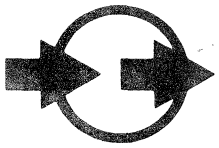
MODEL TC-120/128 TAPE CONTROLLER
HARDWARE MANUAL



western peripherals™

Division of WESPERCORP

14321 New Myford Road • Tustin, California 92680 • (714) 730-6250 • TWX: 910 595-1775 • Cable: WESPER

(5)

MODEL TC-120/128 TAPE CONTROLLER
HARDWARE MANUAL

PUBLICATION NUMBER

01200146 C

western peripherals

14321 MYFORD ROAD
TUSTIN, CALIFORNIA 92680

PRINTED IN U.S.A.

February, 1981

PREFACE

This manual provides information necessary for the installation and maintenance of the Western Peripherals Model TC-120/128 Tape Controller, used with Data General or Data General-emulating computers.

The manual is divided into the following sections:

Section I	General Description
Section II	Installation
Section III	Programming
Section IV	Theory of Operation

SECTION I

GENERAL DESCRIPTION

TABLE OF CONTENTS

SECTION I

GENERAL DESCRIPTION

1.1 DESCRIPTION OF EQUIPMENT

1.2 The Western Peripherals Model TC-120/128 is a universal magnetic tape controller/formatter which is hardware and software compatible with the Data General family of computer systems, providing both NRZI and phase encoded (PE) format capability in a single embedded printed circuit board. The controller is also compatible with all other computers emulating the Data General computer family, using the standard-sized 15 inch x 15 inch circuit boards. The controller contains all interface, control, status, and formatting electronics to emulate the Data General tape subsystem and installs directly into any available card slot in the computer or expansion chassis. The controller board interfaces with the standard backplane and, using a special connector, interfaces to the tape drives through the rear of the computer. Three ribbon cables interconnect the controller with the tape drives through cable adapters, which also provide daisy-chaining capabilities for multiple drive installations.

1.3 DRIVE COMPATIBILITY

1.4 The controller will handle up to eight industry-compatible (IBM/ANSI) read-after-write (dual gap) tape drives. The controller is capable of handling tape drives in varying combinations of speeds, densities, and formats. The controller can select either

of two switch selectable speeds in the range from 6.25 to 125 inches per second (ips).

1.5 Single or dual density NRZI and PE tape drives may be used with densities of 200, 556, or 800 bits per inch (bpi) NRZI 7-track,800 bpi NRZI 9-track, and 1600 bpi PE 9-track (PE mode not available in Model TC-128. Software density control is available for dual density operation. The controller is compatible with all industry-standard tape drives.

1.6 OTHER FEATURES

1.7 The controller is compatible with the I/O bus and with existing magnetic tape software, utilizing the standard magnetic tape controller registers. Enhancements of the standard registers provide other features which add to the usefulness of the controller. Transfers of register information between the tape controller and the computer are made under I/O transfer control via device code #22. Device code #62 may be used for a second tape system if over eight tape drives are used or other system requirements are such that a second controller must be used. The device code may be changed by moving a jumper. Data transfers are in a 16-bit word format via the bus.

1.8 In 7-track, 4-6-6 bit packing allows a full 16-bit word memory dump transfer to and from magnetic tape. Accomplished without special software, the automatic read and write on-the-fly feature allows non-stop operation when doing consecutive read or write operations. The controller writes and recognizes IBM/ANSI-compatible end-of-file tape marks.

The controller provides an "EDIT" feature which allows a record anywhere on a previously recorded tape to be replaced with an updated record.

1.9 66 bytes of data buffering provide flexibility in assigning priorities when programming data transfers to the computer. The tape motion control, Cyclic Redundancy Check character (CRC) and the Longitudinal Redundancy Check character (LRC) generation, LRC checking, inter-record gap generation and status reporting are included. All write clocks and delay times are derived from a crystal-controlled oscillator. No screwdriver adjustments are required or provided. While the controller can read or write only in the forward direction, it can space (or move to a new position) in both directions.

1.10 The controller may address up to eight drives but can only read, write or space one drive at a time, except for the Rewind Command. This function requires only initiation by the controller. That transport can then be left to rewind while the controller services another drive.

1.11 Programmed I/O transfer instructions are used to specify the starting word address in computer memory, the number of words to transfer, the drive number, and the function to be performed. Programmed I/O transfer instructions are also used to transfer status and address data from the tape controller to the computer. Data word transfers during read and write operations are accomplished by the controller, using the computer's data channel process.

1.12 SPECIFICATIONS

1.13 The following information summarizes the specifications of the tape controller.

1. Computer Interface
   a. Compatibility - The controller is fully hardware and software compatible with the Data General computer family and all other computers emulating Data General computers.
   b. Emulation - The controller emulates the standard Data General tape subsystem.
   c. The controller interfaces directly with the I/O bus through a standard board slot.
   d. Controller Bus Location - The controller may be located in the bus in any slot after the Processor, Memory, and Terminal I/O boards. Bus priority signals must be available to the controller.
   e. Bus Loading - One bus load, using DG-compatible interfacing circuitry.
   f. Tape commands:
      Write
      Read
      Rewind
      Space Forward
      Space Reverse
      Write End-of-File Mark
      Erase

g. Other Mode Controls and Registers:

Memory Address

Word Count

Select Threshold Two

Select Edit Mode

Select Density

Select Pack Mode (7 track 4-6-6 memory dump mode)

Select Even Parity (7 track only)

Select Unit Number

Select Test Mode

h. Controller status:

Error Flag

Data Late

Rewinding

Illegal

High Density

Parity Error

End-of-Tape

End-of-File

Load Point

9-track

Bad Tape

Start-End/Identification Status

First Character Detected

File Protected

Odd-Length Record

Tape Unit Ready

Memory Address

Maintenance Register (CRC-LRC)

i. Device Code:

Standard - 22

Alternate - 62

2. Format Compatibility

Fully compatible with the industry-standard IBM/ANSI digital tape recording format as described in ANSI specifications X3.22-1973 and X3.39-1973.

3. Drive Compatiblity

a. Designed to be compatible with the industry standard drives

b. Read-after-Write only (dual gap head)

c. Single or dual density (operator or software switchable)

4. Tape Speed

6.25 ips, 12.5 ips, 18.75 ips, 25 ips, 37.5 ips, 45 ips, 75 ips, 125 ips. Any two speeds may be set through switches on the controller board. For the P.E. format, the speed difference is limited to: 6.25-18.75 ips, 12.5-37.5 ips, 12.5-45 ips, 18.75-45 ips, 25-75 ips, or 75-125 ips.

5. Format and Density

a. NRZI 7-Track - 200/556/800 BPI

b. NRZI 9-Track - 800 BPI

c. PE 9-Track - 1600 BPI (Not available in Model TC-128)

6. Data Transfers

   a. 9-Track

      The eight data bits of each tape character are transferred to or from the bus as a 16-bit computer word.

   b. 7-Track

      (1) Unpacked (normal mode)

         Tracks B, A, 8, 4, 2 and 1 contain the 6-bit tape characters. Two tape characters are transferred to the CPU for each computer word.

      (2) Packed (4-6-6 memory dump mode)

         One 4-bit and two 6-bit tape characters are transferred for each computer word.

   c. Bus transfers for register information or tape data consist of 16-bit word transfers.

7. Drive Configuration

   a. Up to eight drives in daisy chain configuration

   b. One or two tape drive speeds. (All 7-Track drives must be assigned to Speed "A".)

   c. Single or multiple formats and densities on the daisy-chain.

8. Hardware

   a. Single standard-sized printed circuit board mounted within the computer's card cage (or expansion cabinet)

b. Computer backplane adapter/connector board (Eclipse computers require a special backplane adapter because of limited space)

c. Three interface cables and adapter boards per tape drive

9. Other Features

a. Edit mode for correcting pre-recorded tapes

b. Crystal controlled clocks

c. Phase locked loop read tracking in the PE mode

d. No screwdriver adjustments

10. Error Handling

a. Generates and checks vertical parity, LRC, preambles and postambles

b. Generates CRC characters

c. Detects dead track errors

d. Corrects PE single channel dropouts

11. Data Buffering

The internal buffer between the bus and the tape drive provides 66 bytes of buffering to allow for transfers between the controller and the tape drive during times that the computer bus is unable to service the controller. All data contained in the buffer will automatically be transferred before the operation is aborted. During read operations, the buffer allows a check of false postambles in 9-track PE mode when a single dead track occurs. During read operations, the buffer must be emptied within the maximum times

specified below, otherwise a data late error condition is reported.

Maximum Time After End of Record

Tape Speed	7-Track	9-Track NRZI	9-Track PE
12.5 ips	15.00 ms	3.00 ms	4.10 ms
25.0 ips	7.50 ms	1.50 ms	2.05 ms
37.5 ips	5.00 ms	1.00 ms	1.37 ms
45.0 ips	4.17 ms	0.83 ms	1.14 ms
75.0 ips	2.50 ms	0.50 ms	0.68 ms
125.0 ips	1.50 ms	0.30 ms	0.41 ms

12. Non-Stop "On-the-Fly" Tape Operation

    This feature provides continuous tape motion when consecutive tape commands require tape motion in the same direction on the same tape drive. Under these conditions, the controller will time through the inter-record gap (IRG) in the read mode, or will write the IRG in the write mode and execute the next command without stopping the tape.

13. Power Requirements

    a. Source - Computer or Expansion Chassis power supply

    b. + 5VDC $\pm$ 5% @ 4.8 amps

       +15VDC $\pm$ 10% @ 50 milliamps (backplane pin A10)

14. Physical Specifications

    a. Size 15-inch square (standard DG-sized) single printed circuit board fits standard Data General I/O bus card slot

b. Weight (approximate)

   a. Controller Board 30 oz. (0.85 kg)

   b. Cables and Adapters 26 oz. (0.74kg) per drive

c. Environment

(1) Operational Temperature	0 to 55 degrees C
(2) Storage Temperature	10 to 70 degrees C
(3) Relative Humidity	10 to 90 percent (without condensation)

SECTION II

INSTALLATION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION II

INSTALLATION

2.1 GENERAL INFORMATION

2.2 This section provides information necessary to successfully set up and install the TC-120 Tape Controller into the Data General-type computer system. This information is essential for the initial installation and will also be valuable when the controller is reinstalled after repair.

2.3 The controller is a single printed circuit board that plugs directly into a standard I/O bus card slot in the computer mainframe or in an expansion chassis. Cable assemblies and adapters are provided for interfacing the controller with the drives. (Interface to be specified by the customer at the time of purchase). All dc power required for the operation of the controller is received from the power supply of the host computer system via the backplane connector.

2.4 UNPACKING AND INSPECTION. After removal of the controller components from the shipping containers, visually inspect them for physical damage. Check off each item on the enclosed packing list. In case of damage, retain all packaging and notify the carrier to make a report. Be sure all minor parts and small items are found before discarding any shipping material.

2.5 SYSTEM COMPONENTS. Check the equipment supplied to ensure that all necessary items are included:

1. Tape controller board

   Including proper VCO Speed Chip at location 2N (for PE operation).

   See Table 2-2 for part identification.

2. Backplane connector - adapter.

3. Drive Cable(s), one set per drive.

   For control, write, and read functions.

4. Adapter Paddleboards (3), one set per drive:

   Control Paddleboard

   Write Paddleboard

   Read Paddleboard

   Including:

   Terminators (on the Write and Control Paddleboards)

   Drive Select Jumpers (on the Control Paddleboard)

   See Figure 2-7 for part identification.

5. Program Tapes:

   Diagnostic Program Tape

   Reliability Program Tape

6. Documentation:

   Hardware Manual

   Logic Manual

   Diagnostic Manual

   Instruction Reference Card

7. Other items which should be available:

   Computer

   Tape drives

   Loading device for diagnostics

2.6 PREPARATION

2.7 Locate the position in the computer where the controller will be installed. Remember that the location in the system determines the priority for data channel and interrupt activity. The tape controller usually works well if placed anywhere in the system. Check the cabling distance to the first drive and to any daisy-chained drives, verifying that all cable lengths will be adequate, allowing for proper service loops. Refer to the drive manual to install the drives. The computer and drives must be prepared and checked-out before the controller can be expected to operate.

2.8 SYSTEM SET-UP

2.9 The tape system must be set up properly either when installing the system or after servicing. Proper set-up includes: (1) setting the Speed Switches to the speed of the drives, (2) installing the correct VCO Speed Chip, and (3) checking the backplane priority jumpers. (4) Each set of Tape Drive Adapter Paddleboards must have the proper termination (on the last drive), a Drive Select Jumper (except single drive installations), and Configuration Switch selections. Installation is complete when the system components are plugged in and interconnected. A re-check of the installation ensures that no item is overlooked. The procedures to set-up and install the controller are in the paragraphs that follow. Locations of installation features of the controller board are shown in Figure 2-1. A complete system

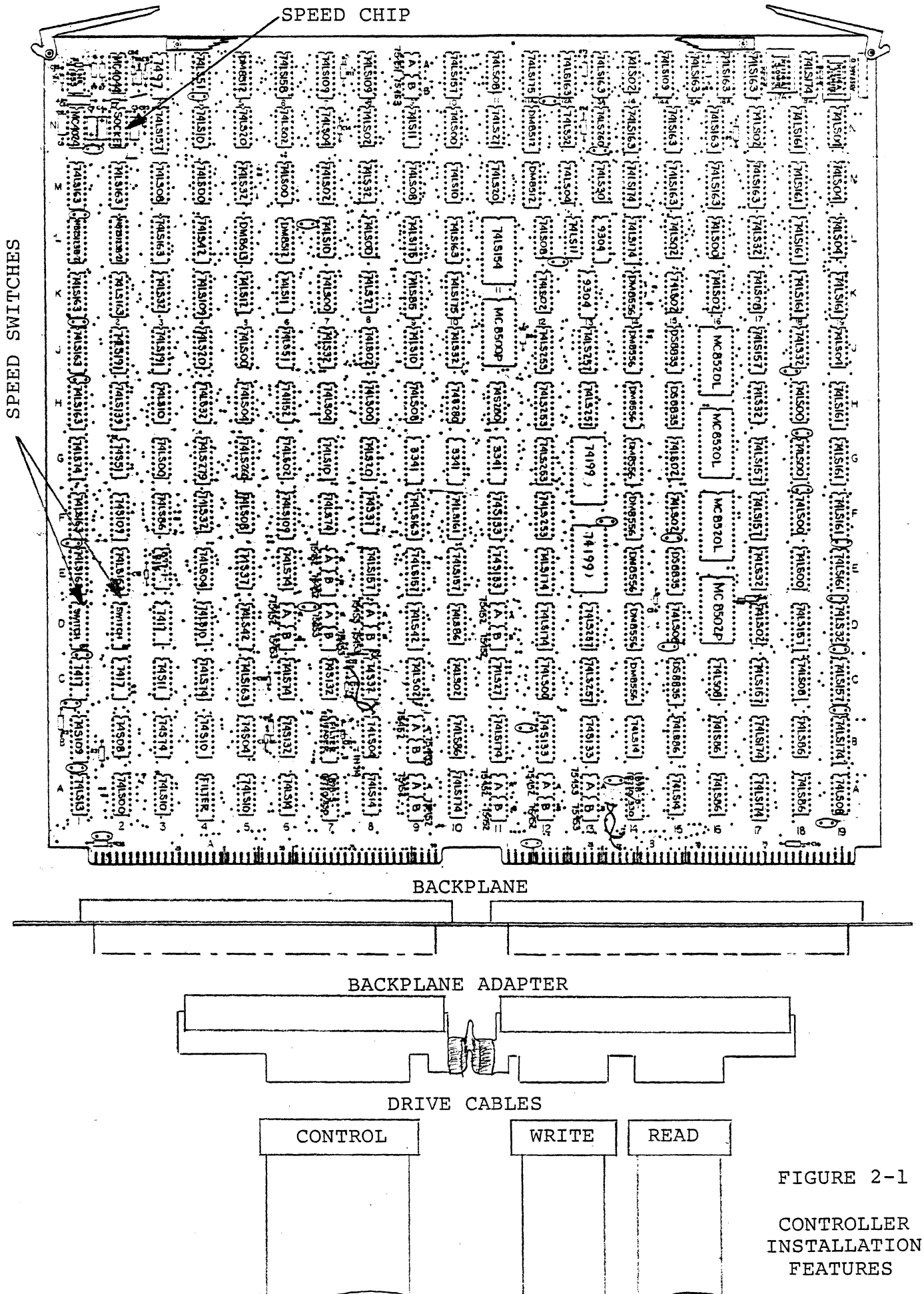


FIGURE 2-1

CONTROLLER INSTALLATION FEATURES

installation is shown in Figure 2-2. Also, check at the rear of the manual for special information which may be pertinent to your installation.

2.10 TAPE SPEED SELECTION. Tape drive speed information is provided to the controller by the code placed in the two speed switches and, for PE, the speed chip placed in the socket at location 2N. Two speed switches are provided for dual speed operation. The switches are located at D1 and D2 as shown in Figure 2-1. The switch module at location D1 selects the primary speed (Speed A) and the switch module at location D2 selects the alternate speed (Speed B). Table 2-1 provides the switch settings for each speed.

2.11 CONFIGURING THE SYSTEM FOR DUAL SPEED OPERATION. 9-track drives of one speed may be assigned to Speed A and 9-track drives of a second speed may be assigned to Speed B. However, all 7-track tape drives must operate at the speed selected for Speed A. A switch on the Control Adapter Paddleboard in each 9-track drive will be set to select either Speed A or Speed B. Set the speed switches as shown in Table 2-1 and record your Speed A and Speed B selections to avoid confusion when setting up the tape drives.

2.12 CONFIGURING THE SYSTEM FOR SINGLE-SPEED OPERATION. For systems using only one tape speed, set both speed switches identically, as shown in Table 2-1. In this configuration, the speed selection switch on the Control Adapter Paddleboard cannot be set wrong for 9-track drives.

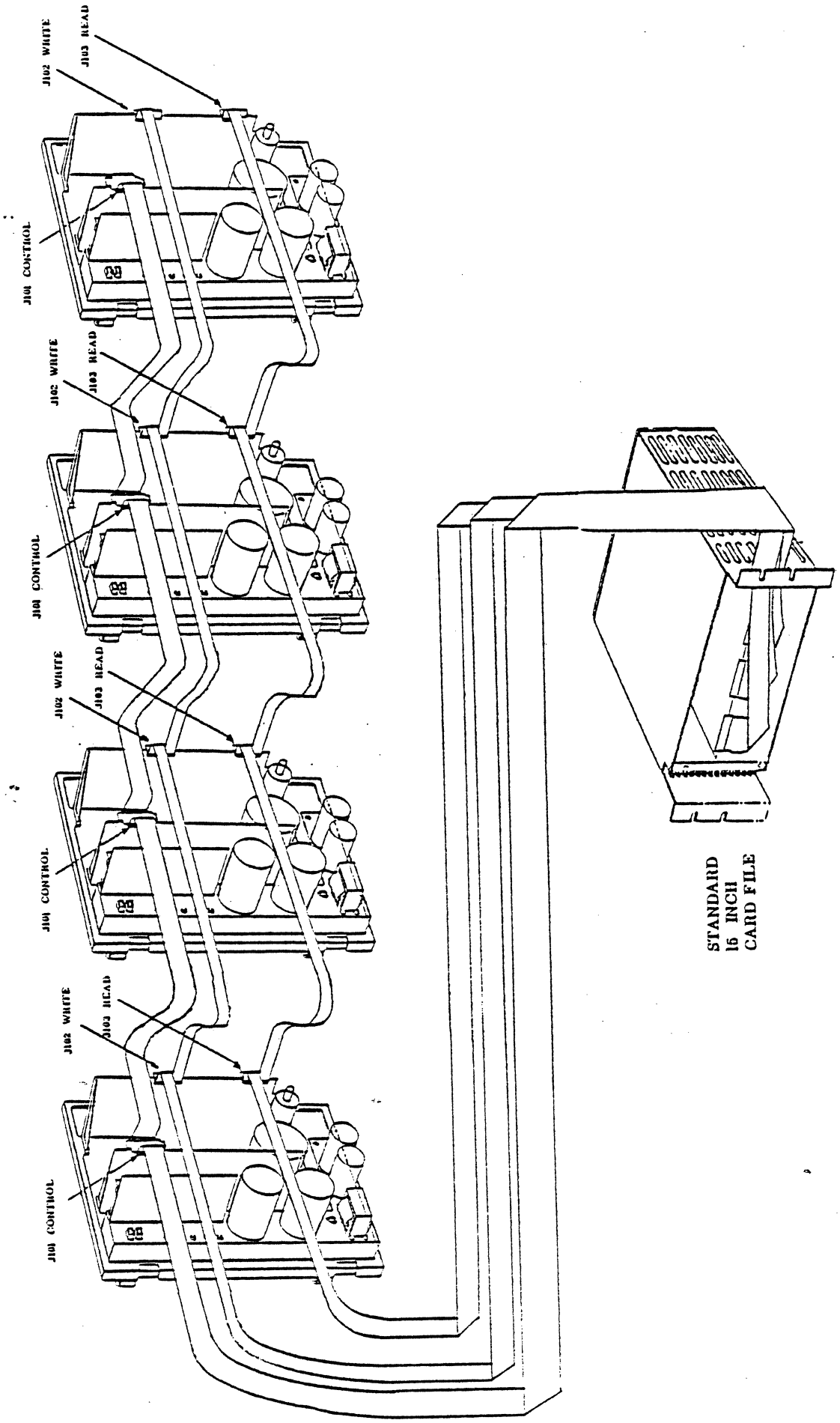


Figure 2-2 Example of Typical System Installation

TAPE SPEED								
SWITCH POSITIONS	6.25 IPS	12.5 IPS	18.75 IPS	25 IPS	37.5 IPS	45 IPS	75 IPS	125 IPS
1	ON	ON	ON		ON			
2	ON		ON				ON	
3				ON	ON		ON	
4		ON	ON	ON	ON	ON	ON	ON
5	ON	ON	ON		ON	ON		
6	ON		ON	ON				
7		ON						
8	ON							

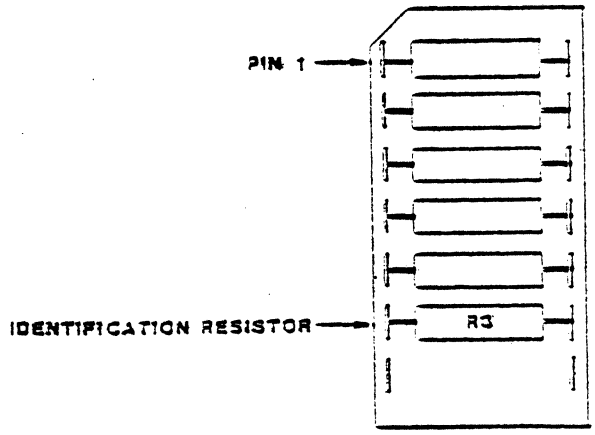
SPEED A: LOCATION D1 SPEED B: LOCATION D2

Note: All other switches are "OFF"

Table 2-1 Speed Selection

2.13 VCO SPEED CHIP (FOR PE OPERATION). In addition to proper speed switch settings, proper PE operation requires insertion of the correct speed chip for the read tracking oscillator (VCO). Table 2-2 provides the part number of each speed chip. The speed chip supplied with each controller when shipped is for the speed specified by the customer at the time of purchase. (Other speed chips are available from the factory). Ensure that the correct part is properly installed in location 2N of the controller. When operating with two PE tape speeds, ensure that both tape speeds are within the limits of the selected speed chip.

NOM. SPEED	SPEED RANGE (IPS)	SPEED CHIP PART NO.	SPEED CHIP IDENTIFICATION (SEE R3)
12.5	6.25 - 18.75	120023-01	RED - VIO - RED
25	12.5 - 37.5	120023-02	BRN - ORG - RED
37.5	12.5 - 45	120023-03	WHT - BRN - BRN
45	18.75 - 45	120023-04	VIO - GRN - BRN
75	25 - 75	120023-05	YEL - ORG - BRN
125	75 - 125	120023-06	ORG - BLK - BRN



Socket at
Location 2N
Board One

Table 2-2 Speed Chips (for PE Operation only)

2.14 EXTENDED ADDRESS FEATURE. For programs which require expanded addressing, jumpers on the controller extend the addressing ragne of the controller from 32K to 64K, but preclude operation in the test mode. To implement this feature, cut the etch which connects A to B (located between 2C and 3C). Also, cut the etch between F and G and add a jumper from F to H (located between 14K and 15K). Note: The Reliability program will not operate on device code 62. Reinstall the jumper to run the Reliability program or patch the program to run device code 62. (This change is not compatible with some programs.)

2.15 EXPANDED WORD COUNT FEATURE. For programs which require expanded word count capability, jumpers on the controller extend the word count register from 12 bits to 16 bits. To implement this feature cut the etch connecting C to D (located between 14J and 15J) and add a jumper from C to E (located between 14K and 15K). (This feature is not compatible with some programs.)

2.16 DEVICE CODE SELECTION. Normally, the Tape Controller is assigned to device code 22, (Mnemonic MTA). A second Tape Controller, if used is assigned to alternate device code 62. To make this change, cut the etch (or remove the jumper) between jumper points "M" and "N". This jumper may be found between location 3F and 4F.

2.17 CONTROLLER INSTALLATION

2.18 Ensure that any keys in the selected backplane connector match the keying slots in the controller. Remove all extra keys from the slot. Place the controller board into the assigned card slot in the computer, assuring that the board seats properly and makes good connection.

2.19 PRIORITY JUMPERS. The data Channel Priority and the Interrupt Priority lines are daisy-chained to the I/O devices. As shown in Figure 2-3, each device receives these signals on pins A94 and A96 and sends these signals from pins A93 and A95 to the next device. There can be no break in the chain throughout the I/O devices. A previously unused card connector may have jumpers across these pins. Remove these jumpers from across the controller's backplane connector pins and check that the priority lines are daisy-chained from the CPU through the devices.

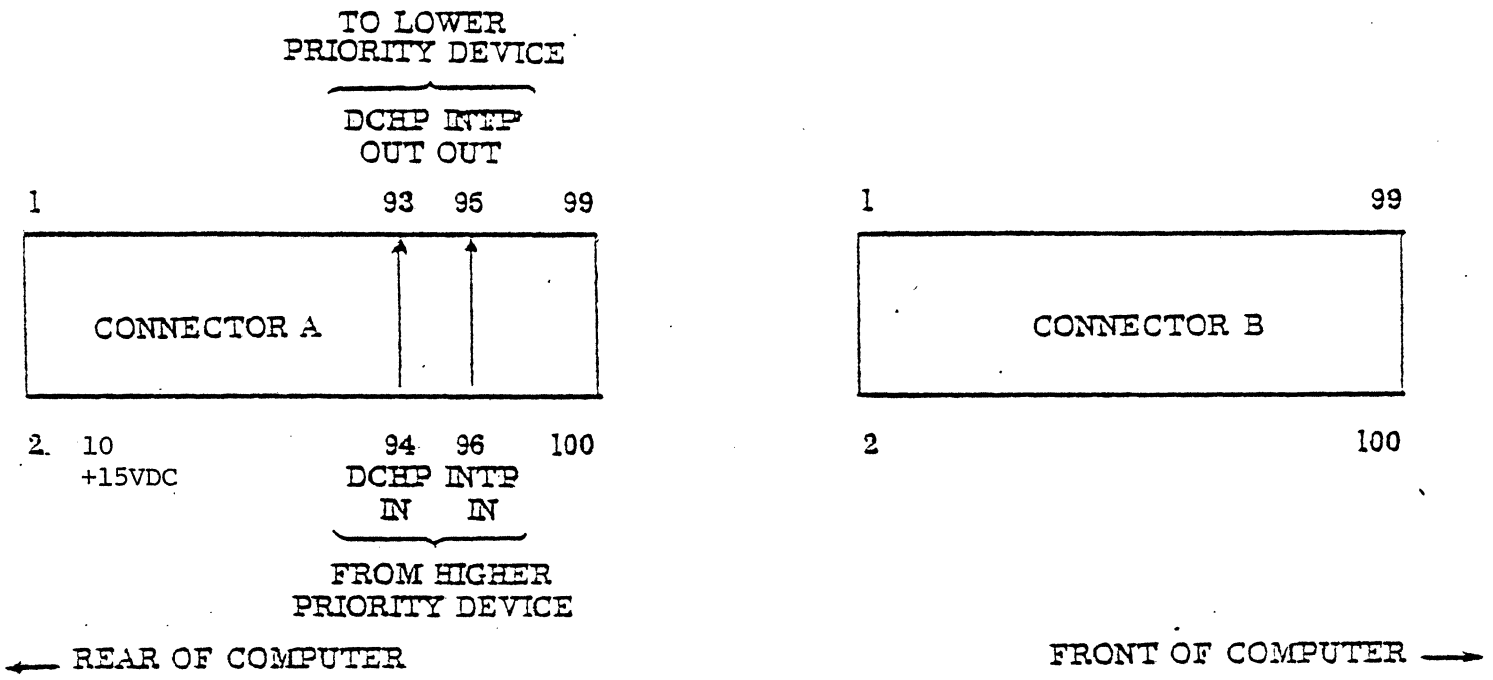


Figure 2-3 Computer Backplane Connector

2.20 OTHER BACKPLANE CONSIDERATIONS. Be certain that the backplane supplies +15VDC on backplane connector pin A10. On some processors this voltage is not supplied to the upper slots and must be wired-in for operation of the tape controller in these locations. Solder this connection as close to the board as possible. The computer's I/O bus must also have proper termination.

2.21 CABLING. A connector adapter assembly provides the interface from the CPU backplane connector to the tape cables and may be installed as follows:

1. Remove or relocate any wires located on the backplane connector pins for the tape controller including wires placed there as a tie point and wires used for a device

which previously occupied that slot. The controller uses all unassigned backplane pins, therefore, no other connections to these pins should be wired to the card slot assigned to the controller. (See Table 2-3 and 2-4) If +15 volts has to be wired to Pin A10, it should be soldered close to the computer backplane. Remove any excess solder from the pins and straighten any bent pins.

2. Attach the adapter connectors to the pins of the backplane connectors, carefully observing pin assignments marked on the connectors. (See Figure 2-4 and 2-5) Seat the connectors firmly on the backplane pins.
3. Neatly dress and tie all cables so that the installation appears orderly and professional.

TABLE 2-3
NOVA TAPE INTERFACE FOR
NOVA, NOVA 1200, NOVA 800, SUPER NOVA, AND SUPER NOVA SC

Signal	Level *	Direction *	Panel Pin	External Bus Pin
GND				1
CLR	H	D	A50	2
DATAO	L	B	B62	3
DATA1	L	B	B65	4
DATA2	L	B	B82	5
DATA3	L	B	B73	6
DATA4	L	B	B61	7
DATA5	L	B	B57	8
DATA6	L	B	B95	9
DATA7	L	B	B55	10
DATA8	L	B	B60	11
DATA9	L	B	B63	12
DATA10	L	B	B75	13
DATA11	L	B	B58	14
DATA12	L	B	B59	15
DATA13	L	B	B64	16
DATA14	L	B	B56	17
DATA15	L	B	B66	18
DATIA	H	D	A44	19
DATIB	H	D	A42	20
DATIC	H	D	A54	21
DATOA	H	D	A58	22
DATOB	H	D	A56	23
DATOC	H	D	A48	24
DCHA	L	D	A60	25
DCHI	H	D	B37	26
DCHMO	L	P	B17	27
DCHM1	L	P	B21	28
DCHO	H	D	B33	29
DCHP IN	L	D	A94*)	30
DCHP OUT	L	D	A93*)	
DCHR	L	P	B35	31
DSO	L	D	A72	32
DS1	L	D	A68	33
DS2	L	D	A66	34
DS3	L	D	A46	35
DS4	L	D	A62	36
DS5	L	D	A64	37
INTA	H	D	A40	38
INTP IN	L	D	A96*)	39
INTP OUT	L	D	A95*)	
INTR	L	P	B29	40
IOPLS	H	D	A74	41
IORST	H	D	A70	42

TABLE 2-3 (Continued)

Signal	Level *	Direction *	Panel Pin	External Bus Pin
MSKO	L	D	A38	43
OVFLO	H	D	B39	44
RQENB	L	D	B41	45
SELB	L	P	A82	46
SELD	L	P	A80	47
STRT	H	D	A52	48
POWER ON	H	D		49
NOT USED				50

*For the two pairs of priority-determining signals, the in signal comes from the processor or the preceding device; the out signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), Jumper Pin A93 to A94 and A95 to A96 to maintain bus continuity.

Pin 1 of the external bus is grounded and the groud wires from all twisted pairs are connected to it. The Power-On line cannot be used to supply power to any external device; it is available only for picking up relays for remote power turn-on. Pin 50 is not used.

**LEGEND: H = HIGH L = LOW B = BI DIRECTIONAL D = FROM PROCESSOR TO DEVICE P = FROM DEVICE TO PROCESSOR

TABLE 2-4
NOVA TAPE INTERFACE FOR
NOVA 1210, NOVA 1220, AND NOVA 820

Signal	Level *	Direction *	Panel Pin	External Bus SIG	External Pin GND
GND				AF	50
CLR	H	D	A50	K	9
DATA0	L	B	B62	w	41
DATA1	L	B	B65	z	44
DATA2	L	B	B82	AD	48
DATA3	L	B	B73	AB	46
DATA4	L	B	B61	v	40
DATA5	L	B	B57	r	36
DATA6	L	B	B95	AE	49
DATA7	L	B	B55	n	34
DATA8	L	B	B60	u	39
DATA9	L	B	B63	x	42
DATA10	L	B	B75	AC	47
DATA11	L	B	B58	s	37
DATA12	L	B	B59	t	38
DATA13	L	B	B64	y	43
DATA14	L	B	B56	P	35
DATA15	L	B	B66	AA	45
DATIA	H	D	A44	F	6
DATIB	H	D	A42	E	5
DATIC	H	D	A54	M	11
DATOA	H	D	A58	P	13
DATOB	H	D	A56	N	12
DATOC	H	D	A48	J	8
DCHA	L	D	A60	R	14
DCH1	H	D	B37	k	31
DCHM0	L	P	B17	d	26
DCHM1	L	P	B21	e	27
DCHO	H	D	B33	h	29
DCHP IN	L	D	A94*)	b	24
DCHP OUT	L	D	A93*)		
DCHR	L	P	B35	j	30
DS0	L	D	A72	X	20
DS1	L	D	A68	V	18
DS2	L	D	A66	U	17
DS3	L	D	A46	H	7
DS4	L	D	A62	S	15
DS5	L	D	A64	T	16
INTA	H	D	A40	D	4
INTP IN	L	D	A96*)	c	25
INTP OUT	L	D	A95*)		
INTR	L	P	B29	f	28

TABLE 2- 4 (Continued)

Signal	Level *	Direction *	Panel Pin	External Bus SIG	External Pin GND
IOPLS	H	D	A74	Y	21
IORST	H	D	A70	W	19
MSKO	L	D	A38	C	3
OVFLO	H	D	B39	1	32
RQENB	L	D	B41	m	33
SELB	L	P	A82	a	23
SELD	L	P	A80	Z	22
STRT	H	D	A52	L	10
POWER ON	H	D		B	2
GND				A	1

*For the two pairs of priority-determining signals, the in signal comes from the processor or the preceding device; the out signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), Jumper Pin A93 to A94 and A95 to A96 to maintain bus continuity.

The numbered pins of the external bus are grounded and the ground wires from all twisted pairs are connected to them. The power-on line cannot be used to supply power to any external device; it is available only for picking up relays for remote power turn-on.

**LEGEND: H = HIGH L = LOW B = BI DIRECTIONAL D = FROM PROCESSOR TO DEVICE P = FROM DEVICE TO PROCESSOR

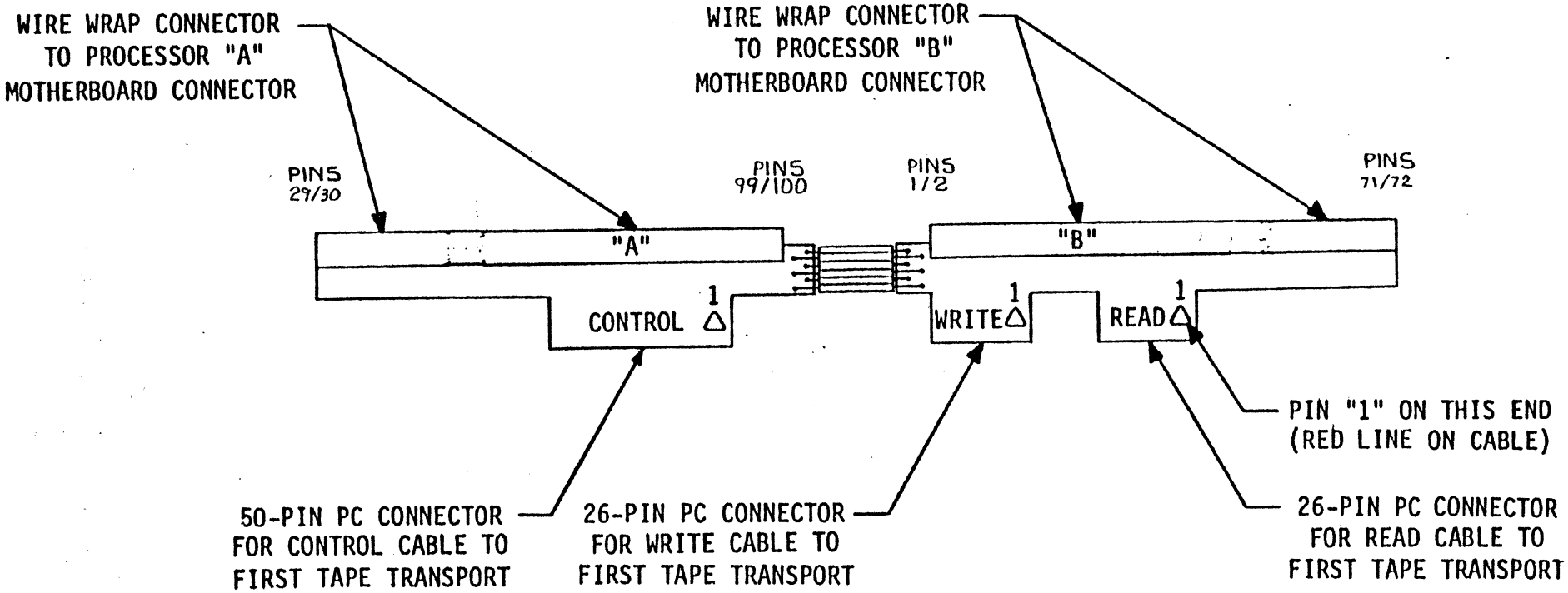


Figure 2-4

Standard Backplane Adapter

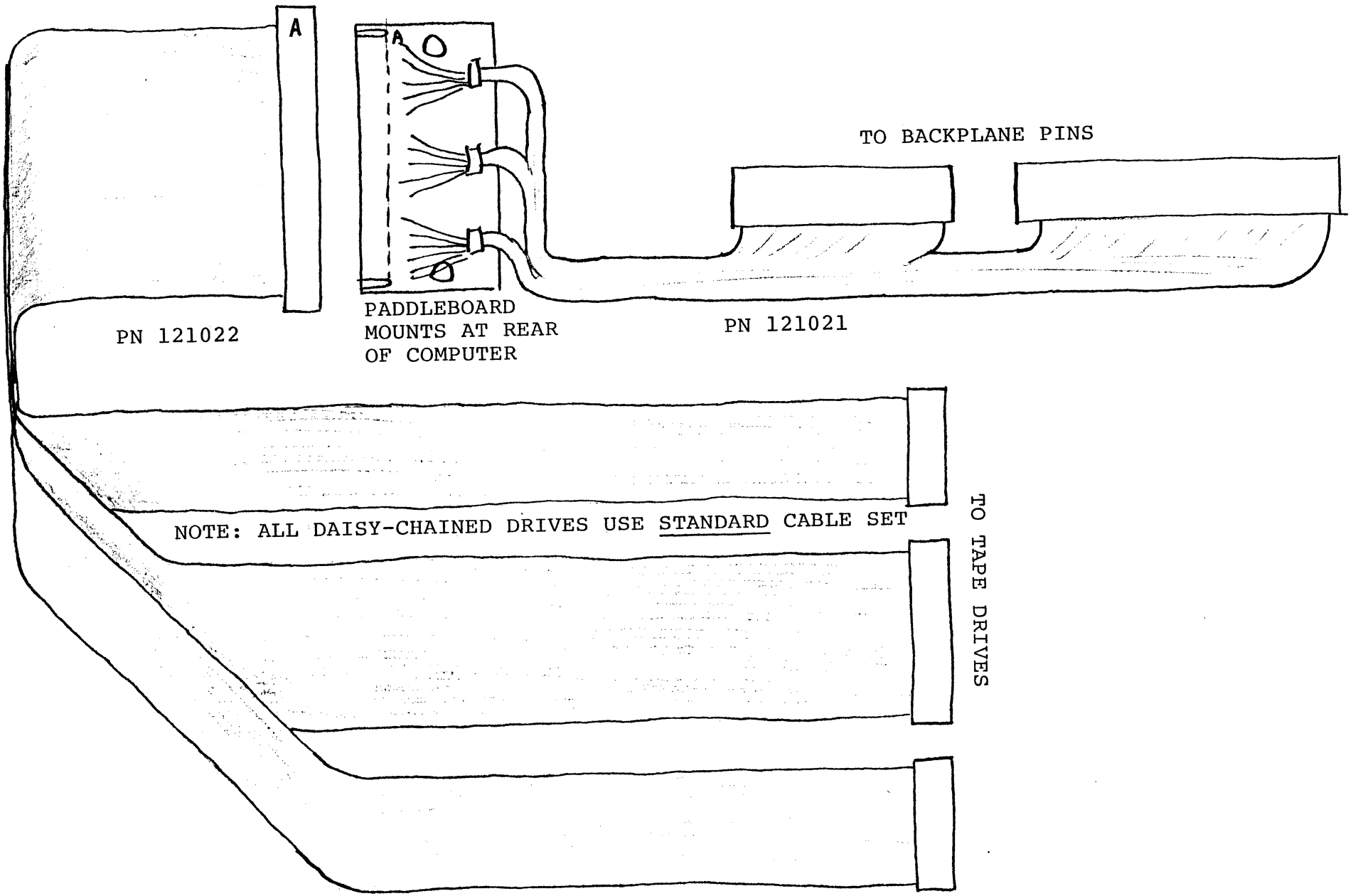


FIGURE 2-5 ECLIPSE CABLES

2.22 CONTROLLER CABLE CONNECTIONS. Locate the following cables:

Description	Conductors	Controller-End Marking
Tape Read Cable	26	Top B2
Tape Write Cable	26	Top B1
Tape Control Cable	50	Top A

Eclipse cable uses a single connnector. (First drive only) The ribbon cables are keyed to prevent incorrect connections. Check the ribbon cable connectors to assure that all keys are in place. Install the Read, Write,and Control cables onto the back-plane connector adapter.

2.23 TAPE DRIVE INSTALLATION

2.24 ADAPTER PADDLEBOARD SET-UP. Locate a set of three Adapter Paddleboards for each tape drive. The Adapter Paddleboards for each drive require proper setup before installation. Setup includes proper termination, switch settings, and installation of drive selection jumper plugs.

2.25 TERMINATORS. Consulting the tape manuals for details, remove all termination devices from each drive. Remove the terminators from the Write and Control Adapter Paddleboards, except the Adapter Paddleboards on the drive located farthest from the controller. See Figure 2-6. Ensure that the last Adapter Paddleboards have the terminators installed as shown.

2.26 CONFIGURATION SWITCHES. Set the switch module on each Control Paddleboard according to the configuration requirements of the tape drive. Switch settings are given in Table 2-5.

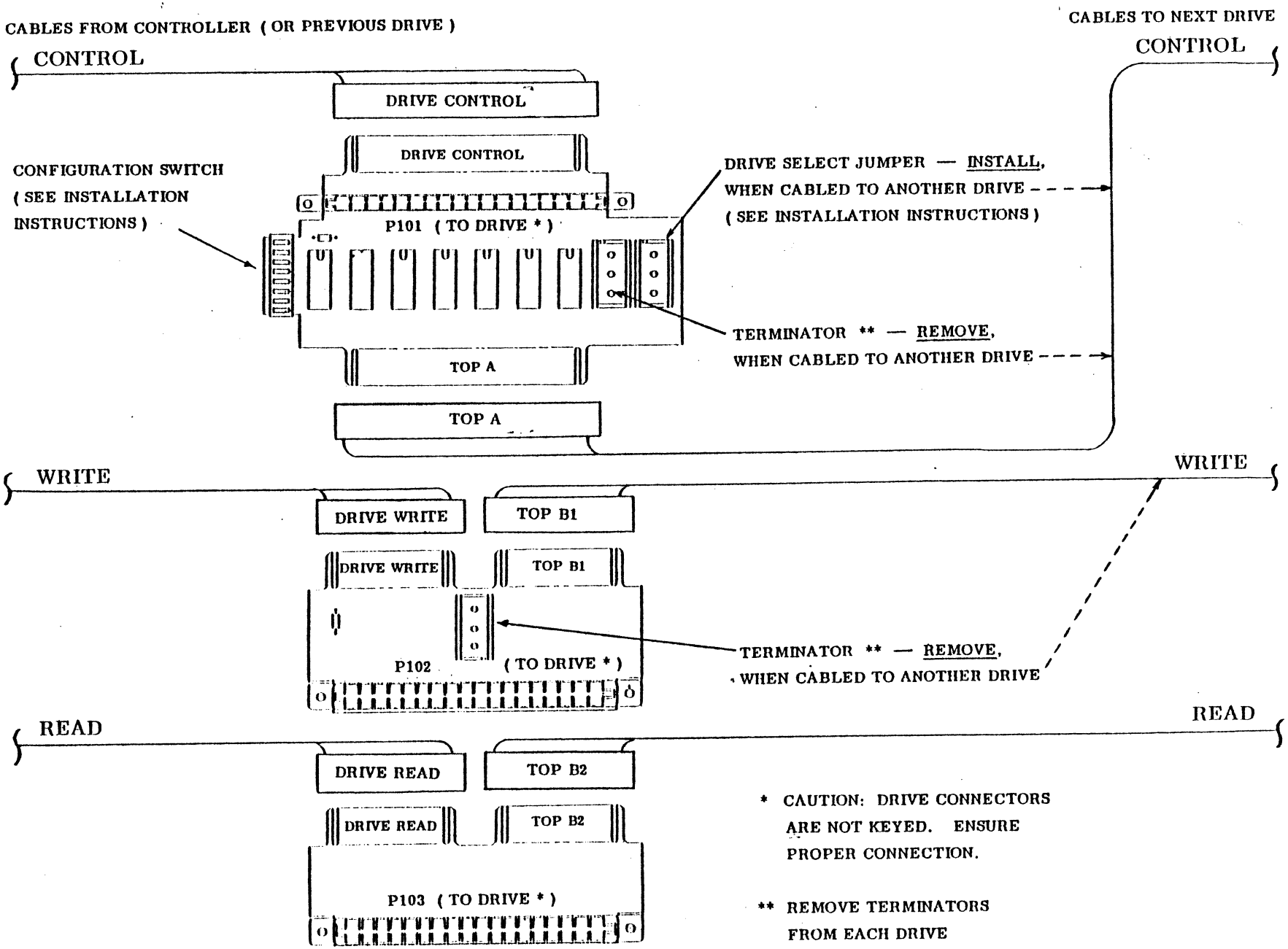


Figure 2-6. Details of Adapter Installation

SWITCH NO.	FUNCTION
1	"ON" for Qantex "OFF" for all other drives
2	"ON" for Kennedy, CDC, or Tandberg drives "OFF' for all other drives
3	"ON" for 7-track drives "OFF" for 9-track drives
4	9-TRACK DRIVE: "ON" for Speed B "OFF" for Speed A 7-TRACK DRIVE: "ON" for 556/800 bpi density "OFF" for 200/556 bpi density
5	Set opposite of Switch 2 (see above)
6	"ON" for 9-track NRZI-only drives "OFF" for all other drives
7	"ON" for dual density or PE drives made by Kennedy, Digidata, or Qantex "OFF" for all other drives
8	Set same as Switch 3 (see above)

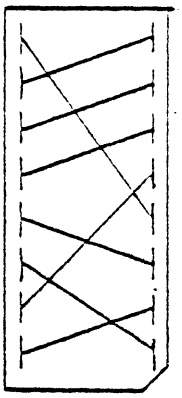
(for assembly numbers 122037, 122038, 122039, and 122044)

Table 2-5 Configuration Switches

2.27 **DRIVE SELECT JUMPERS.** Ensure that the correct Drive Select Jumper is installed in the Control Paddleboards. The last drive does not require a Drive Select Jumper (leaving one installed will have no effect).

1. For tape drives without front panel unit select switches, use jumper part number 122012 as shown in Figure 2-7
2. For tape drives with front panel unit select switches:
   a. Use jumper part number 122010 as shown in Figure 2-7
   b. On drives with Unit Select Switches that receive the select lines from J101, ensure Control Paddleboard Jumpers are installed from P to R (factory etch), N to M, E to F, and G to H. See Table 2-6.
   c. On drives with externally connected Unit Select Switches, connect as shown in Table 2-6.

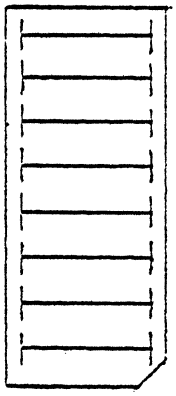
2.28 **TAPE DRIVE INTERCONNECTIONS.** Locate a set of three ribbon cables for each drive (one set is connected to the controller). Check that each connector has its key in place and connect the cables as shown in Table 2-7 and Figures 2-8 and 2-9.



NON-SELECT JUMPER (PN 122012)

For daisy-chained drives

Without front panel Unit Select switches.

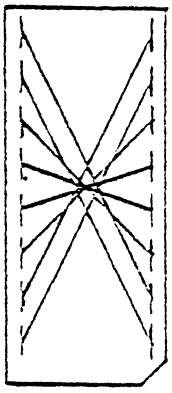


UNIT SELECT JUMPER (PN 122010)

For daisy-chained drives

with Unit Select switch

(Except fourth tape unit)



UNIT SELECT JUMPER (PN 122011)

For daisy-chained drives

with unit select switches

(Install in fourth tape unit)

NOTE: No jumper plug is required on the last tape unit or for single drive installations. However, it should remain in the board for future expansion of the system.

Figure 2-7 Drive Select Jumpers

NOTE: APPLIES TO DRIVE SELECT THUMBWHEEL OPTION ONLY.

Drive Select Line:	Add Jumper:	To Activate J101 Pin:	Connect External Switch To:
Select Ø	P-R (Etch)	J	A
Select 1	N-M	A	B
Select 2	E-F	18	D
Select 3	G-H	V	C
		L	(return line from switch)

Table 2-6 Control Adapter Select Options

(Sequence is repeated for each drive)					
Cables		Paddleboards		Cables	
Controller End	Drive End	Controller End	Daisy Chain End	Controller End	Drive End
Top A	Drive Control	Drive Control	Top A	Top A	Drive Control
Top B1	Drive Write	Drive Write	Top B1	Top B1	Drive Write
Top B2	Drive Read	Drive	Top B2	Top B2	Drive Read

Table 2-7 Connector Legends and Cable Connections

2.29 Connect the Control, Write and Read Adapter Paddleboard connectors to J101, J102, and J013, respectively, on the tape transport. (Reference the tape drive manual for details.) Connect the paddleboards to the drive with care. The green connectors are not keyed to the drive connectors. Therefore, it is possible to (1) install the connector backwards or (2) to place the Adapter Paddleboard on the wrong drive connector (e.g., Read and Write Connectors reversed.) Avoid incorrect connection by (1) verifying the function of each drive connector and (2) physically checking the pin orientation of the mating connectors. If possible, secure the paddleboard connectors to the drive connectors with screws. Neatly dress and tie all cables so the installation appears neat and professional.

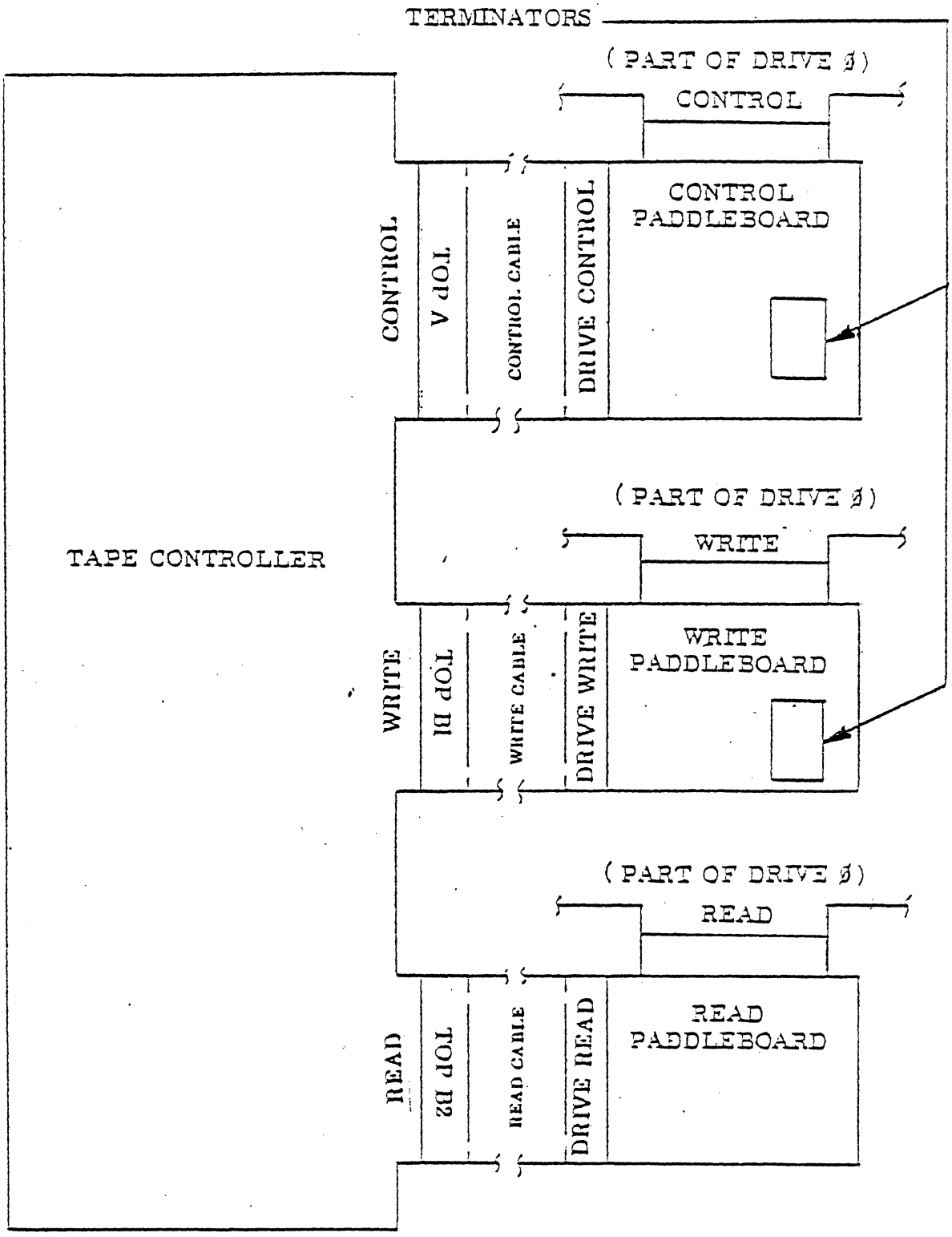


Figure 2-8. Single Tape Drive Connections

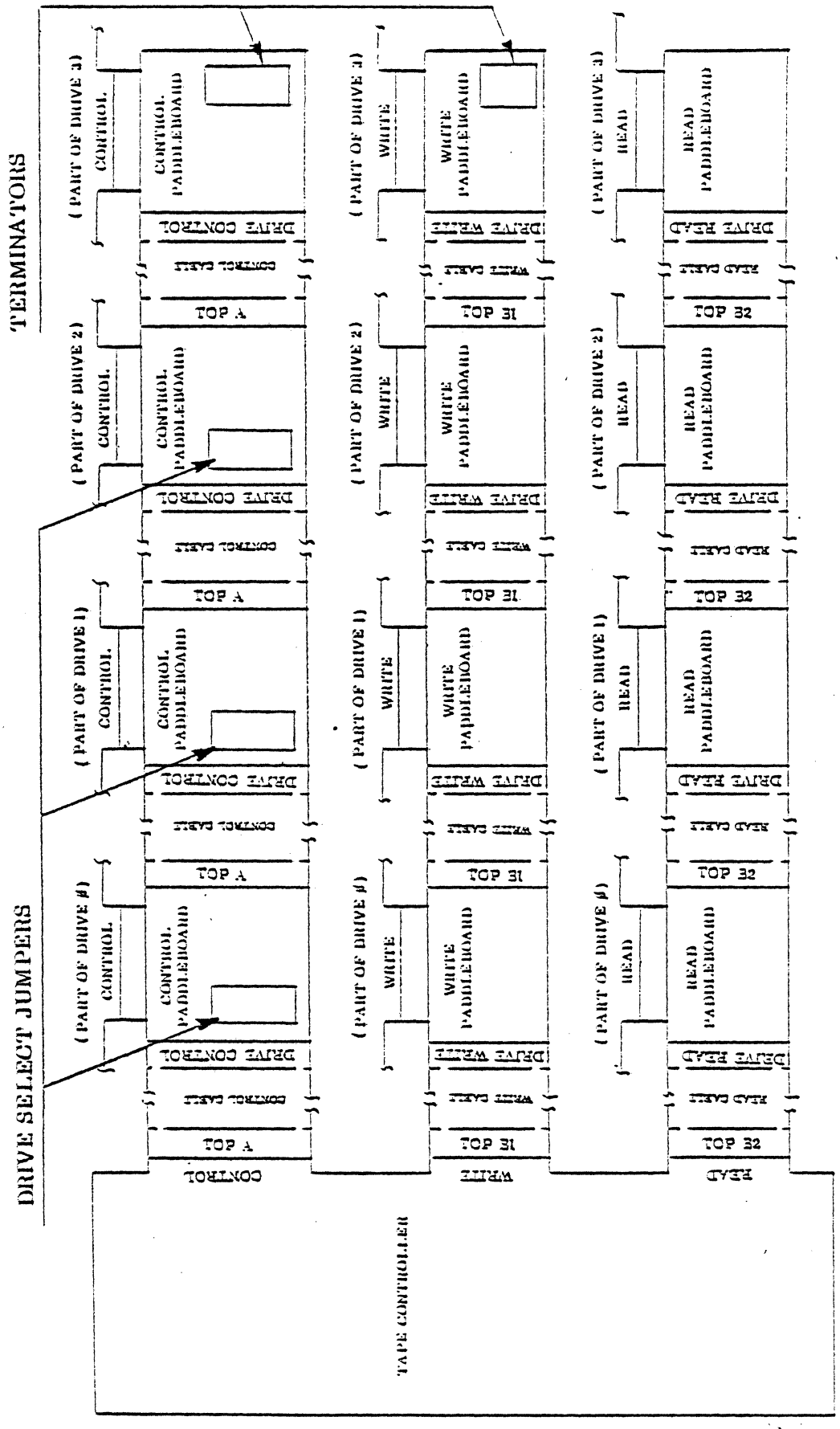


Figure 2-9 Tape Drive Daisy-Chain Connections

2.30 INSTALLATION CHECKLIST

2.31 The installation of the controller is now complete. Double-check your installation before testing and operation.

CHECKLIST

( ) Were all items supplied?

( ) Did you choose a location for the controller which will provide the desired data channel and interrupt priority?

( ) Do all cables reach with adequate service loops?

( ) Are the computer and tape drives ready?

( ) Did you properly set up tape speed including setting Speed A, Speed B, and using the correct VCO Speed Chip?

( ) Did you check the extended address, word count, and device code jumpers?

( ) Did you install the controller correctly?

( ) Did you check the jumpers for the priority lines on the computer backplane?

( ) Did you properly connect the interface adapter to the CPU backplane?

( ) Did you connect the cables properly?

( ) Did you set up the Adapter Paddleboards for proper operation, including:

1. Removing termination devices from each tape drive
2. Removing terminator chips from the Control and Write Adapter Paddleboards, except the last paddleboards in the daisy-chain
3. Setting the configuration switches

4. Ensuring that the correct drive jumpers and options are installed?

( ) Did you connect the ribbon cables to the Adapter Paddleboards at each drive?

( ) Did you connect the Adapter Paddleboards to the tape drives?

WARNING: BEFORE POWERING THE SYSTEM, BE SURE THAT ALL PARTS ARE PROPERLY CONNECTED

The tape system is now ready for testing and operation.

NOTE: Refer to the supplementary information at the back of the manuals for additional advice.

SECTION III

PROGRAMMING

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION III

PROGRAMMING

3.1 SCOPE

3.2 This section contains machine-level programming reference information which describes the registers of the controller. Also contained in this section is information on the operation of the controller, addressing, data transfers, and interrupts. This information will be useful in understanding the operating systems as well as the diagnostic programs. A working knowledge of machine-level programming, along with reference to the information contained in this section, will allow the Customer Engineer to create small diagnostic programs for testing specific functions of the controller.

3.3 PROGRAMMING CONSIDERATIONS

3.4 Information supplied by the program for a tape operation includes the drive unit number, the 2's complement (negative) of the number of words to be processed, an initial memory address for data channel access and the desired function command. For each data transfer, the controller increments the word count (i.e., the negative count of the number of words still to be processed). As each data transfer is completed, the address counter is incremented by one and upon completing the final word in the block, the address

counter is incremented by one while the word counter overflows to zero. When the word count reaches zero, the controller terminates the command (with the address counter pointing to the next address to be processed) and clears BUSY and sets DONE, requesting an interrupt.

3.5 PROGRAM SEQUENCE. Although the program can process data with only one drive at a time, it can rewind the tape on one or more drives simultaneously. After giving a rewind command to the drives, the program can select another drive and issue any command to it. This means that the unit number address and word count information should not be given at the time when the drive is selected for rewind and each time the program wishes to handle a particular drive it must reselect that drive. If several drives are rewinding simultaneously and there is an interrupt, the program should issue a DIA to check status for that drive. To read or write, the program should issue all three commands, DOA, DOB, and DOC, to supply all the necessary information. The order of the instructions is not important, but Start should be given with the last of the three in order for the command to be executed properly.

3.6 The normal programming sequence for operating a single drive is to issue a DOA to select the drive and function, and then issue a DIA to check whether the drive is ready (Status Bit 15). If it is, the program should issue a DOB to set the initial address. Finally, a DOC specifies the word count and starts the operation. For write operations the controller immediately makes data channel requests to load the FIFO before writing begins. Flow charts accompanying this section give examples of programming sequences.

The timing in all cases is dependent upon the transport speed, tape handling characteristics, and density.

3.7 REGISTER TRANSFERS. All command and status information is transferred, with the CPU acting as a "master" device and the controller acting as the "slave". The individual bits within the Command Register control the operations of the device. For example, the command to make the tape system read a block from tape is provided by properly setting bits 10 through 12 in the Command Register. Status conditions are handled by the assignment of bits within the Status Register. All command and status information is written or read by I/O transfer instructions.

3.8 DATA CHANNEL TRANSFERS. Once a function command has been issued to the controller, the operation is executed by the controller, utilizing Data Channel bus transfers to move the data to or from the memory. The Word Count Register and the Memory Address Register are updated throughout the DMA activity. A 32-word FIFO Buffer and the Data Register provide a total of 33 words (66 bytes) of data buffering between tape and data channel. Therefore, the data channel has almost 65 character-times in which to respond to requests by the controller. At the conclusion of an operation, completion is indicated to the CPU through examination of the BUSY and DONE status lines or by utilizing the system interrupts (if enabled).

3.9 TRANSFER ERRORS. The setting of Data Late during a block indicates that information has been lost, but data transfers continue until the controller processes the entire block, at which

time it terminates the command. Also, if the controller reaches the end of the block and an odd number of bytes were read, the controller sets Odd Length Record status.

3.10 INSTRUCTION FORMAT

3.11 The CPU communicates with and maintaines control of the Tape Controller through the use of I/O transfer instructions. Six of these instructions control the transfer of status and command words to or from registers in the controller. Three more of these instructions control Interrupt Acknowledge, Interrupt Mask and I/O Reset. Execution and decoding of each instruction is accomplished in the CPU and causes a control line on the bus to be asserted which initiates a response in the controller. The accompanying table shows the format of these instructions.

1. INSTRUCTION WORD BITS Ø-2 INPUT/OUTPUT INSTRUCTION - These bits indicate that this instruction is an input/output instruction.
2. INSTRUCTION WORD BITS 3-4 ACCUMULATOR DESIGNATION (AC) - These bits designate which one of four accumulator (AC) registers will be used in this instruction.
3. INSTRUCTION WORD BITS 5-7 TRANSFER DESIGNATION - These bits describe the device register involved in the instruction, and also describe Interrupt Acknowledge, Interrupt Priority Mask (mask bit 10), and I/O Reset functions, which are explained in paragraphs to follow.

INSTRUCTION FORMAT AND CODING:

BIT:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	INPUT/OUTPUT INSTRUCTION			ACCUMULATOR (AC)		TRANSFER DESIGNATOR			FUNCTION (F)		DEVICE CODE					
I/O INSTRUCTION	0	1	1													
ACCUMULATOR																
ACC 0				0	0											
ACC 1				0	1											
ACC 2				1	0											
ACC 3				1	1											
TRANSFER DESIGNATOR																
DIA						0	0	1								
DOA						0	1	0								
DIB						0	1	1								
DOB						1	0	0								
DIC						1	0	1								
DOC						1	1	0								
CONTROL FUNCTION																
NONE									0	0						
START									0	1						
CLEAR									1	0						
IOPLSE									1	1						
DEVICE CODE																
22											0	1	0	0	1	0
62											1	1	0	0	1	0
INTA	0	1	1	X	X	0	1	1	X	X	1	1	1	1	1	1
MSKO	0	1	1	0	0	1	0	0	X	X	1	1	1	1	1	1
IORST	0	1	1	0	0	1	0	1	X	X	1	1	1	1	1	1

Table 3-1 Instruction Word Format

5 6 7	Mnemonic	Description
0 0 1	DIA	Data In from Register A (Status)
0 1 0	DOA	Data Out to Register A (Command)
0 1 1	DIB	Data In from Register B (Memory Address)
1 0 0	DOB	Data Out to Register B (Memory Address)
1 0 1	DIC	Data In from Register C (Maintenance)
1 1 0	DDC	Data Out to Register C (Word Count)

4. INSTRUCTION WORD BITS 8 - 9 CONTROL FUNCTION - The four Control Functions which control BUSY and DONE status are described by these bits:

Bits 8 9	Mnemonic	Function
0 0	—	None - No Operation
0 1	S	Start - clears DONE, initiates operation
1 0	C	Clear - clears DONE and BUSY
1 1	P	Pulse - not used

5. INSTRUCTION WORD BITS 10 - 15 DEVICE NUMBER - The device code number is encoded in bits 10-15:

Bits 10 11 12 13 14 15	Device
0 1 0 0 1 0	First Tape Controller (22), Mnemonic MTA
1 1 0 0 1 0	Second Tape Controller (62)

3.12 INTERRUPT ACKNOWLEDGE INSTRUCTION (DIB-, CPU). Interrupts are acknowledged by the CPU through the use of this instruction which asserts the INTA line to the I/O devices. INTA causes the device number to be transferred from the controller to the designated accumulator. The format of the instruction is:

Bit:	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents:	Ø	1	1	X	X	Ø	1	1	X	X	1	1	1	1	1	1

3.13 INTERRUPT MASK INSTRUCTION (DOB-, CPU). Interrupts are selectively disabled in individual devices by this instruction, which asserts the MSKO line to the devices. True bits in the computer word located in the designated accumulator disable interrupts in individual devices. Bit 10 is assigned to the Tape Controller. The format of the instruction is:

Bit:	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents:	Ø	1	1	Ø	Ø	1	Ø	Ø	X	X	1	1	1	1	1	1

3.14 I/O RESET INSTRUCTION (DIC Ø, CPU). I/O devices are reset by asserting the IORST line through the execution of this instruction. The format of this instruction is:

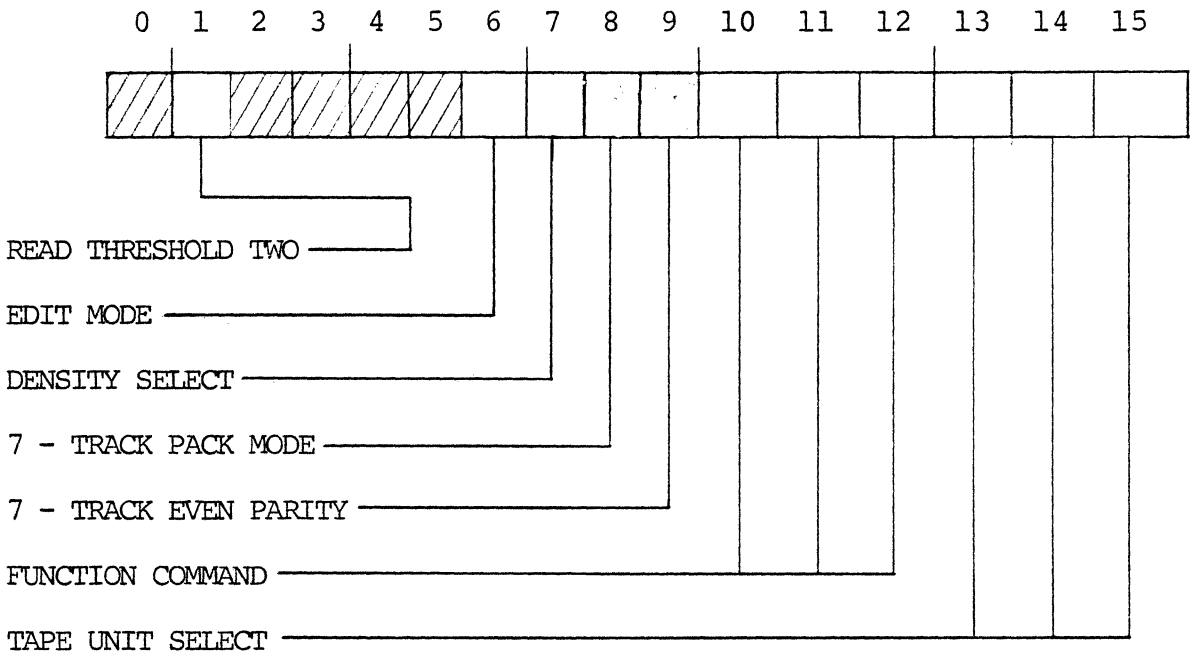
Bit:	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Contents:	Ø	1	1	Ø	Ø	1	Ø	1	X	X	1	1	1	1	1	1

3.15 TAPE CONTROLLER REGISTERS

3.16 OUTPUT REGISTER "A". Using the DOA-,MTA instruction, the CPU selects the function according to the contents of AC bits 10-12, selects the tape unit specified by bits 13-15, and performs the function specified by F.

OUTPUT REGISTER "A" BIT ASSIGNMENTS

(COMMAND WORD)



1. DOA BIT 2 READ THRESHOLD TWO - When reading a block where several retries have failed to recover data, this bit is asserted to reduce the read amplifier threshold level in the tape drive so that subsequent read retries will produce a recognizable data block. This bit remains false for the normal read threshold.
2. DOA BIT 6 EDIT MODE - When bit 6 is set, the Space Reverse operation that follows is performed with special edit timing and the subsequent Write operation is performed with the Overwrite signal to the drive asserted. These operations allow (1) proper head positioning, (2) writing with the erase head off (prevents erasure of other data) and (3) slow turn-on and turn-off of write current.

These activities allow a block in an existing file to be replaced with another block of the same size.

3. DOA BIT 7 DENSITY SELECT - When bit 7 is set, the Density Select signal to the tape drive is asserted. This signal selects PE operation in NRZI/PE drives and (usually) selects high density in 7 track drives. Check your tape drive manual to be certain of tape drive response.

4. DOA BIT 8 7 TRACK PACK MODE - When this bit is set the controller organizes data in one four-bit character and two six-bit characters on tape for each 16-bit computer word. This mode captures all memory bits for "core dump" operations. This bit remains reset for 9-track operations and for normal 7-track packing (two six-bit characters per computer word).

5. DOA BIT 9 7 TRACK EVEN PARITY - This bit, when set, selects even lateral parity required for the 7-track BCD tape format. When this bit is reset, it allows odd parity for normal 9-track operations or the 7-track Binary tape format.

6. DOA BITS 10-12 FUNCTION COMMAND - To perform any operation, the program must select the tape drive while issuing the command. In addition, the program may select threshold, edit, density, packing, or parity and issue word (or record) count and memory address information. All commands are initiated by issuing the Start control function which clears DONE and sets BUSY, placing the controller into operation. At the conclusion of the operation, the

controller clears BUSY and sets DONE, requesting an interrupt unless interrupts are disabled. An exception to the above is the rewind command which does not actually place the controller into operation, but merely issues the command to the tape unit. The function command bits select one of eight command functions, as follows:

Bit 10	Bit 11	Bit 12	
0	0	0	Read
0	0	1	Rewind
0	1	0	No Operation
0	1	1	Space Forward
1	0	0	Space Reverse
1	0	1	Write
1	1	0	Write EOF
1	1	1	Erase

A. Read. The program must specify word count, and an initial address. The controller reads a single record from tape and sends the data via the data channel to the locations that are specified by the address counter until either the end of record is detected or the word counter overflows, whichever occurs first. For operations with variable length records, specifying a larger word count ensures that the entire record will be read. Record length can then be determined by comparing the initial value of the address counter with its final contents, which will be one-greater

than the address to which the last word in the record was transferred. If the record contains an odd number of data characters, the last byte is "right justified" in the final word transferred to memory and odd length status will be set. Data late status during the record indicates that information has been lost, but data transfers will continue until end of record is detected or word count overflow occurs. If the record is a NRZI file mark, its single "data" character is transferred to memory with EOF status indicated.

B. Rewind. This command initiates a rewind operation in the addressed tape drive, which rewinds the tape onto the supply reel at high speed and stops at load point. Start does not affect the controller, but simply initiates the rewind operation in the addressed drive, leaving the controller free for further use by the program.

C. Space Forward. The program should issue a (negative) word count equal to the number of records to be spaced. The controller spaces forward over the given number of records unless it encounters a file mark or the end of tape, in which case it stops at the file mark or at the end of the record in which the EOT marker is encountered. To space over a file, the program can simply issue a zero (maximum) word count.

D. Space Reverse. The program should issue a (negative) word count equal to the number of records to be spaced. If Load Point is true, Start sets Illegal

and DONE, and the controller does not go into operation. Otherwise, the controller spaces reverse over the given number of records, but it stops the tape automatically upon encountering a file mark or the Load Point. To space over a file, the program can simply issue a zero (maximum) word count.

E. Write. The program must specify a (negative)word count, and an initial memory address. If Write Lock is true, Start sets Illegal and DONE, and the controller rejects the operation. Otherwise, the controller makes an immediate data request for the first word, and it writes the words it receives via the data channel from the locations specified by the address counter until either the word counter overflows or a Data Late error occurs, at which time the controller terminates the record, setting DONE and initiating an interrupt.

F. Write End of File. Unless write lock is set, Start sets the controller into operation to write a file mark. With write lock true, the command is rejected, setting Illegal and DONE status.

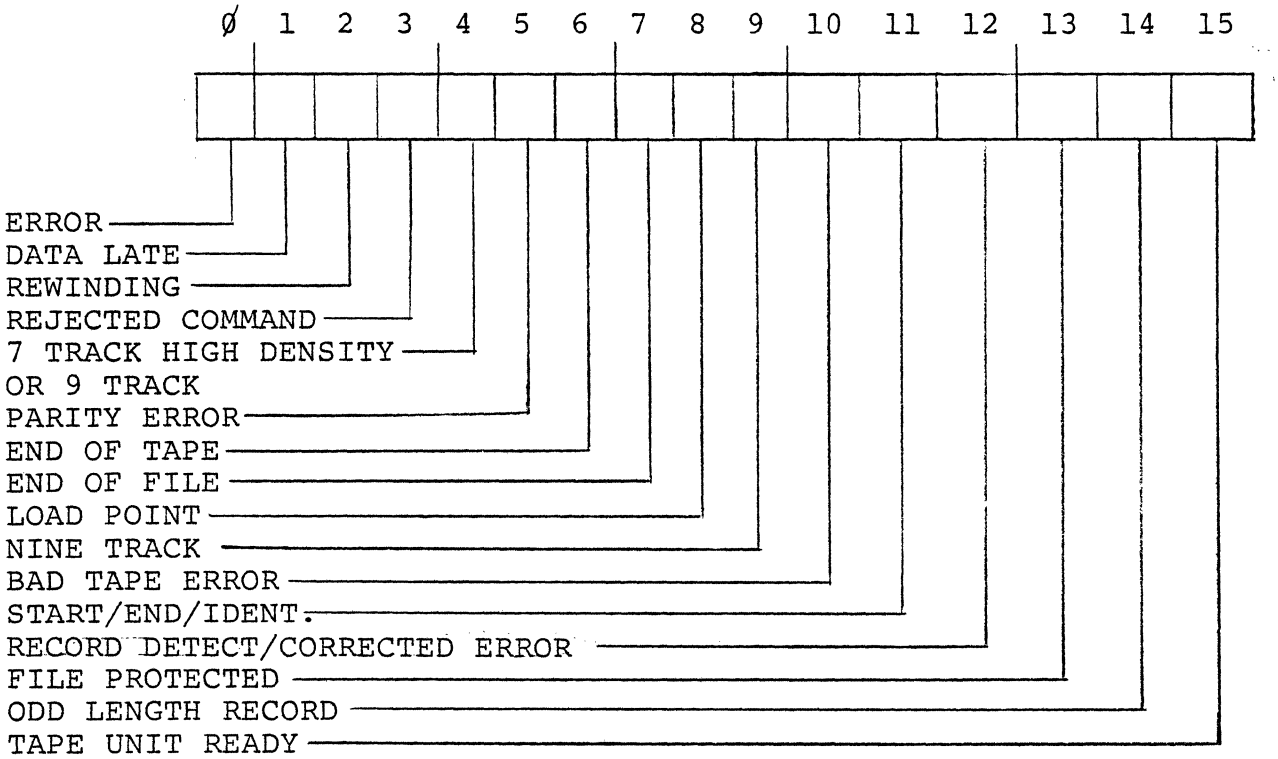
G. Erase. Unless write lock is set, Start sets the controller into operation to erase a short section of tape. This provides a method of erasing a bad record from a damaged portion of tape on which the program has found it impossible to write data without errors.

7. DOA BITS 13-15 TAPE UNIT SELECT (SLT 1, 2, 4) - These bits specify one of the eight possible tape units. All operations defined in the DOA register and all status conditions defined in the DIA register refer to the unit indicated by these bits.

LOGICAL DRIVE	DRIVE SELECT LINES		
ADDRESS	SL1 (Bit 13)	SL2 (Bit 14)	SL4 (Bit 15)
Ø	False	False	False
1	False	False	True
2	False	True	False
3	False	True	True
4	True	False	False
5	True	False	True
6	True	True	False
7	True	True	True

3.17 INPUT REGISTER "A". Using the DIA-, MTA instruction, the CPU reads the contents of the status register into the designated accumulator and performs the function specified by F. The Start clears Error, Data Late, Parity Error, End-of-File, and Bad Tape Error. The Clear function resets those status bits plus resetting the Illegal bit. The remaining flags are supplied by the addressed tape drive (which is automatically reset to logical Unit Ø after the Clear function is issued).

INPUT REGISTER "A" BIT ASSIGNMENTS
(STATUS REGISTER)



1. DIA BIT Ø ERROR FLAG (ERR) - This error examination bit is set when bit 1,3,5,6,7,8,10 or 14 of the status register is true. This bit is cleared as a result of a Start, Clear, or I/O Reset instruction.

2. DIA BIT 1 DATA LATE - The data late bit is set when the controller overflows (or "underflows") its internal buffer during an operation. This error indicates that the data channel failed to respond to a request quickly enough to keep up with the tape transfer rate. This condition causes an immediate termination of the read or write operation in progress. This bit will also be set during a read operation when the internal

buffer of the controller is not emptied before the tape begins to stop. The ERR bit in the status register will be set when the data late bit is true.

3. DIA BIT 2 REWINDING (RWDG) - The rewind status bit is set by the selected drive when it receives a rewind command from the controller or operator panel and is cleared by the selected drive when the tape arrives at load point, completing the rewind operation.

4. DIA BIT 3 REJECTED COMMAND (REJ) - When an illegal command is received the controller does not go BUSY and the command is disregarded. DONE status will be set and an interrupt requested (if enabled). The program must issue a CLEAR function before preceeding (Start does not reset rejected command status). The REJ bit sets the ERR bit in the Status Register. The REJ status bit is set for any of the following conditions:

   A. Write, write-end-of-file, or erase command is issued for a drive which is file protected (DIA Bit 13).

   B. A space reverse command is issued for a drive whose tape is at load point (DIA Bit 8).

   C. A command is received when the controller is BUSY, or when the tape drive is not ready (DIA Bit 15) or is off line.

5. DIA BIT 4 7 TRACK HIGH DENSITY OR 9 TRACK - When set, this bit indicates that the selected tape drive is

either a 9 track unit or a 7 track unit operating in the high density mode. This bit is reset for the 7 track low density mode only.

DENSITY STATUS

	Bit 4 -- Density	Bit 9 -- 9-Track
7-Track Low Density	0	0
7-Track High Density	1	0
9-Track P.E.	1	1
9-Track NRZI	1	1

6. DIA BIT 5 PARITY ERROR (PAR ERR) - The parity error bit is set when the controller detects a longitudinal (LRC) or lateral parity error, PE multiple dead track error,or format error during a read, write, or write EOF operation. A parity error is also indicated for a corrected error condition during a write operation. The parity error bit does not affect the transfer of data. During a write operation, the entire record will be transferred onto tape or in a read operation, the entire record will be transferred to memory. The ERR bit will be set when the parity error status is true.
7. DIA BIT 6 END OF TAPE (EOT) - The end of tape bit is set when the marker at the end of tape is encountered while the tape is moving in the forward direction. This bit will be reset when the marker is passed while performing a rewind or space reverse operation. The ERR bit will be set when the EOT bit is true.

8. DIA BIT 7 END OF FILE (EOF) - The EOF bit is set when a file mark is written or is detected during a read, space forward, or space reverse operation. If an error exists in a file mark character, it is recognized, rather, as a very short data record. Since the EOF condition requires attention by the CPU, the EOF bit sets the ERR bit in the status register.
9. DIA BIT 8 LOAD POINT (LPT) - The load point bit is set when the tape drive detects the load point marker at the beginning of the magnetic tape. Since the load point condition requires attention by the CPU, the load point bit will set the ERR status.
10. DIA BIT 9 NINE TRACK (9 TRK) - This status line will be set to indicate to the operating system that the tape system will accept full 8 bit characters on a 9 track drive. When a 7 track drive is selected, this bit is reset to indicate that the tape system will handle 6-bit tape characters.
11. DIA BIT 10 BAD TAPE ERROR (BTE) - When a bad tape error is detected, the ERR bit in the status register is set. The bad tape error bit sets when:
    A. More than two end-of-record characters are detected (or "trash-in-the-gap")
    B. Two or more characters are missing from the record (false end of record)
    C. Reverse spacing over an unrecognized file mark.

12. DIA BIT 11 START/END (SEND)/IDENT. - This status bit will be true at the start of a tape operation prior to data transfer or at the end of an operation after data transfer and before DONE status is indicated. This bit is also set when the PE identification burst is read from the tape.

13. DIA BIT 12 RECORD DETECTED/CORRECTED ERROR (1ST CHAR./CPE) - This status bit will be set when the read section of the controller encounters data on the magnetic tape. It is also set when the controller has corrected for a single dead track error when reading data in the P.E. mode.

14. DIA BIT 13 FILE PROTECTED (FPT) - The file protect status bit is set to prevent the software from attempting to write information on the tape when the operator has mounted a tape with the write enable ring removed. (Also called "Write Lock")

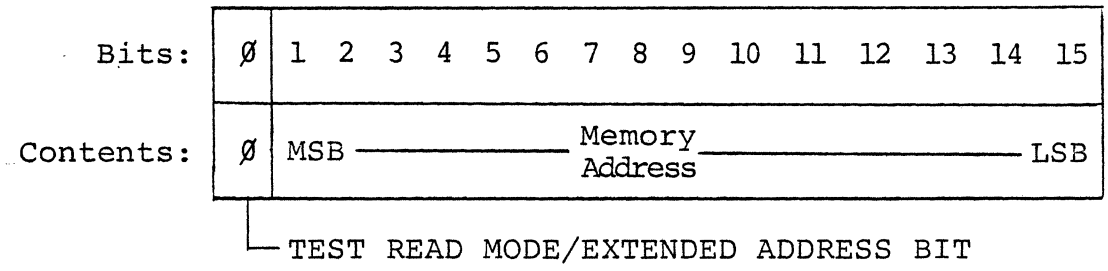
15. DIA BIT 14 ODD LENGTH RECORD (ODD) - The odd length record status bit is set by the controller to indicate that the amount of data read from the tape was one byte less than the amount of data specified by the word counter. The ERR status bit will be set when ODD is true.

16. DIA BIT 15 TAPE UNIT READY (RDY) - The tape unit ready bit is set when the selected tape unit is stopped and is cleared when the controller begins to execute a function command.

3.18 OUTPUT REGISTER "B". Using the DOB -, MTA instruction, the CPU loads the starting address of the data buffer area in memory from the accumulator into the address counter and performs the functions specified by F. The Memory Address Register normally contains 15 memory address counter bits. Bit Ø is a "Test Mode" bit and should remain a Ø. The register is used to provide the memory address for data transfers in Read and Write operations. Prior to issuing a command, the Memory Address Register is set to the memory address of the first memory location used for data transfers in a Write or Read operation. The Memory Address Register is incremented by one immediately after each memory access. Thus, at any instant of time, the Memory Address Register points to the next higher address than the one which had most recently been accessed. After a Data Late error condition, the Memory Address Register contains the address of the location in which the failure occurred.

3.19 If the Test Mode bit is set in conjunction with a Read operation, then the controller will execute a Test Read operation. Unless the Word Counter overflows, the controller will transfer the CRC (LRC in 7 track) character into the memory location which follows the data. The diagnostic program will examine these check characters to ensure that they are properly generated. The extended memory capability is enabled by a jumper, allowing 16-bit 64K addressing capability. The Test Mode is disabled in this configuration.

REGISTER "B" BIT ASSIGNMENTS
(ADDRESS REGISTER)



3.20 INPUT REGISTER "B". Using the DIB-, MTA instruction, the CPU reads the current memory address from the Memory Address Register (as previously described) into the selected accumulator and performs the function specified by F. (Bit Ø is always a zero unless Extended Address is enabled). At the end of an operation, the memory address is one-greater than the address of the last word transferred.

3.21 OUTPUT REGISTER "C". Using the DOC-, MTA instruction, the CPU specifies the number of words or records to be processed according to the contents of the designated accumulator and performs the function specified by F. The Word/Record Count Register is a 12-bit binary counter (Bits Ø-3 are not used and should remain zero, unless Expanded Word Count is enabled). The register is used to count words during Read or Write operations, or records in a Space Forward or Space Reverse operation. When used in a Write operation, the Word Count Register is initially set by the program to the 2's complement (or negative) of the number of words to be written on tape. The Word Count Register increments

by one immediately after data channel transfer. The Word Count Register overflows to zero after the last word of the record has been read from memory. This word count zero condition starts the controller into the end-of-record sequence to terminate the operations. When the Word Count Register is used in a Read operation, it is set to the 2's complement of a number equal to or greater than the maximum expected record length, indicating the memory allocation for the read data. Data transfer is terminated when the record length is greater than the allocated memory, as determined by the Word Count Register overflowing before the end-of-record is detected.

3.22 When the Word Count Register is used in a Space Forward or Space Reverse operation, it is set to the 2's complement of the number of records to be spaced over. It is incremented by one each time a record passes the head whether the tape is moving in the forward or reverse direction.

OUTPUT REGISTER "C" BIT ASSIGNMENTS
(WORD COUNT REGISTER)

Bits:	Ø 1 2 3	4 5 6 7 8 9 10 11 12 13 14 15
Contents:	Not Used	MSB — Word Count — LSB

EXPANDED WORD COUNT CAPABILITY

3.23 INPUT REGISTER "C". Using the DIC-, MTA instruction, the CPU reads the Maintenance Register into the designated accumulator and performs the function specified by F. The Maintenance Register is a 16-bit register which is used for diagnostic purposes. After

the completion of an operation, 8 bits of the CRC character and 8 bits of the LRC character are placed into the Maintenance Register and made available to the program.

INPUT REGISTER "C" BIT ASSIGNMENTS
(MAINTENANCE REGISTER)

Bits:	Ø 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15
Contents:	CRC CHARACTER	LRC CHARACTER

3.24 OPERATION STATUS CONTROL

3.25 BUSY and DONE flags are sensed by the CPU during I/O Skip instructions. These flags indicate the operational status of the controller. Operations are initiated and controlled by the Control Function (F = Clear, Start, and Pulse) of the I/O transfer instruction.

3.26 The Clear control function clears BUSY, DONE, ERROR, DATA LATE, PARITY ERROR, END-OF-FILE, BAD TAPE, ILLEGAL, and the other miscellaneous flags in the controller, terminates operations if the controller is currently processing data, and returns drive selection to drive Ø. The Start function also clears the above flags (except illegal) and is used to start tape operations. The operation to be performed is specified by the Function bits of the Command Register; in other words, the program specified a command by placing the controller in the appropriate mode and actually begins the command by issuing a Start function. The program issues Start to set Busy, and thus prevents the controller from beginning any other commands while processing data.

3.27 INTERRUPTS

3.28 An interrupt is requested when an operation is completed on the selected drive, an action which also clears BUSY status and sets the DONE status line. If the selected function results in a rejected command, the controller sets the appropriate status bit, sets Done, and requests an interrupt. Interrupts may be disabled by executing a Mask Out instruction with bit 10 set.

3.29 DATA TRANSFER FORMATS

3.30 Table 3-2 illustrates the correspondence between tape characters, tape channels, and CPU computer word bits. In 9 track each computer word contains two tape characters and all bits are used. In the 7 track non-packed mode, only six bits are available for each tape character. CPU bits 0,1,8 and 9 remain unused. In the 7 track packed mode three tape characters are used with four, six and six bits each. This allows all CPU bits to be written on a 7 track tape. In this mode, the number of tape characters handled will always be three times the word count rather than the normal, two times the word count.

CPU BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
9 TRACK TAPE CHARACTERS	← FIRST TAPE CHARACTER →								← SECOND TAPE CHARACTER →							
9 TRACK TAPE CHAN. ASSIGNMENT	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
7 TRACK TAPE CHARACTERS	0	0	FIRST TAPE CHARACTER						0	0	SECOND TAPE CHARACTER					
7 TRACK TAPE CHAN. ASSIGNMENT			B	A	8	4	2	1			B	A	8	4	2	1
7 TRACK PACK MODE CHARACTERS	FIRST TAPE CHARACTER								SECOND TAPE CHARACTER							
7 TRACK PACKED CHAN. ASSIGNMENT	8	4	2	1	B	A	8	4	2	1	B	A	8	4	2	1

TABLE 3-2 COMPUTER WORD - TAPE CHANNEL TRANSFER FORMATS

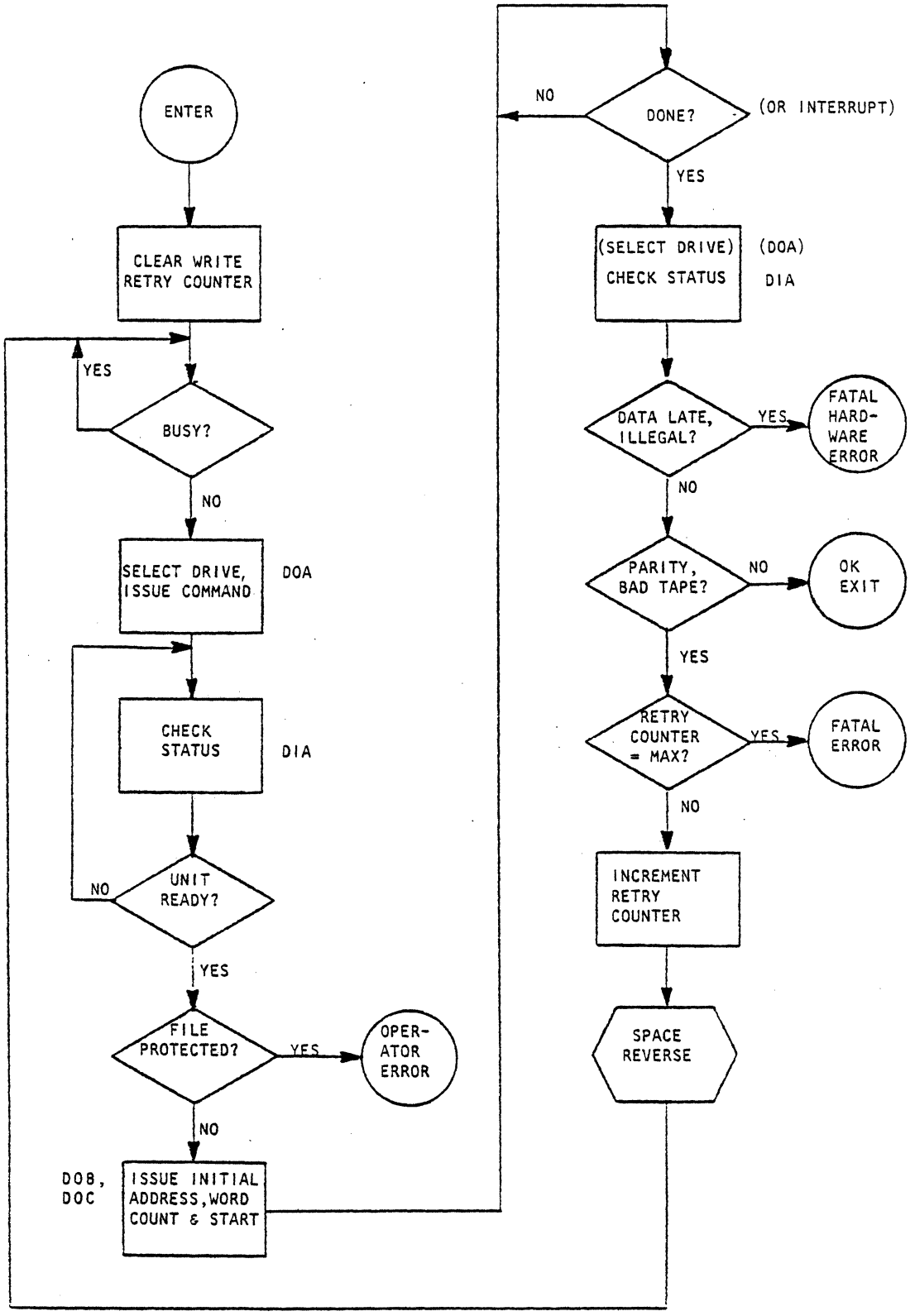


Figure 3-1. "WRITE" Flowchart

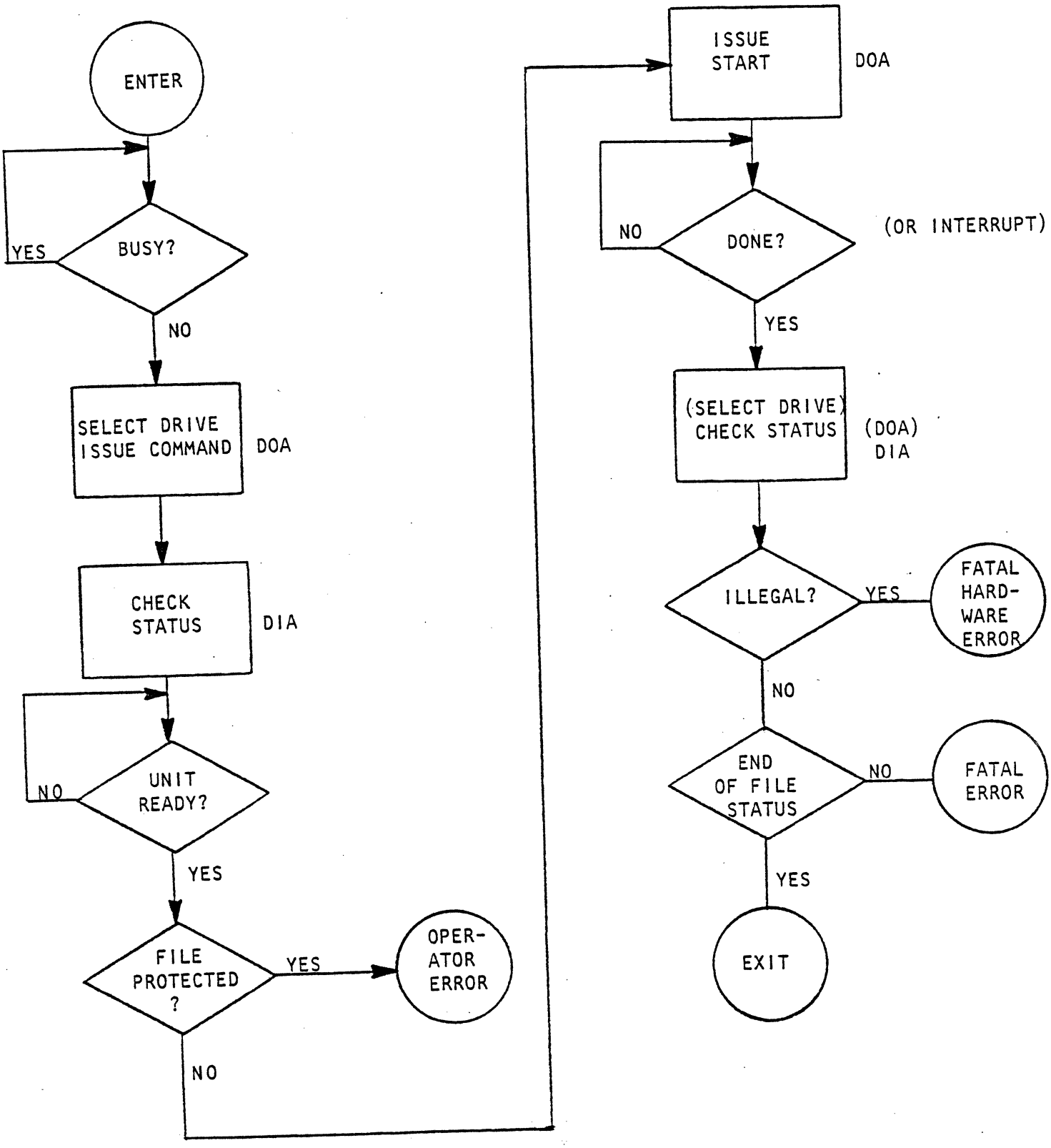


Figure 3-2. "WRITE END OF FILE" Flowchart

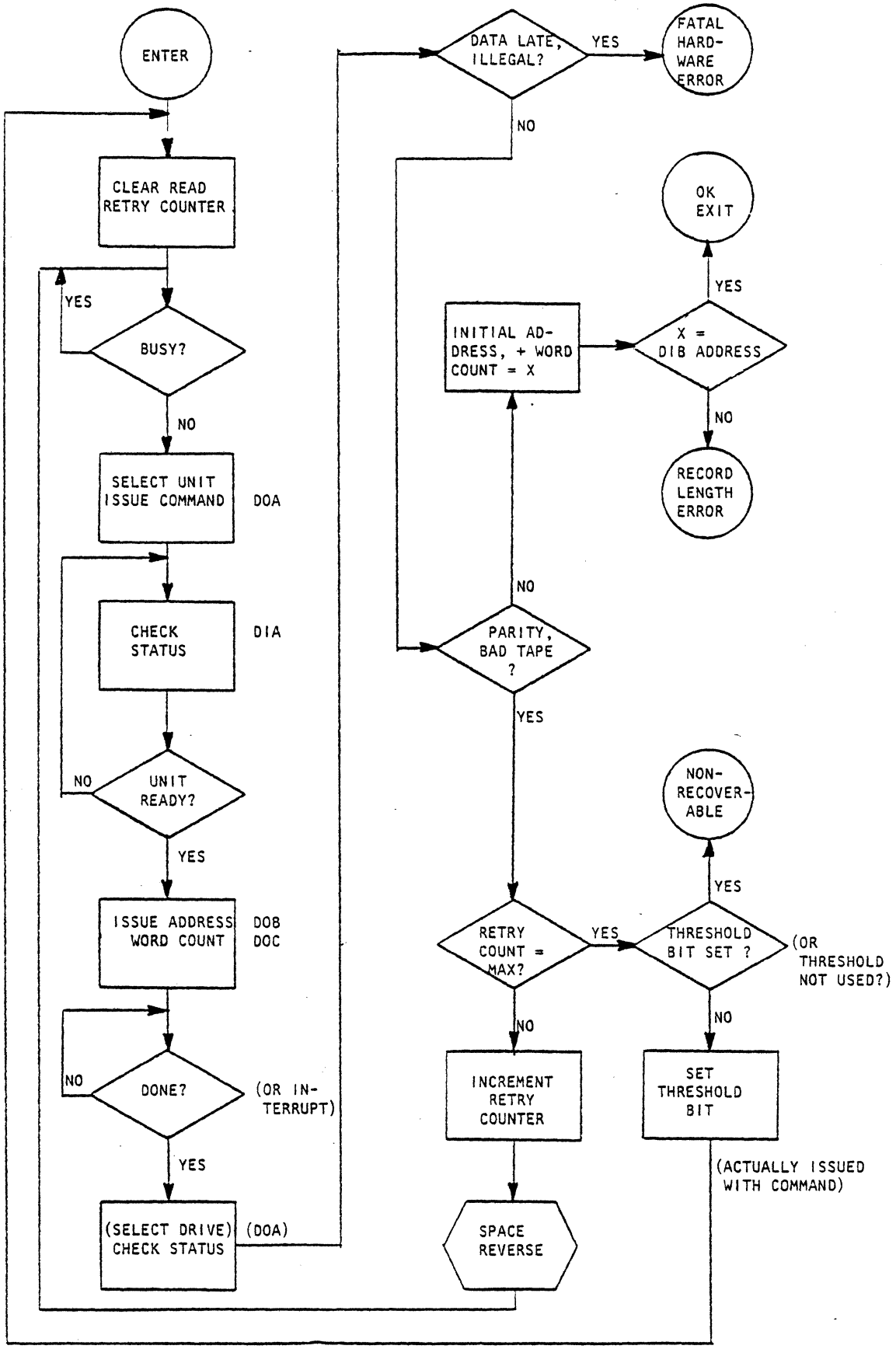


Figure 3-3. "READ" Flowchart

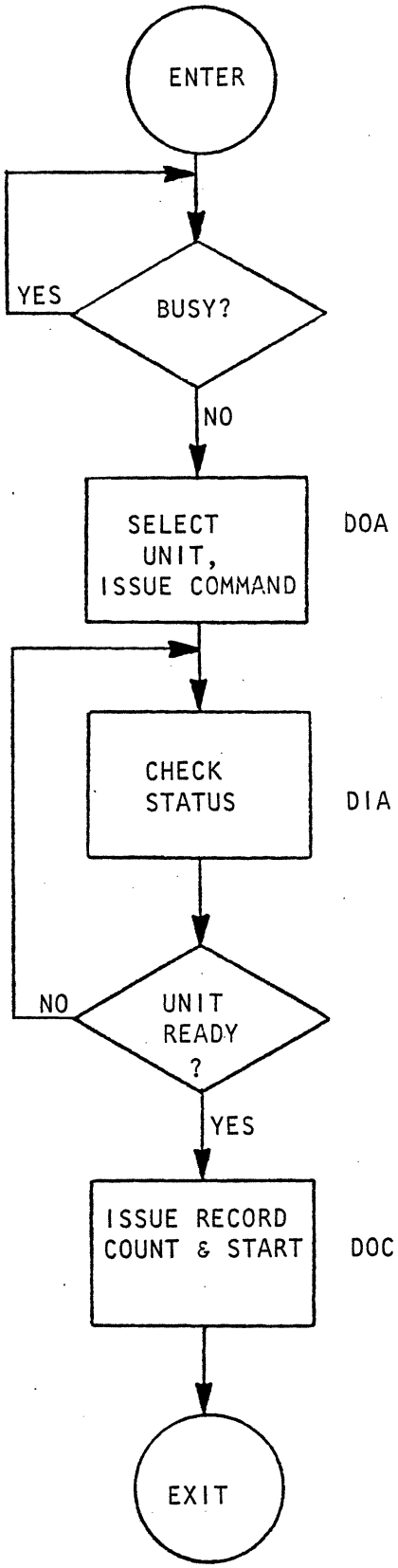


Figure 3-4. "SPACE FORWARD/REVERSE" Flow Chart

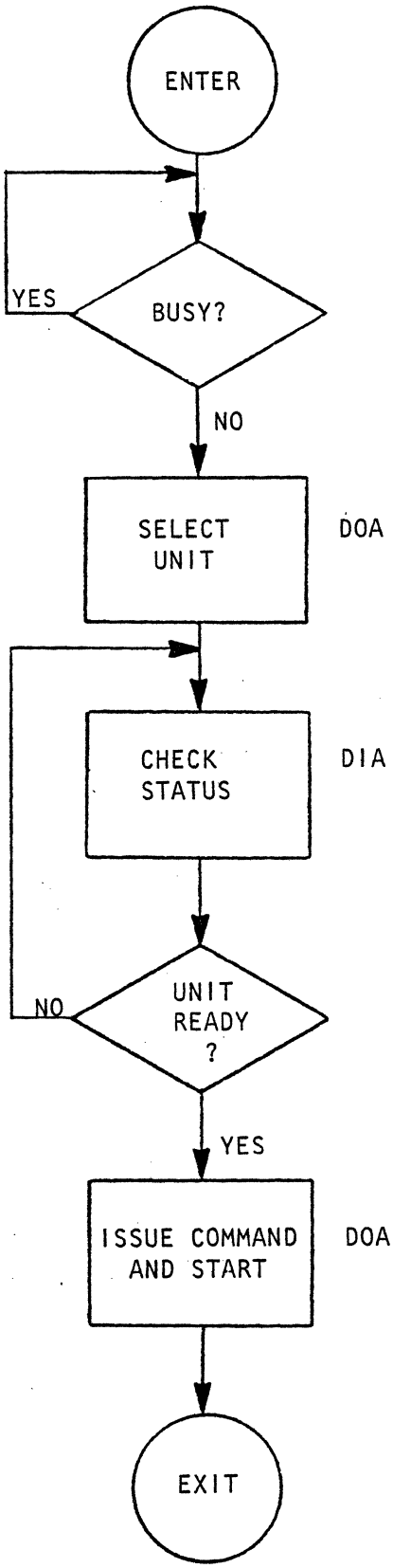


Figure 3-5. "REWIND" Flow Chart

SECTION IV

THEORY OF OPERATIONS

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF ILLUSTRATIONS

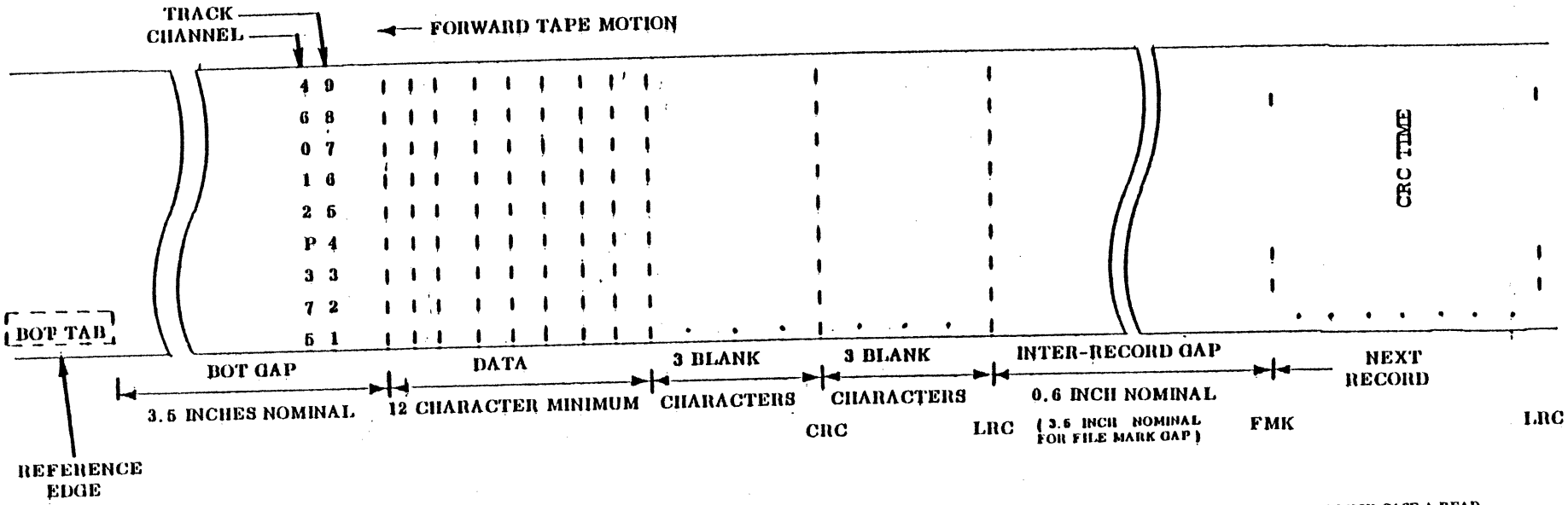
SECTION IV

THEORY OF OPERATION

4.1 TAPE FORMAT

4.2 The Western Peripherals Tape Controller interfaces to industry-standard tape drives which write nine or seven bit characters laterally across the tape. The density of the characters written on the tape is determined by the type of tape drive, the density selection made on the tape drive, and (in some cases) the density selection made in the command issued by the CPU. A data block (record) written on tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus a parity bit that is generated by the controller to conform with odd or even parity as specified by the program or the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in one Read or Write operation. The controller separates adjacent records by automatically erasing a 0.6 inch (0.75 inch in 7-track) segment of tape to form an interrecord gap (IRG) between them. The controller always stops and starts the magnetic tape in an interrecord gap.

4.3 NINE-TRACK NRZI FORMAT. As shown in Figure 4-1, each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. Following the LRC character, a 0.6 inch IRG is written, in which all nine tracks are erased. The LRC character produces an even longitudinal



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRC AND THE LRC) IS EVEN. IN THE 9-TRACK FORMAT THE LRC WILL NEVER BE AN ALL-ZEROS CHARACTER.
5. IT IS POSSIBLE FOR THIS CRC CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRC. THE CRC CONTAINS ALL ZEROS. THIS RECORD IS SEPARATED BY 3.6 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL BIG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 4-1 9-Track NRZI Tape Format

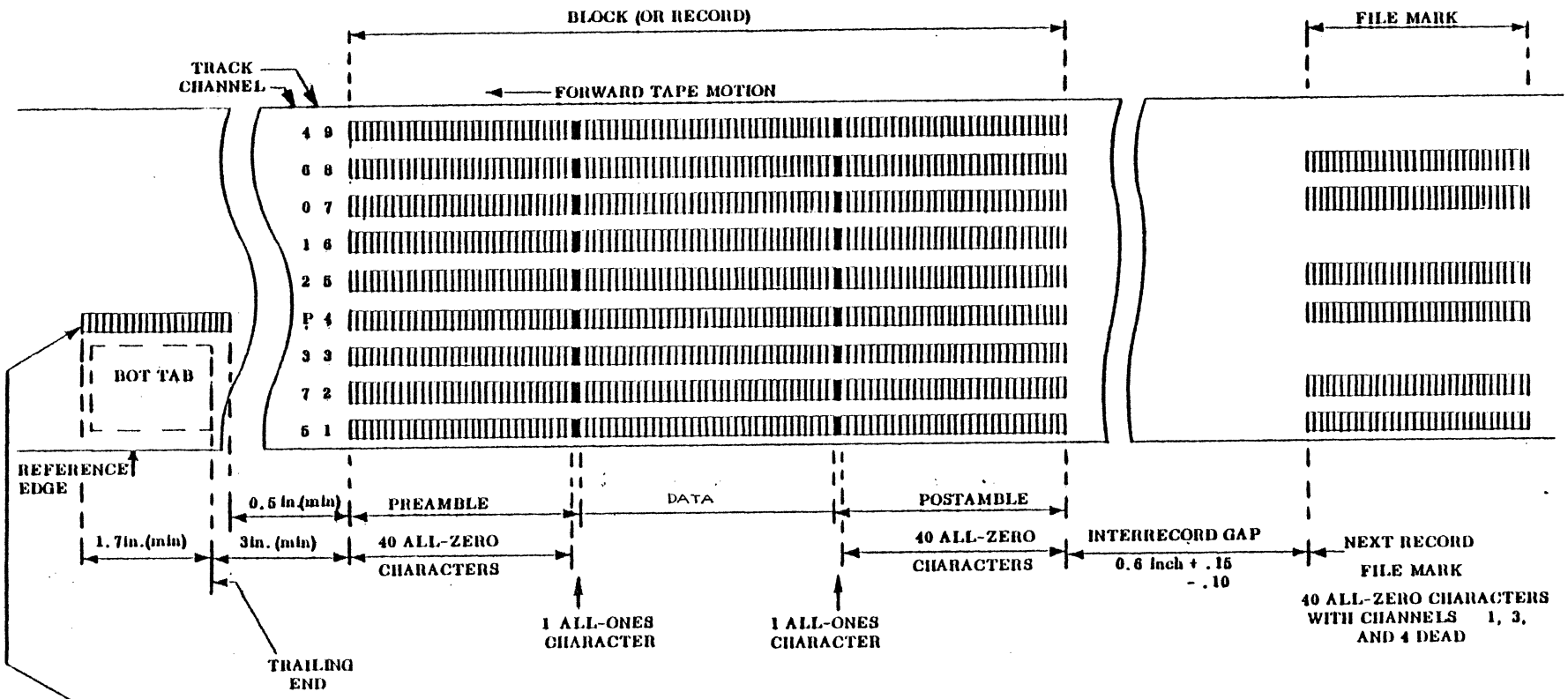
parity in each of the tracks along the length of the tape. Reading or writing, the controller checks to ascertain that the lateral parity of every data character is odd and that every track has even longitudinal parity.

4.4 The 9-track file mark consists of a single character record with a one-bit in channels 3, 6, and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

4.5 **NINE-TRACK PE FORMAT.** The standard Phase Encoded (PE) 1600 bits per inch format, shown in Figure 4-2, consists of a preamble, a variable length data block, and a postamble. The preamble consists of 40 characters containing zeros in all tracks followed by a character containing ones in all tracks. Each data character contains eight data bits and an odd vertical parity bit. The last data character is followed by the postamble (which is the reverse image of a preamble), an all-ones character followed by 40 all-zeros characters.

4.6 When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst, consisting of alternate ones and zeros in the parity (P) track, with all other tracks erased. The file mark consists of 40 characters with all zero bits similar to those in the preamble, except that channels 1, 3, and 4 are erased.

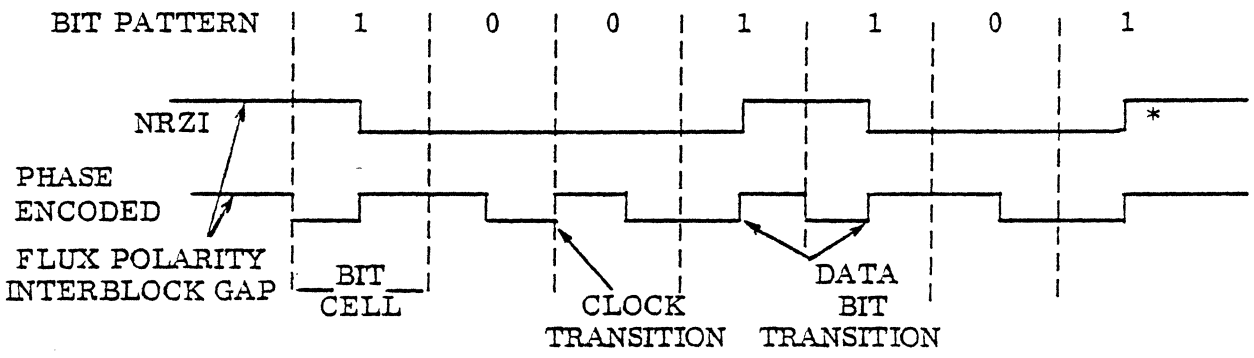
4.7 Phase encoded recording differs from NRZI recording in the recording method as well as the format. In Figure 4-3 NRZI and phase encoded waveforms of similar density are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.



NOTES

1. TAPE SHOWN OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. A FILE MARK IS A 40-CHARACTER PREMABLE BURST WITH CHANNELS 1, 3, AND 4 DEAD. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
5. DATA PACKING DENSITY IS FIXED AT 1600 BITS PER INCH.

Figure 4-2 9-Track PE Tape Format



NOTES:

NRZI--ANY CHANGE IN POLARITY IS A "1" BIT; NO CHANGE IS A "0" BIT.

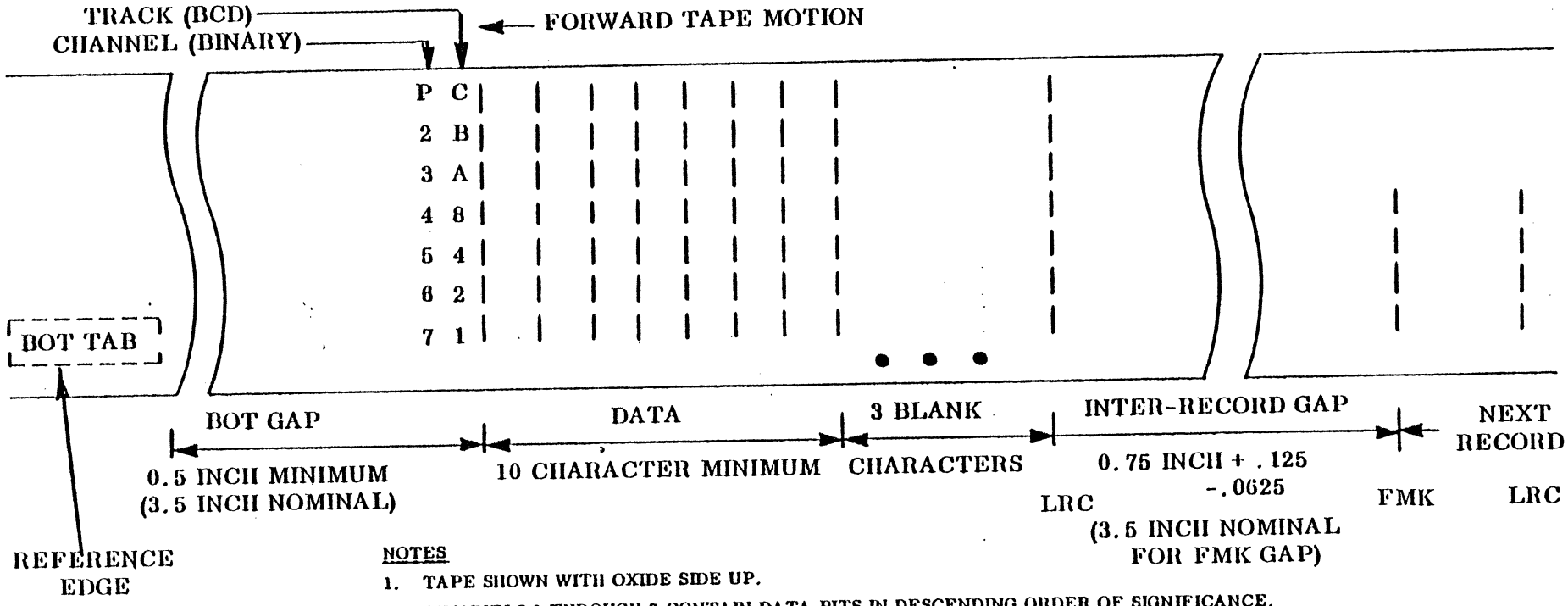
* LAST CHARACTER IS LRC

PHASE ENCODED--DATA BIT TRANSITION IN DIRECTION OF IBG IS A "1" BIT.
--DATA BIT TRANSITION OPPOSITE IN DIRECTION OF IBG IS A "0" BIT.

Figure 4-3 PE and NRZI Recording Comparison

4.8 Phase encoded recording requires at least one flux change per bit cell. A binary one is represented by a flux change to the flux polarity of the interrecord gap. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

4.9 SEVEN-TRACK NRZI FORMAT. As shown in Figure 4-4, each data character contains six bits of data and one odd or even parity bit. The data is transferred to the CPU on bits 2 through 7 and bits 10 through 15 of the bus. Bits Ø and 1 and bits 8 and 9 are always zero. Following the last data character, three blank characters (EOR) are written, followed by the LRC character. No CRC character is used in the 7-track format. In the even parity mode an octal zero character is illegal and may be converted by software to an octal twelve when writing to tape to prevent writing an unrecoverable character (no read strobes are produced for an all-zeros character). A twelve-to-zero conversion by software should then occur in the Read mode.



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRC. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.75 INCH) FROM THE FOLLOWING RECORD.
6. DATA PACKING DENSITY MAY BE 200, 556, OR 800 BITS PER INCH.

Figure 4-4 7-Track NRZI Tape Format

4.10 The 7-track file mark consists of a single character record with a one-bit in tracks 8, 4, 2, and 1. The file mark character, followed by three blank characters, is identical to the LRC which terminates the file mark record.

4.11 SEVEN-TRACK PACKED MODE. If bit 8 of the DOA Register is set when reading or writing a 7-track tape, all bits of the computer word are utilized for the transfer. The format used for the 7-track packed (core dump) mode is identical to the normal 7-track mode. However, three tape characters are transferred on the tape drive for every computer word transferred. The first four bits from the computer (bits Ø-3) are transferred to the tape drive on tracks 8, 4, 2, and 1. This tape character contains zeros in tracks B and A. Then the next six bits (bits 4-9) are transferred onto all six tape tracks. This operation continues with the third transfer (bits 10-15).

4.12 MISSING CHARACTERS. The controller checks for missing characters when reading. Two or more contiguous missing characters will be interpreted as an EOR gap. If this condition occurs in the data portion of the record, Bad Tape Error (BTE) status will be reported.

4.13 END-OF-FILE MARK. The program can group sets of data records into files. The end of a file is indicated by an End of File (EOF) mark. The NRZI File Mark is a special record containing one special data character and its LRC. The PE File Mark consists of 40 characters in a combination of active and dead tracks. Each EOF in the NRZI format is preceded by a 3.5 inch IRG. Spacing operations automatically terminate upon detection of the File Mark.

4.14 TAPE-END MARKERS. The ends of all tapes contain reflective strips that are detected by photo cells in the transport. The Load Point marker is located at least ten feet in from the beginning of the tape and constitutes the logical Beginning of Tape (BOT). The Space Reverse and Rewind commands automatically stop at this marker. At least three inches of tape intervene between the BOT marker and the first record.

4.15 The end-of-tape (EOT) reflective strip is located at least 14 feet from the end of the tape. The program should not record more than a few feet beyond the EOT marker, leaving at least ten feet of the tape for a trailer. A status bit is set and Space Reverse operations are terminated when the tape passes beyond the EOT marker.

4.16 RECORD LENGTH. The minimum record length for the controller is one character (or 18 characters per ANSI specification). Maximum length is limited only by the capacity of the Word Counter to 4K (or optionally 64K) words (2048 characters per ANSI specification). When writing, the controller divides each computer word into two data bytes. In reading, the bytes are reassembled into a computer word.

4.17 EFFECTIVE TRANSFER RATE. During the actual processing of the data part of a record, the data transfer rate is fixed. However, in a long tape the effective, or average, transfer rate depends somewhat upon record length. Record length determines the percentage of tape taken up by the gaps. At the highest density (1600 bpi) each record gap occupies the space of 960 characters. Figure 4-5 shows the storage capacity of a reel of tape at various record lengths. The effective transfer rate is therefore determined by record length as well as tape speed and density.

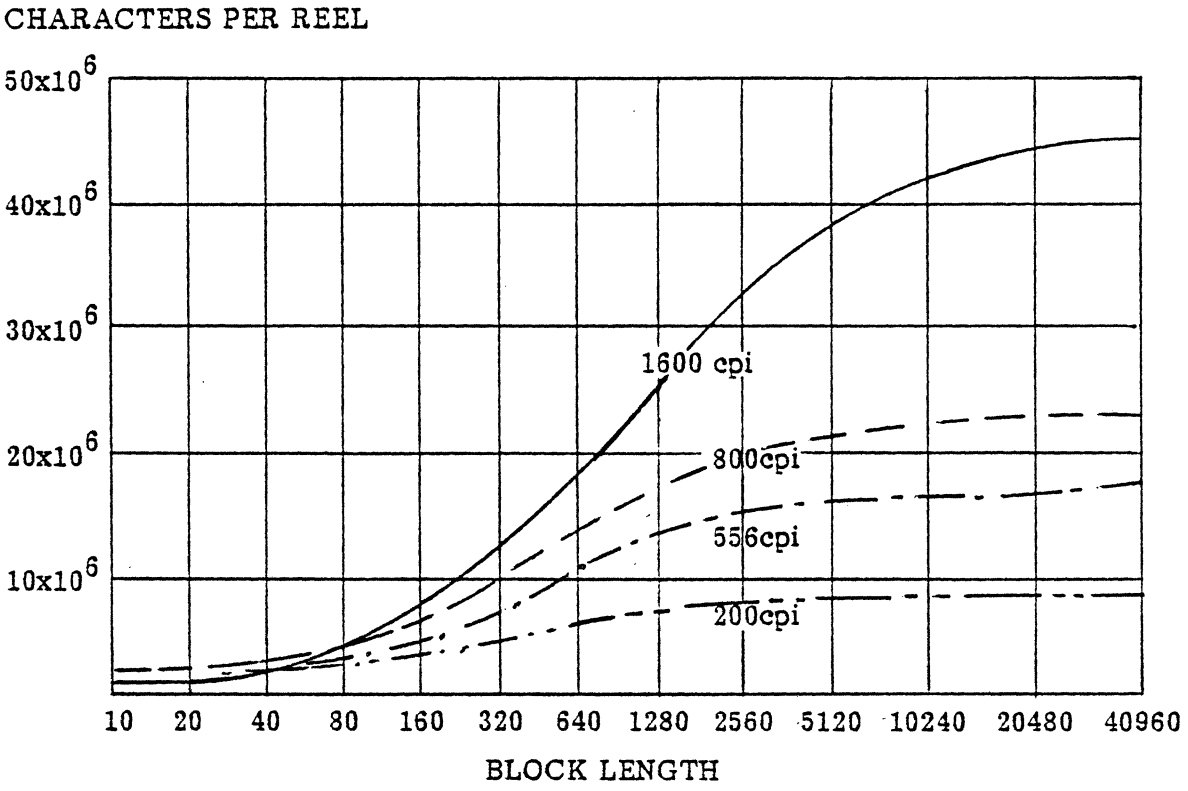


Figure 4-5 Comparison of Packing Density, Phase Encoded and NRZI Formats

4.18 TAPE DRIVE INTERFACE

4.19 INTERFACE SIGNALS. Figure 4-6 shows the signals on the interface between the controller and the tape drives. Table 4-1 lists and describes these signals. The selected tape drive returns status signals to the controller that indicate the type of tape drive, as shown in Table 4-2.

4.20 INTERCONNECTIONS. Three connectors, designated CONTROL, WRITE, and READ, are provided on the controller printed circuit board for making cable connections to the tape drives. Ribbon cable assemblies are provided for each of these three connectors. The other end of each ribbon cable assembly is connected to a connector adapter assembly (paddleboard). For the WRITE and CONTROL lines, terminators are removed from the tape drives and a termin-

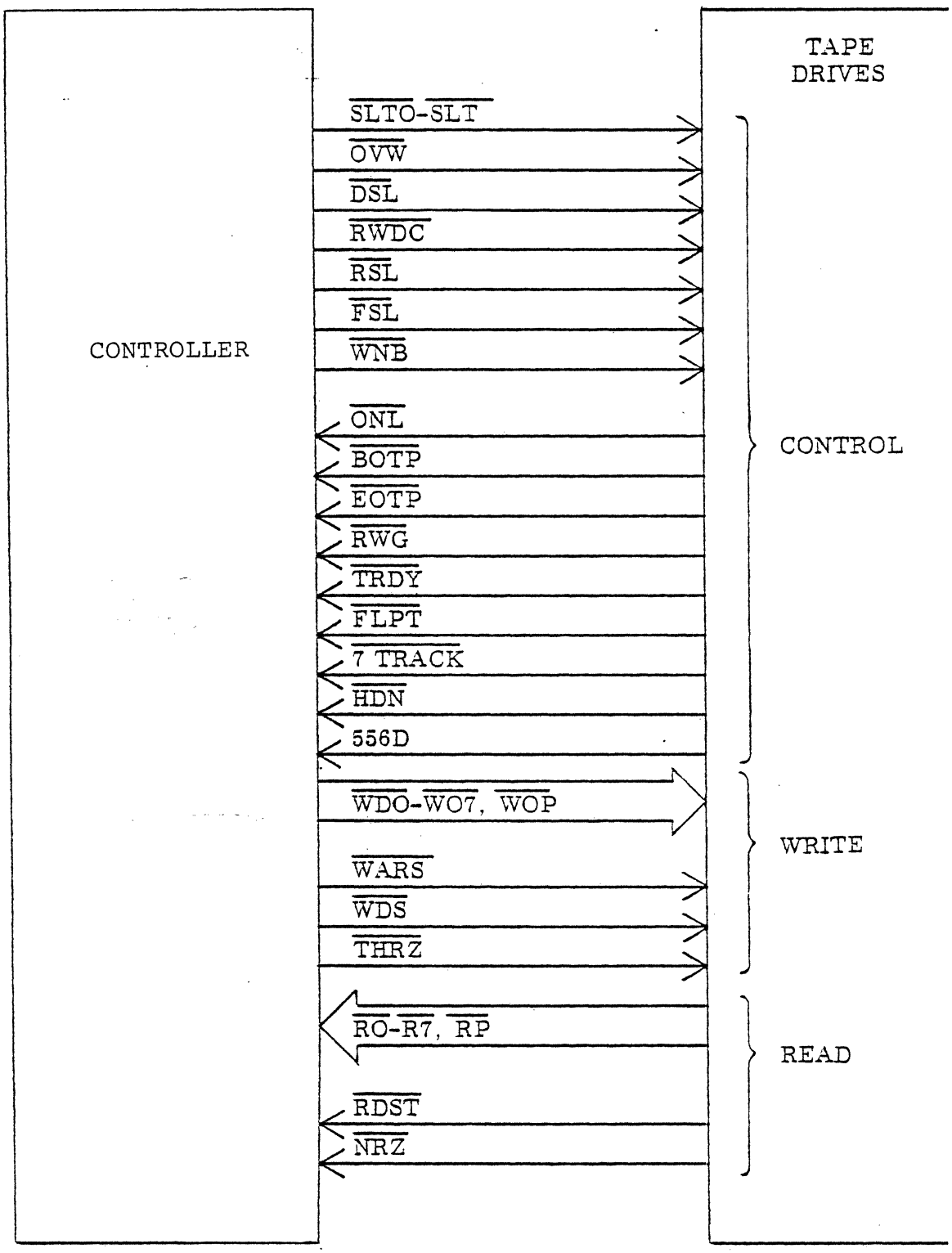


Figure 4-6 Tape Drive Interface

Table 4-1. Tape Drive Interface Signals

MNEMONIC	SOURCE	TERM	COMMENT
CONTROL CABLE:			
SLTØ-7	Controller	Select Drive Ø-7	Specified tape drive is selected.
WNB	Controller	Write Enable	Enables write operations in selected tape drive.
FSL	Controller	Synchronous Forward Command	The selected tape drive initiates tape motion in the forward direction.
RSL	Controller	Synchronous Reverse Command	The selected tape drive initiates tape motion in the reerse direction.
RWDC	Controller	Rewind Command	The selected tape drive executes a high-speed red operation.
OVW	Controller	Overwrite	The edit mode is enabled in the selected tape drive.
DSL	Controller	Density Select	When this line is active, high density is selected in the selected tape drive. When the line is inactive, low density is selected.
ONL	Drive	On Line	The selected tape drive is on-line.
BOTP	Drive	Beginning of Tape	The selected tape drive is at load point.
EOTP	Drive	End of Tape	Tape in the selected tape drive is at the end of tape marker.
RWG	Drive	Rewinding	The selected tape drive is rewinding.
TRDY	Drive	Ready	The selected tape drive is on-line and ready for operation.
FLPT	Drive	File Protect	The selected tape drive is write-protected so that a write operation cannot be executed.

Table 4-1. Tape Drive Interface Signals (cont.)

MNEMONIC	SOURCE	TERM	COMMENT
7 TRACK	Drive	7-Track	The selected tape drive is a 7-track unit.
HDN and	Drive	Density/Tape	Density for 7-track units;
556D		Speed Select	tape speed for 9-track units.
WRITE CABLE:			
WDØ to WD7 and WDP	Controller	Write Data Lines	Tape write data bus.
WARS	Controller	Write Amplifier Reset	Resets tape write amplifiers. Generates LRC character.
WDS	Controller	Write Data Strobe	Strobes tape write data into tape drive.
THR2	Controller	Threshold No. 2	When this line is active, read threshold No. 2 is selected. When the line is inactive, threshold No. 1 is selected.
READ CABLE:			
RØ to R7 and RP	Drive	Read Data Lines	Tape read data bus.
RDST	Drive	Read Strobe	Strobes read data into the controller.
NRZ	Drive	NRZ	When this line is active from a 9-track drive, it indicates a 9-track NRZ unit; when the line is inactive from a 9-track drive, it indicates a 9-track PE unit.

NOTE: All tape drive interface lines are active low.

ator chip is installed on the paddleboards in the last tape drive in the daisy chain.

4.21 DRIVE SELECT LOGIC. Each tape drive is selected by the controller when its respective select line is activated. Eight select lines are used to control the eight possible tape drives. The active select line is determined by the drive select bits of the Command Register. While the first Control Paddleboard in the daisy chain receives all of the select lines, the propagation of tahe select lines to the next drive is controlled by the Drive Select Jumper plug.

4.22 Three kinds of jumper plugs are used: One is for standard drives, one is for drives with drive selection thumbwheel switches, and one is installed in the fourth drive in installations using thumbwheel switches. A standard daisy-chained system is shown in Figure 4-7 where SLT Ø connects to drive Ø, SLT 1 connects to drive 1, etc. Each drive select jumper increments the drive select lines one position so that the next drive in position becomes the next numbered drive. Figure 4-8 illustrates a system using drives with select switches. Four of the select lines are made available to each drive, and the operator selects (with the thumbwheel switch) which select line will activate a particular drive. The operator must ensure that each drive is set to a different number. Caution: A separate installation step is required to connect all four select lines to each drive. Note: Some drive manufacturers mark the thumbwheel switch 1 through 4 for drive selections Ø through 3, respectively, with position Ø sometimes used as an off-line position.

Type of Tape Drive	Status Signal			
	7 TRACK	HDN	556D	NRZ
9-track, Tape Speed A	High	. . .	High	. . .
9-track, Tape Speed B	High	. . .	Low	. . .
9-track, PE (1600 bpi)	High	. . .	. . .	High
9-track, NRZ (800 bpi)	High	. . .	. . .	Low
7-track, 800 bpi	Low	Low	Low	. . .
7-track, 556 bpi	Low	High	Low	. . .
7-track 556 bpi	Low	Low	High	. . .
7-track, 200 bpi	Low	High	High	. . .

Table 4-2 Status Signal Indicating Tape Drive Type

TAPE DRIVE TIMING PARAMETERS

TAPE SPEED (IPS)	RAMP TIME (MS)	DATA RATE (cb/s) AND PERIOD (us) AT:								R-A-W DELAY (MS)
		1600 bpi *		800 bpi		556 bpi		200 bpi		
		RATE	PERIOD	RATE	PERIOD	RATE	PERIOD	RATE	PERIOD	
6.25	60	10K	100	5K	200	3.475K	287.2	1.25K	800	24
12.5	30	20K	50	10	100	6.95K	143.6	2.5K	400	12
18.75	20	30K	33.3	15	66.6	10.4K	96.2	3.75K	266.7	8
25	15	40K	25	20	50	13.9K	72	5K	200	6
37.5	10	60K	16.65	30	33.3	20.85K	48.7	7.5K	133.3	4
45	8.33	72K	13.9	36	27.8	25K	40	9K	111.1	3.33
75	5	120K	8.35	60	16.7	41.7K	24.5	15K	66.6	2
125	3	200K	5	100	10	69.5K	14.4	25K	40	1.2

* For 3200fci timing, multiply rate or divide period by two.

Table 4-3 Tape Drive Timing Parameters

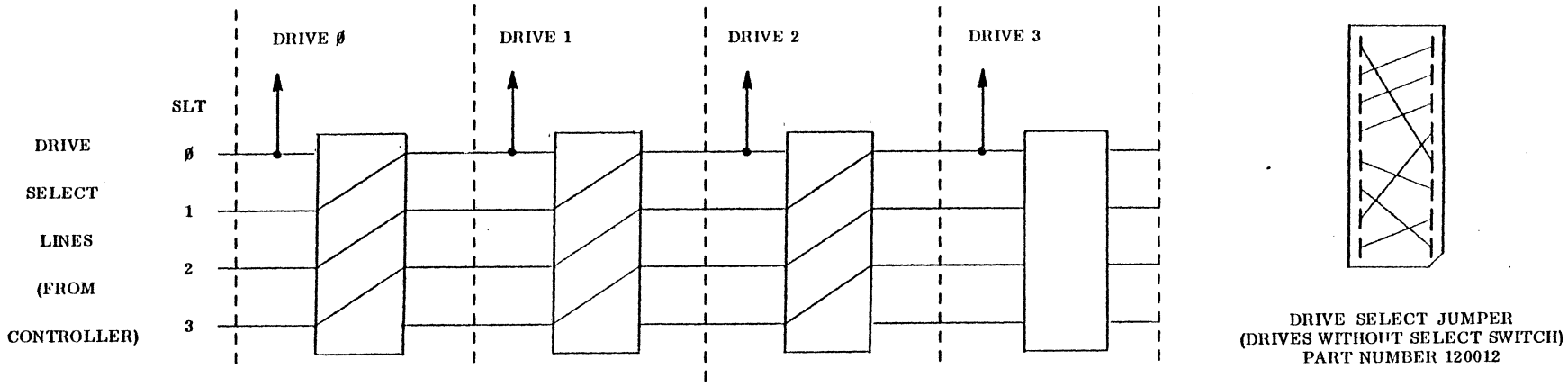


Figure 4-7 Standard Drive Select Logic

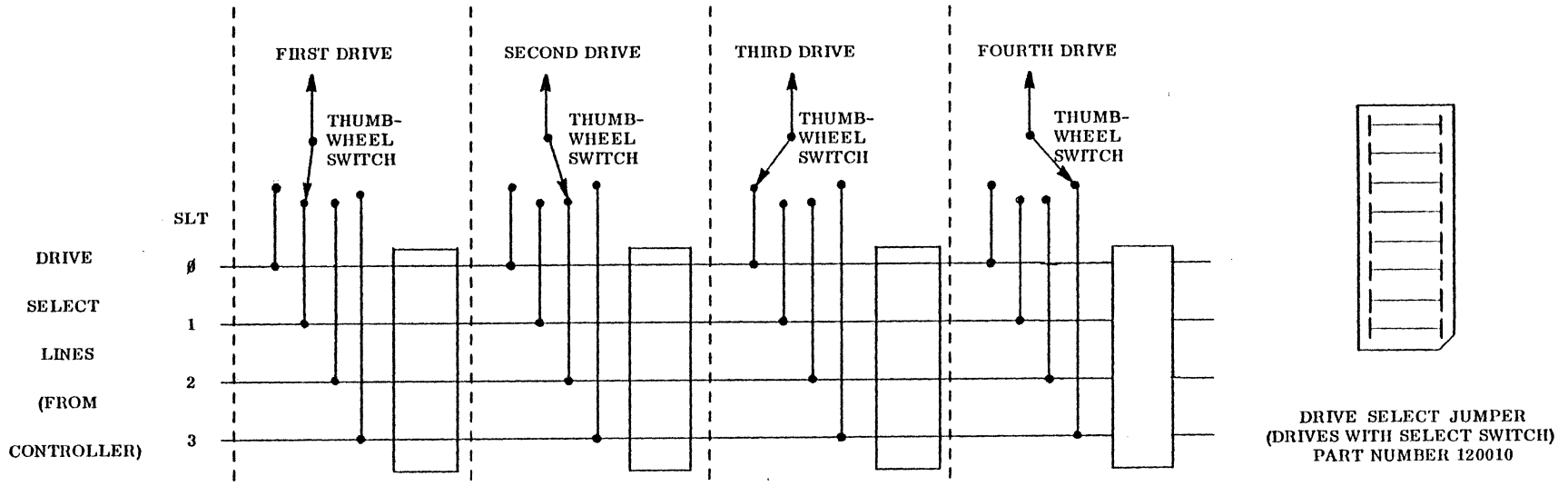


Figure 4-8 · Drive Select Logic Using Select Switches

4.23 COMPUTER INTERFACE

4.24 IN-OUT BUS ORGANIZATION. The bus consists of sixteen bidirectional data lines, six device selection lines and nineteen control lines from the processor to the devices, and six control lines from the devices to the processor. Signals on the control lines from the processor synchronize all transfers on the data lines, start and stop device operations, and control the data channel and program interrupt. Over the control lines to the processor, a device can indicate the states of its Busy and Done flags and request a program interrupt or a data channel access.

4.25 Signals on the control lines from the processor not only specify a particular function but also supply all timing information needed for the execution of that function. No bus timing functions are performed by the devices that connect to the bus; all such timing is supplied by the processor in the signals sent over the bus control lines.

4.26 BUS TRANSFERS. There are two types of in-out data transfers: the movement of words or characters by the program and the automatic transfer of data via the data channel. The program can service the controller by sensing Busy and Done or by allowing the device to interrupt when it requires service. This controller is automatic, since it uses data channel cycles for the transfer of data and requires response by the program only for control purposes (such as when a transfer is complete or there is some special situation, such as an error, which the program must handle, or to issue a new command).

4.27 BUS INTERFACE SIGNALS. The binary signals on the bus have two states, low and high, which correspond respectively to nominal voltage levels of Ø and +2.7 volts. Any level between ground and .4 volts is interpreted as low and

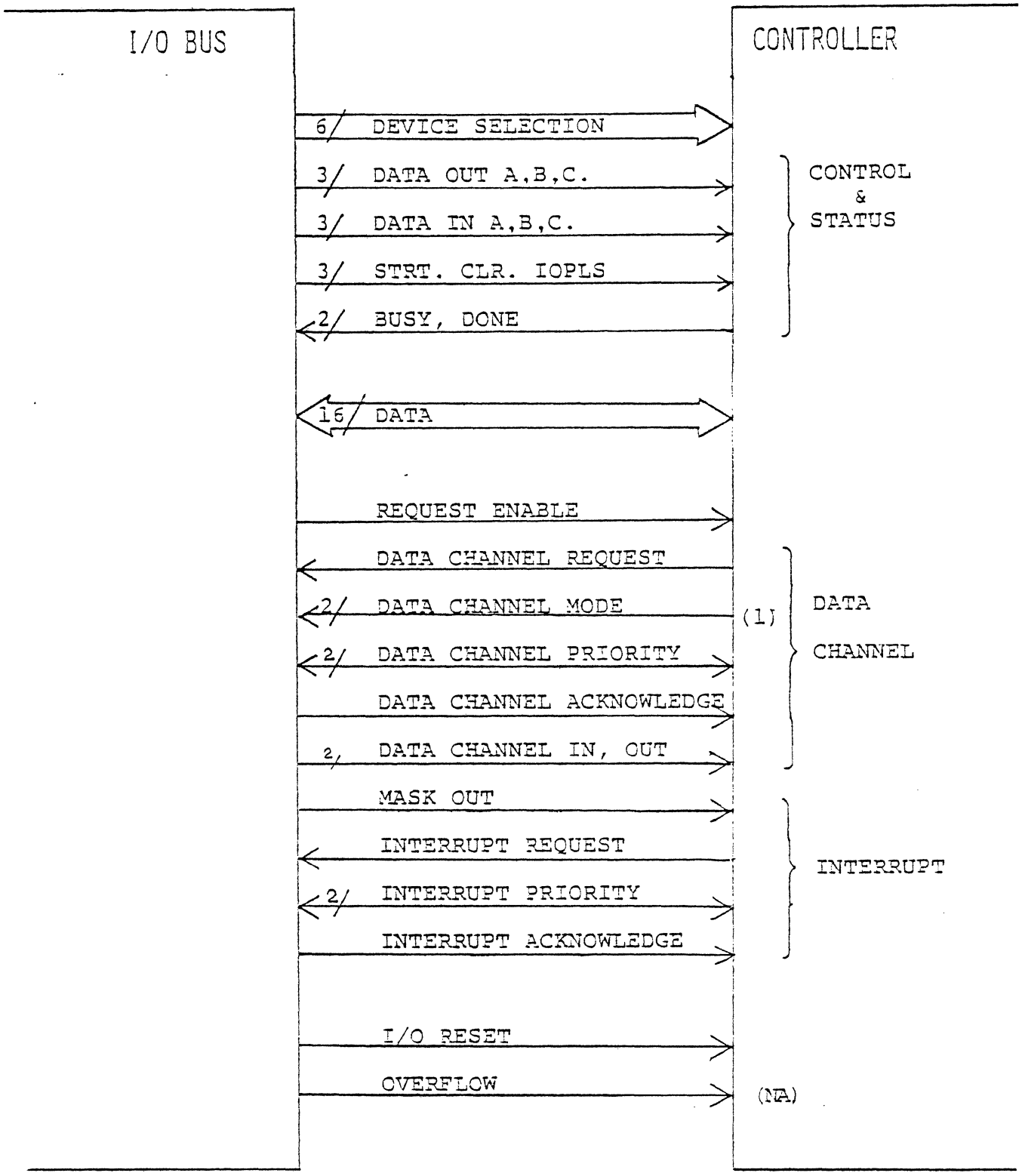


Figure 4-9 Computer Interface

any level more positive than 2.2 volts is interpreted as high. The level listed for a signal in the following list is the voltage level on the line when the signal represents a 1, true condition, or produces the indicated function. A low true signal is indicated in the schematic diagrams by a bar over its mnemonic term.

1. DSØ-5 (DEVICE SELECTION)- The Device Selection lines are low-true signals from the processor, on which the processor places the device code (bits 10-15 of the instruction word) during the execution of an in-out instruction. Only the selected device responds to control signals generated during the instruction.

2. DATAØ-15 (DATA) - The Data lines are bidirectional low-true signals. All data and addresses are transferred between the processor and the devices attached to the bus via these sixteen lines.
   For programmed output the processor places the AC specified by the instruction on the data lines and then generates DATOA, DATOB or DATOC to load the data from the lines into the corresponding register in the device selection by DSØ-5, or generates MSKO to set up the Interrupt Disable flags in all of the devices according to the mask bits on the data lines or generates DCHO to load the contents of the data lines into the data buffer in the device that is being serviced.
   For programmed input the processor generates DATIA,DATIB or DATIC to place information from the corresponding register in the device selected by DSØ-5 on the data lines, or generates INTA to place the code of the nearest device that is requesting an interrupt on data lines 10-15. The processor then loads the data from the data lines into the AC selected by the instruction. To get an address for data channel access; The processor generates DCHA to place a memory address, of the nearest device that is requesting access onto the data lines from the memory

address register of the device. For data channel input the processor generates DCHI to place the data buffer of the device being serviced onto the data lines and then loads the contents of the lines into the memory buffer.

3. DATOA (DATA OUT A) - The Data Out A line is a high-true signal generated by the processor after AC has been placed on the data lines in a DOA to load the data into the A register in the device selected by DSØ-5.

4. DATIA (DATA IN A) - The Data In A line is a high-true signal generated by the processor during a DIA to place the A register in the device selected by DSØ-5 on the data lines.

5. DATOB (Data Out B) - The Data Out B line is a high-true signal from the processor which is equivalent to DATOA but loads the B register.

6. DATIB (DATA IN B) - The Data In B line is a high-true signal from the processor which is equivalent to DATIA but places the B register on the data lines.

7. DATOC (DATA OUT C) - The Data Out C line is a high-true signal from the processor which is equivalent to DATOA but loads the C register.

8. DATIC (DATA IN C) - The Data In C line is a high-true signal from the processor which is equivalent to DATIA but places the C register on the data lines.

9. STRT (START) - The Start line is a high-true signal generated by the processor in any nonskip I/O instruction with an S control function (bits 8-9= 1) to clear Done, set Busy, and clear the INT REQ flip/flop in the device sleected by DSØ-5.

10. CLR (CLEAR) - The Clear line is a high-true signal generated by the processor in any nonskip I/O instruction with a C control function (bits 8-9=10) to clear Busy, Done and the INT REQ flip/flop in the device selected by DSØ-5.

11. IOPLS (I/O PULSE)-The I/O Pulse line is a high-true signal generated by the processor in any nonskip I/O instruction with a P control function (bits 8-9=11). This signal is not used in the tape controller but is used with positioning commands with the disc controller.

12. SELB (SELECTED BUSY) - The Selected Busy line is a low-true signal generated by the controller, when selected, if its Busy flag is set.

13. SELD (SELECTED DONE) - The Selected Done line is a low-true signal generated by the controller, when selected, if its Done flag is set. In addition, an interrupt (unless masked) is initiated by the controller.

14. RQENB (REQUEST ENABLE) - The Request Enable line is a low-true signal generated by the processor at the beginning of every memory cycle to allow all devices on the bus to request program interrupts or data channel access. RQENB sets the INT REQ flip/flop if Done is set and Interrupt Disable is clear. Otherwise it clears INT REQ. RQENB sets the DCH REQ flip/flop if the DCH SYNC flip/flop is set. Otherwise it clears DCH REQ.

15. INTR (INTERRUPT REQUEST) - The Interrupt Request line is a low-true signal generated by the controller when its INT REQ flip/flop is set. This informs the processor that the device is waiting for an interrupt to start.

16. INTP (INTERRUPT PRIORITY) - The Interrupt Priority line is a low-true signal generated by the processor for transmission serially to the devices on the bus. If the INT REQ flip/flop in a device is clear when the device receives INTP, the signal is transmitted to the next device.

17. INTA (INTERRUPT ACKNOWLEDGE) - The Interrupt Acknowledge line is a low-true signal generated by the processor during the INTA instruction. If the controller receives INTA while it is also receiving INTP and its INT REQ flip/flop is set, it places its device code on data lines 10-15.

18. MSKO (MASK OUT) - The Mask Out line is a low-true signal generated by the processor during the MSKO instruction after AC has been placed on the data lines to set up the Interrupt Disable flags in all devices according to the mask bit pattern on the data lines.

19. DCHR (DATA CHANNEL REQUEST) - The Data Channel Request line is a low-true signal generated by the controller when its DCH REQ flip/flop is set. This informs the processor that the device is waiting for data channel access.

20. DCHP (DATA CHANNEL PRIORITY) - The Data Channel Priority line is a low-true signal generated by the processor and transmitted serially to the devices on the bus. If the DCH REQ flip/flop in the controller is clear when it received DCHP, the signal is transmitted to the next device.

21. DCHA (DATA CHANNEL ACKNOWLEDGE) - The Data Channel Acknowledge line is a low-true signal generated by the processor at the beginning of a data channel cycle. If a device receives DCHA while it is also receiving DCHP and its DCH REQ flip/flop is set, it places the memory address to be used for data channel access on the data lines and sets its DCH SEL flip/flop.

22. DCHMØ, DCHM1 (DATA CHANNEL MODE) - The Data Channel Mode lines are low-true signals generated by the controller (DCHMØ only) when its DCH SEL flip/flop is set to inform the processor of the type of data channel cycle desired as follows:

DCHMØ	DCHM1	
Ø(H)	Ø(H)	Data Out
Ø(H)	1(L)	Increment memory (not used by controller)
1(L)	Ø(H)	Data in
1(L)	1(L)	Add to memory (not used by controller)

In response to the Data Channel Mode request, the processor performs the necessary functions internally, and generates DCHI and/or DCHO for the required in-out transfers.

23. DCHI (DATA CHANNEL IN) - The Data Channel In line is a high-true signal generated by the processor for data channel input (DCHMØ=1) to place the data register of the device selected by DCHA/DCHP on the data lines.

24. DCHO (DATA CHANNEL OUT)- The Data Channel Out line is a high-true signal generated by the processor for data channel output (DCHMØ=Ø) after the data has been placed on the data lines to load the register of the controller when selected by DCHA/DCHP.

25. IORST (I/O RESET) - The I/O Reset line is a high-true line generated by the processor during power-on, during the IORST instruction or when the console reset switch is pressed to clear the control flip/flops in all interfaces connected to the bus.

4.28 BUS CONNECTIONS. (Tables 2-3 and 2-4) The back panel of the chassis that holds the printed circuit board has two 100-pin connectors for each slot. The bottom slots are wired for the central processor. The back panel connectors of the upper slots are identical and are wired to the memory and in-out buses. In an expansion chassis added to the basic unit, all connector pairs are wired for the memory and I/O busses. An unregulated-15 VDC is available at pins at the power supply end on the back panel. The bus system is designed for a maximum length of 50 feet including signal path length within devices and inside the processor. Proper termination for all forty-seven bus signals is available using part number DGC 1013. This part has an I/O cable plug for plugging into the last position on the bus in place of the cable to another device.

4.29 BUS OPERATIONS. Three classes of operations take place over the in-out

bus: programmed transfers (or more generally the execution of in-out instructions), events associated with requesting and acknowledging a program interrupt, and data channel transfers. Relationships among the various bus signals involved in these operations are shown in a series of diagrams accompanying this section. In the diagrams, each signal or group of signals is represented by a horizontal line with a raised section. In the case of a control signal that is generated at a specific time to control some particular function, the raised section represents the time that the function is true. For signals that carry binary information, such as the data and device selection signals, the raised section indicates the time during which that information is held on the bus. The level of a line in the diagram has no connection with the voltage level of the signal: the time that a control signal is true is represented by the raised part of the line no matter whether the signal is true when high or low.

4.30 PROGRAMMED TRANSFERS (Figure 4-10). Throughout the duration of any in-out instruction, the processor holds the device code on the device selection lines (DSØ-5) for decoding by the device. The processor generates DATIA, DATIB, or DATIC to place the corresponding register on the data lines in the device selected by DSØ-5. At the end of the DATI level the processor strobes the data into the AC selected by the instruction. Following the transfer the processor generates the pulse for the Control Function if called for by the instruction. The acknowledgment of an interrupt is the same as data input except the INTA (which replaces the DATI) places on the data lines the device code of the nearest device that is requesting an interrupt.

4.31 While the processor placed the AC selected by the instruction on the data lines, it generates DATOA, DATOB or DATOC to load the data from the lines into the corresponding register in the device selected by DSØ-5. When the data

is dropped, the processor generates the pulse for the control function if called for by the instruction. When using a mask to set device priorities for the program interrupt, the processor executes the same sequence as for data output but generates MSKO (in place of a DATO pulse) to set up the Interrupt Disable flags in all devices according to the information on the data lines. To allow the processor to sense the state of a device, a device places its Busy and Done flags on the SELB and SELD lines whenever it recognizes its code on the device selection lines.

4.32 PROGRAM INTERRUPT (Figure 4-11). When the controller completes an operation it sets its Done flag. The processor generates RQENB, which places the interrupt request signal INTR on the bus. The leading edge of RQENB is used to set INT REQ to ensure sufficient time for the serial INTP function to settle down before the processor attempts to discover which device has priority. The controller receives INTP IN only if there is no higher priority device requesting an interrupt; the INTP signal terminates at the first device whose INT REQ flip/flop is set. If the program is to use the same device again, it must clear Done so the device will not immediately request an interrupt when the interrupt system is turned back on and interrupt Disable is cleared.

4.33 DATA CHANNEL TRANSFERS (Figure 4-12). Not all events associated with a data channel transfer actually occur in the processor cycle devoted to it: there is overlap so preliminary events occur in the preceding cycle, which may be the final cycle of an instruction or another data channel cycle. In all cases a memory address is sent into the processor in the preceding cycle which is extended while the data is transferred. Transfer operations within the processor cycle officially designated as the data channel cycle for the given access occur only if a word is sent out. The events associated with a data channel request are similar to those of an interrupt request. The DCHP signal

terminates at the first device whose DCH REQ flip/flop is set. When a device requires access it sets DCH SYNC. Once this flip/flop is set the next RQENB from the processor places the data channel request signal (DCHR) on the bus by setting DCH REQ. Synchronization must be on the leading edge of RQENB to ensure sufficient time for the serial DCHP function to settle down. If a device is waiting for access, then after RQENB terminates in the final cycle of an instruction, the processor turns on DCHA, whose leading edge sets the DCH SEL flip/flop in the nearest device that is requesting service. The device places a memory address on the bus for the duration of DCHA. When DCHA terminates, the processor strobes the address into its memory address register. The address is supplied by an address counter in the controller so that access is made to consecutive memory locations. The true state of DCH SEL places the appropriate state of DCHMØ on the bus to select the transfer mode. This signal remains on the bus as long as the DCH SEL remains set; but there is no conflict with other cycles, for when DCHA sets DCH SEL in one device, it clears those in all others. The leading edge of DCHA also clears DCH SYNC. Then while the leading edge of the next RQENB is setting request flip/flops in other devices, it will clear DCH REQ in the controller unless DCH SYNC has been set.

4.34 The remaining functions associated with data channel access depend on the type of transfer being made. For Data In, as DCHA ends, the processor turns on DCHI and the final instruction cycle is extended while DCHI holds the contents of the data register on the bus. At the end of DCHI the processor strobes the data into the memory buffer and begins the next processor cycle by generating RQENB, which turns off DCHR. For Data Out, the processor retrieves a word from the addressed memory location and brings it into the memory buffer. It completes the cycle by placing the contents of the memory buffer on the data lines and generating DCHO to load the word into the controller data register.

4.35 If several devices are requesting access simultaneously or a single device is requesting access at the maximum rate, the processor will execute a number of data channel cycles consecutively before going on to an interrupt or the next instruction When this occurs, adjacent cycles overlap. If the DCH SYNC flip/flop in the device that is being serviced is clear at the leading edge of RQENB in the data channel cycle, then RQENB clears DCH REQ in that device. But if DCH SYNC is already set again, DCH REQ simply stays set, making a second request. In either case RQENB sets the request flip/flops in any other devices that require service. If there is a second request from any source, the processor generates a second DCHA after completing whatever operations are necessary for the first access. DCHA thus occurs at the end of RQENB for Data In, but following the output of data for Data Out. This second DCHA sets the DCH SEL flip/flop in the device that now has priority (clearing all others) and initiates whatever other operations are necessary to prepare for the second transfer.

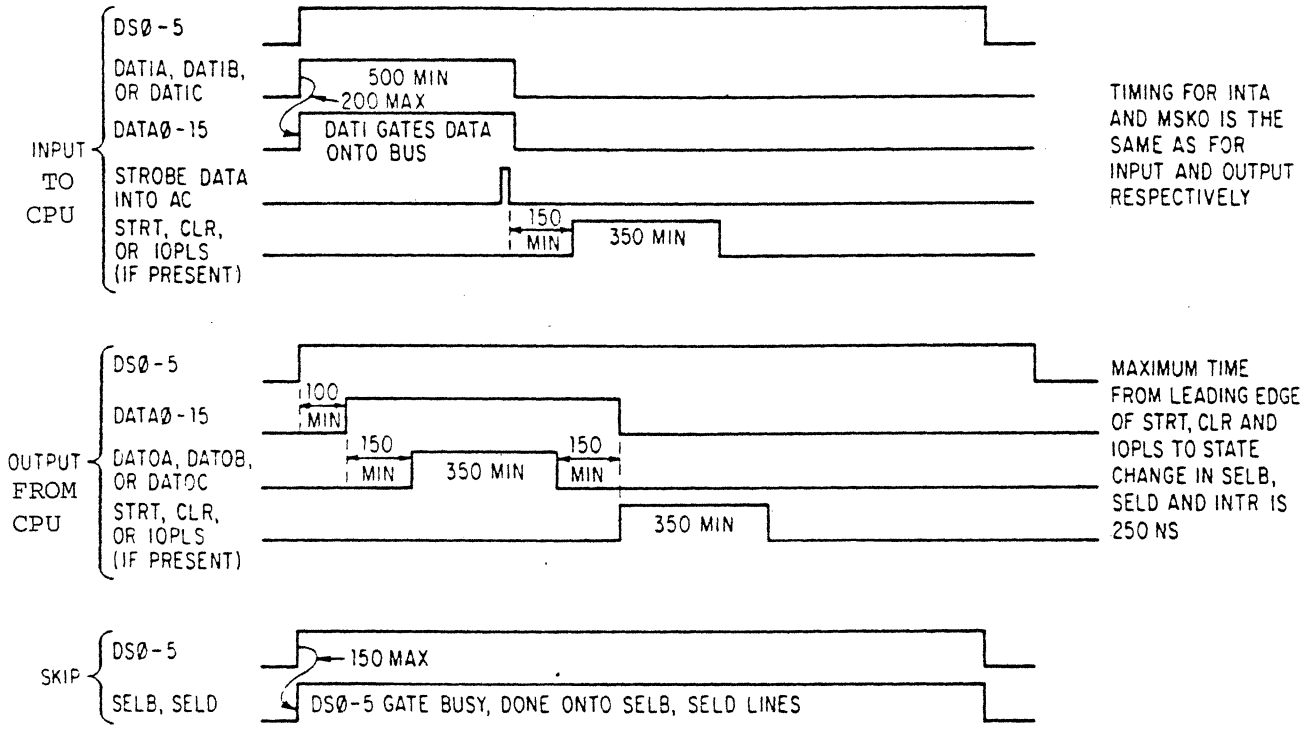


Figure 4-10 PROGRAMMED TRANSFERS (IN-OUT INSTRUCTIONS)

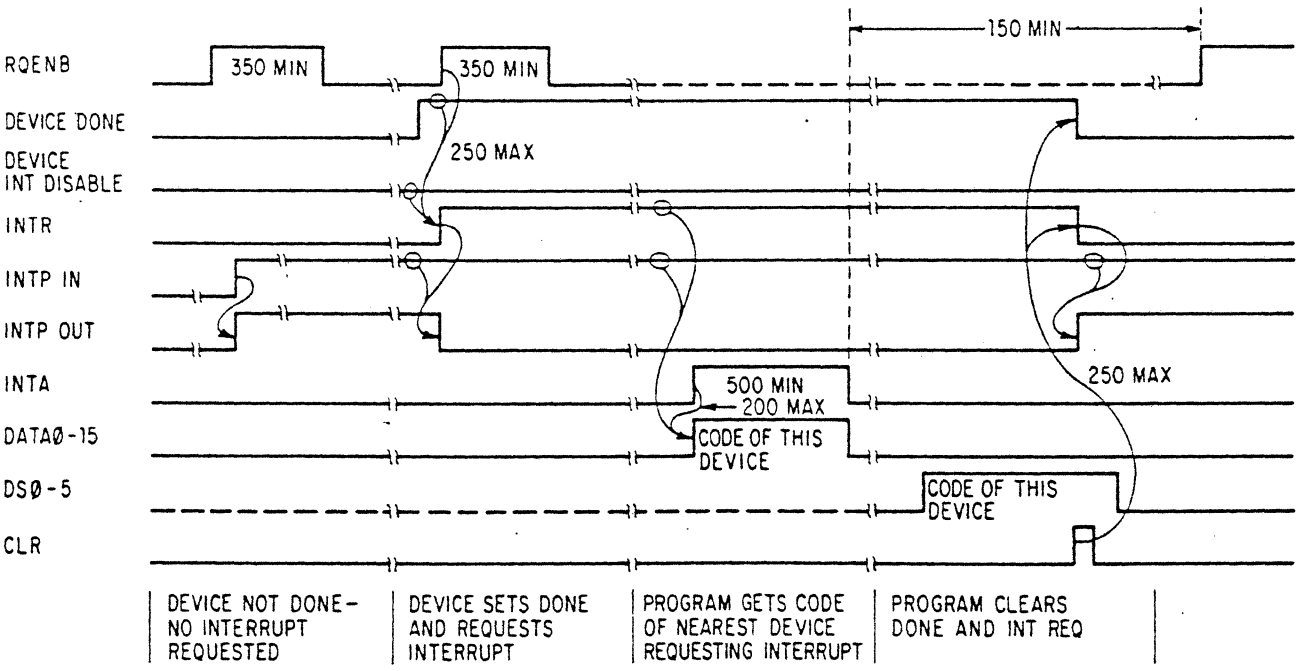


Figure 4-11 PROGRAM INTERRUPT

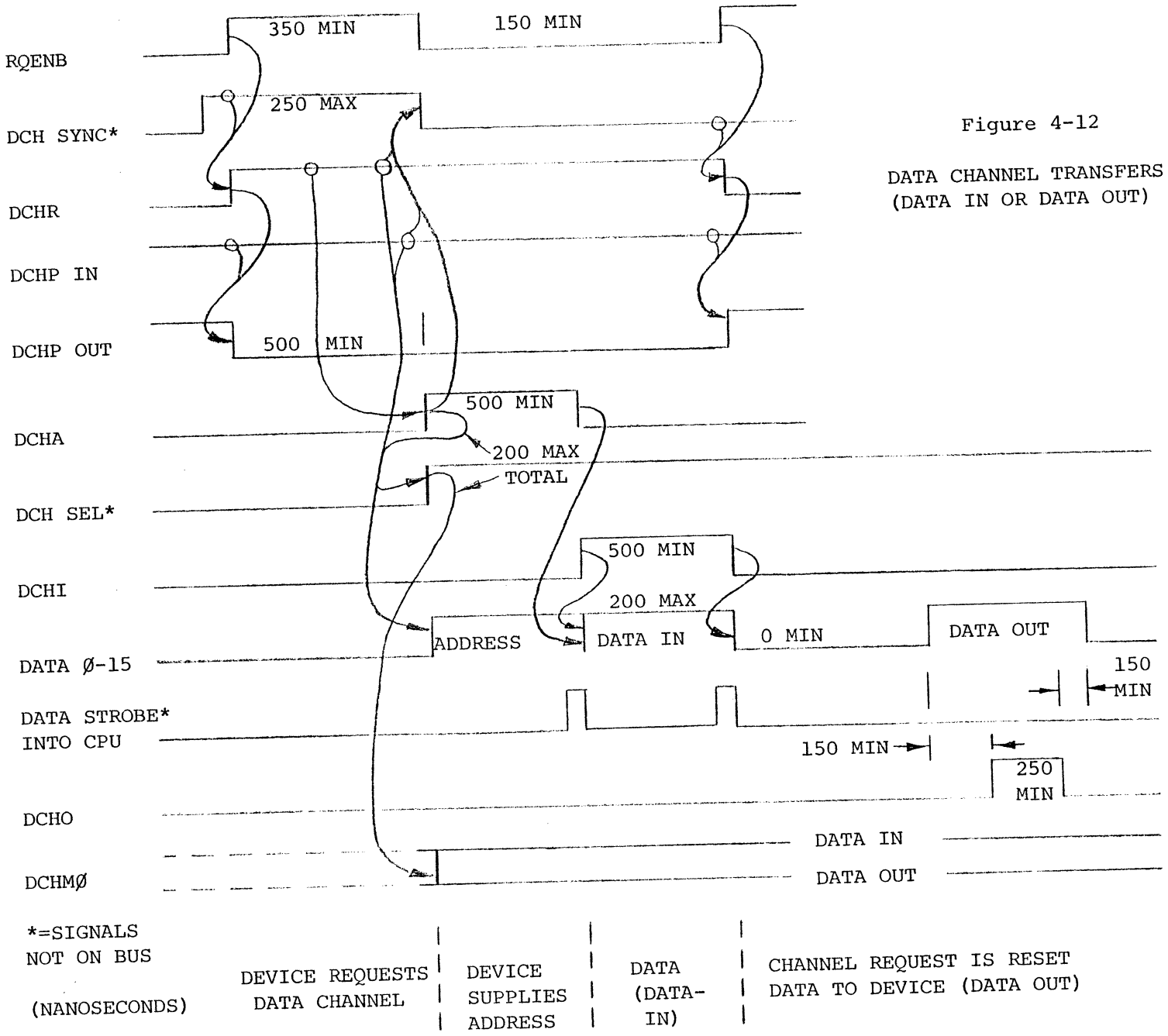


Figure 4-12

DATA CHANNEL TRANSFERS
(DATA IN OR DATA OUT)

4.36 CONTROLLER BLOCK DESCRIPTION

4.37 The operation of the controller is based on and controlled by two sequence counters which execute the functions of the controller. The Main Sequencer, together with the Delay Generator, handles the timing for the format of the data on tape. The Write/Read Sequencer transfers tape characters to and from the FIFO in the correct order. Interfacing with the computer bus, the controller provides the required control, status, data transfer, interrupt and formatting functions to control and operate standard tape drives. The result is a controller which adheres to standard interfacing requirements and produces compatible tapes as described in previous paragraphs. A block diagram of the tape controller is shown in Figure 4-13, which is summarized in the following paragraphs.

4.38 COMPUTER DATA BUS INTERFACE. This logic block contains tri-state bus transceivers to interface the computer bus data lines with the internal tri-state data bus of the controller. The interface passes data between the controller's internal bus and the computer bus with the direction of transfer controlled by the type of operation being performed. Memory address from the Address Register are provided over these lines during Data Channel operations. The controller places its device code on these lines during an interrupt.

4.39 PROCESSOR I/O CONTROL. This logic handles the bus control signals used for processor access to the registers of the controller. This logic also receives and decodes the Device

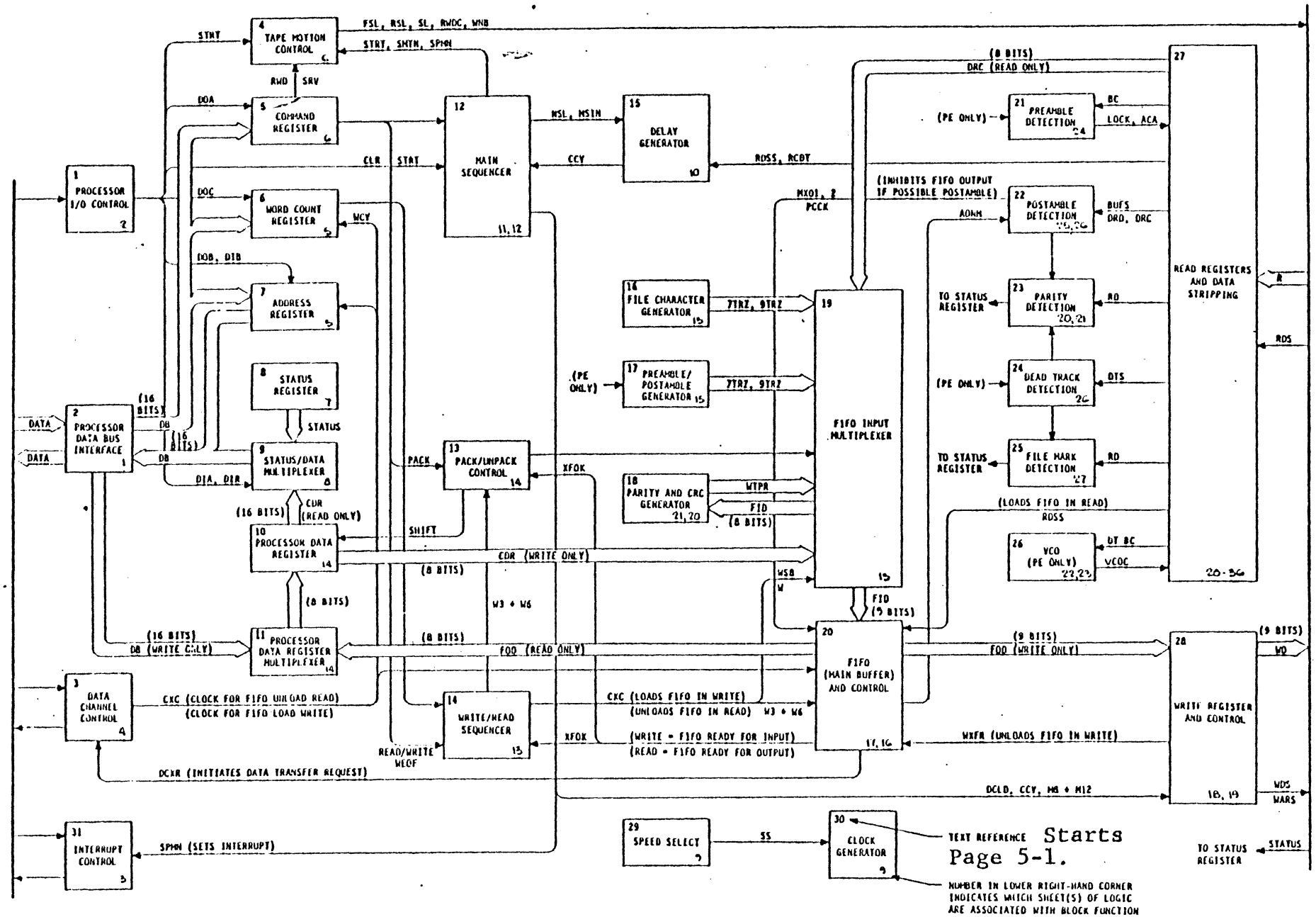


Figure 4-13 TC120 BLOCK DIAGRAM

Select signal and generates the Busy and Done signals. Included is the logic for the Start, Clear, and I/O Reset functions.

4.40 INTERRUPT CONTROL. This logic interrupts the processor when the Done flip/flop is set at the end of each operation, or if an illegal command is received. This circuit requests interrupts and processes the priority and acknowledge signals returned from the processor. It supplies the device code to the processor and also passes the priority to the next device when the controller is not interrupting. This circuit also receives the Mask bit for interrupt enable/disable.

4.41 DATA CHANNEL CONTROL. This logic generates and handles all the bus control signals required for Data Channel memory access when the controller is transferring magnetic tape data during execution of tape data operations.

4.42 ADDRESS REGISTER. This register is loaded and examined through the internal bus. During Data Channel activity, the register provides current address information through the I/O Bus Interface to the processor. The Programming Section includes detailed information on this register.

4.43 WORD/RECORD COUNT REGISTER. This write-only register is loaded through the internal bus of the controller with the two's complement of the number of words to be transferred or record to be spaced-over. The register counts out the computer words (or records, when spacing). When maximum count is reached, the Write/Read Sequencer is signaled to terminate the operation after the

next operation. Refer to the Programming Section for more information.

4.44 COMMAND REGISTER. This circuit receives and latches the Command Register bits and decodes and distributes the command functions and drive selections. Additional circuits provide Error Summary, Busy and other status bits. The functions of the command Register bits are explained in the Programming section of the Manual.

4.45 DRIVE CONTROL. The Drive Control circuit drives all the control signals provided to the tape unit through the control interface cable. A flip/flop in the circuit provides control of the tape motion command signals.

4.46 STATUS LOGIC. This logic receives status information from the drive and from controller circuits. These signals are latched, checked for error conditions and/or distributed to controller circuits. Many of these signals are also provided to the Status/ Data Multiplexer as Status Register bits. The Busy latch is also contained in this logic.

4.47 STATUS/DATA MULTIPLEXER. This multiplexer is enabled when transferring data from tape as well as when the processor is reading the Maintenance Register (Data Register) or the Status Register. The multiplexer accepts data from the Data Register and status from the various status circuits and provides a path for this information to the internal bus of the controller.

4.48 CLOCK GENERATOR. This circuit is the source for all controller system clocks. It consists of two crystals, and the associated crystal selection and clock line driver circuits.

4.49 SPEED DIVIDER. This logic contains the speed clock counter and the speed select switches to provide a system clock proportional to the tape speed of the selected drive.

4.50 DELAY GENERATOR. This logic block consisting of proms and counters, generates all the delay times, time-outs, and tape clock rates for the various states of the main sequencer. See Table 4-4.

4.51 START CONTROL. This logic receives and executes the Start function. If the command is valid and requires sequencer action, the Start Motion signal is developed to start the Main Sequencer and initiate tape motion. This circuit also checks for and initiates non-stop operations.

4.52 MAIN SEQUENCER. This block contains the main sequence counter and associated control and decoding logic. This sequencer generates the control signals used for generating and handling the interrecord gap and character spacing for the data on tape. As well as controlling various circuits, the Main Sequencer addresses delays in the Delay Generator which produces the required delays, strobes, and timeouts. The main sequence states are:

1. Idle - StateØ - In this state the sequencer is waiting for a start command for the next operation.

CRYSTAL OSCILLATOR	"XTAL"	"CLK" PERIOD					
Normal Source 7.2 mhz	139 ns	12.5 us	6.25 us	4.17 us	3.47 us	2.08 us	1.25 us
Alternate 5 mhz Source	200 ns	18.0 us	9.00 us	6.00 us	5.00 us	3.00 us	1.80 us
SPEEDS:		12.5 ips	25 ips	37.5 ips	45 ips	75 ips	125 ips

STATE	TYPE DELAY	SPEEDS						Decimal Delay Constant	Octal 2's Comp.	Prom Address	
		12.5ips	25 ips	37.5ips	45 ips	75 ips	125ips			Oct.	Dec.
0	IDLE	12.50 us	6.25 us	4.17 us	3.47 us	2.08 us	1.25 us	-1	177777	0	0
1	STOP Delay	31.99 ms	15.99 ms	10.66 ms	8.89 ms	5.33 ms	3.20 ms	-2559	173001	1	1
2 * ●	Post Delay Forward 9 Track - Write	2.86 ms	1.43 ms	954.00 us	795.00 us	477.00 us	286.20 us	-159	177541	22	18
2 ●	Post Delay Forward 7 Track - Write	20.14 ms	10.07 ms	6.71 ms	5.60 ms	3.36 ms	2.01 ms	-1119	175641	2	2
2 *	Post Delay Forward 9 Track - Read	1.98 ms	993.75 us	662.50 us	552.08 us	331.25 us	198.75 us	-159	177541	22	18
2	Post Delay Forward 7 Track - Read	13.99 ms	6.99 ms	4.66 ms	3.89 ms	2.33 ms	1.40 ms	-1119	175641	2	2
3 *	Post Delay Reverse Normal	11.99 ms	5.99 ms	4.00 ms	3.33 ms	2.00 ms	1.20 ms	-959	176101	23	19
3	Post Delay Reverse Edit Mode	15.99 ms	7.99 ms	5.33 ms	4.44 ms	2.66 ms	1.60 ms	-1279	175401	3	3
4	Start Delay Write Extended Gap	361.59 ms	180.79 ms	120.53 ms	100.44 ms	60.26 ms	36.16 ms	-28927	107401	4	4
5	Start Delay Write Normal	33.99 ms	16.99 ms	11.33 ms	9.44 ms	5.66 ms	3.40 ms	-2719	172541	5	5
5 *	Start Delay Write PE Load Point	47.99 ms	23.99 ms	16.00 ms	13.33 ms	8.00 ms	4.80 ms	-3839	170401	25	21
6	Start Delay Read Load Point	39.99 ms	19.99 ms	13.33 ms	11.11 ms	6.66 ms	4.00 ms	-3199	171601	6	6
7	Start Delay Read Normal	19.59 ms	9.79 ms	6.53 ms	5.44 ms	3.26 ms	1.96 ms	-1567	174741	7	7
8 *	Write Clock Period 200 BPI	400.00 ms	200.00 us	133.33 us	111.11 us	66.67 us	40.00 us	-32	177740	30	24
8 ●	Write Clock Period 556 BPI	144.00 us	72.00 us	48.00 us	40.00 us	24.00 us	14.40 us	-8	177770	10	8
9 *	Read Activity Timeout 200 BPI	1.00 ms	500.00 us	333.33 us	277.78 us	166.67 us	100.00 us	-80	177660	31	25
9 ●	Read Activity Timeout 556 BPI	360.00 us	180.00 us	120.00 us	100.00 us	60.00 us	36.00 us	-20	177754	11	9
10 *	End of Record Timeout 200 BPI	3.20 ms	1.60 ms	1.07 ms	888.89 us	533.33 us	320.00 us	-256	177400	32	26
10 ●	End of Record timeout 556 BPI	1.15 ms	576.00 us	384.00 us	320.00 us	192.00 us	115.20 us	-64	177700	12	10
12	Write Clock Period 800 BPI	100.00 us	50.00 us	33.33 us	27.78 us	16.67 us	10.00 us	-8	177770	14	12
12 *	Write Clock Period 3200 FCI	25.00 us	12.50 us	8.33 us	6.94 us	4.17 us	2.50 us	-2	177776	34	28
13	Read Activity Timeout 800 BPI	250.00 us	125.00 us	83.33 us	69.44 us	41.67 us	25.00 us	-20	177754	15	13
13 *	Read Activity Timeout 3200 FCI	125.00 us	62.50 us	41.67 us	34.72 us	20.83 us	12.50 us	-10	177766	35	29
14	End of Record Timeout 800 BPI	800.00 us	400.00 us	266.67 us	222.22 us	133.33 us	80.00 us	-64	177700	16	14
14 *	End of Record Timeout 3200 FCI	50.00 us	25.00 us	16.67 us	13.89 us	8.33 us	5.00 us	-4	177774	36	30

*Selects second delay constant ● Uses alternate crystal

All values rounded, as required

TABLE 4-4 MAIN SEQUENCER CLOCK AND DELAY TIMES

2. Start Delay State 4, 5, 6, or 7 - These states delay writing, reading, or detection of a record until tape is up to speed and until the tape format requirements are met. The ID burst is written in State 4 if the operation starts at load point and the controller is in Phase Encoded mode.
3. Write Mode State 8 or 12 - These states are entered in the write modes only and are used for timing the actual strobing of data onto tape. Tape density is regulated by the delay accessed by these modes.
4. Read Mode State 9 or 13 - These timeout delays are used to detect end-of-record missing characters in all data and spacing modes. These states are also used during transfer of read data in the Read Mode and when detecting records in the Space Mode.
5. End-of-Record Mode State 10 or 14 - These timeout states are used to wait for CRC and LRC characters at the end of a record and to detect the interrecord gap.
6. Post Delay State 2 or 3 - These states provide a delay between end-of-record detection and stopping of tape to provide proper format-compatible gap lengths.
7. Stop Delay State 1 - This state provides a delay after removal of the motion command to allow the tape to come to a complete stop. This delay is omitted when performing automatic non-stop operations.

STATE	FUNCTION	COMMENTS
0	IDLE	Waiting for next operation
1	STOP DELAY	Waiting for tape to completely stop motion.
2	POST DELAY FORWARD	Delays stopping of tape for correct Positioning in gap and to provide proper gap length when writing.
3	POST DELAY REVERSE	
4	START DELAY WRITE (BOT)	Delay after starting of tape to allow tape speed to stabilize at full speed.
5	START DELAY WRITE	
6	START DELAY READ (BOT)	
7	START DELAY READ	
8	WRITE MODE 200 BPI, 556 BPI	Entered in write mode only Writes information on tape
12	WRITE MODE 800 BPI, PE	
9	READ MODE 200 BPI, 556 BPI	Transfers read information in read mode. Waits for end of record in write mode.
13	READ MODE 800 BPI, PE	Detects record in space mode.
10	END OF RECORD 200 BPI, 556 BPI	Additional delay at end of record to allow reading of CRC and LRC characters
14	END OF RECORD 800 BPI, PE	

Table 4-5 Main Sequencer States

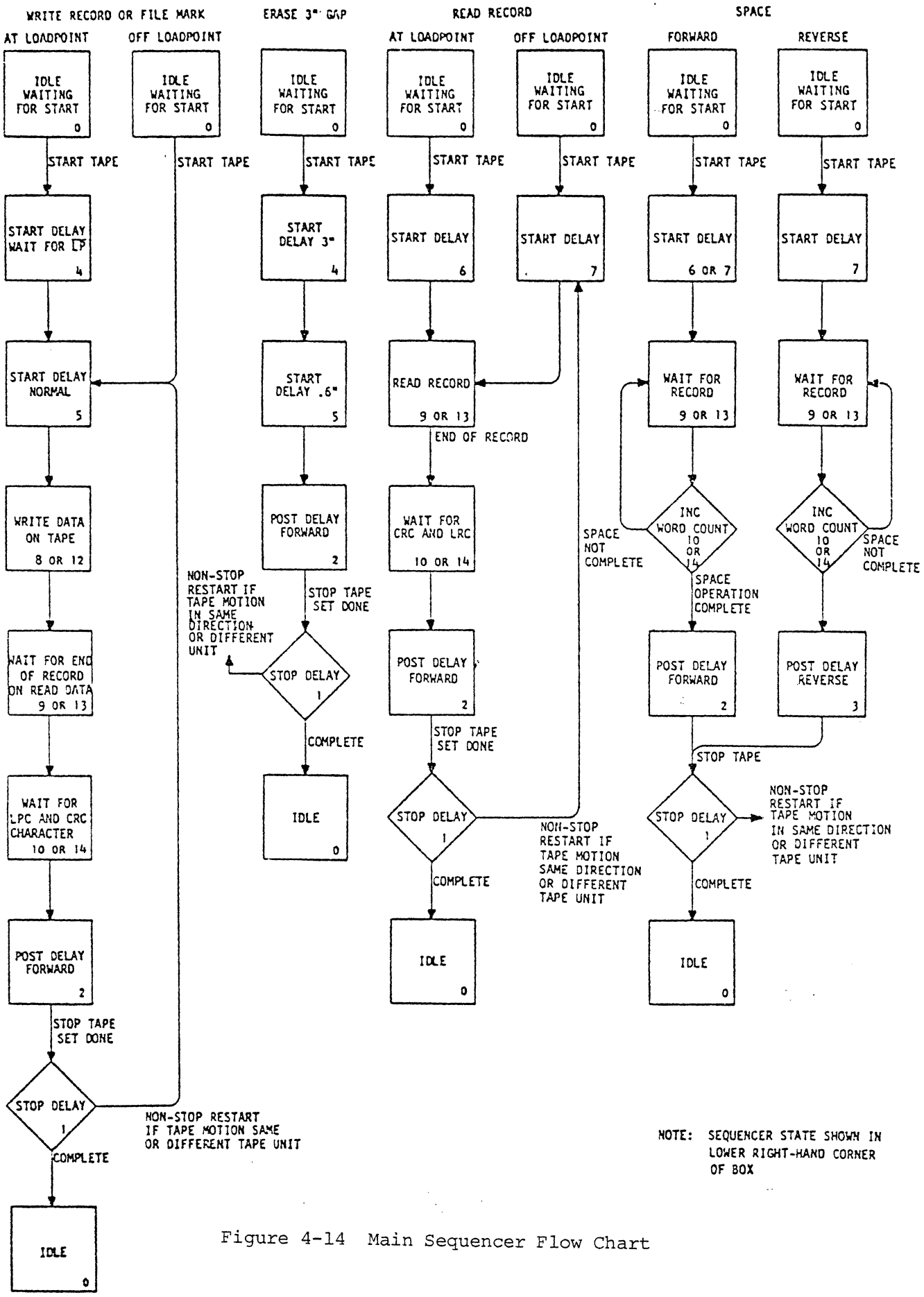


Figure 4-14 Main Sequencer Flow Chart

4.53 WRITE/READ SEQUENCER. (See Tables 4-6 and Figure 4-15). This sequencer controls and formats data transfers between the Data Register and the FIFO (First In, First Out main buffer). Also, the sequencer handles the generation of required format characters. The Write/Read sequences are:

1. Preamble Zeros State Ø - The sequence, enters this state to generate the all-zero characters when writing the preamble in the PE mode. The sequencer remains in this state for 40 clock times, until 40 characters are generated.
2. Preamble One State 1 - This state is used to generate the all-ones character when writing the preamble in the PE mode.
3. First Character State 2 - This state is repeated during normal writing and reading operations for packing and unpacking the first character of each computer word.
4. Second Character State 3 - This state is repeated during normal writing and reading operations for packing and unpacking the second charcter of each computer word.
5. First Packed Character State 4 - This state is repeated during packed writing and reading operations for packing and unpacking the first character (4 bits) of each computer word.
6. Second Packed Character State 5 - This state is repeated during packed writing and reading operations for packing and unpacking the second character (6 bits) of each computer word.

7. Third Packed Character State 6 - This state is repeated during packed writing and reading operations for packing and unpacking the third character (6 bits) of each computer word.
8. File Mark Character State 7 - The sequencer enters this state in the NRZI mode to generate the special file mark character when writing a NRZI file mark.
9. Postamble One State 8 - This state is used to generate the all-ones character when writing the postamble in the PE mode.
10. Postamble/File Mark Zeros State 9 - The sequencer enters this state to generate the all-zero characters when writing the postamble or file mark in the PE mode. The sequencer remains in this state for 40 clock times, until 40 characters are generated.
11. CRC Gap State 10 - The sequencer enters this state to generate the all-zero characters (blanks) between the final data character and the CRC character when writing in the 9 track NRZI mode. The sequencer remains in this state for 3 clock times until the 3 characters are generated. When writing a NRZI file mark, these 3 characters become part of a long LRC gap, since the CRC is replaced by an all-zero character (blank).
12. CRC Character State 11 - This state generates the CRC character when writing in the 9 track NRZI mode. When writing a NRZI file mark, this character is replaced by an all-zeros character (blank) which becomes part of a long LRC gap.

13. LRC Gap State 12 - The sequencer enters this state to generate the all-zero characters (blanks) preceeding the LRC character when writing in the NRZI mode. The sequencer remains in this state for 3 clock times until 3 characters are generated.

14. LRC/Reset State 13 - This state generates the reset for the tape drive write circuits. This creates the LRC character when writing in the NRZI mode.

4.54 DATA REGISTER MULTIPLEXER. In a write operation, this multiplexer gates I/O bus data bits 8 through 15 into the Data Register. (Bits Ø through 7 are provided directly to the register.) In a read operation, it gates the FIFO output into the Data Register. The third section of the multiplexer is needed for the 7 track packed mode.

4.55 DATA REGISTER. The Data Register is the temporary storage register which provides the initial data buffering where data is held just prior to being stored in memory, or just after being read from the memory and is used to implement the packing and unpacking of data between a 16-bit processor word and the 4-, 6- or 8-bit tape characters. Complete 16-bit words are always transferred to or from memory.

4.56 PACK/UNPACK CONTROL. This circuit controls the shifting of the Data Register to assemble and disassemble processor data and tape data. For normal transfers, this circuit executes 8-bit shifts. For data transfers in the 7-track memory dump packed mode, the register shifts 6 places per shift sequence.

TABLE 4-6

WRITE/READ SEQUENCER STATES

STATE	FUNCTION	# Clock Cycles	USE
0	Generate 40 Preamble Zeros	40	Write Phase Encoded Only
1	Generate Preamble All Ones	1	Write Phase Encoded Only
2	Process First Character (Nonpack)	1	Read and Write non 7 track or 7 track non pack
3	Process Second Character (Nonpack)	1	Read and Write non 7 track or 7 track non pack
4	Process First Character (Pack)	1	Read and Write 7 track pack mode only
5	Process Second Character (Pack)	1	Read and Write 7 track pack mode only
6	Process Third Character (Pack)	1	Read and Write 7 track pack mode only
7	Generate File Mark Character	1	NRZ Write File Mark only
8	Generate Postamble All Ones	1	Write Phase Encoded only
9	Generate 40 Postamble Zeros	40	Write Phase Encoded only
10	Generate 3 Character CRC Gap	3	Write 9 track NRZ only
11	Generate CRC Character	1	Write 9 track NRZ only
12	Generate 3 Character LRC Gap	3	Write NRZ only
13	Generate LRC Character	1	Write only

TABLE D

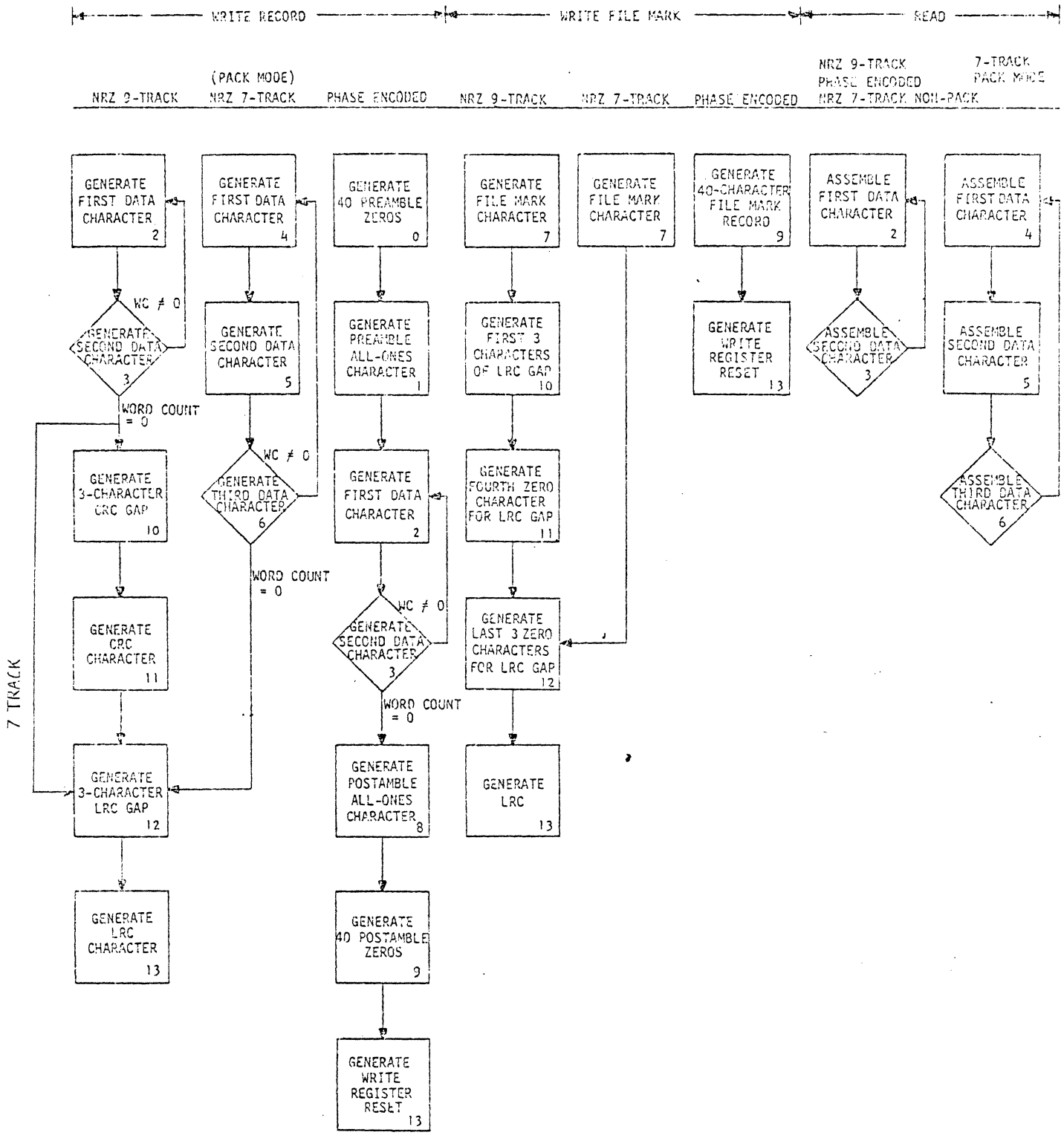


Figure 4-15 Write/Read Sequencer Flow Chart

4.57 FILE MARK/ZERO/ALL-ONES CHARACTER GENERATOR. These circuits create the seven track and nine track file mark character codes at the FIFO input Multiplexer. In addition, this logic creates the all-zeros and all-ones characters at the FIFO Input Multiplexer to write the Preamble and Postamble in Phase Encoded records and the all-zero characters for the CRC gaps and LRC gaps in NRZI records.

4.58 FIFO INPUT MULTIPLEXER. This logic multiplexes information into the FIFO. This information includes:

1. Read Data
2. Write Data
3. File Mark Data
4. Preamble, Postamble, and Gap Data (all Zeros)
5. All Ones

4.59 FIFO CONTROL. In addition to generating clocks for the FIFO, the FIFO Control handles stripping of CRC and LRC characters as well as postamble data so that Data presented to the CPU has the format and check characters removed.

4.60 FIFO. This is the main buffer for write and read data, and the control for the transfer of the data into and out of the FIFO. This logic block contains a 64 character FIFO (First In-First Out Memory) that stores the data being transferred in either direction. This becomes the temporary holding device for examination of the postamble, and also provides a substantial data buffer that eases programming considerations in the computer.

4.61 WRITE CLOCK GENERATOR. While the Delay Generator develops overall timing which determines recording density, this counter circuit generates relative timing to transfer data through the Write Register and to strobe the data to the tape drive.

4.62 WRITE REGISTER. This register stores, processes and gates output data from the FIFO buffer to the tape write bus during write operations. Included is logic to add PE clock transitions to the data.

4.63 PARITY/LRC CHECKER. This logic checks the lateral and longitudinal parity and reports these and other format errors in the data read from tape.

4.64 PARITY GENERATOR. This logic circuit generates the lateral (ODD or EVEN) character parity used for write data operations.

4.65 CRC GENERATOR. This logic calculates and generates the Cyclic Redundancy Check Character for 9-track NRZI tapes.

4.66 VCO CONTROL. This circuit supplies data rate information to the VCO from one of two master tracks. The second track is a back-up in case the first reference track goes dead.

4.67 VCO. This Voltage Controlled Oscillator is a data rate error compensating Phase Locked Loop for the Read Channels when reading Phase Encoded data. It locks onto one of two master tracks (Track 2 or 1), providing a time base that is a function of the actual data rate for the recovery of the phase encoded data. This mode of recovering data is able to tolerate wide

variations in tape speed, assuring a high degree of data integrity.

4.68 PREAMBLE DETECTOR. This logic detects read activity on any channel and then, after approximately thirty-two character times, releases the data channels to check for dead tracks and to look for the sync bits. (Phase Encoded mode only.)

4.69 POSTAMBLE DETECTOR. This circuit detects all possible and real postamble character patterns. It inhibits output of the FIFO if the FIFO's output is an all Ones character that could be the start of the postamble. The PE Postamble consists of one tape character of all-ones followed by forty tape characters of all-zero bits. The postamble detector examines all of these characters and strips them from the read data. In cases where one track is being corrected, it prevents false postambles from being misinterpreted. This is most important with marginal or dirty tapes, as it prevents data from being lost due to premature detection of false postambles. (Phase Encoded mode only.)

4.70 DEAD TRACK DETECTOR. This logic detects single or multiple dead tracks in the Read data. Due to the self-clocking nature of phase encoded data, it is possible to detect bit dropouts in the data. Single dead tracks have automatic data correction: When a bit is dropped, a dead track detector senses it immediately and the data recovery electronics go into the data correction mode whereby parity information is used to restore the lost data. This is known as a "soft error" in the Read mode. If more than one track has bit dropouts in a single block, then a multiple dead track error is detected and error correction is impossible.

This is defined as a "hard error". Multiple dead track errors set Parity Error status. Other conditions detected in this circuit include all-ones, all-zeros, and PE file mark dead tracks.

4.71 FILE MARK DETECTOR. This circuit detects File Mark records picked up by the read data electronics and reports them via the Status Register.

4.72 READ LOGIC. For NRZI read data from tape, this logic block contains a buffer which also acts as a transition detector for Phase Encoded read data from tape. Due to the combination of high density (1600 bits per inch) of the data recorded on tape and the non-controllable portion of static and dynamic skew characteristics of the drive, phase encoded data may have as much as one bit displacement in writing and an additional one bit displacement in reading, resulting in a net possible two bits of bit-to-bit displacement to the controller according to format specifications. In order to recover the data properly, each track has a standard four-bit deskew register that is used in reassembling the data byte. Other PE functions include read window generation (for clock transition removal), sync bit detection, dead track detection, and error correction.

4.73 MISCELLANEOUS LOGIC. Other circuits in the Controller include Load Point Start, Read Strobe Synchronizer, NRZI/PE Control, and Record Detector.

APPENDIX A

SIGNAL GLOSSARY

This appendix contains a glossary of logic terms appearing on the controller logic diagrams.

TERM LIST

ORIGIN	NMONIC	TERM	COMMENTS
	+5R	+5 Volts Resistive	Used as pullups for unused gates.
24	ACA	Any Channel Active	(Phase Encoded only.) Detects a read transition on any track except the parity track ↑ =ACA=BC0+BC1+BC2+ BC3+BC4+BC5+BC6+BC7.
24	ACAS	Any Channel Active Synchronized	ACA synchronized with "VCRD."
17	AONM	All Ones Marker	Indicates the FIFO output is an all Ones character. Used to detect possible start of postamble in Read Mode. (Phase Encoded only.)
28-36	BC0-7,P	Bit Clock 0,7,P	Cell transition clock for read data. (Phase Encoded only.)
7	BOT	Beginning of Tape	Status from tape transport indicating that tape is positioned at the load point marker.
10	BOTH	Beginning of Tape Hold	Holds of start forward start delay until beginning of tape status is false.
7	BOTP	Beginning of Tape	Unbuffered status signal from tape transport.
12	BOTS	Beginning of Tape Synchronized	"BOT" synchronized with "CLK."
20	BTE	Bad Tape Error	Set when 3 or more characters are detected after end of record is detected or when an One character record is detected that is not a file mark.
17	BUFC	Buffer Clock	Clock used to update output of read deskew register to next character. (Phase Encoded only.)

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
17,15, 28-36	BUFF	Buffer Full	Indicates when a complete character is present on output of Deskew Register (Phase Encoded only.)
17	BUFS	Buffer Full Synchronized	"Buff" synchronized with "CLK."
7	BUSY	BUSY	Status to processor indicating that controller is busy doing a tape operation.
5	CAEN	Current Address Enable	Gates the address register onto the "DB" bus during a "DIB" or "DMAA" cycle.
22	CARD	Reference Channel Active Detector	Switches VCO reference from "XTAL" to active reference channel (2 or 1). (Phase Encoded only.)
10	CCY	Delay Counter Carry	Indicates delay counter has reached maximum count.
14	CDI8-15	Computer Data Register Input 8-15	Multiplexed input to computer data register bits 8-15. During write = DB8 - DB15. During Read = FO-7.
16	CDRC	Computer Data Register Control	Indicates when computer data register is full or empty. True indicates full in write operation and empty in read operation.
14	CDRO-15	Computer Data Register Bits 0-15	Data Register used for packing and unpacking of data and transfer to or from processor.
16	CDXR	Computer Data Transfer	Indicates transfer of data between "FIFO" and "CDR."
4	CHRQ	Channel Request	Requests data channel access to processor.
2	CLEAR	CLEAR	Clear IOP from processor I/O Bus.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
9	CLG	CLOCK ÷ 2	Used to implement IB burst write strobe. (Phase Encoded only.)
9	CLK	CLOCK	System clock rate = tape speed x 6400.
2	CLR	CLEAR	"CLEAR" gated with tape device code.
17	RST + CLR	CLEAR or RESET	Clear or reset command from processor.
6	CMCL	COMMAND CLOCK	"DOA" gated with tape device code. Clock used to load the command register.
16	CPE	Corrected Parity Error	Indicates that a single dead track has been detected during read operation. (Phase Encoded only.)
21	CRCC	Cyclic Redundancy Clock	Clock that generates the CRC character during a write operation. (9 track NRZ only.)
15	CREN	Cyclic Redundancy Enable	Gates the CRC generator onto the "FID" Bus.
14	CWCL	Computer Word Register Clock	Clock used for loading and shifting of the "CDR."
4	CXC	Computer Transfer Clock	Clock generated at the end of a DMA cycle or at detection of a record in a space operation.
28-36	C12-0-7, P	Carry Count 12	Carry output of first stages of window counter. (Phase Encoded only.)
1	DATA 0-15	Data Bits 0-15	Processor Data Bus.
2	DATI A, B, C	Data in A, B, C	Processor Data in I/O Clocks.
2	DATO A, B, C	Data Out A, B, C	Processor Data Out I/O Clocks.

TERM LIST (Continued)

RIGIN	NMONIC	TERM	COMMENTS
1	DBO-15	Data Bus 0-15	Buffered processor data bus.
4	DCHA	Data Channel Address	Gates the address register onto the processor data bus during the address phase of a data channel access.
4	DCHI	Data Channel In	Gates the "CDR" onto the processor data bus during a data channel in cycle.
4	DCHMO	Data Channel Mode Out	Selects data out mode during a data channel access.
4	DCHO	Data Channel Out	Loads the processor data bus into the "CDR" during a data channel out cycle.
4	DCHP IN, OUT	Data Channel Priority In, Out	Processor serial priority line for data channel.
4	DCHR	Data Channel Request	Processor data channel request bus.
4	DCHS	Data Channel Select	Indicates that this device has the highest priority if it is requesting a data channel.
4	DCI	Data Channel In	Gates "CDR" onto processor data bus.
4	DCO	Data Channel Out	Loads the processor data bus into the CDR during a DMA operation.
4	DCR	Data Channel Request	Initiates data channel request.
16	DCXR	Data Channel Transfer Request	Sets "DCR" and resets "CDRC."
2	DIA + DIR	"DIA" or "DIR"	Used to enable the status and data multiplexer onto the "DB" bus.

TERM LIST (Continued)

RIGIN	NMONIC	TERM	COMMENTS
2	DIA	Data in "A"	I/O command from processor that reads the status register.
2	DIB	Data in "B"	I/O command from processor that reads the address register.
2	DIX	Data in Transfer	Gates the "DB" bus onto the processor data bus during any I/O or DMA transfer to processor.
10	DLCD	Delay Clock Delayed	Delay counter time out delayed by one clock time in order to load new constant from ROM into delay counter.
10	DLCR	Delay Counter Preset	Presets the delay counter to the ROM output.
14	DLD	Data Load	Initiates pack/unpack SHIFT of "CDR" loads FIFO data into "CDR" in read operation.
21	DLDG	Data Load Gated	Used to generate CRC clock and read load of "CDR."
4	DMAA	Direct Memory Access Address	Gates the address register onto the processor data bus during a data channel transfer.
15	DMEN	Data Multiplexer Enable	Gates the data multiplexer onto the "FID" bus except when CRC is being written or an all Ones character is being written.
15	DMES	Data Multiplexer Enable Seven Track	Same as "DMEN" except it disables two most significant bits when in seven track mode.
15	DMSL	Data Multiplexer Select	Select control for data multiplexer (least significant bit).
2	DOA	Data Out "A"	Clock from processor I/O that loads the command register.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
2	DOB	Data Out "B"	Clock from processor I/O that loads the address register.
2	DOC	Data Out "C"	Clock from processor that loads the word count register.
14	DOMD	Data Out Mode	Switches "CDR" clock to DCHO during a data channel out transfer from processor to controller.
3	DONE	DONE	Done flag to processor indicating that the requested operation is complete.
28-36	DRCO-7,P	Data Read Corrected 0-7,P	Corrected read data from tape read register.
28-36	DRDO-7,P	Data Read 0-7,P	Uncorrected read data from tape read register. Data = "0" if track is dead. (P.E.)
6	DSL	Density Select	Command register density control bit True = low density, False = high density.
2	DSO-5	Device Select 0-5	Processor I/O Device Select.
26	DTAL	Dead Track All	Detects end of phase encoded record at read head. (P.E. only.)
26	DTM	Dead Track Multiple	Indicates that more than one track is dead when reading a phase encoded record. (P.E. only.)
22	DTR	Dead Track Reference	Indicates that VCO reference track is dead. Causes VCO to switch to alternate reference track. (P.E. only.
26	DTS	Dead Track Single	Indicates that only one track is dead when reading phase encoded data. (P.E. only.)

RIGIN	NMONIC	TERM	COMMENTS
28-36	DTSO-7,P	Dead Track Synchronized 0-7,P	"DT" synchronized with "CLK." (P.E. only.)
28-36	DTO-7,P	Dead Track 0-7,P	Indicates no detection of transition on read channel. (P.E. only.)
6	EDIT	Edit Mode	Command register bit that sets up over Write mode.
7	EOT	End-of-Tape	Buffered status from Tape Transport indicates tape position is past the end-of-tape marker.
7	EOTP	End-of-Tape	Unbuffered "EOT."
11	EOTS	End-of-Tape Synchronized	"EOT" synchronized with "CLK."
21	EPC	Even Parity Check	Checks tape read parity False = Odd parity True = Even parity
20	EPS	Even Parity Select	Controls parity generator False = Odd parity True = Even parity
7	ERR	ERROR	Bit 0 of status register. True if any of the following are true: OLR + FM + BOT + RJCT + EOT + TMR+ BTE + PER.
6	EVP	Even Parity	Parity control bit of command register. False selects odd parity. True selects even parity.
27	FCC1,2	File Check 1,2	2 bit counter that counts number of characters detected after end-of-record detection.
27	FCC3	File Check 3	Sets if more than one character is detected in a record.

TERM LIST (Continued)

RIGIN	NMONIC	TERM	COMMENTS
6	FCT1,2,4	Function 1,2,4	Command register function code (3 bits). 0 = Read 1 = Rewind 2 = No effect 3 = Space Forward 4 = Space Reverse 5 = Write 6 = Write End-of-File 7 = Write 3" Gap
17	FICC	F1FO Clock Control	"SCY" delayed by one "XTAL" time for implementing F1FO control and other miscellaneous timing considerations.
17	FICL	F1FO Input Clock	Used to clock data into F1FO data buffer.
15	FIDO-7,P	F1FO Input Data 0-7,P	F1FO data input bus.
16	FILD	F1FO Input Load	Control that indicates data is ready to be loaded into F1FO.
17	FIR	F1FO Input Ready	Indicates F1FO is ready to accept data input.
7	FIRST	First Character	Status indicating detection of beginning of record at read head.
17	FI1,2,3	F1FO Input Ready 1,2,3	Raw F1FO input ready signals.
7	FLPT	File Protect	Unbuffered file protect status from tape indicates no write operations can be executed.
27	FM	File Mark	Status indicating that a file mark has been detected by read head either NRZ or Phase Encoded.
27	FMDT	File Mark Detect	NRZ file mark detect status.
27	FMRS	File Mark Reset	Resets file mark detect logic if a file mark is not detected at end-of-record.

RIGIN	NMONIC	TERM	COMMENTS
11	FNCP	Function Complete	Terminates space operation when true.
17	FOCL	F1FO Output Clock	Updates F1FO output to next available character.
17	FODO-7,P	F1FO Output Data 0-7,P	F1FO output bus.
16	FOLD	F1FO Output Load	Control used to update F1FO output to next character.
28-36	FONO-7,P	First One Detector 0-7,P	Detects end of preamble of read data (P.E. only).
17	FOR	F1FO Output Ready	Indicates data is ready at output of F1FOS.
17	F01,2,3	F1FO Output Ready,1,2,3	Raw F1FO output ready status.
7	FPT	File Protect	Buffered file protect status indicating tape can not be written on.
6	FSL	Forward Synchronous Line	Control to tape unit that causes it to run forward.
6	GAP	GAP	Command function decode that writes a 3 inch gap.
4	GEXS	Generate Extra Transfer	Transfers last word to processor if record odd length.
7	HDEN	High Density	Buffered status from tape indicating density configuration of tape in 9 track. False = PE and True = NRZ.
7	HDN	High Density	Unbuffered "HDEN" status.
20, 25	HER	Hard Error	Sets parity status if a non-correctable read error has occurred.
20	HPE	Hard Parity Error	Status indicating that a non-correctabl error has occured in read logic.

RIGIN	NMONIC	TERM	COMMENTS
20	IDEN	Identification	Status to processor indicating that tape being read is written in Phase Encoded.
3	INRQ	Interrupt Request	Initiates interrupt of computer upon completion of operation.
3	INTA	Interrupt Address	Gates the device code of the interrupting device onto the processor data bus when asserted.
3	INTPIN	Interrupt Priority In	Interrupt priority from processor or previous device.
3	INTPOUT	Interrupt Priority Out	Interrupt priority to next device.
3	INTR	Interrupt Request	Processor I/O interrupt request bus.
2	IORST	I/O Reset	Processor I/O bus reset.
24	LOCK	LOCK	Goes true after approximately 32 preamble bits have been detected allowing the read data channels to look for the first one bit.
6	LONG	Long Window	Optional control from command register to lengthen read window. (Phase Encoded only.)
7	LPST	Load Point Start	Indicates that tape operation was initiated with tape positioned at load point.
17	LRCW	Longitutional Redundancy Check Write	FlFO output that controls the resetting of the write amplifiers in a write operation.
3	MASK	MASK	Inhibits interrupt of processor when set.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
12	MSIN	Main Sequencer Increment	Increments the main sequencer counter to the next state.
3	MSKO	Mask Out	Strobe from processor to control the "MASK" Flip Flop.
12	MS1,2,4,8	Main Sequencer 1,2,4,8	4 bit main sequencer counter.
25	MX01,2	Maximum Count 1,2	Counts all One characters. When both lines true F1FO output contains last all Ones character in F1FOS.
12	MO-7	Main Sequencer Decode 0-7	Main Sequencer states decode.
12	M2+M3	Main Sequencer State 2 or 3	Main Sequencer post delay states.
12	M8+M12	Main Sequencer State 8 or 12	Main Sequencer write states.
12	M9+M13	Main Sequencer State 9 or 13	Main Sequencer read states.
12	M10+M14	Main Sequencer State 10 or 14	Main Sequencer end-of-record states.
6	NEF	No Effect Function	Command function has no effect on operation.
27	NFRS	Non File Mark Reset	Resets file mark detector at end of record if no file mark detected.
12	NSL	Next State Load	Loads main sequencer with next logical state required in an operation.
11	NS1,2,4,8	Next State Bits 1,2,4,8	Next state input to main sequencer counter.
13	NW1,2,4,8	Next Write State Bits 1,2,4,8	Next state input to write/read sequencer counter.

TERM LIST (Continued)

RIGIN	NMONIC	TERM	COMMENTS
24	OLR	Odd Length Record	Status to processor indicating that record read did not have correct integer multiple of characters required for the pack mode selected.
25	OMCL	Ones Monitor Clock	Clock that counts all ones characters on output of F1FOS. (Phase Encoded only.)
26	ONAL	One All	Indicates that read character is an all Ones character.
7	ONL	On Line	Raw status from tape transport indicating that selected transport is on-line.
7	ONLN	On Line	Buffered "ONL" status.
6	OVW	Over Write	Line on tape transport control bus that selects edit mode.
6	PACK	Pack Mode	Selects 4-6-6 packing in 7 track operation. (7 track only.)
25	PCCK	Postamble Count Check	Allows check of length of postamble.
20	PCCK*	Postamble Count Check Gated	"PCCK" anded with "PSER." Indicates when a possible postamble is being checked.
7	PE	Phase Encoded	Configures controller for Phase Encoded operation.
7	$\overline{PE}$ + $\overline{SRV}$	Phase Encoded or Synchronous Reverse	Controls inversion of read data.
27	PEFM	Phase Encoded File Mark	Indicates detection of file mark in Phase Encoded operation.

ORIGIN	NMONIC	TERM	COMMENTS
27	PENF	Phase Encoded Non File Mark	Negates file mark detection if end of preamble detected. (Phase Encoded only.)
25	PEOT	Postamble One Tabulate	Clocks possible postamble counter for every all Ones character loaded into F1FOS.
7	PER	Parity Error	Status to processor indicating an error in either the vertical or longitudinal parity of the read data in a write or read operation.
25	PPCE	Possible Postamble Count Enable	Enables the possible postamble counter to count up or down depending if a all Ones character is being loaded in or unloaded from F1FOS.
24	PRDT	Preamble Detect	Prevents "DTAL" from going True until ≈ 16 bits into the preamble.
20	PSCK	Postamble Check	Forces parity error if false postamble is detected with no single dead track.
25	PSER	Postamble Error	Terminates any possible postamble as being invalid.
15	PSOK	Postamble OK	Indicates possible postamble has detected between 32 and 48 all Zero's after an all Ones character.
18	PWFG	Phase Encoded Write File Mark Gated	Disables data on write track 1 when operating on 7 track or writing a Phase Encoded file mark.
18	PWFM	Phase Encoded Write File Mark	Disables tracks 3 and 4 when writing a Phase Encoded file mark.
27	RCDT	Record Detector	Detects read data activity.

RIGIN	NMONIC	TERM	COMMENTS
28-36	RDDO-7,P	Read Data Delayed	Stored read data delayed by 1 "VCOC" clock time. Used for transition detection.
28-36	RDO-7,P	Read Data 0-7,P	Unprocessed buffered read data from tape read bus.
7	RDS	Read Strobe	Buffered read strobe from tape read bus.
28-36	RDSO-7,P	Read Data Stored 0-7,P	Tape Read data storage register.
22	RDSS	Read Data Strobe Synchronized	Read data strobe synchronized with "CLK."
7	RDST	Read Strobe	Raw read strobe from tape read bus.
7	RDY	Ready	Buffered ready status from tape control bus. Indicates tape is online and ready for operation.
6	READ	Read Mode	Indicates command register function is read one record.
24	RJCT	Reject	Status to processor indicating an illegal operation was attempted.
12	RMS	Reset Main Sequencer	Initializes main sequencer to state "0."
28-36	RO-7,P	Read 0-7,P	Raw read data from tape read bus.
20	RPE	Read Parity Error	Output of read parity detector "0" good parity "1" bad parity.
3	RQCL	Request Clock	Processor clock for implementing data channel and interrupt priority.
3	RQENB	Request Enable	Raw priority clock from processor I/O bus.
6	RSL	Synchronous Reverse Line	Tape control bus line implementing reverse tape motion.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
8	RSS	Read Strobe Synchronized	NRZ read strobe synchronized with "CLK." (NRZ only.)
3	RSST	Reset Start	Initializing control for a clear, reset, or start command.
2	RST	Reset	Buffered "IORST" line from processor I/O bus that initializes controller.
2	RSTG	Reset Gated	Reset or clear command.
11	RVRS	Reverse Stored	Stored after start of operation. Used as comparison for determining if previous operation had tape motion in same direction as new operation.
6	RWD	Rewind	Function decode of command register rewinding selected tape unit if executed.
6	RWDC	Rewind Command	Command on tape control bus initiating are wind on selected unit.
7	RWDG	Rewinding	Buffered status from tape control bus indicating selected tape unit is rewinding.
7	RWG	Rewinding	Raw rewinding status of tape control bus.
9	SCY	Speed Clock Carry	Carry from divider generating speed proportional clock.
12	SDLY	Start Delay	Indicates that the main state counter is in one of the states generating start delay. (States 4, 5, 6, or 7.)
2	SELB	Sense Line Busy	Processor skip test for busy condition.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
6	SELO-7	Select 0-7	Decoded select control from command register.
7	SEND	SEND	Status to processor indicating that controller is in a start or post delay.
6	SFR	Space Forward	Decode of command register function implementing a space forward x records.
14	SHIFT	SHIFT	Controls shifting of computer data register ("CDR") for packing and unpacking of data.
11	SLS1,2,4	Select Stored Bits 1,2,4	Command register select code stored after start of operation used to check if new operation is on same unit as old operation.
6	SLO-7	Select 0-7	Tape unit select bus to tape transports.
12	SMTN	Start Motion	Initiates start of a new tape motion command except rewind.
6	SPACE	Space Command	Decode of command function indicating that function is a space forward or reverse command.
27	SPCC	Start Post Count Control	When end-of-record is detected this control starts post delay if function is completed, otherwise it sets up the reading of the next record.
6	SPMN	Stop Motion	Stops tape motion and sets done at end of post delay.
6	SRV	Space Reverse	Space reverse decode of command register function.
10	SSC	Select Second Constant	Selects alternate from constant for delay counter.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
9	SS1-8	Speed Select 1-8	Speed clock divider control.
11	STAR	START	Start command from processor I/O bus synchronized with "CLK"). It is held true until actual start of operation.
2	START	START	Raw processor I/O start control.
2	STRT	START	Buffered start from processor I/O control.
11	STSQ	Start Synchronizer	Implements synchronizing of start control.
2	STW	Sixty Two	Selects alternate processor device code of 62.
7	S556	Select 556	Switch clock to alt crystal when 556 bpi density is selected and main sequencer is in state 8 or above.
21	TMR	Timing Error	Status to processor indicating that data channel did not service a request in time to prevent overflow of buffer.
16	TMRS	Timing Error Set	Direct sets "TMR."
6	TMTN	Tape Motion	Controls tape motion forward and reverse (except rewind).
7	TPRDY	Tape Ready	Status to processor indicating that tape is ready for motion command.
22	TRCL	Track Ready Clock	Switches the VCO reference from the crystal to the reference read track.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
16	TRD	Test Read	Forces the CRC and LRC characters into the "CDR" after record is read.
7	TRDY	Tape Ready	Raw ready line from tape control bus.
23	VCOC	Voltage Controlled Osc. Clock	Clock for read decoder derived from VCO.
22	VCOG	Voltage Controlled Osc. Gated	"VCOC" when operating in Phase Encoded mode. "RDS" when operating in NRZ mode.
9	VCOR	Voltage Controlled Osc. Reference	Divided clock from crystal Osc. used as reference for VCO when not tracking read data.
9	VCRD	Voltage Controlled Osc. Reference Divided	VCOR÷2. Used for generating ID burst at beginning of Phase Encoded tape.
22	VTR	VCO Reference Track	Selects track 2 or 6 for VCO reference depending on which track is active.
22	VTRS	VCD Reference Track Switch	Changes reference track selection if selected reference track goes dead.
19	WARS	Write Amplifier Reset	Tape write bus control that resets tape write amplifier.
18	WCEN	Write Clock Enable	Enables counter that generate tape write clock.
19	WCLK	Write Clock	Used to load the write register.
5	WCY	Word Count Carry	Indicates when word count register is incremented to zero terminating a write or read operation.
13	WCZ	Word Count Zero	Indicates completion of a write or read data transfer or space operation.

TERM LIST (Continued)

RIGIN	NMONIC	TERM	COMMENTS
8	WDC	Write Data Clock	Clock to tape transport write register.
	WDO-7,P	Write Data 0-7,P	Tape write data bus.
9	WDS	Write Data Strobe	Tape write bus clock.
	WEFG	Write End-of-File Gated	Phase Encoded write end-of-file.
9	WEN	Write Enable	Generates "WDS" and "WXFR" in write mode. Determines write clock rate.
6	WEOF	Write End-of-File	Decode of command register function to write a file mark.
6	WNB	Write Enable	Write control bus to tape transport.
28-36	WNDO-7,P	Window 0-7,P	Used in Phase Encoded read to mask out the phase transition from bit transitions.
8	WRITE	Write Mode	Decode of command register function instructing controller to write one record.
9	WRS	Write Reset	Controls reset of tape write amplifiers.
6	WRT	Write Modes	Any of the three write function WRT = Write + WEOF + Gap.
	WRTG	Write Gated	Controls write data multiplexer.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
18	WSTR	Write Start	Resets Phase Encoded clock counter into proper phase at start of write operation.
13	WS8	Write Sequence 8	Most significant bit of write/read sequencer counter.
15	WS8G	Write Sequence 8 Gated	Used to generate all Zeros characters.
21	WTPR	Write Parity	Output of write parity generator.
19	WXFR	Write Transfer	Updates FIFO output to next character in a write operation.
13	WZG	Write Zero Generator	Forces write multiplexer to zero output.
13	WO-15	Write/Read Sequence 0-15	Decoded write/read sequencer state.
13	W3 + W6	Write/Read Sequence 3 or 6	Completion of the packing or unpacking of a computer word.
9	XDSA	Crystal Select A	Selects Crystal "A" for "XTAL" used except when writing or reading a 556 bpi in 7 track operation.
9	XDSB	Crystal Select B	Selects Crystal "B" for "XTAL" used for writing or reading 556 bpi 7 track only.
16	XFOK	Transfer OK	FIFO and "CDR" ready for transfer of data between them.
9	XTA	Crystal "A"	Normal source of clock.

TERM LIST (Continued)

ORIGIN	NMONIC	TERM	COMMENTS
9	XTAL	Crystal Clock	Basic system clock.
9	XTB	Crystal "B"	Clock source for writing or reading 556 bpi 7 track.
13	ZGC	Zero Generator Carry	Terminates generating of preamble and postamble Zeros and CRC and LRC gaps.
26	ZRAL	Zero All	Indicates that read character is all Zero's.
7	556 BPI	556 Bits per Inch	Indicates tape density select is 556 bpi.
7	556	556	Determines speed select if tape 9 track determines whether 7 track tape densities are 200 bpi/556 bpi or 556 bpi/800 bpi.
7	556D	556 Density	Raw "556" line from tape control bus.
7	7 Track	7 Track	Raw bus signal from tape transport indicating selected drive is a 7 track unit.
7	7 TRH	7 Track High Density	Decode indicating selected tape unit is a 7 track unit in High Density.
7	7 TRL	7 Track Low	Decode indicating selected unit is a 7 track unit in Low Density.
15	7 TRZ	7 Track Zero	Generates 7 track file mark character when writing file mark, otherwise it is at zero to generate all Zero's character.
7	800 BPI	800 Bits Per Inch	Decoded indicated that unit is NRZ and 800 bpi density.
7	9 TRK	9 Track	Indicates selected tape unit is a 9 track unit configured for NRZ.

RIGIN	NMONIC	TERM	COMMENTS
15	9 TRZ	9 Track Zero	Generates 9 track file mark character when writing file character, otherwise it is at Zero to generate all Zero's character.

UNPACKING AND RECEIVING INSPECTION

Before signing for your shipment which has arrived, use the delivery receipt to check off each package, accounting for all packages listed. Inspect the shipping containers immediately for evidence of mishandling during transit and note the damage on all copies of the delivery receipt before signing it. If a container is damaged, request that the carrier's agent be present when the package is opened.

Compare the packing list attached to the shipping container against your purchase order to verify that the shipment is correct. Notify the department issuing the requisition and the Purchasing department that the shipment has arrived.

Unpack the shipping containers and inspect each item for external or concealed damage such as broken controls and connectors, dented corners, bent panels, scratches, loose or damaged components, damaged subassemblies, etc. If any damage is found while unpacking, notify your supplier and the delivering carrier immediately and request inspection.

Retain the shipping container and packing material for examination in the settlement of claims or for future use. Be sure all minor parts and small items are found before discarding any shipping material.

NOTES

INSTALLATION CHECKLIST - CIPHER 100X

1. Open carton.
2. Turn over and lift off carton.
3. Remove corner pads.
4. Open inner carton.
5. Turn over and lift off carton from drive.
6. Locate manual and mounting hardware.
7. Inspect the drive - Contact the carrier if any concealed shipping damage is discovered.
8. On some cabinets, a mounting frame is required to mount the drive because the door swings against the edge of the cabinet. Mount the extender frame at the appropriate location in the cabinet. Be sure the hinge holes are on the correct side.
9. Refer to the tape drive manual.
10. Mount the tape drive hinges at an appropriate location on the cabinet. Place the longer hinge at the top. Place nylon washers on hinge pins.
11. Place drive on its back and remove screw from shipping frame.
12. Mount drive on hinges and secure with hinge safety block. Secure drive latch.

NOTES

WARRANTY

WESTERN PERIPHERALS warrants articles of equipment manufactured by it to be free from defects in material and workmanship under normal use and service, its obligation under this warranty being limited to making good at its factory any article of equipment which shall within one year after delivery of such article of equipment to the original purchaser be returned intact to it, or to one of its authorized service stations, with transportation charges prepaid, and which its examination shall disclose to its satisfaction to have been thus defective; this warranty being expressly in lieu of all other warranties expressed or implied and of all other obligations or liabilities on its part, and WESTERN PERIPHERALS neither assumes not authorizes any other persons to assume for it any other liability in connection with the sale of its products.

This warranty shall not apply to any article of equipment which shall have been repaired or altered outside the WESTERN PERIPHERALS factory or authorized service stations, nor which has been subject to misuse, negligence or accident, incorrect wiring by others, or installation or use not in accord with instructions furnished by the manufacturer.