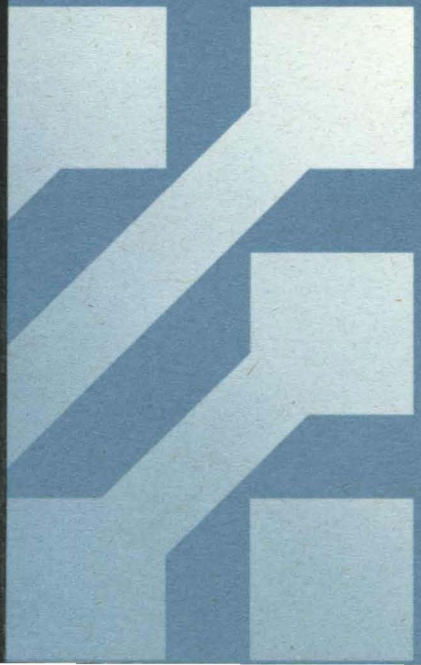
TECHNICAL REFERENCE MANUAL

# *Caviar WDAC140/AC280*

*40 and 80 Megabyte*

*3.5-inch drive*



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***Radio Frequency Interference Statement***

This Western Digital product has been verified to comply with the limits for a Class B computing device pursuant to Part 15, subpart B, of FCC rules. This does not guarantee that interference will not occur in individual installations.

Western Digital is not responsible for any television, radio, or other interference caused by unauthorized modifications of this product.

If interference problems do occur, please consult the system equipment owner's manual for suggestions. Some of these suggestions include the relocation of the computer system away from the television or radio, or placing the computer AC power connection on a different circuit or outlet.

This digital apparatus does not exceed the Class B limits for radio noise for digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

# 1.0 DESCRIPTION AND FEATURES

## 1.1 General Description

The Caviar series of Western Digital intelligent drives provides 42/85 megabytes of storage in a 3.5-inch form factor and low profile 1-inch height. Designed for use in AT-compatible systems, Caviar is the premier storage solution that achieves unsurpassed reliability and optimum performance.

Caviar features CacheFlow, Western Digital's exclusive multi-segmented adaptive disk caching system, which dynamically partitions the 8-Kbyte (32-Kbyte optional) buffer and adapts during disk operations to the optimum caching mode to dramatically enhance read/write performance. To meet the demands of high performance 80386, 80386SX, and 80486 systems, Caviar has an average seek time of less than 17 milliseconds. When coupled with Western Digital's 7600 core logic chipset, Caviar achieves higher data transfer rates with zero wait states, which means even faster system performance.

Caviar drives are preformatted (low-level), and defects are mapped out before shipment, ensuring defect-free media. Additional Caviar features include linear logical/physical address translation, automatic head parking, embedded servo control data on each track, and 56-bit error correction code.

Western Digital offers reliable, cost-effective storage solutions by integrating design and manufacturing in a process known as "interarchitecture." Critical functions, including storage, intelligent drive control, core logic, video, and communication functions, are integrated into a variety of platform-specific solutions. Designers in each arena work closely with each other, developing solutions with a first-hand knowledge of all the components that interact in the platform. This interaction between component designers means Western Digital can guarantee compatibility and build in exclusive functionality.

## 1.2 Advanced Product Features

### *CacheFlow*

Designed exclusively by Western Digital to minimize disk-seeking operations and rotational latency delays, CacheFlow is the industry's first adaptive, multi-segmented disk caching system. CacheFlow constantly evaluates not only the size of the data request but the type of data request, that is, whether the application is sequential, random, or repetitive. CacheFlow then dynamically partitions the Caviar's 8-Kbyte (32-Kbyte optional) RAM buffer into equal-sized segments and selects the appropriate caching mode for optimum system performance.

### *Automatic Head Parking*

Head parking is automatic with the Caviar series of intelligent drives. On power-down, the heads retract to a safe, non-data landing zone and lock into position, improving data integrity and resistance to shock.

### *Advanced Defect Management*

The Caviar is preformatted (low level) at the factory and comes equipped with a full complement of defect management characteristics. Extensively tested during the manufacturing process, media defects found during intelligent burn in are mapped out with Western Digital's high performance defect management technique. No modifications are required before installation.

### *Embedded Sector Servo Control*

The Caviar records servo data on every sector for precise head positioning by the servo.

### *Dual Drive Operation*

The Caviar supports dual drive operation by means of a "daisy chain" cable assembly and configuration options for master or slave drive designation.

### *Intelligent Drive*

The Caviar does not require a slot-mounted controller card. The hard disk has the controller circuitry and 40-pin ATA IDE connector attached directly to the drive.

### *Translation*

The Caviar provides a linear disk address translator to convert logical sector addresses to physical sector addresses which means Caviar guarantees compatibility to any drive set-up parameter.

### *Error Recovery*

Caviar uses a 56-bit Error Correction Code (ECC) for automatic detection and correction of errors in the data field.

### *Guaranteed Compatibility*

Western Digital performs extensive testing in its Functional Integrity Testing Labs (FIT Lab ) to ensure compatibility with all AT-compatible computers and standard operating systems.

# 2.0 SPECIFICATIONS

## 2.1 Performance Specifications

| | |
|---|---|
| Average Seek * | Sub-17 Milliseconds |
| Track-to-Track Seek | 6 Milliseconds |
| Maximum Seek | 28 Milliseconds |
| Index Pulse Period | 16.67 Milliseconds (0.1%) |
| Average Latency | 8.34 Milliseconds (0.1%) |
| Rotational Speed | 3595 Revolutions/min. (0.1%) |
| Controller Overhead | 0.3 Milliseconds average |
| Data Transfer Rate Buffer to Disk | 1.2 MBytes/sec |
| Data Transfer Rate Buffer to Host** | 4.5 MBytes/second |
| Interleave | 1:1 |
| Buffer Size | 8-Kbyte (32-Kbyte optional) Static RAM |
| Error Rate Soft | <1 in $10^{10}$ bits read |
| Error Rate Hard | <1 in $10^{12}$ bits read |
| Spindle Start Time | 5 seconds typical<br>15 seconds maximum |
| Spindle Stop Time | 6 seconds |
| Start/Stop Cycles | 10,000 cycles minimum |
| Acoustics*** | |
| Idle Mode | 40 dBA at 1 meter |
| Seek Mode | 42 dBA at 1 meter |

* "Average Seek " is determined by dividing the total time required to seek between all possible ordered pairs of track addresses by the total number of these ordered pairs.

** "Data Transfer Rate from the Buffer to the Host" is based on the sustained transfer of buffered data in MBytes per second.

*** The maximum difference between adjacent octave bands is 12 db (no pure tones).

## 2.2 Physical Specifications

| **Physical Specifications** | **Caviar AC280** | **Caviar AC140** |
|---|---|---|
| Recommended Setup Parameters* | 980 x 10 x 17 (CYL x heads x SPT) | 980 x 5 x 17 (CYL x heads x SPT) |
| Formatted Capacity | 85.3 MBytes | 42.7 MBytes |
| Interface | 40-pin PC/AT | 40-pin PC/AT |
| Actuator Type | Rotary Voice Coil | Rotary Voice Coil |
| Number of Disks | 2 | 1 |
| Data Surfaces | 4 | 2 |
| Number of Heads | 4 | 2 |
| Number of Cylinders | 1082 | 1082 |
| Average Track Density | 1,405 TPI | 1,405 TPI |
| Formatted Cylinder Capacity | 78,848 bytes | 39,424 bytes |
| Bytes per Sector | 512 | 512 |
| User Sectors per Drive | 166,628 | 83,314 |
| User Sectors per Cylinder | (4 x 39) - 2 = 154 | (2 x 39) - 1 = 77 |
| Physical Sectors per Track | 39 | 39 |
| Servo Type | Embedded Sector Servo | Embedded Sector Servo |
| Recording Method | 2,7 RLL | 2,7 RLL |
| Recording Density | 31,591 BPI | 31,591 BPI |
| Flux Density | 21,061 FCI | 21,061 FCI |
| Ecc | 56 bit | 56 bit |
| Head Park** | Automatic Head Parking | Automatic Head Parking |

* Do not exceed the maximum sector capacity (83,314 sectors for Caviar AC140, 166,628 sectors for Caviar AC280) when specifying the number of cylinders, heads, and sectors per track. Exceeding the specified limits results in the drive parking, spinning down and the disk controller returning the ID NOT FOUND error to the host.

** Seeking to a cylinder greater than or equal to cylinder 981 (translation mode: 980 cylinders X 10 heads X 17 sectors/track for the Caviar AC280, or 980 cylinders x 5 heads x 17 sectors per track for the Caviar AC140) parks the read/write heads and spins down the drive. Turning the system power off causes the Caviar to perform an automatic head park operation.

### 2.2.1 Physical Dimensions

| | |
|---|---|
| Height | 1.00 (±0.02) Inches (2.54 ±0.05 cm) |
| Length | 5.75 (±0.02) Inches (14.60 ±0.05 cm) |
| Width | 4.00 (±0.02) Inches (10.16 ±0.05 cm) |

### 2.2.2 Weight

| | |
|---|---|
| Weight | 1.12 Pounds ( 508 grams) |

### 2.2.3 Mechanical Specifications

Figure 2-1 shows the mounting dimensions and locations of the screw holes for the Caviar intelligent drive.

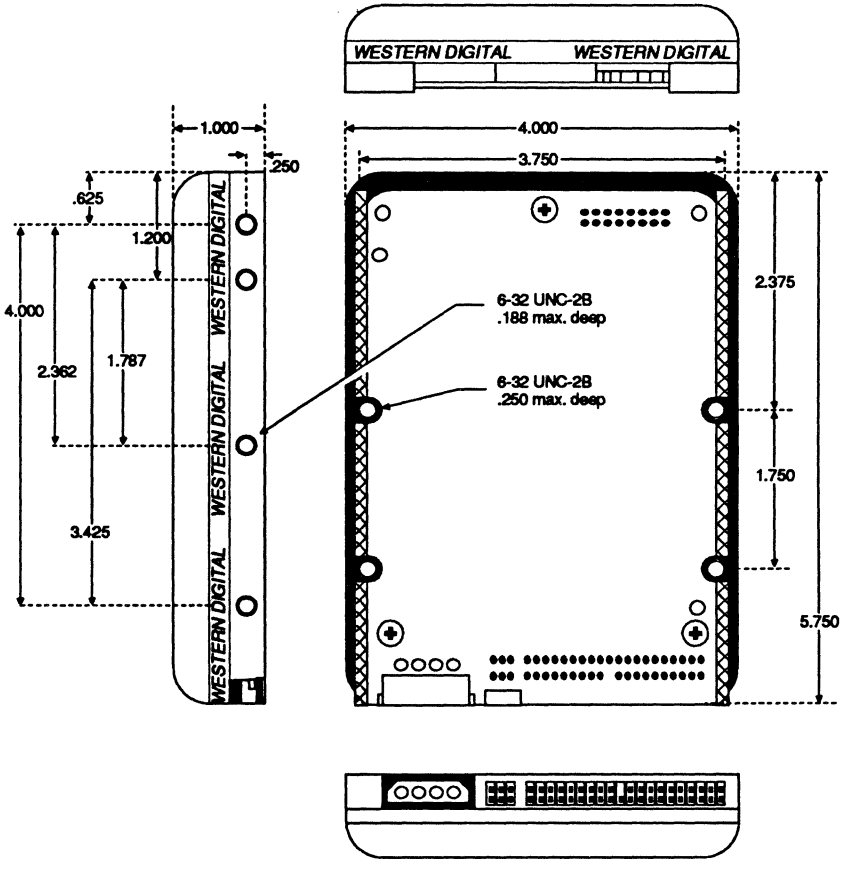



*Figure 2-1. Caviar AC140/AC280 Mounting Dimensions*

## 2.3 Electrical Specifications

### 2.3.1 12 VDC and 5 VDC Typical Current

| Operation | Input Voltage | | Power |
|---|---|---|---|
| | 12 VDC (±5%) | 5 VDC (±5%) | |
| Read | 0.350 A | 0.220 A | 5.30 W |
| Write | 0.350 A | 0.220 A | 5.30 W |
| Random Seek | 0.375 A | 0.220 A | 5.60 W |
| Spin up* | 1.20 A | 0.200 A | 15.40 W |
| | 1.40 A max | 0.25 A max | |

**Note: Spin-up mode begins at zero RPM spindle speed and ends with normal spindle speed. A complete spin-up operation typically requires five seconds. Maximum spin-up power is dissipated during the first two seconds of spin up. Refer to Figure 2-2*

### 2.3.2 Ripple

| Ripple | Maximum | Frequency |
|---|---|---|
| 12 VDC | 200 mV (peak-to-peak) | 0 - 20 MHz |
| 5 VDC | 100 mV (peak-to-peak) | 0 - 20 MHz |

### 2.3.3 Power Connectors and Cables

| | |
|---|---|
| Power Connector | 4-Pin MOLEX (P/N 15-24-4041 or equivalent) |
| Mating Connector | Body (AMP 1-480424-0 or equivalent)<br>Pins (AMP 60619-4 or equivalent) |
| Power Cable Wire Gauge | 18 AWG |

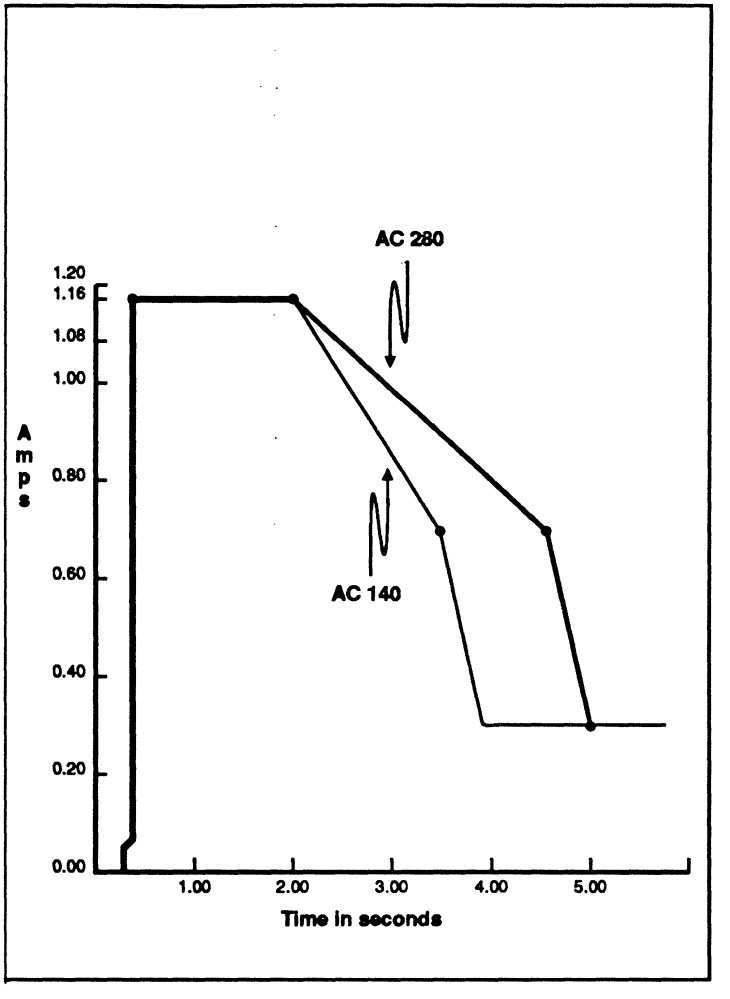



*Figure 2-2. +12V Current Draw During Spin Up (Master Mode)*

### 2.3.4 Grounding

The mounting screws connect the head disk assembly and the printed circuit board to the system chassis ground. Therefore, no external grounding strap is required.

## 2.4 Environmental Specifications

*Note: Non-operating limits indicate where device damage can occur. Operation at these limits is not intended and should be limited to the conditions specified in the operating characteristics.*

### 2.4.1 Shock and Vibration

| **Shock** | |
|---|---|
| Operating | 10Gs |
| Non-operating | 75Gs |
| *Note: Half-sine wave of 11 msec duration, two half-sine waves per second maximum, with no non-recoverable errors.* | |
| **Vibration** | |
| Operating | 5-17 Hz, 0.034" (double amplitude)<br>17-400 Hz, 0.75G (Peak) |
| Non-Operating | 5-20 Hz, 0.195" (double amplitude)<br>20-500 Hz, 4G (Peak) |
| Sweep Rate | One-half octave/minute |

### 2.4.2 Temperature and Humidity

| **Temperature** | |
|---|---|
| Operating | 5° C to 50° C |
| | 10° C/hour Thermal Gradient |
| Non-Operating | -40° C to 60° C |
| | 20° C/hour Thermal Gradient |
| *Note: The system environment must allow sufficient air flow to maintain the casting temperature at or below 55° C* | |
| **Relative Humidity** | |
| Operating | 8% to 80% RH non-condensing |
| Maximum Wet Bulb | 26° C |
| Non-operating | 5% to 95% RH non-condensing |
| Maximum Wet Bulb | 26° C |

### 2.4.3 Atmospheric Pressure

| | |
|---|---|
| Altitude - Operating | -1000 to 10,000 feet |
| Altitude - Non-Operating | -1000 to 40,000 feet |

## 2.5 Agency Approvals

The Caviar meets the standards of the following regulatory agencies:

Underwriters Laboratories
UL-Standard 1950, Standard for Safety, Information Processing and Business Equipment; File Number - E101559

Federal Communication Commission
Verified to comply with FCC Rules for Radiated and Conducted Emission, Part 15, Subpart B, for Class B Equipment

Canadian Standards Association
CSA-Standard C22.2, No. 950 - M89 Information Processing and Business Equipment; File Number LR 68850

TUV Essen Laboratories
IEC 950 (EN 60 950) Safety of Information Technology Equipment Including Electrical Business Equipment

## 2.6 Reliability Specification

| | |
|---|---|
| MTBF | 100,000 Power-on hours |
| MTTR | 10 Minutes typical |
| Component Design Life | 5 Years |
| Warranty Period | Two Year |

## 2.7 Compatibility Per Functional Integrity Testing

The FIT Lab™ or Functional Integrity Testing Lab ensures that the Caviar has guaranteed compatibility. Before any drive is released to the factory, it must complete a two-phase FIT process. The FIT process results in a matrix compatibility test which includes:

- Host systems
- Other intelligent drives
- Operating systems (e.g., DOS, Novell, Xenix, Unix, OS/2)
- Application programs (e.g., word processing, data base management, spreadsheets, desktop publishing, CAD and graphics in single and multi-user environments)
- Benchmarks (e.g., third party benchmarks such as Core Test and P.C. Bench)

In the first phase of FIT the Caviar is run through the following tests:

- Mechanical mounting
- EMI susceptibility
- BIOS compatibility with third party and Western Digital hardware

In addition to these tests, there are five types of tests that are run in both Phase I and Phase II:

- Alpha tests (Western Digital Proprietary compatibility test suite)
- Benchmark tests
- Peripheral compatibility tests
- Host compatibility tests
- Operating system compatibility tests

The selection of host systems is based upon market representation and systems that have previously presented unique compatibility problems. Examples of host systems used in FIT include:

- Extremely fast units with very short timing windows
- Specific OEM systems that utilize unique operating systems
- Additional host systems supplied by OEMs requesting FIT

The five types of tests that are run in both Phase I and Phase II are described below:

### *Alpha Tests*

The Alpha Tests exercise all of the read, write and seek functions of the firmware in both the physical and translation modes.

### *Benchmark Tests*

The benchmark tests are listed in the following table:

Bench Test
Bench 23
Bench 26
Core Test
Masm Test
ASM51 Test
dBase Test
MS "C" Compiler Test
File copy and compare test
Wordstar Word search test
Wordstar Spelling test
Wordstar loading and saving test
Lotus Test
Testdisk

### *Peripheral Compatibility Tests*

The peripheral compatibility tests verify the drive's operation with other intelligent disk drives, i.e., dual-drive compatibility.

### *Host Compatibility Tests*

The host compatibility tests verify the disk's operation with a variety of host computers. The tests include formatting, diagnostics, benchmark testing and file copy and compare.

### *Operating System Compatibility Tests*

The operating system compatibility tests verify the drive's operation in various operating systems including DOS, Novell, Xenix, Unix and OS/2.

# 3.0 PRINCIPLES OF OPERATION

This section describes the principles of operation of the Caviar from the following viewpoints:

- Drive electronics
- Head disk assembly (HDA)

## 3.1 Block Diagram

A block diagram of the Caviar is provided in Figure 3-1.

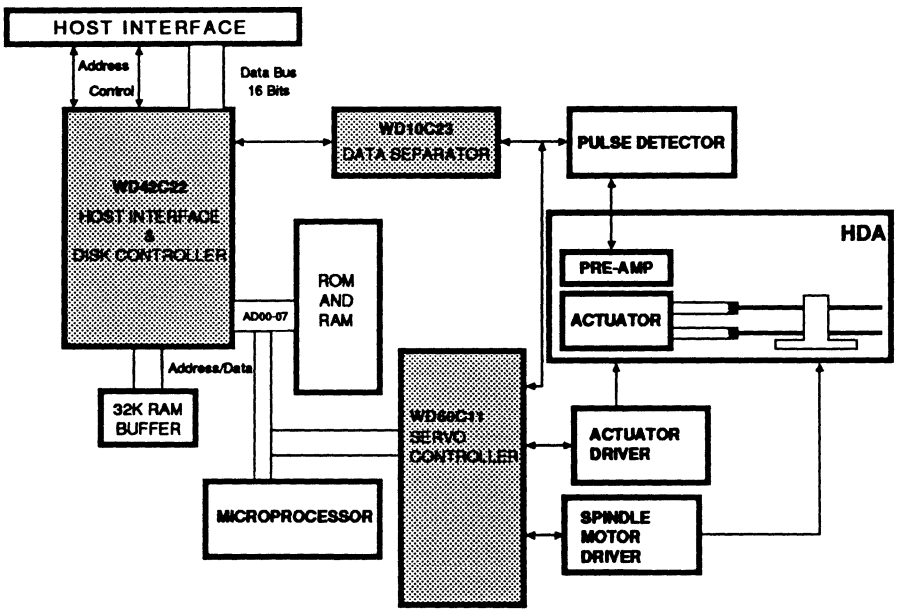



*Figure 3-1. Block Diagram*

## 3.2 Drive Electronics

Caviar's intelligence resides in the specialized electronic components mounted on the four-layer printed circuit board assembly. These devices perform the intricate operations described in section 4. The Caviar consists of the following drive electronic components:

- WD42C22 Winchester Disk Controller
- Buffer RAM
- WD60C11 Servo Controller
- WD10C23 Data Separator
- Microprocessor ROM and RAM
- Pulse Detector
- Spindle Motor Driver
- Actuator Driver

### 3.2.1 WD42C22 Winchester Disk Controller

TheWD42C22 integrates a high performance, low cost Winchester formatter/controller, CRC/ECC generator/checker, host interface, and buffer manager into a single, 84-pin PQFP device. The controller/formatter encodes and decodes data to and from the WD10C23 data separator. The CRC/ECC generator/checker calculates ECC for the data field. The host interface directly connects to the host system bus via internal 12 mA drivers. The buffer manager controls the buffer RAM and handles the arbitration between the host interface and drive controller.

### 3.2.2 Buffer RAM

A 8-Kbyte (32-Kbyte optional) static RAM buffer enhances data throughput by buffering sector data between the Caviar and the AT system bus. The RAM only buffers read/write data and ECC information. The buffer is accessed by two channels, each having a separate 15-bit address and byte-count register. The channels operate simultaneously, accepting read and write operations from two data paths. The address access time for the buffer RAM is 120 ns (maximum).

### 3.2.3 WD60C11 Servo Controller

The WD60C11 provides servo discrimination, track address capture, and measures servo burst amplitudes. A servo burst is a momentary servo pattern used in embedded servo control implementations, usually positioned between sectors. The WD60C11 also provides spindle motor control.

### 3.2.4 WD10C23 Data Separator

The WD10C23 handles the sensitive read/write signals between the WD42C22 and the read channel circuitry at a rate of 12 megabits-per-second. Read data refers to previously written data, with phase, frequency, and write splice noise. The WD10C23 removes the noise and sends clean digital read signals to the WD42C22. The WD10C23 conditions write data to be recorded on the drive. Data to and from the WD42C22 is precisely clocked to the WD10C23.

### 3.2.5 Microprocessor ROM and RAM

A 16-bit microprocessor controls and coordinates the activity of the HDA and the WD42C22. The microprocessor receives and sends command or status information over an internal multiplexed address/data bus. The microprocessor monitors spindle and actuator activity until the WD42C22 asserts the microprocessor's interrupt line. The WD42C22 asserts the interrupt when the host writes to the Command Register or at the end of either a host or disk transfer. The microprocessor uses 8 Kbytes (32 Kbytes optional) of external ROM and 2 Kbytes of external static RAM. Firmware controlling all these functions, including the adaptive multi-segmented cache, resides in the microprocessor's external 32-Kbyte ROM.

### 3.2.6 Pulse Detector

The pulse detector amplifies and qualifies the RLL-encoded signals from the preamplifier on the flex circuit. Pulse qualification in read mode is accomplished using level qualifications of differentiated input zero crossings. An AGC amplifier compensates for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry.

In write mode, the circuitry is disabled. The AGC gain stage input impedance switches to a lower level to allow fast settling of the input coupling capacitors during a write-to-read transition.

### 3.2.7 Spindle Motor Driver

The three-phase spindle motor driver can supply up to 1.4A to the spindle motor. The driver is controlled by the WD60C11 Servo Controller.

### 3.2.8 Actuator Driver

The actuator driver provides precision placement of the read/write heads by means of the voice coil motor. A digital-to-analog converter in the WD60C11 controls this H-bridge driver, which uses +12V, +5V and ground.

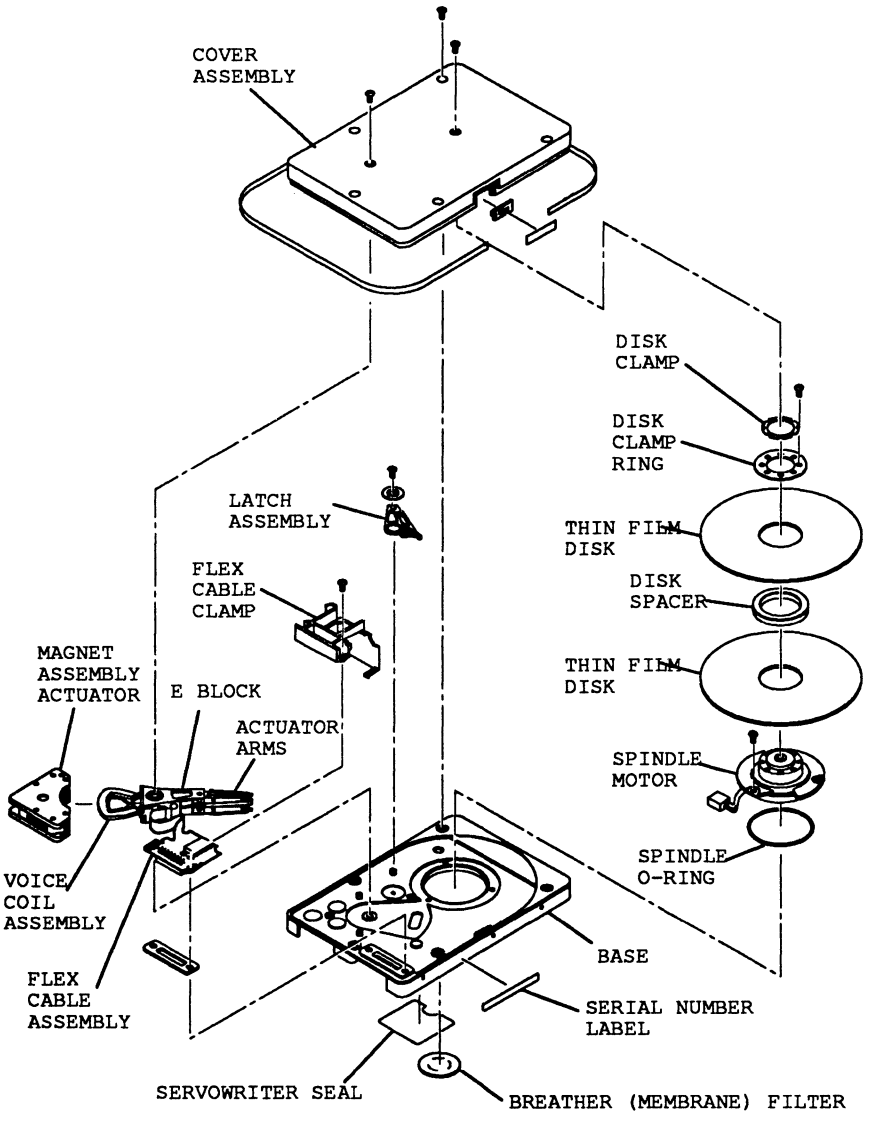



*Figure 3-2. Mechanical Exploded View*

## 3.3 Head Disk Assembly (HDA)

The functional parts of the HDA are mounted to a common die-cast housing with a sealed cover. The assembly provides exact mechanical relationships between the spindle, headstack, and voice coil through precise machined dimensions on the housing. A clean environment is also maintained within the HDA enclosure.

The HDA consists of the following mechanical subassemblies:

- Base/Cover Assembly
- Spindle Motor
- Disk Stack Assembly
- Headstack Assembly
- Voice Coil Assembly
- Air Filtration System

### 3.3.1 Base/Cover Assembly

The single-piece cast base provides a mounting platform for the components of the assembly. The base/cover assembly has machined mounting surfaces for the spindle motor, voice coil, and pivot. To ensure a Class 100 environment within the HDA, a tape seal is wrapped around the base and cover castings.

### 3.3.2 Spindle Motor

The spindle motor assembly consists of a brushless three-phase motor, spindle bearing assembly, disk mounting hub, and a ferrofluid magnetic seal. The entire spindle motor assembly is completely enclosed in the HDA and bolted to the base casting. The motor rotates the spindle shaft at 3595 RPM.

Proprietary spindle electronics sense motor speed and angular position by monitoring the spindle motor's back electromotive force (BEMF). Using BEMF sensing, instead of the conventional Hall effect or inductive motor position sensors, lowers the power consumption and increases reliability. Motor driver circuits dynamically brake the spindle during motor spin down.

### 3.3.3 Disk Stack Assembly

The disk stack assembly consists of disks, disk spacers, and a disk clamp. In the Caviar AC280, two disks and one spacer are placed on the hub and clamped into place. The Caviar AC140 has one disk and a spacer.

The platters of the Caviar drives are thin inflexible aluminum disks. Each disk is plated with a layer of nickel, followed by the magnetic media coating. A thin film of carbon overcoat protects the magnetic material against wear and abrasion from the read/write heads. The final lubricant layer provides further protection between the read/write heads and media during take-offs and landings.

### 3.3.4 Headstack Assembly

The headstack assembly consists of the following mechanical subassemblies:

- Read/Write Heads
- Actuator Arm
- Flex Circuit

#### *Read/Write Heads*

The metal-in-gap (MIG) read/write heads consist of a mini-composite slider assembly mounted on a Whitney class suspension system. MIG heads have sputtered metal in the head gap. The metal in the gap allows greater sensitivity to magnetic flux reversals than normal composite heads. The mini-composite slider is a small block of ceramic material. Bonded into the outer rail of the mini-slider is the read/write head. The read/write head induces voltages in a coil mounted above the head. A linkage between the actuator block and the read/write heads, the flexure, connects the slider to the actuator arm. The Caviar actuator is statically balanced about the pivot center.

#### *Actuator Arm Assembly*

The actuator arm assembly is illustrated in Figure 3-2. This assembly is servo-controlled and derives position information from the sector servo data embedded in all disk tracks.

#### *Flex Circuit*

The head conductors are flex cables routed through the flex circuit assembly inside the HDA. The flex circuit assembly transfers signals between the read/write heads and the voice coil actuator motor. A preamplifier IC, located on the flex circuit, maximizes the read/write heads' signal strength while minimizing noise.

### 3.3.5 Voice Coil Assembly

The voice coil assembly consists of an upper and lower magnet plate, a flat rotary coil, a bidirectional crash stop, and a pivot bearing.

The pivot assembly fits in the actuator block bore.

### 3.3.6 Air Filtration System

It is absolutely essential that air circulating within the drive be particle free. The HDA is assembled in a Class 100 purified air environment, then sealed with tape. To retain this clean environment, the Caviar is equipped with two filters. One filter, the recirculating filter, cleans the air within the HDA. The recirculating filter traps any particulates which may be generated during head landings or take-offs. Mounting the recirculating filter next to the disk places the filter in the direction of the air flow. This strategic placement of the filter allows the rotating disks to act as an air pump forcing air through the recirculating filter. A second filter, the breather filter, cleans any external air entering the HDA. The breather filter also equalizes the internal and external air pressure. The breather filter is located on the bottom of the HDA.

# 4.0 ADVANCED PRODUCT FEATURES

Western Digital's Caviar series of intelligent drives provides a choice of data storage capacities for the IBM PC/AT and compatibles with a full complement of advanced product features. This section describes the following Caviar advanced product features:

- CacheFlow
- Defect Management and Format Characteristics
- Error Recovery Process
- Translation
- Dual Drive Option

## 4.1 CacheFlow

CacheFlow is the industry's first adaptive, multi-segmented disk caching system.

### 4.1.1 Purpose of CacheFlow

CacheFlow was designed by Western Digital to minimize disk seeking operations and the overhead due to rotational latency delays. CacheFlow constantly evaluates not only the size of the data request but the type of data request, that is, whether the application is sequential, random or repetitive. CacheFlow then dynamically partitions the Caviar's 8-Kbyte (32-Kbyte optional) RAM buffer into segments and selects the appropriate caching mode for optimum system performance.

### 4.1.2 Benefits of CacheFlow

In a typical application, most host requests are for sequential data. CacheFlow's adaptive design enables the Caviar to eliminate unnecessary disk seeking operations by immediately implementing the Sequential mode once the data has been analyzed. Applications such as "Core Test" or other benchmark utilities, on the other hand, request the same data over and over again. CacheFlow provides a similar performance edge by switching to the Repetitive mode of operation.

### 4.1.3 CacheFlow Operation

Sequential mode is the default mode of operation for CacheFlow. The Caviar initially partitions the 8-Kbyte (32-Kbyte optional) cache buffer into four caching segments. As seeking operations begin, CacheFlow monitors the data's sector address and sector count parameters as illustrated in Figure 4-1. CacheFlow then uses a simple hit score algorithm to either increase or decrease the segment size for optimal performance.

CacheFlow switches from Sequential mode to Repetitive mode during read operations if the same block is accessed twice. Both modes read ahead after the host-requested data has been read. By storing read-ahead data in the sector buffers, the cache hit score can be significantly improved.

CacheFlow transfers host write data immediately to the sector buffer. A write operation does not affect the buffer's cache segments since write data is not cached. Only the sectors that are rewritten are purged from the buffer.

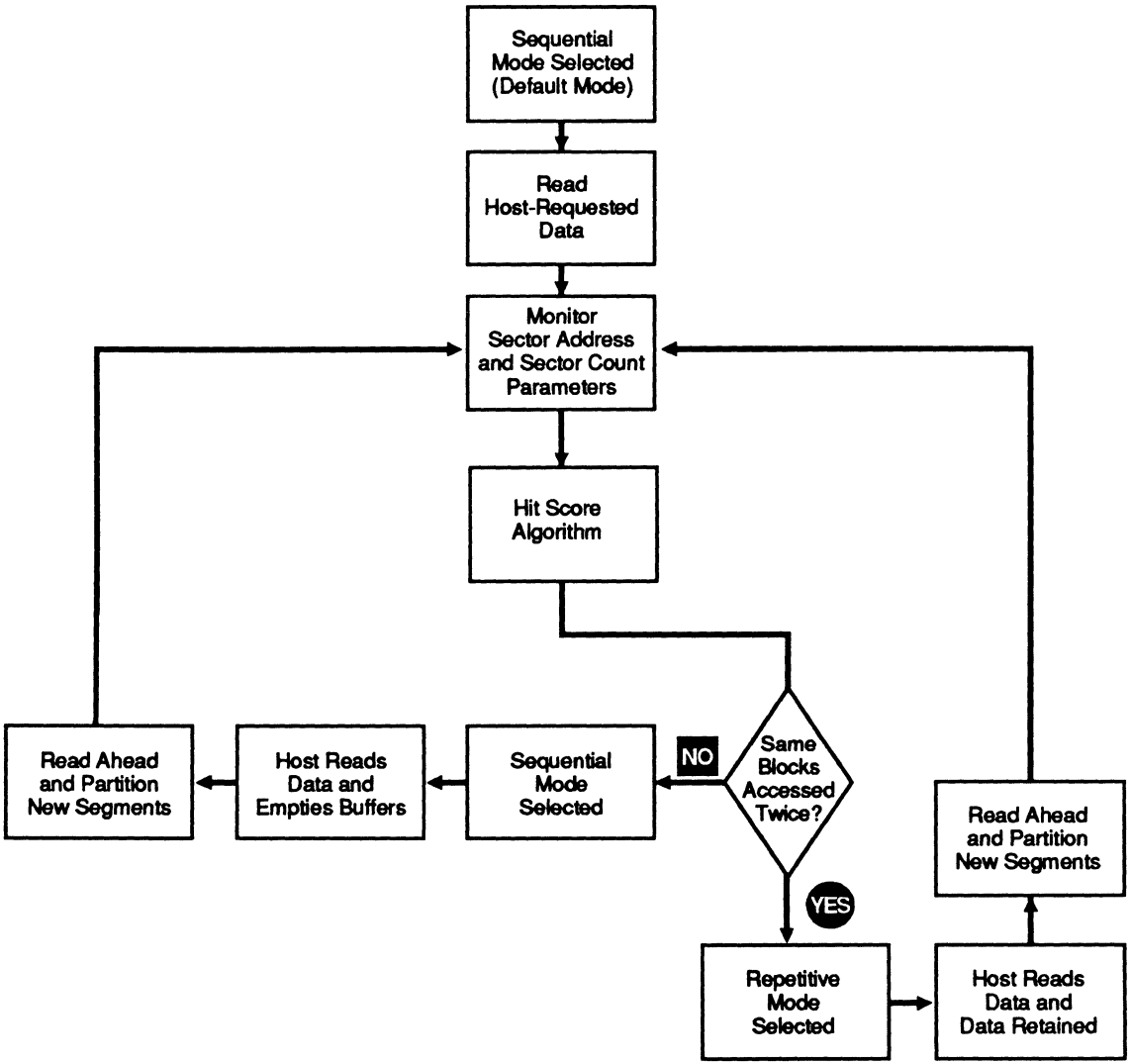



*Figure 4-1. Cache Flow Algorithm*

### 4.1.4 Sequential Mode

The sequential caching mode is the standard read-ahead cache. After reading all of the host-requested data into the segment(s), CacheFlow continues to read ahead until the cache is full. After the host reads the requested data from the cache, a new cache beginning is established following the last sector buffer returned to the host. Based on the hit score algorithm, sequential mode adapts the number of segments to optimize segment performance.

The default mode of four cache segments provides optimum cache performance. A larger number of segments may limit cache effectiveness because the segment may not store enough sequential sectors. A smaller number of segments may limit effectiveness for random reads.

### 4.1.5 Repetitive Mode

The Repetitive caching mode resembles a static buffer. If the same blocks are accessed twice, the Repetitive mode is selected. Repetitive mode also reads ahead and can override the number of segments to build one large segment with the maximum hit score. Unlike Sequential Mode, however, the sector buffers containing the host-requested data remain valid after the hosts reads the data.

## 4.2 Defect Management and Format Characteristics

### 4.2.1 Defect Management

Every Caviar undergoes factory-level intelligent burn in, which thoroughly tests for any defective sectors on the media before the drive leaves the manufacturing facility. Following the extensive tests, a primary defect list is created. The list contains the sector, cylinder, and head numbers for all defects. The purpose of the sector/track map is to manage the reallocation of spare sectors and tracks after they have been assigned.

Western Digital offers a defect management utility called WDAT_IDE, to manage any additional defects that may occur after prolonged use. Refer to section 8 for additional information.

### 4.2.2 Format Characteristics

The Caviar is shipped from the factory preformatted (low level) with all the defects mapped out. This eliminates the need for the end-user to enter defects during installation. No additional low-level formatting is required, although a high-level format must still be performed.

In order to be compatible with existing, industry standard defect management utility programs, the Caviar supports logical format. When the host issues the Format Track command, the Caviar performs a logical version of this command in response to the host's interleave table request for good and bad sector marking. (The logical format does not corrupt the defect management that has been applied to the drive.)

If the host issues the Format Track command during normal operating modes, the data fields of the specified track are filled with a data pattern of all zeroes. The interleave table identifies any bad sectors on a given track. The interleave table must contain 512 bytes of data. There are two bytes per sector for each entry in the interleave table. The first byte marks the sector as good or bad. The first byte is set to "00H" to indicate a good sector or to "80H" to indicate a bad sector. The second byte designates the logical sector ID number.

## 4.3 Error Recovery

The Caviar has two means of error recovery:

- Read/Write Retry Procedure
- Extended Read Retry Procedure

The Caviar's retry procedures are implemented for the following errors:

- ID Not Found (IDNF)
- Data Address Mark Not Found (DAMNF)
- Error Correction Code (ECC)

The host may explicitly enable/disable retries in the Read, Write and Read Verify commands. All other commands and the controller's internal disk read and write operations are always performed with retries enabled. If retries are disabled, the Caviar will not perform any disk controller retry operations and will immediately set the appropriate bit in the Error Register.

The Read/Write Retry Procedure will perform up to ten basic retry operations to succeed in reading or writing a specified sector. If recovery is achieved, the Caviar continues executing the command. For a write operation, if these retries fail to validate the ID fields on a specified track, then an IDNF error is reported to the Caviar's Error Register and the command is terminated.

For a read operation, the Caviar will perform the Extended Read Retry Procedure to recover the data. The Extended Read Retry Procedure employs up to sixteen combinations of early/late window shifts and positive/negative track offsets to recover read data. This procedure is used for the IDNF, DAMNF and ECC errors. If the retry operation is successful, the Caviar clears any existing window shift or track offset before continuing with the command. If the retry operation failed, the Caviar reports the appropriate error to the Error Register, with the exception of an ECC error. In the case of an ECC error, the drive performs up to eight retries to obtain two consecutive matching syndromes. If matching syndromes are found, and the error spans eleven bits or less, the data is corrected, the CORR bit is set in the host's status register, and the command continues. If two consecutive matching syndromes are not found, or if the error spans more than eleven bits, the Caviar reports an ECC (uncorrectable) error to the Error Register.

## 4.4 Translation

The Caviar implements linear address translation. The translation mode and translated drive configuration are selected by using the Set Drive Parameters command to issue head, and sector/track counts to the translator. The product of the cylinder, head, and sector/track counts must be equal to or less than the maximum number of sectors available to the user. The maximum number of sectors per drive for the Caviar AC140 and AC280 are 83,314 and 166,628 sectors, respectively. Each sector consists of 512 bytes.

The minimum value for any translation parameter is one. The maximum value for any translation parameter is as follows:

| | |
|---|---|
| Sectors/track | 63 |
| Heads | 16 |
| Cylinders/drive | 1024 |

The values in the Sector Count Register and the SDH Register determine the sectors per track (SPT), and heads. Regardless of the values of the SPT and the heads, Caviar will always be in the translation mode. Refer to section 2.2 for the recommended setup parameters.

## 4.5 Dual Drive Option

The Caviar supports dual drive operations by means of configuration options for master or slave drive designation. A jumper must be placed in the drive's option area for both master and slave configurations. Connection to the host is implemented by means of a daisy-chain cable assembly. These configurations are described in section 6.

The SDH Register contains the master/slave select bit for the Caviar. The $\overline{\text{DASP}}$ signal is a time-multiplexed indicator of "drive active or slave present" on the Caviar's I/O interface. At reset, this signal is an output from the slave drive, and an input to the master drive, showing that a slave drive is present. For all times other than reset and drive diagnostics, $\overline{\text{DASP}}$ is asserted at the beginning of command processing and released upon completion of the command. If the master drive option has been configured, the Caviar will not respond to commands or drive status on the interface when the slave bit is selected in the SDH Register.

# 5.0 HOST INTERFACE AND AT COMMAND SET

This section describes:

- J2 pin assignments
- Caviar registers
- Caviar commands
- Host interface read timing
- Host interface write timing
- Error reporting

## 5.1 J2 PIN ASSIGNMENTS

The Caviar interfaces with the host I/O bus via the 40-pin connector (J2) illustrated in Figure 5-1. Table 5-1 identifies the pin numbers of the J2 connector and the corresponding signal names and signal functions.

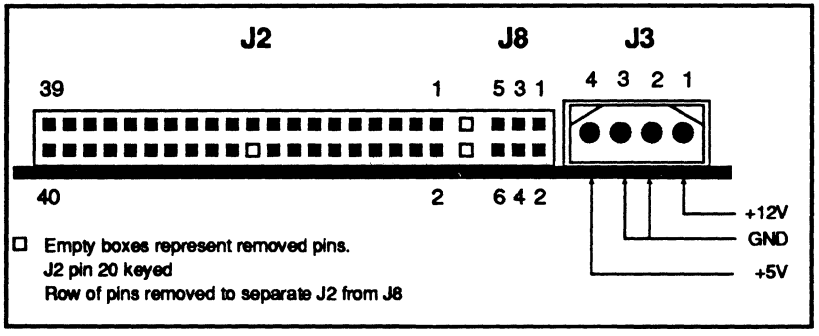



*Figure 5-1. Standard Factory Connectors*

| Pin Number | Mnemonic | Signal Name | I/O | Function |
|---|---|---|---|---|
| 1 | $\overline{RST}$ | $\overline{Reset}$ | I | Initializes the Caviar when asserted. |
| 3,5,7,9, 11,13, 15, 17 | HD7-0 | Host Data Bus Bits 7-0 | I/O | The tristate, 8-bit, bidirectional bus for transferring status and control information between the host and the Caviar. |
| 4,6,8, 10,12, 14,16,18 | HD8-15 | Host Data Bus Bits 8-15 | I | The upper data bus is used during data transfer only (16-bit data transfer). |
| 2,19,22, 24,26, 30,40 | GND | Ground | | |
| 20 | | | | Key - Not connected. |
| 21,27, 28,29 | | | | Reserved – Not connected |
| 23 | $\overline{IOW}$ | $\overline{I/O\ Write}$ | I | The host controller asserts $\overline{IOW}$ when a data or control byte is written to the Caviar. |
| 25 | $\overline{IOR}$ | $\overline{I/O\ Read}$ | I | The host controller asserts $\overline{IOR}$ when a data or status byte is read from the Caviar. |
| 31 | INTRQ | Interrupt Request | O | The Caviar asserts INTRQ to request interrupt service from the host. |
| 32 | $\overline{I/OCS16}$ | $\overline{I/O\ Channel\ Select\ 16}$ | O | Identifies data transfers to or from the host as 16 bits wide. |

*Table 5-1. J2 Pin Descriptions*

| Pin Number | Mnemonic | Signal Name | I/O | Function |
|---|---|---|---|---|
| 35,33, 36 | HA0-2 | Host Address Bus | I | A0, A1 and A2 address I/O ports 0 through 7. |
| 34 | $\overline{\text{PDIAG}}$ | $\overline{\text{Passed}}$ $\overline{\text{Diagnostics}}$ | I/O | Output from slave drive when it has passed its diagnostics. Input to master drive. |
| 37 | $\overline{\text{HCS0}}$ | $\overline{\text{Host}}$ $\overline{\text{Chip}}$ $\overline{\text{Select}}$ $\overline{0}$ | I | The host asserts $\overline{\text{CS0}}$ to address and communicate with the Caviar on the I/O channel. |
| 38 | $\overline{\text{HCS1}}$ | $\overline{\text{Host}}$ $\overline{\text{Chip}}$ $\overline{\text{Select}}$ $\overline{1}$ | I | The host asserts $\overline{\text{CS1}}$ to address and communicate with the Caviar auxilliary registers. |
| 39 | $\overline{\text{DASP}}$ | $\overline{\text{Drive}}$ $\overline{\text{Active/Slave}}$ $\overline{\text{Present}}$ | I/O | This open collector output is a time multiplexed signal indicating drive active or slave present. At reset, this signal is an output from the slave drive and an input to the master drive, showing that a slave drive is present. For all times other than reset and drive diagnostics, $\overline{\text{DASP}}$ should be asserted by the master and slave drives during command execution. |

*Table 5-1. J2 Pin Descriptions (cont.)*

| Pin Number | Mnemonic | Signal Name | Circuit Definition Code |
|---|---|---|---|
| 3-18 | D0 - D16 | Host Data Bus | Bidirectional - Circuit A |
| 35<br>33<br>36 | SA0<br>SA1<br>SA2 | Host Addr Bus<br>A0, A1 and A2 | Input - Circuit B |
| 23 | $\overline{\text{IOW}}$ | $\overline{\text{I/O Write}}$ | Input - Circuit B |
| 25 | $\overline{\text{IOR}}$ | $\overline{\text{I/O Read}}$ | Input Circuit B |
| 31 | HINTRQ | Interrupt Request | Output - Circuit A |
| 32 | $\overline{\text{IOCS16}}$ | $\overline{\text{I/O Channel Select 16}}$ | Output - Circuit A |
| 34 | PDIAG | Passed Diag | Output - Circuit A<br>Open collector |
| 37<br>38 | $\overline{\text{CS0}}$<br>$\overline{\text{CS1}}$ | $\overline{\text{Card Selects}}$ | Input - Circuit B |
| 39 | $\overline{\text{HACT}}$ | $\overline{\text{Host Active}}$ | Output - Circuit A<br>Open collector |

*Table 5-2. AT Host Electrical Characteristics*

| Symbol | Parameter | Min | Type | Max | Units | Test |
|---|---|---|---|---|---|---|
| Ioh | High Level Output Current | | | -5 | mA | 2.4 volts |
| Iol | Low Level Output Current | | | 12 | mA | 0.4 volts |
| Vih | High Level Input Voltage | 2 | | | V | |
| Vil | Low Level Input Voltage | | | 0.8 | V | |
| Voh | High Level Input Voltage | 2.4 | | | V | VCC = MIN<br>Vih = Vih min<br>Vil = Vil max |
| Vol | Low Level Input Voltage | | | 0.4 | V | VCC = MIN<br>Vih = Vih min<br>Vil = Vil max<br>Iol = 12 mA |
| Iil | Input Leakage | | | ± 10 | uA | VCC = 0 to VCC |

*Table 5-3. Data Bus SD0-16, INTRQ, and $\overline{I/OCS16}$; Circuit A*

| Symbol | Parameter | Min | Type | Max | Units | Test |
|---|---|---|---|---|---|---|
| Vt + | High Level Threshold | 1.5 | 1.7 | 2.0 | V | VCC = TYP |
| Vt – | Low Level Threshold | 0.6 | 0.9 | 1.1 | V | VCC = TYP |
| Vik | Input Clamp Voltage | | | -0.5 | V | VCC = MIN |
| | Hysteresis | 0.4 | 0.8 | 1 | V | VCC = MIN (VT + – VT-) |
| Ii | Input Current MAX Input Voltage | | | 10 | uA | VCC = MAX |
| Vol | High Level Input Voltage | | | 20 | | VCC = MIAX Vih = 2.7 V |
| Iil | Low Level Input Current | | | 20 | uA | VCC =MAX Vil = 0.4 V |

*Table 5-4. Schmitt Trigger Inputs $\overline{IOR}$, $\overline{IOW}$; Circuit B*

## 5.2 Host Interface Registers

### 5.2.1 Register Address Map

The task file occupies the address space shown in Table 5-5. The task file's ten registers pass command, status, and data information between the host and the Caviar. All registers are eight bits wide, except for the Data Register which is 16 bits wide. These registers are accessed via control lines HA0-2, $\overline{CS0}$, and $\overline{CS1}$. When the drive is busy, only the Status Register is accessible with $\overline{CS0}$ active. The Alternate Status Register is always accessible with $\overline{CS1}$ active.

| $\overline{CS0}$ | $\overline{CS1}$ | HA2 | HA1 | HA0 | Registers | |
|---|---|---|---|---|---|---|
| | | | | | **Read Function** | **Write Function** |
| 0 | 1 | 0 | 0 | 0 | Data | Data |
| 0 | 1 | 0 | 0 | 1 | Error | |
| 0 | 1 | 0 | 1 | 0 | Sector Count | Sector Count |
| 0 | 1 | 0 | 1 | 1 | Sector Number | Sector Number |
| 0 | 1 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 0 | 1 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 0 | 1 | 1 | 1 | 0 | SDH | SDH |
| 0 | 1 | 1 | 1 | 1 | Status | Command |
| 1 | 0 | 1 | 1 | 0 | Alt Status | Fixed Disk Control |
| 1 | 0 | 1 | 1 | 1 | Digital Input | |

*Table 5-5. Task File Map*

### 5.2.2 Data Register

The Data Register holds the data to be transferred to or from the host on read and write commands. All data transfers are high speed and 16 bits wide, except for the ECC bytes transferred during read long or write long commands which are 8 bits wide.

### 5.2.3 Error Register

The Error Register contains an error code that indicates a particular type of failure. Not used.

The Error Register contains an error code that indicates a particular type of failure. The register contains a valid error code only if the Status Register error bit 0 is set. The only exceptions are power-up and issuance of a diagnostic command. In these cases the Error Register contents are valid regardless of the condition of the Status Register's error bit. These two exceptions cause the following error values:

01 = No error
02 = Not applicable
03 = Buffer RAM error
04 = WD42C22 register error
05 = Microprocessor internal RAM error or ROM checksum error
8X = Slave drive failed

If a slave drive is present and has failed its diagnostic, 80H is ORed with the master drive's status bits. To read the slave's error code, the host should select the D bit in the SDH Register. In all other cases the Error Register bits are defined as follows when asserted:

| Bit Positions | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BBD | ECC | 0 | IDNF | 0 | AC | TK0 | DAMNF |

| | |
|---|---|
| BBD | Bad Block Detected |
| ECC | Error Correction Code (uncorrectable error detected) |
| IDNF | ID Not Found (target sector could not be found) |
| AC | Aborted Command |
| TK0 | Track 0 (unable to find a valid track 0) |
| DAMNF | Data Address Mark Not Found |

Error Register Bit 7 (BBD)
If bit 7 is asserted, it indicates that the Caviar detected a bad block mark in a sector ID field while attempting a read or write.

Error Register Bit 6 (ECC)
If bit 6 is asserted, it indicates that the Caviar detected an uncorrectable data error while reading a target sector.

Error Register Bit 5
Not used.

Error Register Bit 4 (IDNF)
If bit 4 is asserted, it indicates that the Caviar was unable to locate a valid ID field for the specified logical address.

Error Register Bit 3
Not used.

Error Register Bit 2 (AC)
If bit 2 is asserted, it indicates that the Caviar has terminated the current command. This is due to one of the following:

- Illegal write current condition (write fault)
- No seek complete
- Drive not ready condition
- Invalid command code

Error Register Bit 1 (TKO)
If bit 1 is asserted, it indicates that the Caviar was unable to locate a valid track 0 indication. This bit is only valid after a Recalibrate command.

Error Register Bit 0 (DAMNF)
If bit 0 is asserted, it indicates that the Caviar was unable to locate a valid Data Address Mark (DAM) within a given number of byte times after the ID field.

### 5.2.4 Write Precompensation Register

The Write Precompensation Register is ignored during normal write operations since the Caviar automatically determines the proper write precompensation. The contents of this register are only used by the Set Buffer Mode command.

### 5.2.5 Sector Count Register

The Sector Count Register indicates the number of sectors to be transferred during a read, write or verify operation. (A value of zero indicates a count of 256 sectors.) During a format operation, this register contains the number of sectors per track (SPT) and must correspond with the values indicated by the Set Drive Parameters command. When read by the host, this register indicates the number of sectors, if any, that were not read or written during the previous command. The Sector Count Register contents are used by the following commands:

Read Sector
Write Sector
Format Track
Read Verify
Set Drive Parameters
Read Multiple
Write Multiple
Set Multiple

### 5.2.6 Sector Number Register

The Sector Number Register defines the target sector for the current operation when written to by the host. The contents of this register are used by the following commands:

Read Sector
Write Sector
Read Verify
Read Multiple
Write Multiple

### 5.2.7 Cylinder Low/Cylinder High Registers

The Cylinder Low/Cylinder High Registers contain the logical cylinder addresses for commands that require an address. These registers also serve as a 16-bit command register for extended commands. Extended commands are beyond the scope of this document. The Cylinder Low Register contains the eight low-order bits of the starting cylinder number. The Cylinder High Register contains the three high-order bits of the starting cylinder number.

| Bit Position | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LSB | LSB | LSB | LSB | LSB | LSB | LSB | LSB |
| 0 | 0 | 0 | 0 | 0 | MSB | MSB | MSB |

The contents of the Cylinder Low/Cylinder High Registers are used by the following commands:

Seek
Read Sector
Write Sector
Format Track
Read Verify
Read Multiple
Write Multiple

### 5.2.8 SDH Register

The SDH Register selects the drive and head number for a particular operation. The bit assignments are as follows:

| Bit Positions | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | SS1 | SS0 | D | HS3 | HS2 | HS1 | HS0 |
| SS1 - SS0 = Sector Size (512 byte) = 01<br>D = Drive Select Bit<br>HS3 - HS0 = Logical Head Select Bits | | | | | | | |

SS1 and SS0 (sector size bits) are set to 0 and 1, respectively. This setting fixes the sector size at 512 bytes/sector. When the D bit is set, the slave drive is selected. When the D bit is reset, the master drive is selected. HS3 - HS0 specify the desired logical head number. The contents of this register are used by the following commands:

Recalibrate
Seek
Read Sector
Write Sector
Format Track
Read Verify
Set Drive Parameters
Read Multiple
Write Multiple
Set Multiple
Read Buffer
Write Buffer
Identify Drive
Set Buffer Mode

### 5.2.9 Status Register

The Status Register contains the drive's status following a command. Reading the Status Register resets any pending interrupt. These are the bit assignments:

| Bit Position | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | WF | SC | DRQ | CORR | IDX | ERR |

| | |
|---|---|
| BSY | Busy, indicates state of controller |
| RDY | Ready, indicates state of target drive |
| WF | Write Fault, indicates hazardous condition and aborts the requested command |
| SC | Seek Complete |
| DRQ | Data Request |
| CORR | Data Was Corrected |
| IDX | Index, index pulse of target drive |
| ERR | Unrecoverable error |

Status Bit 7 (BSY)
This bit reflects the state of the controller. It is activated with a command request, and it is deactivated at command completion. An attempt by the host to read any task file register other than the Status Register while BSY = 1 results in the host receiving the contents of the Status Register.

Status Bit 6 (RDY)
This bit reflects the state of the target drive. Any command requested while RDY = 0 is not honored. If a command request is executed and, if RDY becomes inactive, the command is aborted.

Status Bit 5 (WF)
This bit indicates the occurrence of a write fault at the target drive. The presence of a write fault condition causes the current command request to abort. Subsequent command requests are not honored until the condition clears.

Status Bit 4 (SC)
When set, this bit indicates the last requested seek has been completed.

Status Bit 3 (DRQ)
This bit is high when data is to be transmitted between the host and target controller.

Status Bit 2 (CORR)
When this bit is set, it indicates that one or more of the sectors sent to the host had a correctable error in the data field which was corrected via the ECC algorithm.

Status Bit 1 (IDX)
This bit reflects the target drive's index pulse.

Status Bit 0 (ERR)
When this bit is set, it indicates that an unrecoverable error has occurred. The host may ascertain the type of error by reading the Error Register.

### 5.2.10 Command Register

The host requests a controller/drive function by writing a function code in the Command Register. The write action sets the BSY bit in the Status Register. See section 5.3 for a description of all commands supported by the Caviar.

### 5.2.11 Alternate Status Register

The Alternate Status Register provides the same information (without resetting a pending interrupt) as the Status Register at a different address.

### 5.2.12 Fixed Disk Control Register

The Fixed Disk Control Register allows for a programmable controller reset and provides the ability to enable or disable control of the fixed disk priority interrupt.

| Bit Position | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | RST | IDS | 0 |

The software-controlled reset bit (RST) maintains the fixed disk in a reset condition as long as it is active (high). This bit must be turned on for a minimum of 5.0 microseconds, then off, to complete the reset function.

In dual drive configurations, the slave drive negates PDIAG upon receiving the reset signal and asserts PDIAG after completing its reset routines. The master drive, after completing its reset routines and before negating BSY, waits up to 3 milliseconds for the slave drive to assert PDIAG.

The interrupt disable control bit (IDS) is used to disable (high) or enable (low) controller interrupts. Disabling an interrupt does not clear a pending interrupt. Disabling interrupts also tristates the INTRQ line. A pending interrupt executes once interrupts are re-enabled. Interrupts are disabled following a system master reset.

### 5.2.13 Digital Input Register

The Digital Input Register reflects the current state of the floppy change flag and the fixed disk drive's select, head select and write gate signals. If the floppy disk option on the adapter board is not installed, bit 7 remains tristated.

| Bit Position | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DCG | $\overline{WTG}$ | $\overline{HS3}$ | $\overline{HS2}$ | $\overline{HS1}$ | $\overline{HS0}$ | $\overline{DS2}$ | $\overline{DS1}$ |
| DCG | Diskette Change Flag | | | | | | |
| $\overline{WTG}$ | Write Gate On | | | | | | |
| $\overline{HS3}$,$\overline{HS2}$, $\overline{HS1}$, $\overline{HS0}$ | Drive Head Select (binary) | | | | | | |
| $\overline{DS2}$,$\overline{DS1}$ | Drive Select | | | | | | |

| Command | Hex Opcode | Binary Opcode | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Recalibrate | 1X | 0 | 0 | 0 | 1 | X | X | X | X |
| Seek | 7X | 0 | 1 | 1 | 1 | X | X | X | X |
| Read | 2X | 0 | 0 | 1 | 0 | 0 | 0 | L | R |
| Write | 3X | 0 | 0 | 1 | 1 | 0 | 0 | L | R |
| Format Track | 50 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Read Verify | 4X | 0 | 1 | 0 | 0 | 0 | 0 | 0 | R |
| Execute Diag. | 90 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Set Drive Parameters | 91 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Read Multiple | C4 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Write Multiple | C5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| Set Multiple | C6 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| Reserved | E0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Read Buffer | E4 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| Write Buffer | E8 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| Identify Drive | EC | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Set Buffer Mode | EF | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| L = Long mode bit | 0 = Normal mode, normal ECC functions<br>1 = Long Mode |
| R = Retry bit | 0 = Error retries and ECC enabled<br>1 = Error retries disabled |
| X = Don't Care | |

*Table 5-6. Standard Command Opcodes*

## 5.3 Caviar AC140/AC280 Commands

Table 5-6 lists the binary/hexadecimal codes specific to each command supported by Western Digital's Caviar intelligent drive.

To initiate a controller operation, the host first transfers the pertinent information to the task file and writes the command to the Command Register. The controller validates the contents of the task file registers and then performs the desired function. The Caviar commands are briefly defined in the following subsections.

### 5.3.1 Recalibrate (10H)

The Recalibrate command causes the Caviar to move the read/write heads from anywhere on the disk to cylinder zero. Upon receipt of the command, the intelligent drive asserts BSY and issues a seek to cylinder zero. The intelligent drive waits for assertion of SEEK COMPLETE before updating the Status Register, clearing BSY, and setting INTRQ. If the read/write heads cannot reach cylinder zero, the ERR bit and TK0 bit are asserted in the Status and Error Registers, respectively.

The Recalibrate command does not invalidate any cache segments, but ensures that any segment associated with the new physical cylinder number becomes the current read/cache segment.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 0 | 0 | 1 | X | X | X | X |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |
| D = Drive Designation Bit | X = Don't Care | | | | | | | |

### 5.3.2 Seek (70H)

The Seek command positions the read/write heads over the cylinder specified in the task file's cylinder number registers. When the command is received, the Caviar asserts BSY in the Status Register, starts the seek operation, and sets INTRQ. The seek is not completed before the Caviar returns the interrupt. If BSY is cleared before SEEK COMPLETE is asserted, the Caviar can receive another command. SEEK COMPLETE is asserted when the heads reach the specified cylinder.

Seek does not invalidate any cache segments, but ensures that any segment associated with the new physical cylinder number becomes the current read/cache segment. For performance in multi-tasking environments where overlapped seeks are utilized, the Seek command references the cache hit score and defers the seek until a cache run has completed.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 1 | 1 | 1 | X | X | X | X |
| SDH | Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| X = Don't Care | | | | | | | | |

### 5.3.3 Read Sector (20H)

For a Read Sector command, the task file's registers determine the number and location of the sectors transferred to the host. The host can request a maximum of 256 sectors, but only single-sector reads are allowed in long mode. A sector count of zero specifies 256 sectors. If the drive is not positioned at the specified cylinder, an implied seek occurs. If the long mode bit is set, four ECC bytes are transferred along with the data. Single burst data errors of up to 11 bits are corrected if retries are enabled and the long mode is not selected. An interrupt occurs before the data read from each sector is transferred to the host.

With CacheFlow, the requested sector address and sector count parameters are monitored to perform segment partitioning and sequential/repetitive switching. If partitioning changes are not required, the currently active segment is checked for data. If the physical cylinder is valid, but no data is present, a read disk operation begins. If the physical cylinder is invalid, other active cache segments are checked for data before the seeking operation begins. If the read disk operation must proceed to the next cylinder, other active cache segments are once again checked for data before the seek. Switching cylinders always opens a new cache segment for the new read disk operation.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 0 | 1 | 0 | 0 | 0 | L | R |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | 1 – 256 Sectors to be Read | | | | | | | |
| Sector Number | Starting Sector Number | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| L= Long Mode Bit | R = Retry Bit | | | | | | | |

### 5.3.4 Write Sector (30H)

For a Write Sector command, the host transfers a number of sectors (1-256) to the drive, starting at the logical address specified by the task file registers. Only single-sector writes are allowed in long mode. An implied seek occurs if the drive is not positioned at the specified address. If the long mode bit is set, then the host will transfer four ECC bytes along with the data.

An interrupt is generated as the data for each sector is required, except the first. The first data buffer contents are sent after the host has issued the command and the data request status bit is "on."

DRQ must be received before the host write buffers begin transferring to the base segment. The base segment is reserved for write operations. Other caching segments remain valid. Caching segments that contain sectors that were referenced by the disk write operation become invalid before the write is completed.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 0 | 1 | 1 | 0 | 0 | L | R |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | 1 – 256 Sectors to be Written | | | | | | | |
| Sector Number | Starting Sector Number | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| L= Long Mode Bit | R = Retry Bit | | | | | | | |

### 5.3.5 Format Track (50H)

The track specified by the task file is formatted with ID and data fields in accordance with the interleave table transferred to the sector buffer. The buffer contains SPT entries, 1 through SPT for the track's ID fields. These SPT values are totally dependent upon the translation mode selected. The buffer must contain descriptors for the current translation SPT value. If these entries are not present, then no operation is executed on that sector. The data fields are initialized to zeroes. The interleave table identifies any bad sectors on a given track and must contain 512 bytes of data. This table is composed of two bytes per sector as follows:

- The first byte is set to "00H" to indicate a good sector or to "80H" to indicate a bad sector.
- The second byte designates the logical sector ID number (1-SPT).

Unused bytes may be uninitialized. The Sectors-per-Track (SPT) and Sector-Size values are specified in the Sector Count and SDH Registers, respectively. Only 512 bytes per sector are allowed. The Sectors-per-Track value in the Sector Count Register must correspond with the value indicated by the Set Drive Parameters command. An interrupt is generated upon completion of the command.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Sectors per Track | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Cylinder Address LSB | | | | | | | |
| Cylinder High | Cylinder Address MSB | | | | | | | |

### 5.3.6 Read Verify (40H)

The Read Verify command is the same as a Read command except that the requested sectors are not transferred to the host.

With CacheFlow, the requested sector address and sector count parameters are monitored to perform segment partitioning and sequential/repetitive switching. If partitioning changes are not required, the currently active segment is checked for data. If the physical cylinder is valid, but no data is present, a read disk operation begins. If the physical cylinder is invalid, other active cache segments are checked for data before the seeking operation begins. If the read disk operation must proceed to the next cylinder, other active cache segments are once again checked for data before the seek. Switching cylinders always opens a new cache segment for the new read disk operation.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 0 | 1 | 0 | 0 | 0 | 0 | 0 | R |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | 1 – 256 Sectors to Verify | | | | | | | |
| Sector Number | Starting Sector Number | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| R = Retry Bit | | | | | | | | |

### 5.3.7 Execute Diagnostics (90H)

The Execute Diagnostics command causes the Caviar to execute its self-test routines and to report a result code in the Error Register as follows:

01 No Error
02 Not Applicable
03 Buffer RAM error
04 WD42C22 register error
05 Microprocessor Internal RAM error or ROM checksum error
8X Slave drive failed

The following tests are performed:

- ROM checksum test
- RAM test. Tests 2 Kbytes of the microprocessor and the 8-Kbyte (32-Kbyte optional) buffer RAM. An incrementing pattern is written to both internal and external RAM and then read back.
- A register test of the WD42C22.

If the Caviar is configured as a master drive, it monitors the PDIAG (passed diagnostics) line. A slave drive pulls this line active low once it has successfully performed its diagnostics. If the Execute Diagnostics command is issued with the slave drive selected, both drives execute the command just as if the command had been issued to the master drive. The master drive's task file drives the bus, and it waits up to five seconds for the slave drive to assert PDIAG. The D bit is always returned as zero to the host following the Execute Diagnostics command.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| SDH | Drive | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |

### 5.3.8 Set Drive Parameters (91H)

The Set Drive Parameters command configures the Caviar for a specific number of sectors per track (SPT) and heads. The values in the Sector Count register and the SDH Register determine SPT and heads, respectively. Regardless of the values for SPT and heads, the Caviar will always be in translation mode. A value of 17 for SPT and a value of 10 heads for the Caviar AC280 and 5 heads for the Caviar AC140 are recommended. These configurations yield 980 host-addressable cylinders.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| SDH | Drive and Heads | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Sectors per Track | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |

### 5.3.9 Read Multiple (C4H)

The Read Multiple command operates similarly to the Read Sectors command except for the following conditions:

- Data transfers occur in multiple sector blocks.
- Long bit is invalid.
- Retries are always performed.

Interrupts and DRQs occur once per block of multiple sectors. The number of sectors per block is set using the Set Multiple command. When the Read Multiple command is issued, the Sector Count value sets the total number of sectors to be transferred (not blocks or block count). Sector count need not be a multiple of the block. Partial block transfers are completed when the remaining sectors are ready for transfer. The Caviar must be in multiple mode for this command to operate correctly. Otherwise, the command aborts.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | 1 - 256 Sectors to be Read | | | | | | | |
| Sector Number | Starting Sector Number | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| Long Mode Bit invalid for this command. Retries always allowed | | | | | | | | |

### 5.3.10 Write Multiple (C5H)

The Write Multiple command operates similarly to the Write Sectors command except for the following conditions:

- Data transfers occur in multiple sector blocks.
- Long bit is invalid.
- Retries are always performed.

Interrupts and DRQs occur once per block of multiple sectors. The Number of Sectors-per-Block value is set using the Set Multiple command. When the Write Multiple command is issued, the Sector Count value sets the total number of sectors to be transferred (not blocks or block count). Sector count need not be a multiple of the block. Partial block transfers are completed when the remaining sectors are ready for transfer. The Caviar must be in multiple mode for this command to operate correctly. Otherwise, the command aborts.

DRQ must be received before the host write buffers begin transferring to the base segment. The base segment is reserved for write operations. Other caching segments remain valid. Caching segments that contain sectors that were referenced by the disk write operation become invalid before the write is completed.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| SDH | Sector Size, Drive and Head | | | | | | | |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | 1 - 256 Sectors to be Written | | | | | | | |
| Sector Number | Starting Sector Number | | | | | | | |
| Cylinder Low | Starting Cylinder LSB | | | | | | | |
| Cylinder High | Starting Cylinder MSB | | | | | | | |
| Long Mode Bit invalid for this command. Retries always allowed | | | | | | | | |

### 5.3.11 Set Multiple (C6H)

The Set Multiple command sets the number of sectors per block to be transferred between the host and the Caviar for the Read and Write Multiple commands. The Number of Sectors-per-Block value is loaded into the Sector Count register. The maximum number of sectors per block is eight. A value beyond the limit causes command termination. A value of one is considered valid. A value of zero disables multiple mode.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Number of Sectors/Block | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |
| D = Drive Designation Bit | X = Don't Care | | | | | | | |

### 5.3.12 Read Buffer (E4H)

The Read Buffer command allows the host to read "Buffer 0" of the Caviar 32-Kbyte RAM cache, i.e., the 512 bytes of the first sector buffer in the base cache segment.

| Register | Binary Opcode | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |
| D = Drive Designation Bit | X = Don't Care | | | | | | | |

### 5.3.13 Write Buffer (E8H)

The Write Buffer command functions identically to the Read Buffer command except that 512 bytes of data are transferred from the host to the Caviar RAM cache.

*Note: The Read and Write Buffer commands only affect the first 512 bytes of the Caviar RAM cache.*

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |
| D = Drive Designation Bit | X = Don't Care | | | | | | | |

### 5.3.14 Identify Drive (ECH)

The Identify Drive command transfers 512 bytes of data that specify the drive's parameters. The host is required to read the parameters out of the sector buffer when the Caviar sets DRQ and IRQ. Table 5-7 lists the parameters read by the host.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | Don't Care | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |
| D = Drive Designation Bit | X = Don't Care | | | | | | | |

| Word | Description* |
|---|---|
| 0 | General configuration (427A hex) |
| 1 | Number of fixed cylinders (980) |
| 2 | Number of removable cylinders (0) |
| 3 | Number of heads (10) (5) |
| 4 | Unformatted bytes per track (9656) |
| 5 | Unformatted bytes per sector (568) |
| 6 | Physical sectors per track (17) |
| 7 | Minimum size of ISG in bytes (7) |
| 8 | Reserved |
| 9 | Minimum PLO bytes (14) |
| 10 - 19 | Serial number (ASCII characters, WDnnnnnn) |
| 20 | Controller type (3) |
| 21 | Controller buffer size in 512-byte increments (62) |
| 22 | Number of ECC bytes transferred on long operations (4) |
| 23 - 26 | Firmware Rev. (ASCII characters, X.XX) |
| 27 - 46 | Controller model number (ASCII characters, WDAC280 or WDAC140) |
| 47 | Number of sectors/interrupt on read/write multiples (8008 hex) |
| 48 | Double word I/O (0) |
| 49 | Relocation capabilities (0) |
| 50-255 | Reserved |
| ** Note: The data structure for the identify drive command contains 512 bytes of information* | |

*Table 5-7. Identify Drive Command*

### 5.3.15 Set Buffer Mode (EFH)

The Set Buffer Mode command enables or disables CacheFlow. If the Precompensation Register is set to AAH, then CacheFlow is enabled. If the Precompensation Register is set to 55H, then CacheFlow is disabled. To modify the default number of cache segments, the Precompensation Register is set to A1H-A5H to enable caching with one to five segments as specified in the following table.

| **Register** | **Binary Opcode** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| SDH | X | X | X | D | X | X | X | X |
| Write Precomp | AAH or 55H, A1H-A5H | | | | | | | |
| Sector Count | Don't Care | | | | | | | |
| Sector Number | Don't Care | | | | | | | |
| Cylinder Low | Don't Care | | | | | | | |
| Cylinder High | Don't Care | | | | | | | |

D = Drive Designation Bit

X=Don't Care

AAH enables look-ahead read.

55H disables look-ahead read.

A1H enables caching with 1 segment.

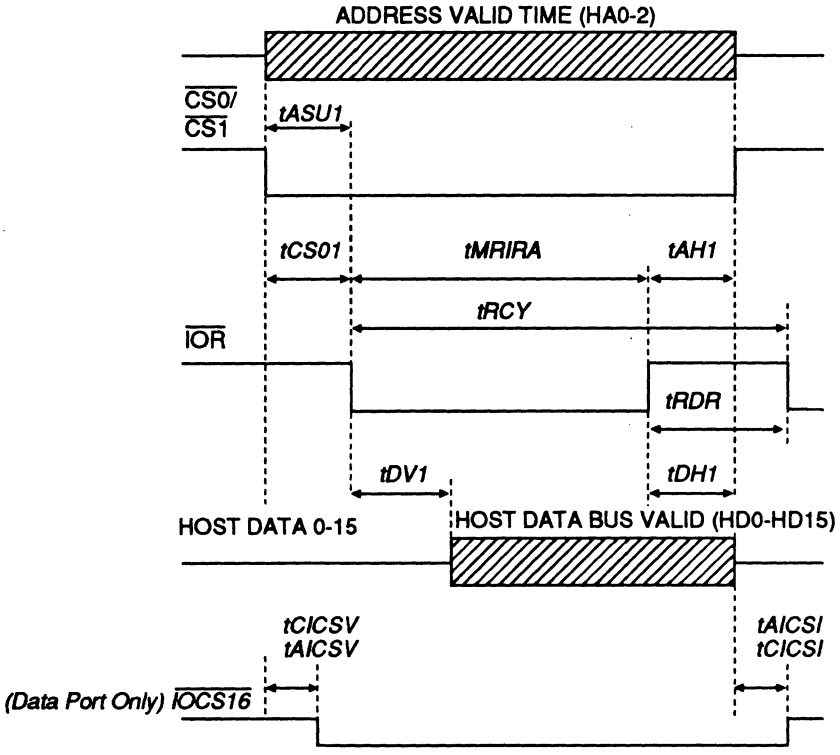
A2H enables caching with 2 segments.

A3H enables caching with 3 segments.

A4H enables caching with 4 segments.

A5H enables caching with 5 segments.

## 5.4 Host Interface Read Timing

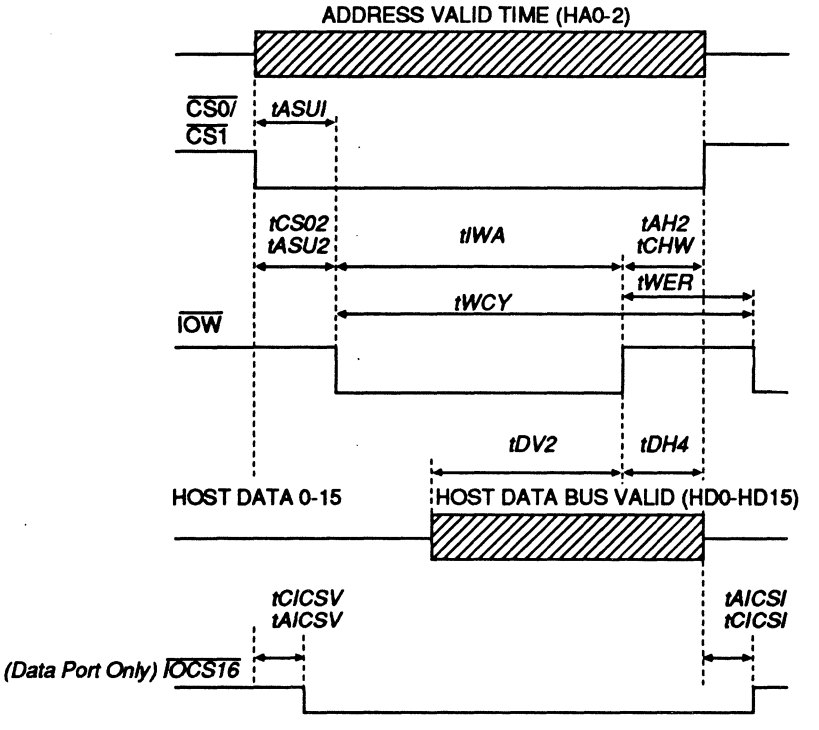



| SYMBOL | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| tASUI | Address setup time | 30 | |
| tCS01 | Chip select setup time | 22 | |
| tMRIRA | I/O read active - Port 0 | 75 | |
| | I/O read active - other ports | 100 | |
| tAH1 | Chip select/Address hold time | 10 | |
| tDV1 | Data valid time - Port 0 | | 60 |
| | Data valid time - other ports | | 100 |
| tDH1 | Data hold time | 5 | 50 |
| tRDR | Chip select/Read recovery time | 20 | |
| tCICSV | IOCS16 valid from CS0 | | 42 |
| tAICSV | IOCS16 valid from HA0 | | 40 |
| tCICSI | IOCS16 inactive form CS0 | | 47 |
| tAICSI | IOCS16 inactive form HA0 | | 45 |
| tRCY | Read cycle time - Port 0 | 444 | |
| | Read cycle time - other ports | 150 | |

Note: All units of measurement are in nanoseconds, unless otherwise noted.
All values based on a maximum load capacitance of 50 pf.

*Figure 5-2. Host Interface Read Timing*

## 5.5 Host Interface Write Timing




| SYMBOL | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| tASU2 | Address setup time | 30 | |
| tCS02 | Chip select setup time | 22 | |
| tIWA | I/O read active - Port 0 | 75 | |
| | I/O read active - other ports | 100 | |
| tAH2 | Address hold time | 20 | |
| tDV2 | Data setup - Port 0 | 50 | |
| | Data setup - other ports | 50 | |
| tDH4 | Data hold time | 15 | |
| tCHW | Chip select hold time | 10 | |
| tCICSV | IOCS16 valid from CS0 | | 42 |
| tAICSV | IOCS16 valid from HA0 | | 40 |
| tCICSI | IOCS16 inactive form CS0 | | 47 |
| tAICSI | IOCS16 inactive form HA0 | | 45 |
| tWCY | Write cycle time - Port 0 | 444 | |
| | Write cycle time - other ports | 150 | |
| tWER | Write recovery time | 20 | |

Note: All units of measurement are in nanoseconds, unless otherwise noted.
All values based on a maximum load capacitance of 50 pf.

*Figure 5-3. Host Interface Write Timing*

## 5.6 Error Reporting

Table 5-8 lists all the valid error conditions which can occur for a given command. The Caviar drive checks the Command Register at the start of a command to determine if any condition exists which could result in a terminated command. The command is then attempted. Any subsequent error terminates the command at the point where it is encountered.

| Command | Error Message | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | BBD | UNC | IDNF | AC | DRDY | DWF | DSC | CORR | ERR |
| Recalibrate* | | | | V | V | | V | | V |
| Seek | | | | V | V | | V | | V |
| Read** | V | V | V | V | V | | V | V | V |
| Read Long** | V | | V | V | V | | V | | V |
| Write | V | | V | V | V | V | V | | V |
| Write Long | V | | V | V | V | V | V | | V |
| Format Track | | | | V | V | V | V | | V |
| Read Verify | V | V | V | V | | | | V | V |
| Execute Diag. | | | | | | | | | V |
| Set Drive Parameters | | | | | | | | | |
| Read Multiple | V | V | V | V | V | | V | V | V |
| Write Multiple | V | | V | V | V | V | V | | V |
| Set Multiple | | | | V | | | | | V |
| Read Buffer | | | | | | | | | |
| Write Buffer | | | | | | | | | |
| Identify Drive | | | | | V | | V | | V |
| Set Buffer Mode | | | | V | | | | | V |
| Invalid Command | | | | V | | | | | V |

| | | | |
|---|---|---|---|
| BBD | Bad Block Detected | DWF | Drive Write Fault Detected |
| UNC | Uncorrectable Data Error | DSC | Drive Seek Complete Error |
| IDNF | ID Not Found | CORR | Data was Corrected |
| AC | Abort Command Error | ERR | Error Bit is Status Register |
| DRDY | Drive Not Ready Error | V | Valid Error for Command |

* Also sets TK0 in Error Register if track zero not found.
** Also sets DAMNF in Error Register if data address mark not found.

*Table 5-8. Error Reporting*

# 6.0 INSTALLATION AND SETUP PROCEDURES

## 6.1 Unpacking

### 6.1.1 Handling Precautions

Western Digital products are designed to withstand normal handling when unpacking and installing the drive. Care must be taken to avoid excessive mechanical shock or electrostatic discharge that can permanently damage the Caviar and void the warranty. When the Caviar is not in its shipping container or installed in its proper host enclosure, it must be placed on an antistatic surface. To prevent damage, do not unpack your Caviar until you are ready to install it.

***Inspection of Shipping Container***
Carefully examine the container for obvious shipping damage, e.g., holes, signs of crushing, or stains. Notify the carrier and your Western Digital representative if you observe any shipment damage. Always move the shipping container in the upright position indicated by the arrows on the container.

### 6.1.2 Removal From Shipping Container

Remove the Caviar from the shipping container only for inspection or installation. Carefully open the box. The Caviar is always shipped in a foam-insert package. When removing the Caviar from the foam insert, grasp the drive at the sides, behind the bezel (if the Caviar has been shipped with a bezel). Gently place the Caviar in its antistatic bag on a clean, level, grounded work station. Do not stack drives or stand the Caviar on edge.

***CAUTION:*** ***Never drop the Caviar from any height when removing it from the shipping container. Dropping the Caviar can severely damage the head disk assembly or printed circuit board.***

Handle the Caviar only by holding the metal cover of the head disk assembly. Do not touch circuit board components. Do not attempt to open its sealed compartment. Failure to observe these restrictions will void the warranty.

### 6.1.3 Removal From Antistatic Bag

Before removing the Caviar from its antistatic bag:

- Make sure that your work station is properly grounded.
- Wear a properly grounded wrist strap with good skin contact.
- Avoid contact with any component on the printed circuit board.

After attaching your wrist strap, gently remove the Caviar from the antistatic bag. Handle the Caviar only by the base casting areas. Never lift the Caviar by the printed circuit board or the bezel. Handle the Caviar with the printed circuit board facing downward during installation.

### 6.1.4 Moving Precautions

If it becomes necessary to move your computer system, turn off the power to automatically park the heads. Parking moves the heads to a safe, non-data landing zone where they are locked into place. This helps protect the media and the heads from accidental damage due to vibration, moving, or shipping.

## 6.2 Mounting Restrictions

### 6.2.1 Orientation

The Caviar can be mounted in many different ways depending upon the physical design of your system. Figure 2-1 shows the Caviar AC140/AC280 mounting dimensions and location of the screw holes.

### 6.2.2 Screw Size Limitations

The Caviar is mounted to the chassis using four 6-32 screws.

***CAUTION:*** ***Screws which are too long will damage board components. The screw must engage no more than six threads (3/16 inch).***

## 6.3 Installation Configuration

### 6.3.1 Determining Your Configuration

You can configure the Caviar in one of two ways:

- The drive is cabled directly to a 40-pin connector on the motherboard.
- The drive is cabled to an adapter card mounted in one of the expansion slots in the computer.

Both configurations use a 40-pin host interface cable.

If you are using the Caviar drive as one of two hard disk drives in the computer (dual installation), you may use either configuration. In dual installations, you must use a 40-pin host interface cable with three connectors, and daisy-chain the two drives to the motherboard or adapter card. Western Digital provides three adapter cards for use with the Caviar drive:

- The WDAT-140 supports two intelligent drives.
- The WDAT-240 supports two intelligent drives and two floppy drives.
- The WDAT-440 supports two intelligent drives, two floppy drives, two serial ports, and one parallel port.

### 6.3.2 Dual Installations

Dual installations require a master/slave drive configuration, where one drive is designated as the primary (master) drive and the other is designated as the secondary (slave) drive. The Caviar drive is compatible in dual installations with other intelligent drives that support a master/slave configuration. The Caviar drive is not compatible with ST-506 drives.

You can install the Caviar drive with a Conner CP342 or CP3022 drive if the Conner is configured as the master drive. This configuration is supported for all PC/AT-compatible computers except the original IBM PC/AT.

If your installation requires the use of an adapter card, it is useful to know that you may also be able to connect your floppy drive(s) to the adapter card. If you use the WDAT-240 adapter card, you may connect two floppy drives to the adapter card.

### 6.3.3 Jumper Settings

The Caviar drive has a jumper block (J8) located next to the 40-pin connector on the drive. If you are installing the Caviar drive as the only intelligent drive in the system, you do not need to install jumpers on the J8 connector. This is considered a standard single drive installation, and no jumpers are required.

*Note: Even with no jumper installed, the Caviar checks the DRIVE ACTIVE/SLAVE PRESENT (DASP) signal to determine if a slave intelligent drive is present.*

If you have a dual installation (two intelligent drives), you must designate one of the drives as the master and the other as the slave drive. The jumper pins on the J8 connector need to be configured for the dual installation. Refer to Figure 6-1 for an illustration of all jumper settings.

To designate the intelligent drive as the master, place a jumper shunt on pins 5-6. With the Caviar configured as the master drive, the Caviar assumes that a slave drive is present. The jumper on pins 5-6 is optional if the slave drive follows the same protocol (Common Access Method AT Bus Attachment) as the Caviar.

To designate the intelligent drive as the slave, place a jumper shunt on pins 3-4. When the Caviar is configured as the slave drive, the Caviar delays spin up for four seconds after power-up reset. This feature prevents overloading of the power supply during power-up.

If your system is a PC/AT compatible computer not manufactured by IBM, and it contains a Conner CP342 or CP3022 drive, you can install the Caviar drive as a second drive. In this configuration, the Conner drive must be configured as the master, and the Caviar as the slave. To designate the Caviar drive as the slave to the Conner drive, place the jumper shunts on pins 1-2 and 3-4.

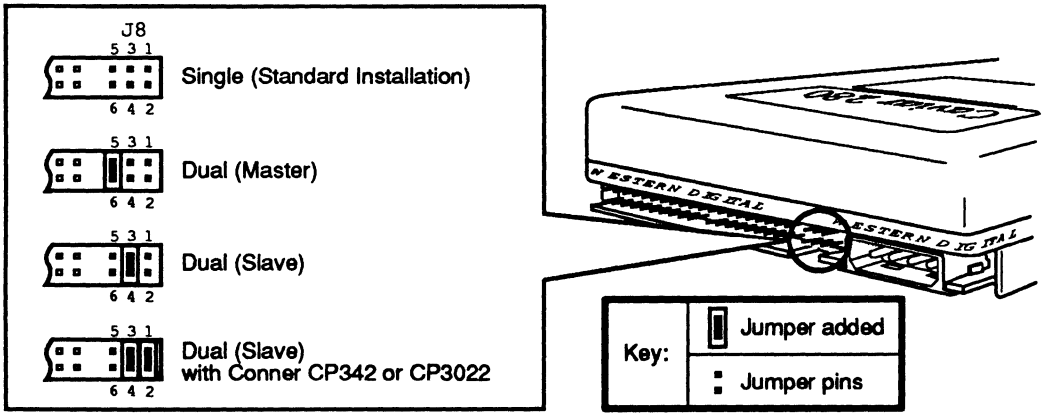



*Figure 6-1. Jumper Settings*

## 6.4 Installing the Caviar Drive

### 6.4.1 Mounting the Drive

For dual installations, it is usually easier to completely install one intelligent drive in the lower position first. The order of intelligent drives is unimportant if you are using two Western Digital drives. As explained previously, one must be jumpered as the master drive and the other as the slave drive. When the installation is complete, the drives are daisy-chained together.

### 6.4.2 Cabling and Installation Steps

Make sure your interface cable is no longer than 18 inches to minimize the noise which is induced on the data and control buses. Also, if you are connecting two drives together, you need a daisy-chain cable that has three 40-pin connectors.

***CAUTION:*** ***You may damage the Caviar drive if the interface cable is not connected properly. To prevent incorrect connection, use a cable that has keyed connectors at both the drive and host ends. Refer to Figure 6-2 which shows pin 20 as the key. (This pin has been removed from the J2 connector. The female connector on the interface cable will have a plug in position 20 to prevent incorrect connection.)***

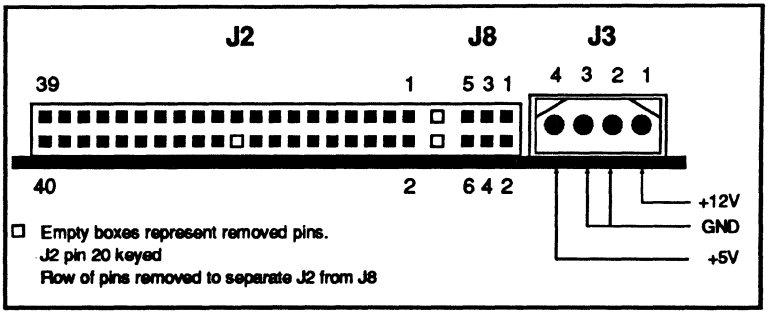



*Figure 6-2. Standard Factory Connectors*

1. Connect the 40-pin interface cable to the 40-pin J2 connector on the Caviar hard drive as shown in Figure 6-3. For dual installations, daisy-chain the two drives together by connecting them with a three-connector interface cable.

2. Route the cable toward the motherboard or card slot area. The cable should easily route from the hard drive to the card slot area. The cable should not block any air flow paths.

3. Insert the drive halfway into the drive bay.

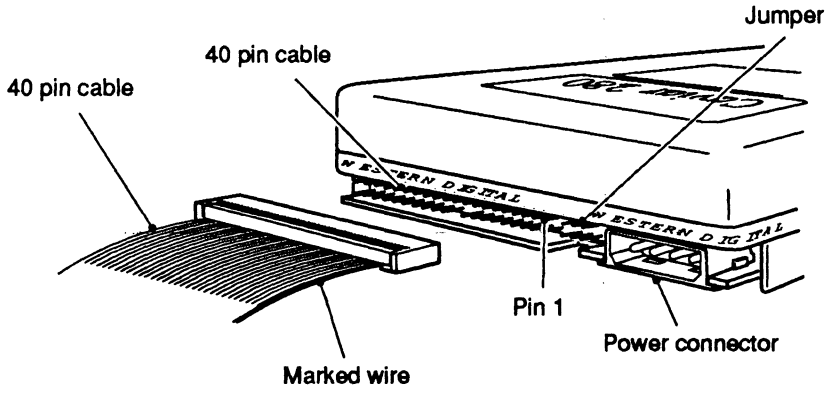



*Figure 6-3. Caviar Connector Locations*

4. Connect the power supply cable to the J3 connector (4-pin power connector shown in Figure 6-2) on the Caviar drive. Dual drive installations: If you do not have two internal power connectors, you will require a Y-adapter to provide power to both units as shown in Figure 6-4.

5. Attach the other end of the power cable to the power supply in your computer.

6. Completely insert the drive into your system drive bay.

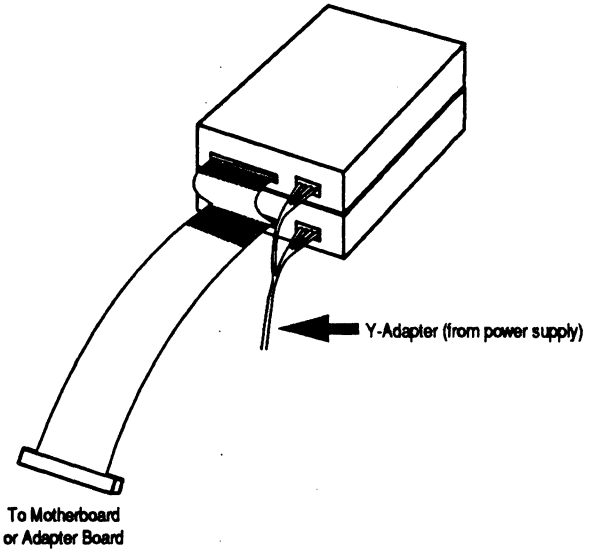



*Figure 6-4. Y-Adapter Cabling*

7. Mount the Caviar drive to the drive bay using four 6-32 screws. Be sure to use the correct size screws. Do not install the screws past six threads (3/16 inch). Screws that are too long will damage the Caviar drive.

***CAUTION:*** ***Screws which are too long will damage board components. The screw must engage no more than six threads (3/16 inch).***

8. Connect the interface cable from the intelligent drive to the host as follows:

- If you have a 40-pin connector on the motherboard, connect the other end of the interface cable to the motherboard connector.
- If your installation requires an adapter card, as explained previously, install the adapter card as described in section 6.5.
- If you do not need to install the adapter card, close the computer case according to the instructions provided in your system manual and proceed to section 6.6.

## 6.5 Installing the Adapter Card

If you are installing the Western Digital adapter card, configuration will probably be unnecessary. You only need to change the default jumper settings if you want to disable the floppy drive controller or set an alternate address at 370-377.

If you need to change the adapter card configuration, do so before attaching any cables or installing the card into the slot.

*NOTE:Remove or disable any existing floppy or serial/parallel controllers which are being replaced by the adapter card controllers.*

For more information on Western Digital adapter cards, contact the Western Digital Literature Distribution Department and request a copy of the AT Host Adapters Installation Guide (Part Number WDATHAIG).

## 6.6 Setup Procedures

### 6.6.1 Preparing the Caviar Drive for Use

The Caviar is preformatted (low level) at the factory and comes equipped with a full complement of defect management characteristics. No modifications are required before installation. If at some later time you need to perform defect management, contact Western Digital Technical Support for information on the WDAT_IDE utility as described in section 8.

Your computer operating system provides an initial setup utility which is either ROM-based or on floppy diskettes. The system setup procedures vary from system to system, but each setup procedure allows you to tell the system what type of hardware you are using. Follow the setup instructions in your operating system manual (MS-DOS or other operating system).

### 6.6.2 Selecting Drive Tables

One step in your computer system setup utility procedure asks you to specify the type of drive used in your system. Use the following procedure to specify your drive type:

- If you are installing the 40 MByte drive in your system, select "drive type 17" from the drive tables displayed during the setup utility procedure. Type 17 typically defines a drive with 977 cylinders, 5 heads, and 17 sectors per track.

- There are no specific standards for the 80 MByte drive. However, the Caviar uses a translation scheme that provides complete compatibility with any drive setup parameters you select. Refer to Table 6-1 for a list of recommended drive parameters. Choose the 80 MByte drive table from the drive tables displayed during the setup utility procedure. Make sure that the total drive capacity (number of cylinders multiplied by the numbers of heads multiplied by the number of sectors/track) does not exceed the total number of sectors available on the drive. i.e., 166,628 for the Caviar AC280 and 83,314 for the Caviar AC140. Refer to section 2 for information on the Caviar drive's physical specifications.

| **Caviar AC140** | | | |
|---|---|---|---|
| Cylinders | Heads | Sectors/Track | Sectors/Drivers |
| 980 | 5 | 17 | 83,300 |
| 977 | 5 | 17 | 83,045 |
| 700 | 7 | 17 | 83,300 |
| 640 | 5 | 26 | 83,200 |

| **Caviar AC280** | | | |
|---|---|---|---|
| Cylinders | Heads | Sectors/Track | Sectors/Drivers |
| 980 | 10 | 17 | 166,600 |
| 640 | 10 | 26 | 166,400 |
| 841 | 6 | 33 | 166,518 |
| 980 | 5 | 34 | 166,600 |

*Table 6-1. Drive Table Parameters*

### 6.6.3 Partitioning the Drive For Use Under DOS

You need to partition your drive(s) to meet certain DOS version requirements. Partitioning divides your disk into one or more partitions that function as separate disk drives. Use the DOS "FDISK" command to display a series of menus that help you partition the hard disk for MS-DOS.

Your version of DOS determines how you can partition your disk(s):

- If you have a DOS version earlier than 3.3, you can only address 32 MBytes maximum on your drive. You cannot partition the drive(s) without second-party software. We recommend that you upgrade to DOS 3.3 or above.

- If you have DOS version 3.3 or above (less than version 4.0), DOS allows you to partition larger drives into logical disk drives with a maximum of 32 M-Bytes per partition.

- If you are working with DOS version 4.0 or higher, you can partition the disk drive(s) into one or more logical drives. You are not limited to 32 MBytes per partition.

"FDISK" automatically assigns drive IDs to the partitions. Refer to your system manual for more information on partitioning drives.

### 6.6.4 High-level DOS Formatting

High-level format the first logical drive (the "C:" drive) by entering "FORMAT C:/S" at the "A:" prompt.

If you designated other drives or partitions during the "FDISK" routine, you need to format those drives as well.

### 6.6.5 Preparing the Caviar Drive For a Novell Network

If you are installing Novell, you must "COMPSURF" the Caviar drive using the following parameters:

| | |
|---|---|
| Format the disk? | No |
| Maintain the current media defect list? | No |
| Enter media defects? | No |
| Number of sequential passes | Default |
| Number of I/O random test | Default |
| Are parameters correct? | Yes |

After running "COMPSURF" on the Caviar drive, enter "NETGEN." Refer to your Novell installation manual for more information on "COMPSURF" and "NETGEN."

### 6.6.6 Booting the System

After you have formatted your drive(s) and installed the operating system on your intelligent drive, re-boot your system.

If your system will not boot, or if you are unable to make the new drive the current drive, refer to your operating system documentation to be sure that you ran the system utility correctly, specified the drive tables, and that you partitioned and formatted your hard disk(s) correctly. If your system still won't boot, you may have improperly installed or connected your hard drive. Re-read the installation instructions provided in this manual to be sure that you installed and connected everything properly.

# 7.0 MAINTENANCE

The Caviar requires no preventive maintenance and contains no user-serviceable parts. The service and repair of the Caviar can only be performed at a Western Digital Service Center. Please Contact your Western Digital representative for warranty information and service/return procedures.

Observe the following precautions to prolong the life of the drive:

- Do not attempt to open the sealed compartment of the Caviar as this will void the warranty.
- Do not lift the Caviar by the bezel or the printed circuit board.
- Avoid static discharge when handling the Caviar.
- Avoid harsh shocks or vibrations.
- Do not touch the components on the printed circuit board.
- Observe the environmental limits specified for this product.
- If it becomes necessary to move your computer system, turn off the power to automatically park the heads. Parking the heads moves the heads to a safe, non-data landing zone and locks the heads into place. This helps protect the media and the heads from accidental damage due to vibration, moving or shipping.
- To protect your data, back it up regularly. Western Digital assumes no responsibility for loss of data. For information about back-up and restore procedures, consult your DOS manual. There are also a number of utility programs available that you can use to back up your data.

# 8.0 WESTERN DIGITAL DRIVE UTILITY

All Caviar intelligent drives are defect-free and pre-formatted (low level) at the factory. After prolonged use, any drive, including Caviar, may develop additional defects. If you continue receiving read (or write) data errors in any given file at the DOS level, then you can use the defect management utility WDAT_IDE. The WDAT_IDE utility program developed for the Caviar recovers, relocates, and rewrites user data to the nearest spare sector and maintains a secondary defect list. WDAT_IDE does not format the entire drive; WDAT_IDE only re-formats the defective sector or track. The Caviar has two spare sectors per cylinder. An entire track is not relocated unless the track contains three bad sectors or multiple non-recoverable errors.

### *Technical Support Bulletin Board*

You may download Western Digital's diagnostic utility, WDAT_IDE from the Technical Support Bulletin Board if you have a modem.

To access the bulletin board you require:

- A Hayes-compatible modem
- 1200 or 2400 Baud rate
- Format: 8 data bits, 1 stop bit, no parity

The Bulletin Board numbers are (714) 753-1234 with a Hayes-compatible modem of 1200 or 2400 baud rate or (714) 753-1068 with a Hayes-compatible modem of 9600 baud rate. The Bulletin Board will ask you some preliminary questions about your modem set-up and the type of system you are calling from before sending you the main menu. Refer to your modem manual for instructions on proper modem setup.

To gain access to the main menu, follow these general steps:

- Select <S> for software
- Select "Storage"
- Select "Utilities"
- Specify WDAT_IDE for the Caviar
- To receive the software program, select <D> and then the transfer protocol. Respond to the prompts for transfer protocol, file name, etc.

On screen Help (H) is available if you have any problems. If you need additional assistance, contact Technical Support at (714) 932-4900.

# 9.0 TROUBLESHOOTING

The following tips and procedures may help you determine the cause of a problem.

- If you have a problem with your Caviar, first re-read the installation instructions to be sure that you followed them correctly. It is important to enter information exactly as instructed.

- Verify that you have correctly followed the setup procedures for your system.

- Verify that you have properly formatted and partitioned the Caviar with DOS FDISK and FORMAT (or an equivalent utility).

- Check your physical installation:
  - Jumper selections on the Caviar
  - Correct cabling
  - Adapter card - properly seated and configured
  - System power supply
  - Controller conflicts

- Observe the environmental limits specified for this product.

If you are unable to resolve your problem, contact your Western Digital representative. If you are unable to contact your Western Digital representative, please contact Western Digital Technical Support at (714) 932-4900.

# 10.0 GLOSSARY

**AT Bus Attachment (ATA)** = The interface defined by International Business Machines for the original AT disk controller. Western Digital designed the Caviar drives to be fully ATA compatible.

**Auto Park** = Turning off the intelligent drive's power causes the Caviar AC140/AC280 to move the read/write heads to a safe non-data landing zone and locks them in place.

**Average Access Time** = The average access time indicates how long it takes the drive to find a block of data on the disk. Average access time is determined by dividing the total time required to seek between all ordered address pairs by the total number of these ordered pairs.

**Block** = A group of bytes handled, stored and accessed as a logical data unit, such as an individual file record.

**Buffer** = A temporary data storage area that compensates for a difference in data transfer rates and/or data processing rates between sender and receiver.

**Class 100** = A clean room standard specified by a U.S. Federal standard. Essentially, the standard limits the number of particles per cubic foot to no more than 100 particles. No particle can exceed 0.5 micron.

**Correctable error** = An error that can be overcome by the use of Error Detection and Correction schemes.

**Data separator** = The data separator (WD10C23) removes phase, frequency and write splice noise from the read data and presents clean digital read signals to the controller. It also conditions write data to be recorded on the drive. Data to be written is precisely clocked from the controller to the WD10C23.

**Data Synchronizer** = An electronic circuit that produces a clock signal that is synchronous with the incoming data stream. The clock signal is then used to decode the data using the appropriate recording code.

**Data Transfer Rate** = The rate that digital data is transferred from one point to another, expresses in bits per second or bytes per second.

- "Data Transfer Rate to Disk" is the internal disk transfer rate in Mbits per second.
- "Data Transfer Rate from the Buffer to the Host" is based on the sustained transfer of buffered data in Mbytes per second.

**Dedicated Landing Zone** = A designated radial zone on the disk chosen to avoid contact with the data cylinders, where contact starting and stopping occur by design.

**Defect Free** = A term used to describe recording surfaces which have no detectable defects.

**Defect Management** = A general methodology of eliminating data errors on a recording surface by mapping out known bad areas of the media. Defective sectors are retried and data is written in alternate locations.

**Error Correction Code** = A mathematical algorithm that can detect and correct errors in a data field by adding check bits to the original data.

**Error Rate** = The number of errors of a given type that occur when reading a specified number of bits.

**Formatted Capacity** = The actual capacity available to store data in a mass storage device. The formatted capacity is the gross capacity minus the capacity taken up by the overhead data required for formatting the media.

**Hard Error** = An error that cannot be overcome by repeated readings and repositioning of the head.

**Hard Sectored** = A technique which uses a digital signal to indicate the beginning of a sector on a track. In contrast, soft sectoring allows the controller to determine the beginning of a sector by reading the format information from the disk.

**Index Pulse Signal** = A digital pulse signal indicating the beginning of a disk revolution. An embedded servo pattern or other prerecorded information is present on the disk following Index.

**Landing Zone** = The heads move to this location on the inner cylinders following a Park command. User data is not stored at this location.

**Latency** = The period of time that the read/write heads wait for data to rotate in an accessible position. For a disk rotating at 3558 RPM, the average latency is 8.45 milliseconds.

**Logical Address** = A storage location address that may or may not relate directly to a physical location. The logical address is usually used when requesting information from a controller. The controller performs a logical-to-physical address conversion and retrieves the data from a physical location in the storage device.

**MTBF** = Mean Time Between Failures

**MTTR** = Mean Time to Repair

**Recoverable Error** = A read error, transient or otherwise, that can be corrected by ECC recovery or by rereading the data.

**Rotational Latency** = The amount of delay in obtaining information from a disk drive that can be attributed to the rotation of the disk.

**Servo Burst** = A momentary servo pattern used in embedded servo control implementations, usually positioned between sectors or at the end of a track.

**Soft Error** = A data error which can be overcome by rereading the data or repositioning the head.

**Uncorrectable Error** = An error that cannot be overcome with Error Detection and Correction.

**Unrecoverable Error** = A read error which cannot be overcome by an ECC scheme or by rereading the data.

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