Rev. 11-25-73	A
Rev. 2-25-74	B
Rev. 4-10-74	C
Rev. 6-3-74	D
Rev. 10-2-74	E
Rev. 11-14-74	F
Rev. 11-20-74	G
Rev. 12-11-74	H
Rev. 12-16-74	I
Rev. 1-30-75	J
Rev. 3-26-75	K
Rev. 5-2-75	L
Rev. 12-15-75	M

PRELIMINARY

C P 1 6 3 1 B

512 X 22 MICROPROGRAM ROM

(MICROM)

PRELIMINARY

PREPARED BY		WESTERN DIGITAL		TITLE CP1631B 512 X 22 MICROPROGRAM ROM (MICROM)	
CHECK BY					
APPD R & D		ISSUE DATE	SHEET 1 of 14	NUMBER 500281	REV M
APPD ENG					
APPD OP'S					

INTRODUCTION

The WDC CP1631B (MICROM) is a 512 word by 22-bit N-channel silicon gate ROM. The ROM coding is programmed on the diffusion mask level (1N). The primary application for the ROM is for microprogram storage in the WDC microprocessor system. It is designed to interface directly with the CP1611B and CP1621B microprocessor chip set. The chip is packaged in a 40-lead plastic cavity dual-in-line package.

FEATURES

- Organization - 512 X 22
- Access Time - < 200 nsec
- Bi-Directional, Common Address and Data Bus Directly Compatible With WDC Microprocessor Microinstruction Bus
- Low Power Dissipation - Typically 150 mW
- Four High Voltage Clocks

OPERATION

The basic operation of the microinstruction Control ROM (MICROM) is to receive addresses sent on the Microinstruction Bus (MIB) from the location counter of the CP1621B Control Chip, decode the address, access the ROM, and then output a 22-bit wide microinstruction to the Microinstruction Bus. The microinstruction address is transferred to the MICROM during Ø2. It is decoded during Ø3 and the ROM is accessed during Ø4. The microinstruction is transferred to the MIB bus at Ø1. Address and data on the MIB is active low (Logic "1" = Low). The MIB bus is precharged high by all MICROMs on the bus as described by the following definitions of pin functions.

1. $\overline{\text{MIBØØ}}$ - $\overline{\text{MIB1Ø}}$; The address is transferred into the MICROM on these lines at Ø2 from the CP1621B. They are unconditionally precharged high at Ø4 by all the MICROMs on the MIB. $\overline{\text{MIBØØ}}$ is the least significant address ($\overline{\text{AØ}}$) and $\overline{\text{MIB1Ø}}$ is the most significant address ($\overline{\text{A1Ø}}$). The microinstruction data is placed on these lines at Ø1 by conditional discharge. $\overline{\text{MIBØØ}}$ is the LSB of the microinstruction. Chip selection is performed by $\overline{\text{MIBØ9}}$, $\overline{\text{MIB1Ø}}$, and Chip Select. These signals are programmable.

2. $\overline{\text{MIB11}}$ - $\overline{\text{MIB14}}$; These lines are microinstruction outputs only. They are unconditionally precharged high at Ø4 and conditionally discharged at Ø1 by the ROM microinstruction data.

3. $\overline{\text{MIB15}}$; This line functions like $\overline{\text{MIB11}}$ - $\overline{\text{MIB14}}$ except that it is precharged high during Ø3 by the MICROM.

4. $\overline{\text{MIB16}}$; This is a MICROM Input and output line. It is unconditionally precharged high at both Ø2 and Ø4. Microinstruction data is transferred out at Ø1 as with the other MICROM outputs. This output will enable the loading of the Return Register (RR) on the Control Chip when it is low at Ø1 ($\overline{\text{LRR}}$). At Ø3 it performs as an Output Enable for the MICROM. If this line is discharged low by the Control Chip at Ø3 then MICROM lines $\overline{\text{MIBØØ}}$ to $\overline{\text{MIB15}}$ and $\overline{\text{MIB18}}$ - $\overline{\text{MIB21}}$ will not be discharged at the next Ø1.

5. $\overline{\text{MIB17}}$; This MICROM output functions like $\overline{\text{MIB11}}$ to $\overline{\text{MIB14}}$. It is used on the Control Chip to enable the "Read Next Instruction" translation while overriding any other translation. Discharging $\overline{\text{MIB17}}$ to a low at Ø1 activates

the translation.

6. $\overline{\text{MIB18}}$ - $\overline{\text{MIB21}}$; These four lines are extra TTL compatible outputs which can be used for external control functions. They are not used by the Control or Data chips. These outputs have wired-OR capability.

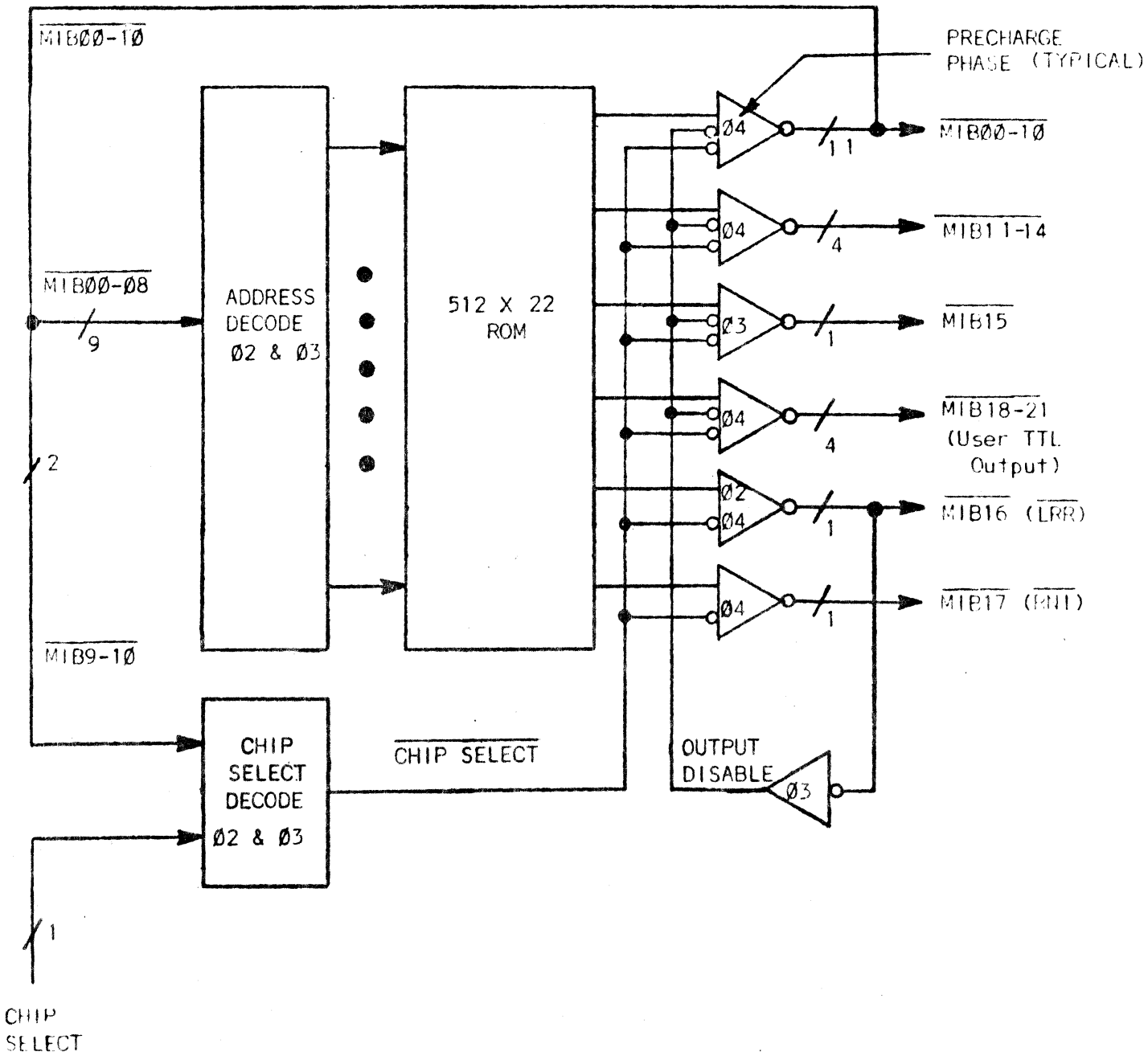
7. CHIP SELECT (CS); This is an MOS level input that will select (Enable) the MICROM with a high input level. This input is sampled like an address input at Ø2.

NOTE: A transistor programmed in the Memory Matrix will read as a high level on the Microinstruction Bus when it is accessed.

Chip Select and Output Disable functions are performed by two additional rows in the ROM Matrix and therefore are programmable to affect any or all of the outputs.

NOTE: The MICROM is responsible for precharging the MIB lines unconditionally. $\overline{\text{MIBØØ}}$-$\overline{\text{MIB14}}$ and $\overline{\text{MIB17}}$-$\overline{\text{MIB21}}$ are precharged high during Ø4. $\overline{\text{MIB15}}$ is precharged high during Ø3 and $\overline{\text{MIB16}}$ is precharged high during Ø2 and Ø4. (The MIB lines are precharged also when the chip is disabled.)

CP1631B - 11K (MICROM)



PREPARED BY		WESTERN DIGITAL CORPORATION	TITLE FIGURE NO. 1 512 X 22 MICROPROGRAM ROM (MICROM) - CP1631B	
APPD OPERS.				
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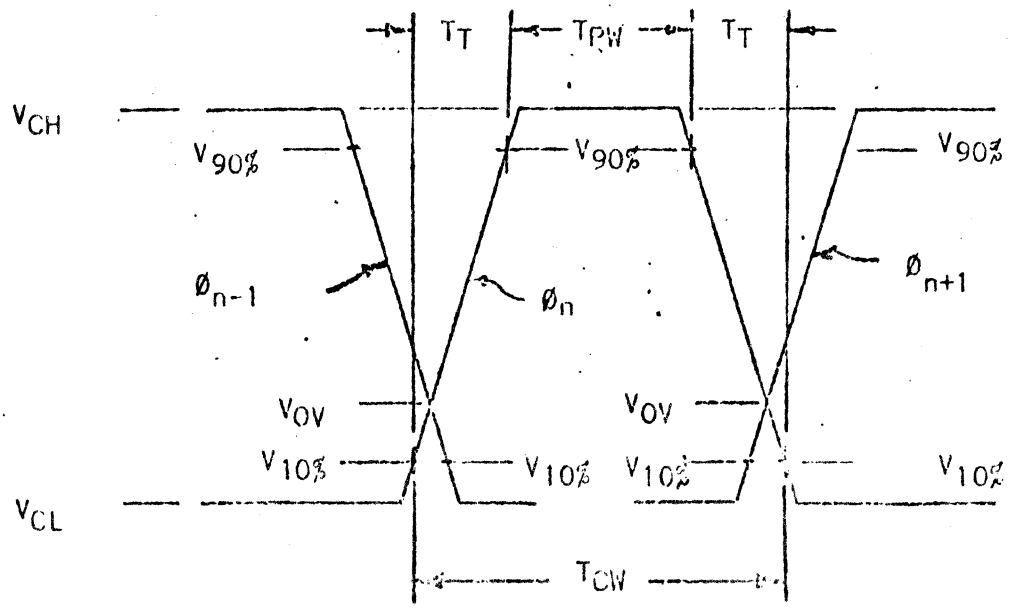
APPD ENG				

CLOCK DIAGRAM



DEFINITION OF 10% AND 90% VOLTAGE POINTS FOR CLOCK, INPUTS AND OUTPUTS

$$V_{10\%} = V_{LOW(max.)} + .1\left[V_{HIGH(min.)} - V_{LOW(max.)}\right]$$

$$V_{90\%} = V_{LOW(max.)} + .9\left[V_{HIGH(min.)} - V_{LOW(max.)}\right]$$

This definition applies to clock, input and output pins.

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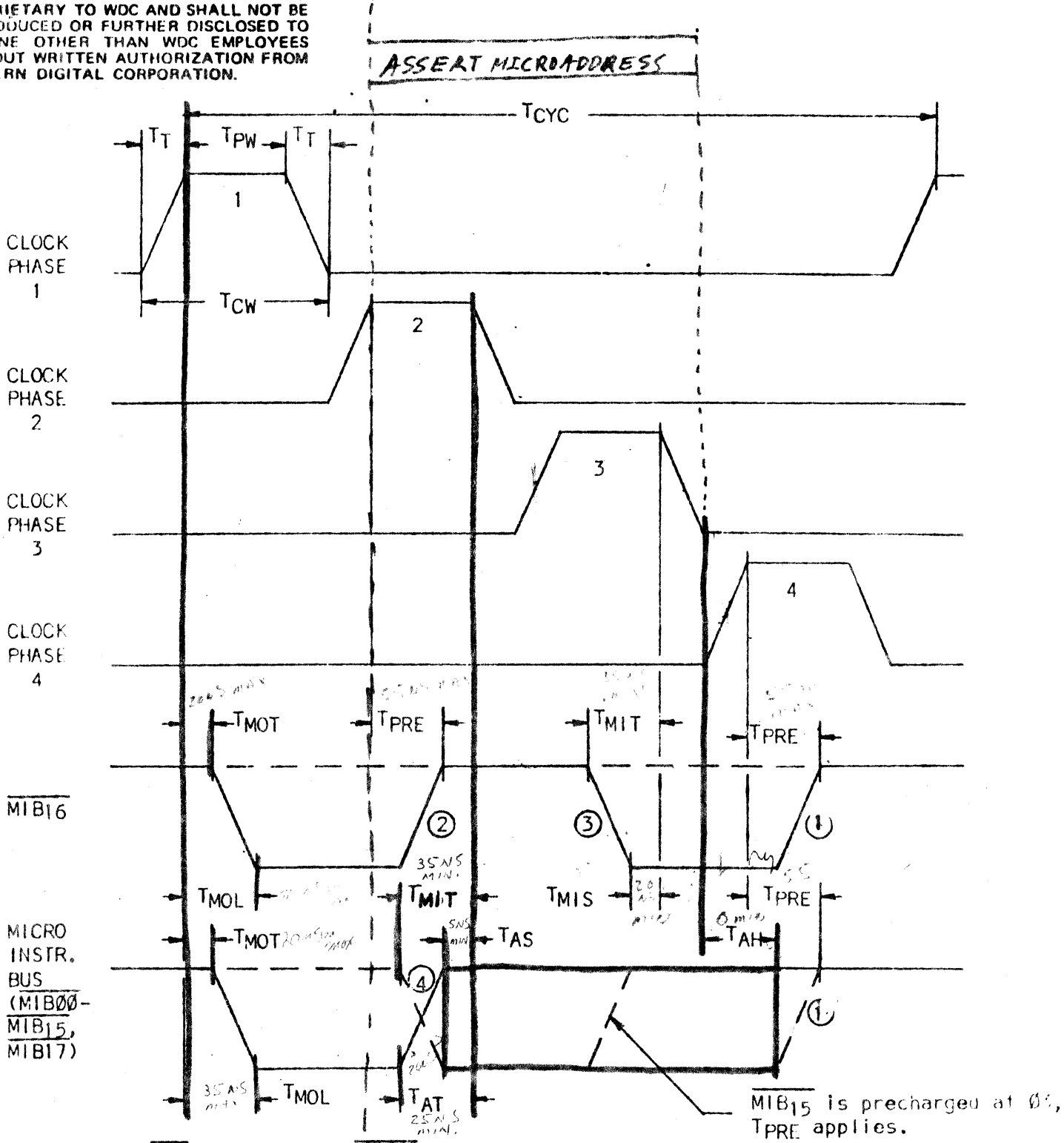
APPD P & D		ISSUE DATE	SHEET 6	NUMBER 500281



NOTES:
1. MIB lines except MIB15 are precharged high at Phase 4.
2. MIB16 is also precharged high at Phase 2.
3. MIB16 is discharged to disable the MIBØØ - MIB15 and MIB18-MIB21 outputs at Ø1 from discharging low.
4. Address input transistions occur only on MIBØØ-MIBIØ lines and Chip Select.
5. Switching times are measured at 10% and 90% of specified levels.

PREPARED BY		WESTERN DIGITAL CORPORATION		TITLE FIGURE NO. 2 MICROM TIMING DIAGRAM CP1641P	
APPD OPERS.					
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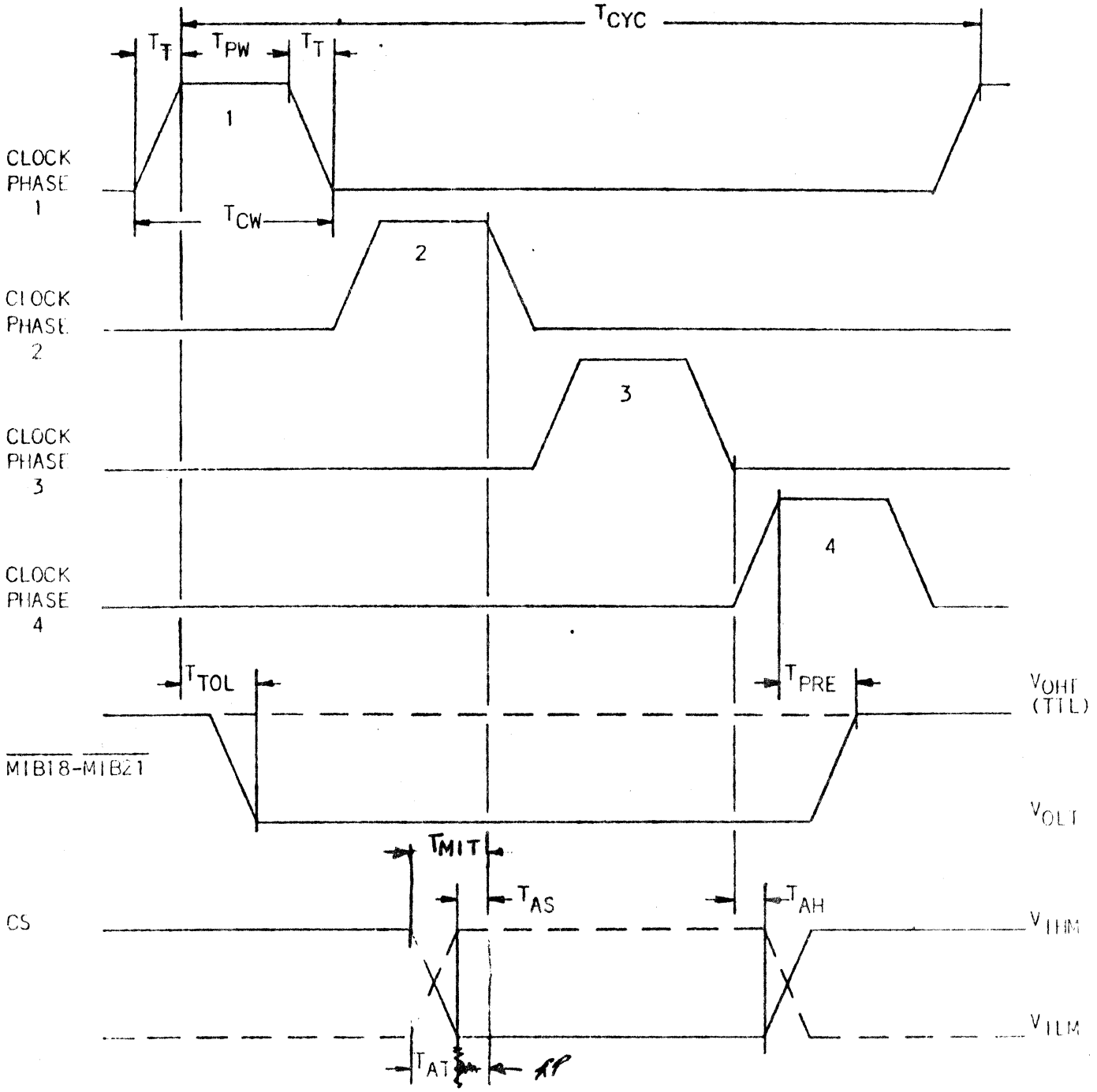
APPD ENG					



NOTE: TTL outputs ($\overline{MIB18}$-$\overline{MIB21}$) are unconditionally driven high at Ø4 and conditionally driven low at Ø1. This conditional low will be valid until the next Ø4.

PREPARED BY		WESTERN DIGITAL CORPORATION		TITLE: FIGURE NO. 3 TTL OUTPUT TIMING CP1631B	
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ABSOLUTE MAXIMUM RATINGS OVER FREE AIR TEMPERATURE RANGE
(Unless Otherwise Noted)*

Supply Voltage V_{DD} (See NOTE)	-0.5V to 15V
Supply Voltage V_{CC} (see NOTE)	-0.5V to 15V
Supply Voltage V_{BB} (see NOTE)	-10V to 1.0V
All Other Pin Voltages (see NOTE)	-1.0V to 15V
Clock Voltage (see NOTE)**	-1.0V to 15V
Operating Free Air Temperature Range	0°C to 125°C
Storage Temperature Range	-55°C to 125°C

NOTE: These voltage values are with respect to V_{SS} Supply Voltage. If V_{BB} is more positive than any other voltage, then I_{BB} must be limited to 10ma.

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum-rating conditions for extended periods may affect device reliability.

** The other three clock voltages must be between 0.5V and -0.6V except for switching overlaps. Not more than one clock may be high at any one time.

Applying power to the part may be any sequence of conditions that do not violate the maximum ratings specified on this sheet.

OPERATING CHARACTERISTICS

T_{CASE} = ØºC to 70ºC, V_{DD} = +12.0V ± .6V, V_{BB} = -3.9 ± .25V, V_{SS} = ØV, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	COMMENTS AND CONDITIONS
I_L	Leakage Current For Any Pin Other Than Clock Or Power			±10	µA	V_{IN} = 5.25V/ØV
I_{BB}	V_{BB} Supply Current			-500	µA	V_{BB} = -5.25V
I_{LC}	Clock Leakage Current			±100	µA	V_{CLOCK} = 13.7V/ØV
I_{CCAVE}	Average V_{CC} Operating Current*		10.0	20.0	mA	T_{CYC} = 300 nsec C_L = 25 pf
I_{DDAVE}	Average V_{DD} Operating Current		10.0	20.0	mA	T_{CYC} = 300 nsec C_L = 50 pf
V_{IHM}	Input High Voltage (All Inputs)	4.0		V_{CC}	V	
V_{ILM}	Input Low Voltage (All Inputs)	0.0.		0.8	V	
V_{OHM}	Output High Voltage (MOS)	4.35		V_{CC}	V	I_O = -30 µA
V_{OHT}	Output High Voltage (TTL)	2.4		V_{CC}	V	I_O = -50 µA
V_{OLM}	Output Low Voltage (MOS)	V_{SS}		0.4	V	I_O = 100 µA
V_{OLT}	Output Low Voltage (TTL)	0.0		0.4	V	I_O = 1.8 ma
V_{OV}	Overlap Voltage Of Any Two Adjacent Clock Phases	0.0		3.0	V	
V_{CH}	Clock High Voltage (SEE NOTE)	11.8 12.0		13.0 13.7	V	V_{DD} = 11.4 V_{DD} = 12.6
V_{CL}	Clock Low Voltage (SEE NOTE)	-0.6		0.5	V	

NOTE: Linear interpolation applies for V_{CH} when V_{DD} is between 11.4V and 12.6V. No overshoot or undershoot allowable.

*Note: The majority of this current is used to precharge the output capacitance, C_L; and therefore, is proportional to the C_L precharged by the MICROM and the frequency of discharge.

AC CHARACTERISTICS

T_{CASE} = ØºC to 70ºC, V_{DD} = +12V ± .6V, V_{BB} = -3.9V ± .25V, V_{SS} = ØV, V_{CC} = +5.ØV ±0.25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{PW}	Clock Width High (All Phases)	55		240	nsec	
T_{CW}	Clock Width Low (All Phases)	75		300	nsec	
T_T	Clock Transition Time (All Phases)	5			nsec	
T_{CYC}	Clock Period (All Phases)	300		1000	nsec	
T_{MOL}	Output Propagation Delay From Ø1 Clock			35	nsec	C_L = 50 pf
T_{PRE}	Time To Precharge Outputs High			55	nsec	C_L = 25 pf
T_{MIS}	Input Set-Up Time on MIB16 At Phase 3	20			nsec	
T_{TOL}	TTL Out Switching Low			55	nsec	Figure 5
T_{AS}	Address Set-Up Time	5			nsec	
T_{AH}	Address Hold Time	Ø			nsec	
T_{MOT}	Output Transition Start Delay Time			20	nsec	C_L = 50 pf
T_{MIT}	Input Transition Start Set-Up Time	35			nsec	
T_{AT}	Address Transition Start Set-Up Time	25			nsec	

CAPACITANCE

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$C_{\emptyset 1}$	Clock Phase 1 Capacitance		20	50	pf	
$C_{\emptyset 2}$	Clock Phase 2 Capacitance		40	60	pf	
$C_{\emptyset 3}$	Clock Phase 3 Capacitance		20	50	pf	V_{IN} = ØV, V_{SS} = ØV, V_{DD} = ØV, V_{BB} = -3.9V f = 1 MHz
$C_{\emptyset 4}$	Clock Phase 4 Capacitance		50	100	pf	
C_D	Data Input/Output Pin Capacitance		5.0	8.0	pf	
C_C	Clock To Clock Capacitance		3.0	6.0	pf	

FIGURE 4

PIN ASSIGNMENT
CP1631B

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Ø3	21	Ø2
2	VBB	22	VCC
3	NC*	23	CHIP SELECT
4	NC	24	NC
5	NC	25	NC
6	NC	26	$\overline{\text{MIB11}}$
7	$\overline{\text{MIB15}}$	27	$\overline{\text{MIB1Ø}}$
8	$\overline{\text{MIB14}}$	28	$\overline{\text{MIBØ9}}$
9	$\overline{\text{MIB13}}$	29	$\overline{\text{MIBØ8}}$
1Ø	$\overline{\text{MIB12}}$	3Ø	$\overline{\text{MIBØ7}}$
11	$\overline{\text{MIB16}}$	31	$\overline{\text{MIBØ6}}$
12	$\overline{\text{MIB17}}$	32	$\overline{\text{MIBØ5}}$
13	$\overline{\text{MIB18}}$	33	$\overline{\text{MIBØ4}}$
14	$\overline{\text{MIB19}}$	34	$\overline{\text{MIBØ3}}$
15	$\overline{\text{MIB2Ø}}$	35	$\overline{\text{MIBØ2}}$
16	$\overline{\text{MIB21}}$	36	NC
17	NC	37	$\overline{\text{MIBØ1}}$
18	NC	38	$\overline{\text{MIBØØ}}$
19	VSS	39	VDD
2Ø	Ø4	4Ø	Ø1

* NOTE: NC means No Connection.

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APPD OP'S					

NEW REVISIONS

REVISION	DATE	PAGES	CHANGES
G	3-25-75	1	New Title Page with new revision
		6	Old: The address remains on the bus for one complete clock cycle. The data is . . . New: The address is valid on the bus during Phases 2, 3, and 4. The data is . . .
		9	CE changes to CS
		10	New Clock Diagram
		11	Output delay times measured from 10% voltages of the clocks.
		12	Delete Supply Voltage V_{CC}.
		13	New
		14	New
		15	V_{IN} = ØV added, and 12V changed to ØV for V_{DD}.
		17	New TTL Output Test Load.
(G)	4-8-75	10	Added "For Clock Inputs and Outputs"
	NOTE: Page 15 becomes Page 16.		
H	5-2-75	1	New Revision added to Title Page.
		10	Comment added: "This definition applies to clock, input and output pins."
		13	I_L Condition line: V_{IN} - changed to V_{IN} =. V_{OLM} Condition line: I = changed to I_O =. V_{CH} and V_{CL} line has same Condition comment.
		14	T_{DOV} and T_{DOT} line Condition statements changed to read: Fig. 5.
		17	Title added: Figure 5, and 50 pf added, from DUT line.
	NOTE: All pages contain current revision letter (H).		
I	11-10-75	11	Redrawn with output delays measured from 90% of clocks, T_{MOT} and T_{MIT} times added
		13	T_A changed to T_{CASE} V_{BB} =-5.0 changed to V_{BB} = -3.9V I_L MAX ±5 changed to ±10 I_{BB} MAX 10Q changed to -500 I_{LC} MAX ±30 changed to ±100 I_{DDAVE} TYP 10 changed to 20.0 I_{DDAVE} MAX 20 changed to 35.0 V_{IHM} MIN 4.0 changed to 4.25 V_{CH} MIN 11.4 changed to 11.8 V_{CH} MAX 12.6 changed to V_{DD} + 1.1V V_{CL} MIN 0.0 changed to -0.6 V_{IHT} MIN 2.4 changed to 3.0 1.0V Overshoot and Undershoot Allowable changed to No Overshoot or Undershoot Allowable

CP1611B

NEW REVISIONS Con't

REVISION	DATE	PAGE	CHANGES
1	11-10-75	14	T_A changed to T_{CASE} V_{BB} = -5.0V changed to V_{BB} = -3.9V T_{PW} MIN 40 changed to 55 T_{CW} MIN 70 changed to 75 T_T MAX dropped T_{MIH} MIN 0 changed to 5 T_{MOL} MAX 40 changed to 35 T_{JOL} MAX 40 changed to 35 T_{DIS} MIN 0 changed to 15 T_{DIH} MIN 0 changed to 10 T_{WLS} MIN 0 changed to 10 T_{MIT} and T_{MOT} added "NOTE: THESE TIMES, ETC." dropped
		15	$C_{\emptyset 1}$ TYP 30 changed to 40 $C_{\emptyset 1}$ MAX 50 changed to 60 $C_{\emptyset 2}$ TYP 30 changed to 40 $C_{\emptyset 2}$ MAX 50 changed to 60 $C_{\emptyset 3}$ TYP 30 changed to 40 $C_{\emptyset 3}$ MAX 50 changed to 60 $C_{\emptyset 4}$ TYP 30 changed to 40 $C_{\emptyset 4}$ MAX 50 changed to 60 C_D MAX 8.0 changed to 15.0 V_{BB} = -5V changed to V_{BB} = -3.9V
NOTE: All pages contain current revision Letter (1)			
(1)	11-14-75	11	T_{WHH} measured from 10% $\emptyset_4$ changed to 10% of $\emptyset_1$
		12	V_{BB} 0.5V changed to 1.0V Pin Voltages -0.5V changed to -1.0V Clock Voltages -0.5V changed to -1.0V Operating Temp. Range 70°C changed to 125°C (If V_{BB} is more, etc.) added to NOTE ** -0.5V changed to -0.6V
		13	I_{LC} CONDITION 12.6V changed to 13.7V V_{IHM} MIN 4.25 changed to 4.1 V_{CH} MAX V_{DD} + 1.1V changed to 13.0 for V_{DD} = 11.4V, 13.7 for V_{DD} = 12.6 V_{CH} MIN 11.8 changed to 12.0 for V_{DD} = 12. NOTE added V_{IHT} MIN 3.0 changed to 2.4
		14	T_{DOV} MAX 75 changed to 70 T_{DOT} MAX 60 changed to 55 T_{WHS} MIN 15 changed to 20 T_{WLS} MIN 10 changed to 20
(1)	11-26-75	15	C_D MAX 10.0 changed to 15.0

Accepted as is
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1/28/76