WANG

6104

VS-25/45 Computer Systems

Customer Engineering
Product Maintenance Manual

741-1032

PREFACE

This document is the Standard Maintenance (STD) Manual for the VS-25/45 Computer Systems. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the VS-25/45 Computer Systems. It will be updated on a regular schedule.

The last page before the back cover is a comment sheet. Please take the time to fill out the comment sheet and return it, via the Home Office mail pouch, addressed to:

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Customer Engineering Technical Documentation
M/S 8237
437 South Union Street.
Lawrence, Mass.
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Fourth Edition (October 1984)

This edition of the VS-25/45 Computer Systems STD manual obsoletes document(s) no. 729-1032-B/B-1. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Service Notices (PSN's) or subsequent editions.

CUSTOMER ENGINEERING

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This PUB: 741-1032-1 VS-25/45 Computer Systems

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REASON FOR CHANGE:

This PUB provides installation, operation, checkout, and troubleshooting instructions for the 2-Megabyte Main Memory Option for the VS-25/45 Computer

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INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	Title Page/ii	Title Page/ii
2.	xiii/xiv	xiii/xiv
3.		Appendix D
4.		
5.		
6.		
7.		
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9.		
10.		

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CUSTOMER ENGINEERING

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This PUB adds a description of the Async. Controller (Appendix E) to the VS-25/45 Product Maintenance Manual.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	xiii/xiv	xiii/xiv
2.	Nothing	Appendix E
3.		
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Update Chapter 7, Illustrated Parts Breakdown

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	xiii/xvii	xiii/xvii
2.	7-1/7-11	7-1/7-11
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WARNING

****
*
* DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY
* CIRCUMSTANCE. EXTREMELY DANGEROUS VOLTAGE AND
* CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-
* LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.
*
* DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER
* SUPPLY; IT IS FIELD REPLACEABLE ONLY.
*
* AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC
* POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,
* ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO
* PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO
* DRAIN THROUGH THE BLEEDER RESISTORS.
*
****

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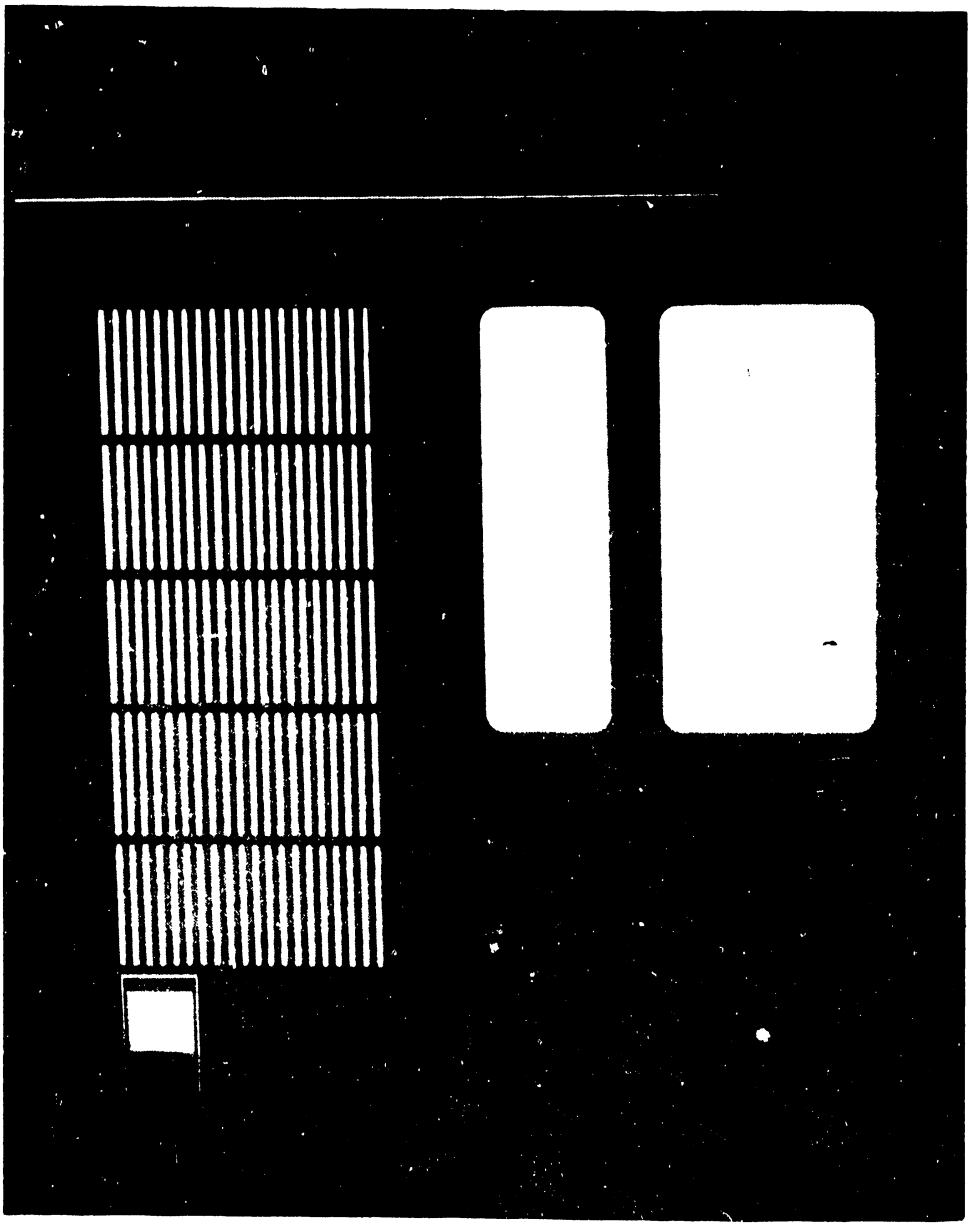

CHAPTER 1 INTRO-DUCTION

CHAPTER 1

INTRODUCTION

1.1 PURPOSE

This manual contains information necessary to install and maintain the VS-25/45 CPU. As new information becomes available it will be provided as either update or revisions to this manual, or as Product Service Notice (PSN) documents.

1.2 SCOPE

This manual is divided into eight chapters, as follows:

Chapter 1: "Introduction" provides information on available VS documentation; gives a brief description of the VS-25/45 system and system software, system configurations, and associated peripherals; and provides system specification information.

Chapter 2: "Theory of Operation" provides a discussion of block diagram level theory for the VS-25/45 CPU and main frame components. The theory explains each logical element beginning at the 'System' level and includes the major component subgroups within a given board.

Chapter 3: "Operation" identifies all VS-25/45 main frame switches and indicators, including a functional description of each, together with settings and operating procedures.

Chapter 4: "Installation" gives guidelines necessary to make sure that the installation site conforms to specific requirements of the VS-25/45 system; provides procedures for unpacking and inspecting the VS-25/45 main frame; and provides instructions for initial set-up and operation of the VS-25/45, together with associated program-loading and operation-confirmation procedures.

Chapter 5: "Preventive and Corrective Maintenance" gives guidelines and schedules for necessary preventive maintenance routines. Included in this chapter is a list of tools and test equipment required for proper repair and maintenance of the VS-25/45 system. Also included are removal and replacement procedures pertaining to disassembly and replacement of system components that are field-replaceable.

Chapter 6: "Schematics" are not provided as part of this Standard Manual. The schematics are published in the VS-25/45 Computer System Schematics Manual, WLI P/N 729-1185-A.

Chapter 7: "Illustrated Parts Breakdown (IPB)" contains the illustrated parts breakdown used for identification when ordering field-replaceable components.

Chapter 8: "Troubleshooting" identifies the available microcode diagnostics, and off-line and on-line diagnostic test programs and gives guidelines for their use. Also provides flow charts for remote diagnostic certification, and troubleshooting flow charts for isolating fault locations to field-replaceable or field-repairable components.

Appendices: The appendices provide the customer engineer with a ready reference of necessary information. These appendices include a mnemonics listing, definitions for signal names, VS-25/45 microinstructions, and the complete list of VS-25/45 Self-test Monitor Diagnostic Error Codes.

1.3 RELATED PUBLICATIONS

The following is a list of current documents published by Customer Engineering required to ensure correct installation and maintenance of a VS-25/45. Also included is a list of current VS documents and data sheets published by Corporate Publications.

Table 1-1. Customer Engineering Publications

SUBJECT	CLASS	PART NUMBER
1.2-Mbyte Diskette Drive (Service SA 850/851)	3101	729-0862
33-Mbyte Quantum Disk Drive	3108	729-1048/53/60
75-Mbyte CDC SMD Disk Drive	3106	729-0211-A
90-Mbyte CDC Phoenix Disk Drive	3105	729-0198-B
288-Mbyte CDC SMD Disk Drive	3106	729-0211-A
620-Mbyte CDC FMD Disk Drive	3106	729-1253/54
2529V Cartridge Tape Drive	3203	729-1184-A
928W Master Data Link	7303	729-1268
6554 TC Processor	7303	729-1043
FTU (Field Test Unit) Operator's Manual	2201	729-0073
Systems Installation Guide - VS, 2200, WP/OIS	1106	729-0907
VS 25/45 Schematics Manual	6104	729-1185-A1
VS Printers	33XX	729-XXXX
VS Reference Summary Guide	6101	729-0716
VS Workstations	3404	729-XXXX

Table 1-2. Corporate VS Documents

DOCUMENT TITLE	PART NUMBER
Customer Site Planning Guide	700-5978D
VS Customer Planning and Resource Guide	700-6727
VS 25/45 SHOWNV/LOADNV NVRAM Utilities, Version 9350	760-1135
VS 25 Bulletin	800-3108-02
VS 3271 Emulation User's Guide (2nd Edition)	800-1306EM-02
VS ATMSWPS Conversion Guide	800-1499TU-02
VS Assembler Language Pocket Guide	800-6203AP-02
VS Assembler Language Reference	800-1200AS-03
VS BASIC Language Reference	800-1202BA-04
VS BASIC Quick Reference	800-6205BQ-01
VS Batch Communications User's Guide	800-1305BC-01

Table 1-2. Corporate VS Documents (cont'd)

DOCUMENT TITLE	PART NUMBER
VS Batch Communication User's Guide Addendum	800-1305BC-01.01
VS COBOL Conversion Guide	800-1204CC-02
VS COBOL Quick Reference	800-6200CP-04
VS COBOL Reference	800-1201CB-06
VS Card Reader Utility Reference	800-1323CU-01
VS EZQUERY Reference	800-1129EQ-01
VS Emulation of SNA 3274 and 3777, General Description	800-1326SE-01
VS FORTRAN Reference	800-1208FR-01
VS File Management Utilities Reference	800-1308FM-02
VS General Purpose Asynch. Comm. Programmers Guide	800-1325AI-01
VS/IIS 5548Z Typesetter Operating Instructions	800-1501TO-01
VS/IIS Advanced Functions Reference Guide	800-1122AR-01
VS/IIS List Management Operator's Guide	800-1120LO-01
VS/IIS Supervisor's Procedures	800-1110WS-02
VS KEYENTRY Operator's Guide	800-1113KO-02
VS KEYENTRY Supervisor's Guide	800-1114KS-01
VS 2265V-3 Disk Drive Operating Procedures Sum. Card	800-6209
VS Model 2529V Cartridge Tape Drive Summary Card	800-6212
VS Model 5575 Band Printer User's Manual	800-1504
VS Operating System Services	800-1107OS-04
VS Operating System Services Pocket Guide	800-6204OP-02
VS PL/1 Language Reference Manual	800-1209PL-02
VS Principles of Operation	800-1100PO-05
VS Procedure Language Quick Reference	800-6201PP-03
VS Procedure Language Reference	800-1205PR-04
VS Program Development Tools Reference	800-1307PT-03
VS Programmer's Guide to VS/IIS	800-1304PW-04
VS Programmer's Guide to VS/IIS Update	800-1304-04.01
VS Programmer's Introduction	800-1101PI-06
VS RPG II Language Reference	800-1203RP-05
VS RPG II Language Reference Addendum	800-1203RP-05.01
VS RPG II Language Reference Addendum	800-1203RP-05.02
VS Software Bulletin - Release 5.3	800-3109
VS Software Bulletin - Release 5.3 Addendum	800-3109.01
VS Software Bulletin - Release 5.3 Addendum	800-3109.02
VS Software Bulletin - Release 6.0	800-3111-01
VS SNA 3777-3 Emulator User's Guide	800-1330
VS SYSGEN Procedure (Release 5.01)	800-8201SP-05
VS System Activity Monitor (SAM) Reference Manual	800-1324-01
VS System Management Guide	800-1104SM-03
VS System Operation Guide	800-1102SO-06
VS System Utilities Reference	800-1303UT-03
VS TOTAL Pocket Guide	800-6207
VS TOTAL Reference Guide	800-1123TR-01
VS Teletypewriter Emulation (TTY) User's Guide	800-1314TU-02
VS USERSUBS Reference	800-1315US-01
VS User Aid COMPILE	800-3312
VS User Aid COMPUTE	800-3301CP-02
VS User Aid LIBRXREF	800-3309XR-01
VS User Aid MAIL	800-3302MA-01
VS User Aid PRINTIBM	800-3308PI-01
VS User Aid PRINTVS	800-3303PR-01

Table 1-2. Corporate VS Documents (cont'd)

DOCUMENT TITLE	PART NUMBER
VS User Aid SORT LINK	800-3310SL-01
VS User Aid TAPEDUMP	800-3311
VS/WP Introducing Word Processing on the VS	800-1407IW-02

Table 1-3. Corporate VS Data Sheets

DATA SHEET TITLE	PART NUMBER
VS Data Communications	800-2107-03
VS Disk Drives	800-2504-03
VS Ergo 2 Ergonomic	800-2500-01
VS EZQUERY	800-2113-01
VS Graphics Facility	800-1446-01
VS Ideographic Data Processing System (Chinese)	800-2502-01
VS Ideographic Data Processing System (Japanese)	800-2501-01
VS/IIS List Management	800-2407LM-01
VS/IIS Readability Index Generator	800-2406RI-01
VS/IIS 5548Z Typesetter	800-2110-01
VS KEYENTRY	800-2300-01
VS Languages	800-2201-07
VS MATHPLANNER	800-1484-01
VS MATHPLANNER	800-1484-02
VS Printers	800-2507-01
VS Processors	800-2105-03
VS Punched Card Reader	800-2506-01
VS Remote WangNet	800-2304-02
VS SNA 3274 Emulation	800-2302-01
VS SNA 3777 Emulation	800-2303-01
VS SNA Emulation	800-2307-01
VS System Activity Monitor (SAM)	800-2116
VS System Software	800-2101-04
VS Tape Drive	800-2505-01
VS Teletypewriter Emulation (TTY)	800-2109-02
VS Transdata 810	800-2119
VS Workstations	800-2503-01
VS/WP Integrated Information System	800-2103-04
VS25 and VS45	800-3107-01

1.4 SYSTEM DESCRIPTION

The Wang VS-25/45 computer system is a high performance data processor with the programming flexibility of Virtual Storage. The differences between the VS-25 and the VS-45 are configuration differences only. (Refer to paragraph 1.13). The VS-25/45 supports interactive, multiuser operations in a general purpose computer environment and offers programming capability in BASIC, COBOL, FORTRAN, PL/1, and RPG II languages. The VS-25/45 also supports Assembler and Procedure languages. The VS Procedure Language Interpreter allows operational sequences to be performed without user interaction.

Serving as a complete commercial data processing system housed in a compact cabinet, the VS-25/45 consists of a CP5 processor with up to 1.024 mega-

bytes of Main Memory; from 33 megabytes (VS-25) to 2.4 gigabytes of on-line disk storage (VS-45 w/large external disk drives); up to 20 workstations; and from one to twelve other types of serial devices. Parallel workstations or printers are not supported on the VS-25/45.

The basic differences between the VS-25 and the VS-45 are as follows:

VS-25	VS-45
1-10 workstations	1-20 workstations
1-6 nonworkstation serial devices	1-12 nonworkstation serial devices
Internal disk drives only	Internal or external disk drives

The VS-25/45 main frame is based on the three major board assemblies shown in figure 2-1, the System Block Diagram. These assemblies are the Central Processor (CP), the Main Memory, and the 8086 microprocessor controlled Bus Processor (BP). The BP and I/O device adapter (DA) section serve as an interface between the peripheral devices and the VS-25/45 system bus.

The following paragraphs provide general descriptions of the major components that make up the VS-25/45 main frame.

1.4.1 CENTRAL PROCESSOR

The CP5 Central Processor (CP) consists of a single CPU board, housed in a compact cabinet with the Main Memory and optional I/O device adapters. The CP5 processor is a faster, more sophisticated version of the CP3 processor used in the VS-50/60/80. It supports the same instruction set as the CP3, with the exception of certain privileged instructions related to address translation.

The VS-25/45 CP supports binary, packed decimal, and floating-point arithmetic. Included in the CP are 32 16-bit general purpose registers and 32 16-bit floating-point and control registers. As in the VS 50/60/80, the machine instruction set is compatible with the IBM 370 instruction set.

1.4.2 CONTROL MEMORY

Control Memory (CM) in the VS-25/45 is 8K words (5 bytes per word) of loadable RAM chips located on the CPU board. Operational or diagnostic microcode may be loaded into CM using either the 2270V-4 Diskette Drive, provided at the front of the VS-25/45 cabinet, or the System Disk Drive. A loadable CM allows for functional CP expansion. For example, CP microcode updates and the use of loadable CP microdiagnostics, is accomplished by using a diskette instead of replacing expensive PROMs.

Eight (K)bytes of PROM, on the Bus Processor board, stores the bootstrap program needed to load the operational or diagnostic microcode into CM.

1.4.3 MAIN MEMORY

The VS-25/45 uses one Main Memory board containing 512K bytes, 768K bytes, or 1.024M bytes. The board is logically divided into 8 rows of 128K bytes with 16 RAM chips per row. Each chip supplies 64K bits X 1-bit of dynamic RAM.

1.4.4 BUS PROCESSOR

The Bus Processor (BP) board, with the 16-bit 8086 microprocessor, has control of the VS-25/45 I/O section. Only one BP can be installed in the VS-25/45. The 8086 microprocessor executes the BP microcode to communicate with the VS-25/45 CPU and to control the Device Adaptors (DAs).

The BP has three major functions. The first is interfacing between the CPU/Main Memory and the device adapters. The second is as a controller for the standard dual-sided, double-density diskette drive, used for loading microcode, diagnostics, and the operating system software. The third is as a telecommunications controller for the Remote Diagnostic functions.

1.5 CPU MOTHERBOARD

The 210-7907 CPU Motherboard provides the link between the CP board, the Main Memory board, the Bus Processor, and all I/O device adapter boards. A brief description of all circuit boards installed, in order, in the VS-25/45 CP Motherboard follows:

1. 210-7900 Main Memory (MM) board - Used for storage of software instructions and data. Three versions are currently available; 210-7900-3A, 4A, or 5A, accessing 512, 768, or 1,024K bytes of RAM respectively. Also contains the Error Detection & Correction circuitry, and the Address Refresh Generator circuitry.

2. 210-8303 Central Processing Unit (CPU) - Contains Control Memory, all general and work registers, status registers, branch decision logic, multiplier, real-time clock, Translation RAM, binary ALU, decimal ALU, instruction counter, trap handling logic, and the System Identification PROM.

3. 210-8304 Bus Processor (BP) board - Has the logic to interface between the CPU, Main Memory, and the Device Adapters; the Diskette Drive Controller; the bootstrap PROM; the NVRAM; and the System Clock. The current version of the BP (210-8304-A) supports 128K bytes of Code RAM (CRAM). A new version (210-8304-1A), under development, will contain 256K bytes of CRAM.

1.6 INPUT/OUTPUT DEVICE ADAPTERS

In the VS-25/45, the BP relieves the CPU of the time consuming task of communicating directly with attached peripherals. With this feature, I/O processing and data processing can run concurrently on the VS-25/45 with the resultant increase in processor job handling speed. Following is a list of the available device adapters for the various peripherals:

1. 25V27 (210-7906) 32-port Serial I/O Device Adapter (SIO DA) - A modified serial data link double buffers the data to/from Main Memory. Control Mode code and all relevant BP information are transferred and/or stored by the BP via the Data RAM (DRAM). Supports the 2246S Serial Workstation, the 2246/56C Combined Workstations, the 2266/76S/C Archiving Workstations, the 2229V Archiving Cartridge Tape

Drive, and the 6554 Telecommunications Processor, plus all serial printers. May be used in place of, but not with, the Intelligent Serial I/O Device Adapter (ISIO DA).

2. 25V37 (210-8616) 32-port Intelligent Serial I/O Device Adapter (ISIO DA) - An intelligent serial master data link of the 928 type. The ISIO DA allows the VS-25/45 to interface with the high speed slave data link channels. Parallel processing supports concurrent Central Processing and multiple Direct Memory Access operations. All of the workstations and serial devices supported by the SIO DA are also supported by the ISIO DA. May be used in place of, but not with, the standard Serial I/O Device Adapter (SIO DA).

NOTE

The 25V37 device adapter requires the installation of the 210-8304-1A Bus Processor and Operating System software version 6.20.

3. 25V55 (210-8325) Quantum Fixed Disk Drive I/O Device Adapter - Designed to support one or two Media Tolerant Quantum Winchester fixed disk drives. The unformatted capacity of each is 34M bytes.

4. 2 50-1/4 (210-8312/13/14/15) 1 to 4-port Storage Module Disk Drive (SMD) I/O Device Adapter - Interfaces with externally housed large disk drives of the CMD (2280V-1/3), SMD (2265V-1,2), and FMD (2265V-3) types. Each SMD DA will only support the number of disk drives indicated by its dash number and cannot be field upgraded. Storage capacity may range from 30 megabytes (one 2280V-1) to 2.4 gigabytes (4 unformatted 2265V-3 FMDs).

NOTE

The 22V65-3 620 Megabyte drive requires support by Operating System software version 6.10.

5. 25V76-1/2 (210-8337/8367) 1 and 2-port Telecommunication I/O Device Adapters (TC DA) - Intelligent adapters which support up to four lines per VS-25/45, using either four 25V76-1 single port adapters, or two 25V76-2 dual port adapters. The system may run a different protocol on each line concurrently from the same DA. Each line is software selectable for RS 232C, RS 366, RS 449, or X.21. and supplied with applicable hardware. Currently supported industry standard protocols for bisynchronous transmission include 2780/3780 emulation, 3271 emulation, and HASP. Data transfer rates to 19.2K Baud per second with protocols of asynchronous, bisynchronous, and bit-oriented synchronous are supported. The device adapter supports bidirectional Direct Memory Access (DMA) on a 16-bit bus to the VS-25/45 Main Memory and the Bus Processor's Data RAM.

NOTE

The 25V76-1 Device Adapter requires minimum Operating System software version 5.03.70.

The 25V76-2 Device Adapter requires the installation of the 210-8304-1A Bus Processor and Operating System software version 6.20.

1.7 SYSTEM DISKETTE DRIVE

The Model 2270V4 Diskette Drive is used for loading microcode, diagnostics, and the operating system software (Coldstart) and will support all of the standard VS utilities.

The drive writes 154 data tracks, with eight 256-byte sectors per track, on two surfaces at double density for a capacity of 1.25 Megabytes. Double-density is obtained by using the modified frequency modulation (MFM) recording method.

1.8 FRONT PANEL

There are facilities available for mounting visual display indicators on the front of the VS-25/45 cabinet.

The Bus Processor has four hexadecimal displays, located on the front panel, to visually display status information to the System Operator.

Each of the Telecommunication lines has an 8-LED display mounted on the front panel which indicates to the System Operator one of three TC states; Off, Normal Status, and Diagnostic Status. In addition, there are two momentary contact switches, Clear and Disconnect, which are used to signal the communication interface of a change in operational status.

Refer to Chapter 3, Operation, and Chapter 8, Troubleshooting, for further details.

1.9 POWER SUPPLY

Power for the VS-25/45 main frame is supplied from a Wang built Model SPS450 Switching Power Supply (279-0735) and supplies all dc voltages. The unit is located on the left side behind the front cover. A red 'LED' located on the front of the supply indicates that all dc voltages are on.

This unit is not accessible by the customer and is not field adjustable. Any work involving this unit should be done by a Wang Customer Engineer (Refer to Chapter 5, Preventive and Corrective Maintenance). Make sure to heed the following warning.

WARNING

```
**************************************************************
*                                                            *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY        *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND          *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-       *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.   *
*                                                            *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER            *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                   *
*                                                            *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC   *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,       *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO    *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO       *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                    *
*                                                            *
**************************************************************
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1.10 SOFTWARE DESCRIPTION

The current minimum operating system support for the VS-25/45 systems is Release 5.03.70. However, this operating system will not support the 22V65-3 620 Megabyte Fixed Module disk drive or the soon to be released Intelligent Serial Device Adapter (ISIO). These and other pending hardware introductions will require a later version of the VS Operating System; e.g. Release 6.10. or 6.20.

Software release 5.03. contained several additional new features and functional improvements over previous releases. Major areas of change are in the Command Processor, the Operator's Console Menu, and the SYSGEN procedure. Most other features of Release 5.03. are similar to previous releases and are discussed in paragraphs 1.10.1 through 1.10.4.

A new operating system release, 6.10, includes several new features and functional changes to VS systems. For complete details, refer to VS Software Bulletin Release 6.10, WLI P/N 800-3111-01. Some of the highlights are listed below.

1. Operating system enhancements:
   a. A Broadcast facility to allow workstation messages to be sent between an Operator's Console and user workstations, including Operator-to-user and user-to-Operator facilities.
   b. Allows assignment of Operator privileges to a User ID as well as to a workstation.
   c. Allows reservation of diagnostic cylinders on 2265V-3 and Q2040 disk drives for stand-alone disk diagnostics.
   d. Extends disk I/O operation timeout period from 60 seconds to 160 seconds.
   e. Changes in the Set Print Mode Default screen to allow spooled print files to be sent to a specific device address (a printer, or a TC device which may be changed to a remote printer) instead of the lowest device-numbered printer available.

2. Networking Operations:
   a. Allows automatically queuing a print file to the Transmit queue so that it can be printed on a remote system.
   b. Allows automatically queuing a print file to the physical system after logging on to a remote VS.

3. COLDSTART:
   a. Can now be used with any VS system, not just VS-25/45 systems.
   b. Permits bringing up a new system by formatting the system disk and copying a minimum system to it.

4. Control Mode Dump:
   a. Is now the same for all VS systems.
   b. Supports an option on VS-24/45/90/100 processors to put a dump on a disk volume as a file, using DISKINIT, while preserving the volume's VTOC.

5. System Software:
   a. Enhancements to several utilities, including BACKUP, CONTROL, COPY, DISKINIT, EDITOR, and SECURITY.
   b. Supports a new utility, IOELOG, for examining an I/O error log file.

6. New Devices:
   a. Release 6.0 supports the following new devices - Wang Professional Computer, 6300GM Graphics workstation, 2529V cartridge tape drive, 2265V-3 620Mb disk drive, and the 5575 band printer.

1.10.1 USER CONVENIENCE FEATURES

The continuing implementation of user convenience features make the VS-25/45 easy to use by programmers and nonprogrammers alike. These features, along with many others, include a versatile data entry, file maintenance, and report generation facility; an interactive text editor for entering and editing source programs; an easy-to-use symbolic debug facility for program debugging; and a large assortment of system utility programs.

1.10.2 EXPANDED OPERATING SYSTEM FEATURES

Recent changes in the Command Processor include a slightly changed Main Menu to reflect the combination of two commands, SHOW DEVICE STATUS and MOUNT/DISMOUNT VOLUMES, into one called COMMAND DEVICES. This new command also includes several new options that allow the user to perform such functions as changing mount restrictions and modifying work and spool file eligibility more easily.

Changes in the Operator's Console menu include the displaying and controlling of all devices through separate PF keys (PF9 through PF13). PF14 now allows setting up eight workstations as dual operator/user mode terminals, and the activating of the PRINT I/O ERROR LOG command.

1.10.3 ADDITIONAL SYSTEM UTILITIES

The VS-25/45 system provides a variety of additional system utility

programs to support the general programming task. These include, among others, the COPY, SORT, and LINK utilities summarized below.

The versatile COPY utility permits the user to copy a single program or data file, an entire library of such files, or a complete disk volume. For data files, the COPY utility provides an option to change the file organization from sequential to indexed or indexed to sequential.

The SORT utility provides high-speed sorting and merging capabilities for both indexed and sequential files, with either fixed or variable length records.

The LINK program is used to link together two or more program modules into a single large program, and also offers the option to remove the symbolic debug information previously inserted for debugging purposes.

Other utilities include a translation utility which translates from EBCDIC to ASCII and vice-versa; a special copy utility which copies and automatically translates Wang 2200 program and data files to VS format (and vice-versa); a display utility, which can be used to display and/or print printer files; a procedure language interpreter utility which allows the programming of operational sequences performed without user interaction.

Table 1-4 lists currently available VS-25/45 utility programs with a brief description of the function of each.

Table 1-4. VS-25/45 System Utility Programs

PROGRAM NAME	DESCRIPTION
ASSEMBLER	Assembles a source program written in VS assembler language.
BACKUP	Copies, consolidates, and Restores a file, library, volume.
BASIC	Compiles a program written in VS BASIC.
COBOL	Compiles a program written in VS COBOL.
COMPRESS	Consolidates used and free extents on a volume.
CONDENSE	Generates single record type data file from multi-record type.
CONTROL	Creates a Control file that defines all field, record, and file attributes for a specified data file.
COPY	Copies files/libraries/volumes from one location to another. Also modifies/rebuilds file organization or index structures.
COPY2200	Copies and automatically converts files from standard 2200 format to standard VS format, and vice versa.
COPYWP	Copies/deletes/renames/reorganizes/merges documents/libraries from one VS WP system to another. Converts a document to file or a file to document for VS data, source, print, or 2780 TC.
DATENTRY	Creates and/or maintains records in a data file as defined by specifications in Control File(s); also lists or prints files.
DEBUGGER	VS Symbolic Debugger allows user to interactively monitor an executing program, locate and correct errors, and alter flow.
DISKINIT	Initializes, Reformats, Relabels, or Verifies a disk volume. Writes a volume label and optional Volume Table of Contents in VS format. Removes and identifies all bad blocks in VTOC.
DISPLAY	Displays file contents on the workstation screen.
DUMP	Creates a print file from a full Segment 2 memory dump which includes a program's variables, buffers, and control blocks using the DUMP function of the Debug Processor.

Table 1-4. VS-25/45 System Utility Programs (cont'd)

PROGRAM NAME	DESCRIPTION
EDITOR	Enters, displays, and edits source procedure or program text.
EZFORMAT	Generates a customized data entry and maintenance program corresponding to a user-designed screen format and control file. Alternate to DATENTRY for existing DMS files.
FORMCNTL	Creates Forms Definition file for VS forms-loadable printers.
FORTRAN	Compiles a program written in VS FORTRAN.
FLOPYDUP	Duplicates diskettes, creates/transfers diskette image files.
IBMCOPY	Copies/converts IBM format diskette file to/from VS file for mat soft-sectored diskettes. Translates ASCII to/from EBCDIC.
INFO	A custom on-line help and information documentation facility.
INQUIRY	Interrogates/tests data files for user-specified field values.
LINKER	Combines two or more compiled or assembled program modules into a single executable program.
LISTVTOC	Produces complete or selective listings of a specified volume's Table of Contents, and examines the VTOC for errors.
LISTWP	Generates summary reports of VS WP documents/file attributes.
PL/1	Compiles source programs written in VS PL/1.
PATCH	Modifies specific HEX values or object files. Prints HEX dump.
PRINT	Places a print file in print queue with user-selected options.
PROCEDURE	An Interpreter utilizing a source program written in Procedure Language to perform interactive and/or background operations.
REPORT	Produces customized reports from a data file.
RPG II	Compiles source programs written in VS RPG II.
SAM	Interactive monitor provides performance/usage of VS system.
SECURITY	Protects system resources at System, File, and Access level.
SORT	Sorts records in data file(s) by key values, with optional capability to merge two or more sorted files.
SYSGEN	Generates control blocks that comprise the Operating System nucleus.
TAPECOPY	Copies any combination of files where tape is in/output media.
TAPEINIT	Initializes 7 or 9 track tape to Wang std., IBM , or NO label format; user select Parity, Density, write end-of-tape marker.
TCCOPY	Emulates IBM 2780/3780 protoculs for non-VS communication.
TRANSL	Automatically translates files to or from ASCII or EBCDIC character sets. Also translates files according to USER defined translation table.
TTY	Emulates standard, asynchronous (ASCII) teletypewriter device.
VERIFY	Tests primary index, alternate indices, and data chain of indexed files to disclose file structure problems.
VSCOPY	VS to VS communication/manipulation of executable image files.

1.10.4 FILE PROTECTION AND SECURITY

All VS-25/45 system disk and tape files are classified according to a flexible file protection and security system, tailored at installation to the specific needs of the user. This system is under the direct control of the System Security Administrator(s) at each installation. The System Security Administrator(s) are specially recognized users who determine the meaning and use of the file protection classes. They are able to access all files on the system, including the System User List and have unlimited access rights.

1.10.4.1 File Protection Codes

Every program, procedure, and data file on the system can be placed in one of thirty file protection classes. Protection class codes are designated by a capital letter, 'A' through 'Z', which represent protection classes whose meanings are assigned by the System Security Administrator(s). Such assignments normally are given mnemonic relationships, as indicated in the following list of "typical" examples:

Class W = The Work Order File
Class P = The Product File
Class C = The Customer File
Class Q = The Sales Quota File

1.10.4.2 Special Protection Codes

The system also recognizes four special (system) classes, " " (space or blank), "$" (currency symbol), "@" (at sign), and "#" (number or pound sign), each of which are reserved for specific uses:

Class " " - Designates UNPROTECTED FILE: Files in this class may be deleted, executed, read, and/or written to by all users. This is the default class for files that are not assigned a system class.

Class "$" - Designates READ/EXECUTE FILE: This file class allows any system user or program to read and/or execute the file, but only the owner of record (that is, the user who created the file) and the system security administrator can write to it. This class is used for subroutines and macros that can be read and incorporated into other program files, but most be protected against direct modification. All system macros are assigned to this file class.

Class "@" - Designates EXECUTE-ONLY FILE: All users may use the file, but only the owner of record and the system security administrator can read it or write to it. Files which must be protected from modification, should be assigned this classification. All system utility files, at system generation time, should also be assigned to this class.

Class "#" - Designates PRIVATE or SYSTEM SECURITY ADMINISTRATION FILES: These files are not available to any of the normal class codes. The "#" class, unlike the other file protection classes, is used to define one protection class (PRIVATE) for each user. When specified, the "#" class code identifies those files which can be accessed only by the owner of record and by the System Security Administrator.

1.10.4.3 User Access Rights

Before users of the system can access a protected file, they must identify themselves using the LOG-ON command. At log-on time, the user's LOG-ON ID and PASSWORD are validated by lookup in the SYSTEM USER LIST, and the user's "access rights" are determined relative to the defined file protection

classes. Access rights are listed in the SYSTEM USER LIST for each file of a protection class and are used to specify three different levels of privilege in order of increasing responsibility, as follows:

1. BLANK " " - Access by System Security Administrator(s) Only.

2. EXECUTE "E" - Execute-Only Access. Applicable to program files only. User may run files of this class, but may not copy, examine, link, modify, or read them.

3. READ "R" - Read, and Execute Access. Program files may be copied, debugged, and linked. Data files may be opened in INPUT mode only.

4. WRITE "W" - Write, Read, and Execute Access. User has complete access rights and may also Scratch, Protect, Modify, Delete and Debug this classification of files.

These access rights are checked whenever a user attempts to execute a program or procedure, open an existing file, or rename or scratch a file.

1.11 ERROR DETECTION AND CORRECTION

To ensure the integrity of information stored in memory and on external storage devices (disks), the system provides automatic error detection and correction facilities. In physical memory, all single-bit errors are corrected automatically, while multi-bit errors cause an error indication. Similar checks also are performed on information stored on disk.

1.12 REMOTE DIAGNOSTIC FACILITIES

Remote Diagnostic Service is a maintenance program that is offered to VS-25/45 customers. The primary goal of the service is to isolate problems remotely so that the Customer Engineer can bring the correct parts and supply the customer with a responsive and efficient level of service.

The VS-25/45 hardware includes a Telecommunication capability on the Bus Processor board to establish a link with the Remote Maintenance Center. The two basic features of the Remote Diagnostic Service involves the ability to read the Nonvolatile RAM (NVRAM), located on the BP board, and the capability to run all the off-line diagnostics remotely. Remote Diagnostic Support is described in paragraph 8.3.

1.13 CONFIGURATIONS

The modular design of the VS-25/45 system permits it to be readily expanded with additional physical memory (to a maximum of 1.024M bytes), on-line storage devices, and additional workstations and printers (to a maximum of 32 SERIAL peripherals). Expansion can be carried out with no impact on existing software, except for the need to "regenerate" the Operating System software to reflect the newly added devices. Consequently, the user with distributed data processing requirements can purchase several assorted system configurations of differing size and complexity, and can use a common set of application software on all systems.

Table 1-5. VS-25/45 Models

MODEL #	SERIAL TAG #	MEMORY SIZE	MAIN MEMORY P/N
VS25-8A	157/177-7131	512Kb	210-7900-3A
VS25-12A	157/177-7132	768Kb	210-7900-4A
VS25-16A	157/177-7133	1024Kb	210-7900-5A
VS25-8C	157/177-7168	512Kb	210-7900-3A
VS25-12C	157/177-7169	768Kb	210-7900-4A
VS25-16C	157/177-7170	1024Kb	210-7900-5A
VS45-8A	157/177-7176	512Kb	210-7900-3A
VS45-12A	157/177-7177	768Kb	210-7900-4A
VS45-16A	157/177-7178	1024Kb	210-7900-5A
VS45-8C	157/177-7181	512Kb	210-7900-3A
VS45-12C	157/177-7182	768Kb	210-7900-4A
VS45-16C	157/177-7183	1024Kb	210-7900-5A
VS45-8X	157/177-7171	512Kb	210-7900-3A
VS45-12X	157/177-7172	768Kb	210-7900-4A
VS45-16X	157/177-7173	1024Kb	210-7900-5A

NOTE

The serial tag number prefix for 50 cps ac line frequency machines is 157. The serial tag number prefix for 60 cps ac line frequency machines is 177.

Table 1-6. VS-25 CPU Configurations

MODEL	MEMORY SIZE	DISK DRIVE(S)	SERIAL PORTS
VS25-8A	512K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS25-12A	768K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS25-16A	1024K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS25-8C	512K bytes	25V55 Disk DA Two 33 Megabyte Fixed Disks Model 2270V-4 DSDD Disk	16
VS25-12C	768K bytes	25V55 Disk DA Two 33 Megabyte Fixed Disks Model 2270V-4 DSDD Disk	16
VS25-16C	1024K bytes	25V55 Disk DA Two 33 Megabyte Fixed Disks Model 2270V-4 DSDD Disk	16

Table 1-7. VS-45 CPU Configurations

MODEL	MEMORY SIZE	DISK DRIVE(S)	SERIAL PORTS
VS45-8A	512K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32

Table 1-7. VS-45 CPU Configurations (cont'd)

MODEL	MEMORY SIZE	DISK DRIVE(S)	SERIAL PORTS
VS45-12A	768K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32
VS45-16A	1024K bytes	25V55 Disk DA 33 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32
VS45-8C	512K bytes	25V55 Disk DA Two 33 Megabyte Fixed Disks Model 2270V-4 DSDD Disk	32
VS45-12C	768K bytes	25V55 Disk DA Two 33-Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32
VS45-16C	1024K bytes	25V55 Disk DA Two 33-Megabyte Fixed Disks Model 2270V-4 DSDD Disk	32
VS45-8X	512K bytes	25V50 Disk DA Model 2270V-4 DSDD Disk	32
VS45-12X	768K bytes	25V50 Disk DA Model 2270V-4 DSDD Disk	32
VS45-16X	1024K bytes	25V50 Disk DA Model 2270V-4 DSDD Disk	32

1.13.1 TYPICAL VS-25/45 SYSTEM-OPTION CONFIGURATIONS

1. VS-25/45 Options:

MODEL	DESCRIPTION
25V37	32-port Intelligent Serial Device Adapter
25V50-1	1-port Storage Module Disk Drive DA (VS-45X only)
25V50-2	2-port Storage Module Disk Drive DA (VS-45X only)
25V50-3	3-port Storage Module Disk Drive DA (VS-45X only)
25V50-4	4-port Storage Module Disk Drive DA (VS-45X only)
25V55	Quantum Fixed Disk Device Adapter (except VS-45X)
25V76-1	Single Port Telecommunications Device Adapter
25V76-2	Dual Port Telecommunications Device Adapter

2. Software For VS-25 System:

   All compilers and utilities
   ADMS
   Word Processing
   Mailway Level II
   Key Entry

3. Software For VS-45 System:

   All compilers and utilities
   ADMS
   Word Processing
   Mailway
   Key Entry
   Voice
   Facsimile

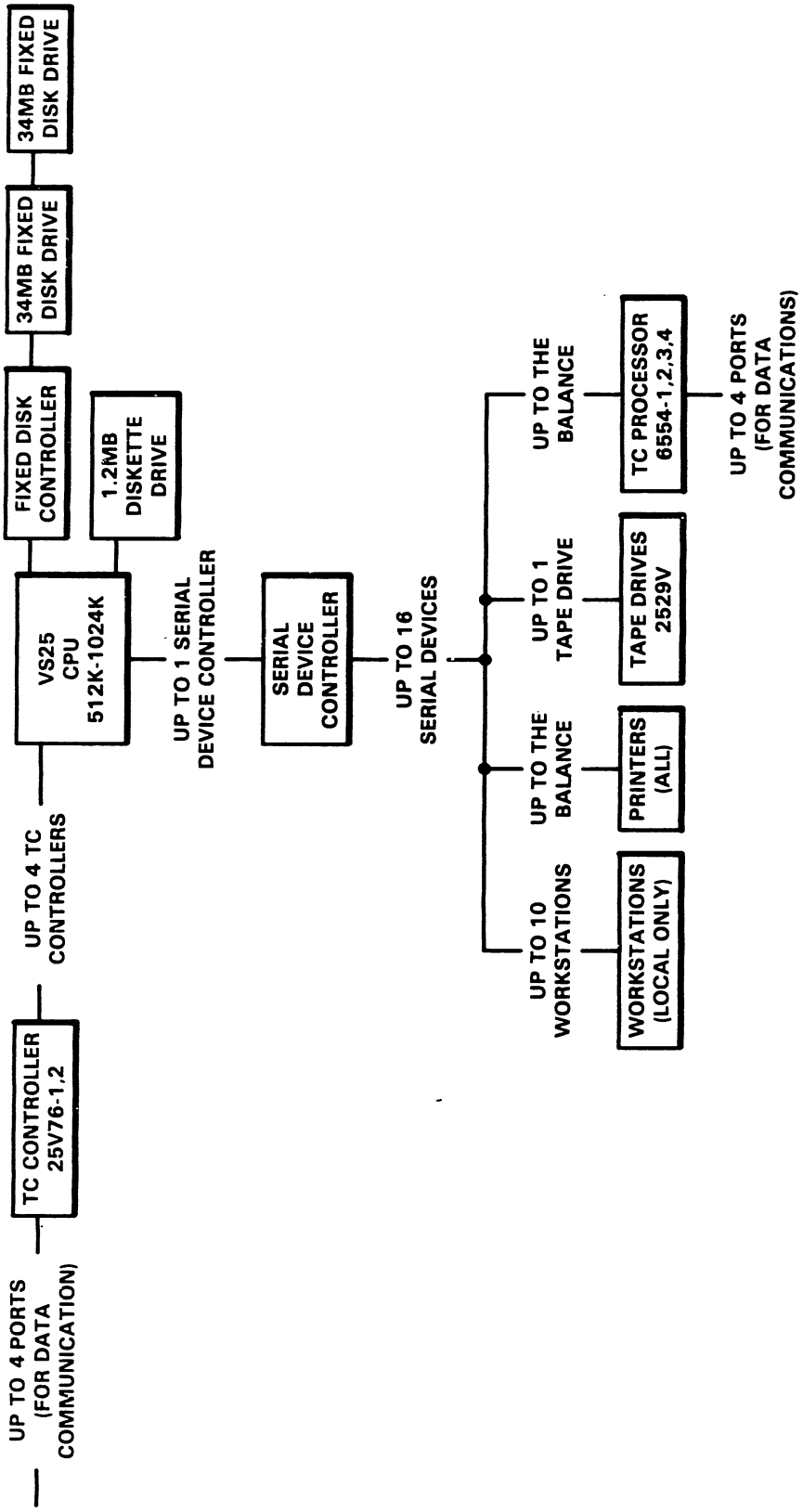

Figure 1-1. VS-25 Configurations

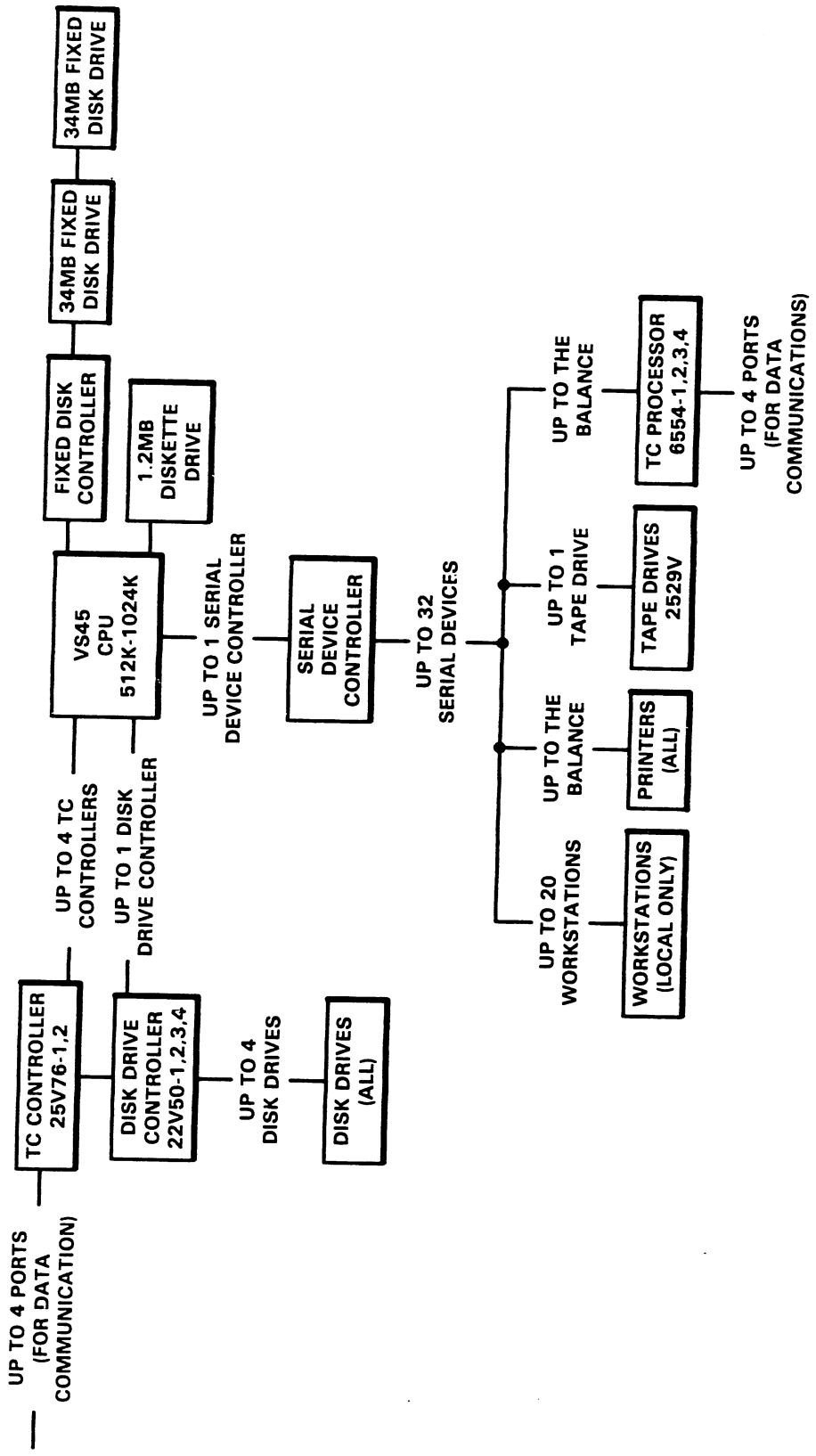

Figure 1-2. VS-45 Configurations

1.14 ASSOCIATED PERIPHERALS

The VS-25/45 system supports currently offered VS peripheral devices, except parallel workstations and printers. The following tables list those peripherals available for the VS-25/45.

Table 1-8. Serial Devices

SYSTEM	DEVICE	MAXIMUM #	ADAPTER	NOTES
VS-25	Workstations	10	25V27 SIO/ 25V37 ISIO	All VS workstations, except remote workstations/printers
VS-25	Printers	6	25V27 SIO/ 25V37 ISIO	All VS printers
VS-45	Workstations	20	25V27 SIO/ 25V37 ISIO	All VS workstations, except remote workstations/printers
VS-45	Printers	12	25V27 SIO/ 25V37 ISIO	All VS printers

Table 1-9. Disk Devices

SYSTEM	DEVICE	MAXIMUM #	ADAPTER	NOTES
VS-25	Quantum	2	25V55	67M bytes maximum capacity
VS-45	Quantum	2	25V55	67M bytes maximum capacity
VS-25	2270V-1/2/3	8	25V27 SIO/ 25V37 ISIO	Plus 8 Archiving Workstations
VS-45	2270V-1/2/3	16	25V27 SIO/ 25V37 ISIO	Plus 16 Archiving Workstations
VS-45	2280V-3 CMD	4	25V50	VS-45X models only. 360M bytes maximum capacity
VS-45	2265V-1 SMD	4	25V50	VS-45X models only. 300M bytes maximum capacity
VS-45	2265V-2 SMD	4	25V50	VS-45X models only. 1.2G bytes maximum capacity
VS-45	2265V-3 FMD	4	25V50	VS-45X models only. 2.4G bytes maximum capacity

Table 1-10. Tape Devices

SYSTEM	DEVICE	MAXIMUM #	ADAPTER	NOTES
VS-25	2529V	1	25V27 SIO/ 25V37 ISIO	Serial cartridge tape drive
VS-45	2529V	1	25V27 SIO/ 25V37 ISIO	Serial cartridge tape drive

Table 1-11. Telecommunications Processors

SYSTEM	DEVICE	MAXIMUM #	ADAPTER	NOTES
VS-25	6554 TCP	1	25V27 SIO/ 25V37 ISIO	1 TCP with maximum of 4 ports
VS-45	6554 TCP	1	25V27 SIO/ 25V37 ISIO	1 TCP with maximum of 4 ports

1.15 TELECOMMUNICATIONS

Versatile data communications facilities for the VS-25/45 are supported by the 25V76-1 (210-8337) and 25V76-2 (210-8637) Telecommunications Device Adapters.

The 25V76-1 (single port option) and the 25V76-2 (dual port option) are intelligent device adapters which support RS-232, RS-449, RS-366, and X.21 interfaces at speeds up to 19.2-K Baud per second. These adapters will be capable of managing asynchronous, bisynchronous, and bit-oriented synchronous proto- cols currently supporting the TCB-1 controller. The device adapters support bidirectional Direct Memory Access (DMA) on a 16-bit bus to the VS-25/45 Main Memory and the Bus Processor's Data RAM.

1.16 SYSTEM SPECIFICATIONS

DIMENSIONS

	INCHES	CENTIMETERS
Width	27.0	68.6
Height	36.0	91.4
Depth	26.5	67.3

SERVICE CLEARANCES

	INCHES	CENTIMETERS
Front	36	91.4
Rear	24	60.9
Left	0	0
Right	0	0
Top	20	50.8

NET WEIGHT

POUNDS	KILOGRAMS
250	110

POWER REQUIREMENTS

	115V/60Hz	230V/50Hz
Ac Variation	+/-10%	+/-10%
Amps	15	7.8
Watts	850	850
Dedicated Circuit	Yes. With 20 Amp circuit breaker in computer room	

HEAT OUTPUT

BTU/HR	KCAL/HR
2890	730

TEMPERATURE

	MINIMUM	MAXIMUM
Fahrenheit	+60°	+90°
Celsius	+15.5°	+32.2°

HUMIDITY

	MINIMUM	MAXIMUM
Noncondensing	20%	80%

ALTITUDE

Maximum

FEET	METERS
10,000	3048

NOTE

Tape drives installed above 4000 ft. (1200 meters) and disk drives installed above 6500 ft. (1960 meters) require high-altitude options.

CABLE LENGTH

Power

FEET	METERS
6	1.8

ARCHITECTURAL

Control Memory Size	- 8 K-Words Maximum.
Virtual Program Address Space	- 1 Mbyte per user (including program file).
Virtual Data Address Space	- 1 Mbyte per user (including system overhead).
Main Memory Size	- 512 Kbytes (min.) to 1.024 Mbyte (max.).
Main Memory Bus Size	- 16-bit half-word, 6-bit parity (ECC) field.
Main Memory Cycle Time, avg.	- 400 nanoseconds (normal read/write), 800 nanoseconds (extended cycle for RMW or error correction).
Main Memory Refresh Cycle	- Every 12.5 microseconds.
System Clock	- 20 MHz, 50 nanosececonds.
CP Microinstruction Size	- 40 bits long (18-bit Process Field, 5-bit Memory Field, 16-bit Branch Field, 1-bit odd parity)
CP Microinstruction Time	- 500 nanoseconds (average)
CP Registers	-Thirty-two 16-bit File Registers. Thirty-two 16-bit System (Control and Floating Point) Registers. Thirty-two 16-bit Auxiliary Registers. Thirty-two 16-bit General Registers. 128 16-bit Work Registers
CP Cycle	- 200 nanoseconds
CP Data Path	- 16 Bits Wide
CP Address Path	- 24 Bits Wide
Main Memory Data Path	- 16 Bits Wide
Main Memory Address Path	- 21 Bits Wide
Bus Processor DA Data Path	- 16 Bits Wide
Device Address Path	- 16 Bits wide

CHAPTER 2

THEORY OF OPERATION

CHAPTER 2

THEORY OF OPERATION

2.1 VS-25/45 OVERVIEW

This chapter provides a block-diagram level theory discussion of the VS-25/45 CPU and main frame components.

The VS-25/45 main frame is based on the three major board assemblies, three external busses, and up to six device adapters boards. The primary functional units are the CP5 Central Processor, the Main Memory, and the 8086 controlled Bus Processor. The Bus Processor and I/O Device Adapters serve as an interface between the peripheral devices and the VS-25/45 Central Processing Unit (CPU). The VS-25/45 CPU consists of the CP5 Central Processor (with it's Arithmetic and Logic Unit [ALU], and instruction interpretation, execution and control functions), Main Memory (MM) storage, and the three system busses. (See figure 2-1, the System Block Diagram.) A brief explanation of each function and their interaction follows.

2.1.1 VS-25/45 MAIN MEMORY BUS

The VS-25/45 Main Memory Bus was designed to integrate memory operations and system communication between Main Memory (MM) and the Central Processor (CP), the Device Adapters (DAs), and a newly designed and more sophisticated Bus Processor (BP). The Main Memory Bus has 61 signal lines who's functions are given in table 2-1 on page 2-3 following.

A requester acquires a bus cycle by raising its Memory Request In (MRI) signal. Main Memory acknowledges this signal giving a Memory Grant Strobe (MGS) to the highest priority requester, which immediately enables its address and control buffers (and if doing a write, its data buffers) onto the Bus. Later in the cycle, if Main Memory needs to give the requester data, it will pulse the Memory Data Strobe (MDS) line. Each requester has a separate MRI and MGS line, but all have a common MDS line. The MDS line notification must be inhibited by the requesters except when their specific MGS is active.

The Main Memory controller uses three Memory Control Bits (MCB0-2) initiated and supplied by the requester to control the request. These three bits are defined to give eight read or write functions during a Main Memory operation: four read/write with error correction and four without. After the operation is complete, the MM controller responds with two Memory Status Bits (MSB0-1) which signals the results of the operation to the requester.

There are three defined states of completion using MSB0-1: a successful operation, an Invalid (or nonexistent) Memory Address (IMA), and an error uncorrected by Error Correction Code (ECC). A double bit error (or an ECC uncorrected error) will be reported by MSB0-1. Corrected single bit errors are not reported by MSB0-1 but are reported to the BP on the Error Count (ECNT) line. The ECNT line sends each single or double bit parity error to a counter on the Bus Processor board.

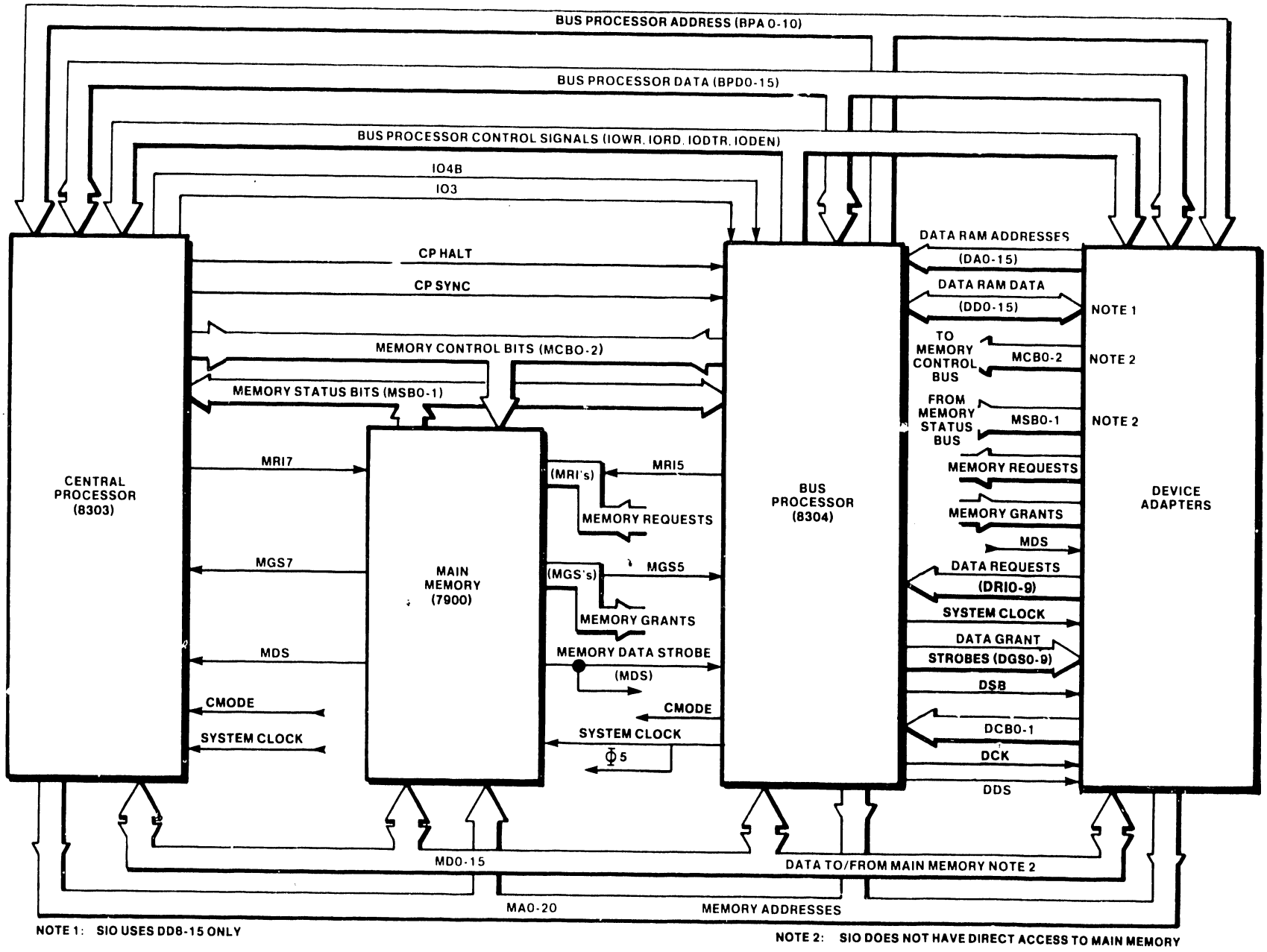

Figure 2-1. VS-25/45 System Block Diagram

Table 2-1. Main Memory Bus

FUNCTION (No. of Lines)	MNEMONICS	OPERATION
Memory Address Lines (21)	MA0-20	BP/CP/DAs to MM (Note 1)
Memory Data Lines (16)	MD0-15	Bidirectional (Note 2)
Memory Control Bits (3)	MCB0-2	BP, CP, or DAs to MM
Memory Status Bits (2)	MSB0-1	MM to BP, CP, or DAs
BP Memory Request In (1)	MRI5	BP to Main Memory
CP Memory Request In (1)	MRI7	CP to Main Memory
DA Memory Request In (6)	MRI0-4, 6	DAs to MM (Note 1)
BP Memory Grant Strobe (1)	MGS5	MM to Bus Processor
CP Memory Grant Strobe (1)	MGS7	MM to Central Processor
DA Memory Grant Strobe (6)	MGS0-4, 6	MM to DAs (Note 1)
Memory Data Strobe (1)	MDS	MM to BP,CP,DAs (Note 3)
MM Error Count Signal (1)	ECNT	MM to Bus Processor
System Clock (20 MHz) (1)	(Phi S)	BP to CP and MM (Note 4)

NOTES

1. The SIO Device Adapter does not have access to Main Memory via the Main Memory Bus. Access is via the Data RAM Bus and the Data RAM which serves as a double buffer.

2. Main Memory Data lines are bidirectional between BP, CP, DAs, and Main Memory except for the SIO DA discussed in Note 1.

3. Inhibited by all requesters unless a specific MGS is active.

4. The System Clock is intended for use by the CP and MM only. (DCK is reserved for the DAs.)

2.1.2 VS-25/45 BUS PROCESSOR BUS

The second major bus on the VS-25/45 is the Bus Processor Bus. The BP Bus provides direct communication with, and control of, the various Device Adapters. It also controls the exchange of status and other information between the BP and the CP. Along with the BP Address and Data lines, it handles the external interrupts from the DAs, the I/O Device Adapter control signals, and the CP control bits and interrupts. (An interrupt is an error condition or a request-for-assistance condition that will cause a break in the normal sequence of instruction execution.) The Control Mode and Initialize functions are routed throughout the system via the BP Bus.

The BP I/O control signals, I/O Data Enable (IODEN), I/O Data Transmit or Receive (IODT/R), I/O Read (IORD), and I/O Write (IOWR), are use to control the Device Adapters' operations and to perform diagnostic functions on the CP. The Bus Processor Bus uses 56 operational signa lnes as shown in table 2-2.

Table 2-2. Bus Processor Bus

FUNCTION (No. of Lines)	MNEMONICS	OPERATION
BP Address Lines (11)	BPA 0-10	BP to CP and DAs (Note 1)
BP Data Lines (16)	BPD 0-15	Bidirectional (Note 2)
BP Interrupt Lines (18)	BPINT 0-17	DA to BP 8086 Processor
Bus Processor I/O Control Signals (4)	IODEN, IODT/R, IORD, and IOWR	BP to Central Processor and Device Adapters.
CP (Command) Control Bits (2)	IO3/IO4B	CP to BP (Note 3)
BP (Command) Control Bit (1)	CMODE	BP to Central Processor
CP Execution Interrupted (1)	CPHALT	CP to BP (Note 4)
CP Comparator Reached (1)	CPSYNC	CP to BP (Note 5)
System Initialization (1)	INIT	PS to BP, CP and DAs
CP Real Time Clock (1)	RECK	PS to CP (Note 6)

NOTES

1. The current Bus Processor hardware only allows for eleven address lines.

2. Bus Processor Data lines are bidirectional between the BP, and the CP, or DAs.

3. IO3 and IO4B are CP to BP control lines where IO3 can be set by the CP and cleared (reset) by the BP, and IO4B is set by the BP and cleared (reset) by the CP.

4. CPHALT is a status signal which indicates to the BP that the CP is not running. The BP can stop and/or start the CP as required.

5. This line is raised (during diagnostic mode only) whenever the CP comparator value (address) is reached.

6. The Real-Time-Clock on the CP is incremented by a pulse from the Power Supply each 1/120th of a second (8.33 ms).

2.1.3 VS-25/45 DATA RAM BUS

The third system-wide bus on the VS-25/45 is the Data RAM Bus. The DRAM Bus provides direct communication with and subsequent control of the Data RAM by the various requesters (Device Adapters, etc.) when they are using the DRAM. It supplies both address and data line access to the Data RAM for all requesters. This allows independent operation of both the DRAM and the BP.

The DRAM Bus supports the path between the DRAM (with it's resident memory controller and parity) and all Device Adapters, a direct path to the BP 8086 microprocessor, and a Direct Memory Access (DMA) path to Main Memory. Any Device Adapter may utilize the DRAM as a double buffer data pool to Main Memory if the hardware and software for that device are so designed (eg: the SIO).

The exchange of status and other information among the BP, the DAs, and the DRAM is accomplished by the DRAM control and request lines on the DRAM Bus. The operation of these lines is essentially the same as their counterparts on the Main Memory Bus (paragraph 2.1.1) with the exception of Error Correction Code (ECC) capability.

The Data RAM does not have Error Detection and Correction circuitry. Instead it uses parity error notification. Consequently, the number of lines for control and status have been reduced by one each (DCB0-1, and DSB). A parity error from the DRAM is reported to the requester on the DSB line. It is non-recoverable since ECC is not used. In addition, DRAM data is not checked for an Invalid Memory Address.

The DRAM Clock (DCK) is a buffered output of the System Clock, and has the same diagnostic feature of fast, normal, and slow operation. It is also controlled by the Bus Processor software through the BP hardware latch, activated by switch S1, and is used during system diagnostics. The Data RAM Bus carries 57 operational signal lines as shown in table 2-3.

Table 2-3. Data Ram Bus

FUNCTION (No. of Lines)	MNEMONICS	OPERATION
DRAM Address Lines (16)	DA 0-15	BP/DAs to DRAM (Note 1)
DRAM Data Lines (16)	DD 0-15	Bidirectional (Note 2)
DRAM Request In (10)	DRI 0-9	BP/DAs to DRAM (Note 3)
DRAM Grant Strobe (10)	DGS 0-9	DRAM to BP/DAs (Note 3)
DRAM Control Bits (2)	DCB 0-1	BP or DAs to Data RAM
DRAM Status Bit (1)	DSB	DRAM to BP or DAs
DRAM Data Strobe (1)	DDS	DRAM to BP/DAs (Note 4)
DRAM Clock (20 MHz) (1)	DCK	DRAM to some DAs (Note 5)

NOTES

1. DRAM Address Line DA15 is not currently used by the DRAM and must always be zero.

2. Data RAM data lines are bidirectional between the DRAM and the BP, or Device Adapters.

3. There are thirteen DRI/DGS interrupts to the DRAM, ten external and three internal.

4. The DDS line notification is common to all DRAM requesters and must be inhibited by the requesters unless their specific DGS is active.

5. The DRAM Bus Clock is a buffered output from the System Clock (Phi S) on the Bus Processor board and must be used by all Device Adapters that require a 20 MHz clock signal.

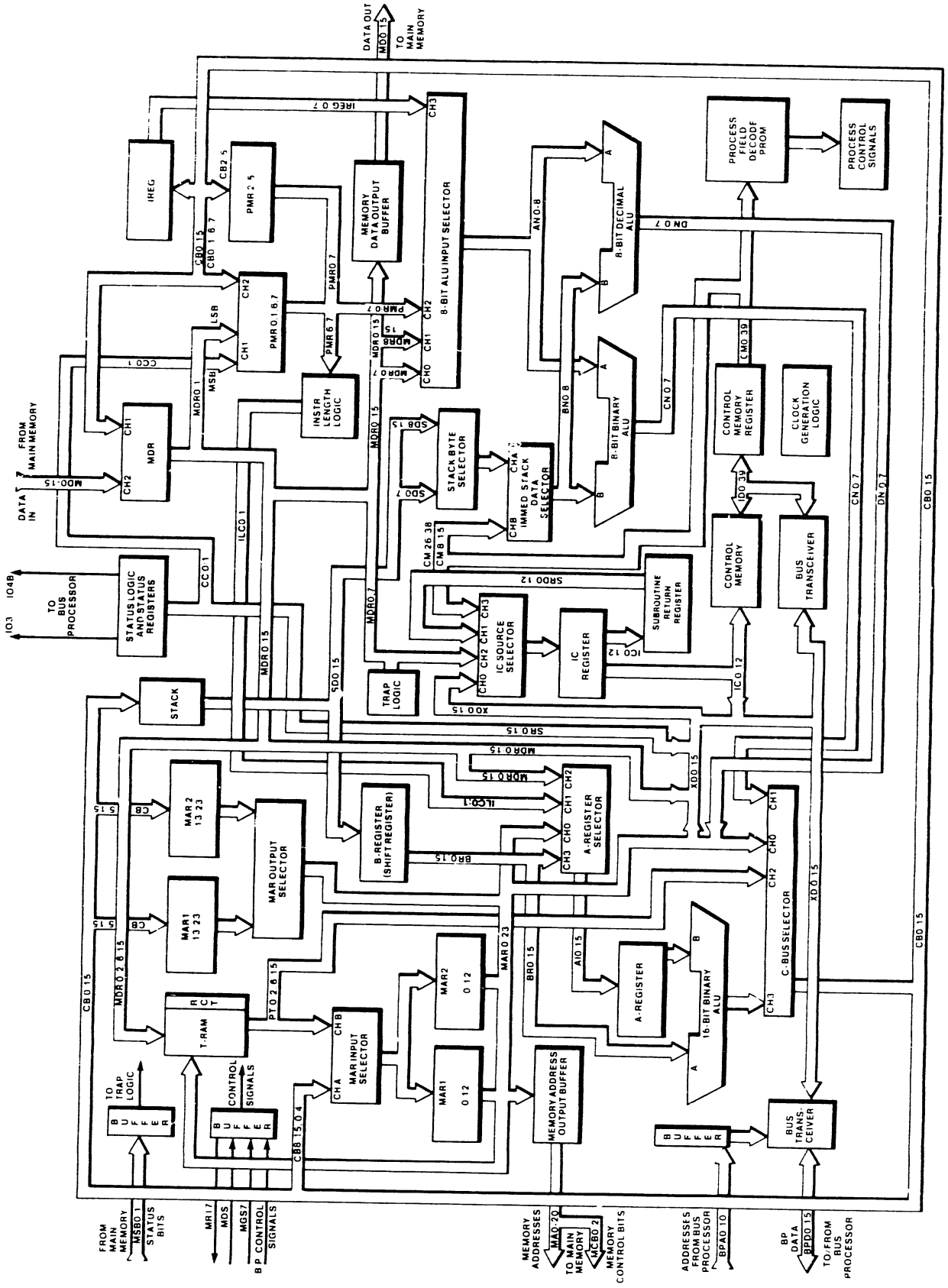

Figure 2-2. VS-25/45 CPU Block Diagram

2.2 VS-25/45 CENTRAL PROCESSOR

The CP5 Central Processor's primary task is to execute the VS-25/45 machine instruction set and to monitor the results of execution. (There are actually two instruction sets in the CP, the machine instruction set and the microinstruction set. Each machine instruction is a microcode routine stored in the CP's Control Memory.)

As can be seen in figure 2-2, the CP Block Diagram, the CP contains facilities for addressing physical main memory; fetching and storing information; arithmetic and logical processing of data; sequencing instructions in the desired order; and initiating communication between Main Memory and the external devices. The Central Processor is one board containing many standard and unique logical elements.

The VS-25/45 CP is microcode compatible with the VS-50/60/80. Existing VS-80 microcode can be run on the VS-25/45, with the exception of translation and input/output differences. The VS-25/45 supports over 8 megabytes of virtual memory address space and can access physical memory up to 1M byte, where 1M byte is defined as 1,048,576 bytes.

2.2.1 CP CONTROL MEMORY

The VS-25/45 Control Memory (CM), a loadable 8K-Word Random Access Memory, is part of the CP5 board. The CM features twenty 2K-byte (where 1K byte is defined as 1024 bytes) high speed RAM chips which stores all CP microinstructions. The CP Control Memory Word (CMW) is 5 bytes long (39 bits, plus one parity bit). The current microprogram contains approximately 6K-Words of microinstructions.

The Control Memory Word has the same fields as the VS-60/80, including: Microopcode Table, Stack-Operand Encoding, Process Field Encoding, Memory Field Encoding, and Branch Field Encoding. The CP Branch Field allows 13 bits (8K-byte possible locations) for Control Memory addressing.

The loadable Control Memory RAM permits CP microcode updates, microcode expansion, and the use of microlevel diagnostics. All system microcode is recorded on disk and is loaded into the Control Memory via the Bus Processor.

2.2.2 GENERAL CP/MAIN MEMORY (MM) OPERATIONS

Memory operations are write 8-bits (one byte), write 16-bits (two bytes), and read 16-bits (halfword). The CP can initiate only one memory read or write operation for each microinstruction. CP memory read or write requests rely on a physical address contained in a Memory Address Register (MAR) and data contained in a Memory Data Register (MDR). There are two MARs and one MDR. The memory operation field of the microinstruction selects a Memory Address Register and indicates the type of read/write operation or address ripple (incrementing or decrementing a MAR value) operation.

Main Memory Error Correction Code (ECC) testing takes place for each two-byte (halfword) operation or a write one-byte operation. ECC attempts to correct a single bit error within a halfword. A CP microtrap is taken for multi-bit parity errors within a halfword read operation, or for one-byte write operations.

2.2.2.1 Read And Write

The read operation uses the selected Memory Address Register contents at the start of the microinstruction. The CP must wait for the data to be returned before resuming microinstruction execution. Error returns for read operations are handled by parity error or invalid memory address (IMA) microtraps after the microinstruction has completed. When an IMA is encountered, the memory operation is not completed, that is, Main Memory is not altered.

The write operation uses the contents of the MDR and the contents of one of the MARs at the start of the microinstruction. The CP cannot continue program execution until it receives a 'memory operation complete'. Parity error returns for 1-byte write operations and invalid addresses are handled by the same microtrap as the halfword read operation.

2.2.2.2 Translation

When a translation operation changing virtual memory addresses into physical memory addresses is performed, memory read, write, and ripple operations are allowed after the physical address is formed. A Translation RAM (T-RAM), after translating the virtual address, supplies the physical addresses for the two Memory Address Registers. One bit of the microinstruction selects the MAR.

2.2.2.3 Ripple

The Memory Address Register ripple operation involves a small increment or decrement of the MAR value. Both Memory Address Registers support ripple operations. The ripple operation is specified by the ripple portion of the memory operation field format of the microinstruction. The ripple operation for the MARs only affects the low order bits of the MAR. The high order bits are never modified by the ripple operation. If a memory read or write operation is also requested, then the ripple occurs after the memory operation has been initiated. A ripple operation always involves a corresponding Page bit to indicate that the MAR address has or has not crossed a 2K-byte memory page boundary (page-break). A status bit is set if there is no carry-out and the status bit is reset if the ripple causes a carry-out from the MAR.

2.2.2.4 Memory Address Registers

The CP uses the two Memory Address Registers (MARs) in conjunction with the Memory Data Register. The MAR select bit of the microinstruction chooses either the first or the second MAR. The select bit is also used for translation operations that involve a MAR. The memory operation uses a 21-bit physical address from either of the 24-bit MARs.

One MAR bit controls a byte-swap function for a 16-bit read or write. (Two bytes of data can be logically swapped after data is read from memory or before data is written to memory.) An 8-bit write uses the full MAR address with the data taken from the high order byte of the Memory Data Register (MDR). A read-modify-write (RMW) can be performed at the memory controller for this one-byte write. (A RMW, a two-memory cycle operation, must read a halfword, replace a byte, and rewrite the halfword.) An invalid memory address trap is taken if the address exceeds the maximum memory size for either read or write operations. The trap is taken one microinstruction after the memory operation is completed.

From an operational viewpoint, each MAR may be divided into two sections. The low order bits of the MARs (bits 13-23) can be rippled +1, +2, or -1, but the high order address bits (0-12) are not modified by a ripple. A ripple sets or resets the PAGE status bit. MAR ripple operations are not allowed for any microinstruction that loads or stores either of the MARs.

The MARs are not available as Arithmetic Logic Unit (ALU) operands but MAR contents can be moved to and from a pair of registers with Transfer MAR and Transfer Stack Pair instructions.

The high order bits, MAR 3-12, are transferred to the memory address lines as MA 20-11 and the low order bits, MAR 13-23, as MA 10-0 due to the convention of the Intel 8086 microprocessor used on the Bus Processor board. The 8086 views the memory address lines as the reverse of the VS-25/45 CPU; that is, the most significant bit as the least significant bit. This is also true with the actual data as the 8086, during a memory access, sees the even byte as the odd byte and the odd byte as the even byte. Table 2-4 shows the inversion of the Memory Address Register bits to the Memory Address line values. (Refer to table 2-10, VS-25/45 Main Memory Addresses, for complete memory address values.)

Table 2-4. Memory Address Register Output Inversion

MAR BIT	MA LINE BIT
MAR 23	MA0
MAR 22	MA1
MAR 21	MA2
MAR 20	MA3
MAR 19	MA4
MAR 18	MA5
MAR 17	MA6
MAR 16	MA7
MAR 15	MA8
MAR 14	MA9
MAR 13	MA10
MAR 12	MA11
MAR 11	MA12
MAR 10	MA13
MAR 9	MA14
MAR 8	MA15
MAR 7	MA16
MAR 6	MA17
MAR 5	MA18
MAR 4	MA19
MAR 3	MA20

2.2.2.5 Main Memory Data

Data to and from Main Memory is transferred through the Memory Data Register (MDR). The MDR can be accessed as 2-byte halfwords and also as high and low order bytes of the halfword. High MDR bytes are used for all 8-bit Arithmetic Logical Unit operations.

Data to be written to Main Memory (MM) are transferred from the MDR via the Memory Data lines (MD0-15) on the Main Memory Bus and the CP waits for a 'memory operation complete'. Data from Main Memory is transferred by the Main Memory Controller into the MDR via the Main Memory Bus.

2.2.3 CP ADDRESS TRANSLATION

The physical main memory storage capacity of the VS-25/45 is 1M bytes. Because the VS-25/45 uses Virtual Memory techniques, Main Memory can be made to appear as large as 8M bytes. The translation of virtual addresses to physical (Main Memory) addresses is performed by the CP. Three elements recognized by the Operating System (the master control program) during translations are segments, pages, and page frames.

The current operating system defines three segments of up to 1M byte each. (A segment is required to be a block of contiguous disk storage.) The first, Segment 0, stores the supervisory routines and data for the Operating System. The second segment (Segment 1) is reserved for each user's program. Segment 2, the third type, can vary from 64K bytes to 1M byte (in 4K byte increments) for each user's data. A page is 2048 contiguous bytes (2K-bytes) of disk storage space within the user program or data segments, and a page frame is a Main Memory area exactly large enough to contain a disk page.

Since the system is intended to operate in a multitask, multiuser environment, it is necessary to have a mapping mechanism to direct the CP to the pages of the tasks being executed. The CP uses a 4K-bit by 13-bit local Translation RAM (T-RAM) to perform the mapping (translation) of a 24-bit virtual memory address (VA) into its current corresponding 24-bit physical main memory address. Each T-RAM entry, which can be loaded from the contents of the Memory Data Register, contains a page frame number, a fault bit, and read and write protect bits. These correspond to a particular page within the total virtual address space. The translation operation addresses the T-RAM entry using the virtual address.

The page frame number read from the T-RAM is loaded into a section of either of the MARs. The output of the MARs is concatenated with the low order bits of the virtual address (a location within the page) from another section of either of the MARs, to form a 24-bit physical Main Memory address. Only 21 bits are actually sent to Main Memory.

If the operation traps on an invalid virtual page address (page fault), the macroinstruction can be restarted and the T-RAM entry can be updated. A trap is also taken if the page is protected against being read or overwritten.

The CP maintains a table for each page frame entry in the T-RAM to record a Reference (R) bit, indicating a page was recently used, and a Change (C) bit, indicating the contents of a page were modified. A 1K-bit by 2-bit RAM is responsible for maintaining the Reference And Change Table (RCT). The R bits tell the Operating System which pages have not been used recently and may be written over with new pages. The C bits allows the Operating System to determine which pages have been modified and should be written back onto disk to make room in memory for new pages. These two R and C bits are updated to reflect the page frame status during each Memory Operation translation process. The translation operation addresses the T-RAM entry using the virtual address. Addressing the RCT is done by the MAR after it has been modified by the T-RAM

entry. An RCT physical address entry can be cleared or inspected by microinstructions.

2.2.4 CP STACK

The CP Stack, a local RAM storage area, is configured as 256 16-bit (halfword) registers. The Stack is divided into five functional areas as follows:

FILE REGISTERS:	Used as work registers by the CP microprogram. Also stores the microprogram constants created at initialization and supports ALU Level 1 operations.
SYSTEM REGISTERS:	Used to hold the outer-program Control Registers and Floating Point Registers, and to support ALU Level 2 operations.
AUXILIARY REGISTERS:	Used as work or spare registers and support only ALU Level 3 operations.
GENERAL REGISTERS:	Used to hold the outer-program General Registers and support ALU Level 2 operations.
WORK REGISTERS:	Used in relation to translation operations and support ALU Level 3 operations.

NOTES

1. The term "ALU Level" describes the types of ALU (Arithmetic Logical Unit) operations that can be performed on the Stack elements.

2. ALU Level 1 - All ALU operations are supported including binary and decimal arithmetic, logical, and shift operations for either 8-bit or 16-bit operands.

3. ALU Level 2 - Most ALU operations are supported but not the full set as described in Level 1. (i.e. 16-bit ALU processing functions and the 'generate base-displacement (BD) operation'.)

4. ALU Level 3 - Only move operations are directly supported.

The unit of retrieval from the Stack can be eight bits (1-byte) or 16 bits (2-byte halfword) increments. One Control Memory bit acts as a byte select and determines which half of the Stack is used. The Stack uses an 8-bit address.

2.2.5 CP MICROTRAPS

CP microtraps, interrupts to the CP microprogram, can occur due to process, memory, branch field operations, or external conditions. When a trap condition is detected, the CP hardware forces a branch to a specific Control Memory address. This address is determined by the type of trap and is used to

begin execution of a routine intended to take action in response to the condition causing the trap. All microtraps branch to locations in the Control Memory and the current microinstruction will finish before a trap is taken. Some examples of CP microtraps are Address Translation and Protection, Invalid Memory Address, Memory Parity Errors, and Pagespans.

The Address Translation trap indicates an address translation fault or that the virtual address is too large. The Protection trap indicates that the RAM used for translation operations is protected (from use by other than the 'owner') against reading or overwriting of a page. The memory operation error traps (address or parity errors) are traps that can occur during either read or write operations. These traps are taken one microinstruction after the operation is complete. A Pagespan trap indicates that a logical page boundary in Main Memory has been crossed. The following table lists the microtraps in descending priority:

Table 2-5. Command Processor Microtraps

TRAP ADDRESS	TRAP NAME	CONDITION
0001		Not Used
0002		Not Used
0003	TRAP03	Address Translation Trap (T-RAM Fault) (Set Status Register Bit S6).
0004	TRAP04	Protection Trap.
0005	INVA	Memory Trap (Invalid Physical Address).
0006	MPAR	Main Memory Parity Error (Bit S6 set = MAR in use on MPAR trap.
0007	TALIGN	Alignment Trap (BOP = TRP ALIGNx).
0008	TBI	Pagespan Trap (Page = 0 when BOP = BI).
0009	TCC	Trap for BOP = TRP CC/MASK.

2.2.6 CP STATUS REGISTER

The CP maintains a 16-bit Status Register whose content is set as a result of external conditions, CP arithmetic and logical operation results, and microprogram flags. The status bits indicate to the CP that an "event" has occurred. Status bits are accessed in 4-bit groups for conditional branching. Table 2-6 gives the eight CP Status Bits currently used by CP5.

2.2.7 GENERAL CP HARDWARE AND LOGIC

Included in the CP are many multipurpose hardware elements, a few of which are described below.

2.2.7.1 8-Bit Binary Arithmetic Logic Unit

The 8-bit Binary ALU (BALU) consists of two 4-bit high speed parallel arithmetic logic units cascaded for performing operations on one byte (8 bits) of data. Controlled by four function select inputs and a Mode control input, it can perform 16 possible logic operations or 16 different arithmetic operations. The Mode control input determines whether all internal carries are inhibited and the device performs logic operations (Or, Nor, Exclusive Or, And, Nand, or Compare) on the individual bits, or whether the carries are

enbled and the device performs arithmetic operations (Add, Subtract, Compare, or Double) on the two bytes.

2.2.7.2 8-Bit Decimal Arithmetic Logic Unit

The 8-bit Decimal ALU (DALU) consists of two 4-bit high speed binary coded decimal (BCD) arithmetic units cascaded to allow eight bits (one byte) of data to be acted on as a whole. Depending on the state of the Add/Subtract control, the unit produces the BCD sum or difference of two decimal numbers. A decimal addition (A plus B) is performed by adding two 8-bit fields. A decimal subtract operation (A minus B) is performed by nine's complement addition yielding the difference of two BCD numbers.

Table 2-6. Command Processor Status Bits

BIT	NAME	CONDITION
S0	CA	Carry Bit. Carry In/Out for Decimal/Binary Operations.
S1	-	(Spare)
S2	ALU 0	Or Non 0 result for 8/16 Bit Move or Arithmetic Operations.
S3	PAGE	Set/Reset when MAR Rippled. Carry-out of MAR13. (New Page)
S4	STATE	Protection Checking. Indicates System or User State.
S5	DEC	Set for Invalid Decimal digit found in A or B Bus Operand for Decimal Add/Subtract with Carry.
S6	MSEL	From Trap 0003/0006. MAR in use when Trap taken.
S7	-	(Spare)
S8	DEBUG	Required Microprogram convention; no hardware significance.
S9	CM	Control Mode. CP Control Mode button.
S10	IO3	Set by BP. BP has stored I/O Status Word in memory.
S11	TIM	Real-time-clock tick. Set from AC line frequency.
S12	OVF	Overflow from 2's compliment arithmetic. From Add with Carry or Subtract with Carry instructions.
S13	IO4	Receive bit IO4B when CIO 0 issued.
S14	TRCT	Reference Bit--Read/reset access to Reference & Change Table.
S15	TRCT	Change Bit--Read/reset access to Reference and Change Table.

2.2.7.3 16-Bit Binary Arithmetic Logic Unit

The 16-bit Binary ALU (BALU) consists of four 4-bit high speed parallel arithmetic logic units cascaded for performing operations on a halfword (16 bits) of data. Controlled by four function select inputs and a Mode Control input, it can perform 16 possible logic operations or 16 different arithmetic operations. The Mode Control input determines whether all internal carries are inhibited and the device performs logic operations (Or, Nor, Exclusive Or, And, Nand, or Compare) on the individual bits, or whether the carries are enabled and the device performs arithmetic operations (Add, Subtract, Compare, or Double) on the two halfwords (4 bytes).

2.2.7.4 Process Field Decoder

The Process Field Decoder stores control signals, in Programmable Read Only Memory (PROM), that are used internally by the CP. Depending on the process field of the microinstruction, each microinstruction is broken down into 2 or 3 nanoinstruction cycles. The PROMs are addressed by the process field, the signals are read out of the PROMs, and are distributed to various

CP hardware elements to direct the data and address flow of the instruction currently being executed.

2.2.7.5 Indirect Register

The Indirect Register, comprising two 4-bit up/down counters, is used as a general work register and for addressing entries within the CP Stack. The Indirect Register holds the second byte of each macroinstruction after decoding and allows indirect access to the Stack General Registers. The Indirect Register is loaded with A Bus and B Bus operands for 8-bit logical immediate operations.

2.2.7.6 Program Mask Register

The Program Mask register holds the Condition Code bits, the System Mask bits, and the Instruction Length Code bits. These three code fields are used by specialized microinstructions to support outer-level machine language. The Program Mask Register is a dedicated register and is part of the outer program Program Control Word (PCW). (The PCW is used to control instruction sequencing and to hold and indicate the status of the system in relation to the program currently being executed.) The Condition Code indicates the results of the majority of the machine arithmetic, logical, and Input/Output operations, while the System Mask is used to enable or disable various interrupts. The Instruction Length indicates the length of the current machine language instruction.

2.2.7.7 Microinstruction Counter (MIC) Source Selector

The MIC Source Selector has four channels used to select a source for the address of the next microopcode to be executed.

When Channel 0 is selected, the CP is halted and data to be written into Control Memory is transferred by the Bus Processor. The CP is halted during power-on initialization to allow the BP to load the system microcode. The CP is also halted by the BP to let the BP control the CP for diagnostic purposes.

Channel 1 is selected and the input is the contents of the Subroutine Return Register, the next microinstruction address, that will be used for a Conditional Subroutine Return.

Channel 2 is selected and the input is the contents of the Memory Data Register High, or four bits from the trap logic. If any trap is detected, the address of the trap is placed into the MIC Source Selector.

Channel 3 is selected and used when an Unconditional branch is executed and Control Memory bits are needed as a full branch address. Conditional branching can be done by partially loading the Microinstruction Counter.

2.2.7.8 Microinstruction Counter Register

The Microinstruction Counter Register (MIC), a series of four, 4-bit counters, is used as addressing for the Control Memory RAM. The MIC register contains the current address and is incremented by one to prepare the next address. The sequential incrementing of the Microinstruction Counter and the fetching of microinstructions continues unless interrupted by traps or branches.

2.2.7.9 Subroutine Return Register

The Subroutine Return Register consists of four 4x4 register files used for storing the subroutine return address from the Instruction Counter Register. It is counted down by a Conditional Subroutine Return Branch and counted up by an Unconditional Subroutine Branch where the current microaddress plus one is saved in the Subroutine Return Register. The branch is taken to the microaddress.

2.2.7.10 A-Register Source Selector, A-Register, and B-Register

The A Register Source Selector, A Register, and B Register (a shift register) are data selection and transfer paths for inputs to the 16-bit binary Arithmetic Logic Unit (ALU).

2.2.7.11 8-Bit ALU Input Selector, Stack Byte Selector, and Immediate/Stack Data Selector

These three elements are all data selection and transfer paths for inputs to the 8-bit binary and 8-bit decimal ALUs.

The 8-Bit ALU Input Selector has four channels to choose the Memory Data Register high or low byte, the Program Mask register, or the Indirect Register, for 8-bit logical operands with immediate data.

The 8-bit Stack Byte Selector selects the high or low order byte of Stack data for the 8-bit ALUs.

The 8-bit Immediate/Stack Data Selector chooses either the byte of data from the Stack Byte Selector or an 8-bit logical operand with immediate data from the Control Memory.

2.2.7.12 System Identification PROM

A self-supporting System Identification Number (SYSID) feature was designed into the CP hardware to prevent unauthorized use of software products (which may be sold separately). The SYSID was designed to contain two types of information, the System Number and Feature Mask.

The System Number is a machine readable serial number, and the Feature Mask is a bit mask indicating which WANG-supplied software is authorized for use on a given system.

The SYSID feature, however, which is to be stored in a PROM at location L228 on the CP board, has not been implemented to date.

2.3 VS-25/45 MAIN MEMORY

The VS-25/45 Main Memory (figure 2-3) is configured on one memory board (module) containing up to 512K halfwords (1M-byte), and is logically divided into eight rows of 64K halfwords per row. Main Memory (MM) uses a 64K-bit by 1-bit dynamic RAM chip (16 chips per row). The Main Memory board also decodes the memory operation, generates the internal memory control signals, decodes addresses, and generates error indications.

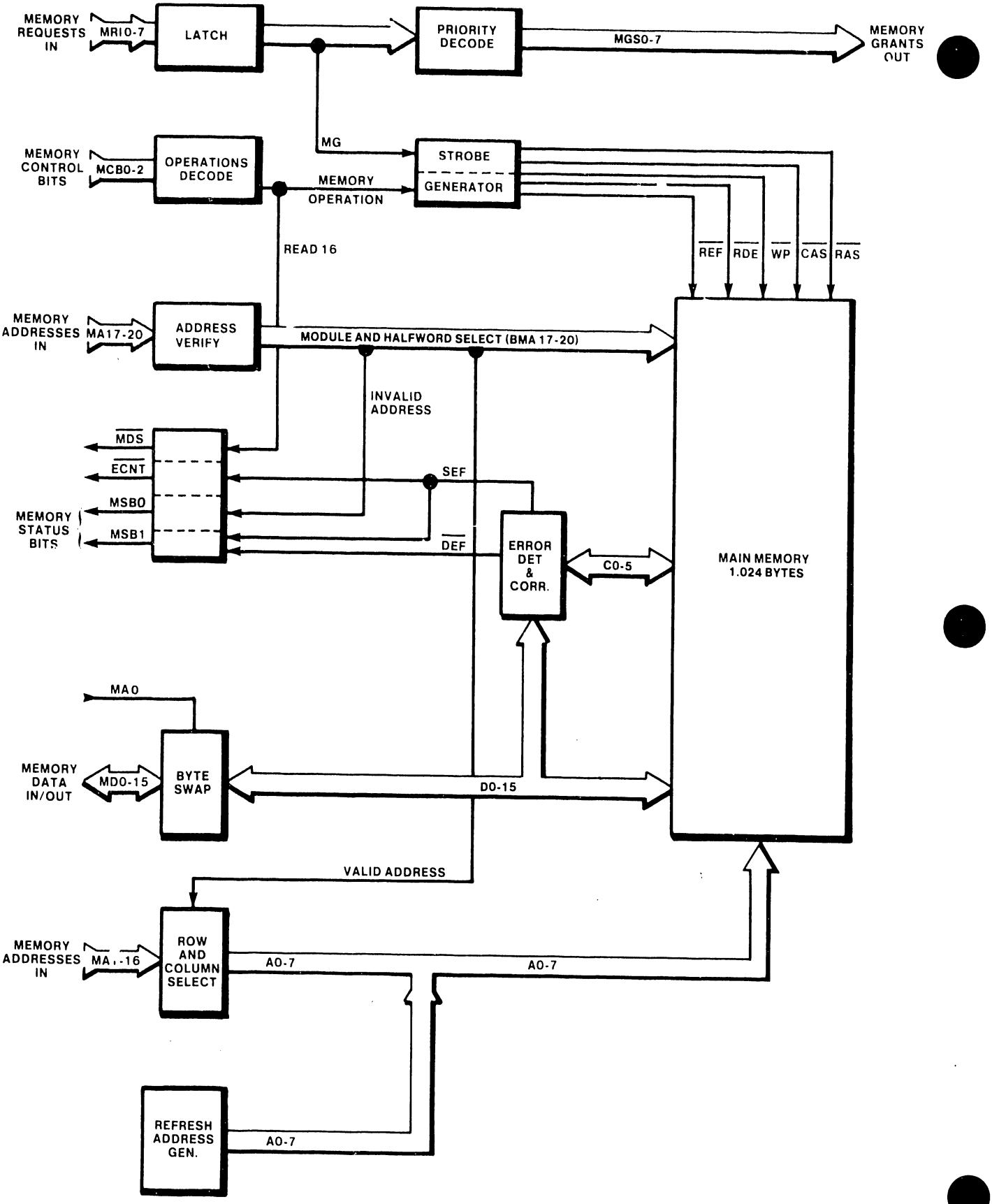

Figure 2-3. VS-25/45 Main Memory Block Diagram

2.3.1 MAIN MEMORY OPERATIONS

A requester acquires a bus cycle by raising its Memory Request In (MRI) signal. Main Memory acknowledges this signal by giving a Memory Grant Strobe (MGS) to the highest priority requester, which immediately enables its address and control buffers (and if doing a write, its data buffers) onto the Bus. Later in the cycle, if Main Memory needs to give the requester data, it will pulse the Memory Data Strobe (MDS) line. Each requester has a separate MRI and MGS line, but all have a common MDS line. The MDS line notification must be inhibited by the requesters except when their specific MGS is active.

There are several types of Main Memory operations including: write-8-bits (using either the high or low order byte of the halfword) which is known as a Read-Modify-Write (RMW), write-16-bits (2-bytes), and read-16-bits (halfword). However, the actual memory data word written, or read, is either 8-bits or 16-bits plus a 6-bit Error Correction Code field (ECC). Main Memory is written or read under software control using the MCB0-2 control bits.

The Main Memory cycle time is eight system cycles (400 nanoseconds) for a normal read or write, or 16 system cycles (800 ns) for an RMW or extended operation (MM read with a single bit error correction). A system cycle (system T-state) is defined by the 20 MHz System Clock (Y2) located on the Bus Processor board and is equal to 50 nanoseconds (50 ns).

2.3.2 MAIN MEMORY CONTROL AND STATUS

The Main Memory controller uses three externally generated Memory Control Bits (MCB0-2) supplied by the requester to control the request. These three bits are defined to give eight read or write functions during a Main Memory operation, four read/write with error correction and four without. The three MCB's are defined as follows:

Table 2-7. Main Memory Control Bits

MCB2	MCB1	MCB0	OPERATION
0	0	0	WRITE-8 from low byte bus without error correction.
0	0	1	READ-16 without error correction.
0	1	0	WRITE-16 without error correction.
0	1	1	WRITE-8 from high byte bus without error correction.
1	0	0	WRITE-8 from low byte bus with error correction.
1	0	1	READ-16 with error correction.
1	1	0	WRITE-16 with error correction.
1	1	1	WRITE-8 from high byte bus with error correction.

Error detection still works regardless of MCB2. After the operation is complete, the MM controller responds with two Memory Status Bits (MSB0-1) which signals the success of the operation to the requester.

There are three defined states of completion using MSB0-1 (as given in table 2-8): a successful operation; an Invalid (or nonexistent) Memory Address (IMA); and an error uncorrected by Error Correction Code (ECC). Single bit errors, corrected by the ECC circuitry, are only reported on the Error Count (ECNT) line and are not reported by MSB0-1.

Each single or double bit parity error is sent to a counter on the Bus Processor board using the ECNT line. When the error count reaches a predetermined value, an ECC interrupt is generated to indicate that a RAM chip on the Main Memory board is defective. Any double bit error will be reported using Memory Status Bits MSB0 and MSB1. Thus, error detection is accomplished on the MM board and signaled to the various requesters using the two Memory Status Bits and the ECNT line.

Table 2-8. Main Memory Status Bits

MSB1	MSB0	RESULTS
0	0	Sucessful operation.
0	1	Invalid (non-existent) Memory Address.
1	0	Uncorrected ECC error.
1	1	Undefined.

Internal Main Memory control signals, generated on the memory board, are initiated by any one of the nine possible requesters. These requests are prioritized with the highest priority being Main Memory refresh and the lowest priority being a CP Main Memory request. A list of Memory Request In (MRI) (and corresponding Memory Grant Strobe) priorities, with Main Memory Refresh given a priority level of zero, is given below.

Table 2-9. Main Memory Priority Interrupts

PRIORITY	I/O PORT	REQUESTOR
0	--	REFRESH (Note 1)
1	MRI 0	CMD/FMD/SMD (Note 2)
2	MRI 1	Quantum
3	MRI 2	Reserved
4	MRI 3	SIO/ISIO
5	MRI 4	Reserved
6	MRI 5	DRAM to MM DMA (Note 2)
7	MRI 6	Telecommunication
8	MRI 7	CP5 (Note 2)

NOTES

1. The REFRESH priority (0) has an internal control path (hardwired) and is not connected to the Main Memory Bus.

2. MRI/MSG priorities will vary with the system configuration. The order given above is the recommended order of priorities with three provisos; namely large disk drives will always have the highest priorities, BP must always be MRI/MGS 5, and the CP is always last (MRI/MGS 7).

The internal control signals generated are Row Address Strobe (RAS), Column

Address Strobe (CAS), Read Enable (RDE), Write Pulse (WP), Check Bit Write Pulse (CBWP), and Refresh (REF).

2.3.3 MAIN MEMORY ADDRESSING

Memory addresses are supplied by memory operation requesters. Of the 21 address bits available (MA0-20), eight bits (MA1-8) are used as row addresses and eight bits (MA9-16) are used as column addresses. The row and column addresses are received and divided by the Memory Address Input Multiplexer. Each of the eight rows of 128K bytes is selected by MA17-19, while MA20 is always zero (only one board allowed). MA0, the low order bit, is used to initiate a data byte-swap select within the 16-bit data halfword (high to low and low to high). The lowest addressable memory unit (MA1) is two bytes (16-bit halfword). Refer to table 2-10, Main Memory Addresses.

Table 2-10. Main Memory Addresses

MA BIT	MEMORY CAPACITY	COMMENTS
MA 20	1M Byte	(Must be Zero)
MA 19	512K Bytes	64K-Halfword Select
MA 18	256K Bytes	64K-Halfword Select
MA 17	128K Bytes	64K-Halfword Select
MA 16	64K Bytes	Column Address
MA 15	32K Bytes	Column Address
MA 14	16K Bytes	Column Address
MA 13	8K Bytes	Column Address
MA 12	4K Bytes	Column Address
MA 11	2K Bytes	Column Address
MA 10	1K Bytes	Column Address
MA 9	512 Bytes	Column Address
MA 8	256 Bytes	Row Address
MA 7	128 Bytes	Row Address
MA 6	64 Bytes	Row Address
MA 5	32 Bytes	Row Address
MA 4	16 Bytes	Row Address
MA 3	8 Bytes	Row Address
MA 2	4 Bytes	Row Address
MA 1	2 Bytes	Row Address
MA 0	-	Byte-swap Select

2.3.4 MAIN MEMORY WRITE

A Memory Request for a write results in a Memory Grant being returned to the requester while the memory controller generates an internal memory grant from the request. When the requester receives the Memory Grant, it replies by placing addresses MA0-20, data MD0-15, and control bits MCB0-2 on the respective busses. The type of write operation (8-bit or 16-bit) is decoded. The Row Address Strobe (RAS) is generated and the row addresses are selected from the Memory Address Input Multiplexer, followed by the Column Address Strobe (CAS) and the column addresses from the multiplexer. The address is checked for validity, and if the address is invalid, the appropriate response is taken by the CP.

The CP checks the validity of an address by comparing the address with the

switch settings on the Main Memory board. If the address exceeds the maximum memory size allowable, and if the CP was the requester, the Invalid Memory Address Trap is set in the CP. The trap is taken after the operation is completed. If the CP was not the originator of the request, the originator is notified of the invalid address.

The data is also available at the Data Input Multiplexer. It is now determined whether the entire 16-bit halfword will be written as it appears, if an 8-bit byte-swap will take place (where the low bus data is written to high byte memory and high byte data is written to low byte memory), or if a Read-Modify-Write (RMW) is required (where the high order or low order byte is selected and replaced within the halfword). (The RWM is actually a two cycle operation with the first cycle being the halfword read and the second cycle being the modified write.) The resulting halfword is latched and held for ECC generation. The ECC is generated by the Error Detection And Correction (EDAC) circuit and accompanies the data halfword as it is written to Main Memory. The parity RAMs are written at the same time as the data RAMs.

2.3.5 MAIN MEMORY READ

A Memory Request for a read (16-bit halfword only) also results in a Memory Grant being returned to the requester while the memory controller generates an internal memory grant from the request and again decodes the operation. When the requester receives the Memory Grant, it replies by placing addresses and controls on the bus. However, the requester does not place data on the bus, but instead is notified to expect data from the Main Memory by MM raising its Memory Data Strobe (MDS). The RAS is generated and the row addresses are selected, followed by the CAS and column addresses. The address is again checked for validity, and if the address is invalid, the appropriate response is taken by the CP.

The write logic is now inactive allowing data to be read from the RAMs. The data is checked and corrected, if necessary, (refer to paragraph 2.3.6, Error Detection And Correction) and sent to the Memory Data Output Drivers where the high and low order bytes can be swapped. As the requester has been alerted to expect data to its Memory Data Register, the drivers are enabled and the data is placed on the bus.

2.3.6 MAIN MEMORY ERROR DETECTION AND CORRECTION

Error detection and correction is done by using a unique Error Detection And Correction (EDAC) integrated circuit. For a memory write cycle, this IC generates a 6-bit ECC field from the incoming data halfword that is to be written to memory. During a read cycle, the IC detects and corrects single bit errors in either the 16-bit memory data field or the 6-bit ECC field. Any single bit error will cause the memory cycle to be extended, the data in error will be retained, corrected, and rewritten to memory. Corrected single bit errors are not indicated to the requester, however, they are transferred to the BP (via the ECNT line on the Main Memory Bus) for recording in the system error log.

Double bit errors are detected by the EDAC, but are not corrected. These two bit errors can occur in either the data or ECC field, or as a single bit error in each field during the same memory operation. If the CP was the requester, the dual bit errors set the Main Memory Parity Error Trap. Any

other requester is also notified of the error. EDAC can be enabled or disabled by the appropriate request for memory operation instruction.

2.3.7 MAIN MEMORY REFRESH

Because a dynamic RAM cannot store data indefinitely, the data must be rewritten at least once every 2 milliseconds. Rewriting the RAM is done internally and is called 'refresh'. This operation has priority over all other memory operations. The VS-25/45 does a Main Memory refresh every 12.5 microseconds.

When a refresh cycle is initiated, the Row Address Strobe (RAS) is enabled for all RAMs, as they require refresh with RAS only cycles. Row refresh addresses are supplied by a counter on the memory board. Memory Requests are inhibited while the refresh counter is counting. Normal memory operations also accomplish refresh but do not affect the normal refresh timing.

2.4 VS-25/45 INPUT/OUTPUT SECTION

The VS-25/45 Input/Output (I/O) section serves as the interface between the peripheral devices and the VS-25/45 CPU. The I/O section consists of the Bus Processor board and up to six device adapter boards.

The Bus Processor board supports three major functional areas: The Bus Processor circuitry, the Floppy Diskette Controller, and the Remote Diagnostic Telecommunication Channel.

Since the BP channels all communications between the CP and the Device Adapters, and in certain cases also routes Direct Memory Access (DMA) to Main Memory, it is the key to all I/O operations.

2.4.1 BUS PROCESSOR

The Bus Processor board , with it's 16-bit 8086 microprocessor, has control of the VS-25/45 I/O section. (See figure 2-4 on page 2-23.) Only one BP board can be installed in the VS-25/45. The 8086 microprocessor executes the BP microcode which allows the BP to communicate with the VS-25/45 CPU and to control the Device Adaptors.

The BP circuitry may be divided into three operational areas: The 8086 microprocessor and related control circuitry; the Data RAM (DRAM) and it's control circuitry; and the BP controlled Direct Memory Access (DMA) channel. The 8086 microprocessor has control of the Bus Processor DMA channel to the Main Memory. However, access to (and subsequent control of) the BP DMA channel is limited to an indirect path via the DRAM.

2.4.1.1 BP Microprocessor Control Circuit

The BP microprocessor (8086) has two internally connected operational areas. The first, the Execution Unit (EU), which contains the data registers and the arithmetic-logic unit, performs the basic processing functions. The second, the Bus Interface Unit, prefetches and queues instructions before they are required by the EU, and provides functions related to operand fetch and store, address relocation, and bus control, all in parallel with EU processing.

2.4.1.1.1 BP Control Memory (PROM)

The 4K halfword (8K byte) Bus Processor Programmable Read Only Memory (PROM) contains microcode instructions needed to do initial diagnostic checking, Initial Program Loading (IPL), and to bootstrap the necessary microcode and diagnostic code from the IPL device (Floppy Diskette, System Disk, or external disk drive).

2.4.1.1.2 BP Code RAM (CRAM)

The BP Code Random Access Memory (CRAM), which includes the 8086 stack and work area, is used to store the BP microcode loaded from the IPL device. Two versions of the Bus Processor board are presently in the field: an earlier version which has 128K bytes of Code RAM, and the most resent version which has been expanded to 256K bytes of CRAM.

The BP Code RAM is refreshed by the CRAM Controller at 15 microsecond intervals. The Controller generates a refresh cycle with each 30 clock ticks received from the Program Interrupt Timer (PIT1-0). (See paragraph 2.4.1.1.7 for information on the Program Interrupt Timers.)

2.4.1.1.3 BP Addressing

The Bus Processor Addressing scheme requires related functions to be consistent throughout the VS-25/45 system. Whichever Device Adapter has an I/O address of 01xx HEX, will also have a Data RAM Request of zero (DRI 0), a DRAM Grant Strobe of zero (DGS 0), a Memory Request of zero (MRI 0), a Memory Grant of zero (MGS 0), and BP (External 8086) Interrupts of 0-2 (BPINT 0-2). (See table 2-11 on page 2-25 for complete Bus Processor address space priorities.)

The priority scheme insures that the DRAM-to-MM DMA has a higher priority (MRI 5) than the last Device Adapter (usually the TC DA). However, the TC-to-DRAM Request (DRI 5) has a higher priority than the 8086-to-DRAM (DRI 5.3), the MM DMA-to-DRAM (DRI 5.5), or the LSI DMA-to-DRAM (DRI 5.7) requests.

Any Device Adapter which uses I/O address 03xx through 06xx may have two DRI/DGS's. For example, an 'Intelligent' DA may have a higher priority for the device interface and a lower priority for the processor resident on the DA board. Since there are ten DRI's/DGS's available on the bus, only four out of the possible six DA's may have two requests (two DRI's/DGS's) each.

Each Device Adapter's I/O Address, DRI/DGS, MRI/MGS, and BPINT lines are jumper controlled and should be verified by the Customer Engineer during installation of any new Device Adapter. (Refer to Chapter 5.) These interrupts and priorities will vary with the system configuration. The order given in table 2-11 is the recommended order of priorities with three provisos: large disk drives will always have the highest priorities; the BP is always MRI/MGS 5; and the CP is always last (MRI/MGS 7).

The Bus Processor does an I/O Read of the first address of each Device Adapter during the power-up sequence (eg: 100, 200, etc.). The BP fetches an eight bit value which is the identification of the Device Adapter type. The BP decodes the eight bit value to determine which type of DA is at that address. It then stores this information in it's Code RAM for use by the microcode (either diagnostic or operational). The Device Adapter identification for each board type is given in table 2-12 on page 2-25.

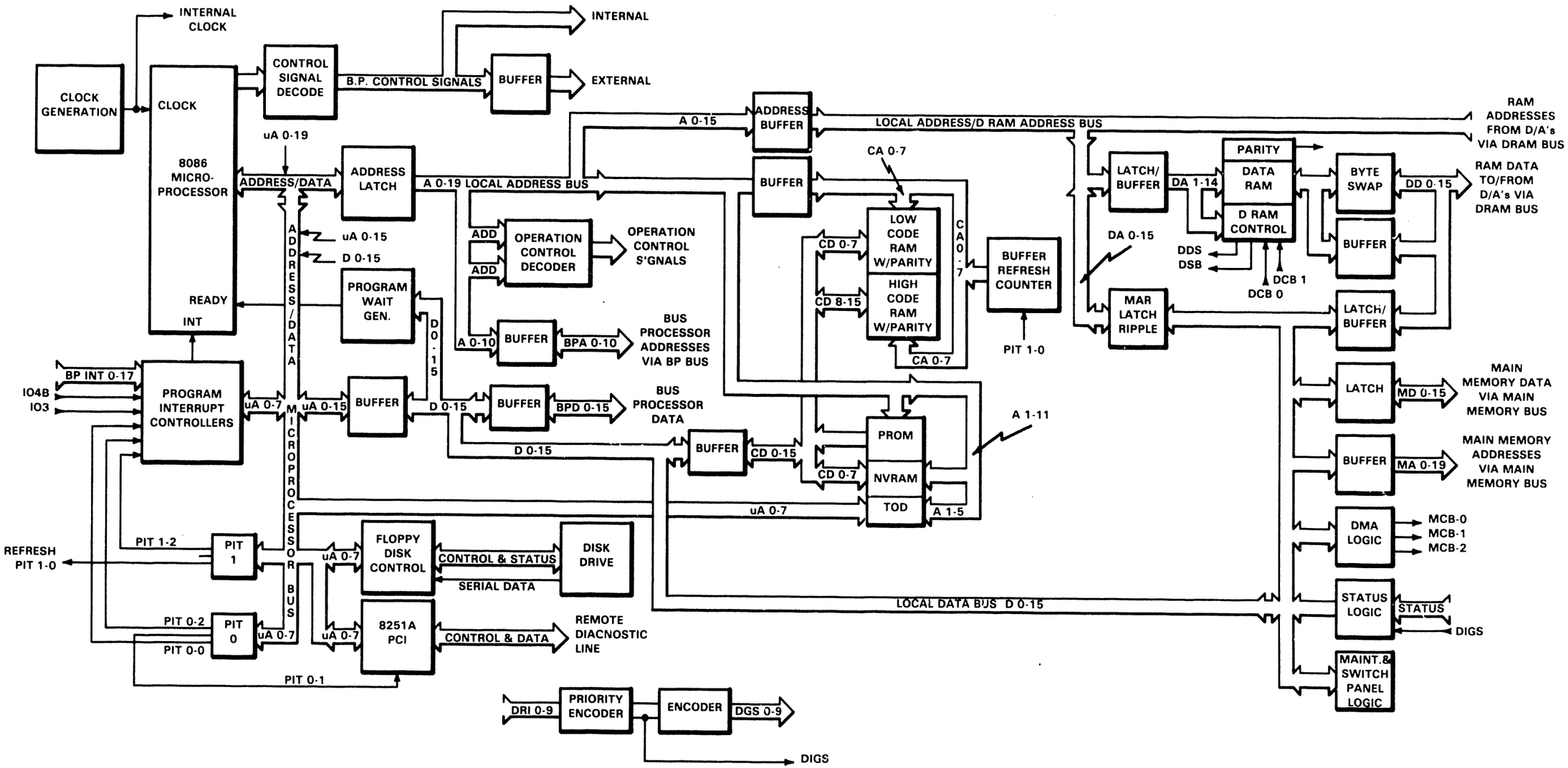

Figure 2-4. VS-25/45 Bus Processor Block Diagram

Table 2-11. Bus Processor Address Space Priority Interrupts

PRIORITY NUMBER	I/O ADDRESS	DRI/DRG NO. 1	DRI/DRG NO. 2	MM INTRS. MRI/MGS	BP INT.	BOARD or FUNCTION
1	01xx	0	-	0	0 - 2	CMD/FMD/SMD
2	02xx	1	-	1	3 - 5	Quantum
3	03xx	2	-	2	6 - 8	(Reserved)
4	04xx	3	-	3	9 - 11	SIO or ISIO
5	05xx	4	-	4	12 - 14	(Reserved)
6	06xx	5	-	6	15 - 17	TC
7	00xx	5.3	-	-	(See note)	8086 - DRAM
8	00xx	5.5	-	5	(See note)	MM DMA - DRAM
9	00xx	5.7	-	-	(See note)	LSI DMA - DRAM
10	03xx	-	6	2	6 - 8	(Reserved)
11	04xx	-	7	3	9 - 11	(SIO or ISIO)
12	05xx	-	8	4	12 - 14	(Reserved)
13	06xx	-	9	6	15 - 17	(TC)
14	07xx	-	-	7	-	CP5

Table 2-12. Device Adapter Identification

8 BIT VALUE D7 D0	DEVICE ADAPTER (BOARD TYPE)
0000 0000	SIO Data Link
0010 0100	Quantum 1
0010 0101	Quantum 2
0010 1000	CMD/FMD/SMD - 1 Port
0010 1001	CMD/FMD/SMD - 2 Port
0010 1010	CMD/FMD/SMD - 3 Port
0010 1011	CMD/FMD/SMD - 4 Port
1000 0000	ISIO Data Link
1000 0100	2200 Data Link
1000 1000	Wang Net Data Link
1001 0000	TC-1 Board No. 1 - 1 Port
1001 0001	TC-2 Board No. 1 - 2 Port
1001 0010	TC-1 Board No. 2 - 1 Port
1001 0011	TC-2 Board No. 2 - 2 Port
1110 0000	Cable Interface Unit (Inboard)

NOTES

1. D7 = x Type of Device Adapter.

   = 0 DA without microprocessor.
   = 1 DA with microprocessor.

2. D6-D5 = xx Type of board.

   = 00 SIO, ISIO, 2200, TC, etc.
   = 01 Disk.
   = 10 Reserved.
   = 11 Network, Processor.

NOTES

3. D4-D2 = xxx Particular board within a type.

   = 000 14" Disk Drive (Obsolete)
   = 001 Quantum Disk Drive.
   = 010 Large Disk Drive (SMD).

4. D1-D0 = xx Number of ports.

   = 00 CMD/FMD/SMD Disk with 1 port.
   = 01 CMD/FMD/SMD Disk with 2 port.
   = 10 CMD/FMD/SMD Disk with 3 port.
   = 11 CMD/FMD/SMD Disk with 4 port.

There are two sets of address space as seen by the 8086 microprocessor. The 8086 can access up to 1M byte of memory address space, and up to 64K bytes of I/O address space. The 1M byte of address space may be accessed in half-word (two-byte), high order byte, or low order byte increments and is allocated as follows:

Table 2-13. 8086 Microprocessor Memory Address Allocation

OPERATIONAL AREA	ADDRESS RANGE	COMMENTS
Code RAM	000 to 256K bytes	256K bytes
Data RAM	256 to 288K bytes	32K bytes
(Must not be used)	288 to 512K bytes	(224K bytes)
NVRAM	512 to 516K bytes	2K bytes, low byte only
(Must not be used)	516 to 768K bytes	(256K bytes)
(Must not be used)	768 to 1016K bytes	(248K bytes)
BP Cntrl Memry (PROM)	1016 to 1024K bytes	4K halfwords

The first 400 HEX bytes of CRAM are assigned as interrupt vectors as follows:

Table 2-14. Bus Processor Interrupt Vectors

ALLOCATED CRAM ADDRESSES	FUNCTION/COMMENTS
000 to 07F HEX bytes	Special Interrupt Vectors
080 to 3FF HEX bytes	I/O Interrupt Vectors

The 8086 uses I/O opcodes in order to access the 64K bytes of I/O address area. The I/O address space is allocated on a space available basis (for the various functions or Device Adapters) as given in table 2-15.

2.4.1.1.4 BP RAM Parity

Both the BP's Code RAM and the Data RAM have parity. Power-up diagnostics are allowed to test the parity generating and checking logic of each.

If a CRAM parity error occurs during microcode execution, the system halts and must be reinitialized. The Data RAM has its own parity generation and checking circuit which is discussed in paragraph 2.4.1.2.2.

Table 2-15. Bus Processor I/O Address Allocation

FUNCTION	ADDRESS (HEX)	COMMENTS
BP Control	00xx	BP I/O
Intel 8086	00Fx	Reserved by Intel
Device Adapter	01xx	CMD/FMD/SMD
Device Adapter	02xx	Quantum
Device Adapter	03xx	Reserved
Device Adapter	04xx	SIO/ISIO
Device Adapter	05xx	Reserved
Device Adapter	06xx	Telecommunications
CP5	07xx	CP diagnostic I/O

NOTES

1. Address lines A0 and A11 through A15 must always be zero but are not checked by hardware.

2. Address locations 0800 through FFFF are not allocated and must not be used.

2.4.1.1.5 BP Status Register

The BP (8086) maintains a 16-bit Status Register whose content is set as a result of initialize and reset buttons, error conditions, and interrupts. The status bits indicate to the BP that an "event" has occurred. Table 2-16 includes all BP status bits.

Table 2-16. Bus Processor Status Bits

BIT	NAME	CONDITION
D0	IO3	IO3 is set.
D1	IO4B	IO4B is set.
D2	BP-CMODE	Control Mode button pressed since latch was last cleared.
D3	HARD/SOFT	Soft sector disk in floppy disk drive.
D4	MM-MSB0	IMA. Invalid memory address accessed during MM DMA.
D5	MM-MSB1	ECC. Parity error occurred during Main Memory DMA.
D6	MM-DSB	ECC. Failure encountered during MM DMA access of DRAM. Status bit cleared by 'Clear-MM-DMA Status' command.
D7	BP-DSB	ECC. Failure encountered during BP/Fioppy access of DRAM. Status bit cleared by 'Clear-DRAM Status' command.
D8	D1A0	DRAM DRI Encoder # 1 A0 output.
D9	D1A1	DRAM DRI Encoder # 1 A1 output.
D10	D1A2	DRAM DRI Encoder # 1 A2 output.
D11	D1GS	DRAM DRI Encoder # 1 GS output.
D12	D2A0	DRAM DRI Encoder # 2 A0 output.
D13	D2A1	DRAM DRI Encoder # 2 A1 output.
D14	D2A2	DRAM DRI Encoder # 2 A2 output.
D15	D2E0	DRAM DRI Encoder # 2 E0 output.

2.4.1.1.6 BP Clock Generation Circuitry

The Bus Processor board has four crystal controlled clock generating circuits which supply the appropriate timing pulses throughout the system.

Crystal Y1 produces a 24 MHz (50 percent duty cycle) clock frequency used to generate the timing pulses required by the 8086 microprocessor on the Bus Processor board. Its frequency is divided down to an 8 MHz (33 percent duty cycle) clock frequency which is used to control the 8086's operational functions.

Crystal Y1A generates a 32.768 MHz output frequency used to drive the Time-of-Day (TOD) chip. The Date/Time Clock function was to be utilized by the Customer and the Operating System to maintain TOD information during power-down and/or power failures. (Refer to paragraphs 2.4.1.1.9 and 2.4.1.1.10)

Crystal Y2 generates the VS-25/45 System Clock frequency of 20 MHz. It supplies the necessary timing for the CP5 and Main Memory boards via the Mother board, as well as the Data RAM on the BP board. It is also available (as the buffered output DCK) for the use of the Device Adapters via the Motherboard and the DRAM Bus.

The 20 MHz clock may be modified under software control (Refer to paragraph 2.4.1.1.16). The modified clock frequencies are +10% (22 MHz) for FAST clock, -10% (18 MHz) for SLOW clock, or disabled for NO clock. (Turning the system clock off [NO clock] also turns off the REFRESH to CRAM.) These three clock functions are used for system diagnotics and are disabled during normal operation (Refer to paragraph 2.4.1.1.15).

The 8 MHz clock (Y3) generates the timing pulses required by the Floppy Diskette Controller (FDC) circuits and is used to generate a 4 MHz output for the LSI-DMA channel, and a 2 MHz frequency for the Programmable Interrupt Timers (PIT0-1).

2.4.1.1.7 BP Programmable Interrupt Timers (PITs)

The BP has two 3-channel Programmable Interval Timers (PIT's) to generate six timing functions. The two chips are referred to as PIT0 and PIT1. Only five of the channels are currently in use with each channel's function as follows:

PIT0	CHANNEL 0 -	Counts a 2 MHz clock for BP software timing .
	CHANNEL 1 -	Counts a 2 MHz clock to generate the baud rate for the 8251A Remote Diagnostics PCI (USART).
	CHANNEL 2 -	Counts the soft ECC errors in Main Memory.
PIT1	CHANNEL 0 -	Counts a 2 MHz clock for BP CRAM refresh timing.
	CHANNEL 1 -	Not Used.
	CHANNEL 2 -	Counts a 2 MHz clock for BP software timing.

2.4.1.1.8 BP Battery Backup

The VS-25/45 Bus Processor has two functions which are supplied with a battery backup; the Time-of-Day Clock (TOD) counter chip, and the Nonvolatile RAM (NVRAM) memory chip.

A 3.6V Lithium battery (BT1) supplies Battery backup to the TOD and NVRAM chips (See figure 5-6). During power-on, a special regulator circuit, VR1, supplies a constant voltage to the two chips to eliminate any current flow from the battery. Whenever there is a power loss, either momentary or long term (e.g. after power-down) the battery backup circuit supplies sufficient power to maintain the NVRAM and TOD information.

The Lithium Battery has an estimated life of 18 months to 2 years in the backup mode. It is not a field replaceable component, and consequently, battery replacement will require the contents of the NVRAM to be copied to a disk file, a complete Bus Processor board swap, and the reloading of the replacement board's NVRAM.

2.4.1.1.9 BP Time-of-Day (TOD) Clock

A real time function was designed to supply accurate date/time information to the system, and, for the convenience of the Customer, the Time-of-Day function. Currently, however, the necessary software has not been implemented to allow use of the hardware functionality.

2.4.1.1.10 BP Nonvolatile RAM (NVRAM)

The Bus Processor contains a memory area called a Nonvolatile Random Access Memory (NVRAM). The NVRAM is 2K-bytes (low byte only) in size. It is physically located on the BP board and is logically located within the BP's memory address space.

The NVRAM stores the customer identification, service location, system serial number, and customer service contract information. System hardware and software configuration, including system device adapters (with device addresses, serial numbers, and ECO levels), and authorized Wang-supplied software packages, are maintained. Finally, a log of the twelve most recent service calls including SRN's, repair and subunit codes, are stored in the NVRAM. The battery power supply ensures the NVRAM retains this information even when the system is powered off.

The NVRAM can be read and written on-site by the Customer Engineer. It does not store any information initially and must be loaded by the CE during system installation. From that point on, the NVRAM information can be displayed and updated during each service call using the NVRAM Utility Programs. Modification of the NVRAM with the addition of hardware and/or software packages purchased later is easily accomplished via the NVRAM Utility Programs.

2.4.1.1.11 BP Display

The BP has four hexidecimal LEDs, located on the front panel. The display provides the user (and the C.E.) with pertinent information concerning the operating condition of the VS-25/45. The LED's are blanked (not lighted) when the system is operating normally, except during power-up diagnostics. During the power-up diagnostic mode, the LED's display various codes indicating the interim diagnostic status and will normally change every three to four seconds (except when waiting for access to a disk and the disk is not ready).

The Front Panel HEX display is arranged in two rows of two displays each and are accessed two at a time by the BP. The lower two LED's are always zero

unless an error is being displayed, or the LED's are in the initial counting sequence. If at any time, the lower two are non-zero then the LED'd are displaying a current, valid error. The system will halt at the displayed error code message until reinitialized, or until it receives some other external input.

2.4.1.1.12 BP Initialization

At initialization time, the BP must check both its Code RAM and its Data RAM. Then it must check the IPL device interface with a known data pattern. Once this is done, the BP can then load its microcode into the DRAM, move the microcode to CRAM, and branch to execute the microcode. In this way the BP knows that the RAMs are reliable before executing the microcode. The BP must also load its Wait State Generator and check it using the PIT that is counting the 2 MHZ clock, to ensure that the Wait State Generator is operating correctly (generating the correct number of wait states).

2.4.1.1.13 BP Interrupts

Interrupts, a request-for-assistance condition, can be passed back and forth between the BP and the CP. VS-25/45 BP/CP communication is governed by two status bits; IO3 and IO4B. These bits allow a number of functions to be controlled by the BP and/or CP while indicating the current state of each processor's tasks. Interrupts are also generated by the Device Adapters, Main Memory DMA, Floppy Diskette Controller and LSI DMA, certain PIT channels, and other CP and BP requesters.

2.4.1.1.13.1 BP/CP Interrupts

The IO4B bit provides a interlock to insure that the CP does not overwrite the current command before the BP can read it. The CP uses a redefined Control I/O (CIO) instruction to move the IO4B bit from the BP to the IO4 bit in the CP's Status Register so the bit can be tested. If IO4B = 1, the BP is ready to accept another command; if IO4B = 0, the BP has not yet accepted the last command. The CP can clear IO4B bit by a modified CIO instruction causing the BP to trap. The BP can set the IO4B bit in the CP Status Register, thus telling the CP that it can send the next command to the BP.

The IO3 bit provides a flag to let the BP know when the current I/O Interrupt has been accepted by the CP. The BP can read the IO3 bit in the CP Status Register. It can also receive an interrupt when IO3 is cleared by the CP, indicating that the I/O interrupt has been accepted by the CP. The BP can set the CP IO3 Status Bit to tell the CP that there is an interrupt pending.

2.4.1.1.13.2 Additional BP Interrupts

The BP has 40 possible interrupts, 22 of which are external. The first four, which are dedicated to the master Programmable Interrupt Controller (PIC), can not be used and are masked off. The next four are also routed to the master PIC and are dedicated to four slave PICs as noted in table 2-17 below. These four PICs service four groups of eight interrupts each in a descending order of priority.

All of these interrupts can be masked as a whole by an 8086 internal status bit, and individually, by means of a mask register in each of the PICs. The highest priority interrupts are for Device Adapters and the lowest priority interrupts are for the Programmable Interval Timers.

Table 2-17. Bus Processor Interrupts

PRIORITY	INTERRUPT	DEVICE ADAPTER/USE/COMMENTS
0	(Unused)	Must be masked off.
1	(Unused)	Must be masked off.
2	(Unused)	Must be masked off.
3	(Unused)	Must be masked off.
4	H/W slot	Dedicated to second 8259A.
5	H/W slot	Dedicated to third 8259A.
6	H/W slot	Dedicated to fourth 8259A.
7	H/W slot	Dedicated to fifth 8259A.
8	BP INT 0	CMD/FMD/SMD
9	BP INT 1	CMD/FMD/SMD
10	BP INT 2	CMD/FMD/SMD
11	BP INT 3	Quantum
12	BP INT 4	Quantum
13	BP INT 5	Quantum
14	BP INT 6	(Reserved)
15	BP INT 7	(Reserved)
16	BP INT 8	(Reserved)
17	BP INT 9	SIO/ISIO
18	BP INT 10	SIO/ISIO
19	BP INT 11	SIO/ISIO
20	BP INT 12	(Reserved)
21	BP INT 13	(Reserve)
22	BP INT 14	(Reserved)
23	BP INT 15	Telecommunications
24	BP INT 16	Telecommunications
25	BP INT 17	Telecommunications
26	BP DSB	8086-DMA access to DRAM parity error.
27	DMA-DSB	FDC-DMA access to DRAM parity error.
28	-	(Spare)
29	-	(Spare)
30	CP HALT	CP notifies BP that CP has halted.
31	BP PE INT	Parity error during diagnostic operation.
32	IO4B	IOCW to be read by BP (IO4B low).
33	MM-DMA-INT	Error or terminal count completion.
34	IO3	IOSW to be read by CP (IO3 low).
35	FDC INT	Operation complete or error generated.
36	CP SYNC	Pulse generated when the address in the CP's MIC equals the address in the Comparator Latch.
37	PITO-0	Counts 2 MHz clock for BP S/W timing.
38	PIT1-2	Counts 2 MHz clock for BP S/W timing.
39	PITO-2	Counts single bit (soft) errors in MM.

Each Device Adapter has access to six sets of three consecutive interupts. Each of the three interrupts can be jumpered to one of six interrupt lines on a three boundary (i.e. 0-2, 3-5, 6-8, etc. with the highest priority interrupt depending on the I/O address). The DA's interrupts can be modified for each system configuration. A list of the various interrupts is given in table 2-17.

2.4.1.1.14 BP Wait States

The BP, at initialization time, uses six wait states per cycle, regardless

of the cycle. After initialization, the BP loads the Wait State Latch with the one's compliment minus one of the number of wait states needed for each type of operation. For example: six wait states (binary 110) has a one's compliment of 001. Subtracting one from the value 001 gives 000, the value loaded into the Wait State Latch. By this method, binary 111 is not allowed.

2.4.1.1.15 BP Diagnostic Capabilities

The Bus Processor has primary system control during loading and diagnostic operations over virtually all major system areas. The CP, Main Memory, all subsystems on the BP board (TC, FDC, etc.), all device adapters, and any function which has a path to the DRAM may be accessed. This allows for a large number of stand-alone diagnostics. (Diagnostics without using either the CP or MM.) Once system diagnostics have been successfully completed, the BP releases control of the system to the CP.

The BP has total diagnostic control over the CP. This includes reading and writing Control Memory; stopping, starting and/or stepping the CP; changing the clock speed; reading and writing the Microinstruction Counter (MIC); setting a comparator stop; reading various registers; and giving scope Sync pulses for (to) the appropriate MIC address. BP I/O control signals are used to load the MIC, Control Memory, and to Read/Write various registers. In general, the BP has all of the capabilities of the 'Hardware Tester'. When in diagnostic mode, the BP can:

1. READ OR WRITE CONTROL MEMORY:

   a. Halt the CP by an I/O instruction. (CPHALT exists as a HALT CIO which is under the control of the BP. The BP can stop and/or start the CP as required.)
   b. If required, Read the MIC in order to Restore it to its original value after performing the operation.
   c. Load the MIC with the Address that the BP will Read or Write.
   d. Read or Write the Control Memory using 16-bit I/O commands with two bits of the I/O address stating which 16 bits (out of the 40-bit control word) is to be Read or Written.
   e. Reload the MIC and repeat step 'd.' until all 16-bit 'halfwords' that are to be Read or Written have been completed.
   f. Restore the MIC to its original value, as required by step b.

2. STOP OR STEP THE CP:

   Use one of three Out commands to change the CP from Run Mode to Step (Halt) Mode (or vice versa) while a third Out command can give the CP a Step pulse.

3. CHANGE THE CP CLOCK SPEED:

   Use one Out command to control the CP clock speed. The commands are: Normal, Slow, Fast, and No Clock and are set through the BP's hardware latch. (Refer to paragraph 2.4.1.1.16).

4. READ OR WRITE VARIOUS REGISTERS:

   Read or Write the MIC, and any other register, with either an In or an Out instruction when the CP is halted. (See I/O addressing for exact addresses.)

5. SET A COMPARATOR ADDRESS:

   Set a Comparator address in the CP by writing an address in the Comparator Latch and enabling or disabling the Comparator. (Enabling the CP Comparator will result in a CP 'Stop-on-Compare' when the value of the CP Comparator equals the value of the CP's MIC.)

6. GIVE A SCOPE SYNC PULSE:

   Generate a scope Sync pulse by setting the Comparator Latch but not enabling it.

NOTE

1. The BP must instruct the CP to be in Step Mode before issuing any of the following commands:

   a. Read or Write Control Memory.
   b. Load/Increment the Microinstruction Counter.
   c. Read MAR1 or MAR2.
   d. Set CP clock speed.

2. These commands are ignored by the CP if it is not in step mode.

2.4.1.1.16 BP Diagnostic Hardware Latch

The System Clock (Phi S) has the added feature of Fast, Slow, or No clock operation as directed by the Bus Processor through the BP hardware latch. This feature (which is implemented by the software reading of switch S1) may be used during system diagnostics to determine the marginal operating limits of the system. The hardware latch is used to control four BP diagnostic hardware signals (five functions), and is cleared (all bits set to zero) at initialization time. The five functions are:

ALLOW PARITY ERROR:
- 0 = Normal operation (write good parity). HALT 8086 for CODE RAM parity error. Report error for DRAM parity error.
- 1 = Interrupt, but do not halt, the 8086 for CRAM parity error on Read. Do not write a new parity bit or alter a parity bit on a CRAM or DRAM Write regardless of source of access.

CRYSTAL:
- 0 = Crystal controlled clock speed for DRAM is enabled. Must be 1 if FAST = 1 or SLOW = 1.
- 1 = Crystal controlled clock speed for DRAM is disabled.

FAST:
- 0 = The fast speed clock for the DRAM is disabled.
- 1 = The fast speed clock for the DRAM is enabled. Must be 0 if SLOW = 1 or CRYSTAL = 0.

SLOW: 0 = The slow speed clock for the DRAM is disabled.
1 = The slow speed clock for the DRAM in enabled. Must be 0 if FAST = 1 or CRYSTAL = 0.

NO CLOCK: The NO clock function is achieved by disabling the Slow, Crystal, and Fast clock bits (set to 0,1,0).

2.4.1.1.17 BP Software Switches

The BP has an eight position DIP switch (S1) that is read by the BP microprocessor to determine diagnostic mode or normal system operation. (Refer to paragraph 3.2.9 for details of the switch settings.)

2.4.1.2 BP Data RAM

The 32K-byte Data RAM (DRAM) on the BP board is a separate high speed static RAM much like a smaller secondary main memory. (A Static RAM does not require Refresh.) The DRAM is used as an I/O buffer pool and is accessible to the 8086 Microprocessor, the LSI (Floppy Disk) DMA, Main Memory DMA, and the I/O devices, all via the DRAM Bus. It has its own memory controller and parity generating circuitry which utilizes the Allow Parity Error function of the Diagnostic Hardware Latch on Writes. A DRAM parity error is returned to the device in the form of a status bit, and it is up to the device to report the failure. The BP may specify any address in the DRAM within the address limitations of a particular I/O device in order to take full advantage of the DRAM as a buffer.

2.4.1.2.1 DRAM Control

There are thirteen request paths into the DRAM, ten external and three internal, all on an I/O address space priority basis. (External paths are those parts which are completed via the Mother Board.) Ten of the paths are reserved for the I/O Device Adapter (I/O DAs) to DRAM Request In (DRIs). The three internal request paths are the 8086 Microprocessor Request path, the Main Memory DMA Request path, and the LSI (FDC) DMA Request path. (See table 2-18 on page 2-35.) There are also a corresponding number of DRAM Grant Strobe (DGSs) paths from the DRAM.

These DRIs and DGSs are controlled by jumpers on each DA. Some DAs may have two priorities; for example, a high priority for the device interface and a low priority for a resident processor. 'Intelligent' DAs are not required to use the second DRI/DGS path (and, presently, none do).

All DA's must provide an 8-bit identification value which is hardwired into every board. This value specifies four aspects of each board: with or without a resident processor, type of board, particular board within a type, and the number of ports (or peripherals supported). A list of currently existing values may be found in table 2-12 on page 2-25.

The DRAM memory controller uses two Data Ram Control Bits (DCB's) to control the request. The two DCB's are defined in table 2-19 on the adjacent page.

Table 2-18. Data RAM Priority Requests

PRIORITY NUMBER	I/O ADDRESS	DRI/DRG NO. 1	DRI/DRG NO. 2	SUGGESTED BOARD OR FUNCTION
1	01xx	0	-	CMD/FMD/SMD
2	02xx	1	-	Quantum
3	03xx	2	-	(Reserved)
4	04xx	3	-	SIO or ISIO
5	05xx	4	-	(Reserved)
6	06xx	5	-	TC
7	00xx	5.3	-	8086 Processor
8	00xx	5.5	-	Memory DMA
9	00xx	5.7	-	FDC LSI DMA
10	03xx	-	6	(Reserved)
11	04xx	-	7	(SIO or ISIO)
12	05xx	-	8	(Reserved)
13	06xx	-	9	(TC)

NOTES

1. Note that second level priorities (DRI/DGS 6-9) must be reserved for the devices using the first level priorities (because the I/O address is the same).

2. Only four Device Adapters which use both DRIs/DGSs may be installed in a given system.

Table 2-19. Data RAM Control Bits

DCB1	DCB0	OPERATION
0	0	WRITE-8 data from low byte bus.
0	1	READ-16.
1	0	WRITE-16.
1	1	WRITE-8 data from high byte bus.

The Write-8-low commands allow for the fact that the 8086 puts the data on the low byte bus when it is necessary to write the low byte, and likewise, puts the data on the high byte bus when it is necessary to write the high byte (Write-8-high).

DCB0 and DCB1 are decoded to determine the type of operation to be performed. If an 8-bit byte-swap will take place, where the low bus data is written to high byte memory and high byte data is written to low byte memory, then A0 controls the byte swapping operation. When A0 = 0, data on the low byte bus is written to the low byte. When A0 = 1, data on the low byte bus is written to the high byte (and data on the high byte bus is written to the low byte). Bytes are swapped only when A0 is high. If a Read-Modify-Write (RMW) is required, where the high order or low order byte is selected and replaced within the halfword, then A0 is not (necessarily) part of the operation.

The resulting halfword is latched and held for parity generation. Parity

is generated by the DRAM parity generation and checking circuit and accompanies the data halfword as it is written to memory. The parity RAMs are written at the same time as the data RAMs.

2.4.1.2.2 DRAM Parity

The Data RAM has its own parity generation and checking circuit. Parity errors (on Read) are returned to a specific device in the form of a status bit (on the DSB line) and it is up to the device to report the failure. (Refer to paragraph 2.4.1.1.16 for parity error handling in diagnostic mode.)

2.4.1.2.3 DRAM Timing

The Data RAM has a fixed, rather than asynchronous, cycle time of 300 nanoseconds (ns), divided into six equal T-states of 50 ns. This means that even if no request is present at the beginning of the cycle, the DRAM controller takes the full 300 ns before sampling the request lines again.

2.4.1.3 BP Main Memory Direct Memory Access

The Bus Processor has control of a Direct Memory Access (DMA) channel to Main Memory and can read and step (ripple) all MAR's connected to the DRAM/MM DMA channel. The DMA channel has its own controller with a DMA path to Main Memory and the DRAM. The 8086 microprocessor, and the Floppy Diskette Controller (FDC) can only access Main Memory by moving their data through the DRAM while using the MM DMA channel. In other words, their only means of communication with Main Memory is an indirect path via the Data RAM.

Since the BP controls the DMA function, the BP instructs the DMA controller to transfer the data between the DRAM and MM. The FDC must notify the BP when it has completed the transfer of a block of data to the DRAM (via the LSI-DMA channel). The BP then directs the MM DMA to begin the transfer and the transfer proceeds under the control of the MM DMA.

2.4.2 FLOPPY DISKETTE DRIVE CONTROLLER

The second major functional area of the Bus Processor board is the Floppy Diskette Controller (FDC). The FDC is based on a Large Scale Integrated (LSI) circuit. It supports a dual-sided, double-density, diskette drive. It also has a Phase Lock Loop (which includes a Phase/Frequency Detector, a Loop Filter, and a Voltage Controlled Oscillator) and a DMA channel. The FDC does not have a DMA path to Main Memory but instead uses the LSI DMA path to the DRAM.

2.4.2.1 Floppy Diskette Drive Controller LSI Chip

The FDC Large Scale Integration chip contains the circuitry and control functions for interfacing its processor to the floppy diskette drive. The VS-25/45 supports a single diskette drive on the main frame. (Additional diskette drives must be supported by Archiving Workstations.) It is capable of supporting single density format (FM) or Double Density format (MFM) including single or dual sided (soft sector only) recordings.

The FDC LSI operates in a DMA mode. The BP microprocessor has only to load the necessary control commands into the FDC/LSI and MM DMAs. All data transfers are then under control of the FDC and the MM DMA controller, and intervention by the 8086 is no longer required until the DMA operation is complete.

The FDC can perform 15 different commands, initiated by a multibyte transfer from the 8086 microprocessor and resulting in a multibyte transfer back to the BP microprocessor after execution of the command. Each command consists of three phases:

1. Command: The FDC receives all information needed to perform a particular operation from the microprocessor.
2. Execution: The FDC performs the operation.
3. Result: Status and other "housekeeping" information are made available to the microprocessor.

2.4.2.2 Phase Lock Loop

The Phase Lock Loop (PLL), also known as a data separator, is designed to handle single and double density diskette drives. The PLL is comprised, in part, of a loop that synchronizes itself to disk read data using a VCO SYNC signal. The loop consists of a Phase/Frequency Detector, Loop Filter, and a Voltage Controlled Oscillator (VCO).

When not reading data, the loop locks to the system Write Clock using the Phase/Frequency Detector. The P/F Detector insures that the loop will lock on frequency no matter how great the the original frequency error. When the VCO SYNC signal is received, the loop is already operating at the nominal data readback frequency. The frequency error that the loop must then respond to is the difference between the actual and nominal readback frequencies and that error is equal to twice the spindle speed regulation. Because of this, manual adjustment of the free-running VCO frequency is not necessary.

This type of circuit results in several advantages. First, no adjustment is necessary (or possible); second, it will operate with FM or MFM encoded data; third, it will use only the leading edge of the read data, meaning that the width of the read data pulse is not important.

2.4.2.2.1 Phase/Frequency Detector

The output of a Phase/Frequency Detector is a signal that varies with the difference in phase of its two input frequencies. The detector is a linear detector meaning that the output is proportional to the phase difference. Because it is a true Phase/Frequency Detector, the two input signals do not have to be at the same frequency. They may be harmonically related and still result in a zero output if the phase angles of both inputs are the same. This is how a constant frequency VCO can be compared to a readback data stream whose instantaneous frequency depends on the data pattern. Finally, this is a logical detector meaning that it is designed to operate with logic input levels.

2.4.2.2.2 Loop Filter

When the Voltage Controlled Oscillator (VCO) is operating at a different frequency, or is not in phase with the incoming data (either nominal clock frequency or read data), the loop filter develops a phase error. This error, when multiplied by the gain of the Phase Detector and the dc gain of the filter, is enough to move the control voltage the required amount (which in turn changes the frequency of the VCO in the direction of the input frequency). Using an integrator in the filter makes the dc gain almost infinite.

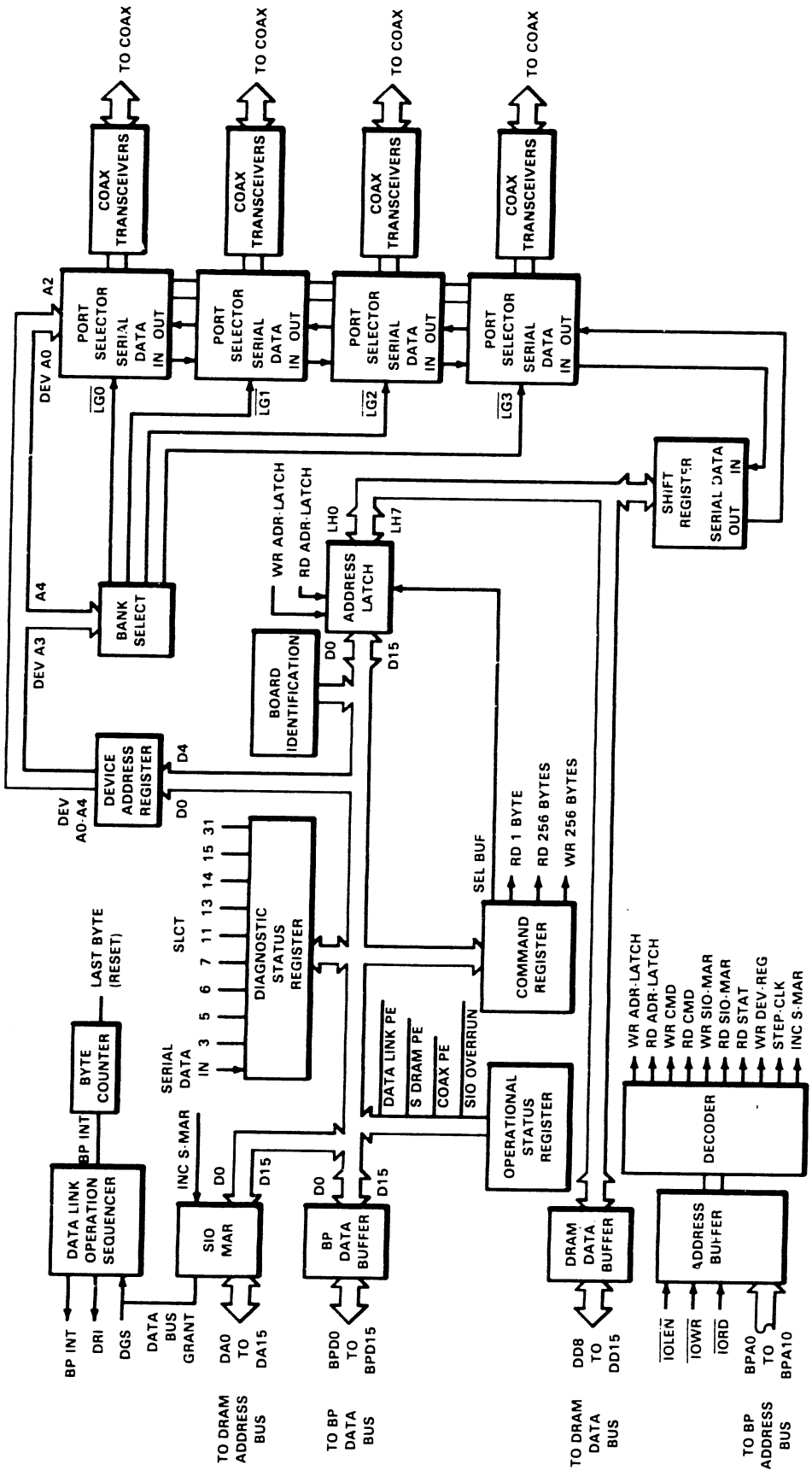

Figure 2-5. VS-25/45 Serial I/O Device Adapter Block Diagram

2.4.2.2.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator accomplishes FM and MFM operation by selecting (by VCO sync) the appropriate half of this dual mode oscillator. Because the Phase Detector requires that the read clock be a square wave, the VCO operates at twice the read clock frequency and is then divided by two, resulting in a frequency of 0.5 MHz for FM or 1 MHz for MFM. This corresponds to 0.25 Mbyte/second for FM or 0.5 Mbytes/second for MFM.

2.4.2.3 LSI-DMA Channel to the DRAM

The FDC has access to Main Memory via the LSI-DMA channel to the Data RAM. Once the 8086 microprocessor loads the appropriate command into the FDC, the 8086 is released and all DMA transfers are handled by the LSI DMA hardware path to the Data RAM. Data from the FDC is loaded into the DRAM, via the DRAM Bus, at the next available DRAM address. At this point, the MM-DMA initiates its operation and begins to transfer data from the DRAM to Main Memory via the MM Bus. Data may be loaded by the LSI-DMA to the DRAM at the same time that data is being transferred from the DRAM to the MM-DMA. This results in an extremely high rate of data transfer between the FDC and Main Memory.

2.4.3 REMOTE DIAGNOSTIC TELECOMMUNICATION CHANNEL

Remote Diagnostic Service is a maintenance program that is offered to VS-25/45 customers. The primary goal of the service is to isolate problems remotely so that the Customer Engineer can bring the correct parts with him, thus suppling the customer with a responsive and efficient level of service.

The VS-25/45 hardware includes a Telecommunication (TC) channel on the Bus Processor board which is used to establish a link with the Remote Maintenance Center. The two basic features of the Remote Diagnostic Service involves the ability to read the Nonvolatile RAM (NVRAM), located on the BP board, and the capability to run all the off-line diagnostics remotely. Remote Diagnostic Support is described in paragraph 8.3.

2.5 SERIAL I/O DEVICE ADAPTER

The SIO Device Adapter (SIO DA), figure 2-5, is a modified 928 serial data link with the capabilities of a 16-port VS-60/80 device adapter. It uses the Bus Processor Data RAM (BP DRAM) to double buffer data on its way to and from Main Memory. The PROMs that stored the SIO control mode code have been removed from the SIO DA and the DA control mode code is now stored on disk where it can be moved directly to the workstation via the DRAM. In addition, the serial I/O device file information which was previously stored on the DA, along with all other information that the BP needs, is now stored in the BP's Code RAM. This allows easy access by the BP to all information that may be required.

2.5.1 SIO DA Data Link

The SIO DA data link operates in a manner similar to the VS-60/80 data link, but uses line drivers and receivers similar to those found in OIS hardware. The Data Link Sequence Controller on the Device Adapter controls the sending of commands, addresses, and data to the selected serial device over the coaxial lines. A Shift Register provides the serial-to-parallel and

parallel-to-serial data conversion for transmission and reception between the I/O device and the SIO DA. The data received from the I/O device is stored in the BP DRAM until needed elsewhere.

A Bank Selector selects one of two 8-port input/output banks while the Port Selector selects one of the eight ports. All coaxial lines (used or unused) are driven with zero bits for improved noise immunity. Any byte transmitted from the port over the coaxial lines has an eleven bit protocol: a Start bit (a one); eight data bits; a Parity bit; and a Stop bit (a zero). The Device Adapter bit clock generator needs the Start bit, during the receive mode, to begin operation.

The interface between the BP and the SIO DA uses a bidirectional Data Latch for isolating the Motherboard from the internal data bus, an Address Buffer to isolate the Motherboard from the internal address bus, and an Operational Status Register to store status information that can be read by the BP. A data length register (byte counter) causes an interrupt to be sent to the BP and clears the SIO DA logic when an instruction is complete.

A hard-wired 8-bit Board Identification Register, which is read by the BP, provides identification of the device adapter (ie: SIO - 928 Serial Data Link). Data Requests (DRI), Data Grants (DGS), and BP Interrupts (BPINT) are jumper selected on the DA. Each must match the I/O address space scheme for the DRAM.

2.5.2 SIO DA Buffering and DMA Path

The SIO Device Adapter does not have a direct path to Main Memory. Its only means of communication with Main Memory is an indirect path via the Data RAM and the DRAM Bus. The DA uses the DRAM as an I/O data buffer pool which double buffers the data between the I/O device and Main Memory. (Data from the SIO DA is loaded into the DRAM, at the next available DRAM address.) The BP may specify any address in the DRAM within the address limitations of the I/O device allowing the device to take full advantage of this feature.

The BP instructs the Main Memory-DMA controller to transfer the data between the DRAM and Main Memory. The MM-DMA initiates and controls the operation, and the transfer of data is accomplished via the MM Bus. Data may be transferred by the SIO-DMA to or from the DRAM at the same time that data is being transferred between the DRAM and Main Memory by the MM-DMA. This double buffering arrangement results in a very high rate of data transfer between Main Memory and the I/O device.

2.5.3 SIO DA Data Transfers

There are only two types of data transfers to or from serial devices that can be done by the Device Adapter; 'Read or Write one-byte' and 'Read or Write 256-bytes'. The data transfers are initiated by four data link operation commands. The following are brief descriptions of the actions taken by the BP, the SIO DA, and the serial device during data transfers resulting from those commands.

2.5.3.1 Write Dev One-Byte

The Bus Processor writes one byte to the Data RAM for later tranmission. It then loads the required registers (except the command register) on the SIO

DA. Eight bits of BP data are transmitted to the DA's Device Address Register to select the port of the serial device. (Data bits D0-D4 are the port select.) The BP transmits 16 bits of zeros to clear the DA's Memory Address Register (MAR) and the MAR is then initialized to the BP DRAM address where the data to be transmitted resides. Eight bits of BP data containing the command byte (which activates the SIO DA) are then transmitted to the Device Adapter's Command Register.

The Device Adapter transmits the command byte (and each data byte) to the selected device with a Start bit added to the beginning, and an odd parity bit and a Stop bit added to the end making the command byte (or data byte) an eleven-bit byte protocol. (The device is normally in the receive mode.) Following the eleven-bit command byte, two bytes of address previously sent from the BP to the DA's Address Latch are transmitted to the device.

The first three data bits of every command received by the serial device are a special header (101) that the device uses to make sure that coaxial line noise does not start its timing circuits. (When the device decodes the three bits, it uses the first one bit to initialize its timing circuits which count out the eleven-bit intervals needed for a byte transfer.) The parity bit of the command byte is tested and, if valid, the command is decoded and loaded into the device command register.

One byte of data is sent from the BP DRAM to the DA's bidirectional data latch, converted to serial data by the shift register, and transmitted to the device over the coaxial lines at 4.27 megabits per second. The device stores the data byte in its memory. No response is transmitted to the SIO DA by the serial device. Upon completion of the transmission, the Device Adapter clears it's command register, sends an interrupt which notifies the BP that the operation is terminated and, simultaneously, becomes deactivated.

2.5.3.2 Write Dev 256-bytes

The procedure used for 'Write 256-bytes' is essentially the same as the 'Write one-byte' with the exception of the data string length. Initially, the Bus Processor writes 256 consecutive bytes to the Data RAM. The BP follows the same protocol concerning the Device Adapter's registers, command bytes, and address bytes as it did for the 'Write one-byte' command.

The Device Adapter follows the same protocol concerning command bytes and address bytes as it did for the 'Write one-byte' command. One byte of data at a time is sent from the BP DRAM to the I/O device by the DA starting at the current address pointed to by the Device Adapter's MAR. The MAR address is incremented by one after each one-byte transfer until all 256 bytes have been transferred.

The device begins storing the data in its main memory and increments it's own byte address counter. The transfer ends when all 256 bytes have been sent by the DA. Again, no response is transmitted from the device to the Device Adapter and, upon completion of the transmission, the Device Adapter clears it's command register, sends an interrupt to the BP, and becomes inactivate.

2.5.3.3 Read Dev One-Byte

The Bus Processor loads the required registers (except the command regis-

ter) on the SIO DA thus selecting the serial device to be read. The DA's Memory Address Register (MAR) is cleared and the MAR is then initialized to the DRAM address which will receive the data. The BP then loads the DA's Command Register, activating the Device Adapter.

The Device Adapter begins transmitting the command byte, the two address bytes, and ten microseconds of zeros to the I/O device. (The ten microsecond delay provides the turn-around time necessary for the lines to stabilize.) The DA's receivers are enabled for incoming data after the ten microseconds of zeros are transmitted and the DA waits for the first non-zero bit (Start Bit) of the incoming data. (This entire procedure, after the tranmission of the command byte, is the line turn-around sequence.)

After the command and address are received by the device, the device reverses the coaxial lines so that data can be sent to the Device Adapter. Seven microseconds after the DA began transmitting zeros, the device begins transmitting zeros, and then transmits it's data over the coaxial lines to the Device Adapter.

When the data (one byte) is received by the Device Adapter, the byte is strobed into the DRAM via the DA's DMA. Upon completion of the transmission, the Device Adapter clears it's command register, sends an interrupt to the BP, and terminates it's operation.

NOTES

1. During receive mode, the Device Adapter will wait a maximum of 30 microseconds for the next Start Bit. If no response is received within that time period, a time-out has occurred. An immediate interrupt is sent to the BP by the Device Adapter which then clears it's logic and deactivates.

2. When receiving data from a device, a minimum of eight microseconds must pass prior to any new operation being initiated to that device.

2.5.3.4 Read Dev 256-bytes

As noted in the write operations, the procedure used for 'Read 256-bytes' is essentially the same as the 'Read one-byte'. Initially, the Bus Processor loads the required registers, selects the serial device, and clears the DA's MAR and loads the DRAM address for the incoming data. It then loads the Device Adapter's Command Register, activating the DA.

The Device Adapter again transmits the command byte, the two address bytes, and the line turn-around zeros to the I/O device. The DA's receivers are enabled after ten microseconds and the DA waits for the first non-zero bit of the incoming data. (The line turn-around sequence is initiated.) The Device Adapter will wait a maximum of 30 microseconds before initiating a time-out.

After the command and address are received by the device, the device re-

verses it's coaxial lines. Seven microseconds after the DA began transmitting zeros, the device again transmits zeros. It then begins transmitting data over the coaxial lines to the Device Adapter, while incrementing it's own byte address counter. The transfer ends when all 256 bytes have been sent by the I/O device to the DA.

When the data is received by the Device Adapter, one byte of data at a time is strobed into the DRAM by the DA's DMA circuit starting at the address pointed to by the Device Adapter's MAR. The MAR is incremented by one after each one-byte transfer to the DRAM until all 256 bytes have been received. Upon completion of the transmission, the Device Adapter clears it's command register, sends an interrupt which notifies the BP that the operation is complete and again becomes inactivate.

2.5.4 Additional SIO DA Control Commands

There are two Control Commands use by the Device Adapter during it's operation: Restart and Give Status.

2.5.4.1 Restart

A restart command is sent to the selected device by the Device Adapter in much the same manner as the 'Write one-byte' command. After the Bus Processor has loaded the SIO DA's registers (including the Command Register), the DA transmits the Restart Command. The command resets the device CPU and the device not ready condition is cleared. No response is transmitted to the Device Adapter by the serial device. The operation is terminated at the end of the command by the Device Adapter in a normal 'Write one-byte manner.

2.5.4.2 Give Status

The Give Status command is initiated after read or write operations to find out if there were any errors detected by the device. If there were errors, the read or write instruction must be repeated. The operation of the Device Adapter almost identical to the 'read 1 byte command'.

After the Bus Processor has loaded the SIO DA's registers (including the Command Register), the DA transmits the Give Status Command to the selected device and the line turn-around sequence is initiated.

The device transmits status information (not ready, line error, local memory parity error, device type, etc.) to the Device Adapter. After the status (one byte) is received by the DA, it is strobed into the DRAM at the address indicated by MAR and the operation is terminated. If no status is received, a time-out will occur, and an immediate interrupt is sent to the BP by the Device Adapter which then clears it's logic and deactivates.

2.5.5 SIO DA Data Overrun

For both 'Write one-byte' and 'Write 256-bytes' commands, data overrun, where the last byte of data from the DRAM has not been transmitted but the next byte has been requested, is checked by the Device Adapter's Data Overrun Detector. If overrun is detected, a "garbage" byte of data is transmitted by the DA's controller to the serial device. The detector remembers the error but does not terminate the command. The operation terminates when the DA's

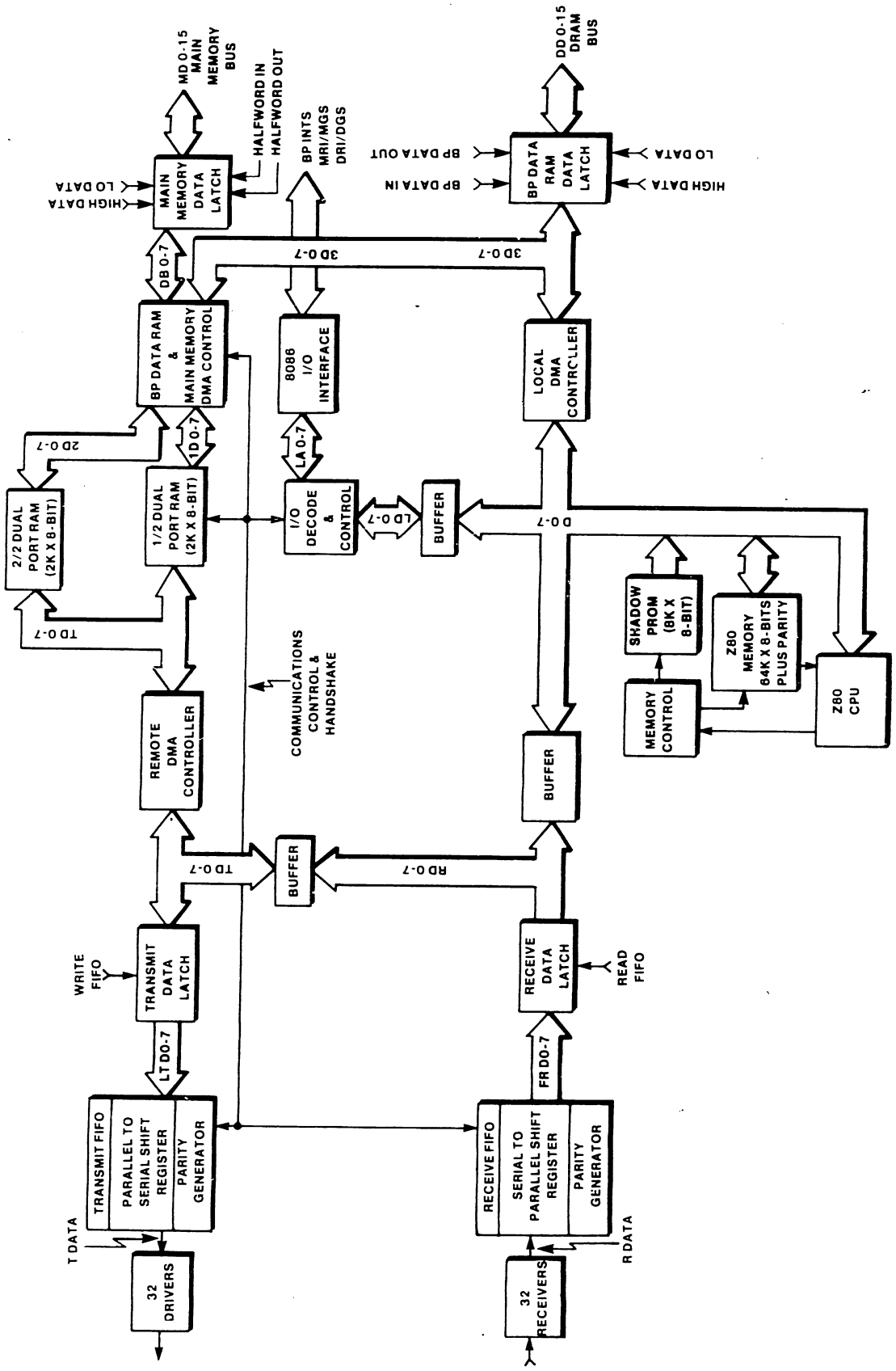

Figure 2-6. VS-25/45 Intelligent SIO Device Adapter Block Diagram

controller has transmitted the correct number of bytes. The BP detects the error by reading the status register on the Device Adapter.

2.6 INTELLIGENT SERIAL INPUT/OUTPUT (ISIO) DEVICE ADAPTER

The Intelligent Serial Input/Output (ISIO) Device Adapter (figure 2-6) is a 32-port intelligent 928 type serial master data link. The ISIO DA allows the VS-25/45 to interface with the high speed slave data link channels. Parallel processing and buffered internal busses supports concurrent central processing and multiple Direct Memory Access (DMA) operations.

The ISIO uses the following Large Scale Integration (LSI) components:

1. Z80A-Central Processing Unit (CPU).
2. Two Z80A-CTCs (Counter/Timer Circuits) for extensive timer/counter functions as well as interrupt handling.
3. Two 9517A and one hybrid DMA controllers, all of which may be operating at the same time.

The ISIO also features:

1. 8K bytes of shadow PROM.
2. 64K bytes of Data RAM.
3. Three separate internal busses for parallel processing.
4. Four separate external busses/interfaces.
5. Two banks of dual-port RAM to facilitate efficient data transfer between the BP and Main Memory, and the Master Data Link (MDL).
6. Three different DMA controllers.
7. DMA transfers to BP Data RAM and Main Memory at the same time.
8. Master Data Link that can transmit and receive at the same time, to accommodate diagnostic and IPL modes.

2.6.1 DIRECT MEMORY OPERATIONS

All DMA operations are initialized and controlled by the CPU. The local DMA controller resides on the same bus as the CPU and uses four channels. These four channels, in order of priority, are: receive First In, First Out (FIFO) buffer, receive BP Data RAM, transmit FIFO, and transmit BP Data RAM.

The remote DMA controller is dedicated to servicing the transmit and receive FIFO's. It moves data between the FIFO's and the dual-port RAM. The hybrid DMA controller interfaces the BP Data RAM and/or Main Memory to the dual-port RAM. This controller includes a memory command generator, byte-to-word converter, and a DMA multiplexer sequencer.

The remote and hybrid DMA controllers use two banks of dual-port static RAM as their memory. These two memory banks are independent and may be accessed simultaneously by either DMA controller. The CPU supervises these 'scratch pads' with an I/O command.

2.6.2 MASTER DATA LINK (MDL)

The Master Data Link (MDL) has separate transmit and receive controllers. Each controller includes a shift register, 16-byte FIFO, parity, and necessary

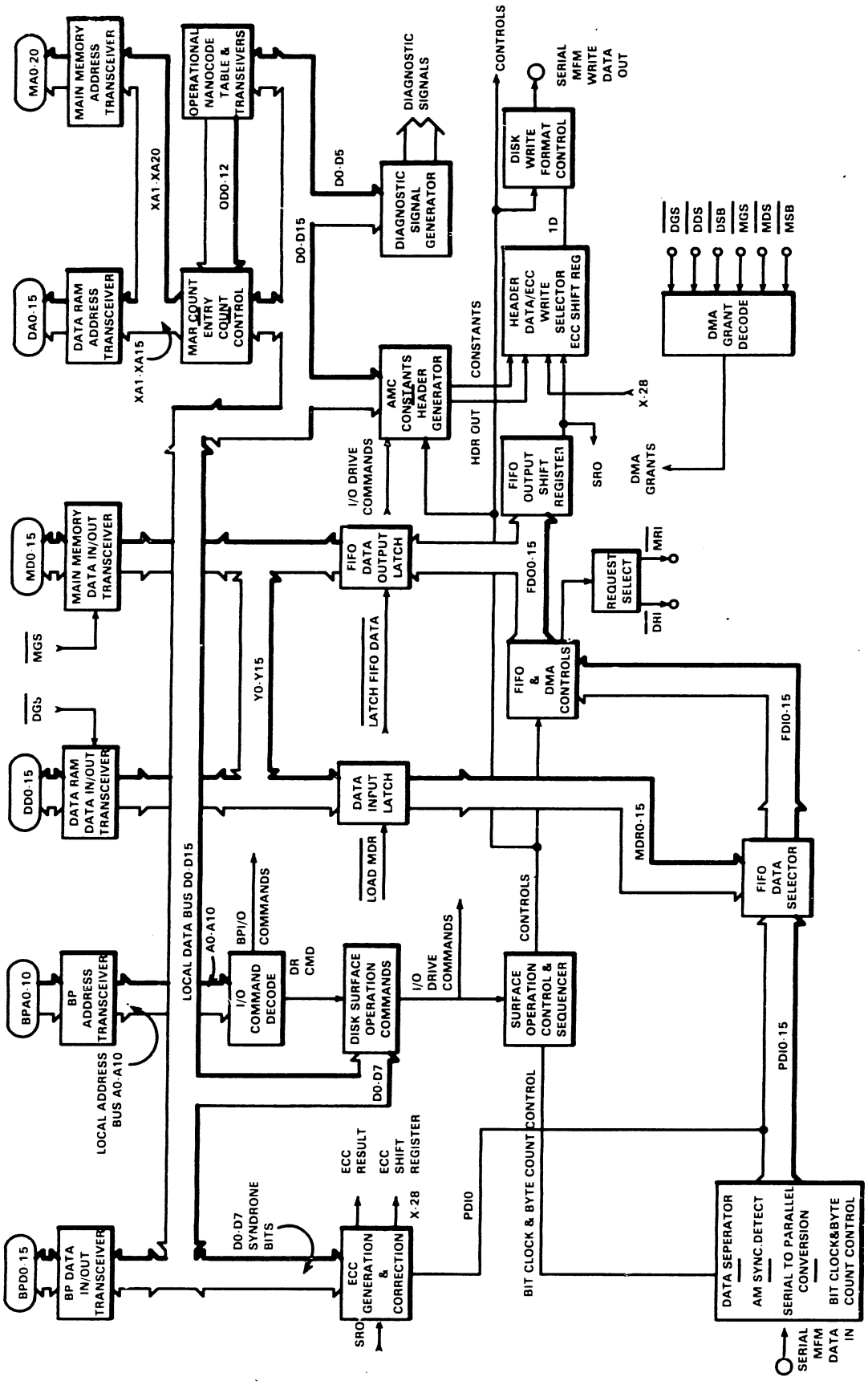

Figure 2-7. VS 25/45 Quantum Disk Drive Device Adapter Block Diagram

control logic. The FIFO's are accessible by both the local and remote DMA controllers, as well as the CPU. The master link will support both internal and external loopback, such that the entire MDL, including the receivers and drivers, may be tested under software control (diagnostic mode).

The I/O decode and control logic is the CPU's path to controlling the DA. All external interfaces/busses are controlled through the I/O. The I/O control includes two Z80A-CTC programmable counter/timer devices. The first CTC has the highest interrupt priority and will handle the transmit byte count, End Of Process (EOP) interrupt (last byte sent to transmit FIFO), and background timing. The second CTC handles the receiver byte count, BP Data RAM interrupt, and parity error on the MDL receive.

2.7 QUANTUM FIXED DISK DRIVE INPUT/OUTPUT DEVICE ADAPTER

The Quantum Disk Device Adapter is designed to handle two 8" Quantum 'Winchester' fixed disk drives. Each drive will contain 32M bytes of formatted (42M bytes unformatted) data. The drive has eight surfaces (eight heads) and 512 cylinders for a total of 4096 tracks. The functional block diagram is shown in figure 2-7.

2.7.1 SURFACE OPERATIONS

The Device Adapter will set up for a surface operation by seeking the correct cylinder and loading the stepper counter. It will then load the corresponding cylinder and head register pointing to the first surface to be operated upon. The DMA counter will then be loaded with the number of halfwords to be transferred (The DA only does halfword (two-byte) operations.), and the First In, First Out (FIFO) buffer will be checked to assure that it is empty before starting the operation. The Operational Nanocode Table will be initialized and the Drive Command will be issued thus beginning the surface operation.

2.7.1.1 Disk Format

The Quantum Controller will soft sector format the disk two ways; either with 256-byte sectors for 32 sectors per track or 2K-byte (2048) sectors for four sectors per track. (The 256-byte sector function has not been implemented by the VS Operating System software.) The drive uses no sector pulses, only index pulses, and sectors are detected by address marks. When formatting a sector, the entire track must be formatted.

During formatting, the Device Adapter awaits the leading edge of the Index Pulse. Once it has sensed this edge, the format operation begins. Both types of format begin with a 16-byte gap (G1) to provide a head switching recovery period, and end with another gap (G4) which provides a speed tolerance buffer for the entire track.

When sector formatting begins, each sector includes the header sync field (Sync1), header address mark, the header (cylinder, head, and sector numbers), header Error Correction Code (ECC), and the G2 gap. This is followed immediately by the data sync field (Sync2), data field address mark, 'data filler' from the DA's Memory Data Register, the data ECC, and gap G3 (which allows for line voltage variations in disk speed). Sector formatting is repeated four times for 2K-byte sectors (or 32 times for 256-byte sectors). After gap G4 is written, the format operation terminates with an interrupt to the BP.

2.7.1.2 Disk Write

To begin writing, the Device Adapter must sense the trailing edge of the sector pulse. The DA's Memory Address Register (MAR) is then loaded with the memory address entry from the Operational Nanocode Table (ONT). The MAR contains the memory address (either Data RAM or Main Memory) from which the data is to be transferred.

The header address mark is compared with the header address mark constant in the data separator, and the header is compared with the header stored in the header register. If the headers do not match, a Header Check status bit is set in the DA's Status Register, no data will be written to the disk, and the operation will be terminated. The header ECC is also checked and if the header ECC matches, the Device Adapter reads one halfword (two bytes) at a time from the applicable memory and increments the MAR by one. (A header ECC error can be detected, but is not correctable.)

The data is entered into the FIFO buffer. The Device Adapter writes Sync2 (10 bytes of zeros), and the data address mark thus designating the start of the data field and the data is written from the FIFO to the disk. From this data, data ECC (29 bits) is computed and written onto the disk after all data (2048 bytes) are transferred from memory to the disk.

If the entry count is not yet zero, the Entry Count Register is decremented by one, the next valid entry from the ONT is entered into the MAR, and another sector is written. (Refer to paragraph 2.7.5, Multisector Operations.) After all entries are completed, the Device Adapter signals completion by an interrupt to the Bus Processor.

2.7.1.3 Disk Read

The Disk Read operation is essentially the reverse of the Disk Write operation. The trailing edge of the sector pulse is sensed, and the MAR is loaded with the memory address entry from the Operational Nanocode Table. Data will be transferred to the memory address stored in the MAR.

The header address mark and the header are again checked. If they do not match, the Header Check status bit is set in the DA's Status Register, no data will be read from the disk, and the operation will be terminated. After a successful checking of the header ECC, the Device Adapter checks the data address mark and prepares to read the data. The DA reads one halfword (two bytes) at a time from the disk and increments the MAR by one.

The data is entered into the FIFO buffer after which it is written to memory. A total of 2048 bytes are transferred from disk to memory. While reading, the ECC remainder is computed and this remainder is compared against the ECC read from disk. If a discrepancy occurs, the Data ECC Error status bit is set.

The Entry Count Register is decremented by one (until it reaches zero) and the next valid entry from the Operational Nanocode Table is entered into the MAR and another sector is read. After all entries are read, the DA interrupts the BP to signal completion.

2.7.1.4 Read and Ignore Header

This command will allow the controller to read data while ignoring the header. Used for the recovery of data where the Header may have degraded to the point of no compare.

2.7.1.5 Verify

The Verify command is similar to the Read command with the exception that the data in memory is read at the same time as the data on disk and the two are compared bit by bit. At the end of this operation, the microprogram has only to inspect and test the status and ECC remainder.

2.7.1.6 Diagnostic Write

The diagnostic program uses this command to write to disk bad data with a good ECC remainder. The data field and the four bytes of memory following it are written onto the disk.

2.7.1.7 Diagnostic Read

Similar to the Read command, this command is used to read into memory the data and ECC remainder for diagnostic testing of the error correction logic. It causes the data field and the first four bytes immediately following it (the ECC remainder) to be read into memory.

2.7.2 ERROR CORRECTION

Upon completion of a Read operation, the Data ECC Error (DECC) status bit is examined. If it has been set, an ECC Error has occurred and correction will be attempted for one 10-bit error.

The Attempt Error Correction command, when issued, will search for the first address in error in the block. The ECC Result bit is checked; if it is one, the error is not correctable (Fatal) but if it is a zero, the error is correctable. If the error is correctable, 10 bits of ECC data is read.

Data from the Main Memory or Data RAM is retrieved as indexed by the ECC address. The ECC data and the MM/DRAM is exclusively ORed and the result of the OR is written back into the MM/DRAM at the data's original location. The Error Bit Reset command is then issued.

2.7.3 VERIFY FIFO

There are two diagnostic commands used to verify the integrity of the FIFO, they are 'Fill FIFO' and 'Empty FIFO'. In diagnostic mode, with the first entry in the Operation Nanocode Table (ONT) initialized to a valid MAR address, the MAR is loaded with the address of the data to be written into the FIFO.

After setting the Data RAM/Main Memory DMA source, issuing the 'Fill FIFO' command will cause the FIFO to be loaded with sixteen (2-byte) halfwords of data, from either the DRAM or MM, using the ONT and the MAR. The hardware will issue a DRI or MRI, and receive a DGS/MGS, transferring data automatically until the FIFO has been completely loaded. Termination will be caused by the Input Ready signal on the FIFO going inactive. The address from the ONT will

be latched into the MAR for the first halfword. Subsequent DMAs will increment the MAR by one with each DGS/MGS received from the Bus Processor.

To complete the verification of the FIFO, while still in diagnostic mode with an initialized Operational Nanocode Table and a loaded MAR, the DRAM/MM DMA destination is set, and the 'Empty FIFO' command is issued.

The hardware will, again, issue a DRI or MRI, and receive a DGS/MGS, transferring data automatically until the FIFO has been emptied. The Output Ready signal on the FIFO, by going inactive, will terminate the operation. Likewise, the address from the ONT will be latched into the MAR for the first halfword and subsequent DMAs will increment the MAR by one.

2.7.4 QUANTUM STATUS REGISTER

The Quantum DA maintains a 16-bit Drive and Controller Status Register whose content is set as a result of initialize and reset buttons, error conditions, and interrupts. The status bits indicate to the DA that an "event" has occurred. Table 2-20 includes all Quantum status bits.

Table 2-20. Quantum Disk Drive Status Register Bits

BIT	NAME	CONDITION
D0	FIFO OVERFLOW OR UNDERFLOW	Memory not available to accept data, FIFO O/F. Memory busy during Write, not enough data to FIFO.
D1	SECTOR OVERRUN	No Data Address Mark found or Track not formatted.
D2	MEMORY ERROR	DRAM/MM parity or Invalid Memory Address (IMA).
D3	SEEK COMPLETE 1	End of Seek, Drive 1 w/o regard to drive selected.
D4	DATA CHECK ERROR	Data from disk not Verified with data in Memory.
D5	HEADER ERROR	Header/ECC Compare Error. Read and Ignore Header to recover data. Header ECC can not be corrected.
D6	DATA ECC ERROR	ECC comparison error in Data Field, Attempt Error Correction must be performed.
D7	STEPPER BUSY	Steppr Counter busy / not avail. for overlap Seek.
D8	ECC DONE	Indicates ECC correction operation complete.
D9	ECC (ATTEMPTED) CORRECTION RESULT	Notification of Error correction attempt & result to Operating System. Not correctable if High bit.
D10	DRIVE 1 SELECTED	High when Drive 1 is selected.
D11	DRIVE 0 SELECTED	High when Drive 0 is selected.
D12	SEEK COMPLETE 0	End of Seek, Drive 0 w/o regard to drive selected.
D13	TRACK 00	Head positioned on Track Zero of selected drive.
D14	WRITE FAULT	Write Fault on selected drive - Deselect to Clear.
D15	DRIVE READY	Notifies DA that selected drive is/is not ready.

2.7.5 MULTISECTOR OPERATION

Multisector operations are handled by the Device Adapter without intervention by the Bus Processor between each sector operation. A block of 1024 halfwords (2048 contiguous bytes) will be written to (or read from) each sector. Multiple sectors can be written or read using the Operational Nanocode Table (ONT).

The ONT is initialized with the DMA address for each sector to be accessed

up to a maximum of nine sectors (18K contiguous bytes), and the remainder invalidated (validity bit set to zero). The Entry Count Register is loaded with the desired number of sectors, and the first head (first track), corresponding to the first ONT entry, is selected. The DA will relate each table entry to a Rotation and Sector number.

The DA starts seeking its first valid entry at Rotation Zero, closest to the nearest sector, as the disk is spinning. (Entries must start with the first rotation.) When it finds the valid sector entry that is closest to it on the track, it start the operation. Consecutive valid entries (valid entries must be consecutive) are taken until the Entry Count equals zero, or it encounters the end of the table or an invalid entry. (Multisector operations terminate on any error without finishing any remaining sectors.)

If the entry count equals zero, the operation is terminated normally. If the entry count does not equal zero, the DA goes back to the top of the table and looks for the next valid entry. After it has found the next valid entry, it then continues taking entries until the entry count equals zero, at which time the operation is terminated.

2.7.6 INTERRUPTS

Interrupts are generated on three levels (The Bus Processor accepts three interrupts per Device Adapter.), as follows:

Level 1. I/O Interrupts

a. Attempted ECC Correction, ECC complete.
b. Data ECC Error.
c. Header Error (Header Check Error or Header ECC Error.
d. Data Compare Error (from Verify operation).
e. Memory Error (memory parity or Invalid Memory Address).
f. FIFO Overflow/Underflow Status Bit High.
g. Sector Overrun.
h. Normal surface operation termination.

Level 2. Seek Complete 0 (or Stepper Not Busy 0) - Generated after Drive 0 has finished seeking.

Level 3. Ready/Seek Complete 1 (or Stepper Not Busy 1) - Ready line interrupt generated when the selected disk drive is first powered-up. After that, this interrupt is generated after drive 1 is finished seeking.

2.8 STORAGE MODULE DISK DRIVE DEVICE ADAPTER

The Storage Module Disk Drive (SMD) I/O Device Adapter interfaces with externally housed large disk drives of the Cartridge Module, Storage Module , and Fixed Module Drive types. The Device Adapter is offered in 1-port, 2-port, 3-port and 4-port versions. None of the versions can be upgraded to support additional drives.

The SMD DA can perform multisector operations with rotational optimization. Multisector operations are done by the DA, without intervention from

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Figure 2-8. VS 25/45 SMD Disk Drive Device Adapter Block Diagram

the Bus Processor, between each sector operation. Once the last sector in a multisector operation has been serviced, an interrupt is generated. If an error condition occurs, the multisector operation stops at the failing sector and an interrupt is generated. A multisector operation can service any number of sectors up to one complete revolution of the disk. The sectors can be located on one head or two adjacent heads.

2.8.1 WRITE COMMANDS

COMMAND	BP ADDRESS (HEX CODE)
Start	0100
Load Command Register	0102
Load Tag Register	0104
Load Track/Head Register	0106
Load Write Latch	0108
Load Operation Counter	010A
Deselect	010C
Reset	010E
Set Tag Strobe	0110
Load RAM	0112
Enable Seek Error interrupt	0114
MAR Clock	0118
Load FIFO Buffer	011A
Diagnostic Clock 1	011C
Diagnostic Clock 2	011E

2.8.1.1 Start (HEX 0100)

This command initiates format, write, read, verify, and error correction operations. The DA executes the requested operation as set up in the Command Register. When the operation completes, or an error is detected, an Operation Complete interrupt is generated.

2.8.1.2 Load Command Register (HEX 0102)

This command loads the contents of the BP data bus into the Command Register. The Command Register format is shown below.

ECC D2	ECC D1	DIAG M2	DIAG M1	COR MODE	DIAG SP	HCE EN	DMA EN
D15	D14	D13	D12	D11	D10	D9	D8

EN M/D	DMA R/W	VER	CMD 4	CMD 3	CMD 2	CMD 1	CMD 0
D7	D6	D5	D4	D3	D2	D1	D0

The Command Register bit definitions are as follows:

1. CMD0 thru CMD2 - These three bits form a code used by the DA to select 1 of 7 surface operations as shown below:

2. CMD3 - If this bit is set, head selects are inhibited during a multi-sector operation. If this bit is reset, a head select tag is issued for each sector to be serviced. The Head bit (HDB) in the sector table indicates which one of two possible head address are selected.

CMD2	CMD1	CMD0	COMMAND
0	0	0	Reserved For Diagnostics
0	0	1	Format (without data field)
0	1	0	Format (with data field)
0	1	1	Write
1	0	0	Write (in ECC diag mode)
1	0	1	Read
1	1	0	Read (in ECC diag mode)
1	1	1	Verify

3. CMD4 - Defines the sector size for the surface operations listed above. If this bit is set, a 2K byte sector size is selected. If this bit is reset, a 256 byte sector size is selected.

4. VERIFY - This bit will be set when setting up for a Verify operation. It enables data compare checks and disables the loading of the read latch when reading data off the disk.

5. DMA R/W - If this bit is set, the DA's DMA control is set to Write 16 mode. If this bit is reset, the DMA control is set to Read 16 mode.

6. ENABLE M/D - If this bit is set, the DA's DMA control selects the BP data ram. If this bit is reset, the DMA control selects main memory.

7. DMA ENABLE - Will be set for all surface operations that require data to be transferred to or from memory (main memory or Data RAM).

8. HEADER CHECK ENABLE - If this bit is set, the header bytes (track, head, and sector) are checked for correct contents during write, read, and verify operations. If this bit is reset, the header is still read but is not checked.

9. DIAGNOSTIC SECTOR PULSE - This bit is used only when operating in Diagnostic mode 1 (DIAG M1 SET). When DIAG M1 is set, sector and index signals SP and IX are inhibited. If this bit is set, the presents of a pulse is simulated. When not operating in diagnostic mode, this bit remains reset to allow normal operation.
10. CORRECTION MODE - If this bit is set the DA is set up to perform an error correction. If a drive is selected, it must be deselected before the COR MODE bit is set.

NOTE

The following bits are used only for diagnostic testing.

11. DIAG M1 - If this bit is set, the following conditions will occur:
    a. Each time a Diagnostic Clock-2 command is issued, one clock pulse occurs on the clock lines.
    b. The Sector Count bus (SB0-SB5) is held low.
    c. Signals SP (sector pulse) and IX (index pulse) are held low. If a drive is selected, it must be deselected before the DIAG M1 bit is set.

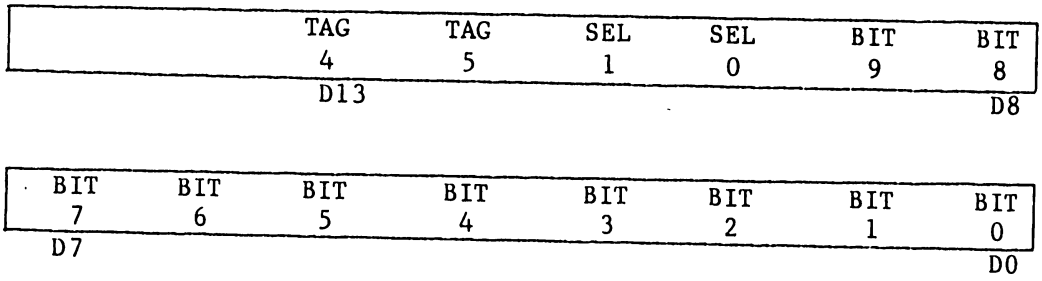
12. DIAG M2 - If this bit is set, the following conditions occur:
    a. The bit timing circuitry (BT1-BT8) is enabled.
    b. The state counter (SC0-SC3) is in load mode.

13. ECC D1 - If this bit is set, DMA operations are modified to transfer six extra bytes.

14. ECC D2 - Allows BP data bus bit 7 (D7) onto the input of the ECC Register.

2.8.1.3 Load Tag Register (HEX 0104)

This command loads the contents of the BP data bus into the Command Register. The Tag Register format is shown below.



The Tag Register bit definitions are as follows:

1. BITS 0-9 - These bits are interrupted at the drive as either a cylinder address, head address, or control lines depending on which one of four tags has been activated.

    a. When setting up for a seek operation, bits 0-9 are loaded with binary cylinder address.

    b. When setting up for a head select operation, bits 0-4 are loaded with a binary head address. If the drive is a CDC CMD type, bits 0-2 are loaded with a binary head address. Bit 4 indicates which volume will be selected. If bit 4 is set the fixed disk is selected. If bit 4 is reset, the removable cartridge is selected.

c. For a control operation, bits 0-9 have the following definitions:
   (1) Bit 0 - Write Gate
   (2) Bit 1 - Read Gate (always set to 0)
   (3) Bit 2 - Servo Offset Plus
   (4) Bit 3 - Servo Offset Minus
   (5) Bit 4 - Fault Clear
   (6) Bit 5 - Not Used (always set to 0)
   (7) Bit 6 - Return to Zero
   (8) Bit 7 - Data Strobe Early
   (9) Bit 8 - Data Strobe Late
   (10) Bit 9 - Release (for Dual Port drives only)

d. On Dual Port drives, bit 9 is defined as a Priority Select bit for a Unit Select operation. For a normal unit select, this bit is reset. If the DA is seizing control of a drive, the unit select operation is executed with bit 9 set.

2. SEL 0 & SEL 1 - These bits select one of four disk drives when a Unit Select Tag is issued. They also select one of four sector counters, one of four index pulses, and one of four sector pulses. SEL bits are decoded as follows:

SEL1	SEL0	Drive Selected
0	0	0
0	1	1
1	0	2
1	1	3

3. TAG 4 & TAG 5 - These bits are not used at the present time.

2.8.1.4 Load Track/Head Register (HEX 0106)

This command loads the contents of the BP data bus into the Track/Head Register. The Track/Head Register format is shown below.

TRK 7	TRK 6	TRK 5	TRK 4	TRK 3	TRK 2	TRK 1	TRK 0
D15							D8

TRK 9	TRK 8	HD 5	HD 4	HD 3	HD 2	HD 1	HD 0
D7							D0

The eight low order bits of this register represent the head byte of the header field. When setting up for a multisector operation which involves two adjacent heads, the lower of the two head addresses is loaded. The DA increments this head byte by one when servicing a sector on the upper head address.

The eight high order bits represent the track byte of the header field.

2.8.1.5 Load Write Latch (HEX 0108)

This command loads the contents of the BP data bus into the Write Latch. This loads a 16-bit data source when setting up for a write or verify operation with DMA inhibited (DMA EN bit not set). For a write operation, the data stored in the write latch is repeatedly recorded in the data field of each sector that is serviced. For a verify operation, the data stored in the write latch is repeatedly verified against the data read of the disk.

NOTE

The Command Register must be loaded before loading the Write Latch.

2.8.1.6 Load Operation Counter (HEX 010A)

This command loads the eight low order bits (D0-7) of the BP data bus into the operation counter. The operation counter is loaded during the set up of a surface operation with the 2's complement of the number of sectors to be serviced.

2.8.1.7 Deselect (HEX 010C)

For a SMD type drive, this command forces any drive selected to be deselected.

For a CMD type drive, this command will select the drive specified by the Select bits in the Tag Register.

Any one of the following conditions also force a deselect:

1. If a system initialization occurs.

2. If another controller seizes control of the selected drive. (This applies only to dual port drives.)

2.8.1.8 Reset (HEX 010E)

This command performs the following functions:

1. Initializes control logic.
2. Clears the FIFO buffer.
3. Clears the MAR.
4. Clears any operation status bits that are set.
5. Releases the stored last sector value. (Refer to paragraph 2.8.2.7.)

System initialization provides the same function as a Reset command.

2.8.1.9 Set Tag Strobe (HEX 0110)

This command loads BP data bus bits D0-D3 into the Tag Strobe Register. The Tag Strobe Register format is shown below.

UNIT	TAG	TAG	TAG
SEL	3	2	1
D3			D0

The Tag Strobe Register bit definitions are as follows:

1. Tag 1 - If this bit is set, then immediately reset, a Tag 1 strobe is sent to the selected drive. The drive interprets the Tag 1 strobe as a request to seek. The drive seeks to the cylinder address specified by the Tag Register.
2. Tag 2 - If this bit is set, then immediately reset, a Tag 2 strobe is sent to the selected drive. The drive interprets the Tag 2 strobe as a request to select a head. The drive selects the head specified by the Tag Register.
3. Tag 3 - If this bit is set, then immediately reset, a Tag 3 strobe is sent to the selected drive. The drive interprets the Tag 3 strobe as a control operation. The drive executes one of the following control operations defined by the Tag Register:
   a. Fault Clear (Bit 4 set)
   b. Return to Zero (Bit 6 set)
   c. Release (Bit 9 set)
   d. When executing a servo offset (Bit 2 or 3), Tag 3 must be set and remain set until the surface operation in offset mode has completed.
4. Unit Sel - If no drive is selected and this bit is set, and then immediately reset, a Unit Select tag is issued. The drive specified by bits SELO & 1 in the Tag Register is selected. If a drive is selected, a Deselect command must be issued before another Unit Select tag.

2.8.1.10 Load RAM (HEX 0311)

This command loads the contents of the BP data bus into the DA RAM. The RAM is addressed by the low order bit of the DA's MAR. The MAR is cleared by issuing a Reset command before loading the RAM. Each time a Load RAM command is issued the MAR increments by one.

When setting up for a surface operation, the RAM is loaded with a sector table. The sector table contains entries for each sector address. The number of entries in the sector table is determined by the number of sectors per track.

Once a surface operation has been initiated by issuing a Start command, the sector table in RAM is addressed by the selected drive's Sector Counter. The Sector Counter always points to sector table entry corresponding to the next sector to be entered.

The sector table entry format is shown below.

ADD 20	ADD 19	ADD 18	ADD 17	ADD 16	ADD 15	ADD 14	ADD 13
D15							D8

ADD 12	ADD 11	ADD 10	ADD 9	ADD 8	IXB	HDB	SOP REQ
D7							D0

The sector table entry bit definitions are as follows:

1. SOP REQ - If this bit is set, the next sector entered is serviced. If this bit is not set then no operation is performed in the next sector.

NOTE

The remaining bits in the sector entry have no meaning if the SOP REQ bit is not set.

2. HDB - Indicates which one of two possible heads on which the surface operation will be performed. If this bit is set, the head address that was loaded in the Track/Head Register is incremented by one. If this bit is not set, the head address remains as loaded in the Track/Head Register.

3. IXB - If this bit is set, the leading edge of the Index pulse will indicate that sector zero has been entered. If this bit is not set, the Index pulse will not indicate entering a sector. For the 9-sector/track format this bit will always be set to zero. For the 64-sector/track format this bit will be set to zero for all entries in the table except the sector zero entry.

4. ADD 8 thru ADD20 - This field contains the 13 high-order bits of the starting memory address for the next sector operation. The low order bits of starting address (ADD0-ADD7) are hardwired to 0.

NOTE

For surface operations with DMA inhibited, the address field of the sector entry has no meaning.

When setting up for an error correction operation, location 0 in RAM will be loaded with a HEX ED00 for a 2K byte sector size or HEX E980 for a 256 byte sector size. When the DA is in error correction mode, the RAM address will be forced to zero.

2.8.1.11 Enable Seek End Interrupt (HEX 0114)

This command is used to enable the Seek End interrupt. Once an interrupt occurs, the Seek End interrupt is reenabled.

A Seek interrupt is generated when any drive connected to the DA completes a seek operation. A drive does not have to be selected to generate a Seek interrupt.

If the DA attempts to select a dual port drive that is reserved by another controller, the drive notes the select attempt. If the other controller should release the drive, a Seek interrupt occurs at the DA that attempted earlier to select the drive.

2.8.1.12 MAR Clock (HEX 0118)

This command may be used for diagnostic purpose or for setting up the Memory Address Register (MAR) for an error correction operation. It issued to increment or load the MAR. If a MAR Clock command is issued with the COR (Correction Mode) bit in the Command Register not set, the MAR is incremented by one. If this command is issued with the COR bit set, the MAR is loaded. Address bits 8-20 will be loaded with the address field of the entry in location 0 of the DA's RAM. (Refer to paragraph 2.8.1.10.) Address bits 1-7 are loaded as show below:

AD7	AD6	AD5	AD4	AD3	AD2	AD1
0	1	0	0	1	1	0

2.8.1.13 Load FIFO (HEX 011A)

This diagnostic command loads up to 16 words in the DA's FIFO (First In, First Out) buffer. If the main memory address Read/Write bit in the Command Register is set, then the contents of the memory data latch is loaded into the FIFO. If the DMA R/W bit is not set, then the contents of the read latch are loaded into the FIFO.

2.8.1.14 Diagnostic Clock-1 (HEX 011C)

This diagnostic command performs the following functions:

1. Load the data on parallel inputs and outputs of the Serial Register into the Data Latch.
2. Load the contents of the BP data bus into the Memory Data In Latch. (DMA EN and DMA R/W bits in the command latch must not be set.)
3. Load the low order bits of the BP data bus (D0-7) into the ECC Reference Register.

2.8.1.15 Diagnostic Clock-2 (HEX 011C)

This diagnostic command is used only when simulating operations in the diagnostic mode (DIAG M1 bit set in the command latch). Diagnostic Clock-2 is used to sequence the operation instead of the usual servo and read clocks from the disk. Each time a Diagnostic Clock-2 is issued, one bit cell time of an operation is simulated.

2.8.2 READ COMMANDS

COMMAND	BP ADDRESS (HEX CODE)
Read Device Code	0100
Read Disk Status	0102
Read Operation Status	0104
Read ECC	0106
Read Disk Type	0108
Read Data	010A
Read Sector	010C
Read Operation Count	010E
Read MARL	0110
Read MARH	0112
Read FIFO	0114
Read PROM	0116
Read State Count	0118
Read Tag Register	011A

2.8.2.1 Read Device Code (HEX 0100)

This command places the contents of the Device Code Register on the BP data bus to be read by the BP.

The BP data bus format for the Read Device Code Register.

X	X	X	X	X	X	X	X
D15							D8

0	0	1	0	1	0	A1	A0
D7							D0

NOTE

X represents an unknown state.

The A0 and A1 bits define the number of drives that the DA can support as shown below:

A0	A1	# OF DRIVES
0	0	1
1	0	2
0	1	3
1	1	4

2.8.2.2 Read Disk Status (HEX 0102)

This command places disk status on the BP data bus to be read by the BP.

SEEK END 3	SEEK END 4	SEEK END 1	SEEK END 0	X	X	X	X
D15							D8

NOT SEL	BUSY	0	WRT PROT	FLT	SEEK ERR	ON CYL	UNIT RDY
D7							D0

NOTE

X represents an unknown state.

The disk status bit definitions are as follows:

1. UNIT RDY - This bit will set when the drive is ready. This indicates that the drive is up to speed, the heads are loaded, and there are no faults.

2. ON CYL - This bit sets when the heads are positioned over a track.

3. SEEK ERROR - This bit sets when a seek operation fails to complete the normal time period or an illegal cylinder address was given. A Restore command must be issued to clear this status.

4. FLT - This bit sets when any one of the following conditions occurs in the drive:

   a. DC voltage fault.
   b. Head Select fault (more then one head selected).
   c. Write fault.
   d. Write or read while off cylinder.
   e. Write gate during a read operation.

5. WRT PROT - This bit sets when the drive is in write protect mode. This indicates that write operations will be inhibited.

6. BUSY - This bit sets when the DA attempts to select a dual port drive that is reserved by the other port. This bit never sets when selecting a single channel drive.

7. NOT SEL - This bit sets when the DA is not selecting a drive.

8. SEEK END 0 - This bit sets when drive 0 is executing a Seek command. When the seek completes it is cleared. Drive 0 does not have to be selected for this bit to be set.

9. SEEK END 1 - Same as Seek End 0 but for drive 1.

10. SEEK END 2 - Same as SEek End 0 but for drive 2.

11. SEEK END 3 - Same as Seek End 0 but for drive 3.

2.8.2.3 Read Operation Status (HEX 0102)

This command places the operation status on the BP data bus to be read by the BP. The format of the BP data bus for a Read Operation Status command is shown below.

Z3	Z2	Z1	IN RDY	OUT RDY	LAST SEC	MEM ECC	IMA
D15							D8

DMA CHK	NULL	ECC	DCE	HCE	OVRN	CWPE	SOR
D7							D0

The data bus bit definitions are shown below.

1. SOR - Indicates a sector overrun error has occurred. Sector overrun means that the next sector was entered while performing a surface operation.

2. CWPE - Indicates that a parity error has been detected on the DA's control PROM.

3. HCE - Indicates an error has been detected in the header field during a write, read, or verify operation on the disk.

4. DCE - Indicates that an error has been detected in the data field during a verify operation on the disk.

5. ECC - Indicates that an error has been during a read or verify operation on the disk.

6. NULL - This bit sets after performing an error correction operation if the error is correctable. If this bit is not set at the completion of an Error Correction command, then the error is not correctable.

7. DMA CHK - This bit sets when entering a sector to be serviced if the FIFO is not empty or the previous DMA operation did not complete.

8. IMA - This bit sets if an illegal address is detected by main memory during a DMA operation. This bit is not used when the Data RAM is selected.

9. MEM ECC - This bit sets if an ECC error is detected by main memory during a DMA operation. If data RAM is selected, it sets when a DRAM parity error is detected during a DMA operation.

10. LAST SEC - Indicates entering the last sector of a multisector operation.

NOTE

When any one of the status bits listed above are set, the operation immediately terminates and an Operation Complete interrupt is generated.

11. OUT RDY - Indicates that the DA's FIFO buffer has data to sent out. It is used for diagnostic purposes and as an indication on Read operations with DMA that the DMA completed.

12. IN RDY - This bit sets when the DA's FIFO buffer is ready to accept data. It is used only for diagnostic purposes.

13. Z1 - Indicates that ECC bits EC1-EC7 do not compare with the contents of the ECC Reference Register. It is used only for diagnostic purposes.

14. Z2 - Indicates that ECC bits EC8-EC15 do not compare with the contents of the ECC Reference Register. It is used only for diagnostic purposes.

15. Z3 - Indicates that ECC bit EC17-EC23 do not compare with the contents of the ECC Reference Register. It is used only for diagnostic purpose.

2.8.2.4 Read ECC (HEX 0304)

This command places the ECC syndrome bits on the BP data bus to be read by the BP. The format of the Read ECC command is shown below.

X	X	X	X	PD 12	PD 11	PD 10	PD 9
D15							D8

PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1
D7							D0

NOTE

X represents an unknown state.

The ECC syndrome bits are used only after performing an error correction operation in which a correctable error was found. The BP corrects the bad data by exclusive ORing the bad data with the syndrome bits. (Refer to paragraph 2.8.4.) This command can also be used for diagnostic purposes.

2.8.2.5 Read Disk Type (HEX 0108)

This command places the contents of the Disk Type switches on the BP data bus to be read by the BP. The format of the BP data bus for a Read Disk Type command is shown below.

PORT 3				PORT 2			
DTB3	DTB2	DTB1	DTB0	DTB3	DTB2	DTB1	DTB0
3	3	3	3	2	2	2	2
D15							D8

PORT 1				PORT 0			
DTB3	DTB2	DTB1	DTB0	DTB3	DTB2	DTB1	DTB0
1	1	1	1	0	0	0	0
D7							D0

The disk type switches are divided into 4 groups. Each group represents a different disk port. The switch settings in each group indicate to the BP what type of disk drive is connected to each port.

2.8.2.6 Read Data (HEX 010A)

This command places the contents of the data latch on the BP data bus to be read by the BP. During surface operations the data latch is clocked at Bit time 8 (BT8) of each byte cycle. The high order half is loaded with the data on the parallel inputs to the Serial Register. The low order half is loaded with the data on the parallel outputs of the Serial Register. The data latch can also be loaded by issuing a Diagnostic clock.

If a header check or data compare error should occur, the expected byte is stored in the high order half of the data latch (D8-D15). The bad byte of data read off the disk is stored in low order half of the data latch (D0-D7). By reading the State Count and Timer it can also be determined which byte in the header or data field was bad.

2.8.2.7 Read Sector (HEX 010C)

This command places the contents of the Sector Register and the Operation Counter on the BP data bus to be read by the BP. The format of the Sector Register and the Operation Counter is shown below.

X	X	X	X	X	X	X	X
D15							D8

		SECTOR COUNT					
0	0	SB	SB	SB	SB	SB	SB
		5	4	3	2	1	0
D7							D0

NOTE

X represents an unknown state.

At the completion of a surface operation the Sector Register contains the last sector address serviced. This value is used when an error occurs during a multisector operation to determine on which sector the error occurred. Once a Reset command has been issued, the stored last sector address is released. The Sector Register indicates the current sector address of the selected drive.

2.8.2.8 Read Operation Count (HEX 010E)

This command places the contents of the Operation Counter on the BP data bus to be read by th BP. The format of the BP data bus for a Read Operation Count command is shown below.

X	X	X	X	X	X	X	X
D15							D8

OC 7	OC 6	OC 5	OC 4	OC 3	OC 2	OC 1	OC 0
D7							D0

NOTE

Where 'X' represents an unknown state.

At the completion of a surface operation without error the operation count should equal zero. If an error occurs during a multisector operation and the operation count is zero, then the error occurred during the last sector. This means that all other sectors were serviced without error.

If an error occurs and a residual count remains in the operation counter, then the error occurred in the middle of the multisector operation. The residual count is the 2's complement of the number of sectors that were not serviced because an error was encountered.

2.8.2.9 Read MARL (HEX 030C)

This command is used to place Memory Address Register bits 1-16 on the BP data bus to be read by the BP. The LSB (AD0), which is not read by this command is hardwired to 0.

2.8.2.10 Read MARH (HEX 030E)

This command places Memory Address Register bits 17-20 on the BP data bus to be read by the BP.

During the error correction operations the Memory Address Register is used to count ECC shifts. If a correctable error is detected, the count in the Memory Address Register indicates the starting location of the error in the data field. This count equals the number of bit positions in from the beginning of the data field to the error.

2.8.2.11 Read FIFO (HEX 0114)

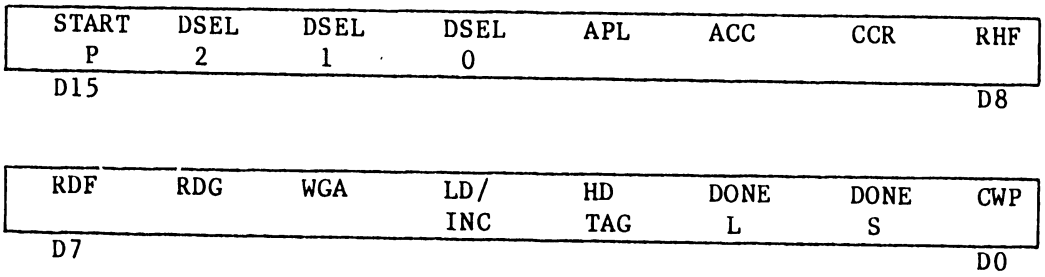
This diagnostic command unloads one word in the FIFO buffer onto the BP data bus to be read by the BP. The DMA EN bit in the Command Register must be set before issuing a Read FIFO command.

2.8.2.12 Read PROM (HEX 0312)

This diagnostic command places the contents of the Diagnostic PROM latch onto the BP data bus to be read by the BP.

The Diagnostic PROM latch is loaded with the contents of the PROM latch every BT7 time during load, surface, and diagnostic mode operations. The PROM latch controls the state of the disk interface control logic. When a surface operation terminates by generating an Operation Complete interrupt, the PROM diagnostic latch contains the last state of the last operation performed.

During a simulated operation when operating in Diagnostic mode (DIAG M1 SET) the contents of the PROM latch can be checked after each BT7 time by issuing a Read PROM command. The format of the Read PROM command shown below.



The Read PROM command bit definitions are shown below.

1. CWP - This is the parity bit for the entire PROM control word (CWO-CW23). The parity bit is set for odd parity.

2. DONE S - Terminates the current surface operation.

3. DONE L - Terminates the current load operation.

4. HD TAG - Activates the head select tag (Tag 2).

5. LD/INC - If this bit sets, the following events occur:

   a. The memory address bits AD8-AD20 are loaded with the contents of the address field in the sector table at BT1 time. Address bits AD1-AD7 are loaded with all 0's.
   b. The head byte from the Track/Head Register is loaded into the head address counter at BT1 time.
   c. If the HDB bit in the sector table is set, the head address counter is incremented by one at BT5 time.

6. WGA - If this bit is set and RDG was not active in the previous byte cycle, then Write Gate is immediately activated. If this bit sets and RDG was active in the previous byte cycle, then Write Gate is activated at BT5 time. If this bit clears Write Gate is immediately turn off.

7. RDG - Activates the Read Gate.

8. RDF - If this bit is set, the disk control logic is set up to read the data field of a sector. Setting this bit also changes the clock source used for timing and shifting data for Servo clocks to Read clocks.

9. RHF - If this bit is set, the disk control logic is set up to read the header field of a sector. Setting this bit also changes the clock source used for timing and shifting data from Servo clocks to Read clocks.

10. CCR - If this bit sets, the ECC Register and Serial Data Register are cleared.

11. ACC -

    a. For a write operation, if this bit is set, the serial ECC Register output data (PD12) is sent on the write data line to the disk. The Serial Data Register is also cleared. If this bit is not set, the Serial Data Register output (SDO) is sent on the write data line.
    b. For a read operation, if this bit is set, the loading of the read latch is inhibited.
    c. For a verify operation, if this bit is set, the clocking of the data compare error flip-flop is inhibited.

12. APL - If this bit is set, the Serial Data Register is loaded with the contents of the Data In bus (DI's) every BT8 time.

13. DSEL 0-2 - These bits make up a code that enables one of five data sources onto the Data In bus to the Serial Data Register.

    Decoding of DSEL 0 - 2:

DSEL2	DSEL1	DSEL0	DATA SOURCE
0	0	0	Sync Byte (HEX 01)
0	0	1	Track Byte
0	1	0	Head Byte
0	1	1	Sector Byte
1	X	X	Write Latch

NOTE

X indicates don't care.

14. START P - If this bit is set, the state timer be loaded at BT8 time. This bit is normally only set when the PROM latch is initialized. This bit is cleared on the first BT8 time of a load of surface operation.

2.8.2.13 Read State Count (HEX 0118)

This diagnostic command places the contents of the State Count latch onto the BP data bus to be read by the BP.

The State Count latch is loaded with the contents of the State Timer and State Counter every BT7 time during load and surface operations. When a surface operation terminates by generating an Operation Complete interrupt, the last state and timer count remain in the State Count latch. If a header or data compare error occurred, this count can be used to determine which byte was bad.

When simulating operations in the diagnostic mode, this command may be issued to verify that the operation is sequencing properly.

Format of the BP data bus for a Read State Count command is shown below.

STATE COUNT

0	0	0	SC 4	SC 3	SC 2	SC 1	S 0
D15							D7

TIMER COUNT

C 7	C 6	C 5	C 4	C 3	C 2	C 1	C 0
D7							D0

The State Count is used to address the PROM's. This counter is incremented at BT1 time only when the Timer Counter provides a carry out.

The Timer Counter is used to control the time period of each individual state of an operation. When a load or surface operation is initiated, the high order bits of the PROM control word (CW16-23) are loaded into the timer counter at BT8 time. This is a 2's compliment number equal to the time period (in byte times) of the first state. This count is incremented at each BT8 time until it generates a carry out.

When carry out sets, the state counter increments at BT1 time and at the next BT8 time the next state timer value is loaded. The next state is also loaded into the PROM latch. This sequence of events continues until the operation terminates by setting DONE L or DONE S. The state counter and timer both clear when the operation terminates.

2.8.2.14 Read Tag Bus (HEX 011A)

This command places the contents of the Tag bus on the BP data bus to be read by the BP. The format of the BP data bus for a Read Tag Bus command is shown below.

UNIT SELTAG	TAG 3	TAG 2	TAG 1	SEL 1	SEL 0	BIT 9	BIT 8
D15							D8

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
D7							D0

The Read Tag Bus command bit definitions are shown below.

1. BIT 0 thru BIT 9 - These bits are the Tag bus bits to the drive. They are normally controlled by BIT 0-9 of the Tag Register. Bit 0 is also set by Write Gate (WTG). Bit 1 is also set by Read Gate (RDG). During load operations with CMD3 in the Command Register not set, BIT 0-7 of the Tag Register is disabled. The head address counter is enabled in its place.

2. SEL0 & SEL1 - These bits represent the SEL0 & 1 bits from the Tag Register.

3. TAG 1 - This bit represents the Tag 1 bit from the Tag Strobe Register.

4. TAG 2 - This bit represents the Tag 2 bit from the Tag Strobe Register. It is also set by the HD TAG bit in the PROM latch.

5. TAG 3 - This bit represents the TAG 3 bit from the Tag Strobe Register. It is also set by signal SOP.

6. UNIT SEL TAG - This bit represents the Unit Select Tag to the drive. If the Unit Sel Tag strobe is set in the Tag Strobe Register, this bit is set. If the Unit Select Tag strobe is cleared this bit remains set if a drive was selected. If a drive was not selected it is cleared.

2.8.3 SURFACE OPERATION

A surface operation is an operation that transfers data to or from the disk drive. Data is recorded on individual sectors in the format shown below.

Pre amble	Sync Char	Head er	Write Splice	PLO Sync	Sync Char	Data	ECC	Pad	Gap

Sector field bit definitions are shown below.

1. Preamble - This field begins with the leading edge of sector pulse and contains all zero's. It is recorded to allow for head skew, other drive tolerances and for PLO sync time. This field is 33 bytes long for the nine sectors per track format and 27 bytes long for the 64-sector per track format.

2. Sync Character - This single byte always equals HEX 01. The sync character is used to enter into the header or data field.

3. Header - This field consists of three bytes; a track byte, a head byte and a sector byte. These bytes are used to give each sector a unique address (or header).

   a. Track Byte

TRK 7	TRK 6	TRK 5	TRK 4	TRK 3	TRK 2	TRK 1	TRK 0
MSB							LSB

b. Head Byte

TRK 9	TRK 8	HD 5	HD 4	HD 3	HD 2	HD 1	HD 0
MSB							LSB

NOTE

HD 4 indicates which volume is selected when a CMD type drive is selected. This bit is set to a one for sectors on the fixed disk and set to a zero for sectors on the removable cartridge. The head byte also contains high order track bits 8 & 9.

c. Sector Byte

0	0	0	0	SEC 3	SEC 2	SEC 1	SEC 0
MSB							LSB

4. Write Splice - This field represents the time between turning off read gate (after reading the header bytes) and turning on write gate to write the PLO (Phase Lock Oscillator) sync, sync char, data and ECC. The splice time is five bit times.

5. PLO Sync - This field is made up of all zero's and is used to allow time for the drive's PLO to sync up before reading the sync character. This field is 12 bytes long for the 9-sector per track format and 11 bytes long for the 64 sector per track format.

6. Data - This field contains 2K bytes of data for the 9-sector per track format and 256 bytes of data for the 64-sector per track format.

7. ECC - This field contains a 35-bit ECC code that is generated from the sync character and data field during a write operation.

8. Pad -This field is recorded with 13 bits of zeros before turning off write gate.

9. Gap - This field is not recorded during write and format (with data) operations. It begins at the end of the Pad field and ends at the leading edge of the next sector pulse. This field is approximately 126 bytes long for the 9-sector per track format and approximately nine bytes long for the 64-sector per track format.

2.8.3.1 Device Adapter Set Up for Surface Operations:

The following shows a typical sequence of events necessary for executing any surface operation.

1. Issue a Reset command.

2. Load the Tag register. (Refer to paragraphs 2.8.3.2 through 2.8.3.8.) If the Tag register was set up properly from the previous operation, then this step is not necessary.

3. Set Tag 3. (Only if reading or verifying in Offset mode.)

4. Load the Command Register with a value that defines the type of surface operation to be executed. (Refer to paragraph 2.8.1.2). If the type of surface operation is identical to the previous operation, then this step is not necessary.

5. Load the Operation Counter with the 2's complement of the number of sectors to be serviced.

6. Load the Track/Head register with the track and head address. If the Track and Head address is the same as the previous operation, then this step is not necessary.

7. Load the Write Latch with a 16-bit data pattern. (Only if executing a format with data, Write or Verify operation without DMA.)

8. Using the Load RAM command, load the sector table as shown below. (Nine sector per track format is shown)

	RAM ADDRESS	ENTRY FOR SECTOR
1st load	0	1
2nd load	1	2
3rd load	2	3
4th load	3	4
5th load	4	5
6th load	5	6
7th load	6	7
8th load	7	8
9th load	8	0
10th load	9	Note

NOTE

The 10th load is always a value of all 0's.

9. Issues a Start command. (If a Servo Offset was set up then wait for On Cylinder before issuing the Start.)

2.8.3.2 Format (without data field)

This command is used to record the preamble, header sync character, and the header bytes.

Bit 0 in the Tag register is set to a 1 and bits 1-9 to 0's before issuing this command.

2.8.3.3 Format (with data field)

This command is used to record a whole sector (header & data field) in the format shown in paragraph 2.8.3. Bit 0 in the Tag register is set to a 1 and bits 1-9 to 0's before issuing this command.

2.8.3.4 Write

This command is used to record data in a sector. A Write operation begins by reading and checking the header bytes. If the header bytes are correct, then write gate will be turned on and the PLO sync field thru the PAD field will be recorded. (Refer to paragraph 2.8.3.) Bits 0-9 in the Tag register must be set to 0's before issuing this com- mand.

2.8.3.5 Write (in ECC diagnostic mode)

This command is the same as the write command described in paragraph 2.8.3.4 except that the ECC field is not recorded from the remainder calculated on the DA. Instead, three extra words are read from memory (main memory or data RAM) and recorded in place of the ECC and PAD fields.

This command along with the Read (in ECC diagnostic mode) command is used to create ECC errors for the purpose of testing error detection and correction. Data read into memory during a Read (in ECC diagnostic mode) can be modified to create an error. It can then be rewritten onto the disk with the Write (in ECC diagnostic mode) command.

This command is executed with DMA. The DMA is modified for this command to allow the transfer of three extra words by setting ECC D1 in the Command Register. Bits 0-9 in the Tag register are set to 0's before issuing this command.

2.8.3.6 Read

This command is used to read the data field of a sector. A read operation begins with the reading and checking of the header bytes. If the header bytes are correct then the operation will go on to read the data and ECC fields. Bits 0, 1, 4-6, & 9 must always be set to 0's bits 2, 3, 7 & 8 will be set according to the table below:

BIT 8	BIT 7	BIT 3	BIT 2	TYPE OF OPERATION
0	0	0	0	Normal
0	0	0	1	Servo Offset Plus
0	0	1	0	Servo Offset Minus
0	1	0	0	Data Strobe Early
1	0	0	0	Data Strobe Late
0	1	0	1	Servo Offset Plus & Data Strobe Early
1	0	0	1	Servo Offset Plus & Data Strobe Late
0	1	1	0	Servo Offset Minus & Data Strobe Early
1	0	1	0	Servo Offset Minus & Data Strobe Late

NOTE

If the operation is performed in offset mode, the Tag 3 bit in the Tag Strobe register must be set. The Start command should not be issued until the drive goes on Cylinder. To release the offset, the Tag bit must be cleared. Another Start command must not be issue until at least 5 ms. after releasing the Offset.

2.8.3.7 Read (in ECC Diagnostic Mode)

This command is the same as the Read command described in paragraph 2.8.3.6, except that the ECC field is also written to memory along with the data field.

This command along with the Write (in ECC diagnostic mode) command is used to create ECC errors for the purpose of testing error detection and correction. Data that is read into memory can be modified and rewritten onto the disk with the Write (in ECC Diagnostic Mode) command.

This command is executed with DMA. The DMA is modified for this command to allow the transfer of 3 extra words by setting the ECC D1 bit in the command register.

Bits 0-9 in the tag register must be set to 0's before issuing this command.

2.8.3.8 Verify

This command is used to verify the data recorded on a sector. A verify operation begins by reading and checking the header bytes. If the header bytes are correct, the operation will go on to read the data and ECC fields.

The data read off the disk is compared one byte at a time against data read in from memory. If the operation is executed without DMA the data will be compared with the contents of the Write latch. If a Data Compare error is detected the operation will immediately terminate.

The Tag register bits should be set up as shown in paragraph 2.8.3.6.

2.8.3.9 Error Correction Procedure

If an ECC error occurs, the DA has the ability to correct error bursts up to 12 bits in length by using the following procedure:

1. Set the COR bit in the Command register.
2. Issue a Reset Command.
3. Load RAM with a HEX ED00 (for 2K byte sector size).
4. Issues a MAR Clock command.
5. Issue a Start command.
6. Wait for an Operation complete interrupt.

7. Read the Operation Status. If the Null bit is not set, the error is considered not correctable. If the Null bit is set, the error is correctable and the following steps are be performed:
   a. Issue a Read MARL command. The residual count in the MARL will indicate the starting location of the error burst in bit locations from the beginning of the data field.
   b. Issues a Read ECC command. The syndrome bit pattern is exclusive ORed with the bad data to correct it.

2.9 TELECOMMUNICATIONS DEVICE ADAPTER

The 25V76-1 single port Telecommunications (TC) option (figure 2-9) and the 25V76-2 dual port TC option (figure 2-10) are intelligent DAs which support RS-232C, X.21, or RS-449, program selectable modem line interfaces at speeds up to 19.2 kilobaud per second. The line encoding may be standard NRZ (Non Return to Zero) or NRZI (Non Return to Zero-One). An RS366 interface, standard for Automatic Calling Units (ACU), allows the 25V76 to originate a communication session.

These adapters can manage asynchronous, bisynchronous, and bit-oriented synchronous protocols and are flexible enough to support almost any protocol and line discipline. The adapter also supports bidirectional Direct Memory Access (DMA) on a 16-bit bus to the VS-25/45 main memory and the Bus Processor's Data RAM.

Because the 25V76 provides a wide range of line disciplines and link protocols, the following Large Scale Integration (LSI) components are used:

1. Z80A-Central Processing Unit (CPU)
2. Z80A-SIO/2 (Serial Input/Output)
3. Z80A-CTCs (Counter Timer Circuit)
4. 9517A-Direct Memory Access (DMA) controllers

The 25V76 will also use Medium Scale Integration (MSI) components to provide:

1. 128K bytes of Random Access Memory (RAM)
2. Memory Parity control
3. PROM I/D space decoder
4. VS-25/45 bus interfaces
5. X.21, RS-232-C, and RS-449 MODEM interfaces
6. RS-366 Automatic Calling Unit interface
7. Deadman timer
8. Status display panel
9. Power-Up Diagnostics

2.9.1 TC GENERAL DESCRIPTION

The central processing element (Z80A-CPU) shares a common bus with two 9517A-DMA controllers; a Line DMA controller and a Bus Processor (BP) DMA controller. The DMA allows high speed communications (up to 200 kilobytes per second) with very little system overhead. The CPU and both controllers rely on Bus Request/Bus Acknowledge protocol to synchronize exchange of the bus control.

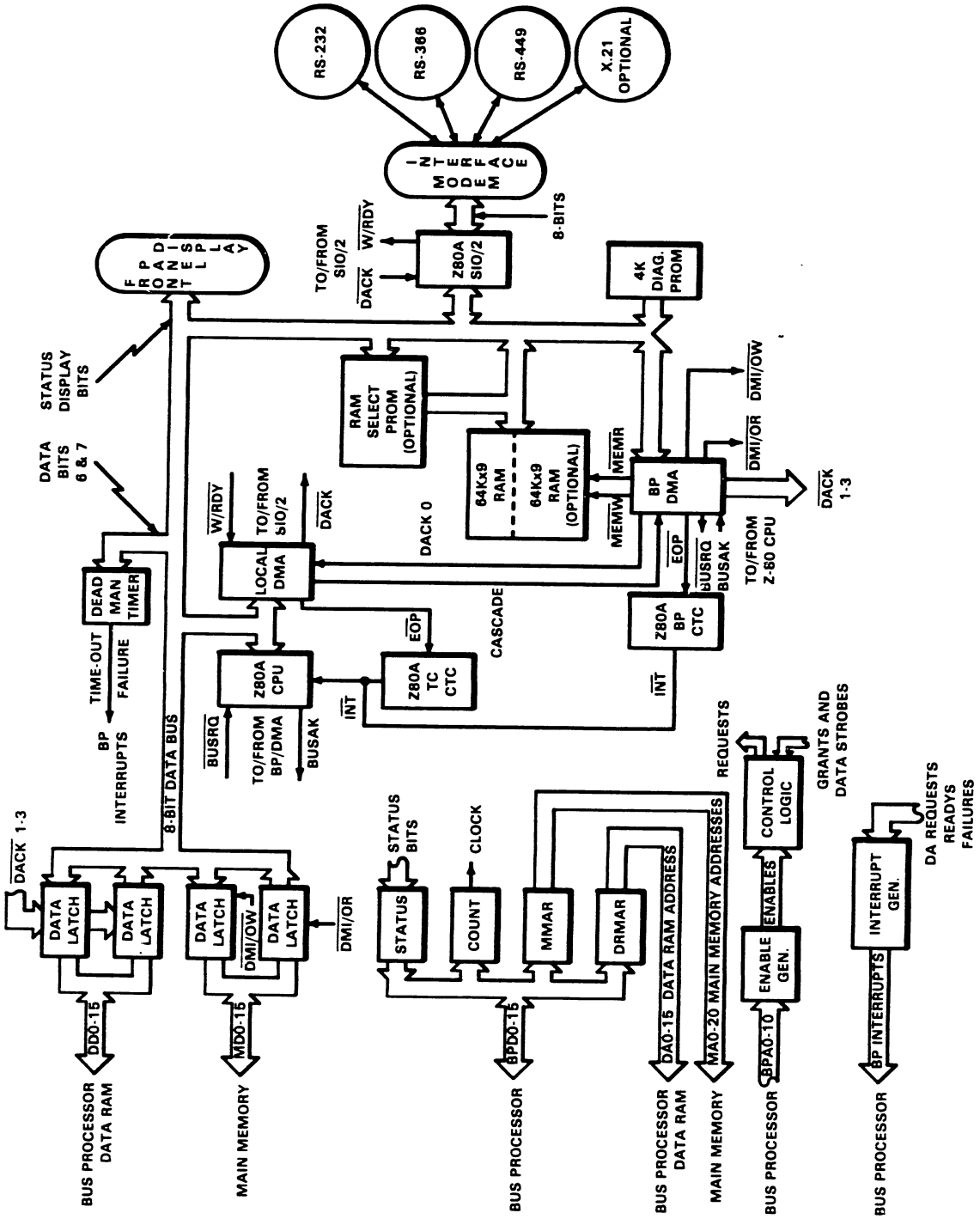


Figure 2-9. VS-25/45 Telecommunications Device Adapter Block Diagram

The Z80A-SIO/2, a programmable, dual-channel device, provides formatting of data for serial data communications. It is controlled by the CPU and/or the Line DMA controller.

The Z80A-CTC is a programmable four-channel device that provides counting and timing functions for the Z80A-CPU. One Z80A-CTC provides a BAUD rate clock, a timer, and Line DMA controller completion interrupts. A second Z80A-CTC provides a slow clock and BP DMA controller completion interrupts.

The Deadman timer ensures that the 25V76 will not "hang" the communications line in the event of a hardware or software fault. The timer will force Request to Send (RTS) into the inactive state if not reset by the system software every 0.5 seconds or less. The timer may optionally force the CPU into a nonmaskable interrupt service routine if the timer expires.

The Status Display Register provides signals to a LED display. This allows a variety of conditions to be displayed to the system operator. The BP can read this display to identify diagnostic or operating status.

2.9.2 TC/CPU FUNCTIONS

Under direction of the system software, the CPU controls all functions of the 25V76. Programming the SIO/2, CTC, and the DMA controllers is done by the system software by executing IN and OUT (I/O) instructions. The BP controls the Reset, Initial Program Load (IPL) functions, and DMA to the BP and through the BP Main Memory transfer Status/Control Registers.

The 25V76 memory is both the control storage and data storage for the CPU. The CPU control storage is loaded by the BP and execution begins at the address pointed to by CTC 2 channel 1 interrupt vector after a BP Restart command. If a Memory Parity Error (MPE), Deadman Timer expire, or Illegal PROM Address (IPA) Error is detected during execution, the CPU is optionally trapped by a nonmaskable interrupt regardless if any other maskable interrupts, and the BP is notified.

2.9.3 INSTRUCTION SPACE/DATA SPACE SELECTOR

The Instruction Space/Data Space (I/D) Selector Register is the control for operating the memory in I-mode (Instruction mode) only, D-mode (Data mode) only, or in I/D-mode. The bits in the register are encoded as follows.

	D0	D1	D2	D3-D7
I-Mode	X	1	X	X
D-Mode	X	0	1	X
I/D-Mode	1	0	0	X

The 25V76 memory space is divided into two 64K word x 9-bit (including parity) sections referred to as I-space (Instruction space) and D-space (Data space). In I-mode, the opcode fetches and data accesses (read or write) all take place in the I-space memory. In D-mode, the opcode fetches and data accesses all take place in the D-space memory. In I/D-mode, opcode fetches come from I-space memory and data accesses take place in D-space memory. Refresh is maintained in both memory spaces regardless of the operation mode because

the RAM must be rewritten at least every two milliseconds to retain data. This allows software to switch between modes without loss of data due to memory decay.

For DMA transfers, the data comes from I-space when in I-mode, and from D-space when in D-mode or I/D-mode.

2.9.4 OPCODE DECODE PROM

When software selects the I/D-mode of operation in the 25V76, a 2716 (2K byte) EPROM and associated circuitry are responsible for steering data to or from the correct memory space.

The 2716 decode PROM has the following internal structure:

PAGE	CODES FOR
0	Opcodes 00-FF
1	Maskable interrupt (Mode 2)
2	Nonmaskable interrupt
3	Unused page
4	X'CB' (dual M1 cycle instructions)
5	X'DD' (dual M1 cycle instructions)
6	X'ED' (dual M1 cycle instructions)
7	X'FD' (dual M1 cycle instructions)

NOTE

All unused locations contain a X'40' code, which indicates an illegal PROM address.

During an opcode fetch (M1 cycle), I-space is selected. The instruction opcode is read out of memory and sent to the inputs of a transparent Opcode Latch. The data is latched at the end of the Memory Request and provides an address to page 0 in the decode PROM.

At the end of the instruction cycle, the four low order bits of the PROM output code are loaded into a Bit-Shifter Register. Each following Memory Request shifts the bits out of the register providing a steering mechanism for the memory selection logic. Every time a 1 is shifted out, D-space is enabled, and when a 0 is shifted out, I-space is enabled. The next M1 cycle clears the Bit Shifter and the sequence is repeated.

The codes contained in the decode PROM were derived by examining each Z80 instruction and deciding where the next operation after the opcode fetch cycle is to take place.

If the instruction to be executed requires two opcode fetches, the PROM code addressed by the first opcode is used to change the selected PROM page. The second opcode is fetched and addresses the new PROM page which then transfers the appropriate code to the Bit Shifter.

Not all 256 HEX combinations are valid for the second opcode. If the second opcode is invalid, a special code is read out of the PROM and generates an Illegal PROM Address (IPA) Nonmaskable Interrupt. The IPA check is always enabled regardless of the memory mode in which the 25V76 is operating, thus providing a continuous verification of the second opcode.

Listed below are the M-cycle codes that are used throughout the opcode map.

CODL	DEFINITION
CDH	Operand data read of high byte
I/O	Internal CPU operation
MR	Memory read
MRH	Memory read of high byte
MRL	Memory read of low byte
MW	Memory write
MWH	Memory write of high byte
MWL	Memory write of low byte
OCF	Opcode fetch
ODL	Operand data read of low byte
PR	Port read
PW	Port write
SRH	Stack read of high byte
SRL	Stack read of high byte
SWH	Stack write of high byte
SWL	Stack write of low byte

2.9.5 9517A LINE DMA CONTROLLER

The Line DMA controller allows high speed data transfer between the SIO/2 and 25V76 memory. The CPU controls the function of the DMA controller through I/O instructions.

The SIO/2 Receiver (Channel A) and Transmitter (Channel B) are double buffered by the DMA controller and the associated circuits. Channels 0 and 2 support data input for the SIO/2 Receiver and are called the Receiver Channel pair. Channels 1 and 3 support data output for the SIO/2 Transmitter and are called the Transmitter Channel pair.

Table 2-21. SIO/2 Controls

Control	Type	Function
TxCA	Input	Internal Clock (IxC) derived from LCTC Ch
RxCa	Input	Receiver Clock, selectable Internal/External
DCDA	Input	Carrier Detect from MODEM (DCD)
RxDA	Input	Received Data from MODEM
RTSA	Output	Not Used
CTSA	Input	Ring Indicator (RI)
TxDA	Output	Looped back to RxDB
TxCB	Input	Transmitter Clock, selectable Int/Ext
RxCB	Input	Internal Clock (IxC)
DCDB	Input	MODEM Data Set Ready (DSR)
RxDB	Input	Looped back from TxDA
RTSB	Output	Request to Send (CTS) from MODEM
CTSB	Input	Clear to Send (CTS) from MODEM
TxDB	Output	Data Transmitted to MODEM
W/RDYA	Output	Request DMA Controller Channel 0/2 service
W/RDYB	Output	Request DMA Controller Channel 1/3 service
RESET	Input	Processor RESET

The Next and Current Channel Registers, one set of external registers for each DMA Channel pair, control the routing of the SIO/2 DMA requests to one of the channels in the pair. When an End Of Process (EOP) is signaled by the DMA controller for a particular channel pair, the Next Channel Register is copied into the Current Channel Register effectively switching to the next desired channel. In addition, CTC 1 will signal an interrupt for that pair.

This type of channel switching allows the system software to set the Next Channel Register to the inactive channel of that pair, program all the required register values for the next desired memory buffer, and then unmask the channel to wait for EOP on the active channel. When the EOP occurs, the Next is copied to the Current Register, W/RDYx (Write/Ready) is routed to the previously inactive channel, and future requests are honored by the newly selected channel.

The Line DMA controller options must be set for Late Write, DACK (Data Acknowledge) outputs active LOW, DREQ (Data Request) inputs inactive high, single byte transfer mode, and rotating DREQ priority.

CTC 1 Channels 2 and 3's Clock/Trigger inputs monitor the DMA Channel pairs 0/2 and 1/3, respectively, for an EOP. CTC 1 will request an interrupt if either of the inputs go low and provide the vector during interrupt acknowledge.

2.9.6 9517A BP DMA CONTROLLER

The BP DMA controller allows high speed data transfer between the VS-25/45 bus and 25V76 memory. The CPU controls the DMA controller functions through I/O instructions.

The BP DMA Channel 0 is cascaded to Line DMA Channel 0, so BP DMA, Line DMA, and CPU share a common bus and use Bus Request/Bus Acknowledge to synchronize exchange of the bus controls.

The BP DMA Channel 1 is a BP Message Receiver which receives the fixed bytes message from BP Data Ram to a fixed 25V76 memory location.

The BP DMA Channel 2 is used as DA Message Transmitter which transmits the fixed byte message from 25V76 memory to BP Data Ram.

The BP DMA Channel 3 provides all the data transfers between 25V76 memory and BP DRAM/Main Memory. A Byte Count Register, to keep counting down data bytes transferred, is external to the DMA controller.

CTC 2 Channel 1, 2, and 3 monitor the BP DMA Channel 1, 2, and 3 respectively for an EOP.

The BP DMA controller options are set for Extended Write, DACK outputs active LOW, DREQ inputs active high, single byte transfer mode, and routing DREQ priority.

2.9.7 SIO/2 FUNCTIONS

The SIO/2 converts data from 8-bit parallel format to one of several serial formats and vice versa. (Refer to table 2-20.) In addition, the SIO/2 performs character and line buffering, line control and status monitoring, and

error protection and detection. Both Synchronous and Asynchronous line disciplines are supported. Synchronous mode supports both Bit Oriented Protocols (BOP) and Character Oriented Protocols (COP). Asynchronous mode (Start/Stop) allows variable data, stop bit, and parity fields.

The CPU controls the SIO/2 functions by I/O instructions. The CPU may also select data line encoding, NRZ to NRZI conversion, and internal or external BAUD rate clock by Output to the Line Control Register.

Within the SIO/2, Channel A is configured as the Receiver and Channel B as the Transmitter. This configuration allows full duplex DMA operations by using the Wait/Ready function of each channel. Channel A DMA request may be sent to either Channel 0 or Channel 2 of the DMA controller. Also, Channel B may be sent to either Channel 1 or Channel 3 of the DMA controller. Channel A's Transmitter is looped back into Channel B's receiver for diagnostic use.

2.9.8 CTC FUNCTIONS

The CTCs provide the 25V76 with timing and counting functions, as well as providing Z80 interrupt mode 2 capabilities for the 9517A DMA controllers. The CTCs are programmed by the CPU and are mapped in the I/O space.

2.9.8.1 CTC 1

In CTC 1, Channel 0 is used to generate an Internal Clock (IxC) which may be sent to the SIO/2 Receiver and/or Transmitter. Channel 1 is used for software event timing. Channels 2 and 3 are used to alert the CPU of Line DMA (memory to or from SIO) completion.

Channel 0 may be programmed for either counter mode or timer mode depending on the desired BAUD rate. Channel 0 output rate is divided by two to produce a 50/50 duty cycle Internal Clock. This clock is supplied to the SIO/2, the RS-232-C interface (pin 11), CTC 1 Channel 1, and to the Internal/External Clock selector. The RS-449 interface may selectively emit, on the TT signal, either the external clock (ST) or the Internal Clock (IxC).

Channel 1 may be programmed for either timer mode or counter mode operation to generate an interrupt on each time-out. Timer mode allows a number of system clock cycles before generating each interrupt, while Counter mode counts a number of IxC clock cycles before generating each interrupt.

Channels 2 and 3 monitor the DMA controller's EOP signal for each Channel pair and are programmed for count mode operation to interrupt on a single failing edge of the Clock/Trigger input.

2.9.8.2 CTC 2

CTC 2 uses Channel 0 as a slow timer. The output of Channel 1 of CTC 1 is used as input to Channel 0 of CTC 2. When the CTC is in timer mode it allows a variable number of system clock cycles before generating each interrupt. Since CTC 1 Channel 1 in counter mode counts a number of IxC clock cycles before generating each interrupt, and CTC 2 Channel 0 can also run in the same mode, the slow timer can run at interrupt periods ranging from IxC to 256 times 256 times IxC when both are in counter mode. Thus an interrupt period as long as 54 seconds can be set up for the slow timer. With both fast and

slow timers in timer mode, the slow timer will generate an interrupt in 32ms after CLK/TRG1 of CTC 1 activates. In the timer mode, CTC will not start timing until it gets triggered.

Channels 1, 2, and 3 of CTC 2 are used to alert the CPU of BP DMA completion. They monitor the second DMA controller's EOP signal for channels 1, 2, and 3 respectively. These CTC channels are programmed for count mode operation to interrupt on a single falling edge of the Clock/Trigger input.

2.9.9 DEADMAN TIMER CONTROL REGISTER

The Deadman Timer Control Register contains two control bits to control the timer. The CPU controls the contents of the Deadman Timer Control Register which is mapped in the I/O space. The contents of the control register are all set at processor reset time. The control bits have the following configuration:

Table 2-22. Deadman Timer Control Register Format

Data Bit Position	Control Bit Name	Function
D0-05		Unused
D6	DNMI	Disables Deadman NMI Interrupt
D7	DDMT	Disables Deadman timer

2.9.10 DEADMAN TIMER

The Deadman timer prevents the communications line from being "hung" by the 25V76 in the event of a software or hardware failure. The CPU controls the Deadman timer functions through I/O instructions. Two control bits, DNMI and DDMT, are provided to select the timer options. The timer must be used whenever Request to Send (RTS) is to be sent to the modem. It may also be used as a general software time-out device to produce a nonmaskable interrupt. Once enabled, the timer is periodically reset by the system software at least every 0.5 seconds to prevent it's 0.7 second expiration time.

If DNMI is set to one, the CPU will not be interrupted regardless of the state of the Deadman timer. If DNMI is set to zero, the CPU will be unconditionally interrupted when the timer expires, via Nonmaskable Interrupt (NMI). The DNMI bit is set to one, disabling the NMI, before the DDMT is set to disable the timer. It is only reset after the DDMT is reset, to enable the timer.

DDMT enables the Deadman timer. Setting DDMT will stop the timer function and disable the RTS signal to the modem. If the NMI function is being used it is turned off before the timer is disabled. Resetting DDMT will start the timer and allow a RTS signal to be sent to the modem. If the NMI function is desired, it is enabled after the DDMT bit is reset.

2.9.11 25V76 INTERRUPT HANDLING

The 25V76 interrupt scheme is standard for the Z80A family except for the DMA controllers. The DMA controllers are not Z80 family components, but instead use channels of the CTC chips to signal interrupts. Data transfers be-

tween 25V76 and VS-25/45's bus are transparent to the CPU after DMA has been set up.

The 25V76 hardware is designed so that if an interrupt occurs while in I/D-mode, D-space is selected for the duration of the interrupt acknowledge cycle. This allows the contents of the program counter to be stored in data memory. During a maskable interrupt (Mode 2), the interrupt service routine address is also read from D-space.

The selection of D-space during an interrupt acknowledge is controlled by the Opcode Decode PROM and the associated circuitry. When a maskable interrupt occurs the acknowledge selects page 1 of the decode PROM. All 256 locations of page 1 contain the same code which is read out, loaded, and shifted through the Bit Shifter selecting D-space for the remaining memory accesses during the acknowledge cycle. When an NMI occurs, the NMI signal selects page 2 of the decode PROM. The code output from the PROM steers the program counter PUSH to D-space.

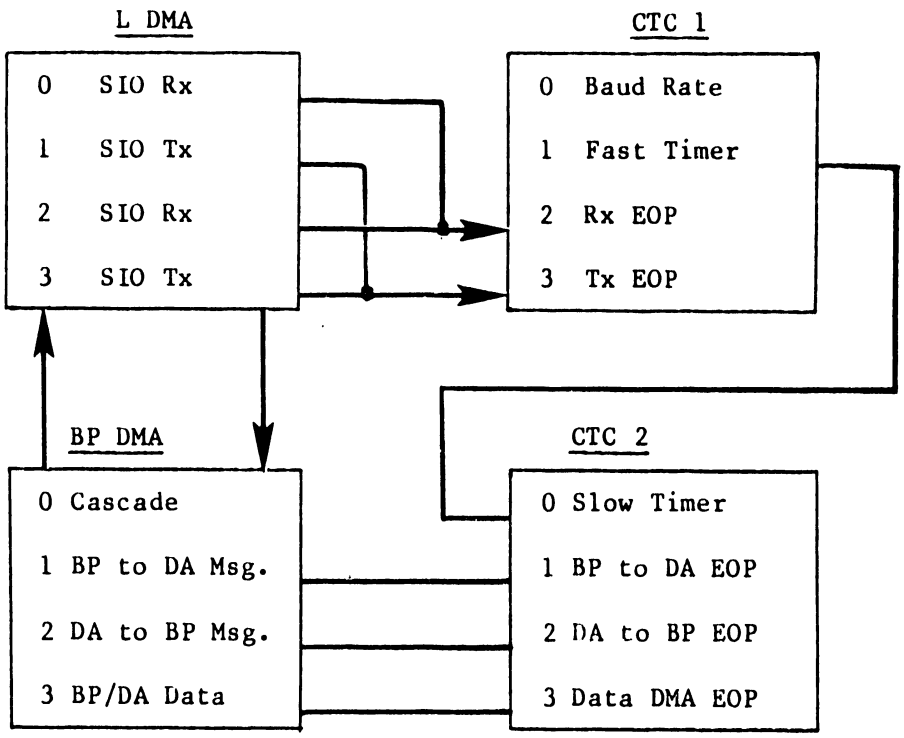
Vectored interrupts (MODE2) allow fast services and easy mapping of service routines through the use of a Vector table. The maskable interrupt priority, from highest to lowest, for each device is as follows:

Table 2-23. Vectored Interrupt Priorities

Highest	SIO	Channel A	Receiver
			Transmitter
			External/Status
		Channel B	Receive
			Transmitter
			External/Status
	L CTC	Channel 0	Baud Rate Clock
		Channel 1	Timer
		Channel 2	L DMA Controller 0/2 EOP
		Channel 3	L DMA Controller 1/3 EOP
	BP CTC	Channel 0	Slow Clock
		Channel 1	BP DMA Controller 1 EOP
		Channel 2	BP DMA Controller 2 EOP
Lowest		Channel 3	BP DMA Controller 3 EOP

2.9.12 TC-BP/DA DMA TRANSFERS

The figure below illustrates how the DMA and CTC chips are interconnected on the 25V76.



2.9.13 AUTOMATIC CALLING UNIT

The RS-366 Automatic Calling Unit (ACU) Interface allows the 25V76 to originate dialed calls. The CPU controls this interface through the I/O instructions. The modem signals RI or IC, and TM; and the Local Memory Parity Error Register (LMPE) are attached to the Status Register. The SF/RF modem signal (see RS-449) is attached to the control register as follows:

Table 2-24. ACU Register Format

Data Bit	0	1	2	3	4	5	6	7
Control	NB1	NB2	NB4	NB8	DPR	CRQ	ZERO	SF/RF
Status	ACR	PND	PWI	COS	DLO	RI/ RXDA	TM	LMPE

NOTES

1. SF/RF is active low, all the rest are active high.
2. RI is the signal RXDA in the X.21 interface.

2.9.14 LINE INTERFACE

The Line Interface Register allows the 25V76 to select Internal or External SIO/2 Receiver clock, Internal or External SIO/2 Transmitter clock (the

RS-449 signal TT is identical to the SIO/2 Transmitter clock), NRZ or NRZI line encoding, and X.21, RS-449 or RS-232C interface. The CPU controls the Line Interface Register through I/O instructions. Only data bits 0-3 are used, the others are set to zero. The Line Control Register format is shown below.

Data Bit	0	1	2	3 4
Control	RC EXT/INT	IC EXT/INT	NRZ/NRZI	RS-232-C/RS-449/X.21
Select	1 = EXT	1 = EXT	1 = NRZ	See table below

	D3	D4
RS-4499	0	0
RS-232-C	1	0
X.21	0	1
X.21	1	1

2.9.15 ADDRESS/STATUS SWITCHES

The Address/Status switches SW1 and SW2 enable the 25V76 to obtain configuration information. The eight switch settings are an address within a network or a status indicating an expected 25V76 operation. Therefore, the switch settings are software specified. The switch settings are obtained by a CPU IN instruction in the I/O space. The switch settings are shown in table 5-7.

All switch settings which have zero for the top four bits have been reserved for diagnostic use.

2.9.16 DIAGNOSTIC FUNCTIONS

The 25V76 provides several diagnostic functions. The Memory Parity Generator may be controlled by the CPU through OUT instructions. If the Memory Parity Generator is disabled:

1. Fixed Parity (a 1 bit) is written to memory for all subsequent memory write accesses.
2. The status of the MPE Failure is inhibited to the BP.
3. NMI is not sent to the CPU on LMPE error detection.

Local Memory Parity Error (LMPE) may be examined by a CPU Input instruction from the ACU Status Register. LMPE is cleared by an OUT instruction or RESET.

At Power-Up time, or by command of the BP, the Processor section is RESET and Memory is forced to I-mode. The 4K bytes of EPROM (2716) is mapped into the memory space at address X'0000'. Termination of the EPROM program will result in the processor being left in the state described in the Diagnostic Termination paragraph, 2.9.18.4.

When the diagnostics are completed the Status Display is set to indicate the 25V76 Status and the CPU exits Diagnostic Mode by an Output instruction. The EMPROM will be mapped out of the memory space and the CPU will be halted.

2.9.17 STATUS DISPLAY

The Status Display Register controls a LED display, mounted on the front panel, which allows a variety of conditions to be displayed to the system operator.

Table 2-25. TC DA Front Indicator Control Panel (Normal TC Operation)

INDICATOR NAME/TYPE	PURPOSE
LED1	Received Data
LED2	Transmitted Data
LED3	Clear-to-Send
LED4	Request to-Send
LED5	Carrier Detect
LED6	Data Terminal Ready
LED7	Data Set Ready
LED8	Power On

Table 2-26. TC DA Front Indicator Control Panel (Power-Up and IPL)

LEDS 1-7 CONDITIONS	LED 8 CONDITIONS	TC DA STATUS
All on	Blinking	Test running
All off	On	Test passed
Some on/some off	Blinking	Test failed

The display panel also provides two momentary contact switches: Disconnect, which clears the Data Terminal Ready Signal, and Clear, which generates Power-On Reset state for the DA.

2.9.18 TC-BUS PROCESSOR/DEVICE ADAPTER INTERFACE

Much of the VS-25/45 BP/25V76 Telecommunications Device Adapter hardware designs are based on the current BP/22V06 Telecommunications I/O Processor protocol. With three DMA Channels handling all the bus transfers, the DA can simultaneously communicate with MM and DRAM with little overhead to the DA CPU.

2.9.18.1 TC-BP to DA I/O Command

VS-25/45 BP I/O spaces are jumper selectable, the 12 pin jumper will allow the third bit of 25V76 I/O Address to range from 0 to 7.

2.9.18.2 TC Interrupt

INTO is the highest priority interrupt from the 25V76 to the BP. It is jumper selectable in corresponding to BP INT number 0,3,6,9,12, or 15. INTO is triggered upon a DA fatal error (i.e. MPE, IPA, and Timeout, or DA Request). In the BP interrupt service routine, the BP will read the Status Register to check which error caused the interrupt. When the DA request interrupt have been sent to the BP, a failure interrupt can not be generated until the DA Request situation goes away and vise versa.

INT1 is jumper selectable in respect to BP INT # 1,4,7,10,13 or 16. This interrupt happens only on the DA from BUSY state changing to READY state.

INT2 is the lowest priority interrupt from the 25V76 to the BP and also jumper selectable in respect to BP INT # 2,5,8,11,14, or 17. This interrupt is generated by BP DMA EOP1, BP DMA EOP2, or the Byte Count Register counting down to zero during the data passing cycle. On receiving this interrupt, the BP has to check with the Status Register in the DA to know either if a Message Passing EOP or a Data Passing EOP is complete and reset that particular latch to allow any pending interrupt to be generated.

2.9.18.3 TC Handshake Procedure Between BP and DA

When the DA has correctly set up the BP DMA, the following sequences are the steps BP must accomplish:

BP SEND MESSAGE TO DA

Wait until DA Ready
Set DRAM MAR
Enable BP Message Passing Control Latch Wait for INT2
Upon receiving INT2, check if it is Message Passing EOP Yes - Next step No - Continue waiting
Clear Message EOP Latch

DA SEND MESSAGE TO BP

Upon receiving INT0, check if it is DA Request Interrupt Yes - Next step No - Stop
Set DRAM MAR
Enable DA Message Passing Control Latch Wait for INT2
Upon receiving INT2, check if it is Message Passing EOP Yes - Next step No - Continue waiting
Clear Message Completion Latch

DATA TRANSFER

Write DA/MM MAR(s), set up byte count, Write Control Register to select data passing function (Read/Write DR/MM - data coming out of 25V76 and stored in DR/MM is a Write function).
Enable BP DMA Channel 3 Wait for INT2
On receiving INT2, check if it is Data Passing EOP Yes - Next step No - Continue waiting
Clear Data Completion Latch

After each bus transfer cycle, the BP will also read the Status Register to see if any Memory Parity Error (MIMA, MECC, DECC) has been latched during the transfer.

2.9.18.4 TC Diagnostic Termination

Upon successful completion of any diagnostic, certain steps are taken to insure proper conditions for DA microprogram loading. The diagnostic program insures DA components will be left in the states detailed below.

Disable all nonmaskable interrupting devices

Z-80 CPU

Interrupt mode 2 set
Stack pointer set to X'FFF0'
I-Vector (register) set to X'00'

DA RAM

Set to I-Space only
Parity enabled
Diagnostic PROM disabled

DMA HARDWARE

Interrupt vector for CTC2 Channel 0 set to X'0088'
CTC2, Channel 1 (BP to DA messages) a. Set for 12-byte transfer, starting at location X'0100' b. Interrupt to DA at End of Process (EOP)
CTC2, Channel 3 (VS main memory to DA RAM transfer) a. Set for 64 byte transfer, starting at location X'0000' b. No Interrupt to DA at End of Process (EOP)
Final instruction sequence (executed by diagnostic from RAM)
Exit Diagnostic Mode
Set DA ready status
Set Status LED SL8 ON for successfully completing diagnostics
Enable interrupts
Halt

CHAPTER 3 OPERATION

CHAPTER 3

OPERATION

3.1 GENERAL

This chapter provides the CE with tables listing all VS-25/45 main frame switches and indicators, daily turn-on and normal and emergency shut-down procedures. Included in this chapter are the procedures for using these switches and a brief statement on the purpose of each switch and indicator.

3.2 SWITCHES

Table 3-1 lists the switches found on the VS-25/45. Locations of the switches are shown in figures 3-1 and 3-2.

Table 3-1. VS-25/45 Switches

SWITCH NAME/TYPE	LOCATION	PURPOSE
AC POWER ON/OFF	Power Panel	Applies ac power to the CP main frame when in the 1 position.
DC INITIALIZE Pushbutton	Power Panel	Initializes switching power supply to apply dc power to Motherboard and drives.
CONTROL MODE Green Pushbutton	Front Panel	Forces system into Control Mode if Control Mode microcode is loaded.
INITIALIZE Red Pushbutton	Front Panel	Causes system to IPL from selected disk drive and system clock to be reset.
BOOTSTRAP MEDIA	Front Panel	Selects disk drive for cold-start or IPL. (Diskette, Quantum, or SMD.)
LOCAL/REMOTE Switch	Front Panel	Allows normal operation or connects VS25 /45 to modem for remote test with RDC.
DISCONNECT Pushbutton	TC Front Panel	Clear Data Terminal Ready Signal for TC Device Adapter
CLEAR Pushbutton	TC Front Panel	Generate Power On Reset state for TC Device Adapter
MEMORY SIZE DIP-Switch	7900 Main Memory board	Selects main memory size. Refer to paragraph 3.2.7.
BP SOFTWARE DIP-Switch	8304 BP board	Determines diagnostics mode or normal system operation. Read by the BP 8086. Refer to paragraph 3.2.8

3.2.1 POWER PANEL

The Power Panel, mounted on the front of the SPS450 Switching Power Supply, contains the ac power On/Off switch, ac Power On lamp, and the DC Initialize pushbutton. (See figure 3-1.)

Source-power is applied to the switching power supply directly from the ac input source. To turn on the system:

1. Depress the ac power On/Off switch to the 1 position. When the ac power On/Off switch is pressed, the Power On lamp is lit indicating

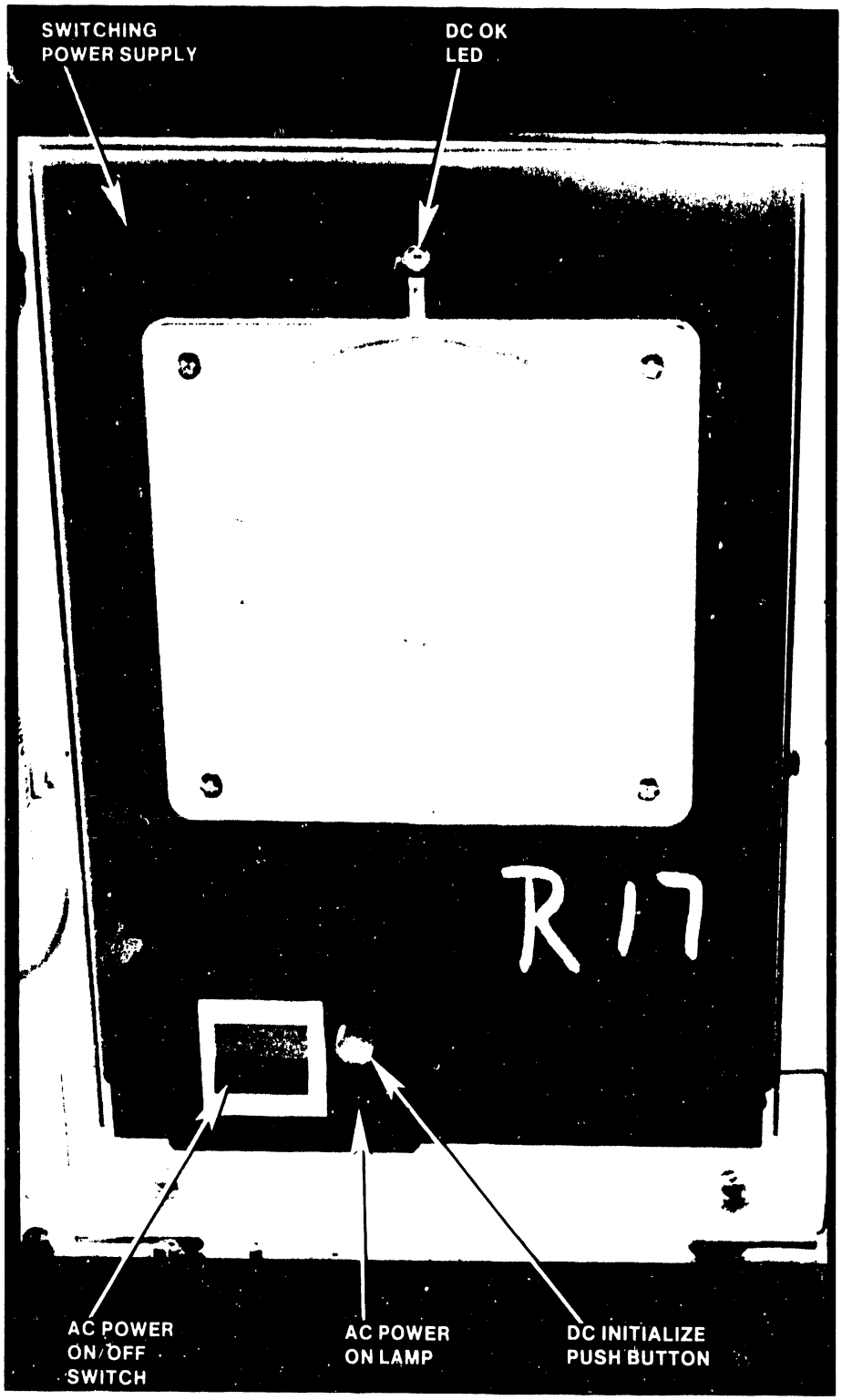


Figure 3-1. Power Panel Switches and Indicators

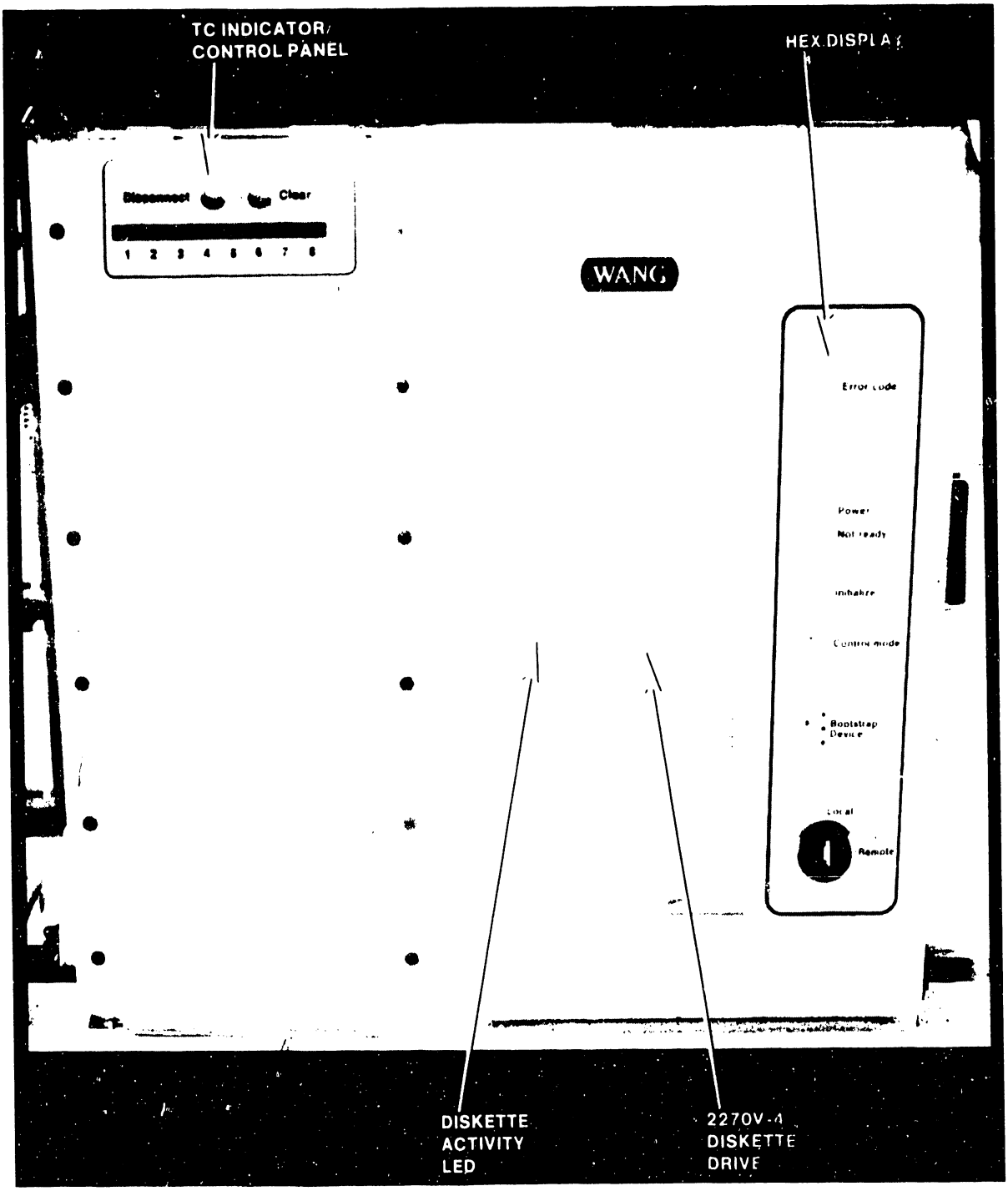


Figure 3-2. Front Panel Switches and Indicators

that ac power is being supplied to the switching power supply, cooling fans, diskette drive, and Quantum disk drive(s).

2. Wait 5 seconds after ac power is applied and then press the DC Initialize pushbutton. This turns on the switching power supply to provide dc voltages to the Motherboard and the internal disk drive(s). The DC Power On LED on the power supply, and the Power On LED and the four HEX displays on the Front Panel should light. If the LEDs do not light or the HEX displays go on and then go out within two seconds, a system power supply problem exists.

3. To remove power from the main frame, depress the ac power On/Off switch to the 0 position.

3.2.2 FRONT PANEL

The 210-7913 Front Panel board, located in the right-front corner of the main frame, contains several pushbuttons, switches and indicators, which allow the user to load system or diagnostic microcode, initialize the system, force the system into Control Mode, select a disk drive, and display system error status. (See figure 3-2.)

3.2.3 TC DA FRONT CONTROL/INDICATOR PANEL

The 25V76-1/2 TC DA Front Indicator/Control Panel (270-0814) is mounted on the VS-25/45 Front Panel (figure 3-2) to the left of the diskette drive. The panel contains 8 LED indicators and two pushbutton switches. The pushbutton switches are described in table 3-1. The TC DA status is indicated by the LEDs as described in tables 3-3 and 3-4.

3.2.4 CONTROL MODE PUSHBUTTON

Pressing the green Control Mode button sets the CM bit to one, forcing the CP into the Control Mode. The VS-25/45 Control Mode is similar in operation to the VS 60/80/100 Control Mode.

3.2.5 INITIALIZE PUSHBUTTON

Pressing the red Initialize pushbutton forces the system into the Initialized state. In this state, the system is as follows:

1. Main memory, Segment Control Registers (SCRs), and CP Reference And Change Table are all set to zero.
2. Page Table for Segment Zero (Operating System) is loaded into the T-Ram for access by the CP. Remaining T-Ram entries are faulted.
3. System Clock is zeroed and Comparator bits are set to one. As a result, the user must enter the date and time into the system whenever the system is initialized using the Initialize pushbutton.
4. BP-PROM receives control and is ready to start the bootstrap process.
5. BP checks BP Code RAM, BP Data RAM, and IPL disk drive interface. BP then loads microcode into the Data RAM, moves the microcode to Code RAM, and branches to execute the microcode.

3.2.6 BOOTSTRAP MEDIA SWITCH

The three-position Bootstrap Media switch enables the user to select the disk drive to cold-start or IPL the system. These three positions are:

1. Up - Select the Model 2270V-4 diskette drive.
2. Center - Select the system's internal Winchester disk drive(s).
3. Down - Select the SMD disk drive(s). (VS-45 systems only.)

3.2.7 LOCAL/REMOTE SWITCH

The two-position, key operated Local/Remote switch will allow normal system operation when it is in Local. When in Remote, it will connect the system to the Remote Diagnostic Center (RDC), via a modem and telephone line, for remote diagnostic operation. The RDC center will be able to read the Nonvolatile RAM or down-line run diagnostic packages already loaded on the system.

If the switch is in the Remote position, the system will not IPL. Turn the switch to the Local position and remove the key from the lock.

Because of its function as a diagnostic tool, a detailed description of the Local/Remote switch will be included in Chapter 8 of this document.

3.2.8 MEMORY SIZE SELECTION

Minimum memory size is 512K bytes and maximum main memory size is 1 Megabyte (1024K bytes). Memory can be increased in 256K byte increments until maximum memory size is reached.

A 5-position DIP switch (S1), located on the 210-7900 Main Memory board, determines the size of main memory. (See figure 5-4 for the location of the switch.) Table 5-1 provides information for determining switch settings for different memory sizes. Incorrectly altering the switch settings can result in the system refusing to IPL correctly.

The settings of switch S1 on the 210-7900 Main Memory board are compared with the high-order memory address bits (MA17-20) in the comparator chip at location L252. The SYSGEN procedure checks the switch and requests the size it reads regardless of whether the size is legitimate.

If the switch setting exceeds 1024K bytes and the address entered during the SYSGEN procedure does not exceed 1024K bytes, the system processes the address normally. If the switch setting does not exceed 1024K bytes and the address entered during the SYSGEN procedure does exceed 1024K bytes, the SYSGEN procedure requests the memory size parameter to be reentered.

However, if the switch settings are higher than the actual physical memory and that size is entered during the SYSGEN procedure, the memory address is accepted as legitimate and the CP attempts to process the address. This will result in the system hanging up during initialization or returning a "MACHINE CHECK CODE 001" (not enough memory for IPL) during initialization.

3.2.9 BP SOFTWARE SWITCH SETTINGS

An eight-position DIP switch, located on the 210-8304 BP board, is used by the 8086 microprocessor to determine the type of diagnostics to be run. (See figure 5-6 for the location of the switch.) Table 5-2 provides information for determining switch settings for diagnostic functions.

3.3 INDICATORS

Table 3-2, 3-3, and 3-4 lists the indicators found on the VS-25/45. Locations of the indicators are shown in figures 3-1 and 3-2.

Table 3-2. V3-25/45 Indicators

INDICATOR NAME/TYPE	LOCATION	PURPOSE
POWER ON lamp	Power Panel	Indicates ac Power On Switch activated. Ac power applied to switching power supply
POWER ON LED	Power Supply	Indicates dc power is ok.
POWER ON LED	Front Panel	Indicates dc power is ok.
NOT READY LED	Front Panel	When ON, power-up diagnostics are running. When OFF, system microcode is running.
HEX DISPLAY	Front Panel	Four hexadecimal displays for reporting system errors.
ISIO DIAGNOSTIC LED	ISIO Board	Indicates power-up diagnostics for the ISIO are running.

Table 3-3. VS-25/45 TC Device Adapter Front Indicator/ Control Panel (Normal TC Operation)

INDICATOR NAME/TYPE	PURPOSE
LED1	Received Data
LED2	Transmitted Data
LED3	Clear-to-Send
LED4	Request to-Send
LED5	Carrier Detect
LED6	Data Terminal Ready
LED7	Data Set Ready
LED8	Power On

Table 3-4. VS-25/45 TC Device Adapter Front Indicator/ Control Panel (Power Up and IPL)

LEDS 1-7 CONDITIONS	LED 8 CONDITIONS	TC DA STATUS
All on	Blinking	Test running
All off	On	Test passed
Some on/some off	Blinking	Test failed

3.3.1 HEX DISPLAY

The Front Panel monitors system error status and provides the user with information concerning the error condition of all I/O devices connected to the

main frame as well as data concerning the BP and CP status. The Front Panel has four HEX displays arranged in two rows of two displays each. Because of its function as a diagnostic tool, a detailed description of the HEX Displays is included in chapter 8 of this document.

3.3.2 POWER SUPPLY POWER ON LED

The Power On LED is located on the switching power supply chassis just above the fan. This LED indicates whether or not the correct voltages are being applied to the main frame. At initial power-up this LED lights as the voltages are applied to the main frame.

NOTE

Since the Power On LED's normal status is ON, a trouble condition exists when the LED is OFF. However, the LED indicates only that the voltages are present at the power supply, it does not indicate that actual voltages on the Motherboard are within limits.

3.3.3 ISIO DIAGNOSTIC LED

A single LED is mounted at the top of the ISIO board. The LED is on when the ISIO power-up diagnostics are running and will go out when the diagnostics have completed. If the diagnostics have failed, the LED will stay on.

3.4 SUPPORT MATERIALS

No special support materials are necessary for the VS-25/45 main frame.

3.5 DAILY POWER-UP PROCEDURES

After all peripherals are connected to the main frame, the daily power-up and power-down procedures for the VS-25/45 system are as follows:

1. Make sure that the main frame power connector is plugged into the power source receptacle.
2. Power up Workstation 0 and the primary disk drive.
3. Depress the main frame ac power On/Off switch to the 1 position.
4. Wait 5 seconds and then press the DC Initialize pushbutton located on the main frame Power Panel.
5. After the PROM-based power-up diagnostics have completed (the NOT READY light on the Front Panel has gone out), position the cursor on W/S 0 next to the IPL volume name and press ENTER. The Self-Test Monitor diagnostics (figure 4-16) will begin running. (See table 8-3 for diagnostic error code information.)
6. After the IPL Self-Test Monitor diagnostics have completed, enter the name of the configuration file and press ENTER.
7. Enter the date and time and press ENTER.
8. When System Initialization has completed, the VS Operators Console screen will appear and the system is ready for normal operation.

3.6 DAILY VERIFICATION PROCEDURES

Daily verification procedures are as follows:

1. Perform an IPL from the system disk.
2. Log on to a workstation and and run the WSDKTEST diagnostic located in @SYSTST@ library on the system disk.
3. If there are no errors cancel the diagnostic, log off the system, and let the customer resume normal daily operations.

3.7 DAILY POWER-DOWN PROCEDURES

CAUTION

IMPROPERLY POWERING DOWN THE SYSTEM AND/OR ANY DISK DRIVE CAN RESULT IN DAMAGE TO THE VOLUME TABLE OF CONTENTS (VTOC) OF THE DISK DRIVE(S).

1. Make sure all operators have logged off of the system.
   a. Press PF key 13 (WORKSTATIONs) on an operators console to check that the operators have logged off of the system.
   b. Press PF key 7 (NONINTERACTIVE Tasks) on an operators console to check the background tasks on the system. Look under the User column to identify any operator running a background task.
2. Press the green Control Mode button. This prevents any disk I/O command in process from being halted prior to completion.
3. Power down all peripheral devices according to procedures in the applicable documents in Class 3000.
4. Depress the main frame ac power On/Off switch to the 0 position.

3.8 EMERGENCY SHUT-DOWN PROCEDURES

In case of an emergency situation when the normal daily shut-down procedure can not be used, perform the following:

1. Press the green Control Mode button, if possible. This prevents any disk I/O command in process from being halted prior to completion and prevents possible damage to any disk VTOC.
2. Depress the POWER On/Off switch to the 0 position.
3. Disconnect the main frame power connector from the power source receptacle.

3.9 OPERATOR PREVENTIVE MAINTENANCE

No operator preventive maintenance is necessary on the VS-25/45 main frame.

CHAPTER 4

INSTAL-LATION

CHAPTER 4

INSTALLATION

4.1 GENERAL

This chapter describes the procedures for unpacking, inspecting, and installing the VS-25/45 main frame. Included in this chapter are instructions for system interconnection and initial power-up. Refer to Chapter 3, Operation, and Chapter 5, Preventive and Corrective Maintenance and Removal/Replacement, of this manual for more information needed to complete installation. Actual installation should not begin until the site requirements detailed in the following publications have been met.

DOCUMENT TITLE	WLI P/N
Customer Site Planning Guide	700-5978D
Systems Installation Guide for VS, 2200, and WP/OIS Systems	729-0907
VS Customer Planning and Resource Guide	700-6727

Plus any other pertinent documents in Class 1106.

4.2 INSTALLATION SITE CHECK

Prior to installation, the following conditions must have been met:

1. All site plans must have been approved by both the customer and a Wang service representative.
2. All building alterations must have been completed and inspected.
3. All electrical wiring, air conditioning, and telecommunications (TC) modifications must have been installed and tested.
4. If the installation is an upgrade only (CP replacement), the salesperson will make sure that serial peripheral devices replace all parallel peripheral devices.
5. The salesperson will also make arrangements to replace all 2260V 10-Mbyte Drives. These drives are NOT supported on the VS-25/45 system.

NOTE

It is the responsibility of the salesperson to make sure that an upgrade site meets all necessary VS-25/45 specifications.

6. The CE will perform a preinstallation inspection two weeks prior to delivery. At this time, the CE will check the site for compliance with VS site specifications. The CE will bring any unsatisfactory conditions noted to the attention of the customer for correction.

NOTE

Before installation of a VS-25/45 can take place, the minimum specifications as described in the previously listed publications should be met. Failure to meet these requirements can be cause for the installing CE to deem a site as unsuitable for the proper functioning of a VS-25/45 system.

4.3 TOOLS AND TEST EQUIPMENT

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022A	727-0119

4.4 UNPACKING

Before unpacking the VS-25/45, check all packing slips to make sure that the proper equipment has been delivered. Refer to the serial tag information below. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).

4.4.1 CLAIMS INFORMATION

If damage is discovered during inspection, file an appropriate claim promptly with the carrier involved, and notify:

WLI DISTRIBUTION CENTER
Department #90
Quality Assurance Department
Tewksbury, MA. 01876.

State the nature and extent of damage and make arrangements for replacement equipment, if necessary. Make sure to include this information:

WORK ORDER #_____
CUSTOMER NAME_____
CUSTOMER #_____
MODEL #_____
SERIAL #_____

Table 4-1. VS-25/45 Models

MODEL #	SERIAL TAG #	MEMORY SIZE	MAIN MEMORY P/N
VS25-8A	157/177-7131	512Kb	210-7900-3A
VS25-12A	157/177-7132	768Kb	210-7900-4A
VS25-16A	157/177-7133	1024Kb	210-7900-5A
VS25-8C	157/177-7168	512Kb	210-7900-3A
VS25-12C	157/177-7169	768Kb	210-7900-4A
VS25-16C	157/177-7170	1024Kb	210-7900-5A
VS45-8A	157/177-7176	512Kb	210-7900-3A
VS45-12A	157/177-7177	768Kb	210-7900-4A
VS45-16A	157/177-7178	1024Kb	210-7900-5A
VS45-8C	157/177-7181	512Kb	210-7900-3A
VS45-12C	157/177-7182	768Kb	210-7900-4A
VS45-16C	157/177-7183	1024Kb	210-7900-5A
VS45-8X	157/177-7171	512Kb	210-7900-3A
VS45-12X	157/177-7172	768Kb	210-7900-4A
VS45-16X	157/177-7173	1024Kb	210-7900-5A

NOTE

The serial tag number prefix for 50 cps ac line frequency machines is 157. The serial tag number prefix for 60 cps ac line frequency machines is 177.

4.4.2 TELECOMMUNICATIONS ADAPTER UPGRADE KIT

Upgrade kit (UJ), WLI P/N 177-7167, to install the Single Port Telecommunications Device Adapter will contain the following components:

COMPONENT DESCRIPTION	WLI PART NUMBER
SINGLE PORT TC DEVICE ADAPTER CARD	210-8337-A
FRONT INDICATOR/CONTROL PANEL CABLE	220-3247
FRONT INDICATOR/CONTROL PANEL	270-0814
REAR CABLE CONNECTOR PANEL	270-0824

Upgrade kit (UJ), WLI P/N 177-7216, to install the Dual Port Telecommunications Device Adapter will contain the following components:

COMPONENT DESCRIPTION	WLI PART NUMBER
DUAL PORT TC DEVICE ADAPTER CARD	210-8637-A
FRONT INDICATOR/CONTROL PANEL CABLES	220-3012
FRONT INDICATOR/CONTROL PANELS	270-0814
REAR CABLE CONNECTOR PANEL	270-0825

Internal cables, connecting the TC DA to the Rear Cable Connector Panel, will be supplied in the Connector Interface Option (CIO) ordered with the upgrade kit. Part numbers for the Connector Interface Options are listed below.

CIO OPTION DESCRIPTION	WLI PART NUMBER
RS-232 & CCITT/V.24	220-3244
RS-336 & CCITT/V.25 *	220-3244
X.21	220-3245
RS-449	220-3246

* - Required for auto-dial capability using Bell 801 or similar modems. Part numbers for TC Interface cables (ordered separately), connecting the Rear Cable Connector Panel to the modem, are listed below.

INTERFACE CABLE DESCRIPTION	LENGTH	WLI PART NUMBER
RS-232 & CCITT/V.24 (25-PIN)	12 FEET	220-0332
" " " / " " "	25 "	220-0333
" " " / " " "	50 "	220-0334
RS-336 & CCITT/V.25 (25-PIN)	12 "	220-0332
" " " / " " "	25 "	220-0333
" " " / " " "	50 "	220-0334
X.21 (15-PIN)	12 "	220-0274
" " "	25 "	120-2326-01
" " "	50 "	120-2326-02
RS-449 (37-PIN)	12 "	220-0248
" " " "	25 "	120-2325-01
" " " "	50 "	120-2325-02

4.4.3 SMD ADAPTER UPGRADE KITS

The adapter is offered in four versions.

The upgrade kit(s) (UJ) to install the SMD DA will contain the following components:

UPGRADE KIT DESCRIPTION	WLI PART NUMBER
1-PORT SMD DEVICE ADAPTER KIT	177-7162
2-PORT SMD DEVICE ADAPTER KIT	177-7163
3-PORT SMD DEVICE ADAPTER KIT	177-7164
4-PORT SMD DEVICE ADAPTER KIT	177-7165

Each upgrade kit(s) will contain the following components:

DESCRIPTION	WLI PART NUMBER
SMD DISK ADAPTER CARD	See below
SMD REAR CABLE CONNECTOR PANEL	270-0702

WLI PART NUMBER	VERSION
210-8312	1-PORT
210-8313	2-PORT
210-8314	3-PORT
210-8315	4-PORT

Each adapter version cannot be upgraded to support additional drives.

4.4.4 UNPACKING THE MAIN FRAME

1. It is suggested that some assistance be available to help unpack the main frame cabinet.
2. Cut the strapping that secures the top cover and outside tube to the cushion pallet. (If the strapping is metal, be careful that it does not spring out and away from the shipping container.)
3. Remove the top cover, corrugated/foam top cushion, and outside tube. (See figure 4-1.)
4. Remove the four corner shipping bolts securing the VS-25/45 cabinet to the cushion pallet.
5. Remove the two foam and wood support blocks from under the main frame cabinet.
6. Slightly loosen the two nuts on the cushion pallet feet at the front of the pallet.
7. Remove the two nuts from the cushion pallet feet at the rear of the pallet.

WARNING

The main frame cabinet weighs approximately 250 pounds. Be careful when performing the following steps.

8. While firmly grasping the rear top of the cabinet, lift the cushion pallet up over the right cushion pallet foot bolt and partially swing the foot out away from the pallet. (See figure 4-2.)
9. Repeat the previous procedure for the left cushion pallet foot.
10. Alternate steps 9 and 10 while lowering the cushion pallet until it is resting on the floor.
11. Carefully roll the VS-25/45 main frame cabinet off the rear of cushion pallet. (See figure 4-3.)
12. Move the CPU cabinet to its permanent location and remove the top and front covers. (Refer to paragraphs 5.2 and 5.3 for disassembly procedures.)
13. Turn the two front leveling pads down until they support the cabinet.
14. Adjust the leveling pads to align the unit with adjacent equipment. Make sure the cabinet is level with no detectable rocking motion,
15. Once the cabinet is in place, check the service clearances as listed below.

SERVICE CLEARANCES	INCHES	CENTIMETERS
Front	36	91.4
Rear	24	60.9
Left	0	0
Right	0	0
Top	20	50.8

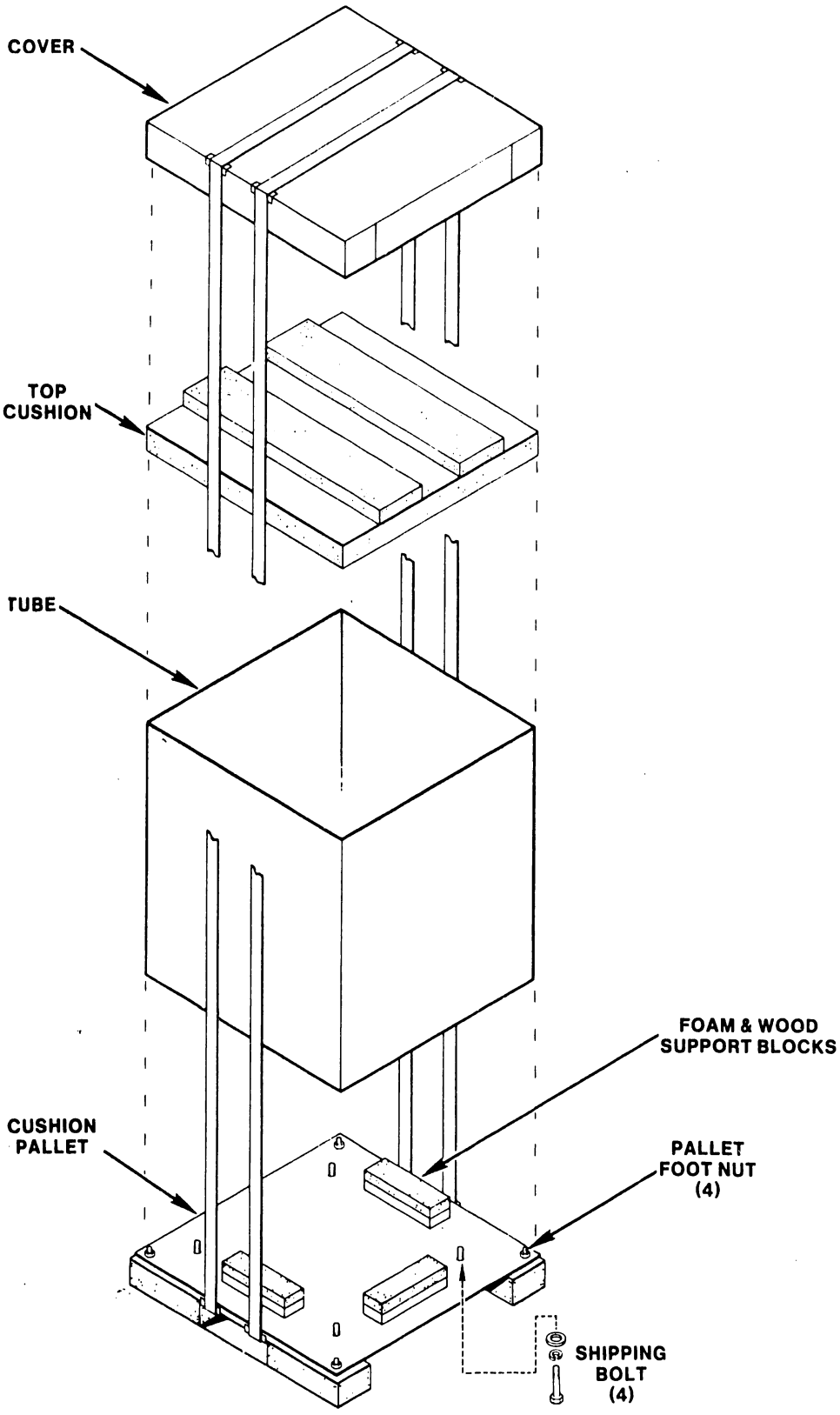


Figure 4-1. VS-25/45 Shipping Carton

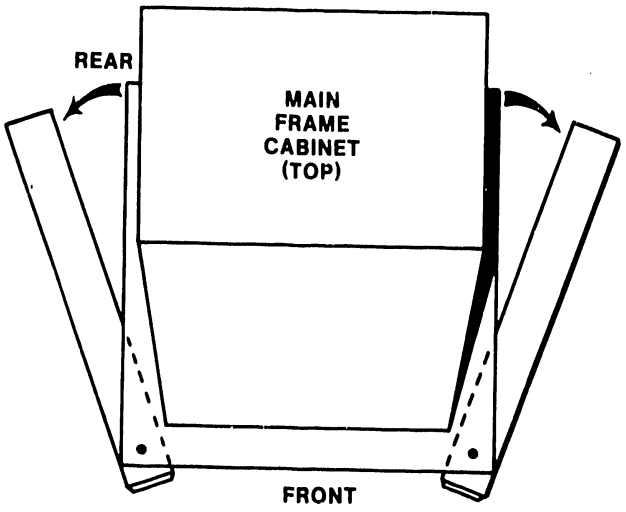


Figure 4-2. Swinging Cushion Pallet Feet

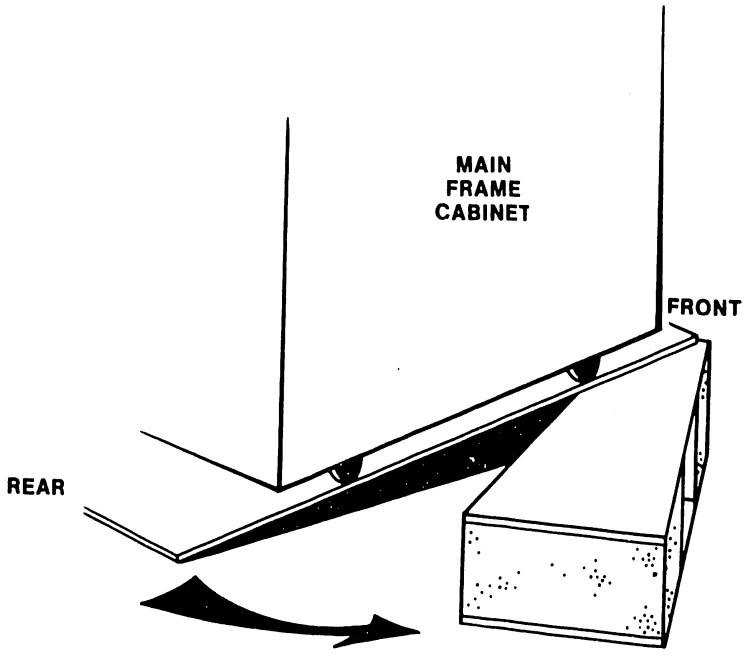


Figure 4-3. Rolling Cabinet Off Cushion Pallet

4.4.5 UNPACKING THE PERIPHERALS

Before proceeding, carefully unpack all peripherals according to procedures outlined in applicable maintenance manuals in Class 3000. As each unit is unpacked, check it for any obvious shipping damage.

4.5 MAIN FRAME INSPECTION

NOTE

New quality assurance procedures and tests have shown that VS CPUs arriving on the customer's premises require only visual inspection, voltage checks, software loading, and cabling. Therefore, the following new inspection and installation procedures for all VS CPU products are effective immediately.

DO NOT REMOVE PRINTED CIRCUIT BOARDS FOR INSPECTION

DO NOT CLEAN PRINTED CIRCUIT BOARD CONTACTS WITH AN ERASER

INSPECT CPU MAIN FRAME VISUALLY

REPORT INSTALLATION PROBLEMS ON THE INSTALLATION REPORT AND STATE SPECIFIC CAUSES OF FAILURE

To make sure of the integrity of the equipment, a detailed internal inspection must be performed before final installation of the system. Perform an internal inspection of the main frame, as follows: (See figure 4-4.)

1. Inspect the interior of the main frame for packing material or such shipping damage as broken connectors and loose fastening hardware.
2. Refer to the shipping list to make sure that the correct circuit boards have been shipped. Refer to paragraph 4.6.1 for the minimum hardware revision levels.
3. Make sure that the System Identification (I.D.) PROM is installed at location L228 on the 210-8303 CPU board. The serial number written on the I.D. PROM should match the system serial tag number located on the rear panel.
4. Carefully inspect the motherboard and fans for obvious damage or loose connections.
5. Inspect the power supply assembly for damage and loose connections. At this time, make sure that all power supply connections are tight.
6. If necessary, vacuum clean the unit.
7. Do not reassemble the main frame at this time.
8. If damage is discovered at any time during the inspection, follow the reporting procedure in paragraph 4.4.1.

4.5.1 PERIPHERAL INSPECTION

After inspecting the main frame, carefully inspect each peripheral according to procedures outlined in the applicable maintenance manuals in Class 3000. If damage is discovered at any time during the peripheral inspection, follow the reporting procedure in paragraph 4.4.1.

4.6 MINIMUM REQUIREMENTS

4.6.1 HARDWARE

WLI PART NUMBER	DESCRIPTION	REVISION LEVEL
210-7900-3A	512 Kbyte Main Memory board	1
210-7900-4A	768 Kbyte Main Memory board	1
210-7900-5A	1 Megabyte Main Memory board	1
210-8303	CPU board	0
210-8304-A/1A	Bus Processor board	6
210-7906	32-Port SIO DA	2
210-8616	32-Port Intelligent SIO DA	NOT RELEASED
210-8325	Quantum Drive DA	3
210-8312	1-Port SMD Disk DA	3
210-8313	2-Port SMD Disk DA	3
210-8314	3-Port SMD Disk DA	3
210-8315	4-Port SMD Disk DA	3
210-8337	1-Port Telecommunications DA	1
210-8637	2-Port Telecommunications DA	NOT RELEASED
210-7913	Front Panel board	R1
210-7907	Main Frame Motherboard	R1

4.6.2 COLDSTART PACKAGE

The 5.03.70 Operating System Coldstart package, WLI P/N 195-2453-5, contains diskettes and documentation. The following list contains the part numbers of the individual diskettes.

SOFTWARE DESCRIPTION	VERSION	COMMENTS	WLI P/N
Format	5.03.70		735-0041C
SYSTM1	5.03.70		735-0042C
SYSTM2	5.03.70		735-0043C
SYSTM3	5.03.70		735-0044C
MACLIB	5.03.70		735-0045C
WSCODE	5.03.70		735-0046C
PRCODE	5.03.70		735-0047C
UTLTY1	5.03.70		735-0048C
UTLTY2	5.03.70		735-0049C
NVRAM Utilities	8350	Load/Show NVRAM	732-0032

The 6.10 Operating System Coldstart package, WLI P/N 195-2456-5, contains diskettes and documentation. The following list contains the part numbers of the individual diskettes.

SOFTWARE DESCRIPTION	VERSION	COMMENTS	WLI P/N
Format	6.10		735-0068
SYSTM1	6.10		735-0069
SYSTM2	6.10		735-0070
SYSTM3	6.10		735-0071
SYSTM4	6.10		735-0072
UTLTY3	6.10		735-0075
MACLIB	6.10		735-0076

6.10. Operating System Coldstart Package (cont'd)

SOFTWARE DESCRIPTION	VERSION	COMMENTS	WLI P/N
WSCODE	6.10		735-0077
PRCODE	6.10		735-0078
NVRAM Utilities		Load/Show NVRAM	735-0079
UTLTY1	6.10		735-0073
UTLTY2	6.10		735-0074

4.6.3 DIAGNOSTIC PACKAGES

The Stand-Alone Diagnostic Monitor package, WLI P/N 195-2458-5, contains the following diagnostics:

TEST ID	TEST NAME	VERSION
CT1000	CP Control Memory	1334
CT2000	BP/CP Communication	1334
CT3000	BU Branch Opcode	1334
CT4000	Status, Conditional Branch	1334
CT5000	Subroutine Stack Data	1334
CT6000	Subroutine Stack Addressing	1334
CT7000	Register, Immediate Opcodes	1334
CT8000	CPU Stack Diagnostic	1334
CT9000	Logical and Shift Opcodes	1334
CTA000	8-Bit and 16-Bit ALU Test	1334
CTB000	MAR, TRAM, and RCT Test	1334
CTC000	BD, IAD, CC, and DSET Test	1334
CTD000	BI Branch Opcode Test	1334
CPTSTR	CPU Tester	1334
MT1000	Main Memory Test	1334
BT2000	DMA Test	1337
BT3000	SA850 Floppy Disk Diagnostic	1354
QT1000	Q2040 Quantum DA Diagnostic	33C
DT1000	CMD/SMD Disk DA Diagnostic	1334
BT1000	USART/Modem Diagnostic	1354
BT5000	Bus Processor Diagnostic (NVRAM)	1354
TT1000	Telecommunications DA 1-Port	1334
TT2000	Telecommunications DA 2-Port	1334
ST1000	Dumb 928 (SIO) Data Link DA	1330
ST2000	Smart 928 (ISIO) Data Link DA	1330
BT4000	VS25/45 Multitasker	6354

OTHER DIAGNOSTICS

DIAGNOSTIC NAME	VERSION	WLI P/N
22V06 Local Loopback Test (TCIOPTST)	1130	702-0132A
Boot Loader	82C8	195-7479-3
Device Monitor	21A0	702-0175
FTU45		732-0026
FTU On-Line	6365	195-2652-3
TPTEST	6224	702-0187
VS On-line Printer Monitor, Part I	2242	702-0179A
VS On-line Printer Monitor, Part II	2211	702-0178

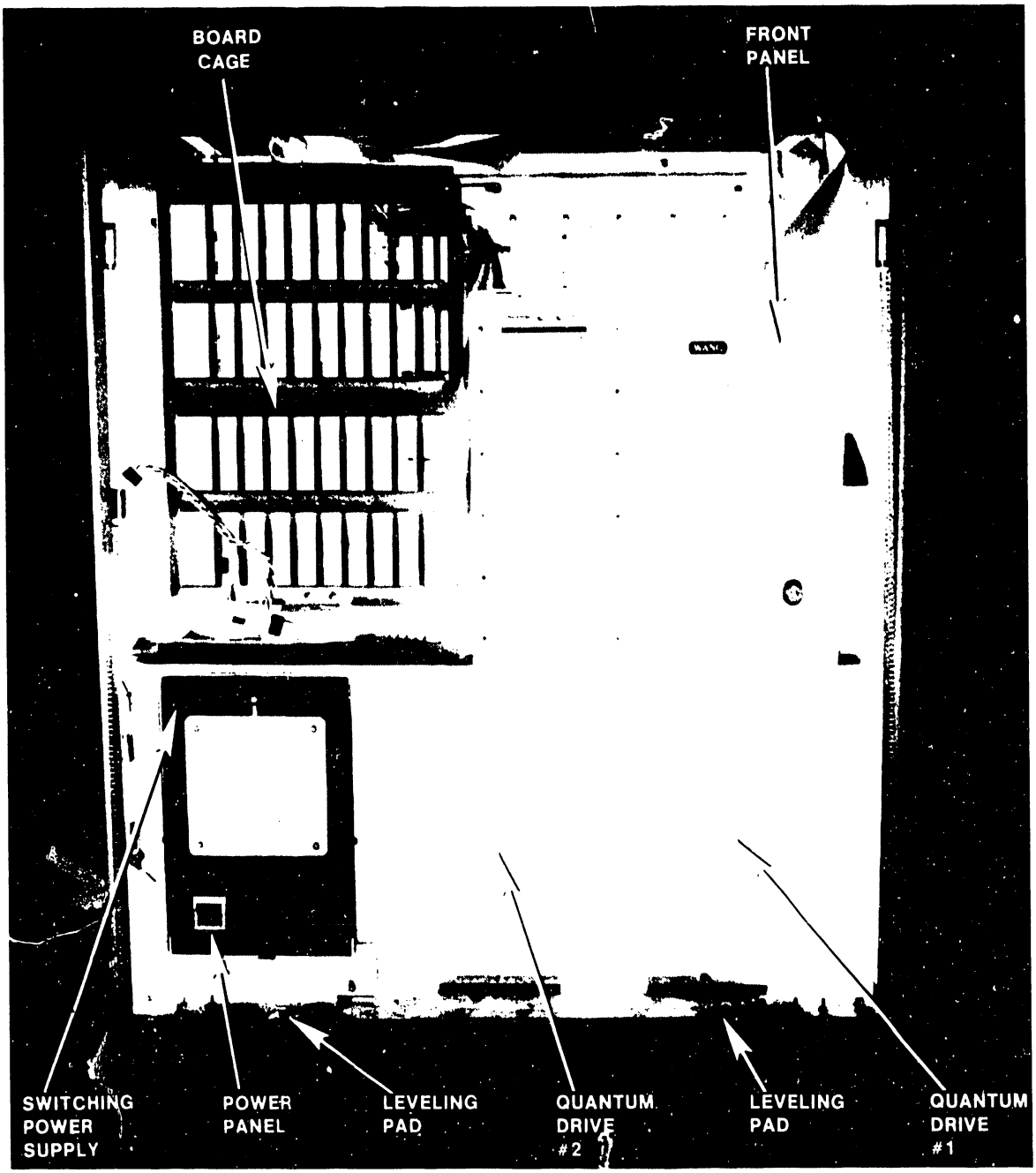


Figure 4-4. VS-25/45 With Top and Front Covers Removed

4.7 QUANTUM DRIVE INSTALLATION

1. Quantum drive #1 is the right hand drive and drive #2 is the left hand drive. The drive(s) is bolted to the cabinet by one 5/16 inch hex bolt at the front of the drive(s) which is secured by a "pem" nut under the cabinet. Remove the hex bolt while holding the "pem" nut under the cabinet.
2. Carefully slide forward and inspect the Quantum drive. The "A" and "B" signal, and ac and dc power cables are connected to the rear of the drive.
3. On the right side of the drive, loosen the 11/32 inch hex nut securing the locking clip on the Quantum drive pulley (figure 4-5).
4. Rotate the locking clip away from the pulley.
   DO NOT ROTATE THE PULLEY.
5. Retighten the 11/32 inch hex nut.
6. Unlock the actuator (figure 4-6) by rotating the actuator lock counterclockwise as far as it will go (approximately 1/2 turn). The embossed arrow will now point to RUN.
   DO NOT FORCE THE ACTUATOR.
7. Before installing the drive, check the options jumpers and terminator IC on the Quantum Drive Control PC board (Quantum #20-2000). They should be installed as follows. (See figure 4-7.)
   a. Minus (-) power selection to the -15vdc connection.
   b. Rezero selection between pin C and pin 5.
   c. Drive Select to the appropriate DS pin. If the drive is to be #1, install the jumper on DS1; if the drive is to be #2, install the jumper on DS2. DO NOT jumper pin A. This will cause the drive to be selected constantly.
   d. Seek Complete (SK COMP) between pin D and pin 1.
   e. Type 7438 terminator IC installed at location 6J of last drive.
8. Make sure the signal and power cables are still connected to the rear of the drive as follows: (Refer to table 5-3.)
   a. For two drives, the "A" cable is daisy chained from the 210-8325 DA board to J1 of drive #2 and then to J1 of drive #1.
   b. For one drive, the end of the "A" cable is connected to J1 of drive #1.
   c. There is a separate "B" cable from the DA to J2 of each drive.
9. Slide the drive back into the cabinet on its "bayonet" slide on the bottom of the drive.
10. Reinstall the 5/16 inch hex bolt and "pem" nut that were removed in step 1.

Figure 4-5. Quantum Drive Spindle Lock

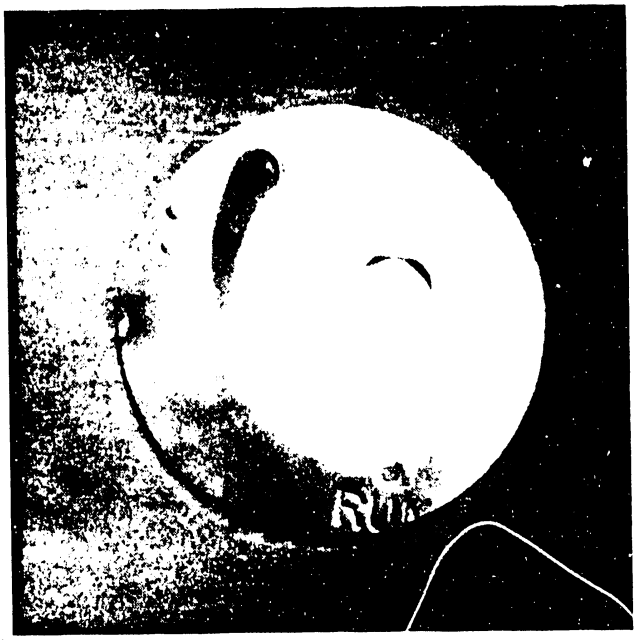


Figure 4-6. Quantum Drive Actuator Lock

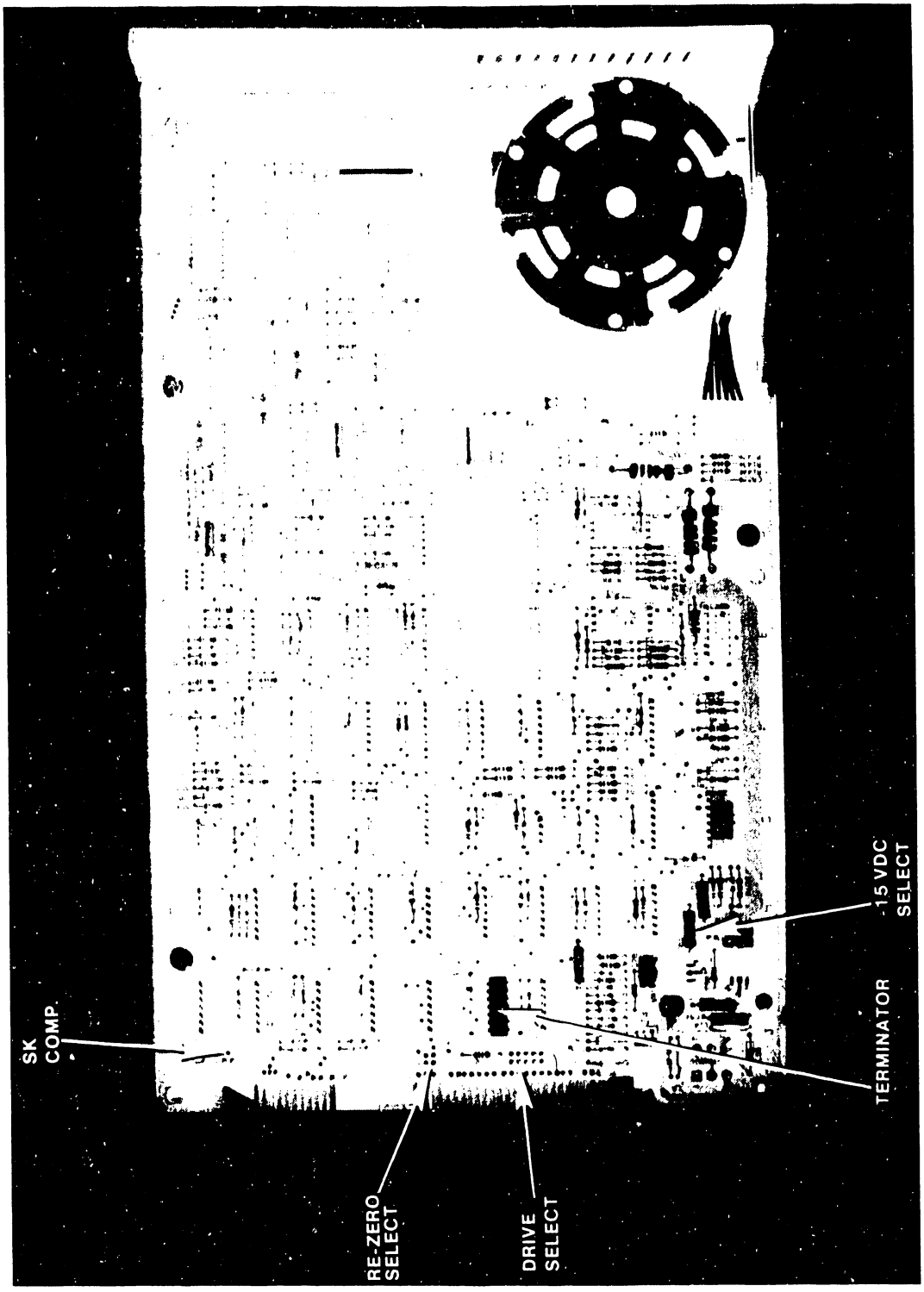


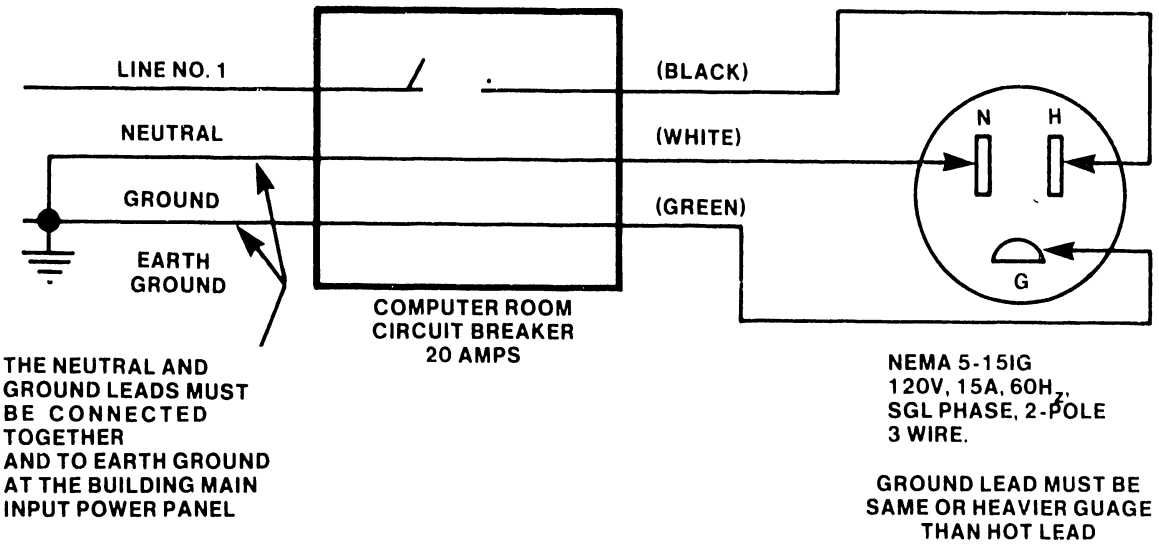
Figure 4-7. Quantum Drive Jumper Options

4.8. MAIN FRAME SOURCE-POWER CHECK

Before completing main frame reassembly and peripheral equipment installation, check the main frame power source receptacle for proper wiring and service, as defined in figure 4-8 and table 4-2. Perform the following electrical checks to make sure that the receptacle meets all specified requirements before proceeding with the installation.

CAUTION

Failure to perform the following check properly can result in serious damage to main frame circuits and to connected peripherals.



NEMA Configuration:	RECEPTACLE BODY	MATCHING CONNECTOR
	5-15IG	5-15IP

Figure 4-8. Power Service Requirements for VS-25/45 Main Frame

Table 4-2. DVM Chart For Voltage Measurements At The Receptacle

TEST POINT LOCATIONS	DMV READINGS
H TO N	115V AC (+/-10%)
H TO G	115V AC (+/-10%)
G TO N	+0V AC*

* If a difference in potential of more than 0.2 Vac exists between Neutral and Ground, notify building electrician that power supply is NOT ACCEPTABLE.

4.8.1 INITIAL MAIN FRAME POWER-UP

1. Make sure that the ac power On/Off switch on the Power Panel (figure 3-1) is in the 0 position and then plug the main frame power connector into the power source receptacle.
2. Perform the following in the sequence given: (Figures 3-1 and 3-2.)
   a. Set the Front Panel Bootstrap Media switch to the up position (select diskette drive). No diskette should be in the drive.
   b. Depress the ac power On/Off switch to the 1 position.
   c. Make sure the ac Power On lamp on the Power Panel is lit, the main frame cooling fans are turning, and the internal Quantum disk drive motor(s) are running.
   d. Wait 5 seconds after ac power is applied and then press the DC Initialize pushbutton.
   e. Make sure that the DC Power On LED on the power supply, the Power On LED on the Front Panel, and the HEX Display LEDs are lit after the DC Initialize pushbutton has been pressed. If the HEX Display LEDs go out after 2 seconds, there is a problem with the dc voltage compare circuit in the power supply.
   f. The HEX display on the Front Panel will begin counting down a series of numbers from FFFF to 0000 and then count up through a series of diagnostic routines (typically 10, 11, 12, 13, 14, 15, and 16) and stop at 9820, Diskette drive not ready. If any number (except 9820) is displayed for more than 15 seconds, the system has failed one of the diagnostics.
   g. At the same time the HEX display on the Front Panel is counting, the TC DA PROM-based power-up diagnostics will be running as shown on the TC DA Front Indicator/Control Panel. (Table 3-4.) The diagnostics will complete successfully in about 12 seconds.

NOTE

If the diagnostics failed and the voltages listed below are correct, refer to Chapter 8, Trouble Shooting, and Appendix B, Self-Test Monitor Diagnostic Error Codes.

   h. The following voltages must be checked on the VS-25/45 at the motherboard test points (figures 4-9 and 4-10). (Adjustments to the switching power supply should not be performed in the field.)
   i. If the dc voltages are out of operating limits, the switching power supply must be replaced (paragraph 5.6).

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+12.0	+11.1V to +12.8V	35mV RMS or 50mV Pk-to-Pk
-12.0	-11.5V to -12.5V	35mV RMS or 50mV Pk-to-Pk
+5.0	+4.5V to +5.7V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.5V to -5.5V	35mV RMS or 50mV Pk-to-Pk
IV (+12.0)*	+11.5V to +12.8V	35mV RMS or 50mV Pk-to-Pk

* - IV (Independent Voltage) was spare +12 Vdc, now used with regular +12 Vdc for current loading purposes.

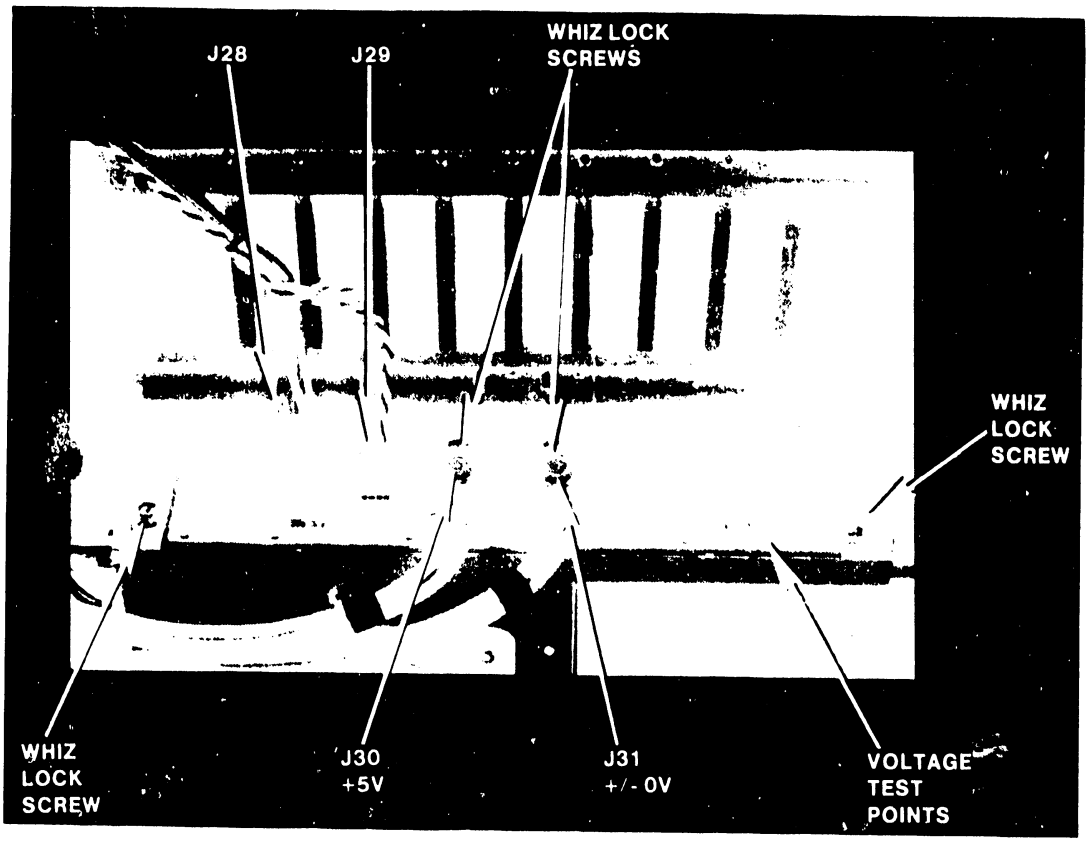


Figure 4-9. Motherboard Power Connectors

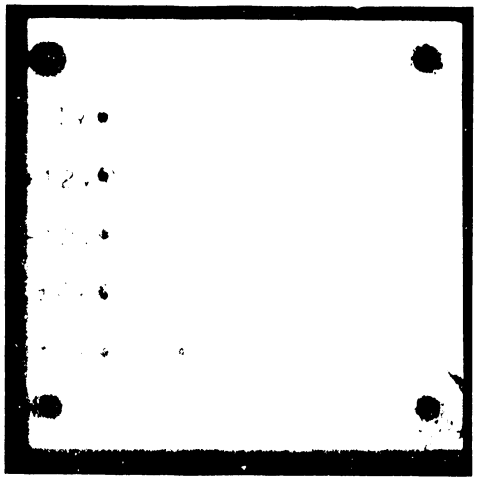


Figure 4-10. Motherboard Voltage Test Points

4.9 VERIFY SYSTEM DISK

If the voltage checks are normal, the system disk must be verified to make sure the pre-recorded system software has not been damaged. If the system disk does not pass verification, it must be reformatted and a coldstart (paragraph 4.9.1) must be performed. To verify the system disk drive:

1. Connect Workstation 0 to Port 0 on the Serial I/O Device Adapter, as described in paragraph 4.12.2, and power up workstation 0.
2. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
3. Make sure the Bootstrap Media switch (see figure 3-2) on the Front Panel is in the up position (selects the diskette drive).
4. Insert the diskette labeled FTU45 into the diskette drive and close the door.
5. Press the red Initialize button (figure 3-2) on the Front Panel.
6. The HEX display on the Front Panel will begin counting as was described in paragraph 4.8.1, step 2f. This time the display should turn blank after completing the diagnostics.
7. The IPL Drive Selection screen should appear on Workstation 0.

```
                VS Self Test Monitor Package
                      IPL Drive Selection
                   Bootstrap Volume = FTU45

  Device     Capacity     Type     Volume      Status
  2270V-4    1.2 Mb       Dsket    FTU45
  Q2040       33 Mb       Fixed    SYSTEM      Media Tolerant

          Position Cursor to Indicate Device and Select:
================================================================
(ENTER) IPL                    (8) STAND-ALONE DIAGNOSTIC MONITOR
```

NOTES

1. If the IPL Drive Selection screen does not appear, try another diskette. If the screen still doesn't appear, insert the Stand-Alone Diagnostic diskette and run the Stand-Alone Diagnostics. Also, refer to the trouble shooting flow charts in Chapter 8.
2. If the IPL Drive Selection screen appears but fails to recognize the system disk label, continue the verify procedure. If FTU will not read the system disk, Coldstart the disk. (Paragraph 4.10.1.)

8 Position the cursor next to the disk labeled FTU45 and press ENTER.
9. The Self-Test Monitor diagnostic will begin running as shown below.

NOTE

To successfully run the (BP) USART Loopback Verification Test of the Self-Test Monitor, either an RS-232 Loopback connector (WLI P/N 420-1040) or a modem must be connected to the RS-232 Remote Diagnostic connector on the CPU rear panel. The modem must have ac power applied to it and signal DSR (Data Set Ready) must be ON. If the Loopback connector or the modem is NOT installed, the test will respond with Nonfatal Error, code 3C03. Press ENTER to continue.

VS Self Test Monitor Package
System Hardware Status
System Volume = FTU45

Status	Diagnostic		
Passed	(SIO)	Serial Data Link Test	
Non-Fatal Error	(BP)	USART Loopback Verification Test	Code = 3C03
Passed	(CPU)	CP Control Memory & CP/BP Test	
Passed	(CPU)	CP Random Operands Test	
Passed	(CPU)	CP Integrity Test	
Passed	(MM)	Main Memory Integrity Test	
Passed	(BP)	BP DMA & MARS Test	

Diagnostics Completed, Beginning System Initialization

10. In about 90 seconds, after all tests have passed and system microcode has loaded, Workstation 0 will display the the message:
"WANG VS UNIVERSAL STAND-ALONE DIAGNOSTIC MENU"
11. Press PF5 - FTUA.
12. W/S 0 will display the message:
"INFORMATION REQUIRED BY PROGRAM FTU TO DEFINE DRIVE"
13. Enter the following:
DEVICE - 110 (refer to table 8-7 for device numbers to run FTU45 as a stand-alone diagnostic on other drives)
VOLUME - SYSTEM (or the appropriate volume name)
ALIGN PK - NO
14. Press PF17 - FIXED DISK.
15. W/S 0 will display the message:
"RESPONSE REQUIRED BY PROGRAM FTU TO ACKNOWLEDGE STATUS"
16. Press PF15 - CONTINUE
17. W/S 0 will display the message:
"INFORMATION REQUIRED BY PROGRAM FTU TO SELECT FUNCTION"
18. Press PF1 - VERIFY DISK
19. W/S 0 will display the message:
"INFORMATION REQUIRED BY PROGRAM FTU TO DEFINE OPTIONS"
20. DO NOT modify option fields.
Press ENTER.
21. W/S 0 will display the message:
"FUNCTION RUNNING. PRESS ANY PFK TO ABORT."

22. W/S 0 will list any errors as they happen. Verify is considered to have failed if:
    a. Any hard errors are detected.
    b. More than 12 soft errors are detected.
    c. Any soft errors are detected between sectors 0000 to 00F8.
23. When Verify is completed, in about 8 minutes, W/S 0 will display: "FUNCTION COMPLETE. ENTER FOR MENU"
    Unless Verify is going to be run again, press PF16 - END OF JOB. The screen displayed will again be:
    "WANG VS UNIVERSAL STAND-ALONE DIAGNOSTIC MENU".
24. If Verify failed, go to paragraph 4.10 and perform the Coldstart procedure. If Verify DID NOT fail, go to paragraph 4.11, Bootstrap programs and the IPL Process.

4.10 COLDSTART PROGRAM

The basic VS-25/45 CPU currently supports only one removable diskette media (the 1.2 Megabyte diskette). In order to bring up the VS Operating System on this basic hardware, if the system disk does not pass the verification portion of the FTU45 stand-alone diagnostic, the fixed disk must be initialized and then loaded with the necessary operating system files. The Coldstart program provides this function.

NOTE

The 5.03.70 Operating System Coldstart program does not run on and will not support the 22V65-3 620 Megabyte drive. This drive is supported by Operating System 6.10. Refer to paragraph 4.10.2.

Coldstart is a stand-alone program which is IPLed from a media tolerant diskette. The program uses the diskette drive, the fixed drive, and Workstation 0. The program copies the OS files from a series of disks. The Coldstart program builds a media-tolerant VTOC on the fixed disk as it copies the OS files. Coldstart can also copy the CP and BP code and bootstrap files to the fixed disk, allowing both bootstrapping and IPLing from the fixed disk.

Additional Coldstart functionality is being considered in order to assist in backing up fixed-disk files (to diskette) in case of damage to the fixed disk during system operation. However, a diskette-based version of the OS is not planned for VS-25/45 system support.

4.10.1 OPERATING SYSTEM 5.03.70 COLDSTART PROCEDURE

The Self-Test Monitor diagnostics are run as part of the Coldstart and or daily IPL procedure. At any time CPU integrity becomes suspect, the microcode diagnostics must be loaded and run. (Refer to Chapter 8, Troubleshooting, for complete diagnostic procedures.)

1. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
2. Set the Bootstrap Media switch (see figure 3-2) on the front panel to the up position (selects the diskette drive).

3. Insert the diskette labeled Format into the diskette drive and close the door.
4. Press the red Initialize button (figure 3-2) on the front panel. In about 30 seconds W/S 0 will display the following Menu:

```
                VS Self Test Diagnostic Monitor
                      IPL Drive Selection
                   Bootstrap Volume = FORMAT

Device      Capacity     Type      Volume      Status
2270V-4     1.2 Mb       Dsket     FORMAT      Media Tolerant
Q2040        33 Mb       Fixed

            Position Cursor to Indicate Device and Select:
================================================================
(ENTER) IPL                        (8) STAND ALONE DIAGNOSTIC MONITOR
```

5. Position the cursor next to the disk labeled FORMAT and press ENTER.
6. The Self-Test Monitor diagnostics will begin running. (See table 8-2 for diagnostic error code information.)

NOTE

To successfully run the (BP) USART Loopback Verification Test of the Self-Test Monitor, either an RS-232 Loopback connector (WLI P/N 420-1040) or a modem must be connected to the RS-232 Remote Diagnostic connector on the CPU rear panel. The modem must have ac power applied to it and signal DSR (Data Set Ready) must be ON. If the Loopback connector or the modem is NOT installed, the test will respond with Non-fatal Error, code 3C03. Press ENTER to continue.

```
                VS Self Test Monitor Package
                    System Hardware Status
                    System Volume = FORMAT

Status            Diagnostic
Passed            (SIO) Serial Data Link Test
Non-Fatal Error   (BP)  USART Loopback Verification Test  Code = 3C03
Passed            (CPU) CP Control Memory & CP/BP Test
Passed            (CPU) CP Random Operands Test
Passed            (CPU) CP Integrity Test
Passed            (MM)  Main Memory Integrity Test
Passed            (BP)  BP DMA & MARS Test

        Diagnostics Completed, Beginning System Initialization
```

7. If the Main Memory Integrity test fails, refer to paragraph 8.4.2.5 for instructions on running the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.
8. After the Self-Test Monitor diagnostics have completed, W/S 0 will display the Volume Initialization Information Request screen.

```
                    *** VS-25 Coldstart ***

                        Fixed Disk = Q2040

   The following information is required for volume initialization:

Volume name                    - SYSTEM
Volume owner                   -
Date (MM/DD/YY)                -   /  /
VTOC size (in blocks)          - 100

        Please supply the required parameters and press ENTER
                                or
         Press PF1 to continue without initializing the disk.
```

9. Enter the requested information and press either:
   a. ENTER for a complete format of an unformatted drive (go to step 10.), or
   b. PF1 to write a new volume label on a previously formatted drive. (Go to step 11.)
10. W/S 0 will respond with the following message: "Disk Formatting In Progress". (The Quantum drive will take approximately 40 minutes to for t.)
11. When the Formatting (or relabeling) is complete W/S 0 will respond with the following message: "Formatting complete. Please insert first disk to be copied."
12. Remove the Format disk and insert the diskette labeled SYSTM 1 into the diskette drive and close the door. W/S 0 will respond with the following message: "Copy in progress".
13. When the copy is finished, W/S 0 will respond with the following message: "All files on this disk have been copied. Please mount the next volume to be copied and press ENTER, or press PF16 to terminate".
14. Remove SYSTM 1 and insert the diskette labeled SYSTM 2 in the diskette drive, and press ENTER. W/S 0 will again respond with the following message: "Copy in progress".
15. When the copy is finished, W/S 0 will again respond with the following message: "All files on this disk have been copied. Please mount the next volume to be copied and press ENTER, or press PF16 to terminate".
16. Repeat step 15, using successively numbered diskettes, until the contents of all disks labeled "SYSTM" have been copied.
17. After removing the final Coldstart disk from the diskette drive, press PF16 to terminate. W/S 0 will respond with the following message: "Copy complete. IPL when ready!"
18. Set the Bootstrap Media switch on the front panel to the middle position (selects the internal fixed drive).

19. IPL the system (paragraph 4.11.1) and log on as user CSG.
20. Run the GENEDIT program (refer to the VS25 Bulletin, WLI P/N 800-6183), declare all peripherals, and reIPL.
21. Run the BACKUP program, using the RESTORE function, and copy the following volumes to the system disk: NVRAM, MACLIB, WSCODE, PRCODE, UTLTY1, UTLTY2, WP1, and WP2
22. When the message "The WORK file cannot be placed on the output volume. Please respecify." appears, press PF1 to continue.
23. When all volumes have been copied, the Coldstart procedure is complete.

4.10.2 OPERATING SYSTEM 6.10 COLDSTART PROCEDURE

The 6.10 Coldstart is a self-contained, stand-alone program. It doesn't use the normal operating system, nor can the normal operating system use it. The Coldstart utility has two modes of operation, the Copy mode and the Backup mode. The Copy mode allows three different ways to copy data from the input diskette to the system volume.

1. Initialize the system volume before copying the data.
2. Reformat the system volume before copying the data.
3. Copy only those files that you want to add to or update the system volume with.

The method selected depends on circumstances. If a new system is being installed, it is likely that the disk to be used for the system volume is not initialized. Because the disk must be initialized before it can be used, select the first option.

The second option, reformatting, can be used to bring up a system when the system volume has been initialized previously. Reformatting clears the volume of existing data and rewrites the VTOC. This option is required if the system volume is not media tolerant.

The third option, Copy only, allows loading new system files without rebuilding the entire system. Coldstart checks for duplicate file names, flags each, and allows you to skip the input file or to rename either the old or the new file.

The Backup method of Coldstart (paragraph 4.10.2.1) is useful on single disk systems in the situation where, for some reason, you can read but not IPL from the system disk. By running the Backup mode before reformatting, undamaged data resident on the volume can be preserved.

NOTE

The Coldstart Backup module does not work on a disk with either hard I/O errors or a bad VTOC.

1. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
2. Set the Bootstrap Media switch (see figure 3-2) on the front panel to the up position (selects the diskette drive).

3. Insert the diskette labeled Format into the diskette drive and close the door.
4. Press the red Initialize button (figure 3-2) on the front panel. In about 30 seconds W/S 0 will display the following Menu:

```
                VS Self Test Diagnostic Monitor
                      IPL Drive Selection
                   Bootstrap Volume = FORMAT

  Device     Capacity     Type     Volume      Status
  2270V-4    1.2 Mb       Dsket    FORMAT      Media Tolerant
  2265V1      75 Mb       Rem

            Position Cursor to Indicate Device and Select:
================================================================
(ENTER) IPL                      (8) STAND ALONE DIAGNOSTIC MONITOR
```

5. Position the cursor next to the disk labeled FORMAT and press ENTER.
6. The Self-Test Monitor diagnostics will begin running. (See table 8-2 for diagnostic error code information.)

NOTE

To successfully run the (BP) USART Loopback Verification Test of the Self-Test Monitor, either an RS-232 Loopback connector (WLI P/N 420-1040) or a modem must be connected to the RS-232 Remote Diagnostic connector on the CPU rear panel. The modem must have ac power applied to it and signal DSR (Data Set Ready) must be ON. If the Loopback connector or the modem is NOT installed, the test will respond with Non-fatal Error, code 3C03. Press ENTER to continue.

```
                VS Self Test Monitor Package
                      System Hardware Status
                      System Volume = FORMAT

  Status            Diagnostic
  Passed            (SIO) Serial Data Link Test
  Non-Fatal Error   (BP)  USART Loopback Verification Test  Code = 3C03
  Passed            (CPU) CP Control Memory & CP/BP Test
  Passed            (CPU) CP Random Operands Test
  Passed            (CPU) CP Integrity Test
  Passed            (MM)  Main Memory Integrity Test
  Passed            (BP)  BP DMA & MARS Test

          Diagnostics Completed, Beginning System Initialization
```

7. If the Main Memory Integrity test fails, refer to paragraph 8.4.2.5 for instructions on running the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.
8. After the Self-Test Monitor diagnostics have completed, W/S 0 will display the System Disk Specification screen.

*** Wang VS Coldstart ***

The primary purpose of the COLDSTART stand-alone utility is to bring up a new machine by formatting the system disk and copying a minimum system to it. COLDSTART may also be used to add programs to an existing system (Copy only) or to backup an existing system.

Please specify the system disk and press ENTER.

Device Type -
Physical Device Address (hex) -

Device Type	Description	Device Type	Description
2265V-1	75 Meg Rem Disk	2265V-2	275 Meg Rem Disk
2280V1F	30 Meg F/R Disk (F)	2280V1R	30 Meg F/R Disk (R)
2280V2F	60 Meg F/R Disk (F)	2280V2R	60 Meg F/R Disk (R)
2280V3F	90 Meg F/R Disk (F)	2280V3R	90 Meg F/R Disk (R)
2265V1A	75MB R dual port Dk	2265V2A	288M R dual port Dk
2265V3	620M R dual port Dk	Q2040	8 inch Fixed Disk

9. Enter the device type (above) and device address for the output volume, the volume to which you are copying the system software or from which you are backing up. The address of the drives are:
   a. Quantum drive #1 = 2400
   b. Quantum drive #2 = 2401
   c. SMD DA port #0 = 3400
   d. SMD DA port #1 = 3401
   e. SMD DA port #2 = 3402
   f. SMD DA port #3 = 3403

   Press ENTER

NOTE

Coldstart works on any drive. However, a system bootstrap must be from a diskette, the fixed disk of a VS-25 or VS-45, or the removable part of a fixed/removable disk.

10. The Coldstart main menu will appear, allowing selection of a Copy or Backup operation.

```
                    *** Wang VS Coldstart ***


          Press PF4 to COPY to system disk, or
                PF5 to BACKUP the system disk.
          Press PF1 to return to the previous screen.
```

11. Select Copy (PF4). The Select Copy Mode screen will appear.

```
                    *** Wang VS Coldstart ***


          Press PF2 to INITIALIZE the system disk,
                PF3 to REFORMAT the system disk, or
                PF4 to COPY only.
          Press PF1 to return to the previous screen.
```

12. Press either:
    a. PF2 to initialize a disk that failed FTU45 (go to step 13), or
    b. PF4 to copy files to an initialized disk (go to step 15).
13. The System Disk screen should appear. Enter the requested information and press ENTER to continue.

```
                    *** Wang VS Coldstart ***

                          System Disk

    The following information is required for volume reformatting:

Volume name                   - SYSTEM
Volume owner                  -
Date (MM/DD/YY)               -   /  /
VTOC size (in blocks)         -


        Please supply the required parameters and press ENTER.
         or Press PF1 to return to the mode selection screen.
```

14. Coldstart then initializes or reformats the system disk. W/S 0 will respond with the following message: "Disk Formatting In Progress".
15. After initialization (or reformatting) is complete, or the copy only option was selected, Coldstart requests mounting the first diskette to be copied.
16. Remove the Format disk and insert the diskette labeled SYSTM 1 into the diskette drive and close the door.
17. When the copy is finished, W/S 0 will respond with the following message: "All files on this disk have been copied. Please mount SYSTM2." (Coldstart gets the name of the next diskette to be mounted from the current diskette.)
18. Repeat step 17 until the contents of all diskettes labeled "SYSTM" have been copied.
19. When the last diskette has been copied, W/S 0 will respond with the following message: "IPL when ready"
20. Set the Bootstrap Media switch on the front panel to the middle position (selects the internal fixed drive) or to the down position (selects external drives).
21. IPL the system (paragraph 4.11.1) and log on as user CSG.
22. Run the GENEDIT program (refer to the VS25 Bulletin, WLI P/N 800-6183), declare all peripherals, and reIPL.
23. Run the BACKUP program, using the RESTORE function, and copy the following volumes to the system disk: NVRAM, MACLIB, WSCODE, PRCODE, UTLTY1, UTLTY2, WP1, and WP2
24. When the message "The WORK file cannot be placed on the output volume. Please respecify." appears, press PF1 to continue.
25. When all volumes have been copied, the Coldstart procedure is complete.

4.10.2.1 Operating System 6.10 Backup Procedure

The Backup mode helps to preserve data on a system volume that may have been damaged. The data may be read from the volume but it can't be IPLed from. Backup doesn't correct the damage but it does help recover the readable data.

NOTE

Backup reformats but doesn't initialize output diskettes. Any diskettes to be used for outputs must be initialized before Coldstart is loaded. Don't use duplicate volume names for the output diskettes.

1. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
2. Set the Bootstrap Media switch (see figure 3-2) on the front panel to the up position (selects the diskette drive).
3. Insert the diskette labeled Format into the diskette drive and close the door.
4. Press the red Initialize button on the front panel. In about 30 seconds W/S 0 will display the IPL Drive Selection menu.
5. Position the cursor next to the disk labeled FORMAT and press ENTER.

6. The Self-Test Monitor diagnostics will begin running. (See table 8-2 for diagnostic error code information.)
7. If the Main Memory Integrity test fails, refer to paragraph 8.4.2.5 for instructions on running the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.
8. After the Self-Test Monitor diagnostics have completed, W/S 0 will display the System Disk Specification screen.
9. Enter the device type and device address for the output volume, the volume to which you are copying the system software or from which you are backing up. The address of the drives are:
   a. Quantum drive #1 = 2400
   b. Quantum drive #2 = 2401
   c. SMD DA port #0 = 3400
   d. SMD DA port #1 = 3401
   e. SMD DA port #2 = 3402
   f. SMD DA port #3 = 3403

   Press ENTER
10. The Coldstart Main Menu will appear, allowing selection of a Copy or Backup operation.
11. Select Backup (PF5). The Diskette Volume Label screen will appear.

```
                    *** Wang VS Coldstart ***

                          Backup Diskette

     The following information is required for volume formatting:

Volume name                    -
Volume owner                   -
Date (MM/DD/YY)                -   /  /
VTOC size (in blocks)          - 008

        Please supply the required parameters and press ENTER
```

12. Enter the requested information and press ENTER.
13. Dismount the Format diskette and mount the first Backup diskette.
14. The Diskette Volume Label screen will appear throughout the Backup process before each request to mount the next diskette.

4.11 BOOTSTRAP PROGRAMS AND IPL PROCESS

Because the VS-25/45 system does not contain any PROM-based operational microcode, all CP and BP operational microcode must be loaded into the system by the bootstrap programs. (Note that the bootstrap programs cannot coexist with the operational CP and BP code; therefore, no system-level CP/BP functions, such as Control Mode, are available while the bootstrap programs are executing).

Pressing the Initialize Button starts the bootstrap process from the disk device indicated by the 3-position Bootstrap Media switch. The bootstrap programs perform power-up initialization and diagnostic functions and then uses the Workstation 0 screen to allow the operator to select either "IPL the system" or "Run Off-line Diagnostics" from the selected IPL device.

The VS-25/45 system functions just like other VS machines once execution of the IPL text has begun. However, since the bootstrap programs do not maintain the Time of Day clock during their power-up and initialization process, the VS-25/45 will require resetting the clock after every IPL from a power off condition.

4.11.1 IPL PROCEDURE

1. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
2. Set the Bootstrap Media switch to the center position (select the fixed drive).
3. Press the Initialize button on the front panel. (The HEX display on the front panel will begin counting down from FFFF.) In about 45 seconds W/S 0 will display the following Menu:

```
                    VS Self Test Monitor Package
                        IPL Drive Selection
                    Bootstrap Volume = SYSTEM

  Device      Capacity     Type      Volume      Status
  2270V-4     1.2 Mb       Dsket
  Q2040        33 Mb       Fixed     SYSTEM      Media Tolerant


            Position Cursor to Indicate Device and Select:
==========================================================================
(ENTER) IPL                          (8) STAND-ALONE DIAGNOSTIC MONITOR
```

4. Position the cursor next to the system volume and press ENTER.
5. The Self-Test Monitor diagnostics will begin running. (See table 8-2 for diagnostic error code information.)

```
                    VS Self Test Monitor Package
                        System Hardware Status
                        System Volume = SYSTEM

Status          Diagnostic
Passed          (SIO) Serial Data Link Test
Passed          (BP)  USART Loopback Verification Test
Passed          (CPU) CP Control Memory & CP/BP Test
Passed          (CPU) CP Random Operands Test
Passed          (CPU) CP Integrity Test
Passed          (MM)  Main Memory Integrity Test
Passed          (BP)  BP DMA & MARS Test

        Diagnostics Completed, Beginning System Initialization
```

6. If the Main Memory Integrity test fails, refer to paragraph 8.4.2.5 for instructions on running the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.
7. After the Self-Test Monitor diagnostics have completed, the system will IPL. In about 75 seconds W/S 0 will display the request for information to specify the name of the configuration file.

```
***Message M0001 BY SYSGEN

                        INFORMATION REQUIRED


 Specify the name of the system configuration file and press (ENTER)
                              - or -
          Press (1) to use one workstation and one disk.

                        SYSFILE = @CONFIG@
                        SYSLIB  = @SYSTEM@

   Specify the communications configuration file to be used, if any

                        COMMFILE =
                        COMMLIB  = @SYSTEM@
```

8. Enter the correct information and press ENTER. The System Generation process will begin.
9. W/S 0 will respond with a request for information required to set date and time.
10. Enter the data and time and press ENTER.
11. System Initialization will begin and in about 45 seconds W/S 0 will display the standard VS Operators Console screen, completing the process.

4.12 SYSTEM INTERCONNECTION

After microcode is loaded and SYSGEN has been performed, power down the main frame and connect all peripheral devices according to the configuration created during SYSGEN. See figure 4-11, the following paragraphs, and the appropriate documents in Class 3000 for cabling procedures.

4.12.1 CONNECTOR PLATE-TO-I/O DEVICE ADAPTER CABLING

Before installing cables in the connector plates at the rear of the main frame, all cables between the plates and associated device adapters must be installed. Make sure that the cable from the connector plate containing workstation 0 connects to J2 of the Serial I/O Device Adapter assembly in Motherboard slot #4.

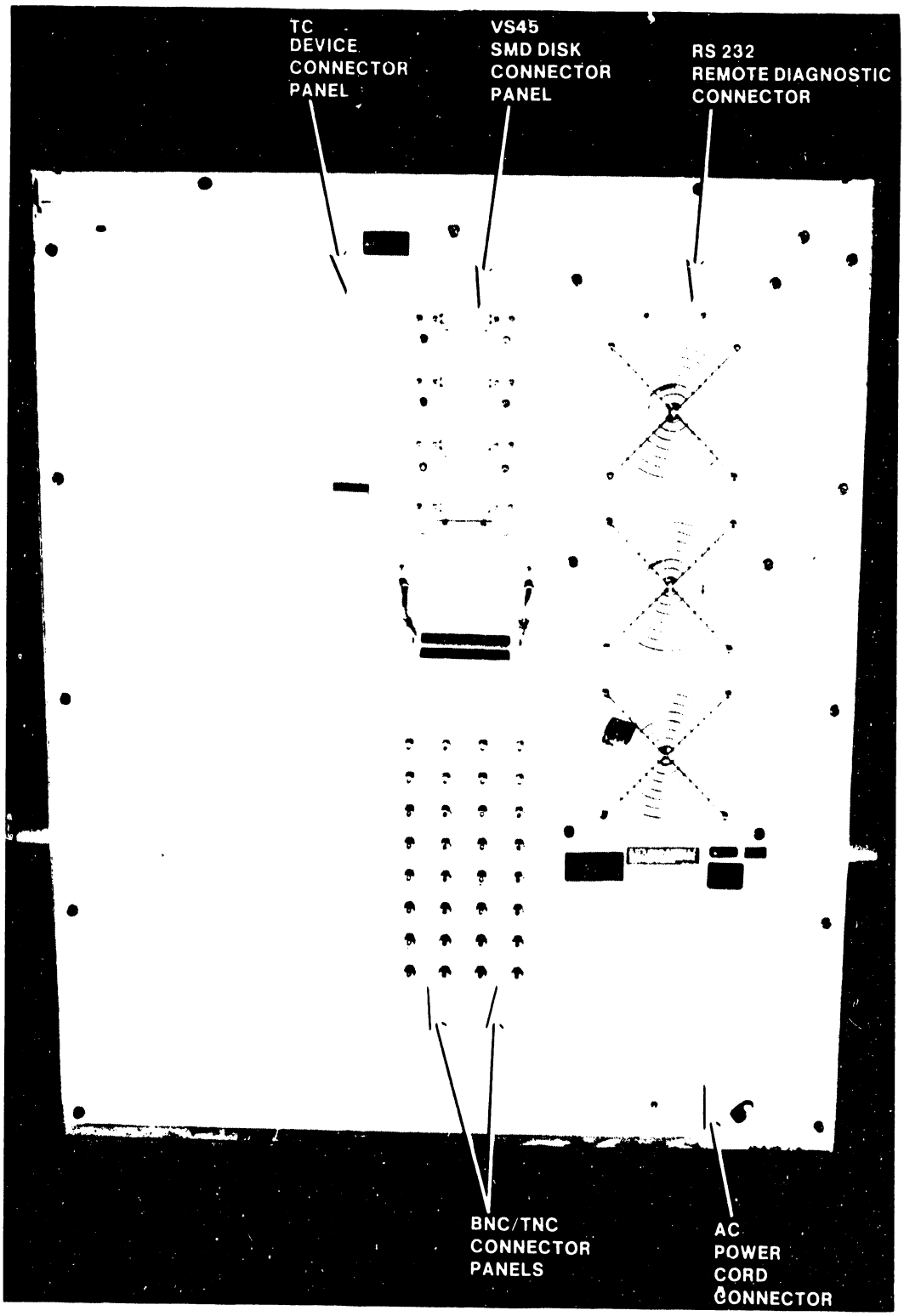


Figure 4-11. VS-25/45 Rear Panel Connector Plate Locations

4.12.2 BNC/TNC CONNECTORS

Serial I/O devices (workstations, printers, etc.) connect to the main frame by means of standard BNC/TNC connectors mounted on a 16-connector plate (WLI P/N 270-0704). Maximum cable length for these devices is 2000 feet (610 meters). Workstation 0 MUST be connected to Port 0 on the Serial I/O Device Adapter. The connectors for Workstation 0 are located in the upper right corner of the connector plate on the rear of the main frame. See figure 4-12. for details on connector plate and BNC/TNC count for peripherals.

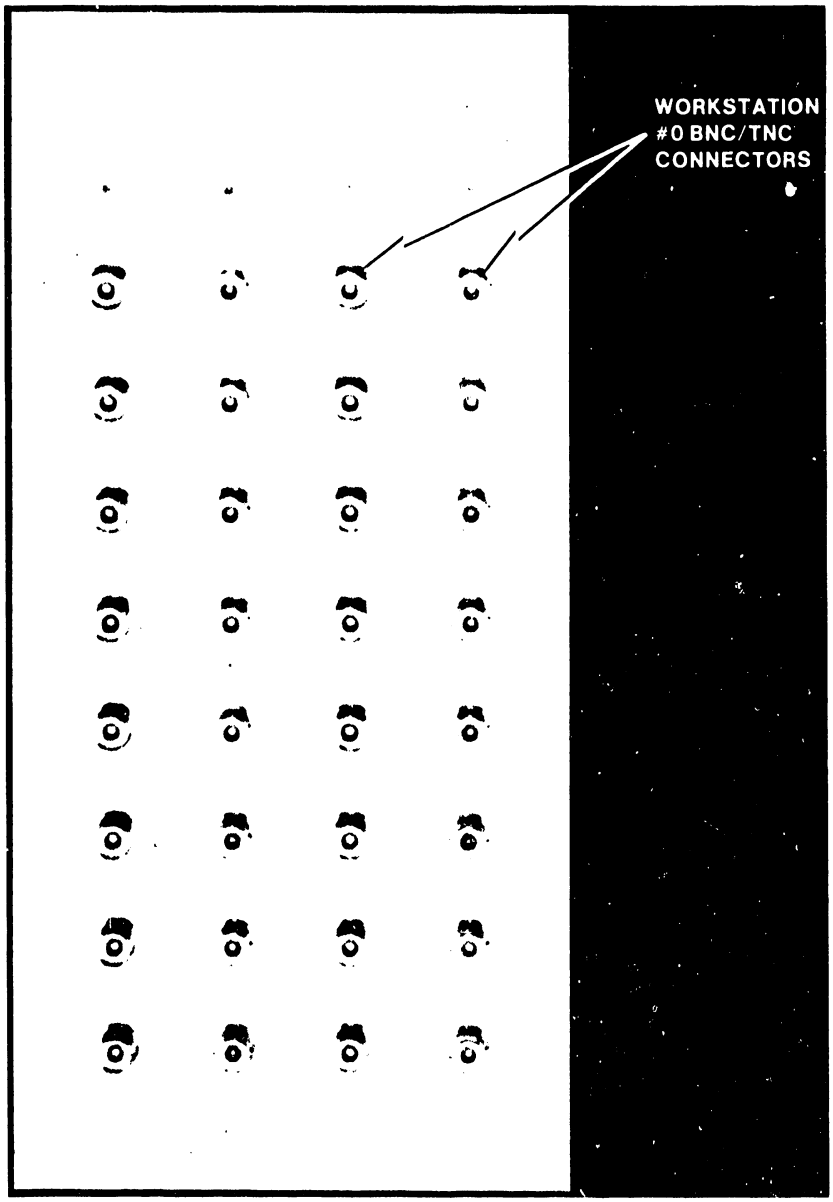


Figure 4-12. WLI P/N 270-0704 BNC/TNC Connector Plate

4.12.3 SMD DISK CABLE CONNECTORS

The external disk cables (disk drive to main frame) must be connected to a disk cable connector panel (WLI P/N 270-0702, figure 4-13.) at the rear of the main frame. Two sizes of disk cable connectors and clamps are located on the disk cable connector panel. The top four (narrow) connectors contain 26-pin sockets for the 4 "B" cable connections; the bottom (wide) connector contains a 60-pin socket for the "A" cable connection. This connector panel is cabled internally to the 25V50 SMD DA.

Before connecting an external disk cable prepare it as follows, if necessary:

1. Remove 6 inches of plastic sheathing from one end of the cable.
2. Fold the copper shield back exposing the disk cable.

Connect the disk cables as follows:

1. Disassemble the cable clamp by removing the Phillips screws on either side of the clamp.
2. Lay the copper shielded section of the external disk cable against the piece of the clamp still connected to the main frame.
3. Reassemble the cable clamp by installing the two Phillips screws removed in step 1. Make sure that pin 1 of the cable is oriented properly and tighten the clamp screws until solid contact with the copper shield is made. DO NOT overtighten as this could damage the disk cable.
4. Plug the cable into the cable connector on the disk connector panel. The top connector connects to Port 3 of the SMD DA, the second connector connects to Port 2, and so forth. The top four connectors of each disk connector panel connect the "B" cable of each drive; the bottom connector on the panel connects the "A" cable daisy-chained through each drive to the VS-45 main frame.
5. Connect the internal cables, supplied with the connector panel, on the correct connectors on the SMD DA card. (Figure 5-13.)

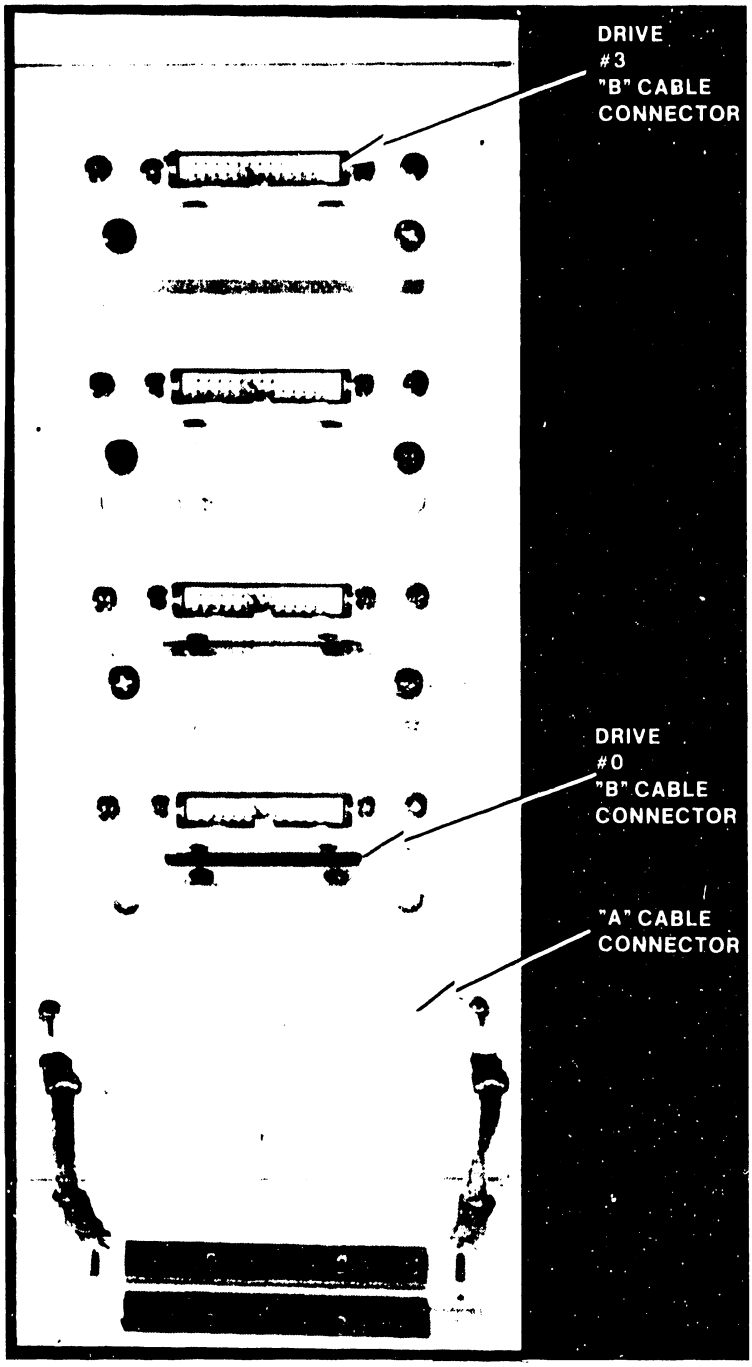


Figure 4-13. 270-0702 Rear Cable Connector Panel For SMD Disk Device Adapter.

4.12.4 TELECOMMUNICATION CONNECTORS

The external telecommunications cables (modem to main frame) must be connected to a cable connector panel (WLI P/N 270-0824 for the 1-port TC adapter and WLI P/N 270-0825 for the 2-port TC adapter)) at the rear of the main frame. This panel supports three different TC connections, providing plugs for both the modem and Automatic Calling Unit (ACU) cables. This connector panel is cabled internally to the 25V76-1/2 TC DA (figures 5-16 or 5-17).

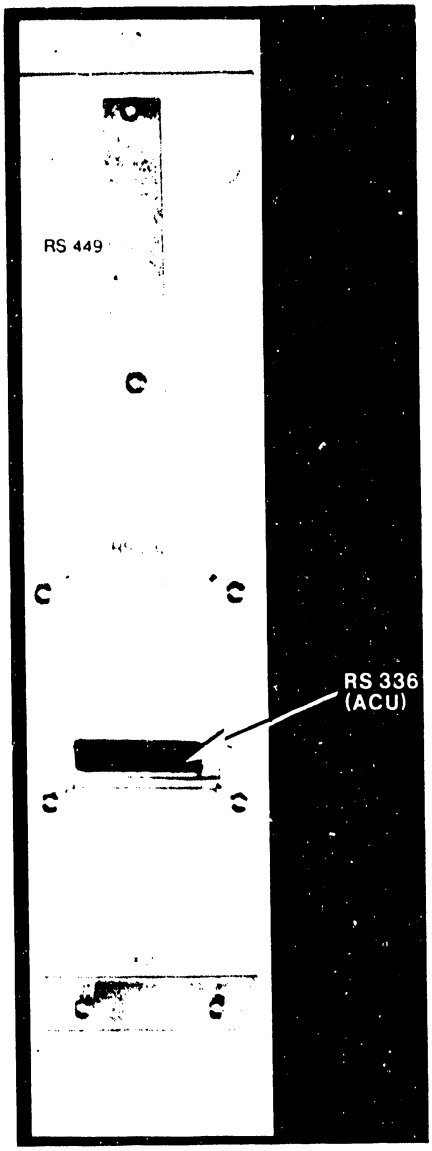


Figure 4-14. 270-0824 Rear Cable Connector Panel For Telecommunications Adapter.

4.13 PRELIMINARY SYSTEM CHECKOUT

At this point, all peripherals should be installed, powered off, and connected to their respective device adapters. Before proceeding, perform the following checkout procedure:

1. Visually inspect all main frame circuit boards for correct switch settings and proper cabling configuration.
2. Visually inspect all peripheral devices to make sure that I/O cabling is correctly installed, all switch settings are correct, and all covers and panels are in place.
3. Make sure that all devices are powered off.

4.13.1 DAILY POWER-UP/POWER-DOWN PROCEDURES

After all peripherals are connected to the main frame, the daily power-up and power-down procedures for the VS-25/45 system are as follows:

1. POWER-UP
   a. Make sure that the main frame power connector is plugged into the power source receptacle.
   b. Power up Workstation 0 and the primary disk drive.
   c. Depress the main frame ac power On/Off switch to the 1 position.
   d. Wait 5 seconds and then press the DC Initialize pushbutton located on the main frame Power Panel.
   e. After the PROM-based power-up diagnostics have completed (the NOT READY light front panel has gone out), position the cursor on W/S 0 next to the IPL volume name and press ENTER. The Self-Test Monitor diagnostics will begin running. (See table 8-2 for diagnostic error code information.)
   f. After the IPL Self-Test Monitor diagnostics have completed, enter the name of the configuration file and press ENTER.
   g. Enter the date and time and press ENTER.
   h. When System Initialization has completed, the VS Operators Console screen will appear and the system is ready for normal operation.

2. POWER-DOWN
   a. Make sure all operators have logged off of the system.
      1) Press PF13 (WORKSTATIONs) on an operators console to check that the operators have logged off of the system.
      2) Press PF7 (NONINTERACTIVE Tasks) on an operators console to check the background tasks on the system. Look under the User column to identify any operator running a background task.
   b. Press the green Control Mode button. This prevents any disk I/O command in process from being halted prior to completion.
   c. Power down all peripheral devices according to procedures in the applicable documents in Class 3000.
   d. Depress the main frame ac power On/Off switch to the 0 position.

4.14 SYSTEM TURNOVER

NOTE

When the customer chooses the Remote Diagnostic feature, the Remote Diagnostic Certification Procedures (paragraph 8.3.1) must be performed.

1. Remove any scratch or Customer Engineering disks from the diskette drive.
2. Perform an IPL from the system disk.
3. Log on to a Workstation and use the Command Processor display functions to display the files in the @SYSTEM@ library on the customer's operating system disk. Check through the listed files to make sure all customer-purchased options are present.
   If the BASIC compiler was purchased by the customer, for example, the following files should be present in the @SYSTEM@ library:
   a. BASIC
   b. CVBASIC
   If the COBOL compiler was purchased, conversely, the following files should be present:
   a. COBOL
   b. WC1PASS1
   c. WC1PASS2
   If the RPG compiler was purchased, only the following file should be present:
   a. RPGII
4. Delete any of the above compilers not purchased by the customer from the related files using the Command Processor SCRATCH function.
5. Demonstrate to the customer or to the responsible computer operator how the disk initialization procedure is performed. Initialize and verify Quantum drive #2 using the DISKINIT system utility program.
6. Mount customer scratch packs on all additional disk drives. (The customer determines which packs will be scratch packs.) Perform a disk initialization procedure on each of the customer's scratch packs.

CAUTION

Make sure that the customer's scratch packs have no files on them before performing the initialization procedure. Demonstrate loading and unloading of disk packs, emergency power-down of the disk drive, and disk drive fault recovery.

6. Perform the following Evening Shut-down Procedure and explain each step to applicable customer personnel:
   a. Make sure all workstations have been logged-off.
   b. Press the green Control Mode button on the VS-25/45 front panel.
   c. Place all drives in the Load Mode condition (heads unloaded).
   d. Power down all workstations and printers.
   e. Unload and power down all tape drives.

7. Perform the following Daily Start-up Procedure and explain each step to applicable customer personnel:
   a. Bring all disk drives up to the ready condition.
   b. On Workstation #0, press the X key and then the ENTER key.
   c. Power on all other workstations and press the HELP key at each workstation (a LOG-ON screen should be displayed on each CRT).
   d. Power on all printers and all tape drives.
8. Allow the customer to test the system using his programs. If the customer is satisfied with the operation of the system, officially turn the system over to the customer. (As of this printing, there is no official form to sign which effects turnover, nor has one been proposed. This should be merely a verbal notification given by the CE performing the installation.)

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 GENERAL

This chapter consists of preventive maintenance requirements and removal and replacement procedures for field-replaceable components in the VS-25/45 main frame.

5.2. PREVENTIVE MAINTENANCE

Periodic maintenance is essential to the proper operation of the VS-25/45 main frame and associated peripherals. Because of its design, the main frame requires a minimum amount of maintenance to ensure continued efficient operation.

5.2.1 TOOLS

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401

5.2.2 TEST EQUIPMENT

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022A	727-0119

5.2.3 MATERIALS

No special materials are necessary to perform main frame preventive maintenance.

5.2.4 PREVENTIVE MAINTENANCE SCHEDULE

Scheduled maintenance for the main frame will be performed annually, (in conjunction with a service call if no PM has been performed within a year) and is as follows:

PROCEDURE	ITEM	NOTES
Inspect/clean	Main frame filter (inside front cover)	If necessary
Inspect	Main frame interior	Look for dust & loose hardware. Clean.
Inspect/clean	Diskette drive read/ write heads	Refer to Shugart SA850 /851 Mnl. P/N 729-0862
Inspect	Main frame fans	Replace damaged fans. Paragraph 5.3.4.17
Check	Main frame voltages	Paragraph 5.2.5
Run diagnostics	Main frame & peripherals	Refer to Chapter 8 & Class 3000

5.2.5 MAIN FRAME VOLTAGE CHECKS

The following voltages, and their limits, are checked on the VS-25/45 at the Motherboard test points (figures 5-26). Adjustments to the switching power supply should not be performed in the field.

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+12.0	+11.1V to +12.8V	35mV RMS or 50mV Pk-to-Pk
-12.0	-11.5V to -12.5V	35mV RMS or 50mV Pk-to-Pk
+5.0	+4.5V to +5.7V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.5V to -5.5V	35mV RMS or 50mV Pk-to-Pk
IV (+12.0)*	+11.5V to +12.8V	35mV RMS or 50mV Pk-to-Pk

* - IV (Independent Voltage) was spare +12 Vdc, now used with regular +12 Vdc for current loading purposes.

5.2.6 PERIPHERAL PREVENTIVE MAINTENANCE

Refer to the appropriate documents in Class 3000 for PM procedures for all VS-25/45 associated peripherals.

5.3 CORRECTIVE MAINTENANCE

5.3.1 ALIGNMENTS

There are no alignment procedures for the VS-25/45 main frame.

For any corrective maintenance or alignments of the diskette drive, refer to the Shugart SA850/851 Maintenance Manual, WLI P/N 729-0862.

5.3.2 REMOVAL AND REPLACEMENT

These paragraphs describe the steps involved in removing and replacing or reinstalling all major field-replaceable components in the VS-25/45 main frame.

5.3.3 TOOLS

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401
Alcohol Pads	660-0130

NOTE

If a PCB is removed from the system for maintanance reasons, the contacts of the PCB may be cleaned with an alcohol pad. Do not use an eraser.

5.3.4 TEST EQUIPMENT

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022A	727-0119

5.3.4.1 Top Cover Removal

Remove the top cover as follows: (See figures 5-1 and 5-1a.)

1. At the rear of the main frame cabinet, two slot-head fasteners secure the top cover to the back panel. Use a wide-blade screwdriver to disengage the fasteners by turning them 1/2-revolution counterclockwise.
2. With the fasteners free, slide the top cover 2-3 inches to the front to disengage the top cover from the front cover catch. This frees the top cover from the cabinet.
3. At the front of the cabinet, firmly grasp the top cover on each side and lift it up and away from the cabinet.

Reinstall the top cover by reversing this procedure.

5.3.4.2 Front Cover Removal

Remove the front cover as follows: (See figures 5-2 and 5-2a.)

1. Remove the top cover as described above.
2. The front cover attaches to the upper and lower part of the cabinet by means of metal tabs inserted into slots on the cabinet. Grasp the top of the front cover firmly and lift up and out of the cabinet.

Reinstall the front cover by reversing this procedure.

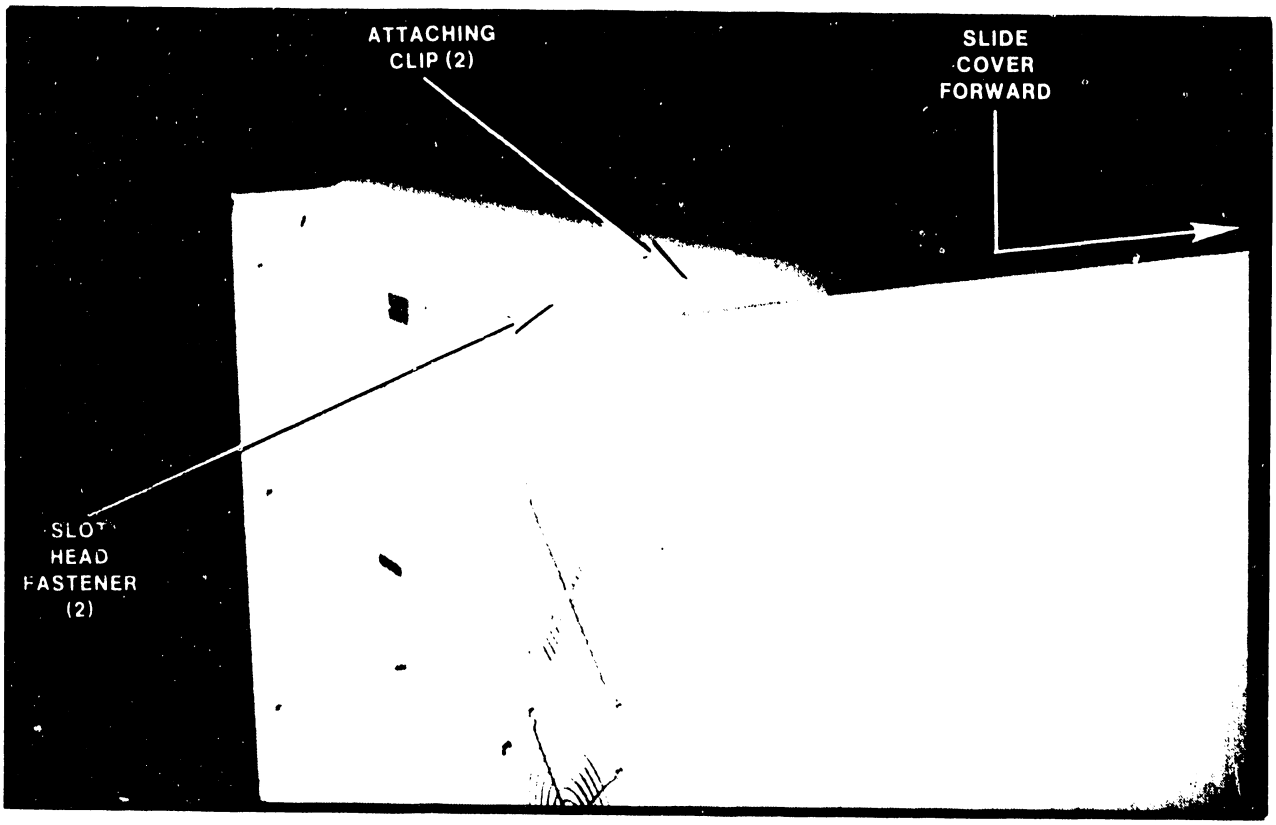


Figure 5-1. Top Cover Removal

Figure 5-1a. Top Cover Removal

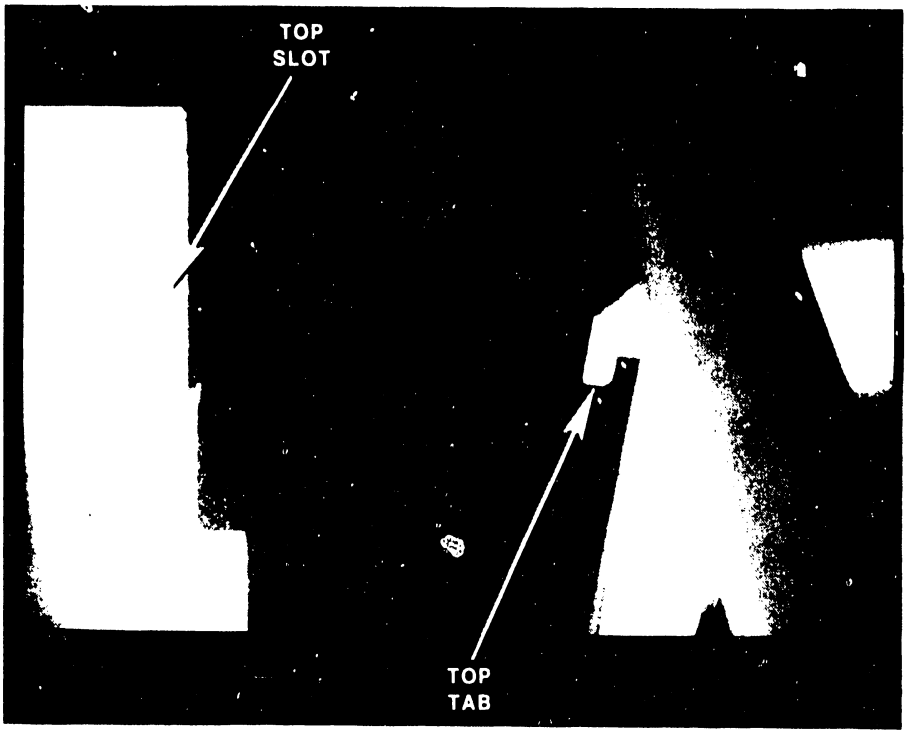


Figure 5-2. Front Cover Removal

Figure 5-2a. Front Cover Removal

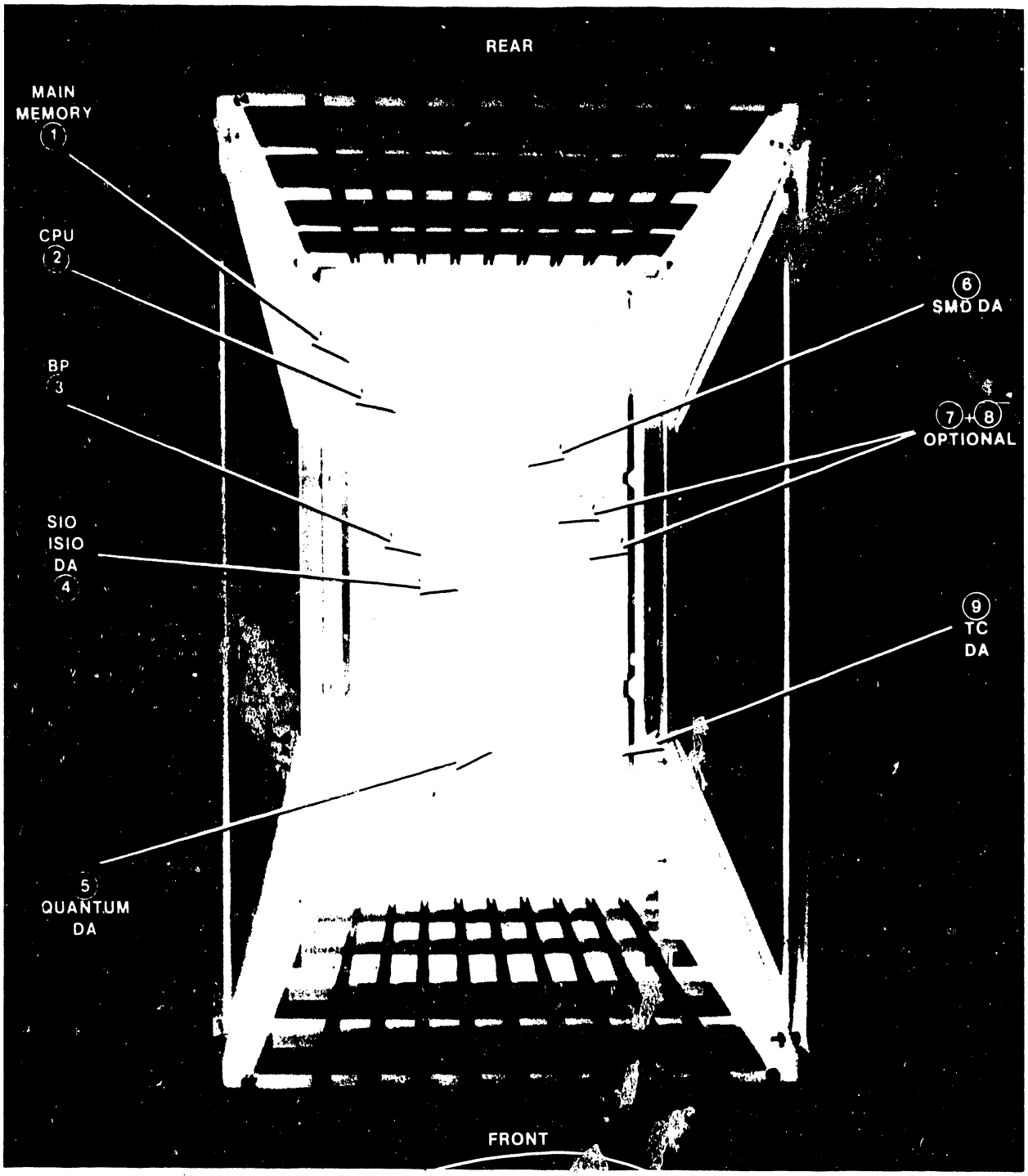


Figure 5-3. VS-25/45 Motherboard

5.3.4.3 CP Circuit Board Removal and Replacement

Three boards comprise the VS-25/45 processor; Main Memory, CPU, and BP. The removal and replacement procedures for the these boards are given in the order in which they are found on the Motherboard. (Figure 5-3.)

CAUTION

Be careful when replacing the large, flexible VS-25/45 boards. Make sure that all boards are seated properly in the correct Motherboard sockets. Don't damage the sockets when inserting the boards. Make sure all boards have their component sides facing left when viewed from the chassis front.

A board locator label (below) is on the front of the VS-25/45 board cage.

SLOT #	1	2	3	4	5	6	7	8	9
	MM	CP	BP	I/ODA1	I/ODA2	I/ODA3	I/ODA4	I/ODA5	I/ODA6

5.3.4.3.1 210-7900 Main Memory Board Removal and Replacement

1. Press the green Control Mode button. This prevents any disk I/O command in process from being halted prior to completion.
2. Power down the main frame by depressing the ac power On/Off switch to the '0' position.
3. Remove the top cover as described in paragraph 5.3.4.1.
4. Each circuit board is held in place by two snaplocks. One snaplock tab fits under the top edge of the front rail of the board cage assembly and the second snaplock tab fits under the top edge of the rear rail of the board cage assembly.
5. Remove the Main Memory board (figure 5-4) from Motherboard slot #1 by lifting the snaplocks to free the board from the Motherboard connectors. Once the board is free of the connectors, ease it straight up in the board guides and out of the board cage.
6. After checking the memory size switch settings on the board as shown in table 5-1, insert the new Main Memory board in the board guide and lower it to the Motherboard connector.

Table 5-1. VS-25/45 Main Memory Size Select Switch

SW. NO.	1	2	3	4	MEMORY SIZE (IN BYTES)
	ON	ON	OFF	OFF	512K (Min)
	ON	OFF	ON	OFF	768K
	ON	OFF	OFF	OFF	1024K (Max)

NOTE

Switch #5 is not used and is always OFF.

7. Make sure the board edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.
8. Push down on the snaplocks to seat the board in the Motherboard.

CAUTION

DO NOT USE EXCESSIVE FORCE WHEN PUSHING DOWN ON THE SNAPLOCKS.

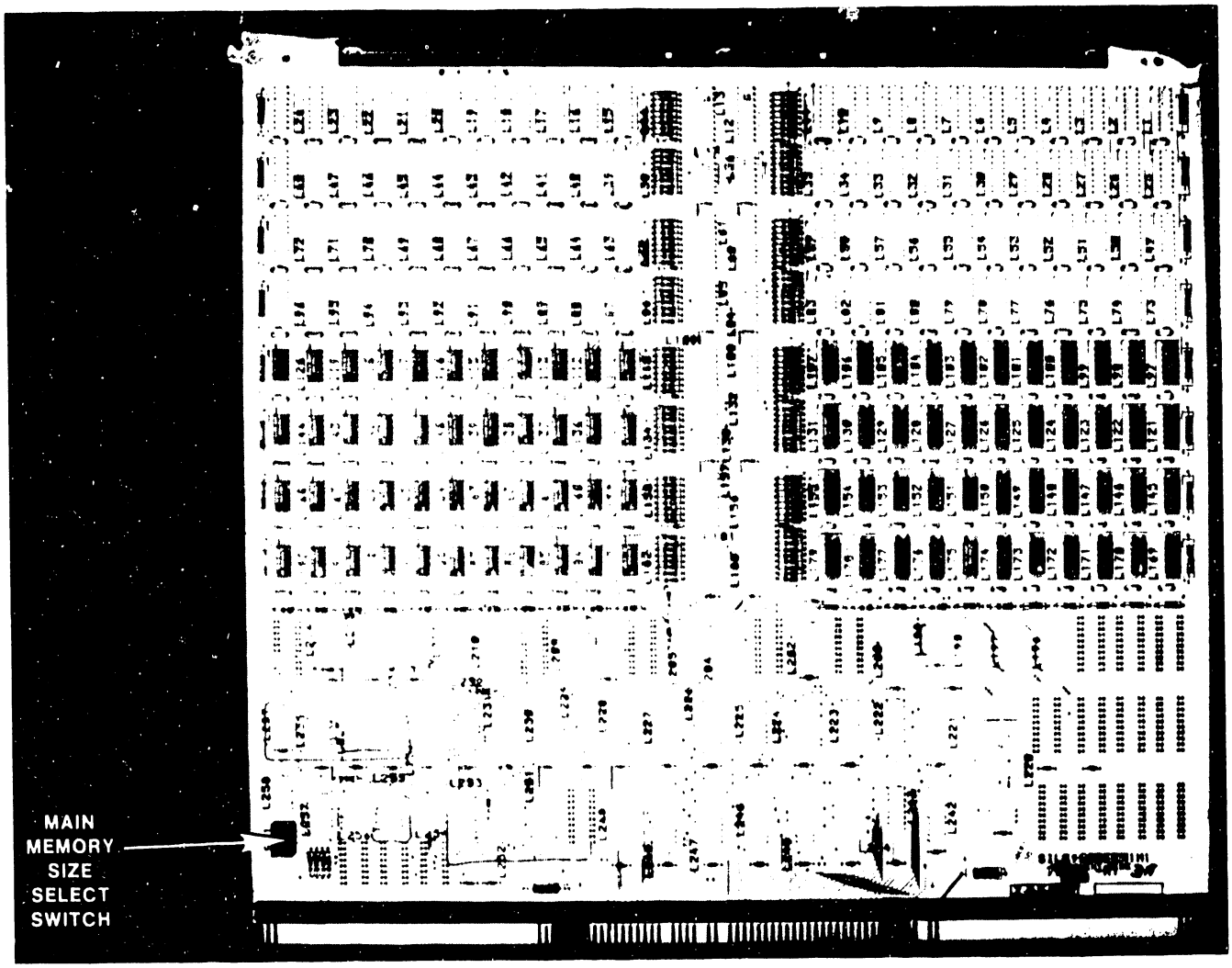


Figure 5-4. 210-7900 Main Memory Board

5.3.4.3.2 210-8303 CPU Board Removal and Replacement

1. Remove the CPU board (figure 5-5) from Motherboard slot #2 as described in 5.3.4.3.1. (Be careful the snaplock tabs don't damage the two top corner chips on the CPU.) If the CPU board is to be replaced, the System Identification PROM at location L228 most be removed for reinstallation on the new CPU board.
2. Make sure to reinstall the System Identification PROM at location L228 and install the new CPU board as described in 5.3.4.3.1.

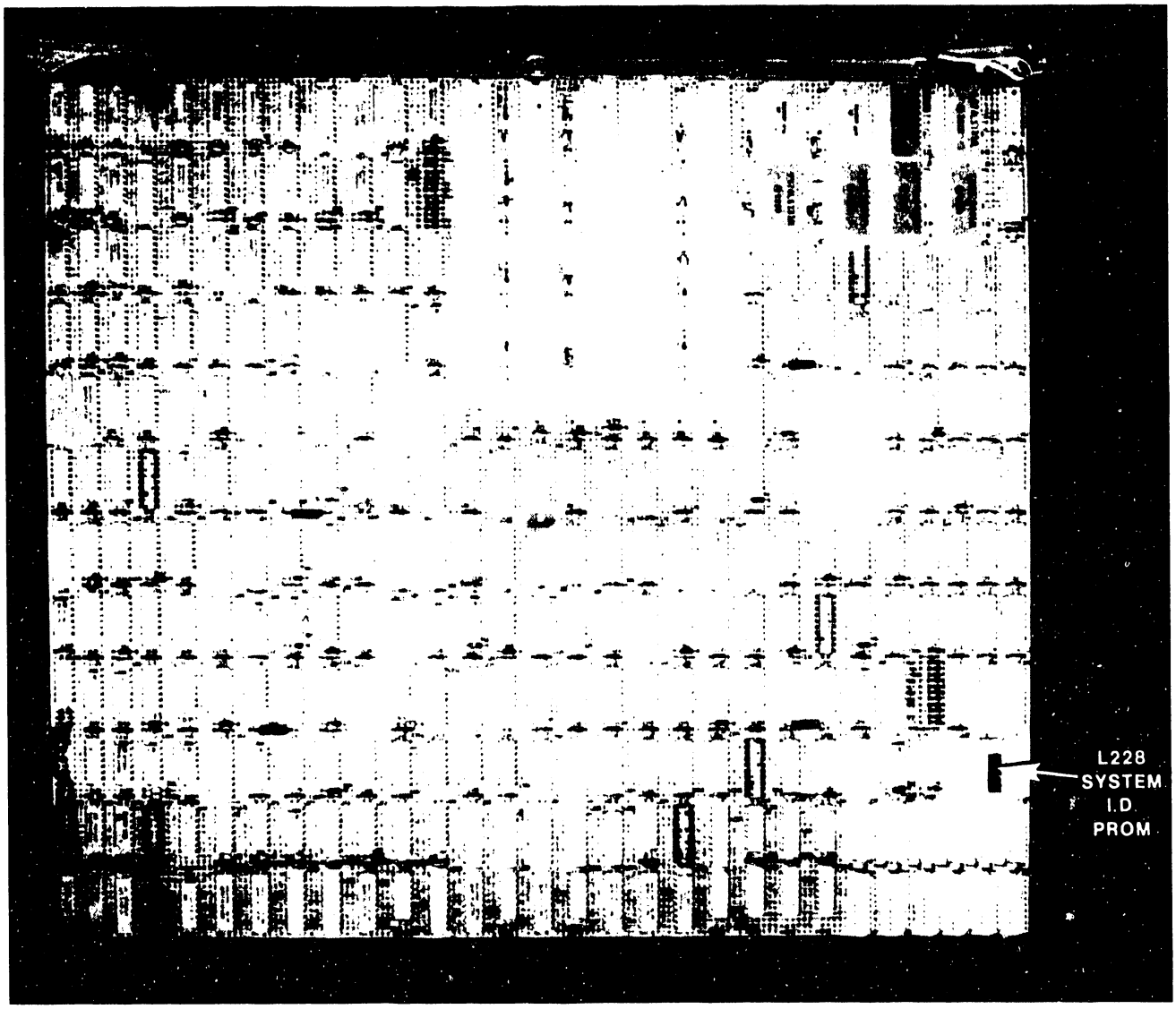


Figure 5-5. 210-8303 CPU Board

5.3.4.3.3 210-8304 BP Board Removal and Replacement

11. Before removing the BP board (figure 5-6) from Motherboard slot #3, disconnect the 26-pin connector from J1, the 34-pin connector from J2, and the 50-pin connector from J3 of the board.
12. Remove the board as described in 5.3.4.3.1.
13. Make sure that all of the BP Software Switches (table 5-2) are in the OFF position and install the new board as described in 5.3.4.3.1.
14. Reconnect all cables. (Refer to table 5-3.)

Table 5-2. VS-25/45 BP Software Switch Settings

SWITCH #	PURPOSE (WHEN ON)	NORMAL POSITION
8	Diagnostic mode. ON to read other switches	OFF
7	Bypass Core Diagnostic	OFF
6	Bypass Core Diagnostic & Diagnostic Monitor	OFF
5	Loop on Core Diagnostic	OFF
4	Reserved	OFF
3	Reserved	OFF
2	Data RAM clock	OFF
1	Data RAM clock	OFF

All switches must be OFF for normal operation of power-up diagnostics and system initialization.

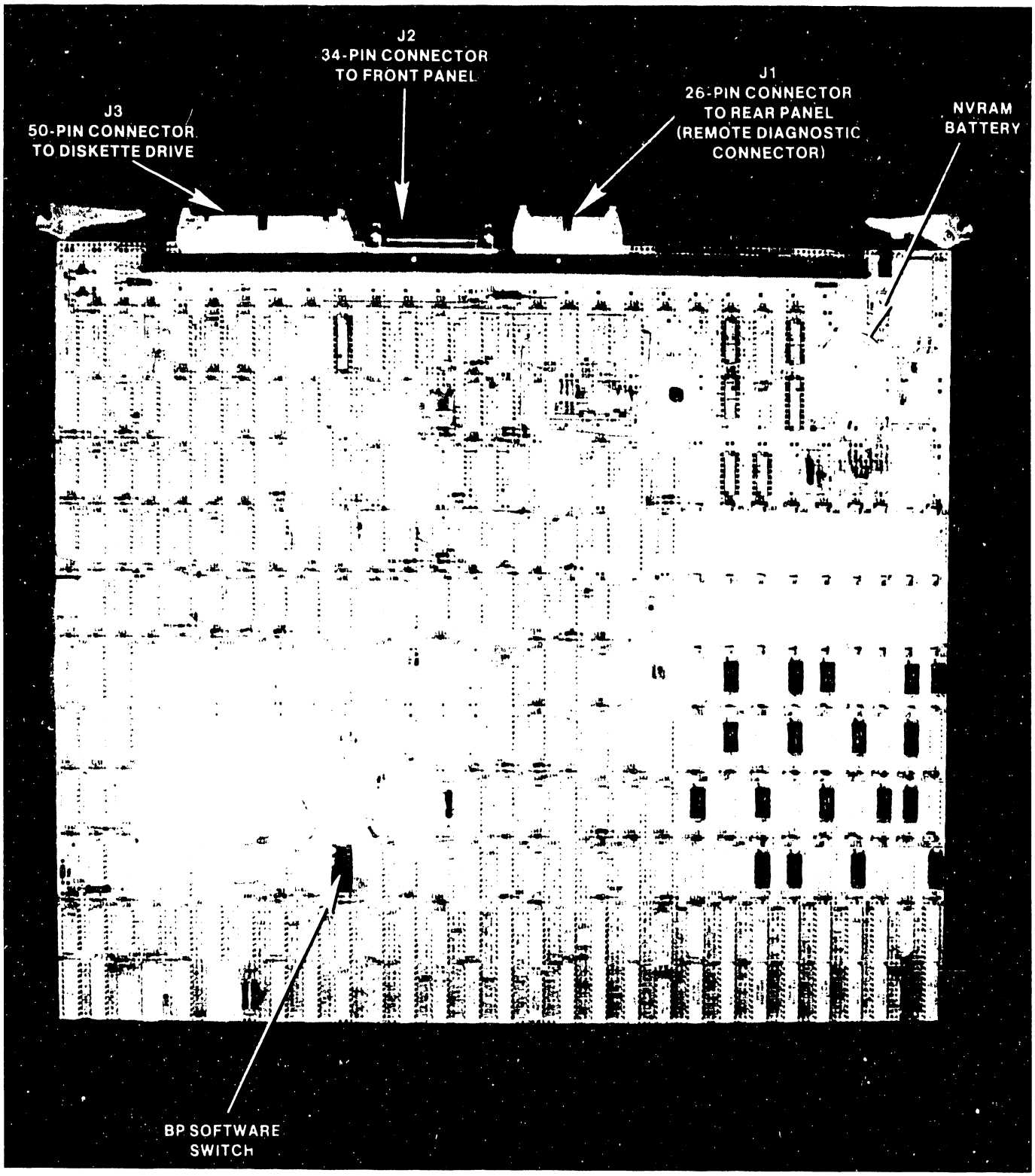


Figure 5-6. 210-8304 Bus Processor Board

Table 5-3. VS-25/45 Internal Signal Cable Connections

PC BOARD	CONNECTOR	CONNECTOR TYPE	CONNECTOR	PC BOARD
210-8304	J1	26-pin conn.	Remote	Rear Panel
"	J2	34-pin conn.	J1	210-7913 Front Panel
"	J3	50-pin "	J1	Diskette Drive
210-7906	J2	34-pin conn.	BNC/TNC	Rear panel
"	J3	" " "	" "	" "
"	J4	" " "	" "	" "
"	J5	" " "	" "	" "
210-8616	J3	34-pin conn.	BNC/TNC	Rear panel
"	J4	" " "	" "	" "
"	J5	" " "	" "	" "
"	J6	" " "	" "	" "
210-8325	J1	20-pin "B" conn.	J2	Quantum Dr #1
"	J2	" " "B" "	J2	" " #2
"	J3	50-pin Daisy "A"	J1	" " #2 to #1
210-8312	J1	60-pin conn.	"A"	Rear Panel
210-8313	J2	34-pin conn.	"B"	" "
210-8314	J3	" " "	"B"	" "
210-8315	J4	" " "	"B"	" "
	J5	" " "	"B"	" "
210-8337	J1	40-pin conn.	TC Conn	Rear Panel
"	J13	20-pin conn.	" "	" "
"	J2	26-pin conn.	" "	" "
"	J3	" " "	" "	" "
"	J4	20-pin conn.	Display	TC Front Panel
210-8637	J2A	26-pin conn.	TC Conn	Rear Panel
"	J3A	" " "	" "	" "
"	J13A	20-pin conn.	" "	" "
"	J2B	26-pin conn.	" "	" "
"	J3B	" " "	" "	" "
"	J13B	20-pin conn.	" "	" "
"	S1 & S2	16-pin conn.	Display	TC Front Panel

Table 5-4. VS-25/45 Internal Power Cable Connections

PC BOARD	CONNECTOR	CONNECTOR TYPE	CONNECTOR	PC BOARD
210-8010 Switching P/S	J3, 4, 8, 9, 11, &12	3-pin conn. (ac) (parallel) Note 1 (via conn. block)	J4 J4	Quantum Drive(s) Diskette Drive Fans
210-8011 Switching P/S	J4, 5, & 6 J7 J8	6-pin conn. (dc) (parallel) Note 1 4-pin conn. 8-pin conn.	J5 J5 J28 J29	Quantum Drive(s) Diskette Drive 210-7907 Mthboard " " "
210-8012 Switching P/S	J13 J6 J6	5-pin conn. #6 wire (+5 Volts) #6 wire (+/-0 Volts)	J28 J30 J31	210-7907 MthBoard " " " "

NOTE

1. Actual Switching Power Supply connections may vary depending on system configurations.

5.3.4.4 DA Circuit Board Removal and Replacement

There are five different styles of device adapters (DAs) used in the VS-25/45. The removal and replacement procedures for the different adapters are given in the order in which they are found in the Motherboard. (Figure 5-3.)

DAs are assigned to the Motherboard slots in the following order:

Table 5-5. VS-25/45 Recommended Adapter Placement

I/ODA#	MOTHERBOARD SLOT	ADAPTER TYPE		WLI P/N
1	4	25V27*	SIO	210-7906
1	4	25V37*	Intelligent SIO	210-8616
2	5	25V55	Quantum Disk	210-8325
3	6	25V50-1	1-port SMD Disk	210-8312
3	6	25V50-2	2-port SMD Disk	210-8313
3	6	25V50-3	3-port SMD Disk	210-8314
3	6	25V50-4	4-port SMD Disk	210-8315
4	7	Optional		
5	8	Optional		
6	9	25V76-1	Telecomm.	210-8337
6	9	25V76-2	Telecomm.	210-8637

* - Either the standard SIO or the Intelligent SIO may be installed in the VS-25/45, but not both.

5.3.4.4.1 210-7906 SIO DA Removal and Replacement

1. Press the green Control Mode button. This prevents any disk I/O command in process from being halted prior to completion.
2. Power down the main frame by depressing the ac power On/Off switch to the 0 position.
3. Remove the top cover as described in paragraph 5.3.4.1.
4. Each circuit board is held in place by two snaplocks. One snaplock tab fits under the top edge of the front rail of the board cage assembly and the second snaplock tab fits under the top edge of the rear rail of the board cage assembly.
5. Remove all connectors from the top of the Serial I/O Device Adapter (figure 5-7) in Motherboard slot #4 (I/ODA1). Note the position of all connectors for later reassembly.
6. Remove the device adapter from Motherboard slot #4 by lifting the snaplocks to free the adapter from the Motherboard connectors. Once the adapter is free of the connectors, ease it straight up in the board guides and out of the board cage.
7. Check the jumpers (figure 5-8) on the device adapter and install the adapter in Motherboard slot number #4. (Workstation 0 must be connected to port #0 of this DA. This is a microcode convention and MUST be adhered to. (Refer to paragraph 4.11.2.) Insert the new adapter in the board guide and lower it to the Motherboard connector.
8. Make sure the adapter edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.
9. Push down on the snaplocks to seat the adapter in the Motherboard.

CAUTION

DO NOT USE EXCESSIVE FORCE WHEN PUSHING DOWN ON THE SNAPLOCKS.

10. Reconnect all cables.

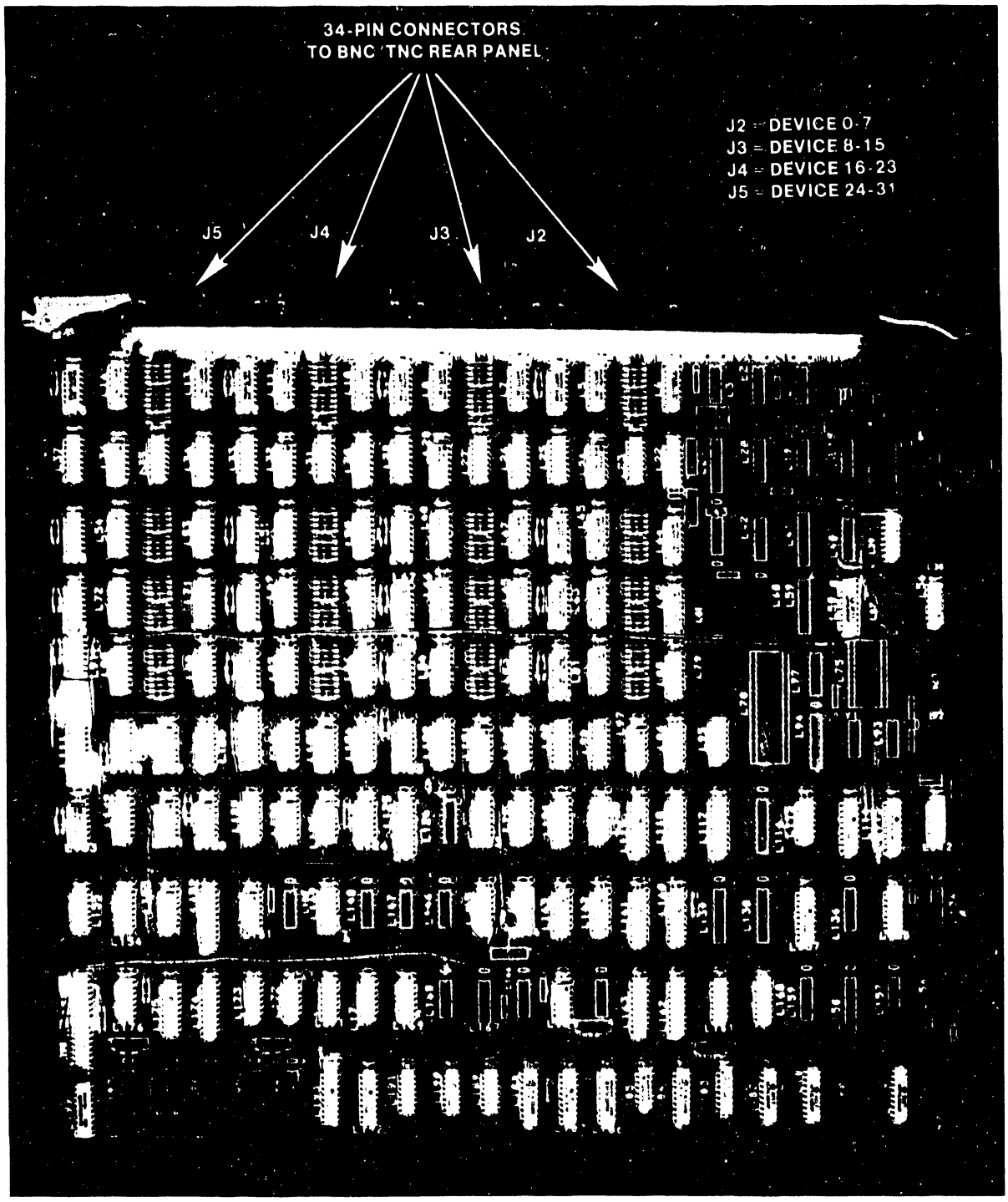


Figure 5-7. 210-7906 Serial I/O Adapter

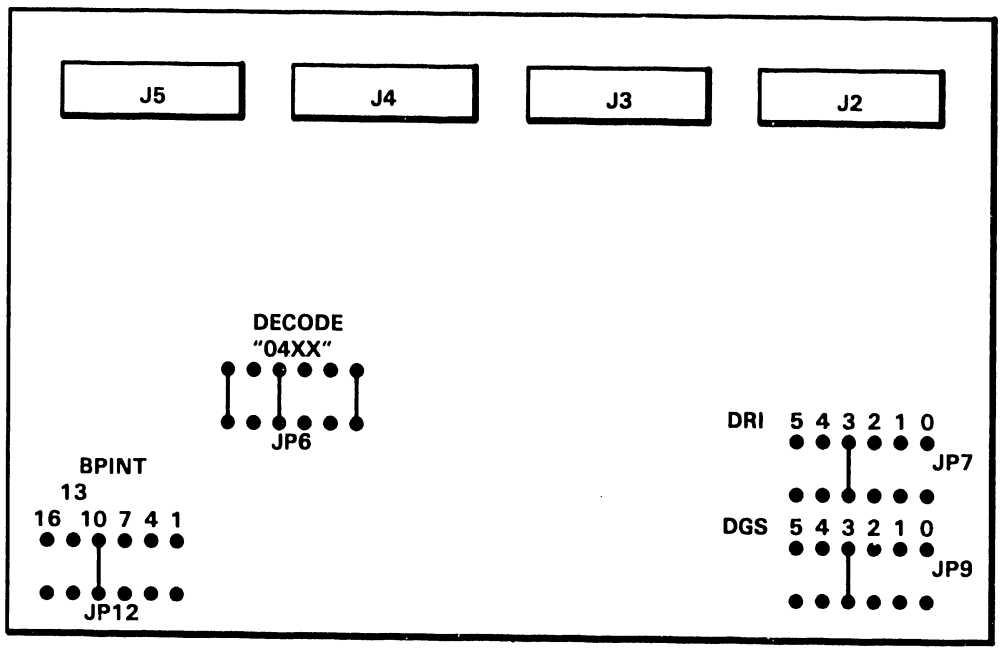


Figure 5-8. 210-7906 Serial I/O Adapter
Connector and Jumper Locations

5.3.4.4.2 210-8616 ISIO DA Removal and Replacement

1. Remove all connectors from the top of the Intelligent Serial I/O Device Adapter (figure 5-9) in Motherboard slot 4 (I/ODA1). Note the position of all connectors for later reassembly.
2. Remove the device adapter as previously described in 5.3.4.4.1.
3. Check the jumpers (figure 5-10) on the device adapter and install the new adapter in Motherboard slot #4 as described in 5.3.4.4.1.
4. Reconnect all cables.

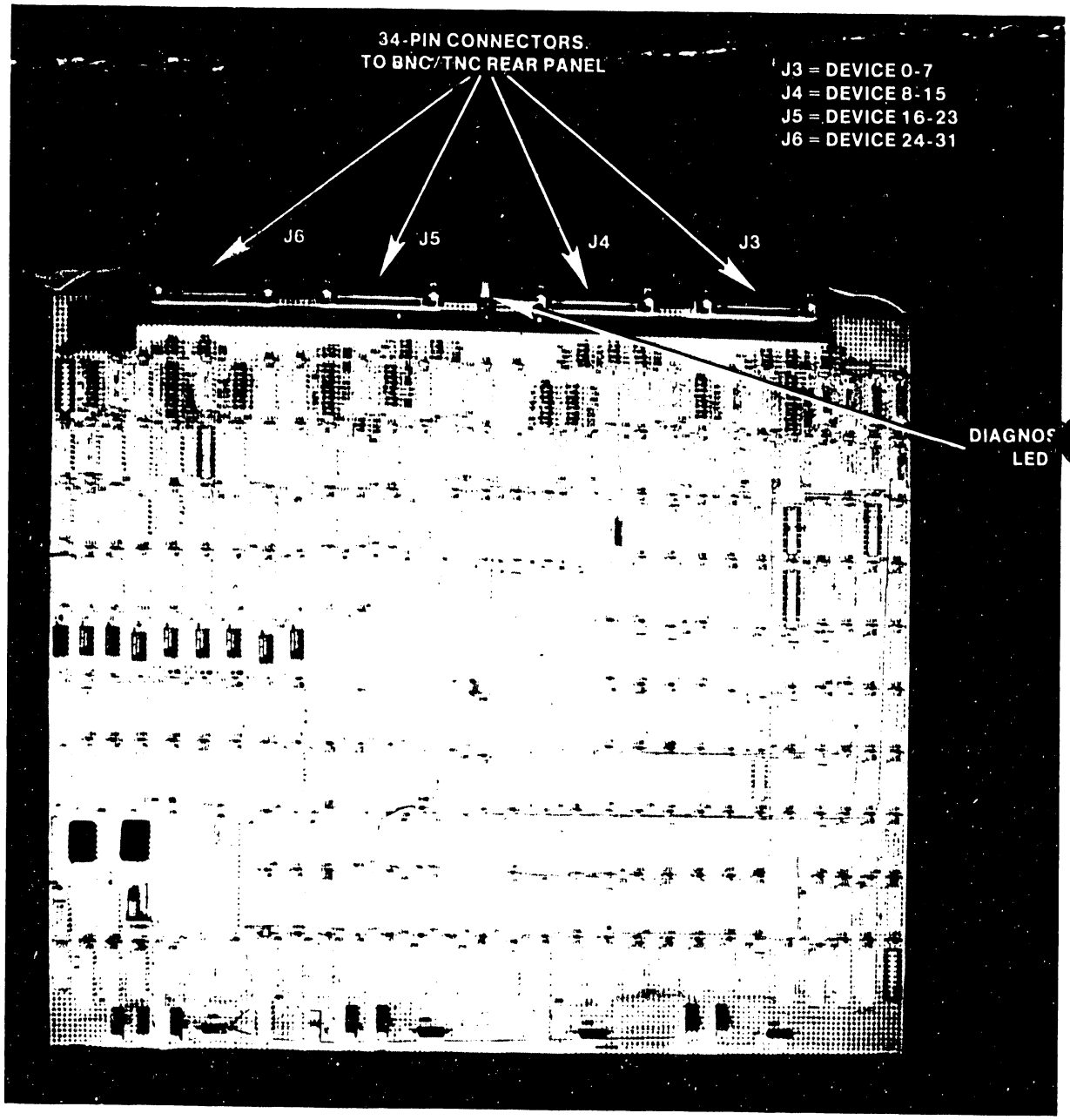
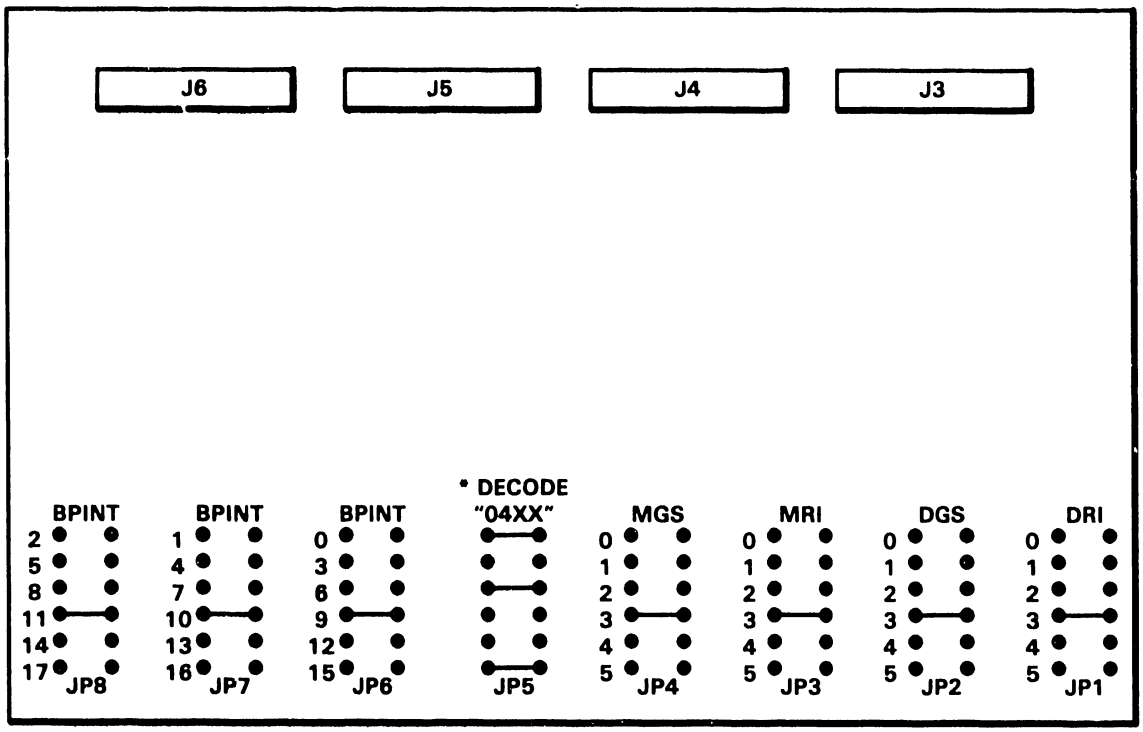


Figure 5-9. 210-8616 Intelligent Serial I/O Adapter



* STANDARD CONFIGURATION. OTHER POSSIBLE CONFIGURATIONS.

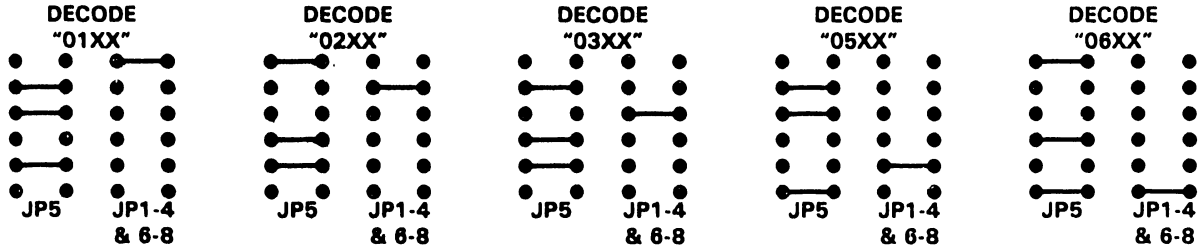


Figure 5-10. 210-8616 Intelligent Serial I/O Adapter
Connector and Jumper Locations

5.3.4.4.3 210-8325 Quantum DA Removal and Replacement

1. Remove all connectors from the top of the Quantum Device Adapter (figure 5-11) in Motherboard slot #5 (I/ODA2). Note the position of all connectors for later reassembly.
2. Remove the device adapter as previously described in 5.3.4.4.1.
3. Check the jumpers (figure 5-12) on the device adapter and install new the adapter in Motherboard slot #5 as described in 5.3.4.4.1.
4. Reconnect all cables.

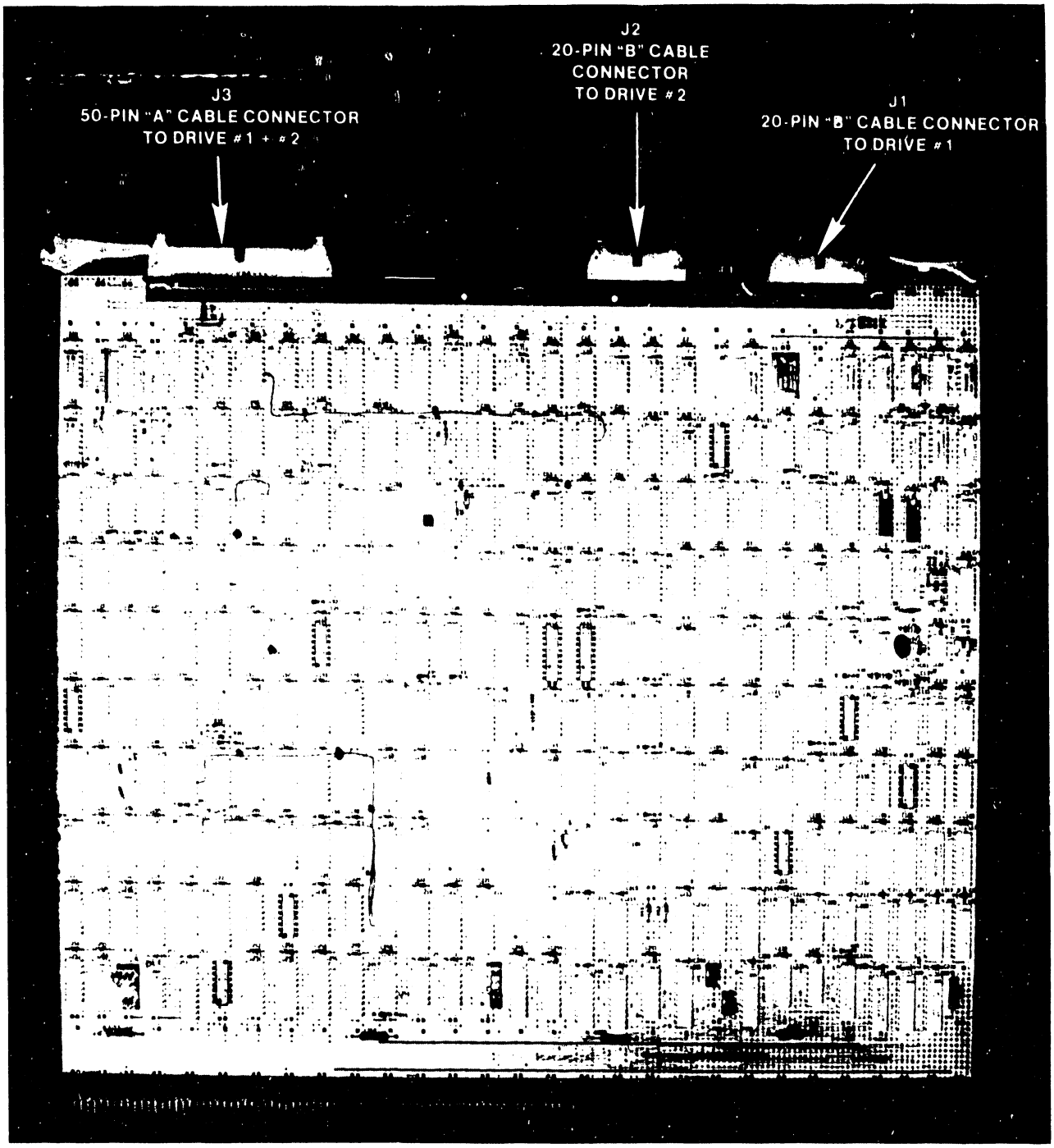


Figure 5-11. 210-8325 Quantum Disk Device Adapter

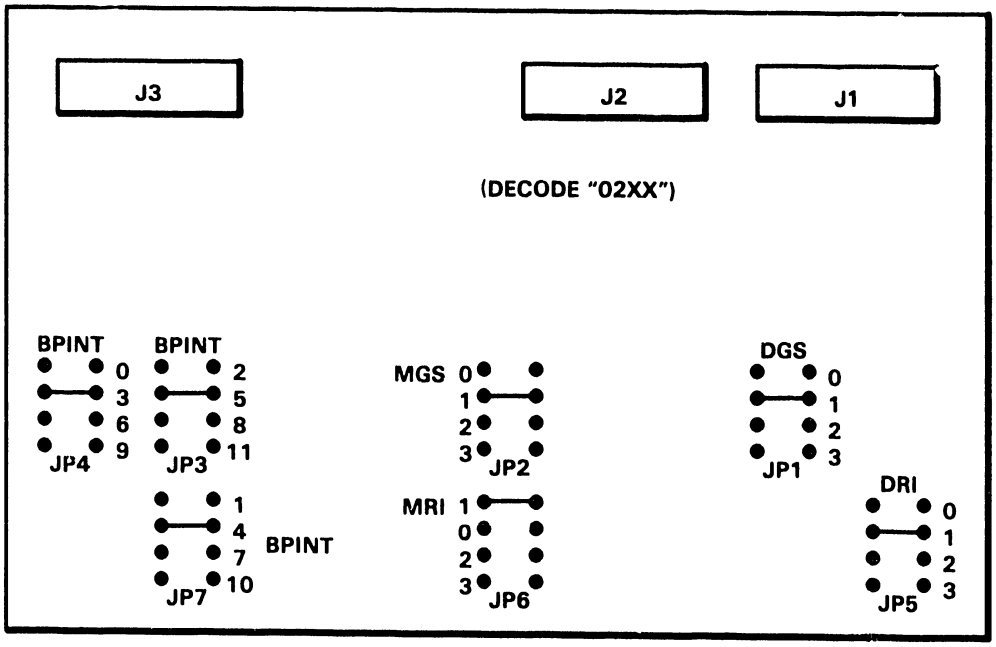


Figure 5-12. 210-8325 Quantum Device Adapter
Connector and Jumper Locations

5.3.4.4.4 210-8312/13/14/15 SMD DA Removal and Replacement

1. Remove all connectors from the top of the 210-8312, 8313, 8314, or 8315 SMD Device Adapter (figure 5-13) in Motherboard slot #6 (I/ODA3). Note the position of all connectors for later reassembly. (Note the position of all cables on the boards that are already installed in the system. Some of these cables may have to be removed to allow installation of the SMD DA.)
2. Remove the device adapter as previously described in 5.3.4.4.1.

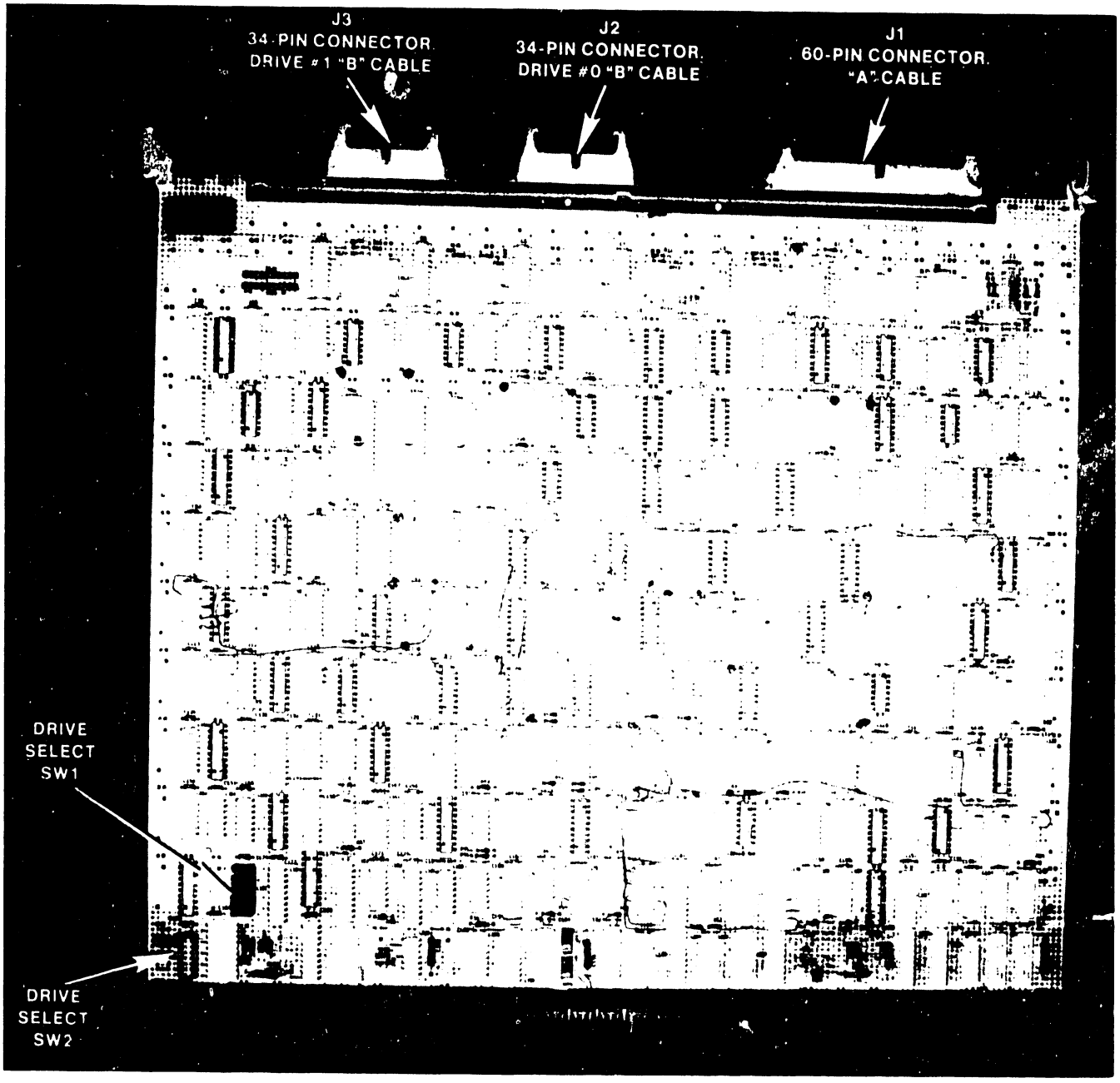
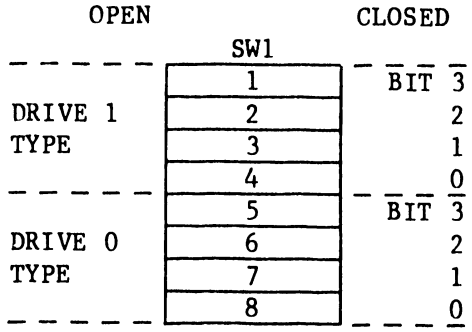


Figure 5-13. 210-8313 2-Port SMD Disk Device Adapter

3. The two 8-position disk device type switches, SW1 and SW2, define the type of drive connected to the SMD DA ports 0-3. Set the switches for the type of drive(s) connected to the system, referring to figures 5-13 and 5-14, and table 5-6. On the #210-8312 (1-port) and #210-8313 (2-port) adapters, SW2 may not be installed. The switch location may be hard-wired to indicate that ports number 2 and 3 cannot be used.



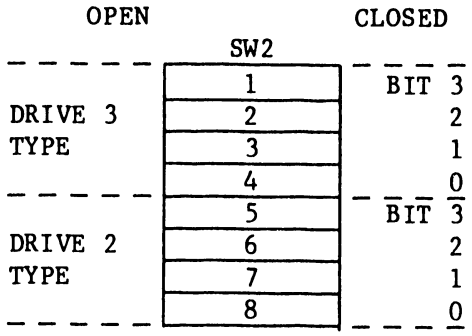


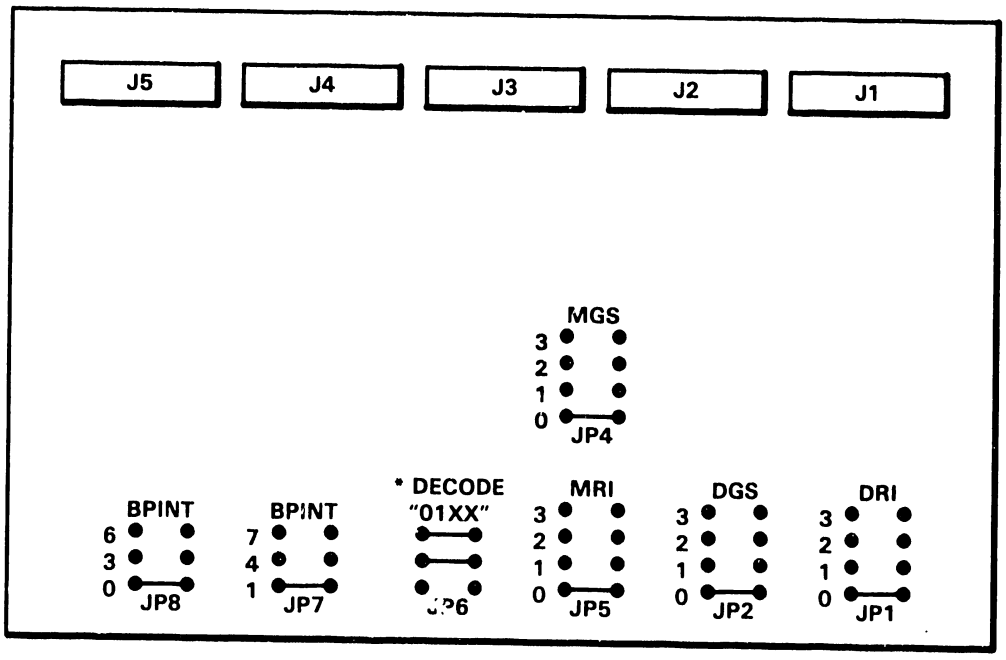
Figure 5-14. SMD Disk Device Adapter.
L192 and L211 Disk Device Type Switch Settings.

Table 5-6. SMD Disk Drive Types

DRIVE TYPE	BIT 3	BIT 2	BIT 1	BIT 0
75Meg SMD	Open	Open	Open	Open
288Meg SMD	Open	Open	Open	Closed
30Meg CMD	Open	Closed	Open	Open
60Meg CMD	Open	Closed	Open	Closed
90Meg CMD	Open	Closed	Closed	Open
76Meg NEC	Closed	Open	Open	Closed
620Meg FMD	Closed	Open	Closed	Closed
No Drive	Closed	Closed	Closed	Closed

4. Check all address selection jumpers as shown in figures 5-13 and 5-15. Make sure that no SMD DA addresses conflict with other DA addresses.

   Device address for a single SMD adapter = 01xx.
   Device address for a second SMD adapter = 02xx.



*** STANDARD CONFIGURATION. OTHER OPTIONAL CONFIGURATION.**

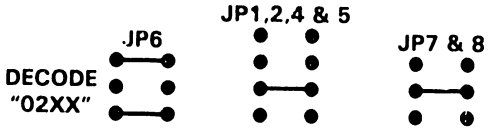


Figure 5-15. SMD Disk Device Adapter
Connector and Jumper Locations

5. Install the new 210-8312, 8313, 8314, or 8315 SMD DA in Motherboard slot #6 as described in 5.3.4.4.1.
6. Reconnect all cables.

5.3.4.4.5 210-8337/8637 TC DA Removal and Replacement

1. Remove all connectors from the top of the 1-port 210-8337-A Telecommunications Adapter (figure 5-16) or 2-port 210-8637-A Telecommunications Adapter (figure 5-17) in Motherboard slot #9 (I/ODA6). Note the position of all connectors for later reassembly. (Note the position of all cables on the boards that are already installed in the system. Some of these cables may have to be removed to allow removal and replacement of the Telecommunications Adapter.)
2. Remove the device adapter as previously described in 5.3.4.4.1.
3. Check the settings of the 8-position Address/Status switch(s) SW1 (1-port) and SW1 and SW2 (2-port). (See figures 5-16, 5-17, and 5-18, and table 5-7.)

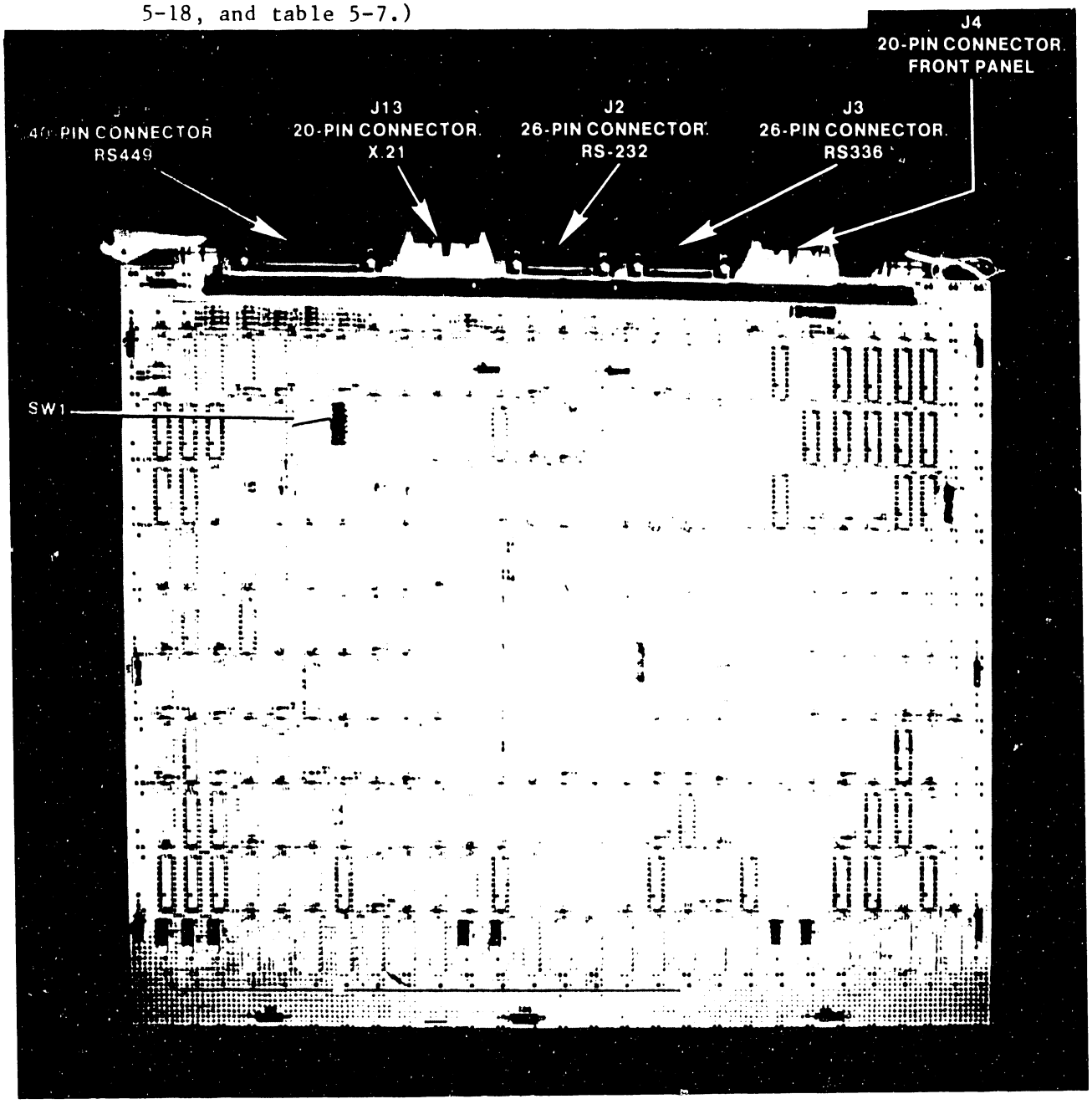


Figure 5-16. 210-8337 1-Port Telecommunications Adapter.

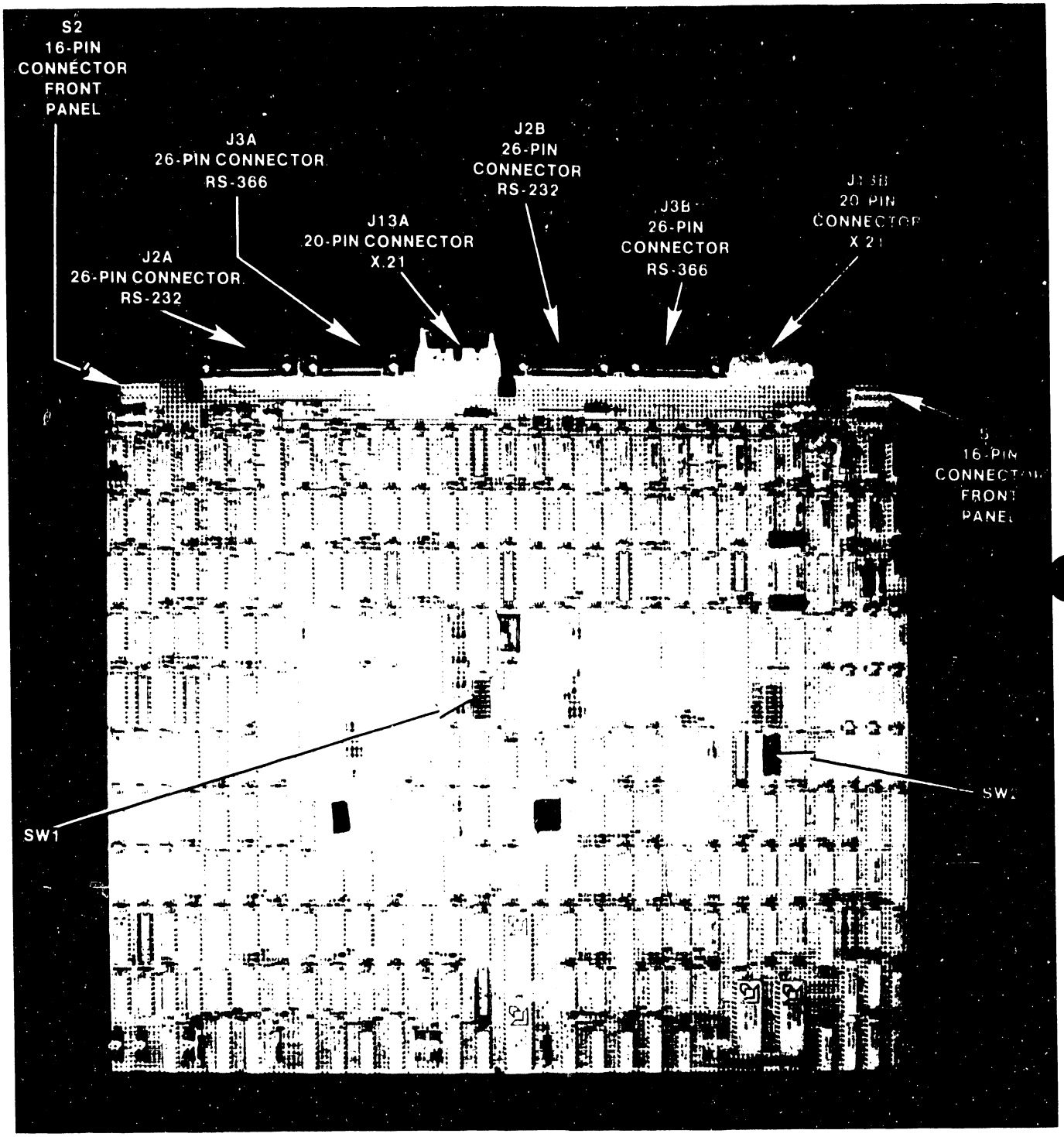


Figure 5-17. 210-8637 2-Port Telecommunications Adapter.

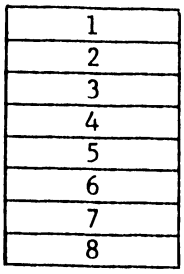


Figure 5-18. 210-8337/8637 Telecommunications Adapter. Address/Status Switch SW1/SW2.

NOTES

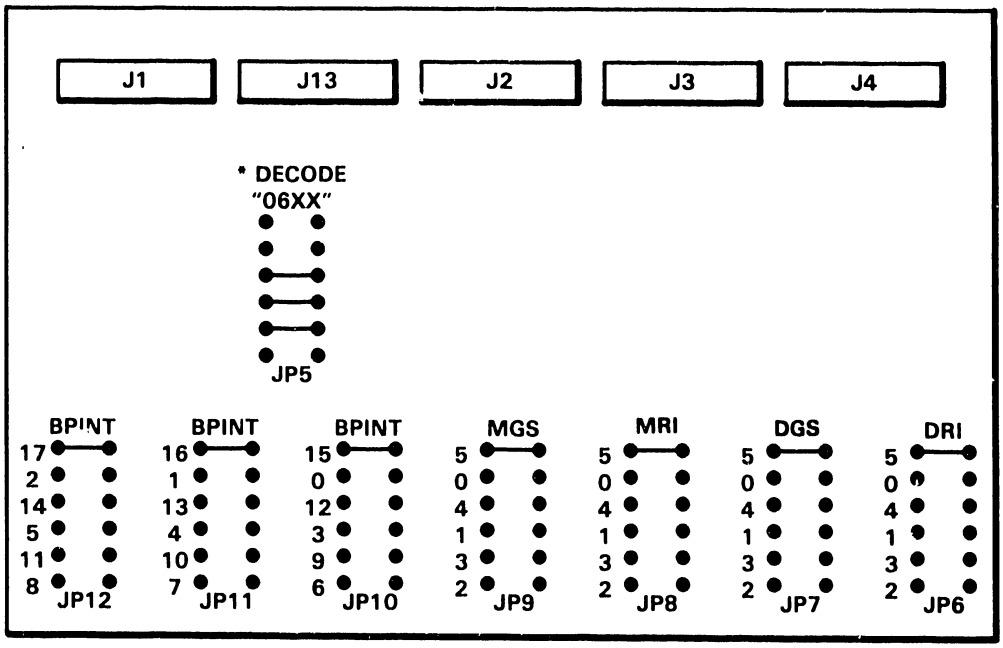
1. SW1 is for 1-port TC adapter and SW1 and SW2 are for 2-port TC adapter.
2. All switches should be off unless the 64K byte RAM option or the X.21 Interface option have been ordered.

Table 5-7. SW1/SW2 Address/Status Switch Settings

SW#	SWITCH NAME	PURPOSE (WHEN ON)	NORMAL POSITION
1	Loop on Bit	Repeat TC DA test sequence	OFF
2	Ext. Loopback	To support external RS232 loopback connector	OFF
3	Loop on Error	Repeat any test in error	OFF
4	Stop on Error	Holds error code in TC DA LED display. Needs SW3 ON	OFF
5	Bypass Power-up	Bypass all power up tests	OFF
6	Loop On Test	Repeat current TC DA test	OFF
7	X.21 Option	Supports X.21 interface	OFF
8	128K Option	Supports 128K byte TC DA memory	OFF

4. Check all address selection jumpers as shown in figures 5-19 and 5-20. Make sure that no TC DA addresses conflict with other DA addresses.

Device Address for a single TC DA = 06xx.
Device Address for a second TC DA = 05xx.
Device Address for a third TC DA = 03xx.
Device Address for a fourth TC DA = 02xx. (See next note 1.)
Device Address for a fourth TC DA = 01xx. (See next note 2.)



* STANDARD CONFIGURATION USED WHEN SYSTEM HAS ONLY ONE TC DA. OTHER POSSIBLE CONFIGURATIONS.

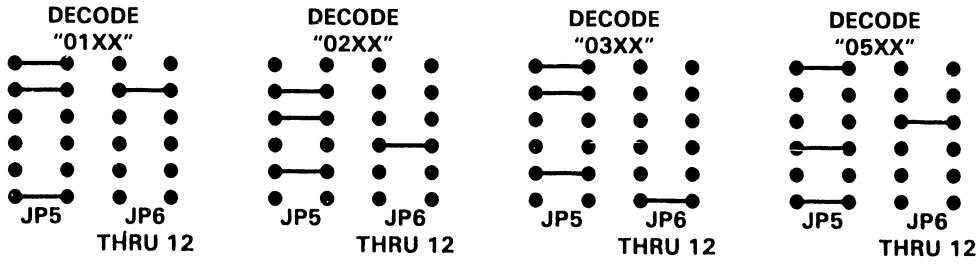


Figure 5-19. 210-8337 1-Port TC Device Adapter Connector and Jumper Locations

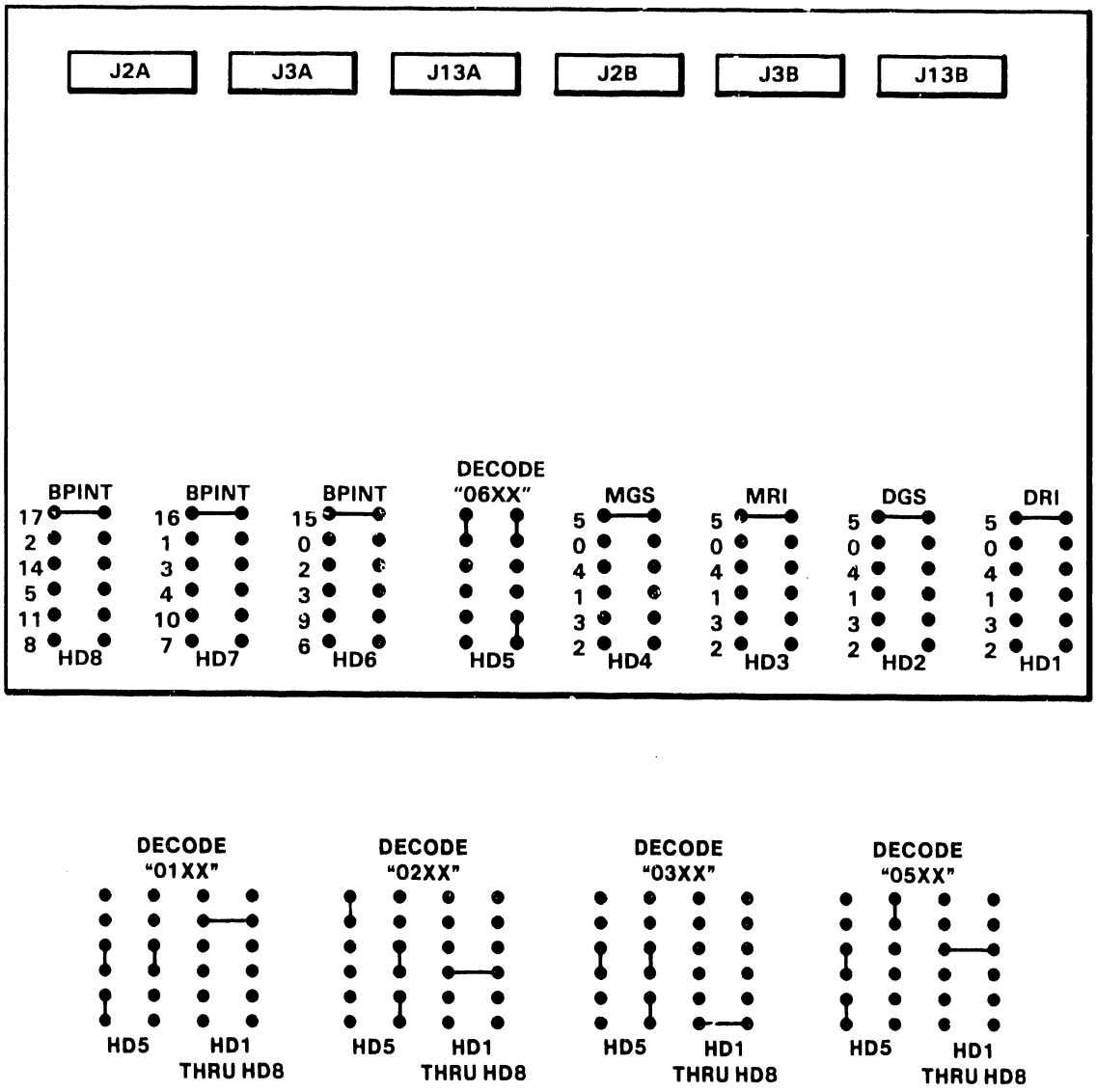


Figure 5-20. 210-8637 2-Port TC Device Adapter
Connector and Jumper Locations

NOTES

1. Device address of 02xx may be used only if system has no Quantum DA.
2. Device Address of 01xx may be used only if system has no SMD DA.

5. Install the new device adapter in Motherboard slot #9 as described in 5.3.4.4.1.
6. Reconnect all cables.

5.3.4.5 Front Panel Removal

The 210-7913 Front Panel board (figure 5-21) in the VS-25/45 is attached to the Front Panel frame. Remove the Front Panel board as follows:

1. Power down the main frame by depressing the ac power On/Off switch to the '0' position.
2. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
3. Remove the 34-pin connector from J1 of the 7913 board.
4. Remove the 2-pin Local/Remote key lock switch connector from J2 of the 7913 board.
5. Remove the four Phillips screws from the stand-offs on the 7913 board.
6. Remove the board.

5.3.4.6 Front Panel Replacement

Reinstall the Front Panel by reversing the above procedures.

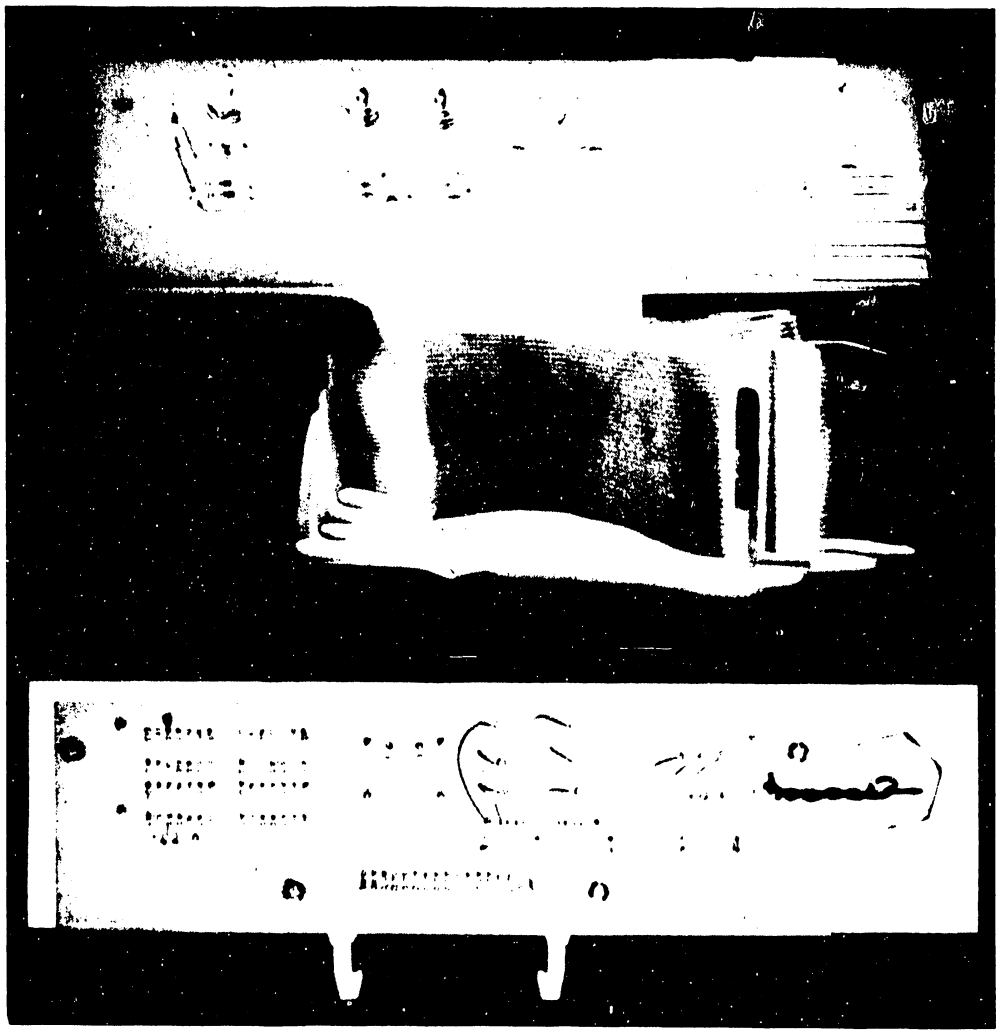


Figure 5-21. Front and Rear View of 210-7913 Front Panel Board

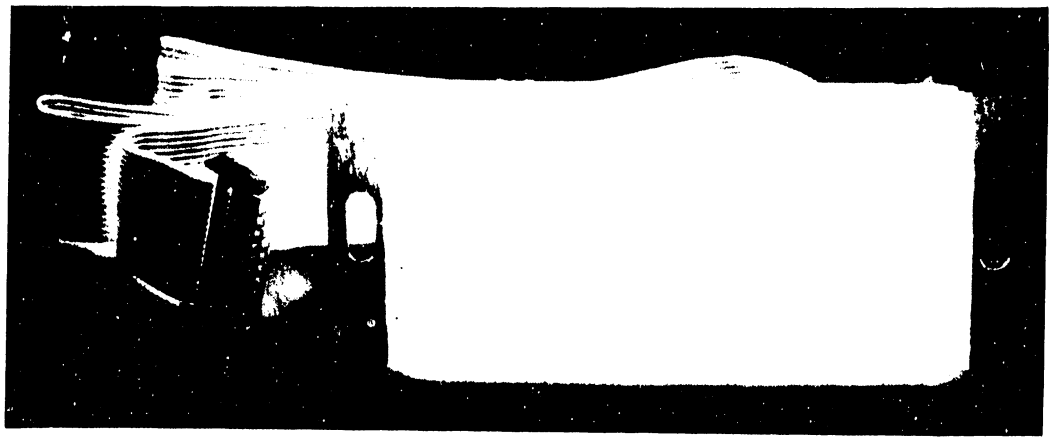
5.3.4.7 TC DA Front Indicator/Control Panel Removal

The 25V76-1/2 TC DA Front Indicator/Control Panel, WLI P/N 270-0814, (figure 5-22) is mounted on the VS-25/45 Front Panel (figure 3-2) to the left of the diskette drive. It is not necessary to remove the diskette drive assembly to remove or reinstall the panel.

1. Power down the main frame by depressing the ac power On/Off switch to the '0' position.
2. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
3. Remove the 20-pin connector from J1 of the Indication/Control panel.
4. Remove the two nuts and two lock washers from the inside of the Indicator/Control Panel.
5. Remove the panel.

5.3.4.8 TC DA Front Indicator/Control Panel Replacement

1. To reinstall the panel, reverse the above procedure.



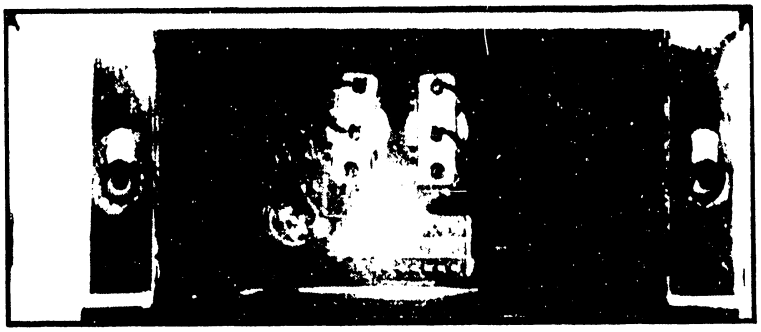


Figure 5-22. Front and Rear View of 270-0814
Telecommunications Adapter Indicator/Control Panel

5.3.4.9 Motherboard Removal

Removal of the 210-7909 CPU Motherboard should be done only if it has been determined conclusively that the problem is in the Motherboard. The following steps describe the procedures involved in removing the VS-25/45 Motherboard.

CAUTION

When reinstalling the Motherboard, make sure no conductive (metal) parts of the Motherboard come in contact with the frame. This could cause a short to ground on the Motherboard resulting in damage to CPU or I/O boards when power is applied.

To remove the Motherboard: (Figures 5-23 and 5-24.)

1. Press the green Control Mode button. This prevents any disk I/O command in process from being halted prior to completion.
2. Power down the main frame by depressing the ac power On/Off switch to the '0' position and unplug the power connector from the power source receptacle.
3. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
4. Note the position of all cables on the circuit boards for later reassembly and then remove all board cables.
5. Remove all circuit boards. (Paragraph 5.4.)
6. Disconnect the 9-pin connector from J28 and the 6-pin twisted pair connector from J29 at the front of the Motherboard. DO NOT remove the two #6 wire cables (+5 Volts and +/-0 Volts) at the front of the Motherboard at this time.
7. Remove the two 5/16 inch Whiz Lock screws that secure the front of the board cage assembly to the frame.

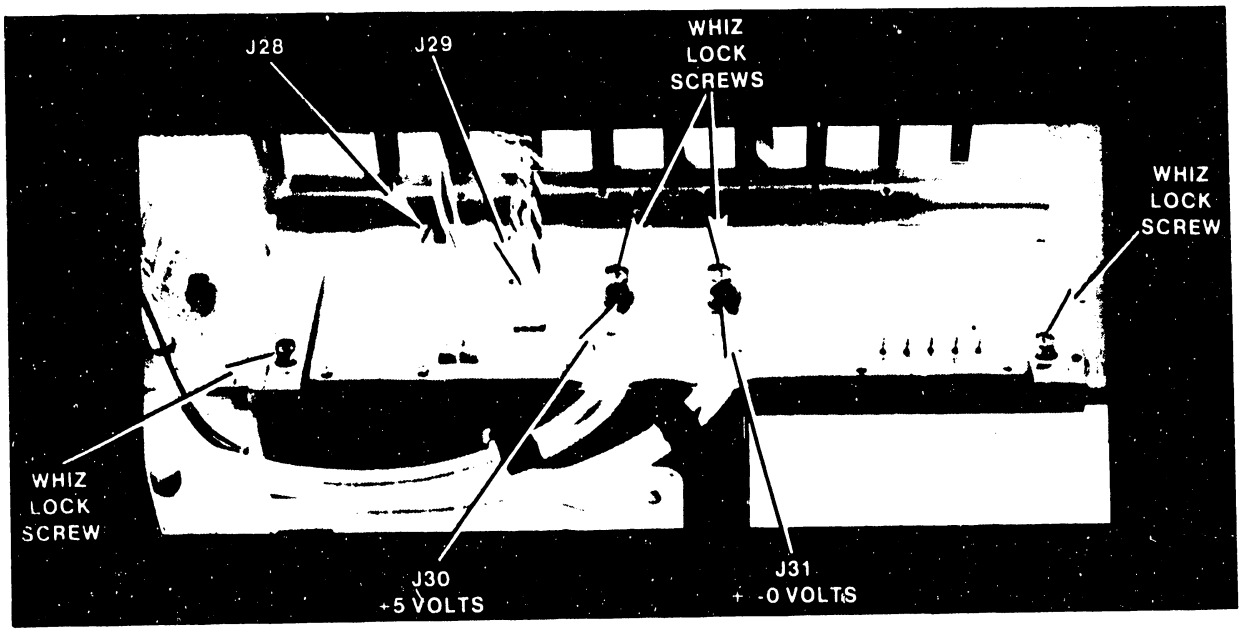


Figure 5-23. Motherboard Power Connectors

8. The rear of the board cage assembly is attached to the frame by two studs seated in slots in the frame. Pull the entire board cage assembly forward slightly and lift up on the rear of the cage to disengage the studs from the slots.
9. Pull the entire board cage assembly forward about 6 inches.
10. Make sure that the two #6 wire cables at the front of the Motherboard are labeled +5 Volts (J30) and +/-0 Volts (J31).
11. Remove the two SILVER 11/32 inch Whiz Lock screws securing the #6 wire cables to the front of the Motherboard. The two screws are secured by Whiz Lock nuts under the Motherboard. Remove the Whiz Lock screws while holding the Whiz Lock nuts under the Motherboard.
12. With all screws, nuts, and cables removed, grasp the board cage assembly and pull it forward and out of the main frame.
13. Set the cage assembly out on the floor or on a table.
14. Remove the 30 Phillips screws from the top of the motherboard.
15. Carefully slide the Motherboard out of the front of the board cage assembly. Do not bend the pins on the bottom of the Motherboard.

5.3.4.10 Motherboard Replacement

To replace the Motherboard:

1. To reinstall the board cage assembly, reverse the above procedure.
2. Make sure that all screws and nuts are reinstalled in their proper locations, and that all wires and cables are installed correctly.
3. Make sure that no metal part of the Motherboard makes contact with the main frame board cage assembly (see CAUTION above).
4. Reinstall all circuit boards (paragraph 5.4) as shown in figure 5-3 and make sure that all board cabling is installed correctly.

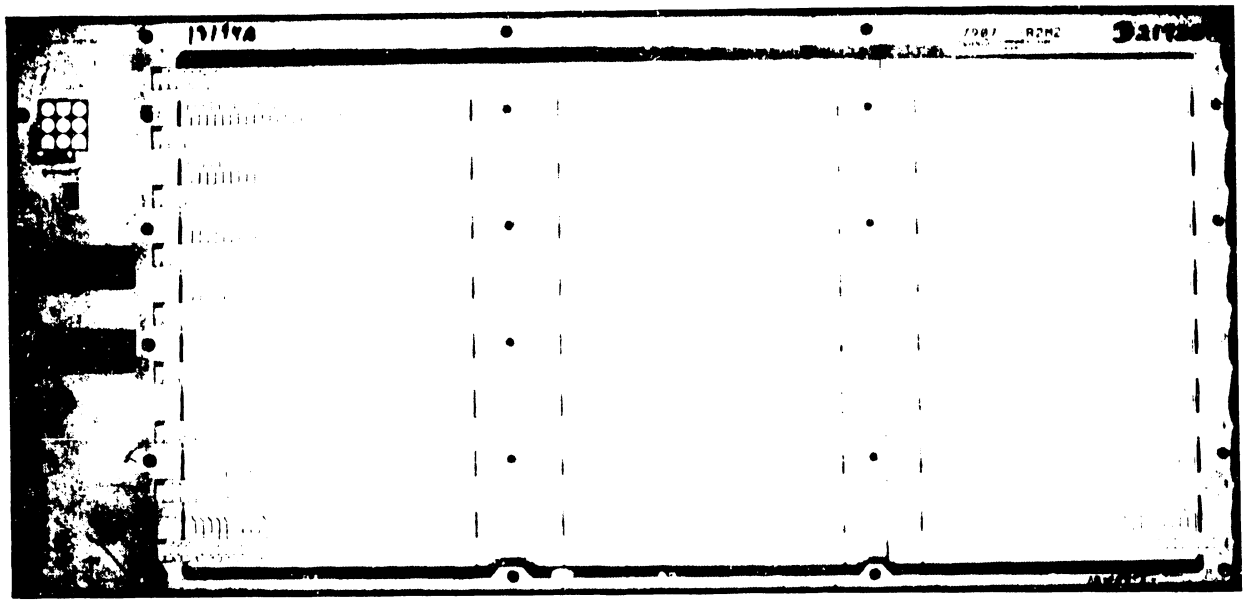


Figure 5-24. Motherboard

5.3.4.11 Power Supply Removal

WARNING

```
**************************************************************
*                                                            *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY        *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND          *
*     CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN       *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.   *
*                                                            *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER            *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                   *
*                                                            *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC   *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,       *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO    *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO       *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                    *
*                                                            *
**************************************************************
```

To remove the 270-0735 Switching Power Supply: (See figure 5-25.)

1. The power supply is located to the left of the Quantum disk drive(s).
2. Power down the main frame by depressing the ac power On/Off switch to the '0' position and unplug the power connector from the power source receptacle.
3. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
4. Remove the single 5/16" hex bolt located directly under the front edge of the supply.
5. Slide the supply far enough forward to expose the cables at the rear of the supply. (There is a piece of foam sound insulating material to the right of the supply. Be careful not to tear the foam when removing and installing the supply.)
6. Note the locations (table 5-4) of the cables on the rear of the supply for reinstallation and then remove the cables. The cables are keyed to ensure proper insertion.
7. Firmly grasp the power supply under the front edge and pull the supply out of the cabinet.

5.3.4.12 Power Supply Replacement

To replace the 270-0735 Switching Power Supply:

1. To reinstall the power supply, reverse the above procedure.
2. After making sure that the ac power ON/OFF switch on the Power Panel is in the '0' position, plug the main frame power connector into the power source receptacle.
3. Perform the following in the sequence given:
   a. Depress the ac power ON/OFF switch to the '1' position.
   b. Make sure that the ac POWER ON lamp on the Power Panel is lit and that the main frame cooling fans are turning.

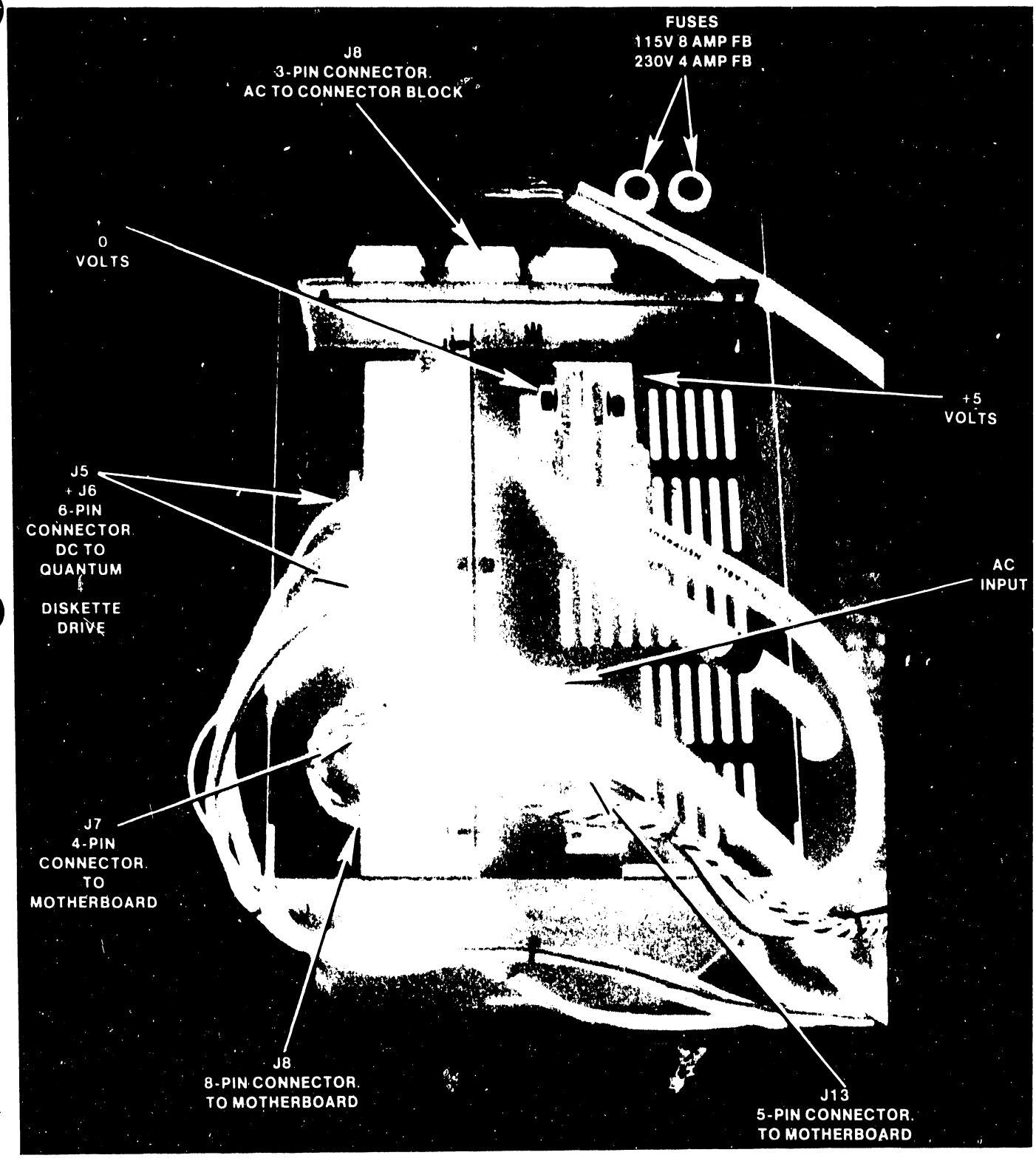


Figure 5-25. Rear View of Power Supply

c. Wait 5 seconds after ac power is applied and then press the DC Initialize pushbutton.
d. Make sure that the DC Power On LED on the power supply, the Power On LED on the front panel, and the HEX Display LEDs are lit after the DC Initialize pushbutton has been pressed. If the HEX Display LEDs go out after 2 seconds, there is a problem with the dc voltage compare circuit in the power supply.
e. The following voltages should be checked on the VS-25/45 at the Motherboard test points. (It is not intended that adjustments on the switching power supply be performed in the field.)

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+12.0	+11.1V to +12.8V	35mV RMS or 50mV Pk-to-Pk
-12.0	-11.5V to -12.5V	35mV RMS or 50mV Pk-to-Pk
+5.0	+4.5V to +5.7V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.5V to -5.5V	35mV RMS or 50mV Pk-to-Pk
IV (+12.0)*	+11.5V to +12.8V	35mV RMS or 50mV Pk-to-Pk

* - IV (Independent Voltage) was spare +12 Vdc, now used with regular +12 Vdc for current loading purposes.

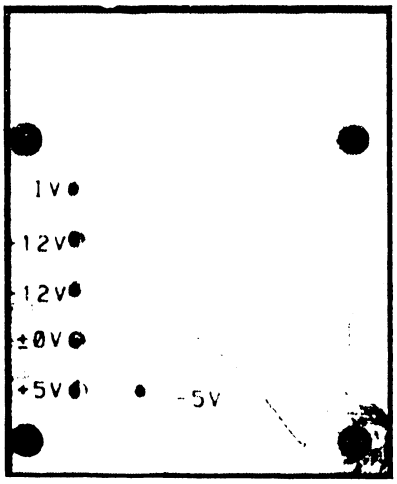


Figure 5-26. Motherboard Voltage Test Points

5.3.4.13 Quantum Drive Removal

To remove a drive:

1. Power down the main frame by depressing the ac power On/Off switch to the '0' position.
2. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
3. Quantum drive #1 is the right hand drive and drive #2 is the left hand drive. The drive(s) is bolted to the cabinet by one 5/16 inch hex bolt at the front of the drive(s) which is secured by a Pem nut under the cabinet. Make sure the drive has stopped turning and then remove the hex bolt while holding the Pem nut under the cabinet.

4. Carefully slide the drive forward. The "A" and "B" signal, and ac and dc power cables are connected to the rear of the drive. Note the locations of these cables for reinstallation and then remove the cables. The cables are keyed to ensure proper insertion.
5. Slide the drive forward and out of its bayonet slide on the bottom of the drive. Remove the drive from the cabinet, avoiding contact between the drive and adjacent equipment.
6. Lock the actuator and the drive pulley. (Figures 5-27 and 5-28.)

5.3.4.14 Quantum Drive Replacement

To replace a drive:

1. Tilt the new Quantum drive and loosen the 11/32 inch hex nut securing the locking clip on the Quantum drive pulley. (See figure 5-27.)
2. Rotate the locking clip away from the pulley.
   DO NOT ROTATE THE PULLEY.
3. Retighten the 11/32 inch hex nut.
4. Unlock the actuator (see figure 5-28) by rotating the actuator lock counterclockwise as far as it will go (approximately 1/2 turn). The embossed arrow will now point to RUN.
   DO NOT FORCE THE ACTUATOR.
5. Before installing the drive, check the revision level, options jumpers, and the terminator IC of the Quantum Drive Control PC board (Quantum #20-2000). They should be as follows. (See figure 5-29.)
   a. PC board should be at revision level E or above. PC boards that are revision level E and above will have a type 7438 IC at location 1J. If the PC board is below revision level E, it can be used in a VS-25/45 if the system contains only one Quantum drive. If the system contains two Quantum drives, a PC board below revision level E can't be used.
   b. Minus (-) power selection to the -15 Vdc connection.
   c. Rezero selection between pin C and pin 5.
   d. Drive Select to the appropriate DS pin. If the drive is to be #1, install the jumper on DS1; if the drive is to be #2, install the jumper on DS2. DO NOT jumper pin A. This will cause the drive to be selected constantly.
   e. Seek Complete (SK COMP) between pin D and pin 1.
   f. Type 7438 terminator IC installed at location 6J of last drive.
6. Connect the signal and power cables to the rear of the drive as follows: (Refer to table 5-3.)
   a. For two drives, the "A" cable is daisy chained from the 210-8325 DA board to J1 of drive #2 and then to J1 of drive #1.
   b. For one drive, connect the end of the "A" cable to J1 of drive #1.
   c. There is a separate "B" cable from the DA to J2 of each drive.
7. Slide the drive back into the cabinet on its bayonet slide on the bottom of the drive.
8. Reinstall the 5/16 inch hex bolt and Pem nut.
9. Secure the actuator and the pulley on the defective drive.

Figure 5-27. Quantum Drive Spindle Lock

Figure 5-28. Quantum Drive Actuator Lock

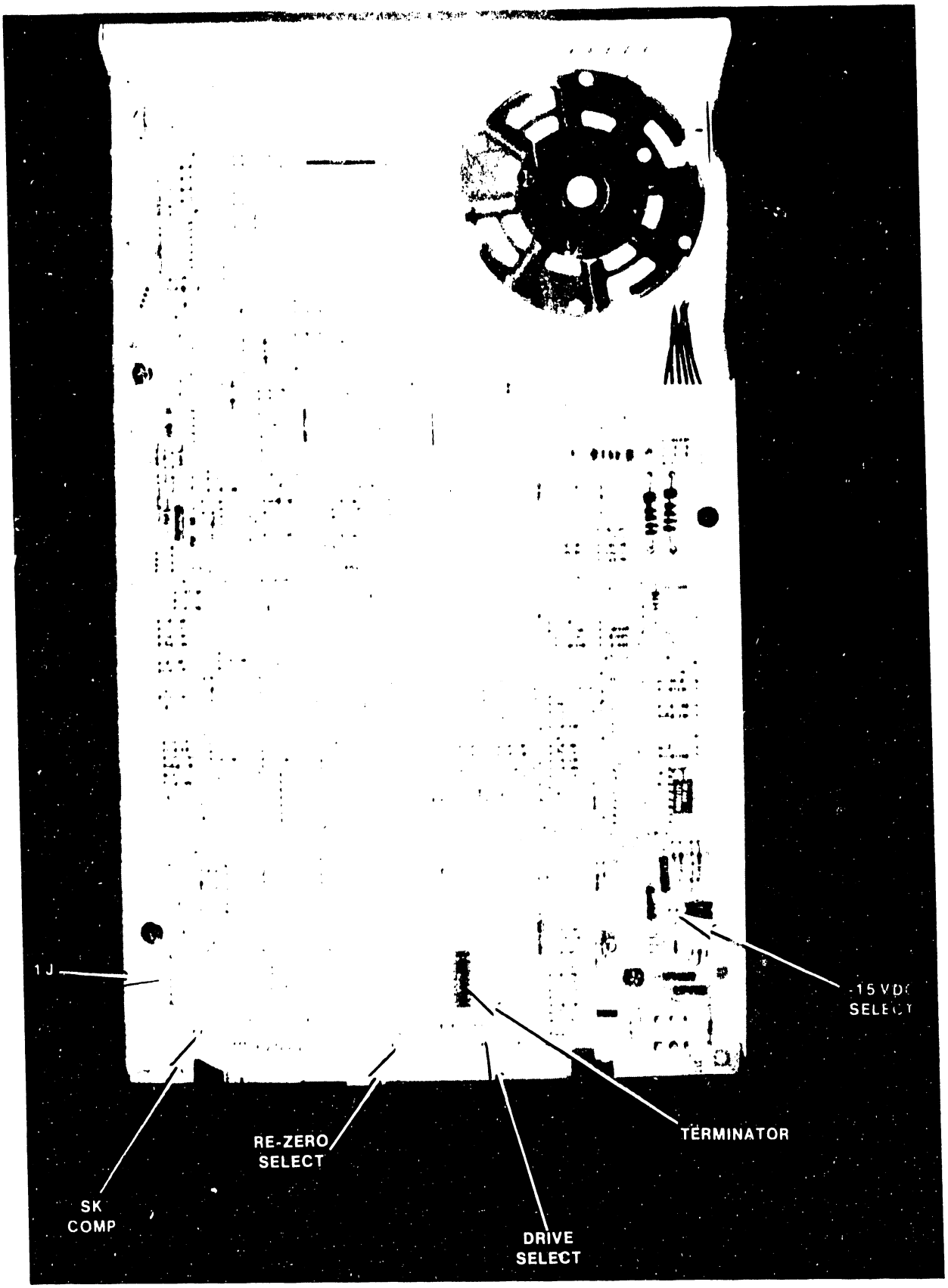


Figure 5-29. Quantum Drive Jumper Options

5.3.4.15 Diskette Drive Removal

The 278-4028 Diskette Drive in the VS-25/45 is bolted to the main frame cabinet shelf. Remove the diskette drive as follows:

1. Power down the main frame by depressing the ac power On/Off switch to the '0' position.
2. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
3. Remove the 50-pin signal connector from J1, the 3-pin ac connector from J4, and the 6-pin dc connector from J5 of the Diskette Drive.
4. Remove the hex bolt from the rear base and the 2 nuts from the front panel bracket of the drive. (Figure 5-30.)
5. Slide the drive to the rear of the main frame, lift it from the rear slot, and up and out of the main frame.

5.3.4.16 Diskette Drive Replacement

1. To reinstall the Diskette Drive, reverse the above procedure.

NOTE

If the replacement drive is not WLI P/N 278-4028, check TAC Newsletter #30208, Category III.A.11 (3101) for the correct jumper configurations.

2. Make sure the 50-pin signal connector is orientated correctly on J1.

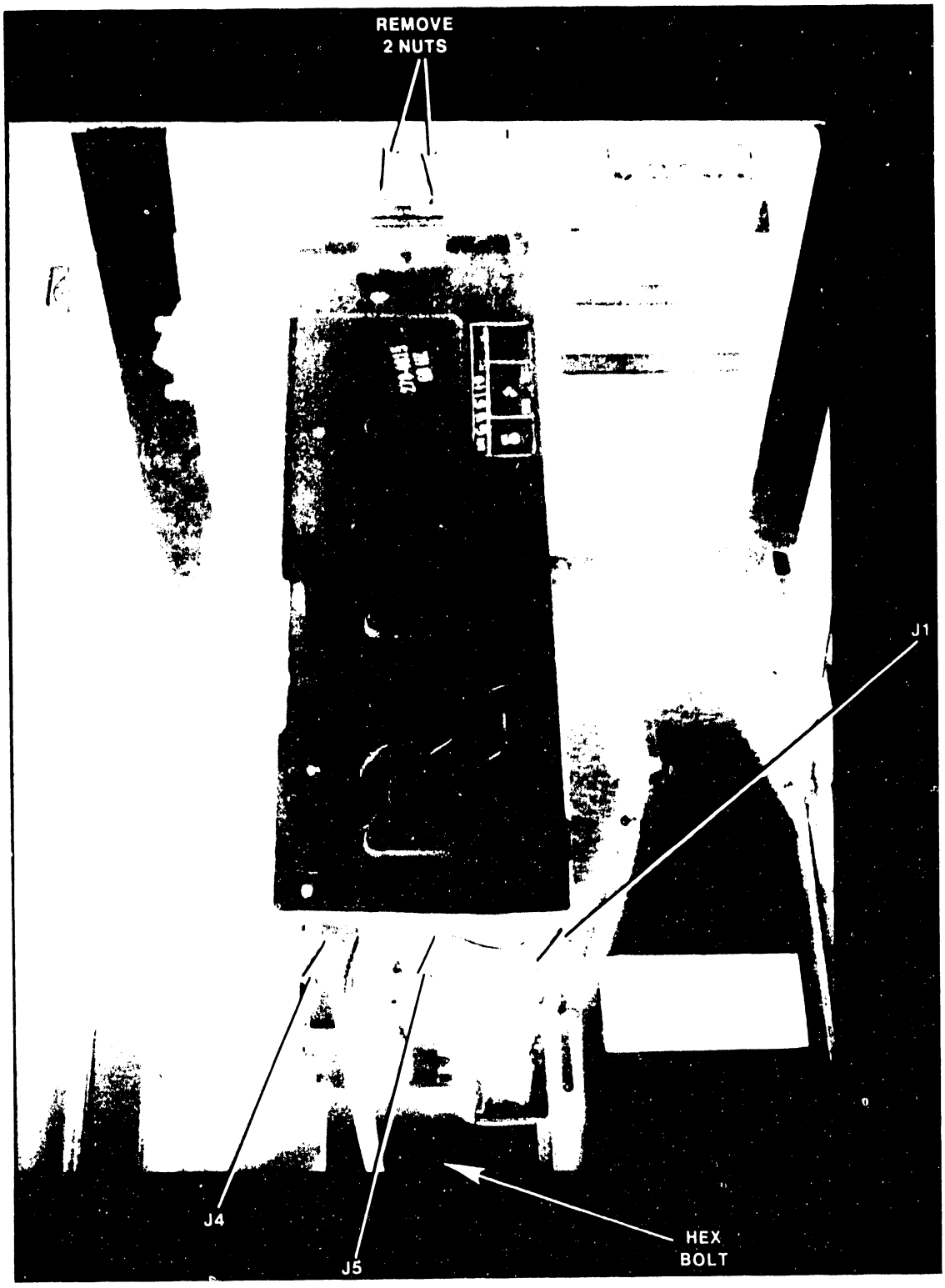


Figure 5-30. Diskette Drive

5.3.4.17 Fan Removal

The three cooling fans used in the VS-25/45 main frame cabinet are mounted vertically on the back panel of the main frame. Before an individual fan can be removed, the board cage must be moved and the entire fan panel assembly must be removed. Remove a damaged or defective muffin fan as follows:

1. Power down the main frame by depressing the ac power On/Off switch to the '0' position and unplug the power connector from the power source receptacle.
2. Remove the top and front covers (paragraphs 5.3.4.1 and 5.3.4.2).
3. Mark and disconnect any circuit board cables that may interfere with removal of the fan panel assembly. Do not remove any circuit boards.
4. Remove the two 5/16 inch Whiz Lock screws that secure the front of the board cage assembly to the frame. (Figure 5-23.)
5. Disconnect the 9-pin connector from J28, the 6-pin twisted pair connector from J29, and the +5 Volts and +/-0 Volts #6 cables as instructed in paragraph 5.3.4.9.
6. Pull the entire board cage assembly forward about 6-8 inches.
7. Disconnect the brown 6-pin fan panel assembly power connector located to the rear of the Diskette Drive.
8. Remove the 6 hex bolts holding the fan panel assembly to the back panel. (Figure 5-31.)
9. Remove the fan panel assembly from the inside of the main frame.
10. To remove either of the top two fans, remove the 8 Phillips screws holding the fan baffle (figure 5-32) to the fans. It is not necessary to remove the baffle to remove the bottom fan.
11. Disconnect the plug on the lower left of the fan(s) to be removed.
12. Remove the 4 screws and nuts holding the fan to the fan panel assembly, and remove the fan.

5.3.4.18 Fan Replacement

1. To install a fan, reverse the above procedure.
2. Reconnect all cables. (Refer to table 5-3.)

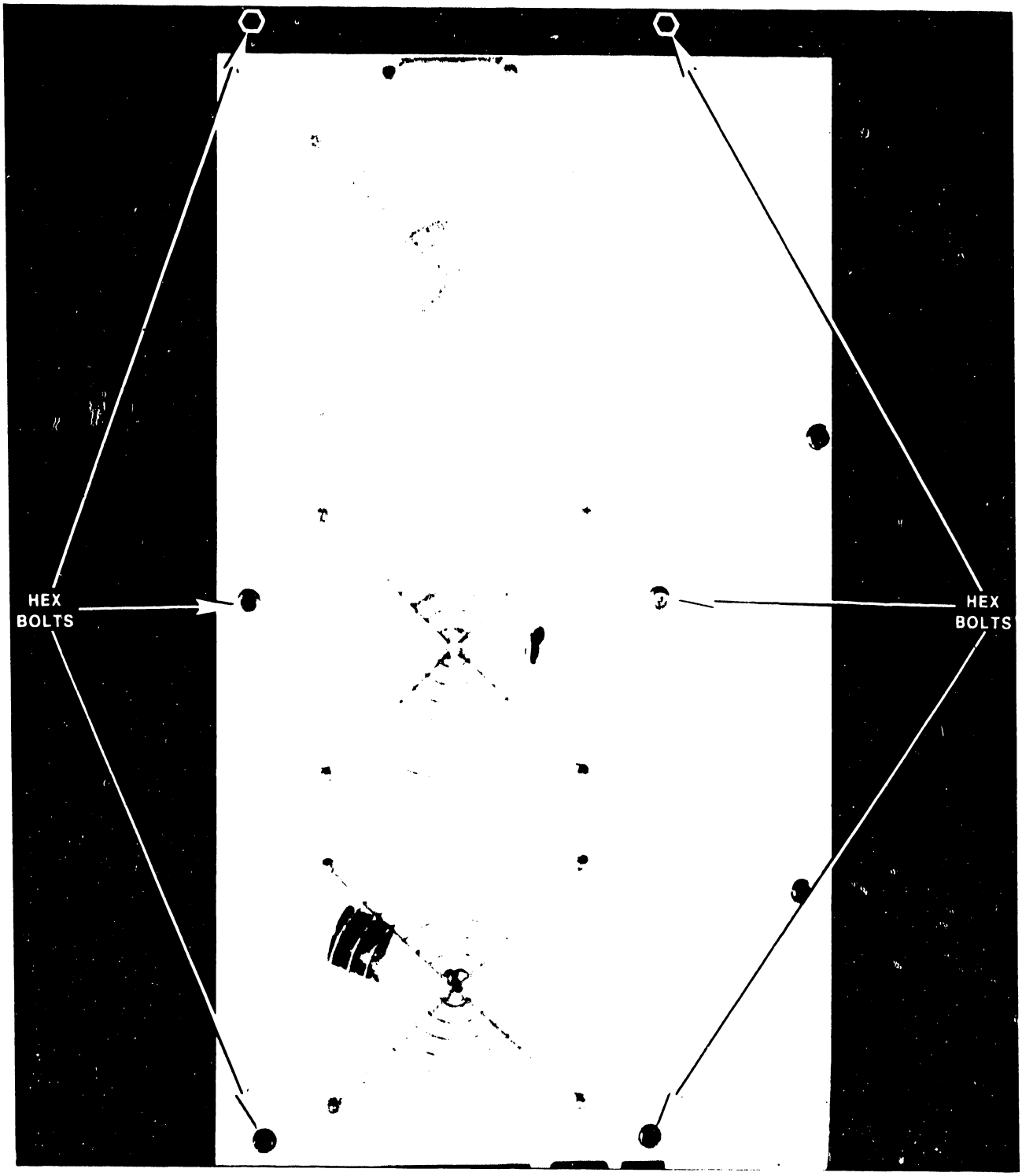


Figure 5-31. Fan Panel Assembly

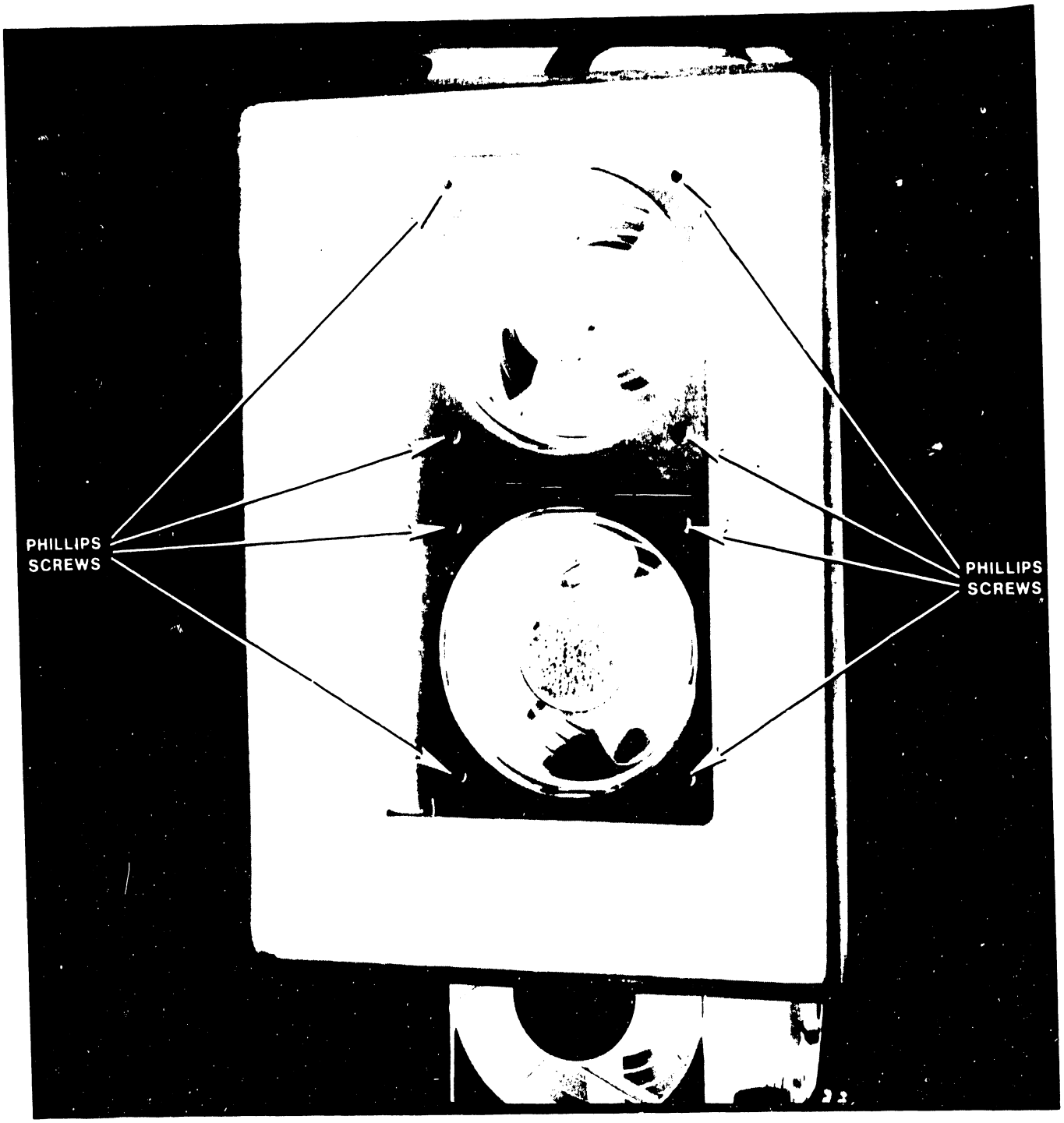


Figure 5-32. Fan Baffle

CHAPTER 6 SCHE-MATICS

CHAPTER 6

SCHEMATICS

Schematics are not provided as part of this Standard Manual. The schematics appear in the VS-25/45 Computer System Schematics Manual, WLI P/N 729-1185-A.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

7.1 SCOPE

This chapter contains the illustrated parts breakdown for the VS-25/45 Computer System. Use this breakdown for part number identification when ordering field-replaceable components.

Table 7-1. Internal Signal Cable Part Numbers

FROM PC BOARD	(CONNECTOR)	TO PC BOARD	(CONNECTOR)	PART NUMBER
210-8304	J1	Rear Panel	Remote	220-3224
"	J2	210-7913	J1	220-3226
"	J3	Diskette Drive	J1	220-3225
210-7906	J2	Rear Panel	BNC/TNC	220-3080
"	J3	" "	" "	" "
"	J4	" "	" "	" "
"	J5	" "	" "	" "
210-8616	J3	Rear Panel	BNC/TNC	220-3080
"	J4	" "	" "	" "
"	J5	" "	" "	" "
"	J6	" "	" "	" "
210-8325	J1	Quantum Dr. #1	J2 (B cable)	220-3227
"	J2	Quantum Dr. #2	J2 (B cable)	220-3227
"	J3	Quantum Dr. #1&2	J1 (A cable)	220-3228
210-8312	J1	Rear Panel	"A"	220-3158
210-8313	J2	" "	"B"	220-3156
210-8314	J3	" "	"B"	220-3156
210-8315	J4	" "	"B"	220-3156
	J5	" "	"B"	220-3156
210-8337	J1	Rear Panel	TC Conn	220-3246
"	J13	" "	" "	N/A
"	J2	" "	" "	220-3224
"	J3	" "	" "	220-3224
"	J4	TC Front Panel	Display	220-3247
210-8637	J2A	Rear Panel	TC Conn	220-3224
"	J3A	" "	" "	220-3224
"	J13A	" "	" "	N/A
"	J2B	" "	" "	220-3224
"	J3B	" "	" "	220-3224
"	J13B	" "	" "	N/A
"	S1 & S2	TC Front Panel	Display	220-3102

Table 7-2. Internal Power Cable Part Numbers

FROM PC BOARD	(CONNECTOR)	TO PC BOARD	(CONNECTOR)	PART NUMBER
Rear Panel		Power Supply	AC Input	220-1867
210-8010 Switching P/S	J3, 4, 8, 9, 11, 12 (Note 1)	AC Receptacle Mount (Note 2)		220-1865
AC Receptacle Mount (Note 3)		Quantum Drives Diskette Drive Fan Cable Conn.	J4 J4	220-1869
Fan cable Connector		Fans		220-3273
210-8011 Switching P/S	J4, 5, &6 J7 J8	Quantum Drives Diskette Drive 210-7907 (Note 4) 210-7907	J5 J5 J28 J29	220-1864 220-1864 220-3272 220-3272
210-8012 Switching P/S	J13 J6 (+5V) J6 (0V)	210-7907 210-7907 210-7907	J28 J30 (+5V) J31 (0V)	220-3272 220-0293 220-0290

NOTES

1. J3, 4, 8, 9, 11, and 12 are parallel ac output jacks. Only one jack will be used.
2. Part number 220-1865 is a single cable from the power supply ac output connector (J3, etc.) to an ac receptacle mount located on the shelf at the rear of the main frame.
3. Part number 220-1869 is a multi-connector (breakout) cable from the ac receptacle mount to the Quantum drive(s), the diskette drive, and the fan cable connector.
4. Part number 220-3272 is a milti-connector wiring harness.

Table 7-3. RAM Replacement Chips

BOARD	DESCRIPTION	WLI P/N	VENDOR	VENDOR P/N
210-8303	CPU C.M.	377-0413	HITACHI	HM6147-3
210-7900	MAIN MEMORY	377-0415-X	SEE SERIES I/D	

SERIES I/D	VENDOR	VENDOR P/N	WLI P/N
377-0415-X	TEXAS INST.	TMS4164C-2	377-0415
377-0415-X	FUJISTU	MB8264-20	726-8101-F
377-0415-X	HITACHI	HM48641P-3	726-8101-H
377-0415-X	INTEL	D2164-20	726-8101-I
377-0415-X	MOTOROLA	MCM6665AL-20	726-8101-M
377-0415-X	MOSTEX	MK4560/P-15	726-8101-MX
377-0415-X	NEC	UPD4164C-2	726-8101-N

VS25/45 CABINET ASSEMBLY (ASSEMBLY PART NO. 279-4146-TW)

ITEM NO.	PART NO.	DESCRIPTION
1	458-3096	SIDE PANEL R.H.
2	279-0523-TW	FRONT PANEL ASSEMBLY
3	660-0817	DUST FILTER
4	458-1095	FRONT PANEL, (WELDMENT)
5	600-0809	ATTENUATOR, SOUND FRONT PANEL
6	458-3093	MIDDLE SHELF
7	660-1044	ATTENUATOR, SOUND 14"x5"
8	660-1045	ATTENUATOR, SOUND 18"x6" W/HOLE
9	660-1043	ATTENUATOR, SOUND 18"x5"
10	650-6201	10-32x5/8 FLANGE WHIZ LOCK
11	449-0229	LATCH PAD
12	278-4025	QUANTUM DISK DRIVE
13	270-0735	SWITCHING POWER SUPPLY
14	458-3022	POWER SUPPLY CARRIER
15	655-0032	LEVELING GUIDE
16	655-0915	BLACK CASTER
17	458-3095	SIDE PANEL L.H.
18	660-7041	ATTENUATOR, SOUND 21"x7"
19	660-1042	ATTENUATOR, SOUND 21"x5"
20	458-2059	STOP, TOP COVER
21	650-4160	8-32x1/2 PAN HD PHIL
22	650-0029	8-32 LOCKNUT KEPS
23	651-0273	RECP SNAP-ON #4
24	651-0224	OVAL HD STUD DZUS
25	279-4090-TW	TOP COVER ASSEMBLY
26	458-3087	COVER, TOP (WELDMENT)
27	452-2709	CABINET STIFFNER
28	650-6122	10-32x3/8 FLANGE WHIZ LOCK

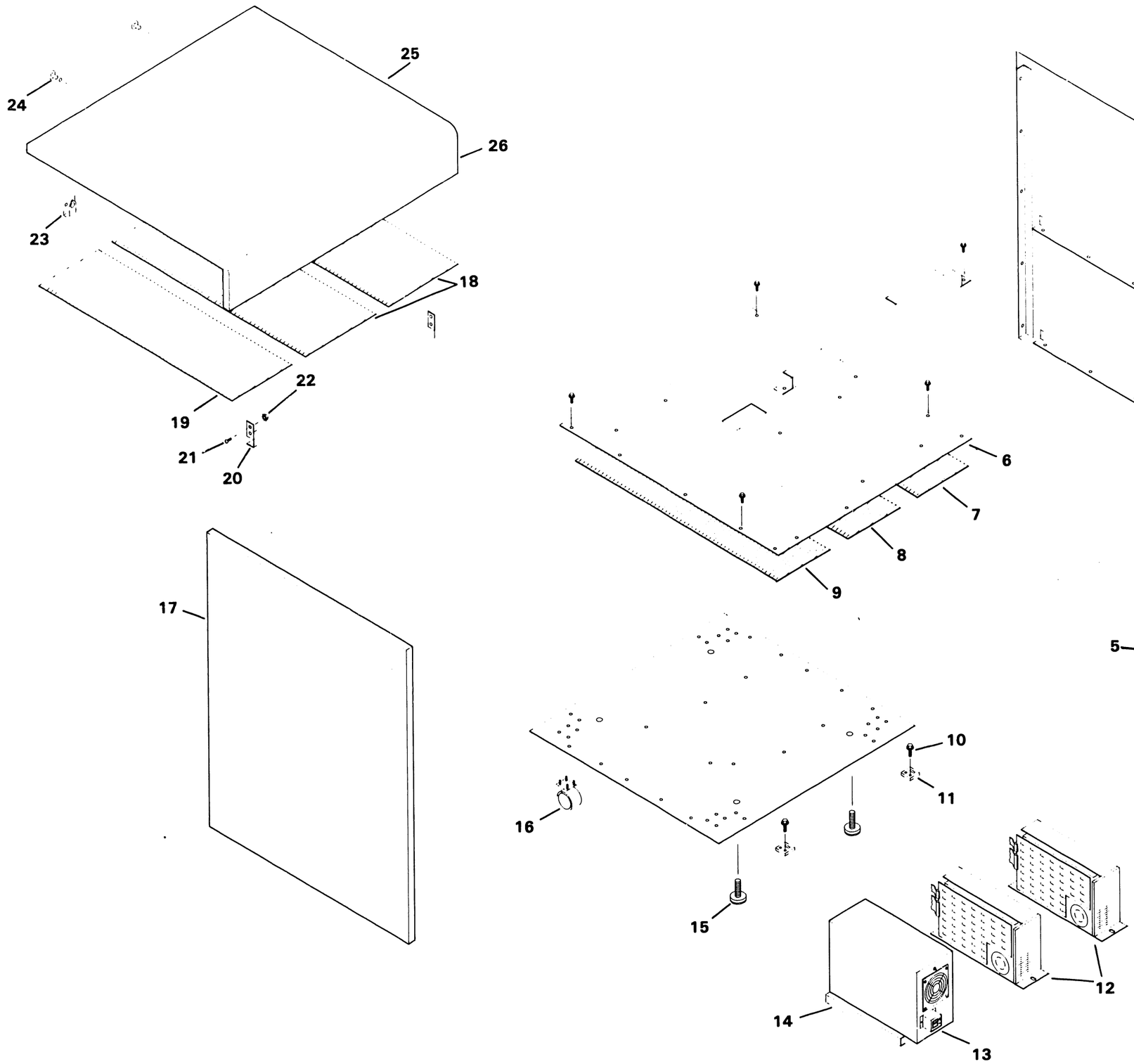


FIGURE 1 VS25/45 CABINET ASSEMBLY (ASSEMBLY PART NO. 279-4146-TW)

VS25/45 FRONT PANEL ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
1	210-7913	FRONT PANEL BOARD
2	220-7913	LOCAL/REMOTE KEY SWITCH
3	452-2248	DEAD FRONT PANEL
4	PART OF 2	
5	PART OF 7	
6	615-1970	BLANK PANEL
7	270-0814	T.C. FRONT PANEL
8	PART OF 7	
9	PART OF 7	
10	PART OF 7	
11	278-4028	DISKETTE DRIVE

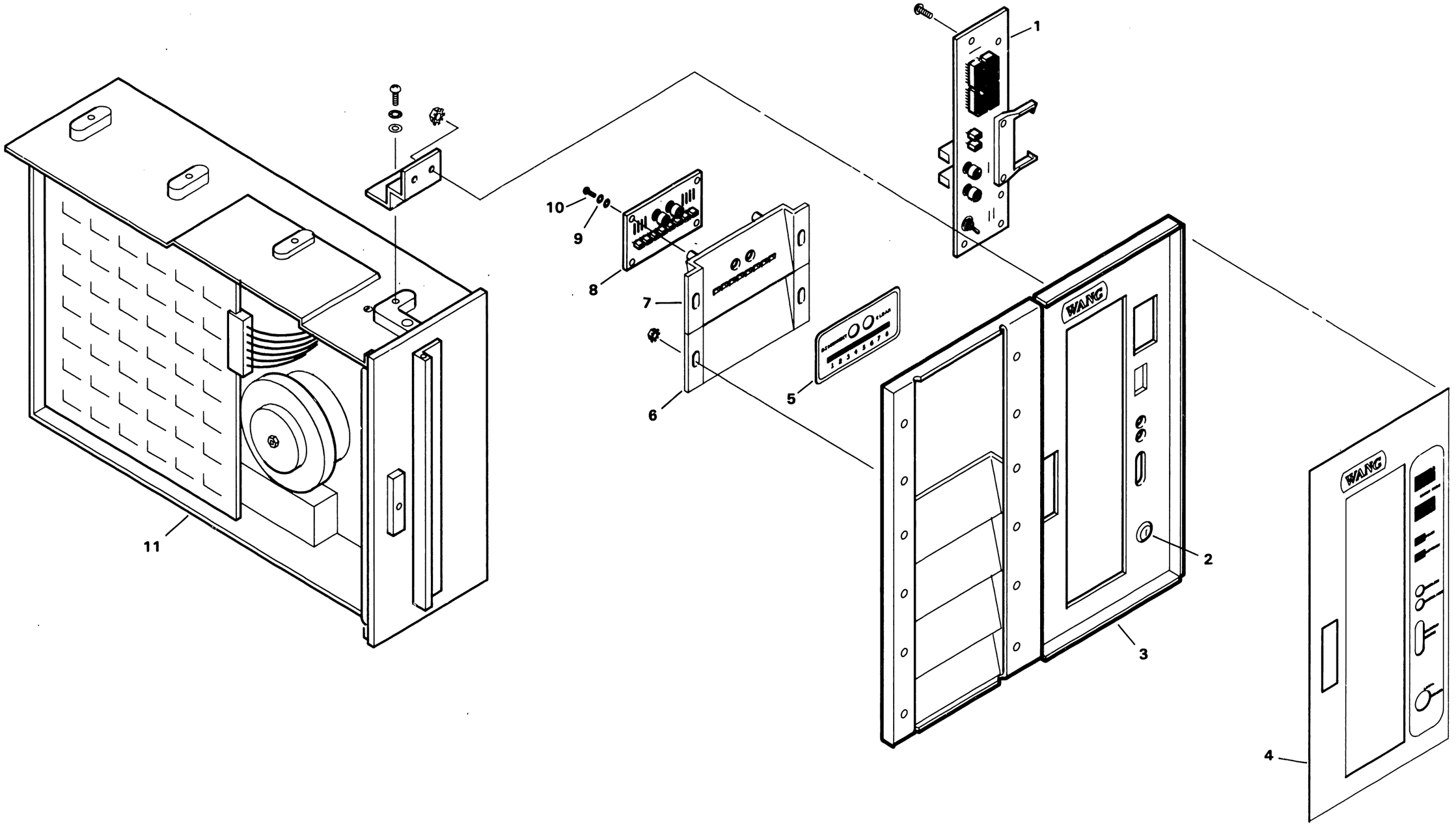


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FIGURE 2 VS25/45 FRONT PANEL ASSEMBLY (NO ASSEMBLY PART NO.)

VS25/45 REAR PANEL ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
1	655-0055	RED CAP
2	652-6002	10-32 LOCKNUT KEPS
3	270-0728	FAN PANEL
4	220-3224	REMOTE DIAGNOSTIC T.C. CABLE
5	400-1003	FAN, 100 CFM
5	400-1013	FAN, 70 CFM
6	650-6201	10-32x5/8 FLANGE WHIZ LOCK
7	220-1867	POWER CORD & FILTER ASSEMBLY
8	270-0704	BNC/TNC CONNECTOR PANEL
9	458-0954	"A" CABLE CLAMP
10	458-1021	"B" CABLE CLAMP
11	650-6124	10-32x3/8 PARKERIZED SCREW
12	452-2391	PLATE, BLANK
13	452-2394	PLATE, BLANK FULL
14	458-3092	REAR PANEL
15	452-4135	CABLE GUIDE

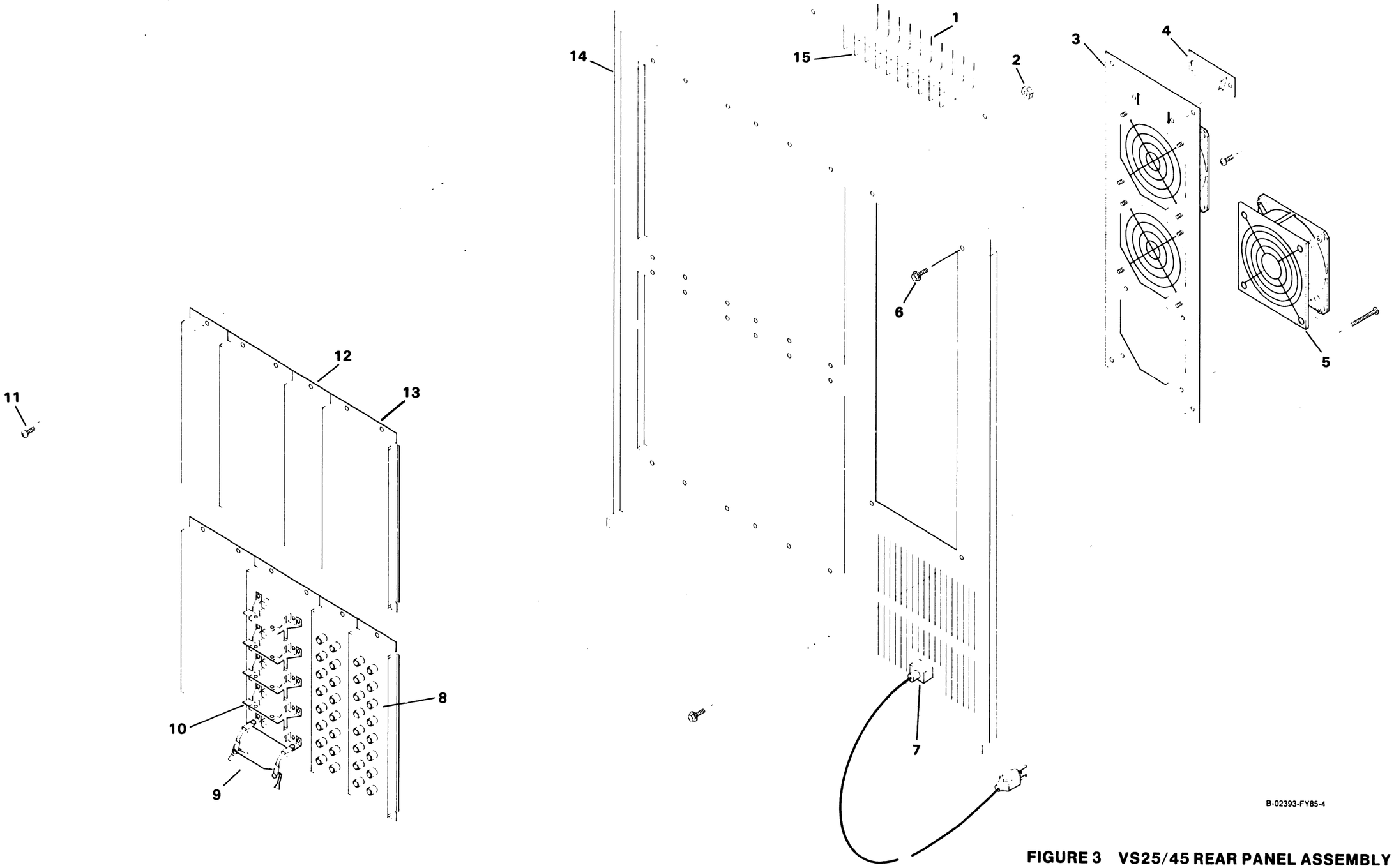

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FIGURE 3 VS25/45 REAR PANEL ASSEMBLY (NO ASSEMBLY PART NO.)

VS 25/45 MOTHERBOARD & CARD CAGE ASSEMBLY (NO ASSEMBLY PART NO.)

ITEM NO.	PART NO.	DESCRIPTION
1	279-0522	CARD CAGE ASSEMBLY
2	220-0293	±0 VOLT CABLE
3	220-0290	+5 VOLT CABLE
4	270-3272	POWER SUPPLY TO MOTHERBOARD HARNESS
5	PART OF 1	
6	PART OF 1	
7	PART OF 1	
8	PART OF 1	
9	210-7907	MOTHERBOARD
10	PART OF 1	
*11	210-7900	MAIN MEMORY BOARD
12	210-8303	CPU BOARD
13	210-8304-1A	BUS PROCESSOR BOARD
14	210-7906-A	SERIAL I/O ADAPTER
15	210-8325-A	QUANTUM DISK DEVICE ADAPTER
16	PART OF 1	
17	PART OF 1	
18	654-0200	LUGS
	**210-8316	ISIO ADAPTER
	210-8337-A	1 PORT TC/DA
	210-8637	2 PORT TC/DA
VS 45		
	210-8312-A	SMD/DA 1 PORT
	210-8313-A	SMD/DA 2 PORTS
	210-8314-A	SMD/DA 3 PORTS
	210-8315-A	SMD/DA 4 PORTS
	*210-7900-1	256KB
	*210-7900-2	384KB
	*210-7900-3	512KB
	*210-7900-4	768KB
	*210-7900-5	1024KB

** 210-8316 REPLACED BY A 210-8616A

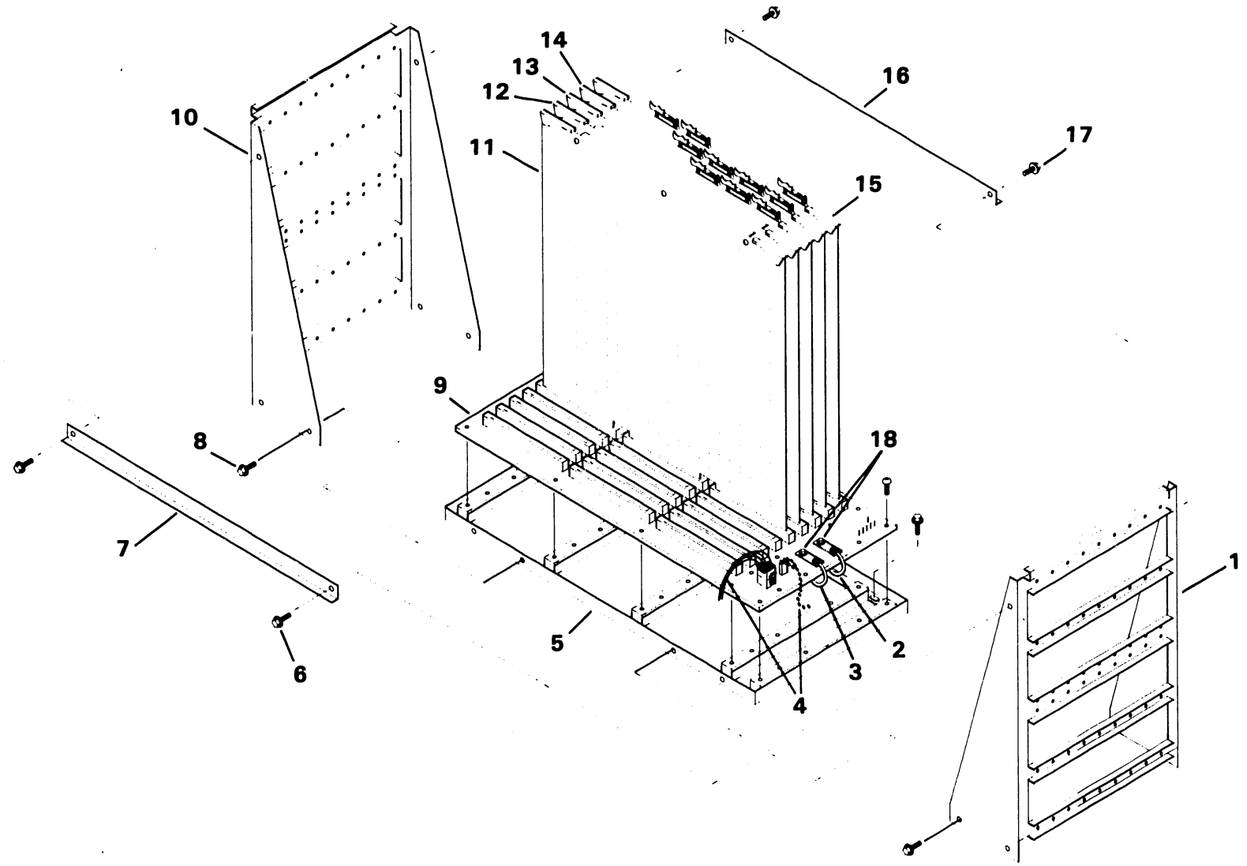

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FIGURE 4 VS25/45 MOTHERBOARD & CARD CAGE ASSEMBLY (NO ASSEMBLY PART NO.)

CHAPTER 8 TROUBLE-SHOOTING

CHAPTER 8

TROUBLESHOOTING

8.1 GENERAL

This chapter describes the available on-line and off-line diagnostic test programs and gives guidelines for their use. Also provides guidelines for isolating fault locations to field-replaceable or repairable components.

8.2 VS-25/45 DIAGNOSTIC FACILITIES

Two types of diagnostics are available to the VS-25 and VS-45: inner-level microcode diagnostics and outer-level memory and peripheral diagnostics. With these diagnostics the CE is able to locate and repair most of the problems that occur in the system. All available diagnostics must be run, prior to turnover to the customer, as a check for system integrity.

The VS-25/45 system will use the existing diagnostic and error reporting facilities already available on the VS-80 and VS-100. This includes the basic set of test programs and Stand-Alone diagnostic programs, updated as necessary for the VS-25/45. At the Operating System (OS) Release 5.03 level, the standard on-line diagnostics and error log features are present. A more powerful error log display program is also under development.

The VS-25/45 system architecture can be thoroughly tested using an integrated set of off-line hardware diagnostics running on the 8086 microprocessor controlled Bus Processor (BP). These off-line diagnostic programs provide a sophisticated, yet user-friendly, interface to any level of user. The programs are easily accessible through the power-up procedure.

The programs provide a comprehensive test of system hardware functionality in a building block manner. The programs provide error isolation options so that the user can pursue error situations down to the desired level of detail. The packaging of the programs on the standard bootstrap disk provides for easy access and usage.

Also available now is home office Remote Diagnostic Support. This feature is described in paragraph 8.3.

All VS-25/45 systems have 2K byte Nonvolatile Random Access Memory (NVRAM). The NVRAM contains customer information, system configuration, hardware configuration, and service log information for the remote diagnostic facilities. Refer to paragraph 8.4.

8.3 REMOTE DIAGNOSTIC SUPPORT

As part of its remote maintenance objectives, Customer Engineering offers remote diagnostic service as a maintenance program to VS-25/45 customers. The primary goal of the service is to isolate problems remotely so that the CE can bring the correct parts and supply the customer with a responsive and efficient level of service.

The VS-25/45 hardware supports several features related to remote diagnostic service. These include a basic TC capability on the BP board. The 8086 microprocessor code necessary to establish a link with the Remote Maintenance Center resides in the BP-PROM.

There are two basic remote diagnostic service features supported. One feature involves the NVRAM (paragraph 8.4) on the BP board. The NVRAM will be maintained by various application programs, operating system hooks and microcode support so that it contains:

1. Customer information section
2. System configuration section
3. Hardware configuration section
4. Service log section

The NVRAM is the first block of data transmitted from the VS-25/45 during a remote diagnostic session.

The second feature involves the capability to run all the BP Off-line Diagnostics remotely. Locally resident diagnostic packages, already loaded on the system, can be run from the Remote Maintenance Center. (Refer to paragraphs 3.2.7. and 8.3.2).

8.3.1 REMOTE DIAGNOSTIC CERTIFICATION PROCEDURES

Before any remote diagnostic service sessions can be run, the remote maintenance data link between the VS-25/45 site and the home office Technical Assistance Center (TAC) must be verified. The procedure requires that the CE make an on-site call and work directly with the TAC to establish that the data link is working. It is the responsibility of the on-site CE to troubleshoot and resolve any telecommunications related problem.

Once the data link has been certified, it should not be necessary for the CE to return to the site to participate in the remote diagnostic sessions. The customer will normally be responsible for initiating and coordinating the remote diagnostic session with the TAC.

The following flow charts (figure 8-1) describe the remote diagnostic certification procedures, while figure 8-2 shows the modem and telephone line connections and the modem switch settings.

For more information on the WA3451 Wang Modem, refer to Customer Engineering Documentation Class 7401 and the WA3451 Asychronous/Synchronous Modem User Manual, WLI P/N 700-6975. Also, refer to the following TAC Newsletters:

#30830 - "Initialize Nonvolatile RAM"
#30830 - "Remote Maintenance Implementation"
#30920 - "VS-25/45 Remote Maintenance Information"
#30927 - "Nonvolatile RAM"

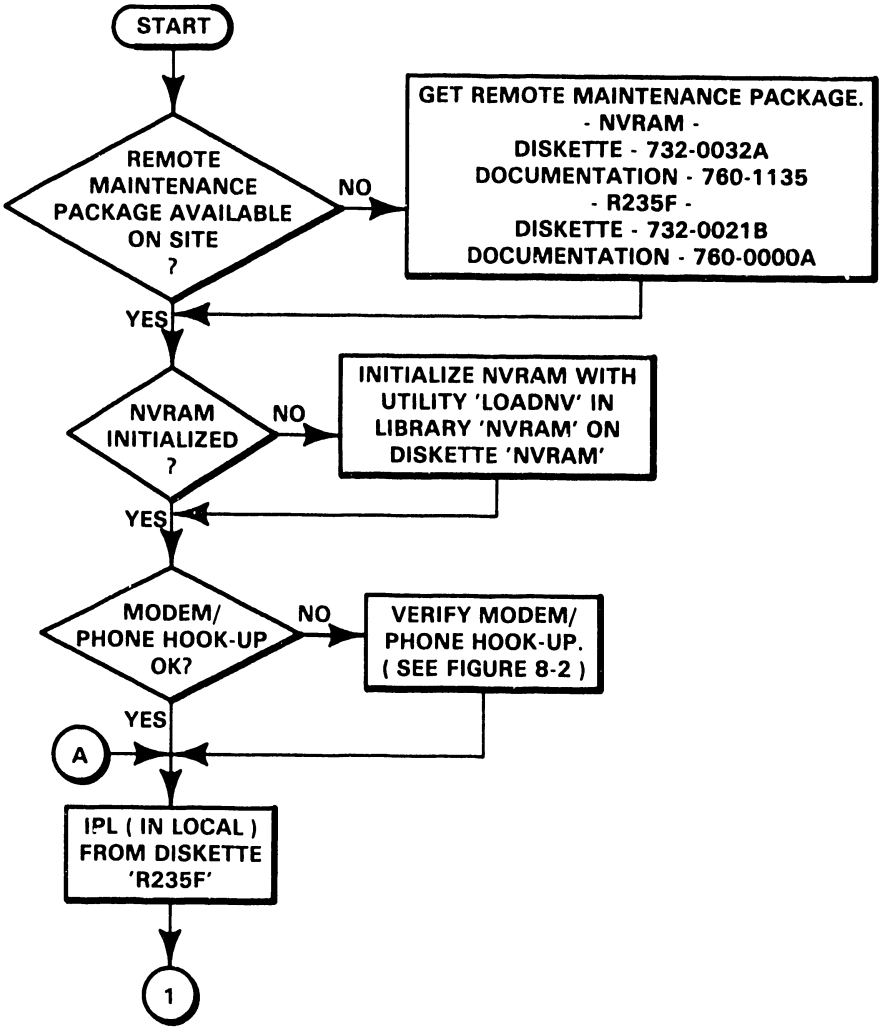


Figure 8-1. Remote Diagnostic Certification Flowchart (1 of 4)

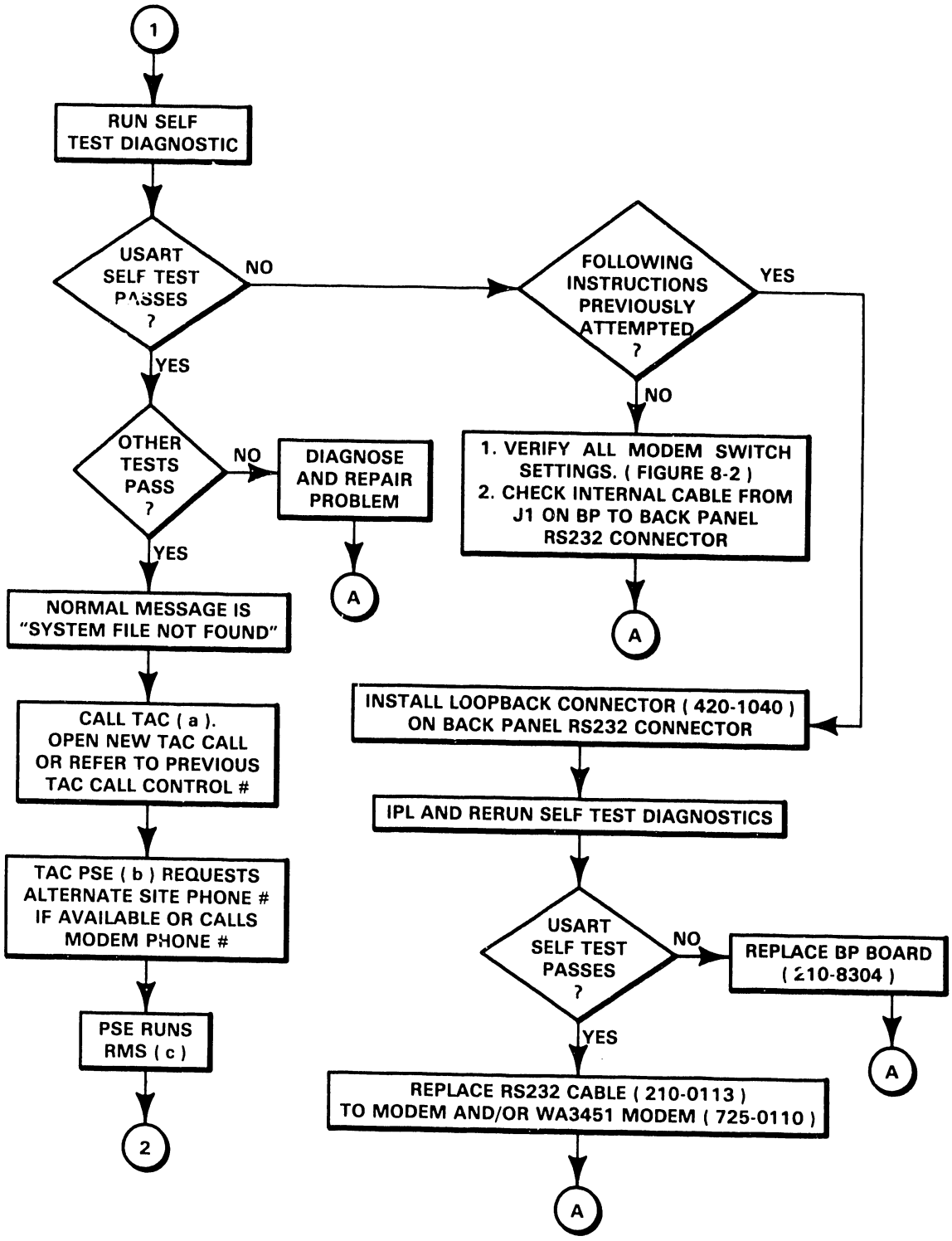


Figure 8-1. Remote Diagnostic Certification Flowchart (2 of 4)

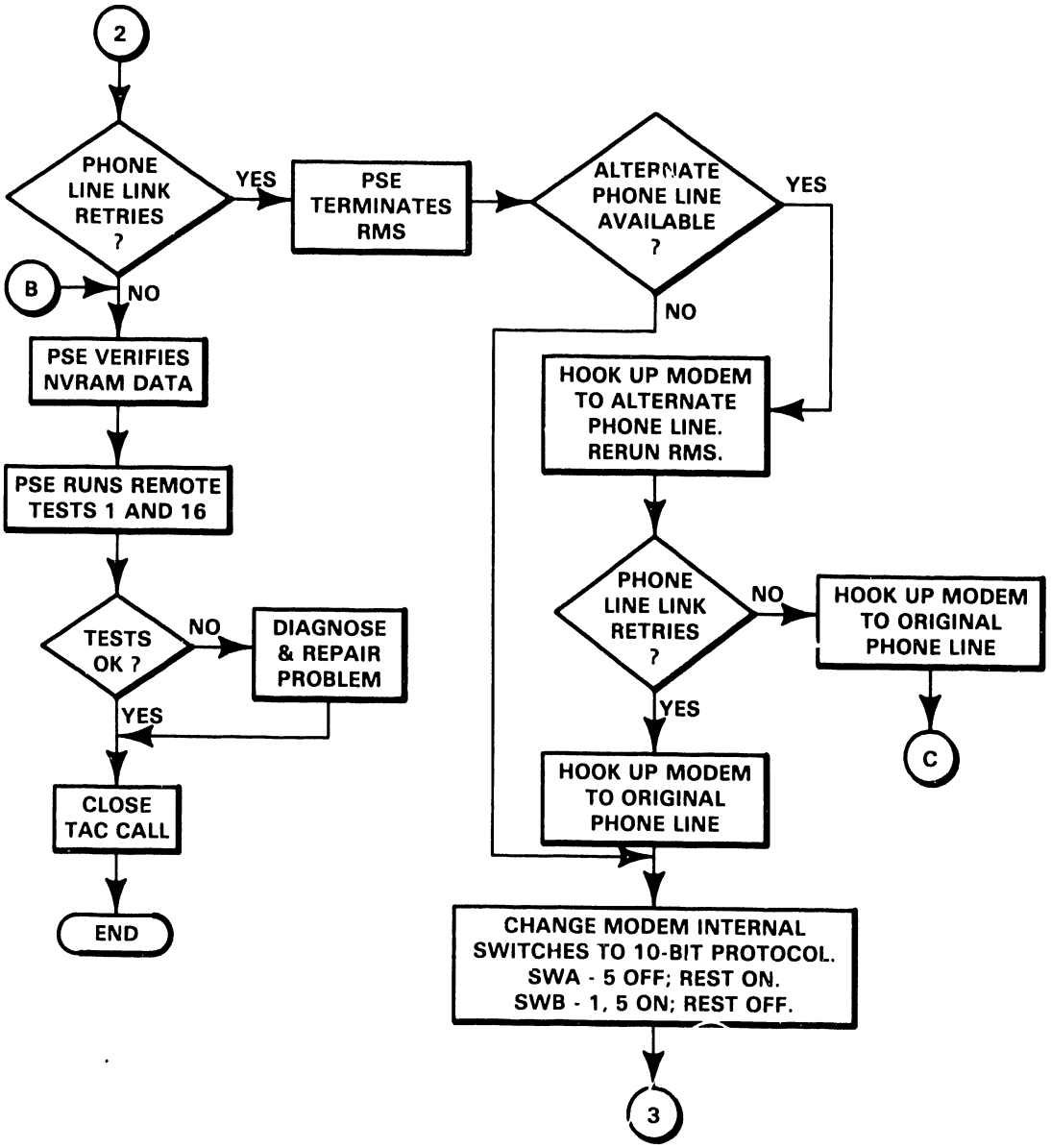


Figure 8-1. Remote Diagnostic Certification Flowchart (3 of 4)

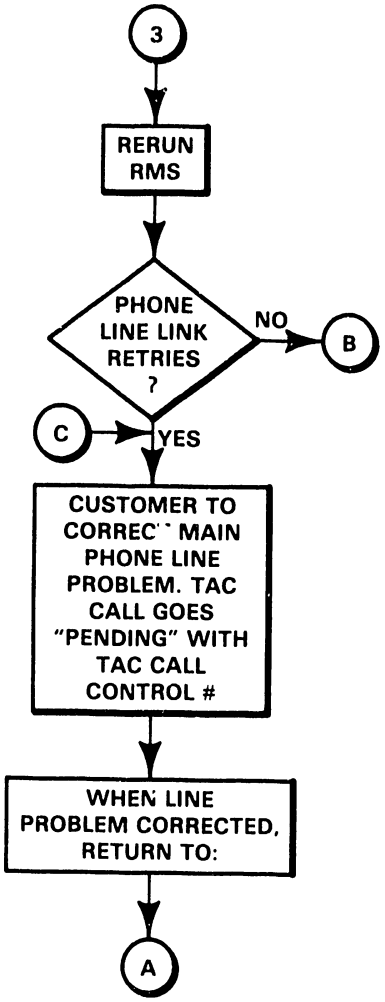
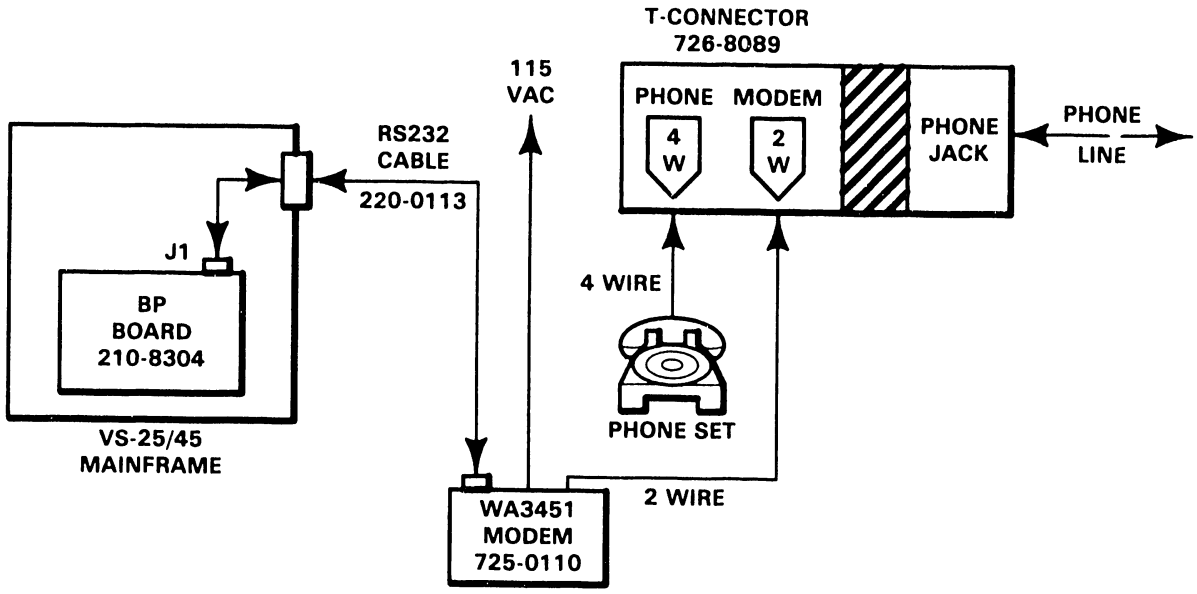
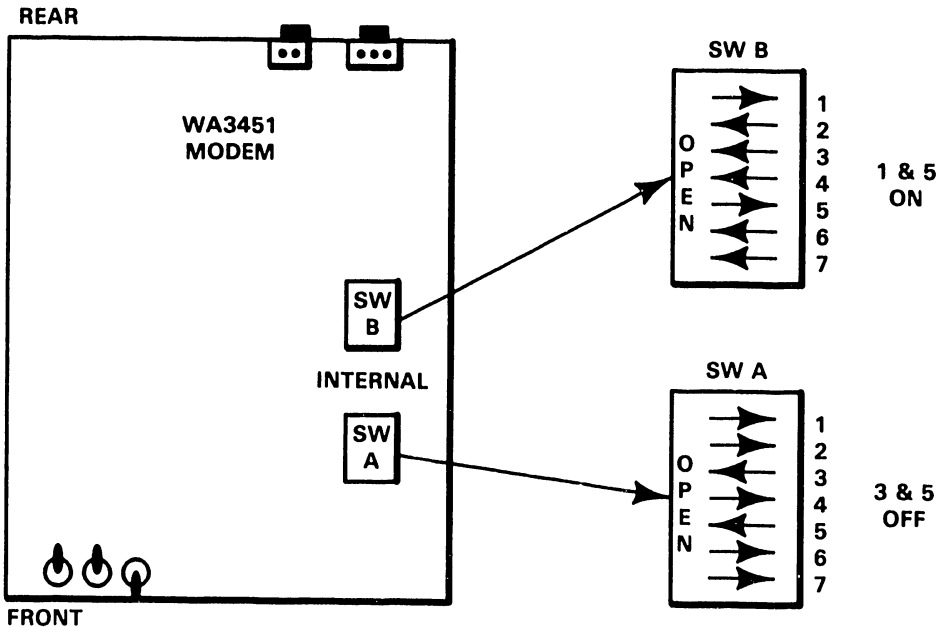


Figure 8-1. Remote Diagnostic Certification Flowchart (4 of 4)



MODEM/PHONE LINE HOOK-UP



MODEM SWITCHES

SW A & SW B NORMAL SETTINGS

Figure 8-2. Modem/Phone Connections and Modem Switches

8.3.2 REMOTE DIAGNOSTIC PROCEDURES

It is normally the customer who initiates the remote diagnostic session and coordinates with the Remote Maintenance Center (RMC) during the testing. Except at time of system installation, it isn't necessary for the CE to be present at the site during the remote diagnostic session.

The basic remote diagnostic procedure is as follows:

1. Suspecting a CPU problem, the customer notifies the Area Call Control Center (CCC).
2. The CCC then calls the home office Technical Assistance Center (TAC).
3. The TAC Remote Maintenance Center (RMC) establishes a telephone line data link between the RMC diagnostic system and the customer's VS-25/45.
4. The RMC reads and analyzes the information from the VS-25/45's Nonvolatile Random Access Memory (NVRAM).
5. The RMC runs the diagnostics from the diagnostic diskette inserted in the diskette drive of the customer's system.
6. The RMC notifies the Area CCC of the test results and which Field Replaceable Unit, if any, failed.
7. The CCC notifies the local Customer Engineer who completes the service call, including updating the NVRAM.

8.4 NONVOLATILE RAM (NVRAM)

All VS-25/45 systems have a special 2K byte x 8-bit memory area called a Nonvolatile Random Access Memory (NVRAM). The NVRAM is physically located on the Bus Processor (BP) board and is logically located within the BP's memory addressing space.

The primary purpose of the NVRAM is to provide a snapshot of customer information, system configuration, hardware configuration, and service log information for the remote diagnostic facilities. At the beginning of a remote diagnostic session, all the contents of the NVRAM, plus the power up error codes, will be transmitted to the Remote Maintenance Center. This snapshot will aid the Center in diagnosing the customer's problem.

The NVRAM can be written and read on-site by two utility programs; LOADNV and SHOWNV. The NVRAM initially contains no information until data is entered using the LOADNV utility. From that point on, the contents of the NVRAM can be displayed and updated during each service call.

A small battery, also located on the BP, provides back-up power to make sure that the NVRAM retains its data when the system is normally powered off, or in case of power outages.

8.4.1 NVRAM UTILITIES

For a complete description of the NVRAM Utilities refer to Documentation Release 9350, WLI P/N 760-1135.

Two applications programs, LOADNV and SHOWNV, are used to manage the NVRAM. These programs run under the VS Operating System and support features which include displaying, modifying, and printing any of the defined NVRAM fields. The LOADNV program also supports backup/restore functions between the physical NVRAM and a disk file. The NVRAM may be viewed using either the LOADNV or the SHOWNV programs, but may be modified only with the LOADNV program.

The LOADNV and SHOWNV programs display and/or print a formatted view of the NVRAM. This formatted view currently consists of four sections. The following is an overview of the contents of each section:

1. Customer Information Section - this section, loaded at installation time, includes customer identification, service location, system serial number, and information regarding the type of customer service contract.

2. System Configuration Section - includes operating system version and CPU and BP microcode versions. It also contains a system-wide ECO map and a system maintenance count. This, along with the Customer Information Section, covers all system-level information.

3. Hardware Configuration Section - is segmented by device Adapter (DA) with each DA's devices being tracked by their Physical Device Addresses. Serial number, ECO-level, and error counts (maintained dynamically by the CPU and BP microcode) are stored separately for each device. The CE can view and alter devices as a group (eg: all serial devices) or individually.

4. Service Log Section - contains one entry per service call. An entry includes call report number, and repair and subunit codes. A maximum of 12 entries can be stored, after which the oldest entry is discarded.

8.4.1.1 LOADNV Utility

The LOADNV program provides flexible read and optional modify control to all NVRAM sections. The program supports loading the NVRAM at installation time, creating backup disk files of the NVRAM data, and entering service call report information.

After running LOADNV, a check can be made of hard copy output to verify the changes. If any errors are detected, the program can be rerun recalling the output just created and only the particular field(s) within a section which need correcting can be selected. The field(s) can be easily modified and the updated data replaced.

The program also allows a prototype disk file to be created. This file can be initialized for a general VS-25/45 I/O device configuration. The prototype file can then be used as a standard starting point file for on-site running of LOADNV at system installation time.

The operation of the LOADNV utility is divided into three distinct processes:

1. Selection of input data

The initial screen of the LOADNV program is used to define the input data to be used by the utility. One of the three input options may be selected. The three input options and their most common uses are:

a. Disk file input - provides the LOADNV utility with a preformatted NVRAM image file from a disk, at which time further updates may be made.

b. Default input - used when creating an NVRAM image from scratch, such as for a new VS-25/45 system installation.

c. Direct NVRAM input - uses the actual data in the NVRAM as input for the utility. It would be most commonly used to update the service log section.

2. Processing and modification of the selected input data

a. Section selection menu - once the input data is defined by selecting one of the three input options, the LOADNV program then allows this data to be processed or modified. Data is accessed by logical NVRAM section name (customer information section, system configuration section, hardware configuration section, and service log section). As many sections as may be required can be accessed and modified. All modifications are made to the input data and held within the LOADNV program. The final disposition of the updated data is determined by the output options.

3. Selection of the destination of the processed or modified data.

After modifying the desired section(s), the LOADNV program displays the output options. One of three output options may be selected.

a. Create NVRAM image file - allows the NVRAM data to be written to a user-specified disk file. Useful for saving NVRAM data to be used later.

b. Load data into NVRAM - allows NVRAM data to be written directly into the physical NVRAM, destroying the previous contents. It would be most commonly used to update the service log section.

c. Load NVRAM and create NVRAM image file - Combines both of the previous options, also destroying the previous contents of the NVRAM.

After the output section is created, the LOADNV program performs the selected function and also creates a formatted NVRAM print file. The print file is created and placed in the system print queue on HOLD.

8.4.1.2 SHOWNV Utility

The SHOWNV program allows either examining the physical NVRAM without any possibility of accidentally modifying the current data, or examining an NVRAM image file. It will also generate hard copy printouts of either.

1. Selection of input data

The initial screen of the SHOWNV program is used to define the input data to be used by the utility. One of two input options may be selected, as follows;

a. Use an existing NVRAM image file - provides the SHOWNV utility with a preformatted or backup NVRAM image file from disk. Uses the 2K NVRAM disk image file as input to the utility.

b. Use NVRAM native - Allows current NVRAM data to be used as input by the utility. Commonly used to examine service call information. No data modifications may be made.

2. Processing Functions

Once the input data is defined, the SHOWNV program creates a formatted print file of the NVRAM or Image File data, whichever is selected as input. It then displays the print file via a link to the VS DISPLAY utility. Data is displayed in a format identical to the print format used by the LOADNV utility. All processing functions within the DISPLAY utility are available to manage the print file.

8.5 HEX DISPLAYS

The Front Panel (figure 3-2) monitors system error status and is used by the CE in conjunction with the microcode diagnostics for troubleshooting the VS-25/45 main frame. The front panel has four HEX displays arranged in two rows of two displays each. The panel provides information concerning the CP and BP status as well as the error condition of I/O devices in the IPL path (ie: Workstation 0 and the IPL disk drive selected by the Bootstrap Media switch).

When a fault is detected by the microcode diagnostics, the results are displayed as a HEX code which indicates which board or unit failed. (Refer to table 8-2 for the VS-25/45 Self-Test Monitor diagnostic error code breakdown of the top two Front Panel HEX digits, and Appendix B for the full list of 4-digit Self-Test Monitor diagnostic error codes.)

Once the CE has identified the failing board and recorded the error code, the board is sent to a Repair Depot. At the depot, repair personnel will run the same diagnostics the CE ran to verify the observations of the CE. This duplicating of trouble conditions results in fast turn-around time in the ultimate repair of the board.

8.6 MONITOR PACKAGES

An important diagnostic tool for testing the VS-25/45 CPU is a series of microcode diagnostics (bootstrap programs) executing from the BP to provide diagnostic services for the CP and BP. These diagnostics allow the CE to test all major CPU, BP, main memory, DMA, and disk and diskette drive functions.

Loaded from disk or diskette, the bootstrap program uses the Workstation 0 screen to allow the operator to select either IPL the System (Self-Test Monitor) or run Stand-Alone Diagnostic Monitor. (Note that the bootstrap programs cannot coexist with the operational CP and BP code; therefore, no system-level CP/BP functions, such as Control Mode, are available while the bootstrap programs are executing.)

8.6.1 SELF-TEST MONITOR

The Self-Test Monitor diagnostics are run, from library @DIAGST@, as part of the normal daily power-up procedures (paragraph 4.13.1) or at any time the system is IPLed (paragraph 4.11.1). The Bus Processor DIP switches (figure 5-6) must all be OFF.

Table 8-2 is a listing of the error code breakdown of the top two HEX digits of the front panel and will reflect the error code displayed on the workstation if any Self-Test Monitor (power-up) diagnostic fails.

Table 8-1. Self-Test Monitor Diagnostic Programs

TEST NO.	TEST ID	TEST NAME
1	ST0500	SIO
2	BT0500	BP USART Loopback
3	CT0500	CP Control Memory & CP/BP
4	CT0800	CP Random Operands
5	CT0B00	CP Integrity
6	MT0500	Main Memory Integrity
7	BT0800	BP DMA & MARS

8.6.1.1 Telecommunications DA Diagnostics

The TC DA PROM-based power-up diagnostics will run any time the system is powered-up or IPLed. The diagnostics will run at the same time as the BP power-up diagnostic and will complete successfully in about 12 seconds.

The LEDS on the 25V76-1/2 TC DA Front Indicator/Control Panel (table 3-4) only show that a failure occurred. The type of error is not defined. If an error occurred during the power-up diagnostics, run the Stand-Alone diagnostics as instructed in paragraph 8.6.2 to verify that an error did occurred. Ignore the TC DA LED display when running the Stand-Alone Diagnostic Monitor. Any errors will be displayed on the workstation screen and the VS-25/45 Front Panel HEX display. If the error is verified, replace the 25V76-1/2 TC DA.

Table 8-2. VS-25/45 Self-Test Monitor Diagnostic Error Codes
(Error code breakdown of the top two Front Panel HEX digits)

GENERAL	SPECIFIC	GENERAL ERROR NAME	SPECIFIC ERROR NAME
00		Bus Processor (PROM) and BP Operational Code	
10		Bus Processor	
20		Bus Processor	
30		Bus Processor	
40		Diagnostic Monitor	
	41		First Boot File
	42		Self-Test
	43		Self-Test
	44		System Loader
	45 to 49		Diagnostic Monitor & Files
	4A		Not Used
	4B		CPU Control Memory
	4C		CPU Self-Test
	4D		CPU Random Test
	4E		CPU Main Memory
	4F		BP DMA and MARs
50		Fixed Disk DA	
60		Fixed Disk DA	
70		Serial I/O DA *	
80		Diskette Dr. Controller	
90		Device Error	
	90		Workstation Zero
	92 to 94		Not Used
	95		Fixed Disk Device
	96 to 97		Not Used
	98		Diskette Device
	99 to 9A		Not Used
	9B		SMD Disk Device
	9C to 9F		Not Used
A0		Motherboard Signal	
	A0 to A3		Un-isolated
	A4 to A7		SIO Signal
	A8 to AB		Fixed Disk Signal
	AC to AF		SMD Disk Signal
B0		SMD Disk DA	
C0		Invalid Error Code	
D0		Invalid Error Code	

* - Workstation 0 must be powered-up and connected to the system.

NOTES

For the full list of 4-digit Self-Test Monitor diagnostic error codes, refer to:

1. Appendix B of this manual.
2. VS-25 Diagnostic Monitor Package documentation - WLI P/N 732-0018.
3. VS-25 Bulletin - WLI P/N 800-3108.

8.6.2 STAND-ALONE DIAGNOSTIC MONITOR

The Stand-Alone Diagnostic Monitor programs will run, from library @DIAGMN@, in the order that they are shown in table 8-3. If testing is not altered by operator action or by hardware failure, the Monitor automatically cycles on the set of diagnostic programs.

Table 8-3. Stand-Alone Diagnostic Monitor Programs

TEST NO.	TEST ID	TEST NAME
1	CT1000	CP Control Memory
2	CT2000	BP/CP Communication
3	CT3000	BU Branch Opcode
4	CT4000	Status, Conditional Branch
5	CT5000	Subroutine Stack Data
6	CT6000	Subroutine Stack Addressing
7	CT7000	Register, Immediate Opcodes
8	CT8000	CPU Stack Diagnostic
9	CT9000	Logical and Shift Opcodes
10	CTA000	8-Bit and 16-Bit ALU Test
11	CTB000	MAR, TRAM, and RCT Test
12	CTC000	BD, IAD, CC, and DSET Test
13	CTD000	BI Branch Opcode Test
14	CPTSTR	CPU Tester
15	MT1000	Main Memory Test
16	BT2000	DMA Test
17	BT3000	SA850 Floppy Disk Diagnostic
18	QT1000	Q2040 Quantum DA Diagnostic
19	DT1000	CMD/SMD Disk DA Diagnostic
20	BT1000	USART/Modem Diagnostic
21	BT5000	Bus Processor Diagnostic (NVRAM)
22	TT1000	Telecommunications DA 1-Port
23	TT2000	Telecommunications DA 2-Port
24	ST1000	Dumb 928 (SIO) Data Link DA Diag
25	ST2000	Smart 928 (ISIO) Data Link DA Diag
26	BT4000	VS25/45 Multitasker

8.6.2.1 Stand-Alone Diagnostic Monitor Screen Descriptors

```
                    VS 25/45 Diagnostic Monitor Package
   (1) = Error Loop       (4) = Program Loop   (7) = Step    (16) = Exit
   (2) = Routine Loop     (5) = Pause          (10) = Clear all Settings
   (3) = Stop on Error                         (13) = Display Error Log

Program Name : VS25/45 Main Memory Diagnostic-- Error Count        = 00000
Routine Name : 40 MM Integrity---------------   Routine Loop Count = 00000
Error Code   =                                  Program Loop Count = 00000
Program Status : Test In Progress               Monitor Pass Count = 00000

Messages:
```

Figure 8-3. Stand-Alone Diagnostic Monitor Screen

1. Program Name - the name of the program currently being performed
2. Routine Name - the name of the test routine currently being performed
3. Error Code - the code of the most recently detected error.
4. Program Status - the status of the diagnostic currently being performed (e.g. Test in Progress, Stop an Error, Program Pause, etc.)
5. Error Count - a count in decimal of the number of errors which have been detected. This count is cumulative and it is reset only by reIPLing or by returning to the Program Selection menu.
6. Routine Loop Count - identical to Program Loop Count except that this count applies to routines rather than to diagnostics.
7. Program Loop Count - a count in decimal of the number of loops which have been made through the diagnostic currently being performed. This value is only displayed when the loop-on-program option is in effect. It is cleared when the loop-on-program option is deselected.
8. Monitor Pass Count - a count in decimal of the number of loops which have been made through the set of diagnostics. It is cleared by reIPLing or returning to the Program Selection menu.

8.6.2.2 Error Messages and User Prompts

The routine currently being performed writes error messages and user prompts in the lower half of the screen. If more than one error occurs, only the last error message will be left on display, although the error count is updated for each error.

8.6.2.3 Running The Stand-Alone Diagnostic Monitor

1. Make sure the Local/Remote switch (figure 3-2) is in the Local position. (The system will not IPL if the switch is in Remote.)
2. Set the Bootstrap Media switch to the correct position (refer to paragraph 3.2.7).
3. Press the Initialize button on the front panel. (The HEX display on the front panel will begin counting down from FFFF.) In about 45 seconds W/S 0 will display the following Menu:

```
                VS Self Test Diagnostic Monitor
                      IPL Drive Selection
                   Bootstrap Volume = SYSTEM

  Device     Capacity     Type     Volume      Status
  2270V-4    1.2 Mb       Dsket
  Q2040       33 Mb       Fixed    SYSTEM      Media Tolerant

            Position Cursor to Indicate Device and Select:
 ================================================================
 (ENTER) IPL                      (8) STAND-ALONE DIAGNOSTIC MONITOR
```

Figure 8-4. IPL Drive Selection

4. Position the cursor next to the system volume and press PF8, Stand-Alone Diagnostic Monitor.
5. Workstation 0 will display a cautionary notice and request a YES or EXIT response. Enter the correct response.
6. If YES is entered, Workstation 0 will display the following Menu:

```
                VS-25/45 Diagnostic Monitor Package
                      Test Selection Option
To Select Tests, Position Cursor And Press Any NON-BLANK. Press SPACE
or DELETE To Deselect a Test. Press PF8 to Start An Automatic Sequence.
Press ENTER to Begin Testing. Press PF16 to Terminate.

          Test Name                              Test Name

_ CP Control Memory Diagnostic          _ DMA Test
_ BP/CP Communication Test              _ SA850 Floppy Disk Diagnostic
_ BU Branch OPcode Test                 _ Q2040 Quantum DA Diagnostic
_ Status, Conditional Branch            _ CMD/SMD Disk DA Diagnostic
_ Subroutine Stack Data                 _ USART/Modem Diagnostic
_ Subroutine Stack Addressing           _ Bus Processor Diagnostic
_ Registers, Immediate OPcodes          _ Telecommunications DA 1-Port
_ CPU STack Diagnostic Test             _ Telecommunications DA 2-Port
_ Logical and Shift Opcodes             _ Dumb 928 Data Link DA Diag
_ 8-Bit and 16-Bit ALU Tests            _ Smart 928 Data Link DA Diag
_ MAR, TRAM, and RCT Test               _ VS25/45 Multitasker
_ BD, IAD, CC, and DSET Test            _
_ BI BRanch Opcode Test                 _
_ CPU Tester                            _
_ Main Memory Test                      _
```

Figure 8-5. Standard Sequence Display Screen

7. Press PF8 to start the automatic sequence. (Note that the automatic sequence skips the CPU Tester. The sequence runs only as far as, and includes, the BP DMA test during one pass.)
8. Run the Stand-Alone Diagnostic Monitor (figure 8-3) for one complete, error-free pass. This should take about 15 minutes depending on main memory size. Check the Monitor Pass Count on the workstation screen to determine when one complete pass has been made.
9. If any errors occur, display the error log, using PF13, at the end of one complete pass. (Refer to paragraph 8.6.2.4.)
   If the Main Memory Integrity test fails, refer to paragraph 8.6.2.5 for instructions on how to locate the failing memory chip.
10. If no errors occurred, press PF16, EXIT, to return to the Standard Sequence display screen. (If a routine is in progress when PF16 is pressed, the routine will complete before the Standard Sequence display occurs. This may take several seconds, depending on the routine.)
11. Press PF16 again to terminate and return to the IPL Drive Selection screen.
12. IPL the system.

8.6.2.4 Displaying The Error Log

The error log may be displayed by pressing PF13. The Error Log Display Screen (figure 8-6) shows the 23 most recent Stand-Alone Diagnostic Monitor errors listed as 8-character codes, such as BE101007.

The first two digits (00-20 hex) of each error code identify the unit; the second two digits (00-20 hex) identify the test number; the third two digits (00-FF hex) identify the routine within the test; and the fourth two digits (00-FF hex) identify the error within the routine.

Error codes are written from left-to-right, top-to-bottom. They wrap-around to the top and start overlaying when the 23 x eight error log buffer becomes full.

The CE can select the failing unit from the 8-character error code and replace that unit, using the following example:

1. The USART/Modem Diagnostic portion of the Stand-Alone Diagnostic Monitor fails. (Loopback connector, WLI P/N 420-1040, is installed.)
2. Press PF13, Display Error Log.
3. Select the 1st error code character as shown in figure 8-6, such as BE101007 xx xx (where xx = don't care).
4. Use table 8-4, below, and compare the 1st error code character with the failing unit. In this case, B compares with the Bus Processor. As the USART logic is on the BP board, replace the BP board.
5. After viewing the log, press ENTER to save the error log and return to the Burn-In Sequence or press PF1 to DELETE the error log and return to the Burn-In Sequence.

```
BE101007 04 16
BE101009 04 00
BE101007 04 01
BE101007 04 02
BE101007 04 03
BE101007 04 04
BE101007 04 05
BE101007 04 06
BE101007 04 07
BE1C1007 04 08
BE101007 04 09
BE101007 04 0A
BE101007 04 0B
BE101007 04 0C
BE101007 04 0D
                    Press ENTER to Save Log, PF1 to Delete
```

Figure 8-6. Error Log Display Screen

Table 8-4. Comparing Error Code Character

1ST ERROR CODE CHARACTER	FAILING UNIT
B	Bus Processor
S	Serial IO DA or Workstation 0
M	Main Memory
C	CPU
Q	Quantum DA or Quantum disk drive
D	SMD DA or SMD disk drive
F	Diskette DA or Diskette drive
T	T/C DA

8.6.2.5 Main Memory Stand-Alone Diagnostic

If the Main Memory Integrity portion of the Self-Test Monitor fails, the Stand-Alone Diagnostic Monitor must be run to determine the location of the failing memory chip.

1. If the Main Memory Integrity portion of the Self-Test Monitor fails, the following display will appear on W/S 0 screen.

```
                    VS Self Test Monitor Package
                        System Hardware Status
                        System Volume = SYSTEM

Status              Diagnostic
Passed              (SIO) Serial Data Link Test
Passed              (BP)  USART Loopback Verification Test
Passed              (CPU) CP Control Memory & CP/BP Test
Passed              (CPU) CP Random Operands Test
Passed              (CPU) CP Integrity Test
Failed              (MM)  Main Memory Integrity Test
                    (BP)  BP DMA & MARS Test


     Error Code = 4E20

          Press PF (8) to Load Stand-Alone Diagnostic Monitor
```

Figure 8-7. Main Memory Error During Self-Test Monitor

2. Press PF8 to load the Stand-Alone Diagnostic Monitor.
3. Workstation 0 will display figure 8-5, the Standard Sequence Menu.
4. Press PF8 to run the automatic sequence.
5. Allow the Stand-Alone Diagnostic Monitor to run until memory error(s) appear (figure 8-8).

```
                    VS Diagnostic Monitor Package
  (1) = Error Loop      (4) = Program Loop   (7) = Step   (16) = Exit
  (2) = Routine Loop    (5) = Pause         (10) = Clear all Settings
  (3) = Stop on Error                       (13) = Display Error Log

Program Name : VS25/45 Main Memory Diagnostic-- Error Count         = 00077
Routine Name : 20 MM Integrity---------------   Routine Loop Count = 00000
Error Code   = ME002001                         Program Loop Count = 00000
Program Status : Test In Progress               Monitor Pass Count = 00000

Messages:

  RECEIVED DATA NOT EQUAL TO EXPECTED DATA
  RECEIVED DATA (MDR)  =  00 05
  EXPECTED DATA  =  00 04
  ADDRESS (MAR1)  =  0E 05 20
  (Status Bit 5 = 1 indicates MM Parity Trap taken)
  (Status bit 12 = 1 indicates Invalid Address Trap taken)
  CP Status Register  =  24 10
```

Figure 8-8. Main Memory Error During Stand-Alone Monitor

6. Press PF3, Stop On Error.
7. Look at the Messages portion of W/S 0 screen, using figure 8-8 as an example, showing:

   a. RECEIVED DATA NOT EQUAL TO EXPECTED DATA
   b. RECEIVED DATA (MDR) = 00 05
   c. EXPECTED DATA = 00 04
   d. ADDRESS (MAR1) = 0E 05 20

8. Look at the two high order MAR1 address hex digits and find the correct row of RAM chips on the main memory board from table 8-5.

   a. EXAMPLE - ADDRESS (MAR1) = 0E xx xx (where xx = don't care).

Table 8-5. Converting MAR Address to RAM Chip Row

TWO HIGH ORDER HEX DIGITS	ROW	
0E or 0F	7	(TOP)
0C or 0D	6	
0A or 0B	5	
08 or 09	4	
06 or 07	3	
04 or 05	2	
02 or 03	1	
00 or 01	0	(BOTTOM)

   b. The failing chip is in row seven (top row of figure 8-9, the layout of the 210-7900 Main Memory board).

9. Look at the four MDR data hex digits and find the correct chip in row seven from figure 8-9.

   a. EXAMPLE - RECEIVED DATA (MDR) = 00 05
   - EXPECTED DATA = 00 04

DATA HEX DIGITS	TWO HIGH ORDER DIGITS								TWO LOW ORDER DIGITS							
DATA BITS	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
RECEIVED DATA (00 05)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
EXPECTED DATA (00 04)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
DIFFERENCE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

   b. The difference shows that the first low order hex digit picked up a 1-bit.
   c. Looking at figure 8-9, the 1-bit of the first low order hex digit in row seven is L1, the failing chip.

10. Power down the system, remove the 210-7900 Main Memory board, and replace the failing memory chip. Refer to Chapter 7, Illustrated Parts Breakdown for RAM chip part numbers.
11. Power up the system and rerun the Stand-Alone Diagnostic Monitor to make sure that there are no more errors.

TOP OF BOARD

	TWO HIGH ORDER HEX DIGITS								TWO LOW ORDER HEX DIGITS							
DATA BITS	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
ROW 7	L24	L23	L22	L21	L20	L19	L18	L17	L8	L7	L6	L5	L4	L3	L2	L1
ROW 6	L48	L47	L46	L45	L44	L43	L42	L41	L32	L31	L30	L29	L28	L27	L26	L25
ROW 5	L72	L71	L70	L69	L68	L67	L66	L65	L56	L55	L54	L53	L52	L51	L50	L49
ROW 4	L96	L95	L94	L93	L92	L91	L90	L89	L80	L79	L78	L77	L76	L75	L74	L73
ROW 3	L120	L119	L118	L117	L116	L115	L114	L113	L104	L103	L102	L101	L100	L99	L98	L97
ROW 2	L144	L143	L142	L141	L140	L139	L138	L137	L128	L127	L126	L125	L124	L123	L122	L121
ROW 1	L168	L167	L166	L165	L164	L163	L162	L161	L152	L151	L150	L149	L148	L147	L146	L145
ROW 0	L192	L191	L190	L189	L188	L187	L186	L185	L176	L175	L174	L173	L172	L171	L170	L169

BOTTOM OF BOARD

Figure 8-9. 210-7900 Main Memory Layout

8.7 VS-25/45 MEMORY AND PERIPHERAL DIAGNOSTICS

Memory and peripheral diagnostics available to the VS-25/45 are divided into two categories: On-Line and Stand-Alone. The following paragraphs provide a brief description of these diagnostics.

8.7.1 ON-LINE DIAGNOSTICS

With On-Line diagnostics, located in library @SYSTST@, the CE logs on to the system through a workstation and executes a specific test routine, which runs under control of the operating system (while the customer is running). All currently available VS 60/80/100 on-line test routines will be available on the VS-25/45. Diagnostic programs currently available for individual peripherals are as follows:

Table 8-6. On-line Diagnostics

DIAGNOSTIC NAME	WLI P/N	VERSION	FUNCTION
TPTEST	702-0187	6224	Magnetic tape diagnostic for Kennedy and Telex tape drives. Requires OS version 5.01.51 or later.
FTU On-line	195-2652-3	6365	On-line version of FTU simulator. Supports all current VS disk drives including soft-sector. Allows CE to do most disk read, write, and control functions. CE can do most disk alignment procedures without removing disk drive from system. Requires OS version 5.0 or later.
Device Monitor	702-0175	21A0	Tests for all serial WSs, AWSs, AWS Hard or Soft-sectored controller boards, TCB1, TC Black Box, and Z80 typesetter.
VS On-line Printer Part I Monitor	702-0179A	2242	Low speed serial printers including 5521,5531, 5535, 5581WD, 6581WC and DW20.
VS On-line Printer Part II Monitor	702-0178	2211	High speed serial printers, including 5570/71, 5573/74, 5575, and 5531W6.

8.7.2 STAND-ALONE DIAGNOSTICS

Using the Stand-Alone diagnostic routines, located in library @DIAGMN@, the CE creates a mini-operating system with a menu display of all currently available Stand-Alone test routines. The CE then selects and executes the desired test. The customer cannot access the system while these tests are being performed. Currently available diagnostics are as follows:

Table 8-7. Off-line Diagnostics

DIAGNOSTIC NAME	WLI P/N	VERSION	FUNCTION
FTU45	732-0026		Allows the exercising of disk units still connected to the system. Permits verifying, reading and writing, initializing, positioning heads, and alternate seeks. The following are the device numbers to run FTU45 on other VS-25/45 disk drives: 100 - for diskette drive. 110 - for system Quantum drive #1. 111 - for optional Quantum drive #2. 120 - for SMD DA, port 0 121 - for SMD DA, port 1 122 - for SMD DA, port 2 123 - for SMD DA, port 3
Stand-Alone Boot Loader	195-7479-3	82C8	Displays diagnostic menu on Workstation 0. @SYS000@ first loads the microcode file @MC2246S into the WS, then displays the diagnostic menu.
Stand-Alone Diagnostic Monitor	195-2458-5	R235F	Refer to paragraph 8.6.2

8.8 CONTROL MODE

Control Mode is a CPU state where normal programming activities are suspended and certain other facilities (mainly diagnostic and initialization) are made available to the user. These facilities are divided into two groups of commands as follows:

1. LOAD Group - contains commands for initializing the OS, loading a Stand-Alone program, loading a diagnostic program, or restarting a program from an initialized state.
2. DEBUG Group - contains commands for displaying or modifying main memory, general registers, control registers, or the PCW. Also included in this group are commands for single step program execution, hard copy dump of memory and registers, and virtual address translation.

Control Mode uses Workstation 0 for communications between the operator and the system. To enter Control Mode, Workstation 0 must be powered-on. Control Mode uses only the top line of the CRT display (line one); the contents of the line are saved on entry and restored at exit. This makes Control Mode transparent to any program that may be using Workstation 0. For a detailed discussion of Control Mode commands, refer to Chapter 6 of the VS Principles of Operation manual (WLI P/N 800-1100PO-04). All standard VS 60/80/100 control mode functions are available on the VS-25/45.

Table 8-8. VS-25/45 BP Operating System Error Codes

ERROR CODE	CONDITION
Blank	No error, normal operation
00E0	Unable to load microcode to workstation 0
00E1	Main memory parity error occurred during Code RAM DMA
00E2	Main memory DMA attempted to access nonexistent address
00E3	BP Data RAM parity error occurred
00E4	Front Panel Bootstrap Media switch in wrong position
00E5	Pascal exception of unknown origin occurred
00E6	An invalid device adapter type value has been detected
00E7	A DMA operation between data RAM and main memory timed out

Front Panel HEX Displays of BP System Code

ERROR CODE	CONDITION
00E8	CP set illegal command out area code
00E9	Repeated DMA attempts for command out area failed
00EA	Repeated DMA attempts for processor interrupt area failed
00EB	SIO/CIO raced with EC or NC IOSW (possible OS failure)
00EC	IRQ/DAR raced with EC or NC IOSW (possible OS failure)
00ED	Main memory error correction count exceeded it's limit of 1

Front Panel HEX Displays. Results
of BP Initiating Control Mode Entry

ERROR CODE	CONDITION
00EE-00F3	Not used
00F4	IPL device returned damaged status (hardware error)
00F5	IPL device was not ready (intervention required)
00F6	BP memory or disk address error while accessing IPL device
00F7-00FF	Not used

Front Panel HEX Displays only
when BP is in Control Mode

VS-25/45 OPERATOR LEVEL TROUBLESHOOTING FLOW CHART

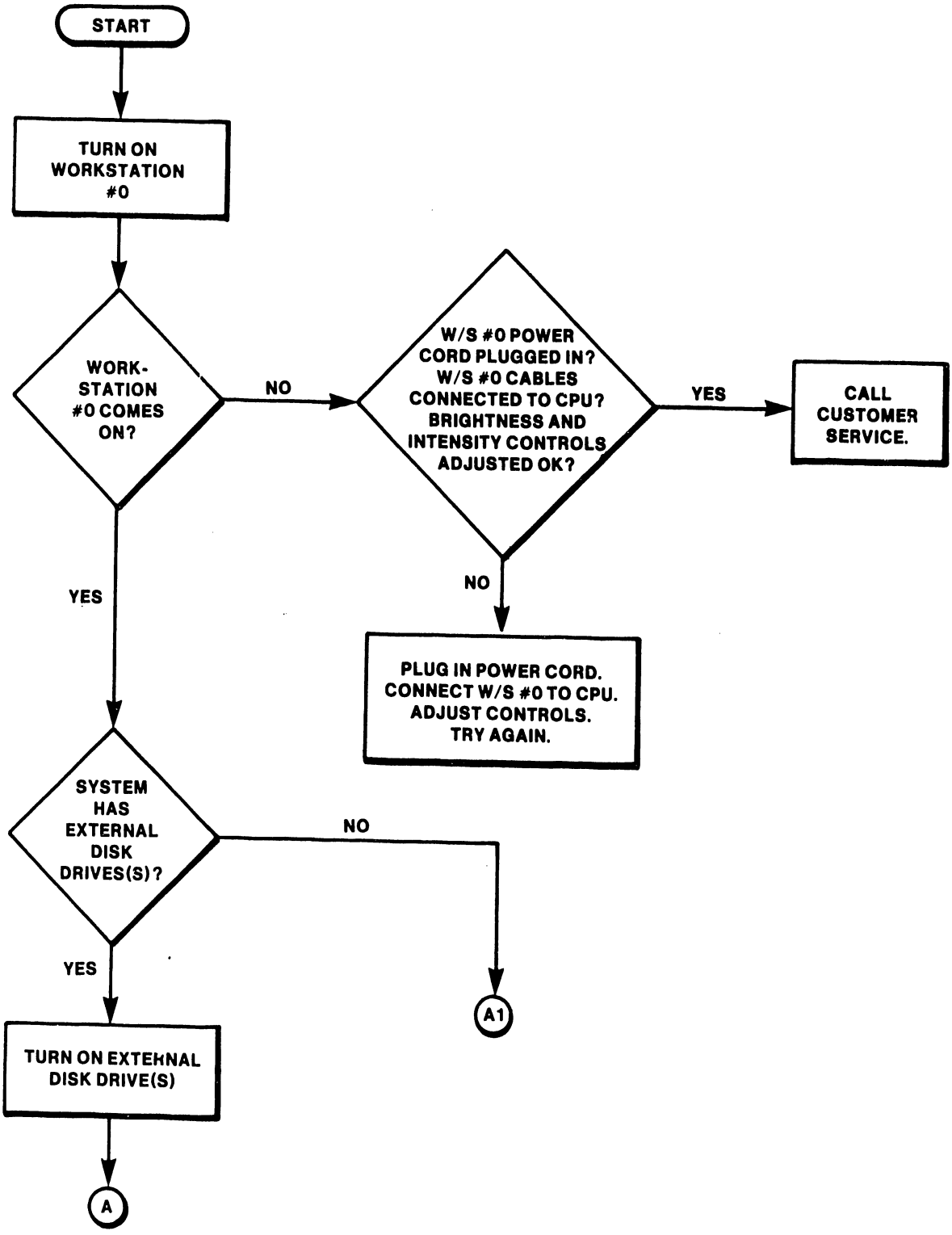


Figure 8-10. Operator Troubleshooting Flowchart (1 of 5)

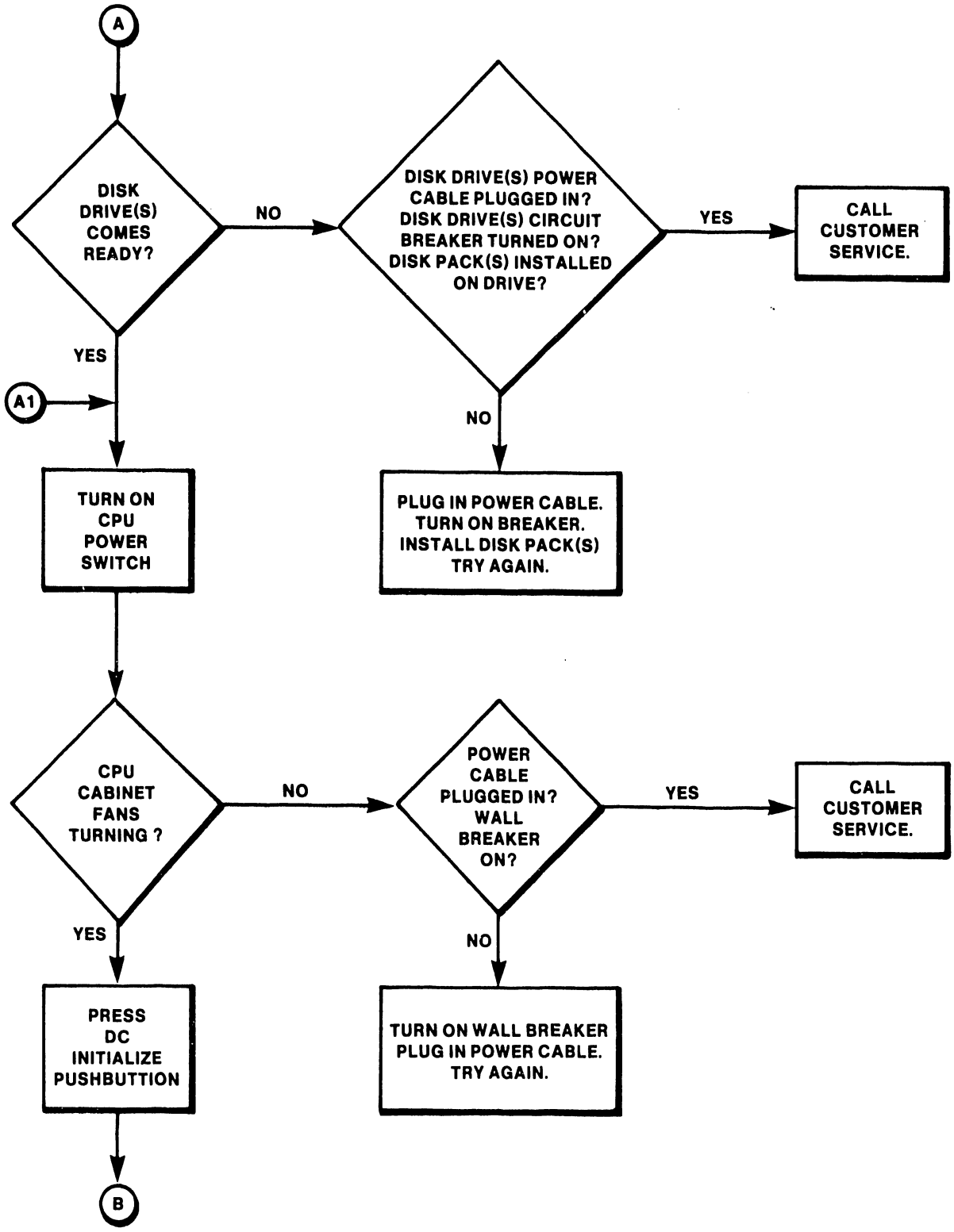


Figure 8-10. Operator Troubleshooting Flowchart (2 of 5)

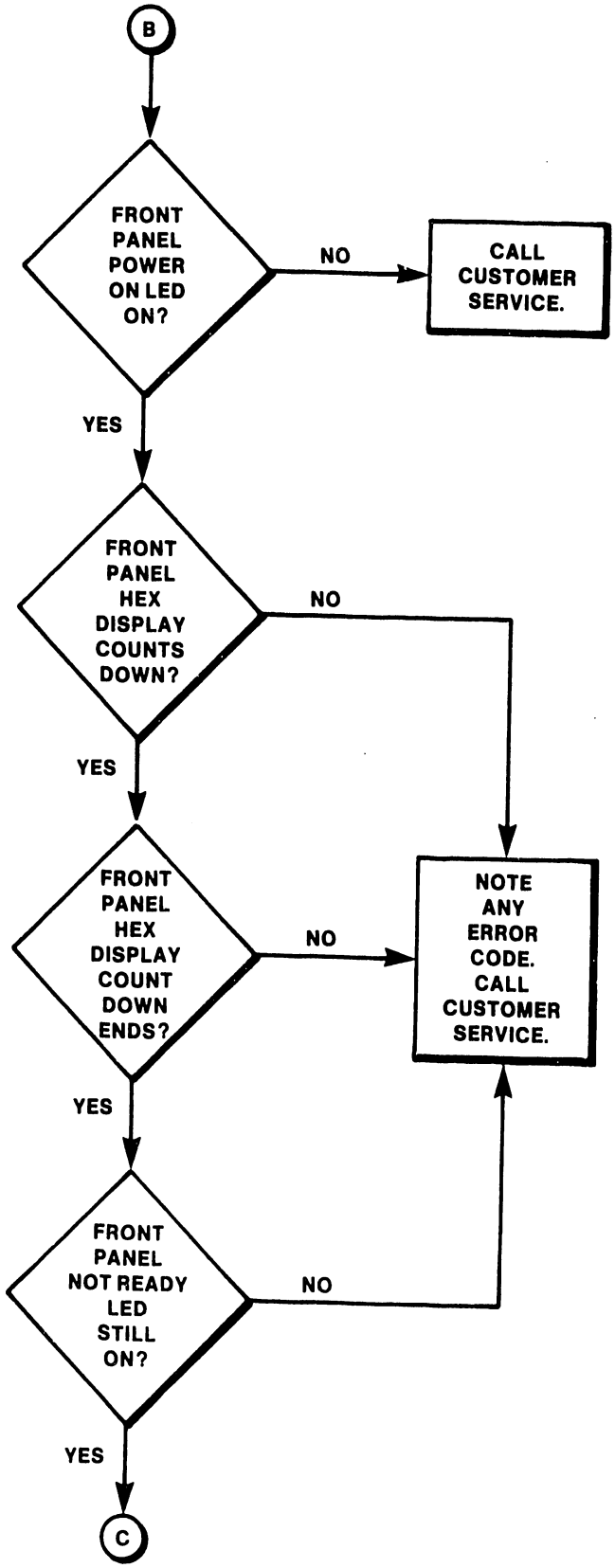


Figure 8-10. Operator Troubleshooting Flowchart (3 of 5)

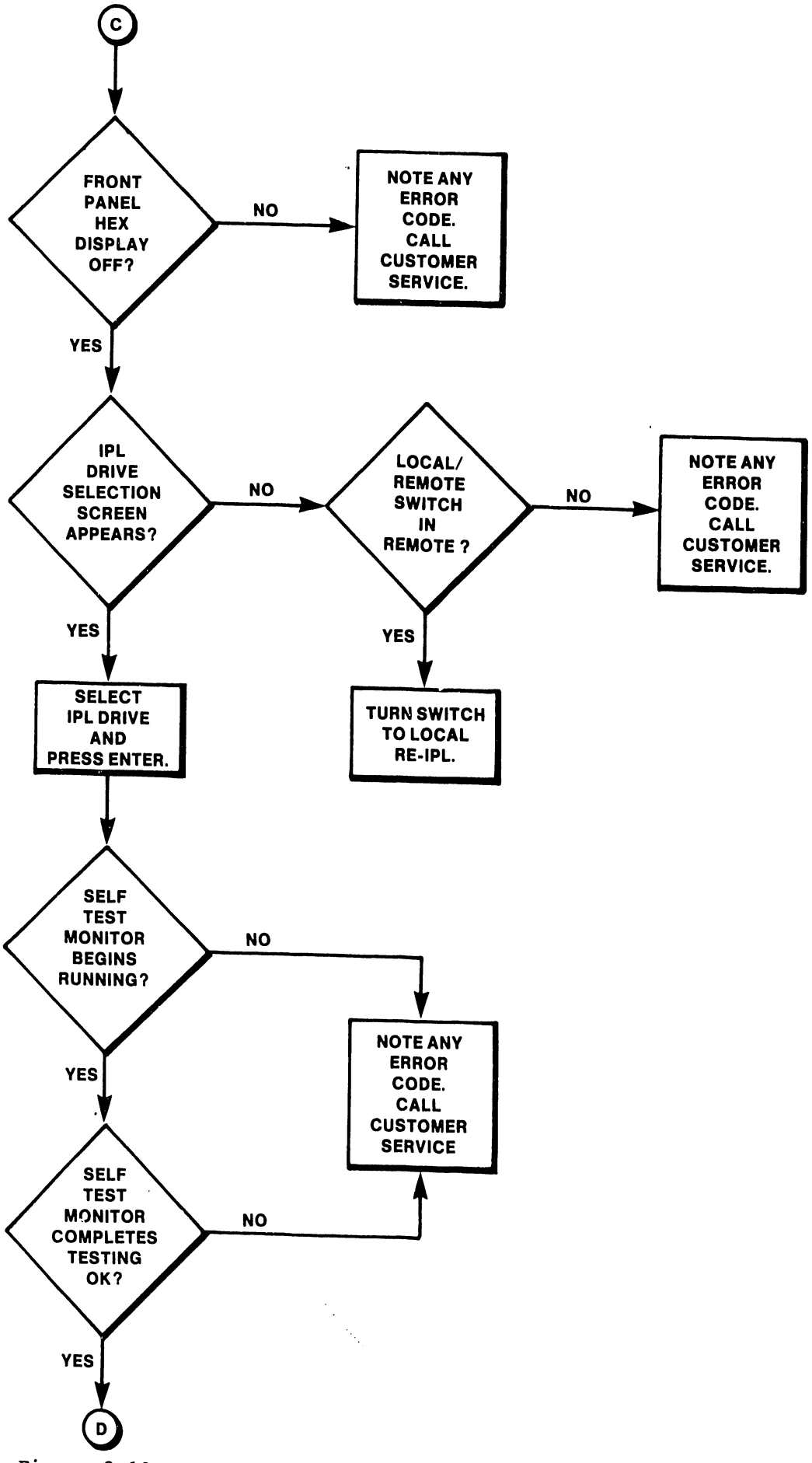


Figure 8-10. Operator Troubleshooting Flowchart (4 of 5)

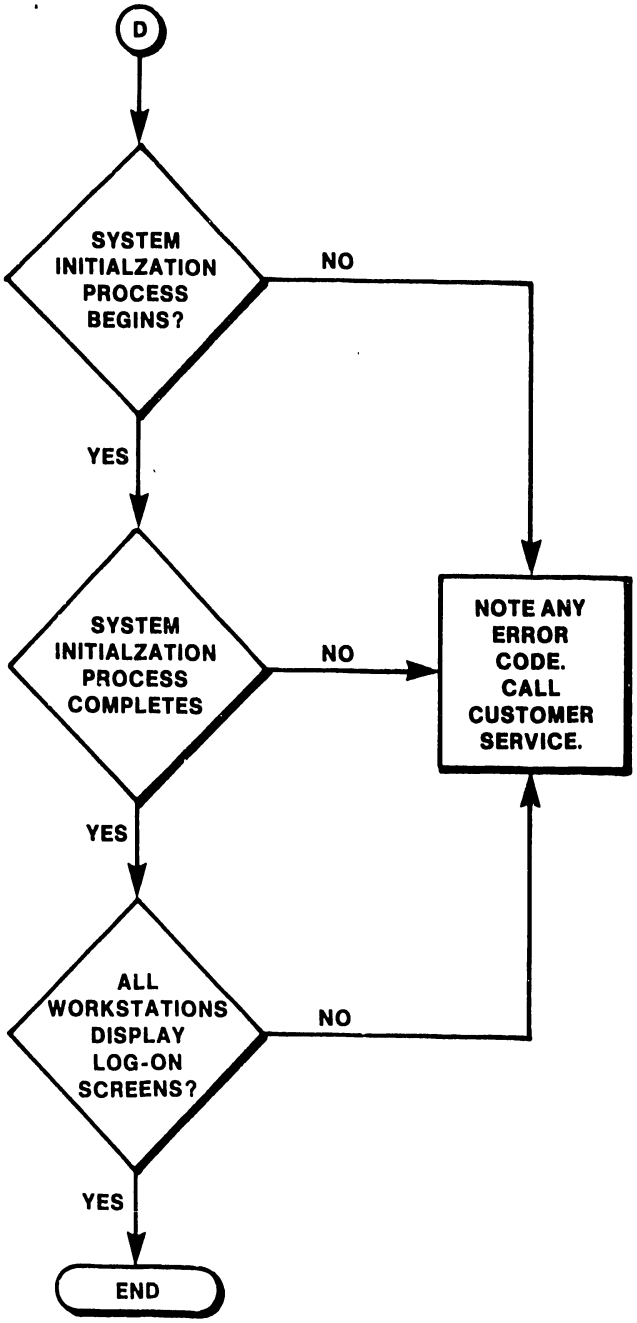


Figure 8-10. Operator Troubleshooting Flowchart (5 of 5)

VS-25/45 CUSTOMER ENGINEERING LEVEL TROUBLESHOOTING FLOW CHART

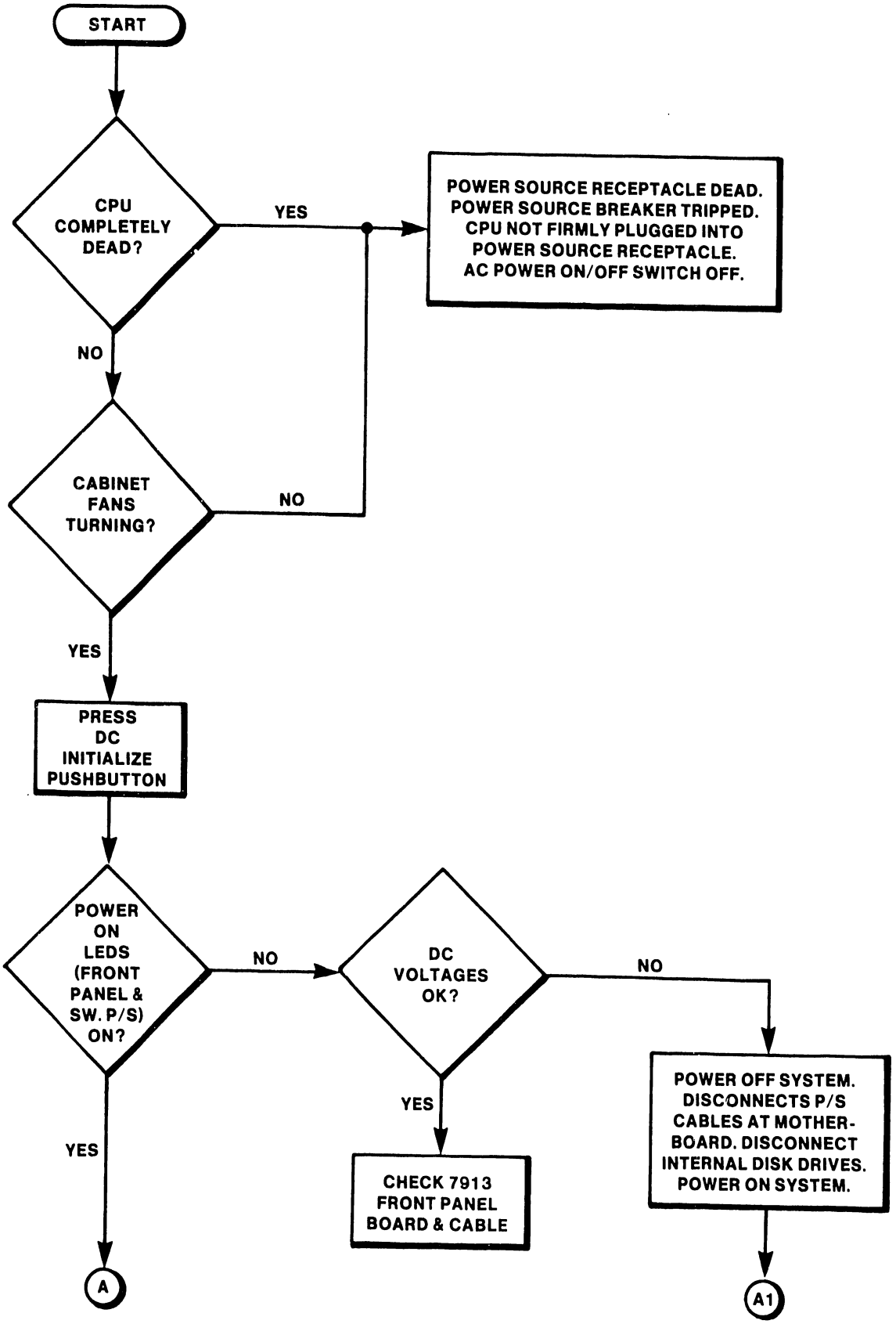


Figure 8-11. CE Troubleshooting Flowchart (1 of 5)

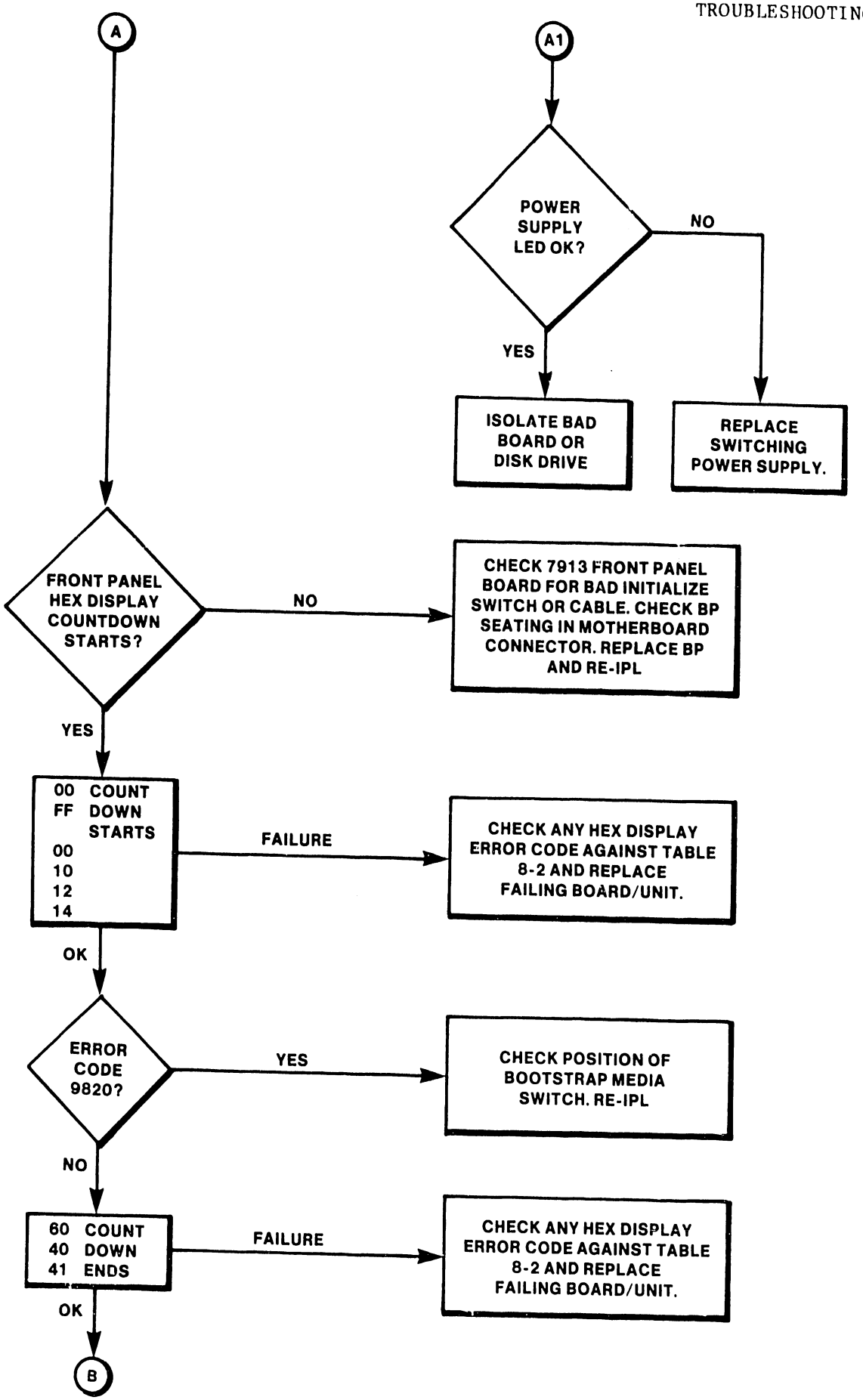


Figure 8-11. CE Troubleshooting Flowchart (2 of 5)

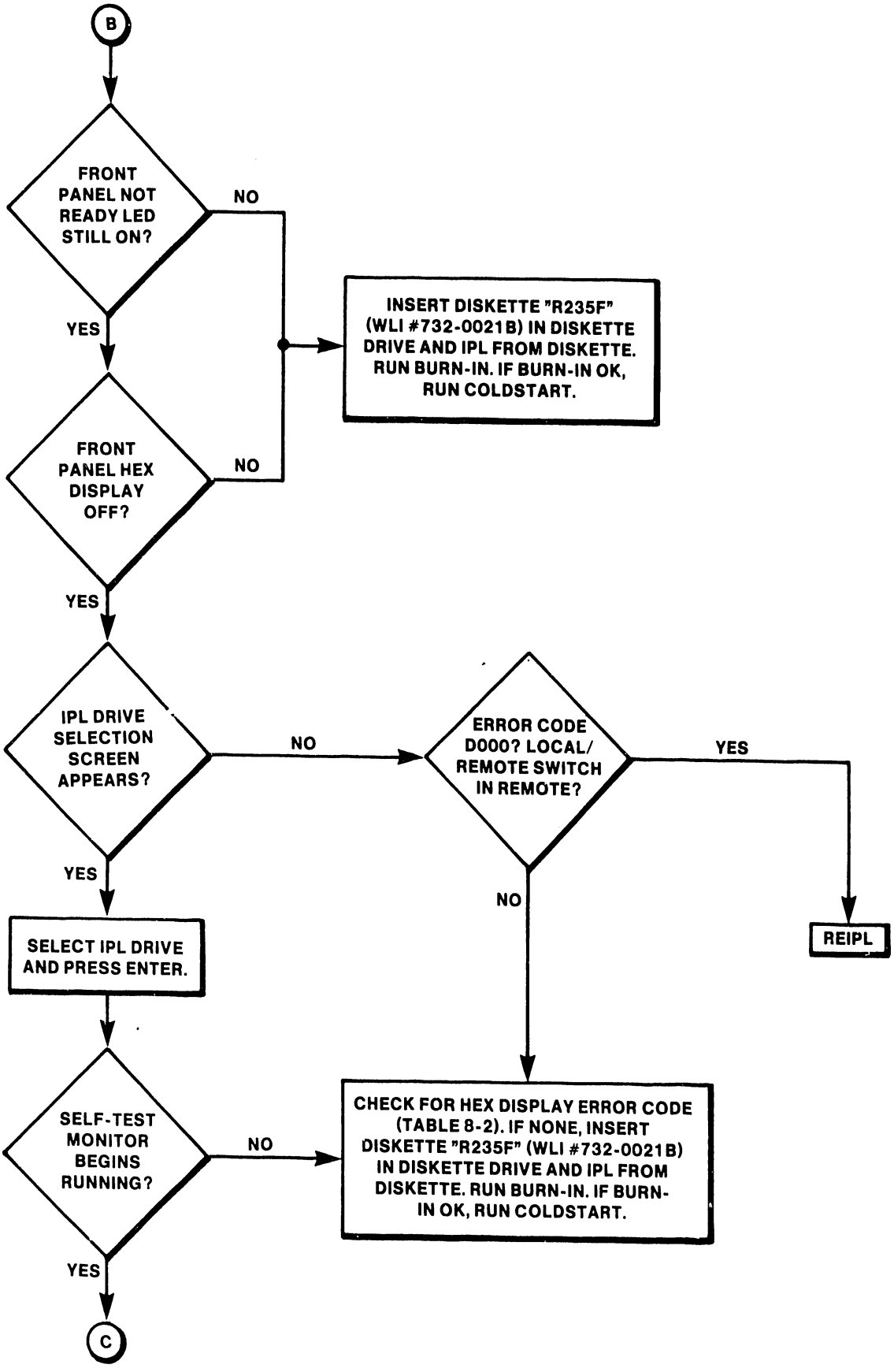


Figure 8-11. CE Troubleshooting Flowchart (3 of 5)

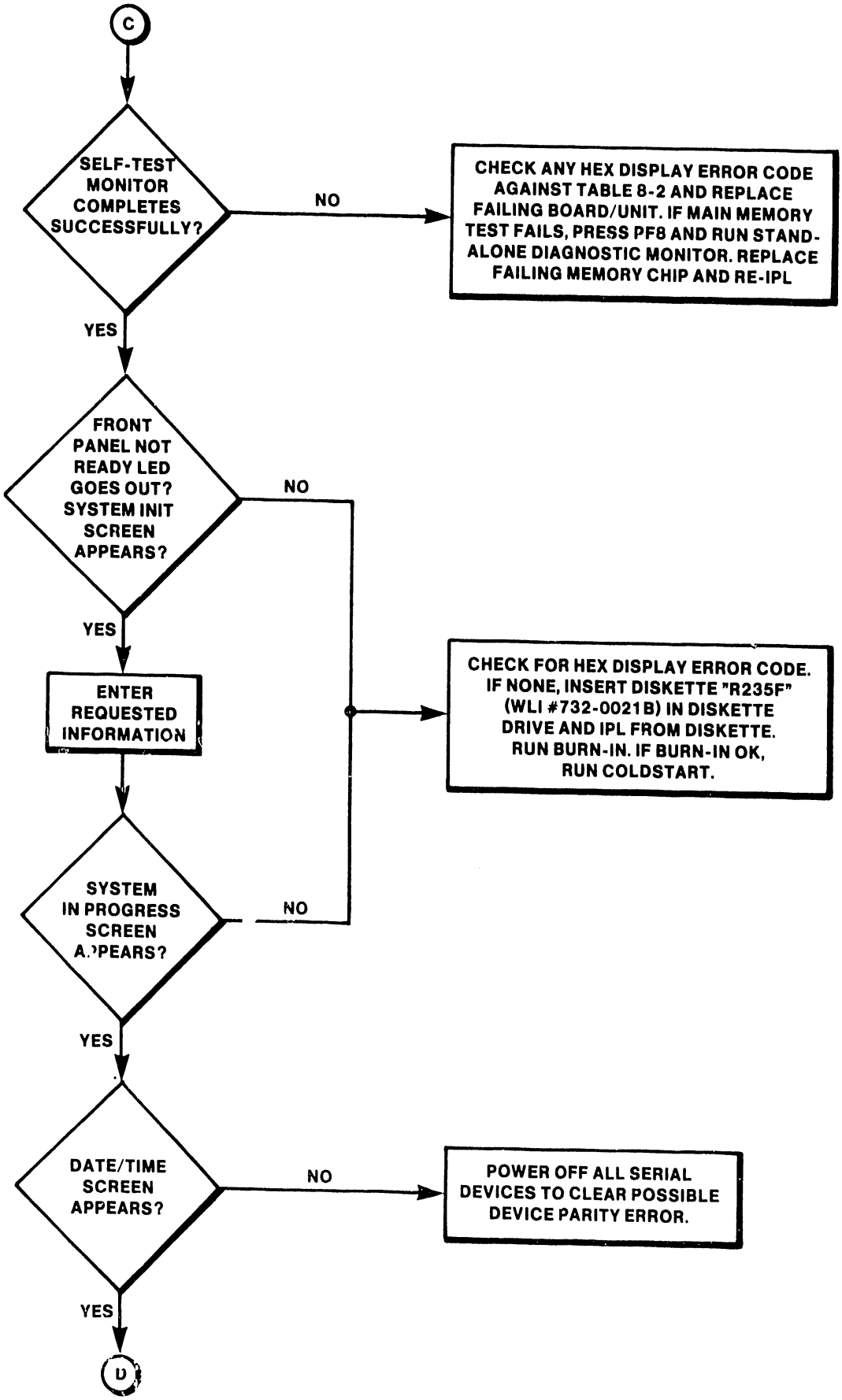


Figure 8-11. CE Troubleshooting Flowchart (4 of 5)

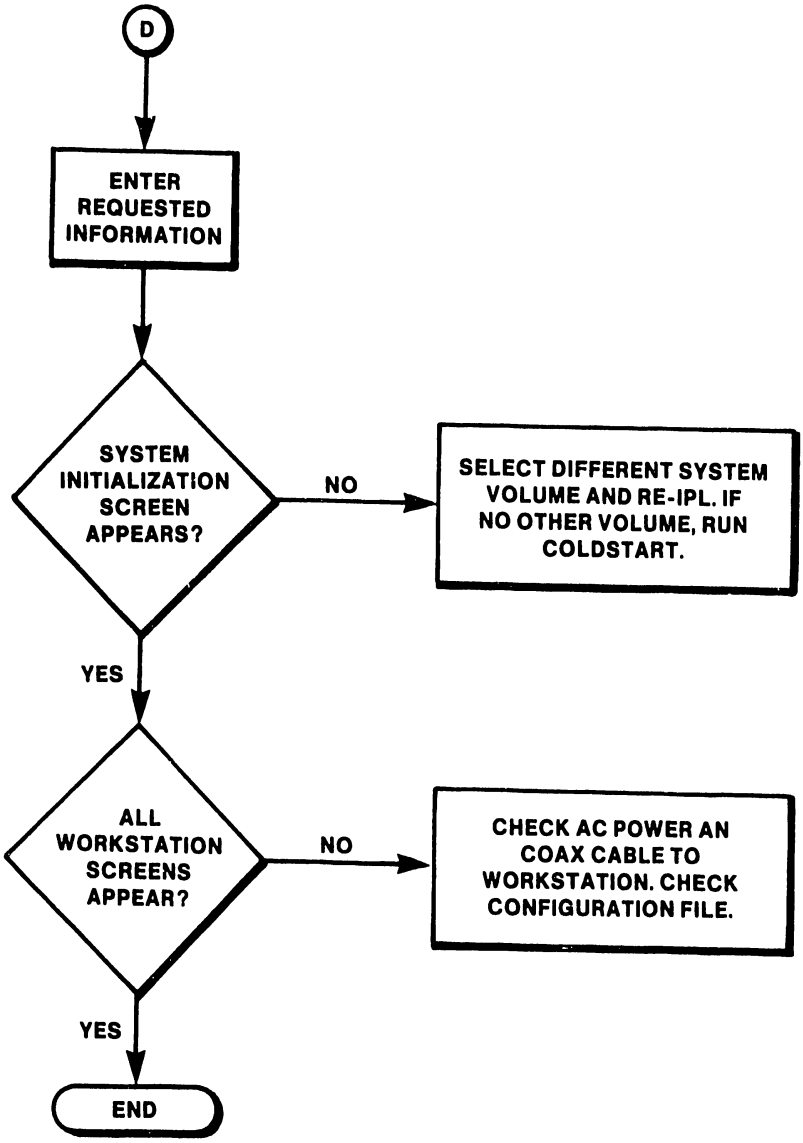


Figure 8-11. CE Troubleshooting Flowchart (5 of 5)

APPENDIX A

APPENDIX A

MNEMONICS, WORDS/PHRASES, MICROINSTRUCTIONS, & MISCELLANEOUS HARDWARE RELATED FUNCTIONS

DEFINITIONS FOR VS-25/45 SIGNAL-NAME (TRUE) MNEMONICS

MNEMONIC	DEFINITION	SOURCE	DESTINATION	DESCRIPTION
BPA0-19	BP Addresses	BP	CP, DA's	Addresses to load CPU CM RAM
BPD0-15	BP Data	BP	CP, DA's	Data for CPU CM RAM
BPINT0-15	BP Interrupts	BP	BP	Interrupts from 8253 PIT to 8259A PIC
BR0-15	B Register	CP	Cp	B Register data output
CB0-31	C Bus Data	CP	CP	C Bus output data
CM0-39	Control Memory	CP	CP	Microinstruction Data Bits
CN0-7	BALU	CP	CP	8-bit BALU output
DA0-15	Data RAM Addresses	DA's	BP	One word of address for BP Data RAM addressing
DD0-15	Data RAM Data	BP,DA's	DA's,BP	One word of data to or from BP/DA's
DN0-7	DALU	CP	CP	8-bit DALU output
MA0-20	Memory Address	CP,BP DA's	MM	CP/BP/DA memory addresses for main memory
MAR0-23	Memory Add Reg	CP	CP	MAR output addresses
MD0-15	Memory Data	MM	CP,BP,DA's	CP/BP/DA memory data to/from main memory
MDR0-15	Memory Data Reg	CP	CP	MDR output data
MCB0-2	Main Memory Control Bits	CP,BP, DA's	MM	Command bits for MM
MGS0-7	Memory Grant Strobe	MM	CP,BP, DA's	Main Memory Access granted
MRI0-7	Memory Request In Strobe	CP,BA, DA's	BAP	Request to main memory for access
MSB0-1	Main Memory Status Bits	MM	CP,BP, DA's	Status bits from the MM
PMR0-7	Program Mask Register	CP	CP	Program Mask Reg data output

MNEMONIC	DEFINITION	SOURCE	DESTINATION	DESCRIPTION
PTO-15	Page Table	CP	CP	Page Table output from T-RAM
SDO-15	Stack Data	CP	CP	Data from CP Stack
UO-15	BALU	CP	CP	16-bit BALU output

VS-25/45 MNEMONICS

MNEMONIC	HARDWARE ORIENTATED DEFINITION
A-Register Source Selector	Selects 1 of 4 inputs for A-Register
ALLOW PE	Allow code RAM parity error
ALU	Arithmetic-Logical Unit
ALU Input Selector	Output to 8-bit Decimal ALU/Binary ALU
ALU Level 1	All ALU operations
ALU Level 2	Most ALU operations
ALU Level 3	Move operations
AMX0-2	Input select bits for A-Register Source Selector. From Process Field Decoder
AR0-15	A-Register data
Auxiliary Registers	Work or spare CP Stack registers
BALU	Binary Arithmetic Logic Unit(s) (8 and 16-bit)
BCD	Binary coded decimal
BIU	Bus Interface Unit
BMDS	Memory Data Strobe
BP	Bus Processor
BP-DSB	BP status bit. ECC failure encountered during BP access of Data RAM
BP-TR1	BP status bit. Initialize button pressed
BP-TR2	BP status bit. Reset button pressed
BPA0-19	BP Addresses
BPD0-15	BP Data
BR0-15	B Register Data
BRCK	B Register Clock
C-Bus Selector	Selects 1 of 4 inputs for C-Bus
CA	Carry Bit
CAS	Column Address Strobe
CB0-15	C-Bus Data
CBT	Change bit
CCS0-1	Condition Code bits
CDLI	Control Device Level Interface
CIO	Control I/O
CM	Control Memory
CM	Control Mode
CNT0-1	Used to address Process Field Decoder PROMs. Generated by counter clocked by master clock
CP5	VS-25/45 Central Processor
CPDEN	CP Data Enable
CRAM	Code RAM
CRYSTAL	Crystal clock speed for Data RAM
CSEL	CM bit 12. Selects high or low order byte of CP Stack data for 8-bit ALUs
DA	Data RAM Address
DALU	Decimal Arithmetic Logic Unit (8-bit)
DD	Data RAM Data
DEC	Status bit set for Invalid Decimal digit found in A or B Bus Operand for Decimal Add/Subtract with Carry
DEF	Dual Error (Memory)

MNEMONIC	HARDWARE ORIENTATED DEFINITION
DGS	Data Grant Strobe
DIGS	Data In Grant Strobe
DMA	Direct Memory Access
DRAM	Data Random Access Memory
DRI	Data Request In
ECC	Error Correction Code
ECNT	Error Count
ENO-2	BP address bits 1 and 2 used to enable Control Memory bus transceiver
EU	Execution Unit
FAST	Fast clock speed for Data RAM
FDC	Diskette Drive Controller
Fault bit	T-RAM invalid virtual address
General Registers	Outer program General Registers
HOB	High Order Bit
I/O	Input/Output
IA2-12	Addressing for Control Memory RAMs (IA2-12) from Instruction Counter Register
IC	Instruction Counter
IC Source Selector	Selects address source for Control Memory RAM
ICO-1	Chip select for Control Memory RAMs
INVA	Invalid physical memory address
IO3	Interrupt to let BP know when current I/O-Interrupt has been accepted by CP
IO4B	Interrupt bit providing interlock so CP does not overwrite current command before BP can process it
IODEN	I/O Data Enable
IODTR	I/O Data Transmit/Receive
IORD	I/O Read
IOWR	I/O Write
IPL	Initial program loading
IREG	Instruction Register
IREG	Indirect Register
Immediate/Stack Data Selector	Selects input to 8-Bit Binary/8-Bit Decimal ALU
Instruction Counter Register	Addressing for Control Memory RAM
Instruction Length Code	Indicates length of current machine language instruction. Used by specialized microinstructions to support outer-level machine language
LDBR	Load B-Register
LDSO-2	Load strobes
LOOPBACK	Loop necessary signals back to test UART
MA	Memory Address
MAO-12	Memory address bits
MAO-20	Memory address lines
MA11-20	Memory Address Output Buffer Data
MAR1	Memory Address Register #1
MAR2	Memory Address Register #2
MCB	Memory Control Bit
MD	Memory Data
MDR	Memory Data Register

MNEMONIC	HARDWARE ORIENTATED DEFINITION
MDRH	Memory Data Register High
MDRL	Memory Data Register Low
MDS	Memory Data Strobe
MG	Memory Grant
MGS	Memory Grant Strobe
MM-DSB	BP status bit. ECC during MM DMA access of Data RAM
MSB0	Invalid main memory address
MSB1	ECC Error
MOP	Memory operation field (Control Memory bits 18-22)
MPAR	Memory Parity Error
MRI	Memory Request In
MSB	Memory Status Bit
MSEL	Trap 0003/0006. MAR in use when trap taken
Main Memory ECC	Error Correction Code
Memory Address Output Selector	Concatenates 13 bits of T-RAM addresses with low order 11 bits of virtual address to form 24-bit physical Main Memory address
MAR Input Selector	Selects high input order bits for MAR from C Bus or T-RAM
PA	Physical Main Memory address
PMR	Program Mask Register
PROM	Programmable Read Only Memory
Process Field Decoder	Control signals stored in PROMs
R/W	Read/Write
RAM	Random Access Memory
RAS	Row Address Strobe
RBT	Reference bit
RCT	Page Frame Reference And Change Table
RDE	Read
REF	Refresh
RMW	Read modified write
Read and Write Protect Bit	Protects page against being read or over-written.
Ripple operation	Increment/decrement MAR
SD0-15	CP Stack Data
SEF	Main memory single bit error
SHBR	Shift B-Register
SID	System Identification Number
SIO DA	Serial I/O Device Adapter
SLOW	Slow clock speed for Data RAM
SMX0-7	Generated from Process Field Decoder to select Stack Address Multiplexor for CP Stack Addressing
SRD0-12	Source of address of next microopcode to be executed. From Subroutine Return Register
Snn(0-15)	CP Status bits
Stack	Local RAM area used for temporary storage by CP
Stack Address Multiplexor	Selects Stack Address source
Stack Byte Selector	Select high/low order byte of CP Stack data for 8-bit ALUs
Stack File Registers	Work registers for CP microprogram

MNEMONIC	HARDWARE ORIENTATED DEFINITION
State	System/User State
Subroutine Return Register	Contains next microinstruction address, to be used for Conditional Subroutine Return
System Mask bits	PMR2-5. Enables/ disables various interrupts
System Registers	Outer program Control/ Floating Point Registers
T-RAM	Translation RAM (PT0-15)
TALIGN	Alignment Trap
TBI	Pagespan Trap
TC	Telecommunications
TCC	BOP Trap
TIM	Real-time clock tick
TRAP03	Translation Trap (T-RAM Fault)
TRAP04	Protection Trap (Page Table 1/2)
Traps	Interrupts to CP microprogram
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
VA	Virtual memory address
VCO	Voltage Controlled Oscillator
WP	Write Pulse
WT0-2	Write enable for Control Memory RAM. From IOWR-IO Write
Work Registers	128 16-bit CP Stack registers used in relation to translation operations
XD0-15	Control Memory data bus transceiver data
XDR0-15	Input from BP to IC Source Selector as source for address of the next microopcode to be executed

MNEMONIC	SOFTWARE ORIENTATED DEFINITION
BOP	Branch field of CP microinstruction
FLUB	File Length and User Block
INVA	Invalid Address
IO	Input/Output
IOCA	I/O Command Address
IOCW	I/O Control Word
IOSW	I/O Status Word
LRU	Least Recently Used
MMPFT	Main Memory Page Frame Table
MOP	Memory Operation field of CP microinstruction
NOP	No Operation
OS	Operating System
OVF	Overflow
PA	Physical Address
PCW	Program Control Word
PF	Page Frame
PFN	Page Frame Number
POP	Process field of CP microinstruction
PT	Page Table
PTA	Page Table Address
PTE	Page Table Entry
R/C	Reference and Change status bits
RP	Read Protect
RS	Reset State
Segment 0	512 Kbytes of supervisory routines/data for Op System
Segment 1	512 Kbytes for user program
Segment 2	4K to 512 Kbytes (in 4K increments) for user data
SIO	Start I/O
SQB	Status Qualifier Byte
VA	Virtual Address
WP	Write Protect

VS-25/45 WORDS/PHRASES

WORD/PHRASE	DEFINITION
Background Processing	Automatic execution of batched lower priority programs by Operating System whenever no higher priority programs are being handled.
Base Address	Starting address of a page frame.
Byte Index	A value, when added to a base address, that results in true physical address of a byte in main memory.
Command Processor	Special program used to call up all system functions.
Concatenated	Linked together in a series.
Current PCW	The "active" or "controlling" PCW - the one that pertains to instruction that is currently being executed.
Data Base Management System	Process (program) that allows multiple users to access common data files.
Demand Paging	Memory management feature where portions of a program are called into memory as they are needed.
Displacement	See Byte Index.
Distributed Processing	Technique of sharing a Central Processor among more than one user.
Dynamic Access Mode	Technique which lets program switch back and forth between sequential access and random access in same data file.
File	Logical unit of data records.
Indexed Filing	Technique which stores data records in the order of specified key values.
Interactive	Process to allow users to communicate directly with a system (eg; from a workstation).
Locality Of Reference	Quality of a program prepared for maximum execution speed by means of remaining on one page frame as long as possible before branching elsewhere.
Macro	Named routine that is called up for processing whenever the corresponding name is specified as part of a high level instruction.
Linking	Connecting or tying together.

WORD/PHRASE	DEFINITION
Macro ('Inner-layer' type)	Series of microinstructions which, when executed, accomplish the purpose of the Macro ... equivalent to a machine instruction, IBM instruction, or Assembler instruction).
Macro ('outer-layer' type)	An instruction which, when executed, calls up a sequence of instructions (a subroutine) for execution, and then branches back to the original program.
Macroassembler	Computer having the capability to process defined macro's.
Macroinstruction	Name of a routine, prepared in Assembler language, that gets called up for execution whenever the name is used as part of a high level instruction.
Menu	Generally, a list of available options displayed on the CRT when the system is turned on or after an operation has been completed. The term menu should be used to define the presence (existing or desired) of a list of two or more program branching possibilities OR parameter identification inputs that the system must solicit from the operator.
Multiprogramming	Quality of a computer to process more than one program simultaneously.
Outboard Side	External to (away from) the CP.
Page	Block of 2,048 contiguous one-byte virtual memory locations that begin at an address of zero, 2048, or some multiple of 2048.
Page Fault	Indication that a particular page is not in main memory.
Page Fault Exception	Error condition indicating that a page is invalid.
Page Frame	2K blocks of contiguous one-byte physical memory locations that begin at a physical (main) memory address of zero, 2048, or some multiple of 2048.
Page In	Read from disk into main memory.
Page Out	Write to disk from main memory.
Page Table	An entry into Translation RAM containing the starting address of a physical page boundray.

WORD/PHRASE	DEFINITION
Paging Task	That portion of the operating system that controls paging.
Print File	Disk file that is to be printed by a specific printer at the convenience of the Operating System and/or the System Console operator.
Print Queue	Collection of print file records pertaining to one or more printers (also, the sequence list identifying those records and the order in which they are to be printed).
Print Spooling	Temporarily storing print jobs on disk until a printer is available.
Procedure (Language)	Language used to create special text functions to perform operations normally executed interactively at a workstation.
Program Interrupt	Break in the normal sequence of instruction execution because of an error or request for assistance. The supervisory system seizes control to take action.
Prompt	Name of a message (usually a one-liner) directing the operator to perform some action.
Relocatability	Capability of a program to be initiated at any page frame and to randomly occupy any number of additional page frames as a consequence of a linkage of its subsequent parts by an address pointer.
Segment	Block of contiguous one-byte virtual memory locations, with the block beginning on a decimal value virtual address of zero, 1,048,576, or some multiple of that value.
Segment Control Register	CP register containing the page table virtual address and the page table length.
Sequential Filing	Technique which stores data records in the order in which they are written or entered.
Stack	Local RAM area used for temporary storage by the CP.
Swapped Into	When an entire program is brought into main memory and allowed to run for a certain amount of time.
Swapped Out	When an entire program is replaced in main memory by another program which is allowed to run for a certain amount of time.

WORD/PHRASE	DEFINITION
System Console	Workstation that additionally or alternatively controls special functions not available to other, "regular" workstations of the system.
Thrashing	Phenomenon of excessively moving pages back and forth between memory and secondary storage" (particularly because of "removing a page from memory and then immediately needing it again due to a page fault referencing that page").
Virtual Address	Disk address containing the location of a page. The disk address will be translated to a physical main memory address by the CP so the page will be read into the correct main memory location for a particular user.

VS-25/45 MICROINSTRUCTIONS

MNEMONIC	OPCODE	MICROINSTRUCTION ORIENTATED DEFINITION
A	0A	Add (CA in=0; no CA out)
AC	02	Add with Carry
ACM	3C	Add with carry
ACO	06	Add with Carry (CA in = 1)
ACP	0B	Add for Pagespan Check
ACV	07	Add with Carry (Overflow bit set)
ACZ	03	Add with Carry (CA in = 0)
AND	08	Logical AND
ANDI	20	Logical AND Immediate
ANDM	39	Logical AND
BD	37	Generate Base Displacement Address
CCS1	2C	Set CC based on ALU, CA, and S1
CCS2	2D	Set CC directly (from S14 and S15)
CCSET	2E	Set Explicitly (immediate)
CIO	2A	Communication operation (CP - BP)
CSGN	2F	Set CC based on register sign and value
DACM	3E	Decimal add with Carry
DGC	38	Disable ECC generation
DSCM	3F	Decimal subtract with Carry
DSET	2B	Setup for decode
IAD	36	Instruction Address Update
LTRAM	16	Load T-RAM entry (16 bits from MDR)
MMI	30	Move MDR Indirect
MMI+1	31	Move MDR Indirect +1
MMI-1	32	Move MDR Indirect -1
MMR	18	Move MDR
MMR8	1C	Move MDRH
MMS	1A	Move MDR to System Register
MMS8	1E	Move MDRH to System
MRM	19	Move Register
MRM8	1D	Move Register
MSI	33	Move Stack Indirect
MSI+1	35	Move Stack Indirect +1
MSI-1	34	Move Stack Indirect -1
MSM	1B	Move System Register
MSM8	1F	Move System Register
MV	0D	Move
MVI	24	Move Immediate
MVS	0E	Move System Register
MVSI	0F	Move System Register
NANDI	21	AND Immediate (no result)
NOP	27	No operation
NXORI	23	XOR Immediate (no result)
OR	09	Logical OR
ORI	22	Logical OR Immediate
ORM	3A	Logical OR
RTRAN	28	Translate for read address
SC	00	Subtract with Carry (B-A)
SCI	05	Subtract Inverted (A-B)
SCO	01	Subtract with Carry (CA in = 1)
SCOM	3D	Subtract with Carry (CA in=1)

MNEMONIC	OPCODE	MICROINSTRUCTION ORIENTATED DEFINITION
SCV	04	Subtract with Carry (OVF set)
SHL	14	Shift left 1 bit
SHL4	10	Shift left 4 bits
SHL4Z	12	Shift left 4 bits (bits in = 0)
SHR	15	Shift right 1 bit
SHR4	11	Shift right 4 bits
SHRZ4	13	Shift right 4 bits (bits in = 0)
STRAM	17	Store T-RAM entry (16 bits to MDR)
TMAR	25	Transfer MAR
TSTK	26	Transfer Stack pair
WTRAN	29	Translate for write address
XOR	0C	Logical XOR
XORM	3B	Logical exclusive OR

VS-25/45 MICROINSTRUCTION FIELDS

39 BIT MICROINSTRUCTION (CONTROL MEMORY BITS)			
PROCESS FIELD (POP)	MEMORY FIELD (MOP)	BRANCH FIELD (BOP)	
CM0	CM18	CM23	CM38

Process field (CM0-CM17)
1. Microopcode field
2. A-operand field
3. B-operand field

PROCESS FIELD FORMAT			
MICRO-OPCODE	A-OPERAND	B-OPERAND	
CM0	CM6	CM12	CM17

Memory field (CM18-CM22)
1. Memory Address Register (MAR) select
2. Memory operation
3. MAR ripple

MEMORY FIELD FORMAT			
MAR SELECT	MEMORY OPERATION	MAR RIPPLE	
CM18	CM19	CM21	CM22

MEMORY ADDRESS REGISTER (MAR) SELECT FIELD	
CM18	MAR REGISTER SELECTED
0	MAR1
1	MAR2

MEMORY OPERATIONS FIELD		
CM19	CM20	MEMORY OPERATION
0	0	NO OPERATION (NOP)
0	1	READ TWO BYTES
1	0	WRITE TWO BYTES
1	1	WRITE ONE BYTE

VS-25/45 MICROINSTRUCTION FIELDS

MEMORY MAR RIPPLE FIELD		
CM21	CM22	RIPPLE
0	0	RIPPLE +1
0	1	RIPPLE +2
1	0	RIPPLE -1
1	1	NO RIPPLE

Branch field (CM23-CM38)
1. Branch operation field
2. Microaddress (or other operands)

BRANCH FIELD FORMAT 1 - FULL-ADDRESS BRANCH

BRANCH OPCODE	MICRO-ADDRESS (13 BITS)

CM23 CM26 CM38

BRANCH FIELD FORMAT 2 - CONDITIONAL BRANCH

BRANCH OPCODE	STATUS SELECT	MICRO-ADDRESS (6 LOW BITS)

CM23 CM26 CM33 CM38

BRANCH FIELD FORMAT 3 - STATUS BIT MANIPULATION

BRANCH OPCODE	STATUS SELECT A-SELECT	STATUS OPCODE	STATUS BIT B-SELECT

CM23 CM26 CM30 CM33 CM37 CM38

BRANCH FIELD FORMAT 4 - ALIGNMENT TRAP

BRANCH OPCODE		A1	A2	A3

CM23 CM26 CM36 CM37 CM38

STACK ADDRESS	16 BITS WIDE
00 1F	FILE REGISTERS (32)
20 3F	SYSTEM REGISTERS (32)
40 5F	AUXILIARY REGISTERS (32)
60 7F	GENERAL REGISTERS (32)
80 FF	WORK AREA (128)

VS-25/45 Stack Organization and Register Location

REQUEST FOR MEMORY OPERATIONS			
MCB0	MCB1	MCB2	OPERATION
0	0	0	WRITE 8 (LOW BYTE) DISABLE ECC
0	0	1	WRITE 8 (LOW BYTE) ENABLE ECC
0	1	0	READ 16 DISABLE ECC
0	1	1	READ 16 ENABLE ECC
1	0	0	WRITE 16 DISABLE ECC
1	0	1	WRITE 16 ENABLE ECC
1	1	0	WRITE 8 (HIGH BYTE) DISABLE ECC
1	1	1	WRITE 8 (HIGH BYTE) ENABLE ECC

CP commands decoded into following memory instructions
1. Write 8 - Write byte. Write the low order byte of MDR to memory
2. Write 8 - Write byte. Write the high order byte of MDR to memory
3. Write 16 - Write word from MDR
4. Read 16 - Read word into MDR

VS-25/45 CP Memory Operation Decoding (Memory Control)

RESULTS OF MEMORY OPERATIONS		
MSB0	MSB1	STATUS
0	0	OPERATION OK
1	0	INVALID MEMORY ADDRESS
0	1	ECC (PARITY) ERROR
1	1	NOT DEFINED

VS-25/45 CP Memory Status Bits

BIT	NAME	CONDITION
S0	CA	Carry Bit. Carry In/Out for Decimal/Binary Operations.
S1	SPARE	
S2	ALU	0 Or Non-0 result for 8/16 Bit Move or Arithmetic Operations.
S3	PAGE	Set/Reset when MAR Rippled. Carry-out of MAR13. (New Page)
S4	STATE	Protection Checking. Indicates System or User State.
S5	DEC	Set for Invalid Decimal digit found in A or B Bus Operand for Decimal Add/Subtract with Carry.
S6	MSEL	From Trap 0003/0006. MAR in use when Trap taken.
S7	SPARE	
S8	DEBUG	
S9	CM	Control Mode. CP Control Mode button.
S10	IO3	Set by BP. BP has stored I/O Status Word in memory.
S11	TIM	Real-time clock tick. Set from AC line frequency cycle.
S12	OVF	Overflow from 2's compliment arithmetic. From Add with Carry/Subtract with Carry instructions.
S13	IO4	Receive bit IO4B when CIO 0 issued.
S14		From Reset Reference/Change Entry for Reference/Change value.
S15		From Reset Reference/Change Entry for Reference/Change value.

VS-25/45 CPU Status Bits

MAR BIT	MA LINE BIT
MAR 23	MA0
MAR 22	MA1
MAR 21	MA2
MAR 20	MA3
MAR 19	MA4
MAR 18	MA5
MAR 17	MA6
MAR 16	MA7
MAR 15	MA8
MAR 14	MA9
MAR 13	MA10
MAR 12	MA11
MAR 11	MA12
MAR 10	MA13
MAR 9	MA14
MAR 8	MA15
MAR 7	MA16
MAR 6	MA17
MAR 5	MA18
MAR 4	MA19
MAR 3	MA20

VS-25/45 Memory Register Data Bit To Memory Address Line Values

TRAP ADDRESS	TRAP NAME	CONDITION
0003	TRAP03	Translation Trap (T-RAM Fault) (Set Status Register Bit S6)
0004	TRAP04	Protection Trap
0005	INVA	Memory Trap (Invalid Physical Address)
0006	MPAR	Memory Parity Error (Bit S6 set = MAR in use on MPAR trap
0007	TALIGN	Alignment Trap (BOP = TRP ALIGNx)
0008	TBI	Pagespan Trap (Page = 0 when BOP = BI)
0009	TCC	Trap for BOP = TRP CC/MASK

VS-25/45 CP Microtraps

RP	WP	RESULT
0	0	No Protection
0	1	No Write Allowed In User State
1	0	No Read, Write, Or Execute Allowed In User State
1	1	No Write Allowed In System Or User State

VS-25/45 Read/Write Protection Bits

CC SET TO	CONDITIONS
00	If ALU = 0 and Status Bit S1 = 0
01	CARRY bit = 0
10	CARRY bit = 1

CC SET TO	CONDITIONS
00	If ALU = 0 and Status Bit S1 = 0
01	HIGH ORDER BIT = 1
10	HIGH ORDER BIT = 0

VS-25/45 Set Condition Code Bits

IF CC =	THEN TRAP I
00	IREG bit 0 =
01	IREG bit 1 =
10	IREG bit 2 =
11	IREG bit 3 =

VS-25/45 Condition Code Check With Trap

MA BIT	HEX	MEMORY CAPACITY	COMMENT
MA 20	0	1MEG BYTES	MODULE SELECT
MA 19	F	512K BYTES	64K WORD SELECT
MA 18		256K BYTES	64K WORD SELECT
MA 17		128K BYTES	64K WORD SELECT
MA 16		64K BYTES	COLUMN ADDRESS
MA 15	F	32K BYTES	COLUMN ADDRESS
MA 14		16K BYTES	COLUMN ADDRESS
MA 13		8K BYTES	COLUMN ADDRESS
MA 12		4K BYTES	COLUMN ADDRESS
MA 11	F	2K BYTES	COLUMN ADDRESS
MA 10		1K BYTES	COLUMN ADDRESS
MA 9		512 BYTES	COLUMN ADDRESS
MA 8		256 BYTES	ROW ADDRESS
MA 7	F	128 BYTES	ROW ADDRESS
MA 6		64 BYTES	ROW ADDRESS
MA 5		32 BYTES	ROW ADDRESS
MA 4		16 BYTES	ROW ADDRESS
MA 3	F	8 BYTES	ROW ADDRESS
MA 2		4 BYTES	ROW ADDRESS
MA 1		2 BYTES	ROW ADDRESS
MA 0			BYTE SWAP SELECT

VS-25/45 Main Memory Addresses

SW. #	1	2	3	4	MEMORY SIZE
	ON	ON	OFF	OFF	512 KB
	ON	OFF	ON	ON	640 KB
	ON	OFF	ON	OFF	768 KB
	ON	OFF	OFF	ON	896 KB
	ON	OFF	OFF	OFF	1024 KB

Note: Switch #5 is not used and is always OFF.

VS-25/45 Main Memory Size Select Switch

APPENDIX B

APPENDIX B

VS-25/45 SELF-TEST MONITOR DIAGNOSTIC ERROR CODES
(FULL LIST OF 4-DIGIT TEST/ERROR CODE NUMBERS)

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
00	
0000	8086 not running
00E0	Workstation 0 hung on IPL
00E1	Main memory parity error occurred during a code RAM DMA
00E2	Main memory DMA attempted to access a nonexistent address
00E3	BP Data RAM parity error has occurred
00E4	Front panel Bootstrap Media switch in wrong position
00E5	Pascal exception of unknown origin occurred
00E6	Invalid DA type value has been detected
00E7	CP set an illegal command out area code
00E9	Repeated DMA attempts for command out area failed. BP initiates entry into Control Mode
00EA	Repeated DMA attempts for processor interrupt area failed. BP initiates entry into Control Mode
00EB	SIO/CIO raced with EC or NC IOSW (possible OS failure). BP initiates entry into Control Mode
00EC	IRQ/DAR raced with EC or NC IOSW (possible OS failure). BP initiates entry into Control Mode
00ED	Main memory error correction count exceeded it's limit of 1. BP initiates entry into Control Mode
00F4	IPL device returned 'damaged' status (hardware error)
00F5	IPL device was not ready (intervention required)
00F6	BP memory or disk address error while accessing IPL device
01	PROM POWER ON
0100	BP code hung on jump to routine start
0102	BP code hung when wait state generator set
02	PROM CHECKSUM
0201	BP PROM Checksum error
04	I/O Communication Check
0401	BP can't access I/O address 4 (DMAR)
06	INTERRUPT CONTROLLER
0600	BP routine halted, unknown cause
0601	BP 8259 mask not readable on master SI = Mask pattern
0602	BP 8259 mask not readable on slave 4 SI = Mask pattern
0603	BP 8259 mask not readable on slave 3 SI = Mask pattern
0604	BP 8259 mask not readable on slave 2 SI = Mask pattern
0605	BP 8259 mask not readable on slave 1 SI = Mask pattern
08	PROGRAMMABLE INTERVAL TIMER
0800	BP routine halted, unknown cause
0801	BP data miscompare on PIT count read SI = EXP, DI = Rcvd
0802	BP PIT count incorrect
0803	No BP PIT interrupt request
0A	RAM COMMUNICATION CHECK
0A01	BP parity error can't be cleared
0A02	BP RAM address 0 can't be accessed
0A03	BP RAM low-byte parity error can't be forced
0A04	BP RAM high-byte parity error can't be forced
0A05	BP DATA RAM not available BX = DRAM status

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
0C	RAM and PARITY RAM DATA LINE TEST
0C00	BP routine halted, unknown cause
0C01	BP RAM data miscompare
0C02	Unexpected BP PE, address = DS:BX Main RAM data = SI
0C03	BP RAM data miscompare
0C04	Forced BP PE not detected
0E	RAM ADDRESS LINES TEST
0E00	BP routine halted, unknown cause
0E01	BP RAM data miscompare
0E02	Unexpected BP parity error
0E03	BP RAM chip addressing error
0E04	BP parity RAM chip addressing error
0E05	BP RAM bank addressing error
0E06	BP parity RAM bank addressing error
10	RAM INTEGRITY TEST, WORD OPERATIONS
1000	BP routine halted, unknown cause
1001	BP RAM data miscompare, pattern B6DB
1002	Unexpected BP PE, pattern B6DB
1003	BP RAM data miscompare, pattern 6DB6
1004	Forced BP PE low byte not detected
1005	BP RAM data miscompare, pattern 6DB6, 2nd read
12	RAM INTEGRITY TEST, BYTE OPERATIONS
1201	BP RAM data miscompare, pattern 6C, low byte
1202	Unexpected BP PE, pattern 6C, low byte
1203	BP RAM data miscompare, pattern DB, high byte
1204	Forced BP PE not detected, pattern 3, high byte
1205	BP RAM data miscompare, pattern 3, low byte overwritten
1206	BP RAM data miscompare, pattern 3, high byte overwritten
14	RAM BLOCK MOVE OPERATIONS and NOISE SENSITIVITY TEST
1401	BP RAM data miscompare, word string move
1402	BP RAM data miscompare, byte string move
1403	BP RAM data miscompare, '0' in bank of '1's, low address
1404	BP RAM data miscompare, '0' in bank of '1's, high address
20	PARITY ERROR INTERRUPT TEST
2000	BP routine halted, unknown cause
2001	BP CODE RAM PE interrupt not detected
2002	BP DATA RAM PE interrupt not detected
22	WAIT STATE GENERATOR TEST
2200	BP routine halted, unknown cause
2201	BP CODE RAM wait states can't be changed
2202	BP PROM, I/O wait states can't be changed
24	WAIT STATE GENERATOR
2401	Changing PB CODE RAM wait states didn't change CODE RAM access time
2402	Changing PB PROM wait states didn't change PROM access time

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
3C	MEMORY LOOPBACK SELF TEST
3C01	8251, 8251 input line
3C02	8251, C/D or data line, clock, modem
3C03	I/O decode logic, inverter
3C04	8251, modem
3C05	8251
3C06	8251, buffer or modem
3C07	8251, buffer or modem
3C08	8251, buffer or modem
3C09	8251, buffer or modem
3C0A	8251, modem
3C0B	8251
3C0C	8251, modem
3C0D	8251
3C2C	Local/Remote switch or buffer
38	DISKETTE POWER-UP TEST
3801	DMA status register not cleared after Master Clear
3802	Diskette DMA error on write/read pattern of 00000
3803	Diskette DMA error on write/read pattern of 0AAAA
3804	Diskette DMA error on write/read pattern of 05555
3805	Diskette DMA error on write/read pattern of 0FFFF
3806	Diskette Word Count Register error on pattern of 00000
3807	Diskette Word Count Register error on pattern of 0AAAA
3808	Diskette Word Count Register error on pattern of 05555
3809	Diskette Word Count Register error on pattern of 0FFFF
380A	FDC not ready for commands after reset
380B	FDC error on sense drive status command
380C	FDC error on recalibrate command
380D	Not on track 0 after recalibrate command
9820	Diskette drive not ready
9821	Error on seek to track 77
9822	Drive won't recalibrate
3E	Unexpected interrupt handler
3EXX	Unexpected BP interrupt. XX = interrupt type serviced.
3EFF	Unexpected BP interrupt. The interrupt type is unknown.
40	Load Bootstrap file
4000	Hung during Bootstrap operation
4011	SMD media error
4012	SMD drive controller error
4014	SMD drive not ready
4018	SMD program error/media error
401A	SMD disk pack not relabeled via DISKINIT
401C	SMD bad file load/checksum error
4021	Diskette media error
4022	Diskette drive controller error
4024	Diskette drive not ready
4028	Diskette program error/media error
402C	Diskette bad file load/checksum error

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
4031	Quantum media error	
4032	Quantum drive controller error	
4034	Quantum drive not ready	
4038	Quantum program error/media error	
403C	Quantum bad file load/checksum error	
4090	SMD bad volume label read	
4091	SMD media error	
4092	SMD drive controller error	
4094	SMD drive not ready	
4098	SMD program error/media error	
409A	SMD non-bootstrap volume	
409C	SMD bad file load/checksum error	
40A0	Diskette bad volume label read	
40A1	Diskette media error	
40A2	Diskette drive controller error	
40A4	Diskette drive not ready	
40A8	Diskette program error/media error	
40AA	Diskette non-bootstrap volume	
40AC	Diskette bad file load/checksum error	
40B0	Quantum bad volume label read	
40B1	Quantum media error	
40B2	Quantum drive controller error	
40B4	Quantum drive not ready	
40B8	Quantum program error/media error	
40BA	Quantum non-bootstrap volume	
40BC	Quantum bad file load/checksum error	
41	BOOTSTRAP LOADER	
4110	Unlabeled volume (VOL1 missing)	Volume Label
4111	Media error	Volume Label
4112	Controller H/W error	Volume Label
4114	Drive Not Ready	Volume Label
4116	Program error (divide)	Volume Label
4118	Program error (bad data)	Volume Label
4119	Media error	Bit map
411A	Controller H/W error	Bit map
411C	Drive Not Ready	Bit map
411E	Program error (divide)	Bit map
4120	Program error (bad data)	Bit map
4121	Media error	VTOC
4122	Controller H/W error	VTOC
4124	Drive Not Ready	VTOC
4126	Program error (divide)	VTOC
4128	Program error (bad data)	VTOC
412A	FDX1 ID doesn't match	VTOC
412B	FDX2 ID doesn't match	VTOC
412C	FDR1 ID doesn't match	VTOC

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
4131	Media error	Self Test Mon
4132	Controller H/W error	Self Test Mon
4133	Checksum doesn't match	Self Test Mon
4134	Drive Not Ready	Self Test Mon
4136	Program error (divide)	Self Test Mon
4138	Program error (bad data)	Self Test Mon
413A	Library not found	Self Test Mon
413B	File not found	Self Test Mon
413C	FDR1 not found	Self Test Mon
413E	Extents greater than 3	Self Test Mon
4141	Media error	Diagnostic Monitor
4142	Controller H/W error	Diagnostic Monitor
4143	Checksum doesn't match	Diagnostic Monitor
4144	Drive Not Ready	Diagnostic Monitor
4146	Program error (divide)	Diagnostic Monitor
4148	Program error (bad data)	Diagnostic Monitor
414A	Library not found	Diagnostic Monitor
414B	File not found	Diagnostic Monitor
414C	FDR1 not found	Diagnostic Monitor
414E	Extents greater than 3	Diagnostic Monitor
4151	Media error	System Loader
4152	Controller H/W error	System Loader
4153	Checksum doesn't match	System Loader
4154	Drive Not Ready	System Loader
4156	Program error (divide)	System Loader
4158	Program error (bad data)	System Loader
415A	Library not found	System Loader
415B	File not found	System Loader
415C	FDR1 not found	System Loader
415E	Extents greater than 3	System Loader
41E0	Diskette status error	
41F0	Invalid H/W configuration	
41FD	BP CODE RAM parity error	
41FE	BP DATA RAM parity error	
41FF	Unknown interrupt on the BP	
42	SELF TEST MONITOR	
4210	Unlabeled volume (VOL1 missing)	Volume Label
4211	Media error	Volume Label
4212	Controller H/W error	Volume Label
4214	Drive Not Ready	Volume Label
4216	Program error (divide)	Volume Label
4218	Program error (bad data)	Volume Label
4219	Media error	Bit map
421A	Controller H/W error	Bit map
421C	Drive Not Ready	Bit map
421E	Program error (divide)	Bit map
4220	Program error (bad data)	Bit map
4221	Media error	VTOC
4222	Controller H/W error	VTOC

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
4224	Drive Not Ready	VTOC
4226	Program error (divide)	VTOC
4228	Program error (bad data)	VTOC
422A	FDX1 ID doesn't match	VTOC
422B	FDX2 ID doesn't match	VTOC
422C	FDR1 ID doesn't match	VTOC
4231	Media error	W. S. File
4232	Controller H/W error	W. S. File
4233	Checksum doesn't match	W. S. File
4234	Drive Not Ready	W. S. File
4236	Program error (divide)	W. S. File
4238	Program error (bad data)	W. S. File
423A	Library not found	W. S. File
423B	File not found	W. S. File
423C	FDR1 not found	W. S. File
423E	Extents greater than 3	W. S. File
4241	Media error	@ST0500@ in @DIAGST@
4242	Controller H/W error	@ST0500@ in @DIAGST@
4243	Checksum doesn't match	@ST0500@ in @DIAGST@
4244	Drive Not Ready	@ST0500@ in @DIAGST@
4246	Program error (divide)	@ST0500@ in @DIAGST@
4248	Program error (bad data)	@ST0500@ in @DIAGST@
424A	Library not found	@ST0500@ in @DIAGST@
424B	File not found	@ST0500@ in @DIAGST@
424C	FDR1 not found	@ST0500@ in @DIAGST@
424E	Extents greater than 3	@ST0500@ in @DIAGST@
4251	Media error	@BT0500@ in @DIAGST@
4252	Controller H/W error	@BT0500@ in @DIAGST@
4253	Checksum doesn't match	@BT0500@ in @DIAGST@
4254	Drive Not Ready	@BT0500@ in @DIAGST@
4256	Program error (divide)	@BT0500@ in @DIAGST@
4258	Program error (bad data)	@BT0500@ in @DIAGST@
425A	Library not found	@BT0500@ in @DIAGST@
425B	File not found	@BT0500@ in @DIAGST@
425C	FDR1 not found	@BT0500@ in @DIAGST@
425E	Extents greater than 3	@BT0500@ in @DIAGST@
4261	Media error	@CT0500@ in @DIAGST@
4262	Controller H/W error	@CT0500@ in @DIAGST@
4263	Checksum doesn't match	@CT0500@ in @DIAGST@
4264	Drive Not Ready	@CT0500@ in @DIAGST@
4266	Program error (divide)	@CT0500@ in @DIAGST@
4268	Program error (bad data)	@CT0500@ in @DIAGST@
426A	Library not found	@CT0500@ in @DIAGST@
426B	File not found	@CT0500@ in @DIAGST@
426C	FDR1 not found	@CT0500@ in @DIAGST@
426E	Extents greater than 3	@CT0500@ in @DIAGST@
4271	Media error	@CT0800@ in @DIAGST@
4272	Controller H/W error	@CT0800@ in @DIAGST@
4273	Checksum doesn't match	@CT0800@ in @DIAGST@

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
4274	Drive Not Ready	@CT0800@ in @DIAGST@
4276	Program error (divide)	@CT0800@ in @DIAGST@
4278	Program error (bad data)	@CT0800@ in @DIAGST@
427A	Library not found	@CT0800@ in @DIAGST@
427B	File not found	@CT0800@ in @DIAGST@
427C	FDR1 not found	@CT0800@ in @DIAGST@
427E	Extents greater than 3	@CT0800@ in @DIAGST@
4281	Media error	@CTOB00@ in @DIAGST@
4282	Controller H/W error	@CTOB00@ in @DIAGST@
4283	Checksum doesn't match	@CTOB00@ in @DIAGST@
4284	Drive Not Ready	@CTOB00@ in @DIAGST@
4286	Program error (divide)	@CTOB00@ in @DIAGST@
4288	Program error (bad data)	@CTOB00@ in @DIAGST@
428A	Library not found	@CTOB00@ in @DIAGST@
428B	File not found	@CTOB00@ in @DIAGST@
428C	FDR1 not found	@CTOB00@ in @DIAGST@
428E	Extents greater than 3	@CTOB00@ in @DIAGST@
4291	Media error	@MT0500@ in @DIAGST@
4292	Controller H/W error	@MT0500@ in @DIAGST@
4293	Checksum doesn't match	@MT0500@ in @DIAGST@
4294	Drive Not Ready	@MT0500@ in @DIAGST@
4296	Program error (divide)	@MT0500@ in @DIAGST@
4298	Program error (bad data)	@MT0500@ in @DIAGST@
429A	Library not found	@MT0500@ in @DIAGST@
429B	File not found	@MT0500@ in @DIAGST@
429C	FDR1 not found	@MT0500@ in @DIAGST@
429E	Extents greater than 3	@MT0500@ in @DIAGST@
42A1	Media error	@BT0800@ in @DIAGST@
42A2	Controller H/W error	@BT0800@ in @DIAGST@
42A3	Checksum doesn't match	@BT0800@ in @DIAGST@
42A4	Drive Not Ready	@BT0800@ in @DIAGST@
42A6	Program error (divide)	@BT0800@ in @DIAGST@
42A8	Program error (bad data)	@BT0800@ in @DIAGST@
42AA	Library not found	@BT0800@ in @DIAGST@
42AB	File not found	@BT0800@ in @DIAGST@
42AC	FDR1 not found	@BT0800@ in @DIAGST@
42AE	Extents greater than 3	@BT0800@ in @DIAGST@
42E2	SIO timeout	
42E3	SIO failure	
42E4	SIO overrun	
42E5	SIO DATA RAM parity error	
42E6	SIO serial parity error	
42E7	Workstation powered off	
42E8	Workstation coaxial parity error	
42E9	Workstation memory parity error	
42EA	Workstation has no code	
42EB	Workstation invalid status	
42E0	Diskette status error	
42F0	Invalid hardware configuration	

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
43	SELF TEST MONITOR	
4371	Media error	Overlay @CM0800@
4372	Controller H/W error	Overlay @CM0800@
4373	Checksum doesn't match	Overlay @CM0800@
4374	Drive Not Ready	Overlay @CM0800@
4376	Program error (divide)	Overlay @CM0800@
4378	Program error (bad data)	Overlay @CM0800@
437A	Library not found	Overlay @CM0800@
437B	File not found	Overlay @CM0800@
437C	FDR1 not found	Overlay @CM0800@
437E	Extents greater than 3	Overlay @CM0800@
4381	Media error	Overlay @CM0B00@
4382	Controller H/W error	Overlay @CM0B00@
4383	Checksum doesn't match	Overlay @CM0B00@
4384	Drive Not Ready	Overlay @CM0B00@
4386	Program error (divide)	Overlay @CM0B00@
4388	Program error (bad data)	Overlay @CM0B00@
438A	Library not found	Overlay @CM0B00@
438B	File not found	Overlay @CM0B00@
438C	FDR1 not found	Overlay @CM0B00@
438E	Extents greater than 3	Overlay @CM0B00@
4391	Media error	Overlay @MM0500@
4392	Controller H/W error	Overlay @MM0500@
4393	Checksum doesn't match	Overlay @MM0500@
4394	Drive Not Ready	Overlay @MM0500@
4396	Program error (divide)	Overlay @MM0500@
4398	Program error (bad data)	Overlay @MM0500@
439A	Library not found	Overlay @MM0500@
439B	File not found	Overlay @MM0500@
439C	FDR1 not found	Overlay @MM0500@
439E	Extents greater than 3	Overlay @MM0500@
44	SYSTEM LOADER	
4410	Unlabeled volume (VOL1 missing)	Volume Label
4411	Media error	Volume Label
4412	Controller H/W error	Volume Label
4414	Drive Not Ready	Volume Label
4416	Program error (divide)	Volume Label
4418	Program error (bad data)	Volume Label
4419	Media error	Bit map
441A	Controller H/W error	Bit map
441C	Drive Not Ready	Bit map
441E	Program error (divide)	Bit map
4420	Program error (bad data)	Bit map
4421	Media error	VTOC
4422	Controller H/W error	VTOC
4424	Drive Not Ready	VTOC
4426	Program error (divide)	VTOC
4428	Program error (bad data)	VTOC
442A	FDX1 ID doesn't match	VTOC

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
442B	FDX2 ID doesn't match	VTOC
442C	FDR1 ID doesn't match	VTOC
4431	Media error	W. S. 0 File
4432	Controller H/W error	W. S. 0 File
4433	Checksum doesn't match	W. S. 0 File
4434	Drive Not Ready	W. S. 0 File
4436	Program error (divide)	W. S. 0 File
4438	Program error (bad data)	W. S. 0 File
443A	Library not found	W. S. 0 File
443B	File not found	W. S. 0 File
443C	FDR1 not found	W. S. 0 File
443E	Extents greater than 3	W. S. 0 File
4441	Media error	B. P. File
4442	Controller H/W error	B. P. File
4443	Checksum doesn't match	B. P. File
4444	Drive Not Ready	B. P. File
4446	Program error (divide)	B. P. File
4448	Program error (bad data)	B. P. File
444A	Library not found	B. P. File
444B	File not found	B. P. File
444C	FDR1 not found	B. P. File
444E	Extents greater than 3	B. P. File
4451	Media error	C. M. File
4452	Controller H/W error	C. M. File
4453	Checksum doesn't match	C. M. File
4454	Drive Not Ready	C. M. File
4456	Program error (divide)	C. M. File
4458	Program error (bad data)	C. M. File
445A	Library not found	C. M. File
445B	File not found	C. M. File
445C	FDR1 not found	C. M. File
445E	Extents greater than 3	C. M. File
4461	Media error	CP uCode File
4462	Controller H/W error	CP uCode File
4463	Checksum doesn't match	CP uCode File
4464	Drive Not Ready	CP uCode File
4466	Program error (divide)	CP uCode File
4468	Program error (bad data)	CP uCode File
446A	Library not found	CP uCode File
446B	File not found	CP uCode File
446C	FDR1 not found	CP uCode File
446E	Extents greater than 3	CP uCode File
44E0	DMA timeout	
44E1	DMA failure	
44E2	SIO timeout	
44E3	SIO failure	
44E4	SIO overrun	
44E5	SIO DATA RAM parity error	
44E6	SIO serial parity error	

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
44E7	Workstation powered off	
44E8	Workstation coaxial parity error	
44E9	Workstation memory parity error	
44EA	Workstation has no code	
44EB	Workstation invalid status	
44EC	CPU failure	
45	DIAGNOSTIC MONITOR	
4510	Unlabeled volume (VOL1 missing)	Volume Label
4511	Media error	Volume Label
4512	Controller H/W error	Volume Label
4514	Drive Not Ready	Volume Label
4516	Program error (divide)	Volume Label
4518	Program error (bad data)	Volume Label
4519	Media error	Bit map
451A	Controller H/W error	Bit map
451C	Drive Not Ready	Bit map
451E	Program error (divide)	Bit map
4520	Program error (bad data)	Bit map
4521	Media error	VTOC
4522	Controller H/W error	VTOC
4524	Drive Not Ready	VTOC
4526	Program error (divide)	VTOC
4528	Program error (bad data)	VTOC
452A	FDX1 ID doesn't match	VTOC
452B	FDX2 ID doesn't match	VTOC
452C	FDR1 ID doesn't match	VTOC
4531	Media error	W. S. 0 File
4532	Controller H/W error	W. S. 0 File
4533	Checksum doesn't match	W. S. 0 File
4534	Drive Not Ready	W. S. 0 File
4536	Program error (divide)	W. S. 0 File
4538	Program error (bad data)	W. S. 0 File
453A	Library not found	W. S. 0 File
453B	File not found	W. S. 0 File
453C	FDR1 not found	W. S. 0 File
453E	Extents greater than 3	W. S. 0 File
4541	Media error	Test Table File
4542	Controller H/W error	Test Table File
4543	Checksum doesn't match	Test Table File
4544	Drive Not Ready	Test Table File
4546	Program error (divide)	Test Table File
4548	Program error (bad data)	Test Table File
454A	Library not found	Test Table File
454B	File not found	Test Table File
454C	FDR1 not found	Test Table File
454E	Extents greater than 3	Test Table File
45E0	DMA timeout	
45E1	DMA failure	

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION	
45E2	SIO failure	
45E3	SIO timeout	
45E4	W.S. failure	
45E5	W.S. failed start	
45E6	W.S. failed load	
45E7	W.S. failed restart	
45E8	Invalid burn-in table	
46	DIAGNOSTIC MONITOR	
46X1	Media error	Test File X
46X2	Controller H/W error	Test File X
46X3	Checksum doesn't match	Test File X
46X4	Drive Not Ready	Test File X
46X6	Program error (divide)	Test File X
46X8	Program error (bad data)	Test File X
46XA	Library not found	Test File X
46XB	File not found	Test File X
46XC	FDR1 not found	Test File X
46XE	Extents greater than 3	Test File X
47	DIAGNOSTIC MONITOR	
47X1	Media error	File X + 15
47X2	Controller H/W error	File X + 15
47X3	Checksum doesn't match	File X + 15
47X4	Drive Not Ready	File X + 15
47X6	Program error (divide)	File X + 15
47X8	Program error (bad data)	File X + 15
47XA	Library not found	File X + 15
47XB	File not found	File X + 15
47XC	FDR1 not found	File X + 15
47XE	Extents greater than 3	File X + 15
48	DIAGNOSTIC MONITOR	
48X1	Media error	Overlay X
48X2	Controller H/W error	Overlay X
48X3	Checksum doesn't match	Overlay X
48X4	Drive Not Ready	Overlay X
48X6	Program error (divide)	Overlay X
48X8	Program error (bad data)	Overlay X
48XA	Library not found	Overlay X
48XB	File not found	Overlay X
48XC	FDR1 not found	Overlay X
48XE	Extents greater than 3	Overlay X
49	DIAGNOSTIC MONITOR	
49X1	Media error	Overlay X + 15
49X2	Controller H/W error	Overlay X + 15
49X3	Checksum doesn't match	Overlay X + 15
49X4	Drive Not Ready	Overlay X + 15
49X6	Program error (divide)	Overlay X + 15
49X8	Program error (bad data)	Overlay X + 15
49XA	Library not found	Overlay X + 15
49XB	File not found	Overlay X + 15
49XC	FDR1 not found	Overlay X + 15

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
49XE	Extents greater than 3 Overlay X + 15
4B	CPU memory self test @CT0500@
4B00	CPU failed self test. Run CPU diagnostics
4B01	CPU instruction counter can't be set to zero
4B02	Data error on write/read of control memory
4B03	Data error on read/write/read sequence of control memory
4B04	CPU hardware status register error. Bit2 not reset after setting CPU into 'STEP' mode.
4B05	CPU hardware status register error. Bit2 not set after setting CPU into 'RUN' mode.
4B06	CPU hardware status register error. Bit2 not reset after setting CPU into 'STEP' mode after 'RUN' mode.
4B07	CPU hardware status register error. Bit3 not reset after disabling CPU address comparator.
4B08	CPU hardware status register error. Bit3 not set after enabling CPU address comparator.
4B09	CPU hardware status register error. Bit4 not set after enabling CPU address comparator and setting compare address equal to MIC.
4B0A	CPU hardware status register error. Bit4 not reset after enabling CPU address comparator and setting compare compare address not equal to MIC.
4B0B	CPU hardware status register error. Bit3, 4, or 5 not reset after disabling CPU address comparator.
4B0C	CPU hardware status register error. Bit3, 4, or 5 not reset after disabling CPU address comparator, with compare address set equal to MIC.
4B0D	CPU hardware status register error. Bit3, or 4 not set after enabling CPU address comparator, with compare address set equal to MIC.
4B0E	Sync interrupt not detected
4B0F	CPU hardware status register error. Bit3, or 4 not reset after disabling CPU address comparator, with compare address set equal to MIC.
4B10	CPU hardware status register error. CPU 'CIO 7' status bit set after execution of a NOP instruction.
4B11	CPU 'HALTED' interrupt not detected on a step in 'STEP' mode.
4B12	CPU hardware status register error. CPU 'CIO 7' status bit not set after execution of a CIO 7 instruction.
4B13	CPU 'HALTED' interrupt not detected when a CIO 7 instruction executed.
4B14	CPU hardware status register error. CPU 'CIO 7' status bit not reset after execution of a NOP instruction.
4B15	CPU 'HALTED' interrupt not detected when a NOP instruction executed.
4B16	CPU 'SYNC' interrupt not detected.
4B17	CPU hardware status register error. Bit7 not set or Bit3 not reset after setting 'NANO STEP' mode.
4B18	Incorrect MIC after executing ENABLE IO3.
4B19	Incorrect MIC after executing CLEAR IO3.
4B1A	CPU IO3 status bit not cleared by CLEAR IO3 Instruction.
4B1B	BP IO3 status bit not set by CLEAR IO3 Instruction.

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
4B1C	Incorrect MIC after executing CLEAR IO4 instruction.
4B1D	CPU IO4 bit not cleared by CLEAR IO4 instruction.
4B1E	Incorrect MIC after executing CLEAR IO4b instruction.
4B1F	BP IO4b status bit not set after executing CLEAR IO4b instruction.
4B20	Incorrect MIC after executing MOVE IO4b to IO4.
4B21	CPU IO4 status bit not clear after moving IO4b to IO4.
4B22	Incorrect MIC after executing MOVE IO4b to IO4.
4B23	BP IO3 status bit not reset after SET IO3 instruction.
4B24	BP IO4b status bit not reset after SET IO4b instruction.
4B25	CPU IO4 not set after SET IO4b, and MOVE IO4b TO IO4 instruction executed.
4B26	CPU IO3 status bit not set after SET IO3 instruction executed.
4B27	Incorrect MIC after CLEAR IO3 instruction executed.
4B28	CPU IO3 status bit not reset after CLEAR IO3 instruction executed.
4B29	BP IO3 status bit not set after executing CLEAR IO3 instruction.
4B2A	IO3 interrupt not detected when IO3 cleared.
4B2B	Incorrect MIC after executing CLEAR IO4b instruction.
4B2C	BP IO4b status bit not set after executing CLEAR IO4b instruction.
4B2D	IO4b interrupt not detected when IO4b cleared.
4B2E	Incorrect MIC after executing CLEAR IO4b instruction.
4B2F	CPU IO4 status bit cleared after executing CLEAR IO4b instruction.
4B30	Incorrect MIC after executing DISABLE IO3.
4B31	CPU IO3 status bit not clear when setting IO3 after disabling IO3.
4B32	Incorrect MIC after executing ENABLE IO3.
4B33	CPU IO3 bit not set after enabling IO3.
4B34	CPU NANO code error.
4C	CPU operational self test @CT0800@
4C00	CPU failed self test, run CPU diagnostics
4C10	Time out
4C20	CPU detected error
4D	CPU integrity self test @CT0B00@
4D00	CPU failed self test, run CPU diagnostics
4D10	Time out
4D20	CPU detected error
4E	Main memory self test @MT0500@
4E00	Main memory failure, run main memory diagnostics
4E10	Time out
4E20	CPU detected main memory error
4F	BP DMA self test @BT0800@
4F00	BP DMA failure, run BP DMA diagnostics
4F10	Time out
4F20	DMA error

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
60	Quantum self test
A810	No Quantum ID on system
9522	Quantum not ready timeout
6014	Quantum recalibrate seek complete 0 interrupt timeout
6016	Quantum stepper seek complete 0 interrupt timeout
6118	Quantum track 0 status missing
62	Quantum read routine, 2 sectors
6202	No Quantum ID on system
6204	Quantum drive 0 not ready
6206	Quantum seek complete 0 interrupt timeout
6208	Quantum programming error, # of blocks too big
620A	Quantum read completion interrupt timeout
620C	Quantum DA status error
62D0	Quantum programming error, block # too big
62E0	Quantum attempt error correction interrupt timeout
62E1	Quantum ECC done status bit missing
62F0	Quantum seek complete 0 interrupt timeout on recalibrate
62F1	Quantum track 0 status missing after recalibrate
63	Quantum read routine, 9 sectors
6302	No Quantum ID on system
6304	Quantum drive 0 not ready
6306	Quantum seek complete 0 interrupt timeout
6308	Quantum programming error, # of blocks too big
630A	Quantum read completion interrupt timeout
630C	Quantum DA status error
63D0	Quantum programming error, block # too big
63E0	Quantum attempt error correction interrupt timeout
63E1	Quantum ECC done status bit missing
63F0	Quantum seek complete 0 interrupt timeout on recalibrate
63F1	Quantum track 0 status missing after recalibrate
71	SIO address latch
7101	Address latch failure
71FD	Unexpected interrupt
71FE	Unexpected SIO interrupt
72	SIO write/read byte
7201	Write byte completion interrupt failure
7202	Read byte completion interrupt failure
7203	Data compare error
7204	Status error
7205	SMAR ripple failure
72FD	Unexpected interrupt
72FE	Unexpected SIO interrupt
72FF	Get control of workstation failure
73	SIO write/read 256
7301	Write 256 completion interrupt failure
7302	Read 256 completion interrupt failure
7303	Data compare error
7304	Status error
7305	SMAR ripple failure

TEST/EC#	TEST TITLE/ERROR CODE DESCRIPTION
73FD	Unexpected interrupt
73FE	Unexpected SIO interrupt
73FF	Get control of workstation failure
76	SIO give status
7601	Give status completion interrupt failure
7602	Data compare error
7603	Status error
76FD	Unexpected interrupt
76FE	Unexpected SIO interrupt
76FF	Get control of workstation failure
90	SIO give status
9011	Workstation powered off status
9015	Coaxial parity, parity, or not running status
90FD	Unexpected interrupt
90FE	Unexpected SIO interrupt
A4	SIO ID test
A401	Device ID not found
A4	SIO SMAR test
A402	SMAR register failure
A4FD	Unexpected interrupt
A4FE	Unexpected SIO interrupt
B0	SMD,CMD, and FMD Device Adapter
B004	Ready status bit failed to set
B012	SMD DA not found on the system
B014	SMD DA port specified doas not exist
B016	SMD DA at an illegal address (0400H, 0500H, or 0600H)
B022	SMD DA could not be properly reset
B032	Disk drive could not be selected
B034	Drive fault could not be cleared
B042	Seek interrupt not detected after a restore (BTZ) operation
B048	Seek interrupt not detected after a seek to track operation
B052	ECC error could not be detected
B062	Operation complete interrupt not detected after a read operation
B068	Operation complete interrupt not detected after an ECC correction operation
B082	Drive status error after restore (RTZ) operation
B084	Drive status error after seek operation
B086	Drive status error after read operation
B092	Read sector operation failed (HCE)
DE	
DEAD	Program trap for execution from nonexistent memory space

APPENDIX C

APPENDIX C

NEC DISK DRIVE

1. INTRODUCTION

The VS-25/45 product line offers an optional 76 Megabyte (formatted) NEC model D2246 Winchester disk drive. One NEC drive can replace one or two VS-25/45 system Quantum drives. The NEC drive can be ordered for new VS-25/45 systems or as an upgrade kit for existing systems. This PUB gives instructions for installing an upgrade kit and Coldstarting the system.

Operation of the NEC drive requires a 256K-byte Bus Processor (210-8403-1A with revision 3 EPROMs), the Intelligent Serial I/O Adapter (210-8616-A), the 25V50-1 (1-port) SMD Device Adapter (210-8312-A), - all supplied with the upgrade kit - and VS Operating System 6.20 or higher.

The NEC drive uses dc power from the existing VS-25/45 SPS450 Switching Power Supply, but the 210-8011 Multi-Output Control board in the P/S must be at E-Revision level 1 or higher. The revision level may or may not be shown on a sticker affixed to the power supply. If the revision level is not shown, or is lower than E-Revision 1, refer to FCO 1068 and ECO 29327.

Basically the procedure involves removing the old 128K-byte Bus Processor (if this type of BP is installed in the system) and installing a new 256K-byte Bus Processor; removing the Serial I/O adapter and installing the Intelligent Serial I/O Adapter; removing the Quantum Device Adapter and the Quantum Disk Drive; and installing the 25V50-0 SMD Device Adapter and the NEC disk drive.

NOTE

The NEC disk drive will be repaired by replacing individual printed circuit board assemblies. (Refer to figure C-22 and the NEC Disk Drive Maintenance Manual, WLI P/N 729-1452.) Do not order or replace the complete disk drive.

a. Related Documents

DOCUMENT TITLE	WLI PART NUMBER
FCO #1068/ECO #29327	
NEC Disk Drive Maintenance Manual	729-1452
VS-25/45 Product Maintenance Manual	729-1032-B
VS-25/45 Schematics Manual	729-1185-A
VS 25 Bulletin	800-3108-02
VS Software Bulletin - Release 6.20	800-3114-01

b. VS-25/45 Upgrade Kits

MODEL #	WLI P/N	DESCRIPTION
UJ-3246	205/206-3246	Upgrade from VS-45X to VS-45N
UJ-3247	205/206-3247	Upgrade from VS-25/45A to VS-25/45N
UJ-3248	205/206-3248	Upgrade from VS-25/45C to VS-25/45N

Part number prefix 205 = International systems.
Part number prefix 206 = Domestic systems.

c. Contents of Upgrade Kit

PART NUMBER	QUANTITY	DESCRIPTION	COMMENTS
210-8304-1A	1	256K-byte Bus Processor	Rev 3 EPROMS
210-8312-A	1	SMD device adapter	25V50-0 (1-port)
210-8616-A	1	Intelligent SIO adapter	
220-2059	1	Dc power cable	
220-3331	1	B disk drive cable	
220-3332	1	A disk drive cable	
278-4032	1	NEC disk drive	Tested
452-0308	1	NEC drive mounting plate	
650-4080	4	Screw	
650-9082	2	Shoulder screw	

d. Other Hardware Requirements

PART NUMBER	QUANTITY	DESCRIPTION	COMMENTS
210-8011	1	Multi-Output Control PCB (SPS450 P/S)	E-Revision 1 or higher

e. Software Requirements

The 6.20 Operating System Coldstart package contains diskettes and documentation. The part numbers of the package and the individual diskettes are not yet available.

SOFTWARE DESCRIPTION	VERSION	COMMENTS	WLI P/N
Format	6.20		735-XXXX
SYST01	6.20		735-XXXX
SYST02	6.20		735-XXXX
SYST03	6.20		735-XXXX
SYST04	6.20		735-XXXX
SYST05	6.20		735-XXXX
UTLTY3	6.20		735-XXXX
MACLIB	6.20		735-XXXX
WSCODE	6.20		735-XXXX
PRCODE	6.20		735-XXXX
NVRAM Utilities		Load/Show NVRAM	735-XXXX
UTLTY1	6.20		735-XXXX
UTLTY2	6.20		735-XXXX

2. VS-25/45 CONFIGURATIONS

MODEL #	SERIAL TAG #	MEMORY SIZE	MAIN MEMORY P/N
VS25-8AN	157/177-7243	512Kb	210-7900-3A
VS25-12AN	157/177-7244	768Kb	210-7900-4A
VS25-16AN	157/177-7245	1024Kb	210-7900-5A
VS45-8AN	157/177-7246	512Kb	210-7900-3A
VS45-12AN	157/177-7247	768Kb	210-7900-4A
VS45-16AN	157/177-7248	1024Kb	210-7900-5A

NOTE

The N in the model number, such as VS25-8AN, designates a VS25-A with an NEC drive installed.

Table C-1. VS-25/45N CPU Configurations

MODEL	MEMORY SIZE	DISK DRIVE(S)	SERIAL PORTS
VS25-8AN	512K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS25-12AN	768K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS25-16AN	1024K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	16
VS45-8AN	512K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32
VS45-12AN	768K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32
VS45-16AN	1024K bytes	25V50 Disk DA 76 Megabyte Fixed Disk Model 2270V-4 DSDD Disk	32

3. NEC MODEL D2246 PRODUCT SPECIFICATIONS

Formatted Storage Capacity	Per Unit (Megabyte) 76 Per Cylinder (Byte) 109,826 Per Track (Byte) 18,304
Number of Disks	4
Number of Cylinders	692
Number of Data Heads	6
Number of Servo Heads	1
Sectors Per Track	9
Recording Mode	Modified Frequency Modulation (MFM)
Interface Mode	Nonreturn To Zero (NRZ)
Data Transfer Rate	1,198K Bytes/Sec.
Power Dissipation	100 Watts (running) 150 Watts (peak starting for 20 seconds)
Heat Generation	340 BTU/Hour (86 Kcal/Hour) - running

4. VOLTAGE CHECKS AND ADJUSTMENTS

NOTE

Before beginning installation of the NEC drive, make sure to run the BACKUP utility to copy all the customer's files to diskettes.

CAUTION

Dc voltages within the specified operating limits, given in table C-2, are critical to the operation of the NEC drive. Perform the following voltage checks/adjustments before installing the NEC drive.

a. Remove the main frame top and front covers.
b. Using a digital voltmeter, check the voltages at the Motherboard test points (figures C-1 and C-2), except for the +24 Volts which should be measured at J5, pin 1 of the Floppy disk drive (figure C-3). If the voltages are within operating limits, proceed to paragraph 5, 210-8304 BP Board Removal and Replacement. If the dc voltages are not within operating limits, the switching power supply must be adjusted. The power supply must be removed from the main frame to make the adjustments.

Table C-2. DC Voltage Limits

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+12.0	+11.4V to +12.6V	35mV RMS or 50mV Pk-to-Pk
-12.0	-11.5V to -12.5V	35mV RMS or 50mV Pk-to-Pk
+5.0	+4.75V to +5.25V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.75V to -5.25V	35mV RMS or 50mV Pk-to-Pk
IV (+12.0)	+11.4V to +12.6V	35mV RMS or 50mV Pk-to-Pk
+24.0	+21.6V to +26.4V	35mV RMS or 50mV Pk-to-Pk

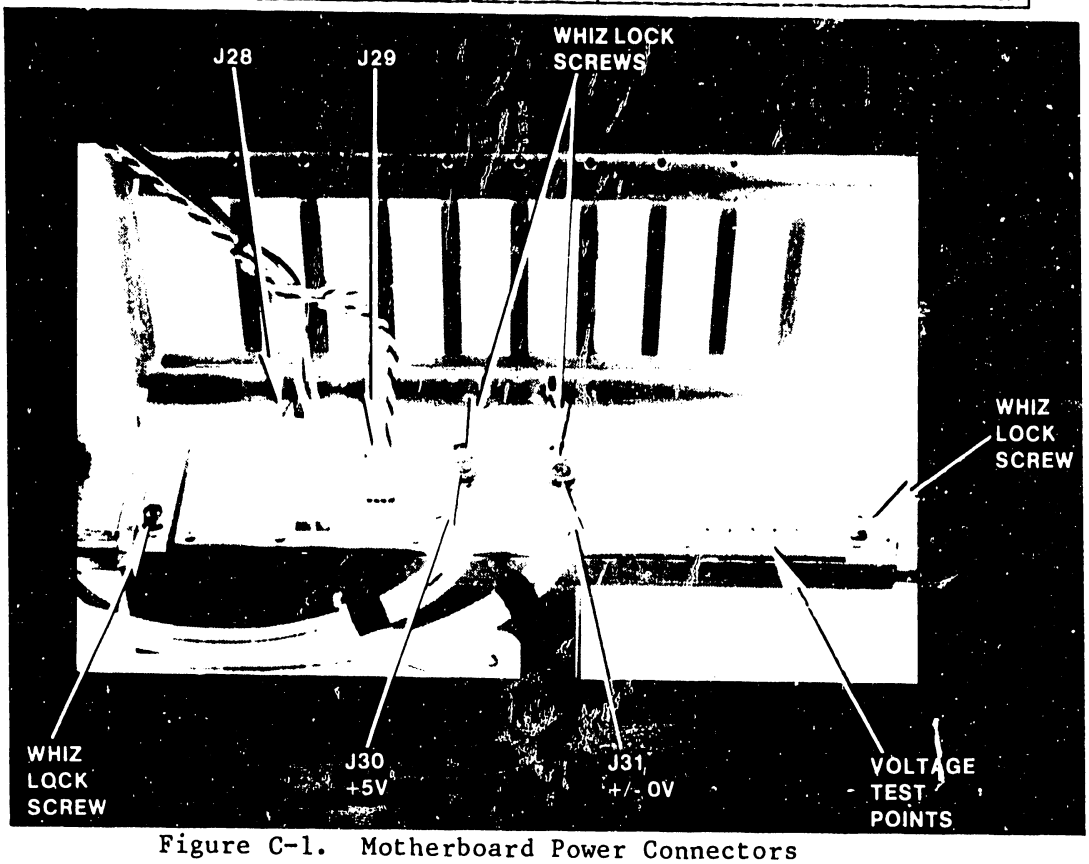


Figure C-1. Motherboard Power Connectors

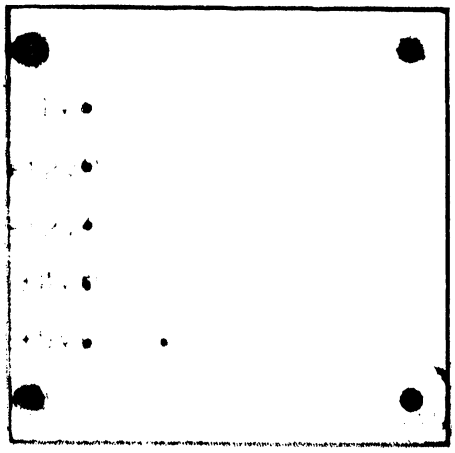


Figure C-2. Motherboard Voltage Test Points

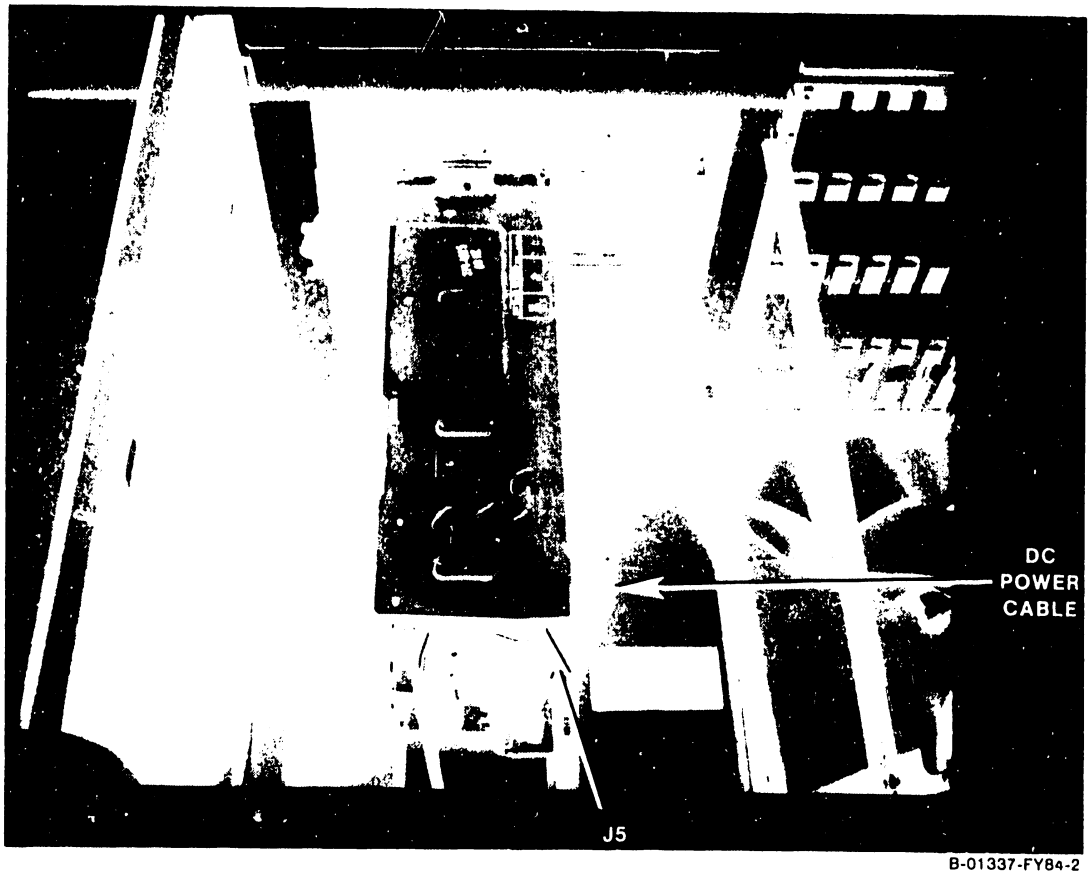


Figure C-3. Diskette Drive

c. To remove the Switching Power Supply and adjust the voltages:

WARNING

```
**************************************************************
*                                                            *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY        *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND          *
*     CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN       *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.   *
*                                                            *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER            *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                   *
*                                                            *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC   *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,       *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO    *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO       *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                    *
*                                                            *
**************************************************************
```

1. Press the green Control Mode button on the VS-25/45 Front Panel. This prevents any disk I/O command in process from being halted prior to completion.
2. Power down the main frame by depressing the ac power On/Off switch to the 0 position and unplug the power connector from the power source receptacle.
3. Remove the single 5/16" hex bolt located directly under the front edge of the supply.
4. Carefully slide the supply far enough out of the main frame to expose the rear of the supply and allow access to the adjustment pots. (There is a piece of foam sound insulating material to the right of the supply. Be careful not to tear the foam when removing and installing the supply.)
5. Plug the main frame power connector into the power source receptacle and depress the ac power On/Off switch to the 1 position.
6. Wait 5 seconds after ac power is applied and then press the DC Initialize pushbutton.
7. With a nonmetallic adjustment tool, adjust the voltage(s) to within the operating limits and reinstall the power supply. (See figures C-4 and C-5 for the locations of the adjustment pots.)
8. After the voltages have been adjusted, power down the system and reinstall the power supply. Leave the system powered off and proceed to paragraph 5, 210-8304 BP Board Removal and Replacement.

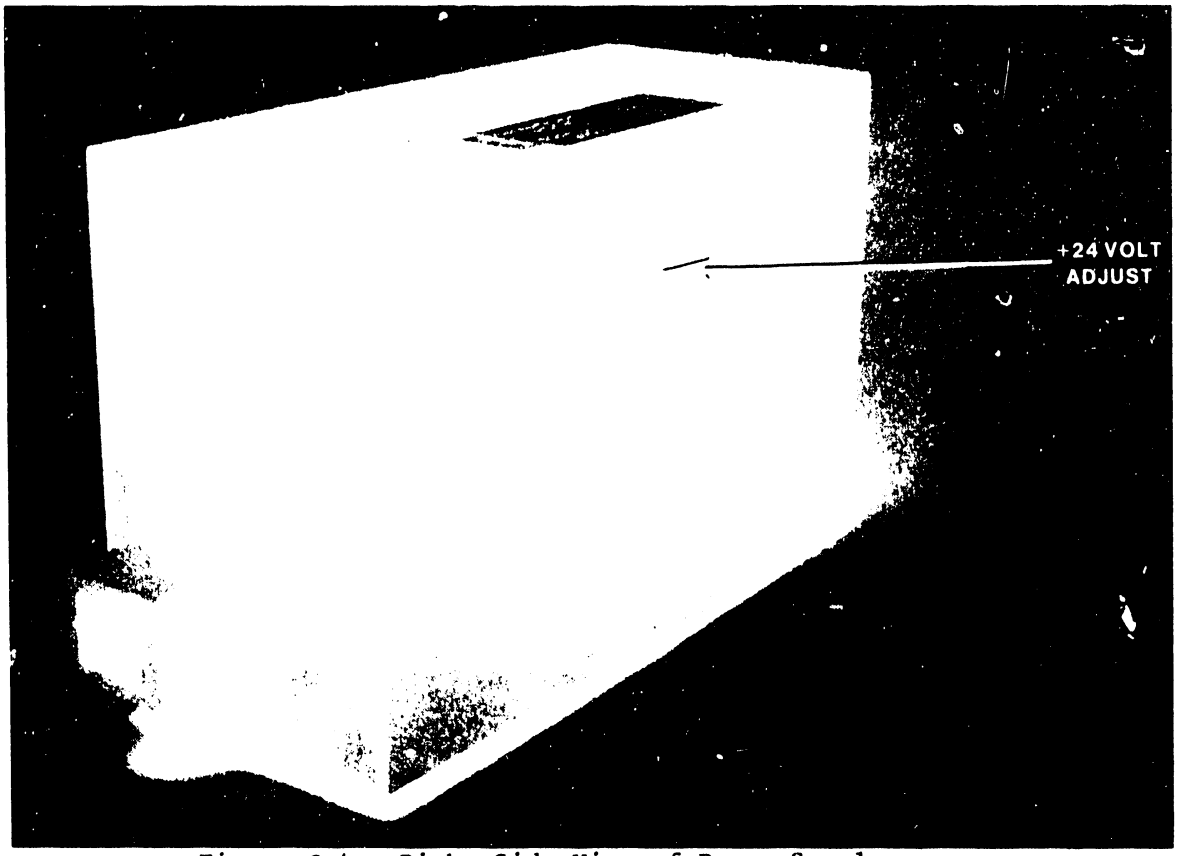


Figure C-4. Right Side View of Power Supply

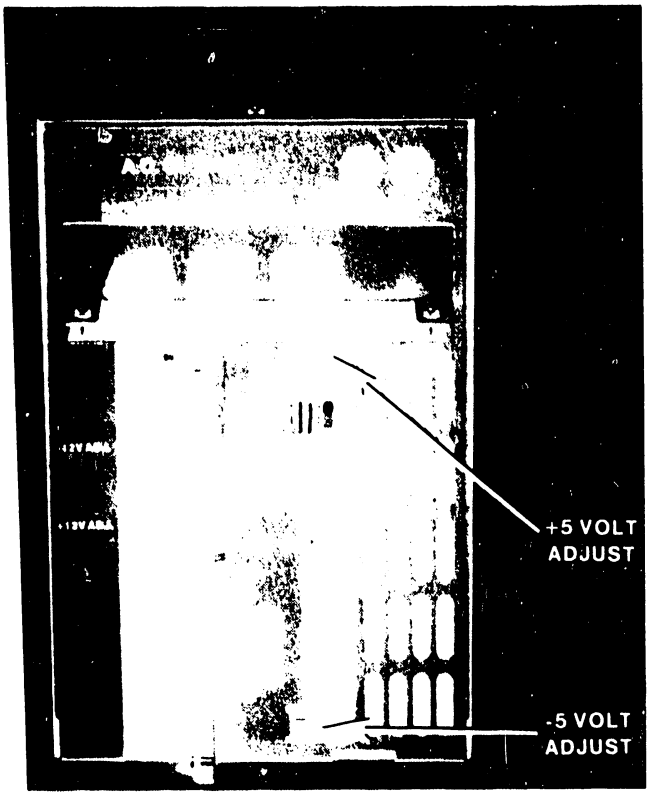


Figure C-5. Rear View of Power Supply

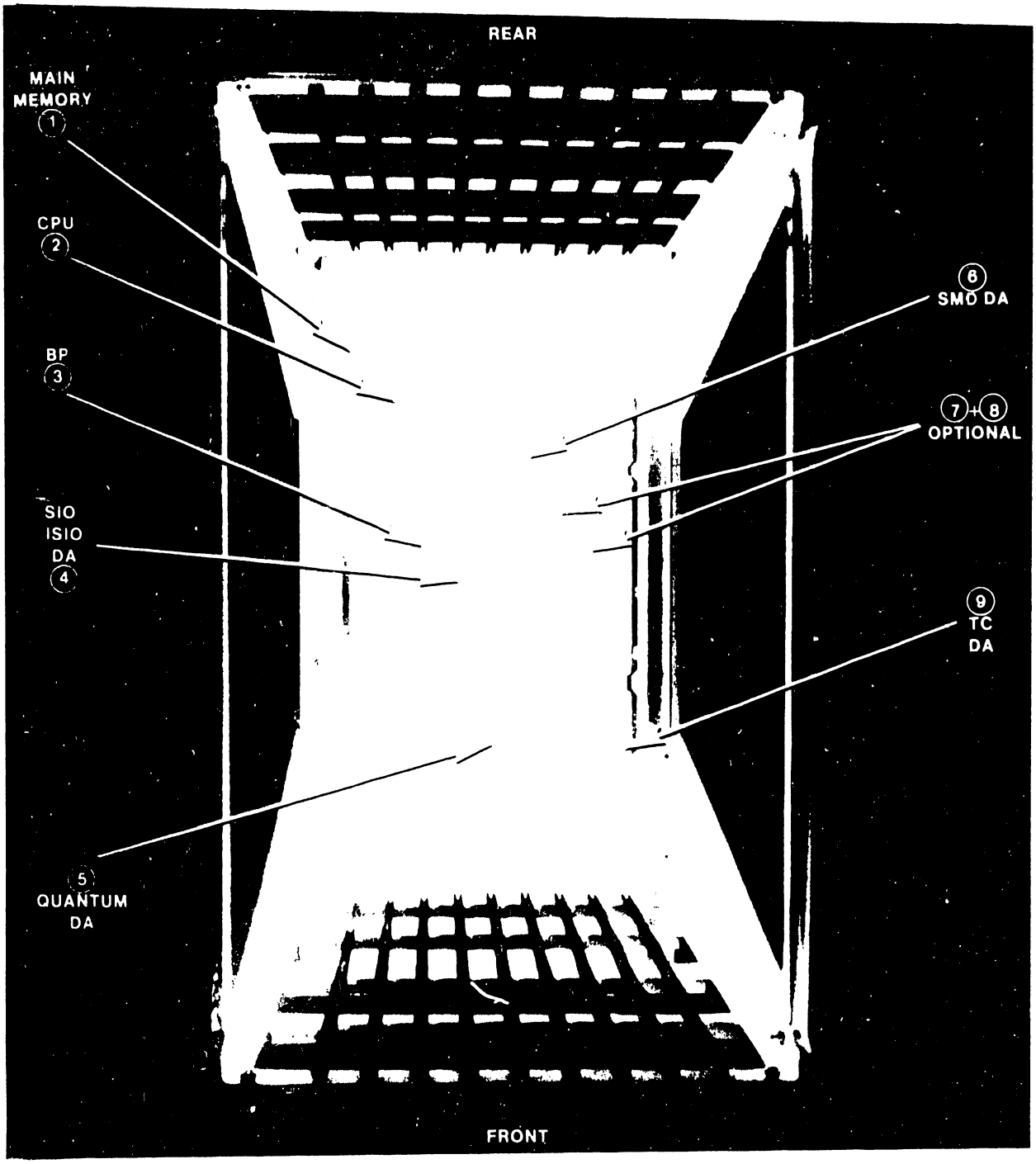


Figure C-6. VS-25/45 Motherboard

5. 210-8304 BP BOARD REMOVAL AND REPLACEMENT

a. Press the green Control Mode button on the VS-25/45 Front Panel. This prevents any disk I/O command in process from being halted prior to completion.
b. Power down the main frame by depressing the ac power On/Off switch on the Power Panel to the 0 position.
c. Each circuit board is held in place by two snaplocks. One snaplock tab fits under the top edge of the front rail of the board cage assembly and the second snaplock tab fits under the top edge of the rear rail of the board cage assembly.
d. Before removing the BP board (figure C-7) from Motherboard slot #3, disconnect the 26-pin connector from J1, the 34-pin connector from J2, and the 50-pin connector from J3 of the board.
e. Remove the BP by lifting the snaplocks to free the board from the Motherboard connectors. Once the board is free of the connectors, ease it straight up in the board guides and out of the board cage.
f. Make sure that all of the BP Software switches (table C-3) on the new board are in the OFF position.
g. Insert the new BP board in the board guide and lower it to the Motherboard connector.
h. Make sure the board edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.
i. Push down on the snaplocks to seat the board in the Motherboard.

CAUTION

DO NOT USE EXCESSIVE FORCE WHEN PUSHING DOWN ON THE SNAPLOCKS.

j. Reconnect all cables.

Table C-3. VS-25/45 BP Software Switch Settings

SWITCH #	PURPOSE (WHEN ON)	NORMAL POSITION
8	Diagnostic mode. ON to read other switches	OFF
7	Bypass Core Diagnostic	OFF
6	Bypass Core Diagnostic & Diagnostic Monitor	OFF
5	Loop on Core Diagnostic	OFF
4	Loop on Error	OFF
3	On = 4Mhz clock to 8086 microprocessor Off = 8Mhz clock to 8086 microprocessor	OFF
2	Data RAM clock	OFF
1	Data RAM clock	OFF

All switches must be OFF for normal operation of power-up diagnostics and system initialization.

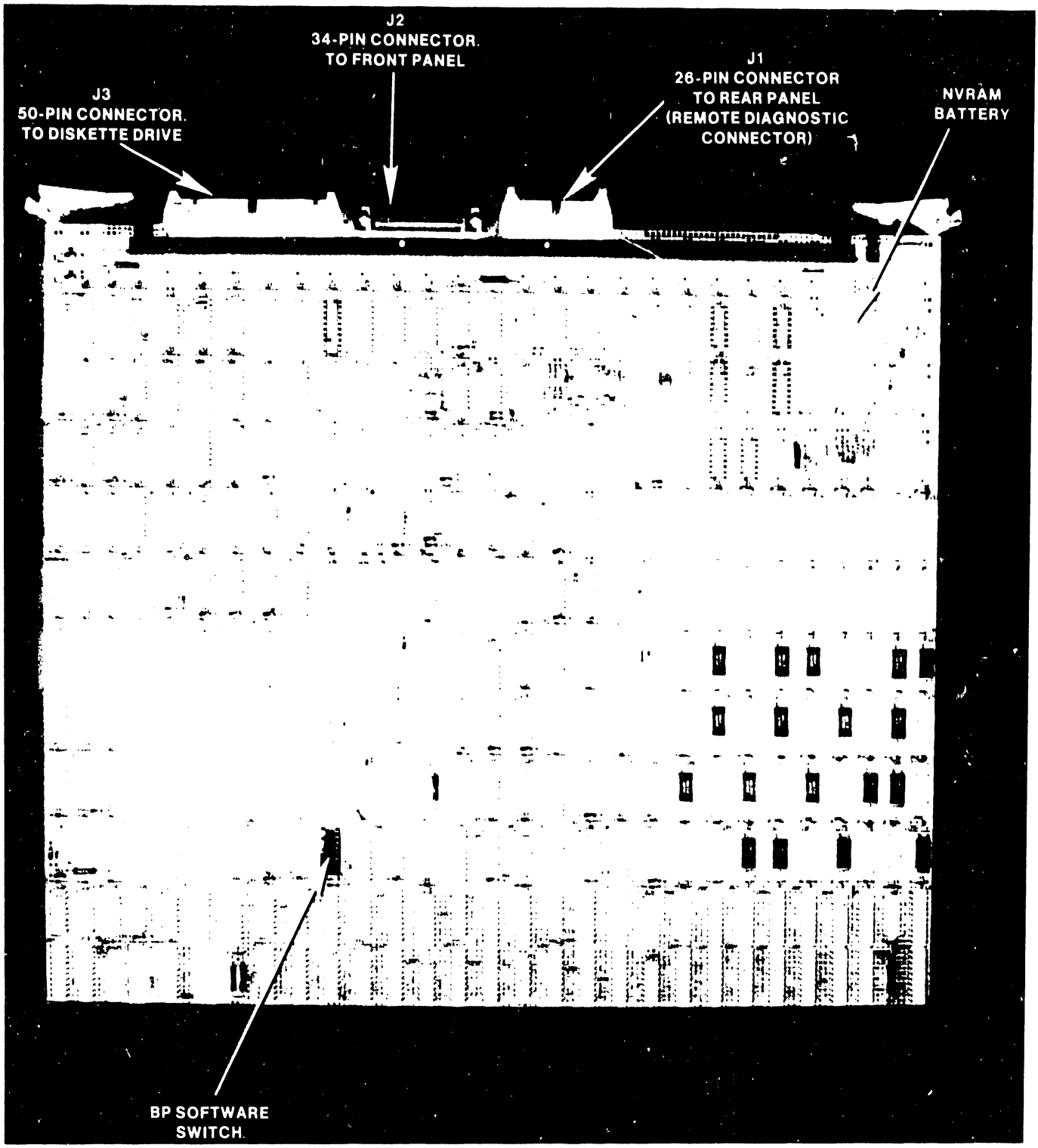


Figure C-7. 210-8304 Bus Processor Board

6. 210-7906 SERIAL I/O DA REMOVAL

a. Remove all connectors from the top of the Serial I/O Device Adapter (figure C-8) in Motherboard slot #4 (I/ODA1). Note the position of all connectors for installation of the ISIO board.

b. Remove the device adapter by lifting the snaplocks to free the adapter from the Motherboard connectors. Once the adapter is free of the connectors, ease it straight up in the board guides and out of the board cage.

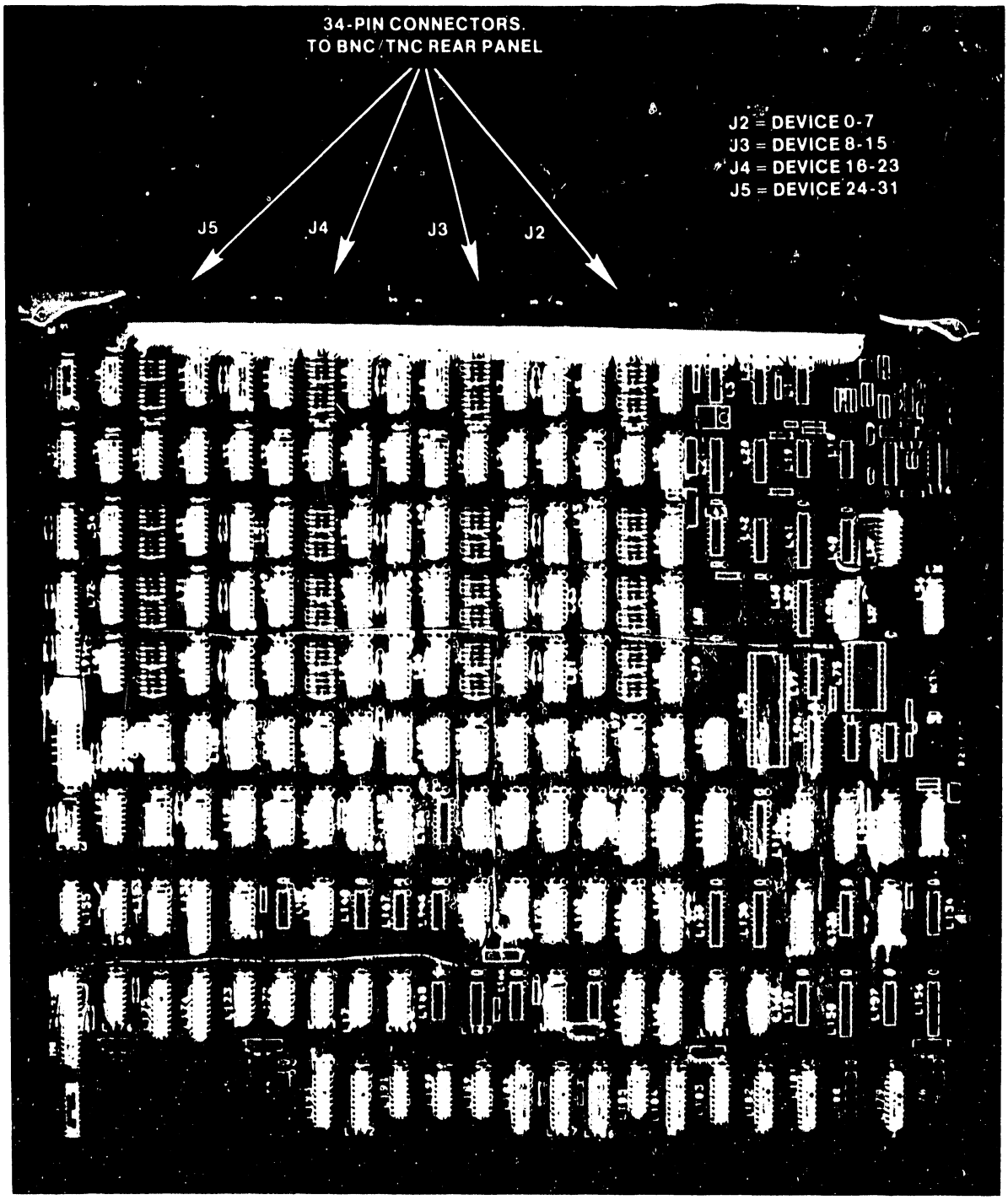


Figure C-8. 210-7906 Serial I/O Adapter

7. 210-8616 ISIO INSTALLATION

a. Check the jumpers (figure C-10) on the ISIO device adapter and install the adapter in Motherboard slot #4. (Workstation 0 must be connected to port #0 of this DA. This is a microcode convention and MUST be adhered to.) Insert the new adapter in the board guide and lower it to the Motherboard connector.

b. Make sure the adapter edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.

c. Push down on the snaplocks to seat the adapter in the Motherboard.

d. Reconnect all cables.

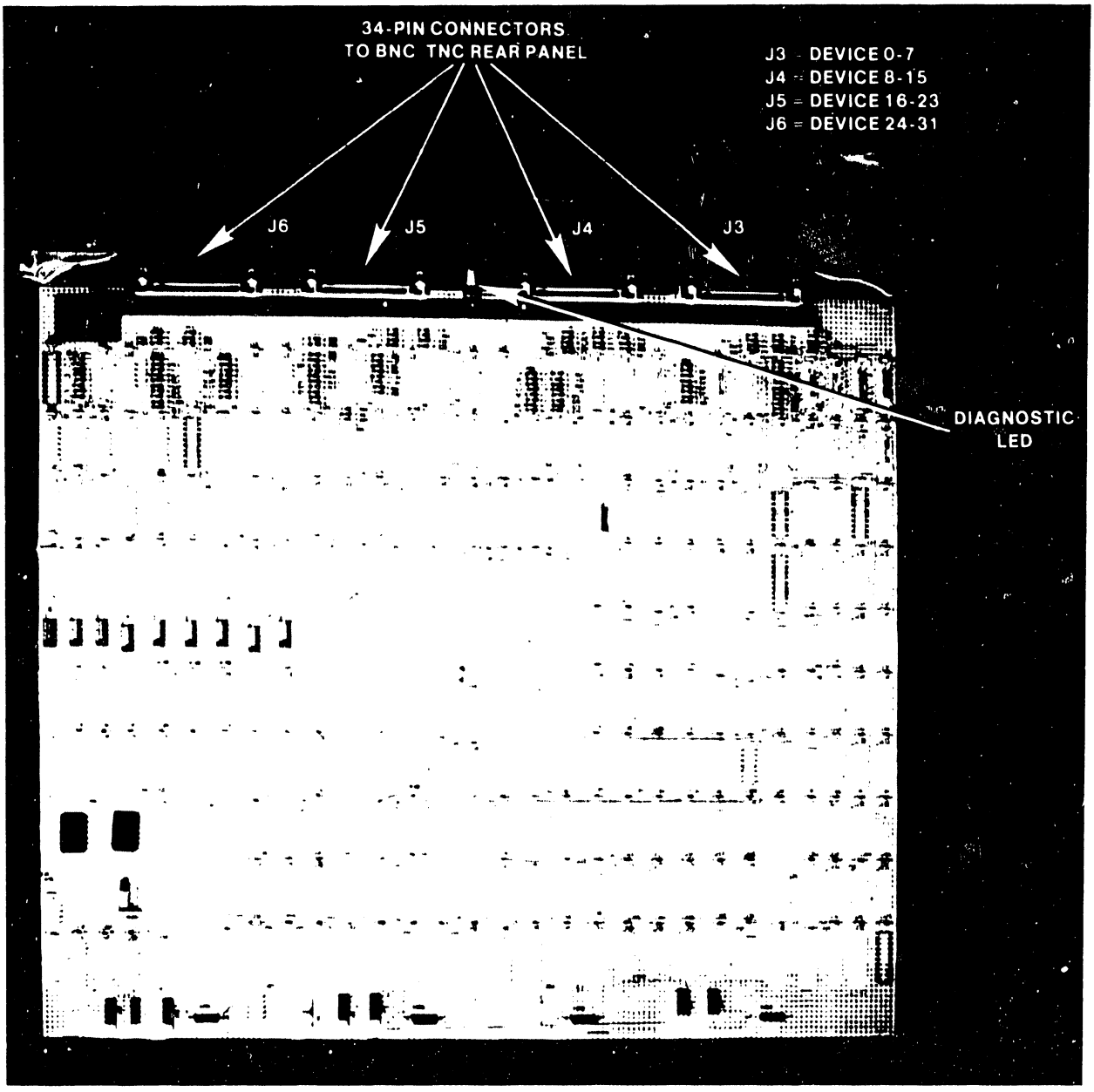
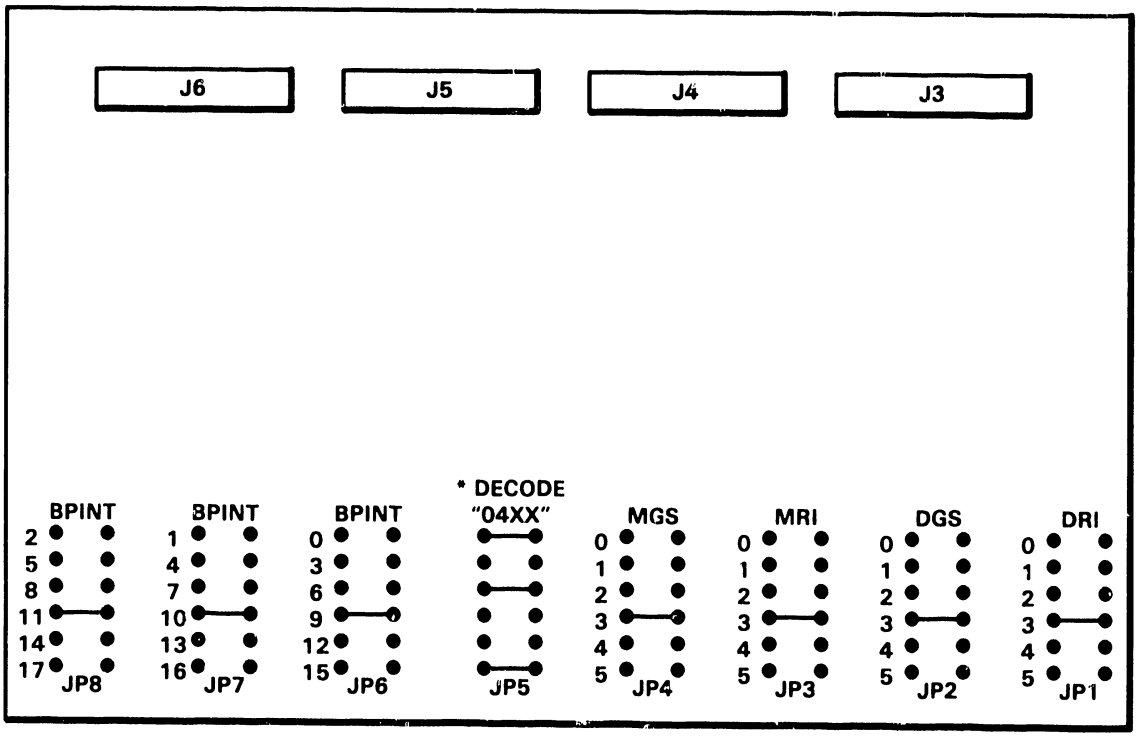


Figure C-9. 210-8616 Intelligent Serial I/O Adapter



* STANDARD CONFIGURATION. OTHER POSSIBLE CONFIGURATIONS.

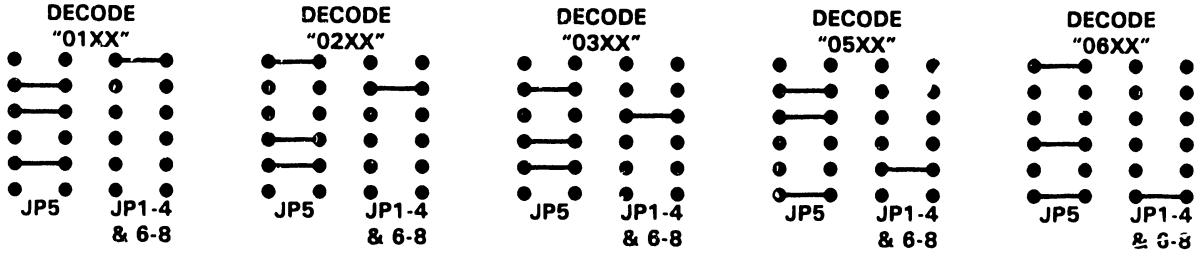


Figure C-10. 210-8616 Intelligent Serial I/O Adapter Connector and Jumper Locations

8. QUANTUM DA/QUANTUM DRIVE REMOVAL

a. Before installing the NEC drive, all Quantum drives and the 210-8325 Quantum Device Adapter must be removed.

b. To remove the Quantum Device Adapter:

1. Remove all connectors from the top of the Quantum Device Adapter (figure C-11) in Motherboard slot #5 (I/ODA2).
2. Remove the device adapter by lifting the snaplocks to free the adapter from the Motherboard connectors. Once the adapter is free of the connectors, ease it straight up in the board guides and out of the board cage.

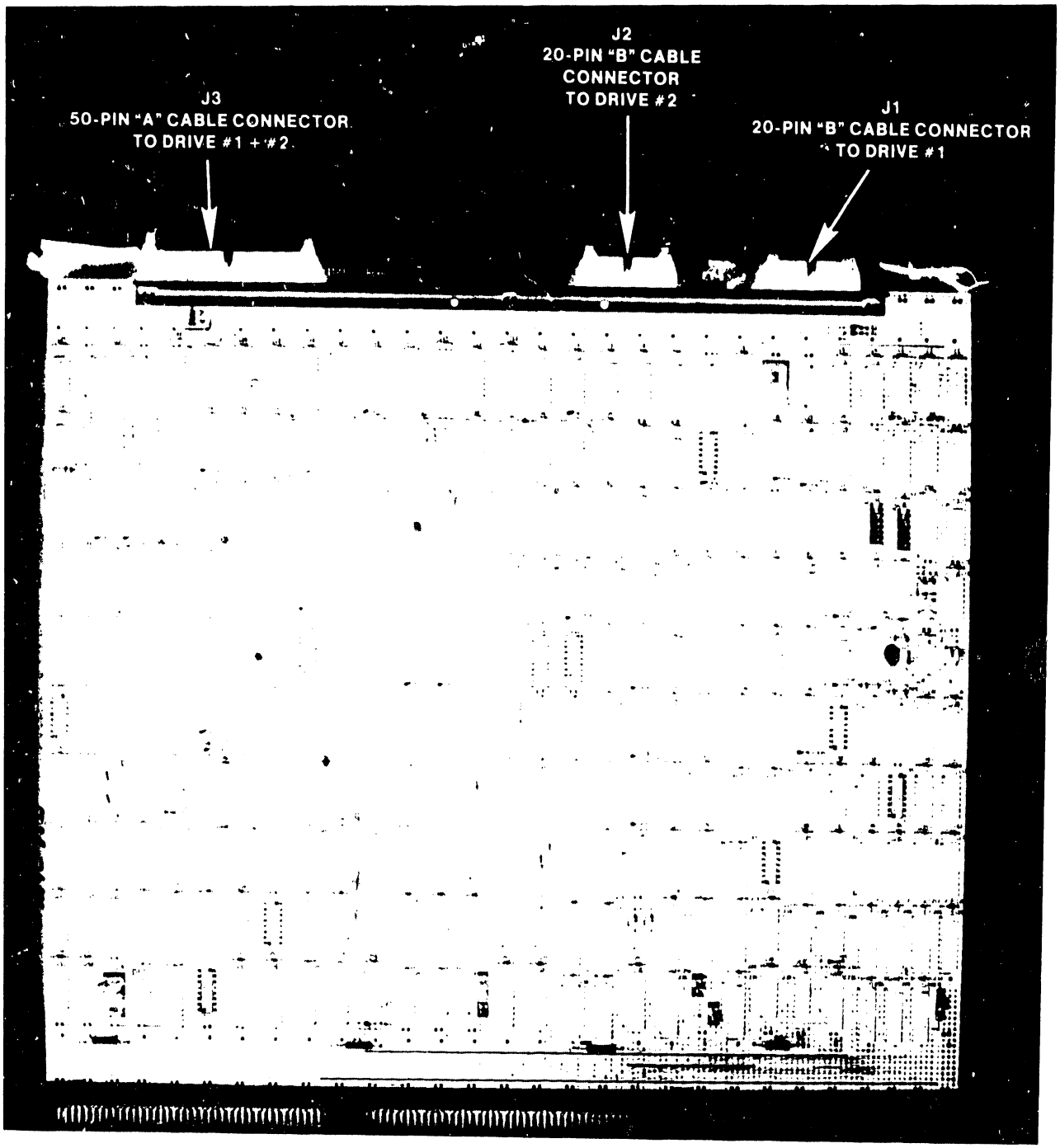


Figure C-11. 210-8325 Quantum Disk Device Adapter

c. To remove the Quantum drive(s):

1. The Quantum drive(s) is bolted to the cabinet by one 5/16 inch hex bolt at the front of the drive(s) which is secured by a Pem nut under the cabinet. After the drive has stopped turning, remove the hex bolt while holding the Pem nut under the cabinet.
2. Carefully slide the drive forward. The A and B signal, and ac and dc power cables are connected to the rear of the drive. Remove the A and B cables from the drive and from the system.

Remove the ac and dc cables from the drive. Disconnect the dc cable from J5 of the SPS450 Switching Power Supply (figure C-21) and remove the cable from the system. A new dc cable will be used for the NEC drive. The drive does not use ac power.

3. Slide the drive forward and out of its bayonet slide on the bottom of the drive. Remove the drive from the cabinet, avoiding contact between the drive and adjacent equipment.
4. Lock the actuator and the drive pulley. (Figures C-12 and C-13).

d. Return the Quantum drive(s) and the Quantum Device Adapter to local (branch/district) stock.

Figure C-12. Quantum Drive Spindle Lock

Figure C-13. Quantum Drive Actuator Lock

9. SMD DA INSTALLATION

a. Install the 210-8312 SMD Device Adapter (figure C-14) in Motherboard slot #6 (I/ODA3), figure C-6.

b. Set the 8-position disk device type switch SW1 for the NEC drive, referring to figures C-14 and C-15. The switch is at location L178 on the adapter.

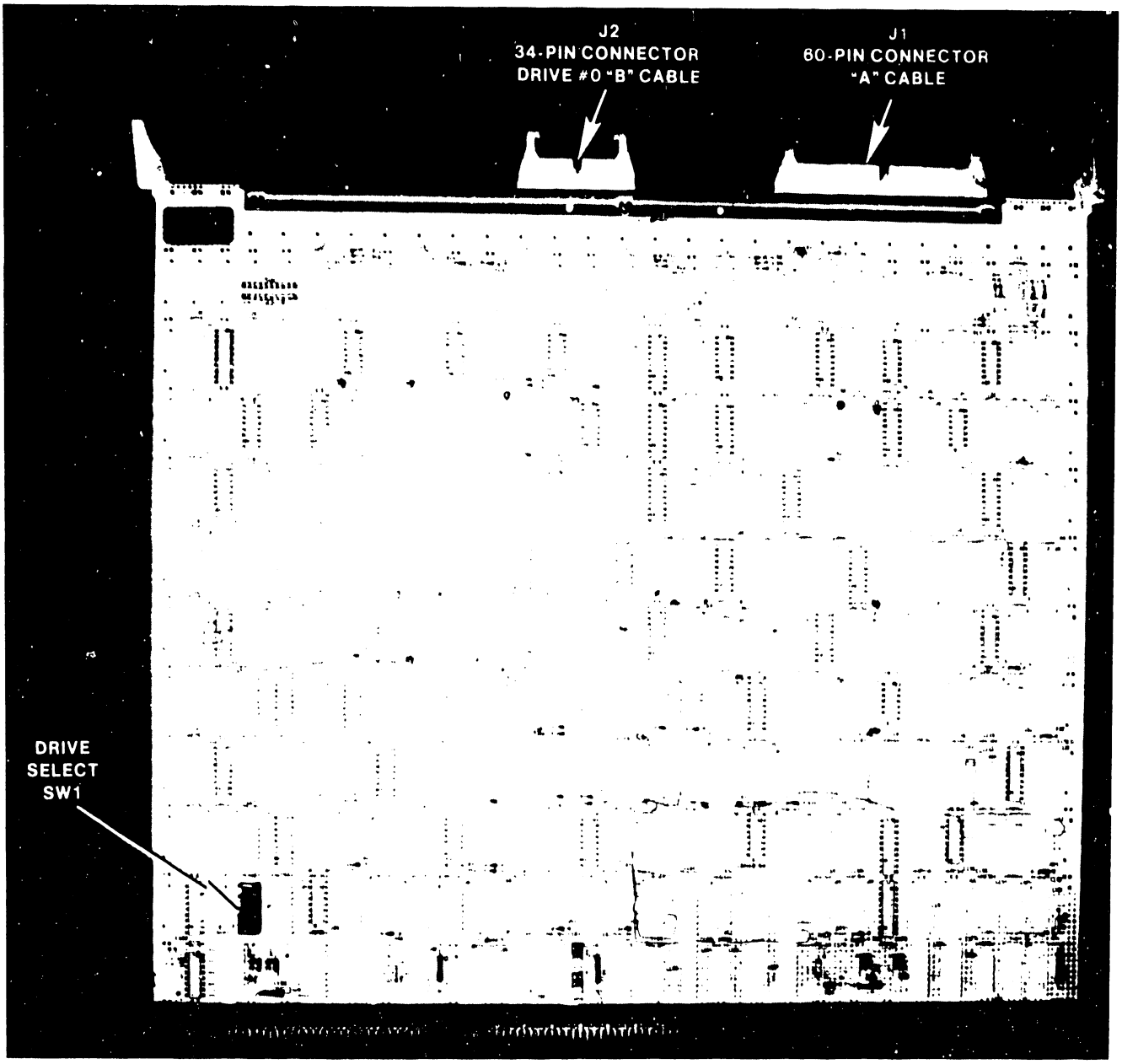


Figure C-14. 210-8312 1-Port SMD Disk Device Adapter

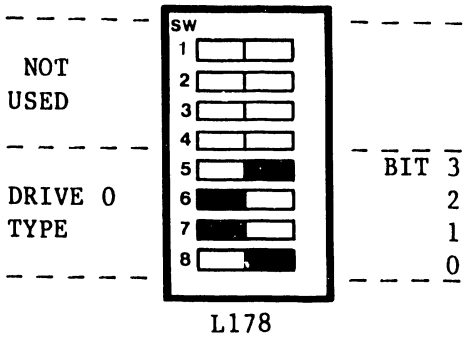


Figure C-15. SMD Disk Device Adapter.
Disk Device Type Switch Setting For NEC Drive.

c. Check all address selection jumpers as shown in figure C-16. The device address for the SMD adapter is 02xx. Make sure that the SMD DA address does not conflict with other DA addresses.
d. Install the adapter in Motherboard slot number #6. Insert the adapter in the board guides and lower it to the Motherboard connector.
e. Make sure the adapter edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.
f. Push down on the snaplocks to seat the adapter in the Motherboard.
g. Connect the new A cable (220-3332) to J1 and the new B cable (220-3331) to J2 of the SMD DA. (Figure C-14.)

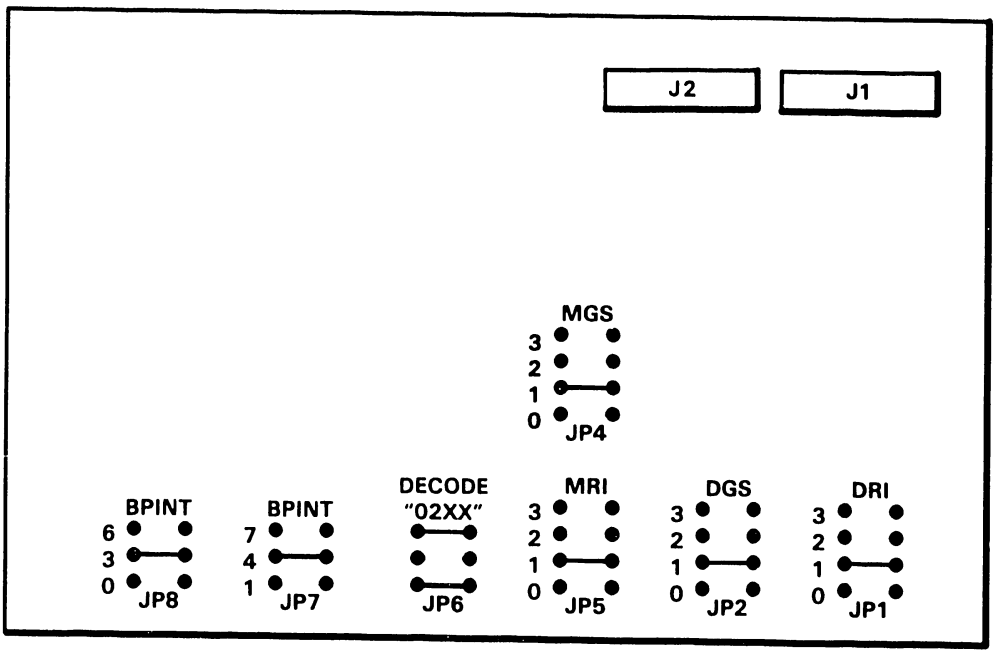


Figure C-16. SMD Disk Device Adapter
Connector and Jumper Locations

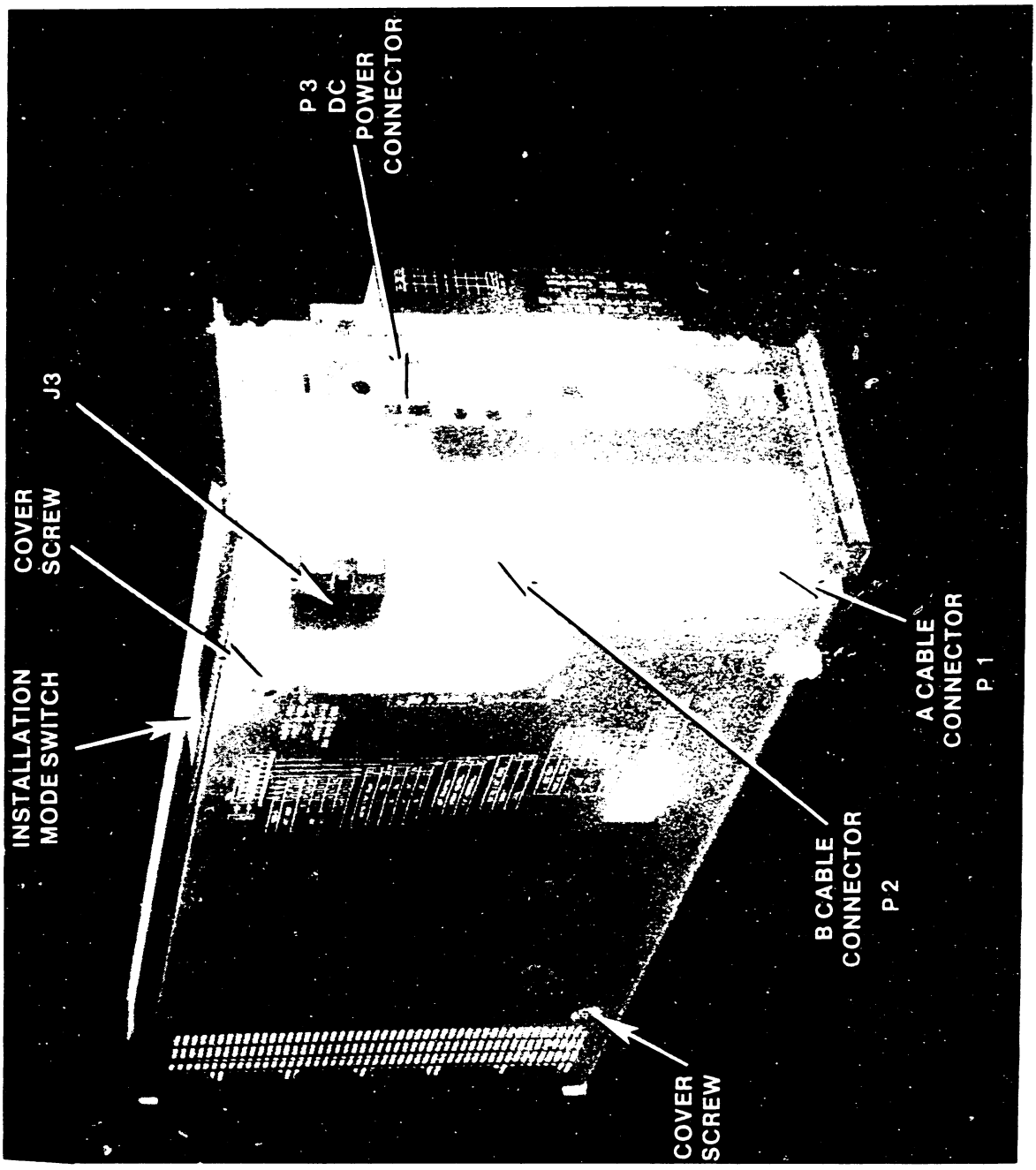


Figure C-17. NEC Disk Drive

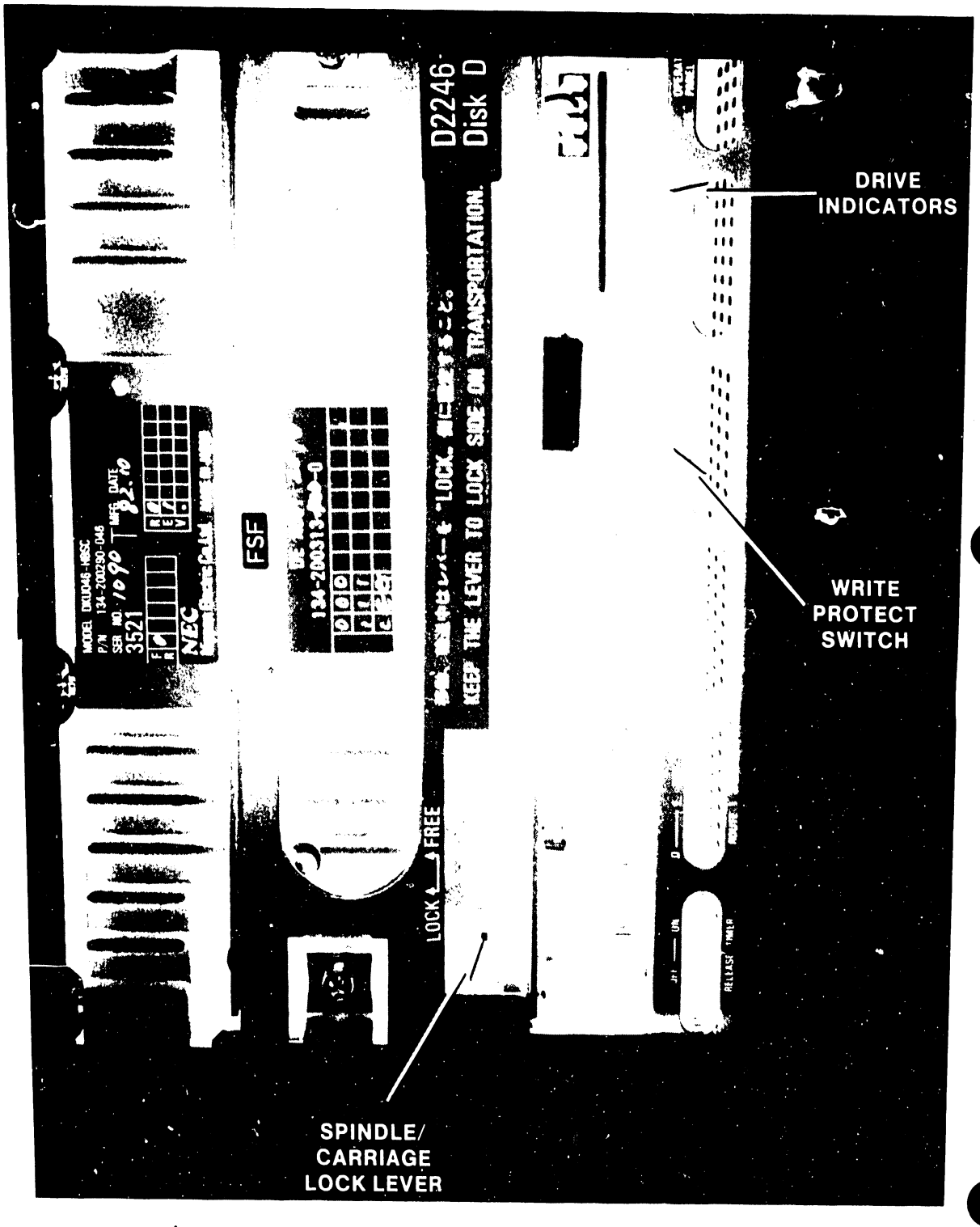


Figure C-18. Front View of NEC Drive

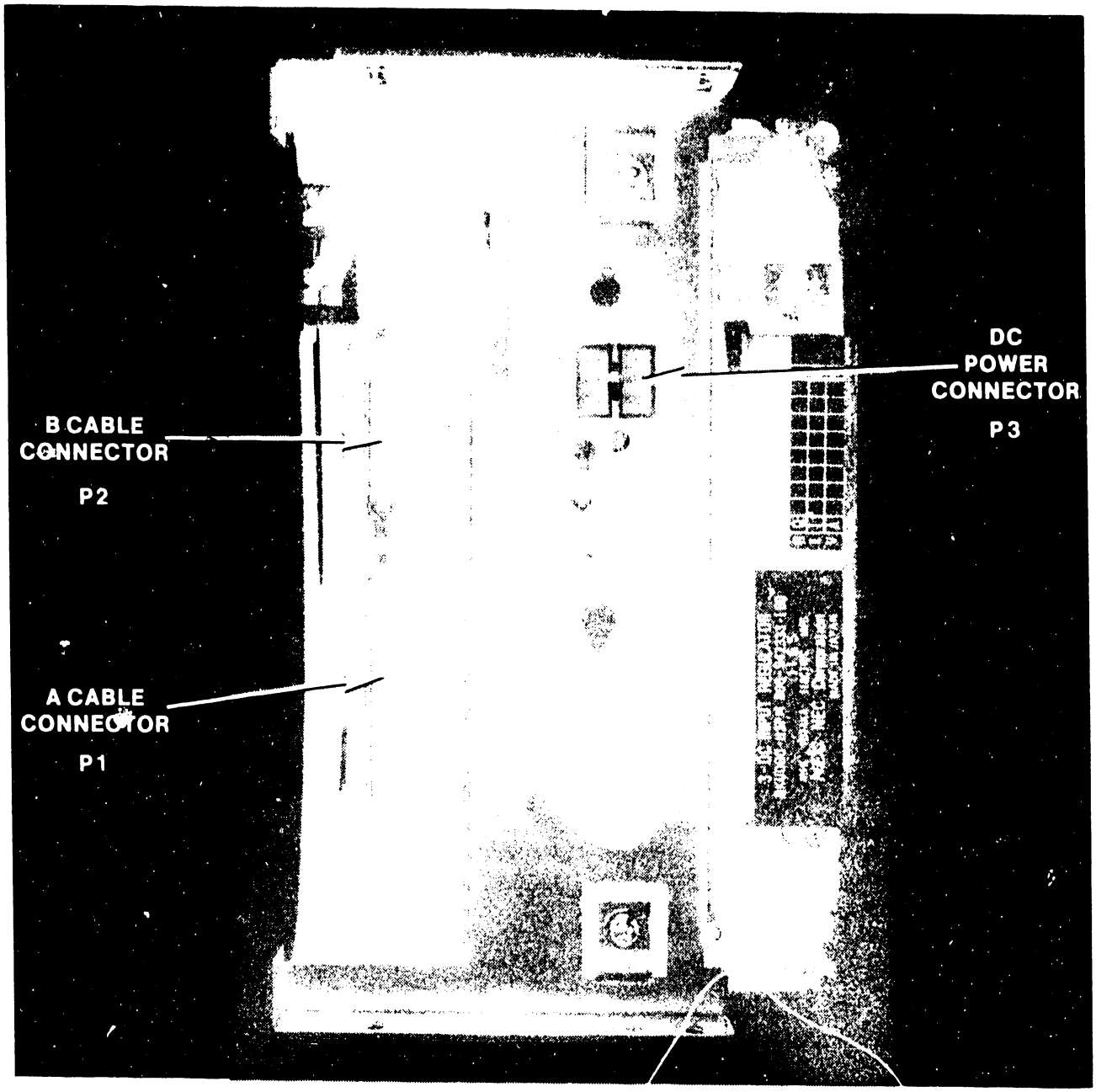


Figure C-19. Rear View of NEC Drive

10. NEC DRIVE INSTALLATION

CAUTION

The drive weighs approximately 30 pounds (14 kilograms).

a. After unpacking and before installing the NEC drive, check the Installation Mode, the Control Mode, and the Number of Sectors switches on the Logic/Servo PCB in the drive as follows:
   1. Lay the drive down on its left side, with the red Spindle/-Carriage Lock Lever toward the front.
   2. Remove the two Phillips screws (figure C-17) from the upper right corner and the lower left corner of the right side cover. Carefully lift off the cover.
   3. Remove the three signal cables from P55, P53, and P41 on the top of the Logic/Servo board (figure C-20). Remove the 9-pin power connector P3 on the rear of the board. Note the positions of the cables for reinstallation.
   4. Remove the two Phillips screws from the upper left corner and the lower right corner of the board. Carefully tip the board to the left so that the component side is facing up. There is a single ground wire and a 2-wire cable still connected to the board.
   5. Check each of the three switches as shown in figure C-20. They must be set as shown in the figure. The Number of Sectors and the Control Mode switches have clear plastic covers that must be removed before the switches can be set. Make sure to put the covers back on before reinstalling the board.

b. Carefully tip the board back to its normal position, backplane side up, and reinstall the two Phillips screws. Make sure that the 2-wire cable does not get caught between the board and the upper left board bracket.

c. Reinstall the three signal cables and the the 9-pin power connector on the board.

d. Make sure that there are no cables in the way and carefully reinstall the right side cove and the two Phillips screws.

e. Set the drive back to its normal vertical position with the red Spindle/Carriage Lock Lever still facing toward the front.

f. Set the drive on the 452-0308 mounting plate and secure all four corners of the drive to the mounting plate with the 650-4080 mounting screws.

g. Before sliding the drive all the way back into the cabinet, connect the A signal cable to P1 and the B signal to P2, and the dc power cable (220-2059) to the 6-pin connector P3 at the rear of the drive. (Figure C-19.) The drive does not use ac power.

h. Slide the drive and mounting plate into the cabinet. Bolt down the drive through the two holes at the front of the mounting plate to the two holes in the main frame cabinet where the Quantum drives would normally be bolted. Use two 650-9082 shoulder screws.

i. Unlock the spindle and carriage from their shipping position by moving the red Spindle/Carriage Lock Lever on the front of the drive (figure C-18) to the right, push it up as far as it will go, and then move it to the left into the Free position.

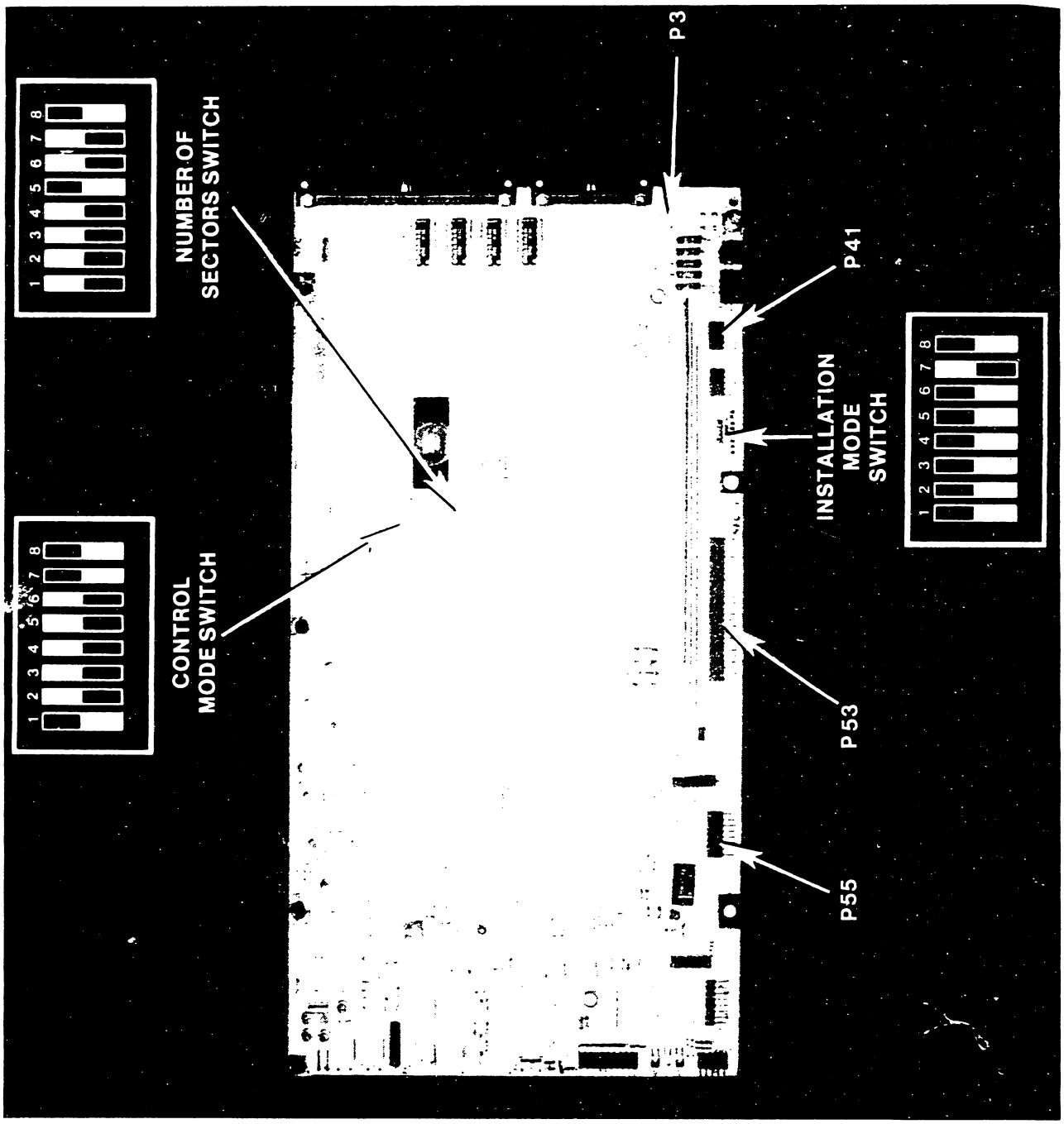


Figure C-20. Disk Drive Logic and Servo PCB

j. Connect the dc power cable from the disk drive to the 6-pin connector J5 on the switching power supply. (Figures C-21 and C-22.)

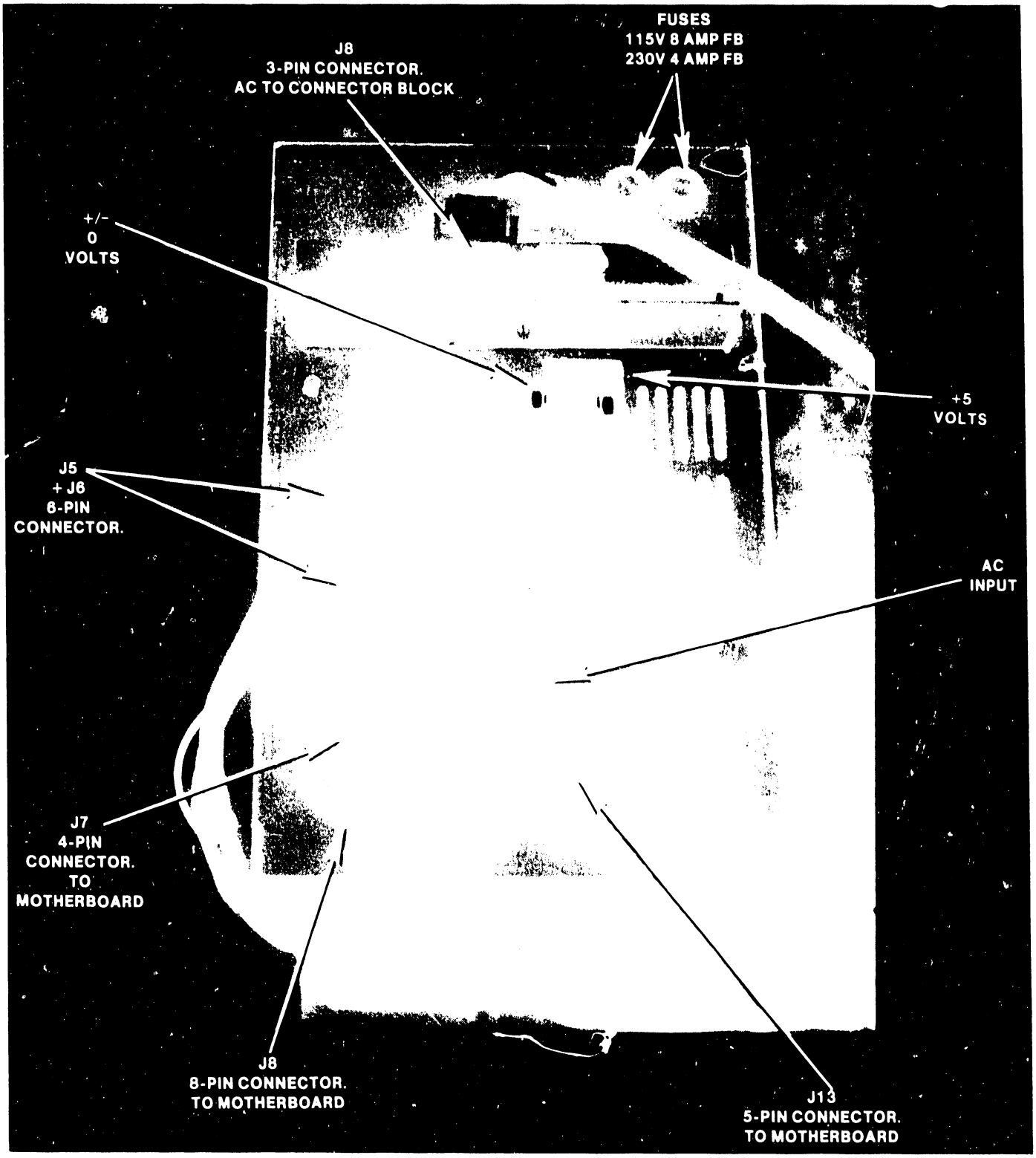


Figure C-21. Rear View of VS-25/45 Power Supply

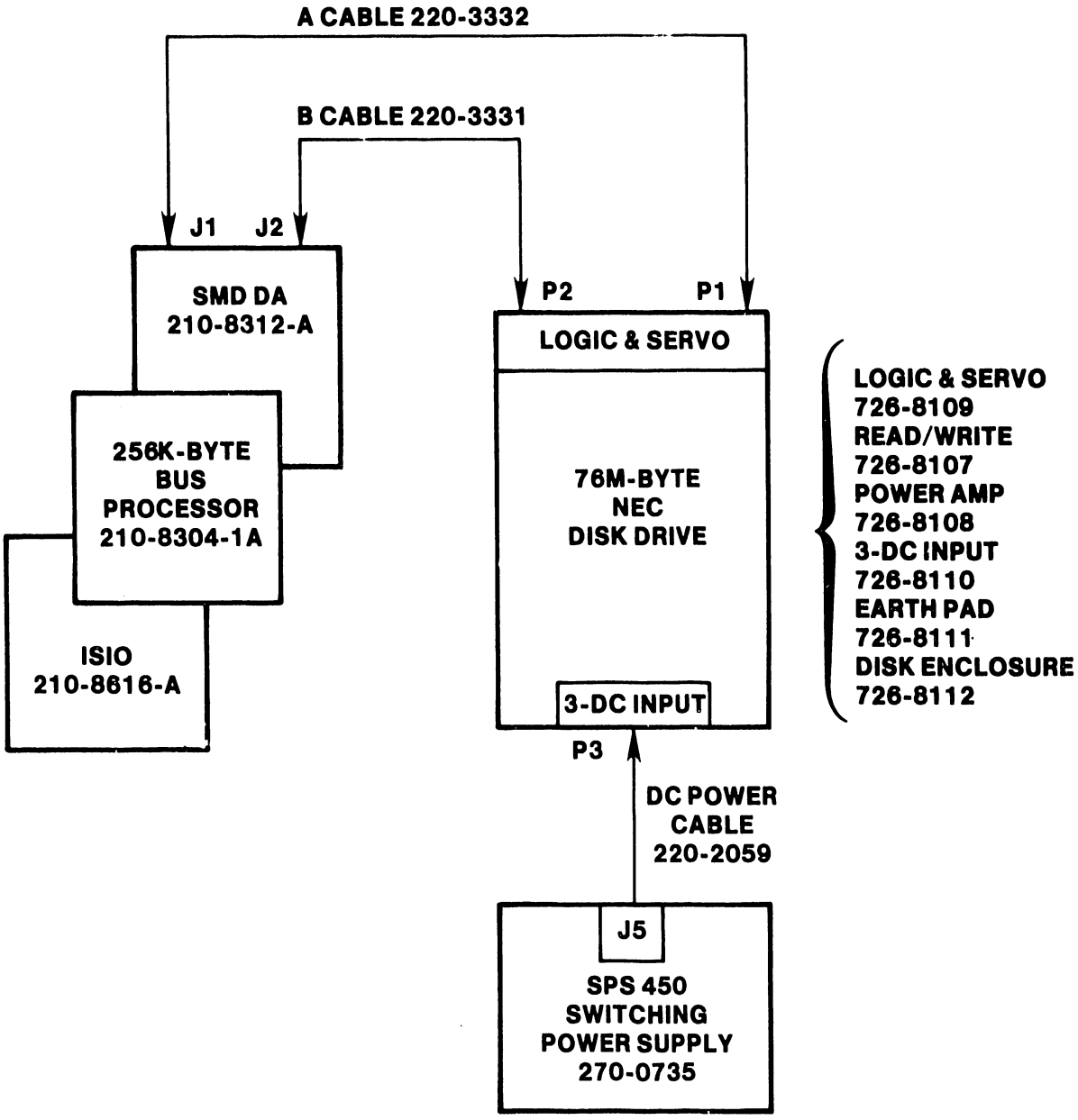


Figure C-22. NEC Disk Drive Cable Interconnections

Table C-4. NEC Drive Switches

SWITCH NAME/TYPE	LOCATION	PURPOSE
WRITE PROTECT Toggle switch	Front of drive	Places the drive in the write protected mode
INSTALLATION MODE DIP switch	Logic/Servo PCB	Unit Select/Motor Start Delay/Unit Mounting Position/Motor Start Mode
CONTROL MODE DIP switch	Logic/Servo PCB	Device Type/Format Write Release/Tag Bit #4 Inhibit/Fault Inhibit
NUMBER OF SECTORS DIP switch	Logic/Servo PCB	Selects number of sectors per track (Nine sectors per track for VS-25/45)

Table C-5. NEC Drive Indicators

INDICATOR NAME/TYPE	LOCATION	PURPOSE
READY LED (GREEN)	Front of drive	Indicates unit is up to speed and heads are on cylinder. Fault can still exist
FAULT LED (RED)	Front of drive	Indicates fault condition within drive. (Drive is automatically write protected)
SEEK ERROR LED (ORANGE)	Front of drive	Indicates a seek error within drive. (Drive is automatically write protected)

11. NEC DRIVE REMOVAL

To remove a drive:

a. Power down the main frame by depressing the ac power On/Off switch to the 0 position.
b. Remove the main frame top and front covers.
c. Make sure the drive has stopped turning and then lock the spindle and carriage into their shipping position by moving the red Spindle/Carriage Lock Lever on the front of the drive (figure C-18) to the right, push it down as far as it will go, and then move it to the left into the Lock position.
d. Remove the two shoulder screws securing the front of the mounting plate to the two holes in the main frame cabinet.

CAUTION

The drive weighs approximately 30 pounds (14 kilograms).

e. Carefully slide the drive forward. The A and B signal, and dc power cable are connected to the rear of the drive. Note the locations of these cables for reinstallation and then remove the cables. The cables are keyed to ensure proper insertion.
f. Remove the four screws securing the four corners of the drive to the mounting plate and remove the drive from the mounting plate.

12. NEC DRIVE REPLACEMENT

To install a replacement drive, refer to NEC Drive Installation procedures.

13. MAIN FRAME POWER-UP

a. Make sure that the ac power On/Off switch on the Power Panel is in the 0 position and then plug the main frame power connector into the power source receptacle.

b. Perform the following in the sequence given:

1. Set the Front Panel Bootstrap Media switch to the up position (select diskette drive). No diskette should be in the drive.
2. Depress the ac power On/Off switch to the 1 position.
3. Make sure the ac Power On lamp on the Power Panel is lit, the main frame cooling fans are turning, and the diskette drive motor is running. The NEC drive should not be running.
4. Wait 5 seconds after ac power is applied and then press the DC Initialize pushbutton.
5. The NEC drive should power up after the DC Initialize pushbutton is pressed. Make sure that the DC Power On LED on the power supply, the Power On LED on the Front Panel, and the HEX Display LEDs are lit after the DC Initialize pushbutton has been pressed. If the HEX Display LEDs go out after 2 seconds, there is a problem with the dc voltage compare circuit in the power supply.
6. The HEX display on the Front Panel will begin counting down a series of numbers from FFFF to 0000 and then count up through a series of diagnostic routines (typically 10, 11, 12, 13, 14, 15, and 16) and stop at 9820, Diskette drive not ready. If any number (except 9820) is displayed for more than 15 seconds, the system has failed one of the diagnostics.
7. At the same time the HEX display on the Front Panel is counting, the TC DA PROM-based power-up diagnostics will be running as shown on the TC DA Front Indicator/Control Panel. The diagnostics will complete successfully in about 12 seconds.
8. Check the dc voltages.

NOTE

If the diagnostics failed and the voltages listed below are correct, refer to VS 25 Bulletin, WLI P/N 800-3108-02, for Self-Test Monitor Diagnostic Error Codes.

14. COLDSTART PROGRAM

The basic VS-25/45 CPU currently supports only one removable diskette media (the 1.2 Megabyte diskette). In order to bring up the VS Operating System on this basic hardware, the NEC disk drive must be initialized and then loaded with the necessary operating system files. The Coldstart program provides this function.

Coldstart is a stand-alone program which is IPLed from a media tolerant diskette. The program uses the diskette drive, the fixed drive, and Workstation 0. The program copies the OS files from a series of disks. The Coldstart program builds a media-tolerant VTOC on the fixed disk as it copies the OS files. Coldstart can also copy the CP and BP code and bootstrap files to the fixed disk, allowing both bootstrapping and IPLing from the fixed disk.

Additional Coldstart functionality is being considered in order to assist in backing up fixed-disk files (to diskette) in case of damage to the fixed disk during system operation. However, a diskette-based version of the OS is not planned for VS-25/45 system support.

15. OPERATING SYSTEM 6.20 COLDSTART PROCEDURE

The 6.20 Coldstart is a self-contained, stand-alone program. It doesn't use the normal operating system, nor can the normal operating system use it. The Coldstart utility has two modes of operation, the Copy mode and the Backup mode. The Copy mode allows three different ways to copy data from the input diskette to the system volume.

Initialize the system volume before copying the data.
Reformat the system volume before copying the data.
Copy only those files that you want to add to or update the system volume with.

The method selected depends on circumstances. If a new system is being installed, it is likely that the disk to be used for the system volume is not initialized. Because the disk must be initialized before it can be used, select the first option.

The second option, reformatting, can be used to bring up a system when the system volume has been initialized previously. Reformatting clears the volume of existing data and rewrites the VTOC. This option is required if the system volume is not media tolerant.

The third option, Copy only, allows loading new system files without rebuilding the entire system. Coldstart checks for duplicate file names, flags each, and allows you to skip the input file or to rename either the old or the new file.

The Backup method of Coldstart is useful on single disk systems in the situation where, for some reason, you can read but not IPL from the system disk. By running the Backup mode before reformatting, undamaged data resident on the volume can be preserved.

NOTE

The Coldstart Backup module does not work on a disk with either hard I/O errors or a bad VTOC.

a. Make sure the Local/Remote switch is in the Local position. (The system will not IPL if the switch is in Remote.)
b. Set the Bootstrap Media switch on the front panel to the up position (selects the diskette drive).
c. Insert the diskette labeled Format into the diskette drive and close the door.
d. Press the red Initialize button on the front panel. In about 30 seconds W/S 0 will display the following Menu:

VS Self Test Diagnostic Monitor
IPL Drive Selection
Bootstrap Volume = FORMAT

Device	Capacity	Type	Volume	Status
2270V-4	1.2 Mb	Dsket	FORMAT	Media Tolerant
2220	76 Mb	Fixed		

Position Cursor to Indicate Device and Select:

(ENTER) IPL (8) STAND ALONE DIAGNOSTIC MONITOR

e. Position the cursor next to the disk labeled FORMAT and press ENTER. The Self-Test Monitor diagnostics will begin running.

NOTE

To successfully run the (BP) USART Loopback Verification Test of the Self-Test Monitor, either an RS-232 Loopback connector (WLI P/N 420-1040) or a modem must be connected to the RS-232 Remote Diagnostic connector on the CPU rear panel. The modem must have ac power applied to it and signal DSR (Data Set Ready) must be ON. If the Loopback connector or the modem is NOT installed, the test will respond with Non-fatal Error, code 3C03. Press ENTER to continue.

VS Self Test Monitor Package
System Hardware Status
System Volume = FORMAT

Status	Diagnostic	
Passed	(SIO) Serial Data Link Test	
Non-Fatal Error	(BP) USART Loopback Verification Test	Code = 3C03
Passed	(CPU) CP Control Memory & CP/BP Test	
Passed	(CPU) CP Random Operands Test	
Passed	(CPU) CP Integrity Test	
Passed	(MM) Main Memory Integrity Test	
Passed	(BP) BP DMA & MARS Test	

Diagnostics Completed, Beginning System Initialization

f. If the Main Memory Integrity test fails, run the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.

g. After the Self-Test Monitor diagnostics have successfully completed, W/S 0 will display the Standalone Utility System screen.

```
*** Wang VS Standalone Utility System ***

The Standalone Utility System allows users of single-disk systems to
perform operations on their system disks that are not available under
normal VS operating system control.

Please select the desired function by pressing the appropriate PF key:

    (2) COLDSTART - Used for formatting, copying to, or backing up
                    the system disk.

    (3) CIP       - Used to consolidate free extents on the volume
                    without the need to do a full volume backup and
                    restore.
```

h. Press PF 2, COLDSTART. W/S 0 will display the System Disk Specification screen.

```
*** Wang VS Coldstart ***

The primary purpose of the COLDSTART standalone utility is to bring up a new
machine by formatting the system disk and copying a minimum system to it.
COLDSTART may also be used to add programs to an existing system (Copy only)
or to backup an existing system.

            Please specify the system disk and press ENTER.

                Device Type                    - 2220
                Physical Device Address (Hex)  - 2400

Device Type   Description            Device Type   Description
2260VR        10 Meg F/R Disk (R)    2260VF        10 Meg F/R Disk (F)
2265V1        75 Meg Rem Disk        2265V2        275 Meg Rem Disk
2280V1R       30 Meg F/R Disk (R)    2280V1F       30 Meg F/R Disk (F)
2280V2R       60 Meg F/R Disk (R)    2280V2F       60 Meg F/R Disk (F)
2280V3R       90 Meg F/R Disk (R)    2280V3F       90 Meg F/R Disk (F)
2265V1A       75MB R dual port Dk    2265V2A       288M R dual port Dk
2265V3        620 Meg Fixed Disk     Q2040         8 inch Fixed Disk
2265V3A       620Mb Dual Port Disk   2220          8in 75meg fixed disk
D2257         160Mb 8in Fixed Disk   2230          32Mb 5-1/4in Fix Dsk
```

i. Enter the device type of 2220 (above) and physical device address of 2400 (formerly the Quantum device address) for the NEC drive. Press ENTER

NOTE

Coldstart works on any drive. However, a system bootstrap must be from a diskette, the fixed disk of a VS-25 or VS-45, or the removable part of a fixed/removable disk.

j. The Coldstart main menu will appear, allowing selection of a Copy or Backup operation.

```
*** Wang VS Coldstart ***

Press PF4 to COPY to system disk, or
      PF5 to BACKUP the system disk.
Press PF1 to return to the previous screen.
```

k. Select Copy (PF4). The Select Copy Mode screen will appear.

```
*** Wang VS Coldstart ***

Press PF2 to INITIALIZE the system disk,
      PF3 to REFORMAT the system disk, or
      PF4 to COPY only.
Press PF1 to return to the previous screen.
```

l. Press PF2 to initialize the NEC drive.
m. The System Disk screen should appear. Enter the requested information and press ENTER to continue.

```
                    *** Wang VS Coldstart ***

                            System Disk

    The following information is required for volume reformatting:


Volume name                 - SYSTEM
Volume owner                -
Date (MM/DD/YY)             -   /  /
VTOC size (in blocks)       -


        Please supply the required parameters and press ENTER.
        or Press PF1 to return to the mode selection screen.
```

n. Coldstart then initializes the system disk. W/S 0 will respond with the following message: "Disk Formatting In Progress".
o. After initialization is complete, Coldstart requests mounting the first diskette to be copied.
p. Remove the Format disk and insert the diskette labeled SYST01 into the diskette drive and close the door.
q. When the copy is finished, W/S 0 will respond with the following message: "All files on this disk have been copied. Please mount SYST02." (Coldstart gets the name of the next diskette to be mounted from the current diskette.)
r. Repeat step q. until the contents of all diskettes labeled SYST have been copied.
s. When the last diskette has been copied, W/S 0 will respond with the following message: "IPL when ready"
t. Set the Bootstrap Media switch on the front panel to the middle position (selects the internal fixed drive) or to the down position (selects external drives).
u. IPL the system and log on as user CSG.
v. Run the GENEDIT program (refer to the VS25 Bulletin, WLI P/N 800-6183), declare all peripherals, and reIPL.
w. Run the BACKUP program, using the RESTORE function, and copy the following volumes to the system disk: NVRAM, MACLIB, WSCODE, PRCODE, UTLTY1, UTLTY2, WP1, and WP2
x. When the message "The WORK file cannot be placed on the output volume. Please respecify." appears, press PF1 to continue.
y. When all volumes have been copied, the Coldstart procedure is complete.
z. Use the RESTORE option of the BACKUP utility to restore the customer's files.

16. BOOTSTRAP PROGRAMS AND IPL PROCESS

Because the VS-25/45 system does not contain any PROM-based operational microcode, all CP and BP operational microcode must be loaded into the system by the bootstrap programs. (Note that the bootstrap programs cannot coexist with the operational CP and BP code; therefore, no system-level CP/BP functions, such as Control Mode, are available while the bootstrap programs are executing).

Pressing the Initialize Button starts the bootstrap process from the disk device indicated by the 3-position Bootstrap Media switch. The bootstrap programs perform power-up initialization and diagnostic functions and then uses the Workstation 0 screen to allow the operator to select either "IPL the system" or "Run Off-line Diagnostics" from the selected IPL device.

The VS-25/45 system functions just like other VS machines once execution of the IPL text has begun. However, since the bootstrap programs do not maintain the Time of Day clock during their power-up and initialization process, the VS-25/45 will require resetting the clock after every IPL from a power off condition.

17. IPL PROCEDURE

a. Make sure the Local/Remote switch is in the Local position. (The system will not IPL if the switch is in Remote.)
b. Set the Bootstrap Media switch to the center position (select the fixed drive).
c. Press the Initialize button on the front panel. (The HEX display on the front panel will begin counting down from FFFF.) In about 45 seconds W/S 0 will display the following Menu:

```
                VS Self Test Monitor Package
                    IPL Drive Selection
                  Bootstrap Volume = SYSTEM


  Device     Capacity     Type     Volume      Status
  2270V-4    1.2 Mb       Dsket
  2220        76 Mb       Fixed    SYSTEM      Media Tolerant


          Position Cursor to Indicate Device and Select:
 ================================================================

 (ENTER) IPL                    (8) STAND-ALONE DIAGNOSTIC MONITOR
```

d. Position the cursor next to the system volume and press ENTER.
e. The Self-Test Monitor diagnostics will begin running.

```
                    VS Self Test Monitor Package
                        System Hardware Status
                        System Volume = SYSTEM

Status          Diagnostic
Passed          (SIO) Serial Data Link Test
Passed          (BP)  USART Loopback Verification Test
Passed          (CPU) CP Control Memory & CP/BP Test
Passed          (CPU) CP Random Operands Test
Passed          (CPU) CP Integrity Test
Passed          (MM)  Main Memory Integrity Test
Passed          (BP)  BP DMA & MARS Test

        Diagnostics Completed, Beginning System Initialization
```

f. If the Main Memory Integrity test fails, run the Main Memory test portion of the Stand-Alone Diagnostic Monitor to locate the failing memory chip.

g. After the Self-Test Monitor diagnostics have completed, the system will IPL. In about 75 seconds W/S 0 will display the request for information to specify the name of the configuration file.

```
***Message M0001 BY SYSGEN

                        INFORMATION REQUIRED

 Specify the name of the system configuration file and press (ENTER)
                              - or -
          Press (1) to use one workstation and one disk.

                        SYSFILE = @CONFIG@
                        SYSLIB  = @SYSTEM@


   Specify the communications configuration file to be used, if any

                        COMMFILE =
                        COMMLIB  = @SYSTEM@
```

h. Press PF1 to use one workstation and one disk. The System Generation process will begin.
i. W/S 0 will respond with a request for information required to set date and time.
j. Enter the data and time and press ENTER.
k. System Initialization will begin and in about 45 seconds W/S 0 will display the standard VS Operators Console screen, completing the process.
l. Run the GENEDIT utility and reconfigure the following:
    1. NEC drive as device type 2220.
    2. IOP #0 as a 25V02 Small Disk IOP.
    3. IOP #1 as a 25V50-0 Disk Device Adapter.
    4. Device 016 as a 22V704.
m. ReIPL the system and turn it over to the customer.

APPENDIX D

APPENDIX D

2-MEGABYTE MAIN MEMORY OPTION

PREFACE

This document is an addendum to the First Customer Shipment (FCS) Manual for the VS-15 Computer System and to the Standard (STD) Manual for VS-25/45 Computer Systems.

The purpose of this addendum is to provide the Wang-trained Customer Engineer (CE) with instructions to install, operate, checkout, and troubleshoot the 2-Megabyte Main Memory option. This addendum will be updated (or incorporated into the respective base manual) on a regular schedule.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER D1

INTRODUCTION

D1.1 SCOPE AND PURPOSE

This addendum to the VS-15 Computer System FCS manual and to the VS-25/45 Computer Systems manual provides instructions to increase the main memory capacity of the present VS-15/25/45 to either 256K, 512K, 1M, or 2M by replacing the original main memory board with a new 210-9300 Main Memory Board.

D1.2 MODEL DESCRIPTION

The 210-9300 PCB is very similar to the existing 210-7900 PCB thereby facilitating ease of installation. Because of hardware limitations, present VS-15/25/45 Systems can only support a maximum main memory size of 2-megabytes. As a result, hardware invalid memory address (IMA) detection is not supported at 2-megabytes; it simply wraps around to address zero. IMA detection is supported for the smaller sizes however.

The model structure for the main memory option is as follows:

MODEL	SIZE
210-9300-A	256K
210-9300-1A	512K
210-9300-2A	1MEG
210-9300-B	2MEG

D1.3 SOFTWARE REQUIREMENTS

Software Operating System release 6.30 is required to support operation of the 2-Megabyte Main Memory Board. The current CP5 CPU-microporgram (version 5.12.01) is adequate to support operation of the new memory board.

CHAPTER D2

THEORY OF OPERATION

Theory of operation for the 2-megabyte main memory board is not provided as part of this addendum.

CHAPTER D3

OPERATION

The 2-megabyte main memory does not require any special instructions for operation in the VS-15/25/45 Computer System.

CHAPTER D4

INSTALLATION

D4.1 GENERAL

This chapter presents information for unpacking, inspecting and installing the 2-megabyte main memory board into the VS-15/25/45 Computer System. General information concerning VS-15/25/45 installation is found in Chapter 4 of this Product Maintenance Manual.

D4.2 UNPACKING/PACKING

The 2-megabyte main memory board is packed in a shipping carton as shown in figure D4-1. Refer to figure D4-1 while performing the procedure given below.

Unpacking:

1. Before unpacking the 2-megabyte main memory board, inspect the shipping carton for damage. If any damage is noticed, notify the carrier immediately. Do not open the carton until the carriers' representative is present. If there is no apparent damage to the shipping carton, proceed to step 2.

2. Using a sharp knife, carefully cut the shipping tape used to secure the carton. Carefully open the carton and save all packaging material for reshipment, if necessary.

3. Check the contents against the shipping bill to ensure that nothing is missing or damaged.

4. Inspect the 2-megabyte main memory board for shipping damage. Any damage claims should be handled as specified in section 4 of the VS-15/25/45 Computer System manuals.

Packing

The 2-megabyte main memory board can be repackaged for shipment by reversing the steps given above.

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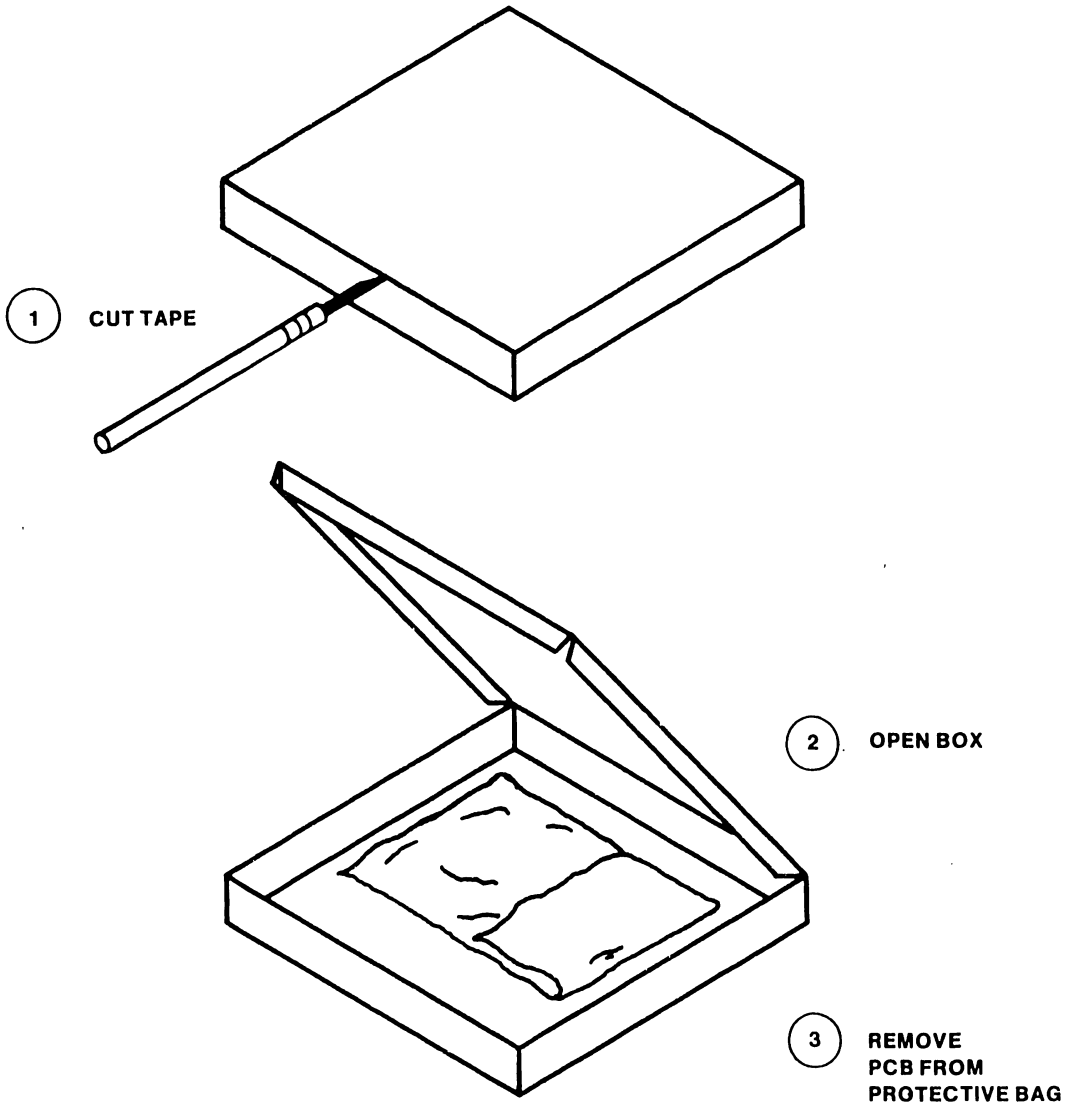


Figure D4-1 Unpacking the 2-Megabyte Main Memory Board

D4.3 SWITCH SETTINGS AND JUMPER CONFIGURATIONS

The 2-megabyte main memory board is programmed for operation via switch SW1 and jumpers JP1-JP4. SW1 defines the memory size and JP1-JP4 specify whether 64K or 256K RAM chips are used. Figure 4-2, in addition to showing the location of switch SW1 and jumpers JP1-JP4, defines memory chip loading and associated chip part numbers. Instructions for setting up the board are given below.

D4.3.1 Switch SW1

1. Verify that the correct chips are in the specified locations corresponding to the maximum memory size (see memory chip loading chart on figure 4-2).

2. Set the five switches of SW1 to define maximum memory size.

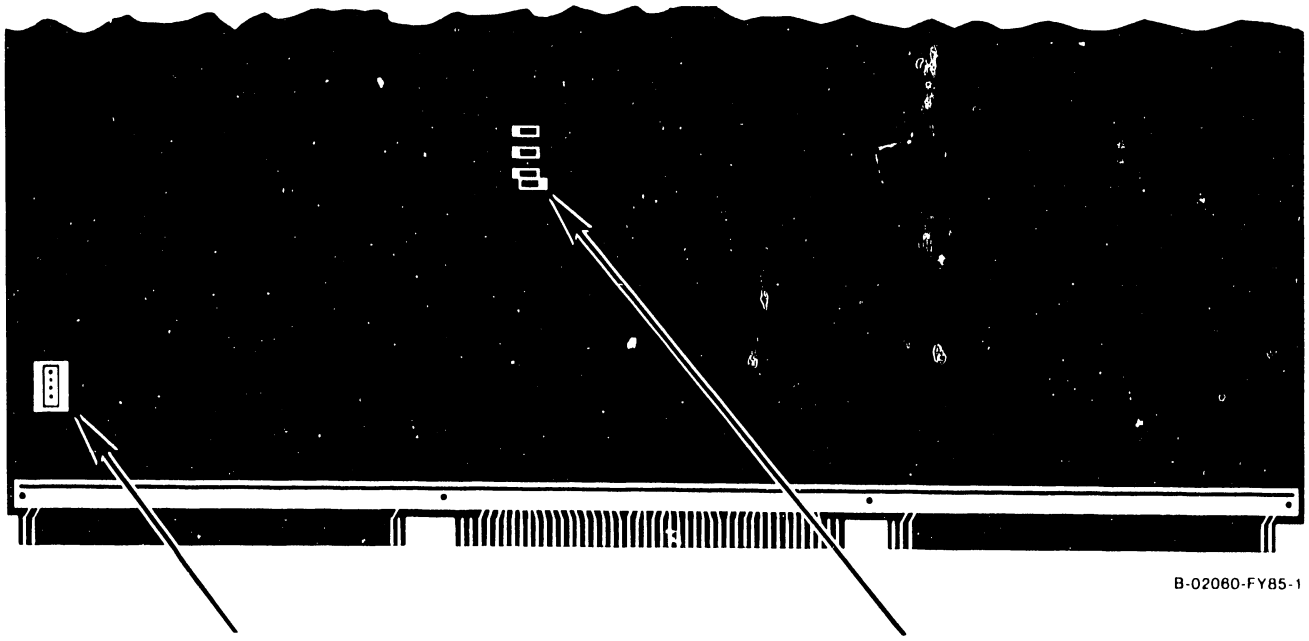
D4.3.2 Jumpers JP1-JP4

Each of the four jumpers JP1-JP4 contains three pins. Pin 1 is on the left, pin 2 in the center, and pin 3 on the right. The respective shorting plug for each jumper can be installed either between pins 1 and 2 (left) or between pins 2 and three (right). In no case is the shorting plug completely removed. Instructions for setting up jumpers JP1-JP4 are presented below.

1. Refer to the memory chip loading chart presented in figure 4-2 and determine that the memory board contains either 64K RAM chips (P/N 377-0415) or 256K RAM chips (P/N 377-0589).

2. If the board contains 64K RAM chips, connect the shorting plug for jumpers JP1, JP2, and JP3 between pins 1 and 2 (left). If the board contains 256K RAM chips, connect the shorting plug for jumpers JP1, JP2, and JP3 between pins 2 and 3 (right).

3. Install the shorting plug for jumper JP4 between pins 1 and 2 (left) for all RAM configurations.



SW1 SWITCH SETTINGS

MODEL	SIZE	1	2	3	4	5
9300-A	256K	ON	ON	ON	ON	OFF
9300-1A	512K	ON	ON	ON	OFF	OFF
9300-2A	1M	ON	ON	OFF	OFF	ON
9300-B	2M	ON	OFF	OFF	OFF	ON

JUMPER CONFIGURATIONS

JUMPER	64K RAMS	256K RAMS
JP1	PINS 1 & 2	PINS 2 & 3
JP2	PINS 1 & 2	PINS 2 & 3
JP3	PINS 1 & 2	PINS 2 & 3

JP4 IS ALWAYS JUMPERED BETWEEN PINS 1 & 2

MEMORY CHIP LOADING*

9300-A (256K) 377-0415 CHIPS IN L145-155, 158-179, 182-192

9300-1A (512K) 377-0415 CHIPS IN L97-107, 110-131, 134-155, 158-179, 182-192

9300-2A (1M) 377-0415 CHIPS IN L1-11, 14-35, 38-59, 62-83, 86-107, 110-131, 134-155, 158-179, 182-192

9300-B (2M) 377-0589 CHIPS IN L97-107, 110-131, 134-155, 158-179, 182-192

*ALL CONFIGURATIONS REQUIRE A 377-0416 CHIP IN LOCATION L220

CHIP TYPES: 377-0415 = 64K X 1
377-0416 = 16-BIT PARITY ERROR GENERATOR
377-0589 = 256K X 1

Figure D4-2 Memory Board Switch Settings and Jumper Configurations

D4.4 2-MEGABYTE MAIN MEMORY BOARD INSTALLATION

1. Power down the VS-15/25/45 by pressing the ac power on/off rocker switch to the 0 position.
2. Remove ac power cable from its outlet.
3. Remove top cover (see section 5).
4. Carefully remove the old memory board from slot 1 of the card cage (see section 5).
5. Verify new memory board switch settings and jumper configurations per section D4.3.
6. Carefully install new main memory board into slot 1 of the card cage.
7. Reinstall top cover.
8. Insert ac power cable into its outlet. Power up the CPU by depressing the ac power on/off rocker switch to the 1 position.
9. Run Diagnostics (chapter 8) to verify correct system operation.
10. Return old memory board to stock.

CHAPTER D5

PREVENTIVE AND CORRECTIVE MAINTENANCE

D5.1 GENERAL

The 2-megabyte main memory board does not require any preventive maintenance or inspection. Corrective maintenance entails running memory diagnostics and swapout replacement of the board, if defective.

CHAPTER D6

SCHEMATICS

D6.1 GENERAL

This section contains the related schematics for the 2-megabyte main memory board.

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER D7

ILLUSTRATED PARTS BREAKDOWN (IPB)

D7.1 GENERAL

If defective, the entire 2-megabyte main memory board should be swapped out and replaced as a complete unit by re-ordering under the correct part number as follows:

MODEL	SIZE
210-9300-A	256K
210-9300-1A	512K
210-9300-2A	1MEG
210-9300-B	2MEG

NOTE

The exact model number of the board to be replaced can be determined by matching up memory chip type and loading as specified in figure D4-2.

CHAPTER D8

TROUBLESHOOTING

D8.1 GENERAL

The 2-megabyte main memory board is not repaired in the field. If found defective after running system and memory diagnostics, the board is swapped out and replaced with a new one.

APPENDIX E

Appendix E

Async. Controller
25V36

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

List of Tables

CHAPTER 1

INTRODUCTION

Chapter 1 information is not provided as part of the First Customer Shipment (FCS) Manual, but will appear in the Standard Product Maintenance Manual.

CHAPTER 2

THEORY OF OPERATION

Chapter 2 information is not provided as part of the First Customer Shipment (FCS) Manual, but will appear in the Standard Product Maintenance Manual.

CHAPTER 3

OPERATION

3.1 GENERAL

This chapter provides the CE with a daily verification procedure. Only sections which directly apply to the Async. Controller have been included in this chapter. If further information is required, refer to the VS-25/45 Computer System Product Maintenance Manual.

3.6 DAILY VERIFICATION PROCEDURES

1. Power on workstation 0.
2. Place the VS-25/45 AC On/Off switch in the "On" position.
3. After approx. 5 seconds press the DC Initialize button.
4. Upon completion of the Power-up diagnostics (ref. Chapter 8 of the VS-25/45 Manual), fill in the configuration, and time/dat fields, and verify that the screen on any workstation configured through the Async. Controller appears as follows in Figure E3-1.

Wang VS Logon

Workstation 1 3:29 pm Thursday January 17, 1985

Hello new user
Welcome to the WANG VS

Please identify yourself by supplying the following information

Your userid =
Your password =

and press (ENTER) to logon

or press (PF11) to enter operator mode immediatly

Figure E3-1 Workstation Screen

5. Using a previously defined password insure that log-on is possible from the workstation.
6. If there are no errors, log off the system, and let the customer resume normal daily operation.

CHAPTER 4

INSTALLATION

4.1 GENERAL

This chapter describes the procedures for unpacking, inspecting, and installing the VS-25/45 Async. Controller. Included in this chapter are instructions for jumper setting, interconnection, and initial power-up. Refer to Chapter 3, Operation, and Chapter 5, Preventive and Corrective Maintenance and Removal/Replacement, of this manual for more information needed to complete installation. Actual installation should not begin until the site requirements detailed in the VS-25/45 Maintenance Manual have been met. Only sections which directly apply to the Async. Controller have been included in this chapter. If further information is required, refer to the VS-25/45 Computer System Product Maintenance Manual.

4.4 UNPACKING

1. Before unpacking the Controller Board and associated boards, check all packing slips to make sure that the proper equipment has been delivered.
2. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).
3. Open the boxes and remove the PC Boards as shown in Fig. E4-1.

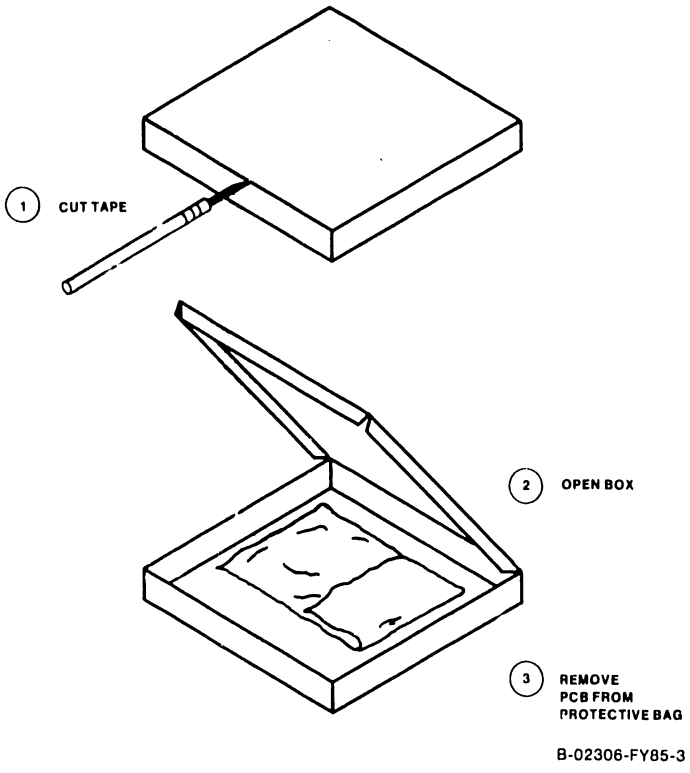


Figure E4-1 Unpacking the Async. Controller Board

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4.4.5 INSPECTION

1. Inspect the Async Controller and associated circuit boards for packing material or such shipping damage as broken connectors.
2. If damage is discovered during the inspection, follow the reporting procedure in section 4.4 of the VS-25/45 Maintenance Manual.

4.6 MINIMUM REQUIREMENTS

4.6.1 HARDWARE

Minimum requirements for hardware are listed in section 4.6 of the VS-25/45 Maintenance Manual.

4.6.2 SOFTWARE

Operating software revision 6.4X.XX is required for operation of the Async. Controller. Refer to the proper software release notice for software configuration instructions.

4.9 HARDWARE CONFIGURATION

1. Prior to installing the Async. Controller Board, verify the system address configuration. There are ten jumpers, J6 through J15 on the Controller Board, (ref. Figure E4-2) which provide I/O Addressing information to the system. Table E4-1 gives a listing of the possible address configurations and jumper settings. These jumpers must be set correctly to insure proper operation.
2. With the system power off, insert the Controller Board into an available I/O Device Adapter slot by Placing it in the board guides and lowering it to the Motherboard connector.
3. Make sure the board edge connectors are lined up with the motherboard connector slots and the snaplock tabs are under the top rails.
4. Push down on the snaplocks to seat the board in the motherboard.

CAUTION
DO NOT USE EXCESSIVE FORCE WHEN PUSHING DOWN ON THE SNAPLOCKS

5. Remove the blank "break out" panel in the rear of the machine (ref. Fig. E4-3), and using the hardware provided, attach the Async. rear panel assy.

6. Connect the Ribbon Cables as shown in Figure E4-4.

7. Attach async. peripherals to the rear panel as required.

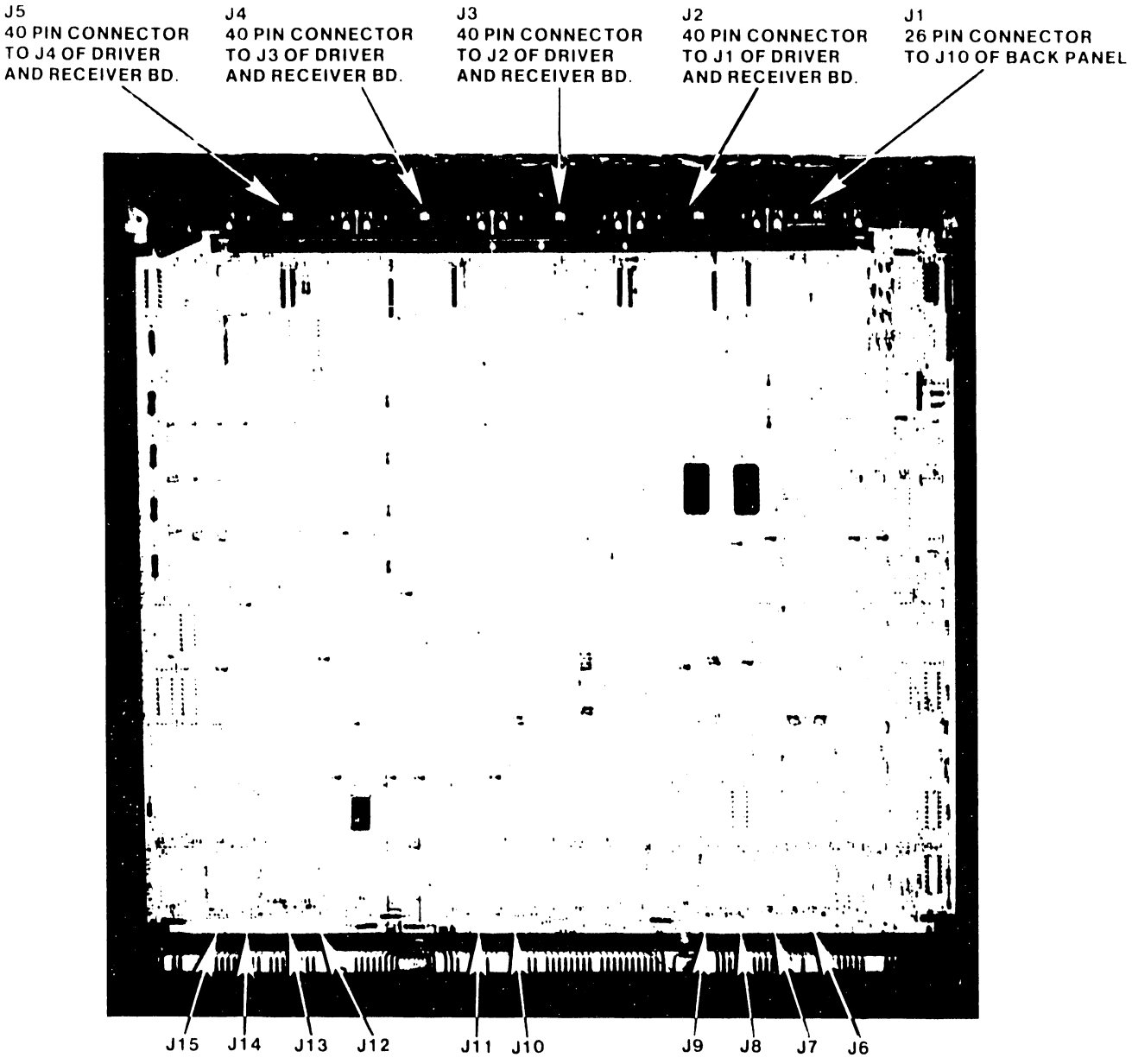


Figure E4-2 Async. Controller Board 25V36

Table E4-1 Jumper Configurations

I/O ADDRESS	J15	J14	J13	J12	J11	J10	J8	J6
600								
500								
400								
300								
200								
100								

NOTE: Remove all jumpers from J7 and J9.
These are not used at this time.

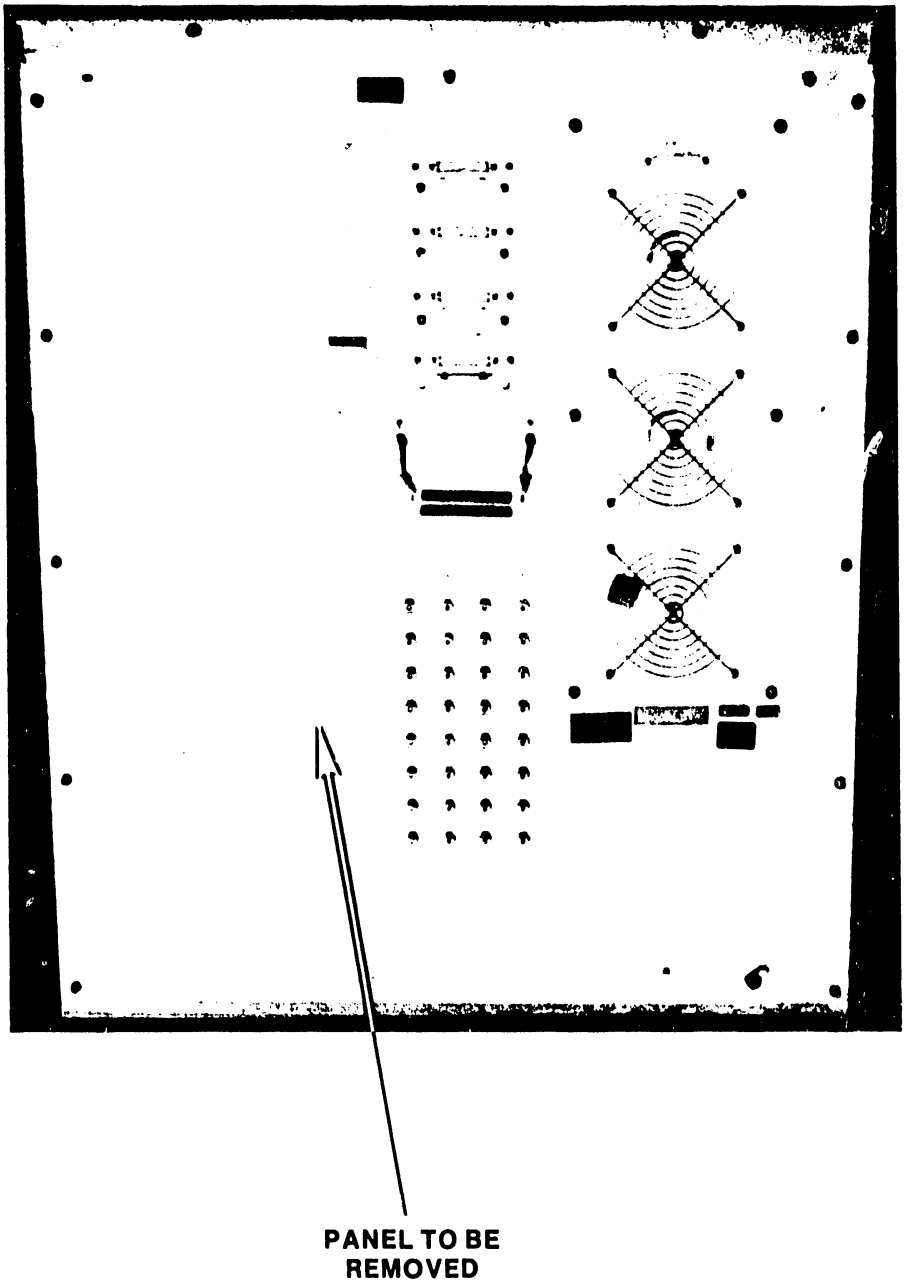
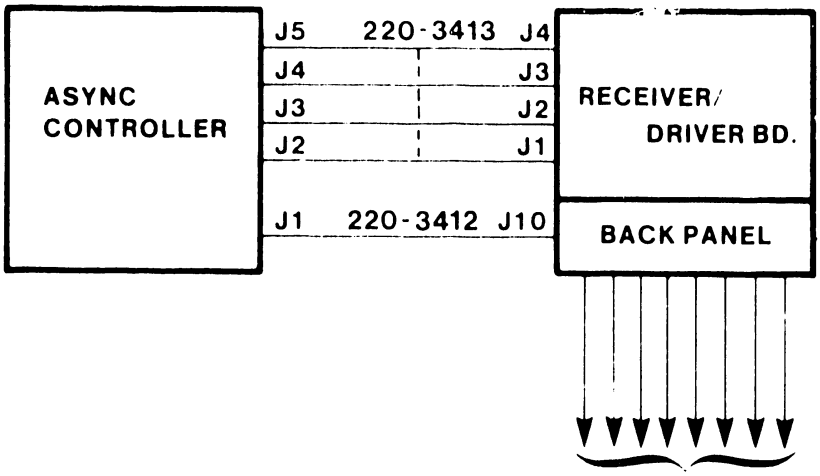
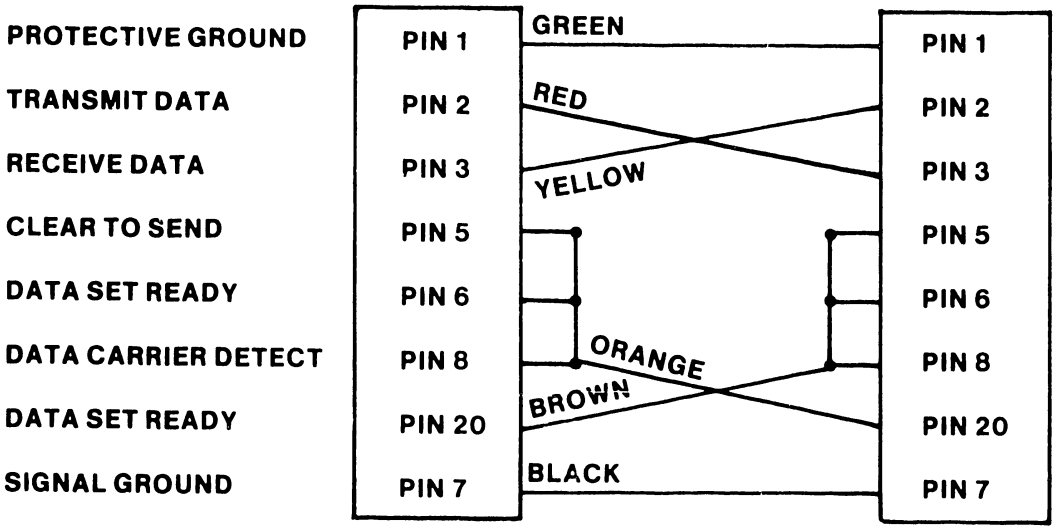


Figure E4-3 VS-25/45 Breakout Panel



RS232 INTERFACE TO WORKSTATIONS (2000 FT MAX. SEE DETAILED DRAWING BELOW) (2110 WORKSTAION CONFIGURATION SHOWN) B-02306-FY85-1



RS232 INTERFACE TO 2110 WORKSTATION

B-02306-FY85

Figure E4-4 Cable Connections

4.10 PRELIMINARY SYSTEM CHECKOUT

1. Power on all workstations currently configured into the system.
2. Place the VS-25/45 AC On/Off switch in the "On" position.
3. After approx. 5 seconds press the DC Initialize button.
4. Upon completion of the inbuilt diagnostics (see Chapter 8 of the VS-25/45 Manual), fill in the configuration, and the time/date fields, and verify that the screen on the workstations configured through the Async. Controller appear as in Figure E4-5.
5. Using a previously defined password ensure that log-on is possible from each workstation.
6. If there are no errors, log off, and turn the system over to the Customer.

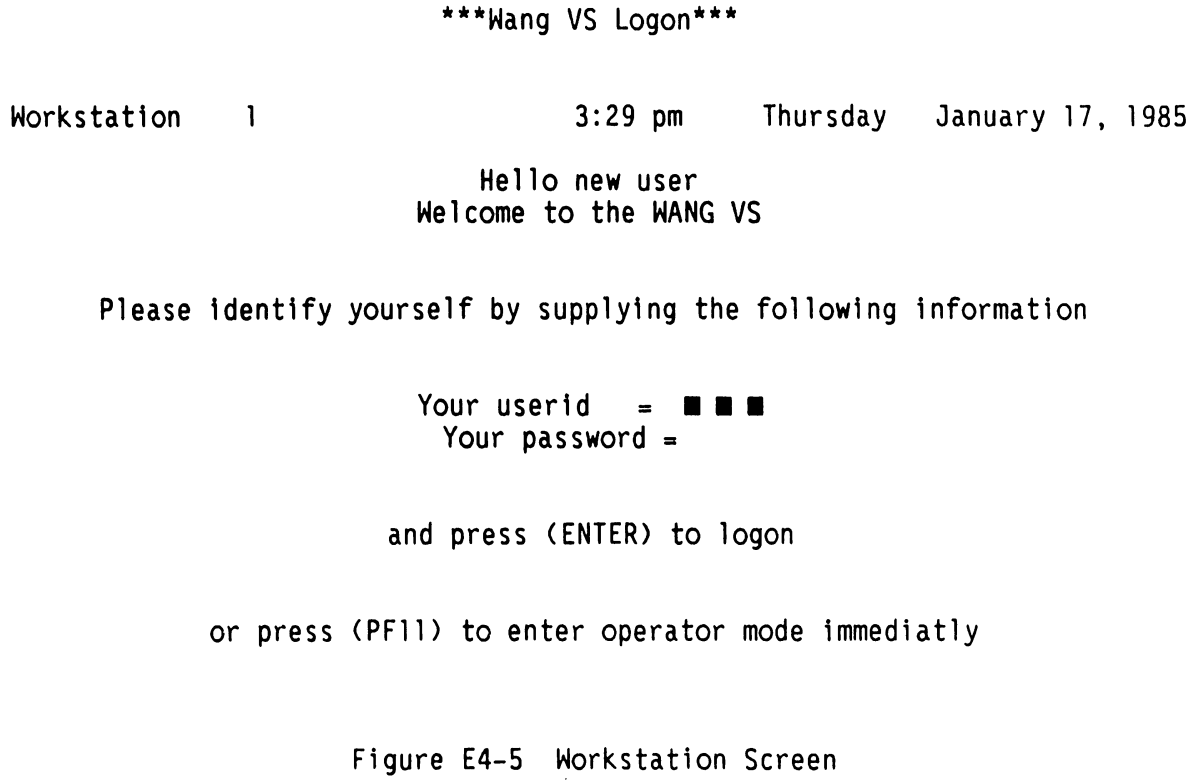


Figure E4-5 Workstation Screen

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 GENERAL

This chapter describes the procedures for the removal and replacement of the Async. Controller Board, the Line Driver and Receiver Board, and its associated Back Panel. Only sections which directly apply to the Async. Controller have been included in this chapter. If further information is required, refer to the VS-25/45 Computer System Product Maintenance Manual.

5.2 REMOVAL AND REPLACEMENT

NOTE

If the Async. Controller Bd. or the Line Driver/Receiver Daughter Bd. have been removed from the system for maintenance reasons, the contacts of the PCB's may be cleaned with an alcohol pad. Do not use an eraser.

5.2.1 Async. Controller Board Removal and Replacement

1. Insure that all users have logged off the system.
2. Press the green Control Mode Button on the VS. This prevents any disk I/O command in process from being halted prior to completion.
3. Power down the main frame by depressing the AC Power On/Off switch to the O position.
4. Remove all cabling from the Controller Board.
5. The Async. Controller Board is held in place by two snaplocks. One snaplock tab fits under the top edge of the front board cage assembly rail and the second snaplock tab fits under the top edge of the rear board cage assembly rail.
6. Remove the Controller Board from its Motherboard slot by lifting the snaplocks to free the board from its Motherboard connectors. Once the board is free of the connectors, ease it straight up in the board guides and out of the board cage.
7. To replace the Controller Board, insert it into the board guides and lower it to the Motherboard connector.
8. Make sure the board edge connectors are lined up with the Motherboard connector slots and the snaplock tabs are under the top rails.
9. Push down on the snaplocks to seat the board in the Motherboard.
10. Reconnect all cables. (Ref. Figure E4-4.)

5.2.2 Line Driver/Receiver Daughter Board Removal and Replacement

1. Insure that all users have logged off the system.
2. Press the green Control Mode Button on the VS. This prevents any disk I/O command in process from being halted prior to completion.
3. Power down the main frame by depressing the AC Power On/Off switch to the 0 position.
4. Remove all cables from the Line Driver/Receiver Daughter Board.
5. To remove the board, squeeze the locking pins in the upper corners, (ref. Fig E5-1) and lift forward and straight up.
6. To replace the board, insert it back into its motherboard connector, and gently push the board onto the locking pins such that the pins go through the holes on the board and lock into place.
7. Reconnect all cables. (Ref. Figure E4-4.)

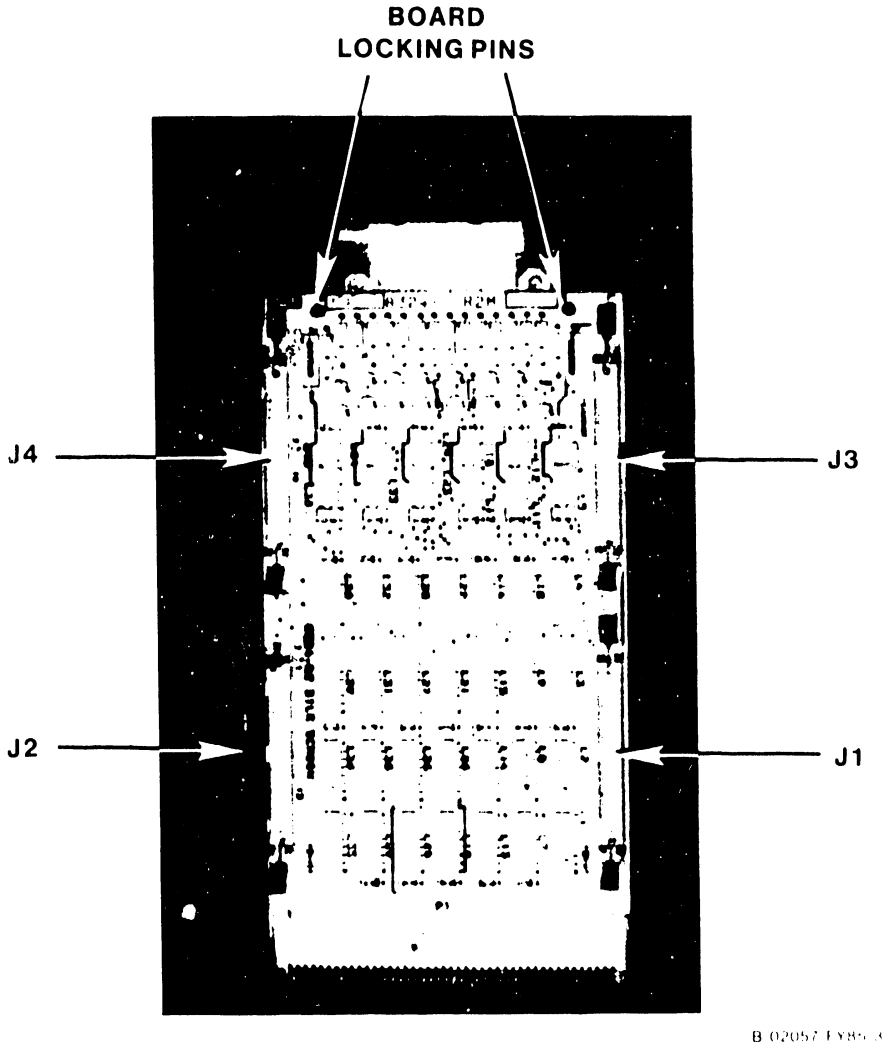


Figure E5-1 Line Driver/Receiver Daughter Board

5.2.3 Back Panel Removal and Replacement

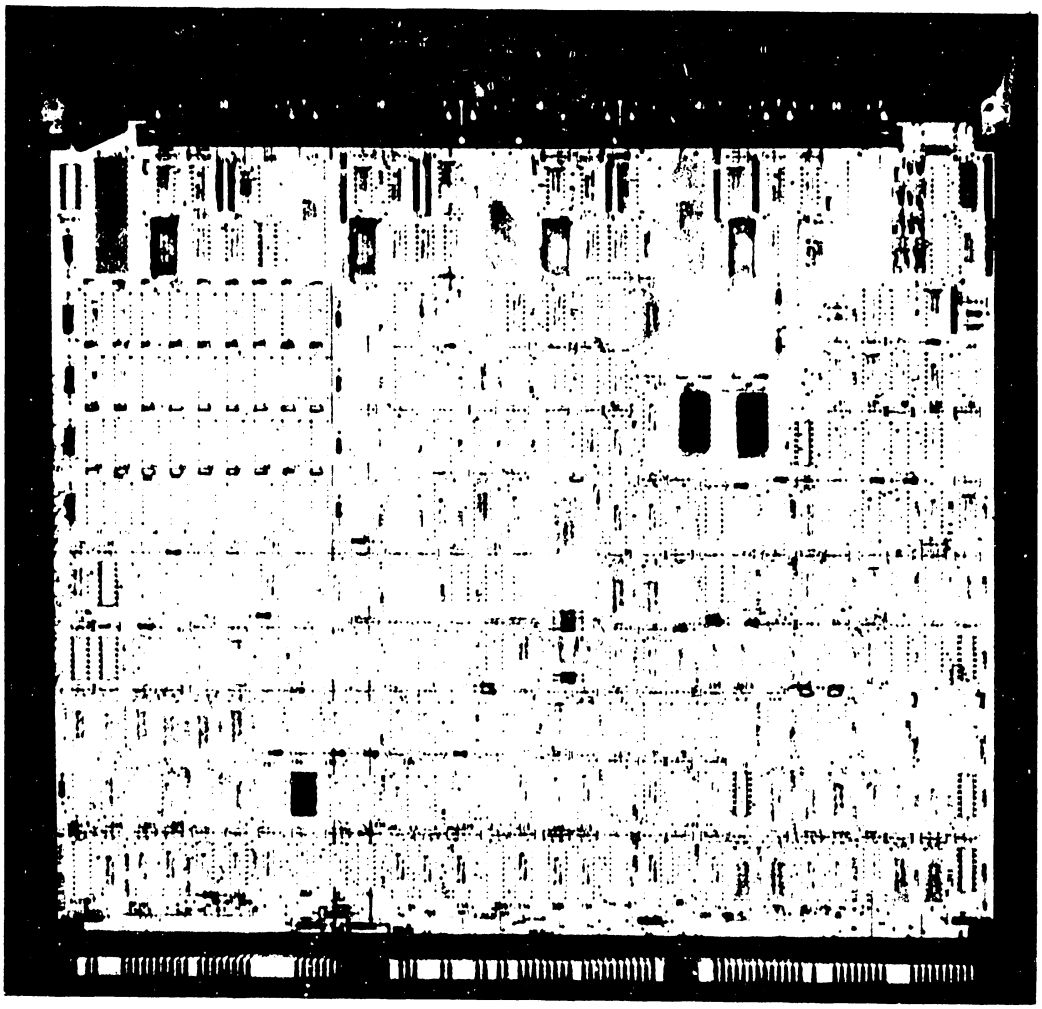
1. Insure that all users have logged off the system.
2. Press the green Control Mode Button on the VS.
3. Power down the main frame by depressing the AC On/Off switch to the 0 position.
4. Remove all cables from the Line Driver/Receiver Motherboard.
5. Remove and save all hardware holding the back panel in place.
6. Carefully lift the back panel and Motherboard out of the system.
7. To replace the back panel, insert it into the system and secure with the hardware saved in step 4.
8. Reconnect all cables. (Ref. Figure E4-4.)

CHAPTER 6

ILLUSTRATED PARTS BREAKDOWN

6.1 SCOPE

This chapter contains the illustrated parts breakdown for the VS-25/45 Async. Controller. Use this breakdown for part number identification when ordering field-replaceable components.



B 02090-FY85-3

Figure E6-1 VS-25/45 Async. Controller Board
210-7955

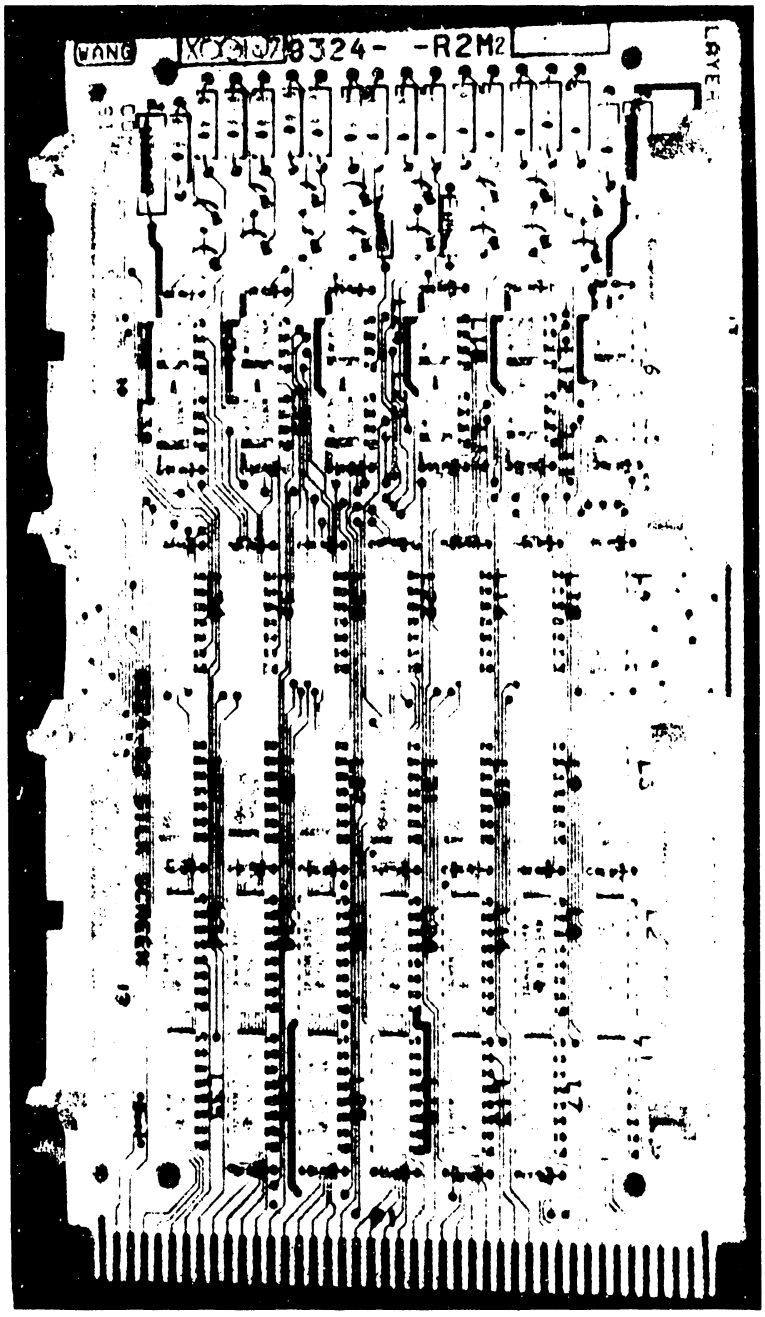


Figure E6-2 Line Driver/Receiver Daughter Board
210-8324

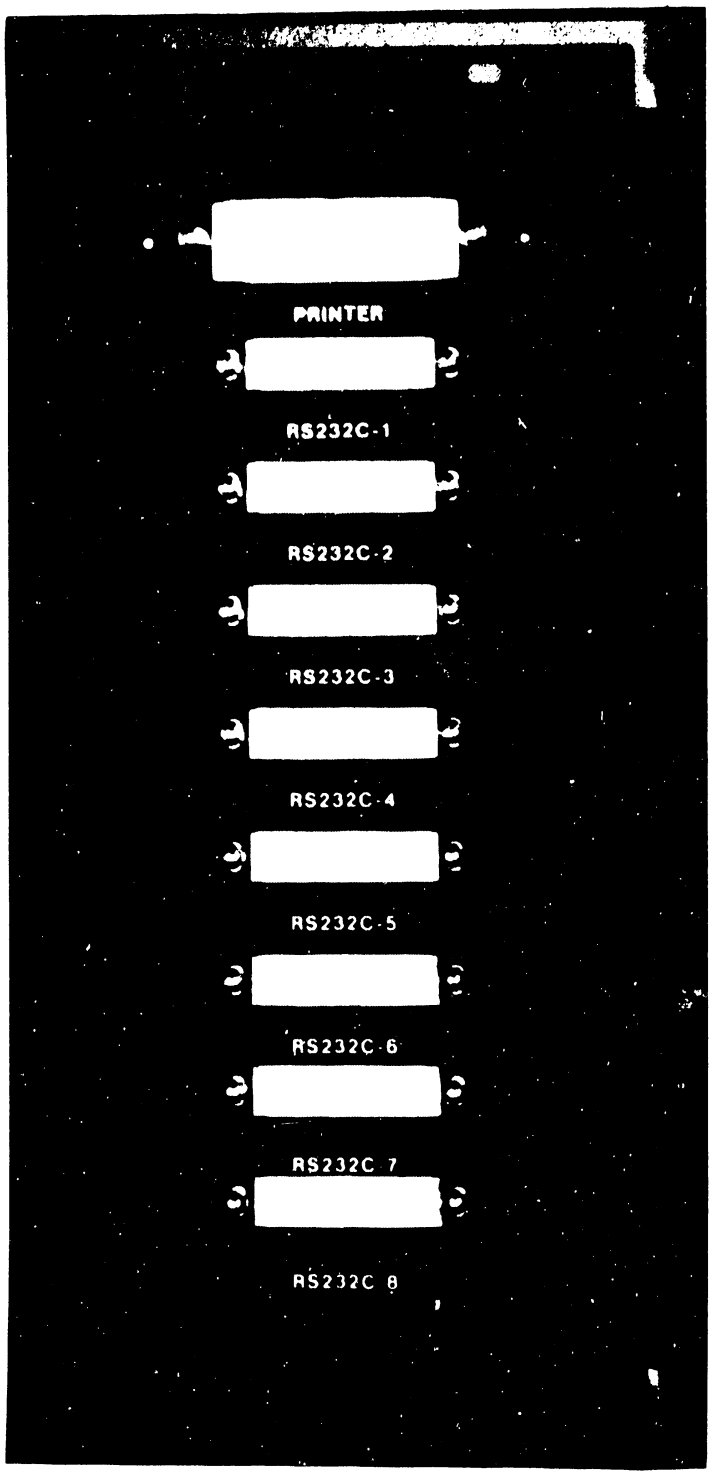


Figure E6-3 Async. Rear Panel (Includes 210-8324 Assy.)
272-0042

RECOMMENDED SPARE PARTS FOR FIELD REPLACEMENT

ITEM	PART NUMBER	DESCRIPTION
1.	210-7955	Async. Controller Board
2.	272-0042	Async. Rear Panel
3.	210-8324	Driver/Receiver Board
4.	220-3413	Forty pin ribbon cable
5.	220-3412	Twenty-six pin ribbon cable

CABLING PART NUMBERS

2110 WORKSTATION CABLING

FEET	PART NUMBER
25	220-0521
50	120-2381-01
100	120-2381-02
500	120-2381-03
1000	120-2381-04
2000	120-2381-05

RS 232-C TC CABLING

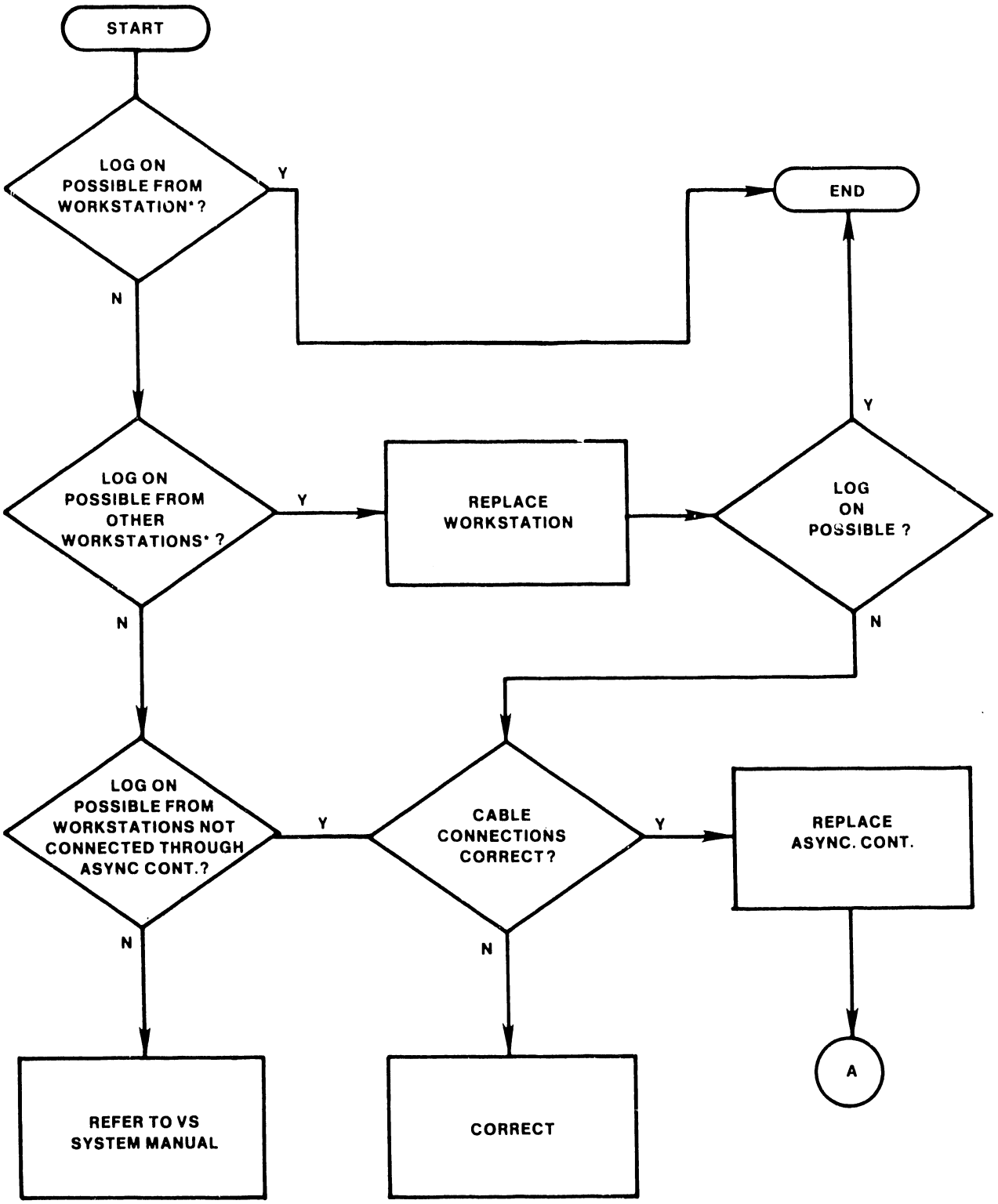
FEET	PART NUMBER
12	220-0113
25	220-0219
50	220-0220

CHAPTER 7

TROUBLESHOOTING

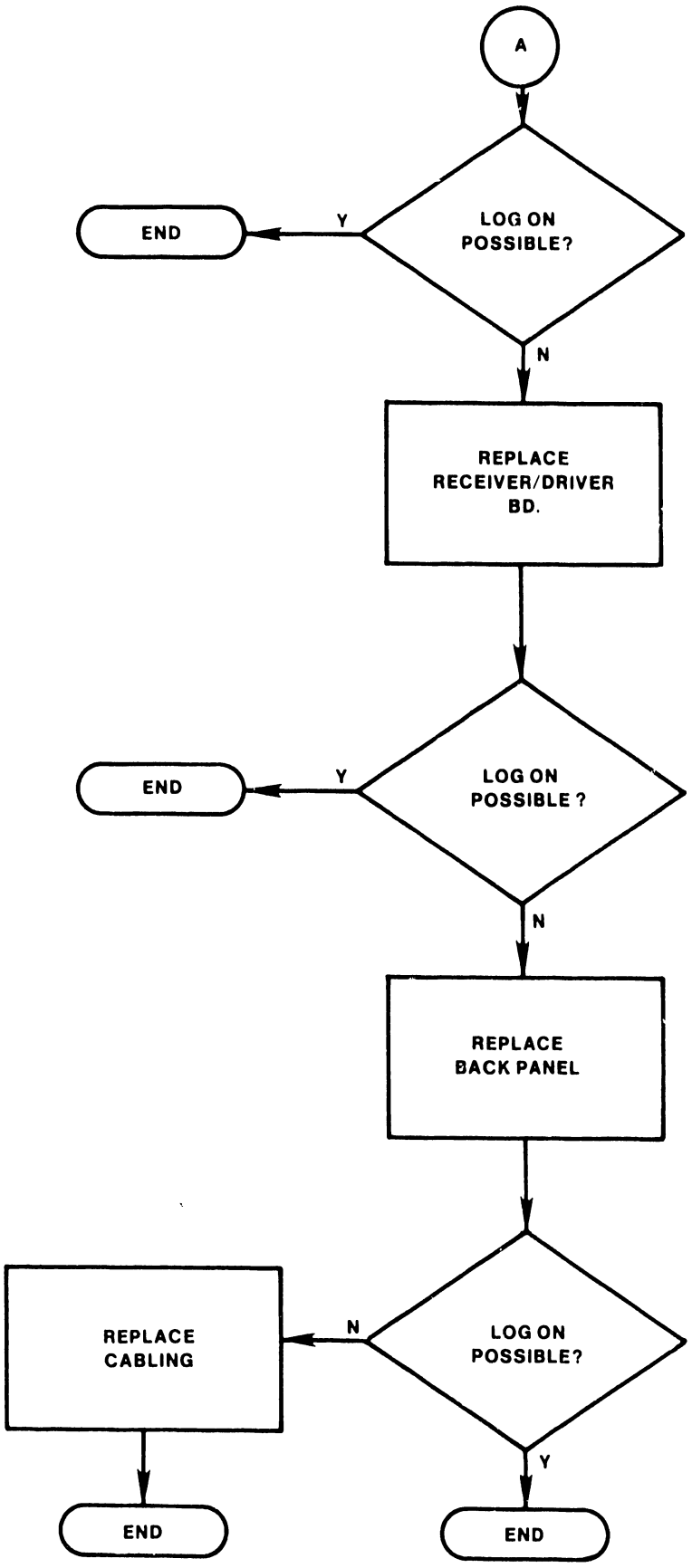
GENERAL

This chapter provides guidelines, in flowchart form, for isolating fault locations of field replaceable (or repairable) units.



* DENOTES DEVICE CONFIGURED THROUGH THE ASYNC CONTROLLER

B-02315-FY85-1



B-02315-FY85-3

CHAPTER 8

SCHEMATICS

The schematics for the Async. Controller Board (210-7155), the Line Driver and Receiver Motherboard (210-8323), and the Line Driver and Receiver Daughterboard (210-8324) may be found in the microfiche version of the VS-25/45 Product Maintenance Manual.

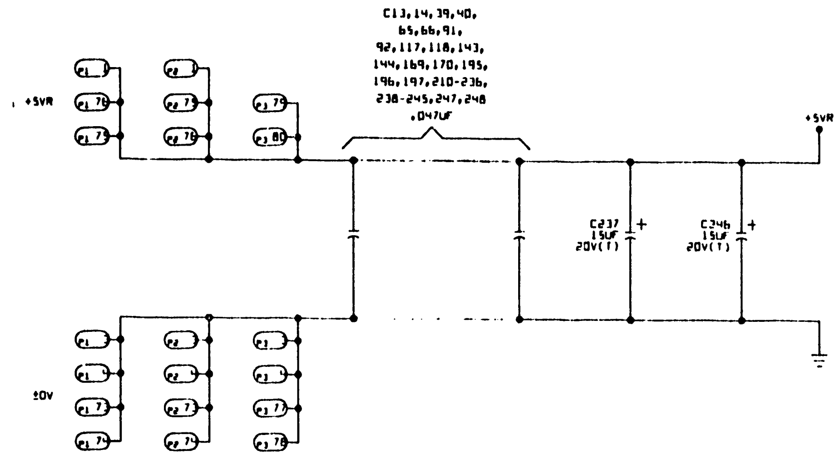
THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

APPENDIX D

SCHE-
MATICS

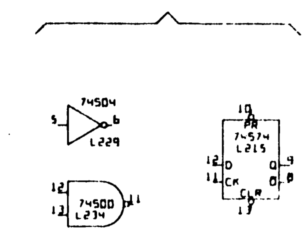
NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



MNEMONICS	COORD.
ECNT	2A7
BS	2H14
MA0	2C14
MA1-MA16	3J14
MA17	3H14
MA18-MA21	2D14
MCB0-MCB2	2C14
MDS	2A7
MD0-MD3	3B14
MD4-MD7	3C14
MD8-MD11	3D14
MD12-MD15	3F14
MGS0-MGS7	2K1
MR10-MR17	2J14
MSB0	2A8
MSB1	2A7
REXT	2A8

SPARES



210 • 209 • 377 OR 378																	
210	209	L1-11, 14-24	L25-35, 38-48	L49-59, 62-72	L73-83, 86-96	L97-107, 110-120	L121-131, 134-144	L145-155, 158-168	L169-179, 182-192	L220	C2-12, 15-25	C28-38, 41-51	C54-64, 67-77	C80-90, 93-103	C106-116, 119-129	C132-142, 145-155	C158-168, 171-181	C184-194, 198-208
9300-A (256K)	9300							377-0415	377-0415	377-0416							300-1833	300-1833
9300-1A (512K)	9300-1					377-0415	377-0415	377-0415	377-0415	377-0416					300-1833	300-1833	300-1833	300-1833
9300-2A (1M)	9300-2	377-0415	377-0415	377-0415	377-0415	377-0415	377-0415	377-0415	377-0415	377-0416	300-1833	300-1833	300 1833	300-1833	300-1833	300-1833	300-1833	300-1833
9300-B (2M)	9300-3					377-0589	377-0589	377-0589	377-0589	377 0416					300-1833	300-1833	300-1833	300-1833

NO	REVISION	DATE	BY
A	ORIGINATED PER DWR NO. E22292 APPR	7-24-84	JSH
B	REVISED PER DCR NO. 00477 DCR-R NO. 00210 CHKR	8-27-84	JSH
1	REVISED PER ECO NO. 33990 CHKR	12-3-84	A.A.B

0 N

WANG LABORATORIES, INC.

SCHEMATIC DIAGRAM

TITLE 4 MEG BYTE MEMORY M/L

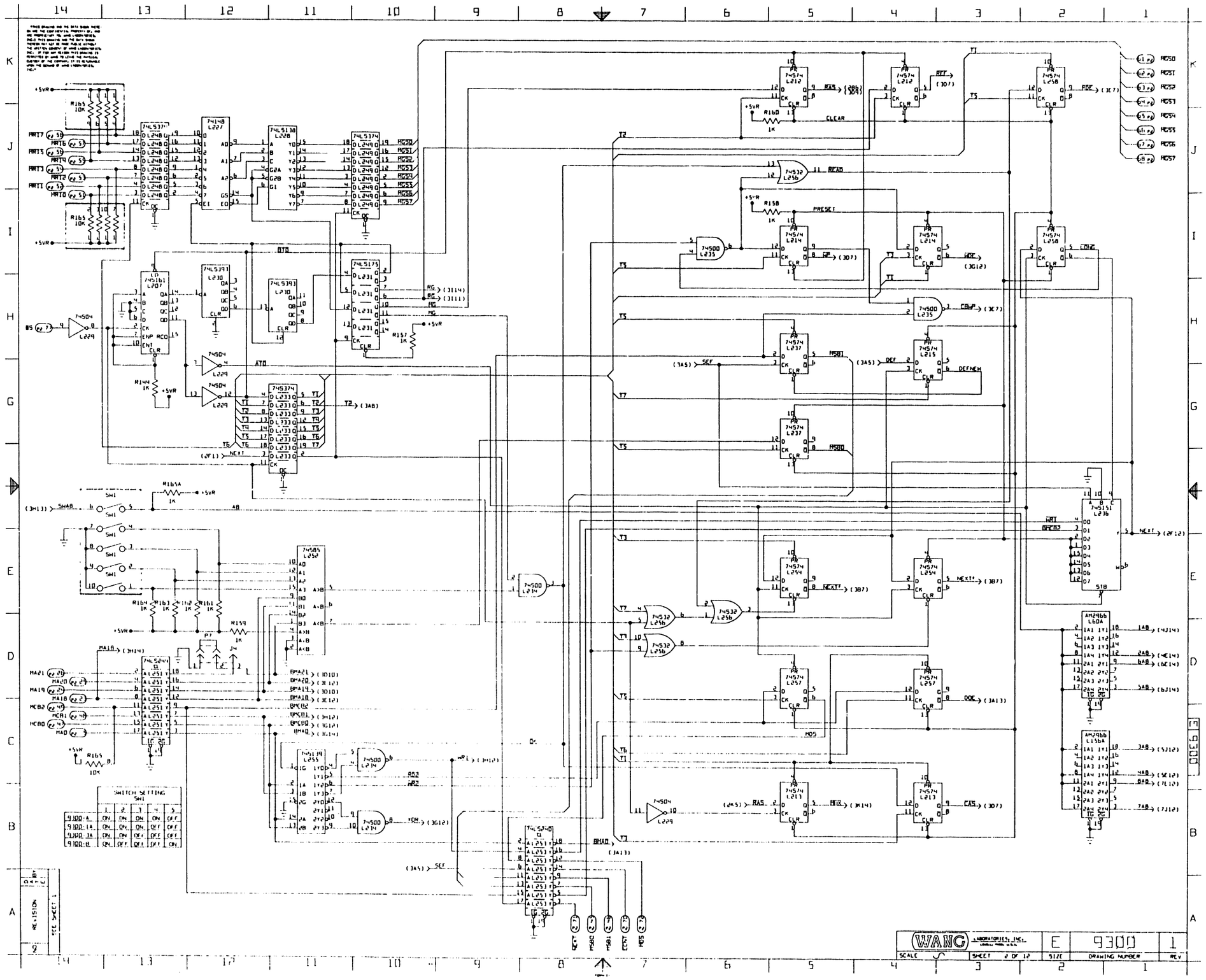
MODEL NUMBER VS 25

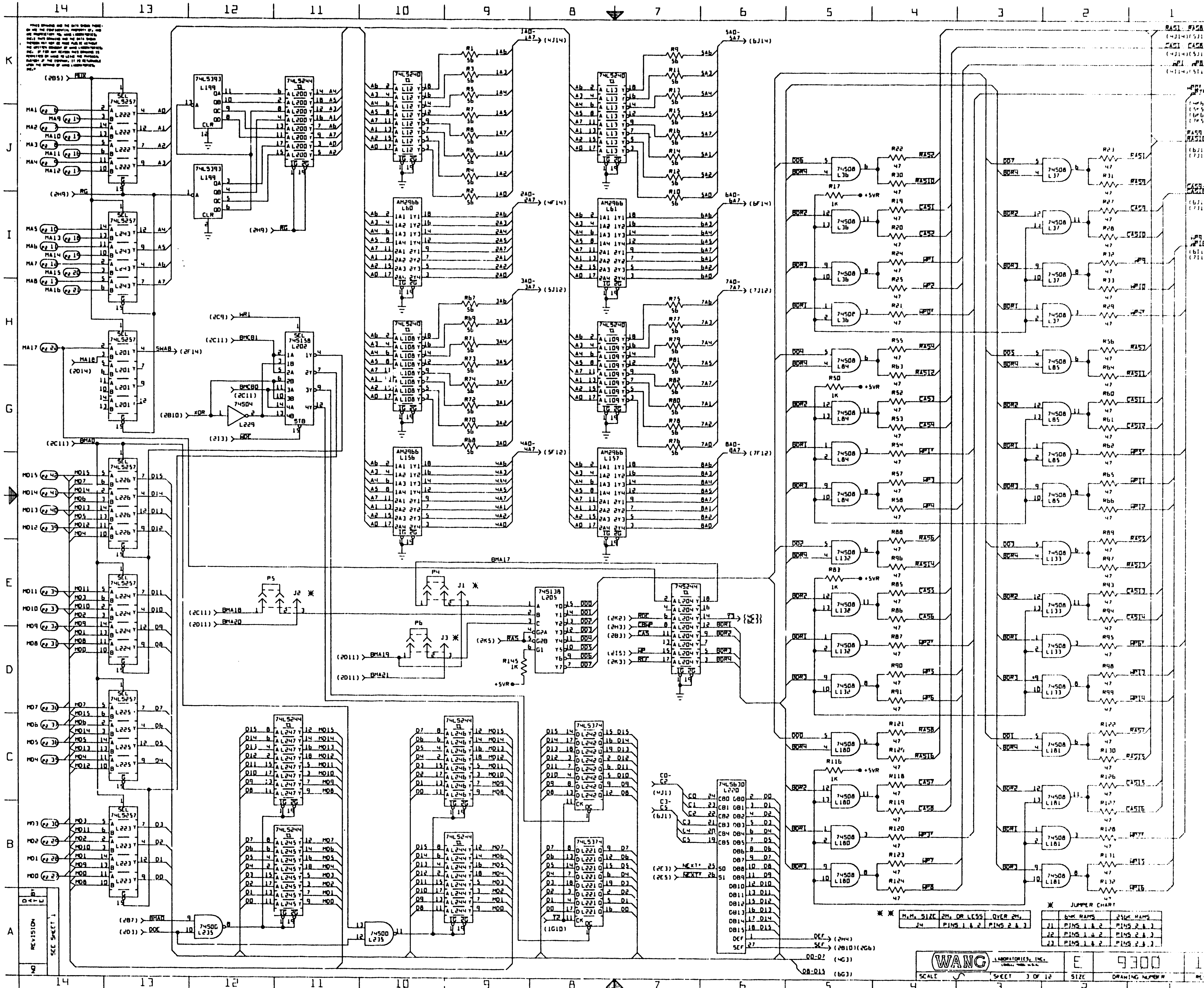
WANG PART NUMBER 210-9300

DWN JSH CHK ENG JP DIR

SIZE E DRAWING NUMBER 9300 REV 1

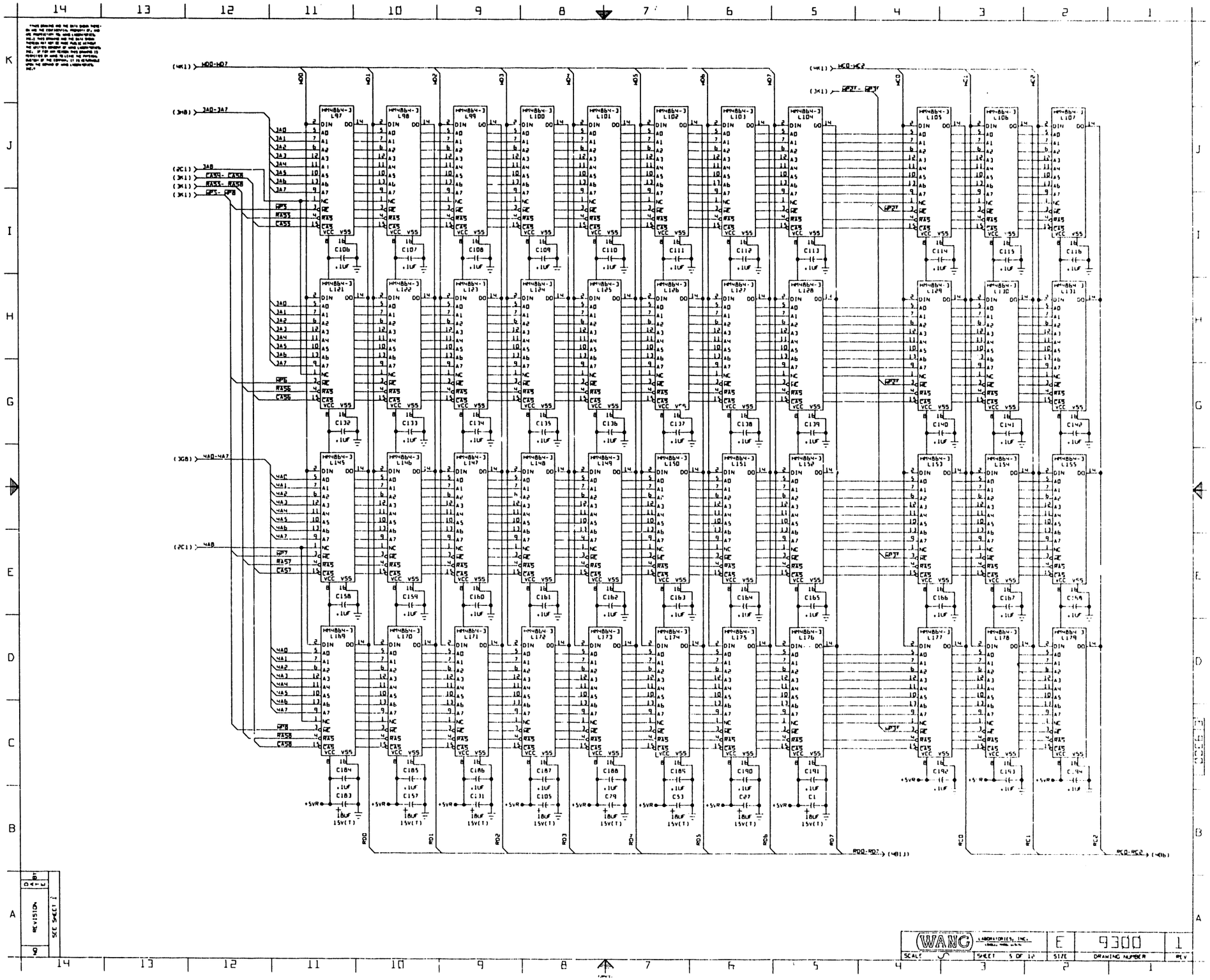
SCALE SHEET 1 OF 12


SWITCH SETTING SW1
WANG LABORATORIES, INC.
SCALE
SHEET 2 OF 12
SIZE E
DRAWING NUMBER 93000
REV 1
REVISION
SEE SHEET 1


WANG
LABORATORIES, INC.
E
9300
1
SCALE
SHEET 3 OF 12
SIZE
DRAWING NUMBER
REV
JUMPER CHART
REVISION
SEE SHEET 1

NO	REVISION	BY	DATE
	SEE SHEET 1		

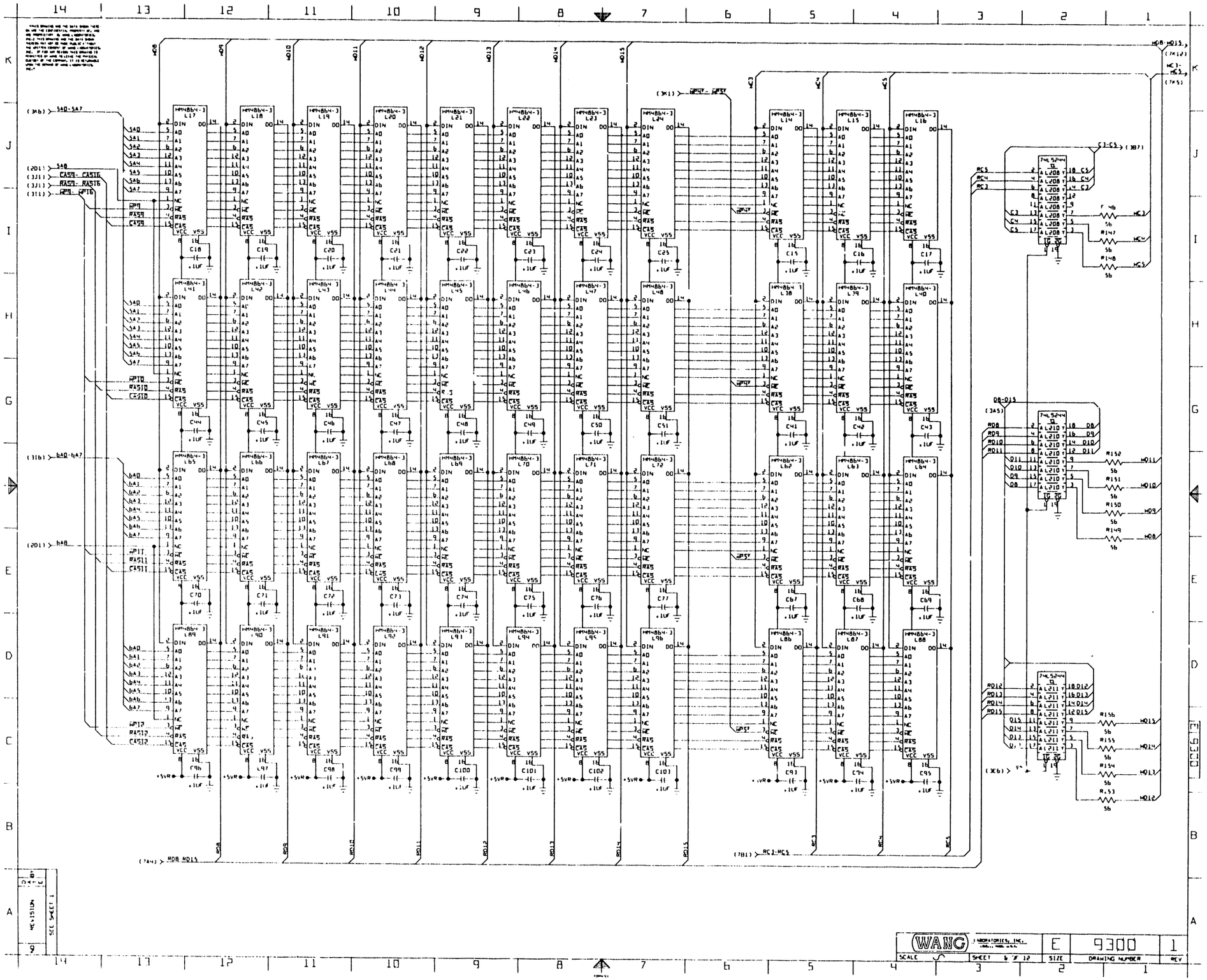
WANG LABORATORIES, INC.			
SCALE	SHEET 4 OF 12	SIZE E	DRAWING NUMBER 9300 REV 1

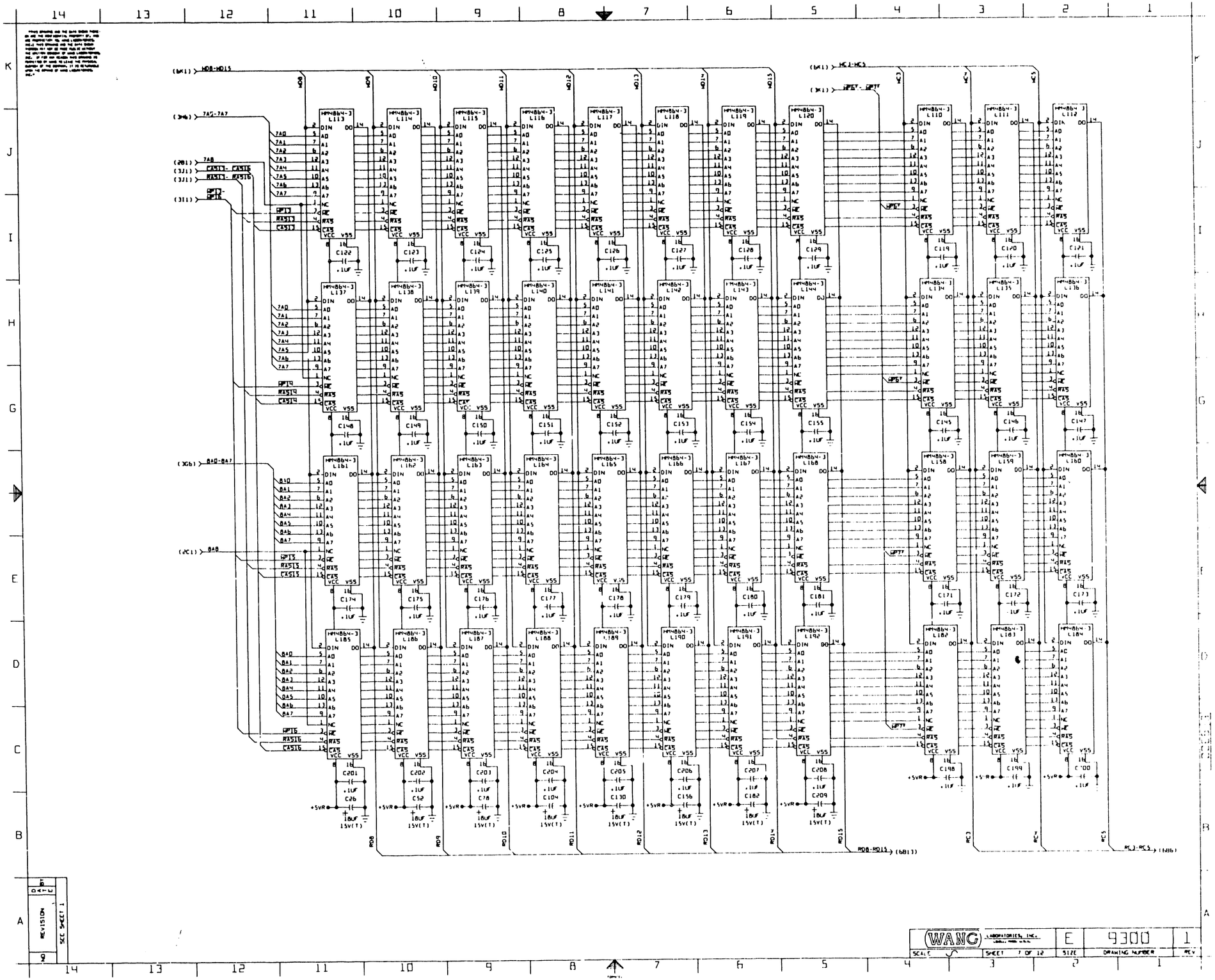


WANG LABORATORIES, INC.		E	9300	1
SCALE	SHEET 5 OF 12	SIZE	DRAWING NUMBER	REV

REVISION | DATE | BY | TO

SEE SHEET 2


MD0-MD15
MC1-MC5
SA0-SA7
BA0-BA7
CAS0- CAS1
RAS0- RAS1
WE
RP9
RP10
RP11
RP12
C1-C5
DB-D15
R146
R147
R148
R152
R151
R150
R149
R156
R155
R154
R153
74LS244
MD0 MD15
RC1-RC5
SEE SHEET 1
REVISION
WANG LABORATORIES, INC.
SCALE
SHEET 6 OF 12
SIZE
E
9300
DRAWING NUMBER
1
REV



WANG LABORATORIES, INC.		E	9300	1
SCALE	SHEET 7 OF 12	SIZE	DRAWING NUMBER	REV

DATE	BY
REVISION	
NO	SEE SHEET 1

WANG LABORATORIES, INC. RUN DATE: 12/17/84 14:48

>>>>> ELECTRICAL PARTS LIST <<<<< SHEET OF PAGE 1

(FINAL PARTS LIST)

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L
ASSEMBLY LEVEL & TITLE: 209 PCA VS SM SYS 256K MEM
PARTS LIST REVISION (P): 1
ARTWORK REVISION (B): 50
ASSEMBLY REVISION (A): 01
SCHEMATIC REVISION (S): 01
DWR OR MOST RECENT ECO: 33990D
CREATED: 07/12/84 14:58
LAST MODIFIED: 12/17/84 14:02 BY: RS
EDITING REVISION: 18

* REF. DES.	* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *
C155 - C168 C171 - C181 C184 - C194 C198 - C208	200-1833-	.1U	CAP CERAMIC MONO AXIAL LEADED +80%-20% 50V Z5U		44
C13 - C14 C39 - C40 C65 - C66 C91 - C92 C117 - C118 C143 - C144 C169 - C170 C195 - C197 C210 - C136 C238 - C145 C247 - C248	340-1966-	.047U	CAP CERAMIC MONO AXIAL +80 -20% 50V Z5U		54
C1 C26 - C27 C52 - C53 C78 - C79 C104 - C105 C130 - C131 C156 - C157 C182 - C183 C209	300-4018-	18U	CAP TANT AXIAL 10% 15V		16
C237 C246	300 4022-	15U	CAP TANT AXIAL 10% 20V		2
SW1	325-1501-	SWITCH	SLIDE SPST 5 POS		1
R19 - R25 R27 - R33 R52 - R58 R60 - R66 R85 - R91 R93 - R99 R118 - R124 R126 - R132	330-1048-	47.000	RES FIXED METAL FILM 1/4W 5% 200PPM		56
R1 - R16 R67 - R82	330-1057-	56.000	RES FIXED METAL FILM 1/4W 5% 200PPM		54

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L SCHEMATIC REVISION (S): 01 SHEET OF PAGE 3

* REF. DES.	* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *
L60 L60A L61 L156 L156A L157	376 0553-	AM2966	IC OCTAL DYN MEM DRIVER W/3-ST OUT		6
L220	376 9015-	SKT 28	IC SOCKET 28 PIN DIL MOUNT		1
L145 - L155 L158 - L179 L182 - L192	377 0415-	4164	IC 64KX1 DRAM 200NS REF REQUIRE 4MS/256 ROW		44
@3	452-2707-	STIFFN	STIFFENER LOWER		1
@2	452-2708-	STIFFN	STIFFENER UPPER		1
@26 - @27	465-1238-	EXTRCTOR	EXTRACTOR		2
@1	510-9300-		PCB		1
@4 - @10	650-2083-	SCREW	SCREW		7
@18 - @24	652-2004-	NUT	NUT		7
@11 - @17	653-2009-	WASHER	WASHER		7
J1 - J4	654-0104-	1 CONT	CONN PC HEADER SINGLE ROW .100		4
@25	660-0341-	L.T.	LOCK TITE (QTY FOR THIS A/R)		1

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L SCHEMATIC REVISION (S): 01 SHEET OF PAGE 2

* REF. DES.	* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *
R133 - R143 R146 - R166 R17 R50 R83 R116 R144 - R145 R167 - R164 R168A	330-3011-	1K	RES FIXED METAL FILM 1/4W 5% 200PPM		15
R168	333-0809-	10.000K	RESISTOR NETWORK TYPE: 10/09/C/SS		1
P4 - P7	380-4506-	2 CONT	CONN SHUNT .100 CTR		4
L231	376-0160-	74LS175	IC QUAD D-TYPE FLIP-FLOP		1
L227	376-0171-	74148	IC 8-LINE-TO-3-LINE OCTAL PRIORITY ENCODER		1
L229	376-0197-	74S04	IC HEX INVERTER		1
L36 - L37 L84 - L85	376-0200-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES		8
L132 - L133 L180 - L181 L212 - L218 L237 L256 L257 - L258	376-0202-	74S74	IC DUAL D-TYPE POS EDGE TRIGRD F/F W/PRESET/C		8
L201 L222 - L226 L243	376-0204-	74LS257	IC QUAD 2-LINE TO 1-LINE DATA SEL/MUX		7
L256	376-0208-	74S32	IC QUAD 2-INPUT OR GATE		1
L234 - L238	376-0228-	74S00	IC QUAD 2-INPUT NAND GATE		2
L252	376-0259-	74S85	IC 4-BIT MAGNITUDE COMPARATOR		1
L207	376-0278-	74S161	IC SYN 4-BIT BINARY COUNTER W/DIRECT CLEAR		1
L221	376-0286-	74LS374	IC OCTAL D-TYPE FLIP-FLOP TRI-STATE		4
L242 L248 - L249 L196 - L198 L200 L208 L210 - L211 L244 - L247 L251	376-0288-	74LS244	IC OCTAL BUFFER/LINE DRIVER W/TRI STATE		12
L228	376-0294-	74LS138	IC 3-LINE TO 8-LINE DECODER/MULTIPLEXER		1
L12 - L13 L108 - L109	376-0297-	74LS240	IC OCTAL BUFFER/LINE DRIVER/LINE RECEIVER		5
L253 L205	376-0298-	74S138	IC 3-LINE TO 8-LINE DECODER/MULTIPLEXER		1
L202	376-0301-	74S158	IC QUAD 2 TO 1-LINE DATA SELECTOR/MUX INVERT		1
L233	376-0305-	74S374	IC OCTAL D-TYPE EDGE-TRIG F/F TRI-STATE		1
L199 L230	376-0307-	74LS393	IC DUAL 4-BIT BINARY COUNTER		2
L255	376-0333-	74S139	IC 2 TO 4-LINE DECODER/MULTIPLEXER		1
L236	376-0336-	74S151	IC 1 OF 8 DATA SEL/MUX		1
L204	376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI-STATE		1

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L SCHEMATIC REVISION (S): 01 SHEET OF PAGE 4

* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *

(CAUTION - THE FOLLOWING PARTS/COMPONENTS CONTAINED IN THIS B.O.M. ARE NOT RECOMMENDED FOR NEW DESIGNS)

376-0197-	74S04	IC HEX INVERTER	1
376-0200-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES	8
376-0202-	74S74	IC DUAL D-TYPE POS EDGE TRIGRD F/F W/PRESET/C	8
376-0205-	74S32	IC QUAD 2 INPUT OR GATE	1
376-0228-	74S00	IC QUAD 2-INPUT NAND GATE	2
376-0298-	74S13A	IC 3-LINE TO 8 LINE DECODER/MULTIPLEXER	1
376-0301-	74S158	IC QUAD 2 TO 1-LINE DATA SELECTOR/MUX INVERT	1
376 0305-	74S374	IC OCTAL D TYPE EDGE TRIG F/F TRI STATE	1
376-0333-	74S139	IC 2 TO 4-LINE DECODER/MULTIPLEXER	1
376-0336-	74S151	IC 1 OF-8 DATA SEL/MUX	1
376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI-STATE	1

*** END-OF-REPORT ***

WANG	WANG LABORATORIES, INC. LOWELL, MA U.S.A.	BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO.			MFG ENGR	
	SEE ENGRG SPECIFICATIONS No.	TITLE 4 MEG BYTE MEMORY			
FINISH	TOL. UN. AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' REMOVE BURRS	210-9300	C	9300	1
	SCALE NOT TO SCALE	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

(FINAL PARTS LIST)

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L
ASSEMBLY LEVEL & TITLE: 209-1 PCA VS SM SYS 512K MEM ML
PARTS LIST REVISION (P): 1
ARTWORK REVISION (R): 00
ASSEMBLY REVISION (A): 01
SCHEMATIC REVISION (S): 01
DWR OR MOST RECENT ECO: 339900
CREATED: 07/12/84 14:58
LAST MODIFIED: 12/17/84 14:02 BY: MS
EDITING REVISION: 13

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
C106 - C116 C119 - C129 C132 - C142 C145 - C155 C158 - C168 C171 - C181 C184 - C194 C198 - C208	300-1833-	.1U	CAP CERAMIC MONO AXIAL LEADED +80%-20% 50V Z5U		88
C13 - C14 C39 - C40 C65 - C66 C91 - C92 C117 - C118 C143 - C144 C169 - C170 C195 - C197 C210 - C236 C238 - C245 C247 - C248	300-1966-	.047U	CAP CERAMIC MONO AXIAL +80 -20% 50V Z5U		14
C1 C26 - C27 C52 - C53 C78 - C75 C104 - C105 C130 - C131 C156 - C157 C182 - C183 C209	300-4018-	18U	CAP TANT AXIAL 10% 15V		16
C237 C246	300-4022-	15U	CAP TANT AXIAL 10% 20V		2
SW1	325-1501-	SWITCH	SLIDE SPST 5 POS		1
R19 - R25 R27 - R33 R52 - R58 R60 - R66 R85 - R91 R93 - R99	330-1048-	47.000	RES FIXED METAL FILM 1/4W 5% 200PPM		56

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
R110 - R124 R126 - R132 R1 - R16 R67 - R82 R133 - R143 R146 - R158	330-1067-	56.000	RES FIXED METAL FILM 1/4W 5% 200PPM		54
R17 R59 R83 R116 R144 - R145 R167 - R164 R165A	330-3011-	1K	RES FIXED METAL FILM 1/4W 5% 200PPM		16
R165	333-0889-	10.000KW	RESISTOR NETWORK TYPE: 10/09/C/SS		1
P6 - P7	380-4506-	2 CONT	CONN SHUNT .100 CTR		4
L231	376-0160-	74LS175	IC QUAD D-TYPE FLIP-FLOP		1
L227	376-0171-	74148	IC 8-LINE TO 3-LINE OCTAL PRIORITY ENCODER		1
L229	376-0197-	74S04	IC HEX INVERTER		1
L36 - L37	376-0208-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES		8
L84 - L86 L132 - L133 L180 - L181					
L212 - L218 L237 L256	376-0282-	74S74	IC DUAL D-TYPE POS EDGE TRIGRD F/F W/PRESET/C		8
L257 - L258 L201 L222 - L226 L243	376-0204-	74LS257	IC QUAD 2-LINE TO 1-LINE DATA SEL/MUX		7
L256	376-0205-	74S32	IC QUAD 2-INPUT OR GATE		1
L234 - L235	376-0228-	74S00	IC QUAD 2-INPUT NAND GATE		2
L252	376-0259-	74S85	IC 4-BIT MAGNITUDE COMPARATOR		1
L207	376-0278-	74S161	IC SYN 4-BIT BINARY COUNTER W/DIRECT CLEAR		1
L221 L242 L248 - L249	376-0286-	74LS374	IC OCTAL D-TYPE FLIP-FLOP TRI STATE		4
L196 - L198 L200 L208 L210 - L211 L244 - L247 L251	376-0288-	74LS244	IC OCTAL BUFFER/LINE DRIVER W/TRI STATE		12
L228 L12 - L13 L108 - L109 L253	376-0294- 376-0297-	74LS138 74LS240	IC 3-LINE TO 8-LINE DECODER/MULTIPLEXER IC OCTAL BUFFER/LINE DRIVER/LINE RECEIVER		1 5
L205	376-0298-	74S138	IC 3-LINE TO 8-LINE DECODER/MULTIPLEXER		1
L202	376-0301-	74S158	IC QUAD 2 TO 1-LINE DATA SELECTOR/MUX INVERT		1
L233	376-0305-	74S374	IC OCTAL D TYPE EDGE TRIG F/F TRI STATE		1
L199	376-0307-	74LS393	IC DUAL 4 BIT BINARY COUNTER		2

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
L210					
L255	376-0333-	74S139	IC 2 TO 4-LINE DECODER/MULTIPLEXER		1
L236	376-0336-	74S151	IC 1-OF-8 DATA SEL/MUX		1
L204	376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI-STATE		1
L60	376-0553-	AM2966	IC OCTAL DYN MEM DRIVER W/1-ST OUT		6
L60A L61 L156 L156A L157					
L270	376-9015-	SKT 28	IC SOCKET 28 PIN DIL MOUNT		1
L97 - L107 L110 - L131 L134 - L155 L158 - L179 L182 - L192	377-0415-	4164	IC 64KX1 DRAM 200NS REF REQUIRE 4MS/256 ROW		88
@3	452-2707-	STIFFN	STIFFENER LOWER		1
@2	452-2708-	STIFFN	STIFFENER UPPER		1
@26 - @27	465-1238-	EXTRCTOR	EXTRACTOR		2
@1	510-9300-		PCB		1
@4 @10	650-2083-	SCREW	SCREW		7
@18 - @24	652-2004-	NUT	NUT		7
@11 - @17	653-2009-	WASHER	WASHER		7
J1 - J4	654-0104-	3 CONT	CONN PC HEADER SINGLE ROW .100		4
@25	660-0341-	L.T.	LOCK TITE (QTY FOR THIS A/R)		1

WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
(CAUTION - THE FOLLOWING PARTS/COMPONENTS CONTAINED IN THIS B.O.M. ARE NOT REC ADED FOR NEW DESIGNS)				
376-0197-	74S04	IC HEX INVERTER		1
376-0208-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES		8
376-0282-	74S74	IC DUAL D TYPE POS EDGE TRIGRD F/F W/PRESET/C		8
376-0205-	74S32	IC QUAD 2 INPUT OR GATE		1
376-0228-	74S00	IC QUAD 2 INPUT NAND GATE		2
376-0298-	74S138	IC 3 LINE TO 8 LINE DECODER MULTIPLEXER		1
376-0301-	74S158	IC QUAD 2 TO 1-LINE DATA SELECTOR/MUX INVERT		
376-0305-	74S374	IC OCTAL D-TYPE EDGE TRIG F/F TRI STATE		.
376-0333-	74S139	IC 2 TO 4 LINE DECODER/MULTIPLEXER		1
376-0336-	74S151	IC 1 OF 8 DATA SEL/MUX		1
376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI STATE		1

*** END-OF-REPORT ***

		BY	DATE	APPROVED BY	DATE
WANG	WANG LABORATORIES, INC. LOWELL, MA U.S.A.	DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO.			MFG ENGR	
	SEE SHEET SPECIFICATIONS NO.	TITLE 4 MEG BYTE MEMORY			
FINISH	TOL. EX. AS NOTED .XX ± .010 .XXX ± .005 ANG ± 1°30'	210-9300	C	9300	1
	SCALE SHT 9 OF 12	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

(FINAL PARTS LIST)

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L
ASSEMBLY LEVEL & TITLE: 209-2 PCA VS SM SYS 1M MEM ML
PARTS LIST REVISION (P): 1
ARTWORK REVISION (R): 00
ASSEMBLY REVISION (A): 01
SCHEMATIC REVISION (S): 01
DWR OR MOST RECENT ECO: 339900
CREATED: 07/13/84 14:58
LAST MODIFIED: 12/17/84 14:02 BY: RS
EDITING REVISION: 12

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
C2 C12 C15 - C26 C28 - C38 C41 - C51 C54 - C64 C67 - C77 C80 - C90 C93 - C103 C106 - C116 C119 - C129 C132 - C142 C145 - C155 C158 - C168 C171 - C181 C184 - C194 C198 - C208	300-1833-	.1U	CAP CERAMIC MONO AXIAL LEADED +80%-20% 50V Z5U		176
C13 - C14 C39 - C40 C65 - C66 C91 - C92 C117 - C118 C143 - C144 C169 - C170 C195 - C197 C210 - C236 C238 - C245 C247 - C248	300-1966-	.047U	CAP CERAMIC MONO AXIAL +80 -20% 50V Z5U		54
C1 C26 - C27 C52 - C53 C78 - C79 C104 - C105 C130 - C131 C156 - C157 C182 - C183 C209	300-4018-	18U	CAP TANT AXIAL 10% 15V		16
C237	300-4022-	15U	CAP TANT AXIAL 10% 20V		2

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
C246					
SW1	325-1501-	SWITCH	SLIDE SPST 5 POS		1
R19 - R25 R27 - R33 R52 - R58 R60 - R66 R85 - R91 R93 - R99 R118 - R124 R126 - R132	330-1048-	47.000	RES FIXED METAL FILM 1/4W 5% 200PPM		56
R1 - R16 R67 - R82 R133 - R143 R146 - R156	330-1057-	56.000	RES FIXED METAL FILM 1/4W 5% 200PPM		54
R17 R50 R83 R116 R144 - R145 R157 - R164 R165A	330-3011-	1K	RES FIXED METAL FILM 1/4W 5% 200PPM		15
R165	333-0809-	10.000KH	RESISTOR NETWORK TYPE: 10/09/C/SS		1
P4 - P7	350-4506-	2 CONT	CONN SHUNT .100 CTR		4
L231	376-0160-	74LS175	IC QUAD D-TYPE FLIP-FLOP		1
L227	376-0171-	74148	IC 8-LINE-TO-3-LINE OCTAL PRIORITY ENCODER		1
L229	376-0197-	74S04	IC HEX INVERTER		1
L36 - L37 L84 - L85 L132 - L133 L180 - L181	376-0200-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES		8
L212 - L215 L237 L254	376-0202-	74S74	IC DUAL D-TYPE POS EDGE TRIGRD F/F W/PRESET/C		8
L257 - L258 L201 L222 - L226 L243	376-0204-	74LS257	IC QUAD 2-LINE TO 1-LINE DATA SEL/MUX		7
L256	376-0205-	74S32	IC QUAD 2-INPUT OR GATE		1
L234 - L235	376-0228	74S00	IC QUAD 2-INPUT NAND GATE		2
L252	376-0259-	74S85	IC 4-BIT MAGNITUDE COMPARATOR		2
L207	376-0278-	74S161	IC SYN 4-BIT BINARY COUNTER W/DIRECT CLEAR		1
L221	376-0286-	74LS374	IC OCTAL D-TYPE FLIP-FLOP TRI-STATE		1
L242 L248 - L249 L196 - L198 L200 L208 L210 - L211 L244 - L247 L281	376-0288-	74LS244	IC OCTAL BUFFER/LINE DRIVER W/TRI STATE		4 12

WANG WANG LABORATORIES, INC. LOWELL, MA 01851

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL
MODEL NO.
SEE ENGR SPECIFICATION NO.
FINISH
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACT ± 1/64 XXX ± .005 ANG ± 1° SURFACE FINISH
SCALE NONE

TITLE 4 MEG BYTE MEMORY

DWNG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-9300	C	9300	1

* REF. DES.	* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *
L228	376-0294-	74LS138	IC 3-LINE TO 8-LINE DECODER MULTIPLEXER		1
L12 - L13	376-0297-	74LS240	IC OCTAL BUFFER/LINE DRIVER/RECEIVER		6
L108 - L109					
L253					
L205	376-0298-	74S138	IC 3-LINE TO 8-LINE DECODER MULTIPLEXER		1
L202	376-0301-	74S158	IC QUAD 2 TO 1-LINE DATA SELECTOR MUX INVERT		1
L233	376-0305-	74S374	IC OCTAL D-TYPE EDGE TRIG FLIP FLOP TRI STATE		1
L199	376-0307-	74LS393	IC DUAL 4 BIT RIPPLE COUNTER		2
L230					
L255	376-0333-	74S139	IC 2 TO 4-LINE DECODER MULTIPLEXER		1
L236	376-0336-	74S151	IC 1-OF 8 DATA SELECTOR		1
L204	376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI-STATE		1
L60	376-0551-	AM2966	IC OCTAL D W/ DRIVER TRI STATE		6
L60A					
L61					
L156					
L156A					
L157					
L220	376-9015-	SKT 28	IC SOCKET 28 PIN DIL MOUNT		1
L1 - L11	377-0415-	4164	IC 64Kx1 DRAM 200NS REF REQUIRE 4MS/256 ROW		176
L14 - L35					
L38 - L59					
L62 - L83					
L86 - L107					
L110 - L131					
L134 - L155					
L158 - L179					
L182 - L192					
Ø3	452-2707-	STIFFN	STIFFENER LOWER		1
Ø2	452-2708-	STIFFN	STIFFENER UPPER		1
Ø26 - Ø27	445-1238-	EXTRCTOR	EXTRACTOR		2
Ø1	510-9300-		PCB		1
Ø4 - Ø10	650-2083-	SCREW	SCREW		7
Ø18 - Ø24	652-2204-	NUT	NUT		7
Ø11 - Ø17	653-2209-	WASHER	WASHER		7
J1 - J4	654-0104-	3 CONT	CONN PC HEADER SINGLE ROW .100		4
Ø25	660-0341-	L.T.	LOKA TITE (QTY FOR THIS A/R)		1

*	*WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *

(CAUTION - THE FOLLOWING PARTS/COMPONENTS CONTAINED IN THIS B O M ARE NOT RECOMMENDED FOR NEW DESIGNS)

	376-0147	74S04	IC HEX INVERTER
	376-0200-	74S08	IC QUAD 2 INPUT POSITIVE AND GATES
	376-0202-	74S74	IC DUAL D TYPE POS EDGE TRIGGERED F F W/PRESET &
	376-0215-	74S32	IC QUAD 2 INPUT OR GATE
	376-0228-	74S00	IC QUAD 2 INPUT NAND GATE
	376-0298-	74S138	IC 3 LINE TO 8 LINE DECODER MULTIPLEXER
	376-0301-	74S158	IC QUAD 2 TO 1 LINE DATA SELECTOR MUX INVERT
	376-0305-	74S374	IC OCTAL D TYPE EDGE TRIG FLIP FLOP TRI STATE
	376-0333-	74S139	IC 2 TO 4 LINE DECODER MULTIPLEXER
	376-0336-	74S151	IC 1 OF 8 DATA SELECTOR
	376-0338-	74S244	IC OCTAL BUFFER/LINE DRIVER/RECEIVER TRI STATE

*** END-OF REPORT ***

WANG LABORATORIES, INC.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO			MFG ENGR	
	SEE DRAWING SPECIFICATIONS NO.	TITLE: 4 MEG BYTE MEMORY			
FINISH	SIZE B SCALE NONE WEIGHT	210-9300	C	9300	1
	SCALE	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

(FINAL PARTS LIST)

BOARD NO. & TITLE: C9300 4 MEG BYTE MEMORY M/L
ASSEMBLY LEVEL & TITLE: 209-3 PCA VS SM SYS 2M MEM ML
PARTS LIST REVISION (P): 1
ARTWORK REVISION (R): 00
ASSEMBLY REVISION (A): 01
SCHEMATIC REVISION (S): 01
DWR OR MOST RECENT ECO: 33990D

CREATED: 07/12/84 14:55
LAST MODIFIED: 12/17/84 14:02 BY: MS
EDITING REVISION: 12

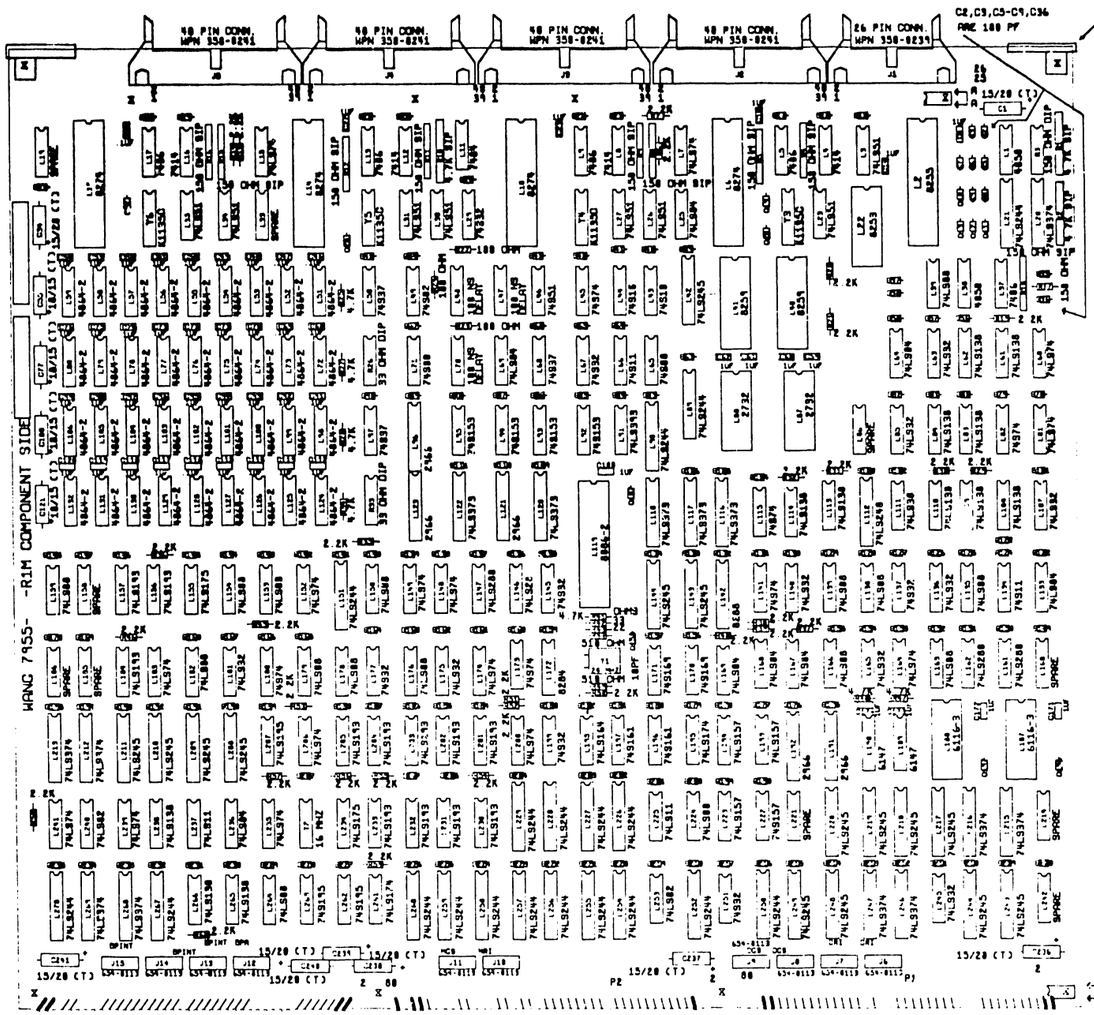
* REF. DES.	* WANG PART NO.	* VALUE/TYPE *	DESCRIPTION	* DRAWING NO. *	QTY. *
C106 - C116 C119 - C129 C132 - C142 C145 - C155 C158 - C168 C171 - C181 C184 - C194 C198 - C208	300-1833-	.1U	CAP CERAMIC MONO AXIAL LEADED +80%-20% 50V Z5U		88
C13 - C14 C39 - C40 C65 - C66 C91 - C92 C117 - C118 C143 - C144 C169 - C170 C195 - C197 C210 - C236 C238 - C245 C247 - C248	300-1966-	.047U	CAP CERAMIC MONO AXIAL +80 -20% 50V Z5U		54
C1 C26 - C27 C52 - C53 C78 - C79 C104 - C105 C130 - C131 C156 - C157 C182 - C183 C209	300-4018-	18U	CAP TANT AXIAL 10% 15V		16
C237 C246	300-4022-	15U	CAP TANT AXIAL 10% 20V		2
SW1	325-1501-	SWITCH	SLIDE SPST 5 POS		1
R19 - R25 R27 - R33 R52 - R58 R60 - R66 R85 - R91 R93 - R99	330-1048-	47.000	RES FIXED METAL FILM 1/4W 5% 200PPM		56

WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO.	TITLE: 4 MEG BYTE MEMORY			
	SEE ENGRG SPECIFICATIONS No.				
FINISH	TOL EX AS NOTED XX ± 010 FRAC ± 1/64 XXX ± 005 ANG ± 1° 30' FINISH 125	210-9300	C	9300	1
	SCALE SHT 12 OF 12	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

APPENDIX E

SCHE-
MATICS

DO NOT BORDE



BY	J FELTON	CHAT	D.T.	JAR	JAR	JAR	JAR	PRA	DF	DF
DATE	3/23/83	6/9/83	10/83	3/26/84	7/1/84	8/23/84	8/23/84	11/30/84	4/28/85	4/28/85
REVISION	ORIG 61686	ECO 287870	ECO 294850	ECO 307110	ECO 330820	ECO 337870	ECO 337880	ECO 339310	ECO 33452	ECO 33757
ID	R0/0	R1/1	R1/2	R1/3	R1/4	R1/5	R1/6	R1/7	R1/8	R1/9

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 5 PERCENT EXPRESSED IN OHMS.
3. L22,L67,L68 LOAD 24 PIN SOCKET 376-4803 (QTY 3)
4. L6,L7,L10,L11,L16,L17,L20 LOAD 16 PIN SOCKET 376-4811 (QTY 6)
5. L49,L71 LOAD 28 PIN SOCKET 376-4813 (QTY 2)
6. TZ-6 LOAD TEKNA 376-4808 (QTY 5)
7. Y1 TEFLON TUBING (685-0128).
8. Y1 BUSS WIRE (680-4007).

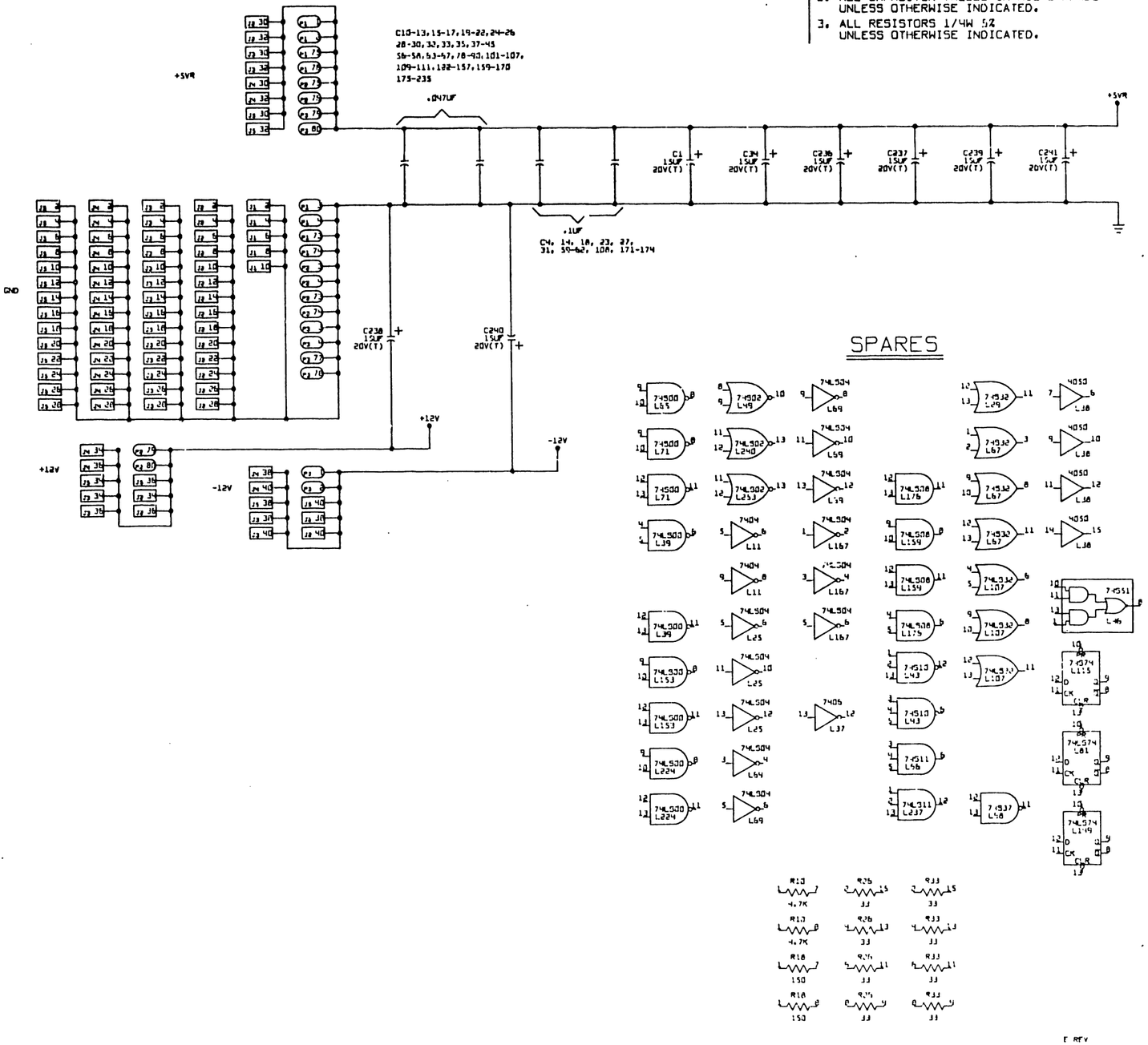
WANG	BY J FELTON	DATE 7/83	APPROVED BY
	MODEL NO v9-25		
	PART NO 218-7955-R1		
	TITLE ASSEMBLY DRAWING ASYNC DEV CONT M/L		
	218-7955-R1	D 7955	9

MNEMONICS	COORD.
ADR	9E9
BPA1-BPA3	5G14
BPA4-BPA7	5F14
BPA8-BPA10	5C14
BPD0-BPD7	5G9
BPD8-BPD15	5H4
BPINT1-BPINT7	5D3
BUSY	5A6
CT51,CT52	8D8
CT53	8J8
CT54	8J8
CT55,CT56	8D14
CT57	8J14
CT58	8J14
DATA1-DATA8	9H3
DAV	9B6
DA0-DA15	7H7
DCB0-DCB1	/B1
DCD1-DCD4	9F14
DCD5-DCD8	9D1
DD0	9J14
DD0-DD15	5C4
DD50-DD54	9K14
DR10-DR19	9K3
DTB	9J14
DTR1-DTR2	8C8
DTR3-DTR4	8J8
DTR5-DTR6	8J8
DTR7-DTR8	8J8
EXTXC1	8A7
EXTXC2	8C7
EXTXC3	8G7
EXTXC4	8G7
EXTXC5	8B14
EXTXC6	8C14
EXTXC7	8G14
EXTXC8	8H14
EXRXC1	8A7
EXRXC2	8B7
EXRXC3	8H7
EXRXC4	8F7
EXRXC5	8A14
EXRXC6	8B14
EXRXC7	8F14
EXRXC8	8G14
FAULT	9F7
INIT	4F14
IOREN	9E14
IOWR	9K14
IOWR	9F14
% 1-MA20	7K1
MC00-MC02	7J1
MD1	9J14
MD0-MD15	5K9
MD50-MD36	9J14
MR10-MR16	9J3
MDRW-MSB1	9J14
MC	4G7
MSBOK ON	9F7
RESET	9B1
RT01	8E1
RT02	8B1
RT03	8J1
RT04	8H1
RT05	8F8
RT06	8B8
RT07	8J8
RT08	8H8

MNEMONICS	COORD.
RXOUT	8C8
RXOUT	8D8
RXOUT,RXOUT	8J8
RXOUT	8C14
RXOUT	8D14
RXOUT,RXOUT	8J14
SPART	9F7
SLCT	9F7
TXOUT	8D1
TXOUT	8K1
TXOUT,TXOUT	8J1
TXOUT	8C8
TXOUT	8D8
TXOUT,TXOUT	8J8
+5V-+5V	9B1

NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



SPARES

E REV 4 N

WANG		SCHEMATIC DIAGRAM			
ASSY NUMBER: VS-25	MANG PART NUMBER: 210 7455	TITLE: VS-25 ASYNC DEVICE CNTRL			
		DWN	PRD	CHK	ENG	DC	DIR
		E	7955				12
SCALE: C	SHEET 1 OF 4	SIZE	DRAWING NUMBER				REV

MICROPROESSOR

CLOCK GENERATOR

8086 DATA BUFFER

8086 ADDRESS LATCH

ADDRESS DECODING

WANG

DYNAMIC RAM ADDRESS MUX

REFRESH ROW COUNTER

DRAM ADDRESS DRIVER

EPROM (4KW)

EPROM ADDRESS BUFFER

DRAM DATA LATCH

DRAM DATA BUF

DYNAMIC RAM TIMING

100 NS DELAY L70

100 NS DELAY L47

133 NS DELAY L48

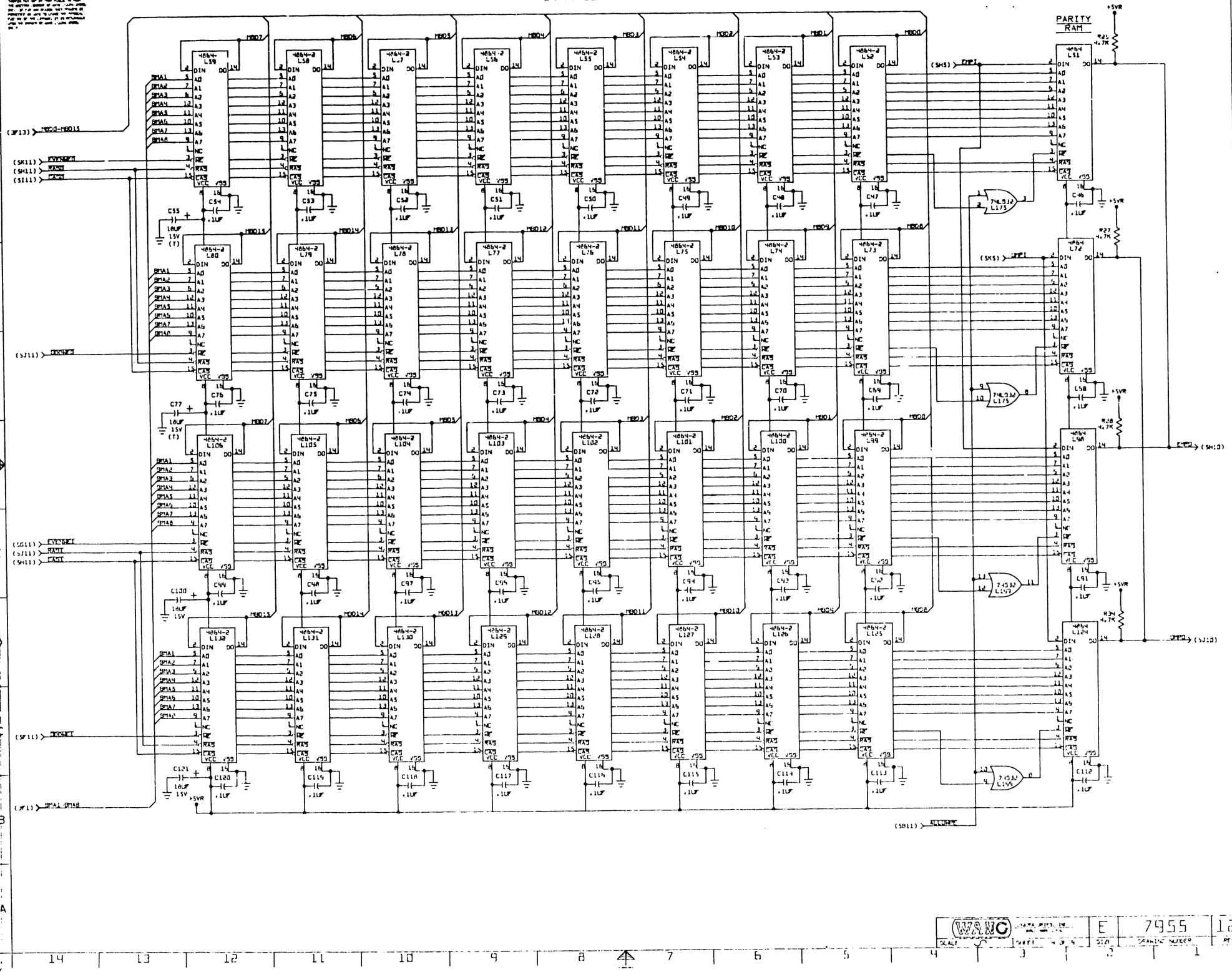
WANG

E

7955

9

DYNAMIC RAM


PARITY RAM
4864-2
74LS32
+5VR
(SH5)
(SH10)
(SJ10)
(SK11)
(SH11)
(SI11)
(SJ11)
(SG11)
(SF11)
(SB11)
(3F13)
(3F1)
C55
C77
C130
C121
10UF 15V (T)
.1UF

DRAM CONTROL DRIVERS

DRAM PARITY GENERATOR

SRAM -V5 BUS DATA BUFFER

SRAM-BUS DATA BUFFER

PROGRAMMABLE TIMER

PROGRAMMABLE INTERRUPT CONTROLLER

SRAM ADDRESS MUX

SRAM ADDRESS DRIVER

WANG		E	7955	12
SCALE	SHEET	SIZE	DRAWING NUMBER	REV

STATIC RAM (2KW)

PARITY RAM

SRAM PARITY GENERATOR

DMA WORD COUNTER

BAUD RATE GENERATORS

SRAM - VS BUS DATA LATCH

MAIN MEMORY DATA BUF

MAIN MEMORY DATA BUS

DMA CONTROL

DATA RAM DATA BUF

BP DATARAM DATA BUS

BUS PROCESSOR INTERRUPT SELECT

WANG		E	7955	12
SCALE	SHEET	SIZE	DRAWING NUMBER	REV

DATA RAM ADDRESS BUFFER

DATA RAM ADDRESS BUS

DMA MM OR DATARAM ADDRESS REG.

MM ADDRESS BUFFER

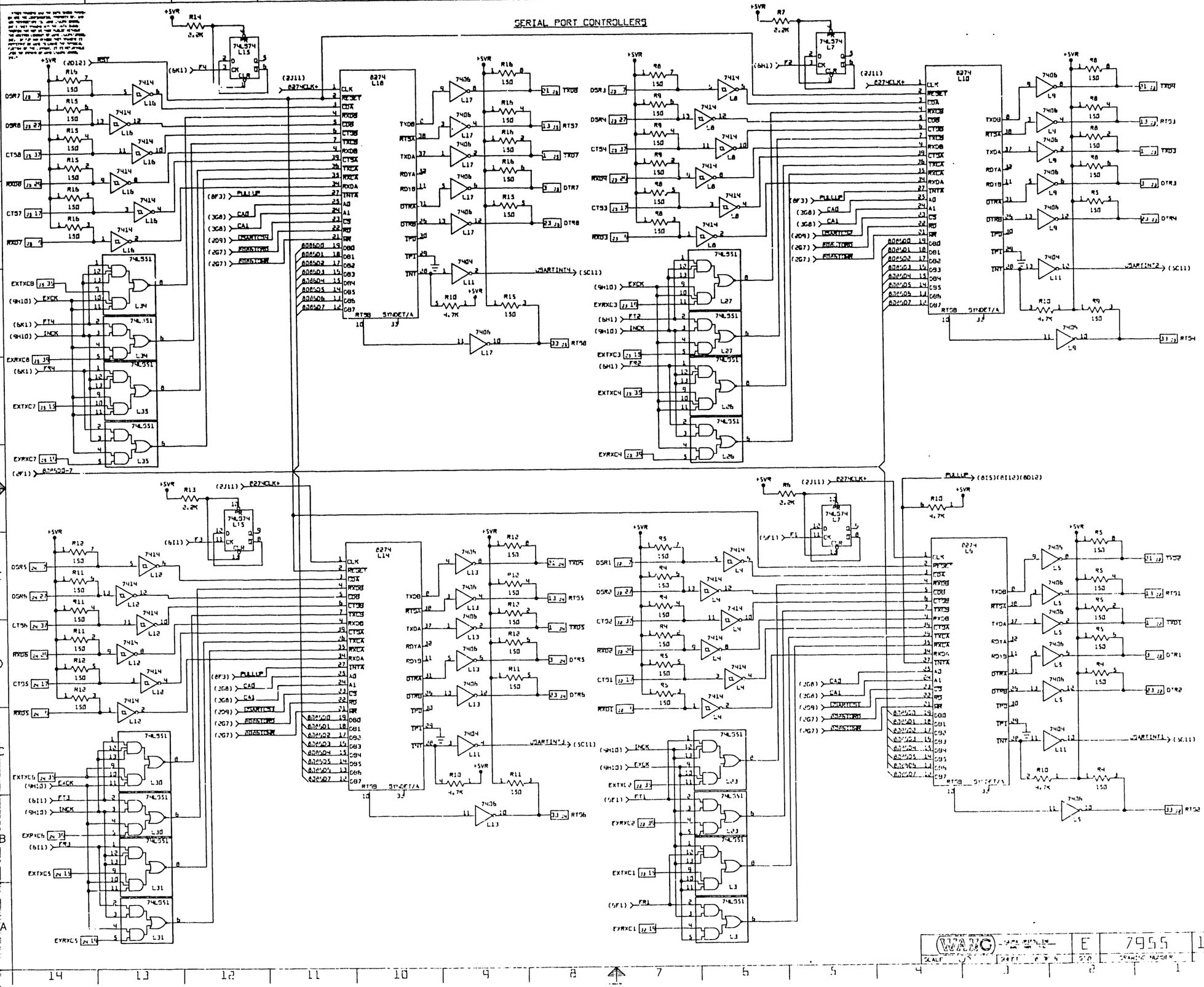
MAIN MEMORY ADDRESS BUS

DMA CONTROLLER LOAD MUX

DMA SRAM ADDRESS REG.

WANG		E	7955
SCALE	SHEET	SIZE	DRAWING NUMBER

SERIAL PORT CONTROLLERS



WANG	E	7955	12
SCALE	SHEET	DRAWING NUMBER	REV

BUS GRANT SELECT

BUS REQUEST SELECT

ADC TO BP SOFTWARE STATUS

BP TO ADC SOFTWARE STATUS

PRINTER PORT DATA

BP TO DMA ADDRESS DECODE

V3 BUS PROCESSOR DATA BUS

V3 BUS PROCESSOR ADDRESS BUS

ADC TO BP HARDWARE STATUS

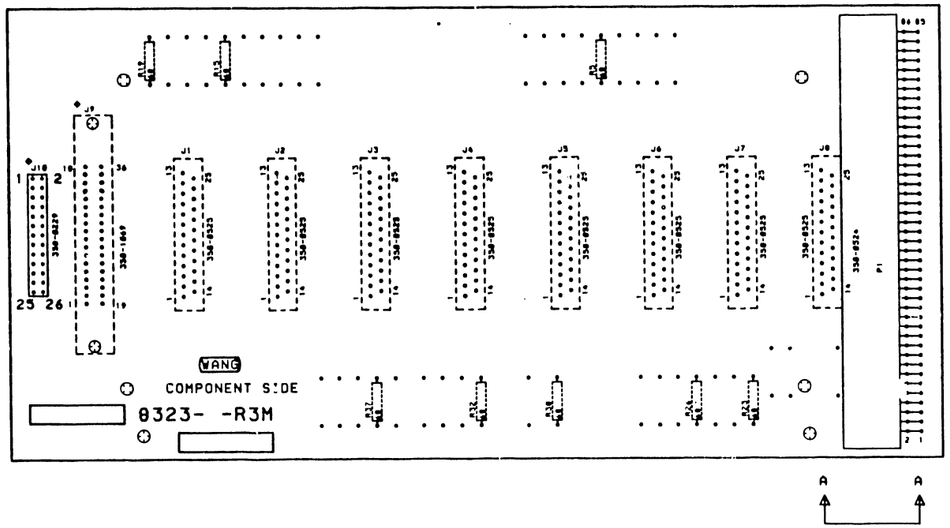
PRINTER PORT CONTROL

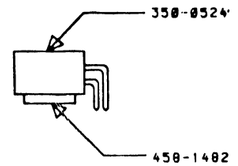
BOARD ADDRESS SELECT

WANG

E | 7955 | 12

SCALE | SHEET | SIZE | DRAWING NUMBER | REV





DETAIL A-A

NOTES: 1.UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W 5% EXPRESSED IN OHMS.
2.ALL COMPONENTS OTHER THAN P1 AND J1-8 ARE MOUNTED ON CIRCUIT SIDE OF BOARD.
* DO NOT LOAD J9 OR J10 FOR 210-8323-1

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN G.TYNES	6/8/82	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS15/25/100	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE ASYNC DEVICE CONTROLLER CONNECTOR BD. ASSEMBLY DRAWING			
FINISH	ALL EX. AS NOTED	210-8323-R3	C	8323	7
	SCALE 1/1 SHT 1 OF 1	BOARD PART NUMBER	SIZE	DRAWING NUMBER	REV

DO NOT SCALE

BA0	22	R28 68Ω	2	BA0	BA5	42	R30 68Ω	25	BA5	BA2	62	R15 68Ω	21	BA2	BA1	82	R19 68Ω	21	BA1	RESET	26	39	RESET
BA3	3	R37 68Ω	23	BA3	CB0	23		5	CB0	DD6	43		17	DD6	CF6	63		8	CF6	DDB	88	77	DDB	±0V	2,10	19	±0V
CF3	4		8	CF3	-12V	24	-12V			CD5	44		20	CD5	CC6	64		6	CC6	DBB	89	75	DBB	±0V	9,10	20	±0V
CA3	5		4	CA3	CD7	25		20	CD7	DB2	45		15	DB2	CE6	65		22	CE6	DATA1	1,10	2	DATA1	±0V	6,10	21	±0V
CE3	6		22	CE3	BBB	26		3	BBB	CA5	46		15	CA5	CB6	66		5	CB6	DATA2	3,10	3	DATA2	±0V	8,10	22	±0V
DB4	7		15	DB4	CF7	27		8	CF7	CD6	47		20	CD6	CD1	67		20	CD1	DATA3	5,10	4	DATA3	±0V	10,10	23	±0V
CC3	8		6	CC3	DB7	28		15	DB7	CA6	48		4	CA6	CF2	68		8	CF2	DATA4	7,10	5	DATA4		±0V	24	±0V
DD4	9		17	DD4	CE7	29		22	CE7	CF5	49		85	CF5	CF1	69		81	CF1	DATA5	9,10	6	DATA5		±0V	25	±0V
CB3	10		5	CB3	-12V	30	-12V			BA6	50	R5 68Ω	26	BA6	CB2	70		52	CB2	DATA6	11,10	7	DATA6		±0V	26	±0V
BB4	11		36	BB4	CC7	31		6	CC7	CE5	51		225	CE5	CE1	71		221	CE1	DATA7	13,10	8	DATA7		±0V	27	±0V
																								±0V	85	86	±0V
BA4	12	R32 68Ω	24	BA4	BA7	32	R26 68Ω	21	BA7	DD2	52		17	DD2	CC2	72		62	CC2	DATA8	15,10	9	DATA8	±0V	1	21	IOV
DB3	13		15	DB3	CB7	33		5	CB7	CC5	53		65	CC5	CC1	73		61	CC1	DSTBIN	17,10	19	DSTBIN	USR8	19,10	18	USR8
CF4	14		84	CF4	CD4	34		20	CD4	BB3	54		33	BB3	CE2	74		22	CE2	ACK	19,10	10	ACK	POWER ON	22,10	17	POWER ON
CD3	15		20	CD3	CA7	35		47	CA7	CB5	55		55	CB5	CB1	75		51	CB1	BUSY	21,10	11	BUSY	SMART	12,10	16	SMART
CE4	16		224	CE4	CA4	36		44	CA4	DD3	56		17	DD3	CD2	76		202	CD2	PE	23,10	12	PE	DSTBOUT	19,10	14	DSTBOUT
CF8	17		88	CF8	DD7	37		17	DD7	DB5	57		155	DB5	DB1	77		151	DB1	SLCT	24,10	13	SLCT	USR1	16,10	15	USR1
CC4	18		64	CC4	CD8	38		20	CD8	BB5	58		35	BB5	BB1	78		31	BB1	FAULT	25,10	33	FAULT	DAV	22,10	34	DAV
CE8	19		228	CE8	BB7	39		37	BB7	BB6	59		36	BB6	BB2	79		32	BB2								
CB4	20		54	CB4	CA8	40		48	CA8	DD5	60		175	DD5	DD1	80		171	DD1								
CC8	21		68	CC8	DB6	41		15	DB6	CA2	61		42	CA2	CA1	81		41	CA1								

REVISION	BY	DATE	APPROVED
SEE SHEET 2			

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

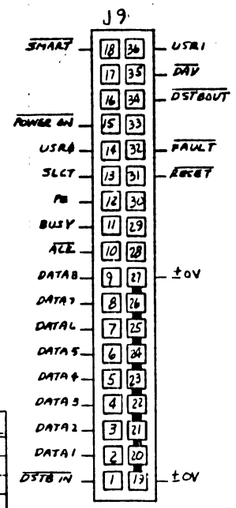
	BY	DATE	APPROVED BY	DATE
DWN	P.G. Daniel	7-12-82	E ENGR	
CHK			M ENGR	
			MFG ENGR	

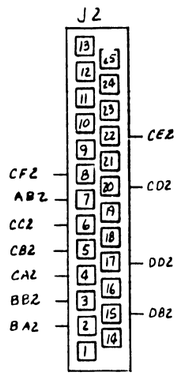
MATERIAL — MODEL NO. VS-15, LS/100 — TITLE: ASYNC DEVICE CONTROLLER CONNECTOR BOARD

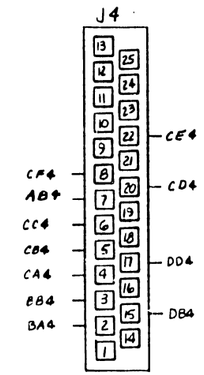
FINISH — 210-8323 | D | 8323 | 6

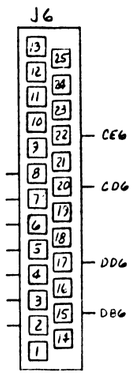
8323

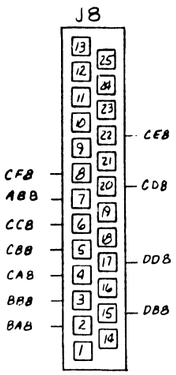
DO NOT SCALE

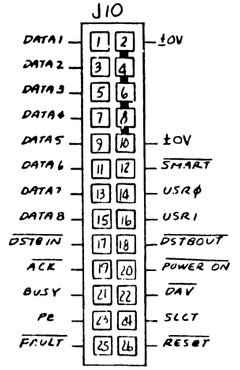


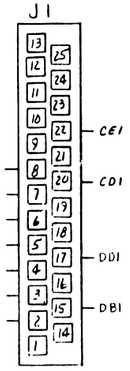


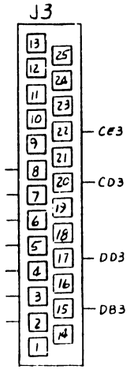


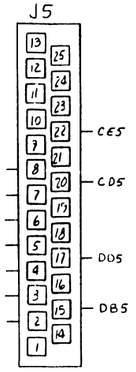


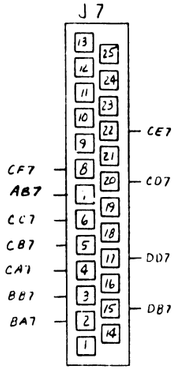


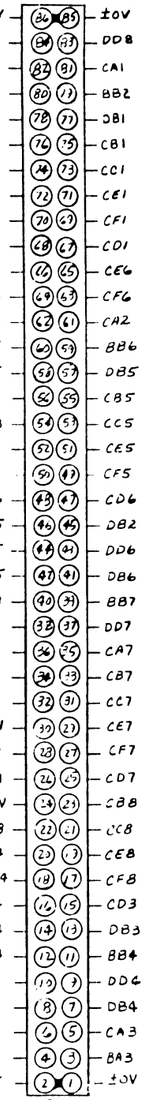












MNEMONIC	COORD.
BA1	1G4
BA2	1G6
BA3	1G11
BA4	1D11
BA5	1G8
BA6	1E8
BA7	1D9
BA8	1G9
ACK	1C4
BB1	1B6
BB2	1B6
BB3	1C8
BB4	1D11
BB5	1B8
BB6	1B8
BB7	1B9
BB8	1F9
BUSY	1C4
CA1	1A6
CA2	1A8
CA3	1F11
CA4	1C9
CA5	1F8
CA6	1E8
CA7	1C9
CA8	1A9
CB1	1C6
CB2	1E6
CB3	1E11
CB4	1A11
CB5	1C8
CB6	1F6
CB7	1D9
CB8	G9

MNEMONIC	COORD.
CC1	1D6
CC2	1D6
CC3	1E11
CC4	1B11
CC5	1D8
CC6	1G6
CC7	1D9
CC8	1A11
CD1	1F6
CD2	1C6
CD3	1G11
CD4	1C9
CD5	1G8
CD6	1F8
CD7	1F9
CD8	1B9
CE1	1D6
CE2	1C6
CE3	1F11
CE4	1C11
CE5	1D8
CE6	1F6
CE7	1E9
CE8	1B11
CF1	1E6
CF2	1F6
CF3	1G11
CF4	1C11
CF5	1E8
CF6	1G6
CF7	1F9
CF8	1B11

MNEMONIC	COORD.
DB1	1B6
DB2	1F8
DB3	1D11
DB4	1F11
DB5	1B8
DB6	1A9
DB7	1E9
D38	1G4
DD1	1A6
DD2	1D8
DD3	1C8
DD4	1E11
DD5	1A8
DD6	1G8
DD7	1B9
DD8	1G4
DATA1-DATA8	1F4
DAV	1B3
DSTBIN	1D4
DSTBOUT	1C3
FAULT	1B4
PE	1C4
POWER ON	1C3
RESET	1G3
SLCT	1B4
SMART	1C3
USR0	1D3
USR1	1B3

EIA DESIGNATION	DESCRIPTION
AB	SIGNAL GND
BA	TRANSMIT DATA
BB	RECEIVE DATA
CA	REQUEST TO SEND (RTS)
CB	CLEAR TO SEND (CTS)
CC	DATA SET READY (DSR)
CD	DATA TERMINAL READY (DTR)
CE	RING INDICATOR (RI)
CF	DATA CARRIER DETECT (DCD)
DB	EXTERNAL TRANSMIT CLOCK
DD	EXTERNAL RECEIVE CLOCK

NOTE: ALL RES ARE VAW 5% UNLESS OTHERWISE SPECIFIED.

P1 E REV

REVISION	BY	DATE	APPROVED BY	DATE

WANG PART NO	DRAWING NO	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR J CHEN	
CHK			M ENGR	
			MFG ENGR	

MATERIAL — MODEL NO VS-15, VS-120 — SEE ENGRG SPECIFICATIONS No.

FINISH — UNLESS OTHERWISE NOTED .XX ± .010 .XXX ± .005 ANG. ± 1/2° FRACT. ± 1/64

TITLE ASYNC DEVICE CONTROLLER CONNECTOR BOARD

WANG PART NUMBER 210-8323 | SIZE D | DRAWING NUMBER 8323 | REV 6

DO NOT SCALE

ASVR

R7 2.2K

BA1 (28)

BA2 (40)

±5V -12V +12V

L6 75150 — L5 75150 — L12 75150 — L40 75150 — L33 75150 — L39 75150

L10 — L32

TxD1 (11) — RTS1 (13) — DTR1 (31) — TxD2 (21) — RTS2 (33) — DTR2 (25) — TxD3 (12) — RTS3 (13) — DTR3 (32) — TxD4 (24) — RTS4 (35) — DTR4 (23)

Q2 MPS6518 — Q1 MPS6512 — R2 120Ω 1/2W — R1 120Ω 1/2W — -12V — +12V

Q3 MPS6512 — Q4 MPS6518 — R3 120Ω 1/2W — R4 120Ω 1/2W

Q15 MPS6512 — Q16 MPS6518 — R17 120Ω 1/2W — R18 120Ω 1/2W — T3

Q13 MPS6512 — Q19 MPS6518 — R15 120Ω 1/2W — R16 120Ω 1/2W — T4

HSVR — R1C 2.2K

CD4 (34) CA4 (36) — BA4 (12) CD3 (15) CA3 (57) BA3 (31) CD2 (16) CA2 (41) CD1 (27) CA1 (81)

DTR8 (24) RTS8 (33) TxD8 (14) DTR7 (34) RTS7 (34) TxD7 (4) DTR6 (23) RTS6 (33) TxD6 (15) DTR5 (33) RTS5 (35) TxD5 (13)

L16 — L17 75150 — L18 75150 — L11 75150 — L28 — L24 75150 — L34 75150 — L23 75150

+12V — R8 120Ω 1/2W — Q7 MPS6512 — T5 — Q8 MPS6518 — R9 120Ω 1/2W — -12V

Q5 MPS6512 — T6 — Q6 MPS6518 — R5 120Ω 1/2W — R6 120Ω 1/2W — +12V — -12V

Q9 MPS6512 — Q10 MPS6510 — R11 120Ω 1/2W — R12 120Ω 1/2W — T7 — +12V — -12V

Q11 MPS6512 — Q12 MPS6518 — R13 120Ω 1/2W — R19 120Ω 1/2W — T8 — +12V — -12V

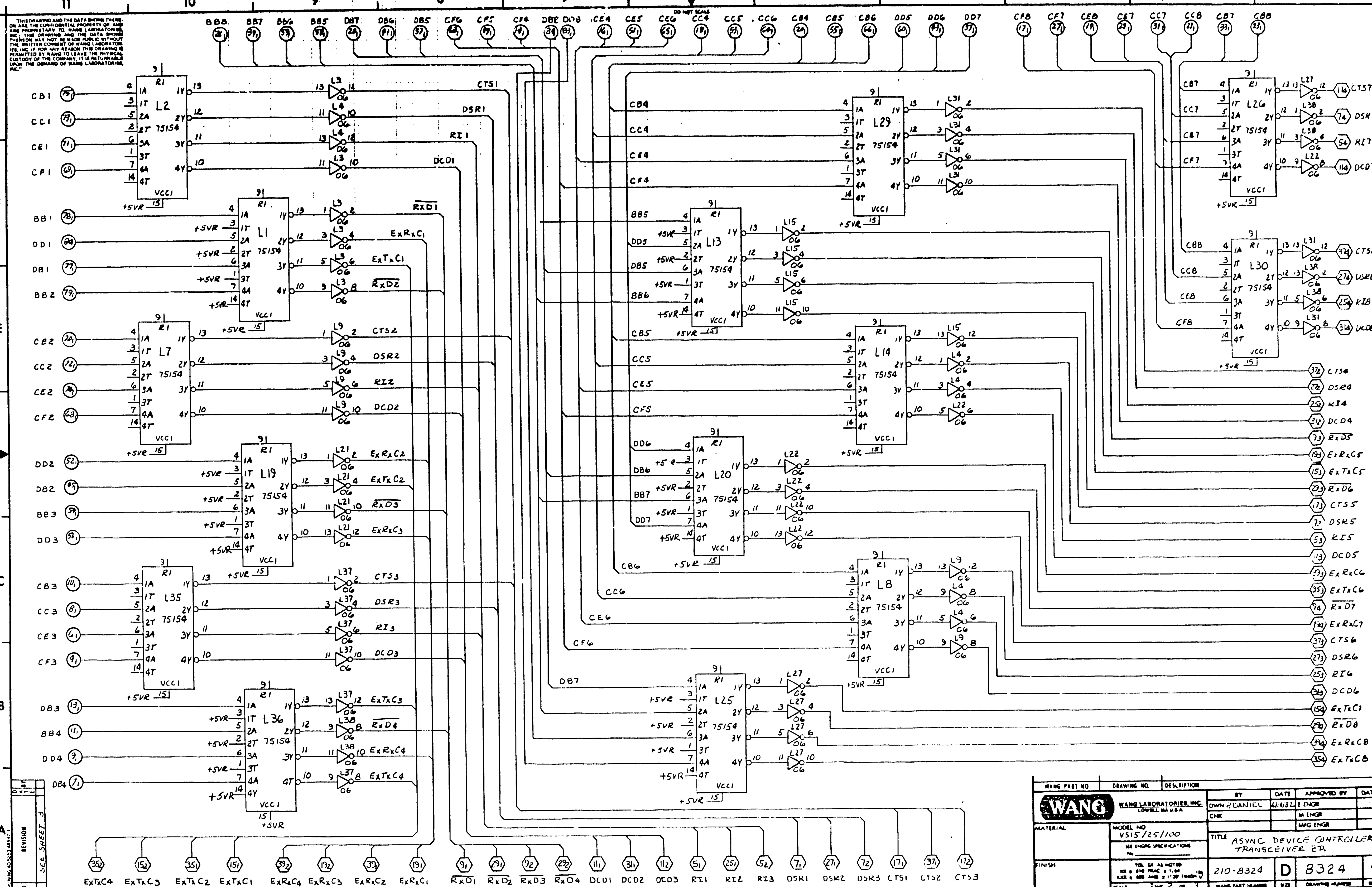
BA5 (42) CA5 (44) CD5 (46) BA6 (50) CA6 (48) CD6 (47) BA7 (32) CA7 (35) CD7 (25) BA8 (22) CA8 (40) CD8 (38)

WANG PART NO.	DRAWING NO.	DESCRIPTION
WANG LABORATORIES, INC. LOWELL, MA U.S.A.		
MATERIAL	MODEL NO VS15/25/100	TITLE ASYNC DEVICE CONTROLLER TRANSCEIVER BD.
FINISH	210-8324	D 8324 4

BY	DATE	APPROVED BY	DATE
DWN P.G. DAN-CL	6y.4/12	E ENGR	
CHK		M ENGR	
		MFG ENGR	

NO	REVISION	BY	DATE
	SEE SHEET 3		

D 8324


"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."
DO NOT SCALE
L2 75154
L1 75154
L7 75154
L19 75154
L35 75154
L36 75154
L29 75154
L13 75154
L14 75154
L20 75154
L8 75154
L25 75154
L26 75154
L30 75154
CTS1 DSR1 RI1 DCD1
RXD1 ExRxC1 ExTxC1 RxD2
CTS2 DSR2 RI2 DCD2
ExRxC2 ExTxC2 RxD3 ExRxC3
CTS3 DSR3 RI3 DCD3
ExTxC3 RxD4 ExRxC4 ExTxC4
CTS4 DSR4 RI4 DCD4
RxD5 ExRxC5 ExTxC5 RxD6
CTS5 DSR5 RI5 DCD5
ExRxC6 ExTxC6 RxD7 ExRxC7
CTS6 DSR6 RI6 DCD6
ExTxC7 RxD8 ExRxC8 ExTxC8
CTS7 DSR7 RI7 DCD7
CTS8 DSR8 RI8 DCD8
REVISION
SEE SHEET 3
WANG PART NO.
DRAWING NO.
DESCRIPTION
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
BY
DATE
APPROVED BY
DWN P. DANIEL 6/14/82
CHK
E ENGR
M ENGR
MFG ENGR
MATERIAL
MODEL NO VS15/25/100
SEE ENGRG SPECIFICATIONS No.
FINISH
TITLE ASYNC DEVICE CONTROLLER TRANSCEIVER BD.
210-8324
D
8324
4
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
SCALE
SHT 2 OF 3

DO NOT SCALE

I.C. LOCATION	TYPE	WL. PART NO.
L1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 29, 30, 35, 36	75154	376-0077
L3, 4, 9, 15, 21, 22, 27, 31, 37, 38	7406	376-0055
L5, 6, 11, 12, 17, 18, 23, 24, 33, 34, 39, 40	75150	376-0076
L10, 16, 28, 32	7416	376-0139

I.C. TYPE	LOCATION	SPARES
7406	L15	1
	L21	2
	L27	1

MNEMONICS	COORD.
BA1	1G8
BA2	1B6
BA3	1A7
BA4	1A7
BA5	1F1
BA6	1E1
BA7	1D1
BA8	1C1
BB1	2F11
BB2	2E11
BB3	2D11
BB4	2B11
BB5	2G9
BB6	2G5
BB7	2G10
BB8	2G10
CA1	1A6
CA2	1A6
CA3	1A7
CA4	1A8
CA5	1F1
CA6	1E1
CA7	1D1
CA8	1B1
CB1	2G11
CB2	2E11
CB3	2C11
CB4	2G5
CB5	2G5
CB6	2G5
CB7	2G2
CB8	2G1
CC1	2G11
CC2	2E11
CC3	2C11
CC4	2G6
CC5	2G6
CC6	2G5
CC7	2G2
CC8	2G2
CD1	1A6
CD2	1A6
CD3	1A7
CD4	A8
CD5	1E1
CD6	1D1
CD7	1C1
CD8	1B1

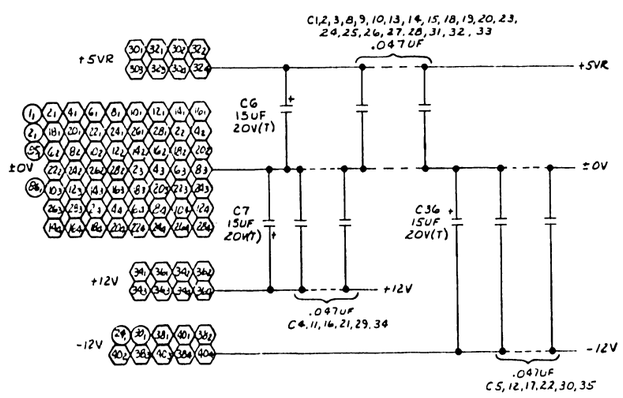
MNEMONICS	COORD.
CE1	2F11
CE2	2E11
CE3	2C11
CE4	2G7
CE5	2G6
CE6	2G6
CE7	2G3
CE8	2G3
CF1	2F11
CF2	2D11
CF3	2B11
CF4	2G7
CF5	2G8
CF6	2G8
CF7	2G3
CF8	2G3
CT51	2A4
CT52	2A4
CT53	2A4
CT54	2E1
CT55	2D1
CT56	2B1
CT57	2G1
CT58	2F1
DB1	2E11
DB2	2D11
DB3	2B11
DB4	2A11
DB5	2G8
DB6	2G8
DB7	2G9
DB8	2G7
DCD1	2A7
DCD2	2A7
DCD3	2A6
DCD4	2D1
DCD5	2C1
DCD6	2B1
DCD7	2F1
DCD8	2E1
DD1	2F11
DD2	2D11
DD3	2C11
DD4	2B11
DD5	2G4
DD6	2G4
DD7	2G4
DD8	2G8

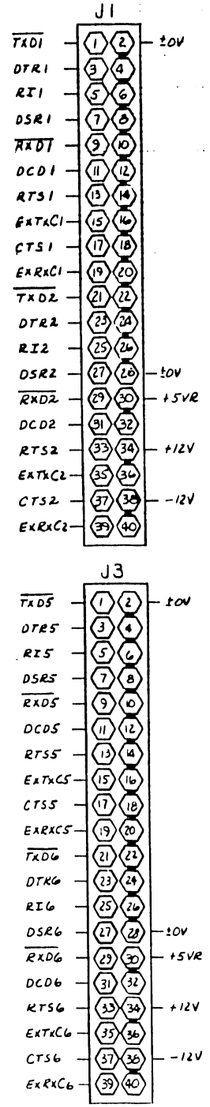
MNEMONICS	COORD.
DSR1	2A5
DSR2	2A5
DSR3	2A5
DSR4	2D1
DSR5	2C1
DSR6	2B1
DSR7	2G1
DSR8	2E1
DTR1	1E11
DTR2	1D11
DTR3	1C11
DTR4	1B11
DTR5	1G4
DTR6	1G4
DTR7	1G5
DTR8	1G5
ExRxC1	2A8
ExRxC2	2A9
ExRxC3	2A9
ExRxC4	2A9
ExRxC5	2D1
ExRxC6	2C1
ExRxC7	2C1
ExRxC8	2B1
ExTxC1	2A10
ExTxC2	2A10
ExTxC3	2A10
ExTxC4	2A11
ExTxC5	2D1

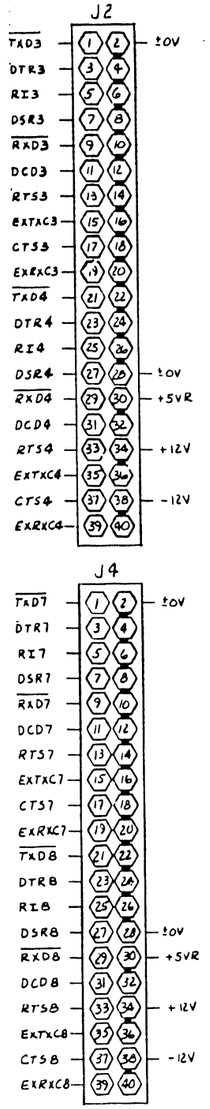
MNEMONICS	COORD.
ExTxC6	2C1
ExTxC7	2B1
ExTxC8	2B1
RI1	2A6
RI2	2A6
RI3	2A5
RI4	2D1
RI5	2C1
RI6	2B1
RI7	2F1
RI8	2E1
RTS1	1F11
RTS2	1E11
RTS3	1D11
RTS4	1B11
RTS5	1G4
RTS6	1G4
RTS7	1G4
RTS8	1G4
$\overline{RxD1}$	2A8
$\overline{RxD2}$	2A8
$\overline{RxD3}$	2A7
$\overline{RxD4}$	2A8
$\overline{RxD5}$	2D1
$\overline{RxD6}$	2D1
$\overline{RxD7}$	2C1
$\overline{RxD8}$	2B1

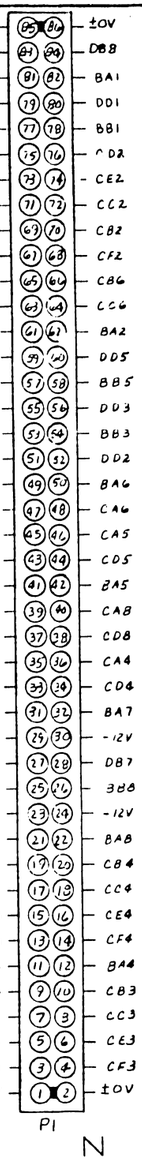
MNEMONICS	COORD.
$\overline{TxD1}$	1F11
$\overline{TxD2}$	1E11
$\overline{TxD3}$	1D11
$\overline{TxD4}$	1C11
$\overline{TxD5}$	1G4
$\overline{TxD6}$	1G4
$\overline{TxD7}$	1G4
$\overline{TxD8}$	1G5

NOTE: ALL RESISTORS ARE 1/4 W 5% UNLESS OTHERWISE SPECIFIED.









E-REV 1

WANG PART NO	DRAWING NO	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
	DENNIS DANIEL	6/10/74	ENGR'G. CHIEF	
	CHECKED	6/24/74	M. ENGR.	
			MFG ENGR	

MATERIAL

MODEL NO. VS1K/12S/100

SEE ENGRG SPECIFICATIONS No.

FINISH

UNLESS OTHERWISE NOTED: XXX ± .010 YYY ± 1/64 XXX ± .005 ANG ± 1° 30' FINISH

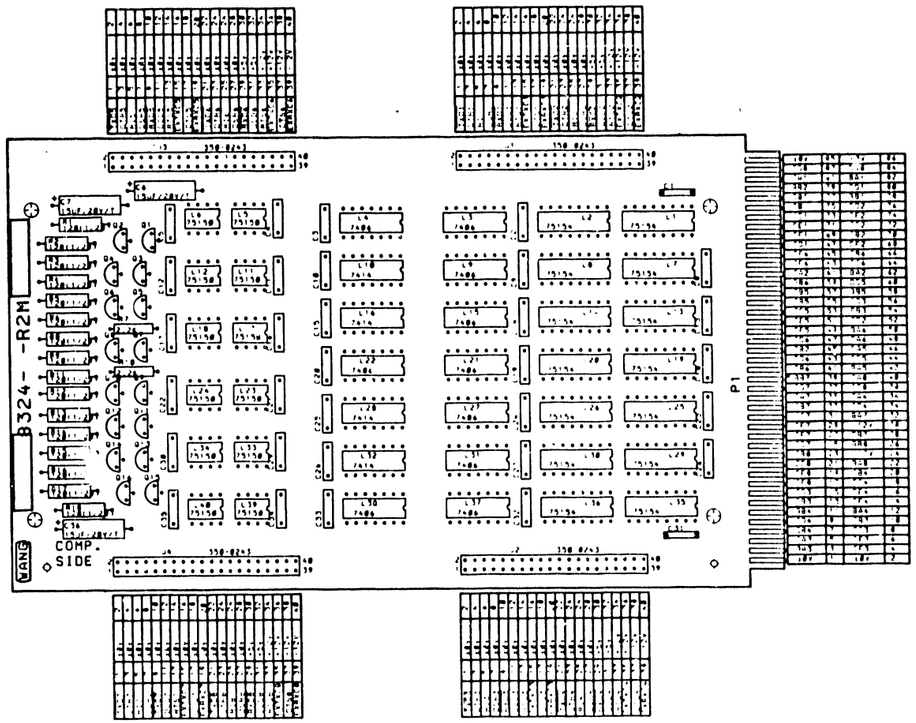
TITLE ASYNC DEVICE CONTROLLER TRANSCEIVER BD.

210-8324 | D | 8324 | 4

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

SCALE | SHT 1 OF 1

REVISION	BY	DATE	APPROVED



NOTES: 1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W.5%.EXPRESSED IN OHMS.
ALL CAPACITORS ARE .047UF.P/N 300-1966
Q1,3,5,7,9,11,13,15 ARE MPS6512.
Q2,4,6,8,10,12,14,16 ARE MPS6518.

WANG		BY	DATE	APPROVED BY	DATE
		DWN G.TYNES		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. PH001F VS15/25/100	E C CONTROL		MFG ENGR	
	SEE ENGR. SPECIFICATIONS NO. 10-203	TITLE ASYNC DEVICE CONTROLLER TRANSCEIVER BD. ASSEMBLY DRAWING			
FINISH		210-8324-R2	C	8324	3
	SCALE 1/1	DWG PART NUMBER	SIZE	DRAWING NUMBER	REV

N

WANG LABORATORIES, INC

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851 TEL (617) 459 5000 TWX 710 343 6769, TELEX 94 7421

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