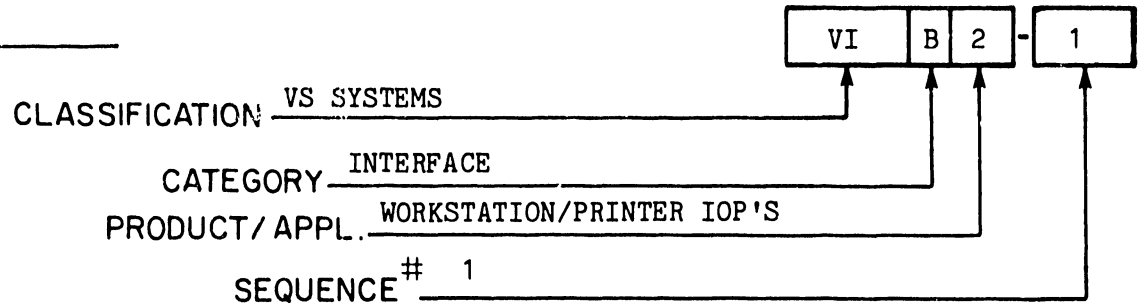
CUSTOMER ENGINEERING

PRODUCT SERVICE NOTICE

DATE: 4/9/81



TITLE:

MODEL 22V17 SERIAL WORKSTATION/PRINTER/ARCHIVING
WORKSTATION INPUT/OUTPUT PROCESSOR (IOP)

This PSN contains the following 22V17 IOP information.

1. GENERAL DESCRIPTION
2. SWITCH SETTINGS
3. PROM LOADINGS
4. INSTALLATION
5. DIAGNOSTICS
6. TROUBLESHOOTING
7. THEORY OF OPERATION

The following is a list of documentation categories referenced by this PSN. Documentation from these other categories is required for the performance of certain IOP installation/maintenance tasks.

VS-50/60/80 Mainframes -- VI.A.1
VS-100 Mainframe -- VI.A.2
VS Systems Diagnostics -- VI.C.3
General IOP Information -- VI.B.0

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1. GENERAL DESCRIPTION

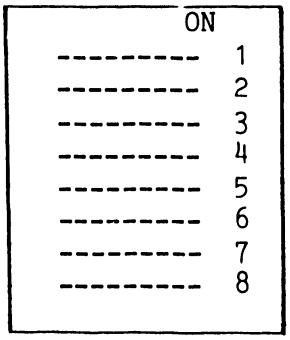
The 22V17 IOP (WL# 212-3016) supports the 2246C/S Serial Workstations, serial printers, and the 2266C/S Archiving Workstations (VS-AWS). The 22V17 is composed of a WL# 210-7810-A IOP Motherboard and a WL# 210-7216-B Device Adapter board. This 7810-based IOP supports up to 16 physical ports with 32 different addresses (devices). This allows multiple-device peripherals such as the Archiving Workstation (terminal and diskette drive attached to the IOP via the same I/O cable) to be used. The 22V17 is available in two models: a 22V17-1 which supports up to eight workstations and/or printers in any combination; and a 22V17-2 which supports up to sixteen such devices in any combination. The two models utilize the same WL# 212-3016 IOP, however, the 22V17-1 comes with one 8-port adapter plate (WL# 279-0358), and the 22V17-2 comes with two such adapter plates. (The adapter plates are mounted on the rear panel of the mainframe cabinet and house the TNC and BNC connectors to which the peripheral units are attached. The connectors on these plates are connected to the IOP via two ribbon cables. Ports 1-8 are connected to jack J1 on the 22V17 and ports 9-16 are connected to Jack J2.)

2. SWITCH SETTINGS

Device Address Switch

Each system peripheral device has a one-byte (eight bits) device address. All decimal values from 0 to 255 are legitimate addresses. Device addresses for the various peripherals are determined by the setting of switchbank SW1 on the WL# 210-7810-A IOP motherboard (ref: FIGURE 1). The settings for the device address switch are given below.

SWITCH SETTING	BIT WEIGHT
ON	
ON	
ON	
X	32
X	64
X	128
ON	
ON	



SETTINGS S4	S5	S6	DEVICE RANGE
ON	ON	ON	0-31
OFF	ON	ON	32-63
ON	OFF	ON	64-95
OFF	OFF	ON	96-127
ON	ON	OFF	128-159
OFF	ON	OFF	160-191
ON	OFF	OFF	192-223
OFF	OFF	OFF	224-255

OFF = ACTIVE

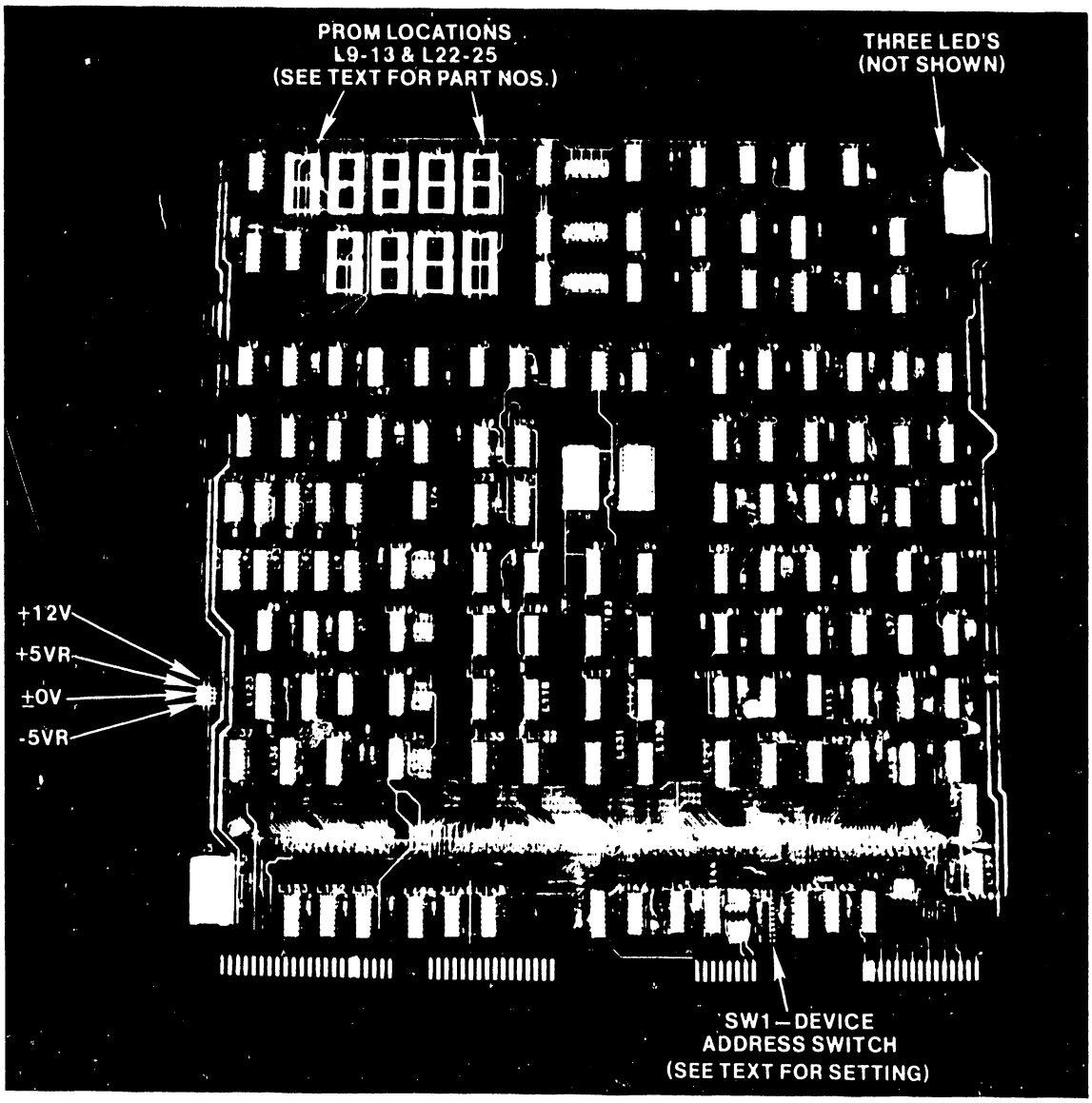
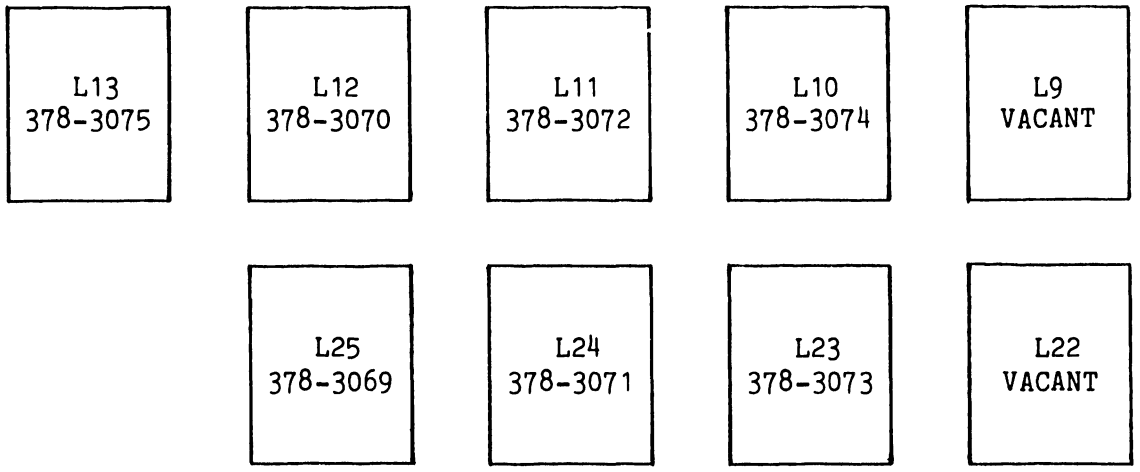


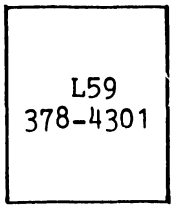
FIGURE 1 WL NO. 209-7810 IOP MOTHERBOARD (WITHOUT PROM'S)

3. PROM LOADING

WL# 210-7810-A IOP Motherboard (ref: FIGURE 1)



WL# 210-7216-B Device Adapter (ref: FIGURE 2)



4. INSTALLATION

Refer to the appropriate mainframe maintenance manual in documentation category VI.A.1 or VI.A.2 for information concerning the installation of the 22V17 IOP. After installing the IOP, check and adjust if necessary the dc voltages present on the IOP as explained in the mainframe manual. Voltage check points on the 22V17 IOP are shown in FIGURE 1 of this Notice.

5. DIAGNOSTICS

There are no diagnostics specifically designed to test the 22V17 IOP. Refer to documentation category VI.C.3 for detailed information concerning the standard workstation, printer, and/or diskette drive diagnostics which should be used to verify the operational integrity of the IOP.

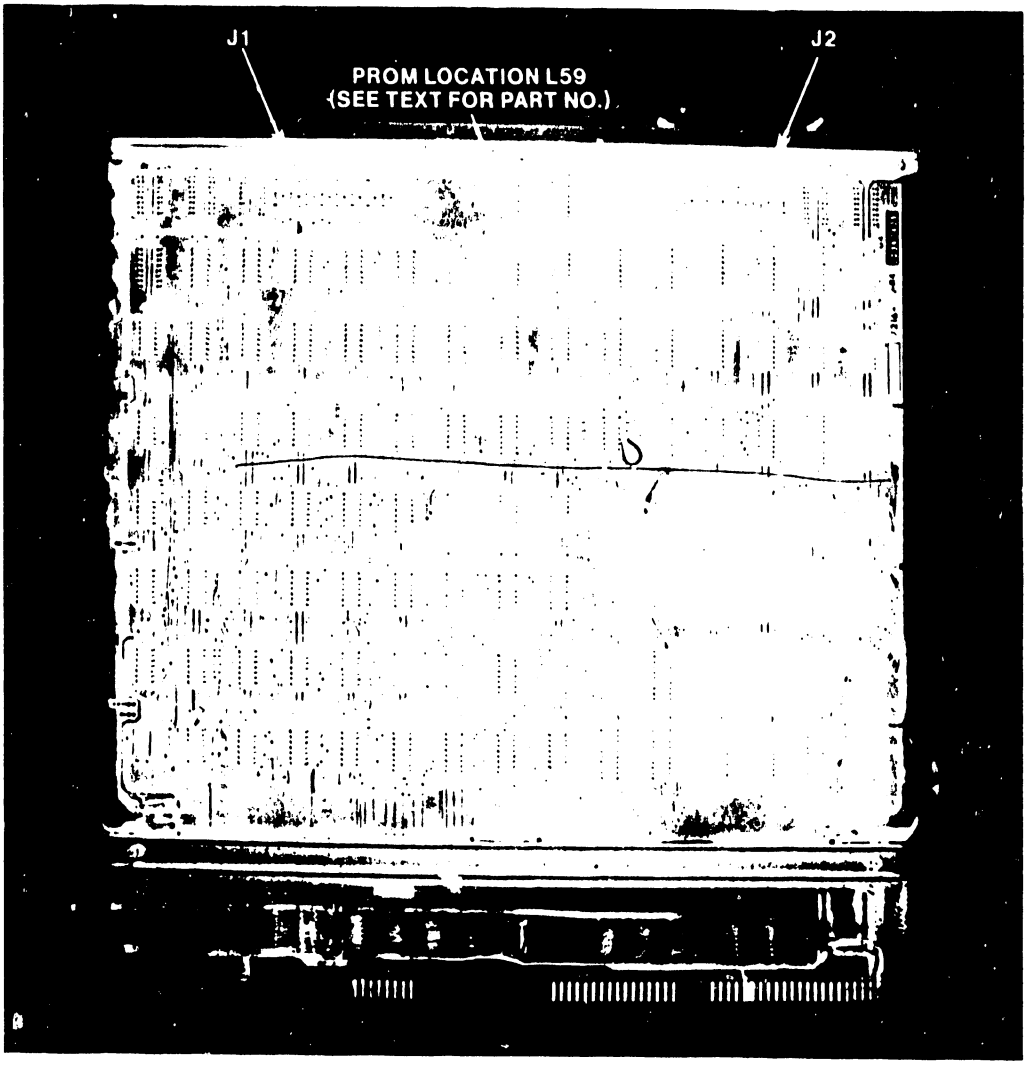


FIGURE 2 WL NO. 210-7216-B DEVICE ADAPTER

6. TROUBLESHOOTING

Three LED's are available at the top right corner of the WL# 210-7810-A IOP Motherboard to aid in troubleshooting a defective system that contains a 22V17 IOP. As viewed from the component side of the board the LED's represent left to right: *PCBRI (Processor Communication Bus Request In), *R/B (Ready/Busy), *MRI (Memory Request In). (NOTE: * means active low.)

The *PCBRI signal is activated whenever the IOP requests access to the Processor Communication Bus (PCB). The CP grants access to the requesting IOP by issuing a *PCBGS (Processor Communication Bus Grant Strobe). The LED indicating the state of the *PCBRI signal is normally off. If for some reason the PCB does not respond to the requesting IOP granting access, the LED will be on.

The *MRI signal is activated whenever the IOP requests access to the Main Memory Bus (MMB). The CP grants access to the requesting IOP by issuing a *MGS (Memory Grant Strobe). The LED indicating the state of the *MRI signal is normally off. If for some reason the MMB does not respond to the requesting IOP granting access, the LED will be on.

The *R/B signal indicates activity of the IOP.

These LED's should aid troubleshooting during two difficult circumstances:

1) When the IPL terminates unsuccessfully and no error message is displayed on the System Console screen.

2) When the system "hangs up" during normal operation.

The activity of these LED's varies based on the number of IOP's in the system, the number of active users, the system configuration, and other factors.

It may be helpful to observe the activity of the LED's during an IPL and also during normal system operation. The LED's on the disk IOP should be extremely active as the Operating System is loaded, and the LED's on the serial IOP's should show activity when the microcode for the peripherals is being loaded.

Follow the hints listed below to help correct a problem:

-- If all LED's on a single IOP are ON, replace that IOP first.

-- If the PCBRI LED on a single IOP is ON, replace that IOP first and then the PCB if needed.

-- If the MRI LED on a single IOP is ON, replace that IOP first and then the MMB if needed.

-- If the PCBRI LED on several IOP's is ON, replace the PCB first.

-- If the MRI LED on several IOP's is ON, replace the MMB first.

Some failures may occur where these LED's will offer no help in resolving the problem. They were added to the IOP Motherboard to aid the Customer Engineer in troubleshooting communication failures between the IOP and the PCB/MMB.

7. THEORY OF OPERATION

Software/Firmware

To support multiple device peripherals, the 22V17 IOP must make a distinction between the devices attached to the same port. The 22V17 utilizes a Device Routing Table (DRT) to accomplish this. (A Device Routing Table is also used by the Telecommunications IOP's.) The DRT consists of the following information:

IOP Port--Port number on IOP (0-15)
Cluster Port--Port number on cluster (always 0--for future applications)
Device--Device number of peripheral attached to port (0-3)
Type--Additional device information not used for addressing

The DRT is structured during the SYSGEN procedure and stored in the IOP RAM during IPL. When the IOP receives an IOCW (Input/Output Control Word) from the Central Processor, the IOP microcode refers to the DRT and routes data to/from the appropriate device.

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