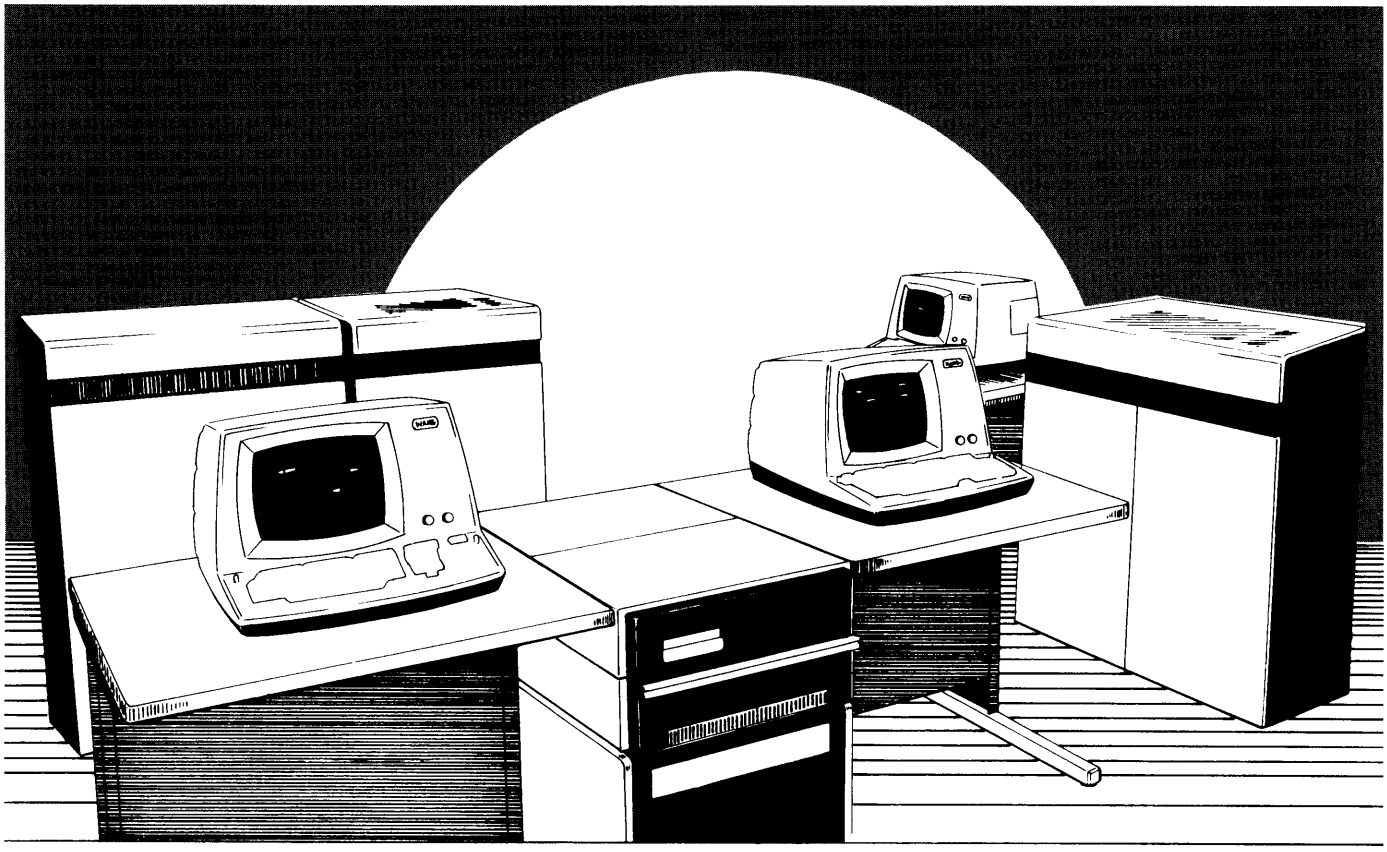
Wang Computer Systems

VS Processors



- **HIGH PERFORMANCE**
- **SYSTEM RELIABILITY**
- **MODULAR EXPANDABILITY**
- **INDEPENDENT I/O PROCESSORS**

INTRODUCTION

The Wang VS series of general-purpose computer systems incorporates virtual storage and is designed for multi-user interactive operation. Since VS software and serial peripherals are compatible with each Central Processor in the VS family, the series offers an ideal growth path from the basic configuration of the VS-50 up through the VS to the VS-100. The VS-50 supports 28 megabytes of on-line storage in its basic configuration, which can be expanded to support up to 2.3 billion bytes of on-line storage. The VS also supports up to 2.3 billion bytes of on-line storage, while the VS-100 may be configured with a maximum of 4.6 billion bytes of on-line storage. The configurations and capacities of each central processor model in the VS series are summarized in the Model Summary diagram. All the VS systems offer a range of sophisticated data management facilities, and support large on-line files.

The VS family of systems shares the same languages and utilities, compatible operating systems, and many of the same Input/Output Processors (IOPs) and peripheral devices. The high-level languages available are COBOL, RPG II and BASIC, with PL/I and FORTRAN under development. The VS family of systems also supports Assembler language and a Procedure language, which allows operational sequences to be performed without user interaction. An Advanced Data Management System is available, and a Data Base Management System has been announced. Magnetic tape drives, several types of disk drives, a variety of printers, and telecommunications are supported. A word processing option (directly compatible with Wang's popular Office Information Systems) is also supported. Further details of these and other features of the VS product line are contained in the following VS Data Sheets: *VS Data Communications, VS Data Base Management System,*

VS KEYENTRY, VS Languages, VS MAILWAY, VS Peripherals, VS 2246C Serial Workstation, VS System Software, and *VS/WP Integrated Information System.*

The principal design goals of the Wang VS family are high-performance, modular expandability, high system reliability, and ease of use. To achieve these goals, the VS systems are composed of several processing modules: a Central Processor, main memory, multiple independent IOPs which control peripheral devices, and a system bus which integrates all of these components. The high-speed Central Processor supports a very powerful machine instruction set and controls the operation of the other processors. The main memory system provides a high data-exchange rate with processors competing for memory service on a cycle-stealing basis.

On the VS-100, an auxiliary high-speed memory, called cache memory, is used to provide high-speed data access to the Central Processor, thus overcoming the discrepancy between the cycle speeds of main memory and the Central Processor. The System Bus Controller on the VS-100 functions as the memory controller and provides flexible communication between the Central Processor and IOPs, as well as providing diagnostic data. On the VS-100, a Bus Adapter supports an I/O subsystem consisting of a bus, IOPs, and peripherals.

The use of multiple discrete processing modules contributes to a significant increase in overall system performance as well as improved reliability and ease of maintenance. The modular design also makes it easy to increase memory size and add new peripherals when future expansion is necessary.

Model Summary

Model	VS-50	VS	VS-100
Maximum Memory	512K	512K	2048K
Minimum Memory	128K	128K	256K
Maximum Number of IOPs	7	8	16
Maximum Number of Disk IOPs	2	2	4
Maximum Disk Capacity (billion bytes)	2.3	2.3	4.6
Included On-line Storage	29.26M	308K	308K
Maximum Number of Workstations	32	32	128

THE VS-50, VS, AND VS-100 PROCESSORS

The VS-50, VS, and VS-100 are compatible processors which offer a wide range of alternatives in terms of processing rate, storage capabilities, and configuration options. All processors share a common machine instruction set, enabling each processor to run the same utilities and compatible operating systems. User programs which run on one system will run, without modification, on either of the other systems. This software compatibility, at both object and source code levels, is especially valuable to users considering long-term growth prospects.

The VS-100 supports all serial peripherals supported by the VS-50 and the VS. Expansion from the VS-50 or VS to the VS-100 can thus be achieved without modification or replacement of existing peripherals. Parallel devices, however, are supported only by the VS model Central Processor. The ability to transport software and peripherals significantly reduces the total expense and disruption involved in expanding from a smaller Central Processor to a larger one.

Along with a high degree of compatibility with the other processors in the VS family, the VS-100 offers many improvements in the realm of processing capability and system features.

The VS-50, in its basic configuration, provides 128K bytes of main memory; through memory additions, the VS-50 and VS provide a maximum of 512K bytes (one-half megabyte) of main memory. The VS-50 is supplied with one serial workstation, and can support up to five more serial workstations in its basic configuration. Through additions to the systems, both the VS-50 and VS can support up to 32 workstations. The VS-50 is also supplied with an internal 28-megabyte fixed disk drive and a 1.26-megabyte diskette drive which supports standard Wang 256-byte sectoring and various soft sector options, some with 3741 formatting compatibility. With additional disk drives, the VS-50 can support up to 2.3 billion bytes of on-line storage. The VS also provides a maximum of 2.3 billion bytes of on-line storage. IOPs on the VS-50 and the VS have direct access to main memory. A 16-bit data path to memory enables the Central Processor and all IOPs to access one halfword (16 bits) of memory on each memory cycle.

The VS-100 provides a redesigned and expanded architecture based on a much faster Central Processor. The VS-100 supports up to 2048K bytes (2 megabytes) of main memory and can handle up to 128 workstation users concurrently. Additionally, the VS-100 supports up to 4.6 billion bytes of on-line storage. Two new architectural components, a separate cache memory and a system bus with a 64-bit data path, enhance performance further. The cache memory serves as a high-speed auxiliary memory area used by the Central Processor as a buffer between itself and main memory. The use of a system bus with a 64-bit

data path to memory permits the Central Processor and IOPs to read or write a doubleword (64 bits) on each memory access. The net effect of these new features is a dramatic improvement in total system performance on the VS-100.

The three Central Processors in the VS series share the same approach to handling I/O operations. On the VS-100, however, IOPs do not communicate directly with main memory, but are connected to a Bus Adapter (BA). The principal function of the BA is to interface between the 16-bit data path of the IOPs and the 64-bit data path of the system bus. Each BA controls up to eight IOPs; since the VS-100 supports a maximum of two BAs, the total number of IOPs supported is effectively doubled from 8 to 16, with a corresponding increase in the number of peripheral devices which can be attached.

The Wang VS-50, VS, and VS-100 offer the user a wide range of choices in terms of cost, performance, and expandability, with the assurance of complete software, data file, and serial peripherals compatibility.

VS-50 COMPUTER SYSTEM

The VS-50, in its basic configuration, is the newest system in the VS series. It is designed to serve as an entry-level system, easily expandable as user requirements change; and as a component in a distributed data processing system, for departmental use in large organizations. System architecture, and Central Processor and main memory characteristics are the same for the VS-50 and the VS.

Main memory ranges in size from 128K bytes to a maximum of 512K bytes in increments of 128K bytes. Word processing is supported on any VS-50 with 256K bytes of memory, from VS workstations 2246C and 2266C, which have combined data processing/word processing keyboards. All VS telecommunications options, including MAILWAY™, Wang's electronic mail facility, are available on the VS-50.

VS-50 Peripherals and IOPs

The basic configuration of the VS-50, with 128K byte memory, supports up to six serial workstations (one of which is included with the purchase of each VS-50 system) and any VS serial printers, up to a total of eight devices. The VS-50, which supports only serial devices, is supplied with one eight-port IOP, Model 22V17-1, for serial workstations and printers. With an optional 16-port IOP, Model 22V17-2, the basic configuration of the VS-50 can support additional printers.

The Central Processor cabinet of the VS-50 contains a sealed 14-inch fixed Winchester disk drive and controller. This disk provides a total of 28 megabytes of online storage; approximately 9 megabytes of the fixed disk are reserved for system software. Also contained in the Central Processor cabinet of the VS-50 is a diskette drive which accepts both hard and soft sectored diskettes, with a maximum capacity of 1.26 megabytes, and provides facilities for system backup and software transfer. The diskette drive can be accessed by any workstation on the VS-50 system for data processing functions. The diskette drive can also accept and create diskettes compatible with Wang's WP/OIS and 2200 Business Systems and other VS systems, as well as IBM-formatted diskettes.

The serial workstation supplied with the VS-50 supports all VS data processing functions except KEYENTRY, and also serves as the Operator's Console. This workstation must be located within 25 feet of the Central Processor cabinet.

VS-50 Expandability

The VS-50 can be expanded to a maximum configuration similar to that of the VS. All the disk drives, tape drives, and serial peripherals available for the VS are also supported on the VS-50. Up to six user-selected IOPs may be added to the system, in addition to the Model 22V17-1 Serial Workstation/Printer IOP supplied with each VS-50.

VS COMPUTER SYSTEM

The VS is a small-to-medium-scale system intended for a commercial multi-user environment. VS hardware is relatively simple in design, combining reliable operation with good performance and ease of maintenance. The basic architectural components are an efficient Central Processor, main memory, and up to eight independent IOPs which control all peripheral devices. A dual system bus provides communication between the Central Processor, IOPs, and main memory, as illustrated in the following diagram of VS Architecture.

The VS Central Processor

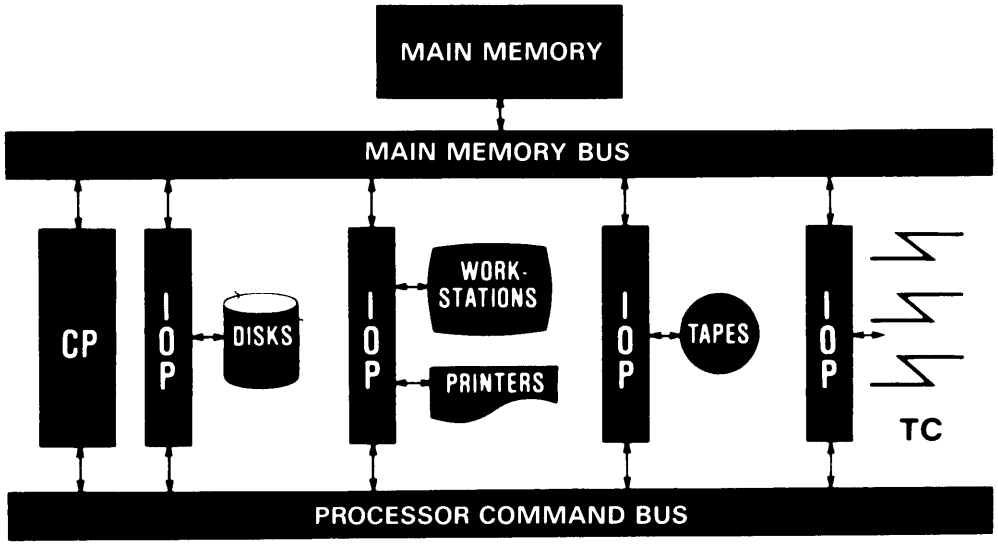
The Central Processor executes instructions and controls the initiation and termination of data transfer between I/O devices and main memory. On the VS, the Central Processor communicates with main memory via the Main Memory Bus (MMB), which provides a 16-bit data path. The MMB is also used by IOPs communicating with memory.

The VS Central Processor supports binary, packed-decimal, and floating-point arithmetic. The Central Processor includes sixteen 32-bit, general-purpose registers and four 64-bit, floating-point registers. The VS machine instruction set is very similar to the 370 machine instruction set.

Communication between the Central Processor and the IOPs is performed via the Processor Command Bus (PCB). When an I/O operation to or from a particular device is necessary, the Central Processor instructs the IOP controlling that device to begin the I/O transfer. At that point, the IOP assumes all responsibility for communicating with the device and for routing the data to or from the specified location in main memory. Like the

MAILWAY ™ is a trademark of Wang Laboratories, Inc.

VS ARCHITECTURE



Central Processor itself, each IOP can access main memory directly via the MMB. The Central Processor is thus free to perform other processing while the data transfer takes place. This arrangement permits extremely efficient handling of I/O data transfers and results in very good performance for I/O-intensive programs. To further improve total throughput, the cycle times of the Central Processor and the MMB are synchronized with the cycle time of main memory, eliminating the necessity of a synchronization check prior to performing a memory access.

The VS Main Memory

Main memory is dynamic Random Access Memory (RAM). On the VS, main memory ranges in size from 128K bytes to a maximum of 512K bytes in increments of 128K bytes. The basic unit of memory is a halfword (16 bits); however, the addressing structure permits individual bytes to be accessed by a program. The Central Processor and all IOPs communicate with main memory via the MMB. The architecture thus permits one halfword (16 bits) to be read or written on each memory cycle. To improve reliability, the VS supports automatic single-bit error correction, and detection of most multi-bit errors.

The VS I/O Processors

Control of external devices is handled by intelligent IOPs, each of which is specialized to control one or more devices of a particular type. On the VS, each IOP communicates directly with main memory via the MMB. When a command to initiate an I/O operation is received from the Central Processor, the IOP accesses the specified I/O device and begins the data transfer. The IOP has responsibility for directing data to or from the appropriate location in memory and for performing most I/O error-checking (and, where possible, correction) for its devices. These operations therefore occur independently of, and concurrently with, the activities of the Central Processor.

VS Expandability

The VS provides a smooth, continuous growth path from a small, relatively inexpensive configuration consisting of 128K of memory, two or three workstations, a single printer, a diskette drive, and a disk drive. The VS can be expanded to a maximum configuration of 512K bytes of memory, with up to 32 workstations, multiple printers, and more than 2 billion bytes of disk storage. All of this expansion can be carried out with no changes to user application software, using the same operating system and Central Processor.

If further expansion is required, the VS Central Processor can be replaced with a VS-100 Central Processor, which offers faster performance, larger memory (up to 2 megabytes), and supports many more peripheral devices. Most VS peripherals (excluding parallel workstations and printers, and diskette drives) are directly compatible with the VS-100 and can be detached from the VS Central Processor and attached to the VS-100 without modification. Finally, because the VS-100 supports the same machine instruction set as the VS, along with same operating system and utilities, expansion from a VS to a VS-100 can be accomplished with no changes in user software and no retraining of personnel.

VS-100 COMPUTER SYSTEM

The VS-100 is the medium-to-large-scale model in the VS family which features faster performance, larger

main memory, and support for many more peripherals than the VS models previously discussed. The basic architectural components are an efficient Central Processor, main memory, a cache memory, a system bus and System Bus Controller (SBC), one or two BAs, and up to 16 independent IOPs which control all peripheral devices, as illustrated in the following diagram of VS-100 Architecture.

The VS-100 Central Processor

The nucleus of the VS-100 system is its high-speed Central Processor. The Central Processor performs instruction execution and oversees the initiation and termination of the I/O operations, communicating with main memory and the IOPs via the system bus. In order to provide the best possible Central Processor throughput, both the system bus cycle and the main memory cycle are synchronous with the Central Processor cycle.

The VS-100 Central Processor supports binary, packed-decimal, and floating-point arithmetic. The Central Processor includes sixteen 32-bit, general-purpose registers and four 64-bit, floating-point registers. The VS-100 machine instruction set is very similar to the 370 machine instruction set.

The Central Processor can control the state of external VS-100 processors and has initialization control over all processors attached to the VS-100 system bus. The Central Processor can effect direct initialization of any attached IOP and its peripheral devices.

The VS-100 Main Memory

The VS-100 main memory system contains up to eight 256K byte memory modules and the SBC. The SBC performs the functions of the memory controller. Main memory is dynamic Random Access Memory (RAM). The basic unit of the main memory is a 32-bit data word. However, memory is also byte-addressable.

Each memory module holds either even- or odd-addressed words. The memory module arrangement supports 64-bit read or write operations. All read operations cause a doubleword (8 bytes or 64 bits) to be accessed. Write operations can be performed in aligned units of 1, 2, 4, or 8 bytes.

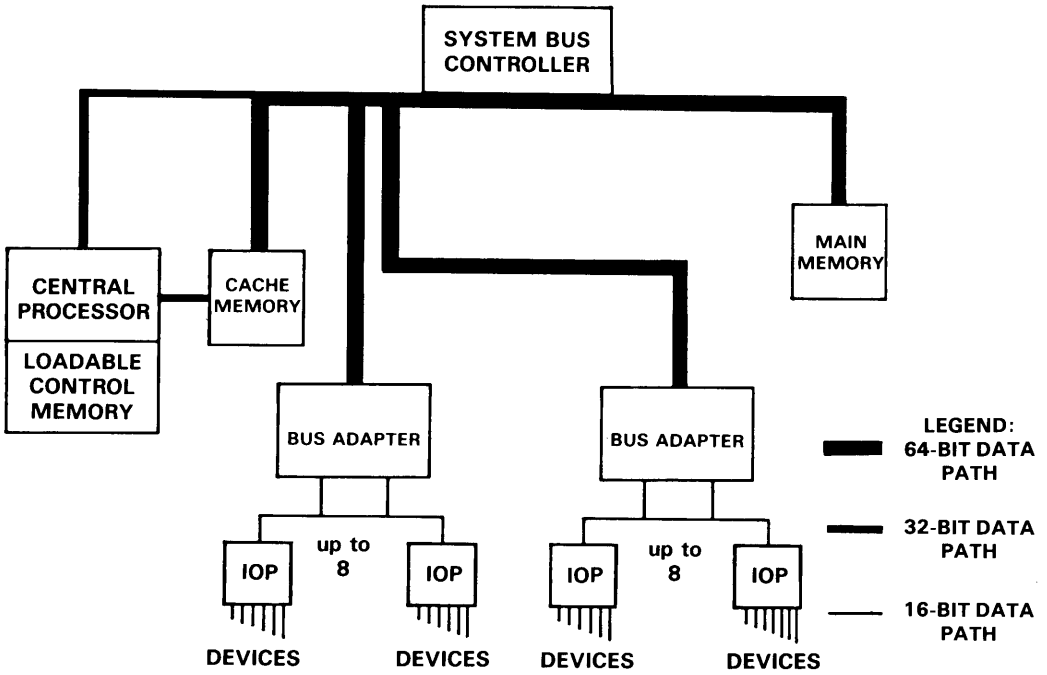
The VS-100 chassis can hold eight memory boards for a maximum main memory size of 2 megabytes. Main memory is expanded in 256K byte increments.

The VS-100 Cache Memory

The Central Processor cache memory is an auxiliary, high-speed 32K byte memory which provides a buffer between the Central Processor and main memory. The cache memory provides high-speed data read access to the Central Processor. The utilization of cache memory overcomes the discrepancy between the memory cycle speed and the faster data-access rate of the Central Processor.

The cache memory uses a direct-mapped organization, indexed by physical address. The cache memory

VS-100 ARCHITECTURE



always contains a subset of the data found in main memory, and remains consistent when other processors modify main memory. Cache memory is accessed by the Central Processor whenever a Central Processor read or write operation is performed. A write-through strategy is employed for updating both the cache and main memory when Central Processor write operations are performed.

The Central Processor uses the cache memory as its buffer, that is, each time a read of memory is required, the cache memory is accessed first. If the cache did not contain the data required by the Central Processor, a doubleword is read from main memory and used to update a pair of cache entries (in parallel). Thus, main memory is directly accessed only when the requested data has not already been loaded into the cache.

The VS-100 System Bus and Bus Controller

The system bus is the primary communication path between the Central Processor, main memory, and the Bus Adapter(s). The system bus provides a 64-bit data path between the components of the VS-100.

The System Bus Controller (SBC) controls the usage of the VS-100 system bus cycles. The SBC serves as both a memory controller and a communication controller between processors. The SBC contains a bus log to capture error cases and aid in the diagnostic process. It also provides flexible inter-processor communication service for generalized message communication and interrupt service between processors.

All Central Processor commands to external processors are passed through the SBC. The major interface between the SBC and Central Processor is the External Control Register (ECR), which is held at the SBC. The ECR allows the Central Processor to control external events and to communicate with the other processors via interrupt services and other forms of communication.

The VS-100 Bus Adapter

The Bus Adapter (BA) is an intermediate processor between the VS-100 Central Processor and the IOPs. The main services the BA provides are those of data-buffering and routing.

The BA is used to support a modular I/O subsystem consisting of an outboard bus (similar to that on the VS), IOPs, and attached devices. The BA serves as an interface between the 16-bit IOP data path and the 64-bit data path of the VS-100 system bus. The IOPs use 16-bit-wide read and write operations, while data is transferred to and from memory 64 bits at a time. The BA automatically blocks data going from an IOP to memory and deblocks data going from memory to an IOP. Thus, the BA effectively utilizes the high-speed, 64-bit system bus path during I/O operations. The BA has access to standard read and write service on the VS-100 bus.

The BA supports communication between the Central Processor and the IOPs. The BA receives Central Processor commands directly and also requests Central Processor interrupt service, using standard system bus protocols.

The VS-100 system can support one or two BAs. Each BA supports up to eight IOPs.

The VS-100 I/O Processors and Peripherals

Peripheral devices are interfaced to the VS-100 system through the use of IOPs. These IOPs are specialized to support certain types and numbers of peripheral devices. An IOP acts as a controller for its attached devices and provides main memory services required in the course of handling I/O operations.

Because the IOPs perform memory access in units of 16 bits, they are interfaced to the 64-bit data paths of the VS-100 system bus by means of the BA.

I/O initiation is accomplished by sending a command to the appropriate IOP. The IOP performs all I/O control operations independent of the Central Processor. The IOP issues an interrupt request when its operation is completed. Thus, the Central Processor requires only modest communication facilities in order to handle I/O operations. The Central Processor must have the ability to issue a command to an IOP, and it must be able to sense interrupt requests from the IOP and to grant such requests.

The VS-100 Diagnostic Features

System reliability and serviceability are enhanced on the VS-100 by using a combination of hardware features, including powerful off-line diagnostics and on-line error isolation and error recovery. Some of the most effective features are those which support automatic error recovery at the hardware level.

The main memory supports the automatic correction of single-bit errors and the detection of most multi-bit errors. Main memory also provides the ability to directly control error correction codes, which is useful not only for diagnosing the error-coding feature but also for generating error cases and testing error-handling features in other components. Diagnostic tests for explicitly verifying processor traps or status bits can be created without physical changes being required.

A Bus Transaction Log (BTL) is provided in the SBC to record all the appropriate information in case of main memory or cache errors.

VS-100 Expandability

The VS-100 is provided with a minimum of 256K bytes of memory (expandable by 256K byte modules to 2048K bytes, or two megabytes). The maximum on-line disk storage capacity is 4.6 billion bytes. The VS-100 can support a maximum of 16 IOPs, each specialized to support certain types and numbers of peripheral devices. Up to 128 workstations can be attached.

VS-50, VS, AND VS-100 IOPs

All IOPs available to control peripheral devices on the VS-50, VS, and VS-100 are described in the following list. More detailed specifications and descriptions of all VS system IOPs may be found in the *VS Peripherals Data Sheet.*

22V01 Parallel Workstation/Printer IOP

Supports up to three 2246P Parallel Workstations and one parallel printer or four parallel workstations. Available only with the VS Model Central Processor.

22V02 Diskette IOP

Supports one 2270V System Diskette Drive (308 kilobytes). Available only with the VS Model Central Processor.

22V05-2 and 22V25-2 Seven- and Nine-Track Tape Drive IOPs

Support up to four 2209V-1 and/or 2209V-2 Nine-Track Magnetic Tape Drives and/or 2209V-3 Seven-Track Magnetic Tape Drives, in any combination. The 22V05-2 IOP is available with the VS-50 and VS Model Central Processors; the 22V25-2 IOP is available with the VS-100 Model Central Processor.

22V06 and 22V26 Communications IOPs

Available in three versions to support synchronous communications:

- 22V06-1 and 22V26-1 — Support one synchronous communications line.
- 22V06-2 and 22V26-2 — Support two separate synchronous communications lines.
- 22V06-3 and 22V26-3 — Support three separate synchronous communications lines.

At least one line supports an automatic calling unit. The 22V06 Models are available with the VS-50 and VS Model Central Processors; the 22V26 Models are available with the VS-100 Model Central Processor.

22V07 Serial Workstation/Printer IOP

Supports serial workstations (except VS Archiving Workstations) and printers. Model 22V07 IOPs are supported only on the VS Model Central Processor. Available in two versions:

- 22V07-1 — Supports up to eight 2246S Serial Workstations, 2246C Serial Workstations with word processing capability, or serial printers, in any combination.
- 22V07-2 — Supports up to sixteen 2246S Serial Workstations, 2246C Serial Workstations with word processing capability, or serial printers, in any combination.

22V08 and 22V28 Disk Drive IOPs

Support up to four 2265V and 2280V Disk Drives in any combination. The 22V08 is available with the VS-50 and VS Model Central Processors; the 22V28 is available with the VS-100 Model Central Processor.

22V17 and 22V27 Serial Workstation/Printer IOPs

Archiving Workstation Models 2266S and 2266C are supported by the 22V17 and 22V27 IOPs, and are *not* supported by the 22V07 IOPs. One 22V17-1 Workstation/Printer IOP is supplied with each VS-50, and one 22V27-1 Workstation/Printer IOP is supplied with each VS-100. Available in two versions:

- 22V17-1 and 22V27-1 — Support up to eight 2246S Serial Workstations, 2246C Serial Workstations with word processing capability, Archiving Workstation Models 2266S and 2266C, or serial printers, in any combination.
- 22V17-2 and 22V27-2 — Support up to sixteen 2246S Serial Workstations, 2246C Serial Workstations with word processing capability, Archiving Workstation Models 2266S and 2266C, or serial printers, in any combination.

The 22V17 IOPs are available with the VS-50 and VS Model Central Processors; the 22V27 IOPs are available with the VS-100 Model Central Processor.

VS-100 ADDITIONAL BUS ADAPTER

CO-1001 Additional Bus Adapter

For VS-100 systems using more than eight IOPs or more than two *disk* IOPs, an additional bus adapter is needed to serve as an intermediary between the Central Processor and the IOPs, supporting up to an additional eight IOPs.

VS-50, VS, AND VS-100 PERIPHERAL DEVICES

This section lists peripheral devices available for configuration with the VS-50, VS, and VS-100 Central Processors. The VS-50 also includes a 28-megabyte fixed Winchester disk drive, located within the Central Processor cabinet. More detailed specifications and descriptions of all peripherals supported by the VS family of Central Processors are available in the *VS Peripherals Data Sheet.* Peripherals supported only by the VS are indicated by shading; all other peripherals are compatible with the VS-50, the VS, and the VS-100.

Workstations

2246P	Parallel Workstation
2246S	Serial Workstation
2246R	Remote Workstation
2246C	Serial Workstation with word processing capability
2266S-1	308-Kilobyte Serial Archiving Workstation (AWS) for hard sectored diskettes
2266S-2	1.26-Megabyte Serial AWS for soft sectored diskettes
2266S-3	1.26-Megabyte Serial AWS for hard and soft sectored diskettes
2266C-1	308-Kilobyte Serial AWS with word processing capability, for hard sectored diskettes

2266C-3	1.26-Megabyte Serial AWS with word processing capability, for hard and soft sectored diskettes

Disk Drives

2265V-1	75-Megabyte Disk Drive
2265V-2	288-Megabyte Disk Drive
2280V-1	30-Megabyte Fixed/Removable Disk Drive
2280V-2	60-Megabyte Fixed/Removable Disk Drive
2280V-3	90-Megabyte Fixed/Removable Disk Drive

Tape Drives

2209V-1	Nine-track, 1600 bit-per-inch, 120 kilobyte-per-second, 75 inch-per-second Magnetic Tape Drive
2209V-2	Nine-track Magnetic Tape Drive • 800 bits-per-inch, 60 kilobytes-per-second, 75 inches-per-second • 1600 bits-per-inch, 120 kilobytes-per-second, 75 inches-per-second
2209V-3	Seven-track, 556 or 800 bit-per-inch, 60 kilobyte-per-second, 75 inch-per-second Magnetic Tape Drive

Printers

2221V	Parallel Matrix Character Printer (132 columns/200 characters per second)
2231V-2	Parallel Matrix Character Printer (132 columns/120 characters per second)
2273V-1	Parallel Band Printer (250 lines per minute/48-, 64-, and 96- character sets, for remote site use only)
5521	Serial Matrix Character Printer (132 columns/200 characters per second)
5531-2	Serial Matrix Character Printer (132 columns/120 characters per second)
5570	Serial Solid Character Chain Line Printer (600 lines per minute)
5571	Serial Solid Character Chain Line Printer (430 lines per minute/96-character set)
5573	Serial Band Printer (250 lines per minute/48-, 64-, and 96- character sets)
5574	Serial Band Printer (600 lines per minute/48-, 64-, and 96- character sets)
6581W	Serial Daisy Printer (30 characters per second)
6581WC	Serial Daisy Printer (30 characters per second)

Remote Communications MSU

2247V-4	Remote location Modem Sharing Unit (supports up to four 2246R Remote Workstations with optional remote parallel printers)

VS Family Machine Instruction Set

The VS-50, VS, and VS-100 all share a common (non-privileged) machine instruction set. This instruction set includes all the instructions found in the IBM 370 Commercial Instruction Set. It also includes the long-format, normalized floating-point instructions and a number of additional features which are not found in the 370 set. The VS family machine instruction set includes the following features.

- A number of stack-oriented instructions support standard call and return sequences for both system and user maintained pushdown stacks. The instructions include support for a protected back chain of both program "calls" and Supervisor calls (SVCs). The system stack provides a powerful and efficient Operating System interface for all VS user programs.
- Linked list instructions for queue and semaphore manipulation are supported.
- Instructions for branching and for address generation "relative to the program counter" are supported.
- Instructions for data compression and expansion are included. Instructions for efficient packing and manipulation of ASCII-codes are also included.

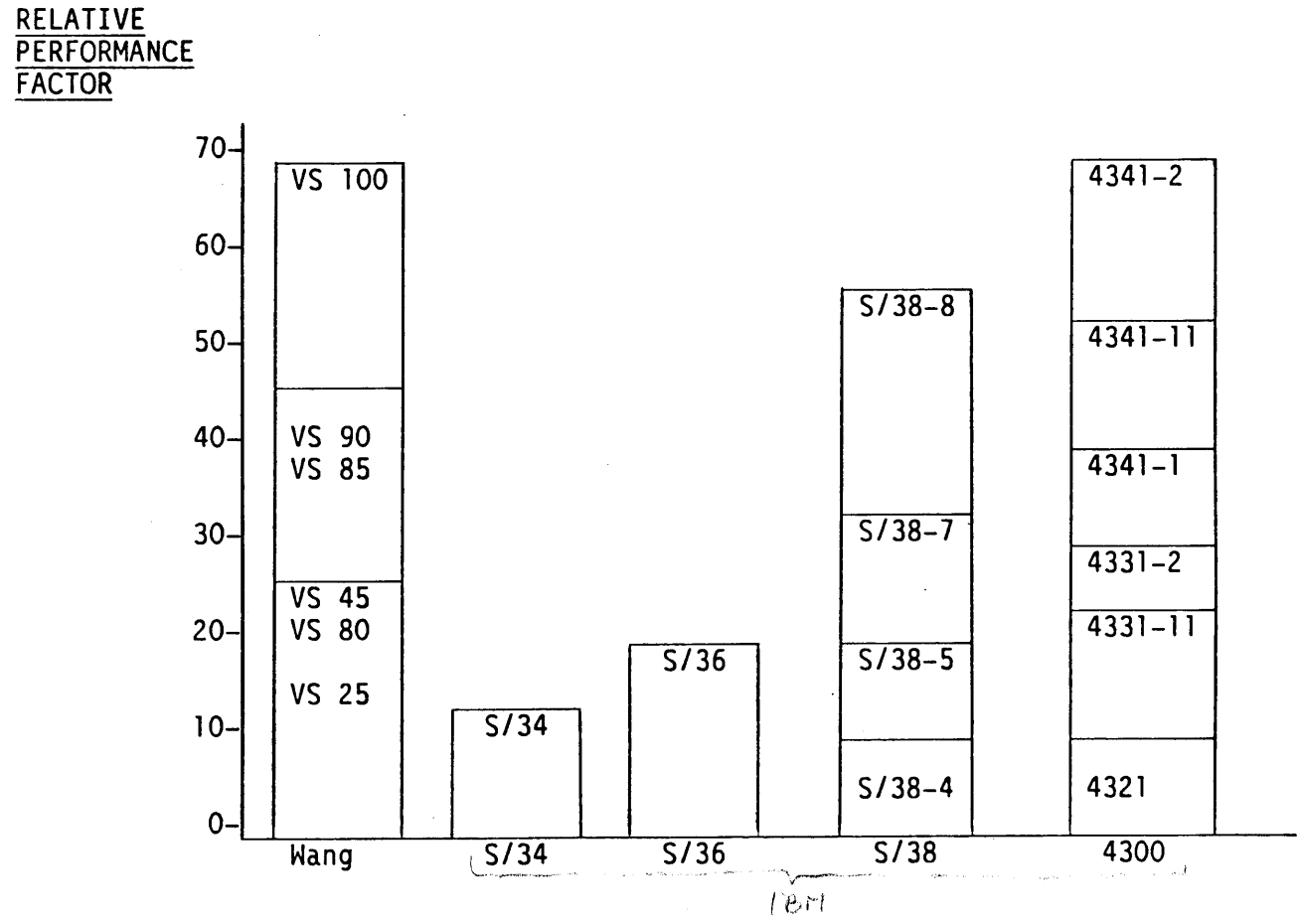
WANG LABORATORIES, INC.
ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL. (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

This document was set on a Wang typesetter.

Printed in U.S.A.
800-2105-03
9-82-15M

Appendix A

Relative
Performance Estimates
of
Wang VS Systems
and
IBM S/34, S/36, S/38, and 4300



Notes: (1) Table based on an analysis appearing in Computerworld regarding relative performance. The IBM S/34 and S/36 are best estimates.

(2) Relative performance of any system will vary on a wide number of variables including, in part, operator performance, job mix, fine "tuning" of system software, and individual applications being processed.