WANG

3404

VS/WP/OIS
ARCHIVING WORKSTATIONS

Models:

2266C-1, -3
2266S-1, -2, -3
2276C-1, -3
AWS-1, -4
5740

Customer Engineering
Product Maintenance Manual **741-0865-A**

COMPANY CONFIDENTIAL

PREFACE

This document is the Product Maintenance Manual (PMM) for the Wang Archiving Workstations. The manual is organized in accordance with Customer Engineering Technical Documentation's approved PMM outline. The scope of this manual reflects the type of maintenance philosophy selected for this product.

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with sufficient instructions to operate, troubleshoot, and repair the Archiving Workstations. The manual will be updated on a regular schedule or as necessary. Such updates will be published either as Publication Update Bulletins (PUBs) or as full revisions.

Fourth Edition (August 1985)

This edition of the Archiving Workstations PMM manual obsoletes documents 729-0865-B and 742-0865. Use of the material in this document is authorized only for the purpose stated in the Preface, above.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd.)

CHAPTER 4 INSTALLATION **Page**

CHAPTER 5 PREVENTIVE AND CORRECTIVE MAINTENANCE

TABLE OF CONTENTS (Cont'd.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd.)

LIST OF TABLES

CHAPTER 1 INTRO-DUCTION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 SCOPE AND PURPOSE

This manual provides installation, operation, maintenance, and troubleshooting information for Archiving Workstations used across the Wang WP/OIS and VS product lines. Section 1.5.1 details the VS models covered while section 1.5.2 details the WP/OIS models covered.

Figure 1-1 shows a representative Archiving Workstation (AWS) model, including the Archiving Master and the Terminal, and identifies the terminology used throughout this manual for the product and its individual components.

This manual describes in detail the subassemblies of the Archiving Master and the Terminals with the exception of the the Floppy Disk Drive unit in the Archiving Master. This unit is the Shugart 850/851 in the VS AWS, and the Shugart 901 in the WP/OIS AWS. While certain details of these units are covered herein, it will be necessary to refer to the Original Equipment Manufacturer (OEM) documentation for complete information on these units.

1.2 APPLICABLE DOCUMENTATION

A complete listing of technical documentation is located in the Technical Documentation Catalog/Index (742-0000). Other product documentation is identified in the Corporate Resource Catalog (700-7647).

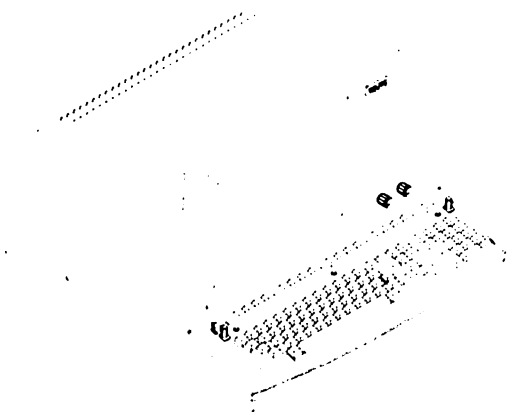
1.3 DIAGNOSTICS

In WP/OIS systems, the diagnostic tests used with the AWS are system-dependent. Table 1-1 lists currently available diagnostic programs used for the WP/OIS AWS, along with their part numbers. Documentation is supplied with diagnostic packages.

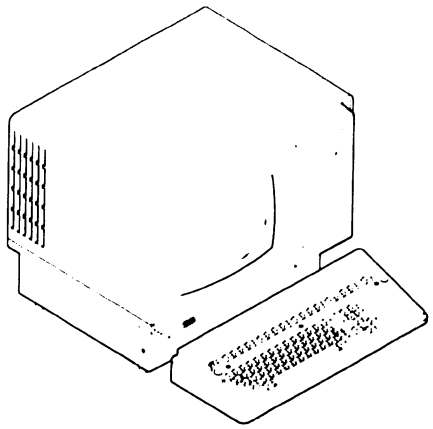
Revisions of diagnostic packages are normally mentioned in Technical Service Bulletins (TSBs).

Table 1-1
WP/OIS AWS Diagnostics

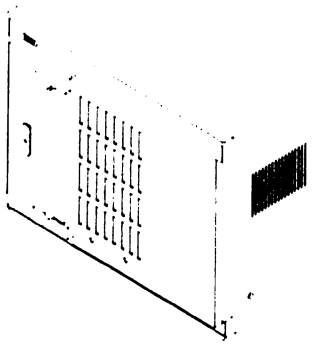
Package Name	Part Number		Rev.
OIS On-line Device 3(1).....	195-2549-3	(8")	2330
OIS On-line Device 3(1).....	195-2549-9	(5 1/4")	2330



5506 TERMINAL



5730 TERMINAL



ARCHIVING MASTER

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Figure 1-1 Archiving Workstation

In VS systems, diagnostics are resident in the system volume in library @SYSTST@, as well as being available on diskette under the part numbers listed in Table 1-2. Documentation is supplied with diagnostic packages.

Revisions of diagnostic packages are normally mentioned in Technical Service Bulletins (TSBs).

Table 1-2
VS AWS Diagnostics

Package Name	Part Number	Rev.	Type
FTU	195-2626-3	6385	Stand-Alone
FTU, Any Rev. O/S, No Soft-Sector Support	702-0099	3.8	On-Line
FTU, O/S 5.0 or Later, With Soft-Sector Support	702-0099A	61C4	On-Line
VS Device 3	195-2604-3	2334	On-Line
VS 25 BP-Based Diagnostic Monitor, Rev. 2 BP Only	732-0018	2170	Stand-Alone
FTU25, VS 25 FTU, Rev. 2 BP Only.	732-0019	6111	Stand-Alone
VS 25 BP-Based Diagnostic Monitor, Rev. 3 BP Only	732-0021	22C5	Stand-Alone
FTU25, VS 25/45 FTU, Rev. 3 BP Only	732-0036	6111	Stand-Alone

1.4 AWS FEATURES

Addition of an AWS to either a VS or WP/OIS system affords the user direct archiving of data stored on the system, without having to access the master unit's disk drive. Data is archived on 8-inch floppy diskettes. The AWS supports the same system functions as any other workstation in the system in addition to the archiving function. Telecommunications is optionally available. (See section 1.9.) Depending on the model, the AWS supports a variety of diskette media formatting methods, either hard-sector, soft-sector, or both in some models.

1.5 AWS GENERAL DESCRIPTION

The Archiving Workstation includes two units which operate together to perform the desired functions. Referring to Figure 1-1, the two units are the Archiving Master and the Terminal. The Archiving Master contains the Floppy Disk Drive unit along with its associated control logic boards. Also contained in the Archiving Master are the boards usually associated with the Terminal, and a power supply.

The Terminal contains only the CRT monitor and its associated electronics and power supply, along with a keyboard. The Terminal is connected to the Archiving Master where the logic circuits necessary for Terminal operation reside.

1.6 AWS CONFIGURATIONS

1.6.1 CONFIGURATION IN VS SYSTEMS

Table 1-3 lists the models available for VS system application, along with the individual hardware subassemblies found in each model. Figure 1-2 is a block representation of the VS AWS and its internal subassemblies. The model number designations and features of the VS AWS models are defined below.

2 2 x 6 y - z

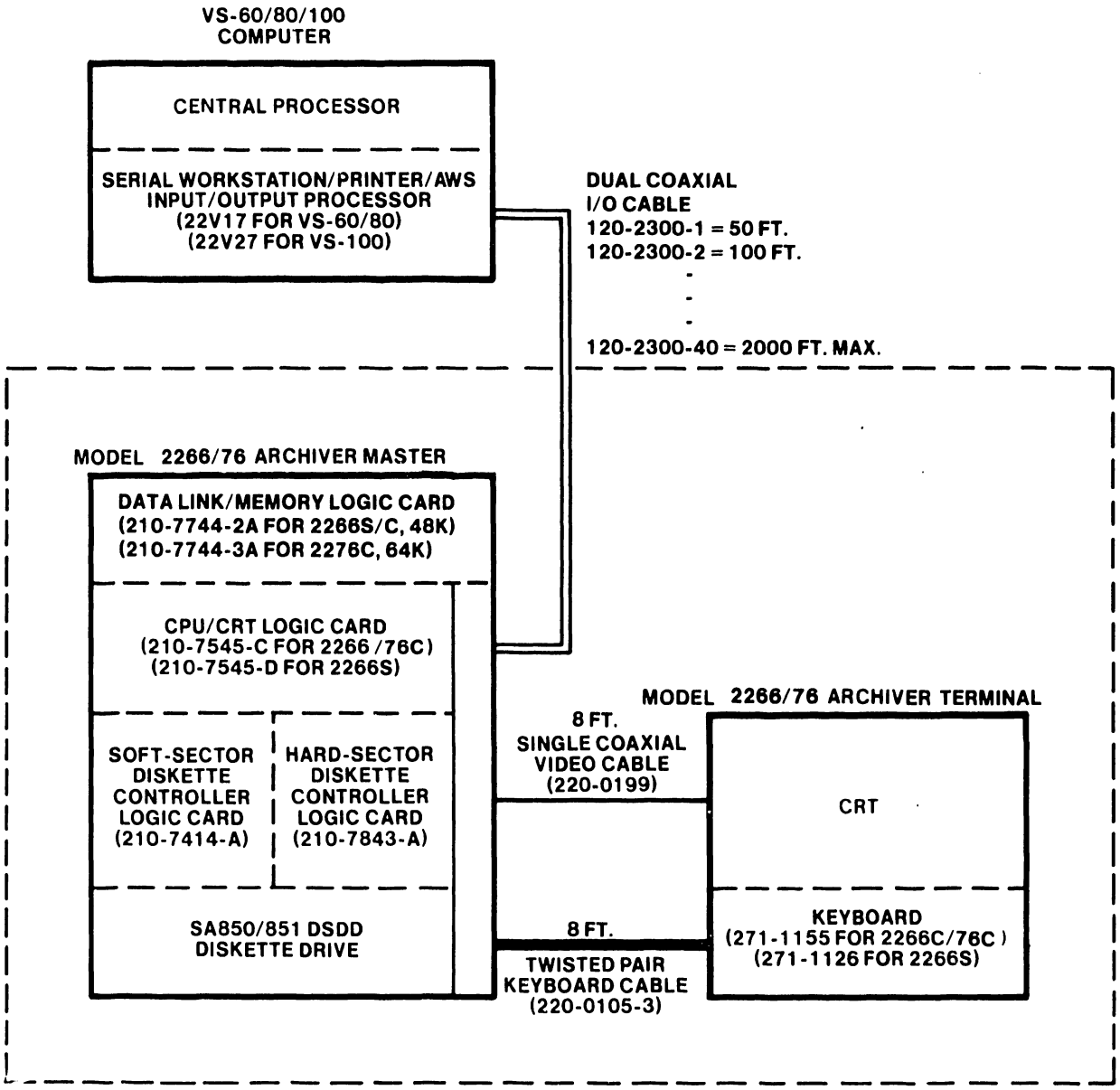
- z: Describes type of disk formatting capability: -1 = hard-sector only, -2 = soft-sector only, -3 = both.
- y: Describes type of functions supported: S = data processing only, C = combined data and word processing.
- x: Describes memory size: 6 = 48k, 7 = 64k.

Within the Archiving Master is the Model 2270V Double-Side, Double-Density (DSDD) Diskette Drive (Shugart 850/851) and the associated logic boards. The Archiving Master connects to the VS system mainframe CPU via an appropriate Input/Output Processor (IOP).

Table 1-3
VS AWS Model/Features/Composition Matrix

TYPE OF SYSTEM.....	COMBINED DP/WP		SERIAL DP ONLY			COMBINED DP/WP/OIS	
Model Number.....	2266C-1	2266C-3	2266S-1	2266S-2	2266S-3	2276C-1	2276C-3
WLI P/N, 60 Hertz.....	176-5180	176-5181	176-5182	176-5183	176-5184	176-5178	176-5179
WLI P/N, 50 Hertz.....	156-5180	156-5181	156-5182	156-5183	156-5184	156-5178	156-5179
Combined DP/WP Archiver Terminal WLI P/N 177-7051	X	X				X	X
2246C VS/WP Combo Keyboard WLI P/N 271-1155	X	X				X	X
Serial DP VS Archiver Terminal WLI P/N 177-7050			X	X	X		
8300 Serial Keyboard WLI P/N 271-1126			X	X	X		
Data Link/48K Memory Printed Circuit Assy. (PCA) WLI P/N 210-7744-2A	X	X	X	X	X		
Data Link/64K Memory (PCA) WLI P/N 210-7744-3A						X	X
Combined WS CRT/CPU PCA WLI P/N 210-7545-C (*)	X	X				X	X
Serial WS CRT/CPU PCA WLI P/N 210-7545-D (*)			X	X	X		
Hard-Sector Diskette I/O Controller PCA WLI P/N 210-7843-A	X	X	X		X	X	X
Soft-Sector Diskette I/O Controller PCA WLI P/N 210-7414-A		X		X	X		X
114 Power Supply Regulator PCA, WLI P/N 210-7316	X	X	X	X	X	X	X
1-MB DSDD Floppy Disk Drive, WLI P/N 278-4021	X	X	X	X	X	X	X

(*) -C and -D suffixes for the 210-7545 CRT/CPU PCA define the appropriate PROM loading on the assembly. -C PROMs contain microcode for combined DP/WP application; -D PROMs contain microcode for DP-only application.



MODEL 2266/76 VS ARCHIVING WORKSTATION

Figure 1-2 VS AWS Hardware Composition

1.6.2 CONFIGURATION IN WP/OIS SYSTEMS

Figure 1-3 is a block representation of the hardware components of the WP/OIS AWS.

The WP/OIS AWS is available in three configurations under model numbers AWS-1, AWS-4 and 5740. Two of the models, AWS-1 and AWS-4, are identical in all respects with the exception of the memory size on the 210-7744 Data Link/Memory Board; the AWS-1 comes equipped with 48k of memory while the AWS-4 comes equipped with 64k of memory. The 48k board (7744-2A) is the minimum requirement for WP functions while 64k (7744-3A) is required to support all OIS functions. The 5740 model is identical to the AWS-4 except it uses the ERGO 2 style 5730 Terminal instead of the 5506 Terminal used with AWS-1,4 models.

Included is an Archiving Master, and a Terminal externally identical to the 5536 or ERGO 2 series Terminals used in WP/OIS systems. The AWS supports the same functions as any other workstations in the system, with the addition of the archiving function. The actual model numbers of the Terminals supplied with the AWS-1,4 and 5740-4 are 5506 and 5730 respectively. The logic boards responsible for Terminal operation, as with the VS AWS, reside in the Archiving Master.

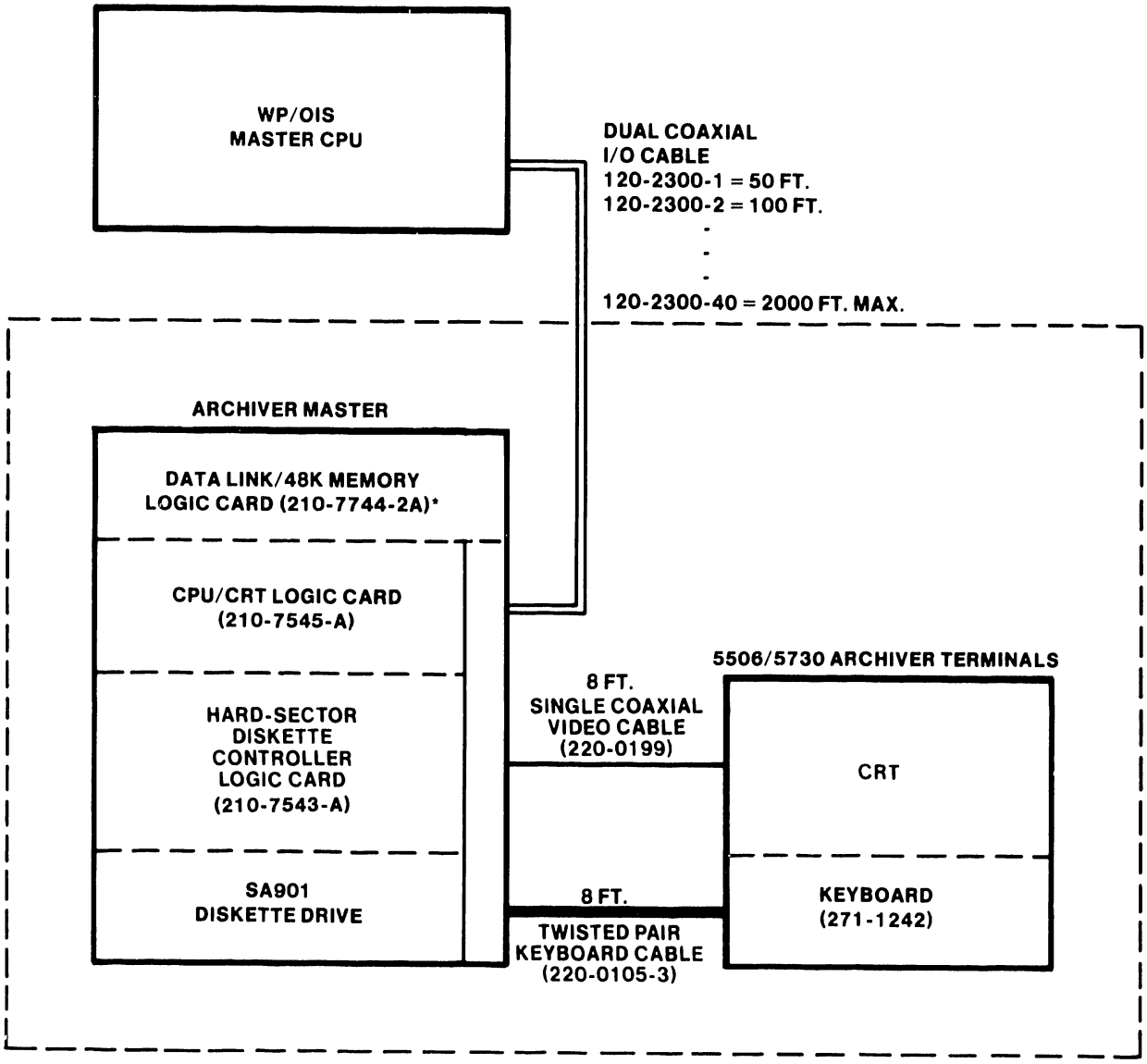
Also in the Archiving Master is the Shugart 901 Floppy Disk Drive providing hard-sector formatting of 8-inch floppy diskettes. The AWS-1, AWS-4 and 5740 are available only with hard-sector capability. The Archiving Master connects to an input/output port of the WP/OIS Master CPU.

1.7 HARDWARE GENERAL DESCRIPTION

1.7.1 TERMINAL (CRT/KEYBOARD UNIT)(Refer to Figure 1-4)

The Terminals used in the AWS contain a CRT display monitor and an attached keyboard (AWS-1,4) or detached keyboard (5740). No logic circuits reside in the unit. The Terminal plugs into any convenient 115V/60 Hz or 230V/50 Hz outlet through a built-in seven-foot power cord. The monitor power supply is switchable for either 115V/60 Hz or 230V/50 Hz input power. Connection to the Archiver Master unit is made through an eight-foot data cable and one coaxial video cable.

The Terminals use a 12-inch video Cathode Ray Tube (CRT) display with a 210-7456 Monitor Electronics board, common to many Wang workstations. The CRT screen has total display capacity of 1,920 characters arranged in 24 rows with 80 characters per row.



MODEL AWS-1 & AWS-4 WP/OIS ARCHIVING WORKSTATION

* A 48K MEMORY CARD (-2A) IS SUPPLIED IN MODEL AWS-1. A 64K MEMORY CARD (-3A) IS SUPPLIED IN MODEL AWS-4, AND IS REQUIRED FOR FULL SUPPORT OF OIS FUNCTIONS.

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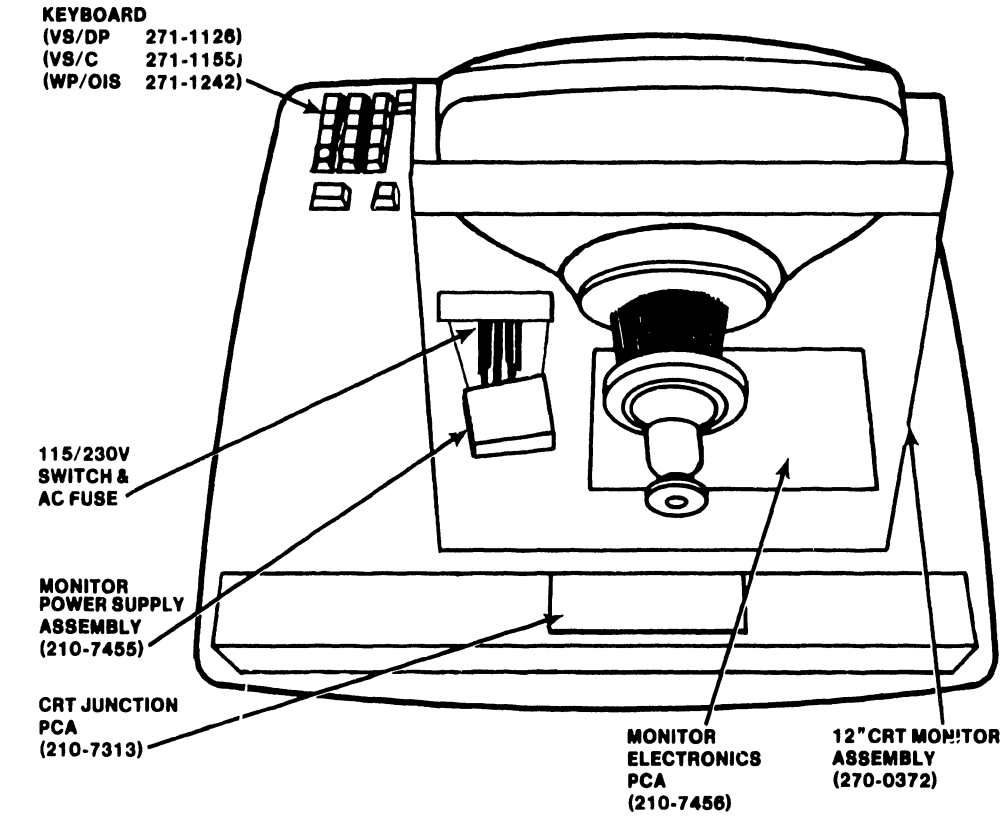
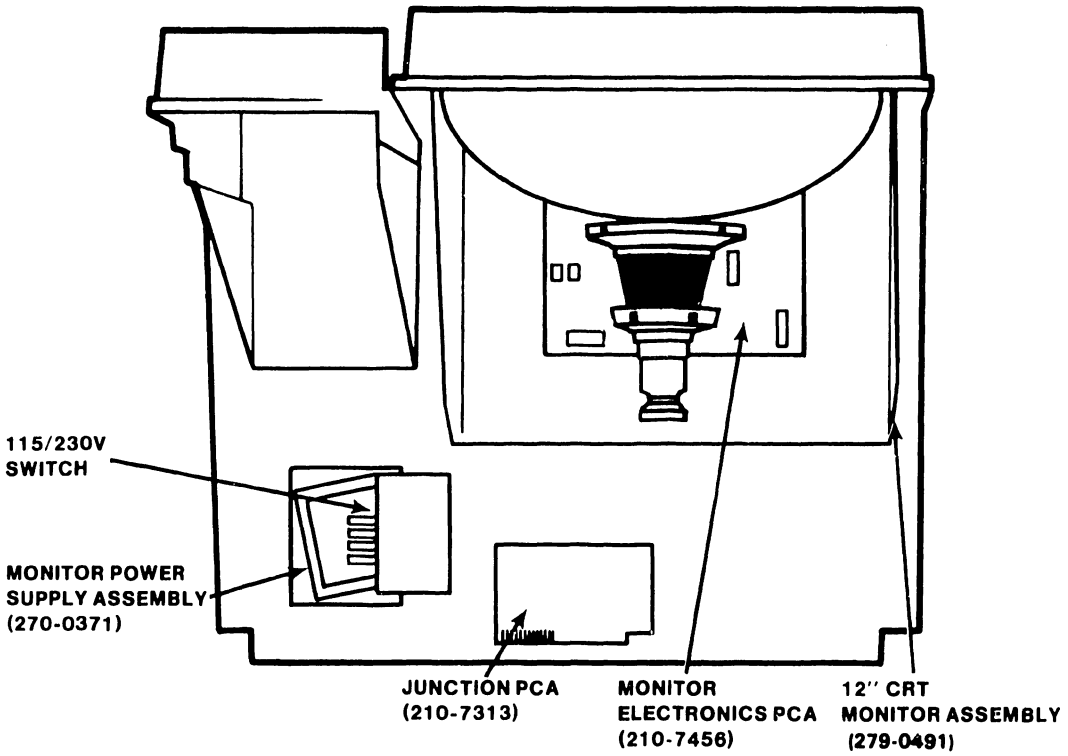
Figure 1-3 WP/OIS AWS Hardware Composition



5506 TERMINAL



5730 TERMINAL

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Figure 1-4 Archiver Terminals, Internal View

Keyboards used in the Terminal vary with the model and application. In VS models configured for DP-only use, the standard DP keyboard, 271-1126, is used.

VS models configured for combined DP/WP use the 271-1155 keyboard. The DP-only keyboard's special function keys (the 16 keys closest to the CRT) are marked with the PFnn designations used in the DP application, while the combined keyboard shows these designations on a marker strip which lays flat in front of the special function keys. The keys are marked, in this case, with the standard WP functions.

WP/OIS Terminals use a variety of keyboards depending on model and application. The 5506 terminal uses the standard 271-1242 WP keyboard or the optional 271-1243 Keyboard with numeric keypad. The 5730 terminal uses the standard 271-1242 WP keyboard or the following optional keyboards: 271-1243 keyboard with numeric keypad, 271-1245 expanded keyboard.

1.7.2 DISK DRIVE

The Disk Drive is mounted in the Archiver Master unit to the left of the card cage chassis (refer to Figure 1-5). In the VS AWS, this is a Shugart 850/851 Double Side, Double Density (DSDD) unit, supporting both hard and soft-sector diskette formatting. Refer to the table of related publications for VS systems (Table 1-1) for more information on this unit.

In the WP/OIS AWS this unit is a Shugart 901, supporting hard-sector formatting only. Refer to the table of related publications for WP/OIS systems (Table 1-2) for more information on this unit.

1.7.3 ARCHIVER MASTER UNIT

The Archiver Master unit for both VS and WP/OIS systems contains the same chassis and power supply, with minor differences in PCA loading. The primary difference between the VS and the WP/OIS Archiver Master unit is the Disk Drive (refer to section 1.6.2). The following subsections briefly describe the major PCAs found in this unit. Figure 1-5 is an internal view of the Archiver Master unit.

1.7.3.1 Archiving Master Unit Motherboard

The Archiving Master unit uses a Motherboard to provide the passive hardware connections between the major PCAs of the system. In the VS AWS, this is a 210-7615 Motherboard, distinguished from the WP/OIS Motherboard (210-7546) by the additional circuit runs and socket required to support the Soft-Sector Controller PCA. Thus, the WP/OIS Motherboard cannot be used in a VS system.

1.7.3.2 Power Supply Regulator

The Power Supply Regulator board in the Archiver Master unit is a 210-7316, which is similar to the 210-7156 board used in many Wang workstations. The board supplies +24, ±12 and ±5 volt dc outputs to power the boards in the Archiver Master unit.

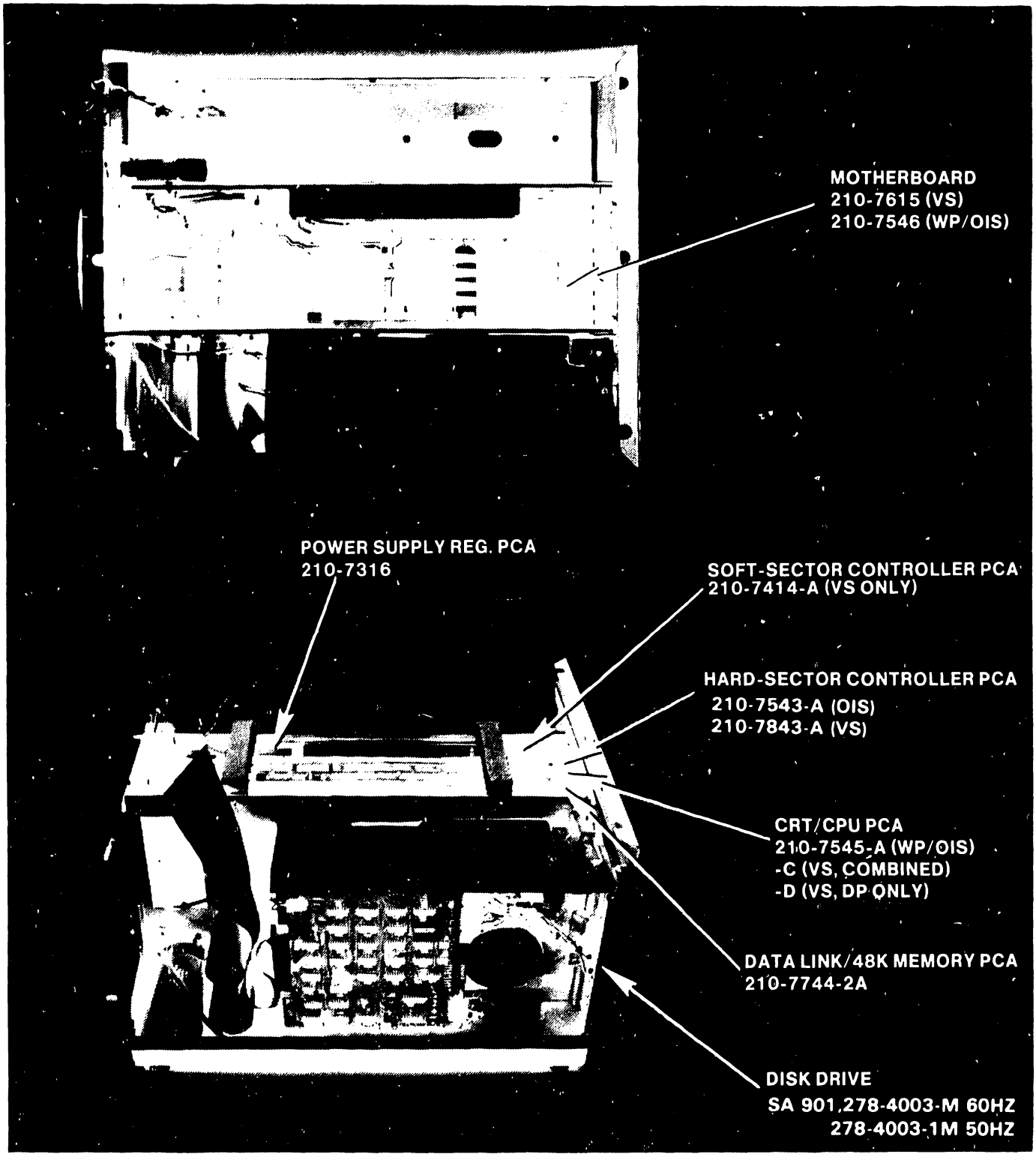


Figure 1-5 Archiver Master Unit, Internal View

1.7.3.3 Data Link/48K Memory Board

The Data Link/48K Memory Board used in the VS and WP/OIS AWS is the 210-7744-2A board. This board contains logic circuitry identical to the 7544 board found in many Wang workstations, and differs from that board only in its PROM loading. The 210-7744-2A board contains a special bootstrap loader PROM (location L120, WLI P/N 378-4302) used exclusively in the VS AWS system. (This special VS function is described in detail in Appendix B of this manual. The bootstrap PROM is not present in the WP/OIS AWS and L120 is normally vacant.)

The -2A suffix of the board's part number indicates its memory size, in this case, 48k. This is the minimum requirement for VS and WP Archiving Workstations. For full support of OIS functions, 64k of memory is required on this board, indicated by a part number suffix of -3A.

The data-link circuit on this board is the main link for data transfer between the Archiving Master unit and the mainframe CPU associated with the host system.

1.7.3.4 CRT/CPU Logic Board

The CRT/CPU board contains the video display logic, CRT memory, keyboard interface logic and the Z-80 CPU. The AWS uses the 210-7545 board used in many Wang workstations. It contains identical circuitry for both the VS and WP/OIS AWS, with the exception of the PROM loading on the board. PROM loading is defined by the letter suffix of the part number. The table below cross-references the three different PROM loadings used, their associated letter suffixes, PROM locations, part numbers and model usage.

CRT/CPU Board PROM Loading

AWS Model	CRT/CPU P/N & Suffix	PROM Location	PROM P/N	PROM Description
WP/OIS	7545-A	L51	378-2216	114 CRT CHARACTER
		L52	Vacant	
VS DP Only	7545-D	L51	378-2030-R1	STANDCRT L8
		L52	Vacant	
VS DP/WP Combined	7545-C	L51	378-2216	114 CRT CHARACTER
		L52	378-2030-R1	STANDCRT L8

1.7.3.5 Hard-Sector Diskette Controller Boards

These boards (210-7543-A for OIS and 210-7843-A for VS) are used in conjunction with the Shugart 901 (OIS) or 850/851 (VS) Disk Drives. They are designed to function with the Z-80 CPU as its host and, together with the Disk Drive, it provides standard Wang format, hard-sector capability in the VS and WP/OIS AWS. The -A suffix of the board part number indicates that it is not equipped with the telecommunications (TC) option. Archiving workstations equipped with the TC option come with the 210-7843-1A version of this board.

The Hard-Sector Diskette Controller Board can operate by itself (hard-sector formatting only) or with the Soft-Sector Floppy Diskette Controller Board, as in the VS AWS.

1.7.3.6 Soft-Sector Diskette Controller Board

This board (210-7414-A) is used in conjunction with the Shugart 850/851 Disk Drive in the VS AWS only. It is designed to function with the Z-80 CPU as its host and, together with the Disk Drive, it provides soft-sector capability in the VS AWS. The soft-sector formatting of diskettes duplicates certain IBM diskette formats, thus allowing the VS system to accept and create diskettes compatible with a variety of IBM formatting techniques as detailed in Table 1-6.

The Soft-Sector Diskette Controller Board can operate by itself (soft-sector formatting only) or with the Wang-format, Hard-Sector Floppy Diskette Controller.

1.8 SPECIFICATIONS

Specifications for the Archiving Master and the Terminal are given in Table 1-6 for the VS AWS and in Table 1-5 for the WP/OIS AWS. Table 1-8 contains specifications for diskette formatting techniques supported by the Shugart 850/851 Disk Drive in the VS AWS. Figure 1-6 is a representation of standard Wang diskette media and associated specifications.

1.9 OPTIONS

The WP/OIS AWS is available with telecommunications (TC) as an option. The TC option is designated by "TC" after the standard model number, and these units are equipped with a 210-7543-1A Hard Sector Disk Controller PCA, which contains the TC circuitry.

TC is not supported on the VS AWS.

A Keyboard with a numeric keypad is available as an option on the WP/OIS AWS Terminal. Part number for the optional Keyboard is 271-1243.

Table 1-4
VS AWS Specifications

Parameter	Archiving Master	Terminal
Net Weight:	65 lb. (29.3 kg)	37.5 lb. (16.9 kg)
Physical Dimensions: Height Width Depth	 13.3 in. (33.7 cm) 16.5 in. (41.9 cm) 22.0 in. (55.9 cm)	 13.5 in. (34.3 cm) 19.8 in. (50.3 cm) 20.5 in. (52.0 cm)
Power Requirements:	115 Vac/60 Hz (±10%) 230 Vac/50 Hz (±10%) 250 Watts	115 Vac/60 Hz (±10%) 230 Vac/50 Hz (±10%) 72 Watts
Fuses:	2.0 Amps/115 Vac 1.0 Amps/230 Vac	0.6 Amps/115 Vac 0.3 Amps/230 Vac
Heat Output:	710 BTU/Hour (177.5 kCal/Hour)	102 BTU/Hour (25.5 kCal/Hour)
Ambient Temperature:	60° to 80° F (15° to 27° C)	60° to 80° F (15° to 27° C)
Ambient Relative Humidity:	35 to 65% Non-Condensing	35 to 65% Non-Condensing
Cable Lengths: Power (from unit to ac power) I/O (to/from Master CPU)	 6.0 ft. (1.8 m) 2000 ft., max. (609.6 m)	 7.0 ft (2.1 m) Not Applicable
Video (between units) Keyboard (between units)	8.0 ft. (2.5 m) 8.0 ft. (2.5 m)	

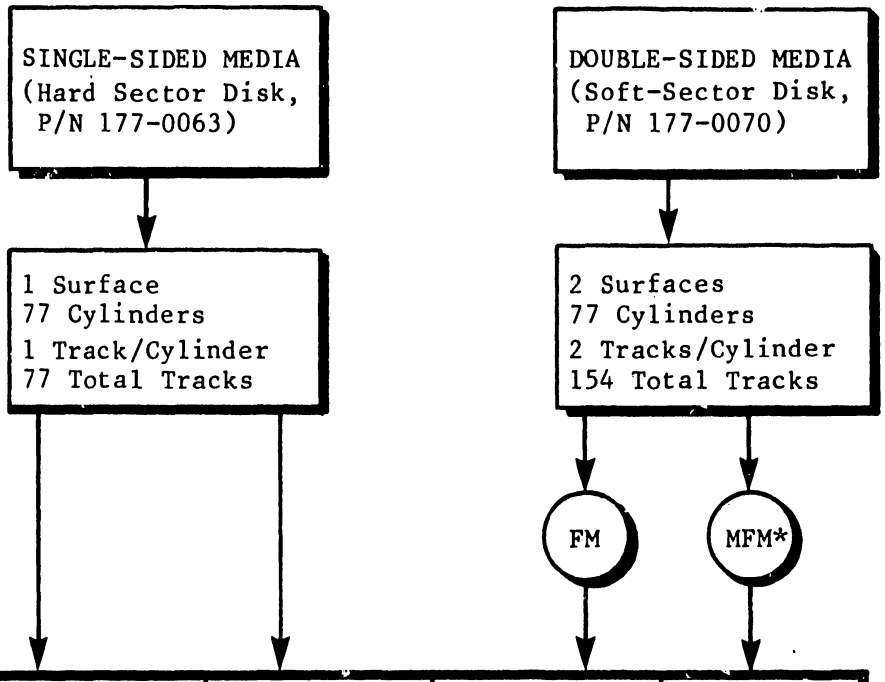
Table 1-5
WP/OIS AWS Specifications

Parameter	Archiving Master	Terminal 5506	Terminal 5730
Net Weight:	20 lb. (9.1 kg)	54 lb. (24.5 kg)	64 lb. (29.1 Kg)
Physical Dimensions:			
Height	13.3 in. (33.7 cm)	13.5 in. (34.3 cm)	15.9 in. (40.4 cm)
Width	16.5 in. (41.9 cm)	19.8 in. (50.3 cm)	20.0 in. (50.8 cm)
Depth	22.0 in. (55.9 cm)	20.5 in. (52.0 cm)	16.4 in. (41.6 cm)
Power Requirements:	115 Vac/60 Hz (±10%) 230 Vac/50 Hz (±10%) 250 Watts	115 Vac/60 Hz (±10%) 230 Vac/50 Hz (±10%) 50 Watts	
Fuses:	3.0 Amps/115 Vac 1.5 Amps/230 Vac	0.6 Amps/115 Vac 0.3 Amps/230 Vac	
Heat Output:	710 BTU/Hour (177.5 kCal/Hour)	102 BTU/Hour (25.5 kCal/Hour)	
Ambient Temperature:	60° to 80° F (15° to 27° C)	60° to 80° F (15° to 27° C)	
Ambient Relative Humidity:	35 to 65% Non-Condensing	35 to 65% Non-Condensing	
Cable Lengths:			
Power (from unit to ac power)	6.0 ft. (1.8 m)	7.0 ft (2.1 m)	
I/O (to/from Master CPU)	2000 ft., max. (609.6 m)	Not Applicable	
Video (between units)	8.0 ft. (2.5 m)		
Keyboard (between units)	8.0 ft. (2.5 m)		

Table 1-8 VS Archiver Compatibility Data (Using DISKINIT, DMS or IBMCOPY)

MODE	FORMAT	WANG/IBM DISKETTE	DATA TRACKS	SECTORS/ TRACKS	BYTES/ SECTOR	TOTAL CAPACITY	VS-ARCHIVER SUPPORTED	COMMENTS
1. Hard Sector (Wang White Label) Single Side/ Single Density	Wang Std.	177-0063	77	16	256	315,392	Yes	Use For: WP Archiving on VS; DP Backup on VS Compatible with: MVP (2270/2270A), VP (2270/2270A)
2. Soft Sector Single Side/ Single Density (IBM Diskette 1) (Wang Green Label)	1. IBM BASIC DE	230-5830 or (177-0074)	73	26	128	242,944	Yes	Used By: IBM 5114, 3741, 32, 34, 38, 4300,8100 (Use IBM Copy Utility) *Wang MVP, VP, LVP, SVP (Use IBM Copy Utility)
	2. IBM GENERAL DE	230-5830	74	26	128	246,272	No	Used By: IBM 5114, 3741, 32, 34, 38, 4300, 8100
		230-5845	74	15	256	284,160	No	Used By: IBM 5114, 38, 8100
		166-9954	74	8	512	303,104	No	Used By: IBM 5114, 32, 34, 38
	3. _____							
	4. _____							
	5. Wang Non-Std.	177-0074	77	26	128	256,256	No	
			77	15	256	295,680	No	
			77	8	512	315,392	No	
			77	4	1024	315,392	No	
3. Soft Sector Single Side/ Double Density (When using this format, a diskette certified for single sided/double density operation is required.)	1. _____							
	2. _____							
	3. Wang Native SL		77	8	1024	630,784	Yes	Used For: DP Backup on VS (Contains VTOC; 2kb blocks); supported by Diskinit and DMS
	4. Wang Native NL		77	8	1024	630,784	Yes	Supported by Diskinit and DMS;(No VTOC; 2kb blocks);
	5. Wang Non-Std.		77	26	256	512,512	No	
			77	15	512	591,360	No	
			77	8	1024	630,784	No	
			77	4	2048	630,784	No	
4. Soft Sector Double Side/ Single Density (IBM Diskette 2) (Wang Red Label)	1. IBM BASIC DE	176-6870	74(x2)	26	128	492,544	Yes	Used By: IBM 38
	2. IBM GENERAL DE	176-6870	74(x2)	26	128	492,544	No	Used By: IBM 5114, 38
			74(x2)	15	256	568,320	No	Used By: IBM 5114, 38
	3. _____							
	4. _____							
	5. Wang Non-Std.	177-0070	77(x2)	26	128	512,512	No	
		177-0070	77(x2)	15	256	591,360	No	
		177-0070	77(x2)	8	512	630,784	No	
		177-0070	77(x2)	4	1024	630,784	No	
5. Soft Sector Double Side/ Double Density (IBM Diskette 2D) (Wang Red Label)	1. IBM Type 'H'DE	176-6872 or (177-0070)	74(x2)	26	256	985,088	Yes	Used By: IBM 38, 8100 (Use IBM Copy Utility) : Wang LVP, SVP(Capacity for LVP/SVP=(74+75) x26x256=991,744); (use 2200 Copy Utility)
	2. IBM GENERAL DE	176-6872	74(x2)	26	256	985,088	No	Used By: IBM 5114, 34, 38
		166-9044	74(x2)	15	512	1,136,640	No	Used By: IBM 5114, 38
		166-9045	74(x2)	8	1024	1,212,416	No	Used By: IBM 5114, 34, 38
	3. Wang Native SL	177-0070	77(x2)	8	1024	1,261,568	Yes	Used For: DP Backup on VS (contains VTOC; 2kb blocks; Supported by Diskinit and DMS
	4. Wang Native NL	177-0070	77(x2)	8	1024	1,261,568	Yes	Supported by Diskinit and DMS;(No VTOC; 2kb blocks)
	5. Wang Non-Std.	177-0070	77(x2)	26	256	1,025,024	No	
			77(x2)	15	512	1,182,720	No	
			77(x2)	8	1024	1,261,568	No	
			77(x2)	4	2048	1,261,568	No	

*Wang 2200 Series normally uses this format only when providing IBM 3741 compatibility



System: / Parameter	WP/OIS AWS	VS AWS	VS AWS	VS AWS
Disk Drive:	SA-901	SA-851	SA-851	SA-851
Density:	Single	Single	Single	Double
Sectors/Track:	16	16	4	8
Bytes/Sector:	256	256	1024*	1024*
Total Sectors:	1232	1232	616	1232
Total Bytes:	315,392	315,392	630,784	1.25M
Total 2k Blocks:		154	308	616
End Block No.:		153 (dec.)	307 (dec.)	615 (dec.)
Logical (SYS):		99 (hex)	133 (hex)	267 (hex)
Normal (IOCW):		4C8 (hex)	998 (hex)	1338 (hex)

*Default: When soft-sector media is used, MFM is the default mode. The default bytes/sector value is 1024 for MFM or FM. See Table 1-8 for other sector sizes available via the IBMCOPY utility.

Figure 1-6 Diskette Specifications

CHAPTER 2

THEORY OF OPERATION

TABLE OF CONTENTS

CHAPTER 2 THEORY OF OPERATION **Page**

LIST OF ILLUSTRATIONS

Figure **Title** **Page**

CHAPTER 2

THEORY OF OPERATION

2.1 INTRODUCTION

This section of the manual provides theory of operation descriptions for each functional unit in the Archiving Workstation (AWS). In most cases, each description is accompanied by a block diagram of the unit. Each subassembly is identified by its common name and part number. Refer to section 1.5.1 and 1.5.2 of this manual to determine the actual subassemblies used in a particular model AWS.

The chapter is divided into two main subsections reflecting the organization of AWS functions. The two main subsections are, workstation functions and archiving functions. The contents of this chapter are arranged as shown below.

Section 2.2	Workstation Functions
Section 2.3	Archiving Functions

2.2 WORKSTATION FUNCTIONS

2.2.1 HARDWARE ORGANIZATION

Workstation functions are carried out by the CRT/Terminal in conjunction with two boards in the Archiving Master. The CRT/Terminal contains the 12-inch monitor, a keyboard and a power supply, while the Archiving Master houses the CRT/CPU Board and the Data Link/48K Memory Board. Operation of the two logic boards in the Archiving Master is supported by the power supply and the Motherboard contained in that unit. Refer to section 2.3.1 for hardware descriptions of the power supply and Motherboard.

2.2.2 FUNCTIONAL OVERVIEW

Workstation logic resides on two circuit boards, PCA 210-7545 (CRT/CPU) and PCA 210-7744 (Data Link/Memory). The major logic functions are:

210-7545 PCA	210-7744-2A PCA
a. Instruction/Bus control (CPU)	a. Main Memory
b. Video Display Logic	b. Data Link
c. CRT Memory	
d. Keyboard Logic	

These functions are interconnected by the System Address Bus and the System Data Bus.

2.2.3 BASIC WORKSTATION FUNCTIONS (Refer to Figure 2-1)

2.2.3.1 Z-80 Central Processor Unit (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from Main Memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

2.2.3.2 Bootstrap PROM (VS Only)

A bootstrap PROM, located on the 7744 Data Link/Memory Board in the VS AWS only, contains special instructions which enable the AWS to read diskettes for troubleshooting purposes.

2.2.3.3 Parity Generation and Test

The Parity Generator/Tester checks the accuracy of all data received by the CPU before it enters the processor. Parity errors are communicated to the user through CRT display messages.

2.2.3.4 IN-OUT Decoders

Memory instructions IN and OUT instruct the CPU to transfer data into or out of an I/O device rather than memory. The IN-OUT decoder identifies the selected I/O device.

2.2.3.5 Keyboard Interface Logic

During an appropriate IN instruction the Keyboard Interface places a character code onto the Data Bus. The CPU examines the character and stores it in the CRT memory buffer to be placed on the CRT display.

2.2.3.6 Video Display Logic

Video Display Logic continuously reads characters from CRT memory, converts them into an appropriate stream of video dots, and arranges these dots on the CRT display. Video Display Logic also reads a Control Memory. This Control Memory indicates the display status of each character: normal, intensified, underlined, etc.

2.2.3.7 Data Link

The Data Link permits workstation memory to be loaded or read by the master. The master can write new memory instructions into workstation memory;

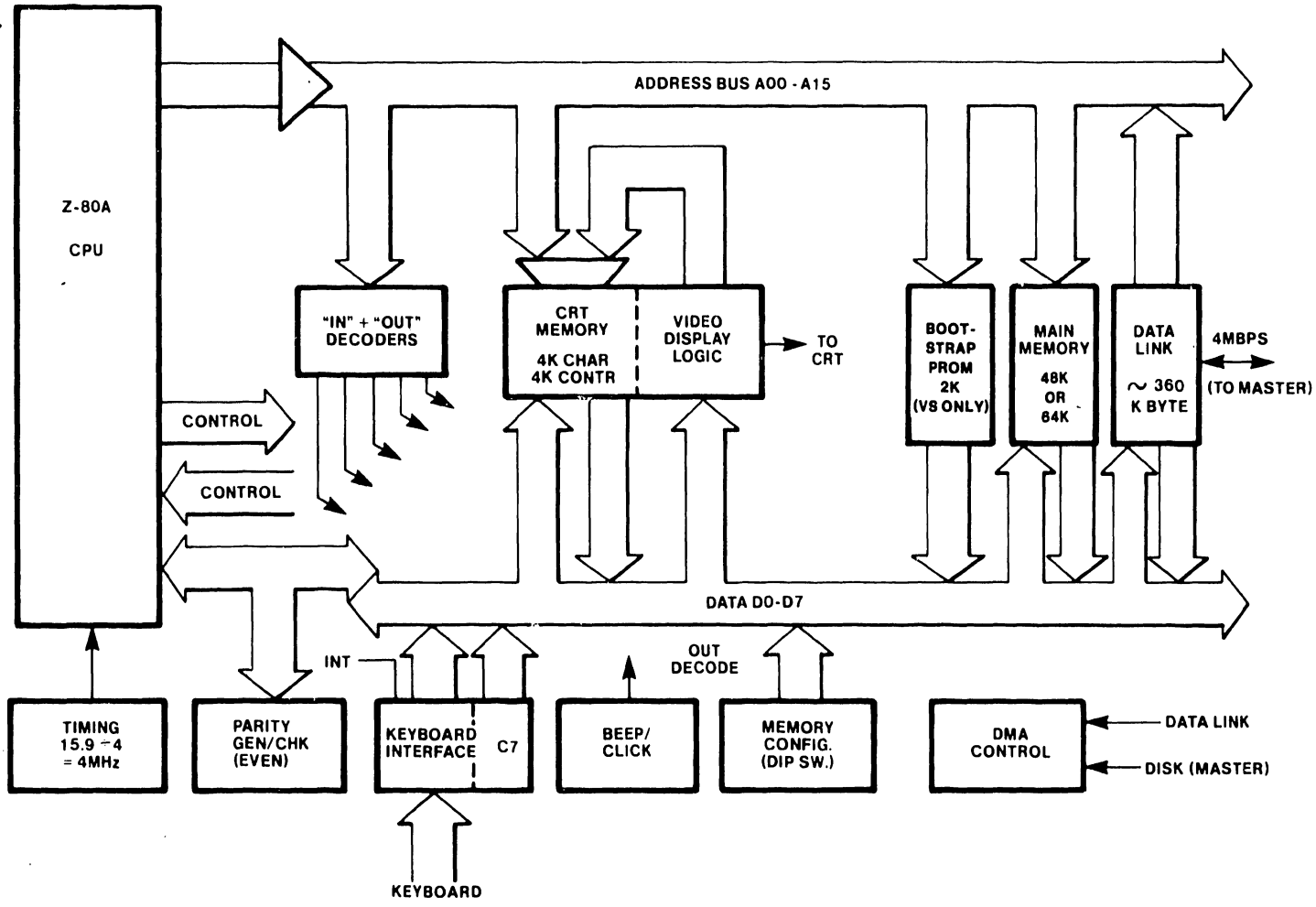


Figure 2-1 Workstation Functions Block Diagram

it can also record (archive) information entered by the workstation onto a common disk. The workstation CPU is disabled when the master uses the Data Link. During this time Direct Memory Access (DMA) logic, rather than the CPU, synchronizes memory read/write operations. DMA logic does not support CRT memory transfers.

2.2.4 210-7545 CRT/CPU PCA

The 7545 PCA contains Video Display Logic, CRT Memory, Keyboard Interface, Z-80A CPU, and these related logic functions:

a. IN-OUT decoders
b. Parity generation and check (even parity)
c. Memory Configuration (dip switches)
d. Audio prompt (beep/click)

2.2.4.1 Video Display and Control Logic

Refer to Figure 2-2 (Video Display and Control Logic Block Diagram).

The AWS displays 1920 character locations arranged in 24 rows of 80 characters or columns. Each character on the screen has a unique memory-address containing the code of the character being displayed. The number of characters per row may be extended to 158 to accommodate the extended columns used by wide-platen printers and line printers. These additional 1872 character spaces (total 3792) are also accommodated in CRT memory, however, only 80 columns can be displayed at one time. The additional row length can only be observed by performing a horizontal scroll (Optional-WP, Standard-OIS).

An additional four-bit control field is associated with each CRT address. This control field permits each character to be blinked, intensified, underlined, and/or accompanied by a cursor. Separate parity bits accompany each character and each control field to ensure data integrity.

Memory locations are sequentially displayed by addressing memory with "column" (character) and "row" (line) counters. Extended rows are accommodated by indexing the column counter with an offset value supplied by the CPU.

The display initially presents all 80 characters in the top row. When the last character has been displayed, the row count is incremented and the next row of 80 consecutive locations is displayed. When the last character of the last row is reached, the cycle is repeated. Sixty screen displays occur per second.

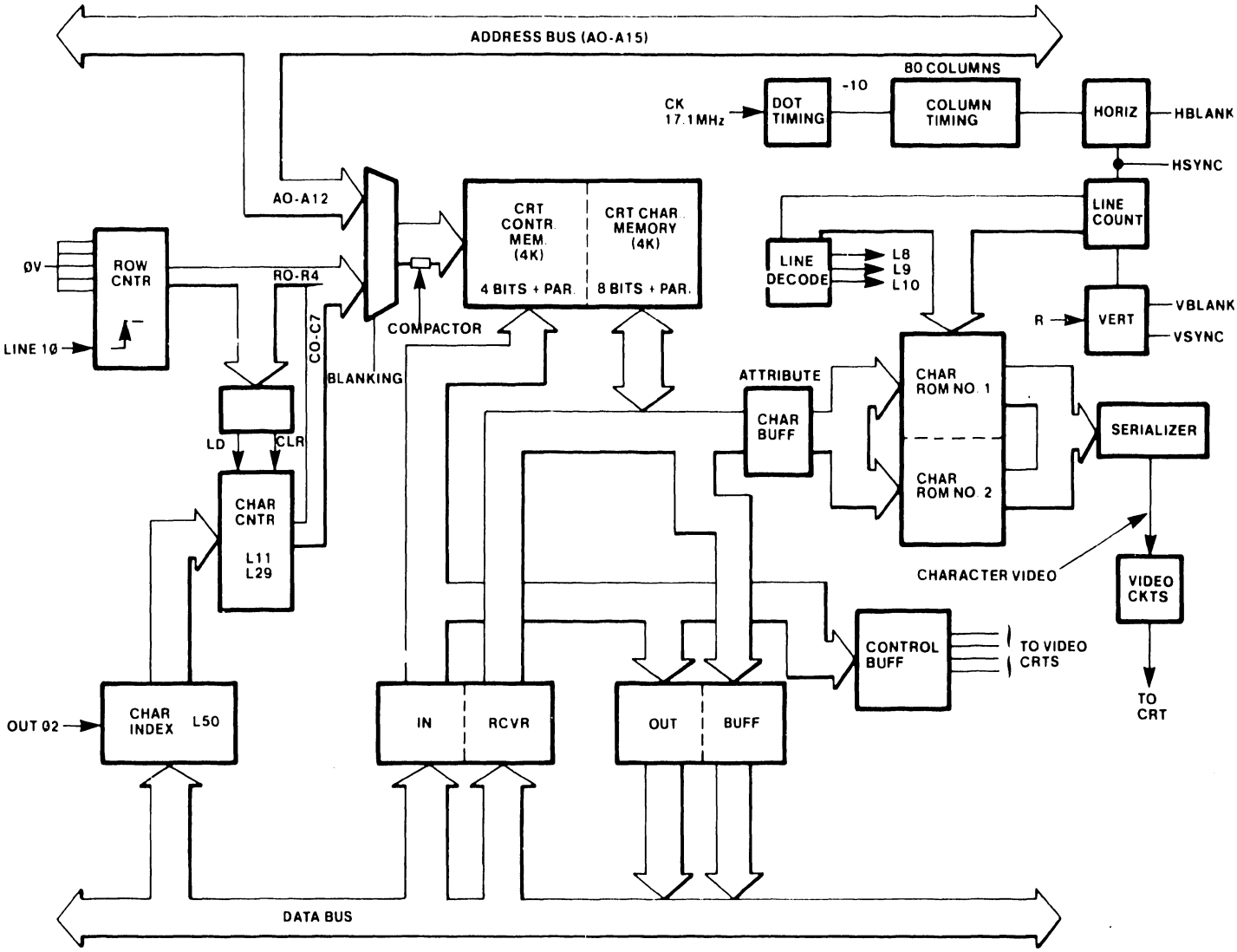


Figure 2-2 Video Display and Control Block Diagram

2.2.4.2 Dot Matrix Display

Refer to Figure 2-3. The workstation CRT displays and emphasizes characters using a raster scan display. The display is partitioned into a series of 10 x 11 dot matrices. Alphanumeric and special characters are created by illuminating a specific pattern of dots within the matrix associated with each character position. Specific characters are displayed in an 8x8 portion of the matrix; cursor and underlines are displayed in the lower 10x2 portion of the matrix.

Most character information is contained in the first seven lines of the matrix. The eighth line provides room for descenders, such as the tail of a comma or the bottom portion of the letter "g." The ninth line, line #8, may contain half of a blinking cursor. The tenth line, line #9, may contain an underline or the bottom half of the cursor. The eleventh line, line #10, provides vertical spacing.

A horizontal group of matrices form a character row. Information within a matrix is displayed by illuminating an appropriate selection of dots for each character in a row during eight successive scan lines.

2.2.4.3 Character Generation

Refer to Figure 2-2. Video display logic continuously reads characters from CRT memory. Either of two Character ROMs forms each character. Each ROM converts character codes into illuminated-dot sequences that form selected character shapes on the display during each scan line. ROM output is serialized and supplied to the video output circuit. Video display logic also reads a special Control Memory that determines the display status of each character (normal, intensified, underlined, etc.).

2.2.4.4 Video Control Logic

Video control logic produces a four-level analog signal for CRT electronics. The four levels provide:

a. normal display/intensified display
b. blanked display/sync pulses (intensified blanking)

The analog signal is digitally generated and controlled. It causes characters to be displayed at normal intensity, high intensity, underlined, and blinking. It also displays an intensified and blinking, double-lined cursor, and manages CRT blanking.

Information is blanked during vertical and horizontal retrace, each time CRT memory is updated or read by the CPU, and between characters (while the character-video shift register is being loaded).

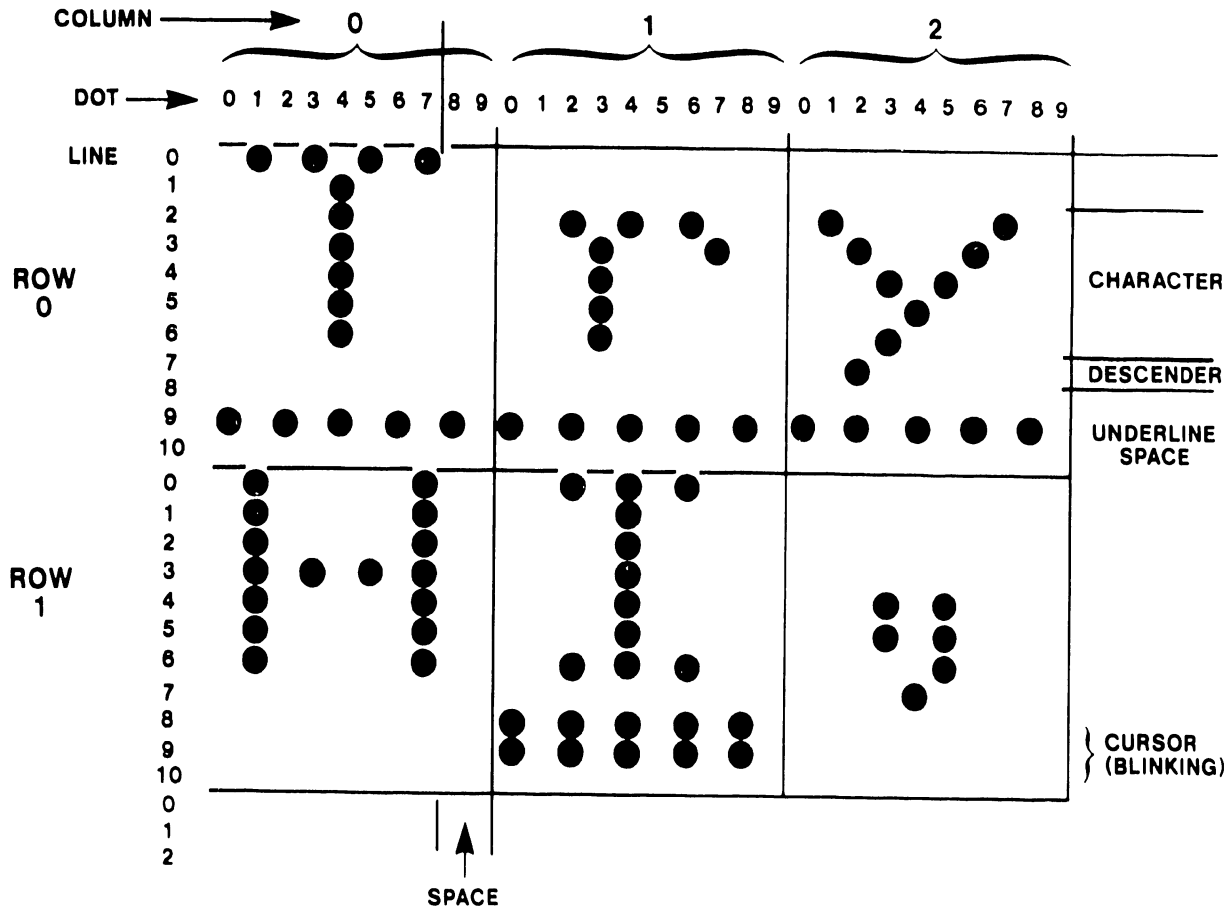


Figure 2-3 Dot Matrix Display

2.2.4.5 CRT Memory Input/Output Control

The Z-80A CPU employs the same control signals to read information from the CRT memory buffer and to read main memory. Mapping the CRT memory buffer into the top 16K of the memory-addressing range speeds the frequent CRT display updates required for word processing. (This upper addressing range may be reassigned by software to serve as program memory.)

Unlike main memory, neither the Data Link nor the Disk can employ DMA to read CRT memory. This is a consequence of the Row/Column addressing scheme used by CRT memory.

The Control Input and Output Buffers are disabled and the character-output buffer cleared both during a Power-Up Reset and when bad parity is found. Either condition freezes the CRT display and forces zeros onto the Data Bus.

Data is clocked into the character buffer at the end of a CRT character time while CRT memory is being addressed from the bus. The bus does not address CRT memory unless a high address is received with a Memory Request asserted; Workstation DMA devices do not use Memory Request and cannot write into CRT memory.

2.2.4.6 Keyboard Interface (Figure 2-4)

The keyboard interface accepts characters from the keyboard and generates a processor interrupt, enabling data to be transferred by the CPU to CRT memory and thus to the Display. During each transfer, Keyboard Interface logic supplies the keyboard with a signal to inhibit additional transfers until the current character has been accepted by the processor. The Z-80A CPU responds to keyboard interrupts by issuing a command which forces a hard-wired signal, C7, onto the data bus. The CPU interprets C7 as a RESTART command.

The keyboard interface also performs these functions:

a. Keystroke debounce
b. Repeat keys

2.2.4.7 Keystroke Processing

There are two types of keystroke operations: single key and repeat key. Single keystroke processing requires the keyboard interface to:

a. Recognize the keystroke
b. Inhibit the generation of additional keystrokes
c. Inhibit the recognition of additional keystrokes
d. Provide time (10ms) for keystroke debounce
e. Generate an interrupt request
f. Clear interrupt and character/keystroke inhibits as soon as the CPU reads the character.

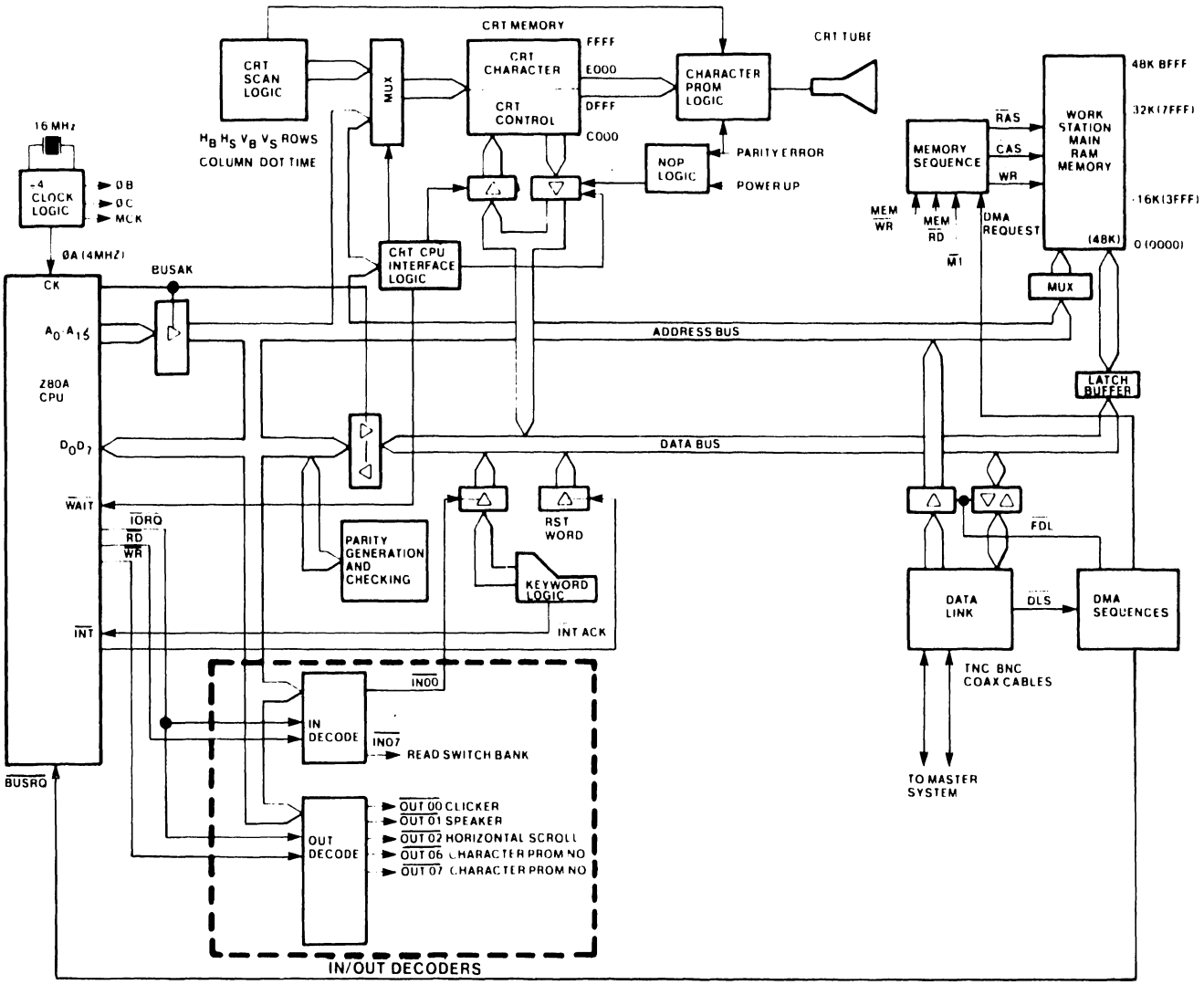


Figure 2-4 Keyboard Interface

Repeat keystroke processing requires these additional Interface functions:

a. Initiate a quarter-second delay to recognize a request for repeat
b. Recognize repeat keys
c. Generate repetitive interrupts every 60 ms for repeat keys other than cursor east/west keys
d. Shorten the repeat delay to 30 ms during horizontal cursor movement (The cursor crosses more character spaces when moving horizontally than when moving the same distance vertically.)
e. Permit any key to be repeated when the desired key is pressed nearly simultaneously with any repeat key

2.2.4.8 IN-OUT Decoders (Figure 2-5)

Certain memory instructions direct the CPU to transfer data either into or out of an I/O device rather than Workstation memory. These instructions are designated IN and OUT, followed by two-digit hex identifiers. When the CPU receives an IN or OUT instruction, the IN-OUT decoders identify the device. For example, a signal from the IN decoder (during an appropriate IN instruction) causes the Keyboard Interface to place a character code onto the data bus. The instruction sequence causes the CPU to examine the character and store it in the CRT memory buffer, to be displayed on the CRT display.

The IN-OUT decoders also control the Workstation audio prompt (beep/click) feature, and optional horizontal scroll requests.

2.2.4.9 Parity Generation and Check

Memory Parity logic is one of two parity generation/detection circuits. The other circuit is integral to the Data Link. Memory Parity logic generates and then tests for even parity on all data transfers leaving or entering the CPU through the data bus.

During a CPU write, each parity bit is calculated and stored in Main Memory, CRT character Memory, or CRT Control Memory, depending upon which memory is enabled.

The parity line is checked on each CPU read. If a Memory Parity Error is detected, the error is noted in the the CPU status register. Such an error is also indicated in this register during a CRT control memory write. The Data Link also tests memory parity before generating its own line parity during a Master Read command.

A detected memory parity error immediately freezes the CRT display and generates all zeroes on the data bus. This is done by disabling the CRT memory receivers and clearing the character-output buffers. An all-zero data bus is interpreted by the CPU as a string of continuous NOP instructions. The NOPs disable the CPU while maintaining the necessary Memory Refresh cycles.

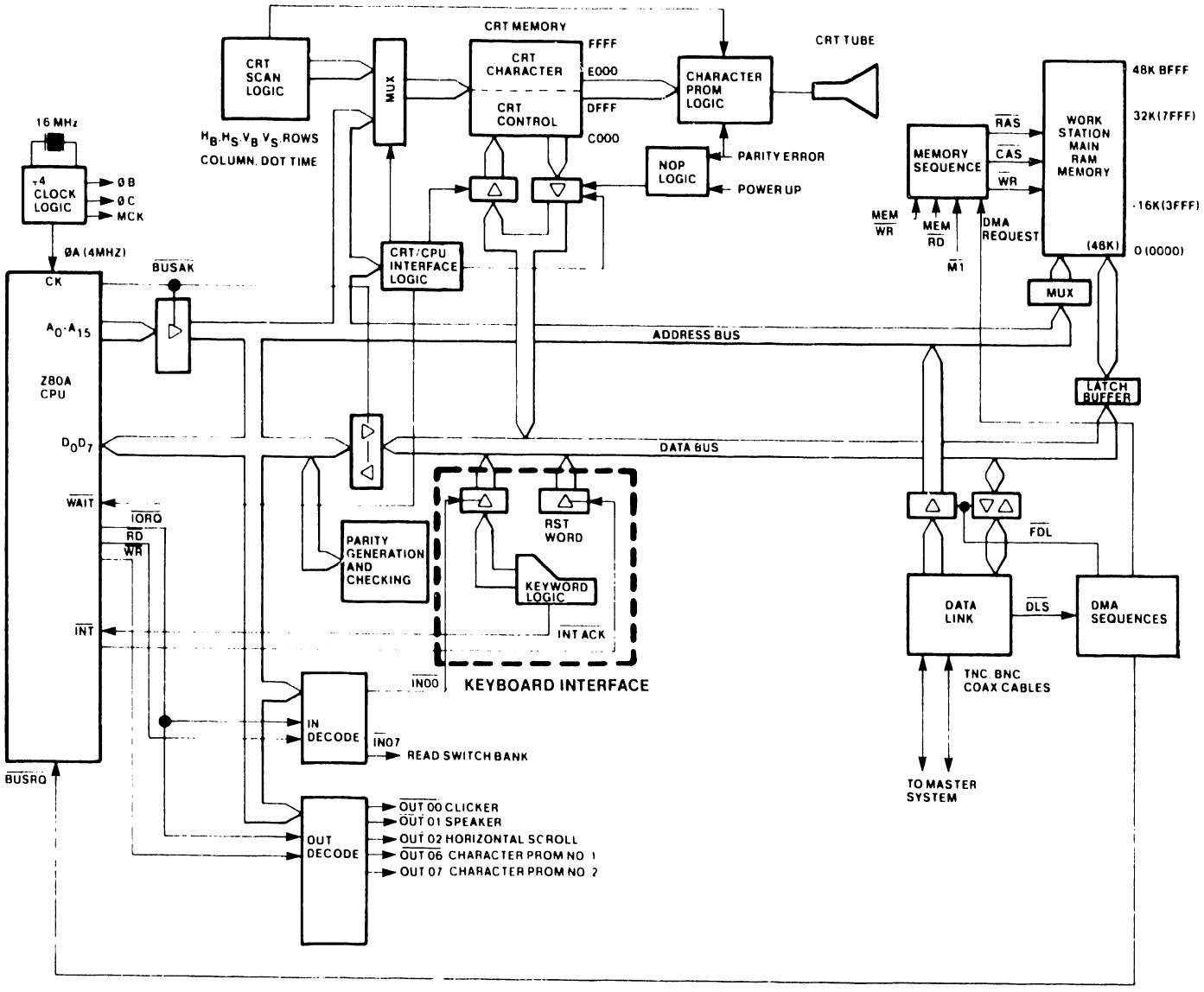


Figure 2-5 I/O Decoding

The CPU can escape from the disabling NOPs only through a Z-80A RESET. Reset can be accomplished by:

a. Executing Data Link RESTART command
b. Accessing Diagnostic PROM
c. Cycling ac power.

Following CPU restart, system software attempts to locate the error and to determine if processor operation should continue despite the error.

The processor may override parity protection. In this mode, parity errors are indicated on the display by forcing the underlining of all CRT characters. Parity detection circuitry is tested by forcing bad parity to be written and then reading back the same data location.

2.2.4.10 Z-80A CPU (Figure 2-6)

The Z-80A CPU controls workstation logic. CPU signals are sequenced according to both its internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bi-directional data flow is accomplished by an eight-bit, tri-state data bus. The CPU transmits address information through a sixteen-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

a. M1 -- CPU Fetch Cycle. This line is active during the first cycle (fetch cycle) of each instruction-request cycle, and during the special interrupt cycles.

b. MREQ -- Memory Request. Active when the CPU accesses memory to fetch either an instruction or data.

c. IORQ -- Input/Output Request. Becomes active to indicate either an input or an output to a peripheral device during the interrupt-acknowledge cycles.

d. RD -- Read. When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.

e. WR -- Write. When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.

f. RFSH -- Refresh. During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines. These lines are:

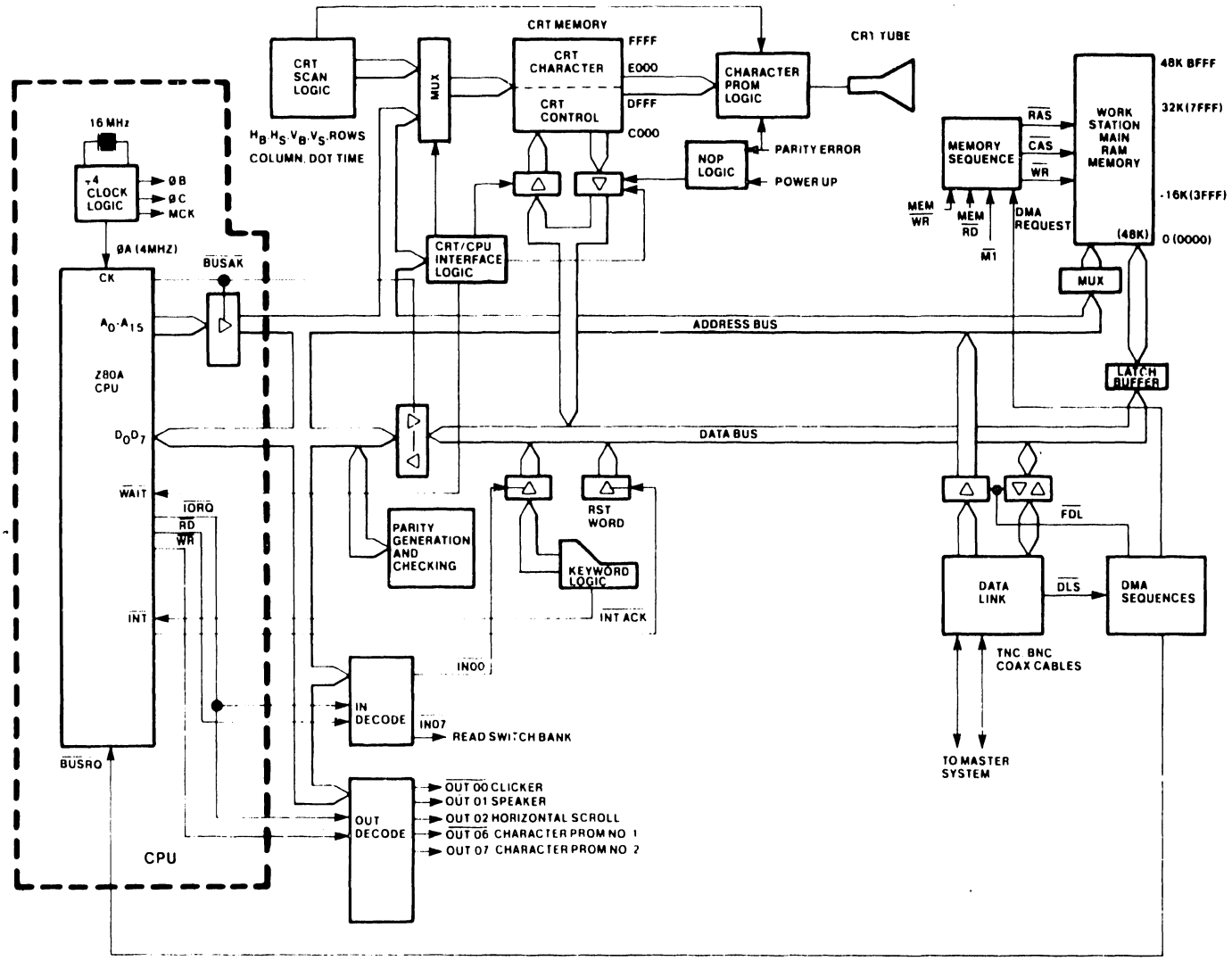


Figure 2-6 Z-80 CPU

a. BUSRQ -- Bus Request. Becomes active when an outside device requests bus access. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device.

b. BUSAK -- Bus Acknowledge. Becomes active to indicate that the CPU has complied with a BUSRQ.

c. WAIT -- Becomes active to request the CPU to extend the current memory-access or I/O cycle as long as the WAIT is present. It is employed in this workstation to synchronize CPU and CRT logic during data transfers.

2.2.4.11 CPU Interrupts

The Workstation employs one interrupt mode, mode 0, which is both hardware and software selected. At power-up, both the CPU and the external hardware are set for mode 0 type interrupts. When an interrupt is generated in this mode the CPU is restarted to address 0000 HEX. In the VS/WP/OIS AWS, this interrupt is asserted with each keystroke. CPU interrupts must be re-enabled after each interrupt so that further interrupts can be accepted.

The CPU employs two interrupt inputs:

a. NMI -- Non-Maskable Interrupt. An NMI is an unconditional entrance to the program.

b. INT -- Interrupt. INT is the input signal for all other interrupting devices in the system that are under software control.

2.2.5 210-7544/7744 DATA LINK/MEMORY PCA

The 7544/7744 PCA contains Main Memory, Data Link and DMA Control, as well as a Bootstrap PROM.

2.2.5.1 Bootstrap PROM (VS Only)

The Bootstrap PROM holds special instructions which allow the AWS to read diskettes without AWS microcode being down-loaded from the Master CPU.

2.2.5.2 Memory

Workstation memory is configured in three categories (Figure 2-7): Main Memory, CRT Memory, and PROM (Bootstrap) Memory.

2.2.5.2.1 Main Memory

This board is available with four Main Memory RAM loadings, however, for AWS operation, 48k of RAM is the minimum requirement, with 64k being required for full OIS capability.

Main RAM can be accessed by both the CPU and the Data Link. (The Data Link is a DMA path.) Main RAM occupies addresses from 0 to the upper limit of the loading; the maximum is 64K. Note, however, that some master units are limited in the amount of slave memory they can address through the Data Link.

Row Address Select (RAS) and Column Address Select (CAS) logic is employed to address main memory. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting 16-bit main memory addresses to be written and read by the 8-bit Z-80A CPU. RAS/CAS logic transfers highand low-order address bits through the same chip pins at different times.

RAS/CAS cycles are required any time main memory is addressed. Main memory is addressed during these operations:

-CPU instruction fetch/refresh cycle
-CPU data read
-CPU data write
-DMA transfer.

A CPU instruction fetch is requested for as long as the CPU indicates that an instruction address is on the address bus. This request is delayed by one CPU clock time.

2.2.5.2.2 CRT Memory

CRT Memory is discussed in Section 2.2.4.5. CRT RAM occupies addresses from 48K to 64K. This portion of memory can be addressed only by the CPU and by CRT scan logic. No DMA path can access CRT memory. The CPU writes characters that are to appear on the screen, and may read characters that are already being displayed.

Although CRT memory contains fewer than 4k display characters it requires 16k of address space. The additional addressing is needed for attribute memory and to support the row/column addressing method. CRT memory-address space is mapped into the top 16k of main memory to simplify CRT display update by the CPU. Special logic permits the top 16k of memory to be switched from CRT memory to additional main (program) memory when the workstation is used for data processing applications.

2.2.5.2.3 Bootstrap PROM (VS AWS Only)

The Bootstrap PROM overlays the bottom 2k of main memory. If the PROM has been selected, the bottom 2k of RAM cannot be read, although it can be written. The PROM should be selected only as described in Appendix B.

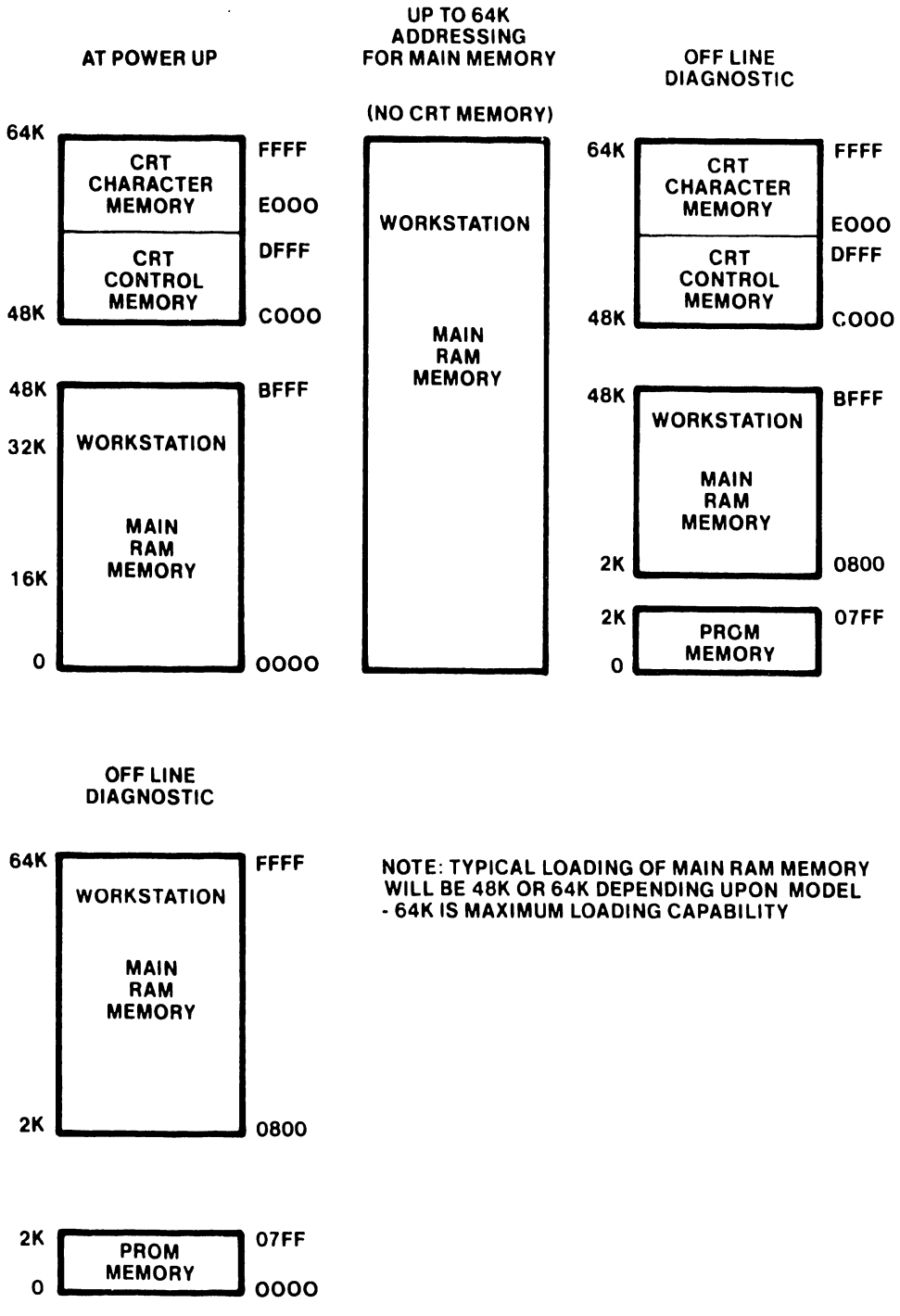


Figure 2-7 Memory Organization

Both main and CRT memories have a parity bit. This bit is checked for data integrity on every read. PROM memory is not checked for parity. When a parity error is detected, the CPU stops and all characters are underlined on the CRT display. When the PROM is read, memory parity errors are cleared.

2.2.5.3 Data Link

The data link (Figure 2-8) permits the Master to transfer data at high speed between its main memory (or disk) and main memory in its peripheral subsystems. In particular, the Master uses this link to load programs into workstations, store documents produced at workstations, and to feed high-speed printers.

Each workstation is connected to the Master separately, through a radial bus structure. All transmissions are controlled by the Master.

Data is transferred directly between memories using DMA logic. Data transfer is carried out in a serial, asynchronous, byte-oriented format using a half-duplex line. The transmission line itself is a balanced pair of coaxial cables operating at 4M baud. The actual data transfer rate is approximately 260k bytes per second.

2.2.5.3.1 Data Link Commands

Six Data Link commands permit the Master to:

a. Check Slave STATUS and ID
b. Initiate Slave Operation (RESTART)
c. Load Slave Memory (WRITE -- 2 commands)
d. Store Slave Data (READ -- 2 commands)

STATUS and ID commands send Slave status and ID to the Master on command.

RESTART commands reset the Slave CPU on command from the Master.

WRITE and READ commands may each transfer either 1 byte or 256 bytes. A one-byte command transfers a single DMA cycle. A 256-byte command transfers a single page of data.

WRITE DATA (1 byte) commands the Slave to receive data (one DMA cycle) from the Master on command.

WRITE BYTE (256 bytes) commands the Slave to receive data (one page) from the Master on command.

READ DATA (1 byte) commands the Slave to send data (one DMA cycle) to the Master on command.

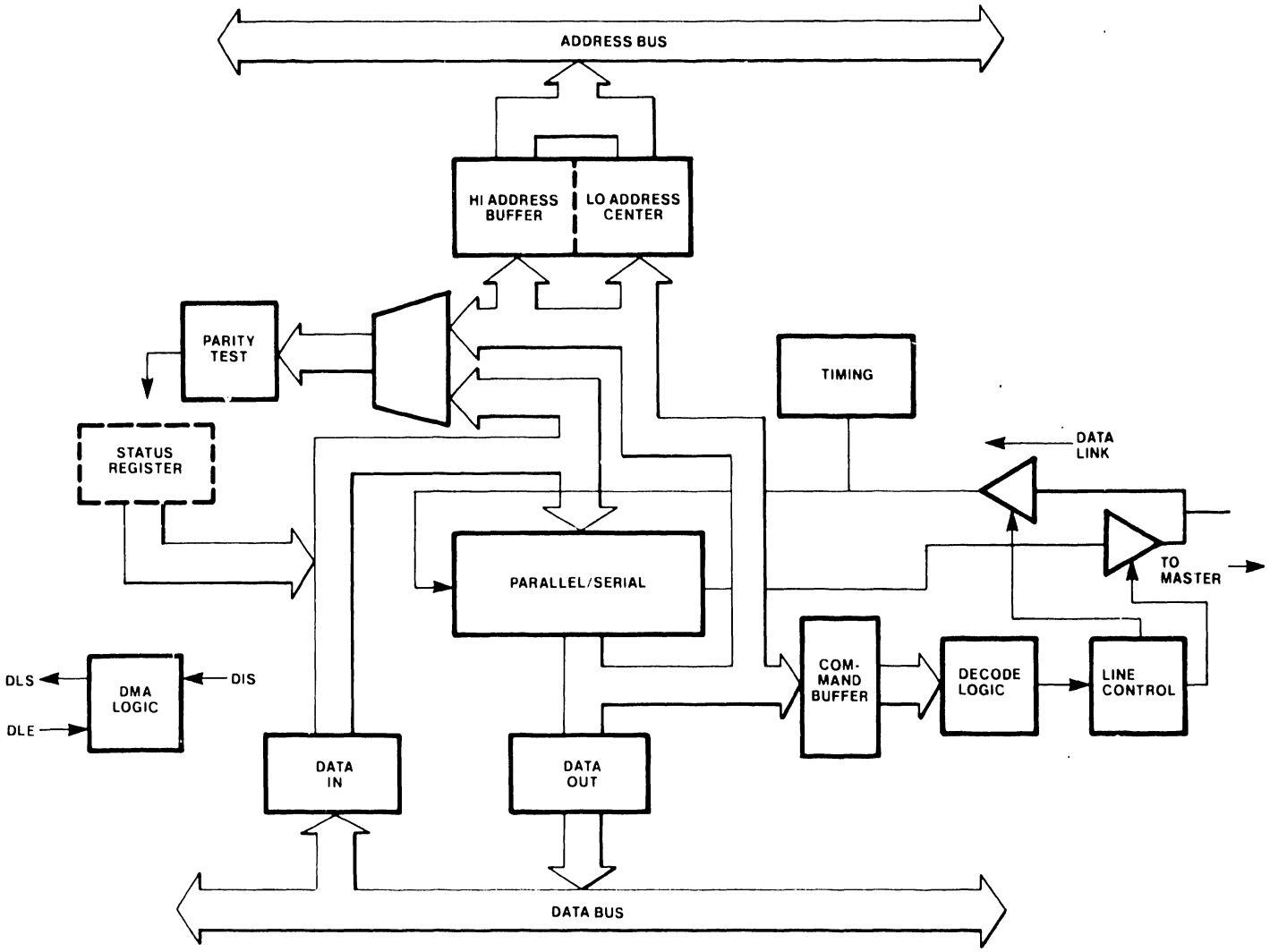


Figure 2-8 Data Link Block Diagram

READ BYTE (256 bytes) commands the Slave to send data (one page) to the Master on command.

2.2.5.3.2 Data Path Logic Function

The data path defines the path by which information bytes are transferred between the serial data link and the data bus, address bus, command register, or status register.

The workstation portion of the data link normally monitors the serial, half-duplex transmission line. The first "1" detected by the differential line receiver causes a timing circuit to count out the eleven-bit intervals needed for a byte transfer. When the last bit of the serial/parallel shift register has been loaded, line parity is tested, the first byte of information is loaded into a command register, and a DMA bus request is initiated. Since stray line noise may start the timing circuits, three bits in the first byte are checked for a special header character. The remaining bits can be decoded to indicate a command if and only if the header is correct.

After the first byte has been transmitted, data link operation depends on the decoded command. A Data Transfer command (Read or Write) loads the next two bytes into the high and low address registers, respectively. The low address register is a counter that increments the DMA byte address following each transfer. A 256-byte transfer command ends when the address counter overflows. For Write operations, a data byte(s) immediately follows the low half of the address. For Read operations, line-control logic must reverse the half-duplex line before data can be sent to the master. A built-in delay (8 microseconds) provides time for the line to quiet before data is transmitted.

Non-data commands (Status and Restart) do not transfer an address. Restart generates a 1.8-microsecond reset pulse to the Workstation CPU. Status causes a Data Link Status Word to be transmitted to the Master CPU after a line reversal.

The Master monitors each command during its execution and clears the Data Link when the command has been completed.

2.2.5.3.3 Timing Logic Function

Timing is normally enabled to receive data. Timing logic recognizes the start bit preceding each byte and determines when the entire byte has been received. It also provides bit timing when information is transmitted to the Master. During Read and Status commands, timing logic clears timing during line reversal and maintains continuous timing while transmitting.

2.2.5.3.4 Line Control

Line control ensures that the Data Link is ready to receive command inputs

from the Master when the Data Link is not in use, determines that the line is quiet before reversing the half-duplex line, generates and checks line parity on each byte, and clears the Data Link both after each command and in the event of a line failure.

Line Control logic interlocks the Data Line Drivers and Receivers to ensure that the Workstation does not transmit into itself. The Line Drivers are disabled until they are required to transmit data or status to the Master during a specific command.

2.2.5.3.5 Command Decode Logic Function

This function decodes and validates commands from the Master after a valid command (three-bit header) has been recognized.

2.2.5.3.6 Bus Requests and DMA Operation

Bus Requests are generated by the Data Link when a non-processor device requires direct-memory-access (DMA) for a data transfer. DMA transfers typically move blocks of data between main memory and mass storage devices. DMA operations have a higher priority than CPU operations due to real-time requirements.

Before a DMA device can use the bus it must gain control of the bus from the CPU. The CPU permits it to do so by recognizing the presence of a Bus Request and disabling its own bus inputs and outputs as soon as its current machine cycle has been completed. The CPU indicates when the cycle is complete by asserting Bus Acknowledge. The DMA device now has control of the bus for as long as Bus Request remains asserted.

Since CPU bus-control logic is not available to supply data transfer timing or to initiate refresh cycles during a DMA operation, separate DMA bus timing must be provided by the DMA device. Some provision is required to ensure that refreshes occur often enough to preserve memory content.

DMA requests are accepted from the Data Link. The Data Link is given priority to reduce delays in the Master. This priority schedule allows a pending Disk Bus Request to be converted to a Data Link Transfer if the Data Link Request is received before disk transfer actually begins. Priority logic, then, effectively inhibits the unselected DMA device once DMA transfers begin.

DMA Enables permit selected devices to place DMA addresses and data onto the system bus. DMA Enables also ensure that only the selected device is allowed to control the main memory write control lines.

2.2.6 210-7313 CRT JUNCTION PCA

The CRT Junction PCA is an interconnect/distribution point for the signals connected between the Terminal and the Archiver Master by the KEYBOARD connector and associated cable. (Refer to Figure 2-9.)

Keyboard logic lines are routed directly from the CRT Junction PCA connector to the keyboard by a ribbon cable. In addition to the keyboard logic lines are two power supply lines (+12 and +24 volts), and the two lines associated with the speaker and clicker.

The +12 volt input from the Archiver Master is applied to a voltage regulator device which provides +5 volts regulated for the keyboard logic and for other circuitry on the CRT Junction PCA. The +5 volt regulator is adjustable. The +24 volt input is applied to a 17 volt zener and forwarded to the keyboard.

The logic-level signal that triggers the clicker is applied to a driver stage which switches the current for the clicker device on the keyboard. The speaker trigger lifts a reset condition from the speaker astable multivibrator which oscillates for the duration of the active SPK signal, thus driving the speaker with an audio tone.

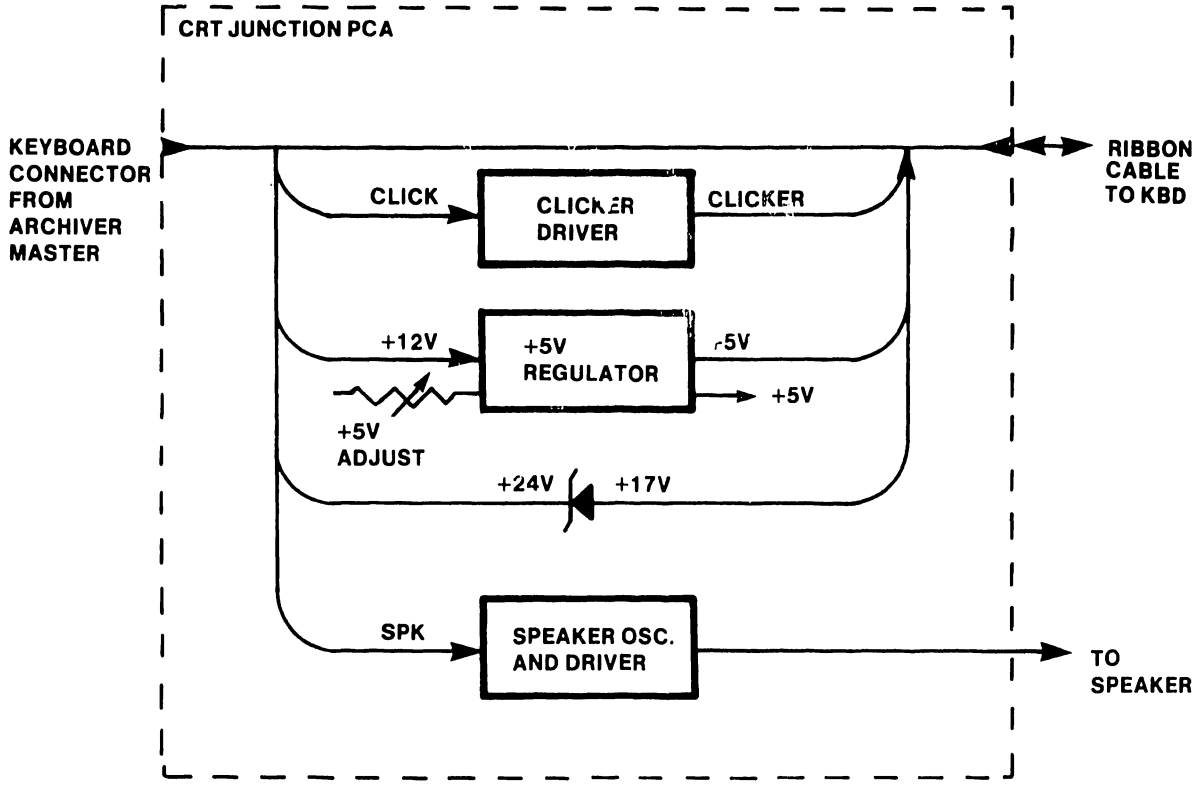


Figure 2-9 CRT Junction PCA Block Diagram

2.3 ARCHIVING FUNCTIONS

2.3.1 HARDWARE ORGANIZATION

Archiving functions are carried out by subassemblies contained wholly in the Archiving Master. These include the Soft-Sector Diskette Controller Board, the Hard-Sector Diskette Controller Board and the Disk Drive unit. Each of the boards and the two Disk Drive models are covered separately in subsections 2.3.4 through 2.3.6.

The Motherboard and the Power Supply, both within the Archiving Master, are described below in subsections 2.3.2 and 2.3.3.

2.3.2 ARCHIVING MASTER MOTHERBOARD

The 210-7615 Motherboard (VS) and the 210-7546 Motherboard (WP/OIS) provide socket connections and printed-circuit back-panel wiring for the logic cards used in this system, as well as extra socket locations and printed-circuit connections compatible with other applications. The VS Motherboard contains additional circuit connections required to support the Soft-Sector Controller Board, which is unique to the VS AWS.

The Motherboard is designed so as to route as many signals as possible to identically-numbered pins on all card locations, as shown in the motherboard schematics. These schematics actually are mnemonic listings for actively-wired connector pins, including signal connections that are not currently used by the logic cards normally installed in those locations. This common-bus design can accommodate future growth.

Active interconnections can be traced on the schematics for the existing logic cards. Although the Motherboard contains no active components, its circuitry does include the sensing resistor for the +5V bus, together with interconnections between various components of the overall power-supply subsystem, as shown in the 7316 PS Regulator Board schematic.

2.3.3 POWER SUPPLY REGULATOR (WLI P/N 210-7316)

The Master Unit power supply subsystem consists of an input electromagnetic interference (EMI) box, a power transformer, a regulator card and various filter capacitors, together with one external sense resistor mounted on the Motherboard and a pass transistor mounted on the heatsink assembly. The EMI box contains the power switch and fuse and two unfused convenience outlets, together with an EMI filter to eliminate undesirable signals that might be supplied via the input power connections to the power transformer. The power transformer has three center-tapped secondaries, which are full-wave rectified to provide unregulated +28VUR, +8VUR, and both +15VUR and -15VUR outputs. Circuitry on the regulator card and the heat sink assembly then converts these unregulated dc voltages to regulated +24VR, +12VR, +5VR, -5VR, and -12VR outputs for use by the Master Unit logic cards, by the disk drive, and

(via cable connection) by the keyboard circuit in the Terminal. (The monitor assembly in the Terminal has its own independent power supply.)

The two negative-voltage regulator circuits are not adjustable, but the three positive-voltage circuits contain respective adjustment potentiometers that are accessible from the top edge of the regulator card: R10 to adjust the +24V level, R17 to adjust the +5V level, and R35 to adjust the +12V level. Since each regulator circuit has a current-limiting design, including a voltage fold-back capability, no fuses are required for any of these regulator circuits.

The +5VR regulator circuit uses a 723-type voltage regulator (L2) as its basic control element. A reference voltage developed inside the 723-type chip is applied through a variable voltage divider controlled by +5V adjustment potentiometer R17 to the non-inverting input of that same regulator chip to allow for adjustment of the +5VR output level to the system.

The inverting-input connection to that same regulator chip is the output of a 2N5301 pass transistor mounted on the external heat sink assembly, as passed through sense resistor R1 on the Motherboard. Fed by the diode-rectified +8VUR transformer output, this pass transistor output connects through card pins D and 4 as the nominal +5VR system voltage to the 723-type regulator chip. The resulting bias and error signals cause a current flow through that chip from the +15VUR-supplied V_C terminal through an internal transistor to the V_{OUT} terminal, driving the base of a 2N6387 Darlington amplifier (Q4). The amplified current then controls the output of the source-voltage pass transistor on the external heatsink assembly.

The pass transistor output also connects directly as the +5VS sense input through pin 8 and a voltage divider as one input to an LM339 comparator (L5), which also receives the +5VR input from the other side of the external sense resistor. The output of the comparator normally clamps the CL input of the 723-type regulator to ground potential. If the supply current approaches 15A, however, the comparator switches to let current flow into CL through a 3.3K resistor (R19) connected to the +15VUR line. This condition turns on an internal transistor in the regulator, causing the voltage feedback loop to become degenerative and driving the output to a low voltage that turns off the pass transistor. The LM339 comparator then oscillates, waiting for the excessive load to be removed.

The +12VR power regulation circuit is similar to the just-described +5V circuit, except that the load current is lower and the Darlington amplifier (Q2) serves as the pass transistor. The +12VR regulation circuit is built around 723-type voltage regulator L1, which draws its operating voltage from the +28VUR line. This regulator has its internally-generated reference voltage output connected directly to the non-inverting input, and its V_{OUT} output is fed back to the inverting-input terminal through a variable voltage divider controlled by +12V adjustment potentiometer R35. Resistor R37 provides the necessary current-sense function, and the comparator switches at approximately 2A.

The +24V supply uses another 723-type voltage regulator (L3), this one having its internal reference voltage tied to the non-inverting input through a fixed divider, while the output voltage is fed back to the inverting input through an adjustable divider controlled by +24V adjustment potentiometer R10. A line running from the non-inverting input to the voltage monitoring circuit (L4) shuts down this supply whenever the front-panel reset pushbutton is pressed or or whenever a failure occurs with respect to any of the +12VR, +5VR, or -5VR outputs.

The base-drive circuit of the Darlington pass transistor (Q1) differs from those of the other positive-voltage supplies in that the Q1 transistors are connected in a common-emitter configuration. Drive current is internally dropped from the +28VUR line, and the +24VR output is the Q1 collector-to-emitter voltage drop. The base-drive level connects to V_C of 723-type voltage regulator L3 through the internal circuit and then from V_{OUT} to a current-sink path provided by zener diode D1. Current sense is provided by resistor R7, shutting down the supply at about 2.5A in the same way as described for the other circuits.

The -5VR and -12VR regulator circuits are totally-integrated, non-adjustable circuits (Q5 and Q3, respectively), which provide internal over-current fold-back capacity. They draw their power from the -15VUR side of the 15 Vac output from the transformer.

The voltage monitor circuit is based around another LM339 quad-comparator chip (L4). The outputs of its four comparators are wire-ANDed to produce the *Auto Reset signal at pin J. Three of the comparators check the +12VR, +5VR, and -5VR outputs against zener-controlled reference levels, while the fourth is controlled by a time-constant circuit made up of C5 and R13, which produces a low-level *Prime pulse during power-up or goes low whenever the reset push-button at the front panel is pushed.

2.3.4 DISK DRIVE

The Disk Drive unit in the VS AWS is a Shugart 850/851 Double-Sided/ Double-Density floppy drive. Theory and service instructions for this assembly are provided in the OEM manual reprint as listed in Table 1-1 of this manual. Correction/update information and/or any material peculiar to the VS AWS or other Wang equipment are supplied as PSN supplements to that documentation, and are also listed in Table 1-1.

The Disk Drive unit in the WP/OIS AWS is a Shugart 901 Hard-Sector floppy drive. Theory and service instructions for this assembly are provided in the OEM manual reprint as listed in Table 1-2 of this manual. Correction/update information and/or any material peculiar to the WP/OIS AWS or other Wang equipment are supplied as PSN supplements to that documentation, and are also listed in Table 1-2.

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* These signals are active low.

2.3.5 SOFT-SECTOR DISK CONTROLLER BOARD

The major sub-components of the Soft-Sector Disk Controller Board are connected to a single system bus. Two interfaces are used: device level interface (DLI) and host system interface (HSI). The DLI connects with the Shugart 850/851 Double Sided, Double Density (DSDD) Disk Drive while the HSI connects directly to the host system address, data and control buses.

2.3.5.1 Device Level Interface (DLI)

Referring to Figure 2-10, the DLI consists of the following functional blocks:

- Data Separator
- Write Data/Precompensation
- Status Receivers
- Line Drivers
- Programmable Track Counter (Filter Switch)

2.3.5.1.1 Data Separator

This circuit is a phase-locked oscillator and is used to recover data from recorded media. The circuit is designed to allow maximum margin in separating data and generating a clock window for use with the 765 Floppy Disk Controller (FDC) device.

2.3.5.1.2 Write Data/Precompensation

This network allows data to be written to a diskette with or without precompensation. IBM compatibility requires that precompensation is not used.

2.3.5.1.3 Status Receivers

The Status Receivers hold status data received from the Disk Drive, for interrogation by the host Z-80 CPU. Details of the input/output status word are given in section 2.3.5.4.

2.3.5.1.4 Line Drivers

Line Drivers amplify control gates and stepping commands to the Disk Drive.

2.3.5.1.5 Programmable Track Counter

This counter is programmed during the initialization phase when power is first applied to the unit. Once the two's complement number has been loaded, the counter keeps track of the cylinder number presently under the read/write head. At the appropriate cylinder, this logic network enables an active

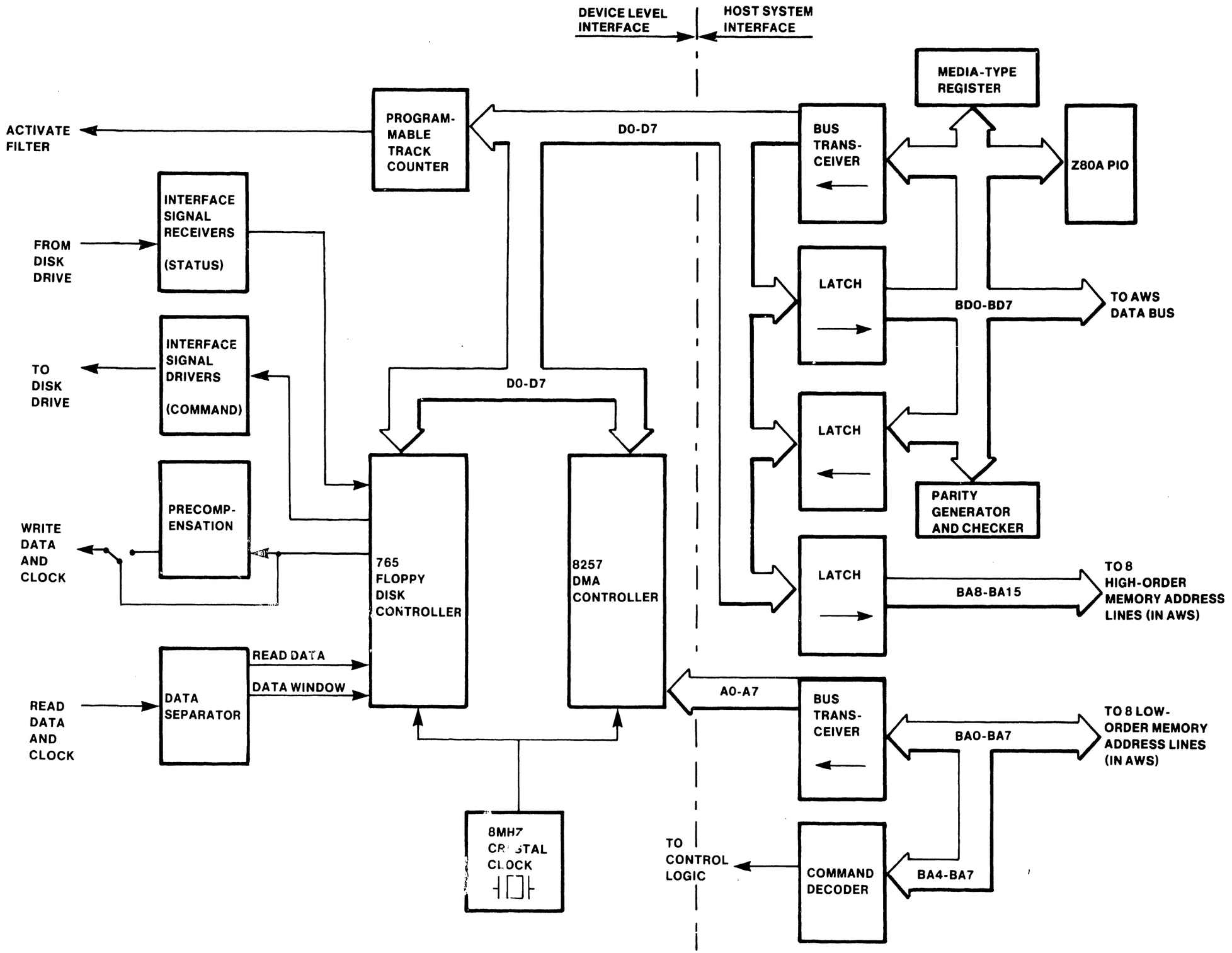


Figure 2-10 Soft-Sector Disk Controller Board Block Diagram

filter within the Disk Drive. For the SA 850/851 Disk Drive, the track switch is set to equal 60 by loading a value of 17.

2.3.5.2 Host System Interface (HSI)

Referring to Figure 2-10, the HSI consists of the following functional blocks:

- Parity Checker/Generator
- Command Decoder (Address Lines)
- Media Type Register
- DMA Hardware:
  - -- Address Register
  - -- Terminal Count Register
  - -- Status Register

2.3.5.2.1 Parity Checker/Generator

This logical network is used to check and generate even parity on the host system bus.

2.3.5.2.2 Command Decoder

The commands used to drive the controller are decoded from the host system bus via this address line decoder. Details of the input/output command word are given in section 2.3.5.3.

2.3.5.2.3 Media Type Register

This register contains information regarding the type of media inserted in the Disk Drive.

2.3.5.2.4 DMA Hardware

This logic network allows the CPU to function during the data transfer phase. Once programmed, the DMA Hardware automatically increments the MAR (memory address register) by +1 each memory cycle. At the correct count of data transfers, the DMA Hardware issues a Terminal Count and stops further data passing. The data count is programmable.

2.3.5.3 Input/Output Command Word (IOCW)

The IOCW specifies the command to be executed and contains all information necessary to perform any task involving a peripheral device, including reading from, writing to, and controlling an I/O device. The IOCW tells the IOP where in main memory any transfer of data is to begin and how many bytes of information are to be transferred. In the case of control functions, the IOCW initiates specific device operations that do not involve data transfer, such as restoring a disk drive.

IOCW Format:

WORD 0 (BYTES 0 AND 1)

Field	Command & Command Modifier Bits								M. M. Source or Target Address							
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Function	C	C	M	M	M	r	i	p	A	A	A	A	A	A	A	A
Digit	1				2				3				4			
Byte	BO								B1							

WORD 0 (BYTES 2 AND 3)

Field	Main Memory Source or Target Address															
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Digit	5				6				7				8			
Byte	B2								B3							

WORD 1 (BYTES 0 AND 1)

Field	Byte Count															
Bit	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
Digit	9				10				11				12			
Byte	B4								B5							

WORD 1 (BYTES 2 AND 3)

Field	Sector Address															
Bit	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Digit	13				14				15				16			
Byte	B6								B7							

WORD 2 (BYTES 0 AND 1)

Field	Sector Address								Not Available							
Bit	64	65	66	67	68	69	70	71	0	1	2	3	4	5	6	7
Digit	17				18											
Byte	B8															

Breakdown of Word 0 (Byte 0) of the IOCW:

Bits 0	Bits 1	Function
C	C	Command Bits
0	0	No Function
0	1	Read from Disk
1	0	Write to Disk
1	1	Control the Disk

Bits 2	Bits 3	Bits 4	(i = 0) Function
M	M	M	Command Modifier Bits
0	0	0	Seek Command
0	0	1	Delete Data Condition (Read/Write Command) Read Device ID & Settings (Control Command)
0	1	0	Set Single Density (FM Mode)
0	1	1	Set Double Density (MFM Mode)
1	0	0	Write Verify (Write Command) Format the Track (Control Command)
1	0	1	"0" Origin Addressing (Wang Format)
1	1	0	"1" Origin Addressing (IBM) Format
1	1	1	Not Used

Bit 5 (r) Retry Bit: If = 1, suppress retries upon detection of errors, and set the EC bit in the IOSW equal to 1 at first occurrence of an error.

Bit 6 (i) Indirect Bit: If = 1 during a Read or Write Command, use the Main Memory Address field in the IOCW (word 0, bytes 1, 2, and 3) as a pointer to an Indirect Address List rather than an Absolute Memory Address. Additional memory fetches may be necessary before the command can be completely decoded.

If = 1 during a Control Command, specifies a Set Sector Size command. MMM contains the sectorization code to be used in the setting.

Bit 7 (p) Platter Type Bit: If = 1, perform the current operation on the removable platter, when applicable.

IOCW Examples:

1. Read Disk Sector(s) Command |0 1 M M | M r i p|

   a. Where MMM = 000:

      The Read Command, which has an implied "seek" in it, transfers data

on the disk starting at the relative 256-byte pseudo-sector number specified in bytes 6-7-8, and extending n-bytes long (where "n" is the number specified in bytes 4-5) to Main Memory starting at the target address specified in bytes 1-2-3. The 256-byte pseudo-sector specification implies limitation on the value of the number supplied in bytes 6-7-8 since some sector sizes are greater than 256 bytes/sector:

If the sector size is (bytes/sector):	Then the limitations on the pseudo-sector address are:
128	None (sectors are read in pairs)
256	None
512	One low-order zero bit required
1024	Two low-order zero bits required
2048	Three low-order zero bits required

The "r" and "i" bits act as previously defined.

b. Where MMM = 001:

This Read Command option forces the firmware to check the data qualifier on the media itself to verify that the specified sector is flagged as "Deleted Data." If not, the IOSW will indicate "Illegal Sector ID" (IID) and no transfer will take place.

2. Write Disk Sector(s) Command |1 0 M M | M r i p|

a. Where MMM = 000:

The standard Write Command is similar to the read operation except that data is transferred from Main Memory to the disk media, and what was a target address specified in bytes 1-2-3 is now a source address specifying where to fetch the data to be transferred to the disk. The "r" and "i" bits act as defined previously.

b. Where MMM = 001:

Same as "a" above except that a "Deleted Data Address Mark" is written on the media which makes the corresponding data inaccessible except through the "Read Deleted Data" command. This feature is available in the NEC-756 device and is supported by the firmware but its use is left up to the CPU programmer.

c. Where MMM = 100:

This option of the Write Command forces a verify phase after the write phase whereby the firmware reads the data just written on the disk

in the write phase and reports any problems encountered in the IOSW status flags.

3. Seek Addressed Cylinder Command |1 1 0 0 | 0 r 0 x|

This command is not required since the I/O commands all imply a seek operation prior to any other action. It is listed here and implemented in the firmware for compatibility with the other disk product commands and for any special use the CPU programmer may find. The target cylinder where the access mechanism is positioned as a result of this command is computed from the relative sector address specified in bytes 6-7-8. The Main Memory and Byte Count fields are ignored, and the "r" bit functions as previously defined.

4. Format Addressed Track Command |1 1 1 0 | 0 r 0 x|

The smallest unit of disk space that can be formatted at a time is limited by the DSDD hardware to a track and the contents of the control information used in the formatting procedure. This is generated in the NEC-765 device and is compatible with the IBM System 34 (double density) and IBM System 3740/3741 (single density) formats. The track to be formatted is derived from the relative sector address specified in bytes 6-7-8, and all sectors residing there are formatted. The option "r" functions as previously defined.

5. Get Device ID and Settings Command |1 1 0 0 | 1 x 0 x|

This Control Command is a NOOP (no operation) command since the only action that results is the return of the IOSW (Input/Output Status Word). The IOSW contains the device ID, media type, and format codes. The NOOP qualification is based on the fact that the IOSW is returned after the execution of all other commands. The CPU examines the IOSW device-dependent sub-fields returned by this (or any other) command at the time the media is loaded, since this is the only way to get an indication of what type of media is inserted in the drive (hard/soft sector, single/double sided). Refer to section 2.3.5.4 for more information about the IOSW device-dependent code bits.

6. Set Density Command |1 1 0 1 | 0 x 0 x| & |1 1 0 1 | 1 x 0 x|

The Set Density Command directs the archiver to set the recording mode of the diskette drive to single (FM) or double (MFM) density mode. The codes are as follows:

```
Single Density:   |1 1 0 1 | 0 x 0 x|
Double Density:   |1 1 0 1 | 1 x 0 x|
```

The Main Memory Address field, the Data Count field, and the Device Dependent field as well as the "r" and "p" command modifier bits are ignored when this command is detected since the Command Byte bits alone completely specify the operation requested. This command is only valid for soft-sectored media, which is the default setting.

7. Set 0 or 1 Origin Sector Address Logic |1 1 1 0 \| 1 x 0 x| or
|1 1 1 1 \| 0 x 0 x|

IBM formatted media uses "1 origin" logic in addressing sectors within tracks. The command detailed here will enable the CPU user to read or write media brought from or taken to an IBM environment. The "0 origin" logic is the default setting and is Wang's standard mode. The codes are as follows:

0 Origin Logic: |1 1 1 0 \| 1 x 0 x|
1 Origin Logic: |1 1 1 1 \| 0 x 0 x|

The CPU user may need to set other IBM compatible parameters in order to read or write IBM compatible media. This command is only valid with soft-sectored media.

8. Set Sector Size |1 1 0 0 \| 0 x 0 x| through |1 1 1 0 \| 0 x 1 x|

A Control Command is understood as a Set Sector Size command when the "i" bit is active and the MMM field is set to one of the values listed in the following table. The effect of the command on the way data is recorded on the DSDD media is dependent on the current density setting as shown below.

i=1	FM (Single Density)		MFM (Double Density)	
MMM	Bytes/Sector	Sectors/Track	Bytes/Sector	Sectors/Track
000	128	26	Invalid	Invalid
001	256	15	256	26
010	512	8	512	15
011	1024	4	1024	8
100	2048	2	2048	4

The default setting of the sector size is 1024 bytes/sector and remains unchanged until the firmware receives a command to change it to one of the above valid settings. Since the default density setting is double density, the default number of sectors per track is 8.

2.3.5.4 Input/Output Status Word (IOSW)

All communication from an I/O device to the VS system is by means of I/O status words. An IOSW is stored for every I/O interrupt and is from one to eight bytes in length.

IOSW Format:

WORD 0 (BYTES 0 AND 1)

Field	General Status								Error Status							
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Function	IRQ	NC	EC	U	PC		DAR		IC	MPE	MAE	DM	DAM	IL	DCT/PP/DP	
Digit	1				2				3				4			
Byte	B0								B1							

WORD 0 (BYTES 2 AND 3)

Field	Device Dependent Codes															
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Function					IDA	IDC	SO	SI	WP	NRO		DC	IID	CRC	0	ISP
Digit	5				6				7				8			
Byte	B2								B3							

WORD 1 (BYTES 0 AND 1)

Field	Residual Byte Count															
Bit	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
Digit	9				10				11				12			
Byte	B4								B5							

WORD 1 (BYTES 2 AND 3)

Field	Retry Indicators								Add. Device Dependent Status Bits							
Bit	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Function	Retry Setup				No. of Retries				DRO		MDF			MDT	DDS	ZOO
Digit	13				14				15				16			
Byte	B6								B7							

Breakdown of the IOSW:

1. Word 0, Byte 0 (General Status Byte):

   Bit 0 (IRQ) Intervention Required: If = 1, indicates operator intervention required before further device operation is possible.

Bit 1 (NC) Normal Completion: If = 1, indicates normal completion even if retries were needed to correct an initial problem. The EC bit flags the cases where retries were needed before normal completion was reached.

Bit 2 (EC) Error Completion: If = 1, indicates error completion even if retries cleared the original problem.

Bit 3 (U) Unsolicited Interrupt: If = 1, indicates the interrupt causing this IOSW to be returned was unsolicited. More bits are checked before determining the cause of this interrupt.

Bit 4 (PC) Processing Complete: If = 1, indicates the IOP is now "Ready." This bit is set by the IOP firmware rather than the device Z-80 processor firmware.

Bit 5 (DAR) Data Area Early Release: This bit signifies a Data Area Early Release. It is not used in conjunction with the DSDD firmware.

Bits 6 & 7 These bits are not used.

2. Word 0, Byte 1 (Error Status Byte):

Bit 8 (IC) Invalid Command: If = 1, flags an invalid command, i.e., any command not supported by the device processor.

Bit 9 (MPE) Memory Parity Error: If = 1, flags a memory parity error detected by either the IOP or the device processor.

Bit 10 (MAE) Memory Address Error: If = 1, flags a Main Memory Address error specification in bytes 1-2-3 of the IOCW.

Bit 11 (DM) Device Malfunction: If = 1, flags a device malfunction.

Bit 12 (DAM) Device Malfunction After Transmission: Similar to DM except the malfunction in the device or memory was detected after a data transmission operation.

Bit 13 (IL) Incorrect Length: If = 1, indicates the Byte Count specified in bytes 4-5 (bits 32 - 47, Residual Byte Count) was not valid for this device, for the media density, or for the sector size specification. Byte counts that imply multi-cylinder operations are also flagged as IL.

Bit 14 - 15

1 1 (DCT) Device Configuration Table: Signifies the IOP requires a device configuration table for the device in question before any further I/O operation is possible (22V06 or 22V17).

1 0 (PP) Peripheral Processor: Signifies a peripheral processor microprogram is required before any further I/O processing can be resumed (22V06 only).

0 1 (DP) Device Processor: Signifies a device processor microprogram load request to the CPU, without which further communication with the device is not possible. This indicates the device processor firmware was discontinued and has to be refreshed and restarted (22V07 or 22V17).

Breakdown of Device Dependent Codes:

1. Word 0, Byte 2 (IOSW):

Bit 20 (IDA) Illegal Disk Address: If = 1, flags an illegal disk address (address too large for disk or address not track-aligned).

Bit 21 (IDC) Illegal Data Count: If = 1, flags an illegal data count for the disk (e.g., spans the cylinder).

Bit 22 (SO) Sector Overrun: If = 1, flags a sector overrun condition.

Bit 23 (SI) Incomplete Seek: If = 1, flags a seek incomplete condition.

2. Word 0, Byte 3 (IOSW):

Bit 24 (WP) Write Protect: If = 1, indicates a write protect condition. (In the case of the DSDD drive, the indication is on the media in the form of a tab on the floppy edge rather than a setting of the drive itself.)

Bit 25 (NRO) Not Ready: If = 1, indicates a not ready signal was received before or while the drive was in operation. This informs the CPU there may be unsafe data on the media at the spot where the current operation was specified, or there is no media inserted in the drive.

Bit 27 (DC) Data Compare Error: If = 1, flags a data compare error as a result of a Verify operation.

Bit 28 (IID) Illegal Sector ID: If = 1, flags an illegal sector ID on the media, hence there may be unsafe data at that spot.

Bit 29 (CRC) CRC Error: If = 1, flags an invalid CRC was detected by the hardware.

Bit 30 (O) Memory Overrun: Not applicable since the DMA is local to the device processor environment.

Bit 31 (ISP) Short Sector: Indicates a short sector was detected.

3. Word 1, Byte 7 (IOSW):

Bit 56 (DRO) Not used. Reserved for dual-port drives only.

Bit 57-59 (MDF) Media Format: Indicates the sector size and the relative sector/track currently in effect. The code used is the same as that for a Set Sector Size command (refer to section 2.3.5.3, IOCW example 8).

Bit 60-61 (MDT) Media Type:
00 = Drive Not Ready (no media inserted)
01 = Media is Hard-Sectored
10 = Media is Soft-Sectored, Single-Sided
11 = Media is Soft-Sectored, Double-Sided

Bit 62 (DDS) Double Density Status:
0 = Single Density is in effect
1 = Double Density is in effect

Bit 63 (ZOO) Zero/One Origin Sector Addressing Status:
0 = 0 Origin in effect (Wang-Compatible)
1 = 1 Origin in effect (IBM-Compatible)

Glossary of Codes for the Archiver IOCW and IOSW

Code	Definition
CC	Command Code
CRC	Invalid CRC
DAM	Device/Memory Error (detected after transmission)
DAR	Not used on Archiver diskette
DC	Data Compare Error
DCT	IOP requires Device Configuration Table (DCT, 22V06) or Device Routing Table (DRT, 22V17)
DDS	Double Density Status 0 = single density 1 = double density
DM	Device Malfunction

Code	Definition
DP	Device Processor Microprogram Required (22V07 and 22V17 IOPs)
DRO	Drive Reserved by Other Port (dual port drives only)
EC	Error Completion
i	R/W Command = address field is indirect address list Control Command = specifies a Set Sector Size command
IC	Invalid Command
IDA	Illegal Disk Address
IDC	Illegal Data Count
IL	Incorrect Length
IID	Illegal Sector ID
IRQ	Intervention Required
ISP	Short Sector
MPE	Memory Parity Error
MAP	Memory Address Error (in bytes 1-2-3 of IOCW)
MDF	Media Format
MDT	Media Type 00 = drive not ready (no media) 01 = hard sector 10 = soft sector, single-sided 11 = soft sector, double-sided
MMM	Command Modifier Bits
NC	Normal Completion
NRO	No Ready Signal While Drive in Operation
O	Memory Overrun (not applicable for Archiver)
p	Perform Operation on Removable Platter (ignored by firmware)
PC	IOP Ready
PP	Peripheral Processor Microprogram Required (22V06 IOP Only)
r	Skip Retry on Errors and Set EC Bit in IOSW
SO	Sector Overrun
SI	Seek Incomplete
WP	Write Protect
U	Unsolicited Interrupt
ZOO	Zero/One Origin Sector Addressing 0 = 0 origin in effect 1 = 1 origin in effect

2.3.6 HARD-SECTOR CONTROLLER BOARD

The 210-7843-A and 210-7543-A Hard-Sector Controller Boards serve two functions in the Archiving Workstation, data transfer to/from and control of the the hard-sector disk drive unit, and, in the -1A version of the board, telecommunications (TC) control. The main elements are shown in Figure 2-11 and discussed below.

2.3.6.1 Relation to the AWS System

The Hard-Sector Controller Board uses the bi-directional Data Bus of the AWS to transfer data for both input and output operations. It uses the uni-directional Address Bus for Target and Source memory addresses (see section 2.3.6.2).

The Z-80 microprocessor on the CRT/CPU Board controls all operations of the Archiving Disk Drive through the Input/Output Command signals from the Input/Output Decoders (also on the CRT/CPU Board). The Data Link/Memory Board contains the main memory used to store and retrieve data used for the archiving function. The Data Link portion of that board serves as the interface between the AWS and the Host CPU.

2.3.6.2 Memory Address Registers (MAR), Page and Byte Count

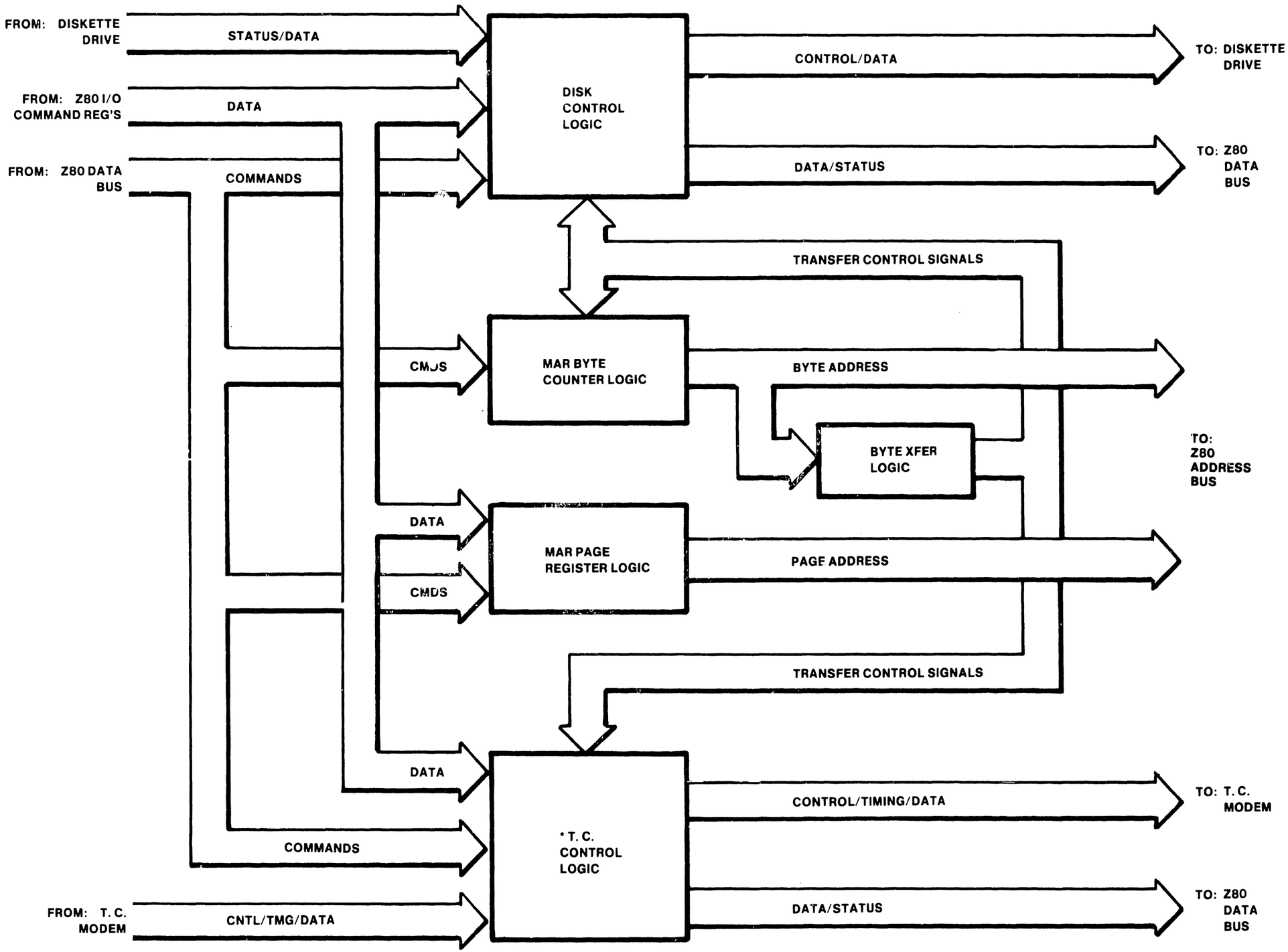
To accomplish either the archiving or the TC function, a main memory Source or Target address is referred to by the Hard-Sector Controller Board.

The main memory Source address is the address from which data will be retrieved and sent out to some device. The MAR Page Register and MAR Byte Counter operate together to provide this address. The Z-80 CPU loads the MAR Page Register with the page address through its Data Bus. The MAR Byte Counter is reset to zero after the page address is loaded. At this point, input or output transfers can begin, starting from the address specified by the MAR Page Register and MAR Byte Counter. The MAR Byte Counter will increment by one as each byte is transferred into or out of memory until all 256 bytes are transferred, thus keeping track of the specific address within the memory page specified by the MAR Page Register.

The main memory Target address is the address to which data is stored. The MAR Page Register and MAR Byte Counter perform the same function for the Target address as for the Source address described above, that is, pointing to some address in main memory.

2.3.6.3 Data Transfer

Data is transferred to the Disk Drive or a TC modem via the Z-80 Data Bus. Data sent to either circuit is sent in parallel (eight bits wide). Upon receiving data, both circuits verify correct parity, convert the data to



*T.C. (TELECOMMUNICATIONS) NOT AVAILABLE ON VS AWS.

Figure 2-11 Hard-Sector Controller PCA Block Diagram

serial form and then transmit it to either the Disk Drive or a TC modem.

Data can also be transferred into the main memory from the Archiving Disk Drive or a TC modem. The actual data path is the reverse of the one described above, that is, data is received in serial format from either the Disk Drive or a TC modem, checked for parity errors and converted to eight-bit parallel format. The data is then forwarded to the main memory Target address one byte at a time.

2.3.6.4 Disk Control Operations

2.3.6.4.1 Track Positioning

When power is applied to the AWS, the CPU determines the position of the read/write head in the Disk Drive by stepping the head down until the Track Zero Flag is detected. This flag causes an interrupt of the CPU. After confirming that the interrupt was caused by the Track Zero Flag, the CPU sets an internal counter to zero and maintains track count from that point on.

The actual positioning of the read/write heads is accomplished by first selecting the Disk Drive via the OUT'0B' instruction. This instruction generates the following signals:

Head Direction	(HDIR)
Floppy Drive Select	(SFL1 or SFL2)
Head Load	(HDL1 or HDL2)

Stepping of the read/write head is caused by executing the OUT'08' instruction, which generates the Head Step signal (HSTP).

2.3.6.4.2 Sector Detection

Sector data is tracked on this board, rather than on the CRT/CPU board as with track data. The primary element used to track sector data is a Z-80 Counter Timer Circuit (CTC). The CTC contains four down counters, two of which are used for tracking sector data. An eight-bit value is loaded into the CTC down counter, received from the Z-80 Data Bus. The CTC is then decremented each time a Sector Pulse Out signal is received from the index/sector logic, which generates the signal as a result of the sector and index holes on the floppy diskette media.

When the down counter in the CTC reaches a count of zero, it interrupts the CPU. Upon receipt of this interrupt, the CPU starts the sequence that will result in the actual input or output data transfer.

2.3.6.5 TC Control

TC is supported on the -1A version of the Hard-Sector Controller Board. The TC option enables the AWS to be connected as a remote workstation, communicating with the Host CPU's data link via telephone lines.

TC input/output operations are 256 bytes in length, with the main memory Source/Target addresses formed through the MAR Page Register and MAR Byte Counter.

The heart of the TC portion of the board is the Universal Synchronous/Asynchronous Receiver/Transmitter (USART) device. The USART accepts parallel format data, as on the system data bus, and converts it to serial format for presentation to a TC modem. At the same time it can accept serial data from the modem and convert it to parallel for transmission over the system data bus.

Although several I/O instructions are sent to this board by the Z-80 CPU, the board also generates internal I/O instructions via the MAR Byte Counter. A complete list of these instructions appears below.

IN'02' - Read TC Status Register
IN'03' - Read TC Interrupt Status Register
IN'04' - Read TC Status Switch SW1

OUT'11' - Select TC Baud Rate
OUT'12' - Clear Keyboard Interrupt When TC Enabled
OUT'13' - Clear 10 msec Timer When TC Enabled
OUT'14' - Select Async/Bisync Clock
OUT'16' - Disable TC Interrupts
OUT'17' - Enable TC Interrupts

The Z-80 CPU uses the following signals to generate any one of the nine possible I/O instructions:

RD - Read
WR - Write
IORQ - I/O Request
M1 - Memory 1 (Fetch) Cycle
A0 - A5 - Address bits by MAR Byte Counter

CHAPTER 3 OPERATION

TABLE OF CONTENTS

CHAPTER 3 OPERATION **Page**

LIST OF ILLUSTRATIONS

Figure **Title** **Page**

CHAPTER 3

OPERATION

3.1 INTRODUCTION

This chapter describes the operating controls and indicators associated with the Archiving Workstation. Section 3.2 deals with the Terminal while section 3.3 covers the Archiving Master. Section 3.4 deals with general AWS operation.

3.2 TERMINAL OPERATION

3.2.1 CONTROLS AND INDICATORS

The adjustment controls for the AWS Terminal are located on the front (5506) bottom (5730) and rear of the cabinet. The function and location of each control is defined below.

Front Panel Controls (Refer to Figure 3-1)

- BRIGHTNESS Control (left - 5506)(bottom front - 5730): The BRIGHTNESS control sets the brightness of all displayed characters, affecting normal and highlighted characters e- qually. (The range of this control can be adjusted with the intensity gain control, a service adjustment located at the top of the CRT/CPU PCA. Refer to Figure 4-10.)

- CONTRAST Control (right - 5506)(bottom rear - 5730): The CONTRAST control sets the relative display intensity between normal and highlighted characters.

Rear Panel Controls (Refer to Figure 3-1)

- SPK (Speaker) Control: The SPK control sets the volume of the internal audio prompt.

- CLK (Clicker) Control: The CLK control sets the volume of the keyboard clicker.

- On/Off Toggle Switch: This switch turns power to the Terminal on or off.

- FUSE: The fuse is installed in a knurled-cap holder next to the power cord. To access the fuse, turn the knurled cap counterclockwise. For systems operating on 115V, 60 Hz power, use a 0.6A, slow-blow fuse; for systems operating on 230V, 50 Hz power, use a 3.0A slow-blow fuse.

3.2.2 KEYBOARD

The Terminal is equipped with a variety of keyboards, depending on the model. Nevertheless, the keyboard operations are essentially similar between models and the following discussion covers all three keyboard types, noting areas which are unique to VS or WP/OIS units.

The keyboards feature the conventional typewriter format, cursor control and editing keys, and special function keys. The special function keys are either those normally associated with Wang WP/OIS units or those normally associated with data processing units (Program Function nn keys). Additionally, VS DP and combined Terminals are equipped with a numeric keypad at the extreme right of the keyboard.

The following paragraphs describe the actions associated with each group of keys. For convenience of discussion, the keyboard has been divided into four zones as shown in Figure 3-1.

Zone 1 - Typewriter Keyboard: Similar to a standard typewriter, this zone contains the alphanumeric characters, the special purpose characters such as @ # $ ¢ and the arithmetic operators "+ - * / = ", TAB, GL, RETURN and SHIFT keys which perform the following functions:

- TAB sets the format line zone and advances the cursor through successive zones on the screen to facilitate table creation.

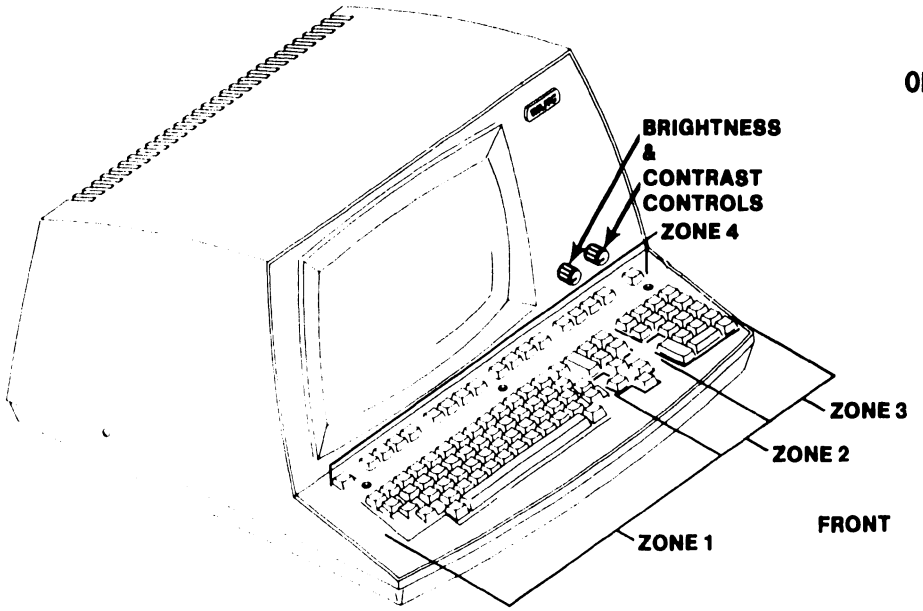
- GL (glossary) is a useful function in Word Processing whereby repeatedly used text may be created once, stored on disk and retrieved again with two keystrokes, GL followed by the glossary number.

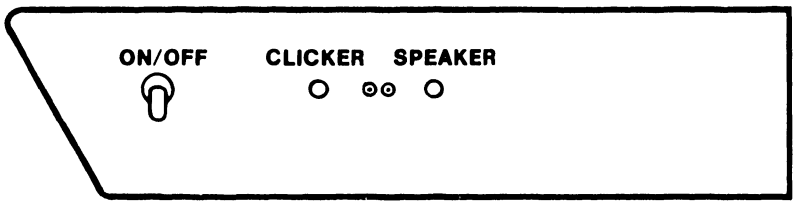
- RETURN terminates the present text line and repositions the cursor at the beginning of the next line.

Zone 2 - Cursor Control and Editing Keys: This zone contains editing keys (INSERT and DELETE), location keys (NEXT SCRN and PREV SCRN), and cursor control keys which control movement of cursor in the indicated direction, up, down, right, and left.

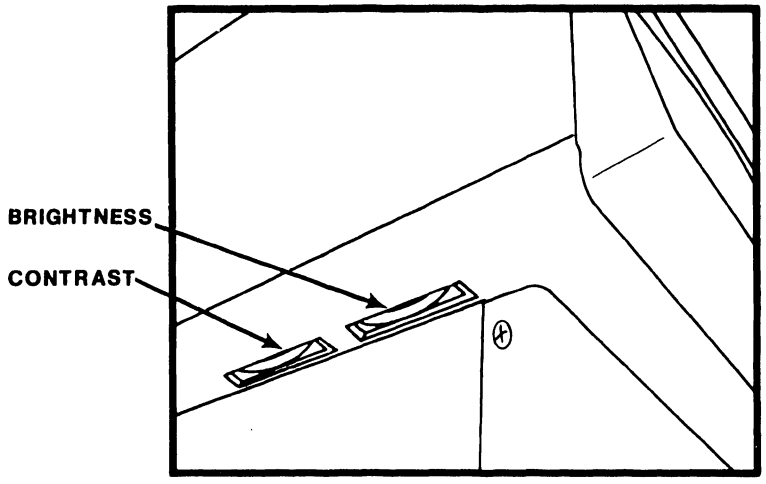
Zone 3 - Numeric Keypad: Provided as standard on the VS Terminal but optional on the WP/OIS Terminal, the numeric zone is a standard 10-key numeric pad for rapid entry of numeric characters. The numeric keys are grouped here for convenience. Digits can be entered by using the numeric keys in either the numeric or the alphanumeric zone.

Zone 4 - Special Function Keys: Across the top of the keyboard are 16 Special Function keys. On the WP/OIS Terminal, or the VS combined Terminal, these keys provide the special word processing functions which simplify document creation and revision. For example, the CENTER key automatically centers a line of text, the MOVE key allows any amount of consecutive text to be moved within a document, and the REPLC key allows a character-defined sequence to be

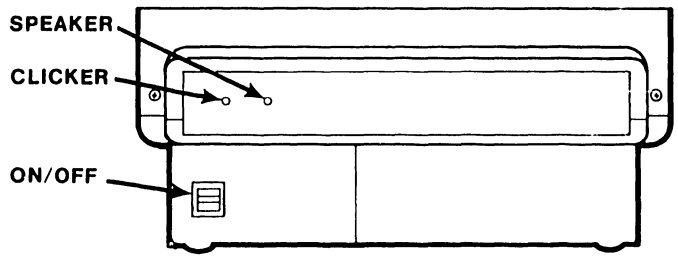




REAR
5506 TERMINAL



NOTE: KEYBOARD LAYOUT FOR THE 5730 DETACHABLE KEYBOARD IS THE SAME AS THE 5506 KEYBOARD AS SHOWN ABOVE.



REAR

5730 TERMINAL

B-02469-FY85-6

Figure 3-1 Controls and Indicators - AWS Terminals

replaced with another within a document. For data processing, these keys can call up any of 16 special Program Functions (PF1 through PF16).

The Terminal also includes a Caps Lock feature. Caps Lock (activated by pressing the LOCK key) produces uppercase alphabetic characters as well as the special characters located on the numeric keys.

The keyboard allows characters to be underlined. On non-English versions of the keyboard, characters can also be accented. Some keys on the keyboard will repeat if held down. Any key can be made to repeat by holding down one of the cursor direction keys before pressing and releasing the key to be repeated. The microprocessor in the workstation automatically adjusts the repeat key rate according to the rate at which characters are being echoed to the CRT. The keyboard clicker sounds each time the repeated character is transmitted. Thus, both aural and visual evidence of the repeated character are given to the user. (The repeating key is particularly useful for moving the cursor when editing.)

Special features of the Terminal keyboards include the following:

- Keyboard Clicker: The clicker provides an audio response when a key is sufficiently pressed. The volume of the keyboard clicker can be adjusted.

- N-Key Rollover: This feature permits a new key to be pressed and output to the workstation while a previous key is still being held down. This process can continue for any number of keys; each new key pressed takes precedence over any keys already held down. The N-key rollover feature helps eliminate errors during high-speed typing.

- Audio Prompt: The prompt provides audio feedback to indicate the occurrence of errors or special conditions, e.g., pressing an undefined special function key, typing beyond a specified field, displaying an error message. The volume of the audio prompt can also be adjusted.

3.3 ARCHIVING MASTER OPERATION

REAR PANEL CONTROLS (Refer to Figure 3-2)

- ON/OFF Power Rocker Switch: When the ON/OFF power switch is in the ON position (upper half depressed), electrical ac-power service is supplied to the Archiving Master.

- FUSE: The fuse is installed in a knurled-cap holder next to the power cord. To access the fuse, turn the knurled cap counterclockwise. For systems operating on 115V, 60 Hz power, use a 3.0A fuse; for systems operating on 230V, 50 Hz power, use a 1.5A fuse.

FRONT PANEL CONTROLS AND INDICATORS (Refer to Figure 3-2)

- Disk Drive Door Release: When the Disk Drive door is closed, pressing this button causes the door to open, popping any diskette mounted in the drive to its released position. On the VS AWS (SA 850/851 Disk Drive) and newer models of the WP/OIS AWS (SA 901 Disk Drive), a red LED indicator in this pushbutton lights when the door is closed. Also, an automatic latching mechanism locks the door shut, preventing re- moval of the disk while it is being accessed (whenever the heads are loaded).

  Older models of the WP/OIS AWS (SA 901 Disk Drive) do not have the activity light on the door release pushbutton or the automatic latching feature.

- Disk Drive Activity Indicator: This is a red LED indicator located at the bottom edge of the unit, closest to the Disk Drive door. On the WP/OIS AWS, it is normally lit to indicate power on and is extinguished during diskette read or write operations.

  On the VS AWS, this LED is lit to indicate power on but goes out whenever the Disk Drive door is closed.

- WP/OIS Bootstrap Button: This is a recessed red pushbutton located to the right of the Disk Drive Activity Indicator. On the WP/OIS AWS, pressing this button causes the workstation to re-IPL from the Master CPU.

- VS AWS Bootstrap Button: This is a recessed red pushbutton located to the right of the Disk Drive Activity Indicator. On the VS AWS, it loads microcode from the internal Bootstrap PROM into memory to enable the VS AWS to read diskettes.

  The purpose of the VS bootstrap operation is to allow the CE to start a VS System from the VS AWS itself. The bootstrap also allows an IPL from the VS AWS Disk Drive in case it is not possible to do so from the system disk because of a disk drive or interface problem. To eliminate the possibility of an unintentional bootstrap, VS AWS systems are presently being built with this button either disconnected or completely left out of the unit even though the access hole may still be there as shown in Figure 3-2. The details of bootstrap operation are presented in Appendix B.

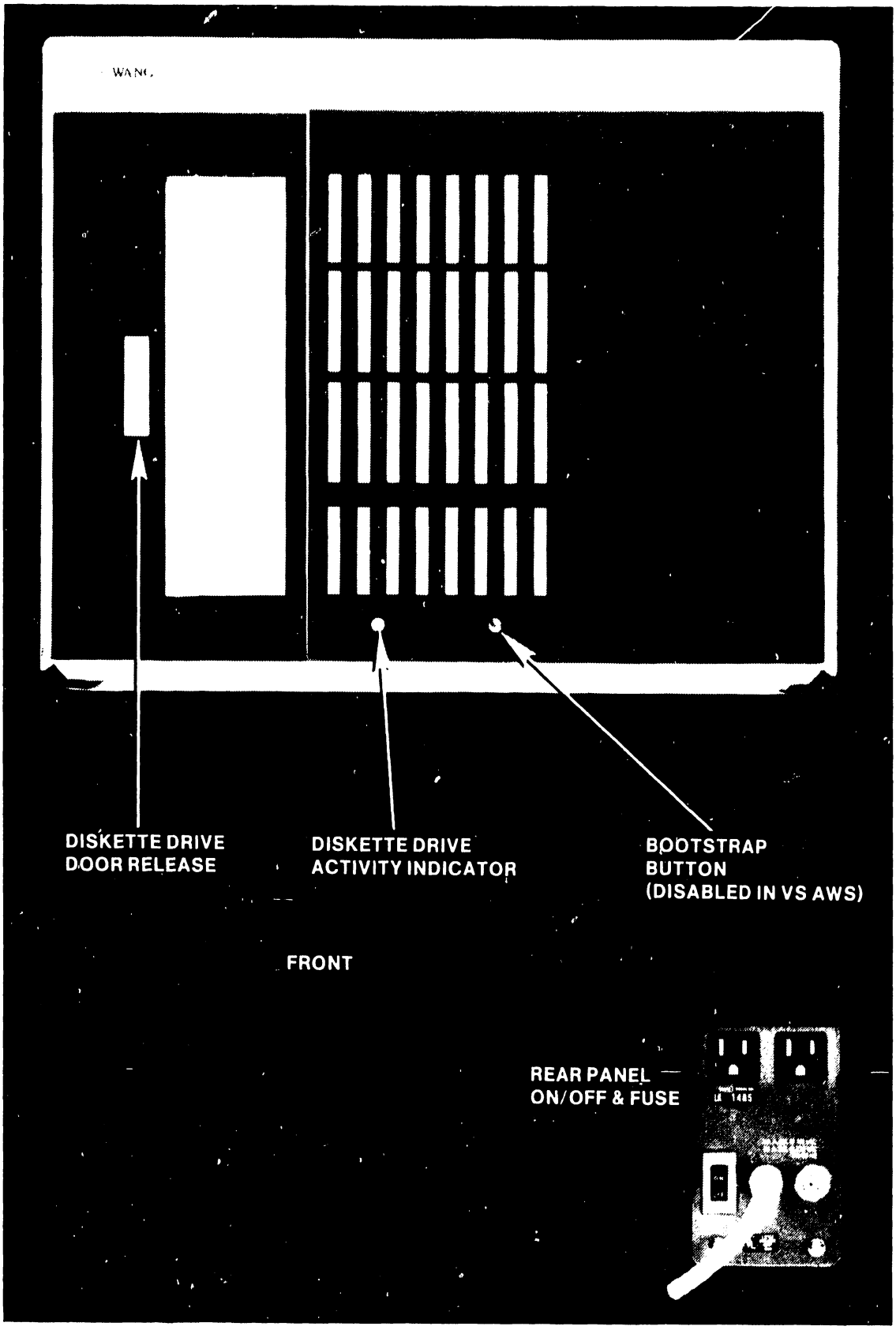


Figure 3-2 Archiving Master Controls and Indicators

3.4 AWS OPERATION

3.4.1 TURN ON

To turn on the AWS, simply set both the Archiving Master unit and Terminal power switches ON.

3.4.2 PERFORMANCE VERIFICATION

Performance verification can be accomplished in two ways, by use of normal system operating procedures or by running the appropriate system diagnostics.

Refer to section 1.3.3 for available diagnostics for the VS and WP/OIS systems.

To verify operation through normal system operating procedures, turn the AWS on per 3.4.1 above and verify that the Terminal's BRIGHTNESS and CONTRAST controls function correctly. Refer to the applicable WP/OIS/VS operator guide; verify that all keys and special keys produce the correct results.

For the WP/OIS AWS and VS AWS with word processing capability, the following tests can be performed to determine if the AWS is functioning normally:

1. Create a new document.

2. Edit a document by:

   a. supercopying text from another document
   b. super global replacing words contained within the text
   c. deleting words in the text

3. File document to archive diskette.

4. Retrieve document from archive diskette.

5. Delete document from archive diskette.

6. Delete document from library.

7. Go to step 1 and repeat procedure once.

In the VS AWS equipped with soft-sector capability, exercise the DISKINIT, DMS and/or IBMCOPY utilities to determine proper operation of these features.

If the AWS fails during normal operational checkout, refer to Chapter 8 of this manual.

CHAPTER 4

INSTAL-LATION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER 4

INSTALLATION

This chapter contains information required to properly install the VS/WP/OIS Archiving Workstation.

4.1 INSTALLATION SITE CHECK

4.1.1 ENVIRONMENTAL

The environment in which an AWS operates can greatly affect its performance. Considerations of temperature, humidity and cleanliness are discussed below.

4.1.1.1 Temperature Considerations

The recommended operating temperature range for the AWS is from 60°F to 80°F (15°C to 27°C), but a range from 50°F to 90°F (10°C to 32°C) is allowable. Since nearly all locations are heated, low outside temperatures are usually not a problem. High temperatures can be a problem, however, in locations that do not have air conditioning. If the system is used where temperatures exceed the maximum specified, component failure rates will drastically increase, resulting in costly downtime.

High temperatures can also cause warping and distortion of data-storage material, resulting in lost data. If an air conditioning unit is already installed or if one is to be installed, such equipment must be powered on a power line separate from the one connecting to the AWS unit. If separate power is not used, data errors can occur when the air conditioner is in use.

Air conditioning also removes moisture and dust from the air by lowering the humidity. Lower humidity levels along with static build-up from carpets and synthetic clothing can impart a static electrical charge on operating personnel. When the operator comes in contact with the unit, the resultant static discharge can cause unit failures and/or destruction of recorded data.

4.1.1.2 Humidity Considerations

The recommended relative-humidity range is from 35% to 65%. Humidifiers or dehumidifiers should be installed to increase or decrease the humidity as required. If carpeting is to be installed, be sure it is a non-static variety. If carpeting already exists which is not of the non-static type, it will either have to be treated with a non-static spray or an electrically conductive mat must be installed to prevent a static charge build-up. Carpets treated with non-static spray should be thoroughly cleaned before the first treatment, and they should be retreated at least once every three months

thereafter. If an electrically conductive mat is used, it should be installed under the unit's operating area and must be properly connected to an earth ground.

4.1.1.3 Cleanliness Considerations

Dust can accumulate rapidly within the AWS since it contains no air filters. Dirt and grease form a film that prevents proper heat dissipation from components and can also create a leakage path for signals. To prevent this type of failure, all air conditioning, heating and ventilating units should have air filters installed; these filters should be cleaned or replaced regularly.

4.1.2 ELECTRICAL SERVICE CONSIDERATIONS

The AWS is designed to operate domestically with a 115V, 60 Hz power source, or internationally with a 230V, 50 Hz power source. Refer to Table 1-6 or 1-7 for power requirements for either the VS or WP/OIS AWS.

The source outlet should not be electrically connected to other equipment capable of generating voltage fluctuations on the power line (such as paper shredders, electrical stamp machines/staplers, coffee makers, etc.) Both the Archiving Master and the Terminal are outfitted with three-wire power cords, designed for connection to a standard grounded outlet. The ground pin of the line cord is connected to the chassis of the associated unit to protect operating personnel from electrical shock.

4.1.3 EQUIPMENT POSITIONING

Equipment positioning is limited only by the following cable lengths:

- A maximum of 2000 feet from the Archiving Master to the Master CPU.
- A maximum of 50 feet between the Archiving Master and the Terminal. Note that the standard cables supplied with the AWS only allow for the two units to separated by eight feet. Part numbers for longer cables available for interconnecting the two units are given below.

Cable Type	Length (ft.)	Part Number
Video	25	220-0139
Keyboard	25	120-22VS-2
Video	50	120-2292-50
Keyboard	50	120-22VS-5

Other than the above considerations, no special requirements apply with respect to equipment positioning except for common-sense considerations of operator convenience and non-interference with traffic flow.

4.2 UNPACKING AND INSPECTION

4.2.1 INSPECTION UPON ARRIVAL

When the equipment arrives, immediately locate the packing slip and note the work order number. Verify the equipment model and serial number as listed on the packing slip.

Before opening the container, inspect it carefully for signs of damage (crushed edges, puncture holes, tears, etc.) If damage is noted, promptly notify the appropriate carrier.

4.2.2 UNPACKING

4.2.2.1 Terminal

All models of the AWS except the 5740 come packaged in two containers, one for the Terminal and one for the Archiving Master. Figure 4-1 shows the method used to pack the Terminal. The 5740 comes packed in three containers, one for the Archiving Master, one for the Terminal and one for the Keyboard. Use the following procedure to unpack the Terminal.

1. Carefully cut the sealing tape and open the top of the shipping container.

2. Roll the container so that the open top rests on the floor or a table.

3. Lift the container off of the Terminal.

4. Remove the fitted packing covers from both sides and the front of the Terminal.

5. Remove the plastic bag from around the Terminal.

6. Remove cardboard flaps and tape from the top and front of the Terminal.

7. If the Terminal is a model 5730, remove the Keyboard from the container.

Save all packing material until the AWS has been found to perform satisfactorily.

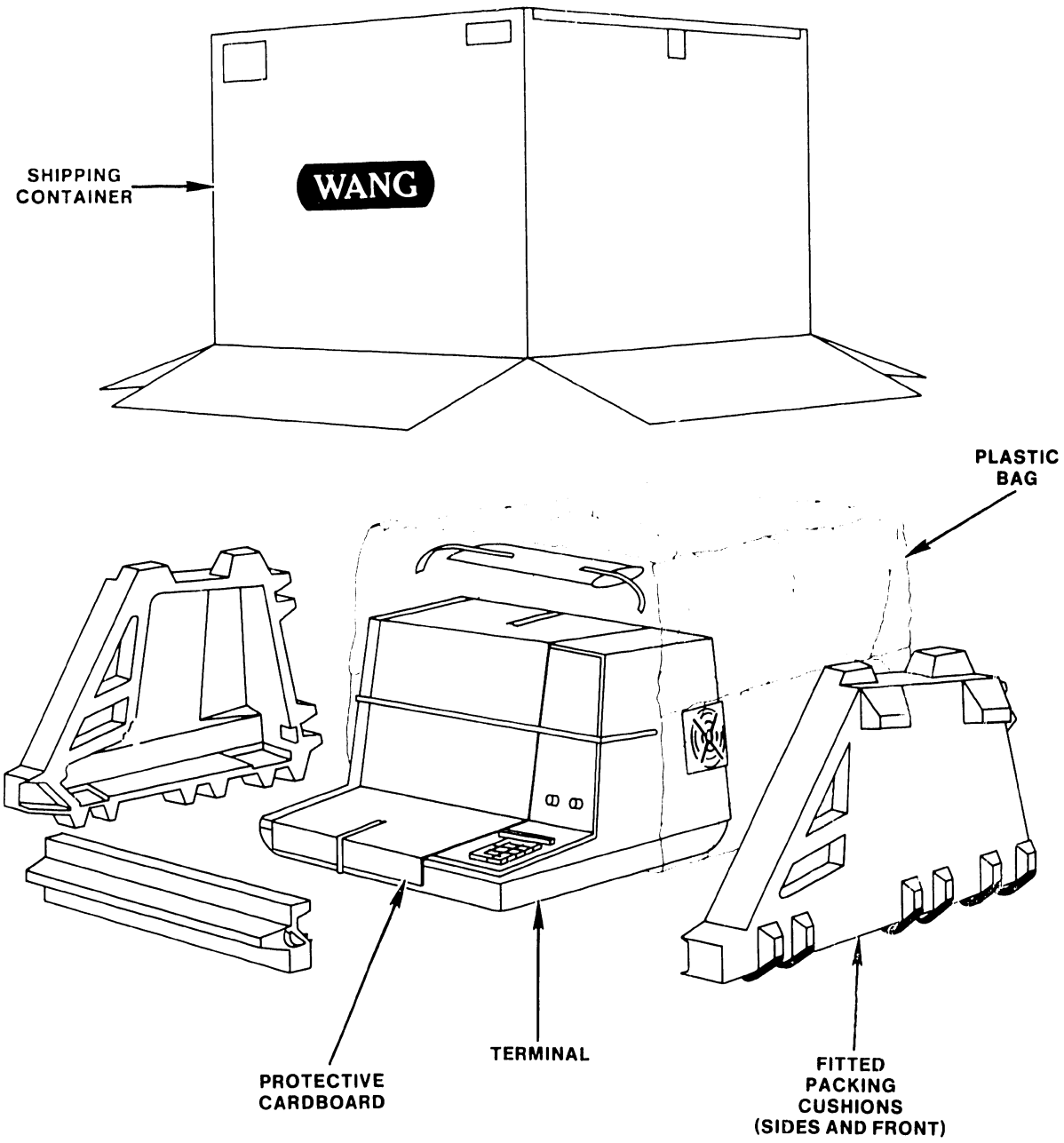


Figure 4-1 Unpacking the Terminal

4.2.2.2 Archiving Master

The Archiving Master may be packed one of two ways, depending on its place of manufacture. Figure 4-2 shows method "A" which can be identified by the plastic bands strapped around the shipping container. Use the following method to unpack Archiving Masters packed according to this method.

1. Place the container on the floor with the arrow pointing up.

2. Cut the plastic shipping bands and lift the upper half of the container off of the unit.

3. Remove the top cushion assembly.

4. With the help of another person, lift the Archiving Master out of the bottom tray.

Save all packing material until the AWS has been found to function satisfactorily.

Figure 4-3 shows alternate packing method "B" which can be indentified by the sealing tape used to to seal the shipping container. Use the following method to unpack Archiving Masters packed according to this method.

1. Place the shipping container on the floor with the top up.

2. Carefully cut the sealing tape securing the flaps of the shipping container and open the container.

3. Remove the top fitted packing cushion.

4. With the help of another person, lift the Archiving Master out of the shipping container.

5. Remove the plastic wrapping from around the unit.

Save all packing material until the AWS has been found to function satisfactorily.

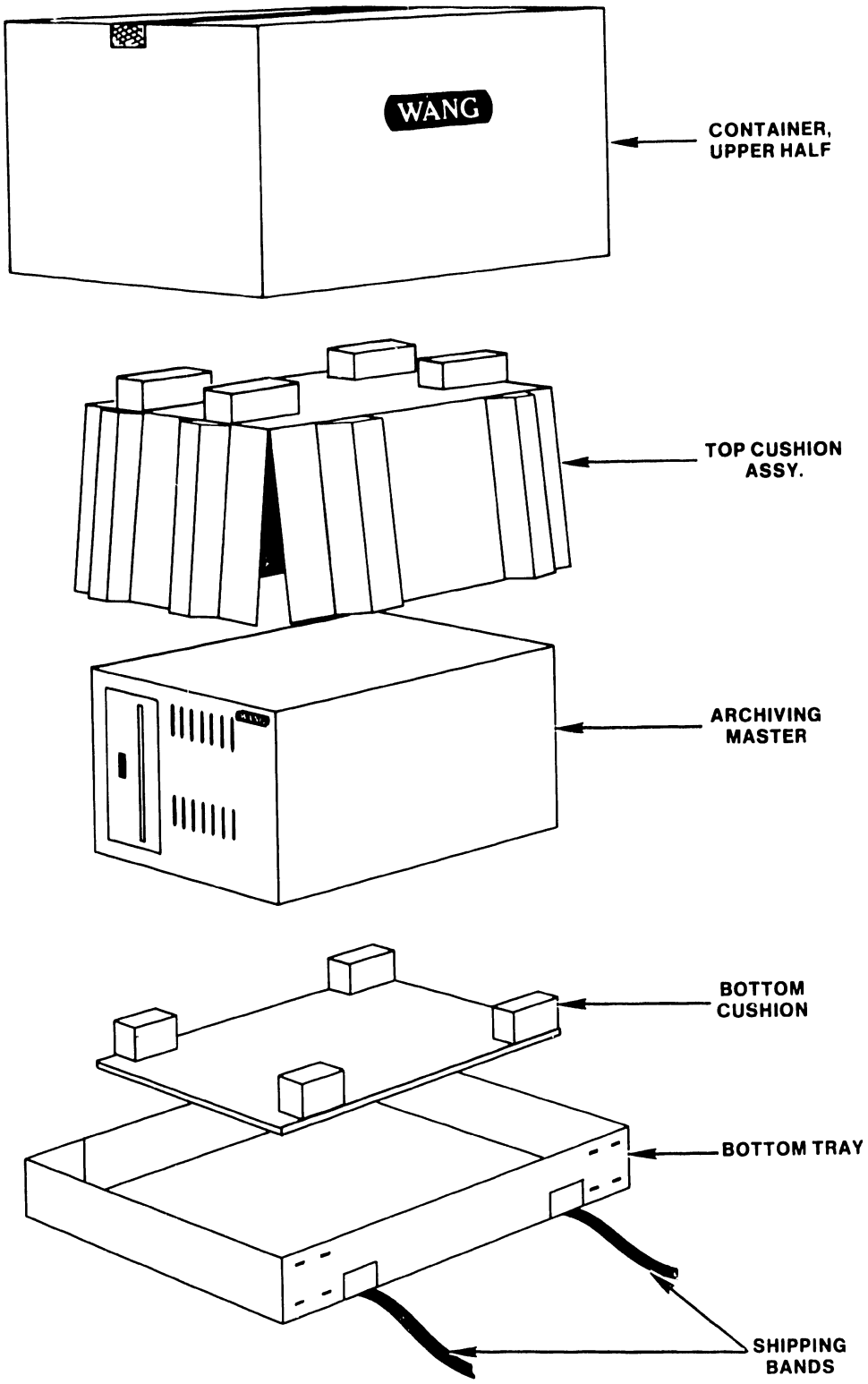


Figure 4-2 Unpacking the Archiving Master
(Method A)

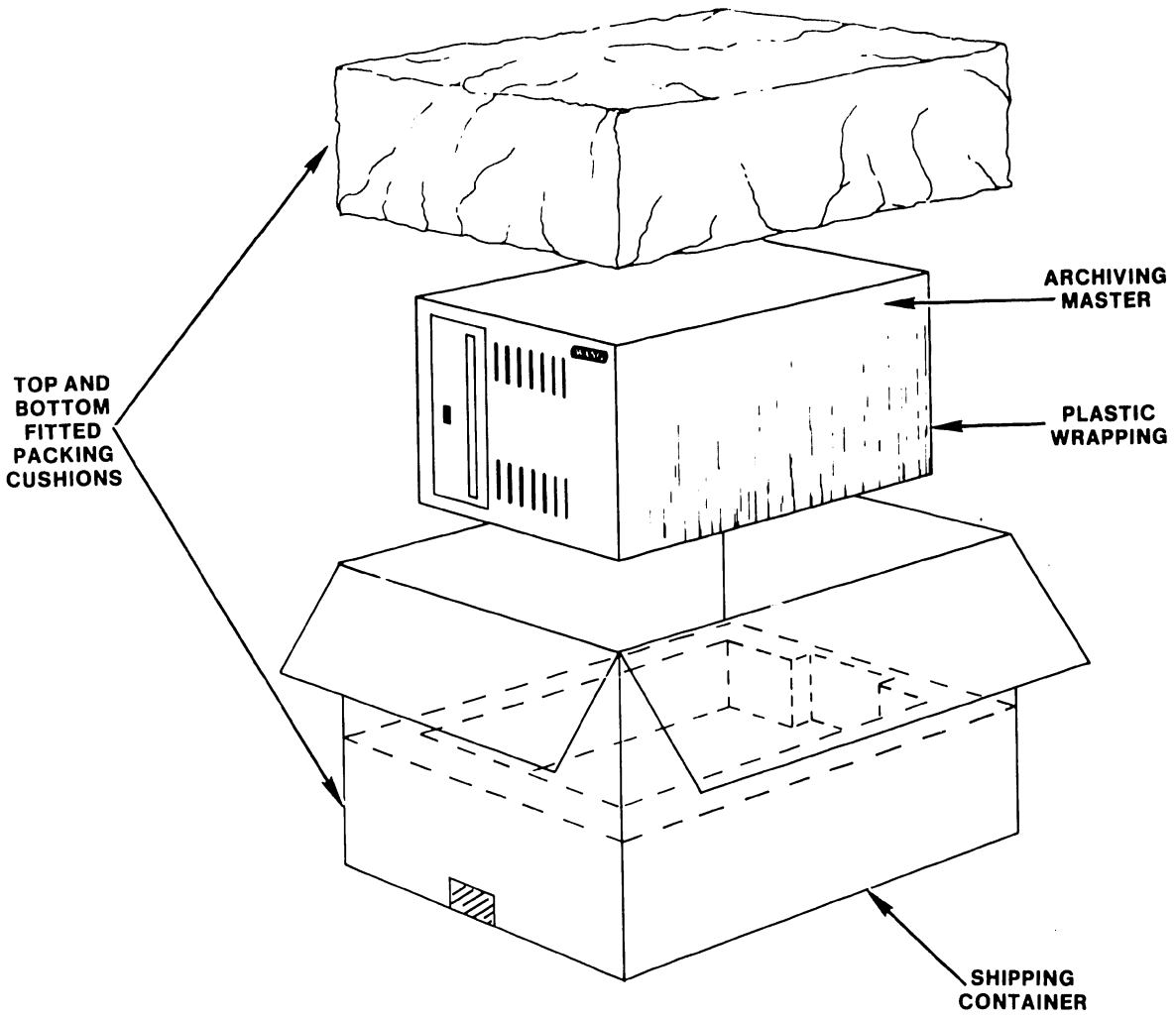


Figure 4-3 Unpacking the Archiving Master
(Method B)

4.3 INSTALLATION

The following subsections detail the installation procedure for the AWS:

4.3.1 REMOVING AWS COVERS

In order to make the inspections and switch settings required during installation, use the following procedures to gain access inside both the Archiving Master and the Terminal.

4.3.1.1 Gaining Internal Access to the Terminal

4.3.1.1.1 Model 5506

1. Referring to Figure 4-4, remove three screws located under plastic strip on keyboard and remove keyboard cover plate.

2. Remove one screw from each side of Terminal near lower edge of cover.

3. Lift cover up and away from Terminal; take care not to hit or nick CRT, or strain BRIGHTNESS/CONTRAST control wires.

4. Grasp the locking tabs of the BRIGHTNESS/CONTRAST control harness connector and press inward toward the harness to release the connector. Simultaneously pull the connector from its socket. Lay cover on its side next to Terminal.

4.3.1.1.2 Model 5730

1. Referring to Figure 4-4, remove two screws located on each side of the rear of the Terminal.

2. PLace both hands on the top of the Terminal, push the cover back along the side tracks, and lift it from the unit.

4.3.1.2 Gaining Internal Access to the Archiving Master

1. Referring to Figure 4-5, remove six screws (three each side) securing the cover to the Archiving Master.

2. Remove cover.

3. Remove two screws securing the Printed Circuit Assembly (PCA) hold-down brackets and remove the brackets.

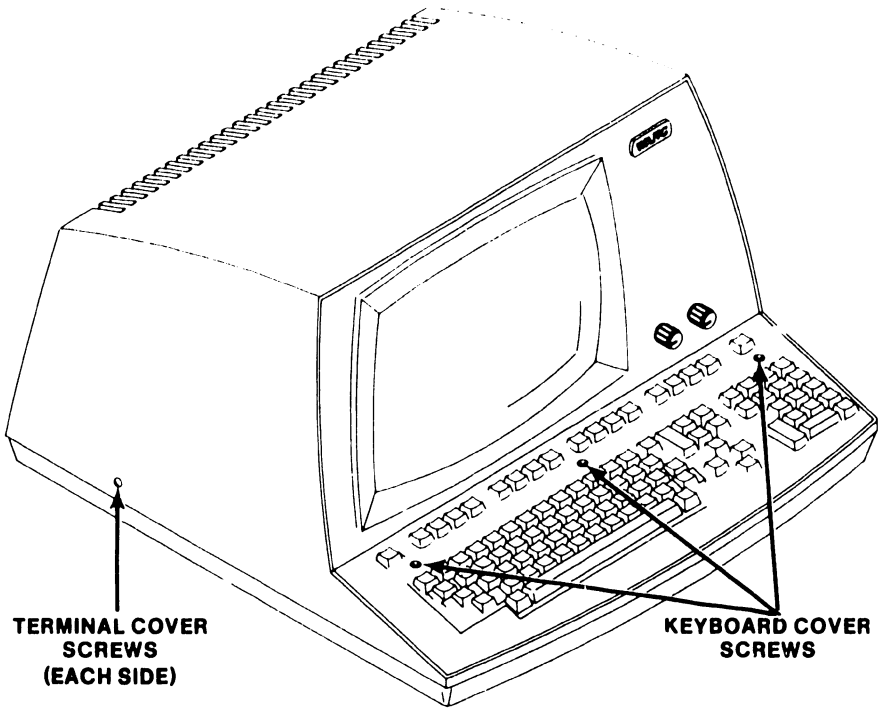


Figure 4-4 Terminal Cover Removal

(show three side screws, ref to other side)

Figure 4-5 Removing the Archiving Master Cover

4.3.2 PRE-INSTALLATION INSPECTION

The following pre-installation inspection of the Archiving Master is recommended:

1. Confirm that the Disk Drive assembly is installed in place and fastened securely to the left (from the front) of the card cage.

2. Manually turn the Disk Drive stepping motor worm gear fully counterclockwise to move heads to outermost track.

3. Push door-release pushbutton to pop cardboard shipping disk separating opposing heads of the Disk Drive (Shugart 850/851 only). Save the shipping disk for any future system relocation by storing it inside the Archiving Master, in the empty space to the right of the card cage.

4. Confirm that the power supply transformer (mounted next to the Power Supply Regulator card on the right wall of the card cage) matches the available power service and that the correct fuse is installed: (Refer to Figure 4-6)

Power Service	Required Transformer	Fuse
115V/60 Hz	P/N 410-0111	2.5A slow-blow
230V/50 Hz	P/N 410-0113	1.5A slow-blow

5. Verify that the cables associated with the Disk Drive are all plugged securely into their proper connectors. These connections include the I/O cable connection on the Motherboard, the ac power connection at the rear of the Disk Drive and the dc power harness also at the rear of the Disk Drive. These connections are shown in Figures 4-6 and 4-7.

4.3.3 TERMINAL SWITCH SETTINGS

The 12-inch monitor Power Supply in the Terminal is switchable for either 115/60 Hz ac power or 230V/50 Hz ac power. Referring to Figure 4-8, set the switch to match the ac power available at the installation site. Also, check that the ac power fuse is the correct value for the ac power input as follows:

Power Service	Fuse
115V/60 Hz	0.6A slow-blow
230V/50 Hz	3.0A slow-blow

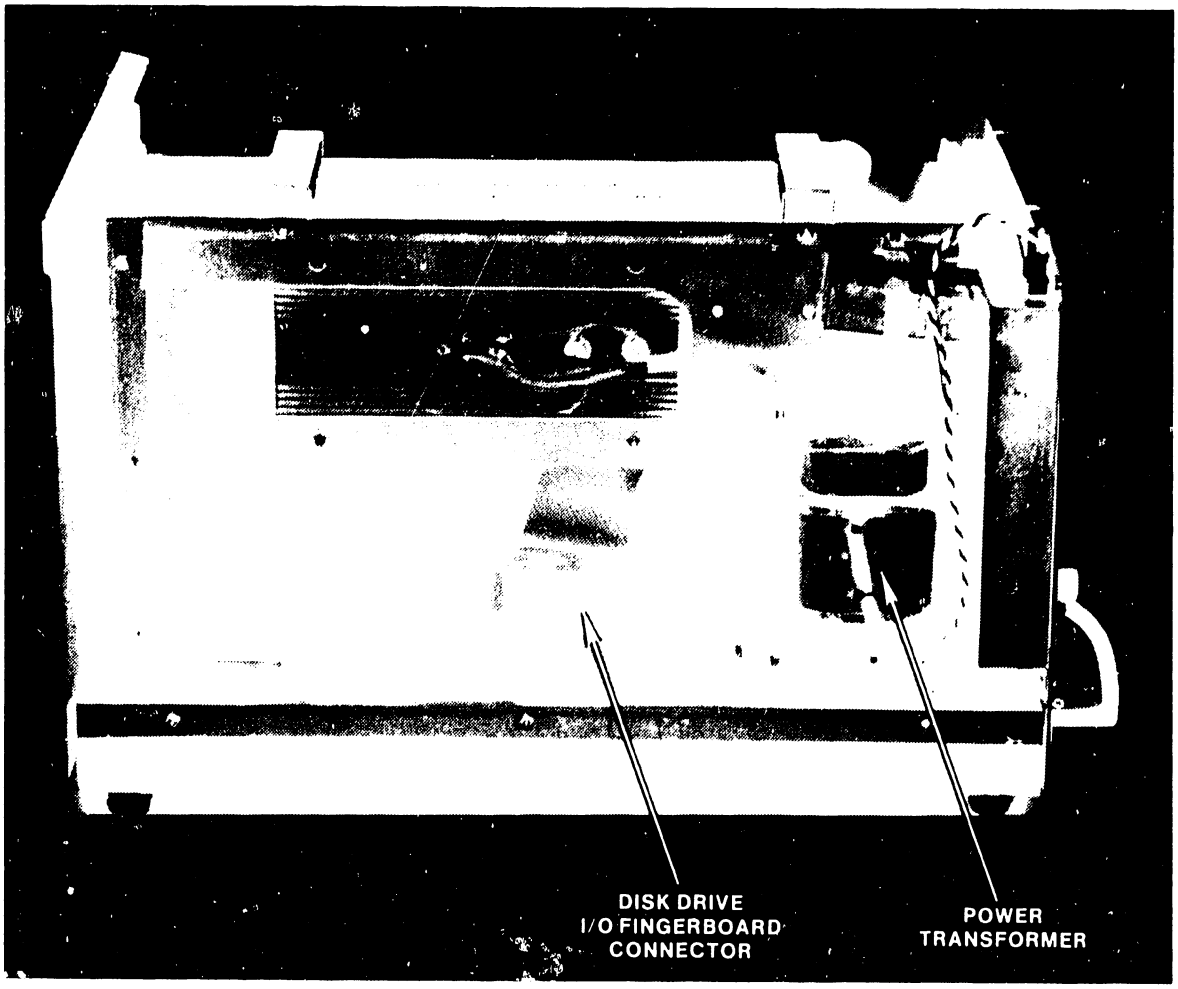


Figure 4-6 Power Transformer and Disk I/O Connection at Motherboard
(Archiving Master)

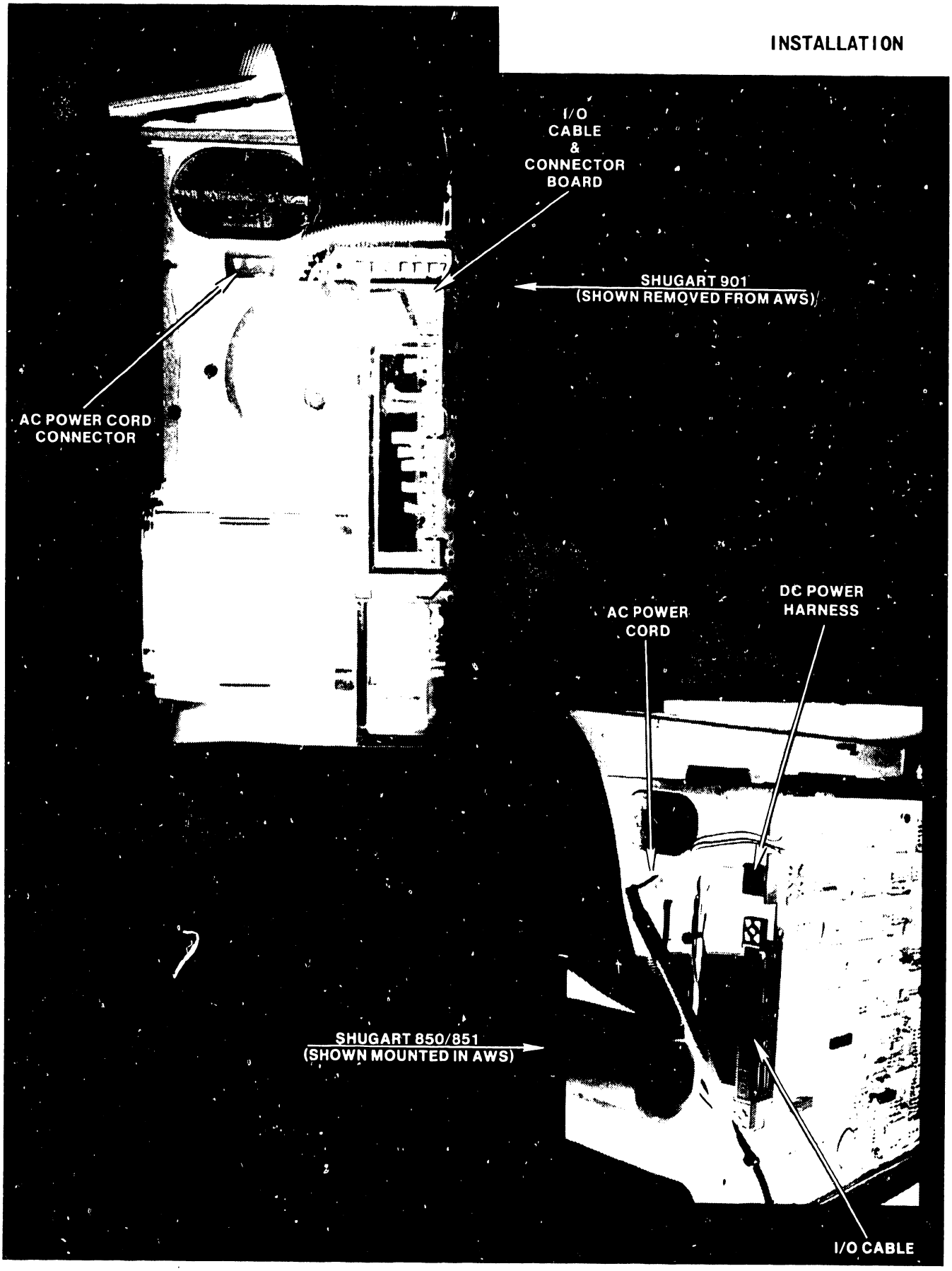


Figure 4-7 Disk Drive Cable Harness Connections
(Archiving Master)

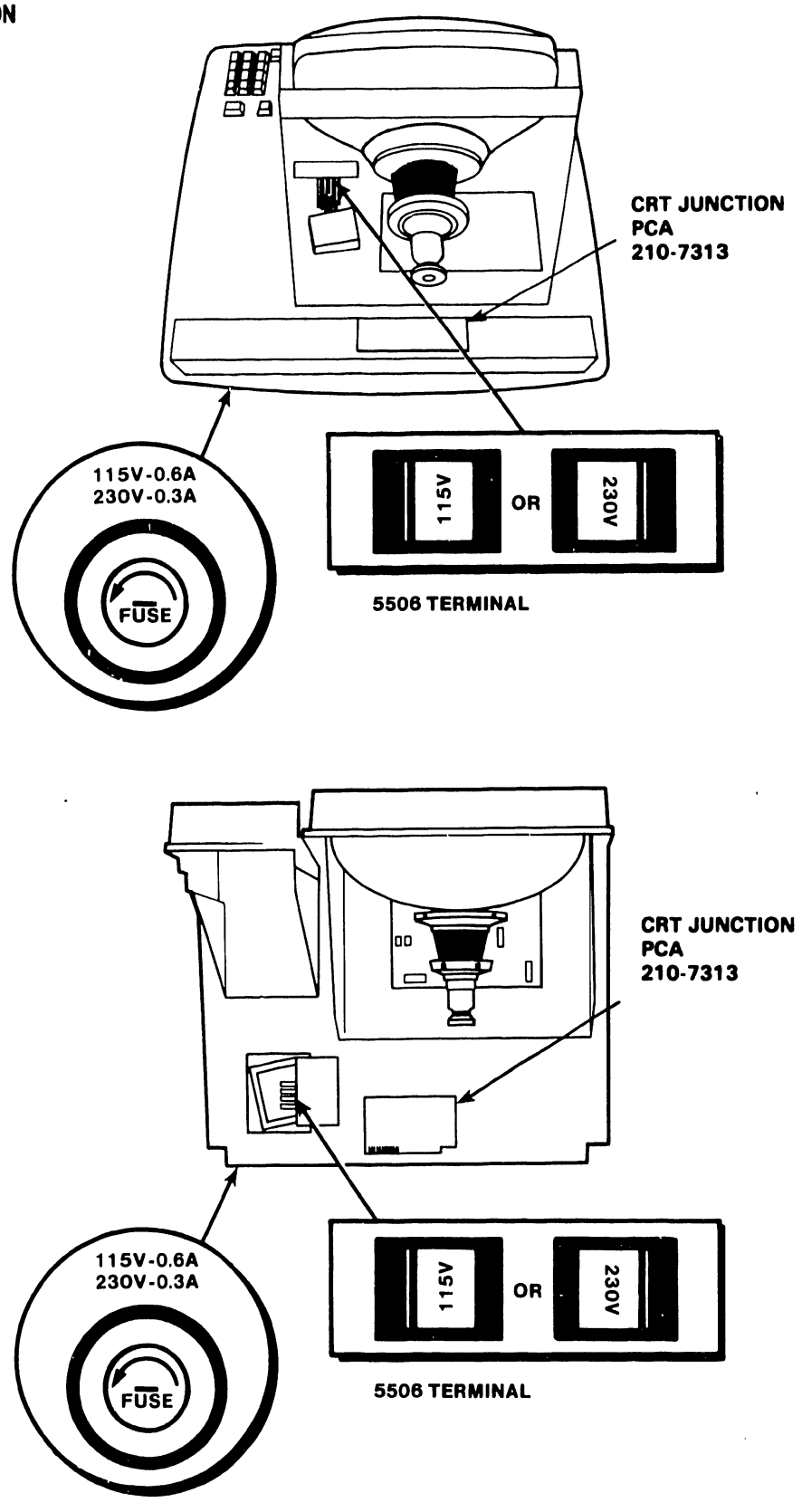


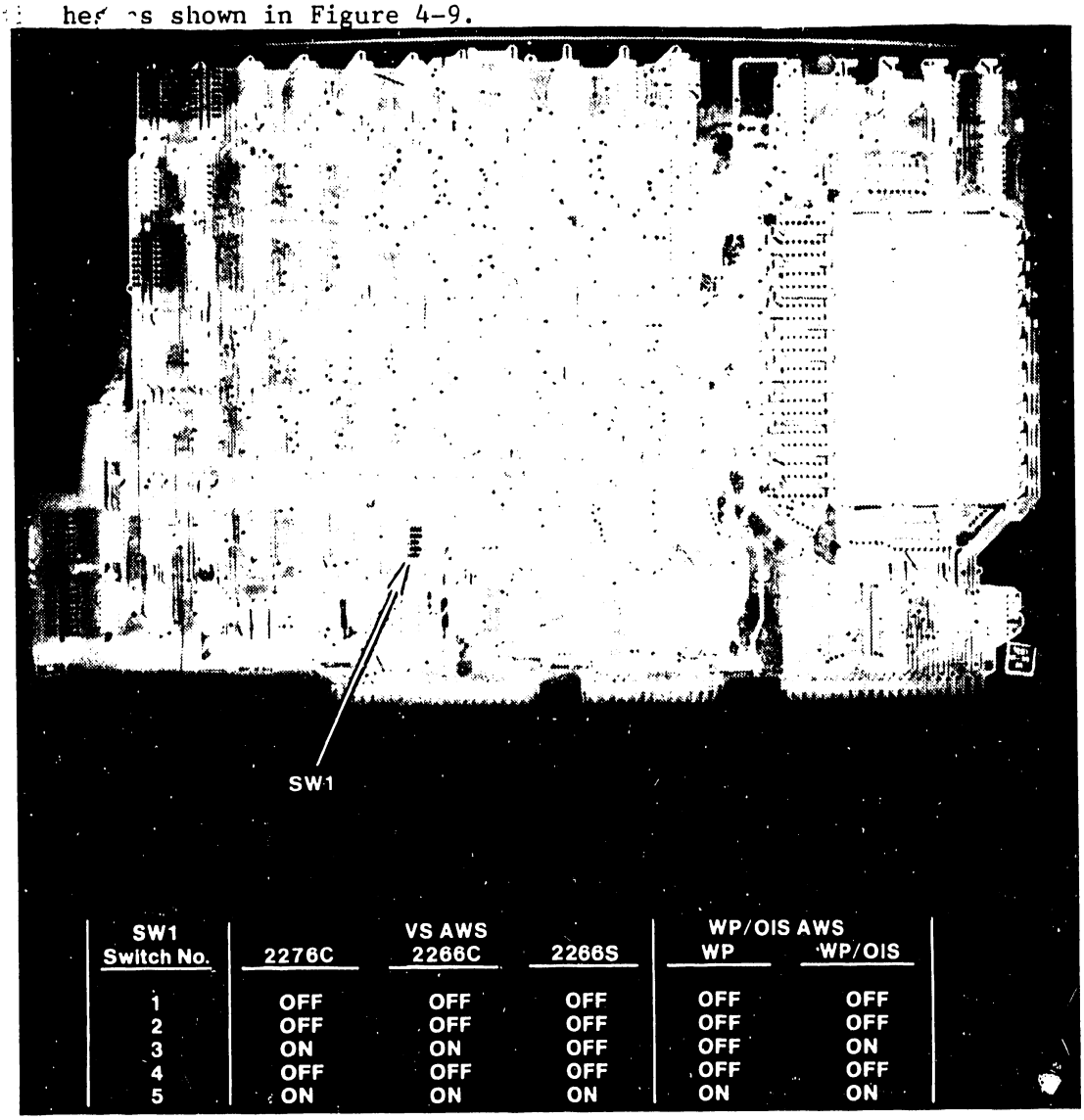
Figure 4-8 115V/230V Switch Setting, Monitor Power Supply (Terminal)

4.3.4 ARCHIVING MASTER SWITCH SETTINGS

Switch settings on boards within the Archiving Master are required to inform the host system of the type of peripheral device that is connected as well as other information vital to the correct operation of the AWS. Remove the PCAs from the Archiving Master and make the switch settings as detailed in the following subsections.

4.3.4.1 Data Link Memory PCA

The Data Link Memory PCA (210-7544/7744) contains a dual inline package (DIP) switch in the L107 logic location. The host system reads the settings of this switchbank whenever it executes an IN'07' command. Set the individual he[illegible]s shown in Figure 4-9.



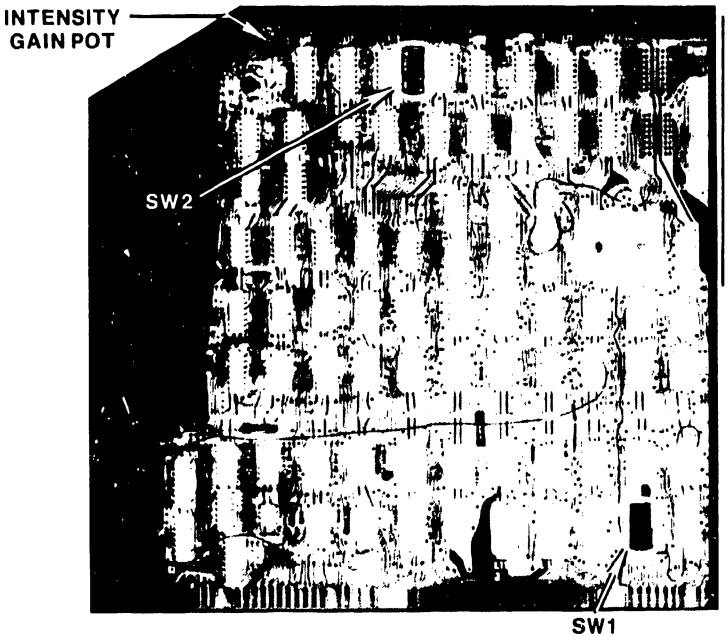
SW1 Switch No.	VS AWS 2276C	VS AWS 2266C	VS AWS 2266S	WP/OIS AWS WP	WP/OIS AWS WP/OIS
1	OFF	OFF	OFF	OFF	OFF
2	OFF	OFF	OFF	OFF	OFF
3	ON	ON	OFF	OFF	ON
4	OFF	OFF	OFF	OFF	OFF
5	ON	ON	ON	ON	ON

Figure 4-9 Data Link/Memory PCA Switch Settings

4.3.4.2 CRT/CPU PCA (Refer to Figure 4-10)

The CRT/CPU PCA (210-7545-A, C, D) contains two DIP switchbanks which must be set according to the AWS configuration. Switch SW1 provides the Master CPU with information about the workstation and the options that it contains. Set the individual switches as shown in Figure 4-10. Figure 4-10 also defines the meaning of each switch state in the SW1 switchbank.

SW2 on the CRT/CPU PCA is set to select the scan logic for different ac input power frequencies. Domestically, the AWS operates with 115V/60 Hz input power while internationally it operates with 230V/50 Hz input power. Set the individual SW2 switches as shown in Figure 4-10. The switch settings are the same for all models of the AWS.



SW2 Switch No.	Domestic Power 115V/60 Hz	International Power 230V/50 Hz
1	OFF	ON
2	OFF	ON
3	OFF	ON
4	OFF	OFF
5	OFF	OFF
6	ON	OFF
7	ON	OFF
8	ON	OFF

SW1 Switch No.	VS AWS 2276C	VS AWS 2266C	VS AWS 2266S	WP/OIS AWS WP	WP/OIS AWS WP/OIS	COMMENTS ON =	COMMENTS OFF =
1	OFF	OFF	OFF	OFF	OFF	TC	NO TC
2	ON	ON	ON	ON	ON	DISK DRIVE	NO DISK DRIVE
3	ON	OFF	OFF	OFF	ON	MEMORY SIZE SEE CHART BELOW	
4	ON	ON	OFF	ON	ON		
5	OFF	OFF	OFF	OFF	OFF	PROP. SPACE	STANDARD
6	OFF	OFF	OFF	OFF	OFF	256 CHAR. PROM	128 CHAR. PROM
7	OFF	OFF	OFF	ON	ON	IN08 ACTIVE	IN08 NOT ACTIVE
8	OFF	OFF	OFF	OFF	OFF	NOT USED	

MEMORY SIZE CHART

SW3	SW4	
OFF	OFF	16K
ON	OFF	32K
OFF	ON	48K
ON	ON	64K

Figure 4-10 CRT/CPU PCA Switch Settings

4.3.4.3 Hard-Sector Controller PCA

The Hard-Sector Controller PCA [210-7843-A (VS) 210-7543-A (OIS)] contains DIP switch SW1 which must be set as shown below and illustrated in Figure 4-11. All switches are OFF in units without the telecommunications option (TC). Units with TC must have switch 2 ON.

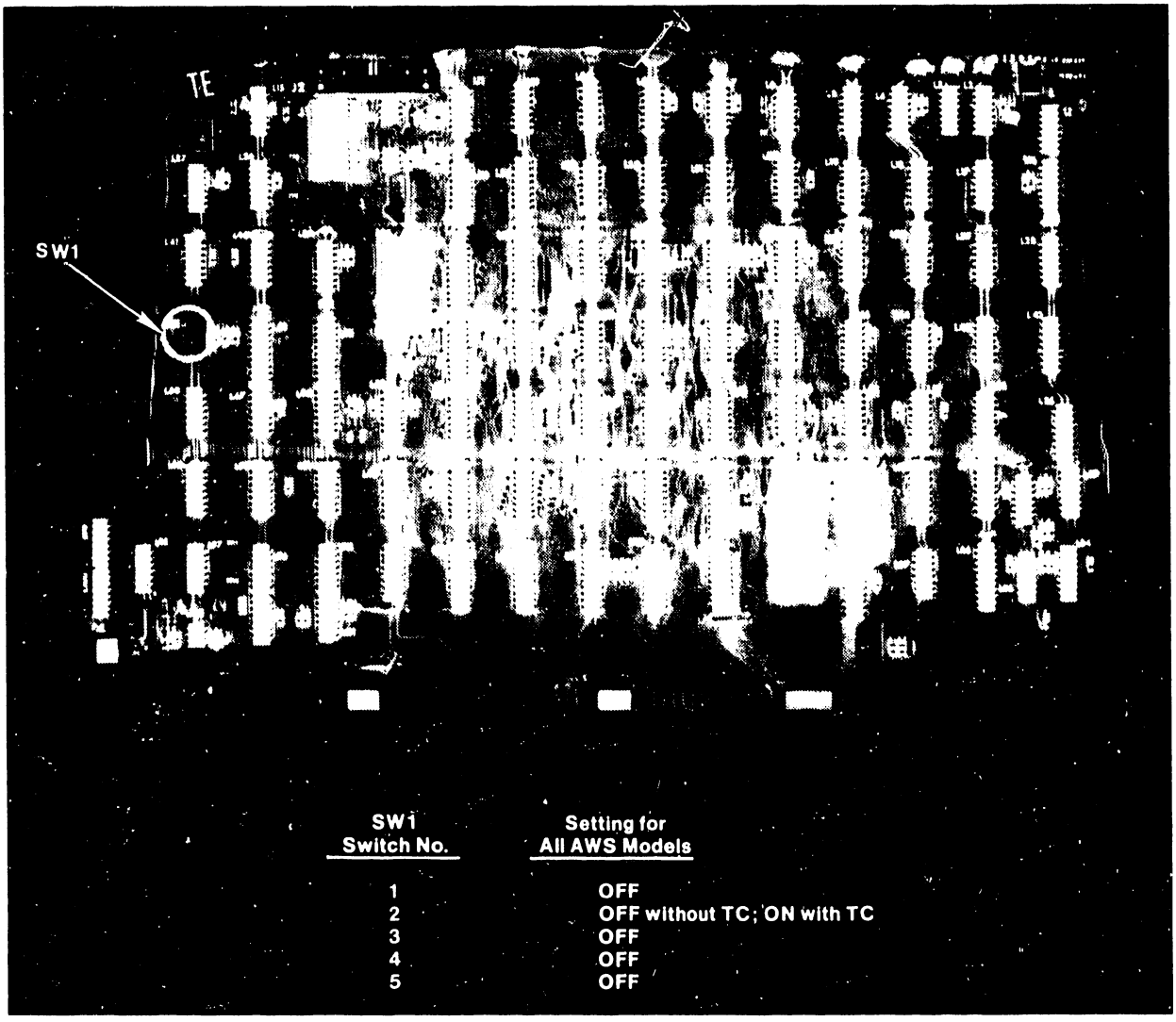


Figure 4-11 Hard Sector-Controller PCA Switch Settings

4.3.4.4 Soft-Sector Controller PCA (Refer to Figure 4-12)

The Soft-Sector Controller PCA (210-7414-A) appears only in certain VS AWS models. (Refer to Table 1-5.) The board contains DIP switch SW1 which must be set as shown below and illustrated in Figure 4-12.

To support the IBMCOPY utility, this PCA must have an NEC 765 AC device (P/N 377-0426) in location L59. The NEC 765 device will not support this utility.

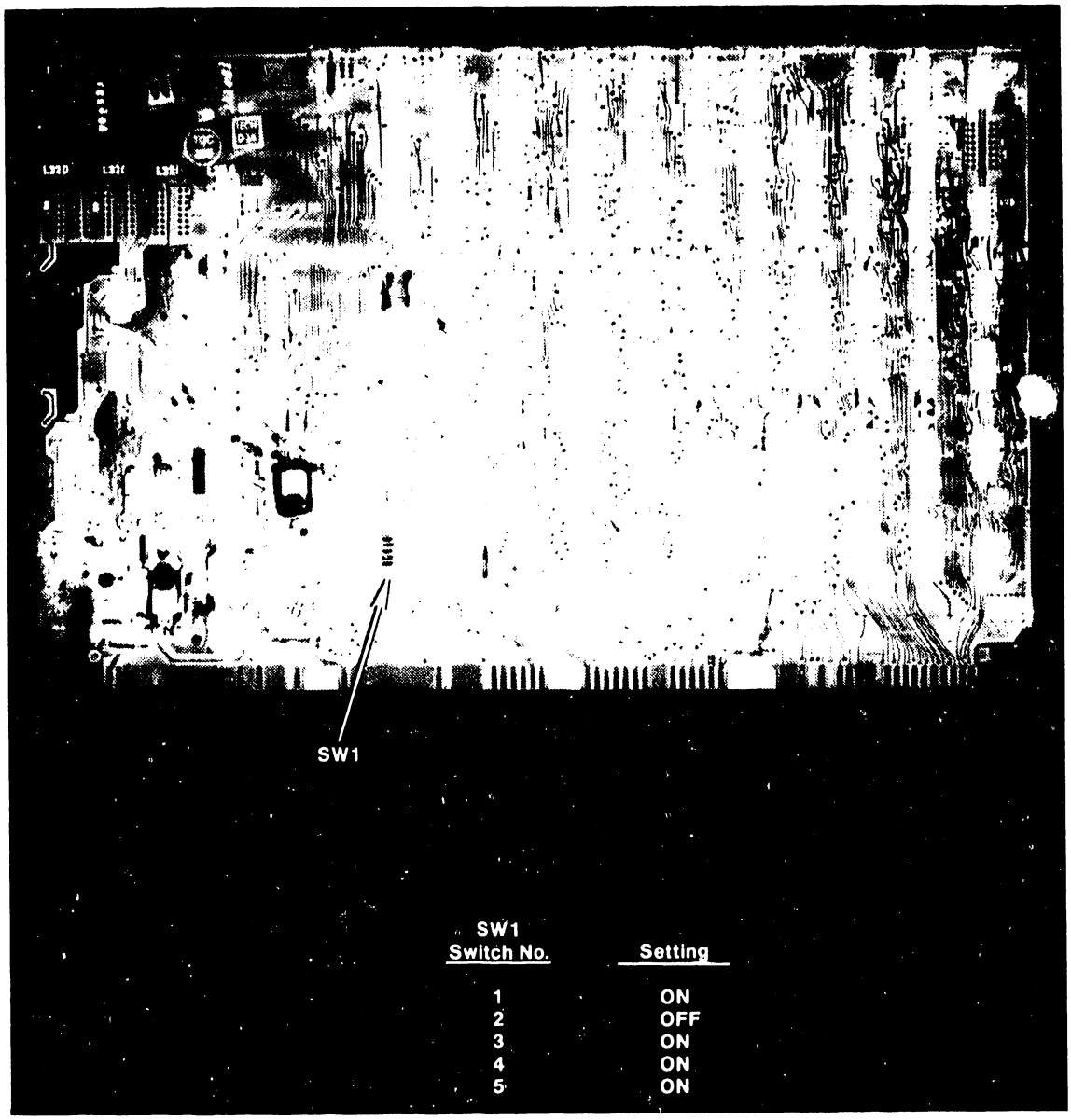


Figure 4-12 Soft-Sector Controller PCA Switch Settings

4.3.4.5 Shugart 850/851 Disk Drive

The circuit board on the Shugart 850/851 Disk Drive contains jumpers which are set at the factory for proper operation with the VS AWS. These jumpers should not be disturbed. The jumpering information below is for reference and lists the different types of circuit boards that may be provided with the Disk Drive.

Identifying the Board - The type of board provided with the Disk Drive can be identified by the Shugart assembly number stamped in black on the component side of the board (refer to Figure 4-13). Below is a list of assembly numbers for the boards presently used in the Shugart 850/851 Disk Drive.

25189-2	25201-2	25216-0
25190-2	25202-3	

Jumpers - The following table shows the jumpers required on the boards for them to function in the VS AWS. Jumper clips are available under part number 350-4506. Figure 4-13 illustrates the location of these jumpers on the 25202-3 board.

	Assembly Numbers		
Jumpers	25189-2 25190-2	25201-2 25202-3	25216-0
Y	OUT	OUT	OUT
850	IN	IN	IN
IW (not connected to ground)	IN	IN	IN
2S	IN	IN	IN
DC	IN	IN	IN
C to HI	IN	IN	IN
S2	IN	IN	IN
IT	IN	IN	IN
FM	OUT	OUT	IN
MFM	OUT	OUT	IN
RS	IN	IN	IN
M	IN	IN	IN
AF	*	IN	OUT
FS	IN	IN	IN
TS	OUT	OUT	OUT
DS2	IN	IN	IN
In location 4F, cut shunt at positions:	2/4 (HL & B)	2/4 (HL & B)	2/4 (HL & B)

(*) Refer to modifications to the 25189-2 & 25190-2 boards under next heading.

Modifications - In addition to the jumpers noted above, certain modifications must be made to the board for proper operation in the VS AWS. These additional items are described below.

25189-2 & 25190-2 Boards Only:

- Jumper pins 3 and 11 of IC 8D.
- Jumper pin 11 of IC 8D to pin F.

All Boards:

- Insert the terminator block (P/N 220-3137) at location 5E.
- Cut etch on non-component side of PCA between IC 3E pin 8 and IC 3F pin 1.
- Jumper pin 851 to IC 3F pin 1.

4.3.4.6 Shugart 901 Disk Drive

The circuit board on the Shugart 901 Disk Drive contains jumpers which are set at the factory for proper operation with the WP/OIS AWS. These jumpers should not be disturbed. The jumpering information below is for reference. Use it as a check of proper jumpering of the board provided with the Disk Drive, or for setting the jumpers on replacement Disk Drive units.

The jumpers given below apply to Shugart 901 Logic Board number 25006-7. This identification number is stamped in black on the component side of the board. Refer to figure 4-14 for jumper locations.

Jumper	Configuration	Jumper	Configuration
A	IN	N	IN
B	IN	P	OUT
C	OUT	R	OUT
D	OUT	S	OUT
E	IN	T	OUT
F	OUT	X	OUT
G	OUT	Y	IN
H	OUT	U1	IN
J	OUT	U2	OUT
K	OUT	DS	IN
L	IN	*R13	OUT
M	IN	(*) R13 is a 150-Ohm resistor.	

Modifications:

- Install a jumper wire from E to R for WP/OIS operation.
- Install Door Lock Kit (725-0053-93) Installation instructions are provided. Make the following changes to the 25006-7 PCA (figure 4-14).
  - Cut etch between U3E and U3F
  - Install wire between B and U3F pin 7
  - Remove wire from J6 pin 3 and relocate to Door Lock feedthrough hole

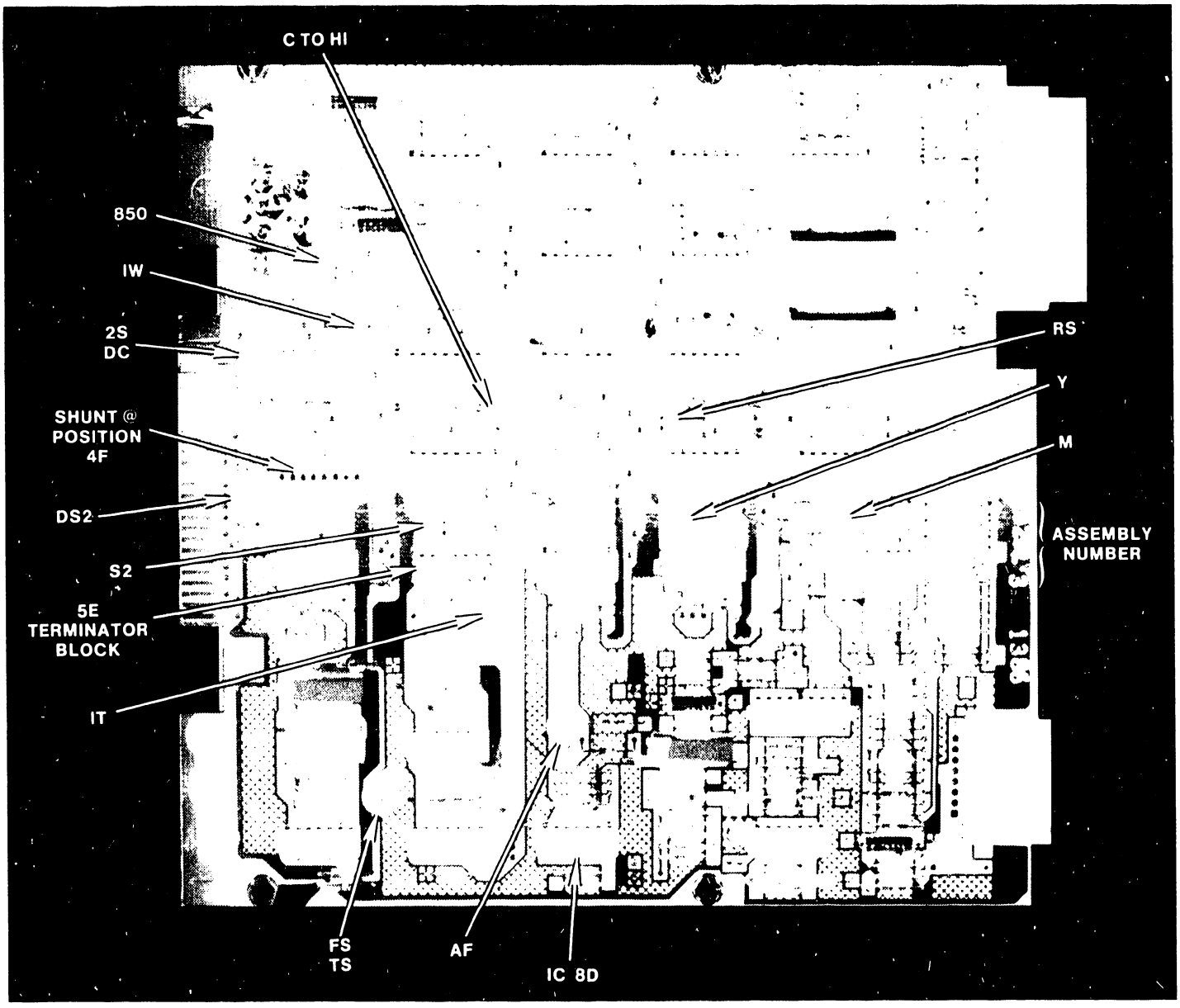
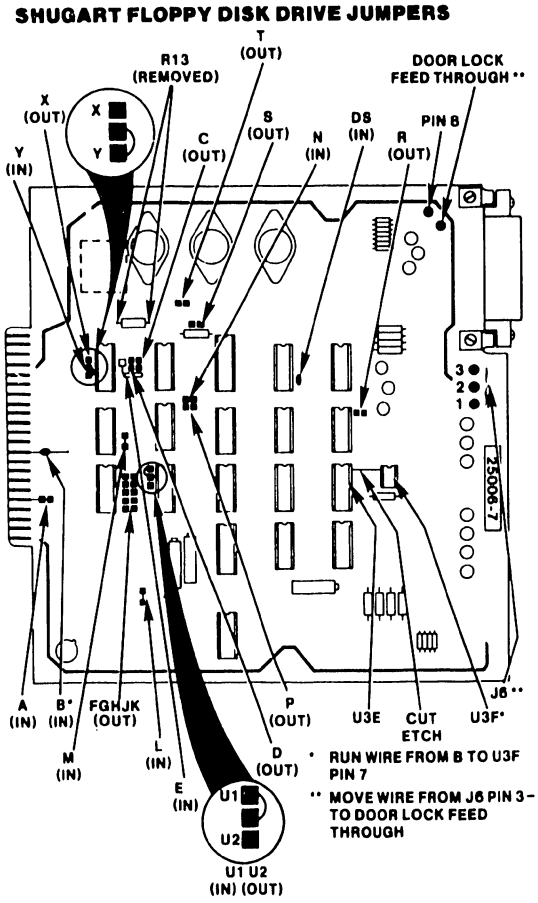


Figure 4-13 Shugart 850/851 Logic Board Jumpers (25202-3 Shown)



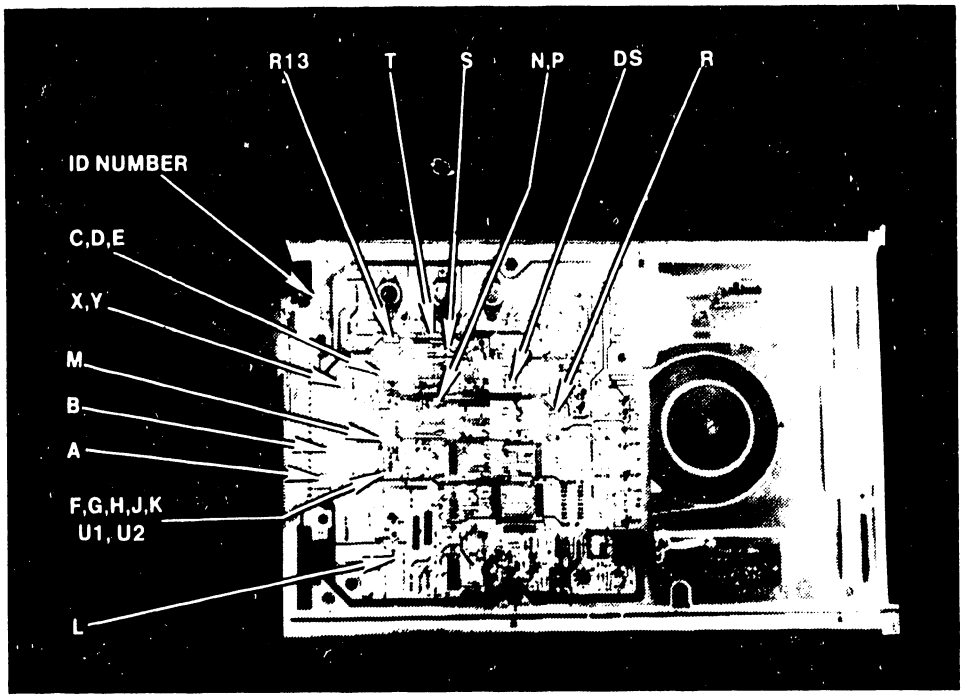


Figure 4-14 Shugart 901 Logic Board Jumpers

4.3.5 SYSTEM INTERCONNECTIONS

Referring to Figure 4-15, make the required connections between the Terminal and the Archiving Master and the Master CPU as directed below.

1. Connect the 220-0105-3 cable from the KEYBOARD connector on the rear of the Terminal to the KEYBOARD connector on the rear of the Archiving Master. Connect the Keyboard cable to the KEYBOARD connector on the rear of the Terminal (5730 ONLY).

2. Connect the 220-0199 single coaxial cable from the VIDEO connector on the rear of the Terminal to the VIDEO connector on the rear of the Archiving Master.

3. Connect a dual coaxial cable from the DATA LINK connectors on the rear of the Archiving Master to the Master CPU. These connections are a BNC/TNC pair and can only be connected BNC to BNC, TNC to TNC. The length of this cable is not to exceed 2000 feet.

   NOTE

   Special instructions required for proper connection of the VS AWS to the Input/Output Processor along with the required SYSGEN procedure are in Appendix B of this manual.

4. Plug the ac power cords into suitable ac power outlets.

4.4 POST-INSTALLATION CHECKS

This section details the final checks to be made before turning the equipment over to the customer.

4.4.1 SYSTEM SOFTWARE COMPATIBILITY

4.4.1.1 VS System Software Compatibility

Information given in this manual is compatible with VS Archiving Workstation microcodes given below in current operating system 05.03.70.

@MC2266S: 05.00.07* @MC2266C: 05.01.03 (also used for 2276C)

*This version is required for use of IBMCOPY utility.

4.4.1.2 WP/OIS System Software Compatibility

Information given in this manual is compatible with all current WP/OIS operating system software versions.

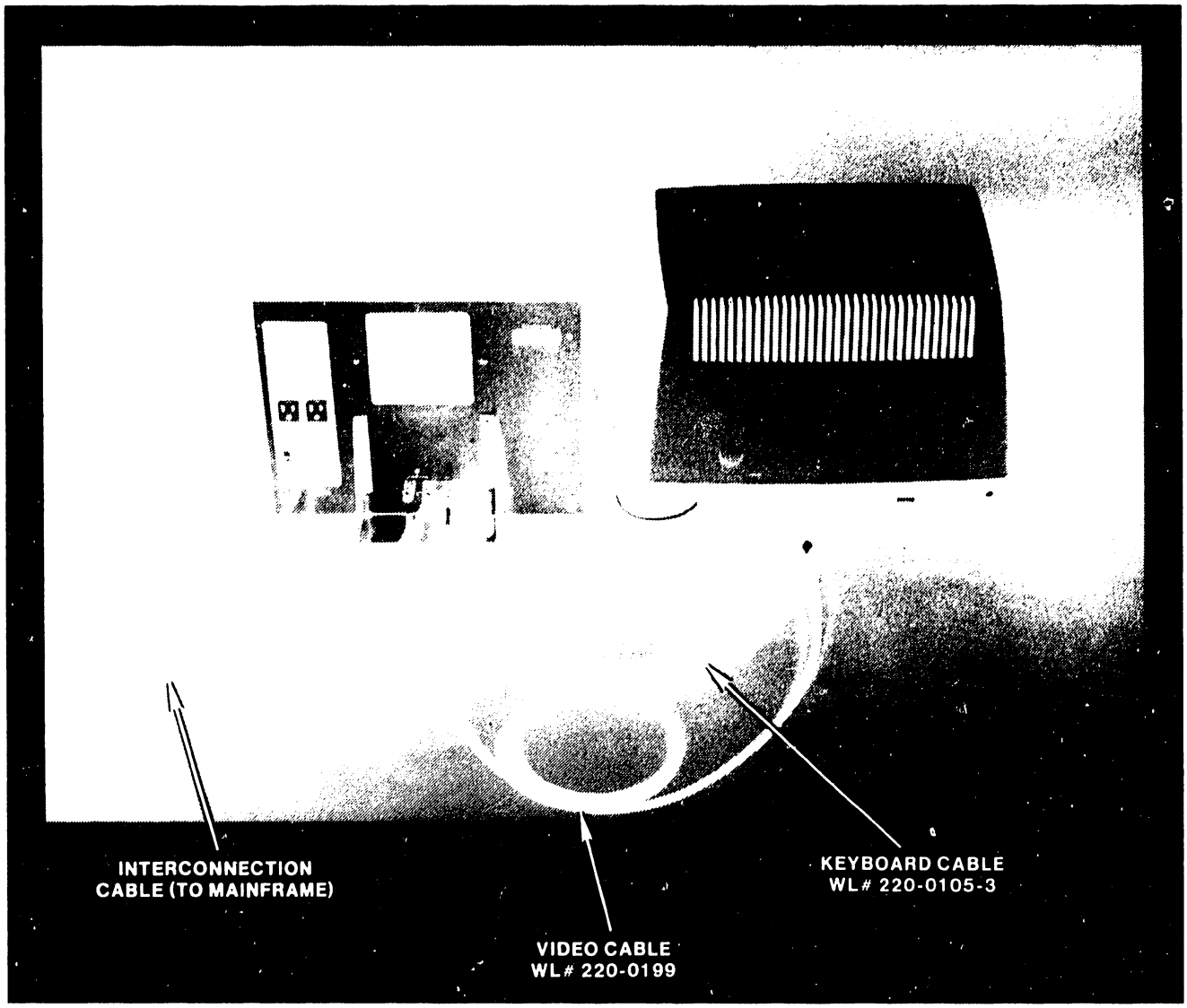


Figure 4-15 AWS Interconnections

4.4.2 SYSTEM TURN-ON

Before initial system turn-on, plug the BRIGHTNESS/CONTRAST control harness into its connector on the 12-inch monitor chassis, if it had been previously disconnected.

To initially turn on the AWS, simply set the Archiving Master unit rear panel ON/OFF switch to the ON position, and set the Terminal rear panel On/Off toggle switch to the ON position.

The Terminal CRT raster should appear after about thirty seconds, along with the workstation main menu. Should the menu not appear, adjust the BRIGHTNESS and CONTRAST controls on the front panel of the workstation (Figure 3-1).

NOTE

If a raster and/or menu does not appear, refer to Chapter 8 of this manual for troubleshooting procedures.

After a raster/menu has been obtained, proceed with the voltage checks in the next section.

4.4.3 VOLTAGE CHECKS

At this point, the internal power supplies in both the Archiving Master and the Terminal should be checked to confirm that they are within the allowable tolerance for proper operation of the AWS.

Referring to Figure 4-16, the following voltages can be measured at the upper corner of the Data Link/Memory (DL/M) PCA or at J2 of the Motherboard. Connect a suitable digital multimeter positive lead to the listed test points, negative lead to TP±0V, and confirm the following voltages. If the voltages do not measure within the allowable limits, adjust them with the potentiometers listed below on the Power Supply Regulator PCA.

DC Voltage	Adjustment Potentiometer	Monitoring Test Point	Acceptable Range
+12V	R35 (Front)	Middle TP, DL/M PCA	11.8V thru +12.2V
+5V	R17 (Middle)	Rear TP, DL/M PCA	+4.9V thru +5.1V
-5V	Nonadustable	Front TP, DL/M PCA	-4.9V thru -5.1V
+24	R10 (Rear)	J2 pin 14, Motherboard	+23.6 thru +24.4V

Only after the above voltages have been checked and adjusted should the Terminal voltages be checked. Terminal voltages are derived from the +24 and +12 volt supplies from the Archiving Master. Measure the +12 volt line in the Terminal at the points shown in Figure 4-17 (acceptable range is +11.8 through +12.2 Vdc). If necessary, adjust the Monitor Power Supply using R4 near the

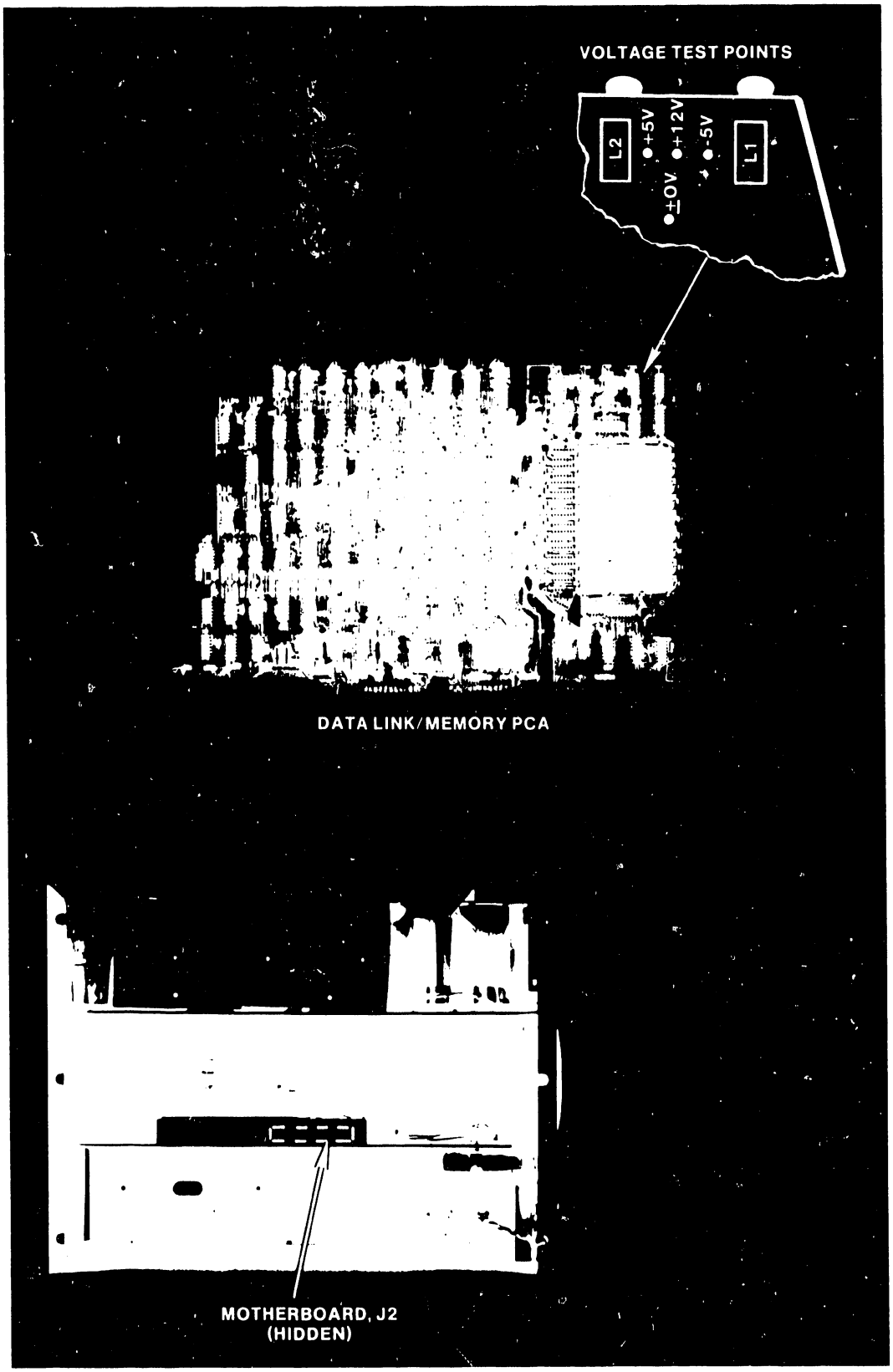


Figure 4-16 Power Supply Checks and Adjustments
(Archiving Master)

top of the Power Supply subassembly (see Figure 4-8 for location).

Measure the Terminal +5 volt supply at the emitter of Q1 on the CRT Junction PCA (see Figure 4-8 for location). Allowable range is +4.9 through +5.1 Vdc. If necessary, adjust using R2 on the CRT Junction PCA.

4.4.4 DIAGNOSTICS

After the voltage checks have been completed, use the diagnostics listed in either Table 1-3 or Table 1-4 to check the ability of the AWS to operate properly.

To make a final operational check of the AWS, perform the performance verification procedure in section 3.4.2 of this manual.

4.4.5 AWS BUTTON-UP

Replace the covers on both the Terminal and the Archiving Master unit by reversing the removal procedures in section 4.3.1, giving careful attention to the following items:

- Be sure to replace the PCA hold-down brackets in the Archiving Master.
- Verify that no cables/harnesses within the Archiving Master interfere with the operation of the ventilating fan.

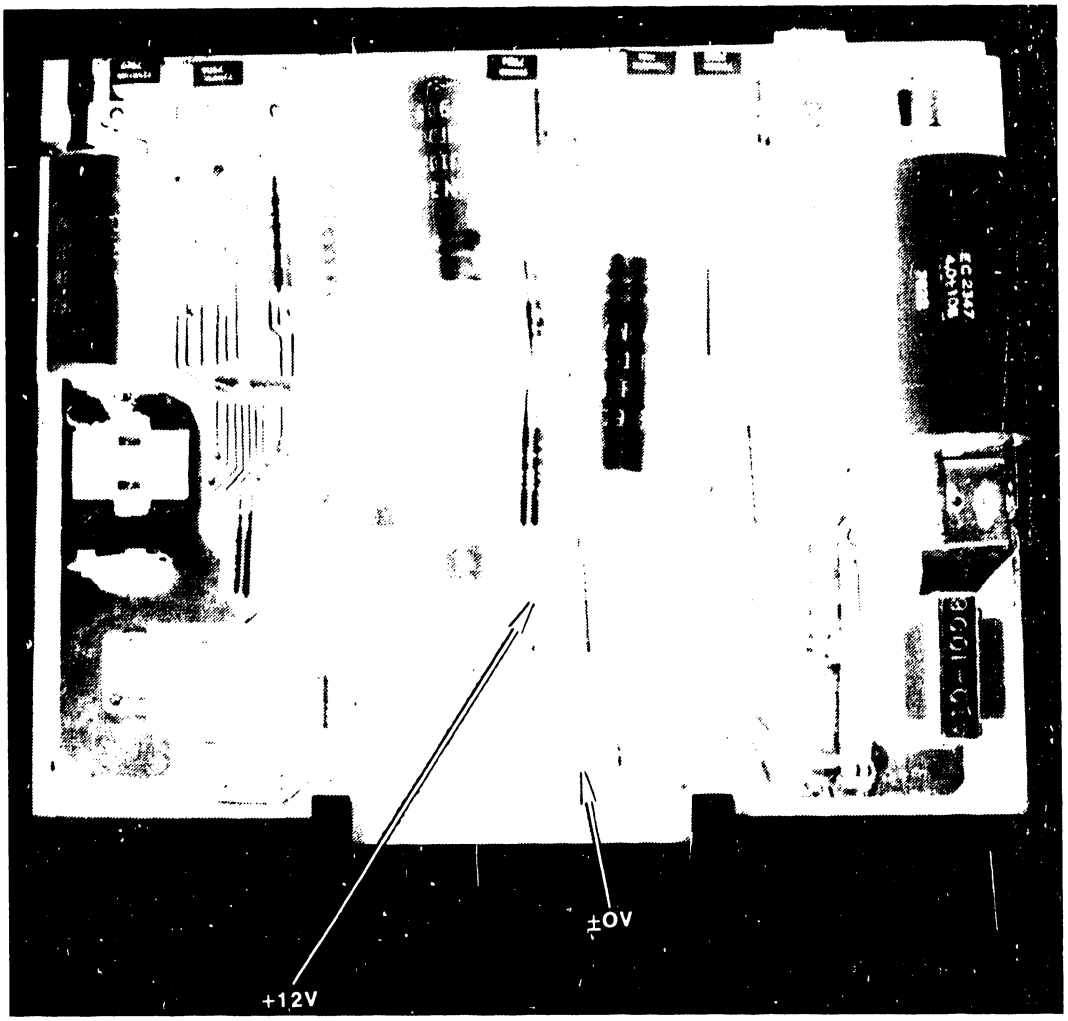


Figure 4-17 Power Supply Checks and Adjustments
(Terminal)

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 REQUIRED TOOLS, TEST EQUIPMENT AND ACCESSORIES

The following items are required to carry out the preventive and corrective maintenance activities described in this chapter or elsewhere in this manual.

Description

CE Tool Kit
Digital Multimeter
Oscilloscope, Dual Trace
Dysan 360/2A Double Sided
Alignment Diskette (VS Only)
Cartridge Alignment Tool
Head Loading Tool
PC Card Extender Board

5.2 PREVENTIVE MAINTENANCE

Preventive Maintenance should be performed on a regular basis to help prevent workstation equipment failures. The suggested plan for regular preventive maintenance follows.

5.2.1 SEMI-ANNUALLY (QUARTERLY IN AN INDUSTRIAL ENVIRONMENT) OR DURING AN UNSCHEDULED TROUBLE CALL

5.2.1.1 Cleaning

Remove power from the AWS Master and Terminal and clean as follows:

1. Dust Terminal keyboard with a soft-bristled brush.

2. Clean the CRT screen, using a good quality glass cleaner and soft, lint-free cloth.

3. Wipe exterior of workstation, using a damp, lint-free cloth.

4. Vacuum dust from the ventilating slots in the cover of the Terminal and the Archiving Master, and from around the fan at the rear of the Archiver Master.

5.2.1.2 Checks and Adjustments

Apply power to the Archiver Master and Terminal and proceed as follows:

1. Check and adjust the Archiver Master power supply voltages, as described in section 4.4.3.

2. Check and adjust the Terminal display voltages, as described in section 4.4.3.

3. Check for proper character display. Perform the Video Display Alignment Procedure (section 5.3.2), if required.

5.2.1.3 Diagnostics

Run applicable diagnostics (section 1.2.2) to verify proper AWS operation.

5.2.2 ANNUALLY (SEMI-ANNUALLY IN AN INDUSTRIAL ENVIRONMENT)

Check all cables and connectors for proper seating. Loose or damaged connectors should be repaired or replaced.

5.2.2.3 Shugart Disk Drive Preventive Maintenance

The following preventive maintenance tasks should be performed on the Shugart Disk Drives (850/851, VS; 901, WP/OIS). Refer to section 1.2.1 for the OEM manual which details these procedures.

Area	Action
Actuator Band, Capstan and Shaft	Clean of oil, dust and dirt if necessary.
Belt	Inspect for frayed or weakened areas. Replace if necessary.
Base	Clean base, inspect for loose screws, connectors or switches.
850/851 Read/Write Heads	Check for proper alignment. (See section 5.3.3.)
901 Read/Write Heads	Clean heads of oil, dust or dirt with a pad soaked in alcohol. If worn, install replacement head load pad kit (726-1005).

5.3 CORRECTIVE MAINTENANCE

This section contains adjustment and alignment procedures required in the Archiving Master and the Terminal. The tools, test equipment and accessories required for these procedures are listed in section 5.1. Procedures included are listed below.

Section	Procedure
5.3.1	Voltage Checks and Adjustments
5.3.2	Video Display Alignment
5.3.3	Shugart 850/851 Mechanical Alignments (VS only)

5.3.1 VOLTAGE CHECKS AND ADJUSTMENTS

All but one of the voltage checks and adjustments for the Archiver Master and the Terminal are detailed in section 4.4.3 of this manual. The dynamic focus adjustment in the Terminal, the one remaining voltage check/adjustment, is given below.

Pre-Alignment Conditions: - Remove cover from Terminal (section 5.4.1).
- Set Terminal On/Off switch to ON.
- Set Archiver Master ON/OFF switch to ON.

Refer to Figure 5-1 for the following procedure.

1. Connect an oscilloscope to pin M of the Monitor Electronics PCA, ground lead to a convenient ground (±0V).

CAUTION

Use a non-metalic tuning wand when adjusting dynamic focus coil Z1.

2. Adjust dynamic focus coil Z1 for 250 ± 10% volts peak-to-peak on the oscilloscope.

5.3.2 VIDEO DISPLAY ALIGNMENT

Pre-Alignment Conditions: - Remove cover from Terminal (section 5.4.1).
- Set Terminal On/Off switch to ON.
- Set Archiver Master ON/OFF switch to ON.

Refer to Figure 5-1 for the following procedure.

1. Create a document which will display a screen filled with alternating "HO" characters.

2. Set both horizontal hold (R33) and vertical hold (R15) to the middle of their stable display range.

3. Adjust the BRIGHTNESS and CONTRAST controls so that the CRT raster is plainly visible, but do not set so high as to cause blooming.

4. Adjust vertical size control R24 so that the raster measures 6.5 inches (16.5 cm) top to bottom on the 12" display. (Use a standard or metric scale.)

5. Adjust vertical linearity control R18 so that character rows at the top, middle and bottom of the screen are the same height.

6. Repeat 4 and 5 until both requirements are met.

7. Adjust width coil Z2 so that the raster measures 8 inches (20.3 cm) from left to right on the 12" display. (Use standard or metric scale.)

8. Adjust horizontal linearity coil Z3 so that character columns at the left, middle and right of the screen are the same width.

9. Repeat 7 and 8 until both requirements are met.

10. Adjust horizontal phasing control R35 to center the "HO" character block horizontally on the raster.

11. Adjust focus control R28 for the sharpest overall screen display.

12. Center the raster on the CRT face with the trim tabs located on the rear of the yoke.

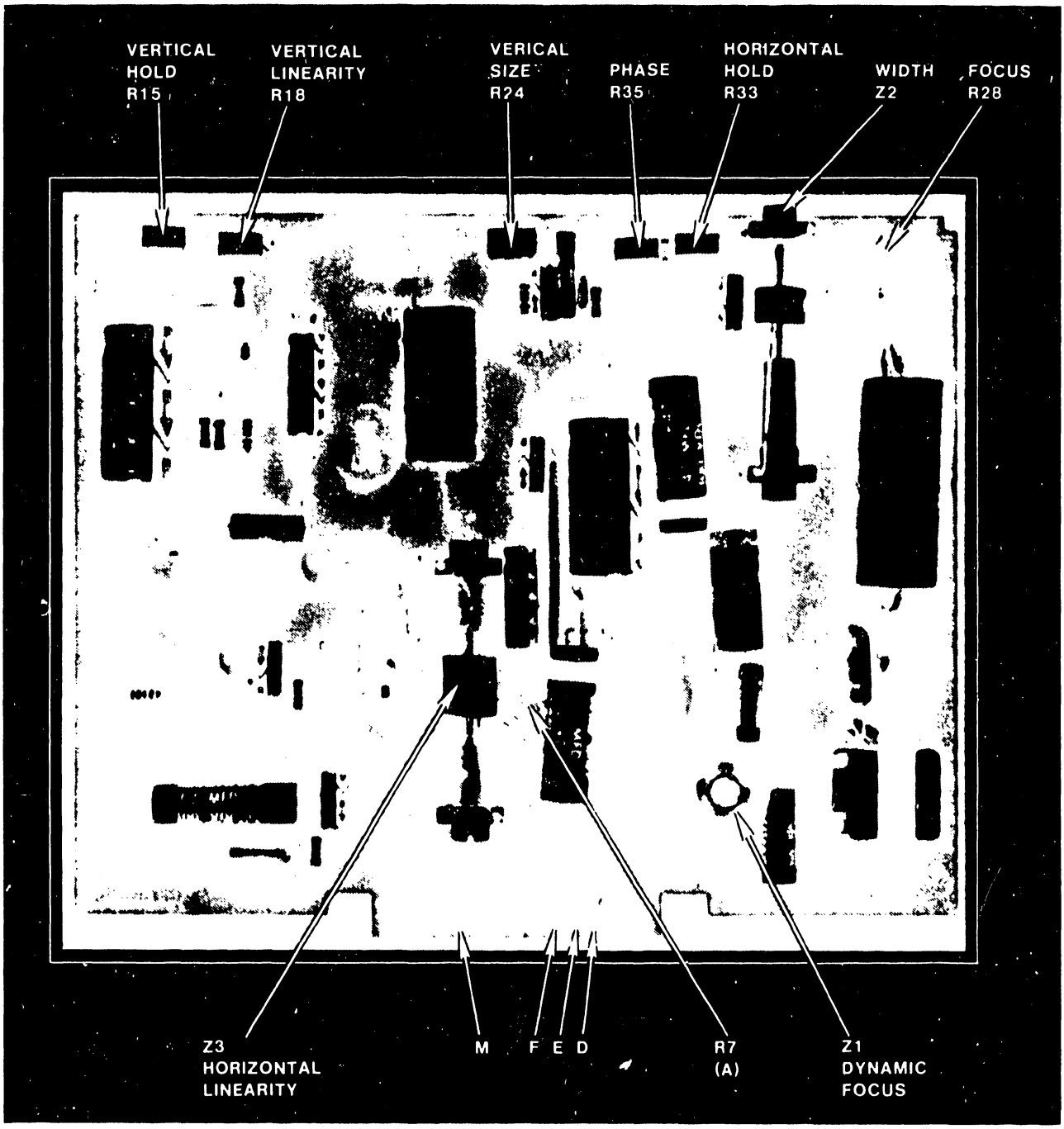


Figure 5-1 Video Alignment Test Points and Adjustments

5.3.3 SHUGART 850/851 MECHANICAL ALIGNMENTS (VS ONLY)

Mechanical alignments for the Shugart 850/851 Disk Drive used in the VS AWS are included here. The procedures are grouped by subheadings for ease of reference, but should be performed in the sequence given and in their entirety.

Pre-Alignment Conditions:
- Remove cover from Archiver Master (section 5.5.1).
- Remove the Disk Drive from the Archiver Master (section 5.5.3), but leave all cables connected.
- Set Terminal On/Off switch to ON.
- Set Archiver Master ON/OFF switch to ON.

Refer to Figures 5-2 and 5-3 for the following procedures.

1. Load diagnostic program FTU61C4 and load the alignment diskette (726-1922) in the Disk Drive.

2. In response to the diagnostic menu prompt, enter the Disk Drive number and name, and then press ENTER.

3. When the function menu appears, select SOFT SECTOR by pressing PF 11.

5.3.3.1 Index and Sector Adjustment

1. Prepare an oscilloscope and connect as shown below.

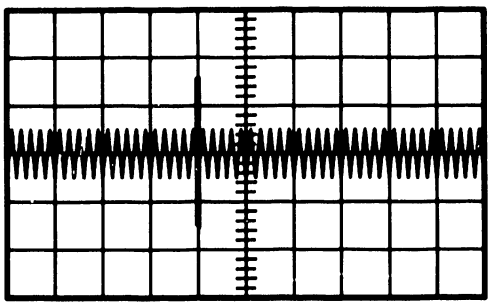
   - Probe Channel A, AC: TP1
   - Probe Channel B, AC: TP2
   - Sync: DC, external negative; Sync Probe: TP12 (INDEX pulse)
   - Time Base: 50 usec/division
   - Vertical Sensitivity: 0.5 volts/division
   - Mode: Add and Invert Channel B
   - Trigger Mode: Normal

2. On the function menu, enter cylinder 0001 as both the beginning and ending cylinder (FROM CYL = 0001, TO CYL = 0001).

3. Press PF 6 for alternate seeks.

The FTU program will now execute and position the read/write heads over cylinder 1. The heads will remain in this postion until any PF key is pressed. This allows data and index signals to be checked for proper alignment.

4. Observe the timing pulse on the oscilloscope. From the start of the sweep to the leading edge of pulse should be 200 $\pm$ 50 usec (see figure below). If the timing is not within tolerance, adjust according to steps 5 through 7 following. If the timing is within tolerance, proceed to step 8.



INDEX PULSE TIMING

5. Loosen the index transducer holding screw until the transducer is just able to be moved (see Figure 5-2).

6. Adjust the transducer until the timing is within tolerance as given in step 4.

7. Tighten the index transducer holding screw and re-check the timing.

8. Repeat steps 2 through 7 of this procedure, entering cylinder 0076 as both the beginning and ending cylinder to verify proper operation.

5.3.3.2 Head Radial Alignment

1. Prepare an oscilloscope as shown below.

   - Probe Channel A, AC: TP1, Ground to TP5
   - Probe Channel B, AC: TP2, Ground to TP6
   - Sync: DC, external negative; Sync Probe to TP12 (INDEX pulse)
   - Time Base: 20 msec/division
   - Vertical Sensitivity: 0.2 volts/division
   - Mode: Add and Invert Channel B
   - Trigger Mode: Normal

2. Enter cylinder 0038 as the beginning and ending cylinder (FROM CYL = 0038, TO CYL = 0038). This will loop the FTU program on cylinder 38 allowing the read/write head output to be monitored and/or adjusted.

3. Press PF 6 to select alternate seeks.

4. Observe the oscilloscope display and compare it with Figure 5-4. This display represents the exact location of the read/write head on track 38. The amplitude of the lobes must be within 70% of each other. If this is not the case, adjust according to steps 5 and 6.

5. Loosen two or four mounting screws on the radial alignment plate as shown in Figure 5-3.

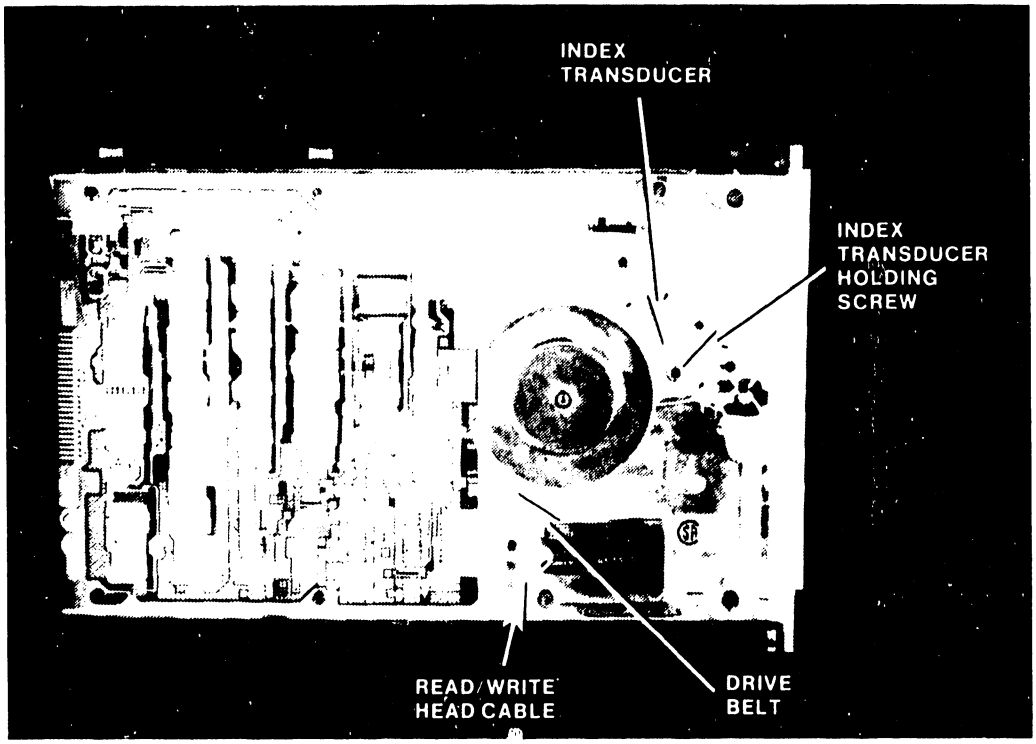


Figure 5-2 Shugart 850/851, Left Side

6. Turn the eccentric adjusting screw (see Figure 5-3) to move the plate and make the adjustment. When the lobes are of equal amplitude, tighten the mounting screws.

7. Press any PF key to halt, then PF16 to return to function menu.

8. Check the adjustment by stepping off track in both directions and returning. Re-adjust if required.

5.3.3.3 Track 00 Detector Adjustment

The head radial alignment procedure (section 5.3.3.2 above) must be performed before this procedure is carried out.

1. Prepare an oscilloscope as shown below.

   - Probe Channel A, DC: TP26, Ground to TP5
   - Sync: Channel A, continuous auto
   - Time Base: 10 msec/division
   - Vertical Sensitivity: 1.0 volts/division
   - Trace Line: Set equal to ground and position in screen center

2. Enter cylinder 0001 as the beginning and ending cylinder address (FROM CYL = 0001, TO CYL = 0001).

3. Press PF 6 to select alternate seeks.

4. Observe the oscilloscope. TP26 should be high (between +3 and +5 volts). If this is not the case, adjust according to step 5 following.

5. Loosen the holding screw on the track zero assembly as shown in Figure 5-3. Move the assembly toward the spindle until TP26 goes high.

6. Return to the function menu, enter 0002 as the beginning and ending cylinder addresses and press PF 6 to select alternate seeks.

7. Observe the oscilloscope. TP26 should be low (0 volts). If not, move the track zero assembly toward the actuator until TP26 goes low.

8. Return to the function menu, enter 0001 and 0002 as the cylinder addresses, press PF 6 (alternate seeks) and observe TP26. This will automatically step the head between cylinders 1 and 2. Observe that TP26 is low at cylinder 2 and high at cylinder 1. A correct adjustment is indicated by a square wave display on the oscilloscope.

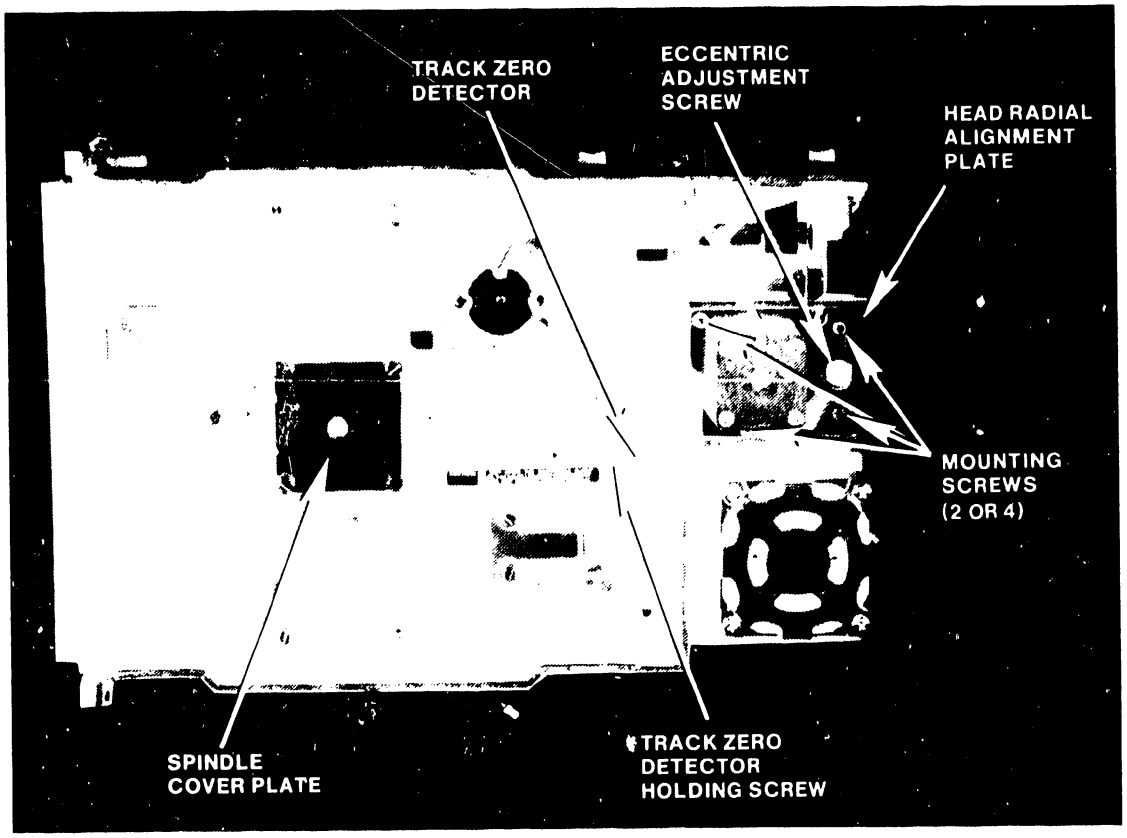


Figure 5-3 Shugart 850/851, Right Side

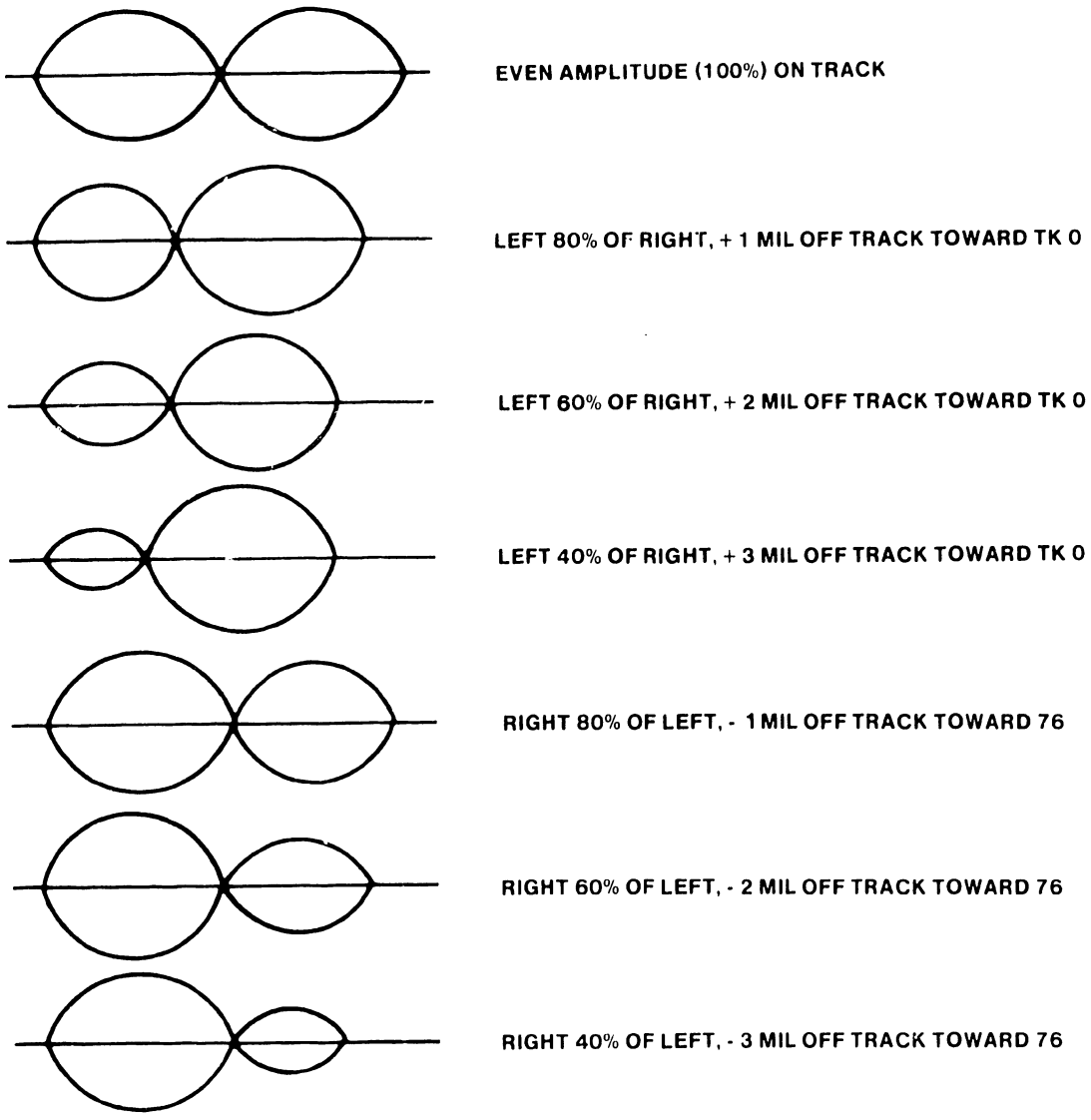


Figure 5-4 Head Radial Alignment Waveform and Interpretation

5.4 TERMINAL REMOVAL AND RE-INSTALLATION PROCEDURES

This section contains removal and re-installation procedures for major assemblies in the Terminal. Before removing a particular assembly, ensure that the power switch is off and the ac power cord is unplugged on both the Terminal and Archiver Master. Remove the Terminal cover as described in section 5.4.1. Refer to section 6 (Illustrated Parts Breakdown) for supplementary parts location and identification information.

WARNING

CRT DISCHARGE PROCEDURE

Before performing any of the procedures in this section, discharge the CRT anode according to the following procedure.

Even with power removed, the Terminal cathode ray tube can hold a charge of several thousand volts. To eliminate the risk of accidental CRT discharge, which can result in serious injury, discharge the CRT anode as follows:

1. Attach one end of a length of insulated wire to the metal shaft of a plastic-handled, heavy-duty screwdriver.

2. Attach the other end of the wire to chassis ground.

3. Using a non-conductive tool such as a plastic alignment tool, carefully raise the edge of the rubber anode cap high enough to insert the screwdriver.

4. Taking care not to touch the metal shaft of the screwdriver or any metal part of the Terminal, discharge the CRT anode by touching the anode clip with the grounded screwdriver.

5. After discharging the CRT, remove the grounding wire and reseat the rubber anode cap.

5.4.1 COVER

5.4.1.1 5506 Monitor (Figure 4-4)

Removal:

1. Remove three screws located under plastic strip on keyboard and remove keyboard plate.

2. Remove one screw from each side of Terminal near lower edge of cover.

3. Remove keyboard cover plate.

4. Lift cover up and away from Terminal; take care not to hit or nick CRT, or strain BRIGHTNESS/CONTRAST control wires.

5. Grasp the locking tabs of the BRIGHTNESS/CONTRAST control harness connector and press inward toward the harness to release the connector. Simultaneously pull the connector from its socket. Lay cover on its side next to Terminal.

Re-installation:

To re-install the Terminal cover, reverse the removal procedure.

5.4.1.2 5730 Monitor (Figure 4-4)

Removal:

1. Remove one screw from each side on rear of Terminal near lower edge of cover.

2. Slide cover back along tracks about three inches. Lift cover up and away from Terminal.

Re-installation:

To re-install the Terminal cover, reverse the removal procedure.

5.4.2 KEYBOARD

5.4.2.1 5506 Monitor (Figure 5-5)

Removal:

1. Remove the Terminal cover per section 5.4.1.

2. Scribe the location of the four screws that secure the keyboard to the Terminal. This will enable easier re-installation of the keyboard.

3. Remove four screws that secure the keyboard to the base of the Terminal.

4. Remove two screws securing the keyboard ribbon cable clamp and remove the clamp.

5. Lift the right side of keyboard up to access the keyboard grounding wire and disconnect the wire from its grounding lug.

6. Disconnect the keyboard ribbon cable from the underside of the keyboard assembly and remove the keyboard.

5.4.2 KEYBOARD (Continued)

Re-installation:

To re-install the keyboard, reverse the removal procedure. Be sure to install spring washers and align marks scribed in step 2 with the keyboard mounting screws for proper mechanical and electrical installation.

5.4.2.2 5730 Monitor

Removal

1. Disconnect keyboard from base unit.
2. Remove two screws from underside of keyboard.
3. Remove top portion of keyboard enclosure.
4. Disconnect keyboard connector and ground wire from keyboard.
4. Lift keyboard away from bottom portion of keyboard enclosure.

Re-installation:

To re-install the keyboard, reverse the removal procedure.

5.4.3 MONITOR CHASSIS

5.4.3.1 5506 Monitor

1. Remove cover per section 5.4.1.
2. Disconnect one Molex connector connecting the rear panel VIDEO jack to the BRIGHTNESS/CONTRAST control wire harness.
3. Disconnect the ac power cord from the ac power plug on the Terminal base plate.
4. Remove four hex-head screws that secure the monitor chassis to the Terminal base plate.
5. Lift the monitor chassis out of the Terminal.

Re-installation:

To re-install the monitor chassis, reverse the removal procedure.

5.4.3 MONITOR CHASSIS (Continued)

5.4.3.2 5730 Monitor

1. Remove cover per section 5.4.1.
2. Disconnect two Molex CRT connectors.
3. Remove four hex-head mounting screws that secure the monitor chassis to the support posts.
4. Lift the monitor chassis out of the Terminal.
5. Take off CRT bezel by removing four mounting screws (two on each side).

Re-installation:

To re-install the monitor chassis, reverse the removal procedure.

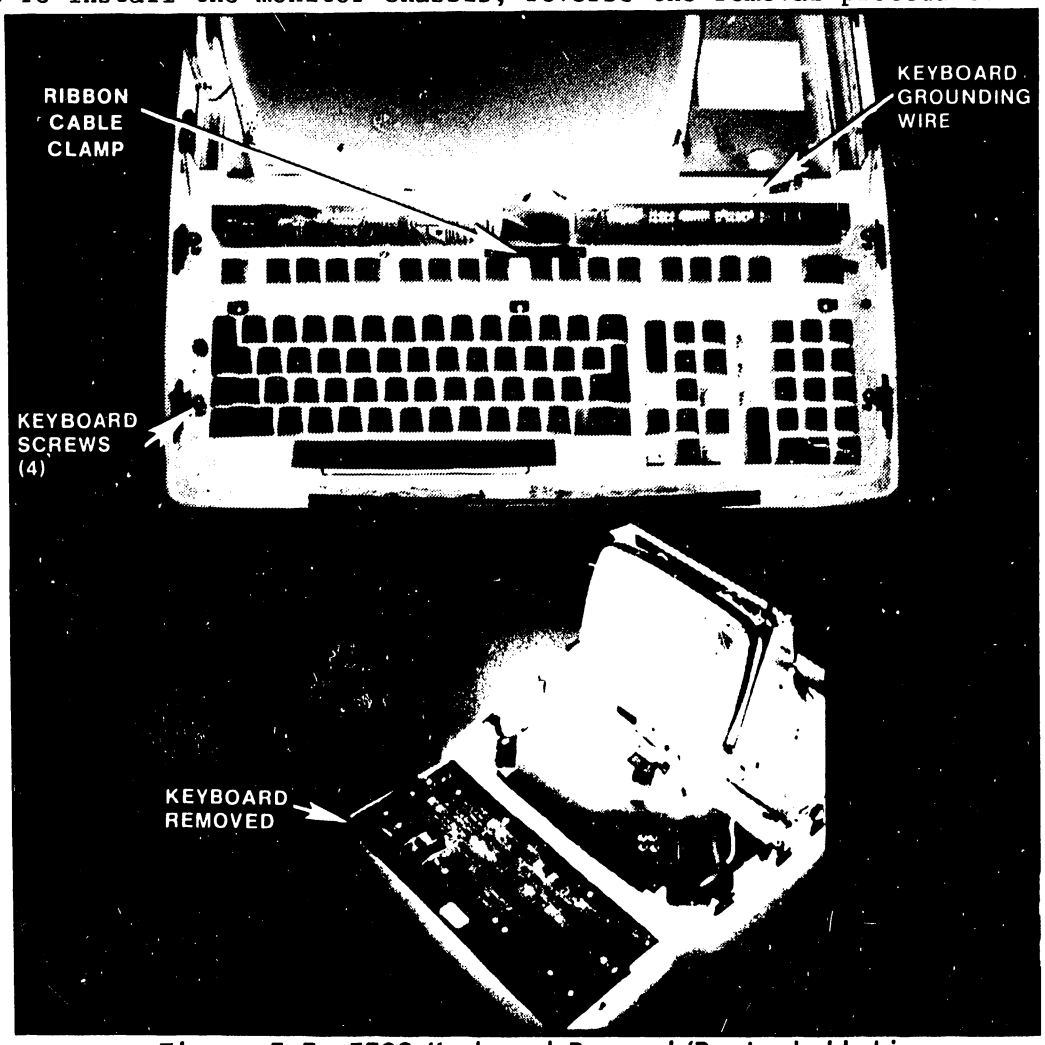


Figure 5-5 5506 Keyboard Removal/Re-Installation

5.4.4 TERMINAL BASE PLATE CHASSIS/JUNCTION PCA

5.4.4.1 5506 Monitor

Removal:

1. Remove cover per section 5.4.1.
2. Remove keyboard per section 5.4.2.
3. Remove monitor chassis per section 5.4.3.
4. Disconnect one ground wire from its grounding lug at front of base plate.
5. Remove four screws securing the base plate to the molded base.
6. Lift the base plate chassis with the CRT Junction PCA out of the molded base.
7. Remove keyboard ribbon cable from CRT Junction Board.
8. Remove two screws securing transistor heat sink bracket to the Terminal base plate.
9. Remove two threaded standoffs securing KEYBOARD rear panel connector to rear panel.
10. Remove CRT Junction Board and heat sink together.

Re-installation:

To re-install the Terminal base plate/Junction PCA, reverse the removal procedure.

5.4.4.2 5730 Monitor

Removal:

1. Remove power supply per section 5.4.7.
2. Disconnect three Molex connectors.
3. Remove 4 screws securing base plate to base.
. Remove ground wires.

5.4.4 TERMINAL BASE PLATE CHASSIS/JUNCTION PCA (Continued)

Re-installation:

To re-install the CRT Junction Board, reverse the removal procedure.

5.4.5 KEYCAP AND SWITCH

Removal:

1. Remove keyboard per section 5.4.2.
2. Using the keycap removal tool (P/N 726-9545), remove keycap from switch being replaced and as many adjacent keycaps as required to provide adequate work space.
3. Unsolder four terminals of the keyswitch from underside of keyboard.
4. Insert the switch extractor tool (P/N 726-9608). Grip switch extractor and pull straight up, removing switch from keyboard.

Replacement:

1. Insert new keyswitch. Take care to orient the switch properly and observe the solder terminals are through the printed circuit board prior to snapping in place.
2. Solder new switch in place.
3. Replace the keycap(s). When work has been completed, perform a visual check to insure that keycaps have been installed on correct switches. Test new switch to be certain that it functions properly.

5.4.6 MONITOR POWER SUPPLY

5.4.6.1 5506 Monitor

Removal:

1. Remove monitor chassis per section 5.4.3.
2. Unwrap ac power cord from around monitor chassis.
3. Remove wire harness from cable clamp on monitor power supply.
4. Disconnect in-line Molex connector connecting power supply to Monitor Electronics Board.
5. Remove three hex-head screws securing monitor power supply to monitor chassis.

5.4.6 MONITOR POWER SUPPLY (Continued)

5.4.6.1 5506 Monitor

6. Tilt rear of power supply subchassis up to disengage its slot from the monitor chassis.

7. Lift monitor power supply up and out of monitor chassis.

Re-installation:

To re-install the monitor power supply, reverse the removal procedure, being sure to engage the slot in power supply subchassis with the monitor chassis.

5.4.6.2 5730 Monitor

Removal:

1. Remove monitor cover per section 5.4.1.

2. Disconnect 3 Molex connectors.

3. Remove four screws that secure power supply to base plate.

4. Lift power supply up and out of monitor chassis.

Re-installation:

To re-install the monitor power supply, reverse the removal procedure, being sure to engage the slot in power supply subchassis with the monitor chassis.

5.4.7 MONITOR ELECTRONICS BOARD

5.4.7.1 5506 Monitor

Removal:

1. Remove monitor chassis per section 5.4.3.

2. Pull Monitor Electronics Board from its socket and slide out from the CRT screen side of the monitor chassis.

Re-installation:

To re-install the monitor power supply, reverse the removal procedure.

5.4.7 MONITOR ELECTRONICS BOARD (Continued)

5.4.7.2 5730 Monitor

Removal:

1. Remove Terminal cover as described in section 5.4.1.2.

2. Remove one screw from each side of Electronics Board cover (Figure 5-6).

3. Pull Monitor Electronics Board from its socket and slide out from the monitor chassis.

Re-installation:

To re-install the Monitor Electronics Board, reverse the removal procedure.

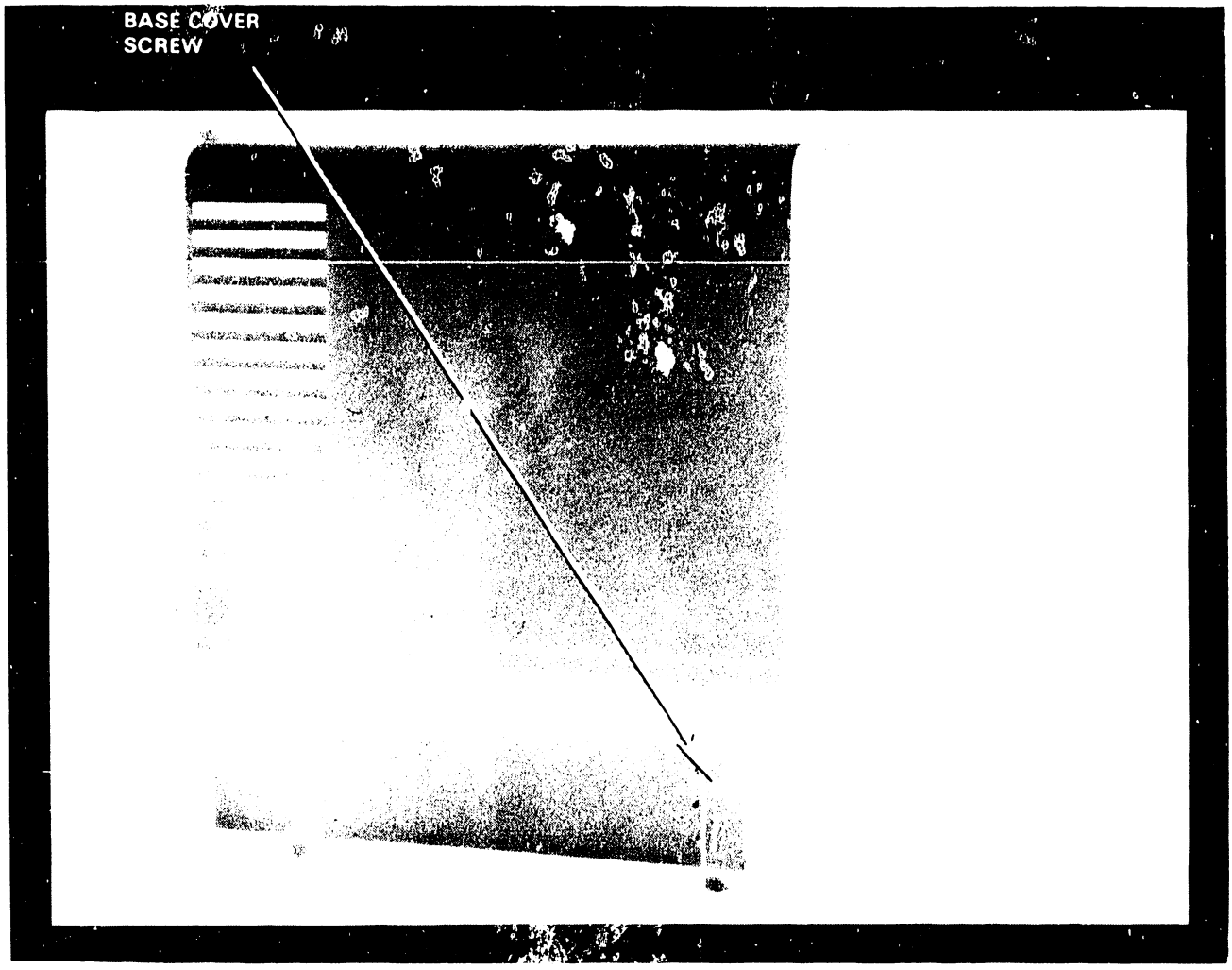


Figure 5-6 Removing the 5730 Monitor Electronics Board Cover

5.5 ARCHIVER MASTER REMOVAL AND RE-INSTALLATION PROCEDURES

This section contains removal and re-installation procedures for several major assemblies in the Archiver Master. Before removing a particular assembly, ensure that the power switch is off and the ac power cord is unplugged on both the Archiver Master and Terminal. Remove the Archiver Master cover as described in section 5.5.1. Refer to section 7 (Illustrated Parts Breakdown) for supplementary parts location and identification information.

5.5.1 COVER (Figure 4-5)

Removal:

1. Remove six screws (three each side) securing the cover to the Archiver Master.

2. Remove cover.

Re-installation:

To re-install the cover, reverse the removal procedure being sure that the air vents (slots) are toward the front of the unit.

5.5.2 PRINTED CIRCUIT ASSEMBLIES

Removal:

1. Remove cover per section 5.5.1.

2. Remove screws securing two PCA support brackets to card cage side plate and remove the PCA support brackets.

3. To remove any of the main logic PCAs, disconnect any associated plugs noting their locations for later installation and lift the PCA out of the card cage.

4. To remove the Power Supply Regulator PCA, remove two screws securing its heat sink bracket to the card cage side plate and lift it out of the card cage.

Re-installation:

To re-install any of the PCAs, reverse the removal procedure.

5.5.3 DISK DRIVE (Figure 5-7)

Removal:

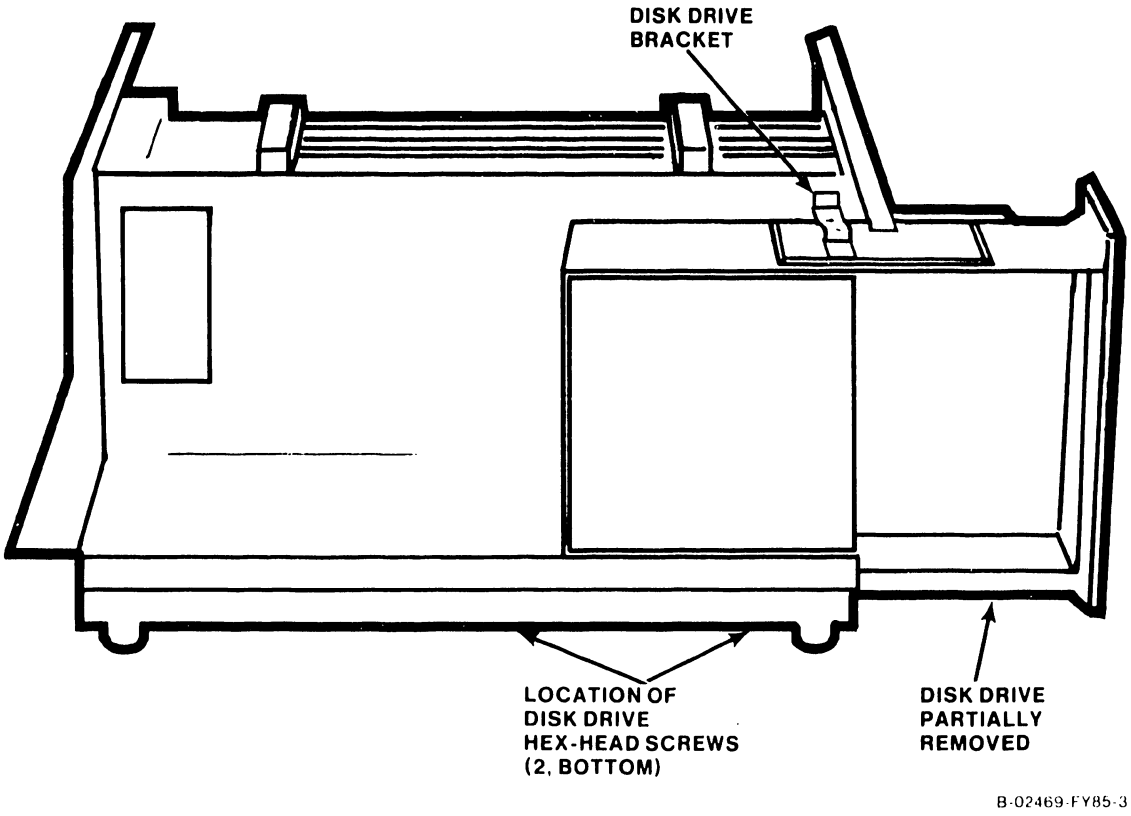


Figure 5-7 Removing the Disk Drive

1. Remove cover per section 5.5.1.

2. Disconnect plugs connecting Disk Drive to associated circuitry in the Archiver Master, noting their location and orientation for later installation.

3. Remove two hex-head bolts securing Disk Drive to Archiver Master bottom plate.

4. Remove one screw securing Disk Drive to bracket at top front edge of Disk Drive.

5. Slide Disk Drive forward and out of Archiver Master.

If the Shugart 850/851 Disk Drive is to be repackaged for shipment, turn the stepping motor worm gear fully clockwise to move the heads to the innermost track and insert the cardboard shipping disk in the drive. This will prevent the opposing read/write heads from striking each other in transit.

Re-installation:

To re-install the Disk Drive, reverse the removal procedure.

5.5.4 EMI FILTER BOX

Removal:

1. Remove cover per section 5.5.1.

2. Disconnect two wires from lugs at top of EMI filter box.

3. Remove four screws securing EMI filter box to rear panel.

4. Pull filter box away from rear panel and rest it on work surface.

The filter box can be separated sufficiently from the Archiver Master for most service activity though it is still connected to the master by a grounding wire. To completely remove the EMI filter box, disconnect the ground wire from either the Archiver Master or EMI filter box grounding stud.

Re-installation:

To re-install the EMI filter box, reverse the removal procedure.

5.5.5 CHASSIS AND MOTHERBOARD

If it is determined that the Motherboard needs replacement, order the entire chassis with the Motherboard under the appropriate part number as listed in section 7 of this manual. The entire chassis with the Motherboard installed is supplied, less the AWS PCAs and Disk Drive.

CHAPTER 6

ILLUSTRATED PARTS BREAKDOWN

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 6

ILLUSTRATED PARTS BREAKDOWN

6.1 INTRODUCTION

This chapter contains illustrated parts breakdowns (IPBs) for the Archiver Master and Terminals associated with the VS/WP/OIS Archiving Workstations. The illustrations identify the subassemblies referred to throughout the manual in the various maintenance procedures. The part numbers of each of these items are given, along with identification of parts common or unique to the VS and WP/OIS models of the AWS. RSL items are indicated with an asterisk.

6.2 LIST OF ILLUSTRATED PARTS BREAKDOWNS

Title	Figure	Table
Archiver Master	6-1	6-1
5506 Terminal	6-2	6-2
5730 Terminal	6-3	6-3

6.3 TOP ASSEMBLY PART NUMBERS

Top assembly part numbers for the models covered in this manual are listed below.

Model Number	Top Assembly Number, 60 Hz	Top Assembly Number, 50 Hz
2266C-1	176-5180	156-5180
2266C-3	176-5181	156-5181
2266S-1	176-5182	156-5182
2266S-2	176-5183	156-5183
2266S-3	176-5184	156-5184
2276C-1	176-5178	156-5178
2276C-3	176-5179	156-5179
AWS-1	176-5050	156-5050
AWS-4	176-5110	156-5110
5740	187-9359	167-9359

TABLE 6-1, ARCHIVER MASTER (1 of 3)

AWS INTERNAL VIEW 1

ITEM NO.	PART NO.	DESCRIPTION
*1	400-1001	FAN
2	449-0101	FAN GUARD
3	270-0583	FILTER BOX ASSY
4	279-1039	BOTTOM PAN ASSY

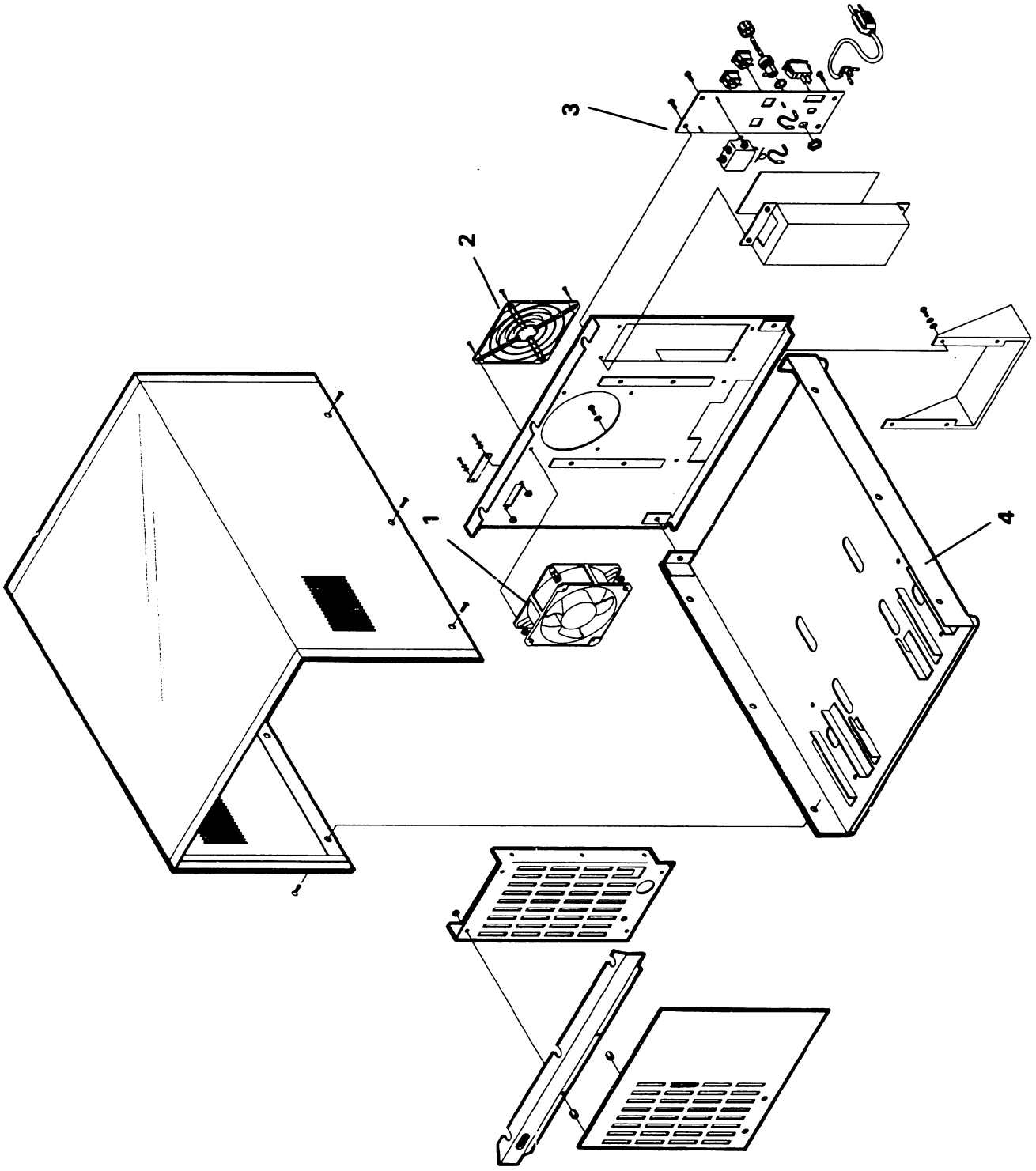


Figure 6-1 Archiver Master (1 of 3)

TABLE 6-1, ARCHIVER MASTER (2 of 3)

AWS INTERNAL VIEW 2

ITEM NO.	PART NO.	DESCRIPTION
*1	210-7744	DATA LINK
*1	210-7545	CPU
*1	210-7414	SOFT SECTOR VS
*1	210-7843	HARD SECTOR VS
*1	210-7543	HARD SECTOR OIS
*2	210-7615	MOTHER BOARD VS
*2	210-7546	MOTHER BOARD OIS
*3	451-1152	CHASSIS,ELECTRONICS
*4	725-0053-91	FLOPPY DISK DOOR KIT
*5	278-4021	DISK,FLOPPY 8" VS (60HZ)
*5	278-4021-1	DISK,FLOPPY 8" VS (50HZ)
*5	278-4003	DISK,FLOPPY 8" OIS (60HZ)
*5	278-4003-1	DISK,FLOPPY 8" OIS (50HZ)
*	270-0581	CHASSIS ASSY (OIS)
*	270-0678	CHASSIS ASSY (VS)
*	220-3120	DISK I/O CABLE (VS)
*	220-3011	DISK I/O CABLE (OIS)

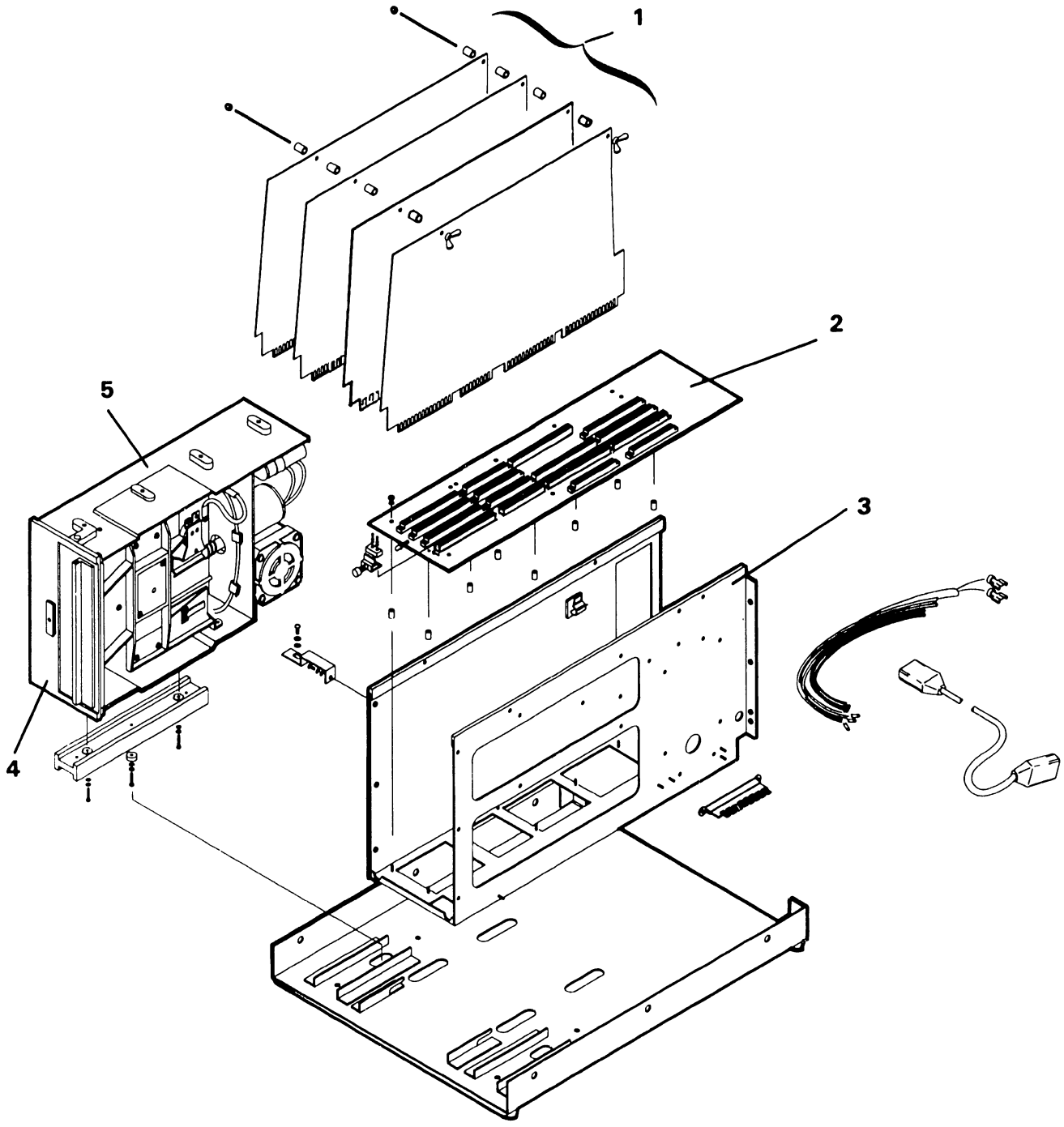


Figure 6-1 Archiver Master (2 of 3)

TABLE 6-1, ARCHIVER MASTER (3 of 3)

AWS INTERNAL VIEW 3

ITEM NO.	PART NO.	DESCRIPTION
1	300-3069	CAP 27K UF
2	300-3067	CAP 12K UF
3	300-3050	CAP 12K UF
*4	210-7316	PCA,REGULATOR
*5	270-0551	HEATSINK HARNESS ASSY

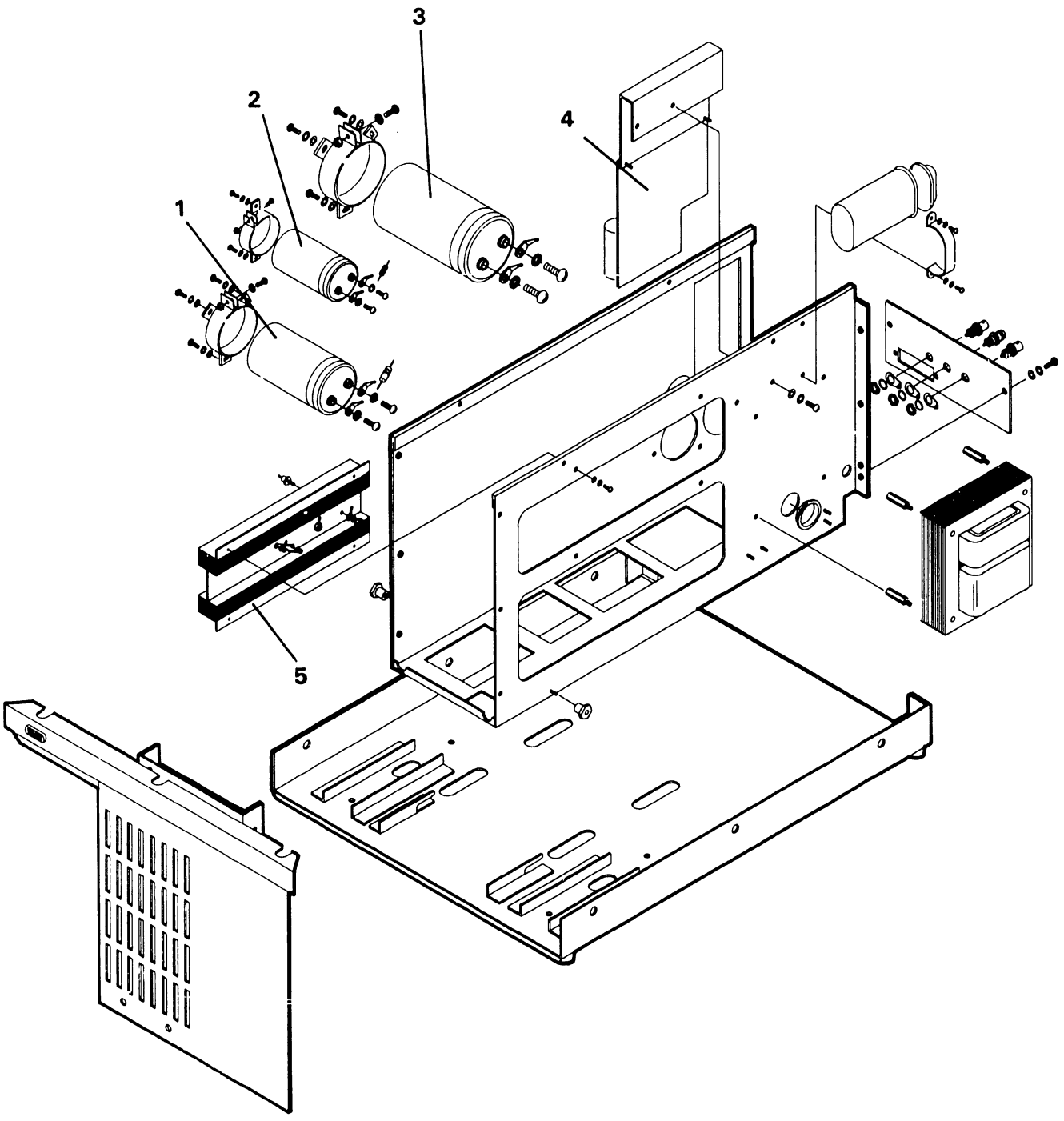


Figure 6-1 Archiver Master (3 of 3)

TABLE 6-2, 5506 TERMINAL (1 of 2)

AWS WORKSTATION (COVERS ASSEMBLY)

ITEM NO.	PART NO.	DESCRIPTION
1	449-0143S	COVER, AWS (SLOT)
1	449-0606	COVER,(FCC)
1	449-0460	COVER,CLOSED VENT
2	615-0398	FUNCTION STRIP
3		FUNCTION STRIP
4	452-2372	FINISHING PLATE (VS)
4	452-1081	FINISHING PLATE (OIS W/NUMERIC KP)
4	452-1092	FINISHING PLATE (OIS)
5	449-0459	12" CRT BEZEL
6	449-0548	PLATE WANG LOGO
7	655-0157	KNOB ALCO
8	652-0036	NUT SM. PAT.3/8"-32
9	653-0022	WASHER 3/8 INT.TH.
10	336-0032	BRIGHTNESS POT
10	336-0035	CONTRAST POT
11	654-1185	SOCKET
12	279-0509	CLICKER ASSY (NOT SHOWN)
12	325-2450	SWITCH,HALL EFFECT 4A2B
12	325-2451	SWITCH,HALL EFFECT 4B2K
12	325-2452	SWITCH,HALL EFFECT 4A2K
12	325-2453	SWITCH,HALL EFFECT 4B2B
12	325-2454	SWITCH,HALL EFFECT 4B3K
12	325-2455	SWITCH,HALL EFFECT 4B3A
12	370-0004	LAMP,WHITE
13	279-1026	BASE ASSY.
13	279-1038	BASE ASSY,(FCC)
14	271-1126	KEYBOARD (VS-DP)
14	271-1155	KEYBOARD (VS-COMBINED)
14	271-1242	KEYBOARD (OIS-STANDARD)
14	271-1243	KEYBOARD (OIS-NUMERIC KP)

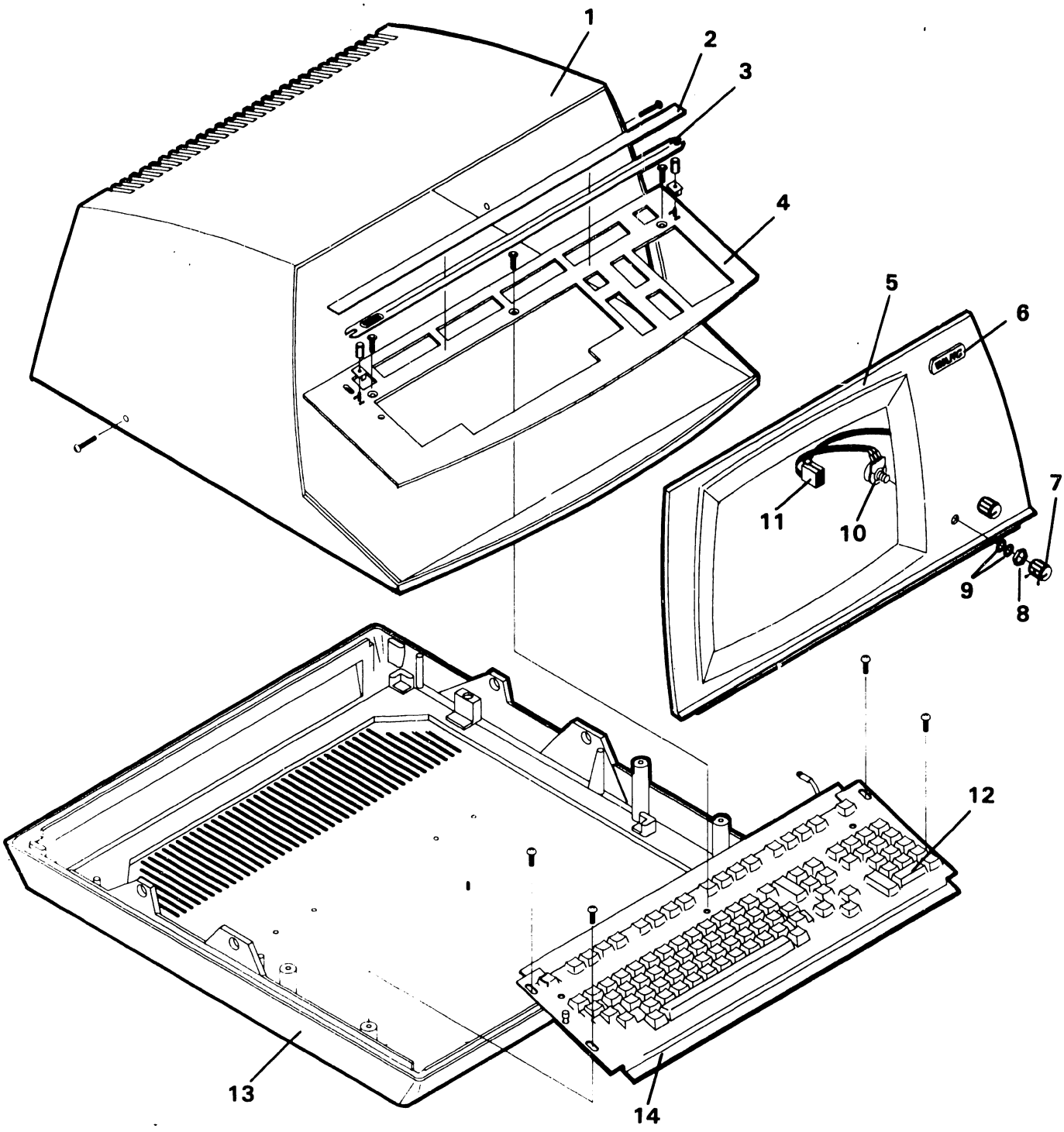


Figure 6-2 5506 Terminal (1 of 2)

TABLE 6-2, 5506 TERMINAL (2 of 2)

AWS WORKSTATION (CHASSIS ASSEMBLY)

ITEM NO.	PART NO.	DESCRIPTION
1	451-4473	SUPPORT BRACKET
2	451-3857	SIDE PANEL(R.H.)
3	651-0037	#8X3/8"SLTD HEX S.T. SCREW
4	465-1643	GROUNDING SPRING
5	651-0037	#8X3/8" SLTD HEX S.T. SCREW
6	270-3092	DEFLECTION YOKE
7	340-0108	CRT
8	651-0053	#10X3/8" HEX S.T. SCREW
9	210-7456	PCA 12" MONITOR ELEC.
10	451-1100	CHASSIS,CRT
11	350-2073	ANODE CONNECTOR
12	380-3011	20KV DIODE
13	270-3104	FLYBACK TRANSFORMER ASSY.
14	462-0413	SPACERS
15	451-4472	NECKSAVER BRACKET
16	478-0448	NECKSAVER BRACKET INSULATOR
17	451-3856	SIDE PANEL(L.H.)
18	452-4042	CARD GUIDE
19	410-2005	LINE FILTER,5 AMP CORCOM 5K1
20	320-0300	SPEAKER 3" 8 OHM
21	451-3919	5595-4 REAR PANEL
22	459-3919	GND STATIC REAR PANEL
23	220-1076	POWER CORD ASSY.
24	360-1025-SB	FUSE 3.0 AMP 250V
24	360-1006-SB	.6A FUSE
*25	360-1031	FUSE HOLDER 90 DEGREE CONTACT
26	360-9000	RUBBER WASHER
27	360-9003	LOCK WASHER
28	360-9002	HEX NUT
29	325-0033	TOGGLE SWITCH
30	336-0033	POT
31	336-0034	POT
32	220-3086	RIBBON CABLE
33	220-3085	RIBBON CABLE/RS/232
	270-0447	REAR PANEL ASSY WITH 7313 PCA
	210-7313	CRT JUNCTION PCA
	270-0372	12" MONITOR ASSY WITH 7456 PCA
	*270-0371	MONITOR PS WITH 7455 PCA
	*210-7455	REG. PCA

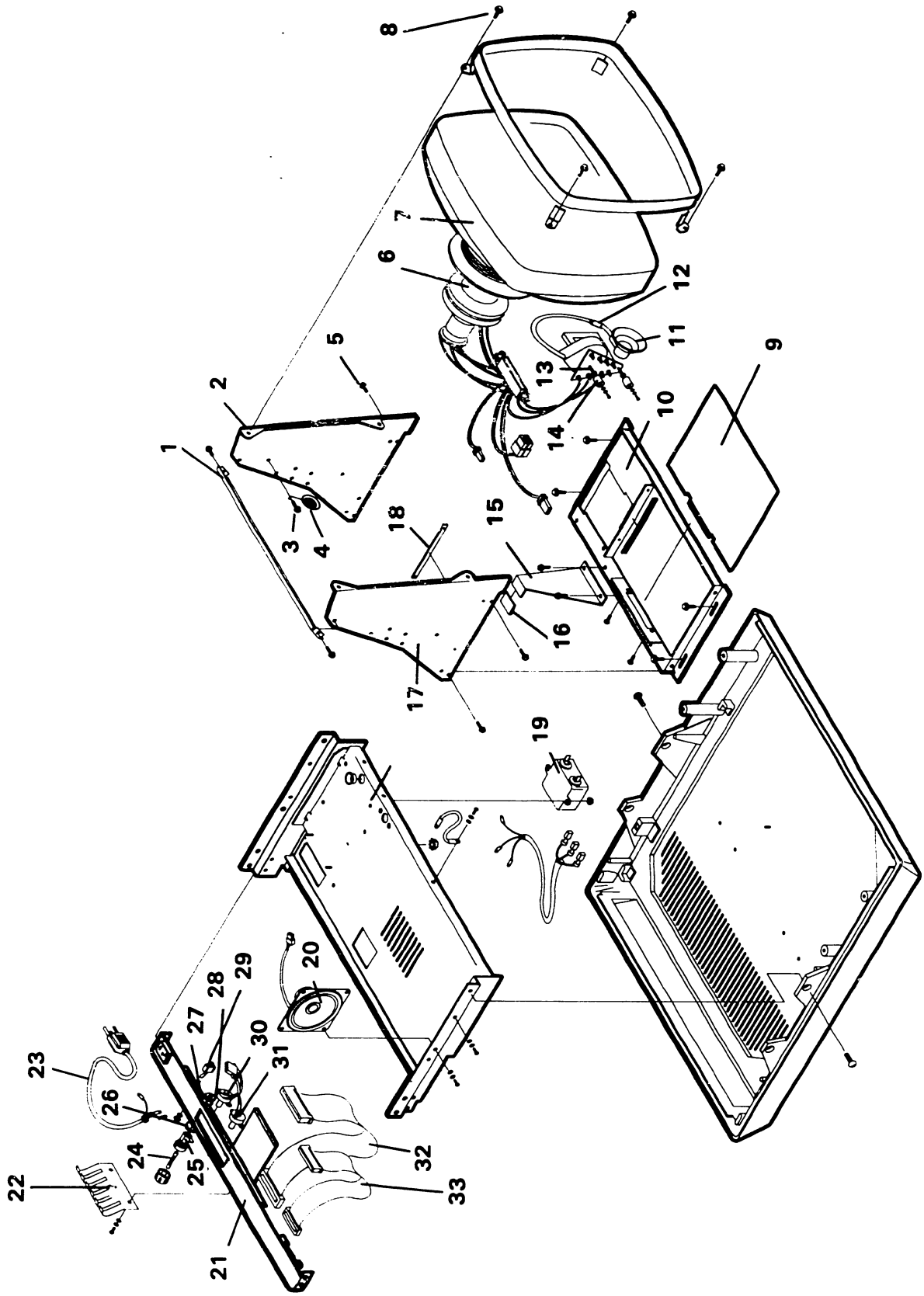


Figure 6-2 5506 Terminal (2 of 2)

TABLE 6-3, 5730 TERMINAL (1 of 2)

5730 TERMINAL INTERNAL VIEW 1

ITEM NO.	PART NO.	DESCRIPTION
*1	279-0491	CRT & BEZEL ASSY
*2	210-7456	MONITOR PCA
*3	449-0442	BASE,COVER
	271-1243	KEYBOARD,STANDARD W/NUMERIC KEYPAD
	271-1242	KEYBOARD,STANDARD
	271-1245	KEYBOARD,EXPANDED

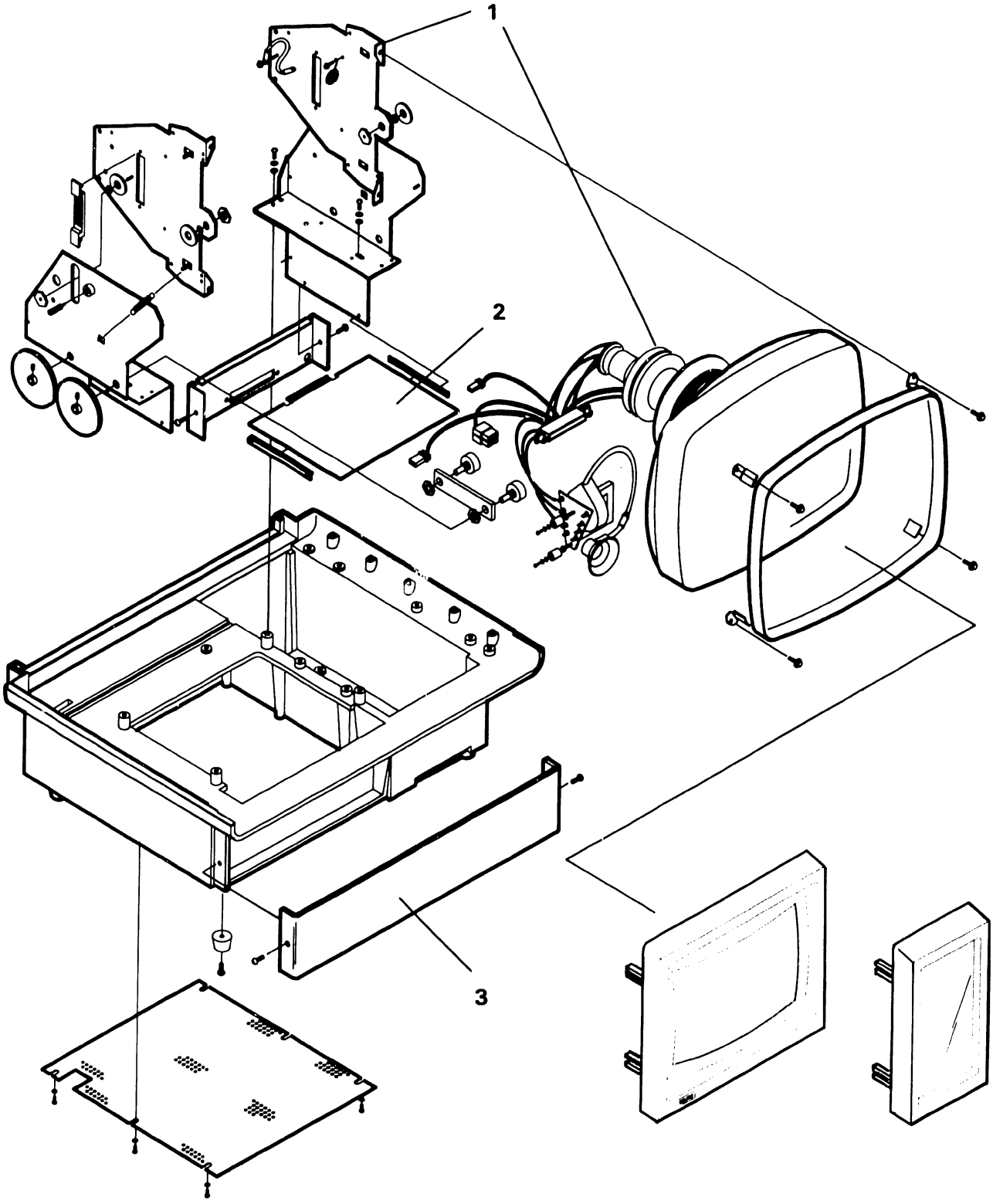


Figure 6-3 5730 Terminal (1 of 2)

TABLE 6-3, 5730 TERMINAL (2 of 2)

5730 TERMINAL INTERNAL VIEW 3

ITEM NO.	PART NO.	DESCRIPTION
1	270-0371	POWER SUPPLY
2	279-1025	BASE ASSY
3	270-3215	FILTER ASSY
4	210-7313	PCA REGULATOR
5	279-0507	REAR PANEL
6	360-1031-SB	FUSE 3.0 SB

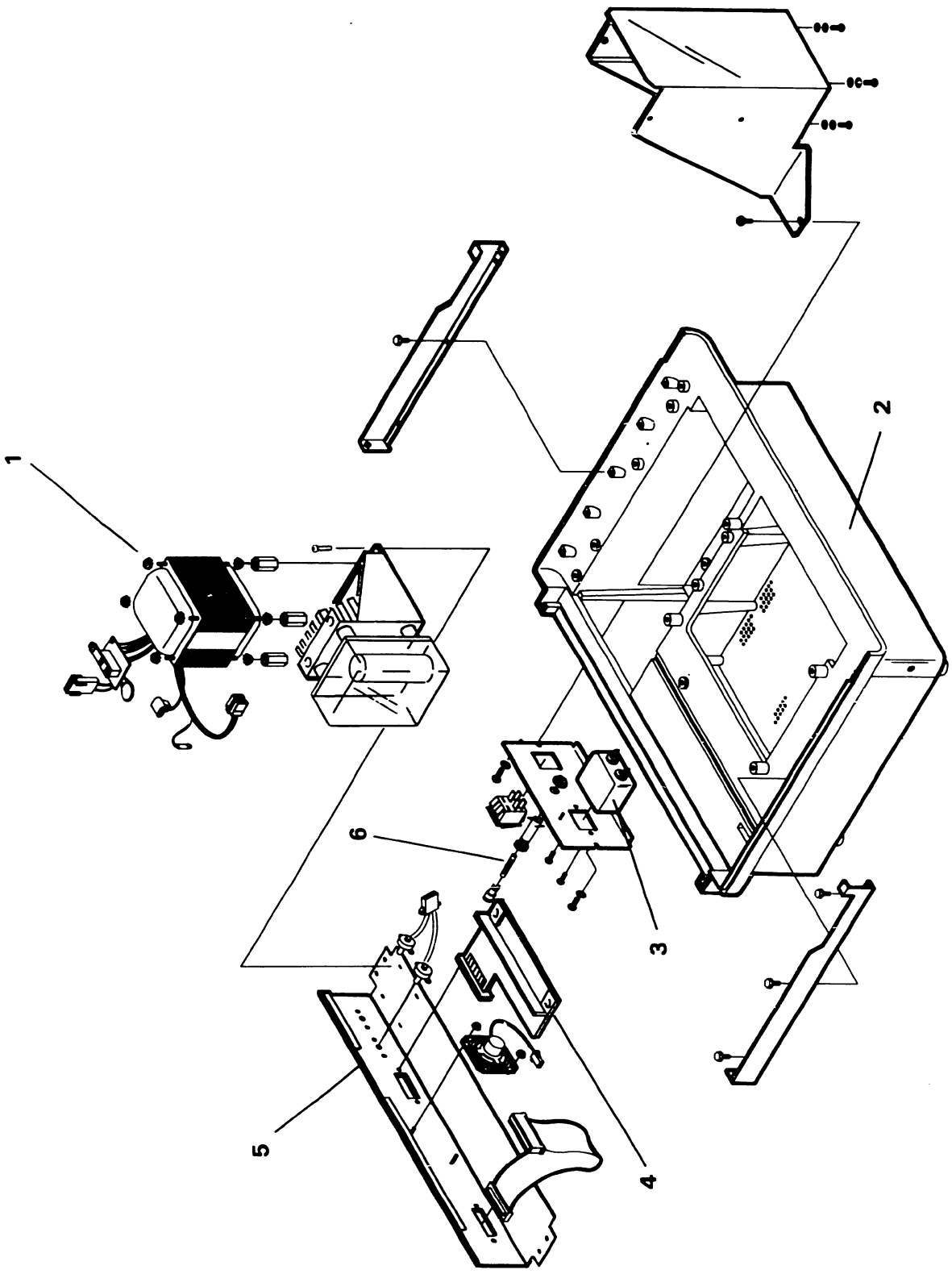


Figure 6-3 5730 Terminal (2 of 2)

CHAPTER 7

TROUBLE-SHOOTING

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER 7

TROUBLESHOOTING

7.1 INTRODUCTION

This chapter contains troubleshooting information for both the VS AWS (section 7.3) and the WP/OIS AWS (section 7.4). General checks common to all AWS models are contained in section 7.2.

7.2 GENERAL TROUBLESHOOTING CHECKS

Before proceeding with the more in-depth troubleshooting outlined in sections 7.3 or 7.4, make a careful visual inspection of the Terminal and the Archiving Master and check the items listed below.

- Are the ac power cords of the units securely plugged into their power outlets?
- Are the VIDEO and KEYBOARD cables between the Terminal and the Archiving Master securely connected to their respective connectors?
- Is the data link dual-coaxial cable from the Archiving Master to the Master CPU securely connected at both units?
- Are the PCAs in the Archiving Master firmly seated in their respective sockets?
- Are the Disk Drive cables in the Archiving Master firmly seated in their respective sockets?
- Is the jumper on the motherboard between connector 1 pin B and connector one pin P removed? If not, remove it.

7.3 VS AWS TROUBLESHOOTING

Troubleshooting for the VS AWS is provided in flowchart form in Figure 7-1.

7.4 WP/OIS AWS TROUBLESHOOTING

Troubleshooting for the WP/OIS AWS is provided in flowchart form in Figure 7-2, and in the following subsections dealing with symptoms related to the Data Link/Memory and CRT/CPU PCAs.

Data Link/Memory PCA Symptoms:

Symptoms that indicate 7744 PCA failure are generally related to workstation main memory or to communication with the system master (data link).

- No startup - blank screen
- LINE ERROR message on startup
- PARITY message on startup
- All "9"s displayed on screen - PROM trying to load. Correct switch setting. Switch 1 must be OFF.

CRT/CPU PCA Symptoms:

Symptoms that indicate a bad 7545 PCA are generally related to CPU, video, or keyboard functions. The board should be replaced when any of the problems listed here are encountered.

- Keyboard repeat keys function incorrectly
- Keyboard entry is erratic or absent
- Display is erratic or erroneous
- Video sync problems (try pot adjustments first)
- Intensity and character control (underline, etc) problems (try pot adjustments first)
- Beeper/clicker problems (also check speaker and speaker circuit)
- Faulty peripheral selection
- System program does not load

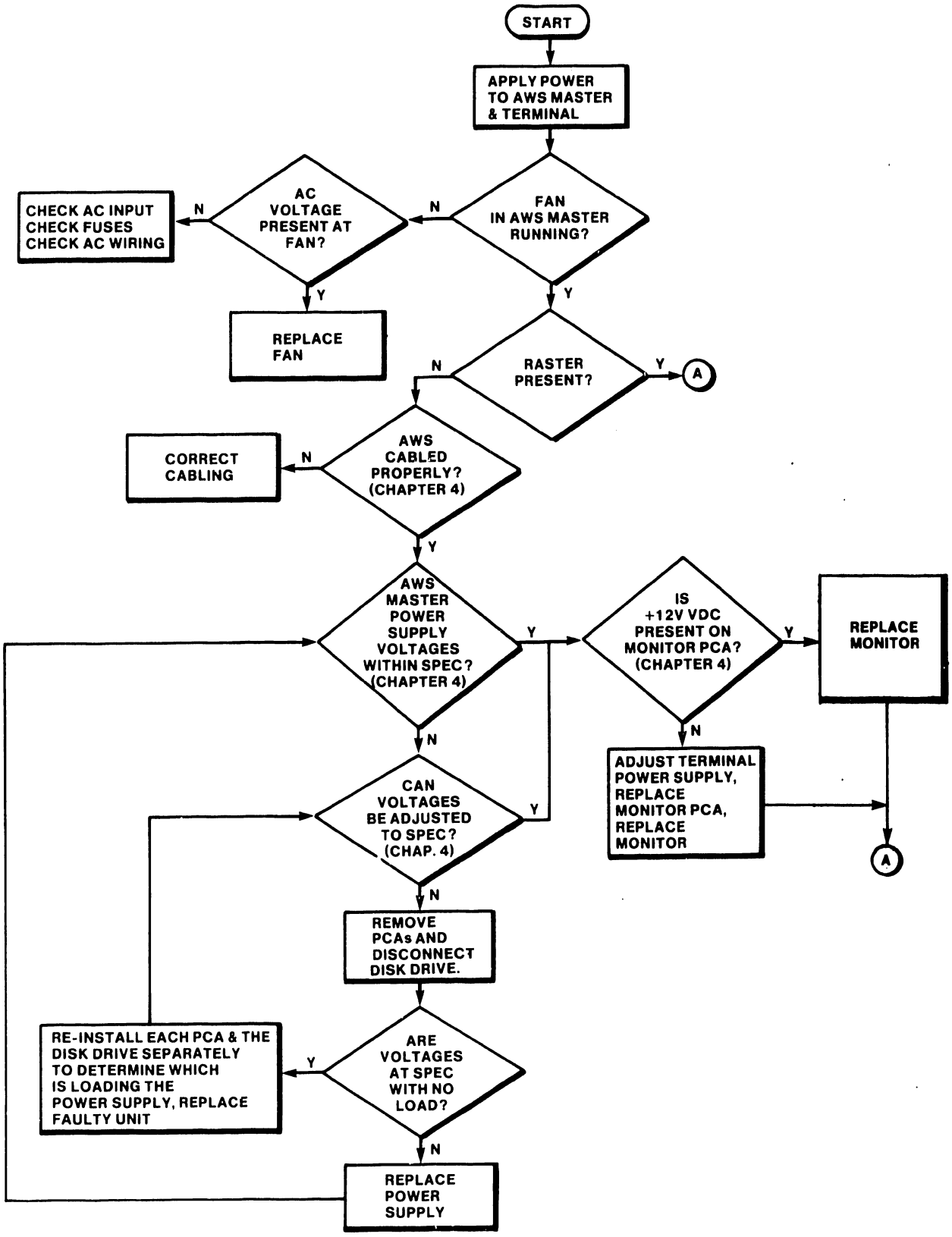


Figure 7-1 VS AWS Troubleshooting Flowchart
(Sheet 1 of 3)

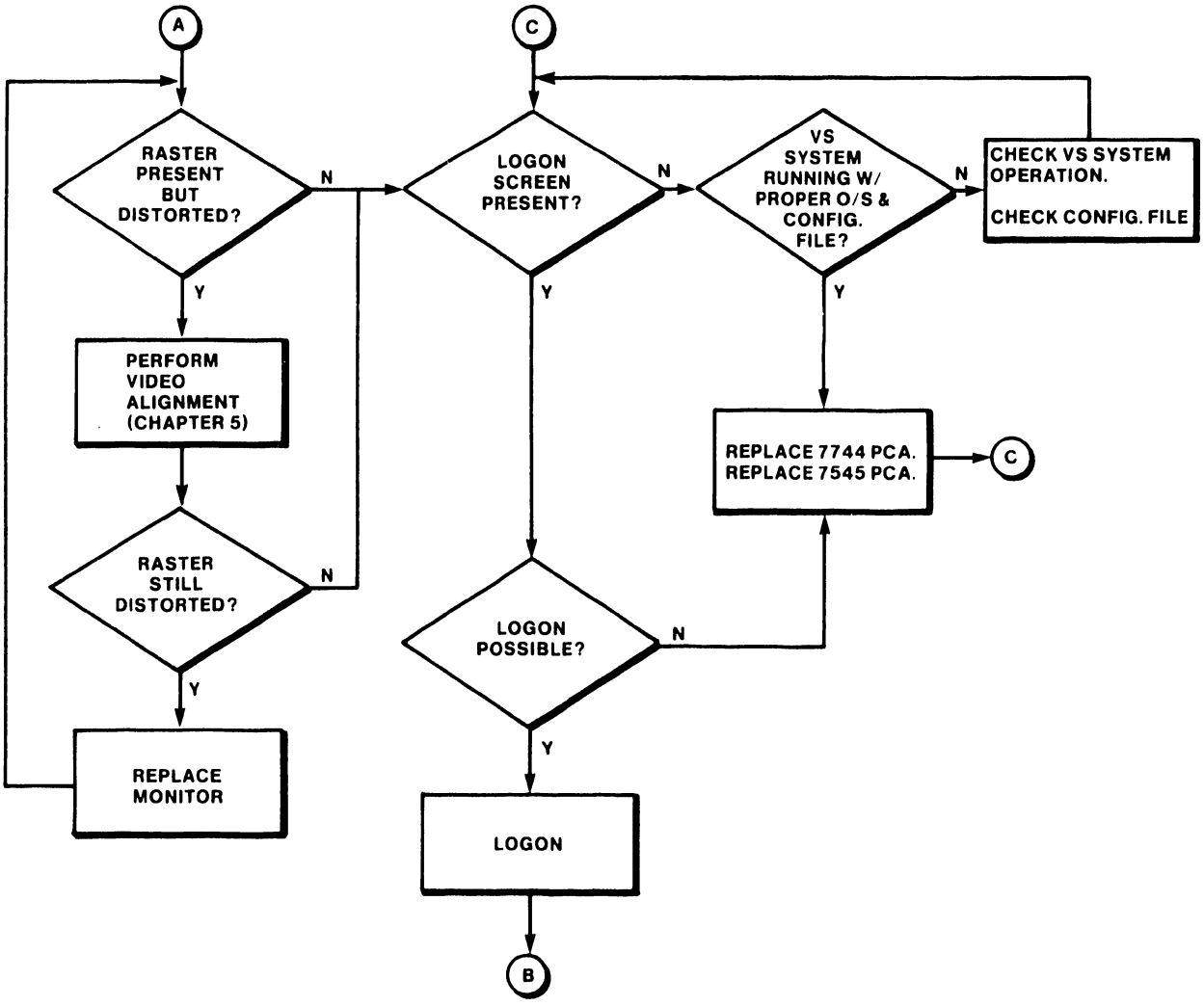


Figure 7-1 VS AWS Troubleshooting Flowchart
(Sheet 2 of 3)

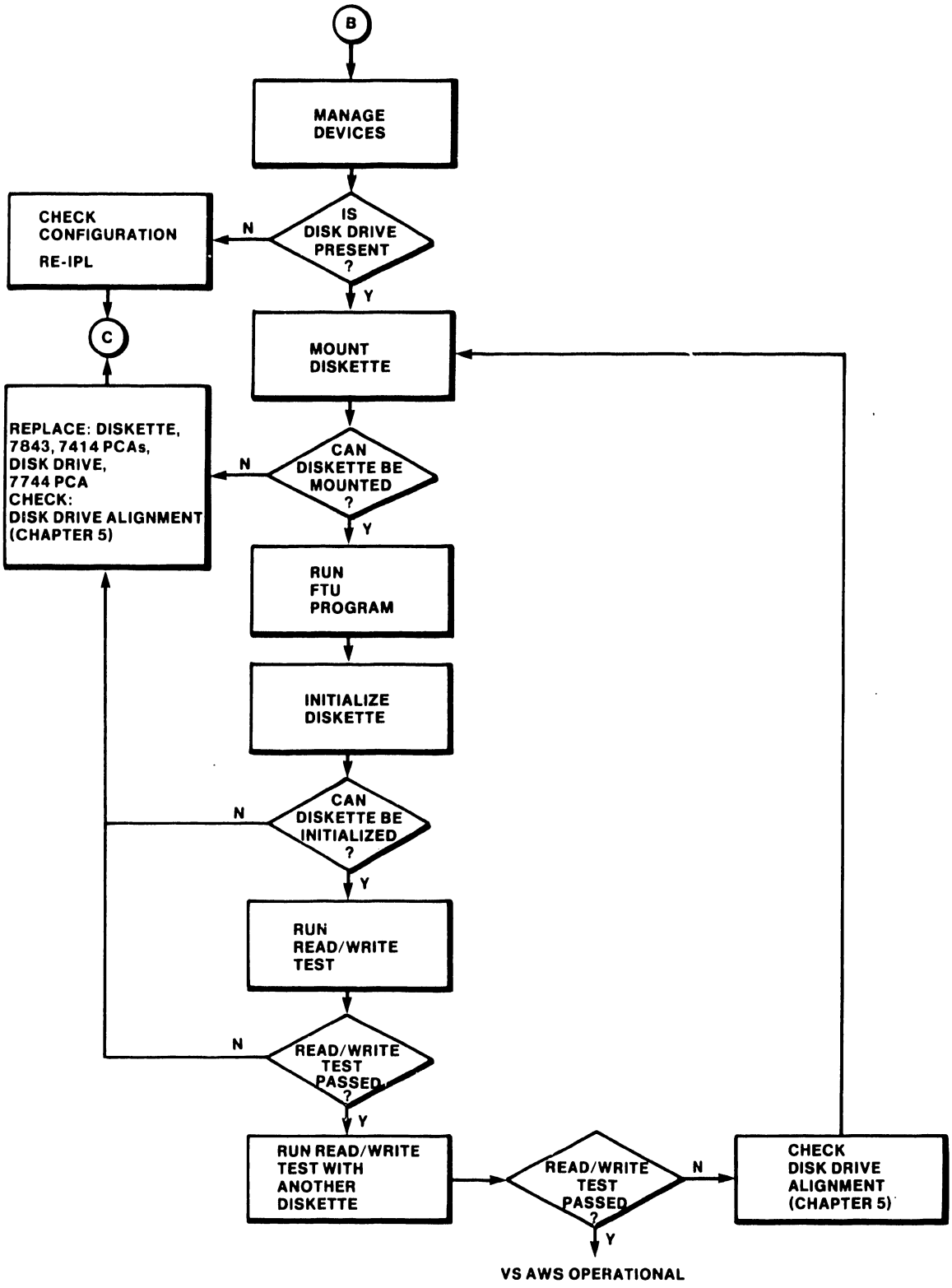


Figure 7-1 VS AWS Troubleshooting Flowchart
(Sheet 3 of 3)

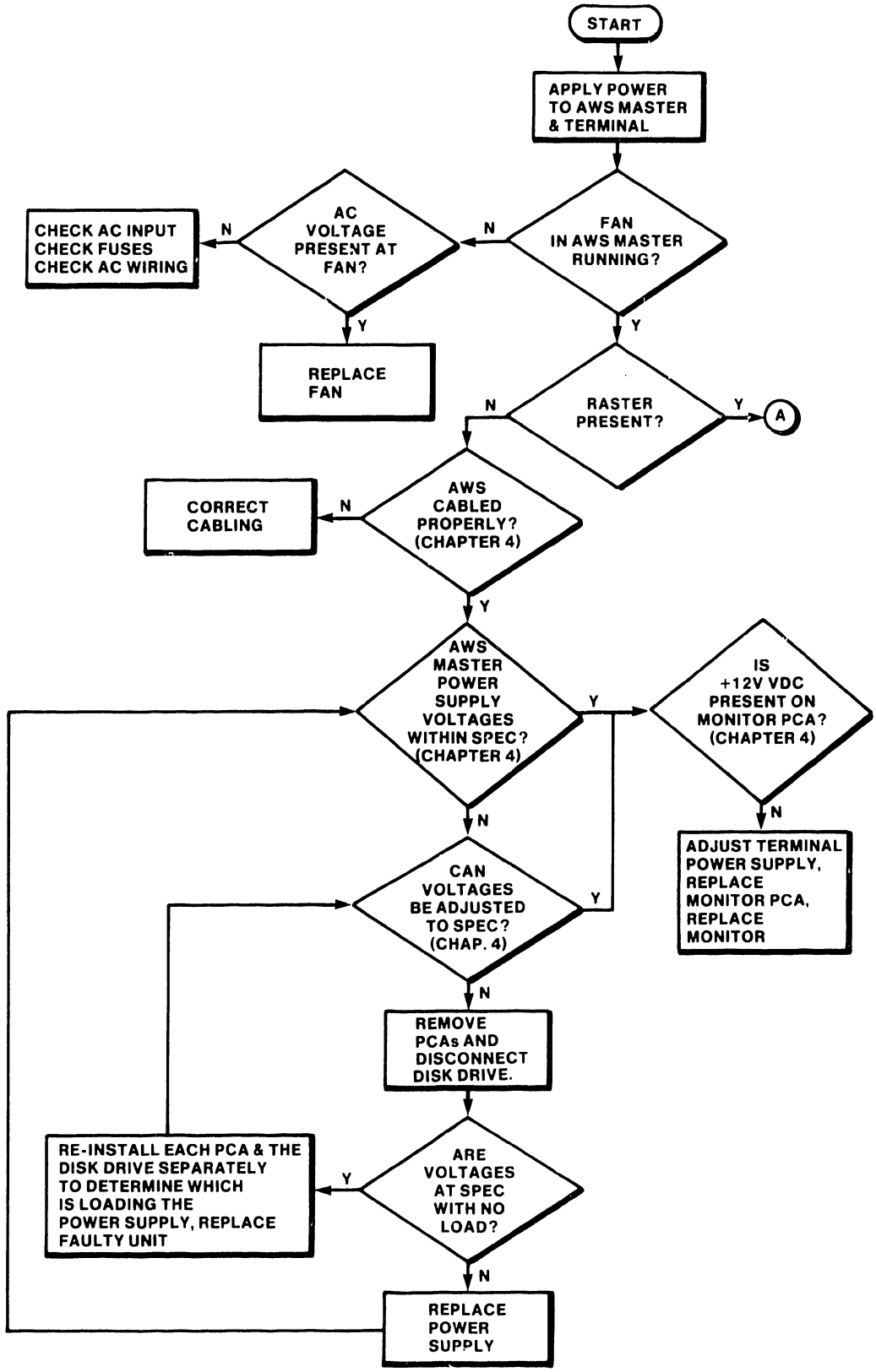


Figure 7-2 WP/OIS AWS Troubleshooting Flowchart
(Sheet 1 of 2)

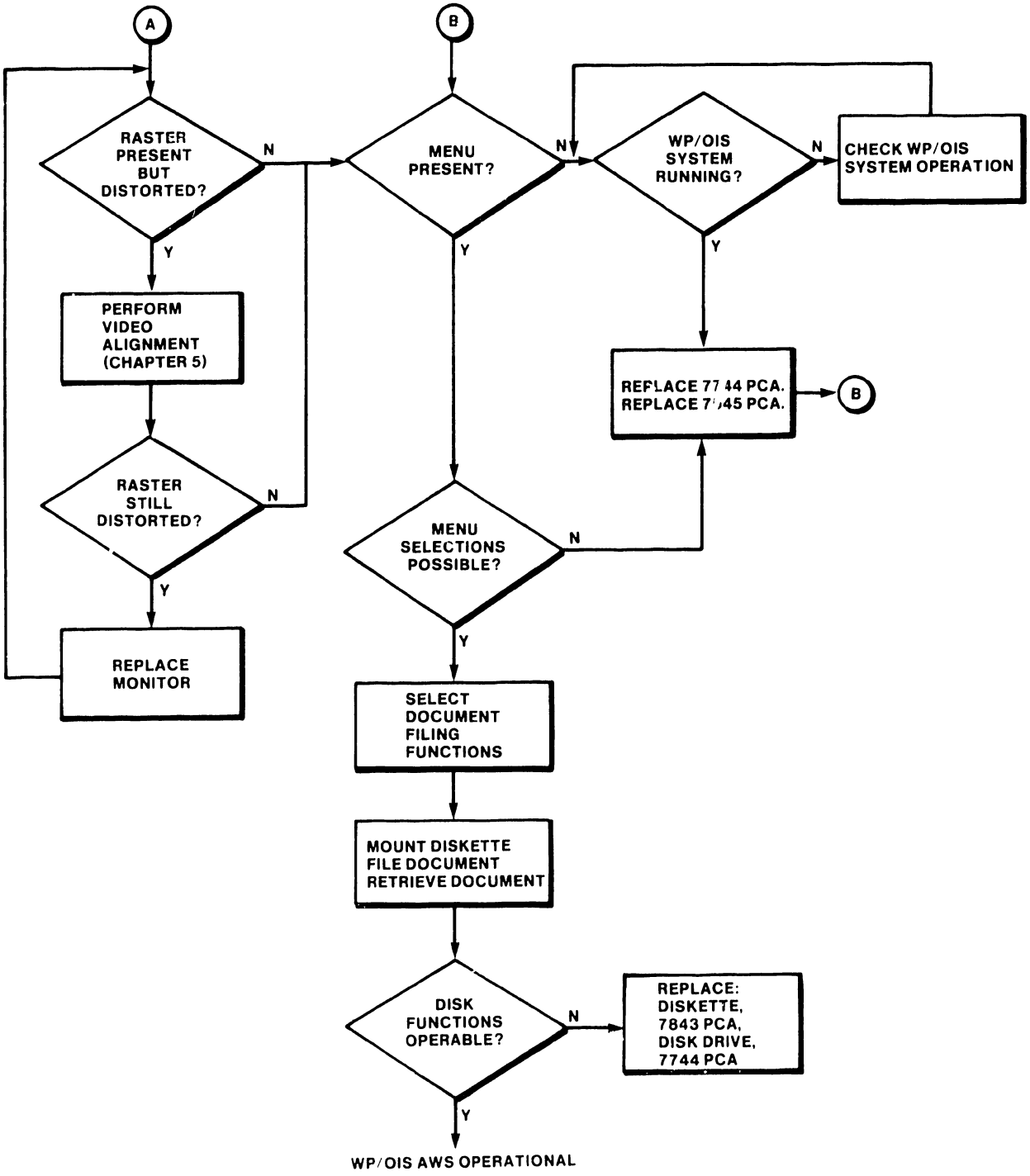


Figure 7-2 WP/OIS AWS Troubleshooting Flowchart
(Sheet 2 of 2)

APPENDIX A

TABLE OF CONTENTS

APPENDIX A

GLOSSARY OF MNEMONICS

MNEMONIC	DEFINITION
ACT	Active bit
ADL	Memory Address Latch
ADMX	Memory Address Multiplexer
ALU	Arithmetic Logic Unit
ARS	Active Read State
AMX	A-bus Multiplexer
AWS	Active Write State
BA	Bus Adapter
BALU	Binary Arithmetic Logic Unit
BCD	Binary Coded Decimal
BMX	B-bus Multiplexer
BNM	Branch-to-Next-Macro
BOP	Branch Operation
BRMX	Branch Multiplexer
CABF	'CM' Address Buffer
CAR	Current Address Register
CBL	C-bus Latch
CBMMX	C-bus/Main-Memory Data Multiplexer
CBn (CB0 - CB31)	C-bus (output) data
CC	Condition Code bit
CCMP	Continuous Comparator
CCNT	Continuous Counter
CDIBF	'CM' Data Input Buffer
CDOBF	'CM' Data Output Buffer
CDOMX	'CM' Data Output Multiplexer
CHBF	Current Half-word Buffer
CM	Control Memory
CMAL	'CM' Address Latch
CMBF	Control Memory Buffer
CMR	'CM' Register
CMX	C-bus Multiplexer
CMn	Control Memory bits: CM0 through CM47(?)
CTBC	Count To Be Compared
DALU	Decimal Arithmetic Logic Unit
DCA	Decimal Carry status bit
DEC	Decimal status bit
DTBF	Main Memory Data Buffer
DWD	Doubleword
ECR	External Condition Register
ECR	Write External Condition Register

MNEMONIC	DEFINITION
FLUB	File Length and User Block
GS	Group Select (field)
IAR	Indirect Address Register
IC	Instruction Counter
ICLD	Instruction Counter Load
IEM	Interrupt Enable Mask
INTM	Intermediate Register
IPC	Inter-Processor Communication
IREG	Indirect Register
IREG Counter	Indirect Register Counter
IREG MUX	Indirect Register Multiplexer
IREG1	Indirect Register #1
IREG2	Indirect Register #2
IRM	Interrupt Request Mask
LDA	Logical Device Address
LRU	Least Recently Used
M	Monitor (status flag bit)
M4BF	MDR4 Buffer
MAMX	MAR Multiplexer
MAR0	Memory Address Register #0
MAR1	Memory Address Register #1
MAR2	Memory Address Register #2
MBS1	Multiplication Byte Select; Multiplier Buffer Storage 1
MBS2	Multiplication Byte Select; Multiplier Buffer Storage 2
MDR0	Memory Data Register #0
MDR1	Memory Data Register #1
MDR2	Memory Data Register #2
MDR3	Memory Data Register #3
MDR4	Memory Data Register #4
MDRN	MDR Next Word
MDRN1	MDR Next Byte
MDRP	MDR Prior Word
MLPY	Multiplier Unit
MMPFT	Main Memory Page Frame Table
MMRD	(Main Memory Read) control word
MMn (MM0 - MM31)	Main Memory (output) data
MODE	Mode bit
MOP	Memory Operation (read or write); Multiply Operation
NAMX	Next Address Multiplexer
NOP	No (Memory) Operation

MNEMONIC	DEFINITION
OS	Operating System
OVF	Overflow
PB	Pagebreak Bit
PDA	Physical Device Address
PFN	Page Frame Number
PMR	Program Mask Register
PMX	PMR Multiplexer
POP	Process Operation
PROM	Programmable Read-Only Memory
PT	Page Table
R/C	Reference and Change (status bits)
RABF	Control Memory Address Buffer
RAM	Random Access Memory
RCM	Read Control Memory (Deliver byte to PMR)
RCT	Reference/Change (bit) Table
RDBF	Control Memory DAta Buffer
RECR	Read External Condition Register
RIPC	Read IPC Register; Read IPC Data
RMUX	Rotate Multiplexer; Rotating Multiplexer
ROM	Read-Only Memory
RP	Read Protect
SAI	Set Address Indirect
SAMX	Subroutine Address Multiplexer
SBC	System Bus Controller
SCA	Shift Carry status bit
SCR	Segment Control Register
SHFT	Data Shifter
SR	Shift Register
SSTK	Subroutine Address Stack
STKMX	Stack Address Multiplexer
T-RAM	Translation Random Access Memory
T-RAM	Translate Random Access Memory
TAL	T-RAM Address Latch
TC	Type-Code
TINT	Tester Interface
TRMX, TRMUX	T-RAM Multiplexer
VA	Virtual Address
VMAR	Virtual Memory Address Register
W1MX	WK1 Multiplexer
W2MX	WK2 Multiplexer
WCM	Write Control Memory (Set CM byte from PMR)
WIPC	Write IPC Register; Write IPC Data
WK1	Work Register #1

MNEMONIC	DEFINITION
WK1-A	Work Register 1--A-Bus
WK2	Work Register #2
WK2-A	Work Register 2--A-Bus
WMX1	WK1 Multiplexer
WMX2	WK2 Multiplexer
WP	Write Protect

APPENDIX B

TABLE OF CONTENTS

APPENDIX B VS SYSTEM APPLICATIONS

LIST OF ILLUSTRATIONS

APPENDIX B

VS SYSTEM APPLICATIONS

B-1 INTRODUCTION

This appendix contains information specific to Archiving Workstations used in VS systems. The areas covered are listed below.

Section B-2 System Interconnection, including typical system configurations, I/O port assignments, and SYSGEN considerations.

Section B-3 IPL-ing from the VS AWS on the VS-100.

B-2 SYSTEM INTERCONNECTION

The following information deals with special considerations in connecting a VS AWS to a VS Mainframe via an appropriate IOP. Use the information in addition to the installation information in Chapter 4 of this manual.

B-2.1 General

Two types of device interfacing - physical and logical - must be considered when interconnecting a VS AWS to its host VS Mainframe. The physical interface is the single coax pair required to connect the VS AWS to one of the serial IOP ports in the VS Mainframe.

The logical interface takes into consideration that although the VS AWS is connected with a single coax, it actually consists of two peripheral devices: a workstation and a disk drive. The VS operating system software will treat the workstation and disk drive as separate devices and therefore different device numbers must be assigned during the SYSGEN process to maintain this distinction. Further, the workstation must be assigned the lower of the two device numbers.

This enables the workstation to be used by one operator while the disk drive is copying a file for another operator. This type of operation is possible as long as the AWS is not in the word processing mode. (In the word processing mode, a different microcode file, @MCWP@, is loaded into the VS AWS. The disk drive is dedicated to the archiving workstation while it is being used for word processing. The drive can be used for archiving by the workstation but is no longer available to anyone else on the system. When the VS AWS is taken out of the word processing mode, the disk drive is available to all again.)

B-2.2 Typical System Configuration

Figure B-1 depicts a typical VS system configuration and illustrates both the physical and logical aspects of device interconnection. The overall system includes six peripheral devices: three VS AWS Systems, one 2246S Serial WS, one 2246C Combined WS, and one 5573 Bandprinter. All of these peripherals are interfaced to the VS Mainframe either through a 22V17 IOP (VS 60 and VS 80) or through a 22V27 IOP (VS 100).

Each of the six peripheral device cabinets shown in Figure B-1 is physically connected through a mainframe adapter plate, to an individual IOP port via a single paired-coax cable .

NOTE

The coax cables must be connected to consecutively-numbered IOP ports with no gaps between ports.

Even though each VS AWS is physically connected to one IOP port, it must be assigned two logical device addresses: one for its 2266S/C Workstation, and one for its 2270V1/V2/V3 Floppy Disk Drive.

NOTE

The 2266S/C workstation must always be assigned the lower of the two logical device numbers for the VS AWS, and the 2270V1/V2/V3 Floppy Disk Drive assigned the higher number

B-2.3 SYSGEN Considerations

Figure B-2 is a screen display showing the individual operating system device numbers assigned during SYSGEN for the hardware connected as shown in Figure B-1. The nine consecutive device numbers (0 through 8) correspond to the logical configuration of the hardware peripherals comprising the system.

Figure B-3 is the resultant screen displayed during a "Show Port Assignment" for the same hardware connected as shown in Figure B-1. The double listings for ports 0, 1, and 4 indicate a physical configuration of two peripheral devices interfacing over one coax line.

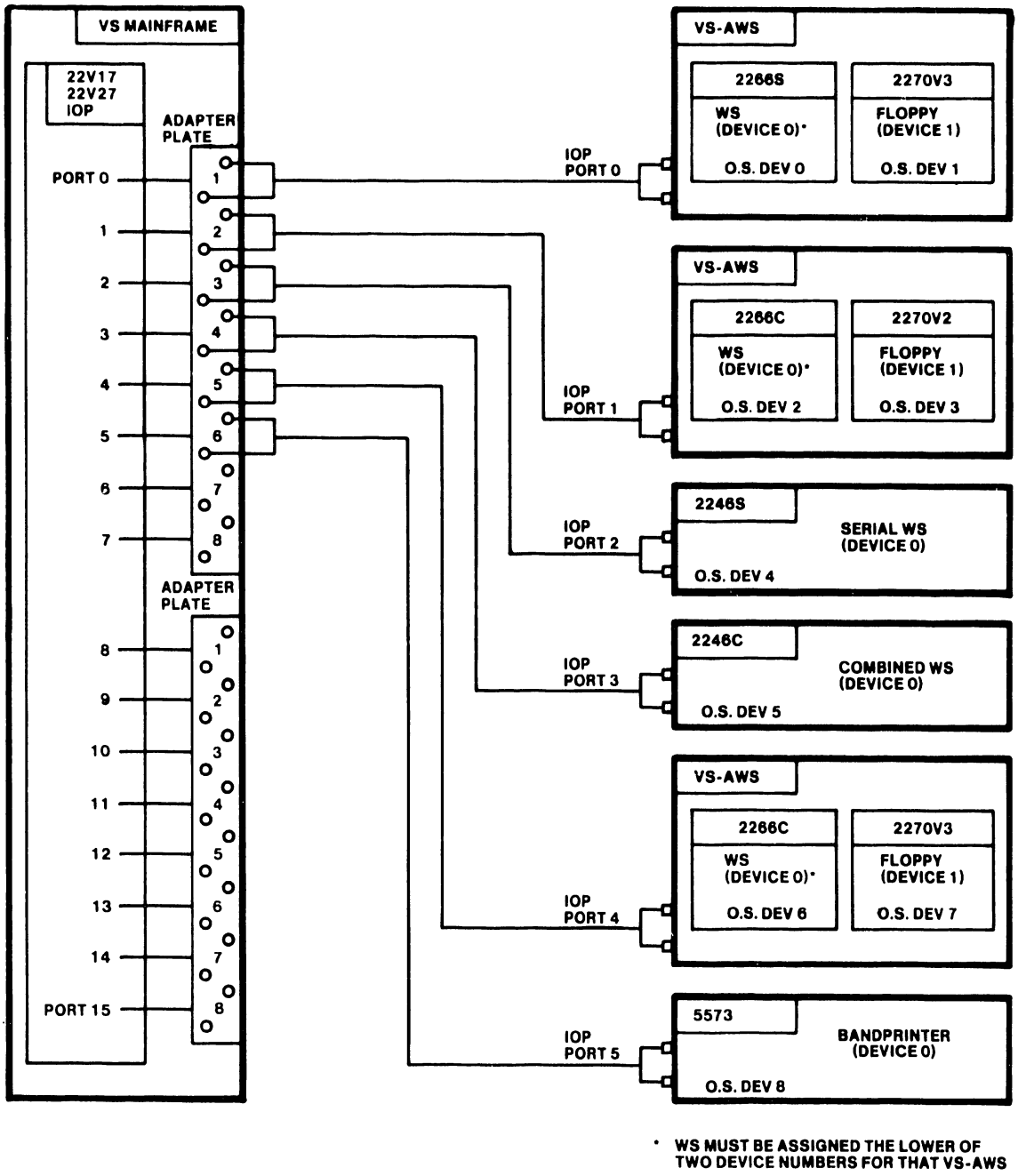


Figure B-1 Typical VS System Configuration

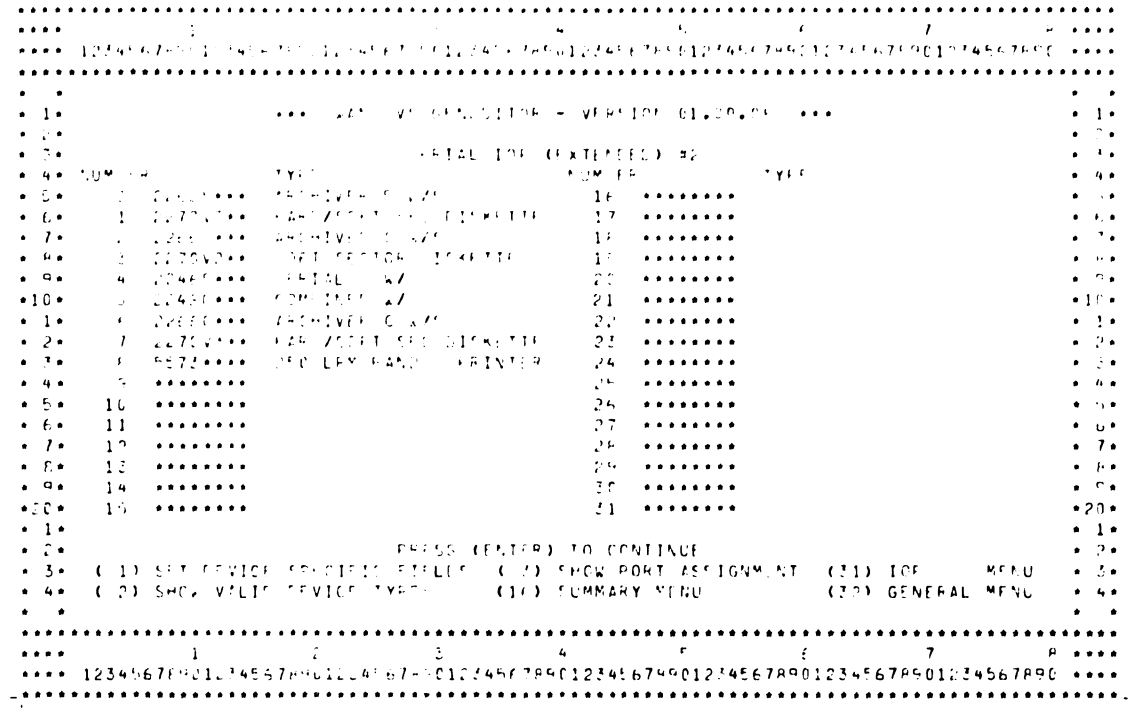


Figure B-2 Device Number Assignment Display Screen

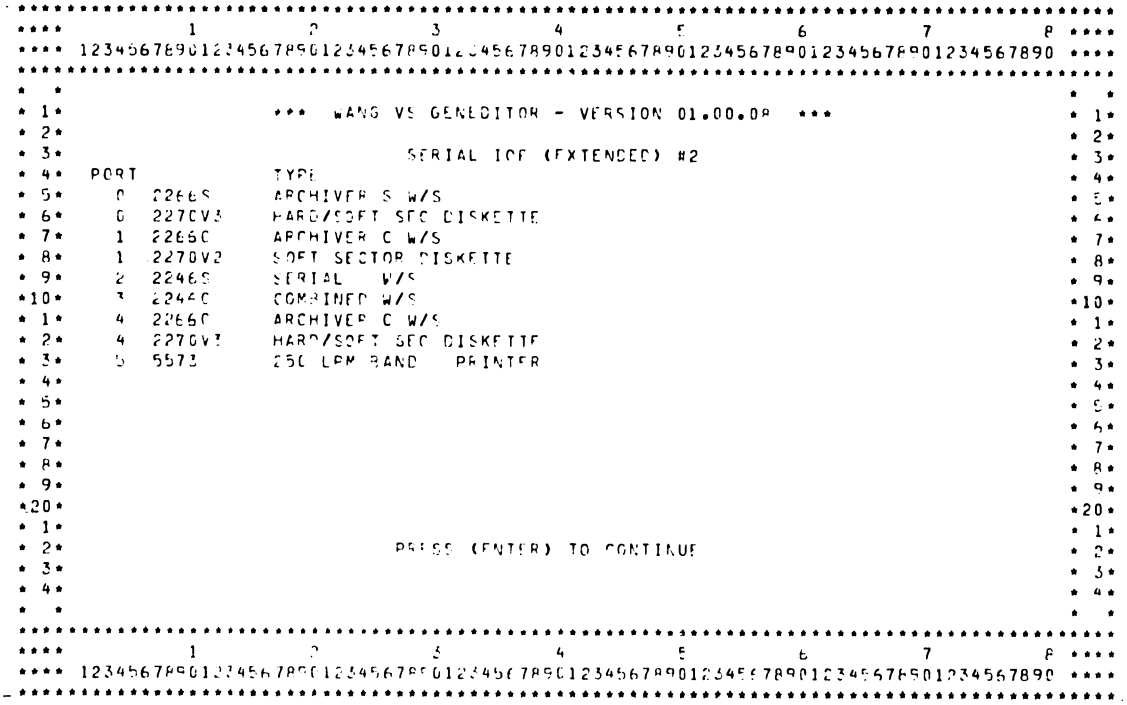


Figure B-3 Show Port Assignment Display Screen

B-3 IPL-ING FROM AWS ON VS-100

The VS AWS contains a bootstrap loader PROM which allows diagnostic loading from the VS AWS, completely bypassing the system disk drive. The purpose of the bootstrap operation is to allow the CE to start a VS System from the VS AWS itself. The bootstrap also allows an IPL from the VS AWS Floppy Diskette Drive in case it is not possible to do so from the system disk because of a disk drive or interface problem. This method of bootstrapping from the VS AWS assumes that this unit is fully operational.

The following ECOs must be installed in order to IPL from a VS-100 AWS.

- VS-100 CPU Microcode Revision 4.54.02 or above.
- VS-100/22V27 Serial IOP Microcode Revision 5.0.7.VSRM-0027-R3. PROM part numbers 378-2583 through 378-2589, rev 3; 378-3036, -3037, rev 3; 378-4301, rev 1.

B-3.1 Procedure

The procedure below should be followed when IPL-ing from the VS-100 AWS. Please note that the procedure requires use of a bootstrap diskette. The contents of a bootstrap diskette are defined along with the instructions for creating one in section B-3.4.

1. Connect the VS AWS to Port 0 of the 22V27 Serial IOP (set as IOP 0).
2. Insert a bootstrap diskette into the VS AWS floppy diskette drive. Refer to section B-3.4 to create such a diskette.
3. Press the LOAD button on the VS Mainframe CPU.
4. Observe the Terminal. It should display CONTROL MODE R 00. If not, AWS microcode needs to be loaded into the AWS. Proceed with step 5. If CONTROL MODE R 00 is displayed on the Terminal, proceed with the IPL-ing procedure at step 6.
5. Initiate a bootstrap operation by shorting the bootstrap etches on the Motherboard (refer to Figure B-4) and following the bootstrap prompts (see section B-3.5). When the bootstrap is complete, press the LOAD button on the VS Mainframe CPU. Observe the Terminal for the display, CONTROL MODE R 00.
6. Enter R 21 to IPL from Device 1 (VS AWS Floppy Diskette Drive).
7. Press ENTER. The program will execute as described in the sub-steps below.

   a. After issuing the command, a five second delay occurs. With the

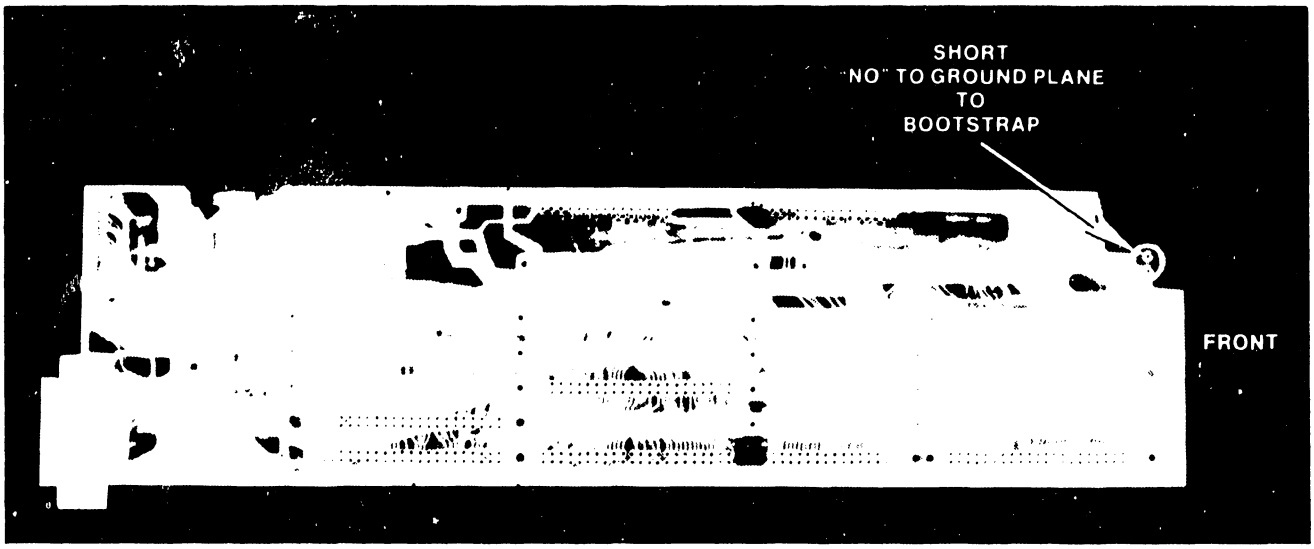


Figure B-4 Bootstrap Lands on Motherboard

disk present, the first I/O will begin and disk drive activity should be audible. The screen will remain with the R 21 message. (If no disk is present in the drive, the INT REQ message will be displayed after the delay.)

b. If neither case described in "a" above occurs after the five second delay, it is equivalent to an I/O ERROR message, although the message does not appear on the screen.

c. If disk operation has begun, it will be at one minute and fifteen seconds that the next I/O is issued to the diskette and the AWS screen clears.

d. At one minute and twenty seconds, the IPL screen appears on the AWS and IPL is completed. The standard diskette IPL text will load @SYS000@ from diskette library @SYSTEM@, and the standard diagnostic menu will appear on the Terminal CRT.

B-3.2 Bootstrap Pushbutton

To eliminate the possibility of an unintentional bootstrap, VS AWS Systems are presently being built with this button either disconnected or completely left out of the unit even though the access hole may still be there as shown in Figure 3-2. In order to initiate a bootstrap on these units, the CE must remove the cover and short the appropriate lands on the Motherboard as shown in Figure B-4.

B-3.3 Bootstrap Button Configurations

At present, three configurations of the bootstrap function can be found in VS AWS Systems. These configurations and some circuit wiring modifications that the CE should perform are described below.

Fully-Operational Button - If the VS AWS has a Bootstrap button that is connected to the motherboard, and the button is pressed while the system is operating, the VS AWS may be "lost" to the operating system and require an IPL to restore normal operation. For these systems, the CE should cut the common lead from the pushbutton to the motherboard to disable it.

Bootstrap Button Inoperable - If the VS AWS has a Bootstrap pushbutton which seems inoperable, the common lead may have been cut as described in the preceding paragraph; or the pushbutton itself may be defective. In either case, the CE should cut the common lead from the pushbutton to the motherboard.

No Bootstrap Pushbutton - A few early VS AWS systems had no pushbutton installed at all. To implement a bootstrap operation from one of these systems, short the etches shown on Figure B-4.

B-3.4 Creating a Bootstrap Diskette

The procedure for creating a bootstrap diskette is presented below. It should be executed beforehand on an operational VS system running software version 5.00.13 or later.

The bootstrap PROM on the 210-7744 PCB contains a program which can only load the first file found in the VTOC. This file, therefore, must be the microcode routine for the VS AWS (@MC2266S or @MC2266C). Either file will work, but, ideally it should correspond to the archiver in use with the system. If not, dots may appear on the screen in place of spaces, and certain keyboard keys - notably arrows - will be in error. The abnormal appearance of the screen display, however, will not impair the diagnostic testing routine.

NOTE

The DISKINIT program must be run first to ensure that the VTOC is empty. Do not scratch all files on a diskette and then copy @MC2266C onto it. This file may not end up as the first file in the VTOC.

1. Run DISKINIT to initialize either a hard or soft-sectored diskette, ideally one of each (volume name is optional).

2. Run COPY to copy file @MC2266C into Library @SYSTEM@ on the initialized diskette.

3. Copy file @SYS000@ from Library @DIAGSA@ into Library @SYSTEM@ on the diskette.

4. Copy file VS100MEM into Library @DIAGSA@ on the diskette.

5. Copy file FTU into Library @DIAGSA@ on the diskette.

B-3.5 Archiver Bootstrap Screens

The following screens are encountered during a bootstrap load of the archiver microcode:

Message 1: If the bootstrap button is pressed with no diskette mounted:

BOOTSTRAP: WAITING FOR A BOOTSTRAP FLOPPY!

Message 2: Once a bootstrap diskette has been mounted and the first file in the VTOC has been located, the following message indicates the file which is to be loaded by the bootstrap:

BOOTSTRAP: BOOTING FILE @MC2266S" IN LIBRARY "@SYSTEM@":

[PLEASE HIT (RET) TO PROCEED]

Message 3: Once the indicated file has been loaded into the Archiver, the following message prompts the user to begin execution by displaying the following message:

BOOTSTRAP: STARTING FILE "@MC2266S" IN LIBRARY "@SYSTEM@:

[PLEASE HIT (RET) TO PROCEED]

Message 4: If disk errors are encountered during the bootstrap process, the following message is displayed:

BOOTSTRAP: DISK ERRORS, CANNOT CONTINUE!

Message 5: If the diskette in an NL diskette, the "first" file block is unused, or if general VTOC errors are detected during the bootstrap process, the following message is displayed:

BOOTSTRAP: BAD VTOC ON BOOTSTRAP VOLUME!

APPENDIX C

TABLE OF CONTENTS

APPENDIX C

MODEL CONVERSIONS

Archiving Workstations can be converted to different models by implementation of various kits offered by Wang. As part of the procedure, a new model number is assigned to the converted unit. The new model number appears on a sticker which is affixed to the workstation to alert the CE that this particular unit was modified. A listing of each available "UJ" kit number and its corresponding model number change is listed below:

C-1 VS MODEL CONVERSIONS

UJ NUMBER	ORIGINAL MODEL NO.	NEW MODEL NO.
3038	2266S-3	2266C-3
3041	2266C-1	2266C-3
3041	2266S-1	2266S-3
3041	2276C-1	2276C-3
3042	2266S-2	2266S-3
3094	2266S-1	2266C-1
3095	2266S-1	2266C-3
3096	2266S-2	2266C-3
3135	2266C-1	2276C-1
3136	2266C-1	2276C-3
3137	2266C-3	2276C-3

C-2 WP/OIS MODEL CONVERSIONS

UJ NUMBER	ORIGINAL MODEL NO.	NEW MODEL NO.
1008	AWS-1	AWS-4
1008	AWS-1TC	AWS-4TC
1060	AWS-1	AWS-1TC
1060	AWS-4	AWS-4TC
1061	AWS-1	AWS-4TC

SCHE-
MATICS

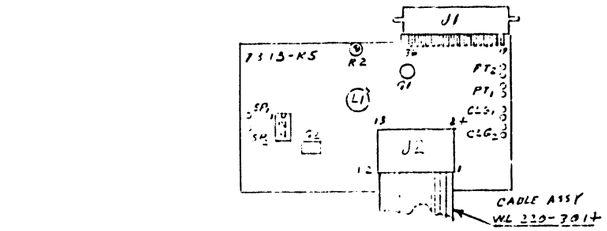
SCHEMATICS

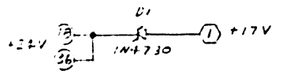
INTRODUCTION

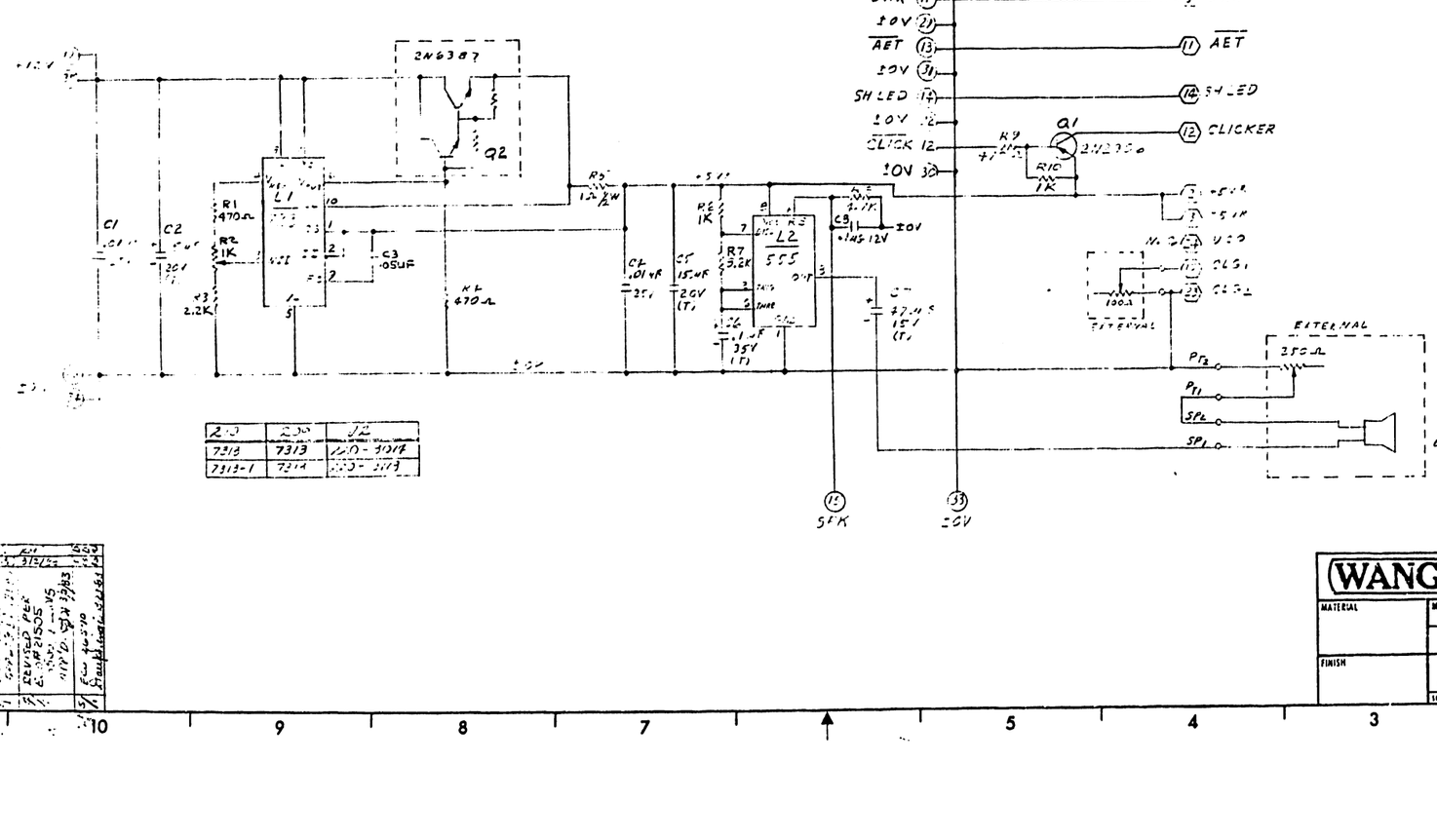
Schematic diagrams for the component parts of the Archiving Workstation are included in this section of the manual. Interconnection drawings are provided in the form of a Motherboard schematic for the VS AWS, and in the form of a wiring chart of the Motherboard for the WP/OIS VS. The schematics reflect the latest revisions at the time of printing.

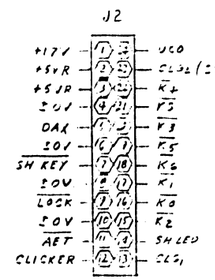
LISTING OF SCHEMATICS

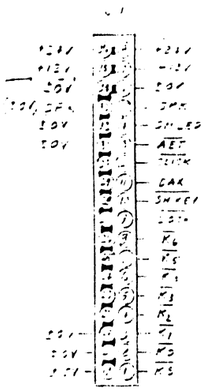
Drawing Number	Title	Comments
7313	CRT Junction Board PCA	Common
7316	114 Power Supply Regulator PCA	Common
7414-A	Soft-Sector Disk Controller PCA	VS Only
7455	Monitor Power Supply Regulator PCA	Common
7456	12" Monitor Electronics PCA	Common
7545-A, -C, -D	CPU/CRT PCA	Common
7543-A, -1A	Hard-Sector Disk Controller PCA	WP/OIS Only
7546	WP/OIS AWS Motherboard PCA	WP/OIS Only
7615	VS AWS Motherboard PCA	VS Only
7544/7744-2A-3A	Data Link 48K/64K Memory PCA	Common
7843-A, -1A	Hard-Sector Disk Controller PCA	VS Only











LOCATION	W.L. PART NO	TYPE
L1	376-0066	723
L2	376-0126	555

	W.L. PART NO	TYPE
R1,4,7	330-2047	470Ω 1/4W 5%
R2	330-1051	1K 1/4W 5%
R3	330-3053	2.2K 1/4W 5%
R5	331-0010	1K 1/2W 10%
R6,10	330-3011	1K 1/4W 5%
R7	330-3053	2.2K 1/4W 5%
R8	330-3078	2.7K 1/4W 5%
C1,2	1000-1103	.01µF 100V
C3,5	1000-1072	.05µF 100V
C4	1000-1103	.01µF 100V
C6	1000-1103	.01µF 100V
C7	1000-1103	.01µF 100V
C8	1000-1103	.01µF 100V
C1	1000-1103	.01µF 100V
Q1	375-1017	2N2907
Q2	375-1052	2N6387
D1	377-1001	IN4730
J1	340-1017	36 PIN EDGE
J2	SEE CHART	24 PIN EDGE

2.0	2.5	J2
7313	7313	220-3018
7313-1	7314	220-3019

NOTE:
ALL RES. ARE 1/4W 5%
UNLESS OTHERWISE SPECIFIED.

E.C.O.

REV	DESCRIPTION	DATE	APPROVED
A	REVISED PER E.C.O. M-1505	1-15-83	

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. (TYPICAL MADE U.S.A.)

MATERIAL

MODEL NO. 114
SEE ENGRG SPECIFICATIONS
No.

FINISH

TOL EX. AS NOTED
XX ± FRAC ±
XXX ± ANG ±
SCALE NAT CF 1

TITLE CRT CONTROLLER

220-7313 | D | 7313 | 5
MFG PART NUMBER | SIZE | DRAWING NUMBER | REV

DO NOT SCALE

TRANSFORMER WL # 410-0111 DWG. #5368-107

PRIMARY 115 VAC 60 HZ

A.C. OUTLETS (2) 654-0074

PRIMARY 220-240 VAC 50 HZ

A.C. OUTLETS (2) 654-0074

MOUNTED EXTERNAL

MOUNTED MOTHER BOARD

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN F S S	4/7?/	E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO 114	TITLE PS REGULATOR BOARD			
	SEE ENGRG SPECIFICATIONS No.				
FINISH	TOL ±0 AS NOTED .XX = FRAC = .XXX = ANG = FINISH	210-7316	D	7214	
	SCALE	SHT 1 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER

DO NOT SCALE

NMEMONIC	COORDINATE
AUTO RESET	1F1
BASE PT	1E6
PRIME	1G2
±0V	1B6
-5VR	1B1
+5VR	1D6
+5VS	1E6
-12VR	1B1
+12VR	1C1
15VAC1	1E6
15VAC2	1C6
+15VUR	1C6
+24VR	1G1
+28VUR	1F6
30VAC1	1G6
30VAC2	1G6

LOCATION	TYPE	SPARES
L5	LM339	1

SIGNAL-TERMINAL DESIGNATIONS, VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

+12VR	A	1	+12VR
-12VR	B	2	-12VR
PRIME	C	3	PRIME
+5VR	D	4	+5VR
+24VR	E	5	+24VR
-5VR	F	6	-5VR
±0V	H	7	±0V
AUTO RESET	J	8	+5VS
15 VAC 2	K	9	15 VAC 2
15 VAC 1	L	10	15 VAC 1
BASE PT.	M	11	BASE PT.
30 VAC 1	N	12	30 VAC 1
30 VAC 2	P	13	30 VAC 2
+15VUR	R	14	+15VUR
+28VUR	S	15	+28VUR

COMP SIDE — WIRING SIDE

NOTE:
1. ALL RESISTORS ARE 1/4W 5%
UNLESS OTHERWISE SPECIFIED

NO.	REVISION	BY	DATE	APPROVED
0	ORIGINATED PER ECO# 4715	FSS	4/21/75	
1/2	REVISED PER ECO# 4800 & 4801	FSS	7/18/75	
1/2	REVISED PER ECO# 4802	FSS	10/31/75	
2	ADD'L PER ECO# 10069	CMM	3-31-79	
3	ADD REQUIRED PER ECO# 11785	BSR	6/19/79	
4	REVISED PER ECO# 23505	BSR	2/3/83	
5	REVISED PER ECO# 23344	SSR	2/8/83	
6	REVISED PER ECO# 24278	EM-S	2-1-85	

E.REV. 1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	F.S.S.	4.21.75	E ENGR G. GILKS	5/6/75
CHK	G.D.	5/6/75	M ENGR	
			MFG ENGR	

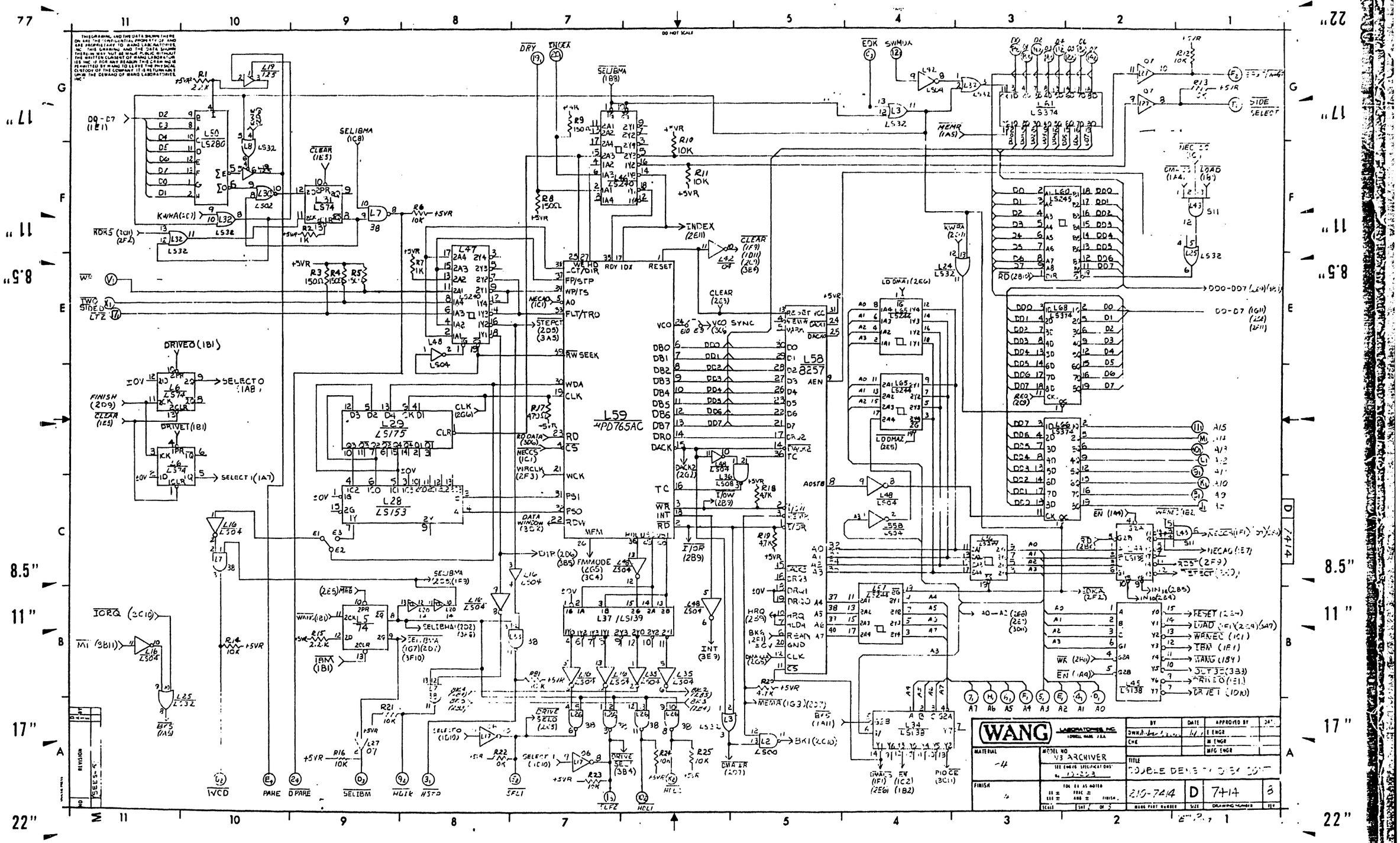
MATERIAL — MODEL NO. 114 — SEE ENGRG SPECIFICATIONS No. ____

FINISH — TOL. EX. AS NOTED .XX ± FRAC ± .XXX ± ANG. ± FINISH √

TITLE: PS REGULATOR BOARD

SCALE: 1ST 2 OF 2 — WANG PART NUMBER: 210-7316 — SIZE: D — DRAWING NUMBER: 7316 — REV: 6

D 7316


DRIVE0 (1B1)
DRIVE1 (1B1)
SELECT0 (1A8)
SELECT1 (1A7)
FINISH (2D9)
CLEAR (1E5)
DO - D7 (1E1)
KWHA(2C1)
RDRS (2H1) (2F2)
SELIBMA (1C8)
CLEAR (1E5)
DRY
INDEX
SELIBMA (1B8)
EOK
SWMDA
MEMR (1A5)
INDEX (2E11)
CLEAR (1F9) (1D11) (2C1) (3B4)
RESET
CLEAR (2C3)
WE HD -CT/DIR
RDY 1DX
FP/STP
WP/TS
A0
FLT/TRO
STEPCT (2D5) (3A5)
RW SEEK
WDA
CLK
RD
CS
WCK
PSI
PSO
RDW
DATA WINDOW (3D2)
WFM
DIP (2D6) (3B5)
FMMODE (2G5) (3C4)
INT (3E9)
VCO
VCO SYNC (3C6)
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DRQ
DACK
TC
WR
INT
RD
L58 8257
AEN
HRQ (2B9)
HLDA
READY
GND
CLK
CS
IOR (2B9)
IOW (2B9)
AD0-AD7
A8-A15
DACK2 (2G1)
DMA-LR (2D7)
BK1 (2C10)
BK0 (1E11)
IORQ (2C10)
MI (3B11)
RFS (1A5)
WCD
PARE
DPARE
SELIBM
WDTK
HSFD
SFLT
TCFF
HDLT
L59 μPD765AC
L28 LS153
L29 LS175
L37 /LS139
L58 8257
L67 LS244
L68 LS374
L69 LS244
L90 LS245
L34 LS139
L45 LS138
L46 LS374
L47 LS240
L48 LS04
L49 LS32
L50 LS280
L31 LS74
L6 LS74
DMA1 (2E6)
LDMA1
LDMA2
LDMA2 (2E5)
REQ (2D9)
RD (2B8)
WR (2H1)
EN (1A4)
DDO-DD7 (1G11) (2L4) (2F11)
DD0-DD7
AO-A2 (2E6) (2E7) (3D11)
IDKA (2F2)
IN1 (2B5)
IN0 (2B4)
RESET (2E4)
LOAD (1E1) (2B4) (3A7)
WANEC (1C1)
IBM (1B1)
WANG (1B4)
SLT3E (3B3)
WANEO (1E1)
DRIVE1 (1D10)
RECAG (1E7)
RDS (2F9)
STEPCT (2D5)
WANEC (1B2)
EN (1A4)
RECDS (1F1)
WE (1A1)
DRIVE SELO (2K5)
SELECT 1 (1C10)
SELECT0 (1D10)
WR2 (2B5)
WR3 (2A4)
WANEO (1E1)
WANG (1B4)
SLT3E (3B3)
DRIVE1 (1D10)
RECAG (1E7)
RDS (2F9)
STEPCT (2D5)
WANEC (1B2)
EN (1A4)
RECDS (1F1)
WE (1A1)
DRIVE SELO (2K5)
SELECT 1 (1C10)
SELECT0 (1D10)
WR2 (2B5)
WR3 (2A4)
R1 2.2K
R2 1K
R3 150Ω
R4 150Ω
R5 5K
R6 10K
R7 1K
R8 150Ω
R9 150Ω
R10 10K
R11 10K
R12 10K
R13 10K
R14 10K
R15 2.2K
R16 10K
R17 47Ω
R18 4.7K
R19 4.7K
R20 4.7K
R21 10K
R22 0Ω
R23 10K
R24 10K
R25 10K
RP1 10K
+5VR
DO NOT SCALE
THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON ARE LOANED SUBJECT TO THE AGREEMENT THAT NEITHER IT NOR THE INFORMATION IT DISCLOSES WILL BE MADE AVAILABLE TO ANY PERSON OR ORGANIZATION NOT PERMITTED BY WANG TO HAVE IT AND THAT IT WILL BE RETURNED UPON THE DEMAND OF WANG LABORATORIES, INC.
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MATERIAL -4
MODEL NO VS ARCHIVER
SEE ENGR'G SPECIFICATION No 12-2223
FINISH -4
TOL ON XX AS NOTED .XX ± .FRAC ± .XXX ± .ANGS ± FINISH
SCALE
SHT / OF 3
215-7414
D
7414
3
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
BY
DATE
APPROVED BY
DWN
CHK
E ENGR
M ENGR
MFG ENGR
TITLE
DOUBLE DENSITY DISK CONT
REVISION
NO
SHEET 4

DO NOT SCALE

MR

+5VR

SW1

R26 2.2K
R27 2.2K
R28 2.2K
R29 2.2K
R30 2.2K

±0V

L47 LS244

D0-D7 (1E1)

IWR STEP1 (3A4)

IWR STEP (2C1)

RDST (1C1)

INDEX (1F6)

L12 9602

R31 47K 5%

C2 .0039 µF 35V

CLR1

FINISH (1D1)

DETECT (1C1)

L23 LS74A

+5VR

R42 1K

R40 5.6K

C6 82 PF

BKI (1A5)

R41 1K

L12 9602 CLR 2

REQ (1D2)

L18 74

KDKS (1F11)

CLEAR (1E5)

L36 LS08

SELIBMA (1C8)

R44 10K

L7

NECCS (1C1)

RD (E2)

WR (C1)

RD (2C2)(1E3)(3B0)

WR (3F0) (1B2)

L57 LS244

L25 LS32

L2 LS00

R45 180Ω

C7 390 PF

C8 150 PF

R46 5.6K

R47 1K

I/OW (1C5)

I/OR (1C6)

HRQ (1B5)

L1 9602

CLR2

CLK (1D8)

XTAL1

8MHZ

C1 .01UF

R32 820Ω

R33 820Ω

L42 LS04

L41 LS161

DMA CLK (1B5) (3F9)

FM MODE (1C7)

R34 1K

L51 LS157

C3 560 PF

L53 74

R35 1K

R36 470Ω

WRCLK (1C7)

DACK 2 (1F4)

ECHA (1B2)

KDKS (1F11)

L32

R37 1K

-5VR

BKG (1B5)

AO (1B3)

A1 (1B3)

A2 (1B3)

DMACS (1A4)

L24 LS32

LO DMA1 (1E4)

LO DMA2 (1D4)

MR8 (1B9)(3D11)

L95 LS04

RESET (1B1)

L4 LS08

R38 33K

C4 390 PF

L15 9602

CLEAR (1E5)

R39 1K

MEMR (1A5)

R43 1K

L18 74

KWRA (1F11)

DMAWR (1A5)

L19 125

KWRA (1F4)

SELIBMA (1B8)

R48 4.7K

KWR (1G10)

STEPCT (1E7)

DRIVE SELO (1A7)

DIR (1C7)

L48 LS04

L38 LS32

L49 LS193

L39 LS193

DN UP CAR BOR

D0-D7 (1E1)

LOAD (1B1)

R49 1K

L74

BC2 (1B6)

BC1 (1A6)

BC0 (1B8)

BC5 (1A8)

IN30 (1B2)

L8 LS32

R50 1K

SELIE4A1 (1C8)

L40 LS73

R52 10K

IWR STEP (2E0)

IWRSTEP

DKS (3J3)

KWR (E3)

MR1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY:	DATE
		DWN		ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO V5 ARCHIVER			MFG ENGR	
	SEE ENGR SPECIFICATIONS No 10-223	TITLE DBL DENSITY DISK CONT.			
FINISH	TOL EX AS NOTED .XX ± FRAC ± .XXX ± ANG ±	210-7414	D	7414	8
	SCALE	SHT 2 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER REV

REVISION	DATE	BY
SEE SHEET 1		

DO NOT SCALE

INT M2 (6A) · KP (H4) · P/C WAIT · RD DATA (S1) · BST (12)

PDN (3C5)

L63 LS32 · L55 LS08 · L21 · S11 · L54 LS32 · L63 LS32 · L54 LS32 · L63 LS32 · L63 LS32 · L55 LS08 · L54 LS32 · SEL BMA (1B8) · DMA (2F5) CLK

D0-D7 (1E1) · DIR · L69 LS245 · A0 (1B3) · MRB (CE5) · L55 LS08

L62 Z80A-PIO: D0-D7, CE, C/D SEL, B/A SEL, ASTB, BSTB, IEI, RD, IORQ, MI, IEO, INT, ARDY, BRDY, A0-A7, B0-B7 · INT (1B4)

R67 2.2K · R68 2.2K · +5VR · +5V · GND · VCC

BA (16) · PIO CE (1A3) · IORQ (2) · IORQ (1B11) · RD (2B10) · MI (Z) · ØB (B)

L55B LS04 · L22 LS08 · L64 LS74 · R69 2.2K · R72 10K · L33 3B · L4 LS08 · L42B LS32

SELIBMAI (1C8) · LOAD (1B1)

R53 1K · L69A · R70 · TP1 · L63A LS74 · L55A LS74 · L70 LS00 · L55A LS74

R71 · C30 · TP3 · RD DATA (1D1) · VCO SYNC (1E6)

R55 1.21K ⅛W 1% · R57 100Ω · R58 2.2K · R59 2K · R56 1K · R62 3.9K · R63 4.02K ⅛W · R64 1K ⅛W 1% · C16 27pf · Q1 2N3904 · Q2 2N3906

VR1 7905 · -12V · C12 1uF (HF) · C13 .33uF (T) · C14 1uF (T) · C15 .1uF (HF) · ±0V · R82 470Ω · D1 GER · C20 5.6uF 35V (T) · R65 470Ω

C26 .1uF (HF) · C28 .05uF · C29 .05uF · C27 .1uF (HF) · +5V

C24 470 PF (M) · C21 .1uF · C22 BF · VCK L62B · IF · VCC1 VCC2 VEE · C22 .1uF (HF) · C23 1uF (T) · C25 .05uF · R60 1K · R81 1K · L63C MC10125

R61 1K · L55A LS74 · C31 1uF (T) · C32 .1uF (HF) · R83 470Ω · VR2 7805 · C33 1uF (T) · C34 .33uF (T) · R84 4.02K ⅛W 1% · C86 18pf · Q3 2N3905 · R85 1K · PDN (3B6)

L70 LS00 · -70 · L69A

DRIVE SEL1 (1A7) · DIR (1C7) · STEPCT (1E7) · L20 · L52B LS32 · L52A LS193 BCD · DD0-DD7 (1E1) · R73 1K SIP · L52 LS74 · L4 LS08 · R79 10K · IWR STEP1 (2F10) · F3 IWR STEP1 · 18 INT

L52C LS157 · STB · SEL · FM MODE (1C7) · JUMPER · R66 1K · L42C LS74 · DATA (1C7) · TP2

L32A LM723 · R86 1K · R88 2.2K · C87 .0047uF · R87 680Ω · R89 470Ω · R90 470Ω · +12V

C35 390 PF · C36 390 PF · R75 2.2K · L10 9602 · C37 390 PF · R76 47K 5% · C38 15 UF (T) · R74 2.2K · R77 22K · C-R1 · C-R2

L9 3B · 9 AUTO RESET · 10 P-RCMSW · OUT 30 (1B1) · CLEAR (1E5) · L8 LS32 · R78 10K

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN Chritley	5-13-8	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS ARCHIVER			MFG ENGR	
	SEE ENGRG SPECIFICATIONS No. 10-203	TITLE DBL DENSITY DISK CONT.			
FINISH	UNLESS OTHERWISE NOTED .XX ± .XXX ± FRAC ± ANG ± FINISH	2IC-7414	D	7414	3
SCALE	SHT 3 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

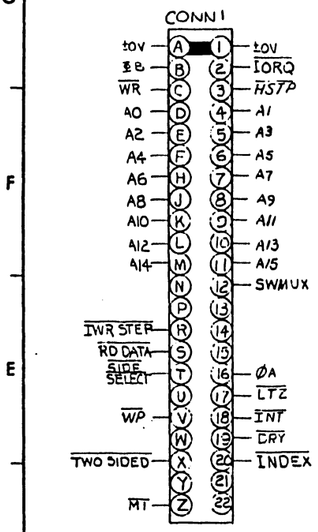
REVISION · NO · SEE SHEET 5

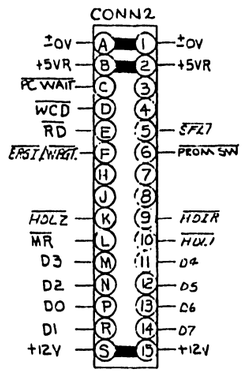
DO NOT SCALE

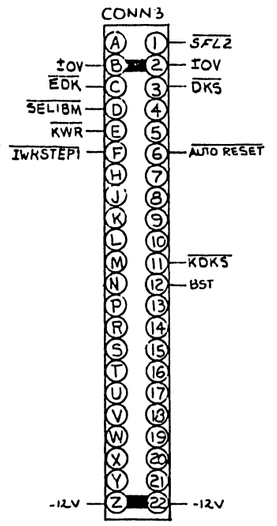
7414 R6

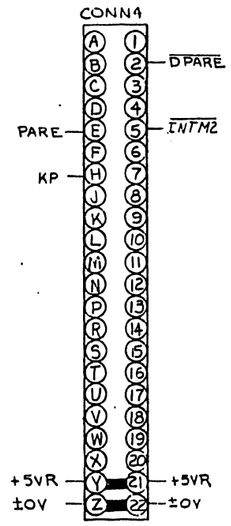
WANG LABORATORIES INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN TK	1-3-85	ENGR	
	CHK		ENGR	
			MFG ENGR	
MATERIAL: N/L	MODEL NO: 5 ARCHIVER; SEE ENGR SPECIFICATION No. 10-203	TITLE: DOUBLE DENSITY DISK CONTROL		
FINISH: N/L	TOL EX AS NOTED: XX = ±, FRAC = ±, XXX = ±, ANG = ±, FINISH	20-7414	D	7414 3
SCALE	SHT 1 OF 1	MFG PART NUMBER	SIZE	DRAWING NUMBER REV

NO	REVISION	DATE	BY









LOCATION	TYPE	SPARE
L1	9602	1
L15	"	1
L70	74LS00	1
L20	7414	2
L5	7474	1
L52		1
L53		1
L8	74LS32	1
L13		3
L42B		3
L54		2
L9	7438	2
L17	7406	4
L19	74125	1
L21	74S11	2
L22	74LS08	2
L35		1
L27	7407	3
L30	74LS02	3
L35	74LS04	3
L40	74LS74	1
L43	74S11	1
L36	74LS244	1
L63C	MC10125	1
L69A	7414	5
L71	74123	1

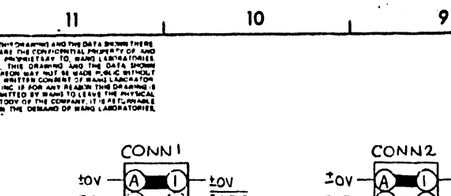
COMPONENT	TYPE	W.L.PART NO.
R58,88	R1,15,26-30,47-69,73,74 2.2K 1/4W 10%	330-3022
	R2,7,34,35,37,39,41-43, 47,49,50,53, 56, 60,61,66,80,85 1K 1/4W 10%	330-3010
	R3-5,8,9,70 150Ω 1/4W 10%	330-2015
	R4,10-14,16,21-25,44, 72,78,79,81 10K 1/4W 10%	330-4010
	R17,36,82,83,87,90,65 470Ω 1/4W 10%	330-2047
	R18-20,48 4.7K 1/4W 10%	330-3047
	R31,76 47K 1/4W 5%	330-1048
	R32,33 820Ω 1/4W 10%	330-2082
	R38 33K 1/4W 10%	330-4033
	R40,46 5.6K 1/4W 10%	330-3056
	R45 180Ω 1/4W 10%	330-2018
	R87 680Ω 1/4W 10%	330-2068
	R55 1.21K 1/8W 1%	333-0106
	R93 2K POT	336-0036
	R51 100Ω 1/4W 10%	330-2010
	R63 4.02K 1/8W 1%	333-0060
	R64, 91 1K 1/8W 1%	333-0089
	R71 6.19K 1/8W 1%	333-0069
	R75,77 22K 1/4W 10%	330-4022
	R84 4.02K 1/8W 1%	333-0060
	R86 1K POT	336-1014
	R62 3.9K 1/4W 10%	330-3039

COMPONENT	TYPE	W.L.PART NO.
C1	.01UF 25V	300-1903
C2	40UF 35V (T)	300-4011
C3	560PF 500V	300-1560
C4,7,35-37	390 PF 500V	300-1390
C6	82PF 500V	300-1082
C8	150PF 500V	300-1150
C10,38,82 84	15UF 20V (T)	300-4022
C12,15, 21-23, 26,27,32 33	.1UF 50V(M.F.)	300-1930
C13,34	.33UF 35V (T)	300-4008
C14,31	1UF 35V	300-4030
C16	27PF	300-1027
C25,28,29	.05UF 12V	300-1900
C39-8,85	.047UF 50V	300-1926
C87	.0056μF 500V	300-1915
C36	8pf	300-1018
C20	5.64μF 35V (T)	300-4017
C30	10pF 500V MICA	300-5033
C24	470pf 500V mica	300-5035
D1	GER	380-0000
Q1	2N3904	375-1080M
Q2,3	2N3705	375-1069M
VR2	7805	374-0001
VR1	7905	374-0002
XTAL	8.0,5% HC-18/U	321-0009
SW1	SW SLIDE 5P05	325-1501

IC LOCATION	TYPE	W/L PART #
L1,10,12	9602	376-0104
L2,79	74LS00	376-0207
L3,8,13,15,24,25, 32,38,42B,52B,54, 65	74LS32	376-0211
L4,22,30,55	74LS08	376-0153
L5,14,52,53	7474	376-0006
L6,23,31,42C,55A, 63A,64	74LS74A	376-0155
L32A	LM723	376-0473
L7,9,26,33	7438	376-0128
L11	SPARE	
L16,35,55B	74LS04	376-0180
L17	7406	376-0055
L19	74125	376-0324
L21,43	74S11	376-0237
L27	7407	376-0076
L28	74LS153	376-0156
L29	74LS175	376-0160
L30	74LS02	376-0208
L34,44,45	74LS158	376-0254
L37	74LS139	376-0226
L39,42A,49,52A	74LS193	376-0220
L41	74LS14	376-0233
L42	7404	376-0010
L46,47	74LS240	376-0297
L50	74LS32C	376-0242
L51	74157	376-0082
L52C	74LS157	376-0214
L55	74161	376-0054
L56,57,65,67	74LS244	376-0228
L58	8257	SEE CHART
L59	UPD765C	SEE CHART
L60,69,7A	74LS245	376-0225
L61,66,68	74LS374	376-0286
L62	Z80 PIO	SEE CHART
L63B	MC1658	376-0483
L63C	MC10125	376-0482
L69A,20	7414	376-0139
L71	74123	376-0080
L58,59,62	40PINSKT	376-5011

MNEMONICS	LOCATION
AUTO RESET	2B1
AC-A7	1A3
A8 A15	1D1
D0-D7	1G3
BST	3C5
DKS	2A5
HDTP	1A8
DPARE	1A9
SFLT	1A7
SFL2	1A7
EDK	1B4
HOLT	1A6
HOL2	1A6
ØA	3D11
EA-M2	3G3
IORQ	1B11
INDEX	1G7
INT	3A4
IWR STEP	2C1
IWR STEP1	3A9
KDKS	2C11
KP	3C4
KWR	2A5
MR	3B11
MR	2G8
ØB	3B11
PARE	1A10
PC WAIT	3C8
PROM SW	3B1
RD	2B11
RD DATA	3G8
RST	1G7
SELIBM	1A9
SIDE SELECT	1G1
SFTP	1A8
SW MUX	1G9
LTZ	1E11
TWO SIDED	1E11
WE	2B11
WCD	1A10
EBSTWRST	1G1
WZ	1E11

210 = 209 + 377 OR 378				
210	209	L58	L59	L62A
7414-A	7414	377-0359	377-0966	377-0342



DIST	REVISION	BY	DATE	APPROVED	DATE
10	ORIGINATED PER DWG# 727 APP'D	MZ	7-30-81		
2/2	REVISED PER ECN# 13957 APP'D	MZ	8-4-81		
2/1	REVISED PER ECO# 14311 APP'D	MZ	8-11-81		
1/1	REVISED PER ECO#18376 APP'D	MZ	9-3-81		
5/2	REVISED PER ECO# 18376 APP'D	MZ	9-3-81		
4/2	REVISED PER ECO# 19246 APP'D	MZ	9-27-81		
3/2	REVISED PER ECO# 19304 APP'D	MZ	10-1-81		
4/1	REVISED PER ECO# 20153 APP'D	MZ	10-14-81		

E-REV 4

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVALS	DATE
DWN			ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL —

FINISH —

MODEL 10 VS ARCHIVER

SEE ENGR SPECIFICATION No. 10-2-23

TOL UNLESS NOTED

TITLE DOUBLE DENSITY BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7414	D	7414	B

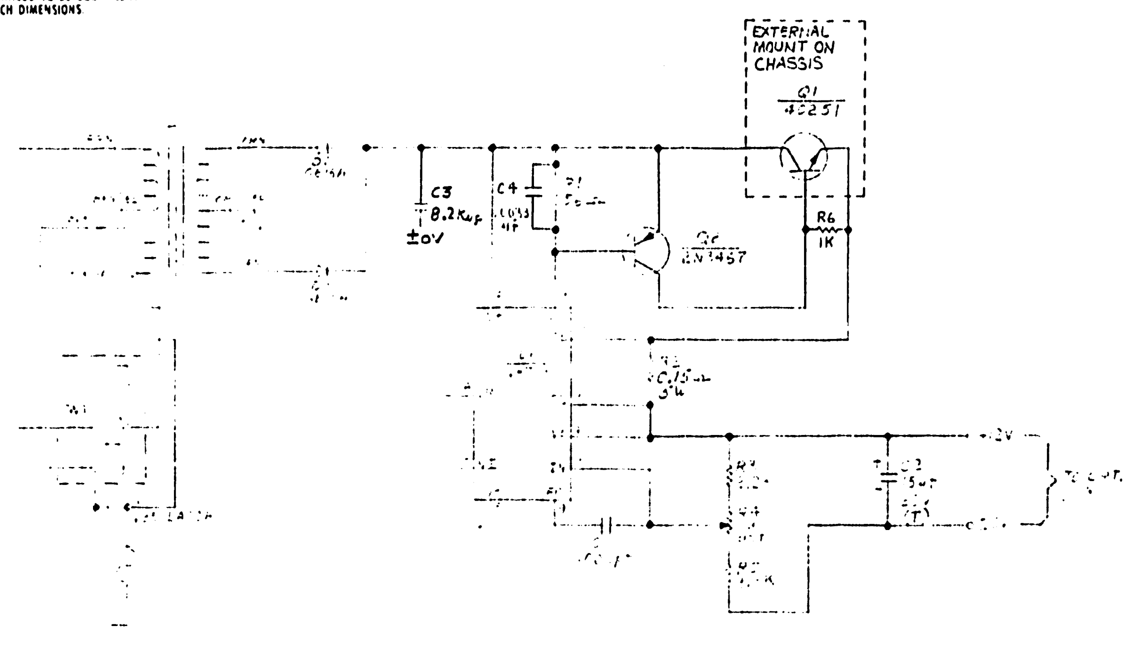
SCALE — SHT 5 OF 5

THE INFORMATION CONTAINED IN THIS DRAWING IS THE PROPERTY OF WANG LABORATORIES, INC., AND IS CONFIDENTIAL AND PROPRIETARY TO WANG LABORATORIES, INC. IT MAY NOT BE COPIED, REPRODUCED OR USED IN WHOLE OR IN PART FOR ANY REASON

MILLIMETERS IN PARENTHESIS
TOLERANCES TO BE EQUIVALENT
TO INCH DIMENSIONS

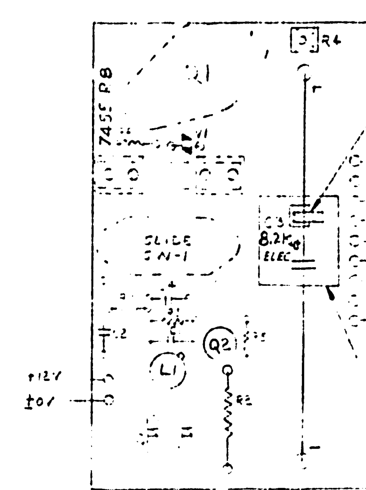
DO NOT SCALE

HOLE LEGEND & TOLERANCES		
SYM	DESCRIPTION	QTY



LOCATION	W...	PIN
L1	376-00..	5

TYPE	COMPONENT	WANG PART NO.
56Ω ¼W 10%	[illegible]	[illegible]
.15Ω 5W 5%	[illegible]	[illegible]0015
2.2K ¼W 10%	[illegible]	[illegible]
1K single Adj Pot	R4	[illegible]
3.3K ¼W 10%	R5	[illegible]
1K ¼W 10%	R6	330-3010
1000pf 100V 5%	[illegible]	[illegible]-5006
15μf 20V 10% (T)	C2	300-4022
GE15A	[illegible]	[illegible]8
		[illegible]-2117
8.2K μf 15V Elect.	C3	300-3078
125 .A 39A		
	Q1	[illegible]
2N3457	Q2	375-1026
[illegible]	C4	300-1900



CABLE TYE 2S (225-1006)

AC
LINE CORD
BLK/YEL
BRN/YEL
BLK
BRN
BRN/YEL 20V
BRN
BRN

BASE CABLE TYE MOUNT (...)

REVISION

QTY.	ITEM	WANG PART NO.	DRAWING NO.	DESCRIPTION
NEXT ASSY.				

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO.

SEE ENGRG. SPECIFICATIONS No.

TITLE

FINISH

TOL. EX. AS NOTED

SCALE | SHT

WANG PART NUMBER | D | DRAWING NUMBER | REV

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MILLIMETERS IN PARENTHESIS.
TOLERANCES TO BE EQUIVALENT TO INCH DIMENSIONS

DO NOT SCALE

EXTERNAL CONTRAST — VIDEO IN — VIDEO ±0V — NOT LOADED FOR 7456-2

VARIATION CHART			
COMP	7456	7456-1	7456-2
R19	330-3069	330-4023	330-3063
C30	300-2412	300-2417	300-2412
C31	300-2413	300-2418	300-2413
Z2	320-0053	320-0056	320-0053
Z3	320-0051	320-0058	320-0051
HOR.YOKE	320-0052	320-0057	320-0052
FLY-BACK	410-1007	410-1006	410-1007
R5	330-2123	330-2069	330-3069
* V YOKE L	YEL	BLU	YEL
* V YOKE K	BLU	RED	BLU
* H YOKE H	RED	YEL	RED

*COMPONENTS NOT LOADED FOR 7456-2	
R9	330-2063
R11	331-2010
R12	330-1023
R44	337-3012
C3	330-1820
C15	300-1622
Q5	375-1014
Q2	375-1056
D4,10	380-1001
C32	300-1047
Q1	375-1012
R10	330-2033
R40	330-2048

7456 R7 — R15 R18 R24 R35 R33 — FOCUS R29 — WIDTH — L3 — L2 — R3 — Q2 — Q1 — R9 — DYNAMIC FOCUS — T1 — CRT — 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

+12V — VIDEO IN — VIDEO ±0V — R1 100Ω ½W 10% — R2 2.2K — R3 6.7K — R9 680Ω — D1 IN752A — L2 NE 592 — R5 SEE VARIATION CHART — R8 150Ω — D4 — C2 35µf 18V — C15 15µf 60V — D10 — C32 47µf — R40 470Ω — MPS-U09 — Q2 — MPS-6512 — Q1 — C3 820 pf — R44 47Ω — R11 22Ω — R10 820Ω — ±0V

L3 TVA 1074 — R13 56Ω 2W 10% — VERT. HOLD — R15 100K CW — C5 0.15µf — R16 10K — C6 1000µf 25V — IN1004 — D2 — D3 3.1V 1W 1N757 — R17 220Ω — C7 100µf 25V — R41 27K — R18 5K VERT. LINEARITY — R19 SEE VARIATION CHART — R42 15K — C8 .02 MYLAR 220Ω — R21 — R20 220K — R22 22K CW — C10 33µf 15V — R24 20Ω — R25 2.2Ω ½W 10% — C11 1000µf 25V — C9 .02µf — TP6 — R23 15K — V YOKE L — V YOKE K — VERT. YOKE — EXTERNAL — VERT. SIZE — +12V — ±0V

L1 TBA 750 — R30 6.8K — C21 .1µf 20V — R31 470K — C22 .1µf 20V — C23 .1µf 20V — R32 180Ω — C26 .47µf MYLAR 100V — C28 10µf 15V — C24 50µf 50V — C25 .1µf 50V — R33 5K NON-HOLD — R34 5.6K — C27 .22µf 100V — R35 10K PHASE — C29 35µf 16V — R36 68Ω — R37 5.1K — R38 2.2K — Q3 — R39 100K — C30 SEE VARIATION CHART — R46 47Ω — Q4 — D11 — R7 33Ω 1W 10% — C31 SEE VARIATION CHART — Z2 WIDTH — Z3 HOR. LINEARITY — T1 — SEE CHART — HOR. YOKE SEE VARIATION CHART — H YOKE BLK — TP1 — D — E — F — ±0V

NOTES:
1. CONNECT S2 LEAD TO PIN B UNLESS OTHERWISE TO ACHIEVE RASTER CUT OFF.

EXTERNAL — # IN CRT SOCKET LEAD — 390-0101 — VIDEO OUT — +12V — ±0V — YEL 270Ω BRN — BLK — GRN — RED — ORN — 1K — SEE NOTE 1 — SEE CHART — HG17 — G1 — FOCUS — G2 — VG1 K — DYNAMIC FOCUS — R26 1.2 MEG — C12 .02 MF 1400V — C13 .02 MF 1400V — C14 .1µf 400V — C16 .22-.22PF — R22 100K — R23 100K — C17 .02µf 6KV — C18 .22 MF MYLAR — BRIGHT BOTTOM — BRIGHT CENTER — BRIGHTNESS — R29 270K — R43 150K — BRIGHT TOP — D7 — D5 — D6 — D8 — C19 .1000µf 25V — C20 .1000µf 25V — C17 .50µf 50V — FB-1 — FB-2 — FB-3 — FB-5 — FB-6 — FB-8 — H YOKE — HOR. YOKE SEE VARIATION CHART

FB LOCATION	W.L. PART NO	QTY
L1	376-0260	1
L2	376-0239	5
L3	376-0261	13

EXTERNAL — SIGNAL DESIGNATIONS VIEW FROM BOTTOM (WIRING) SIDE OF CONNECTOR

	FB-5	
G2	FB-6	
±0V	FB-8	
±0V	FB-3	
±0V	FB-1	
H-YOKE - G	FB-2	
H-YOKE - BLK	+12VD	
V-YOKE K	+12VR	
V-YOKE G	G2	
FOCUS	TP2	
G1	TP1	
VIDEO OUT	BRIGHT BOTTOM	
VIDEO ±0V	BRIGHT CENTER	
VIDEO IN	BRIGHT TOP	

COMP SIDE — WIRING SIDE

COMP.	W.L. PART NO.
C1, 24	300-3006
C4, 10, 27	300-3009
C3	300-1820
C9	300-1470
C12	300-2415
C26, 29	300-2247
C14	300-2316
C16, 18	300-1915
C19	300-3010
C21, 23	300-1978
C22	300-4000
C25	300-2416
C28	300-2618
C4, 5, 17	300-1912
C5	300-2215
C6, 20	300-2662
C7	330-1033
C13	300-1776
C32	300-1247
C1	375-1111
C2	375-1057
C3	375-1057
C4	375-1014
C5	375-1019
C15	300-4022
T1	410-1006
R1, 10	SEE CHART
C30, 31	SEE CHART
Z2, 3	SEE CHART
HOR. YOKE	SEE CHART
FLY-BACK	SEE CHART
V YOKE	SEE CHART
H YOKE	SEE CHART
H YOKE	SEE CHART
R2, 3	336-1021
R24	336-1021
R25	331-0022
R29	336-0031
R18, 33	336-1020
R33	333-3067
R35	336-1015
Q7	372-1033
R41	330-1039
D1	380-2050
D2	380-4000
D3	380-3021
D5, 7	380-3009
D6, 9	380-3310
D8	380-1312
D4, 10	380-1001
Z1	320-0054

E-REV 7456 [6] — E-REV 7456-1 [5] — E-REV 7456-2 [1]

REVISION	BY	DATE	APPROVED BY	DATE
CHK = K			ENGR R.S.	
ENG G.D.		10-21-77	M. NOR	
			MFG ENGR	

QTY	ITEM	WANG PART NO	DRAWING NO	DESCRIPTION
NEXT ASSY				

WANG LABORATORIES, INC. — MATERIAL — FINISH — MODEL NO 7" → 12 WANG MONITOR — SEE ENGR SPECIFICATIONS — TOL FOR AS NOTED .X = ±.1 .XX = ±.02 ANG = ±1° — SCALE — SHT — OF

TITLE ELECTRONICS FOR 9" MOVIE MONITOR

SEE CHART | D | 7456 | 14

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

DO NOT SCALE

INT (2F1)

+5V +5VR GND VCC INT

R9 10K +5VR

74LS244 L90 L74 L41 7404

HALT

WAIT (1B2) 7411 L94 WAIT

P/C WAIT C2 R1 2.2K +5VR

TESTER BUS RQ 3S R93 2.2K +5VR

MPE (JB8) HOLD (1B11) 7432 L42 7411 L94 BUSRQ

R3 2.2K +5VR R2 4.7K

D BUS RQ W1

RESTART A6 R4 4.7K +5VR NMI

DL RESTART (3A9) BPF (3B6)

RESTART T4 R5 4.7K +5VR 7400 L68 L93 7404 RESET

TMR 1S R6 2.2K +5VR 7408 L69 MRB (3B8)

MRA (2E8) (3B3)

WTR D4 7402 L53 PWRST (1A7)

AUTO RESET 15 R97 2.2K +5VR L93 7404

7474 L95 2CLR 2D 2PR 2CK 2Q

CRTP (3B4) 74C8 L65

MPE6 (1E2) 7432 L42

RD (1D1)

74LS280 L92 PARE (3C7)

WRE (1C1) 74125 L63

L44 7404 L66 7404

HCLR (1F10)

OUTOE (1F1) 7408 L67

PRPWRS 14 7408 L67

+5VR R3 4.7K

BUS C2

SEE SH 5

E4 PART

20 BPF L2 MR

MPE (3D7) K2 MPE

4 BUSAK

A4 PWRST

P1 DBA

BUSAK (1E4)(3C5) 7404 L93

R7 2.2K +5VR

D8-D7 (2C9)(3B1)

7410 L61

BUSAK (1B8)

MREQ IORQ WR RD M1 RFSH

R11 10K R12 10K R13 10K R14 10K +5VR

74LS245 L91 DIR

D8 D1 D2 D3 D4 D5 D6 D7

INTACK (2G5) 7408 L71

R16 +5VR 7408 L79 7474 1PR 1CK 1D 1CLR

CCMM (2F5) (4A6) (3B2)

MCK (1F5) 7408 L81 7474 2CLR 2D 2PR 2CK 2Q L96

L108 74LS138 L109 74LS138 L110 74LS138

A8 A1 A2 A3 A4 A5 (1C4)(3G9)(4C2)

OUT00 (2E6) OUT08 (2C1)

IN00 (2E6)(2B2) IN07 (2B4)

Y1 15.9744 MHZ R15 470Ω R16 330Ω C1 68PF L106 74H04 MCK (1C4)

L44 7404 L66 7404 L106 74H04

L46 7400 L69 7404 L62 7402

R21 1K R19 2.2K +5VR

7474 L74 1PR 1CK 1D 1CLR 2CLR 2D 2PR 2CK 2Q

L107 S74 L107 S74

R25 10Ω R26 330Ω +5VR SPS6551 R99 33Ω

IORQ (2G6) MREQ (1C11,1B4)

R22 4.7K R23 +5VR

WREN (4E6) 7408 L81

M1 (2G6)

RR (1C11,3A7)

7474 L86 L87 L96 L101

A13 (1G2) 7410 L64 WCMAR (3D7) WCNT (3D7)

7404 L66 BL (3D4) A13 (3A7)

R24 +5VR R99 2.2K

IA (4C8)

CWAIT (1F1C)

MREQ (1E2) 7432 L83

BLA (3B7) U4 BLA

P2 R2 N2 M2 L2 K2 H2 8S 11S 12S 13S 14S 10S 12S 9S

D0 D1 D2 D3 D4 D5 D6 D7 MCK 3Z

13 INT 12 OUTOA 8 OUTOB 7 OUTOC 6 OUTOD (2C1) INT06 (3C1) INT05 (3C1) INT04 (3C1) OUT03 (2C1) INT02 (3C1) INT01 (3C1)

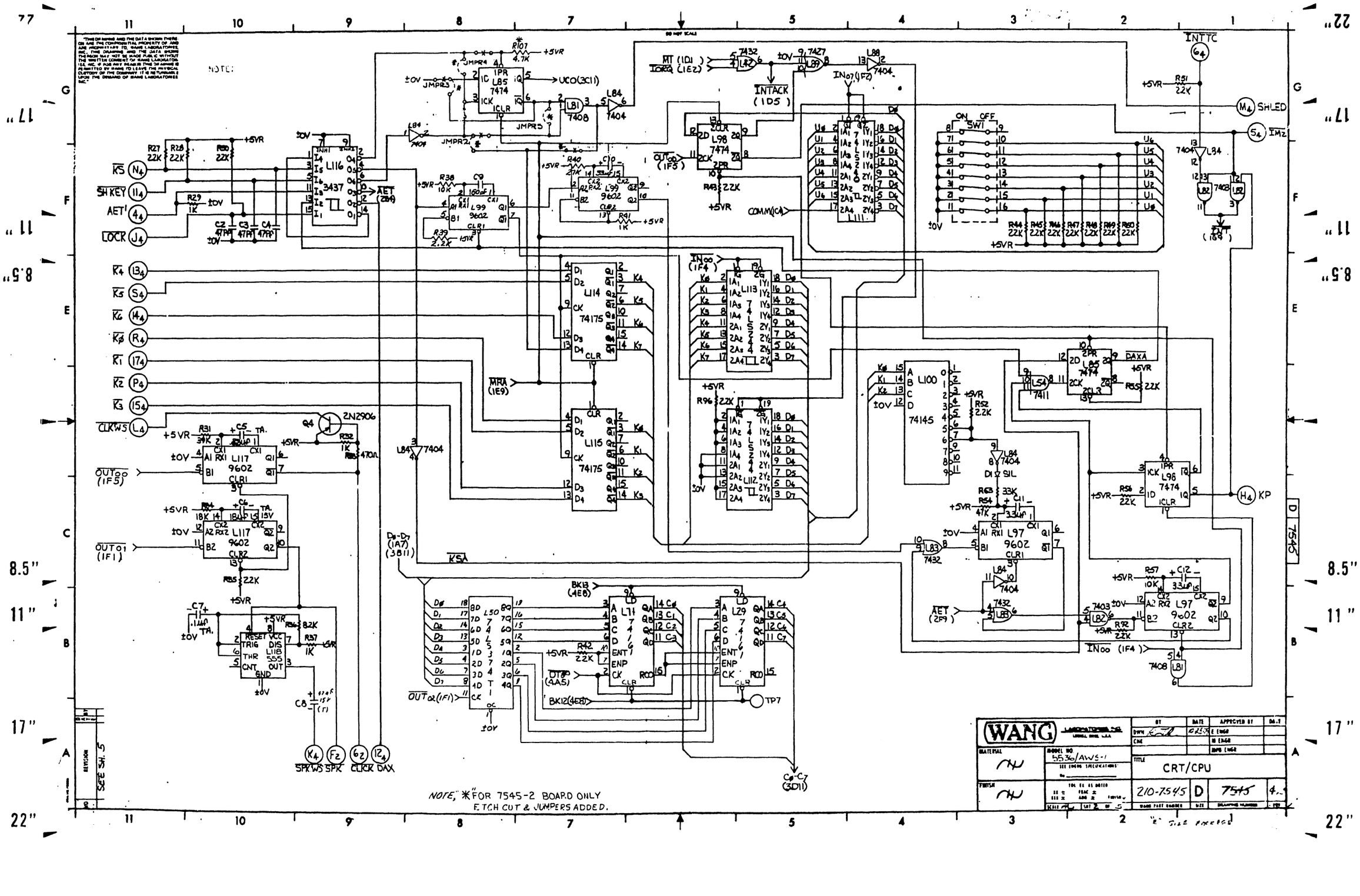
R1 IN06 N1 IN05 T1 ΦA 5S B ΦB

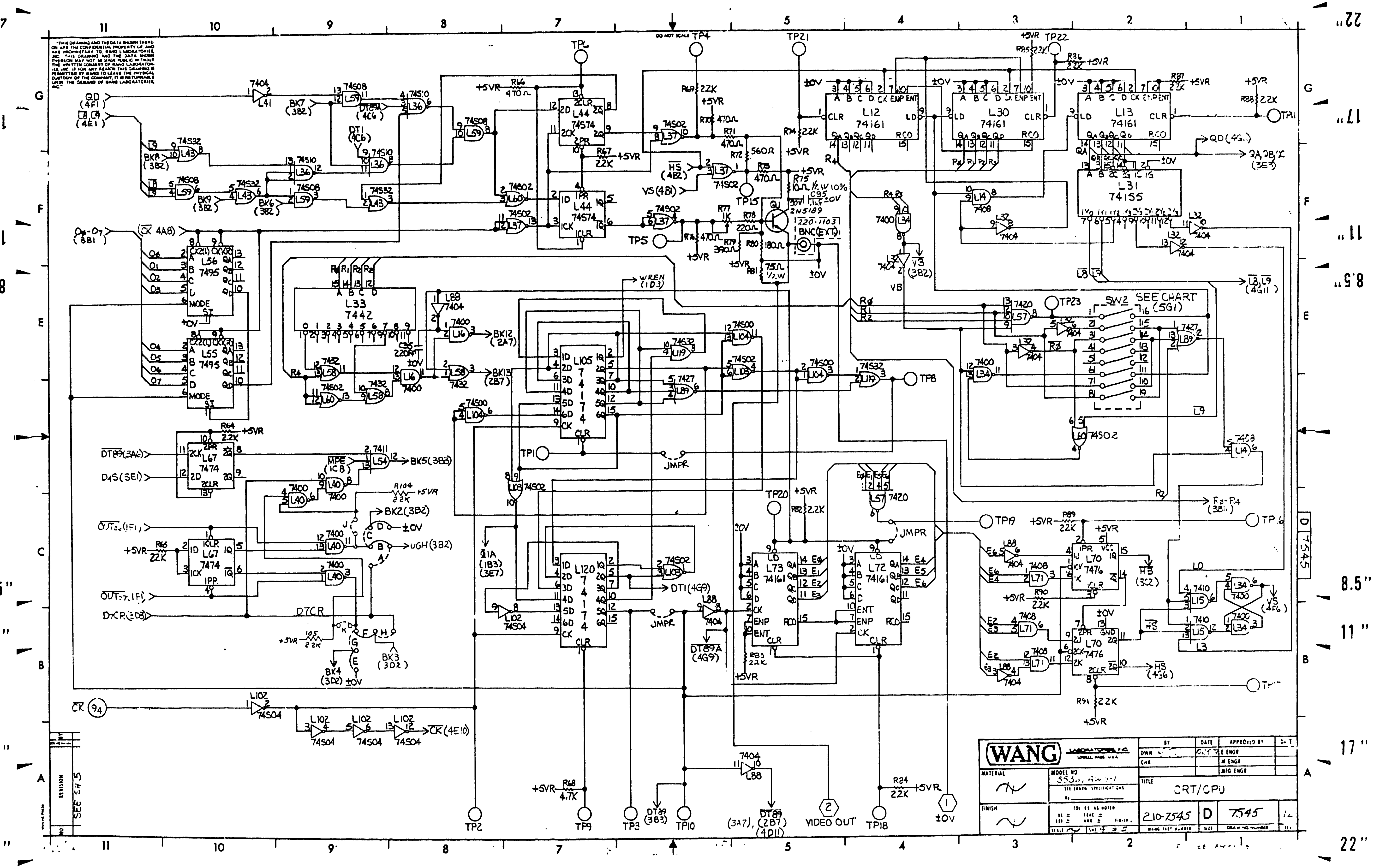
11S 4Z MREQ N5 2I IORQ L3 1I WR E5 E2 RD 7S 3I MI 2S Y1 RFSH 3Y WRE WRE (1C9)

L83 7432

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY
	DWN		E ENGR
	CHK		M ENGR
			WHG ENGR
MATERIAL	MODEL NO 370 20/AWS-1	TITLE CRT/CPU	
FINISH	TOL EX AS NOTED .XX ± .XXX ± ANG ±	210-7545	D 7545
	SCALE	WANG PART NUMBER	SIZE DRAWING NUMBER

D 7545

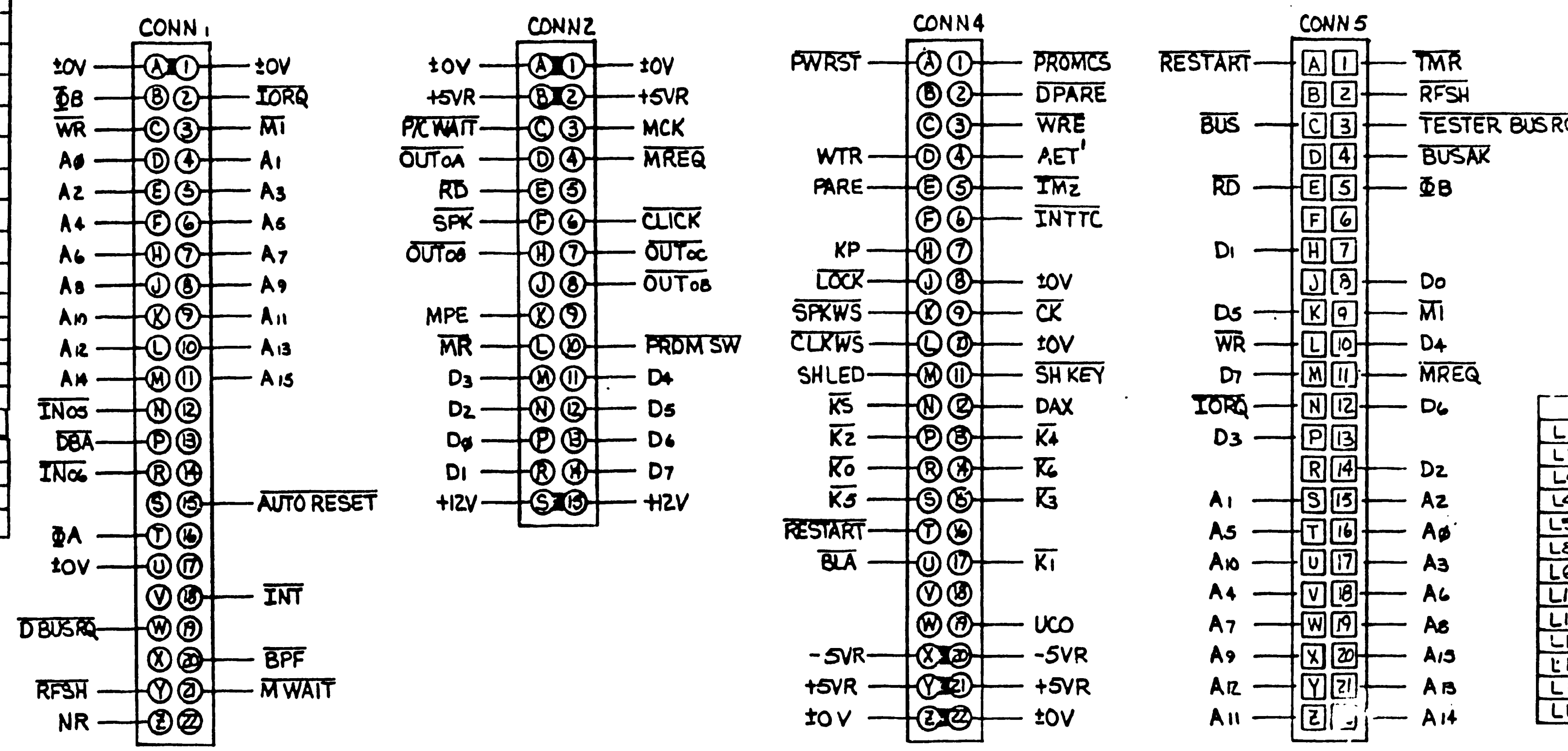

NOTE:
DO NOT SCALE
INTTC
SHLED
IMZ
KP
INTACK (1D5)
IN07 (1F2)
IN00 (1F4)
OUT00 (1F5)
OUT01 (1F1)
OUT02 (1F1)
MRA (1E9)
DA-D7 (1A7) (3B11)
KSA
BK13 (4E8)
BK12 (4E8)
DTP (4A5)
AET (2B4)
AET (2B9)
SPKWS
SPK
CLICK
DAX
CLKWS
KS
SHKEY
AET'
LOCK
SEE SH. 5
NOTE, "*" FOR 7545-2 BOARD ONLY
ETCH CUT & JUMPERS ADDED.
WANG
CRT/CPU
210-7545
D
7545

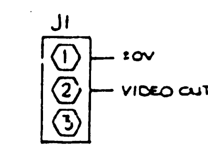

WANG
LABORATORIES, INC.
LOWELL, MASS. U.S.A.
CRT/CPU
210-7545
D
7545
SEE ENGRG SPECIFICATIONS
DO NOT SCALE

DO NOT SCALE

MNEMONICS	COORDINATES
AET'	2F11
AUTO RESET	1D11
Aø-A15	3A8
BLA	1A4
BPF	1A9
BUS	1A11
BUSAK	1A8
CK	4B11
CLKWS	2D11
CLICK	2A9
DAX	2A9
DBA	1A6
DBUS RQ	1F11
DPARE	3G1
Dø-D7	1A5
IM2	2G1
INT	1G1
INTTC	2G1
IORQ	1E1
INO5	1F1
INO6	1F1
KP	2C1
KS	2F11
Kø-K6	2E11
LOCK	2F11
MCK	1A4
MI	1D1
MPE	1A8
MR	1A9
MREQ	1E1
MWAIT	1F11
NR	3A8
ΦA	1E1
ΦB	1E1

MNEMONICS	COORDINATES
OUToA-OUToc	1G1
OUToB	1G1
PARE	1A10
P/C WAIT	1F11
PROMCS	1B11
PROM SW	3A11
PWRST	1A7
RD	1D1
RESTART	1E11
RFSH	1D1
SH KEY	2F11
SHLED	2G1
SPK	2A9
SPKWS	2A9
TESTER BUS RQ	1F11
TMR	1E11
UCO	3C11
VIDEO OUT	4A5
WR	1D1
WRE	1D1
WTR	1D11

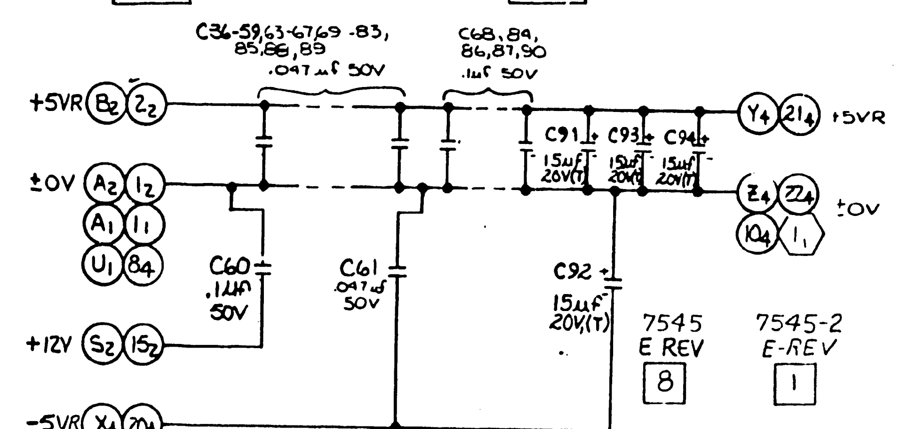




SPARES		
L15	7410	1
L16	7400	2
L41	7404	4
L45	7474	1
L53	7402	3
L80		2
L66	7404	2
L101	7474	1
L102	74S04	1
L103	74S02	1
L104	74S00	1
L119	74S32	2
L121	74367	1

JUMPER CHART		
L51	L52	ADD JUMPERS
377-0317	377-0317	B,D,E,F
377-0317	377-0348	A,C,E,F
377-0348	377-0317	B,D,G,H
377-0348	377-0348	A,C,G,H

SWITCH CHART	
SW2	
50 HZ	60HZ
TOP 3 SWITCHES ON, ALL OTHERS OFF.	BOTTOM 3 SWITCHES ON ALL OTHERS OFF.



7545 E REV	7545-2 E-REV	7545-3 E-REV
8	1	1

D 7545

REVISION		
ORIGINAL ISSUE DWN: [illegible] APP'D: F.S.S.	0	[illegible]
REVISED PER ECN #1065 APP'D: F.S.S.	1/0	11-12
REV PER ECN 11513 APP'D F.S.S.	2/6	[illegible]
REV PER ECN 11665 APP'D F.S.S.	3/1	[illegible]
REV PER ECN 11697 APP'D F.S.S.	4/2	[illegible]
REV PER ECN 12000 APP'D F.S.S.	5/2	[illegible]
REV PER ECN 12523 APP'D F.S.S.	6/3	[illegible]
REV PER ECN 12667 APP'D F.S.S.	7/4	[illegible]
REV PER ECN 12875 APP'D [illegible]	8/4	[illegible]
REV PER ECN 13052 APP'D [illegible]	9/5	[illegible]
REV PER ECN 13266 APP'D [illegible]	10/6	[illegible]
REV PER ECN 13274 APP'D [illegible]	11/6	[illegible]
REV PER ECN 13713 APP'D [illegible]	12/6	[illegible]
REV PER ECN 13865 APP'D [illegible]	13/6	[illegible]
REV PER ECN 13871 APP'D [illegible]	14/7	[illegible]
REVISED PER ECN # 14776 APP'D [illegible]	15/7	[illegible]
REV PER ECN # 14635, 14791 APP'D [illegible]	16/7	[illegible]
REVISED PER ECN # 14687, 14812 APP'D [illegible]	17/7	10-20-80
REVISED PER ECN # 15825, 16035 APP'D [illegible]	18/7	[illegible]
REVISED PER ECN # 16237 APP'D [illegible]	19/7	10-3-80
REVISED PER ECN # 16891 APP'D [illegible]	20/7	11-13-80
REVISED PER ECOS 17715 & 17721 APP'D [illegible]	21/7	2-4-81
REVISED PER ECO# 17711 APP'D [illegible]	22/7	2-13-81
REVISED PER ECO # 18057 APP'D [illegible]	23/7	2-17-81
REVISED PER ECO # 17499 APP'D [illegible]	24/7	3-5-81
REVISED PER ECO # 18212, 18345, 18363, 10909 APP'D [illegible]	25/7	3-23-81
REVISED PER ECO # 18913 APP'D [illegible]	26/7	4-21-81
REVISED PER ECO # 18933 APP'D [illegible]	27/7	5-1-81
REVISED PER ECO # 19689 APP'D [illegible]	28/7	7-9-81
REVISED PER ECO # 21635, 21807 APP'D [illegible]	29/7	2-4-82
REVISED PER ECO# 22932 APP'D [illegible]	30/7	5-10-82
REVISED PER ECO # 22933 APP'D [illegible]	31/7	5-12-82
REVISED PER ECO # 23157 APP'D [illegible]	32/7	5-28-82
REVISED PER ECO # 23113, 23310 APP'D [illegible]	33/7	6-8-82
REVISED PER ECO # 23510 APP'D [illegible]	34/7	7-8-82
REVISED PER ECO # 23949 APP'D [illegible]	35/7	7-30-82
REVISED PER ECO # 13278 & 24900, APP'D [illegible]	36/7	10-20-82
REVISED PER ECO'S 21586, 21587, 21623, 21714, 21874 APP'D: DJ CORBIN	[illegible]	5-4-83
REVISED PER ECO'S 25575 & 25633 APP'D: DJ CORBIN	38/8	5-4-83
REVISED PER ECO 26976 APP'D: DJ CORBIN	39/8	5-4-83
REVISED PER ECO 28038, 28048 APP'D [illegible]	40/8	7-1-83
REVISED PER ECO 29560 APP'D [illegible]	41/8	[illegible]
REVISED PER ECO 32435 APP'D [illegible]	42/8	[illegible]

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	10-25-79	E ENGR [illegible]	[illegible]
CHK	[illegible]	[illegible]	M ENGR	
			MFG ENGR	

MATERIAL: ~

FINISH: ~

MODEL NO. 5536/ANS-1

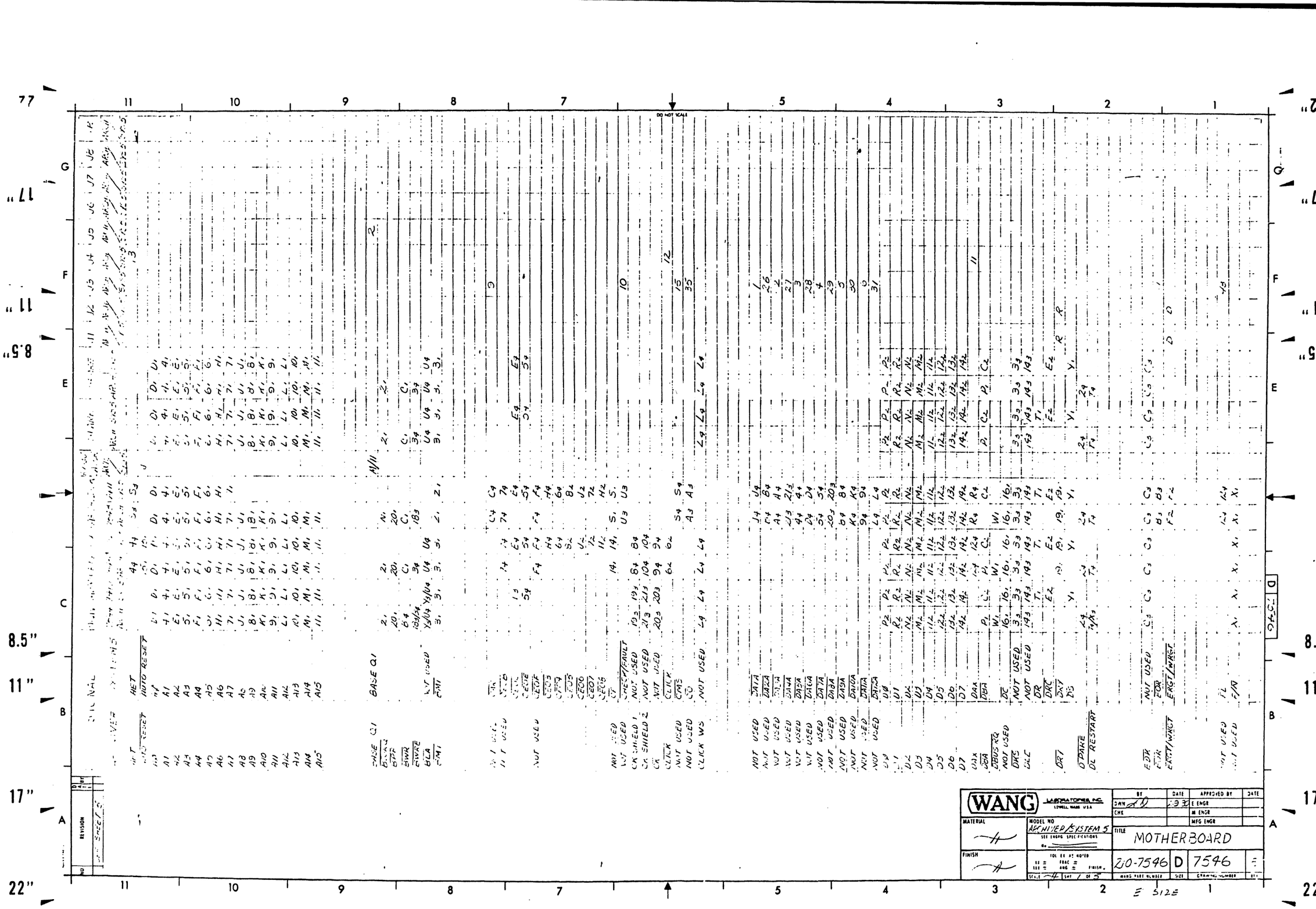
SEE ENGRG SPECIFICATIONS No.

TOL EX AS NOTED

SCALE ~ SHT 5 OF 5

TITLE: CRT/CPU

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7545	D	7545	42


WANG LABORATORIES, INC.
LOWELL, MASS. U.S.A.
MATERIAL
MODEL NO
ARCHIVER/SYSTEM 5
SEE ENGRG SPECIFICATIONS
TITLE
MOTHERBOARD
FINISH
TOL ON AS NOTED
FRAC =
ANG =
FINISH
SCALE 1/4
SHT 1 OF 5
20-7546
D
7546
SIZE
DRAWING NUMBER
REV
DRN
CHK
E ENGR
M ENGR
MFG ENGR
DATE
APPROVED BY
DATE
REVISION
NO
BY
SHEET
8.5"
11"
17"
22"
E SIZE

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN RD.	2-3-77	E ENGR	
	CHK		SW ENGR	
			MFG ENGR	
MATERIAL H	MODEL NO ARCHIVER SYSTEMS (SEE ENGRG SPECIFICATIONS)	TITLE MOTHERBOARD		
FINISH H	TOL ±± AS NOTED .XX = ±.010 .XXX = ±.005 ANG = ±1 DEG.	210-7546	D	7546
	SCALE 1/2 SHT 2 OF 3	WANG PART NUMBER	SIZE	DRAWING NUMBER

E SIZE

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN		E ENGR	
	CHK		M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. ARCHIVED/SYSTEM 5 (SEE ENGRG SPECIFICATIONS)		TITLE MOTHER BOARD	
FINISH	TOL EE AS NOTED XX = ±.010 XXX = ±.005 ANG = ±1°		210-7546 (WANG PART NUMBER)	D (SIZE) 7546 (DRAWING NUMBER)
	SCALE 1/2	SHT 3 OF 3	E SIZE	

7546

SIGNAL

ARCHIVER SYSTEMS

SPARE

SPARE

SPARE

SPARE

DO NOT SCALE

NO	REVISION	DATE	APPROVED
	SEE SHEET 5		

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	L.R.	2/1/82	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL —

MODEL NO ARCHIVER SYSTEMS
SEE ENGRG SPECIFICATIONS
No.

TITLE MOTHERBOARD

FINISH —

TOL EX AS NOTED
XX ± FRAC ±
XXX ± ANG ±
FINISH √

SCALE — UNIT 2 OF 2

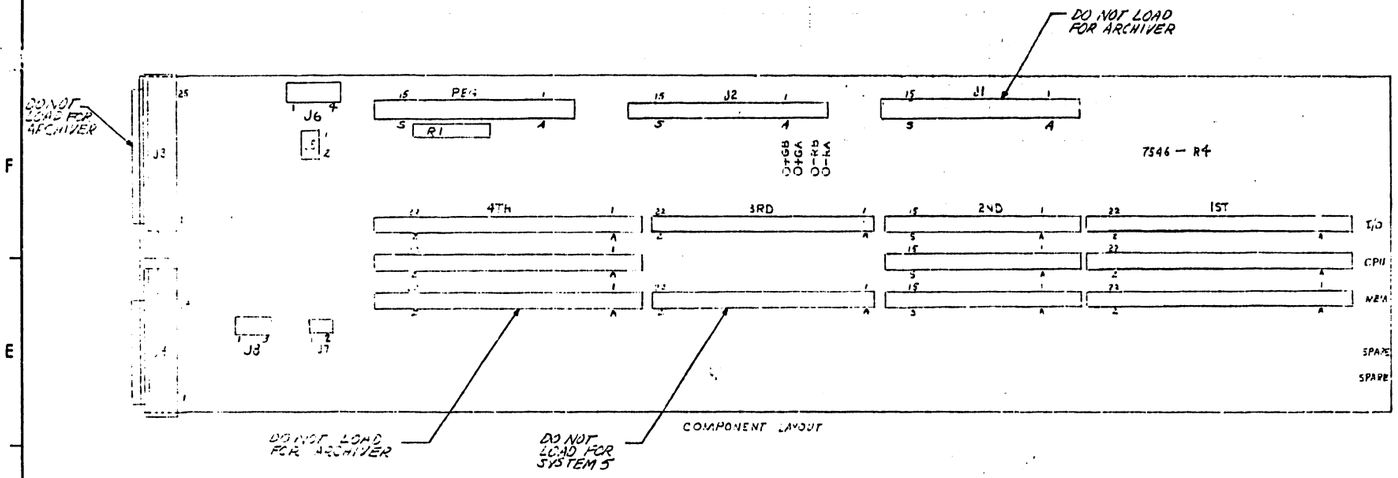
210-7546 | D | 7546

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

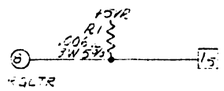
D 7546

SIZE

DO NOT SCALE



COMPONENT	WANG PART NO.	TYPE
	334-0021	
	350-1362	50 PIN
	654-1195	CONN 4 POS
	654-1195	CONN 3 POS
	350-6121	



NOTES: 1) DO NOT LOAD J1, CPU, 3RD, CONN. MEM. 4TH CONN. ON ALL -1 BOARDS.

REVISION	BY	DATE
REVISED PER ECO# 19850		

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. 7546 MEM SYSTEM 5

SEE ENGR'G SPECIFICATIONS

No. —

FINISH

TOLERANCES AS NOTED

XX ± FRAC ± XXX ± ANG ± FINISH

SCALE SHT 5 OF 5

TITLE MOTHER BOARD

WANG PART NUMBER

SIZE D

DRAWING NUMBER

REV

DO NOT SCALE

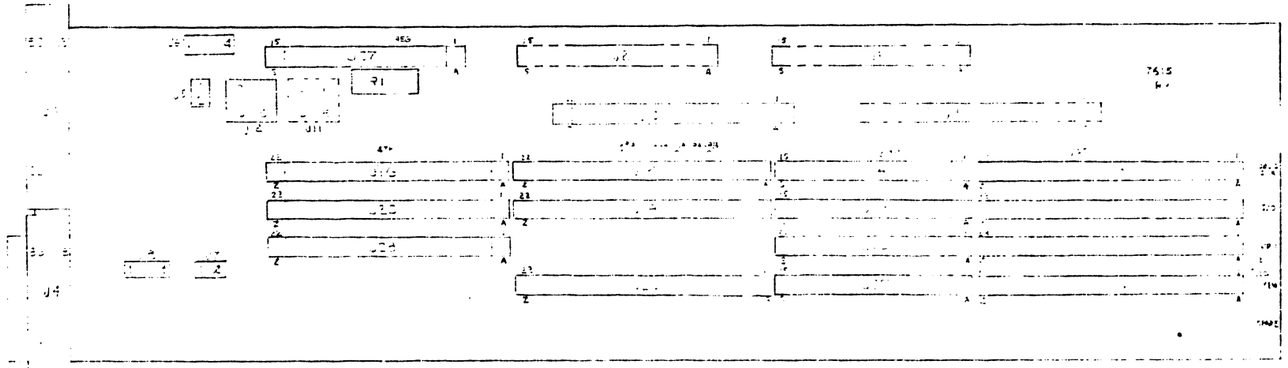
	BY	DATE	APPROVED BY	DATE
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	DWN		E ENGR	
	CHK		M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO		TITLE	
	SEE ENGRG SPECIFICATIONS No.			
FINISH	TOL EX AS NOTED .XX = FRAC = .XXX = ANG = FINISH		D	
	SCALE - SHT OF	WANG PART NUMBER	SIZE	DRAWING NUMBER REV

NO	REVISION	BY	DATE

DO NOT SCALE

COMPONENT	W.L PART NO	TYPE
J14, 18, 22, 25, 27	350-0011	30 PIN CONN.
J19, 26	350-0039	44 PIN CONN.
J4	350-1005	36 PIN CONN.
J5, 7	654-1198	2 PIN CONN.
J13, 15, 20, 23, 24	350-0021	44 PIN CONN.
J12	654-2186	6 PIN CONN.
J6	654-1194	4 PIN CONN.
J8	654-1133	3 PIN CONN.
R1	334-0031	220Ω 1W, 5%

+5V S — R1 — +5V R



REVISION	BY	DATE	APPROVED BY	DATE
REVISED PER ECO [illegible]			E ENGR	
			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL MASS. U.S.A.

MATERIAL — MODEL NO — SEE ENGRG SPECIFICATIONS No.

FINISH — TOL UNLESS NOTED .XX ± .010 .XXX ± .005 FINISH

SCALE — SHT — OF

TITLE

WANG PART NUMBER — SIZE D — DRAWING NUMBER

DO NOT SCALE

REVISION	BY	DATE	APPROVED	DATE
SEE SHEET 1				

	BY	DATE	APPROVED BY	DATE
DRAWN	RD	5/15/80	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

FINISH

MODEL NO APCHIVER
SEE ENGRG SPECIFICATIONS
No.

TOL EX AS NOTED
XX ± FRAC ±
XXX ± ANG ± FINISH

SCALE SHT OF

TITLE DATA LINK MEMORY

SEE CHART | D | 7744 | 14

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

DO NOT SCALE

RAS0-RAS3 (1B3)

A11-A15 (3B1)

RD (1E6)

MRDD (1B4)

PROMSEL (2B11)

R20 33Ω R21 33Ω R22 33Ω R23 33Ω R24 22Ω

CAS (1C1)

DO-D7 (3A5)

A0-A13 (3B5)

PARE (2A9)

MWR1 (1G1)

SWMUX (2E1)

BLA (1G3)

MRD (1G1)

PARE (2F11) (2C7)

SWMUX (3E11)

PARE (2A5)

PROMSEL

MWAIT

DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
MATERIAL	MODEL NO ARCHIVER	DWN A.B.	5/15/81	E. ENGR	
	SEE ENGG SPECIFICATION No.	CHK		M. MGR	
FINISH	TOL EX AS NOTED .XX ± FRAC ± .XXX ± FINISH			MFG ENGR	
	SCALE — SHT 2 OF 7	TITLE DATA LINK MEMORY			
		WANG PART NUMBER	SIZE D	DRAWING NUMBER 7744	REV

DO NOT SCALE

SRIN (4F2)

SW1

PROM SW (2G9)

STATUS (4B5)

STATUS (4B4)

SRCK (4D8)

CTCL (4B3)

SROUT (4G4)

DOL (4B6)

DIS (4C5)

FXE (4D6)

HOP (3A7)

PAKE (2A9)

RSO 2.2K +5VR

BK1 (3B8)

PARE (2A9)

PS1 2.2K +5VR

NO DATA (4G6)

BK1 (3F6)

I.E (3E10) (1G2)

PCLK (4C5)

FXE (4D6)

STATUS CLR (4B1)

EDL (1L7)

SWMUX (2A9)

MR (L2)

MR (1G4)(1E1)

DIS (4C5)

LWR (3E9)

HOP (3G5) (3G8)

DO-D7 (2D9)

D0 D1 D2 D3 D4 D5 D6 D7

145T (4G1)

T1 (4A6)(1D8)(3B6)

T2 (4C9)(4A5)(4B4)

T3 (4D3)

T4 (4C3)

T1·T2 (3B6)

LRD (4A5)(1G2) (4D3)

IBT (4A1) (5C1)

2.5 4BT (4G5)(1G1)(4E5)

LWR (3B8)(4A5) (1G2)

TRANS (1D8)

C138 .390pf

DLCL (4D1)

REC (4C3) (4D6)

REC (4G10) (4B7)

EDL (1C9)

T1·T2 (3F1)

T1 (3F2)

A0-A15 (1D3)(2D11)(2D9)

BK2 (1D10)

ENDRST (4B2)

RESTART (4B2)

DL RESTART

MI (1E9)

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

C72 470pf

C73 470pf

C138 .390pf

+5VR

±0V

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DAN R.S	5-15-78	E ENGR	
		CHE		M ENGR	
MATERIAL	MODEL NO AP-CHIVER SEE ENGRG SPECIFICATIONS			MFG ENGR	
FINISH	TOL UNLESS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH	TITLE DATA LINK MEMORY			
	SCALE NONE SHT 3 OF 7	SEE SHEET	D	7744	14
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

REVISION | SEC SHEET 7

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

CK SHIELD #1 (±0V) (19₃)

CK SHIELD #2 (±0V) (21₃) ±0V

XTAL 17.1 MHz

R66 330Ω R67 330Ω C78 680pF L127 504 L127 5049 L127 5049 TP2 TP1

CK (20₃)

R53 39K +5VR C74 .0015μF SRIN (4FZ) RM4 22K +5VR

R54 22K +5VR C75 100pF ±0V

L85 9602 L85 9602 CLR2 CLR1

INST (3G3)

L27 L25 532 L40 08 → BK9 (4DZ)

NO DATA (3B9)

→ PARST (1F5)

SROUT (2D8) L40 08

L125 113 1A 1B 2A 2B 2C 1C 1Y 1S 2Y 2S 1P 2P

R57 2.2K +5VR

R58 270Ω +5VR DLE (14₃)

R59 Ω R60 390Ω +5VR R61 91Ω

+GA (K₃) TMC +GB (L₃) -RA (S₃) BMC -RB (M₃)

→ TXE (3E7)

REC (3D4)

+5VR P55 2.2K ±0V

L112 04

L128 74LS161 ENP ENT A B C D CK LD CLR QA QB QC QD RCO

L111 7474 2CLR 2D 2Q 2CK 2PR 2Q̄ → RXE (4F2)

+5VR RB3 2.2K

L130 7474 2PR 2D 2Q 2CK 2CLR 2Q̄

L111 7474 1CLR 1CK 1Q 1D 1PR 1Q̄ → TXE (3B10) (3G8)

REC (3D4)

L99 508 L89 02 R63 2.2K +5VR

L130 7474 1PR 1CK 1Q 1D 1CLR

→ SRCK (3D9)

L99 502 L98 500 L127 5049 L127 5049 L99 08

+5VR R68 2.2K

L109 S194 SR SHR SHL QA QB QC QD

SRIII (4F2) L96 532 L96 532

±0V

L109 161 LD ENP ENT CK A B C D RCO QA QB QC QD

R69 +5VR 2.2K ±0V

L110 S138 G1 G2B G2A A B C Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

L84 04 L95 502 L95 502 L84 04 L84 04 L40 08 → PCLK (3310)

→ DIS (3B8) (3G10)

L41 08 REC (3D4) L95 508 → DOL (3C9)

T7 (1F5) L84 04 TRCL (4B2) 112 04

Te (4C8) CO (3A9) +5VR R56 2.2K

L100 7474 2PR 2D 2Q 2CK 2CLR 2Q̄

L126 75107A 1A 1B 1G STB 2B 2A 2G 1Y 2Y CBO Vcc-

R62 2.2K +5VR L95 502 RXE (4E6) SRIN (3G8) (4G9) (4B11)

C81 .05μF 15μF 20V(T) ±0V -5V

25687 (3E5)

L86 7474 2CLR 2D 2Q 2CK 2PR 2Q̄

L100 7474 1CLR 1D 1Q 1CK 1PR 1Q̄

R64 2.2K +5VR

L30 00 (3A4) CO → CO (1F5)

KDLS (1B9)

L29 EDL (1D9) L100 7474 1PR 1CK 1Q 1D 1CLR

T2 (3F2) L99 508 ENDIT (4A6)

LRD (3F4) L39 20 L39 20 L38 30 L38 30 L39 02 → DLCL (3E5)

BK9 (4G6) L112 04 +5VR R65 2.2K

IBT (3E4) T3 (3F2) L98 00 L96 32 L96 32 T4 (3F3) C79 220pF IOV

REC (3D4) L97 7474 1PR 1D 1Q 1CK 1CLR → TRCL (3D9)

TRCL (4C8)

STATUS (3D9) L41 08 L37 10 → STATUS CLR (2A C)

RESTART (3C2) L34 10

ENDRST (3D1) EB (1D7)

L37 10 T2 (3F2)

L84 04 ±0V L101 153 1G0 1G3 1C1 1C2 2C0 2C1 2C2 2C3 1Y 2Y

T1 (3F2) L39 508 T2 (3F2) ENDIT (4C3) L98 500 IBT (3E4)

LRD (3F4) LWR (3E4)

L127 5049 L127 5049 L99 08 L127 5049 TP2 TP1

L99 502 L98 500 L96 532 L96 532

L84 04 L84 04 L95 502 L95 502 L40 08 L41 08 L95 508 L89 02 L39 508 L99 508

L112 04 L112 04 L39 20 L39 20 L38 30 L38 30 L39 02 L98 00 L96 32 L96 32 L37 10 L34 10

L29 L99 508 L98 500 L39 508

L127 5049 L127 5049

REVISION NO	SEE SHEET 7		

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	AG	5-[illegible]	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL — MODEL NO ARCHIVER — SEE ENGRG SPECIFICATIONS No. —

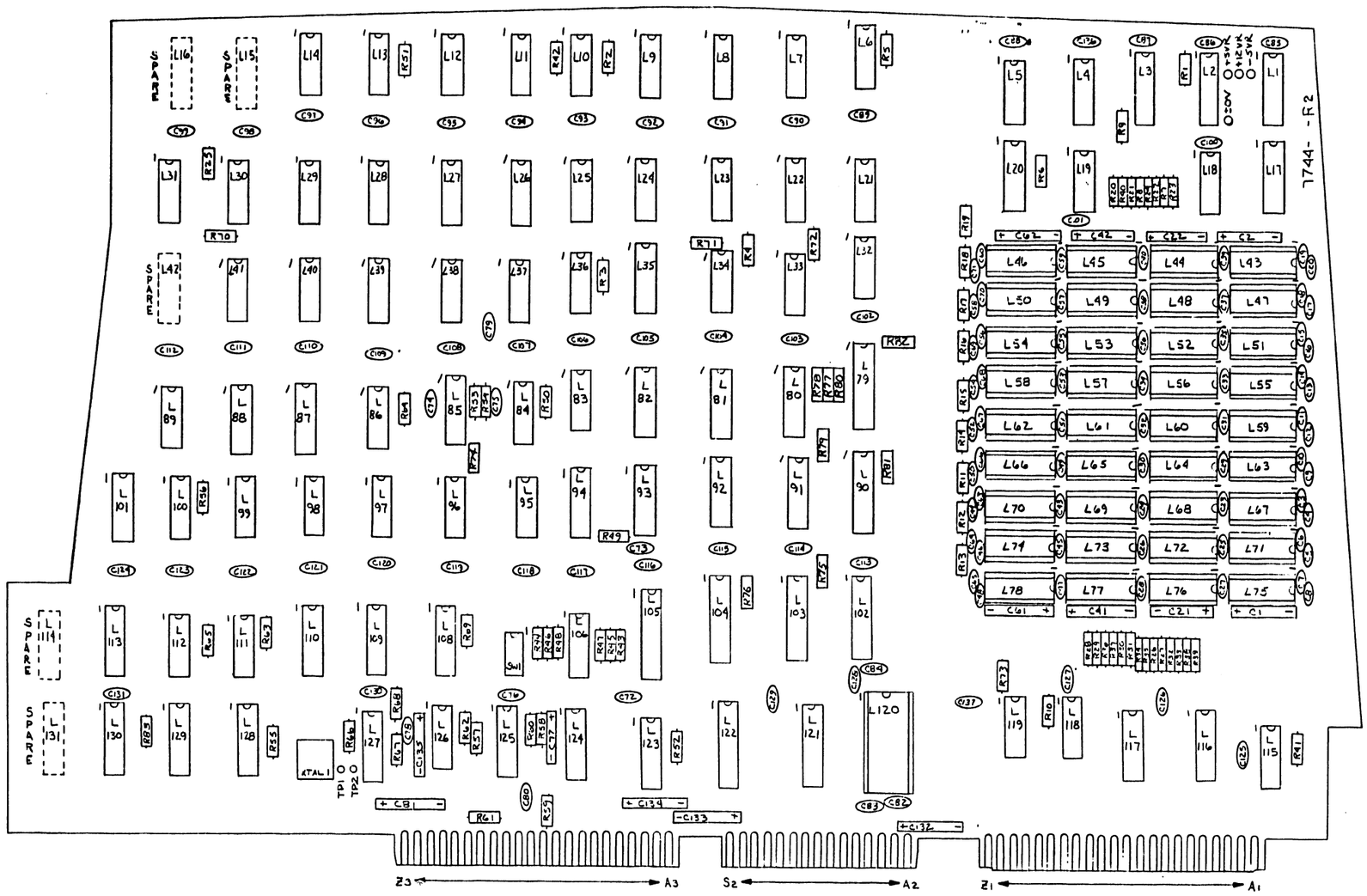
FINISH — TOL EX AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH √

TITLE: DATA LINK MEMORY

SCALE — WANG PART NUMBER — SIZE D — 7744 — DRAWING NUMBER — REV

F S.C.L.

DO NOT SCALE



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN WS	6-1-3/4	E ENGR	
		CHK		M 'NGR	
MATERIAL	MODEL NO ARCHIVER			MFG ENGR	
	SEE ENGRG SPECIFICATIONS No.	TITLE DATA LINK MEMORY			
FINISH	TOL EE AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH √	SEE CHART	D	7744	4
	SCALE — SHT 5 OF 7	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

NO.	REVISION	DATE	APPROVED
M	SEE SHEET 7		

DO NOT SCALE

210 = 209 + 377 OR 378						
210	209	L43, 47, 51, 55, 59, 63, 67, 71, 75	L44, 48, 52, 56, 60, 64, 68, 72, 76	L45, 49, 53, 57, 61, 65, 69, 73, 77	L46, 50, 54, 58, 62, 66, 70, 74, 78	L120
7744-A	7744	377-0345				
7744-1A	7744-1	377-0345	377-0345			
7744-2A AWS-22666	7744-2	377-0345	377-0345	377-0345		
7744-2B	7744-2					378-4302
7744-3A	7744-3	377-0345	377-0345	377-0345	377-0345	
7744-B	7744	377-0345				378-4399
7744-3B	7744-3	377-0345	377-0345	377-0345	377-0345	378-4256
7744-3C	7744-3	377-0345	377-0345	377-0345	377-0345	378-4251
7744-3D	7744-3	377-0345	377-0345	377-0345	377-0345	378-4417

NO	REVISION	BY	DATE
	SEE SHEET 2 OF 7		

WANG LABORATORIES, INC. LOWELL, MASS.

	BY	DATE	APPROVED BY	DATE
DWN			E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO 2236A PRINTER

SEE ENGR'G SPECIFICATIONS

No.

FINISH

TOL ON AS NOTED

TITLE DATA LINK MEMORY

SEE CHART D

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

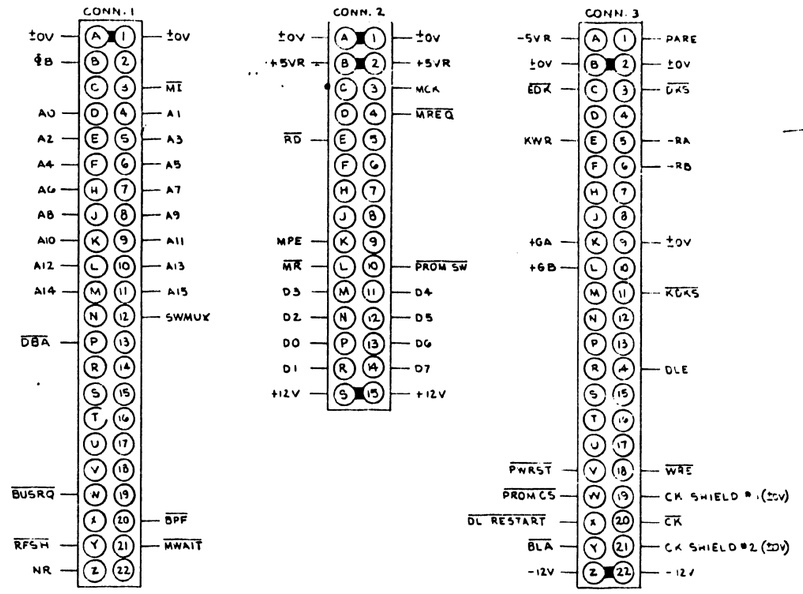
DO NOT SCALE

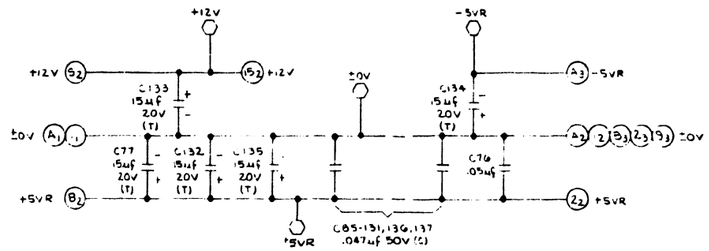
COMPONENT	TYPE	W.L. PART NO.
C1,2,21,22,41,42, 61,62	5.0µf 35V(T)	300-4017
C3-20,25-40, 43-60,63-71, 82-84	.1µf 50V H.F. (C)	300-1930
C72,73	470pf 500V (C)	300-1470
C74	.0015µf 500V(C)	300-1907
C75	100pf 500V (C)	300-1100
C76,80,85-131, 136,137	.047µf 50V (C)	300-1966
C77,81,132-135	15µf 20V (T)	300-4022
C78	680pf 500V(C)	300-1680
C79	220pf 500V(C)	300-1220
C138	390pf 500V(C)	300-1390
R1-6,9,25,41-52, 55-57,62-65,68, 69,71,74,83	2.2K 1/4W 5%	330-3023-48
R7,8,11-23,26-39	33Ω 1/4W 5%	330-1034-48
R10,70,72,73,75-82	10K 1/4W 5%	330-4011-48
R24,40	22Ω 1/4W 5%	330-1023-48
R53	39K 1/4W 5%	330-4043-48
R54	22K 1/4W 5%	330-4023-48
R58	270Ω 1/4W 5%	330-2028-48
R59	100Ω 1/4W 5%	330-2011-48
R60	390Ω 1/4W 5%	330-2039-48
R61	91Ω 1/4W 5%	330-1092-48
R66,67	330Ω 1/4W 5%	330-2034-48
XTAL	15.9A FINNED SVS	600-7007
XTAL	17.1 MHZ HC-18/U	321-0018
L43-78	16 PIN SOCKET	376-9002
L120	24 PIN SOCKET	376-9003
SW1	SPDS SPST	325-1501

TYPE	LOCATION	SPARES
74S00	L98	1
7402	L24	1
	L89	1
7404	L12	1
	L106	1
	L112	1
74S04	L127	2
7408	L10	2
	L41	1
7432	L31	2
	L113	3
7474	L2	1
7410	L119	1
74S11	L21	2

I.C. LOCATION	TYPE	W.L PART NO
L1	7475	376-0013
L2,8,13,23,84,97, 100,111,130	7474	376-0006
L3,92-94,109	74S134	376-0221
L4,6,7,36	74S74	376-0202
L5,127	74S04	376-0197
L9,18,99	74S08	376-0200
L10,26,40,41	7408	376-0081
L11	7481	376-0012
L12,84,106,112	7404	376-0010
L14,22,28,31,113	7432	376-0093
L15,16,42,114,131	SPARES	
L17,110	74S138	376-0298
L19,33,98	74S00	376-0228
L21	74S11	376-0237
L24,89	7402	376-0016
L25,96	74S32	376-0205
L27,30	7400	376-0002
L29	7411	376-0194
L32	74125	376-0324
L34,37,119	7410	376-0003
L35	74LS194A	376-0416
L38	7430	376-0031
L39	7420	376-0004
L43-78	MK4116	SEE CHART
L79	74LS373	376-0313
L80,88	7442	376-0003
L81,82	74157	376-0082
L83	74LS280	376-0241
L85	9602	376-0104
L87,91	74174	376-0098
L90,102,105,122	74LS244	376-0288
L95	74S02	376-0199
L101,120	74153	376-0048
L103,104,121	74LS374	376-0286
L108,123,124,128,129	74161	376-0094
L115	74LS74	376-0155
L116,117	74S157	376-0217
L118	7427	376-0125
L120	2716	SEE CHART
L125	75113	376-0256
L126	75107	376-0149

MNEMONICS	COORDINATE
A0-A15	3A1-3A4
$\overline{BLA}$	2C11
$\overline{BPF}$	1G3
$\overline{BUSRQ}$	1B6
$\overline{CK}$	4A11
CK SHIELD #1	4F11
CK SHIELD #2	4F11
$\overline{DBA}$	1D11
$\overline{DKS}$	1F11
DLA	4G1
$\overline{DL\ RESTART}$	3D1
D0-D7	3A5,3A6
$\overline{EDK}$	1B8
+GA	4G1
+GB	4G1
$\overline{IB}$	1G8
$\overline{KDKS}$	1B9
$\overline{KWR}$	1G2
MCK	1B2
$\overline{MI}$	1E11
MPE	3E11
$\overline{MR}$	3A11
$\overline{MREQ}$	1B11
NR	3F11
PARE	2A9
$\overline{PROM\ CS}$	2A8
$\overline{PROM\ SW}$	3D11
$\overline{PWRST}$	4G5
-RA	4G1
-RB	4G1
$\overline{RD}$	1B5
$\overline{RFSH}$	1B2
SWMUX	1E10
$\overline{WRE}$	1G5





NOTES:
1. ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

7744 E-REV | 7744-1 E-REV | 7744-2 E-REV | 7744-3 E-REV

REVISION	BY	DATE	APPROVED
ORIG ISSUED PER ECO #1133 APPD:		4-19-83	
REVISED PER ECO #2150, 2350, 25500 APPD:		10-31-83	
REVISED PER ECO #2530 APPD:		9-23-82	
REVISED PER ECO #2267 APPD:		4-22-82	
REVISED PER ECO #1959 APPD:		11-27-81	
REVISED PER ECO #1693 APPD:		8-4-81	
REVISED PER ECO #1503 APPD:		3-25-81	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
JWH	3-30	E ENGR	
CHE	4-3-83	M ENGR	
		MFG ENGR	

MATERIAL —#—

FINISH —+—

MODEL NO ARCHIVER

SEE ENGR. SPECIFICATIONS No.

TOL. TO BE AS NOTED .XX ± .XXX ± ANG ± FINISH

SCALE NONE SHT 1 OF 1

TITLE DATA LINK MEMORY

SEE CHART | D | 7744 | 1--

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS TO REMAIN SUBJECT TO THE CONTROL OF WANG LABORATORIES, INC."

DO NOT SCALE

SELIBM (D3)

SELIBM (:A10) (:B1)

SELIBM (1011) (4D3)

OUT OC (12)

SWMUX (11)

INDEX 2 (A1)

SECTOR 2 (2)

INDEX 1 (B1)

SWMUX (1011)

IPO (3B9)

SPO (4D10) (3E11)

SOC (4C7)

MR (1C11) (2E7) (3E3)

MR + DC (3C11)

CEW (1A9) (3B9) (3F2)

ERGT WRGT (F1)

SELIBM (1G6)

RBZ 1GC

DC (3G7)

DC (3C1)

SDF (3D9)

SC (1B3)

WCS (3D11)

SA+CEW (3D11)

C4 (3D9) (1C11)

BIT (1D3) (3C9)

EAB (3D11) (1D9)

FLT (3E6)

BBS (3E4)

XTAL1 10MHz

C1 680PF

R20 330Ω

R21 330Ω

BCN (3G9)

ACK (3F9) (3G9)

ACK + SC (3E2) (1D10)

SC (1G8) (1C11)

TP6

SC (3G9)

CS (3E9)

RCK (3F10)

DDAR

DRS

PARE

SRCOUT (3F9)

HSTD

HWR

SEE SHEET 5

REVISION

NO

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
MATERIAL	MODEL NO. 2200VS P/S A	DWN LDB	7-3-3G	E ENGR	
	SEE ENGR. SPECIFICATIONS	CHK		M ENGR	
	No.			MFG ENGR	
FINISH	TOL. ±2 AS NOTED .X ± .FRAC ± .XXX ± .DEC ± .FINISH √	TITLE ARCHIVER I/O BOARD			
		SCALE SIZE D	DRAWING NUMBER 7843	REV 9	
		DO NOT SCALE	SHEET 1 OF 2		

DO NOT SCALE

NOTE: * INDICATES COMPONENTS THAT ARE NOT LOADED FOR 7843 VERSION.

XTAL 2 2.4576 MHZ

SEE SHEET 5

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
	DRWN L.D.J	7-3-75	E ENGR		
	CHK		M ENGR		
			MFG ENGR		
MATERIAL	MODEL NO. 2200VS PL35A	TITLE	ARCHIVER I/O BOARD		
	SEE ENGRG. SPECIFICATIONS*				
FINISH	TOL. EX. AS NOTED	SEE CHART	D	7843	9
	SCALE CWO LOT 2 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

DO NOT SCALE

BST (12₃)

AUTO RESET (G3)

PROMSW (G2)

WCD (D2)

SC (IA4)

ACK (IB3)

257X (3D1)

BCK (IB3)

237X (3D1)

SROUT (IC9)

SAIN (IE10)

CEN (IB1)

SOC+MR (IG1)

DC (IE4)

STE (4E7)

RDD (15₁)

PB (P₁)

RCK (14₁)

PB (4F4)

PB (1F5) (4F3)

ROT (3D5)

TP7

CS (IG9)

CS (IB5)

SA (IC11)

SPO (IE1)

ECS (IC1)

KWR (1B11)

MR + DC (1G1)

EAB (1C4)

WCS (1D3)

SA + CEN (1E5)

SOR (1D1)

DAY (4E7)

DEV (19)

IND5 (10₄)

RET (S₃ 4₄)

LTE (4E6)

LTE (17)

WB (1₁)

WB (4E6)

LED (12)

BIT (1D5)

KP (4E10)

IPO (1B2)

D0-D7 (1E10) (4E5)

D7 (3F3)

EDKA (1C10)

A0 (1E1) (1G7)

A1 (1E1) (2G8)

A2 (1E1) (RG8)

A3 (1F2) (1G8)

A4 (1E3) (4E6) (2G8)

A5 (2E4) (4E7)

A6 (4E6)

A7 (4F9)

D1 A0

E1 A1

F1 A2

G1 A3

H1 A4

J1 A5

K1 A6

L1 A7

FLI (1B8)

FLI (1D7) (1F9)

BOS (1C7)

TP5

190 (3B2)

30" (1E4)

ESS 2.2K

2550 (1B11)

ACK+SC (1D3)

257X (3G9)

237X (3G9)

C4 (1D4)

DFC (4F1)

ZERO (1D3)

190 (1D6) (3D8)

F/N (4C4) (3F8)

TP1

DC (4E6) (1E5)

D7 (3D8)

OUT 10 (2D1)

MR (1G2)

R45 180Ω

R46 390Ω

R47 180Ω

R48 390Ω

R52 1K

R53 2.2K

R50 2.2K F/N (3B1)

R51 2.2K

R54 2.2K

R55 2.2K

R56 2.2K

R57 2.2K

R58 2.2K

R59 2.2K

R60 15K

R61 2.2K

R62 15K

R64 1K

R85 2.2K

R86 22K

R87 22K

R88 47K

R89 10K

R91 10K

C11 390PF

C12 390PF

C13 390 PF

C14 15UF 20V(T)

C8

35V(T)

REVISION NO. SEE SHEET 5

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN LDS		7-3-74	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL — MODEL NO. 2200VS PL33A — SEE ENGR. SPECIFICATIONS — No.

FINISH — TOL. EX. AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √

TITLE: ARCHIVER I/O BOARD

SCALE NONE — SHT 3 OF 5 — MADE FOR NUMBER — SIZE D — DRAWING NUMBER 7843 — REV 9

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO, WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS TRANSFERED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE

IORQ (N1)
MCK (3K)
RD (2P2)
INT ME (N1)
MI (2J)
OUT OA (6J)
OUT 08 (4J)
OUT08 (16G)
WR (2N)
KP (H4)
KP (3C9)(2B7)
ΦA (T1)
ΦB (1F4)
A7 (3A5)
A6 (3A5)
A5 (3A5)
A4 (3A5)
AG (3A5)
MRC (2D6)
DRY (3C9)
SRE (3F9)
SOR (1D1)
WR (3B10)
LTE (1C8)
DC (3C1)
SPO (1E2)
SOC (16I)
SELTBN (16G)
INT (10J)
MI - IORQ (2M2)(2B7)
F/N (3B1)
EOKA (1C10)
LED (4J)
SHIELD (U1)
C19-64 .047UF
C17 15UF 20V(T)
C65 15UF 20V(T)
C18 15UF 20V(T)
C66 15UF 20V(T)
+12V
-12V
+5VR
±0V
A15
A14
A13
A12
A11
A10
A9
A8

NOTE: * INDICATES COMPONENTS THAT ARE NOT LOADED FOR 7843 VERSION.

REVISION	BY	DATE	APPROVED BY	DATE
	DWN LDB	7-3-81	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL — MODEL NO. 2200VS PA33A — SEE ENGR. SPECIFICATIONS No.

FINISH — TOL. EX. AS NOTED: XX ± FRAC. ± / XXX ± ANG. ± / FINISH √

TITLE: ARCHIVER I/O BOARD

SCALE CHD | SHT 4 OF 7 | SEE CHART | SIZE D | DRAWING NUMBER 7843 | REV 9

WANG PART NUMBER

DO NOT SCALE

210=209 + 377 OR 378

210	209	L12,25	L13,14	L26	L27	L37	L38	L51	L52,53	L67	L87	L73	L74	L78,79	L92	L103	R24-29,32-35,37,38,41,42,78	R30,31	R34,43	R39	R40	R44	C3	C4	C5	C6	C7	J1	JMPR1	JMPR2	JMPR3	Q1	Q2	J2	SW1	XTAL2	L24
7843-1A	7843-1	376-0077	376-0076	376-0005	376-0104	376-0285	377-0352	376-0297	376-0288	376-0006	376-0294	377-0371	377-0373	376-0094	376-0286	376-0126	330-3022	330-2047	331-2012	330-5034	330-3016	330-1068	300-1911	300-1903	300-1906	300-2147	300-1047	376-9016	LOADED	LOADED	LOADED	375-1012	375-1014	350-0046	325-1501	321-0027	376-0282
7843-A	7843											377-0371	377-0373																								

MNEMONICS	COOR'D.
AB	2G4
$\overline{AET}$	3C11
AUTO RESET	2G1
AØ-A7	3A6
AB-A15	4B1
$\overline{BA}$	2B3
$\overline{BB}$	2G3
$\overline{BST}$	3G4
CA	2B3
$\overline{CB}$	2G2
$\overline{CC}$	2G2
$\overline{CF}$	2G2
$\overline{CD}$	2B3
CSP	2G2
$\overline{DB}$	2G3
DD	2G3
$\overline{DKS}$	1A5
$\overline{DPAR}$	1A5
$\overline{DRY}$	3F11
DØ-D7	1F11
$\overline{EDK}$	1D11
$\overline{ERGT/WRGT}$	1F11
$\overline{HDIR}$	4E1
$\overline{HDLT}$	4F1
$\overline{HDLZ}$	4F1
$\overline{HSTP}$	1A10
$\overline{INDEX1}$	1G5
$\overline{INDEX2}$	1G5
$\overline{INDS}$	3C11
$\overline{INT}$	4A1
$\overline{INTM2}$	4G4
$\overline{INTTC}$	2A5
$\overline{IORQ}$	4G9

MNEMONICS	COOR'D
$\overline{BA}$	4E11
$\overline{BB}$	3F11
$\overline{OUT\ OA}$	4G2
$\overline{OUT\ OB}$	4G1
$\overline{OUT\ OC}$	1G6
$\overline{OUT\ OB}$	1B11
# SH'ELD	4C11
PARE	1A5
P/C WAIT	4G1
$\overline{PROMSW}$	3F1
$\overline{RCK}$	3F11
$\overline{RD}$	2G2
$\overline{RDD}$	3F11
SCA	2B3
$\overline{SECTOR1}$	1G5
$\overline{SECTOR2}$	1G5
$\overline{SELIBM}$	1G7
$\overline{SFLT}$	4F1
$\overline{SFL2}$	4F1
SWMUX	1G5
$\overline{WCD}$	3E1
$\overline{WP}$	3B11
$\overline{WR}$	2D1
KDKS	1C11
KP	4E11
$\overline{KWR}$	1A10
$\overline{LED_1}$	3A10
$\overline{LED_2}$	4C11
$\overline{LTZ}$	3B11
MCK	4G7
$\overline{MR}$	1G2
$\overline{MT}$	4G4

CONN.1

$\overline{SECTOR1}$	A 1	$\overline{INDEX2}$	
$\overline{INDEX1}$	B 2	$\overline{SECTOR2}$	
$\overline{WR}$	C 3	$\overline{HSTP}$	
AØ	D 4	A1	
A2	E 5	A3	
A4	F 6	A5	
A6	H 7	A7	
A8	J 8	A9	
A10	K 9	A11	
A12	L 10	A13	
A14	M 11	A15	
$\overline{IORQ}$	N 12	SWMUX	
BB	P 13		
	R 14	$\overline{RCK}$	
	S 15	$\overline{RDD}$	
BA	T 16		
# SHIELD	U 17	$\overline{LTZ}$	
$\overline{WP}$	V 18	$\overline{INT}$	
	W 19	$\overline{DRY}$	
	X 20		
	Y 21		
$\overline{MT}$	Z 22		

CONN.2

±0V	A 1	±0V	
+5VR	B 2	+5VR	
P/C WAIT	C 3	MCK	
$\overline{WCD}$	D 4		
$\overline{RD}$	E 5	$\overline{SFLT}$	
$\overline{ERGT/WRGT}$	F 6	$\overline{PROMSW}$	
$\overline{OUT\ OB}$	H 7	$\overline{OUT\ OC}$	
	J 8	$\overline{OUT\ OB}$	
$\overline{HDLZ}$	K 9	$\overline{HDIR}$	
$\overline{MR}$	L 10	$\overline{HDLT}$	
D3	M 11	D4	
D2	N 12	D5	
DØ	P 13	D6	
D1	R 14	D7	
+12V	S 15	+12V	

CONN.3

	A 1	$\overline{SFL2}$	
±0V	B 2		
$\overline{EDK}$	C 3	$\overline{DKS}$	
$\overline{SELIBM}$	D 4		
$\overline{KWR}$	E 5	$\overline{OUT\ OA}$	
	F 6	AUTO RESET	
	H 7		
	J 8		
	K 9		
	L 10		
	M 11	KDKS	
	N 12	BST	
	P 13		
	R 14		
$\overline{AET}$	S 15		
	T 16		
	U 17		
	V 18		
	W 19	$\overline{INT\ M2}$	
	X 20		
	Y 21		
-12V	Z 22	-12V	

CONN.4

	A 1		
	B 2	$\overline{DPAR}$	
	C 3		
PARE	D 4	$\overline{AET}$	
	E 5		
KP	F 6	$\overline{INTTC}$	
	H 7		
	J 8		
	K 9		
	L 10	$\overline{INOS}$	
	M 11		
	N 12		
	P 13		
	R 14		
	S 15		
	T 16		
	U 17		
	V 18		
	W 19	$\overline{LED1}$	
$\overline{LED2}$	X 20		
+5VR	Y 21	+5VR	
±0V	Z 22	±0V	

J1

CSP	1 24	CSP	
CF	2 23	CF	
CD	3 22	CD	
SCA	4 21	SCA	
CC	5 20	CC	
	6 19		
CB	7 18	CB	
DD	8 17	DD	
CA	9 16	CA	
BB	10 15	BB	
DB	11 14	DB	
BA	12 13	BA	

J2

	1 14		
BA	2 15	DB	
BB	3 16		
CA	4 17	DD	
CB	5 18		
CC	6 19	SCA	
AB	7 20	CD	
CF	8 21		
	9 22		
	10 23		
SCA	11 24		
CSP	12 25		
	13 26		

IC TYPE	LOCATION	SPARES
7400	L43	1
7404	L3	5
	L98	2
74S04	L2	3
7407	L90A	3
7410	L85	1
7411	L18	1
	L40	2
7438	L1	2
	L100	2
7473	L31	1
7474	L99	1
9602	L27	1
	L33	1
74LS244	L52	1

NOTE:
1. ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.
2. DO NOT LOAD P/N 376-9015 IN L38 ON PLAIN REVISION.

REVISION	NO	WHO	DATE	ECN
[illegible]	2	[illegible]	8-12-82	[illegible]
REVISED PER ECO # 22089 APP'D: [illegible]	3	[illegible]	3-3-82	[illegible]
REVISED PER ECO # 22533 APP'D: [illegible]	4	[illegible]	7/25/01	[illegible]
REVISED PER ECO # 23567 APP'D: [illegible]	5	[illegible]	7/25/11	[illegible]
REVISED PER ECO # 21584 25823,24123,24124, 24243,24252 APP'D DOC # 23821	6	[illegible]	3/21/84	[illegible]
REVISED PER ECO # 23695 APP'D: [illegible]	7	[illegible]	5-31-85	[illegible]
REVISED PER ECO # 23694 APP'D: [illegible]	8	[illegible]	6-24-85	[illegible]
REVISED PER ECO # 24680 APP'D DOC # 24841	9	[illegible]	11/12/86	[illegible]

E-REV 2 7843
E-REV 2 7843-1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN LDB	7-3-82	ENGR	
	CHK		M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. 2200VS P/334		TITLE ARCHIVER I/O BOARD	
	SEE ENGR SPECIFICATIONS			
FINISH	TOL EX AS NOTED		SEE CHART / D / 7843 / 9	
	SCALE	SHT 1 OF 1	WANG PART NUMBER / SIZE / DRAWING NUMBER / REV	

WANG LABORATORIES, INC

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

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