WANG

CONTROL DATA CORPORATION
FIXED STORAGE DRIVE
THEORY
Volume 2

Models:

PA5G1/G2	(Wang 2268V-3)
PA5N1/N2	(Wang 2268V-4)

COMPANY PROPRIETARY STATEMENT

Customer Engineering
OEM Reprint

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PREFACE

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to troubleshoot and repair the Control Data Corporation Fixed Storage Drive, Wang 2268V-3 and Wang 2268V-4.

First Edition (April 1985)

This document is a reprint of volume 2 of the Maintenance Manual for the Control Data Corporation Fixed Storage Drive. The material in this document may be used only for the purpose stated in the Preface. Updates and/or changes to this document will be published as Publications Update Bulletins (PUB's) or subsequent editions.

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CD CONTROL DATA
CORPORATION

CDC® FIXED STORAGE DRIVE

PA5G1

PA5G2

PA5N1

PA5N2

THEORY OF OPERATION

GENERAL MAINTENANCE INFORMATION

TROUBLE ANALYSIS

ELECTRICAL CHECKS

REPAIR AND REPLACEMENT

Volume 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
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B (11-26-84)	Manual revised to incorporate series codes 05 and 06 changes.

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    Customer Documentation Dept.
    5950 Clearwater Drive
    Minnetonka, MN. 55343
or use Comment Sheet in the back
of this manual.

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LIST OF EFFECTIVE PAGES

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PREFACE

This manual contains maintenance information for the CONTROL DATA® PA5G1/2 and PA5N1/2 Fixed Storage Drives (FSDs). It is prepared for customer engineers and other technical personnel directly involved with maintaining the FSD.

The information in this manual is presented as follows:

Section 1 - Theory of Operation. Describes power functions, electromechanical functions, interface, unit selection, servo surface decoding, sector detection, seek functions, head selection, read/write functions, and fault detection.

Section 2 - General Maintenance Information. Contains information on warnings and precautions, maintenance tools and materials, testing the drive, and accessing the drive for maintenance.

Section 3 - Trouble Analysis. Contains procedures and information to assist in troubleshooting the drive.

Section 4 - Electrical Checks. Provides electrical test procedures.

Section 5 - Repair and Replacement. Contains procedures and information on the replacement and adjustment of drive assemblies.

The following manuals apply to the FSD and are available from Control Data Corporation, Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

Publication No.	Title
83324760	PA5G1/PA5G2 and PA5N1/N2 Hardware Maintenance Manual, Volume 1 (contains general description, operation, installation and checkout information, and parts data)
83324770	PA5G1/PA5G2 and PA5N1/N2 Hardware Maintenance Manual, Volume 2
83324780	PA5G1/PA5G2 and PA5N1/N2 Hardware Maintenance Manual, Volume 3 (contains diagrams)
83322440	CDC Microcircuits, Volume 1 (provides functional descriptions for integrated circuits)
83324440	CDC Microcircuits, Volume 2 (provides functional descriptions for integrated circuits)

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IMPORTANT SAFETY INFORMATION AND PRECAUTIONS

Proper safety and repair is important to the safe, reliable operation of this unit. Service should be done by qualified personnel only. This maintenance manual describes procedures recommended by the manufacturer as effective methods of servicing the unit. Some of these procedures require the use of specially designed tools. For proper maintenance and safety, these specially designed tools should be used as recommended.

The procedures in this maintenance manual and labels on the unit contain warnings and cautions which must be carefully read and observed in order to minimize or eliminate the risk of personal injury. The warnings point out conditions or practices that are potentially hazardous to maintenance personnel. The cautions point out practices which, if disregarded, could damage the unit and make it unsafe for use.

For the safety of maintenance and operating personnel, the following precautions must be observed:

- Perform all maintenance in accordance with the procedures given in this manual.

- Read and observe all cautions and warnings provided in the procedures and labeled on the unit.

- Use the special tools called out in the maintenance procedure.

- Observe sound safety practices when performing maintenance.

- Use caution when troubleshooting a unit that has voltages present. Remove power from unit before servicing or replacing components.

- Wear safety glasses when servicing units.

- Wear safety shoes when removing or replacing heavy components.

It is also important to understand that these warnings and cautions are not exhaustive. The manufacturer could not possibly know, evaluate and advise maintenance personnel of all conceivable ways in which maintenance might be performed or the possible risk of each maintenance technique. Consequently, the manufacturer has not completed any such broad evaluation. Thus, any persons who use any non-approved maintenance procedure or tool must first satisfy themselves that neither their safety nor the unit performance will be jeopardized by the maintenance techniques they select.

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ABBREVIATIONS

A	Ampere	CLK	Clock
ABV	Above	CLR	Clear
ac	Alternating Current	cm	Centimeter
ADD	Address	CNTR	Counter
ADDR	Address	COMP	Comparator
ADJ	Adjust	CONT	Control
ADRS	Address	CONTD	Continued
AGC	Automatic Gain Control	CT	Center Tap
ALT	Alternate	CYL	Cylinder
AM	Address Mark	D/A	Digital to Analog
AME	Address Mark Enable	dc	Direct Current
AMP	Amplifier, Ampere	DET	Detect
ASSY	Assembly	DIFF	Differential
BLW	Below	DIV	Division
C	Celsius	DLY	Delay
CB	Circuit Breaker	DRVR	Driver
CDA	Complete Drive Assembly	ECL	Emitter Coupled Logic
CDC	Control Data Corporation	ECO	Engineering Change Order
CH	Channel	EN	Enable
CHK	Check	ENBL	Enable

ABBREVIATIONS (Contd)

EXT	External	IND	Index	
F	Fahrenheit, Fuse	INTRPT	Interrupt	
FCO	Field Change Order	I/O	Input/Output	
FDBK	Feedback	IPB	Illustrated Parts Breakdown	
FIG	Figure	IPS	Inches per Second	
FLT	Fault	kg	Kilogram	
FSD	Fixed Storage Drive	kPa	Kilopascal	
ft	Foot	kW	Kilowatt	
FTU	Field Test Unit	lb	Pound	
FWD	Forward	LED	Light Emitting Diode	
GND	Ground	LSI	Large Scale Integration	
HD	Head	LTD	Lock to Data	
HEX	Hexagon	m	Meter	
Hg	Mercury	MAX	Maximum	
HR	High Resolution	MB	Megabyte	
HYST	Hysteresis	MEM	Memory	
Hz	Hertz	MHz	Megahertz	
IC	Integrated Circuit	mm	Millimeter	
IDENT	Identification	MPI	Magnetic Peripherals, Inc.	
in	Inch			

ABBREVIATIONS (Contd)

MPU	Microprocessor Unit	PS	Power Supply
MRK	Mark	PWR	Power Supply
ms	Millisecond	RCVR	Receiver
MTR	Motor	RD	Read
mV	Millivolt	RDY	Ready
NC	No Connection	REF	Reference
NORM	Normal	REQ	Request
NRZ	Non Return to Zero	RES	Resolution
ns	Nanosecond	REV	Reverse, Revision
OC	On Cylinder	RGTR	Register
OS	One-Shot	r/min	Revolutions Per Minute
OSC	Oscillator	RSD	Removable Storage Drive
P	Plug	RTZ	Return to Zero
PD	Peak Detect	R/W	Read/Write
pF	Picofarad	s	Second
PG	Page	S/C	Series Code
PHH	Phillips Head	SEC	Second
PLO	Phase Lock Oscillator	SEL	Select
PROC	Procedure	SEQ	Sequence
PROG	Programmable	SPD	Speed

ABBREVIATIONS (Contd)

SS	Sector Switch		W	Watts
T	Tracks to go		W/	With
TF	Thread Forming		W/O	Without
TIM	Timer		W PROT	Write Protect
TP	Test Point		W+R	Write or Read
TSP	Troubleshooting Procedure		W·R	Write and Read
TTL	Transistor-Transistor Logic		WRT	Write
			XFR	Transfer
V	Volts, Voltage		Ω	Ohms
Vbb	Bias Voltage		$	Hexadecimal Address
VCC	Bias Voltage		uF	Microfarad
VCO	Voltage Controlled Oscillator		us	Microsecond

SECTION 1
THEORY OF OPERA-TION

1. THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 1-1):
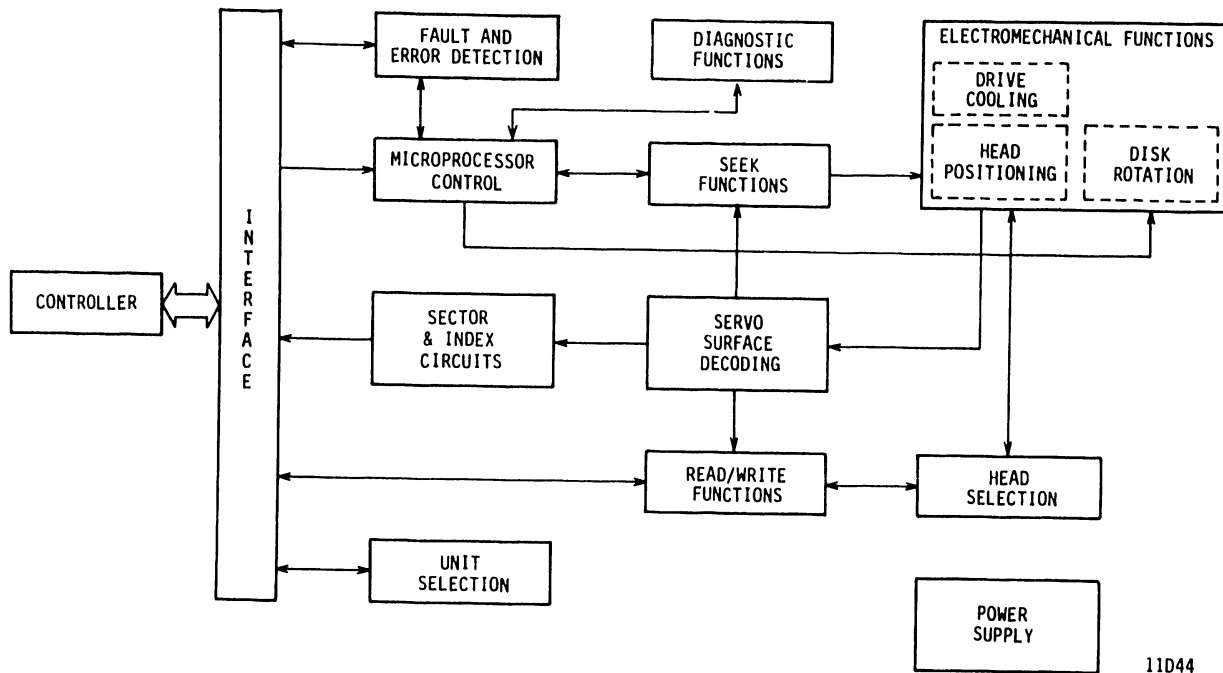
Figure 1-1. Drive Functional Block Diagram

- Power Functions - Describes how the drive provides the voltages necessary for drive operation.

- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drive disk rotation, head positioning, and air flow systems.

- Interface - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.

- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.

- Servo Surface Decoding - Explains how the decoding of the data read from the servo surface by the servo head is used to locate the radial position of the heads during a seek movement, the rotational position of the disks (indicated by the Index signal) when the heads are on track, and the exact speed of the disks (indicated by the 2.41/1.612 MHz clock signal).

- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.

- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disks.

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in volume 3 of the hardware maintenance manual should take precedence over those in this section if there is a conflict between the two.

POWER FUNCTIONS

GENERAL

Power functions are processes that take place within the power supply and the drive when the drive is powered up and powered down. These processes depend on whether the drive is set up for local or remote operation. In all cases, the power up and power down sequences are controlled through MPU programming that monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.

- Local/Remote Power Sequencing -- Explains how the drive may be powered up either at the drive or by the controller.

- Power On Sequence -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.

- Power Off Sequence -- Describes how the drive is powered down, including unloading the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply provides the drive with basic dc supply voltages when circuit breaker CB1 is placed in the ON position. The drive itself has no ac power requirements. All drive circuitry, including the electronics, cooling fan, and drive motor, is operated with the dc supply voltages. The ac power cable connects the power supply (through CB1) to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the Installation and Checkout section of Hardware Maintenance Manual, Volume 1.

The dc power cable connects the power supply to the drive. When CB1 is ON, this cable transmits four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -24 V. The -5, -24, and +24 V supplies are protected against overload by pop-out circuit breakers on the power supply. The dc power cable also contains signal lines, which are enabled by control circuitry in the drive, to switch on 40 V dc power to the drive motor and produce disk rotation.

There are secondary power supplies on the drive's Control Board that develop additional bias voltages for certain integrated circuits. One supply steps down the +24 V input and develops a regulated +15 V source. Another supply steps down the -24 V input and develops a regulated -15 V source. A third supply steps down the -15 V supply to develop a regulated bias of -8.3 V for the servo preamp chip.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer to the Fault and Error Conditions discussion.

LOCAL/REMOTE POWER SEQUENCING

The local/remote feature selects whether or not the controller can control starting and stopping the drive motor. Part of drive installation is setting the LOCAL/REMOTE switch (on the drive I/O Board) for either local or remote operation. The LOCAL/REMOTE switch setting determines start conditions for the drive motor during power up. With the LOCAL/REMOTE switch in LOCAL, start conditions require only that the START switch is in the On position. With the LOCAL/REMOTE switch in REMOTE, start conditions require that the START switch is in the On position and that the controller has activated the Sequence Hold and Sequence Pick signals.

In a system of several drives set up for remote operation, all drives receive Sequence Hold and Sequence Pick at the same time. Once Sequence Pick is received, a delay circuit in the I/O circuitry activates +Start Enable after an interval equal to five seconds multiplied by the drive address. Thus, each drive in the system has a unique start-up interval. However, when Sequence Hold goes inactive, it causes all drives to stop their drive motors at the same time.

POWER ON SEQUENCE

The power on sequence takes place in two steps. Power on ini-
tialization occurs when dc power is applied to the drive. Fol-
lowing successful initialization, a load operation occurs each
time that start conditions become available. Figure 1-2 is a
simplified diagram of the power on circuitry, and figure 1-3 is
a flowchart of the sequence. The following paragraphs describe
power on initialization in detail and summarize the load opera-
tion. More information about load operations is given under
Seek Functions.

Placing power supply circuit breaker CB1 ON enables dc power to
the drive. A level detector on the Control Board monitors the
+5 Vdc input from the power supply and sets the -Low Vcc line
high when this input reaches +4.9 V. Until this time, the DC
Master Clear latch is set, and its output, the -DC Master Clear
signal, remains low. In the Sector Counter Gate Array, the low
-DC Master Clear signal resets the sector counter. In
addition, the low -DC Master Clear signal disables the
interface by blocking unit selection and the remote power
sequencing circuitry. In dual channel drives, the low -DC
Master Clear signal blocks unit selection by either controller.

The -MPU Reset line to the MPU goes low when -DC Master Clear
goes low, and it is held low by a one-shot for about 3 ms after
the -Low Vcc line goes high. When -MPU Reset goes high, the
MPU performs three self-test operations to initialize itself.
These tests are as follows:

- The MPU performs a checksum calculation on the ROM con-
  tents. This test validates that the MPU's firmware in-
  structions are readable.

- The MPU tests its internal RAM by writing information in-
  to it and reading it back.

- The MPU initializes its PIAs by sending data to them and
  reading it back.

If the first two tests fail, the MPU halts and all the individ-
ual fault LEDs on the Fault Display Board remain lit. If the
third test fails, the MPU tries to light the First Seek LED and
halts. None of these tests can produce an operating panel
FAULT indication, and there is no way to clear these faults ex-
cept for turning CB1 OFF.
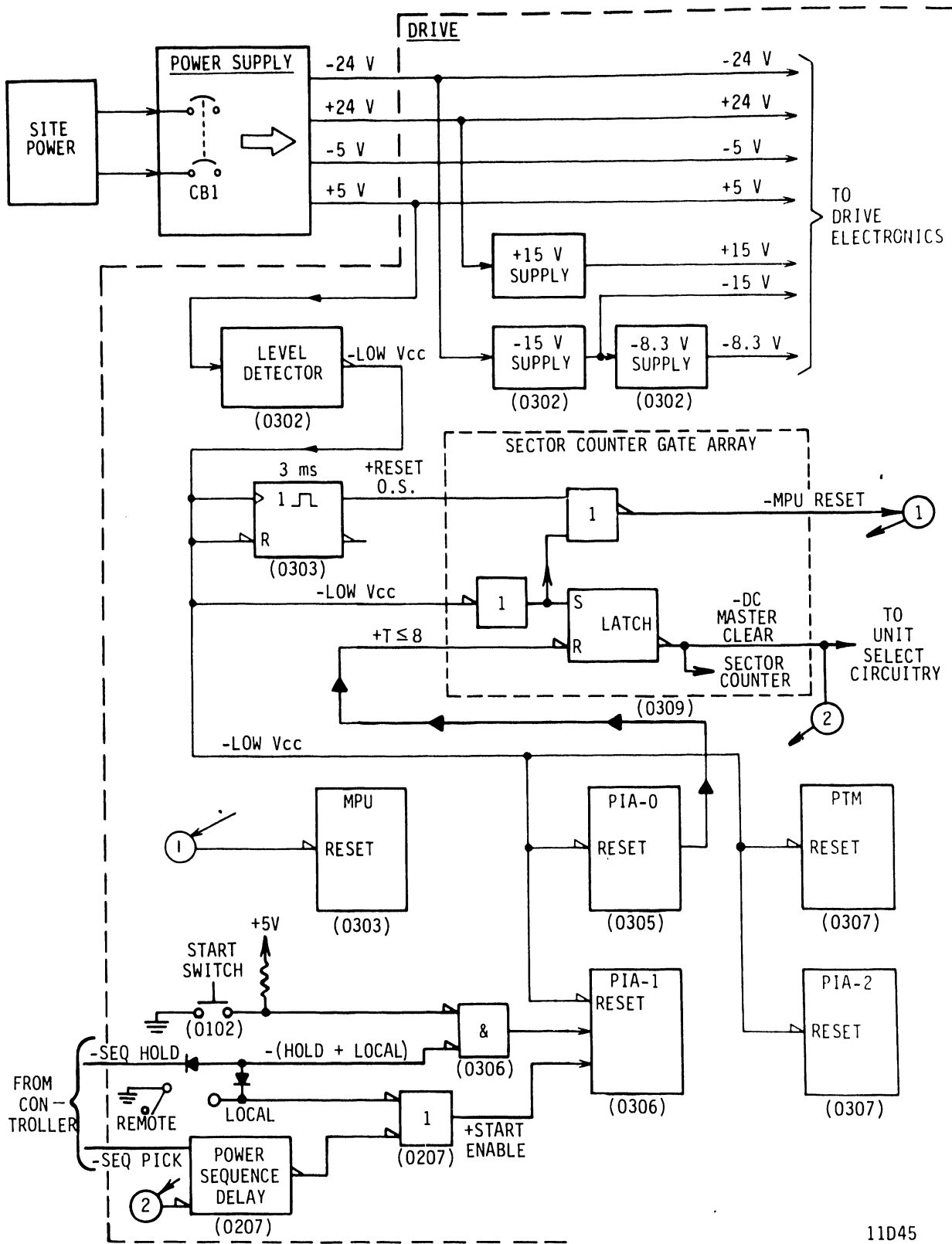
Figure 1-2. Power On Circuitry

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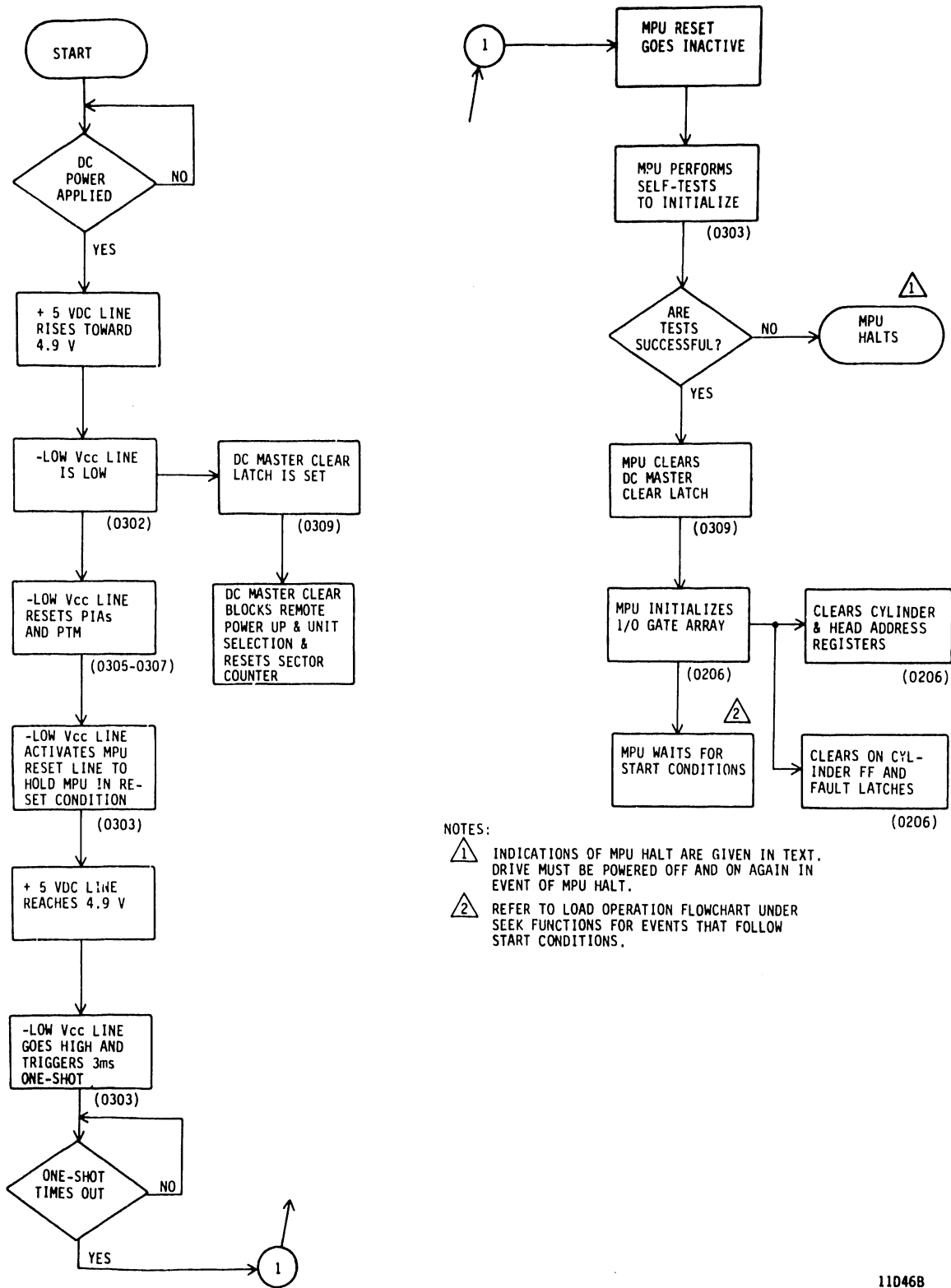
Figure 1-3. Power On Sequence Flowchart

Flowchart text (left column, top to bottom):

START

DC POWER APPLIED — NO / YES

+5 VDC LINE RISES TOWARD 4.9 V

-LOW Vcc LINE IS LOW (0302) → DC MASTER CLEAR LATCH IS SET (0309)

DC MASTER CLEAR BLOCKS REMOTE POWER UP & UNIT SELECTION & RESETS SECTOR COUNTER

-LOW Vcc LINE RESETS PIAs AND PTM (0305-0307)

-LOW Vcc LINE ACTIVATES MPU RESET LINE TO HOLD MPU IN RESET CONDITION (0303)

+5 VDC LINE REACHES 4.9 V

-LOW Vcc LINE GOES HIGH AND TRIGGERS 3ms ONE-SHOT (0303)

ONE-SHOT TIMES OUT — NO / YES → (1)

Flowchart text (right column, top to bottom):

(1) → MPU RESET GOES INACTIVE

MPU PERFORMS SELF-TESTS TO INITIALIZE (0303)

ARE TESTS SUCCESSFUL? — NO → MPU HALTS △1 / YES

MPU CLEARS DC MASTER CLEAR LATCH (0309)

MPU INITIALIZES I/O GATE ARRAY (0206) → CLEARS CYLINDER & HEAD ADDRESS REGISTERS (0206)

MPU WAITS FOR START CONDITIONS △2

CLEARS ON CYLINDER FF AND FAULT LATCHES (0206)

NOTES:

△1 INDICATIONS OF MPU HALT ARE GIVEN IN TEXT. DRIVE MUST BE POWERED OFF AND ON AGAIN IN EVENT OF MPU HALT.

△2 REFER TO LOAD OPERATION FLOWCHART UNDER SEEK FUNCTIONS FOR EVENTS THAT FOLLOW START CONDITIONS.

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With the self-tests complete, the MPU clears the DC Master
Clear latch in the Sector Counter Gate Array and initializes
the circuitry within the I/O Gate Array. The MPU communicates
with the I/O Gate Array via I/O Control lines 1, 2, and 3. The
MPU pulses I/O Control lines 1 and 2 with a serial code that
clears the Cylinder Address register (CAR), the Head Address
register (HAR), the On Cylinder FF, and the Fault latches.

At this point, power on initialization is complete. This pro-
cess will not be repeated until dc power is removed and reap-
plied to the drive (via CB1). The MPU waits for start condi-
tions by monitoring the START switch and (in remote operation)
the Sequence Hold and Sequence Pick signals from the controller.

When start conditions are present, the MPU directs the load
operation. The load operation energizes the drive motor to
bring the disks up to speed and loads the heads to position
them at cylinder zero on the disks. Details of the load opera-
tion are given under Seek Functions. When the load operation
is complete, the drive waits for commands from the controller.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive
motor. There are two conditions that initiate a power off se-
quence. One is a loss of start conditions, and the other is a
loss of dc power to the drive.

A loss of start conditions occurs when the START switch is
pressed to release it from the Start position or (in remote
operation) when the controller deactivates Sequence Hold and
Sequence Pick. The MPU monitors the start conditions and di-
rects an unload operation when they are removed. The unload
operation (discussed under Seek Functions) uses servo control
to move the heads completely outward over the landing zone.
The heads are held in this position by a retract command until
the actuator is locked by the actuator locking solenoid. The
MPU then drops the Motor Run command to disable the Motor Speed
Control, and the friction brake stops the drive motor. The
drive remains in this condition until start conditions reappear.

A loss of dc power results when power supply circuit breaker
CB1 is switched OFF or when there is a loss of site ac power.
When the dc voltages drop, an emergency retract takes place
under hardware control. The emergency retract operation (de-
scribed under Seek Functions) requires no MPU intervention, and
it uses voltage generated by the decelerating drive motor to
drive the heads outward to the landing zone. When the heads
have moved outward to the landing zone, the actuator locking
solenoid automatically holds them in this position. With a
loss of dc power, the drive motor loses its excitation and is
stopped by the friction brake.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices using drive power and working under the control of drive logic circuitry. These functions include disk rotation, head positioning, and drive cooling and ventilation.

DISK ROTATION

General

Disk rotation is accomplished by an electromechanical system that accelerates the disks to 3600 r/min during power up and stops disk rotation with friction braking during power down. The mechanical and electrical aspects of this system are discussed in the following paragraphs.

Mechanical Description

The mechanical components used for disk rotation are the spindle, the drive motor, and the brake.

Spindle

The disks are mounted on the spindle assembly. The spindle, like the disks, is part of the module. When the spindle is rotated by the drive motor, the disks rotate with the spindle.

Drive Motor

The FSD has a direct drive system for disk rotation with the drive motor mounted concentrically on the spindle. The motor has a three-phase stator surrounded by a four-pole rotor. The motor speed control (described in the next topic) provides pulsed excitation to the three stator windings. To keep the stator pulses in phase with rotor position, the speed control uses feedback from sensors located in the motor. These sensors employ the Hall Effect to sense flux reversals from the rotor magnets. As the rotor magnets pass each sensor, its output line toggles.

Electrical Description

General

Electrical operation of the drive motor is discussed in two functional areas:

- Motor Control System -- discusses how the drive motor is started and how its speed is regulated.

- Friction Motor Braking -- discusses how the drive motor is decelerated.

Motor Speed Control

The motor speed control regulates operation of the drive motor. Subject to interlocks, the microprocessor issues a command to start the drive motor during the power on sequence (see Power On Sequence discussion). The motor speed control activates the 40 V dc output of the power supply and uses this power source to excite the stator windings in the drive motor. The control and status lines between these system elements are shown in figure 1-4.

To start the drive motor, the microprocessor drops the -Motor Run line. The drive motor receives power as long as this line is held low. With the -Motor Run line low, the motor speed control issues the -Enable Motor Power command to switch on the 40 V dc output of the power supply. During the interval when jog current is high (see Seek Functions), the MPU activates the +Low/-Hi Start Current line to limit the current drain for the 40 V supply.

The motor speed control divides each shaft rotation of the motor into twelve 30° segments. During each segment, a current path is selected through two of the three stator coils. These stator excitations are timed so that, in each segment, the selected stators exert a counterclockwise torque on the permanent magnets of the rotor.

Rotational position of the motor shaft is relayed to the motor speed control by sensors S1, S2, and S3 located inside the motor. The sensors are positioned at 30° intervals. Each sensor employs the Hall Effect to output a digital level that switches when the polarity of the local magnetic field reverses. The waveforms of S1, S2, and S3 are shown in figure 1-5.

83324770 A
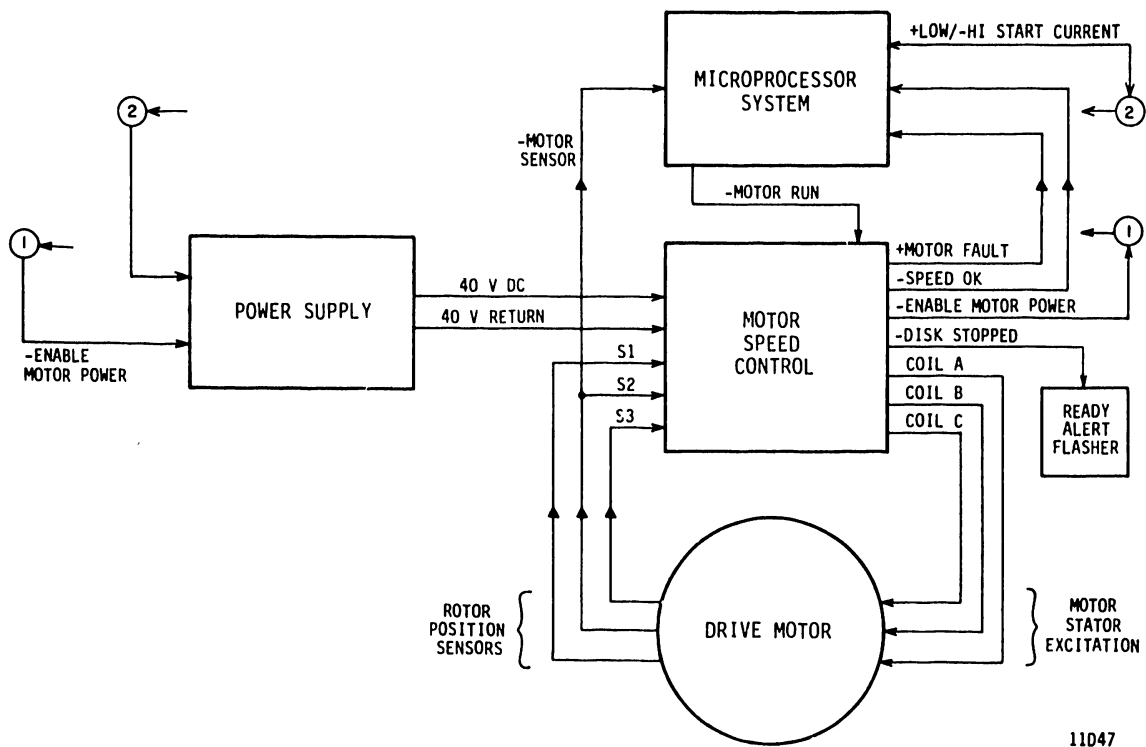
Figure 1-4. Motor Speed Control System Diagram

The motor speed control regulates motor speed by modulating the width of the pulses applied to the stator coils. The motor speed is kept within the following range: 3564 r/min (16.83 ms/rev) to 3636 r/min (16.34 ms/rev). The pulses have maximum width until the rotation time decreases to 16.83 ms. Then the pulse width decreases linearly to a zero value corresponding to a rotation time of 16.34 ms.

Figure 1-6 shows simplified logic for the motor speed control. The control modulates the motor pulses as follows: Once per rotation, a signal called +360° Pulse goes active. This signal triggers a 16.34 ms reference delay, derived by subdividing the 4 MHz clock in the motor speed control. This reference delay corresponds to one motor rotation at the maximum allowable

ONE MOTOR ROTATION
AT SPEED > NOMINAL

ONE MOTOR ROTATION
AT SPEED < NOMINAL

SENSOR S1

SENSOR S2

SENSOR S3

+DRIVE ENABLE

+40V

OPEN

40 V RETURN

COIL A

COIL B

COIL C
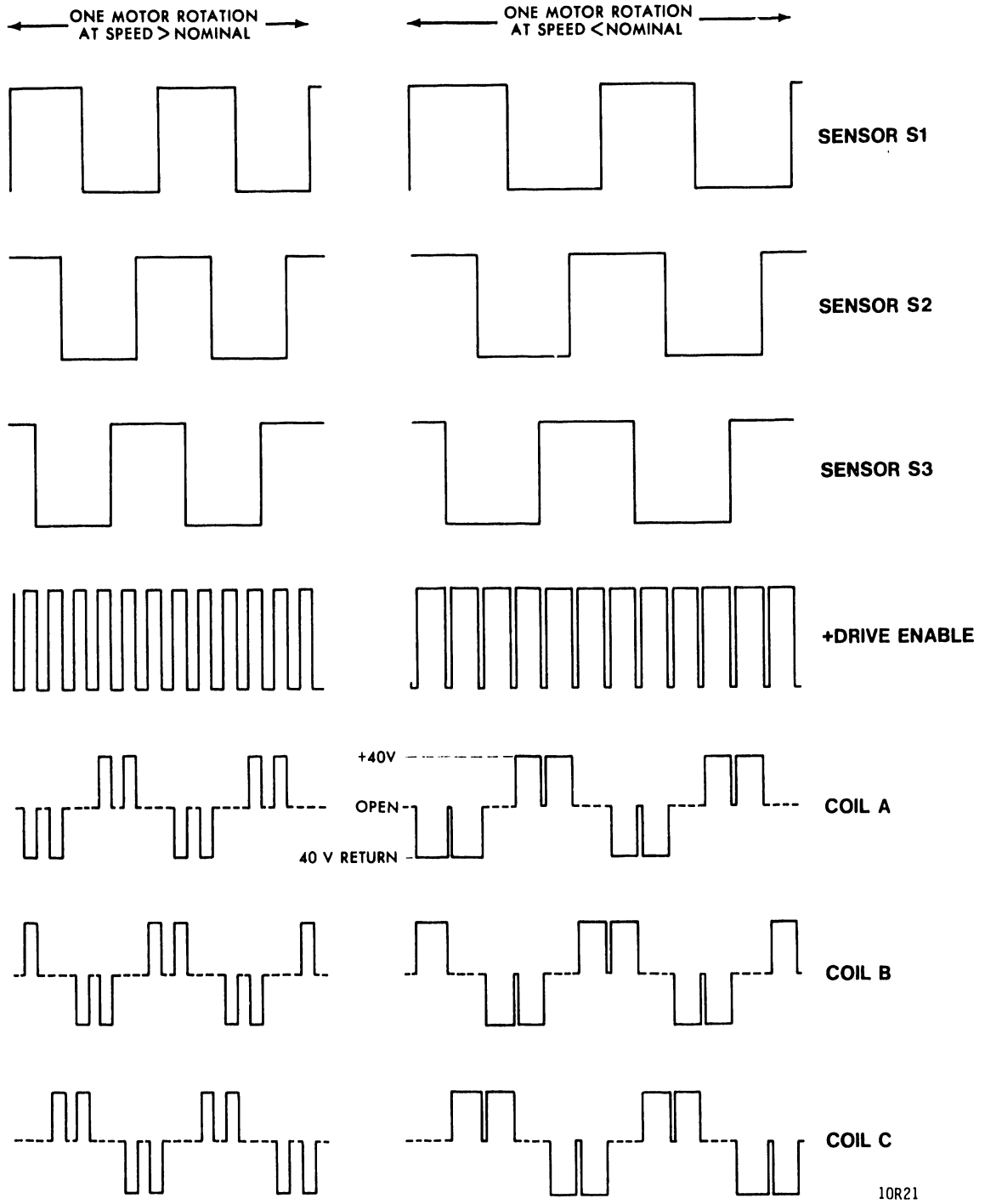
10R21

Figure 1-5.   Speed Control Waveforms and Timing

83324770 A

Figure 1-6.   Motor Speed Control Simplified Logic

MOTOR CONTROL LSI CHIP

4 MHZ OSCILLATOR
(0404)

16.34 ms DELAY GENERATOR

EN

÷2

360° PULSE

COMPARATOR

TRIGGER GENERATOR

30° PULSES

PULSE GENERATOR

+DRIVE ENABLE

S1
S2
S3

SENSOR FAULT

+MOTOR FAULT
(TO MPU)

(0403)

S3
S2
S1

DRIVE MOTOR

STATOR SWITCHING CIRCUITRY

COIL A
COIL B
COIL C

S3
S2
S1
40 V POWER
+DRIVE ENABLE

(0405)
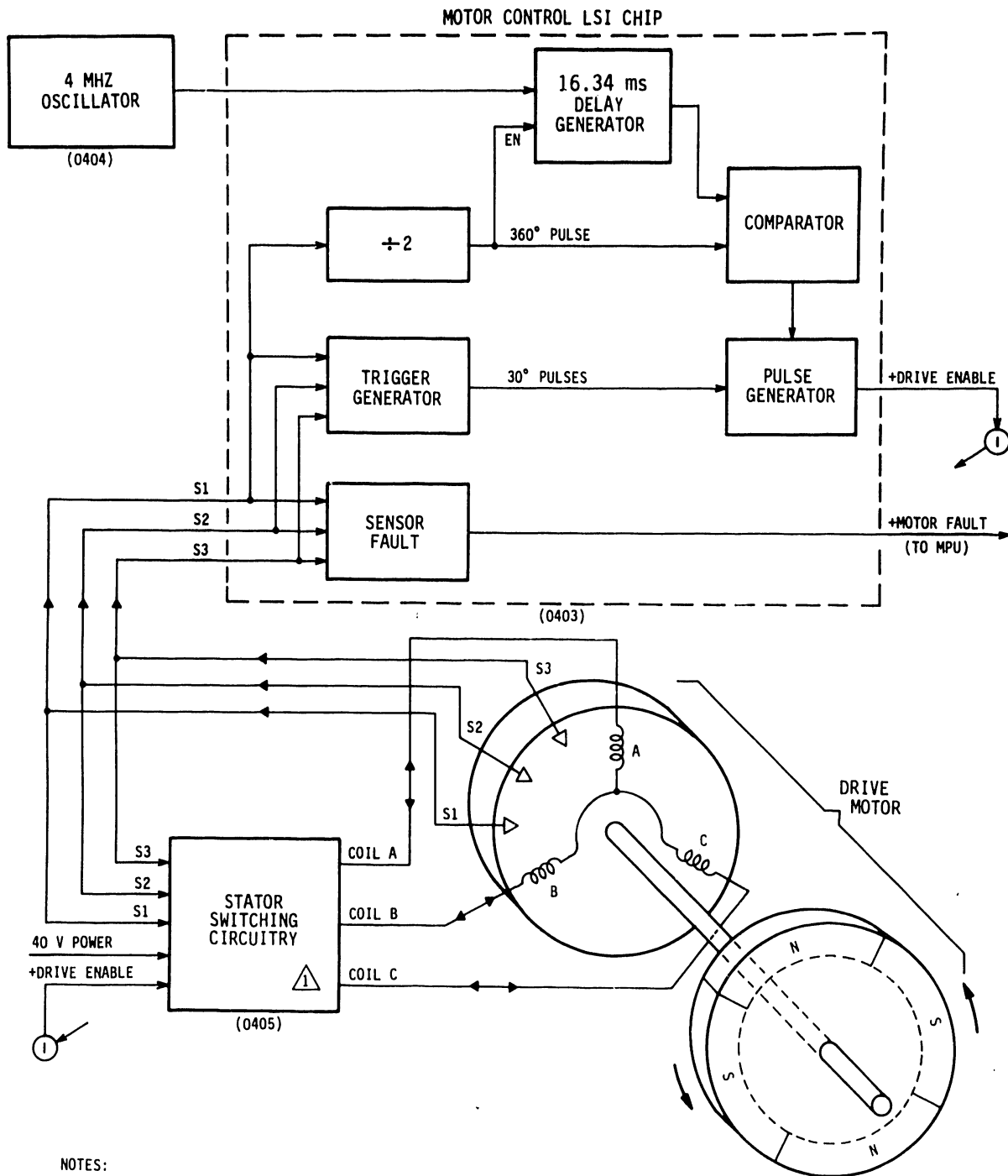
NOTES:

⚠ REFER TO SPEED CONTROL WAVEFORMS AND TIMING DIAGRAM FOR INPUT AND OUTPUT WAVEFORMS OF THIS CIRCUIT.

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speed. A comparator circuit outputs a pulse that is active from the end of the reference delay until the next 360° Pulse. The active time for the comparator output pulse determines the on-time of the +Drive Enable line during each 30° segment of motor rotation. Power is applied to the stator windings only when +Drive Enable is high. This condition is updated once per motor rotation, and the duty cycle of the motor is readjusted to keep the motor speed within its specified range.

Three status outputs are generated by the motor speed control and are used as follows:

- +Motor Fault -- indicates to the MPU that the drive motor has a bad magnetic sensor.

- -Speed OK -- indicates to the MPU that the drive motor speed is between 3564 and 3636 r/min and that no motor fault is present.

- -Disk Stopped -- indicates to the interlock circuitry that the last disk rotation exceeded two seconds.

Friction Motor Braking

The drive motor decelerates during the power off sequence under control of the friction brake. A transistor switch on the motor speed control board energizes the brake during drive motor operation to release the brake and allow the motor to turn. The brake remains energized as long as the -Enable Power Supply control line is low. When the motor is powered down, this line goes high, deenergizing the brake and allowing it to contact the rotor in the drive motor.

The motor speed control activates the -Disk Stopped line to indicate that braking is complete. This output to the interlock circuitry turns off the flasher circuit for the Ready indicator to show that power down is complete.

HEAD POSITIONING

General

Data is written on and read from the disk by the heads. The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by the actuator mechanism which is an integral part of the drive. The actuator is controlled by inputs received from the servo circuits (refer to the discussion on Seek Functions).

Actuator and Magnet Physical Description

The actuator (shown in figure 1-7) consists of the actuator housing, the carriage and voice coil assemblies, and the head-arm assemblies. The head-arm assemblies, with the heads mounted at their front, are mounted at the forward end, and the voice coil at the opposite end, of the carriage assembly. The carriage assembly fits within and is provided with horizontal movement into/out of the permanent magnet by bearings riding along a carriage track. During head positioning, the carriage rides the track towards or away from the magnet and over the disk surfaces.
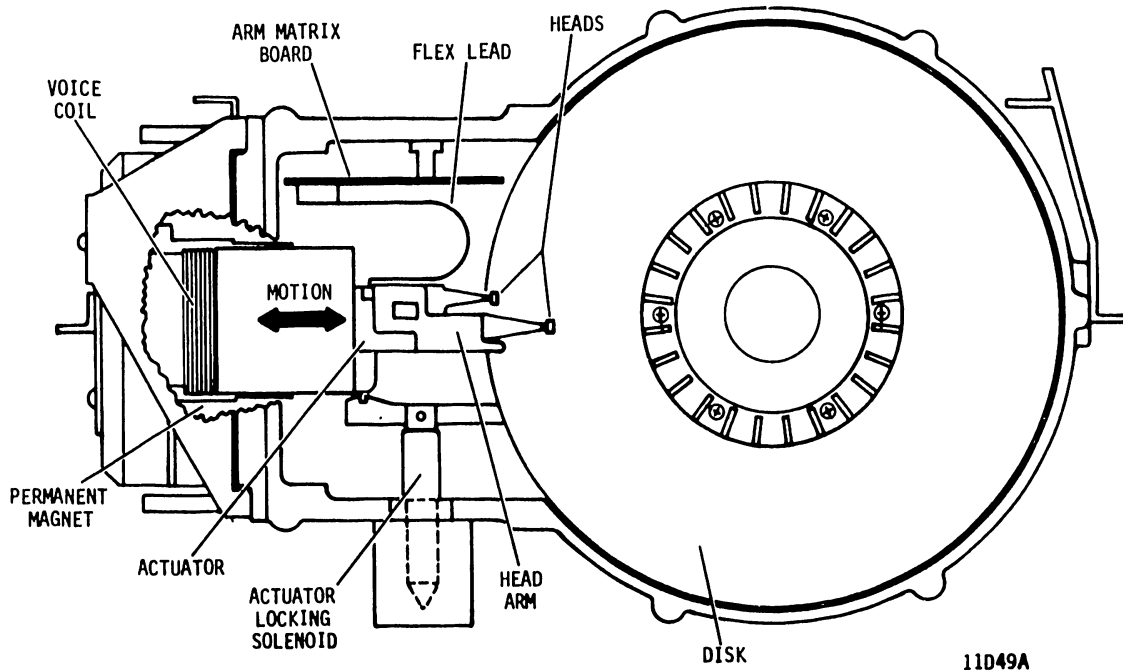
Figure 1-7. Actuator and Magnet Assembly

Whenever the drive is powered down, the actuator is latched in the unloaded position with the heads over the landing zone. The actuator remains locked until the next power up sequence when the MPU releases the actuator locking solenoid. The automatic actuator locking feature eliminates the need to manually lock the actuator when transporting the drive.

Actuator and Magnet Functional Description

The voice coil is mounted at the opposite end of the arm assembly and moves in and out of the magnet as the servo signals change. The magnet is mounted on the housing in a position which allows the voice coil to move as the field in the coil changes. This small in and out motion of the voice coil in the magnet provides the motion for the heads over the disk surface. The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the analog servo system and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil.

The current from the power amplifier causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnet. This reaction either draws the voice coil into the magnet or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEADS

General

The heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Up to four heads are attached to each supporting arm. The heads and arm together are called a head-arm assembly. The head-arm assemblies are attached to the front of the actuator assembly (figures 1-7 and 1-8).

The drive has 24 data heads and one servo head. The data (or read/write) heads are used to record data on and read data from the disk data surfaces. The servo head is used to read prerecorded data from the servo disk surface for use by the drive analog servo circuits.
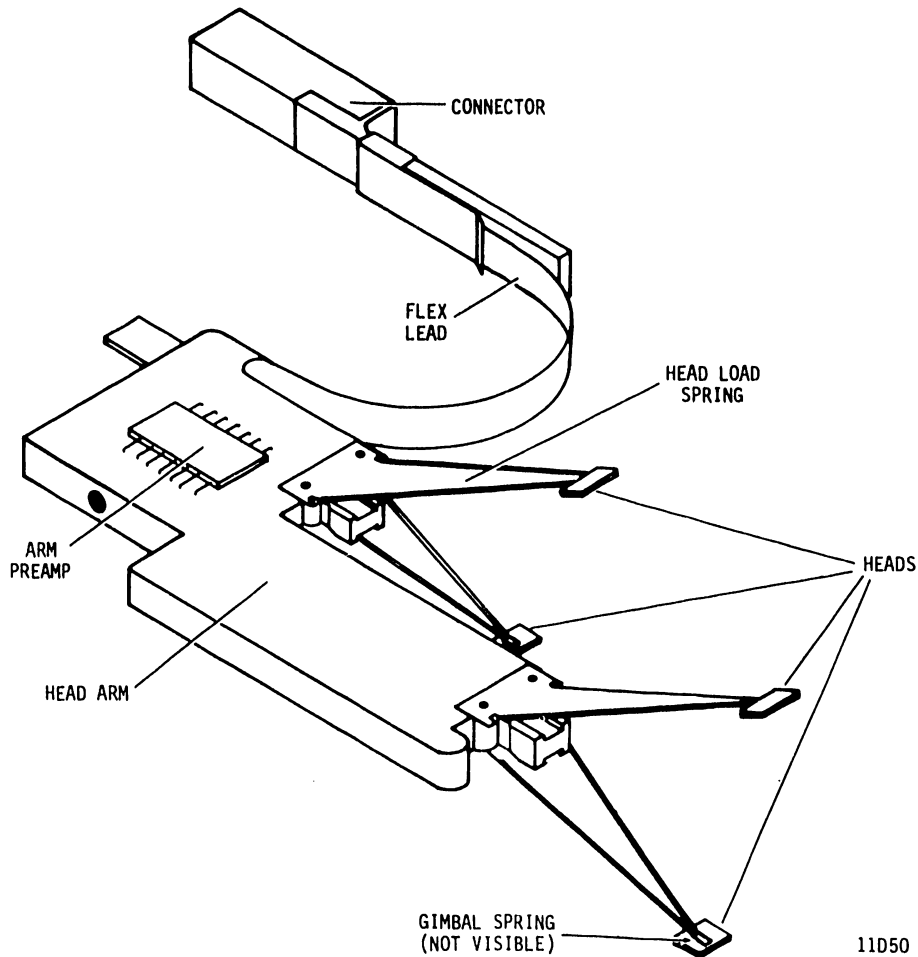
Figure 1-8. Data Heads

The following paragraphs describe the physical characteristics of the movable head-arm assemblies and how they function during head load and retract sequences. Further information about the heads is found in the discussions on seek and read/write functions.

Head-Arm Assembly

Each head-arm assembly consists of a rigid arm, supporting either two or four heads on load springs and gimbal springs (figure 1-8). The head-arm assemblies are mounted at the front of the actuator carriage and follow the in/out motion of the carriage created by the reaction of the voice coil magnetic

field to the field of the permanent magnet. The rigid arm by itself does not provide the action necessary for the heads to load or unload. The head load spring forces its associated head toward the disk surface; the gimbal spring allows the head free axial movement along its vertical and horizontal axes independent from the rigid arm.

Read/write information is transferred to and from the heads through cables connected to a preamp mounted on the arm. The preamps interface to the read/write circuitry via the Arm Matrix board, located inside the sealed module.

Head Loading

In the retract (non-operating) condition, the head load springs are forcing their respective heads against the disk surface in the landing zones. There are two landing zones on each data surface -- one for each head. At their extreme outward travel, the heads are located over their respective landing zones. When the system powers up, the program turns on the drive motor. When the drive motor is rotating the disks at acceptable speed, the heads move away from the disk surfaces and fly on the cushion of air created by disk rotation. At this point in the power on sequence, the actuator is unlocked and the heads are moved inward to track zero. Until the power off sequence is begun, the heads continue to fly on the cushion of air.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the forces of the head load spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

If the disk drops below speed, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the data areas and locked over the landing zone when the disk speed drops below a safe operating level.

AIR FLOW SYSTEM

The air flow system is divided into two parts, one for the drive unit and the other for the sealed module.

The drive air flow system (figure 1-9) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive air flow system is the fan that is mounted on the rear panel. The fan motor is driven from the -24 V power from the external power supply. The fan pulls ambient air through the input and primary filter of the front panel. The fan circulation travels over the electronics, cooling these assemblies before leaving the drive through the back panel. The system intake port is located on the front panel. This port is covered by the primary filter which keeps large particles from being drawn into the system.

The fan speed is monitored by a circuit on the I/O board. Pulses from the fan retrigger a one-shot, and the one-shot remains set as long as the fan speed is satisfactory. If the +Fan Fault line goes active, the MPU retracts the heads and powers down the drive motor. Similarly, the MPU checks the +Fan Fault line during a load operation and requires that the line is inactive before powering on the drive motor.

The air flow system for the module is a self-contained closed loop system (figure 1-10). The system consists of a fan, circulation filter, and breather filter. The fan blades are located at the top of the hub assembly, and the rotation of the spindle rotates these fan blades. The motion of the blades above the cut out pulls air through the circulation filter into the disk area.

If the pressure within the module becomes less than the surrounding atmosphere, makeup air enters through the breather filter to equalize the pressures. Likewise, if the module pressure exceeds atmospheric pressure, air leaves the module through the breather filter.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

The following discussion describes both the I/O cables and I/O signal processing.

AIR
EXHAUST

AIR
INTAKE
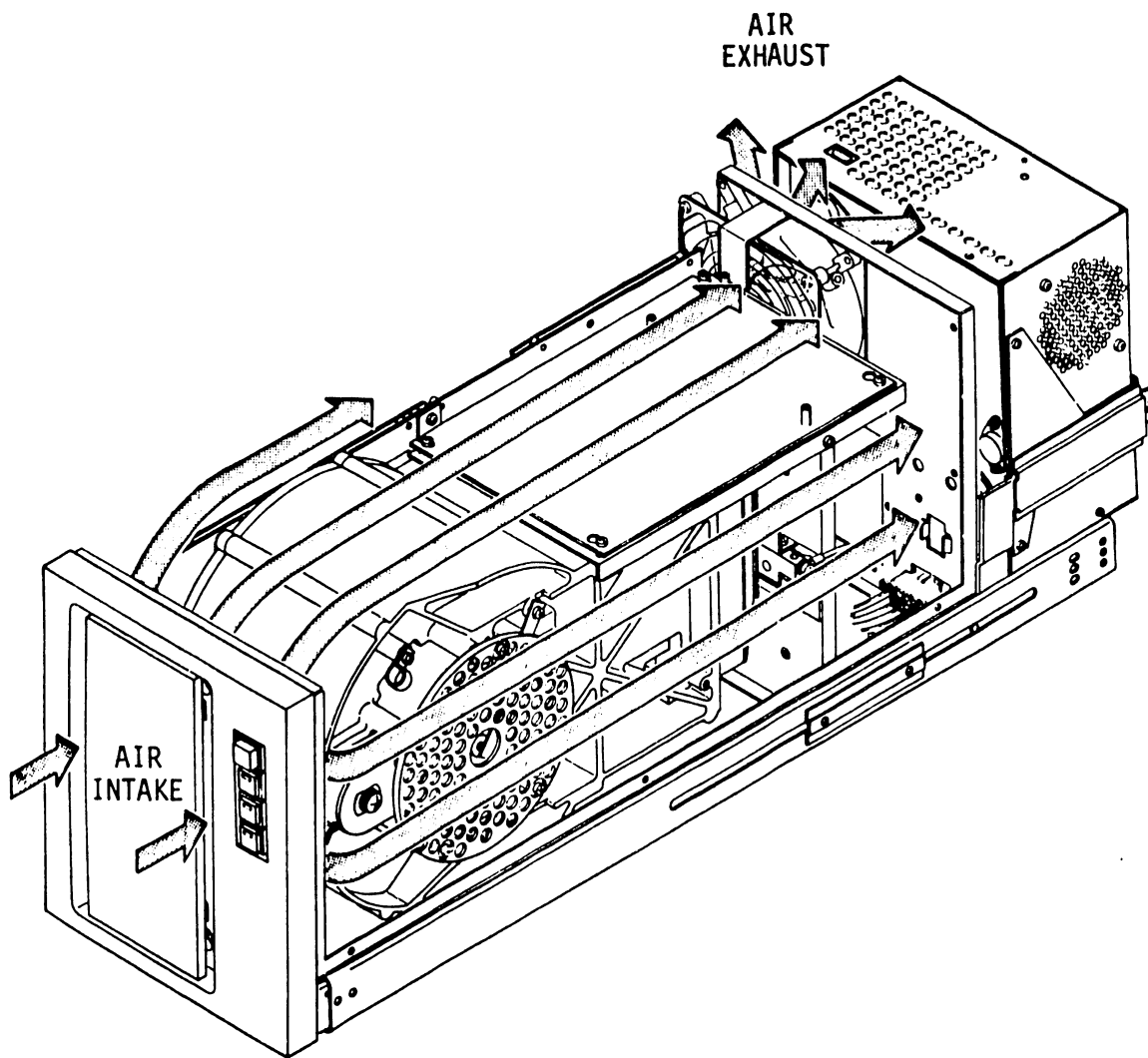
11D51

Figure 1-9. Drive Air Flow System

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CIRCULATION
FILTER
(ABSOLUTE)

ACTUATOR

MAGNET

INLET
MAKEUP
AIR FLOW

BREATHER FILTER
(ABSOLUTE)

HEADS

DRIVE MOTOR

FAN BLADE

DISKS

11D52A
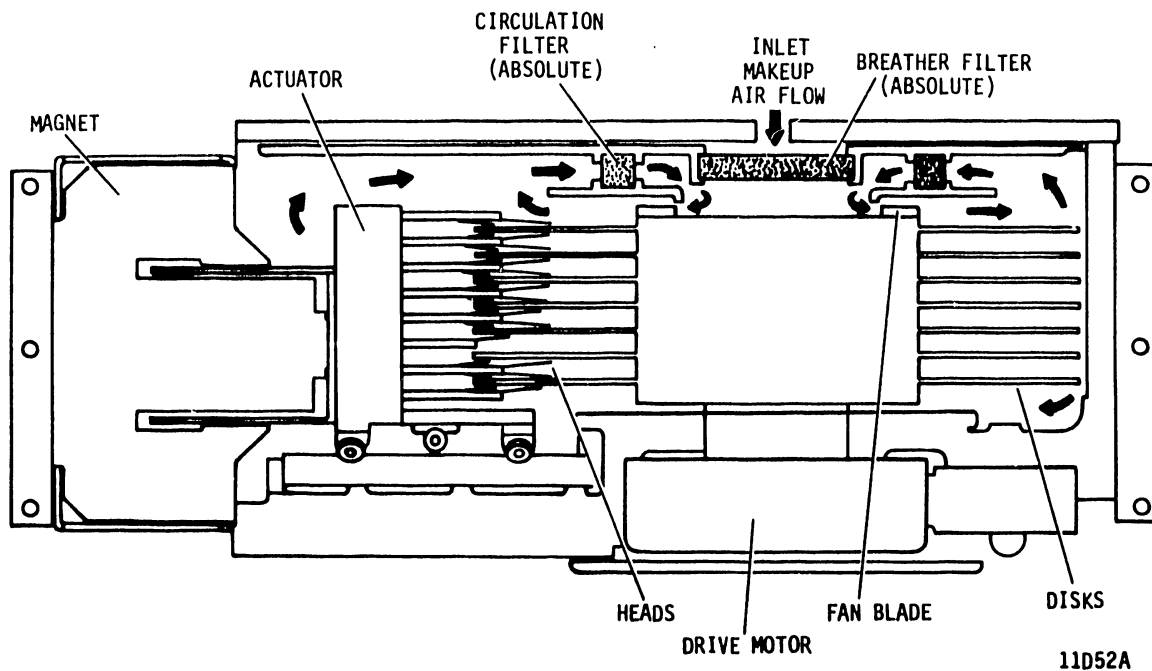
Figure 1-10. Module Component Placement and Air Flow

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller.

The B cable carries read/write data, clock, and status information between drive and controller. Figure 1-11 shows all lines (except those not used) in the A and B cables. The functions of each of these lines is explained in table 1-1.
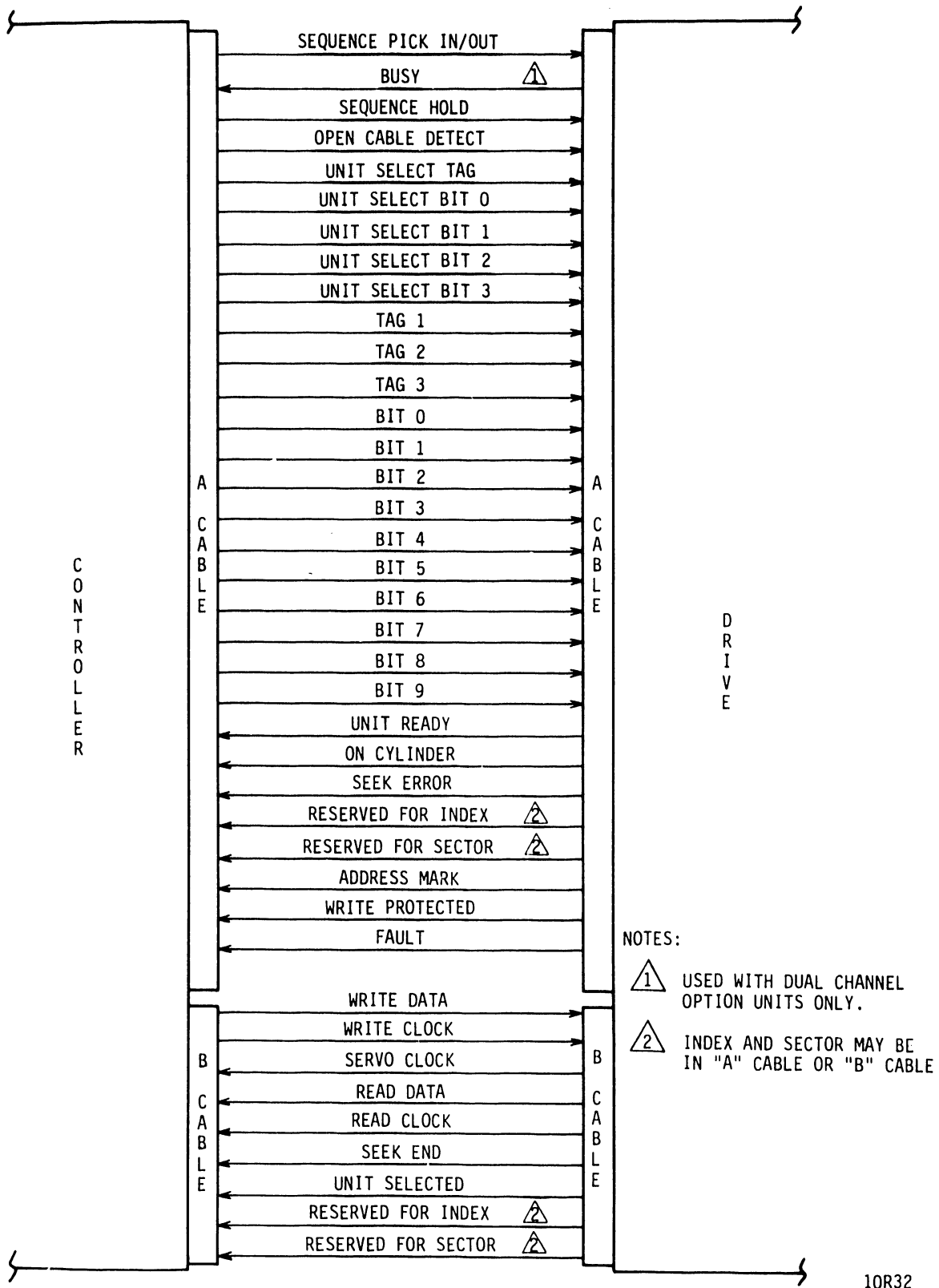
Figure 1-11.   Interface Lines

NOTES:

1. USED WITH DUAL CHANNEL OPTION UNITS ONLY.

2. INDEX AND SECTOR MAY BE IN "A" CABLE OR "B" CABLE

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TABLE 1-1.   INTERFACE LINES

Signal	Meaning
Function: Power Up Sequencing	
Sequence Pick	A ground from the controller on this line starts the power on cycle when the drive's LOCAL/REMOTE switch is in the REMOTE position, provided that the START switch has been pressed and that Sequence Hold is active from the controller. Sequence Pick triggers a delay circuit that delays the power on sequence for an interval based on the drive address.
Sequence Hold	A ground from the controller on this line holds the drives in a power on condition when the drive's LOCAL/REMOTE switch is in the REMOTE position, provided that the START switch is left in the Start position. Removing the ground from this line powers down all operating drives in the system.
Function: Controller Selecting Drive	
Unit Select Tag	This signal gates Unit Select lines into logical number compare circuit. Unit is selected after 600 ns (maximum) internal time lapse. Drive will not process commands until selected.
	When the Unit Select Tag is accompanied by the proper logical address and Bus Bit 9 active, this indicates a priority select status in dual channel systems. The drive is unconditionally selected and reserved by the channel issuing this command provided that this channel has not been disabled.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Unit Select Bits 0, 1, 2, and 3	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive determined by the logical address plug inserted in the operator panel. Drives can be numbered 0 through 7. Bit 3 must be inactive for a unit selection to occur.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. This line must be active before the drive will respond to any command from controller.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at drive receiver. If the A cable is disconnected or if controller power is lost, unit selection and/or controller commands are inhibited.

Function: Drive Indicates Operational Status	
Unit Ready	Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the Control board.

TABLE 1-1.   INTERFACE LINES (Contd)

Signal	Meaning
Busy	Used only in dual channel drives, this signal is generated when a controller attempts to select a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by a jumper on the Control board, by a switch on the operator panel, by a fault condition, or by a loss of motor speed. Attempting to write while the write protect mode is active results in a fault condition.
On Cylinder	This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
Seek End	This signal indicates either an on cylinder status or seek error status resulting from a seek operation that has terminated.
Seek Error	This signal indicates that the drive was unable to complete a seek within 250 ms, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyond cylinder 710.

The seek error can be cleared by an RTZ command or by a power up operation. |

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Fault	When this line is active, it indicates that one or more of the following faults exist: ● First Seek fault ● Head Select fault ● DC voltage fault ● Write fault ● Write or read attempted while off cylinder ● Write gate during a read operation
Address Mark	When an address mark has been found, this line goes high.

Function: Controller Sends Commands to Drive	
Bits 0 through 9 (Bus Lines)	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Tag 1 (Cylinder Select)	This tag line gates the data on the bus lines to the drive Cylinder Address register. The bus bits have the significance listed below. Bus bits 0-9, with the value shown below, encode the cylinder address for the seek operation. Cylinder addresses above 710 are illegal and will encode a seek error.

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TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
	Bus Bit **Function**
	0 Cylinder Address 2^0
	1 Cylinder Address 2^1
	2 Cylinder Address 2^2
	3 Cylinder Address 2^3
	4 Cylinder Address 2^4
	5 Cylinder Address 2^5
	6 Cylinder Address 2^6
	7 Cylinder Address 2^7
	8 Cylinder Address 2^8
	9 Cylinder Address 2^9
Tag 2 (Head Select)	This tag line gates the data on the bus lines to the drive Head Address register. The bus bits have the significance listed below.
	Bus Bit **Function**
	0 Head Address 2^0
	1 Head Address 2^1
	2 Head Address 2^2
	3 Head Address 2^3
	4 Head Address 2^4
Tag 3 (Control Select)	This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the bus lines is active. The significance of the bus bits is as follows:

Table Continued on Next Page

TABLE 1-1.   INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	<table><tr><td>Bus Bit</td><td>Name</td><td>Function Performed</td></tr><tr><td>0</td><td>Write Gate</td><td>Enables write driver. Not accepted if there is a seek error or fault status.</td></tr><tr><td>1</td><td>Read Gate</td><td>Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status.</td></tr><tr><td>2</td><td>Servo Offset Plus</td><td>Offsets the positioner 75 microinches toward the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms.</td></tr><tr><td>3</td><td>Servo Offset Minus</td><td>Offsets the positioner 75 microinches away from the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms.</td></tr><tr><td>4</td><td>Fault Clear</td><td>A pulse sent to the drive that clears the Fault flip-flop provided that the fault condition no longer exists.</td></tr></table>

Table Continued on Next Page

83324770 A

TABLE 1-1.   INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	**Bus** **Bit** **Name** **Function Performed** 5 Address Mark Enable — When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read gate, an address mark search is initiated. 6 RTZ — A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error flip-flop. 7 Data Strobe Early — Enables the read comparator to strobe the data at a time earlier than nominal. 8 Data Strobe Late — Enables the read comparator to strobe the data at a time later than nominal. 9 Release — Used with dual channel option only, it clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion.)

Table Continued on Next Page

TABLE 1-1.   INTERFACE LINES (Contd)

Signal	Meaning
Functions: Read, Write, and Clocks	
Read Data	This line transmits data recovered from the disk. This data is transmitted in NRZ form to the controller.
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell and is transmitted continuously.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface.
Write Clock	This clock is the Servo Clock etransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Enable.
Servo Clock	Servo Clock is a phase-locked signal generated from the servo track tribits. The Servo Clock frequency is 14.52 MHz in 515 MB drives or 9.67 MHz in 340 MB drives. Servo Clock is continuously transmitted.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except local power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information concerning the operation back to the controller via the drivers. Figure 1-12 shows the basic logic involved in the routing of the I/O signals.

Certain I/O signals cannot be transmitted or received unless the drive is selected. These signals include the tag and bus bit signals from the controller and the status bits to the controller.

WRITE CLOCK → RCVR

WRITE DATA → RCVR

READ/WRITE

TAG 2 (HD SEL) → & RCVR → HEAD SELECTION

WRITE CIRCUITS

READ CIRCUITS

BUS BIT 0 → & RCVR
BUS BIT 1 → & RCVR
BUS BIT 2 → & RCVR
BUS BIT 3 → & RCVR
BUS BIT 4 → & RCVR
BUS BIT 5 → & RCVR
BUS BIT 6 → & RCVR
BUS BIT 7 → & RCVR
BUS BIT 8 → & RCVR
BUS BIT 9 → & RCVR

BITS 0-4

FUNCTION DECODE

BITS 0-9

WRITE GATE
ADDRESS   MARK ENABLE
READ GATE
DATA STROBE EARLY
DATA STROBE LATE
CLEAR FAULT
RELEASE   /2\
SERVO OFFSET PLUS
SERVO OFFSET MINUS
RTZ

WRITE PROTECT CIRCUITS

FAULT DETECTION

BITS 0-9 → MPU

SEEK CIRCUITS

TAG 3(CONTROL SEL) → & RCVR

TAG 1 (CYL SEL) → & RCVR

POWER SEQUENCE DELAY

SERVO SURFACE DECODING

INDEX AND SECTOR COUNTER

SEQUENCE PICK
SEQUENCE HOLD

UNIT SEL BIT 0 → RCVR
UNIT SEL BIT 1 → RCVR
UNIT SEL BIT 2 → RCVR
UNIT SEL BIT 3 → RCVR

UNIT SELECTION → SELECT COMPARE → TO DRIVERS /3\

UNIT SEL TAG → RCVR

OPEN CABLE DETECT → RCVR

/1\

NOTES:

/1\ DUAL CHANNEL DRIVES HAVE A SET OF DRIVERS AND RECEIVERS FOR EACH CONTROLLER

/2\ APPLICABLE ONLY TO DUAL CHANNEL UNITS

/3\ SEE SHEET 2 FOR DRIVE TO CONTROLLER SIGNAL PROCESSING

11D53-1

Figure 1-12.   I/O Signal Processing (Sheet 1 of 2)
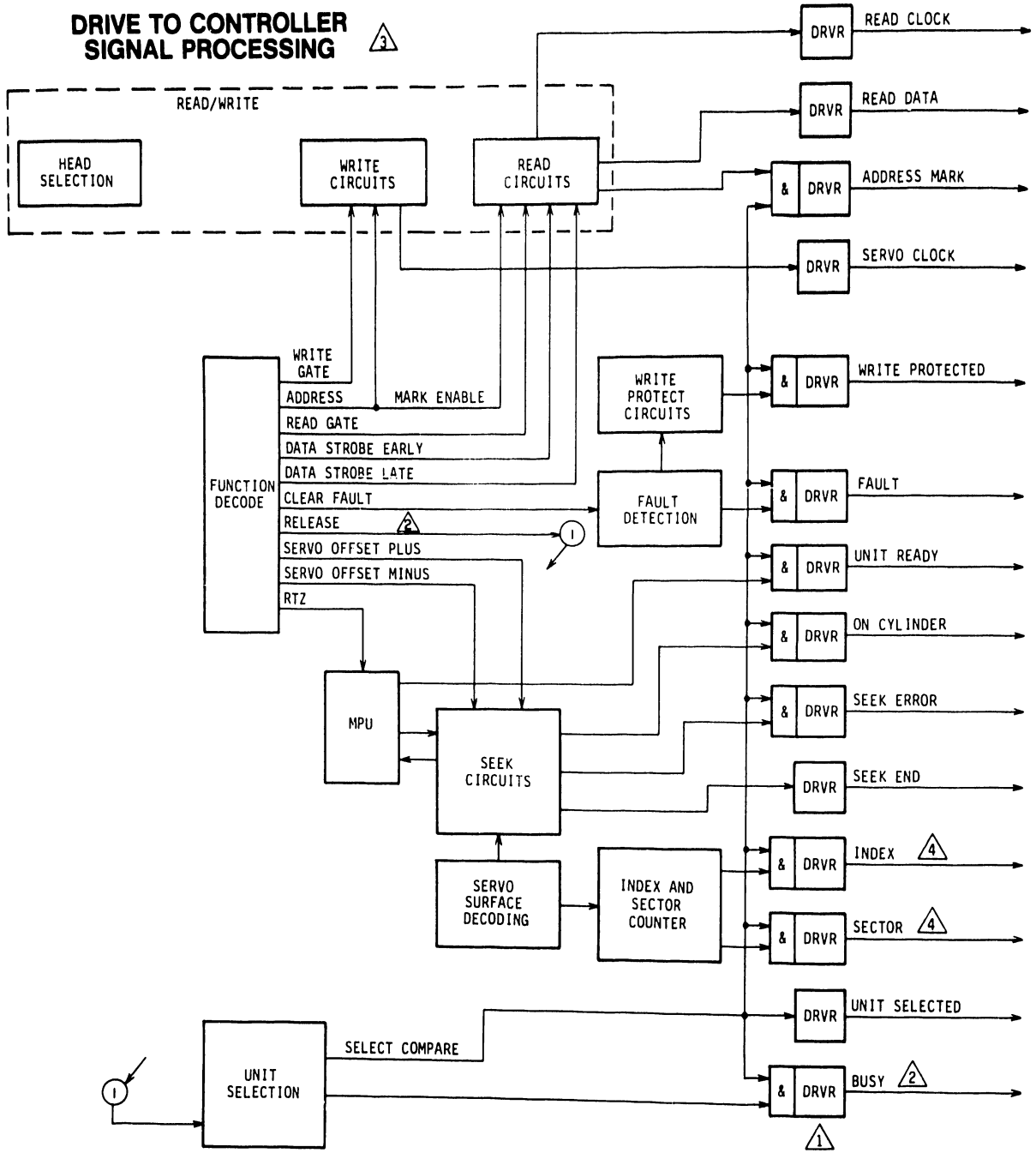
DRIVE TO CONTROLLER SIGNAL PROCESSING △3

NOTES:

△1 DUAL CHANNEL DRIVES HAVE A SET OF DRIVERS AND
RECEIVERS FOR EACH CONTROLLER

△2 APPLICABLE ONLY TO DUAL CHANNEL UNITS

△3 SEE SHEET 1 FOR CONTROLLER TO DRIVE SIGNAL PROCESSING

△4 INDEX AND SECTOR SIGNALS ARE SENT CONTINUOUSLY WHEN
INDEX/SECTOR JUMPER PLUG IS IN "B" POSITION

11D53-2

Figure 1-12.   I/O Signal Processing (Sheet 2)

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All commands (except unit select) are sent to the drive via the tag and bus bit lines. The tag lines define the basic operation to be performed and the bus bits further define and modify the basic operation. Table 1-1 explains the functions of all tag and bus lines.

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 1-13) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drive's logical address is determined by the logical address plug which fits into the operator panel. Depending on the plug used, this address can be any number from 0 to 7. If no plug is used, the number is 7.

If the address sent by the controller is the same as that of the drive and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power), the drive enables its Select Compare signal.
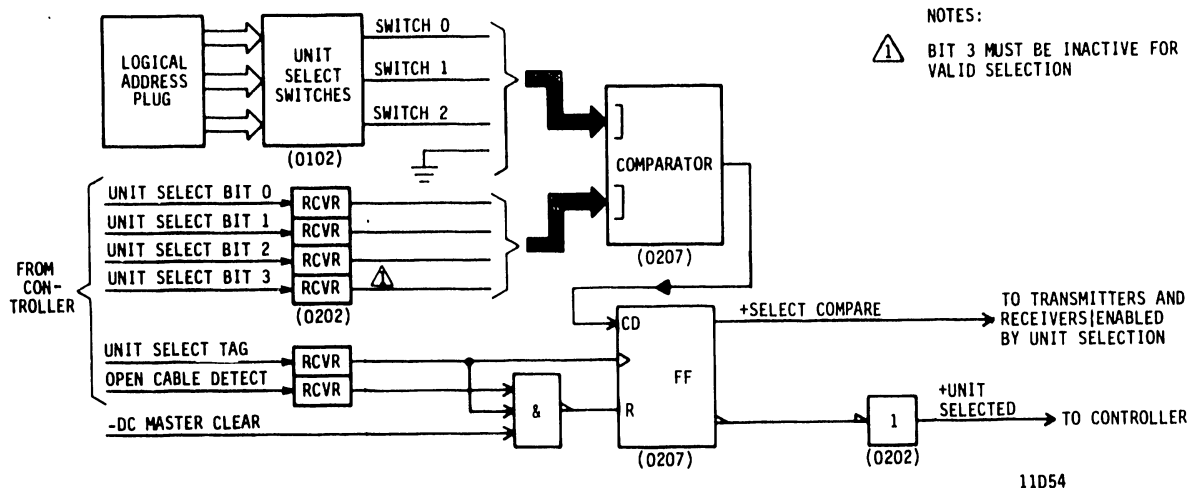
Figure 1-13. Unit Select Logic (Single Channel)

The Select Compare signal enables the receivers and drivers to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.

- Reserve – Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.

- Release – Releases drive from reserved condition.

- Priority Select – Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.

- Maintenance Disable – Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 1-14 shows the select logic associated with channel I selection and table 1-2 describes the major elements on this figure. Figure 1-15 is a flowchart of the dual channel unit select and reserve functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.

- Drive is not selected but is reserved by other controller.

- Channel to drive attempting selection has been disabled by either a priority or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address plug. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 1-13).
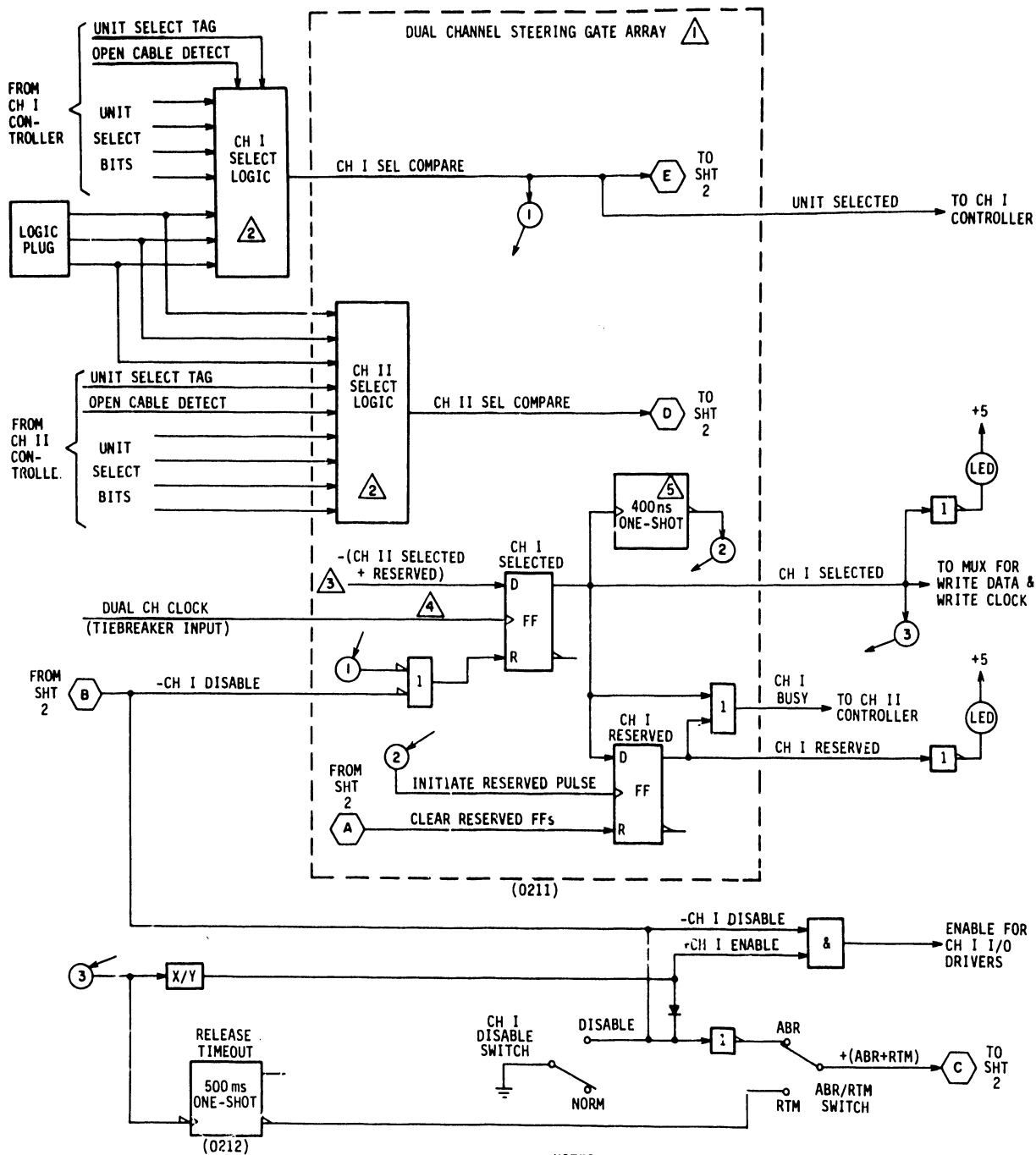
NOTES:

△1 GATE ARRAY CIRCUITS ARE SHOWN ON SHEET 2 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.

△2 FOR DETAILS, SEE DIAGRAM FOR SINGLE CHANNEL UNIT SELECTION.

△3 SIGNAL DERIVED FROM CH II SELECTED FF AND CH II RESERVED FF.

△4 INVERTED TIEBREAKER SIGNAL CLOCKS CH II SELECTED FF.

△5 FOR 340 MB DRIVES, ONE-SHOT TIMES OUT IN 300 ns.

11D55-1

Figure 1-14. Channel I Dual Channel Logic (Sheet 1 of 2)
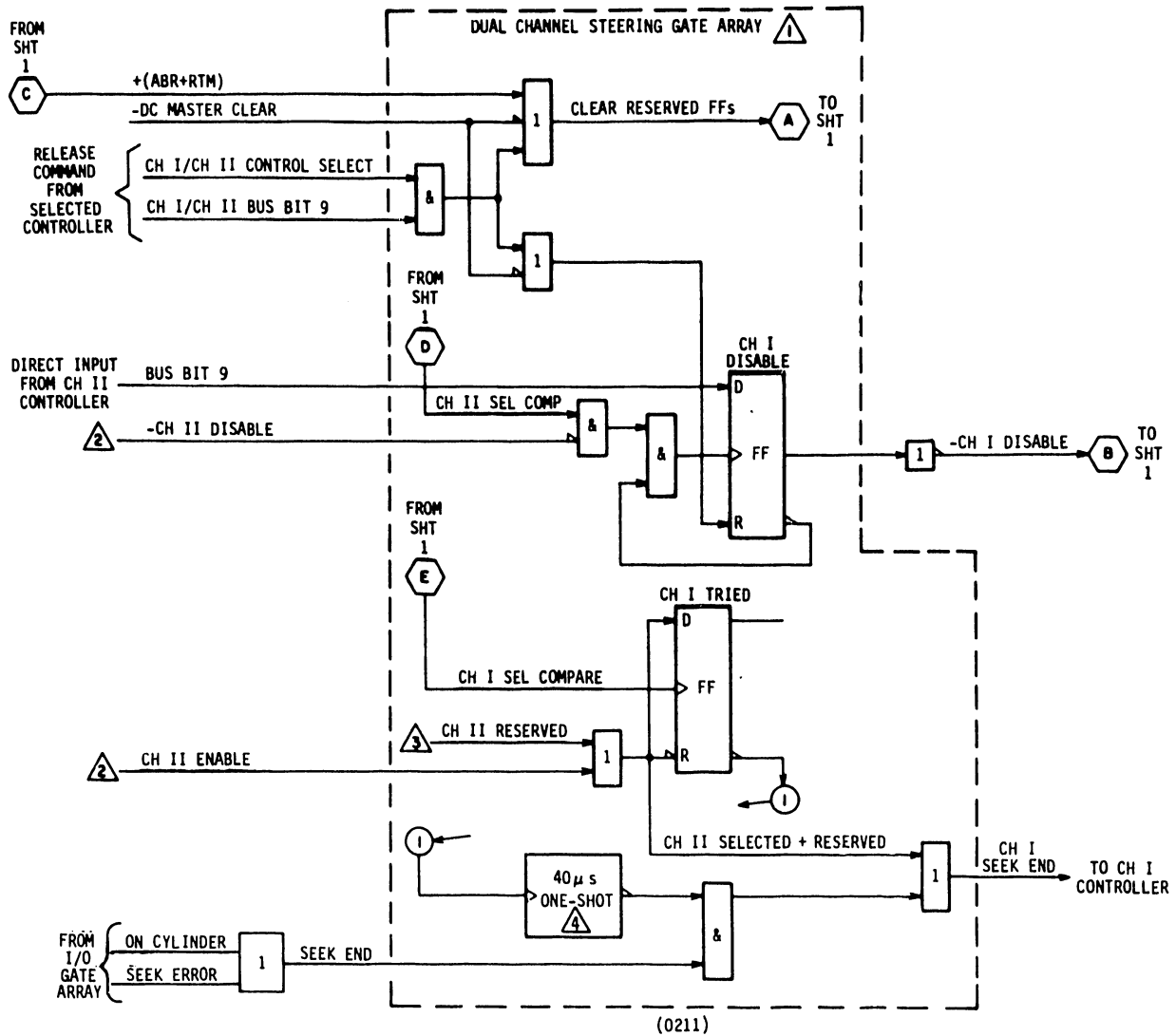
NOTES:

△1 GATE ARRAY CIRCUITS ARE SHOWN SHEET 1
ALSO. FOR EACH CHANNEL I FF SHOWN,
THERE IS A COMPARABLE CHANNEL II FF.

△2 SIGNALS DERIVED FROM CHANNEL II OUTPUTS
OF GATE ARRAY.

△3 SIGNAL DERIVED FROM CH II RESERVED FF.

△4 FOR 340 MB DRIVES, ONE-SHOT TIMES OUT IN 30 μS.

11D55-2

Figure 1-14.   Channel I Dual Channel Logic (Sheet 2)

CH I SENDS UNIT SELECT TAG AND DRIVE ADDRESS

ADDRESS SAME AS DRIVES — NO / YES

SET CH I SELECT COMPARE FF

△1 **DRIVE DOES NOT RESPOND. CH I MUST WAIT UNTIL CH II RELEASES** — YES — **CH I DISABLED VIA ABR SELECT** — NO

ENABLE BUSY TO CH I CONTROLLER CH I CAN ISSUE PRIORITY SELECT OR WAIT FOR CH II RELEASE — YES — **CH II HAS DRIVE SELECTED OR RESERVED** — NO

ENABLE UNIT SELECTED STATUS TO CH I CONTROLLER

CH II PREVENTED FROM SELECTING OR RESERVING DRIVE

△2 **TRIGGER 500 ms RTM TIMEOUT (ONE SHOT)**

SET CH I TRIED FF

SET CH I SELECTED FF AND LIGHT LED

ENABLE CH I RECEIVERS/TRANSMITTERS SO DRIVE WILL RESPOND TO CH I CONTROLLER COMMANDS

ENCODE BUSY SIGNAL TO CH II CONTROLLER

TRIGGER RESERVE ONE-SHOT (400 ns TIME OUT IN 515 MB DRIVES OR 300 ns IN 340 MB DRIVES)

WHEN CH II DESELECTS, SEEK END TO CH I GOES LOW FOR 40 µs (IN 515 MB DRIVES) OR 30 µs (IN 340 MB DRIVES)

TO SHT 2 — A

NOTES: △1 ABR POSITION PREVENTS RESET OF RESERVED FF'S EXCEPT BY PRIORITY SELECT. EITHER CHANNEL DISABLE SWITCH IN DISABLE POSITION HOLDS RESERVE FF'S IN RESET CONDITION AND PREVENTS SELECTION OF THE DRIVE BY THE ASSOCIATED CONTROLLER UNTIL PLACED IN NORM.

△2 TIMEOUT STARTS WHEN CHANNEL SELECTED FF CLEARS.

11D188-1A

Figure 1-15. Dual Channel Selection Flowchart (Sheet 1 of 2)

83324770 B

FROM
SHT 1

A

SET CH I
RESERVED FF
AND LIGHT LED

CH I
COMPLETED
OPERATIONS AND
DROPPED UNIT
SELECT — NO

YES

RESET CH I
SELECT
COMPARE FF

RESET CH I
SELECTED FF
AND EXTINGUISH
LED

DISABLE UNIT
SELECTED SIGNAL
TO CH I
CONTROLLER

CH I ENABLE SIG-
NAL DROPPED TO
DISABLE CH I
RECEIVERS AND
TRANSMITTERS

DID
CH I
RELEASE DRIVE
VIA TAG 3 AND
BUS BIT 9 — NO

RESET OF CH I
SELECTED FF
ALLOWS 500 ms
RELEASE ONE-SHOT
TO TIME OUT

YES

ABR/RTM
SWITCH ON
RTM — NO

CH I RESERVE FF
REMAINS SET

YES

1

DRIVE RESERVED
UNTIL CH I
RELEASES OR CH II
PRIORITY SELECTS

1

CLEAR CH I
RESERVE FF
AND EXTINGUISH
LED

CH II
TRIED FF
SET

DRIVE AVAILABLE
FOR SELECT/RESERVE
BY EITHER
CHANNEL

YES

CLEAR CH II TRIED
FF. SEEK END TO
CH II CONTROLLER
GOES LOW FOR 40 µs
(IN 515 MB DRIVES)
OR FOR 30 µs
(IN 340 MB DRIVES)

110188-2A

Figure 1-15.   Dual Channel Selection Flowchart (Sheet 2)

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One Shot	Times out 500 ms after drive is deselected. If drive is in RTM mode, the reserved FF is cleared when timeout occurs.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Disable Switch	Disables channel I whenever it is set to DISABLE position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I** Selected FF	Sets during select and reserve sequence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).

Table Continued on Next Page

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Initiate Reserved Pulse	Generates a pulse whenever Select Compare signal goes true. The pulse length is 400 ns for 515 MB drives or 300 ns for 340 MB drives. This pulse creates a delayed clock for the Channel I and Channel II Reserve FFs.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one shot.
Select Tried One Shot	Generates a pulse whenever either Tried FF clears. The pulse length is 40 microseconds for 515 MB drives or 30 microseconds for 340 MB drives. This pulse is sent to controller (associated with the Channel Tried FF that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning channel I and shown in figure 1-14.

**The Channel Selected FF's are alternately clocked by the Dual Channel Clock signal to prevent simultaneous selection.

The Select Compare signal causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF. With these FFs set, the drive sends Unit Selected to the channel I controller indicating that it is ready to accept further commands.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag or changes the logical address to another drive. At this time, the drive's Channel I Selected FF clears, thus disabling the drive drivers and receivers for that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also Clear. This is cleared by either a release or priority select function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 40 microseconds (30 microseconds for 340 MB drives). This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

● Timeout release pulse

● Release command

The timeout release pulse is capable of releasing the drive from only the reserved condition. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets) and times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one shot has any effect on the Release FF depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Maintenance Disable Function

It is also possible to disable either channel by setting the Disable switch for that channel (refer to figure 1-14) to the DISABLE position.

DRIVE SERVO SYSTEM

The drive writes data on and reads data from the disk data recording areas under the directions of the controller. These operations cannot be done randomly, however, for when the controller wishes to retrieve data, it must be able to find the exact location where that data has been stored. This problem is resolved by mapping the disks into discrete sections called "Tracks" which are narrow concentric bands that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called "Sectors".

After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed. The operation of positioning the heads over the desired track is called a Seek operation. The drive servo system under the direction of the microprocessor unit (MPU) performs the Seek operation to position the heads by using information read from the servo surface by the servo head.

The data recording areas of each of the disks (2 areas on each of 12 disk surfaces) are divided into 711 tracks, and these are assigned sequential number addresses from 0, which is located on the outer edge of the recording area, through 710 which is located on the inner edge of the data recording area closest to the hub. Since there are 24 data recording areas, each with 711 tracks with addresses 0 through 710, the controller must select 1 of 24 possible tracks with the same cylinder address number. This further selection is done by assigning numbers to the data recording areas (and the heads associated with the data areas) from 0 through 23.

Once a particular cylinder is selected, the controller then further narrows down location selection by addressing one of 24 heads located at the selected cylinder. Each track is subdivided into equal segments called "Sectors". This division is accomplished by the setting of a group of switches called Sector switches (see the discussion called Sector Detection). When the controller has selected the unit, the track, and the head, then it waits for the particular sector(s) where it wishes to write (store) or retrieve (read) data. Another option for locating an area on a track to be operated upon is by writing an Address Mark at a specific location on the track, and then looking for the mark at the beginning of a read operation.

When the controller commands the drive to go to a cylinder/head/sector where it wishes to perform a read or write operation, the drive servo system under the direction of the MPU performs the positioning (Seek) operation. The MPU program uses information read from the servo surface by the servo head to do the Seek operation. The following discussion will describe servo surface decoding and then describe seek functions.

SERVO SURFACE DECODING

GENERAL

The servo surface is a prerecorded disk surface in the module that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the servo head across the servo surface correspond exactly to movements of the data heads across the data surfaces.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal

- Rotational position of the disks, indicated by the Index signal

- Exact speed of the disks, indicated by the clock signal from the servo PLO.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

- Tribit Recording Scheme

- Servo Surface Format

- Tribit Decoder Circuit Operation

TRIBIT RECORDING SCHEME

Servo information consists of tribit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track. Each track has eighty segments, each consisting of a special nine-byte resync pattern followed by 327 normal servo bytes.

Unless the servo head is positioned directly over one servo track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 1-16 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

In figure 1-16, two normal bytes are followed by a resync byte. Each normal byte contains three bits -- a sync bit and two position bits. The sync bits have negative polarity and are recorded on all tracks. The position bits have positive polarity and are staggered from track to track so that they make separate contributions to the composite servo signal.

The resync byte shown in figure 1-16 has a missing sync bit and one position bit (half the number of position bits in the normal byte). Adjacent tracks have coinciding sync bits as well as staggered position bits.

SERVO SIGNAL RECORDED IN TRACK "A" ON SERVO DISK

SERVO SIGNAL RECORDED IN TRACK "B" ON SERVO DISK

POSITION BITS

COMPOSITE SERVO SIGNAL PICKED UP WHEN SERVO HEAD IS ABOVE THE CENTERLINE "C" BETWEEN TRACKS "A" AND "B"

NORMAL BYTE   NORMAL BYTE   FIRST RESYNC BYTE   MISSING SYNC BIT

SYNC BIT

PART OF SERVO SURFACE
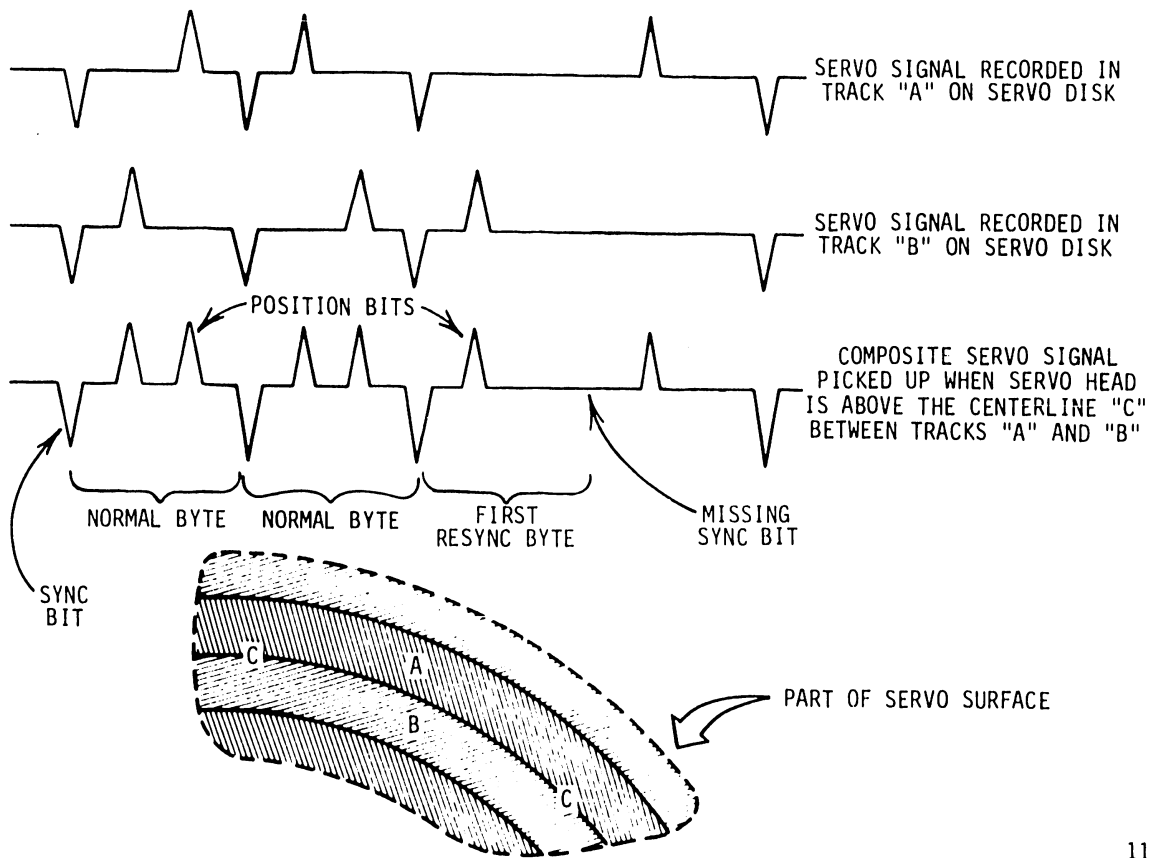
11D56

Figure 1-16. Tribit Pattern

The special nine-byte resync patterns appearing 80 times per disk rotation contain different combinations of resync bytes and normal bytes, depending on what the pattern designates on the disk surface. The different patterns and their relation to the disk format are explained under the next topic. Each nine-byte pattern is followed by 327 normal bytes. Thus, for each disk rotation, the servo head detects 80 X 336 or 26 880 servo bytes.

The relative amplitude of the position bits within each servo byte is used to indicate the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent tribit signals. The amplitude of each position bit within a servo byte is proportional to the read coil overlap of the recorded servo tracks. With the head centered, each adjacent servo track contributes equal position bit amplitudes. As the head moves away from its centered position toward one servo track, the track being approached makes a greater contribution to the detected position bits than the one being left. The tribit demodulator converts this variation into the position signal used by the seek circuitry (see Position Demodulation).

Figure 1-17 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two servo tracks, and the position bits have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the position bits have different amplitudes.

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The servo surface format divides the disk surfaces into four zones: an 711-track data zone, two guardbands, and a buffer zone. The guardbands indicate areas of the disk that cannot be used for recording of data, and servo encoding extends beyond the normal limits of head positioning. The outer guardband consists of 10 tracks on the outer portion of the disk. The inner guardband consists of 250 tracks on the inner portion of the disk. The buffer zone consists of two tracks located between the outer guard band and the data zone. In addition, all four zones contain an encoded "reference line" which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.
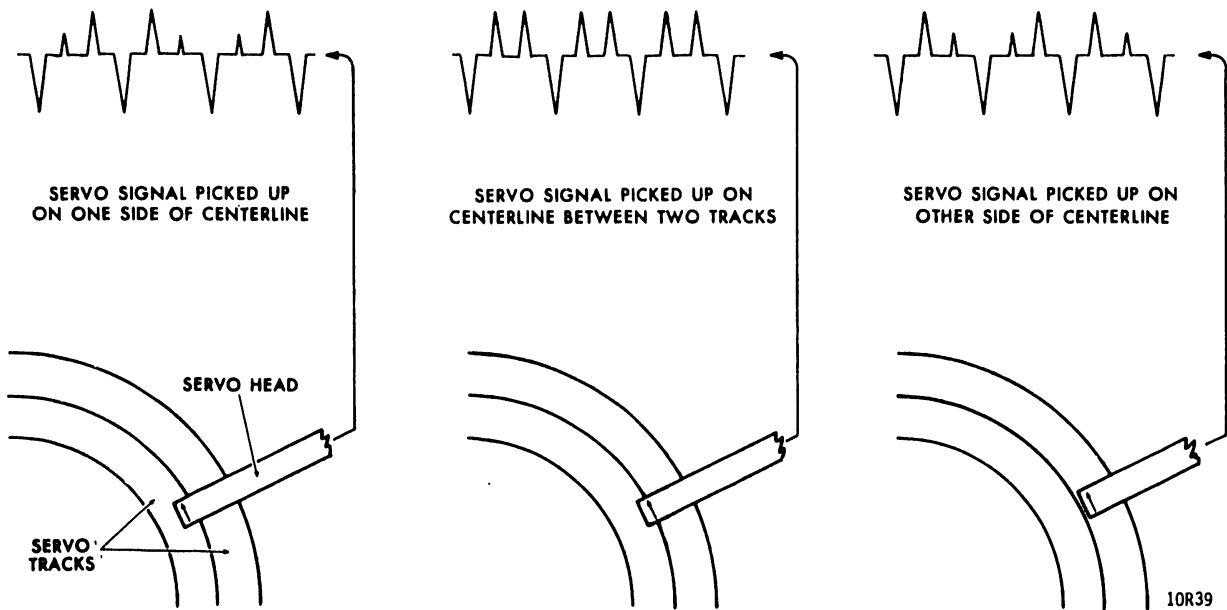
Figure 1-17. Tribit Signal Variations

Figure 1-18 shows the positioning of heads on the module disk surfaces and explains, in the exploded portion of the drawing, how formatting information is encoded on the disk. As described in the Tribit Recording Scheme discussion, nine-byte resync patterns are used as format indicators. Each of the nine bytes is either a resync byte (labelled "1") or a normal byte (labelled "0"). With the two bytes labelled in this manner, each nine-byte code can be designated as a nine-bit pattern number. The Index pattern (101000101) marks the logical beginning of each servo track. The remaining 79 coded patterns spaced around each servo track depend on the zone for that track. The outer guardband is encoded with pattern 100010101, the data zone and buffer zone with pattern 100010001, and the inner guardband with pattern 101010001.

Refer to the Index and Guardband Decoding discussion for a description of the circuitry that performs this decoding.

DATA HEADS

DATA TRACKS | DATA TRACKS
DATA TRACKS | DATA TRACKS

DATA HEADS

DATA TRACKS | DATA TRACKS
DATA TRACKS | DATA TRACKS

DATA HEADS

DATA TRACKS | DATA TRACKS
DATA TRACKS | DATA TRACKS

DATA HEADS

ACTUATOR

DATA TRACKS | DATA TRACKS
DATA TRACKS | DATA TRACKS

DATA HEADS

DATA TRACKS | DATA TRACKS
GB | SERVO TRACKS | GB

SERVO HEAD   (S)

INNER GUARD BAND:
250 TRACKS

SERVO ZONE:
711 TRACKS

OUTER GUARD BAND:
10 TRACKS

UNUSED SURFACE
DATA TRACKS | DATA TRACKS

DATA HEADS

DATA TRACKS | DATA TRACKS
DATA TRACKS | DATA TRACKS

DATA HEADS

HUB

-SPINDLE-

A

NINE-BYTE RESYNC PATTERNS:

x = INDEX - - CODE 101000101

d = DATA ZONE - - CODE 100010001

i = INNER GUARD BAND - - CODE 101010001

o = OUTER GUARD BAND - -
CODE 100010101 WITH
2-TRACK BUFFER ZONE
(CODE 100010001) ADJACENT
TO DATA ZONE

SHADED AREAS [▒▒▒] BETWEEN RESYNC
PATTERNS SHOW TRACK SEGMENTS WHERE
327 NORMAL SERVO BYTES ARE RECORDED

—A—
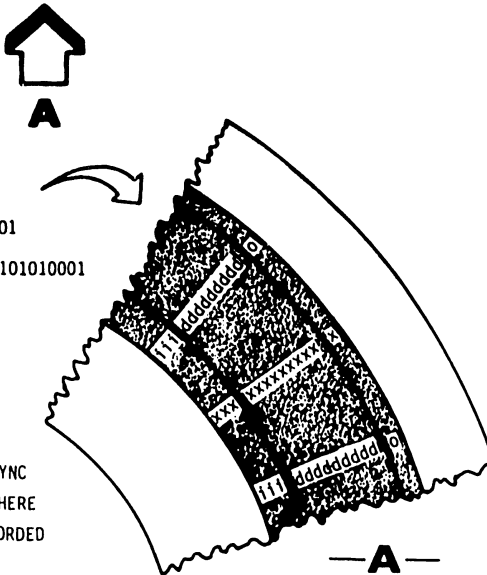
11D57

Figure 1-18.   Servo Disk Format

TRIBIT DECODER CIRCUIT OPERATION

General

Operation of the tribit decoder circuitry is discussed first in
terms of its relation to other systems within the drive. This
is followed by explanations of the individual functions per-
formed by the decoder.

System Overview

Decoding the information present in the servo signal is essen-
tial for other functional areas of drive operation. Figure
1-19 is a functional block diagram showing signal flow between
the tribit decoder and these other functional areas.

Inputs to the decoder come from the servo preamp and the MPU.
The servo preamp amplifies the signal detected by the servo
head. The +Slope signal, supplied by the MPU, sets up the
phase of the decoded Position signal so that it can be used by
the seek circuits.

The MPU monitors three output signals from the decoder. During
normal seek operations, the servo head remains over the data
zone. Thus, when the Inner or Outer Guard Band Pulses go act-
ive, the MPU reacts by altering the seek protocol. Improper
decoder operation can affect seek reliability. For this rea-
son, the MPU monitors the –Demodulator Active line.

Data transfers to and from the disk must be coordinated with
respect to the rotational position of the disk. The Index sig-
nal is decoded and is input to the Sector Detection circuitry
which, in turn, generates a given number of Sector pulses per
disk rotation. The controller coordinates data transfers based
upon the Index and Sector pulses transmitted to it via the in-
terface.

In the 340 MB drive, the 1.612 MHz Clock from the decoder is
used by the R/W PLO circuitry to form a 9.67 MHz Servo Clock.
In the 515 MB drive, the 2.41 MHz Clock from the decoder is
used by the R/W PLO circuitry to form a 14.5 MHz Servo Clock.
The Servo Clock operates at exactly six times the frequency of
the clock from the tribit decoder, and it tracks the rotational
velocity of the disk. The controller transfers data to the
disk in sync with the Servo Clock. This compensation in the
rate of data transfers to the disk makes the written data
pattern independent of disk speed.

83324770 A
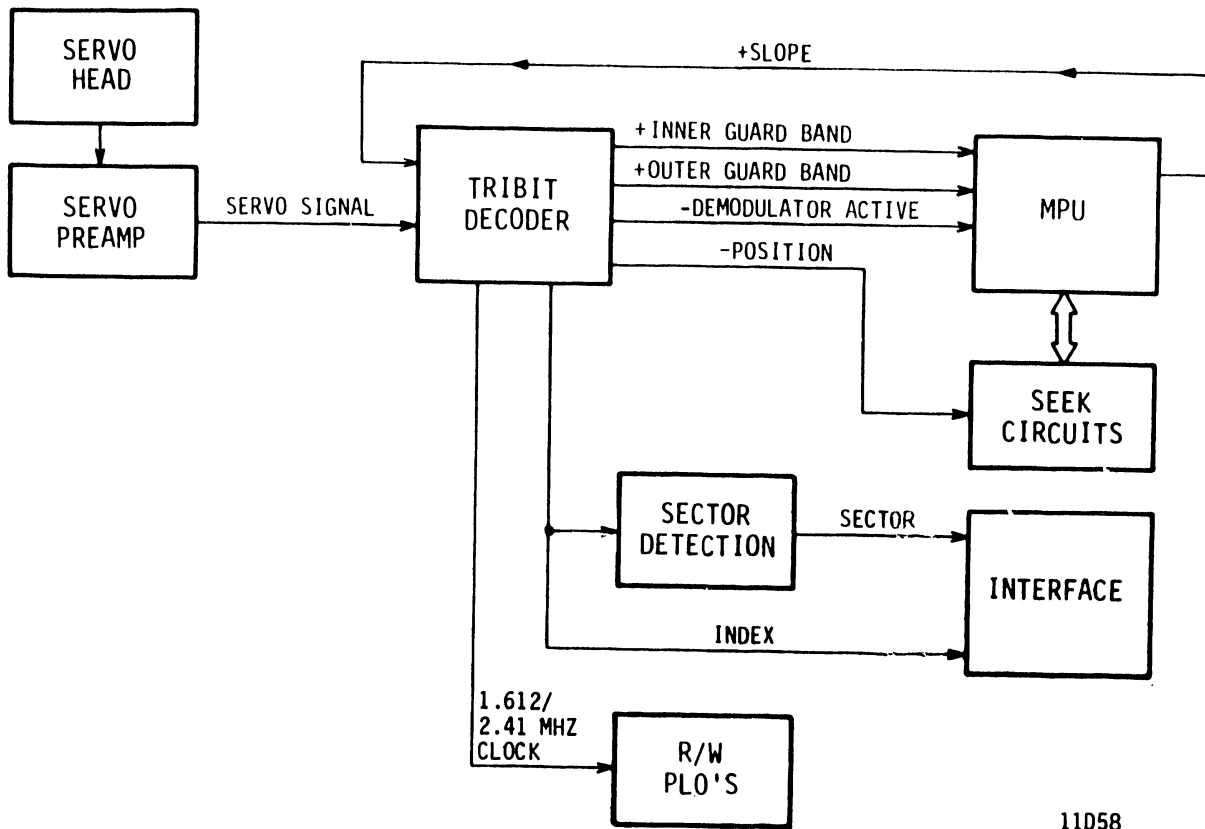
```
                                        +SLOPE
     ┌──────────┐
     │  SERVO   │
     │  HEAD    │
     └────┬─────┘
          │
          ▼
     ┌──────────┐   SERVO SIGNAL   ┌──────────┐  +INNER GUARD BAND   ┌──────────┐
     │  SERVO   │─────────────────▶│  TRIBIT  │───────────────────▶ │   MPU    │
     │  PREAMP  │                  │ DECODER  │  +OUTER GUARD BAND   │          │
     └──────────┘                  │          │───────────────────▶ │          │
                                   │          │  -DEMODULATOR ACTIVE │          │
                                   │          │───────────────────▶ │          │
                                   │          │     -POSITION        └──────────┘
                                   └──────────┘                           ▲
                                                                          ║
                                                                          ▼
                                                                     ┌──────────┐
                                                                     │  SEEK    │
                                                                     │ CIRCUITS │
                                                                     └──────────┘

                                   ┌──────────┐    SECTOR      ┌──────────┐
                                   │  SECTOR  │──────────────▶ │          │
                                   │DETECTION │                │INTERFACE │
                                   └──────────┘      INDEX     │          │
                                                   ──────────▶ └──────────┘
     1.612/
     2.41 MHZ                      ┌──────────┐
     CLOCK ──────────────────────▶│  R/W     │
                                   │ PLO'S    │
                                   └──────────┘
                                                      11D58
```

Figure 1-19.   Tribit Decoder System Diagram

The remaining topics within this discussion cover the operation
of circuits within the tribit decoder. Figure 1-20 is a block
diagram showing these circuits and their interconnections.

Sync Bit Detector

The Sync Bit Detector monitors the Tribits signal from the
Servo Preamp and generates a pulse on the -Sync Detect line
each time a sync bit occurs in the Tribits signal. Sync bit
detection is essential for all other tribit decoder functions
because sync bits are the primary input to the Servo PLO cir-
cuit which in turn controls the timing of the Position Demod-
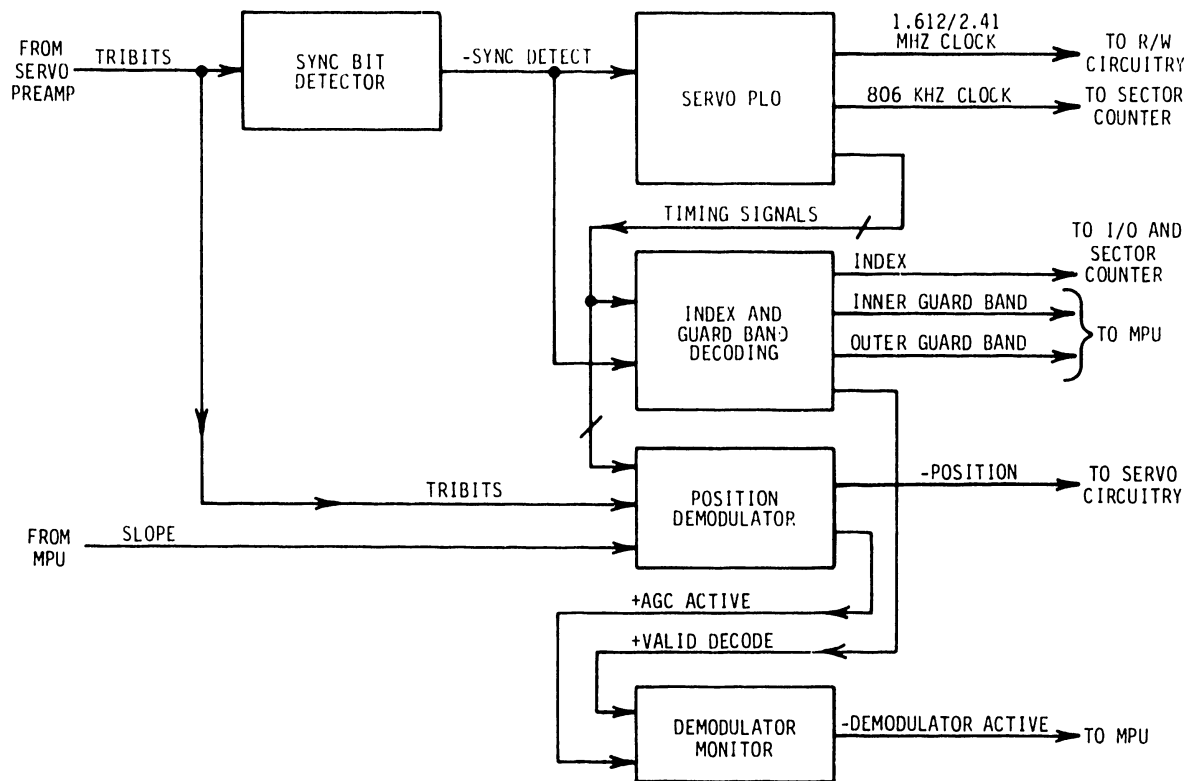
Figure 1-20.   Tribit Decoder Block Diagram

ulator and the Index and Guard Band Decoder. In addition, the
-Sync Detect signal reflects the encoding used to indicate In-
dex, Data, and Guardband regions on the servo surface. Figure
1-21 is a block diagram of the Sync Bit Detector.

The Tribits signal is applied to an AGC-controlled differential
amplifier. The amplifier output passes through a buffer stage
and is ac-coupled to the input of the first comparator. A dc
offset at the comparator input allows the comparator to be en-
abled only by the most negative portion of each sync bit.
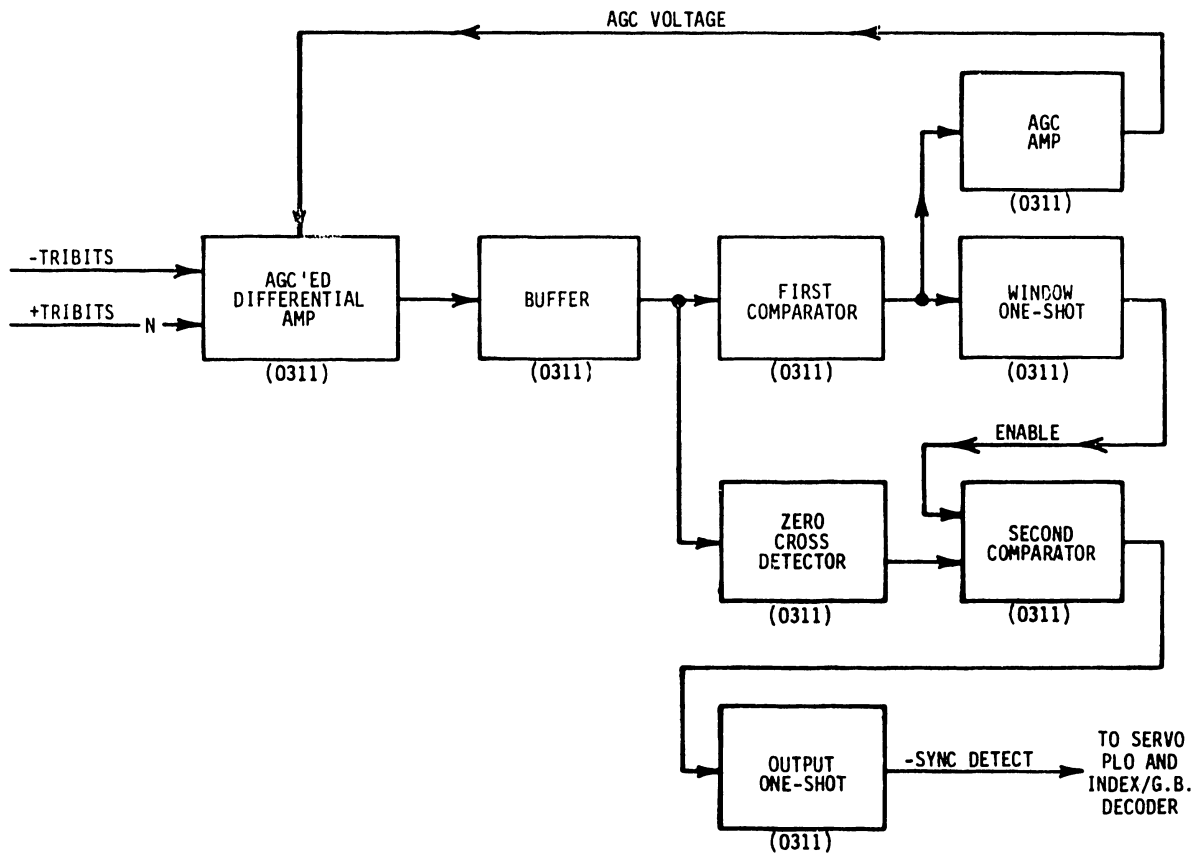
Figure 1-21.   Sync Bit Detector

Output pulses from the first comparator perform two functions. The AGC amp looks at these pulses and develops an AGC voltage to control the gain of the differential amplifier at the input. This AGC loop operates to ensure that the pulses coming from the first comparator have a constant duty cycle.

In addition to controlling AGC, the output pulses trigger a one-shot to develop a window during which sync bit detection is enabled. The gate from the window one-shot enables a second comparator. The input to the second comparator is the Tribits signal, differentiated by a zero-cross detector. The second comparator reacts only to zero-crossings produced when sync bits are expected because it is disabled at other times. Seeing an acceptable zero crossing, the second comparator triggers the output one-shot to generate a negative pulse on the -Sync Detect line.

Servo PLO

The Servo PLO uses a phase-locked loop to keep the timing in the tribit decoder synchronized to the detection of sync bits in the Tribit signal. As shown in figure 1-22, a portion of the Servo PLO circuitry is located in the Demodulator Logic Chip. Circuitry external to the chip includes a charge pump, the 9.67 MHz Voltage-Controlled Oscillator (VCO) and logic that compensates for missing sync bits.

The Sync Bit Detector supplies -Sync Detect pulses to the phase comparator in the Demodulator Logic Chip. As described under Servo Surface Format, each servo track has patterns encoded by missing sync bits to locate index on the disk and to indicate whether the track is in an inner or outer guard band or in the data zone. However, the phase comparator latch must be reset
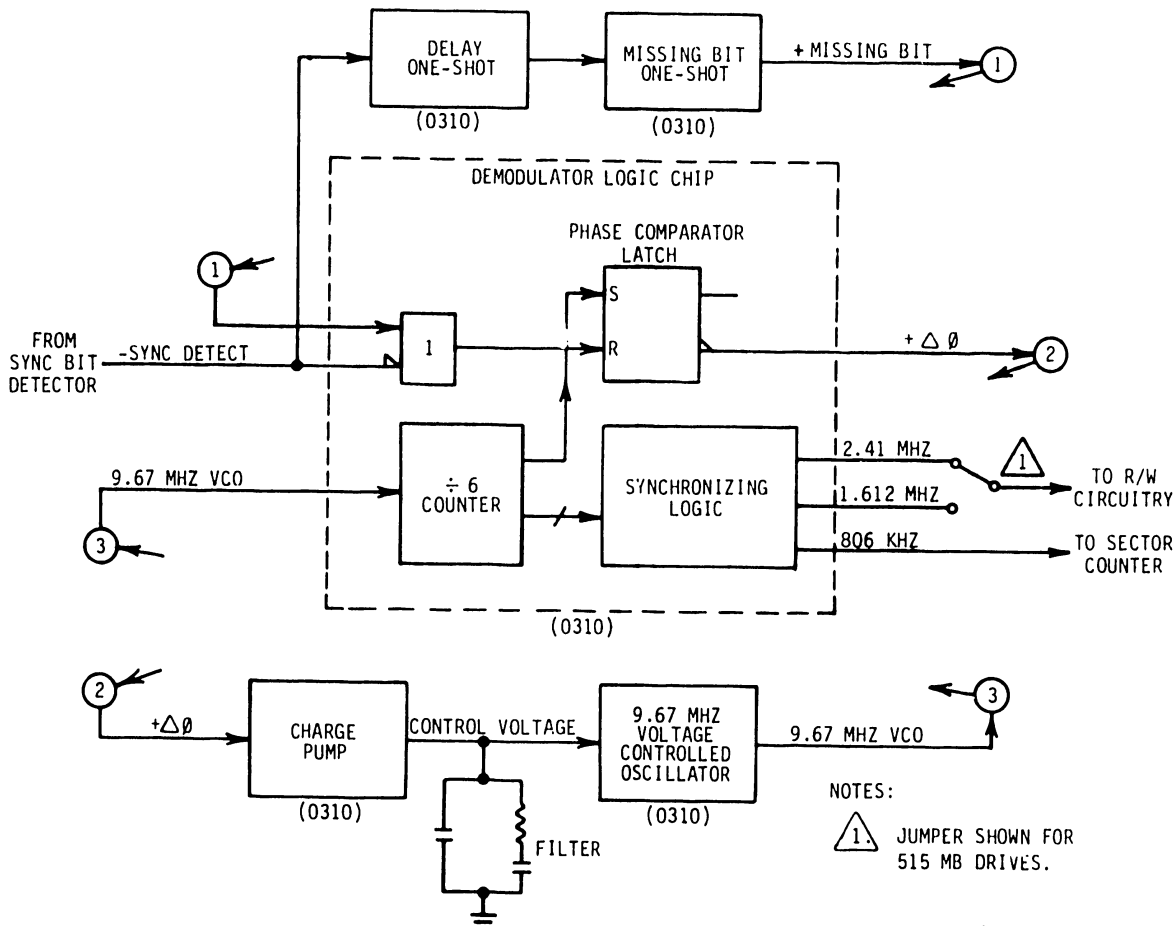
Figure 1-22.   Servo PLO Block Diagram

at regular intervals of about 620 ns. Because the encoded patterns never contain two consecutive missing sync bits, it is possible to develop a "dummy" trigger pulse whenever a sync bit is missed. To do this, -Sync Detect pulses clock a retriggerable one-shot. Each missing bit allows the one-shot to time out and trigger the missing bit one-shot. In this way, the phase comparator latch is reset periodically either by pulses on the -Sync Detect line or on the +Missing Bit line.

The Set input to the phase comparator latch is derived from a Divide-by-Six counter in the Demodulator Logic Chip. This counter is clocked by the 9.67 MHz signal from the VCO, which oscillates at six times the repetition rate of -Sync Detect pulses. The counter subdivides the interval between -Sync Detect pulses into six equal parts. Through various logical combinations of the outputs of the counter stages, the synchronizing logic develops gates needed for the different decoding operations. Because the PLO keeps the Divide-by-Six counter phase-locked to the detected sync bits, these timing gates stay synchronous with the tribit pattern. One of these gates, the Set input to the phase comparator latch, goes active when three VCO oscillations have occurred following reset of the latch. Thus, the +Delta Ø signal generated by the latch is active for three VCO oscillations and is then inactive until the next Reset input occurs (approximately three VCO oscillations later).

The phase comparator latch causes the VCO to shift in frequency when the active interval and the inactive interval of the +Delta Ø signal are not equal. This frequency shift is governed by a charge pump that supplies the control voltage to the VCO. When the +Delta Ø signal is inactive, the charge pump supplies current to the capacitors filtering the control voltage to the VCO (making the control voltage more negative). When the +Delta Ø signal is active, the charge pump draws current from these capacitors (making the control voltage more positive). Thus, any imbalance in the set and cleared intervals of +Delta Ø produces a net change in the control voltage.

Consider three situations of changing disk speed and its effect on the Servo PLO. When the disks are rotating at constant speed and the VCO is phase-locked, the set and cleared intervals of the phase comparator latch are equal, the control voltage is normal, and the VCO frequency remains the same. During a decrease in disk speed, the VCO frequency must decrease. In this case, the Set input to the latch is early, and +Delta Ø is inactive longer than it is active. This makes the control voltage more negative which in turn reduces the VCO frequency. During an increase in disk speed, the VCO frequency must increase. In this case, the Set input to the latch is late, and +Delta Ø is active longer than it is inactive. This makes the control voltage more positive which in turn increases the VCO frequency.

The Divide-by-Six counter develops timing signals used by the Position Demodulator and by the Index and Guard Band Decoder. In addition, the following clocks are derived from the VCO signal:

- 806 kHz -- derived by dividing the VCO signal by twelve and supplied to the Sector Counter Gate Array.

- 2.41 MHz -- derived by dividing the VCO signal by four and supplied to the Write PLO in 515 MB drives.

- 1.61 MHz -- derived by dividing the VCO signal by six and supplied to the Write PLO in 340 MB drives.

Position Demodulator

The Position Demodulator consists of the circuitry in the Tribit Decoder that develops the -Position signal. It derives this signal from the position bits in the Tribit pattern while depending on timing information developed from the sync bits in the Tribit pattern. The timing information is consistent on all servo tracks while the position information changes from track to track. Consistent timing information keeps the demodulator synchronized (regardless of the position or velocity of the servo head) and allows the demodulator to detect the changes in position information from which the -Position signal is derived. Figure 1-23 is a block diagram of the Position Demodulator, and figure 1-24 provides typical waveforms for the circuit. The following paragraphs review how position is encoded on the servo surface, discuss signal flow through the demodulator, and describe briefly how the Position signal is used by the servo circuitry.

As described earlier under Tribit Recording Scheme, any given tribit pattern contains two position bits. One bit is supplied by each of the two servo tracks closest to the servo head, and the two bits are staggered so they appear in sequence in the Tribit signal. If the position bits available from one set of alternate servo tracks are designated as #1 bits and the position bits from the remaining tracks are designated as #2 bits, then the Position signal is positive when the #2 bit amplitudes exceed the #1 bit amplitudes and is negative when the #1 bit amplitudes exceed the #2 bit amplitudes. The synchronizing logic in the Demodulator Logic Chip develops gating signals (+ØA and +ØB) that discriminate between the #1 bits and #2 bits. This logic is initialized when an Index pattern (resync pattern) occurs in the Tribit signal (see Index and Guard Band Decoding). Through the resync process, gating signals internal to the Demodulator Logic Chip are forced to match the format of the tribits as they were recorded on the servo surface.
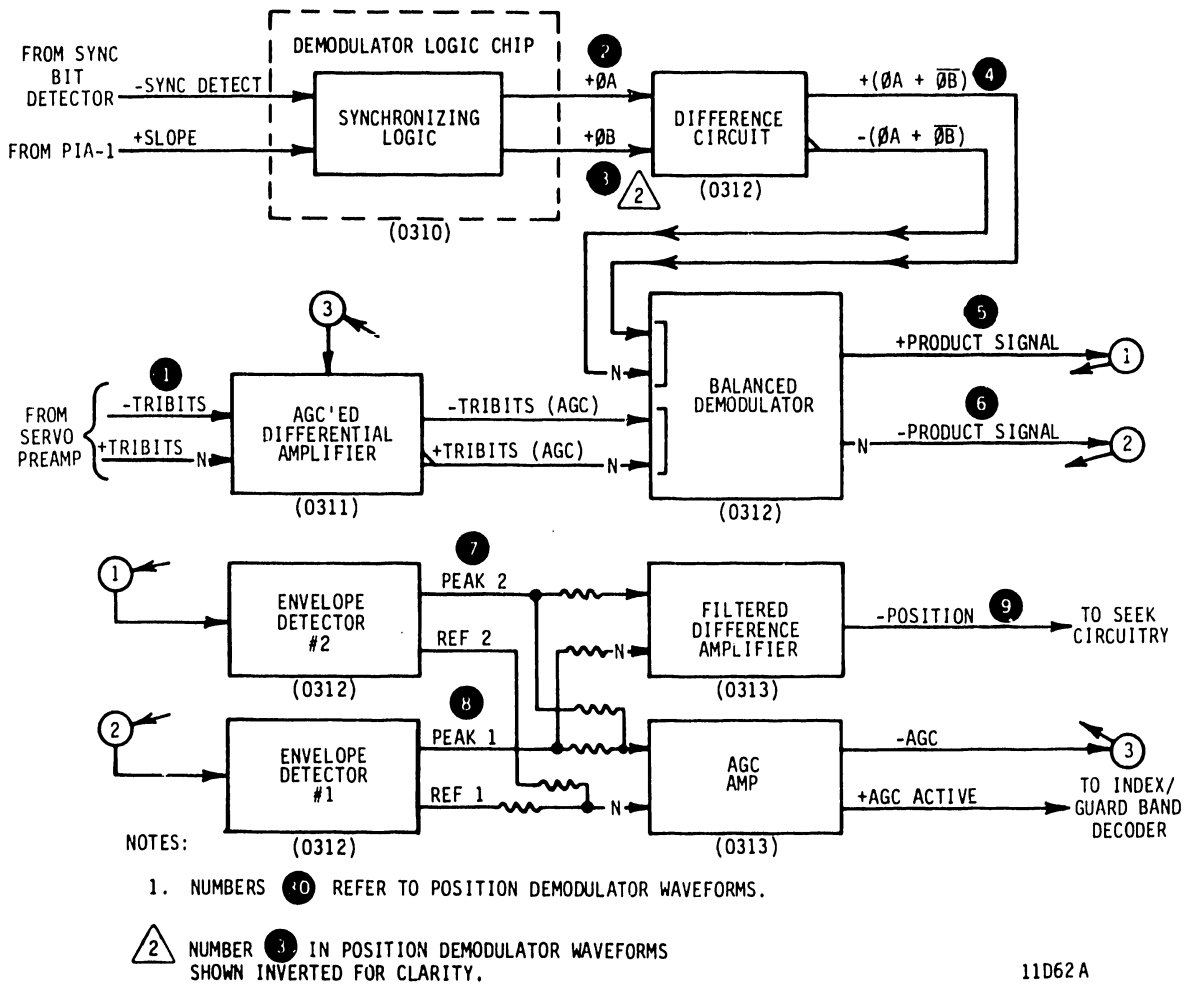
Figure 1-23. Position Demodulator Circuitry

Figure 1-24. Position Demodulator Waveforms
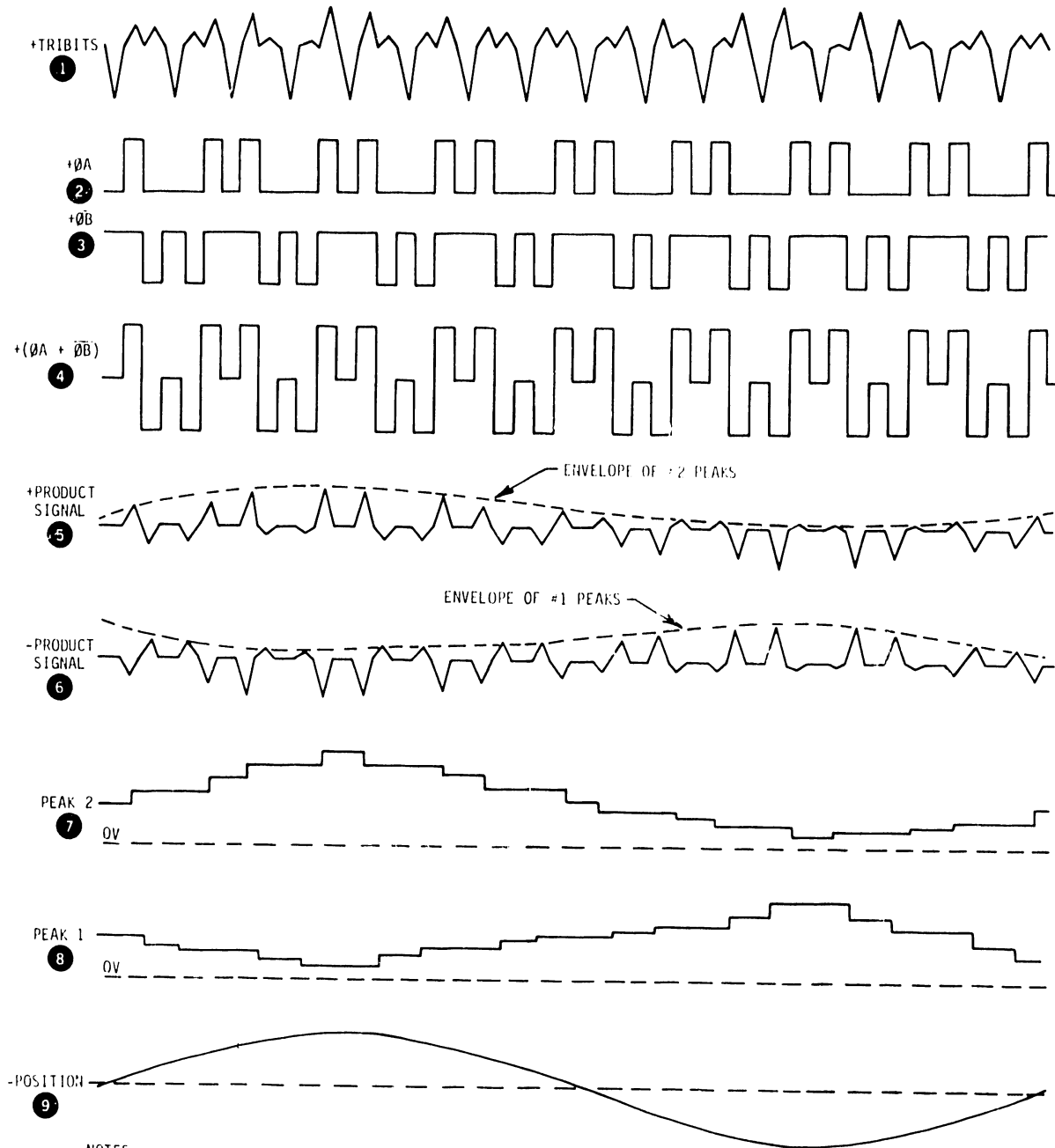
NOTES:

1. NUMBERS **30** REFER TO POSITION DEMODULATOR CIRCUIT DIAGRAM.

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These internal gating signals are output from the Demodulator
Logic Chip as the +ØA and +ØB signals. However, the MPU con-
trols which internal gate becomes +ØA and which gate becomes
+ØB via the +Slope signal issued by PIA-1. At the start of a
new seek, the MPU sets the level of the +Slope signal, thereby
choosing whether or not to interchange the +ØA and +ØB sig-
nals. Interchanging them inverts the Position signal and al-
lows the MPU to ensure that the +Position signal will have the
required slope as the seek circuits position the heads at their
new destination. This slope requirement is discussed further
under Seek Functions.

As shown in figure 1-23, the balanced demodulator uses the
+ØA and +ØB signals to develop, from the Tribits signal, in-
put signals for the two channels of envelope detection. The
balanced demodulator has two differential inputs: a three-step
gating signal and an Amplified Tribits signal. The Amplified
Tribits signal is produced from the Tribits signal by an AGC-
controlled differential amplifier. A difference circuit devel-
ops the +(ØA + not-ØB) signal and its inverse from the +ØA
and +ØB gates.

Figure 1-24 shows typical input and output waveforms for the
balanced demodulator. The balanced demodulator multiplies the
two input signals to create complementary product signals. Be-
cause the three-step gating signal is zero when sync bits ap-
pear, the product signals contain only position peaks. In the
+Product signal, the #2 bits are positive and the #1 bits are
negative. In the -Product signal, the opposite is true.

Although each envelope detector's input contains both positive
and negative peaks, the detector is sensitive only to changes
in the positive peaks. Each detector uses two transistors to
update the voltage on a capacitor. In intervals where the en-
velope amplitude is increasing (successive peaks are more posi-
tive), one transistor pulls the capacitor voltage up. In in-
tervals where the envelope amplitude is decreasing, the other
transistor pulls the capacitor voltage down. Because this ad-
justment occurs at the instant of peak detection, the output
signal from the detector steps to a new level, holding that
level until the next peak. Additional transistors in each de-
tector circuit act as current sources and provide temperature
compensation.

The envelope detectors' outputs, the Peak 1 and Peak 2 signals,
are differential inputs to a filtered difference amplifier.
This stage develops the -Position signal by subtracting Peak 1
from Peak 2. It uses a low-pass filter to remove from the -Po-
sition signal any high frequency noise, resulting from the

steps in the Peak 1 and Peak 2 inputs. The -Position signal is zero when the servo head is centered between two servo tracks. At this time, the data heads are positioned directly over a data track. The -Position signal varies either positive or negative depending on displacement of the servo head from that centerline.

The AGC Amp monitors the sum of the Peak 1 and Peak 2 signals, relative to the sum of two bias voltages (Ref 1 and Ref 2) from the envelope detectors, to produce an AGC voltage for the differential input amplifier. AGC action keeps the peak-to-peak amplitude of the -Position signal independent of servo signal variations. A level detector, connected to the AGC voltage, issues the +AGC Active signal to indicate that position demodulation is satisfactory. If the +AGC Active signal goes low or if valid decoding ceases (see the next topic), the -Demodulator Active line goes high, warning the MPU that the tribit decoder is not functioning properly.

With one exception, movement of the servo head from one track to an adjacent track reverses the polarity of the Position signal. This is true when the servo head crosses tracks in the guard bands and the data zone. However, the buffer zone, located between the outer guard band and data zone, has two consecutive tracks that are recorded with identical (not alternating) position information. Thus, as the servo head moves across these tracks, the Position signal stays negative and does not cross zero as it does in the other zones. This characteristic of the Position signal is needed for Return to Zero seeks (see Seek Functions).

Index and Guard Band Decoding

The index and guard band decoding circuitry produces output pulses each time the servo head detects certain codes in the pattern of sync bits on the servo surface. This circuitry also originates the +Valid Decode signal which is used to indicate reliable decoder operation. Refer to Servo Surface Format for a description of the sync bit codes and their location on the servo disk.

Figure 1-25 is a block diagram of the index and guard band decoding circuitry. This circuitry is located in the Demodulator Logic Chip.

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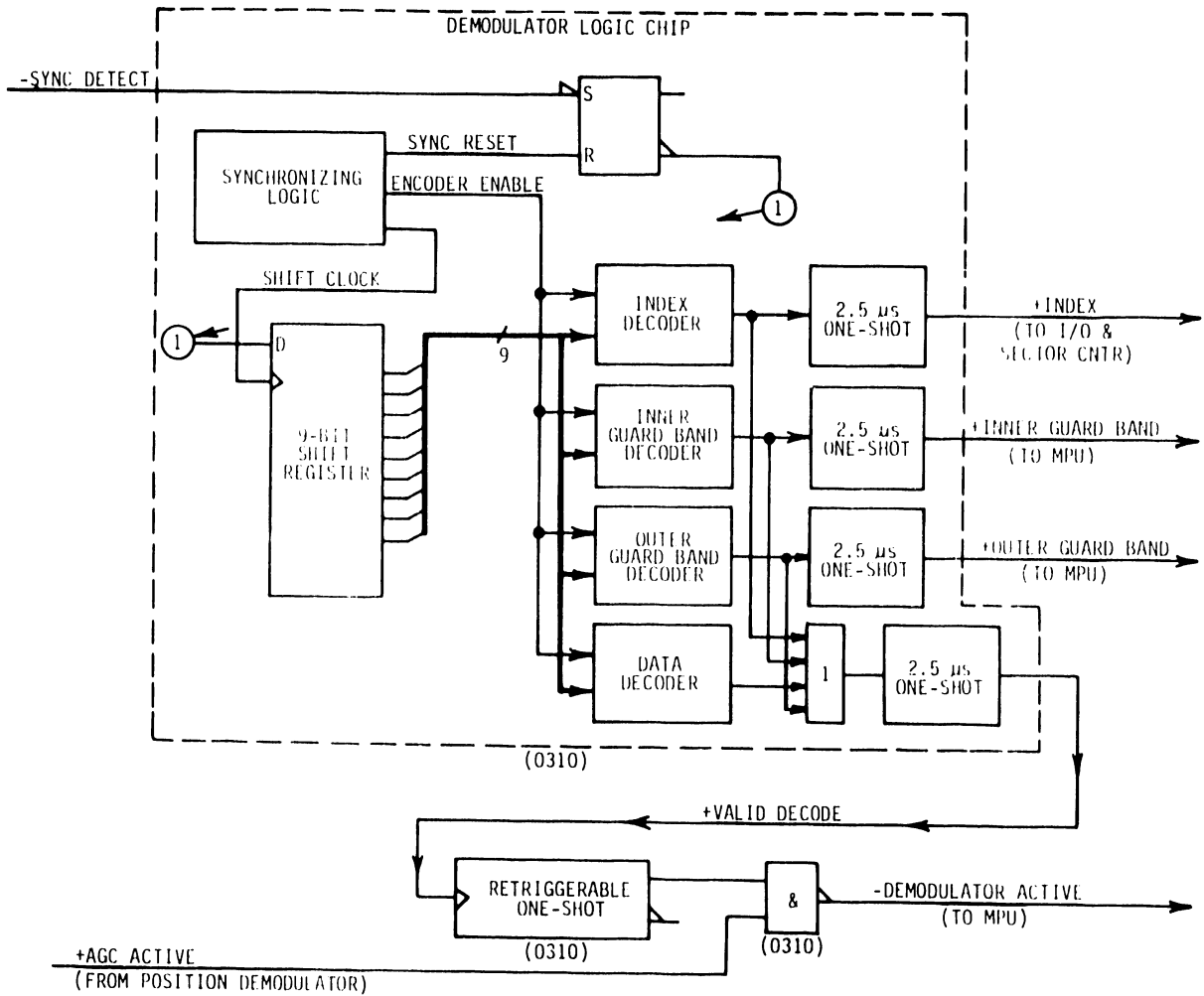
Figure 1-25.   Index and Guard Band Decoder

The decoding circuit responds to three timing signals that repeat in sequence for each tribit pattern detected. The synchronizing logic, controlled by the Servo PLO, issues the Sync Reset signal prior to the detection of each sync bit. If a sync bit is detected, a low pulse on the -Sync Detect line sets a FF. If no sync bit was detected, however, the FF remains reset. The next timing signal, Shift Clock, clocks the output of the FF into the first stage of a 9-bit shift register and produces a shift in the register.

The shift register contains information about whether a sync bit was present in each of the nine preceding tribit patterns. After clocking the shift register, the synchronizing logic activates a gate (Decoder Enable) that enables each of the decoder circuits shown in figure 1-25. Each decoder looks for a particular pattern of ones and zeros in the shift register's outputs corresponding to a code of missing sync bits on the servo track. The codes detected are as follows:

- When the register contains 101000101, the Index Decoder triggers two one-shots to activate the +Index and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010101, the Outer Guard Band Decoder triggers two one-shots to activate the +Outer Gu d Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 101010001, the Inner Guard Band Decoder triggers two one-shots to activate the +Inner Guard Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010001, the Data Decoder triggers a one-shot to activate the +Valid Decode line for 2.5 microseconds. The Demodulator Logic Chip has no output corresponding to the code for the data zone.

The Inner and Outer Guard Band signals are supplied as interrupts to the microprocessor at PIA-1. These interrupts inform the microprocessor that the heads are not located over the data zone. The Index signal is sent to the controller and is used by the Sector Counter, as described in the next topic.

Pulses on the Valid Decode line are supplied as triggers to a retriggerable one-shot. During normal decoder operation, this one-shot stays set. If the one-shot times out, the -Demodulator Active line to the MPU goes high to indicate improper decoding.

Sector Detection

The sector detection circuit (figure 1-26) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

A Sector pulse is generated each time the Sector counter (located in the Sector Counter Gate Array) reaches its maximum count (4095). A carry from the counter triggers a 1.25 microsecond one-shot which generates the Sector pulse. The counter is incremented by the 806 kHz clock pulses, derived from the Servo PLO signal in the Demodulator Logic Chip. The Index pulse resets the counter allowing 13 440 clock pulses per revolution of the disk.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13 440 divided by 64) and the counter would be preset to 3886. In this case, the counter starts at 3886 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to volume 1 of the maintenance manual for details regarding the setting of the sector switches.

SEEK FUNCTIONS

GENERAL

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of a microprocessor unit (MPU), control this function. The drive servo circuits translate MPU instructions into electromechanical motion to position the read/write heads accurately and to allow the transfer of magnetic pulses to and from a disk storage surface. The two main topics of this section describe servo circuit operation and the sequencing of
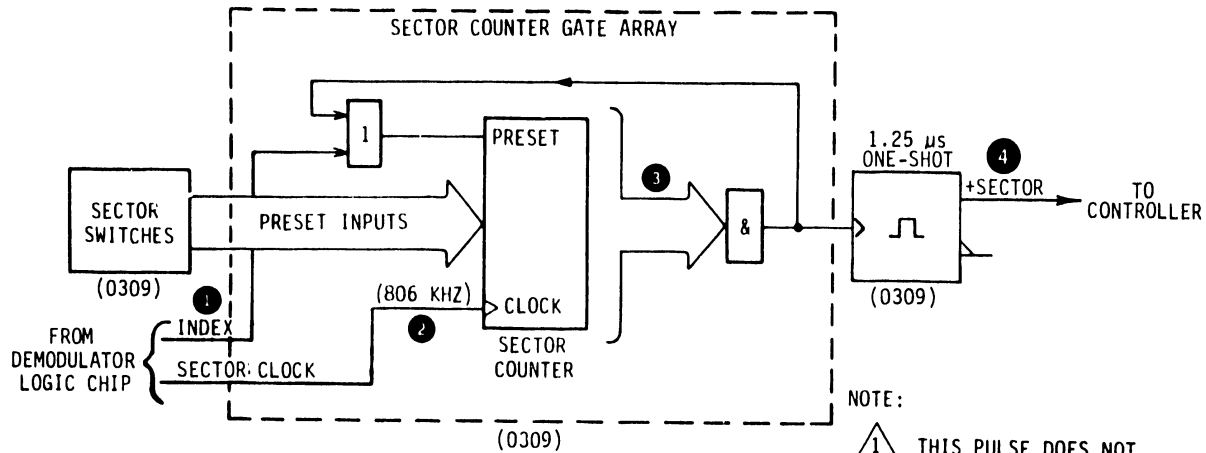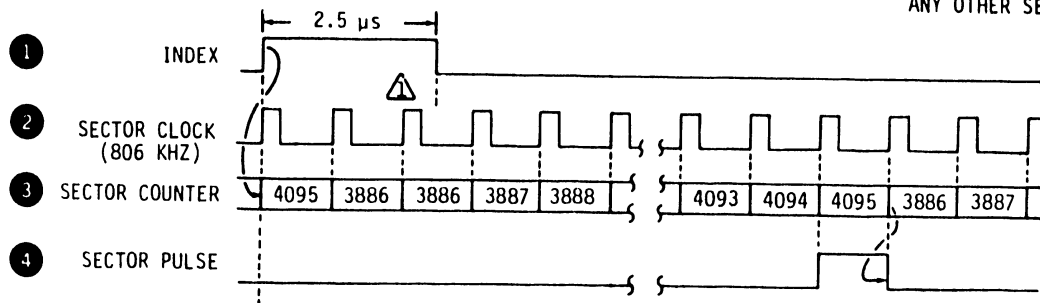
Figure 1-26.   Sector Detection - Logic and Timing

events in different types of seeks. Since these subjects are
interrelated, they are preceded by an overview of system opera-
tion that explains the roles played by the interface and the
MPU, and that describes the servo functions in general terms.

SYSTEM OVERVIEW

Each seek operation can be described in terms of four basic
drive activities. These activities are shown in terms of gen-
eral information flow between major drive functional elements
in figure 1-27. These activities occur in the following se-
quence:
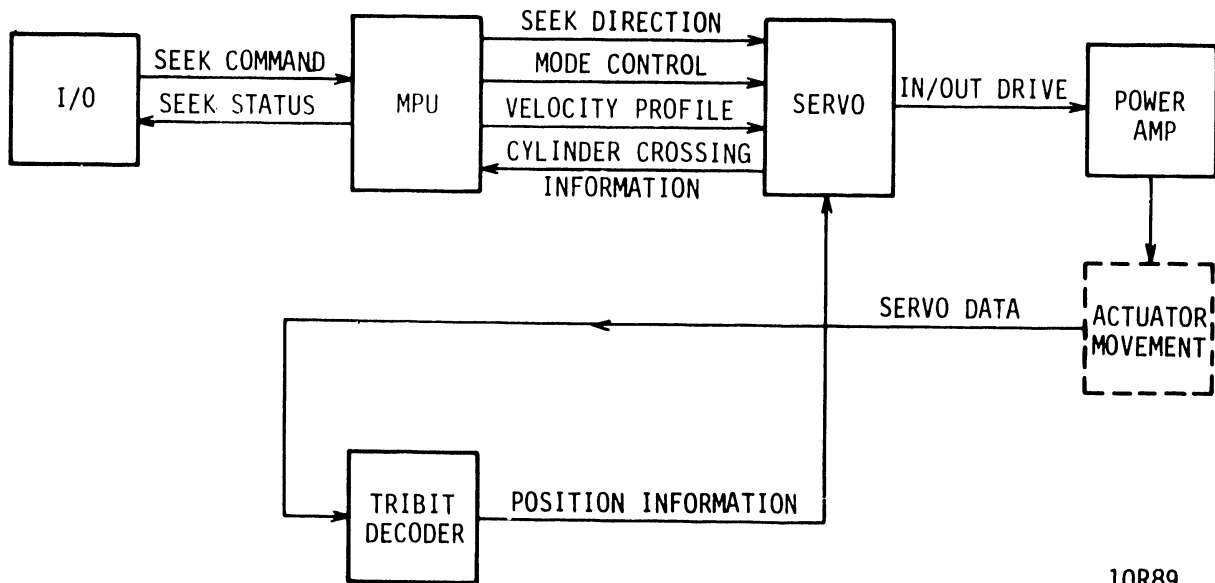
Figure 1-27. Seek Functions Block Diagram

- Command -- The interface processes the command from the controller that instructs the drive to seek to a different cylinder on the disks.

- Control -- The MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.

- Execution -- The servo circuitry executes the seek in response to control information received from the MPU. This execution is accomplished in three modes: the coarse mode, during which the actuator is moved at a controlled velocity toward its destination; the settle-in mode, in which the actuator locks in to its final position; and the track-following mode, in which the actuator position is maintained until another seek is commanded. The servo controls current to the voice coil to move the actuator/heads via in and out drive signals to the power amp. Position information from the tribit decoder serves as a feedback source to the servo loop and is converted into cylinder crossing information for the MPU.

●   Status -- The MPU informs the controller via the inter-
     face whether or not the seek was accomplished success-
     fully. This indicates whether or not a reliable data
     transfer can be performed on the selected cylinder.

The concept of a closed loop is essential to understanding the
operation of the servo system. Figure 1-28 shows a generalized
servo loop that illustrates several principles governing the
servo loops in the drive. The inputs to the summing amp are
added, and any departure of the sum away from zero indicates
that the system is unbalanced. To compensate for the imbal-
ance, the summing amp issues a correction signal to the mechan-
ical system. The response of the mechanical system is convert-
ed into an electrical signal which is an input to the summing
amp. Mechanical movement continues until the system balance is
restored, corresponding to a null in the summing amp inputs.

The drive employs two basic servo loops, a coarse loop used in
the coarse mode and a fine loop used in the settle-in and
track-following modes. In figure 1-29, the model of figure
1-28 is used to show the coarse servo loop in simplified form.
In the coarse loop, the actuator moves at a prescribed velocity
from the original cylinder address to the final cylinder ad-
dress. The summing amp receives two inputs -- one signal rep-
resents the prescribed (desired) velocity of the actuator and
the other represents the measured velocity of the actuator.
When the desired velocity exceeds the measured velocity, de-
sired current is produced to accelerate the actuator. When the
measured velocity exceeds the desired velocity, desired current
is produced to decelerate the actuator. The actuator is al-
lowed to coast when the two inputs are equal.

In figure 1-30, the model of figure 1-28 is used to show the
fine servo loop in simplified form. In the fine loop, the
heads settle-in to their destination position and then maintain
their position on track. The summing amp has no programmed in-
put. Its only input is the Position signal, which is nulled at
track center and varies positive or negative depending on how
far the heads are displaced from track center. Any displace-
ment of the heads from track center is adjusted by the fine
loop until the summing amp input is nulled.

The following paragraphs discuss the circuit operation of these
loops in more detail and then go on to describe the sequence of
events in typical seeks.
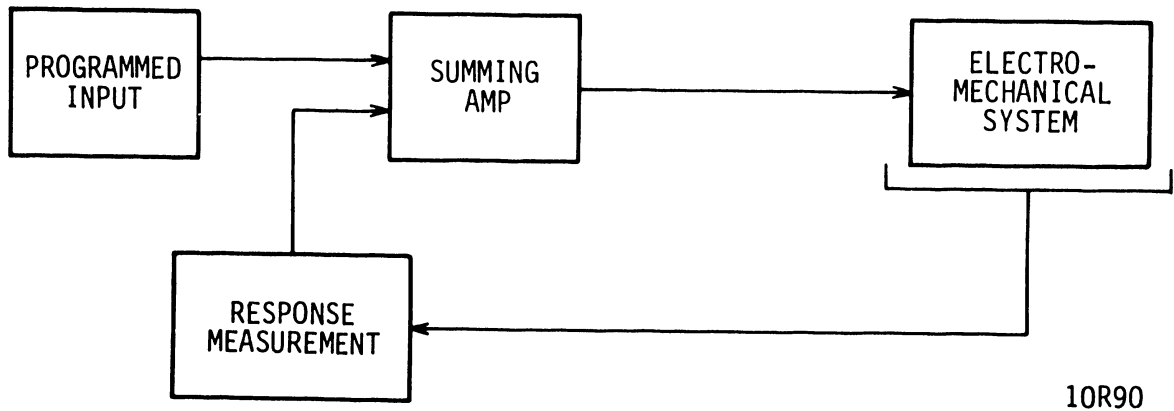
Figure 1-28.   Generalized Servo Loop
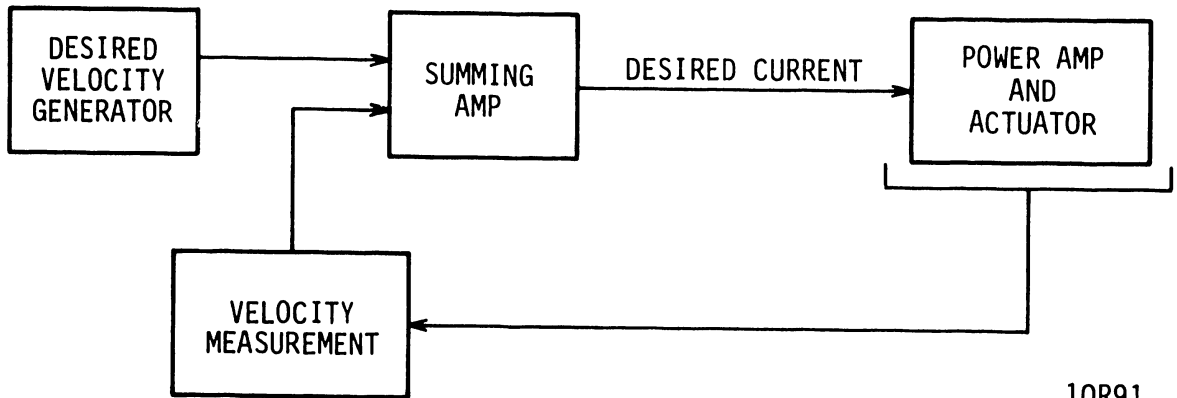
Figure 1-29.   Simplified Coarse Servo Loop
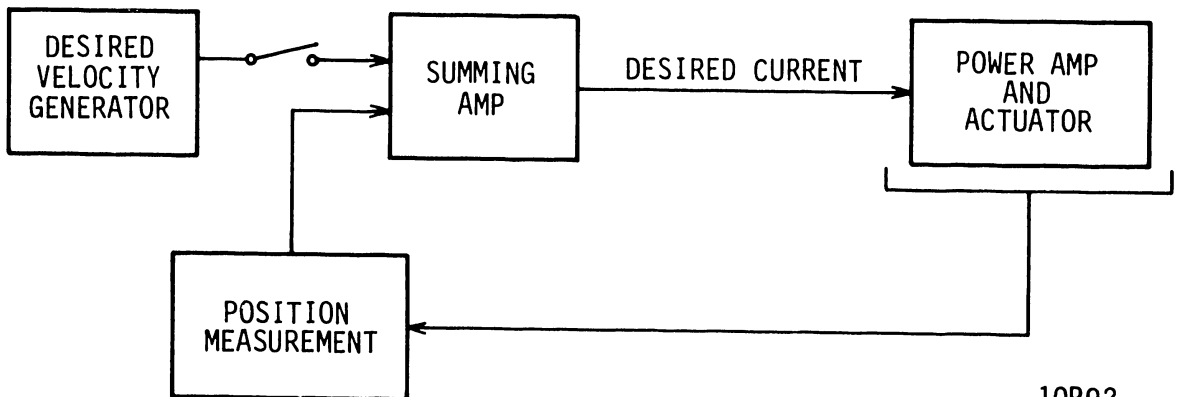
Figure 1-30.   Simplified Fine Servo Loop

SERVO CIRCUIT FUNCTIONS

General

Servo circuit functions are discussed in terms of the two basic loops within the servo circuitry (coarse and fine loops). The coarse loop and the fine loop have some circuit elements in common. These common circuit elements are described in detail under Coarse Loop Operation and are mentioned briefly under Fine Loop Operation. Seek operations follow defined sequences in which the MPU exercises control over the servo circuitry. These sequences are described under the next topic, Types of Seeks.

Coarse Loop Operation

General

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one half track of the new address. Figure 1-31 is an overall block diagram of the coarse loop circuitry. Discussion of the coarse loop is presented in the following topics·

- Microprocessor Control System

- Desired Velocity Generation

- Cylinder Pulse Detection

- Velocity Measurement

- Summing Amp

- Power Amp Driver

- Power Amplifier

Microprocessor Control System

The microprocessor control system monitors various functions of the drive and executes most of the control sequences required for seek functions. The following paragraphs provide a general description of the components and signal paths in the microprocessor system, and describe the role of the microprocessor system pertaining to seek functions. Figure 1-32 is a block diagram of the microprocessor system. Readers interested in internal operation of the microprocessor and its peripheral chips may refer to the CDC Microcircuits Manual for more information.

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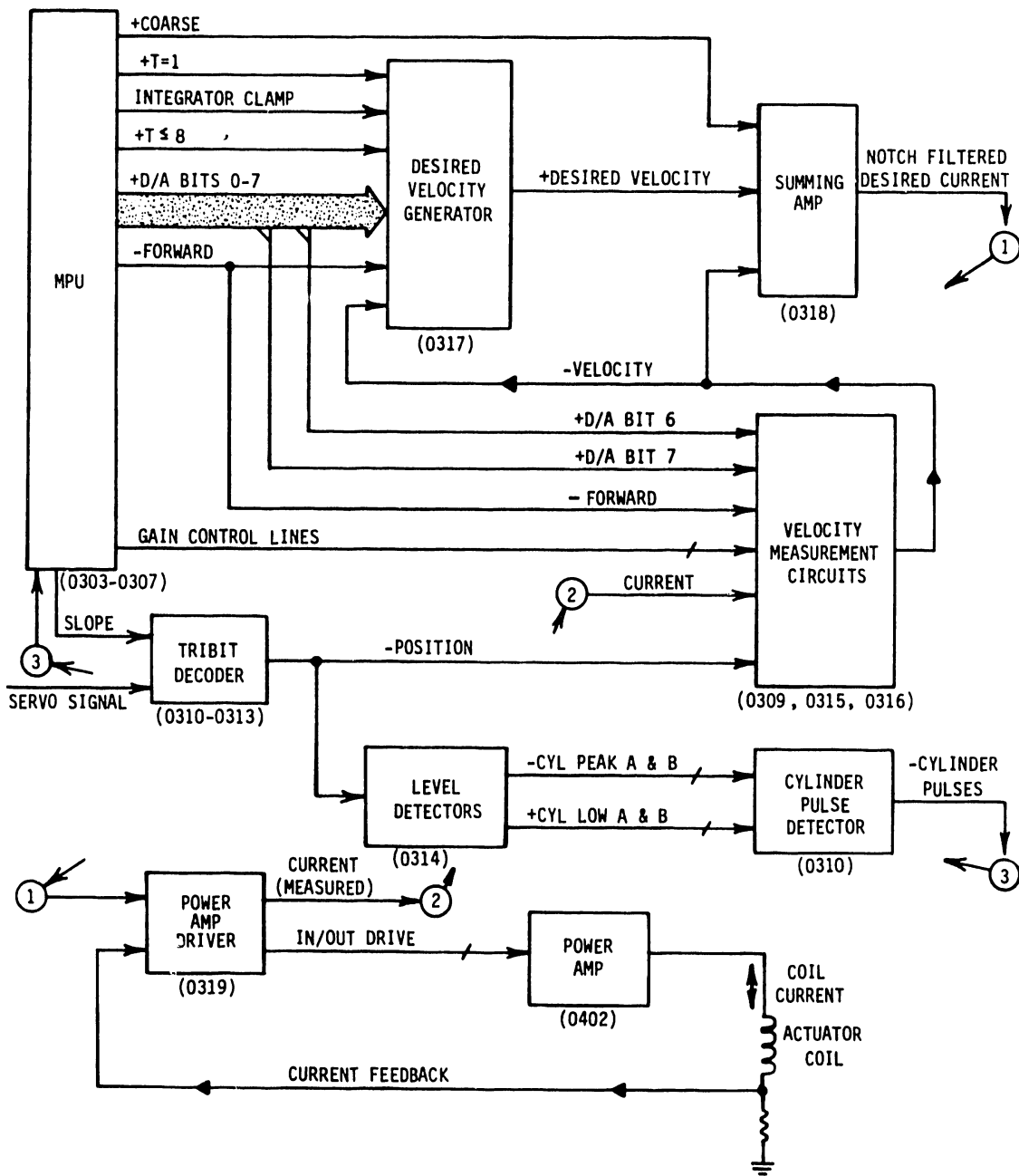
Figure 1-31.   Coarse Loop Block Diagram
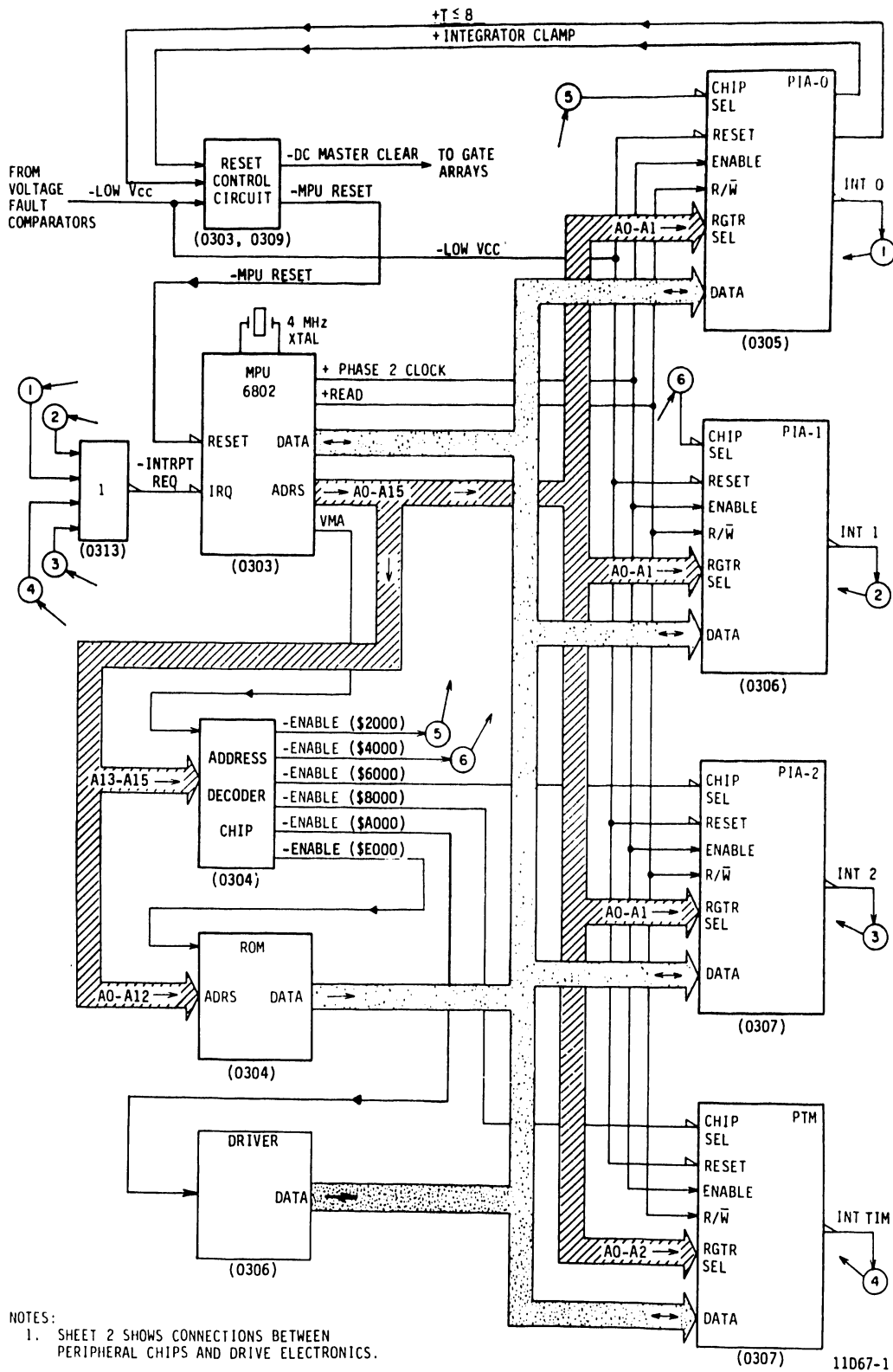
Figure 1-32. Microprocessor Control System (Sheet 1 of 2)
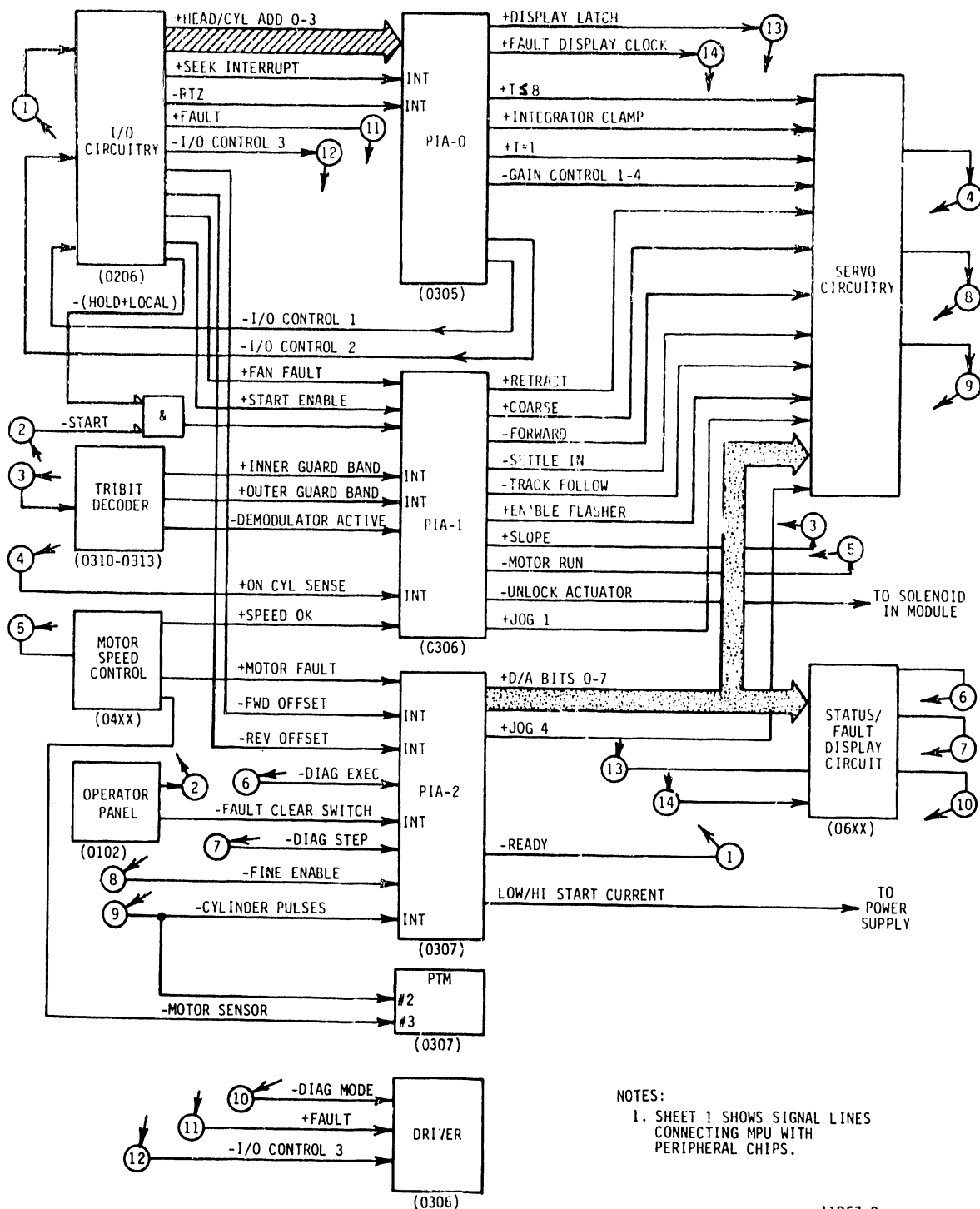
Figure 1-32. Microprocessor Control System (Sheet 2)

The microprocessor control system consists of a 6802 micropro-
cessor unit (MPU), a 8K-byte read-only memory (ROM), three per-
ipheral interface adapter (PIA) chips, and a programmable tim-
ing module (PTM). The MPU communicates with its peripheral
chips via an 8-bit bidirectional data bus, a 16-bit address
bus, and several control lines. A decoder chip monitors Ad-
dress lines 13 through 15 and develops chip select signals for
each peripheral chip whenever the Valid Memory Address line is
active. The MPU sets the Read line to read data from a periph-
eral or clears the line to write data into a peripheral. The
Phase 2 Clock, developed by a crystal-controlled oscillator in
the MPU, provides a timing reference for the system.

The firmware instructions for the MPU reside in the ROM. De-
tailed information about the MPU programming is beyond the
scope of this manual. However, the various sequences which the
MPU performs are outlined under Power Functions and Types of
Seeks. The ROM also contains a lookup table that specifies a
velocity profile for normal seeks.

A driver chip and three PIAs allow the MPU to monitor the digi-
tal levels of certain signals developed in hardware external to
the microprocessor system. In addition, the MPU can output
various command signals via the PIAs. Certain PIA input sig-
nals form maskable interrupts to the MPU. When unmasked, these
interrupts inform the MPU of status changes, that require
switching to a different routine within its firmware. The
specific PIA inputs and outputs are listed in figure 1-32 and
are referenced in the applicable circuit descriptions. A set
of PIA lines requiring additional explanation includes I/O Con-
trol lines 1, 2, and 3. I/O Control lines 1 and 2 go from
PIA-0 to the I/O Gate Array. These lines allow the MPU to per-
form various operations inside the gate array, such as setting
the On Cylinder and Seek Error FFs, multiplexing cylinder and
head addresses out of the array, and reading various fault sta-
tuses via the I/O Control 3 line.

Within the PTM, counter #2 allows the MPU to count tracks-to-go
in a seek. This counter is decremented during seeks by cylin-
der pulses. Counter #3 is used by the MPU to generate timeouts
for various operations and to make speed checks of the drive
motor.

The MPU system performs the following basic functions during
drive operation:

● It monitors start and interlock conditions to initiate
   load and retract operations.

● It starts and stops the drive motor, and it checks motor
   speed.

- It monitors the Seek Interrupt line and executes normal seeks.

- It specifies the desired actuator velocity during coarse seeks.

- It monitors the RTZ Interrupt line and executes RTZ seeks.

- It controls the On Cylinder and Seek Error FFs in the I/O Gate Array.

- It performs diagnostic functions in response to inputs entered on the Fault Display board.

These functions are described in detail in the remainder of Seek Functions. In addition, the MPU exchanges fault status with the I/O Gate Array. This activity is discussed under Fault and Error Conditions.

Desired Velocity Generation

The desired velocity circuit generates the +Desired Velocity signal, a changing analog voltage that indicates the desired velocity of the actuator throughout the coarse mode of the seek. Throughout the seek, the MPU refers to a table in the ROM that specifies desired velocity in binary form as a function of the number of tracks to go (T), which is the number of track crossings remaining until the heads reach their destination.

The velocity table is organized in a manner that allows one table of values to be used for all seeks. The maximum velocity of the table is for 255 tracks, and as the values decrease, a velocity profile is developed whereby velocity is proportional to the square root of the distance remaining. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position. The organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when T=30 is the same regardless of the total seek length.

The desired velocity circuit provides a ramp signal from the D/A (Digital to Analog) Converter based upon the eight D/A Bits it receives from the ROM table via PIA-2 (see figure 1-33). When T≤8, however, the two uppermost D/A bits are masked out at the D/A and are used elsewhere, and the Integrator Clamp signal is input via PIA-0 to provide a sawtooth signal from the Velocity Integrator to add fill-in current to the ramp as the heads
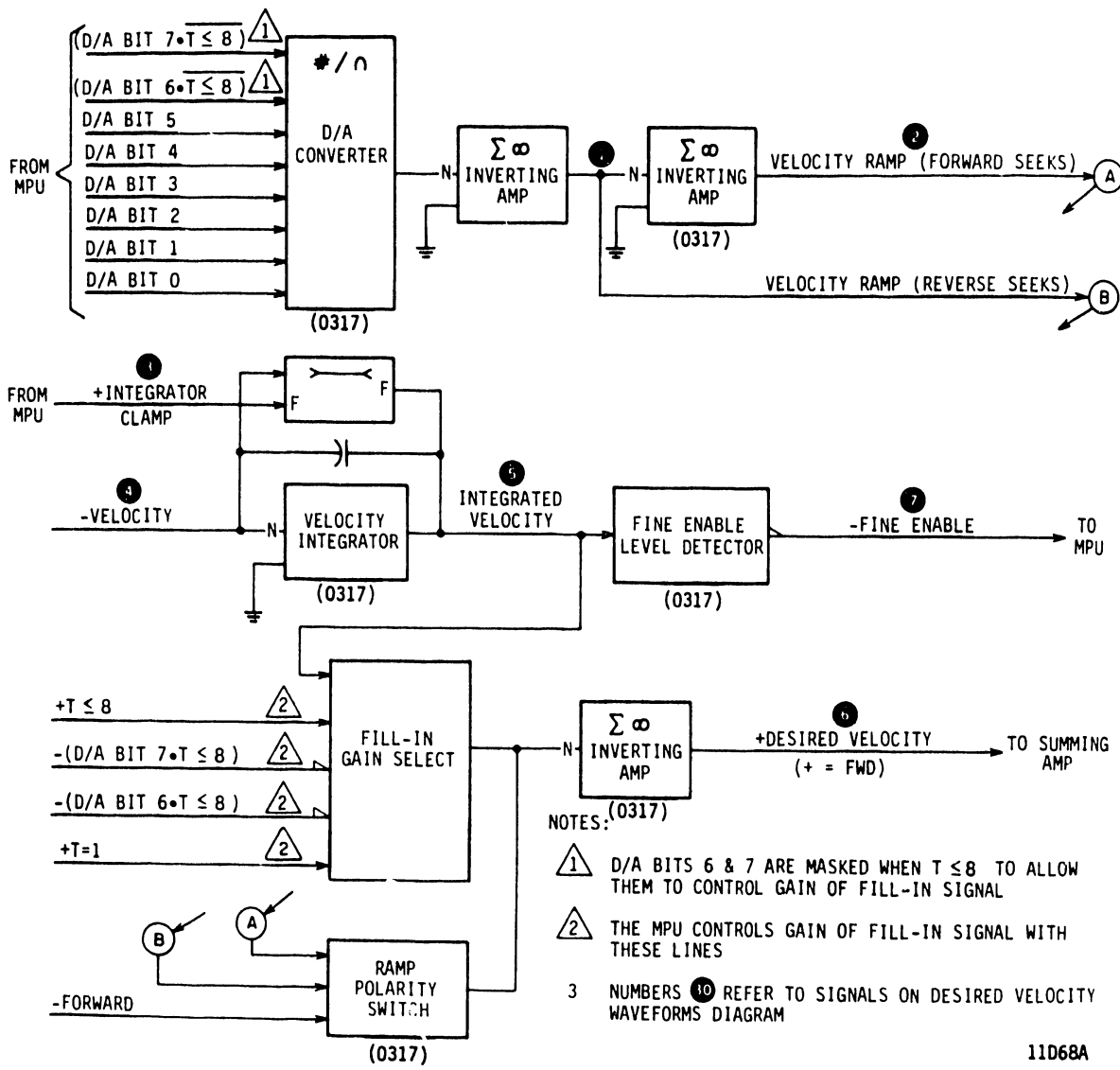
Figure 1-33. Desired Velocity Circuit

approach the selected track. At each cylinder crossing, the MPU refers to a count of tracks to go in PTM Counter #2 and outputs the current value of tabulated velocity using the D/A Bits. Each change in the D/A Bits results in a stepped change in the D/A ramp. Typical waveforms for the desired velocity circuit are given in figure 1-34.

The sawtooth from the Velocity Integrator compensates for the stepped nature of the D/A ramp by filling in the sudden changes in the ramp. When T<40, the sawtooth output is obtained by integrating the -Velocity signal from the velocity circuit. This output is clamped to zero each time a cylinder crossing occurs. D/A Bits 6 and 7 are reserved for controlling the degree of filling provided by the sawtooth in the final portion of the seek (when $T \leq 8$). These bits are set or cleared according to the ROM velocity table, but they are masked out of the D/A Converter input when $T \leq 8$. In the final tracks of the seek, when the velocity signal being integrated is reduced, the portion of the sawtooth applied to the +Desired Velocity signal is increased accordingly.

The sawtooth from the Velocity Integrator serves an additional purpose in the final track of coarse mode. Integrating velocity gives an indication of displacement. Each time the sawtooth reaches a specified value corresponding to a 1/2 track displacement from the last cylinder crossing, a level detector which monitors the sawtooth issues the -Fine Enable signal. With T<1, the MPU looks for this signal and reacts by switching servo operation from the coarse mode to the settle-in mode.

Cylinder Pulse Detection

A Cylinder Pulse is generated each time the heads cross a servo track during the coarse seek operation. Cylinder pulses serve two purposes. First, they decrement Counter #2 in the PTM, keeping its difference count equal to the number of tracks to go in the seek; this points the MPU to the correct tabulated velocity value which is stored in ROM. Second, for T<40 the +Integrator Clamp line goes active during cylinder pulses to clamp the sawtooth output of the Velocity Integrator to zero. Thus, the sawtooth waveform returns to zero each time that the D/A Converter gets a revised input (see Desired Velocity Generation discussion).

During a seek, the Position signal from the Tribit Decoder alternates between positive and negative values (see Servo Surface Decoding discussion). Each zero-crossing of the Position signal corresponds to a cylinder crossing. Figure 1-35 provides a simplified logic diagram and waveforms for this cir-

Figure 1-34. Desired Velocity Waveforms

COAST

|◄── ACCELERATION ──►| |◄─── DECELERATION ───►|

VELOCITY RAMP ❶

T=256   T=0

INVERTED VELOCITY RAMP ❷

T=40

+INTEGRATOR CLAMP ❸

0V

-VELOCITY ❹

INTEGRATED VELOCITY ❺

+DESIRED VELOCITY ❻

-FINE ENABLE ❼

NOTES:

⚠1. AFTER T=1, MPU LOOKS FOR THIS EDGE TO SWITCH SERVO TO FINE LOOP OPERATION.

2. NUMBERS ㉚ REFER TO SIGNALS ON DESIRED VELOCITY CIRCUIT DIAGRAM.

3. THESE WAVEFORMS APPLY TO LONG FORWARD SEEK.

10R134

CIRCUITRY

FROM
TRIBIT
DECODER
➊ -POSITION

INVERTER
(0314)

LEVEL
DETECTOR
➋ -CYL PEAK A

LEVEL
DETECTOR
➌ +CYL LOW A

LEVEL
DETECTOR
➍ -CYL PEAK B

LEVEL
DETECTOR
(0314)
➎ +CYL LOW B

DEMODULATOR
LOGIC CHIP

SWITCHING
LOGIC
(0310)

➏ -CYLINDER PULSES

TO PIA -2
AND PTM #2
COUNTER

WAVEFORMS

-POSITION
➊

-CYL PEAK A
➋

+CYL LOW A
➌

-CYL PEAK B
➍

+CYL LOW B
➎

-CYLINDER
PULSES
➏

11D69

Figure 1-35.   Cylinder Pulse Circuitry and Waveforms

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cuit. The cylinder pulse detector uses four level detectors in
conjunction with switching logic located in the Demodulator
Logic Chip. The two level detectors, designated "A", monitor
the +Position signal, and the two level detectors, designated
"B", monitor the -Position signal. Each level detector
switches its output signal at unique levels, based on its
thresholds and hysteresis. The "A" level detectors recognize
zero-crossings and position peaks of one polarity by activating
the +Cylinder Low A and the -Cylinder Peak A lines respec-
tively. Similarly, the "B" level detectors recognize zero-
crossings and position peaks of the other polarity by acti-
vating the +Cylinder Low B and the -Cylinder Peak B lines.

The four level detector outputs supply control signals to
switching logic in the Demodulator Logic Chip. In developing
the -Cylinder Pulses signal, this logic must sense a position
peak prior to responding to a position zero-crossing. Figure
1-35 shows how transitions in the four input signals produce
the changes in the -Cylinder Pulses signal. This design en-
sures that only one Cylinder Pulse is generated for each zero-
crossing of the Position signal.

Velocity Measurement

A continuous indication of actuator velocity is needed during
the coarse seek mode. The -Velocity signal is developed and
introduced to the coarse loop so that the servo loop can force
actual velocity to match desired velocity. The -Velocity sig-
nal is negative during a forward movement (positive during a
reverse movement), and its amplitude is proportional to veloc-
ity.

As part of the First Load operation, the MPU does a calibration
procedure (a series of 128-track seeks) where it adjusts the
gain of the velocity measurement circuit in order to compensate
for gain variations in the servo disk. The gain is adjustable
in steps depending on which combination of the four gain con-
trol lines is set. Upon finding the optimum combination of
settings, the MPU maintains that combination (output from
PIA-0) until another First Load operation is necessary.

Figure 1-36 is a simplified block diagram of the velocity mea-
surement circuits. Velocity measurement is a sequenced opera-
tion in which the switching control circuit selects different
signal inputs for the Velocity Signal Generator and determines
the operating mode of the Velocity Signal Generator.

Figure 1-36.   Velocity Measurement Circuits

The sequencing pattern repeats itself with every complete oscillation of the -Position signal. Each oscillation of the -Position signal has four distinct regions, as shown in figure 1-37. The positive peak region is followed by a linear region with constant falling slope. Then there is a negative peak region followed by a linear region with constant rising slope. The switching control circuit monitors the -Position signal with two level detectors, one that senses the positive peak region and another that senses the negative peak region. The peak detectors supply inputs, the -Negative Peak and -Positive Peak signals, to the switching control circuit (in the Sector Counter Gate Array) to define the regions of the -Position signal for it. Through control lines -Slope 1 and -Slope 2, the switching control circuit regulates the Velocity Signal Generator.

-POSITION ❶

+DIFFER-
ENTIATED
POSITION ❷

A

E

I

LINEAR REGIONS

-DIFFER
ENTIATED
POSITION ❸

C

G

K

-SLOPE 1
(ACTIVE LOW
CONTROL LINE) ❹

-SLOPE 2
(ACTIVE LOW
CONTROL LINE) ❺

△2

CURRENT ❻

B

D

F

H

J

OV

OV

-VELOCITY ❼

A

B

C

D

E

F

G

H

I

J

K

△1

NOTES:

△1 THE -VELOCITY SIGNAL IS
DEVELOPED FROM 3 SOURCES.
LETTERS A THRU K IDENTIFY
SOURCE FOR EACH REGION

△2 CONTROL LINE FOR FIRST
LINEAR REGION IS ACTIVATED
BY LATCH IN SECTOR COUNTER
GATE ARRAY

3 NUMBERS ㉚ REFER TO SIGNALS
ON VELOCITY MEASUREMENT
CIRCUIT DIAGRAM

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Figure 1-37. Velocity Measurement Waveforms

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In each sequence pattern, the switching control circuit activates one control line during one linear region and the other control line during the other linear region. During the linear regions, the differentiated position outputs are proportional to velocity because velocity is the time rate of position change. So during linear regions, the switching control circuit places the Velocity Signal Generator in the amplifying mode and selects the differentiated input of the proper polarity in each region. In the first linear region of the coarse seek (the first 1/2 track), the MPU presets a latch in the switching control logic with signals on the +D/A Bit 6, +D/A Bit 7, and -Forward lines. Through the rest of the seek, the circuit is self-running. The detected position signal peaks alternately set and clear the latch, and the latch alternately activates the two control lines in successive linear regions. The proper input polarity to the Velocity Signal Generator is a function of the latch state and the level of the -Forward line; this makes the -Velocity signal polarity match the seek direction.

When the -Position signal is in the peak regions and thus neither control line is active, the switching control circuit allows the Velocity Signal Generator to integrate its Current input. This fills in the gaps in the -Velocity signal at times when no differentiated position signal is available.

The Current signal is derived in the Power Amp Driver by amplifying Current Feedback sampled at the actuator. Any acceleration or deceleration of the actuator produced by the servo loop is proportional to this current. Velocity is the integral of acceleration; therefore, when the Velocity Signal Generator integrates the Current signal, it is deriving a velocity signal during Position signal peaks.

Summing Amp

The servo system operates, in each mode, to null the input to the summing amp. The MPU selects the signal input to the summing amp via PIA-1 by enabling one of two analog gates. In coarse loop operation, the +Coarse line is active, and velocity information is input to the Summing Amp. In fine loop operation, the -Settle In line is active and position information is input to the Summing Amp (see discussion of Fine Loop Operation).

The Summing Amp input in coarse loop operation is the sum of the +Desired Velocity and -Velocity signals. When measured velocity is equal to desired velocity, these signal inputs add

to zero, and -Notch Filtered Desired Current, the output of the Summing Amp, is zero. With unmatched inputs, the -Notch Filtered Desired Current line has a voltage level that indicates both the magnitude and the polarity of actuator current that will bring the servo system into balance. Zener diodes in the feedback path of the Summing Amp prevent amplifier saturation by keeping the output amplitude between -10 volts and +10 volts. When -Notch Filtered Desired Current is negative, the resulting actuator current will accelerate the heads in a forward seek or decelerate the heads in a reverse seek.

Power Amp Driver

The Power Amp Driver generates In Drive or Out Drive currents as inputs to the Power Amp in response to the voltage level on the -Notch Filtered Desired Current line from the Summing Amp. Together, the Power Amp Driver and the Power Amp make up a current feedback amplifier. Through a feedback loop that monitors actuator current, the Power Amp Driver adjusts the current in the In Drive line or the Out Drive line as necessary to produce the actuator current specified by the -Notch Filtered Desired Current signal. Figure 1-38 shows the Power Amp Driver in simplified form, and the following paragraphs provide a detailed description of its circuit operation.

The Current Sense signal, an analog voltage proportional to actuator current, is applied to an op amp which amplifies it to produce the +Current signal. The +Current signal is a positive voltage when the actuator exerts inward force and a negative voltage when the actuator exerts outward force. At a second op amp, the +Current and -Notch Filtered Desired Current signals are added, inverted and amplified to produce the +Current Error signal. The +Current Error signal is zero when the actuator current matches the desired current specified by the servo loop. A mismatch makes the +Current Error signal go positive or negative as required to bring the actuator current to the desired value. In this manner, the Power Amp Driver and Power Amp are a closed loop current amplifier.

The +Current Error signal is input to an analog gate which is enabled by the -Enable Power Amp signal. The -Enable Power Amp signal is latched in the Sector Counter Gate Array. Prior to starting the drive motor or loading the heads, the MPU pulses the +T$\leq$8 and -Forward lines to reset the latch and activate the enable. The latch is set to remove the enable either by the MPU (after a head retract) or by a voltage fault. In the case of a voltage fault, the servo remains disabled until the fault condition is cleared. With the analog gate enabled, the +Current Error signal is fed to the inputs of the In and Out Driver transistors.
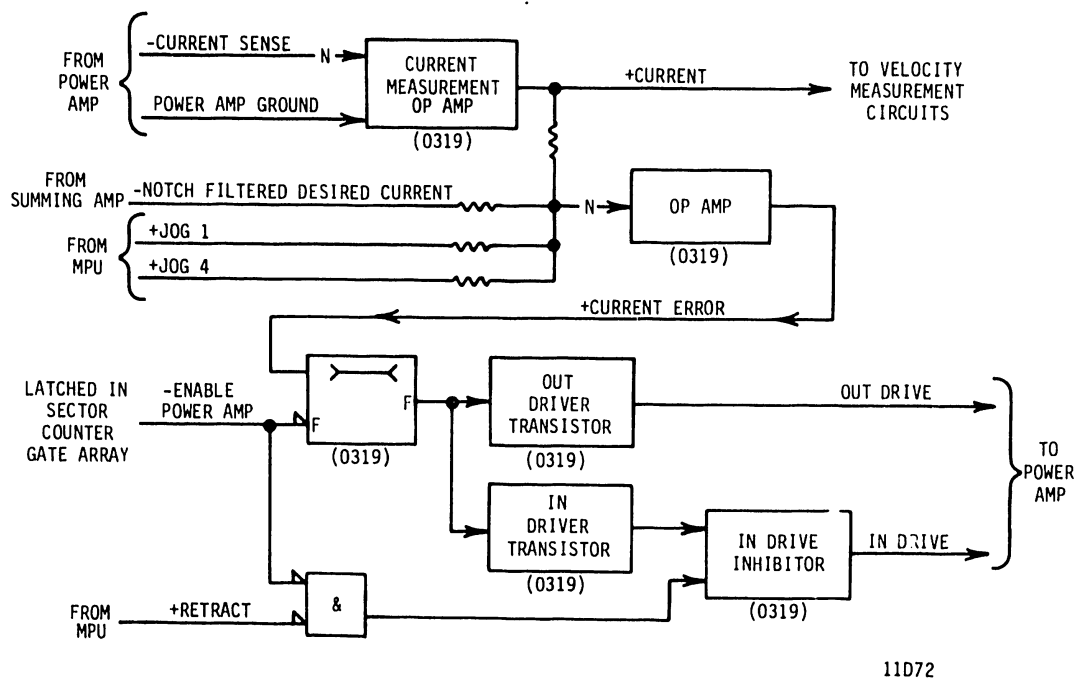
Figure 1-38. Power Amp Driver Circuitry

When the error voltage is positive, it cuts off the Out Driver transistor and regulates the current in the In Drive output line. When the error voltage is negative, it cuts off the In Driver transistor and regulates the current in the Out Drive output line. When the error voltage changes sign, it reverses the direction of actuator current, thereby reversing the force applied to the actuator.

The +Jog 1 and +Jog 4 inputs allow the MPU to move the heads slightly while the drive motor is being started. They supply a negative offset to the +Current Error signal, and the actuator is forced outward against its crash stop. In this way, contact between the heads and the landing zone portion of the disk is broken before the disks begin to rotate. During normal servo operation, the MPU keeps the jog inputs inactive.

Power Amp

The Power Amp, acting on inputs from the Power Amp Driver, produces the actuator current required by the servo loop. Figure 1-39 is a simplified drawing of the Power Amp circuitry.

When positive actuator current is required, the Power Amp Driver generates current in the In Drive line. The In Direction Amplifier amplifies this input current and regulates (positive) current flow from ground through the sampling resistor and the actuator coil to -24 V. The negative voltage on the Current Sense line is supplied to the Power Amp Drive to complete the loop regulating the amplifier (see discussion of Power Amp Driver). In direction actuator current forces the actuator to accelerate during a forward move and to decelerate during a reverse move.

When negative actuator current is required, the Power Amp Driver generates current in the Out Drive line. The Out Direction Amplifier amplifies this input current and regulates (positive) current flow from +24 V through the actuator coil and the sampling resistor to ground. In this case, the voltage on the Current Sense line is positive. Out direction actuator current forces the actuator to accelerate during a reverse move and to decelerate during a forward move.

During retract operations, the Retract Power Amplifier regulates actuator current. This operation is discussed under Retract Control Circuitry.

Fine Loop Operation

General

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek. Figure 1-40 is a simplified block diagram of the fine loop circuitry. Discussion of the fine loop is presented in the following topics:

- Position Error Generation

- Fine Loop Actuator Movement

Figure 1-39.   Power Amp Circuitry
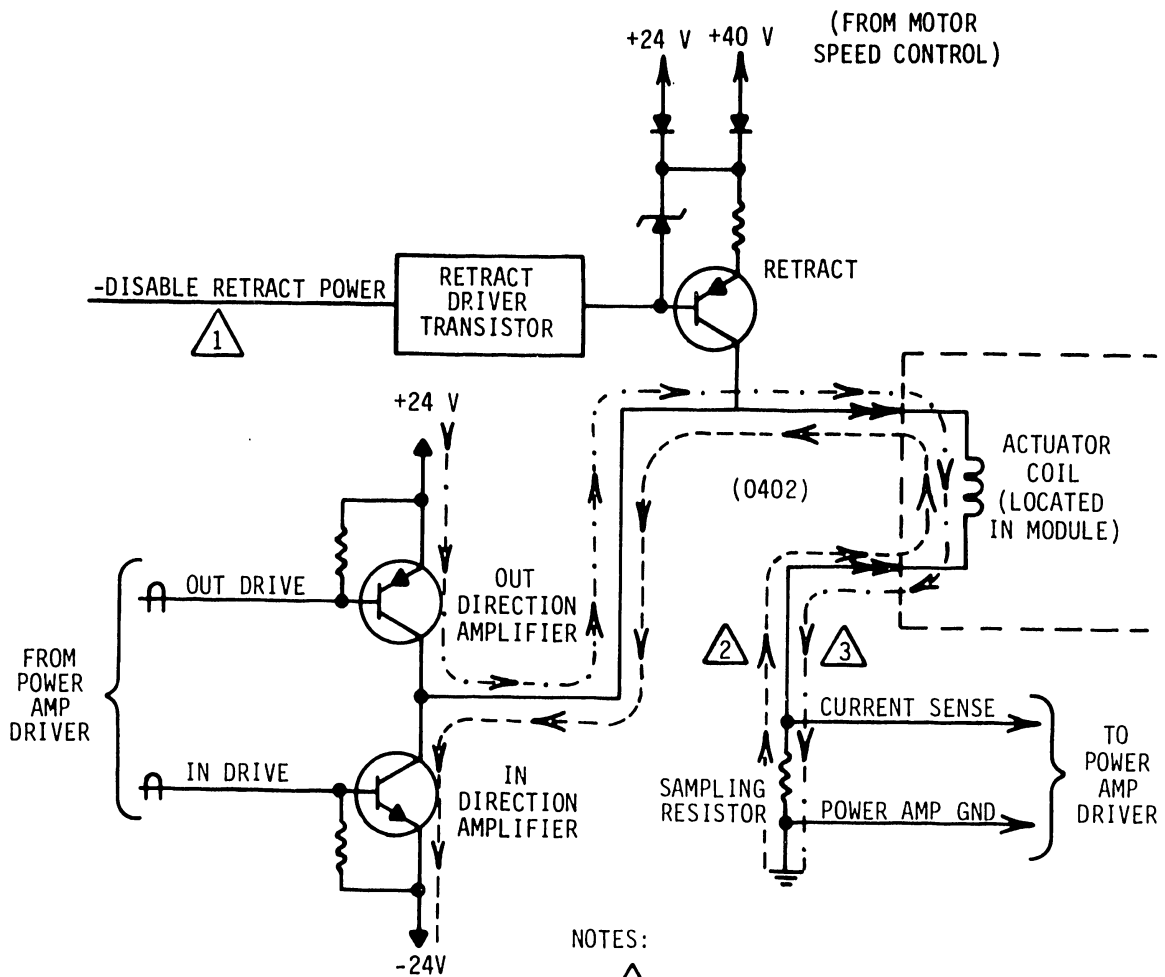
NOTES:

1. ..IGH IF +LOW VCC OR IF +RETRACT IS HIGH.

2. ———◄— SHOWS FLOW OF (POSITIVE) IN DIRECTION CURRENT

3. —►—·— SHOWS FLOW OF (POSITIVE) OUT DIRECTION CURRENT

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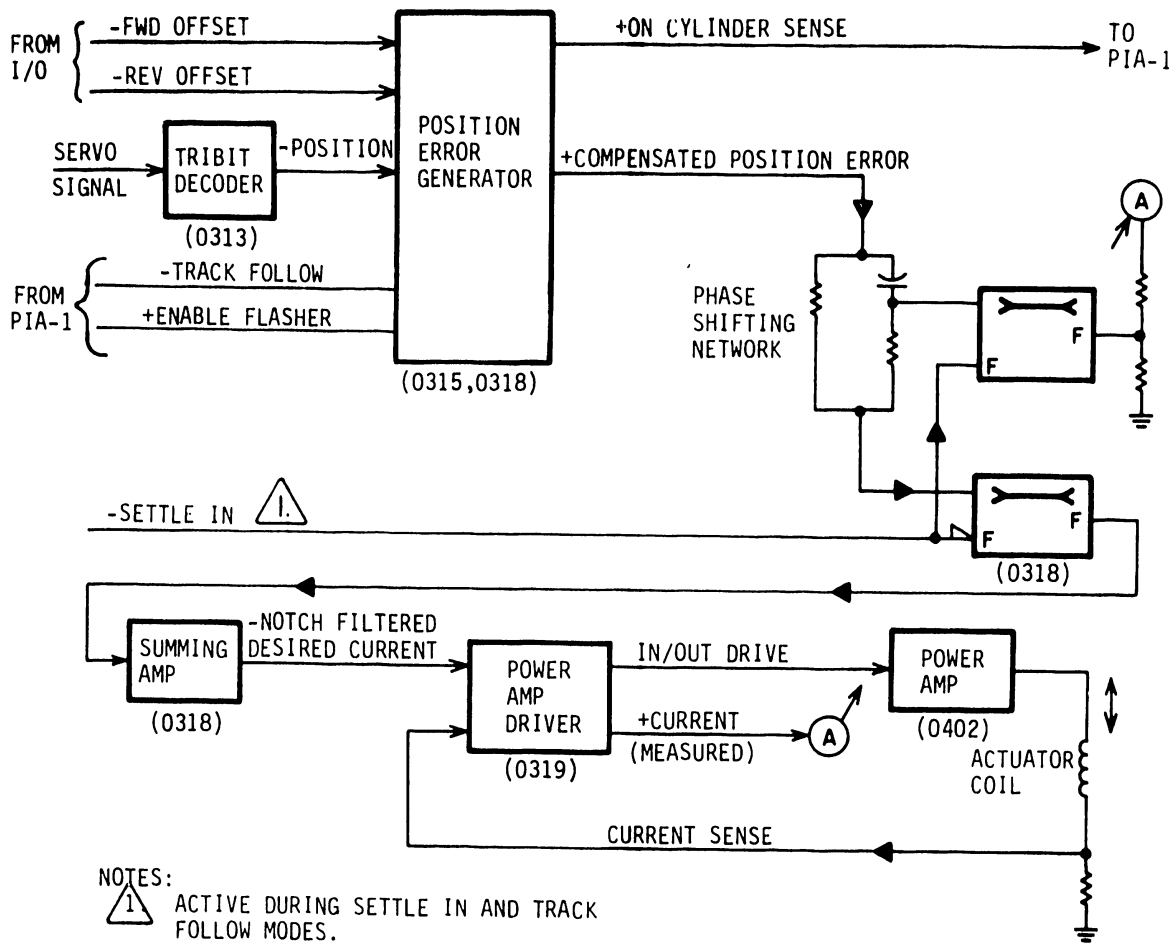
Figure 1-40. Fine Loop Block Diagram

Position Error Generation

In fine loop operation, the servo system adjusts the position
of the actuator to null the input signal to the Summing Amp.
The Summing Amp input developed for fine loop operation is dif-
ferent for settle in and for track-following modes. However,
both of these error signals basically derive from the +Position
signal from the Tribit Decoder.

At the start of a seek, the MPU sets or clears the +Slope input
to the Tribit Decoder to ensure that +Position goes positive as
the heads move inward and negative as the heads move outward
from their destination track. The +Position signal is zero

with the heads exactly on track. This relationship is true for every destination track on the disk. Thus, with some modification, +Position is a suitable error signal for the Summing Amp in the fine loop. The modification takes into account the following considerations:

- Stability of fine servo loop -- requires the addition of a differentiated correction to the error signal.

- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.

- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

Figure 1-41 shows the position error circuitry in simplified form.

The position error circuitry consists of two op amps and a level detector. The first op amp inverts -Position and applies it with an optional offset to the second inverting op amp and
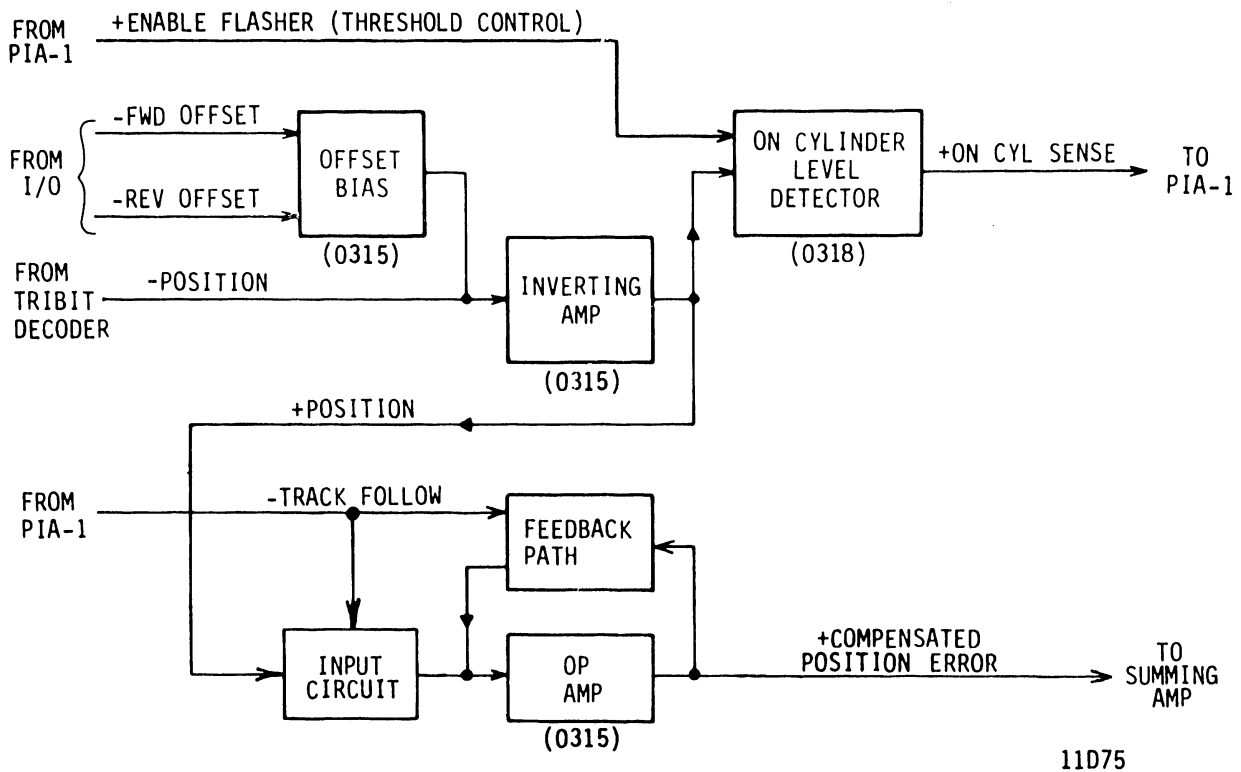
Figure 1-41. Position Error Circuitry

the level detector. An offset, a dc shift of the position signal, results when the controller issues a Servo Offset command in order to recover marginal read data. When the I/O Gate Array decodes Servo Offset Plus (Tag 3 and Bus bit 2), it activates -FWD Offset, and the Offset Bias circuit shifts the position signal about 0.75 V negative. When the I/O Gate Array decodes Servo Offset Minus (Tag 3 and Bus bit 3), it activates -REV Offset, and the Offset Bias circuit shifts the position signal about 0.75 V positive. Servo Offset Plus displaces the heads inward from track center.

The +Position signal from the first op amp inputs both the On Cylinder level detector and the second op amp. The second op amp develops the +Compensated Position Error signal which is used as an error signal for both the settle-in and track-following modes. This op amp has an analog gate in its feedback path that makes it operation different in settle-in mode than it is in track-following mode.

For both settle-in and track-following, the +Compensated Position Error signal passes through a phase-shifting network before being applied to the Summing Amp input. This network, shown in figure 1-40, consists of a resistor which is in parallel with a series-RC differentiator. Adding a differentiated component to the error signal improves the stability of the fine servo loop. Prior to settle-in (T>1/2 track), an analog gate presets the capacitor charge by sampling the +Current signal to permit a smooth transition from the coarse to the settle-in mode. When -Settle-In goes active, it disables that analog gate, allowing the phase-shifting network to operate. A second analog gate is switched on to pass the error signal on to the Summing Amp input.

The MPU allows 0.8 ms for settle-in before switching to the track-following mode. In the track-following mode, the servo maintains the heads on cylinder until a new seek command appears. When -Track Follow goes active, an analog gate modifies the input circuit and feedback path for the second op amp in the position error circuitry. This change increases the low-frequency gain of that amplifier to provide tighter servo control in track-following.

The On Cylinder Sense level detector informs the MPU when to set the On Cylinder FF (in the track-following mode). The detector has two thresholds, controlled by the +Enable Flasher line from PIA-1. Prior to settle-in, the MPU activates the +Enable Flasher line, making the detector circuit sensitive to any settle-in problems. When the position signal drops to the

threshold level of the detector, the detector activates the +On Cylinder Sense signal to generate an interrupt via PIA-1. Once the +On Cylinder Sense signal is steadily active, the MPU responds to this interrupt by issuing On Cylinder status to the I/O Gate Array. With the heads on cylinder, the MPU drops the +Enable Flasher signal to make the On Cylinder Sense level detector less sensitive to changes in the position signal.

Thus, the Summing Amp receives a different input in each seek mode. Response of the servo circuitry to the Summing Amp input is summarized in the next topic.

Fine Loop Actuator Movement

In the fine loop, as in the coarse loop, the Summing Amp develops the -Notch Filtered Desired Current signal in response to its input error signal. The Power Amp Driver and Power Amp, acting as a current feedback amplifier, develop current in the actuator to match the -Notch Filtered Desired Current input signal. This actuator current moves the heads toward track center. As the heads move toward track center, the position error signal goes to zero. The loop is balanced when the heads are at track center and the Summing Amp input is nulled. With a positive Summing Amp input, -Notch Filtered Desired Current is negative; this results in positive actuator current and inward force on the heads.

For details about this circuit operation, refer to the following topics presented under Coarse Loop Operation:

- Summing Amp

- Power Amp Driver

- Power Amp

Retract Control Circuitry

The retract control circuitry moves the actuator outward until the heads are located in the landing zone. As shown in figure 1-42, the -Disable Retract Power signal determines whether the retract control circuitry is operating. When the signal is high, the retract amplifier is cut off. When the signal is low, the retract amplifier acts as a source of out direction current. The amplifier is connected to two voltage supplies -- +24 Vdc from the power supply and the voltage generated by the decelerating drive motor. The amplifier develops actuator current from the supply with the highest potential.

The retract amplifier is biased into operation either when the MPU issues the Retract command or when the +5 Vdc supply voltage drops enough to activate the +Low Vcc signal. The MPU uses the Retract command for normal head unloading before powering down the spindle or if it detects low drive motor speed.

Conditions that enable the retract amplifier also inhibit the In Drive current from the Power Amp Driver. The In Drive Inhibitor is activated if either the +Retract line or the -Enable Power Amp line goes high. The second signal automatically goes high if a voltage fault occurs. Cutting off the In Direction Amplifier ensures that the retract actuator current will be unopposed by in direction current in the power amplifier.
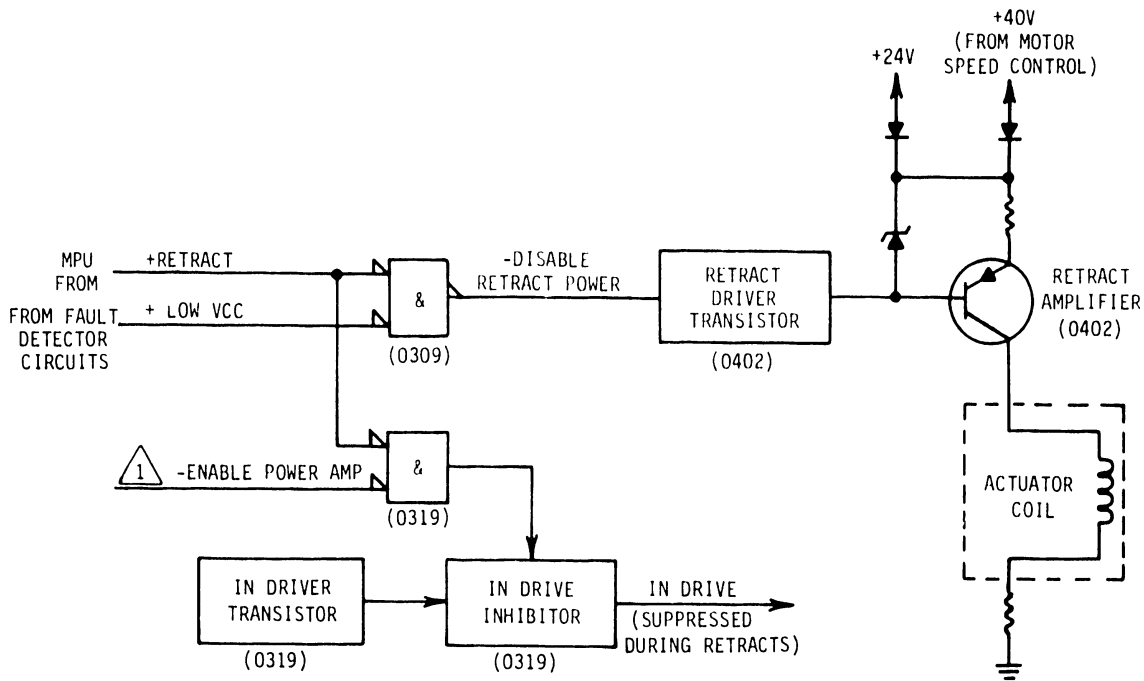
Figure 1-42. Retract Circuitry Block Diagram

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Load Control Circuitry

Loading the heads consists of moving them inward from the land-
ing zone to the data zone. In this process, the MPU controls
the force exerted by the actuator. The force is produced by
actuator current pulses, generated by the load control cir-
cuitry. As shown in figure 1-43, the load control circuitry
uses portions of the coarse servo loop. Unlike coarse servo
control, which feeds back measured velocity in the servo loop,
load control is accomplished without servo feedback.

Figure 1-43 shows the MPU inputs to the load control cir-
cuitry. Throughout the process, the MPU holds +D/A Bits 0-7
active to establish the amplitude of the current pulses, and,
except for the final current pulse, it holds the -Forward line
active. The desired velocity generator supplies a constant
bias on the +Desired Velocity line. By switching the +Coarse
signal on and off, the MPU causes the bias on the +Desired Vel-
ocity line to be applied as pulses to the summing amp. The
power amp driver and power amp develop pulses of actuator cur-
rent in response.

Following its program, the MPU begins the load with a long
pulse to start the actuator moving, followed by a series of
shorter pulses to sustain that motion. While generating the
shorter pulses, the MPU monitors the -Demodulator Active line.
As the heads move out of the landing zone, the Tribit signal is
detected. When the tribit decoder becomes synchronized, it
issues the -Demodulator Active signal. The MPU allows a 40 ms
delay and then counts 100 cylinder pulses to verify that the
tribit decoder is reliable. At this point, the MPU switches
the -Forward line high and creates a long pulse of out direc-
tion actuator current to stop the actuator motion.
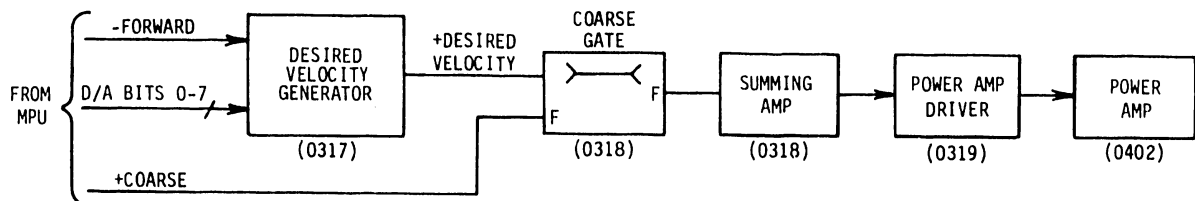
Figure 1-43. Load Circuitry Block Diagram

TYPES OF SEEKS

General

The drive has four basic types of seeks: the load operation, normal seek, return to zero (RTZ) seek, and unload operation. The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The unload operation is an outward movement that moves the heads to the landing zone beyond the outer guard band. Normal seek operations can be either inward or outward movements, depending upon where the new address is located relative to the present address. The four basic seek operations are discussed in the following text.

Load Operation

The load operation is an MPU-controlled sequence that starts the drive motor, moves the heads from the retracted position to track 0, and calibrates the velocity measurement circuitry. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion for details about power on initialization. The load operation is described in the following paragraphs and is flow-charted in figure 1-44.

When power on initialization is complete, the MPU ensures the +Fan Fault line is inactive and waits for start conditions before initiating the load operation. The MPU requires that the START switch is placed in the Start position and (in remote operation) that Sequence Pick and Sequence Hold are available from the controller. Once Sequence Pick is received, a delay circuit in the I/O circuitry activates +Start Enable after an interval equal to five seconds multiplied by the drive address.

With start conditions present, the MPU starts the drive motor. During the first three seconds of motor acceleration, the MPU causes the actuator to move outward against the soft carriage stop. During this motion, called a jog, the heads begin flying over the landing zone. Prior to the jog, the MPU pulses the -Forward and $+T \leq 8$ lines to latch the +Enable Power Amp signal coming from the Sector Counter Gate Array. In addition, the MPU issues the Unlock Actuator command via PIA-1. The MPU controls the jog current by activating the +Jog 1 and +Jog 4 lines to the power amp driver.

Figure 1-44. Load Operation Flowchart (Sheet 1 of 4)

NOTES:

△1 SEE POWER ON FLOWCHART UNDER SEEK FUNCTIONS

△2 WHILE +JOG 4 LINE IS ACTIVE, MPU SWITCHES +LOW/-HIGH START CURRENT LINE HIGH TO LIMIT CURRENT DRAIN ON 40 V SUPPLY

11D78-1

FROM
SHT 1

A

MPU CHECKS MOTOR
SPEED WITH PTM#3
COUNTER

(0307)

IS
MOTOR SPEED
WITHIN LIMITS? →NO

YES

AFTER 10 SECOND DELAY
MPU INITIALIZES GAIN
CONTROL LINES FOR VEL-
OCITY MEASUREMENT

(0305)

IS
+FAULT
LINE ACTIVE? →YES→ TO
SHT 4
B

(0306)
NO

IS
-DEMODULATOR
ACTIVE SIGNAL
HIGH PRIOR TO
LOAD? (0306) →NO→ TO
SHT 4
B

YES

MPU LATCHES THE
+ENABLE POWER AMP
SIGNAL IN SECTOR
COUNTER GATE ARRAY

(0309)

IS
+FAULT LINE
ACTIVE? →YES→ TO
SHT 4
B

(0306)
NO

MPU ISSUES
UNLOCK ACTUATOR
COMMAND   1

(0306)

1 → MPU STARTS A 200ms
       TIMEOUT IN PTM#3
       FOR COMPLETION OF
       FORWARD MOVE

(0307)

MPU ACTIVATES D/A
BITS 0-7 AND
FORWARD LINE

(0306,0307)

MPU PULSES THE
+COARSE LINE TO
DEVELOP ACTUATOR
CURRENT PULSES

(0306)

PULSES CONTINUE
UNTIL -DEMODULATOR
ACTIVE SIGNAL
GOES LOW

(0306)

AFTER A 40 ms
DELAY, PTM #2
COUNTER COUNTS
100 CYLINDER PULSES

(0307)

DID
200 ms
TIMEOUT ELAPSE
YET? →YES→ TO
SHT 4
B

NO

MPU DEVELOPS A
CURRENT PULSE
TO DECELERATE
ACTUATOR

IS
+FAULT LINE
ACTIVE? →YES→ TO
SHT 4
B

(0306)
NO

2

2 → MPU ALLOWS
       ACTUATOR TO COAST
       UNTIL VELOCITY
       DROPS TO 2 IPS

MPU MAKES +COARSE
LINE HIGH AND
-FORWARD LINE HIGH

(0306)

MPU INPUTS
CONSTANT VELOCITY
VIA D/A BITS 0-7

(0307)

ACTUATOR MAKES
A SLOW REVERSE
MOVE

ARE
PULSES DETECTED
ON OUTER GUARD
BAND LINE? →NO
(0306)

YES

MPU REDUCES
D/A INPUT

(0307)

ACTUATOR CON-
TINUES REVERSE
MOVE AT SLOWER
VELOCITY

C TO
   SHT 3

11D78-2A

Figure 1-44.   Load Operation Flowchart (Sheet 2)

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Figure 1-44. Load Operation Flowchart (Sheet 3)

FROM
SHT 3

(D)

WERE
3 OR MORE
ADDITIONAL CYL-
INDER PULSES
COUNTED? —— YES ——→

NO,

DID
-DEMODULATOR
ACTIVE STAY
LOW? —— NO ——→

(0306)

YES

HEADS ARE
POSITIONED AT
TRACK ZERO

MPU
PERFORMS
SCAN CYCLE

MPU PERFORMS
VELOCITY CALI-
BRATION PROCEDURE

WAS
LOAD OPERATION —— NO ——→ (1)
SUCCESSFUL

YES

HEADS ARE
POSITIONED AT
TRACK ZERO

MPU SWITCHES
+ENABLE FLASHER
LINE LOW AND ——→ (2)
-READY LINE LOW

FROM
SHTS 2 & 3

(B)

(1) ——→

MPU SETS
FIRST SEEK
FAULT LATCH

MPU COMMANDS
NORMAL RETRACT

(0306)

MPU LOCKS
ACTUATOR IN
RETRACT
POSITION

MPU INDICATES
SERVO STATUS CODE
ON FAULT DISPLAY
BOARD

FAULT
CLEAR SWITCH
ON OPERATOR PANEL —— NO
PRESSED

YES

MPU INITIATES
ANOTHER LOAD
ATTEMPT

(2)

UNIT READY
SENT TO
CONTROLLER

OPERATOR PANEL
READY LIGHT
ON STEADY

MPU SETS ON
CYLINDER FF, ON
CYLINDER & SEEK
END SENT TO
CONTROLLER

DRIVE NOW READY
TO RESPOND
TO CONTROLLER
COMMANDS

11D78-4A

Figure 1-44. Load Operation Flowchart (Sheet 4)

1-96

83324770 B

The MPU starts the drive motor by issuing the Motor Run command to the motor speed control (via PIA-1) and requires that the +Speed OK line from the Motor Speed Control goes high after a delay from 3 to 25 seconds. Operation of the motor speed control and drive motor is discussed under Electromechanical Functions. With Speed OK, the MPU doublechecks motor speed by counting -Motor Sensor pulses entering the programmable timer (PTM #3). The MPU continues to check motor speed until the speed is between 3564 and 3636 r/min.

Prior to loading the heads, the MPU initializes the Gain Control lines for the velocity measurement circuitry. (These lines are calibrated later in the load operation.) Also, the MPU ensures that the +Fault line is inactive and that -Demodulator Active line is high. Because the landing zone is located beyond the outer guard band, the heads must move forward before a servo signal is detected.

To start the heads moving inward, the MPU latches the +Enable Power Amp signal in the Sector Counter Gate Array and unlocks the actuator. As discussed under Load Control Circuitry, the MPU develops current pulses that force the actuator to move forward from the landing zone. Figure 1-45 shows the carriage trajectory during the load seek. Once the -Demodulator Active signal goes low, indicating that the tribit decoder has locked in the servo signal, the MPU stops issuing current pulses, delays 40 ms, and begins counting cylinder pulses using the programmable timer (PTM #2). After counting 100 cylinder pulses, the MPU uses the load control circuitry to develop a decelerating current pulse.

At this point, the actuator is floating freely over the data zone. Throughout the forward move, the MPU uses a timer to ensure that the move is complete within 200 ms. If the timeout occurred or if the +Fault line went active during the move, the MPU sets the First Seek latch in the I/O Gate Array and lights the front panel FAULT indicator.

After waiting for the actuator velocity to drop to two inches per second, the MPU uses the coarse servo loop to move the heads outward into the outer guard band. To do this, the MPU switches the +Coarse line high and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

Once the heads reach the outer guard band, the MPU reduces the D/A input, and the actuator continues to move outward at reduced velocity. The MPU verifies that the -Demodulator Active signal remains low, and it uses the programmable timer (PTM #2) to monitor cylinder pulses.
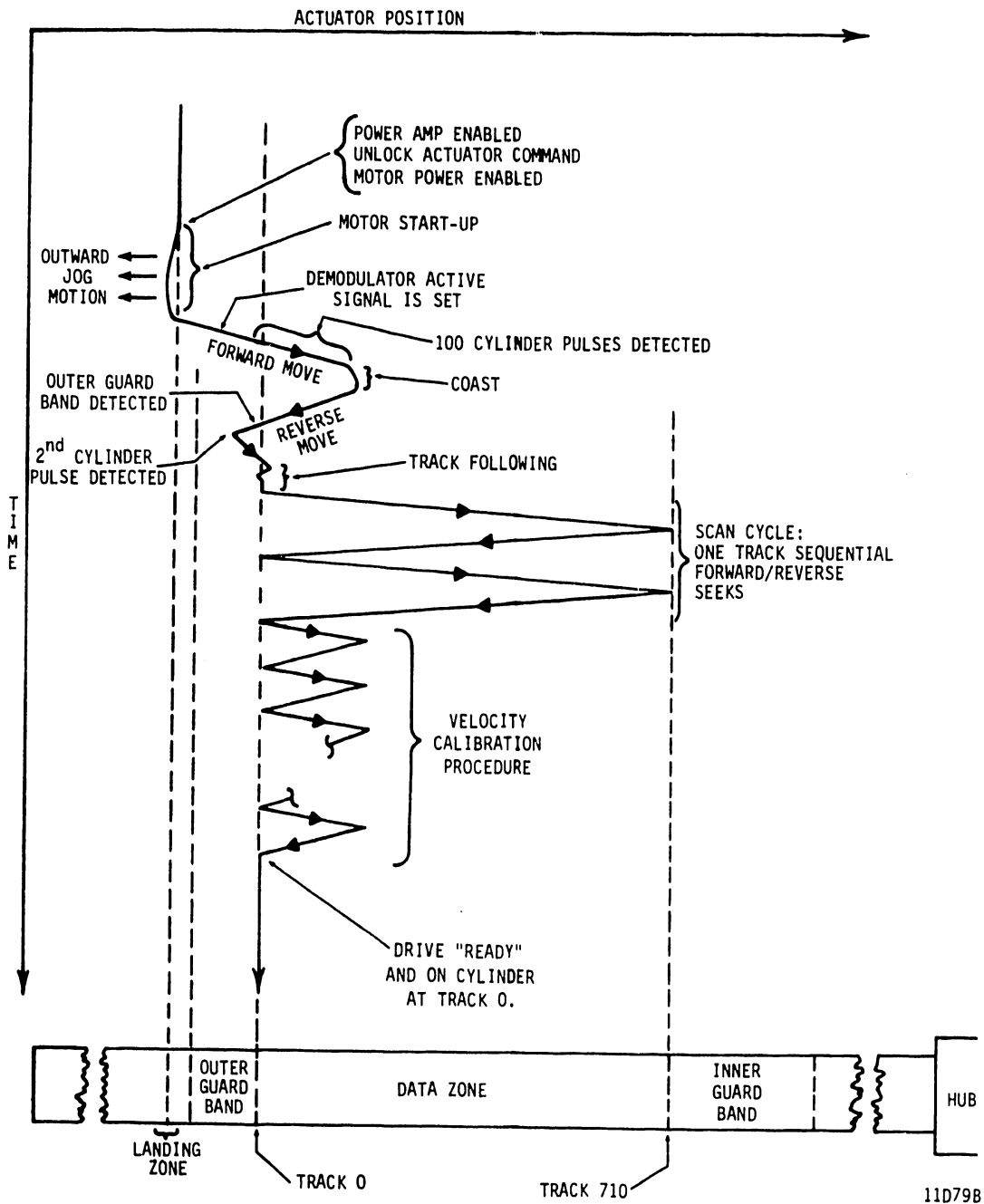
Figure 1-45. Load Seek Trajectory

When PTM #2 has counted the two cylinder pulses for this move, it interrupts the MPU. The MPU reacts by issuing the Forward command to make the heads seek inward. The MPU requires that one cylinder pulse appears before the Outer Guard Band signal goes inactive (or it sets the First Seek fault latch). After the Outer Guard Band signal goes inactive, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T≤8 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond timeout to ensure that the actuator has settled on track. During this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the First Seek fault latch and terminates the load operation.

When On Cylinder Sense has stayed active for 2.1 milliseconds, the MPU ensures that -Demodulator Active is still low (indicating a reliable servo signal) prior to performing the scan cycle and the velocity calibration procedure. In the scan cycle, the MPU commands two seek sequences. Each sequence consists of forward one-track seeks starting at track 0 and ending at track 710, followed by reverse one-track seeks, starting at track 710 and ending at track 0. The velocity calibration procedure follows the scan cycle.

In the velocity calibration procedure, the MPU commands a series of 128-track normal seeks where it adjusts the gain of the velocity measurement circuit in order to compensate for

gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the four gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until the first load operation is repeated.

With the velocity calibration procedure complete, the heads are positioned at track 0. If the load operation was successful, the MPU issues the -Ready signal at PIA-2 and clears the +Enable Flasher signal at PIA-1. With -Ready low, the front panel Ready indicator lights, and Unit Ready status appears on the interface. Also, by inactivating the +Enable Flasher line, the MPU reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array, causing On Cylinder and Seek End status to appear on the interface. The MPU then waits for further instructions from the controller.

If the load operation was unsuccessful, the MPU performs a normal retract, provides a servo status code on the fault display board, sets the First Seek fault latch, and lights the front panel FAULT indicator. This fault can be cleared only by operation of the Fault Clear switch. Pressing the Fault Clear switch initiates another load attempt with a maximum of three tries allowed by the MPU.

Normal Seek

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero track seek requires no actuator movement and the operation is handled by the I/O Gate Array.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an out direction movement of the actuator, while going from a lower-numbered track to a higher-numbered one involves an in movement. Figure 1-46 is a detailed flowchart showing the normal seek operation.

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by raising the Tag 1 (Cylinder Select) signal and placing the desired cylinder address on the Bus bits 0 through 9. The address is gated into the Cylinder Address register (in the I/O Gate Array) by the Cylinder Select Tag.

START

UNIT SELECTED AND ENABLED? — NO

YES

CONTROLLER OUTPUTS TAG 1 WITH CYLINDER ADDRESS ON BUS BITS 0-9
(0206)

IS NEW CYLINDER ADDRESS SAME AS OLD ADDRESS? — YES → ON CYLINDER FF STAYS SET. ON CYLINDER & SEEK END DISABLED ON I/O FOR 30µs (0206)

NO

ON CYLINDER FF CLEARED
(0206)

SEEK INTERRUPT SENT TO PIA-0
(0305)

MPU PULSES I/O CONTROL LINES 1 & 2 TO READ NEW CYLINDER ADDRESS
(0206)

CYLINDER ADDRESS TRANSFERRED IN 4-BIT GROUPS VIA HEAD/CYL ADDRESS LINES 0-3
(0206)

MPU PULSES I/O CONTROL LINES 1 & 2 TO PLACE HEAD ADDRESS ON HEAD/CYL LINES
(0206) → 1

1 → MPU CHECKS WHETHER NEW CYLINDER ADDRESS IS LEGAL (0-710)

IS NEW ADDRESS LEGAL? — NO → TO SHT 5 B

YES

MPU COMPARES NEW ADDRESS WITH PRESENT ADDRESS TO CALCULATE T=TRACKS TO GO AND SEEK DIRECTION

MPU SWITCHES -FORWARD LINE LOW FOR FORWARD OR HIGH FOR REVERSE SEEK
(0306)

MPU SETS OR CLEARS +SLOPE LINE TO TRIBIT DECODER
(0306)

MPU PRESETS VELOCITY CIRCUIT VIA D/A BITS 6 & 7
(0309)

MPU SWITCHES +COARSE & -TRACK FOLLOW LINES HIGH
(0306)

IS +FAULT LINE LOW? — NO → TO SHT 5 B
(0306)

YES

IS -DEMODULATOR ACTIVE LINE LOW? — NO → TO SHT 5 B
(0306)

YES

IS +SPEED OK LINE HIGH? — NO → TO SHT 5 B
(0306)

YES → TO SHT 2 A

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Figure 1-46. Normal Seek Flowchart (Sheet 1 of 5)

83324770 A

1-101

FROM
SHT 1
A

1

MPU STARTS A 60 ms
TIMEOUT IN PTM #3
FOR COMPLETION OF
SEEK
(0307)

MPU CONTINUES
TO INCREMENT
D/A COUNT
(0317)

IS
SEEK A
ONE-TRACK
SEEK?

NO

MPU SWITCHES
T≤8 LINE LOW
AND +INTEGRATOR
CLAMP LINE HIGH
(0305)

ACTUATOR
CONTINUES TO
ACCELERATE

YES

MPU CLEARS +INTE-
GRATOR CLAMP LINE
TO ENABLE
VELOCITY INTEGRATOR
(0317)

MPU STARTS BUILDING
ACCELERATING VELO-
CITY RAMP BY INCRE-
MENTING D/A BIT LINES
(0317)

AT TRACK CROSS-
ING, CYLINDER
PULSE IS
GENERATED
(0310)

CYLINDER PULSE
DECREMENTS
PTM #2 COUNTER
(0307)

MPU SWITCHES
+T=1 AND +T≤8
LINES HIGH
(0305)

ACTUATOR BEGINS
ACCELERATION

CYLINDER PULSE
INTERRUPTS
MPU AT PIA-2
(0307)

MPU BUILDS ACCEL-
ERATING VELOCITY
RAMP: 16 ONE-BIT
INCREMENTS TO
D/A BIT LINES
(0317)

1/3 TRACK INTO
SEEK, MPU LOADS
T INTO PTM #2
COUNTER
(0307)

MPU COMPARES BUILT
UP VALUE OF D/A
COUNT WITH TABUL-
ATED VALUE FOUND
IN ROM
(0304)

HEADS MOVE
UNDER CONTROL
OF ACCELERATING
DESIRED VELOCITY
SIGNAL

1

IS
BUILT UP VALUE
>TABULATED
VALUE?

NO

1

MPU HOLDS D/A
BITS CONSTANT.
INTEGRATED VELO-
CITY REDUCES
DESIRED VELOCITY
(0317)

YES

ACCELERATION
PHASE ENDS

IS
T>256?

NO

D

TO
SHT 3

HEADS MOVE
UNDER CONTROL OF
DECELERATING
DESIRED VELOCITY
SIGNAL

MPU MAKES
+ENABLE FLASHER
LINE HIGH
(0306)

TO
SHT 5

C

YES

COAST PHASE
BEGINS

E

TO
SHT 3

11D80-2

Figure 1-46.   Normal Seek Flowchart (Sheet 2)

Figure 1-46. Normal Seek Flowchart (Sheet 3)

11D80-3

FROM
SHT 3
F

① → IS T>8? —NO→ MPU SETS +T≤8 LINE —→ ② ← IS T=1? —YES→ MPU SWITCHES +T=1 LINE HIGH —→ MPU MONITORS -FINE ENABLE LINE

(0305)

(0305)

(0307)

Left column (YES from IS T>8?):

MPU READS T FROM PTM #2, DECREMENTS T AND REFERENCES ROM TABLE FOR NEXT VELOCITY VALUE (0304)

ACTUATOR MOTION CONTINUES

AT TRACK CROSS-ING, CYLINDER PULSE IS GENERATED (0310) → CYLINDER PULSE DECREMENTS PTM #2 COUNTER (0307)

CYLINDER PULSE INTERRUPTS MPU AT PIA-2 (0307) → MPU PULSES +INTEGRATOR CLAMP LINE (0305)

MPU PUTS REVISED VELOCITY VALUE ON D/A BITS 0-7 (0317)

→ ①

Middle column (NO from IS T=1?):

MPU READS T FROM PTM #2, DECREMENTS T AND REFERENCES ROM TABLE FOR NEXT VELOCITY VALUE (0304)

ACTUATOR MOTION CONTINUES

AT TRACK CROSS-ING, CYLINDER PULSE IS GENERATED (0310) → CYLINDER PULSE DECREMENTS PTM #2 COUNTER (0307)

CYLINDER PULSE INTERRUPTS MPU AT PIA-2 (0307) → MPU PULSES +INTEGRATOR CLAMP LINE (0305)

MPU PUTS REVISED VELOCITY VALUE ON D/A BITS 0-7 (0317)

→ ②

Right column:

MPU MAKES +ENABLE FLASHER LINE HIGH (0306)

C
TO
SHT 5

11D80-4

Figure 1-46.   Normal Seek Flowchart (Sheet 4)

83324770 A

Figure 1-46. Normal Seek Flowchart (Sheet 5)

11D80-5

Inside the I/O Gate Array several processes take place. If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the On Cylinder line remains set and no Seek Interrupt is enabled to PIA-0. If a new seek command requires a seek to a different seek address, however, the Cylinder Select tag clears the On Cylinder FF and triggers a one-shot that sends Seek Interrupt to PIA-0. The MPU responds to this interrupt by initiating a seek routine.

The MPU transfers the destination cylinder address from the I/O Gate Array into its internal RAM via PIA-0 by pulsing the I/O Control 1 and 2 lines. These control lines operate a multiplexer in the gate array to place the address, four bits at a time, on Head/Cylinder Address lines 0-3. After reading the cylinder address, the MPU pulses the control lines to cause the Head Address to be multiplexed onto Head/Cylinder Address lines 0-4.

Prior to starting a seek operation, the MPU checks the new cylinder address supplied by the controller. If the MPU identifies an illegal address (greater than track 710), a Seek Error is declared.

The seek operation from this point until the on cylinder condition is achieved is under the control of the MPU programming. The program compares the new address with the present address (stored in RAM memory) to calculate the difference between the two (T=tracks to go) and the direction of the move (in or out).

In all seeks, the MPU presets certain signal lines to condition the coarse servo loop. The -Forward line is switched low for in direction seeks or high for out direction seeks. The MPU initializes the velocity measurement circuit by setting or clearing a latch in the Sector Counter Gate Array. To do this, the MPU supplies inputs via the D/A Bit 6, D/A Bit 7, and -Forward signals. The MPU checks to make sure that there is no fault condition and that the Demodulator Active and Speed OK signals are active.

If these conditions are met, the MPU loads the programmable timer (PTM #3) with a 60 millisecond timeout count (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout). The MPU sets or clears the +Slope line to the tribit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track. The MPU then starts the seek by making the -Track Follow and the +Coarse lines high and by introducing an accelerating velocity profile to the Desired Velocity circuit.

The remaining coarse seek is very different for one-track seeks than it is for longer seeks. For one-track seeks, the MPU

clears the +Integrator Clamp line, allowing the Velocity Integrator to generate the Integrated Velocity signal. The MPU also sets the T=1 and the T≤8 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal, and it builds an accelerating velocity profile by incrementing the D/A bits input to the D/A Converter one bit at a time.

After 16 increments, the MPU holds the D/A input constant, and a decelerating velocity profile results as the Integrated Velocity signal ramps up. The Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal to bring the Desired Velocity signal toward zero. The MPU monitors the -Fine Enable line, and it switches from coarse to fine loop operation when -Fine Enable goes low.

For seeks greater than one track, a different coarse seek sequence is managed by the MPU. The MPU builds an accelerating velocity ramp by incrementing the D/A bits entering the D/A Converter every 43 microseconds. At approximately 1/3 of a track into the seek, the MPU loads T, the number of tracks to go, into the programmable timer (PTM #2). (A cylinder pulse, generated as the heads cross each track, decrements PTM #2 directly to keep the count T current.)

The MPU continues to increment the D/A bit count, building up the velocity profile, until deceleration conditions are reached. This happens when the D/A count reaches the value specified in the PROM velocity table for the current value of T. For the remainder of the coarse seek, the MPU controls the D/A count based upon the velocity table. For long seeks, the D/A count stays at maximum (all bits set) and the carriage coasts at full velocity prior to actual deceleration.

Throughout the deceleration portion of the coarse seek, the MPU updates the D/A count at each cylinder crossing and activates the velocity integrator circuit once T<40. The MPU clamps integrated velocity to zero by pulsing the +Integrator Clamp line at each cylinder crossing and adjusts the level of the Integrated Velocity signal by means of four control lines to the circuit: T≤8, T=1, D/A bit 6, and D/A bit 7.

When T=1, the MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond timeout to ensure that the actuator has settled on track. Dur-

ing this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the Seek Error FF.

At the end of the timeout, the MPU ensures that -Demodulator Active is low and that there are no pulses on the Inner or Outer Guard Band lines. If the seek operation was successful, the MPU switches the +Enable Flasher line low. This reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array using I/O Control lines 1 and 2. With this FF set, On Cylinder and Seek End status appear on the interface.

If the seek operation was unsuccessful, the MPU sets the Seek Error FF in the I/O Gate Array by using Control lines 1 and 2. With this FF set, Seek Error and Seek End status appear on the interface. As a maintenance aid, the MPU displays a servo status code on the fault display board. These codes, discussed in Section 3, indicate where the seek operation failed.

After providing Seek End status, the MPU waits for further commands from the controller.

Return to Zero Seek

The Return to Zero (RTZ) seek is the operation that moves the heads from any location on the disk to track 0. Although the MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail. If the RTZ seek in a load operation is unsuccessful, the MPU lights the First Seek fault indicator, and a reattempt occurs only if the Fault Clear switch is pressed. If a controller-initiated RTZ seek is unsuccessful, the MPU sets the Seek Error FF, and Seek Error is active on the I/O. In this case, the drive waits for another RTZ command from the controller.

This discussion pertains specifically to the controller-initiated RTZ seek. This seek is flow-charted in figure 1-47. Refer to the Load Operation discussion for details about the RTZ portion of the load operation.

The controller initiates an RTZ operation by outputting Tag 3 (Control Select) along with Bus bit 6. The RTZ Seek command is decoded on the I/O Gate Array where it clears the Cylinder and Head Address registers, the On Cylinder FF, and Seek Error FF (all in the I/O Gate Array). In addition, the I/O Gate Array

START

CONTROLLER OUTPUTS
TAG 3 WITH BUS
BIT 6 TRUE

I/O GATE ARRAY
DECODES RTZ
SEEK COMMAND
(0206)

CLEARS CYLINDER
ADDRESS
REGISTER
(0206)

RTZ SEEK INTER-
RUPTS MPU
AT PIA-O
(0305)

CLEARS HEAD
ADDRESS
REGISTER
(0206)

MPU PRESETS THE
+SLOPE LINE TO
TRIBIT DECODER
(0306)

CLEARS ON
CYLINDER FF &
SEEK ERROR FF
(0206)

IS
+FAULT
LINE ACTIVE?
— YES → TO SHT 2 B

NO

IS
-DEMODULATOR
ACTIVE SIGNAL
HIGH PRIOR TO
RTZ?
— YES → TO SHT 2 B

NO

MPU ALLOWS
ACTUATOR TO COAST
UNTIL VELOCITY
DROPS TO 2 IPS

MPU MAKES +COARSE
LINE HIGH AND
-FORWARD LINE HIGH
(0306)
→ 1

1

MPU INPUTS
CONSTANT VELOCITY
VIA D/A BITS 0-7
(0307)

ACTUATOR MAKES
A SLOW REVERSE
MOVE

ARE
PULSES DETECTED
ON OUTER GUARD
BAND LINE?
(0306)
— NO (loop)

YES

MPU REDUCES
D/A INPUT
(0307)

ACTUATOR CON-
TINUES REVERSE
MOVE AT SLOWER
VELOCITY

IS
-DEMODULATOR
ACTIVE SIGNAL
LOW?
(0306)
— NO → TO SHT 2 B

YES

PTM #2 COUNTER
COUNTS 2
CYLINDER PULSES
(0307)

PTM INTERRUPTS
MPU
→ 2

2

MPU MAKES
-FORWARD LINE
LOW
(0306)

ACTUATOR MAKES
SLOW FORWARD
MOVE

ARE
PULSES DETECTED
ON OUTER GUARD
BAND LINE?
(0306)
— YES (loop)

NO

WAS
AT LEAST
1 CYLINDER PULSE
DETECTED
IN G,B
— NO → TO SHT 2 B

YES → TO SHT 2 A

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Figure 1-47. Return to Zero (RTZ) Seek (Sheet 1 of 2)

FROM
SHT 1
(A)

FROM
SHT 1
(B)

(1)

(3)

(4)

```
┌─────────────┐        ┌─────────────┐
│ MPU WAITS FOR│        │ AFTER A DELAY,│
│ NEXT CYLINDER│        │ MPU MAKES    │
│ PULSE (TRACK -1)│     │ -TRACK FOLLOW│
└─────────────┘        │ LINE LOW     │
                       └─────────────┘
                            (0306)
```

WERE
3 OR MORE
ADDITIONAL CYL-
INDER PULSES
COUNTED? ── YES ──►

NO

```
┌─────────────┐
│ MPU REDUCES │
│ D/A COUNT   │
└─────────────┘
```

```
┌─────────────┐
│ WITH ON CYLINDER│
│ SENSE ACTIVE,   │
│ MPU STARTS A    │
│ 2.1 ms TIMEOUT  │
└─────────────┘
```

DID
-DEMODULATOR
ACTIVE STAY
LOW? ── NO ──►
(0306)

YES

(0307)
(2)

```
┌─────────────┐
│ MPU MAKES   │
│ +INTEGRATOR │
│ CLAMP LINE  │
│ LOW         │
└─────────────┘
    (0305)
```

DID
ON CYLINDER
SENSE STAY ACTIVE
FOR 2.1 ms? ── YES ──► (3)

NO
(0306)

```
┌─────────────┐
│ HEADS ARE   │
│ POSITIONED AT│
│ TRACK ZERO  │
└─────────────┘
```

```
┌─────────────┐
│ MPU MAKES +T=1│
│ AND +T≤8 LINES│
│ HIGH          │
└─────────────┘
    (0305)
```

```
┌─────────────┐
│ MPU STARTS  │
│ AN 11 ms    │
│ TIMEOUT     │
└─────────────┘
```

ARE
PULSES DETECTED
ON GUARD BAND
LINES? ── YES ──►
(0306)

NO

```
┌─────────────┐
│ MPU SETS SEEK│
│ ERROR FF & DROPS│
│ ALL SERVO COMMANDS│
└─────────────┘
```

```
┌─────────────┐
│ MPU MAKES   │
│ +ENABLE FLASHER│
│ LINE HIGH AND│
│ MONITORS -FINE│
│ ENABLE LINE │
└─────────────┘
  (0306,0307)
```

WERE
3 OR MORE
ADDITIONAL CYL-
INDER PULSES
COUNTED? ── YES ──► (4)

NO

```
┌─────────────┐
│ MPU MAKES +ENABLE│
│ FLASHER LINE LOW │
│ AND SETS ON      │
│ CYLINDER FF      │
└─────────────┘
   (0206,0306)
```

```
┌─────────────┐
│ MPU INDICATES│
│ SERVO STATUS CODE│
│ ON FAULT DISPLAY │
│ BOARD        │
└─────────────┘
```

```
┌─────────────┐
│ -FINE ENABLE│
│ LINE GOES   │
│ LOW         │
└─────────────┘
    (0307)
```

DID
ON CYLINDER
SENSE GO
ACTIVE? ── NO ──┐
(0306)

YES

```
┌─────────────┐
│ ON CYLINDER &│
│ SEEK END SENT│
│ TO CONTROLLER│
└─────────────┘
```

```
┌─────────────┐
│ MPU WAITS FOR│
│ RTZ SEEK     │
│ COMMAND FROM │
│ CONTROLLER   │
└─────────────┘
```

```
┌─────────────┐
│ MPU MAKES   │
│ +COARSE AND │
│ -SETTLE IN  │
│ LINES LOW   │
└─────────────┘
    (0306)
```

DID
11 ms TIMEOUT
ELAPSE? ── YES ──► (4)

NO

```
┌─────────────┐
│ DRIVE READY TO│
│ RESPOND TO    │
│ CONTROLLER    │
│ COMMANDS      │
└─────────────┘
```

(1)

(2)

11D81-2

Figure 1-47.   Return to Zero (RTZ) Seek (Sheet 2)

sends the RTZ interrupt to PIA-0 on the Control Board to generate an interrupt to the MPU.

The MPU reads the RTZ interrupt and initiates the RTZ. At this point, the actuator is floating freely over the data zone. Prior to moving the actuator, the MPU checks the -Demodulator Active and the +Fault lines. If either line is high, the MPU sets the Seek Error FF.

After waiting for the actuator velocity to drop to two inches per second, the MPU uses the coarse servo loop to move the heads outward into the outer guard band. To do this, the MPU switches the +Coarse line high and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

Once the heads reach the outer guard band, the MPU reduces the D/A input, and the actuator continues to move outward at reduced velocity. The MPU verifies that the -Demodulator Active signal remains low, and it uses the programmable timer (PTM #2) to monitor cylinder pulses.

When PTM #2 has counted the two cylinder pulses for this move, it interrupts the MPU. The MPU reacts by issuing the Forward command to make the heads seek inward. The MPU requires that one cylinder pulse appears before the Outer Guard Band signal goes inactive (or it sets the Seek Error FF). After the Outer Guard Band signal goes inactive, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T$\leq$8 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond

timeout to ensure that the actuator has settled on track. During this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the Seek Error FF.

At the end of the timeout, the MPU ensures that -Demodulator Active is low and that there are no pulses on the Inner or Outer Guard Band lines. If the RTZ operation was successful, the MPU switches the +Enable Flasher line low. This reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array using I/O Control lines 1 and 2. With this FF set, On Cylinder and Seek End status appear on the interface.

If the RTZ operation was unsuccessful, the MPU sets the Seek Error FF in the I/O Gate Array by using Control lines 1 and 2. With this FF set, Seek Error and Seek End status appear on the interface. As a maintenance aid, the MPU displays a servo status code on the fault display board. These codes, discussed in Section 3, indicate where the seek operation failed.

After providing Seek End status, the MPU waits for further commands from the controller.

Unload Operation

The MPU uses the unload operation during the power off sequence to move the heads completely outward until they are located over the landing zone. The MPU initiates the unload sequence when it detects a loss of start conditions. A loss of start conditions occurs when the START switch is pressed to release it from the the Start position or (in remote operation) when the controller deactivates Sequence Hold.

Seeing a loss of start conditions, the MPU deactivates the Ready signal, drops all commands to the servo circuitry, and then issues the Retract command. The retract moves the heads slowly outward into the landing zone and holds them in contact with the soft actuator stop. After a delay, the MPU drops the Unlock Actuator command to lock the actuator in this position.

The MPU then drops the Motor Run command. The MPU monitors Motor Sensor pulses with the programmable timer (PTM#3); when the motor has stopped rotating, the MPU waits two seconds and drops the Retract command. The MPU allows a 30 second delay (during which the Ready indicator flashes) before it can recognize new start conditions and initiate another load operation.

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/write heads (refer to figure 1-48). The drive has two read/write heads for each data recording surface in the disk module as shown. The drive has 12 recording surfaces and 24 read/write heads. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.
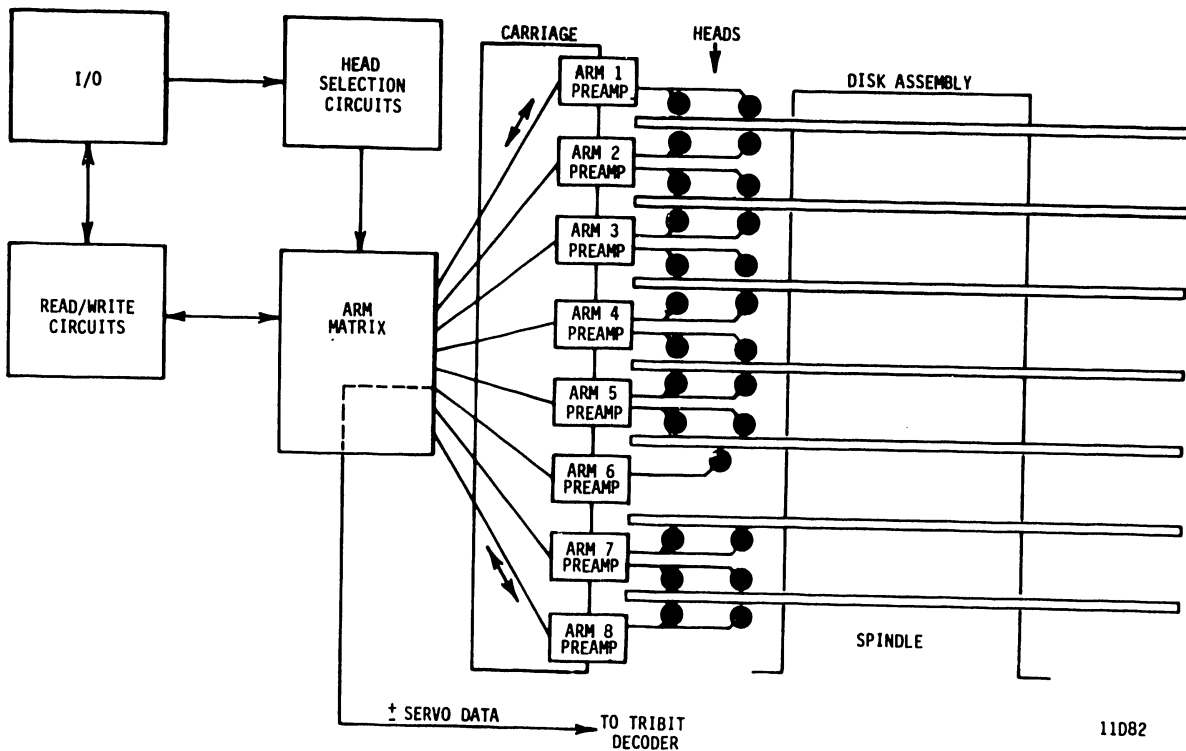
Figure 1-48.   Read/Write Heads

HEAD FUNCTIONAL DESCRIPTION

Each read/write head has a coil wound on its core. This coil interfaces to the read/write circuitry via a preamp mounted on the head-arm. Selecting a head requires selecting an arm preamp and supplying selection signals to that preamp indicating which head on that arm is desired. In response to the signal inputs, the enabled arm preamp selects one of the its heads, and either provides current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Read/Write Functions for details about the Arm Preamp.

During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The Arm Preamp supplies the selected head with a source of write current. At each transition of the write data signal, the preamp reverses the current in the head coil. This switching reverses the flux across the gap in the head (see figure 1-49). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching this current reverses the direction of the flux field across the gap. The flux change defines a data bit. New data is written simply by writing over any data which may already be on the disk.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 1-50). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Prior to head selection, the controller issues a cylinder select command. Under MPU control, the servo system moves the heads to the cylinder specified by the controller.

WRITE CURRENT

CURRENT
FLOW

MAGNETIC FLUX
FLOW

MAGNETIC
COATING
(SURFACE)

BASE

RECORDING
HEAD

SURFACE MOTION

NOTE: RELATIVE HEAD TO SURFACE MOTION, RECORDING (WRITE OPERATION)   11D189

Figure 1-49. Writing Data

READ BACK SIGNAL

READ CURRENT
FLOW

SURFACE MOTION

NOTE: RELATIVE HEAD TO SURFACE MOTION, REPRODUCING (READ OPERATION)

11D190
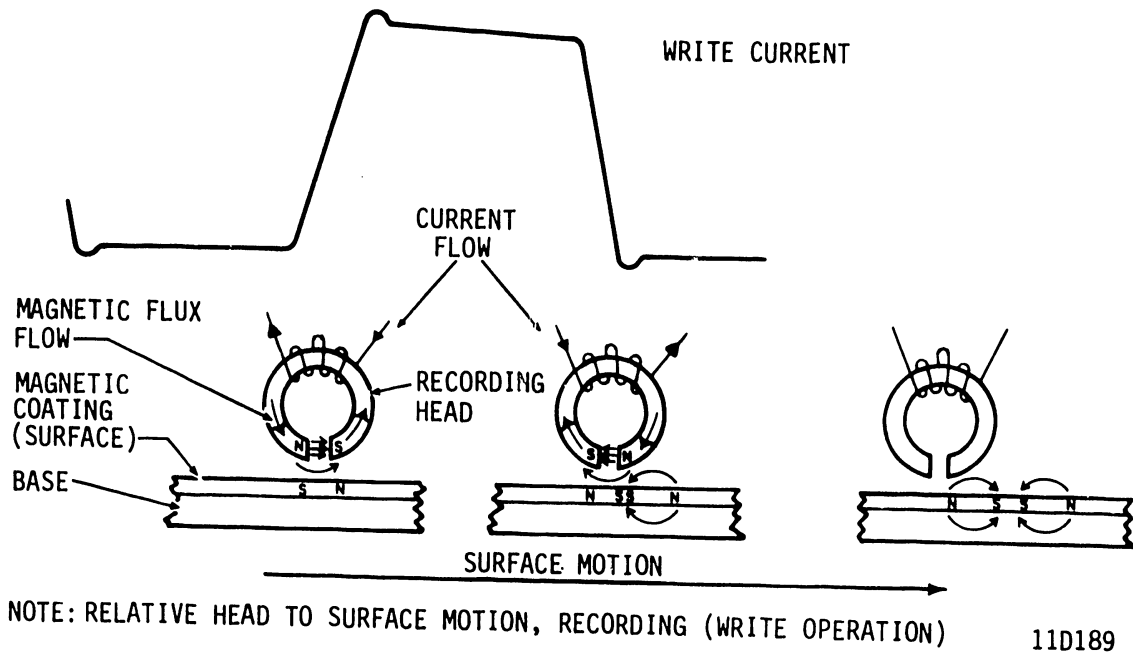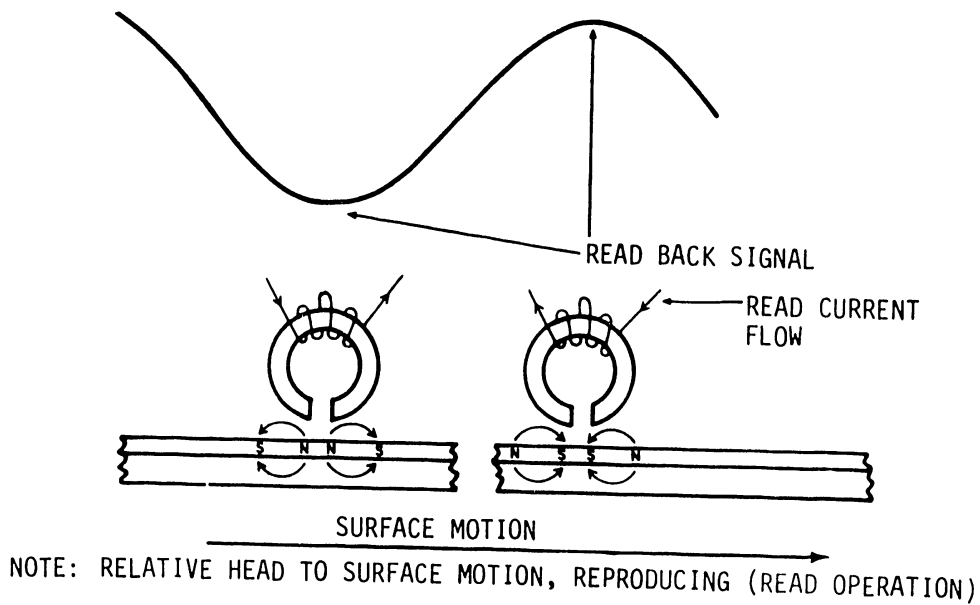
Figure 1-50. Reading Data

By selecting a head, the controller specifies a particular track within that cylinder. Head selection starts when the controller sends the drive a Head Select (Tag 2) command and a head address. The head address is sent on Bus bits 0 through 4.

The Head Select tag gates the address into the Head Address register (HAR) in the I/O Gate Array. Figure 1-51 shows the head selection circuits. The cylinder address and the head address are multiplexed out of the gate array on +Head/Cylinder Address lines 0-4. The MPU controls this multiplexing with I/O Control lines 1 and 2. In the initial phase of a seek, the Head/Cylinder Address lines transfer the new cylinder address to the MPU. With this transfer complete, the lines carry head address information. Thus, whenever the heads are on cylinder, +Head Address line 0 reflects HAR bit 0, and so forth.

The Head/Cylinder Address lines go from the I/O board to the Read/Write board via the Control board. The Read/Write board contains a ROM, addressed by Head Cylinder Address lines 0-4. Depending on its addressing, the ROM activates one its output lines, -Arm Select 1-8, to enable one arm preamp. The enabled arm preamp in turn selects of the heads on its head-arm in response to the +Head Select 1 and 2 lines. These lines are activated by Head/Cylinder Address lines 0 and 1 respectively. The Arm Select, Head Select, and common control lines for the preamps are routed through the Arm Matrix board (inside the module) to the individual arm preamps.

If an illegal head address (greater than 23) is received, no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 1-3 shows the combination of address lines that selects each head.

READ/WRITE FUNCTIONS (515 MB DRIVES)

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for Write Gate and Bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

83324770 A
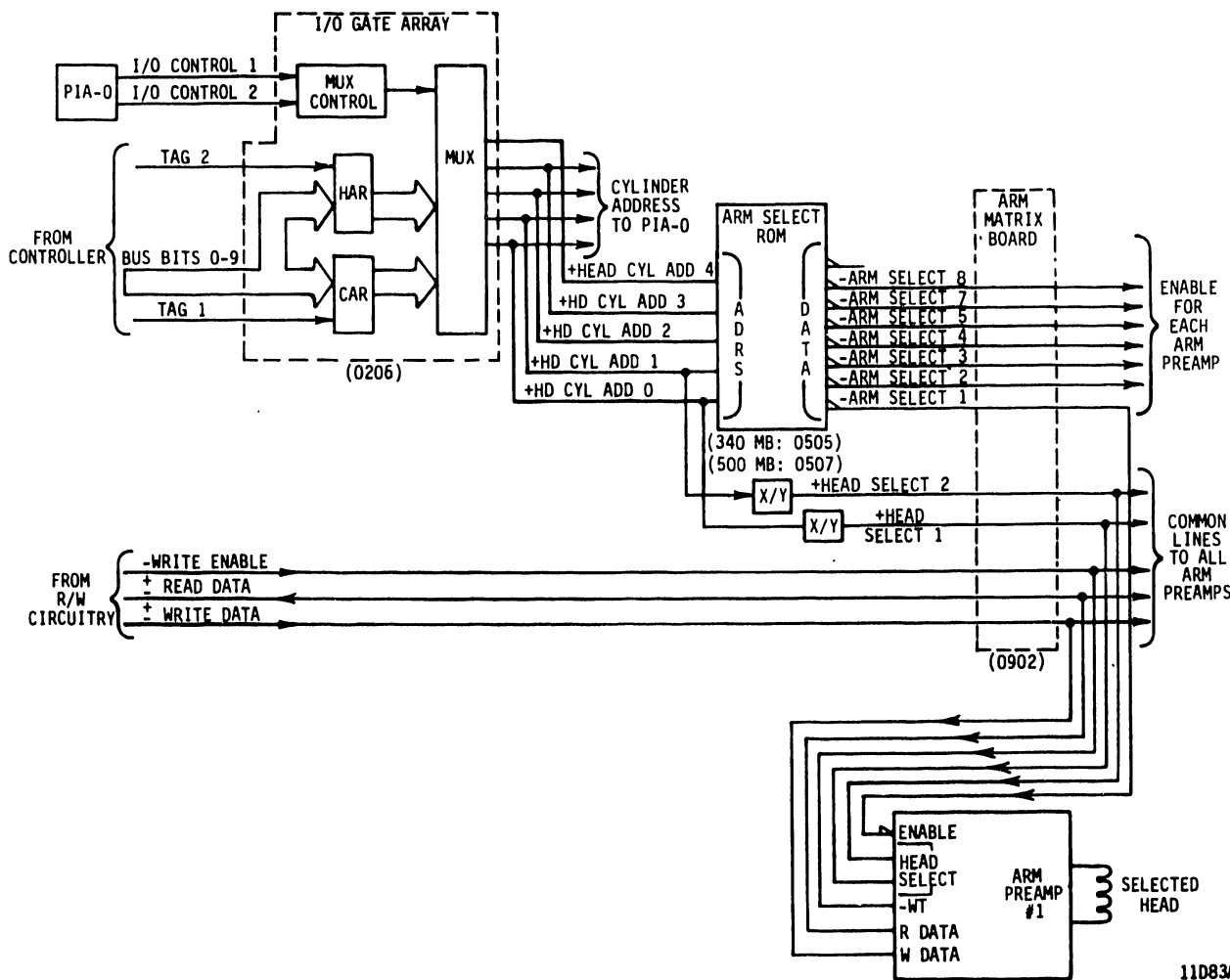
Figure 1-51.   Head Selection Circuits

Figure 1-52 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic R ad/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.

- Write Circuits -- Describes the circuits used by the drive to record data on the disk.

- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

TABLE 1-3. HEAD SELECT ADDRESSING

Head Selected	Arm Selected	+Head/Cylinder Address Lines				
		0	1	2	3	4
0	1	0	0	0	0	0
1	1	1	0	0	0	0
2	2	0	1	0	0	0
3	2	1	1	0	0	0
4	2	0	0	1	0	0
5	2	1	0	1	0	0
6	3	0	1	1	0	0
7	3	1	1	1	0	0
8	3	0	0	0	1	0
9	3	1	0	0	1	0
10	4	0	1	0	1	0
11	4	1	1	0	1	0
12	4	0	0	1	1	0
13	4	1	0	1	1	0
14	5	0	1	1	1	0
15	5	1	1	1	1	0
16	5	0	0	0	0	1
17	5	1	0	0	0	1
18	7	0	1	0	0	1
19	7	1	1	0	0	1
20	7	0	0	1	0	1
21	7	1	0	1	0	1
22	8	0	1	1	0	1
23	8	1	1	1	0	1

READ/WRITE CIRCUITS

FROM CONTROLLER
- WRITE CLOCK
- NRZ WRITE DATA

WRITE CIRCUITS

COMPENSATED 2-7 WRITE DATA

TRIBIT DECODER PLO

TO CONTROLLER
- SERVO CLOCK
- READ CLOCK
- NRZ READ DATA

READ CIRCUITS

2-7 READ DATA

ARM PREAMP

READ/ WRITE HEAD

DISK

HEAD SELECT CIRCUITS
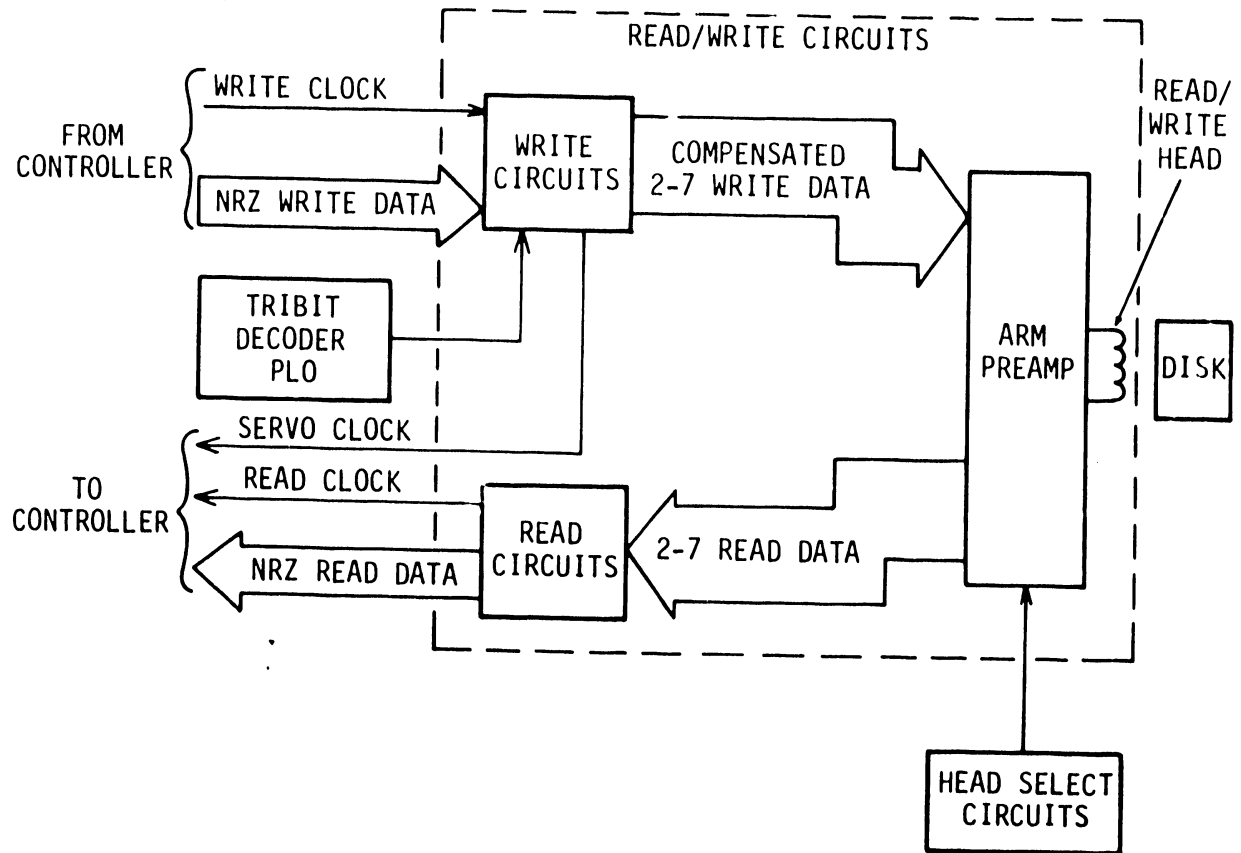
11D84

Figure 1-52. Read/Write Circuits

BASIC READ/WRITE PRINCIPLES

Principles of 2-7 Recording

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write operation. Write circuitry in the drive encodes the incoming data by changing it to 2-7 modulation. Transfers between the read/ write circuitry and the disk use 2-7 modulation. Therefore, in a read operation, read circuitry in the drive must decode the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and the explain why 2-7 modulation is used in the drive.

NRZ data is transferred at a nominal rate of 14.5 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 68.9 ns. For consecutive cells indicating binary 1, the read or write interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the maximum rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 1-4. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data.

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half the NRZ bit cell or 34.45 ns, nominal. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of binary 1 in the code, there are at least two zeros and as many as seven zeros.

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the 2-7 read signal if it were not compensated in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effect of peak shift.

TABLE 1-4. TRANSLATION BETWEEN NRZ AND 2-7 CODES

NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Figure 1-53 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a binary 1 appears in the 2-7 data string. Each toggle of write data reverses the magnetic flux in the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-53. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.

Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates

2-7 CODE   0   1   0   0   1   0   0   0   0   1

WRITE DATA
(INPUT TO HEAD)
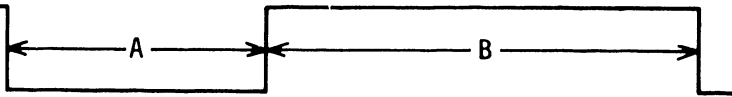
RECORDED FLUX
PATTERN

FLUX REVERSALS

READBACK
VOLTAGE PEAKS

COMPOSITE
READBACK VOLTAGE

PEAK SHIFT AWAY FROM
CLOSER ADJACENT PEAK

RAW
READ DATA
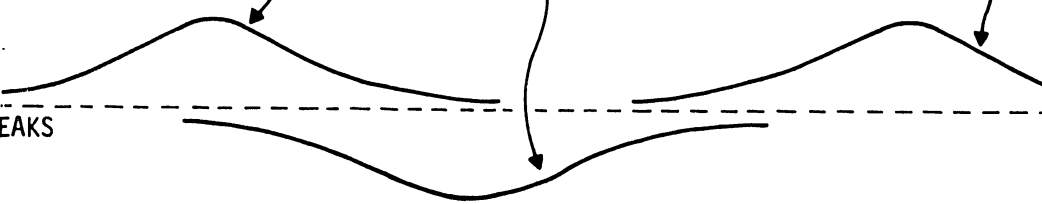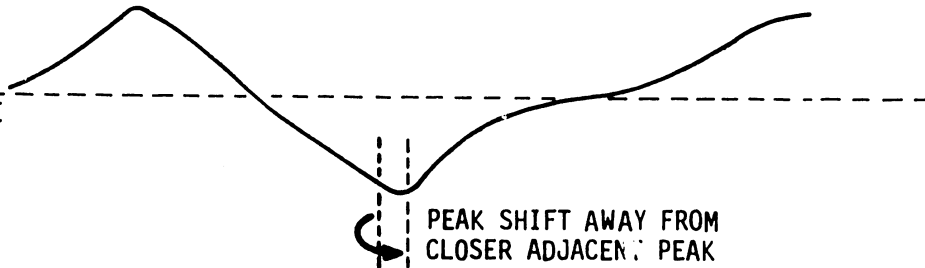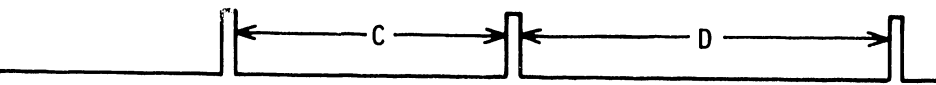
WITHOUT WRITE COMPENSATION, C > A AND D < B,
AND INACCURATE READ DECODING WOULD BE POSSIBLE

10R72A

Figure 1-53.   Peak Shift Waveforms

this problem by advancing or delaying each write transition by an amount that depends on the number of binary 0s leading and trailing the binary 1 producing that transition. When the number leading exceeds the number trailing, write compensation delays the write transition. When the number trailing exceeds the number leading, write compensation advances the write transition. When the two numbers are equal, the transition occurs without compensation. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of Write Compensation under Write Circuits includes a table that defines the compensation shift for each possible data pattern.

WRITE CIRCUITS

General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 14.5 MHz Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is then processed by the write driver circuit. The write driver circuit provides the data signal that controls current switching in the selected arm preamp.

Figure 1-54 shows the write circuits and table 1-5 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 29.01 MHz (2F) Write Clock. As shown in figure 1-55, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.

TABLE 1-5. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 29.01 MHz Write Clock which is divided by two to develop the 14.5 MHz Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Driver Circuits	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Arm Preamp	Switches the write current in the head coil as the signal from the write driver circuits changes polarity.
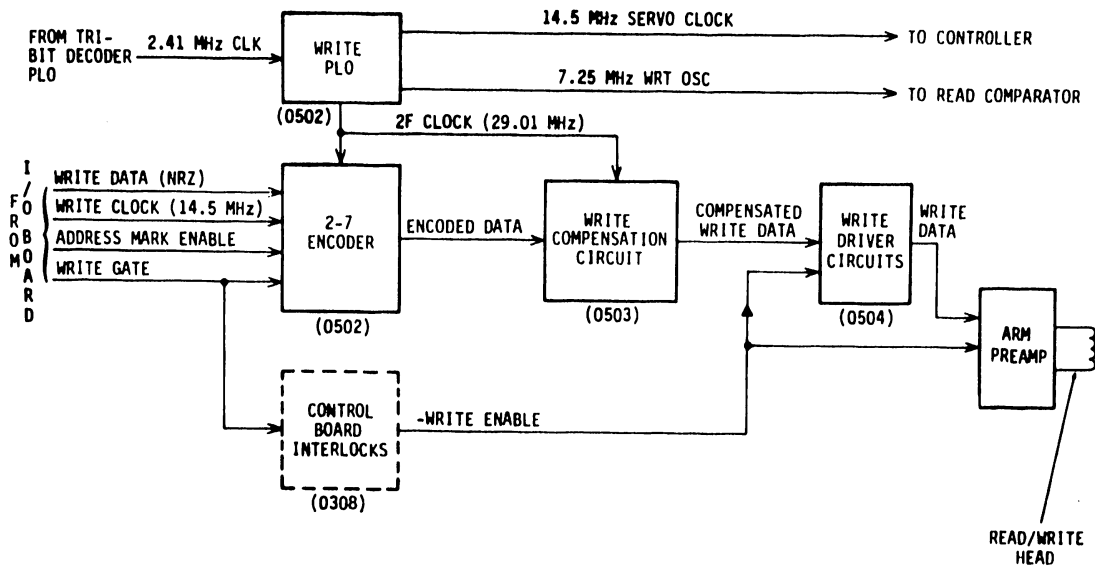
Figure 1-54. Write Circuits Block Diagram

83324770 A
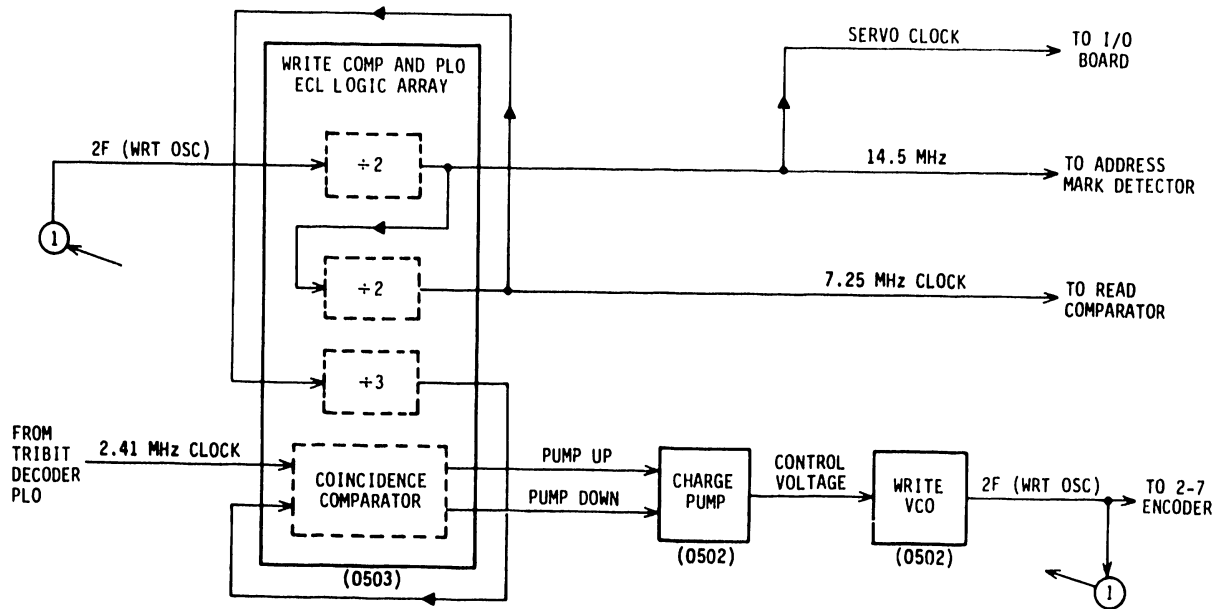
Figure 1-55. Write PLO Block Diagram

The phase-locked loop uses the 2.41 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 29.01 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 2.41 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F (WRT OSC) signal to the 2-7 Encoder circuit.

- 14.5 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.

- 7.25 MHz clock to the Read Comparator circuit.

2-7 Encoder

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 14.5 MHz Write Clock from the controller and the 29.01 MHz 2F Clock from the Write PLO (see figure 1-56). The encoder has a synchronizer that develops two clocks in phase with the 2F Clock -- the 2-7 Data Clock and a 14.5 MHz internal clock. The 2-7 Data Clock is supplied to the write compensation circuit. The internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.

The output shift register shifts its contents on each rising edge of the 2F Clock. The active low serial output of the register is -Encoded Data. This line is active for binary ones and inactive for binary zeros in the 2-7 data unless an address mark is being written. During an address mark, there are no transitions in the written flux, and a segment of the data track is erased. To command an address mark, the controller issues Tag 3 along with Bus bit 0 (Write Gate) and Bus bit 5 (Address Mark Enable). When Bus bit 5 goes inactive, the encoder resumes normal operation.

```
                    ┌─────────────────────────────┐
                    │    2-7 ENCODE - DECODE       │
                    │    ECL LOGIC ARRAY           │
                    │                              │
  FROM      2F (WRT OSC)   ┌ ─ ─ ─ ─ ─ ─ ┐         │
  WRITE ─────────────────►│             │         │    ± 2-7 DATA CLOCK    TO WRITE
  PLO    WRITE GATE       │ SYNCHRONIZER │─────────┼──────────────────►   COMPENSENSATION
         ───────────────►│             │         │                       CIRCUITRY
         WRITE CLOCK      │             │         │
         ───────────────►│             │         │
                          └ ─ ─ ─ ─ ─ ─ ┘         │
                              │   │                │
                          ┌ ─ ▼ ─ ▼ ─ ─ ┐         │
         WRITE DATA       │   PATTERN    │         │
         ───────────────►│ RECOGNITION  │         │
  FROM                    │  CIRCUIT     │         │
  I/O ┤                   └ ─┬─┬─┬─┬─ ─ ┘         │
                          ┌ ─▼─▼─▼─▼─ ─ ┐         │
                          │   OUTPUT     │         │
                         ►│   SHIFT      │         │
                          │ REGISTER     │──┐      │
                          └ ─ ─ ─ ─ ─ ─ ┘  │      │
  ADD MARK ENABLE                          ┌▼┐     │    -ENCODED DATA     TO WRITE
  ─────────────────────────────────────► │&│─────┼──────────────────►  COMPENSATION
                                          └─┘     │                      CIRCUITRY
                    └─────────────────────────────┘
                              (0502)
                                                            11D87
```
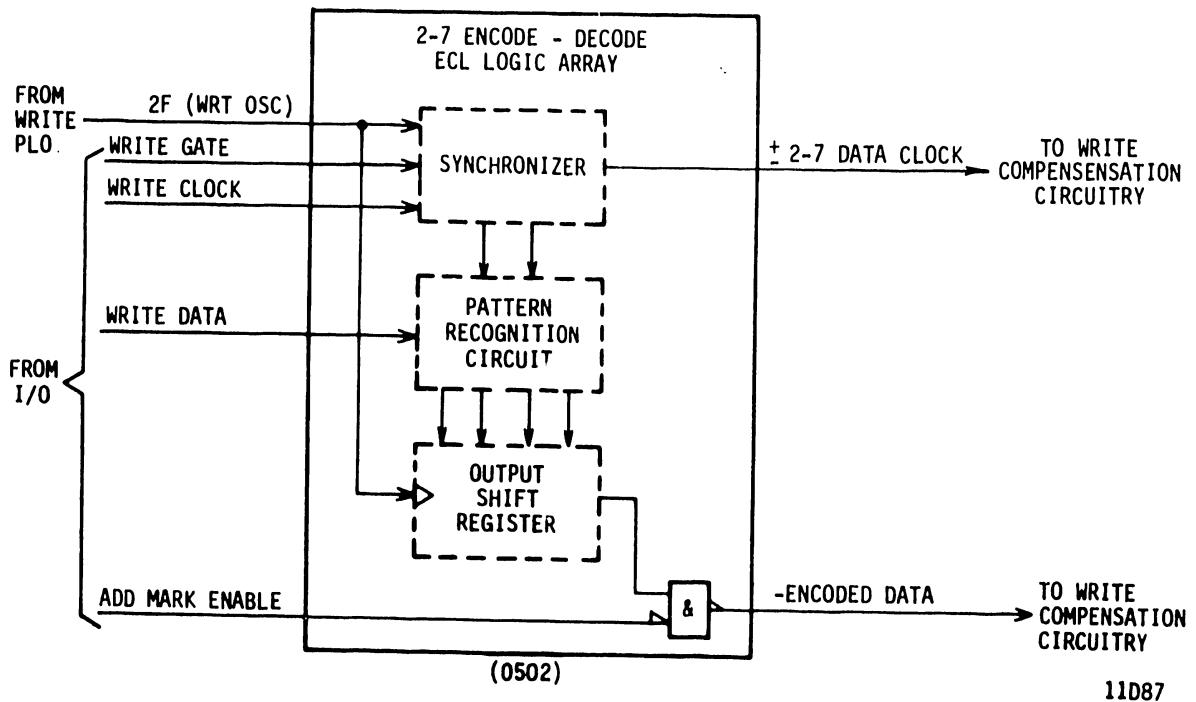
Figure 1-56.   2-7 Encoder Block Diagram

The encoder begins translating NRZ code words with the first
binary zero in the NRZ data occurring on or after the second
rising edge of Write Clock. Encoder operation proceeds contin-
uously, processing all NRZ data input to it until Write Gate
goes inactive.

Write Compensation Circuit

The write compensation circuit modifies the timing of transi-
tions in the encoded 2-7 data in a manner that compensates for
peak shift (refer to discussion on basic read/write principles).

Encoded 2-7 data contains isolated bit cells at binary one pre-
ceded and followed by from two to seven bit cells at binary
zero. Each time the data changes from binary zero to binary
one, the head reverses its flux direction. Write compensation
shifts this positive-going edge away from its nominal timing,
and this timing change is related to the number of zeros pre-
ceding and trailing a binary one in the data pattern.

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The write compensation function takes place in the Write Com-
pensation and PLO ECL Logic Array (see figure 1-57). This chip
is capable of following four different compensation schemes as
dictated by its "A" and "B" inputs. In this drive, input "A"
is pulled low and input "B" is tied high. This selection, and
the delays with which the 2-7 Data Clock enters chip inputs P1
through P9, produce specified time shifts for each possible
data pattern. Table 1-6 specifies the delay for each data pat-
tern relative to the nominal delay present in the circuitry.
In the table, negative delays represent earlier timing and pos-
itive delays represent later timing.

Uncompensated data enters the circuit via the -Encoded Data
line. This data is clocked into a 13-bit shift register. The
delay line develops the clock input by delaying the 2-7 Data
Clock. When the center bit of the shift register contains a
binary one, the circuit looks at the number of register bits
which are zero on each side of the center bit. Depending on
the number of leading zeros and trailing zeros, one of the de-
layed clocks P1 through P9 is applied to an AND gate along with
the center bit of the register. Thus, the AND gate sees the
center register bit go active, followed by the applied clock
going active; with both inputs active, the gate outputs a com-
pensated write data pulse. The positive edge of the compensa-
ted data pulse is timed by the clock selected.
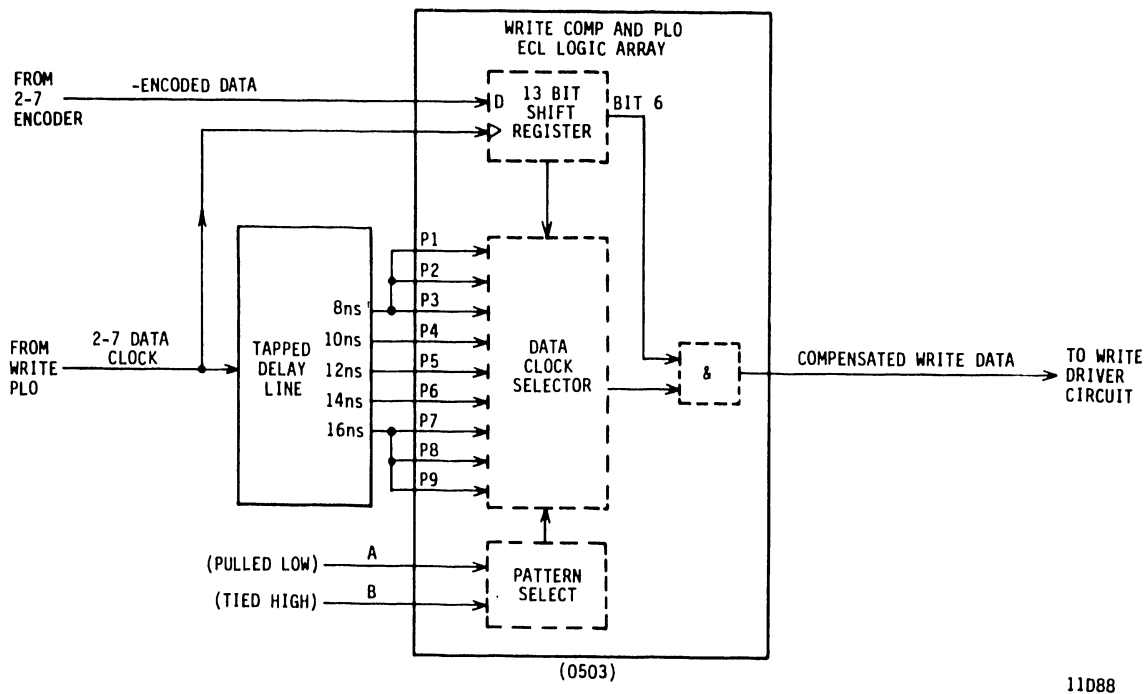
Figure 1-57. Write Compensation Block Diagram

1-128

83324770 A

Table 1-6 specifies the clock input gated out of the write compensation circuit for each possible data pattern. Note that a majority of the data patterns use the P5 clock and have the nominal delay.

After being write compensated, the data is transmitted to the write driver circuit.

TABLE 1-6. WRITE COMPENSATION FOR EACH DATA PATTERN

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number	2	0 ns* P5**	-2 ns P4	-4 ns P3	-4 ns P2	-4 ns P1	-4 ns P1
of	3	+2 ns P6	0 ns P5	0 ns P5	-2 ns P4	-2 ns P4	-2 ns P4
	4	+4 ns P7	0 ns P5	0 ns P5	0 ns P5	0 ns P5	0 ns P5
Leading	5	+4 ns P8	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
Zeros	6	+4 ns P9	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	7	+4 ns P9	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5

*Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.

**Bottom entry indicates which delayed clock enables a compensated output pulse.

Write Driver Circuit

The compensated write data is applied as the clock input to a latch. This latch changes state with each positive edge at its clock input. The write driver circuit operates only when the -Write Enable line is active (low). With -Write Enable inactive, the latch remains cleared, and the Write Data lines to the Arm Preamps remain inactive. The -Write Enable line comes from the Control board and is active only when all the following are true:

- Write Gate is active

- Write Protect is not active

- No faults exist

- Speed OK is active

- Enable Power Amp signal is active

Arm Preamp

Each head arm contains an LSI chip that serves as a preamp for the heads attached to that arm. The LSI chip selects a data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 1-58). These paragraphs concentrate on the preamp's write function and assume that head selection has occurred.

The LSI chip functions as a write driver when the -Write Enable line goes active (low). The chip develops regulated current for the selected head coil and reverses the current in that coil to produce flux reversals on the disk.

Throughout a write operation, write current is always flowing through the head coil. The Write Driver circuit inputs two Write Data lines to the selected Arm Preamp. When a transition occurs on the input lines, the LSI chip switches the write current direction through the head coil. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, there is no switching action, and an unchanging flux is recorded on the disk. Thus, writing an address mark erases a segment of the data track.

```
FROM CONTROL        -WRITE ENABLE
BOARD INTERLOCKS

                    +WRITE DATA
FROM WRITE
DRIVER CIRCUIT {    -WRITE DATA
```

SELECTED ARM PREAMP

WRITE
SELECT

SELECTED
READ/WRITE
HEAD

SELECTED
CURRENT
SWITCH

NOTES:

⚠ PREAMP LOGIC IS SIMPLIFIED TO SHOW WRITE
FUNCTION ONLY. REFER TO HEAD SELECTION
DISCUSSION FOR THIS ASPECT OF R/W PREAMP
OPERATION.
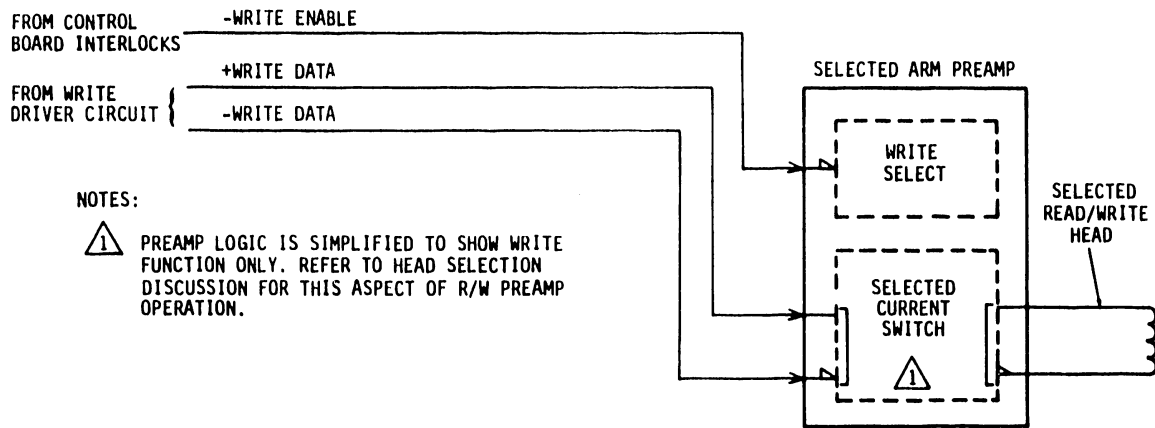
11D178A

Figure 1-58.   Arm Preamp

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with
Bus bit 1 true.   This enables the preamp circuits, which sense
the data written on the disk and generate analog read data sig-
nals.

The analog data goes to the Data Latch circuit which changes it
into digital 2-7 data.

The Read Comparator and PLO circuit generates a 29.01 MHz Read
Clock signal that is phase-locked to the 2-7 read data.   The
2-7 Decoder changes the 2-7 data to NRZ data synchronized to a
14.5 MHz Read Clock.   Both data and clock are then sent to the
controller.

Figure 1-59 shows the main elements in the read circuits and
table 1-7 briefly describes each of these elements.   The fol-
lowing paragraphs further describe the read circuits.

83324770 B
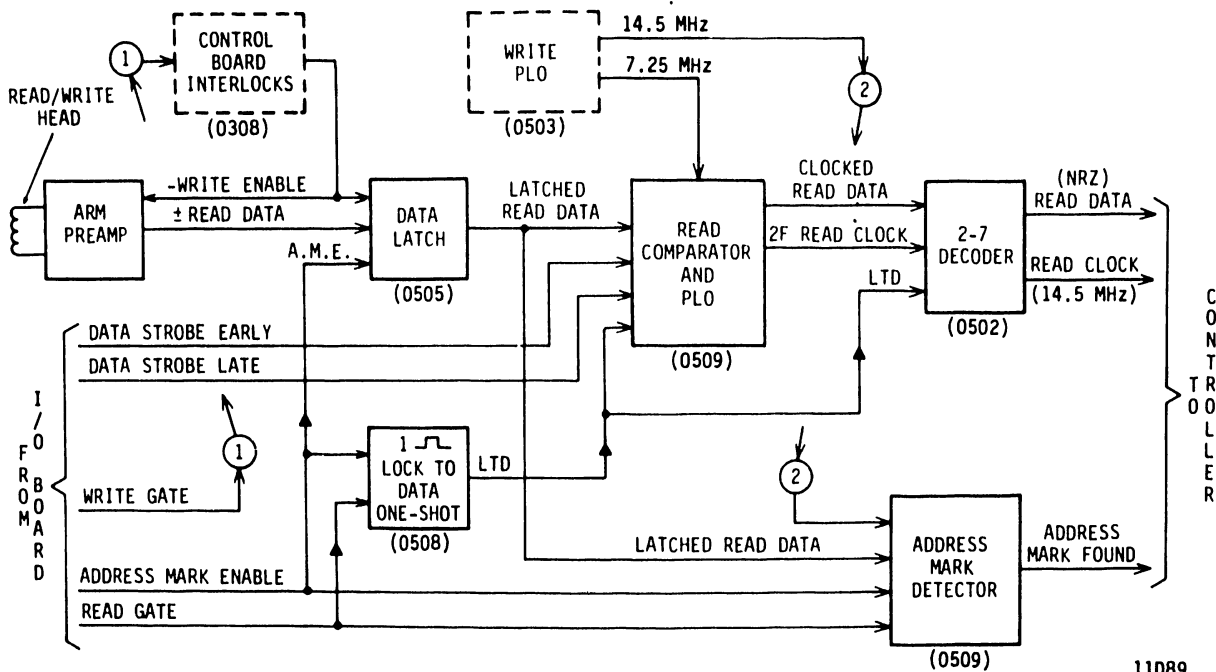
Figure 1-59. Read Circuits Block Diagram

Arm Preamp

The Arm Preamp is an LSI chip that selects a data head on its head arm and either switches write current through the head or amplifies the read signal detected by the head. These paragraphs concentrate on the preamp's read function and assume that head selection has occurred.

The LSI chip functions as a read preamp when the -Write Enable line is inactive (high). The chip contains a separate differential amplifier for each head, and head selection enables the differential amplifier associated with the desired head. In read operations, the coil in the selected head develops a readback pulse when the head passes over a written flux reversal on the disk. The readback pulse is supplied as a differential input to the preamp.

TABLE 1-7. READ CIRCUIT FUNCTIONS

Circuit	Function
Arm Preamp	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Comparator circuit.
Read Comparator and PLO Circuit	Develops a 29.01 MHz Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 14.5 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 14.5 MHz Read Clock.
Address Mark Detector	Detects the address mark and transmits an Address Mark Found to the controller.

The differential amplifier selected in the chip amplifies the read signal and sends it on the Read Data lines to read circuitry on the Read/Write board.

Data Latch Circuit

The Data Latch circuit receives analog read data from the selected Arm Preamp and converts it into digital data. As shown in figure 1-60, some portions of the Data Latch circuit are located inside the Data Latch Analog Master Chip, and other portions are outside the chip.

The input signal is amplified by the Buffer Amp, provided that –Write Enable is inactive (high). The +HCA 0 line establishes the gain of the Buffer Amp -- lower for outer heads or higher for inner heads. After further amplification (inside the master chip), the signal is split into three signal paths -- the high resolution channel, the low resolution channel, and the
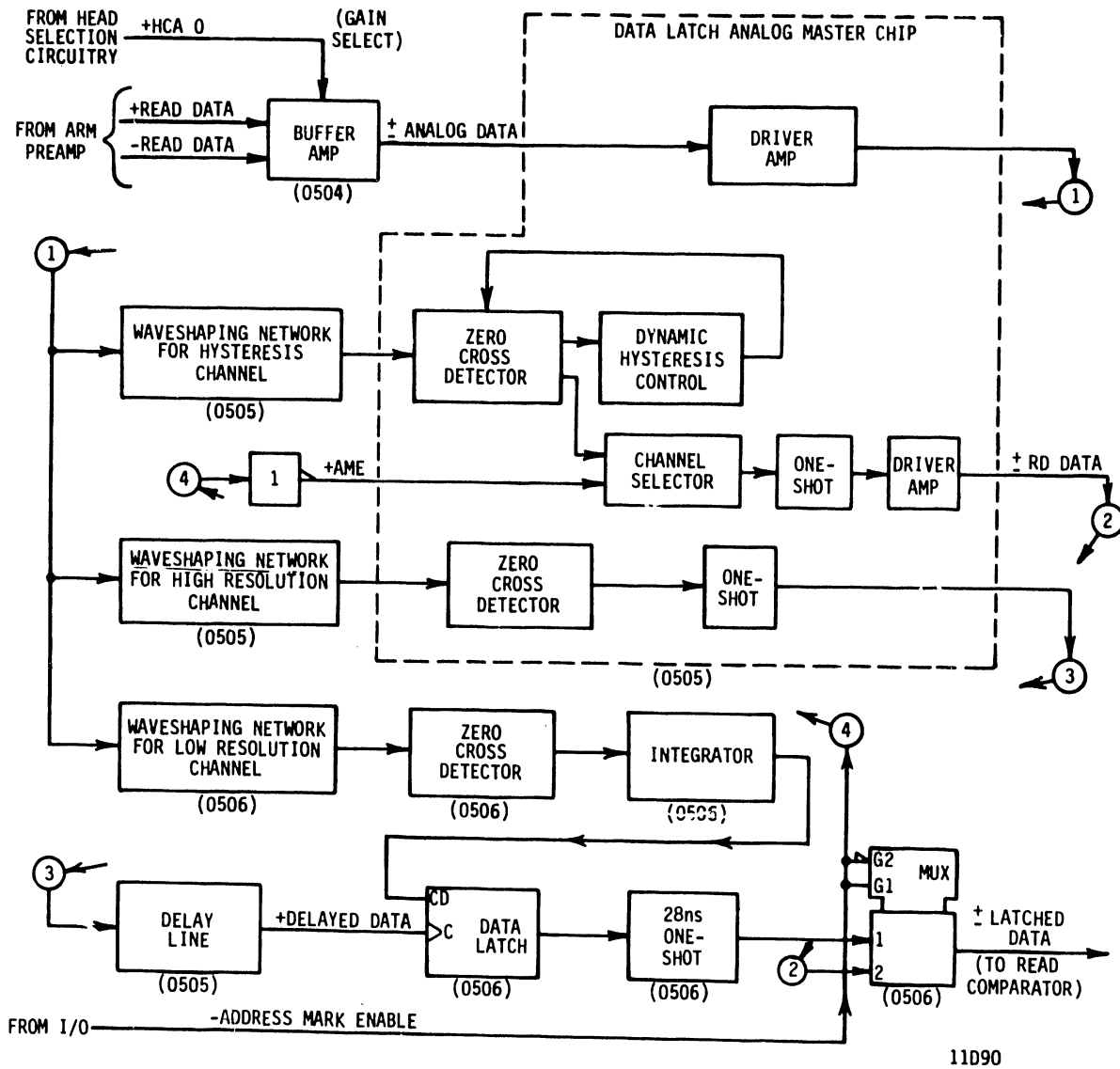
Figure 1-60. Data Latch Block Diagram

hysteresis channel. The high and low resolution channels contain independent wave-shaping circuitry, and they provide separate inputs to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. Each transition of the Data Latch FF triggers a 28 ns one-shot that pulses the +Latched Data output lines once for each written flux transition sensed by the data head. These pulses are gated by a multiplexer to the Read Comparator.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions. The low resolution channel uses a band-pass filter (with a 5 MHz bandwidth) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a band-pass filter (with a 13 MHz bandwidth) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the +Read Data output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when Address Mark Enable goes active, which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. With Address Mark Enable active, the multiplexer selects the output of the hysteresis channel for the + Latched Data signal. Inside the master chip, the hysteresis channel contains a zero-cross detector and a dynamic hysteresis control circuit. To regulate operation of this zero-cross detector and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the output signal.

The +Latched Data from the Data Latch circuitry is sent to the Read Comparator - Address Mark ECL Logic Array.

Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 29.01 MHz Read Clock, and processes latched read data from the Data Latch to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-61 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator - Address Mark ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F RD OSC signal output from the VCO. The 2F RD OSC signal is fed back to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data (-Read Gate and AME low), the phase-locked loop uses the pulse train on the Latched Data line as a timing reference. In this case, the Read Oscillator Control uses a quadrature comparator to drive

Figure 1-61.   Read Comparator and PLO Block Diagram

the Pump Up and Pump Down lines as necessary to keep the rising edges of the 2F RD OSC signal coincident with the rising edges of +Latched Data pulses. For each Latched Data pulse, the quadrature comparator outputs a variable-length pulse on the Pump Up line, followed by a fixed-length pulse on the Pump Down line. When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

When the drive is not reading data (-Read Gate high or AME high), the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, a coincidence comparator in the ECL Logic Array monitors the phase difference between the 7.25 MHz WRT OSC signal (derived from the Write PLO) and the 2F RD OSC signal fed back from the VCO. When the rising edge of the 7.25 MHz signal leads the rising edge of the 2F signal, this comparator pulses the Pump Up line to increase the Read VCO frequency. Conversely, when the rising edge of the 7.25 MHz signal lags the rising edge of the 2F signal, this comparator pulses the Pump Down line to decrease the Read VCO frequency.

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while switching between the quadrature and coincidence comparators. The Stop/Start VCO line goes active for approximately 200 ns after the Latched Data pulse following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock within 2 microseconds during the switching transitions.

The Data Discriminator portion of the Read Comparator - Address Mark ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 1-61). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (34.45 ns), and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control Select) with Bus bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are input to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 14.5 MHz Read Clock.

2-7 Decoder

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 14.5 MHz Read Clock from the 29.01 MHz Read Clock. Both inputs, the 2-7 data and the 29.01 MHz Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 1-4, presented under Basic Read/ Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 1-62 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the +Lock to Data input goes inactive (low). This occurs 3 microseconds after Read Gate goes active unless an address mark search is in progress. If an address mark search is in progress, +Lock to Data goes inactive 3 microseconds after Address Mark Enable goes inactive, provided that Read Gate stays active. Once +Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 14.5 MHz Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

The 14.5 MHz Read Clock is generated from the 29.01 MHz Read Clock as this signal clocks a divide-by-two FF. The Q-output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 29.01 MHz Read Clock determines the positive edge of the 14.5 MHz Clock.

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 14.5 MHz Read Clock.
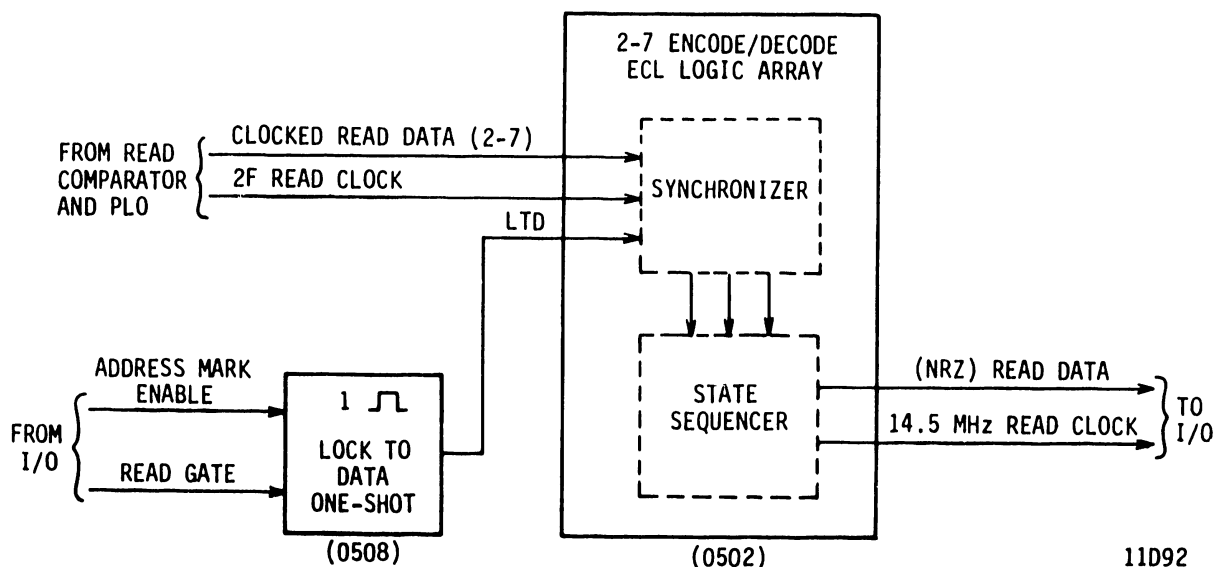
Figure 1-62.   2-7 Decoder Block Diagram

Thus, the interval for each state is one NRZ bit cell (68.9 ns). Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two 2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

The decoder sends the ±NRZ Read Data and ±Read Clock outputs to the I/O board to be transmitted on the interface to the controller.

Address Mark Detection

The Address Mark Detector, which is part of the Read Comparator - Address Mark ECL Logic Array, monitors the Latched Read Data signal from the Data Latch during an address mark search. If a gap of 1.36 to 2.45 microseconds is detected between incoming read pulses, the detector sets the Address Mark Found line, and the I/O circuitry sets the Address Mark line on the interface.

Figure 1-63 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus bits 1 and 5 active. In this situation, the -Read Gate line is low and the AME line is high. Together, these two signal inputs enable the Address Mark Detector.

The detector contains a counter circuit which is driven by the 14.5 MHz Clock signal from the Write PLO until it is reset by incoming read pulses. If the counter is clocked up over an interval from 20 to 36 clock periods, the Address Mark Found line is set. This line remains set until the lock-to-data interval ends (3 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.

```
                    ┌──────────────────────────┐
                    │   READ COMP - ADD MK     │
                    │   ECL LOGIC ARRAY        │
                    │   ┌ ─ ─ ─ ─ ─ ─ ─ ─ ┐    │
       AME+(RD•LTD) │                           │
    ──────────────────►│                     │    │
                    │   │                      │    │
FROM WRT PLO  14.5 MHz CLOCK                   │
    ──────────────────►│   ADDRESS          │    │  ADDRESS MARK FOUND   TO
FROM DATA LATCH  LATCHED READ DATA             │ ──────────────────────► I/O
    ──────────────────►│   MARK             │    │
FROM I/O    -RD GATE  │   DETECTOR         │    │
    ──────────────────►│                     │    │
            -LTD      │                      │    │
    ──────────────────►│                     │    │
                    │   └ ─ ─ ─ ─ ─ ─ ─ ─ ┘    │
                    └──────────────────────────┘
                              (0509)
```
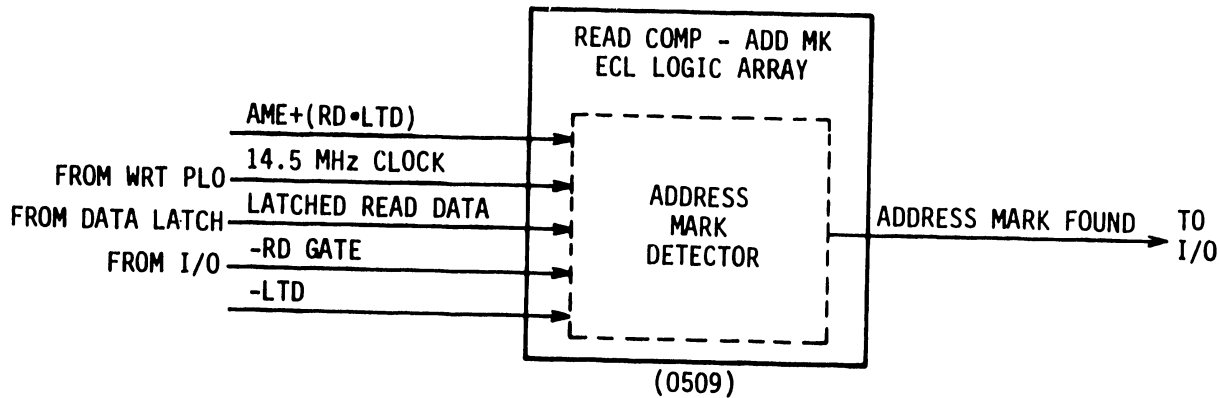
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Figure 1-63. Address Mark Detector Block Diagram

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The detector also contains a discriminator that distinguishes between read data gaps, caused by media defects, and gaps indicating address marks. If a defect is crossed, the discriminator inhibits the Address Mark Found output.

READ/WRITE FUNCTIONS (340 MB DRIVES)

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for Write Gate and Bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

Figure 1-64 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.

- Write Circuits -- Describes the circuits used by the drive to record data on the disk.

- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

BASIC READ/WRITE PRINCIPLES

Principles of MFM Recording

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write operation. Write circuitry in the drive encodes the incoming data by changing it to Modified Frequency Modulation (MFM). Transfers between the read/write circuitry and the disk use MFM. Therefore, in a read operation, read circuitry in the drive must decode the MFM read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and the explain wh· Modified Frequency Modulation is used in the drive.
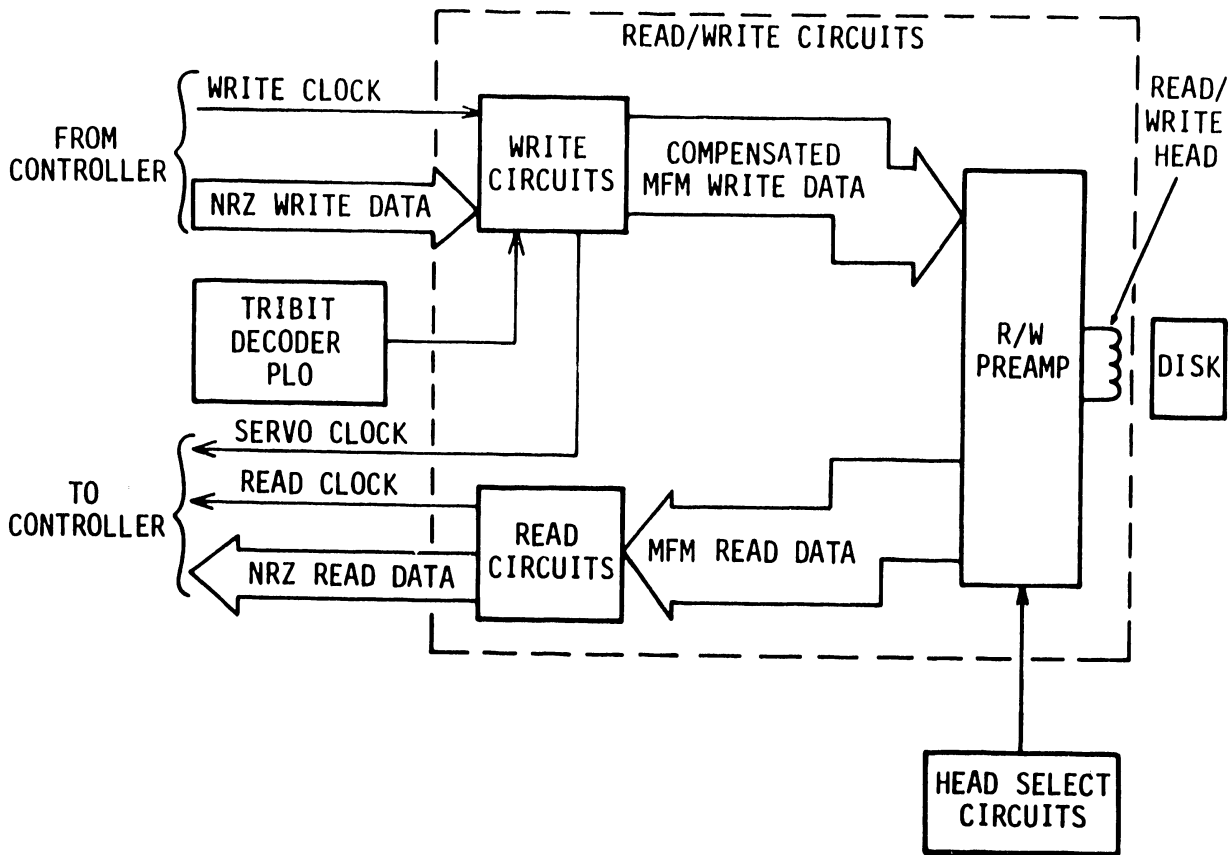
Figure 1-64. Read/Write Circuits

NRZ data is transferred at a nominal rate of 9.67 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 103 ns. For consecutive cells indicating binary 1, the read or write interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

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For disk transfers, the MFM scheme is superior to the NRZ scheme in two ways. First, it reduces the maximum rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 ns in width. The data transfer rate is, therefore, nominally 9.67 MHz.

MFM defines a "1" by writing a pulse at the half-cell time. A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".

- There is a flux transition between each pair of "0" bits.

- There is no flux transition between the bits of a "10" or "01" transition.

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the MFM read signal if it were not compensated in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effect of peak shift.

Figure 1-65 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a pulse occurs in the encoded MFM data . Each toggle of write data reverses the magnetic flux in the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

DATA PATTERN   1   0   0   0

WRITE DATA
(INPUT TO HEAD)

RECORDED FLUX
PATTERN   FLUX REVERSALS

READBACK
VOLTAGE PEAKS

COMPOSITE
READBACK VOLTAGE

PEAK SHIFT AWAY FROM
CLOSER ADJACENT PEAK

RAW
READ DATA
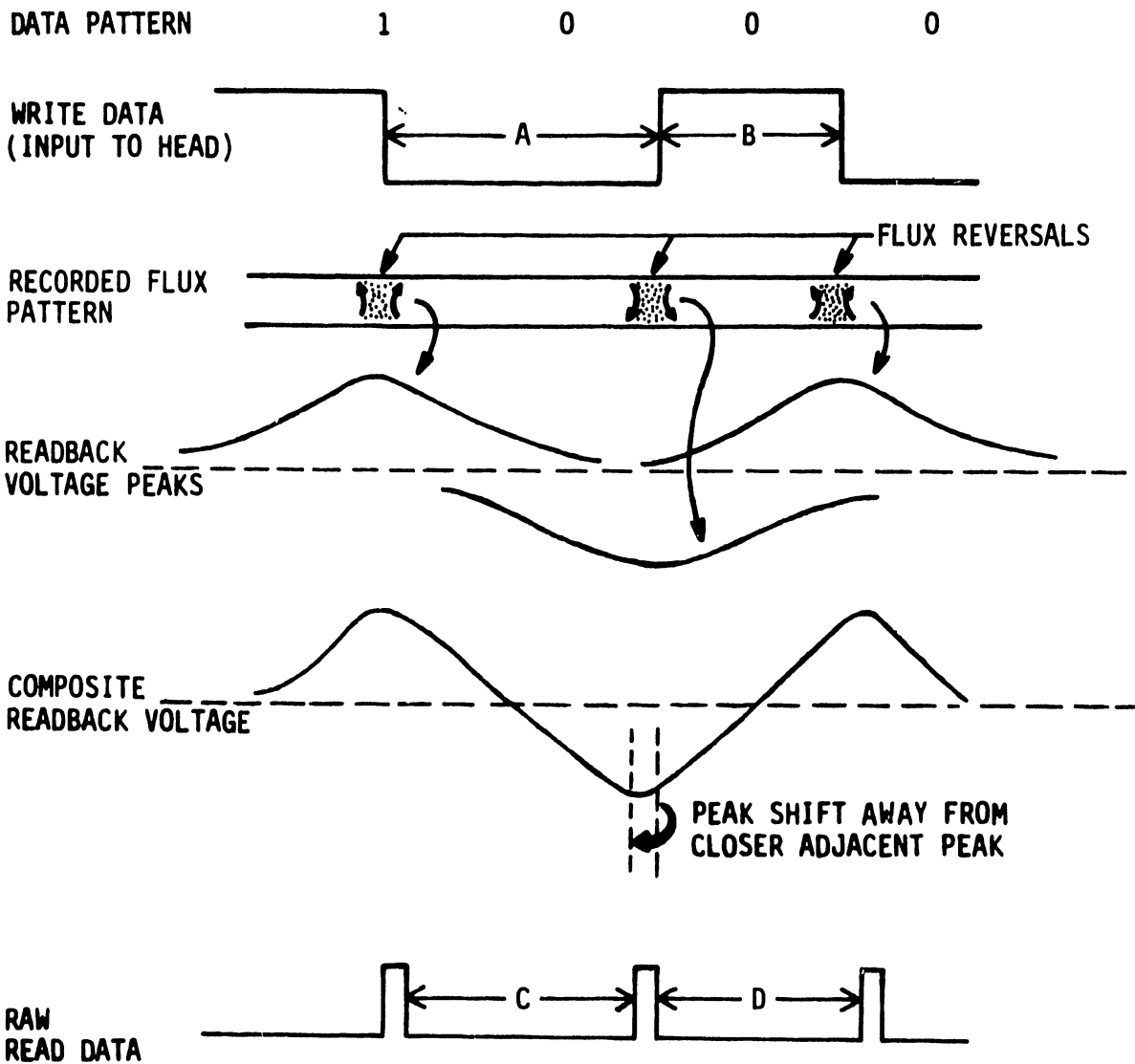
WITHOUT WRITE COMPENSATION, C<A AND D>B,
AND INACCURATE READ DECODING WOULD BE POSSIBLE

11D95

Figure 1-65.   Peak Shift Waveforms

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In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-65. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.

Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates this problem by recognizing two basic data patterns that require advancing a given write transition and two other data patterns that require delaying a given write transition.

Transitions requiring early timing are spaced closer to the preceding transition than they are to the following transition. Transitions requiring late timing are spaced closer to the following transition than they are to the preceding transition. Transitions requiring nominal timing are spaced equally between the preceding and following transitions. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of write compensation under Write Circuits defines the compensation shift in terms of specific rules based on data pattern timing.

WRITE CIRCUITS

General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 9.67 MHz Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the MFM encoder and write compensation circuit. This circuit converts the data to MFM modulation and modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is sent to the arm preamp, which switches current in the selected head.

Figure 1-66 shows the write circuits and table 1-8 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 19.34 MHz (2F) Write Clock. As shown in figure 1-67, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the MFM ECL Logic Array.

The phase-locked loop uses the 1.612 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 19.34 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 1.612 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.
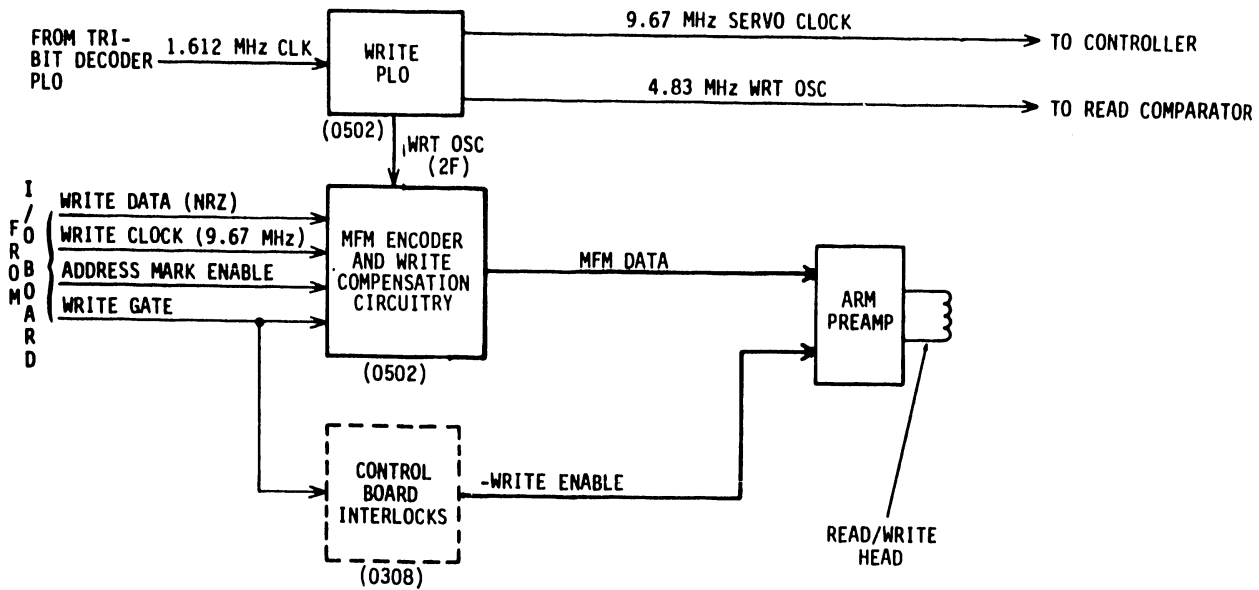
11D96

Figure 1-66. Write Circuits Block Diagram

TABLE 1-8. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 19.34 MHz Write Clock which is divided by two to develop the 9.67 MHz Servo Clock.
MFM Encoder and Write Compensation Circuitry	Converts the NRZ data from the controller to MFM data and compensates the data for problems caused by peak shift.
Arm Preamp	Switches the write current in the head coil as the signal from the MFM Encoder changes polarity.
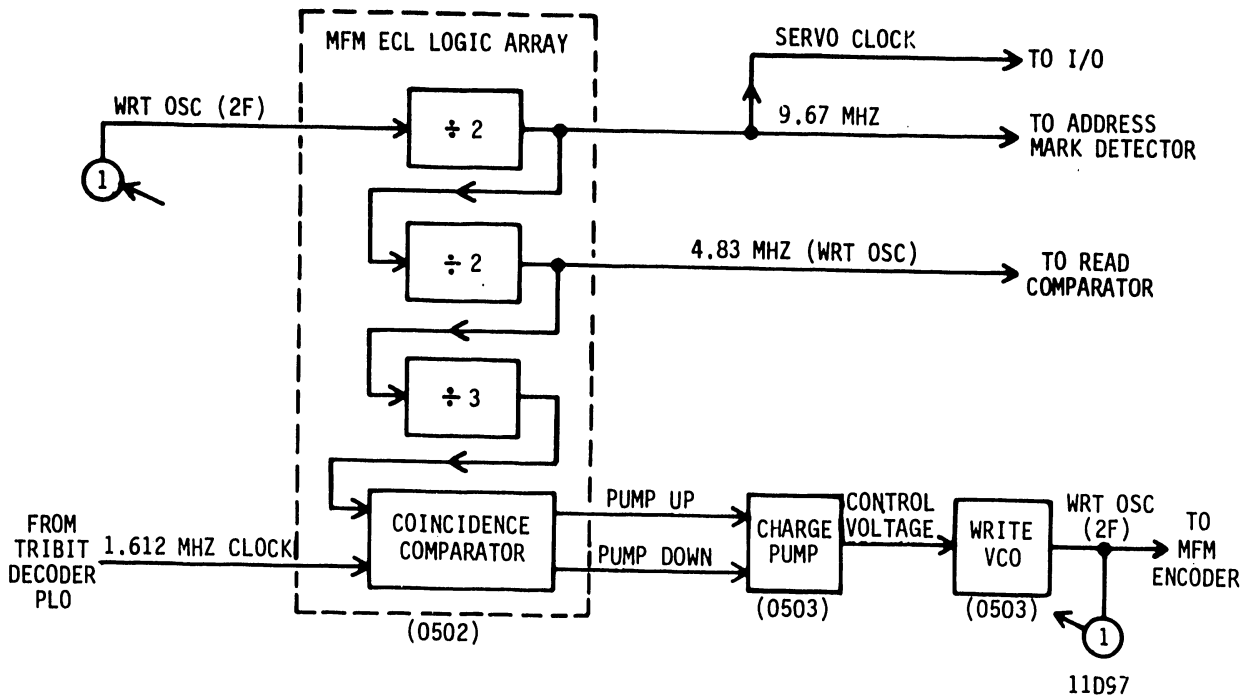
Figure 1-67. Write PLO Block Diagram

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- WRT OSC (19.34 MHz) signal to the MFM Encoder circuit.

- 9.67 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.

- 4.83 MHz clock to the Read Comparator circuit.

MFM Encoder and Write Compensation Circuitry

The MFM Encoder and Write Compensation Circuitry converts NRZ data into MFM data that is compensated for the effects of peak shift. This process takes place in the MFM ECL Logic Array, as shown in figure 1-68. The circuitry includes a clock synchronizer, a pattern decoder, an NRZ to MFM converter, gating circuitry for delayed clocks, a D flip-flop, and a write driver. These are discussed in the following paragraphs.

The clock synchronizer develops several internal clock signals for the circuitry inside the ECL Logic Array. The synchronizer is initialized at the start of a write operation after Write Gate goes active. Both internal clock signals are derived from the 2F clock supplied by the Write PLO. The 1F Internal Clock lags the +Write Clock input but remains in phase with the 2F clock.

The 1F Internal Clock signal clocks NRZ Write Data from the controller into the pattern decoder. The decoder supplies clock decodes (early, nominal, or late) to the gating logic. It also supplies inputs to the NRZ to MFM converter, based on the NRZ data pattern received.

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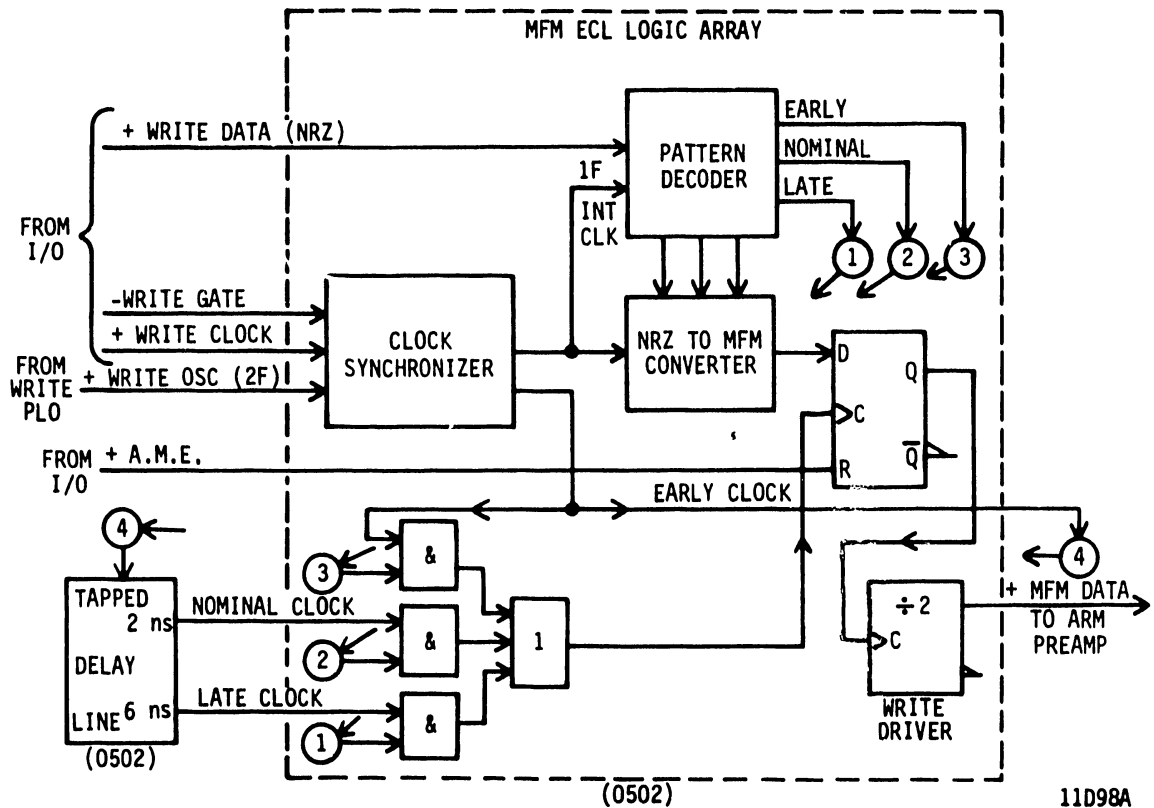
Figure 1-68. MFM Encoder and Write Compensation

The NRZ to MFM converter encodes MFM data following the rules outlined under Basic Read/Write Principles. For each required flux transition on the disk, the converter supplies a pulse to a D flip-flop. These pulses are clocked into the flip-flop by one of three clock signals, to compensate for the effects of peak shift. For each pulse, the gating circuitry selects the proper clock. The Early Clock is generated by the clock synchronizer. From the Early Clock, an external delay line develops the Nominal Clock and the Late Clock.

The rules for write compensation are as follows:

• When the pattern decoder identifies a 1000 pattern, a late clock is enabled for the MFM pulse occurring between the second and third bits.

- When the pattern decoder identifies an X011 pattern, a late clock is enabled for the MFM pulse on the third bit.

- When the pattern decoder identifies an X110 pattern, an early clock is enabled for the MFM pulse on the third bit.

- When the pattern decoder identifies a 0001 pattern, an early clock is enabled for the MFM pulse occurring between the second and third bits.

- For an MFM pulse resulting from other pattern decodes, a nominal clock is enabled.

With the NRZ to MFM converter supplying a D-input and the gating circuitry providing a clock input, the D flip-flop develops a pulse corresponding to each write transition on the disk. The leading edge of each pulse clocks a divide-by-two flip-flop (the write driver). The resulting +MFM Data signal is sent to the selected arm preamp. This signal toggles to produce a flux transition on the disk.

To write an address mark, the controller issues Tag 3 along with Bus bit 0 (Write Gate) and Bus bit 5 (Address Mark Enable). When the A.M.E. signal is active, the D flip-flop stays reset, and there are no flux transitions on the disk. In this case, a segment of the data track is erased.

Arm Preamp

Each head arm contains an LSI chip that serves as a preamp for the heads attached to that arm. The LSI chip selects a data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 1-69). These paragraphs concentrate on the preamp's write function and assume that head selection has occurred.

The LSI chip functions as a write driver when the -Write Enable line goes active (low). The -Write Enable line comes from the Control board and is active only when all the following are true:

- Write Gate is active

- Write Protect is not active

- No faults exist

- Speed OK is active

- Enable Power Amp signal is active

FROM CONTROL
BOARD INTERLOCKS -WRITE ENABLE

FROM MFM
ENCODER { + MFM DATA
           - MFM DATA

SELECTED
ARM PREAMP

WRITE
SELECT

SELECTED
READ/WRITE
HEAD

SELECTED
CURRENT
SWITCH
⚠1

(0902)

NOTES:

⚠1 PREAMP LOGIC IS SIMPLIFIED TO SHOW WRITE
    FUNCTION ONLY. REFER TO HEAD SELECTION
    DISCUSSION FOR THIS ASPECT OF R/W PREAMP
    OPERATION.
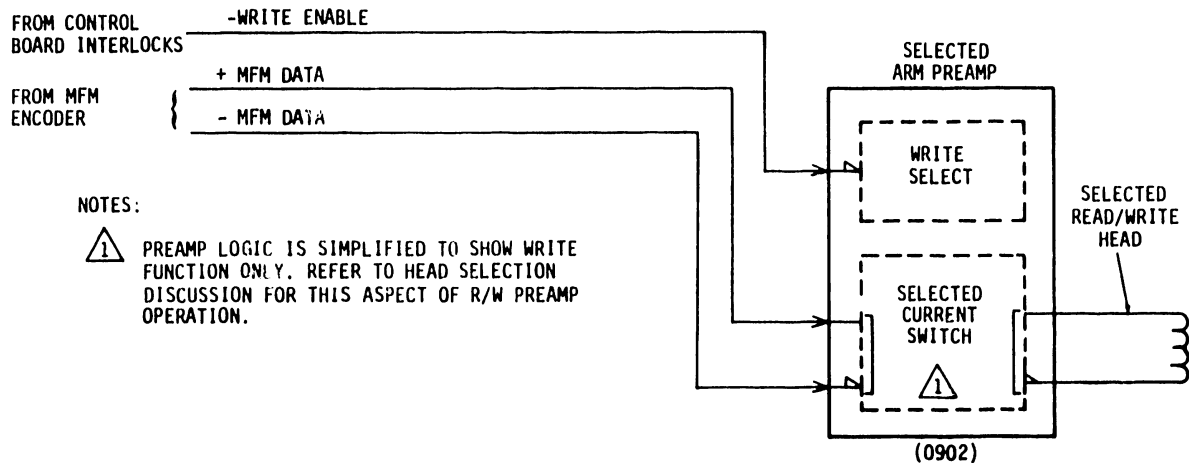
11D99A

Figure 1-69.   Arm Preamp

The chip develops regulated current for the selected head coil
and reverses the current in that coil to produce flux reversals
on the disk.

Throughout a write operation, write current is always flowing
through the head coil. The MFM ECL Logic Array inputs two MFM
Data lines to the selected Arm Preamp. When a transition oc-
curs on the input lines, the LSI chip switches the write cur-
rent direction through the head coil. This switching action
produces a recorded flux reversal on the disk surface.

While an address mark is being written, there is no switching
action, and an unchanging flux is recorded on the disk. Thus,
writing an address mark erases a segment of the data track.

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with
Bus bit 1 true. This enables the preamp circuits, which sense
the data written on the disk and generate analog read data sig-
nals.

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The analog data goes to the Data Latch circuit which changes it into digital MFM data.

The Read Comparator and PLO circuit generates a 19.34 MHz Read Clock signal that is phase-locked to the MFM read data. The MFM Decoder changes the MFM data to NRZ data synchronized to a 9.67 MHz Read Clock. Both data and clock are then sent to the controller.

Figure 1-70 shows the main elements in the read circuits and table 1-9 briefly describes each of these elements. The following paragraphs further describe the read circuits.

Arm Preamp

The Arm Preamp is an LSI chip that selects a data head on its head arm and either switches write current through the head or amplifies the read signal detected by the head. These paragraphs concentrate on the preamp's read function and assume that head selection has occurred.
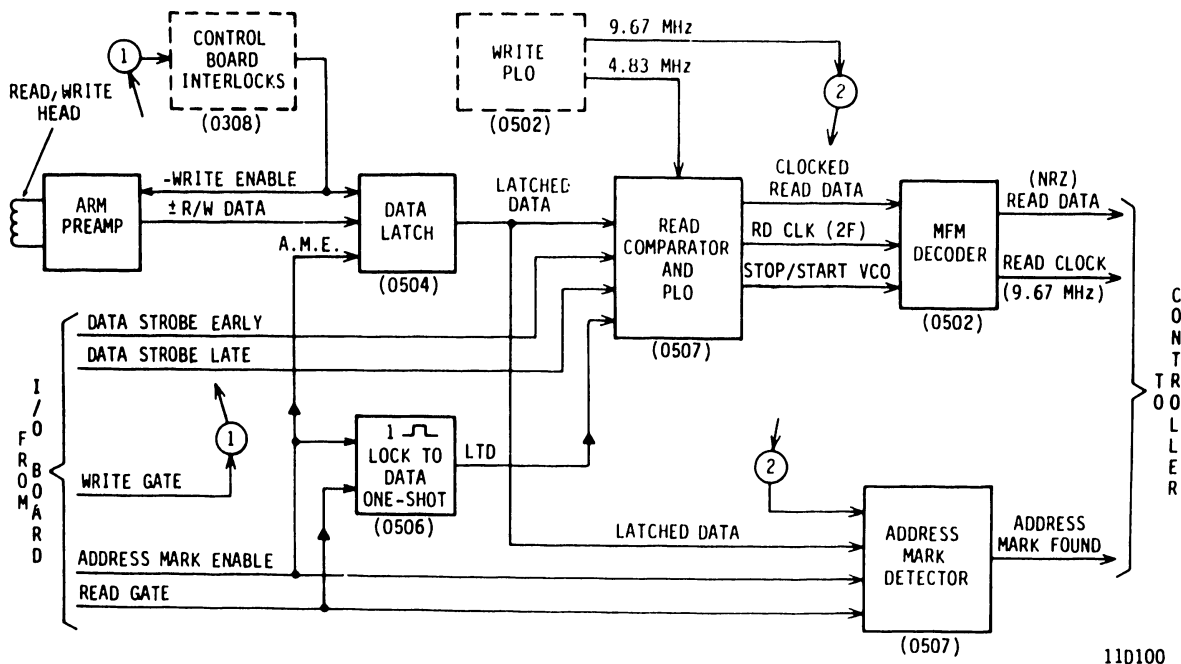
Figure 1-70. Read Circuits Block Diagram

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TABLE 1-9.   READ CIRCUIT FUNCTIONS

Circuit	Function
Arm Preamp	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog MFM data into digital MFM data. This data is sent to the Read Comparator circuit.
Read Comparator and PLO Circuit	Develops a 19.34 MHz Read Clock that is synchronized to MFM read data.
MFM Decoder	Translates data coding from MFM to NRZ modulation and generates 9.67 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 9.67 MHz Read Clock.
Address Mark Detector	Detects the address mark and transmits an Address Mark Found to the controller.

The LSI chip functions as a read preamp when the -Write Enable line is inactive (high). The chip contains a separate differential amplifier for each head, and head selection enables the differential amplifier associated with the desired head. In read operations, the coil in the selected head develops a readback pulse when the head passes over a written flux reversal on the disk. The readback pulse is supplied as a differential input to the preamp.

The differential amplifier selected in the chip amplifies the read signal and sends it on the Read Data lines to read circuitry on the Read/Write board.

Data Latch Circuit

The Data Latch circuit receives analog read data from the selected Arm Preamp and converts it into digital data. As shown in figure 1-71, most of the Data Latch circuit is located inside the Data Latch Analog Master Chip.
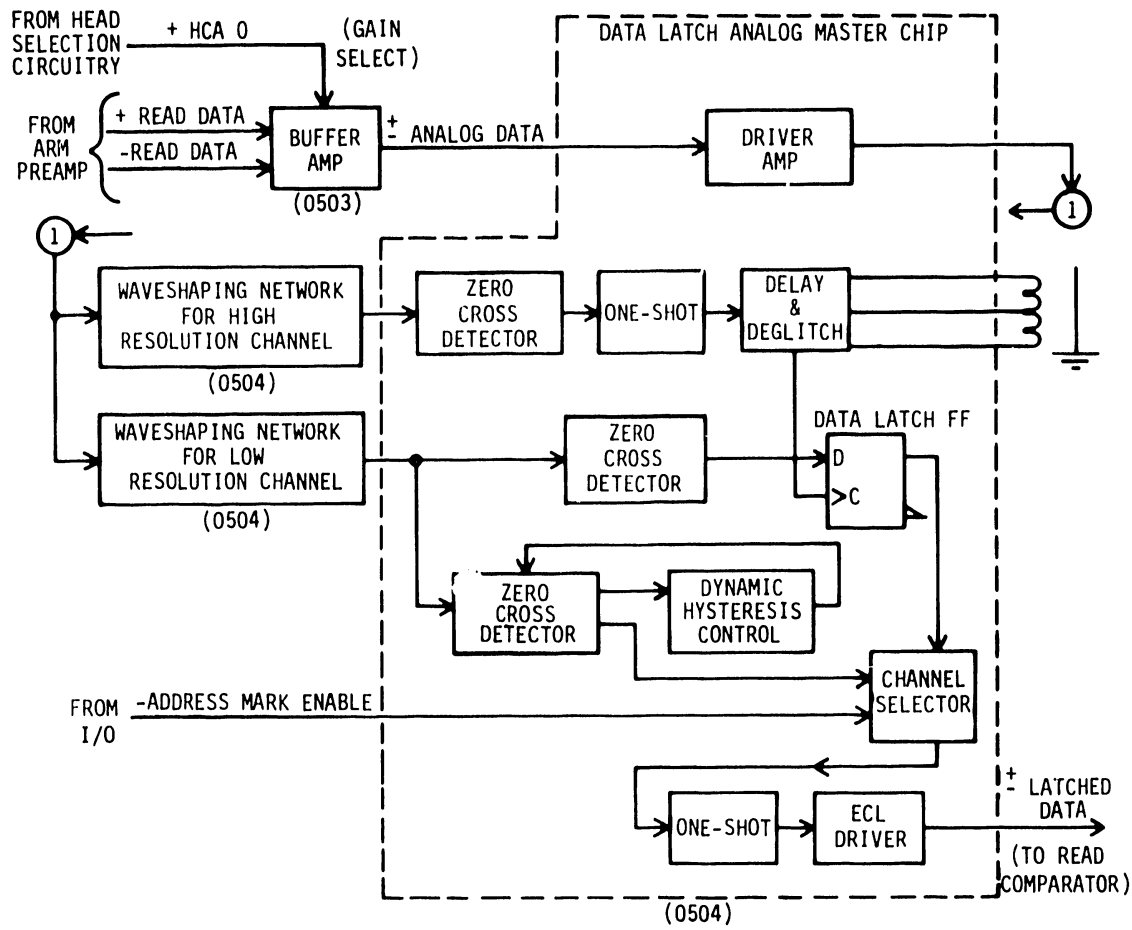
Figure 1-71. Data Latch Block Diagram

The input signal is amplified by the Buffer Amp, provided that
-Write Enable is inactive (high). The +HCA 0 line establishes
the gain of the Buffer Amp -- lower for outer heads or higher
for inner heads. After further amplification (inside the mas-
ter chip), the signal is split into three signal paths -- the
high resolution channel, the low resolution channel, and the
hysteresis channel. The high and low resolution channels con-
tain independent wave-shaping circuitry, and they provide sep-
arate inputs to the Data Latch FF. The high resolution channel
supplies delayed clock pulses to the Data Latch FF, and the low
resolution channel supplies a D-input to the Data Latch FF.
Successive clock pulses toggle the FF when the D-input has
changed. During normal write operations, a channel selector
sends the output of the Data Latch FF to a one-shot. For each
transition of the Data Latch FF, the one-shot pulses the
±Latched Data output lines. Thus, there is an output pulse for
each written flux transition sensed by the data head.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions. The low resolution channel uses a band-pass filter (with a 5 MHz bandwidth) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a band-pass filter (with a 13 MHz bandwidth) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the ±Latched Data output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when Address Mark Enable goes active, which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. With Address Mark Enable active, the channel selector in the master chip selects the output of the hysteresis channel for the ±Latched Data signal. Inside the master chip, the hysteresis channel contains a zero-cross detector and a dynamic hysteresis control circuit. To regulate operation of this zero-cross detector and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the output signal.

The ±Latched Data from the Data Latch circuitry is sent to the Read Comparator - Address Mark ECL Logic Array.

Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 19.34 MHz Read Clock, and processes latched read data from the Data Latch to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-72 is a simplified block diagram of the Read Compara-
tor and PLO circuitry. The phase-locked loop uses the Read Os-
cillator Control portion of the Read Comparator - Address Mark
ECL Logic Array to regulate operation of the Current Pump and
to provide stop/start control of the Voltage-Controlled Oscil-
lator (VCO). The Current Pump supplies a Control Voltage sig-
nal to the VCO that determines the frequency of the 2F RD OSC
signal output from the VCO. The 2F RD OSC signal is fed back
to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two
reference signals. When the drive is reading data (-Read Gate
and AME low), the phase-locked loop uses the pulse train on the
Latched Data line as a timing reference. In this case, the
Read Oscillator Control uses a quadrature comparator to drive
the Pump Up and Pump Down lines as necessary to keep the rising
edges of the 2F RD OSC signal coincident with the rising edges
of +Latched Data pulses. For each Latched Data pulse, the
quadrature comparator outputs a variable-length pulse on the
Pump Up line, followed by a fixed-length pulse on the Pump Down
line. When the Pump Up and Pump Down pulses differ in length,
the Control Voltage to the VCO varies accordingly to phase
shift the VCO and bring it into phase lock.

When the drive is not reading data (-Read Gate high or AME
high), the phase-locked loop maintains the VCO frequency close
to the value it has during read operations. In this mode, a
coincidence comparator in the ECL Logic Array monitors the
phase difference between the 4.83 MHz WRT OSC signal (derived
from the Write PLO) and the 2F RD OSC signal fed back from the
VCO. When the rising edge of the 4.83 MHz signal leads the
rising edge of the 2F signal, this comparator pulses the Pump
Up line to increase the Read VCO frequency. Conversely, when
the rising edge of the 4.83 MHz signal lags the rising edge of
the 2F signal, this comparator pulses the Pump Down line to de-
crease the Read VCO frequency.

The Read Oscillator Control circuitry uses the Stop/Start VCO
line to control VCO operation while switching between the
quadrature and coincidence comparators. The Stop/Start VCO
line goes active for approximately 200 ns after the Latched
Data pulse following a change in the Read Gate signal. While
the Stop/Start VCO line is active, the VCO is inhibited, and
its control voltage is held constant. This enables the Read
PLO to phase lock within 2 microseconds during the switching
transitions.

Figure 1-72. Read Comparator and PLO Block Diagram

The Data Discriminator portion of the Read Comparator - Address Mark ECL Logic Array conditions the (2F) Read Clock and Clocked Read Data signals for use in the MFM Decoder (see figure 1-72). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (51 ns), and positive transitions of the (2F) Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control Select) with Bus bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data, 2F Read Clock, and Stop/Start VCO signals are input to the MFM Decoder, which converts the read data from MFM code into NRZ form and generates the 9.67 MHz Read Clock.

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MFM Decoder

The MFM Decoder converts MFM data into NRZ data and generates
the 9.67 MHz Read Clock from the 19.34 MHz Read Clock. Both
inputs, the MFM data and the 19.34 MHz Read Clock, come from
the Read Comparator and PLO circuitry.

The MFM decoding function takes place within a single ECL Logic
Array, the MFM ECL Logic Array, as shown in figure 1-73. The
decoder consists of a clock synchronizer and divide-by-two
flip-flop, and an MFM to NRZ converter.

The clock synchronizer develops two clocks -- the Internal 1F
Clock signal and the 9.67 MHz Read Clock. Both clocks are de-
rived by dividing the RD CLK (2F) signal by two. This timing
circuitry is synchronized when the Read Comparator circuit de-
activates the Stop/Start VCO signal. The clock synchronizer
selects which edges of the 2F signal determine the transitions
of the 1F signals. The synchronizing process requires that the
RD CLK (2F) signal is locked to an all-zeros data pattern.
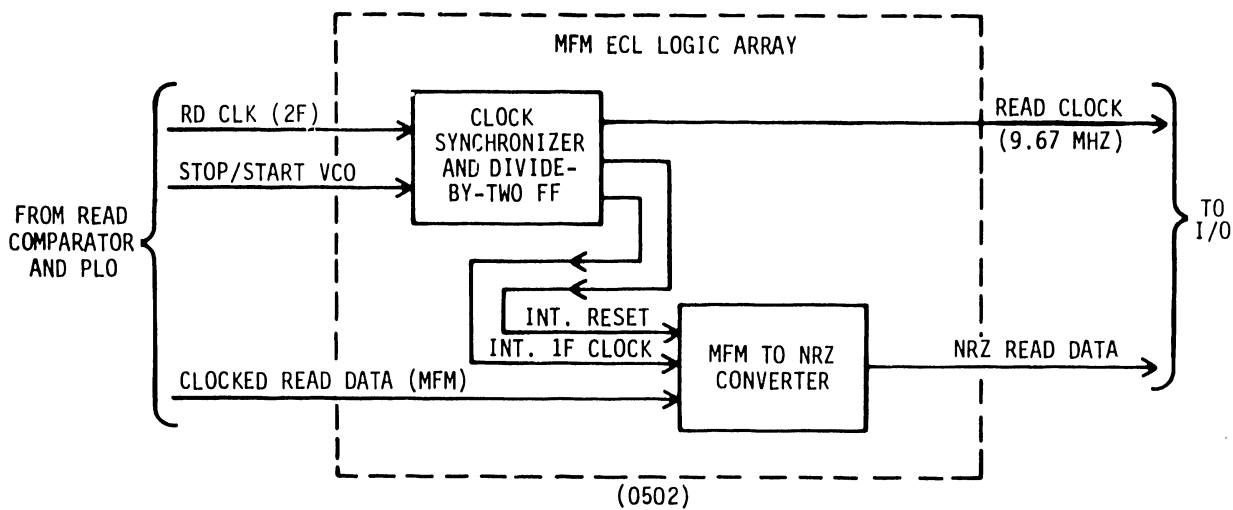
Figure 1-73. MFM Decoder Block Diagram

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In addition to providing a 1F Internal Clock, the clock synchronizer supplies an Internal Reset signal to the MFM to NRZ converter during the synchronizing process. The converter is enabled once this reset signal goes inactive.

The NRZ to MFM converter uses the phase relationship between the Internal 1F Clock signal and the Clocked Read Data signal to output NRZ Read Data. If the Clocked Read Data signal is active when the Internal 1F Clock goes high, this indicates an NRZ "1" and the NRZ Read Data line stays active for 103 ns. If the Clocked Read Data signal is inactive when the Internal 1F Clock goes high, this indicates an NRZ "0" and the NRZ Read Data line stays inactive for 103 ns.

The MFM Decoder sends the ±NRZ Read Data and ±Read Clock outputs to the I/O board to be transmitted on the interface to the controller.

Address Mark Detection

The Address Mark Detector, which is part of the Read Comparator - Address Mark ECL Logic Array, monitors the Latched Data signal from the Data Latch during an address mark search. If a gap of 2.1 to 3.6 microseconds is detected between incoming read pulses, the detector sets the Address Mark Found line, and the I/O circuitry sets the Address Mark line on the interface.

Figure 1-74 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus bits 1 and 5 active. In this situation, the -Read Gate line is low and the AME line is high. Together, these two signal inputs enable the Address Mark Detector.

The detector contains a counter circuit which is driven by the 9.67 MHz Clock signal from the Write PLO until it is reset by incoming read pulses. If the counter is clocked up over an interval from 20 to 36 clock periods, the Address Mark Found line is set. This line remains set until the lock-to-data interval ends (3 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.

The detector also contains a discriminator that distinguishes between read data gaps, caused by media defects, and gaps indicating address marks. If a defect is crossed, the discriminator inhibits the Address Mark Found output.

```
               ┌─────────────────────────────┐
               │     READ COMP - ADD MK       │
               │      ECL LOGIC ARRAY          │
        AME+(RD•LTD)  ┌ ─ ─ ─ ─ ─ ─ ─ ─ ┐
        ──────────────────→│               │
FROM WRT PLO─9.67 MHz CLOCK │               │
        ──────────────────→│   ADDRESS      │
FROM DATA LATCH─LATCHED DATA│   MARK         │ ADDRESS MARK FOUND   TO
        ──────────────────→│   DETECTOR     │─────────────────────→ I/O
FROM I/O ──────-RD GATE     │               │
        ──────────────────→│               │
           -LTD            │               │
        ──────────────────→└ ─ ─ ─ ─ ─ ─ ─ ┘
               └─────────────────────────────┘
                         (0507)
```
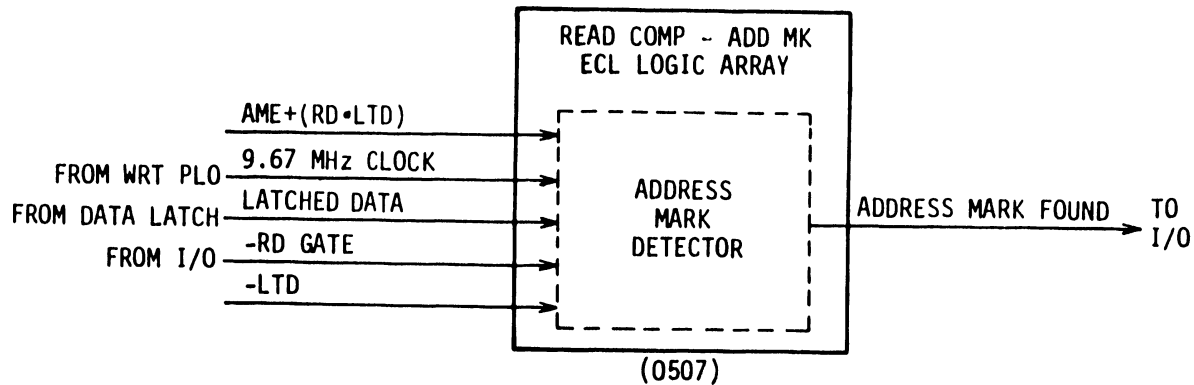
                                                      11D104

Figure 1-74.   Address Mark Detector Block Diagram

FAULT AND ERROR CONDITIONS

GENERAL

The following paragraphs describe those conditions which are
interpreted by the drive as errors. These errors are divided
into two categories: (1) those that generate the Fault signal
and (2) those that do not generate the Fault signal. Included
in the following descriptions are a list of conditions that
produce each error status, the effect of that status on drive
operation, and actions that clear the status indication to re-
turn the drive to normal operation.

ERRORS INDICATED BY FAULT SIGNAL

General

The drive has monitoring circuitry that recognizes six types of
error conditions. When any of these error conditions occurs,
it sets the respective latch in the I/O Gate Array. An OR cir-
cuit in the gate array receives inputs from the six latches;
if one or more of the latches is set, the OR circuit activates
the Fault line. The Fault line remains active until the
latches are cleared.

When the Fault line goes active, it lights the FAULT indicator on the operator panel, disables write operations, and issues Fault and Write Protected status to the controller. The active Fault line interrupts the MPU at PIA-0 (see figure 1-75). The MPU responds by dropping the Ready signal and by communicating with the I/O Gate Array to identify the fault. The Unit Ready line to the controller goes inactive, and the Ready indicator on the operator panel flashes until the fault is cleared.

Communication between the MPU and the I/O Gate Array takes place via I/O Control lines 1-3. Upon receiving the Fault interrupt, the MPU pulses I/O Control lines 1 and 2 to operate a multiplexer inside the gate array. The multiplexer's inputs include the six fault latches inside the gate array, and its output is carried by the I/O Control 3 line to a driver chip monitored by the MPU. There are six individual fault LEDs on the Fault Display board, each corresponding to a fault latch in the gate array. Having read the status of the latches, the MPU lights the corresponding LED(s) via outputs of PIA-2.

Provided the error condition or conditions no longer exist, the Fault signal is cleared by the following:

- Controller Fault Clear command (Tag 3 with Bus bit 4)

- Fault Clear switch on operator panel

- Powering down the drive

The controller Fault Clear command is decoded inside the I/O Gate Array to develop a reset input for the six latches. When the Fault Clear switch is pressed, it interrupts the MPU at PIA-2. The MPU responds by pulsing the I/O Control 1 and 2 lines with a code that develops a reset input for the six latches. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power sequence, and any pre-existing fault status is lost.

The following paragraphs describe the individual fault conditions which set each of the latches in the I/O Gate Array and thus activate the Fault signal.

Voltage or Actuator Current Fault

This fault is generated whenever either the ± 15 or ± 5 voltages are detected to be below satisfactory operating levels or the actuator current exceeds an allowable level. Threshold detec-
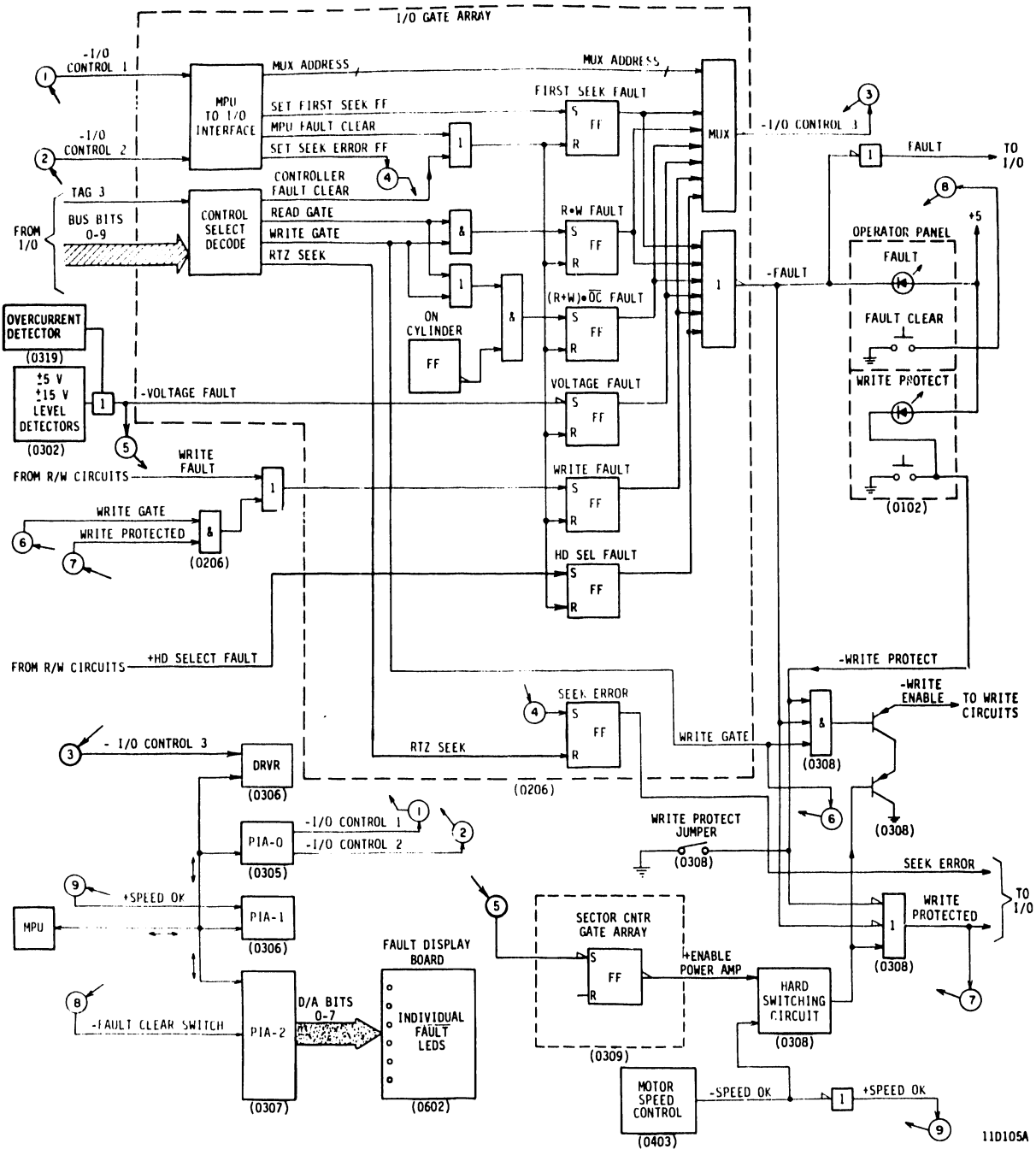
Figure 1-75. Fault and Error Detection Circuitry

tors on the Control board activate the Overcurrent line if the actuator current reaches 5.9 amperes or activate the Voltage Fault line if any of the following voltages drop:

- The +15 V supply drops to 14.35 V.

- The +5 V supply drops to 4.83 V.

- The -5 V supply drops to -4.90 V.

- The -15 V supply drops to -14.46 V.

These two lines, Overcurrent and Voltage Fault, are ORed to develop the -(Voltage + Actuator Current) Fault signal. When this signal goes low, it sets the individual fault latch in the I/O Gate Array and latches the Enable Power Amp signal inactive in the Sector Counter Gate Array. When the Enable Power Amp signal is inactive, it adds an additional degree of write protection, needed to safeguard existing data on the disks by inhibiting the write circuitry while a voltage problem exists. A hard switching circuit deactivates the -Write Enable line when the +Enable Power Amp line is low and keeps it inactive for about 1/2 second after that line is reactivated. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

An additional voltage detector circuit detects when the +5 V supply drops to 4.73 V, making MPU operation unreliable. This condition generates a -Low Vcc signal to produce the Reset signal for the MPU chips and the DC Master Clear signal for the gate arrays. Also, when the Low Vcc signal goes active, the -Disable Retract Power line goes low to produce an emergency retract of the actuator.

Read or Write and Off Cylinder

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write gate from the controller. The I/O Gate Array decodes both gates from Tag 3 commands and contains the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault

A write fault is encoded if any of the following conditions exist:

- Write Gate received while drive is in Write Protected mode

- Write Clock not present when Write Gate is active

- No write data transitions when the Write Gate is active (except when the Address Mark Enable signal is active)

- Head open (bad head detected)

- No Arm Enable signal is active when Write Enable is active.

All conditions except the first one activate the Write Fault line coming from the Read/Write board. Gating circuitry on the Read/Write board develops the Write Fault signal when individual fault conditions are detected, provided that Write Enable is active and Address Mark Enable is inactive. The gating circuitry keeps the Write Fault line inactive during transitions between read and write operation. The Write Fault line or the combination of Write Protect and Write Gate lines active sets the associated latch in the I/O Gate Array.

Head Select Fault

This fault is generated when more than one head is selected during a write operation. When this condition is detected, it sets the associated latch in the I/O Gate Array.

Read and Write Fault

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected internally in the I/O Gate Array to set the associated latch.

First Seek Fault

First Seek fault, as opposed to Seek Error, results from error conditions that occur during power on initialization and the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. First Seek faults generate an active Fault signal while Seek Errors activate the Seek Error and Seek End lines to the controller. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

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Unlike the other individual fault latches, the latch for First Seek fault is set by the MPU. To set the latch, the MPU inputs the I/O Gate Array with a specific pulse code on I/O Control lines 1 and 2. The error conditions resulting in a First Seek fault are monitored by the MPU during the power on initialization and load operation. Assuming that the MPU is operational, it sets the associated latch in the I/O Gate Array if any of the following tests fail:

- Demodulator Active is inactive at the start of the load, but goes active after the heads move inward from the landing zone. Demodulator Active must remain stable throughout the rest of the load.

- The Fault line stays inactive during the load.

- The MPU moves the heads out of the landing zone and detects 100 cylinder pulses before a timeout occurs.

- At least one cylinder pulse is detected in the outer guard band as the heads approach track zero.

- During the first 2.1 ms of track-following, less than three cylinder pulses are detected.

- In the 11 ms interval allowed during track-following if On Cylinder Sense goes inactive, this signal returns to the active level, and less than three cylinder pulses are detected.

- No seek error occurs during the scan cycle or velocity calibration procedure.

The MPU aborts the load operation when a First Seek fault is indicated. Although a controller Fault Clear command will reset the Fault signal, the MPU waits until the operator panel Fault Clear switch is pressed before attempting another load.

ERRORS NOT INDICATED BY FAULT SIGNAL

General

Two types of errors do not generate the Fault status -- seek errors and the motor speed error. The seek error has an associated status FF, while the motor speed error does not.

Motor Speed Error

The -Speed OK signal is developed by circuitry in the Motor Control Gate Array on the Motor Speed Control board. When the spindle speed falls below 3564 r/min, the -Speed OK signal goes high. The -Speed OK signal is used by several circuits on the Control board (see figure 1-75), and these uses are outlined in the following paragraphs.

An interlock circuit monitors the -Speed OK line to provide write protection if the line goes high. Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. A hard switching circuit deactivates the -Write Enable line when -Speed OK goes high and keeps it inactive for about 1/2 second after -Speed OK goes low again.

The MPU monitors the +Speed OK signal at PIA-1. If the +Speed OK signal goes low, the MPU drops the Ready signal, and it retracts and locks the actuator. The MPU then initiates a sequence to restore motor speed.

The MPU has two methods for restoring motor speed when -Speed OK goes high. The MPU checks the +Motor Fault line at PIA-1. If +Motor Fault is active, the MPU drops and then issues the Motor Run command in order to reset the motor fault circuitry in the Motor Control Gate Array. If +Motor Fault is inactive, the MPU keeps the Motor Run command active and tries to bring the motor back up to speed. In either case, the MPU drops the Unit Ready signal to the controller during the low speed condition.

Seek Error

Seek Error is a status signal sent to the controller indicating error conditions that occur during normal seeks and RTZ seeks. The Seek Error signal is active when the Seek Error FF, located in the I/O Gate Array, is set.

During normal seeks and RTZ seeks, the MPU tests certain error conditions. If any tests fail, the MPU sets the Seek Error FF in the I/O Gate Array. These tests include the following:

- The new cylinder address, specified by the controller for a normal seek, is less than or equal to 710.

- The Demodulator Active signal is active at the start and end of normal seeks, and it is active throughout RTZ seeks.

- Fault stays inactive throughout seeks.

- The time required for a normal seek is less than the 60 ms timeout allowed by the MPU.

- During the first 2.1 ms of track-following, less than three cylinder pulses are detected (normal or RTZ seeks).

- In the 11 ms interval allowed during track-following if On Cylinder Sense goes inactive, this signal returns to the active level, and less than three cylinder pulses are detected.

- Less than three guard band pulses are detected at PIA-1 during one seek. Inner and outer guard band pulses are counted in normal seeks. Only inner guard band pulses are counted during RTZ seeks.

If any of these tests fails, the MPU sets the Seek Error FF using I/O Control lines 1 and 2 (see figure 1-75). The MPU also sets the Seek Error FF after getting a reset input to force it out of a hang condition. This causes both the Seek Error and Seek End status signals to be sent to the controller via the I/O transmitters.

In the event of a Seek Error, the MPU drops all servo commands, allowing the heads to remain in their current position over the disks. The seek error condition cannot be cleared except by a controller RTZ command. An attempt by the controller to perform a read or write operation while the seek error condition exists will result in the generation of a Read or Write and Off Cylinder fault.

SECTION 2
GENERAL MAINT-
ENANCE
INFOR-
MATION

2. GENERAL MAINTENANCE INFORMATION

INTRODUCTION

This section contains general information relating to maintenance of the drive. A person performing maintenance should be familiar with the information in this section in addition to being thoroughly familiar with drive operation. Information is divided into the following areas:

- Warnings and Precautions - Lists warnings and precautions that must be observed when working on the drive.

- Electrostatic Discharge Protection - Provides instructions for the proper handling of electrostatically sensitive devices.

- Maintenance Tools and Materials - Lists the tools and materials required to perform maintenance on the drive.

- Testing the Drive - Provides information concerning the electrical testing of the drive.

- Accessing Assemblies for Maintenance - Identifies the various parts of the drive and describes how to access these parts for maintenance.

WARNINGS AND PRECAUTIONS

WARNING

The following topic provides warnings and precautions that must be observed during maintenance. Refer also to Important Safety Information and Precautions located in the front of this manual following the table of contents. Failure to observe the warnings, precautions, and other safety information provided in this manual could result in personal injury.

Observe the following warnings and precautions at all times. Failure to do so may cause equipment damage and/or personal injury.

- Use care while working with the power supply because line voltages are present.

- Do not attempt to disassemble the module. It is not field repairable. Replace the entire module assembly if it is found to be defective.

- Do not operate the drive over an extended period of time without the top cover installed.

- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical components.

- Observe the precautions listed under Electrostatic Discharge Protection.

- If the power supply is placed on a bench for testing, position the supply so that all ventilation holes are open, to allow proper air flow to internal components.

ELECTROSTATIC DISCHARGE PROTECTION

All drive electronic assemblies are sensitive to static electricity, due to the electrostatically sensitive devices used within the drive circuitry. Although some of these devices such as metal-oxide semiconductors are extremely sensitive, all semiconductors as well as some resistors and capacitors may be damaged or degraded by exposure to static electricity.

Electrostatic damage to electronic devices may be caused by a direct discharge of a charged conductor, or by exposure to the static fields which surround charged objects. To avoid damage to drive electronic assemblies, service personnel must observe the following precautions when servicing the drive:

- Ground yourself to the drive - whenever the drive electronics are or will be exposed, connect yourself to ground with a wrist strap (see table 2-1). Connection may be made to any metal assembly or to the ground jack at the rear of the drive. As a general rule, remember that you, the drive, and the circuit boards must all be at ground potential to avoid potentially damaging static discharges.

- Keep boards in conductive bags - when circuit boards are not installed in the drive, keep them in conductive static shielding bags (see table 2-1). These bags provide absolute protection from direct static discharge and from static fields surrounding charged objects. Remember that these bags are conductive and should not be placed where they might cause an electrical short circuit.

- Remove boards from bags only when you are grounded - all boards received from the factory are in static shielding bags, and should not be removed unless you are grounded.

- Turn off power to drive before removing or installing any circuit boards.

- Never use an ohmmeter on any circuit boards.

MAINTENANCE TOOLS AND MATERIALS

The maintenance procedures described in this manual require the use of certain special tools, test equipment, and materials. These are listed in table 2-1 along with the appropriate CDC part number. Note that the list includes only special tools. It is assumed that the service person has normal maintenance tools.

Use of the items listed in table 2-1 is described in the procedures in which they are required. Additional information is provided on the __UQX fault display board (see section 3, Trouble Analysis) and the field test unit (see Testing the Drive).

TESTING THE DRIVE

GENERAL

During testing and troubleshooting the drive is normally required to perform various operations such as reading and writing test data. Either a field test unit or system software can be used to control the drive during these operations.

FIELD TEST UNITS

Either the TB2A3A programmable field test unit (PFTU) or the TB216A field test unit (FTU) can be used to test the 340 MB (PA5G1/2) drive. Only the TB2A3A programmable field test unit (PFTU) can be used to test the 515 MB (PA5N1/2) drive. See table 2-1 for tester part numbers. The tester allows the drive to be operated and controlled independent of the rest of the system. The following, outlines the procedure for connecting the tester to the drive. For specific instructions on connecting and operating the tester, see the PFTU or FTU manual.

TABLE 2-1.   MAINTENANCE TOOLS AND MATERIALS

Description	Part Number
Brake Adjust Shim	CDC 15363045
Field Test Unit (TB216A)	CDC 82338800
Programmable Field Test Unit (TB2A3A with SMD-0 options)	CDC 95614711
Motor Removal Tool	CDC 83350262
Oscilloscope, Dual Trace	Tektronix 475A or equivalent
Scope Probe Tip (Hatchet type)	CDC 12212885
Shipping Damper Adjustment Tool (4 required)	CDC 15363102
Solenoid Wrench	CDC 83350362
Static Shielding Bags and Ground Wrist Straps	See Accessories in Parts Data (Section 4 of Hardware Mainte nance, Volume 1)
Volt/ohmmeter	Ballantine 345 or equivalent digital volt- meter

CAUTION

To avoid possible damage to interface circuit-
ry, always deenergize drive, controller, and
tester before removing or installing I/O ca-
bles.

During testing, the PFTU or FTU I/O cables must be connected to
the drive in place of the system I/O cables. Before discon-
necting the system I/O cables, disable the controller and set
power supply circuit breaker CB1 to the OFF position. In a
daisy chain system, power off all the drives.

When the drive is powered down, remove the system I/O cables
from the drive to be tested. Connect the PFTU or FTU A cable
to drive connector J3 and the PFTU or FTU B cable to drive con-
nector J2. Connect a terminator to drive connector J4. See
the installation section of hardware maintenance volume 1 for
the terminator and its part number. In a daisy chain system,
make whatever connections are necessary to ensure that the
other drives remain under system control, and restore power to
the other drives.

At the completion of testing, restore the drive to normal oper-
ation by reversing the process outlined above.

DRIVE DIAGNOSTICS

The drive has built in diagnostic tests. These diagnostic
tests may be performed via the fault display board (_UQX), lo-
cated behind the drive front panel insert. See section 3,
Trouble Analysis for operating instructions.

SYSTEM SOFTWARE

The drive may also be tested by use of system diagnostic test
programs. This requires use of the controller and the appro-
priate software. In this type of testing, the drive communi-
cates with the controller as in normal online operations, and
special I/O connections are unnecessary.

Refer to manuals or other documentation applicable to the spe-
cific system or subsystem for information concerning the system
software routines.

IDENTIFYING TEST POINTS

The drive circuit boards have test points to aid in signal
tracing during maintenance and troubleshooting. These test
points appear, physically, as shown on figure 2-1 and may be
located anywhere on the component side of the circuit boards.
Most test points on the __VCX (control board) and __SYX/__TQX
(dual and single channel I/O boards) are located at top edge of
board (see figure 2-3 for exact locations. The logic diagrams
show the test points schematically.

The diagrams and maintenance procedures identify a test point
by referring to a connector or the coordinate locator code and
in some cases letter designator. J81-1 is an example of test
point reference where, J81 is the connector and 1 is the pin
number. TP-G620 (B) is an example of a test point reference
where, G620 is the component locator and "B" is the letter des-
ignator. The coordinate locator code indicates where the test
point is located on the board. The introduction to diagrams
section explains how to use the locators. The letter and con-
nector designators are letters, silkscreened onto the board.
The coordinate locators progress in alphabetical order from
left to right and top to bottom (see figure 2-2). Not all test
points have letter designators. In the procedures, the letter
designator is always in parenthesis, following the locator code.
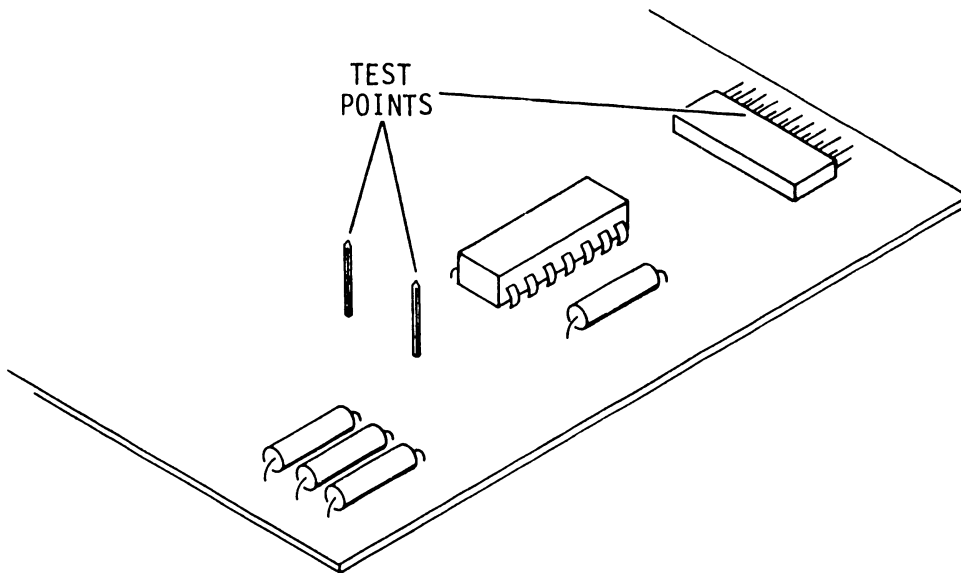
10R109 A

Figure 2-1.   Test Points
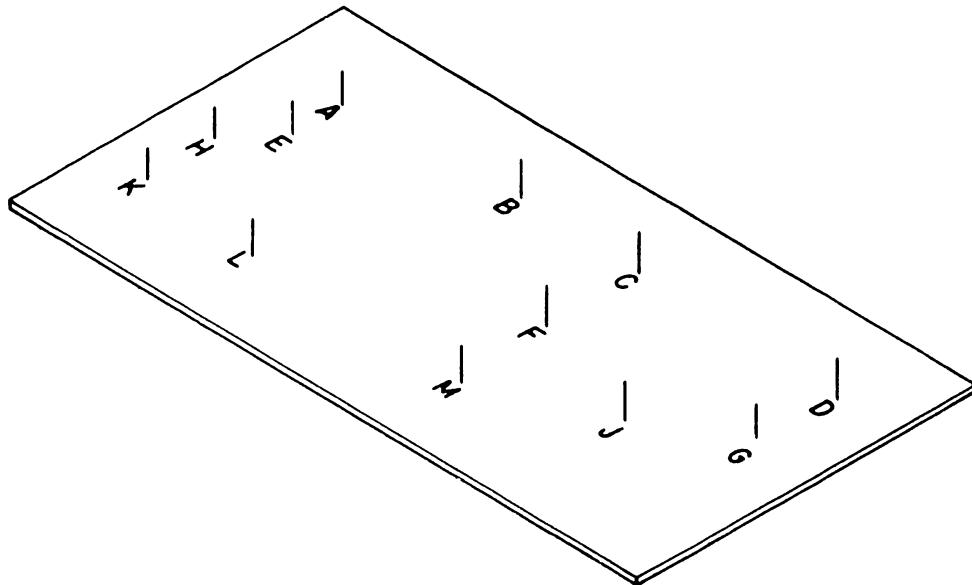
10R110

Figure 2-2. Test Point Letter Designators

ACCESSING ASSEMBLIES FOR MAINTENANCE

The major drive assemblies and components are shown on figure 2-3. These parts are accessed by extending the drive on its slides and removing the top cover.

Extend the drive by using a screwdriver or similar tool to lift the cabinet latch (see figure 2-3), and pulling the drive forward. When extending the drive, exercise caution to ensure that the equipment rack remains stable. Also, take care that the system cabling is not damaged when sliding the drive in and out of the rack.

If it is necessary to remove the drive from the slides, see entire drive removal procedure in section 5 of this manual. Section 5 also contains a top cover removal procedure and procedures for removing most of the other field replaceable parts, including the circuit boards.

Extending the drive and removing the top cover allows access to most circuit board test points. As shown on figure 2-3 the _SYX/_TQX (single and dual channel I/O boards), _UGX/_VHX[1] (340 and 515 MB read/write boards) and _VCX (control board) are readily accessible. The _SWX (power amp/motor control board) is mounted at the rear of the drive. The _STX (servo and read/write preamp board), is located within the module and cannot be serviced.

There are two types of power supplies available with the drive. One type is referred to as an integral power supply. The other type is referred to as a remote power supply (see figure 2-3). The integral power supply is attached to the drive rear panel and shipping bracket (inner rail if drive is slide mounted). The remote power supply can be attached to the inner rail (directly behind the drive) or other remote location, provided clearance for proper air flow is available.

---

[1]Older 515 MB drives used a _SUX read/write board.

Figure 2-3. Component Locator (Sheet 1 of 7)

Labels in figure:

TOP COVER

SUPPORT BRACKET

⟨3⟩ _UGX/_VHX BOARD (READ/WRITE)

⟨1⟩ FAULT DISPLAY BOARD _UQX

⟨2⟩ MODULE

GROUND JACK

⟨1⟩ FRONT PANEL INSERT

FRONT PANEL

OPERATOR PANEL (_PBX)

BRAKE

CARRIAGE LOCKING SOLENOID

_SWX BOARD (MOTOR SPEED CONTROL AND POWER AMP)

NOTES:

⟨1⟩ FILTER AND _UQX ARE BEHIND INSERT.

⟨2⟩ _STX (SERVO AND READ/WRITE PREAMP ARE IN MODULE)

⟨3⟩ _UGX USED ON 340 MB DRIVE
_VHX USED ON NEWER 515 MB DRIVES.
_SUX USED ON OLDER 515 MB DRIVES.

11D106A

TERMINATOR
GROUND

②
I/O CABLE PLATE

J3 J4 J2

③

④
_SYX/_TQX
(I/O BOARD)

FAN

_SVX
(MOTHER BOARD)

_VCX
(CONTROL BOARD)

①
CABINET
LATCH

NOTES:

① LIFT LATCH TO EXTEND DRIVE.

② LOCATED AT REAR OF INTEGRAL POWER SUPPLY
   OR REAR PANEL OF DRIVE, WHEN REMOTE
   POWER SUPPLY IS USED.

③ INSTALL TERMINATORS ON J4 FOR EACH CHANNEL.

④ _SYX USED ON SINGLE CHANNEL DRIVE.
   _TQX USED ON DUAL CHANNEL DRIVE.

11D107A

Figure 2-3. Component Locator (Sheet 2)

(BOTTOM VIEW)

CB4 -5V

CB3 +24V

CB2 -24V

CIRCUIT BREAKER CB1

DC PWR CORD
(J15 DC PWR OUT)

(FRONT VIEW)

CIRCUIT
BREAKERS △1
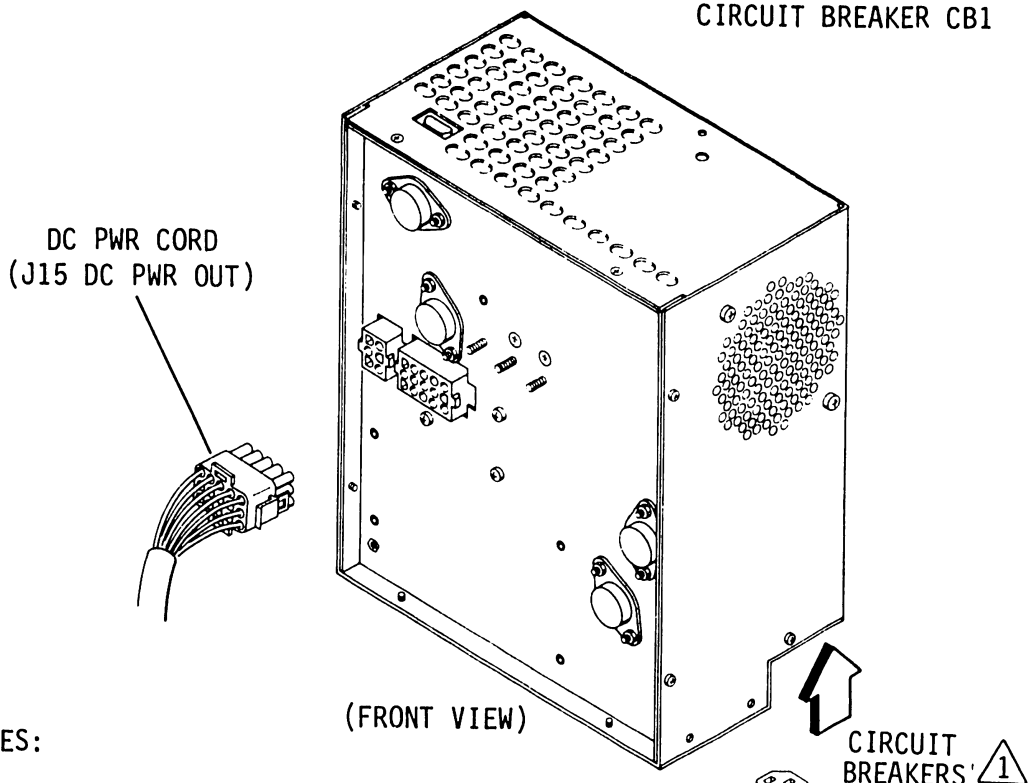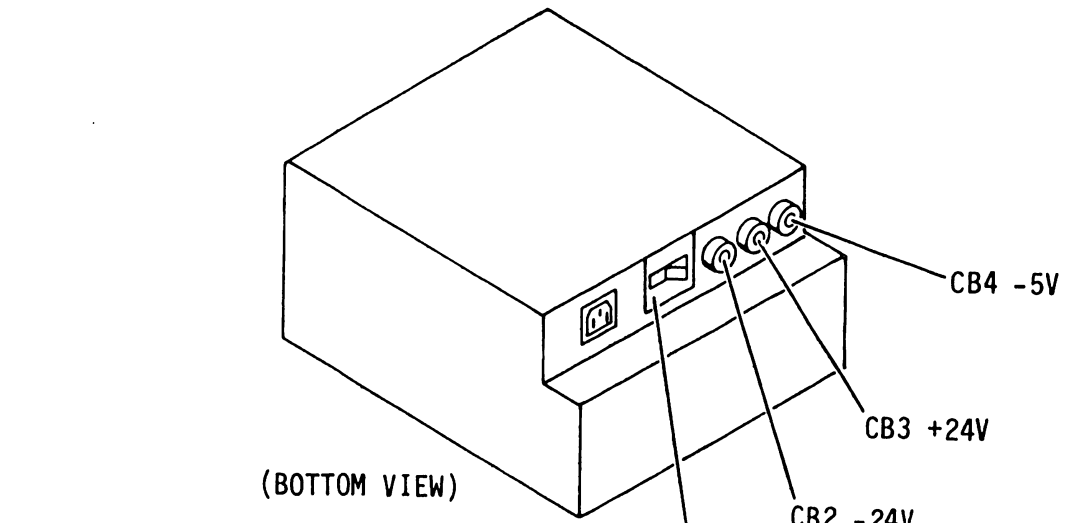
NOTES:

△1 SEE OPERATION SECTION
OF MAINT. VOL. 1

REMOTE POWER SUPPLY

AC PWR CORD
(J1 AC PWR IN)

11D108

Figure 2-3. Component Locator (Sheet 3)

VOLTAGE PROGRAMMING SWITCH

CIRCUIT BREAKER CB1

CB4 -5V

CB3 +24V

CB2 -24V

AC PWR CORD
(J1 AC PWR IN)

J1

I/O CABLE PLATE

(REAR VIEW)
⚠1
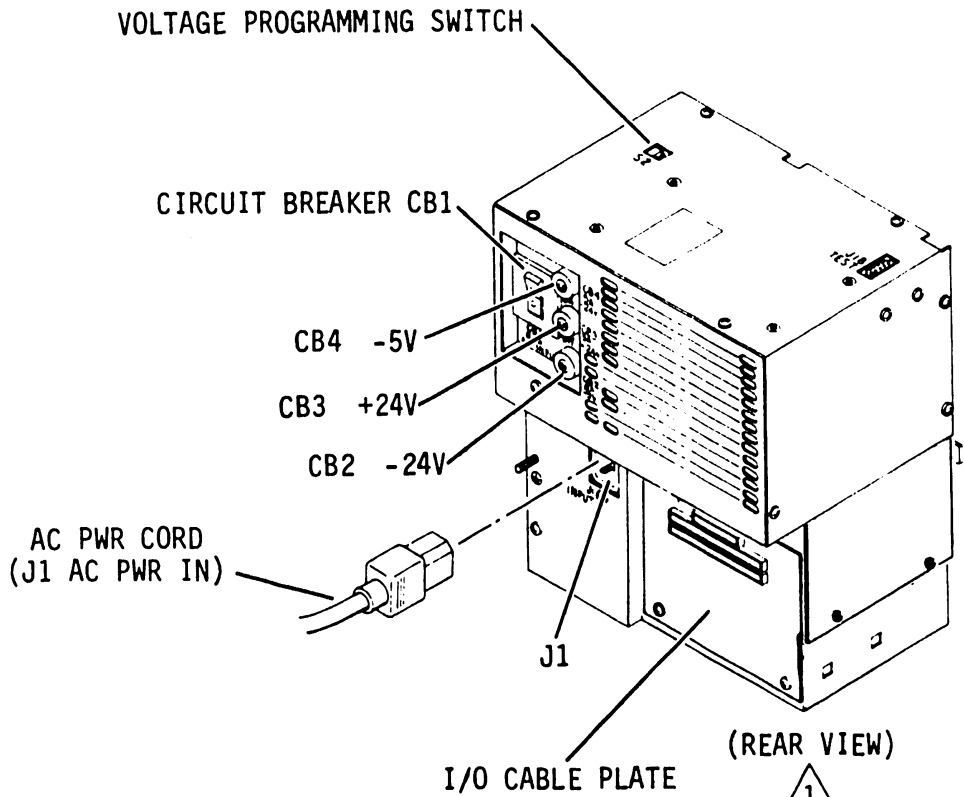
NOTES:

⚠1 POWER SUPPLY IS MOUNTED
ON REAR OF DRIVE.

DC PWR CORD
(P15 DC PWR OUT)

P35 TO
MOTHER BOARD

(FRONT VIEW)
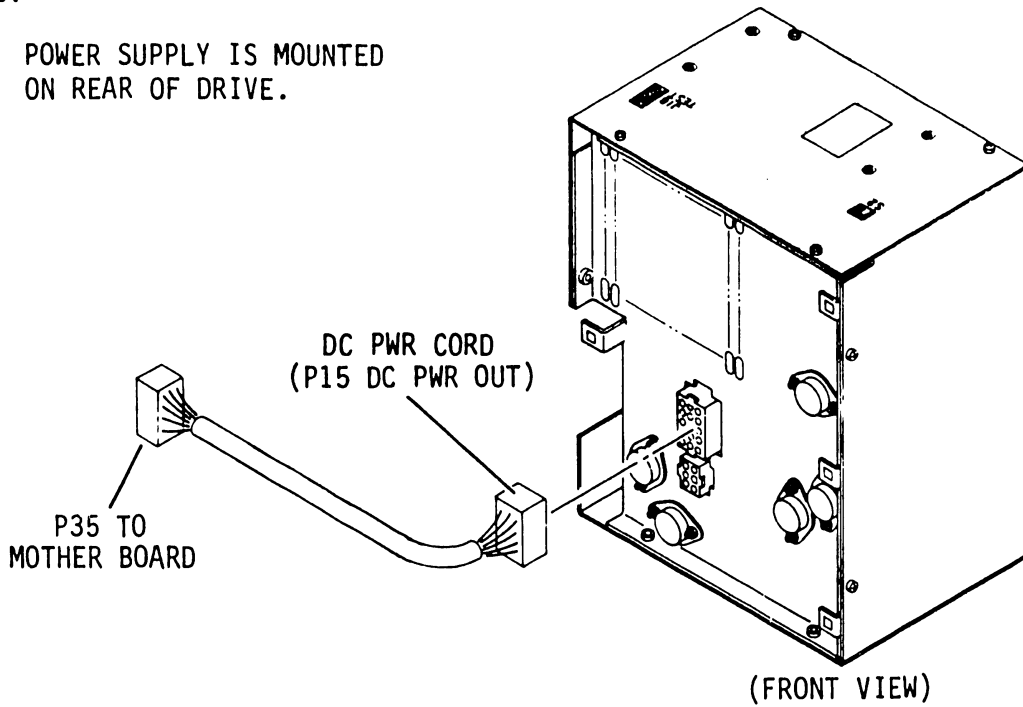
INTEGRAL POWER SUPPLY

11D109A

Figure 2-3. Component Locator (Sheet 4)

P27

J81

△3
2J03/J04

△1

△2
_SYX/TQX
(I/O BOARD)

1J03/J04

1J02

2J02

△3

P20

J28   J13   J80   J26

△1

_VCX
(CONTROL BOARD)

P14   P29
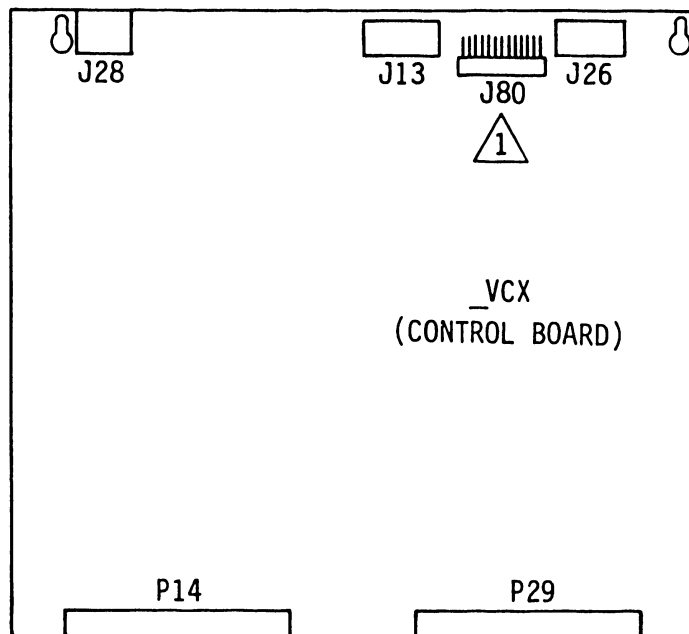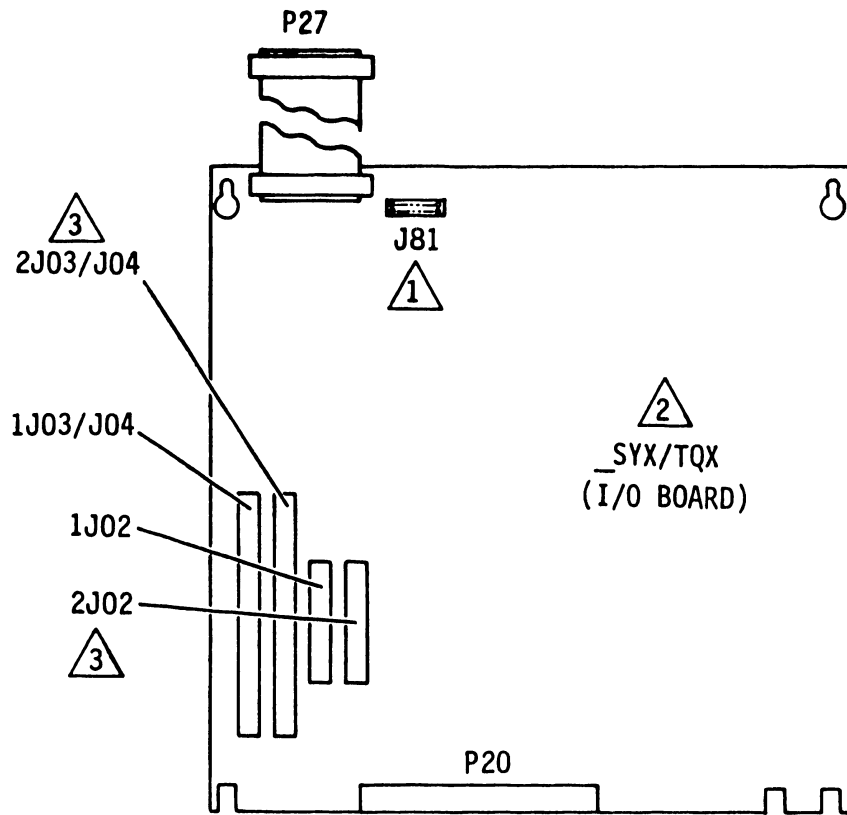
NOTES:

△1 TEST POINTS

△2 _SYX = SINGLE CHANNEL
   _TQX = DUAL CHANNEL

△3 FOUND ON _TQX BOARD

11D110A

Figure 2-3.   Component Locator (Sheet 5)
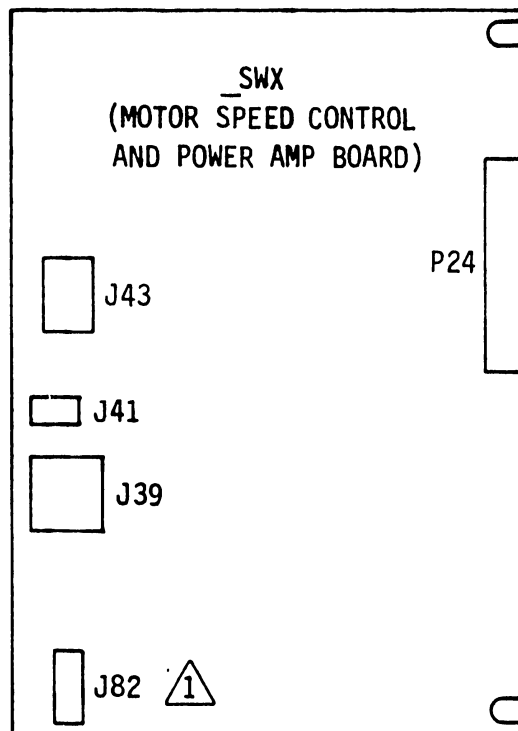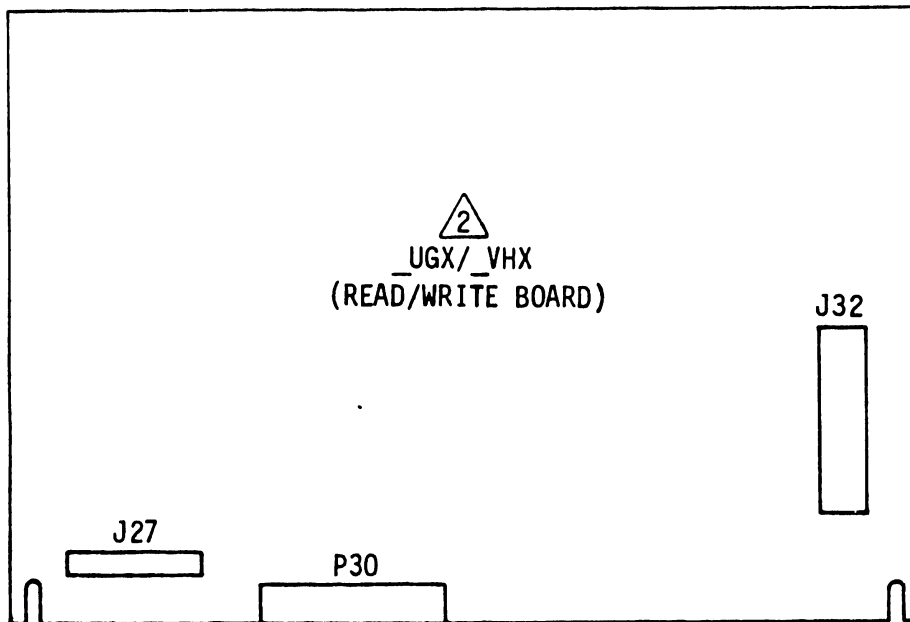
NOTES:

⚠ 1   TEST POINTS

⚠ 2   _UGX USED ON 340 MB DRIVE
      _VHX USED ON 515 MB DRIVE

11D111A

Figure 2-3.   Component Locator (Sheet 6)

                                                              83324770 B

INTEGRAL
POWER SUPPLY

⚠2
SHIPPING
BRACKET

SLIDE
ASSEMBLY

LOCK
RELEASE

SQUARE
NUTS

INNER
SLIDE

OUTER SLIDE

INTERMEDIATE
SLIDE

⚠1

NOTES:

⚠1 USE THESE PARTS LOCATIONS TO DIFFERENTIATE
BETWEEN RIGHT-HAND AND LEFT-HAND SLIDES.
⚠2 USE SHIPPING BRACKET TO SUPPORT POWER
SUPPLY WHEN SLIDES ARE NOT USED.
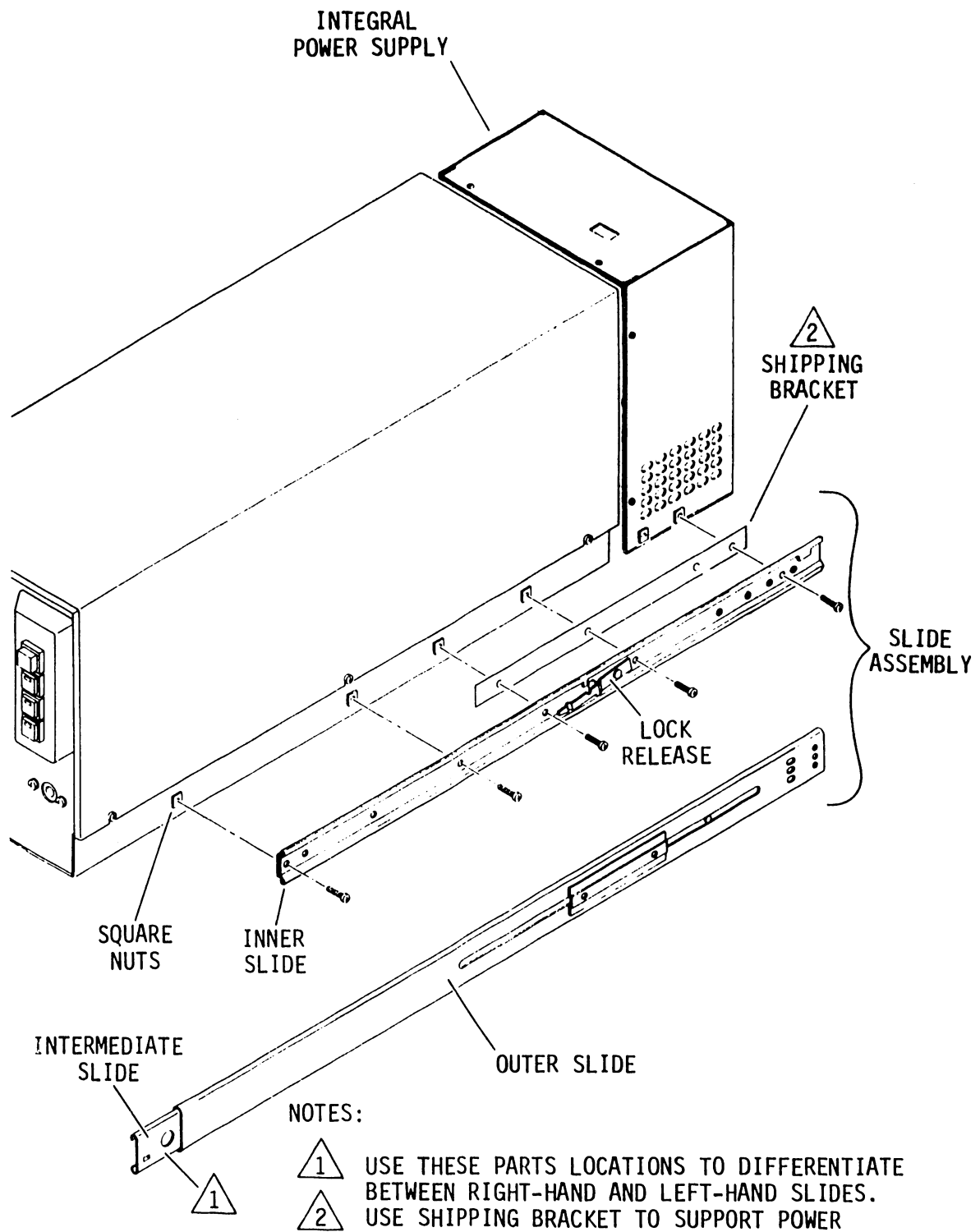
11D12 A

Figure 2-3.   Component Locator (Sheet 7)

SECTION
3
TROUBLE
ANALYSIS

3. TROUBLE ANALYSIS

CAUTION

When servicing the drive, observe all pre-
cautions listed under Electrostatic Discharge
Protection in section 2 of this manual. Fail-
ure to observe these precautions can result in
serious damage to electronic assemblies.

INTRODUCTION

The trouble analysis section contains information on isolating
and correcting problems causing improper drive operation. Per-
sons performing troubleshooting should be thoroughly familiar
with drive operation and with all information in the general
maintenance section of this manual (particularly the warnings
and precautions).

Because of the many types of malfunctions that may occur, the
information in this section will not provide a solution to
every problem. The intention, therefore, is to solve common
problems and to provide a starting point for the rest. The
final recommendation in all cases is to call field support.

Trouble analysis information is divided into two parts:

- Troubleshooting Procedures

- Diagnostic/Servo Status Codes

The troubleshooting procedures describe how to isolate and cor-
rect common drive problems. The procedures cover all the major
areas of drive operation: power, servo, read and write. Dia-
gnostic testing is used to determine which major drive assembly
has failed. The servo status codes apply specifically to the
servo system and describe the status codes presented by the MPU
during servo operation. Probable causes and corrective actions
are also included with the servo status code definitions.

Many of the corrective actions in this section refer to procedures given in Section 4, Electrical Checks and Section 5, Repair and Replacement. All procedures are referred to by number. For example, a reference to procedure 4201 refers to 4201 - Tribit Check in section 4. The first digit always indicates the section (4 or 5) where the procedure is found.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures describe how to isolate and correct common drive problems. Figure 3-1 is an example of a troubleshooting procedure and explains the format. The following paragraphs explain how to use the troubleshooting procedures.

Before starting a procedure, ensure that all assumptions have been satisfied. The assumptions along with other advisory information is given in the introductory paragraph to the procedure and describe conditions that must exist for the procedure to be valid.

When the assumptions are satisfied, proceed to the first step of the procedure. After performing the action or answering the question, follow the line down to the next step. For a question, follow the line beneath the appropriate Y (yes) or N (no) response. Continue until a corrective action is reached.

After taking the first recommended action, retest the unit. If the test results do not change, try recommended action 2, and so on, being sure to retest after each action. The corrective actions which are easier to perform (checking a signal or changing a circuit board, for example) are listed before the more difficult tasks such as replacing the module. If the corrective actions do not solve the problem, call field support.

The procedures appear in the following order:

- TSP1 - Power Check: Provides an overall check of drive power.

- TSP2 - ±5 Volt Check: Shows how to isolate problems in the ±5 volt loads.

- TSP3 - ±24 Volt Load Check: Shows how to isolate problems in the ±24 volt loads.

- TSP4 - First Seek Check: Provides possible causes for the drive failing to successfully complete a first seek.

- TSP5 – Direct or RTZ Seek Check: Provides possible causes for the drive failing to successfully complete a direct or RTZ seek.

- TSP6 – Write Check: Provides information for isolating cause of write errors.

- TSP7 – Read Check: Provides information for isolating cause of read errors.

- TSP8 – Address Mark Check: Provides possible causes for read or write address mark problems.

INDICATES THAT THIS IS SHEET 1
OF TROUBLESHOOTING PROCEDURE 1
(TSP31-1). SHEET 2 WOULD BE TSP31-2

TITLE

ASSUMPTIONS AND/OR
ADVISORY INFORMATION

TSP31-1

TSP31 - Power Check

- STEP
  NUMBER

Refer to procedure C101 - Power System Checks for voltage
specifications.

001   Set START switch to Off and CB1 to On.   ACTION TO BE PERFORMED

002   Does CB1 trip?   FIRST TROUBLESHOOTING QUESTION
       N   Y

YES OR NO RESPONSE   1   Check site power to power supply.
FOR QUESTION BEING
ASKED   2   Replace power supply (proc 5204).   FIRST CORRECTIVE ACTION
                           _   TO BE PERFORMED IN RESPONSE
                                                                          TO STEP 002
003   Do fans start?
       Y   N

UNDERLINE INDICATES
LAST CORRECTIVE   1   Check -24 volts at P38. If power is OK, replace
ACTION IN THIS   fans (proc D201). Otherwise, check wiring.
PARTICULAR SEQUENCE   2   Replace power supply (proc 5204).
                           _

004   Is - 24 volts OK?
       Y   N
                                                         INDICATES THAT PROCEDURE 5204
UNDERLINE ALSO   1   Go to TSP33 - ± 24 Volt Load Check. PROVIDES INFORMATION ON POWER
INDICATES THAT   _   SUPPLY REPLACEMENT
ONLY ONE ACTION   005 Is +24 volts OK?
IS TO BE PERFORMED   Y   N

                           1   Go to TSP33 - +24 Volt Load Check.
                           _

006   Is +5 volts OK?
       Y   N

                           1   Go to TSP32 - +5 Volt Load Check.
                           _

       2
       A

INDICATES THAT PROCEDURE IS
CONTINUED ON SHEET 2 COLUMN A

10R177

Figure 3-1. Example of Troubleshooting Procedure

3-4

83324770 B

Refer to procedure 4101 - Power Checks for voltage spec-
ifications.

001   Set START switch to Off and CB1 to On.

002   Does CB1 trip?
       N   Y
       │   ↓
       │   1   Ensure power supply is set at proper voltage.
       │   ↓
       │   2   Check site power to power supply.
       │   ↓
       │   3   Replace power supply (proc 5205).
       ↓

003   Does fan start?
       Y   N
       │   ↓
       │   1   Check -24 volts at P38 (_SVX mother board).
       │   │   If power is OK, replace fan (proc 5201).
       │   │   Otherwise, check wiring.
       │   2   Replace power supply (proc 5205).
       ↓

004   Is -24 volts OK?
       Y   N
       │   ↓
       │   1   Go to TSP3 - ± 24 Volt Load Check.
       ↓

005   Is +24 volts OK?
       Y   N
       │   ↓
       │   1   Go to TSP3 - ±24 Volt Load Check.
       ↓

006   Are ±5 volts OK?
       Y   N
       │   ↓
       │   1   Go to TSP2 - ±5 Volt Load Check.
       ↓

007   Is -8.3 volts OK?
       Y   N
       ↓   ↓
       2   2
       A   B

```
A   B
1   1
|   |
|   ↓
|   1   Disconnect P28 and recheck -8.3 volts.  If -8.3
|       volts is OK, replace module (proc 5207).  If
|       -8.3 volts is still abnormal, replace _VCX (proc
|       5304).
|
```

008   Are ±15 volts OK?
      Y   N
      | ↓
      | 1   Disconnect _UGX/_VHX from _SVX (mother board) and
      | recheck voltages. If voltage is normal, replace
      | _UGX/_VHX (proc 5301). Otherwise, proceed to
      | next action.
      | 2   Replace _VCX board (proc 5303). If voltage is
      | still abnormal, replace power supply (proc 5205).

009   Are +40 volts OK?
      Y   N
      | ↓
      | 1   Disconnect P24 (_SWX) from _SVX (mother board) and
      | recheck voltages. If voltage is normal, replace
      | _SWX (proc 5304). Otherwise, proceed to next
      | action.
      | 2   Replace power supply (proc 5205).

010   Power Check OK. If problem persists, call field support.

TSP2 - ±5 V Load Check

This check isolates problems with ±5 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

001   Deenergize drive and check for short circuits between:

        • +5 volts or -5 volts and ground.

        • +5 volts and -5 volts.

        • ±5 volts and ±24 volts.

002   Do any short circuits exist?
        N   Y
             ↓
             1   Remove loads (one at a time) to isolate short.
             ↓
             2   Inspect wiring and boards.

003   Remove all loads, except (_VCX) from ±5 volts by dis-connecting P24 (_SWX), P20 (_SYX/_TQX) and P30 (_UGX/_VHX) from _SVX (mother board), P32 (_UGX/_VHX to module) and P13 (_UQX) and P26 (_PBX) from (_VCX) board, then recheck voltages.

004   Are ±5 volts OK?
        Y   N
             ↓
             1   Check wiring and power supply.
             ↓
             2   Replace _VCX (proc 5303).

005   Deenergize drive, add _SWX to +5 volt load by connecting P24 to J24 _SVX (mother board), then recheck voltages.

006   Is +5 volts OK?
        Y   N
             ↓
             1   Replace _SWX (proc 5304).

007   Deenergize drive, add _SYX/_TQX to ±5 volt load by connecting P20 to J20 _SVX (mother board), then recheck voltages.
             ↓
             2
             A

```
        A
        1
        ↓
008    Are ±5 volts OK?
        Y   N
        |   ↓
        |   1   Replace _SYX/_TQX (proc 5302).
        ↓
009    Deenergize drive, add _UGX/_VHX to ±5 volt load by connec-
       ting P30 to J30 _SVX (mother board), then recheck volt-
       ages.
        ↓
010    Are ±5 volts OK?
        Y   N
        |   ↓
        |   1   Replace _UGX/_VHX (proc 5301).
        ↓
011    Deenergize drive, add module to ±5 volt load by connecting
       P32 to J32 (_UGX/_VHX), then recheck voltages.
        ↓
012    Are ±5 volts OK?
        Y   N
        |   ↓
        |   1   Replace module (proc 5207)
        ↓
013    Deenergize drive, add _UQX to ±5 volt load by connecting
       P13 to J13 (_VCX), then recheck voltages.
        ↓
014    Are ±5 volts OK?
        Y   N
        |   ↓
        |   1   Replace _UQX (proc 5203).
        ↓
015    Deenergize drive, add _PBX to ±5 volt load by connecting
       P26 to J26 (_VCX), then recheck voltages.
        ↓
016    Are ±5 volts OK?
        Y   N
        |   ↓
        |   1   Replace _PBX (proc 5202).
        ↓
        1   Replace power supply (proc 5205).  If problem per-
            sists call field support.
```

TSP3 - ±24 Volt Load Check

This check isolates problems with ±24 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

001   Deenergize drive and check for short circuits between:

        • +24 volts and -24 volts and ground.

        • +24 volts and -24 volts.

        • ±24 volts and ±5 volts.

002   Do any short circuits exist?
       N   Y

          1   Remove loads (one at a time) to isolate short.

          2   Inspect wiring and boards.

003   Remove all loads, except (_VCX) from ±24 volts by disconnecting P24 (_SWX), P20 (_SYX/_TQX) and P38 (fan), from _SVX (mother board), then recheck voltages.

004   Are ±24 volts OK?
       Y   N

          1   Check wiring and power supply.

          2   Replace _VCX (proc 5303).

005   Deenergize drive, add _SWX to ±24 volt load by connecting P24 to J24 _SVX (mother board), then recheck voltages.

006   Is ±24 volts OK?
       Y   N

          1   Replace _SWX (proc 5304).

       2
       A

```
            A
            1
            ↓
007    Deenergize drive, add _SYX/_TQX to +24 volt load by
       connecting P20 to J20 _SVX (mother board), then recheck
       voltages.
            ↓
008    Is -24 volts OK?
       Y    N
       |    ↓
       |    1    Replace _SYX/_TQX (proc 5302).
       |
       ↓
009    Deenergize drive, add fan to +24 volt load by connecting
       P38 to J38 _SVX (mother board), then retest.
            ↓
010    Are +24 volts OK?
       Y    N
       |    ↓
       |    1    Replace fan (proc 5201).
       |
       ↓
011    Replace power supply (proc 5205).  If problem persists,
       call field support.
```

TSP4 - First Seek Check

001   Initiate first seek as follows:

        a. Set LOCAL/REMOTE switch to local.

        b. Set CB1 & START switch to ON.

002   Does READY indicator light?
        N   Y
             ↓
003   Drive has successfully completed first seek.

004   Do all fault LEDs light?
        N   Y
             ↓
005   Are ±5 volts OK?
             Y   N
                  ↓
                  1   Check ±5 volts. See TSP2.
                  ↓
                  2   Check connection at J28 (_VCX).

             1   Replace _VCX (proc 5303).

006   Is operator panel fault light on?
        N   Y
             ↓
             Is cooling fan operating?
             Y   N
                  ↓
                  1   Check for loose connector at P38 on _SVX
                  | (mother board).
                  2   If -24 volts is present at P38, replace fan
                  | (proc 5201).
                  3   Replace _SYX/_TQX (proc 5302).

007   Does First Seek Fault LED light?
        Y   N
        ↓   ↓
        2   2
        A   B

```
A    B
1    1

|    ↓

     1    Check P43 (_SWX) to interlock cabling.

     ↓

     2    Replace _SWX (proc 5304).
```

008   Does Volt Fault LED light?
```
N    Y

|    ↓

     1    Check LED's on fault status display board
          (located behind front panel insert) for error
          code.

     2    Check all power harness connections.
```

009   If problem persists, all field support.

TSP5 - Direct or RTZ Seek Check

This test assumes that the following conditions exist: (1) drive is operating under control of the FTU and (2) first seek was successfully completed.

001   Does FAULT indicator light or is Seek Error active?
       Y   N
       | ↓
002 | Direct or RTZ seek is OK.
       |

003   Does Write or Write and Read Fault LED light?
       N   Y
       | ↓
       | 1   Read/write problem. See TSP 6 or 7.
       ↓

004   Does Volt Fault LED light?
       N   Y
       | ↓
       | 1   Power problem. See TSP 1.
       ↓

005   Does On Cylinder go active?
       N   Y
       | ↓
006 | Does error always occur at or near the same cylinder?
       | Y   N
       | ↓
       | 1   Check Module to J28 (_VCX) and P43 and _SWX
       | | board.
       | 2   Replace _SWX board (proc 5304).
       | ↓
       | 3   Replace _VCX (5303).
       | ↓
       | 4   Replace module (proc 5207).
       |
       | 1   Replace module (proc 5207).
       ↓
       2
       A

A
1
↓

007   Does error always occur when seeking to or near the same
cylinder?
    N Y
       ↓
       1   Check LED's on fault status display board
           (located behind front panel insert) for error
           code.

       2   Replace _VCX (proc 5303).
       ↓
       <u>3</u>   Replace module (proc 5207).

    1 Check cabling connection from module to J28 (_VCX).
    ↓
    2 Replace _SYX/_TQX (proc 5302).
    ↓
    3 Replace _VCX (proc 5303).
    ↓
    <u>4</u> Replace module (proc 5207).

TSP6 - Write Check

This check assumes that the drive is performing write or write format operations under control of the FTU.

001   Does Volt Fault LED light?
       N   Y
       | ↓
       | 1   Power problem. Go to TSP1.

002   Does Read and Write Fault LED light?
       N   Y
       | ↓
       | 1   Check I/O connections.
       | ↓
       | 2   Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.
       | ↓
       | 3   Replace _SYX/_TQX (proc 5302).
       | ↓
       | 4   Replace _UGX/_VHX (proc 5301).

003   Does Read or Write and Not On Cylinder Fault LED light?
       N   Y
       | ↓
       | 1   Servo problem. Go to TSP 4 or 5.

004   Does Write Fault LED light?
       N   Y
       | ↓

005   Is problem head related?
           N   Y
           | ↓

006   Is Write Fault active (_UGX/_VHX, TP-C743)?
           Y   N
           | ↓
           | 1   Replace module (proc 5207).

         2   2   2
         A   B   C

```
A   B   C
1   1   1
            │
            1    Check head/cylinder address bits on
                 _UGX/_VHX.  If bits are OK, replace module
                 (5207)  Otherwise, proceed to next action.
            │
            2    Check I/O connections.
            │
            3    Check P27 connector at _UGX/_VHX.
            │
            4    Check P32 to module cabling.
            │
            5    Replace _SYX/_TQX (proc 5302).
            │
            6    Replace _UGX/_VHX (proc 5301).
            │
            7    Replace module (proc 5207).
```

007   Is Write Fault active (_UGX, TP-C743 or _VHX, TP-C642)?

```
        Y   N
            │
            1    Check for data at output of _UGX/_VHX.
                 If data is absent, perform 4303 - Write
                 Data Check.
            │
            2    Check head/cylinder address bits on
                 _UGX/_VHX.  If bits are OK, replace
                 module (proc 5207).

        1   Perform procedure 4303 - Write Data Check.
        │
        2   Replace _UGX/_VHX (proc 5301).
        │
        3   Replace _VCX (proc 5303).
        │
        4   Replace module (proc 5207).

    3
    D
```

D
2
↓

008   Perform procedure 4303 - Write Data Check.
↓

009   Is the 1.621 (_UGX) or 2.41 (_VHX) MHz clock OK?
       Y   N
           ↓
           1   Servo problem.   See TSP 4 or 5.

010   Is the 2F clock OK?
       Y   N
           ↓
           1   Replace _UGX/_VHX (proc 5301).

011   Is the Servo clock OK?
       Y   N
           ↓
           1   Replace _UGX/_VHX (proc 5301).
           ↓
           2   Replace _SYX/_TQX (proc 5302).

012   Are Write Gate, Write Clock, and Write Data present?
       Y   N
           ↓
           1   Check I/O connections.
           ↓
           2   Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.
           ↓
           3   Replace _SYX/_TQX (proc 5302).
           ↓
           4   Replace _UGX/_VHX (proc 5301).

013   Is Write Data Compensated present?
       Y   N
           ↓
           1   Replace _UGX/_VHX (proc 5301).

014   Is Read/Write Data to preamplifier present?
       N   Y
           ↓
015   Write Data Check OK. If problems persist, call field
           support.

       4
       D

```
        D
        3
        │
        ↓
016     Is Write Enable OK?
        Y   N
        │   ↓
        │   1    Replace _VCX (proc 5303).
        │   ↓
        │   2    Replace _UGX/_VHX (proc 5301).
        │
        1   Replace _UGX/_VHX (proc 5301).
        ↓
        2   Replace module (proc 5207).
```
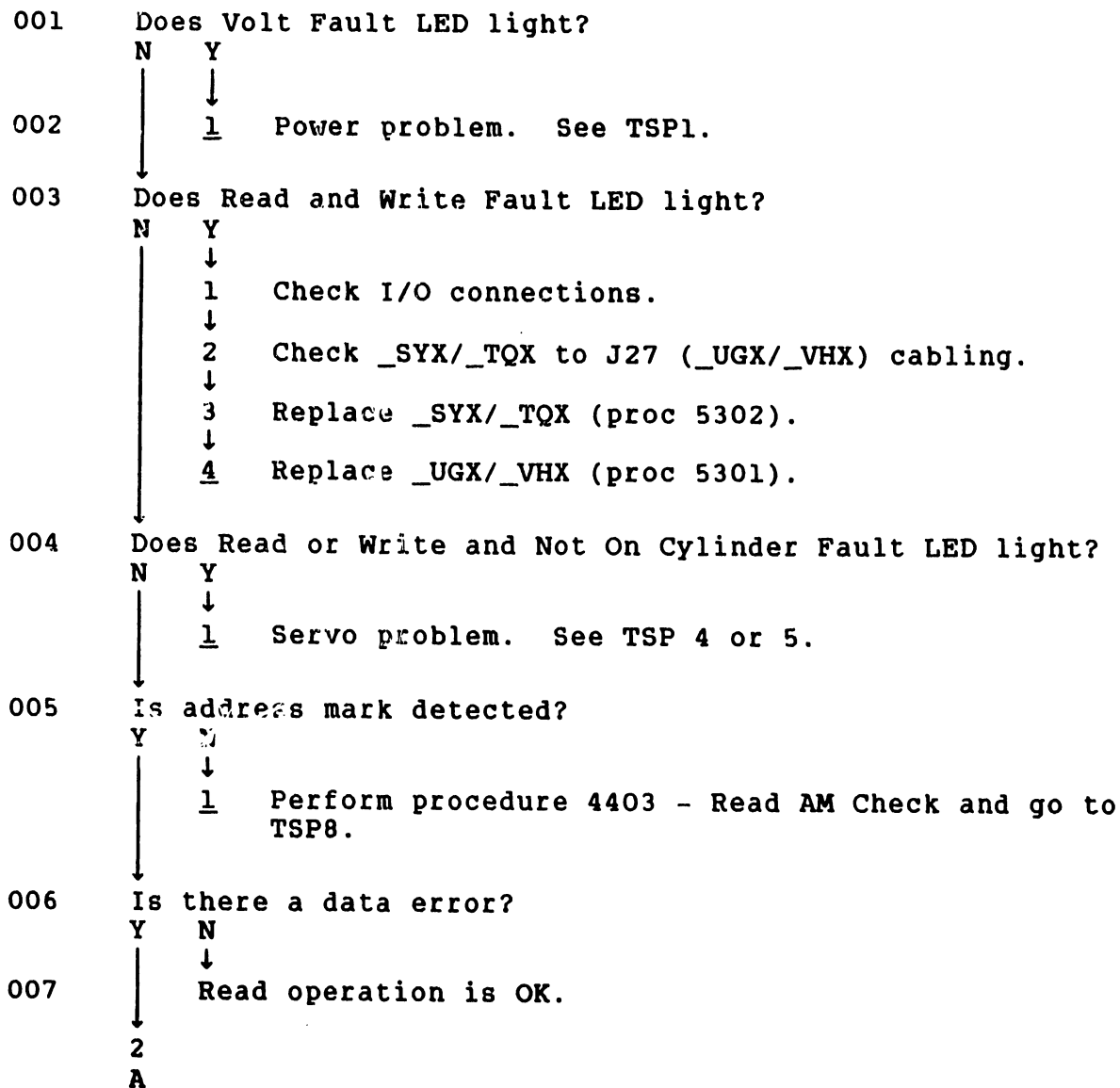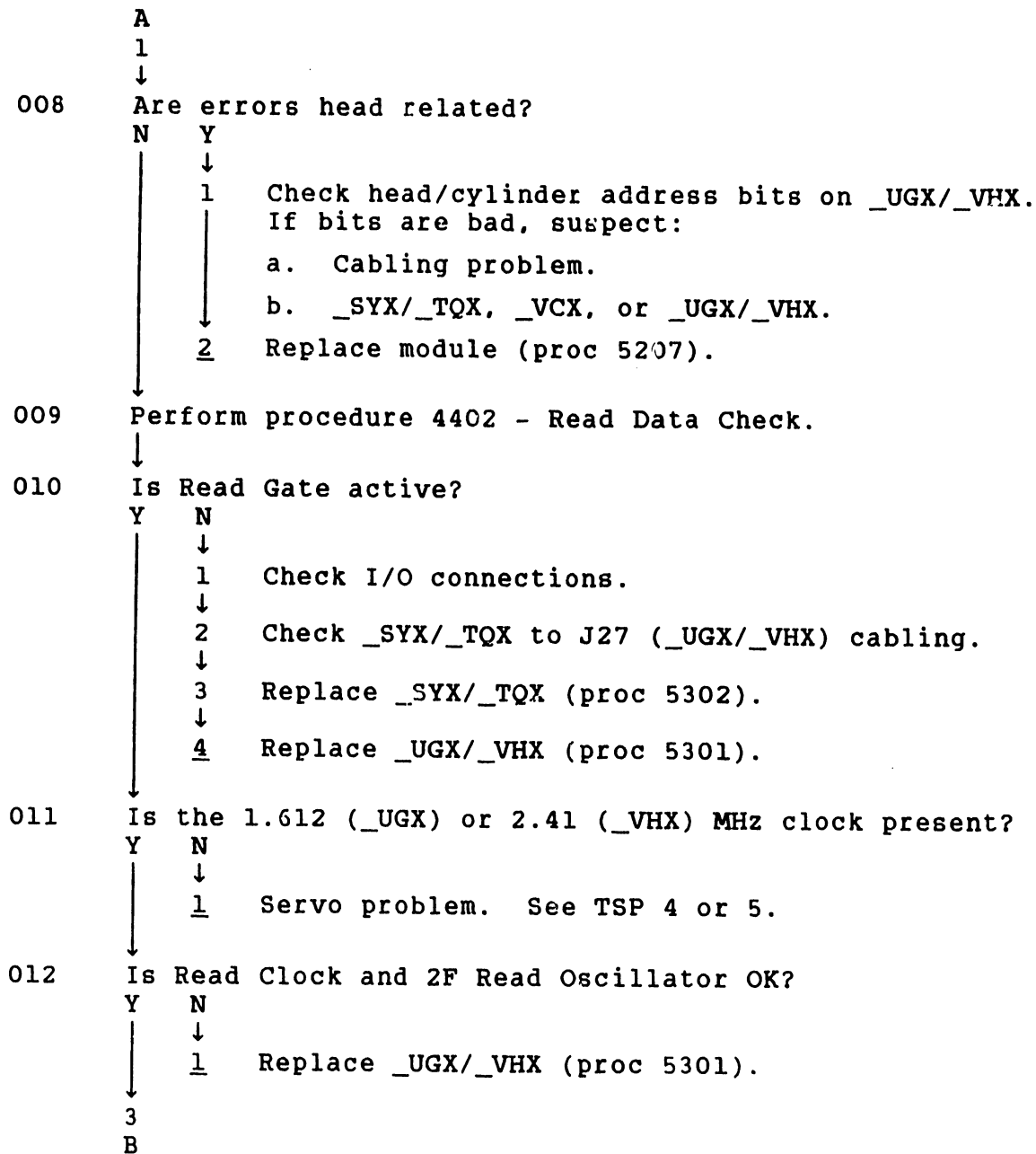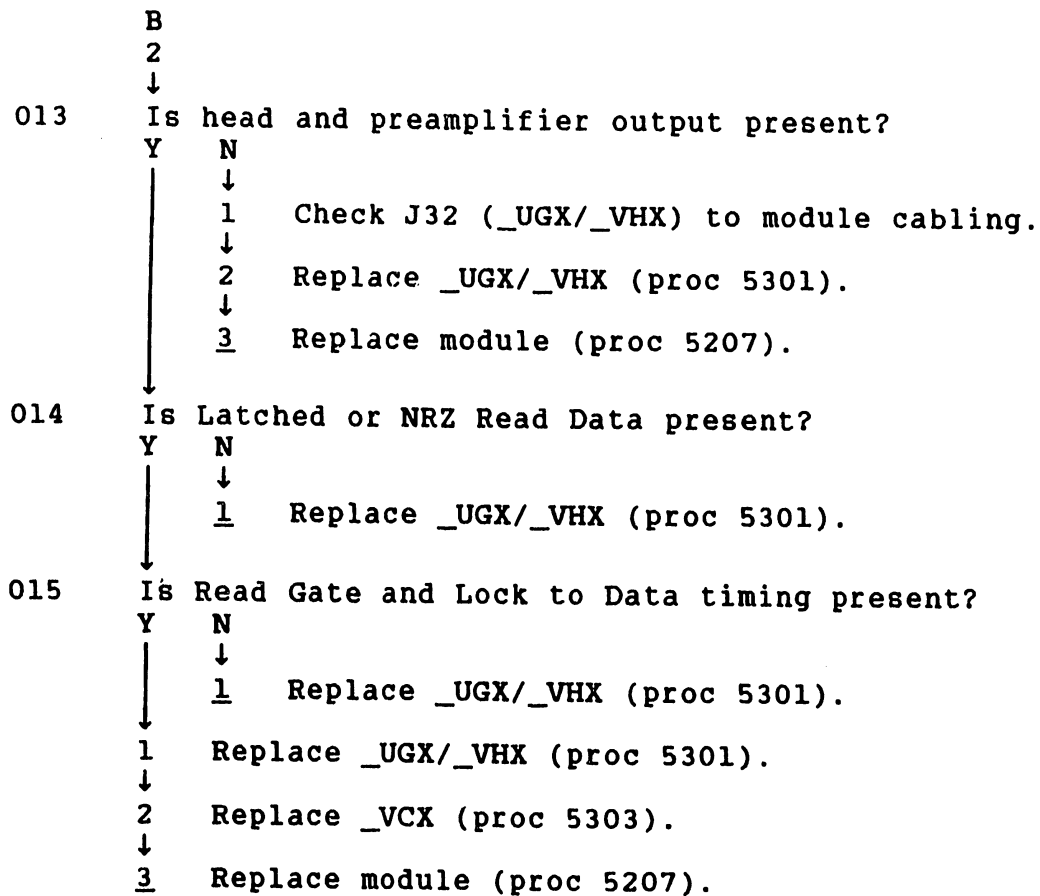
TSP7 - Read Check

This check assumes that the drive is performing read operations
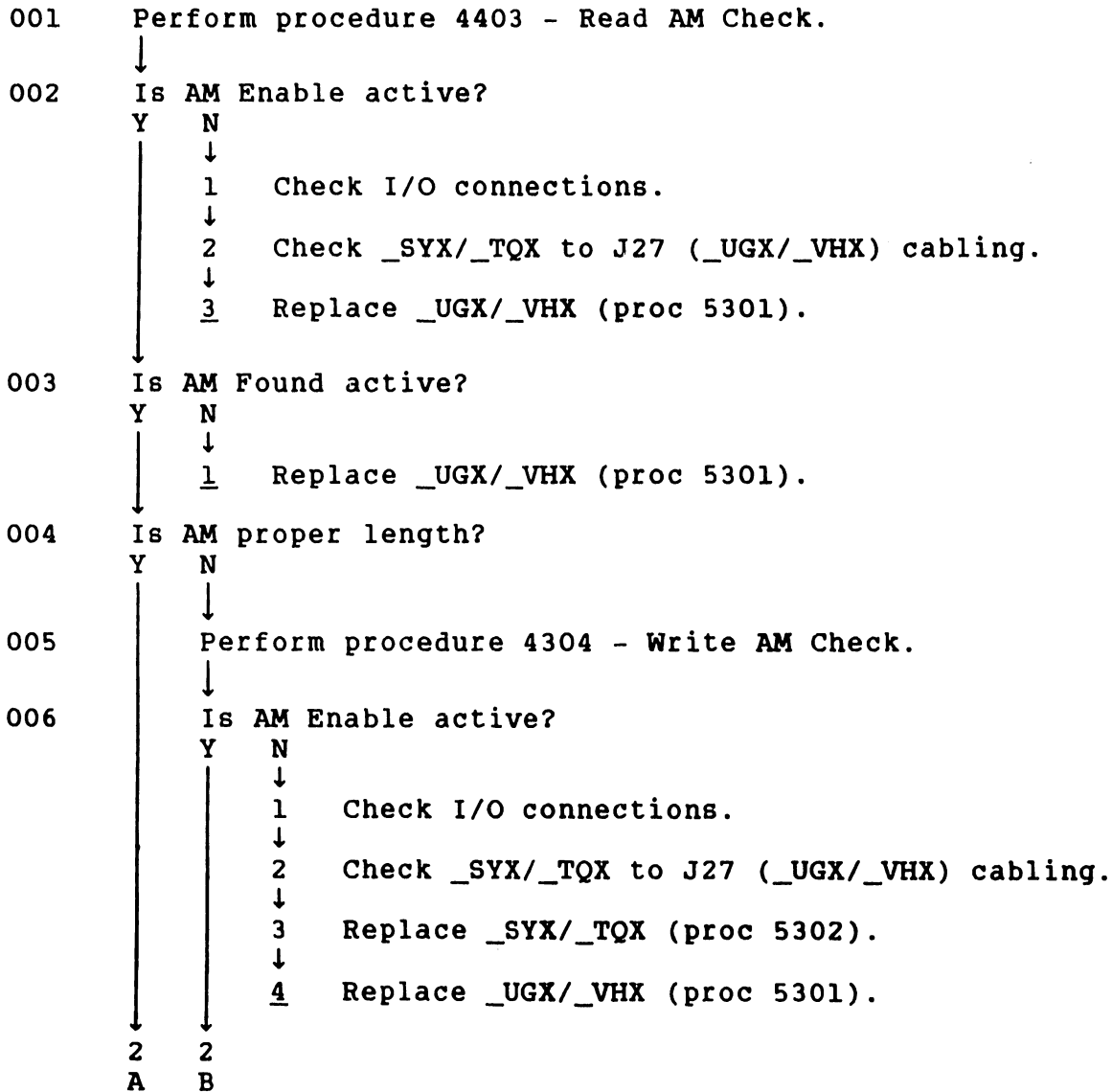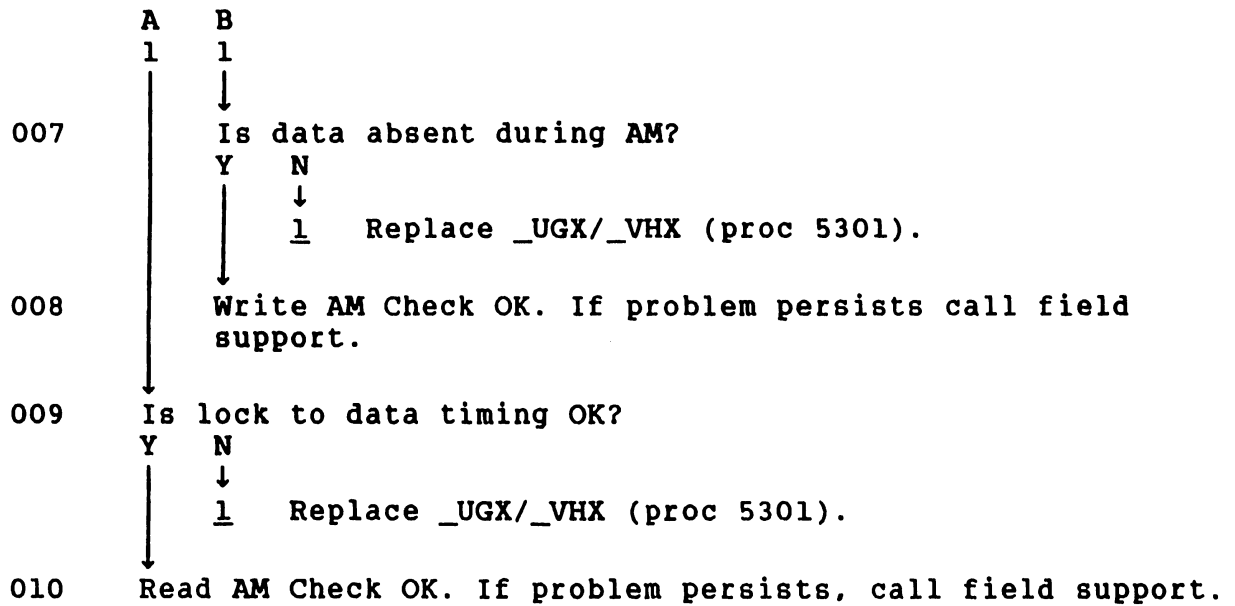under control of the FTU.

001   Does Volt Fault LED light?
       N   Y

002 | 1   Power problem. See TSP1.

003   Does Read and Write Fault LED light?
       N   Y

           1   Check I/O connections.

           2   Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.

           3   Replace _SYX/_TQX (proc 5302).

           4   Replace _UGX/_VHX (proc 5301).

004   Does Read or Write and Not On Cylinder Fault LED light?
       N   Y

           1   Servo problem. See TSP 4 or 5.

005   Is address mark detected?
       Y   N

           1   Perform procedure 4403 - Read AM Check and go to
               TSP8.

006   Is there a data error?
       Y   N

007 | Read operation is OK.

       2
       A

```
        A
        1
        ↓
008     Are errors head related?
        N   Y
            ↓
            1    Check head/cylinder address bits on _UGX/_VHX.
            |    If bits are bad, suspect:
            |    a.   Cabling problem.
            |    b.   _SYX/_TQX, _VCX, or _UGX/_VHX.
            2    Replace module (proc 5207).

009     Perform procedure 4402 - Read Data Check.
        ↓
010     Is Read Gate active?
        Y   N
            ↓
            1    Check I/O connections.
            ↓
            2    Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.
            ↓
            3    Replace _SYX/_TQX (proc 5302).
            ↓
            4    Replace _UGX/_VHX (proc 5301).

011     Is the 1.612 (_UGX) or 2.41 (_VHX) MHz clock present?
        Y   N
            ↓
            1    Servo problem.  See TSP 4 or 5.

012     Is Read Clock and 2F Read Oscillator OK?
        Y   N
            ↓
            1    Replace _UGX/_VHX (proc 5301).
        3
        B
```

```
        B
        2
        ↓
013     Is head and preamplifier output present?
        Y    N
        |    ↓
        |    1    Check J32 (_UGX/_VHX) to module cabling.
        |    ↓
        |    2    Replace _UGX/_VHX (proc 5301).
        |    ↓
        |    3    Replace module (proc 5207).
        |
        ↓
014     Is Latched or NRZ Read Data present?
        Y    N
        |    ↓
        |    1    Replace _UGX/_VHX (proc 5301).
        |
        ↓
015     Is Read Gate and Lock to Data timing present?
        Y    N
        |    ↓
        |    1    Replace _UGX/_VHX (proc 5301).
        ↓
        1    Replace _UGX/_VHX (proc 5301).
        ↓
        2    Replace _VCX (proc 5303).
        ↓
        3    Replace module (proc 5207).
```

TSP8 - Address Mark Check

The following check assumes that the drive is under control of
the FTU.

001   Perform procedure 4403 - Read AM Check.
        ↓
002   Is AM Enable active?
        Y   N
        | ↓
        | 1   Check I/O connections.
        | ↓
        | 2   Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.
        | ↓
        | 3   Replace _UGX/_VHX (proc 5301).

003   Is AM Found active?
        Y   N
        | ↓
        | 1   Replace _UGX/_VHX (proc 5301).

004   Is AM proper length?
        Y   N
        | |
        | ↓
005 | Perform procedure 4304 - Write AM Check.
        | ↓
006 | Is AM Enable active?
        | Y   N
        | | ↓
        | | 1   Check I/O connections.
        | | ↓
        | | 2   Check _SYX/_TQX to J27 (_UGX/_VHX) cabling.
        | | ↓
        | | 3   Replace _SYX/_TQX (proc 5302).
        | | ↓
        | | 4   Replace _UGX/_VHX (proc 5301).
        | |
        ↓   ↓
        2   2
        A   B

```
       A   B
       1   1
       |   |
007    |   Is data absent during AM?
       |   Y   N
       |   |   |
       |   |   1   Replace _UGX/_VHX (proc 5301).
       |   |
008    |   Write AM Check OK. If problem persists call field
       |   support.
       |
009    Is lock to data timing OK?
       Y   N
       |   |
       |   1   Replace _UGX/_VHX (proc 5301).
       |
010    Read AM Check OK. If problem persists, call field support.
```

DIAGNOSTIC/SERVO STATUS CODES

GENERAL

The diagnostic and servo status codes are two digit hexadecimal codes, generated by the MPU, that indicate either the diagnostic tests being initiated or operational status of the drive servo system. The following discussions explain how to perform diagnostic tests and defines various servo status codes.

DIAGNOSTIC TESTING

General

This section describes the steps required to execute the off-line diagnostics provided with the drive. These tests are initiated and monitored via switches and indicators on the Status/Fault Display board (see figure 3-2). This board is located behind the front panel insert and filter. Table 3-1 describes the function of the switches and indicators.
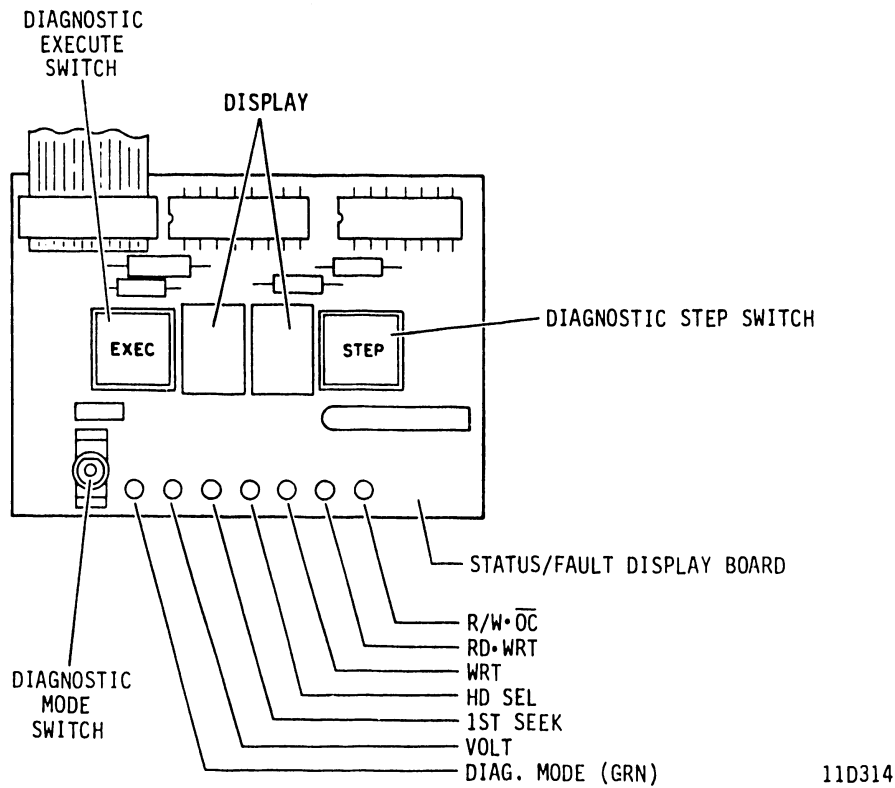
Figure 3-2. Switches and Indicators

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TABLE 3-1. SWITCH/INDICATOR DESCRIPTIONS

Description	Function
Diagnostic Mode Switch	Setting the switch to the up position places the unit in diagnostic mode and disables the interface. The diagnostic mode indicator lights when the switch is set to diagnostic mode. Setting the switch to the down position permits normal controller selection on the interface.
Diagnostic Step Switch (STEP)	Used to step the status/diagnostic fault display pattern from 0 to F. Holding the switch down causes the numbers to increment continuously and wrap around from F to zero. Refer to Diagnostic Execute switch. Note: the switch must be pressed for a minimum of 400 milliseconds to activate.
Diagnostic Execute Switch (EXEC)	Used to enter values in memory. The entries permit test selection, entry of test parameters, and test deselection. The switch must be pressed for a minimum of 400 milliseconds to activate.
Status/Diagnostic Fault Display	Used to display current status when unit is operating in normal mode, or diagnostic options and error codes when operating in diagnostic mode.
First Seek Indicator	Indicates drive failed first seek/load attempt.
Read or Write and Not On Cylinder Indicator	Indicates read or write conditions existed during a seek operation (an off cylinder condition).

Table Continued on Next Page

TABLE 3-1.   SWITCH/INDICATOR DESCRIPTIONS (Contd)

Description	Function
Write Indicator	Indicates that a write fault has occurred.
Read and Write Indicator	Indicates that a write and read command are active simultaneously.
Voltage Indicator	Indicates a below normal voltage condition.
Head Select Indicator	Indicates a multiple head selection condition.
Diagnostic Mode Indicator	Indicates that drive is in diagnostic mode.

Test Selection Procedure

Placing the Diagnostic Mode switch to the ON (up) position causes "00" to be displayed in the Status/Diagnostic Fault Display LEDs. Pressing the Step switch after mode selection allows the operator to increment the least significant (rightmost) display character. Once the desired character is displayed, the operator must press the Execute switch to enter the character into memory.

This procedure must be repeated for the most significant character. Pressing the Execute switch after entering the test number in memory initiates test execution except in those instances where the test requires additional parameter entries. A description of the parameter entries is included with the corresponding test description. After test completion, test 00 is enabled ("00" in Display). To determine if an error occurred, the operator must place the Diagnostic Mode switch in the OFF (down) position and observe the display, or execute Diagnostic Test 00.

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Test Descriptions

General

The individual diagnostic tests are listed in table 3-2 and are described in the following topics.

TABLE 3-2. SUMMARY OF DIAGNOSTIC TESTS

Test Number	Name of Test
00	Display Status/Error Log
01	Display Fault Log
02	Perform MPU Initialization
03	Switch Display Test
04	Calculate Four Most Likely Failed Field Replaceable Units
05	Servo Test
06	Clear Status/Error Log
07	Clear Fault Log
08	Direct Seek
09	Random Seek
0A	Display/Alter Load Delay
0C	Display EPROM Part Number
0D	Load Cylinder Address
0E	Return to Zero

Test 00 -- Display Status/Error Code Log

This test displays the sixteen most recently generated status/error codes. After test selection, the Display provides a pointer to a memory location in the range from 20 to 2F (see figure 3-3). The pointer address minus one contains the last fault condition detected. Continuously pressing the Step switch allows the operator to display the contents of these locations starting at location 20. After displaying location 2F, the display returns to the pointer. The current status is contained in the location preceding the pointer. At the completion of a successful power up operation, the expected contents are as follows: 70, 71, 02, 03, 2E, 07, 08, with 00 in all remaining locations. Refer to the Test 02 description to determine the expected contents of the log when Test 00 is preceded by Test 02. The operator must press the Execute switch to end the test. The status codes displayed in this test are listed and defined later in this section.

Test 01 -- Display Fault Log

This test displays the eight most recently generated fault conditions. After test selection, the display provides a pointer to a memory location in the range from 31 through 39 (see figure 3-3). The pointer address minus one contains the last fault condition detected. Continuously pressing the Step switch allows the operator to display the contents of these locations starting at location 31. After displaying location 39, the display returns to the pointer. The current fault is in the location preceding the pointer. The operator must press the Execute switch to end the test. The definition of each bit within the fault byte is provided below:

Bit		Definition
0	(LSB)	Not Used (01)
1		Voltage Fault (02)
2		Write Fault (04)
3		Read·Write Fault (08)
4		(Read+Write)·Off Cylinder Fault (10)
5		Head Select Fault (20)
6		First Seek Fault (40)
7	(MSB)	Not Used (80)

Test 02 -- Perform MPU Initialization

This test re-executes the MPU initialization procedure. If the spindle motor is operating, the test also re-executes the first seek operation (spindle motor is not recycled). At the conclusion of the initialization, the display returns to test selection ("00" displayed).

TEST 00

OPERATOR ACTION	DISPLAY	NOTES
	0 0	ENTRY INTO TEST 00
EXEC	2 7	SHOWS CURRENT POINTER VALUE
STEP	7 0	STATUS CODE AT LOCATION 20
STEP	7 1	STATUS CODE AT LOCATION 21
STEP	0 2	STATUS CODE AT LOCATION 22
STEP	0 3	STATUS CODE AT LOCATION 23
STEP	2 E	STATUS CODE AT LOCATION 24
STEP	0 7·	STATUS CODE AT LOCATION 25
STEP	0 8	STATUS CODE AT LOCATION 26
9 STEPS	0 0	STATUS CODE AT LOCATION 2F
EXEC →	0 0	EXIT FROM TEST & RETURN TO TEST SELECTION

TEST 01

OPERATOR ACTION	DISPLAY	NOTES
	0 1	ENTRY INTO TEST 01
EXEC	3 5	SHOWS CURRENT POINTER VALUE
STEP	0 0	FAULT CODE AT LOCATION 31
STEP	4 0	FAULT CODE AT LOCATION 32
STEP	0 0	FAULT CODE AT LOCATION 33
STEP	0 2	FAULT CODE AT LOCATION 34 (MOST RECENT ENTRY)
STEP	0 0	FAULT CODE AT LOCATION 35
4 STEPS	0 0	FAULT CODE AT LOCATION 39
EXEC →	0 0	EXIT FROM TESTS & RETURN TO TEST SELECTION

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Figure 3-3. Display Sequence Examples

The Test 00 display of a successful initialization, occurring as a result of Test 02, is determined by the condition of the drive prior to the initialization routine. If the spindle motor was stopped during the initialization, the pointer is set to 25 and the operator must continuously press the Step switch to display the contents of the status/error log. The expected contents are as follows: 70, 71, 02, 03, with 00 in all remaining locations. If the spindle was turning when the initialization was started, the pointer is set to 24 and the operator must continuously press the Step switch to display the contents of the status/error log. The expected contents are as follows: 70, 18, D1, 51, with 00 in all remaining locations.

Test 03 -- Switch Display Test

This test contains two parts. Immediately after test selection, the display alternates between "EE" and "11", and also lights all of the fault indicators. This is repeated ten times. Afterward, the operator may individually test the switches and test jumpers as follows:

Switch	Corresponding LED Lit
Diagnostic Mode	Head Select Fault and Diagnostic Mode.
Local/Remote Mode	Local switch position will light Write Fault LED unconditionally; Remote switch position will light Write Fault LED when controller power sequence switch is activated.
Start	Read/Write Fault (Write Fault must be active).
Fault Clear	Voltage Fault.
Servo Test Jumper	Read or Write and Not On Cylinder Fault.
Execute	Causes "80" to be displayed.
Step	Causes the "80" displayed by the Execute switch to shift right one bit at a time (80, 40, 20, 10, 08, 04, 02, 01, 00).

The switch subtest can be executed any number of times. To exit the test, press Execute switch and Step switch simultaneously.

Test 04 -- Calculate Four Most Likely Failed Field Replaceable
Units

NOTE

Do not execute Test 06 or Test 07 prior to
running Test 04.

This test uses the fault and status history as displayed by
Tests 00 and 01 to predict the most likely cause of drive fail-
ure. For this reason, if other diagnostic tests are run prior
to Test 04 when a malfunction is suspected, these tests could
alter the results of Test 04.

Running the test generates a two digit hex display showing the
first and second most likely failed unit (leftmost digit is
most likely failed unit). Pressing the Step switch changes the
display to the third and fourth most likely failed unit (left-
most digit is third likely failed unit). The field replaceable
unit corresponding to each display is provided in table 3-3.

TABLE 3-3. CODING OF FIELD REPLACEABLE UNITS

Hex Display	Field Replaceable Unit
1	Power Supply
2	Control Board
3	Power Amplifier
4	Drive Motor
5	Read/Write Board
6	Head/Disk Assembly
7	Cooling Fan
8	I/O Board
9	Operator Panel
A	Mother Board
B	Carriage Locking Solenoid
D	Diagnostic Display
F	Air Filter

Test 05 -- Servo Test

This test automatically performs several types of seek operations. These operations are listed below in the order in which they occur:

Operation	Number of Times Executed
RTZ	1
1 Track Seek	16
Servo Recalibrate	8
Max. Length Seek	16

Execution stops when an error is detected or the test completes.

Test 06 -- Clear Status/Error Log

This test clears the status/error log. At the conclusion of the test, the log pointer is set to 20 but is not displayed.

Test 07 -- Clear Fault Log

This test clears the fault log. At the conclusion of the test, the log pointer is set to 31 but is not displayed.

Test 08 -- Direct Seek

This test performs continuous seeks between cylinder zero and the cylinder address loaded by Test OD. The operation is terminated by pressing the Execute switch, or by active fault status.

Test 09 -- Random Seek

This test performs random seeks within the limits of cylinder zero and the maximum cylinder address (710 decimal). Operation is terminated by pressing the Execute switch, or by active fault status.

Test OA -- Display/Alter Load Delay

This test displays and/or alters a count corresponding to the
amount of delay between seeks during the one-track scan portion
of the First Seek routine. To alter the load delay, press the
Step switch the desired number of times to increment the dis-
play to the desired low order digit, then press Execute switch.
Repeat this operation to alter the high order digit. Each dis-
play increment represents 10 milliseconds. A load delay count
of 00 represents default.

Test OC -- Display EPROM Part Number

This test displays the eight digit decimal part number of the
EPROM located on the control board. The display is broken into
four two-digit bytes starting with the most significant byte.
To display the remaining bytes, press the Step switch three
times. To exit, turn off the Diagnostic Mode switch and then
turn it back on. Note: Turning off the Diagnostic Mode switch
causes the drive to perform an RTZ operation.

Test OD -- Load Cylinder Address

This test allows the operator to load a number to be used as
the upper cylinder address in Test 08 (Direct Seek). The cyl-
inder address is expressed as four hexadecimal characters (see
figure 3-4). Initially, the display shows the upper two char-
acters. Advance the righthand character to the desired value
by pressing the Step switch, and load it into memory by pres-
sing the Execute switch. Then, do the same for the lefthand
character. At this time, the display shifts to show the lower
two characters. Repeat the above procedure to load the right-
hand and then the lefthand character into memory. The test
concludes when the Execute switch has been pressed four times.

Test OE -- Return to Zero

This test executes a return to zero (RTZ) seek and exits (dis-
play returns to "00").

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EXAMPLE: LOAD CYLINDER 0710 DECIMAL (02C6 HEXADECIMAL)

AFTER SELECTING TEST OD
USE STEP SWITCH TO ADVANCE
DISPLAY TO "2".

EXEC

RETAIN DEFAULT VALUE
IN THIS DISPLAY POSITION

NOTE: DISPLAY SET TO DEFAULT VALUE ("00")
UNTIL ADVANCED BY STEP SWITCH

EXEC

USE STEP SWITCH TO ADVANCE
DISPLAY TO "6".

EXEC

USE STEP SWITCH TO ADVANCE
DISPLAY TO "C".

RETURN TO
EXEC ➔ TEST SELECTION

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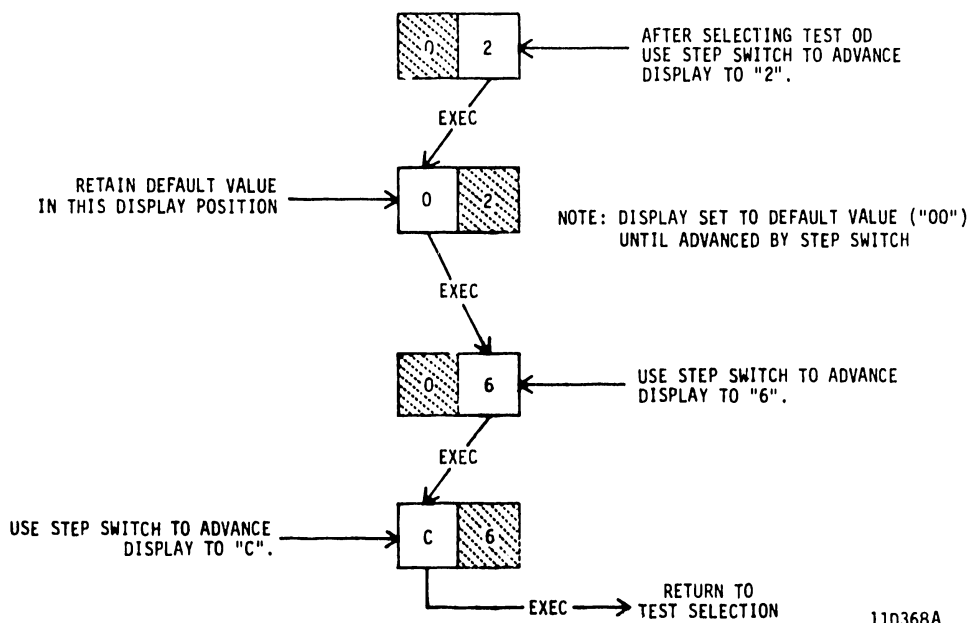
Figure 3-4. Loading An Address in Test OD

SERVO STATUS CODE DEFINITIONS

Whenever the drive is in a power on condition (dc power active), the MPU is periodically checking the operation of the servo status system and generating appropriate status codes. The codes can be visually monitored by removing the drive front panel insert. Table 3-4 is a summary of all the status codes and table 3-5 provides definitions of each code. Each status code definition is divided into three parts:

1. Description: Basic definition of what type of problem the code indicates, during what operations the code appears, what additional error indications are present with the code, and how to initiate a retry or recovery from the error.

2. Probable Causes: What general areas could cause the problem. The purpose here is to provide a general idea of what functional areas could be causing the problem.

3. Actions: What specific things to check to correct the problem. Perform each action and retest the drive before proceeding to the next action. If all actions have been performed and the problem persists, call field support.

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When interpreting the status codes it is important to know that not all codes appearing on the display indicate errors. Some indicate that the operation is still in progress, others that the operation has been successfully completed.

When an operation is in progress, the status is continually changing. Most codes flash on and off very rapidly and are not recognizable. Others will remain for several seconds.

If an error occurs, the status indicates the type of error and where in the sequence the error occurred. The error code will remain active until the proper action is taken to reset it (depends on nature of error).

TABLE 3-4. STATUS CODE SUMMARY

Status Code	Description
00	**Normal On Cylinder** Normal On Cylinder
01	**Normal Motor Stop** Retracting Heads To Landing Zone
02	Stopping Motor
03	Motor Stopped OK
07	**Normal Motor Start** Motor Start In Progress (No Jog)
08	Motor Start In Progress (Including Jog)
09	Speed OK Too Soon
0A	Too Long To Get Up To Speed (Retry)
0B	Too Long To Get Up To Speed (Sensor Fault)
0C	Too Many Startup Failures (No Retry)
0D	Too Many Startup Failures (Sensor Fault)
0E	Motor Speed Too High
0F	Motor Speed Too Low
10	Speed Loss Recovery With Seek Error
	Table Continued on Next Page

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TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Motor Stop During Recovery From Speed Drop
11	Unloading Heads
12	Stopping Motor
	Motor Start During Recovery From Speed Drop
18	Motor Start In Progress (Including Jog)
19	Speed OK Too Soon
1A	Too Long To Get Up To Speed (Retry)
1B	Too Long To Get Up To Speed (Sensor Fault)
1C	Too Many Startup Failures (No Retry)
1D	Too Many Startup Failures (Sensor Fault)
1E	Motor Speed Too High
1F	Motor Speed Too Low
	Normal Load
21	Heads Loaded Before Load Begins
22	Fault After Power Amplifier Driver Enabled
25	Demodulator Active Timeout
	Table Continued on Next Page

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Normal Load (Contd)
26	Cylinder Pulse Timeout
27	Fault After Load Complete
28	Code 22 And Too Many Retries
2B	Code 25 And Too Many Retries
2C	Code 26 And Too Many Retries
2D	Code 27 And Too Many Retries
	Normal RTZ
30	Can't Move In From Outer Guard Band
31	Lost Demodulator Active Before Turnaround
33	Timeout During RTZ
34	Backup Into Outer Guard Band
35	Turnaround
36	Out Of Guard Band Too Soon
37	Can't Find Cylinder Pulse At Track -1
38	Can't Find Fine Enable
39	Settle In On Track 0

Table Continued on Next Page

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Normal Guard Bands
40	Inner Guard Band Detected During Normal Seek
41	Inner Guard Band Detected During On Cylinder Routine
42	Inner Guard Band Detected While On Cylinder
43	Outer Guard Band Detected During Normal Seek
44	Outer Guard Band Detected During On Cylinder Routine
45	Outer Guard Band Detected While On Cylinder
	Normal Seek Timeout
46	Seek Timeout
	(Normal) Can't Stop On Track During On Cylinder Routine
47	Too Long To Get On Cylinder Sense
48	Demodulator Active Lost During On Cylinder Routine
49	Too Many Cylinder Pulses During Settle In
4A	Too Many On Cylinder Dropouts
	Table Continued on Next Page

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Normal On Track
4B	Off Cylinder
4C	Lost Demodulator Active While On Cylinder
4E	Voltage Fault While On Cylinder
	(Normal) Illegal Cylinder Address Greater Than 710
4D	Illegal Cylinder Address
	Reset Dummy RTZ Mode Canceled
50	Recovery From Low Vcc Reset
51	Recovery From MPU Hang Reset
52	Recovered From Low Vcc Reset And Subsequent Speed Loss
53	Recovered From MPU Hang And Subsequent Speed Loss
58	Non-Maskable Interrupt
59	Software Interrupt
5B	Too Many Fan Faults (Greater Than 10)
Table Continued on Next Page	

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Reset Dummy RTZ Mode Canceled (Contd)
5C	Fan Fault
5F	PIA Test Failure
80	Fault Before Seek Begins
90	Recovered From Speed Loss
	Servo Test Diagnostics
60	Servo Test Failure During RTZ
61	Servo Test Failure During Recalibrate
62	Servo Test Failure During 1 Track Seek
63	Servo Test Failure During Maximum Length Seek
64	Failed Recalibrate Test
65	1 Track Seek Too Short
66	1 Track Seek Too Long
67	Maximum Length Seek Too Long
68	Maximum Length Seek Too Short
69	Bad Preseek Status
70	Self Test Complete
71	Fan On
72	Execute Switch Does Not Release
	Table Continued on Next Page

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Load And Fault Detected Before Seek Error Was Set
A1	Heads Loaded Before Load Begins
A2	Fault After Power Amplifier Driver Enabled
A5	Demodulator Active Too Late
A6	Cylinder Pulse Timeout
A7	Fault After Load Complete
A8	Code 22 And Too Many Retries
AB	Code 25 And Too Many Retries
AC	Code 26 And Too Many Retries
AD	Code 27 And Too Many Retries
	RTZ And Fault Detected Before Seek Error Was Set
B0	Can't Move In From Outer Guard Band
B1	Lost Demodulator Active Before Turnaround
B3	Timeout During RTZ
B4	Backup Into Outer Guard Band
B5	Turnaround
B6	Out Of Guard Band Too Soon

Table Continued on Next Page

TABLE 3-4. STATUS CODE SUMMARY (Contd)

Status Code	Description
	RTZ And Fault Detected Before Seek Error Was Set (Contd)
B7	Can't Find Cylinder Pulse At Track -1
B8	Can't Find Fine Enable
B9	Settle In On Track 0
	Guard Bands And Fault Detected Before Seek Error Was Set
C0	Inner Guard Band Detected During Normal Seek
C1	Inner Guard Band Detected During On Cylinder Routine
C2	Inner Guard Band Detected While On Cylinder
C3	Outer Guard Band Detected During Normal Seek
C4	Outer Guard Band Detected During On Cylinder Routine
C5	Outer Guard Band Detected While On Cylinder
	Seek Timeout And Fault Detected Before Seek Error Was Set
C6	Seek Timeout
	Table Continued on Next Page

TABLE 3-4.   STATUS CODE SUMMARY (Contd)

Status Code	Description
	Can't Stop On Track During On Cylinder Routine And Fault Detected Before Seek Error Was Set
C7	Too Long To Get On Cylinder Sense
C8	Demodulator Active Lost During On Cylinder Routine
C9	Too Many Cylinder Pulses During Settle In
CA	Too Many On Cylinder Dropouts
	On Track And Fault Detected Before Seek Error Was Set
CB	Off Cylinder
CC	Lost Demodulator Active While On Cylinder
CE	Voltage Fault While On Cylinder
	Illegal Cylinder Address Greater Than 710 And Fault Detected Before Seek Error Was Set
CD	Illegal Cylinder Address
	Reset Dummy RTZ Mode Active
D0	Recovery From Low Vcc Reset
D1	Recovery From MPU Hang Reset
	MPU Power On Test
FF	MPU Failed Power On Test

TABLE 3-5. STATUS CODE DEFINITIONS

Code	Description
00	<u>Title</u>: Normal On Cylinder <u>DESCRIPTION</u>: The MPU sets code 00 following a successful seek. This status indicates normal operation and lasts until the MPU receives a new seek interrupt or unloads the heads. <u>PROBABLE CAUSES</u>: N.A. <u>ACTIONS</u>: N.A.
01	<u>Title</u>: Retracting Heads To Landing Zone <u>DESCRIPTION</u>: The MPU sets code 01 while it is unloading (retracting) the heads. This status lasts approximately 0.2 seconds under normal conditions. If the heads unload, the motor stop sequence begins and the status changes to 02. If the MPU does not detect a demodulator inactive condition, the status remains at 01 and the motor continues to run. <u>PROBABLE CAUSES</u>: Drive continues to detect Demodulator Active pulses due to noise, control circuit failure or power amp failure. <u>ACTIONS</u>: 1. Replace _VCX board (proc 5303). 2. Replace _SWX board (proc 5304). 3. Replace module (proc 5207).
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
02	Title: Stopping Motor DESCRIPTION: The MPU sets this status during the braking period. After MPU timeout (normally 30 seconds) the status changes to 03. PROBABLE CAUSES: N.A. ACTIONS: N.A.
03	Title: Motor Stopped OK DESCRIPTION: The MPU sets code 02 when it detects that the motor is stopped. This code will be displayed following a normal stop sequence. Code will remain at 03 until microprocessor sees START switch turned on and sequence hold from I/O board. PROBABLE CAUSES: N.A. ACTIONS: N.A.
07	Title: Motor Start In Progress (No Jog) DESCRIPTION: Status 07 is displayed, if a voltage fault is present at beginning of start sequence. PROBABLE CAUSES: Power supply defective. ACTIONS: 1. Check for loose cables at P35 and P40. 2. Perform power checks (Proc 4101).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
08	**Title:** Motor Start In Progress (Including Jog) **DESCRIPTION:** Before starting the motor, the MPU causes the heads to move backwards, in jog. Code 08 is displayed until motor reaches full speed and speed OK is set by motor control circuit. **PROBABLE CAUSES:** N.A. **ACTIONS:** N.A.
09	**Title:** Speed OK Too Soon **DESCRIPTION:** Indicates that, during the power on sequence, it took less than 3 seconds for the motor to get up to speed. This condition stops the power on sequence. **PROBABLE CAUSES:** Faulty speed detection circuits. **ACTIONS:** 1. Replace _SWX board (proc 5304). 2. Replace _VCX board (proc 5303).
OA	**Title:** Too Long To Get Up To Speed (Retry) **DESCRIPTION:** OA is displayed during the stop routine if motor did not come up to speed within 25 seconds of starting. Display changes back to 08 during the start routine. If after three tries the motor does not come up to speed, the motor stops and display changes to OC. **PROBABLE CAUSES:** See code OC. **ACTIONS:** See code OC
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
OB	**Title**: Too Long To Get Up To Speed (Sensor Fault) **DESCRIPTION**: Indicates that the drive is performing a retry after the motor did not come up to speed and a sensor fault was detected. OB is displayed only during the stop routine after a start failure. The display changes back to 08 during the start routine. If after three tries the motor does not come up to speed, the motor stops and display changes to OD. **PROBABLE CAUSES**: Motor or motor control board. **ACTIONS**: 1. Replace _SWX board (proc 5304). 2. Replace motor and cable assembly (proc 5210).
OC	**Title**: Too Many Startup Failures (No Retry) **DESCRIPTION**: Indicates that the drive has failed three times to bring the motor up to speed (see code OA). Setting START Switch to Off and back to On causes three more attempts. **PROBABLE CAUSES**: Power supply, motor control circuits, or motor. **ACTIONS**: 1. Check J40 to J35 and J39 to motor wiring. 2. Check +40 volts from power supply. 3. Ensure brake is not energized constantly. If so replace brake (proc 5204). 4. Replace _SWX board (proc 5304). 5. Replace motor and cable assembly (proc 5210).

Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
OD	Title: Too Many Startup Failures (Sensor Fault) DESCRIPTION: Indicates that the drive has failed three times to bring the motor up to speed (see code OA) and a sensor fault has been detected (see code OB). Setting START Switch to Off and back to On causes three more attempts. PROBABLE CAUSES: Motor or motor control board. ACTIONS: 1. Replace _SWX board (proc 5304). 2. Replace motor & cable assembly (proc 5210).
OE OF	Title: Motor Speed Too High Title: Motor Speed Too Low DESCRIPTION: Indicates that the motor speed is too high (OE) or too low (OF). The MPU performs this check after it receives the Speed OK from the _SWX board. When this condition exists, the drive keeps the motor running while continuing, indefinitely, to check motor speed. The heads do not load. PROBABLE CAUSES: Problem with motor speed control or speed detection circuits. ACTIONS: 1. Replace _SWX board (proc 5304). 2. Replace motor & cable assembly (proc 5210).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
10	**Title**: Speed Loss Recovery With Seek Error **DESCRIPTION**: Indicates that drive has recovered from a speed loss and that seek error occurred during the recovery sequence. The heads are floating and Seek Error is active. On Cylinder and Ready signals will go active when the drive receives an RTZ command. **PROBABLE CAUSES**: Motor failure, motor cable or connector, motor control board, or power supply. **ACTIONS**: If more failures occur: 1. Replace power supply (proc 5205). 2. Replace motor & cable assembly (proc 5210). 3. Replace _SWX board (proc 5304).
11 thru 1F	**Title**: Motor Start During Recovery From Speed Drop. **DESCRIPTION**: Same as codes 01 through 0F but occur during recovery from a loss of speed. The codes covered in this discussion are listed below with the corresponding code (without speed drop) given in parentheses. 11 (01) 12 (02) 18 (08) 19 (09) 1A (0A) 1B (0B) 1C (0C) 1D (0D) 1E (0E) 1F (0F) **PROBABLE CAUSES**: See codes 01 through 0F. **ACTIONS**: See Codes 01 through 0F.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
21	Title: Heads Loaded Before Load Begins DESCRIPTION: Indicates a heads loaded condition before the heads moved forward from the retracted position. This error is detected during a load sequence. When the drive displays code 21, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. ACTIONS: 1. Replace _VCX board (proc 5303).
22	Title: Fault After Power Amplifier Driver Enabled DESCRIPTION: Indicates that the drive detected a fault condition after the power amplifier was enabled. The purpose of a check at this time is to detect a voltage fault before enabling current pulses to move the heads forward. When the drive displays code 22, the following error indications also appear.

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TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active. • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, a controller Fault Clear followed by another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 28 and the Fault Clear switch must be pressed to continue. PROBABLE CAUSES: Voltage fault as a result of enabling power amplifier inputs. Extraneous fault, such as Read and Write, caused by I/O problem. ACTIONS: Check LEDs for cause of fault condition. 1. If voltage fault exists: a. Check ±24 volts (proc 4101). If voltages are abnormal, go to ±24 Volt Load Check (TSP3). b. Replace _SWX board (proc 5304). 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _SWX board (proc 5304).
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
25	**Title:** Demodulator Active Timeout **DESCRIPTION:** Indicates that, during a load sequence, Demodulator Active did not go active within 200 ms after the heads started moving forward. When the drive displays code 25, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 29 and the Fault Clear switch must be pressed to continue. **PROBABLE CAUSES:** Bad tribit detection circuit or bad servo disk. **ACTIONS:** 1. Check cabling at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).

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TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
26	**Title:** Cylinder Pulse Timeout **DESCRIPTION:** Indicates that, during a load sequence, the MPU did not detect 100 cylinder pulses within approximately 350 milliseconds after Demodulator Active went active. When the drive displays code 26, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2C and the Fault Clear switch must be pressed to continue. **PROBABLE CAUSES:** Demodulator failure, bad servo disk or cylinder pulse detection circuits. **ACTIONS:** 1. Check cabling at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).

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TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
27	**Title:** Fault After Load Complete **DESCRIPTION:** Indicates that, during a load sequence, the MPU detected a fault just prior to the time that the heads turn around and move back into the guardband. When the drive displays code 27, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2D and the Fault Clear switch must be pressed to continue. **PROBABLE CAUSES:** Voltage fault due to defective voltage regulator, power supply, power amplifier, or voice coil. Extraneous fault, such as Read and Write, caused by I/O problem. **ACTIONS:** Check LEDs for cause of fault condition.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	1. If voltage fault exists: a. Check ±24 volts (proc 4101). If voltages are abnormal, go to (TSP3) ±24 Volt Load Check. b. Replace _SWX board (proc 5304). c. Replace _VCX board (proc 5303). d. Replace module (proc 5207). 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _SYX/_TQX board (proc 5302).
28 thru 2D	<u>Title</u>: Error Conditions With Too Many Retries <u>DESCRIPTION</u>: Indicates that more than five RTZ error recovery attempts were made following the associated error (codes 22 through 27). After five attempts, the MPU sets one of the codes 28 through 2D and prevents further retries. Pressing the Fault Clear switch clears the error and allows five more retries. The codes covered in this discussion are listed below with the corresponding code (without too many retries) given in parentheses. <u>PROBABLE CAUSES</u>: See codes 22 through 27. <u>ACTIONS</u>: See codes 22 through 27. 28 (22) 2B (25) 2C (26) 2D (27)
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
30	**Title**: Can't Move In From Outer Guardband **DESCRIPTION**: Indicates, during a load or RTZ, that heads were moving in too fast to allow a turnaround in the data zone. Attempting a turnaround could result in the heads moving completely through the data zone, resulting in loss of servo control. When the drive displays code 30, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt. **PROBABLE CAUSES**: Problem with velocity circuits. **ACTIONS**: 1. Initiate RTZ, if error repeats, replace _VCX board (proc 5303).

Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
31	**Title**: Lost Demodulator Active Before Turnaround **DESCRIPTION**: Indicates that during backup portion of RTZ, Demodulator Active went inactive. This indicates that the heads may have moved back through the outer guardband to the outer surface of the disk, without generating outer guardband pulses. When the drive displays code 31, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt. **PROBABLE CAUSES**: Bad servo disk, loose connection or failure that causes loss of velocity control. **ACTIONS**: 1. Check cabling at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
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TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
33	**Title:** Timeout During RTZ **DESCRIPTION:** Indicates that during the backup portion of a load or RTZ, too much time elapsed before the heads reached the outer guardband. When the drive displays code 33, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another load. **PROBABLE CAUSES:** Failure in velocity circuits, bad power amplifier or power amplifier driver circuits. **ACTIONS:** 1. Replace _SWX board (proc 5304). 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
34	**Title:** Backup Into Outer Guardband **DESCRIPTION:** Code 34 is set when the outer guardband is detected during the backup phase of a load or RTZ seek. It normally remains set only until turnaround, when the code changes to 35. If the display stays at 34, it indicates either a timeout (too long to count 2 cylinder pulses) or Demodulator Active inactive error. The following error indications appear in addition to code 34. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. **PROBABLE CAUSES:** Bad tribit decoder circuit or servo disk.

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TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
35	Title: Turnaround DESCRIPTION: Code 35 is set at the turnaround point following the backup phase of a load or RTZ seek. This is the point where two cylinder pulses have been counted, reverse is cleared, and forward is set. Code 35 normally remains set only until the heads move forward four tracks thus bringing the heads to track -1 (preceding cylinder 0) and changing the code to 37. If the display stays at 35, it indicates either a timeout (too long to count 1 cylinder pulse) or Demodulator Active inactive error. The following error indications appear in addition to code 35. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces.

Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit or servo disk. ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
36	Title: Out Of Guardband Too Soon DESCRIPTION: Indicates, during a load or RTZ, that the the drive detected less than one cylinder pulse before the heads moved out of the outer guardband. When the drive displays code 36, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. <u>PROBABLE CAUSES</u>: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. <u>ACTIONS</u>: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
37	<u>Title</u>: Can't Find Cylinder Pulse At Track -1 <u>DESCRIPTION</u>: Indicates that, during a load or RTZ, either Demodulator Active went inactive or too much time elapsed while the drive was looking for track -1 (track preceding cylinder 0). When the drive displays code 37, the following error indications also appear.

Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run. • The servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
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TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
38	**Title**: Can't Find Fine Enable **DESCRIPTION**: Indicates that, during a load or RTZ, either Demodulator Active went inactive or too much time elapsed while the drive was waiting for Fine Enable to go active. When the drive displays code 38, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run. • The servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. **PROBABLE CAUSES**: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.
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TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
39	Title: Settle In On Track 0 DESCRIPTION: Code 39 is set when the heads are within 1/2 track of cylinder 0. It normally remains set only until the heads are on cylinder and the display changes to 0. If the display stays at 39, it indicates that either Demodulator Active went inactive or too much time elapsed before on cylinder went active. The following error indications appear in conjunction with code 39 (B9). If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	• The servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
40	Title: Inner Guardband Detected During Normal Seek DESCRIPTION: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 40, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, defective servo surface, bad tribit decoder circuits, or electrical noise generated by nearby equipment. ACTIONS: 1. Ensure that drive is not located near source of extreme electrical noise. 2. Check for loose cable at J28 on _VCX board. 3. Replace _VCX board (proc 5303). 4. Replace module (proc 5207).
41	Title: Inner Guardband Detected During On Cylinder Routine DESCRIPTION: Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 41, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS: 1. Ensure that drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
42	Title: Inner Guardband Detected While On Cylinder DESCRIPTION: Indicates that inner guardband pulses were detected while the heads were on cylinder. When the drive displays code 42, the following error indications also appear:

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TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS: 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
43	Title: Outer Guardband Detected During Normal Seek DESCRIPTION: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 43, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits or by electrical noise generated by nearby equipment. ACTIONS: 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
44	Title: Outer Guardband Detected During On Cylinder Routine DESCRIPTION: Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 44, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run.
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TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTION: 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
45	Title: Outer Guardband Detected While On Cylinder DESCRIPTION: Indicates that outer guardband pulses were detected while the heads were on cylinder. When the drive displays code 45, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Seek Error goes active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS: 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
46	Title: Seek Timeout DESCRIPTION: Indicates that during a normal seek the drive took longer than 60 milliseconds to reach on cylinder. When the drive displays code 46, the following error indications also appear. • Seek error and Seek End lines go active. • Motor continues to run but servo system is disabled and the heads, although loaded, drift freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Problem with voice coil or velocity circuits.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS: 1. Replace _VCX board (proc 5303). 2. Replace _SWX board (proc 5304).
47	**Title**: Too Long to Get On Cylinder Sense **DESCRIPTION**: Indicates that too much time elapsed from Fine Enable going active to On cylinder going active. When the drive displays code 47, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: On cylinder sense circuits not functioning. ACTIONS: 1. Replace _VCX board (proc 5303). 2. Replace module (proc 5207).
48	Title: Demodulator Active Lost During On Cylinder Routine DESCRIPTION: Indicates that Demodulator Active went inactive as the heads approached on cylinder. When the drive displays code 48, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load and seek to cylinder 0.

Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop. ACTIONS: Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace module. 2. If error occurs at random locations, check for loose cable at J28 on _VCX board. 3. If problem still exists, replace __VCX board (proc 5303).
49	Title: Too Many Cylinder Pulses During Settle In DESCRIPTION: Indicates that three or more cylinder pulses were detected during settle in thus indicating excessive overshoot. Excessive overshoot can result in the heads settling on the wrong cylinder. When the drive displays code 49, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Velocity or cylinder pulse detection circuits. ACTIONS: 1. Check for loose cable at J28 on _VCX board. 2. Replace _VCX board (proc 5303).
4A	Title: Too Many On Cylinder Dropouts DESCRIPTION: Indicates that On Cylinder Sense took too long to stabilize during the settle in phase. When the drive displays code 4A, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, defective module, bad tribit decoder circuits, or electrical noise generated by nearby equipment. ACTIONS: 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VCX board (proc 5303). 3. Replace module (proc 5207).
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
4B	**Title**: Off Cylinder **DESCRIPTION**: Indicates that either On Cylinder Sense went inactive or cylinder pulses were detected while On Cylinder was active. When the drive displays code 4B, the following error indications also appear. • On Cylinder goes inactive. • Seek Error goes active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk. An RTZ command clears the seek error and initiates a seek to cylinder 0. **PROBABLE CAUSES**: Bad servo disk, loose cabling in feedback loop, or poor tracking due to mechanical or electrical noise problems. **ACTIONS**: 1. Ensure that malfunction was not caused by excessive vibration levels (for example, from nearby construction activities or nearby electrical noise (for example, line printers). 2. If error occurs at same cylinder each time, replace module (proc 5207). 3. If error occurs at random locations: a. Check for loose cable at J28 on _VCX board. b. Replace _VCX board (proc 5303). c. Replace module (proc 5207).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
4C	<u>Title</u>: Lost Demodulator Active While On Cylinder <u>DESCRIPTION</u>: Indicates that Demodulator Active went inactive while the heads were on cylinder. When the drive displays code 4C, the following error indications also appear. • On Cylinder goes inactive. • Seek Error goes active. • Motor continues to run. An RTZ command clears the seek error and initiates a load and seek to cylinder 0. <u>PROBABLE CAUSES</u>: Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop. <u>ACTIONS</u>: Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace module. 2. If error occurs at random locations: a. Check for loose cable at J28 on _VCX board. b. If problem still exists, replace _VCX board (proc 5303).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
4D	**Title**: Illegal Cylinder Address **DESCRIPTION**: Indicates that, during a normal seek, the MPU received too high a cylinder address (greater than 710). When the drive displays code 4D, the following error indications also appear. • On Cylinder goes inactive. • Seek Error and Seek End go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. **PROBABLE CAUSES**: Illegal address sent to _VCX by _SYX/_TQX board (defective I/O board). **ACTIONS**: 1. Replace _SYX/_TQX board (proc 5302). 2. Replace _VCX board (proc 5303). 3. Replace _UGX/_VHX board (proc 5301).
4E	**Title**: Voltage Fault While On Cylinder **DESCRIPTION**: Indicates that the MPU detected a voltage fault while On Cylinder was active. When the drive displays code 4E, the following error indications also appear. • READY indicator goes out and Ready line goes inactive.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	● Seek Error goes active. ● FAULT indicator lights and Fault line goes active. ● Motor continues to run. If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0. PROBABLE CAUSES: Power failure within drive, power supply or site power. ACTIONS: Check LEDs for cause of fault condition. 1. If voltage fault exists go to Power Check (TSP1).
50	Title: Recovering From Low Vcc Reset DESCRIPTION: Indicates that recovery from low Vcc reset has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights. The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault Clear switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Momentary power supply or site power failure. **ACTIONS**: 1. If more resets occur check site power, power supply, and drive power wiring.
51	**Title**: Recovering From MPU Hang Reset **DESCRIPTION**: Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. **PROBABLE CAUSES**: Chip failure in MPU system causing instruction to be read incorrectly from EPROM. **ACTIONS**: 1. Replace _VCX board (proc 5303).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
52	**Title:** Recovered From Low Vcc Reset and Subsequent Speed Loss **DESCRIPTION:** Indicates that the heads are floating after recovery from a low Vcc reset followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ. **PROBABLE CAUSES:** Momentary power supply or site power failure. **ACTIONS:** 1. If more resets occur check site power, power supply, and drive power wiring.
53	**Title:** Recovered From MPU Hang And Subsequent Speed Loss **DESCRIPTION:** Indicates that the heads are floating after recovery from an MPU hang followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ. **PROBABLE CAUSES:** Microprocessor failed or conditions existed that caused it to hang in an illegal mode. **ACTIONS:** 1. Replace _VCX board (proc 5303).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
58	**Title**: Non-Maskable Interrupt **DESCRIPTION**: A non-maskable interrupt was detected by the microprocessor even though this type of interrupt should never occur. **PROBABLE CAUSES**: Microprocessor failed or problem with logic on control board. **ACTION**: 1. Replace _VCX board (proc 5301).
59	**Title**: Software Interrupt **DESCRIPTION**: A software interrupt was detected by the microprocessor even though this type of interrupt should never occur. **PROBABLE CAUSES**: Microprocessor failed or problem with logic on control board. **ACTION**: 1. Replace _VCX board (proc 5303).
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
5B 5C	**Title**: Too Many Fan Faults (Greater Than 10) **Title**: Fan Fault **DESCRIPTION**: Indicates that the drive cooling fan has failed. If the fan fault stays set for greater than 400 ms, the drive will stop (similar to using start switch to stop drive) and code 5C will be displayed. During this period, the MPU will continually attempt to clear the fault. If the MPU is successful in clearing the fault, the drive will start; (provided no other faults are present). If ten fan faults occur, the MPU will display code 5B and make no further attempts to clear the fault. In this case the drive must be powered off before another load attempt. **PROBABLE CAUSES**: Clogged air filter, defective cooling fan or dc voltage is missing from fan cable. **ACTION**: 1. If fan is running: a. Check air filter. Clean or replace filter if dirty. b. Replace _SYX/_TQX (Proc 5302). 2. If fan is not running: a. If -24 volts is present at fan connector, replace fan (proc 5201). b. If -24 volts is not present, go to -24 Volt Power Check (TSP3).
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
5F	**Title:** PIA Test Failure **DESCRIPTION:** Indicates that, during power on initialization, the MPU detected a PIA failure. When this occurs the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CB1 to Off and then back to On. **PROBABLE CAUSES:** Bad PIA or defective chip in MPU system. **ACTIONS:** 1. Replace _VCX board (proc 5303).
80	**Title:** Fault Before Seek Begins **DESCRIPTION:** Indicates that a fault condition existed when a normal or RTZ seek was commanded. When the drive displays code 80, the following error indications also appear. • Seek Error and Seek End go active. • Ready goes inactive. • FAULT indicator lights and Fault line goes active. • For a voltage fault, the motor continues to run but heads are unloaded via emergency retract. • For other than a voltage fault, the motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces.
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0. PROBABLE CAUSES: Any of the possible fault conditions. ACTIONS: 1. Check fault LEDs on Status/Fault Display board.
90	Title: Recovered From Speed Loss DESCRIPTION: Indicates that drive has recovered from a speed loss. The heads are loaded but floating and Seek Error is active. On Cylinder and Ready will go active when the drive receives an RTZ. PROBABLE CAUSES: Motor control circuit, motor failure or power supply failure. ACTIONS: If more failures occur: 1. Replace _SWX board (proc 5304). 2. Replace power supply (proc 5205). 3. Replace motor and cable assembly (Proc 5210).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
60	**Title:** Servo Test Failure During RTZ **DESCRIPTION:** Indicates that the drive failed to complete an RTZ operation. The test is initiated with the heads at cylinder zero and requires that the carriage move two cylinders into the outer guardband and then return to cylinder zero. **PROBABLE CAUSES:** MPU failure, break in the cabling between the control board and the module, module failure, power amp failure, or power supply failure. **ACTIONS:** 1. Replace _VCX board (proc 5303). 2. Check cabling between _SWX board and module. 3. Replace _SWX board (proc 5304). 4. Replace module (proc 5207). 5. Replace power supply (proc 5205).
61	**Title:** Servo Failure During Recalibrate **DESCRIPTION:** Indicates that the drive failed to complete six 128-track seeks repeated three times. All seeks start at cylinder zero with a destination of cylinder 127. **PROBABLE CAUSES:** MPU failure, break in the cabling between the control board and the module, module failure, power amp failure, or power supply failure.

Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
	<u>ACTIONS</u>: 1. Replace _VCX board (proc 5303). 2. Check cabling between _SWX board and module. 3. Replace _SWX board (proc 5304). 4. Replace module (proc 5207). 5. Replace power supply (proc 5205).
62	<u>Title</u>: Servo Test Failure During 1 Track Seek <u>DESCRIPTION</u>: Indicates that the drive failed to complete a series of 16 one-track seeks. All seeks originate at cylinder zero and terminate at cylinder one. <u>PROBABLE CAUSES</u>: MPU failure, break in the cabling between the control board and the module, module failure, power amp failure, or power supply failure. <u>ACTIONS</u>: 1. Replace _VCX board (proc 5303). 2. Check cabling between _SWX board and module. 3. Replace _SWX board (proc 5304). 4. Replace module (proc 5207). 5. Replace power supply (proc 5205).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
63	**Title**: Servo Test Failure During Maximum Length Seek **DESCRIPTION**: Indicates that the drive failed to complete a series of sixteen 710-track seeks. All seeks originate at cylinder zero and terminate at cylinder 710. **PROBABLE CAUSES**: MPU failure, break in the cabling between the control board and the module, module failure, power amp failure, or power supply failure. **ACTIONS**: 1. Replace _VCX board (proc 5303). 2. Check cabling between _SWX board and module. 3. Replace _SWX board (proc 5304). 4. Replace module (proc 5207). 5. Replace power supply (proc 5205).
64	**Title**: Failed Recalibrate Test **DESCRIPTION**: Indicates that the servo logic failed to complete the same servo gain number three consecutive times while executing test 61. **PROBABLE CAUSES**: MPU failure or power supply failure. **ACTIONS**: 1. Replace _VCX board (proc 5303). 2. Replace power supply (proc 5205).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
65	Title: 1 Track Seek Too Short DESCRIPTION: Indicates that the drive executed the series of 16 one-track seeks in test 62 too fast. PROBABLE CAUSES: MPU failure. ACTION: 1. Replace _VCX board (proc 5303).
66	Title: 1 Track Seek Too Long DESCRIPTION: Indicates that the drive executed the series of 16 one-track seeks in test 62 too slowly. PROBABLE CAUSES: MPU failure. ACTION: 1. Replace _VCX board (proc 5303).
67	Title: Maximum Length Seek Too Fast DESCRIPTION: Indicates that the drive executed the series of sixteen 710-track seeks in test 63 too fast. PROBABLE CAUSES: MPU failure. ACTION: 1. Replace _VCX board (proc 5303).
	Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
68	**Title**: Maximum Length Seek Too Slow **DESCRIPTION**: Indicates that the drive executed the series of sixteen 710-track seeks in test 63 too slow. **PROBABLE CAUSES**: MPU failure. **ACTION**: 1. Replace _VCX board (proc 5303).
69	**Title**: Bad Preseek Status **DESCRIPTION**: Indicates that drive was not ready at the time a seek operation was initiated. **PROBABLE CAUSES**: Fault detection circuitry not functioning. **ACTION**: 1. Replace _SYX/_TQX board (proc 5302).
70	**Title**: Self Test Complete **DESCRIPTION**: Indicates that the drive successfully completed the power up tests. **PROBABLE CAUSES**: N.A. **ACTION**: N.A.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
71	__Title__: Fan On __DESCRIPTION__: Indicates that the fan is at normal operating speed. __PROBABLE CAUSES__: N.A. __ACTION__: N.A.
72	__Title__: Execute Switch Does Not Release __DESCRIPTION__: Execute switch does not go to inactive state after a timeout following release. This prevents any use of the Fault Display panel. __PROBABLE CAUSES__: 1. Faulty Execute switch. 2. Short to ground in switch wiring. __ACTIONS__: 1. Replace _UQX Fault Display panel (proc 5203). 2. Troubleshoot switch wiring.
Al thru CE	__Title__: Error conditions with Fault present. __DESCRIPTION__: The following codes correspond to codes previously listed, except that the Fault line is active when they are observed. The codes covered in this discussion are listed below with the corresponding (No Fault) code given in parentheses.

<div align="center">Table Continued on Next Page</div>

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	A1 (21) A2 (22) A5 (25) A6 (26) A7 (27) A8 (28) AB (2B) AC (2C) AD (2D) BO (30) B1 (31) B3 (33) B4 (34) B5 (35) B6 (36) B7 (37) B8 (38) B9 (39) CO (40) C1 (41) C2 (42) C3 (43) C4 (44) C5 (45) C6 (46) C7 (47) C8 (48) C9 (49) CA (4A) CB (4B) CC (4C) CD (4D) CE (4E) When the drive displays one of the A1 through CE codes the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active. • Seek Error and Seek End lines go active (not during first seek). • Motor continues to run. If the fault condition no longer exists, a Controller Fault Clear followed by an RTZ or pressing the Fault Clear switch clears the fault and initiates another load. PROBABLE CAUSES: Voltage fault caused by failure within drive, site power, or power supply. Extraneous fault, such as ; ad and write, caused by I/O problem. ACTIONS: Check LEDs for cause of fault condition. 1. If voltage fault exists: a. Check ±24 volts (TSP1). If voltages are abnormal, go to ±24 Volt Load Check (TSP3). b. Replace power supply (proc 5205).

Table Continued on Next Page

TABLE 3-5. STATUS CODE DEFINITIONS (Contd)

Code	Description
	2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _SYX/_TQX board (proc 5302).
D0	Title: Recovering From Low Vcc Reset DESCRIPTION: Indicates that recovery from low Vcc has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights. Code D0 remains set until the Fault line goes inactive. The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault Clear switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received. PROBABLE CAUSES: Momentary power failure. ACTIONS: 1. If more resets occur, check site power, power supply and drive power wiring.
	Table Continued on Next Page

TABLE 3-5.   STATUS CODE DEFINITIONS (Contd)

Code	Description
D1	**Title:** Recovering From MPU Hang Reset **DESCRIPTION:** Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. Code D1 remains set until the Fault line goes inactive. If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. **PROBABLE CAUSES:** Chip failure in MPU system causing instruction mode to be read incorrectly from EPROM. **ACTIONS:** 1. Replace _VCX board (proc 5303).
FF	**Title:** MPU Failed Power On Test **DESCRIPTION:** Indicates that MPU failed power on initialization test. When this occurs, the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CB1 to OFF and then back to ON. **PROBABLE CAUSES:** Bad MPU, RAM, or other failure preventing MPU from operating. **ACTIONS:** 1. Check for a failure in the +5 volts and +24 volts power supply (proc 4101). 2. Replace _VCX board (proc 5303).

SECTION 4

ELEC-TRICAL CHECKS

4. ELECTRICAL CHECKS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in Section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains electrical checks intended for use in isolating problems causing improper drive operation. These procedures should be used in conjunction with the troubleshooting information in section 3.

If the drive appears to be operating properly, failure to meet a specification given here does not in itself indicate improper drive operation. The person performing these procedures should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

When performing electrical checks, refer to section 2, figure 2-3 (component locator) for pin orientation of test points J80, J81 and J82.

Each electrical check procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedure numbers are organized into five categories: 41XX - power checks, 42XX - servo checks, 43XX - write checks, 44XX - read checks, and 45XX - miscellaneous.

The procedures appear in the following order.
- 4101 - Power Checks
- 4201 - Tribit Check
- 4202 - Position Signal Check
- 4203 - Servo Offset Check
- 4204 - On Cylinder Check

- 4301 – Write Fault Grounding (340 MB)
- 4302 – Write PLO Check (340 MB)
- 4303 – Write Data Check (340 MB)
- 4304 – Write Address Mark Check (340 MB)
- 4305 – Write Fault Grounding (515 MB)
- 4306 – Write PLO Check (515 MB)
- 4307 – Write Data Check (515 MB)
- 4308 – Write Address Mark Check (515 MB)
- 4401 – Read PLO Check (340 MB)
- 4402 – Read Data Check (340 MB)
- 4403 – Read Address Mark Check (340 MB)
- 4404 – Read PLO Check (515 MB)
- 4405 – Read Data Check (515 MB)
- 4406 – Read Address Mark Check (515 MB)
- 4501 – Index Check
- 4502 – Sector Check

4101 - POWER CHECKS

The following procedure provides an overall check of the dc voltages used by the drive. Table 4-1, shows the voltages required by each drive component. See the diagrams section of hardware maintenance manual volume 3 for specific information concerning voltage test points.

CAUTION

Because some voltage measurements are on pins adjacent to each other, it is possible to touch both pins simultaneously, thus causing a short circuit. A short circuit will cause serious damage to drive electronic assemblies. Therefore, use extreme caution when performing the following steps.

1. Command continuous seeks between cylinder 0 and 256.

2. Connect voltmeter ground lead to ground (chassis).

TABLE 4-1. DC VOLTAGE DISTRIBUTION

Component	Voltage					
	+5V	-5V	-8.3V	+24V	-24V	+40V
_VCX	X	X	X	X	X	
_UGX/_VHX	X	X				
_SYX/_TQX	X	X			X	
_SWX	X	X		X	X	X
_UQX	X					
_STX*	X	X	X			
Fan					X	
Motor*	X					X
Brake				X		
Op Pnl (_PBX)	X					

*Located in Module

3. Measure between ground and the appropriate connection points to check the following voltages:

Voltage	Connection	Specification
+5 volts	J82-5 (_SWX)	+4.90 to +5.25 volts
-5 volts	J82-7 (_SWX)	-4.90 to -5.30 volts
-8.3 volts	Loc. C305 (_VCX)	-8.1 to -8.5 volts
+24 volts	J82-2 (_SWX)	+21.6 to +26.4 volts
-24 volts	J82-3 (_SWX)	-21.6 to -26.4 volts
+40 volts	J82-4 (_SWX)	+36 to +42 volts

4. Proceed to next test or return drive to online operation.

SERVO CHECKS

4201 - TRIBIT CHECK

1. Connect oscilloscope as shown on figure 4-1.

2. Command direct seek to cylinder 0.

NOTE

- An occasional Seek Error may occur, when oscilloscope probes are attached to servo signal testpoints.

- Servo signal will not be present if heads are in landing zone. If this condition occurs, check for proper operation of carriage locking solenoid.

3. Observe that the relationship between +Tribit and -Tribit signals is similar to that on figure 4-1.

4. Connect oscilloscope as shown on figure 4-2.

5. Observe that the Tribit (AGC'd) signals are similar to that on figure 4-2.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	20 MV/CM	B407 ON VCX /2\	+TRIBITS
CH 2	20 MV/CM	B507 ON VCX /2\	-TRIBITS

/1\

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 µS/CM   MODE: ALT

NOTES:

/1\ X1 PROBES MUST BE USED.

/2\ CONNECT SCOPE PROBE TO COMPONENT LEAD
FARTHEST FROM THE BOARD EDGE.
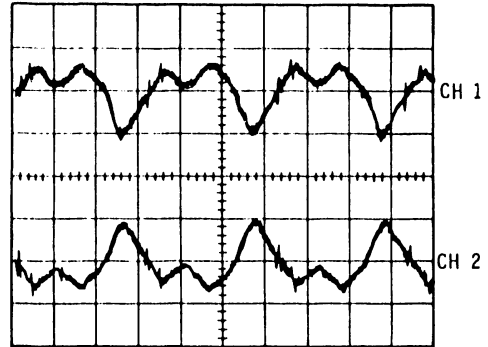
11D116B

Figure 4-1.   Servo Signal Waveform

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.2 V/CM	C117 ON VCX /1\	- TRIBIT (AGC'D)
CH 2	0.2 V/CM	B519 ON VCX /1\	+ TRIBIT (AGC'D)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 µS/CM   MODE: ALT

NOTES:

/1\ CONNECT SCOPE PROBE TO COMPONENT LEAD
CLOSEST TO THE BOARD EDGE.
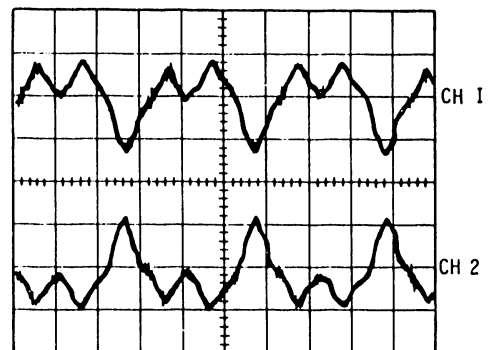
11D117B

Figure 4-2.   Tribits (AGC'd) Waveform

4202 - POSITION SIGNAL CHECK

1. Connect oscilloscope as shown on figure 4-3.

2. Command continuous seeks between cylinders 0 and 256.

3. Observe that the peak to peak value of -Position signal over the period of a complete seek is approximately as shown in figure 4-3.

4. Command continuous seeks between cylinders 0 and 710 and observe that -Position is as described in step 3 (see figure 4-4).

5. Return drive to online operation.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J80-7 ON _VCX	- POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT	TP-J80-4 ON _VCX	- FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM   MODE: CH 1

NOTES:
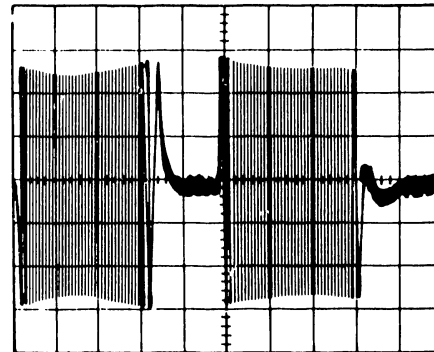
11D118

Figure 4-3. Position Signal (Tracks 0-256)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	2.0 V/CM	TP-J80-7 ON _VCX	- POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	TP-J80-4 ON _VCX	- FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X1O PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM   MODE: CH 1
NOTES:
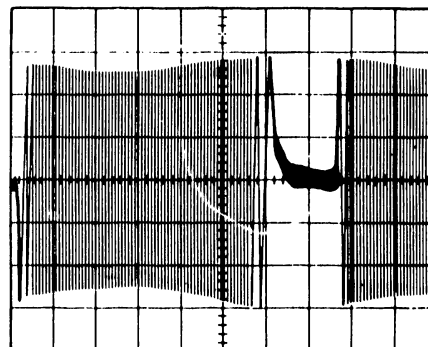
11D119

Figure 4-4.   Position Signal (Tracks 0 to 710)

4203 - SERVO OFFSET CHECK

This procedure checks the amount of head offset caused by a servo offset command. The measurement is made on the -Position signal. The -Position signal has an average dc level of zero, when there is no offset and the heads are on cylinder.

1.   Connect digital voltmeter between J80-7 (_VCX) and ground (chassis).

2.   Command direct seek to cylinder 0 and observe that meter indicates 0 ±50 millivolts.

3.   Command a read operation with positive (forward) offset and observe that meter indicates an average dc offset between +0.60 and +0.90 volts.

4.   Command a read operation with negative (reverse) offset and observe that meter indicates an average dc offset between -0.60 and -0.90 volts.

5.   Proceed to next test or return drive to online operation.

4204 - ON CYLINDER CHECK

This procedure verifies that On Cylinder goes active.

1. Connect oscilloscope as follows:

   a. Connect channel 1 to TP-J81-9 (+On Cylinder) on _SYX/_TQX board.

   b. Trigger +Internal.

   c. Set other controls as appropriate to make measurement in step 3.

2. Command continuous seeks between cylinders 0 and 1.

3. Observe that +On Cylinder goes active.

4. Proceed to next test or return drive to online operation.

WRITE CHECKS (340 MB)

GENERAL

The following procedures, 4301 through 4304, check various aspects of the 340 MB drive write circuit operation. Figure 4-5 is a block diagram showing the major components in the write circuits and the test points used in the procedures.

4301 - WRITE FAULT GROUNDING (340 MB)

If a write fault condition exists, the drive write circuits are disabled. This makes it difficult to test the write circuits and isolate the problem. Grounding the Write Fault signal at the point where it leaves the _UGX board disables the write fault function thus allowing the drive to perform write operations even though fault conditions exist. The following procedure describes the proper method for grounding the Write Fault signal.
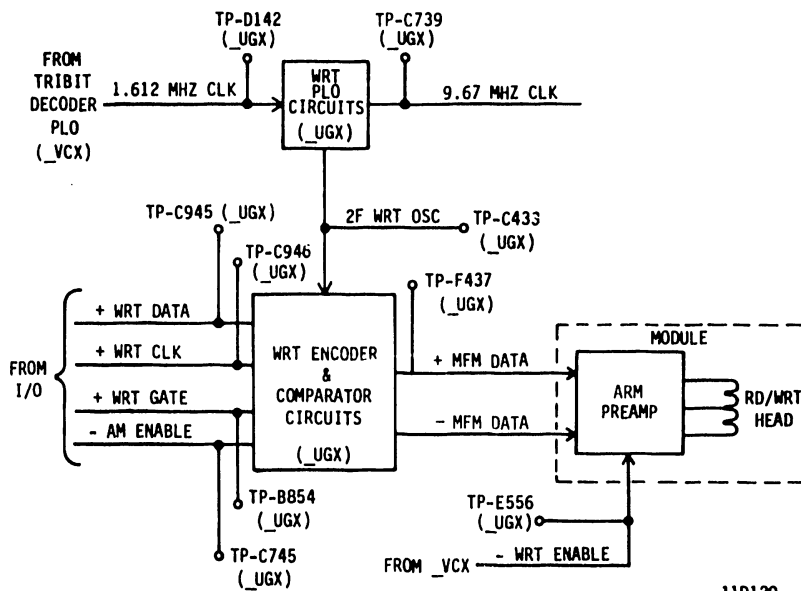
Figure 4-5. Write Circuits Test Points (340 MB)

CAUTION

Perform this procedure only during trouble-shooting when a write fault condition inter-feres with isolating the problem.

1. Remove power from drive as follows:

   a. Press START switch to stop motor and unload heads.

   b. Set CB1 to off.

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can result in loss of customer data.

2. Connect jumper wire between TP-C743 (Write Fault) and TP-A244 (ground) on _UGX board.

3. Power up drive and perform tests. Monitor TP-J81-12 (Fault) on _SYX/_TQX board to determine if write fault condition persists. When testing is complete, remove jumper wire.

4302 - WRITE PLO CHECK (340 MB)

This procedure checks the operation of the write PLO. The PLO provides timing signals used, during write operations by both the drive and controller.

1. Connect oscilloscope and observe that 1.612 MHz Clock frequency is approximately as shown on figure 4-6.

2. Connect oscilloscope and observe that 9.67 MHz Clock frequency is approximately as shown on figure 4-7.

3. Connect oscilloscope and observe that 2F Write Oscillator timing is approximately 19.34 MHz (see figure 4-8).

4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D142 ON UGX	1.612 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 uS/CM   MODE:

NOTES:
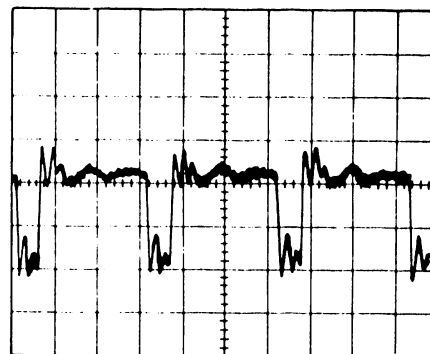
11D121

Figure 4-6. 1.612 MHz Clock Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-C739 ON _UGX	+9.67 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM   MODE:

NOTES:

103 ± 2 NS
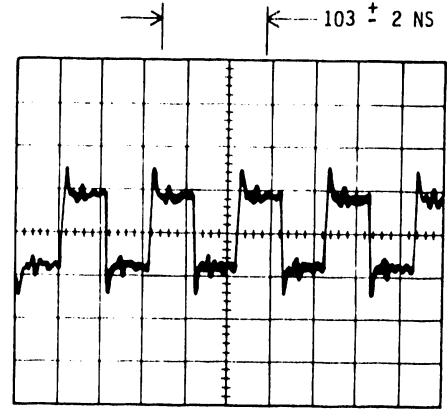
11D122

Figure 4-7.   9.67 MHz Servo Clock Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-C433 ON _UGX	+ 2F (WRT OSC)
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM   MODE:

NOTES:
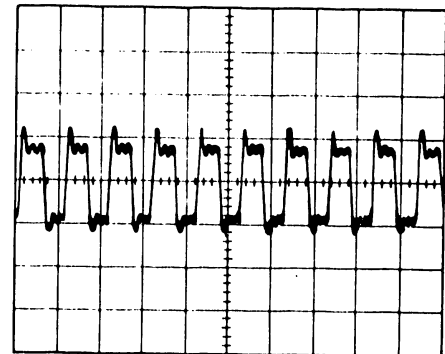
11D123

Figure 4-8.   2F Write Oscillator Timing (340 MB)

83324770 B

4303 - WRITE DATA CHECK (340 MB)

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-5). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding to perform a write operation.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head.

2. Command drive to write a 1010... pattern.

3. Connect oscilloscope and observe that Write Gate and Write Enable appear as shown on figure 4-9.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	2.0 V/CM	TP-B854 ON _UGX	+ WRT GATE
CH 2	2.0 V/CM	TP-E556 ON _UGX	- WRT ENABLE

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 MS/CM   MODE: ALT

NOTES:
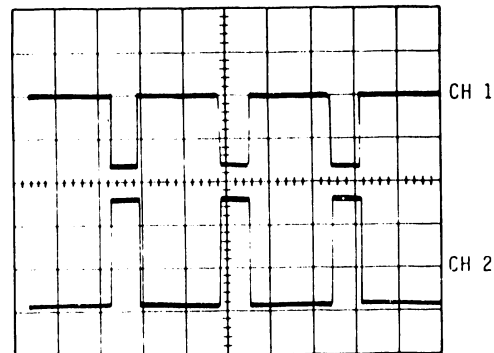
11D128

Figure 4-9. Write Gate Timing (340 MB)

83324770 B

4. Check inputs to write encoder and compensation circuits. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.

   a. Connect oscilloscope as shown on figure 4-10 and observe that Write Clock frequency is approximately 9.67 MHz.

   b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-10. Write Clock should go positive at approximately the center of the data "1" pulses.

5. Check write data input control circuits as follows:

   a. Connect oscilloscope as shown on figure 4-11.

   b. Observe that Write Data to MFM Data pulses are similar to those on figure 4-11.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C945 ON _UGX	+ WRT DATA
CH 2	0.5 V/CM	TP-C946 ON _UGX	+ WRT CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:
   1. DISREGARD ANY GHOST IMAGES.
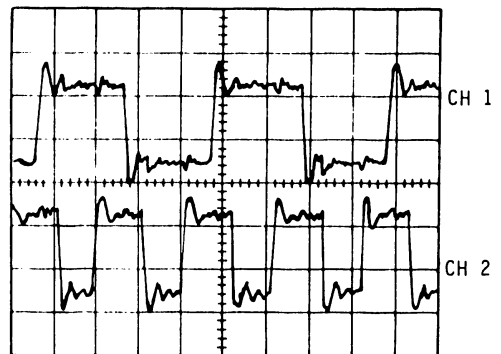
11D129

Figure 4-10.   Write Data to Clock Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-F437 ON _UGX	+ MFM DATA
CH 2	0.5 V/CM	TP-C945 ON _UGX	+ WRITE DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 µS/CM   MODE: ALT

NOTES:

    1. DISREGARD ANY GHOST IMAGES.

11D124
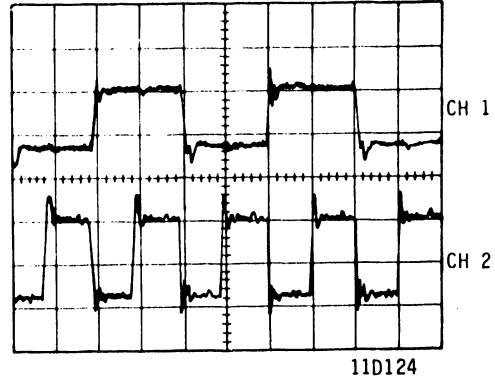
Figure 4-11. Write Data Timing (340 MB)

4304 - WRITE ADDRESS MARK CHECK (340 MB)

This procedure verifies that the drive is not writing during the time that Address Mark Enable is active.

    1.   Command continuous write format with address mark operations using a 1010... data pattern.

    2.   Connect oscilloscope as shown on figure 4-12.

CAUTION

        To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

    3.   Observe that there are no data "1" pulses during the time that Address Mark Enable is active.

    4.   Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C745 ON __UGX	- AM ENABLE
CH 2	0.5 V/CM	TP-F437 ON __UGX	+ MFM DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM   MODE: ALT

NOTES:
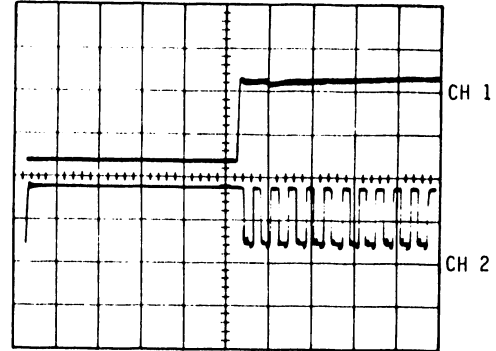
11D125

Figure 4-12.   Write Address Mark Timing (340 MB)

WRITE CHECKS (515 MB)

GENERAL

The following procedures, 4305 through 4308, check various as-
pects of the 515 MB drive write circuit operation. Figure 4-13
is a block diagram showing the major components in the write
circuits and the test points used in the procedures. All ref-
erences to the __VHX read/write board apply also to the __SUX
read/write board (used on older drives).

4305 - WRITE FAULT GROUNDING (515 MB)

If a write fault condition exists, the drive write circuits are
disabled. This makes it difficult to test the write circuits
and isolate the problem. Grounding the Write Fault signal at
the point where it leaves the __VHX board disables the write
fault function thus allowing the drive to perform write opera-
tions even though fault conditions exist. The following proce-
dure describes the proper method for grounding the Write Fault
signal.
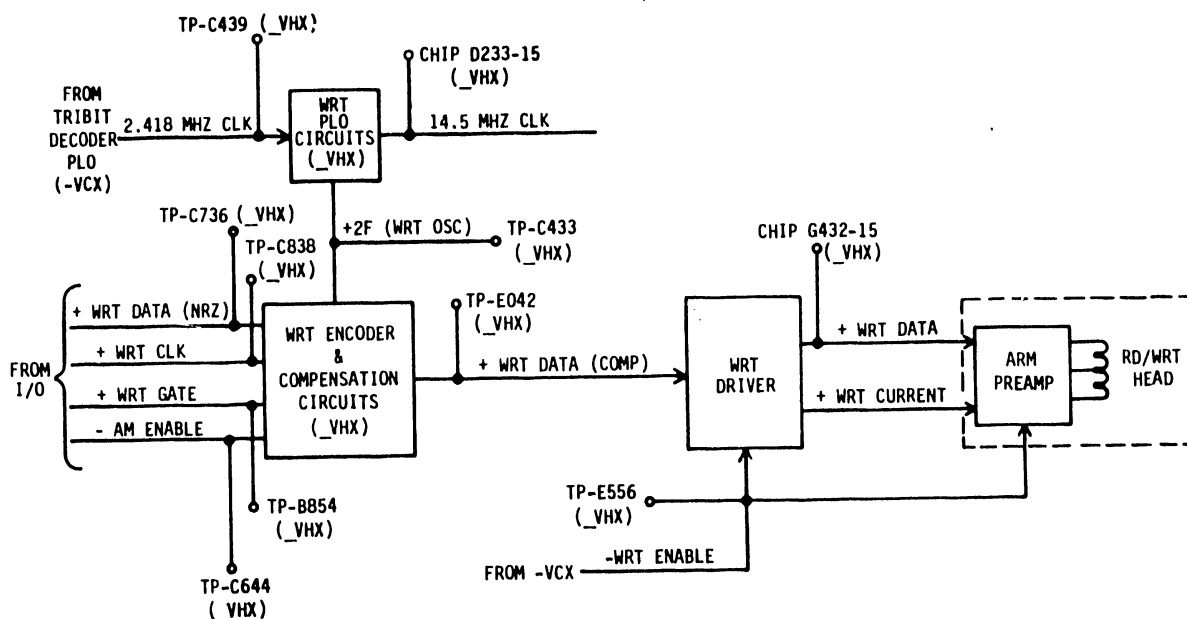
Figure 4-13.   Write Circuits Test Points (515 MB)

CAUTION

Perform this procedure only during trouble-shooting when a write fault condition inter-feres with isolating the problem.

1.   Remove power from drive as follows:

a. Press START switch to stop motor and unload heads.

b. Set CB1 to off.

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can re-sult in loss of customer data.

2.   Connect jumper wire between TP-C642 (Write Fault) and TP-A244 (ground) on _VHX board.

3.   Power up drive and perform tests. Monitor TP-J81-12 (Fault) on __SYX/__TQX board to determine if write fault condition persists. When testing is complete, remove jumper wire.

4306 - WRITE PLO CHECK (515 MB)

This procedure checks the operation of the write PLO. The PLO provides timing signals used, during write operations by both the drive and controller.

1. Connect oscilloscope and observe that 2.418 MHz Clock frequency is approximately as shown on figure 4-14.

2. Connect oscilloscope and observe that 14.5 MHz Clock frequency is approximately as shown on figure 4-15.

3. Connect oscilloscope and observe that 2F Write Oscillator timing is approximately 29.01 MHz (see figure 4-16).

4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C439 ON _VHX	2.418 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 µS/CM   MODE:

NOTES:
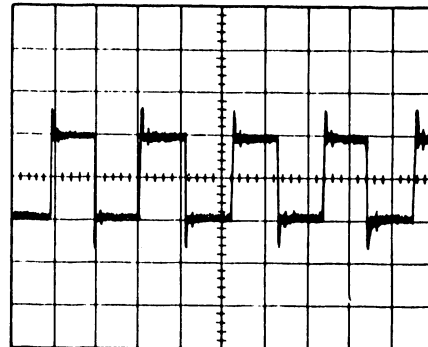
11D138 A

Figure 4-14.   2.418 MHz Clock Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D233-15 ON _VHX	+ 14.5 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM   MODE:

NOTES:
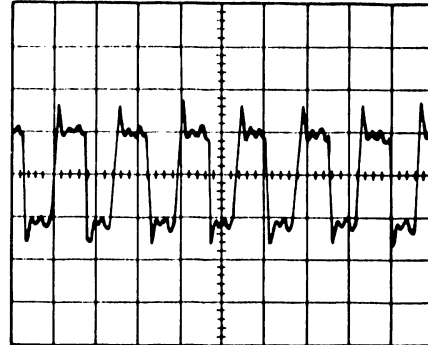
11D139A

Figure 4-15.   14.5 MHz Servo Clock Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT.

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C433 ON _VHX	+ 2F (WRT OSC)
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.02 µS/CM   MODE:

NOTES:
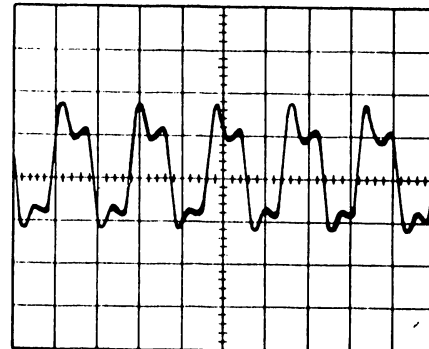
11D140 A

Figure 4-16.   2F Write Oscillator Timing (515 MB)

4307 - WRITE DATA CHECK (515 MB)

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-13). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding to perform a write operation.

CAUTION

> To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head.

2. Command drive to write a 1010... pattern.

3. Connect oscilloscope and observe that Write Gate and Write Enable appear as shown on figure 4-17.

4. Check inputs to write encoder and compensation circuits. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.

   a. Connect oscilloscope as shown on figure 4-18 and observe that Write Clock frequency is approximately 14.5 MHz.

   b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-18. Write Clock should go positive at approximately the center of the data "1" pulses.

5. Check write data (compensated) control circuits as follows:

   a. Connect oscilloscope as shown on figure 4-19.

   b. Observe that timing relationship between write data (compensated) and 2F (write oscillator) is similar to that on figure 4-19.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B854 ON _VHX	+ WRT GATE
CH 2	2.0 V/CM	TP-E556 ON _VHX	- WRT ENABLE

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 MS/CM   MODE: ALT

NOTES:
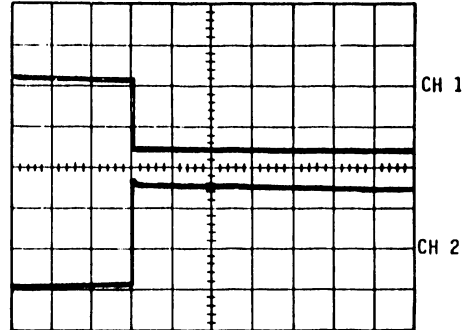
11D141A

Figure 4-17.   Write Gate Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C736 ON _VHX	+ WRT DATA (NRZ)
CH 2	0.5 V/CM	TP-C838 ON _VHX	+ WRT CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	TP-E556 ON _VHX	-WRT ENABLE

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:
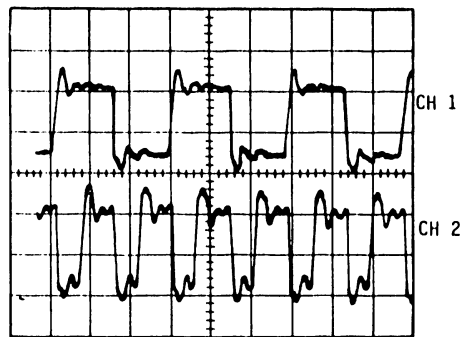
1. DISREGARD ANY GHOST IMAGES.

11D142B

Figure 4-18.   Write Data to Clock Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E042 ON _VHX	+ WRT DATA COMP
CH 2	0.5 V/CM	TP-C433 ON _VHX	+ 2F (WRT OSC)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM   MODE: ALT

NOTES:

CH 1

CH 2
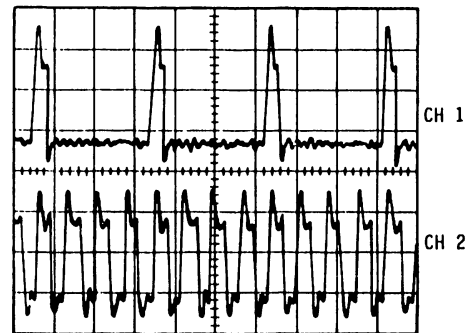
11D143A

Figure 4-19.   Compensated Write Data Timing (515 MB)

6.   Check output of write driver circuit as follows:

   a. Move oscilloscope channel 2 probe to Chip G432, pin 15 on __VHX board or TP-G437 on __SUX board (see figure 4-20).

   b. Observe that signals are approximately as shown on figure 4-20.

7.   Proceed to next test or return drive to online operation.

4307 - WRITE ADDRESS MARK CHECK (515 MB)

This procedure verifies that the drive is not writing during the time that Address Mark Enable is active.

CAUTION

To avoid possible loss of customer data, se-
lect a cylinder and head that will result in
data being written on an unused track.

1.   Command continuous write format with address mark opera-
tions using a 1010... data pattern.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-E042 ON _VHX	+ WRT DATA (COMP)
CH 2	0.5 V/CM	CHIP G432-15 ON _VHX	+ WRT DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: .05 µS/CM   MODE: ALT
NOTES:

    1. DISREGARD ANY GHOST IMAGES.

11D144 B
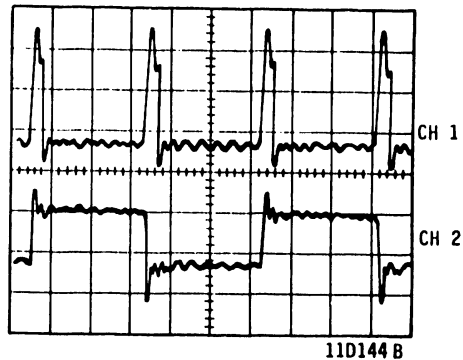
Figure 4-20.   Write Driver Output (515 MB)

2.   Connect oscilloscope as shown on figure 4-21.

3.   Observe that there are no data "1" pulses during the time that Address Mark Enable is active.

4.   Proceed to next test or return drive to online operation.

READ CHECKS (340 MB)

The following procedures, 4401 through 4403, check various aspects of drive read circuit operation. Figure 4-22 is a block diagram showing the major components in the read circuits and the test points used in the procedures.

4401 - READ PLO CHECK (340 MB)

This procedure checks the operation of the read PLO circuits (see figure 4-22). The read PLO provides timing signals used during read operations.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON _VHX	- AM ENABLE
CH 2	0.5 V/CM	TP-E042 ON _VHX	+ WRT DATA (COMP)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM   MODE: ALT

NOTES:

11D145A
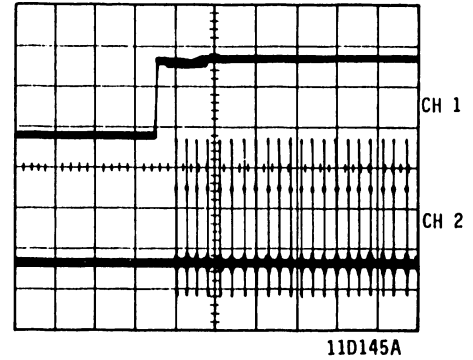
Figure 4-21.   Write Address Mark Timing (515 MB)

11D158
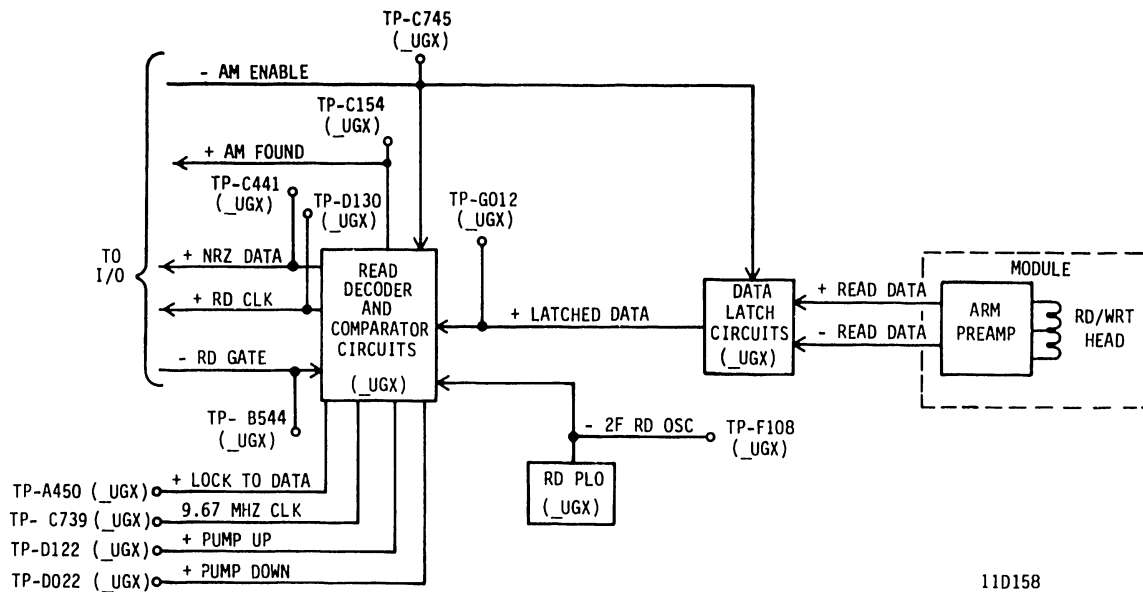
Figure 4-22.   Read Circuits Test Points (340 MB)

1. Connect oscilloscope as shown on figure 4-23 and observe that 2F Read Oscillator frequency is approximately 19.34 MHz.

2. Connect oscilloscope as shown on figure 4-24 and observe that the +Pump Up and +Pump Down signals are coincident.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to write a 1010... pattern using any head.

4. Command drive to perform continuous read operations.

5. Observe that +Pump Up and +Pump Down signals have the same timing relationship shown on figure 4-25.

6. Proceed to next test or return drive to online operation.

4402 - READ DATA CHECK (340 MB)

This procedure checks the operation of the data latch, read comparator, and MFM decoder circuits.

1. Perform Write Data Check (proc 4303).

2. Perform Read PLO Check (proc 4401).

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.

4. Command drive to write a 1010... pattern and then to perform continuous read operations.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-F108 _UGX	- 2F RD OSC
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE:

NOTES:
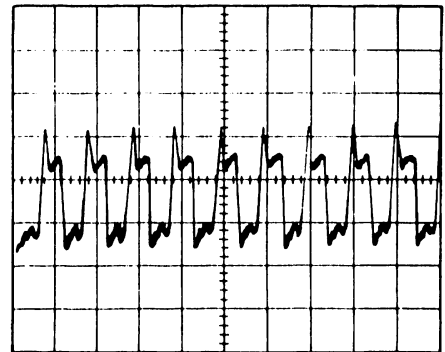
11D130

Figure 4-23.   2F Read Oscillator Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-D122 ON _UGX	+ PUMP UP
CH 2	0.5 V/CM	TP-D022 ON _UGX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

1. MEASUREMENT IS ONLY VALID IF DRIVE IS NOT READING.

2. OBSERVE THAT CH 1 AND CH 2 SIGNALS ARE COINCIDENT.

CH 1

CH 2
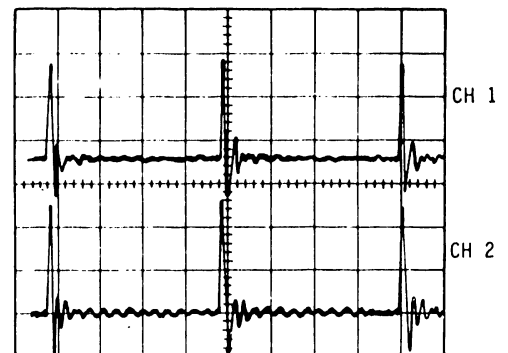
11D131

Figure 4-24.   Pump Up/Down Timing (Not Reading, 340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON _UGX	+ PUMP UP
CH 2	0.5 V/CM	TP-DO22 ON _UGX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:
  1. DISREGARD ANY GHOST IMAGES.
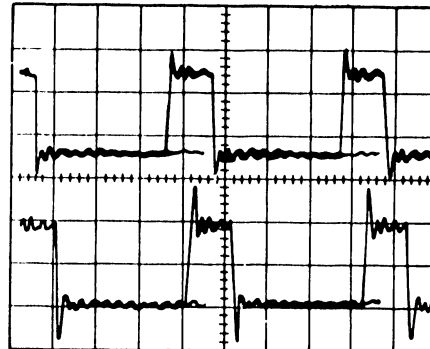
11D132

Figure 4-25.   Pump Up/Down Timing (Reading, 340 MB)

5. Check the Latched Read Data signal and its timing relationship with the 2F Read oscillator signal.

   a. Connect oscilloscope as shown on figure 4-26 and observe that Latched Read Data pulse width is as shown.

   b. Observe that Latched Read Data pulses are approximately coincident with 2F Read Oscillator pulses.

   c. Observe that the data pattern is correct.

6. Check Read Data to Read Clock Timing.

   a. Connect oscilloscope as shown on figure 4-27 and observe that Read Clock frequency is approximately 9.67 MHz.

   b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.

   c. Observe that the NRZ data has a 1010... pattern.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-G012 ON _UGX	+ LATCHED READ DATA
CH 2	0.5 V/CM	TP-F108 ON _UGX	- 2F READ OSC

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

APPROXIMATELY 20 NS

CH 1

CH 2

11D133A
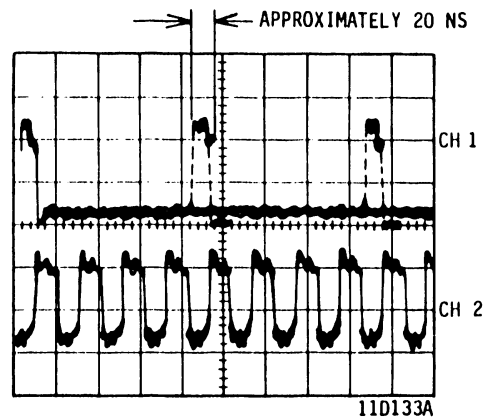
Figure 4-26.   Latched Read Data Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C441 ON (_UGX)	+ NRZ READ DATA
CH 2	0.5 V/CM	TP-D130 ON (_UGX)	+ READ CLOCK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

103 ±10 NS

CH 1

CH 2

103 ±10 NS   51.6 ±4 NS

11D134
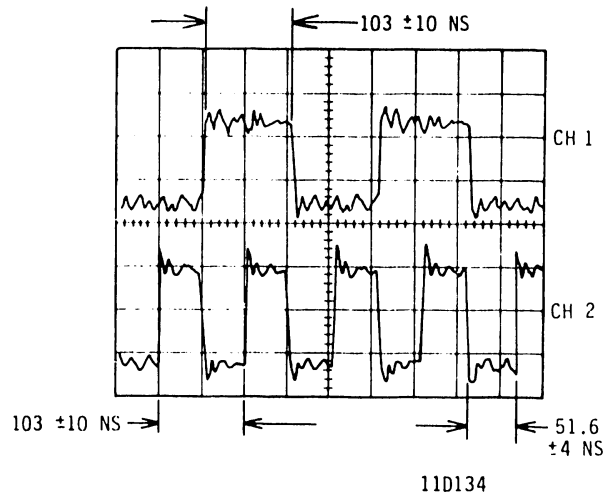
Figure 4-27.   NRZ Read Data Timing (340 MB)

7. Check Read Gate to Lock to Data timing.

    a. Connect oscilloscope as shown on figure 4-28.

    b. Observe that +Lock to Data goes low at the proper time (see figure 4-28).

8. Proceed to next test or return drive to online operation.

4403 - READ ADDRESS MARK CHECK (340 MB)

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, select a head and cylinder that will result in data being written on an unused track.

1. Command a write format in address mark mode using a 1010.. pattern. Then command a continuous read address mark operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B544 ON _UGX	- READ GATE
CH 2	2.0 V/CM	TP-A450 ON _UGX	+LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 µS/CM   MODE: ALT

NOTES:

CH 1

CH 2
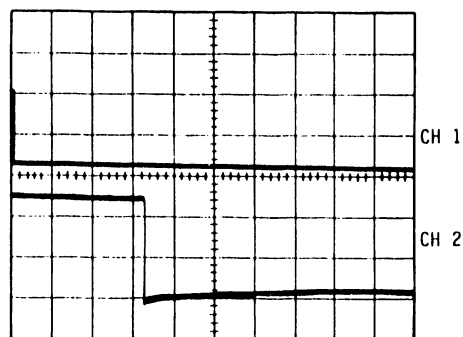
11D126A

Figure 4-28.   Read Gate to Lock to Data Timing (340 MB)

83324770 B

2. Connect oscilloscope as shown on figure 4-29.

NOTE

In "A Intensified" horizontal mode, the brightened marker highlights the segment of the sweep that is displayed later in "B Delayed" horizontal mode.

3. Adjust DELAY TIME MULTIPLIER on oscilloscope to move intensified marker into data pattern (see figure 4-29). To minimize display instability, use first address mark area following index.

4. Referring to figure 4-30 position oscilloscope HORIZ DISPLAY switch to B DELAYED and TRIGGERING to +EXT CH I.

5. Check that the length of the address mark area is within the limits shown on figure 4-30. If it is outside these limits the address mark detection circuits may not function properly.

6. Observe that Address Mark Found goes active immediately following the address mark area.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-F912 ON _UGX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _UGX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT CH 1	TP-J81-2 ON _SYX/_TQX	+ INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM   MODE: ALT

B TIME/ DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "A" INTENSIFIED AND ADJUST DELAY TIME MULTIPLIER TO MOVE MARKER TO ADDRESS MARK.

INTENSIFIED MARKER

CH 1

CH 2

11D127

Figure 4-29.   Scope Setup for AM Found Timing (340 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-F912 ON _UGX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _UGX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT CH 1	TP-J81-2 ON _SYX/_TQX	+INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM   MODE:
B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "B" (DELAYED) AND ADJUST DELAY MULTIPLIER AS REQUIRED.

11D135

Figure 4-30. AM Found Timing (340 MB)

7. Connect oscilloscope as shown on figure 4-31.

8. Observe that +Lock to Data goes active at the proper time (see figure 4-31).

9. Proceed to next test or return drive to online operation.

READ CHECKS (515 MB)

The following procedures, 4404 through 4406, check various aspects of drive read circuit operation. Figure 4-32 is a block diagram showing the major components in the read circuits and the test points used in the procedures. All references to the _VHX read/write board apply also the the _SUX read/write board (used on older drives).

4404 - READ PLO CHECK (515 MB)

This procedure checks the operation of the read PLO circuits (see figure 4-32). The read PLO provides timing signals used during read operations.

1. Connect oscilloscope as shown on figure 4-33 and observe that 2F Read Oscillator frequency is approximately 29.01 MHz.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C745 ON _UGX	- AM ENABLE
CH 2	2.0 V/CM	TP-A450 ON _UGX	+ LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 μS/CM   MODE: ALT

NOTES:

11D136
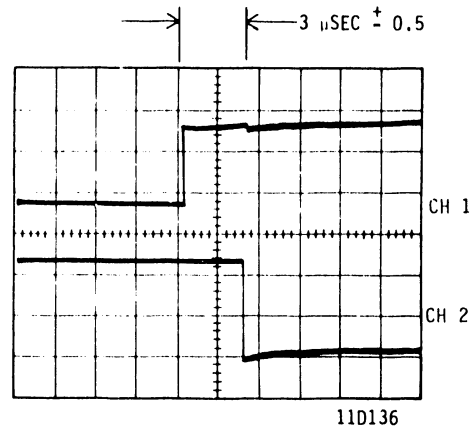
Figure 4-31.   AM to Lock To Data Timing (340 MB)

11D159A
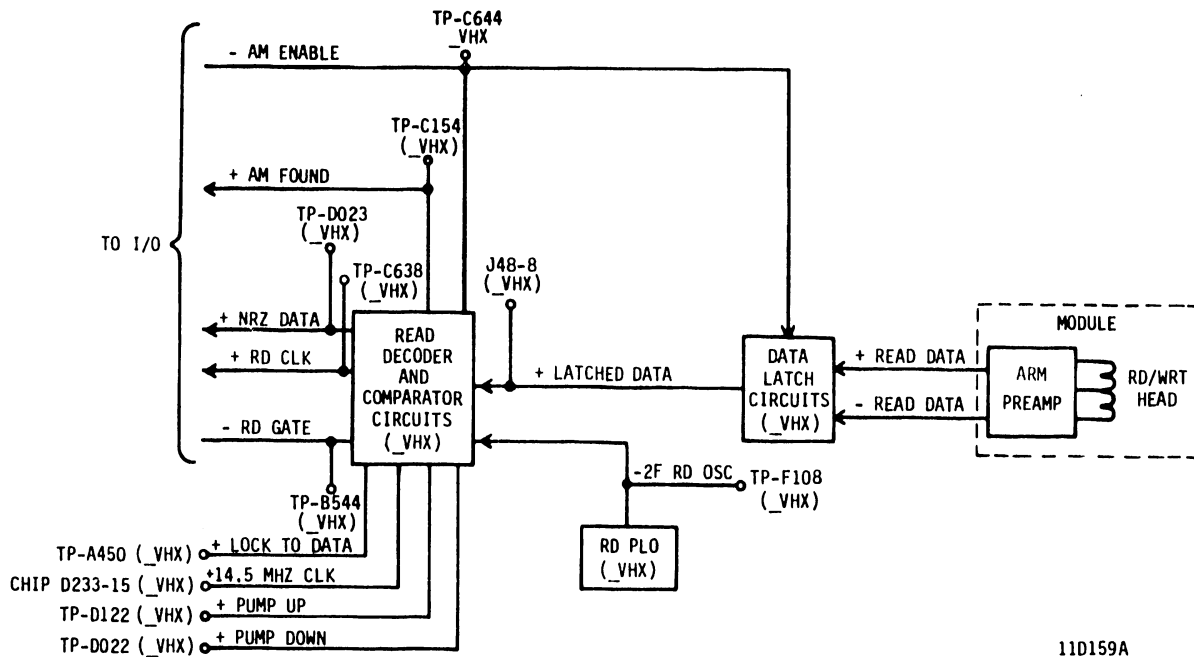
Figure 4-32.   Read Circuits Test Points (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH I	0.5 V/CM	TP-F108 ON _VHX	- 2F RD OSC
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 NS/CM   MODE:

NOTES:
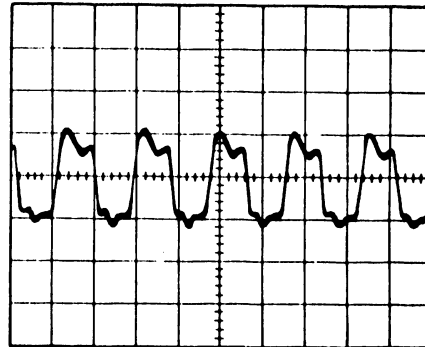
11D146A

Figure 4-33.   2F Read Oscillator Timing (515 MB)

2.   Connect oscilloscope as shown on figure 4-34 and observe that the +Pump Up and +Pump Down signals are coincident.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3.   Command drive to write a 1010... pattern using any head.

4.   Command drive to perform continuous read operations.

5.   Observe that +Pump Up and +Pump Down signals have the same timing relationship shown on figure 4-35.

6.   Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON _VHX	+ PUMP UP
CH 2	0.5 V/CM	TP-D022 ON _VHX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

1. MEASUREMENT IS ONLY VALID IF DRIVE IS NOT READING.
2. OBSERVE THAT CH 1 AND CH 2 SIGNALS ARE COINCIDENT.

11D147 A

Figure 4-34.   Pump Up/Down Timing (Not Reading, 515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON _VHX	+ PUMP UP
CH 2	0.5 V/CM	TP-D022 ON _VHX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

11D148 A
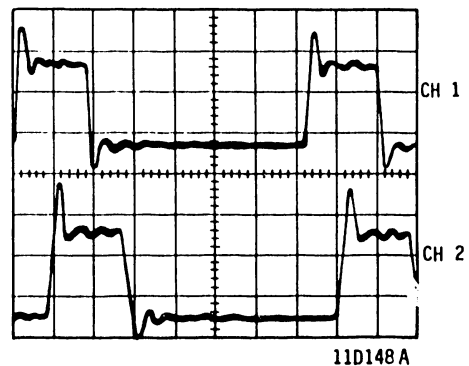
Figure 4-35.   Pump Up/Down Timing (Reading, 515 MB)

4405 - READ DATA CHECK (515 MB)

This procedure checks the operation of the data latch, read comparator, and 2-7 decoder circuits.

1. Perform Write Data Check (proc 4303).

2. Perform Read PLO Check (proc 4401).

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.

4. Command drive to write a 1010... pattern and then to perform continuous read operations.

5. Check the Latched Read Data signal and its timing relationship with the 2F Read oscillator signal.

   a. Connect oscilloscope as shown on 4-36 and observe that Latched Read Data pulse width is as shown.

   b. Observe that Latched Read Data pulses and 2F Read Oscillator pulses have the approximate phase relationship shown in figure 4-36.

   c. Observe that the data pattern is correct.

6. Check Read Data to Read Clock Timing.

   a. Connect oscilloscope as shown on figure 4-37 and observe that Read Clock frequency is approximately 14.5 MHz.

   b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.

   c. Observe that the NRZ data has a 1010... pattern.

7. Check Read Gate to Lock to Data timing.

   a. Connect oscilloscope as shown on figure 4-38.

   b. Observe that +Lock to Data goes low at the proper time (see figure 4-38).

8. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-08 ON _VHX	+ LATCHED READ DATA
CH 2	0.5 V/CM	TP-F108 ON _VHX	- 2F READ OSC

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 2		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 NS/CM   MODE: ALT

NOTES:

    1. DISREGARD ANY GHOST IMAGES.

11D149B
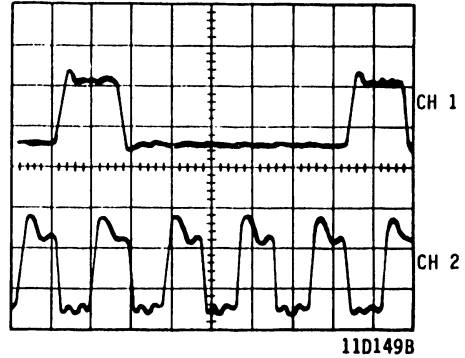
Figure 4-36.   Latched Read Data Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D023 ON _VHX	+ NRZ READ DATA
CH 2	0.5 V/CM	TP-C638 ON _VHX	+ READ CLOCK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM   MODE: ALT

NOTES:

11D150A
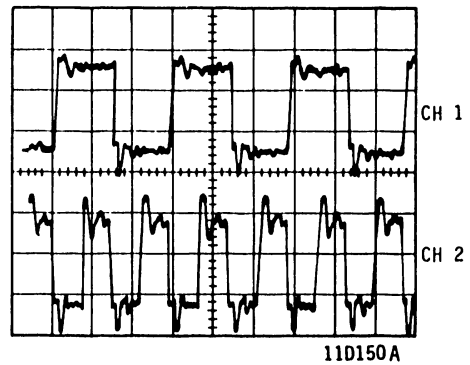
Figure 4-37.   NRZ Read Data Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B544 ON _VHX	- READ GATE
CH 2	2.0 V/CM	TP-A450 ON _VHX	+ LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 µS/CM   MODE: ALT
NOTES:
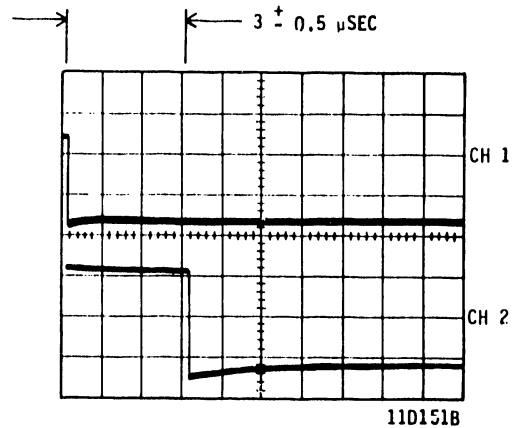
Figure 4-38.   Read Gate to Lock to Data Timing (515 MB)

4406 - READ ADDRESS MARK CHECK (515 MB)

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, se-
lect a head and cylinder that will result in
data being written on an unused track.

1. Command a write format in address mark mode using a
    1010.. pattern. Then command a continuous read address
    mark operation.

2. Connect oscilloscope as shown on figure 4-39.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-8 ON _VHX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _VHX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT CH 1	TP-J81-2 ON _SYX/_TQX	+ INDEX

SCOPE GND TO GND CN LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM   MODE:

B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "A" INTENSIFIED AND
   ADJUST DELAY TIME MULTIPLIER TO MOVE MARKER TO
   ADDRESS MARK.

Figure 4-39.   Scope Setup for AM Found Timing (515 MB)

NOTE

In "A Intensified" horizontal mode, the
brightened marker highlights the segment cf
the sweep that is displayed later in "B Delay-
ed" horizontal mode.

3. Adjust DELAY TIME MULTIPLIER on oscilloscope to move in-
    tensified marker into data pattern (see figure 4-39). To
    minimize display instability, use first address mark area
    following index.

4. Referring to figure 4-40 position oscilloscope HORIZ DIS-
    PLAY switch to B DELAYED and TRIGGERING to +EXT CH I.

5. Check that the length of the address mark area is within
    the limits shown on figure 4-40. If it is outside these
    limits the address mark detection circuits may not
    function properly.

6. Observe that Address Mark Found goes active immediately
    following the address mark area.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-8 ON _VHX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _VHX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT	TP-J80-6 ON _VCX	+ INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM   MODE: ALT

B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "B" (DELAYED) AND ADJUST
   DELAY MULTIPLIER AS REQUIRED.

11D320
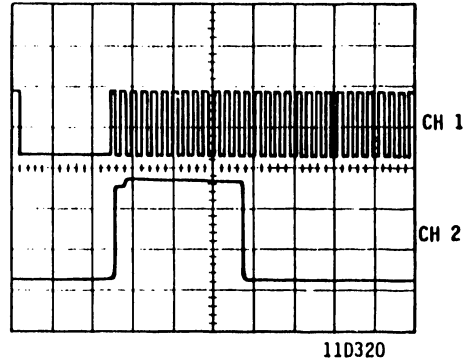
Figure 4-40. AM Found Timing (515 MB)

7. Connect oscilloscope as shown on figure 4-41.

8. Observe that +Lock to Data goes active at the proper time
    (see figure 4-41).

9. Proceed to next test or return drive to online operation.

MISCELLANEOUS LOGIC CHECKS

4501 - INDEX CHECK

This procedure checks that Index is present and has the proper
pulse width. It also checks the time between successive Index
pulses which is an indication of disk rotational speed.

1. Connect oscilloscope as shown on figure 4-42.

2. Observe that the Index pulse width is between 2.2 and 2.8
    microseconds.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON _VHX	- AM ENABLE
CH 2	2.0 V/CM	TP-A450 ON _VHX	+ LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XlO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 µS/CM   **MODE:** ALT

NOTES:

3 ± 0.5 µSEC

CH 1

CH 2

11D154B
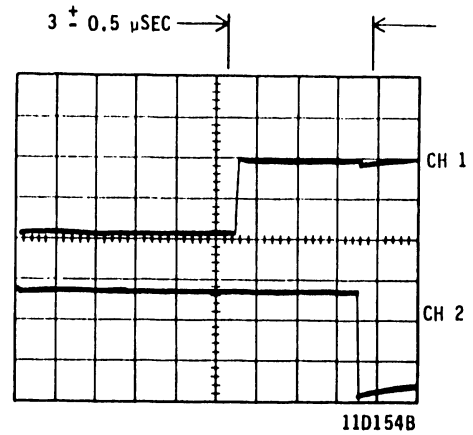
Figure 4-41.   AM to Lock To Data Timing (515 MB)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J81-2 ON _SYX/_TQX	+ INDEX
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XlO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM   **MODE:**

NOTES:

11D155
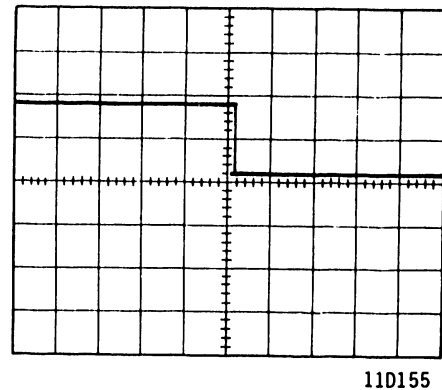
Figure 4-42.   Index Pulse Timing

3. Connect oscilloscope as shown on figure 4-43.

4. Observe that the time between Index pulses is between 16.5 and 16.8 milliseconds.

5. Proceed to next test or return drive to online operation.

4502 - SECTOR CHECK

This procedure checks for the presence of sector pulses and that they have the proper width.

1. Connect oscilloscope as shown on figure 4-44.

2. Observe that the Sector pulse width is between 1.05 and 1.45 microseconds.

3. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J81-2 ON _SYX/_TQX	+ INDEX
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 MS/CM   MODE:

NOTES:
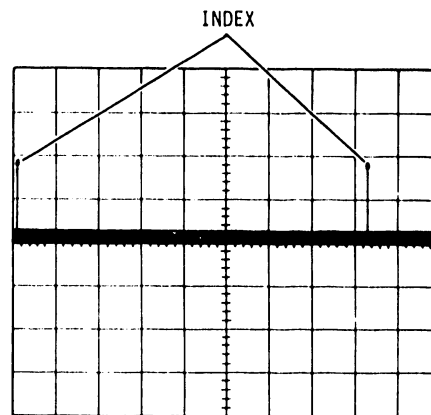
INDEX

11D156

Figure 4-43. Index to Index Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J80-5 ON _VCX	+ SECTOR
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM   **MODE:**
NOTES:
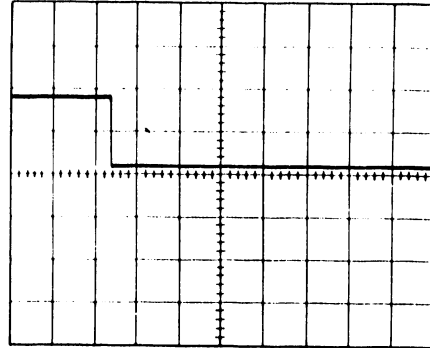
11D157

Figure 4-44.   Sector Pulse Timing

SECTION
5
REPAIR
AND
REPLACE-
MENT

5. REPAIR AND REPLACEMENT

CAUTION

When servicing the drive, observe all precau-
tions listed under Electrostatic Discharge
Protection in section 2 of this manual. Fail-
ure to observe these precautions can result in
serious damage to electronic assemblies.

INTRODUCTION

Repair of the drive is limited to replacement of defective
parts and assemblies. This section describes removal and re-
placement and, where applicable, adjustment of all major field
replaceable parts and assemblies. The information here should
be used in conjunction with that in the parts data section of
Hardware Maintenance Volume 1.

If adjustments are required as a result of replacing a part, it
is specified in the replacement procedure. If an adjustment is
included, and there is some doubt as to the need for replace-
ment, perform the adjustment prior to replacing the part.

The procedures in this section assume that the drive is mounted
on slides in an equipment rack or cabinet. But unless other-
wise specified, it is not necessary to remove the drive from
the slides to perform maintenance. All procedures require that
power be removed from the drive and power supply. The person
performing the maintenance should be thoroughly familiar with
the operation of the drive and with all information in the gen-
eral maintenance section of this manual (particularly warnings
and precautions).

Each procedure is assigned a unique number. The numbers are
used elsewhere in the manual to reference the procedures. The
procedures and numbers are organized into three categories:
51XX - mechanical, 52XX - electromechanical, and 53XX - elec-
tronic (circuit boards).

- 5101 – Entire Drive Removal & Replacement
- 5102 – Top Cover Removal & Replacement
- 5103 – Front Panel Removal & Replacement
- 5104 – Slide Removal & Replacement
- 5201 – Fan Removal & Replacement
- 5202 – Operator Panel (_PBX) Removal & Replacement
- 5203 – Fault Display (_UQX) Removal & Replacement
- 5204 – Brake Removal, Replacement & Adjustment
- 5205 – Power Supply Removal & Replacement
- 5206 – Locking Solenoid Coil Removal & Replacement
- 5207 – Module Removal & Replacement
- 5208 – Shipping Damper Adjustment
- 5209 – Cable Replacement
- 5210 – Motor Assembly Removal & Replacement
- 5301 – _UGX/_VHX Board Removal & Replacement
- 5302 – _SYX/_TQX Board Removal & Replacement
- 5303 – _VCX Board Removal & Replacement
- 5304 – _SWX Board Removal & Replacement
- 5305 – _SVX Board Removal & Replacement

5101 - ENTIRE DRIVE REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the entire drive and assumes that the drive is mounted on slides in an equipment rack. If the drive is to be replaced with another and the inner slides are required for the replacement unit, see procedure 5104 – Slide Removal & Replacement. Two persons may be required to lift the drive on and off the slide assemblies.

REMOVAL

NOTE

For drives with remote power supply mounted on slides (rear of drive), perform step 1 and skip to step 5. For drives with integral power supply, begin with step 2.

1. Perform power supply removal procedure (5205).

2. Lift cabinet latch and pull drive to fully extended position.

3. Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for Ready indicator to stop flashing then set CB1 to OFF.

4. Disconnect ac power cable from AC INPUT connector J1 on power supply.

5. Disconnect I/O cables and terminators from drive.

6. Press slide lock release and pull drive forward until it is free of slide assemblies.

7. Move drive to desired location.

REPLACEMENT

1. Going to the equipment rack, push intermediate slides to fully retracted positions inside outer slides.

2. Lift drive into position in front of rack and guide inner slides into intermediate slides. Push until lock releases engage, then pull drive to fully extended position.

3. Connect I/O cables to drive connectors. See Hardware Maintenance Manual Volume 1 for desired system cabling.

NOTE

For drives with remote power supply, perform step 4. For drives with integral power supply, perform step 5.

4. Perform power supply replacement procedure (5205).

5. Connect AC input connector to J1 on power supply.

5102 - TOP COVER REMOVAL & REPLACEMENT

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Extend drive to fully extended position.

2. Remove power from drive as follows:

    a. Press START switch to release it from start position.

    b. Wait for Ready indicator to stop flashing, then set CB1 to OFF.

3. Loosen screws securing bottom edge of cover to drive.

CAUTION

Cover must be carefully lifted from the center to avoid possible damage to adjacent components.

4. Lift off cover.

REPLACEMENT

CAUTION

When replacing cover, use care to avoid damaging logic boards.

1. Place cover on drive.

2. Tighten screws to secure cover to drive.

3. Push drive back to closed position in rack.

83324770 B

5103 - FRONT PANEL REMOVAL & REPLACEMENT

REMOVAL

1. Remove power from drive as follows:

   a. Press START switch tc release it from start position.

   b. Wait for Ready indicator to stop flashing, then set CB1 to OFF.

2. Remove front panel insert (see figure 5-1) by pulling forward to disengage catches that hold the insert in the front panel.

3. Remove primary filter.

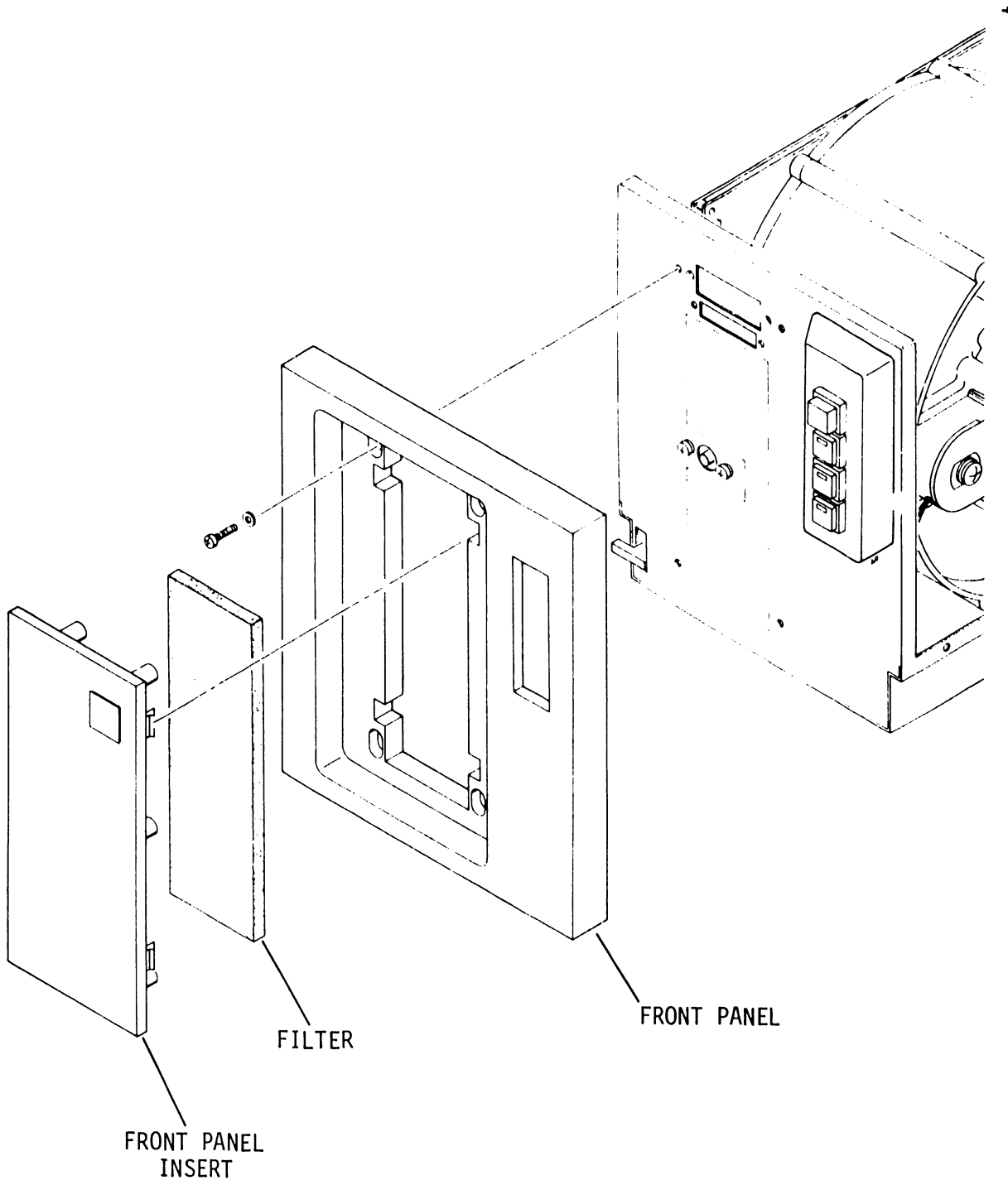4. Remove screws securing front panel to drive and lift panel off drive.

REPLACEMENT

1. Put front panel in place (centered over switches), insert screws, and fasten securely (see figure 5-1).

2. Install primary filter.

3. Replace front panel insert by aligning catches to slots in front panel and pushing on insert until catches snap into place.

5104 - SLIDE REMOVAL & REPLACEMENT

The following procedure describes how to remove and replace the inner slide assemblies. This procedure is used to replace a defective inner slide or if the inner slides must be removed from one drive and installed on another.
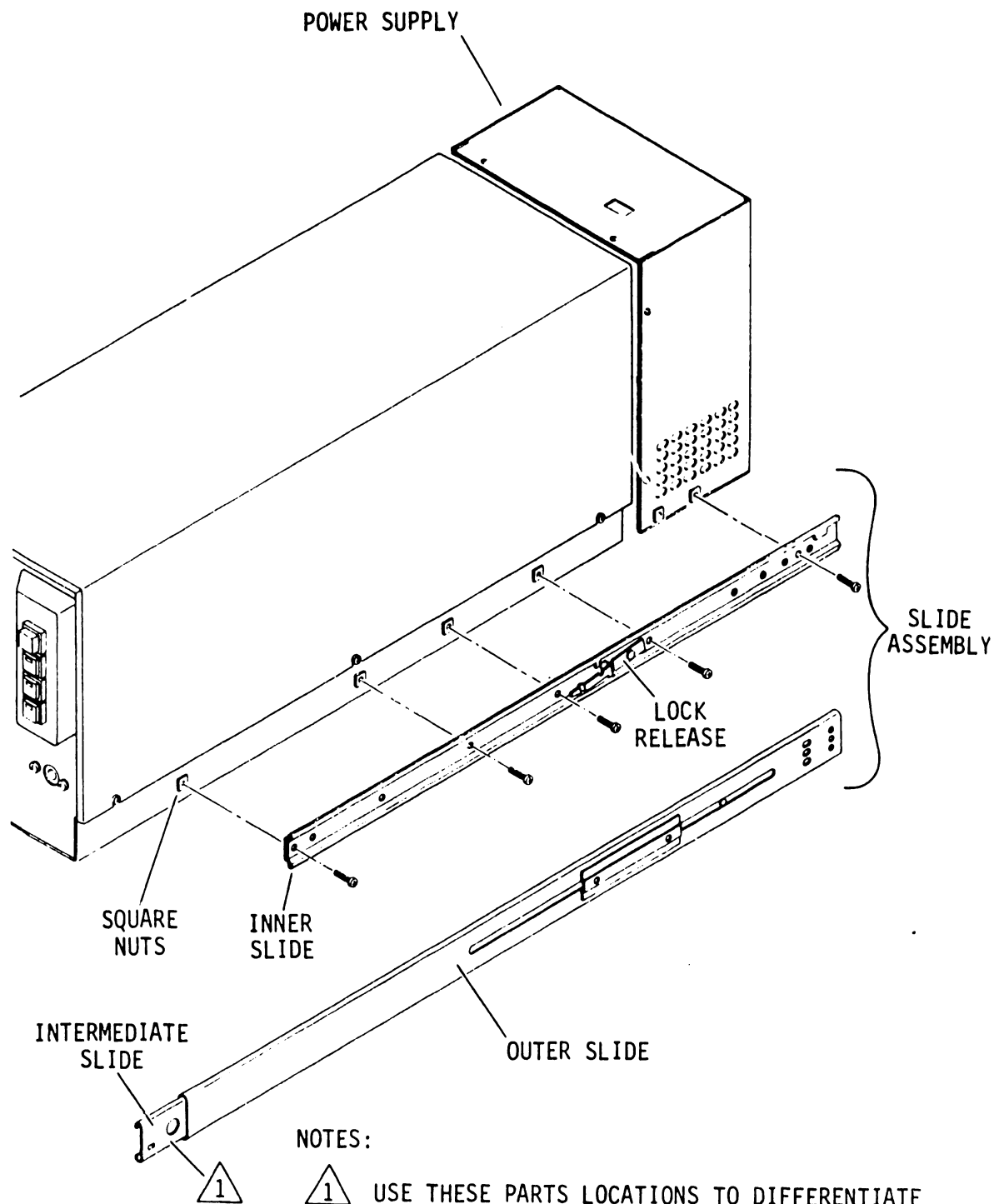
REMOVAL

1. Perform entire drive removal procedure (5101).

2. For drives with remote power supply mounted on slides (rear of drive), remove power supply mounts by removing attaching hardware (see figure 5-8).

3. Remove screws securing slides to drive and remove slides (see figure 5-2).

FRONT PANEL

FILTER

FRONT PANEL
INSERT

11D161

Figure 5-1. Front Panel Removal and Replacement

83324770 B

POWER SUPPLY

SLIDE ASSEMBLY

LOCK RELEASE

SQUARE NUTS

INNER SLIDE

INTERMEDIATE SLIDE

OUTER SLIDE

NOTES:

⚠1

⚠1 USE THESE PARTS LOCATIONS TO DIFFERENTIATE BETWEEN RIGHT-HAND AND LEFT-HAND SLIDES.

11D162A

Figure 5-2. Slide Removal and Replacement

REPLACEMENT

1. Mount inner slides on drive by installing screws through holes in inner slides into square nuts in drive. Figure 5-2 defines which slide component is used on the right-hand side of the drive.

2. Install remote power supply mounts with attaching hardware (see figure 5-8).

3. Perform entire drive replacement procedure (5101).

5201 - FAN REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove power supply as follows:

   a. For drives with integral power supply, perform power supply removal procedure (5205).

   b. For drives with remote power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to allow access to fan hardware.

3. Disconnect P38 from mother board (see figure 5-3).

4. Remove screws securing outer finger guard and fan to drive. Remove guard and fan.

5. Remove screws attaching inner finger guard to fan. Remove guard.

REPLACEMENT

1. Install inner finger guard on fan.

CAUTION

Installing fan backwards will result in improper airflow, which will cause overheating and premature component failure. Orient fans so P38 leads are on lower right when facing rear of drive (see figure 5-3).

2. Align fan to inside and finger guard to outside of rear panel. Attach and tighten securely with screws.
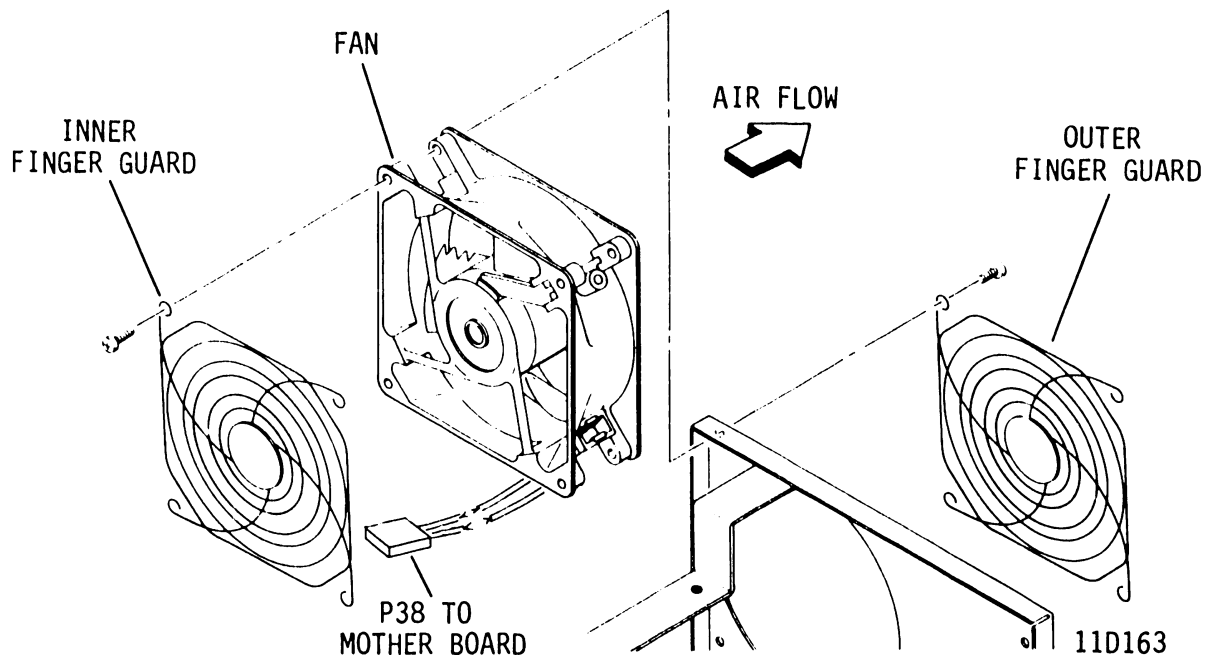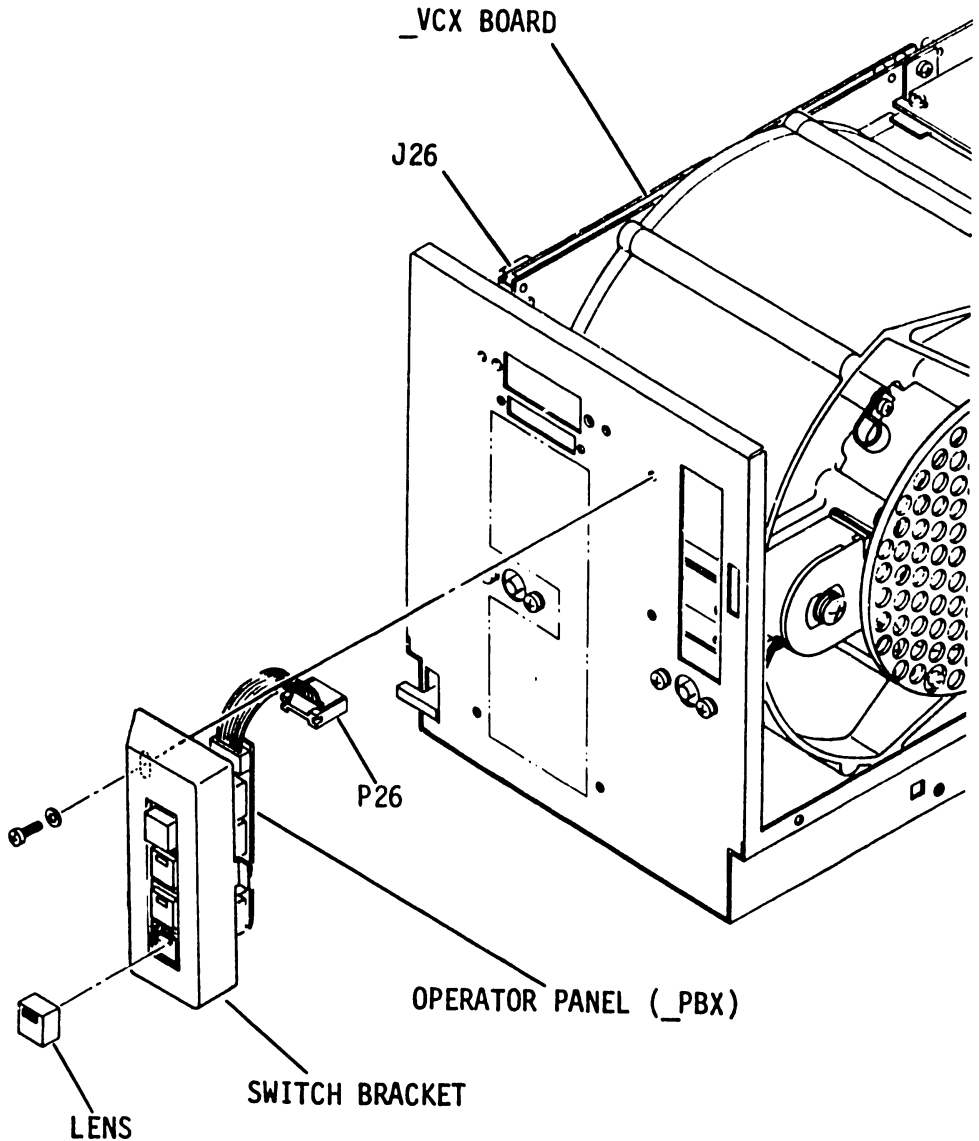
Figure 5-3. Fan Removal and Replacement

3. Connect P38 to J38 on mother board.

4. Replace power supply as follows:

 a. For drives with integral power supply, perform power supply replacement procedure (5205).

 b. For drives with remote power supply, move power supply into operating position. Install and tighten mounting screws.

5. Perform top cover replacement procedure (5102).

5202 - OPERATOR PANEL (—PBX) REMOVAL & REPLACEMENT

The operator panel (see figure 5-4) cannot be repaired and, except for the lenses, must be replaced as an assembly. The lenses can be replaced separately and are removed by carefully prying them from the switches (see figure 5-4). The following describes removal and replacement of the entire operator panel.

_VCX BOARD

J26

P26

OPERATOR PANEL (_PBX)

SWITCH BRACKET

LENS

11D345

Figure 5-4. Operator Panel Removal and Replacement

83324770 B

REMOVAL

1. Perform top cover and front panel removal procedures (proc 5102, 5103).

2. Disconnect P26 from J26 (on _VCX board) and remove cable from cable clips.

3. Remove screws securing switch bracket to chassis and re-move operator panel and bracket assembly from drive.

REPLACEMENT

1. Thread P26 and cable through hole in front panel.

2. Secure operator panel and bracket assembly to drive with screws.

3. Connect P26 to J26 on _VCX board and secure cable in ca-ble clips.

4. Perform front panel and top cover replacement procedures (proc 5102, 5103).

5203 - FAULT DISPLAY (—UQX) REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove front panel insert and filter (see figure 5-5).

3. Disconnect P13 from _VCX board.

4. Remove screws securing _UQX board to front panel bracket and remove board from drive.

REPLACEMENT

1. Position _UQX board to front panel bracket and secure into place with screws (see figure 5-5).
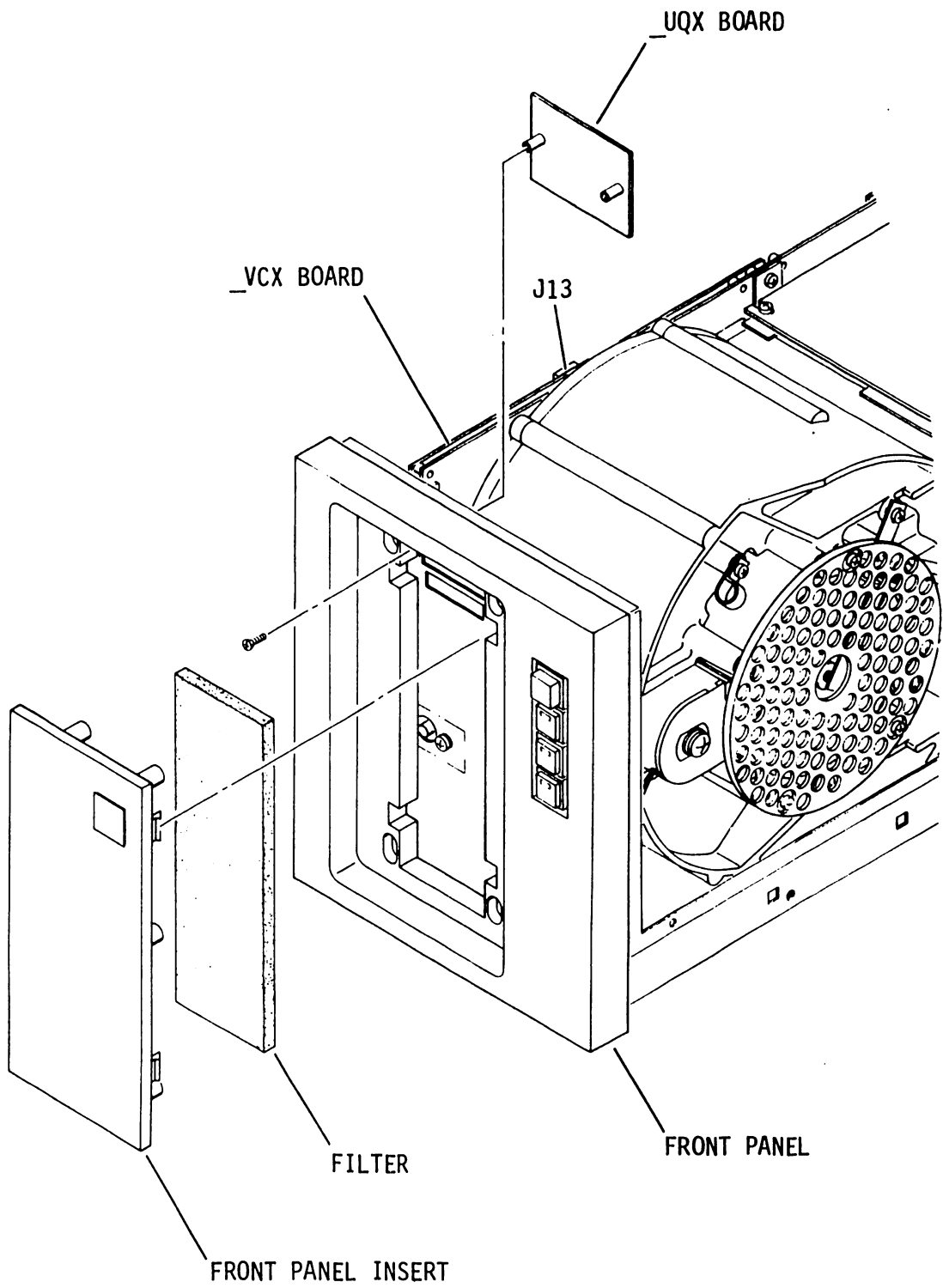
Figure 5-5.   Fault Display (_UQX) Removal & Replacement

11D165

2. Connect P13 to J13 on _VCX board.

3. Replace filter and front panel insert.

4. Perform top cover replacement procedure (5102).

5204 - BRAKE REMOVAL, REPLACEMENT & ADJUSTMENT

The brake (see figure 5-6) must be adjusted each time it is
replaced, as described in the adjustment procedure below. A
special brake adjustment shim (see table 2-1 for part number)
is required to adjust brake.

REMOVAL

1. Perform Top Cover Removal procedure (5102).

2. Remove screws attaching motor shield plate and move plate
   so that it will not interfere with brake removal.

MOTOR
SHIELD PLATE

P41

BRAKE

11D166A
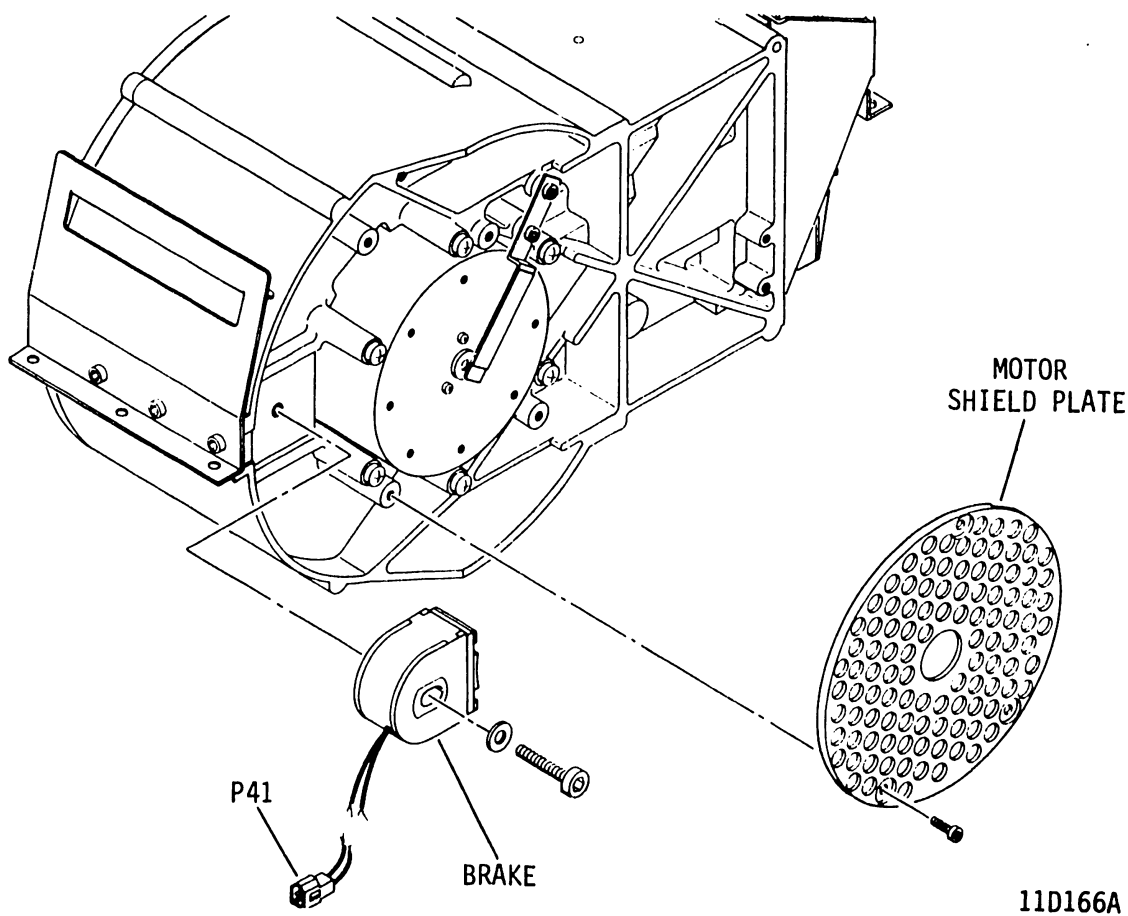
Figure 5-6.   Brake Removal and Replacement

3. Disconnect P41 on _SWX board and clip tie wraps securing cable to drive.

4. Remove screw attaching brake to module and lift off brake.

REPLACEMENT

1. Fit brake to bottom of module, align hole, and install but do not tighten screw.

2. Connect P41 to J41 on _SWX board.

3. Perform brake adjustment procedure starting with step 4.

ADJUSTMENT

1. Perform top cover removal procedure (5102).

2. Remove screws attaching motor shield plate and move plate so that it will not interfere with brake adjustment.

3. Loosen screw securing brake to bottom of module.

4. Insert brake adjustment shim between brake armature and housing (see figure 5-7).

NOTE

Heavy pressure may be required to make the adjustment in the following step.

5. Push brake against motor thus adjusting gap to thickness of shim.

6. Tighten screw to 5.3 N·m (46 lbf·in) and remove shim. Check adjustment.

7. Replace motor shield plate.

8. Reinstall all tie wraps at original locations.

9. Perform top cover replacement procedure (5102

5205 - POWER SUPPLY REMOVAL & REPLACEMENT

The following procedures provide instructions for removing and replacing the integral power supply, or remote power supply

ADJUSTMENT SHIM

0.007 TO 0.013 INCHES

MOTOR
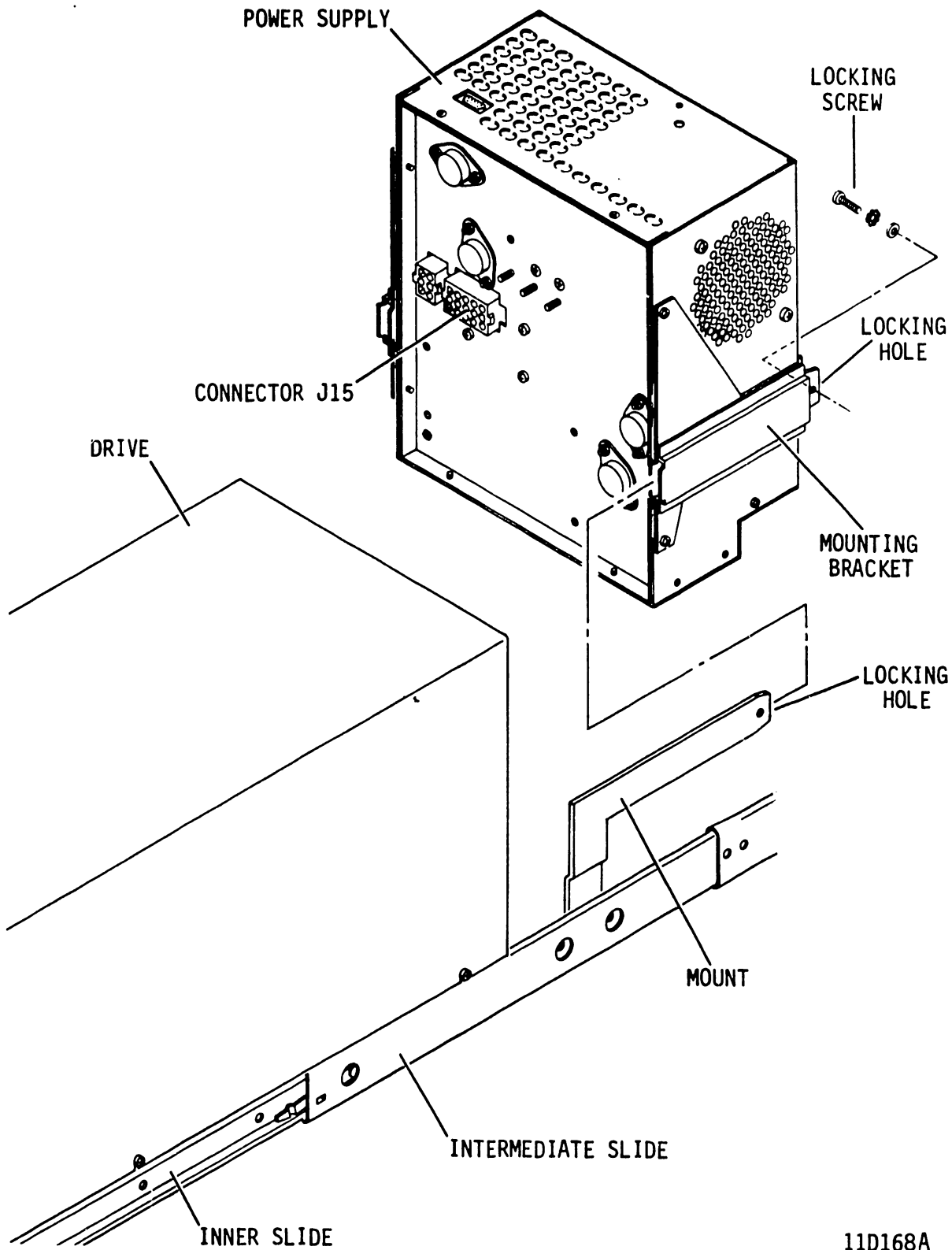
BRAKE HOUSING   BRAKE ARMATURE   BRAKE PAD
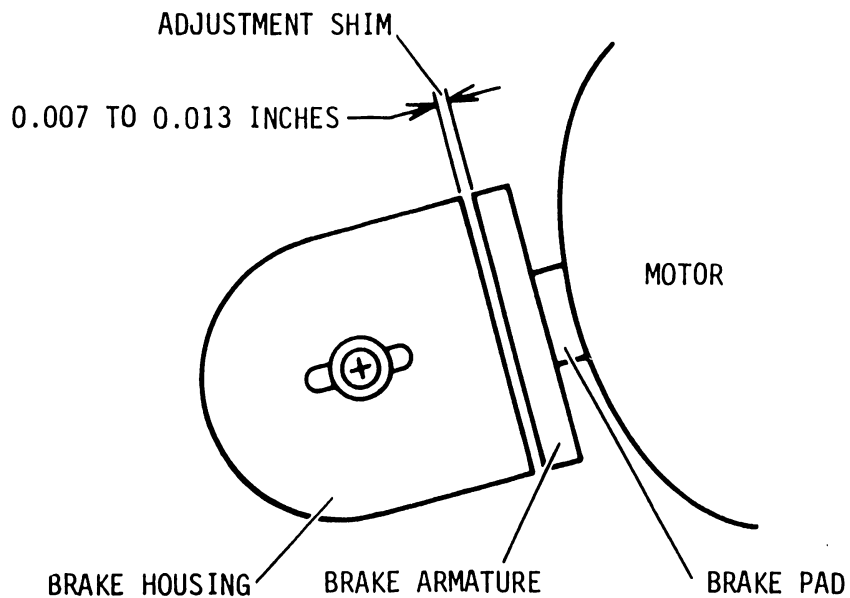
11D167

Figure 5-7.   Brake Adjustment

when it is slide mounted behind the drive (see figure 5-8).   A second person may be needed to support the supply while the mounting hardware is being removed and installed.

REMOVAL (REMOTE POWER SUPPLY)

1.   Lift cabinet latch and pull drive to fully extended position.

2.   Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for Ready indicator to stop flashing then set CB1 to OFF.

3.   Disconnect ac power cable from AC INPUT connector J1 on power supply.

4.   Remove hardware securing bracket to mounts, and slide supply back far enough to allow access to P15 on power supply.

5.   Disconnect P15 and dc ground wire from power supply.

POWER SUPPLY

LOCKING
SCREW

LOCKING
HOLE

CONNECTOR J15

DRIVE

MOUNTING
BRACKET

LOCKING
HOLE

MOUNT

INTERMEDIATE SLIDE

INNER SLIDE

11D168A

Figure 5-8.   Remote Power Supply Removal and Replacement

CAUTION

After removing supply, push drive back into
rack unless replacement supply is to be in-
stalled immediately.

6. Remove power supply.

REPLACEMENT (REMOTE POWER SUPPLY)

1. Position power supply so that mounts and matching slots
   in bracket are aligned as shown in figure 5-8.

2. Connect dc ground wire and P15 to J15 on power supply.

3. Slide power supply toward drive until locking holes in
   bracket align with locking holes in mounts. Secure power
   supply bracket to mounts with mounting hardware.

4. Connect ac power cable to AC INPUT connector J1.

5. Push drive back to closed position in rack.

REMOVAL (INTEGRAL POWER SUPPLY)

1. Perform top cover removal procedure (5102).

2. Disconnect ac power cable from AC input connector J1 on
   power supply.

3. Disconnect I/O cables and terminators from I/O plate on
   power supply.

4. Press slide lock release and pull drive forward until it
   is free of slide assemblies.

5. Move drive to desired location.

6. Remove screws securing I/O plate and side plate (see fig-
   ure 5-9) to power supply.

7. Remove side plate, then remove I/O plate and cable assem-
   bly from power supply.

8. Remove screws securing power supply to drive rear panel and inner rail (or shipping bracket).

9. Move power supply away from drive to gain access to ground terminal on rear panel of drive. Ensure that RF gasket remains attached to the drive rear panel when power supply is removed.

10. Disconnect power supply ground wire from drive rear panel, then remove power supply from drive.

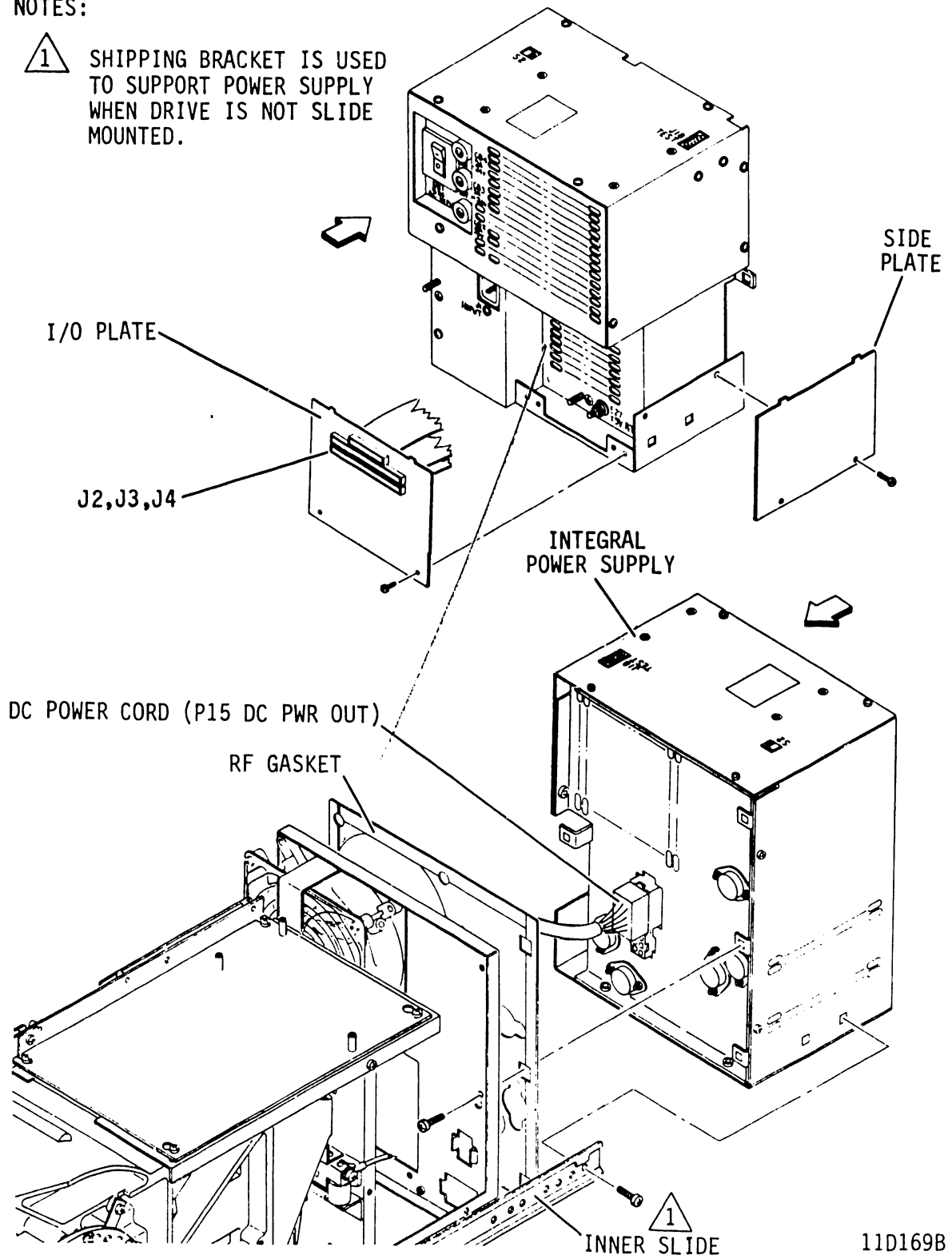11. Disconnect P15 from J15 on power supply.

REPLACEMENT (INTEGRAL POWER SUPPLY)

1. Connect power supply ground wire to ground terminal on drive rear panel.

2. Connect P15 to J15 on power supply (see figure 5-9).

3. Position power supply on drive and inner rail (or shipping bracket) and secure into place with mounting hardware.

4. Install I/O plate and cable assembly, then install side plate. Secure into place with mounting hardware.

5. Going to equipment rack, push intermediate slides to fully retracted positions inside outer slides.

6. Lift drive into position in front of rack and guide inner slides into intermediate slides. Push until lock releases engage, then pull drive to fully extended position.

7. Connect I/O cables and terminator.

8. Connect AC input connector to J1 on power supply.

9. Perform top cover replacement procedure (5102).

5206 - LOCKING SOLENOID COIL REMOVAL & REPLACEMENT

This procedure describes how to replace the locking solenoid coil. The coil is contained in a metal cannister that screws into the bottom of the module (see figure 5-10). A special wrench is required to install the solenoid (see solenoid wrench, table 2-1).
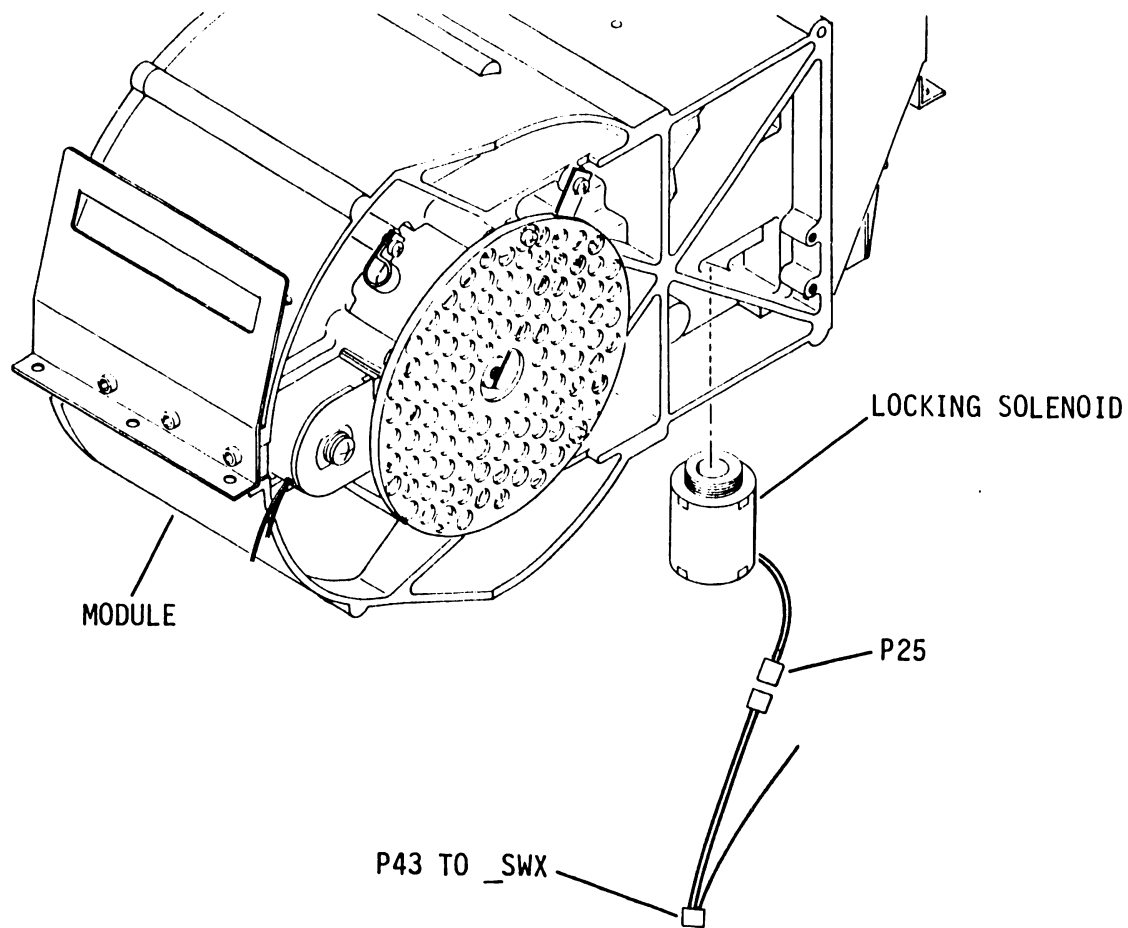
NOTES:

⚠️1 SHIPPING BRACKET IS USED
TO SUPPORT POWER SUPPLY
WHEN DRIVE IS NOT SLIDE
MOUNTED.

SIDE
PLATE

I/O PLATE

J2,J3,J4

INTEGRAL
POWER SUPPLY

DC POWER CORD (P15 DC PWR OUT)

RF GASKET

INNER SLIDE

⚠️1

11D169B

Figure 5-9.   Integral Power Supply Removal and Replacement

LOCKING SOLENOID

MODULE

P25

P43 TO _SWX

11D170A

Figure 5-10.   Locking Solenoid Coil Replacement

CAUTION

This procedure should be performed only by qualified service personnel working in a clean dust free environment. Any contaminants entering the module can damage the heads or disks resulting in loss of customer data.

REMOVAL

1.   Perform entire drive removal procedure (5101).

2.   Move drive to a clean dust free area.

3. Perform top cover removal procedure (5102).

4. Perform module removal procedure (5207), then lay module on its side to gain access to solenoid.

5. Disconnect P25 from J25 cable (see figure 5-10).

6. Using a clean, lint free cloth, carefully clean the solenoid and area surrounding the base of the solenoid.

CAUTION

To minimize chance of contamination, install new coil immediately. Do not remove new coil from its packaging until the time of installation.

7. Using solenoid wrench, turn locking solenoid coil counterclockwise and unscrew it from module.

REPLACEMENT

1. Remove new coil from its packaging, then using solenoid wrench, screw solenoid coil into place in module and tighten to 3.4 N·m (30 lbf·in).

2. Connect P25 to J25 cable.

3. Perform module replacement procedure (5207).

4. Perform top cover replacement procedure (5102).

5. Perform entire drive replacement procedure (5101).

5207 - MODULE REMOVAL & REPLACEMENT

REMOVAL

1. Perform entire drive removal procedure (5101) and move drive to a convenient work area.

2. Perform top cover removal procedure (5102).

3. Perform front panel removal procedure (5103).

4. Remove screws securing operator panel bracket to chassis and lift bracket, with operator panel and cable attached from drive (see figure 5-11).

P28 P32

MODULE

HANDLE

GROUND STRAP

GROUND STRAP

P43

P41

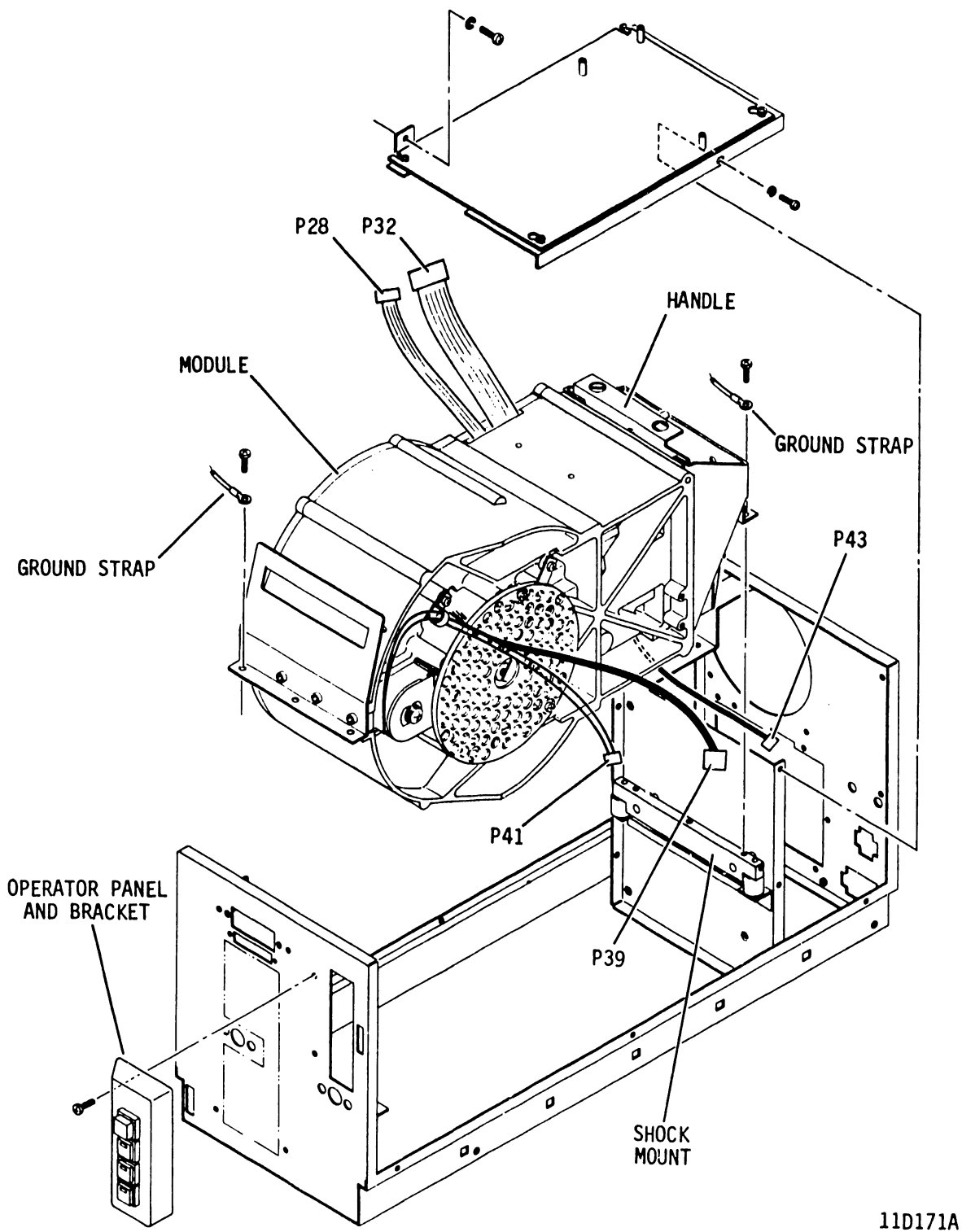OPERATOR PANEL
AND BRACKET

P39

SHOCK
MOUNT

11D171A

Figure 5-11. Module Removal and Replacement

5. Disconnect P27 and P32 from _UGX/_VHX board.

6. Disconnect P28 from _VCX board.

7. Disconnect P39, P41 and P43 from _SWX board.

8. Remove screws securing _UGX/_VHX board bracket and lift bracket (with _UGX/_VHX attached) off drive.

CAUTION

Be certain to have a firm grip on module and handle (if present) before attempting to lift it from drive. Also, take care not to damage cables when removing module.

9. Remove screws (and ground straps) securing module to shock mounts. Grasp module handle (if present) and carefully lift module clear of drive.

REPLACEMENT

1. Install module as follows:

    a. Place module in position shown on figure 5-11.

    b. Set module on shock mounts and, while holding ground straps in place, loosely install mounting screws.

    c. Ensure that space between module and back side of mother board is approximately 7/8 inch, then hold shock mounts to prevent twisting and tighten screws to 1.3 N·m (10 lbf·in).

2. Install operator panel and bracket to chassis.

3. Perform front panel replacement procedure (5103).

4. Perform a final check of all cable routing and connections.

5. Set board bracket (with __UGX/__VHX attached) in place, align holes, then install and tighten screws.

6. Connect P28 to J28 on _VCX board.

7. Connect P39 to J39, P41 to J41 and P43 to J43 on __SWX board.

8. Connect P27 to J27 and P32 to J32 on _UGX/_VHX board.

9. Perform top cover replacement procedure (5102).

10. Perform entire drive replacement procedure (5101).

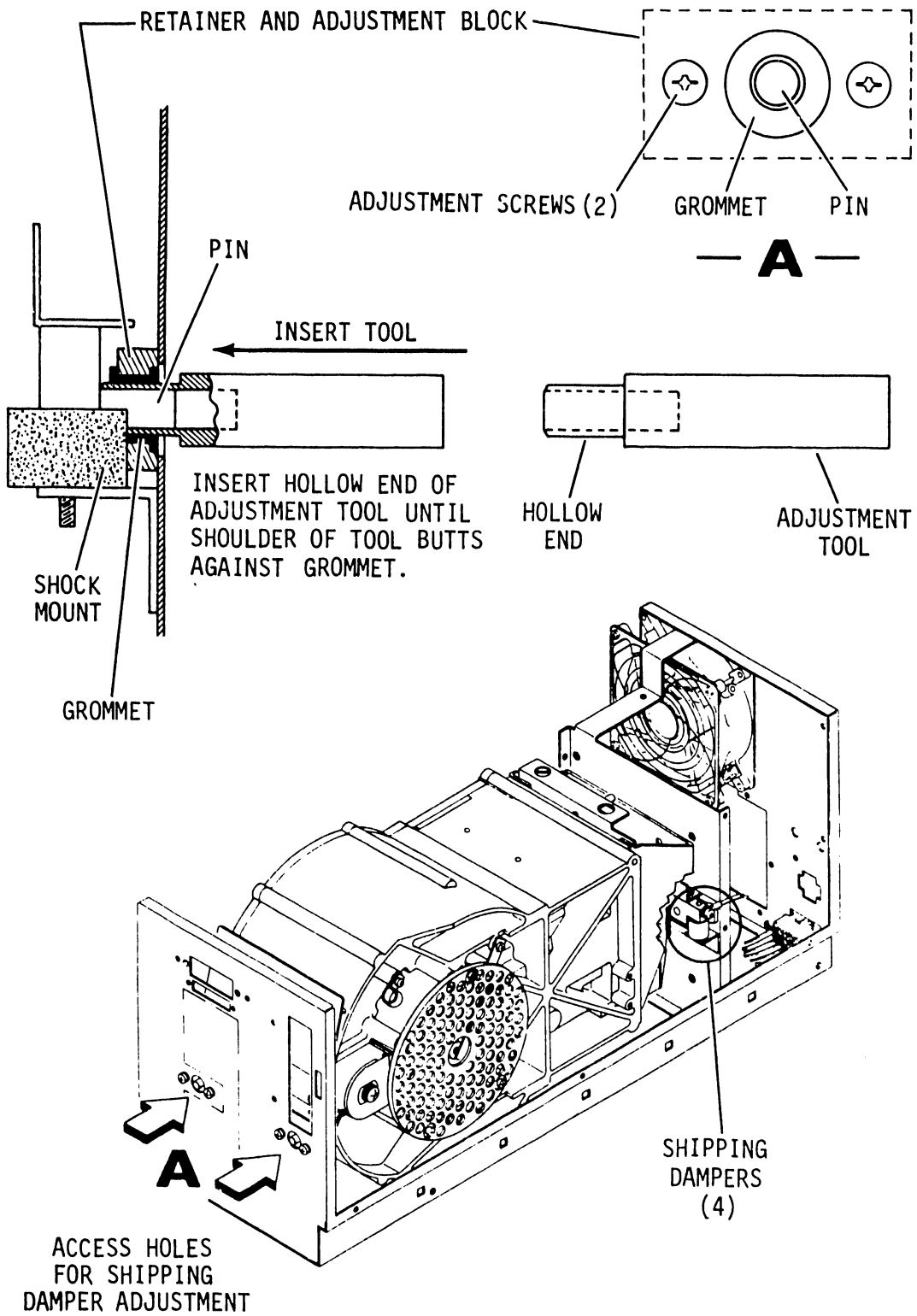## 5208 - SHIPPING DAMPER ADJUSTMENT PROCEDURE

Shipping damper adjustment is only necessary if a module shock mount is replaced. Figure 5-12 shows the shipping dampers and adjustment tool. Four of the adjustment tools are required to perform this procedure.

1. Perform front panel removal procedure (5103) and _SWX board removal procedure (5304) to gain access to the shipping damper adjustment screws.

NOTE

It is necessary to use a philips screwdriver not greater than 4 inches in length or a right angle philips, to adjust the two shipping dampers, located behind _SWX board (see figure 5-12).

2. Position each of the four adjustment tools as follows (all four tools must be in place before adjustment can proceed):

   a. Insert hollow end of adjustment tool into retainer block and grommet.

   b. Push tool until shoulder butts against grommet.

3. Fit pin on each adjustment block into hollow ends of tools until all four blocks butt tightly against tools.

4. Secure blocks by gradually tightening screws, going sequentially from one block to the next, until all screws are tightened to 3.4 N·m (30 lbf·in). Use care not to move blocks out of adjustment.

5. Remove adjustment tools.

6. Perform front panel replacement procedure (5103) and _SWX board replacement procedure (5304).

RETAINER AND ADJUSTMENT BLOCK

ADJUSTMENT SCREWS (2)   GROMMET   PIN

— A —

PIN

INSERT TOOL

INSERT HOLLOW END OF
ADJUSTMENT TOOL UNTIL
SHOULDER OF TOOL BUTTS
AGAINST GROMMET.

HOLLOW
END

ADJUSTMENT
TOOL

SHOCK
MOUNT

GROMMET

SHIPPING
DAMPERS
(4)

ACCESS HOLES
FOR SHIPPING
DAMPER ADJUSTMENT

A

11D179A

Figure 5-12.   Shipping Damper Adjustment

5209 - CABLE REPLACEMENT

All interassembly cables are of the flat ribbon type with the exception of the dc power cable. The dc power cable is made up of individual wires tied together.

All of the flat ribbon cables have one end permanently attached to an assembly and are referred to as trailing cables. When a trailing cable is defective, the cable and the attached assembly must be replaced. However, the dc power cable can be replaced as a separate item.

5210 - MOTOR ASSEMBLY REMOVAL & REPLACEMENT

This procedure describes how to replace the motor, which is located on the module assembly beneath the motor shield (see figure 5-13). A special motor removal tool (see table 2-1 for part number) is required to remove or install the motor.

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect P39 on _SWX board and remove cable from cable clips.

3. Remove screws attaching motor shield and remove shield (See figure 5-13).

4. Remove hardware attaching ground spring and remove spring.

5. Release brake by loosening screw securing brake to bottom of module.

6. Remove three screws securing motor rotor to spindle.

7. Align motor removal tool as shown in figure 5-13. Secure three captive bolts to holes vacated in step 3.

8. Free plunger on tool by disengaging locking pin.

NOTE

In the next step, ensure that central shaft of tool centers on ground spring contact button.

9. Push plunger down and rotate motor rotor to align captive screws with any three of the eight threaded holes in rotor. Tighten captive screws.

83324770 B

①
SHIELD AND GROUND SPRING REMOVAL

GROUND SPRING

MOTOR SHIELD

BRAKE
RELEASE SCREW

GROUND SPRING
CONTACT BUTTON

②
MOTOR REMOVAL

MOTOR STATOR

MOTOR CLAMP

MOTOR
REMOVAL
TOOL

MOTOR ROTOR

CAPTIVE BOLT

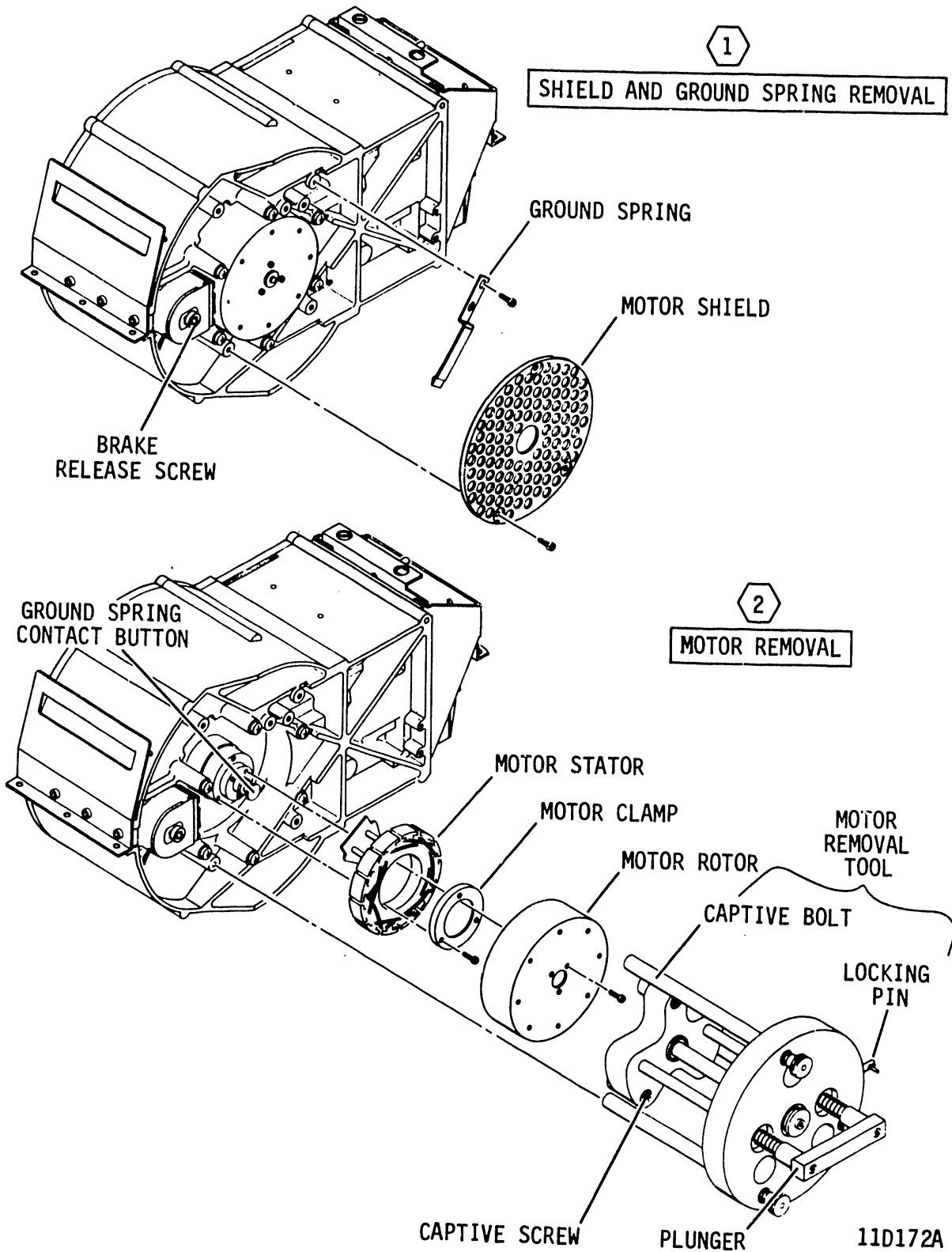LOCKING
PIN

CAPTIVE SCREW   PLUNGER   11D172A

Figure 5-13. Motor Assembly Removal and Replacement

10. Remove rotor by pulling plunger.

11. Remove tool and rotor from module by loosening captive bolts.

12. Remove rotor from tool by loosening captive screws.

13. Remove screws securing motor clamp to spindle. Remove motor clamp.

14. Remove motor stator and cable from spindle.

REPLACEMENT

1. Position motor stator and cable on spindle.

2. Install motor clamp over motor with attaching screws.

3. Attach motor rotor to motor removal tool with captive screws on tool.

4. Pull plunger on tool to upward position.

5. Align tool as shown in figure 5-13. Secure three captive bolts to module.

NOTE

In the next step, ensure that central shaft of tool centers on ground spring contact button.

6. Place rotor in position over motor by pushing plunger down.

7. Loosen captive screws attaching tool to rotor.

8. Remove tool by loosening captive bolts.

9. Manually rotate motor to align three holes in rotor with holes in spindle.

10. Attach rotor to spindle with three attaching screws.

11. Perform steps 4, 5, and 6 of Brake Adjustment procedure (5204).

NOTE

In the next step, ensure that ground spring is centered over contact button.

12. Install ground spring with attaching hardware.

13. Install motor shield with attaching hardware.

14. Connect cable P39 to J39 on _SWX board and secure cable with cable clips.

15. Perform top cover replacement procedure (5102).

5301 - —UGX/—VHX BOARD REMOVAL & REPLACEMENT

This procedure describes removal and replacement of the read/write board. In addition to the _UGX and _VHX boards, it applies to the _SUX board (used in older 515 MB drives).

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect P32 and P27 from _UGX/_VHX board.

3. Loosen screws securing __UGX/__VHX to bracket (see figure 5-14).

4. Place a screwdriver in board slot (shown in figure 5-14) to pry it loose from J30 connector (on mother board), then remove board (out keyhole slots) from drive.

REPLACEMENT

1. Align board to mounting hardware, then connect it to mother board (P30 to J30) and secure into place (see figure 5-14).

2. Connect P32 to J32 and P27 to J27 on _UGX/_VHX board.

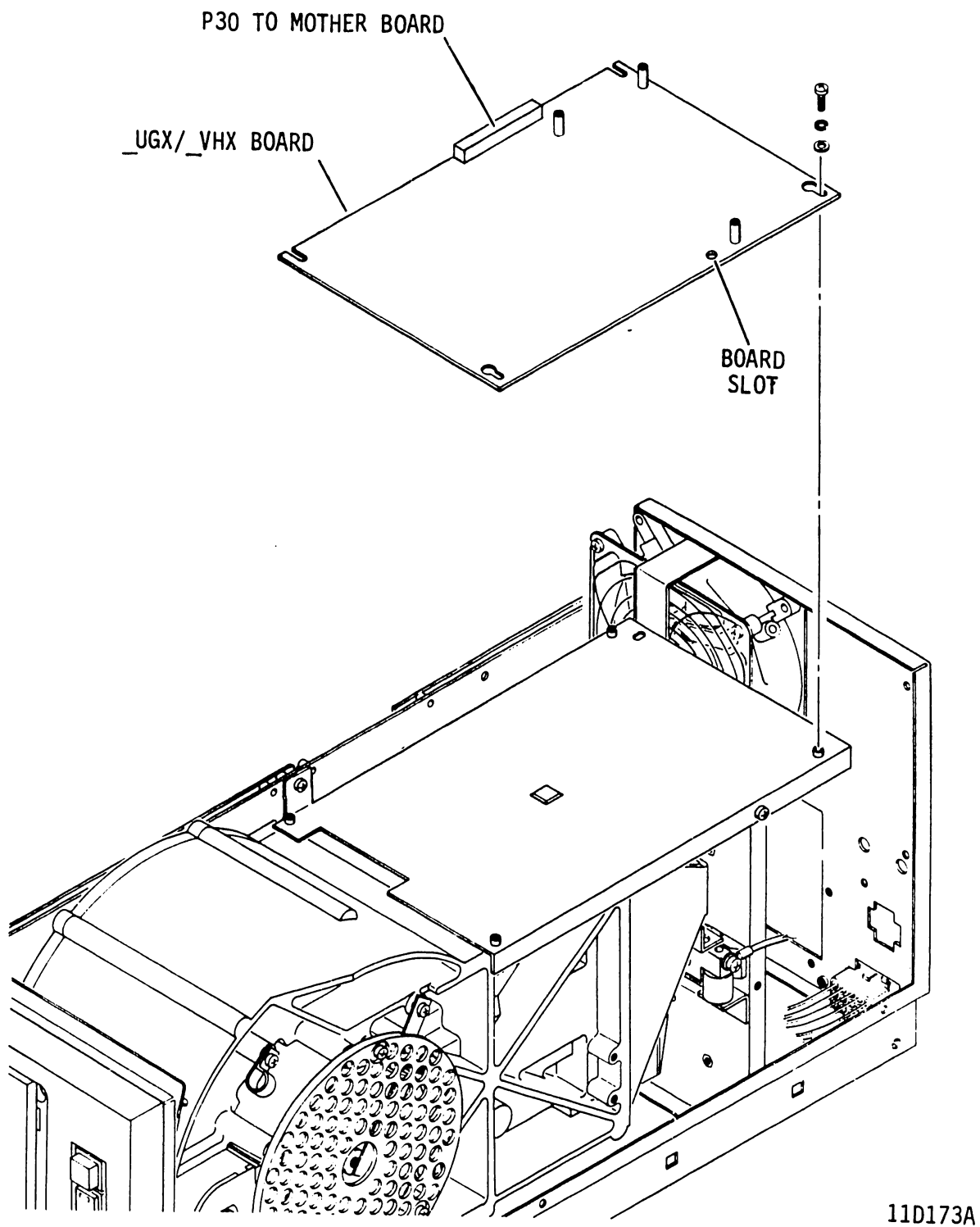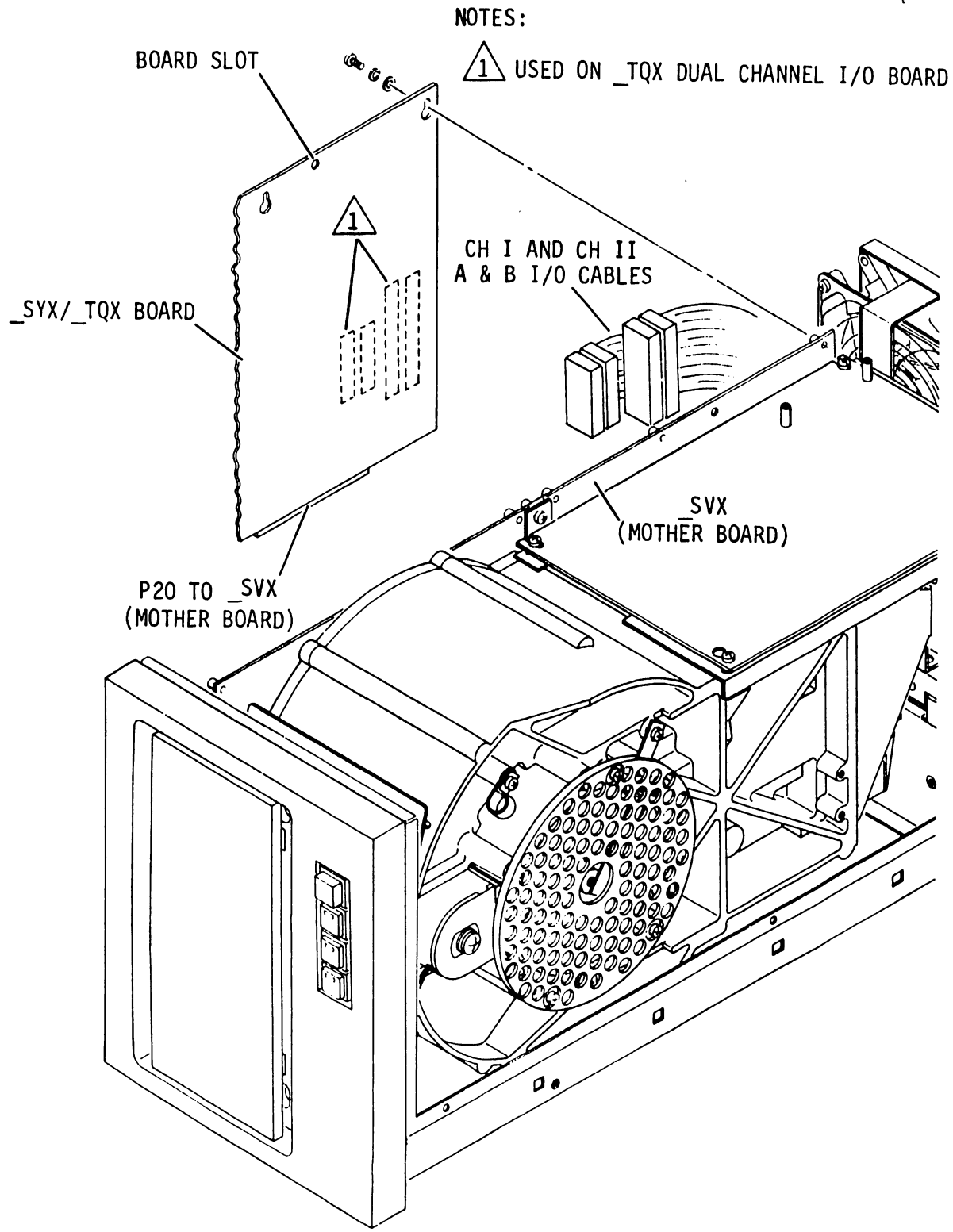3. Perform top cover replacement procedure (5102).

P30 TO MOTHER BOARD

_UGX/_VHX BOARD

BOARD
SLOT

11D173A

Figure 5-14.   _UGX/_VHX Board Removal & Replacement

83324770 B

5302 - —SYX/—TQX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5101).

2. Disconnect P27 from _UGX/_VHX board.

3. Disconnect A and B cables from _SYX/_TQX board (see figure 5-15).

4. Loosen the two screws (top of board) securing _SYX/_TQX board to drive.

5. Place a screwdriver in board slot (shown in figure 5-15) to pry it loose from J20 connector (on mother board), then remove board (out keyhole slots) from drive.

REPLACEMENT

1. Align board to mounting hardware, then connect it to mother board (P20 to J20) and secure into place (see figure 5-15).

2. Connect P27 to J27 on _UGX/_VHX board.

3. Connect A and B cables to _SYX/_TQX board.

4. Adjust switches on board as necessary, then perform top cover replacement procedure.

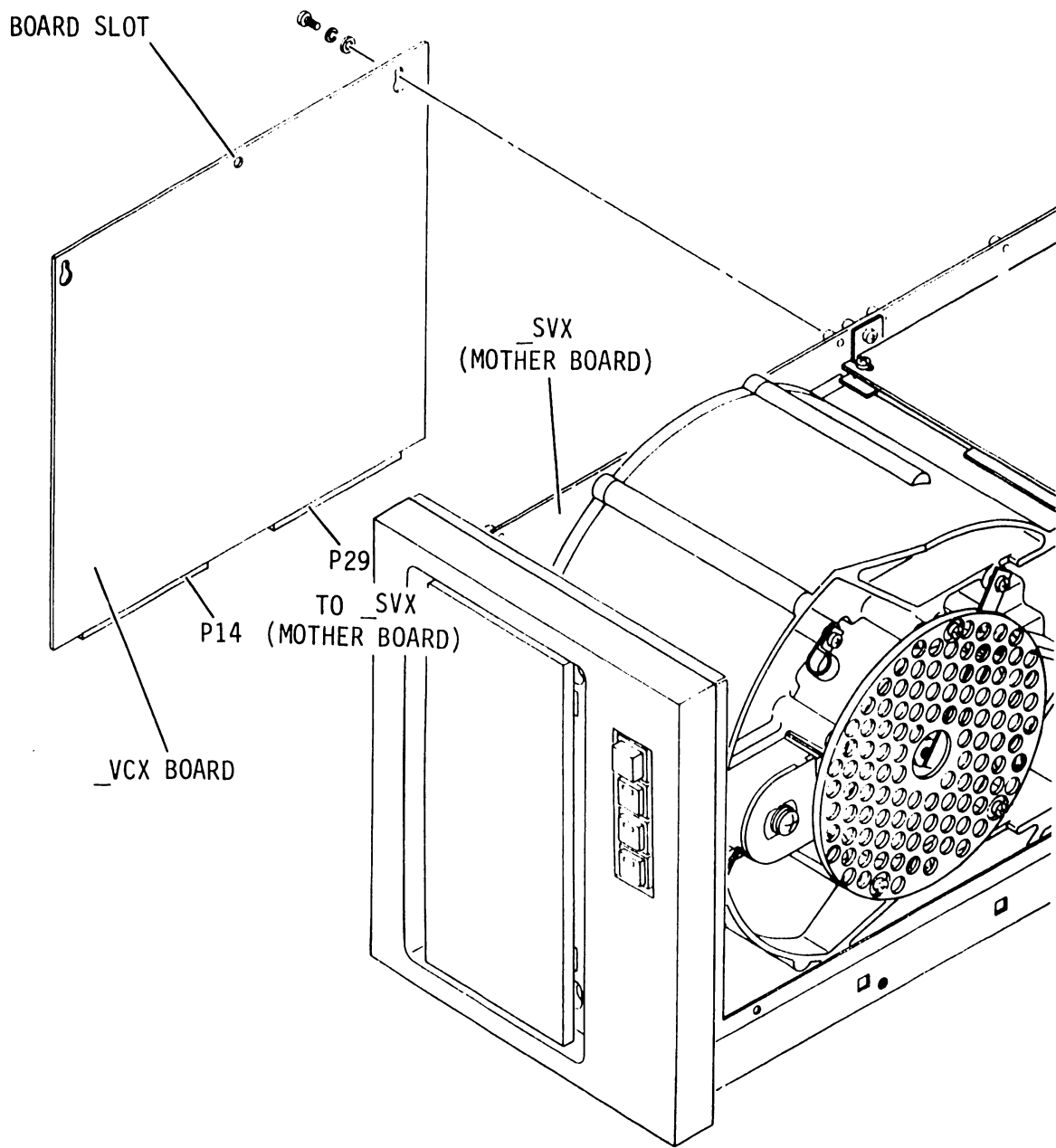## 5303 - —VCX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5303).

2. Disconnect P13, P26 and P28 from _VCX board.

3. Loosen the two screws (top of board) securing _VCX board to drive (see figure 5-16).

4. Place a screwdriver in board slot (shown in figure 5-16) to pry it loose from J14 and J29 connectors (on mother board), then remove board (out keyhole slots) from drive.

NOTES:

△1 USED ON _TQX DUAL CHANNEL I/O BOARD

BOARD SLOT

_SYX/_TQX BOARD

CH I AND CH II
A & B I/O CABLES

_SVX
(MOTHER BOARD)

P20 TO _SVX
(MOTHER BOARD)

11D174A

Figure 5-15.   _SYX/_TQX Board Removal & Replacement

BOARD SLOT

_SVX
(MOTHER BOARD)

P29

TO _SVX
P14 (MOTHER BOARD)

_VCX BOARD

11D175

Figure 5-16.   _VCX Board Removal & Replacement

REPLACEMENT

1. Align board to mounting hardware, then connect it to mother board (P14 to J14 and P29 to J29) and secure into place (see figure 5-16).

2. Connect P13 to J13, P26 to J26 and P28 to J28 on _VCX board.

3. Adjust switches on board as necessary, then perform top cover replacement procedure (5102).

5304 - —SWX BOARD REMOVAL & REPLACEMENT

The __UGX/__VHX board bracket must first be removed from the drive, to allow removal of _SWX board. This step is explained in the following procedure.

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect P27 and P32 from _UGX/_VHX board.

3. Remove the screws securing __UGX/__VHX board bracket to drive, then disconnect P30 from J30 (on mother board) and remove board and bracket assembly from drive (see figure 5-17).

4. Disconnect P39, P41 and P43 from _SWX board.

5. Loosen the two screws (on motor side of drive) securing _SWX board to drive.

6. Place a screwdriver in board slot (shown in figure 5-17), to pry it loose from J24 connector (on mother board), then remove board (out keyhole slots) from drive.

REPLACEMENT

1. Align board to mounting hardware, then connect it to mother board (P24 to J24) and secure into place (see figure 5-17).

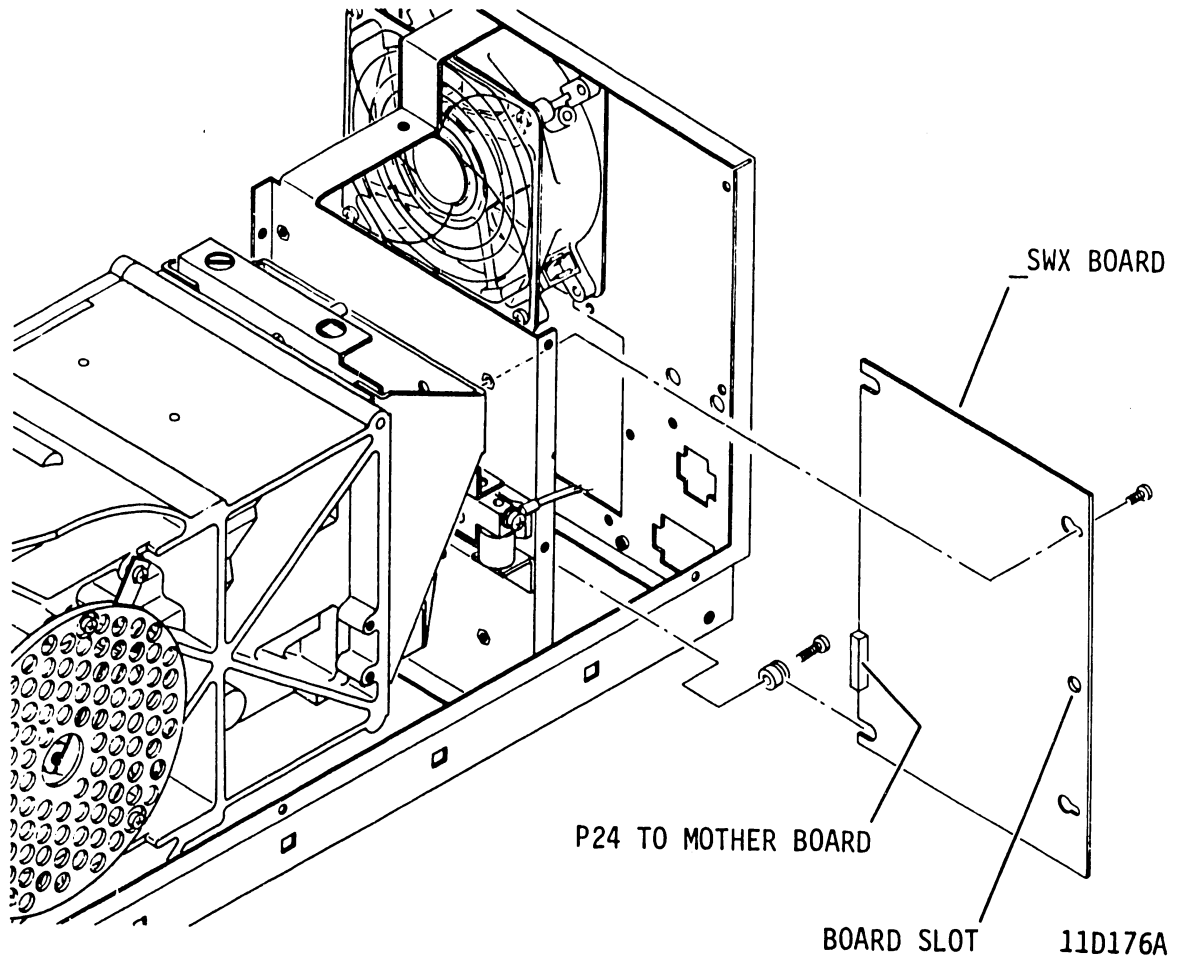2. Connect P39 to J39, P41 to J41 and P43 to J43 on _SWX board.

Figure 5-17. _SWX Board Removal & Replacement

3. Install __UGX/__VHX board and bracket assembly to drive, connect to mother board (P30 to J30) and secure into place with screws.

4. Connect P27 to J27 and P32 to J32 on _UGX/_VHX board.

5. Perform top cover replacement procedure (5102).

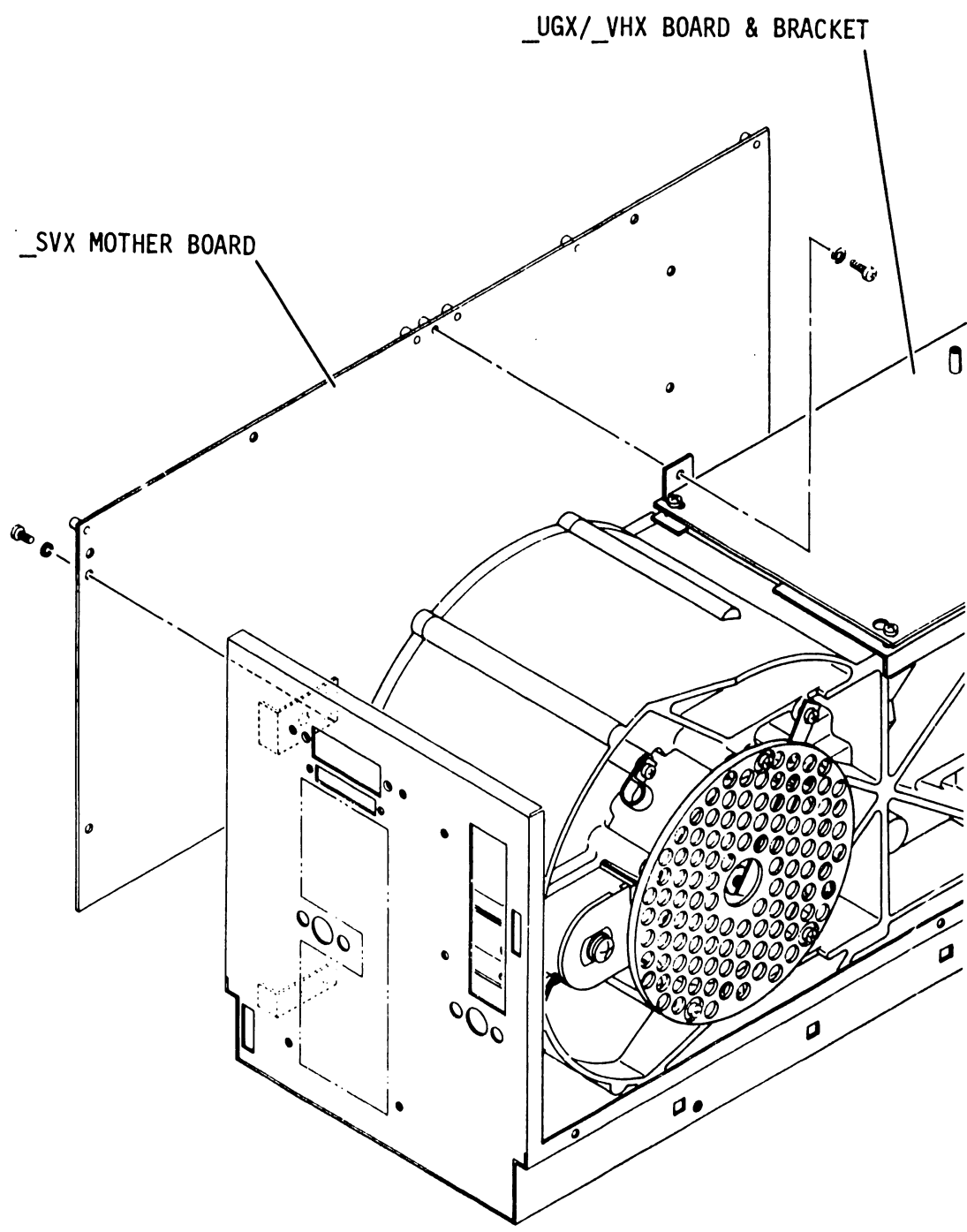## 5305 - —SVX BOARD REMOVAL & REPLACEMENT

Since all logic boards and power connectors are connected to the mother board (__SVX), it is advisable to remove the drive from the equipment rack to perform this procedure.

REMOVAL

1. Perform top cover and entire drive removal procedures (5101 and 5102)).

2. Perform the following procedures:

   a. _UGX/_VHX board removal (5301).

   b. _SYX/_TQX board removal (5302).

   c. _VCX board removal (5303).

3. Remove screw securing __SVX board to __UGX/__VHX board bracket (see figure 5-18).

4. Disconnect P35 and P38 on _SVX board.

5. Remove screws securing _SVX board to drive. Pull board away from _SWX board (to disconnect P24 from J24), then remove _SVX board from drive.

REPLACEMENT

1. Align board to mounting hardware, connect _SVX (mother board, P24 to J24) to _SWX board, then secure into place with screws (see figure 5-18).

2. Connect P35 to J35 and P38 to J38 on _SVX board.

3. Install screw from __UGX/__VHX board bracket to __SVX (mother board).

4. Perform the following procedures:

   a. _UGX/_VHX board replacement (5301).

   b. _SYX/_TQX board replacement (5302).

   c. _VCX board replacement (5303).

5. Perform top cover and entire drive replacement procedures (5101 and 5102)).

_UGX/_VHX BOARD & BRACKET

_SVX MOTHER BOARD

11D177A

Figure 5-18. _SVX Board Removal & Replacement

END