WANG

7300

TELECOMMUNICATION CONTROLLERS

Models:

TCB-1
DLP 64
DLP 128

Customer Engineering
Product Maintenance Manual

729-0887-B

PREFACE

This document is the Standard Maintenance (STD) Manual for the TCB-1, DLP 64, and DLP 128 TC Controllers. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product.

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate and diagnose faults of the TCB-1, DLP 64, and DLP 128 TC Controllers. It will be updated on a regular schedule.

Third Edition, February (1984)

This edition of this STD manual obsoletes document(s) no. 729-0887 and 729-0887-A. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as a Publication Update Bulletin (PUB) or subsequent editions.

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TC CONTROLLER CONVENTIONS

In the chapters that follow reference will be made to the use and implementation of the TCB-1, and in the case of this manual, the DLP 64, and DLP 128 TC Controllers. These TC controllers, specifically the DLP 64 and DLP 128, have been documented and referred to in the following manner:

OIS and Alliance Systems

TCB-1 as - TC-SC-1, TC-SC-2, TC-AC-2, or 6554-1A through 6554-4A.
DLP 64 as - TCB-3 64K, or OIS-TC.
DLP 128 as - TCB-3, OIS-TC1.

VS Systems

TCB-1 as - 6554-1 through 6554-4.
DLP 64 as - TCB-3 64K, or VS-TC.
DLP 128 as - TCB-3, or VS-TC1.

In ordering this controller the TCB-3 "convention" or "nomenclature," is used by Logistics in filling field order requirements. This manual will refer to these controllers as a DLP 64 (TCB-3 64K), and as a DLP 128 (TCB-3). Refer to Chapter 4, for reference to part numbers.

CHAPTER 1 INTRO-DUCTION

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The scope of this manual concerns the TCB-1, DLP 64 (TCB-3 64K), and DLP 128 (TCB-3) TC Controllers, and is intended to enable field personnel to complete the maintenance tasks described below, and to understand what TC controller indications to look for during normal operation, as well as indications relating to fault conditions. This will enable fault isolation, and the action to take to service the fault. Maintenance procedures concern the following areas:

Unpack, set switches and install in OIS and VS Systems.
Refer to diagnostic and loopback test requirements.
Run diagnostics.
Define error indications if diagnostics fail.
Service fault.

Chapter Two provides a block-level description and a functional overview of the TCB-1, DLP 64, and DLP 128 Controllers.

1.2 SYSTEM DESCRIPTION

The TCB-1, DLP 64, and DLP 128, are a motherboard/daughterboard arranged telecommunications controllers. They are designed for use on all Z80A-CPU-based OIS and VS Systems. The TC Controllers are installed and made operational in OIS 40/50, 105/115/125A/130A, and 140/145 Masters, and in the Telecommunications Processor (TCP). One TC Controller may be used on OIS 40/50, 105/115/125A/130A Systems, while 140/145 Systems may be configured with two. Up to four TC controllers may be used in each TCP.

The TCB-1, DLP 64 and DLP 128, Controllers contain interface connectors that are connected, by cable, to an I/O port on the rear of the OIS master or TCP. This cable interface from the controller to the I/O port, enables physical connection of one of four interfaces to a modem or null modem. These controllers support RS-232-C, RS-366, RS-449, and X.21 interfaces. The interfaces that are supported and installed, depends on the software emulation that the system is using. Refer to Chapter Four, Installation Requirements, for the above mentioned systems for more detail.

The TCB-1, DLP 64 and DLP 128 Controllers, support communications software that allows emulation of protocols, the type employed depending on the hardware and software requirements. Typically, emulator software allows a VS System through a TCP, or OIS Master to communicate with other VS or OIS Masters, as well as non-Wang systems. The present available emulation environment supported, and the required communications hardware (TCB-1, DLP 64 and DLP 128), are defined in Table 1-1.

The TCB-1 and DLP 64 contain 64K bytes of memory, while the DLP 128, an enhanced version of the DLP 64 contains 128K bytes of memory. The DLP 64 functionally replaces the TCB-1. The DLP 128, due to increased memory capacity, contains additional circuitry for memory selection.

1.3 COMMUNICATION REQUIREMENTS

Table 1-1 specifies communication requirements of an OIS Master and TCP.

Table 1-1
OIS/TCP TCB-1, DLP 64/128
Communication Requirements

		OIS 40/50	Other Z-80 based OIS and Alliance Systems	VS 25/45-100
WANG NETWORKING	WSN Multi-Point Primary*	N/A	N/A	TCB-1 DLP-64
	WSN Multi-Point Secondary*	DLP-64	TCB-1 DLP-64	TCB-1 DLP-64
	WSN Point-to-Point*	DLP-64	TCB-1 DLP-64	TCB-1 DLP-64
	IDS	N/A	N/A	DLP-64
	X.25	DLP-128	DLP-128	DLP-128
SNA	3274 SNA/SDLC	DLP-128	DLP-128	DLP-64
	3777 SNA/SDLC	N/A	N/A	DLP-64
BISYNC	2780/3780 WPS Enhanced	DLP-64	DLP-64	N/A
	3271 BSC	DLP-64	TCB-1 DLP-64	N/A
ASYNC	Async TTY	DLP-64	DLP-64	N/A
	Teletex		DLP 128	N/A

* Wang Systems Networking (WSN) formerly Remote Wangnet.

1.4 RELATED WANG DOCUMENTATION

Table 1-2 Related Wang Documentation

Document	Reorder No.	Description
Telecommunications Processor (TCP) Product Maintenance Manual	729-1043	Provides installation procedures, data set test descriptions and describes characteristics of Interfaces.
OIS 3270 Emulation User Guide	700-6980	Provides a detailed description of all 3270 Emulation procedures.
Network User's Guide to File Transfer and Remote Log-on	800-1316-RU-02	Provides procedures that will enable interaction of VS and OIS Systems. File transfers, remote log-on and document transfer procedures are discussed.
Network Configuration and Operations Guide	800-1317-RO-02	Provides procedures to edit network edit network configuration files and assign names, services and addresses to VS and OIS systems implemented in a network.
Alliance Batch Communication Interfaces	700-7149	Provides information concerning Users Guide batch TC operation using Alliance software.

CHAPTER 2

THEORY OF OPERATION

CHAPTER 2
THEORY OF OPERATION

2.1 INTRODUCTION

The TCB-1 and DLP 64/128 Controllers are comprised of a motherboard which contains the Processor Section, a daughterboard which contains the Data Link Section, and the Memory Controller Section.

The Processor Section contains circuitry to enable DMA data transfers through the appropriate interface, and to generate vectored interrupts for special characters. The Data Link Section contains circuitry that interfaces the OIS Master/TCP or VS-TCP, through dual coaxial cable as a slave data link. The Memory Controller Section coordinates TC controller memory access between the processor and the data link section. The following paragraphs describe the controllers. Characteristics that are unique to a controller(s) will be identified.

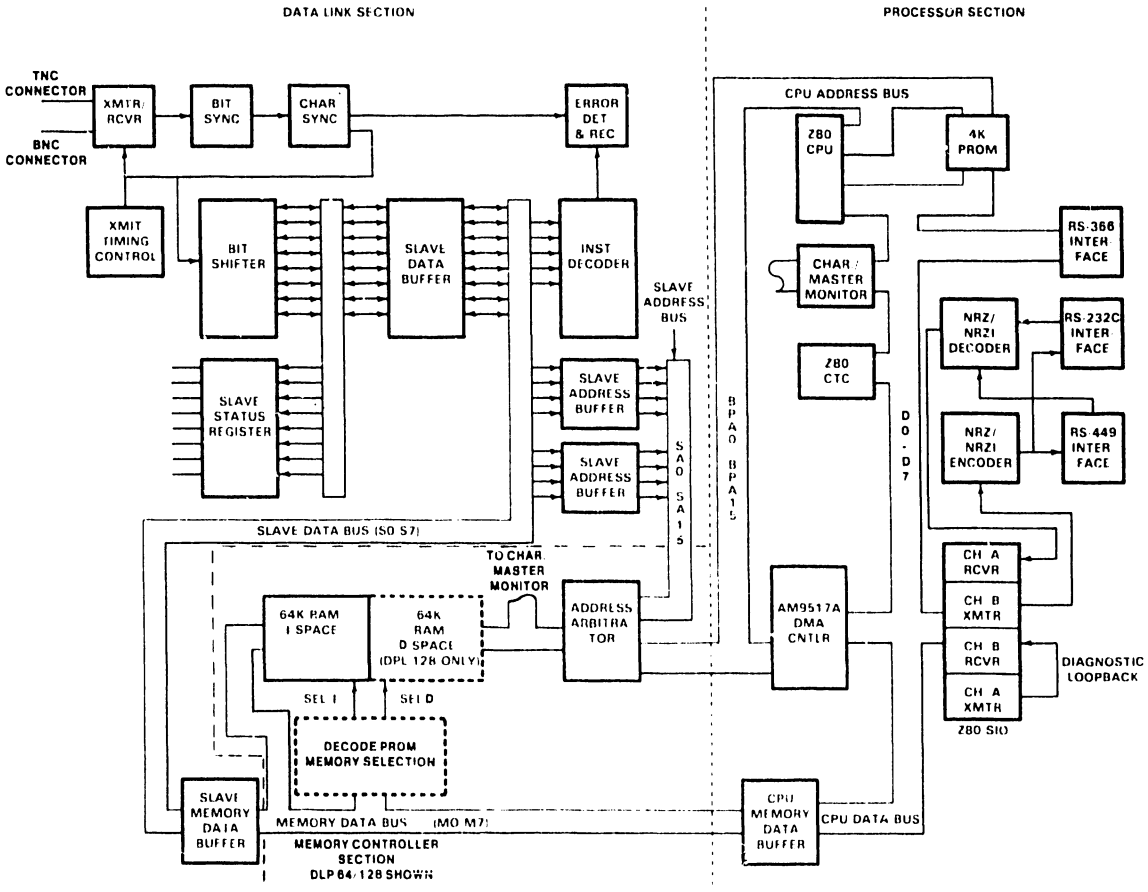


Figure 2-1 Functional Block Diagram

2.2 PROCESSOR SECTION

The Processor section comprises the following components:

Z80A-CPU
Z80A-CTC
Z80A-SIO/2
AM 9517A DMA Controller
Character/Master Monitor
PROM Memory
RS-232C Interface
RS-449 Interface
RS-366 Interface

Z80A-CPU - The Z80A-CPU is the main control and processing element of the TC controller. It operates on a 250 ns clock cycle (4 MHz) and shares a common data bus with the DMA controller and the Z80A-Serial Input Output Controller (SIO/2). The Z80A-CPU resides at location L98.

Z80A-Counter Timer - The Z80A-Counter Timer Chip (CTC), provides timing and counting functions for the TC controller. The CTC is divided into four channels, with channel 0 providing baud rate clock, channel 1 providing software event timing, and channels 2 and 3 alerting the CPU of DMA completion. The Z80A-CTC resides at location L92.

Z80A-Serial Input/Output Controller - The Z80A-Serial Input/Output Controller (SIO/2), converts 8 bit parallel data into one of several serial formats and vice versa. Both synchronous and asynchronous operation, and both character and bit-oriented protocols are supported.

In addition the Z80A-SIO/2, performs character and line buffering, line control and status monitoring, and error protection and detection. The Z80A-SIO/2 consists of two channels, channel A and channel B. Normally the channel A receiver and the channel B transmitter are used for all transmit and receive operations. This allows full duplex operation if required. When running internal diagnostic loopback tests, the channel A transmitter and channel B receiver are used. The SIO/2 resides at location L69.

AM 9517A DMA Controller - The DMA Controller allows high speed data transfers between the Z80-SIO/2 and D space RAM memory. It is controlled by the Z80A-CPU and will support speeds up to 880 Kbps with minimal system overhead. The DMA controller is a four channel device, supporting both SIO/2 transmitters as one two-channel pair, and both SIO/2 receivers as the other two-channel pair. The DMA controller resides at location L94.

This combined with the use of a "next" and "current" channel register for each channel pair, and the Z80A-CTC providing interrupt signaling, insures quick handling of SIO/DMA requests.

Character/Master Monitor - The Character/Master Monitor, provides supervisory services for the TC controllers, by alerting the Z80A-CPU when a specific memory write occurs. Its circuits consist of various components, but are located from L76 to L83.

The character portion of the monitor "watches", for program specified DMA characters deposited in memory, which act as lookup addresses for the 256 byte vector table. The master portion uses data link memory addresses for the same purpose. The retrieved byte from the vector table allows for generation of one of 256 different interrupts, few of which are used at this time. The circuitry responsible for addressing vector memory include multiplexers (L96, L97, and L81). Circuitry associated with character and master monitor supervisory services include:

The Monitor Control Register (L49)	The monitor control register contains eight bits that control the mode of monitor operation, refer to Paragraph 2.2.2, for more detail.
The Monitor Base Register (L66)	The monitor base register contains eight bits, six of which form the starting address of the Master Slave Communication Area (MSCA).
Vector Memory (L79, L80)	Vector memory comprises two 1K-by-4 bit static RAM chips arranged as 1K eight bits. Vector memory contains the interrupt vectors used when program specified characters are deposited, and addresses are written in memory.

PROM Memory - PROM memory is used for TC controller power-up diagnostics. It resides at location L95. The PROM memory consists of 4K worth of extensive power-up diagnostics that will even point to a specific defective RAM chip. It consumes 4K worth of overall memory addressing space.

RS-232C Interface - The RS-232C Interface circuits provide the necessary interface to connect to the standard 25 pin EIA modem connection on the back of the TC controller - equipped OIS Master or TCP. Most of the RS-232C Interface circuits reside at locations L14, L15, L16, L33, and L34.

RS-449 Interface - The RS-449 Interface circuits provide the necessary interface to connect to the 37 pin EIA modem connection on the back of the TC controller - equipped OIS Master or TCP. Most of the RS-449 interface circuits reside at locations L17, L18, L35, and L36. The interface circuitry of the RS-449 interface, supports and is used to implement the X.21 interface. The RS-449 interface is not widely used. Notice that the RS-232C and RS-449 signals may be encoded in NRZ or NRZI format and that either format is receivable.

RS-366 Interface - The RS-366 Interface circuits provide the necessary interface to connect to the 25 pin EIA connection on the back of the TC controller-equipped OIS Msster or TCP. Most of the RS-366 Interface circuits reside at locations L10 - L13. This interface is used to connect to an Automatic Calling Unit for automatic switched network call establishment for communications.

2.2.1 Processor Section Overview

The Z80A-CPU, is the main processing element of the TC controller. The Z80A-CPU controls via software, all functions of the TC controller. Software control, allows the CPU to initialize and program the DMA controller, the SIO/2, CTC, and character/master monitors for all operations.

On a read operation from a telecommunications line, data is input to the motherboard from an interface port (RS-232-C, RS 449/X.21). This data is clocked into the SIO/2 channel A receive port at the baud rate specified by the CTC (channel zero). The SIO/2 converts the serial data to eight bit parallel data. Conversely, during a transmit operation, eight bit parallel data is converted to serial data via the SIO/2 channel B function. This data is transmitted at the specified baud rate to an interface port.

Transfer of eight bit parallel data from/to channel A or channel B of the SIO/2 is accomplished via SIO/2 signals (W/RDYA) or (W/RDYB), which are used to form DMA requests.

Once a DMA request is granted, the DMA controller gains control of the memory address bus and places the low order address on the processor address bus (PA0-PA7), while the high order address (PA8-PA15), are sourced from the DMA data lines (D0-D7). The DMA controller generates a memory request, and transfer of eight bits of data then proceeds directly to/from the SIO/2 and memory. DMA channels 0 and 2, support data input from the SIO/2 receiver and are called the receiver pair. DMA channels 1 and 3, support data output to the SIO/2 transmitter and are referred to as the transmit pair.

When a DMA end of process (EOP) is signalled for a particular channel pair (transmit or receive), the next channel register is copied to the current channel register effectively switching to the next inactive or available DMA channel of that pair. In addition, the CTC will signal an interrupt for that pair (CTC channel 2 = DMA receiver pair; channel 3 = DMA transmit pair).

If the character monitor is enabled during a DMA write to memory (SIO/2 receive function), the characters being deposited are "watched" as explained in Paragraph 2.2.2.

PROCESSOR SECTION

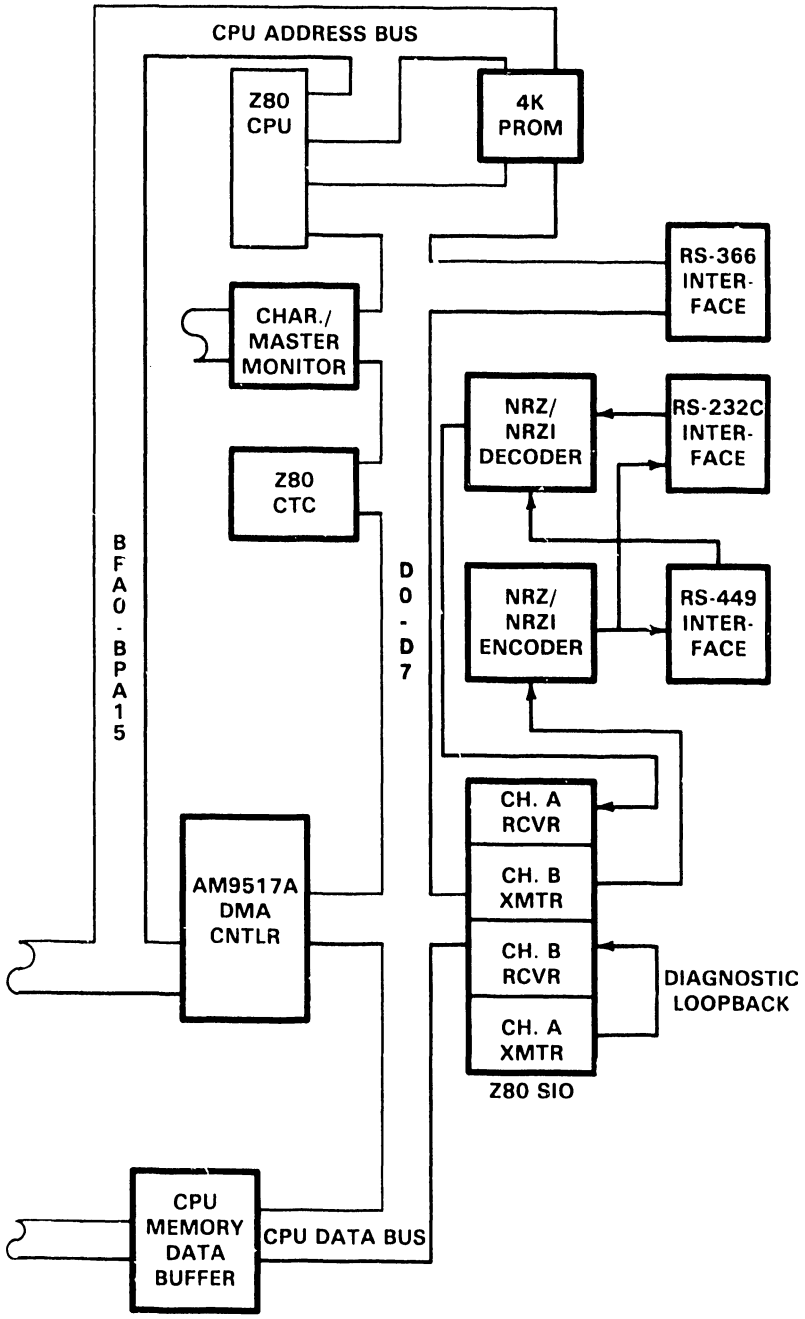


Figure 2-2 Processor Section Block Diagram

2.2.2 Character and Master Monitor

The Character and Master Monitors provide supervisory services for the TCB-1, DLP 64 and DLP 128 controllers. These monitors alert the Z80A-CPU if a specific memory write occurs. Both monitors may be enabled simultaneously.

The Character Monitor, which is enabled by the CHARMON signal, "watches" characters deposited in memory by the DMA controller. Thus, the character monitor can interrupt the Z80A-CPU when specific characters (control, format) are deposited. The Z80A-CPU can then perform an immediate action such as disabling the receiver CRC or switching buffers.

The Master Monitor, enabled by the MASMON signal, "watches" the data link memory write accesses, and can interrupt the Z80A-CPU whenever a OIS master or VS, accesses the master/slave communication area (MSCA) of controller memory. This interrupt may be used to queue another request, awaken a sleeping task, etc.

The Character and Master monitor circuits include the monitor control register, the monitor base register, vector memory, the monitor FIFO, and multiplexer chips and associated circuitry.

The monitor control register, contains eight control, bits six of which determine the mode of monitor operation. The two remaining bits control the deadman timer (Refer to the non-maskable interrupt sequence for more detail relating to the deadman timer). The contents of the monitor control register are under CPU/software control. The control bits have the following format:

Table 2-1 Control Bit Format

Data Bit	Control Bit Reference	Function
D0	MAPOUT	Remove vector memory from processor memory space.
D1	CHARMON	Enable the character monitor function.
D2	MASMON	Enables the master monitor function.
D3	CLRINT	Clears all pending interrupts by clearing monitor FIFO.
D4	INTALL	Forces vector memory bit VO=0, which generate interrupt for all characters.
D5	BUFOFF	Disables buffering by the SIO/2 DMA controller pair.
D6	DNMI	Disables DNMI non-maskable interrupt sequence.
D7	DDMT	Disables Deadman timer.

The monitor base register contains eight bits. Six of the bits (VM10-VM15) form the starting address of the 1K byte master slave communication area (MSCA). These bits are set by the master monitor and compared against the most significant six bits of the data link memory address (SA10-SA15). This comparison takes place during data link write operations to memory, to determine if the MSCA is being accessed. The remaining two bits (VM8-VM9), are used by the Character Monitor to select one-of-four 256 byte recognition tables of vector memory.

Addressing of vector memory is accomplished via multiplexers. This circuitry selects either memory address lines MA0-MA9 (in Master Monitor mode) or data lines BD0-BD7 and base register bits VM8, VM9 (in Character mode) to become the vector memory addresses.

Vector memory comprises two 1K by 4 bit static RAMS arranged as 1K eight bit bytes. Vector memory bits are referred to as V0-V7. If V0=0 of a given byte is set, then the location is activated as being a potential character vector. V7=0 activates a byte as being a master vector. Thus, a single vector memory location may be activated for both Character and Master Vectoring (V0 and V7=0). When a location of vector memory is read it is transferred to the monitor FIFO. Circuitry associated with this transfer, will indicate which monitor (character or master) caused the vector address and will set V7 (1 or 0) accordingly. V0 however, is loaded into the FIFO as 0, to assure that all interrupt service routine - program counters are aligned on halfword boundaries.

Up to 16 vectors may be held in the FIFO awaiting Z80A-CPU acknowledgement. In the event of a FIFO overflow, either a hex 00 or hex 80 vector will be deposited in the FIFO to indicate which monitor was the last to overflow. Refer to paragraph 2.2.3 for further discussion of vector (maskable), interrupt sequence.

2.2.3 Maskable Interrupt Sequence

The vector information contained in vector memory determines which memory events should generate interrupts. If an interrupt is enabled by the Z80A-CPU, the monitor FIFO will present the interrupt request, (generated via the character or master monitor, storing the vector in the monitor FIFO), and pass the interrupt vector to the Z80A-CPU during the time that interrupt acknowledge (INTA) is enabled low.

The Z80A-CPU will read the vector (placed on data lines D0-D7 by the FIFO) and merge it into its I Register (the vector byte becomes the low order address in the I register, whereas the high order byte already resides there). The CPU stores the program counter (PC) on the stack, then outputs the contents of its I register (containing both low and high order bytes) on the address bus to access the vector address table in memory. The contents of the location in the vector address table specified by the I register is then read by the CPU, placed in the PC, and used to access the interrupt service routine.

Once the interrupt service routine is completed, the old program counter is pulled from the stack and restored in the PC. Control is then passed to the interrupted program.

On DLP 128's, all interrupt sequences are steered to D space memory. When a maskable interrupt occurs, the acknowledge (MI/IORQ or INTA) signals, select page 1 of the decode PROM. All 256 locations of page 1 contain the same code which force the access to D space. See Paragraph 2.4, Memory Control Section, for more information on D space selection.

2.2.4 Non-Maskable Interrupt Sequence

For the TCB-1, DLP 64 and DLP 128, Non-Maskable Interrupts (NMI) may be caused by Memory Parity Errors (MPE) or a Deadman Timer (DMT) timeout. On a DLP 128, an additional source of a NMI is an Illegal PROM Address (IPA). Non-maskable interrupts of the DMT or IPA variety may be enabled or disabled via I/O commands (refer to Paragraph 2.2.2, Table 2-1, for reference to I/O commands enabled by data bits D6 and D7).

NMI's on DLP 128's force memory access to D-space. See Paragraph 2.4 for more detail regarding D space selection.

Whenever data is accessed from memory, the 8 data bits along with the memory parity bit are compared to determine that correct parity has been maintained. If an even number of 'one' bits are detected, then a MPE is generated. MPE's on a TCB-1 cause the TCB-1 to perform NOPs. This does not occur on a DLP 64 or a DLP 128.

The deadman timer prevents the communications line from "hanging up" in the event of a software or hardware failure. The deadman timer functions through I/O instructions.

Once enabled the deadman timer is reset by the system software at least every 0.5 seconds to prevent it from timing out. This timeout will produce a non-maskable interrupt.

Two control bits DNMI and DDMT enable or disable the timer functions and are linked with the monitor control register bits. The following conditions enable or disable the timer:

DNMI = 1	-	The Z80A-CPU will not be interrupted regardless of the state of the timer.
DNMI = 0	-	The Z80A-CPU will be unconditionally interrupted when the timer expires via a NMI. DNMI should only be set to one, disabling the NMI, before the DDMT is set to 1 - to disable the timer.
DDMT = 0	-	Setting DDMT to zero will start the timer function.
DDMT = 1	-	Stops the timer function.

On DLP 128's an Illegal PROM Address (IPA), will cause generation of a non-maskable interrupt. An IPA will occur if the second opcode of a dual opcode instruction is invalid or incorrect. A special code, Hex 40, is read out of the PROM and generates the (IPA).

DLP 64 and DLP 128 Controllers, have a second status register independent of the status register normally examined by a master OIS or VS system. This second status register is provided to allow the TC controller software to determine which NMI condition (MPE, DMT, IPA) produced the interrupt. The error condition is loaded into the status register at the time of NMI generation. The error handling routine may then examine the status register by executing an IN '71' (generates NMISTAT). A CLRSTAT command (Out '72') clears the register.

2.3 DATA LINK SECTION

The Data Link section, located on the daughterboard, comprises circuitry for instruction decoding, address selection, and error recovery and detection. The following paragraphs provide a block-level description of the 928 Data Link Section.

Receiver/Transmitter - The receiver/transmitter circuits, are responsible for the reception and transmission of data and control information between the TC controller and the OIS or VS master. This channel operates in a half duplex balanced mode, utilizing a high speed (4.275 Mbps) start/stop line discipline. This circuitry resides at location L19 and L40 on a DLP 64/128; L20 and L40 on a TCB-1.

Transmit Timing Control - The transmit timing control circuits, insure that data and control information sent to the master maintain the correct line discipline. This circuitry resides at location L17, L18, and L37 on a DLP 64/128; L18, L19, and L37 on a TCB-1.

Bit Synchronization - The bit synchronization circuits, synchronize the received bit stream bit by bit, insuring that the TC controller and the master are in synchronization. In addition to synchronizing, these circuits also "strip" the start, parity, and stop bits from the eleven bit transmitted character leaving only the eight bit data or control word. This circuitry resides at location L32, L11, L31, and L13 on a DLP 64/128; L32, L12, L31, and L14 on a TCB-1.

Character Synchronization - The character synchronization circuitry, synchronize the received data or control bit stream character by character, insuring that the controller and the master are in character synchronization. This circuitry resides at location L33 and L34.

Bit Shifter - The bit shifter, is responsible for converting the received serial bit stream into a parallel eight-bit bus and vice versa during transmit operations. This circuitry resides at location L87, L88 on a DLP 64/128; L83 and L82 on a TCB-1.

Instruction Decoder - The instruction decoder, is responsible for sampling the slave data bus information to validate a command or control words that may be present in the first byte of receive data. This circuitry will also decode the data or command word as a 1 byte or 256 byte read/write operation or a control command (restart, status). It also supplies input to the error detection and recovery section when illegal commands or control words are found. This circuitry resides at location L84 and L105 on a DLP 64/128; L100 and L101 on a TCB-1.

Error Detection/Recovery - The error detection/recovery circuits, are responsible for detecting character errors at the character synchronization or instruction decoder sections, and indicating these by setting the CPE (channel parity error) input to the slave status register. These circuits also contain logic to initialize error recovery by use of OPS (Operation Start) which restarts the slave data link channel. This circuitry resides at location L15, L58, L98 on a DLP 64/128; L16, L58, and L95 on a TCB-1.

Slave Status Register - The slave status register maintains a status of three slave conditions and the slaves device type. It maintains status of whether the slave is running (IPL), whether the slave is experiencing a memory parity error (MPE), or whether the slave is experiencing a data error in the form of a channel parity error (CPE). It resides at location L103 on a DLP 64/128; L81 on a TCB-1.

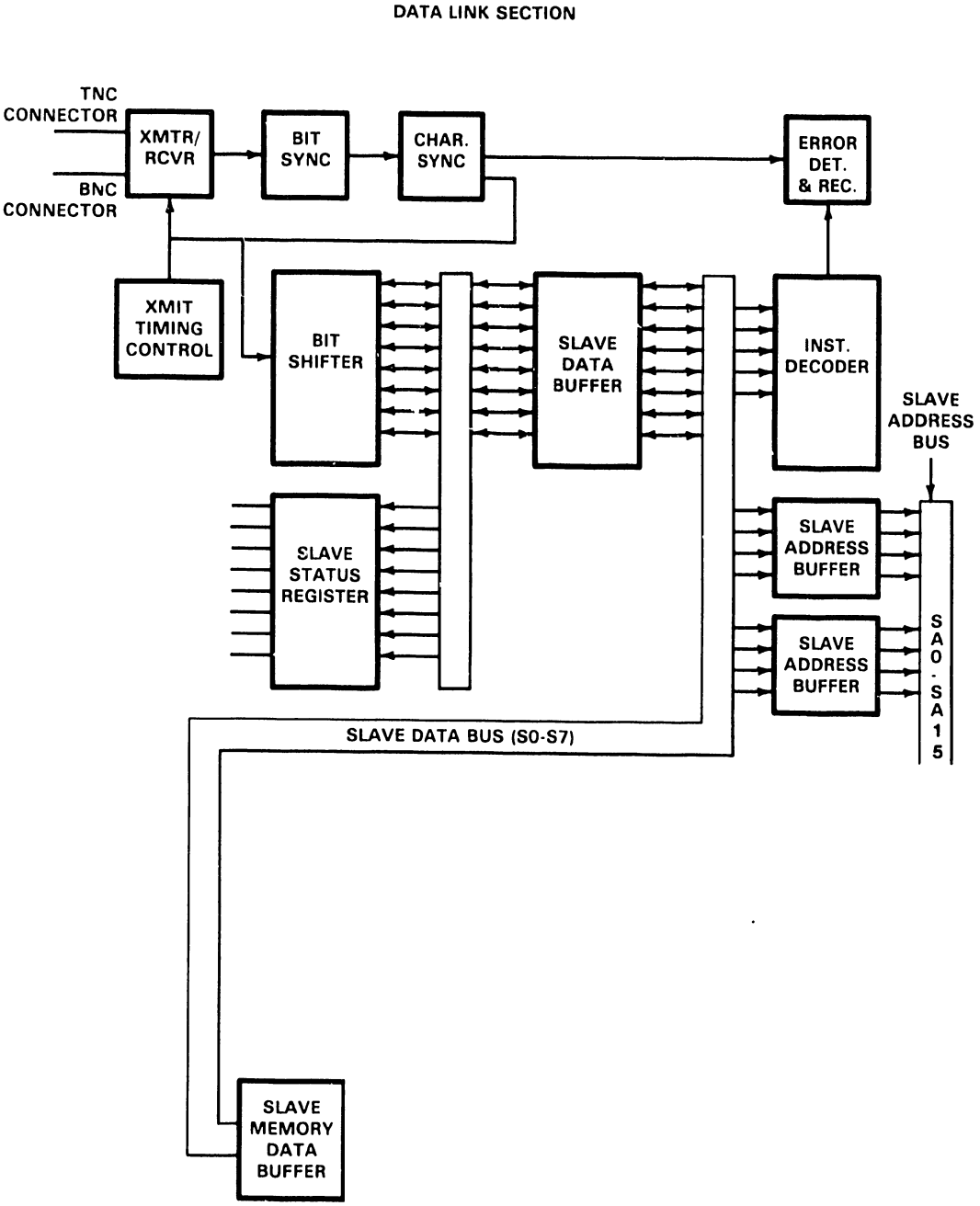


Figure 2-3 Data Link Block Diagram

2.3.1 Data Link Section Overview

The 928 Data Link Section consists of circuitry associated with interfacing an OIS Master/TCP or VS TCP, with slave data links. This is accomplished by transmitting and receiving control and data information, via a dual coaxial cable link, to and from the master associated with that TC controller.

The data link channel operates in a half-duplex mode utilizing a 4.275 Mb/s asynchronous line discipline. The line format consists of a start bit, eight data bits, a parity bit, and a stop bit. The 928 Data Link, under control of the master, can respond to two control commands and four memory access commands as described in Table 2-2.

Table 2-2 Data Link Commands

Command	Result
Restart	The Restart command instructs the 928 Data Link to Reset the processor; clear the IPL, memory parity error (MPE) lines and exit diagnostic mode.
Status	The Status command instructs the 928 Data Link to transmit the 928 Data Link and processor status, channel parity error (CPE), IPL, and memory parity error).
Read 1	The Read 1 command instructs the 928 Data Link to transmit one byte to the master, from the specified TC controller memory address.
Write 1	The Write 1 command instructs the 928 Data Link to receive one byte from the master and deposit it at the specified TC controller memory address.
Read 256	The Read 256 command instructs the 928 Data Link to transmit 256 bytes of data to the master starting at the specified 256 byte aligned address from the specified TC controller memory address.
Write 256	The Write 256 command instructs the 928 Data Link to receive 256 bytes of data from the master and deposit it at the specified 256 byte aligned TC controller memory address.

Control and data information transmitted by the master is received on the TC controller daughterboard, via dual coaxial cable, where the serial data stream is clocked into receiver circuitry. This data is then clocked into bit synchronization circuitry where it is checked for a valid start bit. This circuit checks for a valid start bit by sampling the serial data two times - 32ns apart to ensure that noise does not corrupt detection of the start bit.

Once the start bit is detected, the data from the master is counted and synchronized via the synchronization circuitry which also strips the start, stop and parity bits leaving eight data bits. Character synchronization is provided by character synchronization circuitry to ensure that character data is synchronized to the master. Data and control information that is sent to the master is controlled by transmit timing control circuitry that "turns the line around", disabling the receiver and enabling the transmitter.

After the data is counted and synchronized it is converted from serial to parallel via a bit shifter, and then sampled by instruction decoder circuitry (data selector/multiplexers) that decodes the data to determine if the data bits (first byte) constitute a valid instruction. If a command is invalid, an error will be flagged by the instruction error recovery circuitry and relayed to the status register.

At the same time that the data or control word (first byte) is decoded to determine if the instruction is valid, it is parallel loaded into a parity generator/checker and checked for valid parity. If a parity error is detected a channel parity error (CPE) will be routed to the instruction recovery circuit. Recovery circuitry will in turn relay this parity error to the status register. Refer to Paragraph 2.2.4, for more information relating to the non-maskable interrupt sequence.

A valid command or control word is clocked into the instruction decoder where the command or control word is decoded as a restart command, status command or a read or write (1 byte or 256 byte) command as described in Table 2-2.

After the instruction is decoded, the necessary timing for a slave memory request is generated via the memory timing control circuitry.

To process the instruction, i.e. a 256 byte write, the memory address has to be specified. This occurs upon receiving the second byte (high order address) and third byte (low order address) from the master. The high order address (byte two) is loaded into the slave high order register at B2 time. The slave low order register is loaded with the low order address (third byte) only if the instruction has been decoded as a one byte transfer (read or write). For a 256 byte transfer the slave low order register remains cleared (X '00') thereby forcing all 256 byte transfers to a 256 byte boundary.

The slave memory address (high and low registers) is buffered onto the memory address bus and clocked into the memory selection logic. A memory write or read is then performed depending on the original slave instruction.

If the master monitor has been enabled and the memory address selected is in the master/slave communication area (as it normally is), and the command is a memory write, then a vectored interrupt will be generated by the Master Monitor. Refer to Paragraph 2.2.2, for further information regarding the master monitor.

2.4 MEMORY CONTROL SECTION

The Memory Control Section, located on the daughterboard, monitors requests from the Data Link Section and the Processor Section on a round robin basis. Memory requests are either granted by a READY notification or pended by a WAIT notification, thus allowing processor and 928 data link access interleaving.

The Memory Control Section (see Figures 2-4 and 2-5), for all TC controllers comprise an address arbitrator and memory. Additional memory control circuitry for the DLP 64 and DLP 128, comprises an opcode latch, bit shifter, memory select logic, and opcode decode PROM (DLP 128 only).

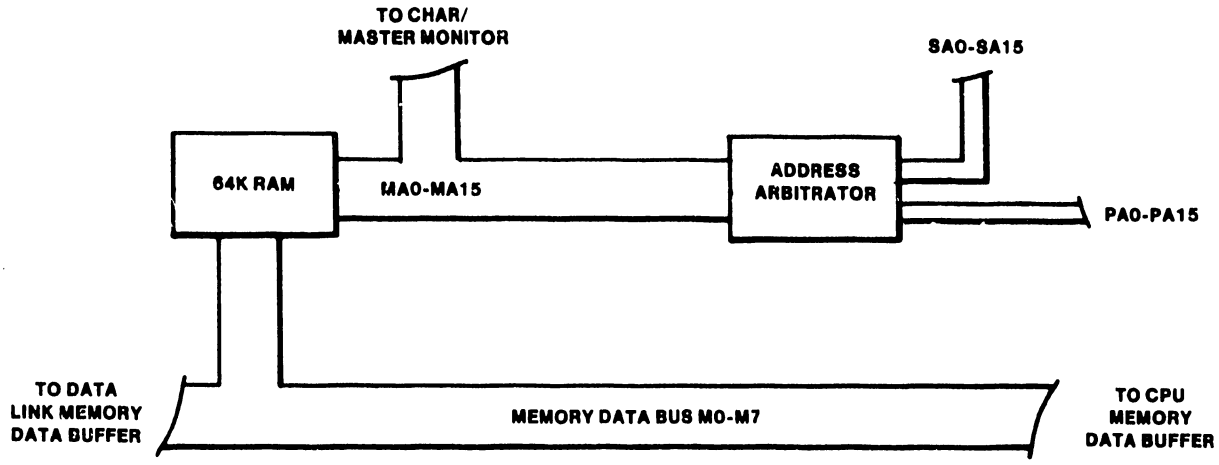


Figure 2-4 TCB-1 Memory Control Section

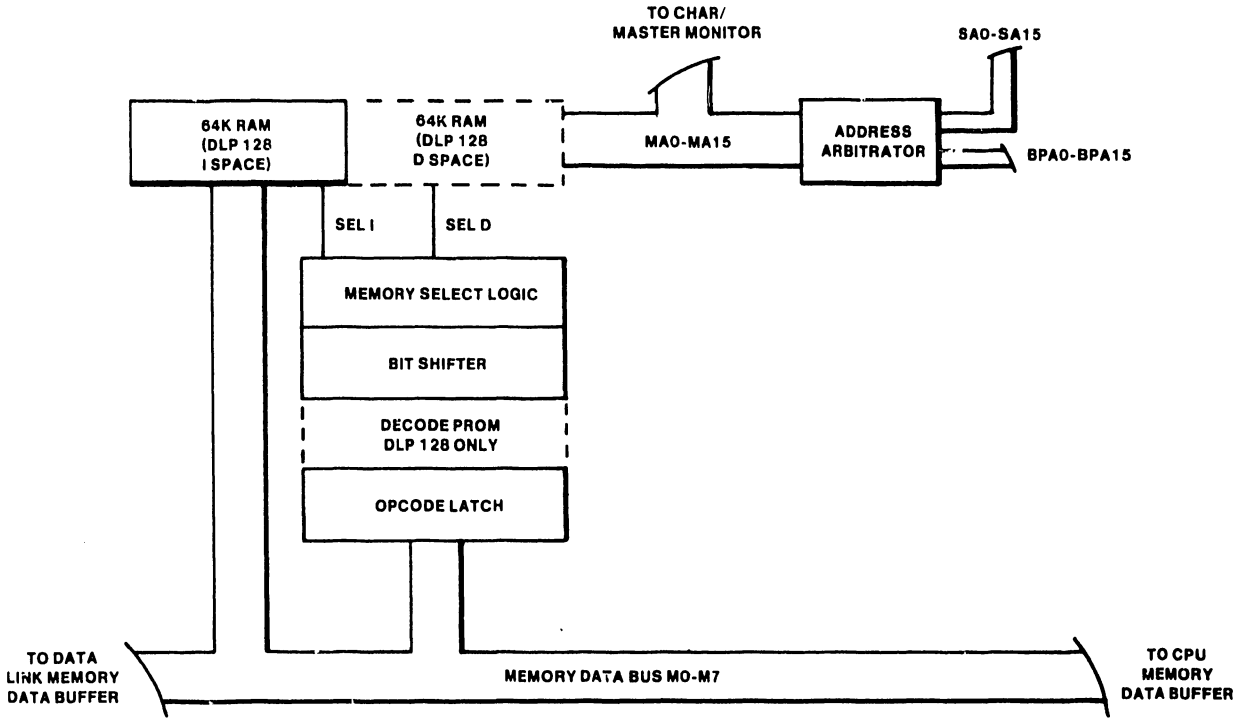


Figure 2-5 DLP 64/128 Memory Control Section

Address Arbitrator - The address arbitrator consisting of 4 multiplexor chips, selectively gates processor or data link address lines as inputs to row and column memory address latches. These chips reside at locations L50, L70, L90, L108 on a DLP 64 or DLP/128; L86, L87, L105, L106 on a TCB-1.

Memory - The memory of the TC controller contains all the controller operating software as well as buffers for communication data being transferred between a master OIS or VS system and the communication line. The memory is organized as 8 bit data bytes, with each byte having its own parity bit. Depending on the controller, the memory is either 64K or 128K bytes wide (see Figure 2-6). The TCB-1 uses 16K X 1 Dynamic RAMS to obtain the overall size requirement, whereas the DLP 64 and DLP 128, use 64K X 1 chips. Note that on the DLP 128, 128K is arranged in two 64K blocks referred to as I-Space and D-Space memory.

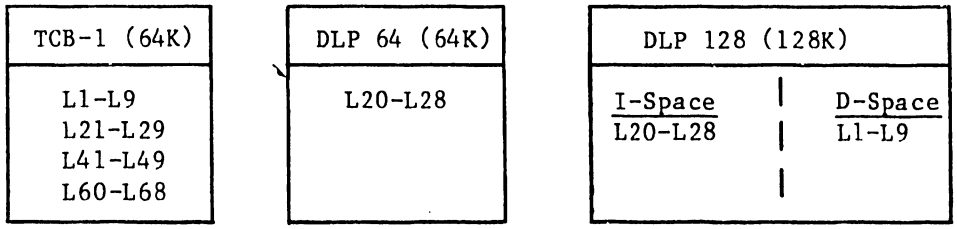


Figure 2-6 RAM Chip Layout

Opcode Latch (DLP 64/128 only) - This 8 bit D-type latch (L42), is loaded with an instruction opcode at the end of a Z80A-CPU opcode fetch cycle (M1). Its contents (opcode) are used to address the I/D PROM.

Bit Shifter (DLP 64/128 only) - The bit shifter, is a 4 bit shift register used to steer memory selection logic to either I-Space or D-Space. It is loaded at the end of a CPU M1 cycle with the low order 4 bits read from the I/D PROM. Each subsequent memory request shifts bits out (from the QD bar) providing a steering mechanism for the memory selection logic. The bit shifter resides at location (L44).

Memory Selection Logic (DLP 64/128 only) - The memory selection logic is responsible for generation of memory row address strobe pulses. One of two pulses may be generated - RASI or RASD which respectively select I-space or D-space for memory access. Major portions of this circuitry reside at locations L64, L47, L48, L66-L68 and L49.

Decode PROM (DLP 128 only) - The decode PROM is a 2K X 8 PROM contained on the daughterboard. The decode PROM is divided into eight pages with each page consisting of 256 bytes. Address election within a page is provided by the output of an opcode latch (L42). Decode PROM page selection is accomplished via PROM address lines A8-A10, which are outputs of a D-type latch (L45).

The decode PROM outputs a code that is used as follows. Bits zero to three of this code is routed to the bit shifter for use as a steering mechanism for I space and D space memory accesses. Bits four, five and seven are routed to L45 and contain code for changing the page accessed in decode PROM. Accessing another page in decode PROM would be typical of an instruction that requires two opcode fetches. Bit six is tested by the hardware to determine if an illegal PROM address (IPA), has been accessed. The decode PROM code is used for generation of maskable and non-maskable interrupts, dual M1 cycle instructions, etc. Decode PROM resides at location (L41).

The codes contained in the decode PROM are derived by examining each Z80A instruction and deciding where the next operation after the opcode fetch is to take place (I space or D space).

2.4.1 Memory Control Section Overview

Controller memory access is granted on a priority basis. The 928 Data Link section has the highest priority while the CPU and DMA respectively have the next lower priorities. Memory address arbitration is controlled by the signal SADRS which, by its state (0 or 1) selects either data link memory addresses (SA0-SA15), or processor (CPU/RAM) memory addresses (PA0 - PA15), to be gated to the memory address lines MA0 - MA15. These (MA0 - MA15) lines in turn are used to form row (RAS) and column (CAS) addresses.

2.4.1.1 TCB-1 Memory

TCB-1 memory is laid out as 4 banks with each bank having 9 16K X 1 DRAMS (M0 - M7, MP). Bank selection is provided by decoding address lines MA14 and MA15. Address lines MA0 - MA13 form row and column addresses.

2.4.1.2 DLP 64/128 Memory

The DLP 64 and DLP 128 contain 64K bytes and 128K bytes of memory respectively. Each use 64K X 1 DRAMs, to meet their respective size allocations. The DLP 128 memory is arranged in two 64K blocks referred to as I-space (instructions), and D-space (data).

The DLP 64 and DLP 128, have added memory control circuitry not available on the TCB-1. On the DLP 64 this circuitry is not used. This is due to communication software, designed for the TCB-1 and carried over for use on DLP 64-based systems, not having the added instructions required to exercise the added DLP hardware. there ·re, the remainder of this discussion will relate to the DLP 128, with DLP 64 exceptions noted as required.

I space contains the software instruction code for the DLP 128, as well as the 1k Master/Slave Communication area address ('0000'-'03FF'). D space contains variables, pointers, tables, and the stack. D space addresses ('0000'-03FF"), (the MSCA equivalent) cannot be accessed.

DLP 128 memory selection logic can operate in three software selectable modes:

1.	I Mode	All memory operations access I space. The DLP 64/128, will default to I mode after any reset (the DLP 64 remains in I mode due to lack of software necessary to change the mode.
2.	D Mode	All memory operations access D space.
3.	I/D Mode	Both I space and D space are utilized. Control circuitry selects the appropriate memory selection circuitry for each selection.

When I/D mode is selected, the opcode latch, along with certain memory selection circuitry is enabled. At the start of a Z80A-CPU instruction fetch (M1 cycle), I space selection is forced by the memory selection circuitry. The opcode is read from memory by the Z80A-CPU and simultaneously applied to the input of the opcode latch. The opcode is loaded into the latch at the end of the M1 request, and provides an address to page 0 of the decode PROM.

At the end of the M1 cycle, the four low order bits of the PROM, output a code that is loaded into a bit shifter. Each subsequent memory request shifts a bit out of the register providing a steering mechanism for the memory selection logic. Every time a '0' is shifted out, D space is enabled (RAS D generation). If a '1' is shifted out, I space is enabled (RAS I generation).

If the instruction requires two opcode fetches the PROM code addressed by the first opcode is used to change the selected PROM page. The new PROM page address is formed via the output of the D type latch.

The second opcode is fetched and addresses the new PROM page which then outputs the appropriate code to the 4-bit - parallel shift register. This sets up selection of I or D space memory as explained above.

Not all 256 Hex combinations (00-FF) are valid for the second opcode. If the second opcode is invalid a special code (Hex 40), is read out of the PROM and generates an illegal PROM address (IPA). This error along with a memory parity error and a deadman timer error will generate a non - maskable interrupt NMI. Refer to Paragraph 2.2.4, for more information relating to the non-maskable interrupt sequence.

CHAPTER 3 OPERATION

Chapter 3
OPERATING INFORMATION

3.1 INTRODUCTION

Chapter 3, provides detail relating to the operation and functional use of the TCB-1, DLP 64 and DLP 128 TC Controllers.

When equipped with a TC Controller, the OIS Master/TCP or VS TCP, requires a new front panel and a rear panel interface connector - the type depending on the interface(s) supported. The front panel LEDS enable monitoring of the interface signals that provide status information during normal operation. Refer to Paragraphs 3.3, 3.4 and 3.5, for more detail regarding front panel LED status indicators.

3.2 TC CONTROLLER SOFTWARE SUPPORT

The following paragraphs describe the software packages supported by the TCB-1, DLP 64 and DLP 128 Controllers. Typical system configurations and the required protocol support are also provided. See Table 1-2, for reference to documentation that provides more detailed information regarding protocol use and installation.

The TCB-1	Remote Wangnet (Wang Systems Networking) on OIS, Alliance, and VS Systems; 3270 on OIS and Alliance Systems.
The DLP 64	Remote Wangnet (WSN) on OIS, Alliance and VS Systems; 3270 on OIS and Alliance Systems; SNA on VS Systems.
The DLP 128	SNA on OIS and Alliance Systems; Teletex on OIS, Alliance and VS Systems.

3.2.1 3270 Emulation

When configured to operate with a TCB-1 or DLP 64 TC Controller running 3270 Emulation Software, an OIS master appears (emulates) to a host to be a remotely located 3271 Control Unit while OIS workstations emulate the 3277 Display Station and 3288 Printer. In this configuration the host controls the emulated control unit which in turn controls the emulated devices. A BISYNC polling protocol is employed and intended for use over a multi-point leased line which supports up to 32 control units. Each control unit may support up to 32 devices.

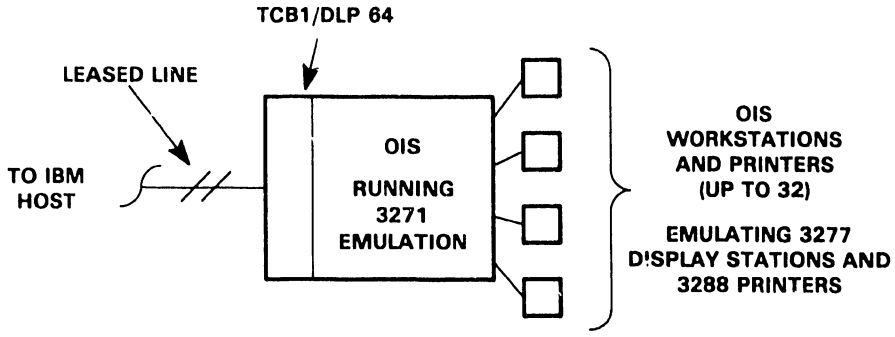


Figure 3-1 3270 Emulation Operation

3.2.2 Asynchronous Operation

When equipped with communication software that emulates Teletype (TTY), an OIS System can send a document to, or receive a document from, another OIS or a non-Wang system that supports the same protocol, in a leased-line or dial-up-line environment. TTY emulation software also provides a limited batch capabilty by allowing an entire document to be sent and received by a Wang or non-Wang Systems.

Since asynchronous protocols are traditionally interactive in nature, emulation software operates in the foreground through a workstation that is dedicated to sending and receiving information while the communications activity is in process. When communication occurs through a system based TC controller (DLP-64), the activity take place in the background allowing workstations to perform other functions.

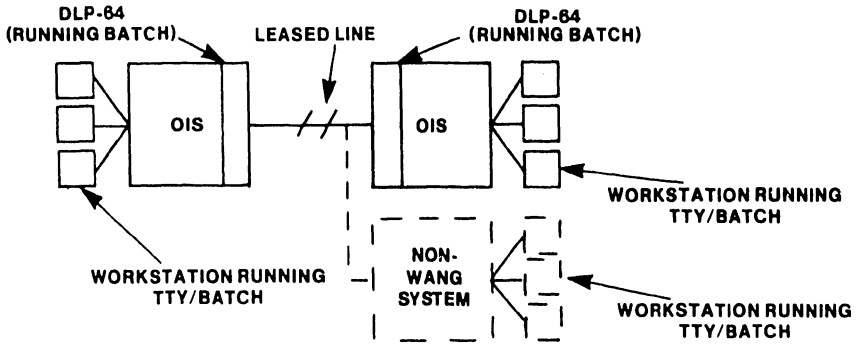


Figure 3-2 Asynchronous/Bisynchronous Operation

3.2.3 Bisynchronous Operation

Communication between two OIS Systems, and with non-Wang Systems, is supported by software that emulates IBM 2780 and 3780 Bisynchronous protocols. The Wang WPS program, is intended for batch communication between two OIS-Systems that support IBM 2780 or 3780, in a point-to-point, half-duplex, bisynchronous environment via a leased or dial-up network. WPS enables transfer of files and libraries between two OIS Systems.

Batch 2780/3780 Emulation Software, allows for batch communications with non-Wang Systems. Batch emulation software supports point-to-point, half-duplex, Bisynchronous communication over leased, or switched (dial-up) networks. Emulation Software allows VS data files or libraries, to be transmitted to other systems and workstations that support 2780 or 3780 protocols. Batch emulation software may operate in foreground mode through a workstation that is dedicated to sending and receiving information while the communications activity is in process. When communication occurs through a system based TC controller (DLP-64), the activity take place in the background allowing workstations to perform other functions (Figure 3-2).

3.2.4 Remote Wangnet (WSN)

Using Remote Wangnet (WSN) software a VS System host is currently capable of sending a document or file to, or receiving a document or file from, a remotely located OIS System and an OIS Workstation is capable of remotely logging on to the VS host in a dedicated or leased line environment (point to point or multi-point) as shown in Figures 3-3 and 3-4. Present releases include VS to VS, OIS to OIS configurations. The TCB-1 or DLP 64, operating with Remote Wangnet (WSN) enables the VS System host to send and receive a document or file to and from several OIS Systems (Nodes) concurrently to provide paths for file transfer and log-on services for each.

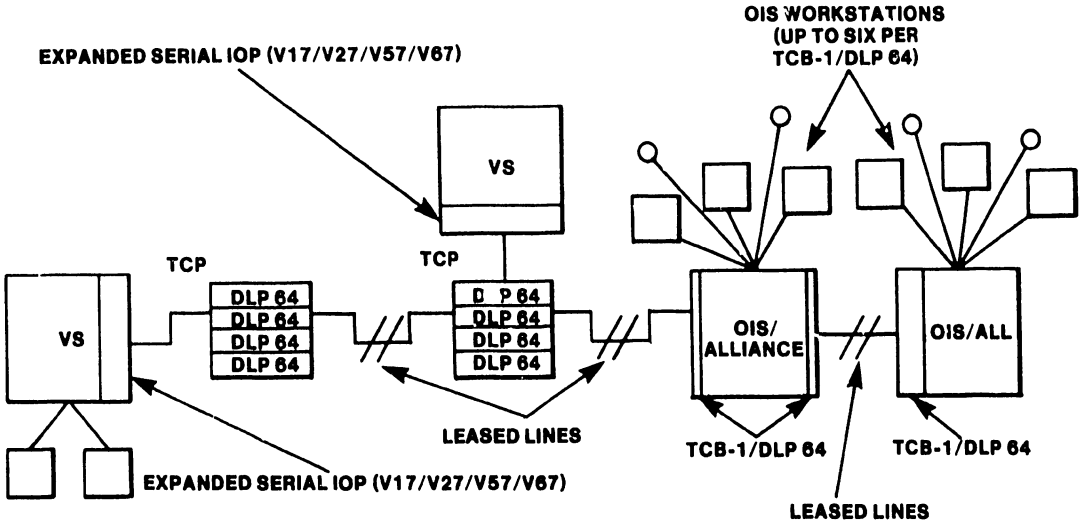


Figure 3-3 Remote Wangnet (WSN) Point-to-Point

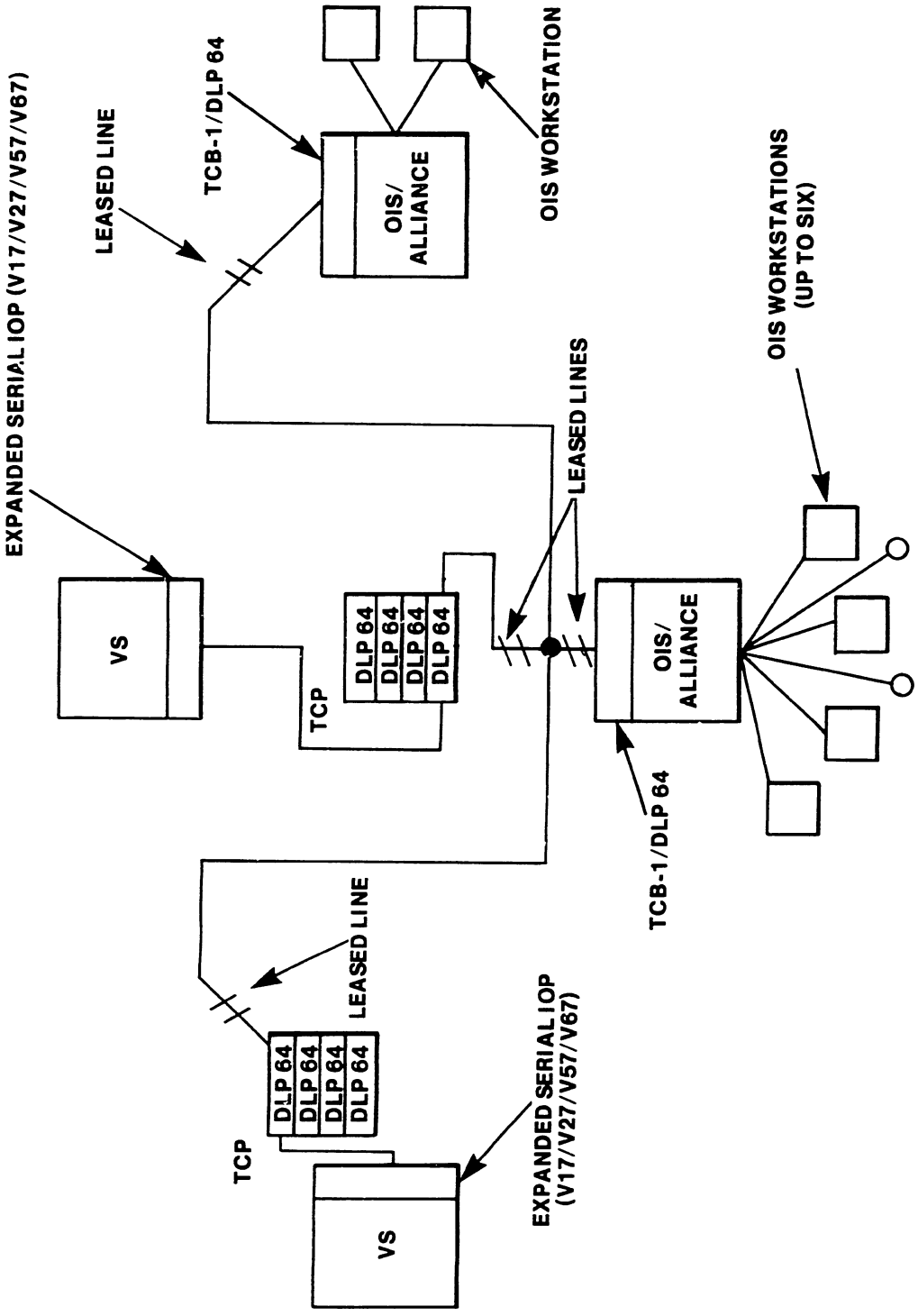


Figure 3-4 Remote Wangnet (WSN) Multi-Point Operation

3.2.5 SNA

When an OIS or VS (system master) is operating with 3274 emulation software, an OIS based DLP 128 Controller or a DLP 64 Controller housed in a TCP, will provide users with interactive access to applications run from an IBM host. Emulation software will support both physical and virtual workstations as well as multiple printers. The emulation runs as an SNA multiple logical unit supporting concurrent data streams to and from the host. By implementing Synchronous Data Link Control (SDLC) line protocol, system master logical devices will communicate at speeds up to 9600 bits per second. Emulation software (3274), communicates in half-duplex mode with a host computer that supports 3274 Cluster Controllers, with up to 32 terminals or printers (3278 Display Stations and 3288 Printers).

When operating with 3777 Emulation software a VS master can access an IBM hosts batch processing capability operating in the SNA format employing SDLC line protocol. The system master SNA emulator can communicate in half-duplex mode with an IBM host over multi-point lines using IBM compatible EBCDIC transmission code. The 3777 emulator, supports up to six concurrent data streams to and from host logical units.

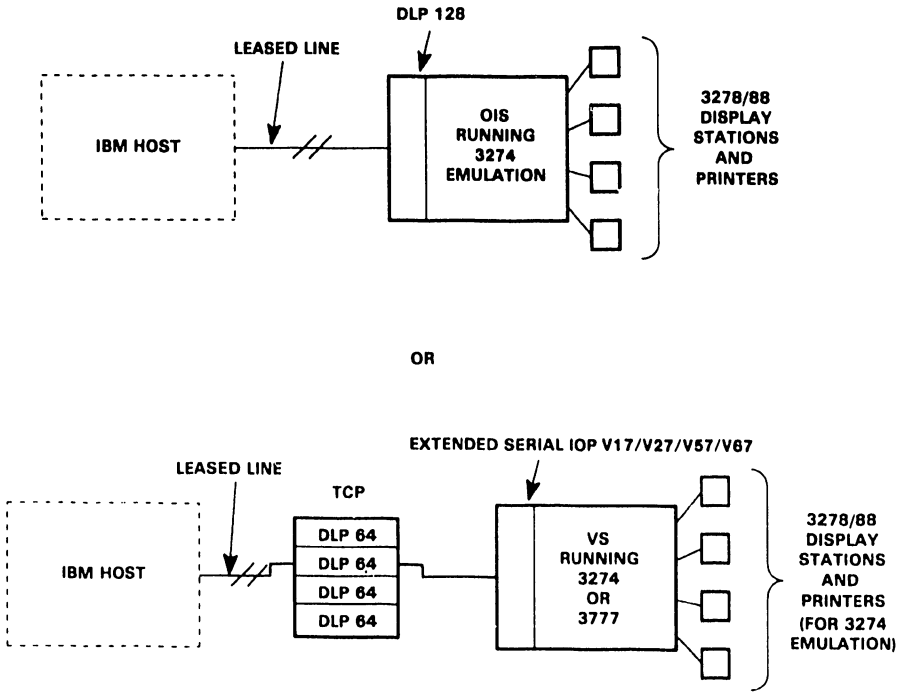


Figure 3-5 SNA 3274/3777 Emulation

3.2.6 Teletex

Teletex service employs a standard specified by the CCITT as a high speed replacement for Telex. The Teletex service as implemented allows a document to be created and printed locally and then printed with full error checking to any other Teletex terminal.

NOTE
When installing Teletex software the workstation date and time option and TCP modification are required.

The OIS Teletex terminal facility will provide any Wang user with the capability of exchanging correspondence (Teletex document) with other Teletex (Wang or Vendor System) via public data networks.

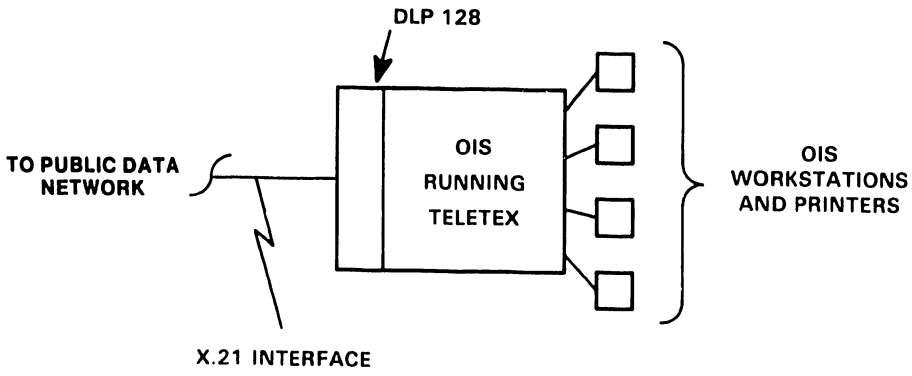


Figure 3-6 Teletex Operation

3.3 OIS 3270 EMULATION FRONT PANEL LED INDICATORS

During normal operation the eight TC front panel LEDS indicate the presence of interface signals. The eighth LED is a D.C. power indicator. The following table describes the LED indicators of an OIS System when running 3270 Emulation Software.

Table 3-1 OIS 3270 Front Panels LEDS

LED Indication	Description
1-Receive Data	Rapidly flashing LED indicates transitions between ones and zeroes representing serially encoded characters received by data communications equipment (DCE) from a remote DTE.
2-Transmit Data	Rapidly flashing LED indicates transitions between ones and zeroes representing serially encoded characters generated by the data terminal equipment (DTE).
3-Clear to Send	LED on indication generated by the DCE to indicate whether or not the data set is transmit enabled.
4-Request to Send	LED on indication generated by the data terminal to condition the local DCE for data transmission.
5-Data Carrier Detect	LED on indication generated by the DCE indicating that data transmission from the remote data set to the DTE is enabled.
6-Data Terminal Detected	LED on indication generated by the DTE used to control switching of the DCE to the communication channel.
7-Data Set Ready	LED on indication generated by DCE indicates that the DCE is capable of transmitting and receiving data signals.
8-Power Indicator	On during normal operation.

3.4 REMOTE WANGNET (WSN) FRONT PANEL LED INDICATORS

The following paragraphs provide reference to the status of LED indicators used to monitor interface signals when running Remote Wangnet Emulation Software. On an OIS, interface signals are monitored from the TC front panel or the TCP front panel. On a VS, interface signals are monitored from the TCP front panel LED's. LED's four and five on OIS Systems differ in Table 3-2.

Table 3-2 Remote Wangnet (WSN) LED Status Indicators

LED Indication	Description
1-System Activity	In normal operation LED #1 will blink several times per second to indicate that microcode has been loaded; and in the absence of other lights, the system is waiting for a line to come up. If the LED is flashing slowly, it indicates that a large amount of message traffic is being processed and that the message traffic requires compression.
2-Received Valid Data	This LED indicates that a message frame was received without a CRC error. Each time a message is received, the LED will invert its state. That is, if the LED is on, it will then turn off when a subsequent message is received.
3-Transmitter Active	When asserted this LED indicates that the transmitter is currently in the process of transmitting a frame on the line. The off state indicates that the transmitter is not active.
4-Data Carrier Signal Detected (VS Systems, TCP)	This LED is asserted when a remote (secondary) system is actively transmitting transmit data.
4-Data Carrier Signal Detected (OIS Systems, TCP)	This LED asserts to indicate that both the local and primary modems are capable of transmitting and receiving data. If modems are not in use and the LED asserts, then it is an indication that the VS Primary software is operating.
5-Virtual Circuit Active	This LED indicates that at least one virtual circuit has been established. As an example, it may indicate that a user has logged on or attempted to log onto the VS, or that a batch file manager is active. This LED may also indicate that a workstation is using a TC controller prior to it being IPL'ed as part of the control functions menu.

Remote Wangnet (WSN) LED Status Indicators (cont,d)

6-Activity to OIS/VS	This LED asserts when the TC controller is in the process of talking to the local host.
7-TC Controller Refusing New Traffic	This LED asserts when the controller has more traffic that it can handle. Additional messages will be refused.
8-Diagnostic Mode	This LED when asserted indicates normal operation of the TC controller. If blinking the controller is in diagnostic mode.
TC Controller Idle	A single light rotating on the TCB-1 from left to right, indicates that the controller is idle and may be loaded by the control menu and initialized.

3.5 TELETEX FRONT PANEL LED INDICATORS

The following table provides reference to the status of LED indicators used to monitor interface signals when running Teletex Terminal Facility Software. On an OIS, interface signals are monitored from the TC front panel or a TCP front panel. On a VS, interface signals are monitored from the TCP front panel LEDs.

Table 3-3 Teletex Front Panel LED Indicators

LED Indication	Description
1-Document Received	When on this LED indicates that a document was received or partly received (at least six sectors worth). LED stays on until the log file is purged.
2-Receive Memory Full	When on the LED indicates that memory is full or near full. Near full being within 4K bytes of capacity.
5-Transmitting Document	This LED blinks as a document is being transmitted.
6-Receiving Document	This LED blinks as a document is being received.

Teletex Front Panel LED Indicators (cont'd)

7-Blink on Signal Scanning	This LED blinks at a three second rate to indicate that the operating system code is still active.
8-Power	This LED is on during normal operation, and blinks for a hardware problem or a fatal software error.

3.6 INTERFACE STANDARDS

Refer to Appendix A for a description of the interface standards supported by the TCB-1, DLP 64 and DLP 128.

CHAPTER 4

INSTAL-LATION

CHAPTER 4
INSTALLATION

4.1 INTRODUCTION

This chapter provides procedures to unpack, inspect, install and verify the correct operation of the TCB-1, DLP64, and DLP128 TC Controllers.

4.2 UNPACKING AND INSPECTION

Before unpacking the TC Controller, perform a careful visual inspection of the shipping carton for any indication of possible damage. The following address should be used to notify Wang of such damage:

Wang Distribution Center
Dept #90
Quality Assurance Department
Tewksbury, MA, 01876

Unpack the TC Controller as shown in Figure 4-1. Open the shipping carton along the edges to prevent damage to the TC Controller. Save the carton and shipping material for use in the event that reshipment is necessary.

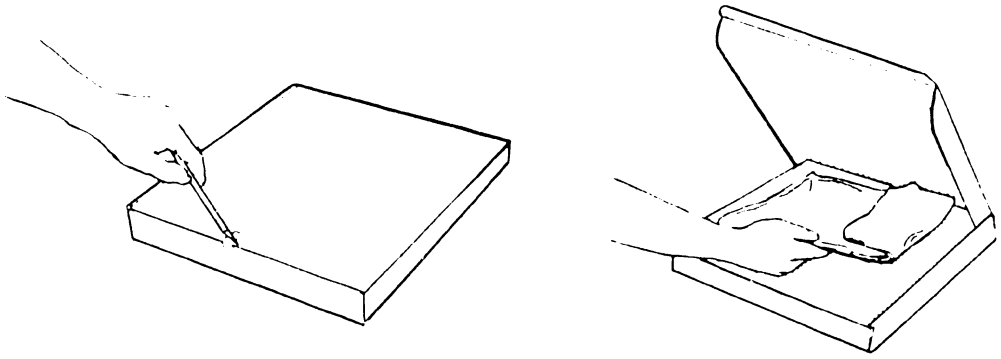


Figure 4-1 Unpacking The TC Controller

4.3 SWITCH SETTINGS

Prior to installing a TCB-1, DLP 64, or DLP 128, switch banks SW1 (OIS line address/VS null modem bit rate) and SW2 (OIS device type) must be set. These switch banks are located on the controller motherboard (see Figure 4-2). On some TC controllers, the individual switches comprising switch banks SW1 and SW2 are labeled "CLOSED" and "OPEN" which correspond to "ON" and "OFF".

4.3.1 OIS Switch Bank SW1 Switch Settings

When used on an OIS master, switches 1, 2, 3, and 4 of switch bank SW1 (location L75) identify the TC controllers line address in hex (1-F). Switches 5, 6, and 7 identify the TC controllers configuration. Switch 8 ON selects diagnostic loopback testing (OFF for normal operation).

OIS batch TC requires that each TC Controller have a unique line address. The line address specified by switch bank SW1 will correspond to the "Connection Line Address" set via the "Edit A Connection Menu" (see the OIS TC User's guide for information concerning OIS menus). Line 01 on the "Edit A Connection Menu" corresponds to Hex 11 on SW1 (for a TCB-1/DLP64 without X.21); line 03 corresponds to Hex 13 (for a TCB-1/DLP64 without X.21). It is recommended that only odd addresses be used in order to conform to the convention established by the WP/OIS TCB product line. In this convention, controllers utilize odd addresses and workstations use even addresses.

OIS 140 class systems may accept up to two TC controllers internally, with each having its own unique line address in the range of (1 to F) hex. Recommended switchbank SW1 settings for the first TC controller are provided in Table 4-1. Refer to Table 4-2 for recommended SW1 switch settings for a second TC controller. OIS 3270 software does not look at switch bank SW1; however, it is recommended that the individual switches of switch bank SW1 be set as indicated. It will save time later if Batch TC is added to the OIS system.

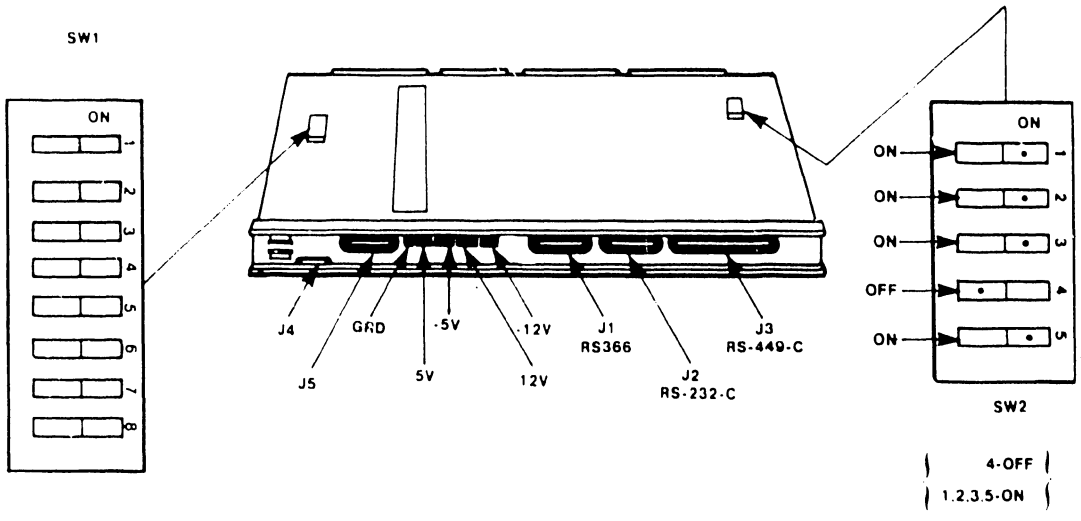


Figure 4-2 Line Address And Device Address Switch Settings

Table 4-1 Switch Bank SW1 Switch Settings (First TC Controller)

	8	7	6	5	4	3	2	1
TCB-1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
DLP-64 (Without X.21)	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
DLP-128 (Without X.21)	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
DLP-64 (With X.21)	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
DLP-128 (With X.21)	OFF	ON	ON	ON	OFF	OFF	OFF	ON

Table 4-2 Switch Bank SW1 Switch Settings (Second TC Controller)

	8	7	6	5	4	3	2	1
TCB-1	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
DLP-64 (Without X.21)	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
DLP-128 (Without X.21)	OFF	OFF	ON	ON	OFF	OFF	ON	ON
DLP-64 (With X.21)	OFF	ON	OFF	ON	OFF	OFF	ON	ON
DLP-128 (With X.21)	OFF	ON	ON	ON	OFF	OFF	ON	ON

4.3.2 OIS Switch Bank SW2 Switch Settings

Switch bank SW2 (location L101) is used to identify this controller as a TC device type. Switches 1, 2, 3, 4, and 5 of switch bank SW2 should be set as follows for each TC controller installed in the master unit:

1=ON, 2=ON, 3=ON, 4=OFF, 5=ON

4.3.3 VS Leased Line Modem Operation

The following switch settings apply to TCP based VS Systems equipped for leased line modem operation

When using a leased-line modem, set SW1 (1 through 4) OFF, and set switch 5 ON.

Table 4-3 Switch Bank SW1 Switch Settings (Leased Line Modem Operation)

	8	7	6	5	4	3	2	1
TCB-1	OFF	OFF	OFF	ON				
DLP-64 (Without X.21)	OFF	OFF	OFF	ON				
DLP-128 (Without X.21)	OFF	OFF	ON	ON			OFF	
DLP-64 (With X.21)	OFF	ON	OFF	ON				
DLP-128 (With X.21)	OFF	ON	ON	ON				

4.3.4 Switch Settings For VS Null Modem Operation

Refer to Table 4-4, for switch settings when a null modem is used as the interface connection for VS System support (TCP). Switches 1 and 2 of switch bank SW1 select the null modem clock speed. All other switches of switch banks SW1 and SW2 should be set as previously indicated.

Table 4-4 Null Modem Switch Settings

Switch Bank SW1		Null Modem Clock
Switch 2	Switch 1	
ON	ON	4800
ON	OFF	9600
OFF	ON	19200
OFF	OFF	64000 (Not Supported)

4.4 INSTALLATION REQUIREMENTS (140/145 Masters)

The following parts list provides reference to assemblies that are needed to install a TC controller in a 140/145 Master. The hardware necessary to complete the installation is listed under each assembly that is underscored.

NOTE
Optional assemblies are marked with an asterisk

Part Description	Part Number
140 Front Panel	270-0628
Lamp Board with a 2 row LED display	210-7665
Lamp Panel Cable	220-3171
One Channel Rear Cable Panel	270-0865
BNC/TNC Cable	220-1648
32" Dual Coaxial Cable	220-0270
Two Channel Rear Panel*	270-0866
Requires two each of the assemblies listed One Channel Rear Cable Panel	
RS-232-C Internal Cable Assembly*	279-0557
RS-232-C Flat Cable	220-3129
Modem Cable	220-0332
RS-366 Internal Cable Assembly*	279-0558
RS-366 Flat Cable	220-3174
Modem Cable	220-0332
X.21 Cable Assembly*	289-0191
X.21 Interface Board	210-7951
X.21 Flat Cable	220-3223
X.21 Adapter Plate	452-0274
Modem Cable	220-0274

The following TC Controller configurations are available based on system requirements:

TCB-1 Controller*	212-3014
CPU Motherboard	210-7763A
Data Link & Memory Board	210-7762A
DLP64 Controller*	212-3040
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-1A
or	
DLP128 Controller*	212-3038
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-A

4.4.1 Top Cover Removal

Perform the following procedure to remove the top cover of the OIS 140/145 master unit (refer to Figure 4-3).

CAUTION

Power down the master unit and disconnect the ac plug before installing or removing any PCBs or internal assemblies

1. Remove the machine screw at the rear of the main chassis. This screw is used to secure the top cover to the main chassis.

2. Push the cover to the rear of the unit to disengage the tab on the front edge of the cover from the front of the main chassis.

3. Lift the cover up and away from the main chassis.

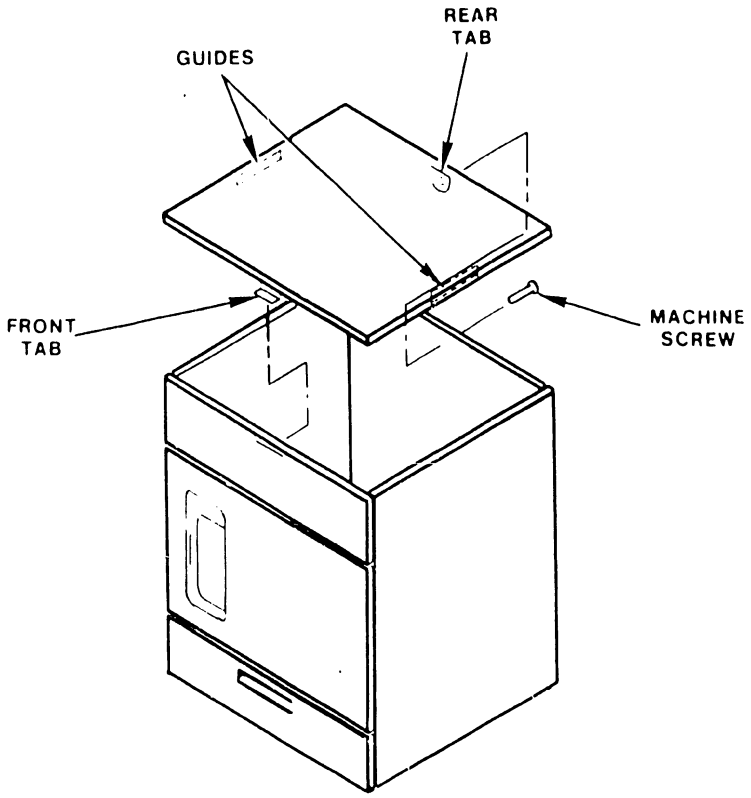


Figure 4-3 Top Cover Removal/Installation

4.4.2 140 Upper Front Panel Removal

To install the TC controller, the upper front panel must be replaced with a 140 front panel consisting of a lamp board with a two-row LED display. Perform the following procedure to remove the existing front panel.

4.4.2.1 Upper Front Panel Removal

1. Lift the panel upward to disengage its four tabs from the slots on the chassis bracket (Figure 4-4).

2. Pull the panel away from the unit.

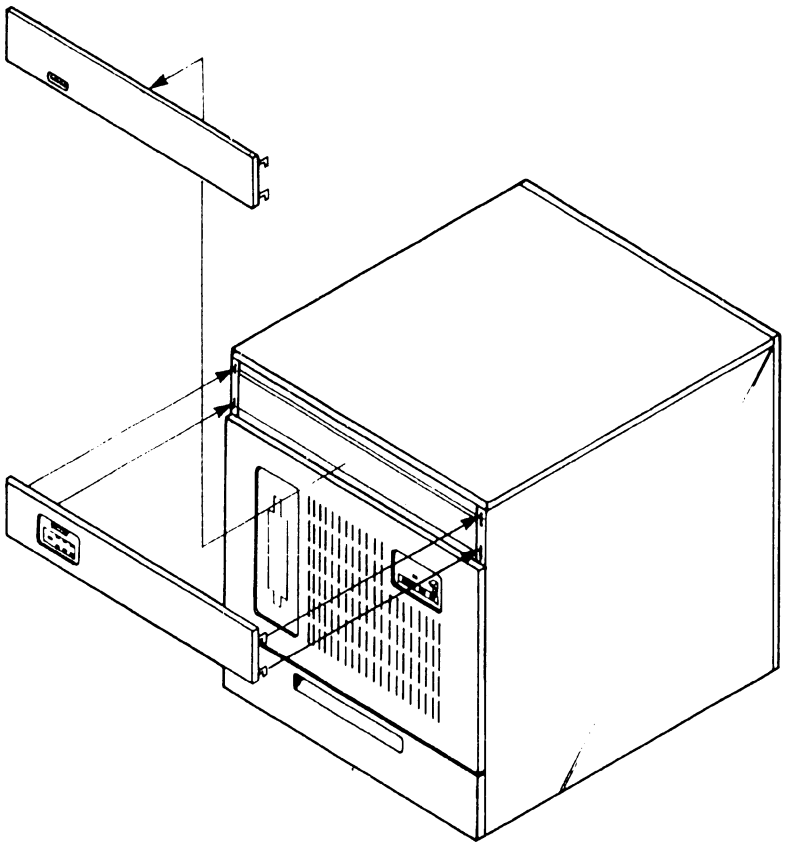


Figure 4-4 Upper Front Panel Removal/Installation

4.4.2.2 New OIS 140/145 Front Panel Installation

The lamp board on the new OIS 140/145 front panel is electrically connected to the TC controller via a Lamp Board Cable (P/N 220-3171). This cable has a socket connector at one end and an edge connector at the other end. Refer to Figure 4-5.

1. Remove the two screws that secure the board retainer to the chassis.

2. Use the removed screws to secure the two new ground lugs (supplied with the new front panel) to the chassis bracket.

3. Connect the two grounding cables (part of new front panel) to the ground lugs.

NOTE

Before plugging the socket connector into connector J1, ensure that socket pin one is properly aligned with connector pin one.

4. Plug the socket connector end of the lamp board cable(s) into the J1 connector on the TC lamp board of the new front panel. Plug in the socket connector of the second cable if two TC controllers are being installed.

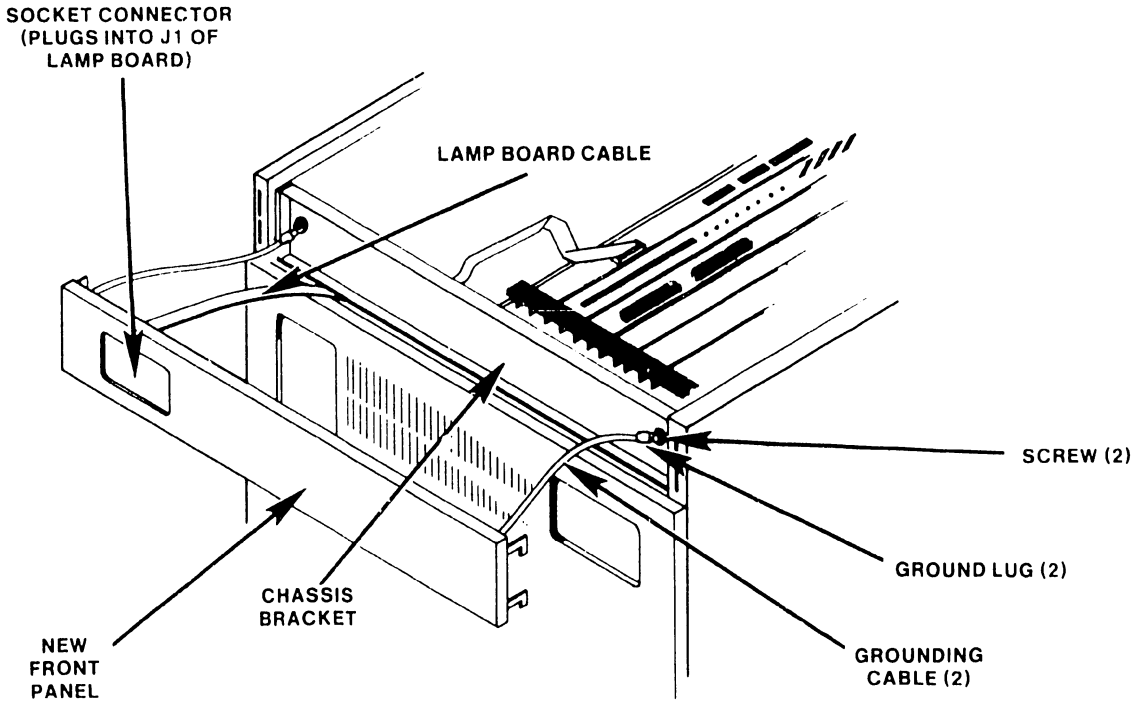


Figure 4-5 New OIS 140/145 Front Panel Installation

5. Route the edge connector end of the lamp board cable(s) through the slot in the side of the U-Chassis (see Figure 4-6). Position the cable for connection to the TC controller as described later in this manual.

6. Install the new 140 Front Panel (P/N 210-0628) by engaging its four tabs in the chassis bracket.

4.4.3 PC Guide Block Installation

On older 140 Class masters it may be possible to install a TC controller backwards into the motherboard. To prevent this, a special PC Guide Block (P/N 449-0314) may be installed. The PC Guide Block should be installed the first time the motherboard is removed for maintenance purposes. All 140/145 Masters manufactured since late 1981 should have this guide block installed.

The parts required to install the PC guide block into a 140/145 Master for one TC controller are listed in Table 4-5. The installation procedure is described below.

Table 4-5 PC Guide Block Installation

Part Description	Quantity	Part No.
PC Guide Block	1	449-0314
Spacer	1	462-0120
Flat-head Screw, 4-40 by 3/4"	1	650-2241
Nylon Washer, #4	1	653-2010
Nut, 4-40	1	652-2000

1. As shown in Figure 4-6 (A view), loosen the two board retainers screws.

2. Note the connecting arrangement of all cables that interface the PCBs. Remove all cables from the PCBs.

3. Note the location of and remove all PCBs from the motherboard.

4. Remove the motherboard (refer to the OIS 140/145 Manual, P/N 729-0664-A).

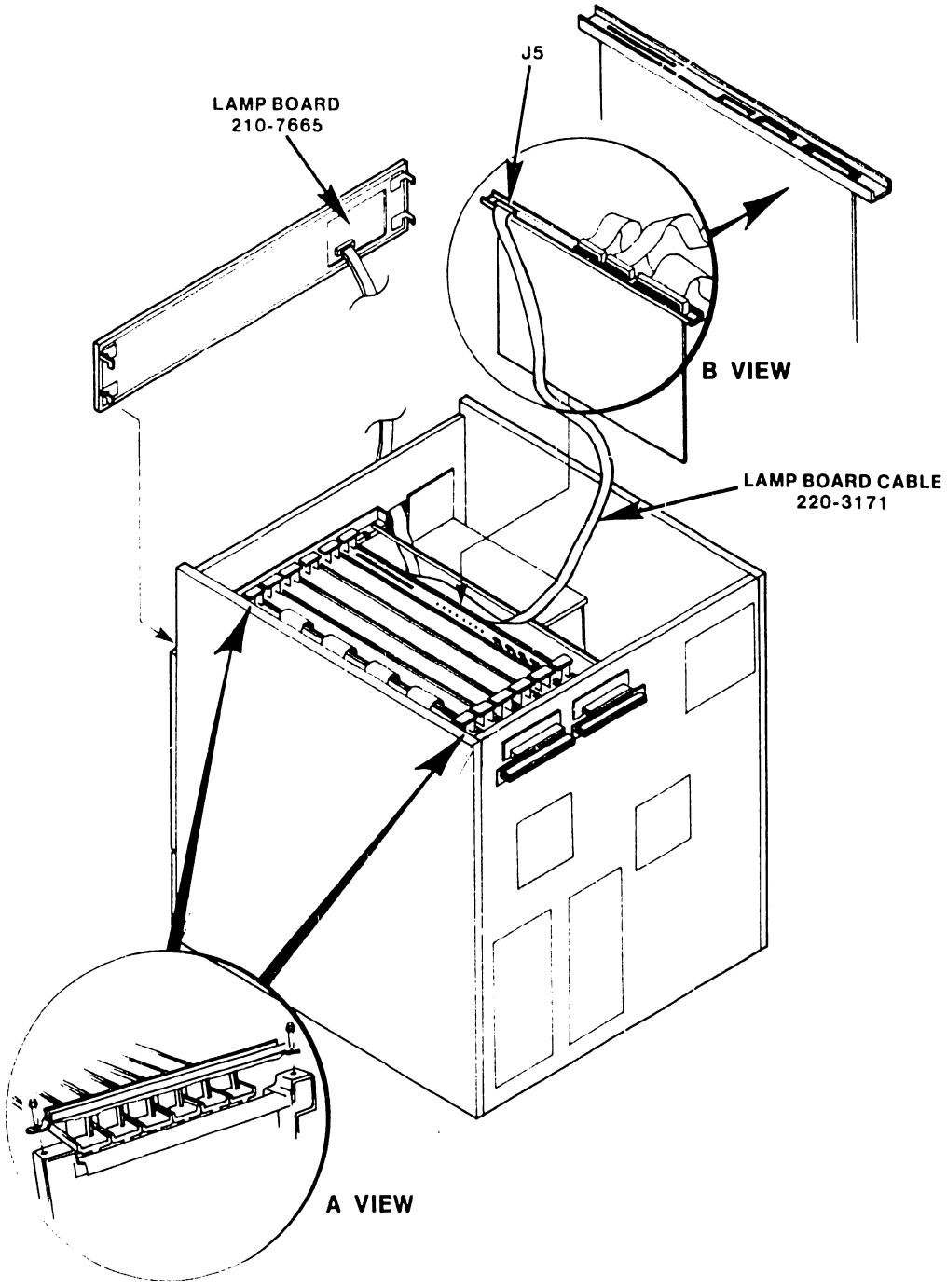


Figure 4-6 TC Controller Installation (140/145 Masters)

5. Two Phillips-head screws secure connector J13 (identified as connector number 1 on some 140/145 Masters) to the motherboard. Remove the rearmost screw from the connector as shown in Figure 4-7.

NOTE

This screw must be removed to allow clearance to install the PC guide block

6. Place the spacer into the center indented hole, located on the bottom side of the PC guide block (there are two indented center holes, either one can be used).

7. Align the center screw hole (with spacer), with the screw hole located directly behind connector J13 (or connector #1) on the motherboard. Insert the 3/4 in. flat head screw through the center hole and spacer on the guide block. Secure the block to the motherboard using the nylon washer and nut.

8. Reinstall the motherboard per OIS 140/145 Manual, 729-0664-A.

9. Install PCBs into their correct locations in the motherboard.

10. Do not install the two board retainers and do not connect any cables until the TC controller(s) are installed.

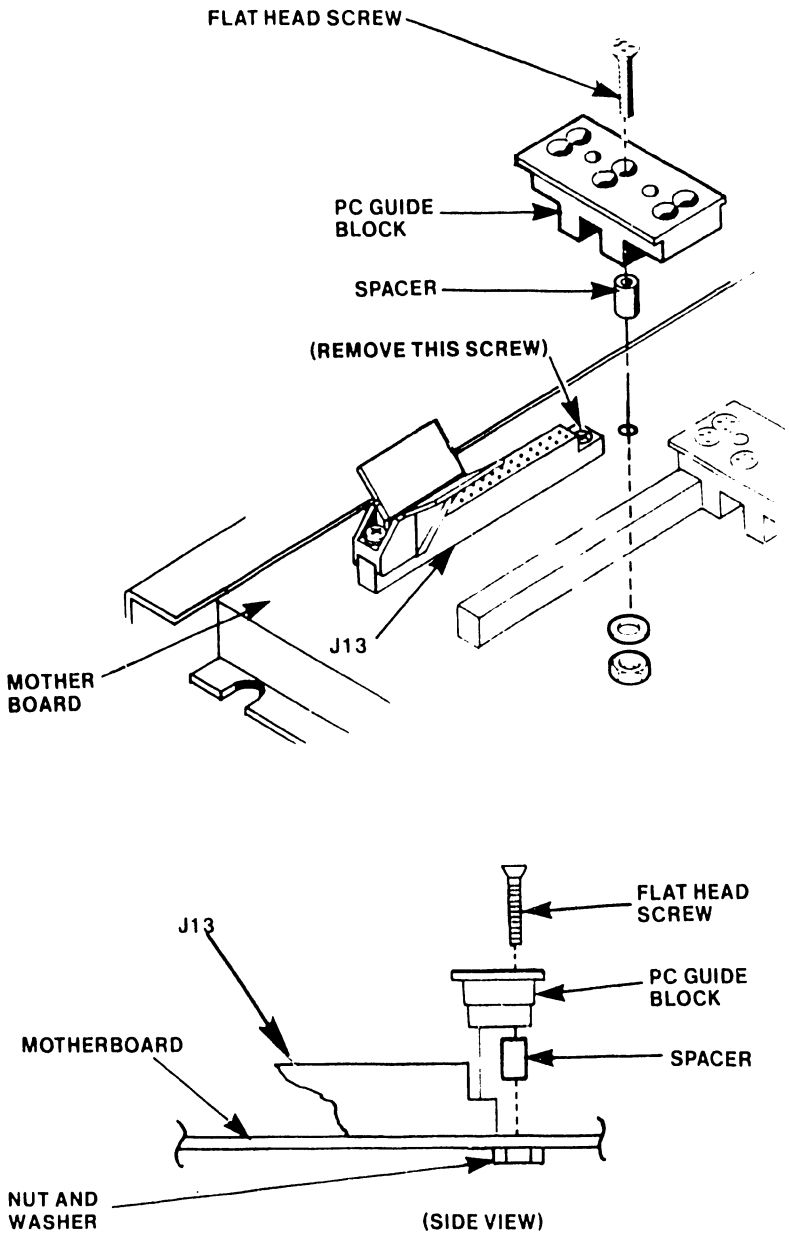


Figure 4-7 PC Guide Block Installation (140/145 Masters)

4.4.4 TC Controller(s) PCB Installation (140/145 Masters)

This section describes the installation of either one or two (maximum), TC controllers into a OIS 140/145 Master. Some early 140/145 Systems were designed to accept only one TC controller. In order to install a second TC controller into one of these early 140/145 Masters, a new Motherboard (P/N 210-7507) with one additional I/O slot must first be installed (refer to the OIS 140/145 Manual, 729-0664-A). The procedure for TC controller installation is as follows:

1. Refer to Paragraph 4.3, to verify TC controller switch settings.

2. Install the TC controller(s) into the I/O slot(s) furthest to the right, when viewing the unit from the back (see Figure 4-6). The board connectors on the motherboard have card guides to ease insertion, and card keys to center the boards.

3. Seat the TC controller board(s) by pushing down firmly on the board handles.

4. Secure the TC controller. Check for a clearance of approximately 1/32" between the TC controller and the rack.

5. Plug the edge connector end of the TC Lamp Panel Cable (P/N 220-3171) into connector J5 on the TC controller mounting bracket (see Figure 4-6, B View).

5. Install all cables previously removed.

4.4.5 Rear Cover Plate Removal/TC Rear Panel Installation

Three edge connectors (RS-232-C, RS-449, and RS-366 interfaces), a 4-pin BNC/TNC interface connector and an edge connector for the TC front panel, are located on the rail of the TC controller PCB. To route and connect the appropriate interface cables to these connectors from outside the master, the existing rear cover plate must be replaced by a TC rear cable panel.

Two versions of the TC rear panel are available on 140 Master Units. The first, a 1-channel TC rear panel allows for connection of one TC controller to a modem. The second version, a 2-channel TC rear panel allows for connection of two TC controllers. As installation procedures are similar for both versions, only the 1-channel TC rear panel installation is discussed.

NOTE

Some early 140/145 Systems are designed to accept only one TC controller. Later units have a motherboard with one additional I/O slot which enables the 140/145 to accept two TC controllers. As a result, early 140/145 Systems require a 1-Channel TC Rear Panel (P/N 270-0629). At a later date, a new motherboard along with a 2-channel TC Rear Panel (P/N 270-0630) may be installed for two channel capability.

With the introduction of the DLP64 and DLP128 to the OIS TC product line, a change was made to the TC rear panel configuration. Previously a TC rear panel was shipped from manufacturing with three interface connectors (RS-232-C, RS-366, RS-449). Beginning in the spring of 1983, a customer must specify the interface option they wish to use (RS-232-C, RS-366, RS-449/X.21).

Refer to Installation Requirements (Paragraph 4.5), to obtain the part numbers of the cables and other items required for use with RS-232-C, RS-366 and X.21 options. If the RS-366 ACU option is being installed, both of the following interface cables are required:

RS-366 Flat Cable (1 each)	P/N 220-3174
RS-232 Flat Cable (1 each)	P/N 220-3129

4.4.5.1 Rear Cover Plate Removal

Remove the existing rear plate by loosening four machine screws that secure it to the rear of the master unit. Pull the rear cover plate away from the unit (Figure 4-8).

4.4.5.2 RS-232-C or RS-366 Interface Cable Installation

Perform the following steps to secure the RS-232-C or RS-366 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-9 (internal side of rear cable panel).

2. Remove the panel insert corresponding to the cable option supplied (e.g. RS-232-C).

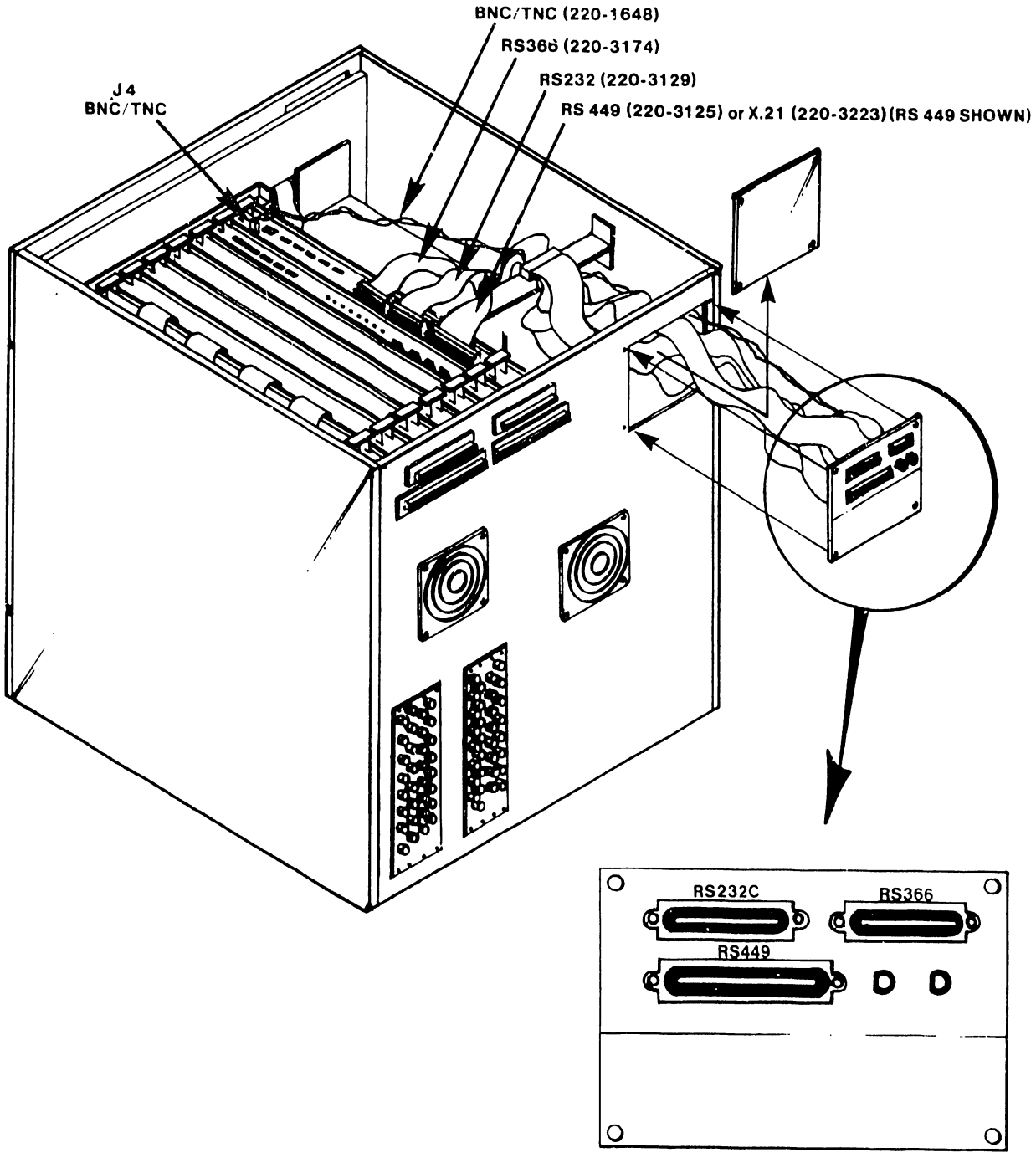


Figure 4-8 Rear Cover Plate Removal/TC Rear Panel Installation (140/145)

3. Align the cable "D" connector behind the panel slot from which the insert was removed in step 2. Position the connector such that the long edge of the "D" connector is on top (see Figure 4-9, view A).

4. Insert two threaded standoffs (P/N 478-0791) through the TC rear panel screw holes.

5. Install the red wire ground lug on one standoff and a washer on the other standoff (Figure 4-9).

6. Secure the "D" connector to the TC rear panel using two 4-40 nuts.

7. Repeat steps 2 through 6 if a second cable is installed (as with the RS-366 option).

8. Proceed to Paragraph 4.4.5.4, to install the TC rear panel.

4.4.5.3 X.21 Interface Cable Installation

Perform the following steps to secure the X.21 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-10 (internal side of rear panel).

2. Remove the panel insert covering the RS-449 slot.

3. Fit the X.21 cable "D" connector to the adapter plate. Make certain that the long edge of the "D" connector is on top (Figure 4-10).

4. Insert two threaded standoffs (P/N 478-0791) through the X.21 adapter plate (P/N 452-0274) and "D" connector screw holes. Ensure pemnuts on adapter plate are facing as shown in Figure 4-10.

5. Install the red wire ground lug on one standoff and a washer on the other standoff (Figure 4-10).

6. Secure the "D" connector to the X.21 adapter plate using two 4-40 nuts.

7. Secure the X.21 adapter plate to the TC rear panel using two 4-40 screws. Insert these two screws through the panel and thread them into the two pemnuts on the adapter plate.

8. Proceed to Paragraph 4.4.5.4, to install the TC rear panel.

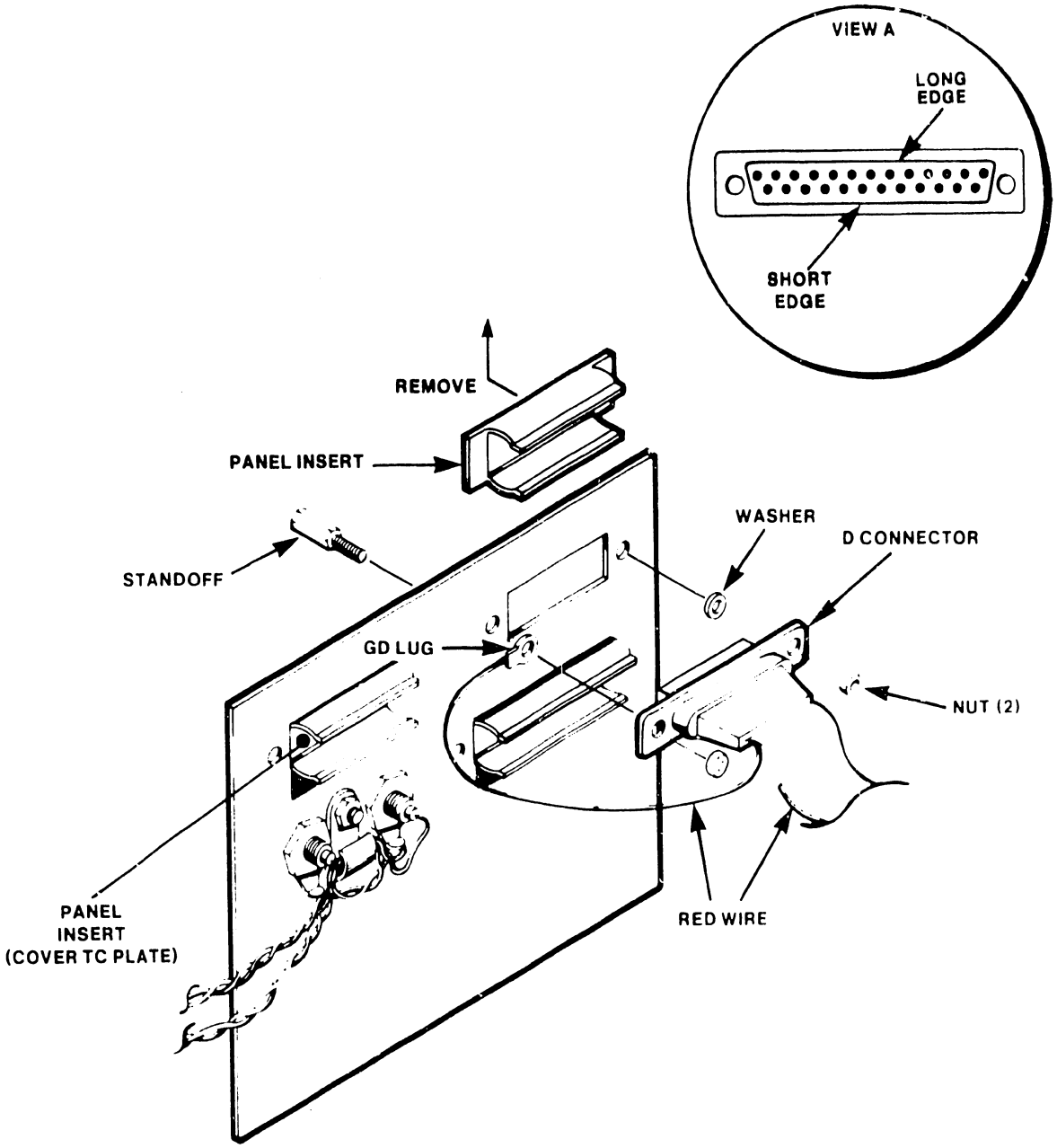


Figure 4-9 RS-232-C or RS-366 Interface Cable Installation
(Installed from inner side of TC rear panel)

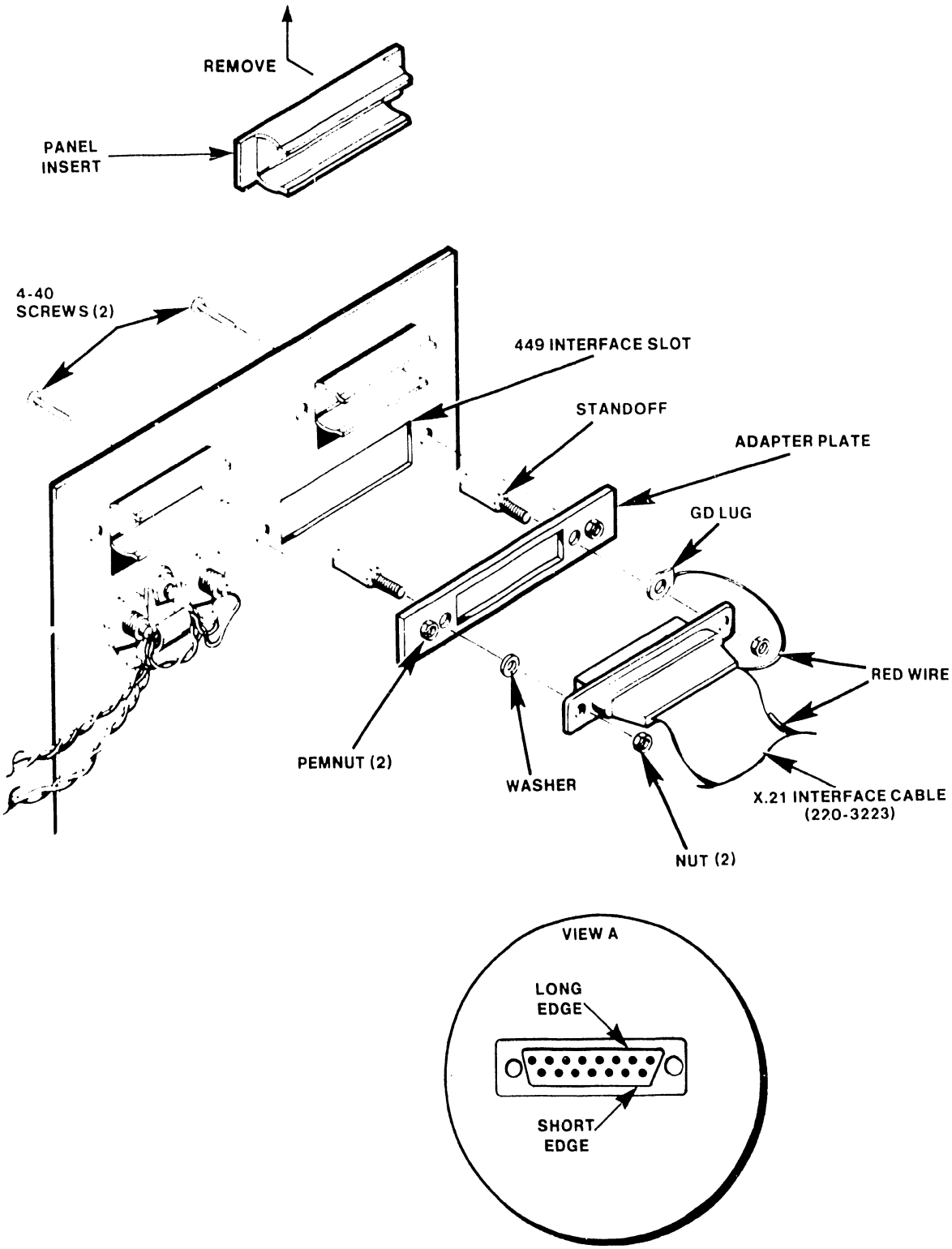


Figure 4-10 X.21 Cable To Panel Installation (Internal side)

4.4.5.4 TC Rear Panel Installation

Perform the following procedure to secure the TC rear panel to the master rear panel. Before performing this procedure ensure that the following cables are present or have been installed on the TC rear panel:

BNC/TNC connector cable (internal)
One or two 20-inch flat interface cables.

1. Route the one or two 20-inch flat interface cables and the BNC/TNC connector cable (not the 32" external cable), through the opening created by the removal of the rear cover plate (Figure 4-8).

2. Use the four machine screws removed from the rear cover plate to secure the TC rear cable panel to the rear of the master unit. Proceed to step 6 if not installing the X.21 interface.

3. Carefully insert the X.21 DIP connector into J2 of the X.21 Adapter Board (P/N 210-7951) as shown in Figure 4-11. Ensure pin alignment.

4. Connect the X.21 adapter board to the RS-449 connector (J3) of the TC controller as shown in Figure 4-11.

5. Proceed to step 7.

6. Connect the 20-inch interface flat cable(s) to the corresponding connector on the rail of the TC controller PCB - (RS-232-C, RS-366, or RS-449) as shown in Figure 4-2. Once the interface cable(s) have been connected, secure them to the U-chassis using the flat cable clamp (P/N 654-1318).

7. Note the key orientation and plug the 4-pin BNC/TNC cable connector from the TC rear panel into connector J4 located on the rail of the TC controller PCB. The BNC/TNC Cable is held into position by a snap-in clamp and should set flush on top of the TC controller.

8. Connect the 32-inch dual coaxial cable from the BNC/TNC connectors on the external side of the TC rear panel to any dual connector port on the rear of the master unit.

4.4.6 Top Cover Installation

1. As shown in Figure 4-3, position the top cover over the OIS 140/145 Master Unit cabinet.

2. Align the cover guides with the main chassis.

3. Lower the cover and push it forward such that the front tab on the cover engages the front of the main chassis. Make sure the rear tab is between the main chassis and the outside of the master unit cabinet.

4. Secure the top cover by installing the machine screw through the hole in the Master cabinet, through the hole in the rear tab, and into the main chassis.

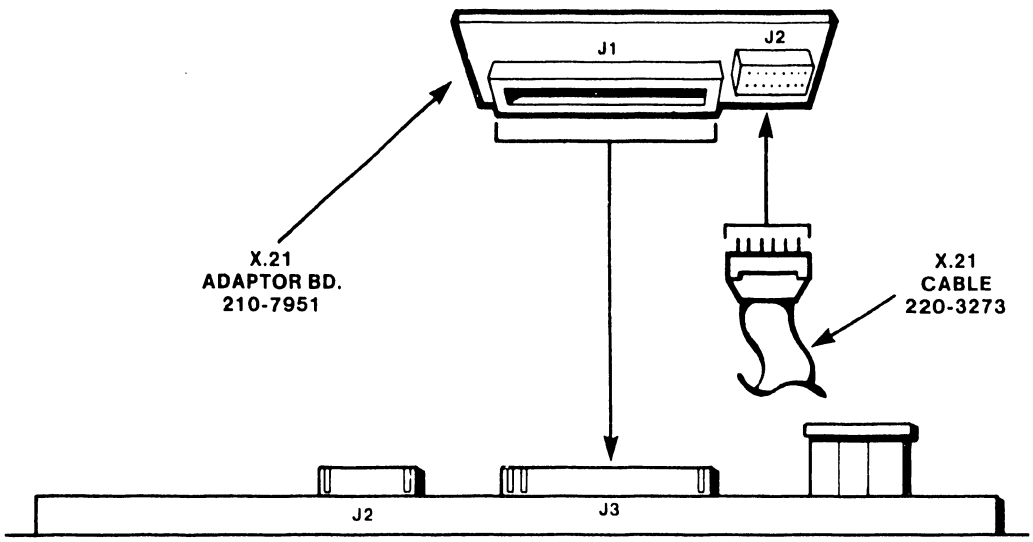


Figure 4-11 X.21 Interface Adaptor Board Installation

4.5 INSTALLATION REQUIREMENTS (105/115/125A/130A) MASTERS

The following parts list provides reference to assemblies that are needed to install a TC controller into a 105/115/125A/130A Master. The hardware necessary to complete the installation is listed under each assembly that is underscored.

NOTE
Optional assemblies are marked with an asterisk

Part Description	Part Number
Front Panel	270-0632
Lamp Board with a 1 row LED display	210-7865
Lamp Panel Cable	220-3171
Rear Cable Panel	270-0867
BNC/TNC Cable	220-1648
18-Inch Dual Coaxial Cable	220-0225
RS 232-C Internal Cable Assembly*	279-0557
RS-232-C Flat Cable	220-3129
Modem Cable	220-0332
RS-366 Internal Cable Assembly*	279-0558
RS-366 Flat Cable	220-3174
Modem Cable	220-0332
X.21 Cable Assembly*	289-0191
X.21 Interface Bd	210-7951
X.21 Flat Cable	220-3223
X.21 Adapter plate	452-0274
Modem Cable	220-0274

The following TC Controller configurations are available based on system requirements:

TCB-1 Controller*	212-3014
CPU Motherboard	210-7763A
Data Link & Memory Board	210-7762A
DLP64 Controller*	212-3040
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-1A
or	
DLP128 Controller*	212-3038
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-A

CAUTION
Remove AC power from master before proceeding

4.5.1 Top Cover Removal

Eight Phillips screws secure the top cover of the master unit: three at each side and two at the rear (Figure 4-12).

1. Remove the two Phillips-head screws at the rear of the chassis.
2. Remove the three Phillips-head screws at each side of the chassis.
3. Slide the cover forward and lift off.

4.5.2 Floppy Diskette Drive Removal

When installing a TC controller into an OIS 105/115/125A/130A Master, the existing TC type front panel must be replaced with a new front panel. To replace the front panel assembly, the diskette drive unit must first be removed.

The diskette drive unit is mounted on a base plate that contains front and rear guides which fit into corresponding slots on the master chassis. The entire unit is secured by a captive hold-down screw. The removal procedure is as follows.

1. Slide the ribbon cable out of its retainer.
2. Disengage the captive hold-down screw (see Figure 4-13A).
3. Firmly grasp the diskette drive by its front panel and slide it forward until it is halfway out of the cabinet.
4. Disconnect the AC power cord and the I/O ribbon-cable-connector PCB assembly at the rear of the diskette drive unit (see Figure 4-13B).
5. Pull the diskette drive out from the master.

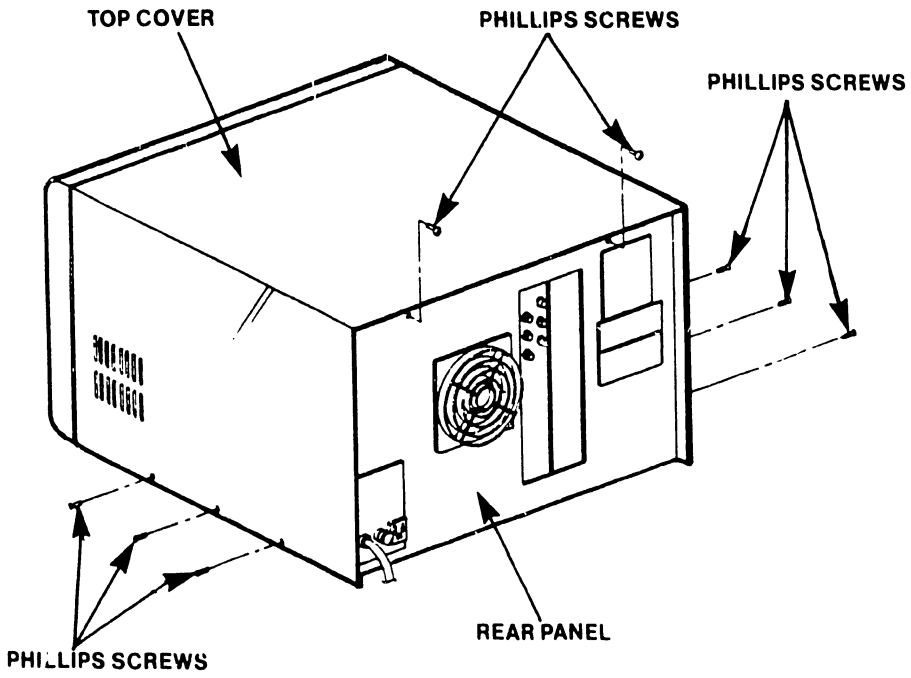
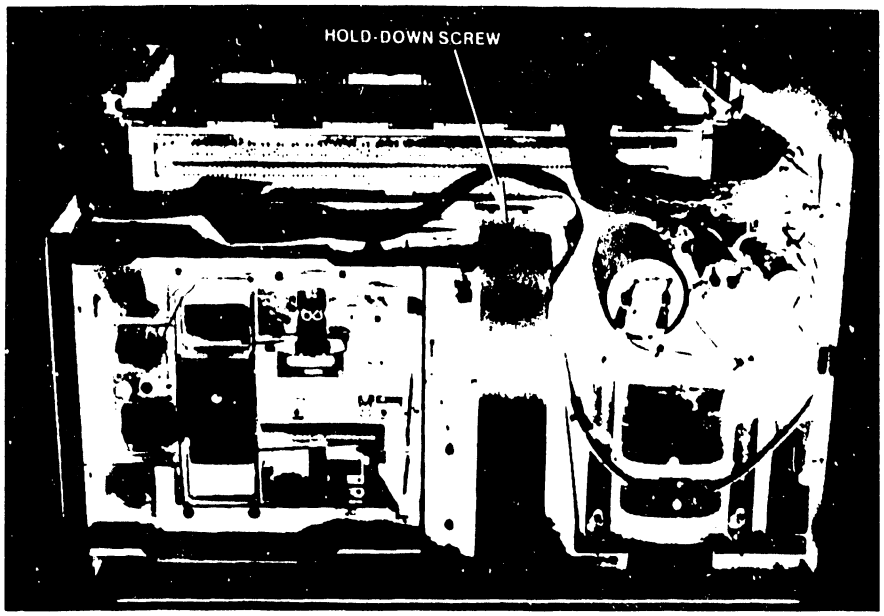
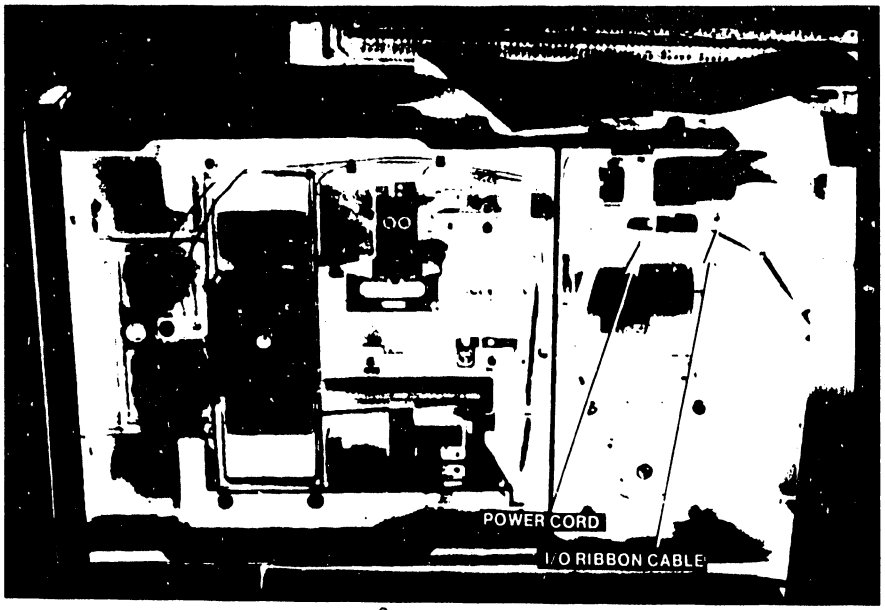


Figure 4-12 OIS 105/115/125A/130A Top Cover Removal/Installation



A
SIDE VIEW TOP
COVER REMOVED



B
SIDE VIEW TOP
COVER REMOVED

Figure 4-13 Removing/Installing the Diskette Drive Unit

4.5.3 Original Front Panel Removal

When a TC controller is installed into a 105/115/125A/130A Master, the front panel must be replaced with a TC Front Panel (P/N 270-0632) which contains a Lamp Board with a single row LED display (P/N 210-7865). Perform the following procedure to remove and replace the existing front panel with a TC front panel.

1. Remove the four Phillips-head screws and washers, two on each side that secure the front panel to the U-chassis (Figure 4-14). Save the screws for use in installing the new front panel.

2. Disconnect the ribbon-cable from motherboard connector J4.

WARNING
Ensure that the AC power cable
is disconnected from the outlet

3. Noting the position and color coding of the two twisted pairs, disconnect the slip-on connectors from the rear of the POWER switch.

4. Lift out the front panel.

5. As shown on Figure 4-14, detach the 125A Front Panel Board (P/N 210-7651) from the front panel by removing the four Phillips-head screws that secure it to the front panel.

4.5.3.1 TC Front Panel Installation

The lamp board (part of new front panel) is electrically connected to the TC controller via a Lamp Panel Cable (P/N 220-3171). This cable has a socket connector at one end and a edge connector at the other end. The socket connector is plugged into the lamp board and the edge connector will be plugged into the TC controller. The TC front panel is installed as follows.

1. Attach the 125A front panel board (removed from the old front panel during step 5 above) to the TC front panel using four Phillips-head screws.

2. Plug the socket connector end of the lamp panel cable into the J1 matching connector on the lamp board. Ensure socket hole #1 is properly aligned with pin #1.

3. Route the edge connector end of the lamp panel cable through the slot in the side of the U-Chassis (Figure 4-14). Position the cable for connection to the TC controller.

4. Reinstall the four slip-on connectors on the rear of the power switch. Note the position and color codes of the twisted pairs. The two black leads are connected to the leftmost connectors and the two white leads are connected to the rightmost connectors.

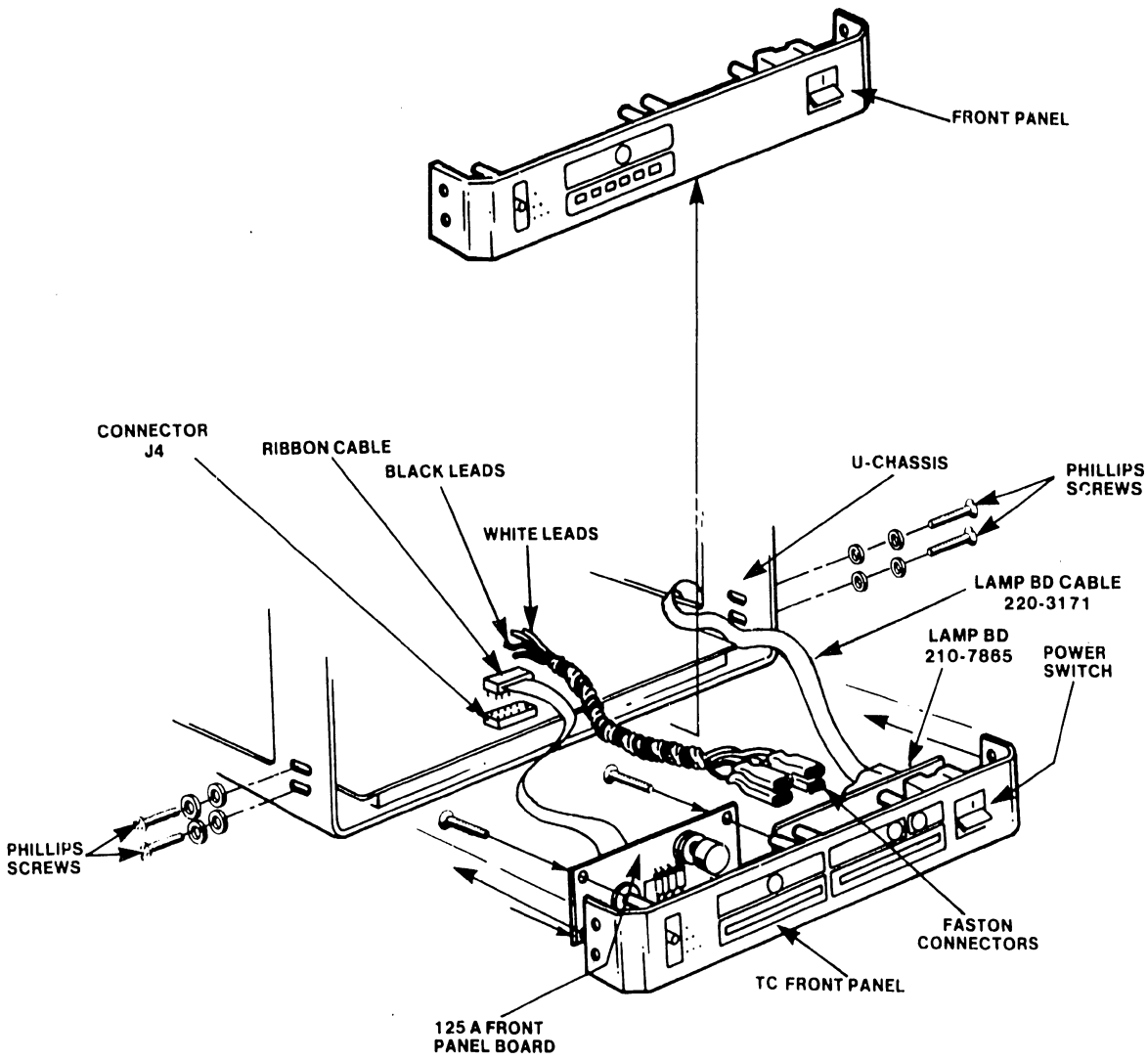


Figure 4-14 Front Panel Removal/Installation

5. Reconnect the ribbon cable between the front panel and J4 on the motherboard.

6. Install the front panel and align the screw holes.

7. Replace the four Phillips-head screws, two on each side, that secure the front panel.

NOTE

If the TC front panel is not properly aligned, the top cover will not seat properly. To properly align the front panel, push the panel towards the rear of the unit before tightening the four Phillips-head screws. If a large gap exist between the TC front panel and the top cover readjust accordingly.

4.5.3.2 Diskette Drive Installation

1. Slide the unit onto the chassis such that the base-plate guides engage the corresponding slots.

2. Firmly push the unit into the slots until the hold-down screw and threaded hole are aligned.

3. Tighten the captive hold-down screw.

4. Reconnect the I/O ribbon cable.

5. Reconnect the ac power cable.

4.5.4 Winchester Controller "A" and "B" Cable Removal

A 50-conductor flat cable connects the Winchester Controller "A" board to the Winchester Drive, and a 20-conductor flat cable connects the Winchester Controller "B" board to the Winchester Drive. These two cables must be disconnected to gain access to the I/O slot needed to install the TC controller.

Refer to Figure 4-15 and perform the following procedure to disconnect the "A" and "B" cables.:

1. Disconnect the 50-conductor flat cable from J1 on the 7650 board.

2. Disconnect the 20-conductor flat cable from J1 on the 7653 board.

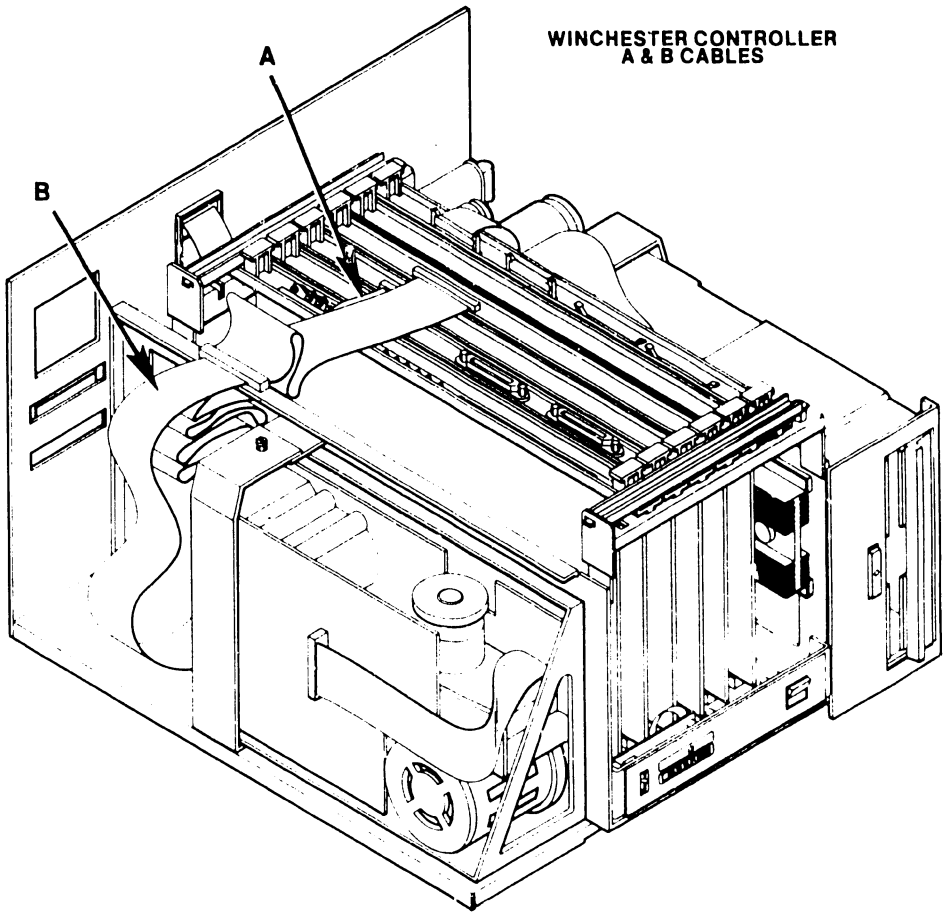


Figure 4-15 Ribbon Cable Connections

4.5.5 PC Guide Block Installation

On older 105/115/125A/130A Masters, it may be possible to install a TC controller backwards into the masters motherboard. To prevent this, a special PC Guide Block (P/N 449-0314) should be installed the first time the motherboard is removed for maintenance purposes. Units manufactured since late 1981 should have this guide block installed.

Table 4-6 lists the parts required to install the PC guide block. The installation procedure is presented below.

Table 4-6 PC Guide Block Installation

Part Description:	Quantity	Part No.
PC Guide Block	1	449-0314
Spacer	1	462-0120
Flat-head Screw , 4-24 by 3/4"	1	651-0058

1. Remove the two board retainers Figure 4-16.

2. Remove the 7501, 7502, and 7950 PCBs to gain access to the motherboard.

3. As shown in Figure 4-17, two Phillips-head screws secure connector J13 (identified as connector number 1 on some 140/145 Masters) to the motherboard. Remove the rearmost screw from the connector.

4. Insert the spacer into the indented center hole, located on the bottom side of the PC guide block (there are two indented center holes, either one can be used).

5. Align the indented screw hole and spacer with the support block screw hole (located directly behind connector J13 on the motherboard). Insert the self-tapping flat-head screw through the center hole and spacer on the guide block. Secure the block to the motherboard by screwing the flat-head screw into the Support Block (P/N 449-0398).

6. Re-install the 7501, 7502, and 7950 PCBs into their correct locations on the motherboard.

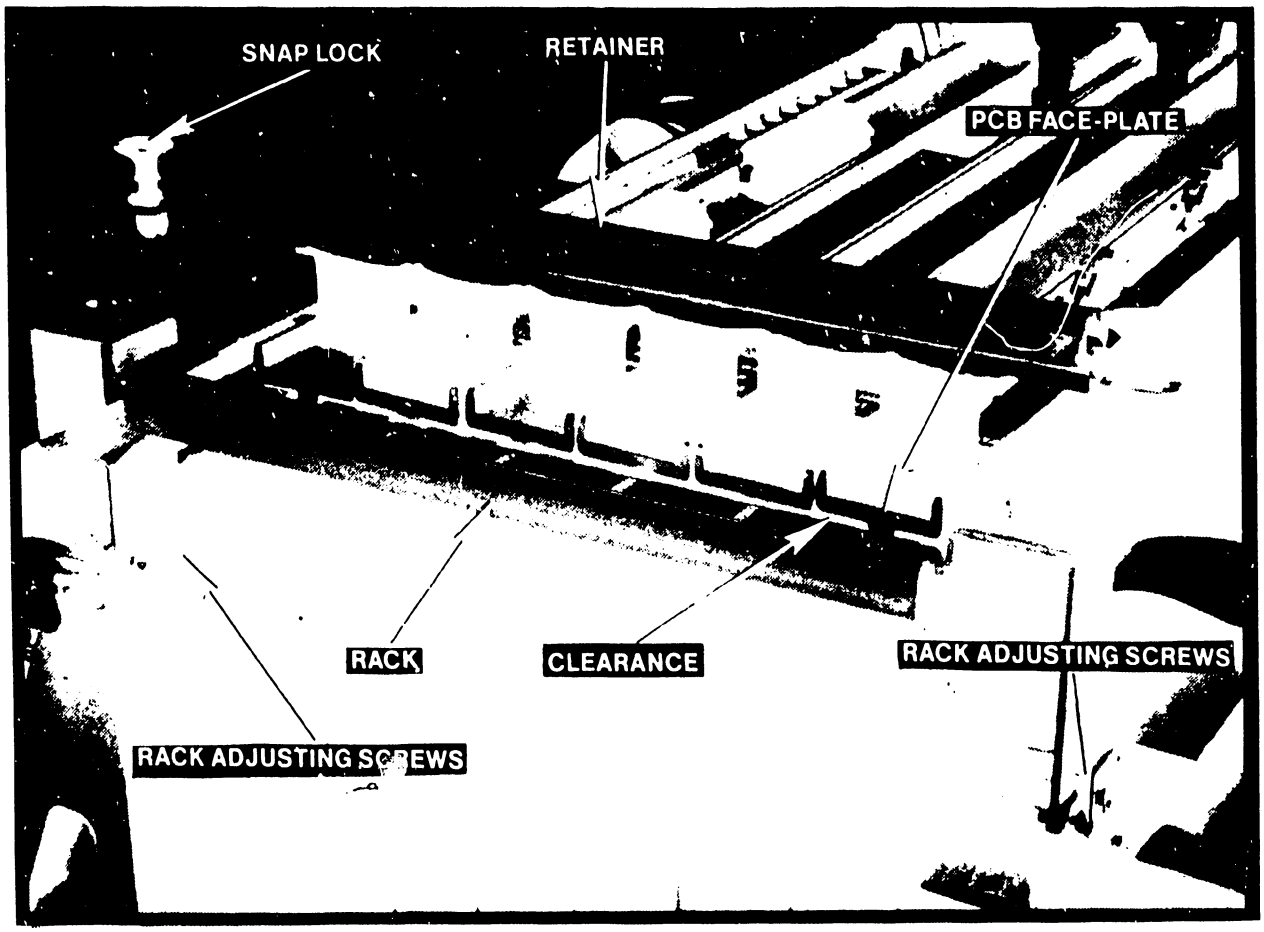


Figure 4-16 PCB Removal/Installation on 105/115/125A/130A Masters

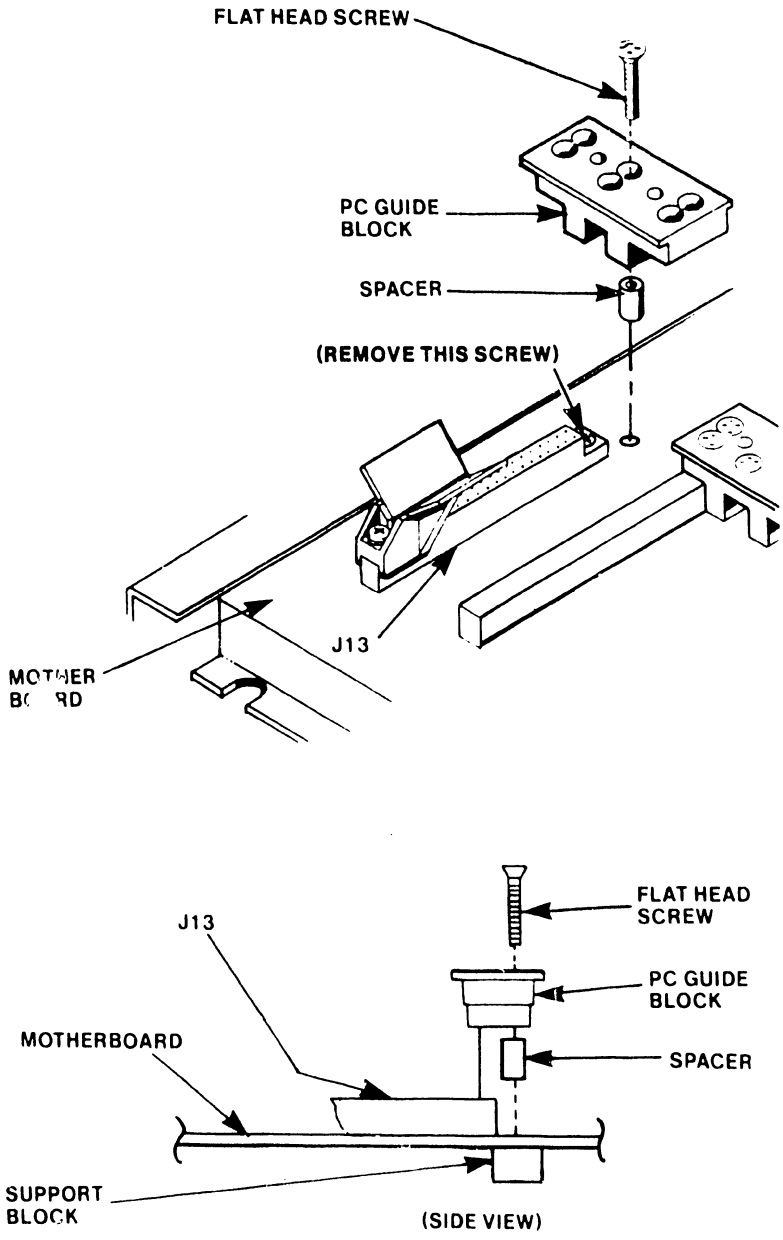


Figure 4-17 PC Guide Block Installation (105/115/125A/130A Only)

4.5.6 TC Controller PCB Installation (105/115/125A/130A) Masters

The TC controller is secured to the motherboard by two board retainers as shown in Figure 4-16.

The TC controller should not fit snugly against the board racks. There should be 1/32-inch of clearance between the TC controller and the rack. The retainers should fit just tightly enough to deform the shorting strip. Perform the following procedure to install the TC controller.

1. Remove the two board retainers.

2. Refer to Paragraph 4.3, to verify TC controller switch settings.

3. Install the TC controller into the I/O slot furthest to the left, when viewing the unit from the front (see Figure 4-18). The board connectors on the motherboard have card guides to ease insertion, and card keys to center the boards.

4. Plug the edge connector end of the Lamp Panel Cable (P/N 220-3171) into the J5 connector on the rail of the TC controller PCB.

NOTE

For ease of installation, connect the lamp panel cable to the TC front panel before installing it.

5. Replace the board retainers (see Figure 4-16).

4.5.6.1 Winchester Controller "A" and "B" Cable Installation

After the TC controller has been installed, connect the 20-conductor and 50-conductor flat cables to their respective boards (Figure 4-15).

1. Connect the 20-conductor flat cable to the J1 connector on the 7653 board.

2. Connect the 50-conductor flat cable to J1 on the 7650 board.

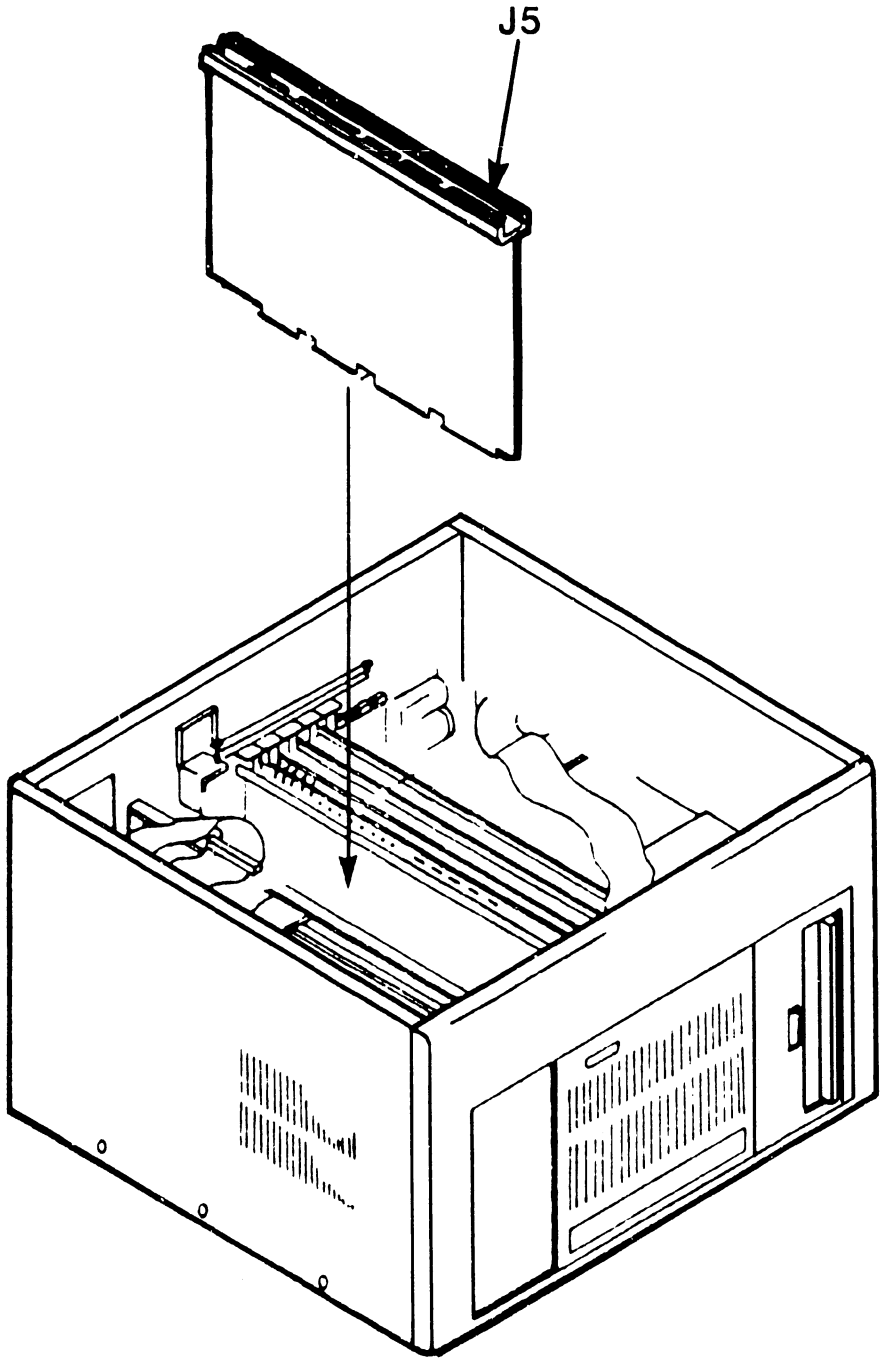


Figure 4-18 TC Controller Installation into 105/115/125A/130A Master

4.5.7 Rear Cover Plate Removal/TC Rear Panel Installation

Three edge connectors (RS-232-C, RS-449, and RS-366 interfaces) and a 4-pin BNC/TNC interface connector are located on the TC Controller PCB. To route and connect the interface cables to these connectors from outside the master, the existing rear cover plate must be replaced by a TC rear panel.

With the introduction of the DLP64 and DLP128 to the OIS TC product line, a change was made to the rear cable panel configuration. Previously a TC rear cable panel was shipped from manufacturing with three interface connectors (RS 232-C, RS-366, RS-449) installed. Beginning in the spring of 1983, a customer must specify the interface option desired (RS-232-C, RS-366, RS-449/X.21).

For the necessary cables for use with RS-232-C, RS-366 and X.21 options, refer to Installation Requirements (paragraph 4.5).

NOTE

In the event that the RS-366 ACU option is ordered, both of the following interface cables are necessary:

RS-366 Flat Cable	P/N 220-3174
RS-232-C Flat Cable	P/N 220-3129

4.5.7.1 Rear Cover Plate Removal

Remove the existing rear cover plate by removing the four machine screws that secure it to the rear of the master unit, then pull the plate away from the unit (Figure 4-19).

4.5.7.2 RS-232-C or RS-366 Interface Cable Installation

Perform the following steps to secure the RS-232-C or RS-366 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-9 (page 4-17, internal side of TC rear panel).

2. Remove the panel insert corresponding to the cable option supplied (e.g. RS-232-C).

3. Align the interface cable "D" connector behind the TC rear panel slot labeled RS -232-C or RS-366. Position the connector such that the long edge of the "D" connector is on the right (see Figure 4-9, view A).

4. Insert two threaded standoffs (P/N 478-0791) through the TC rear panel screw holes.

5. Install the red wire ground lug on one standoff and a washer on the other standoff (Figure 4-9).

6. Secure the "D" connector to the TC rear panel using two 4-40 nuts.

7. Repeat steps 1 through 6 if a second cable is installed (as with the RS-366 option).

8. Proceed to Paragraph 4.5.7.4, to install the TC rear panel.

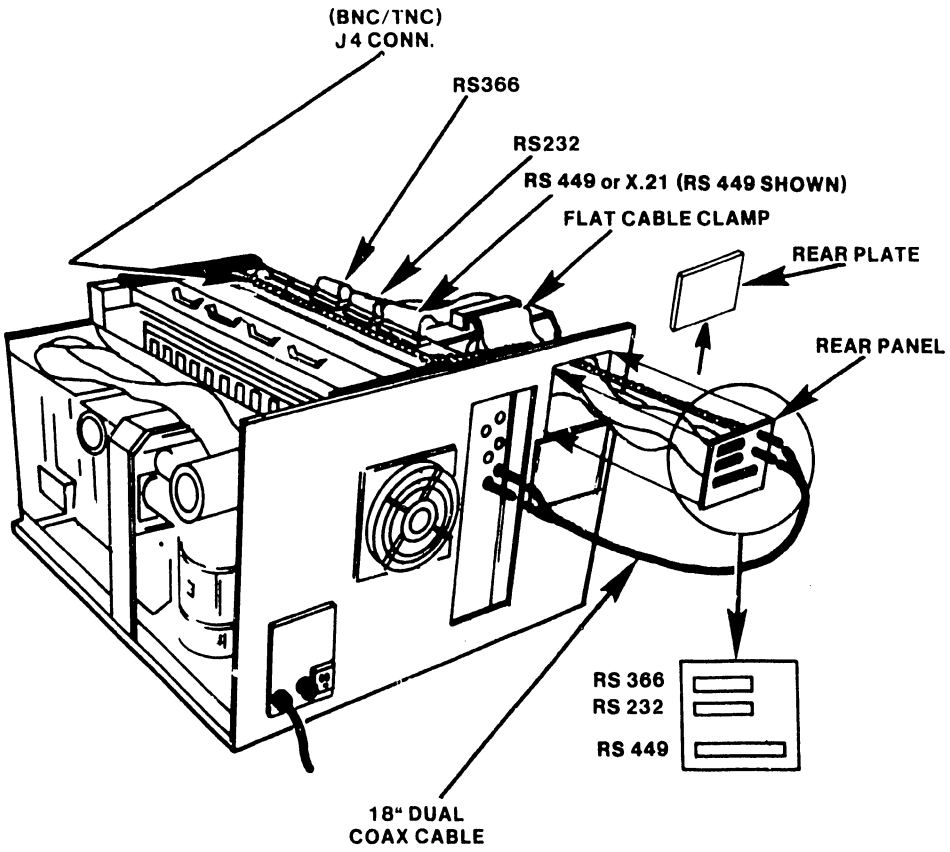


Figure 4-19 Rear Cover Plate Removal

4.5.7.3 X.21 Interface Cable Installation

Perform the following steps to secure the X.21 interface cable to the TC rear panel.

1. Position the TC rear panel as shown on Figure 4-10 (page 4-18, internal side of TC rear panel).

2. Remove the panel insert covering the RS-449 slot.

3. Fit the X.21 cable "D" connector to the adapter plate. Make certain that the long edge of the "D" connector is on top (Figure 4-10, view A).

4. Insert two threaded standoffs (P/N 478-0791) through the X.21 adapter plate (P/N 452-0274) and "D" connector screw holes. Ensure pemnuts on adapter plate are facing as shown in Figure 4-10.

5. Install the red wire ground lug on one standoff and a washer on the other standoff (Figure 4-10).

6. Secure the X.21 cable "D" connector to the X.21 adapter plate by threading two 4-40 nuts onto the standoffs.

7. Secure the X.21 adapter plate to the TC rear panel using two 4-40 screws. Insert screws through the panel and thread them into the two pemnuts on the adapter plate.

8. Proceed to Paragraph 4.5.7.4, to install the TC rear panel.

4.5.7.4 TC Rear Panel Installation

Perform the following procedure to secure the TC rear panel to the master rear panel. Before performing this procedure ensure that the following cables are present or have been installed on the TC rear panel:

BNC/TNC connector cable (internal)
One or two 20-inch flat interface cables.

1. To install the TC rear cable, route the flat cables and the BNC/TNC connector cable through the opening created by removing the rear plate.

2. Using four machine screws secure the TC rear panel to the rear of the master unit.

NOTE
Proceed to step 6 if not installing the X.21 interface.

3. While referring to Figure 4-11 (page 4-20), carefully insert the X.21 DIP connector into J2 of the X.21 adapter board (P/N 210-7951) Ensure pin alignment.

4. Connect the X.21 adapter board to the RS-449/X.21 connector (J3) of the TC controller.

5. Proceed to step 7.

6. Connect the the 20-inch flat cable(s) to the corresponding connector located on the rail of the TC controller PCB (RS-232-C, RS-366 or RS-449/X.21) as shown in Figure 4-2. Once the cable(s) have been connected, secure it to the U-chassis using the flat cable clamp (P/N 654-1318).

7. Note the key orientation and plug the 4-pin BNC/TNC cable connector from the TC rear cable panel into connector J4 located on the rail of the TC controller PCB. The BNC/TNC Cable is held into position by a snap-in clamp and should set flush on top of the TC controller.

8. Connect the 18-inch dual coaxial cable from the BNC/TNC connector on the external side of the TC rear cable panel to any dual connector port on the rear of the master unit.

4.5.8 Top Cover Installation

The instructions for reinstalling the top cover onto an OIS 105/115/125A/130A Master Unit are as follows:

1. Set the top cover over the front of the master and slide fully to the rear (Figure 4-12).

2. Insert and start the two Phillips-head screws at the rear panel; do not tighten.

3. Insert and start the six Phillips-head screws (3 each side) at the sides of the top cover.

4. Tighten all screws.

5. Refer to Paragraph 4.8, to perform the Master Power-On procedure.

4.6 INSTALLATION REQUIREMENTS (OIS 40/50 MASTERS)

The following parts list provides reference to assemblies that are needed to install a TC Controller in an OIS 40/50 Master. The hardware necessary to complete the installation is listed under each assembly that is underscored.

NOTE
Optional assemblies are marked with an asterisk

Part Description	Part Number
Front Panel	270-0873
Lamp Board with a 1 row LED display	210-7865
Lamp Panel Cable	220-3306
Rear Cable Panel	270-0872
BNC/TNC Cable	220-2002
18-Inch Dual Coaxial Cable	220-0225
RS 232-C Internal Cable Assembly*	279-0560
RS-232-C Flat Cable	220-3303
Modem Cable	220-0332
RS-366 Internal Cable Assembly*	279-0561
RS-366 Flat Cable	220-3304
Modem Cable	220-0332
X.21 Cable Assembly*	289-0195
X.21 Interface Bd	210-7951
X.21 Flat Cable	220-3305
X.21 Adapter plate	452-0274
Modem Cable	220-0274

The following TC Controller configurations are available based on system requirements:

DLP64 Controller*	212-3040
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-1A
DLP128 Controller*	212-3038
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-A

4.6.1 Front Panel and Side Cover Removal

The following removal procedure must be performed to remove or install any OIS 40/50 assembly.

1. Using a Phillips-head screwdriver remove the two screws located in the bottom left and right-hand corners of the front panel.

2. Flip up the black flap located directly above the face of the floppy disk drive. Remove the two Phillips-head screws concealed beneath the flap.

WARNING

Avoid operating the 40/50 Master with side covers removed for more than ten minutes as this may cause the switching power supply to overheat. The fans depend on the side covers to maintain proper airflow.

3. The left side cover cannot be removed without first removing the right side cover. Using a Phillips-head screwdriver, remove six screws (from the rear) that secure the right and left side cover(s) to the master chassis (Figure 4-20).

4. Slide the right panel toward the rear of the unit to disengage the tabs which fasten the cover to the front corner post of the OIS 40/50 chassis (Figure 4-21).

5. Disengage the tabs that secure the left cover at the top of the unit and lift the left side cover up and away from the chassis.

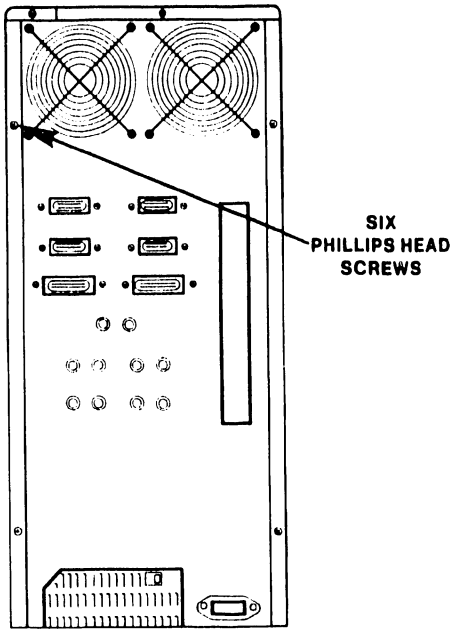


Figure 4-20 40/50 Master Rear Panel Removal

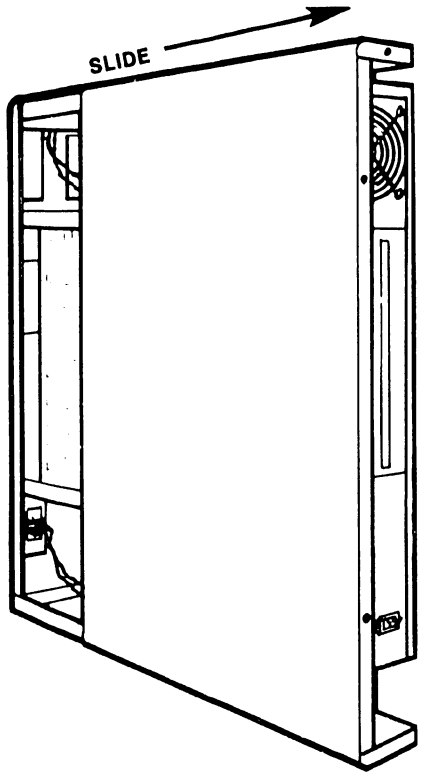


Figure 4-21 Side Cover Removal

4.6.2 Rear Cover Plate Removal/TC Rear Panel Installation

Three edge connectors (RS-232-C, RS-449, and RS-366 interfaces) and a 4-pin BNC/TNC interface connector are located on the rail of the TC Controller PCB. To route and connect the appropriate interface cables to these connectors from outside the master, the existing rear cover plate must be replaced by a TC rear panel.

Refer to Installation Requirements (Paragraph 4.6), to obtain the part numbers of the cables and other items required for use with RS-232-C, RS-366, or the RS-449/X.21 interface options. If the RS-366 ACU option is being installed, both of the following interface cables are required:

RS-366 Flat Cable (1 each)	P/N 220-3304
RS-232 Flat Cable (1 each)	P/N 220-3303

4.6.2.1 Rear Cover Plate Removal

Remove the rear cover plate to allow installation of the interface cable(s) and the TC rear panel.

Remove six Phillips-head screws to remove the rear cover plate (Figure 4-22).

4.6.2.2 RS-232-C or RS-366 Interface Cable Installation

Perform the following steps to secure the RS-232-C or RS-366 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-23 (external side of TC rear panel is shown).

2. Align the interface cable "D" connector behind the panel slot labeled RS-232-C or RS-366. Position the connector such that the long edge of the "D" connector is on the right (see Figure 4-23).

3. Insert two threaded standoffs (P/N 478-0791) through the TC rear panel screw holes and the "D" connector as shown in Figure 4-23.

4. Install the red wire ground lug and washer on the standoffs (back side of "D" connector) as shown in Figure 4-23.

5. Secure the "D" connector to the TC rear panel by threading two 4-40 nuts onto the standoffs.

6. Repeat steps 2 through 6 if a second cable is installed (as with the RS-366 option).

7. Proceed to Paragraph 4.6.2.4, to install the TC rear panel.

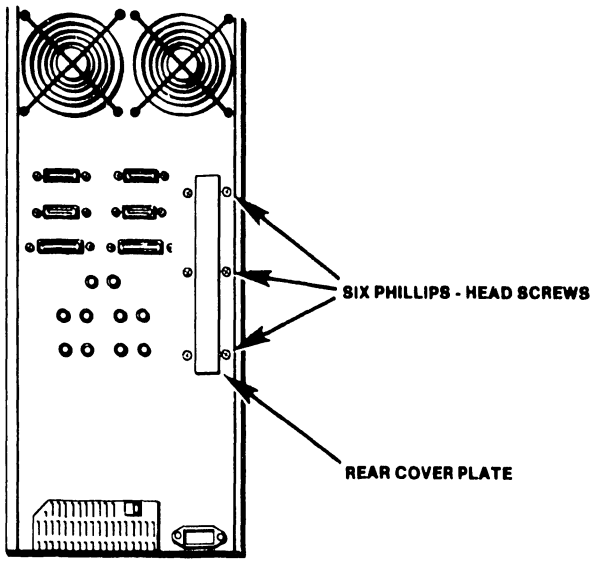


Figure 4-22 Rear Cover Plate Removal

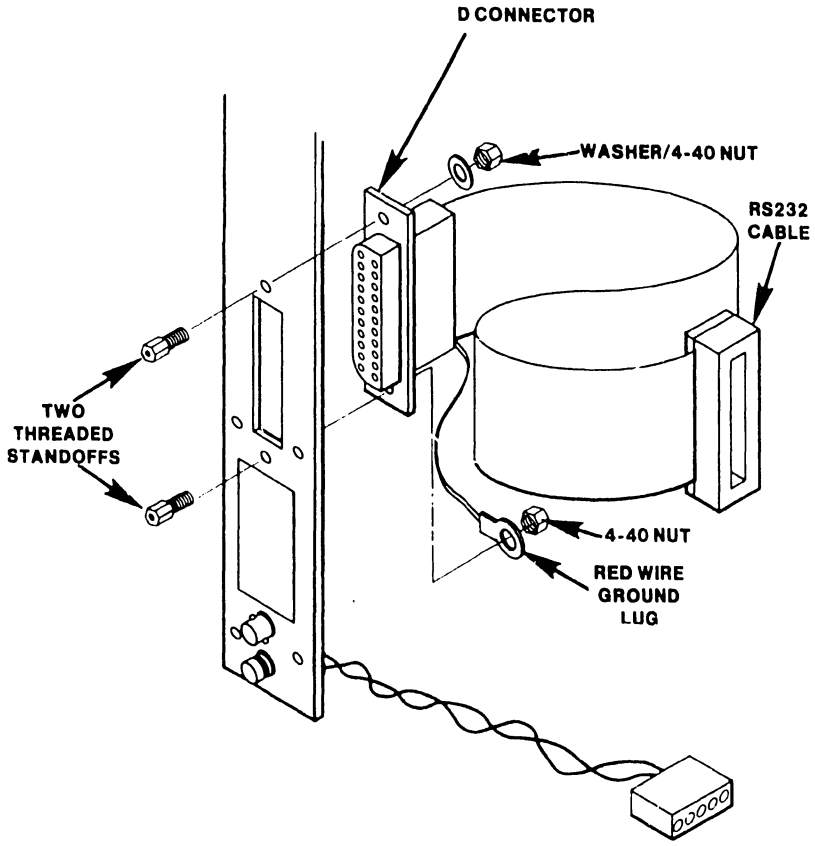


Figure 4-23 RS 232-C or RS-366 Interface Cable Installation
(Installed from inner side of TC Rear Panel)

4.6.2.3 X.21 Interface Cable Installation

Perform the following steps to secure the X.21 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-24 (external view of rear cable panel).

2. Fit the X.21 cable "D" connector to the adapter plate. Make certain that the long edge of the "D" connector is positioned to the right (Figure 4-24).

3. Insert two threaded standoffs (P/N 478-0791) through the X.21 adapter plate (P/N 452-0274) holes. Ensure pemnuts on adapter plate are facing as shown in Figure 4-24.

4. Place the red wire ground lug and washer on the standoffs as shown in Figure 4-24.

5. Secure the "D" connector to the X.21 adapter plate using two 4-40 nuts.

6. Secure the X.21 adapter plate and "D" connector to the TC rear panel using two 4-40 screws. Insert these two screws through the TC rear panel and thread them into the two pemnuts on the adapter plate.

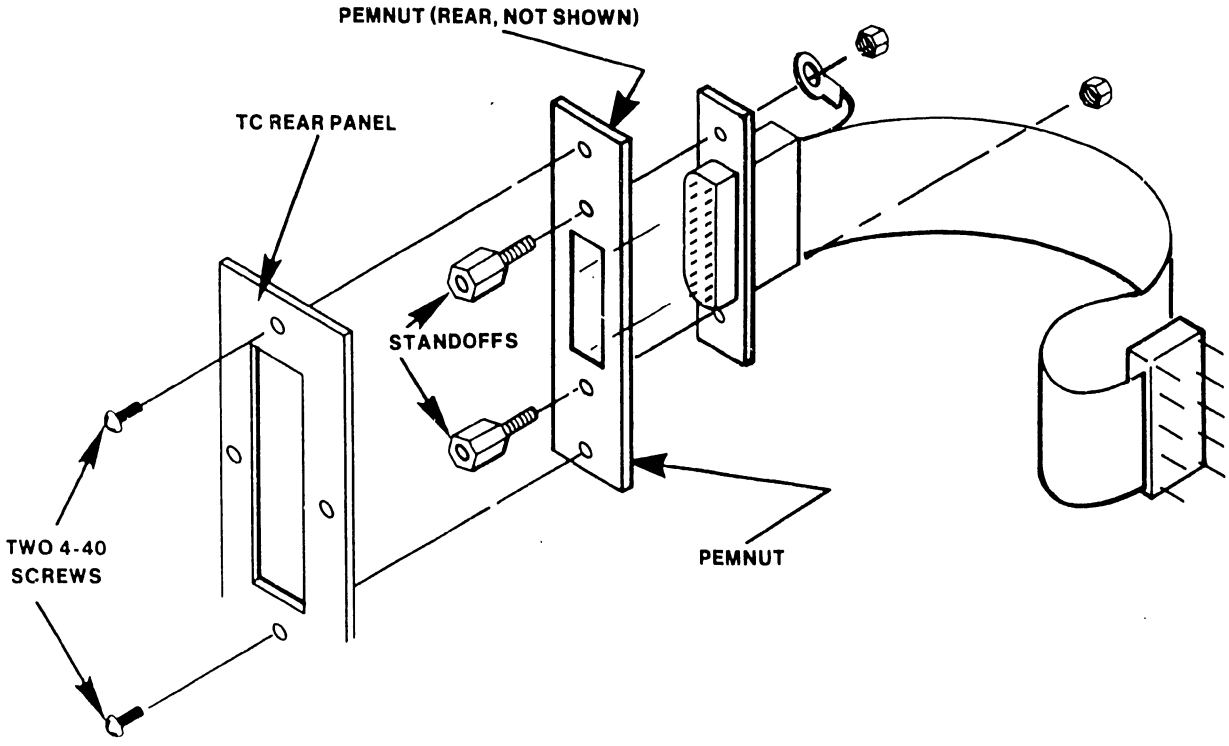


Figure 4-24 X.21 Interface Cable Installation

4.6.2.4 TC Rear Panel Installation

Perform the following procedure to secure the TC rear panel to the master rear panel. Before performing this procedure ensure that the following cables are present or have been installed on the TC rear panel:

BNC/TNC connector cable (internal)
One or two 35-inch flat interface cables

1. Position the TC rear panel over the open slot (from internal side of master) in the masters rear panel as shown in Figure 4-25.

2. Secure the TC rear panel to the master chassis using the six-Phillips-head screws used when removing the rear cover plate.

3. Connect and then route the external 18-in. dual coaxial cable from the TC rear panel to any dual connector port on the rear of the master as shown in Figure 4-25.

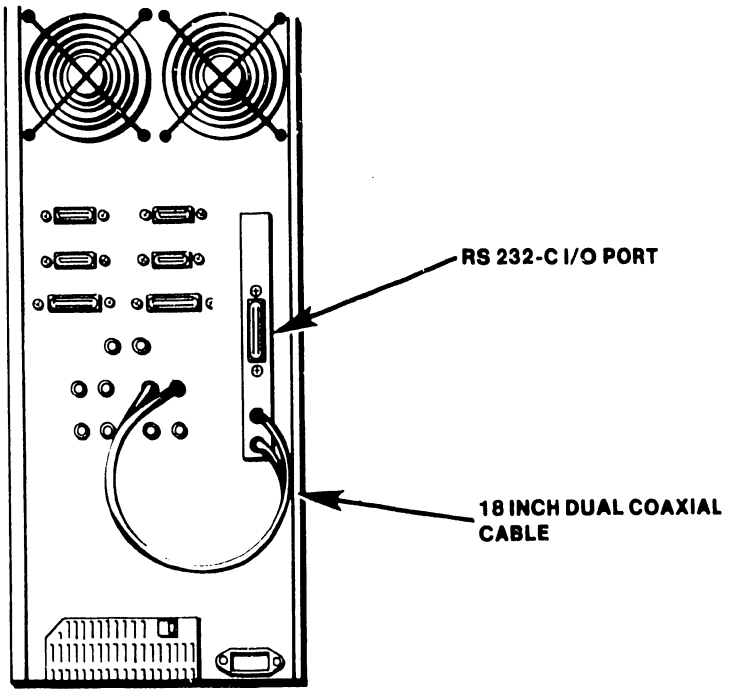


Figure 4-25 TC Rear Panel Installation

4. Route the interface cables through the appropriate side frame slot (X.21 the top most slot, RS 232-C the second slot, and RS-366 the third slot from the top) located on the right-rear-side of master (viewed from rear) as shown in Figure 4-26.

5. Route the BNC/TNC cable through the bottom most side frame slot.

6. Route the interface cables to the front of the master. The interface cable(s) will be connected following completion of the TC Front Panel Installation procedure, Paragraph 4.6.2.5.

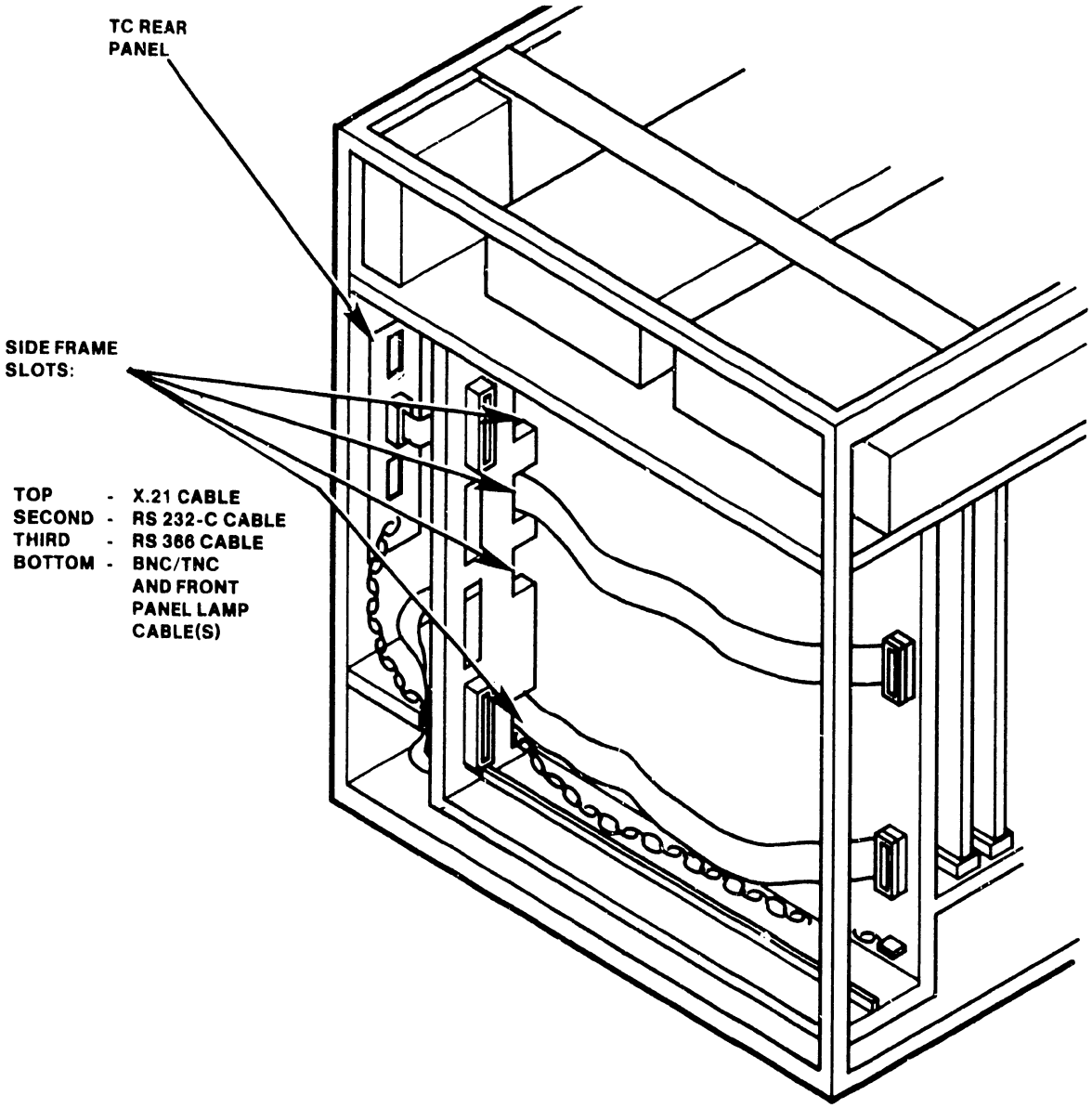


Figure 4-26 Side Frame Slots

4.6.2.5 TC Front Lamp/Switch Panel Installation

Perform the following procedure to remove the front panel blank, install the TC Front Lamp/Switch Panel and to route the front panel cable to the TC controller PCB.

1. Loosen two Phillips-head screws and washers to remove the blank panel. Set screws and washers aside for use when installing the TC front lamp/switch panel (Figure 4-27).

2. Route the front panel cable through the open slot and then align the TC front panel to the open slot. Secure the TC front lamp/switch panel to the chassis using two-Phillips-head screws and washers.

3. Attach the TC front panel cable to the cable clips as shown in Figure 4-27.

4. Route the cable to the rear of the master and down through the enclosure in the rear of the system.

5. Fit the cable through the bottom most slot in the side frame as shown in Figure 4-28.

6. Pull the cable through the slot to the front of the master, and set aside with interface cables (on the inner side of the chassis). The cables will be connected per the TC Controller PCB installation procedure.

NOTE
Ensure that the cable does not rip or tear when feeding through side frame slot

4.6.2.6 TC Controller PCB Installation

1. Refer to Paragraph 4.3, to verify TC controller switch settings.

2. Install the TC controller by pushing firmly on the PCB until it engages with the motherboard slots. Hold cables against the chassis to prevent them from following the TC controller.

3. Connect the cables as follows:

   TC lamp board cable to J5 (bottom most connector).
   BNC/TNC cable to J4.
   RS-232-C and RS-366 interface cables are connected as labeled on the TC controller PCB rail. Perform the X.21 cable installation as follows.

4. Carefully insert the X.21 DIP connector into J2 of the X.21 Adapter Board (P/N 210-7951) as shown in Figure 4-29. Ensure pin alignment.

5. Connect the X.21 adapter board to the RS-449 connector (J3) of the TC controller as shown in Figure 4-29.

6. Refer to Paragraph 4.8, to perform the Master Power-On procedure.

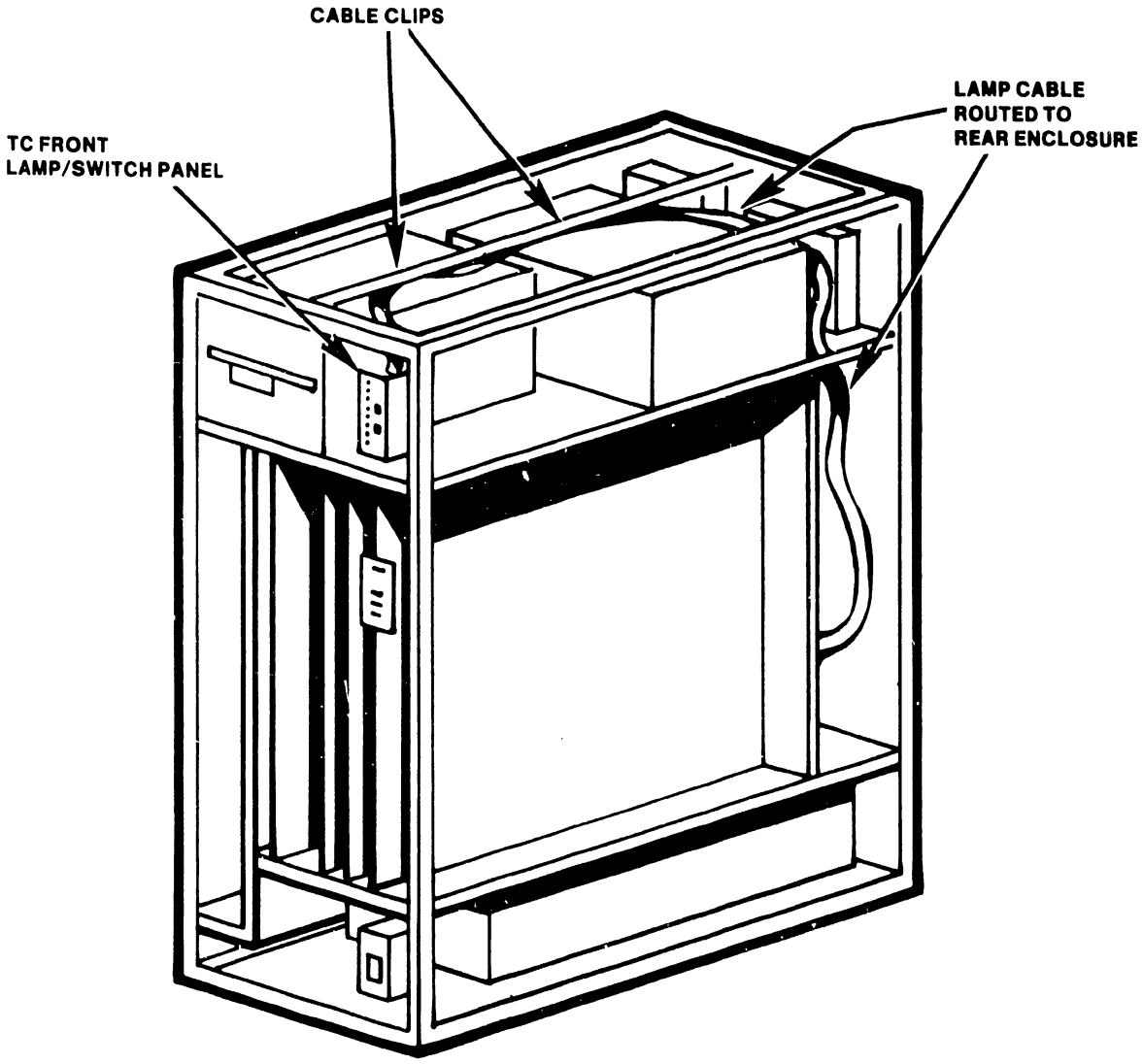


Figure 4-27 TC Front Lamp/Switch Panel
Installation/Cable Routing

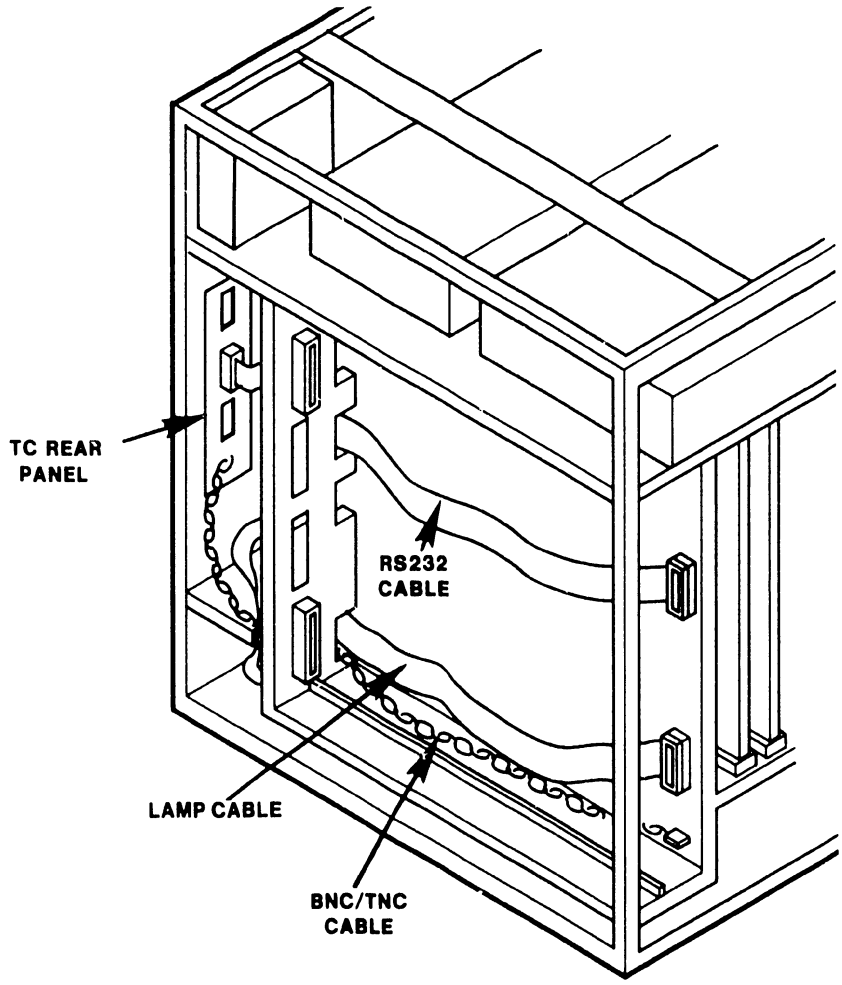


Figure 4-28 TC Lamp Board Cable Routing (bottom side frame slot)

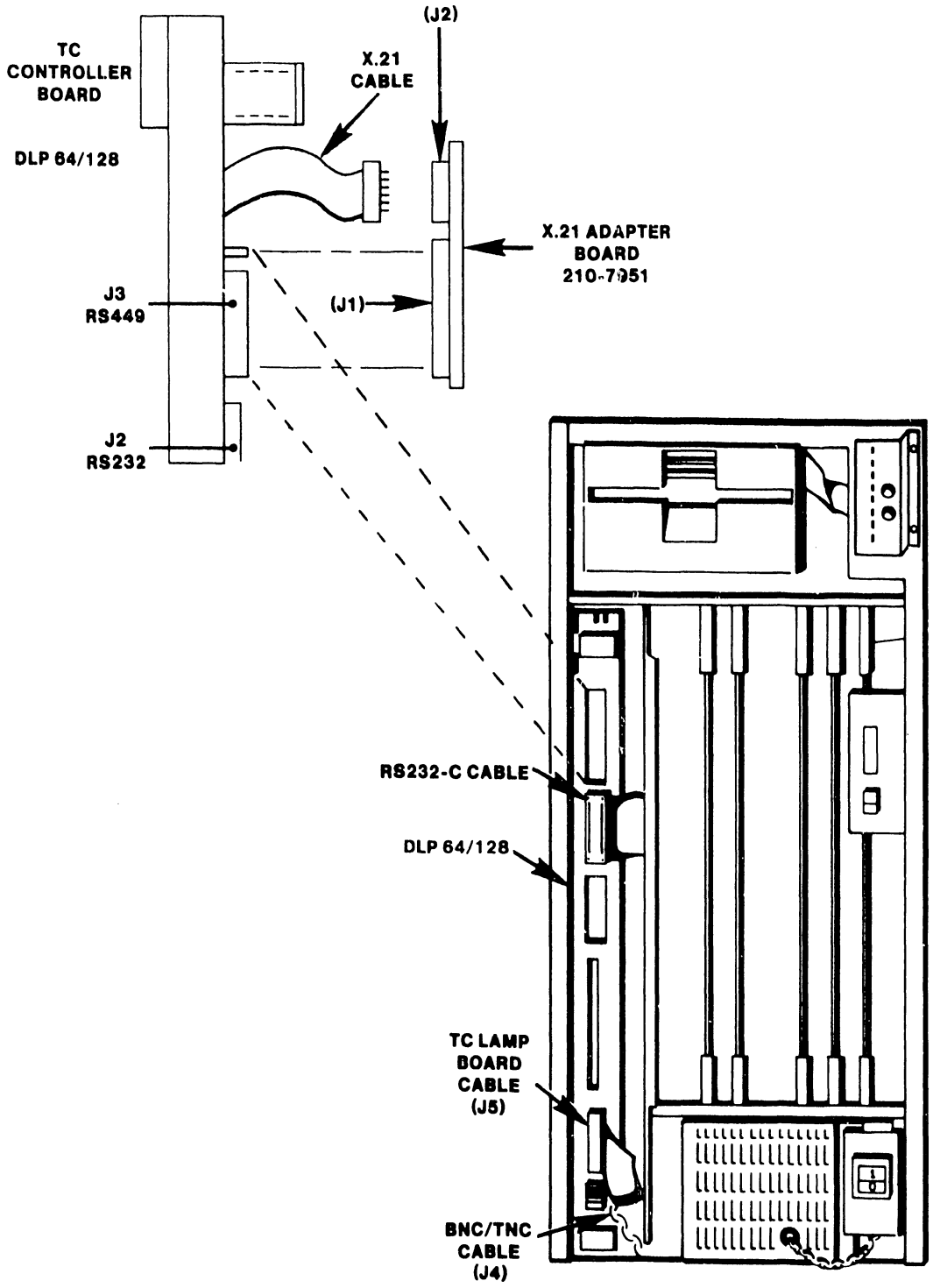


Figure 4-29 TC Controller PCB Installation

4.7 INSTALLATION REQUIREMENTS TELECOMMUNICATIONS PROCESSOR

The following parts list provides reference to assemblies that are needed to install a TC Controller in a Telecommunications Processor (TCP). The hardware necessary to complete the installation is listed under each assembly that is underscored.

NOTE
Optional assemblies are marked with an asterisk

Part Description	Part Number
TC Front Panel	270-0661
Lamp Board	210-7865
Lamp Board Cable	220-3171
Rear Panel Assembly	270-0868
BNC/TNC Cable	220-1710
25 ft. Dual Coaxial Cable	220-0148
RS-232-C Internal Cable Assembly	279-0555
RS-232-C Flat Cable	220-3179
Modem Cable	220-0332
RS-366 Internal Cable Assembly	279-0556
RS-366 Flat Cable	220-3180
Modem Cable	220-0332
X.21 Internal Cable Assembly	289-0191
X.21 Flat Cable	220-3223
X.21 Interface Board	210-7951
Modem Cable	220-0274

The following TC Controller configurations are available based on system requirements:

TCB-1 Controller*	212-3014
CPU Motherboard	210-7763A
Data Link & Memory Board	210-7762A
DLP64 Controller*	212-3040
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-1A
or	
DLP128 Controller*	212-3038
CPU Motherboard	210-7963A
Data Link and Memory Board	210-7962-A

4.7.1 Top Cover Removal

1. Remove the top cover by loosening three screws at the rear of the unit.

2. Slide the top cover forward and lift off TCP chassis.

4.7.2 Lamp Board Installation

Perform the following procedure to install from one up to four (one per TC Controller), lamp board panels in the TCP.

1. Remove the blank panel(s) to allow installation of the lamp board(s).

2. Access lamp board cable and feed the cable through the appropriate lamp board slot (Figure 4-30). The cable will be connected to the TC controller per the TC controller PCB Installation procedure (Paragraph 4.7.3.6).

3. Secure the lamp board to the TCP front panel using four Phillips-head screws.

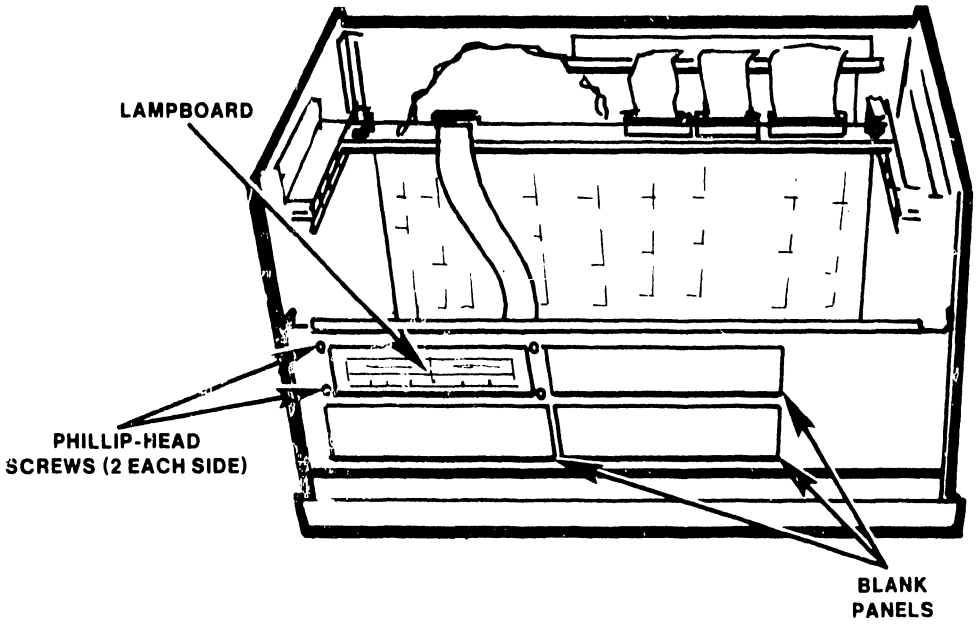


Figure 4-30 Lamp Board Installation

4.7.3 Rear Cover Plate Removal/TC Rear Panel Installation

Three edge connectors (RS-232-C, RS-449, and RS-366 interfaces) and a 4-pin BNC/TNC interface connector are located on the rail of the TC Controller PCB. To route and connect the appropriate interface cables to these connectors from outside the TCP, the existing rear cover plate must be replaced by a TC rear panel.

Refer to Installation Requirements (Paragraph 4.7), to obtain the part numbers of the cables and other items required for use with RS-232-C, RS-366, or the RS-449/X.21 interface options. If the RS-366 ACU option is being installed, both of the following interface cables are required:

RS-366 Flat Cable (1 each)	P/N 220-3180
RS-232 Flat Cable (1 each)	P/N 220-3179

4.7.3.1 Rear Cover Plate Removal

Remove the existing rear cover plate by removing the four Phillips-head screws that secure it to the rear of the TCP.

4.7.3.2 RS-232-C or RS-366 Interface Cable Installation

Perform the following steps to secure the RS-232-C or RS-366 interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-31 (internal side of TC rear panel).

2. Align the interface cable "D" connector behind the panel slot labeled RS-232-C or RS-366. Position the connector such that the long edge of the "D" connector is on the top (see Figure 4-31).

3. Insert two threaded standoffs (P/N 478-0791) through the TC rear panel screw holes and the "D" connector as shown in Figure 4-31.

4. Install the red wire ground lug and washer on the standoffs (back side of the "D" connector) as shown in Figure 4-31.

5. Secure the "D" connector to the TC rear panel by threading two 4-40 nuts onto the standoffs.

6. Repeat steps 1 through 5 if a second cable is installed (as with the RS-366 option).

7. Proceed to Paragraph 4.7.3.5, to install the TC rear panel.

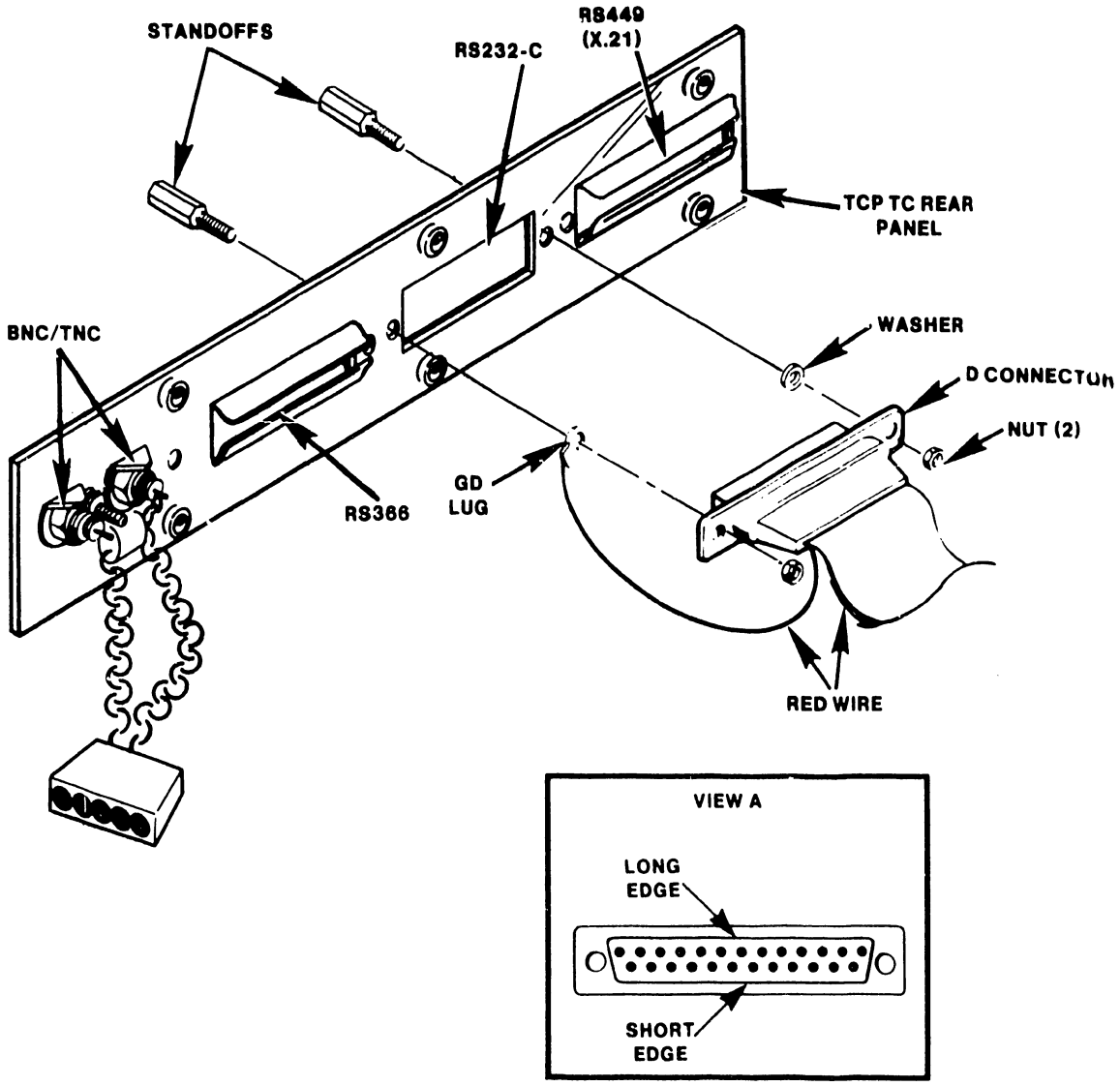


Figure 4-31 RS 232-C or RS-366 Interface Cable Installation

4.7.3.3 X.21 Interface Cable Installation

Perform the following steps to secure the interface cable to the TC rear panel.

1. Position the TC rear panel as shown in Figure 4-32 (internal side of TC rear panel).

2. Fit the X.21 cable "D" connector to the adapter plate. Make certain that the long edge of the "D" connector is on top (Figure 4-32).

3. Insert two threaded standoffs (P/N 478-0791) through the X.21 adapter plate (P/N 452-0274) and "D" connector screw holes. Ensure pemnuts on adapter plate are facing as shown in Figure 4-32.

4. Place the X.21 cable "D" connector on the standoffs (Figure 4-32).

5. Place the red wire ground lug and washer on the standoffs.

6. Secure the "D" connector to the X.21 adapter plate using two 4-40 nuts.

7. Secure the X.21 adapter plate and "D" connector to the TC rear panel using two 4-40 screws. Insert these two screws through the TC rear panel and thread them into the two pemnuts on the adapter plate.

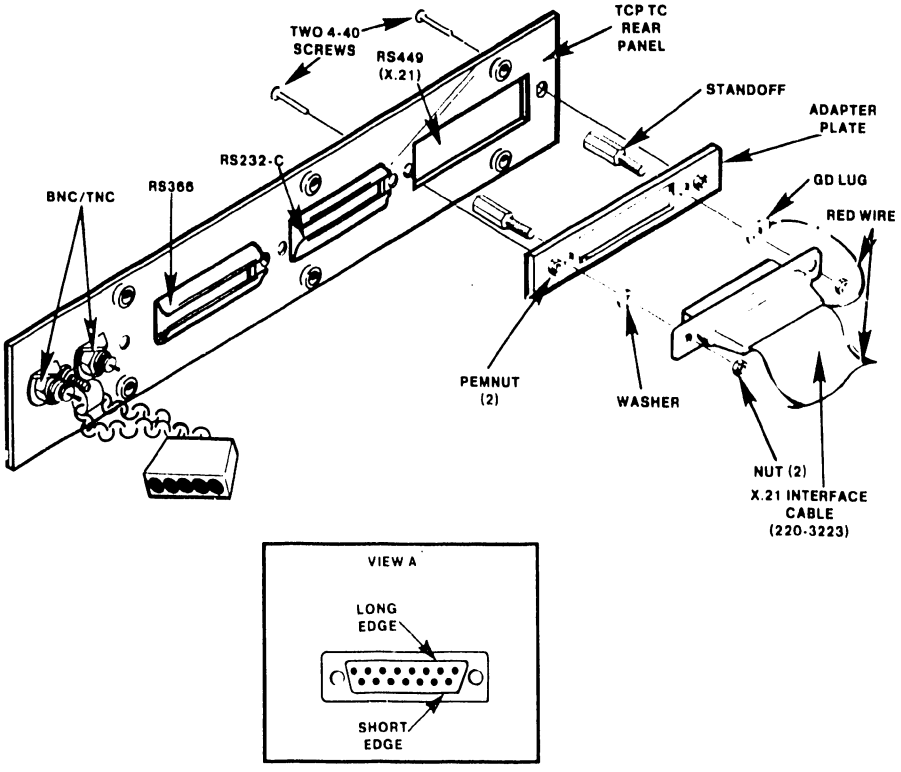


Figure 4-32 X.21 Interface Cable Installation

4.7.3.4 TC Rear Panel Installation

Perform the following procedure to secure the TC rear panel to the TCP rear panel. Before performing this procedure ensure that the following cables are present or have been installed on the TC rear panel:

BNC/TNC connector cable (internal)
One or two 20-inch flat interface cables

1. Position the TC rear panel (with interface cables) over the open slot from inside of TCP chassis. Align and secure using six Phillips-head screws.

2. The cable(s) (interface and BNC/TNC) will be connected per the TC Front Controller PCB Installation procedure, Paragraph 4.7.3.5.

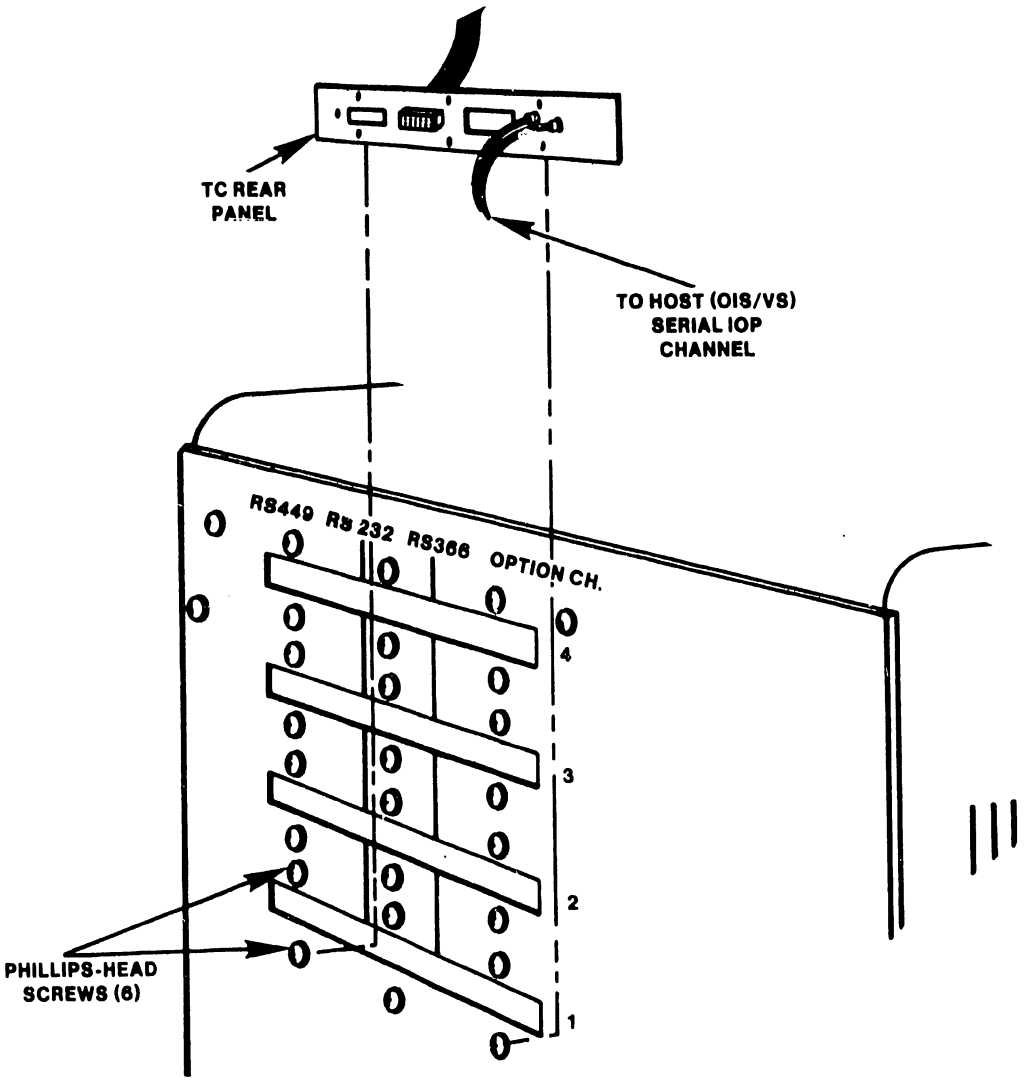


Figure 4-33 TC Rear Panel Installation

4.7.3.5 TC Controller PCB Installation

Perform the following procedure to install (from one up to four) TC controller PCBs.

1. Refer to Paragraph 4.3, to verify TC controller switch settings.

2. Install the TC Controller(s) into the appropriate I/O slot starting with the Channel # 1 I/O slot.

3. Route the BNC/TNC cable (from the TC rear panel) over the cable bracket and plug into J4 on the rail of the TC controller PCB(s) as shown in Figure 4-34.

4. Route the lamp board cable (from the light board) to J5 on the rail of the TC controller PCB(s).

5. Route the following interface cables over the cable bracket and plug in as shown in Figure 4-34.

   RS-366 interface cable to J1
   RS-232-C interface cable to J2
   Perform the X.21 cable installation as follows.

6. Carefully insert the X.21 cable connector into J2 of the X.21 Adapter Board (P/N 210-7951) as shown in Figure 4-35. Ensure pin alignment.

7. Connect the X.21 adapter board to the RS-449/X.21 connector (J3) of the TC controller as shown in Figure 4-35.

8. Connect the 25 ft. dual coaxial cable to/the BNC/TNC ports on the TC rear panel slot and route to an unused host serial IOP port.

9. Refer to Paragraph 4.8, to perform the Master Power-On procedure.

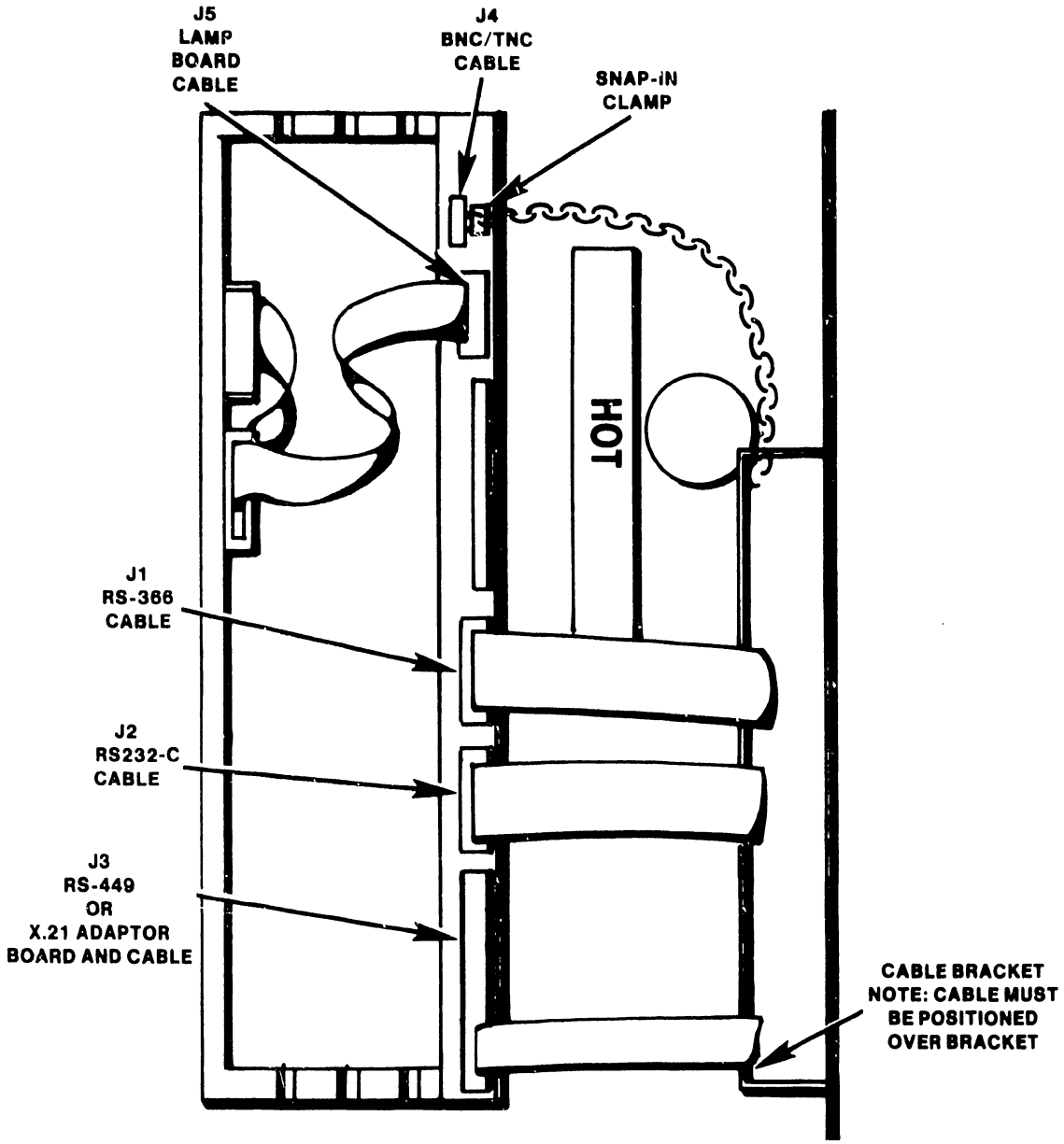


Figure 4-34 Interface Cable Connection

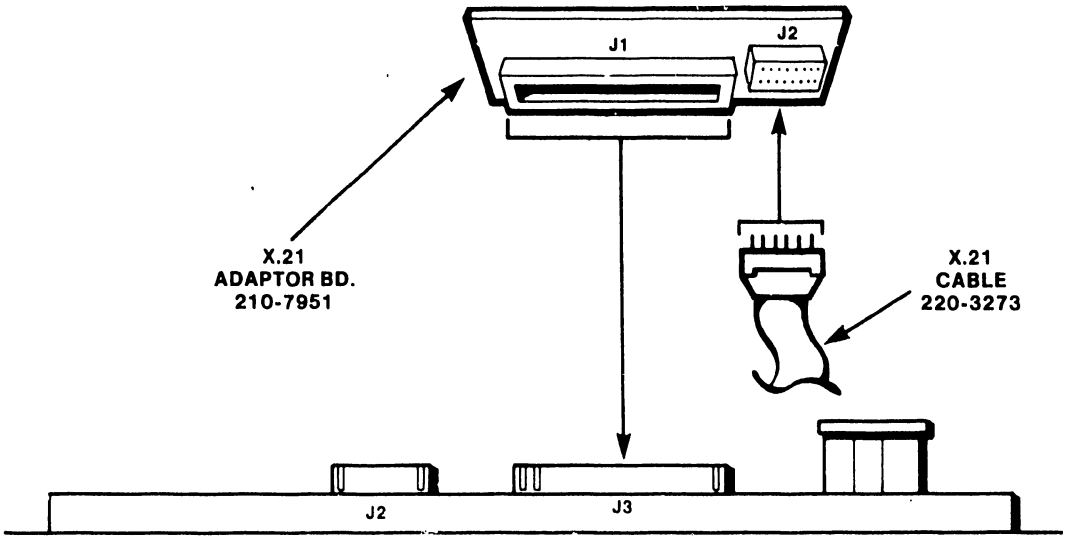


Figure 4-35 X.21 Interface Adaptor Board Installation

4.8 MASTER POWER-ON PROCEDURE

Perform the following power-on procedure to operate the system. This procedure applies to all systems.

1. Position the disk select switch on the master to indicate the location of the system disk (OIS only).

2. Set the power switch on the master processor or TCP - ON.

3. Power Up all system peripheral devices (OIS 140 Class Masters only).

4. Refer to Paragraph 5.4.1, for a description of TCB-1 Power-Up Diagnostics and Paragraph 5.4.3, for a description DLP 64/128 (TCB-3 64K/128K) Power-Up Diagnostics, in the event of a suspected fault condition.

4.9 INTERCONNECTION WITH MODEMS/ACU

One standard modem interface cable is provided to connect the TC controller to the modem. A second cable may be provided for ACU connection. The part number and length of these cable are as follows:

Modem/ACU Cable	Part Number	Length
RS-232-C	220-0332	12 feet
RS-449	220-0248	20 feet
X.21	220-0274	12 feet
RS-366	220-0332	12 feet

Connect the cable from the appropriate connector located on the TC rear panel of the master unit to the connector on the modem. For most Bell modems, this connector is labeled "CUST. EQUIP".

4.10 OPTIONAL CABLES

For modem cable lengths longer than those specified in Paragraph 4.9, the following optional cables are available. Part numbers for these cables are also listed.

	Wang Part Number		
Length	RS-449-C	RS-232-C	X.21
25ft	120-2325-01	220-0333	120-2326-01
50ft	120-2325-02	220-0334	120-2326-02
100ft	120-2325-03	N/A	120-2326-03
350ft	120-2325-04	N/A	120-2326-04
500ft	120-2325-05	N/A	120-2326-05
750ft	120-2325-06	N/A	120-2326-06
1000ft	120-2325-07	N/A	120-2326-07

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

CHAPTER 5
PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 PREVENTIVE MAINTENANCE

Preventive Maintenance procedures do not apply to the TCB-1 and DLP 64/128 Controllers.

5.2 CORRECTIVE MAINTENANCE

The following Paragraphs provide reference to use and operation of Power Up Diagnostics and loopback test procedures for TCB-1, DLP 64/128 TC Controllers. Refer to Section 5.4 for more detail regarding Power Up Diagnostics. A description of EIA Interface Test Sets is also provided, this description applies to all Test Sets currently supported by Customer Engineering.

5.3 TROUBLESHOOTING CHECKLIST

The recommended sequence of troubleshooting the TC Controller is as follows:

1. Check all voltages in the TC Controller (Voltage measurement test points are located on the mounting bracket of the TC Controller board).

2. Run Power Up diagnostics described in section 5.4.

CAUTION Very little clearance is provided for these measurements. Avoid contact between test points and card rail as this may result in a short circuit.

3. Use a DVM (Digital Voltmeter) for all voltage measurements.

4. Position the system power switch to ON.

5. Measure the DC voltages at the test point on the TC Controller board, using GND as reference. The DC Voltage Measurements are:

Test Points	Limits
-12V	-11.8V to -12.2V
+12V	+11.8V to +12.2V
-5V	-4.9V to -5.1V
+5V	+4.9V to +5.1V

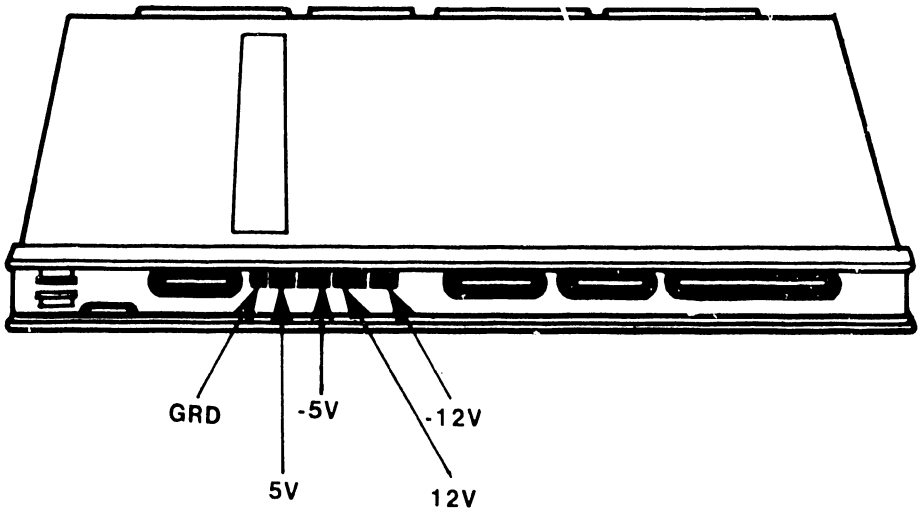


Figure 5-1 Voltage Test Points

5.4 POWER-UP DIAGNOSTICS

Power-Up Diagnostics are initiated after power to the TC controller (OIS Master/TCP or VS TCP) is set on, or after the controller is reset. All diagnostic tests will be executed with the exception of external loopback tests. To enable external loopback testing during power up, switches on the CPU Mother Board must be enabled depending on the communication interface in use. Refer to Paragraphs 5.4.2 and 5.4.4 for external loopback switch settings.

Power-Up diagnostics will verify RAM on the daughterboard, and all LSI components on the motherboard including the Z80-CTC (Counter-Timer Chip), Z80-SIO (Serial I/O Controller), and AM9517 DMA Controller. Options are provided for external loopback testing of the SIO, DMA, and ACU circuits. The interrupt circuitry involved with the "character monitor" is also tested. Upon successful completion of the power-up diagnostics, the data link circuitry is enabled. No data link control testing is done during power up.

5.4.1 TCB-1 Power-Up Diagnostics

Power Up Diagnostics allow for fault isolation to the memory bank and memory chip level through the use of the front panel LED's. Errors may be indicated by the on or off state of LED's 1 through 7. LED number 8 is a power indicator which blinks to indicate diagnostics are in progress or an error condition exists, and stays on solid when the operating system code is loaded and running.

Refer to Table 5-1 for front panel LED error information, Chart 1 for the memory bank and Chart 2 to isolate the faulty memory chip of the TCB - 1.

Table 5-1 TCB-1 LED Status Description

LED Status	Description
1-7 ON and 8 flashing (momentary)	Initial power-on or system reset.
1-7 OFF and 8 flashing	Power Up Diagnostic running no error.
1 ON and 1 or more of (2-7) ON solid and 8 flashing	Memory chip error detected.
1 OFF and 2 ON, 3-7 OFF and 8 flashing	Memory error not repairable by replacing RAM chip.
1-2 OFF, 3 ON and 8 flashing	Fault on motherboard.
1-6 OFF, 7 ON and 8 flashing	Waiting for IPL.
1-7 flashing sequentially and 8 ON	Controller idle. no code loaded diagnostics pass.
1-7 N.A. and 8 ON	Operating system code loaded and running.

1. If LED #1 is on solid and #8 is flashing a potential memory problem exists. Use chart #1 to identify the bank that contains the faulty chip.

LED 2	3	
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

Chart 1 - Bank Identification

2. The status of LED's 4, 5, 6 and 7 indicate which chip in the bank is faulty. Compare the LED indication on the TCB-1 to those in Chart #2 to find the faulty chip.

LED 4	5	6	7	
0	0	0	1	CHIP 1
0	0	1	0	CHIP 2
0	0	1	1	CHIP 3
0	1	0	0	CHIP 4
0	1	0	1	CHIP 5
0	1	1	0	CHIP 6
0	1	1	1	CHIP 7
1	0	0	0	CHIP 8
1	0	0	1	CHIP 9

CHART 2 - Chip Identification

3. Refer to Figure 5-2 for the location of memory chips specified by the LED's.

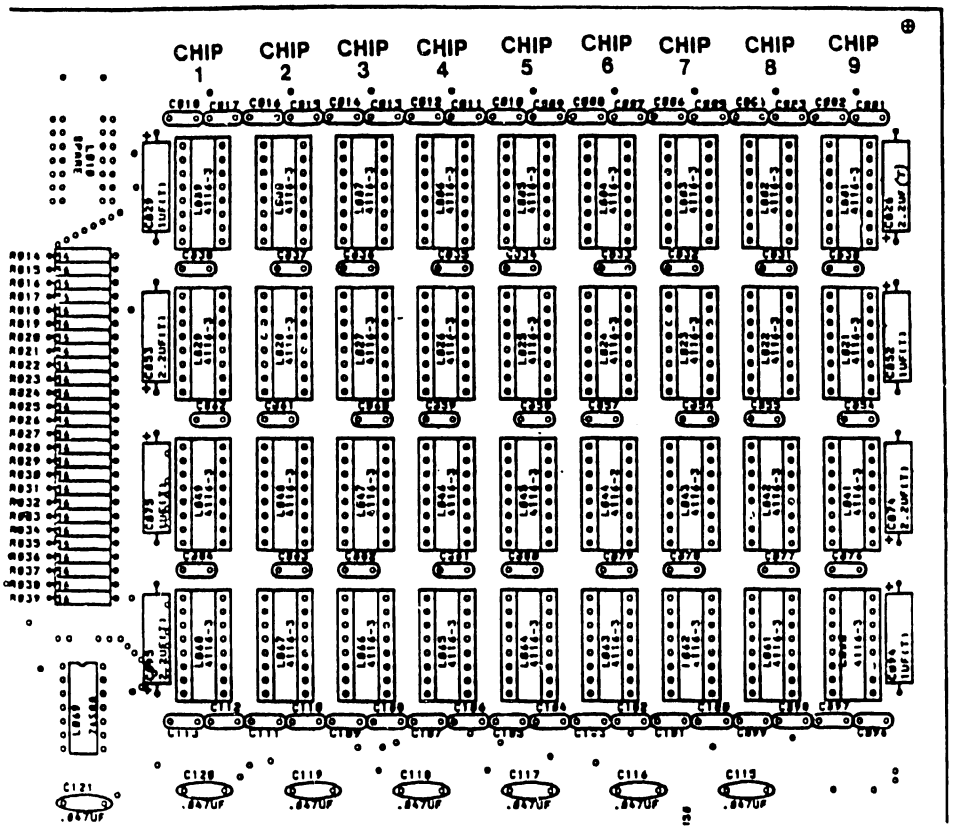


Figure 5-2 Memory Chip Layout

5.4.2 TCB-1 Loopback Test Procedure Requirements

Switches 6, 7, and 8 of switchbank #1 of the TCB-1 motherboard may be used in conjunction with power-up diagnostics to enable testing of the interface connector. Refer to Table 5-2.

Install the Loopback Connector on the corresponding rear panel connector and set the system ON to enable loopback testing.

The following loopback connectors are available for TCB-1 loopback testing.

RS 449	(P/N 270-3193)
RS 232-C/RS 366	(P/N 420-1041)

Table 5-2 TCB-1 Loopback Test Switch Settings

Switch	Test Enable Description
SW 8	ON: Loop on Power-Up Sequence. OFF: Enable data link for operating system.
SW 7	ON: RS 232-C/RS 366 External Loopback and Loopback Testing enable. OFF: Skip RS 232-C/RS 366 Loopback Tests.
SW 6	ON: Enable RS 449 Loopback Testing. OFF: Disable RS 449 Loopback Testing.
SW 5	Must be on all times.
SW 1-4	Not used by Diagnostics.

5.4.3 DLP 64/128 Power Up Diagnostics

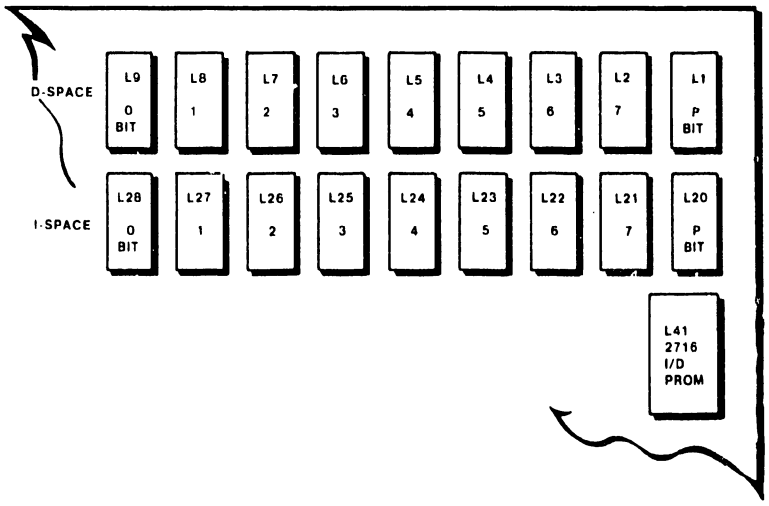
The following Paragraph describes use of DLP 64/128 Power Up Diagnostics to isolate fault conditions to the memory chip level through the use of Front Panel LED's. Refer to Table 5-5, for more detail regarding loopback testing.

Table 5-3 DLP 64/128 LED Status Description

LED Status	Description
1-7 ON and 8 flashing:	Initial power-on, system reset.
1-7 flashing sequentially and 8 ON:	Controller idle (no code loaded) diagnostics passed.
1-7 N.A and 8 ON:	Operating system code loaded and running.
1-6 OFF, 7 ON and 8 flashing:	Power Up Diagnostic completed without error.
1 ON and 8 flashing:	Diagnostic PROM, RAM addressing or Parity Generator Checker Failure. Motherboard fault.
1-5, 7 OFF, 6 ON and 8 flashing:	I/D PROM Checksum failure. Daughter Board fault.
1-5 OFF, 6-7 ON and 8 flashing:	Motherboard - CTC fault.
1-4, 6, 7 OFF, 5 ON and 8 flashing:	Motherboard - DMA fault.
1-4, 6 OFF, 5, 7 ON and 8 flashing:	Motherboard - SIO fault.
1-4, 7 OFF, 5-6 ON and 8 flashing:	Motherboard - X.21 or SIO failure.
1-4 OFF, 5-7 ON and 8 flashing:	Dead Man Timer failure.
1-3, 5-7 OFF, 4 ON and 8 flashing:	I/D PROM switching failure.
1-3, 6 OFF, 4,7 ON and 8 flashing:	SIO/DMA transfer failure.
1-3, 5, 7 OFF, 4, 6 ON and 8 flashing:	Loopback failure.
1-3, 5 OFF, 4, 6, 7 ON and 8 flashing:	Vector RAM failure.
1-3, 6-7 OFF, 4, 5 ON and 8 flashing:	Character Monitor failure.
1-3 OFF, 4, 7 and ON 8 flashing:	Interrupt Vector failure.
1 ON, 2 (OFF=I Space RAM, ON=D Space RAM), 3 OFF, 2-4-5-6 or 7 ON, 8 flashing:	Memory chip error detected refer to Table 5-4.

Table 5-4 Memory Chip Detect

Flashing LED Indicator = ON 2	3	4	5	6	7	Faulty Memory Chip Location	
	OFF				ON	L28	Refer to Figure 5-3.
	OFF			ON		L27	
	OFF			ON	ON	L26	
	OFF		ON			L25	
	OFF		ON		ON	L24	
	OFF		ON	ON		L23	
	OFF		ON	ON	ON	L22	
	OFF	ON				L21	
	OFF	ON			ON	L20	
ON	OFF				ON	L09	
ON	OFF			ON		L08	
ON	OFF			ON	ON	L07	
ON	OFF		ON			L06	
ON	OFF		ON		ON	L05	
ON	OFF		ON	ON		L04	
ON	OFF		ON	ON	ON	L03	
ON	OFF	ON				L02	
ON	OFF	ON			ON	L01	



	I-SPACE	D-SPACE	I/D PROM
DLP 64 210-7962-1A	L20-L28	N/A	N/A
DLP 128 210-7962-A	L20-L28	L1-L9	378-4416

MEMORY LAYOUT DLP 64/128

Figure 5-3 I and D Space RAM

5.4.4 DLP 64/128 Loopback Test Requirements

Access switchbank #1 on the CPU Motherboard to enable Loop on Power Up testing and to select RS 232-C/RS 366, RS 449 and/or X.21 external loopback testing.

Loopback Testing is used in conjunction with power-up diagnostics to enable testing of the interface connector. Also selectable is Loop On Error a repair aid function only.

The following loopback connectors are available for DLP 64/128 loopback testing.

RS 449	(P/N 270-3193)
RS 232-C/RS 366	(P/N 420-1041)
X.21	(P/N 421-0010)

Table 5-5 DLP 64/128 Loopback Test Switch Settings

Switch	Test Enable Description
SW 8	ON: Loop On Power-Up, and external loopback test. Switch 8 when used in conjunction with switches 1, 2, 3, and 7 will enable loopback testing. Refer below for test selection.
SW 7	ON: X.21 TXDB spacing output select. When setting switch 8 ON for external Loop testing of the X.21 connector Switch positions 3 and 7 must also be ON. OFF: RS449 TXDB marking output select.
SW 6	ON: DLP128 Configuration. OFF: DLP64 Configuration.
SW 5	ON: With SW 6 ON DLP128 Configuration. ON: With SW 6 OFF DLP64 Configuration.
SW 4	ON: With SW 8 ON Loop On Error. ON: With SW 8 OFF no meaning.
SW 3	ON: With SW 8 ON and SW 7 OFF = RS449 External Loopback. ON: With SW 8 ON and SW 7 ON = X.21 External Loopback.
SW 2	ON: With SW8 ON = RS 232-C/RS 366 External Loopback.
SW 1	ON: With SW 8 ON = RS 232-C External Loopback.
SW 1, 2, 3	ON: With SW 8 ON & SW 7 OFF = RS 232-C/RS 366, & RS 449 External Loopback. ON: With SW 8 & SW 7 ON = RS 232-C/RS 366, & X.21 External Loopback.

5.5 EIA INTERFACE TEST SET AND BREAKOUT BOXES

An EIA Interface Test Set or "Breakout Box", is a self-contained pocket size test set that can be inserted between the Data Communication Equipment (DCE) or modem and Data Terminal Equipment (DTE). Breakout Boxes allow the user to monitor the interface signals and to isolate and identify sources of trouble.

A Breakout Box contains indicators which continuously monitor the level of the EIA sensing circuits which drive LEDs to indicate the ON or OFF levels of the following EIA signals - transmitted data, received data, request to send, clear to send, data set ready, received carrier detect, data terminal ready, signal quality detect and ring indicator.

Two indicators also monitor the transmit and receive clock signals. Two additional uncommitted indicators are available for monitoring either positive or negative levels on any of the interface lines.

Breakout Boxes also contain 24 switches which allow any of the interface signals except line one, (Frame Ground) to be interrupted. These switches are physically located in the center of the front panel and functionally divide the test set into two halves. One half contains a cable and connector for connecting the test set to the DCE (data communications equipment) or modem. The other half of the Test Set contains a connector to which the DTE (Terminal or CPU) can be connected .

Twenty five pins are located on both sides of the switches. These pins permit monitoring of any of the interface lines with either or both the positive and negative test indicators with jumpers supplied or probing with an external meter or oscilloscope.

To operate a test set the EIA RS-232 interface cable from the modem is unplugged and plugged into the Test Set 25-pin female connector labeled "To DCE" (data communications equipment). The Test Set male connector, labeled "To DCE" is then connected directly to the modem.

CHAPTER 6 SCHE-MATICS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

CHAPTER 7
ILLUSTRATED
PARTS BREAKDOWN

7.1 PARTS LIST BREAKDOWN

The following list provides part numbers and a page reference for replaceable assemblies used on OIS and VS Systems, including TC Controllers, interface cables and Lamp Boards.

Description	Part No.	Fig Reference
TELECOMMUNICATION CONTROLLERS		
TCB-1	212-3014	
DLP-64	212-3040	
DLP-128	212-3038	
X.21 Interface Adapter Board	210-7951	4-11
INTERNAL INTERFACE CABLES		
OIS 105-130A		
RS-232	220-3129	4-19
RS-366	220-3174	4-19
RS-449	220-3125	4-19
X.21	220-3223	4-10, 4-11
OIS 140/145		
RS-232	220-3129	4-8
RS-366	220-3174	4-8
RS-449	220-3125	4-8
X.21	220-3223	4-10
OIS 40/50		
RS-232	220-3303	4-23
RS-366	220-3304	4-23
X.21	220-3305	4-24
TCP		
RS-232	220-3179	4-31
RS-366	220-3180	4-31
RS-449	220-3178	
X.21	220-3223	4-32

Description	Part No.	Fig Reference
FRONT PANEL LAMP (LED) BOARDS (w/o LED's		
OIS 105-130	210-7865	4-14
OIS 140/145	210-7665	4-6
OIS 40/50	210-7865	
TCP	210-7865	
LED (for above PCB's)	370-0031	N/A
LAMP BOARD CABLES		
OIS 105-130	220-3171	4-14
OIS 140/145	220-3171	4-6
OIS 40/50	220-3306	
TCP	220-3171	
BNC/TNC CABLES		
OIS 105-130	220-16484-19	
OIS 140/145	220-16484-8	
OIS 40/50	220-2002	
TCP	220-1710	

CHAPTER 8 TROUBLE-SHOOTING

CHAPTER 8
TROUBLESHOOTING

Troubleshooting Flowcharts will be provided at a later date.

APPENDIX A

MODEM INTERFACE SIGNALS

APPENDIX A
MODEM INTERFACE SIGNALS

EIA-RS 232-C

RS-232-C provides an interface between the data terminal equipment (DTE) - and the data communications equipment (DCE) - typically a modem, employing serial binary data interchange. The following paragraphs describe the RS-232-C modem interface signals. The modem must be in the data mode when checking the control signals.

Table A-1
Summary of RS 232-C Interface Signals

Pin	Circuit	Circuit Name	Function	Source
1			Protective Ground	
2	BA	TXD	Transmitted Data	DTE
3	BB	RXD	Received Data	DCE
4	CA	RTS	Request-To-Send	DTE
5	CB	CTS	Clear-To-Send	DCE
6	CC	DSR	Data Set Ready	DCE
8	CF	RLSD	Received Line Signal Detector	DCE
15	DB	TC	Transmitter Signal Element Timing	DCE
17	DD	RC	Receiver Signal Element Timing	DCE
20	CD	DTR	Data Terminal Ready	DTE

NOTE

The ON condition = (+3 to +25V), the OFF condition = (-3 to -25V).

Pins 1 and 7 are electrically bonded to the chassis and reference ground.

Transmitted Data - Signals on this circuit are generated by data terminal equipment (DTE) and are transferred to the local transmitting signal converter for transmission of data to remote data terminal equipment. The data terminal equipment will not transmit unless an ON condition is present on all of the following circuits:

Circuit CA (Request to Send)
Circuit CC (Data Set Ready)
Circuit CB (Clear-To-Send)

Circuit CD (Data Terminal Ready)

NOTE:
Circuit CF (RLSD) may be required by some modems before transmitting data.

Received Data - Signals on this circuit are generated by the receiving signal converter in response to data signals received from remote data terminal equipment via the remote transmitting signal converter.

Request to Send - The DTE presents this circuit On when the terminal intends to transmit data. Once this signal is present, the DTE must wait for circuit CTS (Clear to Send) before starting data transmission.

Clear To-Send - Signals on this circuit are generated by the data set to indicate whether or not the data set is ready to transmit data. The ON condition together with the ON condition on Circuits CA and CC (Request to Send and Data Set Ready) and if implemented Circuit CD (Carrier Detect), indicates that signals present on circuit Transmitted Data will be transmitted to the communication channel. The OFF condition is an indication to the DTE that it should not transfer data across the interface to Circuit BA (Transmitted Data).

Data Set Ready - Signals on this circuit are used to indicate the status of the local data set. The ON condition off this circuit indicates that the local data communication equipment (DCE) is connected to a communication channel ("OFF hook" in switched service) and the local DCE is not in test (local or remote), or dial mode. The ON condition also indicates that any timing functions required by the switching system to complete a call have been completed.

Received Line Signal - The ON condition of this circuit indicates the DCE is Detector (carrier) receiving a signal which meets the criteria established by the DCE manufacturer. The OFF condition indicates that no signal is being received or that the received signal is unsuitable for demodulation.

Transmitter Signal Element Timing - Signals on this circuit are used to provide the DTE with signal element timing information. The DTE will provide a data signal on Circuit BA (Transmitted Data) in which the transitions between signal element timing nominally occurs at the time of the transitions from OFF to ON of this circuit.

Receiver Signal Element Timing - Signals on this circuit are used to provide the DTE with received signal element timing information. The transition from ON to OFF will nominally indicate the center of each signal element on Circuit BB (Received Data). Timing information on this circuit will be provided at all times when Circuit CF (Received Line Signal Detector) is in the ON condition.

Data Terminal Ready - Signals on this circuit are used to control switching of the DCE to the communications channel. The ON condition prepares the DCE to be connected to the communications channel amd maintains the connection established (e.g. manual call origination, manual answering or automatic call origination.

X.21 Interface

X.21 is general purpose interface between the data terminal equipment (DTE) and data communication equipment (DCE), for synchronous operation on public data networks. Signals that specify the DTE/DCE interface that are supported by X.21 are enabled through a 15 pin connector of which eight are used as specified below.

Table A-2
Summary of X.21 Interface Signals

Pin	Circuit Name	Circuit	Source
1	Protective Gnd	G	
8	DTE ground rtn	Ga	DTE
2,9	Transmit	T	DTE
4,11	Receive	R	DCE
3,10	Control	C	DTE
5,12	Indication	I	DCE
6,13	Signal Element Timing	S	DCE
7,14	Byte Timing	B	DCE

Transmit - Signals on this circuit are generated by the DTE. As well as being used for the transmission of data or selection sequences to the DCE, this circuit may be held in a steady logic state of 0 or 1 together with on or off conditions of the control circuit (C) to signal DTE conditions or states.

Receive - Signals on this circuit are generated by the DCE. The signals may be generated in response to signals received from a remote data set, generated locally by the DCE as response or control information to the DTE or held in a steady logic state of 0 or 1 together with on or off condition of the indication circuit (I) to signal DCE conditions or states.

Control - Signals on this circuit are generate by the DTE. The on or off conditions of this circuit are used together with steady logic states (0 or 1) on the Transmit circuit to signal DTE conditions.

Indication -	Signals on this circuit are generated by the DCE. The on or off conditions of this circuit are used together with steady logic states (0 or 1) on the Receive circuit to signal DCE conditions.
Signal Element Timing	Signals on this Circuit are generated by the DCE. The signals are used for bit rate timing for the DTE.
Byte Timing -	Signals on this circuit are generated by the DCE and are optional. The signal provides byte boundaries for call control character alignment.
Signal Ground	
DTE Common GD.	

Unlike RS232 or RS449, where a DTE's or DCE's condition or state is signaled via a unique control line (ie Request To Send), X.21; uses the T, R, C and I lines to signal encoded state conditions. This is accomplished by the DTE or DCE sending steady logic conditions 0 or 1 on circuits T or R, together with associated conditions (ON or OFF) on circuits C or I, for a period of at least 24 bit intervals. Table A - lists X.21 signaling conditions and associated states:

Table A - 3
X.21 Signaling Conditions and States

State	Circuit				Description
	T	R	C	I	
	1		Off		DTE Ready
	0		Off		DTE Uncontrolled Not Ready
	0		Off		DTE Controlled Not Ready (a 0/1 pattern is transmitted on T circuit)
		1		Off	DCE Ready
		0		Off	DCE Not Ready
1	1	1	Off	Off	Ready (DTE and DCE are Ready)
2	0		On		Call Request
3		X		Off	Proceed to Select (X = DCE transmits contiguous "+" characters preceded by 2 or more SYN characters)
4	X		On		Selection Signal Sequence (X = DTE transmits selection sequence preceded by 2 or more SYN characters)
5	1		On		DTE Waiting
6		X		Off	DCE Waiting (X = DCE transmits 2 or more SYN characters)
7		X		Off	Call progress signal sequence (x = DCE transmits 1 or more call progress blocks
8		X		Off	Incoming Call (X = DCE transmits continuous BEL character preceded by 2 or more SYN characters
9	1		On		Call accepted (DTE accepts incoming call)
10		X		Off	DCE provided information sequence (X = DCE transmits 1 or more DCE provided information blocks)
11		1		Off	Connector in progress (DCE Ready - entered when connection is in progress)

Table A-3 (cont'd)
X.21 Signaling Conditions and States

State	Circuit				Description
	T	R	C	I	
12		1		On	Ready for Data (DCE signals that connection is available for data transfer
13	X	X	On	On	Data Transfer (X = data transfer on circuits T and R.)
14	0	1	Off	Off	Quiescent State - DTE signals controlled not ready and DCE signals ready, simultaneously
15	0	X	On	Off	Call collision - DTE detects incoming call in response to call request
16	0		Off		DTE Clear Request to DCE
17		0		Off	DCE clear confirmation (DCE response to state 16)
18	1	0	Off	Off	Quiescent State - DTE signals ready and DCE signals not ready, simultaneously
19		0		Off	Clear Indication - DCE indicates clearing to the DTE
20	0		Off		DTE clear confirmation - response to state 19
21		1		Off	DCE ready - response to state 17 or 20.

RS-449-C Interface

RS-449 is a general purpose 37-position and 9 position interface for data terminal equipment (DTE) circuit equipment and data communications equipment (DCE) employing serial binary data interchange. The following paragraphs define the electrical signal characteristics of RS 449.

Table A-3 RS 449 Interface Summary

Pin	Circuit Mnemonic	Circuit Name	Source
19,37	Sg	Signal Ground	---
37	SC	Send Common	DTE
20	RC	Receive Common	DCE
28	IS	Terminal In Service	DTE
15	IC	Incoming Call	DCE
12,30	TR	Terminal Ready	DCE
11,29	DM	Data Mode	DCE
4,22	SD	Send Data	DCE
6,24	RD	Receive Data	DCE
17,35	TT	Terminal Timing	DCE
5,23	ST	Send Timing	DCE
8,26	RT	Receive Timing	DCE
7,25	RS	Request To Send	DCE
9,27	CS	Clear To Send	DCE
13,31	RR	Receiver Ready	DCE
33	SQ	Signal Quality	DCE
34	NS	New Signal	DCE
16	SF	Select Frequency	DCE
16	SR	Signaling Rate Selector	DCE
2	SI	Signaling Rate Indicator	DCE
10	LL	Local Loopback	DCE
14	RL	Remote Loopback	DCE
18	TM	Test Mode	DCE
32	SS	Select Standby	DCE
36	SB	Standby Indicator	DCE

Send Common - This conductor is connected to the DTE circuit ground.

Receive Common -This conductor is connected to the DCE circuit ground.

Terminal In Service - The ON condition indicates that the DTE is in service and in switched network applications that employs line polling allows incoming calls to be connected to the DCE. The OFF condition signals that the DCE is not available for service. This may be caused by a DTE test condition.

Incoming Call - The ON condition indicates that an incoming call is being received by the DCE. The OFF condition is maintained during the OFF segment of the ringing cycle.

Terminal Ready - Signals on this circuit are used to control switching of the DCE to and from the communications channel.

Data Mode - The ON condition of this circuit indicates that the DCE is transmitting. The OFF condition is an indication that the DTE is to disregard signals appearing on all other interchange circuits with the exception of Circuit IC (Incoming Call), Circuit TM (Test Mode) and Circuit SB (Standby Indicator).

Send Data - The data signal originated by the DTE to be transmitted via the data channel to one or more remote data stations are transferred on this circuit to the DCE.

Receive Data - The data signals generated by the DCE in response to data channel line signals received from a remote data station are transferred on this circuit to the DTE.

Terminal Timing - Signals on this circuit provide the DCE with transmit signal element timing information.

Send Timing - Signals on this circuit provide the DTE with transmit signal element information.

Receive Timing - Signals on this circuit provide the DTE with receive element timing information.

Request to Send - Signals on this circuit control the data channel transmit function of the local DCE and, on a half duplex channel control the direction of data transmission of the local DCE.

Clear To Send - Signals on this circuit indicate the transmit enable state on the data channel.

Receiver Ready - Signals on this circuit indicate that the DCE receiver may or may not be conditioned to receive data signals from the communication channel.

Signal Quality - Not supported

New Signal - Not supported

Select Frequency - Signals on this circuit are used to select the transmit and receive frequency bands of a DCE.

Signaling Rate Detector - Signals on this circuit are used to select one of the two data signaling rates of a dual rate synchronous DCE or to select one of the two ranges of data signaling rates of a dual range non-synchronous DCE.

Signaling Rate Indicator - Not supported.

Secondary Send Data (To DCE) - Not supported.

Secondary Receive Data (From DCE) - Not supported.

Secondary Request To Send (To DCE) - Not supported.

Secondary Clear To Send (From DCE) - Not supported.

Secondary Receiver Ready (From DCE) - Not supported.

Local Loopback (To DCE) - Not Supported.

Remote Loopback - Not supported.

Test Mode - Not supported.

Select Standby - Not supported.

RS-366 Interface

RS-366 provides an interface between data terminal equipment (DTE) and Automatic Calling Equipment (ACE) for data communication. The following paragraphs define the signal characteristics of RS 366. RS 366 is enabled through a 25 position connector.

Table A-4 RS-366 Interface Summary

Pin	Circuit Mnemonic	Circuit Function	Source
7	SG	Signal Ground	
18	RC	Receive Common	
19	SC	Send Common	
4	CRQ	Call Request	DTE
6	PWI	Power Indication	ACE
22	DLO	Data Line Occupied	ACE
13	DSC	Distant Station Connected	ACE
3	ACR	Abandon Call & Retry	ACE
5	PND	Present Next Digit	ACE
2	DPR	Digit Present	DTE
14	NB1	Digital Signal Circuit 1	DTE
15	NB2	Digital Signal Circuit 1	DTE
16	NB4	Digital Signal Circuit 1	DTE
17	NB8	Digital Signal Circuit 1	DTE

Signal Ground - This conductor directly connects the DTE circuit ground to the ACE circuit ground to provide a conductive path between the DTE and ACE signal commons.

Send Common - This conductor is connected to the DTE circuit ground and is used at the ACE as a reference potential for the interchange circuit receivers.

Call Request - Signals on this circuit are generated by the DTE to request the ACE to originate a call. The OFF condition indicates that the DTE is not using or has completed use of the ACE.

Power Indication - Signals on this circuit indicate whether power is available within the ACE.

ated modem is Off Hook or the associated telephone is in use. The OFF condition indicates that the DTE may originate a call provided that Circuit PWI is ON.

Distant Station Connected - Signals on this circuit indicate whether a connection has been established to a remote data station.

Abandon Call and Retry - Signals on this circuit are used to indicate whether a preset time has elapsed between successive events in the calling procedure. The ON condition indicates that the call should be abandoned.

Present Next Digit - Signals on this circuit are generated by the ACE to control the presentation of digits on Circuits NBV1, NB2, NB4, and NB8 (digits of a called number) (digits used for control purposes).

Digit Present - Signals on this circuit are generated by the DTE to indicate that the ACE may read the code combination presented on Circuits NB1, NB2, NB4, and NB8.

Digit Signals Circuits (NB1-NB8) - Parallel logic signals generated by the DTE that represents the digits of a dialed number or parallel logic signals that are used locally for control purposes.

CHAPTER 6 SCHE-MATICS

CHAPTER 6
SCHEMATICS

6.1 SCHEMATICS

TC controller schematics are provided for the TCB-1, DLP 64, DLP 128 and two Lamp Board assemblies. The Controller Schematics contain motherboard/daughterboard set.

TCB-1/DLP-64	CPU Motherboard	210-7763
	Data Link and Memory Board	210-7762
DLP 128	Motherboard	210-7963
	Daughterboard	210-7962
OIS 40/50, 105-130, VS TCP	Lamp Board	210-7865
OIS 140/145	Lamp Board	210-7665

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HOLE LEGEND & TOLERANCES

HOLE DIA		TOLERANCE	
0.125	0.173	± .003	.003
0.136	0.250	± .004	.004
0.251	0.500	± .005	.005

ITEM	DESCRIPTION	QTY
1		

INT (2D1)

RESET (4B6)

WAIT (4F5)

Φ 250 (4B10)

BUSRQ (4B9)

+5VR

±0V

ENMI (2B11)

R72A 4.7K

L98 Z80A-CPU

RESET, WAIT, Φ, BUSRQ, Vcc, GND, NMI, PA0–PA15, D0–D7

Φ500 (4C10)

L94 8517A

READY (4C9)

DREQ0 (2G2)

DREQ1 (2G4)

DREQ2 (2G2)

DREQ3 (2G4)

READY, CLK, CS, RESET, DREQ0–DREQ3, DB0–DB7, ADSTB, HREQ (4B10), MEMW

R41 68Ω, C57 270pF ±0V

L68 LS373

DB0–DB7, D1–D7, BUSAK (1D10), OC, ENB

PA0–PA15

L95 2732 INTEL

DPO (4D2), CE, OE/VPP, A11, VCC, VSS, +5VR ±0V

PA11

C/G (4D5)

Σ_E → EVEN Σ (4C6)

Σ_O → ODD Σ (4D6)

INT

PA0 → PA15 (4G10)(2G11)

L92 Z80A/CTC

CS0, CS1, RESET, Φ 250 (4B10), CE, DCTC (4E2), M1 (1D10), IORQ (1B6), RD, IEI, IEO, Φ 500 (4C10), CLK/TRG0–CLK/TRG3, ZC/TO0–ZC/TO2

INT, D0–D7

AD (4E6)

TPB

R50 2.2K

IxC (1E2)

L88 LS74

PR, D1, CLR1, Q1, CLK1

L103 125

WR (2D5) (4E8)

MEMW (2C7)

R40 10K +5VR

+5VR R58 2.2K ALT Vcc

R44 2.2K

BK2 (4B9)

AEN

L87 LS04

HALT, BUSAK, AD, M1, MREQ, IORQ, RFSH, WR

BUSAK (1F7)

M1 (4F7)(1F4)

MREQ (4C6)

L86 LS08

MEMR, WAIT

DACK0–DACK3 (2E4)

EOP

R57 4.7K +5VR

RG9 10K +5VR

DDMA (4F2)

L89 LS367

IOR, IOW

RESH (2E1)

R68 10K, R66 10K

READY (4C9)

R42 10K +5VR

R43 10K +5VR

MWAIT (4D9)

L102 LS32

R63 10K +5VR

R65 10K +5VR

R64 10K +5VR

L64 LS08

ZRD (4F8)

DACKR (2E3)

DACKT (2E5)

DI/OW

IOR

DSIO (4G2)

IORQ (4A10) (1F4) (4E9)

L52 LS157

SIOCE, SIORD, IEO (2D1), A, B, 1A–4A, 1B–4B, 1Y–4Y, STB

L69 Z80A SIO-2

RD, M1, RTSIO (4B5), Φ 250 (4B10), B/A, C/D, RESET, W/RDYA, W/RDYB, TxDA, TxDB, RxDA, RxDB, IORQ, SYNCA, SYNCB, DTRA, DTRB, CE, RTSA, RTSB, IEI, IEO, VDD, GND, +5VR ±0V

W/RDYA (2F4)

W/RDYB (2F5)

TxDB (3F7)

DTR (3C6) (3E8)

L532 L18

ERTS (2G7)

RTS (3E8)(3B6)

L532 L62

EOPR (2G3)

EOPT (2G6)

L86 LS08

PP1, PP0, SEL

L86 LS08

PP1, PP0

L89 LS04

L86 LS08

IxC (1E2)

RxCA, TxCA, RxDA, TxCB, RxCB, RxDB, CTSB, CTSA, DSR, DCDA, RI, DCDB

RxDA (3F5), TxCB (3C7), RxCA (3D6), CTSB (3D10), DSR (3F8), RI (3F8), DCDA (3F8)

INT, IEO

L86 LS08

W/RDYA, W/RDYB

RSTSIO (4B5), Φ 250 (4B10), RESET

TxDA, RTSA, TxDB, SYNCA, DTRA, DTRB, RTSB

L532 L18

DTR (3C6) (3E8)

ERTS (2G7)

L532 L62

EOPR (2G3)

EOPT (2G6)

L532 L18

RTS (3E8)(3B6)

PAØ, PA1, RESET, CS0, CS1, Φ 250 (4B10), DCTC (4E2), M1 (1D10), IORQ (1B6), RD, SIEO, Φ 500 (4C10), CLK/TRG0–CLK/TRG3, ZC/TO0–ZC/TO2

INT, D0–D7

+5VR ±0V

LLO, PND, ACR, PWI (1B7, 1F7, 5F7, 1I7)

R1 L13 LS194

PWI, TM (3B10), ACR, R1 (1F8), PND, LLO, COS (3F10), XMPE (4A5)

L32 LS240

+5VR

R6 2.2K ONE (4C9)

L9 LS74

PR, D1, CLR1, Q1, CLK1

PCO

DAC11 (2G9)

L132

D0, D1 (4D4) (4F3) (2B8)

IxC (1E5)(3D8)

BK1 (4D9)

WR

L50 LS240

CK

D0–D7, 1A1–2A4, 1Y1–2Y4, 1G, 2G, TTS, 2S

RD3–RD0, BD3–BD0, NB4–NB1

L31 LS273

1D–8D, CLR, 1Q–8Q

DPR (3A9)

SF/RE (3C3)

NB1, NB2, NB4, NB4 (3B9)

CRQ (3B9)

BD0 – BD7 (2G11)

RESET

TP1

BUSEN (4D6)

RD

L99 LS245

DIR, G, A1–A8, B1–B8

D0–D7

M0, M1, M2, M3, M4, M5, M6, M7

TP2 R1 4.7K +5VR

SEE SHEET 6

REVISION

NO	DATE	BY

	BY	DATE	APPROVED BY	DATE
DWN	GK	2-27-81	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL —

MODEL NO TCB-1

SEE ENGRG SPECIFICATIONS No. —

FINISH —

TOL EX AS NOTED

XX ± FRAC ±

XXX ± ANG ± FINISH √

SCALE — SHT 1 OF 6

TITLE CPU MOTHERBOARD

SEE CHART | D | 7763 | 1

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

2₃ WR

B₃ ZRD

13₁ MRFSH

C₄ M1

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HOLE LEGEND & TOLERANCES

HOLE #	TOLERANCE
.013" - .125	± .003
.126 - .250	± .004
.251 - .386	± .005

SYM	DESCRIPTION	QTY
A		

PA0-PA3 (1G4)
BD0-BD7 (1C2)
+5VR
+10V
-10V
+5V
GND
VCC
RESET (4B6)
EDMT
EOPT (1A5)
EODR (1B5)
DREQ3 (1E9)
DREQ1 (1F9)
DREQ2 (1F9)
DREQ0 (1F9)
DEXTD (4E2)
ERTS (1C4)
ENMI
DACU (1E2)
DDMT
DVMR
DATC
DARC
DNTC
DNRC
DVMC
VM10
VM11
VM12
VM13
VM14
VM15
VM18
VM19
BUFOFF
INTALL
CLRINT
MASMON
CHARMON
MAP OUT
PRMNOP (4F6)
DRBUS (4C6)
WR (1E6)
W/RDYB (1D4)
W/RDYA (1D4)
DDMA (4F2)
DACK1 (1D9)
DACK3 (1C9)
DACKT (1C7)
DACK0 (1D9)
DACK2 (1C9)
DACKR (1C7)
INTA (4C7)
INT (1G11)
PAIREQ (4A7)
OVFL
VBEN
MEMW (1D9)
MRDY (9C10)
RD (4E6)
SMWR
D0-D7 (1E1,3F3) (4B2)
XMI
ENMI (1E11)
RESET (1C10)
RESET (4A6)
MFCA
MA0-MA15
VA0-VA9
VA18
VA19
RASEL
RD/WR
STB SEL
L82 LS158
L83 LS158
L81 LS158
L63 LS138
L66 LS273
L49 LS273
L79 2114-A
L80 2114-A
L93 LS245
L30 LS175
L76 5225
L77 5225
L78 LS174
L59 LS74
L39 LS73
L29 LS74
L47 LS74
L45 LS74
L61 LS74
L103 125
L40 LS02
L41 LS260
L42 LS20
L43 LS00
L44 LS08
L46 LS08
L47 LS04
L48 LS02
L49 LS00
L50 LS04
L51 LS32
L52 LS32
L53 LS32
L54 LS32
L55 LS32
L56 LS32
L57 LS32
L58 LS00
L65 LS266
L67 LS266
L68 LS266
L69 LS266
L70 LS266
L71 LS266
L72 LS266
L73 LS266
L74 LS04
L75 LS27
L76 LS27
L77 LS27
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L92 LS27
L93 LS27
L94 LS27

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DO NOT SCALE

HOLE LEGEND & TOLERANCES

SYM	DESCRIPTION	QTY
	HOLE DIA / TOLERANCE	
	.035 .125 ± .003 .004	
	.128 .190 ± .004 .004	
	.234 .500 ± .005 .005	

RS232 (2F1) → L33 75154 → L34 LS244 → RxD, DCDA(1D5), RI(1D5)(1F2), DSR(1D5)

BB (5) +5VR; DD (8) +5VR; DB (4) +5VR; COS (25) → COS(1F1)

AB (13) ±0V

CF (15) R17B 47K -12V; CE (18) R17A 47K 12V; CC (11) R17C 47K -12V; CB (9) R17D 47K -12V

AA (16) TO FRAME GND

CS (17) R15 100Ω; CS (16) R24 100Ω; RD (11) R29 100Ω; RD (10) R22 100Ω; RT (15) R16 100Ω; RT (14) R25 100Ω; ST (9) R25 100Ω; ST (8) R23 100Ω

L36 26LS32 → CTSB(1D5), RxD, RC, TC

RS449 (2F1) → ENB ENB ±0V

IC (29) RI; RC (2) TM (35); RR (25) R14 100Ω; DM (28) R23 100Ω

L35 26LS32 → DSR

L16 75154

TM(1G2)

RCA (3) → L7 LS79 → L8 LS73 → RxDA(1D5)

CONV (2F1) → L7 LS04 → L8 LS73

TxDB (1C4) → L7 LS04

CTSB → L7 LS04

RTS (1B4) → L15 75150

DTR (1C4) → L18 LS32

TxC → L14 75150

TxC (1E2)

Q1 MPS6512; Q2 MPS6518; R9 120Ω ½W 10% +12V; R5 68Ω; R10 120Ω ½W 10% -12V; C1 1500pf

RCEX (2F1); RCIN (2F1) → L28 LS51 → L9 LS04 → RxCA(1D5)

TCIN (2F1); TCEX (2F1) → L28 LS51 → L9 LS04 → TxCB(1D5)

TxD → L17 26LS31 → DA DB DC DD

DTR (1C4); RS449 (2F1) → L18 LS32; RTS (1B4); R13 2.2K ±0V

CRQ (1D1) → L9 LS04

NB1, NB2, NB4, NB8 (1D1)

L10 75150 (NB8); L11 75150 (NB2, NB4); L12 75150 (NB1); R4 4.7K -12V; R11 2.2K +5VR; TP5; R3 4.7K +12V; TP4

DPR (1D1) → L9 LS04

37 DPR; 27 NB1; 67 NB4; 47 NB2; 87 NB8; 77 CRQ

TRAP (4F9); NOP (4D7); MPE (4B7) → L1A LS08 → L7 LS32 → DSL (4E2)

C37B .1μF MYLAR; R30 3.6M; R29 3.3M; C37A .01μF; 555 TIMER → L84 14 → ACTIVE

DØ-D7 (1E1) (2B8) (4B2) → L91 LS374

R60 2.2K; R59 2.2K; R61 2.2K; R62 2.2K +5VR → L100 LS367

OPT (4E2)

SW2

81 PT4; F1 PT1; J1 PT2; PT3

L38 75150 ±0V -12V +12V → R27 3.3K; R26 4.7K ±0V → 515 SF/SR

SF/RE (1D1)

* HAND WIRE PER ECO # 23394

	BY	DATE	APPROVED BY	DATE
DWN	LEK	2-27-81	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL —//—

MODEL NO TCB-1

SEE ENGRG SPECIFICATIONS No.

TITLE CPU MOTHERBOARD

FINISH —//—

TOL ER AS NOTED

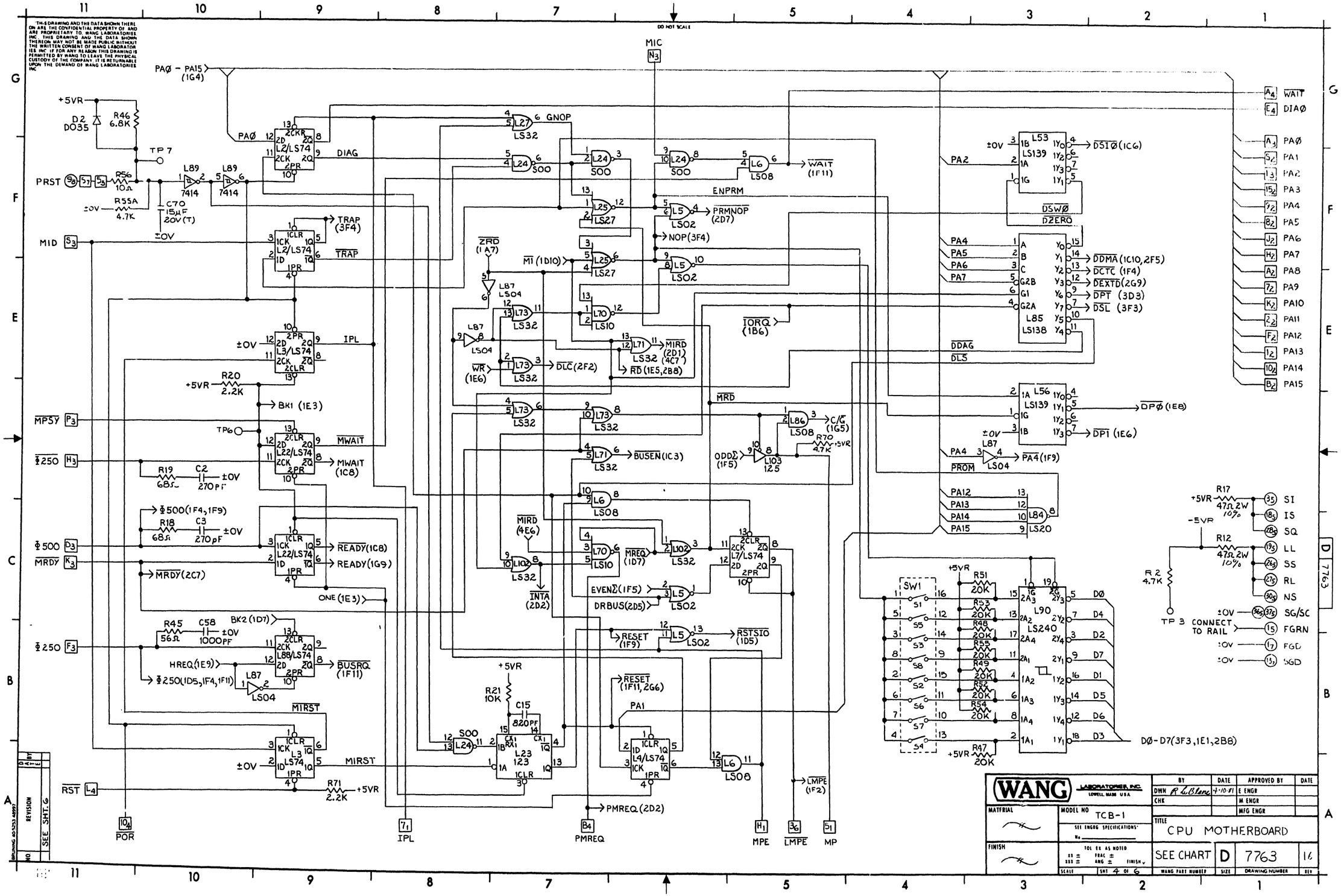
SCALE —//— SHT 3 OF 6

SEE CHART | D | 7763 | 16

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

D 7763

DATE | REVISION | SEE SHEET 6



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WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.	BY	DATE	APPROVED BY	DATE	
	DWN R. LeBlanc	4-10-81	E ENGR		
	CHK		M ENGR		
MATERIAL	MODEL NO TCB-1		MFG ENGR		
	SEE ENGRG SPECIFICATIONS No.		TITLE CPU MOTHERBOARD		
FINISH	TOL EX AS NOTED XX ± FRAC ± XXX ± ANG ± FINISH		SEE CHART	D	7763	16
	SCALE	SHT 4 OF 6	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

NO	REVISION	DATE	BY
	SEE SHT. 6		

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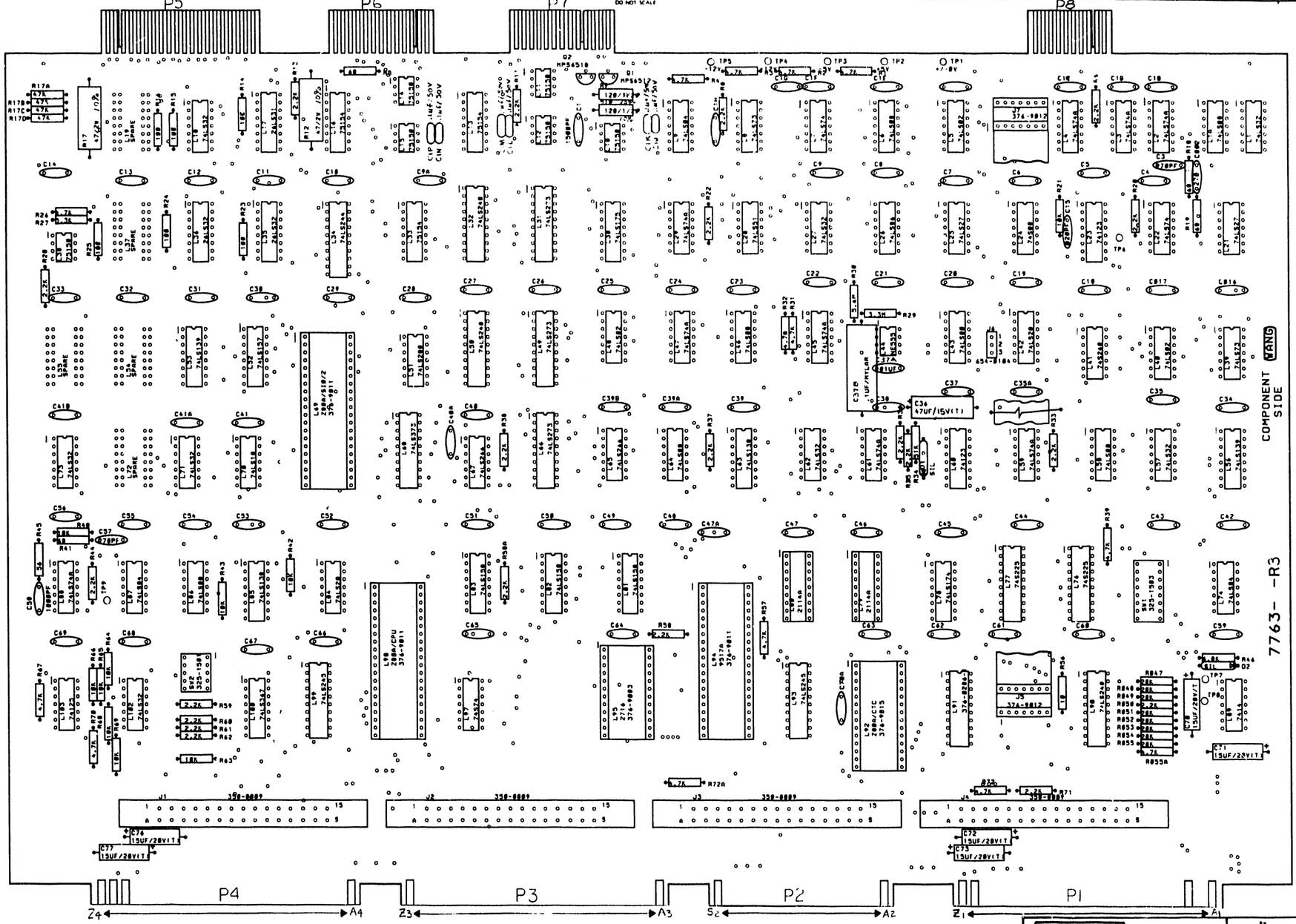

NOTES:

1. ALL CAPACITORS ARE .047μF CERAMIC EXCEPT AS NOTED.
2. L79 & L80 LOAD 18 PIN SOCKET 376-9014 (QTY. 2).
3. J1, J2, J3, & J4 ARE MOUNTED ON CIRCUIT SIDE.
4. TP1 THRU TP9 LOAD TERMINAL POST 654-1192 (QTY. 9).
5. ALL RESISTORS ARE 1/4W 10% EXCEPT WHERE NOTED.
6. J6 LOAD 3 PIN HEADER 654-0104. INSTALL 2 POS. SHUNT 350-4506 INTO HEADER.
7. J5 & J7 LOAD IC PAD 376-9008 (QTY. 2) UNDER 14 PIN SOCKET 376-9012 (QTY. 2).
8. ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

NO	REVISION	BY	DATE
	SEE SHEET 6		

	BY	DATE	APPROVED BY	DATE
DWN	SJ	4-2-81	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO TCB-1

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL EX AS NOTED
XX ± FRAC ±
XXX ± ANG ± FINISH

SCALE 1/1 SHT 5 OF 6

TITLE CPU MOTHER BOARD

SEE CHART | D | 7763 | R3

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

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LOCATION	TYPE	W.L. PART NO
L19,20, 37,54,55,72, 101	SPARE	
L2,3,4,7,22,29,45,47, 59,61,88	74LS74A	376-0155
L5,40,48	74LS02	376-0208
L6,46,64,86,1A	74LS08	376-0153
L8,39	74LS73	376-0304
L9,87,74	74LS04	376-0180
L10,11,12,14,15,38	75150	376-0076
L13,16,33	75154	376-0077
L17	26LS31	376-0470
L18,27, 57,62,71, 73 102,1	74LS32	376-0211
L23,60	74123	376-0080
L24	74S00	376-0228
L25,21	74LS27	376-0245
L26	74LS86	376-0231
L28	74LS51	376-0213
L30	74LS175	376-0160
L31,49,66	74LS273	376-0302
L32,50,90	74LS240	376-0297
L34	74LS244	376-0288
L42,84	74LS20	376-0210
L43,58	74LS00	376-0207
L44	NE555	376-0126
L51	74LS280	376-0242
L52	74LS157	376-0216
L53,56	74LS139	376-0226
L63,85	74LS138	376-0294
L65,67	74LS266	376-0148
L69	Z80A-SIO/2	SEE CHART
L70	74LS10	376-0209
L76,77	74S225	376-0323
L78	74LS174	376-0159
L79,80	2114A	SEE CHART
L81,82,83	74LS158	376-0293
L89	7414	376-0139
L91	74LS374	376-0286
L92	Z80A/CTC	SEE CHART
L93,99	74LS245	376-0285
L94	AM9517A	SEE CHART
L95	2732	SEE CHART
L98	Z80A-CPU	SEE CHART
L100	74LS367	376-0192
L103	74125	376-0324
L97	74S74	376-0202
L41	74S260	376-0206
L35,36	26LS32	376-0471
L68	74LS373	376-0310

COMPONENT	TYPE	W.L. PART NO.
J6	3 PIN HEADER	654-0104
	2 POS SHUNT	350-4506
C1J,1K,1L,1M,1N,1P	.1uF, 50V	300-1930

COMPONENT	TYPE	W.L. PART NO
R45	56Ω ¼W 5%	330-1057
R21,63-66,40,42, 43,68,69	10K ¼W 5%	330-4010
R1-4,26,31,32,39, 57,67,70,72,72A	4.7K ¼W 5%	330-3048
R5,18,19,41	68Ω ¼W 5%	330-1069
R6,8,11,13,2022,28, 50, 33,35-38,49,58-62,71	2.2K ¼W 5%	330-3023
R9,10	120Ω ½W 10%	331-2012
R12,17	47Ω 2W 10%	337-1047
R14-16,23-25	100Ω ¼W 5%	330-2011
R27	3.3K ¼W 5%	331-3034
R29	3.3M ¼W 5%	330-6034
R30	5.6M ¼W 5%	330-6057
R34	27K ¼W 5%	330-4028
R46	6.8K ¼W 5%	330-3069
R47-49,51-55,	20K ¼W 5%	330-4021
R56	10Ω ¼W 5%	330-1011
R17A 17B,17C,17D	47K ¼W 5%	330-4047
C1	1500pf 500V	300-1907
C58	1000pf 500V	300-1906
C3,57,58,2	270pf 500V	300-1270
C1A-C1H,4-14,C9A 16-35,35A37-56,39A,39B 40A,41A 41B,70A, 59-69	.047μF 50V	300-1966
C15	820pf 500V	300-1820
C36	100μf 10V (T)	300-4021
C70-73,76,77	15μf 20V (T)	300-4022
C37A	.01μF 25V	300-1903
C37B	.1μF 100V (M)	300-2270
R55A	4.7K ¼W 5%	330-3048
Q1	MPS6512	375-1012
Q2	MPS6518	375-1014
D2	SIL	380-1001
SW1	8 BANK ROCKER SW	325-1503
SW2	#5 STUD DIG SW	325-9005
L92	28 PIN SKT	376-9015
L69,94,98	40 PIN SKT	376-9011
L95	24 PIN SKT	376-9003
J1,2,3,4	30 PIN CONN	350-0009
L79,80	18 PIN SKT	376-9014
J5,7	14 PIN SKT	376-9012
	16 PIN IC PAD	376-9008

LOCATION	TYPE	SPARES
74LS02	L40	1
74LS08	L1A	2
	L6	1
	L46	1
7414	L89	1
74LS20	L42	1
74LS20	L84	1
74LS32	L1	3
74LS32	L71	1
74123	L23	1
74123	L60	1
74LS139	L53	1
74LS139	L56	1
74LS27	L21	2
74LS27	125	1
74LS86	L26	1
74LS09	L74	4
74S74	L97	1
74LS266	L65	1

MNEMONIC CONT'D	COORD
PAØ-PA15	4F1
PAIREQ	4A7
PND	1G3
POR	4A11
PTØ-PT3	3D1
PRST	4F11
PWI	1G3
RASEL	2D11
RC	3B11
RD	3D11
RD/WR	2D11
RL	7C1
RR	3A11
RS	3A5
RST	4A11
RT	3C11
RESET	2E1
SD	3A5

MNEMONIC CONT'D	COORD
SF/SR	3D1
SGD	4B1
SG/SC	4C1
SI	4D1
SLØ-SL6	3E1
SMWR	2B11
SQ	4C1
SS	4C1
ST	3C11
TM	3B11
TR	3A5
TT	3A5

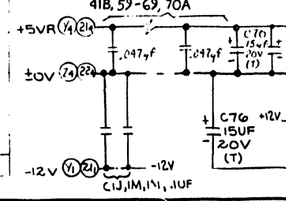
MNEMONIC CONT'D	COORD
WAIT	4G1
WR	1A10
ZRD	1A9

MNEMONIC	COORD
AA	3D11
AB	3F11
ACR	1G3
ACTIVE	3F1
BA	3A4
BB	3G11
CA	3A9
CB	3E11
CC	3E11
CD	3A5
CE	3E11
CF	3E11
CLKØ	3A5
COS	3F11
CRQ	3A6
CS	3D11
DB	3F11
DD	3F11
DIAØ	4G1
DISC	1G4
DLO	1G3
DM	3A11
DPR	3A7
ECAS	2E1
ENMI	2A11
FGD	4B1
FGRN	1C1
MA10-MA15	2G3
IC	2B1
IPL	4A8
IS	4C1
LL	4C1
LMIPE	4A5
MI	1A6
MAØ-MA9	2G11
MIC	4A6
MID	4F11
MØ-M3	1C1
MP	4A4
MPE	4A5
MPSY	4C11
MRDY	4C11
MRFSH	1A8
NB1	3A7
NB2	3A7
NB4	3A7
NB8	3A7
NS	4C1
NMI	2A8

210 = 209 + 377OR 378								
210	209	L69	L79,80	L92	L94	L95		L98
7763-A	7763	377-0393	377-0391 L	377-0371	337-0388	378-6004-R1		377-0368

DATE	BY	REVISION	NO
2-27-81	GK	ORIGINATED PER DWR #103	0
3-31-81	AR	REVISED PER ECO # 19580 APP'D: [illegible]	1/0
5-31-81	GK	REVISED PER ECO #19815 APP'D: [illegible]	2/1
5-31-81	GK	REVISED PER ECO #19815 APP'D: [illegible]	3/1
6-2-81	SDQ	REVISED PER ECO #19916 APP'D: [illegible]	4/1
6-3-81	SDQ	REVISED PER ECO #19937 APP'D: [illegible]	5/2
6-3-81	SDQ	REVISED PER ECO #19937 APP'D: [illegible]	6/2
7-9-81	XP	REVISED PER ECO # 19592 APP'D: [illegible]	7/2
7-9-81	JEP	REVISED PER ECO # 19696 APP'D: [illegible]	8/2
9-4-81	DWR	REVISED PER ECO # 20034 & 20237 APP'D: [illegible]	9/3
9-4-81	DWR	REVISED PER ECO#20387 APP'D: [illegible]	10/4
9-4-81	DWR	REVISED PER ECO#20398 APP'D: [illegible]	11/4
11-24-81	VH	REVISED PER ECO 19845, 20093 APP'D: [illegible]	12/4
2-3-82	PGD	REVISED PER ECO #21828 APP'D: [illegible]	13/4
3-30-82	D.S.	REVISED PER ECO #22221 APP'D: [illegible]	14/4
6-10-82	PGD	REVISED PER ECO # 23396 APP'D: [illegible]	15/5
7-11-83	#3	REVISED PER ECO's 21706, 21707, 21631, 21816, 21748 APP'D: [illegible]	16/5

C1A-C1H,4-14,C9A,16-35, 35A,37-56,39A,39B,40A,41A, 41B,59-69,70A



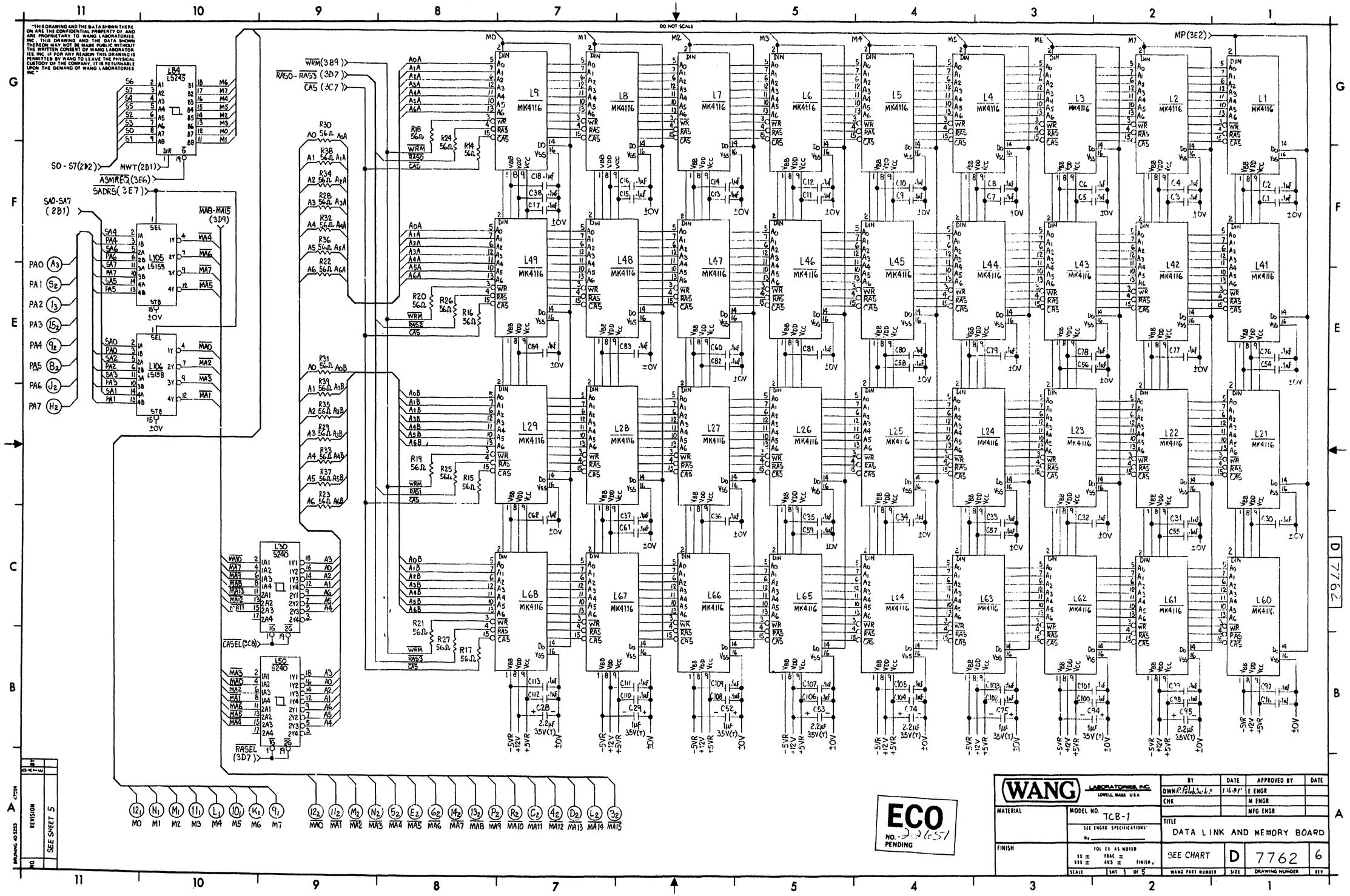
NOLE LEGEND & TOLERANCES			
NOLE DIA		TOLERANCE	
0135	135	± .003	003
128	256	± .004	004
251	500	± .005	005
SYM	DESCRIPTION		QTY
A			

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.			
MATERIAL	MODEL NO	TCB-1	
	SEE ENGRG SPECIFICATIONS No.		
FINISH	TOL ER AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH		
SCALE	SHT 6 OF 6		
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	7763	

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	2/27/81	E ENGR	[illegible]
CHK	[illegible]	[illegible]	M ENGR	
			MFG ENGR	

TITLE: CPU MOTHERBOARD

7763



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DO NOT SCALE
MP(3E2)
WRM(3B9)
RAS0-RAS3 (3D7)
CAS (3C7)
SO-S7(2D2)
MWT(2D1)
ASMREQ(3E6)
SADRS(3E7)
SA0-SA7 (2B1)
MA8-MA15 (3D9)
CASEL(3C8)
RASEL (3D7)
L84 LS245
L105 LS158
L106 LS158
L30 S240
L50 S240
L9 MK4116
L8 MK4116
L7 MK4116
L6 MK4116
L5 MK4116
L4 MK4116
L3 MK4116
L2 MK4116
L1 MK4116
L49 MK4116
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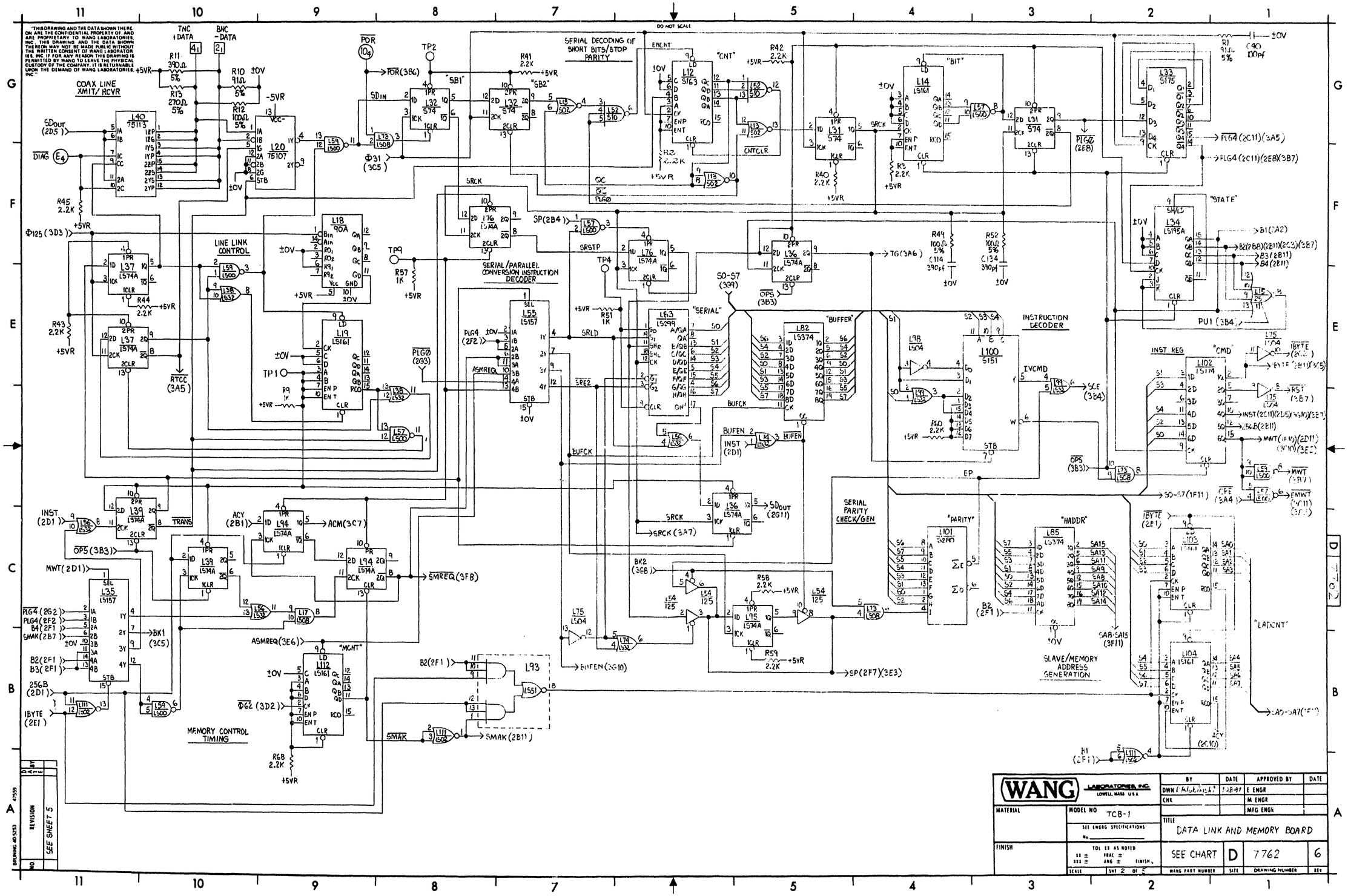
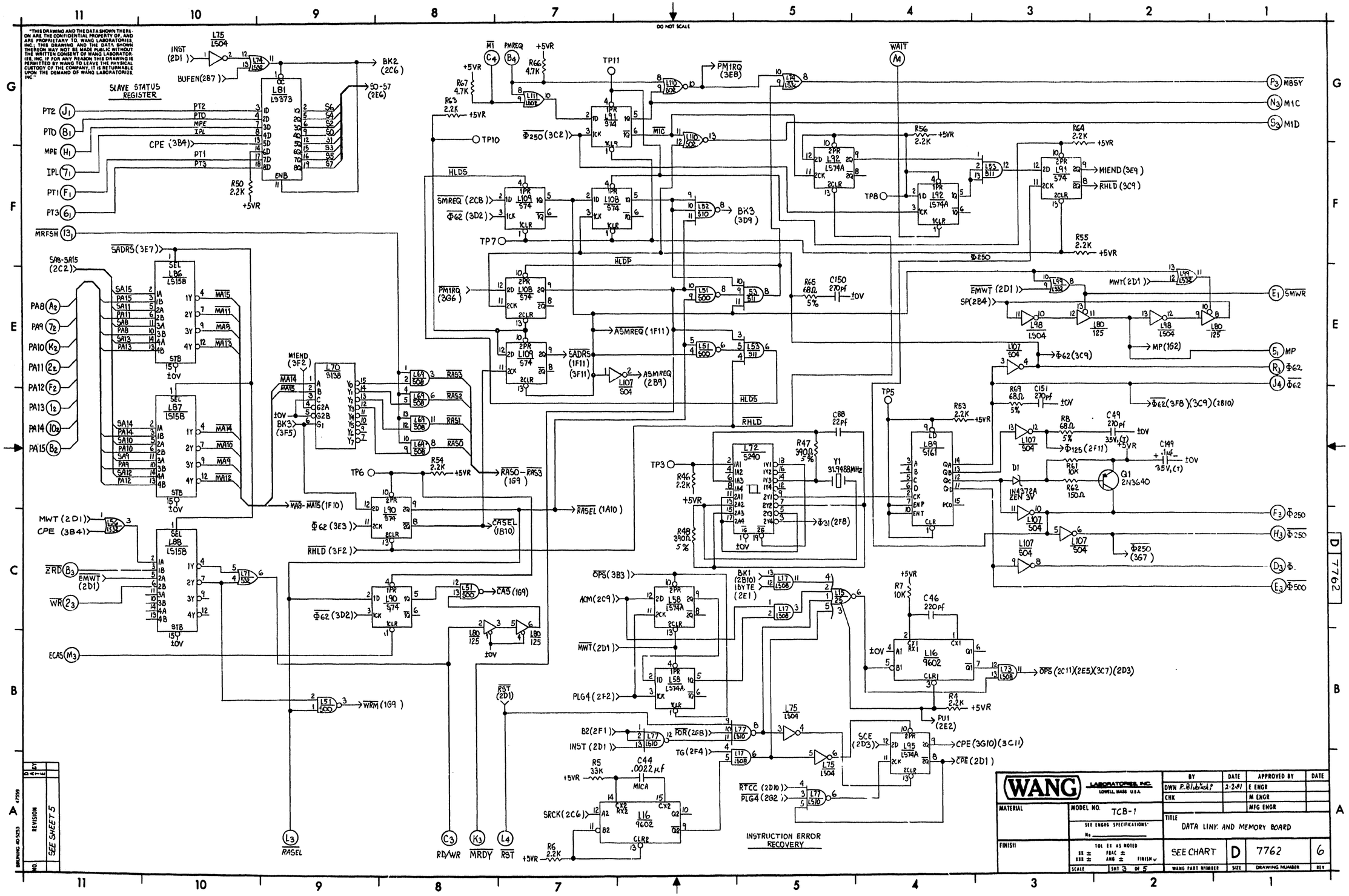
L63 MK4116
L62 MK4116
L61 MK4116
L60 MK4116
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
M0 M1 M2 M3 M4 M5 M6 M7
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13 MA14 MA15
ECO
NO. 2-2651
PENDING
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MATERIAL
MODEL NO. TCB-1
SEE ENGRG SPECIFICATIONS
FINISH
TOL EX AS NOTED
SCALE
SHT 1 OF 5
BY
DATE
APPROVED BY
DATE
DWN R. Polub
1-16-81
E ENGR
CHK
M ENGR
MFG ENGR
TITLE
DATA LINK AND MEMORY BOARD
SEE CHART
D
7762
6
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
REVISION
SEE SHEET 5
BRUNING 40-5253



WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN	7-28-81	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO TCB-1			MFG ENGR	
	SEE ENGRG SPECIFICATIONS No.	TITLE DATA LINK AND MEMORY BOARD			
FINISH	TOL EX AS NOTED XX ± FRAC ± XXX ± ANG ± FINISH	SEE CHART	D	7762	6
	SCALE SHT 2 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

NO	REVISION	DATE	BY
	SEE SHEET 5		

BRUNING 40-5253 47559



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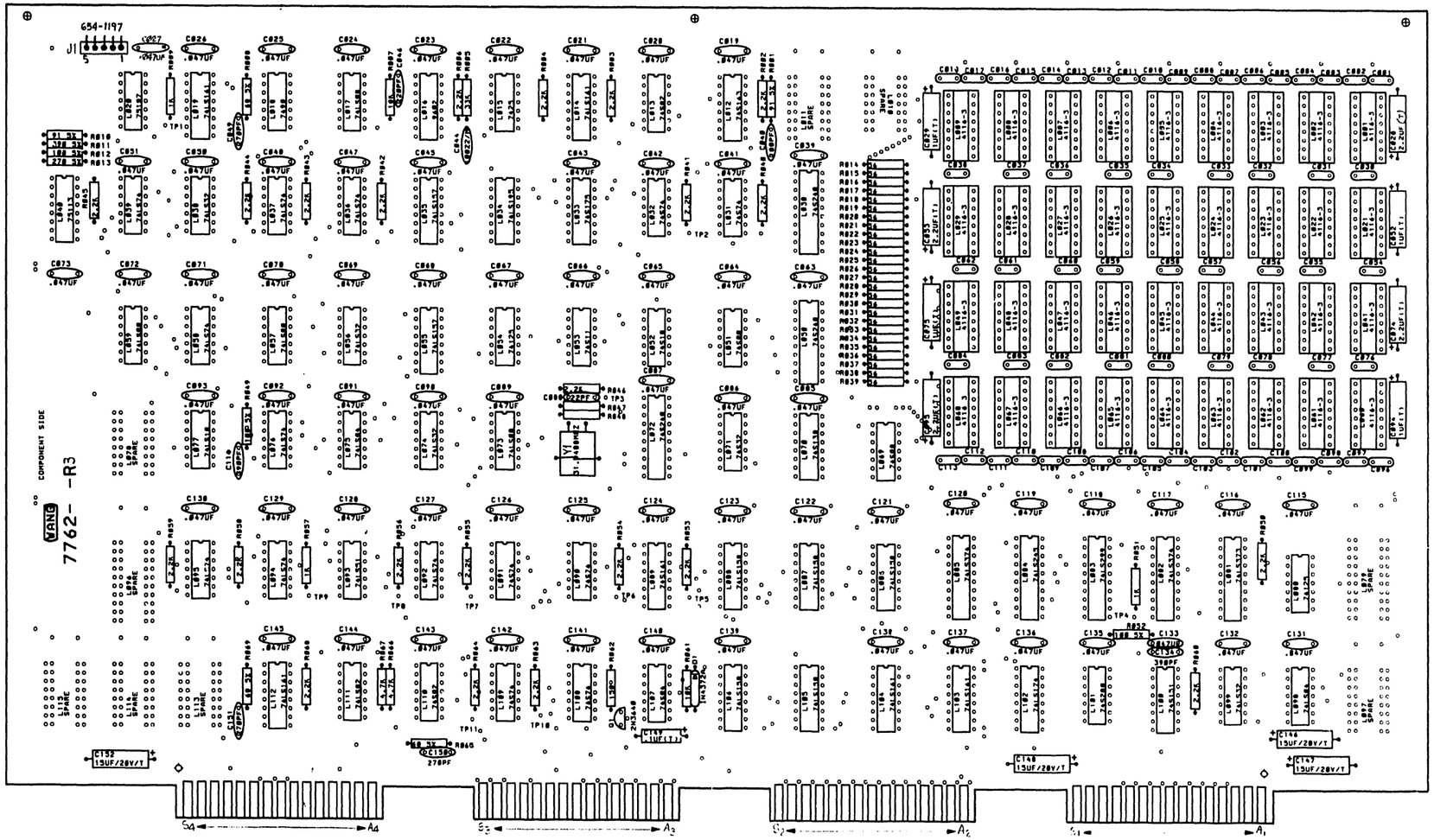
DO NOT SCALE
SLAVE STATUS REGISTER
INSTRUCTION ERROR RECOVERY
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO. TCB-1
TITLE DATA LINK AND MEMORY BOARD
SEE CHART
D
7762
6
SHT 3 OF 5
SEE SHEET 5

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES INC.



WANG LABORATORIES, INC. LOWELL MASS. U.S.A.	BY	DATE	APPROVED BY	DATE	
	DWN R. Blubinski	2-6-81	E ENGR		
	CHK		M ENGR		
MATERIAL	MODEL NO TCB-1		MFG ENGR		
	SEE ENGRG SPECIFICATIONS No.	TITLE DATA LINK AND MEMORY BOARD			
FINISH	TOL EX AS NOTED XX ± XXX ± FRAC ± ANG ± FINISH	SEE CHART	D	7762	6
	SCALE SHT 4 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

NO.	REVISION	DATE	BY
	SEE SHEET 5		

D 7762

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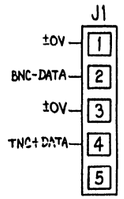
DO NOT SCALE

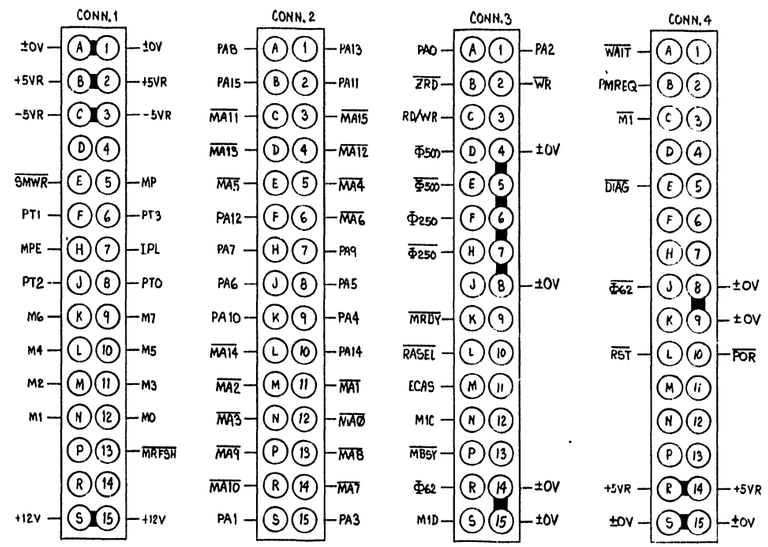
I.C. LOCATION	TYPE	W.L. PART NO.
L1-9,21-29,41-49,60-68	MK4116-N3	SEE CHART
L10,11,78,79,96,97,113-115	SPARES	
L12	74S163	376-0235
L13,110	74S02	376-0199
L14,19,103,104,112	74LS161	376-0233
L15	7425	376-0092
L16	9602	376-0104
L17,73	74LS08	376-0153
L18	7490A	376-0073
L20	75107	376-0146
L30,50,72	74S240	376-0334
L31,32,90,91,108,109	74S74	376-0202
L33	74S175	376-0270
L34	74LS195A	376-0248
L35,55	74LS157	376-0216
L36,37,39,58,76,92,94,95	74LS74A	376-0155
L38,56,74,99	74L532	376-0211
L40	75113	376-0256
L51	74S00	376-0228
L57,59	74LS00	376-0207
L52	74S10	376-0238
L53	74S11	376-0237
L54,80	74125	376-0324
L69	74S08	376-0200
L70	74S138	376-0298
L71	74S32	376-0205
L75,98	74LS04	376-0180
L77	74LS10	376-0209
L81	74LS373	376-0310
L82,85	74LS374	376-0286
L83	74LS299	376-0303
L84	74LS245	376-0285
L86-88,105,106	74LS158	376-0293
L89	74S161	376-0278
L93	74LS51	376-0213
L100	74S151	376-0336
L101	74S280	376-0246
L102	74LS174	376-0159
L107	74S04	376-0197
L111	74LS02	376-0208
L1-9,21-29,41-49,60-68	SKT, 16 PIN	376-9002

TYPE	I.C. LOCATION	SPARES
74S02	L13	1
	L110	2
74LS04	L98	3
74S32	L71	3
74L532	L38	2
74LS51	L93	1
74125	L54	1

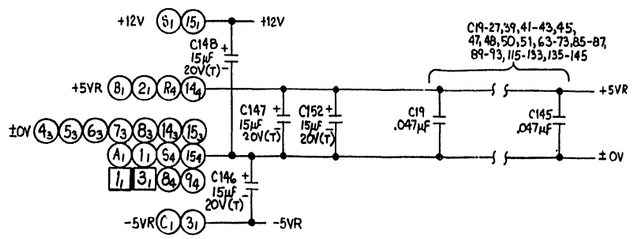
COMPONENT	TYPE	W.L.PART NO
J1	CONN, 5 PIN	654-1197
D1	IN4372A, 3V	380-2129
R1,10	91Ω, ¼W, 5%	330-1092
R2-4,6,40-46,50,53-56,58-60,63,64,68	2.2K, ¼W, 10%	330-3022
R5	33K, ¼W, 10%	330-4033
R7,61	10K, ¼W, 10%	330-4010
R8,65,69	68Ω, ¼W, 5%	330-1069
R9,51,57	1K, ¼W, 10%	330-3010
R11,47,48	390Ω, ¼W, 5%	330-2040
R62	150Ω, ¼W, 10%	330-2015
R12,49,52	100Ω, 1W, 5%	332-2011
R13	270Ω, ¼W, 5%	330-2028
R14-39	56Ω, ¼W, 10%	330-1056
R66,67	4.7K, ¼W, 10%	330-3047
C1-18,30-38,54-62,76-84,96-113	.1μF, 50V	300-1930
C19-27,39,41-43,45,47,48,50,51,63-73,85-87,89-93,115-133,135-145	.047μF, 50V	300-1966
C29,52,75,94	1μF, 35V, (T)	300-4000
C40	100pf, 100V	300-1944
C44	.0022μF, 500V, MICA	300-5012
C46	220pf, 500V	300-1220
C49,150,151	270pf, 500V	300-1270
C88	22pf	300-1022
C28,53,74,95	2.2μF 35V, (T)	300-4027
C114,134	390pf, 500V	300-1390
C146-148,152	15μF, 20V, (T)	300-4022
C149	.1μF 35V, (T)	300-4002
Q1	2N3640	375-1003
Y1	31.9488MHz	321-0044

MNEMONICS	COORD
BNC-DATA	2G9
$\overline{DIAG}$	2F11
ECAS	3B11
$\overline{IPL}$	3F11
$\overline{MA0}$-$\overline{MA15}$	1A9
$\overline{MBSY}$	3G1
M0-M7	1A10
MP	3E1
MPE	3F11
$\overline{M1}$	3G8
$\overline{MRDY}$	3A8
$\overline{MRFSH}$	3F11
M1C	3G1
M1D	3G1
PA0-PA7	1E11
PA8-PA15	3E11
PMREQ	3G7
$\overline{POR}$	2G9
PT0	3G11
PT1	3F11
PT2	3G11
PT3	3F11
$\overline{RASEL}$	3A9
RD/WR	3A8
$\overline{RST}$	3A7
$\overline{SMWR}$	3E1
TNC+DATA	2G9
$\overline{WAIT}$	3G4
$\overline{WR}$	3C11
$\overline{ZRD}$	3C11
$\overline{\Phi62}$	3E1
$\Phi62$	3E1
$\Phi250$	3C1
$\overline{\Phi250}$	3C1
$\Phi500$	3C1
$\overline{\Phi500}$	3C1





210=209+377 OR 378		
210	209	L1-9,21-29,41-49,60-68
7762-A	7762	377-0345-M



E-REV 3

DWN	R.A.P. 2-6-81	LL 5-16-81	SOB 6-3-81	SOP 6-3-81	R.B.P. 7-28-81	D.S. 10-1-81	D.S. 4-5-82
REVISION	ORIG PER DWG #E1025 APP'D: RAP 2/6/81	REVISED PER ECO #1553 APP'D: LL 5/16/81	REVISED PER ECO #1907 APP'D: SOB 6/3/81	REVISED PER ECO #19437 APP'D: SOP 6/3/81	REVISED PER ECO #1959 APP'D: RBP 7-28-81	REVISED PER ECO #2007 APP'D: DS 10/1/81	REVISED PER ECO # 22104 APP'D: DS 4/5/82
NO	0/0	1/0	2/1	3/1	4/2	5/2	6/3

BY	DATE	APPROVED BY	DATE
DWN R.P. Weisbrich Jr	2-6-81	E ENGR	4/3/81
CHK LH Kozol	3-6-81	M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. TCB-1
SEE ENGRG SPECIFICATIONS
No.

FINISH

TOL ES AS NOTED
.XX ± FRAC ±
.XXX ± ANG ± FINISH √

TITLE
DATA LINK AND MEMORY BOARD

SCALE	SHT 5 OF 5	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
		SEE CHART	D	7762	6

D 7762

BRUNING 40-3253 A-7959

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DO NOT SCALE

HOLE LEGEND & TOLERANCES

HOLE DIA	TOLERANCE
.031 .125	± .003 .003
.126 .250	± .004 .004
.251 .500	± .005 .005

011

INT (2D1)

RESET (4B6)

WAIT (4F5)

Φ250 (4B10)

BUSRQ (4B9)

+5VR

GND

L98 Z80A-CPU

R72A 4.7K

NMI (2A10)

HALT

BUSAK

RD

MI

MREQ

IORQ

RFSH

WR

BUSAK (1F7)

L87 LS04

MI (4F7)(1F4)

DDMA (4F3)

L100 LS367

RFSH (2E1)

R68 330R

R66 330R

R63 10K

R65 10K

READY (4C9)

Φ500 (4C10)

PA4 (4D3)

RESET (4B6)

DREQØ (2G2)

DREQ1 (2G4)

DREQ2 (2G2)

DREQ3 (2G4)

L94 95117A

ADSTB

HREQ

HREQ (4B10)

MEMW

MEMW (2C7)

R40 10K

ALT Vcc

R58 2.2K

AEN

AENR

WHICK

DIVØ

DACKØ (2E4)

DACK1 (2E5)

DACK2 (2E4)

DACK3 (2E5)

EOP

R57 4.7K

R69 10K

ICR

IOW

READY (4C9)

R42 10K

R43 10K

R64 10K

L69 LS08

L68 LS373

BUSAK (1D10)

L88 LS74

L103 125

WR (2D5) (4E8)

R44 2.2K

TP9 BK2 (4B9)

AEN

MREQ (4C6)

L84 LS08

L86 LS08

DACKR (2E3)

DACKT (2E5)

DI/OW

I/OR

IORQ

DSIØ (4G3)

IORQ (4E5) (1F4)

L102 LS32

ZRD (4F8)

L62 LS32

EOPR (2G3)

EOPT (2G6)

L95 2732

DFØ (4D3)

R41 68Ω

C57 270pf

L51 LS280

C/G (4D5)

EVEN Σ (4C6)

ODD Σ (4D6)

RD (4E6)

TPB

R50 2.2K

L52 LS157

L53 LS74

L54 LS08

L55 LS32

L56 LS08

L57 LS32

L58 LS08

L59 LS32

L60 LS08

L61 LS08

L62 LS32

L63 LS08

L64 LS08

L65 LS08

L66 LS08

L67 LS08

L68 LS08

L69 Z80A SIO-2

L71 LS32

L72 LS08

L73 LS32

L74 LS74

L75 LS08

L76 LS08

L77 LS08

L78 LS08

L79 LS08

L80 LS08

L81 LS08

L82 LS08

L83 LS08

L84 LS08

L85 LS08

L86 LS08

L87 LS04

L88 LS74

L89 14

L90 LS08

L91 LS08

L92 Z80A-CTC

L94 95117A

L95 2732

L96 LS08

L97 LS08

L98 Z80A-CPU

L99 LS245

L100 LS367

L101 LS08

L102 LS32

L103 125

L104 LS08

L105 LS08

L106 LS08

L107 LS08

L108 LS08

L109 LS08

L110 LS08

L111 LS08

L112 LS08

L113 LS08

L114 LS08

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L116 LS08

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L118 LS08

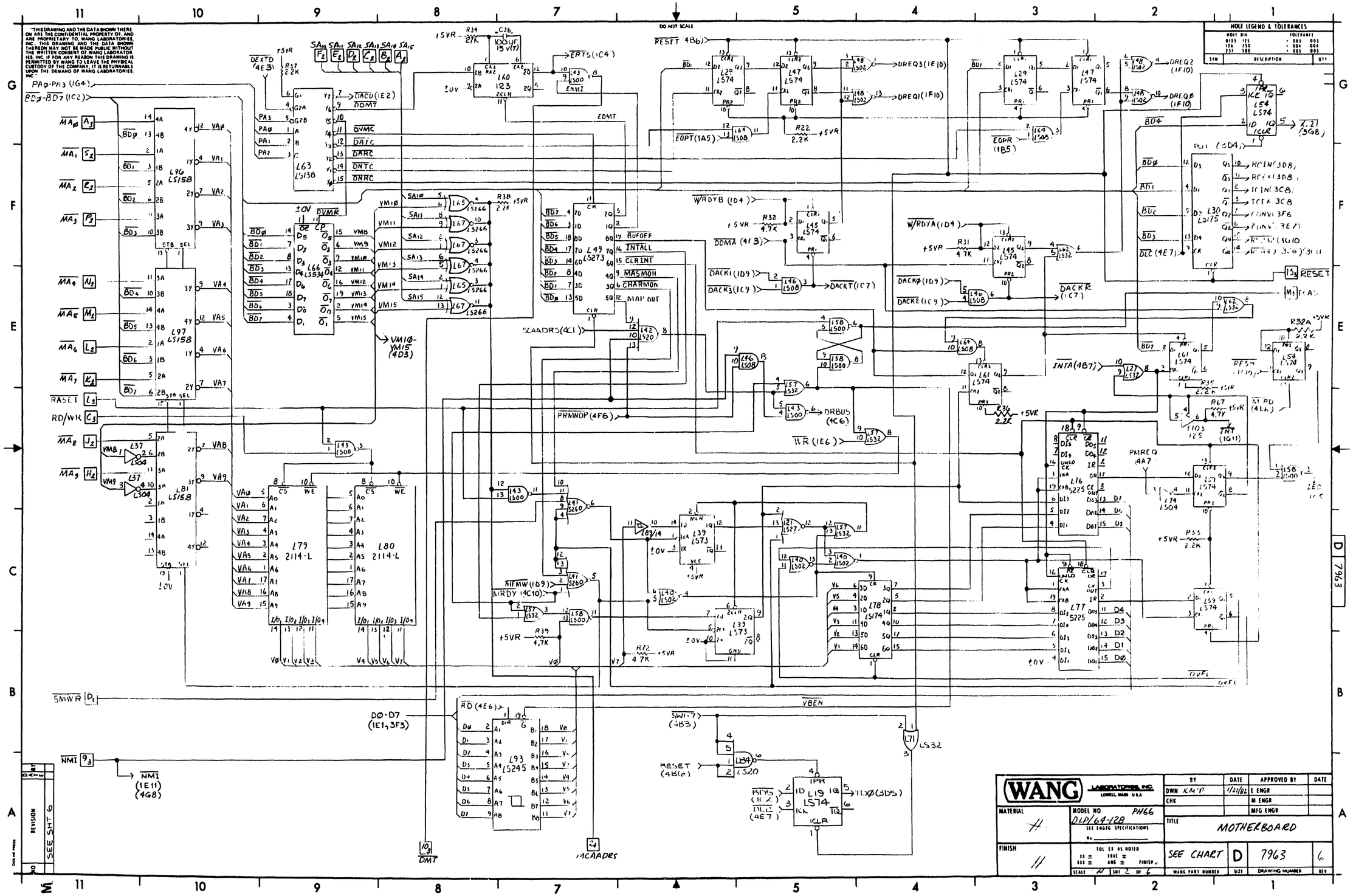
L119 LS08

L120 LS08

L121 LS08

L122 LS08

L123 LS08



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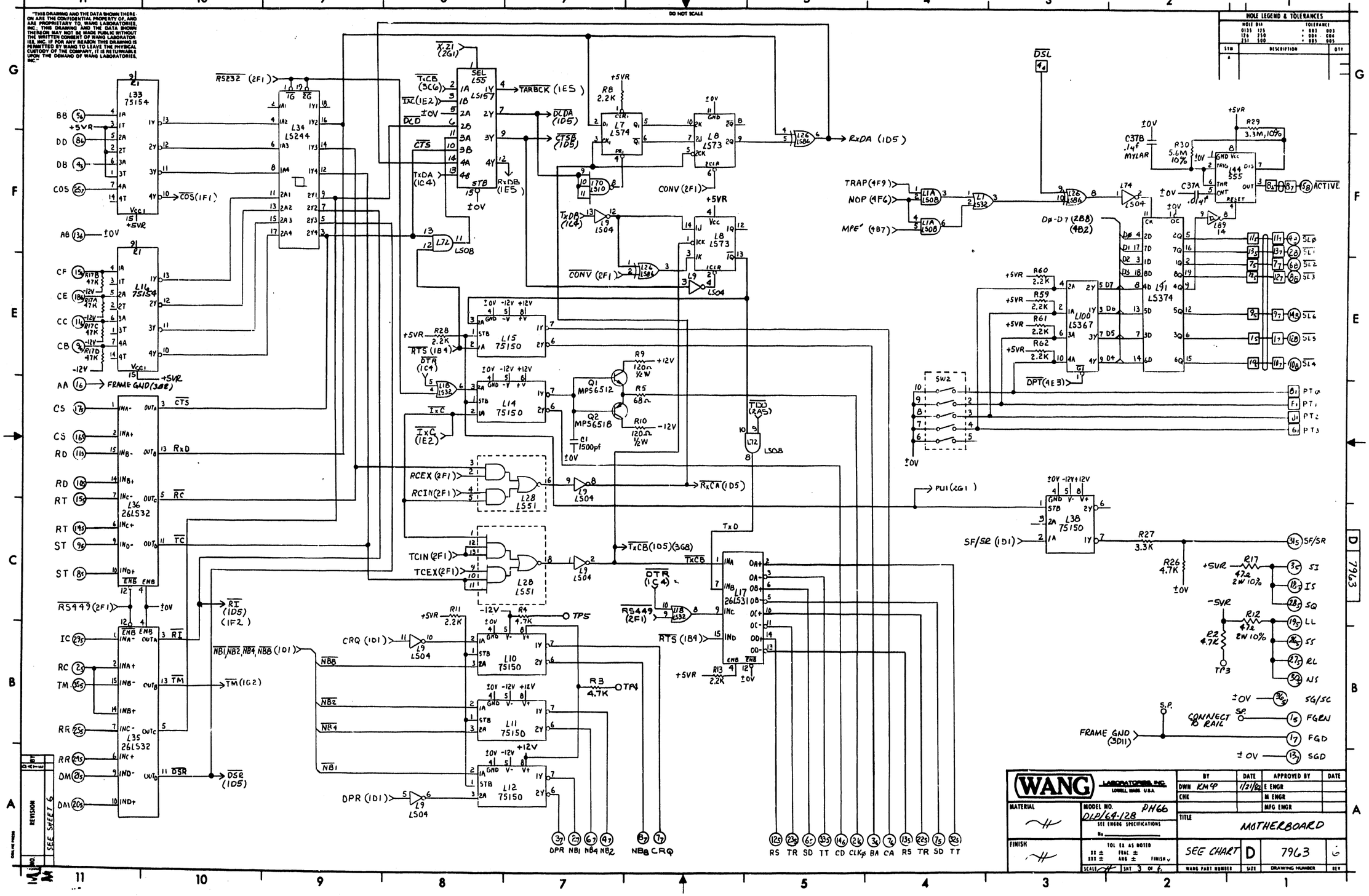
DO NOT SCALE
HOLE LEGEND & TOLERANCES
WANG LABORATORIES, INC.
LOWELL, MASS. U.S.A.
MODEL NO. PH66
DLP/64-128
SEE ENGRG SPECIFICATIONS
MATERIAL
FINISH
TOL EX AS NOTED
SCALE
SHT 2 OF 6
DWN KMP
1/21/82
E ENGR
M ENGR
MFG ENGR
TITLE
MOTHERBOARD
SEE CHART
D
7963
6
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
REVISION
SEE SHT 6



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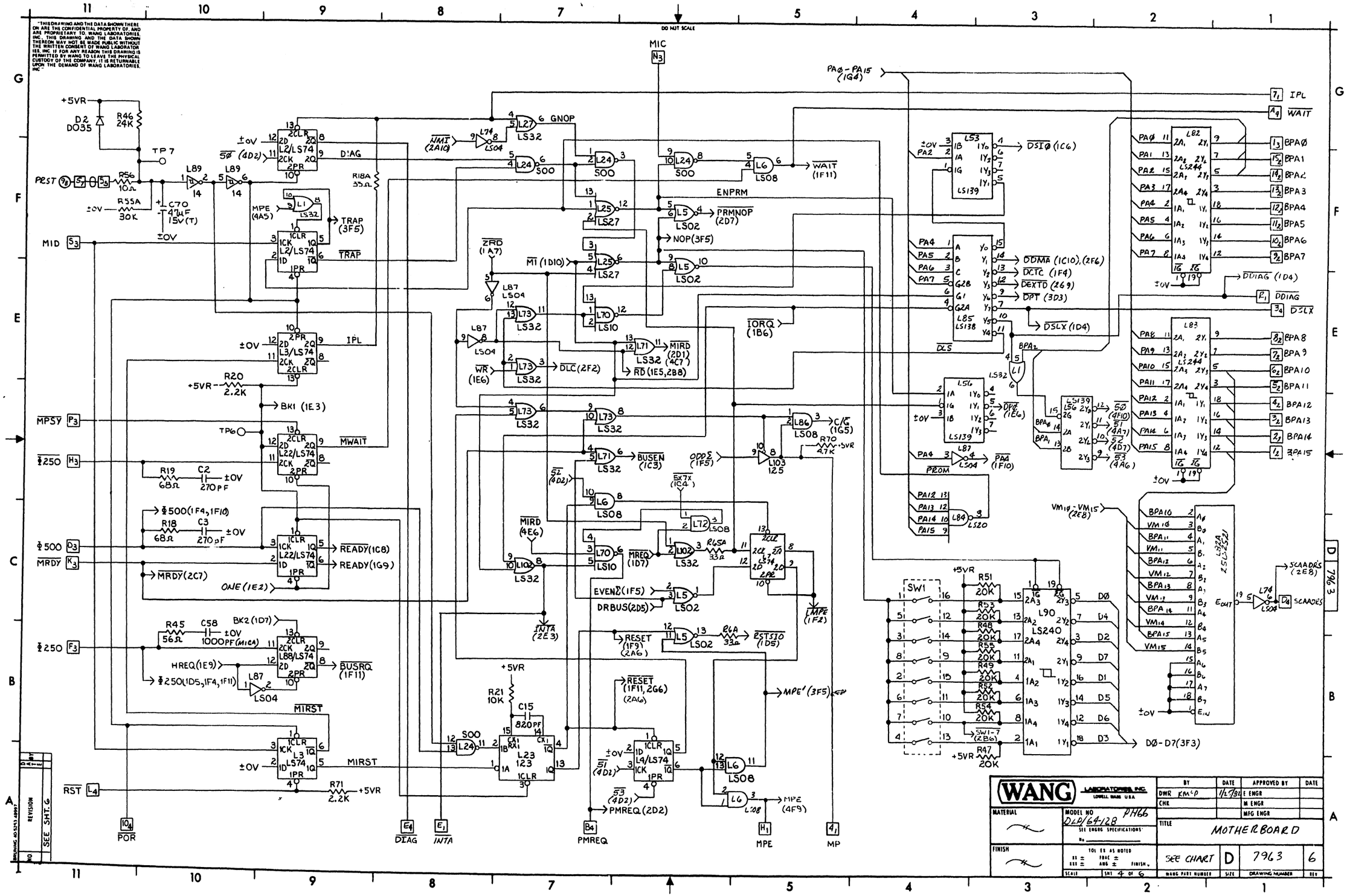
DO NOT SCALE
HOLE LEGEND & TOLERANCES
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
MODEL NO. DLP/64-128 PH66
SEE ENGRG SPECIFICATIONS
TITLE MOTHERBOARD
SEE CHART D 7963 6
WANG PART NUMBER SIZE DRAWING NUMBER REV
SHT 3 OF 6
DWN KMP 1/21/82
E ENGR
M ENGR
MFG ENGR
MATERIAL
FINISH
SCALE
REVISION
SEE SHEET 6



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DO NOT SCALE
MIC
PA0-PA15 (1G4)
IPL
WAIT
BPA0
BPA1
BPA2
BPA3
BPA4
BPA5
BPA6
BPA7
DDIAG (1D4)
DDIAG
DSLX
BPA8
BPA9
BPA10
BPA11
BPA12
BPA13
BPA14
BPA15
VM10-VM15 (2E8)
SCAADRS (2E8)
SCAADRS
DSIO (1C6)
WAIT (1F11)
ENPRM
PRMNOP (2D7)
NOP(3F5)
DDMA (1C10),(2F6)
DCTC (1F4)
DEXTD (2G9)
DPT (3D3)
DSLX (1D4)
DLS
IORQ (1B6)
MIRD (2D1) (4C7)
RD (1E5,2B8)
DLC (2F2)
C/G (1G5)
BUSEN (1C3)
ODD Σ (1F5)
EX7X (1C4)
MIRD (4E6)
MREQ (1D7)
EVEN Σ (1F5)
DRBUS (2D5)
LMPE (1F2)
RESET (1F9) (2A6)
RSTSIO (1D5)
RESET (1F11,2G6) (2A6)
MPE' (3F5)
PMREQ (2D2)
MPE (4F9)
MPE
MP
PMREQ
INTA (2E3)
INTA
DIAG
POR
RST
MIRST
MWAIT
MPSY
Φ250
Φ500
MRDY
READY (1C8)
READY (1G9)
MRDY (2C7)
ONE (1E2)
BK1 (1E3)
BK2 (1D7)
HREQ (1E9)
Φ250 (1D5,1F4,1F11)
BUSRQ (1F11)
MID
PREST
TRAP
MPE (4A5)
DIAG
GNOP
SOO
NMI (2A10)
ZRD (1A7)
MI (1D10)
WR (1E6)
DO-D7(3F3)
SW1
SW1-7 (2B6)
+5VR
+5V
±0V
TP7
TP6
D2 DO35
R46 24K
R56 10Ω
R55A 30K
C70 47μF 15V(T)
R18A 33Ω
R20 2.2K
R19 68Ω
C2 270PF
R18 68Ω
C3 270PF
R45 56Ω
C58 1000PF(MIC4)
R71 2.2K
R21 10K
C15 820PF
R51 20K
R53 20K
R48 20K
R55 20K
R49 20K
R52 20K
R54 20K
R47 20K
R65A 33Ω
R64 33Ω
R70 4.7K
L89
L74 LS04
L27 LS32
L24
L25 LS27
L1 LS32
L2/LS74
L3/LS74
L22/LS74
L88/LS74
L87 LS04
L73 LS32
L70 LS10
L71 LS32
L6 LS08
L5 LS02
L102 LS32
L86 LS08
L103 125
L72 LS08
L23 123
L4/LS74
L53 LS139
L85 LS138
L56 LS139
L87 LS04
L84 LS20
L82 LS244
L83 LS244
LS139
L90 LS240
L82A 25LS2521
L74 LS04
WANG LABORATORIES, INC. LOWELL MASS U.S.A.
MATERIAL
FINISH
MODEL NO DLP/64-128 PH66
SEE ENGRG SPECIFICATIONS
TOL EX AS NOTED
SCALE
SHT 4 OF 6
BY
DATE
APPROVED BY
DATE
DWR KMCD 1/25/82
CHK
E ENGR
M ENGR
MFG ENGR
TITLE MOTHERBOARD
SEE CHART
D
7963
6
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
SEE SHT. 6
REVISION
NO
DATE
BY

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DO NOT SCALE

CABLE ASSY

P5 P6 P7 P8

P4 P3 P2 P1

7963- -R3

REVISION	BY	DATE
SEE SHT. 6		

WANG LABORATORIES, INC. LOWELL MASS U.S.A.

	BY	DATE	APPROVED BY	DATE
	DWN KM'D.	1/21/82	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO PH66 DLP/64-128 (SEE ENGRG SPECIFICATIONS) No ____

FINISH

TOL EX AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH.

TITLE MOTHERBOARD

SCALE SHT 5 OF 6 | SEE CHART | D | 7963 | 6

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

D 7963

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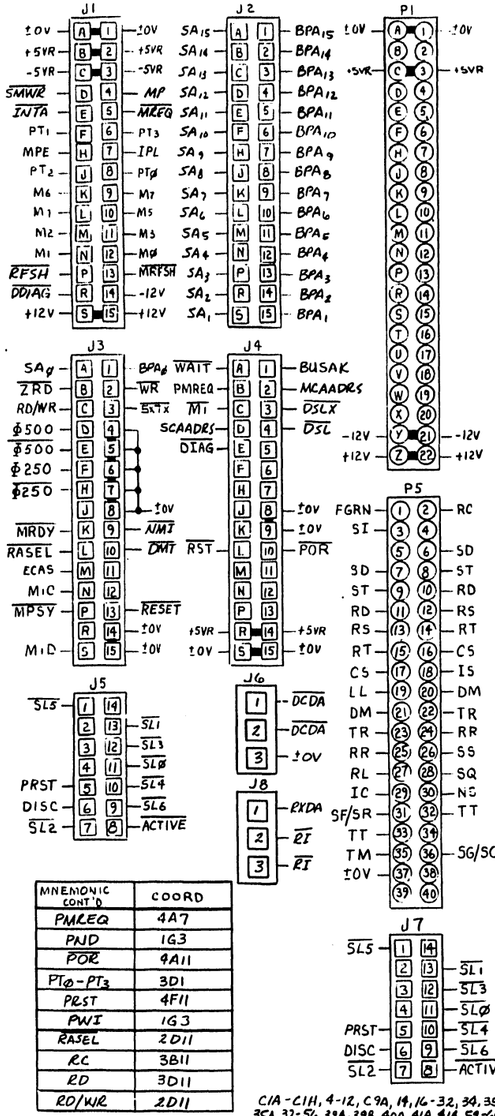
IC LOCATION	TYPE	W L PART NO
L1,18,27,57,62,71,73,102	74LS32	376-0211
L1A,6,46,64,72,86	74LS08	376-0153
L2,3,4,7,22,29,45,47,54, 59,61,88,19	74LS74A	376-0155
L5,40,48	74LS02	376-0208
L8,39	74LS73	376-0304
L9,37,74,87	74LS04	376-0180
L10,11,12,14,15,38	75150	376-0076
L13,16,33	75154	376-0077
L17	26LS31	376-0470
L21,25	74LS27	376-0245
L23,60	74123	376-0080
L24	74S00	376-0228
L26	74LS86	376-0231
L28	74LS51	376-0213
L30	74LS175	376-0160
L31,49	74LS273	376-0302
L32,50,90	74LS240	376-0297
L34,82,83	74LS244	376-0288
L35,36	26LS32	376-0471
L41	74S260	376-0206
L42,84	74LS20	376-0210
L43,58	74LS00	376-0207
L44	NE555	376-0126
L51	74LS280	376-0242
L52,55	74LS157	376-0216
L53,56	74LS139	376-0226
L63,85	74LS138	376-0294
L65,67	74LS266	376-0148
L66	74LS534	376-0544
L68	74LS373	376-0310
L69	Z80A-SIO/2	SEE CHART
L70	74LS10	376-0209
L76,77	74S225	376-0323
L78	74LS174	376-0159
L79,80	2114L	SEE CHART
L81,96,97	74LS158	376-0293
L89	7414	376-0139
L91	74LS374	376-0286
L92	Z80A/CTC	SEE CHART
L93,99	74LS245	376-0285
L94	AM9517A	SEE CHART
L95	2732	SEE CHART
L98	Z80A/CPU	SEE CHART
L100	74LS367	376-0192
L103	74125	376-0324
L82A	25LS2521	376-0317
L69,94,98	40 PIN SOCKET	376-9011
L77,80	18 PIN SOCKET	376-9014
L92	28 PIN SOCKET	376-9015
L95	24 PIN SOCKET	376-9003

210 = 209 + 377 OR 378							
210	209	L69	L79,80	L92	L94	L95	L98
7963-A	7963	377-0393	377-0341-L	377-0371	377-0388	378-9038	377-0368

COMPONENT	TYPE	W.L. PART NO.
R1-4,26,31,32,39, 57,67,70,72,72A,	4.7K ¼W 5%	330-3048
R5,18,19,41	68Ω ¼W 5%	330-1069
R6,8,11,13,20,22,28, 33,35-38,44,50,52-62, 32A,71	2.2K ¼W 5%	330-3023
R6A,18A,65A	33Ω ¼W 5%	330-1034
R9,10	120Ω ½W 5%	331-2013
R12,17	47Ω 2W 10%	337-1047
R17A,17B,17C,17D	47K ¼W 5%	330-4048
R55A	30K ¼W 5%	330-4031
R21,40,42,43,63-66, 68,69	10K ¼W 5%	330-4011
R27	3.3K ¼W 5%	331-3034
R29	3.3M ¼W 10%	330-6033
R30	5.6M ¼W 10%	330-6056
R34	27K ¼W 5%	330-4028
R45	56Ω ¼W 5%	330-1057
R46	24K ¼W 5%	330-4025
R47-49,51-55	20K ¼W 5%	330-4021
R56	10Ω ¼W 5%	330-1011
C70	470F 15V (T)	300-4020
C1	1500pf 200V	300-1964
C1A-C1H,4-12,12A, 9A,14,32A 16-32,34,35,35A,39A, 37-56,39B,40A,41A,41B 59-64,66-69,47A,70A	.047μf 50V	300-1966
C1J,1K,1L,1M,1N,1P	.1μf, 50V	300-1930
C2,3,57	270pf 500V	300-1270
C15	820pf 500V	300-1820
C36	100UF 15V (T)	300-4021
C37A	.01μf 25V	300-1903
C37B	.1μf 100V (M)	300-2210
C58	1000pf 100V(MKM)	300-5006
C71-73,76,77	15μf 20V (T)	300-4022
D2	SIL DO35	380-1001
Q1	MPS6512	375-1012
Q2	MPS6518	375-1014
CABLE ASSY	14 COND. FLAT	220-3170
SW1	SPST, 8POS.	325-1503
SW2	SPST, 5POS.	325-1501
J1,2,3,4	30PIN CONN	350-0009
J5,7	14PIN SOCKET	376-9012

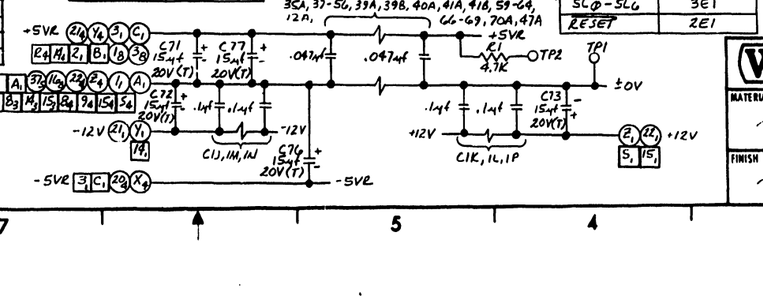
IC LOCATION	TYPE	SPARES
74LS02	L40	1
74LS32	L102	1
74LS04	L37	4
	L74	2
74LS08	L1A	2
7414	L89	1
74LS20	L42	1
74LS27	L21	2
	L25	1
74LS32	L1	1
74LS86	L26	1
74123	L23	1
	L60	1
74LS139	L53	1
74LS74	L19	1
74LS266	L65	2

MNEMONIC CONT'D	COORD
PMREQ	4A7
PND	1G3
POR	4A11
PTØ-PT3	3D1
PRST	4F11
PWI	1G3
RASEL	2D11
RC	3B11
RD	3D11
RD/WR	2D11



MNEMONIC	COORD
RFSH	1A10
RL	3B1
RR	3A11
RS	3A5,3A4
RST	4A11
RT	3C11
SA10-SA15	2G9
SCAADRS	4C1
SD	3A5,3A4
SF/SR	3C1
SGD	3A1
SG/SC	3B1
SI	3C1
SLØ-SL6	3E1
RESET	2E1

MNEMONIC	COORD
SMWR	2B11
SQ	3C1
SS	3B1
ST	3C11
TM	3B11
TR	3A5,3A4
TT	3A5,3A4
WAIT	4G1
WR	1A10
ZRD	1A9
5X7X	1C1
Ø250	4B11
Ø250	4D11
Ø500	4C11
Ø500	1G8



NOTE:
1. ALL RES. ARE ¼W 5% UNLESS OTHERWISE SPECIFIED.

HOLE LEGEND & TOLERANCES			
HOLE DIA		TOLERANCE	
0133	173	.003	.003
174	350	.004	.004
351	500	.005	.005

SYM	DESCRIPTION	DTE
A		

MNEMONIC	COORD
AA	3D11
AB	3F11
ACR	1G3
ACTIVE	3F1
BA	3A4
BB	3G11
BPA6-BPA15	4G1
BUSAK	1A11
CA	3A9
CB	3E11
CC	3E11
CD	3A5
CE	3E11
CF	3E11
CLKØ	3A5
COS	3F11
CRQ	3A6
CS	3D11
DB	3F11
DD	3F11
DDIAG	4E1
DIAG	4A8
DISC	1G4
DLO	1G3
DM	3A11
DMT	2A8
DPR	3A7
DSL	3G3
DSLX	4E1
ECAS	2E1
FGD	3B1
FGRN	3B1
IC	3B11
INTA	4A8
IPL	4G1
IS	3C1
LL	3C1
MA6-MA9	2G11
MI	1A6
MIC	4G6
MID	4F11
M6-M7	1C1
MP	4A5
MPE	4A5
MPSY	4D11
MRDY	4C11
MREQ	1A10
MRFSH	1A8
NB1	3A7
NB2	3A7
NB4	3A7
NB8	3A6
NS	3B1
NMI	2A11
MCAADRS	2A7

E-REV 3

NO	REVISION	BY	DATE
0	ORIGINATED PER DWR E486 APP'D: [illegible]		11/24/82
1	REVISED PER ECO# 23229 APP'D: [illegible]		6/23/83
2	REVISED PER ECO# 24930 APP'D: [illegible]		9/23/83
3	REVISED PER ECO# 25625 APP'D: [illegible]		11/28/83
4	REVISED PER ECO# 26354 APP'D: [illegible]		6/29/83
5	REVISED PER ECO# 28215 APP'D: [illegible]		11/7/83
6	REVISED PER ECO# 29690 APP'D: SJC		12/1/83

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

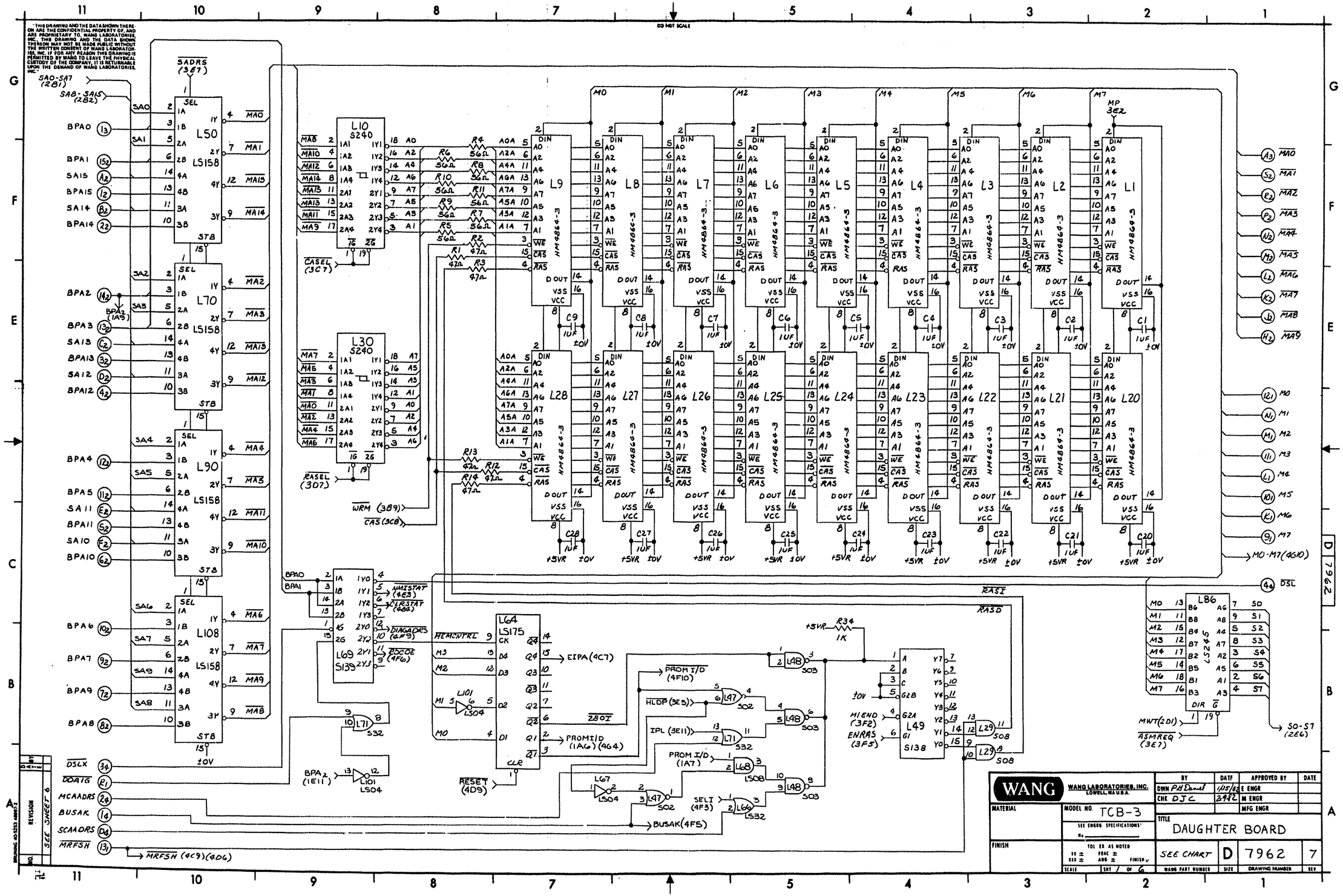
BY	DATE	APPROVED BY	DATE
DWN KNG	11/24/82	E ENGR	
CHK [illegible]	[illegible]	M ENGR	
		MFG ENGR	

MATERIAL: H
MODEL NO: DLP/64-128 DH66
SEE ENGRG SPECIFICATIONS
No.
FINISH: H
TOL EX AS NOTED
XX ± FRAC ± XXX ± ANG ± FINISH √
SCALE H SHT 6 OF 6

TITLE: MOTHERBOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	7963	6

D-7963



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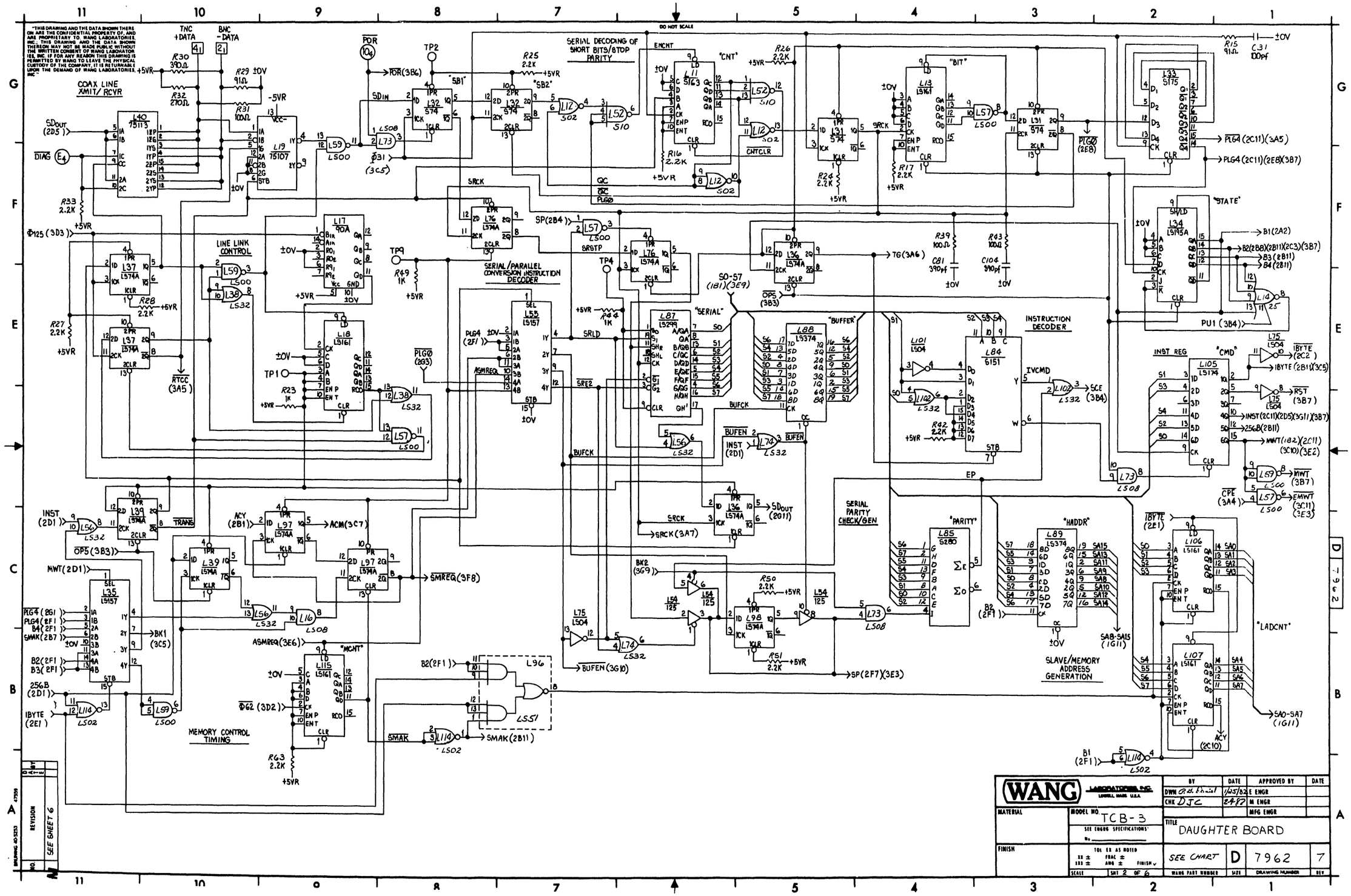
DO NOT SCALE
SADRS (3E7)
SA0-SA7 (2B1)
SA8-SA15 (2B2)
L50 LS158
L70 LS158
L90 LS158
L108 LS158
L10 S240
L30 S240
L69 S139
L64 LS175
L49 S138
L86 LS245
L9 L8 L7 L6 L5 L4 L3 L2 L1
L28 L27 L26 L25 L24 L23 L22 L21 L20
HM4864-3
CASEL (3C7)
RASEL (3D7)
WRM (3B9)
CAS (3C8)
NMISTAT (4E3)
CLRSTAT (4G4)
DIAGADRS (4F9)
ROCDE (4F6)
HEMCNTRL
EIPA (4C7)
PROM I/D (4F10)
HLDP (3E5)
IPL (3E11)
PROM I/D (1A6) (4G4)
PROM I/D (1A7)
SELI (4F3)
BUSAK (4F5)
RESET (4D9)
BPA2 (1E11)
MIEND (3F2)
ENRAS (3F5)
MWT (2D1)
ASMREQ (3E7)
S0-S7 (2E6)
MP 3E2
M0-M7 (4G10)
DSL
RASI
RASD
DSLX
DDAIG
MCAADRS
BUSAK
SCAADRS
MRFSH
MRFSH (4C9) (4D6)
WANG
WANG LABORATORIES, INC. LOWELL, MA U.S.A.
MODEL NO. TCB-3
SEE ENGRG. SPECIFICATIONS
TITLE DAUGHTER BOARD
SEE CHART
D 7962 7
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
SHT 1 OF 6
SCALE
MATERIAL
FINISH
DWN PH Daniel 1/15/82
CHK DJC 2/9/82
E ENGR
M ENGR
MFG ENGR
APPROVED BY
DATE
REVISION
SEE SHEET 6



COAX LINE XMIT/RCVR
SERIAL DECODING OF SHORT BITS/STOP PARITY
LINE LINK CONTROL
SERIAL/PARALLEL CONVERSION INSTRUCTION DECODER
INSTRUCTION DECODER
SERIAL PARITY CHECK/GEN
SLAVE/MEMORY ADDRESS GENERATION
MEMORY CONTROL TIMING
DO NOT SCALE
WANG LABORATORIES INC.
LOWELL, MASS. U.S.A.
MODEL NO. TCB-3
SEE ENGRG SPECIFICATIONS
DAUGHTER BOARD
SEE CHART
D
7962
7
SHT 2 OF 6
SEE SHEET 6

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DO NOT SCALE

INST (2D1) → L75 LS04 → BUFEN (2B7) → L74 LS32 → BK2 (2C6)

L103 LS373: OC, ENB; PT3 (G1), PT2 (J1), PT1 (F1), PT0 (D1), MPE (H1), IPL (J1); +5VR R53 2.2K; MPE (4B10); CPE (3B4); IPL (1B6); 1D–8D, 1Q–8Q → 50-57 (2E6)

WT (C4), PMREQ (B4), +5VR R62 4.7K, TP11, L113 LS02 → PM1RQ (3E8), L74 LS32, WAIT (M)

R58 2.2K +5VR, TP10, M1 (4F11), Φ250 (3C2), L114 LS02, L113 LS02, R60 33Ω, MIC

HLDS, SMREQ (2C8), Φ62 (3D2), L112 574, L111 574, L52 S10 → ENRAS (3D9) (1B4), TP7

HLDP, PM1RQ (3G6), L111 574, R57 33Ω, L51 S00, L53 S11 → HLDP (1B6)

L112 574 → ASMREQ (1B2), L110 S04 → ASMREQ (2B9), L112 574 → SADRS (1G10), L51 S00, L53 S11 → MRDY (4F5)

HLDS, RHLD

TP6, R46 2.2K +5VR, L93 574 (ENRAS (3F5), Φ62 (3E5), RHLD (3F2)) → RASEL (1D9), CASEL (1F3)

MWT (2D1), CPE (3B4), L38 LS32, L91 LS158 (SEL, 1A–4B, 1Y–4Y, STB, 10V), L71 LS32 → L3 RASEL

ZRD (B3), EMWT (2D1), WR (2J3), IPA (4B2), L71 LS32

ECAS (M3), 5X7X (J3), L68 LS08, L66 LS32, L51 S00 → WRM (1C8)

L93 574 (Φ62 (3D2)), L51 S00 → CAS (1C8), L83 125 ×2 (10V) → C3 RD/WR, K3 MRDY, L4 RST

RST (2D1), B2 (2F1), INST (2D1), L77 LS10 (POR (2B8), TG (2F4)), L16 LS08, R19 33K +5VR, C35 .0022μF MICA, L15 9602 (SRCK (2C6), R20 2.2K +5VR), INSTRUCTION ERROR RECOVERY

MOM (2C9), MWT (2D1), PLG4 (2F1), L58 LS74A ×3, BK1 (2B10), 1BYTE (2E1), L16 LS08, L14 S25, +5VR R21 10K, C37 220pf, L15 9602, 10V, L73 LS08 → DPS (2C11)(2E5), R18 2.2K +5VR → PU1 (2E2)

L75 LS04, SCE (2D3), L98 LS74A, L77 LS10 → CPE (3E10)(3C11), CPE (2D1)

L92 S161 (LD, A–D, CK, ENP, ENT, CLR, QA–QD, RCO), TP5, R45 2.2K +5VR

Y1 31.9488 MHZ, +5VR, P5, J2 → #31 (2F8)

L95 LS74A, L53 S11 → M1END (1B4), RHLD (3C9)

R48 2.2K +5VR, R49 2.2K +5VR, R47 2.2K +5VR, TP8, Φ250

EMWT (2D1), SP (2B4), R52 33Ω, MWT (2D1), L102 LS32, L101 LS04, L83 125 → D1 SMWR, MP (1B2)

R61 68Ω, C118 270pf 10V, L110 S04 → Φ62 (3C9), R49 68Ω, C119 270pf 10V → Φ62 (3F8)(3C9)(2B10), R22 68Ω, C90 270pf 10V → Φ125 (2F11)

+5VR, C117 .1MF 35V (T) 10V, R55 10K, R54 150Ω, D1 1N4378A REF 3V, Q1 2N3640

L110 S04 → F3 Φ250, H3 Φ250, Φ250 (3G7), R56 33Ω → D3 Φ500, E3 Φ500

P3 MBSY, N3 M1C, S3 M1D, 4J MP, R3 Φ62, J4 Φ62, F3 Φ250, H3 Φ250, D3 Φ500, E3 Φ500

D 7962

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
MATERIAL	MODEL NO. TCB-3	DWN R.V. Thual	1/15/82	E ENGR	
	SEE ENGRG SPECIFICATIONS No.	CHK DJC	2-4-82	M ENGR	
FINISH	TOL EX AS NOTED .XX ± FRAC ± .XXX ± ANG ± FINISH √			MFG ENGR	
		TITLE DAUGHTER BOARD			
SCALE	SHT 3 OF 6	SEE CHART	D	7962	7
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

DRAWING 40-5253 47799 REVISION BY DATE APPROVED NO. SEE SHEET 6

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DO NOT SCALE

BMI

MO-M7 (1E1)

±OV

+5VR

L42 S373

L41 2716 INTEL

PROMID (1B7)

L68 LS08

MRDY (3E5)

BUSAK (1A6)

L56 LS32

L44 LS195 SH/LD

SELI (1A6)

MI (3G7)

L67 LS04

BMI (9B5)

MREQ (S1)

L65 LS08

PROMID (1B6)

DIAGADRS (1C8)

L66 LS32

L46 S00

RDCDE (1B8)

L43 LS374

MRFSH (1A10)

L81 LS08

L60 LS74

BRFSH

INTA (E1)

RFSH (P1)

L61 LS74

INTPG

L62 LS32

DAB

RESET (1A8)

RESET (B3)

L47 S02

L45 LS175

PGB0

PGB1

DA9

DAI0

L38 LS32

NMISTAT (1C8)

CLRSTAT (1C8)

L63 LS173

DMT (10B)

L101 LS04

DMT

MPE (3E11)

L79 LS74

MPEL

R61 2.2K

LDMT

EIPA (1B7)

MRFSH (1A10)

L65 LS08

R40 2.2K

3M1 (QF10)

IPA (3C11)

INTA

MIREQ

RESET

NMI (9B)

SEE SHEET 6

REVISION

D 7962

WANG	WANG LABORATORIES, INC. LOWELL, MA U.S.A.	BY	DATE	APPROVED BY	DATE
		DWN C. Samuel	10/5/82	E ENGR	
		CHK DJC	2482	M ENGR	
MATERIAL	MODEL NO. TCB-3 SEE ENGRG. SPECIFICATIONS No.			MFG ENGR	
		TITLE DAUGHTER BOARD			
FINISH	TOL ER AS NOTED .XX ± FRAC. ± .XXX ± ANG. ± FINISH √	SEE CHART	D	7962	7
		SCALE	SHT 4 OF 6	WANG PART NUMBER	SIZE / DRAWING NUMBER / REV

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DO NOT SCALE

7962- -R2

COMPONENT SIDE

WANG

Y1 31.9488 MHZ

P4 P3 P2 P1

S A

REVISION	BY	DATE
SEE SHEET 6		

	BY	DATE	APPROVED BY	DATE
DWN PG Bonnell		1/25/82	E ENGR	
CHK DJC		2-4-82	M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL	MODEL NO TCB-3 (SEE ENGRG SPECIFICATIONS Rx ____)	TITLE DAUGHTER BOARD		
FINISH	TOL ± : AS NOTED; .XX ± .XXX ± ANG ± FINISH	SEE CHART	D	7962 7
	SCALE	SHT 5 OF 6	WANG PART NUMBER	SIZE / DRAWING NUMBER / REV

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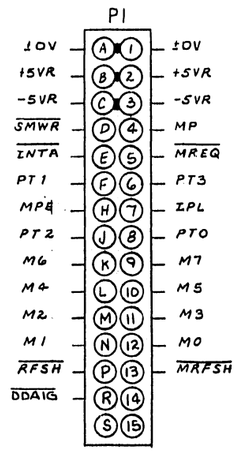
DO NOT SCALE

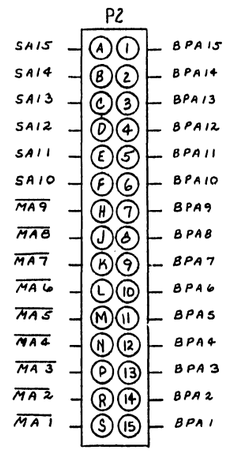
I.C. LOCATION	TYPE	W.L. PART NO.
L1-9, 20-28	HM4864-3	SEE CHART
L10, 30	74S240	376-0334
L11	74S163	376-0235
L12, 47, 113	74S02	376-0199
L13, 18, 106, 107, 115	74LS161	376-0233
L19	7425	376-0092
L15	9602	376-0104
L16, 65, 68, 73, 81	74LS08	376-0153
L17	7490A	376-0073
L19	75107	376-0146
L29	74S08	376-0200
L31, 32, 93, 94, 111, 112	74S74	376-0202
L33	74S175	376-0270
L34, 44	74LS195A	376-0248
L35, 55	74LS157	376-0216
L36, 37, 39, 58, 60, 61, 76, 77, 80, 95, 97, 98	74LS74A	376-0155
L38, 56, 62, 66, 74, 102	74LS32	376-0211
L40	75113	376-0256
L41	2716	SEE CHART
L42	74S373	376-0306
L43, 88, 89	74LS374	376-0286
L45, 64	74LS175	376-0160
L48	74S03	376-0556
L57, 59	74LS00	376-0207
L114	74LS02	376-0208
L49	74S138	376-0298
L50, 70, 90, 91, 108	74LS158	376-0293
L46, 51	74S00	376-0228
L52	74S10	376-0238
L53	74S11	376-0237
L54, 83	74125	376-0324
L63	74S139	376-0333
L63	74LS173	376-0289
L105	74LS174	376-0159
L67, 75, 101	74LS04	376-0180
L71	74S32	376-0205
L110	74S04	376-0197
L77	74LS10	376-0209
L78, 82, 99, 100, 104, 109, 116, 117, 118	SPARE	
L84	74S151	376-0336
L85	74S280	376-0246

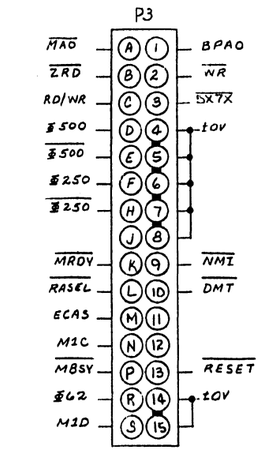
I.C. LOCATION	TYPE	W.L. PART NO.
L86	74LS245	376-0285
L87	74LS299	376-0303
L92	74S161	376-0278
L96	74LS51	376-0213
L103	74LS373	376-0310
L1-9, 20-28	16 PIN SOCKET	376-9002
L41	24 PIN SOCKET	376-9003

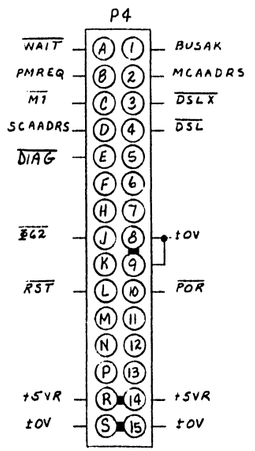
COMPONENT	TYPE	W.L. PART NO.
R1-3, 12-14	47Ω 1/4W 5%	330-1048
R4-11	66Ω 1/4W 5%	330-1057
R15, 29	91Ω 1/4W 5%	330-1092
R16-18, 20, 24-28, 33, 40-42, 45-48, 50, 51, 53, 58, 59, 63.	2.2K 1/4W 5%	330-3023
R19	33K 1/4W 5%	330-4034
R21, 55	10K 1/4W 5%	330-4011
R22, 61, 64	68Ω 1/4W 5%	330-1069
R28, 34, 44, 49	1K 1/4W 5%	330-3011
R30	390Ω 1/4W 5%	330-2090
R31, 39, 43	100Ω 1/4W 5%	330-2011
R32	270Ω 1/4W 5%	330-2028
R52, 56, 57, 60	33Ω 1/4W 5%	330-1034
R54	150Ω 1/4W 5%	330-2016
R62	4.7K 1/4W 5%	330-3048
C1-9, 20-28	1UF(HF) 50V	300-1931
C10-19, 29, 30, 32-34, 36, 38, 39, 41-75, 77-80, 82-103, 105-114	.047UF 50V	300-1966
C31	100PF 500V	300-1100
C35	.0022UF 500V MICA	300-5012
C37	220PF 500V	300-1220
C40, 118, 119	270PF 500V	300-1270
C81, 104	390PF 500V	300-1390
C115, 116, 120	15UF 20V(T)	300-4022
C117	.1UF 35V(T)	300-4002
D1	IN4372A	380-2129
J1	5 PIN HDR.	654-1197
J2	2 PIN HDR.	350-0203
Q1	2N3640	375-1003
FS	SHUNT	350-4500
Y1	31.9488 MHz	321-1002

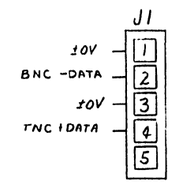
MNEMONICS	COORD.
BNC-DATA	2610
BPA0 - BPA15	1611
BUSAK	1A11
$\overline{DDTAG}$	1A11
$\overline{DMG}$.	2F11
$\overline{DMT}$	4B11
$\overline{DSL}$	1C1
$\overline{DSLX}$	1A11
ECAS	3B11
$\overline{INTA}$	4E11
IPL	3E11
MA0-MA8	1F1
$\overline{MBSY}$	3G1
MCAADRS	1A11
MP	3E1
MPE	3E11
$\overline{MDRY}$	3A8
$\overline{MREQ}$	4E11
$\overline{MRFSH}$	1A11
M0-M7	1F1
$\overline{M1}$	3G8
M1C	3G1
M1D	3G1
$\overline{NMI}$	4A5
PMREQ	3G7
$\overline{POR}$	2G9
PT0 - PT3	3F11
$\overline{RASEL}$	3A9
RD/WR	3A8
$\overline{RESET}$	4D11
$\overline{RFSH}$	4E11
$\overline{RST}$	3A7
SCAADRS	1A11
$\overline{SMWR}$	3E1
SA10 - SA15	1C11
TNC+DATA	2610
$\overline{WAIT}$	3G4
$\overline{WR}$	3C11
$\overline{2RD}$	3C11
$\overline{5X7X}$	3B11
$ 62	3E1
$\overline{$62}$	3E1
$ 250	3C1
$\overline{$250}$	3C1
$ 500	3C1
$\overline{$500}$	3C1





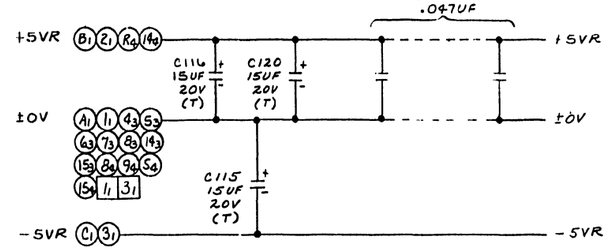






TYPE	I.C. LOC.	SPARES
74S00	L46	2
74S02	L12	1
	L47	1
	L113	2
74S03	L48	1
74LS04	L67	3
	L101	1
74S08	L29	2
74LS08	L65	1
74LS51	L96	1
74125	L54	1
	L83	2

210 - 209 + 377 OR 378				
210	209	L1-9	L20-28	L41
7962A	7962	377-0466	377-0466	378-5137
7962-1A	7962-1		377-0466	



NOTE: ALL RESISTORS 1/4W 5% UNLESS OTHERWISE SPECIFIED.

7962 E-REV	7962-1 E-REV
1	0

NO	REVISION	DRWN	CHK'D	APP'D	DATE
0	ORIGINATED PER DWR # E1485 APP'D: D.J.C.	PGD	D.S.	JEP	4-16-82
1	REVISED PER ECO# 22250 APP'D: D.J.C.	PGD	D.S.	JEP	6-8-82
2	REVISED PER ECO# 23228 APP'D: D.J.C.	PGD	D.S.	JEP	7-20-82
3	REVISED PER ECO#24452 APP'D:	PGD	D.S.S.		11-19-82
4	REVISED PER ECO#25096, 25153 APP'D: D.J.C.	PGD	D.S.S.		11-19-82
5	REVISED PER ECO#25594 APP'D:	PGD	E.O.S.		12-8-82
6	REVISED PER ECO# 25697 APP'D:	PGD	KM'D		12/30/82
7	REVISED PER ECO# 25945 APP'D:	PGD	F.S.S.		2-3-83

DRAWING 40-5253 4809/2

	BY	DATE	APPROVED BY	DATE
	DWN PG Daniel	11/25/82	E ENGR R GREEFKIN	2-4-82
	CHK'D J. CABIN	2-4-82	M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MA. U.S.A.

MATERIAL

MODEL NO. TCB-3

SEE ENGRG SPECIFICATIONS No.

TITLE DAUGHTER BOARD

FINISH

TOLERANCES AS NOTED

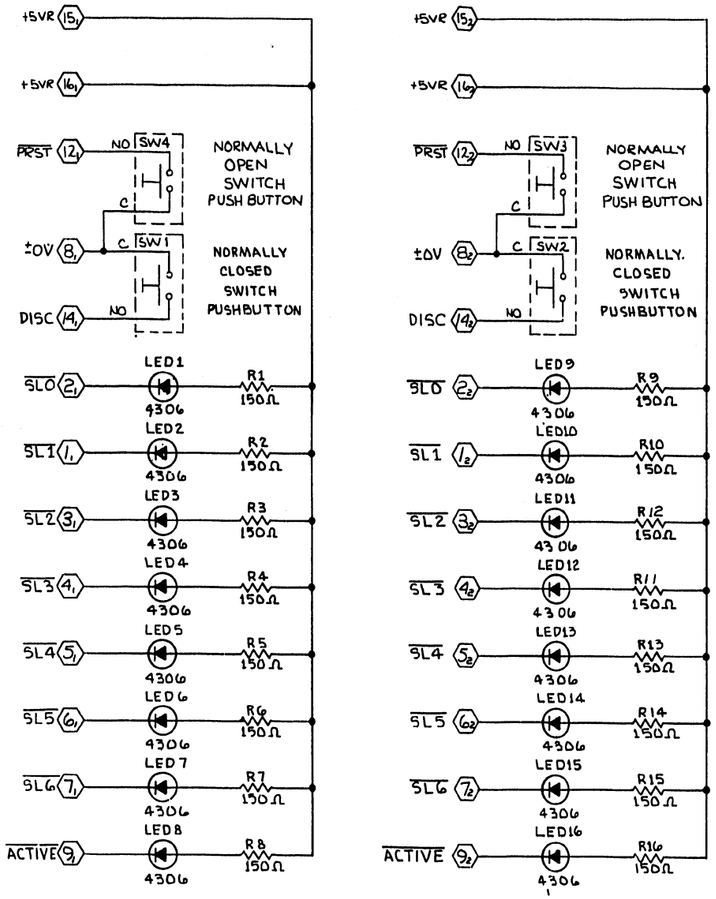
SCALE SHT 6 OF 6

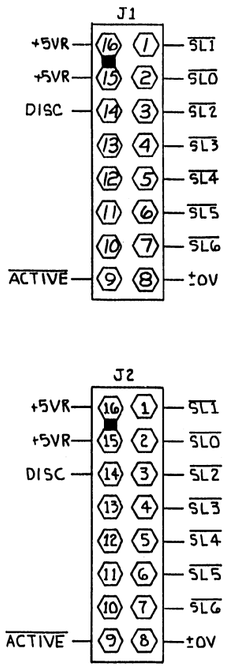
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	7962	7

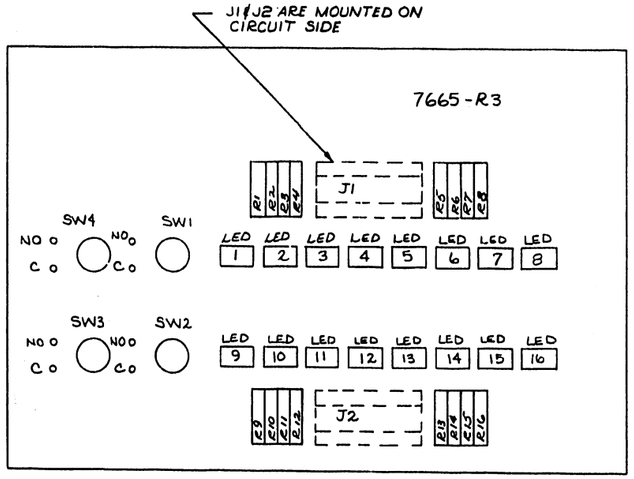
D 7962

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

DO NOT SCALE







MNEMONIC	CO'ORD
ACTIVE	C11, C9
DISC	E11, E9
SL0	E11, E9
SL1	E11, E9
SL2	D11, D9
SL3	D11, D9
SL4	D11, D9
SL5	C11, C9
SL6	C11, C9

COMPONENT	TYPE	W.L. PART NO.
R1-16	150Ω 10% 1/4W	330-2015-4B
LED1-16	4306 2.5V (RED)	370-0031
J1,2	16 PIN CAMBION SOCKET	376-9005
SW1,2,3,4	PUSH BUTTON SWITCH	279-0300

E-REV [0]

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWR#E865 APP'D: [illegible]	S.D.B.	3-20-80
1	REVISED PER ECN#15629 APP'D: [illegible]	JEP	10-14-80
2	REVISED PER ECO#20272 APP'D [illegible]	KMT	10/7/81

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	S.D.B.	3-20-80	E ENGR [illegible]	4/9/80
CHK	[illegible]	4/9/80	M ENGR	
			MFG ENGR	

MATERIAL —||—

MODEL NO. TCB-1

SEE ENGRG. SPECIFICATIONS No.

TITLE LIGHT BOARD

FINISH —||—

TOL. EX. AS NOTED XX ± XXX ± FRAC. ± ANG ± FINISH ✓

SCALE —||— SHT 1 OF 1

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7665	D	7665	2

D 7665

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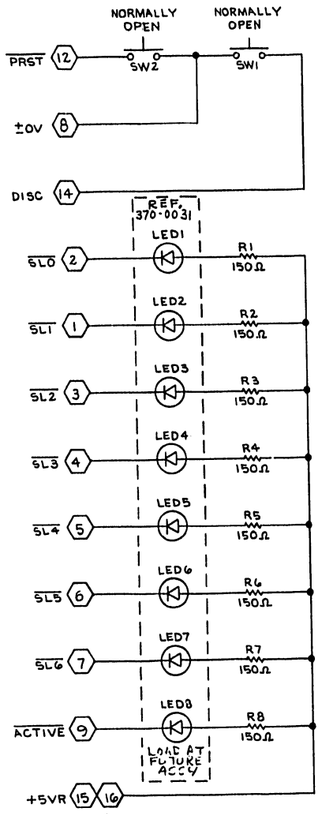
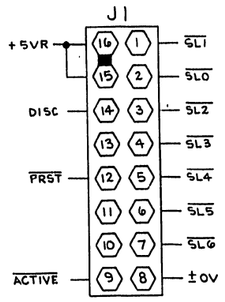
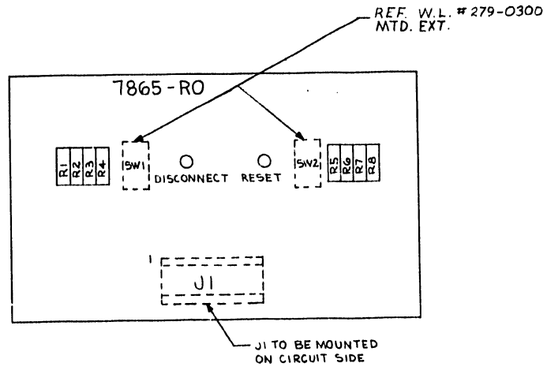
DO NOT SCALE







MNEMONICS	COOR'D
ACTIVE	1C11
DISC	1F11
PRST	1F11
SL0-SL6	1E11
±0V	1F11
+5VR	1C11

COMPONENT	TYPE	W.L. PART NO.
R1-8	150Ω 10% 1/4W	330-2015
J1	16 PIN SOCKET	376-9005

E-REV 0

NO.	REVISION	BY	DATE
0	ORIGINATED PER DWR #E1017 APP'D: [illegible]	E.D.B.	11-5-80
1	REVISED: PER ECO #1897 APP'D: [illegible]	FSS	5-1-81

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	E.D.B.	11/5/80	E ENGR	[illegible]
CHK	[illegible]	[illegible]	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. TCB-1

SEE ENGRG SPECIFICATIONS No.

TITLE LIGHT BOARD

FINISH

TOL EX AS NOTED XX ± XXX ± FRAC ± ANG ± FINISH

SCALE SHT 1 OF 1

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7865	D	7865	1

D 7865

END