VICTOR®

V9000/S1

HARD DISK SUBSYSTEM

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PREFACE

The purpose of this manual is to provide a source of technical information on the V9000/S1 Microcomputer Hard Disk Subsystem. Although intended for Service Engineers, anyone interested in specifications, architecture, functional theory or maintenance practices will find this manual helpful.

Sections of this manual cover:

* Introduction to Winchester Technology
* Overview of Hard Disk Subsystem
* Winchester Drive Handling Precautions
* Host Interface
* Winchester Drive Interface
* Winchester Disk Drives
* Module Replacement Guide
* Diagnostic Software
* Hard Disk Subsystem Error Reporting

Familiarity with the V9000/S1 microcomputer operation, hardware configuration, and comprehension of the MS/DOS Operating System is recommended before proceeding with this manual.

Logic conventions used throughout this manual may vary as follows; High (true) signals will always be written as in the following example (CLK, WR, RD, DMA-ON, etc.), Low (true) signals might vary as in the following example (CLK/ or $\overline{\text{CLK}}$ or -CLK).

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1. GENERAL INFORMATION

1.1 INTRODUCTION TO WINCHESTER TECHNOLOGY

The term Winchester comes not from an inventor's name, but from the code name IBM assigned to the development of the Model 3340 disk memory, which was introduced in 1973. The industry as a whole has borrowed the Winchester name and now generally uses it to describe any disk drive using similar technology. The key element of Winchester technology is that the head-to-disk assembly (HDA) is sealed from outside air and the disk is generally non-removable.

In some ways, Winchester technology is similar to conventional hard-disk drives. As with conventional hard disks, the read/write head floats over the recording medium on an air cushion that keeps the head from contacting the disk. In the case of the Winchester, however, the sealed and extremely clean enviroment of the HDA permits the disk designer to "fly" the read/write head closer to the disk surface. In typical removable-media hard-disk systems, the read/write head flies 60 to 70 microinches above the disk surface. The limitation on the distance the head flies above the disk is based on the minimum distance the head can fly safely above the disk and not risk contact with dust or any other contaminant on the disk. Any contact of this type causes the head to stop flying and crash on the disk surface. Such a crash normally ruins the read/write head and the surface of the disk medium, results in a complete loss of data, and necessitates an expensive repair job. Sealing the HDA in a Winchester drive provides a substantially cleaner environment than that of removable-media disks and allows the designer to fly the head about 20 microinches over the disk surface. This lower head altitude provides higher magnetic flux densities at the recording surface and thus higher recording densities on the disk.

During the read/write/seek operations, the Winchester head flies above the surface of the hard disk platter on an air bearing, supported by carefully balanced aerodynamic forces. As the disk starts or stops, the head takes off or lands from the silicone-lubricated surface of the platter.

A Winchester drive has one or more rigid disks (or platters) typically 5 1/4 inches in diameter. Each disk is coated on both sides with a magnetic medium, usually iron oxide, so that two surfaces per disk are available for the storage of data. The platters are also coated with a silicon lubicant to allow takeoff and landing of the heads.

Each Winchester head has three rails, or raised surfaces. The trailing end of the middle rail holds a magnetic core with wire

coiled around for writing and reading the data. The two outer rails govern the flow of air. The force that results is sufficient to support a weight of 10 grams at a height of half a micrometer above the disk.

Winchester drives have a number of advantages over conventional hard-disk drives. First, they are very low cost both in absolute terms and in terms of cost per bit of storage capacity. In addition, the sealed enviroment of the HDA produces extremely high reliability with MTBF (mean time between failure) figures quoted in excess of 8000 hours. Winchester disk drives also require no preventive maintenance such as changing air filters or cleaning and aligning heads. The primary disadvantage comes from the fact that the storage medium (the actual disk platter) is not removable. This prevents us from backing up data files in the conventional way (that is, by making and storing an exact copy of the disk to be backed up). However, this problem is overcome in systems that have a floppy disk drive such as the V9000/S1 Hard Disk System. Important files may be periodically backed up and kept on floppies in the event of a crash or media failure.

1.1.1 UNDERSTANDING WINCHESTER DISK OPERATION

A Winchester disk is similar to any other disk system in terms of operation and organization. The disk (or platter) can be considered to be composed of concentric tracks of recorded information. Each track is further subdivided into sectors. A typical 5 1/4 inch Winchester drive system may contain upwards of 40,000 individual sectors, each containing its own sector address information and data-storage space. Each track is also contained in what is known as a cylinder. On a single platter Winchester drive a cylinder would contain two tracks, one from the upper surface and one from the lower surface. On a four platter drive the cylinder would contain four tracks, one from the upper and lower surface of each platter. When performing a read/write/ or seek operation the head mechanism, whether two or four heads, positions itself at a certain cylinder and then performs a read or write by turning on one of it's heads.

As the following discussion will show, the operation of a Winchester disk is very similar to that of standard floppy disk drives. The major difference is the speed of operation and the amount of data that a Winchester can hold.

Probably the easiest way to understand disk operation is to go through the steps involved in seeking and reading data on a particular sector of the disk. As the first step in the process, the controller moves the read/write head mechanism to the cylinder containing the desired track by sending control signals to the disk drive. When the read/write head stack is on the proper cylinder, the controller then waits for a specific portion

of the disk called the index position (or mark) to pass under the head. This index position provides orientation information which identifies the start of all tracks. Through interpretation of the command from the controller the proper head is then activated to read a particular track once the index mark is found. The controller begins reading the serial data coming from the disk, looking at the sector address information for each sector until it locates the address indicating the desired sector. The data immediately following this address is then captured and the read is completed.

A disk write operation is performed similarly. The same sequence of events occurs until the controller locates the proper sector. At this point, instead of reading data from the disk, the controller sends new data to the disk for recording.

The final point to be covered is how the sector-address information is put on the disk in the first place. This process is called formatting. When a disk is formatted, the controller starts on track 0 and, following the index mark, writes the sector-address information for the first sector on the disk. It then fills the data area following the first address with nulls or other characters to reserve the data space for future use. As soon as it has filled the area, the controller begins the process over again for the next sector, writing the sector-address information and then reserving the data area. This process continues until all the sectors on the first track of the platter are formatted. The controller then formats the remaining tracks in this same manner.

1.2 OVERVIEW OF HARD DISK SUBSYSTEM

The V9000/S1 Hard Disk Subsystem consists of three major hardware components; The Winchester Disk Drive, Xebec S1410 Controller, and the Direct Memory Access Interface Board (DMA). The DMA Board resides in a slot of the System Expansion Bus. It connects to the controller via the SASI (Shugart Associates System Interface) cable. The controller connects to the disk via two short cables that comprise an ST506 style interface. ST506 refers to the Seagate Technology drive "model 506", which first used this interface. The disk drive is a 5 1/4 inch Winchester with a formatted capacity of approximately 10.6 megabytes. The disk controller is a Xebec S1410. It performs physical level control of the disk, e.g. move the heads, turn on write current, and return status to the host. It accepts sector oriented commands from the host, e.g. read 64 sectors of data starting at sector 100. The DMA board provides an interface from the host system onto the SASI bus and hence to the controller. The DMA board transfers data between system memory and the Hard Disk Subsystem without CPU intervention.

1.3 WINCHESTER DRIVE HANDLING PRECAUTIONS

Winchesters are delicate instruments that require proper care and handling. These units are expected to perform when needed, therefore misuse and/or mishandling will adversely affect the expected performance.

Even though a Winchester Drive is installed in a system it's succeptability to damage is still great. Systems should be given at least 15 seconds on power up or down before movement of the unit. Units should be packed in original shipping containers whenever possible and marked as extremely fragile.

Individual drives should be handled with extreme care. The Winchester Drive can be carried easily in one hand and thus taken for granted. This type of handling exposes the drive to unintentional shock forces and should be avoided. When individual drives are returned they must be packed in a single-pack shipping container (part #187125-01). If more than one drive is returned they must be packed four to a box using the proper shipping container (part #187125-02). When these containers are not readily available packing procedures must adhere to the following guidelines:

SINGLE DRIVE SHIPPING REQUIREMENTS

Single drives must be protected by at least 4 inches of polyurathane foam on all sides (2072 foam), and placed in a cardboard box whose dimensions assure no movement of the drive. (cardboard box specifications: 175 lb test, RSC double wall, #3W, 2P/1C)

MULTIPLE DRIVE SHIPPING REQUIREMENTS

When more than one drive is to be returned, no more than four drives are permitted per container. The drives may be placed next to each other but separated by a 200 lb test RSC single wall cardboard divider. The four drives must be tightly packed in no less than 6 inches of polyurathane foam (2072) on all sides and placed in a cardboard box whose dimensions assure no movement of the drives. (cardboard box specifications: 200 lb test, RSC double wall, #3W, 2P/1C)

The following is a list of do's and don'ts concerning Winchester Drives:

* Drives should be placed on a foam pad when not in a system or shipping container.

* Never stack drives, even if protected by foam.

* No moving parts should be moved, e.g. spindle hub or positioning mechanism.

* The sealed drive assembly should never be opened for any reason.

* If reformatting of the drive is necessary, allow at least 45 minutes of "power on time" before proceeding.

Note: Refer to Technical Bulletin #581-228-SB31 for more information concerning returned drives.

2. HOST INTERFACE

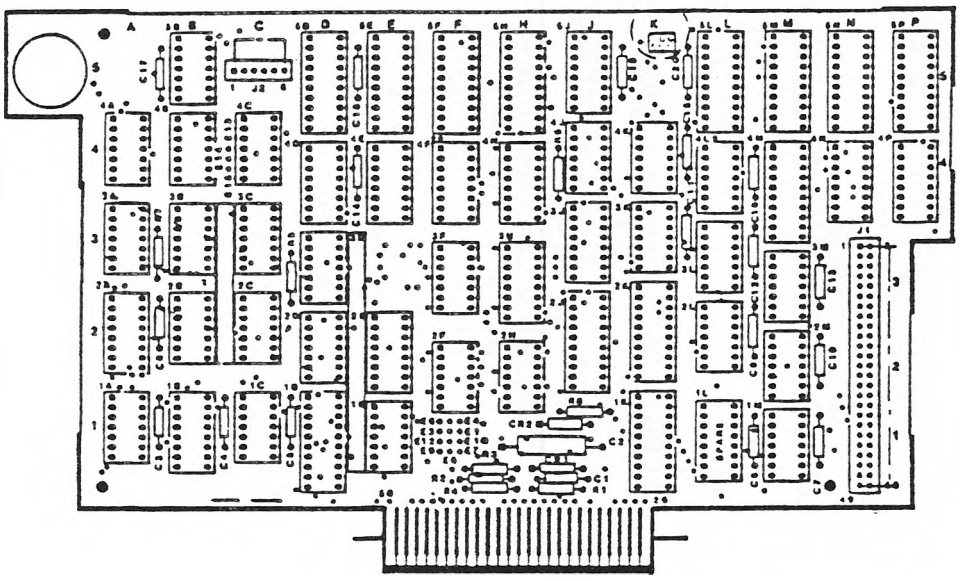
2.1 DIRECT MEMORY ACCESS BOARD (DMA)

The Direct Memory Access Board makes it possible to transfer large arrays of data between the hard disk and system memory without CPU intervention. This task would be very time-consuming, due to the amount of instructions needed to accomplish the transfer, if DMA were not used.

2.1.1 PHYSICAL DESCRIPTION

The DMA board shown in Figure 2.1, when installed in the system, may reside in any slot of the expansion bus. The board is keyed in such a way that the component side of the board is always facing the outside of the mainframe when installed.

There are three connectors on the board, J1 (50 pins), P1 (50 pins), and J2 (6 pins). J1 connects the DMA board to the hard disk controller via a 50 pin flat ribbon cable. When connecting this cable make sure pin one (red key of cable) is connected appropriately to pin one of the DMA board and Xebec Controller. Edge connector P1 is inserted into the system expansion bus. Connector J2 is the bus arbitration link if more than one DMA board is used on the expansion bus.

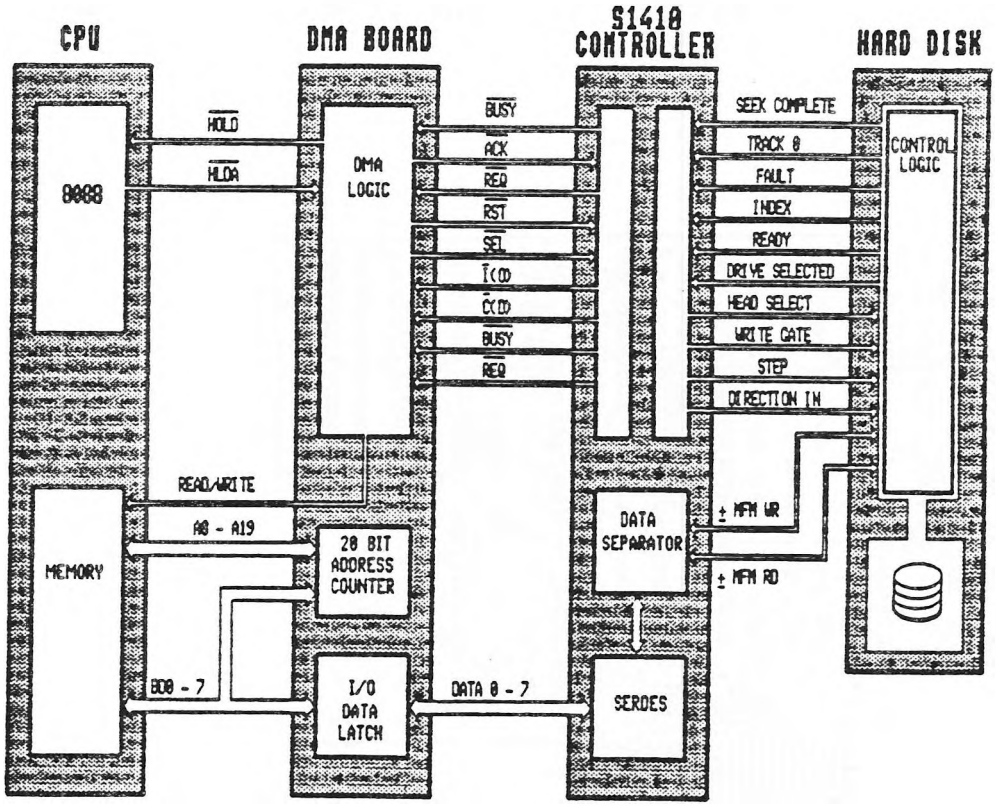


DMA BOARD (DIRECT MEMORY ACCESS)
Figure 2.1

2.1.2 FUNCTIONAL DESCRIPTION OF DMA TRANSFER

Before any transfer of data to or from the hard disk the DMA Board must be selected. The 8088 addresses the DMA Board at EF300. Once the DMA Board has been selected (DMA-ON), CSEL/ (Controller Select) is generated to the Xebec Controller. The hard disk controller responds with a Controller Request (CREQ) asking for what type of transfer is to take place (Command, Data, or Status). The DMA board recognizes CREQ, issues a HOLD to the 8088 and takes control of the bus for transfer of data to or from the hard disk through a handshake sequence (see section 3.1.4.2).

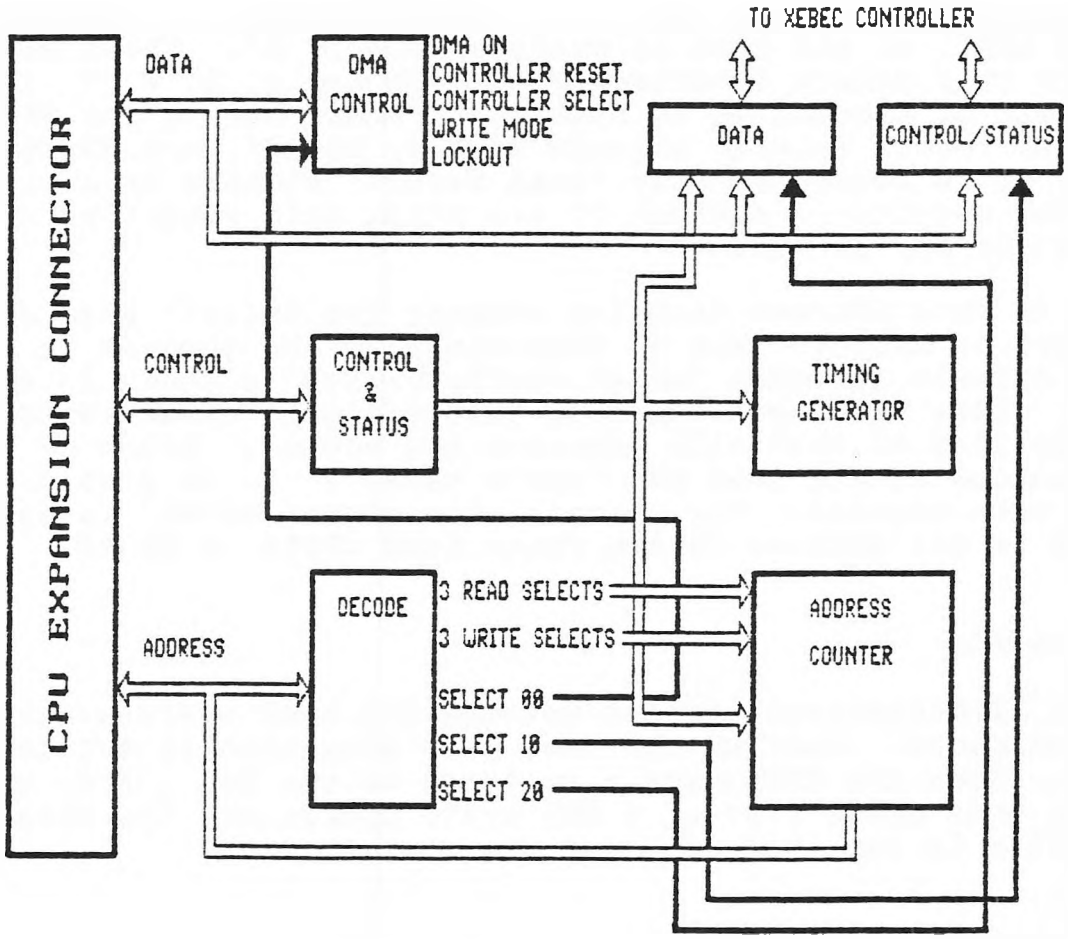
Control information is supplied to the DMA logic to specify an input or output (READ or WRITE) operation in memory. The address register is loaded with the starting address, and a data exchange between the memory and the hard disk is executed. Following each transfer, the address register is incremented to select the next memory location. When the information exchange is completed, the hard disk controller issues a control command which resets the Hold Request line to the processor. This allows the microcomputer to continue with a normal programmed sequence. (See Figure 2.2)



DMA Transfer Block Diagram
Figure 2.2

2.1.3 DMA BOARD THEORY OF OPERATION

The following sections contain information which should be useful to the persons involved in component level repair of the DMA Board. Refer to Figure 2.3 (DMA Board Functional Block Diagram) shown below, and Figure 2.4 (DMA Board Functional Timing Diagram) on page 2-6, as needed.



DMA Board, Functional Block Diagram
Figure 2.3

2.1.3.1 Host Bus Interface

Refer to sheet 2 of the DMA Board Schematic, Figure 2.5, for the following discussion.

Address Decoding

The lower half of sheet 2 shows the Host Bus Address Decoding Logic.

Address lines A12 thru A19, plus signal IO(M/) are decoded by IC's 1E and 2E to produce a "Board select" signal. Board Select is used to enable further decoding of address lines to generate chip select signals. Board Select is also buffered by open-collector gate 3F to generate the EXT IO/ signal to the host. This signal disables the host's buffer for on-board I/O devices.

Octal latch 2K freezes the state of the multiplexed address/data bus (IDB0 thru IDB7) at ALE time to produce A4 thru A7. These address lines drive chip select decoding logic composed of IC's 3K, 3H, and 3J. One half of decoder 3H is enabled by board select and WR/, thus, it generates "Write Select" signals WS-80/, WS-A0/, and WS-C0/. The other half of 3H generates only "Read Select" signals in a similar manner. The outputs of decoder 3J are three chip select signals unqualified by RD/ or WR/.

Note that in this address decoding scheme, the default base address of the board is EF300. This is determined by the jumpers at E1 thru E12. The default (etched) jumper configuration is shown in the schematic. Note also that the chip select signal names indicate the value of A0 thru A7 that will generate the signal. Since A0 thru A3 are not decoded at all they are "don't cares". A4 is also a "don't care" for some signals. For example, the signal WS-80/ is generated by a write to any address in the range from EF380 to EF39F.

Data Bus Buffer

IC 1K is a bi-directional buffer between the host address/data bus and the DMA board. Most of the time 1K's direction is driving the DMA board. When the CPU reads a register on the DMA board, and during the data phase (T2) of a DMA write operation, the direction of the buffer is reversed to drive the host bus.

Control Register

Octal latch 2J is a write only register used to control various functions of the DMA board. Latch 2H conditions the output of 2J to enable/disable DMA mode. The primary function of 2H is ensure that following a system reset the DMA function is disabled.

2.1.3.2 Controller Interface

Refer to sheet 3 of the DMA Board Schematic, Figure 2.5, for the following discussion.

Data Out Latch and Bus Driver

Data from the host to the controller is latched by IC 5L and

driven onto the SASI Bus by the tri-state driver 5P. IC 5P is enabled only when the SASI Bus status line I(O/) is in the output state (low).

Write Strobe Selector

Data that is read from system memory during a DMA cycle must be latched into IC 5L at just the right moment during the read. If this is a read from "on-board" memory (lo-ram) then the correct moment is the falling edge of DLATCH/. If this is a read from expansion memory then the correct moment is the falling edge of T4/. If this is not a DMA cycle at all, i.e. the CPU is writing directly to the controller, then the correct time is the end of the WR/ strobe (the falling edge of HWR). Selection of the appropriate write strobe is accomplished by the logic of IC's 2L, 4L, and 3L.

Bus Receiver and Data In Latch

Data from the SASI Bus to the host is received by IC 5N. This is an inverting buffer with PNP inputs to minimize loading on the bus. In addition it has hysterisis to provide extra noise immunity. To minimize ringing, resistor packs 4P and 4N terminate the bus in a resistance that approximates the characteristic impedance of the bus. The output of 5N is latched into 5M by the falling edge of CREQ. Data from the bus is guaranteed to be valid while CREQ is true.

Read Strobe Enable

The output of tri-state latch 5M is driven onto the DMA data bus when DRD/ is true. DRD/ is true during T2 of a DMA write cycle or during a CPU read of the SASI Data Bus.

Controller Status In Buffers

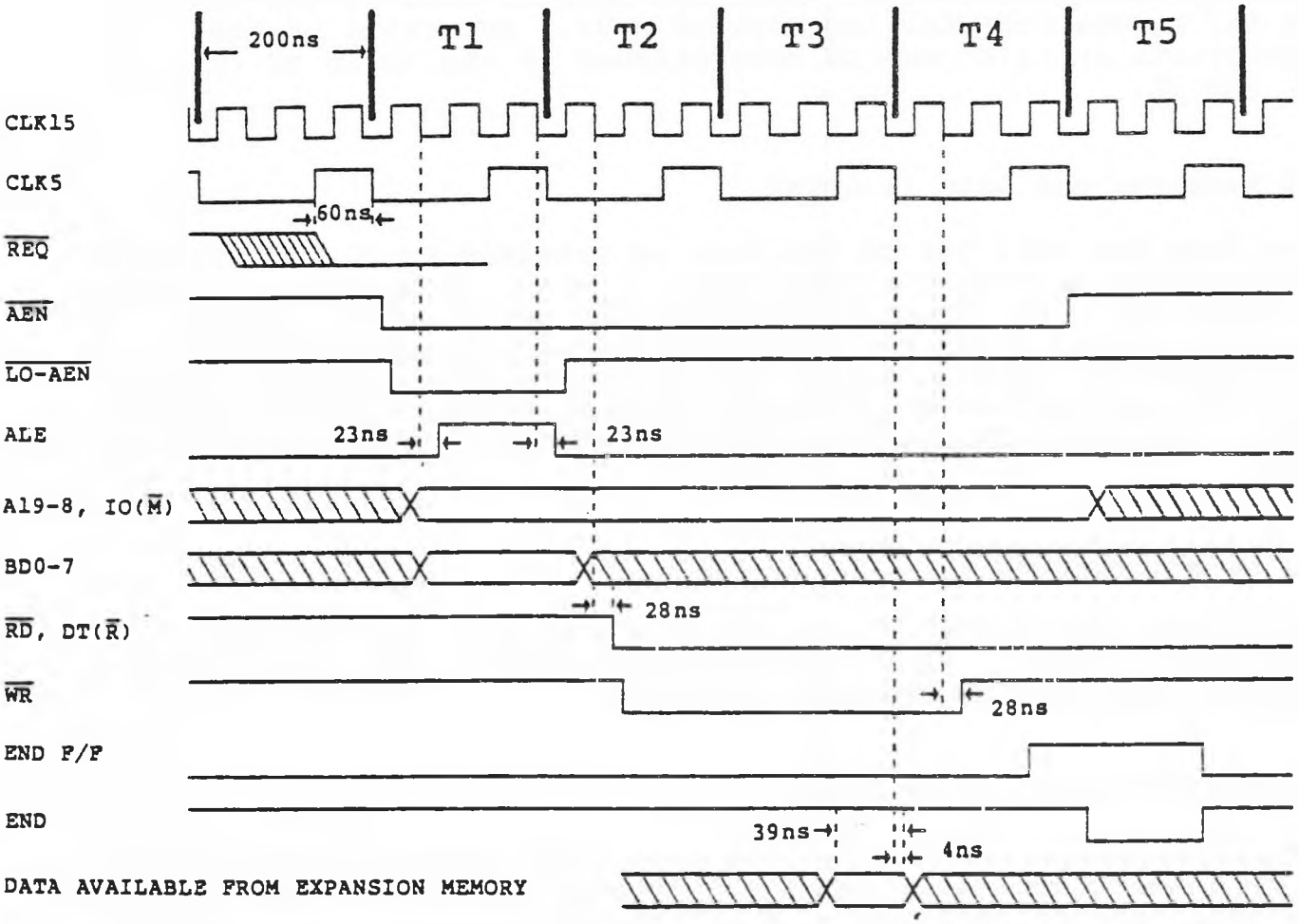
Inverting buffer 4M receives the controller status signals I/(O), -C(D), BUSY/, REQ/, and MSG/. The output of 4M is driven onto the DMA data bus during a CPU read of controller status, i.e. when IC 3M detects HRD/ and S20/ as true.

Controller Reset, Select, and Acknowledge Lines

These three signals are driven onto the SASI bus by open collector buffer 1M. The reset signal (RST/) is caused by a hardware reset at 3M-9 or a programmed reset (CRST) at 3M-10. CRST can be activated by writing to the control register. The RST/ signal is

normally active only for a single pulse during system initialization.

Controller select (SEL/) is activated by writing to the control register. It is pulsed at the beginning of every controller command. Controller acknowledge (ACK/) is generated after the host has read or written a byte of data in response to the controllers request signal (REQ/). See Section 2.1.3.4 for a description of the Acknowledge Logic.



DMA Board Functional Timing Diagram
Figure 2.4

2.1.3.3 DMA Timing Generator

Refer to the top half of sheet 4, DMA Board Schematic (Figure 2.5), for the following discussion.

Shift Register and End Flip-Flops

The five flip-flops contained in IC's 1A and 1B are wired as a shift register clocked by the falling edge of CLK5. A DMA cycle begins when a START/ pulse at OR Gate 2B is clocked into the first cell of the shift register. The output of this cell is fed back to OR gate 2B to hold the start signal. The start signal propagates into succesive cells with each falling edge of CLK5 until finally it is clocked into the END flip-flops with the rising edge of CLK5. The output of the END flip-flops ANDed with CLK5 low generates an END pulse that resets the shift register. The output of the shift register is five staggered timing signals: AEN (T1), T2, T3 (not used), T4, and T5 (END). AEN goes true first, followed by T2 200ns later and so on with T3, T4, and T5.

Host Bus Control Decoding

The staggered timing signals from the shift register are decoded by NAND gates 1C and 2B to generate the host bus control signals; ALE, RD/, and WR/. These are latched by 1D on the falling edge of CLK15. This is to eliminate decoding transients. Latch 1D also provides tri-state bus driving capability. It is enabled onto the host bus during AEN. Pull-up resistors R2, R3, and R4 prevent RD/, WR/, and DT(R/) from floating during bus exchange between the CPU and DMA. Likewise, R1 and other components form a constant-current pull-down network to prevent ALE from floating to an active state.

2.1.3.4 Controller Acknowledge Logic

Refer to sheet 4 of the DMA Board Schematic, Figure 2.5, for the following discussion.

On sheet 4 of the schematic, zones (B thru C) by (6 thru 8) contains the Controller Acknowledge Flip-Flops. The Write Acknowledge Flip-Flop is set by DWR/. This happens whenever the CPU or DMA writes data to the SASI bus. The Read Acknowledge Flip-Flop is set whenever the CPU or DMA reads the SASI data bus.

2.1.3.5 Bus Request Logic

Refer to the bottom half of sheet 4, DMA Board Schematic (Figure 2.5), for the following discussion.

New Request Latch

New Request Latch, 3D, is set every time the controller asserts CREQ and with C(D/) in the data state, i.e. bus requests are not generated by controller requests for command or status byte transfer. In addition, DMA-ON must be true. When a DMA cycle is actually granted the New Request Latch will be cleared during T2. The output of the New Request Latch drives the DMA start logic on sheet 6 of the schematic, and Bus Request Latch, 3D.

Hold Request Latch

The Bus Request Latch generates a hold request (HOLD/) to the CPU, synchronous with CLK5. Unlike the New Request Latch, this latch is not necessarily cleared by a DMA cycle. If CPU LOCKOUT mode is programmed then gates 2B and 2C form a feedback path to keep the bus request latch set until a RELEASE/ signal is applied to its clear input. RELEASE/ is caused by either a RESET signal or a controller request time out.

Request Time-Out Counter

IC 2A counts the number of CLK5's between controller requests. If the count reaches 16 then a signal is generated to release the bus to the processor. This is to ensure that the bus is released between sector bursts of a multi-sector transfer.

2.1.3.6 Interrupt Request Latch

Refer to sheet 4 of the DMA Board Schematic, Figure 2.5, for the following discussion.

When the controller requests the transfer of command or status bytes, Interrupt Request Latch 3C is set. Thus IR4 (optionally jumperable to IR5) is asserted to the Programmable Interrupt Controller on the CPU board. The interrupt latch is cleared by a CPU read of SASI bus status.

2.1.3.7 Bus Arbitration Logic

Refer to sheet 6 of the DMA Board Schematic, Figure 2.5, for the following discussion.

When more than one DMA board (or Bus Master) is used in the system the bus arbitration logic is used to prevent bus contention between the peripheral devices, their respective DMA board, and the host memory via the 6 pin connector "J2" located on the top edge of the board.

Hold Acknowledge Chain

The jumper configuration in the upper left corner of sheet 6 allows HLDA (Hold Acknowledge) to be chained from the "primary" bus master board (DMA board for example) to another bus master board. The primary bus master board being the first in line to receive HLDA from the 8088 via the expansion bus. With the second DMA board strapped E14-E13 HLDA is asserted via the primary bus master board. If signal LCL-HREQ/ (Local Hold Request) is true HLDA is prevented from entering the next bus master board indicating the primary board is contolling the bus.

Start Logic

The START/ signal from nand gate 5B pin 6 is used by the DMA Timing Generator (sheet 4) to begin a DMA cycle. To accomplish this HLDA from the 8088 must be true at 5B pin 1, a request must have been generated by the controller to assert NEW-REQ at 5B pin 4, LCL-HREQ must be true at 5B pin 5, and the bus must have been taken by the active DMA board.

Bus Taken Latch

Once the 8088 has acknowledged a controller request by asserting HLDA the active DMA board issues a BUSY/ signal to indicate it has taken control of the bus. Connector J2's BUSY/ line is bi-directional in operation so either board may respond with a BUSY/ signal. (device 3F is open collector)

Bus Taken Latch 3B generates an 800ns BUSY signal from the Q output pin 5. Once 3B is set the Q/ output pin 6 (feedback enable line thru 4B) assures the Bus Taken Latch remains enabled. Latch 3B is set as a result of HLDA true (4C pin 5), LCL-HREQ true (4C pin 3), and the bus must not be busy (4C pin 4).

Busy Stretch Latch

BUSY at pin 5 of 3B is also routed to the latch at 2H known as the Busy Stretch Latch. This latch delays the BUSY signal by one CLK5 or 200ns. Open collector inverter 3F pins 2 and 12 inverts the BUSY signal from 3B pin 5 respectively and the wire-ored connection of 3F pins 2 and 12 results in a 1 us BUSY/ signal. This extra stretch assures a full DMA cycle.

Bus Release Logic

Gate 3A and 4B make up the Bus Release Logic. Only two situations will cause the DMA board to release the bus. Either END/ is true

(indicated by the completion of a DMA cycle) or by RELEASE/ (caused by a system reset or controller timeout). Either of these situations will clear the Bus Taken Latch thus releasing the bus.

2.1.3.8 Address Counter

Refer to sheet 5 of the DMA Board Schematic, Figure 2.5, for the following discussion.

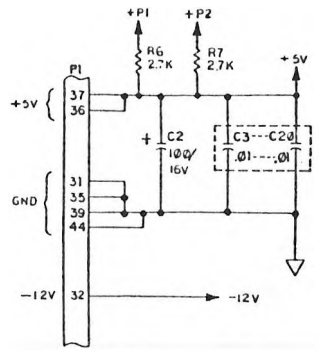
Located on sheet 5 is the 20 bit DMA Address Counter with tri-state outputs. The Low Byte Counter consists of 4H and 5J (address EF380), Middle Byte Counter 4E and 4D (address EF3A0), and High Nibble Counter 4F (address EF3Co). Beginning a DMA transfer these counters are loaded with the starting address in system memory where data from the hard disk will be stored. Each DMA cycle increments the counter by one.

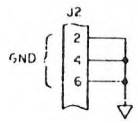
Address data is sent via the IDB0-7 Bus to the 20-bit counter. Signal DMA-ON enables the first half of the Low Byte Counter at 5J pin 7 and 10. Low Byte address is loaded into 4H and 5J by signal WS80/ (Write Select EF380) from the Write Select Decoder on sheet 2. Clocking for the Low Byte Counter as well as the Mid and High Counters is provided by signal WSTB/ (Write Strobe) at 4J pin 1. Signal END/, which is active at the end of the DMA cycle is used to increment the counters. The carry output of 5J pin 15 is used to enable the EP input of the other counters in the chain. Low Byte Counter carry out (pin 15 of 4H) enables the ET input of Mid Byte Counter 4D pin 10. (Input ET is fed forward "internally" to enable the carry output of each LS163 Counter)

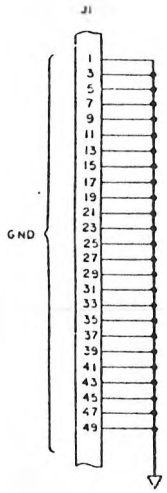
Readback of the address counter is accomplished by the LS244's at 5H, 5F, 5E and 5D. Low Byte IDB0-7 is read via the 244 at 5H when RS-80/ (Read Select EF380) or LO-AEN/ (Low Address Enable) are true. Mid Counter 4E and 4D are read back via 5E and 5D respectively requiring RS-A0/ (Read Select EF3A0) and AEN/ (Address Enable) true. High Counter 4F is read back via 5F requiring RS-C0/ (Read Select EF3C0) and AEN/ true. A8-19 is fed directly to the expansion bus.

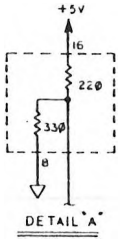
2.1.4 DMA BOARD SCHEMATIC AND ASSEMBLY DRAWING

Contained on the following pages is the schematic #104741 and assembly drawing #104740 of the DMA Board.







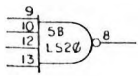


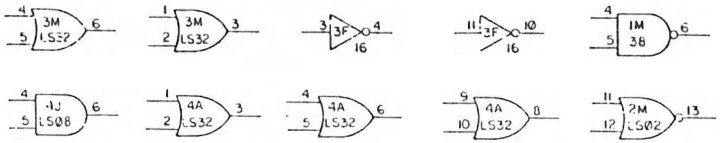
DETAIL 'A'

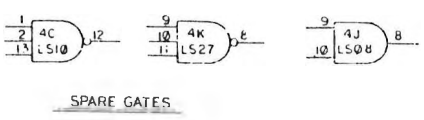
NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE ±5%, 1/4W
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE, GND = 7, +5V = 14

IC TYPE	GND	+ 5V
74LS133	8	16
74LS138	8	16
74LS139	8	16
74LS163	8	16
74S240	10	20
74LS240	10	20
74LS244	10	20
74LS245	10	20
74LS373	10	20
74LS374	10	20







SPARE GATES

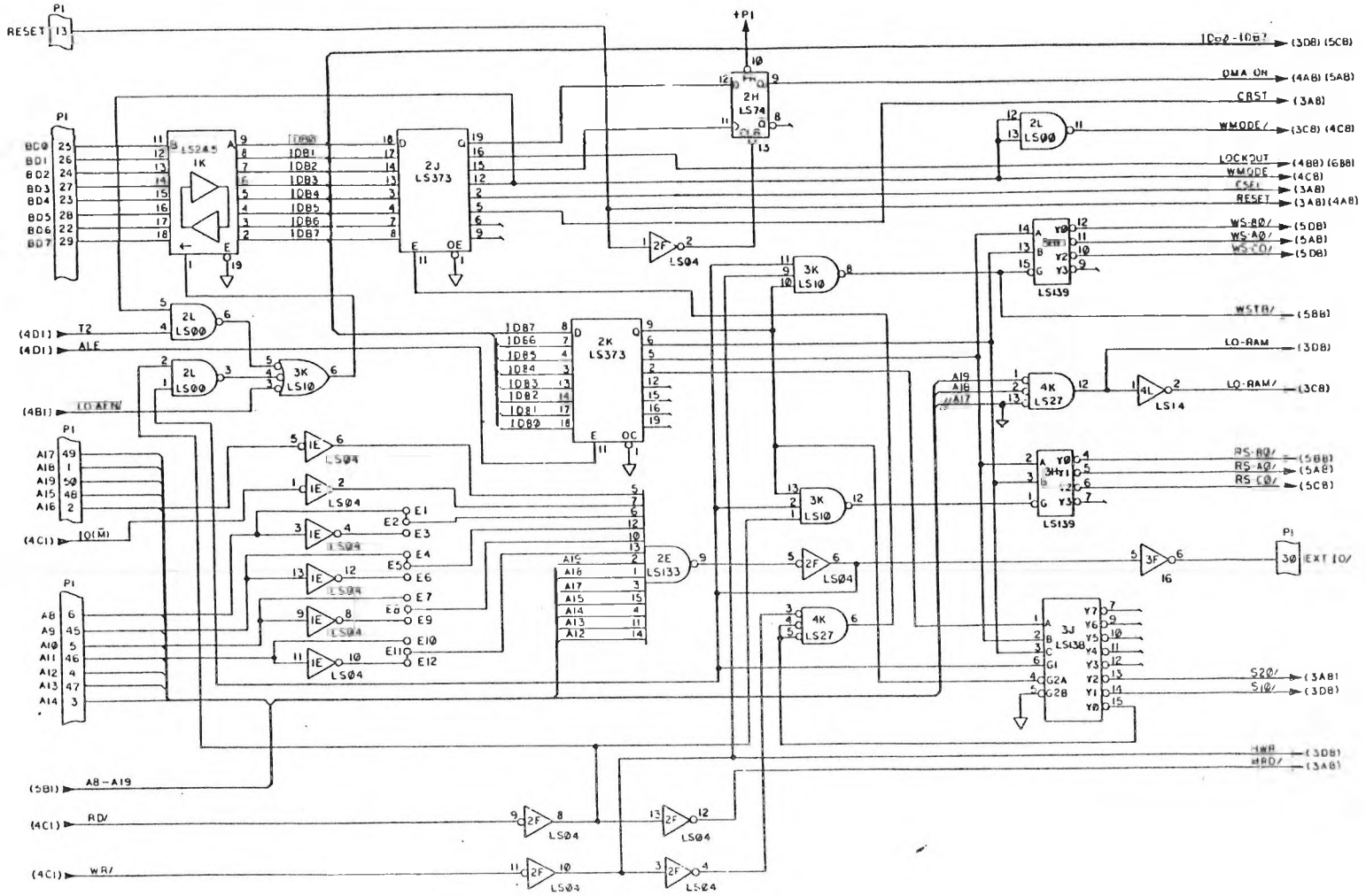
P1	
C2	
E15	
CR2	
R8	
C17	
LAST USED	NOT USED

REFERENCE DESIGNATION

VICTOR
Victor Technologies, Inc

D'SK
DMA INT'R'F'CE SCHEM.

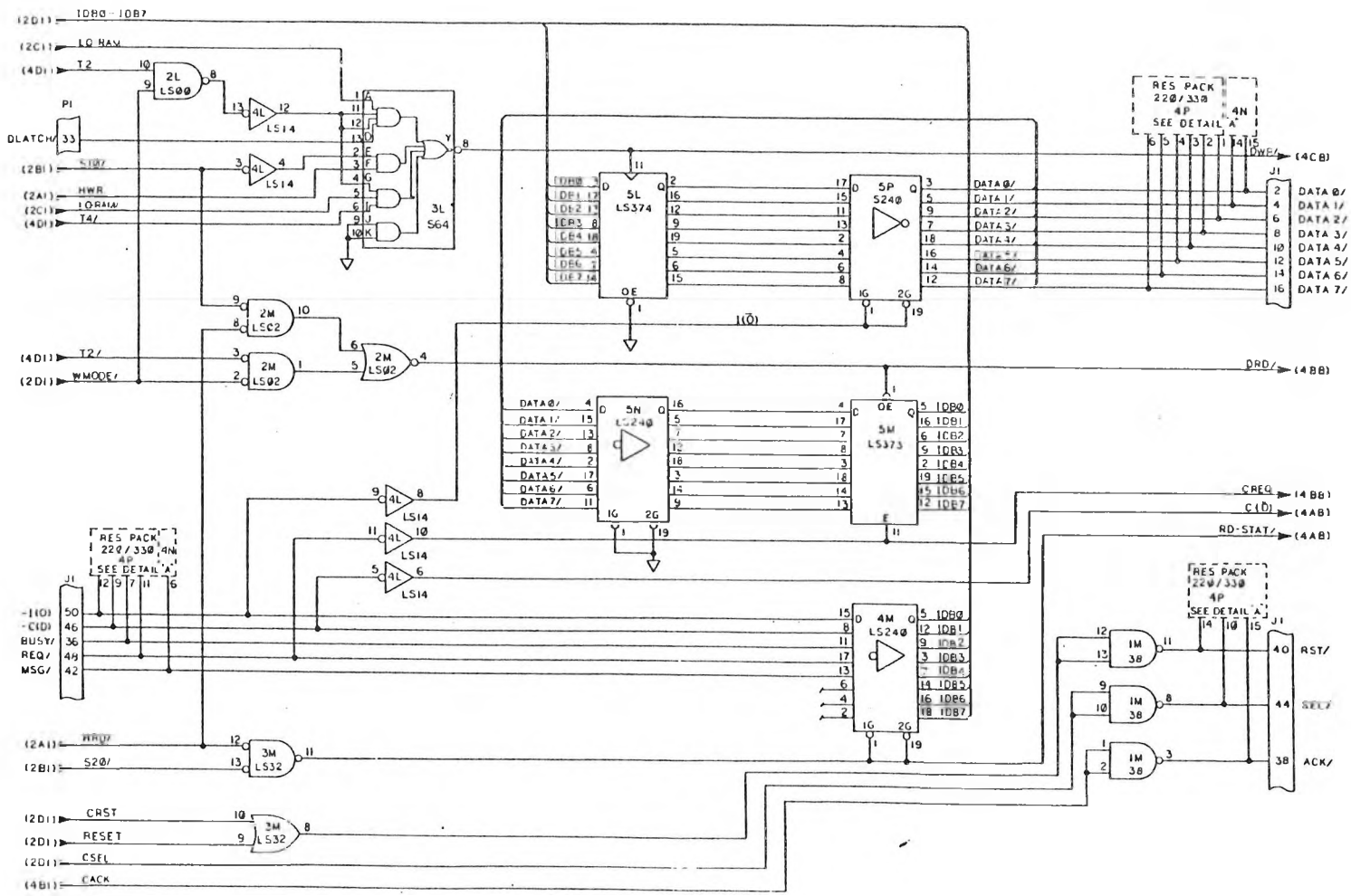
SHT 1 OF 6 | REV A
DWG NO 101161



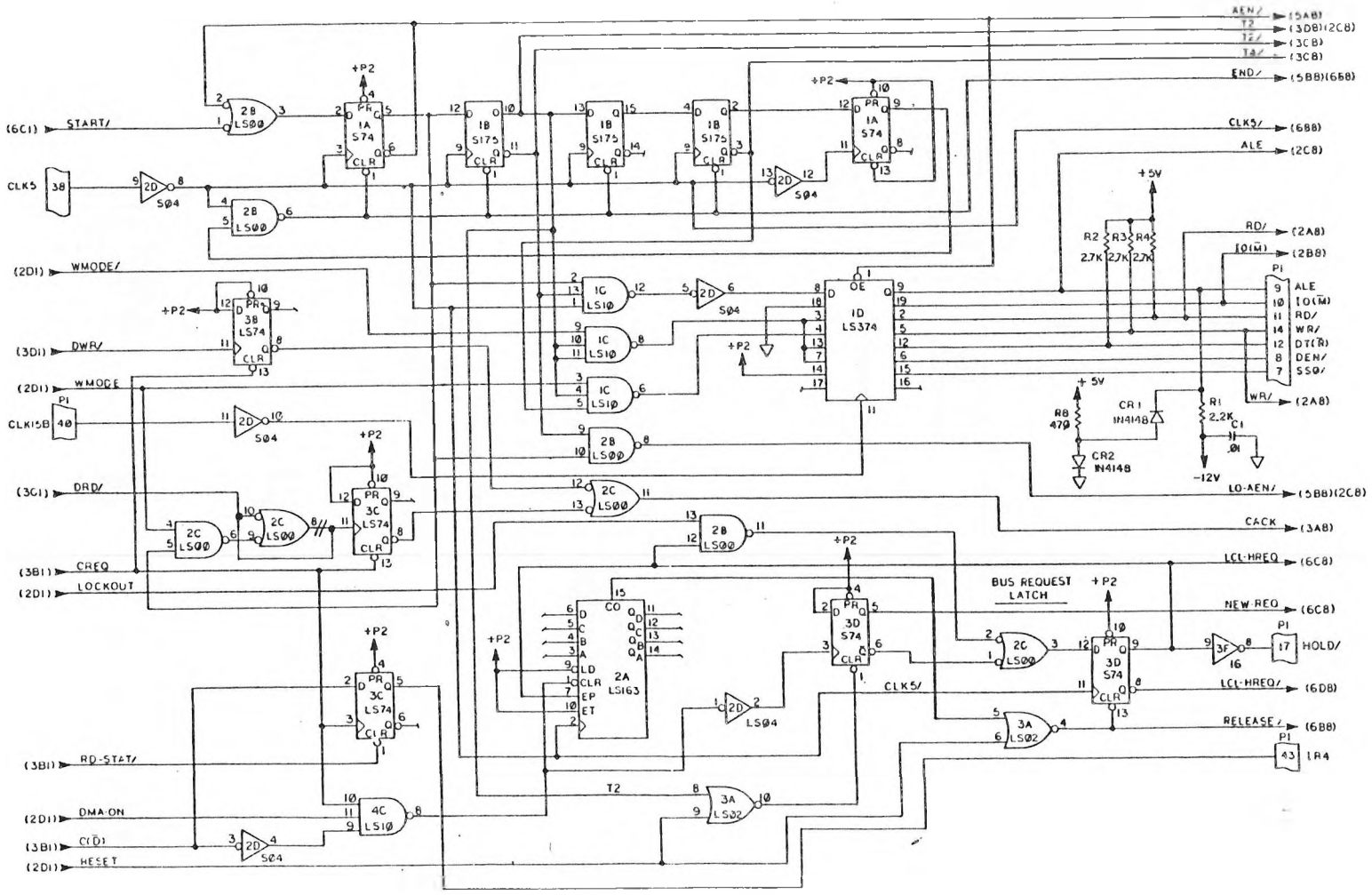
SHT 2 OF 6	REV A
DWG NO 101161	

VICTOR
Victor Technologies, Inc.

D'SK
DMA INT'R'F'CE SCHEM

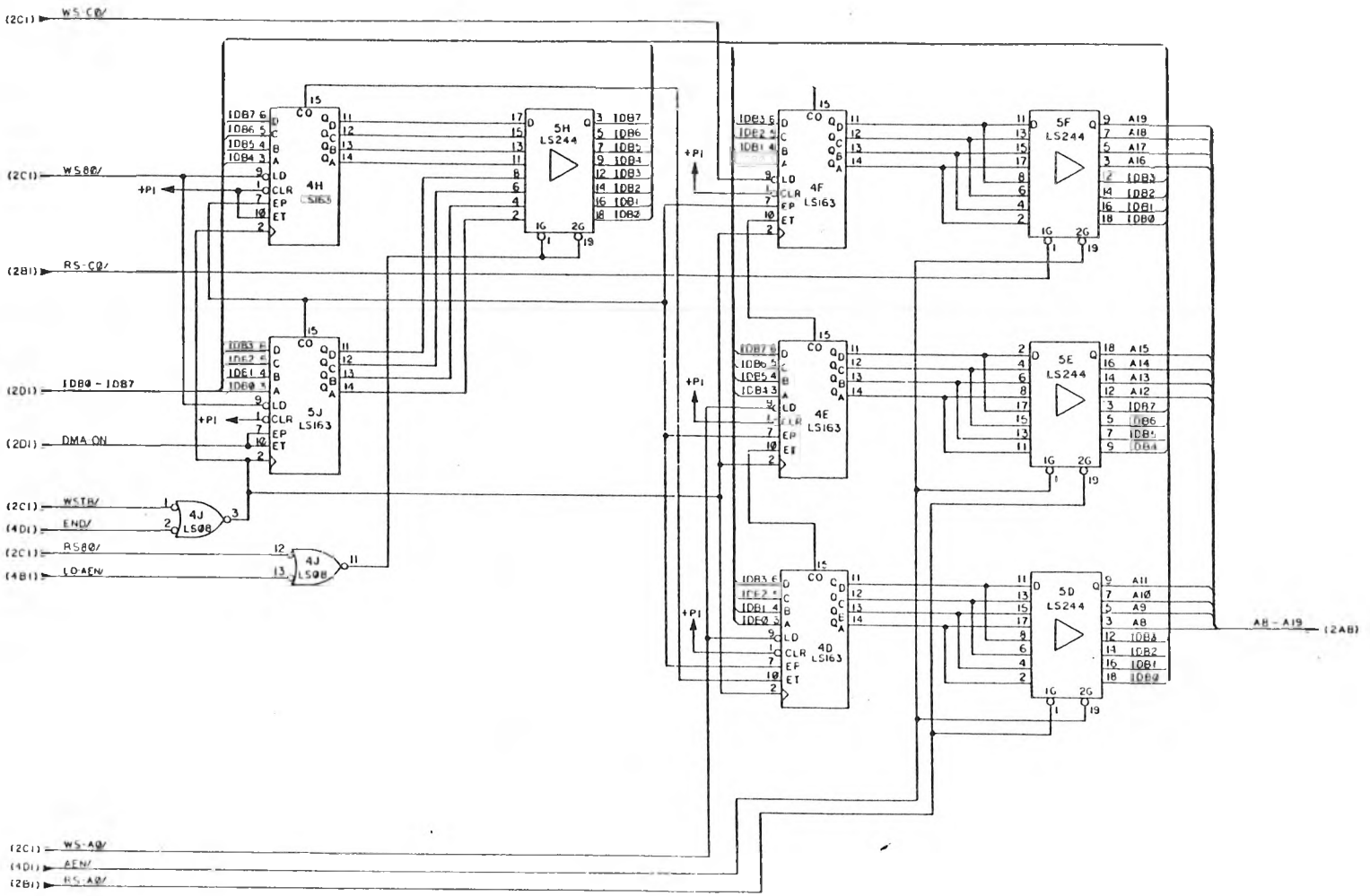


VICTOR	Victor Technologies, Inc
D'SK	DMA INT'R'F'CE SCHEM.
SHT 3 OF 6	REV A
DWG NO 101161	



D'SK
DMA INT'R'F'CE SCH'M

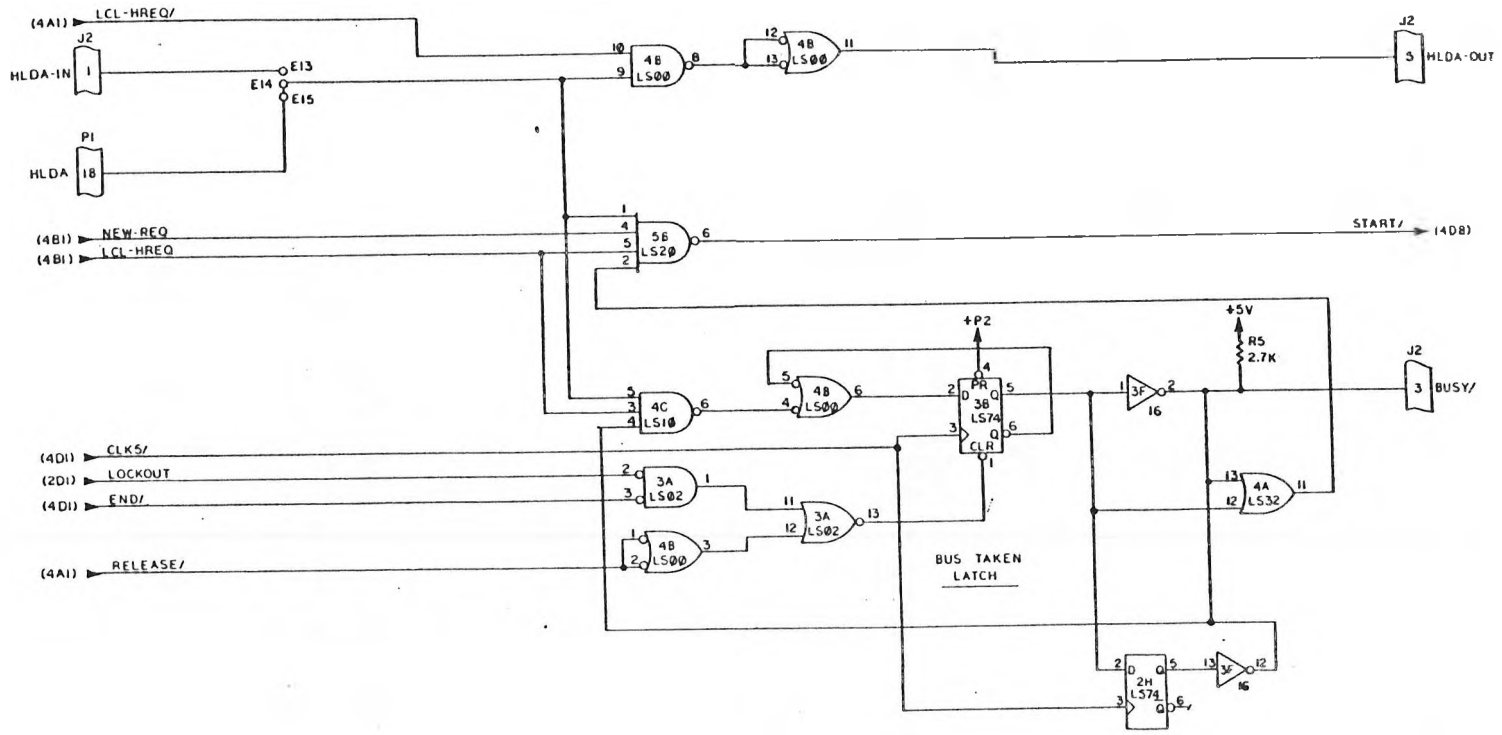
SHT 4 OF 6 REV A
DWG NO 101161



VICTOR
Victor Technologies Inc

D'SK
DMA INT'R'F'CE SCHEM.

SHT 5 OF 6 REV A
DWG NO 101161

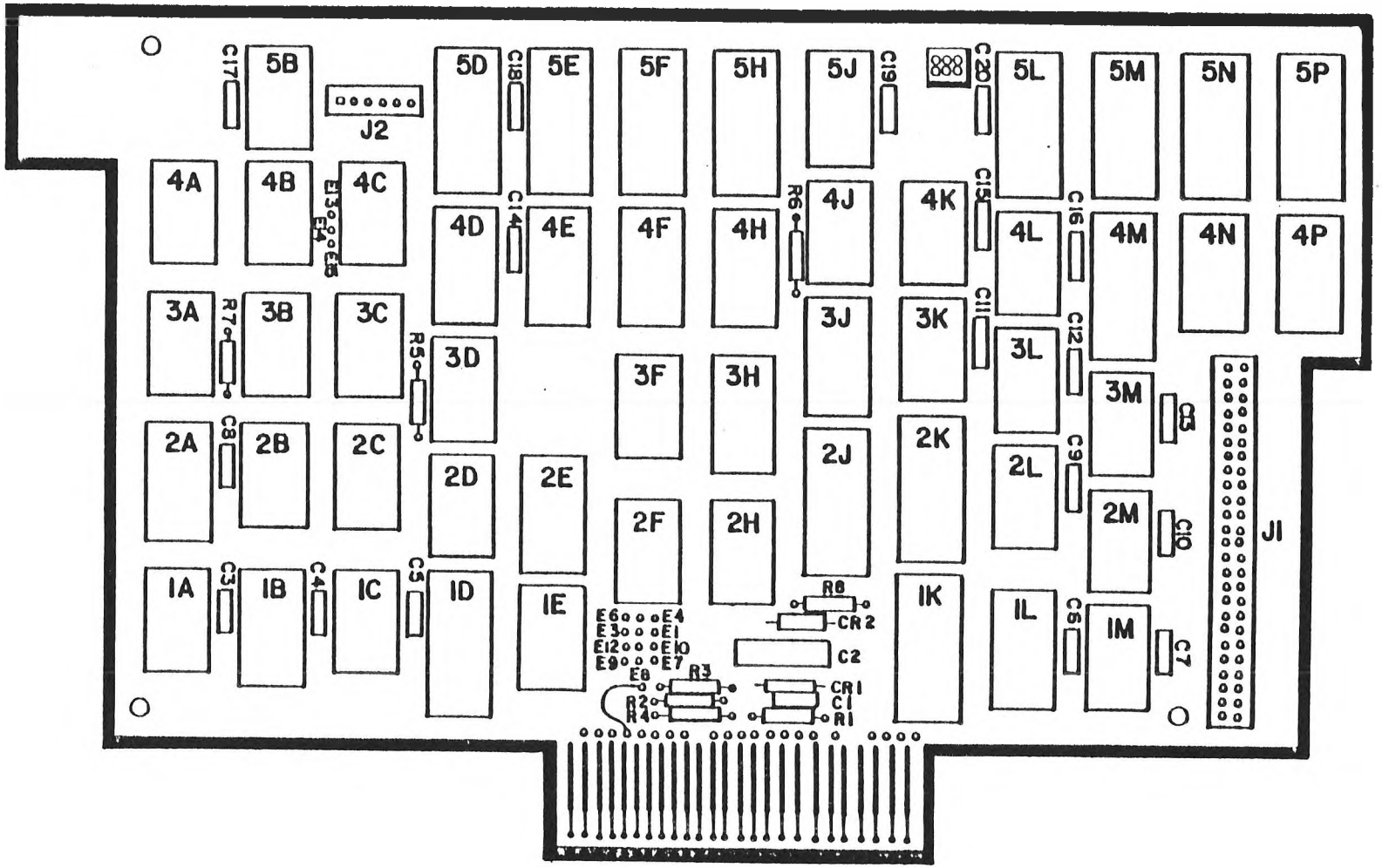


SHT 6 OF 6	REV A
DWG. NO 10116	

D'SK DMA INT'R'F'CE SCHE

VICT

Victor Technologi



DISK DMA INTERFACE

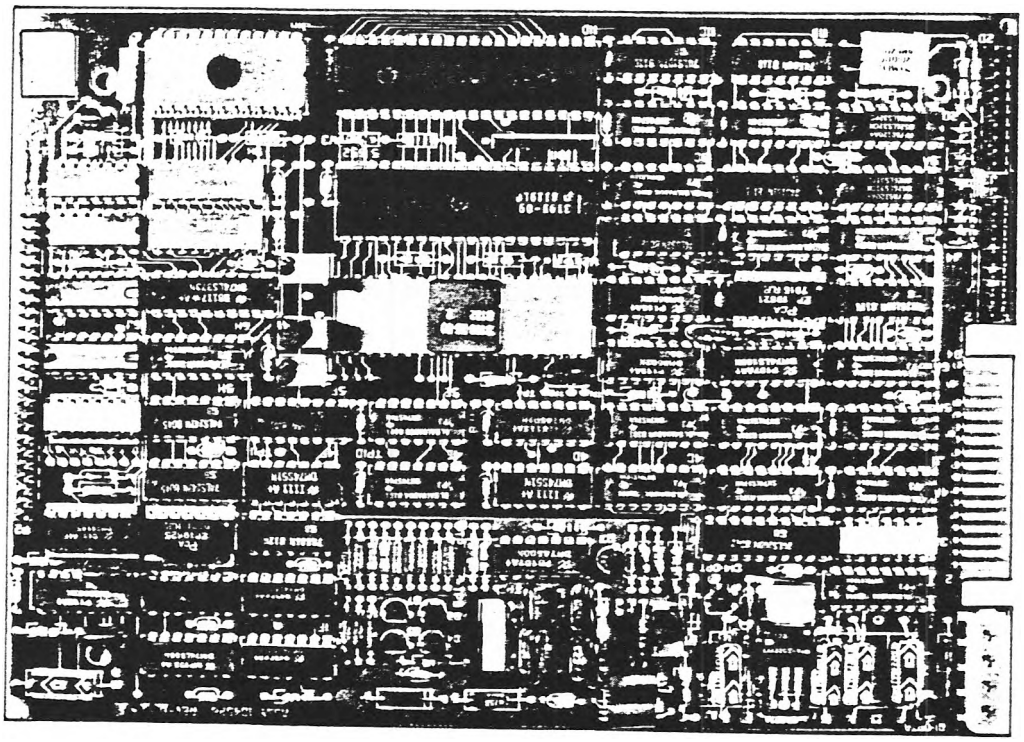
DMA Board Assembly Drawing #104740 (Sheet 1 of 1)
Figure 2.6

3. WINCHESTER DRIVE INTERFACE

3.1 XEBEC S1410 DISK CONTROLLER BOARD

The S1410 Contoller, shown in Figure 3.1, boasts the following operating and design features:

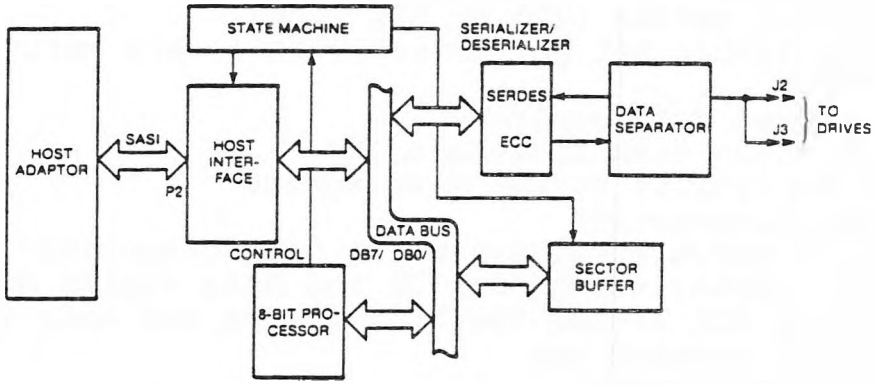
* Interlocked data transfer through the Shugart Asscociates System Interface (SASI)
* Microprocessor-based architecture
* Full-sector buffer (256 or 512 bytes)
* Hardware 32-bit ECC polynomial with 11-bit burst correction
* Field proven data separator
* Seagate ST506 disk interface
* Automatic retries during disk access
* Internal Diagnostics
* Automatic burst error detection and correction
* Separate sector format for ID and data fields with individual ECC fields for both the ID and data fields
* High level command set
* Variable interleave



XEBEC S1410 CONTROLLER BOARD
Figure 3.1

3.1.1 FUNCTIONAL ORGANIZATION

Major areas of the S1410 Controller are shown in the simplified block diagram of Figure 3.2.



S1410 CONTROLLER, FUNCTIONAL ORGANIZATION
Figure 3.2

3.1.1.1 Host Interface

The host interface connects the internal data bus of the S1410 Controller to the SASI Data Bus; the state machine controls the movement of data and commands through the S1410 host interface.

3.1.1.2 Processor

Considered a "smart" controller the S1410 utilizes an eight-bit processor to monitor and control its operation.

3.1.1.3 State Machine

The state machine contols and synchronizes the operation of the Host Adapter (DMA Board), SERDES, and sector buffer.

3.1.1.4 SERDES

The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected disk drive. It converts serial data from the selected disk drive to parallel data which it places on the internal data bus.

3.1.1.5 Data Separator

The data separator converts serial NRZ data to MFM for transfer to the selected disk drive. It converts MFM data coming from the selected disk drive to serial NRZ data for the SERDES.

3.1.1.6 Sector Buffer

The sector buffer stages data transfers between the disk drive and the host to prevent data overruns.

3.1.2 SPECIFICATIONS

This section contains the overall specifications of the S1410 Controller.

3.1.2.1 Electrical

Note: All measurements are made on the controller printed circuit board at the power connector P1.

Table 3.1
Electrical Specifications

Voltage	Range	Current
+5.0 Vdc	4.75 to 5.25 Vdc	2.5 Amp. Max 2.0 Amp. Typ.
+12.0 Vdc	10.8 to 13.2 Vdc	66.0 ma. Max. 48.0 ma. Typ.

Note: The maximum conducted power supply ripple must not exceed 0.10 volts rms, from 0.1 to 25MHz.

3.1.2.2 Enviromental

Table 3.2
Enviromental Specifications

Temperature	0 to 55 degrees Celsius
Relative Humidity	10 to 95 percent non-condensing
Altitude	Sea level to 10,000 feet

3.1.2.3 Connectors

Table 3.3
Controller Mating Connectors

Designation	Function	Type/Source
J1	Drive Control Signals	AMP 88373-3
J2,J3	Drive Data Signals	AMP 86904-1
J4	Test Connector	Not Applicable
P1	Power Supply (housing) (pins)	AMP 1-480424-0 AMP 350078-4
P2	Host interface signals	AMP 86916-1

Note: No connection to J4 must be made. This is for manufacturing test use only.

3.1.2.4 Connector Pin Assignments

The following tables contain the pin assignments of the connectors on the controller board. The tables identify the signals on the pins. Connector P2 signals are defined under section 3.1.2, Theory of Operation.

Table 3.4
Connector J1, Control Signals, Pin Assignments

Signal Pin	Ground Return	Signal Name
2	1	Reduced Write Current
4	3	Head Select 2(2)
6	5	Write Select Gate
8	7	Seek Complete
10	9	Track 00
12	11	Write Fault
14	13	Head Select 2(0)
16	15	Reserved
18	17	Head Select 2(1)
20	19	Index
22	21	Ready
24	23	Step
26	25	Drive Select 1
28	27	Drive Select 2
30	29	Reserved
32	31	Reserved
34	33	Direction In

Table 3.5
Connectors J2 and J3, Data Signals, Pin Assignments

Signal Pin	Ground Return	Signal Name
1	2	Drive Selected
5	6	Spare
7	8	Reserved
-	-	Spares
11	12	Ground
13		MFM Write Data +
14		MFM Write Data -
15	16	Ground
17		MFM Read Data +
18		MFM Read Data -
19	20	Ground

Table 3.6
Connector P2, Host Interface, Pin Assignments

Signal Pin	Ground Return	Signal Name
2	1	Data 0
4	3	Data 1
6	5	Data 2
8	7	Data 3
10	9	Data 4
12	11	Data 5
14	13	Data 6
16	15	Data 7
18	17	Spare
20	19	Spare
22	21	Spare
24	23	Spare
26	25	Spare
28	27	Spare
30	29	Spare
32	31	Spare
34	33	Spare
36	35	$\overline{\text{BUSY}}$
38	37	$\overline{\text{ACK}}$
40	39	$\overline{\text{RST}}$
42	41	$\overline{\text{MSG}}$
44	43	$\overline{\text{SEL}}$
46	45	$\overline{\text{C/D}}$
48	47	$\overline{\text{REQ}}$
50	49	$\overline{\text{I/O}}$

Table 3.7
Connector P1, Power Supply, Pin Assignments

Pin Number	Voltage
1	+12Vdc
2	Ground Return
3	Ground Return
4	+5Vdc

3.1.3 BOARD SETUP

This section contains information used for setting up and installing the board for operation. Except for changing the address of the controller the other information provided is for reference only.

3.1.3.1 Board Jumpers

Jumpers on the S1410 board are listed in Table 3.8, and are shown in Figure 3.3.

Table 3.8
Jumper Locations

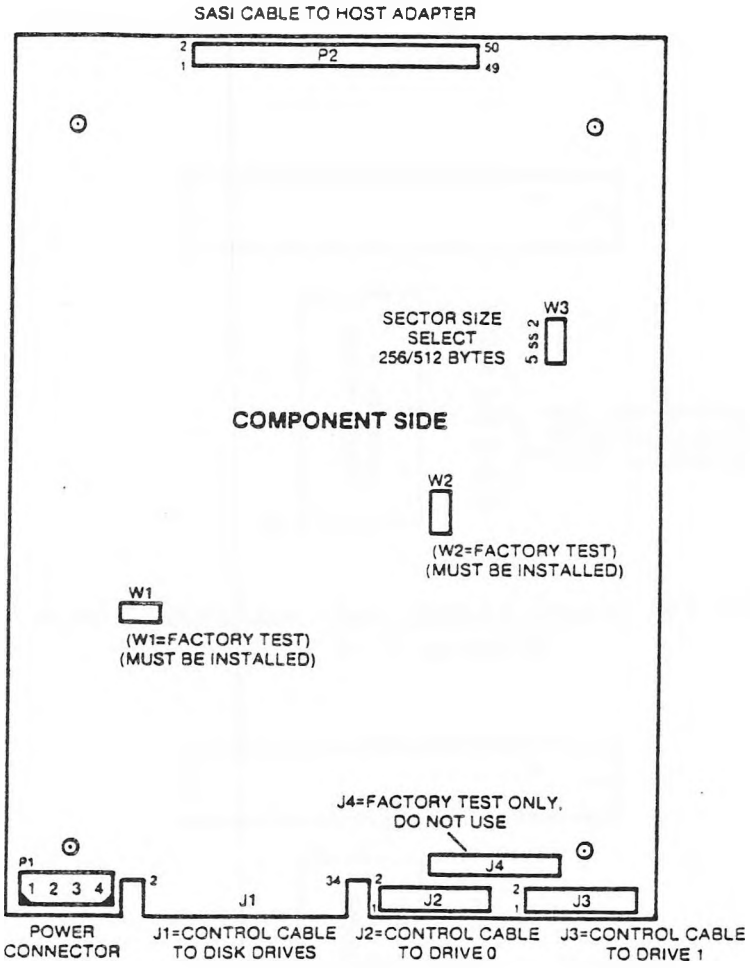
Designation	Function	Connection and Result
W1	Factory Test	Must be installed
W2	Factory Test	Must be installed
W3	Selects Sector Size	SS to 2: 256 byte sector 32 Sectors/Track SS to 5: 512 byte sector 17 Sectors/Track

Note: SS to 5 is the configuration used in the Victor System.

3.1.3.2 Connecting Cables

The following cables must be in place for proper operation of the controller. Included is the maximum length recommended for each cable. Figure 3.3 shows the connector locations.

J1 Control Cable: maximum 20 feet
J2 Data Cable: maximum 20 feet
J3 Data Cable: maximum 20 feet
P1 Power Cable: Not applicable
P2 Host Interface Cable: maximum 15 feet



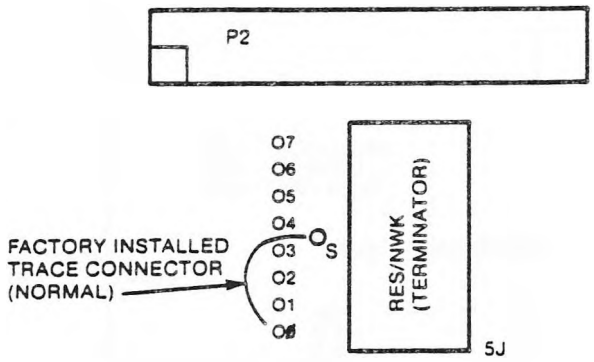
Cable, Connector, and Jumper Locations
Figure 3.3

Note: No connection should be made to J4. Factory test only.

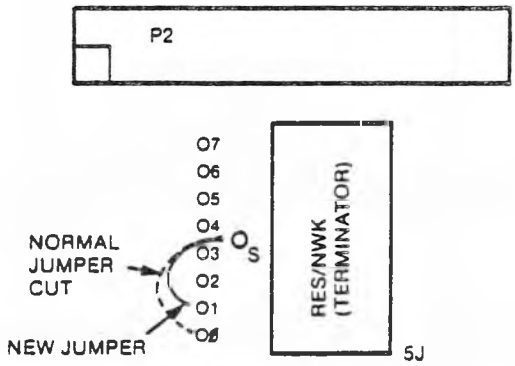
3.1.3.3 Address Jumper Group

The controller supports one of eight unique device addresses. When more than one controller is used in a system, the address jumper on the controller must be changed. Figure 3.4 shows the address jumper group located next to the terminator at position 5J; it also shows that terminal (pad 0) is connected to terminal S. This is the factory-installed jumper, and sets the controller to address 0.

In order to change this address, the factory-installed jumper (trace) must be cut. Then, a new jumper must be connected between terminal S and the selected address terminal. Figure 3.5 shows that the factory-installed jumper has been cut, and a new jumper has been installed between terminal S and address terminal 1. The address of the controller is now 1.



Normal (Factory-Installed) Address Jumper
Figure 3.4



Changed Address Jumper (Controller 1)
Figure 3.5

3.1.4 THEORY OF OPERATION

This section discusses the functional theory of operation of the S1410 Controller and how it is used in the Victor Hard Disk Subsystem.

3.1.4.1 Signal Definitions

The following tables list and define the signals that appear on the SASI Bus lines between the DMA Board and controller. The following designations are used in the tables.

Abbreviation	Definition
Drv	Driver
Rcvr	Receiver
OC	Open Collector
Tri-State	Line has three states: high, low, and high impedance
220/330	Line Termination: 220 Ohms to source voltage/ 330 Ohms to ground

Table 3.9
Host Bus Status Signals

NAME	DRVR/RCVR	DEFINITION
$\overline{I}$/O	Drv OC	$\overline{Input}$/Output: The controller drives this line. A low level on this line indicates that the controller is driving the data in (to the DMA Board) on the SASI Bus. A high level on this line indicates that the DMA Board is driving the data out on the SASI Data Bus. The DMA Board monitors this line and uses it to enable and disable its data bus drivers. This signal is qualified by signal $\overline{REQ}$.
$\overline{C}$/D	Drv OC	$\overline{Command}$/Data: This signal line indicates whether the information on the data bus consists of command or data bytes. A low means command bytes; a high means data bytes. This signal is qualified by signal $\overline{REQ}$.
$\overline{BUSY}$	Drv OC	$\overline{Busy}$: The controller generates this active low signal in response to the $\overline{SEL}$ signal and the address bit (DB0 to DB7) from the DMA Board. The busy signal informs the DMA Board that the controller is ready to conduct transactions on the SASI Bus.
$\overline{MSG}$	Drv OC	$\overline{Message}$: The controller sends this active low signal to the DMA Board to indicate that the current command has been completed. When $\overline{MSG}$ is active, the $\overline{I}$/O signal line is always low so that the controller can drive the bus data lines. This signal is qualified by $\overline{REQ}$.

Table 3.10
Summary of Host Bus Status Signals

$\overline{I/O}$	$\overline{C/D}$	$\overline{MSG}$	DEFINITION
High	Low	High	The Controller receives command from the DMA Board.
High	High	High	The Controller receives data from the DMA Board.
Low	High	High	The Controller sends data to the DMA Board.
Low	Low	High	The Controller sends error status byte to the DMA Board.
Low	Low	Low	The Controller informs the DMA Board that it has completed the current command.

Table 3.11
Controller - Host Handshaking

Name	Drv/Rcvr	Definition
$\overline{REQ}$	Drv OC	$\overline{REQUEST}$: The controller sends this active low signal to the DMA Board for each byte transferred across the interface. This signal qualifies signals $\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$.
$\overline{ACK}$	Rcvr 220/230	$\overline{ACKNOWLEDGE}$: The DMA Board generates this active low signal in response to the $\overline{REQ}$ signal from the controller when the host is ready to receive or transmit a byte of data. In order to complete the handshake, the DMA Board must sen an acknowledge ($\overline{ACK}$) in response to each request ($\overline{REQ}$) from the controller.

Table 3.12
Host Bus Control Signals

Name	Drv/Rcvr	Definition
$\overline{RST}$	Rcvr, 220/220	$\overline{RESET}$: The DMA Board sends this active low signal to the controller to force the controller to the idle state. After $\overline{RST}$ has become active, any controller status is cleared. $\overline{RST}$ also causes the deactivation of all signals to the drives. The time requirement for the $\overline{RST}$ signal is as

follows:

Minumum = 100 ns. Maximum = None

$\overline{SEL}$	Rcvr, 220/330	$\overline{SELECT}$: The DMA Board sends this active low signal to the controller to initiate a command transaction. Along with $\overline{SEL}$, the DMA Board must also send an address bit to select the controller (DB0 for controller). The controller must not be busy. The DMA Board must deactivate SEL before the end of the current command.

Table 3.13
Host Bus Data Signals

Name	Drv/Rcvr	Definition
DB7-DB0	Rcvr,	These are the eight data bits (lines) of the SASI Bus (DB0 = LSB). Each line is also used as address bits to select a controller in systems using multiple controllers. The normal connection (hardwired on the board) is to DB0, which is the address of controller 0. Any other connection requires cutting the existing trace on the board (or jumper) and adding a jumper. The following list shows the bit assignments: DB0 - Controller 0 DB1 - Controller 1 DB2 - Controller 2 DB3 - Controller 3 DB4 - Controller 4 DB5 - Controller 5 DB6 - Controller 6 DB7 - Controller 7

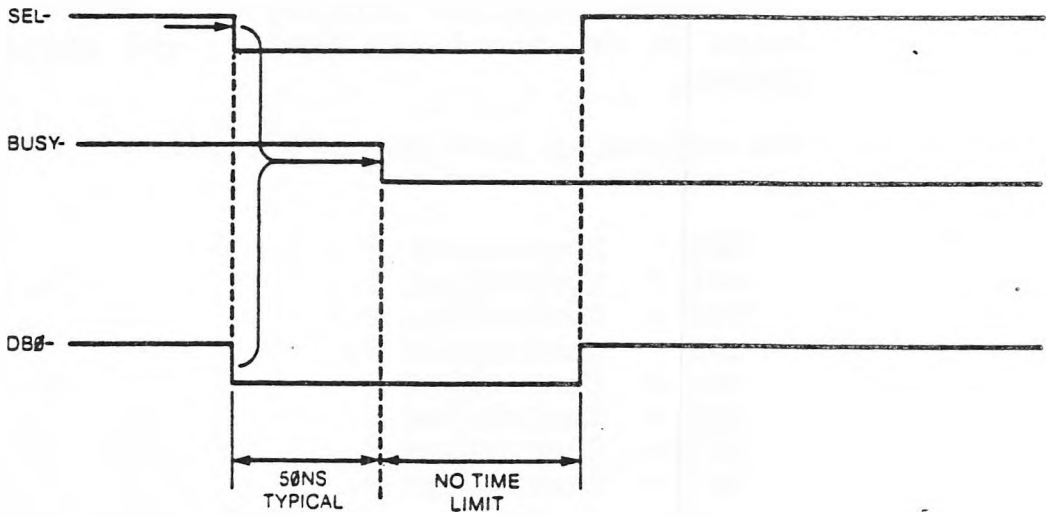
3.1.4.2 Detailed Description (Handshaking and Timing)

The following paragraphs describe the interaction between the controller and DMA Board.

Controller Selection

Before the DMA Board can begin a transaction, it must select the controller. The DMA Board selects the controller by activating the SEL control signal and the address bit of the controller. Any bit, DB0 - DB7, can be the address bit in a system with multiple controllers. For the following discussion, the controller's address is 0.

The timing diagram in Figure 3.6 shows the basic timing requirements. Upon receiving both the SEL signal and DB0, the controller activates the BUSY signal. As shown in the timing diagram, both SEL and DB0 must be active (low) before the controller can activate the BUSY signal. During the selection process, the host has control of the data bus as signified by the deactivation of the I/O line. Selection is complete when BUSY becomes active. The SEL signal must be deactivated by the host interface before the current controller operation has completed. The controller then enters command mode.

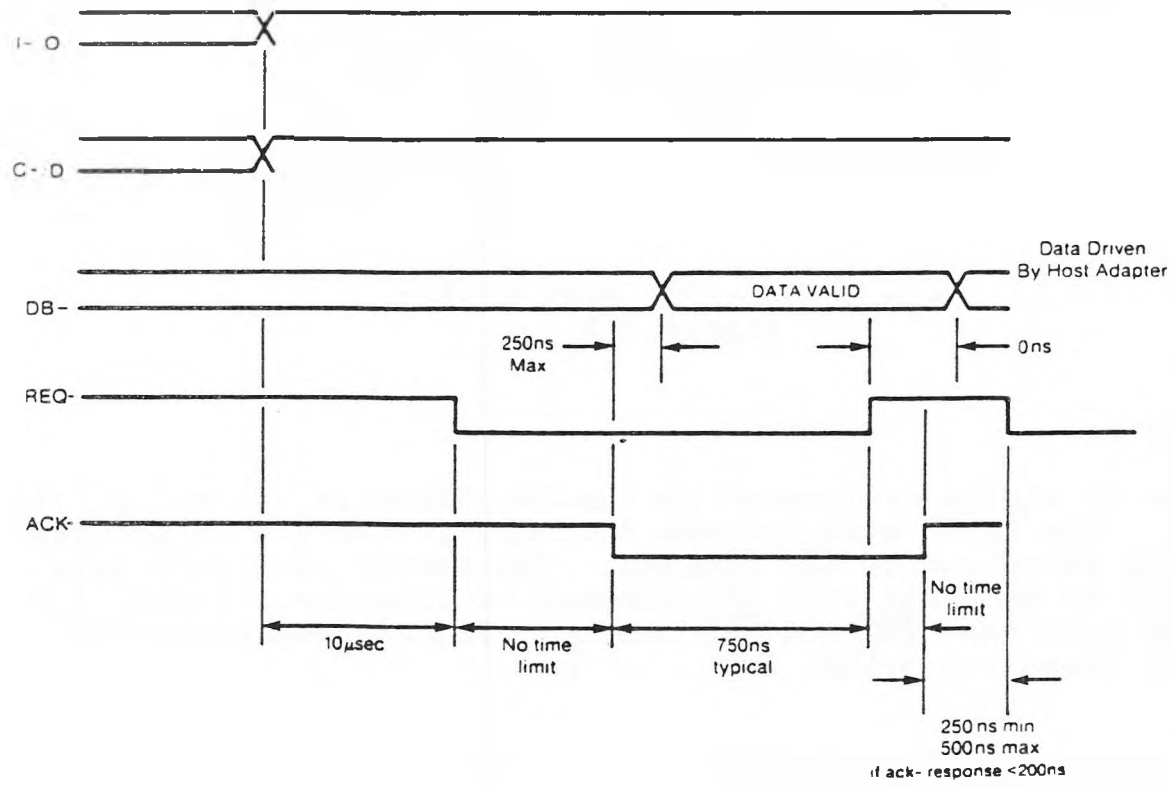


Controller Select Timing
Figure 3.6

Command Mode

The controller receives commands from the DMA Board using a handshaking sequence. The controller places a low level on the C/D (COMMAND/DATA) line to indicate that it wants a command from the DMA Board and places a high level on the I/O line to indicate that the movement of information is from the host adapter out to the controller. The MSG line is high.

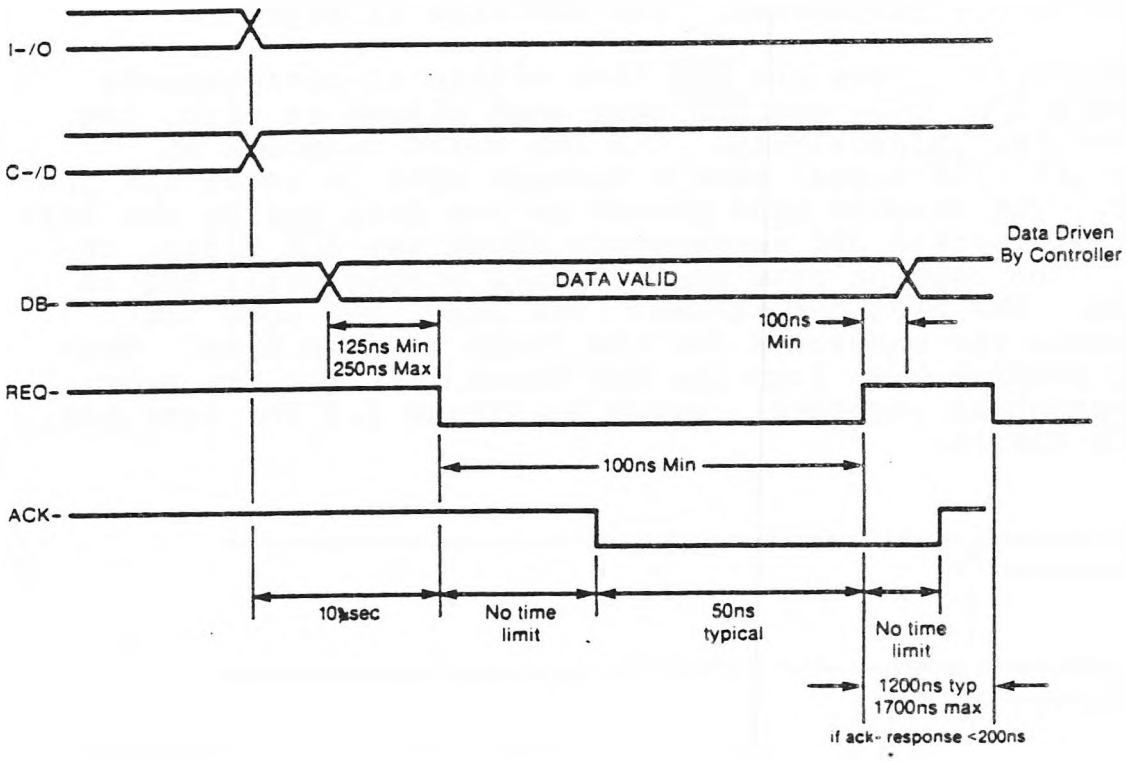
The controller activates the REQ line within 10 microseconds after signals I/O, C/D, and MSG have been placed at high, low, and high levels, respectively. The DMA Board responds by activating the ACK signal when a command byte is ready for the controller. The command byte placed on the data bus by the host must be stable within 250 nanoseconds after the ACK signal is activated. The command byte must be held stable until REQ is deactivated. The host deactivates ACK after REQ goes high. This completes the handshake for the first command byte. Each succeeding command byte from the DMA Board requires the same complete handshake sequence. Refer to Figure 3.7 for data bus, REQ and ACK timing.



Data Transfer From Host Timing
Figure 3.7

Data Transfer

The timing diagrams in Figures 3.7 and 3.8 illustrate the required timing for data transfer.



Data Transfer To Host Timing
Figure 3.8

Status Bytes

Two bytes of status are passed to the DMA Board at the end of all commands. The first byte informs the host if any errors occurred during the execution of the command. The second is a zero byte. It signals to the host that the command is complete. Figure 3.8 shows the data bus, REQ and ACK timing. Figure 3.10 shows the format of these two bytes.

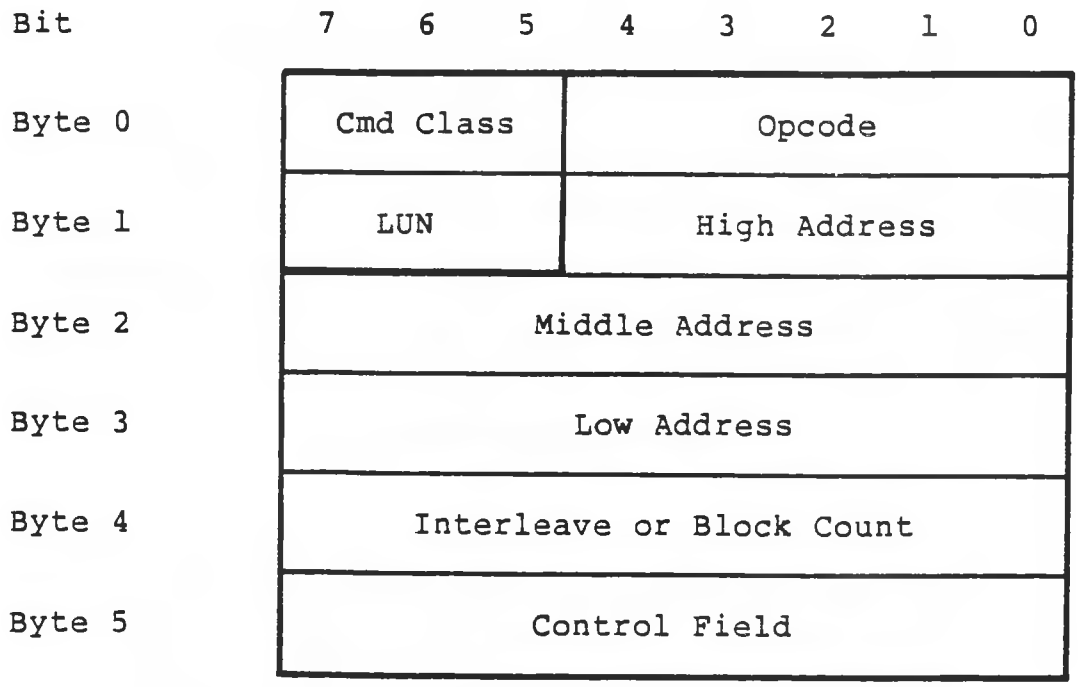
3.1.5 PROGRAMMING INFORMATION

The following section discusses communications between the controller and host from the point of view of the codes that are passed. The host sends commands to the controller via the DMA Board. The controller then performs the commands and reports back to the host. For more information on this section the

reader may wish to obtain a copy of the Xebec S1410 Owner's Manual and Programming Guide by calling (408) 733-4200. Only certain significant commands will be discussed in this section.

3.1.5.1 Commands

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Figure 3.9 shows the composition of the DCB. The list that follows Figure 3.9 defines the bytes that make up the DCB.



Device Control Block (DCB) Format
Figure 3.9

Byte 0 Bits 7, 6, and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command.

Byte 1 Bits 7, 6, and 5 identify the logical unit number (LUN). Bits 4 through 0 contain logical disk address 2.

Byte 2 Bits 7 through 0 contain logical disk address 1.

Byte 3 Bits 7 through 0 contain logical disk address 0 (LSB).

Byte 4 Bits 7 through 0 specify the interleave or block count.

Byte 5 Bits 7 through 0 contain the control field.

At the end of a command, the controller returns two completion status bytes to the host. The format of these bytes is shown in Figure 3.10.

NEXT TO LAST STATUS BYTE

Bit	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	ERR	0

Bits 0,2,3,4,6,and 7: Set to zero

Bit 1: When set, error occurred during command execution.

Bit 5: Logical unit number of drive, d=0 or 1.

LAST STATUS BYTE

Bit	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	ERR	0

Bits 0-7: Set to zero.

Completion Status Bytes
Figure 3.10

3.1.5.2 Control Byte

The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The following list defines the bits of the control byte.

Bit 0 Half-step option of Seagate and Texas Instrument drives.

Bit 1 Half-step option for Tandon Drives.

Bit 2 Buffer-step option for drives made by Computer

Memories, Inc. and Rotating Memories, Inc. (200 microsecond pulse per step).

Bit 3-5 Spare. Set to zero for future use.

Bit 6 If one, during a read sector command, the failing sector is not re-read on the next revolution before attempting correction. This bit should be set to zero for normal operation.

Bit 7 Disable the four retries by the controller on all disk access commands. Set this bit only during the evaluation of the performance of a disk drive.

This bit should be set to zero for normal operation.

Note: The step option bits (2-0) are mutually exclusive and only one option should be selected in any given configuration.

3.1.5.3 Logical Address (High, Middle, and Low)

The logical address of the drive is computed by using the following equation.

Logical Address = (CYADR * HDCYL + HDADR) * SETRK + SEADR

Where : CYADR = Cylinder Address
HDADR = Head Address
SEADR = Sector Address
HDCYL = Number of Heads per Cylinder
SETRK = Number of Sectors per Track

The commands fall into eight classes, 0 through 7; only classes 0 and 7 are used. Class 0 commands are data, non-data transfer, and status commands. Classes 1 through 6 are reserved. Class 7 are diagnostic commands.

Following is a description of two important Class 0 commands; Request Sense Status and Initialize Drive Characteristics. The description includes its class, opcode, and format. When a slash (/) represents a bit position, the slash indicates a don't care.

3.1.5.4 Request Sense Status (Class 0, Opcode 03)

The host must send this command immediately after it detects an error. The command causes the controller to return four bytes of drive and controller status; the formats of these bytes are shown after the DCB. When an error occurs on a multiple sector data transfer, (read or write), the Request Sense Status command

returns the logical address of the failing sector in bytes 1, 2, and 3. If the Request Sense Status command is issued after any of the Format commands or the Check Track Format command, then the logical address returned by the controller points to one sector beyond the last track formatted or checked if there was no error. If there was an error, then the logical address returned points to the track in error. The tables which follow the formats list the error codes as reported internal to the S1410 Controller.

d = drive, 0 or 1

Note: This parameter (d) would be used for indicating which drive receives the command when two drives are chained off one controller.

REQUEST SENSE STATUS FORMAT

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

SENSE BYTE 0

Bit	7	6	5	4	3	2	1	0
Byte 0	See Below							

Bits 0,1,2,3: Error Code (Hex 3 in example above)

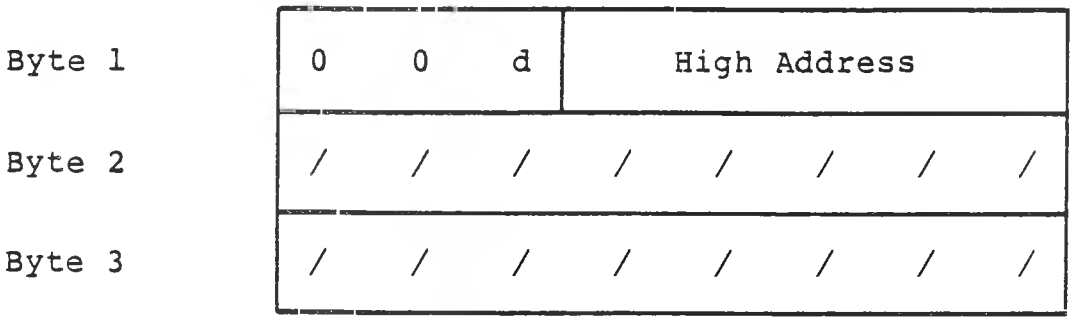
Bits 4,5: Error Type (Hex 0 in example above)

Bit 6: Spare, set to zero

Bit 7: Address valid, when set

Bit 7, the address valid bit in the error code byte (byte 0), is relevant only when the previous command required a logical block address; in which case it is always returned as a one otherwise it is set to zero.

SENSE BYTES 1,2, and 3



The following table (3.14) contains the error codes as reported by the controller when a Request Sense Status command is issued by the host. The table is divided into four areas; Type 0 (Disk Drive), Type 1 (Controller), and, Type 2 and 3 (Command and Miscellaneous). The Summary Error Table shows the hex code with bit 7 (address valid) set and not set.

Note: Present Winchester CPU Boot Roms report system boot errors from the controller with bit 7 set.

Example: X98, X92, X91, etc.

Future Universal CPU Boot Roms will report system boot errors from the controller with bit 7 not set.

Example: X18, X12, X11, etc.

Table 3.14
S1410 Error Code Summary

Error Code (Hex)

Bit 7 Set	Bit 7 Not Set	Meaning
		Type 0 (Disk Drive)
80	00	No error detected: The controller detected no error during the execution of the previous command.
81	01	No index detected from disk drive
82	02	No seek complete from disk drive
83	03	The controller detected a write fault from the disk drive during the last operation.
84	04	After the controller selected the drive, the drive did not respond with a ready signal.
85	05	Not Used.
86	06	After stepping maximum number of cylinders, the controller did not receive track 00 signal from the drive.
87-8F	07-0F	Not Used.
		Type 1 (Controller)
90	10	ID Read Error: The controller detected an ECC error in the target ID Field on the disk.
91	11	Data Error: The controller detected an uncorrectable ECC error in the target sector during a read operation.
92	12	Address Mark: The controller did not detect the target address mark (AM) on the disk.
93	13	Not Used.
94	14	Sector Not Found: The controller found the correct cylinder and head, but not the target sector.
95	15	Seek Error: The controller detected an incorect cylinder or track or both.

(continued from page 3-20)

Error Code (Hex)

Bit 7 Set	Bit 7 Not Set	Meaning
		Type 1 (Disk Drive)
96-97	16-17	Not Used.
98	18	Correctable Data Error: The controller detected a correctable ECC error in the target data field. This is a normal indication of a drive that has been formatted but not configured to contain any data.
99	19	Bad Track: The controller detected the bad track flag during the last operation.
9A	1A	Format Error: During a check-track command, the controller detected one of the following: 1. Track not formatted 2. Wrong interleave 3. ID ECC error on at least one sector
9B-9F	1B-1F	Not Used.
		Type 2 (Command and Miscellaneous)
A0	20	Invalid Command: The controller has received an invalid command from the host.
A1	21	Illegal Disk Address: The controller detected an address that is beyond the maximum range.
A2-AF	22-2F	Not Used.
		Type 3 (Command and Miscellaneous)
B0	30	RAM Error: The controller detected a data error during the RAM sector buffer diagnostic.
B1	31	Program Memory Checksum Error: During its internal diagnostic, the controller detected a program-memory checksum error.
B2	32	ECC polynominal Error: During the controller's internal diagnostic, the hardware ECC generator failed its test.
B3-BF	33-3F	Not Used.

3.1.5.5 Initialize Drive Characteristics (Class 0, Opcode 0C)

This command enables the user to configure the controller to work with drives that have different capacities and characteristics. However, both drive 0 and drive 1 must be of the same manufacturer and model number if two drives are chained off one controller.

After the host sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters. Some of the parameters occupy two bytes; all two-byte parameters are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

C = Maximum number of cylinders (2 bytes)
H = Maximum number of heads (1 byte)
W = Starting reduced write current cylinder (2 bytes)
P = Starting write precompensation cylinder (2 bytes)
E = Maximum ECC data burst length (1 byte)

The parameter for the maximum ECC burst length defines the length of a burst error in the data field that the controller will correct. The burst length is defined as the number of bits from the first error bit to the last error bit. For example, the controller detected a 5-bit ECC error and the erroneous data appeared as C5 (1100 0101) before correction and could appear as D4 (1101 0100) after the correction. However, if the host has set the maximum ECC burst length at 4 bits, the controller would have to flag this data as uncorrectable. This is a type 1, code 1 error.

3.1.6 SECTOR FORMAT

Figure 3.11 shows the format of the sector and the names of the fields of the information traveling over the controller-drive interface. Table 3.15 lists the fields and a description of each field.

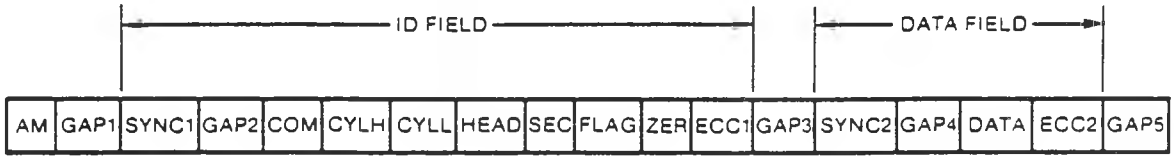
Table 3.15
Sector Field Description

Field	Bytes	Field Description
AM	4	Address Mark
GAP1	9	Zero Byte Gap
SYNC1	1	ID Sync Byte
GAP2	2	ID Zero Byte Gap
COM	1	ID Compare Byte
CYLH	1	Cylinder High (MSB)
HEAD	1	Cylinder Low (LSB)
SEC	1	Head Number

Table 3.15 (Continued)

FLAG	1	Flag Byte
ZER	1	Zero Byte
ECC1	4	ID ECC Bytes
GAP3	16	Zero Byte Gap
SYNC2	1	Data Field Sync Gap
GAP4	2	Data Field Zero Byte Gap
DATA	256/512	Data Field
ECC2	4	Data Field Ecc Bytes
GAP5	14/43	Inter-record Zero Gap

* * * * * * * * *



Sector Format
Figure 3.11

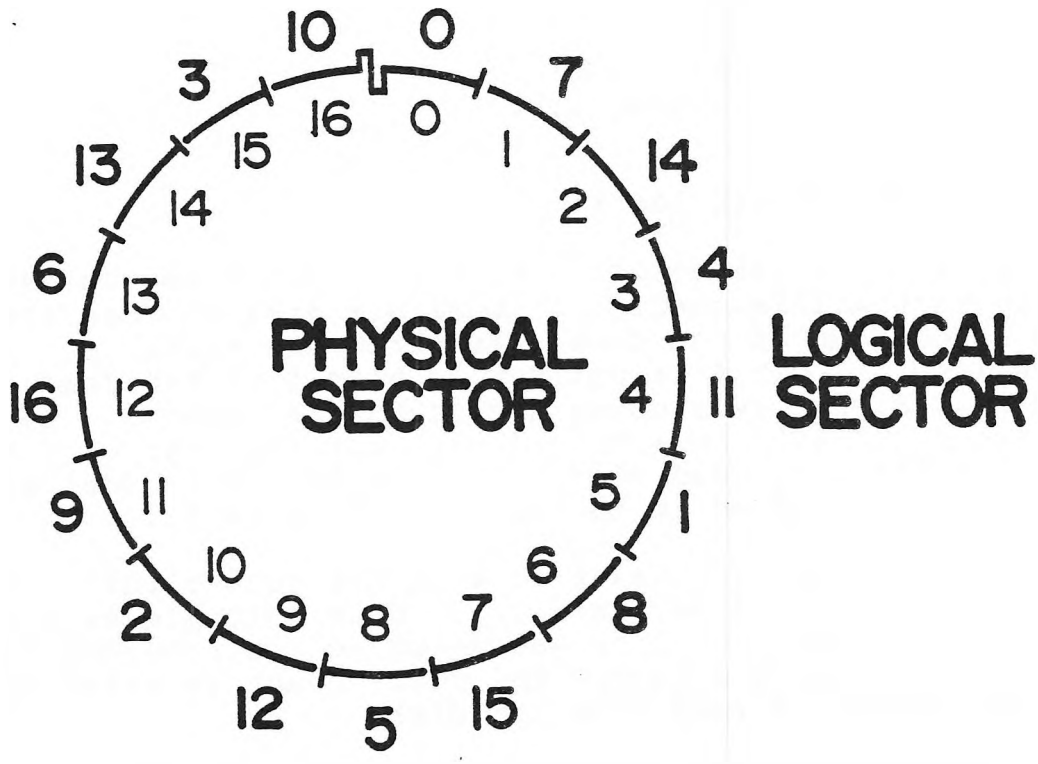
3.1.7 ERROR CORRECTION PHILOSOPHY

Since the typical error correction time of the S1410 controller is approximately 50 milliseconds and therefore greater than the time for one revolution of the disk, the sector in error is optionally re-read (if bit 6 is not set in byte 5 of the read command DCB) on the next revolution during a read command. In most cases, the error will be soft and will not reappear on the re-read. This initial re-read of the failing sector is over and above the retry count passed in the DCB (bit 7, byte 5).

The retry count on errors is preset to 4 by the controller each time a sector has been read successfully. On a multiple sector transfer if an uncorrectable error was detected but subsequently found to be correctable on a retry, the retry count is reset to 4 before the next sector is read from the disk.

3.1.8 SECTOR INTERLEAVING

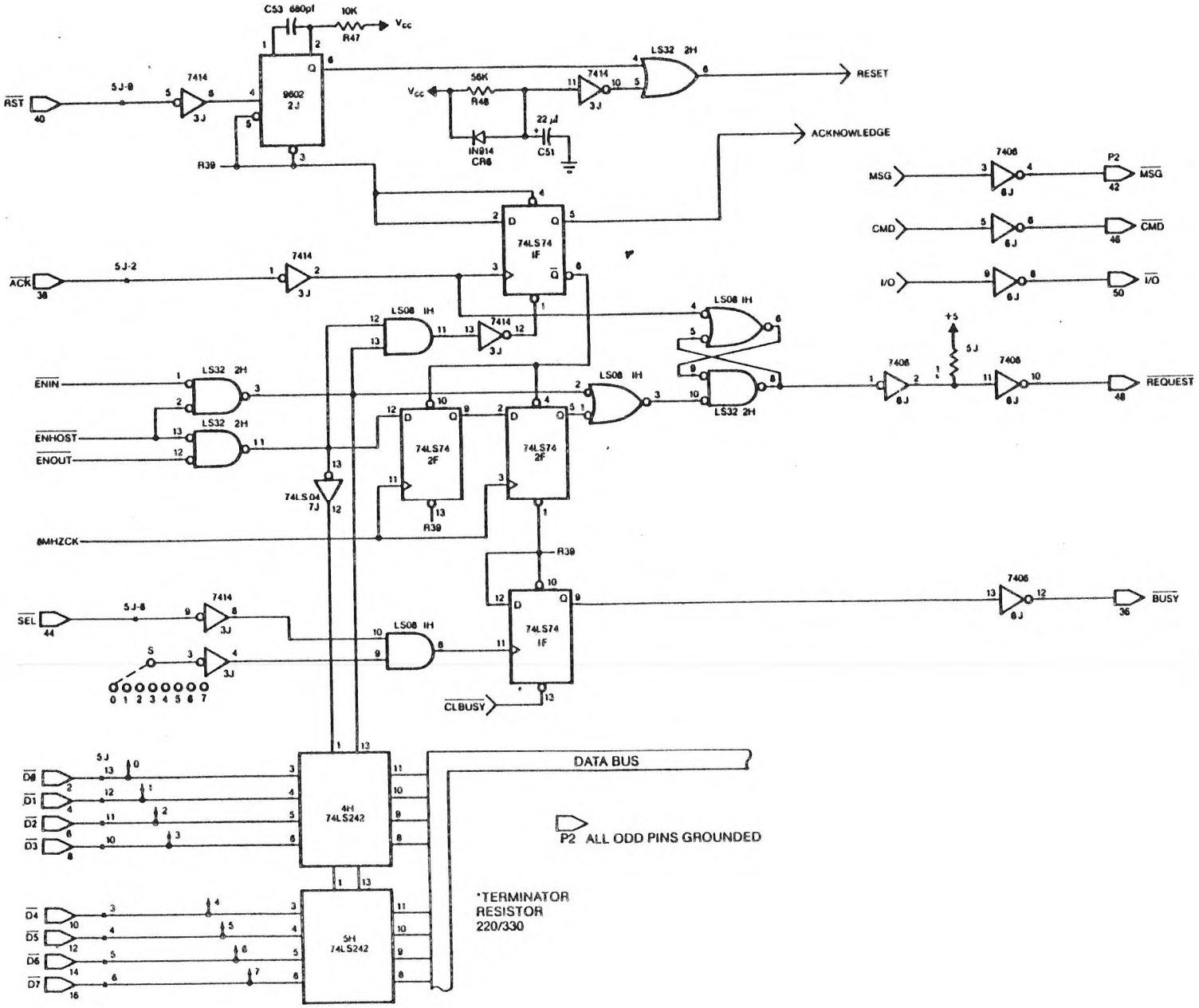
Variable sector interleaving is supported by the S1410 disk controller. When any format command is issued, any interleave value up to the number of sectors-per-track minus one may be passed in the Device Control Block (DCB byte 4). The interleave factor may be adjusted for maximum system performance. Interleaving allows logical contiguous sectors of data on a given track to be mapped onto non-adjacent physical sectors. An interleave factor of five, for instance means that every fifth physical sector is transferred as the next contigous logical sector of data. It does not mean that five sectors of data are transferred in one revolution. Lets say for example sector one contains the data to be read and transferred to the host (using an interleave of five). Sector one is first read into the sector buffer and then during the time the heads are passing over the next four physical sectors of the disk the data is being transferred to the host. If the host cannot transfer the full sector of data during the four sector times available, then the controller has to wait a full revolution before the next logical sector can be read from the disk. If this happens, the interleave factor is too low and should be increased until an increase in operating system speed is noticed.



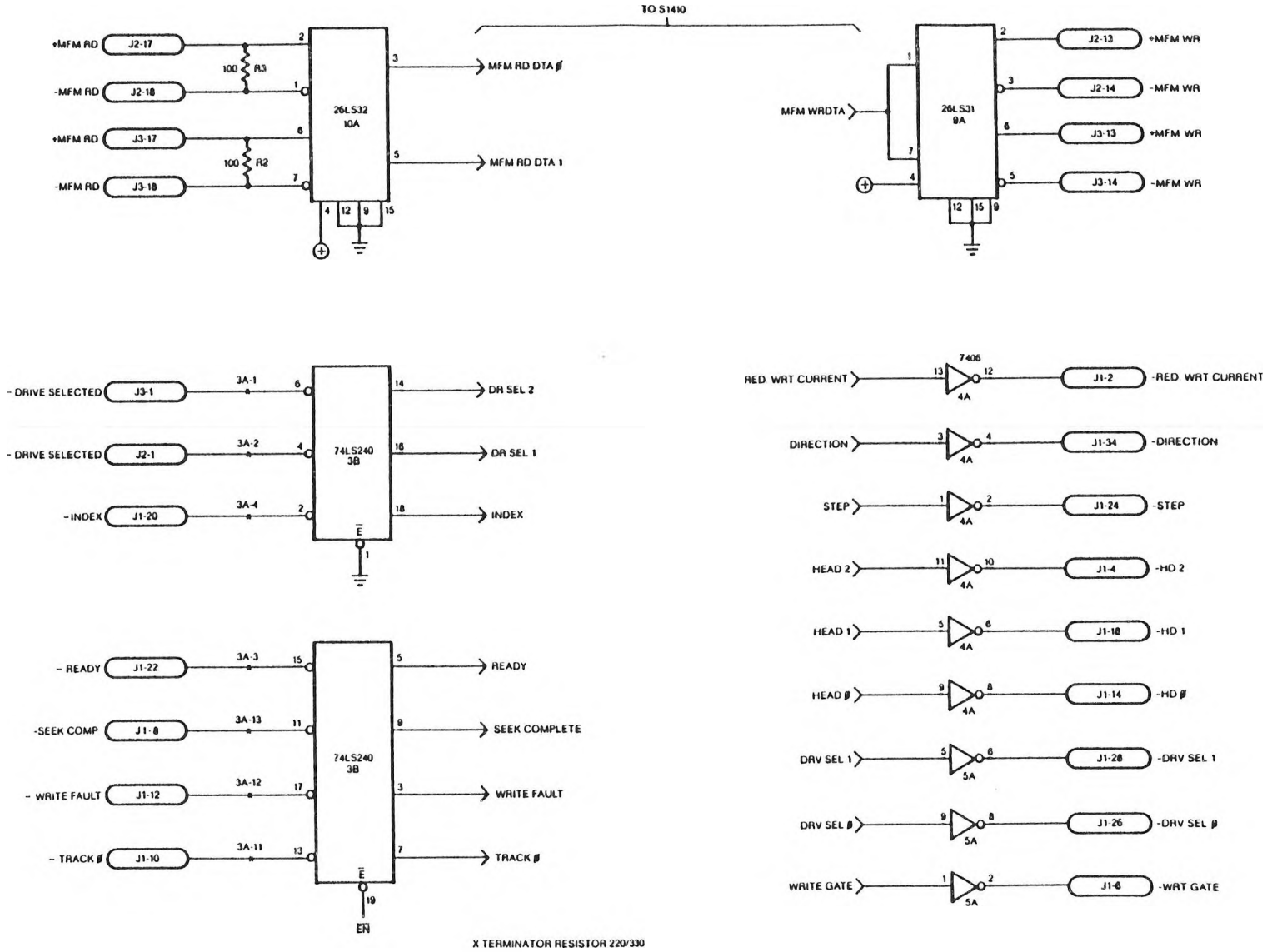
Disk Format Example of 17 Sectors per Track
With an Interleave Factor of 5
Figure 3.12

3.1.9 S1410 HOST AND DRIVE INTERFACE SCHEMATICS

Figure 3.13, page 3-26, contains the Host Interface schematic of the S1410 Controller. Figure 3.14, page 3-27, contains the Drive interface schematic. Internal schematics of the S1410 Controller are not available at this time.



Host Interface Schematic
Figure 3.13



Drive Interface Schematic
Figure 3.14

4. MODULE REPLACEMENT GUIDE

The following section deals only with replacement of major modules of the Hard Disk Subsystem i.e., the Winchester Drive itself, Xebec S1410 Controller Board, and the DMA Interface Board.

4.1 WINCHESTER DRIVE REPLACEMENT

When it becomes necessary to remove and replace the Winchester Disk Drive extreme care must be taken in handling. Refer to Section 1.3, Winchester Drive Handling Precautions, before proceeding.

4.1.1 INTERNAL CONFIGURATION

Figure 4.1 illustrates the system configuration with one internal Winchester Drive which the following replacement guide is intended for.

V9000/S1 With Internal Winchester Drive
Figure 4.1

STEP 1

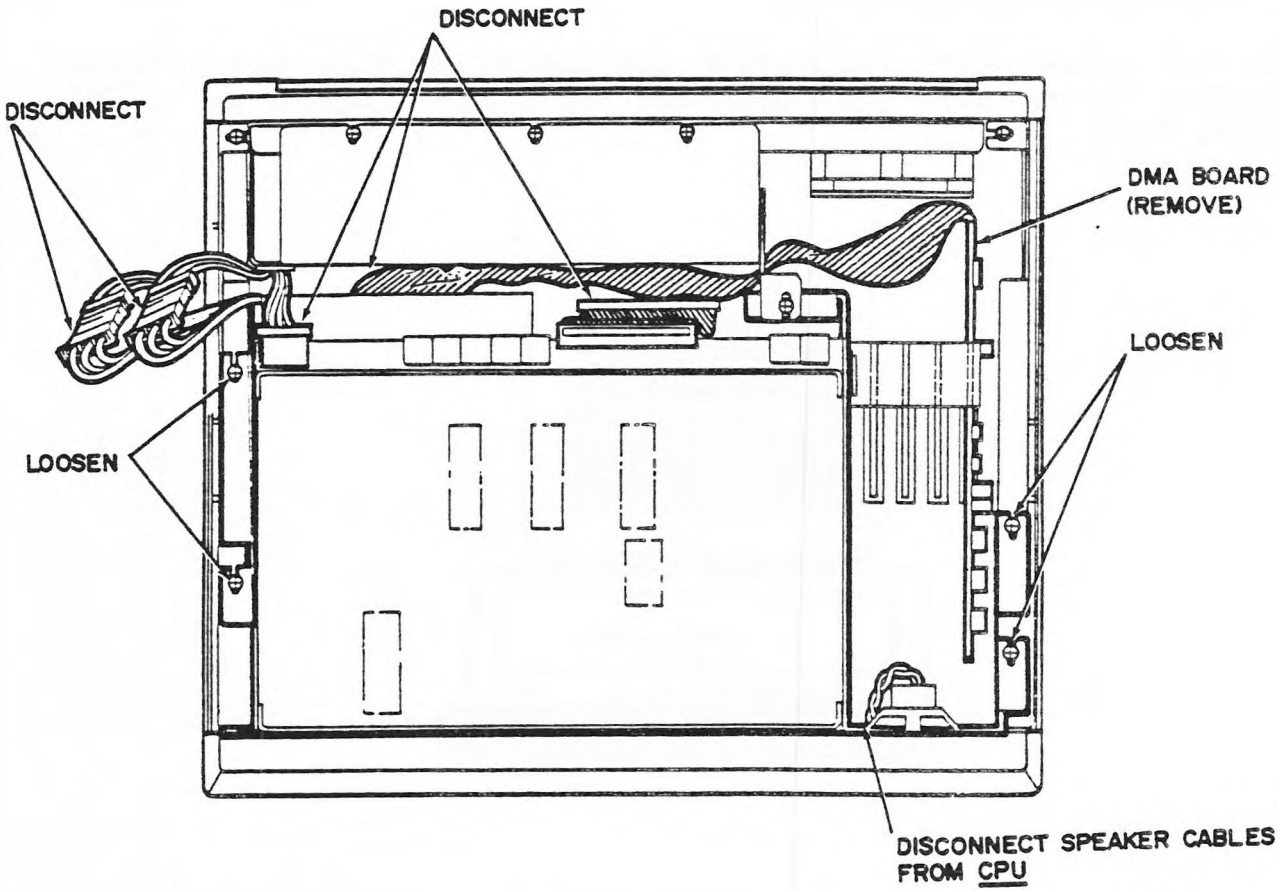
Turn system power off and allow at least 15 seconds for the Winchester Drive to stop spinning before proceeding.

STEP 2

Remove the back panel and top cover of the mainframe.

STEP 3

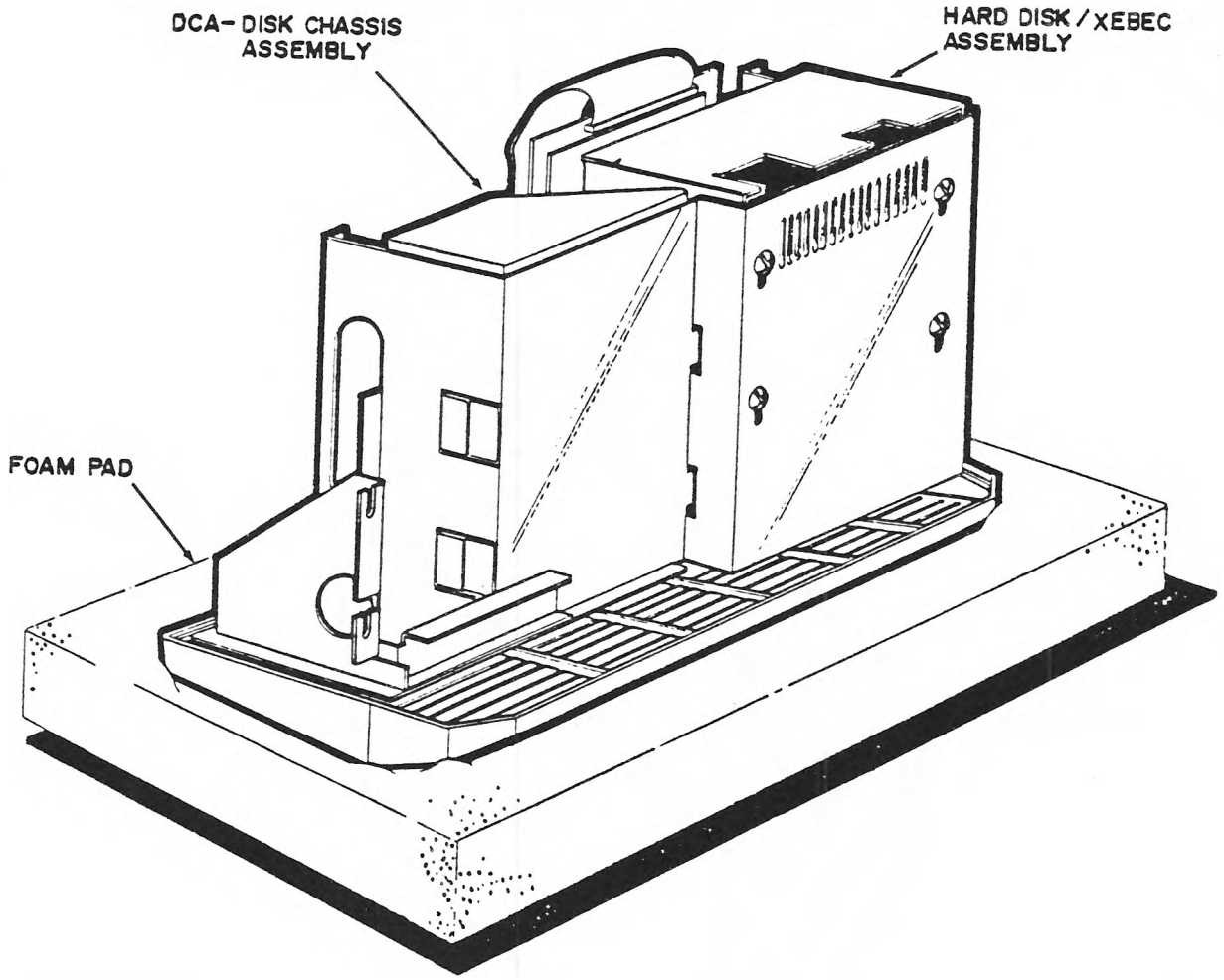
(Refer to Figure 4.2) Loosen the five Disk Chassis Assembly (DCA) screws and disconnect the Floppy Disk Controller Board Power Cable, Hard Disk Power Cable, Xebec Controller Power Cable, and CPU Logic Cable. Also, disconnect the SASI Bus Cable and remove the DMA Interface Board.



Mainframe, Disk Chassis Assembly (DCA), and Cables
Figure 4.2

STEP 4

The DCA is now ready to be removed from the mainframe. Carefully lift and slide forward the entire DCA making sure all cables are not caught on the mainframe chassis. Note the routing of the SASI Bus Cable for reinstallation of the DCA. Once free of the mainframe, rest the assembly (front bezel down) on foam or cardboard. (Refer to Figure 4.3)



Disk Chassis Assembly (DCA)
Figure 4.3

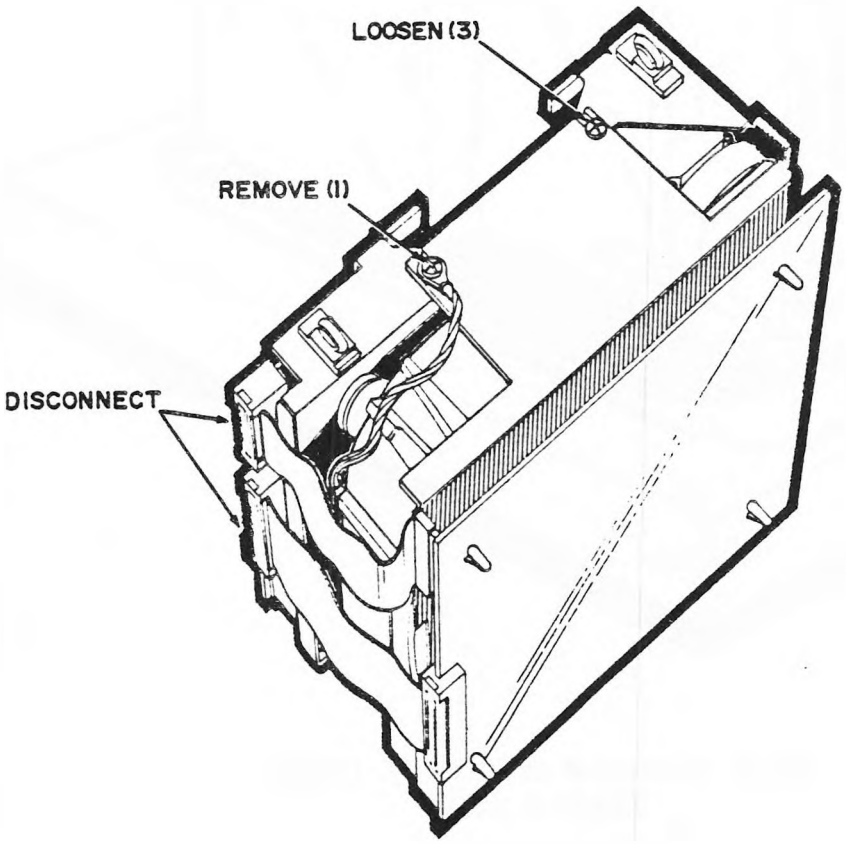
STEP 5

Remove the four screws which secure the Hard Disk/Xebec Board assembly and very carefully remove the assembly from the DCA. Note how the power cables are routed along the slot in the DCA so

they may be routed the same way when installing the replacement drive. Make sure all cables to the Floppy Disk Controller Board are to the side when the assembly is removed. Once removed from the DCA rest the assembly on a foam pad.

STEP 6

(Refer to Figure 4.4) Disconnect the ST506 Interface Cables from the Winchester Drive. Loosen the four screws which secure the Winchester Drive to the Xebec Board Mounting Bracket. The one screw which fastens the ground strap must be removed completely. Make sure the ground strap is installed on the replacement drive in the same manner as it was removed. Carefully remove the drive and place on a foam pad.



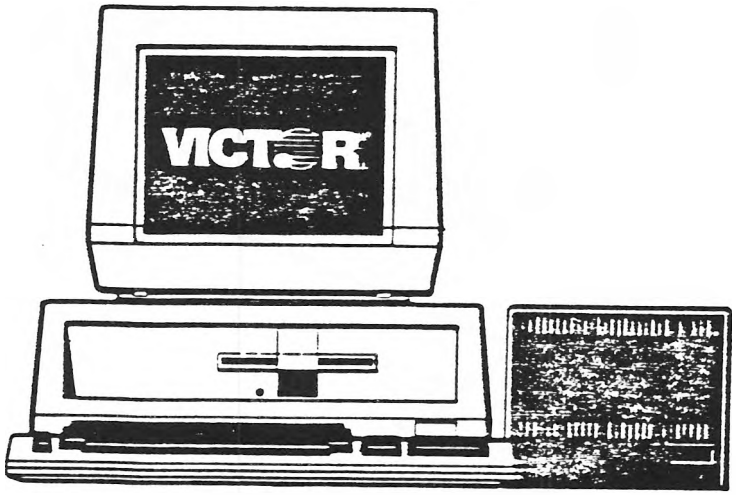
Winchester Drive/Xebec Board Assembly
Figure 4.4

STEP 7

The replacement drive may now be installed by following these procedures in reverse order.

4.1.2 EXTERNAL CONFIGURATION

Figure 4.5 illustrates the system configuration of one external Winchester Drive which the following replacement procedure is intended for.



V9000/S1 With External Winchester Drive
Figure 4.5

STEP 1

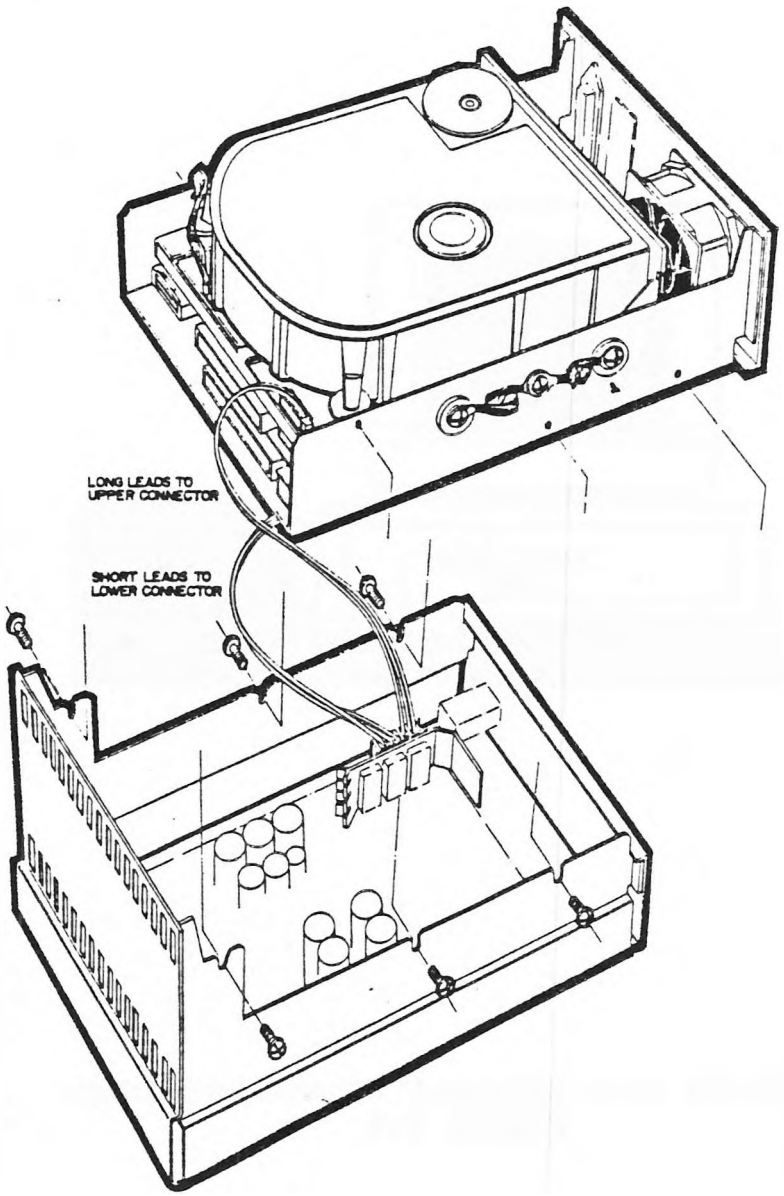
Turn power switch off on mainframe and external drive and allow approximately 15 seconds before proceeding.

STEP 2

Remove the four screws which secure the cover on the External Winchester Drive Unit.

STEP 3

(Refer to Figure 4.6) Loosen the six screws which secure the Winchester Drive/Xebec and Fan Chassis Assembly to the Power Supply Chassis Assembly. Remove the Winchester Drive/Xebec and



External Winchester Drive Unit (Internal View)
Figure 4.6

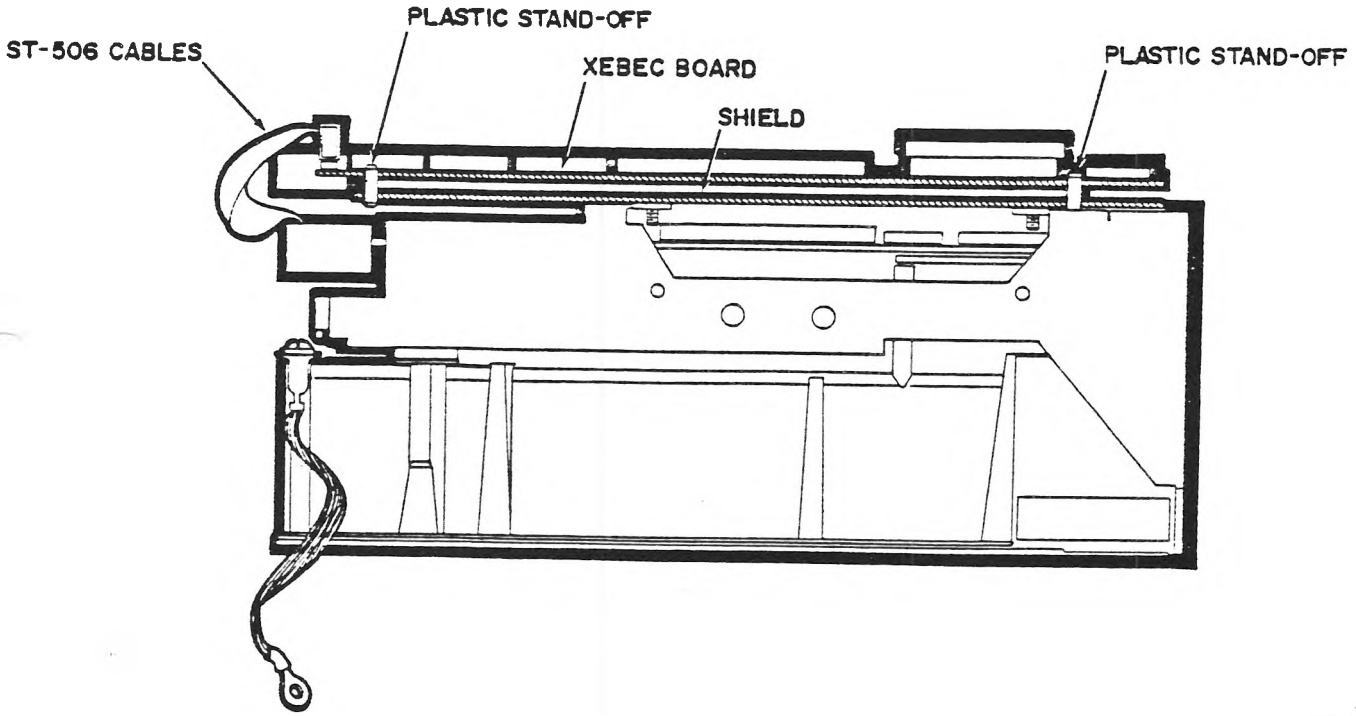
Fan Chassis Assembly and disconnect the power cables to the drive and Xebec Board. Note that the length of the power cables is such that they can only be re-connected to the proper board.

STEP 4

Remove the four screws which secure the Winchester Drive/Xebec Assembly to the chassis, carefully remove it and place on foam. The SASI Data Cable need not be removed.

STEP 5

(Refer to Figure 4.7) Disconnect the ST506 cables and (using a pair of needle nose pliers) remove the Xebec Board from it's mounting bracket by depressing the plastic standoffs. Remove the protective shield from the Winchester Drive Frame. Replacement of the drive may now take place.



Winchester Drive/Xebec Assembly
(External Configuration)
Figure 4.7

STEP 7

Simply follow this procedure in reverse order to reinstall the Winchester Drive paying particular attention to cable routing and placement.

4.2 XEBEC S1410 CONTROLLER REPLACEMENT

4.2.1 INTERNAL CONFIGURATION

Refer to Section 4.1.1 (Steps 1-5) to expose the Xebec S1410 Controller for replacement. Proceed with Step 6 as follows:

STEP 6

Using a pair of needle nose pliers depress the plastic standoffs to facilitate removal of the Xebec Board. Disconnect the SASI Bus Cable and the ST506 Interface Cables. Replace the board and then follow Section 4.1.1 (Steps 1-5) in reverse order.

4.2.2 EXTERNAL CONFIGURATION

Refer to Section 4.1.2 (Steps 1-5) for replacement guidelines.

4.3 DMA INTERFACE BOARD REPLACEMENT

Always a resident of the mainframe, the DMA Board is the easiest module of the Hard Disk Subsystem to replace.

STEP 1

Turn system power off and allow at least 15 seconds for the hard disk to spin down.

STEP 2

Remove the card guide and carefully remove the DMA board from the system expansion slot. Remove the SASI Bus Cable and replace the board and SASI Bus Cable.

NOTE: Make sure the DMA Board is configured properely for the type of system it is to be installed in. Refer to the configuration guide on the DMA Schematic, Figure 2.5, Sheet 1.

STEP 3

Replace the card guide, top cover, and back panel.

5. DIAGNOSTIC SOFTWARE

5.1 FIELD DIAGNOSTIC DISKETTE (HDFIELD) - VER 3.2

Designed for use in the end user's enviroment the diagnostic diskette HDFIELD will help the field engineer diagnose hardware and media related problems. Complete system tests may be invoked or individual modules of the system may be checked by executing the appropriate command. System tests included on this diskette are batch files IOK, XOK, and FOK.

IOK - (Internal Hard Disk System OK) Systems configured with one internal hard disk and one double-sided floppy disk drive.

XOK - (External Hard Disk System OK) Systems configured with one external hard disk drive and two floppy disk drives (double or single-sided).

FOK - (Floppy System OK) Systems configured with two floppy disk drives (double or single-sided) and no hard disk.

HDFIELD'S primary objectives are to:

1) Determine if the system hardware components are defective or degraded.

2) Determine the existence of defective hard disk media which is not currently logged in the drive header label.

These diagnostics reside on a diskette under the MSDOS operating system utilizing the CP/M Emulator. Before using this diskette create a backup on a double sided formatted diskette using dcopy. The "working" backup must have the write protect tab removed!!

Following is a brief description of the programs which are included in the HDFIELD package that excersise the hard disk subsystem:

SHOWSTAT Program SHOWSTAT reads the drive label and prints a summary of the label to the screen. This specifically includes a list of the current bad tracks. The distinction is made between bad tracks listed when the hard disk was initialized and those added after its initialization. The number of bad tracks which have been added during normal usage should be monitored as an indication of disk drive performance degradation. Also displayed is the hard disk serial number. Optionally, all displayed data can also be printed as hard copy output to the LST Device.

DMATEST Program DMATEST tests the hard disk DMA interface to CPU

board expansion bus. This testing is also performed in HDDISK under the DMA test (f2) option. The distinction is that DMATEST is limited to transferring data between the system main memory and hard disk controller memory. No drive access is performed.

HDDISK Program HDDISK is the hard disk test utility program. This utility allows the operator to test each component in the hard disk subsystem. The program is menu driven. The auto test (f1) is recommended as a start. If longer term tests are desired, either the random read (f5) or butterfly read test (f6) should be executed. This program writes only to the pre-established inservice diagnostic track (if it can be identified).

* * * * * * *

The following is a brief description of the tests included in the HDFIELD package to verify the remaining hardware not part of the hard disk subsystem:

******** NOTE ********

These tests are considered go/no-go, thus any failure during the test will halt the program with a failure indication. Error analysis is module related.

SERIAL INTERRUPT TEST (file name SIOITRV3) Tests the ability of the PIC (Programmable Interrupt Controller) to receive interrupt requests from the serial controller.

HIGH RESOLUTION TEST (file name HIRES) Tests high resolution display mode. Fills screen with high resolution display of vertical lines, a single dot wide.

ATTRIBUTES TEST (file name ATRIB) Tests display attributes; writes a message to the screen and then operates on the display attributes. The message is shown in standard, intensified, reverse video, non-display (secret), and underlined modes.

DRIVE BOARD TEST (file name DBT) Tests the floppy disk drives and the floppy drive controller board. Checks that the drive can read, write, and correctly operate at the various speeds. Verifies that the track 0 sensor, write protect switch, and door switch are functioning. DBT, with a command tail of "d b" will test double sided floppy drive "B" only.

CPU TEST (file name CPU) Tests the 8088 internal registers. Places known values in registers, pointers, and indexes and operates on them. Sets flag status to ensure proper operation of the flags.

SINE WAVE TEST (file name SINE) Tests the CODEC circuitry. Processes a constant data pattern through the CODEC circuits at different rates, which broadcasts various sine waves through the

speaker. In addition, verifies volume control (the volume is varied only during the last part of the test).

SERIAL CONNECTION TEST (file name SCONNECT) Tests the serial ports. Primary function is to test the function of lines that terminate on a 6522 chip, rather than the 7201 chip. (The ring indicator-RI- and data set ready - DSR - status bits of the RS-232 connections terminate on the 6522 chip)

Note: SCONNECT must run after Serial Port Test (SPT) to insure proper initialization of the PD7201 and 8253.

SYSTEM MEMORY TEST (filename RAMTEST) Validates the 128K or 256K standard RAM, the 4K static ram, and any Expansion RAM which might be in the system. Writes various data and address patterns to the RAM and verifies the patterns written with a checksum process.

TIMER INTERRUPT TEST (filename TIMIT) Tests the 8253 Timer Output. The 8253 Timer generates interrupts for the PIC. Sets timer for various time periods and polls the PIC with software to verify that interrupt requests pend only when they should.

SERIAL PORT TEST (filename SPT) Tests the serial communication controller. Passes data to and from ports A and B via the loopback cable and then verifies the data. Baud rates from 300 to 19,200 are used.

KEYBOARD TEST (filename KEYTEST) The keyboard test program uses the graphic (High Resolution) mode of the Victor microcomputer to display the keyboard on the screen. Verification of the keyboard is accomplished by depressing the keys and observing the screen.

5.1.1 TEST PHILOSOPHY

This test philosophy is directed at resolving perceived hard disk subsystem problems. If the CPU is defective, it could affect all communications and data analysis associated with the hard disk. Therefore, verification of the system hardware not part of the hard disk subsystem is essential before proceeding to the hard disk.

The two primary reasons for using the hard disk subsystem diagnostic software are to either diagnose and replace defective hardware components or to identify defective media not currently logged in the inservice media list.

Resolving a perceived Hard Disk Subsystem problem begins with the execution of SHOWSTAT. This performs almost no testing, but does confirm that the CPU board and hard disk can communicate. SHOWSTAT provides information about the state of the drive by displaying the drive header label. This includes summaries of the inservice and permanent media lists.

In SHOWSTAT, if the drive header label is defective or cannot be read, then it is virtually impossible for any further interragation of the drive. The only diagnostic software that may run is DMATEST. The item of most concern here would be to identify why the header is defective or cannot be read.

When the drive header label is not correct or cannot be read, it is possible that the failure is not in or associated with the drive, but instead may be in the data path leading to the drive. To help isolate the problem, DMATEST is run next.

DMATEST makes no drive access and provides a good test of the DMA card, and DMA cable (Host Interface Cable), as well as partial test of the controller. If DMATEST is successful, the problem is probably not in the DMA card or DMA cable. If the test fails however, the problem could be a defective DMA card, DMA cable, and/or quite possiblly the Xebec controller.

If SHOWSTAT is successful in reading the header label, the next program to execute is HDDISK. This is a test of the entire subsystem verifying functionality. The operator may select the test options desired from the HDDISK menu. It is recommended that the f1 (auto test) be executed first. In this test, the DMA card and DMA cable are tested as in DMATEST. When this mode successfully completes, a message indicates that the DMA card tested O.K. Next the program tests the Xebec Controller. The same basic tests are repeated, but this time, data is written to and read from the pre-established diagnostic track. All of the internal diagnostic functions of the controller are exercised.

Finally, the entire media is scanned searching for defective media not identified in the inservice media list. If any newly discovered defective media exists, it may be viewed by executing option f7 (Display New Bad). This test allows the user to define any possible defective media, but does not permit logging the bad areas into the defective media list since important information may reside in these areas. This gives the user the option of using HDFIXUP to salvage as much information as possible on the bad track.

If a more exhaustive testing is desired, option f5 (Random) or f6 (Butterfly) tests should be run. These do not perform DMA and controller tests. Random Test allows a random seek pattern to be performed on the media searching for defects. This test does not systematically scan the entire media. Butterfly Test scans the entire media with a butterfly read pattern searching for defective areas. Both tests will run until commanded to stop by hitting the space bar.

If this sequence of tests executes successfully, the subsystem has been tested as much as possible while protecting the end-user's data base. Without destroying the data base, no other tests are available.

As a last resort, system utility HDFORMAT could be used to reformat the entire drive. All data on the drive will be destroyed. The only exception to this is the drive header label. This must be readable; so that the inservice media list can be converted to the permanent media list and rewritten as the new drive label at the completion of this formatting process.

HDFORMAT is primarily intended to be used when large sections of the drive have become inoperative. This format utility will log bad tracks into the list as it finds them.

When HDFORMAT is run, the user is dependent on the latest ARCHIVE save of his data base. All data will be destroyed. HDFORMAT writes the drive label in the formatted state. This requires that HDSETUP be run again to initialize the drive. If HDFORMAT is run, the drive should then be reinitialized and the diagnostic process repeated. This will verify that HDFORMAT did, in fact, correct the problem.

5.1.2 SHOWSTAT

SHOWSTAT is intended to be used to interrogate the Winchester disk drive header label. SHOWSTAT performs no testing except for the fact it does prove the CPU can communicate with the hard disk. The program simply reads the drive header label and presents the information there recorded. The option to print the data to the LST device is provided as well as the option to dump the raw input buffer.

The following is a description of the output generated by SHOWSTAT including, where appropriate, valid responses:

LABEL TYPE This field describes the state of the drive. Valid responses are either 0 or 1. 0 is consistent with a formatted drive, 1 is consistent with an initialized drive.

DEVICE ID This is an identification of the revision level of the drive header label. The only valid response is a 1.

SECTOR SIZE This is the number of bytes in each drive sector. The only valid response is 512.

SERIAL NUMBER This is a 16 character ascii field that contains the drive serial number. Any data may be valid even though it should correspond to the actual serial number. Note: At the present time the serial number of the hard drive may be found on the Xebec Controller mounting bracket. (example number - W3210261) or on the drive itself.

IPL VECTOR These are the initial Boot Program load vector parameters. They may be non-zero in initialized drives only.

The field includes the following:

DISK ADDRESS	The logical disk address of the boot program image.
LOAD ADDRESS	The paragraph address of the memory where the boot program loads. A zero entry indicates a default load to the highest RAM location.
LOAD LENGTH	The length of the boot program in paragraphs.
CODE ENTRY	The memory address of the starting entry of the boot program. Segment of zero defaults to the segment of the loaded program.

PRIMARY BOOT VOLUME The virtual volume number whose label contains a second IPL vector and configuration information.

CONTROLLER PARAMETERS These are parameters which are drive specific, i.e. this part of SHOWSTAT helps the user determine which type of drive the system is using. They are as follows:

OF CYLINDERS
The number of cylinders on the drive:

Tandon TM502 = 306
Tandon TM603 = 230
Seagate ST412 = 306

OF HEADS
The number of heads on the drive:

Tandon TM502 = 4
Tandon TM603 = 6
Seagate ST412 = 4

1st READ WRITE CYCLE
This is the first cylinder for the controller to use reduced write current. The only acceptable value is 128.

1st WRITE PRECOMP
This is the first cylinder for the controller to apply write precompensation. The only acceptable value is 128.

ECC BURST LENGTH
This is the length of the ECC (Error detection and Correction Circuitry) burst error in the data field that the controller will correct. The only acceptable value is 11.

FAST STEP CONTROL BYTE
This is the controller parameter used to envoke the fast stepping algorithm for the specific drive:

Tandon TM502 = 7
Tandon TM603 = 2
Seagate ST412 = 6

INTERLEAVE FACTOR
This is the interleave factor used in formatting the drive. A value of 5 is normally used.

AVAILABLE MEDIA LIST A region list of the usable areas of the disk. From this, the tracks with hard errors and the useful capacity are inherently defined. This list may grow as more hard errors are detected when the drive is re-formatted. Each region is described :

* Physical Address - Disk address of the region.
* Region Size - The number of physical blocks in the region.

WORKING MEDIA LIST A region list of the working areas of the disk. This is derived from the available media list and from the detection of errors during use. Track sparing will cause this list to become unordered by address numbers. Each region is described by:

* Physical Address - Disk address of the region.
* Region Size - The number of physical blocks in the region.

VIRTUAL VOLUME LIST This list only exists on initialized drives. The list contains the number of virtual volumes and the disk logical address where the virtual volume label is contained.

5.1.2.1 SHOWSTAT Operator Instructions

Place the HDFIELD Diskette in floppy drive A or B and close the drive door.

Type SHOWSTAT

The only operator options in SHOWSTAT are to R (repeat the display), D (dump the raw data buffer in hex), P (print the data to the LST

device) and E (exit the program).

5.1.2.2 SHOWSTAT Error Analysis

While very few commands are used, it is possible to encounter errors in the process of reading the header label. Refer to Section 5.3 for error analysis.

5.1.3 HDDISK

HDDISK is designed to provide user definable tests of the hard disk subsystem. Tests are selected from a menu. The operator may choose from a DMA Test, Controller Test, or Media Tests. The Media Tests may be selected from sequential, random, or butterfly seeks. An Auto Test is provided which is a combination of the DMA Test, Controller Test, and Sequential Media Scan.

Similar to Auto Test, Quick Test is provided to verify the hard disk subsystem in less time than Auto Test. Also provided in HDDISK is a menu selection for viewing the drive header label and a selection for summarizing any new bad tracks discovered during testing. HDDISK is designed for use in the end-user enviroment as no writes are made to the drive except to the pre-established inservice diagnostic track.

Program HDDISK, once loaded, attempts to read the drive header label. If this is successful, parameters on the label are compared to determine if the drive is initialized and identify the drive. If this cannot be determined, an error is reported and the program stops. If the label can be identified the program continues. If the label is not initialized, but otherwise valid, a message is presented indicating that other tests may be used. This would be the case on systems from the factory that have no user data in storage.

5.1.3.1 HDDISK Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE HDDISK

A menu of tests is displayed and awaits operator commands. By pressing the appropriate Function Key the particular test is initialized. A small f (f) designates lower case function key and a capital F (F) represents the shifted mode of the function key.

A summary of each test option is provided below:

f1 Auto Test This runs tests f2, f3, and f4.

f2 DMA Test Data is written to the Xebec controller local memory and back to the host with a comparison made. This process is repeated under the appropriate interface variances. These variances are whether the data is being transferred in a block or byte mode (DMA or handshake), with the CPU locked in or out, and with interrupts being handled through polling or not. All possible combinations of these are varied repeating the data transfer and compares. Each operation is executed 10 times.

f3 Xebec Controller Test The pre-established inservice diagnostic track is identified and the DMA test process is repeated. This time however, the data is written to and read from the disk diagnostic track. If the inservice diagnostic track cannot be identified, an error message is presented.

All of the controller internal diagnostics are exercised. This includes a local RAM test, a local checksum process, and a drive interface test.

Any controller option that has not been run is then executed. This includes a specific check of the ECC process. Format options are not verified.

f4 Sequential Test The entire drive media surface is read looking for defective media not currently logged in the drive header label. If new media is discovered, it is logged and displayable upon breaking the scan process with a SPACE or by utilizing option f7. Only a single pass of the drive surface is made.

f5 Random Test The ramdom test performs the same function as the sequential test. In this case, a random addressing pattern is utilized instead of a sequential one. This test is an infinite test that is stopped by pressing the SPACE bar. Media errors are reported the same as in the sequential test.

f6 Butterfly Test This test is exactly the same as Random Test except a butterfly addressing pattern is used instead of a random pattern. This is preferable to random testing when media evaluation is the primary test objective. This test is infinite in duration stopped by pressing SPACE bar.

f7 Display New Bad When f7 is pressed, the program displays the defective media that has been discovered since the start of testing.

F1 Quick Test This causes the program to execute a quick version of f2, f3, and f4. Less DMA and Controller testing is performed and one fifth of the drive is sequentially scanned instead of all of it.

F2 Display Label This causes the program to display the contents of the drive header label as in SHOWSTAT.

F3 Extended Electronics Test This option causes the program to loop on f2 (DMA Test) and f3 (Controller Test). These components will be tested until the operator stops the program by pressing the SPACE bar. Once the SPACE bar is depressed the program will complete it's present test and then stop.

F7 Exit This places the heads on the innermost cylinder and terminates the program.

5.1.3.2 HDDISK Error Analysis

Refer to section 5.3 for any errors which might occur during HDDISK.

5.1.4 DMATEST

DMATEST is designed to perform a quick test of the DMA interface verifying it's functionality. Data is written to and from the Xebec controller buffer memory only. No communication with the drive is required.

5.1.4.1 DMATEST Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE DMATEST

5.1.4.2 DMATEST Error Analysis

Refer to Section 5.3 for any error messages which might occur.

5.1.5 SERIAL INTERRUPT TEST (SIOITRV3)

Designed to test the ability of the PIC (Programmable Interrupt Controller) to receive interrupt requests from the serial controller hardware (NEC 7201).

5.1.5.1 SIOITRV3 Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE SIOITRV3

A successful test will be indicated by the following output:

```
TIMES = 256
OK  OK   OK
We still retain control and have
seen the interrupts come and go in the PIC
```

A successful test will take approximately 30 seconds.

WARNING: The system will appear dead during the test (i.e. keyboard inactive, cursor off, door sense inhibited, etc.); this is normal operation. Also, the diskette will keep rotating.

5.1.5.2 SIOIRTV3 Error Analysis

A failure of SIOIRTV3 will resemble the following:

```
TIMES  =  <number less than 255>
FAIL  --  FAIL  --  FAIL  --  FAIL
FAIL  --  FAIL  --  FAIL  --  FAIL
```

The system will appear to hang when a failure occurs but a carriage return will exit to the operating system.

A failure of SIOIRTV3 indicates a faulty CPU board.

5.1.6 HIGH RESOLUTION TEST (HIRES)

This test program tests the subcircuits which generate the high resolution graphic image on the screen by the Victor display system.

5.1.6.1 HIRES Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE HIRES

The screen will display two zones of vertical lines.

The left side of the screen displays 16 dark lines (one bit wide) for each bit of a character. Dark lines 0 thru A represent bits 0 thru A of a character.

If the subcircuits of the display system are faulty the displayed dark lines will be blocked and white dots will be displayed on these lines.

The right side of the screen is a reverse video of the left side.

After 5 seconds the display will reverse and the program will wait for the exit command (Carriage Return Exits).

CAUTION: It is necessary to wait for the screen to reverse before exiting this test by typing Carriage Return.

5.1.6.2 HIRES Error Analysis

A failure of HIRES indicates a possible fault with the CPU Board or Video Board.

5.1.7 ATTRIBUTES TEST (ATRIB)

This test verifies the ability of the display systems attributes. First a message is written to the screen and it is then operated on by displaying the message in standard mode, intensified, reverse video, nondisplay, and underlined.

5.1.7.1 ATRIB Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE MSBASIC ATRIB

The test may be terminated at any time by typing: CARRIAGE RETURN

5.1.7.2 ATRIB Error Analysis

Any failure to display the appropriate attribute indicates either a faulty CPU Board or Video Board.

5.1.8 DISK BOARD TEST (DBT)

Disk Board Test checks the functionality of the floppy disk controller board and single or double sided floppy drives installed in a system. It verifies that either drive can operate correctly at the various speeds when writing or reading and that the track 0 sensor, write protect switch, and door switch are functioning.

Adding a command tail such as "d b" instructs the diagnostic to test the double sided B drive only. (Internal Hard Disk Systems)

5.1.8.1 DBT Operator Instructions

With the HDFIELD Diskette in floppy drive A or B and a formatted disk in the other drive (if configured with two floppy drives):

NOTE: The formatted diskette must be formatted double or single sided accordingly.

TYPE DBT (For test of two floppy drive system)

DBT Test Sequence:

Speed Test

Write Test

Read Test

TRK0 Sense Test

Switch Test

The program will prompt the user to test the door and write protect switch with SWITCHES? The operator at this point should remove the diskette and re-insert.

The diskette need not be completely removed from the disk drive but only enough to trip the write protect switch.

Once the diskette has been re-inserted a "door closed" message will begin to scroll on the display. At this time CLOSE THE DRIVE DOOR.

Repeat this for the second drive if installed.

To terminate type:

Carriage Return

Using the command tail "d b" (DBT d b) will invoke the floppy drive test for a double sided floppy drive B only.

5.1.8.2 DBT Error Analysis

Any failure during this test indicates a faulty Floppy Drive Controller, Floppy Drive or CPU Board.

5.1.9 CPU TEST (CPU)

The CPU Test is designed to exercise and test the basic instruction set used by the 8088 and check its internal registers.

The test displays symbolically each register and upon successful completion of the test will print "OK" in each register position. If the program detects an error in any of the CPU tests it will display "CPU ERROR".

5.1.9.1 CPU Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE CPU

5.1.9.2 CPU Error Analysis

Failure of this test indicates a faulty CPU board. (most likely the 8088 itself)

5.1.10 SINE WAVE TEST (SINE)

Used to test the CODEC circuitry this test produces a series of sine waves that results in five tones:

1. 6,250hz
2. 3,900hz
3. 3,000hz
4. 1,100hz
5. 100hz

All tones are produced with the volume control full on. The last tone (100hz) is produced at eight different volume levels to verify that the volume control works.

5.1.10.1 SINE Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE SINE

The test automatically returns to the operating system.

5.1.10.2 SINE Error Analysis

Failure indicates problem with CPU board or speaker.

5.1.11 SERIAL CONNECTION TEST (SCONNECT)

Tests status lines used by the serial ports. Checks lines that terminate on a 6522 chip rather than the 7201 serial communication controller, ring indicator (RI) and data set ready (DSR) status bits of the RS-232 connections.

Note: This test requires a Serial Port Loopback Cable!!

5.1.11.1 SCONNECT Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE MSBASIC SCONNECT

5.1.11.2 SCONNECT Error Analysis

Failure of this test indicates a faulty CPU board.

5.1.12 SYSTEM MEMORY TEST (RAMTEST)

RAMTEST tests all ram in the system, including the dynamic ram, 4K static ram, and all expansion ram installed in the expansion slots. Dynamic ram is addressed 0000:0 to 1FFF:F on 128K CPU boards, 0000:0 to 3FFF:F on 256K CPU boards ,Static ram F000:0 to F100:0, and expansion ram beginning at 2000:0 or 4000:0 (depending on type of CPU board, 128K or 256K respectively) to a maximum address of DFFF:F.

Error messages identify the failing memory address of the failure, and expected and actual data found.

RAMTEST will run a number of passes, as specified in a command tail, and then exit to a reboot sequence in the system ROM, as if the system reset had been pushed. RAMTEST preserves a displayed error message by not rebooting if an error has occured.

The number of passes to be run may be any value from 1 to 9999 decimal. If no command tail is included, the program defaults to one pass.

A ten hour run may be selected by passing a command tail of "$". The number of passes to run in a ten hour period is inversely proportional to the amount of RAM installed

A pulsing heart is displayed next to the pass count. If RAMTEST continues normally, this heart is pulsed periodically. Test "run" time is also displayed.

NOTE: If ten hour test is invoked the time count will run from 10:00 to 00:00.

5.1.12.1 RAMTEST Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE RAMTEST

To run the test more than once:

TYPE RAMTEST [n] Where n = number of times from 1 to 9999.

5.1.12.2 RAMTEST Error Analysis

Failure indicates a faulty CPU board or expansion RAM card if installed.

5.1.13 TIMER INTERRUPT TEST (TIMIT)

Designed to test the 8258 Programmable Timer Chip. The program uses the 8253 Timer to generate the Interrupt Request Signal thru the PIC and then verify it.

The count for the Timer to generate the interrupt signal ranges from 100 to 5200. The increment is 20. The test will cycle 255 times before exiting.

5.1.13.1 TIMIT Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE TIMIT

A Succesful pass will be displayed by the following message:

```
TIMER INTERRUPT TEST VERSION E 4.1

TIMES = 255

OK! OK! OK!

THE PRIORITY INTERRUPT CONTROLLER IS GOOD FOR THE
TIMER INTERRUPT TEST
```

An unsuccessful test will display the following:

```
TIMER INTERRUPT TEST VERSION E 4.1

TIMES = XXX ---- (A NUMBER LESS THAN 255)

LARGE FLASHING FAILURE DISPLAY

Type: Carriage Return to exit
```

If the test is successful the program exits to the operating system.

5.1.13.2 TIMIT Error Analysis

Failure of this test indicates a faulty CPU board.

5.1.14 SERIAL PORT TEST (SPT)

This test was designed to test the serial communications controller. Data is transferred between ports A and B via the loopback cable. Baud rates from 300 to 19,200 are used.

5.1.14.1 SPT Operator Instructions

Before running the test a Serial Port Loopback Cable must be installed between ports A and B.

To run the test once type:

SPT

To run the test more than once type:

SPT [n] Where n = any number from 0 to 64000.

If the test is successful, an 'OK' will be displayed and the Program will exit to the operating system.

If the test is unsuccessful, a 'FAIL' will appear on the screen that will alternate between normal and reverse video.

To exit this FAIL indication simply type Carriage Return

5.1.14.2 SPT Error Analysis

A failure of this test indicates a faulty CPU board or possibly the loopback cable.

5.1.15 KEYBOARD TEST (KEYTEST)

The keyboard test program uses the graphic (high resolution) mode of the computer to display exactly the selected keyboard on the screen.

When the user types (closes) one key, the keyboard controller senses the key being depressed and the highlighted image of this selected key will be displayed on the screen.

When the user releases the key, the keyboard controller senses the the key being released and the shaded image of this selected key will

be displayed on the screen.

5.1.15.1 KEYTEST Operator Instructions

With the HDFIELD Diskette in floppy drive A or B:

TYPE KEYTEST

To exit the test:

TYPE CONTROL KEY 1 and then CONTROL KEY 7

5.1.15.2 KEYTEST Error Analysis

Failure of any key indicates either a bad keyboard or CPU board.

5.1.16 INTEGRATED SYSTEM TESTS - IOK, XOK, and FOK

As overall system tests; IOK (Internal Hard Disk System OK), XOK (External Hard Disk System OK), and FOK (Floppy System OK) were created to provide easy-to-use quick checks of system performance. FOK should execute successfully in approximately 8-10 minutes with no expansion ram present. Each additional block of ram will require 3 or 4 more minutes of testing. XOK and IOK should require approximately 15 minutes to complete successfully.Minimal operator interface is required. When running XOK or FOK a double sided formatted diskette is required.

These System Tests are batch files made up of the following individual tests:

	DIAGNOSTIC TEST	FILENAME
	CPU TEST	CPU
	TIMER INTERRUPT TEST	TIMIT
	SERIAL INTERRUPT TEST	SIOITRV3
	SERIAL PORT TEST	SPT
	SERIAL CONNECTION TEST	SCONNECT
	ATTRIBUTES TEST	ATRIB
	HIGH RESOLUTION TEST	HIRES
	SINE WAVE TEST (CODEC)	SINE
*	FLOPPY DRIVE TEST	DBT
**	HDDISK $ (DMA, XEBEC, AND MEDIA SCAN)	HDDISK
	RAMTEST	RAMTEST

* NOTE: System Test IOK, when running DBT, makes use of the command tail "d b" to test the double sided floppy drive B installed in a hard disk "internal" system.

** NOTE: System Test FOK does not use HDDISK.

5.1.16.1 IOK, XOK, and FOK Operator Instructions

Before executing these system tests a serial port loopback cable must be properly installed between port A and port B.

If running IOK - Insert HDFIELD "backup" diskette in floppy drive B. The diskette must have the write protect tab removed!

If running XOK / FOK - Insert HDFIELD "backup" diskette in floppy drive A or B. Insert a double sided formatted diskette in the other drive. The diskette must have the write protect tab removed!

To start the test type the appropriate command for the system configuration you are testing:

IOK (Internal Hard Disk Systems)

or

XOK (External Hard Disk Systems)

or

FOK (Floppy Systems)

An information banner will appear on the screen concerning the version of the diagnostics and system configuration data. Simply hit any key to continue with the test.

The test sequence is as follows:

CPU .....Note if all "OK's" are displayed

B:TEMP1 (TIMIT) .....Timer Interrupt Test

B:TEMP2 (SIOITRV3).....Serial Interrupt Test

SPT .....Serial Port Test

MSBASIC SCONNECT .....Serial Connection Test

MSBASIC ATRIB .....Atributes Test
Note: To terminate PRESS RETURN

HIRES .....High Resolution Test
Note: To terminate PRESS RETURN

SINE .....Sine Wave Test (Codec)

DBT .....Drive Board Test
Note: At the program prompt SWITCHES - Remove the diskette just enough to trip the write protect switch and then re-insert the diskette.

Close the drive door

REPEAT FOR OTHER DRIVE IF SO EQUIPPED

To terminate PRESS RETURN

HDDISK $ .....This tests the DMA board, Xebec Controller board, and then sequentially scans the media.

****
Note: HDDISK is not part of FOK.
****

To terminate PRESS RETURN

RAMTEST.....Flashing heart pattern indicates test is running.
Timer indicates the run time of the test.

5.1.16.2 SYSTEM TEST Error Analysis

PROGRAM	SUSPECT HARDWARE
CPU	CPU BOARD
RAMTEST	CPU BOARD OR XRAM CARD
TIMIT	CPU BOARD
SIOITRV3	CPU BOARD
SPT	CPU BOARD
SCONNECT	CPU BOARD
ATRIB	CPU BOARD, VIDEO BOARD
HIRES	CPU BOARD, VIDEO BOARD
SINE	CPU BOARD, SPEAKER
DBT	CPU BOARD, FLOPPY DISK CONTROLLER, DRIVE
HDDISK $	REFER TO SECTION 5.3

5.3 DIAGNOSTIC ERROR REPORTING

This section of the manual describes the error messages associated with the Hard Disk Subsystem Diagnostics. Specifically, this applies to the following software:

SHOWSTAT
DMATEST
HDDISK

Error reporting by the Hard Disk Diagnostics is designed to direct the Field Engineer towards possible faulty components. The error message will list the suspect hardware in a descending order of probability. Interface errors typically indicate faulty connections or cables. Controller errors are associated more with the DMA board, Xebec Controller board, and the Drive Unit itself.

Error messages which might occur are as follows. Included with each message is a more detailed description of the problem.

1. INTERFACE ERROR
   CONTROLLER TIMEOUT WAITING FOR IO DIRECTION
   POSSIBLE FAILURES ARE
   DMA CABLE
   XEBEC CONTROLLER
   DMA CARD

   The data transfer had been initiated and upon interregation of the direction line, the data path had reversed unexpectedly.

2. INTERFACE ERROR
   CONTROLLER TIMEOUT WAITING FOR REQUEST SIGNAL
   POSIBLE FAILURES ARE
   DMA CABLE
   XEBEC CONTROLLER
   DMA CARD

   The controller was strobed to accept a command and no request response was issued.

3. INTERFACE ERROR
   CONTROLLER TIMEOUT WAITING FOR BUSY SIGNAL
   POSSIBLE FAILURES ARE
   DMA CABLE
   XEBEC CONTROLLER
   DMA CARD

The processor was waiting for the Busy signal to come available and it never did.

4. INTERFACE ERROR
CONTROLLER TIMEOUT WAITING FOR COMMAND SIGNAL
POSSIBLE FAILURES ARE
DMA CABLE
XEBEC CONTROLLER
DMA CARD

The processor was waiting for the command signal and it never became available.

5. INTERFACE ERROR
ERROR STATUS INPUT
POSSIBLE FAILURES ARE
DMA CABLE
XEBEC CONTROLLER
DMA CARD

An attempt was made to check the status of the controller and an error was returned for the request status command.

6. INTERFACE ERROR
BUS STATUS ERROR DURING DCB OUTPUT
POSSIBLE FAILURES ARE
DMA CABLE
XEBEC CONTROLLER
DMA CARD

While transferring the DCB (Data Control Block) to the controller, an error was encountered.

7. INTERFACE ERROR
CONTROLLER TIMEOUT WAITING FOR INTERRUPT TO COMPLETE
POSSIBLE FAILURES ARE
DMA CABLE
XEBEC CONTROLLER
DMA CARD

Data was being transferred utilizing interrupts (poll N) and the transfer did not return.

8. ERROR
POSSIBLE FAILURES ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

The controller detected no error during the execution of the previous command.

9. ERROR
NO INDEX DETECTED FROM THE DISK DRIVE
POSSIBLE FAILURES ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

The controller did not detect an index signal from the drive.

10. ERROR
NO SEEK COMPLETE SIGNAL FROM DRIVE
POSSIBLE FAILURS ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

The controller did not receive a seek complete signal from the drive unit after a seek operation.

11. ERROR
WRITE FAULT DETECTED FROM DRIVE
POSSIBLE FAILURES ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

The controller detected a write fault from the drive unit during the last operation.

12. ERROR
DRIVE NOT READY AFTER IT WAS SELECTED
POSSIBLE FAILURES ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

After the controller selected a drive, the drive did not respond with a ready signal.

13. ERROR
TRACK ZERO NOT DETECTEDD ON RECALIBRATE
POSSIBLE FAILURES ARE
DISK DRIVE UNIT
STATUS/CONTROL CABLE

After stepping the maximum number of cylinders, the controller did not receive a track 00 signal from the

drive unit.

14. ERROR
ADDRESS MARK NOT FOUND
POSSIBLE FAILURES ARE
RADIAL CABLE
DRIVE
XEBEC CONTROLLER

The controller did not detect the target address mark on the disk.

15. ERROR
SEEK ERROR
POSSIBLE FAILURES ARE
STATUS/CONTROL CABLE
DISK DRIVE UNIT

The controller detected an incorrect cylinder or track, or both.

16. ERROR
FORMAT ERROR
POSSIBLE SOFTWARE ERROR
During a check-track command, the controller detected one of the following:

1) Track not formatted
2) Wrong interleave
3) ID ECC error on at least one sector

17. ERROR
INVALID COMMAND
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CARD
DMA CABLE

The controller has received an invalid command from the host.

18. ERROR
ILLEGAL SECTOR ADDRESS
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CABLE
DMA CARD

The controller detected an address that is beyond the maximum range.

19. ERROR
RAM DIAGNOSTIC FAILURE
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CABLE
DMA CARD

The controller detected a data error during the RAM sector buffer diagnostic. (Xebec Controller RAM)

20. ERROR
MEMORY CHECKSUM ERROR
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CABLE
DMA CARD

During it's internal diagnostic, the controller detected a program-memory checksum error.

21. ERROR
ECC DIAGNOSTIC FAILURE
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CABLE
DMA CARD

During the controller's internal diagnostic, the hardware ECC generator failed its test.

22. COMPARE ERROR
POSSIBLE FAILURES ARE
XEBEC CONTROLLER
DMA CABLE
DMA CARD

In many write tests, data compares are performed. This is simply the processor comparing what was read to what was written. If a compare error is encountered, this implies that the controller did not detect an ECC error.