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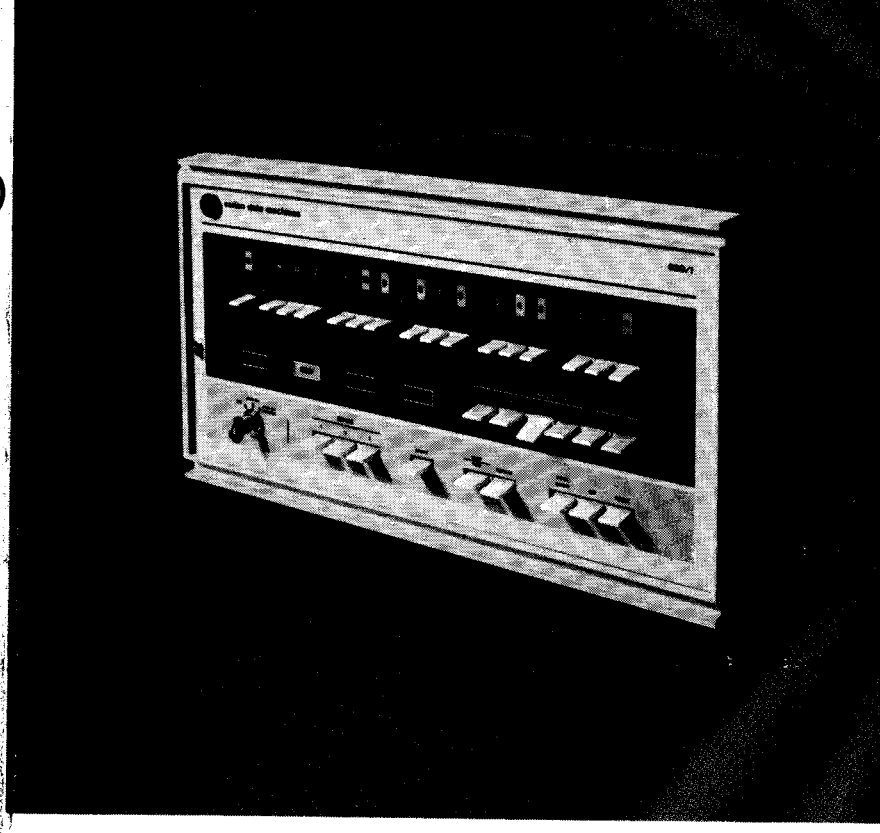

varian 620/f computer handbook

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The Big Company in Small Computers

620/f

COMPUTER HANDBOOK

APRIL 1970

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SECTION 1

USE AND ORGANIZATION OF THE MANUAL

This manual contains an overall description of the Varian Data Machines 620/f computer system.

The manual is divided into five chapters. Chapter I describes the documentation package provided with each computer.

Chapter II contains the system organization that includes a functional description of the computer, specifications of the computer and of internal computer options, and general information concerning system planning.

Chapter III describes peripheral capabilities and consists of a functional description of the 620/f input/output system and descriptions and specifications of peripheral controllers.

Chapter IV describes system operation including preliminary operating procedures and the controls and indicators necessary to operate the computer. Programming concepts and the complete instruction repertoire are also included in this chapter.

Chapter V describes the maintenance concepts of the computer system. Topics discussed include circuit card accessibility, diagnostic programs, and troubleshooting.

Appendices to this manual contain reference material consisting of powers of two, octal to decimal conversion, standard character codes, and teletype character codes.

SECTION 2

SUPPORT DOCUMENTATION

To ensure that the user can utilize the full capability of the 620/f computer system, a series of technical manuals (of which this manual is a part) is provided with each computer.

The 620/f programming reference manual contains the information necessary for programming the computer. The 620/f maintenance manual contains installation and interface data, computer theory of operation, and complete maintenance information. Logic and schematic diagrams, assembly drawings, and wire lists are contained in volume 2 of the maintenance manual. The 620/f read-only memory manual provides a complete description of the read-only memory available with the 620/f computer; the contents of this manual include operation, installation, and maintenance information. In addition, maintenance manuals are provided with each of the internal 620/f computer options. The contents of these manuals include operation, installation, and maintenance information.

Technical manuals provided for the 620/f computer system are:

Document Number	Title
98 A 9908 000	620/f System Reference Manual
98 A 9908 020	620/f Programming Reference Manual
98 A 9908 050	620/f Maintenance Manual
98 A 9908 110	Buffer Interlace Controller Manual
98 A 9908 300	620/f Automatic Bootstrap Loader Manual
98 A 9908 420	620/f Priority Memory Access Manual
98 A 9908 430	620/f Hardware Multiply/Divide Manual
98 A 9908 440	620/f Power Failure/Restart Manual
98 A 9908 450	620/f Real-Time Clock Manual
98 A 9908 540	620/f Read-Only Memory Manual

SECTION 3

SPECIAL SYSTEM DOCUMENTATION

Documentation is also provided for special equipment designed to meet specific customer requirements. Such items include internal computer options, peripheral controllers, and computer configurations that are not considered standard features of the 620/f computer system.

The special system documentation consists of engineering documents such as product performance specifications, installation and assembly drawings, and wire lists. Technical manuals similar to those included in the standard documentation package can also be provided for special equipment.

SECTION 1

COMPUTER SYSTEM

1.1 INTRODUCTION

The Varian Data Machines 620/f computer is a high-speed, general-purpose, digital computer for scientific and industrial applications. Its features include:

Fast operation:	750-nanosecond memory cycle
Large Instruction repertoire	148 instructions
Word length:	16 bits
Modular core memory:	Expandable to 32,768 words in 4,096- or 8,192-word increments
Read only memory:	Contains addressable core, 16-bit word length. Provides a CPU cycle time of less than 550 nanoseconds
Automatic data transfer:	Direct memory access facility provides automatic data transfers with rates to 276,000 words per second
Multiple addressing:	Direct, indirect, relative, index (pre and post), immediate, and extended
Flexible I/O:	Ten devices may be placed on the I/O bus. The I/O system can easily be expanded to include features such as automatic block transfer, priority interrupt, and cycle-stealing data transfers

Extensive software	Complete package includes a symbolic assembler, subroutine library, AID diagnostics, and an ASA FORTRAN compiler

This section provides an overall description of the computer, and consists of computer organization and physical characteristics.

1.2 COMPUTER ORGANIZATION

The functional sections of the computer are illustrated in figure II-1, and described in the following sections.

1.2.1 Control Section

The computer control section generates the basic 9.1 MHz system clock that provides the timing and control signals for all computer operations. It directs the transfer of data between the registers and controls the operations performed. It also interprets instructions read from memory and provides gating functions for executing them. Information from the instruction (I) register is used to generate the timing and control signals.

1.2.2 Decode Section

The decoding section decodes the fields of the instruction word held in the I register to determine the control signal levels. These levels select the timing signals generated by the timing unit in the control section.

1.2.3 Arithmetic Unit

The arithmetic unit performs arithmetic operations and manipulates data. It contains the adder and gating required for the arithmetic logical and shifting operations.

The arithmetic unit also controls the gating of words from the operational registers and the I/O bus to the C bus where they are distributed to the operations or memory registers.

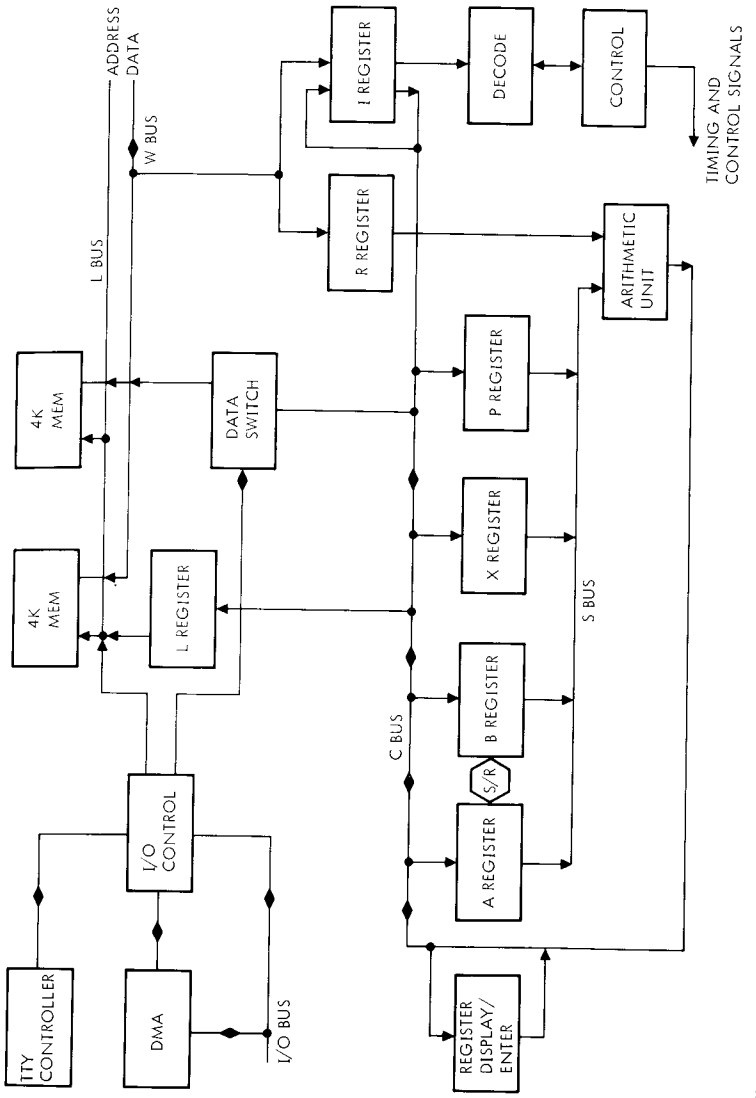

Figure II-1. Computer Functional Organization

1.2.4 Operations Registers

The operations registers are designated A, B, X, and P. The A, B, and X registers are directly accessible to the programmer. The P register is indirectly accessible through use of the jump-class instructions which modify the program sequence.

a. A register. This 16-bit register is the upper half of the accumulator and accumulates the results of logical and addition/subtraction operations, the most significant half of the double-length product in multiplication, and the remainder in division. The A register may also be used for I/O transfer under program control.

b. B register. This 16-bit register is the lower half of the accumulator and accumulates the least significant half of the double-length product in multiplication and the quotient in division. It may also be used for I/O transfers under program control and as a second hardware index register.

c. X register. This full-length register permits indexing of operand addresses without adding time to the execution of indexed instructions.

d. P register. This 15-bit register holds the address of the current instruction and is incremented before each new instruction is fetched. A full complement of instructions is available for conditional and unconditional modification of this register.

1.2.5 Auxiliary Registers

The auxiliary registers are designated I, L, and R.

a. I register. This 16-bit instruction register receives each instruction from memory through the W bus and holds the instruction during its execution. The control fields of the instruction word are routed to the decoding section to determine the required timing and control signals. The five least significant bits of the I register are used as a counter for shift instructions. The I register is accessible to the programmer through the control console.

b. L register. This 16-bit address register contains the address of the memory location currently being accessed.

c. R register. This 16-bit buffer register holds the operations to occur on a memory-cycle-steal basis.

1.2.6 Data Switch Section

The data switch section provides gating logic for operand data being read from or written into memory.

1.2.7 Register Display/Enter Section

The register display/enter section allows the contents of the A, B, X, P, and I registers to be displayed on the appropriate console indicators. This section also enters data and instructions from the console switches to the A, B, X, P, and I registers.

1.2.8 Shift and Rotate

The shift and rotate (S/R) circuit is a special data path to implement A and B register shifts.

1.2.9 Internal Buses

The basic computer contains five buses designated as C, S, W, L, and I/O.

a. C bus. This bus provides the parallel path and selection logic for routing data between the arithmetic unit, data switch section, the operations registers (A, B, X, and P), and auxiliary registers (I and L).

b. S bus. This bus provides the parallel path and selection logic for routing data from the operations registers to the arithmetic unit.

c. W bus. The data switch section is directly connected to all memory modules through the W bus. This bus is actually two unidirectional buses which are time-shared among memory modules.

d. L bus. The L register is directly connected to all memory modules through the unidirectional L bus.

e. Input/output bus. The input/output (I/O) bus is a party-line, bidirectional bus. It permits programmed data transfers between peripheral devices and the computer. The I/O bus also permits plug-in expansion of all peripheral controllers.

1.2.10 Input/Output Control

The I/O control section provides I/O timing and control signals and contains a 16-bit register for the direct memory access (DMA) I/O functions.

1.2.11 Teletype Controller

The teletype controller controls the commands and data transfer between the central processing unit (CPU) and the factory-modified 33 ASR or 35 ASR. The teletype operation is full-duplex, asynchronous, and serial, using the 11-bit ASCII code set.

1.2.12 Memory

The 620/f memory is an expandable, random-access, 3-wire/3D, magnetic-core memory. It provides program and data storage for tthe 620/f computer. The basic package accommodates 4,096 or 8,192 sixteen-bit words. The system is expandable to 32,768 words in 4,096- or 8,192-word increments.

Instruction words read from memory are transferred to the control section for execution. Words may be transferred, under program control, from memory to the arithmetic unit, to the operational registers, or to the I/O bus. Words can be transferred, under program control, to memory from the operations registers or the I/O bus.

Each 8,192-word memory increment consists of four circuit cards.

a. Card 1 contains timing control, address register and decode, data register, and line driver circuits.

b. Card 2 contains two current sources (X and Y) and 32 pairs of switch drivers.

c. Card 3 contains a memory stack module consisting of a diode decoding matrix and a magnetic core array.

d. Card 4 contains 32 inhibit drivers and 32 sense amplifiers. Each half of the inhibit drivers and sense amplifiers is associated with a 4,096 sixteen-bit core mat.

The 620/f memory features a master/slave arrangement, whereby the slave memory module (4K or 8K increment) uses the timing circuits of a master memory module. The slave memory module requires no card 1, thus providing an economical method of memory expansion. However, if the user requires a memory module installed at a distance of up to 10 feet from the computer mainframe, a master memory module (4K or 8K increment) can be used. The block diagram in figure II-1 illustrates a master/master arrangement.

A read only memory (ROM) to provide a nonvolatile computer word storage is also available. It is directly addressable by the CPU which accesses it in the same manner as the regular 3-wire/ 3D memory. The contents of the ROM are prewired at the factory to the user's specifications. From a system point of view, all ROMs are addressed above the regular memory. When operating from the ROM, the CPU cycle time is less than 550 nanoseconds.

1.2.13 Direct Memory Access

The DMA circuit provides the computer with a trapping capability. The DMA trap function consists of automatic data transfers between computer memory and peripheral controllers (such as teletype, paper tape, and magnetic tape controllers). It allows a peripheral device to request the transfer of a data word while temporarily halting the processing of the stored program. To implement the DMA trap function, an optional buffer interlace controller (BIC) must be installed to generate the required trap-out and trap-in requests. To prevent several peripheral devices from requesting data transfers at the same time, an optional priority interrupt module (PIM) can be used to determine the order in which the requests occur. During the interval in which the transfer takes place, the stored program is stopped for 1.8 microseconds for a trap-out operation and 2.3 microseconds for a trap-in operation. This cycle-stealing does not disturb the contents of the operations registers (A, B, X, and P). In this way,

the program can proceed normally at the conclusion of the transfer. The data-transfer rate of the DMA trap function can be as high as 276,000 words per second. This can be determined by adding the trapping sequence time (2.7 microseconds) and the synchronization time (0.92 microseconds), the sum of which gives a transfer-rate period of 3.62 microseconds which is equal to 276,000 words per second.

1.2.14 Interrupt Capabilities

The computer has interrupt capabilities that allow certain internal computer options, on a priority basis, to request the computer to execute an instruction independent of the program in progress. The computer options that can be used in conjunction with the interrupt function are the power fail/restart (PF/R), real-time clock (RTC), PIM, and BIC. During the interrupt, the computer is directed to the memory location specified by the interrupting device and executes the instruction found at that location. The execution of any instruction other than an I/O command can be requested. Normally, the instruction is a jump and mark command and results in the processing of an I/O subroutine. In this event, the interrupt system is automatically inhibited until the inhibit is terminated under program control.

1.3 INTERNAL COMPUTER OPTIONS

Internal options are available to increase the efficiency and versatility of the 620/f computer. These hardware options are available as plug-in units that can be installed in the computer mainframe or in expansion frames.

1.3.1 620/f-5 Memory Protect

The memory protect option provides a means of partitioning core memory whereby the contents of certain memory areas, designated as protected areas, are prevented from being altered by programs operating from areas that are not protected. There are no prerequisites for using the memory protect option.

The memory protect option partitions core memory into equal blocks of 512 words. Each memory protect option can be used to protect up to 32,768 words of core memory. Each 4,096-word block of memory can be divided into eight 512-word blocks. With a maximum 32,768-word memory, there can be a total of sixty-four word blocks.

1.3.2 620/f-10 Multiply/Divide

The multiply/divide option reduces the steps required to perform a multiply or divide subroutine. The types of multiply and divide instructions available are:

a. Single word

b. Double word addressing (preindexing and postindexing)

c. Double word nonaddressing

During multiply, the contents of the B register are multiplied by the contents of the effective memory location. The original contents of the A register do not affect the final product. The product is placed in the A and B registers, with the most significant half in the A register and the least significant half in the B register. The sign of the product is contained in the sign position of the A register. The sign position of the B register is reset to zero. If the contents of the B register and memory contain the largest possible negative number, the result will be zero and the overflow indicator will be set.

During divide, the contents of the A and B registers are divided by the contents of the effective memory location. The quotient is placed in the B register with the sign, and the remainder is placed in the A register with the sign of the dividend.

1.3.3 620/f-13 Real-Time Clock

The RTC provides flexible time orientation that can be used for time-of-day accumulation and as an interval timer. Known periods of time are generated by the RTC for program sequencing.

The main program is periodically interrupted by the RTC to initiate subroutines which accomplish the desired real-time functions. The RTC can generate two types of interrupts: increment and overflow. The first interrupt is a time-base signal that increments a specific memory location when recognized by the computer. The second interrupt occurs when the incremented memory location reaches a count of 040,000. The frequency of the increment interrupt is adjustable and can range from 50 to 10,000 per second. A predelivery factory adjustment sets the RTC to initiate one increment interrupt every millisecond.

1.3.4 620/f-14 Power Failure/Restart

The PF/R provides an orderly shutdown in case of power failure or turnoff and restarts the program when power is restored.

Power input to the computer is indirectly monitored by the PF/R. A power failure monitor voltage in the computer power supply is constantly being sensed to determine power status. If the monitor voltage drops (due to power failure or power switch turnoff), the PF/R causes an interrupt. This interrupt has the highest priority in the system. The central processor then executes a user-programmed service routine that places the contents of volatile registers into memory. The program stops, the memory is disabled, and the system is reset. The power-down service routine cannot be interrupted by lower-priority options or controllers.

When power is restored, the PF/R enables the memory. The CPU executes a user-programmed service routine that restores the contents of the volatile registers, and the system resumes service of the program in progress at the time of the interrupt.

1.3.5 620/f-16 Priority Interrupt Module

The PIM establishes eight levels of interrupt priority for selected peripheral device controllers and stores and processes, in the order of their priority, interrupt requests from these controllers.

The PIM automatically scans the interrupt lines every 900 nanoseconds. If signals occur on more than one interrupt line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored until each has been acknowledged. The PIM permits any or all of the eight interrupt lines to be enabled or disabled.

Acknowledgement of an interrupt by the CPU causes the instruction located at the memory address specified by the PIM to be executed. The instruction may be any of the computer repertoire with the exception of I/O commands. This technique permits an interrupt to be serviced in one instruction period.

1.3.6 620/f-20 Buffer Interlace Controller

The BIC (block transfer supervisor) frees the CPU to perform other functions during block word transfers. The BIC accomplishes this by transferring 16-bit words to and from memory and peripheral controllers connected to the I/O bus. These transfers are made at a maximum rate of 276,000 words per second without the BIC, typical transfer rate is 30,000 words per second.

1.3.7 620/f-15 Automatic Bootstrap Loader

The automatic bootstrap loader is a hardware option that automatically loads the 620/f bootstrap program into core memory from an ROM (integrated circuit). This option saves the time and effort that is involved in manually loading the bootstrap program.

1.3.8 620/f-12 Priority Memory Access

The priority memory access (PMA) provides a capability that allows an external device to have direct access to the 620/f computer memory. A PMA request from an external device preempts use of the memory from the CPU. Except for the PF/R option, a PMA request has the highest priority in the system. To implement the PMA operation, special logic (designed by the user or VDM) is required for interface between the external device and the PMA circuits.

1.3.9 620/f-11 Optional Instruction Set

The 620/f optional instruction set provides the required logic to implement four optional instructions. The four instructions consist of:

a. Transfer switches to A register

b. Jump and set return

c. Bit test

d. Skip if register equal

1.3.9.1 Transfer Switches to A Register

The Transfer Switch to A Register (TSA) instuction transfers the contents of the control console LOAD/ENTRY switches to the A register.

1.3.9.2 Jump and Set Return

The Jump and Set Return (JSR) instruction is a double-word instruction with a jump address in the second word. The instruction stores the contents of the P register in the specified index register (X or B); the next instruction executed is at the jump address.

1.3.9.3 Bit Test

The Bit Test (BT) instruction is a double-word instruction with a jump address in the second word. The instruction tests the condition of a selected bit in the A or B register and jumps if the condition is met.

1.3.9.4 Skip if Register Equal

The Skip if Register Equal (SRE) instruction is a double-word instruction with a skip-out address in the second word. The instruction performs a logical compare between a specified register (A, B, or X) and a memory word specified by the second word. If the result is not equal, the next instruction in sequence is executed. If the result is equal, the next two locations are skipped and the instruction in the third location is executed.

1.4 PHYSICAL CHARACTERISTICS

The basic 620/f computer is contained in a single mainframe chassis which is 10.5 inches high, 21 inches deep, and 19 inches wide. The power supply for the basic computer is contained in a separate chassis, 7.0 inches high, 20 inches deep, and 19 inches wide. For additional I/O capability and memory expansion up to 32K, a memory expansion frame and an I/O expansion frame are available. These expansion frames have the same dimensions as the mainframe.

1.4.1 Mainframe

The mainframe (figure II-2) contains the control console, a CPU tray, a memory tray, and accommmodations for two peripheral controller cards.

The control console contains all of the controls and indicators necessary to operate the computer. The front panel is molded plastic and a printed circuit card mounted behind it holds the lamps and switches. The control console is a swing-away panel hinged to the front of the mainframe. Opening the control console exposes the CPU and memory trays and allows for their removal and installation.

As an added feature, the control console can be located up to 25 feet from the computer mainframe. With a remote control console, the mainframe would contain a blank front panel.

The CPU and memory trays each plug in to three 80-pin connectors mounted on a backplane printed circuit (PC) board in the rear of the mainframe. The CPU tray also connects to a front panel connector that is assembled on the end of a flexible cable. As illustrated in figure II-3, the other side of the backplane PC board contains the external rear panel connectors for the mainframe. These connectors allow the mainframe to be interconnected with memory expansion frame, PMA controller, teletype unit, dc power, and I/O expansion frame.

The CPU tray, as illustrated in figure II-4, contains connectors that accommodate 14 circuit cards. These cards contain all of the circuits for the CPU, I/O control, DMA channel, and teletype controller. The CPU tray circuit cards (figure II-5) are 14.9 inches long and 3.1 inches wide. Each card can accommodate up to 70 integrated circuits and is also used as a printed circuit card for discrete components. The circuit cards contain three card-edge connectors, P1, P2, and P3.

The memory tray, as illustrated in figure II-6, consists of four memory circuit cards approximately 18 inches long and 15.6 inches wide. This configuration depicts an 8K as well as a 4K memory increment. The 8K memory increment requires no more space than a 4K memory increment. When all the memory circuit cards are closed and bolted, the memory tray occupies the same amount of space as the CPU tray.

The two peripheral controller cards are 7.75 inches wide and 12 inches long. These circuit cards (figure II-2) are installed side by side through the rear of the mainframe into two 122-pin connectors.

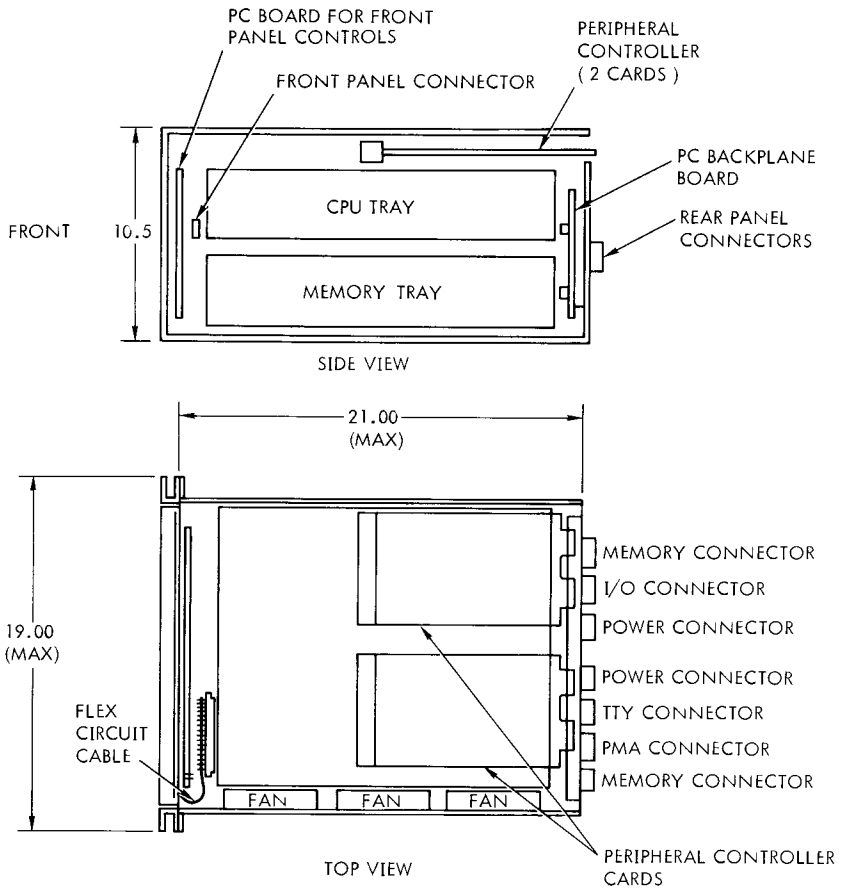

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Figure II-2. Computer Mainframe

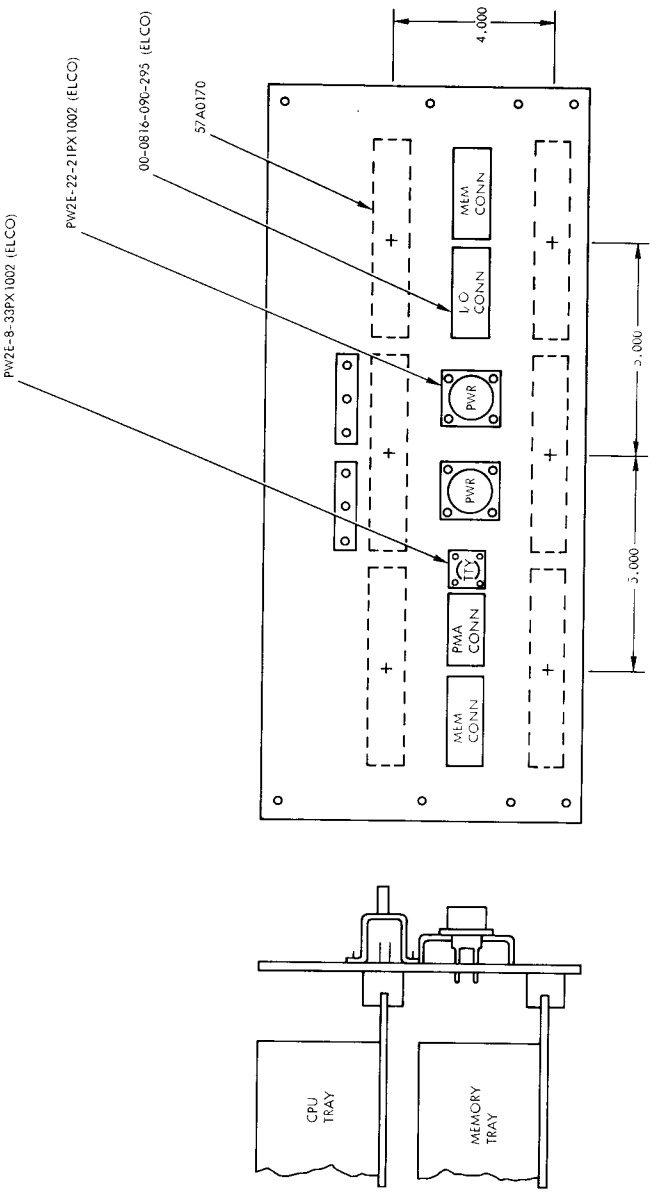

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Figure II-3. Backplane PC Board for Mainframe

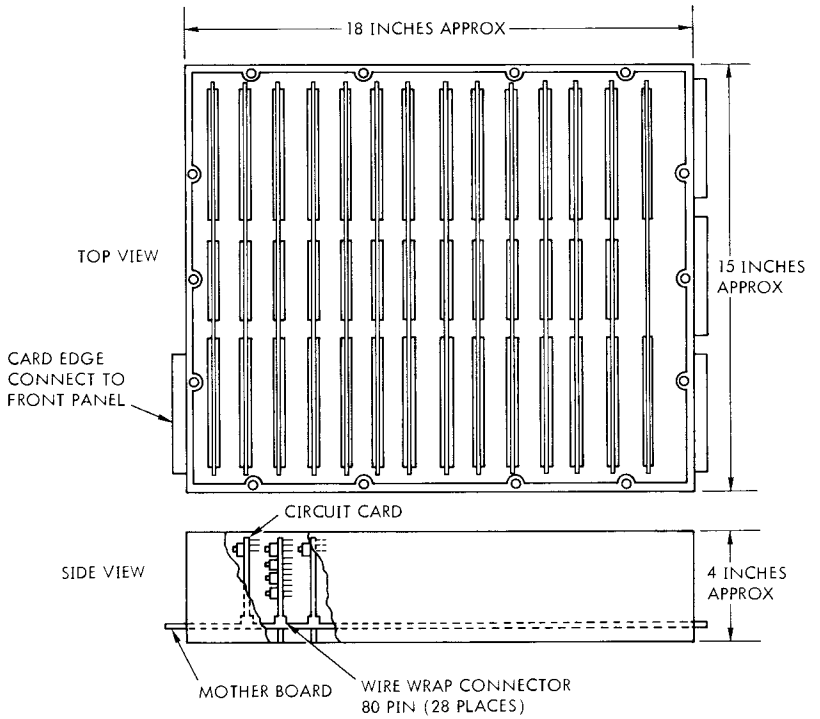

Figure II-4. CPU Tray Layout

1.4.2 Expansion Frames

Expansion frames are available for systems requiring more than 8K of memory or more than two peripheral controller cards. The memory expansion frame (figure II-7) can accommodate the same number of modules as the mainframe. In the memory expansion frame, however, an additional memory tray is installed in place of the CPU tray. The front panel of the memory expansion frame is hinged as in the mainframe. Opening the front panel exposes the two memory trays and allows for removal and

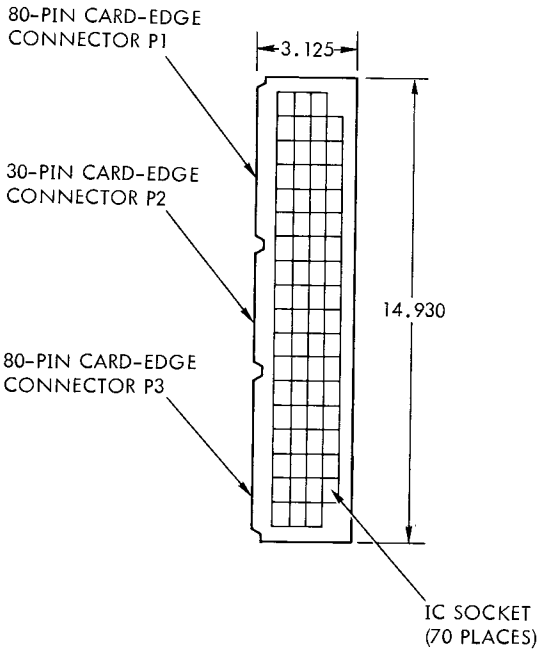

Figure II-5. CPU Tray Circuit Card

installation. A computer system with a mainframe and a memory expansion frame can contain a 24K memory and four peripheral controllers.

The I/O expansion frame (figure II-8) can contain a single memory tray and up to six peripheral controller cards. Memory tray removal and installation is accomplished through the front of the I/O expansion frame when the hinged front panel is opened. The peripheral controller cards are installed through the rear of the I/O expansion frame, and an I/O expansion frame can contain a 32K memory and up to ten peripheral controllers.

A typical system installation showing the expansion capability is illustrated in figure II-9). A power supply is required for the mainframe. The power for the two expansion frames is provided by an additional power supply.

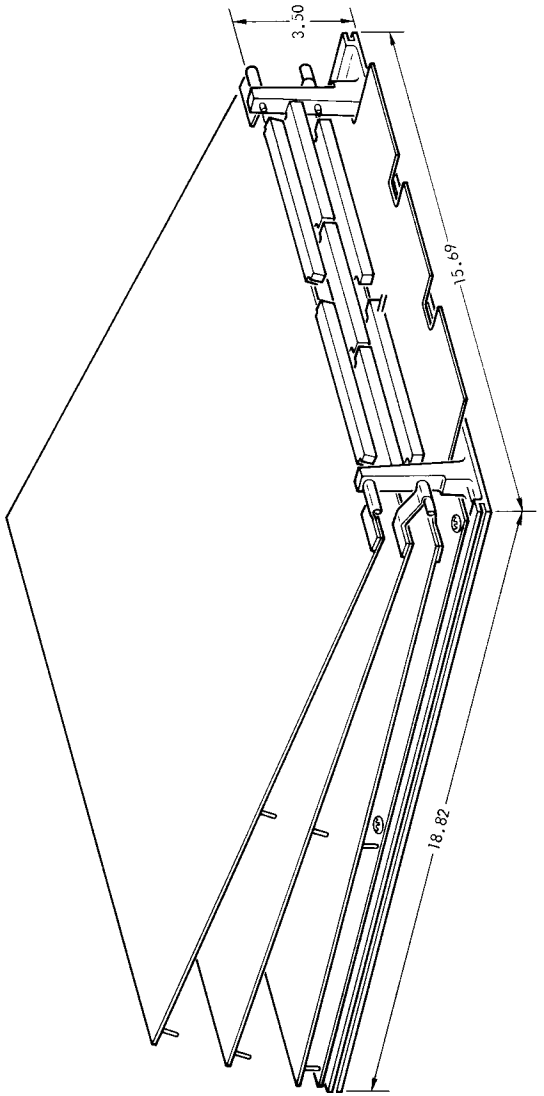

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Figure II-6. Memory Tray

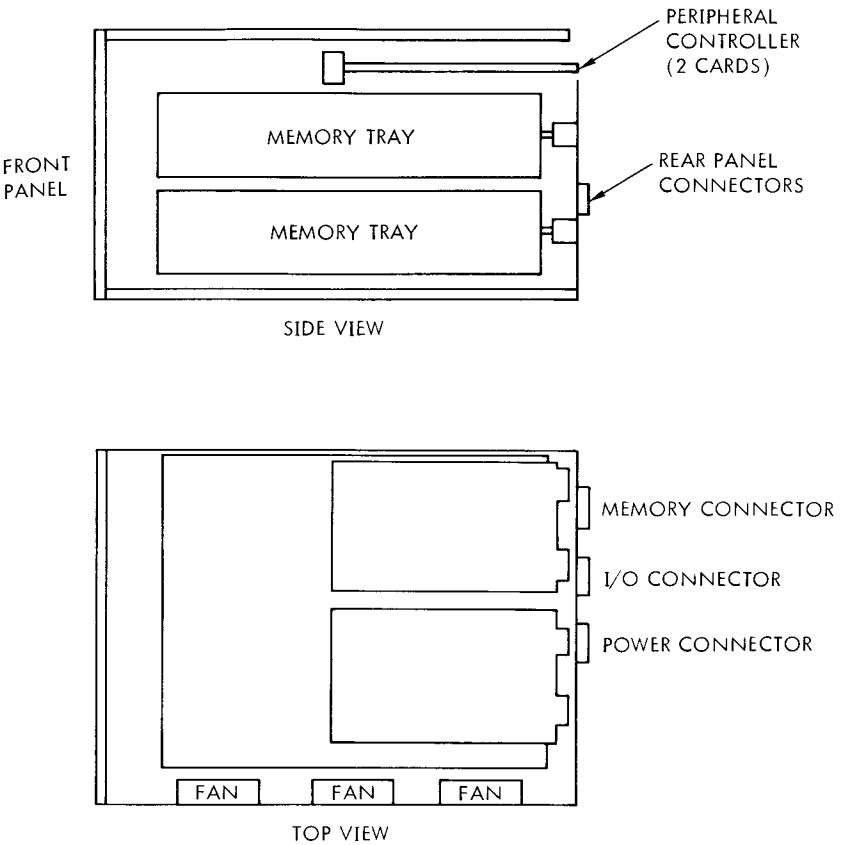

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Figure II-7. Memory Expansion Frame

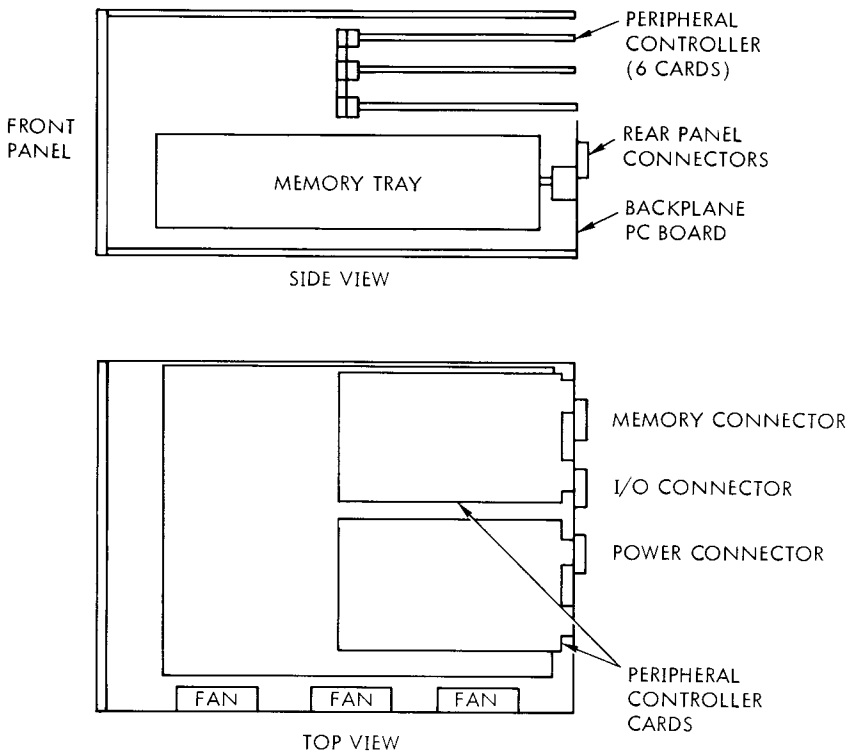

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Figure II-8. I/O Expansion Frame

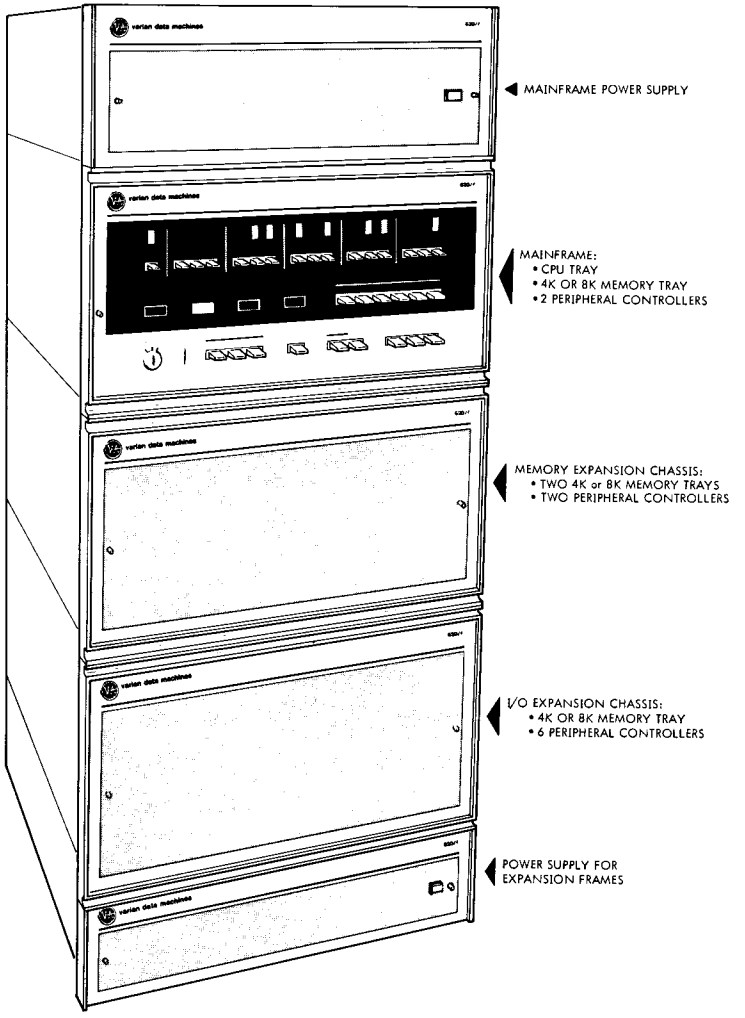

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Figure II-9. Typical System Installation

SECTION 2

SPECIFICATIONS

2.1 COMPUTER SPECIFICATIONS

The specifications for the 620/f computer are listed in table II-1.

Table II-1. 620/f Specifications

Parameter	Description
Type	General-purpose parallel-operation digital computer
Memory (Read/Write)	A 3-wire/3D magnetic core memory with a 16-bit word length, 750-nanosecond full cycle time, 400-nanosecond access time, 4,096-word basic and expandable to 32,768 words in 4,096 increments
Memory	A U-core ROM can be added to the memory system. The total number of words (read/write plus ROM) cannot exceed 32,768. The ROM has a 16-bit word length, addressable core memory. When operating from the ROM, the CPU cycle time is less than 550 nanoseconds
Word Length	Sixteen bits
Machine Cycle Speed	750 nanoseconds
Operations Registers	A register: 16-bit accumulator B register: 16-bit accumulator (least significant half of double-length accumulator) or index register X register: 16-bit index register P register: 15-bit program counter
Auxiliary Registers	I register: 16-bit instruction register L register: 16-bit memory address register R register: 16-bit arithmetic buffer register
Arithmetic	Binary, two's complement notation
Arithmetic Operation Times	Add or subtract: 1.5 microseconds Multiply (optional): Variable, 5.1 microseconds average Divide (optional): 7.0 microseconds Register Change: 750 nanoseconds Input/Output: From A or B register, 1.5 microseconds From memory, 2.25 microseconds
Logic Levels	Positive Logic: (Internal) True = +2.4V minimum, +5V maximum False = -0.5V minimum, +0.5V maximum Negative Logic: (I/O Bus) True = -0.5V minimu, +0.4V maximum False = +2.8V minimum, +3.6V maximum

Addressing Modes:	Direct: to 2,048 words Relative to P register: to 512 words Index with B register hardware: to 32,768 words (does not add to execution time) Multilevel indirect: to 32,768 words Immediate Extended: to 32,768 words
Instructions	148 instructions
Instruction Types	Single-word, addressing Single-word, nonaddressing Double-word, addressing Double-word, nonaddressing
I/O Instruction Types	Program control: Data transfer in: single-word, addressing single-word, nonaddressing double-word, addressing double-word, nonaddressing Data transfer out: single-word, addressing single-word, nonaddressing double-word, addressing double-word, nonaddressing External control: single-word, nonaddressing Program sense: double-word, addressing
Computer Options	Memory protect Buffered interlace controller (BIC) Power failure/restart (PF/R) Real-time clock (RTC) Automatic bootstrap loader (ABL) Priority interrupt module (PIM)

High-speed priority memory access (PMA)
Hardware multiply/divide (M/D)
Bit test (BT)
Transfer switches (TSA)
Skip if register equal (SRE)
Jump and set return (JSR)

Software DAS symbolic assembler operating in the basic 4,096-word memory. Includes 17 basic pseudo-operations. The 8,192-word memory version includes over 30 pseudo-operations

FORTRAN:
Modular one-pass compiler; subset of ASA FORTRAN for 8,192-word memory

AID:
Program analysis package that assists programmers in operating the machine and debugging other programs. Includes basic operational executive subroutines

MAINTAIN:
Modular, two-mode diagnostic package that provides fast verification of CPU and peripheral operation and assists in isolating and correcting suspected faults

Subroutines:
Complete library of basic mathematical, fixed- and floating-point, single- and double-precision, number conversion and peripheral communication subroutines plus provisions for adding application-oriented routines

Dimensions	The mainframe and expansion frames are 10-1/2 inches high, 19 inches wide, and 21 inches deep
Input Voltage	105 to 125V ac or 210 to 250V ac at 50 or 60 Hz*
Input Current	The mainframe power supply requires approximately 15 amperes ac; each expansion frame power supply requires approximately 4 amperes ac.
Temperature	
Operating	0 to 50 degrees C
Storage	-20 to 70 degrees C
Humidity	
Operating	To 90 percent without condensation
Storage	To 95 percent without condensation
Vibration	3 to 10 Hz at 1g force or 0.25 double amplitude, whichever is less. Exponentially raised frequency from 3 to 10 Hz and back to 3 Hz over a 10-minute period, three complete cycles. This specification applies for all three principal axes
Shock	4g for 11 milliseconds (all three principal axes)

* Teletype frequency must be either 50 or 60 + 1/2 - 0 Hz.

2.2 SPECIFICATIONS FOR INTERNAL COMPUTER OPTIONS

The specifications for internal computer options are listed in tables II-2 through II-7.

Table II-2. 620/f-5 Memory Protect Specifications

Parameter	Description
Organization	Consists of command decode logic, mask register selection logic, address decode logic, four 16-bit mask registers, address comparator logic, and instruction decode and error detection logic
Control Capability	Up to sixty-four 512-word memory blocks (32,768 words)
Logic Levels	Positive logic: True equals +2.5 to +5.0V dc False equals 0.0 to +0.5V dc
Input Power	+5V dc, at 725 mA

Table II-3. 620/f-10 Multiply/Divide Specifications

Parameter	Description
Organization	Contains multiply/divide and shift control logic, and extended address control logic

Parameter	Description
Multiply Algorithm	A + B (B • R) = A,B where A = initial A register content B = multiplier (in B register) R = multiplicand (in memory) A,B = product (in A and B registers; most significant half in A, least significant half in B)
Multiplication Capability	Maximum multiplier 32,767 or -32,768 Maximum multiplicand 32,767 or -32,768 Maximum product 1,073,741,824
Divide Algorithm	(A,B)/R = B + A where A,B = dividend (in A and B registers; most significant half in A, least significant half in B) R = divisor (in memory) B = quotient (in B register) A = remainder (in A register)
Division Capability	Maximum divisor 32,767 or -32,768 Maximum dividend 1,073,741,824 Maximum quotient 32,767 or -32,768
Extended Addressing Modes	Relative to P (contents of second word plus P register plus 1) Indexed with X (contents of second word plus X register)

Parameter	Description
	Indexed with B (contents of second word plus B register) Direct (second word is direct address if bit 15 is zero) Indirect (second word is indirect address if bit 15 is one)
Logic Levels	Positive logic: True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Size	One 7-3/4-by-12-inch etched-circuit
Input Power	+5V dc, at 320 mA

Table II-4. 620/f-13 Real-Time Clock Specifications

Parameter	Description
Organization	Contains input line receivers, an address decoder, time-base oscillator, pulse counter, overflow detector, interrupt register, interrupt controller, output line drivers, and external time-base input
Interrupt Priority	Normally second only to the PF/R (if any), but determined by order of placement in the system priority wiring string
I/O Capability	Four external control (EXC) conmands
Type of Interrupt	Incrementation and overflow
Device Address	RTC 047

Parameter	Description
Interrupt Memory Addresses	Incrementation: 044 and 045 Overflow: 046 and 047
Internal Time-Base	Range: 400 Hz to 80 kHz, preselectable (50 to 10,000 incrementation interrupts per second) Output: Rectangular pulses, 0 to +5V dc, 40 to 60 percent duty cycle
Logic Levels:	Negative logic: True: 0.0 to +0.5V dc False: +2.8 to +3.6V dc Positive logic: True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Input Power	+5V dc; +12V dc 480 mA

Table II-5. 620/f-14 Power Failure/Restart Specifications

Parameter	Description
Organization	Consists of a system power monitor (voltage threshold detector), a power-up delay circuit, a power status circuit, and a sequencer for the CPU and memory
Interrupt Priority	Highest level in the system
Power-Down Timing	Less than 1 millisecond after power failure or turnoff detection
Power-Up Timing	Less than 1.1 second after the return of full power

Parameter	Description
Interrupt-Memory Addresses	Power-down: 040 and 041 Power-up: 042 and 043
Sensed Voltage	Approximately +15V dc for normal ac input to the computer
Threshold Voltage Range	Normal ac input 10 percent
Logic Levels To the I/O bus	Negative logic: True: 0.0 to +0.5V dc False: +2.8 to +3.6V dc
To the CPU and Memory	Positive logic: True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Input Power	+5V dc; +12V dc; -12V dc at 350 mA 350 mA

Table II-6. 620/f-16 Priority Interrupt Specifications

Parameter	Description
Organization	Contains three 8-bit registers (line, sync, and mask), an interrupt address generator, priority control logic, and necessary input receivers and output drivers
Interrupt Control Capability	Eight priority levels, user-assignable

Parameter	Description
I/O Capability	Five EXC commands Three transfer commands
Type of Interrupt	High-to-low level transition
Interrupt Line Scan Rate	Once each 900 nanoseconds
Device Address	PIM 040 to 044 User-assignable
Memory Locations Required	Two per connected peripheral device controller, consecutive pairs, 16 total
Interrupt Address Location	May be anywhere in first 128 memory locations. (Except for locations 040 through 047 which are reserved for the PF/R, PIM, and real time clock (RTC) options.)
Priority of PIM	Determined by placement in the priority chain, user-assignable
Priority of Peripheral Device Controllers	Eight levels, determined by hard-wired connection to interrupt cable, user-assignable
Logic Levels	
I/O Cable	Negative logic: True: 0.0 to +0.45V dc False: +2.8 to +3.6V dc
Interrupt Cable	Negative logic: True: 0.0 to 0.5V dc False: +2.5 to +5.0V dc
Internal	Positive logic: True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc

Parameter	Description
Size	One 7-3/4-inch-by-12-inch etched-circuit card
Input Power	+5V dc at 500 mA
Operational Environment	5 to 45 degrees C, 10 to 90 percent relative humidity without condensation

Table II-7. 620/f-20 Buffer Interlace Controller Specifications

Parameter	Description
Organization	Contains input receivers and output drivers, two 15-bit address registers and a sequence control circuit
Control Capability	Up to ten device controllers
I/O Capability	Two external control commands Eleven transfer commands Two sense commands
I/O Transfer Rate	Synchronized to peripheral device rate; maximum 202,000 words per second
I/O Signal Limits (Rise/Fall)	Minimum 10 nanoseconds; maximum 100 nanoseconds
Logic Levels	
To the I/O Bus	Negative logic: True: 0.0 to +0.5V dc False: +2.8 to +3.6V dc
Internal	Positive logic: True: +2.4 to +5.5V dc

Parameter	Description
	False: 0.0 to 0.5V dc
Size	One 7-3/4-inch-by-12-inch etched-circuit card
Connectors	Two 44-terminal card-edge connectors One 122-terminal card-edge connector
Input Power	+5V dc at 630 mA
Operational Environment	5 to 45 degrees C, 10 to 90 percent relative humidity without condensation

SECTION 3

SYSTEM PLANNING

3.1 INTRODUCTION

The 620/f computer is packaged to provide the user maximum convenience, flexibility, and space-saving economies. The computer mainframe, expansion frames, and power supplies are contained in individual cabinets suitable for rack-mounted or table-top installation.

3.2 SPACE REQUIREMENTS

The CPU with various internal computer options, 8K of memory, and two peripheral controllers can be housed entirely in the computer mainframe which is 10.5 inches high, 21 inches deep, and 19 inches wide. The mainframe power supply is contained in a separate chassis which is 7 inches high, 20 inches deep, and 19 inches wide. The standard 33 ASR teletype unit with a stand is approximately 33 inches high, 19 inches deep, and 22 inches wide.

16K of memory and two peripheral controllers can be added with a memory expansion frame. The memory expansion frame is the same size as the computer mainframe. Power is provided by an expansion frame power supply which is contained in a separate chassis 5.25 inches high, 20 inches deep, and 19 inches wide.

8K of memory and six peripheral controllers can be added with an I/O expansion frame, which is also the same size as the mainframe. The I/O expansion frame shares a single power supply with the memory expansion frame. The two expansion frames allow the computer system to contain 32K of memory and ten peripheral controller cards.

3.3 ENVIRONMENTAL AND POWER REQUIREMENTS

Ambient temperature at the installation site can vary between 32 and 122 degrees F with no adverse affects on computer operations. To extend the life expectancy of the computer, however, it is recommended that ambient temperature be maintained between 55 and 85 degrees F. The humidity can be up to 90 percent as long as there is no condensation.

The computer power supplies connect to a standard 115-volt, single-phase, ac power source. Also available, for European installations, are power supplies that operate on 220 volts ac. Power regulation is not required under normal commercial power conditions. The mainframe power supply draws approximately 15 amperes, and the expansion power supply, approxiately 4 amperes.

3.4 SYSTEM INTERCONNECTION

System interconnection is accomplished with cables that mate with connectors at the rear of the mainframe and expansion frames. The types of interconnecting cables and their functions are:

a. Memory Expansion. These cables route memory signals between the mainframe and the expansion frames. The maximum cable length between master memories is 10 feet. The total cable length for a master/slave arrangement must not exceed 3 feet.

b. I/O Expansion. These cables have a maximum length of 15 feet and route I/O signals between the mainframe and the expansion frames.

c. Power. These cables have a maximum length of 20 feet and route +41, +12, 5, and -32 volts from the power supplies to the mainframe and expansion frames.

d. Teletype. This cable has a maximum length of 20 feet and connects a teletype unit to the mainframe.

e. PMA. This is a special-purpose cable that connects the optional PMA circuits in the mainframe to external device interface logic. This cable is normally provided by the user.

The computer frames can be placed side by side, back to back, or rack-mounted in a standard RETMA enclosure. The relative position of each computer frame is not restricted; for example, the mainframe does not have to be installed immediately adjacent to the memory expansion frame. The computer frames are interconnected with 10-foot memory expansion cables and 15-foot I/O expansion cables. The maximum distance between the computer frames, therefore, must not exceed the distance required by the interconnecting cables. Figure II-10 illustrates interconnection of a typical system containing a mainframe, memory expansion frame, teletype unit, and a magnetic tape transport.

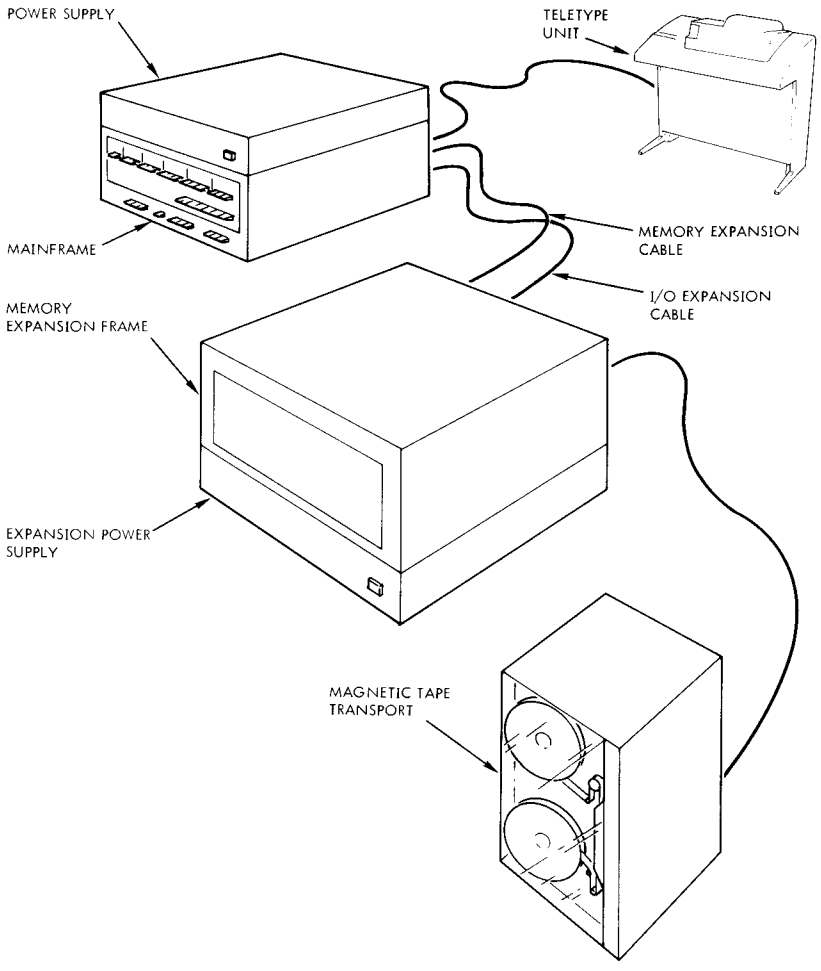

Figure II-10. Typical 620/f System Interconnection

SECTION 1

INPUT/OUTPUT SYSTEM

1.1 INTRODUCTION

The 620/f input/output (I/O) system allows the computer to interface with a large variety of peripheral devices. Interface circuitry to run a specific peripheral device is contained on one or more controller cards that plug into any peripheral controller slot in the mainframe or expansion frames. A controller can control one or more similar peripheral devices. Each controller and the device it controls comprise a peripheral device option. Up to ten peripheral controller cards can be installed in the computer system. All controller cards have the same standard I/O pin assignments, and the mating I/O connectors in the computer are wired uniformly. The controller cards are powered from the computer power supply; all peripheral devices draw their power from the ac power line.

This section describes the I/O system organization, interface signals, and cable characteristics. For I/O word format and coding information, refer to the 620/f programming reference manual.

1.2 ORGANIZATION

The I/O system utilizes a bidirectional I/O bus structure which allows a single set of data and control lines to communicate with all peripheral devices. The I/O bus contains line drivers and line receivers to service up to ten peripheral devices. No additional connections to the computer are required when a new device is added. A block diagram of an I/O system containing the priority memory access (PMA), buffer interlace controller (BIC), and priority interrupt module (PIM) options is illustrated in figure III-1.

Information transfers can occur under the control of a stored program or under external control through the use of the direct memory access (DMA) feature. The standard I/O system provides six types of I/O operation:

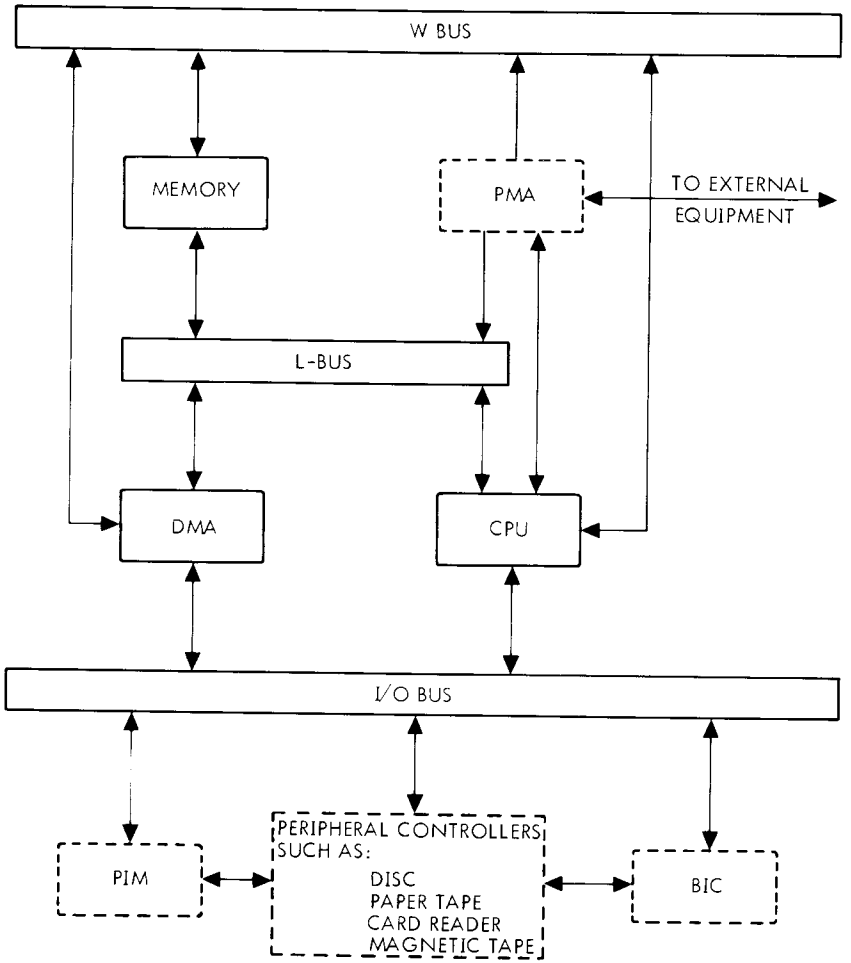

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Figure III-1. I/O System Organization

a. External Control. An external control code is transmitted under program control from the computer to a peripheral controller.

b. Program Sense. The status of a selected peripheral controller sense line is interrogated by the computer under program control.

c. Input Data Transfer. Data are transferred under program control from a peripheral controller to the A register, B register, or any location in memory.

d. Output Data Transfer. Data are transferred under program control to a peripheral controller from the A register, B register, or any location in memory.

e. Direct Memory Access. The DMA feature, in conjunction with a BIC, allows automatic data transfers between peripheral devices and memory without CPU intervention.

f. I/O Interrupt. An external source can activate an I/O interrupt to cause the CPU to execute a single instruction found in an externally indicated memory location. These I/O interrupts normally occur through a PIM.

The I/O system can communicate directly with all peripheral device options under program control. The computer can initiate operation of a peripheral device by transmitting an external control code and a proper device address to the selected controller via the I/O bus. The computer can determine when a device is ready to send or receive information by interrogating its associated sense line. A device can be requested to place a word of data on the I/O bus during a computer input transfer or to accept a word of data placed on the bus by the computer during an output transfer.

1.3 INTERFACE SIGNALS

The I/O interface signals provide communication between the I/O system and peripheral devices. The I/O interface signals are divided into two classes:

a. Signals used during program controlled I/O bus operations

b. Signals used during DMA and I/O interrupt operations

1.3.1 Program Controlled I/O Bus Operation

The I/O interface signals used during program controlled I/O bus operations consist of E bus signals and five I/O control signals.

a. E Bus (EB00-I through EB15-I). The E bus is a 16-bit parallel, bidirectional I/O channel used to transmit control codes, device addresses, and data from the computer to the peripheral devices . In turn, the bus is used by these devices to transmit data to the computer. Ten drivers and ten receivers can be connected to each line. An E bus signal is logically true when it is at 0V dc and logically false at +3V dc.

b. Function Ready (FRYX-I). FRYX-I is generated by the computer to indicate that it has placed a device address and a control code on the E bus. Each peripheral controller examines the device address, and, upon the true-to-false transition of FRYX-I, the addressed device responds to the control code. FRYX-I is logically true at 0V dc and logically false at +3V dc. Ten receivers may be connected to the line.

c. Data Ready (DRYX-I). DRYX-I is generated by the computer. During an output data transfer, DRYX-I indicates that the computer has placed data on the E bus and that the previously addressed peripheral device should strobe the data into its input buffer. During an input data transfer, DRYX-I indicates that the computer has accepted the data placed on the E bus by the peripheral device and that, following the true-to-false transition of DRYX-I, the device should remove the data. DRYX-I is logically true at 0V dc and logically false at +3V dc. Ten receivers can be connected to the line.

d. Sense Response (SERX-I). During the execution of a program Sense (SEN) command, the computer places a function code and a device address on the E bus. The addressed controller is instructed to indicate the status of the specific device condition that is identified by the function code.

If the specified condition is true, the controller responds by setting the SERX-I line true. If the condition is false, SERX-I is left false. SERX-I is logically true at 0V dc and logically false at +3V dc. Ten drivers can be connected to the line.

e. Interrupt Acknowledge (IUAX-I). IUAX-I is generated by the computer to ack on wledge that either a DMA or interrupt operation is in progress. Each

peripheral device controller uses IUAX-I to inhibit normal device decoding. During a program- controlled I/O operation, IUAX-I is held false (+3V dc). Ten receivers can be connected to the line.

f. System Reset (SYRT-I). SYRT-I is used to initialize each peripheral device controller connected to the I/O bus. SYRT-I becomes true when the SYSTEM RESET switch on the control console is pressed. SYRT-I is logically true at 0V dc and logically false at +3V dc. Ten receivers can be connected to the line.

1.3.2 DMA and I/O Interrupt Operations

The I/O interface signals used during DMA and I/O interrupt operations consist of the signals described in section 1.3.1 plus six additional control signals. The six control signals are logically true at 0V dc and logically false at +3V dc. Ten receivers or drivers can be connected to each control line. The six control lines are:

a. Interrupt Acknowledge (IUAX-I). This control signal is set true by the computer to acknowledge that an interrupt or a trap-in or trap-out operation is in process. The interrupting trapping device controller can communicate an address to the computer and can receive data from or send data to the computer only when this control signal is true. IUAX-I is also used to inhibit device address decoding in every device controller during the address phase of an interrupt or DMA operation. This prevents the controllers from interpreting the lower-order bits of a memory address as a device address.

b. Interrupt Request (IURX-I). By setting IURX-I true, the interrupting device controller requests the computer to execute an instruction. The address of this instruction is placed on the E bus by the interrupting device on receipt of IUAX-I from the computer. IUAX-I should be removed following IUAX-I of the interrupt cycle.

c. Trap-Out Request (TPOX-I). By setting TPOX-I true, the trapping device controller (normally th BIC) requests the computer to output one word of data from memory. The address of this word is placed on the E bus by the controller on receipt of IUAX-I from the computer. TPOX-I should be removed following DRYX-I of the trap cycle.

d. Trap-In Request (TPIX-I). By setting TPIX-I true, the trapping device

controller (normally the BIC) requests the computer to input one word of data to memory. The address of this word is placed on the E bus by the controller on receipt of IUAX-I from the computer. TPIX-I should be removed following DRYX-I of the trap cycle.

e. Interrupt Clock (IUCX-I). This control signal from the computer is a 1.1-MHz clock that is disabled by IUAX-I. When IUAX-I is false, the clock is present on the IUCX-I line. When IUAX-I is true, IUCX-I is held true. The true-to-false transition of IUCX-I sets the request flip-flops (IURX-I, TPOX-I, and TPIX-I) in respective controllers.

f. Interrupt Jump (IUJX-I). This control signal from the computer inhibits all interrupts that occur after a jump and mark instruction when that instruction is the result of an interrupt request. This signal becomes true 2.7 microseconds from the false- to-true transition of IUAX-I and remains true for 450 nanoseconds.

Table III-1 summarizes how the E bus signals and control signals are used to determine what is being transferred on the I/O bus during I/O operation .

1.4 I/O CABLE CHARACTERISTICS

The I/O cable routes the E bus and control signals between the computer mainframe and expansion frames. The I/O cable contains twisted pairs of 24-gage wires. The computer, as well as each peripheral controller, contains a cable driver and receiver for each I/O bus line. A typical E bus interconnection is illustrated in figure III-2. Communication on the bidirectional E bus is such that information is transferred from the computer cable driver to a peripheral controller cable receiver or from a controller driver to the computer receiver. Communication between controllers does not occur on the E bus. Each bus line is terminated by 150 ohms to +3V dc at the computer and in a termination shoe at the opposite end of the I/O cable. Ferromagnetic beads (part number 01C0266) eliminate ringing of the rise and fall transitions of the E bus signals. Three beads must be placed in the vicinity of the signal driver to ensure satisfactory signal control; consequently, beads are placed on the driver outputs as shown in figure III-2.

Typical I/O control line interconnections are illustrated in figures III-3 and III-4. The

Table III-1. I/O Bus Signals

OPERATION CONTROL LINE E-BUS BIT LINE	External Control	Sense	Program-Controlled Data Transfer		DMA Data Transfer*		Interrupt Sequence	
EB00-I	FRYX-I**	FRYX-I** SERX-I**	FRYX-I** (Phase 1)	DRYX-I (Phase 2)	IUAX-I (Phase 1)	IUAX-I (Phase 2)	IUAX-I IURX-I	Pairs of signals used for specific interrupts
EB01-I								
EB02-I	Device address	Device address	Device address					
EB03-I								
EB04-I								
IB05-I								
EB06-I								
EB07-I	Function code	Line	Not used					

Table III-1. I/O Bus Signals (continued)

OPERATION	External Control	Sense	Program-Controlled Data Transfer		DMA Data Transfer*		Interrupt Sequence
CONTROL LINE							
E-BUS BIT LINE	FRYX-I**	FRYX-I** SERX-I**	FRYX-I** (Phase 1)	DRYX-I (Phase 2)	IUAX-I (Phase 1)	IUAX-I (Phase 2)	IUAX-I IURX-I
EB08-I				Data	Address	Data	
EB09-I	Not used	Not used					
EB10-I							
EB11-I	External control command	Zero					
EB12-I		Sense Command	Zeros				
EB13-I	Zeros		Data Transfer In				
EB14-I		Zeros	Data Transfer Out				

Table III-1. I/O Bus Signals (continued)

OPERATION	External Control	Sense	Program-Controlled Data Transfer		DMA Data Transfer*		Interrupt Sequence
CONTROL LINE							
E-BUS BIT LINE	FRYX-I**	FRYX-I** SERX-I**	FRYX-I** (Phase 1)	DRYX-I (Phase 2)	IUAX-I (Phase 1)	IUAX-I (Phase 2)	IUAX-I IURX-I
EB15-I	Extended external		Zero				

* Plus TPOX-I or TPIX-I. Requires BIC option.
** IUAX interlock used in address decoding.

configuration of the cable drivers and receivers is the same as for the E bus lines except they are unidirectional.

1.4.1 I/O Cable Driver

The I/O cable driver is a four-input NAND gate, which has been selected so that the saturated common-emitter output stage is capable of conducting up to 70 milliamperes without exceeding a saturation voltage of 0.5V dc. This driver can be collector-tied with another driver to produce a negative-logic-OR function. The driver circuit schematic is shown in figure III-5.

1.4.2 I/O Cable Receiver

The I/O cable receiver is a two-input NAND gate; the schematic is shown in figure III-6. The receiver input represents a maximum load (current source) of 1.4 milliamperes at 0V dc. The receiver input switching threshold is 1.5 0.5V dc.

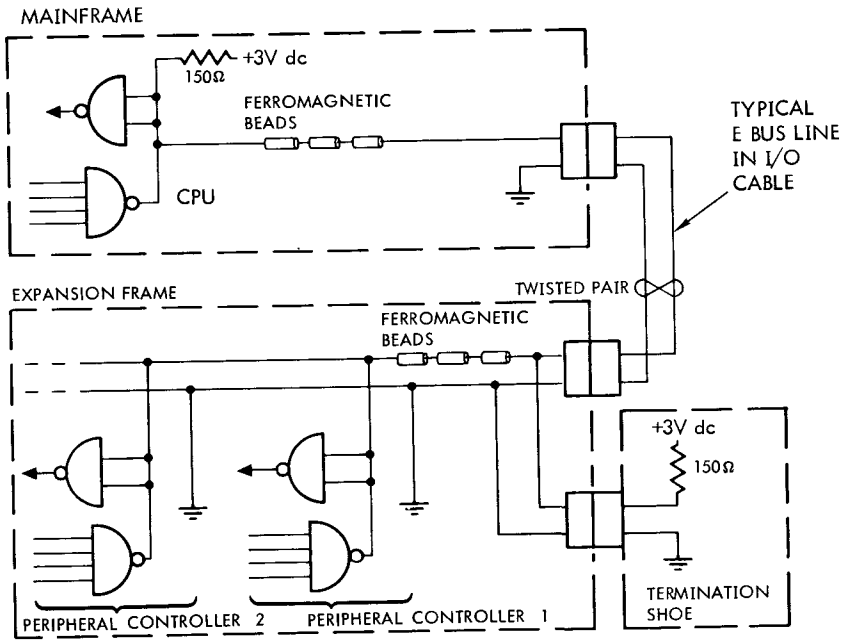

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Figure III-2. Typical E Bus Line Interconnection

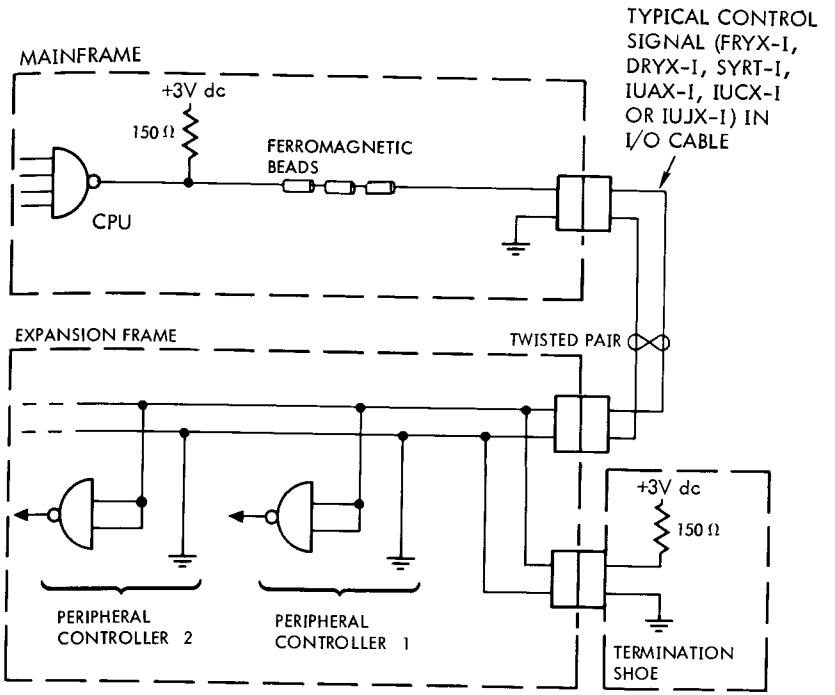

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Figure III-3. Typical Control Signal Interconnection from CPU to Controllers

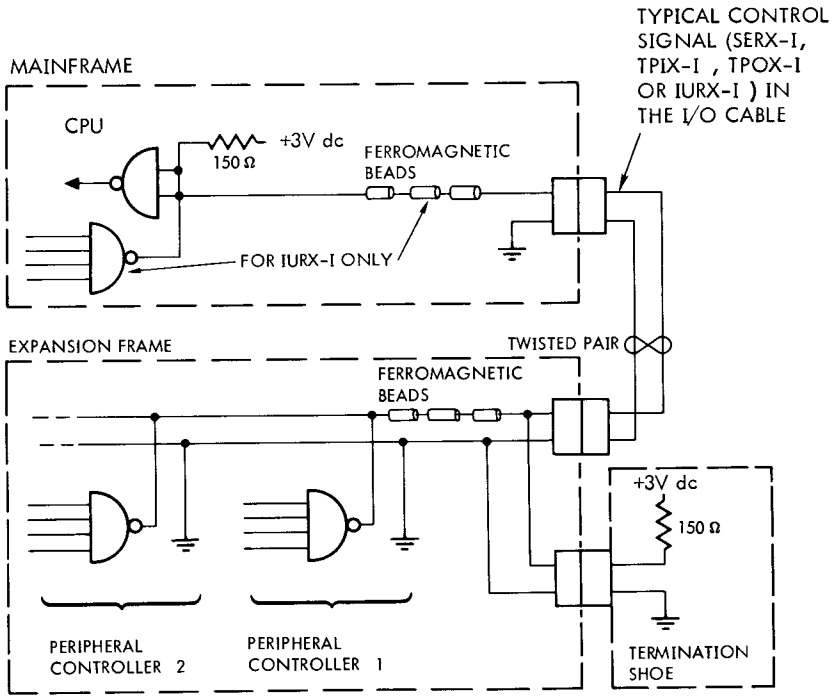

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Figure III-4. Typical Control Signal Interconnection to CPU from Controllers

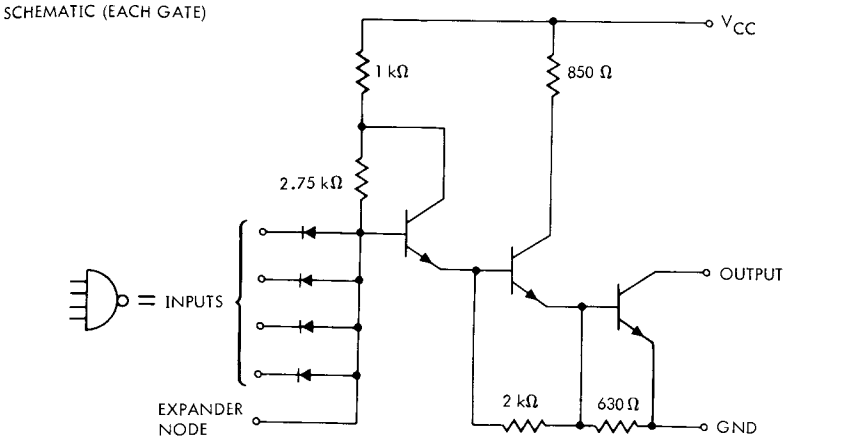

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Figure III-5. I/O Cable Driver

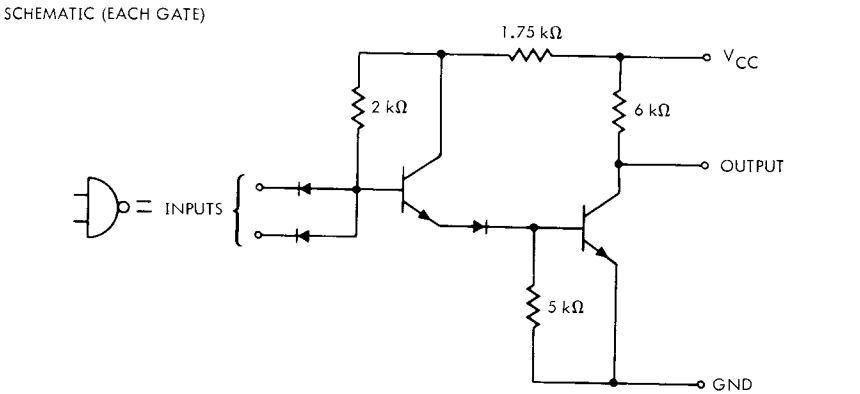

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Figure III-6. I/O Cable Receiver

SECTION 2

PERIPHERALS

2.1 INTRODUCTION

This section describes a sampling of various peripheral options that are available with the 620/f computer. A brief description followed by a list of specifications is provided for each peripheral. The 620/f computer is I/O-compatible with the Varian Data Machines 620/i computer. For this reason (with the exception of the first teletype controller), the peripheral controllers described in this section are the 620/i type. The circuits of the 620/i peripheral controllers are contained on 7-3/4-by-12-inch circuit cards that can be installed in any peripheral controller slots in the 620/f mainframe or expansion frames.

2.2 TELETYPE CONTROLLER

The teletype controller controls the command and information transfer between the computer and one factory-modified teletype unit. The first teletype controller is a standard feature controlled directly by the CPU, and is located in the CPU tray on a single 3-by-15- inch circuit card. Any additional teletype controllers are optional features and are installed in any peripheral controller slots of the mainframe and expansion frames. Each optional teletype controller is contained on a single 7-3/4-by-12-inch circuit card.

The optional teletype controllers can be controlled through the I/O bus or through the buffer interlace controller (BIC). Up to eight teletype units and controllers can be installed in a computer system. One teletype buffer board is required for teletype units and controllers 2 through 8 to be indirectly controlled by the CPU through the I/O bus. If the BIC option is installed, the CPU is free to perform other program functions during data transfers.

The factory-modified teletype unit that is controlled by the teletype controller can be a model 33 ASR, 35 ASR, or 35 KSR. The ASR models have automatic send and receive facilities; the KSR model uses only keyboard-entered instructions and data.

The specifications of the optional teletype controllers are listed in table III-2.

2.3 620/i-22 AND -23 CARD READER SYSTEM CONTROLLER

The model 620/i-22 and 620/i-23 card reader systems (CRS) are peripheral options that read data from 80-column (51-column optional) punched cards and transfer the data to a 620/f computer. The CRS consists of either a Soroban model ERD (620/i-22) SCCR (620/i-23) card reader and a card reader controller.

The controller is constructed with 28 integrated circuit chips and four discrete component assemblies mounted on a standard wired- socket card. The card may be mounted in any peripheral controller slot of an expansion chassis. The interface cable between the controller and the card reader consists of 18 twisted-pair wires. The cable connects to the controller card with one card-edge cable connector. The reader is normally placed on a table top.

The card reader reads the information from punched cards and provides the data to the controller. The card reader controller provides a nonbuffered interface between the card reader and the CPU. It also provides the timing and logic circuits to effect the transfers. The controller can transfer data to the CPU under direct program control or under supervision of a BIC.

The specifications of the controller are listed in table III-3.

2.4 9-TRACK MAG TAPE SYSTEM CONTROLLER

The nine-track magnetic tape system consists of up to four Peripheral Equipment Corporation Series 6000 (620/i-30) tape transports and one 620/i-30 magnetic tape controller (MTC) for processing IBM 2400-compatible tapes.

The MTC provides a buffered interface between the 620/f I/O bus and the tape transport. The MTC accommodates up to four tape transports, but only one of these is in use at any given time.

The MTC is on two wire-wrapped socket cards which can be installed in an expansion chassis. It contains all read/write registers and logic circuitry for the tape transport control.

Table III-2. Teletype Controller Specifications

Parameter	Description
Organization	Contains input and output registers, timing control circuitry for simultaneous two-way transmission, and processor/teletype interface logic.
Peripheral Device	A factory-modified teletype model 33 ASR, 35 ASR, or 35 KSR including cable.
Speed	Operation is controlled by teletype speed. Ten characters per second (or 100 milliseconds per character) at either random or sustained rate.
Modes	Input: from keyboard or paper tape. Output: to typewriter or paper tape.
Device Address	TC 001
Sense Responses	Ready to read. Ready to write.
Memory Access Control	By central processor indirectly. (requires teletype buffer board 01A0688-000). By BIC.
Types of Interrupt	Write ready and read ready interrupts available to a priority interrupt module (PIM).
Logic Levels	Positive logic True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc

Table III-2. Teletype Controller Specifications (continued)

Parameter	Description
Input Power	+5V dc, 440 mA.
Operational Environment	+10 to +45 degrees C, 10 percent to 90 percent relative humidity without condensation.

Computer control of the magnetic tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

If the system contains more than one tape transport, the transports are connected to the MTC in party-line configuration. The program controls the selection of the one transport that can operate at any given time.

The specifications of the controller are listed in table III-4.

2.5 7-TRACK MAG TAPE SYSTEM CONTROLLER

The seven-track magnetic tape system consists of up to four magnetic tape transports and a magnetic tape controller. The system can read and record a magnetic tape that is IBM 2400-compatible for seven- track systems.

The magnetic tape controller provides a buffered interface between the 620/f I/O bus and a seven-track magnetic tape transport. The controller accommodates up to four

Table III-3. 620/i-22 and -23 Card Reader System Controller Specifications

Parameter	Description
Organization	Contains input receivers and output drivers for I/O bus and BIC interface operations. Contains sequence control logic to transfer data from the card reader to the computer.
Capabilities	Provides control of a single card reader Soroban model SCCR (602/i-23) or ERD (620/i-22).
Operating speeds	With SCCR: 600 per minute. With ERD: 1100 cards per minute. Character length: 12 bits, LSB DI00, MSB DI11. Feed type: Both card readers read standard 80-column cards (51 optional) on a per column basis (end feed). Transfer rate: Maximum transfer rate between 620/f computer and controller is 1,420 characters-per-second for the 620/i-23 and 2,500 characters-per-second for the 620/i-22. 620/f read limits: Data input transfer must be performed after the leading edge of the character-ready sense bit within 475 microseconds for the 620/i-23 and within 325 microseconds for the 620/i-22.
Logic levels	Positive logic True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Size	One 7-3/4-by-12-inch etched-circuit card.

Table III-3. 620/i-22 and -23 Card Reader System Controller Specifications (continued)

Parameter	Description
Interconnection	Interfaces with the computer and BIC via a 122-terminal connector. Interfaces with card reader via two 44-terminal connectors.
Input power	+5V dc, 280 mA
Operational Environment	+5 to +45 degrees C; to 90 percent relative humidity without condensation.

transports of the Peripheral Equipment Corporation 6000 series. However, only one tape transport can be selected for use at any one time.

The tape controller comprises two circuit cards and contains all read/write data registers and timing and control logic required to control one tape transport.

Computer control of the magnetic tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

When more than one tape transport is used with the controller, the transports are connected to the controller in party-line configuration. However, only one transport may be operated at a time. Transport selection is program-controllable.

The specifications of the controller are listed in table III-5.

Table III-4. 620/i-30 Magnetic Tape System Controller Specifications

Parameter	Description
Organization	Consists of a clock, drivers, receivers, and the following logic sections: instruction decoding, instruction storage, sense, read/write motion control, read/write data control, read/write data storage, and error checking.
I/O Capability	Six external control commands (EXC). Eight transfer commands. Eight sense commands (SEN). Four transport select commands (EXCB).
Control Capability	Can select one of up to four tape transports at any given time. Resetting the system automatically selects tape transport 1.
Data Word	Buffering is provided for two 16-bit words, each containing two 8-bit bytes.
Error Checking	During writing, cyclic redundancy check (CRC) characters and longitudinal redundancy check (LRC) characters are written for each tape record. During reading, these characters are regenerated and compared with those read. The LRC includes a parity check. Error correction is not provided.
Logic level	Positive logic True: +2.5 to +5.0V dc False: 0.0 to +0.5V dc

Table III-4. 620/i-30 Magnetic Tape System Controller Specifications (continued)

Parameter	Description
Size	Two 7-3/4-by-12-inch wired-socket circuit boards.
Interconnection	Each card interfaces with the computer and BIC via a 122-terminal connector. Each card interfaces with tape transport via two 44-terminal connectors.
Input Power	+5V dc, 3A nominal
Operational Environment	+10 to +45 degrees C, 10 to 90 percent relative humidity without condensation.

2.6 620/i-42 AND -43 DISC MEMORY SYSTEM

The 620/i-42 and -43 disc memory systems comprise two of several rotating memory options that are available. The -42 and -43 disc memory options offer bulk storage for data and library software routines. Data can be stored and retrieved at maximum data transfer rates of up to 59K words per second. The 620/i-42A is a hardware expansion option used to increase the basic data storage of the -42 disc memory to a maximum capacity.

The -42 disc memory option offers a basic storage capacity of 131,072 words. This basic capacity can be expanded to a maximum of 262,144 words by incorporating the -42A expansion option. This expansion feature requires the addition of 128 track head assemblies mounted within the disc memory unit. The -43 disc memory option provides a maximum storage capacity of 262,144 words.

Table III-5. 620/i-31 Magnetic Tape System Controller Specifications

Parameter	Description
Organization	Consists of instruction decode and storage sections, sense, read/write data control and write motion control, read motion control, read/write data storage and error checking sections, clock, and drivers and receivers.
I/O Capability	Eight external control commands (EXC). Eight transfer commands. Eight sense commands (SEN). Four transport select commands (EXCB).
Control Capability	Four tape transports any one of which may be selected for connection to the controller. System reset automatically selects transport 1.
Data Word	Buffering provided for two 16-bit words, each word containing up to two bytes.
Error Checking	LRC and CRC characters are generated during read. Error correction is not provided.
Logic level	Positive logic True: +2.5 to +5.0V dc False: 0.0 to +0.5V dc
Size	Two 7-3/4-by-12-inch wired-socket circuit boards.

Table III-5. 620/i-31 Magnetic Tape System Controlller Specifications

Parameter	Description
Interconnection	Each card interfaces with the computer and BIC option via a 122-terminal connector. Each card interfaces with the tape transport via two 44-terminal connectors.
Input Power	+5V dc, 3 amperes, nominal.
Operational Environment	+10 to +45 degrees C; 10 to 90 percent relative humidity without condensation.

The hardware components comprising a complete operating system for both disc memory options are:

a. Rack mounted disc memory unit containing a built-in operating dc power supply.

b. Interconnecting system cable.

c. Plug-in interface and disc controller logic.

The specifications of the disc memory system are listed in table III-6.

Table III-6. 620/i-42 and -43 Disc Memory System Specifications

Parameter	Description
Disc Interface Controller	
Control	One disc memory unit with a storage capacity up to 262K words, plus parity (non-programmed).
Instruction Set	Eight external control (EXC) commands. Eight data transfer instructions. Four sense response (SEN) instructions.
Priority Assignment	None
Dimensions	7-3/4-by-12-inch plug-in circuit card.
Environment	50 to 113 degrees F (+10 to 45 degrees C), 10 to 90 percent relative humidity without condensation.
Disc Memory Unit	
Organization	128 tracks (620/i-42), 256 tracks (620/i-43). One fixed head per track with 1,024 words per track (plus parity).
Rotational Speed	1800 (+23.4, -54.0) rpm
Average Access Time	8.5 milliseconds
Recoverable Error Rate	Less than one in ten billion bits
Write to Read Recovery Time	Less than 200 miscroseconds
Buffered Mode	59,000 words per second

Table III-6. 620/i-42 and -43 Disc Memory System Specifications (continued)

Parameter	Description
Primary Power	120 12V ac, 60 (-1.5, +0.5 Hz, single phase, 8 A starting current, 1.6 A running current.
Environment	50 to 150 degrees F (+10 to 40 degrees C), 20 to 80 percent relative humidity, vibration 1.0G in 10 to 100 Hz range.
Word Transfer Rate:	
Program Mode	30,000 words per second
Bit Transfer Rate	1.5 MHz maximum for read/write operations
Dimensions	17.75 inches high by 17.20 inches wide by 20 inches deep. (Equipped for standard RETMA 19-inch rack mounting)

2.7 620/i-44,-49 DRUM MEMORY SYSTEM

The drum memory system consists of a drum controller circuit card, a Vermont Research Corporation drum memory unit, and a dc power supply.

The drum memory system is field-expandable to accommodate increased system storage requirements. The smaller of the two drums is expandable in increments of 16 tracks up to a maximum of 128 tracks. The larger model is expandable in increments of 64 tracks up to a maximum of 512 tracks. Each track has 1,920 words (16 bits of storage). This provides a maximum storage capacity of 983,040 16-bit words in a 512 data track system. For a 128 data track system, the storage is 245,760 sixteen-bit words. A computer word stored on the drum unit consists of 16 data bits and one parity bit.

The controller circuit card contains all data registers and timing and control logic required to control one drum memory unit. The drum memory unit contains a single rotating drum, mechanical drive assemblies, and read/write control logic. The dc power supply provides required operating voltages.

Control of the drum memory system by the 620/f computer is accomplished under direction of the BIC. The BIC is a prerequisite of the drum memory system. Data transfer between the drum controller and drum memory unit is accomplished via the drum cable.

The drum controller performs the following functions:

a. Controls bit serial data transfer between the controller and drum memory unit.

b. Monitors and detects parity errors during read-from-drum operations.

c. Controls mode of operation and provides all interface control between the computer and the drum memory unit.

The specifications of the controller are listed in table III-7.

2.8 620/i-52 High-speed Paper Tape System

The high-speed tape system is composed of a controller card, a Tally model 420 paper tape perforator, and a Remex model RS0302RB paper tape reader. A Remex model RS0302ARC paper tape spooler is also available for use with the Remex reader if desired.

The controller card contains a data register which buffers the data words being transferred, a decoder section which interprets instructions received from the computer, a timing and control section which synchronizes operation of the peripheral equipment with the computer and necessary interface hardware.

The paper tape controller can transfer data from the tape reader to the computer; it can also transfer data to the tape perforator from the computer, or it can be used to reproduce paper tapes. The controller can transfer data into the computer in a continuous read mode, which places the tape reader in continuous slew until a stop command is received, or it can operate in a step read mode, requiring a new instruction from the computer for each transmitted data word.

Computer control of the paper tape system is accomplished through the I/O bus. The controller can also be operated under direction of the BIC.

Table III-7. 620/i-44 through -49 Drum Memory System Controller Specifications

Parameter	Description
Organization	Consists of a timing and control section, buffer register, shift register, address register/counter, location counter, comparator, and interface drivers and receivers.
Control Capability	One drum memory unit with up to 983,040 17-bit words (16 data bits plus odd parity).
Program Instructions	Two external control commands (EXC). Three transfer commands (OAR, OBR, OME). Seven sense commands (SEN).
Logic Levels	Positive logic True: +2.5 to +5.0V dc False: 0.0 to +0.5V dc
Operational Modes	Read block transfer Write block transfer
Word Transfer Rate	
60 Hz Primary Power	106,000 16-bit words per second
50 Hz Primary Power	88,500 16-bit words per second
Priority Assignment	BIC dependent
Size	One 7-3/4 inch-by-12-inch wired-socket circuit card
Interconnection	Interfaces with the computer and BIC via a 122-terminal connector. Interfaces with

Table III-7. 620/i-44 through -49 Drum Memory System Controller Specifications (continued)

Parameter	Description
	drum unit via two 44-terminal connectors.
Input Power	+5V dc, 2 amperes.
Operation Environment	+5 to +45 degrees C, 10 to 90 percent relative humidity without condensation.

Each controller is capable of operating one perforator and one reader on a time-shared basis.

The specifications of the controller are listed in table III-8.

2.9 620/i-60 DATA COMMUNICATIONS CONTROLLER

The data communications controller system (DCC-1) provides a data communications link between the 620/f computer and remote teletype terminals.

Using telephone lines as the communications media, bidirectional transmission of binary serial data is accomplished by means of Bell System 103A dataset modems and 33/35 ASR teletype terminals. The 103A dataset modems must be located within 50 feet of their associated interface units.

The DCC-1 system offers an economical and efficient means of providing on-line

Table III-8. 620/i-52 High-speed Paper Tape System Controller Specifications

Parameter	Description
Organization	Consists of a timing and control section, an instruction decoder, and an eight-bit data buffer register.
Control Capability	One tape reader and one tape perforator, operated on a time-shared basis.
I/O Capability	Five external control commands (EXC). Eight transfer commands. One sense command (SEN).
Logic Levels	Positive logic True: +2.5 to +5.0V dc False: 0.0 to +0.5V dc
Operational Modes: Continuous Read Step Read Punch	 300 characters per second. One to 300 characters per second. One to 60 characters per second.
Size	One 7-3/4-by-12-inch etched-circuit card.
Interconnection	Interfaces with the computer and BIC option via a 122-terminal connector. Interfaces with tape punch and reader via two 44-terminal connectors.

Table III-8. 620/i-52 High-speed Paper Tape System Controller Specifications (continued)

Parameter	Description
Input Power	+5V dc, 540 mA.
Operational Environment	+10 to +45 degrees C, 10 to 90 percent relative humidity without condensation.

computer services to many remote users. Some typical applications include: on-line program debugging, on-line computation and execution, information storage and retrieval data, inquiry services, computer aid for 'hands-on' use in classroom instruction, and scientific hybrid simulation. In addition, these remote terminals can also be used in an off-line mode for general-purpose utility program routines.

The overall DCC-1 system consists of the power supply (620/i-95-5), Bell System dataset, teletype coupler, 33/35 ASR teletype, a line controller card, and a multiplexer card.

The multiplexer circuit board (DM171) is used to select and control the operation of all the enabled data channels. The line controller circuit board (DM135) provides the logic for four data communication channels.

The specifications of the line controller and multiplexer cards are listed in table III-9.

Table III-9. 620/i-60 DCC-1 System Line Controller and Multiplex Specifications

Parameter	Description
Organization	Line controller: Contains address gates, clock selection logic, and standard driver /receiver stages. Multiplexer: Contains sense and control function logic, address decode clock and logic circuits, interrupt decode enable logic, and clock timing circuits.
Capability	Line Controller: Selects address and generates the control logic necessary to synchronize and communicate with the 103A dataset modems. Each line controller provides four bidirectional data communications channels. Can be expanded to 16 data communications channels. Multiplexer: Provides the interface between the computer I/O bus and data communication channels. Decodes the address and function data, output function commands, channel address codes, and interrupt command signals.
Logic Level	Line controller and multiplexer: Positive Logic: True: +2.5 to +5.5V dc False: 0.0 to 0.5V dc

Table III-9. 620/i-60 DCC-1 System Line Controller and Multiplex Specifications (continued)

Parameter	Description
Size	Line Controller: Circuitry contained on one 7-3/4-by-12-inch wired circuit board (each board contains logic for four data channels). The system can be expanded to incorporate 12 additional data channels. Multiplexer: Circuitry contained on one 7-3/4-by-12-inch wired circuit board.
Interconnection	Line controller and multiplexer: Each card interfaces with the computer via a 122-terminal connector. Each card interfaces with external devices via two 44-terminal connectors.
Input Power to Line Controller	+5V dc, 300 mA.
Input Power to Multiplexer	+5V dc, 600 mA.
Environmental Characteristics	Line Controller and Multiplexer: 0 to 45 degrees C, 0 to 90 percent relative humidity without condensation.

2.10 620/i-72 DIGITAL PLOTTER SYSTEM

The model 620/i-72 digital plotter system consists of a Calcomp 565 digital plotter and a VDM plotter controller card. This peripheral option produces high quality, ink-on-paper graphic presentation of the computer output data.

The plotter controller provides a fully buffered interface to permit operation of the plotter under program control, or under the direction of a buffer interlace controller. The controller is constructed on a single 7-3/4-by-12-inch circuit board.

The plotter uses digital commands from the computer to produce the plot or drawing on a 12-inch wide roll of paper. These commands actuate step motors to produce incremental movement of the pen with respect to the paper. One step motor controls movement in two directions along the X axis, and a separate motor controls movement on the Y axis. X-axis movement is accomplished by rotating the paper drum in either the +X or -X direction. The pen is moved to the left or right to effect movement on the Y axis. Composite commands can be given to move the pen on two axes simultaneously. This results in commands to move the plotter pen in any of eight directions. Model 565 operates at up to 300 increments per second, with three optional increment sizes: 0.005 inches, 0.010 inches, and 0.1 millimeters. The increment size is specified when ordering.

The specifications for the digital plotter system are listed in table III-10.

2.11 620/i-76 BUFFERED LINE PRINTER

The 620/i-76 buffered line printer represents an operational, self-contained subsystem consisting of a high-speed line printer and an interface controller. It provides impact line printing at speeds of up to 600 lines per minute.

This option offers high performance and printing quality to meet user requirements in a wide range of on-line applications. The line printer can also be used for off-line activities by incorporating the required interface control logic.

Significant features and characteristics of the buffered line printer are listed as follows:

a. Fully buffered line storage of up to a 132 six-bit character capacity.

b. Programmed line space control using standard TTY paper tape format.

c. Up to 600 line per minute printing speeds providing 63 graphic and one blank (ASCII) character codes.

d. High reliability and print-out quality as a result of friction-free, one-piece hammer construction.

The specifications for the buffered line printer are listed in table III-11.

Table III-10. 620/i-72 Digital Plotter System Specifications

Parameter	Description
Plotter	
General	Digital commands actuate step motors to produce plot
Increment Sizes (selected when ordering)	0.005 inches; 0.010 inches; 0.1 millimeter
Speed	300 increments per second (maximum)
Plot Dimensions: X axis	11 inches
Y axis	120 feet
Paper	12 inches wide by 120 feet long edge-punched roll; available in a wide variety of patterns printed on various stocks
Pen	Liquid ink or ballpoint pen
Power Requirements	105 to 125V ac, single phase, 50/60 Hz, 1.5A (maximum)
Physical Dimensions	9.8 inches high, 18.0 inches wide, 14.7 inches deep
Operating Environment	0 to 49 degrees C, 0 to 96 percent relative humidity without condensation
Controller	
General	Controls transfer of six-bit commands from 620/i to plotter

Table III-10. 620/i-72 Digital Plotter System Specifications (continued)

Parameter	Description
Organization	Contains interface circuitry, control and timing logic, and six-bit command buffer
Construction	One 7-3/4-by-12-inch circuit board
Input Power	+5V dc at 380 mA -5V dc at 42 mA -12V dc at 15 mA
Environment	0 to 45 degrees C, 0 to 90 percent relative humidity without condensation

2.12 620/i-80 BUFFERED I/O CONTROLLER

The buffered I/O controller provides a self-contained, programmable hardware interface for general-purpose data handling.

The input and output buffer registers provide parallel word data communications between the computer I/O bus and an external device. In addition to data handling,

Table III-11. 620/i-76 Buffered Line Printer Specifications

Parameter	Description
Character Data	
Code Format	Standard ASCII
Character Codes	Sixty-three printable in one blank
Characters per Line	Up to 132
Horizontal Spacing	Ten characters per inch
Vertical Spacing	Six characters per inch
Paper	
General	Standard fanfold, edge-punched
Dimensions	4 to 19 inches wide with 22 inches between folds
Type	Single copy, 15 pound bond minimum weight multi-copy, up to six parts, 12 pound bond with shot carbon
Ribbon	
General	Vertically fed roll type
Dimensions	14 inches wide by 20 yards long
Cabinet	
Dimensions	Height: 44 inches Width: 46 inches Depth: 25 inches
Weight	
Gross (shipping)	1,000 pounds (approx.)
Net	835 pounds (approx.)
Environment Conditions	
Operating Temperature	65 to 90 degrees F

Table III-11. 620/i-76 Buffered Line Printer Specifications (continued)

Parameter	Description
Relative Humidity	30 to 80 percent without condensation
Heat Dissipation	2500 BTU per hour
Dynamic Characteristics	
Printing Speed	Up to 600 lines per minute
Drum Rotation	615 rpm
Primary Voltage	110 to 130V ac
Range	single phase 60 Hz
Current Requirements	40 A starting, 12 A running

the output buffer register can be programmed to output discrete control bits to an external device.

The buffered I/O controller uses a customer-fabricated U cable, up to 20 feet long, for communication to external devices.

The specifications for the controller are listed in table III-12.

2.13 620/i-81 DIGITAL I/O CONTROLLER

The digital I/O controller (DIOC) provides a programmed link between an external device and the computer. There are eight separate control and sensing lines to permit the user to initialize, implement iterative control sequences, synchronize otherwise asynchronous external devices, and monitor the operational state of an external device.

The DIOC operates entirely under program control. The function code defines one of

Table III-12. Buffered I/O Controller Specifications

Parameter	Description
Organization	Contains operation and function decoding logic, input and output buffer registers, eight sense input gates and eight variable-pulse-width control gates, and interface drivers and receivers.
Capability	Provides buffered data transmission to/from external devices and 620/f computer.
Sensing Line Input Current Load	Nominally 7 milliamperes source at 0 volt.
Buffered Output Register Current Load	Nominally 36 milliamperes source at 0 volt.
Control Pulse Output Current Drive	Up to 65 milliamperes sink at 0 volt
Logic levels	Positive logic True: +2.5 to +5.5V dc False: 0.0 to +0.5V dc
Size	Contained on one 7-3/4-by-12-inch wired-socket board.
Interconnection	Interfaces with the computer via a 122-terminal connector. Interfaces with external devices via two 44-terminal connectors.

Table III-12. Buffered I/O Controller Specifications (continued)

Parameter	Description
Input Power	+5V dc, 1.8 amperes.
Operational Environment	+5 to +45 degrees C, 0 to 90 percent relative humidity without condensation.

eight individual control or sensing lines. The DIOC responds to an EXC command by placing a pulse on the selected output control line. Similarly, it responds to a SEN command by testing the operational state of an external device via the true or false level applied to the selected sense-response line.

The DIOC uses a customer-fabricated U cable, up to 20 feet long, for communication to external devices.

The specifications for the DIOC are listed in table III-13.

2.14 620/i-85 ANALOG INPUT SYSTEM

The analog input system (AIS) converts multiplexed analog input signals to their equivalent digital values for processing by the 620/f computer. The AIS consists of an ADC controller card, a multiplexer ADC card, and a power supply for the analog circuits. The basic AIS multiplexer configuration has 32 input channels connected in a single-ended mode, or 16 channels connected in a differential mode. The multiplexer

Table III-13. 620/i-81 Digital I/O Controller Specifications

Parameter	Description
Organization	Contains address and function decode logic, interface drivers and receivers, eight nonbuffered control pulse output gates, and eight nonbuffered sense response input gates.
Controller Circuitry	Eight control pulse gates Eight sense line gates
Expansion Capability	Standard plug-in expansion of up to 64 control and sense lines.
Control Pulse Output Current Drive	48 milliamperes sink at 0 volt
Sense Response Input Current Load	6.5 milliamperes source at 0 volt
Control Pulse Width	200 nanoseconds.
Control Pulse	Maximum = 100 nanoseconds.
Transition Time	Minimum = 5 nanoseconds.
Logic Levels	Positive logic True: +2.5 to +5.5V dc False: 0.0 to +0.5V dc
Size	Mounted on a standard 7-3/4-by-12-inch etched-circuit card.
Interconnection	Interfaces with computer via a 122-terminal connector.

Table III-13. 620/i-81 Digital I/O Controller Specifications (continued)

Parameter	Description
	Interfaces with external devices via two 44-terminal connectors.
Input Power	+5V dc, 250 mA.
Operational Environment	+10 to +45 degrees C up to 90 percent relative humidity without condensation.

channels can be expanded in increments of 32 single-ended channels, or 16 differential channels. There can be a maximum of 128 single-ended channels or a maximum of 64 differential channels in one AIS.

The specifications for the AIS are listed in table III-14.

2.15 620/i-99 IBM 360/VDM 620 INTERFACE CONTROL UNIT

The IBM 360/VDM 620 interface control unit (IFCU) provides a means of communications between a 620/f computer and an IBM system 360 computer I/O channel. The IFCU enables the 620/f to interpret certain 360 I/O channel commands; conversely, it enables the 360 I/O channel to interpret 620/f response to the commands as if received from an IBM 2803 magnetic tape system, for the purpose of providing a data communication path between Varian Data Machines equipment and IBM system/360 equipment.

The IFCU consists of a controller assembly and an electrical interface unit. The

Table III-14. 620/i-85 Analog Input System Specifications

Parameter	Description
Input Signal Full Scale:	
Differential	+11 volts (including CMV)
Single-ended	10 volts
Over voltage and recovery time (Differential and single-ended)	15 volts (with no damage) 5 microseconds (maximum)
Input Impedance	Selected channel 10 megohms and 30 to 100 pF, plus wiring capacity, depending on expansion channels. Unselected channel 100 megohms and 5 pF, plus wiring capacity.
Source Impedance	0 to 1000 ohms for rated performance.
Throughput	Up to 20,000 samples per second.
Aperture Time	50 nanoseconds
System Accuracy	0.05 percent plus one-half LSB.
Channel Cross Talk	0.01 percent for basic system
Temperature Coefficient	0.1 bit/degree C at 25 degrees C
Warm-up Time	15 minutes to rated accuracy
Operating Temperature	0 to 50 degrees C
Differential Common Mode Rejection	8 ddb at 60 Hz with 500 ohms source unbalance

Table III-14. 620/i-85 Analog Input System Specifications (continued)

Parameter	Description
DC Power:	
Analog	+22 volts at 250 mA per card nominal (+5 percent req.) -22 volts at 200 mA per card nominal (+5 percent req.)
Digital	+5 volts at 400 mA per card nominal (10 percent req.)
AC Power:	115 10V ac, single phase, 50 to 400 Hz
I/O Cabling	Designed and fabricated by the user.
Environmental:	
Storage	-20 to 70 degrees C (up to 100 percent relative humidity without condensation).
Operating	5 to 45 degrees C (up to 90 percent relative humidity without condensation).
Analog Channels:	
Basic AIS	Differential - 16 Single-ended - 32
Basic plus	Differential - 32
AIS-1	Single-ended - 64
Basic plus	Differential - 48
AIS-2	Single-ended - 96
Basic plus	Differential - 64
AIS-3	Single-ended - 128

controller assembly consists of two 7-3/4-by-12-inch circuit cards which are installed in a 620/f I/O expansion frame. The connection to the 360 channel is indirect, routed via card-edge connectors through cables to an electrical interface assembly and then via cable connection to the 360 multiplexer or selector channel.

The electrical interface unit (EIU) consists of IBM compatible drivers and receivers mounted on micro-VersaLOGIC cards which are contained in a standard 19-inch panel assembly. Support of 360 I/O channel operations is accomplished by the IFCU hardware in conjunction with a properly programmed 620/f computer.

The specifications for the IFCU are listed in table III-15.

Table III-15. 620/i-99 IFCU Specifications

Parameter	Description
Function	Provides burst-mode communications path between 620/f computer and an IBM system 360 I/O selector or multiplexor channel by emulating the execution of IBM 2803 magnetic tape system commands received via the channel. The storage capacity of a magnetic tape system is not part of the emulation.
Organization	The IFCU simulates the principle functions of the IBM 2803 control unit; and a properly programmed 620/f computer simulates the principle functions of 16 magnetic tape transports attached to a control unit.
620/f I/O Instructions	Seven External Control Eleven Transfer Eight Sense

Table III-15. 620/i-99 IFCU Specifications (continued)

Parameter	Description	
Data Word 620/f	Two 8-bit bytes packed into 16-bit words per IFCU/620 transfer. Capability of transferring odd numbers of characters.	
IBM	Single eight-bit plus parity bytes per IBM/IFCU transfer	
Data Transfer to/from 620/f	All transfer via buffer interlace controller (BIC)	
360/620 Data Transfer Rate	Typically limited by 360 I/O channel maximum which varies widely with each type of channel. BIC maximum is 404K bytes/sec.	
Error Checking	Odd parity generated and checked on all byte transfers between IBM and IFCU	
Logic levels:		
IBM/IFCU	Logical 1:	+2.25 to +7.0V dc
	Logical 0:	0 to +0.15V dc
IFCU/620	Logical 1:	+2.5 to +3.7V dc
	Logical 0:	0 to +0.5V dc
Internal	Logical 1:	+2.5 to +5.0V dc
	Logical 0:	0 to +0.5V dc
Size		
Controller	Two 7-3/4-by-12-inch circuit cards	
EIU	Rackmounted assembly, 19 inches wide; requires 7-inch vertical rack space	

Table III-15. 620/i-99 IFCU Specifications (continued)

Parameter	Description
Interconnections	Interface with 620/f I/O cable through back plane connector; connects controller to EIU via EIU cable. Interface with 360 I/O channel via IBM cables. One IBM part No. 5351178 and two IBM part No. 5353920 required.
Connectors IBM	Two 48-pin connectors to interface to 'upstream' party-line device (or 360 channel) and two identical 48-pin connectors to interface to 'downstream' device.
Input Power (Nominal)	+5V dc, at 6.0 A -12V dc, at 0.25 A
Operational Environment	+5 to +45 degrees C 10 to 90 percent relative humidity without condensation
Control Panel Functions	a. Power turn-on/turn-off b. Operating mode selection
360 I/O Control Unit Address	The 360 control unit address that the IFCU will respond to may be specified at the time of system configuration.
Prerequisites	a. Priority interrupt module (PIM) b. Buffer interlace controller (BIC). The BIC must be dedicated for the exclusive use of the IFCU at all times that the IFCU is on line to the 360 I/O channel.

SECTION 1

PRELIMINARY OPERATION PROCEDURES

1.1 GENERAL

This section describes the preliminary operating procedures that prepare the computer system for use. The preliminary procedures consist of power on, bootstrap loader program, and the binary load/dump program. These programs must be used when a cold start is required. A cold start occurs when the specific contents of memory are unknown.

1.2 PRELIMINARY PROCEDURES

When a new system is being initialized, or when the contents of memory are unknown, make a cold start:

a. Turn the power switch key to PWR ON.

b. Load the bootstrap loader program, either manually (section 2.2.6.2) or, if the system contains an automatic bootstrap, automatically (section 2.2.3).

c. Load the paper tape binary load/dump program provided. Use a 33/35 ASR Teletype reader or a Remex RS0302RB high-speed reader.

The 620/f is now ready for use. The next section explains the switches and indicators on the control console, and the following section gives the manual loading procedure.

SECTION 2

SWITCHES AND INDICATORS

2.1 GENERAL

Figure IV-1 shows the switches and indicators on the control console of the 620/f computer. Their uses are discussed individually in the following subsections.

In addition to these controls, there is a light on the front of the power supply that is lit when the supply is on.

2.2 CONTROL CONSOLE

Used in conjunction with a teletypewriter and peripheral devices, the control console contains all controls necessary to operate the 620/f computer system.

2.2.1 Power Switch

The key-operated power switch controls the ac input to the 620/f power supply.

In the PWR OFF position, there is no ac input to the power supply.

In the PWR ON position, there is ac power to the power supply and the system is fully operational.

In the PWR ON DISABLE position, there is ac power to the power supply and the computer is operational. However, all control console switches are disabled except the power switch itself. Pressing any switch while the power switch is in PWR ON DISABLE has no effect.

The control console and power supply indicator lights are functional when the power switch is in PWR ON DISABLE.

The key can be removed from the power switch in any of the three positions. To turn

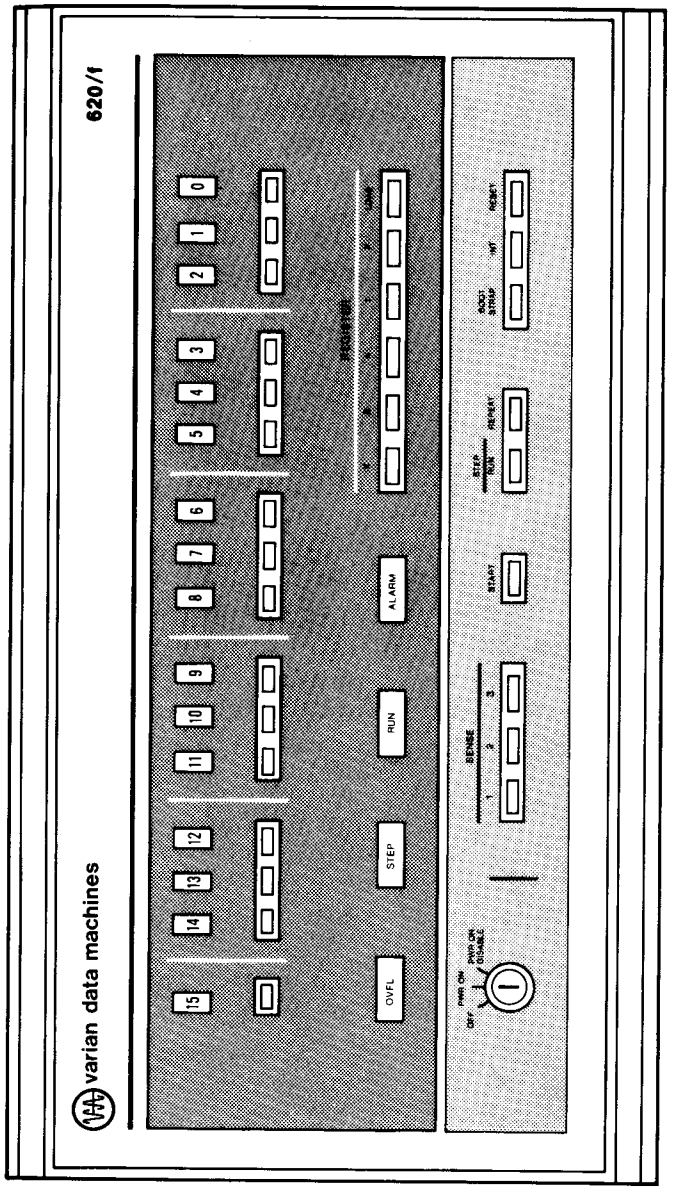

Figure IV-1. 620/f Computer Control Console

VTI1-703

off the computer, place the power switch in the PWR ON position, lift the STEP/RUN switch (section 2.2.2), then turn the power switch to PWR OFF.

2.2.2 STEP/RUN Switch and STEP and RUN Indicators

When the STEP/RUN switch is up, the 620/f is in step mode and the STEP indicator is lit. When the switch is down, the computer is in run mode and the RUN indicator is lit.

If the computer is in the run mode:

a. Pulling the STEP/RUN switch up to STEP position halts the 620/f after completing the execution of the current instruction and fetches the next sequential instruction and places it in the I register. The RUN indicator goes out and the STEP indicator lights.

b. Pressing the START switch (section 2.2.4) starts the program at the location specified by the program counter after executing the instruction in the I register.

If the computer is in the step mode:

a. Pressing the STEP/RUN switch down to RUN position puts the computer in run mode. The STEP indicator goes out and the RUN indicator lights.

b. Pressing the START switch (section 2.2.4) executes the instruction in the I register, and fetches the next instruction from the address specified by the contents of P and places it into the I register.

The STEP/RUN switch is in the RUN position for loading the automatic bootstrap (section 2.2.3), and in the STEP position for manual loading of the bootstrap (section 3.1) and for manual data entry or register display (section 2.2.6).

2.2.3 BOOTSTRAP Switch

BOOTSTRAP is a momentary, spring-loaded switch that is functional in 620/f systems containing the optional automatic bootstrap. In other 620/f systems, this switch is present on the control console but is not connected.

The bootstrap program enables the binary load/dump program to be loaded into memory. Before the automatic bootstrap is loaded into memory, the binary load/dump tape should be inserted into the paper tape reader with the first binary frame at the read station.

To load the automatic bootstrap program:

a. Set the power switch to PWR ON.

b. Set the STEP/RUN switch to RUN.

c. Press and release BOOTSTRAP.

When the automatic bootstrap is thus loaded, load the binary load/dump routine provided on paper tape.

If the system does not contain an automatic bootstrap, load the provided bootstrap program manually (section 2.2.6.2).

2.2.4 START Switch

START is a momentary, spring-loaded switch. Pressing it when the 620/f is in the run mode starts the program. Pressing the START switch when the computer is in the step mode executes the instruction contained in the I register, and fetches the next instruction from the address specified by the contents of P and places in into the I register.

2.2.5 REGISTER Switches

Pressing one of the five REGISTER switches selects the designated register (X, B, A, I, or P) for display or entry (section 2.2.6).

Only one register can be selected at a time. Simultaneously pressing two or more REGISTER switches disables the selection logic and front panel register display.

2.2.6 Register Entry Switches and Display Indicators

The 16 indicators across the top of the 620/f control console display the contents of a selected register. Data are entered into registers on the corresponding register entry switches located under the indicators. The indicators and switches are read from left to right, bits 15 to 0. An illuminated indicator shows that that bit contains a one. For negative data, the sign bit (bit 15) is a one. The indicators and switches are divided into groups of three for ease in reading octal configurations.

2.2.6.1 Register Display

To display the contents of a register, switch the STEP/RUN switch to STEP and press the REGISTER switch for the desired register (section 2.2.5).

The display indicators light when they correspond to register bits that contain ones. To remove the display, pull up on the REGISTER switch and the indicators go out.

2.2.6.2 Data or Instruction Entry

To enter data or instructions in a register:

a. Display the contents of the register (section 2.2.6.1).

b. Enter ones by pressing down on the register entry switches corresponding to the bits to be set.

c. Enter zeros in the other bits by pulling up on all other register entry switches. The indicator lights do not change when the register entry switches are manipulated. They still display the contents of the register.

d. When the desired configuration is entered on the register entry switches, press LOAD (section 2.2.7). This loads the register with the configuration entered on the switches, and the indicators change to display this new configuration in the register.

To enter data into core memory:

a. Load into the I register a storage instruction (STA, etc.).

b. Select the register specified by the storage instruction in step a.

c. Load the selected register using the data entry switches.

d. Press START to execute the instruction in the I register. This stores the contents of the specified register in the effective memory location.

In systems containing the optional TSA instruction, this instruction can also transfer data entered on the control console switches to the A register.

2.2.7 LOAD Switch

LOAD is a momentary, spring-loaded switch. When the 620/f is in step mode and a register has been selected (section 2.2.6), pressing this switch loads the register with the bit configuration entered on the register entry switches.

2.2.8 REPEAT Switch

REPEAT is a toggle switch operative only when the 620/f is in step mode. To repeat an instruction contained in the I register, press REPEAT, and then press START. The instruction is executed again and the program counter advances. However, the contents of the I register remain unchanged.

2.2.9 SENSE Switches

The three SENSE switches are toggle switches permitting program modification by the operator. When the program contains instructions dependent on the setting of these switches (chapter III), jumps and executions occur when the switch condition is met and do not occur when the switch condition is not met.

To set a SENSE switch, press down. To reset it, pull up. Operations dependent on the position of this switch will be executed if the switch is in the position indicated by the instruction, down being the set position.

Example:

> A program can be written so that the operator can obtain a partial total of a column of figures being added by use of the JSS1 (jump if SENSE switch 1 is set) instruction. The program writes individual entries as long as SENSE switch 1 is not set. When the operator wants a partial total, he sets the switch. The program then jumps to an instruction sequence that prints the desired information.

2.2.10 INT (Interrupt) Switch

INT is a momentary, spring-loaded switch used to interrupt the 620/f computer. It is functional only when the 620/f is in the run mode.

In systems that do not contain the optional priorty interrupt module (PIM), pressing INT interrupts to memory location zero.

In systems containing a PIM, pressing INT interrupts to an even-numbered memory location specified by the PIM.

2.2.11 RESET Switch

RESET is a momentary, spring-loaded switch used as initialization control and for stopping I/O operations. Pressing this switch halts the 620/f and initializes the computer and peripherals.

2.2.12 OVFL (Overflow) Indicator

OVFL lights whenever the capacity of the arithmetic unit has been exceeded.

2.2.13 ALARM Indicator

ALARM lights when core memory is overheated. If the power switch key is accessible, turn the power switch to PWR OFF and call the Varian customer service engineer.

If the power switch key is not accessible, turn off the power switch located on the back of the power supply, or pull the main plug, and call the Varian customer service engineer.

SECTION 3

MANUAL OPERATIONS

3.1 GENERAL

With the 620/f in step mode, data or instructions can be manually transferred to or from memory or stored programs can be manually executed.

Note that the I register contains the instruction being executed, while the P register points to the address of the following instructions.

3.2 LOADING, DISPLAY, AND ALTERATION OF MEMORY CONTENTS

To load data or instructions into memory, to display the contents of memory, or to alter the contents of memory, follow the procedures given in section 2.2.6.

3.3 LOADING A GROUP OF SEQUENTIAL MEMORY LOCATIONS

To load a group of sequential memory locations:

a. Place STEP/RUN to STEP and press REPEAT down.

b. Load P register with base address.

c. Load into the I register a storage instruction (STA, etc.) with 100 in the M field (relative addressing), and the base address in the A field.

d. Select the register specified by the storage instruction in step c.

e. Load the selected register using the data entry switches.

f. Press START to execute the instruction in the I register.

g. Repeat steps e. and f. until all instructions are loaded. The next cell to be loaded can be observed by displaying the P register.

3.4 DISPLAYING SEQUENTIAL MEMORY LOCATIONS

To display the contents of a sequential group of memory locations:

a. Place STEP/RUN in STEP, and press REPEAT down.

b. Load P register with base address.

c. Load into the I register a loading instruction (LDA, etc.) with 100 in the M field (relative addressing), and zero in the A field.

d. Select the register specified by the loading instruction in step c.

e. Press START once for each memory location to be displayed.

3.5 MANUAL EXECUTION OF A STORED PROGRAM

To execute a stored program manually:

a. Select STEP mode.

b. Set the P register to the first address of the program.

c. Clear the I register.

d. Press START.

e. Press START again to execute the instruction and to load the next instruction into the I register.

f. Repeat step e. once for each instruction.

3.6 REPETITION OF MANUAL INSTRUCTIONS

To repeat an instruction manually:

a. Press the REPEAT switch down.

b. Press START. This advances the P register but inhibits loading the I register. Thus, pressing START again executes the same instruction.

SECTION 4

PROGRAMMING CONCEPTS

4.1 INTRODUCTION

This section describes the concepts and features of the 620/f computer software. Descriptions of the computer word and number system and the features in the system software package are provided.

4.2 COMPUTER WORD

A 620/f computer word is 16 bits in length and can contain data, a memory address, or an instruction.

4.2.1 Data Word

In data words, the most significant bit (bit 15) is the sign bit. It is zero for positive numbers and one for negative numbers. The other 15 bits contain the data itself. Negative numbers are represented in two's complement form.

4.2.2 Address Word

In address words, the most significant bit (bit 15) is the indirect addressing bit. It is zero for a direct address and one for an indirect address. The other 15 bits contain the address.

4.2.3 Instruction Word

The instruction words are available as single-word addressing and nonaddressing and also as double-word addressing and nonaddressing. The second word of most two-word instructions is an address word. The formats of operational and I/O instructions are described in detail in the 620/f programming reference manual (98 A 9908 020).

4.3 NUMBER SYSTEM

The 620/f computer uses the two's complement technique for arithmetic operations. Negative numbers are represented in two's complement form, and subtraction is accomplished by complement addition. The two's complement of a binary number can be found by replacing all ones with zeros and all zeros with ones, then adding one to the least significant bit position.

The computer uses single precision numbers which contain 15 bits plus a sign bit. The sign bit occupies the most significant bit position (bit 15). A zero in the sign position denotes a positive number; a one in the sign position denotes a negative number. The range of numbers used by the computer is from -32,768 to +32,767. The zero, minus one, and plus and minus full-scale numbers are listed in the binary, octal, and decimal number systems as follows:

Binary	Octal	Decimal	
0111111111111111	077777	+32,767	+Full Scale
0000000000000000	000000	0	
111111111111111	177777	-1	
1000000000000000	100000	-32,768	-Full Scale

4.4 SYSTEM SOFTWARE

A comprehensive package of operational programs is available with the 620/f computer. Included in the software package are the assembler, subroutine library, FORTRAN compiler, debugging package (AID), and diagnostic programs.

4.4.1 Assembler

The 620/f assembler assists in program preparation by translating symbolic source language instructions into an object program for execution on the computer. Although the assembler eliminates the time-consuming effort associated with machine-language programming, it does not compromise the programmer's ability to fully

utilize the 620/f computer. Various memory locations (addresses) can be referred to by labels, rather than absolute locations. Constants can be entered into the computer without converting the numbers into binary or octal form. Useful comments may be added either between symbolic statements or on the symbolic statement itself to allow easy program checkout and documentation.

4.4.2 Subroutines

A comprehensive subroutine library is provided which includes the most commonly used subroutines. The library includes routines for logarithemic, exponential and trigonometric functions, for fixed- and floating-point arithmetic, and for operating standard peripheral equipment. Conventions and instructions are provided so the user can add application programs to the library and be called by the assembler, FORTRAN, or AID.

4.4.3 FORTRAN Compiler

FORTRAN is a universal, problem-oriented programming language designed to simplify the computer solution of mathematical and engineering problems. The syntactical rules for the use of the language are rigorous and require the programmer to reduce the solution characteristics of his problem to a series of precise statements. These statements are evaluated and interpreted by a system program (called the FORTRAN processor) and are translated into the execution language of the computer system.

The FORTRAN compiler for the 620/f computer conforms to the proposed standards for Basic FORTRAN as published by the American Standards Association. The one-pass FORTRAN compiler operates in a 8,192 word computer equipped with only a teletypewriter. Naturally, if higher performance peripherals are in the system, the compiler utilizes them to produce faster compilation.

4.4.4 AID

AID is a collection of useful diagnostic and utility routines that provide on-line debugging of programs. With this package, the programmer can call on a wide variety of functions to aid him in debugging and running his programs. AID includes routines to correct memory, establish breakpoints, search and print memory, etc.

Also included in the AID package is a comprehensive binary paper tape handler that is particularly useful in preserving programs modified on the computer. This routine uses a standard address, data, and check-sum format that is used by the assembler.

4.4.5 Diagnostic Programs

The diagnostic programs are used in the off-line mode to check instructions, memory, and input/output devices and to isolate errors. They can be used in either the preventive or the corrective mode of operation. In the preventative mode, the complete system is checked for operational readiness. If a malfunction exists, in most cases, the preventative will isolate the error. The corrective mode of operation is used when a malfunction is known to exist and the preventive mode does not decisively show the trouble. Proper application of these diagnostic routines can reduce the mean-time-to-repair. The diagnostic programs are described in more detail in Chapter V.

SECTION 5

INSTRUCTION REPERTOIRE

5.1 INTRODUCTION

This section contains 620/f operational instructions, I/O instructions, and device address codes for internal computer and peripheral controller options.

5.2 OPERATIONAL INSTRUCTION

The operational instructions of the 620/f computer are listed in table IV-1.

Table IV-1. Operational Instructions

Mnemonic	Instruction
ADD	Add memory to A register
ADDE	Add extended
ADDI	Add immediate
ANA	AND memory and A register
ANAE	AND extended
ANAI	AND immediate
AOFA	Add overflow to A register
AOFB	Add overflow to B register
AOFX	Add overflow to X register

Mnemonic	Instruction
ASLA	Arithmetic shift left A register
ASLB	Arithmetic shift left B register
ASRA	Arithmetic shift right A register
ASRB	Arithmetic shift right B register
BT*	Bit test
CPA	Complement A register
CPB	Complement B register
CPX	Complement X register
DAR	Decrement A register
DBR	Decrement B register
DIV*	Divide
DIVE*	Divide extended
DIVI*	Divide immediate
DXR	Decrement X register
ERA	Exclusive-OR memory and A register
ERAE	Exclusive-OR extended
ERAI	Exclusive-OR immediate
HLT	Halt
IAR	Increment A register

Mnemonic	Instruction
IBR	Increment B register
IJMP	Jump indexed
INR	Increment memory and replace
INRE	Increment memory and replace extended
INRI	Increment memory and replace immediate
IXR	Increment X register
JAN	Jump if A register negative
JANM	Jump and mark if A register negative
JANZ	Jump if A register not zero
JANZM	Jump and mark if A register not zero
JAP	Jump if A register positive
JAPM	Jump and mark if A register positive
JAZ	Jump if A register zero
JAZM	Jump and mark if A register zero
JBNZ	Jump if B register not zero
JBNZM	Jump and mark if B register not zero
JBZ	Jump if B register zero
JBZM	Jump and mark if B register zero
JMP	Jump (unconditional)

Mnemonic	Instruction
JMPM	Jump and mark (unconditional)
JOF	Jump if overflow indicator set
JOFM	Jump and mark if overflow indicator set
JOFN	Jump if overflow indicator not set
JOFNM	Jump and mark if overflow ind. not set
JS1M	Jump and mark if SENSE switch 1 set
JS2M	Jump and mark if SENSE switch 2 set
JS3M	Jump and mark if SENSE switch 3 set
JSR*	Jump and set return in index register
JSS1	Jump if SENSE switch 1 set
JSS2	Jump if SENSE switch 2 set
JSS3	Jump if SENSE switch 3 set
JS1N	Jump if SENSE switch 1 not set
JS2N	Jump if SENSE switch 2 not set
JS3N	Jump if SENSE switch 3 not set
JS1NM	Jump and mark if SENSE switch 1 not set
JS2NM	Jump and mark if SENSE switch 2 not set
JS3NM	Jump and mark if SENSE switch 3 not set
JXNZ	Jump if X register not zero

Mnemonic	Instruction
JXNZM	Jump and mark if X register not zero
JXZ	Jump if X register zero
JXZM	Jump and mark if X register zero
LASL	Long arithmetic shift left
LASR	Long arithmetic shift right
LDA	Load A register
LDAE	Load A register extended
LDAI	Load A register immediate
LDB	Load B register
LDBE	Load B register extended
LDBI	Load B register immediate
LDX	Load X register
LDXE	Load X register extended
LDXI	Load X register immediate
LLRL	Long logical rotation left
LLSR	Long logical rotation right
LRLA	Logical rotation left A register
LRLB	Logical rotation left B register
LSRA	Logical shift right A register

Mnemonic	Instruction
LSRB	Logical shift right B register
MUL*	Multiply
MULE*	Multiply extended
MULI*	Multiply immediate
NOP	No operation
ORA	Inclusive-OR memory and A register
ORAE	Inclusive-OR extended
ORAI	Inclusive-OR immediate
ROF	Reset overflow indicator
SOF	Set overflow indicator
SOFA	Subtract overflow from A register
SOFB	Subtract overflow from B register
SOFX	Subtract overflow from X register
SRE*	Skip if register equal to memory
STA	Store A register
STAE	Store A register extended
STAI	Store A register immediate
STB	Store B register
STBE	Store B register extended

Mnemonic	Instruction
STBI	Store B register immediate
STX	Store X register
STXE	Store X register extended
STXI	Store X register immediate
SUB	Subtract memory from A register
SUBE	Subtract extended
SUBI	Subtract immediate
TAB	Transfer A register to B register
TAX	Transfer A register to X register
TBA	Transfer B register to A register
TBX	Transfer B register to X register
TSA*	Load A register with switches
TXA	Transfer X register to A register
TXB	Transfer X register to B register
TZA	Transfer zero to A register
TZB	Transfer zero to B register
TZX	Transfer zero to X register
XAN	Execute if A register negative
XANZ	Execute if A register not zero

Mnemonic	Instruction
XAP	Execute if A register positive
XAZ	Execute if A register zero
XBNZ	Execute if B register not zero
XBZ	Execute if B register zero
XEC	Execute (unconditional)
XOF	Execute if overflow indicator set
XOFN	Execute if overflow indicator not set
XS1	Execute if SENSE switch 1 set
XS2	Execute if SENSE switch 2 set
XS3	Execute if SENSE switch 3 set
XS1N	Execute if SENSE switch 1 not set
XS2N	Execute if SENSE switch 2 not set
XS3N	Execute if SENSE switch 3 not set
XXNZ	Execute if X register not zero
XXZ	Execute if X register zero

* Asterisk denotes optional instruction.

Table IV-2. Input/Output Instructions

Mnemonic	Instruction
CIA	Clear and input to A register
CIB	Clear and input to B register
EXC	External control
IME	Input to memory
INA	Input to A register
INB	Input to B register
OAR	Output from A register
OBR	Output from B register
OME	Output from memory
SEN	Program sense

5.3 I/O INSTRUCTION

The I/O instructions of the 620/f computer are listed in table IV-2.

5.4 DEVICE ADDRESS CODES

This section summarizes the device address codes (table IV-3) that are reserved for the teletype controller and internal computer and peripheral controller options. These codes comprise bits 0 through 5 of the I/O instruction (of the first word in the case of a two-word instruction) and bits EB00-I through EB05-I on the E bus. The codes can be altered for special installations.

Table IV-3. Device Address

Octal Class Codes	Octal Addresses Assigned	Internal Option or Controller
00	00	Internal CPU use
01 through 07	01 through 07	Teletype controller
10 through 13	10, 11	Magnetic tape controllers
14 through 17	14 through 17	Disc controllers
20 through 27	20, 21	First BIC
	22, 23	Second BIC
	24, 25	Third BIC
	26, 27	Fourth BIC
30 through 37	30	Card reader
	31	Card punch
	32	Digital plotter
	35, 36	Line printer
	37	Paper tape system (punch and/or reader)
40 through 47	40	PIM
	45	Memory protect
	47	Real-time clock
50 through 53	50 through 53	Optical devices
54 through 57	54 through 57	Analog systems
60 through 67	60 through 67	Digital I/O controllers
70 through 77	70 through 77	Special applications

SECTION 1

INTRODUCTION

The circuitry of the 620/f computer achieves high reliability through extensive use of integrated circuits. For the most part, malfunctions occurring in a computer system are caused by external sources such as overheating, power failure, and operator error. The 620/f computer is designed to reduce the occurrence of malfunctions due to these sources. When an overheating condition occurs, a console alarm indicator lights indicating to the operator that the computer should be turned off. When a power failure (or turn-off) occurs, the power failure/restart (PF/R) option provides an orderly shutdown and restarts the program when power is restored. To prevent accidental setting of console controls during computer operation, the console switches can be disabled with the PWR ON/OFF/ DISABLE switch.

The following sections describe additional features that help simplify the 620/f computer maintenance.

SECTION 2

CIRCUIT CARD ACCESSIBILITY

2.1 INTRODUCTION

All computer circuits are contained on plug-in type circuit cards. Three basic types of circuit cards are used:

a. Cards in the CPU tray, 3 by 15 inches.

b. Cards in the memory tray, 15 by 18 inches.

c. Peripheral controller cards, 7-3/4 by 12 inches.

As described in the following paragraphs, the three card types are easily accessible for troubleshooting during computer operation.

2.2 CARDS IN CPU TRAY

When the computer is turned off and the control console open, the CPU tray can be disconnected from the mother board. A flexible extender cable is connected between the mother board and the CPU tray, allowing the tray to extend forward through the front of the mainframe. The CPU tray is then firmly attached to a bracket mounted on the front of the mainframe. A card can be made accessible for troubleshooting by installing it on an extender card. With the CPU tray and the circuit card in this configuration, the computer can be turned on to begin troubleshooting.

2.3 CARDS IN MEMORY TRAY

The memory trays can be extended through the front of the mainframe or expansion frames in the same manner as the CPU tray. The memory cards are mounted with hinges that allow them to be opened. A card is made accessible for troubleshooting by opening it to a convenient position where it can be held firmly with a support brace.

2.4 PERIPHERAL CONTROLLER CARDS

Any peripheral controller card is accessible for troubleshooting when it is installed on a DM115 extender card. This allows the peripheral controller card to extend outside the rear of the computer frame. In this configuration, the controller interfaces with the CPU through the extender card and with the peripheral device through the two 44-pin card-edge connectors.

SECTION 3

DIAGNOSTIC PROGRAMS

3.1 INTRODUCTION

Diagnostic programs are provided to minimize the maintenance time of the 620/f computer. These programs are used in the off-line mode when the computer is not performing data transfer or control functions.

The diagnostic programs, which are contained on a punched paper tape, exercise the computer and associated peripheral devices with sequences of instruction. The results of these sequences are checked against the proper responses. If an instruction or other operation is improperly executed, the program ends the sequence and causes the printing of information indicating which instruction or operation failed. The technician can then repeat, continue, or halt the diagnostic routine until the fault is isolated and corrected.

The diagnostic programs can be used in either a preventive or a corrective mode of operation.

3.2 PREVENTIVE MODE

The diagnostic programs, when used in a preventive mode of operation, determine whether a malfunction exists and, in most cases, isolate the error. In the preventive mode of operation, the diagnostic program tape is loaded into memory, and the teletype keyboard is used to initiate tests or a sequence of tests. A teletype driver program, which is included on the diagnostic tape, interprets the teletype keyboard input and calls each of the designated test programs the number of times specified in the sequence. If an error occurs, an error indication is printed by the teletype unit.

3.3 CORRECTIVE MODE

The diagnostic programs can be used in a corrective mode of operation when a malfunction is known to exist but the exact nature of the trouble has not been determined. In the corrective mode of operation, a specific diagnostic program can be loaded and run independently of any other program. Each test within a program is initiated manually from the computer control console. Error indications are printed automatically by the teletype unit.

SECTION 4

TROUBLESHOOTING

4.1 INTRODUCTION

The speed and ease with which the computer operator can detect, locate, and correct a malfunction and return the machine to proper operation is a measure of the efficiency of the 620/f system. The computer is electrically and mechanically designed to ease the tasks of maintenance and malfunction correction.

The time required to correct system malfunctions depends on the efficiency of the procedures used. Although various specified techniques may be applied, there is no real substitute for an ordered, logical analysis of the problem and isolation of the cause to the level of the replaceable component. Such an analysis can be based only on knowledge of the equipment design.

4.2 TROUBLESHOOTING TECHNIQUES

One of the most valuable troubleshooting aids available to the technician is the computer control console. By using the controls and indicators, the operator can manually execute simple procedures to check out various computer operations such as register set and reset functions, communication between registers and memory, and arithmetic operations.

The recommended troubleshooting steps for maintaining the computer are illustrated in figure V-1.

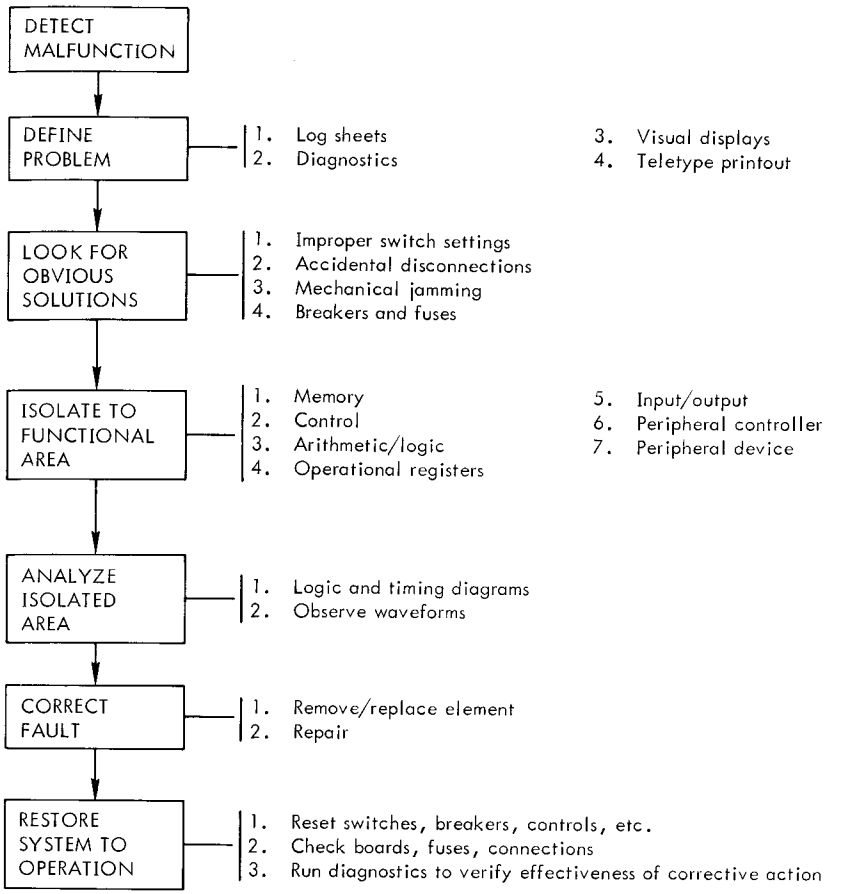

Figure V-1. General Troubleshooting Steps

4.2.1 Define the Problem

Take time to thoroughly define the problem. For example, if the ADD instruction does not produce correct results, is the fault a function of the sign (plus or minus), of the carries, or of some other element Are the operational registers being properly loaded Use the displays, connector pins, and integrated circuit terminals for gathering the necessary data.

4.2.2 Look for Obvious Solutions

Make sure that a malfunction has actually occurred. Relate problems to recent events, such as cleaning or servicing. Look for improperly set controls or test equipment and accidental disconnections of plugs, etc. Consider miscellaneous temporary failures, such as mechanical jamming of peripheral equipment.

4.2.3 Isolate to a Functional Area

Isolate the fault to a functional area, such as memory, control, arithmetic/logic, operational register, I/O, peripheral controller, or peripheral device. The process of isolating the malfunctioning area is generally a straightforward process of eliminating the functional areas that are operating properly.

4.2.4 Analyze the Area

When the fault has been isolated to a functional area, the rest of the system can generally be temporarily ignored. Use the logic and timing diagrams, and observe circuit waveforms to quickly isolate the problem to an individual replaceable element. The computer must be in the step mode (STEP indicator on) before removing input power.

4.2.5 Correct the Fault

Replace the faulty circuit card or other element. Attempt to analyze the cause of the failure before restoring power to prevent the reoccurrence of the failure.

4.2.6 Restore the System to Normal Operation

When the system appears to be operating properly, make sure it is returned to normal operating conditions. If circuit cards have been unseated, be sure all are properly reseated in the connectors. Set all console controls and place the POWER switch in the ON position. Finally, verify proper operation by running the diagnostic programs.

4.3 TEST EQUIPMENT REQUIRED

Recommended test equipment required to maintain the 620/f computer is listed in table V-1.

Table V-1. Required Test Equipment

Equipment	Description
Oscilloscope	Tektronix, type 547 (or equivalent) with dual-trace plug-in unit
Multimeter	Simpson 260 or equivalent
Card Extenders	a. Extender cards for cards in CPU tray b. Extender cards (DM115) for peripheral controllers
Extension Cable	Required for CPU and memory trays
Card Puller	Titchener 1731
Wire Wrap Gun	Denver-Gardener 14R2 or equivalent
Soldering Iron	39-watt pencil type

APPENDICES

Table of Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

OCTAL-DECIMAL INTEGER CONVERSION TABLE

0000	0000
to	to
0777	0511
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000	0512
to	to
1777	1023
(Octal)	(Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL-DECIMAL INTEGER CONVERSION TABLE

2000	1024
to	to
2777	1535
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

3000	1536
to	to
3777	2047
(Octal)	(Decimal)

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

OCTAL-DECIMAL INTEGER CONVERSION TABLE

4000 (Octal)	2048 (Decimal)
to	to
4777 (Octal)	2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 (Octal)	2560 (Decimal)
to	to
5777 (Octal)	3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL-DECIMAL INTEGER CONVERSION TABLE

6000 (Octal)	3072 (Decimal)
to	to
6777 (Octal)	3583 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

7000 (Octal)	3584 (Decimal)
to	to
7777 (Octal)	4095 (Decimal)

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3985	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000785	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

DATA 620/i Standard BCD Codes

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
@	300	00	32	0-2-8	77
A	301	01	61	12-1	13
B	302	02	62	12-2	14
C	303	03	63	12-3	15
D	304	04	64	12-4	16
E	305	05	65	12-5	17
F	306	06	66	12-6	20
G	307	07	67	12-7	21
H	310	10	70	12-8	22
I	311	11	71	12-9	23
J	312	12	41	11-1	24
K	313	13	42	11-2	25
L	314	14	43	11-3	26
M	315	15	44	11-4	27
N	316	16	45	11-5	30
O	317	17	46	11-6	31
P	320	20	47	11-7	32
Q	321	21	50	11-8	33
R	322	22	51	11-9	34
S	323	23	22	0-2	35
T	324	24	23	0-3	36
U	325	25	24	0-4	37
V	326	26	25	0-5	40
W	327	27	26	0-6	41

DATA 620/i Standard BCD Codes (continued)

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
X	330	30	27	0-7	42
Y	331	31	30	0-8	43
Z	332	32	31	0-9	44
[	333	33	75	12-5-8	76*
\	334	34	36	0-6-8	76*
]	335	35	55	11-5-8	76*
↑	336	36	17 (Note)	7-8	76*
←	337	37	20	2-8	76[1]
blank	240	40	20	No Punch	00
!	241	41	52	11-2-8	51
"	242	42	35	0-5-8	62
#	243	43	37	0-7-8	63
$	244	44	53	11-3-8	60
%	245	45	57	11-7-8	64
&	246	46	77	12-7-8	65
'	247	47	14	4-8	66
(	250	50	34	0-4-8	52
)	251	51	74	12-4-8	53
*	252	52	54	11-4-8	47
+	253	53	60	12	45
,	254	54	33	0-3-8	54
-	255	55	40	11	46
.	256	56	73	12-3-8	51
/	257	57	21	0-1	50

DATA 620/i Standard BCD Codes (continued)

Symbol	ASCII	Printer	Mag Tape	Hollerith	FORTRAN
0	260	60	12	0	01
1	261	61	01	1	02
2	262	62	02	2	03
3	263	63	03	3	04
4	264	64	04	4	05
5	265	65	05	5	06
6	266	66	06	6	07
7	267	67	07	7	10
8	270	70	10	8	11
9	271	71	11	9	12
:	272	72	15	5-8	67
;	273	73	56	11-6-8	70
<	274	74	76	12-6-8	76*
=	275	75	13	3-8	55
>	276	76	16	6-8	76[2]
?	277	77	72	12-2-8	76

Note: End-of-file for mag tape.
*: Undefined character.
1: Form control: Return to col 1.
2: Tab control: Skip to col 7.
} FORTRAN System only

Teletype Character Codes

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
0	260	Y	331
1	261	Z	332
2	262	blank	240
3	263	!	241
4	264	'	242
5	265	#	243
6	266	$	244
7	267	%	245
8	270	&	246
9	271	'	247
A	301	(	250
B	302	)	251
C	303	*	252
D	304	+	253
E	305	,	254
F	306	–	255
G	307	.	256
H	310	/	257
I	311	:	272
J	312	;	273
K	313		274
L	314	=	275
M	315		276
N	316	?	277
O	317	@	300
P	320		333
Q	321		334
R	322		335
S	323		336
T	324		337
U	325	Rub Out	377
V	326	NUL	200
W	327	SOM	201
X	330	EOA	202

Teletype Character Codes (continued)

Teletype Character	DATA 620/i Internal Code	Teletype Character	DATA 620/i Internal Code
EOM	203	X-OFF	223
EOT	204	TAPE OFF	
WRU	205	AUX	224
RU	206	ERROR	225
BEL	207	SYNC	226
FE	210	LEM	227
H TAB	211	SO	230
LINE FEED	212	S1	231
V TAB	213	S2	232
FORM	214	S3	233
RETURN	215	S4	234
SO	216	S5	235
SI	217	S6	236
DCO	220	S7	237
X-ON	221		
TAPE AUX ON	222		