VALID

SCALD
Logic Simulator

FEATURES

- Provides easy to use interactive, gate-level logic simulation
- Very high-speed simulation can be accomplished
- Simulates buses and multiple-bit devices in parallel
- Interactive user interface facilitates debugging of designs
  - Can be used interactively from a SCALD-system™ Design Station
  - All signals and memory contents can be displayed or changed
  - Simulated time can be advanced by any amount desired
  - Your debugging strategy can be dynamically changed
- Requires only the logic diagrams as input
  - Does not require user programming
  - Understands high-level graphic primitives
  - Uses graphic user-defined simulation models
- Capable of simulating partially completed designs
- Can be used to develop and debug microcode
- Allows simulation of tri-state and undefined logic
- Generates high-level behavioral models

DESCRIPTION

The SCALD Logic Simulator lets you simulate a design down to the component level. It uses the same design database for simulation as is used for implementation thus making separate descriptions for the system unnecessary.
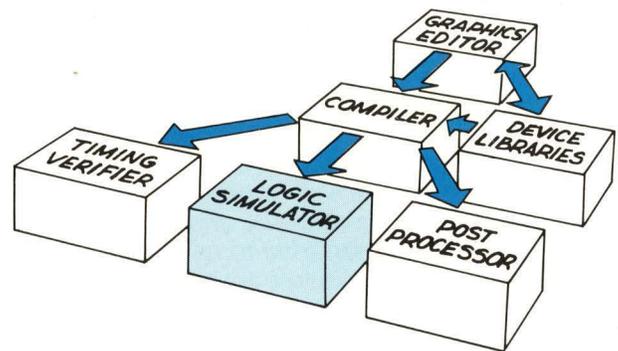
High Speed Simulations

A key feature of the SCALD Logic Simulator is speed. One reason for its high speed is that timing verification is handled separately.

Traditionally, logic simulation and timing verification are combined procedures. By clarifying and separating these functions the SCALD-system™ achieves complete and highly efficient design validation. The SCALD Timing Verifier, when used first, will have already analyzed the design for timing errors, thus simplifying the task of simulation. Additionally, the SCALD Logic Simulator can operate on buses and multi-bit devices in parallel. The result is a simulator that is an order of magnitude faster than other methods—finally making it practical to simulate large designs.

VALID makes available to the engineer device libraries containing complete information on TTL, LSTTL, 10K ECL, 100K ECL, STL, CMOS and memory circuits. You can also create your own simulation libraries for customized devices very easily. This is accomplished by graphically modeling the behavior of the device using a set of simulator primitives provided by VALID. The primitives include gates, flip-flops, multiplexers, adders, registers, memories and other components. More complex primitives, like a complete ALU are also supplied. In addition, the user may take advantage of the hierarchical features of SCALD to construct building blocks from primitives.

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4-State Simulations

The SCALD 4-state simulation approach correctly handles tri-state and undefined values. Start-up analysis of circuits is done by initializing all signals to the undefined state and advancing time. If the design is correct, reset circuitry will place all signals in a known state.

The SCALD Compiler passes logic family information to the simulator so that wire-tie operations can be simulated. The Simulator correctly handles combined output types (e.g. open-collector, open-emitter, tri-state) being simultaneously driven.

Interactive Simulation

The SCALD Logic Simulator is interactive, eliminating the need to devise a complete scenario for simulation prior to its running. The SCALDsystem™ gives you full control over the simulation process and directs your attention to just those signals of current interest. You can easily and dynamically change the debugging plan in response to new information. When used interactively through SCALDsystem's™ design stations, all pertinent simulation information is displayed on the screen. You can examine or modify any signal, bus, or memory in your design. Provide initialization and external stimulus through a simulation command file, or by simulating an additional circuit specially drawn to provide stimulus.

The command file can also be used to exercise a design in a way that is analogous to a diagnostic program. This file may be used to provide circuit stimulus and check certain signals for correct values. This capability allows the designer to verify that previously checked-out circuits are still working correctly after design modifications.

The SCALD Simulator is another example of the unique validation tools that are available from VALID.

```
              SCALD Logic Simulator
Time:      600  Step:    100  Radix: 10      Clock:    100/ 10
Mem path: (219.1P)   16 words/   8 bits

FIBONACCI T-2 <0..15>  00005d    CYCLES COMPLETED <0..7>    06o
FIBONACCI T-1 <0..15>  00008d    CLOCK !C 0-2,3-5 1b
NEW FIBONACCI <0..15>  00013d


Time:      700  Step:    100  Radix: 10      Clock:    100/ 10
Mem path: (219.1P)   16 words/   8 bits

FIBONACCI T-2 <0..15>  00008d    CYCLES COMPLETED <0..7>    07o
FIBONACCI T-1 <0..15>  00013d    CLOCK !C 0-2,3-5 1b
NEW FIBONACCI <0..15>  00021d


Time:      800  Step:    100  Radix: 10      Clock:    100/ 10
Mem path: (219.1P)   16 words/   8 bits

FIBONACCI T-2 <0..15>  00013d    CYCLES COMPLETED <0..7>    10o
FIBONACCI T-1 <0..15>  00021d    CLOCK !C 0-2,3-5 1b
NEW FIBONACCI <0..15>  00034d
```

Figure 1. The SCALDsystem™ display shows the simulator's status. At the top of the screen are pertinent perameters regarding the simulation. Also shown are user selected signals and their state.

Figure 2. Models in the SCALDsystem™ are simply schematic diagrams drawn in terms of Simulator primitives. Shown is the model for a 100155.

![VALID logo]