TECHNICAL MANUAL

OPERATION AND MAINTENANCE WITH PARTS LIST

DATA PROCESSING SET

AN/UYK-20(V)1

Published by direction of Commander Naval Electronics Systems Command

RECORD OF CHANGES

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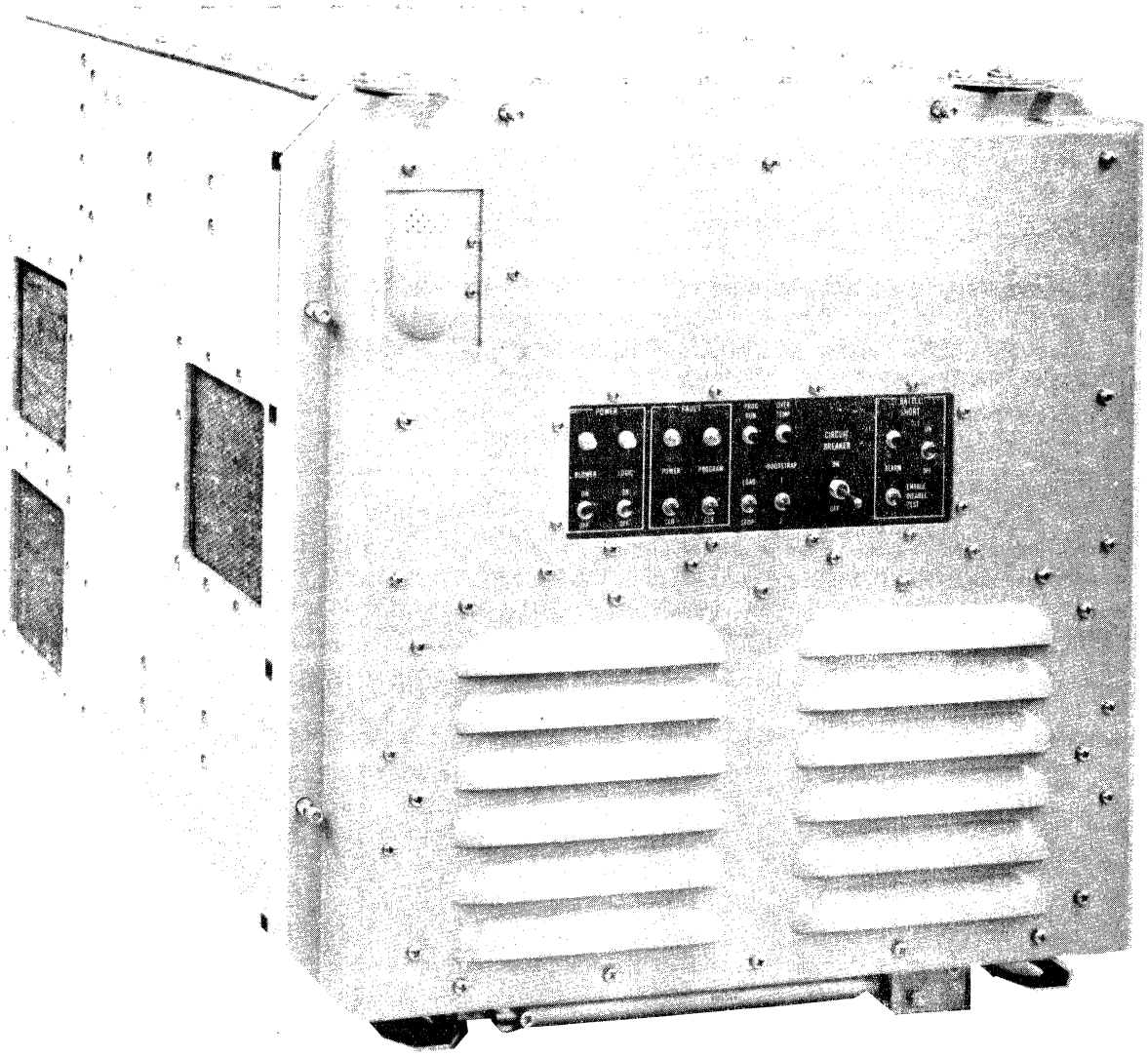


Figure 1-1. Data Processing Set, AN/UYK-20(V)1

CHAPTER 1

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. SCOPE. This technical manual describes the Data Processing Set (figure 1-1), AN/UYK-20(V), hereafter generally called the DPS. The manual documents all variations of the DPS in existence at time of publication, and provides the information normally necessary to install, operate, and maintain it.

1-3. MANUAL ORGANIZATION. This technical manual is divided into ten chapters. Chapter 9, Equipment Diagrams, is in a separate B-size volume. Chapter 10 is in a separate A-size volume and documents the maintenance/diagnostic program. Chapters 1 through 8 are in this volume; a brief description of each chapter follows.

1-4. Chapter 1 - General Information. Chapter 1, General Information, contains a brief description of the DPS and a basic explanation of the functions or operations it performs. It also contains a quick reference table of the equipment characteristics, and lists of recommended tools and associated equipment.

1-5. Chapter 2 - Operation. Chapter 2, Operation, describes the operating controls and indicators, gives instructions for manual operation, and lists the repertoire of computer macro instructions and micro instructions.

1-6. Chapter 3 - Functional Description. Chapter 3, Functional Description, describes the internal operation of the DPS on the basis of primary block diagrams and functional block diagrams.

1-7. Chapter 4 - Preventive Maintenance. Chapter 4, Preventive Maintenance, provides scheduled procedures for ensuring that the DPS is in optimum operating condition.

1-8. Chapter 5 - Troubleshooting. Chapter 5, Troubleshooting, suggests ways to use all data contained in this manual when troubleshooting, and provides procedures for isolating various faults.

1-9. Chapter 6 - Corrective Maintenance. Chapter 6, Corrective Maintenance, provides information for removal, replacement, reinstallation, and repair of parts and assemblies.

1-10. Chapter 7 - Parts List. Chapter 7, Parts List, lists and describes the replaceable electrical and mechanical parts.

1-11. Chapter 8 - Installation. Chapter 8, Installation, contains information concerning equipment installation, including outline drawings to illustrate space requirements and to aid in interconnecting to other equipment.

1-12. Appendices. Appendices following Chapter 8 contain detailed descriptions of the macro and micro instruction repertoires and a glossary of unique terms.

1-13. FUNCTIONAL DESCRIPTION.

1-14. The Data Processing Set AN/UYK-20(V) meets the various processing requirements of Naval shipboard, land-based, and submarine combat systems. It is a modular, medium-scale, general purpose digital data processing device using a microprogrammed control structure. The microprogram consists of micro instructions and control data stored in a read-only memory (ROM). The computer operates from a stored program of macro instructions read from main memory to perform arithmetic operations, solve real-time problems, control other equipment, and perform a variety of other data processing operations. It performs two's complement integer arithmetic using signed numbers. Its logic construction is parallel. The basic word length is 16 bits which may be handled as 8-bit bytes (such as ASCII character codes), as 16-bit words, or as double-length 32-bit words. It has memory addressing capability of up to 65K 16-bit words which may be treated as groups of pages for relative (virtual) addressing. The memory cycle time is 750 nanoseconds. The DPS communicates with peripheral equipment through an I/O controller containing up to 16 channels, which may be parallel or serial channels or a mixture of both. It has an interrupt structure, dependent on priority assignments, which permits interruption of the normal program sequence to perform special functions. It allocates a portion of micro-memory for a user-defined microprogram. It has a real time clock and a monitor clock which operate either from an internal oscillator or from an external clock input.

1-15. Figure 1-2 is a simplified block diagram of the DPS. The sections shown are functional divisions, not separate physical entities. The processor/emulator performs the arithmetic and data processing operations as directed by a program of instructions. The I/O circuits transfer data between the DPS and peripheral equipment. The main memory stores instructions, operands, and other data. The processor, I/O, and memory interface circuits are under the control of a microprogrammed controller (MPC) operating from its own microprogram stored in a read-only memory. Data transfers between the major elements occur over two 16-bit bidirectional busses: a source bus and a destination bus. Control signals between sections do not use the busses, but are wired directly.

1-16. CONTROL PANELS. The DPS has two control panels: an operator's panel and a maintenance panel. The panel controls provide for applying and removing power, starting and stopping operations, operating in different modes, master clearing (master reset), controlling programmed stops, and for other manual control or manipulation of the DPS. The panel controls permit displaying and manually modifying register contents through the register display. The registers that can be displayed and modified are the general registers, the P register (program address register), the memory address register, the U register (macro-instruction register), status register #1, status register #2, the real-time clock registers, the breakpoint register, the I/O control memory, the micro-address register, and the micro-instruction register. A detail description of the operating controls is contained in Chapter 2.

1-17. MICROPROGRAMMED CONTROLLER (MPC). The MPC provides all control functions for the DPS to execute the program stored in main memory. The MPC has its own microprogram (also called firmware) stored in a read-only memory that the MPC executes to provide the control functions and data manipulations. All registers and logic networks in the DPS are addressable by the micro-instructions. For each macro-instruction read from main memory, several micro-instructions are used by the MPC to provide control, timing, and data transfers necessary to execute the macro-

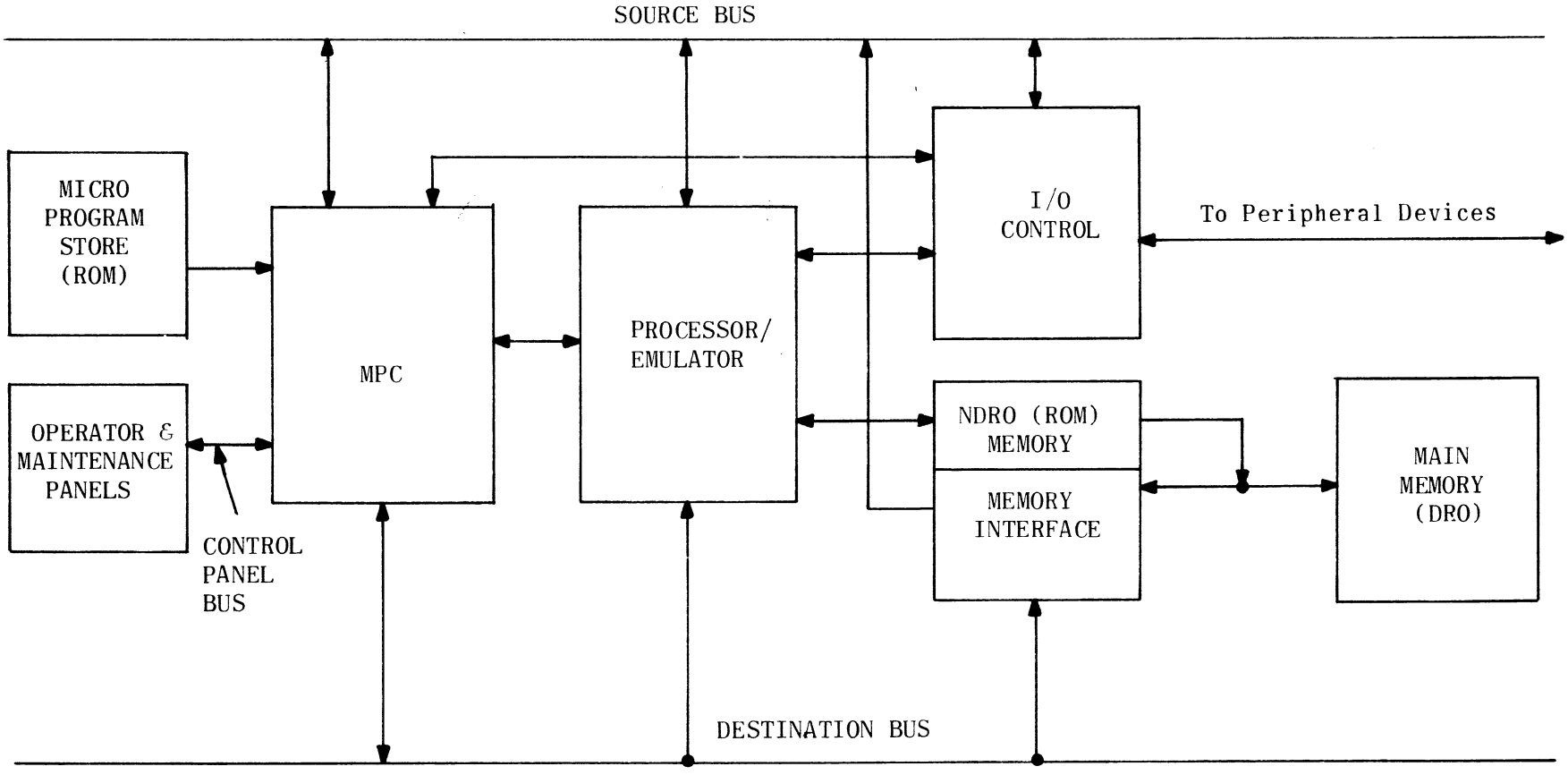


Figure 1-2. Simplified Block Diagram

instruction. In effect, the microprogram replaces some of the control logic that would otherwise be required to execute the macro-instruction.

1-18. The MPC receives an Emulator Control Word (ECW) from the processor for each macro-instruction read from main memory. The ECW contains control bits and an address pointer. The address pointer is the starting address of a microprogram subroutine which the MPC uses to execute that particular micro-instruction. When a subroutine is completed, the MPC branches to a microprogram subroutine to read the next instruction from main memory.

1-19. The MPC also controls the panel display function.

1-20. PROCESSOR/EMULATOR. The processor/emulator contains logic circuits which augment the MPC. It contains an instruction register to hold the macro-instruction during execution and other registers and subsections that operate under MPC control to form an efficient general purpose processor. These include the general registers, status register, real time clock and monitor clock registers, interrupt control, and high-speed shift and multiply circuits.

1-21. An instruction is fetched from main memory and loaded into the instruction register by the MPC via the source bus. The instruction is translated and the processor sends an Emulator Control Word (ECW) to the MPC. Each instruction has its own ECW which is stored in a small ROM. The ECW directs the MPC in execution of the instruction.

1-22. MEMORY INTERFACE. The memory interface handles the transfer of information between the processor or the MPC and main memory, and between I/O control and main memory. An I/O channel memory request has priority over a program request. The memory interface is asynchronous, using requests and acknowledges. It initiates the memory for a read or write operation and sends a 16-bit address to memory. The data word transferred between the memory interface and memory also contains 16 bits.

1-23. The memory interface section contains a 192-word non-destructive readout (NDRO) memory. Access to the NDRO is controlled by the condition of the NDRO mode bit in the status #1 register. When the bit is clear, addresses from 00-77 (octal) and 300 to 477 (octal) are read from the NDRO memory instead of the main memory.

1-24. MAIN MEMORY. The main memory provides storage for the macroprogram. It is available in 8192-word (8K) increments to a maximum of 65,536 words (65K). Word length is 16 bits and the main memory cycle time is 750 nanoseconds nominal.

1-25. I/O CONTROL. The I/O Control section provides for communication between the DPS and peripheral equipments, including up to sixteen I/O channels. The system provides asynchronous parallel I/O channels, expandable in groups of four channels, and/or serial channels, expandable in groups of two channels, to a possible combined total of 16 channels. The channels within a group must have identical interface characteristics. All channels are fully duplexed to permit input and output transmissions to occur simultaneously.

1-26. The parallel I/O channels operate with either a Naval Tactical Data System (NTDS) Fast (-3v), an NTDS Slow (-15v), or an ANEW (+3.5v) interface. They are capable of operation in single word (16 bit) mode or dual word (32-bit) mode. Both single and dual channels are capable of operation in an Intercomputer mode. Dual channels are also capable of operation in a UYK-7 compatible Externally Specified Addressing (ESA) mode when so requested on the initial equipment order.

1-27. The NTDS serial I/O channel is an asynchronous double word length (32-bit) data communication channel formed from two adjoining 16-bit channels. Each 16-bit channel requires one coaxial cable for input and another for output. Information is transmitted using bi-polar, phase modulated, serial pulse trains.

1-28. Synchronous serial channels provide communications at bit rates up to 9600 bits per second (bps). They are capable of accepting an external clock signal.

1-29. Asynchronous serial I/O channels may have any four of the following modulation rates selectable through the program: 75, 150, 300, 600, 1200, or 2400 baud. The four rates desired for each two-channel group must be specified at time of equipment order. The character interval consists of up to ten signal elements with equal time intervals: they comprise one start element, five to seven data elements, one character parity element, and one or two stop elements.

1-30. POWER. The power section includes the power supply and power distribution circuits. This section converts ac input power into the dc power required for the logic circuitry and the memory. The power supply is regulated against input voltage variations and transients, and it protects against output overload conditions. It has sufficient capacitor energy storage so that it continues to provide in-tolerance output power for a minimum of 250 usec after an input voltage loss is detected, to permit storing the contents of the working registers before shutdown occurs.

1-31. PHYSICAL DESCRIPTION.

1-32. Figures 1-1 and 1-3 picture the DPS. Its nomenclature is AN/UYK-20(V) Data Processing Set for the 400 Hz configurations or AN/UYK-20X(V) for the 60 Hz configurations. It consists of a single cabinet. A hinged door, called the Control-Indicator Unit, forms the front of the cabinet. Its front side contains an operator's control panel with the most essential controls and indicators. A more complete maintenance control panel is mounted on the back side of the door and is accessible with the door open. An alarm horn and the air intake grill and filter are also on this door. Immediately behind the door is the memory chassis, which is hinged and mounted on slides so it may be extended and completely exposed for servicing. Behind the memory, and accessible when the memory chassis is extended, are the processor/IOC chassis and the power supply. The rear panel of the cabinet contains the power connector and grounding stud. The cabinet's left side as you face the cabinet contains air exhaust grills for the power supply, processor/IOC chassis, and memory chassis, each of which has its associated blower. Cabinet dimensions are given in Chapter 8 of this manual.

1-33. The processor/IOC chassis is called the Processor-Verifier Unit. It contains two sizes of printed circuit cards. The processor circuits are mostly contained on single-width cards, as illustrated in figure 1-4, and the I/O circuits are mostly contained on triple-width cards, as illustrated in figure 1-5. The single-width circuit cards are single-layer boards with printed wiring on both sides; the triple-width cards are three-layer boards. Single width cards have one 56-pin connector; triple width cards have two connectors. Guide pins on the connectors are keyed to keep the cards from being inserted into the wrong jack, and the card shape keeps them from being inserted into their jacks backwards. The cards have test points along their top edges and a notch or square blivet identifies the first test point. The maintenance philosophy expects faulty cards to be replaced, rather than repaired. The rear panel of the processor/IOC chassis contains the I/O connectors. With the chassis removed from the cabinet this panel can be removed for access to

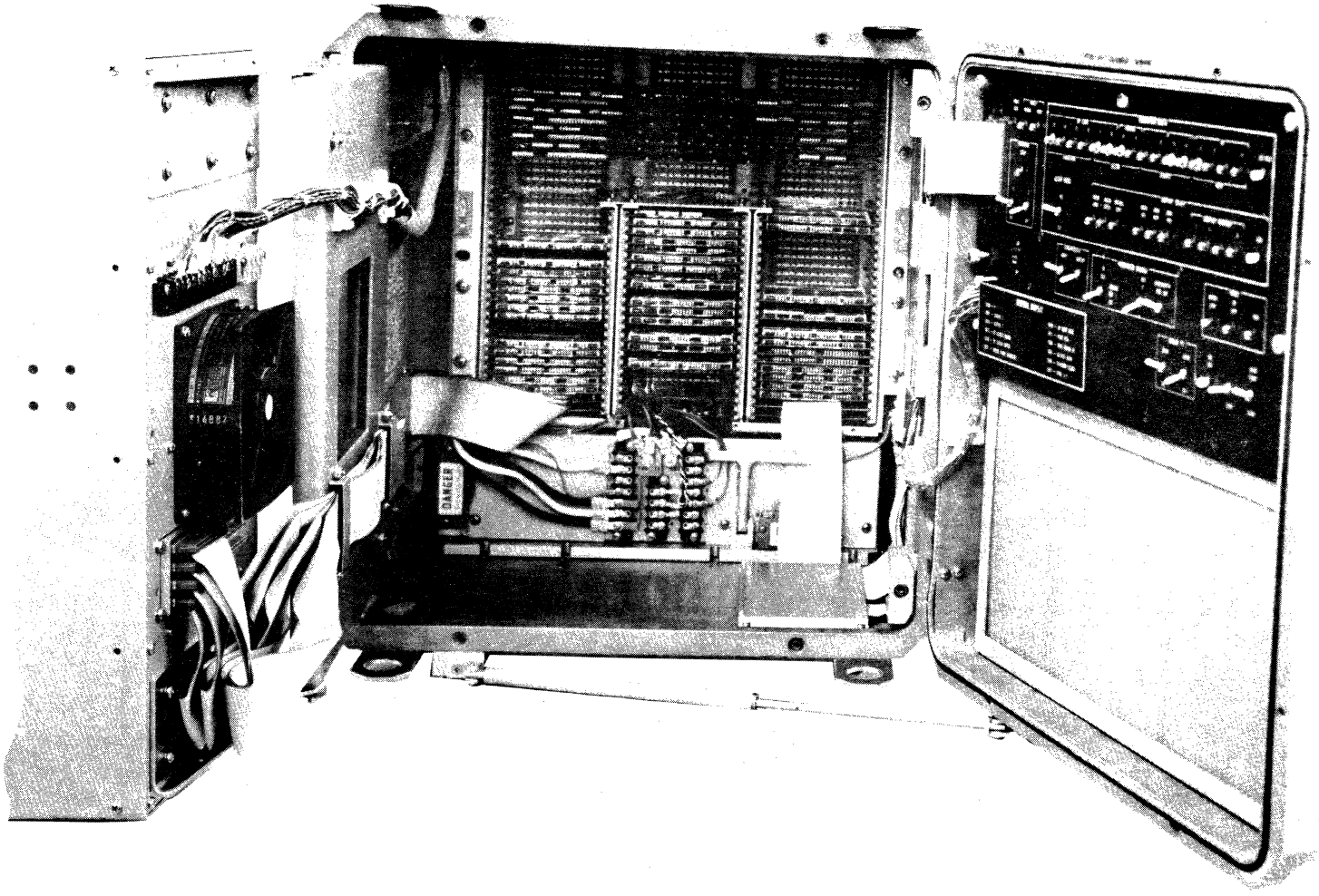


Figure 1-3. Data Processing Set, Open

the I/O connector wire wrap and the circuit card connector wire wrap. The processor/IOC chassis is variable and may contain one or more of the interface kits listed below, depending on the I/O types and interface levels required. Each kit consists of a set of circuit cards.

1) Interface Kit, Slow, MK-1693/UYK-20(V)

2) Interface Kit, Fast, Negative, MK-1694/UYK-20(V)

3) Interface Kit, Fast, Positive, MK-1695/UYK-20(V)

4) Interface Kit, Serial Synch, nomenclature not assigned.

5) Interface Kit, Serial Asynch, nomenclature not assigned.

6) Interface Kit, Fast Serial, nomenclature not assigned.

7) Interface Kit, Slow Serial Synch, nomenclature not assigned.

8) Interface Kit, Slow Serial Asynch, nomenclature not assigned.

1-34. The memory is made up of three different types of circuit boards. These are the Memory Control Board (MCB); the Memory Data Board (MDB); and the Core Memory Unit, MU-604/UYK-20(V), generally called the Memory Array Board (MAB). Each MCB contains control and addressing circuits for up to 32K of memory; each MDB contains a data register and bit drivers for up to 32K of memory; and each MAB contains an 8K x 16 bit core matrix, together with associated drivers and sense amplifiers. The memory chassis, with its full complement of two MCB and two MDB boards is designated the Control, Core Memory Unit. From one to eight Core Memory Units (MAB) are inserted into the chassis to produce the required memory capacity, from 8K to 65K words. A memory chassis containing optional MCB and MDB boards which have additional circuitry for a direct memory access (DMA) feature may be specified at time of order. According to the maintenance philosophy, faulty memory cards, like faulty processor/IOC cards, should be replaced, rather than repaired.

1-35. The power supply is a single chassis, intended for replacement rather than on-site repair. It supplies all dc power needed by the DPS. The power supply exists in six configurations, depending on the input power requirements as follows:

1) 115 Vac, 3Ø Δ , 400 Hz - PP 7032/UYK-20(V)

2) 208 Vac, 3Ø γ , 400 Hz - Nomenclature not assigned

3) 115 Vac, 1Ø, 400 Hz - Nomenclature not assigned

4) 115 Vac, 3Ø Δ , 60 Hz - Nomenclature not assigned

5) 208 Vac, 3Ø γ , 60 Hz - Nomenclature not assigned

6) 115 Vac, 1Ø, 60 Hz - Nomenclature not assigned

TO BE SUPPLIED.

Figure 1-4. Typical Single-Width Circuit Card

TO BE SUPPLIED

Figure 1-5. Typical Triple-Width Circuit Card

1-36. REFERENCE DATA.

1-37. Table 1-1 lists the features of the DPS in quick reference format.

1-38. EQUIPMENT, ACCESSORIES, AND PUBLICATIONS.

1-39. Table 1-2 lists equipment, accessories, and publications normally supplied with the DPS. (Check specific ordering document.)

1-40. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-41. Table 1-3 lists equipment not supplied with the DPS, but usually required for operation or for maintenance.

Table 1-1. Reference Data

ITEM	CHARACTERISTICS
Input Power	115 Vac ± 5%, 3 phase (delta), 115 Vac ± 7%, single phase, or 208 Vac ± 5%, 3 phase (wye); 60 Hz ± 5% or 400 Hz ± 5%; 1000 Watts max.
Internal Power	+ 5 Vdc, +.3V, -.1V, 35 Amp., max. (Logic) + 5 Vdc, ±.25V, 17.5 Amp., max. (Memory) - 5.2 Vdc, ±.3V, 10 Amp., max. + 12 Vdc, ±.6V, 1 Amp., max. + 15 Vdc, ±.3V, 12 Amp., max. - 5 Vdc, ±.4V, 1 Amp., max. - 16 Vdc, ±.8V, 2.4 Amp., max. 100 mv max. combined noise and ripple on all voltages.
Cooling	Ambient air circulated by internal blowers, cu ft/ minute maximum. Maximum heat dissipation: 3400 BTU/hr (1000 watts)
Operating Environment	Operating temperature: 32° to 122°F. (0° to 50°C) Humidity: 95% maximum without condensation Nonoperating temperature: -40° to 167°F (-62° to 75°C)
Size and Weight	Height 20 in. max.; width 19 in. max.; depth 24 in. max., not including shock pins. Weight 200 pounds maximum.
Functional Characteristics	Micro-programmed control structure 750 nsec basic cycle time Word length: 16 bits parallel 65,536 word maximum memory size 16 or 32 general registers Direct and multilevel indirect addressing Program controlled relative addressing

Table 1-1. Reference Data (Cont)

ITEM	CHARACTERISTICS
Functional Characteristics (Cont)	Real-time clock register and Interrupt clock register capable of operating from internal oscillator or external clock source. Breakpoint register; two status registers. Multiclass and multilevel interrupt processing. Running time meter. 192-word bootstrap memory Power monitoring and auto restart Up to 16 input/output channels in any combination of parallel channels in groups of four and serial channels in groups of two. Processor-initiated I/O program chain.
Parallel I/O Channel Basic Features	Processor-initiated program chain; Asynchronous; Full duplex; Buffer Control Memory; Single or Dual Channel (16-bit or 32-bit).
Parallel I/O Channel Options	Available in groups of four to total I/O complement of 16 (the channels within each 4-channel group must have the same characteristics); NTDS Parallel Slow (-15 volt) interface; NTDS Parallel Fast (-3 volt) interface; ANEW Parallel (+ 3.5 volt) interface; Intercomputer or Normal mode, any channel. ESA mode on dual channel (AN/UYK-7 compatible).

Table 1-1. Reference Data (Cont)

ITEM	CHARACTERISTICS
Parallel I/O Rates	Transfer Rates (16-bit words/second) depending on Interface Type: Number of Channels / +3.5V, -3V / -15V 1-4 / 190,000 / 41,600 5-8 / 400,000 / 83,300 9-12 / 750,000 / 124,900 13-16 / 1,000,000 / 166,600 These rates are the maximum for the specified number of active input channels or output channels. The combined transfer rates (both input and output channels active) are twice the rates specified but not greater than 1,300,000 words/second, which is the maximum I/O data handling rate. The 32-bit word transfer rates are slower due to the additional 750 nsec needed for each word to transfer the additional 16 bits to and from memory.
MIL-STD-188 Serial I/O Interface	Either asynchronous or synchronous modes. Full duplex. Buffer control memory. Available in groups of two channels. Modulation rate up to 9600 Bits/second in synchronous mode. Any four of the following bit rates (75, 150, 300, 600, 1200, or 2400) program selectable per two channel group in asynchronous mode. (Rates to be specified on order.) Program selectable character size of 5, 6, 7, or 8 bits. Capable of loopback testing (diagnostic aid). All interface lines of one channel in one connector.

Table 1-1. Reference Data (Cont)

ITEM	CHARACTERISTICS
EIA Standard RS-232 Serial I/O Interface	Either asynchronous or synchronous modes. Full duplex. Buffer control memory. Available in groups of two channels. Modulation rate up to 9600 Bits/second in synchronous mode. Any four of the following bit rates (75, 150, 300, 600, 1200, or 2400) program selectable per two channel group in asynchronous mode. (Rates to be specified on order.) Program selectable character size of 5, 6, 7, or 8 bits. Capable of loopback testing (diagnostic aid). All interface lines of one channel in one connector.
NTDS Serial I/O Interface	Asynchronous mode. Full duplex. Each group consists of one output channel and one input channel. 32-bit data word with sync bits, identifier bits, and control bits (input and output). Continuous communication between interface and peripheral equipment. Output channel - one coax cable. Input channel - one coax cable.

Table 1-2. Equipment, Accessories, and Documents Supplied

QTY PER EQUIP	NOMENCLATURE		
	NAME	DESIGNATION	PURPOSE
1	Data Processing Set	AN/UYK-20(V) or AN/UYK-20X(V)	

Table 1-3. Equipment and Publications Required But Not Supplied

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE
	NAME	DESIGNATION	
2	Technical Manual, Vol. 1	Not available	Technical documentation
	Technical Manual, Vol. 2	Not available	
	Technical Manual, Vol. 3	Not available	
1	I/O Device	Variable	Provide input and output capabilities
1	Power Cable, 3Ø or	7098772-00 or	To connect input power
	Power Cable, 1Ø	7098772-01	
Variable	Input Cable	7126392	To connect parallel I/O
Variable	Output Cable	7126393	channels, if utilized.
Variable	Serial I/O Connector	7128005-00	To connect MIL-STD-188 or RS-232 channels, if utilized.
2	I/O End-around Test Cables	7126394-00	For I/O channel testing
1	Card Extractor, Memory, Right Hand	7128052	To facilitate removal of circuit cards
1	Card Extractor, Memory, Left Hand	7128053	

Table 1-3. Equipment and Publications Required But Not Supplied (Cont)

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE
	NAME	DESIGNATION	
1	Card Extractor, Logic	7100903-00	
1	Diagnostic Program Tape	Not available	Troubleshooting

CHAPTER 2

OPERATION

2-1. INTRODUCTION.

2-2. This chapter presents information concerning the use of the control panel and the maintenance panel, and also lists the repertoire of macroinstructions and microinstructions. The control panel is located on the exterior of the DPS front access door (Control-Maintenance Unit). It contains the minimum of switches and indicators necessary for monitoring and controlling DPS operations. The maintenance panel is on the inside of the access door and is accessible only with the door opened. It permits operating in several modes at several rates, and permits inspecting and/or changing the contents of various registers.

NOTE

Operation of the DPS with the access door opened permits rf radiation.

2-3. CONTROL PANEL SWITCHES AND INDICATORS.

2-4. Figure 2-1 shows the control panel. Table 2-1 describes the panel's switches and indicators.

2-5. MAINTENANCE PANEL SWITCHES AND INDICATORS.

2-6. Figure 2-2 shows the maintenance panel. Table 2-2 describes the panel's switches and indicators. Table 2-3 describes the maintenance panel display select codes.

2-7. OPERATING PROCEDURES.

2-8. TURN-ON PROCEDURE.

1. Operate switches on control panel and maintenance panel to initial settings per table 2-4.

2. Operate CIRCUIT BREAKER ON/OFF switch to ON position.

3. Operate POWER, BLOWER ON/OFF switch to ON position. Observe that POWER, BLOWER indicator lights and that blowers operate to discharge air from three exhaust grills on side of cabinet.

4. Operate POWER, LOGIC ON/OFF switch to ON position. Observe that POWER, LOGIC indicator lights and that FAULT, POWER and OVER TEMP indicators do not light.

NOTE

Turning on power places the DPS in a master cleared state with Run mode selected.

2-9. TURN-OFF PROCEDURE. Depress STOP and reverse above procedure, first turning off POWER, LOGIC, then POWER, BLOWER, and finally CIRCUIT BREAKER.

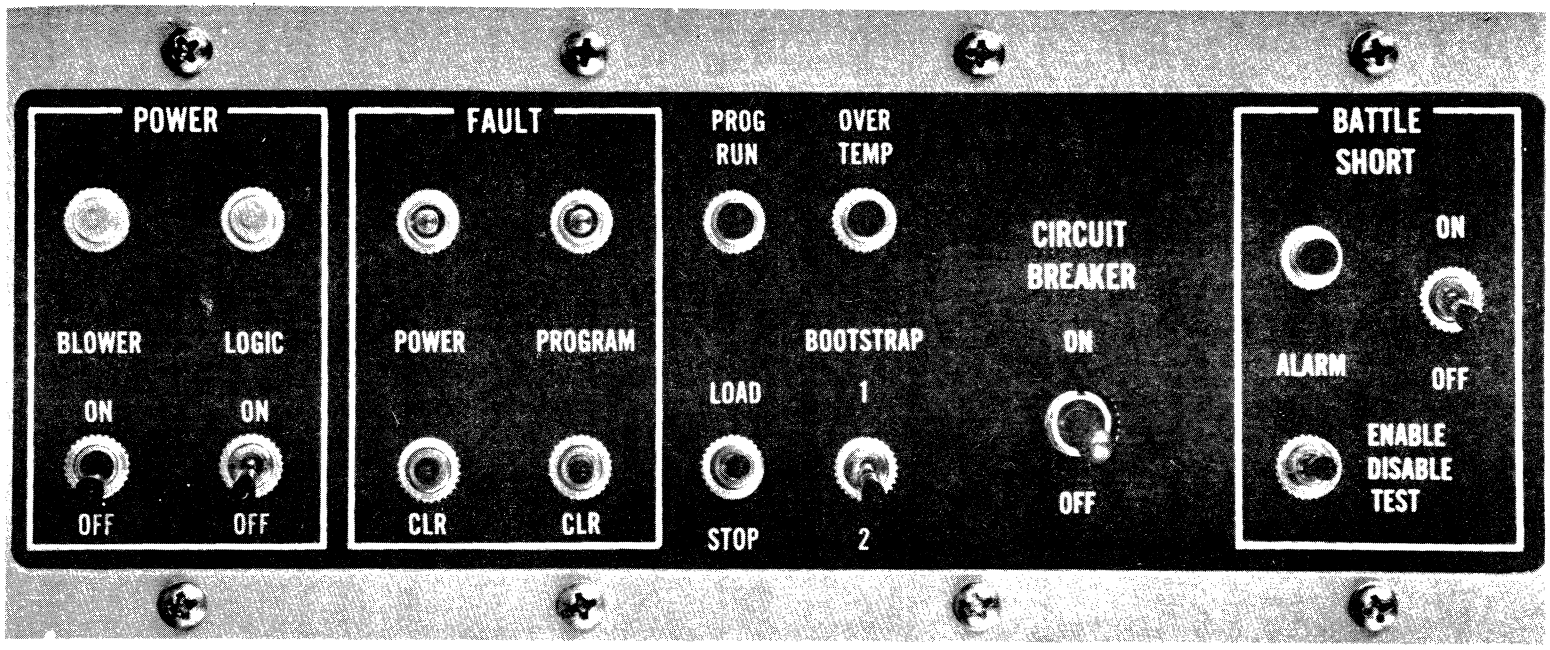


Figure 2-1. Control Panel

TABLE 2-1. CONTROL PANEL SWITCHES AND INDICATORS

IDENTIFICATION	TYPE	FUNCTION
CIRCUIT BREAKER ON/OFF	Two-position toggle switch	ON position enables primary power to the DPS. OFF position disables primary power to the DPS.
BLOWER POWER ON/OFF	Two-position toggle switch	ON position enables power to the DPS cooling fans and enables LOGIC POWER ON/OFF switch function. OFF position disables power to the DPS cooling fans and disables LOGIC POWER ON/OFF switch function.
BLOWER POWER	Indicator (neon with white lens)	When lit, indicates blower power is applied.
LOGIC POWER ON/OFF	Two-position toggle switch	ON position enables power to the dc power supply. OFF position disables power to the dc power supply.
LOGIC POWER	Indicator (incandescent with white lens)	When lit, indicates dc power is applied.
POWER FAULT	Indicator	When lit, indicates a Power Fault Interrupt has occurred.
POWER FAULT CLR	Two-position return-to-neutral toggle switch	When momentarily operated to the CLR position, clears the POWER FAULT indicators on both the control panel and the maintenance panel.
PROGRAM FAULT	Indicator (red LED with clear lens)	When lit, indicates a Program Fault Interrupt has occurred, caused by attempting to execute an illegal instruction.
PROGRAM FAULT CLR	Two-position return-to-neutral toggle switch	When momentarily operated to the CLR position, clears the PROGRAM FAULT indicator on the control panel and the PROG FAULT indicator on the maintenance panel.
PROG RUN	Indicator (green LED with green lens)	When lit, indicates DPS is executing instructions in Run Mode.

TABLE 2-1. CONTROL PANEL SWITCHES AND INDICATORS (CONT)

IDENTIFICATION	TYPE	FUNCTION
OVER TEMP	Indicator (neon with red lens)	When lit, indicates DPS internal cabinet air temperature is within 25^{o} F of the maximum temperature at which the DPS can operate without component damage.
ALARM	Audible	This alarm sounds if the ALARM ENABLE/DISABLE/TEST switch is in the ENABLE position and the internal cabinet air temperature is within 25^{o} F of the maximum temperature at which the DPS can operate without component damage.
ALARM ENABLE/DISABLE/TEST	Three-position toggle switch	ENABLE position enables the audible alarm function. DISABLE position disables the audible alarm function. TEST position causes the audible alarm to sound and the OVER TEMP indicator to light.
BATTLE SHORT ON/OFF	Two-position toggle switch	ON position disables DPS over-temperature shutdown function. OFF position enables DPS over-temperature shutdown function.
BATTLE SHORT	Indicator (neon with red lens)	When lit, indicates BATTLE SHORT switch is in the ON position.
BOOTSTRAP 1-2	Two-position toggle switch	Selects one of two possible bootstrap programs in the NDRO memory. Operates in conjunction with the Op Code = 40RR, a = 7 Conditional Jump macro-instruction and may be used, at programmer's discretion, to control branching in other programs.
LOAD/STOP	Three-position return-to-neutral toggle switch	When momentarily operated to the LOAD position, causes the DPS to execute a master clear, select Run mode, then begin executing the bootstrap program selected by the BOOTSTRAP 1-2 switch. When momentarily operated to the STOP position, causes the DPS to stop executing instructions if the computer is in the Run mode.

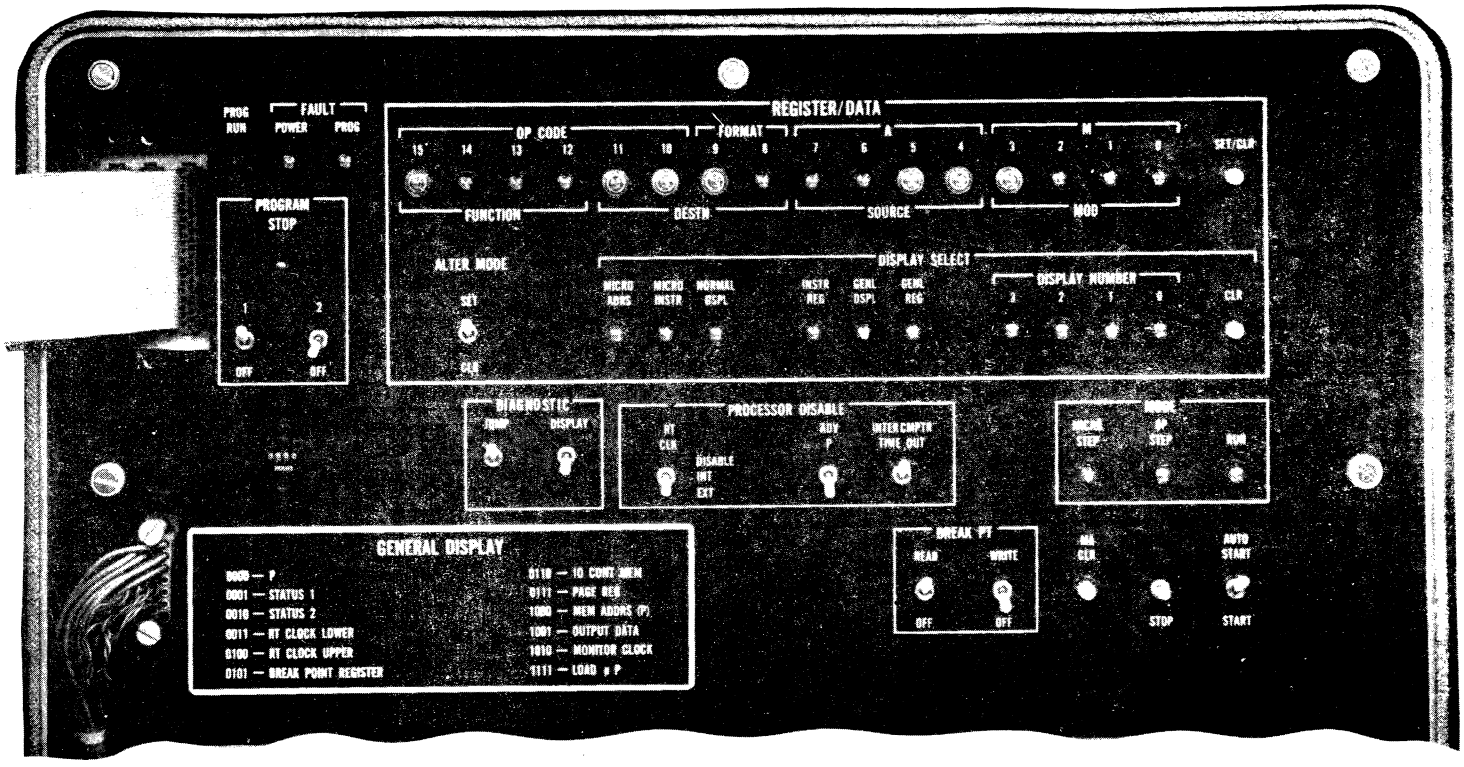


Figure 2-2. Maintenance Panel

TABLE 2-2. MAINTENANCE PANEL SWITCHES AND INDICATORS

IDENTIFICATION	TYPE	FUNCTION
AUTO START/START	Three-position toggle switch	When set to the AUTO START position, causes the DPS to begin executing instructions at NDRO bootstrap memory address 000000 when power is applied or is restored after a power failure. When momentarily operated to the START position, causes the DPS to begin executing instructions in the mode selected.
STOP	Two-position return-to-neutral toggle switch	When operated to the STOP position while the DPS is executing instructions in the Run mode, causes the DPS to stop executing macroinstructions.
MA CLR	Pushbutton switch	When operated while the DPS is not in Run condition, the DPS resets to a master cleared state*. When operated while the DPS is in the Run mode, clears the FAULT indicators on the control and maintenance panels.
BREAK PT READ/OFF	Two-position toggle	READ position causes the DPS to stop executing instructions after reading data from the memory address specified by the contents of the breakpoint register. OFF position disables the read stop.
BREAK PT WRITE/OFF	Two-position toggle	WRITE position causes the DPS to stop executing instructions after writing data in the memory address specified by the contents of the breakpoint register. OFF position disables the write stop.
PROG RUN	Indicator-switch (green LED with green lens)	Indicator function: When lit, indicates the DPS is executing instructions in the Run mode. Switch function: Selects run condition in microstep mode.

* Master Cleared State: P register, status register #1, and status register #2 cleared; real time clock and monitor clock disabled; page registers set equal to their own address; I/O channels cleared as specified for the 70RR, m = 0 macroinstruction, and Normal Display selected.

TABLE 2-2. MAINTENANCE PANEL SWITCHES AND INDICATORS (CONT)

IDENTIFICATION	TYPE	FUNCTION
POWER FAULT	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates a Power Fault Interrupt has occurred. Switch function: When operated clears the POWER FAULT indicators on both the operator's control panel and the maintenance panel.
PROG FAULT	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates a Program Fault Interrupt has occurred caused by attempting to execute an illegal instruction. Switch function: When operated, clears the PROGRAM FAULT indicator on the operator's control panel and the PROG FAULT indicator on the maintenance panel.
PROGRAM STOP	Indicator (red LED with clear lens)	When lit, indicates a programmed stop has been executed. (40RR, A = 11, 12, or 13.)
PROGRAM STOP 1/OFF	Two-position toggle switch	In 1 position, causes a program stop when the DPS executes a jump macro-instruction (40RR with an A-value = 12.
PROG STOP 2/OFF	Two-position toggle switch	In 2 position, causes a program stop when the DPS executes a jump macro-instruction (40RR) with an A-value = 13.
Time meter	4 digit, 0000 to 9999	Records accumulated hours that dc power has been applied.
DIAGNOSTIC JUMP	Two-position toggle switch	In the JUMP position, enables branching on the F = 14, M = 17 Branch micro-instruction. Its usage causes the DPS to jump from the operating micro-program. When used in connection with NORMAL DSPL, GENL DSPL, DISPLAY NUMBER = 1111, and MICRO STEP it enables manual loading of the micro P register. (See paragraph 2-XX.)

TABLE 2-2. MAINTENANCE PANEL SWITCHES AND INDICATORS (CONT)

IDENTIFICATION	TYPE	FUNCTION
DIAGNOSTIC DISPLAY	Two-position toggle switch	In the DISPLAY position while the DPS is in the Microstep mode. a. With MICRO ADRS set, REGISTER/ DATA displays the address of the next microinstruction to the executed. b. With MICRO INSTR set, REGISTER/ DATA displays the microinstruction currently being executed. c. With NORMAL DSPL set, REGISTER/ DATA displays the data on the source bus.
PROCESSOR DISABLES: RT CLK DISABLE/INT/EXT	Three-position toggle switch	DISABLE position inhibits incrementing of the Realtime Clock Register and decrementing of the Monitor Clock register. INT position causes the Realtime-Clock Register and the Monitor Clock register to use the internal clock source for timing. EXT position causes the Realtime Clock Register and the Monitor Clock register to use the external clock source for timing.
PROCESSOR DISABLES: ADV P	Two-position toggle switch	Up position inhibits incrementing of the P-Register, thus causing the DPS to repeatedly perform one 16-bit macroinstruction.
PROCESSOR DISABLES: INTERCMPTR TIME OUT	Two-position toggle switch	Up position inhibits the occurrence of a Class III Intercomputer Timeout Interrupt.
MODE: MICRO STEP	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates DPS is in Microstep mode to execute a single microinstruction. (To clear, depress DISPLAY SELECT CLR switch.) Switch function: When operated, places DPS in Microstep mode.

TABLE 2-2. MAINTENANCE PANEL SWITCHES AND INDICATORS (CONT)

IDENTIFICATION	TYPE	FUNCTION
MODE: OP STEP	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates DPS is in Op Step mode or in Microstep mode to execute a single macroinstruction. Switch function: When operated, clears Run mode and places DPS in Op Step mode, to execute one macroinstruction per operation of the START switch.
MODE: RUN	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates DPS is in Run mode or in Microstep mode to execute successive instructions. Switch function: When operated, clears Op Step mode and enables the Run mode.
DISPLAY SELECT CLR	Pushbutton switch	When operated, clears DISPLAY NUMBER 0 through 3 and clears the Microstep mode.
ALTER MODE SET/CLEAR	Two-position toggle switch	In the SET position, a. Causes individual bit of register being displayed to set when corresponding REGISTER/DATA indicator switch is operated. b. Causes all bits of register being displayed to clear when REGISTER/DATA SET/CLR switch is operated. In the CLEAR position, a. Causes individual bit register being displayed to set when corresponding REGISTER/DATA indicator switch is operated. b. Causes all bits of register being displayed to clear when REGISTER/DATA SET/CLR switch is operated.
REGISTER/DATA SET/CLR	Pushbutton switch	When operated, sets or clears the register being displayed in REGISTER/DATA indicator switches 0 through 15, dependent on ALTER MODE SET/CLEAR position.

TABLE 2-2. MAINTENANCE PANEL SWITCHES AND INDICATORS (CONT)

IDENTIFICATION	TYPE	FUNCTION
REGISTER/DATA 0 through 15	Indicator-switches (red LED with clear lens)	Indicator function: Display contents of selected register. Switch function: Modify contents of selected register.
DISPLAY SELECT: MICRO ADRS MICRO INSTR NORMAL DSPL INSTR REG GENL DSPL GENL REG DISPLAY NUMBER 0-3	Indicator- switches (red LED with clear lens)	Indicator function: When lit as specified in table 2-3, indicate REGISTER/DATA is displaying the corresponding register. Changing the contents of REGISTER/DATA changes the contents of the register being displayed. Switch function: When operated as specified in table 2-3, causes REGISTER DATA to display the corresponding register contents. Operation of any one of MICRO ADRS, MICRO INSTR, or NORMAL DSPL causes the other two to clear. Operation of any one of INSTR REG, GENL DSPL, or GENL REG causes the other two to clear.

TABLE 2-3. DISPLAY SELECT CODES

MICRO ADRS	MICRO INSTR	NORMAL DSPL	INSTR REG	GENL DSPL	GENL REG	DISPLAY NUMBER 3	2	1	0	REGISTER SELECTED
1	0	0	X	X	X	X	X	X	X	μP Register (should be in Microstep mode). (Note 2)
0	1	0	X	X	X	X	X	X	X	μI Register (should be in Microstep mode). (Note 2)
0	0	1	1	0	0	X	X	X	X	Instruction Register
0	0	1	0	1	0	0	0	0	0	P Register
0	0	1	0	1	0	0	0	0	1	Status Register #1
0	0	1	0	1	0	0	0	1	0	Status Register #2
0	0	1	0	1	0	0	0	1	1	RTC Register, Lower 16 Bits
0	0	1	0	1	0	0	1	0	0	RTC Register, Upper 16 Bits
0	0	1	0	1	0	0	1	0	1	Breakpoint Register
0	0	1	0	1	0	0	1	1	0	I/O Control Memory (Note 1)
0	0	1	0	1	0	0	1	1	1	Page Register (I Reg_{0-5} selects register)
0	0	1	0	1	0	1	0	0	0	Memory Address (P selects address)
0	0	1	0	1	0	1	0	0	1	Output Data (I Reg A-field selects channel)
0	0	1	0	1	0	1	0	1	0	Monitor Clock Register (Note 2)
0	0	1	0	1	0	1	1	1	1	Load μP (Note 3)
0	0	1	0	0	1	0	0	0	0	General Register R0
0	0	1	0	0	1	0	0	0	1	General Register R1
0	0	1	0	0	1	0	0	1	0	General Register R2
0	0	1	0	0	1	0	0	1	1	General Register R3
0	0	1	0	0	1	0	1	0	0	General Register R4
0	0	1	0	0	1	0	1	0	1	General Register R5
0	0	1	0	0	1	0	1	1	0	General Register R6
0	0	1	0	0	1	0	1	1	1	General Register R7
0	0	1	0	0	1	1	0	0	0	General Register R10
0	0	1	0	0	1	1	0	0	1	General Register R11
0	0	1	0	0	1	1	0	1	0	General Register R12
0	0	1	0	0	1	1	0	1	1	General Register R13
0	0	1	0	0	1	1	1	0	0	General Register R14
0	0	1	0	0	1	1	1	0	1	General Register R15
0	0	1	0	0	1	1	1	1	0	General Register R16
0	0	1	0	0	1	1	1	1	1	General Register R17

(Note 4)

Note 1: I Reg A-field selects channel, M-field selects word.
Note 2: May be displayed, but cannot be changed.
Note 3: See paragraph 2-XX for load μP procedure.
Note 4: Status Reg #1 bit 14 = 0, selects gen. reg. set 1.
Status Reg #1 bit 14 = 1, selects gen. reg. set 2.

TABLE 2-4. INITIAL SWITCH POSITIONS

SWITCH	POSITION
Control Panel	
POWER-BLOWER ON/OFF	OFF
POWER-LOGIC ON/OFF	OFF
BOOTSTRAP-LOAD/STOP	Neutral (center)
BOOTSTRAP-1/2	1
CIRCUIT BREAKER ON/OFF	OFF
BATTLE SHORT ON/OFF	OFF
ALARM ENABLE/DISABLE/TEST	ENABLE
Maintenance Panel	
PROG STOP 1/OFF	OFF
PROG STOP 2/OFF	OFF
ALTER MODE SET/CLR	SET
DIAGNOSTIC JUMP	Down
DIAGNOSTIC DISPLAY	Down
RT CLK DISABLE/INT/EXT	DISABLE
PROCESSOR DISABLE INTERCMPTR TIME OUT	Down
PROCESSOR DISABLE ADV P	Down
BREAK PT READ/OFF	OFF
BREAK PT WRITE/OFF	OFF
AUTO START/START	Neutral (center)

2-10. MODE SELECTION. The DPS has three basic modes of operation. Run mode is the normal high speed operating mode. An Op Step mode and a Micro Step mode are provided for their usefulness in troubleshooting.

2-11. Run Mode. Run mode is selected automatically during an initial power-on or during an auto start after a power interruption. It may also be selected manually. With Run mode selected, without Micro Step mode selected operation of the control panel LOAD/STOP switch to the LOAD position or operation of the maintenance panel AUTO START/START switch to the START position causes the DPS to begin executing instructions at its normal rate. To stop operate the control panel LOAD/STOP switch to the position or operate the maintenance panel STOP switch. In the stopped condition, in either Run mode or OP Step mode, the MPC cycles the console mode microprogram subroutine to permit monitoring and changing register contents.

2-12. Op Step Mode. Selecting OP STEP clears RUN, and vice versa. In Op Step mode, the DPS executes one macroinstruction per operation of the maintenance panel AUTO START/START switch to the START position.

NOTE

In Op Step mode, the macroinstruction is completed before stopping. In some cases, the instruction register is modified during execution. Example: In Load Multiply macroinstructions, the A-field is incremented to equal M = 1 before stopping.

2-13. Micro Step Mode. With MICRO STEP selected, the DPS executes one microinstruction at a time from the internal micro program. This permits stepping through instructions and observing the actions resulting from each micro step. In Micro Step mode, the contents of the micro P register, the microinstruction register, or the source bus can be displayed, but the contents of other registers cannot be displayed or changed because the MPC cannot cycle the console mode microprogram subroutine. With MICRO STEP, RUN mode, and PROG RUN selected, the DPS performs one microinstruction per operation of the START switch. When the micro steps associated with one macroinstruction have been completed, continued operation of the START switch causes micro stepping through the next macroinstruction. With MICRO STEP OP STEP and PROG RUN selected, each operation of the START switch also executes one microinstruction. However, when the first macroinstruction is completed, continued operation of the START switch causes microstepping of the console mode microprogram subroutine.

2-14. PROGRAM LOAD PROCEDURE.

1. Turn on DPS per paragraph 2-8.

2. Ascertain that the loading device (eg. paper tape unit, magnetic tape unit, etc.) is ready for operation.

3. Set BOOSTRAP 1, 2 switch on control panel to select correct bootstrap load program.

4. Momentarily operate LOAD/STOP switch on control panel to LOAD position. This master clears the DPS initializing it for executing the NDRO bootstrap program, then starts operation.

2-15. PROGRAM STARTING AND STOPPING. If the macro program to be run is already contained in the main memory, insert the program's starting address into the P Register through the REGISTER/DATA as described above. Then operate the START switch. The PROG RUN indicator will light, inidcating that the program is being run. A program may terminate with a STOP instruction, stopping the computer automatically. More likely, it will terminate with a jump instruction turning control of the DPS over to a continuously running executive macro program (often called operating system). In either case, the DPS can be stopped manually at any time by operating the STOP switch to the STOP position.

2-16. MASTER CLEARING (RESETTING). To reset to the initial starting condition, stop the DPS and press the MA CLR switch. When in the Run condition, only the fault flip flops and their indicators clear; all other functions of the master clear are disabled to prevent accidental destruction of program or data.

2-17. BREAKPOINT OPERATION. The breakpoint feature allows an operator to stop DPS operation at any preselected address. This feature is useful for troubleshooting and for debugging programs. To use the breakpoint register, proceed as follows:

1. Depress the STOP switch.

2. Select NORMAL DSPL and GENL DSPL. Set DISPLAY NUMBER indicator-switches to 0101.

3. Insert desired address into REGISTER/DATA indicator-switches.

4. Set BREAKPOINT READ and WRITE switches to enable stopping on a memory read operation only, write operation only, or both.

5. Select RUN mode and operate START switch.

NOTE

DPS executes instruction at selected address before stopping. If address contains a jump instruction, jump will already be performed, making its origin traceable. Therefore, breakpoint address should usually be one less than desired address, so DPS will stop ready to read and execute that instruction.

2-18. MONITORING OR CHANGING REGISTER CONTENTS. Select the register to be displayed per table 2-3. Whenever the DPS is stopped in OP Step or Run modes, the selected register is displayed in REGISTER/DATA, and can be altered by inserting new data into the REGISTER/DATA indicator-swtiches, except as noted in the table. The micro P and microinstruction registers and the contents of the source bus can be displayed in Micro Step mode, with DIAGNOSTIC DISPLAY and MICRO ADRS, MICRO INSTR, or NORMAL DSPL selected, respectively, but cannot be changed. Detailed procedures are presented for changing the contents of a memory address (paragraph 2-19) or of micro P (paragraph 2-21).

2-19. MEMORY MODIFICATION PROCEDURE. This is an "inspect and change" procedure for inspecting and/or changing the contents of a main memory address.

1. Depress STOP switch.

2. Select NORMAL DSPL and GENL DSPL. Set DISPLAY NUMBER indicator-switches to 0000.

3. Set REGISTER/DATA indicator-switches to the desired memory address.

4. Set DISPLAY NUMBER indicator-switches to 1000. Existing contents of that memory address will appear in REGISTER/DATA.

5. To modify the contents of the selected memory address, insert the new data into the REGISTER/DATA.

2-20. MANUAL PROGRAM LOAD OR INSPECT PROCEDURE. If several addresses must be inspected or changed, or if a small program must be stored, it is convenient to use the Inspect and Change Routines of the Utility Programs (UPAK) or the following program:

```
000502) 01 0 02 01    LR (R1) → R2
000503  05 1 00 01    LXI R1 → R0, (R1) + 1 → R1
000504) 40 2 11 00    JS STEP, Jump to Address 000506
000505) 000506
000506) 11 1 00 02    SI (R0) → (R2)
000507) 40 1 373      LJ Jump to Address 000502
```

To use this program perform the following procedure:

1. Load the program in address 000502 - 000507 using the procedures outlined in paragraph 2-14.

2. Load 000502 into the P REGISTER.

3. Press RUN MODE.

4. Set GENERAL REGISTER 1 to the address to be inspected.

5. Select GENERAL REGISTER 0.

6. Press the START switch twice. The contents of the first address to be inspected should be shown in REGISTER/DATA.

7. If it is desired to change the information, clear REGISTER/DATA and set the new contents into it.

NOTE

If the address to be inspected next is not the next consecutive address, clear the P register and set it to the address desired before performing step 8.

8. Press the START switch. The new word (or old if not changed) is now stored in memory, and the contents of the next adjacent address is displayed in the REGISTER DISPLAY.

9. Repeat steps 7 and 8 until all addresses desired are inspected/changed.

2-21. LOAD MICRO P PROCEDURE. When debugging programs, or when manually troubleshooting the DPS, it may be useful to reach a particular micro memory address. The following procedure loads the address into the micro P register:

1. Depress STOP switch.

2. Select NORMAL DSPL and GENL DSPL. Set DISPLAY NUMBER indicator-switches to 1111.

3. Select MICRO STEP mode, MICRO ADRS, DIAGNOSTIC DISPLAY, and PROG RUN.

4. Operate DIAGNOSTIC JUMP toggle switch to up position.

5. Operate START switch repeatedly until selected address appears in REGISTER/DATA. (It may be necessary to step a number of times to complete the microprogram subroutine before micro P is loaded.) When selected address appears in micro P, the next operation of the START switch will perform the microinstruction at that address.

6. To step through successive microinstructions following the selected address, proceed per steps 4, 6, and 7 of paragraph 2-23.

NOTE

To start the microprogram running from a particular microinstruction, perform steps 1, 2, and 4, select RUN mode, and depress START switch.

2-22. OP STEP PROCEDURE. Proceed as follows to perform one macroinstruction at a time:

1. Depress STOP switch.

2. Load desired main memory address into P register by selecting NORMAL DSPL and GENL DSPL, setting DISPLAY NUMBER indicator-switches to 0000, and inserting address into REGISTER/DATA indicator-switches.

3. If necessary, insert required data into general registers and memory addresses that will be used by the macroinstruction.

4. Select OP STEP mode.

5. To keep repeating the same macroinstruction, operate PROCESSOR DISABLES ADV P switch to the up position. (This is usable only for RR and RI format macroinstructions; RK and RX require P to advances to obtain the second half of the instruction.)

6. Depress START switch for each instruction execution.

2-23. MICRO STEP PROCEDURE. Proceed as follows to step through a macroinstruction, performing one microinstruction at a time:

1. Depress STOP switch.

a. If the desired macroinstruction is contained in main memory, set its address into P register by selecting NORMAL DSPL and GENL DSPL, setting DISPLAY NUMBER indicator-swiches to 0000, and inserting address into REGISTER/DATA indicator-switches.

b. If the desired macroinstruction is not in main memory, load it at a convenient address per paragraph 2-19.

c. If desiring to start at a certain microinstruction, load its micro memory address into micro P register per paragraph 2-21.

2. Select MICRO STEP.

3. Select LIAGNOSTIC DISPLAY and:

a. MICRO ADRS to display the address of the next microinstruction to be performed.

b. MICRO INSTR to display the microinstruction being executed, or

c. NORMAL DSPL to display the data on the source bus.

4. Select DIAGNOSTIC JUMP and depress PROG RUN indicator-switch.

NOTE

If RUN mode is selected, DPS will micro step through successive macroinstructions. If OP STEP mode is selected, DPS will micro step to completion of first macroinstruction, then begin micro stepping through console mode micro program subroutine.

5. Depress START switch for each micro step.

6. At completion of micro step sequence, clear MICRO STEP by depressing DISPLAY SELECT CLR switch, and extinguish PROG RUN by selecting OP STEP.

2-24. EMERGENCY OPERATION. A BATTLE SHORT switch on the control panel disables the overtemperature shutdown function, thus permitting the DPS to continue operating in an emergency situation.

2-25. EMERGENCY TURN-OFF. For fast turn-off in an emergency, set the CIRCUIT BREAKER ON/OFF switch to OFF. The DPS will accomplish an orderly shutdown internally, generating a power fault interrupt and storing essential register. Before turning CIRCUIT BREAKER on again set POWER LOGIC and BLOWER switches to OFF.

2-26. MICROINSTRUCTIONS

2-27. The microinstruction repertoire is shown in table 2-5. The repertoire consists of 16 basic microinstructions with many variations. The basic microinstruction format is divided into four 4-bit fields. The F-field, bits 15-12, specifies the function to be performed such as add, subtract, shift, etc. The D-field, bits 11-8, defines the register or network to receive the data on the destination bus. Table 2-6 lists the destinations. Destination 1 (D1) or Destination 2 (D2) is determined by the F-field or M-field for each microinstruction. The S-field, bits 7-4 (sometimes also called the O or origin field), defines the register 1 (S1) or Source 2 (S2) is determined by the F-field or M-field for each microinstruction. The M-field, bits 3-0, modifies the microinstruction. Some microinstructions use special fields of K (constant), X (12-bit address), or F2 (extension of F-field). Appendix A describes each microinstruction in detail.

2-28. MACROINSTRUCTIONS.

2-29. INSTRUCTION FORMATS. The DPS performs instructions using five instruction word formats. Instructions may be single length or double length.

2-30. Format RR. The Format RR instructions are single length and use the format shown in figure 2-3. They perform operations using the general registers. (RR = Register and Register.) Unless otherwise specified in an individual instruction, the a-designator selects the R_a register, and the m-designator selects the R_m register.

2-31. Format RI. The Format RI instructions are also single length. They may be either Type 1 or Type 2. The Format RI Type 1 instructions use the format shown in figure 2-4. Y is generated using the x and d-designators as specified in figure 2-5. Format RI Type 2 instructions use the format shown in figure 2-3. They perform operations using the general registers and a memory reference. (RI = Register and Immediate Memory.) Unless otherwise specified in an individual instruction, the a-designator selects the R_a register, and the m-designator selects the R_m register whose contents shall be used as a memory address Y.

2-32. Format RK. Format RK instructions are double length, consisting of two words stored in consecutive memory addresses. The first word uses the format shown in figure 2-3. The second word is a 16-bit quantity designated y. The Format RK instructions perform operations using general register and memory references. (RK = Register and Constant (Immediate Operand).) Unless otherwise specified in an individual instruction, the a-designator selects the R_a register, and the m and

TABLE 2-5. MICROINSTRUCTION REPERTOIRE

INSTRUCTION FORMAT				DESCRIPTION
15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
F = 0	D	S	M	Transfer
F = 1	X (12 Bits)			Unconditional Branch
F = 2	D	S	M	Add S2
F = 3	D	S	M	Shift
F = 4	D	S	M	Add S1
F = 5	D	S	M	Subtract
F = 6	D	S	M	Logic I
F = 7	D	S	M	Logic II
F = 10	D	K		Add constant
F = 11	D	K		Subtract constant
F = 12	D	K		Transfer constant to D1
F = 13	D	K		Transfer constant to D2
F = 14	F2	K		Branch
F = 15	F2	S	M	Micro control
F = 16	F2	K		Micro repeat
F = 17	D	S	M	Emulate

TABLE 2-6. D-DESIGNATOR

D VALUE	DESTINATION 1 (D1)	DESTINATION 2 (D2)
0	Unassigned	μP register
1	Breakpoint	Condition register
2	P Register	Display register
3	Memory Data register	Cycle counter
4	General register	RTC Upper
5	Status register #1	Unassigned
6	Status register #2	Unassigned
7	RTC Lower	Unassigned
10	A0/Shift Register Upper/Page Address Counter	Page Table
11	A1/Shift Register Lower	Unassigned
12	A2	Instruction register/SGR
13	A3	SGR
14	A4	I/O Control Memory Translator
15	A5	I/O Translator
16	A6/Shift Counter	Output Data
17	A7/MAR	I/O Control Memory

TABLE 2-7. S-DESIGNATOR

S VALUE	SOURCE 1 (S1)	SOURCE 2 (S2)
0	Unassigned	μP Hold Register
1	Breakpoint	Condition Register
2	P Register	Display Register
3	Memory Data Register	Normalize/Panel Select
4	Page Table	RTC Upper
5	IA Pointer	STATUS 1 Register
6	Shift Matrix Output	STATUS 2 Register
7	Monitor Clock/Part Prod/Feed	RTC Lower
10	A0	General Register
11	A1	Cordic Table
12	A2	Instruction Register With AM-Field Sign Extension
13	A3	Instruction Register
14	A4	Class I & II Interrupt Codes
15	A5	Class III Interrupt Codes/ I/O Translator
16	A6	Input Data
17	A7	I/O Control Memory

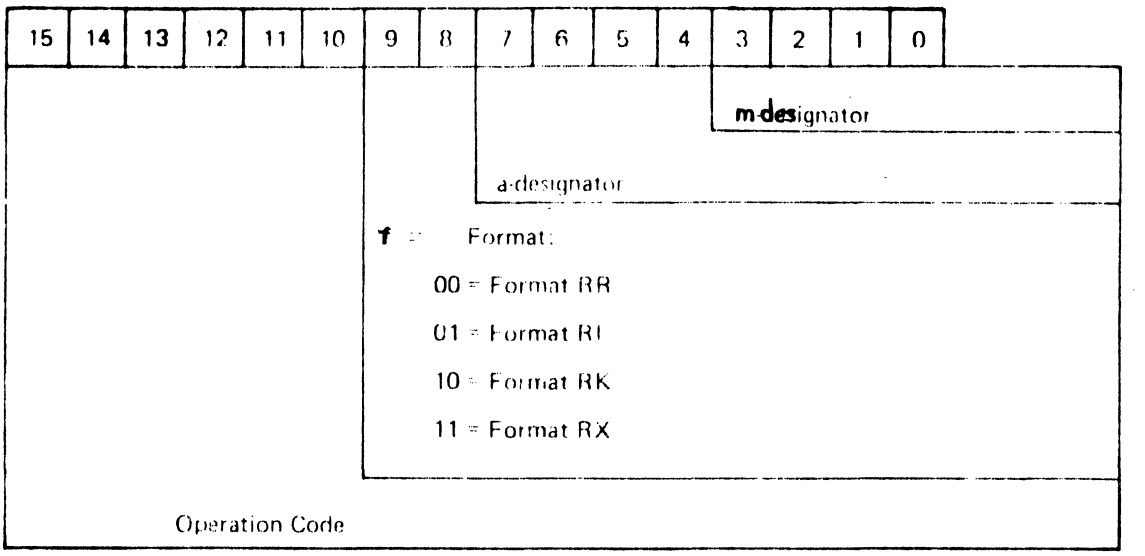


Figure 2-3. Basic Instruction Word Format

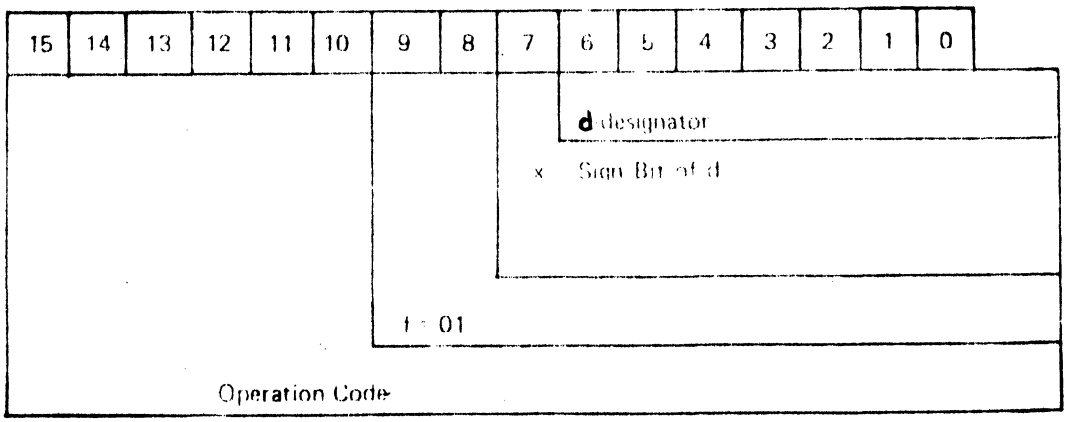


Figure 2-4. Instruction Word Format for Format RI Type 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	1	0	0	1	1	0	1	0	1	1	0	0	1	Contents of P*
X	(Sign Extended)						X		0	0	0	0	0	0	1	d-designator from the instruction word.
																Y shall be the sum of (P) and d as follows:
0	0	0	1	0	0	1	1	0	1	0	1	1	0	1	0	(P) + d when x = 0 (Positive)
0	0	0	1	0	0	1	0	1	1	0	1	1	0	1	0	(P) + d when x = 1 (Negative)

* After normal incrementation resulting from instruction fetch.

Figure 2-5. Address Generation Example for Format RI Type 1 Instruction

y designators are used to form an operand (a 16-bit signed literal or constant) or a memory address, designed Y. Y is formed as follows:

1) When m equals zero, Y is equal to y.

2) When m does not equal zero, Y is the sum of the contents of R_m and Y. The m-designator selects the R_m register.

2-33. Format RX. The Format RX instructions are double length, consisting of two words stored in consecutive memory addresses. The first word uses the format as specified in figure 2-3. The second word is a 16-bit quantity designated y. The Format RX instructions perform either whole word (16-bit) or byte (8-bit) operations using the general registers and memory references as specified in the following subparagraphs. (RX = Register and memory with or without indexing).

2-34. When the Format RX instruction designates whole word operations, the a, m and y-designators are used as follows, unless otherwise specified in an individual instruction:

1) The a-designator selects the R_a register.

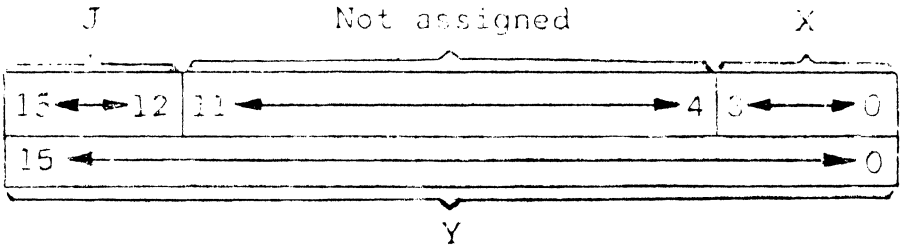
2) The m and y-designators form a memory address designated Y as follows:

a) When m equals zero, Y is equal to y and is a direct memory reference.

b) When m is not equal to 0, 10, 12, 14, or 16 or when m equals 10, 12, 14, or 16 and the 2-bit field of status register #2 corresponding to the particular R_m register is equal to 0 or 1, Y is the sum of the contents of R_m and y is a direct memory reference.

c) When m equals 10, 12, 14, or 16 and the 2-bit field of Status Register #2 corresponding to the particular R_m register is equal to 2, Y is the contents of y and is an address pointer to the first word of a two word indirect memory reference. Figure 2-6 specifies IW word formats and interpretation for indirect addressing.

d) When m equals 10, 12, 14, or 16 and the 2-bit field of status register #2 corresponding to the particular R_m register is equal to 3, Y is the sum of the contents of R_m and y and is an address pointer to the first word of a two word indirect memory reference. Figure 2-6 specifies IW word formats and interpretation for indirect addressing.



J VALUE	ADDRESS DETERMINATION
0	Final operand at Y
1	Final operand at Y + R_X
2	Final operand at Y + R_m
3	Final operand at Y + R_{m+1}
4	Cascaded IW at Y
5	Cascaded IW at Y + R_X
6	Cascaded IW at Y + R_m
7	Cascaded IW at Y + R_{m+1}
10-17	Unassigned

Figure 2-6. Indirect Address Format

2-35. When the Format RX instruction designates byte operations, the a, m and y-designators are used as follows, unless otherwise specified in an individual instruction:

1) The a-designator selects the R_a register.

2) When m does not equal zero, the m-designator selects a General Register designated R_m. The contents of R_m are used to form a memory address designated Y and a byte position in the memory location as follows:

a) The least significant bit (LSB) of the contents of R_m (bit 0) determines the byte position in the selected memory location. When the LSB is 0, the byte is the eight most significant bits (bits 8 through 15) in the memory location. When the LSB is 1, the byte is the eight least significant bits (bits 0 through 7) in the memory location.

b) Y is the sum of y and the contents of R_m right-shifted one position and zero-filled in the left most position. The original value of R_m remains in R_m.

3) When the m-designator equals zero, Y is equal to y and the byte is the eight most significant bits in the memory location.

2-36. Format RL. The Format RL instructions are single length and use the format as specified in figure 2-3. The a-designator selects the R_a register; the m-designator field contains a 4-bit, unsigned literal; the f-designator is interpreted as a secondary function code.

2-37. DOUBLE LENGTH WORDS. The DPS performs double-length word operations when specified in an individual instruction. In the double instructions, the contents of two adjacent registers or memory locations are used as one 32-bit word. The word at a location designated R_a, R_m, or Y becomes the most significant 16 bits of the double length word, and the word at a location designated R_a+1, R_m+1, or Y + 1, respectively, becomes the least significant 16 bits of the double length word. The memory address or register address of the most significant 16 bits must be an even number.

2-38. SHIFT INSTRUCTIONS. Shift instructions shift the contents of a register or registers to the right, left, or left circular. The contents of bits 0 through 5 of the quantity specified in the RK or RR instructions or bits 0 through 3 of an RL format instruction word determine the number of places shifted. The shift operations are as follows:

1) Right shifts move the data toward the least significant bit position. Bits shifted out of the least significant bit position are lost. After each shift step, the most significant bit position is filled with either a zero (zero extended to fill) or a sign bit (sign extended to fill) as specified in the individual instruction.

2) Left shifts move the data toward the most significant bit position. Bits shifted out of the most significant bit position are lost. At each shift step, the least significant bit position is filled with a zero. A sign change at the most significant bit position sets the OVERFLOW designator.

3) Left shift circular means that the data is shifted left, and the bits shifted out of the most significant bit position are transferred to the least significant bit position. A sign change at the most significant bit position sets the OVERFLOW designator.

2-39. INSTRUCTION REPERTOIRE. Table 2-8 lists the macroinstruction repertoire and shows the operation code, the format, and the execution time for each instruction. Detailed descriptions of each instruction are provided in Appendix B.

2-40. MISCELLANEOUS OPERATING AIDS. Miscellaneous items of value to operators of the DPS are listed in the Appendices as follows:

1) Detailed Descriptions of Microinstruction Repertoire - Appendix A.

2) Detailed Description of Macroinstruction Repertoire - Appendix B.

3) Internal Micro Program Listing - Appendix C.

TABLE 2-8. MACROINSTRUCTION REPERTOIRE

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
00	RR	Unassigned (See Note)	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Load	2.25
01	RR	Load	.75
	RI-2	Load	1.5
	RK	Load	1.5
	RX	Load	2.25
02	RR	Unary-Arithmetic	1.0
	RI-2	Load Double	2.25
	RK	Unassigned	-
	RX	Load Double	3.0
03	RR	Unary-Control	.75→8.0
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Load Multiple	1.5 +*N times .75
04	RR	Unary-Shift	3.0→4.0
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Load and Index by 1	2.25
05	RR	Set Bit	1.5
	RI-2	Load and Index by 1	1.5
	RK	Unassigned	-
	RX	Load and Index by 1	2.25

*N = number of registers loaded

NOTE: Unassigned instructions produce an instruction fault.

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
06	RR	Clear Bit	1.5
	RI-2	Load Double and Index by 2	2.55
	RK	Unassigned	-
	RX	Load Double and Index by 2	3.3
07	RR	Compare Bit	1.8
	RI-2	Load PSW	3.0
	RK	Unassigned	-
	RX	Load PSW	3.75
10	RR	Logical Right Single Shift	1.0
	RI	Unassigned	-
	RK	Logical Right Single Shift	1.7
	RX	Byte Store	2.4
11	RR	Algebraic Right Single Shift	1.0
	RI-2	Store	1.7
	RK	Algebraic Right Single Shift	1.7
	RX	Store	2.4
12	RR	Logical Right Double Shift	2.6
	RI-2	Store Double	2.4
	RK	Logical Right Double Shift	3.2
	RX	Store Double	3.2
13	RR	Algebraic Right Double Shift	2.6
	RI	Unassigned	-
	RK	Algebraic Right Double Shift	3.2
	RX	Store Multiple	1.4 + *N x 1.1
14	RR	Algebraic Left Single Shift	1.0
	RI	Unassigned	-
	RK	Algebraic Left Single Shift	1.7
	RX	Byte Store and Index by 1	2.4

*N = number of registers loaded

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
15	RR	Circular Left Single Shift	1.0
	RI-2	Store and Index by 1	1.7
	RK	Circular Left Single Shift	1.7
	RX	Store and Index by 1	2.4
16	RR	Algebraic Left Double Shift	2.7
	RI-2	Store Double and Index by 2	2.6
	RK	Algebraic Left Double Shift	3.3
	RX	Store Double and Index by 2	3.3
17	RR	Circular Left Double Shift	2.4
	RI-2	Store Zeros	1.7
	RK	Circular Left Double Shift	3.0
	RX	Store Zeros	2.4
20	RR	Subtract	.75
	RI-2	Subtract	1.5
	RK	Subtract	1.5
	RX	Subtract	2.25
21	RR	Subtract Double	1.7
	RI-2	Subtract Double	2.25
	RK	Unassigned	-
	RX	Subtract Double	3.0
22	RR	Add	.75
	RI-2	Add	1.5
	RK	Add	1.5
	RX	Add	2.25
23	RR	Add Double	1.5
	RI-2	Add Double	2.25
	RK	Unassigned	-
	RX	Add Double	3.0
24	RR	Compare	.90
	RI-2	Compare	1.5
	RK	Compare	1.7
	RX	Compare	2.25

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
25	RR	Compare Double	1.7
	RI-2	Compare Double	2.25
	RK	Unassigned	-
	RX	Compare Double	3.0
26	RR	Multiply	3.8
	RI-2	Multiply	4.0
	RK	Multiply	4.4
	RX	Multiply	4.6
27	RR	Divide	6.8
	RI-2	Divide	7.0
	RK	Divide	7.4
	RX	Divide	7.5
30	RR	AND	.75
	RI-2	AND	1.5
	RK	AND	1.5
	RX	AND	2.25
31	RR	OR	.75
	RI-2	OR	1.5
	RK	OR	1.5
	RX	OR	2.25
32	RR	Exclusive OR	.75
	RI-2	Exclusive OR	1.5
	RK	Exclusive OR	1.5
	RX	Exclusive OR	2.25
33	RR	Masked Substitute	1.4
	RI-2	Masked Substitute	1.5
	RK	Masked Substitute	2.0
	RX	Masked Substitute	2.25
34	RR	Compare Masked	1.5
	RI-2	Compare Masked	1.7
	RK	Compare Masked	2.1
	RX	Compare Masked	2.4
35	RR	I/O Command	4.0* + I/O Inst
	RI-2	Biased Fetch	2.25
	RK	Remote Execute	1.5 + Inst.
	RX	Biased Fetch	3.0

*Includes the time to clear bits 14 and 15 of memory address 000140.

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
36	RR	Unassigned	
	RI	Unassigned	
	RK	Unassigned	
	RX	Unassigned	
37	RR	Unassigned	
	RI	Unassigned	
	RK	Unassigned	
	RX	Unassigned	
40	RR	Conditional Jump	1.1
	RI-1	Local Jump	1.2
	RK	Conditional Jump	1.7
	RX	Conditional Jump	2.4
41	RR	Index Jump	1.4
	RI-1	Local Jump Indirect	2.0
	RK	Index Jump	2.1
	RX	Index Jump	2.25
42	RR	Jump and Link Register	1.2
	RI	Unassigned	-
	RK	Jump and Link Register	1.2
	RX	Jump and Link Register	2.25
43	RR	Unassigned	-
	RI-1	Local Jump and Link Memory	2.0
	RK	Jump and Link Memory	2.9
	RX	Jump and Link Memory	3.2
44	RR	Jump Register = 0	1.4
	RI-1	Local Jump Equal	1.2
	RK	Jump Register = 0	2.1
	RX	Jump Register = 0	2.25
45	RR	Jump Register $\neq$ 0	1.4
	RI-1	Local Jump Not Equal	1.2
	RK	Jump Register $\neq$ 0	2.1
	RX	Jump Register $\neq$ 0	2.25
46	RR	Jump Register Positive	1.4
	RI-1	Local Jump Greater than Or Equal	1.2
	RK	Jump Register Positive	2.1
	RX	Jump Register Positive	2.25
47	RR	Jump Register Negative	1.4
	RI-1	Local Jump Less Than	1.2
	RK	Jump Register Negative	2.1
	RX	Jump Register Negative	2.25

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
50	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
51	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
52	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
53	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
54	RR	Load Address Register	1.8
	RI-2	Load Address Register	2.6
	RK	Unassigned	-
	RX	Load Address Register Multiple	3.0 + .75 x n*
55	RR	Store Address Register	1.8
	RI-2	Store Address Register	2.6
	RK	Unassigned	-
	RX	Store Address Register Multiple	3.0 + 1.1 x n*
56	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
57	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
60	RL-1	Logical Right Single Shift	1.3
	RL-2	Algebraic Right Single Shift	1.3
	RL-3	Logical Right Double Shift	2.8
	RL-4	Algebraic Right Double Shift	2.8
61	RL-1	Algebraic Left Single Shift	1.3
	RL-2	Circular Left Single Shift	1.3
	RL-3	Algebraic Left Double Shift	2.8
	RL-4	Circular Left Double Shift	2.8

*n = Number of address registers

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
62	RL-1	Subtract	.9
	RL-2	Subtract Double	1.8
	RL-3	Add	.9
	RL-4	Add Double	1.8
63	RL-1	Load	.9
	RL-2	Compare	1.2
	RL-3	Multiply	4.2
	RL-4	Divide	7.4
64	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Subtract	2.25
65	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Add	2.25
66	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Compare	2.25
67	RR	Reserved	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Byte Compare and Index by 1	2.25
70	RR	Channel Control (Command)	30.0 for m = 0-7; 2.0 for m = 10-17
	RR	Channel Control (Chaining)	2.25
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Initiate Transfer (Chaining)	4.5
71	RR	Unassigned	-
	RI	Unassigned	-
	RK	Initiate Chain (Command)	2.25
	RK	Load Control Memory (Chaining)	2.25
	RX	Load Control Memory (Command)	3.0
	RX	Load Control Memory (Chaining)	3.0
72	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Store Control Memory (Command)	3.0
	RX	Store Control Memory (Chaining)	3.0

TABLE 2-8. MACROINSTRUCTION REPERTOIRE (CONT)

OPERATION CODE	FORMAT	INSTRUCTION	EXECUTION TIME MICROSECONDS
73	RR	Halt/Interrupt (Chaining)	1.5
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Set/Clear Flag (Chaining)	3.0
74	RR	Unassigned	-
	RI	Unassigned	-
	RK	Conditional Jump (Chaining)	2.25
	RX	Unassigned	-
75	RR	Search for Sync; Set Monitor/ Set Suppress (Chaining	1.5
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-
76	RR	Set/Clear Discretes (Command)	1.5
	RR	Set/Clear Discretes (Chaining)	1.5
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Store Status (Command)	3.0
	RX	Store Status (Chaining)	3.0
77	RR	Unassigned	-
	RI	Unassigned	-
	RK	Unassigned	-
	RX	Unassigned	-

CHAPTER 3

FUNCTIONAL DESCRIPTION

3-1. INTRODUCTION.

3-2. This chapter describes the internal operation of the DPS. The description is presented in two levels: primary block diagram level and functional block diagram level.

3-3. PRIMARY BLOCK DIAGRAM DESCRIPTION.

3-4. The primary block diagram (figure 3-1) divides the DPS into six major functional sections. These are the Microprogrammed Controller (MPC), the Processor/Emulator, the Memory Interface, the Main Memory, the I/O Controller, and the Power Sections. Data transfers between sections are handled by the Source Bus and the Destination Bus.

3-5. The MPC controls the DPS. The main difference between MPC-controlled computers and standard computers is that most of the hard wired control is replaced by microprogrammed control. They operate, like other computers, from a program of instructions stored in the main memory. This program is called the macroprogram to distinguish it from the microprogram that controls the MPC. The computer instructions are called macroinstructions to distinguish them from the MPC's microinstructions. The MPC in the Data Processing Set, AN/UYK-20(V), is a general purpose controller. It has its own read only memory (ROM) to hold its microprogram, and can be programmed to provide control for a wide range of functions. It is essentially a small computer, and performs many of the required computer functions within its own circuits. The link between the macroprogram and the MPC is provided by an "emulator" which decodes the macroinstructions and causes entrance into an MPC microprogram subroutine to perform (emulate) the desired function. Sometimes all of the circuitry with the exception of the MPC itself is called the emulator, since it all augments the MPC and assists it in emulating required functions. The capabilities of microprogram controlled computers can often be changed or increased simply by adding new translations into the emulator and new subroutines into the microprogram.

3-6. MICROPROGRAMMED CONTROLLER. The MPC executes 16 basic microinstructions with many variations. (See Appendix A for a detailed description of each microinstruction). Data transfers occur over the two bi-directional data buses. The two-bus structure allows instruction overlapping to increase the microinstruction execution rate. Two fields within the microinstruction word define what register or network is applied to the source bus (S-field) and what register or network is the recipient of data on the destination bus (D-field). Simply stated, a microinstruction performs a function on the source and transmits the result to the destination. Following is a description of the major MPC elements.

3-7. The micro memory is a read-only memory. It is capable of holding up to 4K (4096) words of microprogram including 512 addresses usually reserved for optional customer specified routines. Microprograms can be changed only by substituting different pre-programmed cards. The micro memory control section contains the addressing circuits that control the reading of the micro memory. The micro function control section receives the current microinstruction from the micro memory, translates it, and issues control signals to all sections of the DPS to carry out

the instruction. It includes the master clock which provides timing for the entire DPS. The repeat control section controls the repetitive cycling of microprogram subroutines, as required by the Repeat microinstructions. The arithmetic section contains accumulator storage registers and an arithmetic/logic unit (ALU) which performs arithmetic and logical operations on the operands. The display control section, under the control of a microprogram subroutine, provides the interface between the operator and maintenance panels and the displayable registers of the DPS.

3-8. PROCESSOR/EMULATOR. The processor/emulator is concerned with the macroinstructions. It contains many of the registers and functions normally associated with the central processor portion of a computer, but performs its functions under the control of the MPC. The following paragraphs describe the major processor/emulator subsections.

3-9. The function control section translates the macroinstruction word and sends an Emulator Control Word (ECW) to the MPC directing it to perform the proper microprogram subroutine for accomplishing each macroinstruction. The general registers can be used for accumulator storage, as scratch pad registers, as index registers, etc. They are normally addressed by the A and M fields of the macroinstruction word. There may be one or two groups of 16 general registers; if there are two groups, a status register bit determines which group is addressed. The program status section contains the two status registers, the real time clock and monitor clock registers, and the interrupt control circuits. The status registers store program status information, provide for selecting the general register group, enable reading from NDRO memory, control the disabling of interrupts, and control direct and indirect addressing; the real time clock and monitor clock permit the DPS to monitor elapsed time; the interrupt circuits handle program interrupts according to their assigned priorities. The high speed shift and multiply section contains a shifting matrix and multiply logic which operate without involving the MPC arithmetic unit, and perform their tasks faster than possible in the MPC. The multiply logic operates with two multiplier digits at a time.

3-10. MEMORY INTERFACE. The memory interface handles the transfer of information to and from the main memory. It permits reading or writing of full words or either byte of a word, or reading a word, modifying it, and restoring the modified word. The memory interface section divides into three subsections: memory address control, memory data interface, and NDRO memory.

3-11. The memory address control section provides the address information to the main memory. The program address normally increments by one after each memory reference. A breakpoint function allows the program to be stopped when a preselected memory address is referenced. Paging circuits permit the memory to be addressed as 64 separate and interchangeable 1K portions. The memory data interface section transfers data to and from the main memory. The NDRO memory consists of up to 192 words of read-only memory generally used for a bootstrap load program. Access to the NDRO memory is controlled by a bit in status register 1.

3-12. MAIN MEMORY. The main memory, which is used for storage of the macroprogram is a coincident current magnetic core memory, expandable to 65K (65,536) words in 8K (8192) word increments. Word length is 16 bits. Cycle time is approximately 750 nsec for a read or write cycle, and approximately one μsec for a read, modify, restore cycle (called split cycle). The memory chassis holds up to twelve boards of three types: memory control boards (MCB), memory data boards (MDB), and memory array boards (MAB). MCB's contain control and addressing circuits for up to 32K

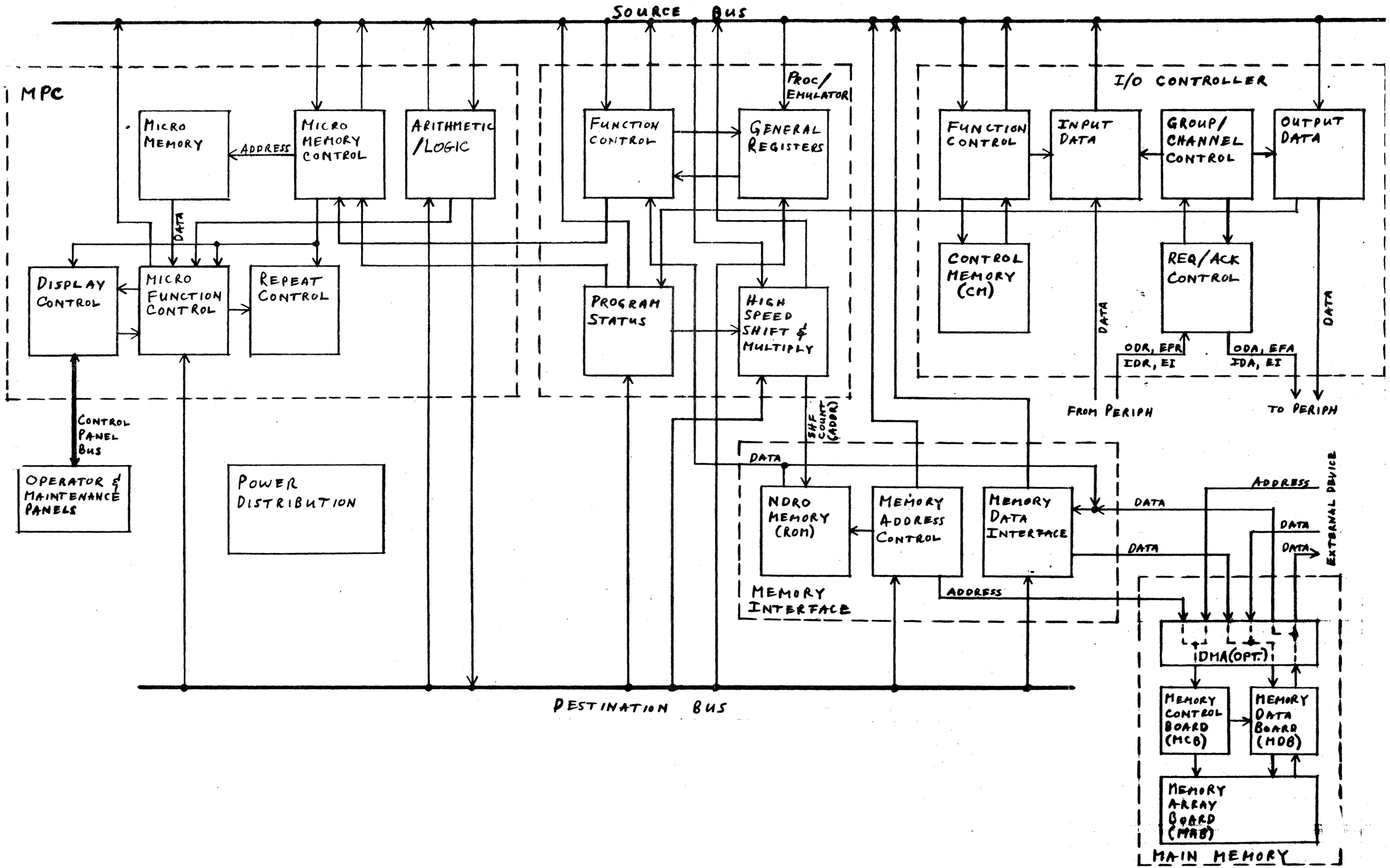


Figure 3-1. Primary Block Diagram

of memory. MDB's contain a data register and bit drivers for up to 32K of memory. In addition, MCB's and MDB's may contain the logic for an optional direct memory access (DMA) feature, which allows the memory to be used also by external devices on a priority basis. Two MCB's and two MDB's are installed to permit memory sizes up to 65K. Each MAB contains 8K of core storage, along with associated drivers and sense amplifiers. A chassis contains from one to eight MAB boards.

3-13. I/O CONTROLLER. The I/O Controller provides communication interface between the DPS and the peripheral equipment via a possible total of 16 input/output channels. Both control and data circuitry are included in the controller. Input/output channels are of two types: parallel and serial. Both types are available in either single or dual channel mode operation. Parallel channels must always exist in complete groups of four adjacent channels. Serial channels are divided into groups of two. For dual channel operation with parallel channels, two adjacent groups are required and the lower group must be even numbered (0 or 2). The channels involved are n and n+4. Dual channel operation with serial channels uses the pair of channels in a two-channel group. The 16 I/O channels, whether parallel or serial or a mixture, divide into four groups of four channels for internal addressing purposes (refer to Table 3-1). The higher numbered channels have the higher priority (channel 17_8 highest, channel 0 lowest).

Table 3-1. Parallel I/O Channel Groups

GROUP	CHANNELS
0	0, 1, 2, 3
1	4, 5, 6, 7
2	10, 11, 12, 13
3	14, 15, 16, 17

3-14. Parallel channels have three optional interfaces: NTDS Slow (-15V), NTDS Fast (-3V), or ANEW (+3.5V). Parallel channels operate asynchronously, with transfer rates per interface as specified in Table 1-1. Parallel channels will operate in the intercomputer mode if so specified on order; otherwise they operate in the normal buffer mode. Serial channels are of three optional types: expanded MIL-STD-188 synchronous or asynchronous, RS-232 standard synchronous or asynchronous, or the NTDS 32-bit asynchronous. Serial channel transfer rates are as specified (synchronous or asynchronous) in Table 1-1. The order of data transfer is from the least significant bit (0) to the most significant bit (15). Both serial and parallel channels operate in full duplex mode.

3-15. The I/O Controller receives/transmits data from/to both the DPS source bus and the peripheral equipment. See figure 3-1, system primary block diagram. The major circuits of the I/O controller are defined below.

3-16. The Input Data Circuitry receives data from peripherals and determines whether the peripheral data or data from the I/O Function Control is to be gated to the source bus. The Req/Ack Control circuitry receives requests (ODR, EFR, IDR, or EIR) from the peripherals, and acknowledges (ODA, EFA, IDA, EIE) those requests. A request must be acknowledged before another similar request is allowed in from

that channel. The Group/Channel Control Circuitry receives the channel requests from the Req/Ack Control and establishes channel and function priority. This circuitry also generates a clear request signal and enables an acknowledge signal to be returned to the peripheral equipment. It generates a group select signal for the Output Data circuitry. The I/O Function Control circuitry receives information from the source bus and passes it to the control memory (CM) or decrements the buffer word counts and increments the address pointers of control memory. The altered counts and pointers may be sent to either CM or the source bus. Data is also taken from control memory and sent to the source bus via the Input Data circuitry. The Output Data circuitry obtains data from the DPS via the source bus and sends the data to the peripheral devices designated by the Group Select signal from the Group/Channel Control.

3-17. POWER. The power supply converts the ac input power to the various dc voltages required by the DPS. It is oscillator controlled. It maintains close-tolerance regulation of the output voltages and provides filtering to limit line noise and transients. It checks for under and over-voltage at the input and for overload at the output. Variations of the power supply permit input power to be 115 Vac or 208 Vac, single phase or three phase, 60 Hz or 400 Hz.

3-18. FUNCTIONAL BLOCK DIAGRAM DESCRIPTION.

3-19. The following paragraphs provide detailed block diagrams and accompanying descriptions for each of the major sections of the computer. The diagrams are as follows: figure 3-2, MPC; figure 3-8, Processor/Emulator; figure 3-16, Memory Interface, figure 3-19, Main Memory; figure 3-29, I/O Controller; and figure 3-54, Power Supply and Distribution. The numbers associated with the lower right hand corner of each symbol on these block diagrams signify the figure numbers of the logic schematics on which the circuitry may be found. The logic schematics are in chapter nine (Volume 2) of this manual.

3-20. MICROPROGRAMMED CONTROLLER (MPC). The MPC executes microinstructions to perform all control operations and data manipulations in the computer. The microinstructions are permanently stored in a read-only memory (ROM). See Appendix A for a detailed description of the microinstruction repertoire. The two-bus (source bus and destination bus) structure allows instruction overlapping as shown in figure 3-3. Overlapping increases the microinstruction execution rate to one microinstruction per clock pulse. The S-field within the microinstruction word defines what register or network is applied to the source bus, and the D-field defines what register or network is the recipient of data on the destination bus. Figure 3-2 is the block diagram of the MPC. Following is a description of the major elements:

3-21. Micro Memory. The micro memory contains the unalterable microprogram. It is a ROM memory, consisting of four printed circuit cards, each containing 1024 (1K) 16-bit words. The ROM cards are factory pre-programmed; therefore microprograms can be changed only by substituting different cards.

3-22. The basic microprogram consumes the first 1-1/2K micro memory addresses, physically located on the cards at locations 5B and 4B. The next 1/2K addresses (3000_8 to 3777_8) are reserved for customer-specified microprogram routines. Note that if customer-specified microprograms are added after the computer leaves the factory, both the micro memory card at location 4B must be replaced, and also the card at location 10C which must generate ECWs for the new macroinstructions. The

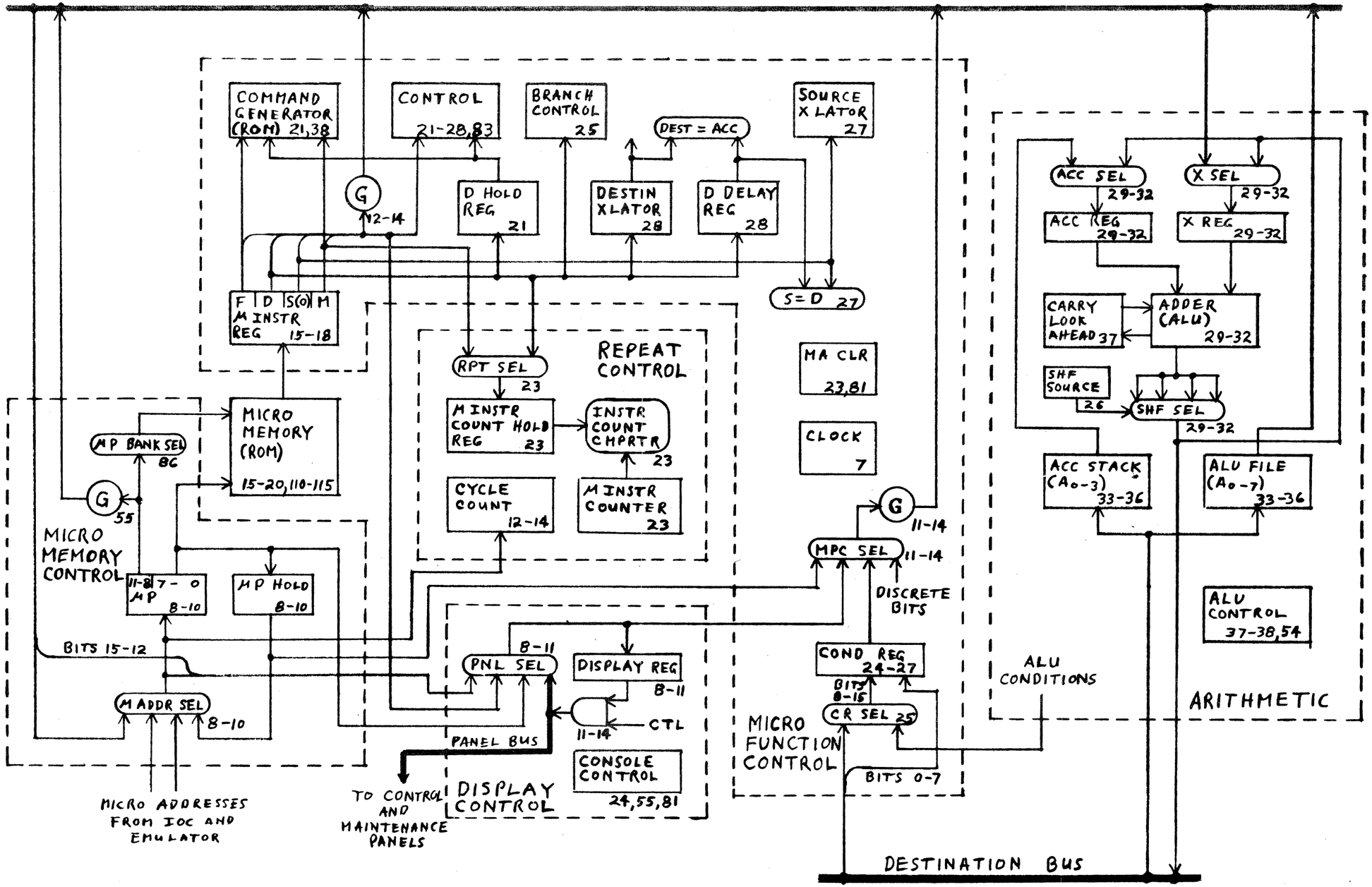


Figure 3-2. MPC Functional Block Diagram

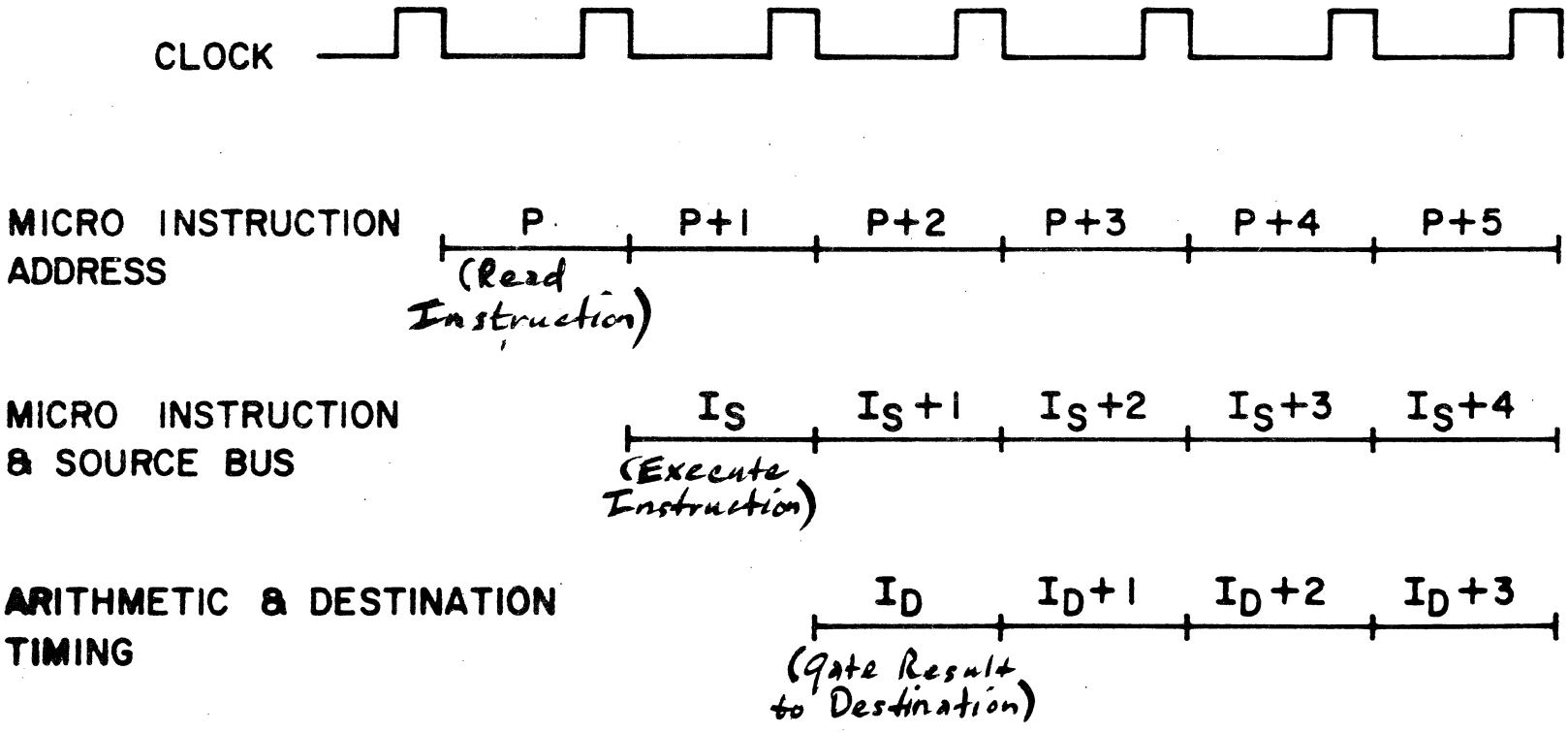


Figure 3-3. Overlapped Bus Operation

third card, at location 3B, contains addresses 4000_8 to 5777_8 and is reserved for the optional extended mathematics microprogram called Math Pack. An MPC diagnostic program occupies the fourth card, at location 2B, which contains addresses 6000_8 to 7777_8.

3-23. The micro memory addresses listed in Table 3-2 are permanently assigned addresses in the basic microprogram. Those labelled as micro interrupt addresses are reached through a Normal Start microinstruction (17 00 00 14). This instruction enables a hardwired priority network that checks the micro interrupts and causes a jump to the proper address if an interrupt is present. If no interrupts are present, it causes a jump to micro address 274_8 and begins the Macro Instruction Read subroutine.

3-24. The address in the micro P register selects a 16-bit microinstruction word from the micro memory. The word remains on the micro memory output lines, available to the micro instruction register until the address is changed.

3-25. Micro Memory Control. The Micro Memory Control section consists mainly of the micro address selector, the micro P register, and the micro P hold register.

3-26. The micro address selector is 12 bits wide. It selects one of four inputs as shown in table 3-3. The inputs labelled Interrupt Address come from the processor/emulator and from the I/O controller, and transfer the fixed addresses of table 3-2. The microprogram subroutines for emulating macro operation codes 40 through 77 occupy micro memory addresses above 1000_8 and are selected by bit 15 of the macro instruction register which accompanies the nine ECW address bits when selected.

3-27. The 12-bit micro P register holds the address of the next instruction to be read from the micro memory. A bank selector uses the upper three bits of the register to select 1/2K (512 word) segments of the memory. The micro P register normally increments by one each clock pulse to form the next address. Jumping or branching to a non-consecutive address requires that the new address be loaded into the register from the source bus via the micro address selector. Since the address field in branch instructions has only eight bits, the upper four bits of the micro P register are gated onto the source bus to accompany the branch address.

3-28. The 12-bit micro P hold register stores the beginning address of a series of microinstructions that are being repeated. The repeat (F = 16) microinstruction initiates the repeat mode. When the last microinstruction in the series is read from micro memory, the contents of the micro P hold register are loaded into the micro P register via the micro address selector to repeat the series again. This continues until the repeat mode is terminated.

3-29. Micro Function Control. The Micro Function Control section of the MPC generates timing and control signals for the MPC and for much of the rest of the DPS. The following paragraphs describe its functional sections.

3-30. The micro instruction register holds the micro instruction that is currently being executed. Most instructions use a basic instruction format which divides the register into four 4-bit fields (F, D, S, and M) as shown in figure 3-4. The F-field specifies the basic function to be performed, such as add, subtract, shift, transfer, etc. The D-field defines the destination register for the result. The S-field specifies the source register on which to perform the function; this field is sometimes called the Origin or O-field. The M-field modifies the basic function

Table 3-2. Fixed Addresses in Micro Memory

	0000	Master Clear (Auto Start)	Interim Sequence Addresses	0300	I/O In Data, Pass > 1
				0310	I/O In Data, Pass 1
				0320	I/O Out Data, Pass > 1
Micro Interrupt Address	0200	I/O Return		0330	I/O Out Data, Pass 1
	0204	Bootstrap Load		0340	IA Byte Mod
	0210	I/O Chain Instr. Read		0344	IA Byte $\overline{\text{Mod}}$
	0214	$\overline{\text{RUN}}$ (Display Routine)		0350	IA Word Mod
	0220	Class I & II Interrupts		0354	IA Word $\overline{\text{Mod}}$
				0360	Norm Byte Mod
	0230	Class III Interrupts		0364	Norm Byte $\overline{\text{Mod}}$
				0370	Norm Word Mod
	0274	Instruction Read Routine		0374	Norm Word $\overline{\text{Mod}}$
				2374	Ill. I/O Instr.
				2376	Ill. CP Instr.
				27XX	IA Table

Table 3-3. Micro Address Selection*

Selector control bits = 00:	Interrupt Address (Bits 1-7, 10)
Selector control bits = 01:	ECW Address Pointer (Bits 0-8) plus IR_{15}
Selector control bits = 10:	Micro P Hold Register
Selector control bits = 11:	Source Bus

*See Volume 2, Figures 9-8 to 9-10.

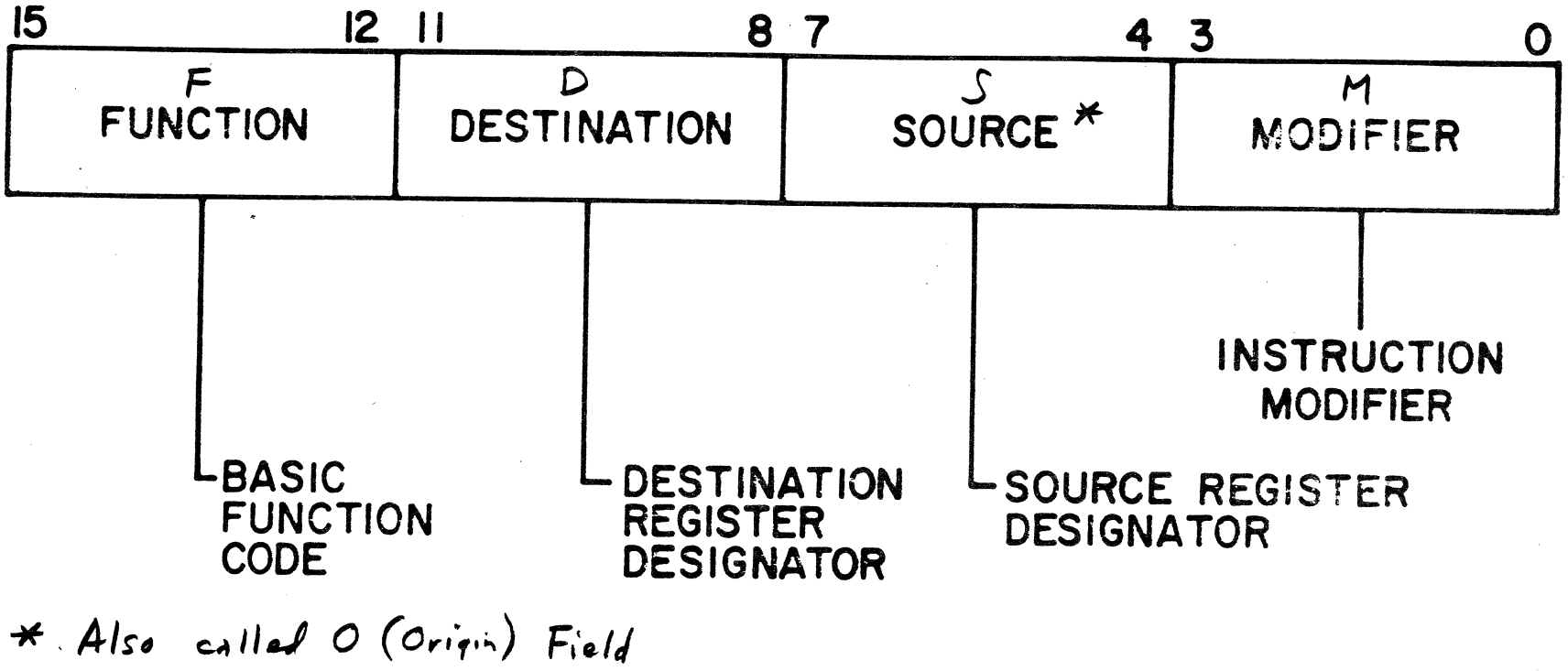


Figure 3-4. Microinstruction Format

in various ways for the different micro instructions. See Appendix A for a description of each micro instruction. The contents of the micro instruction register direct most of the control functions of the DPS. The contents can be gated to the source bus and can be displayed on the maintenance panel through the panel selector.

3-31. Three Command Generator ROM's translate micro instruction codes and generate basic command signals. Two are elements 01 and 02 on the card at location 10B and appear on figure 9-38 in Volume 2. These two primarily control the operation of the MPC Arithmetic Section (ALU) and are, therefore, called the ALU control chips. The Function (F) and Mode (M) fields of the micro instruction word select the addresses in these ROM's. Tables 3-4 and 3-5 show their microcoded contents. The third ROM is element 03 on the card at location 7B and appears on figure 9-21. It decodes the D-field (or F_2 - field) on Repeat (F = 16) microinstructions. It, therefore, is called the repeat control chip. Table 3-6 shows its microcoded contents. Additional MPC control circuits occur throughout the DPS, but mostly appear on logic figures 21 through 28 (Chapter 9) and are grouped into one block labelled Control.

3-32. A number of circuits throughout the Micro Control Section are associated with the D-field of the microinstruction register. The F2 register holds the D-field on Repeat microinstructions, in which the D-field becomes a secondary function code. It is decoded by the repeat control command generator ROM described in the preceding paragraph. The branch control circuits translate the D-field as a secondary function code to determine the branching condition. (See figure 9-25. Chip U07 is enabled for F_2 0-7; U04 is enabled for F_2 11-17. Output of disabled chip is held high. See Appendix A, table A-10 for the branch conditions.) A D-delay register permits the MPC instruction overlap described in paragraph 3-20 and figure 3-3 by holding the destination information for one clock period after the microinstruction register. The contents of the D delay register are compared with the source field of the current microinstruction. If they are the same, the MPC doesn't stop to wait until the data has first been sent to the destination, but simply gates the destination bus data directly through the X selector to make immediate use of it, while simultaneously gating it to its destination. Likewise, the D delay register is compared to the D field of the current microinstruction. If both are designating the same address in the accumulator stack, the MPC gates the contents of the destination bus directly through the accumulator selector. This is necessary, because most microinstructions use the D-field for designating one of the four accumulator stack registers (A_0 - 3) as one of the operand sources, as well as for designating the destination of the result.

3-33. The 16-bit condition register (CR) defines the status of arithmetic operations as shown in figure 3-5. Status is loaded into the condition register when specified by a microinstruction with F = 2 through 7 and save status bit set (M-field bit 3 = 1). Bits 0-7 of the condition register load directly from the destination bus. Bits 8-15 load through the CR selector and may be data from the destination bus or may be arithmetic status bits.

3-34. The 16-bit MPC source selector is the main path for MPC data to be placed on the source bus. Its output is gated to the bus when one of its inputs is designated by the microinstruction S field. It selects inputs as follows:

1) Selector control bits = 00: Discrete bits per table 3-7

2) Selector control bits = 01: Panel Selector

Table 3-4. Microcode for Command Generator ROM Chip U03

Address (Octal)	Contents (Octal)	FUNCTION
00	167	TRANSFER DESTINATION 1
01	267	TRANSFER DESTINATION 2
02	377	JUMP
03	377	JUMP
04	166	ADD SOURCE 2
05	166	ADD SOURCE 2
06	167	SHIFT
07	167	SHIFT
10	166	ADD SOURCE 1
11	166	ADD SOURCE 1
12	164	SUBTRACT
13	164	SUBTRACT
14	167	LOGIC 1
15	167	LOGIC 1
16	167	LOGIC 2
17	167	LOGIC 2
20	176	ADD K
21	176	ADD K
22	174	SUBTRACT K
23	174	SUBTRACT K
24	177	TRANSFER K TO D1
25	177	TRANSFER K TO D1
26	277	TRANSFER K TO D2
27	277	TRANSFER K TO D2
30	337	BRANCH
31	337	BRANCH
32	357	MICRO CONTROL
33	357	MICRO CONTROL
34	373	REPEAT
35	373	REPEAT
36	376	EMULATE
37	376	EMULATE

BIT SIGNIFICANCE

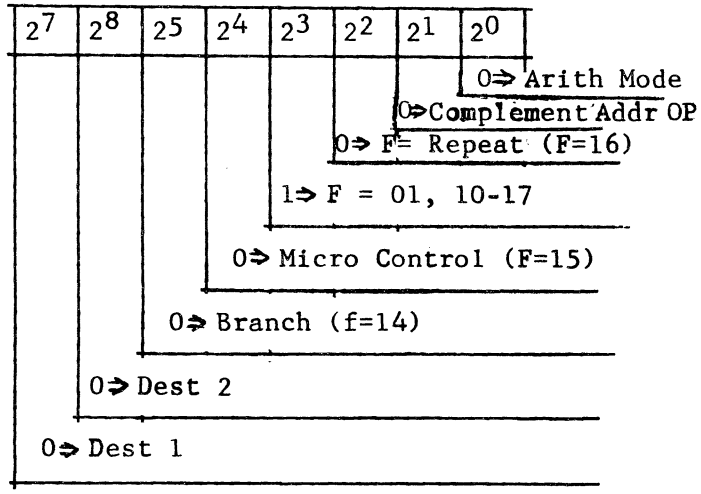
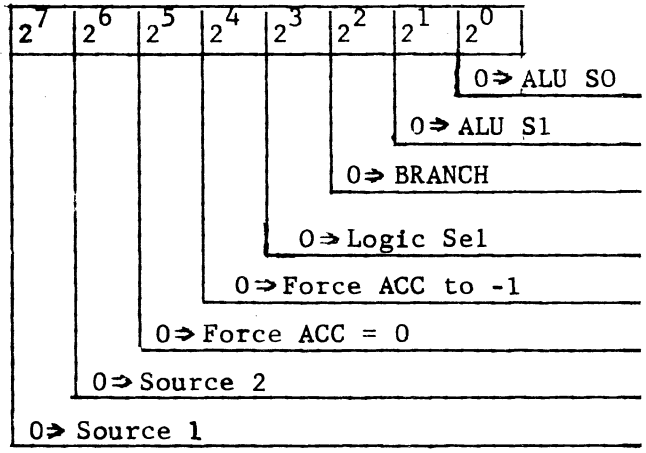


Table 3-5. Microcode for Command Generator ROM Chip U06

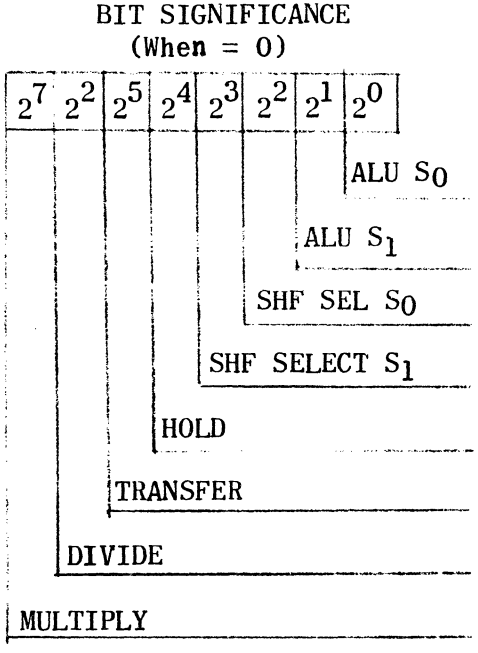
Address (Octal)	Contents (Octal)	Function	
00	177	TRANSFER NORMAL S1	f = 0
01	277	TRANSFER NORMAL S2	
02	176	TRANSFER REVERSE S1	
03	276	TRANSFER REVERSE S2	
04	373	JUMP	f = 1
05	373	JUMP	
06	373	JUMP	
07	373	JUMP	
10	277	ADD S2 NORMAL	f = 2
11	277	ADD S2 NORMAL	
12	237	ADD S2 + 0	
13	257	ADD S2 -1	
14	174	SHIFT LEFT	f = 3
15	174	SHIFT LEFT	
16	175	SHIFT RIGHT	
17	175	SHIFT RIGHT	
20	177	ADD S1 NORMAL	f = 4
21	177	ADD S1 NORMAL	
22	137	ADD S1 +0	
23	157	ADD S1 -1	
24	177	SUB NORMAL	f = 5
25	177	SUB NORMAL	
26	137	SUB FROM 0	
27	137	SUB FROM 0	
30	167	LOGIC 1	f = 6
31	167	LOGIC 1	
32	167	LOGIC 1	
33	167	LOGIC 1	
34	167	LOGIC 2	f = 7
35	167	LOGIC 2	
36	167	LOGIC 2	
37	167	LOGIC 2	



(Reference: Vol. 2, Fig. 9-38)

Table 3-6. Microcode for Command Generator ROM Chip U04

Address (Octal)	Contents (Octal)	Function
00	125	MULTIPLY SINGLE
01	234	DIVIDE SINGLE
02	345	MULTIPLY DOUBLE 2
03	250	DIVIDE DOUBLE 2
04	374	SQUARE ROOT 2
05	343	CORDIC PRESCALE 2
06	377	VECTOR 2 AND 3
07	377	ROTATE 2 AND 3
10	0	
11	0	
12	121	MULTIPLY DOUBLE 1
13	334	DIVIDE DOUBLE 1
14	274	SQUARE ROOT 1
15	363	CORDIC PRESCALE 2
16	367	VECTOR 1
17	373	ROTATE 1
20	125	MULTIPLY SINGLE LAST
21	237	DIVIDE SINGLE LAST
22	345	MULTIPLY DOUBLE 2 LAST
23	253	DIVIDE DOUBLE 2 LAST
24	377	SQUARE ROOT 2 LAST
25	343	PRESCALE 2 LAST
26	377	VECTOR 2 AND 3 LAST
27	377	ROTATE 2 AND 3 LAST
30	0	
31	0	
32	121	MULTIPLY DOUBLE 1 LAST
33	337	DIVIDE DOUBLE 1 LAST
34	277	SQUARE ROOT 1 LAST
35	363	PRESCALE 1 LAST
36	367	VECTOR 1 LAST
37	373	ROTATE 1 LAST



(Reference: Vol. 2, Fig. 9-21)

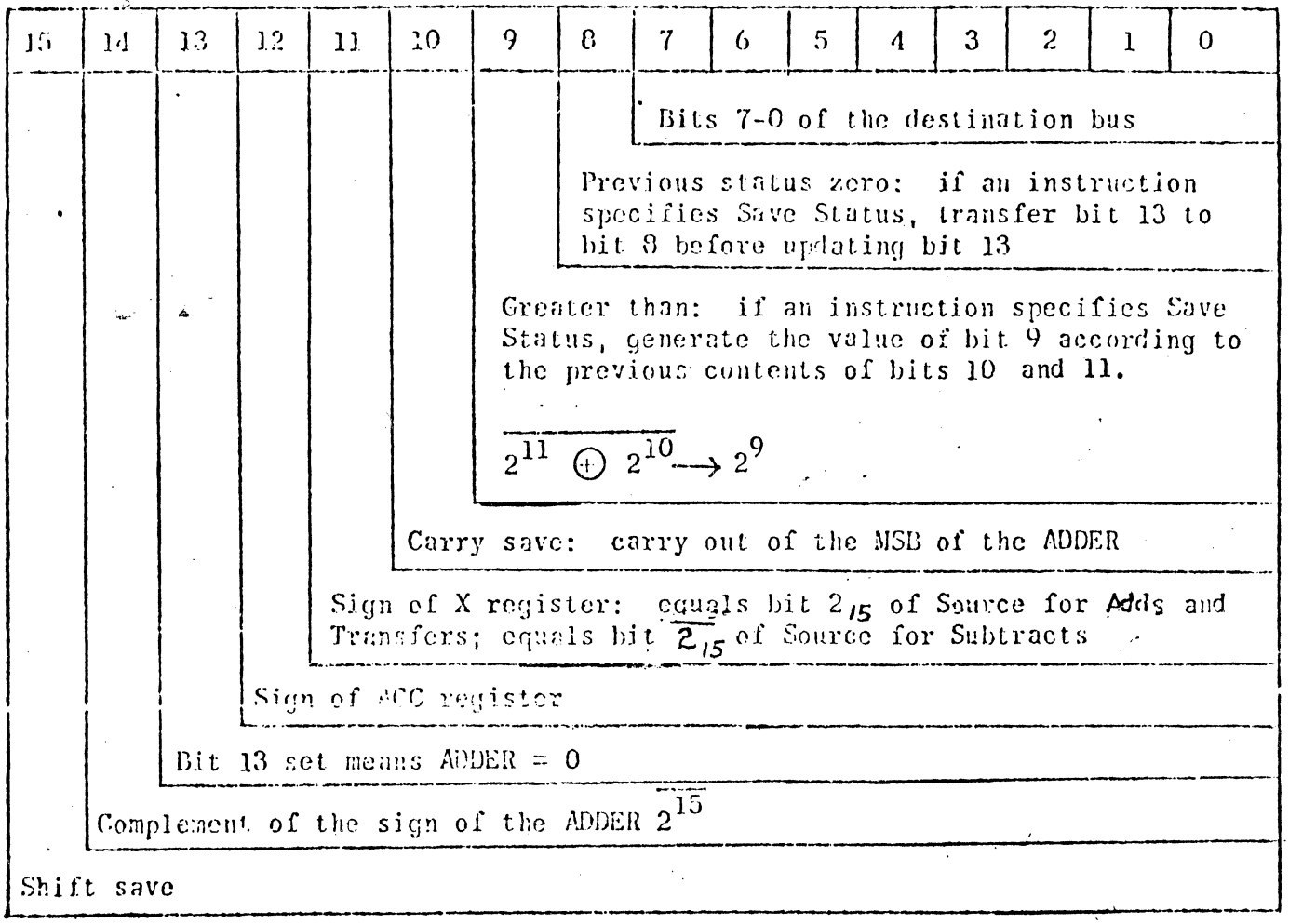


Figure 3-5. Condition Register Format

Table 3-7. Discrete Bit Inputs to MPC Source Selector

BIT	INPUT	
0	Display Number Indicator Switch 0	
1	Display Number Indicator Switch 1	
2	Display Number Indicator Switch 2	
3	Display Number Indicator Switch 3	
4	Alter Mode Switch	
5	I/O Active Signal	
6	General Register Select Indicator Switch	
7	Instruction Register Select Indicator Switch	
8	Normalize 2^0 Signal	Shift Count
9	Normalize 2^1 Signal	
10	Normalize 2^2 Signal	
11	Normalize 2^3 Signal	
12	Normalize 2^4 Signal	
13	Normalize 2^5 Signal	
14	Not used	
15	Not used	

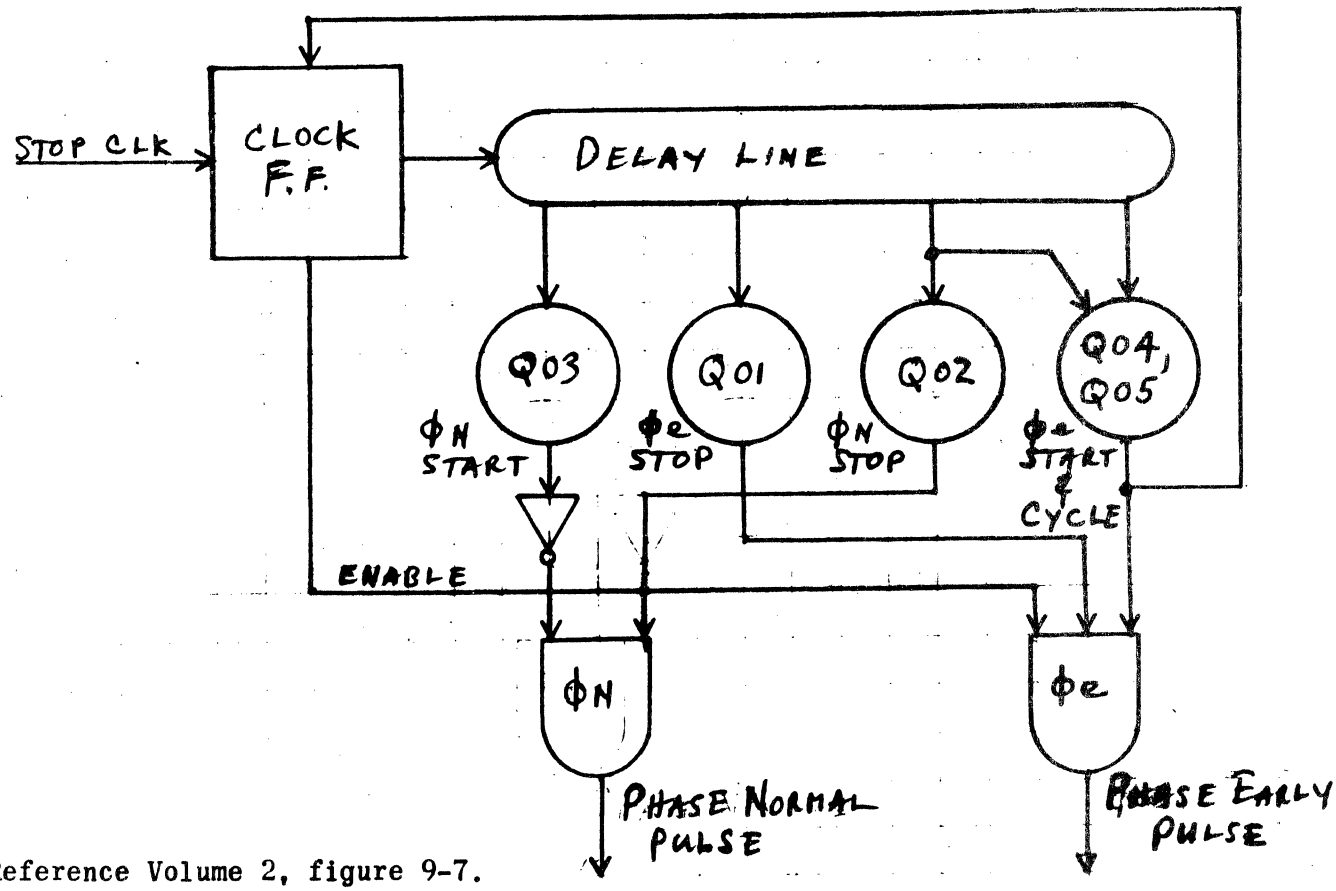
3) Selector control bits = 10: Condition Register

4) Selector control bits = 11: Micro P Hold Register (bits 12 to 15 = 0).

3-35. The master clear (also called master reset) circuits generate the master clear signal from two sources: the MASTER CLEAR switch on the maintenance console, and the power supply. When in Normal (Run) mode, the only effect of the MASTER CLEAR switch is to clear the fault indicators. The power supply monitors the +5 Vdc output and generates a master clear signal if the voltage falls below tolerance. When powering up, the signal is generated to produce an initial clear until the +5 Vdc output reaches its normal operating voltage. The master clear signal sets most of the registers and flip-flops to an initial condition and causes the MPC to enter the micro program at micro memory address 0000 to begin an Initialize subroutine, or to enter the diagnostic subroutine if the diagnostic jump switch is up.

3-36. Figure 3-6 is a simplified diagram of the master clock circuits. They produce a series of timing pulses called the phase early (Øe) and phase normal (Øn) pulses, which are used throughout the DPS. Their frequency and duration depend on the selected delay line taps. Figure 3-7 shows the approximate time relationships of the various elements within the master clock. The clock cycle is approximately 150 nsec. The Øe pulse and the Øn pulse each have a duration of approximately 50 nsec.

3-37. Repeat Control. The repeat control section is concerned with the Repeat microinstructions (function code = 16) which require the repetitive cycling of microprogram subroutines. The section consists of a cycle counter, a microinstruction count hold register, an instruction counter, and a comparator. In the repeat microinstructions, the D-field acts as a secondary function code (F_2). For F_2 codes 0-7, the S & M fields combined are called the K-field and specify the cycle count, which the MPC loads into the cycle counter. The instruction count is generated by hardware. For F_2 codes above 7, the cycle counter must be loaded by a previous instruction, and bits 0-3 of the K-field (the M-field) specify the count for the microinstruction count hold register. The count specified must be one less than the number of microinstructions to be repeated. The repeat microinstruction always sets the microinstruction counter to zero. As each microinstruction in a series is executed, the counter advances by one. When the counter and the microinstruction count hold register are equal, the cycle counter is incremented, the microinstruction counter is reset to zero, and the address stored in the micro P hold register is loaded into micro P to repeat the series. The series repeats until terminated by the cycle counter.



Reference Volume 2, figure 9-7.

Figure 3-6. Master Clock Block Diagram

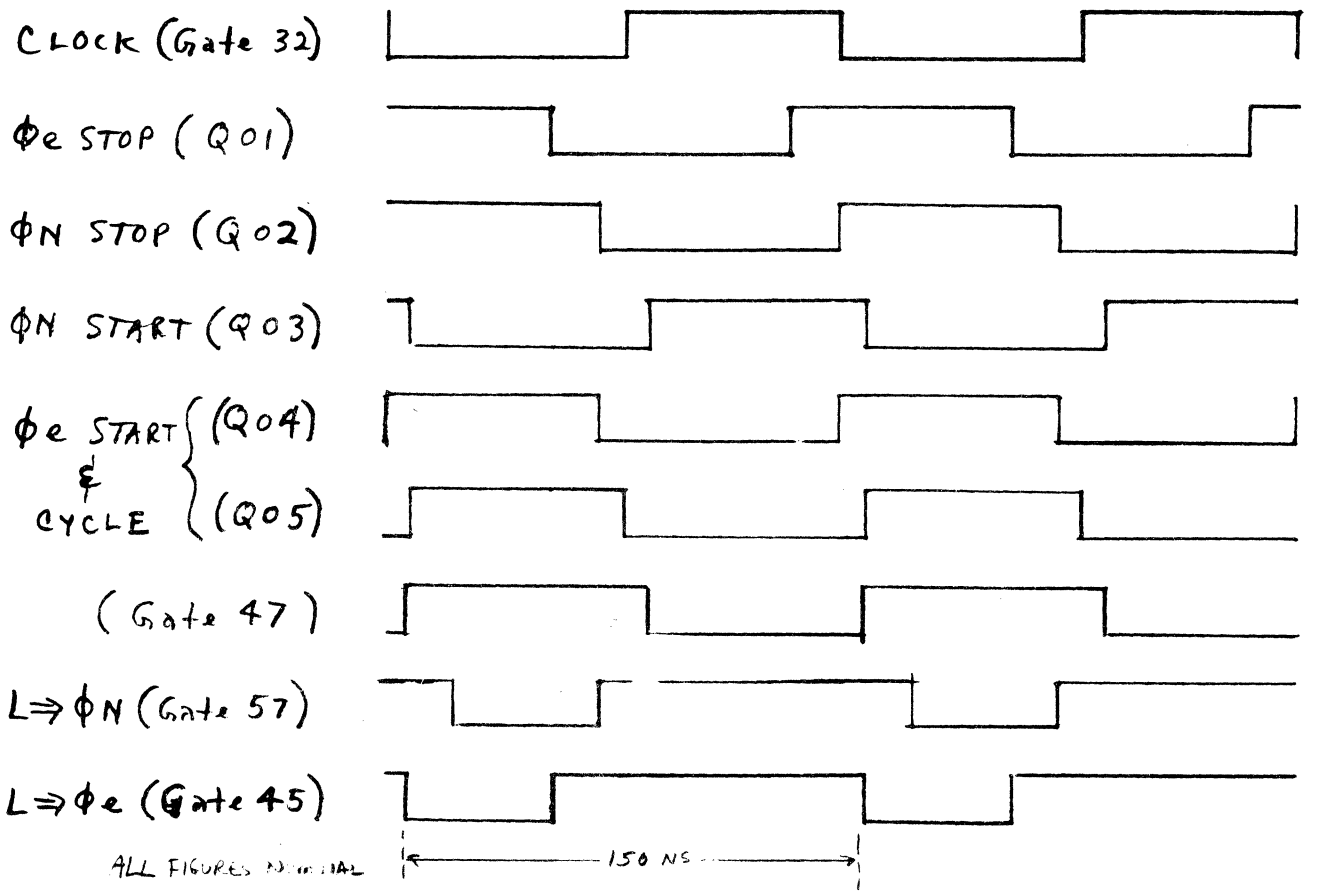


Figure 3-7. Master Clock Timing

3-38. 12-bit cycle counter is loaded through the micro P address selector. It initially receives the complement of the cycle count, and advances by one each cycle until it fills and generates a terminal count signal. It can also be used for other functions, with the micro control (F = 15) microinstruction providing control to advance the counter. The microinstruction counter and microinstruction count hold register each contain four bits. The count hold register receives its input from the repeat selector, which transmits the M-field when F_2 is greater than 7, or generates an instruction count when F_2 is 0 to 7. The instruction count comparator compares the count of the counter and the count hold register.

3-39. Arithmetic. The arithmetic section performs most of the arithmetic and logic functions of the DPS. Arithmetic control is scattered throughout the logic schematics, but mostly appears on figures 9-37 and 9-38. The following paragraphs describe the major elements of the arithmetic section and their functions.

3-40. The arithmetic section contains two scratch pad memory stacks. One is called the ALU file and contains registers A_0 through A_7. The other is called the accumulator stack and contains four registers which are duplicates of A_0 through A_3. When the specified destination of an operand is one of registers A_0 through A_3, it is stored in both the ALU file and the accumulator stack. Data can be written into and read from different addresses of the stacks simultaneously. Both are loaded from the destination bus. Data from the ALU file is placed on the source bus. Data read from the accumulator stack is gated into the accumulator

register via the accumulator selector. The D-field in most microinstructions, besides designating the destination for the result, also designates one of the registers A_0 through A_3 as the accumulator source.

3-41. The accumulator register and X register provide the inputs to the ALU. They, in turn, receive their inputs from the accumulator selector and the X selector. The usual source for the accumulator selector is the accumulator stack (A_0 - A_3). The usual source for the X selector is the source register. Both selectors sometimes use the data from the destination bus, the X selector when S = D and the accumulator when destination = accumulator, as described in paragraph 3-32.

3-42. The heart of the arithmetic section is the arithmetic/logic unit (called the ALU chips and accompanying carry look-ahead chips are described in paragraphs 3- and 3- .

3-43. The ALU output passes through the shift selector, which is capable of shifting the result as shown in table 3-8. A shift source selector determines the input to bit 15 on right shifts and to bit 0 on left shifts. The shift selector handles the shifting required for most of the complex arithmetic functions, such as divide, square root, etc. High speed multiply circuits in the processor/emulator perform the multiply function and a high speed shift matrix performs the shift function. The ALU output through the shift selector goes to the destination bus. Note that this is the only input to the destination bus and, therefore, is always on the bus and is the only data on the bus.

3-44. Display Control. The MPC contains a microprogram subroutine that controls the control panel display function through the display control circuits. The display subroutine begins at micro memory address 214_8. It is entered automatically whenever the computer is not in the Run mode, and thus permits manual manipulation of registers whenever the DPS is not performing instructions. Chapter 2 lists the displayable registers and gives the procedures for displaying and changing them. The display indicator switches on the maintenance panel constantly display the contents of the 16-bit display register through the display bus. The register to be displayed is selected by means of the MICRO ADRS, MICRO INSTR, NORM DSPL, GENL DSPL, INSTR REG, GENL REG, and DSPL NUMBER indicator switches on the maintenance panel. These indicator switches appear on figure 9-24 and 9-55 of the logic schematics in Volume 2. The microprogram loads the contents of the selected register into the display register through the panel selector. When the contents of the display register indicator switches on the panel are manually changed, the microprogram reads the change from the display bus through the panel selector onto the source bus and changes the contents of the actual register. The gating of the panel selector is shown below. The micro address selector and the micro P register have only 12 bits. When the micro P register is gated, the upper four bits are gated as zero's. When the micro address selector is gated, bits 12 to 15 are added from the source bus. This permits this path to be used for transferring source bus data to the display register.

1) Selector control bits = 00: Display bus

2) Selector control bits = 01: Micro address selector

3) Selector control bits = 10: Microinstruction register

4) Selector control bits = 11: Micro P register

3-45. PROCESSOR/EMULATOR. The processor/emulator operates with the program of macroinstructions. For each instruction, it generates an emulator control word (ECW) which causes the MPC to enter the proper microprogram subroutine and to issue the proper control signals for performing the macroinstruction. The processor/emulator contains general registers, a program status section, and high speed shift and multiply circuits, all of which augment the general purpose MPC and combine with it to efficiently perform the tasks required of the Data Processing Set. Figure 3-8 is a detailed block diagram of the processor/emulator. The following paragraphs describe its major sections and subsections.

3-46. Function Control. The function control section translates the macroinstructions and generates control signals that function together with the MPC and its microprogram to control the DPS. It consists of the instruction register (IR), the ECW stack, the emulate control circuits, and the IR selector.

3-47. The 16-bit instruction register holds the macroinstruction that is currently being executed. It receives the instruction from main memory via the memory interface section and the source bus. (See Chapter 2 and Appendix B for descriptions of the macroinstructions and the instruction word formats.) A comparator circuit monitors the A and M fields and, when equal, generates a signal used for the F = 14, F_2 = 12 Branch microinstruction.

3-48. The emulator control word stack is a ROM containing 256 16-bit words. The upper eight bits of the macroinstruction word (six-bit operation code and two-bit format code) address it. At each address, it contains an emulator control word (ECW) peculiar to that instruction. The last portion of the microprogram listing in Appendix C is a listing of the ECW stack contents. Figure 3-9 shows the ECW format. The lower nine bits of each ECW word are called the address pointer and are sent to the MPC as the starting address of a microprogram subroutine. Bits 1 through 4 of the address pointer can be modified by the macroinstruction m-field (IR_{0-3}) through four gates appearing on figure 9-66. The unary macroinstructions use the m-field as a secondary operation code. Modifying the address pointer permits starting at different microprogram addresses for each code. ECW bits 9 through 12 are called the Unary, Overlap, Interim and Modify pointers, respectively. The Unary pointer, when both it and the Modify bit are zero, signifies a Unary macroinstruction, and one of its functions is to enable the ECW address pointer to be modified by the m-field. When the Modify pointer is one, the primary purpose of the Unary pointer is to enable or inhibit the next instruction write function. The Overlap pointer, when equal to one, permits overlap of macroinstructions. It enables the next macroinstruction to be read from main memory early, without waiting for completion of the microprogram subroutine, and enables the setting of a next instruction resident (NIR) control bit, which signifies that the next macroinstruction is already available. The Interim pointer is coded into the ECW word for RK and RX format macroinstructions. These are double length instructions and require an interim memory reference to obtain the second half of the instruction word. The Modify pointer, when zero, combines with the Unary pointer to enable the address pointer to be modified by the m-field. When equal to one, it signifies the RI and RX format macroinstructions, which require an additional memory reference to fetch or store an operand. The upper three bits of the ECW word are the Memory Mode pointers and are interpreted as shown in figure 3-9. Note that bit 13 is the Read/Write bit, signifying read mode when zero and write mode when equal to one. On I/O sequences, memory mode pointer bits are generated according to IOC conditions and the ECW memory mode pointers are disabled.

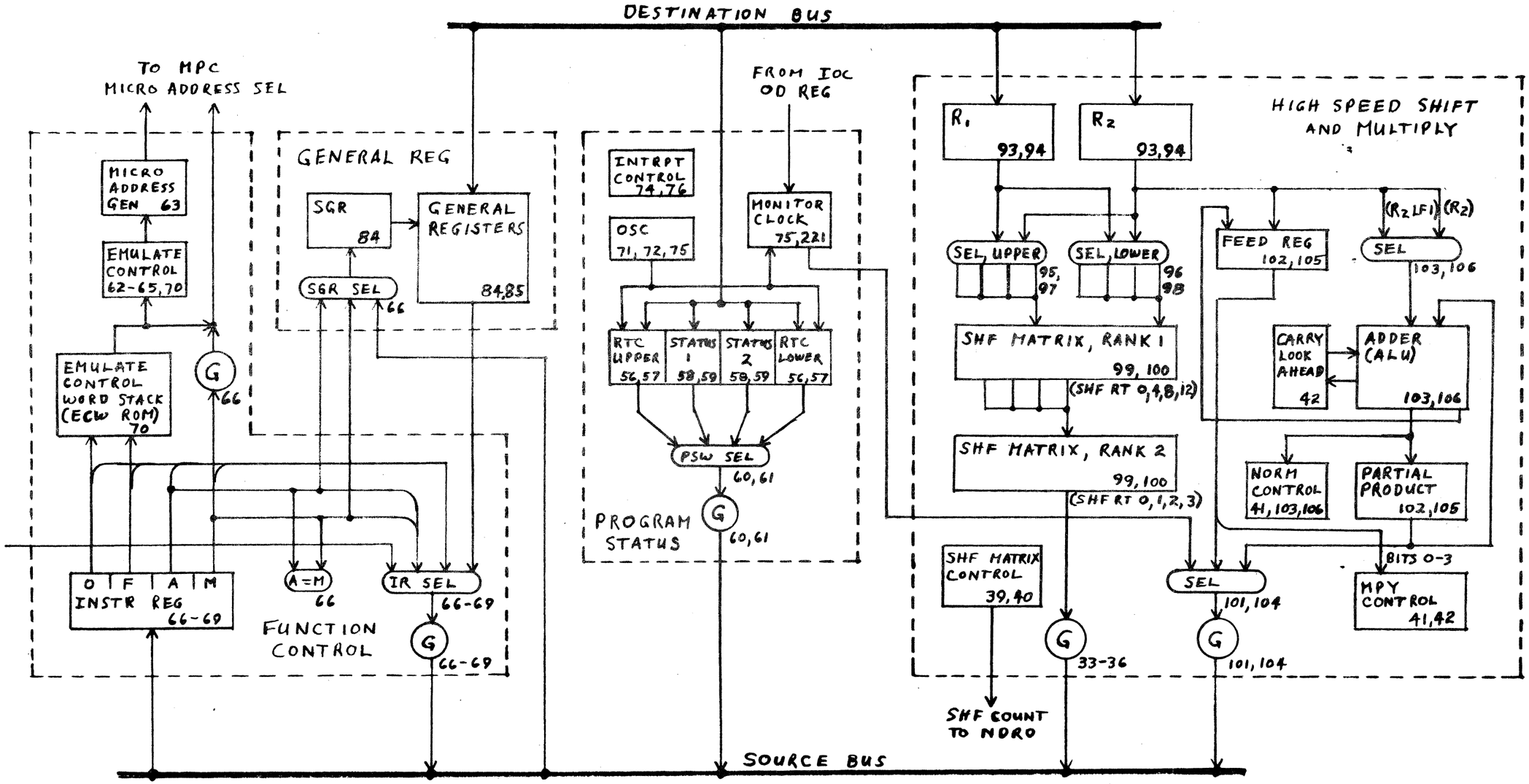


Figure 3-8. Processor/Emulator Functional Block Diagram

Table 3-8. ALU Shift Selector Functions

SELECTOR CONTROL BITS	FUNCTION
00	No Shift
01	Byte Shift (8 Places Circular)
10	Shift Right One Place
11	Shift Left One Place

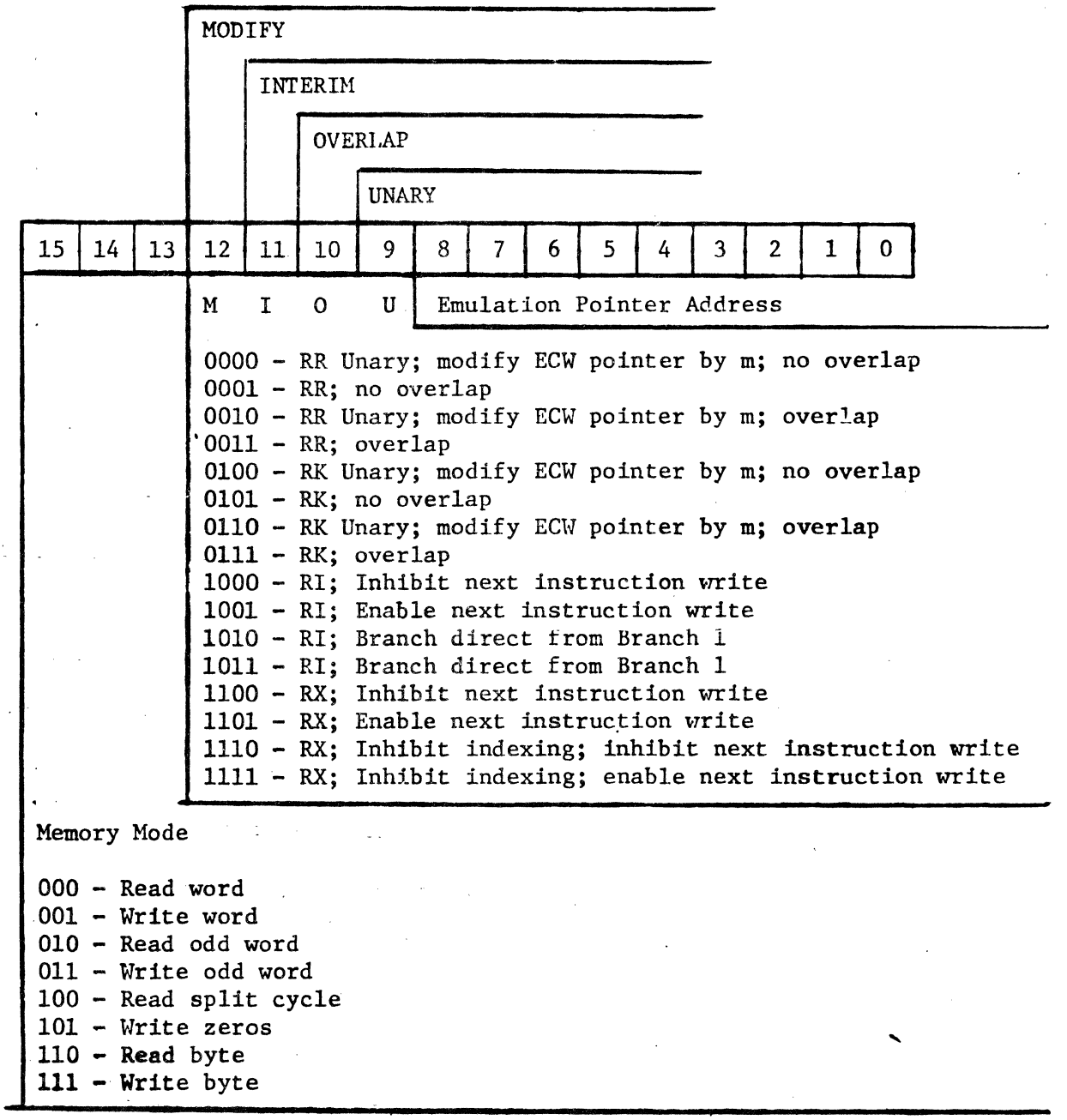


Figure 3-9. Emulator Control Word (ECW) Format

3-49. The emulate control circuits provide the hardwired control logic that functions together with the MPC and its microprogram to control the operation of the DPS. Emulate control circuits are scattered throughout the logic schematics but are mainly found on figures 9-62 through 9-65. For help in understanding these control circuits, refer to the functional operation description starting at paragraph 3- . Micro address generator circuits located on figure 9-63 generate the addresses of fixed microprogram subroutines (see table 3-2). These addresses are generally called interrupt addresses and interim addresses. They are placed on a common bus with similar addresses from the IOC (figure 9-201) and are sent to the micro address selector in the MPC.

3-50. The IR selector, when its output gates are enabled, places one of four inputs onto the source bus as follows:

1) Selector control bits = 00: IR (Instruction Reg)

2) Selector control bits = 01: IR lower byte, sign extended

3) Selector control bits = 10: CORDIC table from NDRO

4) Selector control bits = 11: General Register

3-51. General Registers. The general register section contains the general registers, the SGR, and the SGR selector. A general register stack consists of sixteen 16-bit registers. For the optional second set of general registers, a type 5520 card is used at location 12C instead of the type 5510. The second set is enabled when bit 14 of status register #1 is set. When a register is enabled and is addressed by the SGR register, it becomes active; that is, its contents appear on the stack output lines, and it is capable of being loaded. The general registers receive data directly from the destination bus; their output is placed on the source bus via the IR selector.

3-52. The 4-bit SGR register holds the general register address. It can be incremented by one each clock pulse. The 4-bit SGR selector selects one of four inputs to load into the SGR register as follows:

1) Selector control bits = 00: IR A-field

2) Selector control bits = 01: IR A-field with lower bit clear

3) Selector control bits = 10: IR M-field with lower bit clear

4) Selector control bits = 11: Lower four bits from source bus

3-53. Program Status Section. The program status section contains two status registers, the real time clock and monitor clock, the PSW selector, and the interrupt control circuits.

3-54. Status register #1 and status register #2 are 16-bit registers for storing program status information. Except for several bits, their setting and clearing is a program responsibility. They can be set and cleared using the unary control macroinstruction (Op Code 03). They receive their input from the destination bus. Figure 3-10 shows the significance of the bits in status register #1. Bits 1-3, when set, permit the honoring of interrupts of their assigned class; when cleared, they prevent the honoring of interrupts of their class. Bit 4 is used with the DMA

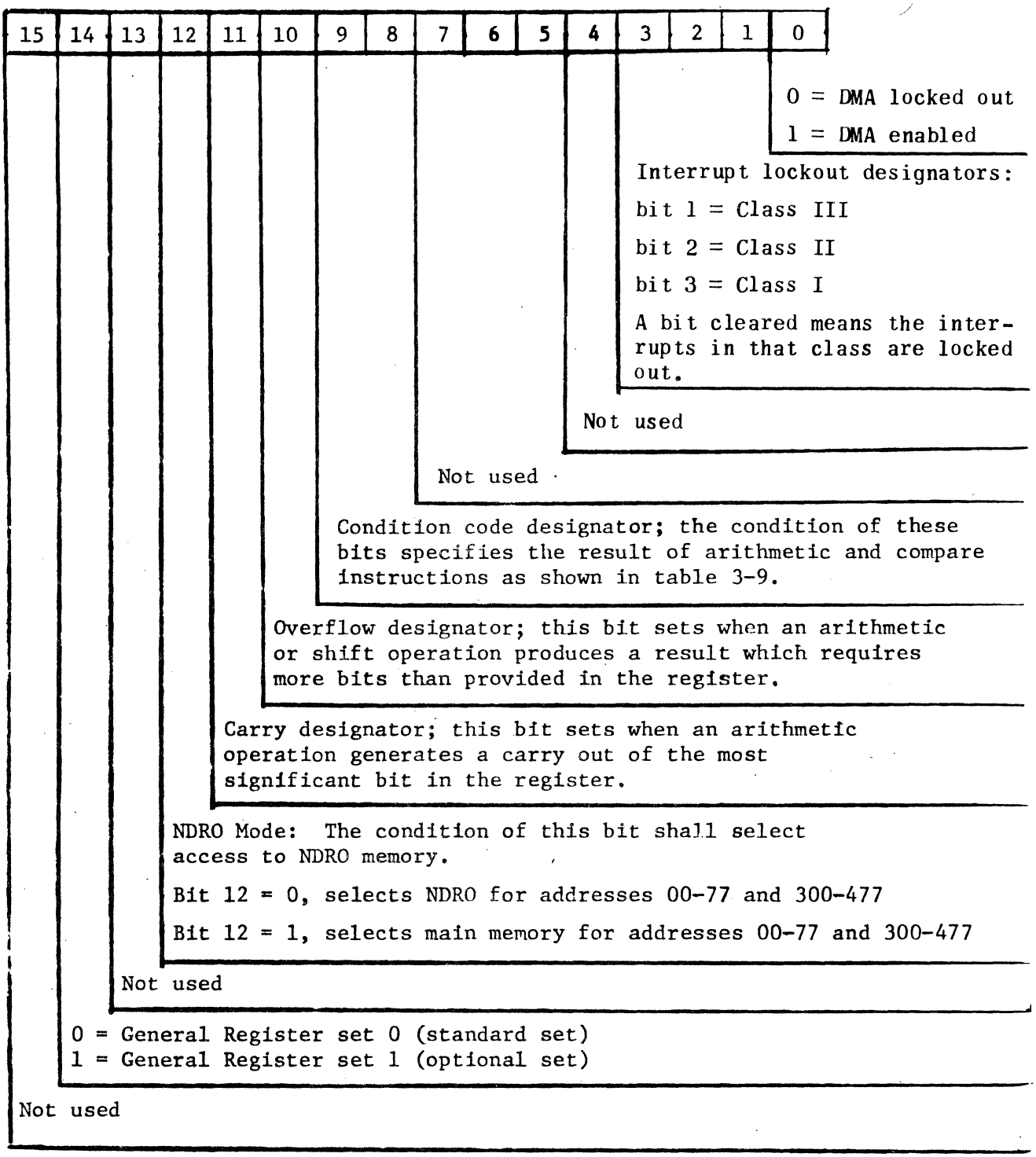


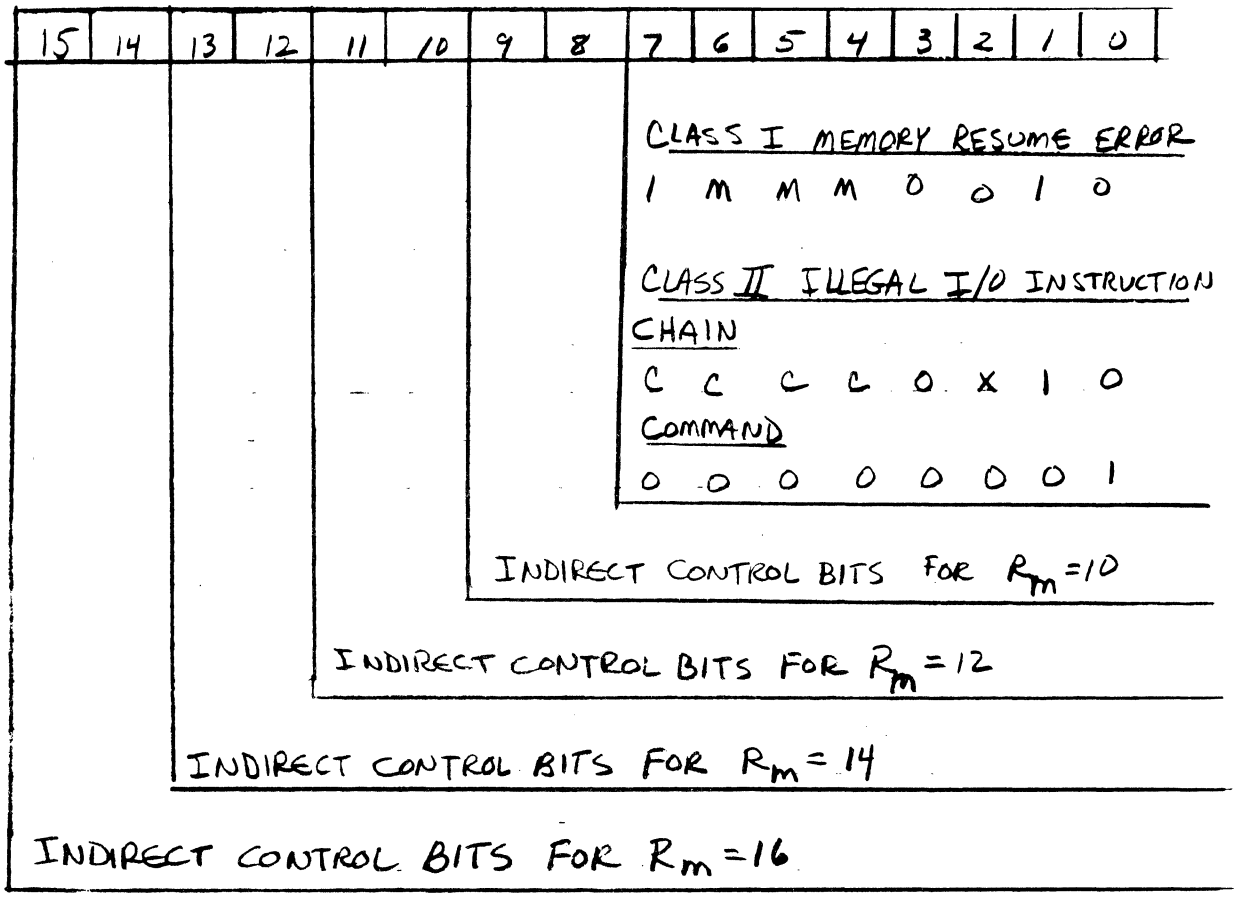
Figure 3-10. Status Register #1 Format

(direct memory access) option; when cleared it disables the DMA port to prevent the external device from gaining access to the main memory. Bits 5-7 are unassigned. Bits 8 and 9 (condition code designators), bit 10 (overflow designator), and bit 11 (carry designator) are capable of being set and cleared automatically as a result of arithmetic operations. See Table 3-9 for the significance of the condition code designators. Bit 12, when cleared, permits referencing the NDRO memory. Bit 14 selects the general register stack to be used. Bits 13 and 15 are unassigned. Figure 3-11 shows the significance assigned to the bits of status register #2. Bits 0-3 are unassigned. Bits 4-7 are assigned to the memory resume error, and show which 1K (1024 word) stack of main memory failed to respond. Bits 8-15 control the use of four general registers for direct or indirect addressing.

3-55. The real-time clock (RTC) register is a 32-bit register divided into two 16-bit registers designated RTC Upper and RTC Lower. It operates in conjunction with an internal oscillator or an external clock signal. The register can be loaded and its incrementing can be enabled and disabled under program control by means of the unary control macroinstruction (Op Code 03). It receives its input from the destination bus. When enabled, the register increments by one at each pulse from the oscillator, and generates the RTC overflow interrupt if the contents of RTC Lower change from all ones to all zeros (i.e., reach its maximum count). The internal RTC oscillator frequency is 1000 Hz. The external clock frequency can be from 0 to 50 KHz; its interface voltage must be 0v to -3v.

Table 3-9. Condition Code Designator Functions

CONDITION CODE		FUNCTION	
Bit	Value	Arithmetic Operation	Compare Operation
8	0	Zero	Equal
8	1	Not zero	Not equal
9	0	Positive	$R_a \geqslant R_m$ or Y
9	1	Negative	$R_a < R_m$ or Y
COMBINED VALUE			
Bit 9	Bit 8		
0	0	Zero	$R_a = R_m$ or Y
0	1	Not zero and positive	$R_A > R_m$ or Y
1	0	Not used	Not used
1	1	Not zero and negative	$R_a < R_m$ or Y



M INTERPRETATION

000 - MEMORY STACK 1
001 - MEMORY STACK 2
010 - MEMORY STACK 3
011 - MEMORY STACK 4
100 - MEMORY STACK 5
101 - MEMORY STACK 6
110 - MEMORY STACK 7
111 - MEMORY STACK 8

C INTERPRETATION

CCCC - CHANNEL NUMBER $0-17_8$

X INTERPRETATION

X = 0: INPUT CHANNEL
X = 1: OUTPUT CHANNEL

INDIRECT CONTROL BIT INTERPRETATION

00 - NORMAL ADDRESSING
01 - NORMAL ADDRESSING
10 - INDIRECT ADDRESSING (WORD AT Y)
11 - INDIRECT ADDRESSING WITH INDEXING (WORD AT Y + R_m)

Figure 3-11. Status Register #2 Format

3-56. The monitor clock register (also called interrupt clock register) is mainly used for monitoring the response time of peripheral devices for the IOC. It may be loaded and enabled by the Unary macroinstruction (Op Code 03). It is loaded from the IOC output data register, and decrements at the same frequency (internal or external) as selected for the RTC register. When operated on the internal clock (1000 Hz) the value of the least significant bit (LSB) is one msec, and a full 16-bit value is 65.536 seconds. When the contents of the register reaches zero, the Monitor Clock interrupt is generated.

3-57. The program status word (PSW) selector selects an output to gate onto the source bus as follows:

1) Selector control bits = 00: RTC upper

2) Selector control bits = 01: Status register #1

3) Selector control bits = 10: Status register #2

4) Selector control bits = 11: RTC lower

3-58. The interrupt control circuits initiate the processing of an interrupt and cause the micro address generator (para 3-49) to send the MPC the starting address of a microprogram subroutine for handling the interrupt (see table 3-2). Interrupts are divided into three classes with decreasing priority as follows: Class I, class II, and class III. Interrupts within a class are also assigned priority as shown in Table 3-10. The code assigned to the honored interrupt is placed onto the source bus through the I/O selector, figures 9-222 through 9-225. When an interrupt is honored, its class and all classes of a lower priority are locked out until released by the processor macroprogram. A higher priority class will interrupt a lower priority class unless it has been locked out by the program. An interrupt class (except power fault interrupt and CP instruction fault interrupt) can be enabled or locked out by the associated interrupt lockout designator in status register #1 (figure 3-10). The programmer, therefore, has complete control over the processing of interrupts. The power up master clear (initial master clear) clears the lockout bits in the status register, thus disabling most interrupts until the program is ready to handle them. The program, when ready, must execute a Load Status Reg #1 macroinstruction (Op Code 03, n = 5) to enable them. Processing of an interrupt consists of storing pertinent data to allow resuming normal macroprogram operation from point of interruption and then transferring control to a macroprogram subroutine to process the interrupt. Eight main memory references are required before transferring control to the interrupt subroutine. Addressing for the eight memory references is shown in figure 3-12. These eight addresses are not loaded into the P register but directly into the memory address register (MAR). When the eight memory references are completed, the contents of the P register, which now contains the address of the first instruction of the interrupt subroutine, are loaded into MAR to start executing the interrupt subroutine. Following is a step-by-step description of the interrupt process.

1. Terminate the current program sequence and lockout all interrupts during steps 2 through 5.

2. Store the contents of the P register, status registers #1 and #2, and the lower RTC register at assigned main memory addresses (figure 3-12).

Table 3-10. Interrupt Priority

CLASS	PRIORITY WITHIN CLASS	INTERRUPT	INTERRUPT CODE (BINARY)
CLASS I Hardware Errors	1	POWER FAULT - Generated by an out of tolerance voltage condition. (No lockout)	000
	2*	MEMORY RESUME - Generated when the main memory fails to acknowledge a request within 12 usec.	001
CLASS II Program Interrupts	1*	CP INSTRUCTION FAULT - Generated when the processor attempts to execute an instruction with an unused operation code, an operation code 00, or an operation code 7X. (No lockout)	000
	2*	IOC INSTRUCTION FAULT - Generated when the IOC attempts to execute an instruction with an unused operation code or any operation code other than 7X.	001
	3	Unassigned	010
	4*	EXECUTIVE RETURN - Generated when the computer executes the 03 RR, m = 0 instruction.	011
	5	RTC OVERFLOW - Generated when the contents of the RTC lower register (bits 0-15) increments from all ones to all zeros.	100
	6	MONITOR CLOCK - Generated when the contents of the monitor clock register equals zero.	101
CLASS III I/O Interrupts	1	INTERCOMPUTER (IC) TIME OUT - Generated in the transmitting computer when the receiving computer fails to accept a data word from the transmitting computer and return a resume signal within the allotted time.	11
	2	EXTERNAL INTERRUPT - Generated when the computer has stored an external interrupt word or, if serial interface (except NTDS), generated for a discrete interrupt.	00
	3	OUTPUT CHAIN (Output Monitor Interrupt) - Generated when the IOC executes the 73 RR, a = 1 (Chain Interrupt) instruction from an output chain.	10
	4	INPUT CHAIN (Input Monitor Interrupt) - Generated when the IOC executes the 73 RR, a = 1 (Chain Interrupt) instruction from an input chain.	01

* If the class lockout is set when this condition is generated, the DPS will stop at completion of the macroinstruction currently being executed.

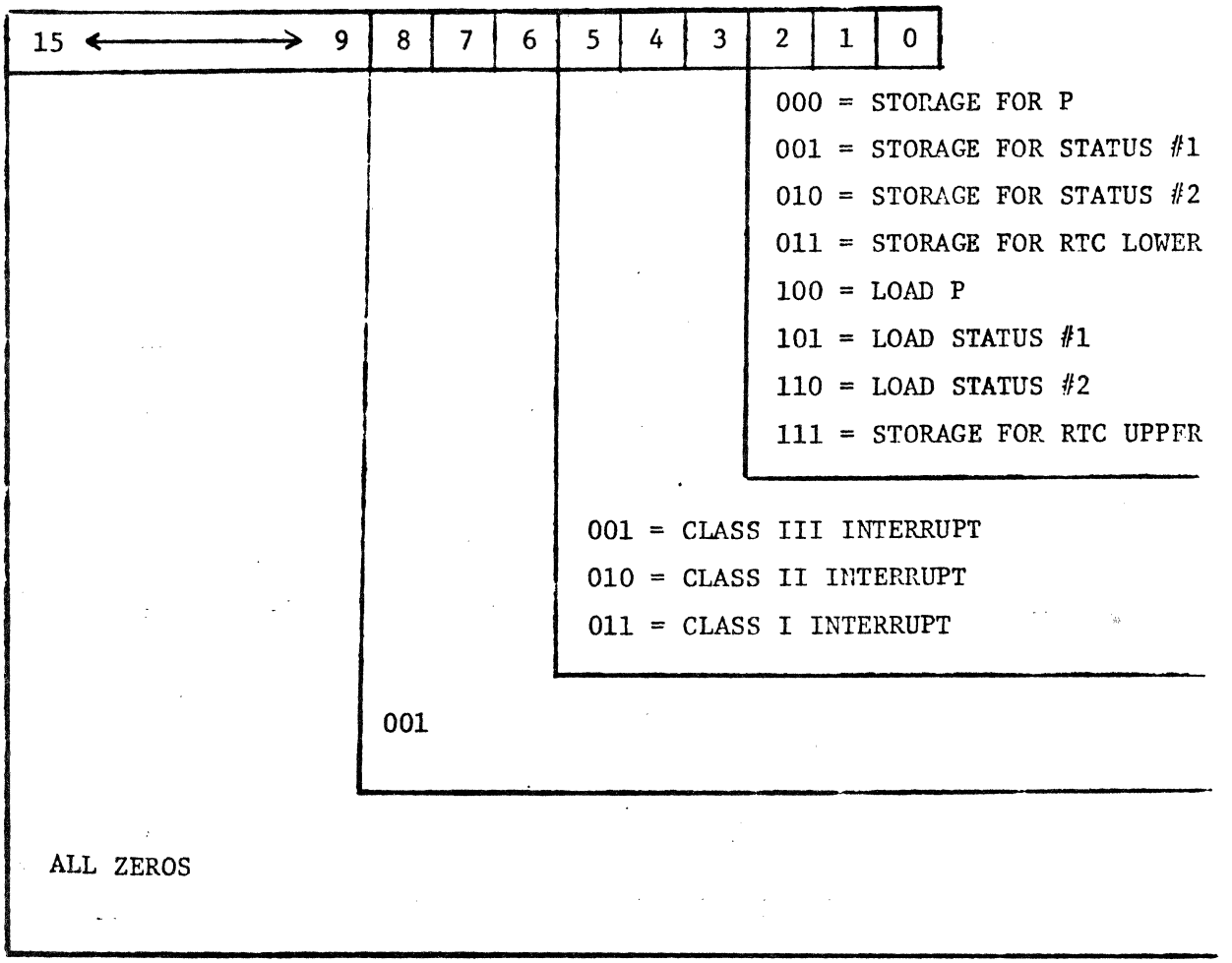


Figure 3-12. Interrupt Addressing

3. Load the P register with the interrupt entrance address. For class I and II interrupts, the entrance address is the sum of the contents of the Load P address from main memory and the index shown in figure 3-13. For class III interrupts, the index shown in figure 3-14 is added to the contents of the Load P address to form the entrance address.

4. Load status registers #1 and #2 with the contents of the assigned memory addresses.

5. Store the contents of the upper RTC register at its assigned memory address.

6. Enable honoring of any interrupts not locked out.

7. Execute the instruction at the interrupt entrance address.

3-59. High Speed Shift and Multiply Section. This section is dedicated to performing the shift and multiply functions for the DPS, including the functions of the Unary Shift macroinstruction (Op Code 04, RR). It performs these functions faster than possible in the arithmetic circuits of the MPC. A description of its main subsections follows.

3-60. R_1 and R_2 are also called shift register upper and shift register lower, respectively. They are the input registers for the high speed shift and multiply section. They receive their data directly from the destination bus. They have the capability of shifting their contents left or right one place when needed for arithmetic operations. The upper and lower selectors determine the nature of the input into their portion of the shift matrix, as required for circular, sign-fill, or zero-fill shifts. A ROM chip in the shift matrix control circuits (09, figure 9-39) is addressed according to the shift count and type of operation, and issues the signals to control each selector. Table 3-11 shows the contents of this chip. Both selectors operate as follows:

1) Selector control bits = 00: Insert zeros into matrix

2) Selector control bits = 01: Insert sign into matrix

3) Selector control bits = 10: Insert R_2 into matrix

4) Selector control bits = 11: Insert R_1 into matrix

3-61. The shift matrix has two ranks. Rank 1 shifts the data to the right 0, 4, 8, or 12 places; rank 2 shifts right 0, 1, 2, or 3 places. The two ranks together can shift any number of places from 0 to 15. They accomplish left shifts by shifting the complementary number of places right. A ROM chip in the shift matrix control circuits (24, figure 9-40) is addressed according to the type of shift and the shift count, and issues the signals to control each rank. Table 3-12 shows the contents of this chip. The output of the shift matrix is placed onto the source bus through gates appearing on figures 9-33 through 9-36. When performing the optional CORDIC functions, the count in the shift counter of the shift control circuits forms an address for referencing the CORDIC table in NDRO memory.

3-62. The fast shift and multiply section performs multiplication two bits at a time under the control of a multiply subroutine in the microprogram. Basically, the operations involved in the multiply are as follows:

1) Multiplier → R_2 reg; clear partial product reg.

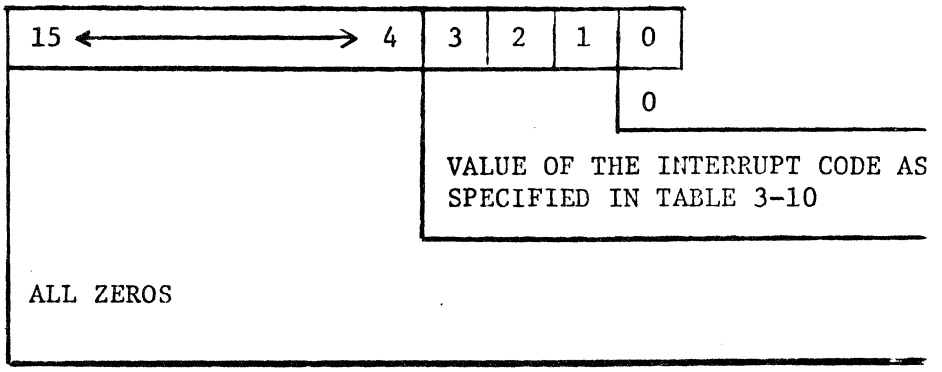


Figure 3-13. Class I and II Interrupt Entrance Address Index

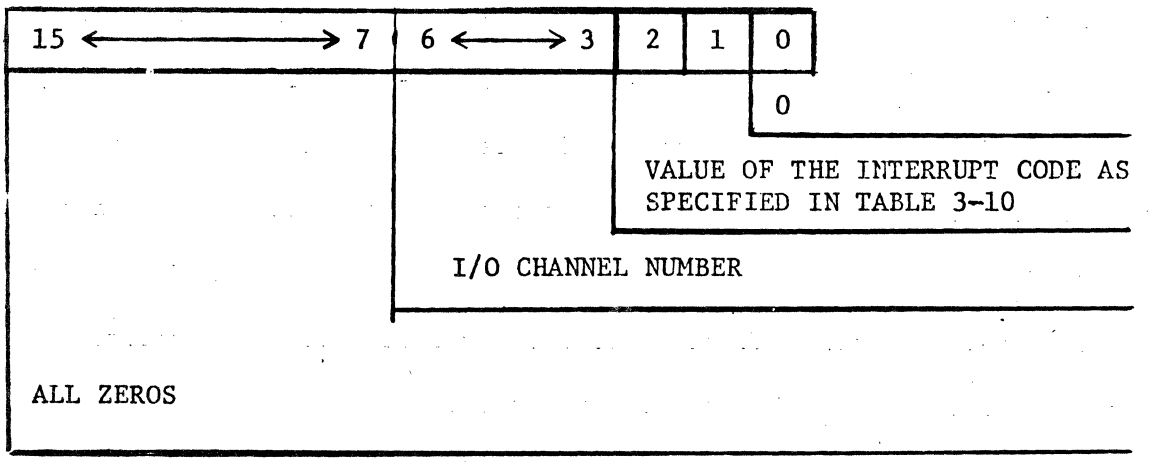


Figure 3-14. Class III Interrupt Entrance Address Index

Table 3-11. Microcode for Shift Control ROM 09

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
000	0	1110	060	48	1010
001	1	1111	061	49	1010
002	2	1011	062	50	1010
003	3	1010	063	51	1010
004	4	1110	064	52	0110
005	5	1111	065	53	0101
006	6	1011	066	54	0101
007	7	1010	067	55	0101
010	8	1011	070	56	1111
011	9	1010	071	57	1111
012	10	1110	072	58	1111
013	11	1111	073	59	1111
014	12	1011	074	60	1111
015	13	1010	075	61	1111
016	14	1110	076	62	0111
017	15	1111	077	63	0101
020	16	0000	100	64	0000
021	17	0000	101	65	0000
022	18	0000	102	66	0000
023	19	0000	103	67	0000
024	20	0000	104	68	0011
025	21	0000	105	69	0011
026	22	1000	106	70	1110
027	23	1010	107	71	1110
030	24	0000	110	72	0000
031	25	0000	111	73	0000
032	26	0000	112	74	0000
033	27	0000	113	75	0000
034	28	1000	114	76	0000
035	29	1010	115	77	0000
036	30	1110	116	78	0011
037	31	1111	117	79	0011
040	32	1111	120	80	0101
041	33	1111	121	81	0101
042	34	1111	122	82	0101
043	35	1111	123	83	0101
044	36	1111	124	84	0111
045	37	1111	125	85	0111
046	38	1111	126	86	1110
047	39	1111	127	87	1110
050	40	0000	130	88	0101
051	41	0000	131	89	0101
052	42	0000	132	90	0101
053	43	0000	133	91	0101
054	44	0000	134	92	0101
055	45	0000	135	93	0101
056	46	1100	136	94	0111
057	47	1111	137	95	0111

Table 3-11. Microcode for Shift Control ROM 09 (Cont)

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
140	96	1011	220	144	0101
141	97	1011	221	145	0101
142	98	1110	222	146	0101
143	99	1110	223	147	0111
144	100	1011	224	148	0111
145	101	1011	225	149	1110
146	102	1110	226	150	1110
147	103	1110	227	151	1000
150	104	1110	230	152	0101
151	105	1110	231	153	0101
152	106	1011	232	154	0101
153	107	1011	233	155	0101
154	108	1110	234	156	0101
155	109	1110	235	157	0111
156	110	1011	236	158	0111
157	111	1011	237	159	1110
160	112	1111	240	160	0111
161	113	1111	241	161	0111
162	114	1111	242	162	0111
163	115	1111	243	163	0111
164	116	1111	244	164	0111
165	117	1111	245	165	0111
166	118	1111	246	166	0111
167	119	1111	247	167	0111
170	120	0000	250	168	0000
171	121	0000	251	169	0000
172	122	0000	252	170	0000
173	123	0000	253	171	0000
174	124	0000	254	172	0000
175	125	0000	255	173	0000
176	126	0000	256	174	0000
177	127	0000	257	175	0000
200	128	0000	260	176	0000
201	129	0000	261	177	0000
202	130	0000	262	178	0000
203	131	0011	263	179	0000
204	132	0011	264	180	0000
205	133	1110	265	181	0000
206	134	1110	266	182	0000
207	135	1000	267	183	0000
210	136	0000	270	184	0000
211	137	0000	271	185	0000
212	138	0000	272	186	0000
213	139	0000	273	187	0000
214	140	0000	274	188	0000
215	141	0011	275	189	0000
216	142	0011	276	190	0000
217	143	1110	277	191	0000

Table 3-11. Microcode for Shift Control ROM 09 (Cont)

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
300	192	0111	360	240	0000
301	193	0111	361	241	0000
302	194	0111	362	242	0000
303	195	0111	363	243	0000
304	196	0111	364	244	0000
305	197	0111	365	245	0000
306	198	0111	366	246	0000
307	199	0111	367	247	0000
310	200	0101	370	248	0000
311	201	0101	371	249	0000
312	202	0101	372	250	0000
313	203	0101	373	251	0000
314	204	0101	374	252	0000
315	205	0101	375	253	0000
316	206	0110	376	254	0000
317	207	0110	377	255	0000
320	208	0000			
321	209	0000			
322	210	0000			
323	211	0000			
324	212	0000			
325	213	0000			
326	214	0000			
327	215	0000			
330	216	0000			
331	217	0000			
332	218	0000			
333	219	0000			
334	220	0000			
335	221	0000			
336	222	0000			
337	223	0000			
340	224	1110			
341	225	1110			
342	226	0000			
343	227	0000			
344	228	0000			
345	229	0000			
346	230	1000			
347	231	0010			
350	232	0111			
351	233	0111			
352	234	0000			
353	235	0000			
354	236	1000			
355	237	1110			
356	238	1110			
357	239	0011			

Table 3-12. Microcode for Shift Control ROM 24

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
400	0	0001	460	48	0000
401	1	0010	461	49	0000
402	2	0011	462	50	0000
403	3	0100	463	51	0000
404	4	0101	464	52	0000
405	5	0110	465	53	0000
406	6	0111	466	54	0000
407	7	1000	467	55	0000
410	8	1001	470	56	0000
411	9	1010	471	57	0000
412	10	1011	472	58	0000
413	11	1100	473	59	0000
414	12	1101	474	60	0000
415	13	1110	475	61	0000
416	14	1111	476	62	0000
417	15	0000	477	63	0000
420	16	1111	500	64	0001
421	17	1110	501	65	0010
422	18	1101	502	66	0011
423	19	1100	503	67	0100
424	20	1011	504	68	0101
425	21	1010	505	69	0110
426	22	1001	506	70	0111
427	23	1000	507	71	1000
430	24	0111	510	72	1001
431	25	0110	511	73	1010
432	26	0101	512	74	1011
433	27	0100	513	75	1100
434	28	0011	514	76	1101
435	29	0010	515	77	1110
436	30	0001	516	78	1111
437	31	0000	517	79	0000
440	32	1110	520	80	1111
441	33	1101	521	81	1110
442	34	1100	522	82	1101
443	35	1011	523	83	1100
444	36	1010	524	84	1011
445	37	1001	525	85	1010
446	38	1000	526	86	1001
447	39	0111	527	87	1000
450	40	0110	530	88	0111
451	41	0101	531	89	0110
452	42	0100	532	90	0101
453	43	0011	533	91	0100
454	44	0010	534	92	0011
455	45	0001	535	93	0010
456	46	0000	536	94	0001
457	47	0000	537	95	0000

Table 3-12. Microcode for Shift Control ROM 24 (Cont.)

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
540	96	1110	620	144	0001
541	97	1101	621	145	0010
542	98	1100	622	146	0011
543	99	1011	623	147	0100
544	100	1010	624	148	0101
545	101	1001	625	149	0110
546	102	1000	626	150	0111
547	103	0111	627	151	1000
550	104	0110	630	152	1001
551	105	0101	631	153	1010
552	106	0100	632	154	1011
553	107	0011	633	155	1100
554	108	0010	634	156	1101
555	109	0001	635	157	1110
556	110	0000	636	158	1111
557	111	1111	637	159	0000
560	112	0011	640	160	0000
561	113	0100	641	161	0001
562	114	0110	642	162	0010
563	115	1011	643	163	0011
564	116	0011	644	164	0100
565	117	1011	645	165	0101
566	118	1001	646	166	0110
567	119	1010	647	167	0111
570	120	1110	650	168	1000
571	121	0000	651	169	1001
572	122	0000	652	170	1010
573	123	0000	653	171	1011
574	124	0000	654	172	1100
575	125	0000	655	173	1101
576	126	0000	656	174	1110
577	127	0000	657	175	1111
600	128	1111	660	176	0001
601	129	1110	661	177	0010
602	130	1101	662	178	0011
603	131	1100	663	179	0100
604	132	1011	664	180	0101
605	133	1010	665	181	0110
606	134	1001	666	182	0111
607	135	1000	667	183	1000
610	136	0111	670	184	1001
611	137	0110	671	185	1010
612	138	0101	672	186	1011
613	139	0100	673	187	1100
614	140	0011	674	188	1101
615	141	0010	675	189	1110
616	142	0001	676	190	1111
617	143	0000	677	191	0000

Table 3-12. Microcode for Shift Control ROM 24 (Cont)

PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA	PROGRAM ADDRESS (OCTAL)	CHIP ADDRESS (DECIMAL)	CHIP DATA
700	192	0100	760	240	0100
701	193	1000	761	241	1000
702	194	1100	762	242	1100
703	195	0000	763	243	0000
704	196	0100	764	244	0100
705	197	1000	765	245	1000
706	198	1100	766	246	1100
707	199	0000	767	247	0000
710	200	0100	770	248	0100
711	201	1000	771	249	1000
712	202	1100	772	250	1100
713	203	0000	773	251	0000
714	204	0100	774	252	0100
715	205	1000	775	253	1000
716	206	1100	776	254	1100
717	207	0000	777	255	0000
720	208	1100			
721	209	1000			
722	210	0100			
723	211	0000			
724	212	1100			
725	213	1000			
726	214	0100			
727	215	0000			
730	216	1100			
731	217	1000			
732	218	0100			
733	219	0000			
734	220	1100			
735	221	1000			
736	222	0100			
737	223	0000			
740	224	1011			
741	225	0111			
742	226	0011			
743	227	1111			
744	228	1011			
745	229	0111			
746	230	0011			
747	231	1111			
750	232	1011			
751	233	0111			
752	234	0011			
753	235	1111			
754	236	1011			
755	237	0111			
756	238	0011			
757	239	1111			

2) R_2 (multiplier) → feed reg.; multiplicand → R_2 reg.

3) Set cycle counter = 6 (to repeat 7 cycles).

4) Initiate Repeat.

5) Cycle 7 times (see figure 3-15). Each cycle looks at the lower bits in the feed register (multiplier) and controls the adder and the insertion of the R_2 register (multiplicand) into the adder as indicated in table 3-13. On each cycle, the adder output is shifted right two places into the partial product register and the two rightmost (least significant) bits are shifted into the most significant bit positions of the feed register. The feed register also shifts two places right so the following cycle can look at the next bits of the multiplier. When the seven cycles are completed, the least significant half of the product is in the feed register, and the most significant half is in the partial product register.

6) Store least significant half of product.

7) Store most significant half of product.

8) Set condition code.

3-63. 26, 27, and 30 of the multiply control circuits (figure 9-42) provide the signals to control the inputs and functions of the multiply adder. The high speed multiply uses the $S_0 = 1$ and $S_1 = 1$ selections. The $S_1S_0 = 00$ selection is used for normalize (scale) and other arithmetic functions, if performed in this section. A ROM chip (22, figure 9-42), addressed according to the type of shift and the instruction count, issues other control signals. Table 3-14 shows the addressing and the contents of this chip.

3-64. For the Scale Factor macroinstruction (04 RR, m = 3), normalize circuits determine the position of the first significant bit in a word, develop a shift count, and cause the word to be shifted accordingly. The word is placed into the R_2 register and sensed at the output of the multiply adder. The normalize detectors sense zeros; therefore, if the word is positive it is complemented by the multiply adder. The most significant 16 bits of double length words are checked first, then the least significant 16 bits. Circuits appearing on figure 9-41 generate the shift count. Double length words require two passes. A flip-flop stores whether or not a significant bit was detected in the first pass, and a 4-bit register holds the shift count, if any, generated on the first pass. Bit 4 of the generated shift count is low (active) only if normalization occurs on the second pass (second half of the double length word). Bit 5 goes low (active) only if no significant bit is detected in either pass, and produces a count of 1000000_2. The shift count is placed onto the source bus through the MPC source selector. The count generated is one count high, so it is decremented by the microprogram. It is then placed into the shift counter and the word is shifted left that many places by the shift matrix to produce the normalized word.

3-65. MEMORY INTERFACE. Figure 3-16 is a block diagram of the memory interface section. The memory interface transfers data to and from the main memory. It divides into four main sections: memory address control, memory data interface, memory control, and NDRO. The following paragraphs describe these sections and their subsections.

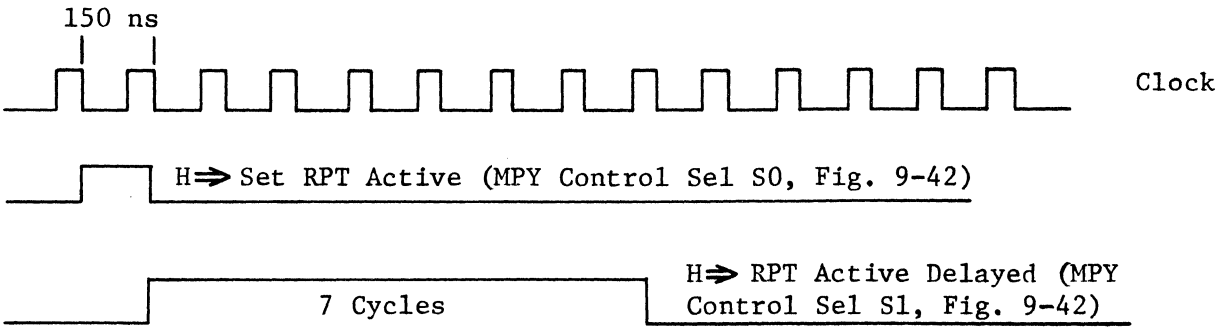


Figure 3-15. Multiply Timing

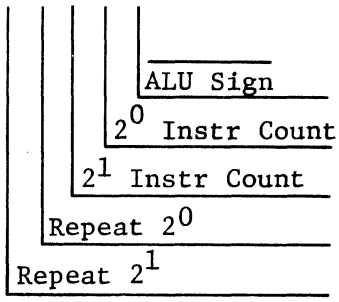
Table 3-13. Adder Functions, High Speed Multiply

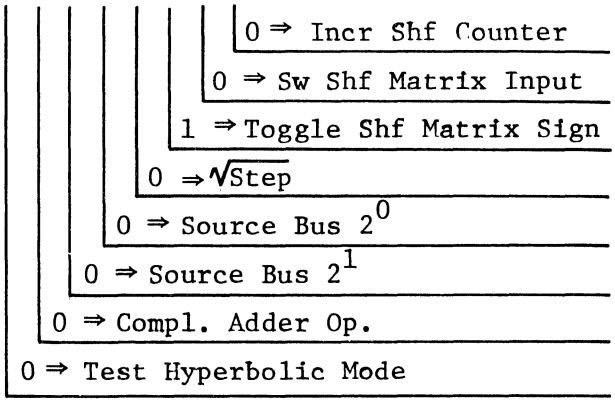
	Feed Reg 3 2 1 0	
Set RPT Active (S0) = 1 (Initiate Repeat)	X X 0 0	Add Zeros
	X X 0 1	Add Multiplicand
	X X 1 0	Subtract 2X Multiplicand
	X X 1 1	Subtract Multiplicand
RPT Active Delayed (S1) = 1 (7 repeated cycles)	0 0 0 X	Add Zeros
	0 0 1 X	Add Multiplicand
	0 1 0 X	Add Multiplicand
	0 1 1 X	Add 2X Multiplicand
	1 0 0 X	Subtract 2X Multiplicand
	1 0 1 X	Subtract Multiplicand
	1 1 0 X	Subtract Multiplicand
	1 1 1 X	Subtract Zeros

(See U7, U11, and U15, figure 9-42)

Table 3-14. Microcode for Multiply Control ROM 22

PROGRAM ADDRESS	CHIP ADDRESS	MICROCODE
0 0 0 0 0	0	0 1 1 1 1 1 1 1
0 0 0 0 1	1	0 1 1 1 1 1 1 1
0 0 0 1 0	2	1 1 1 1 1 1 1 1
0 0 0 1 1	3	1 0 1 1 1 1 1 1
0 0 1 0 0	4	1 0 1 1 1 0 0 0
0 0 1 0 1	5	1 1 1 1 1 0 0 0
0 0 1 1 0	6	0 0 0 0 0 0 0 0
0 0 1 1 1	7	0 0 0 0 0 0 0 0
0 1 0 0 0	8	1 0 1 1 1 1 1 1
0 1 0 0 1	9	1 1 1 1 1 1 1 1
0 1 0 1 0	10	1 0 1 1 1 1 1 1
0 1 0 1 1	11	1 1 1 1 1 1 1 1
0 1 1 0 0	12	1 1 1 1 1 0 0 0
0 1 1 0 1	13	1 0 1 1 1 0 0 0
0 1 1 1 0	14	0 0 0 0 0 0 0 0
0 1 1 1 1	15	0 0 0 0 0 0 0 0
1 0 0 0 0	16	1 1 1 1 1 1 1 1
1 0 0 0 1	17	1 1 1 1 1 1 1 1
1 0 0 1 0	18	1 1 1 1 1 0 0 0
1 0 0 1 1	19	1 1 1 1 1 0 0 0
1 0 1 0 0	20	0 0 0 0 0 0 0 0
1 0 1 0 1	21	0 0 0 0 0 0 0 0
1 0 1 1 0	22	0 0 0 0 0 0 0 0
1 0 1 1 1	23	0 0 0 0 0 0 0 0
1 1 0 0 0	24	1 1 1 1 0 1 1 1
1 1 0 0 1	25	1 1 1 1 0 1 1 1
1 1 0 1 0	26	1 1 0 0 1 1 1 1
1 1 0 1 1	27	1 0 1 0 1 1 1 1
1 1 1 0 0	28	0 0 0 0 0 0 0 0
1 1 1 0 1	29	0 0 0 0 0 0 0 0
1 1 1 1 0	30	0 0 0 0 0 0 0 0
1 1 1 1 1	31	0 0 0 0 0 0 0 0





(Readcut Enable = RPT Active Delayed ⌐ RPT 2^0)

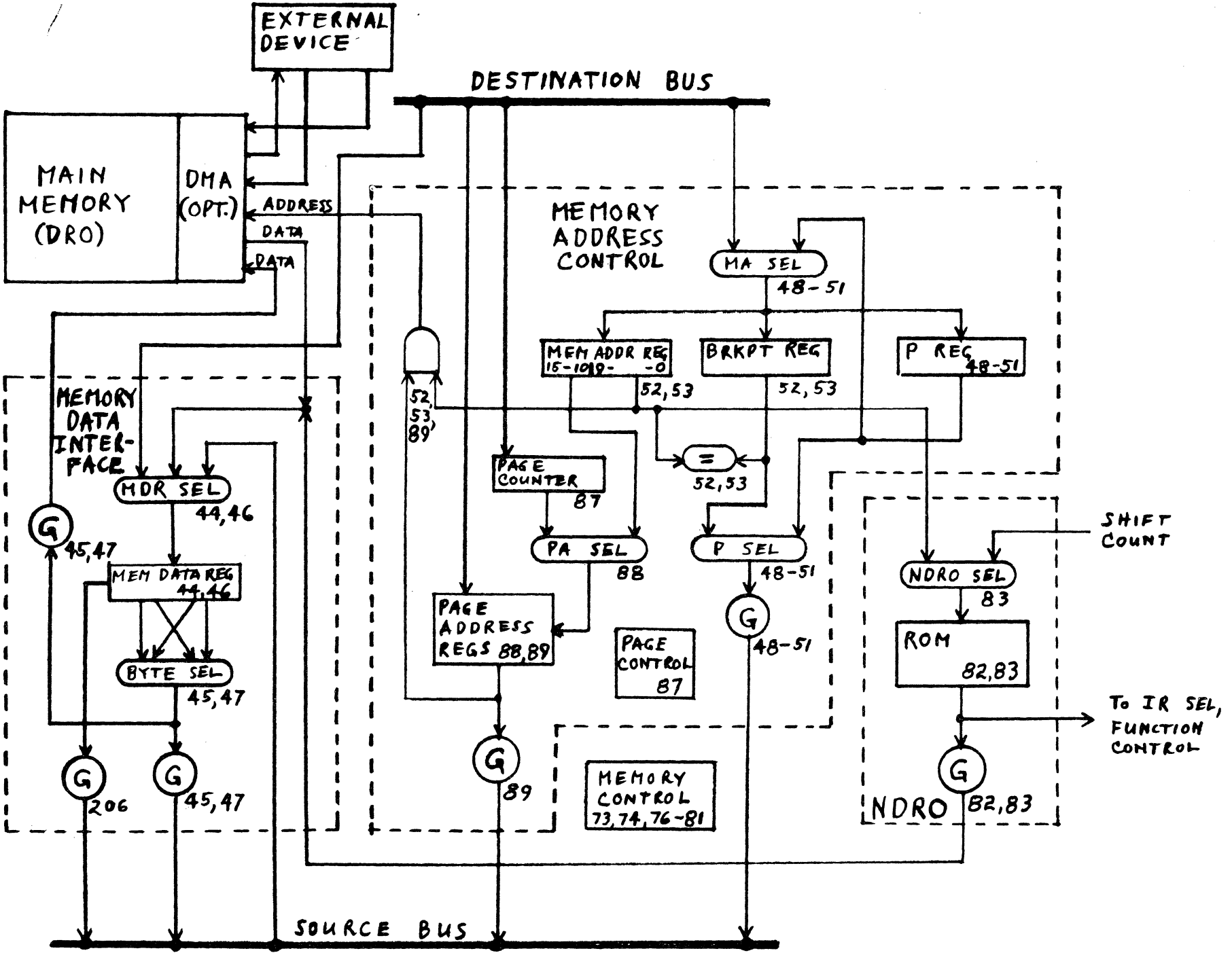


Figure 3-16. Memory Interface Functional Block Diagram

3-66. Memory Address Control. The memory address control circuits provide the address information to the main memory or the NDRO memory.

3-67. The program address register (P register) holds the address of the next macroinstruction. To read the next instruction, its contents are loaded into the memory address register (MAR) through the memory address selector. It then advances by one to be ready for reading the subsequent instruction. Double length instructions require two memory references, with the P register advancing after each reference. Addresses of operands, addresses for Execute Remote instructions (Op Code 35 RK), and addresses for IOC memory references are not placed into the P register; they are placed directly into the MAR from the destination bus through the memory address selector. On jump instructions, the new address is loaded into the P register from the destination bus.

3-68. The breakpoint register permits stopping the DPS when a pre-selected memory address is referenced. This function is especially useful when troubleshooting. The breakpoint register can be loaded manually from the control panel. It works in conjunction with the Read and Write Breakpoint switches on the panel. If the appropriate Read or Write Breakpoint switch is set, the DPS will stop if it references the address contained in the breakpoint register. Comparator circuits appearing on figures 9-52 and 9-53 check for equality between the contents of MAR and the breakpoint register. Gates appearing on figure 9-81 generate a stop signal if equality occurs at a write request while the breakpoint WRITE switch is activated or at a read request while the breakpoint READ switch is activated.

3-69. The address from the memory address register (MAR) is transmitted to main memory through the page addressing circuits. This provides a capability often called relative addressing or virtual memory. It allows a block of program to be placed into any "page" of the main memory, and still be correctly addressed. All memory addresses are subject to page addressing; many of these addresses may already have been indexed or indirectly formed. Page addressing is illustrated in figure 3-17. For page addressing, the lower ten bits of MAR are transmitted directly to the memory. They represent a page of 1024 (1K) addresses. The upper six bits select one of 64 page address registers. The contents of that register become the upper six bits of the memory address and effectively select one of 64 1K pages. The page address registers must be correctly loaded by program means, using the operation code 54 macroinstructions. The uppermost bit of the page address registers is set by the control logic or by bit 15 when loading. It is used as a flag bit. When loading or storing the page address registers, the register number (address) is placed into the page counter. For multiple loads and stores, the counter advances to successive addresses. On master clears, an initialize subroutine residing in address 17_8 - 23_8 of micro memory loads each page address register with its own address, i.e. (00) = 0, (01) = 1, --- (77_8). Therefore, in the initial condition, all memory references are to the true memory addresses.

3-70. Memory Data Interface. The memory data interface section transfers data to and from the main memory. It comprises the memory data register (MDR), the MDR selector, and the byte selector.

3-71. The MDR holds the data being transmitted to or from the memory. It receives its input through the MDR selector as follows: S_1S_0 = 00, Source Bus; S_1S_0 = 01, Destination Bus; S_1S_0 = 11, Memory Data In. The data on the Memory Data In lines can be either from the main memory or the NDRO memory. Data transferring in from memory is gated to the source bus through the byte selector. Data transferring out is gated to the main memory through the byte selector. The byte selector normally

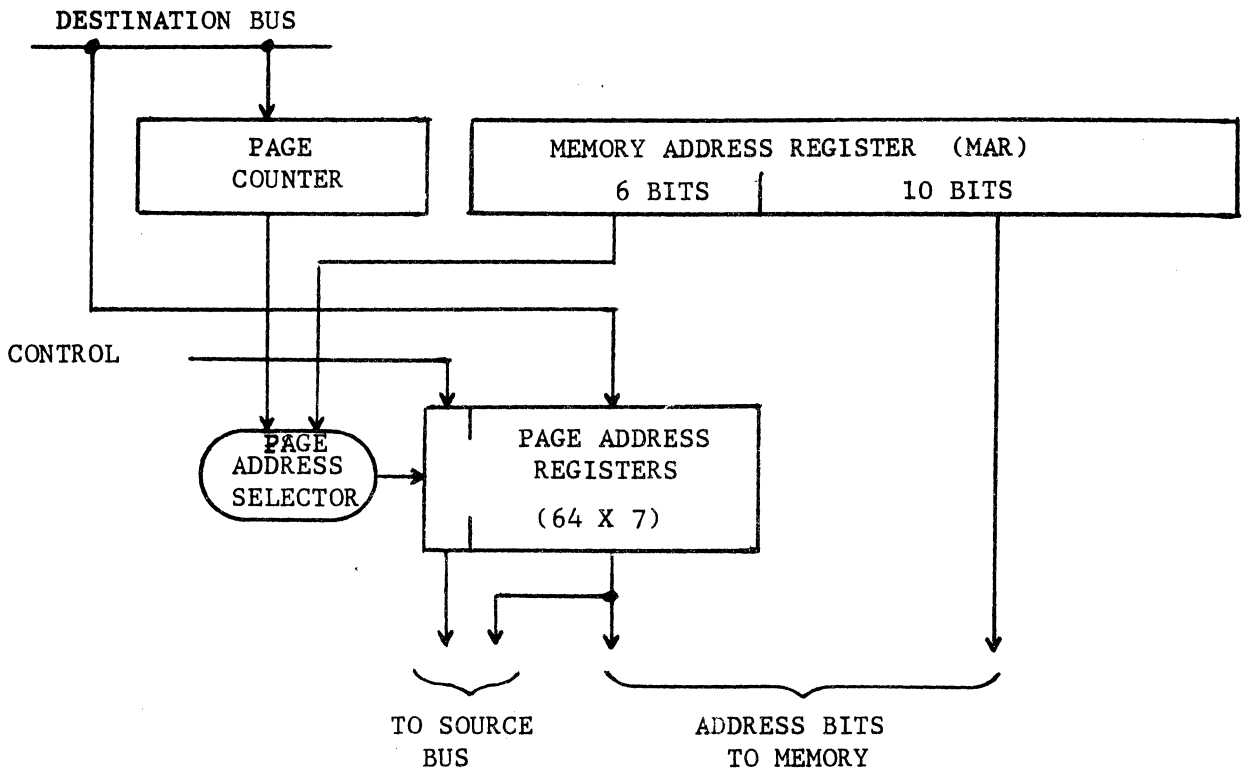
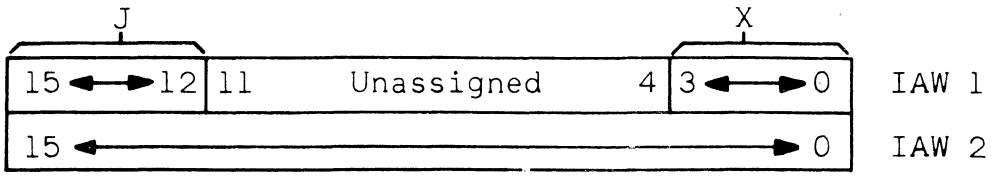


Figure 3-17. Page Addressing Function

transfers the data bit for bit, but when the Reverse Byte signal is present, it interchanges the upper and lower eight bits. MDR bits 12 through 14 are also sent to gates appearing on figure 9-206 which enable the microprogram to look at the J-value of indirect addresses.

3-72. Indirect addressing of operands is possible on RX format macroinstructions with m-field values of 10, 12, 14, or 16. The programmer controls indirect addressing by specifying these m-values and by controlling the contents of the indirect address control bits in status register #2 (see figure 3-11). Indirect address words are double length and have the format shown in figure 3-18. The J-value of the first word determines the formation of the operand address. J-values of 4 through 7 specify a cascaded indirect word; that is they cause formation of the address of another double length indirect word. Cascading may be repeated any number of times before the final operand address is formed.

3-73. NDRO. The DPS has 192 words of semiconductor ROM called the NDRO (non-destructive read-out) memory. It is divided into two blocks. One block contains 64 words and is assigned addresses $00\text{-}77_8$; the other block contains 128 words and is assigned addresses $300 - 477_8$. Generally, the entire 192 words are used for a bootstrap load program. The programs vary according to the channel and type of peripheral device used for program loading. ROM memories are programmed at the time of manufacture and cannot be changed except by substituting a different ROM card. Access to the NDRO memory is exclusive to the processor, and is performed when the NDRO mode bit (bit 12) in status register 1 is clear. The BOOTSTRAP 1-2 switch on the operator's panel permits choosing either of two bootstrap programs



J Value	Address determination
0	Final operand at address specified by (IAW 2)
1	Final operand at address specified by (IAW 2) + (R_x)
2	Final operand at address specified by (IAW 2) + (R_m)
3	Final operand at address specified by (IAW 2) + (R_{m+1})
4	Cascaded IW at address specified by (IAW 2)
5	Cascaded IW at address specified by (IAW 2) + (R_x)
6	Cascaded IW at address specified by (IAW 2) + (R_m)
7	Cascaded IW at address specified by (IAW 2) + (R_{m+1})
10-17	Unassigned

Figure 3-18. Indirect Address Format

combined in the NDRO. In the BOOTSTRAP 2 position, the switch enables the execution of a conditional jump instruction (operation code 40) with an a-designator of 7. The switch may also be used, at the programmer's discretion, to control branching in other programs.

3-74. The NDRO memory is addressed through the NDRO selector. The address is normally from the MAR. However, for the optional CORDIC operations, additional ROM locations are provided in the NDRO, and they are addressed from the shift counter. Bit 2 from the macroinstruction register m-field, inserted as bit 5 of the shift count, determines whether the NDRO memory reference is for a trigonometric or a hyperbolic function. The NDRO memory output is gated onto the memory data in bus for gating through the MDA selector into the memory data register. For CORDIC operations, the NDRO output is gated onto the source bus via the IR selector.

3-75. Memory Control. These circuits control the memory interface. They generate the control signals for the memory and receive control signals from the memory. Refer to the main memory description (para. 3-78) for a discussion of these signals and their effect on memory operation. The memory control circuits are directed by memory mode bits from the S-field on Micro Control (F=15) microinstructions (see Appendix A), or from bits 15-13 of the emulator control word (see figure 3-9). These bits are gated into a storage register and translated by circuitry shown on figure 9-78. Mode bit configurations of 000 or 010 generate a whole word read operation; the full cycle signal is active, and the write upper (zone 2) and write lower (zone 1) signals are inactive, causing a read operation for both bytes. Mode bit configurations of 001 and 011 generate a whole word write operation, with the write upper and write lower signals active, to cause a write operation in both bytes. The write zeros operation (101) is identical except that the MDR to memory bus signal is disabled, so the bus remains zero to write zeros into memory. 010 and 011 generate the memory address 2^0 signal, forcing an odd address. A read byte operation (110) is similar to a whole word read, except that bit 15 of the condition register is sampled by circuitry appearing on figure 9-76 to generate the byte point odd signal on figure 9-78. R_m 2^0 of Byte Load macroinstructions is the byte identifier and is shifted off into condition register bit 15. If the upper byte is required ($CR2^{15}$ clear), the reverse byte signal is generated, causing the upper byte from MDR to be gated into the lower position through the byte selectors. On write byte operations (111), $CR_2{}^{15}$ causes generation of either the write upper or write lower signals. Mode bit configuration 100 generates the read split cycle (read, modify, and restore) operation. The full cycle signal is disabled and a split cycle flip-flop sets to enable generation of the write initiate signal (figure 9-79).

3-76. The write initiate signal is generated only for the restore portion of the split cycle operation. The read initiate signal (figure 9-79) initiates all other memory operations. The load MAR and initiate signal (figure 9-77, element 12) is present on emulate starts and branches, and on Micro Control (F=15) microinstructions with D=4 or 14. It produces the signal called "words" (figure 9-78) to cause the setting of the memory request flip-flop (07905) and generation of the read initiate signal (figure 9-79). When the data available signal comes from the memory, it clears the memory request flip-flop. This sets a data available control flip-flop to disable the clear signal until the memory drops the data available signal.

3-77. Time delay flip-flops 08 and 09 on figure 9-79 control the memory resume fault. The read initiate enable signal sets flip-flop 09. Normally, it is cleared again when the memory request flip-flop clears. If the data available signal doesn't arrive before the time delay expires, flip-flop 08 sets. After another

time delay, its output appears as an artificial resume signal to clear the memory request flip-flop and set the resume error flip-flop (figure 9-76). The total delay for the two time delay flip-flops is factory preset at approximately 12 nsec.

3-78. MAIN MEMORY (MM). The MM stores instructions and data for the macroprogram and, if the optional direct memory access (DMA) logic is installed, can be directly accessed by external devices. The memory is a random-access core storage device using three-wire, 2-1/2D organization. It is capable of operating in two modes: full cycle (read/restore or clear/write) and split cycle (read/modify/write). The memory performs a full cycle in 750 nanoseconds and a split cycle within 1000 nanoseconds. Access time is 425 nanoseconds maximum, measured from the leading edge of the initiate signal, to the time data from a specified address is stable on the data output lines. The basic storage unit in the memory is the Memory Array Board (MAB). It is an 8K word X 16 bit core array. The memory chassis can accommodate up to eight of these 8K arrays, giving a storage capacity of 65K words X 16 bits.

3-79. Memory Organization. The memory core arrays and all related circuitry are contained on three types of circuit boards: memory control board (MCB), memory data board (MDB), and memory array board (MAB). The memory is arranged into two memory banks, each containing a control board, a data board, and from one to four array boards. See figure 3-19. As supplied, the memory chassis contains the control boards and data boards for both banks, and is designated the Control, Memory Unit. Array boards, designated Core Memory Unit, are inserted to produce the desired memory size. The functions of the individual boards are detailed below.

3-80. The memory control board (MCB) contains most of the interface circuitry and control logic for the memory bank. Included on the MCB are:

1) The timing and control logic, which receives the control signals from the processor and generates the internal timing;

2) The address register, which stores the incoming address information and drives the address decoding logic;

3) Address decoding logic, which selects the address and enables the read and write drivers;

4) Module read and write drivers, which provide internal control signals to access a memory address;

5) An optional configuration of the MCB also contains a portion of the DMA logic.

3-81. The memory data board (MDB) contains the following circuits:

1) The data register, which receives and holds data read out of the memory or data to be written into the memory;

2) The data out gates, which gate the contents of the data register to the data output buss;

3) The module write bit gates, which gate the contents of the data register to the bit switches on the array board;

4) An optional configuration of the MDB contains, in addition to the above, the balance of the DMA logic.

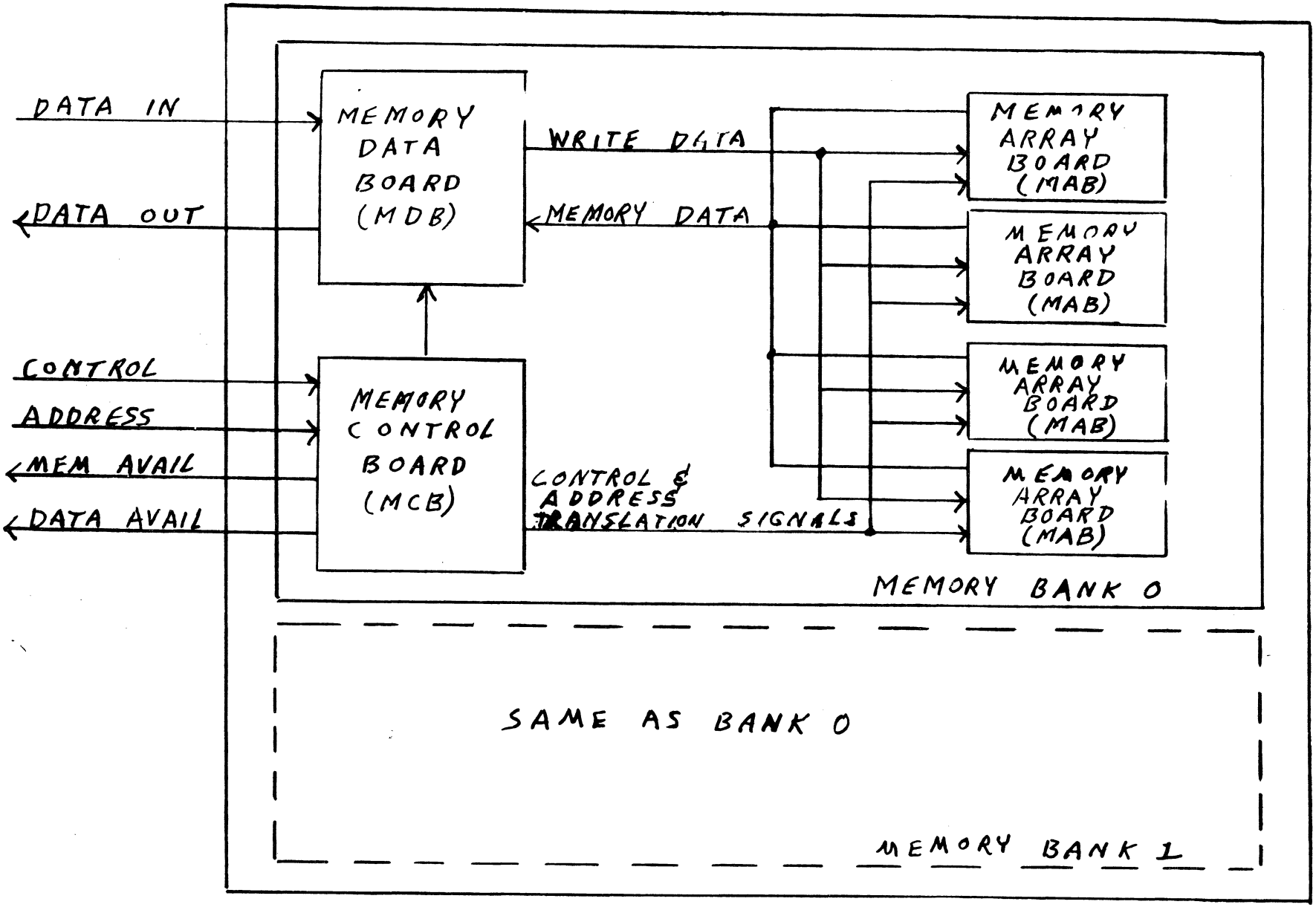


Figure 3-19. Main Memory Block Diagram

3-82. The memory array board (MAB) contains the core arrays and switching and diode circuits, as follows:

1) The core array. This is the basic storage area for the MAB and consists of an 8K X 16 bit core array arranged on one double-sided board. The 8K array further subdivides into 16 mats, one for each bit;

2) The sense amplifiers;

3) A word switch-diode matrix, containing two sets of 16 X 16 diode pairs (one set for each half of the core array).

4) A bit switch-diode matrix containing 16 sets of 4 X 4 diode pairs (one set for each bit mat).

3-83. Operating Modes. The memory is capable of operating in two modes: Full cycle (read/restore or clear/write) and split cycle (read/modify/write). During a full cycle read, data is fetched, or read out from a selected address in memory, and then the same data is restored to the same address location. During a full cycle write, existing data is cleared from a selected address in memory, and new data is written into that address. During a split cycle, data is read out from a given location and replaced wholly or in part with modified data.

3-84. Interface Control Signals. Table 3-15 lists the memory interface signals. The control signals received by - and transmitted from - the memory interface regulate the operation of the memory and inform the controlling equipment (processor or DMA device) of the memory status. The interface signals are described in detail below.

3-85. The +memory select signal functions as an address signal by selecting one of the two banks of memory. Only one of the two memory select signal lines can be high (active) at one time. The signal, in conjunction with the memory initiate, activates the control circuits of the selected memory bank. The signal is received by the memory at the start of both a full and split cycle operation and at the write initiate time of a split cycle operation. The signal must remain active at the memory interface for a minimum of 100 ns.

3-86. The +read initiate signal initiates all memory operations except the write portion of a split cycle operation. The signal activates the memory bank control circuits and must remain active for a minimum of 75 ns.

3-87. The +full cycle signal is received at the start of a full cycle operation. The signal activates circuits which enable the memory timing chain to cycle through twice without interruption, once for the clear or read portion of the memory cycle, and once for the write or restore portion. The activated circuits also help to initialize the control circuits at the end of the operation. The -full cycle signal is received at the start of a split cycle operation and specifies a read/modify/write. The signal activates circuits which a) enable the memory timing chain, b) enable the memory available signal at the end of the read cycle, c) enable re-initiation of the timing chain at the start of the write cycle of the operation, and d) enable initialization of the control circuits at the end of the operation. The signal must remain in the desired state for a minimum of 100 ns after the leading edge of the initiate signal goes high.

Table 3-15. Memory Interface Signals

Inputs to Memory:	
Address In	(15 lines)
Data In	(16 lines)
±Full Cycle	(1 line)
+Read Initiate	(1 line)
+Write Initiate	(1 line)
-Power Fault	(1 line)
-Zone Write Upper	(1 line)
-Zone Write Lower	(1 line)
+Memory Select	(2 lines)
Outputs from Memory:	
Data Out	(16 lines)
-Data Available	(1 line)
+Memory Available	(1 line)

3-88. The -power fault signal is a reset signal generated by the DPS power supply during initial power up, or when the power supply shuts down due to input power failure. The signal causes the memory to clear its control circuits and address register.

3-89. The +write initiate signal is received at the start of the write portion of a split cycle operation and is an order to write data into the memory. The signal activates the memory bank control circuits and must remain active for a minimum of 75 ns.

3-90. The zone write upper and zone write lower signals control the operation of the memory on their bytes of the memory word. When a zone signal is low, the memory data register accepts input data for that byte and writes it into the selected memory address. When a zone signal is high, the memory data register reads data from that byte of the selected address and restores it back again. When both zone signals are low or both high, the memory performs a whole word write or whole word read, respectively. The zone write signals must hold their state for a minimum of 100 ns after the initiate signal becomes active.

3-91. The -data available signal informs the processor or DMA device that data has been read from the memory and is available for sampling on the memory output data lines. The signal is present on a memory output line between 300 and 400 ns after start of the read operation of both full and split cycles.

3-92. The +memory available signal is present on a memory output line except when the memory is processing a memory request. The signal informs the requesting device that the memory can be accessed. The signal is needed by the processor before it can initiate an operation and again before it can initiate the write portion of a split cycle operation.

3-93. Timing and Control Functional Description. The organization of one memory bank is shown in the bank block diagram, figure 3-20. The dotted lines on this diagram show the partitioning of the bank in terms of printed circuit boards, while the blocks inidicate the basic functional units. Each memory bank contains one control board, one data board, and from one to four array boards. The diagram shows only one of the array boards but does show the signals running to/from the other three array boards. Reference may also be made to figure 3-25, a detailed schematic diagram of one core stack and associated switch and diode circuits. The timing and control block of the bank diagram is further detailed in figure 3-21. The timing and control section receives control signals from the memory control interface and initiates internal timing and control signals required to execute a memory operation. The following paragraphs describe the functions of each block in the timing and control block diagram.

3-94. The busy control circuits consist essentially of two flip-flops which are set at the start of a memory operation and whose outputs enable all of the other timing and control section functions. The circuits remain active during all of a full cycle operation. During a split cycle operation, the circuits are active during the read portion, then become inactive, and are again activated at the start of the write cycle. When busy control is inactive, it enables the memory available signal to the requesting device (processor or DMA device).

3-95. The clock-oscillator circuit is activated by a signal from the busy control circuits at the start of a memory cycle and continues to operate until busy control goes inactive. Outputs of the circuit are nominal 30-nanosecond pulses used primarily to clock the timing chain. Figures 3-22 and 3-23 show the clock-oscillator and timing chain pulses. Figure 3-24 shows the clock-oscillator and timing chain circuits. Two clock signals are produced by the clock-oscillator, CLOCK 1 and CLOCK 2. CLOCK 1 is used to produce T1, T3, T5, T7, and T9 of the timing chain, while CLOCK 2 produces T2, T4, T6, and T8.

3-96. The timing chain consists of nine series connected, -edge-triggered flip-flops which are connected as a shift register. Outputs of the timing chain are timing pulses and pulse complements designated T1 through T9, each having a duration of about 190 nanoseconds. The pulses control the sequencing of the memory operations. The timing chain cycles through twice for each kind of memory operation. For a full cycle operation, the timing chain runs continuously until completion of the two timing cycles. For a split cycle, the timing chain cycles once to time the read part of the operation and then becomes inactive until the start of the write portion, at which time the timing cycle is restarted. Pulse T9 is shortened at the end of both timing cycles during a split cycle operation, and T7, T8, and T9 are shortened at the end of the full cycle operation. This occurs when busy control becomes inactive.

3-97. The general reset control initializes the memory control circuits during a power up and prevents accidental loss of memory data in the event of a power loss. Inputs to the control are +5 and +15 volt power, a power fault (-PF) signal from the processor, and a signal from busy control. Outputs are a master clear and enable

signals. During an initial power up or following loss of power, the reset control master clears (initializes) the memory timing and control circuits. When power reaches an operational level, the circuit outputs enable the bit selector, module write drivers, and module read enable drivers. The reset control also permits the memory to execute an orderly shut down sequence when a power failure occurs. Under such a condition, the control maintains its enable outputs until the operation is completed (full cycle) or until the timing chain cycle is completed (split cycle). Thus, in the case of a full cycle or the write part of a split cycle, the memory has time to write data into memory before complete power failure occurs.

3-98. The cycle control section consists of a single flip-flop which is always in the clear state at the start of a memory operation. The flip-flop is set at the start of an operation by the active +full cycle input control signal to specify a read/restore or clear/write operation. If the signal is inactive (-full cycle) at the start of an operation, then the flip-flop remains clear, specifying a read/modify/write operation. Outputs of the flip-flop enable the timing chain, enable the memory available signal following the read portion of a split cycle, and enable final initialization (clearing) of the busy control circuits.

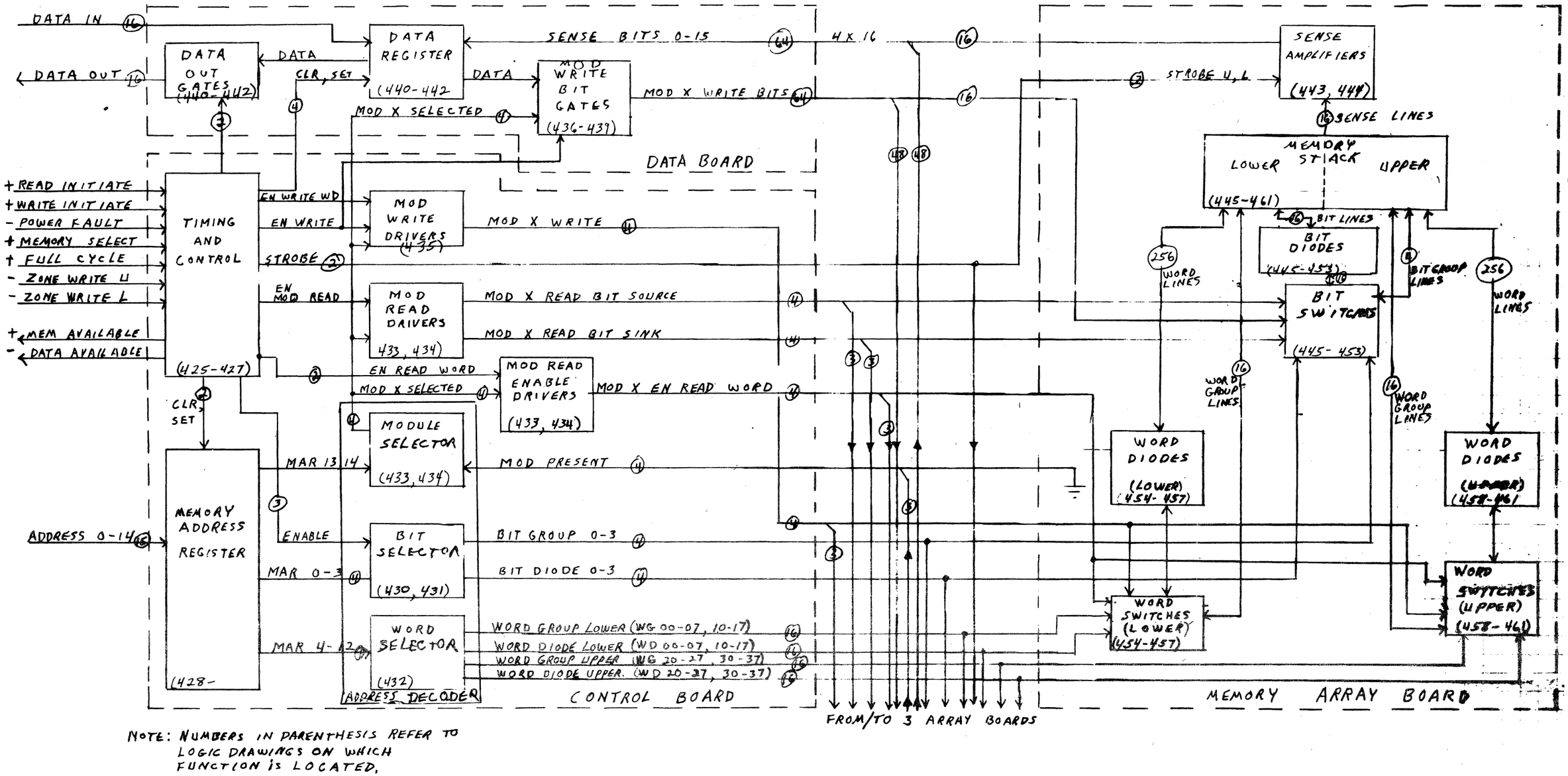
3-99. The read control section is comprised of two read flip-flops, whose outputs combine with other timing and control signals to provide sequencing of the read operation. The Read Initial flip-flop is always in the set state at the start of a memory read cycle, having been set either by a master clear, or by the T5 pulse in the previous memory operation. The flip-flop is cleared by the NOT T5 pulse at the end of the read cycle. The Read Final flip-flop is always in the clear state at the start of a memory read cycle. It is set at T3 time of the first timing cycle and is cleared at T3 time of the second timing cycle.

3-100. The write control section is comprised primarily of the Zone Write Upper and Zone Write Lower (ZW_U and ZW_L) flip-flops. They are set only at the start of a memory operation if the corresponding ZW_U or ZW_L control signal is received. The ZW_U flip-flop clears bits 8-15 of the data register and gates bits 8-15 from the input bus into the data register. ZW_L flip-flop effects the same actions for bits 0-7 of the data word. If a flip-flop is not set, the corresponding byte in the data register will retain the data received from the memory matrix during the read cycle, so the same byte data will be restored to its original matrix address.

3-101. Memory Address Register. The address register functions as an open latch for address bits 0-14 received from the memory input bus. Outputs of the register are continuously applied to the address decoder circuits.

3-102. Address Decoder. The address decoder receives the memory address from the address register and continuously translates the bits to select the address to be accessed. Fifteen address bits are required to select an address in one memory bank. The bits are decoded as shown in table 3-16. The address decoder contains three sub-functions which issue decode signals to select the memory address. They are the module selector, the word selector, and the bit selector.

3-103. The module selector decodes address bits 13 and 14 to select one of the four array boards (8K of memory). As stated in paragraph 3-85, one memory bank (32K) is selected by the memory select input signal. The module selector is enabled if the array board is present in the memory chassis. Outputs of the circuit go to the module read and write drivers and to the module write bit gates.



NOTE: NUMBERS IN PARENTHESIS REFER TO LOGIC DRAWINGS ON WHICH FUNCTION IS LOCATED.

Figure 3-20. Memory Bank Block Diagram

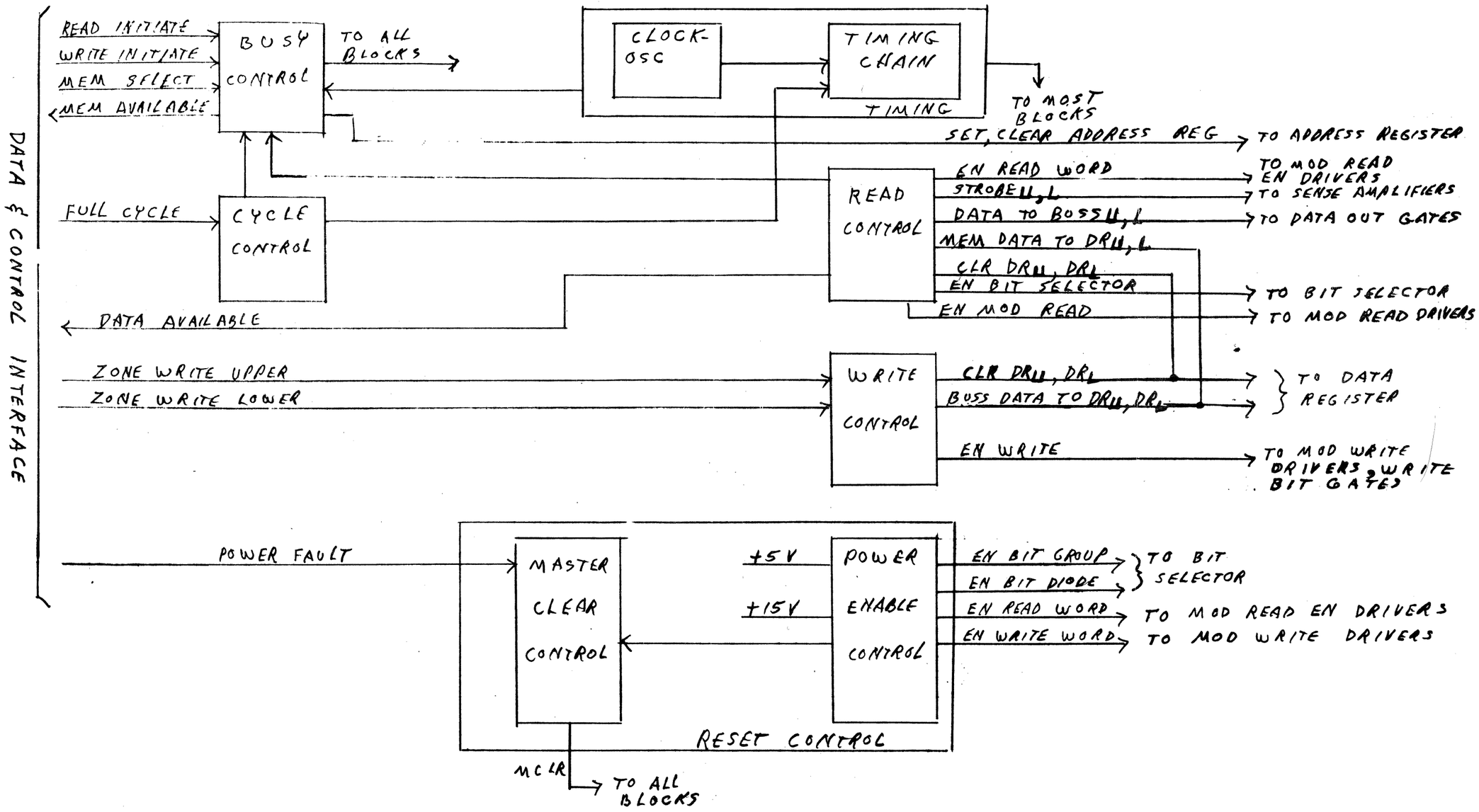


Figure 3-21. Timing and Control Block Diagram

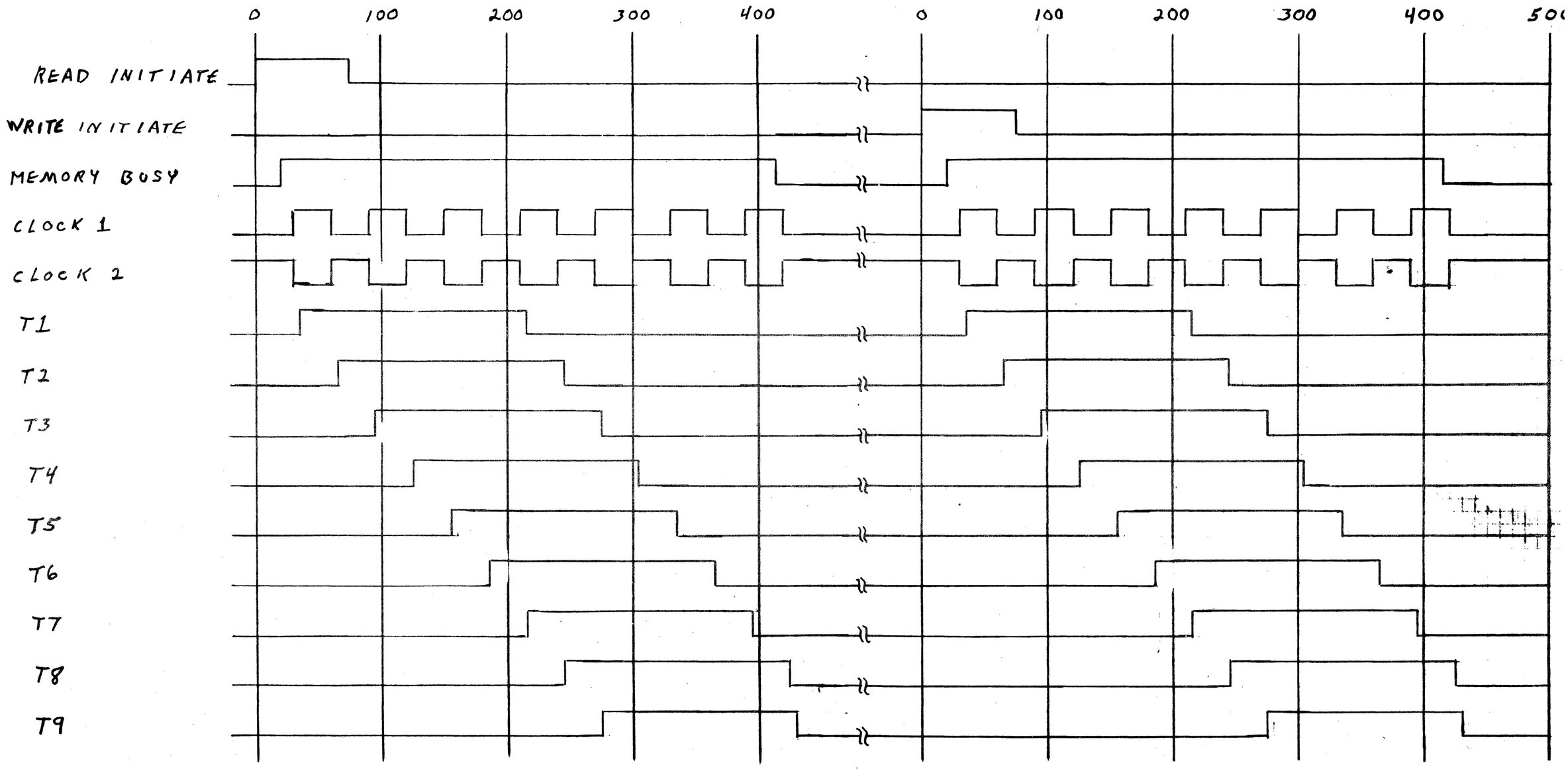


Figure 3-22. Split Cycle Timing

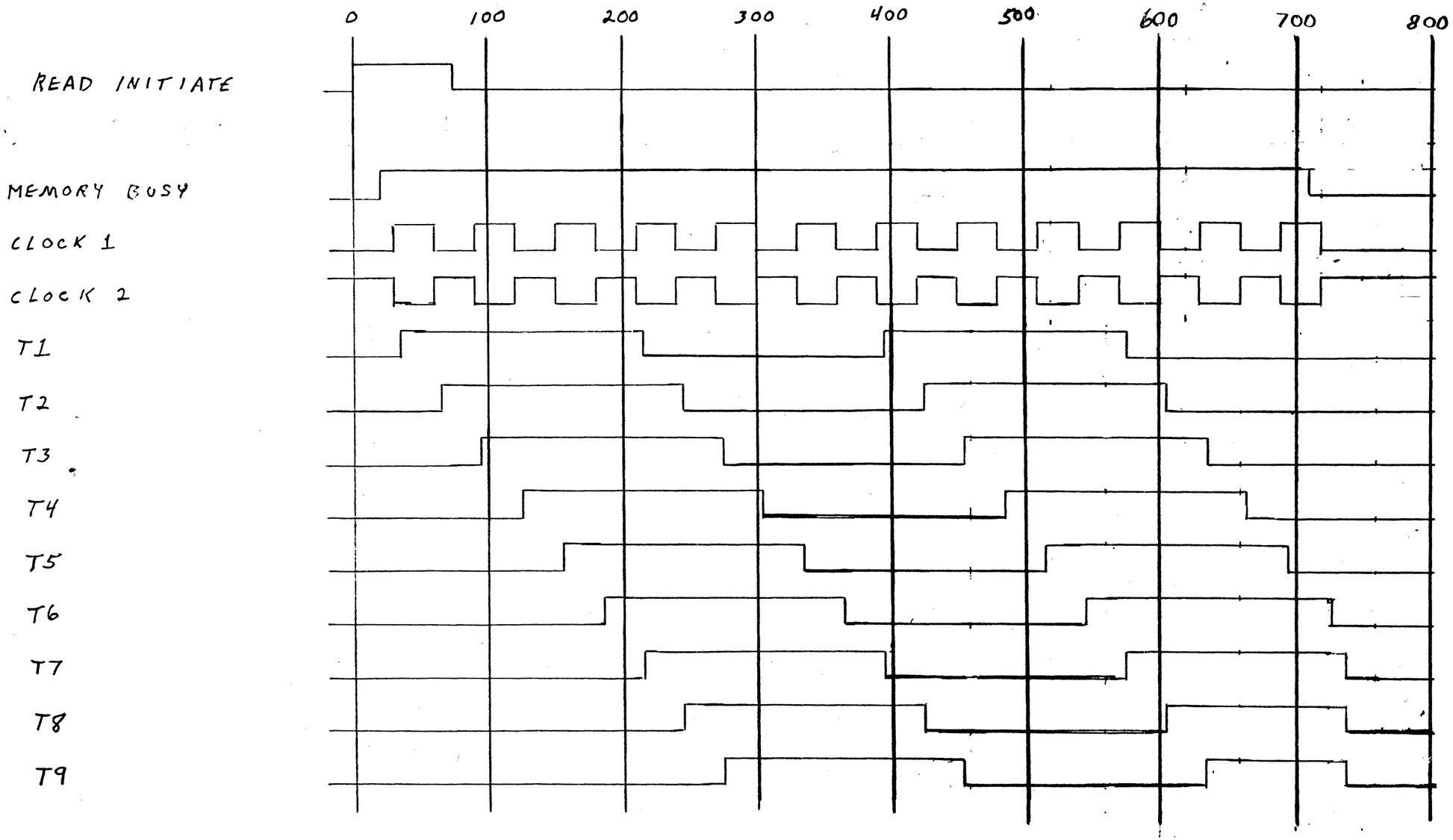


Figure 3-23. Full Cycle Timing

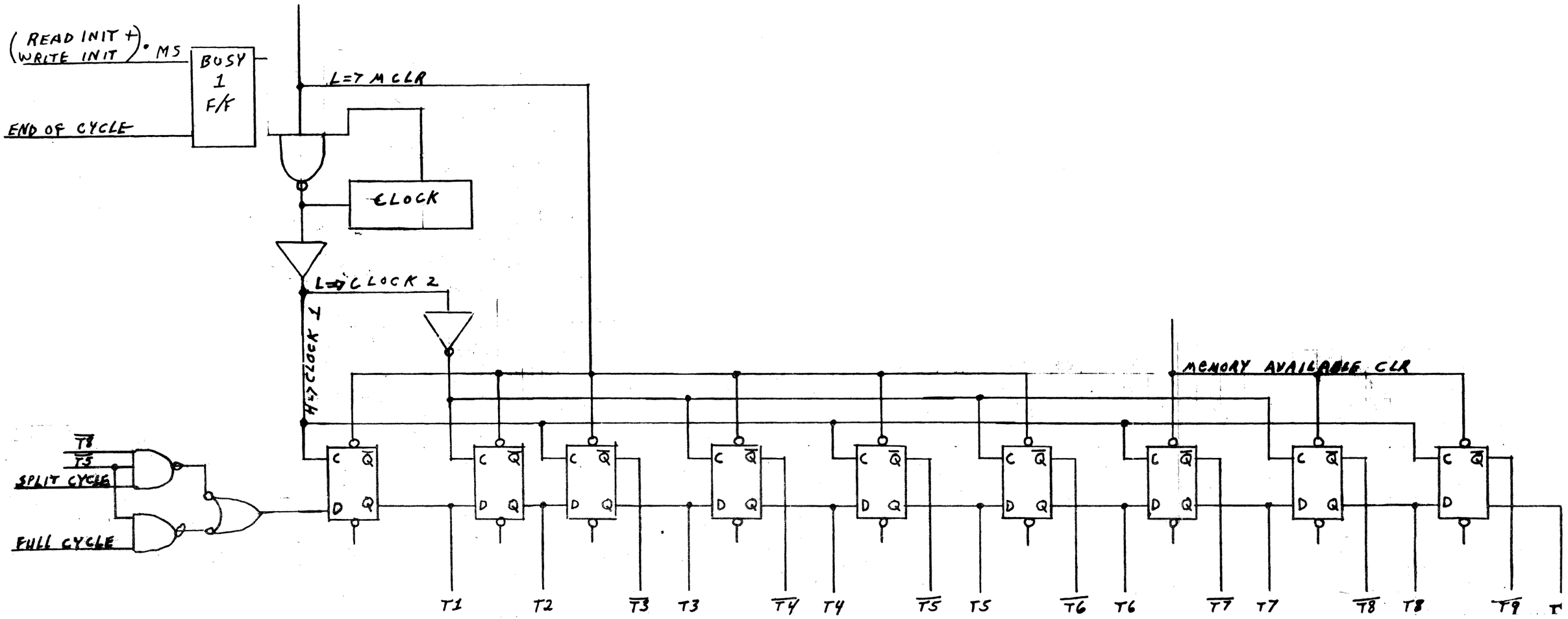


Figure 3-24. Memory Timing Circuits

Table 3-16. Address Bit Decode

ADDRESS BIT	SELECT
14, 13	Select one of four array boards in the memory bank.
12	Select one of two core stack sections on the selected array board.
11 - 8	Select one of 16 word drive lines in each of 16 word groups.
7 - 4	Select one of 16 word groups (bits 12 - 4 in combination select one word drive line in a core stack).
3, 2	Select one of 4 bit drive lines in each of 4 bit groups.
1, 0	Select one of 4 bit groups (bits 3 - 0 in combination select one bit drive line in a core stack).

3-104. The word selector translates bits 4 through 12 to select one word drive line in a core matrix. Bit 12 selects one of the two core array sections (upper or lower) on an array board, thus selecting 4K of memory. Bits 8 through 11 select one of 16 word drive lines in each of 16 word groups, thus narrowing the possible addresses to 256. Bits 4 through 7 are decoded to select one word group out of a possible 16 groups, thereby narrowing the possible addresses to 16. Outputs of the word selector are word diode and word group signals which are continuously applied to the word switch gates on the array board.

3-105. The bit selector decodes bits 2 and 3 of the address register to select one bit drive line in each of four bit groups, thus decreasing the possible memory selection to four addresses. Bits 0 and 1 are decoded to select one bit group from among four groups. At this point the address bits have selected one address in the memory bank. Outputs of the bit selector are bit group and bit diode signals which are continuously applied to the bit switch gates on the array board, except for a period of about 70 nanoseconds at the end of a memory operation.

3-106. Module Read Drivers. The module read drivers consist of four sets of drive gates, one set for each array board. A gate is enabled between the 25 and 365 nanosecond times of a read cycle when the array board has been selected for access by the module selector. Outputs of the gates are module read bit source and read bit sink signals which gate the bit selector decode (bits 0 - 3) to the bit switches, thereby causing read current to flow in the selected bit drive line of each mat in the core array.

3-107. Module Read Enable Drivers. The module read enable drivers consist of four sets of drive gates, one set for each array board. A gate is enabled at T3 time of a read cycle and remains enabled until 365 nanoseconds after zero time of the read cycle. Outputs of the gates are module read enable signals which gate the word selector decode (bits 4 - 12) to the word switches, thereby causing read current to flow in the selected word drive line of the selected core array.

3-108. Module Write Drivers. The module write drivers consist of four sets of drive gates, one set for each array board. The gates are enabled at T2 time of a write cycle if the module has been selected by the module selector, and remain enabled until the end of T4 time of the write cycle. Outputs of the gates are module WRITE signals which gate the address decode to the word write switches during a write operation, thereby causing write current to flow in the selected word drive line.

3-109. Data Register. The memory data register, physically located on the data board, acts as an open latch to hold data received from memory addresses via the sense amplifiers or data received on the memory input lines from the processor or DMA device. The register is cleared at the beginning of the read cycle, and again at the start of the write portion of a split cycle, depending on the setting of the zone write control signals (paragraph 3-90). During a read cycle, data from the sense amplifiers is loaded into the register by the strobe signals, which are active from approximately 295 to 415 time of the read cycle. During a write cycle, data received on the input bus lines is gated into the register by the data to DR signal, which occurs between times 45 and 160 of the write cycle. Data loaded into the register from the input bus may be a complete 16-bit word or an 8-bit byte, as determined by the setting of the zone write flip-flops. Data register outputs go to the data out gates and to the module write bit gates.

3-110. The data out gates enable the data register outputs to the memory output data lines. The data is gated out by the data to bus signals, which occur during T9 time of a read cycle. The module write bit gates consist of four sets of gates, one for each array board in the memory bank. Each set of gates contains 16 gates, one for each bit in the data word. Inputs to the gates are from the data register, and they are gated by the EN WRITE signal which occurs during times T2 and T4 of the write cycle. Outputs of the gates are write bit (0 - 15) signals. The signals are applied to the bit write switch gates, thereby gating in the bit selector decode and causing write current to flow in the selected bit drive line.

3-111. Word/Bit Switches and Diodes. The word and bit switches consist of gating circuits and transistors which "switch" on to cause current to flow in matrix drive lines. Inputs to the switches are address decode signals and internal read or write control signals. A set of the switches is located at each end of the word and bit drive lines, and current flows when the switches at both ends of a line are switched on. See figure 3-25 for switch detail. Two sets of diodes are located at one end of both the word- and bit-matrix drive lines. The sets of diodes are of opposite polarity, one set permitting current to flow in one direction for a read operation, the other set permitting current to flow in the opposite direction for a write operation. The diodes connect on one end to the transistors in the switches; on the other end they connect to the matrix drive lines.

3-112. Memory Stack. Each memory array board holds an 8K array stack, electrically divided into two sections designated as upper and lower. Each stack contains 16 core-mats. A mat holds one bit, for example bit 1, of each of the 8192 (512 X 16) addresses in the stack. A mat is constructed with 512 cores along one axis (word axis) and 16 cores on the other (bit axis). A word drive line runs through all of the 16 cores in one group column of one stack, and a bit drive line runs through all of the 512 cores in one bit row of the stack. A core is read, or written into, when word current and bit current flow through the core at the same time. These "coincident" currents flow in one direction for a read operation and in the opposite direction for a write operation. When a "1" is written into a core, the state of the core is changed from one magnetized state (designated the "0" state) to the opposite

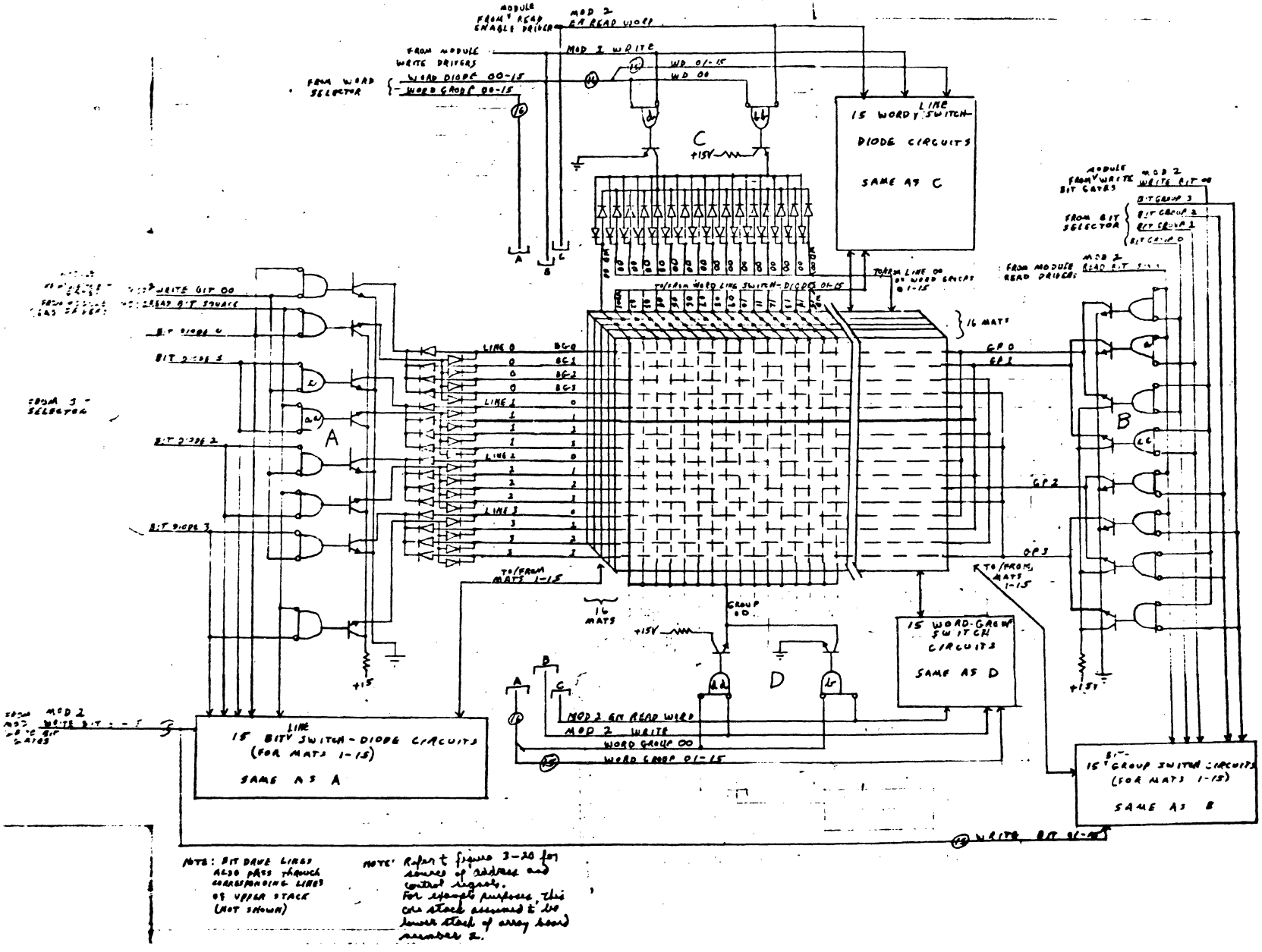


Figure 3-25. Memory Array Board

magnetized state (designated the "1" state). During a read operation, the coincident currents return the core to the "0" magnetized state. The change of flux in the core as the magnetized state switches, induces current in a third line, the sense line, which runs through each core in the mat. The flow of current in the sense line signifies that the core contained a "1". If the core contained a "0", it would not have been changed, and no current would be induced in the sense line. The read operation leaves all cores of an addressed word in the "0" state. During the subsequent write portion of an operation, bit write enables are developed by the mod write bit gates only for those bits of the data register that contain ones, thus permitting write current to flow only through those bit lines where ones are to be written. Therefore, a core is left in the "0" state if a zero is being written in, and is magnetized to the "1" state if a one is being written in.

3-113. Sense Amplifiers. The sense amplifiers detect current on the sense lines during a read operation and amplify it. The sense amplifier outputs are gated to the data register by the STROBE signals, which occur between times 295 and 415 of the read cycle.

3-114. Array Board Circuit Operation. The following paragraphs describe the operation of the memory array board circuits with reference to a specific memory address. Figure 3-25 is a detailed drawing of an array board, which shows the gating and transistor circuits of the memory switches, the diodes, and memory core array for the lower half of a stack. Figure 3-26 is a simplified drawing which shows read and write circuits in relation to one core. Assume that the memory address to be selected is address 5 on array board 2. The format of the address bits would therefore be:

Address Bits:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit State:	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1

With this format, bits 14 and 13 select array board 2; bit 12 selects the lower section of the array stack on board 2; bits 11 through 8 select word line (WD) 00 in each of 16 word groups, and bits 7 through 4 select word group (WG) 00. Bits 3 and 2 select bit line (BD) 01 in each of four bit groups, and bits 1 and 0 select bit group (BG) 01. The heavy lines passing through the core matrix on figure 3-25 are selected by address 5.

3-115. During a read operation, gates lettered "a" on the right and "aa" on the left side of figure 3-25 and gates lettered "b" and "bb" on the top and bottom are selected by the address bit decode. At read time these gates are enabled by the read control signals, causing the outputs of the gates to go high and forward biasing the read transistors. The transistors are now switched on, causing coincident current to flow through the addressed cores. Current flows from ground on the right side of figure 3-25, through transistor "a" to line 1 of the Group 1 lines, through the core and read diode, and through transistor "aa" and a resistor to +15 volts. Current through the word drive line flows from ground on the bottom of the figure through transistor "b" to the line 0 of the Group 1 drive lines, through the core and read diode, and through transistor "bb" and a resistor to +15 volts.

3-116. During a write operation, bit gates lettered "c" and "cc" and word gates lettered "d" and "dd" are selected by the address decode. At write time, the "c" gates are enabled by WRITE BIT 00 and the "d" gates by the MOD 2 WRITE signal, causing the corresponding transistors to switch on. Again current flows from ground

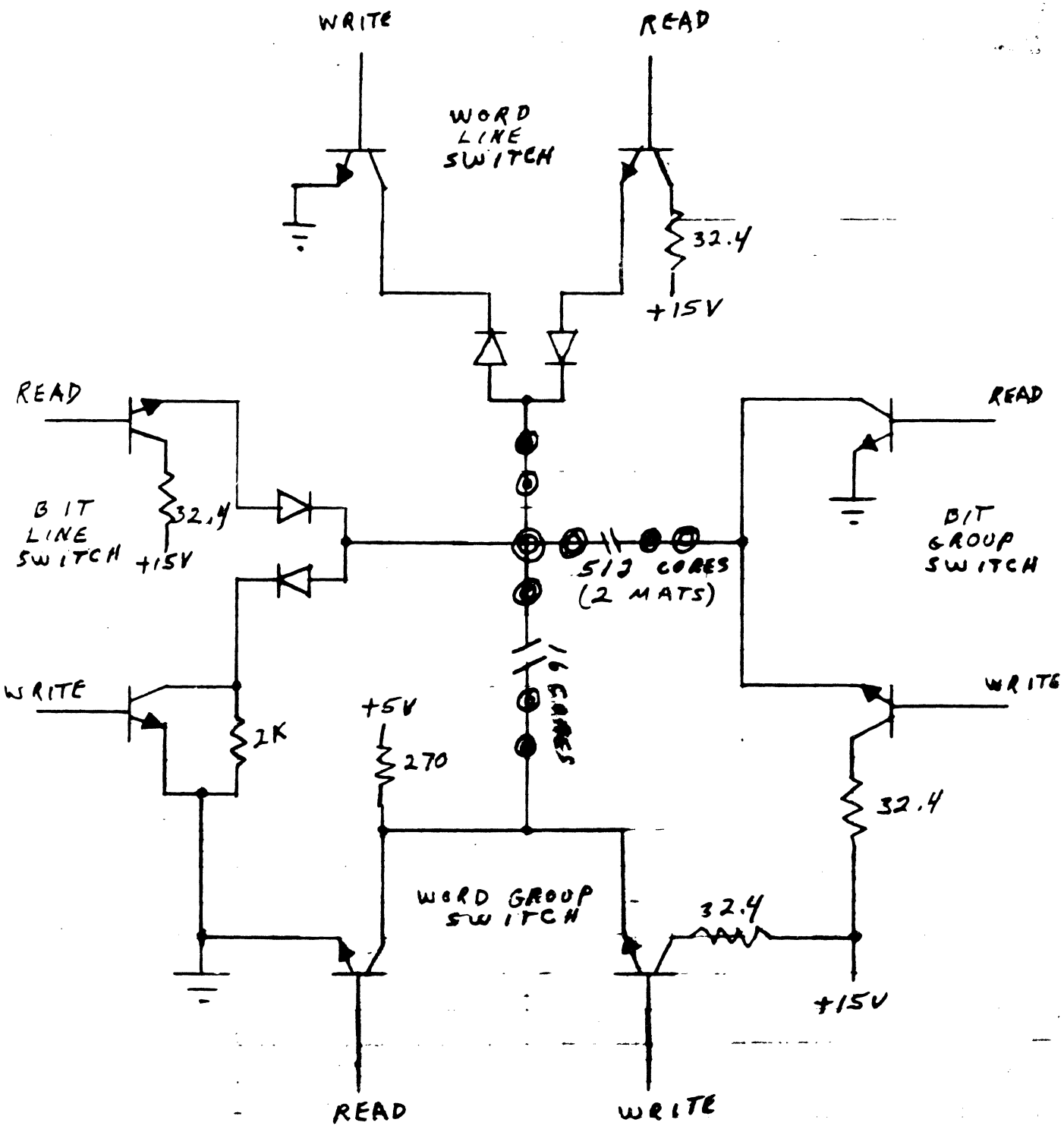


Figure 3-26. Memory Core Drive Circuits

on one side to +15V on the opposite side of the matrix; however, the direction of current flow is opposite to that in a read operation.

3-117. Full Cycle Operation. The full cycle read/restore operation is used to read information from a given memory address and then restore the same information back into the address. Data is first read out from the cores into the data register. It is then sent to the data output lines, completing the read portion of the operation. In the second part of the operation, the same data is stored back into its original location. Table 3-17 shows the sequence of events for the read/restore operation. Data from the desired address location is read out during steps 1 through 10 and restored during steps 11 through 13; figure 3-27 shows the timing relationship for the Read/Restore. The full cycle clear/write operation is identical to the read/restore except that the zone write signals are low, disabling the sense amplifier strobe, and gating processor data into the data register for writing into the cores. For a byte write operation, only one zone write signal is low, causing a clear/write operation for that byte and a read/restore operation for the other.

3-118. Split Cycle Operation. The split cycle read/modify/write operation is used to read a word from memory and then to restore a modified word in its place. During the first part of the cycle, data is read out from the specified address location into the data register. It is then sent to the data output lines, completing the read portion of the operation. During the second portion of the split cycle, modified data is accepted from the data in lines and subsequently stored in the initial address location, thus completing the operation. Table 3-18 shows the sequence of events for the read/modify/write operation. Data from the desired address location is read out during steps 1 through 11. Data is stored during steps 12 through 18. Figure 3-28 shows the timing relationships for the read/modify/write.

Table 3-17. Read/Restore Sequence of Events

STEP	ACTION
1	The cycle is initiated by +Read Initiate = 1, which defines zero time. In addition, the following conditions must be met: +Write Initiate = 0 +Full Cycle = 1 -Zone Write Upper and Zone Write Lower = 0 (+) +Memory Select Address Input stable +Read Initiate must remain true for 75 ns minimum; the remaining signal conditions must remain in the correct state for 100 ns minimum.
2	Output signal +MEMORY AVAILABLE goes false 30 ns after the start of the cycle, indicating a cycle in progress, and blocking further instructions until the operation is completed. It remains low until 740 ns after zero time.
3	Data register is reset by CLEAR DR_U and CLEAR DR_L signals.

Table 3-17. Read/Restore Sequence of Events (Cont)

STEP	ACTION
4	Address information is checked into the address register by the +SET ADD REG signal.
5	-BIT DIODE and -BIT GROUP signals are sent to both core matrices on all array boards to select one bit drive line on all matrices.
6	-WORD DIODE and -WORD GROUP signals are sent to one half of the core matrix on each array board to select one word drive line on each matrix.
7	-MOD READ BIT SINK and -MOD READ BIT SOURCE signals are sent to the core matrix on the selected array board to enable the bit switches, resulting in the generation of drive current in one bit drive line on one array board.
8	-MOD EN READ WORD signal is sent to the selected array board to enable the word line switches, resulting in the generation of drive current in one word drive line in the core matrix on one array board. Core turnover takes place at the cores which receive coincident bit drive and word drive currents. The signals reach the sense amplifiers.
9	Timing signals $STROBE_U$ and $STROBE_L$ are sent to the sense amplifiers, resulting in sense amplifier output, which sets the data register in accordance with the data read from memory.
10	Output signal -DA goes low at data available time and remains in that state for 100 ns, indicating that the requested information is now available and stable on the data output lines. These lines retain the data read out of memory until the $READ_f$ signal goes low in the restore portion of the operation.
11	Timing signal -EN WRITE is sent to the data register outputs to gate the data bits to the bit switch gating circuits of the selected array board, resulting in bit write current through the cores for those data bits containing a "1".
12	-EN WRITE is sent to the word line switches of the selected array board, resulting in the generation of word write current in one word drive line in the core matrix on one array board. Core turnover takes place at the cores which receive coincident bit write and word write currents, thus replacing the original contents of the initial address back into the same address.
13	Output signal +MA goes true at 740 ns, indicating that a new operation may be initiated. At approximately the same time, all memory internal circuits are returned to their initial condition in preparation for reception of a new memory initiate.

Table 3-18. Read/Modify/Write Sequence of Events

STEP	ACTION
1	The read portion of the cycle is initiated by +Read Initiate = 1, which defines zero time. In addition, the following conditions must be met: +Write Initiate = 0 +Full Cycle = 0 -Zone Write Upper and Zone Write Lower = 0(+) +Memory Select Address Input stable +Read Initiate must remain true for 75 ns minimum; the remaining signal conditions must remain in the correct state for 100 ns minimum.
2	Output signal +MEMORY AVAILABLE goes false 145 ns after the start of the cycle, indicating a cycle in progress, and blocking further instructions until the read portion of the operation is completed. It remains low until 440 ns after zero time.
3	Data register is reset by CLEAR DR_U and CLEAR DR_L signals.
4	Address information is clocked into the address register by the +SET ADD REG signal.
5	Decoded outputs of the address register (BIT DIODE-BIT GROUP and WORD DIODE-WORD GROUP) are sent to the memory core matrices to select the memory address.
6	-MOD READ BIT SINK and -MOD READ BIT SOURCE are sent to the selected matrix, resulting in the generation of drive current in one bit drive line in the matrix on one array board.
7	-MOD EN READ WORD signal is sent to the selected matrix, resulting in the generation of drive current in one word drive line of the matrix. Core turnover takes place at the cores which receive coincident bit drive and word drive currents. The signals reach the sense amplifiers.
8	Timing signals $STROBE_U$ and $STROBE_L$ are sent to the sense amplifiers, resulting in sense amplifier output, which sets the data register in accordance with the data read from memory.
9	Output signal -DA goes low at data available time and remains in that state for 100 ns, indicating that the requested information is now available and stable on the data output lines. These lines retain the data read out of memory until the start of the write portion of the operation.

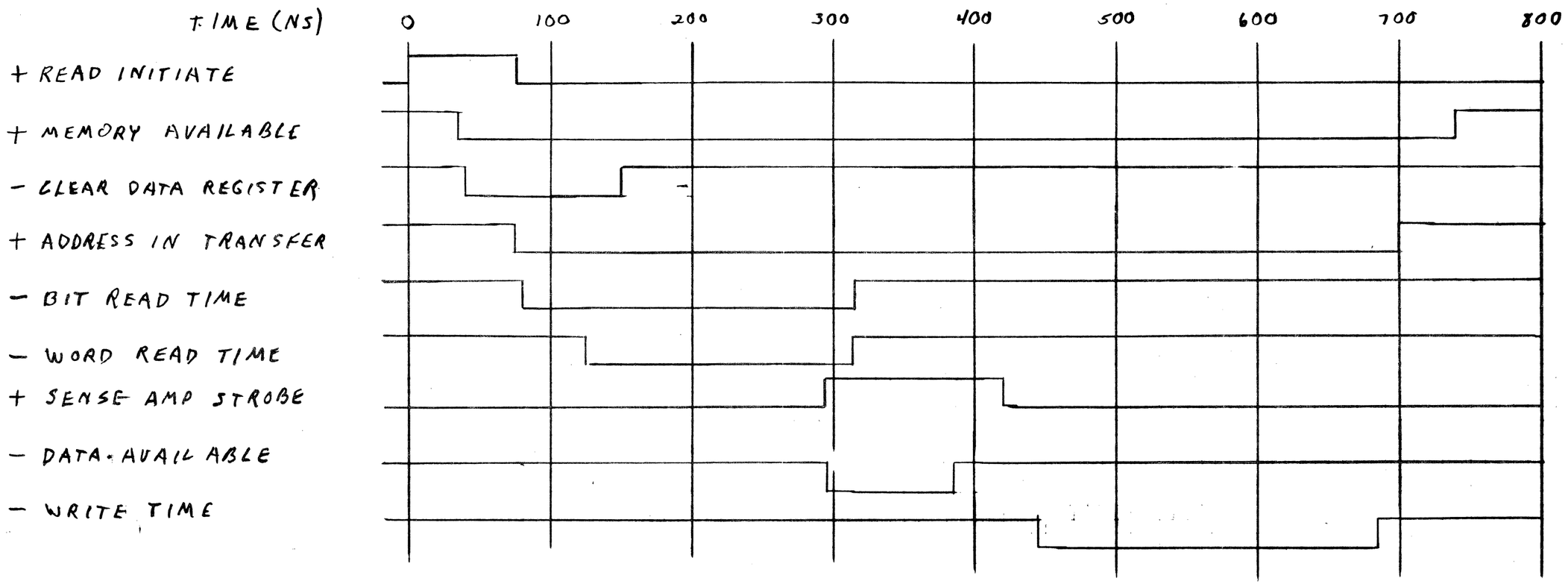


Figure 3-27. Internal Timing - Read/Restore

Table 3-18. Read/Modify/Write Sequence of Events (Cont)

STEP	ACTION
10	+READ INITIATE must be returned to the false (0) state before the end of the read portion of the operation.
11	Output signal +MEMORY AVAILABLE goes true 440 ns after zero time, thus informing the processor that the read portion of the operation has been completed.
12	The write portion of the operation is initiated by Write Initiate = 1 which may not go true earlier than 475 ns after start of the read portion. In addition, the following conditions must be met: +Read Initiate = 0 +Full Cycle = 0 -Zone Write Upper and Zone Write Lower = 1 (low) +Memory Select Data Input must be stable at Write Initiate and remain stable for 150 ns minimum. +Write Initiate must remain true for 75 ns minimum. The remaining signal conditions must remain in the correct state for 100 ns minimum after the leading edge of +Write Initiate.
13	Output signal +MEMORY AVAILABLE goes false, and the command inputs are blocked so as not to accept further instructions.
14	Data register is cleared.
15	Processor data is clocked into the data register. Input data must be stable at this time and must remain so for 100 ns minimum thereafter.
16	Timing signal -EN WRITE is sent to the data register outputs to gate the data bits to the bit switch gating circuits of the selected array board, resulting in bit write current through the cores for those data bits containing a "1".
17	-EN WRITE is sent to the word line switches of the selected array board, resulting in the generation of word write current in one word drive line in the core matrix on one array board. Core turnover takes place at the cores which receive coincident bit write and word write currents, thus storing a one in those cores.
18	Output signal +MA goes true at 440 ns of the write cycle, indicating that a new operation may be initiated. At approximately the same time, all memory internal circuits are returned to their initial condition in preparation for reception of a new memory access instruction.

3-119. INPUT/OUTPUT CONTROLLER (IOC). The IOC provides for communication between the DPS and peripheral equipment or between the DPS and another computer. The IOC may contain up to sixteen 16-bit channels. The channel numbers are assigned octally ($0\text{-}17_8$), but are sometimes referred to decimally ($0\text{-}15_{10}$). An IOC may have all parallel channels or all serial channels or a combination of parallel and serial channels. Parallel channels occur in groups of four, and the four channels within a group must have the same interface level. Available interface levels are NTDS Slow (-15V), NTDS Fast (-3V), and ANEW (+3.5V). Serial channels occur in groups of two, and both channels in the group must be of the same type. The available types are expanded MIL-STD-188 synchronous or asynchronous, RS-232 standard synchronous or asynchronous, and NTDS 32-bit asynchronous. All channels are full duplex, permitting input and output transmissions to occur simultaneously. Normal I/O communication is in the word mode (16-bit); however, communication is also possible in the byte mode (8-bit) or in the dual channel mode (32-bit double length word). Dual channel operation with parallel channels requires a channel from each of two adjacent groups (channels n, n+4). Dual channel operation with serial channels uses the pair of channels in a two-channel group. Intercomputer communication is possible with parallel channels. On intercomputer operation, the transmitting computer holds the data available on the output data lines to the receiving computer until either the receiving computer sets the Resume line or the transmitting computer program proceeds because of the intercomputer timeout (256 to 512 milliseconds). All I/O options are plug-in options, but when adding extra modes of operation (Dual channel, ESA, or Intercomputer) the I/O mode selection card must be wired to include the extra option. Refer to Chapter 6. When changing from parallel to serial I/O where a coaxial cable is required, a 120-pin adapter plug with a coaxial connector is needed. Communication mode changes may require a differently wired connector. Figure 3-29 provides a functional block diagram of the IOC. The following paragraphs present a functional description based on the block diagram.

3-120. Request/Acknowledge Control. The request receivers pick up any requests the peripherals may generate and send the requests to the I/O request oneshots. Each channel has four request receivers, one for Output Data Request (ODR), Input Data Request (IDR), External Function Request (EFR), and External Interrupt (EI). The I/O request oneshots control the requests for each channel. The oneshots insure a request is acknowledged before another similar request is allowed in from the channel. Each channel has four oneshot circuits, one each for ODR, IDR, EFR and EI. The oneshots for each channel are included along with other control circuits for that channel on a single IC device, described in figure . (See also figure 9-362.) The acknowledge circuitry generates an acknowledge signal to the peripheral generating the request.

3-121. Group/Channel Control. The priority scan and priority circuits control both channel priority and function priority. I/O operations are handled according to channel priority first and function priority second. Channels are designated 17_8 (15_{10}) through 0, with channel 17_8 having highest priority. Function priority is determined as each channel is scanned. The highest function priority is external interrupt, output buffer (external function or output data) is second, and input buffer (external function or input data) or chaining have the lowest function priority. Function priority translation for the -15V interface appears on logic schematic figures 9-357 and 9-363. Circuits shown on figures 9-203 and 9-204 gate it according to channel translation and absorb it into the overall priority translation. Table 3-19 shows the functions of the I/O control chip (figure and 9-362) relative to the function bits. On input data function the priority circuit enables the input channel selection of the input receivers. I/OC related operations are performed on a higher

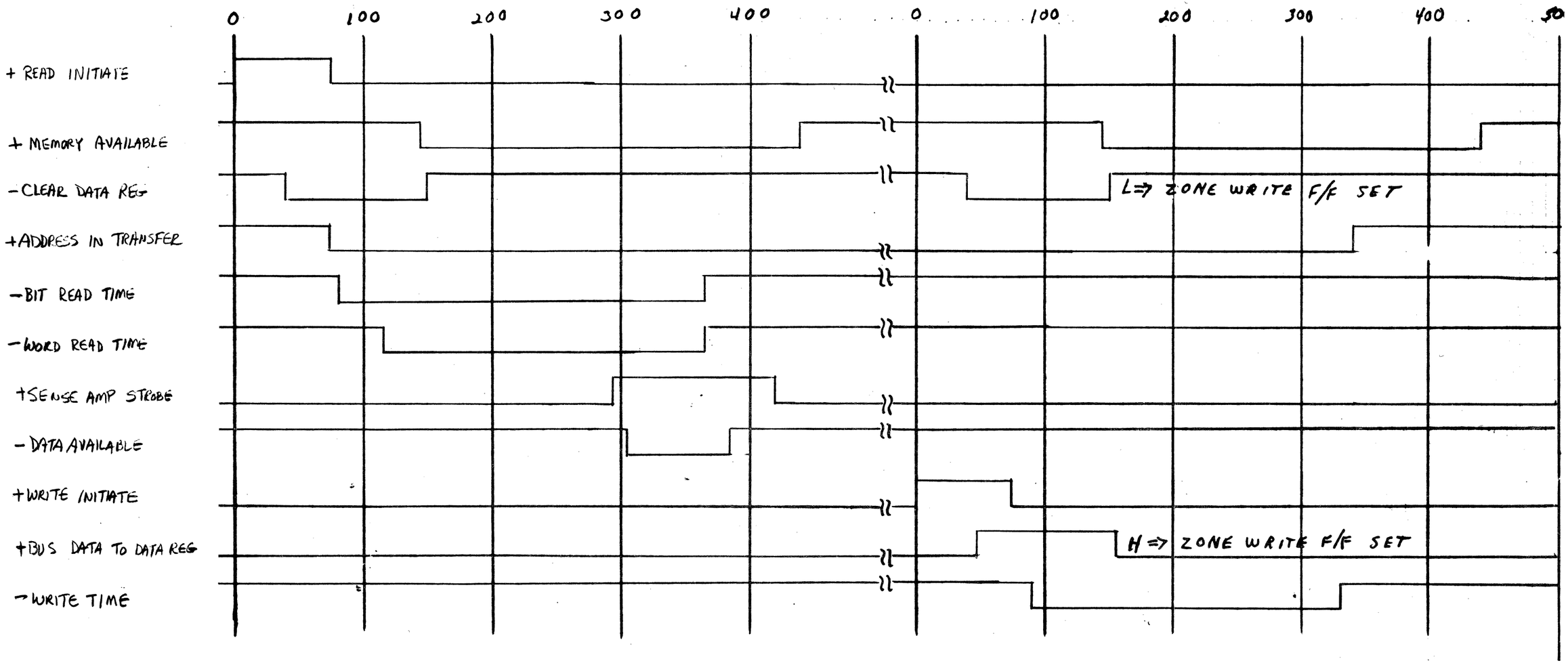


Figure 3-28. Internal Timing - Read/Modify/Write

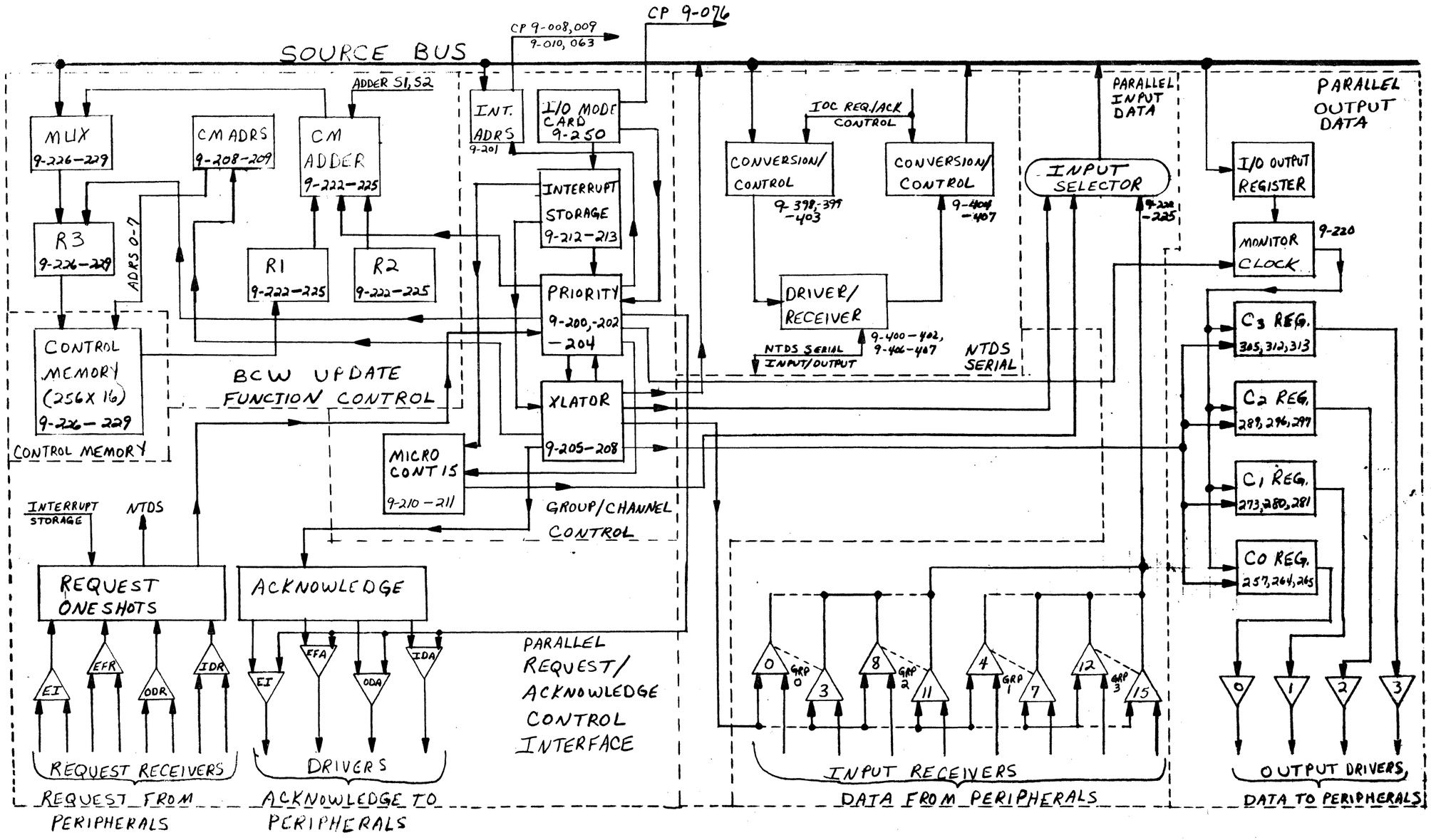


Figure 3-29. IOC Functional Block Diagram

Table 3-19. I/O Control Chip Function Relative to Function Bits

FUNCTION BITS f_1	FUNCTION BITS f_0	FUNCTION
0	0	Input Data (ID) SET/CLR MONITOR (MON) = IN CHAIN SET/CLR ACTIVE (ACT) = IN DATA SET FORCE = FORCE EF/ID SET ACT II = EF DATA/ID CLR ONE SHOT (O.S.) = CLR O.S.
0	1	Output Data (OD) SET/CLR MON = OUT CHAIN SET/CLR ACT = OUT DATA SET FORCE = FORCE EF/OD SET ACT II = EF DATA/OD CLR O.S. = CLR O.S.
1	0	External Interrupt (EI) SET/CLR MON = INT CP SET/CLR ACT = EI DATA CLR O.S. = CLR O.S.
1	1	External Function (EF) SET/CLR MON = INT ENABLE (EN) SET/CLR ACT = CHAIN EN CLR O.S. = CLR O.S.

priority by the MPC than central processor operations. The group/channel translator circuit is controlled by the macro instruction register and enables the required group and channel. After a channel has been activated for a specific function, the translator generates a signal to clear the oneshot for that function and enables an acknowledge via the acknowledge drivers to the peripheral generating the request.

3-122. Input Data. The input parallel receivers accept data from peripherals and pass it to the input selector. There are 16 input receivers per channel, one for each data bit (0-15). When the input receivers are enabled by the Input Channel Select, data from the channel can then pass to the input selector. The input selector gates the receiver inputs to the source bus. The NTDS, RS-232, and MIL-STD-188 serial channels accept data from peripherals, convert it and send it to the source bus via input registers.

3-123. Output Data. The 16-bit C registers hold parallel output data for the channels of their group. The group select lines enable data from the I/O output register to the monitor clock register (figure 9-220) into the C registers. This data is available to the peripherals via output drivers until new data is gated into the registers. The C register contents may be displayed for troubleshooting. The NTDS serial channel converts the data from the source bus and sends it to the peripheral. The RS-232 and MIL-STD-188 output registers accept data from the source bus, the data is converted, and sent to the peripheral.

3-124. I/O Control Memory. Each I/O channel has a control memory with sixteen 16-bit locations for storing and updating of input and output buffer control words (BCW) and chain address pointers. Parallel channels use only six of the sixteen locations; serial channels use an additional three. Figure 3-30 shows the control memory address assignments. Figure 3-31 illustrates the serial control word format. Table 3-20 defines the I/O buffer control word bit assignments.

3-125. Function Control. The 16-bit R1 register holds data for the I/O control memory adder and the I/O Mux. When R1 is enabled, data from control memory is loaded into it. The 16-bit R2 register provides a second input for the I/O CM adder. The R2 register contains predetermined values used by the adder for updating the buffer control words and address pointers. Refer to table 3-21. The 16-bit R3 register places data on the I/O control memory input lines. This data remains on the lines until new data is presented to the register. The I/O Mux provides the input to register R3. One of two inputs can be selected: either the source bus or the output from the I/O control memory adder. The I/O control memory adder is a 16-bit adder which is used to decrement buffer word counts and increment address pointers. The adder receives inputs from registers R1 and R2, and transmits an output to the I/O Mux. The I/O control memory address register provides address selection for the I/O control memory. The address register receives priority inputs 1-7 from the priority circuitry and address drive from the drive circuitry (figures 9-208 and 9-209).

3-126. I/O Operation. I/O activity is first initiated by the I/O Command macroinstruction (Op Code 35, RR). Subsequent I/O operations are controlled by buffer control words obtained from main memory and stored in locations 0 and 1 (input) or 4 and 5 (output) of the I/O control memory for that channel. The control memory adder updates the control words at each I/O operation, decrementing the buffer word count and incrementing the chain address pointer. Parallel input data from the peripheral is received by the input receivers and sent to the source bus via the input selector. Data to be output to the peripherals is received from the source bus and is gated to the correct C register for output by the group select signal

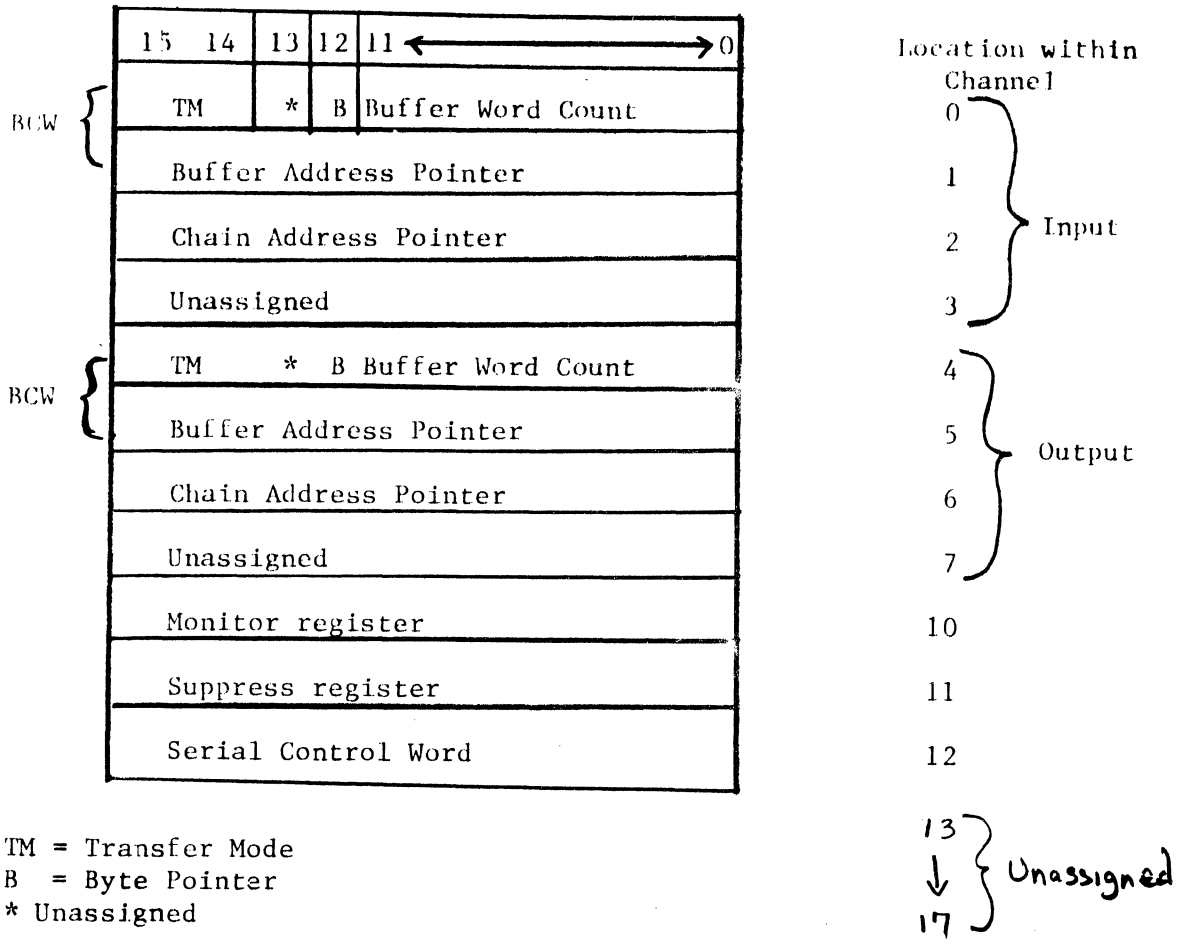


Figure 3-30. I/O Control Memory Format

from the group/channel translator. Tables 3-22 through 3-24 illustrate the relationship of IOC activity to the microinstructions being processed in the MPC. Input and output data transfers use a request/acknowledge system. On input operations the peripheral unit generates a request. When the IOC has granted priority, it accepts the data and acknowledges it, so the peripheral unit can continue the sequence. On output operations, the IOC generates the request to the peripheral device and must receive an acknowledge before it can continue activity in that channel. The two types of I/O instructions are listed below:

1) I/O Command: The Processor/Emulator initiates I/O operation by setting the I/O command request line. This is done whenever the processor executes an I/O command instruction (an operation code of 35 and an RR format). The first instruction executed by the I/O will be a command instruction stored at memory address 000140 (and 000141, if double length). Memory storage locations for command instructions are referred to as the command cell. Subsequent I/O operations during input data, output data, or external function transfers are controlled by buffer control words obtained from main memory and stored in locations 0 and 1 of the I/O control memory assigned to that channel.

2) I/O Chaining: Chaining permits the I/O to operate as an independent programmable device, able to execute a set of consecutive instructions stored in main memory. This has the effect of improving efficiency, since it does not have to interrupt processing operations to devote time to I/O control. Basically, chaining is accomplished by allocating a number of main memory locations to a series of I/O instructions, and directing the I/O, via a single command, to read and perform the series of instructions. Chaining means that the operations for a channel are controlled by a program addressed by the contents of the chain address pointer CM location. Whenever the I/O executes an initiate chain command instruction, chaining is enabled for the selected channel. Chaining operations continue in accordance with the sequential program stored in memory. An address in location 2 (input) or 6 (output) of the internal control memory for each channel, designated the chain address pointer, specifies the address of the next chaining instruction to be executed for that channel. When a chaining instruction is obtained from memory, the I/O increments the contents of the chain address pointer by one if the instruction is single length, and by two if it is double length. When the I/O completes the operations required for the current chaining instruction, it obtains the next instruction thereby keeping the channel active. Chaining continues until halted by program control (instruction 73, RR, a = 0 or 70, RR, a = 0, 10). Continuous looping is possible, permitting updating of input/output buffers to reflect current data.

3-127. Parallel I/O interface. Figure 2-32 and table 3-25 illustrate and define the parallel output interface and signal lines. Figure 3-33 and table 3-26 illustrate and define the parallel input interface and signal lines. The parallel I/O interface may be the NTDS Slow (-15V), the NTDS Fast (-3V), or the ANEW (+3.5V) type. Table 1-1 specifies the maximum transfer rates (words per second) of each type of interface. The interface contains both control and data lines. The following paragraphs describe the characteristics of each parallel interface type.

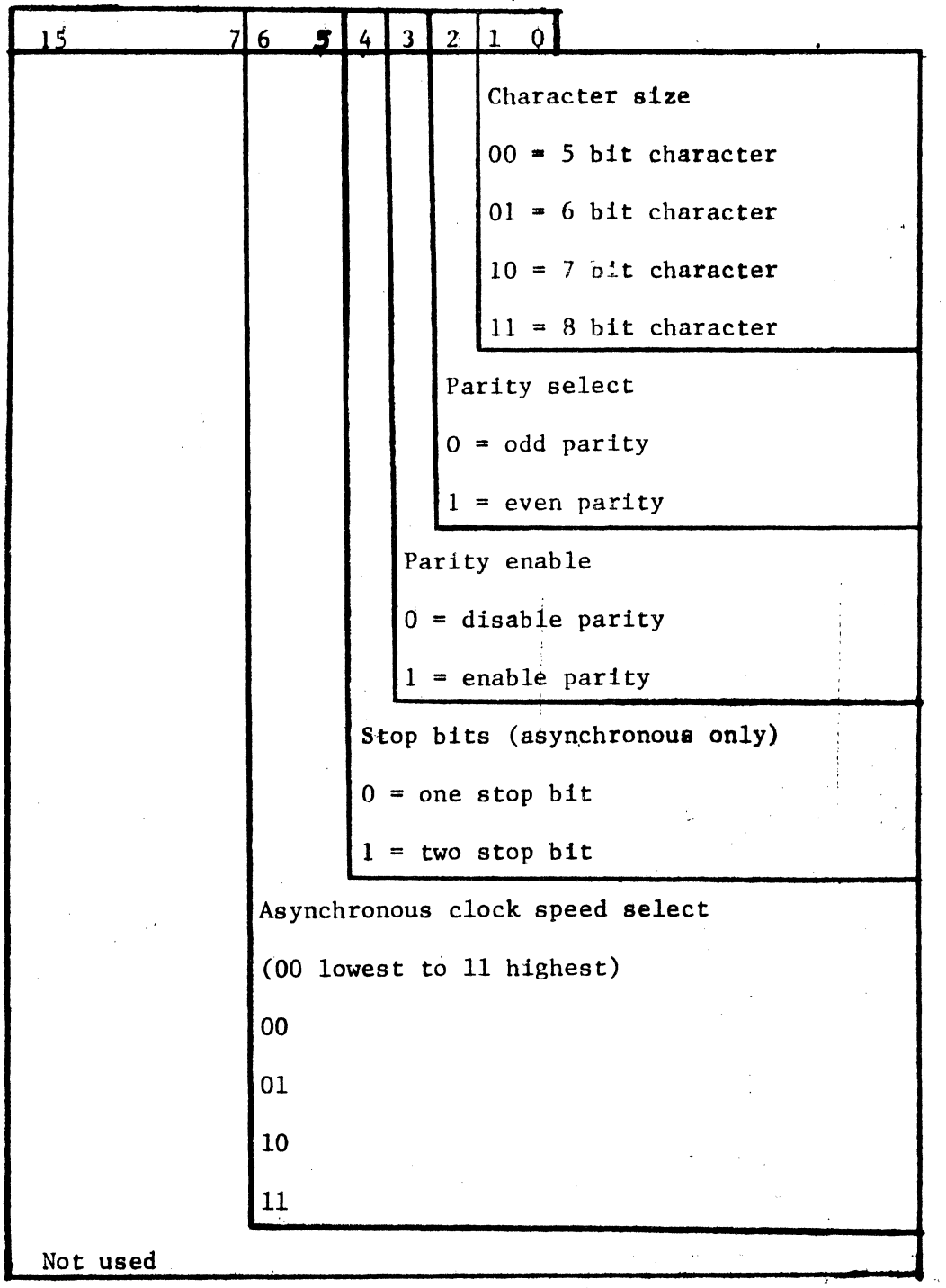


Figure 3-31. Serial Control Word Format

Table 3-20. I/O Buffer Control Word Bit Assignments

FUNCTION	CONTROL MEMORY LOCATION	BIT ASSIGNMENT	DESCRIPTION
Buffer Word Count	Location 0, 4	Bits 0-11	These bits specify the number of bytes, single length words, or double length words to be transferred during the selected operation. An initial count of zero specifies the maximum number of transfers (4096). The contents of the buffer word count are decremented by one for each single length transfer or for two byte transfers.
Byte Pointer	Location 0, 4	Bit 12	This bit specifies which half word (upper or lower) of the memory location specified by the BCW will be used for the next transfer as follows: 0 - upper byte (bits 15-8) 1 - lower byte (bits 7-0) This bit is toggled after each byte transfer.
Not used	Location 0, 4	Bit 13	
Transfer Mode	Location 0, 4	Bits 14, 15	These bits specify the word length to be transferred as follows: 00 Abort transfer 11 Byte transfer (8 bits) 10 Single length transfer (16 bits) 11 Dual channel (32-bit double length transfer)
Buffer Address Pointer	Location 1, 5	Bits 0-15	These bits are the main memory address specified for the next input data, output data, or external function transfer. During single length operations, the pointer is incremented by one for each transfer. During double length transfers, it is incremented by two. During byte transfer it is incremented by one whenever the byte pointer bit toggles from 1 to 0.

Table 3-21. Registers R1 and R2, and ALU Control for Buffers

R1	TM	X	B	Word Count			BCW1 Force / T1 Setup
R2	00	0	1	0	0	X	
ALU Mode	EXCL OR			R1 - 1			T2 EXECUTE TIME
R1	Address						BCW2 Force / T2 Setup
R2	0				0	*	
ALU Mode	R1 + R2						T3 EXECUTE TIME

X = Not significant

* Least significant bit (LSB) of R2 equals one, if: a) TM = Word Mode or, b) B = 1 (B = Byte Pointer of BCW 1 at T1 time).

NOTE

Update of control memory occurs on T3 and T4 times for DATA HIT · $\overline{EI}$. If it is a dual channel operation, PASS 1 does not update word count.

3-128. The -15 volt (NTDS Slow) interface uses 0 volts and -15 volts to represent binary one and binary zero respectively. The switching threshold is -60 $\pm$ 1.5 volts. Figure 3-34 illustrates the output driver-input amplifier interface.

3-129. The -15V input amplifier has the following characteristics:

1) Output of the circuit switches from binary zero to binary one whenever the input signal changes in the positive direction through the range of -7.5 volts to -4.5 volts.

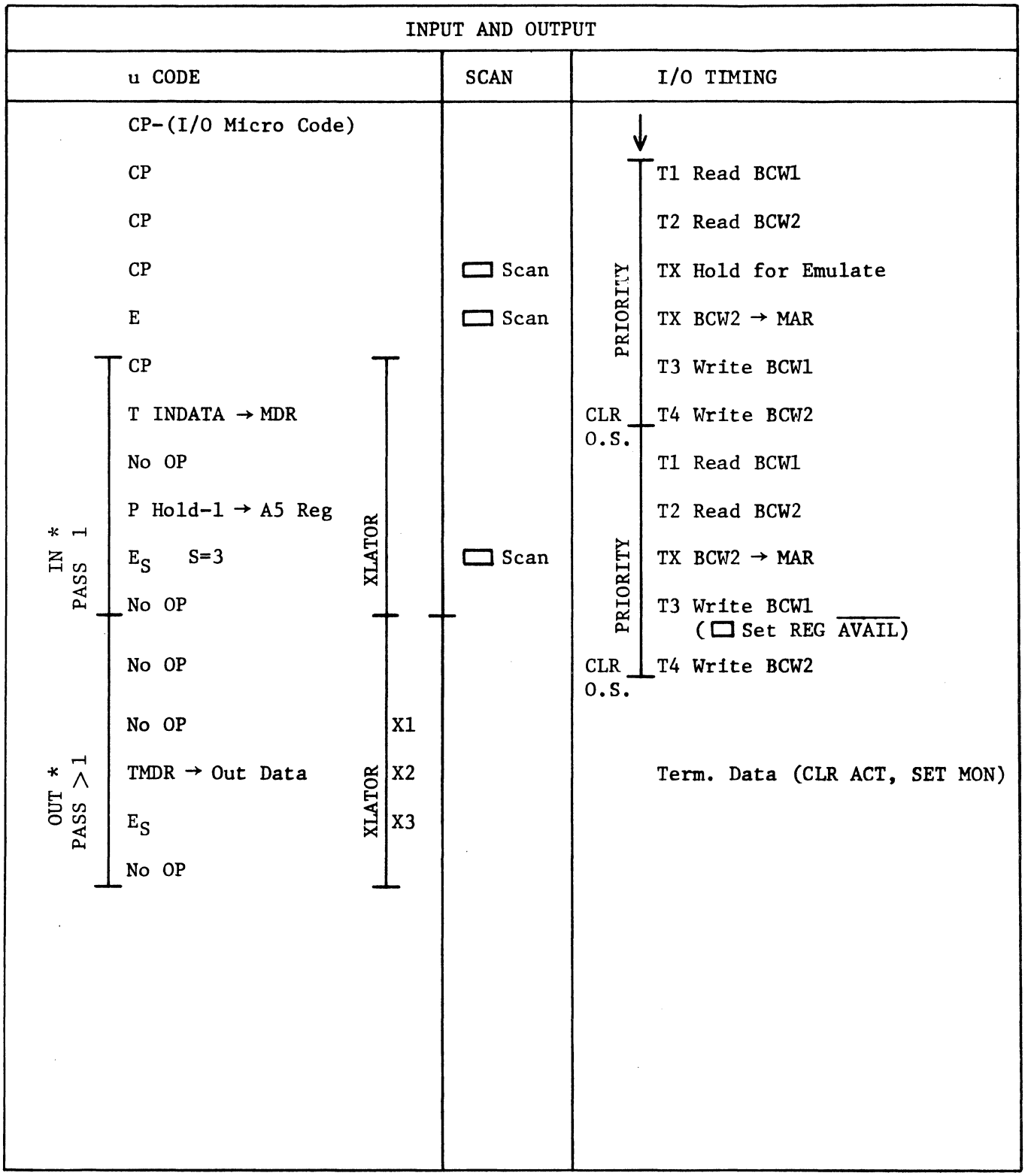
2) Output of the circuit switches from binary one to binary zero whenever the input signal changes in the negative direction through the range of -4.5 volts to -7.5 volts.

3) Circuit output is a binary zero whenever the steady state input signal is more negative than -7.5 volts, and a binary one if the steady state input is more positive than -4.5 volts.

4) If the circuit input is open-circuited, the output is a binary zero.

5) The circuit does not draw more than 4.0 milliamperes for a steady state binary one nor more than 1.0 milliamperes for a steady state binary zero.

Table 3-22. I/O Cycle Timing on Data Transfer



* Saves an address for return to operation if only one data transfer is required.
** No address is saved on multiple data transfers.

Table 3-23. I/O Dual Channel Output Data Transfer

u CODE			SCAN	I/O TIMING	
			Scan		TX
	CP (I/O Micro Code)				T3
	CP				T4
	CP				T1 Read BCW1
	CP				T2 Read BCW2
	E			PRIORITY	TX Hold
	CP				T3
OUT * PASS 1	No OP	XLATOR			T4 Write BCW2
	P Hold-1 → A5 Reg	X1			T1 Read BCW1
	T MDR → Out Data	X2			T2 Read BCW2
	E_{START}	X3	Scan		TX
	No OP				T3 Write BCW1
	No OP				T4 Write BCW2
	No OP	X1			
OUT ** PASS >1	T MDR → Out Data	X2			
	E_{START}	X3			
	No OP				

* Saves an address for return to operation if only one data transfer is required.
** No address is saved on multiple data transfers.

Table 3-24. I/O Dual Channel Input Data Transfer

u CODE	SCAN	I/O TIMING
CP	Scan	TX
CP		T3
CP		T4
CP		T1 Read BCW1
CP		T2 Read BCW2
E	No Scan on DL·PASS 1	TX Hold
CP		T3 DL·PASS 1, No BCW1 UPDATE
T In Data → MDR		T4 Write BCW2
No OP		T1 Read BCW1
P Hold-1 → A5 Reg		T2 Read BCW2
E_{START} S=3	Scan	TX Hold
No OP		T3 Write BCW1
T In Data → MDR		T4 Write BCW2
No OP		
No OP		
E_{START} S=3		
No OP		

IN * PASS 1 — XLATOR X1, X2, X3

IN ** PASS >1 — XLATOR X1, X2, X3

PRIORITY

CLR PASS 1 CONTROL
A_5 → uP
A_6 → A_6

Highest u Int:
Returns control to CP u Code
at point of I/O Break In.

* Saves an address for return to operation if only one data transfer is required.
** No address is saved on multiple data transfers.

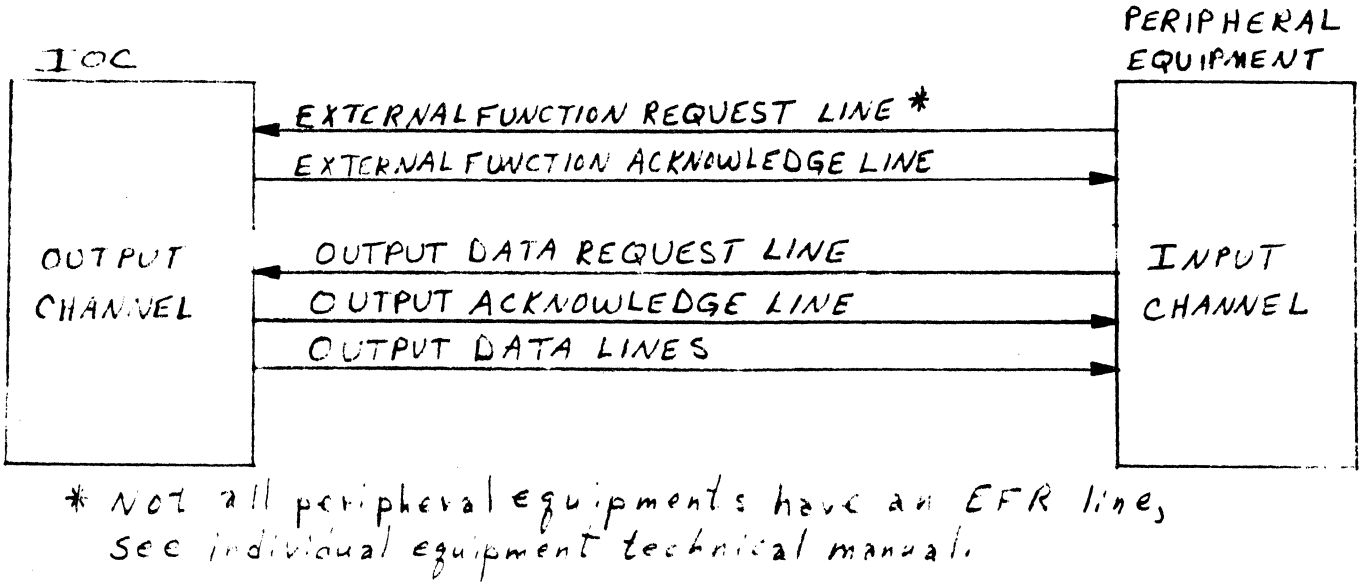


Figure 3-32. Parallel Output Communication Interface

Table 3-25. Function of Parallel Output Channel Lines

NAME OF LINE	DIRECTION OF SIGNAL	FUNCTION
External Function Request Line (Control)	Peripheral Equipment to IOC	Set condition indicates readiness of the peripheral equipment to accept an External Function Code Word on that channel.
External Function Acknowledge Line (Control)	IOC to Peripheral Equipment	Set condition indicates the IOC has placed an External Function Code Word on the Output Data Lines of that channel.
Output Data Request Line (Control)	Peripheral Equipment to IOC	Set condition indicates readiness of the peripheral equipment to accept a word of data on that channel.
Output Acknowledge Line (Control)	IOC to Peripheral Equipment	Set condition indicates the IOC has placed a word of data on the Output Data Lines of that channel.
Output Data Lines (16-Bit Data)	IOC to Peripheral Equipment	Carry 16-bit output data word.

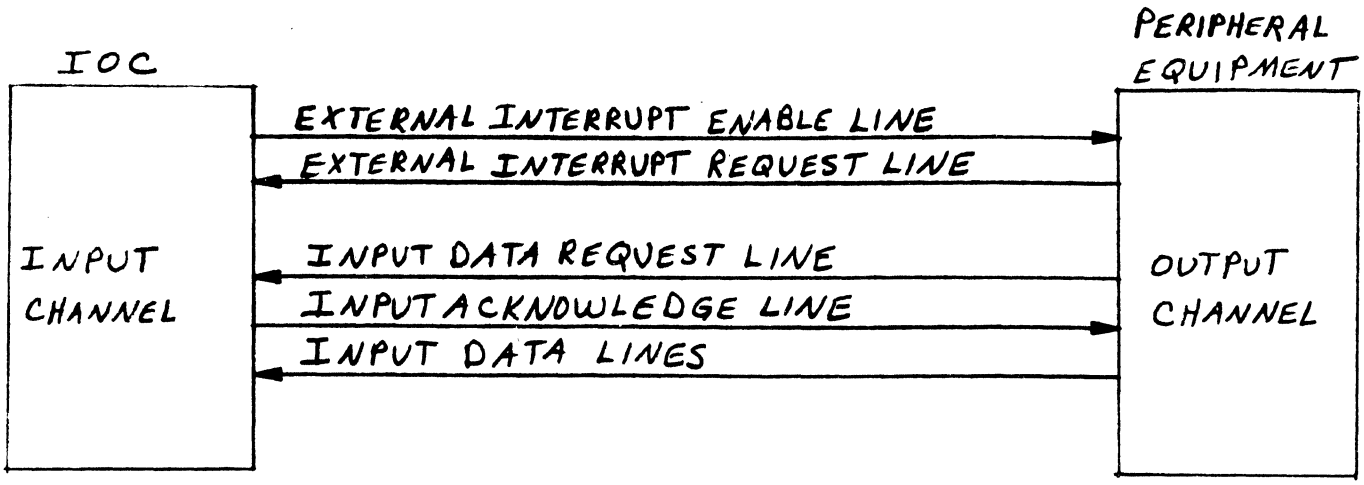


Figure 3-33. Parallel Input Communication Interface

Table 3-26. Function of Parallel Input Channel Lines

NAME OF LINE	DIRECTION OF SIGNAL	FUNCTION
External Interrupt Enable Line (Control)	IOC to Peripheral Equipment	Set condition indicates readiness of the IOC to accept an External Interrupt Code Word on that channel.
Input Data Request Line (Control)	Peripheral Equipment to IOC	Set condition indicates that the peripheral equipment has placed a word of data available to the IOC on the Input Data Lines of that channel.
External Interrupt Request Line (Control)	Peripheral Equipment to IOC	Set condition indicates the peripheral equipment has placed an Interrupt Code word available to the IOC on the Input Data Lines of that channel.
Input Acknowledge Line (Control)	IOC to Peripheral Equipment	Set condition indicates that the IOC has sampled the Input Data Lines of that channel.
Input Data Lines (16-Bit Data)	Peripheral Equipment to IOC	Carry 16-bit input data word.

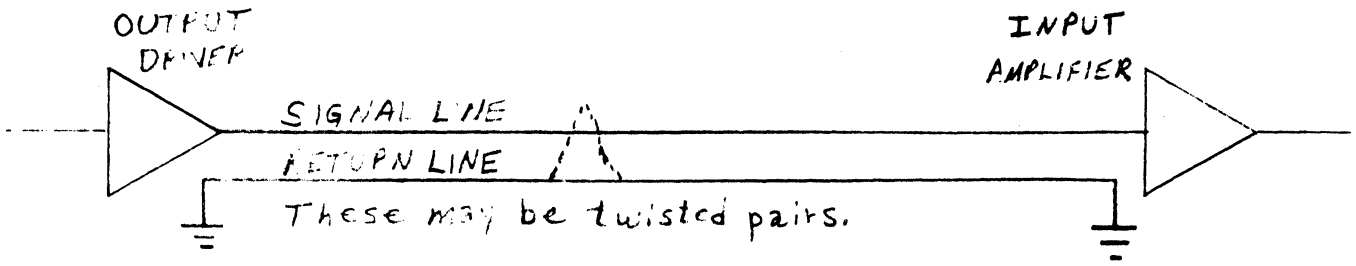


Figure 3-34. Parallel Slow (-15V) Interface

6) Circuit output does not switch as a result of any input transient-pulse signal with an integrated amplitude-duration of less than 15 volt-microseconds (a delay of 1.5 $\pm$ 0.5 microseconds with a 15-volt step input).

3-130. The -15V output driver has the following characteristics when driving a line with 6000 or 12,000 picofarads capacitance:

1) Binary one steady state output voltage is -1.5 volts to +1.5 volts.

2) Binary zero steady state output voltage is -10.0 volts to -17.5 volts.

3) Voltage variations between all binary zero output signals on one channel does not exceed 1.0 volt.

4) Voltage variations between all binary one output signals on one channel does not exceed 1.0 volt.

5) The circuit is capable of supplying 4.0 milliamperes per line for a steady state binary one output, or of sinking 1.0 milliamperes per line for a steady state binary zero output.

6) Circuit output switches in not more than 6.0 microseconds (measured between 10 and 90 percent amplitude points), and at a rate of not more than 5.0 volts per microsecond.

7) If power to the control line driver circuit is removed, the driver presents not less than 100,000 ohms impedance to the line with the restriction that the line voltage is within the range of -10.0 to -17.5 volts.

3-131. The -3 volt (NTDS Fast) interface uses 0 volts and -3 volts to represent binary one and binary zero respectively. The switching threshold is -1.5 $\pm$ 0.4 volts. Figure 3-35 illustrates the output driver-input amplifier interface.

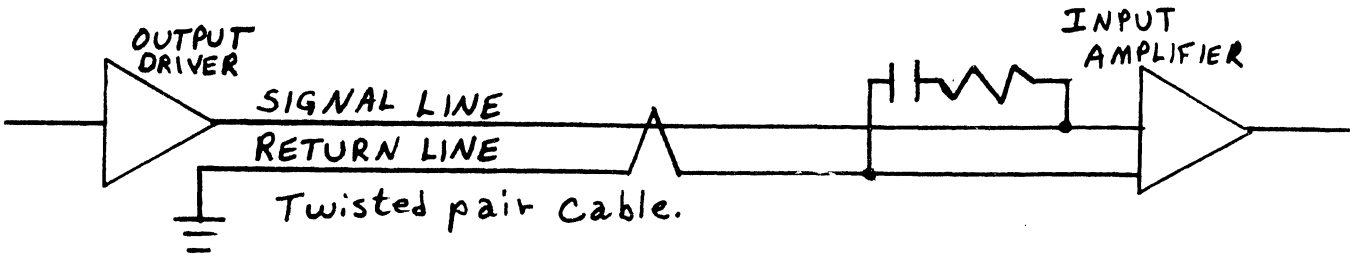


Figure 3-35. Parallel Fast (-3V) Interface

3-132. The -3V input amplifier has the following characteristics:

1) Circuit output switches from binary zero to binary one whenever the input signal changes in the positive direction through the range of -1.9 volts to -1.1 volts.

2) Circuit output switches from binary one to binary zero whenever the input signal changes in the negative direction through the range of -1.1 to -1.9 volts.

3) Circuit output is a binary zero whenever the steady state input signal is more negative than -1.9 volts, and a binary one if the steady state input is more positive than -1.1 volts.

4) If circuit input is open-circuited, the output is a binary zero.

5) The circuit does not draw more than 1.5 milliamperes for a steady state binary one nor more than 0.5 milliamperes for a steady state binary zero.

6) The circuit output will not switch as a result of any input transient-pulse signal that has an amplitude of less than 7.5 volts if its duration and amplitude are common to both sides of the line (common mode).

7) Circuit input presents a terminal impedance to the line equivalent to a resistance of 150 to 180 ohms in series with a capacitance of 0.0068 to 0.0100 microfarads.

3-133. The -3V output driver has the following characteristics when driving a line with impedance of 100 to 180 ohms:

1) Binary one steady state output voltage is 0.0 volts to -0.5 volts.

2) Binary zero steady state output voltage is -3.0 volts to -4.5 volts. (The voltage may be more negative if the driven input circuit presents a more negative signal, with the restriction that the driven input circuit negative voltage does not exceed -7.0 volts.)

3) The circuit is capable of supplying 1.5 milliamperes for a steady state binary one output, or of sinking 0.5 milliampere for a steady state binary zero output.

4) Circuit output switches in not more than 0.4 microseconds (measured between 0.5 and -3.0 volts).

5) If power to the control line driver circuit is removed, the driver presents not less than 100,000 ohms impedance to the line with the restriction that the line voltage is within the range of -3.0 to -7.0 volts.

3-134. The +3.5 volt (ANEW) interface uses 0 volts and +3.5 volts to represent binary one and binary zero respectively. The switching threshold is between +0.8 and +2.2 volts. Figure 3-36 illustrates the output driver-input amplifier interface.

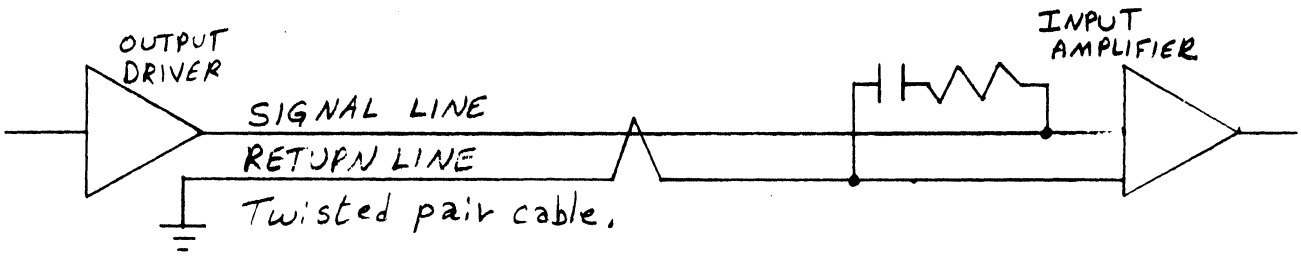


Figure 3-36. Parallel ANEW (+3.5V) Interface

3-135. The +3.5V input amplifier has the following characteristics:

1) Output of the circuit switches from binary zero to binary one whenever the input signal changes in the negative direction through the range of +2.2 volts to +0.8 volts.

2) Output of the circuit switches from binary one to binary zero whenever the input signal changes in the positive direction through the range of +0.8 volts to +2.2 volts.

3) Circuit output is a binary zero whenever the steady state input signal is more positive than +2.2 volts, and a binary one if the steady state input is more negative than +0.8 volts.

4) If the circuit input is open circuited, the output is a binary zero.

5) The circuit does not draw or provide more than 2.5 milliamperes when a +3 volt or 0 volt signal, respectively, is applied to the signal input terminal.

6) The circuit output does not switch as a result of any input transient-pulse signal that has an amplitude between +6.0 and -6.0 volts if its duration and amplitude are common to both sides of the line (common mode).

7) Input circuit presents a terminal impedance to the line equivalent to a resistance of 110 to 160 ohms in series with a capacitance of 0.0068 to 0.01 microfarad.

8) Signal input and return input terminal input resistances are matched to within ±8 percent.

3-136. The +3.5 volt output driver has the following characteristics when driving a line with impedance of 100 to 180 ohms:

1) Binary one steady state output voltage is 0.0 to +0.45 volt. The output driver sinks a current of 40 milliamperes at the +0.45 volt level.

2) Binary zero steady state output voltage is +2.7 volts minimum when supplying 27 milliamperes, or +4.5 volts maximum when open circuited.

3) Output voltage fall times (90% to 10%) and rise times (10% to 90%) are less than 100 nanoseconds.

4) If power to the control line driver is removed, the driver presents not less than 100,000 ohms impedance to the line with the restriction that the line voltage is within the range of +3.0 to +7.0 volts.

3-137. Parallel I/O Timing. Figures 3-37 through 3-42 illustrate the minimum durations of signals, and timing between signals, in the communication sequence for each of the three types of parallel interfaces. Figures 3-37 and 3-38 are for the Slow (-15V) interface. Figures 3-39 and 3-40 are for the Fast (-3V) interface. Figures 3-41 and 3-42 are for the ANEW (+3.5V) interface. I/O operation timing is provided by the DPS Master Clock and is developed into timing signals T1, T2, T3, and T4 in the IOC timing circuitry (logic diagram, figure 9-202).

3-138. When the Input Data Request (IDR) Line is set, the peripheral equipment must clear the IDR Line at least 20 microseconds before it changes the data on the input data lines and sets the External Interrupt Request (EIR) line. This prevents the DPS from interpreting the External Interrupt Code Word (EICW) on the input data lines as an input data word.

3-139. When the External Interrupt Request (EIR) line is set, the peripheral equipment must clear the EIR line at least 20 microseconds before it changes the external interrupt data on the input data lines and sets the Input Data Request (IDR) line. This prevents the DPS from interpreting the input data word on the input data lines as an External Interrupt Code Word (EICW).

3-140. Parallel I/O Operations. The following paragraphs describe the interaction of the IOC and the peripheral equipment for the various parallel I/O operations. Table 3-19 lists the various I/O chip functions.

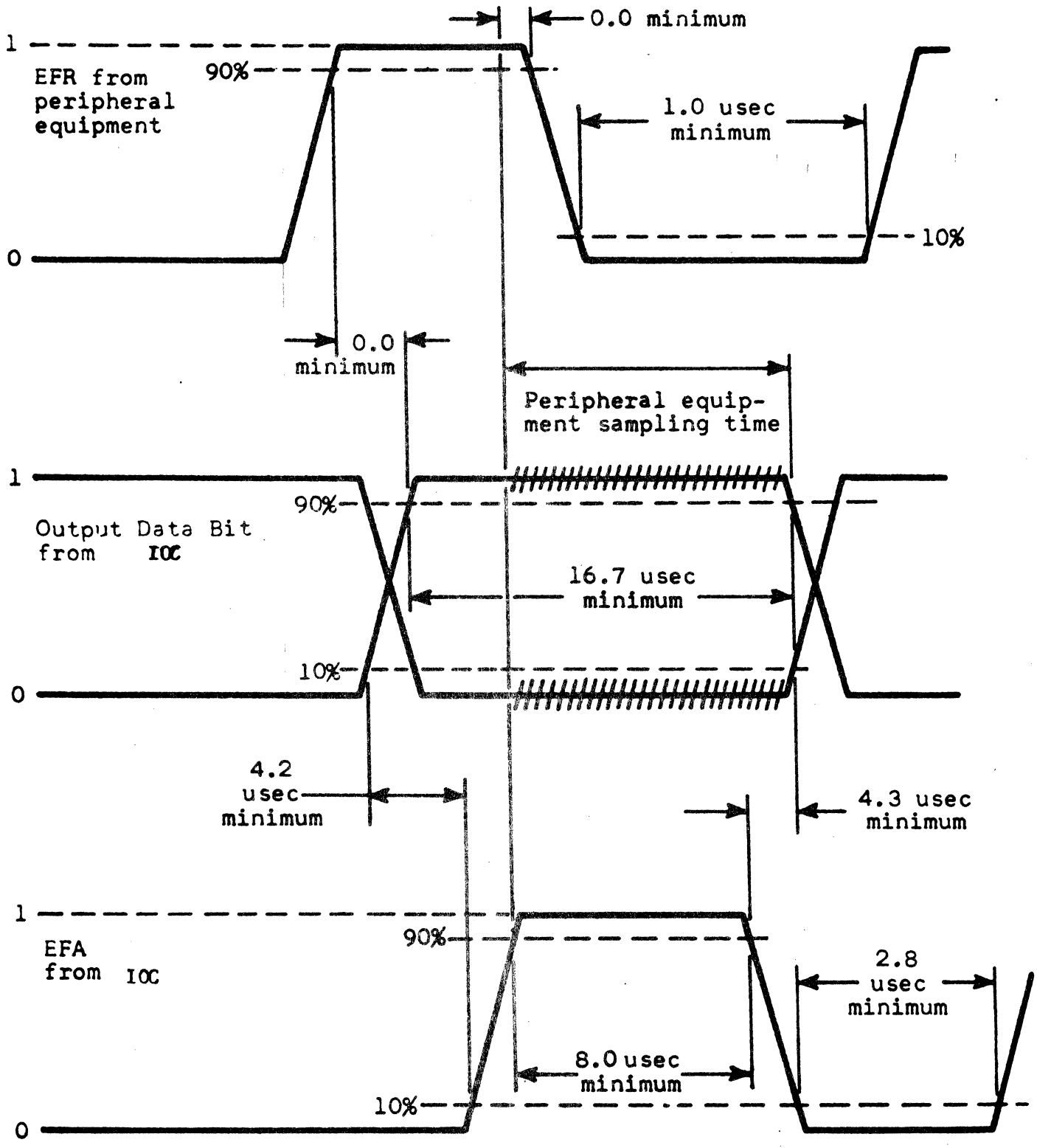


Figure 3-37. Parallel I/O External Function or Output Data Timing (-15 Volt Interface)

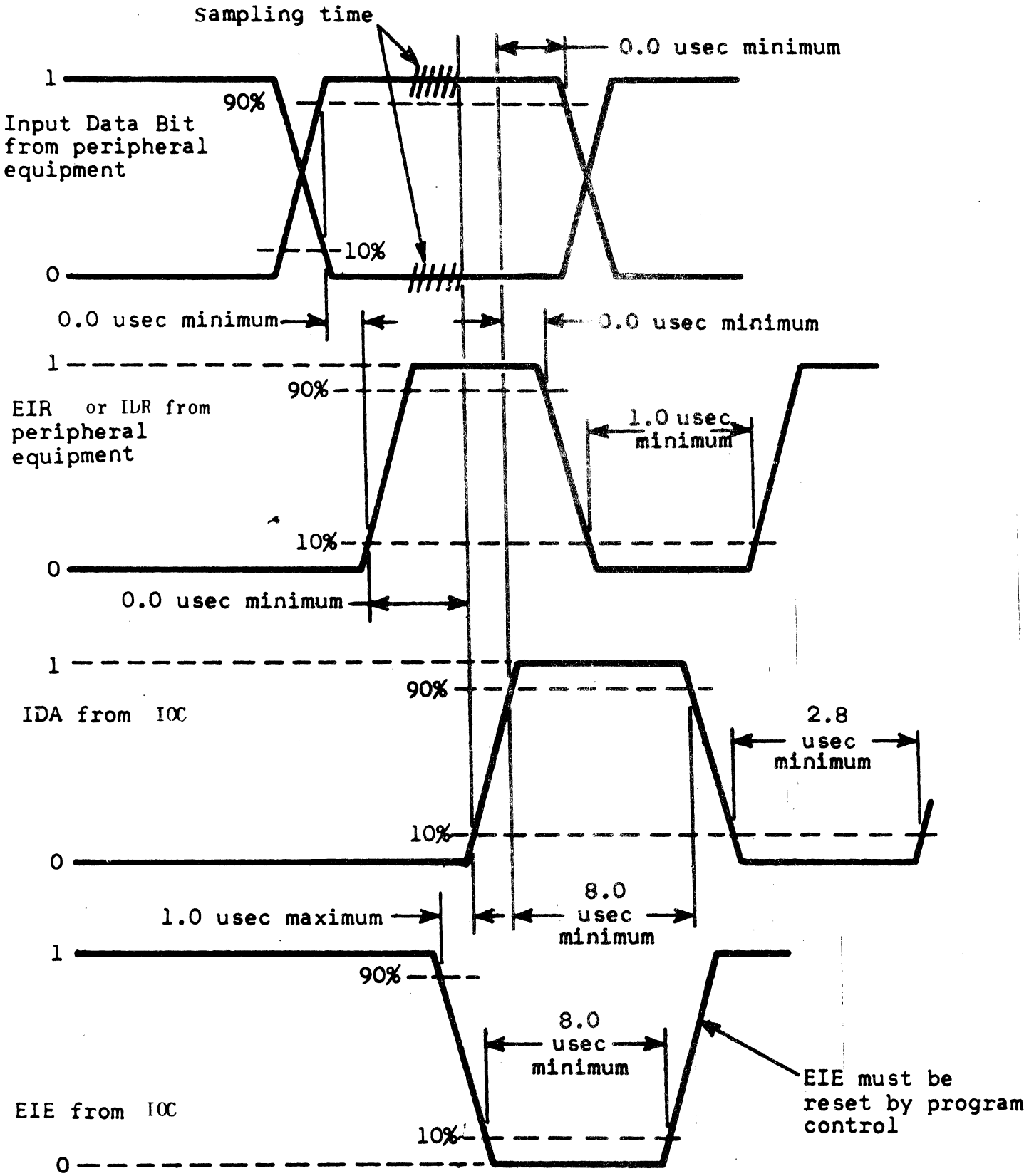


Figure 3-38. Parallel I/O External Interrupt or Input Data Timing
(-15 Volt Interface)

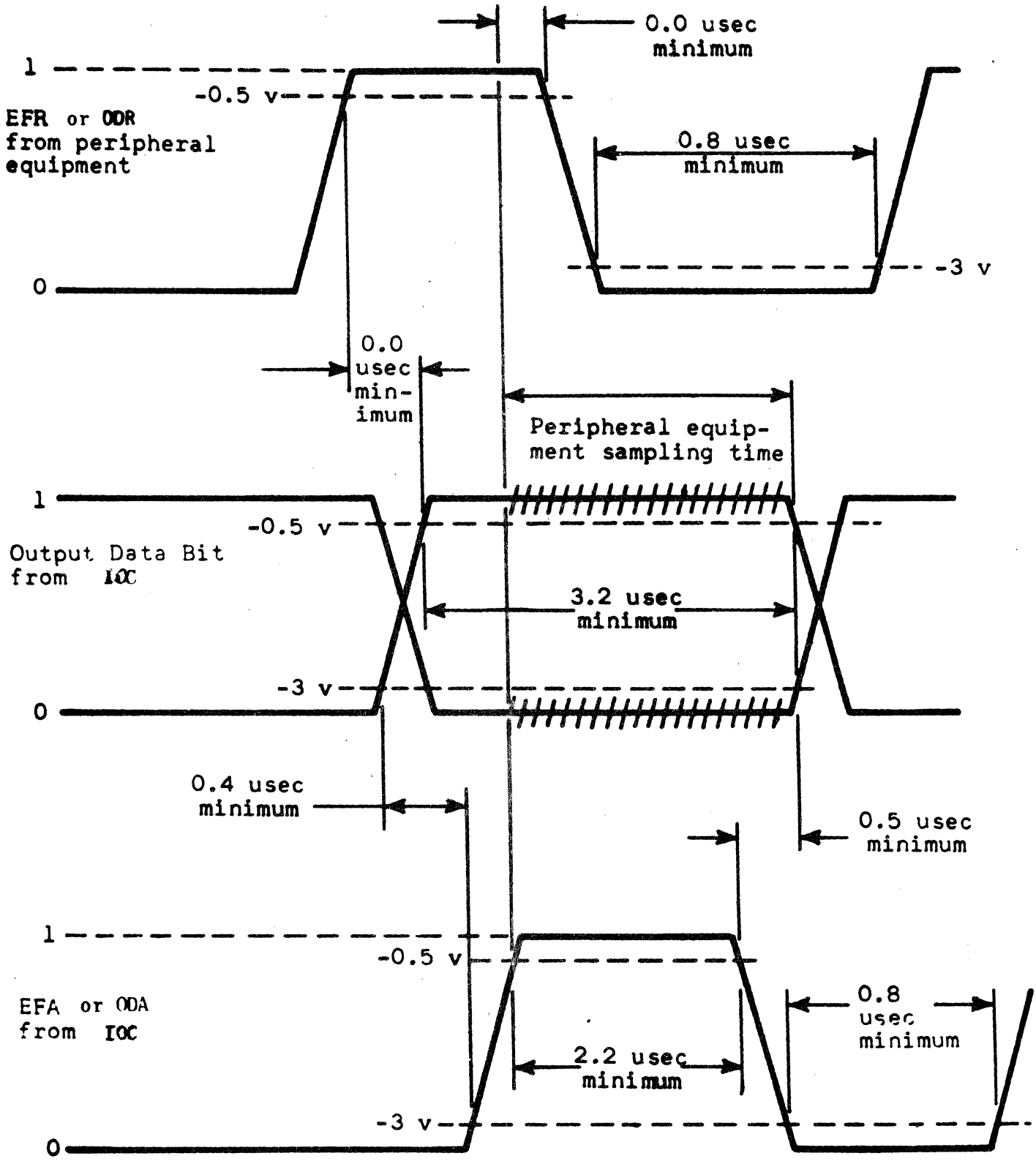


Figure 3-39. Parallel I/O External Function or Output Data Timing (-3 Volt Interface)

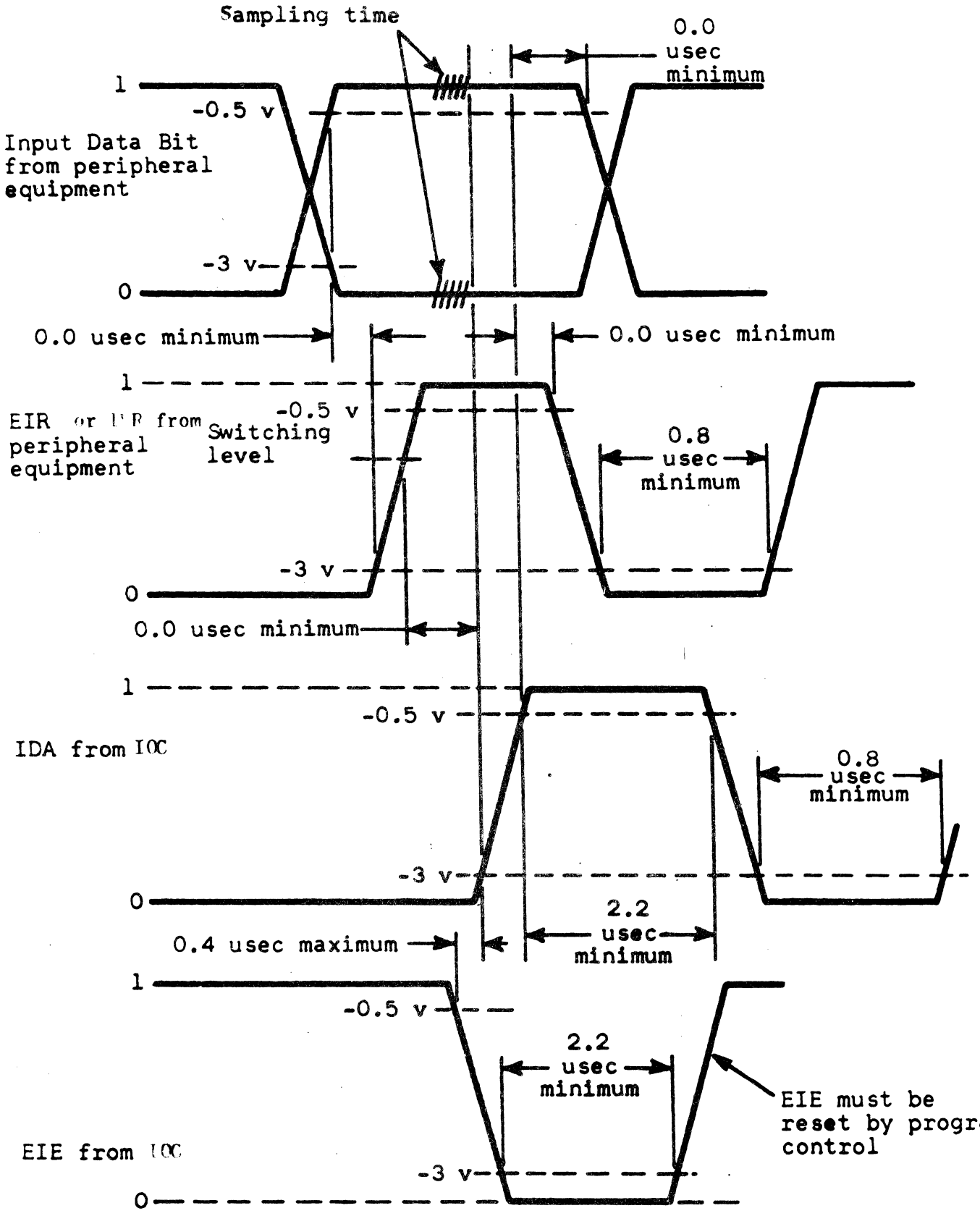


Figure 3-40. Parallel I/O Interrupt or Input Data Timing
(-3 Volt Interface)

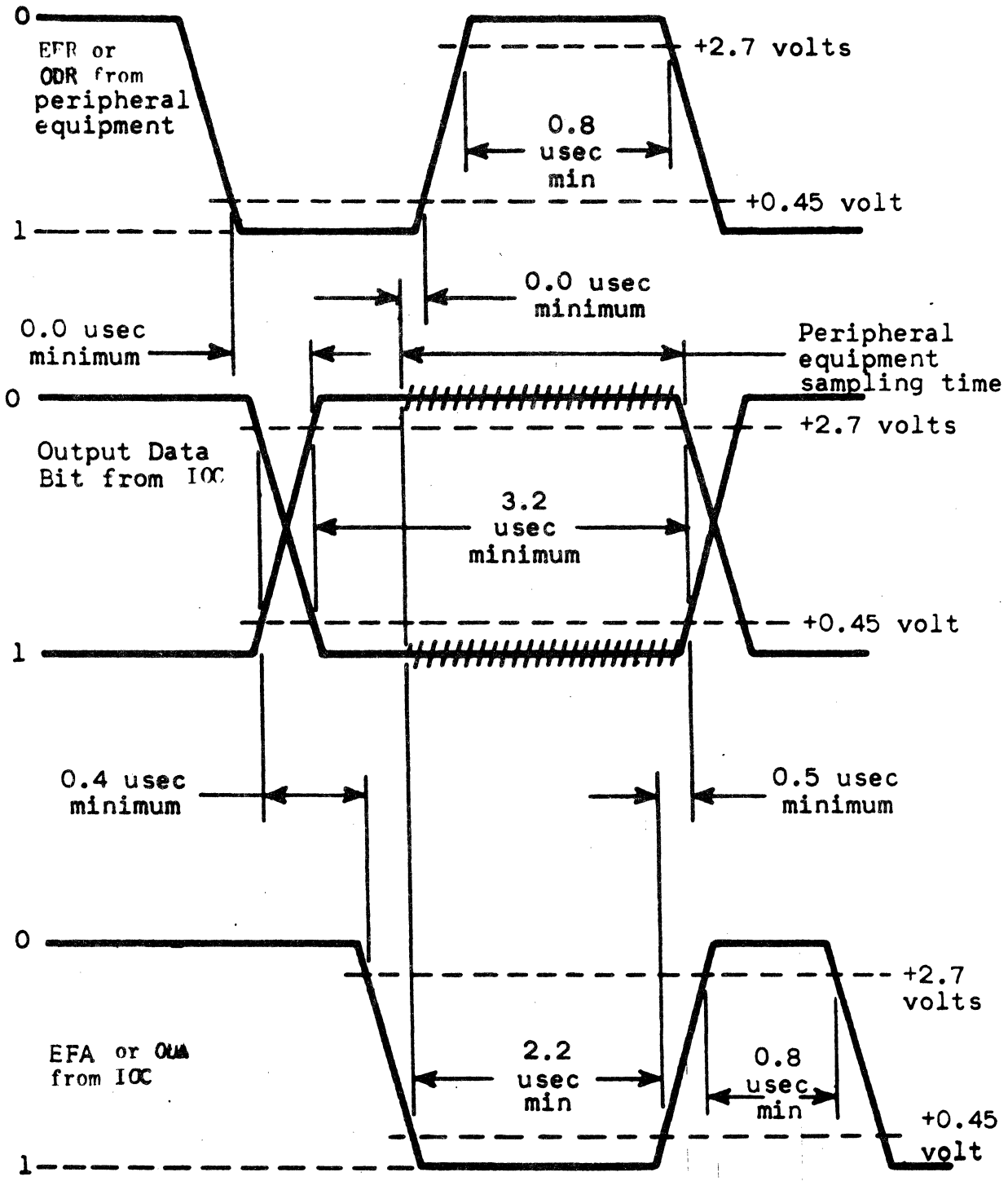


Figure 3-41. Parallel I/O External Function or Output Data Timing (+3.5 Volt Interface)

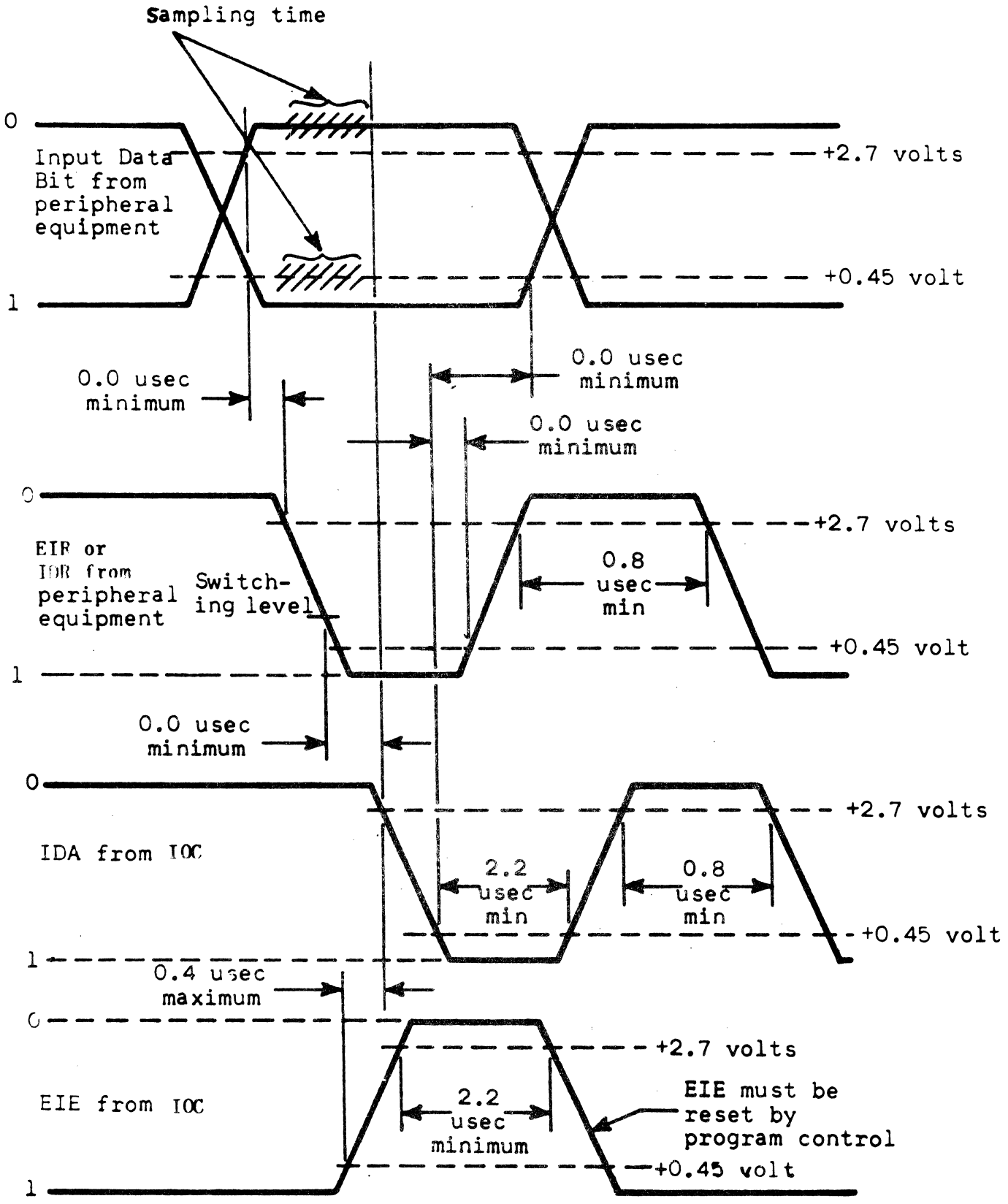


Figure 3-42. Parallel I/O External Interrupt or Input Data Timing (+3.5 Volt Interface)

3-141. When an External Function buffer has been established for a channel, the IOC and peripheral unit on that channel transfer an External Function Code Word (EFCW) in the following manner. See Figures 3-37, 3-39, or 3-41.

1) When the peripheral equipment is ready to accept an External Function Code Word, the peripheral equipment sets the External Function Request line (this may have already happened before the External Function buffer was established).

2) In accordance with internal priority, the IOC detects the setting of the External Function Request line.

3) The IOC places an EFCW on the output data lines.

4) The IOC sets the External Function Acknowledge line (to indicate that the External Function Code Word is on the output data lines).

5) The peripheral equipment detects the setting of the External Function Acknowledge line. (The peripheral equipment may clear the External Function Request line any time after detecting the setting of the External Function Acknowledge line, but it must clear the External Function Request line before the IOC will recognize the next External Function Request.)

6) The peripheral equipment samples the External Function Code Word on the output data lines.

7) The IOC clears the External Function Acknowledge line before it places the next word on the output data lines.

NOTE

Steps 1 and 2 above are omitted for peripheral equipment which do not have an External Function Request (EFR) line.

3-142. When the current instruction of the DPS macroprogram is a Forced External Function, the IOC and peripheral unit on that channel transfer an External Function Code Word in the following manner. The External Function Request line is not involved and the transfer proceeds whether or not the External Function Request line is set. See figures 3-37, 3-39, or 3-41.

1) The IOC places an External Function Code Word on the output data lines.

2) The IOC sets the External Function Acknowledge line (to indicate the EFCW is on the output data lines).

3) The peripheral unit detects the setting of the External Function Acknowledge line. (The peripheral unit may clear the External Function Request line any time after detecting the setting of the External Function Acknowledge line, but it must clear the Request line before the IOC will recognize the next External Function Request.)

4) The peripheral unit samples the EFCW on the output data lines.

5) The IOC clears the External Function Acknowledge line before it places the next word on the output data lines.

NOTE

Programming restrictions may be required for peripheral equipment which cannot accept Forced External Functions at the rate possible. Refer to individual equipment specifications or technical manuals.

3-143. When an output data buffer has been established for a channel, the IOC and the peripheral unit on that channel transfer data in the following sequence. See figure 3-37, 3-39, or 3-41.

1) When the peripheral equipment is ready to accept data, the peripheral equipment sets the Output Data Request line (this may already have happened before the output data buffer was established).

2) In accordance with internal priorities, the IOC detects the setting of the Output Data Request line.

3) The IOC places a word of data on the output data lines.

4) The IOC sets the Output Acknowledge line (to indicate that a word of data is on the output data lines).

5) The peripheral equipment detects the setting of the Output Acknowledge line. (The peripheral equipment may clear the Output Data Request line any time after detecting the setting of the Output Acknowledge line, but it must clear the Output Data Request line before the IOC will recognize the next Output Data Request.)

6) The peripheral equipment samples the data word which is on the output data lines.

7) The IOC clears the Output Acknowledge line before it places the next word on the output data lines. The actual state (binary one or zero) of the data lines is detected, therefore the data lines need not be cleared between words.

3-144. The IOC and the peripheral equipment repeat the above sequence for each successive word of data until they have transferred the entire block of data words specified by the Output Buffer Control Words. On output operation, the IOC provides a delay between gating data to the output lines and setting the ODA or EFA lines to insure the data lines are stable for sampling any time the ODA or EFA lines are set. The ODR and EFR signals, once set by the peripheral unit, remain set until the IOC sets the corresponding acknowledge line, ODA or EFA respectively.

3-145. The IOC and peripheral unit transfer an External Interrupt Code Word (EICW) in the following manner. See figures 3-38, 3-40, or 3-42.

1) The IOC, under program control, sets the External Interrupt Enable line.

2) The peripheral equipment detects the setting of the External Interrupt Enable line.

3) The peripheral equipment places an External Interrupt Code Word on the input data lines.

4) The peripheral equipment sets the External Interrupt Request line (to indicate that the External Interrupt Code Word is on the input data lines).

5) In accordance with internal priorities, the IOC detects the setting of the External Interrupt Request line.

6) The IOC samples the External Interrupt Code Word which is on the input data lines.

7) The IOC sets the Input Acknowledge line.

8) Synchronously with step 7, the IOC clears the External Interrupt Enable line.

9) The peripheral equipment detects step 7 or both steps 7 and 8. (The peripheral equipment may clear the External Interrupt Request line any time after detecting the setting of the Input Acknowledge line, but it must clear the External Interrupt Request line before the IOC will recognize the next External Interrupt Request.)

10) The IOC clears the Input Acknowledge line before it samples the next word on the input data lines.

3-146. When an input data buffer has been established for a channel, the IOC and peripheral unit on that channel transfer data in the following sequence. See figures 3-38, 3-40, or 3-42.

1) The peripheral equipment places a word of data on the input data lines.

2) The peripheral equipment sets the Input Data Request line (to indicate that a word of data is on the input data lines).

3) In accordance with internal priorities, the IOC detects the setting of the Input Data Request line.

4) The IOC samples the data word which is on the input data lines.

5) The IOC sets the Input Acknowledge line (indicating that it has sampled the data word on the input data lines).

6) The peripheral equipment detects the setting of the Input Acknowledge line. (The peripheral equipment may clear the Input Data Request line any time after detecting the setting of the Input Acknowledge line, but it must clear the Request line before the IOC will recognize the next Input Data Request.)

7) The IOC clears the Input Acknowledge line before it reads the next word on the input data lines. The actual state (binary one or zero) of the data lines is detected, therefore the data lines need not be cleared between words.

3-147. The IOC and peripheral equipment repeat the above sequence for each successive word of data until they have transferred the entire block of data words specified by the Input Buffer Control Words. Once the IDR or EIR has been set, the peripheral equipment must not change the state of the input data lines before the IOC has acknowledged the request. The only exception to this is that the IDR or EIR may be cleared before the IDA is received if the possible loss of data is of secondary importance.

3-148. The dual channel mode selector card is required to select dual channel mode. Dual channel operations occur during input data, output data, or external function transfers, when the transfer mode (TM) designators of a buffer control word specify double length (32-bit) I/O transfers. The two parallel channels used simultaneously (n, n + 4) are corresponding channels in consecutive 4-channel groups, which must have the same interface voltage level. Channel n must be in an even numbered group (group 0 or 2). Channel n controls the transfer, and channel n + 4 control is disabled. Channel n + 4 uses memory data located at address Y and channel n uses address Y + 1, where Y is the address specified in the buffer address pointer of the buffer control word. Y must be an even number and must contain the 16 most significant bits of the double length word, with Y + 1 containing the 16 least significant bits. During dual channel operation, an external interrupt word from the peripheral being referenced will be stored at the memory location corresponding to the lower channel (n) only. Tables 3-23 and 3-24 list the dual channel input and output sequences. See figure 3-43 for dual channel jumper cable block diagram. A jumper is plugged into both the input and output connectors on channel connectors of channels n and n + 4. Dual channels are capable of operation in Normal mode, Intercomputer mode (when so specified on initial order), or Externally Specified Addressing (ESA) mode (when so specified on initial order).

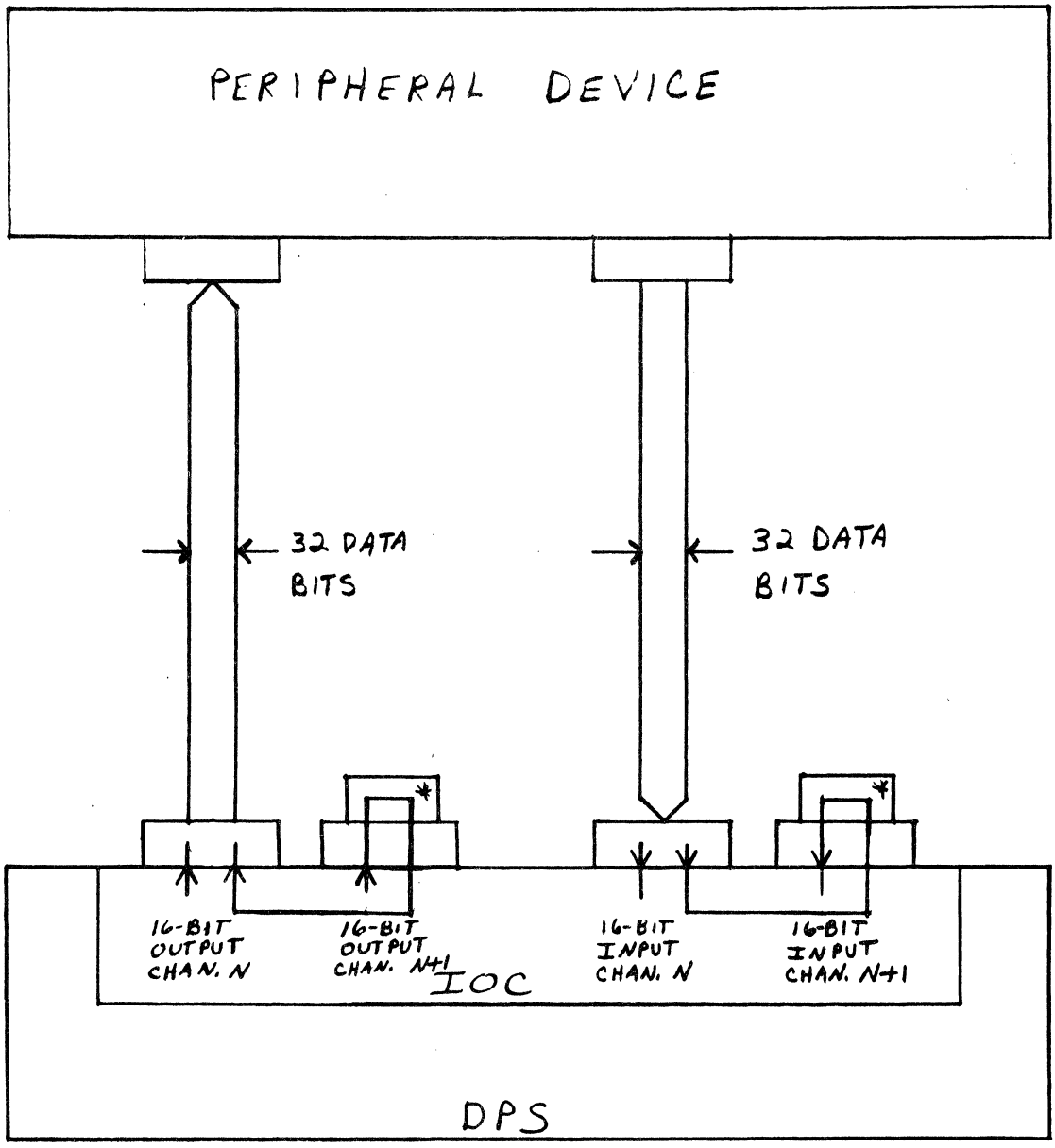
3-149. ESA mode provides an AN/UYK-7 compatible interface. On ESA mode an input and output channel pair may operate to send or receive data on a word-by-word basis. The peripheral device then specifies an address for each output and input word requested. On ESA mode output, the peripheral device places the address on the lower 16 bits of the input channel and signals via the Output Data Request line of the output channel. The IOC places the 32-bits of data (from the requested memory address) on the output channel and sends an Output Data Acknowledge. On ESA mode input, the peripheral device places the data on the high-order 16 data lines and the address on the low-order 16 data lines and signals via the Input Request line of the input channel. The IOC then stores the 32 data lines (data and address) at the requested memory address and sends an Input Acknowledge. Transfers are deactivated by the IOC executing a 70 RR instruction with an m-designator of 0 or 10, or by normal buffer termination. For channels to operate in the ESA mode, the mode selector card must be wired to select the ESA mode. Only dual channels operate in ESA.

3-150. When the DPS and another computer are connected as illustrated in figure 3-44, they are capable of transferring data in the intercomputer mode. Table 3-27 defines the function of each of the intercomputer channel control lines. The transmitting computer holds the data or EF code on the output data lines until the receiving computer sets the Resume line or the transmitting computer program intervenes to resolve no-resume condition.

3-151. Whenever an External Function buffer has been established in the transmitting computer for a channel, the transmitting computer and the receiving computer transfer a command word as follows:

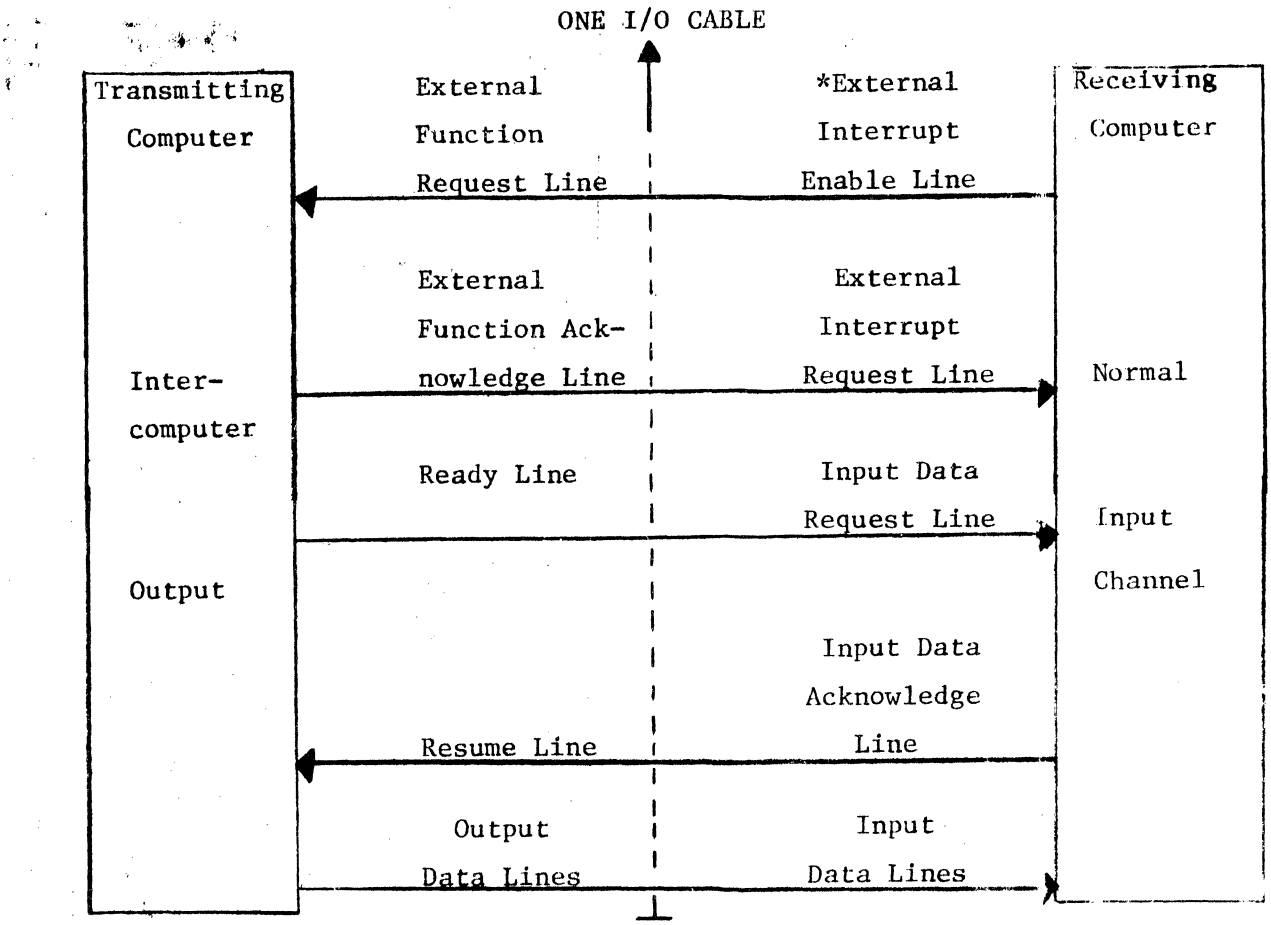
*1) When the receiving computer is ready to accept an External Function Command Word, the receiving computer, under program control, sets the External Interrupt Enable line.

* These steps are omitted for computers which do not have an EIE line.



* Dual Cap.

Figure 3-43. Parallel Dual Channel Jumper Cable Diagram



*Not all computers have an External Interrupt Enable (EIE) line; refer to the individual computer specification or technical manual.

Figure 3-44. Parallel I/O Intercomputer Interface

*2) In accordance with internal priority, the transmitting computer detects the setting of the External Interrupt Enable line (which it recognizes as its External Function Request line).

3) The transmitting computer places an External Function Command Word on the output data lines.

4) The transmitting computer sets the External Function Acknowledge line (to indicate that the External Function Command Word is on the output data lines).

5) In accordance with internal priorities, the receiving computer detects the setting of the External Function Acknowledge line of the transmitting computer (which it recognizes as its External Interrupt Request line).

6) The receiving computer samples its input data lines.

* These steps are omitted for computers which do not have an EIE line.

Table 3-27. Function of Intercomputer Channel Control Lines

NAME OF LINE	DIRECTION OF SIGNAL	FUNCTION
*External Interrupt Enable Line	Receiving Computer to Transmitting Computer	Set condition indicates readiness of the receiving computer to accept an EF command word on that channel.
Ready Line	Transmitting Computer to Receiving Computer	Set condition indicates that the transmitting computer has placed a word of data on the Output Data Lines of that channel.
External Function Acknowledge Line	Transmitting Computer to Receiving Computer	Set condition indicates the transmitting computer has placed an EF Command Word on the Output Data Lines of that channel.
Resume Line	Receiving Computer to Transmitting Computer	Set condition indicates that the receiving computer has sampled the Input Data Lines of that channel.

*Not all computers have the EIE Line; refer to the individual computer specification or technical manual.

7) The receiving computer sets its Input Acknowledge line.

*8) Synchronously with step 7, the receiving computer clears the External Interrupt Enable Line.

9) The transmitting computer detects the setting of the Input Acknowledge line of the receiving computer (which it recognizes as its Resume line).

10) The transmitting computer clears its External Function Acknowledge line before it places the next word on its output data lines, and the receiving computer clears its Input Acknowledge line before it reads the next word on its input data lines.

3-152. Whenever the current instruction of the transmitting computer program is a forced External Function, that computer transfers a Command Word to the other computer as follows:

1) The transmitting computer places an External Function Command Word on its output data lines.

2) The transmitting computer sets its External Function Acknowledge line (to indicate that a Command Word is on the data lines).

* These steps are omitted for computers which do not have an EIE line.

3) In accordance with internal priorities, the receiving computer detects the setting of the External Function Acknowledge line of the transmitting computer (which it recognizes as its External Interrupt Request line).

4) The receiving computer samples its input data lines.

5) The receiving computer sets its Input Acknowledge line.

6) The transmitting computer detects the setting of the Input Acknowledge line of the receiving computer (which it recognizes as its Resume line).

7) The transmitting computer clears its External Function Acknowledge line before it places the next word on its output data lines, and the receiving computer clears its Input Acknowledge line before it samples the next word on its input data lines.

3-153. Whenever an Output Data buffer has been established in the transmitting computer and an Input Data buffer has been established in the receiving computer for the same channel, the transmitting computer and the receiving computer transfer data as follows:

1) The transmitting computer places a word of data on its output data lines.

2) The transmitting computer sets its Ready line (to indicate that a word of data is on its output data lines).

3) In accordance with internal priorities, the receiving computer detects the setting of the Ready line of the transmitting computer (which it recognizes as its Input Data Request line).

4) The receiving computer samples the input data lines.

5) The receiving computer sets its Input Acknowledge line.

6) The transmitting computer detects the setting of the Input Acknowledge line of the receiving computer (which it recognizes as its Resume line).

7) The transmitting computer clears the Ready line before it places the next word of data on its output data lines, and the receiving computer clears its Input Acknowledge line before it samples the next word of data on its input data lines.

The computers repeat this sequence until they have transferred the block of words specified by the buffer control words.

3-154. MIL-STD-188 Serial I/O. The expanded MIL-STD-188 serial I/O channel interface in either synchronous or asynchronous mode is available as a plug-in option.

NOTE

I/O options are plug-in options, but adapter plugs and a rewired jumper mode card may be required to change from one I/O option to another. When an option requires a coaxial cable a 120-pin adapter plug with a coaxial connector is required.

Refer to Chapter 8 for interface jack, pin, and cable assignments. MIL-STD-188 serial I/O channels are available in groups of two channels with the characteristics

listed in table 3-28. Each channel is capable of internal loopback testing under program control. Figure 3-45 illustrates the expanded MIL-STD-188 interface. The MIL-STD-188 interface has seven discrete control lines with +6 volts ON and -6 volts OFF, and five discrete control lines with +6 volts ON and 0 volts OFF. All 12 of the discrete control may be used concurrently. The control lines are lettered rather than named as each application may use the discrete functions differently. Table 3-29 lists the control lines and their function, if designated. Lines TX Clock and RX Clock are used in synchronous mode only to gate the respective data lines. All interface lines for one channel are contained in one interface connector.

3-155. The MIL-STD-188 serial I/O interrupt word format is specified in figure 3-46. Either of the three discrete signals shown cause a Class III external interrupt (see table 3-10).

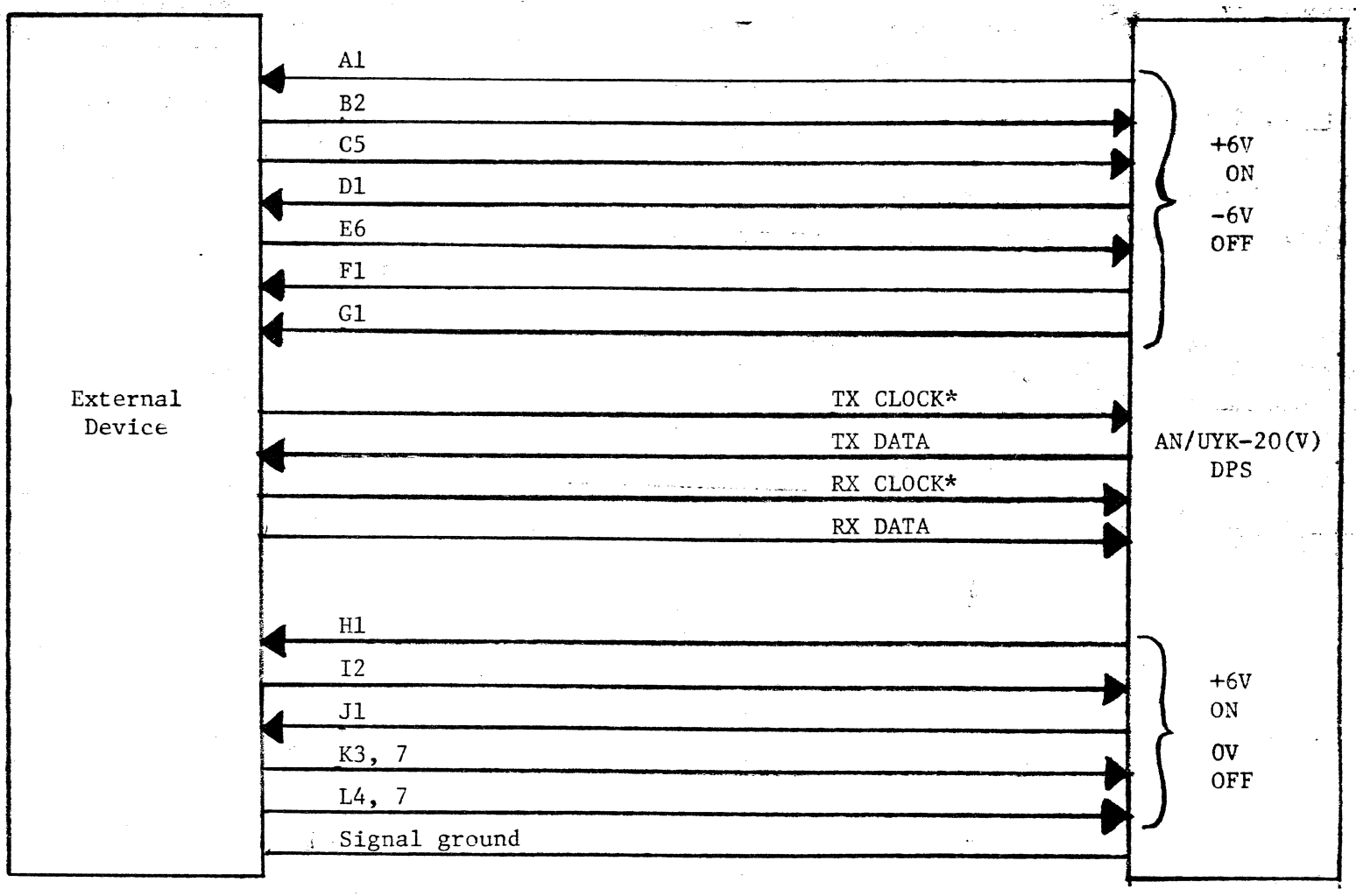
3-156. EIA RS-232 Standard Serial I/O. The RS-232 serial I/O channel interface in either synchronous or asynchronous mode is available as a plug-in option. Refer to Chapter 8 for interface jack, pin, and cable assignments. RS-232 serial I/O channels are available in groups of two channels with the characteristics listed in table 3-30. Each channel is capable of internal loopback testing under program control. Figure 3-47 illustrates the EIA RS-232 standard interface. The RS-232 interface uses eight discrete control lines plus two data and two clock (synchronous mode only) lines. All interface lines for each channel are contained in one interface connector, and all RS-232 data and control lines are EIA standard.

3-157. The RS-232 serial I/O interrupt word format is specified in figure 3-48. The Ring On or Carrier Off events set the Class III external interrupt (see table 3-10). The DPS stores the interrupt word at the main memory address assigned to its channel.

Table 3-28. MIL-STD-188 Serial I/O Characteristics

CHANNEL TYPE	MODULATION RATE	CHARACTER SIZE	CHARACTER INTERVAL
Synchronous	Up to 9600 Bits/Second	5, 6, 7, or 8 level (Selectable under program control)	Parity bit is program selectable, and if used is included in the character interval.
Asynchronous	75, 150, 300, 600, 1200, or 2400 Bits/ second (Any four* of above six rates available (per two channel group) as an ordering option).	5, 6, 7, or 8 level (Selectable under program control)	Includes a Start bit, and under program control one or two Stop bits and a Parity bit.

* Each of the four rates are program control selectable for each channel.



* Synchronous mode only

1. Under Program Control
2. Generates Class III Interrupts when switched to "ON"
3. Inhibits Input Transfers when "OFF"
4. Inhibits Output Transfers when "OFF"
5. Generates Class III Interrupt when switched to "OFF"
6. Available as Status to IOC Program
7. Line will go "ON" when disconnected

Figure 3-45. MIL-STD-188 Serial Channel Interface

Table 3-29. MIL-STD-188 Control Lines

CONTROL LINE	FUNCTION
A1	Under Program Control
D1	Under Program Control
F1	Under Program Control
G1	Under Program Control
H1	Under Program Control
J1	Under Program Control
B2	Generates Class III Interrupt when switched to ON
I2	Generates Class III Interrupt when switched to ON
K3	Inhibits Input Transfers when OFF
L4	Inhibits Output Transfers when OFF
C5	Generates Class III Interrupt when switched to OFF
E6	Available as status to IOC Program
K7	Line goes ON when Disconnected
L7	Line goes ON when Disconnected

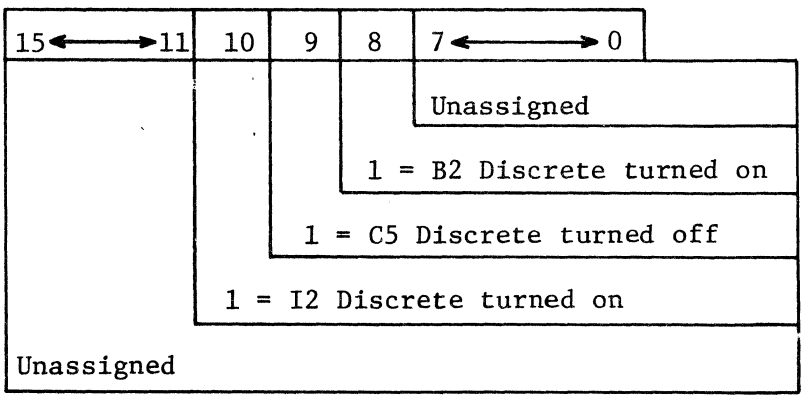


Figure 3-46. MIL-STD-188 Interrupt Word Format

Table 3-30. RS-232 Standard Serial I/O Characteristics

CHANNEL TYPE	MODULATION RATE	CHARACTER SIZE	CHARACTER INTERVAL
Synchronous	Up to 9600 Bits/second	5, 6, 7, 8 Level (Selectable under program control)	Parity bit is program selectable, and if used is included in the character interval.
Asynchronous	75, 150, 300, 600, 1200*, or 2400* Bits/second (Any four** of above six rates available (per two channel group) as an ordering option).	5, 6, 7, or 8 Level (Selectable under program control)	Includes a Start bit, and under program control one or two Stop bits and a Parity bit.

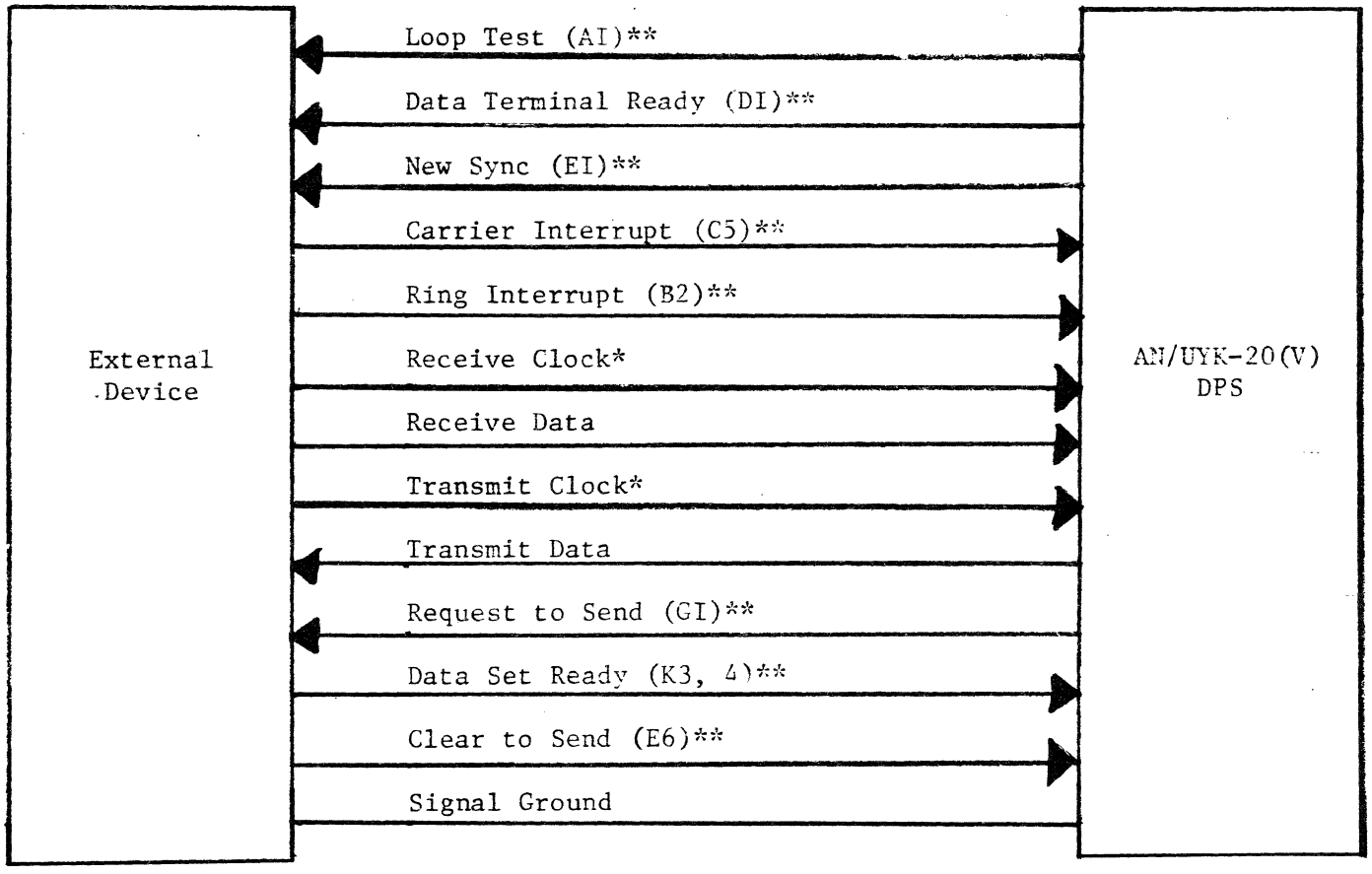
* 1200 and 2400 Bits/second options available at a future date.
** Each of the four rates are program control selectable for each channel.

3-158. NTDS 32-Bit Serial I/O. The NTDS serial I/O channel is available as a plug-in option on the DPS, when so specified on order. NTDS serial I/O channels operate in asynchronous mode and are 32 bits in length (a dual AN/UYK-20(V) word length). Each serial NTDS group consists of an output channel and an input channel. The output channel uses one cable connected at the even-numbered output channel location, and the input channel uses one cable connected at the even-numbered input channel location. The odd-numbered I/O channel connector locations are not used. Each cable, output and input, consists of a coaxial signal line and a return line as shown in figure 3-49. Both the output and input channels transfer 32-bits of data along with sync bits, identifier bits, and control bits. Table 3-31 lists the characteristics of the NTDS 32-bit channel.

3-159. The NTDS serial interface receives control frames, input data words, and external interrupt control words. It transmits control frames, output data words, and external function words. See figure 3-50. There are four types of control frames. Each control frame consists of a sync bit followed by two control bits. For each type of control frame, the two control bits specify the control function (nature of the request or enable, or the not ready status of the equipment). Figure 3-51 defines the four types of control frames.

3-160. The EF and EI control words and the data words have the format shown in figure 3-52. The first bit is the sync bit, the second is the word identifier, and the remaining bits are the information bits of the word.

3-161. The IOC continually interrogates the peripheral equipment on each NTDS serial output channel by sending Output Enable Control Frames (OECF) to the peripheral



* Synchronous mode only
** MIL-STD-188 equivalent

Figure 3-47. EIA RS-232 Standard Serial Channel Interface

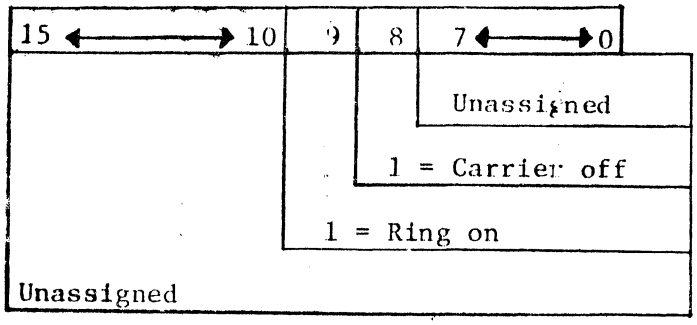


Figure 3-48. RS-232 Interrupt Word Format

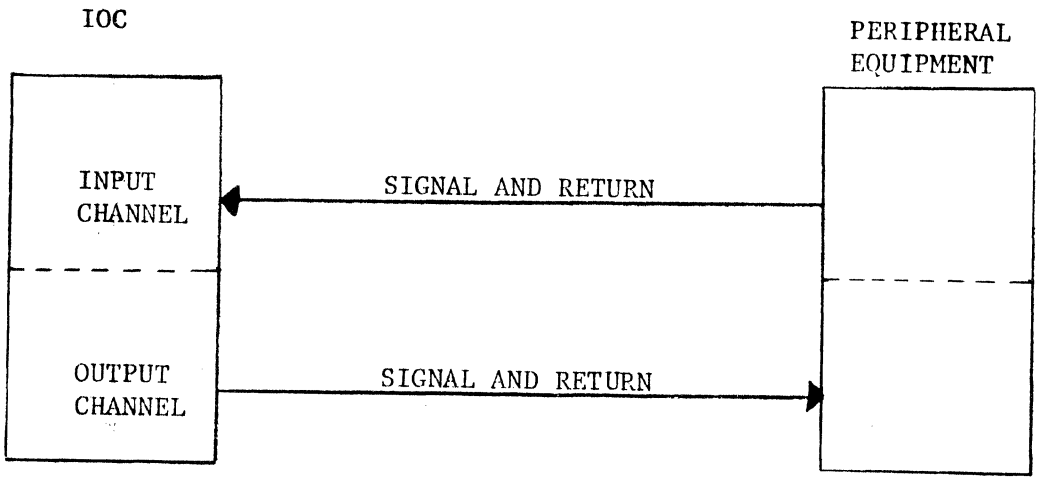


Figure 3-49. NTDS 32-Bit Serial I/O Channel

Table 3-31. NTDS 32-Bit Serial I/O Characteristics

CHANNEL TYPE	MODULATION RATE	DATA CHARACTER SIZE	CHARACTER INTERVAL
Asynchronous	75, 150, 300, or 600 Bits/ second (Accuracy of 1%)	5 or 7 data elements	Consists of ten signal elements with equal time intervals; one start, seven or five data, one Character parity, and one or two stop elements (programing option).

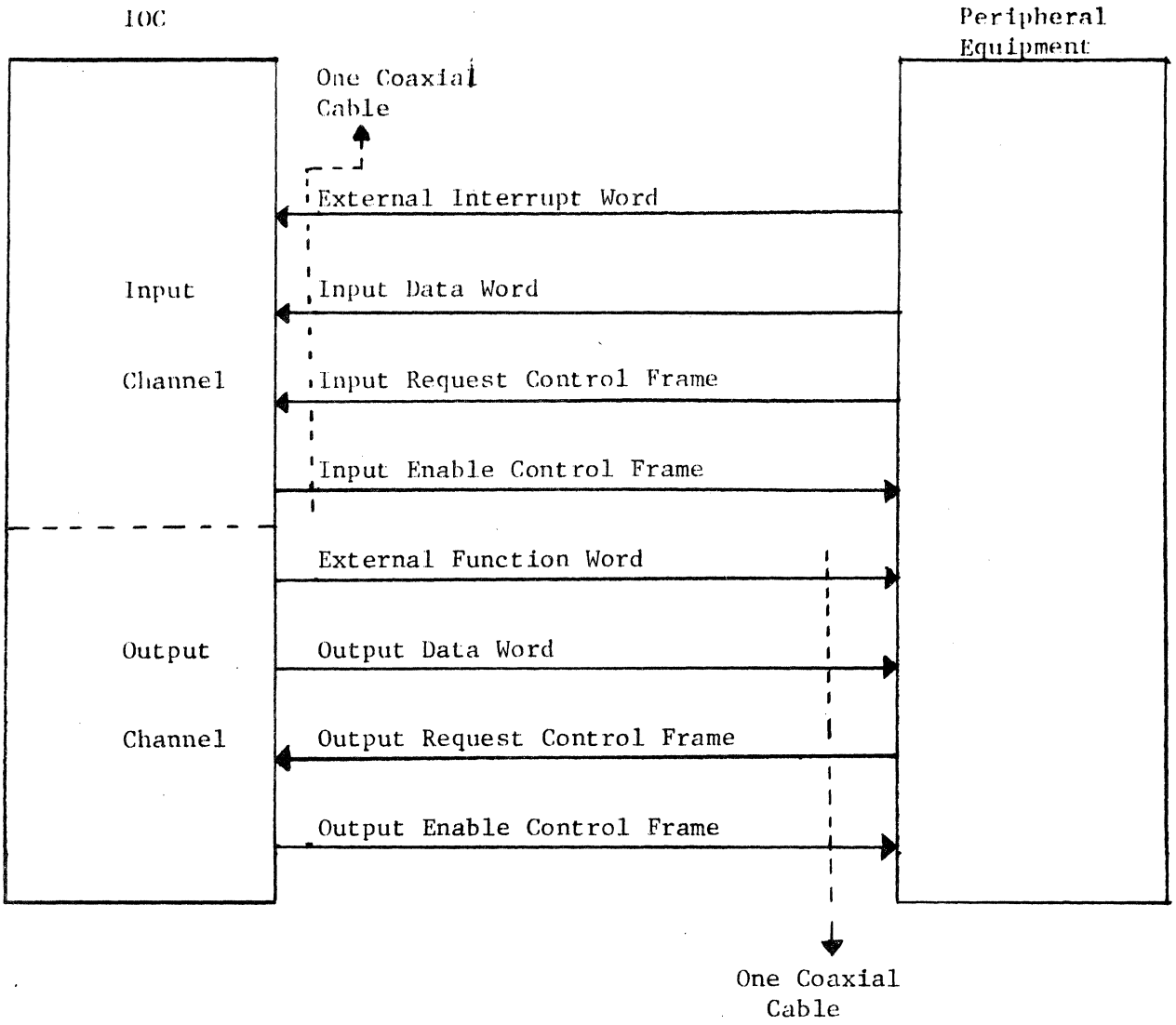


Figure 3-50. NTDS Serial Channel Interface

3	2	1	
		Synchronization Bit	
0	0	=	Not Used
0	1	=	Input Data Request (IDR)
1	0	=	External Interrupt Request (EIR)
1	1	=	IDR and EIR

a. Input Request Control Frame (IRCF), Peripheral-to-DPS

3	2	1	
		Synchronization Bit	
0	0	=	Not Ready
0	1	=	Input Data Enable (IDE)
1	0	=	External Interrupt Enable (EIE)
1	1	=	IDE and EIE

b. Input Enable Control Frame (IECF), DPS-to-Peripheral

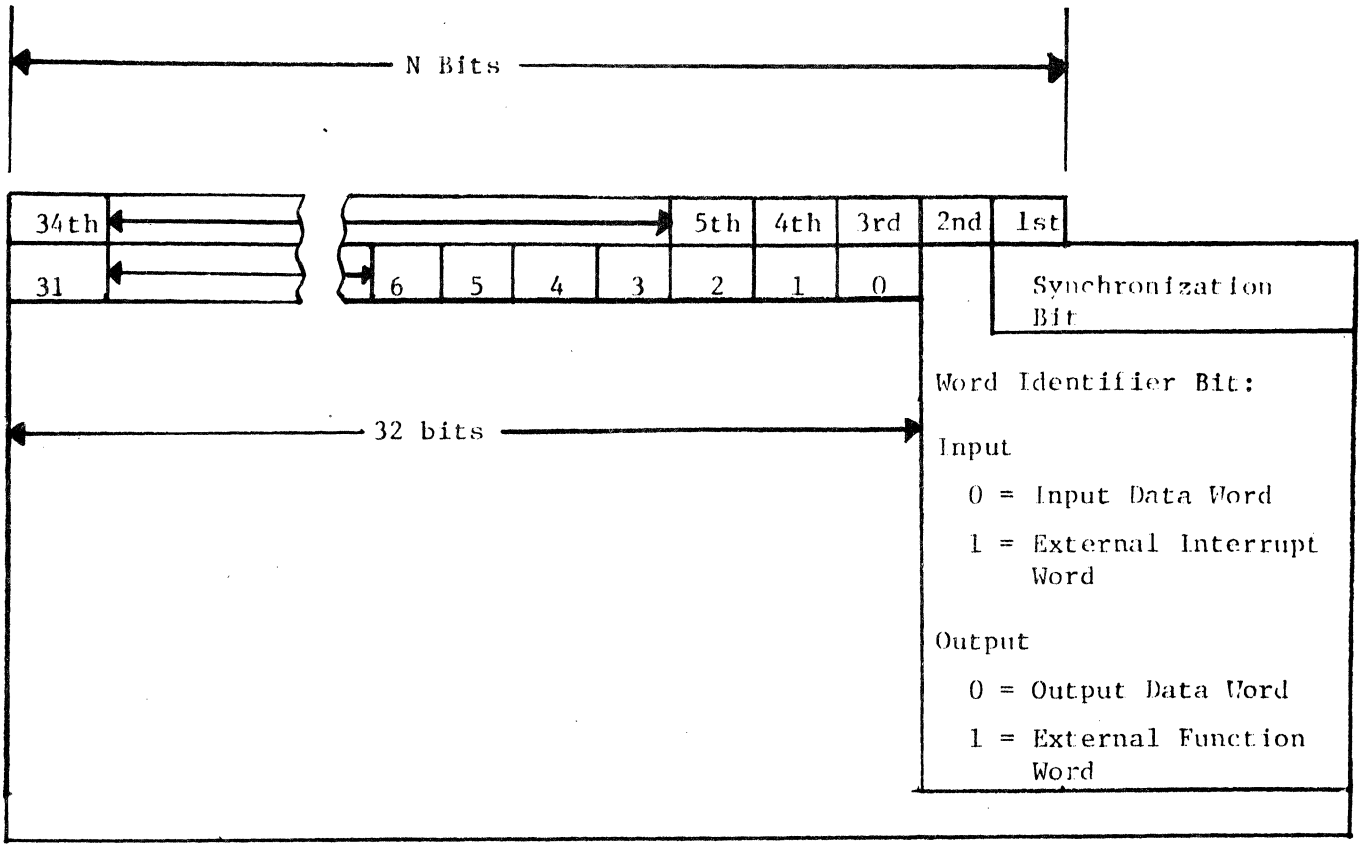
3	2	1	
		Synchronization Bit	
0	0	=	Not Ready
0	1	=	Output Data Request (ODR)
1	0	=	External Function Request (EFR)
1	1	=	ODR and EFR

c. Output Request Control Frame (ORCF), Peripheral-to-DPS

3	2	1	
		Synchronization Bit	
0	0	=	Not Used
0	1	=	Output Data Enable (ODE)
1	0	=	External Function Enable (EFE)
1	1	=	ODE and EFE

d. Output Enable Control Frame (OECF), DPS-to-Peripheral

Figure 3-51. 3-Bit Control Frames



34th bit = last bit in data word and last bit to be transmitted.

Figure 3-52. NTDS Serial I/O Word Format

equipment. The peripheral equipment responds with an Output Request Control Frame (ORCF), with both output data and external function bits set. If the IOC has an active output buffer corresponding to its OECF, it sends, in accordance with internal priorities, a 32-bit output or external function word to the peripheral equipment. If the IOC does not have an active output buffer corresponding to its OECF, another OECF from the IOC and another ORCF sequence from the peripheral equipment occurs. All output control frames and output data are transferred on the output channel cable. Each 32-bit output data word transferred is accompanied by an OECF and an ORCF.

3-162. The peripheral equipment continually interrogates the IOC on each NTDS serial input channel by sending Input Request Control Frames (IRCF), with both input data request and external interrupt bits set, to the IOC. The IOC responds with an Input Enable Control Frame (IECF). If the peripheral equipment is ready with its data, a 32-bit input or interrupt word is sent to the IOC. If the peripheral equipment does not have data corresponding with the IECF from the IOC, another IRCF from the peripheral equipment and another IECF sequence from the IOC occurs. All input control frames and input data are transferred on the input channel cable. Each 32-bit input data word transferred is accompanied by an IRCF and an IECF.

3-163. Serial I/O Timing. I/O operation timing is provided by the DPS Master Clock and developed into timing signals T1-T4 in the IOC timing circuitry, or timing is provided from an external source. To assure reliable data transfers, the following

signal timing restrictions (plus cable propagation time of 1.5 nanoseconds/foot) are required of the equipment. Unless otherwise specified the timing requirements are measured from the leading edge of the synchronization pulse of one event to the leading edge of the synchronization pulse of the succeeding event. Each of the following timing requirements refers to the timing on each individual cable.

1) Consecutive Control Frames: Time between consecutive control frames transmitted by the same equipment must not be less than 18.5 microseconds plus cable propagation time.

2) OECF to ORCF: Time between computer transmitting an OECF and receiving the ORCF from the peripheral equipment must not be greater than 17 microseconds plus cable propagation time.

3) Enable-To-Request Time Exceeded: If this time exceeds 17 microseconds plus cable propagation time, the processor must again send the OECF if data transfer is still required.

4) ORCF to Data: There is no time limit between the time the processor receives the ORCF and the time it transmits the requested output data word.

5) Output to Sync: Time between the trailing edge of the last bit of an output word and the next sync bit must be not less than 200 nanoseconds.

6) IRCF to IECF: Time between receiving an IRCF and transmitting an IECF must not be greater than 15.0 microseconds.

7) IECF to Input: Peripheral equipment must transmit an input word within 15.0 microseconds of receiving an IECF. The time between transmission of an IECF and receiving an input word must not be greater than 17.0 microseconds plus cable propagation time.

8) Input to Sync: Time between the trailing edge of the last bit of an input word to the next IRCF bit must not be less than 200 nanoseconds.

9) Transmitter Receiver Pair: Except when the transmitter is transmitting, the receiver is capable of receiving signals at all times.

3-164. The output timing characteristics for the NTDS serial I/O are listed below.

1) If the peripheral equipment does not respond to the OECF by sending an ORCF, the DPS sends an OECF every 30 microseconds nominal.

2) If the peripheral equipment responds to each OECF with a not ready ORCF, both the OECF and the ORCF occur within 3 microseconds nominal.

3) If the DPS is to send an external function with force, it begins to transfer the data word within 30 μsec nominal after the OECF even if the peripheral equipment did not respond with the ORCF.

4) If normal data transfers occur, the DPS transfers each 32-bit word, along with the required OECF and ORCF, every 7 μsec nominal for an effective data transfer rate of 150,000 words/second (32-bit words).

3-165. Figure 3-53 provides the bi-polar pulse timing and characteristics at the transmitter end for the NTDS serial interface. Information is transmitted via bi-polar, phase modulated, serial pulse trains. The first pulse (sync pulse) of the serial pulse train is a phase zero degree pulse (binary one) and is a high polarity followed by a low polarity. A binary zero pulse is a phase 180 degree pulse (low followed by high). During the time when control frames or data and control words are not being transmitted, no signal is present.

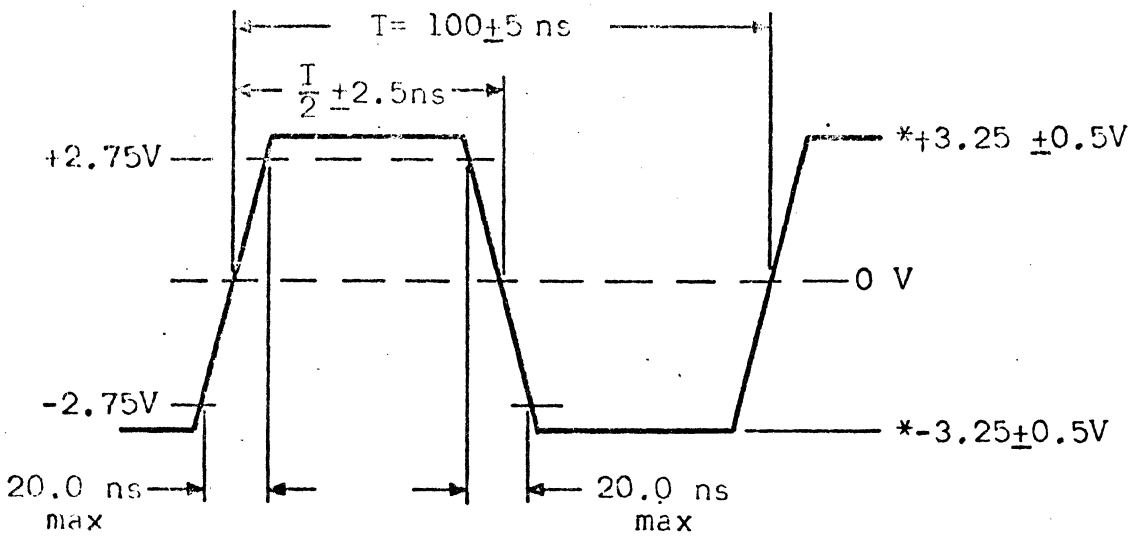


Figure 3-53. Bi-polar Pulse Characteristics

3-166. POWER SUPPLY. The power supply converts the ac input power into the filtered and regulated dc voltages required by the DPS logic and memory circuits. It provides protection against input overvoltage and output overcurrent conditions, and provides master clear and power interrupt status signals to the processor when input or output voltages are out of tolerance. The power supply occupies its own chassis at the bottom rear of the cabinet. Figure 3-54 provides a functional block diagram, and table 3-32 lists the characteristics of the power supply. There are six power supply schematic diagrams, representing six optional input power configurations. These diagrams are in Chapter 9 (Volume II) of this manual; the diagram number for each input option appears in table 3-32. The schematic diagram for the control card used in all power supplies is 7119455. The major functional elements of the power supply are an EMI filter (on 400 Hz options only), an input power transformer (on three phase options only), a rectifier circuit, a switching regulator, a dc-dc converter, power status circuits, and overvoltage/overcurrent protective circuits.

3-167. EMI Filter. An inductor-capacitor filter network is included in each ac power input line on 400 Hz input power options to minimize introduction of external power line noise into the supply and to attenuate transmission of internally generated switching noise. A typical filter network appears on schematic diagram number 7101840, and comprises chokes A3 L1-L9, and capacitors A3 C1-C6.

3-168. Input Power Transformers and Rectifiers. Input transformers and rectifiers both vary according to the input power options as follows.

3-169. Power supply options having a three-phase input power configuration employ an input power transformer with either a delta or wye primary connection. The transformer secondary outputs are rectified by a three-phase full-wave bridge to provide the nominal +150 Vdc required by the switching regulator. An inductor-capacitor averaging filter follows the rectifier to smooth the dc input to the switching regulator. Referring to schematic diagram number 7101840 as an example, the ac input from EMI filter A3 is applied to the delta-connected primary of T1. The T1 secondary outputs are rectified by the full-wave bridge comprised of A7CR14-CR15-CR16, and the resulting dc smoothed by series inductor A1L1, and shunt capacitor A1C1.

3-170. Power supply options having a single-phase input power configuration rectify the input power directly following the EMI filter without use of an input transformer. Referring to the schematic diagram, number 7101875 as an example, the ac input power is applied to rectifier A7CR14 via A8R1 which limits the starting current inrush to protect the power switch. Approximately 50 milliseconds after power application, relay A8K1 closes to effectively remove A8R1 from the circuit. The rectified output from A7CR14 is filtered by shunt capacitor A1C1 and the resulting dc furnished to the switching regulator.

3-171. Internal Power. A +15V bootstrap power supply is included in all power supply configurations to furnish initial operating power to the control circuits during start-up. After start-up, operating power is derived from the dc to dc converter outputs. +5V power is provided for the integrated circuits in the power supply control circuitry.

3-172. The bootstrap power supply consists of a transformer, rectifier, and regulator. Referring to schematic diagram number 7101840, one leg of the three-phase power input is applied to transformer A4T1. The transformer secondary output is rectified by full-wave bridge A6CR1 located on the control card, schematic

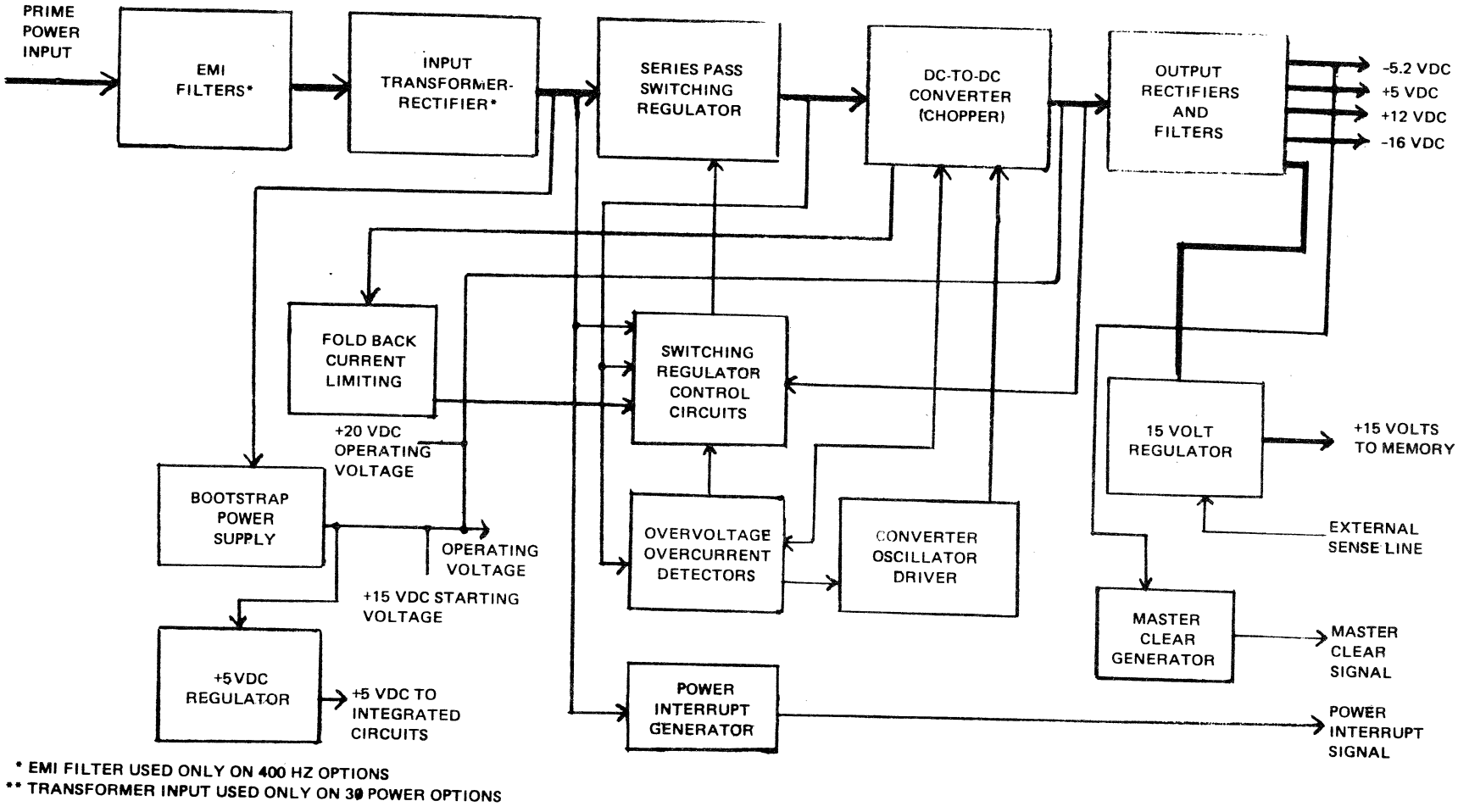


Figure 3-54. Power Supply Overall Functional Block Diagram

Table 3-32. Power Supply Characteristics

ITEM	CHARACTERISTIC/PARAMETER	
Input Power		
- Option 1	115 Vac ±5%, line-to-line, 400 Hz 3Ø delta input (schematic diagram No. 7101840)	
- Option 2	115 Vac ±7%, 400 Hz, 1Ø input (schematic diagram No. 7101875)	
- Option 3	115 Vac ±5%, line-to-line, 60 Hz, 3Ø delta input (schematic diagram No. 7101880)	
- Option 4	115 Vac ±7%, 60 Hz, 1Ø input (schematic diagram No. 7101885)	
- Option 5	115 Vac ±5%, line-to-neutral, 60 Hz, 3Ø wye input (schematic diagram No. 7101990)	
- Option 6	115 Vac ±5%, line-to-neutral, 400 Hz, 3Ø wye input (schematic diagram No. 7101995)	
Total Power Requirement	850 Watts nominal	
Power Supply Power Dissipation	250 Watts nominal	
Output Power	Tolerance	Maximum Load
-5.2 Vdc	±5%	10.0 Amperes
-5.0 Vdc	±5%	1.0 Amperes
+5 Vdc Memory	±5%	18.5 Amperes
+5 Vdc Processor	±5%	42.0 Amperes
+12 Vdc	±5%	1.0 Amperes
+15 Vdc	±2%	12.0 Amperes
-16 Vdc	±2%	2.4 Amperes

diagram number 7119455. The rectified voltage is regulated to +15 Vdc by series-pass transistor A7Q2. Zener diode A6CR6 provides the nominal 15 volt reference for the base of A7Q2. After the supply is in operation, the bootstrap voltage is overridden by the nominal 20 volt operating voltage derived from dc-dc converter output winding A5T2-A29-A31. The output is rectified by diodes A6CR7 and A6CR8, and filtered by series resistor A6R6 and shunt capacitor A6C12. In addition to being used for control circuit operation, this voltage is sensed by the feedback voltage regulator to detect output voltage errors.

3-173. The internal +5 Vdc power furnished to the integrated circuits is derived from the +20 Vdc bus by integrated regulator circuit A7U1. The +20 Vdc input is applied to A7U1-Pin 1. The +50 Vdc output appears at A7U1 Pin 2, and is filtered by capacitor A6C11.

3-174. Switching Regulator Control Circuits. The switching regulator control circuits develop and control the drive supplied to the switching regulator. These circuits consist of an oscillator pulse width modulator, toggle flip-flop, feed forward and feedback voltage sensors, and a driver circuit. They appear in the control card schematic diagram, number 7119455, and are shown in the simplified block diagram, figure 3-55.

3-175. The oscillator is composed of cross-coupled one-shot circuits A6U1A and A6U1B. It produces a 22 KHz single-phase square wave output. The oscillator waveform is shown in figure 3-56. The oscillator output appearing at A6U1B-Pin 9 is applied to toggle flip-flop A6U8-Pin 12 and from A6U1B-Pin 16 to pulse width modulator A6U7-Pin 16. J-K toggle flip-flop A6U8 converts the single phase oscillator signal to a two-phase signal for the pulse width modulator control circuit and the switching regulator driver. The toggle flip-flop outputs appearing at A6U8-Pins 6 and 8 are applied to pulse width modulator A6U9-Pins 4 and 9.

3-176. Voltage comparator A6U6 provides feedback voltage regulation which corrects for dc-dc converter output voltage errors. The comparator senses voltage errors on the +20 Vdc operating bus and responds by providing a correction voltage to A6U1A-B to increase or decrease the oscillator frequency. A6U6 samples the +120 Vdc bus via the voltage divider comprised of A6R23-R39-R31, and output voltage control potentiometer A6R38. The voltage sample is compared with an internally developed reference voltage, with the resultant error voltage supplied to the oscillator as a frequency control bias voltage. This voltage appears at A6U6-Pin 10 and is applied to the oscillator via A6CR19 and A6R2.

3-177. A pulse width modulator circuit provides feed-forward regulation that corrects for input voltage errors. It consists of pulse width modulator control one-shot A6U7 and pulse-width modulator gate A6U9. A voltage sample from the +150 Vdc switching regulator input is dropped to a lower level by resistors A6R1 and R5 and zener diode A6CR9, and is applied as a control bias to one-shot A6U7-Pin 14. Variations in the sampled voltage cause corresponding variations in the width of the output pulse produced by A6U7. This variable width pulse is applied to pulse width modulator gate A6U9-Pins 5 and 10, where it is "anded" with the constant pulse width oscillator signal to produce the pulse-width modulated output. Figure 3-57 shows the pulse width modulator waveform. The A6U9 output can also be inhibited by an overcurrent or overvoltage shut-down signal as explained in paragraphs 3-185 and 3-186.

3-178. The pulse width modulator applies an alternating base drive to switching regulator driver transistors A6Q3 and Q5 via current limiting resistors A6R25

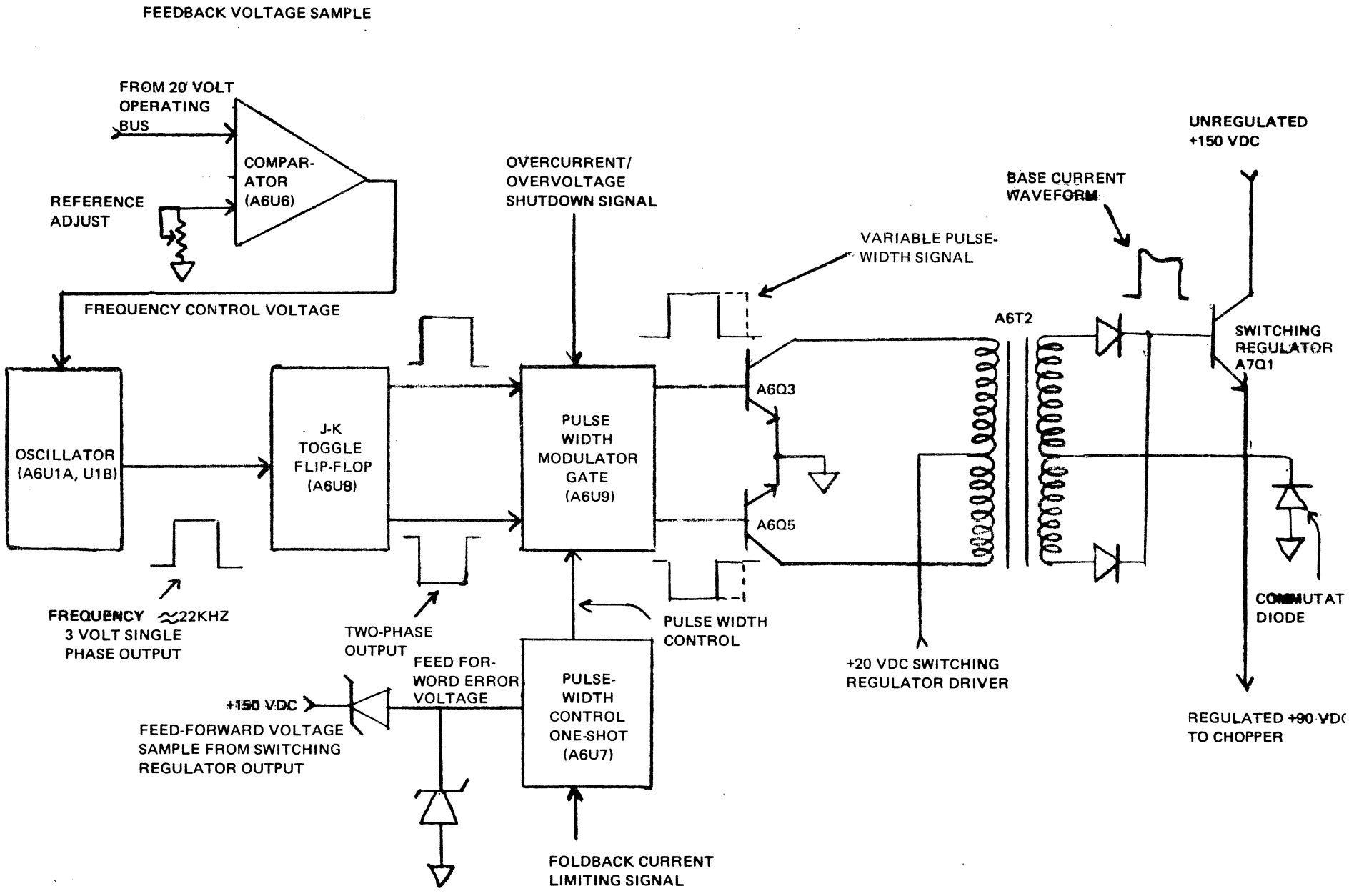
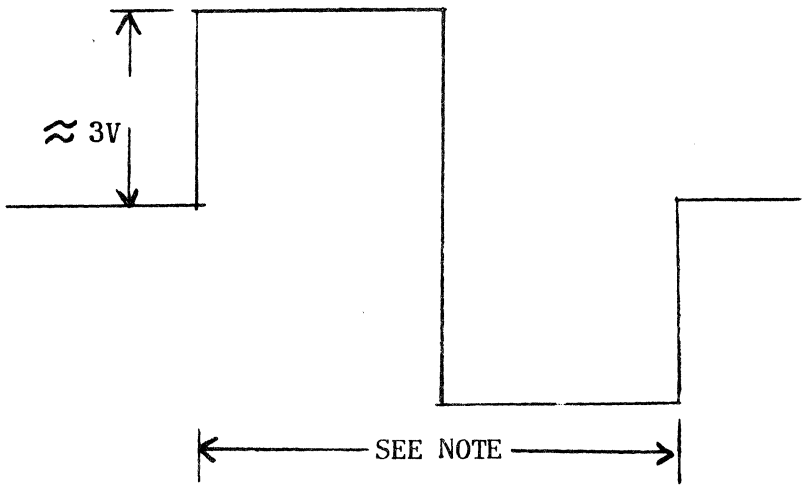


Figure 3-55. Switching Regulator Simplified Block Diagram



NOTE: NOMINAL OSCILLATOR FREQUENCY IS 22 KHz MEASURED AT CIRCUIT A6U1B-PIN 10.

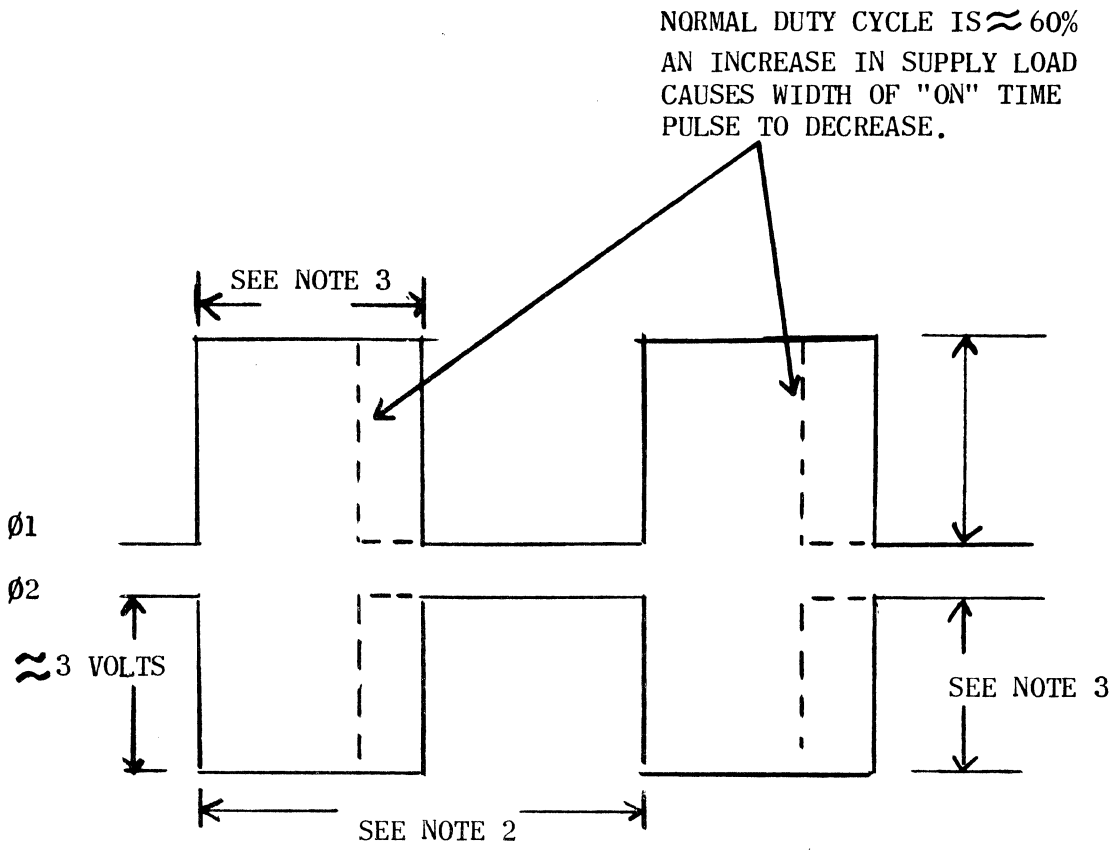
Figure 3-56. Switching Regulator Oscillator Waveform

and R34. Q6Q3 and Q5 are coupled to the base of switching regulator transistor A7Q1 (schematic diagram 710840) via transformer A6T2. Figure 3-58 shows the waveform of this base drive current.

3-179. Series-pass transistor A7Q1 functions as a switching mode voltage regulator. The signal driving it is both pulse width modulated and varied in frequency to control its duty cycle. The +150 Vdc output from the prime power rectifier is applied to the collector and a regulated dc output of approximately +90 volts is derived from the emitter. An inductor-capacitor averaging filter consisting of choke L1 and capacitors A1C2 and A1C3 follows the transistor to filter the dc output. Commutating diode A7CR5, connected across the transistor emitter, bypasses negative voltage excursions occuring during transistor off times as a result of the action of choke L1.

3-180. DC to DC Converter. A dc to dc converter produces the power supply output voltages from the regulated +90 Vdc. The converter consists of an oscillator-driver (chopper) circuit, a transformer, and output rectifiers and filters.

3-181. The converter drive signal is developed by an 11 KHz oscillator comprised of cross-coupled one-shots A6U2A and A2B, shown in schematic diagram 7119455, and in the simplified block diagram, figure 3-59. The oscillator output has a waveform as shown in figure 3-60. It is applied to J-K flip-flop A6U3-Pin 12, which toggles to convert the single-phase oscillator output to a two-phase output appearing at pins 6 and 8. The output from the J-K flip-flop drives shut-down control Gate A6U4, which inhibits the converter drive signal during an overcurrent or overvoltage

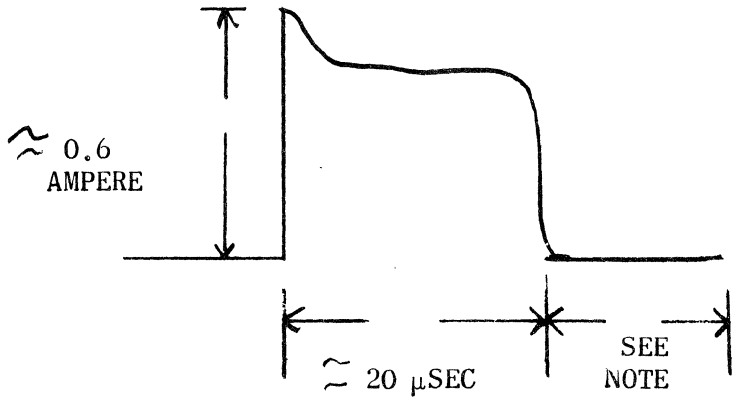


NOTES:
1) PULSES ARE MEASURED AT PULSE WIDTH CONTROL GATES, PINS 6 AND 8 OF INTEGRATED CIRCUIT A6U9.

2) OPERATING FREQUENCY UNDER NORMAL LOAD IS APPROXIMATELY 22 KHz.

3) WAVEFORMS FOR BOTH PHASES SHOULD BE NEARLY SYMMETRICAL IN BOTH AMPLITUDE AND WIDTH.

Figure 3-57. Pulse Width Modulator Voltage Waveform



NOTE: THE WAVEFORM IS MEASURED AT THE BASE OF A7Q1 WITH A CURRENT PROBE. THE DUTY CYCLE UNDER NORMAL LOAD IS APPROXIMATELY 60%.

Figure 3-58. Switching Regulator Base Drive Current Waveform

condition, as explained in paragraphs 3-185 and 3-186. The A6U4 output, pins 6 and 8, is applied to the bases of chopper driver transistors A6Q1 and Q2 via resistors A6R7 and R13. The chopper driver transistors provide the alternating drive signals to chopper transistors A7Q5 and Q6 via transformer A6T1. Figure 3-61 shows the chopper transistor collector voltage waveform.

3-182. The nominal +90 Vdc output from the switching regulator is changed to an alternating voltage via the chopper circuit. This enables voltage conversion via a transformer and provides isolation from the ac power source. Referring to schematic diagram number 7101840, the dc input is switched via transistor pair A7Q5-A7Q6 which are coupled in push-pull parallel to the primaries of transformers A5T1 and A5T2. The alternating drive signals applied to the bases of the transistors are constant in both frequency and pulse width and provide 100% duty cycle operation. An emitter resistor, A4R1, is used with the transistor pair to balance the transistor currents and provide a means of detecting overcurrents by sensing the voltage drop across the resistor. The output voltages are determined by the transformer primary-to-secondary turns ratios. Each output voltage from the chopper transformer secondaries is full-wave rectified and the resulting dc filtered by an inductor-capacitor averaging filter. As a typical example, the +5 Vdc memory output, schematic diagram 7101840, is produced from secondary windings A5B8-C5-B14 and rectified by A7CR8 and CR9, then is filtered by series inductor A2L2 and shunt capacitors A2C5 through C8. After filtering, the dc voltage outputs are supplied to the DPS logic and memory circuits.

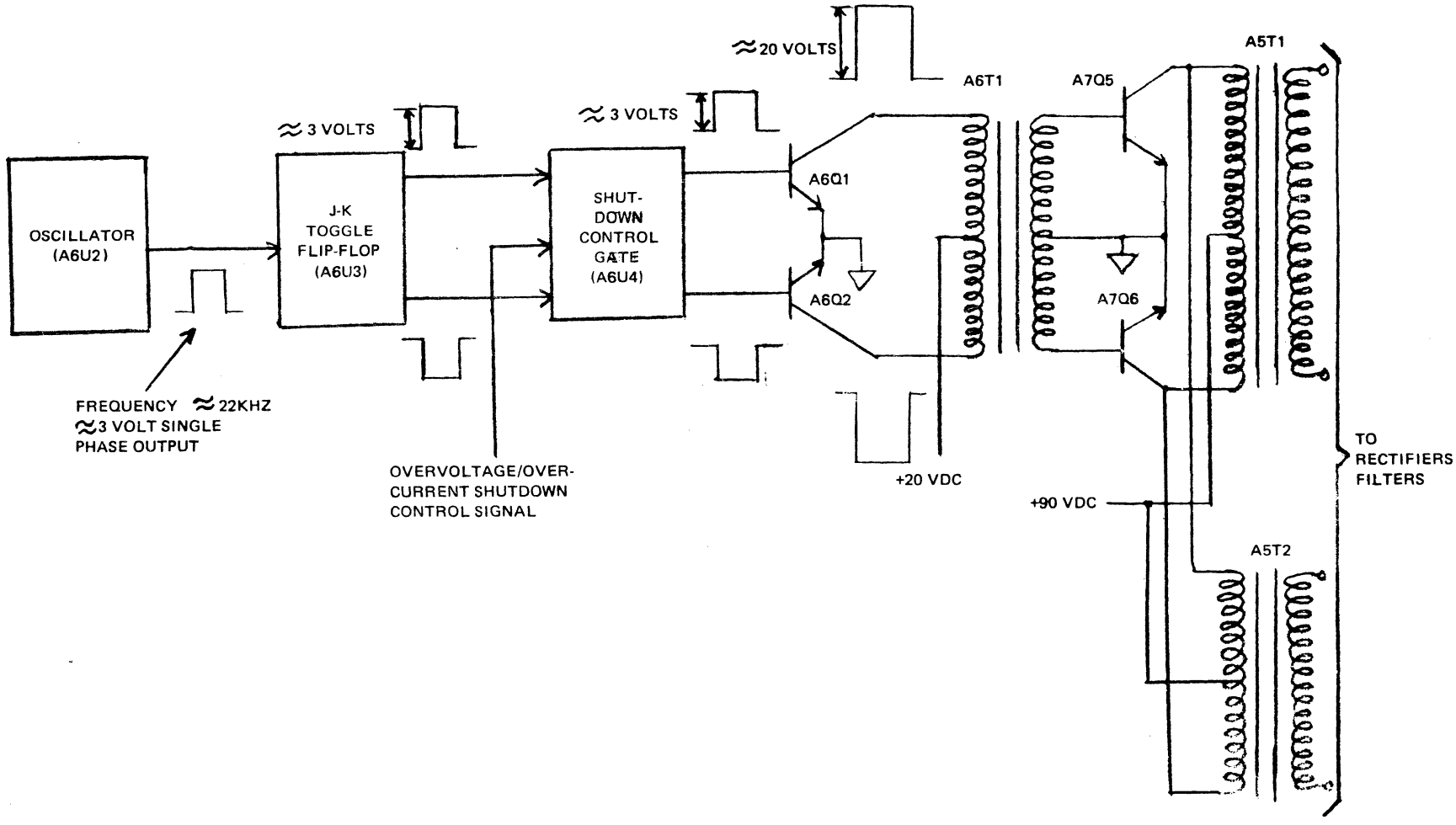
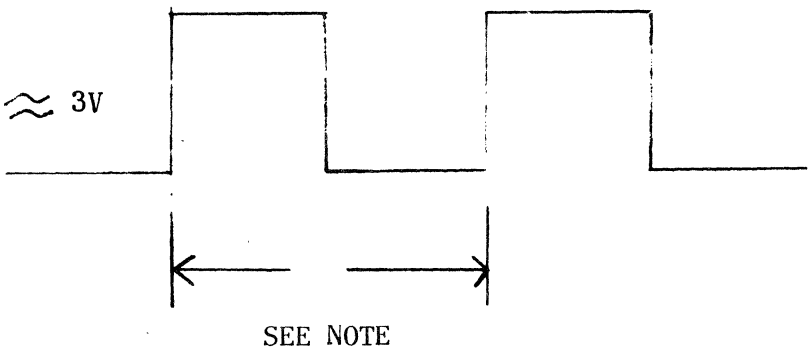
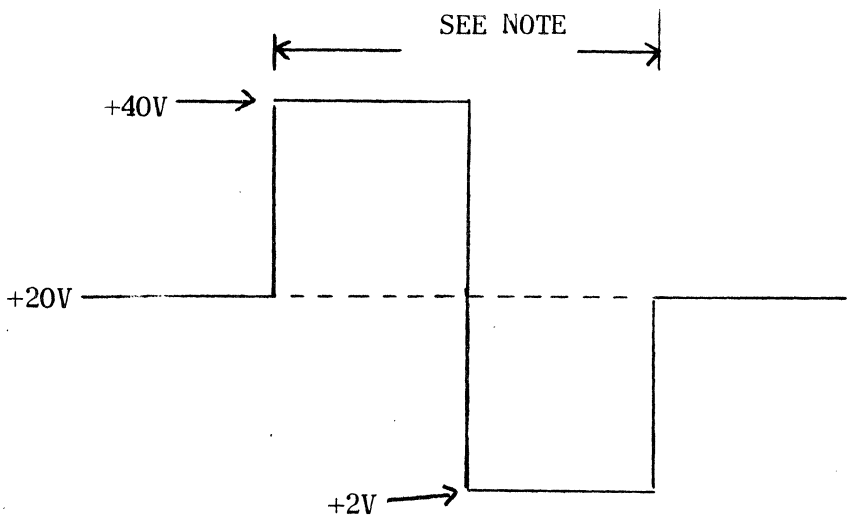


Figure 3-59. Converter Oscillator-Driver and Chopper Circuit Simplified Block Diagram



NOTE: WAVEFORM MEASURES AT A6U2B, PIN 9. FREQUENCY IS ≈ 11 KHz.

Figure 3-60. Chopper Oscillator Voltage Waveform

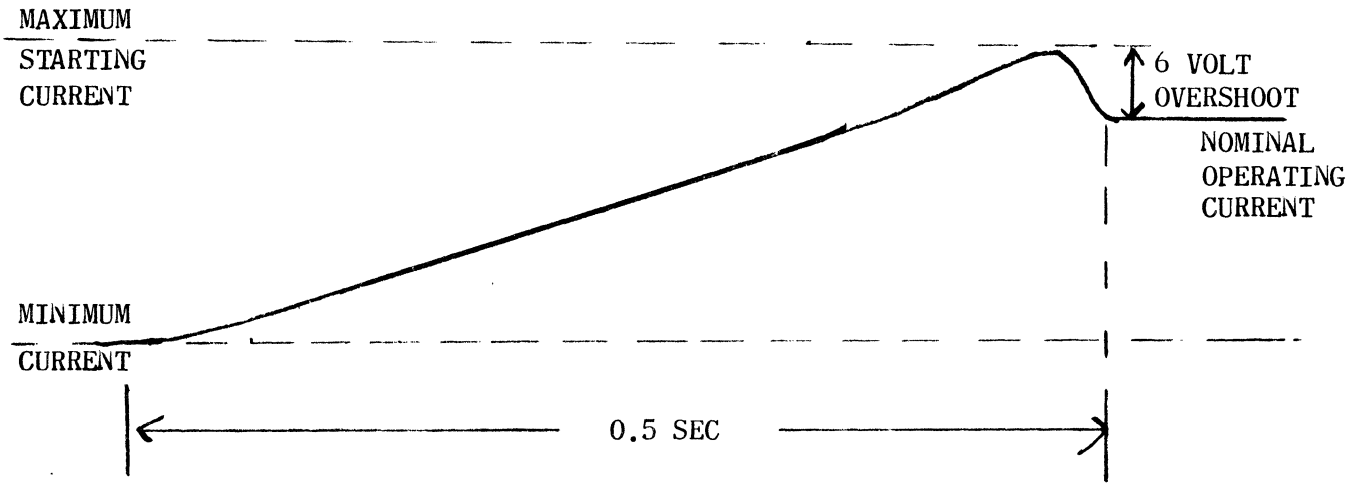


NOTE: WAVEFORM MEASURED AT COLLECTORS OF TRANSISTORS A7Q3 AND A7Q5. NOMINAL FREQUENCY IS 11 KHz.

Figure 3-61. Chopper Transistor Voltage Waveform

3-183. Overcurrent/Overvoltage Sensors. The overcurrent/overvoltage sensors consist of a foldback current limiting circuit, an overcurrent shut-down circuit and an overvoltage shut-down circuit. These circuits appear in the control card schematic diagram number 7119455.

3-184. The foldback current limiting circuit limits the maximum inrush current through the switching regulator during start-up. Figure 3-62 shows the typical starting current ramp and resulting overshoot when power is initially applied and the foldback circuit is operating. The voltage developed across chopper transistor emitter resistor A4R1 (schematic diagram 7101840) is applied to pins 4 and 6 of comparator A6U10 on the control card (schematic diagram 7119455). A6U10 is connected to operate as a trigger, and when the applied voltage reaches a critical value, approximating a 50% overload, the output appearing at pin 9 switches from a low to a high level. This signal is applied to inverter A6U11. The output of A6U11 at pin 8 is then low, and is applied to pulse width modulator A6U7-Pin 13 as an inhibit signal. Thus, the pulse width modulator is alternately inhibited and released during the starting phase to limit the duty cycle of the switching regulator until the chopper current requirement stabilizes.



NOTE: CURRENT MEASURED WITH CURRENT PROBE AT COLLECTOR OF SWITCHING REGULATOR TRANSISTOR A7Q1.

Figure 3-62. Input Starting Current Ramp

3-185. An overcurrent circuit operates to shut down the power supply by inhibiting chopper and switching regulator drive signals if the supply load exceeds approximately 200% of maximum rates value. The overcurrent condition is detected by a sense line monitoring the net average of chopper transistor collector voltages at the junction of resistors A6R15 and A6R79. If the chopper circuit is overloaded, these voltages will become unbalanced, due to one or the other chopper transistor dropping out of saturated operation. When the overload is sufficient to cause this voltage to rise approximately 8 volts, the voltage rise on the sense line will set flip-flop A6Q7-Q8 via zener diode A6CR33 and the base of A6Q7. The flip-flop output then appears as a low at pins 2 and 12 of pulse width modulator control gate A6U9 and pins 5 and 10 of chopper circuit shutdown control gate A6U4. With these gates inhibited, drive signals are effectively removed from the switching regulator and chopper circuit, thus stopping power supply operation. The flip-flop will remain set until input power is temporarily removed, permitting it to reset.

3-186. An overvoltage sensing circuit utilizing zener diode A6CR25 monitors the +90 Vdc switching regulator output and causes flip-flop A6Q7-Q8 to set if this voltage rises to a value between 105 and 115 volts, due to a long-term input power transient. The effect of setting the flip-flop is identical to that described for an overcurrent condition, paragraph 3-185.

3-187. Power Interrupt Generator. A power interrupt generator samples the +150 Vdc input voltage bus and generates a power interrupt signal if the voltage falls to approximately +97 Vdc. This signal warns the processor of an incipient power failure. The circuit, shown in schematic diagram 7119455, is comprised of voltage comparator A6U12, solid-state relay A6F1, and a driver transistor contained in circuit A6Q9. A voltage sample from the +150 Vdc bus is applied to pin 5 of A6U12 via the wiper arm of adjustment potentiometer A6R55. The circuit output drives solid-state relay A6K1. The relay output drives the output transistor contained in A6Q9, pins 8, 9, 10. The output signal is normally high (+5 volts) and switches low (+0.25 volts) when active.

3-188. Master Clear Generator. The master clear generator, shown in schematic diagram 7119455, senses the +5 Vdc supply output and generates a master clear signal if this output falls to +4.7 Vdc or less. A voltage sample from the +5 Vdc bus is applied to voltage sensor circuit A6U13-Pin 5 via the wiper arm of adjustment potentiometer A6R59. When the voltage drops below the set tolerance the circuit output, pin 3, drives a dc-coupled transistor pair, circuit A6Q9-Pins 1, 2, 3, and 5, 6, 7, which provides the master clear output signal. The signal is normally high and switches low in the active state.

3-189. 15 Vdc Regulator. The +15 Vdc Memory voltage is regulated within $\pm$ 2% by a linear series-pass regulator. The regulator consists of sensor-comparator circuit A6U5, schematic diagram 7119455, and series-pass control transistors A7Q3 and Q4, schematic diagram 7101840. Circuit A6U5 compares a sample of the +15 volt output with an internal reference voltage and provides an analog control signal at pin 10 which drives the bases of A7Q3 and Q4. The control signal varies in response to output voltage errors. The regulated output appears at the emitters of A7Q3 and Q4. An external sense line connected to A6U5-Pin 4 via A6R30 and adjustment potentiometer A6R29 permits the regulator to compensate for temperature within the core memory via a thermistor located in the core memory stack.

3-190. POWER DISTRIBUTION. The power distribution schematic diagram, figures 000A and B in Chapter 9,shows ac and dc power routing within the DPS and provides terminal, switch, indicator and relay connection data.

3-191. OPERATIONAL DESCRIPTION.

3-192. The following paragraphs are an operational description of the DPS. The description covers the joint operation of the hardware and firmware (microprogram). The DPS has a master clock that provides two pulses: a phase early (ϕ_e) and a phase normal (ϕ_n) pulse. These two timing pulses and the program of micro instructions are used to execute macroinstructions and to process I/O transfers and interrupts. The micro program consists of many short subroutines that provide control to execute each macroinstruction or control function. Thus, the micro program replaces hardware generated timing sequences and discrete control signals. The following paragraphs describe the basic sequences.

3-193. MACROINSTRUCTION EMULATION. The macroinstruction emulation sequence is the basic sequence that determines the operation to be performed next. Figure 3-63 is a flowchart of the macroinstruction emulation sequence. This sequence starts with an Emulate Start microinstruction. (Most micro program subroutines end with this instruction, thus returning to this sequence.) At this time, I/O requests and micro interrupt requests are honored in priority order. If a request is present, a hardware generated address is loaded into the micro P register to branch to an I/O transfer or micro interrupt subroutine (see table 3-33). (The I/O transfer sequence is described in paragraph 3-194 and micro interrupt sequence is described in paragraph 3-197.) When a request is not present, the next step is to check the Next Instruction Resident (NIR) bit. NIR indicates that a memory request for the next macroinstruction had been made previously. If NIR is not set, a memory request is initiated to fetch the next instruction. Hardware generated address 274_8 is loaded into the micro P register to branch to the instruction read subroutine. The first microinstruction of the subroutine transfers the contents of the memory data register (MDR) to the instruction register (IR), however, if the "Data Available" signal has not been received from memory, the master clock is stopped until the signal is received. (The master clock is disabled when there is a memory reference and the S-field bits 0 and 1 equal 11_2.) In this case, the source was MDR (S = 0011). After the signal is received, the instruction is gated into IR. The next microinstruction in the subroutine is an Emulate Branch 1. I/O requests present at this time will be honored. With no I/O request present, the emulator control word (ECW) bits 9 through 12 are interrogated. If ECW I (bit 11) equals 1, a hardware generated address is loaded into the micro P register to branch to an Interim sequence (see table 3-34). The Interim sequence is used for instructions with RK or RX formats. The end result of the Interim sequence is to place the operand in A6. The Interim sequence ends with an Emulate Branch 2 microinstruction. I/O requests present at this time will be honored. When no I/O request is present, ECW is checked for overlap (ECW bit 10 = 1 and bit 12 = 0) and unary (ECW bit 9 = 0 and bit 12 = 0). If overlap, a memory request is initiated to fetch the next instruction. If unary instruction, the ECW pointer is modified by the m-field. The ECW pointer (bits 0-8) and IR bit 15 are gated to the micro P register to branch to the macroinstruction subroutine. IR bit 15 increases the pointer addressing capability to 1777_8; thus, subroutines for instructions 40 through 77 are at micro program addresses above 1000_8. If the macroinstruction is illegal, the PROG FAULT indicator is set and the Class II interrupt is processed. If Class II interrupts are locked out, the computer is placed in the console mode (Prog Run flip-flop cleared). For legal instructions, the macroinstruction subroutine is executed. Long subroutines allow I/O transfers at specified intervals. The subroutine ends with an Emulate Start microinstruction which starts another emulation sequence.

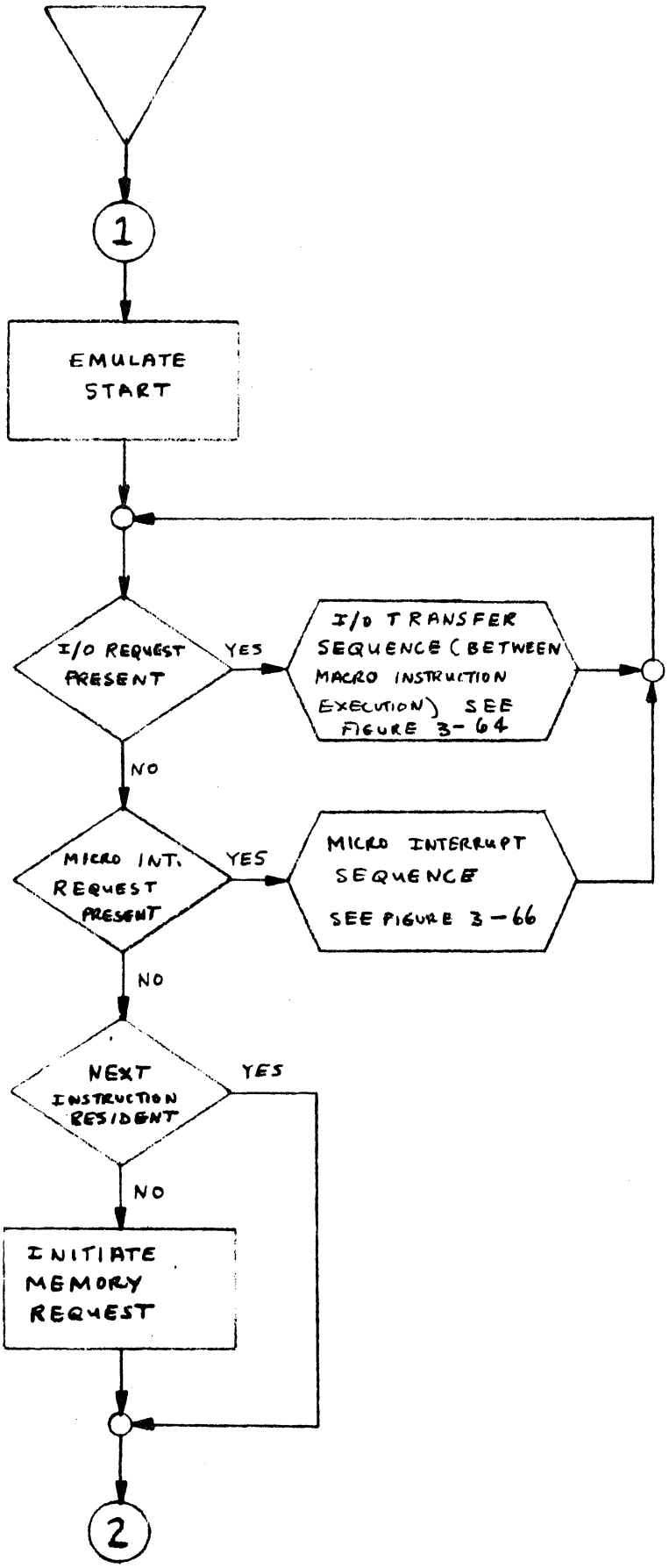


Figure 3-63. Macro Instruction Emulation

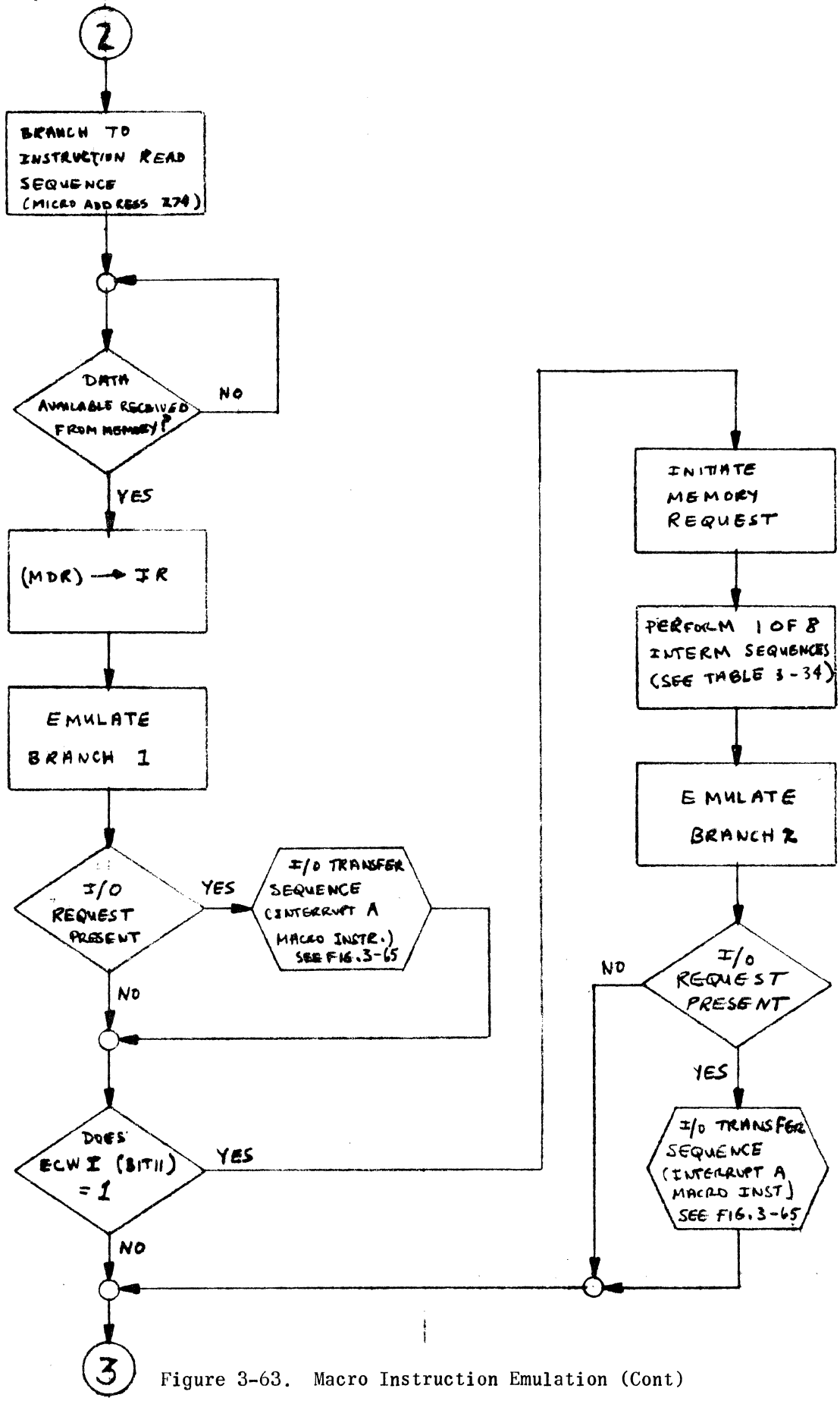


Figure 3-63. Macro Instruction Emulation (Cont)

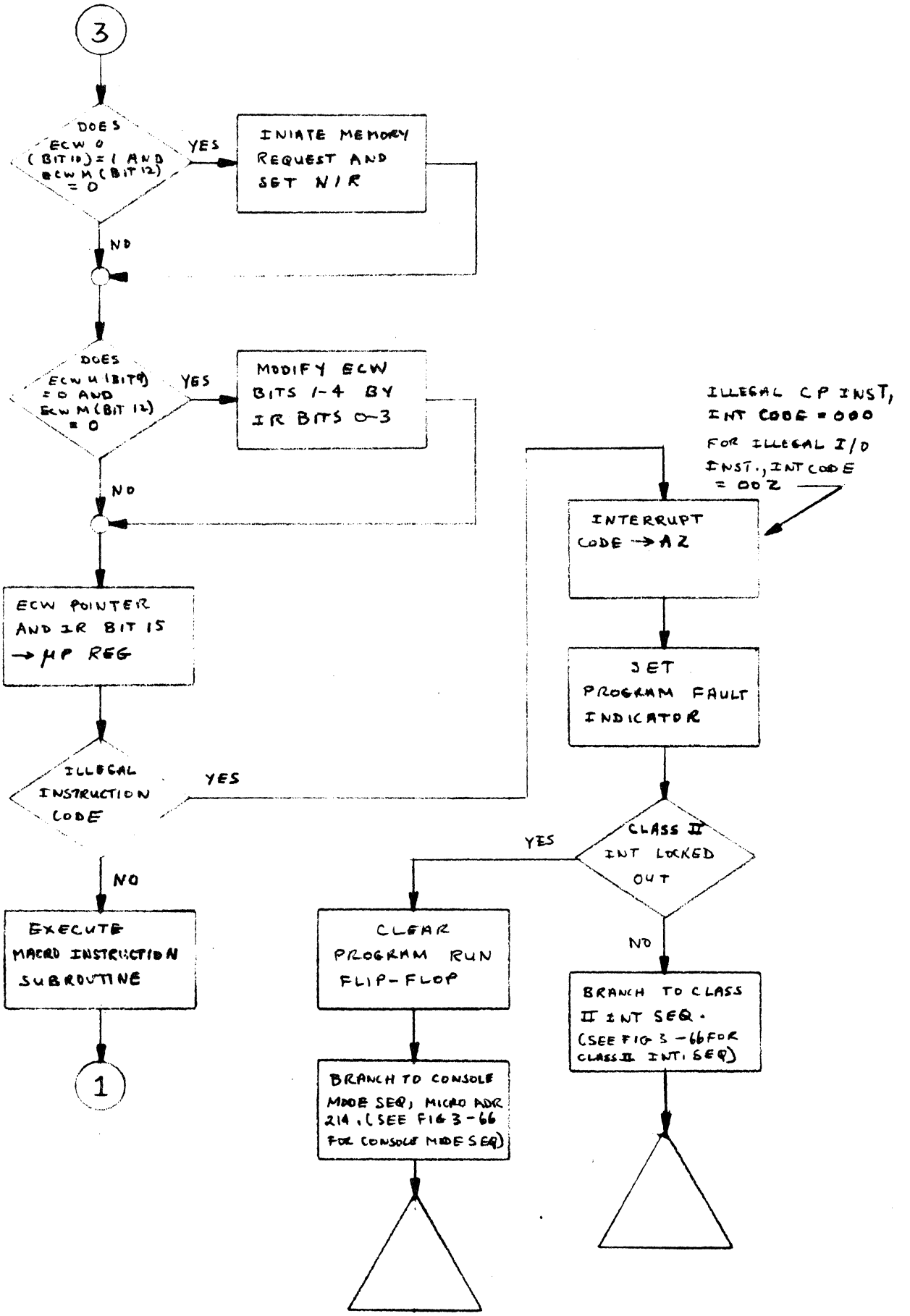


Figure 3-63. Macro Instruction Emulation (Cont)

Table 3-33. Micro Branch Conditions for Emulate Start Operation

PRIORITY	MICRO BRANCH CONDITIONS	ADDRESS LOADED IN MICRO P REG (OCTAL)	NAME OF SUBROUTINE ENTERED
1	I/O Request		
	Output or External Function	320	I/O Output Pass Gt 1
	Input or External Interrupt	300	I/O Input Pass GT 1
2	Return Interrupt	200	Return
3	Load Interrupt	204	Bootstrap Load Switch Function
4	I/O Chain Interrupt	210	Chain Inst Read
5	Not Run Interrupt	214	Run (BAR)
6	Class I or II Interrupt	220	Class I or II
7	Class III Interrupt	230	Class III
8	None of the above	274	Instruction Read

Table 3-34. Micro Branch Conditions for Interim Sequences

INTERIM CONDITIONS	ADDRESS LOADED IN MICRO P REG (OCTAL)	NAME OF SUBROUTINE ENTERED
INDIRECT ADDRESSING·BYTE·MODIFY	340	Indirect Byte Modify
INDIRECT ADDRESSING·BYTE·$\overline{\text{MODIFY}}$	344	Indirect Byte No Mod
INDIRECT ADDRESSING·$\overline{\text{BYTE}}$·MODIFY	350	Indirect Word Modify
INDIRECT ADDRESSING·$\overline{\text{BYTE}}$·$\overline{\text{MODIFY}}$	354	Indirect Word No Mod
$\overline{\text{INDIRECT ADDRESSING}}$·BYTE·MODIFY	360	Normal Byte Modify
$\overline{\text{INDIRECT ADDRESSING}}$·BYTE·$\overline{\text{MODIFY}}$	364	Normal Byte No Mod
$\overline{\text{INDIRECT ADDRESSING}}$·$\overline{\text{BYTE}}$·MODIFY	370	Normal Word Modify
$\overline{\text{INDIRECT ADDRESSING}}$·$\overline{\text{BYTE}}$·$\overline{\text{MODIFY}}$	374	Normal Word No Mod

3-194. I/O TRANSFERS. I/O transfers can occur between macroinstruction execution or can interrupt macroinstruction execution at specified intervals. The two types of transfers are described in the following paragraphs.

3-195. I/O Transfers Between Macroinstructions. Figure 3-64 is a flowchart of the I/O transfer that occurs between macroinstruction execution. The transfer is started by an Emulate Start microinstruction and an I/O request. A memory request is initiated to store the word available from the IOC (input) or to read a word for the IOC (output) and a hardware generated address is loaded into the micro P register to branch to an input or output subroutine. The micro address for an output (Output Data or External Function) transfer is 320_8 and for an input (Input Data or External Interrupt) transfer is 300_8. The DPS stops until the "Data Available" signal is received from memory indicating that the data is in the MDR (output) or has been stored in memory (input). The subroutine ends with an Emulate Start microinstruction to start another emulation sequence (figure 3-63).

3-196. I/O Transfer That Interrupts A Macroinstruction. Figure 3-65 is a flowchart of the I/O transfer that interrupts macroinstruction execution. The I/O transfer can interrupt macroinstruction execution when an Emulate Branch 1 or Emulate Branch 2 microinstruction occurs in the emulation sequence. When an I/O request is present at this time, the return interrupt is set and a micro address is hardware generated to branch to an I/O subroutine. For an output, the micro address is 330_8, and for an input, the micro address is 310_8. The first microinstruction of the subroutine stores the return address in A5. The DPS stops until the "Data Available" signal is received from memory indicating that the data is in the MDR (output) or has been stored in memory (input). The subroutine ends with an Emulate Start microinstruction. If another I/O request is present, the request will be serviced as described in paragraph 3-195. When an I/O request is not present, a micro interrupt request will be present (return interrupt set at beginning of this sequence). Hardware generated micro address 200_8 branches to the return interrupt subroutine. The return address is transferred from A5 back to the micro P register and macroinstruction execution will continue at the point of interruption.

3-197. MICRO INTERRUPTS. Micro interrupts are scanned when an Emulate Start microinstruction is executed and an I/O request is not present. Figure 3-66 is a flowchart of the micro interrupt sequence. Each interrupt has its own hardware generated starting address (see table 3-34). They are honored in the following priority order:

1) Return Interrupt

2) Load Interrupt

3) I/O Chain Interrupt

4) Not Run Interrupt

5) Class I or II Interrupt

6) Class III Interrupt

3-198. The Return Interrupt is set when an I/O request interrupts a micro program sequence (see paragraph 3-196). The interrupt returns the MPC to the micro program sequence where it was interrupted.

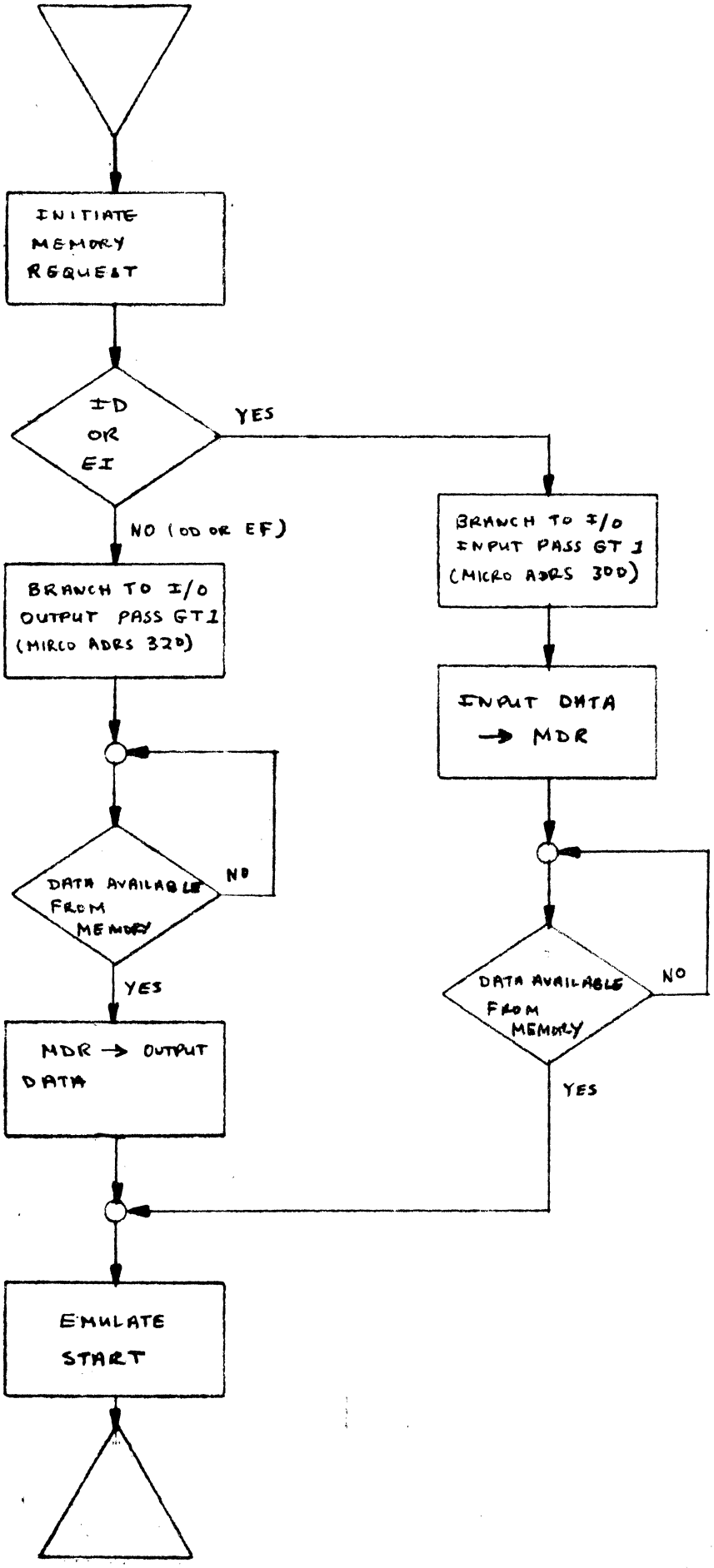


Figure 3-64. I/O Transfer Between Macro Instruction Execution

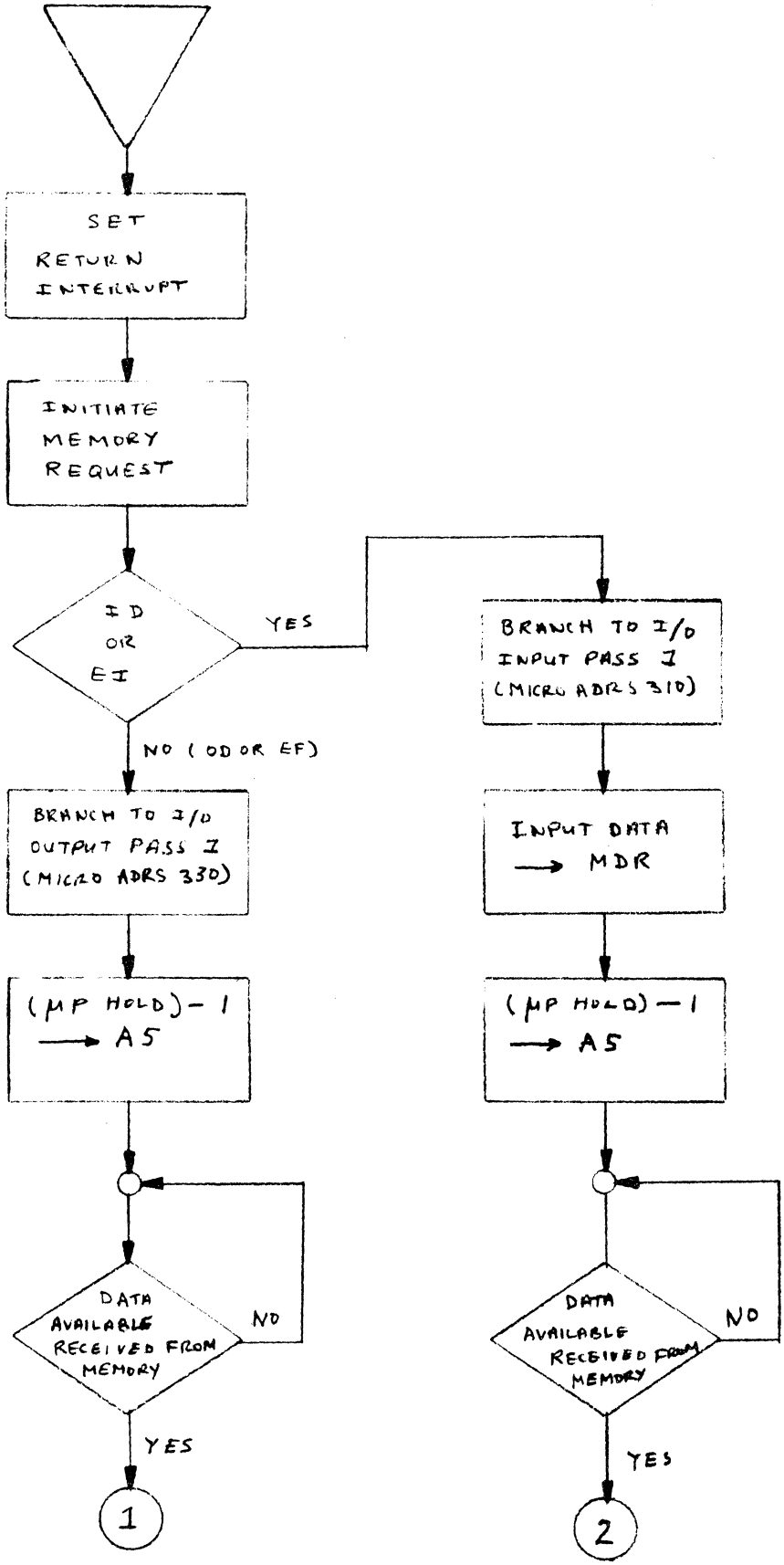


Figure 3-65. I/O Transfer That Interrupts A Macro Instruction

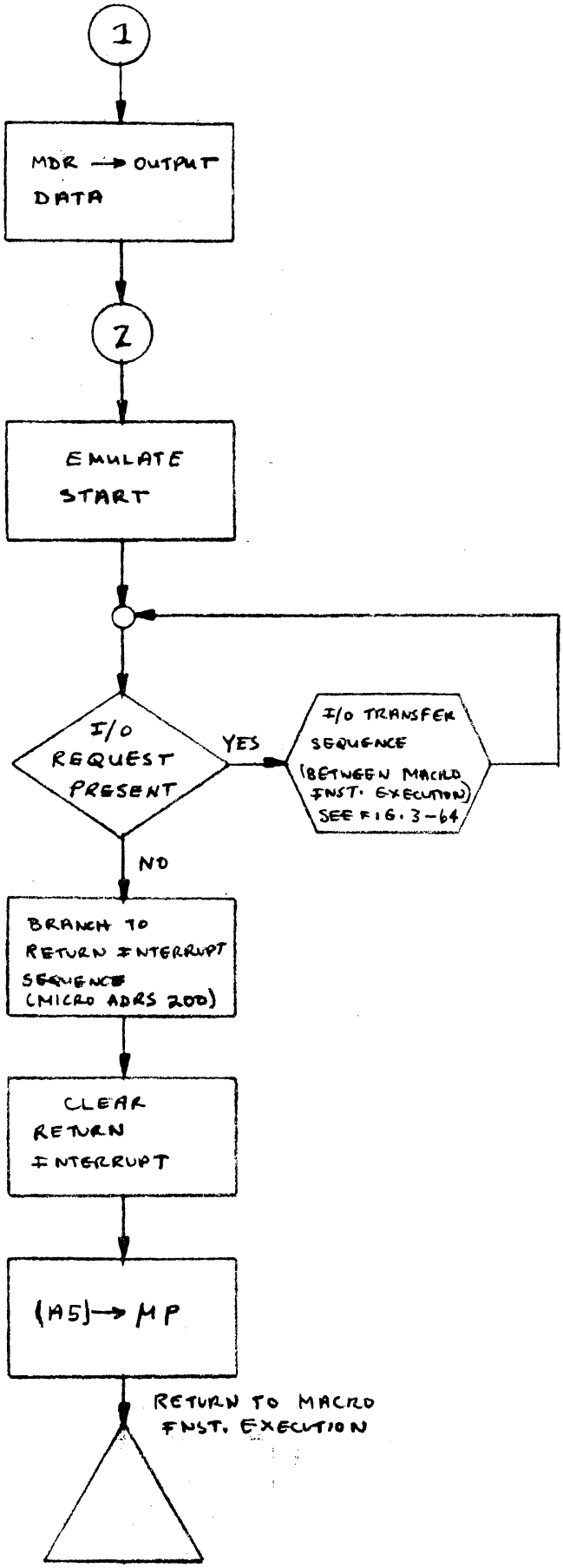


Figure 3-65. I/O Transfer That Interrupts A Micro Instruction (Cont)

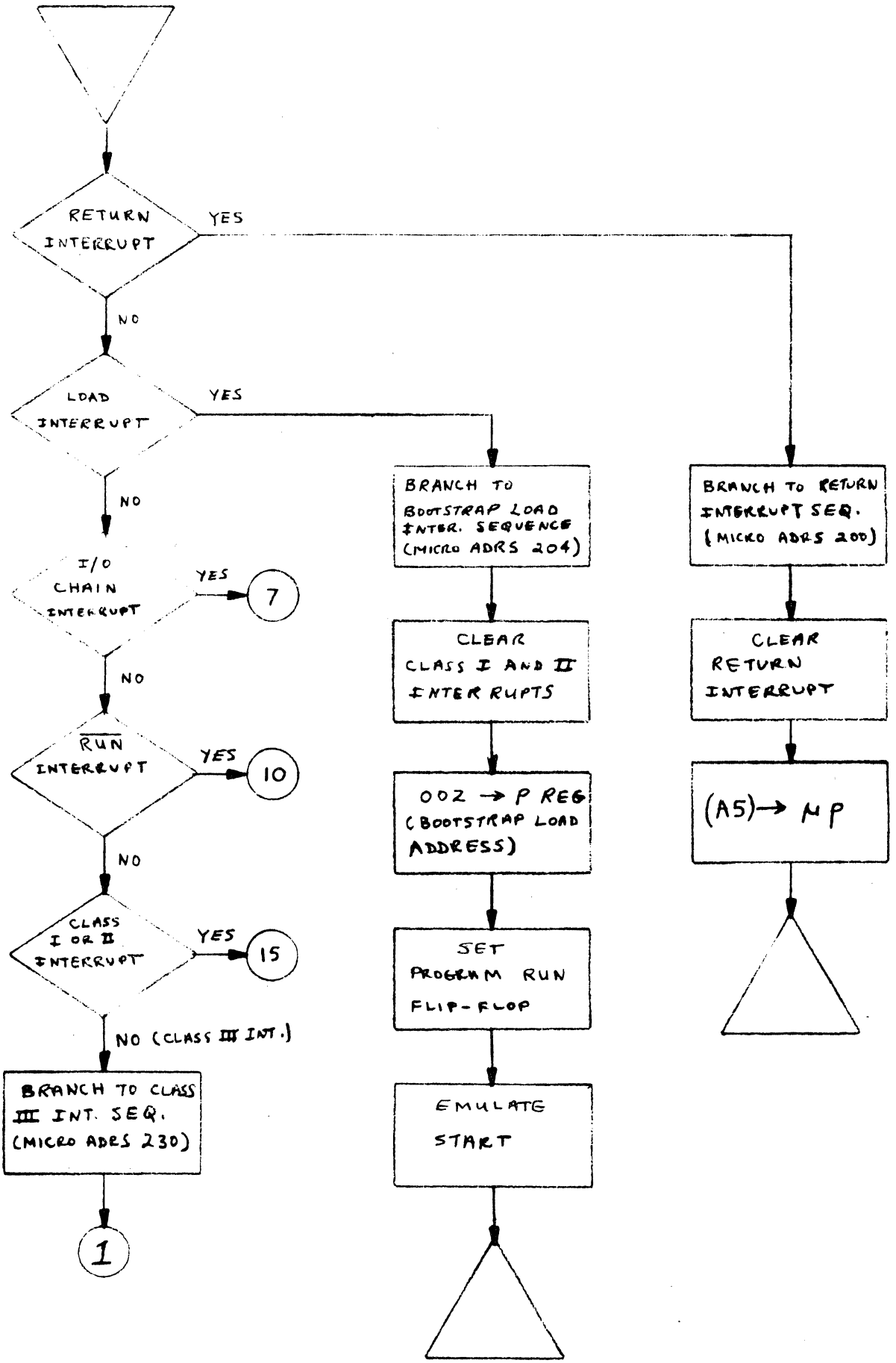


Figure 3-66. Micro Interrupt Sequence

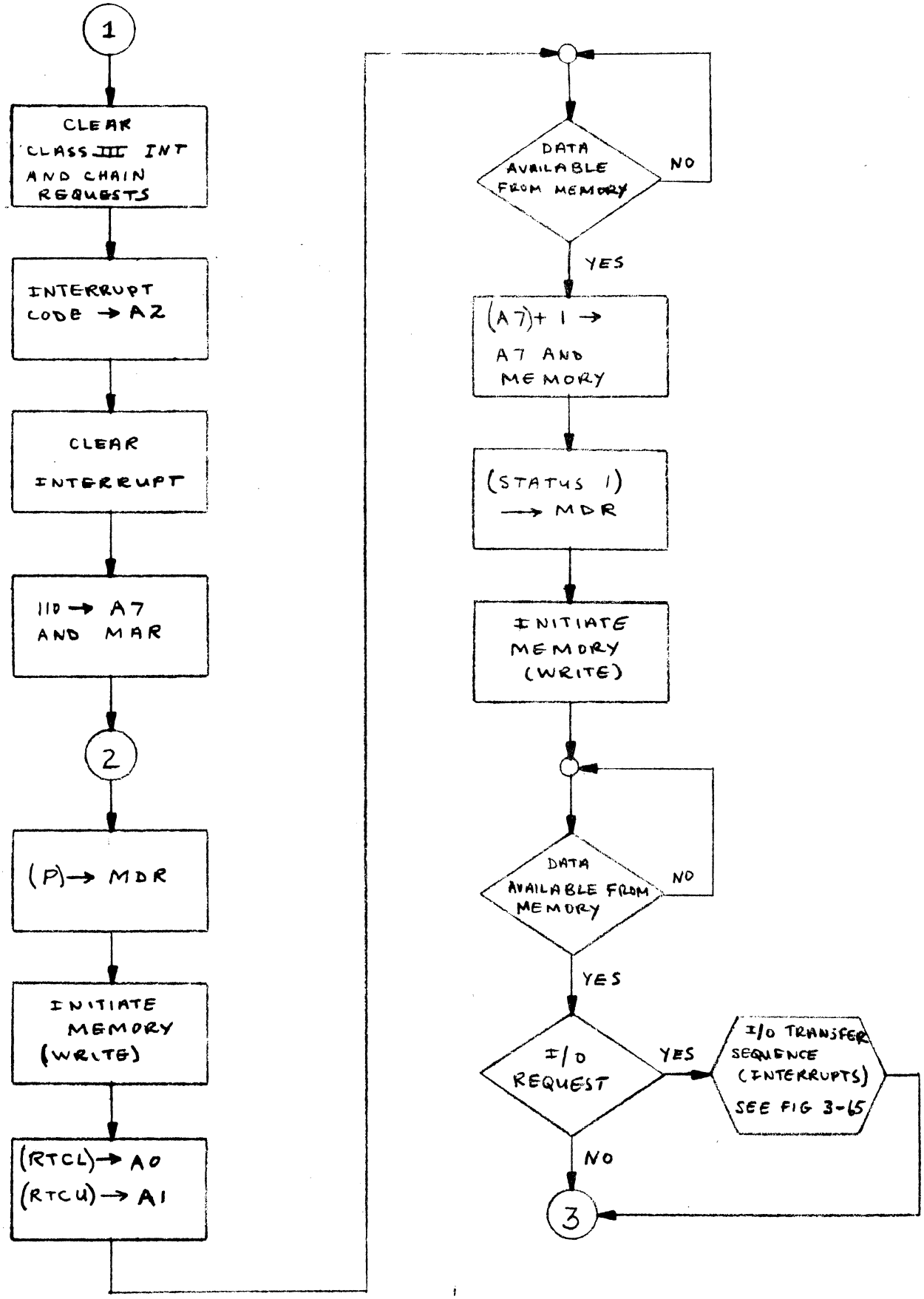


Figure 3-66. Micro Interrupt Sequence (Cont)

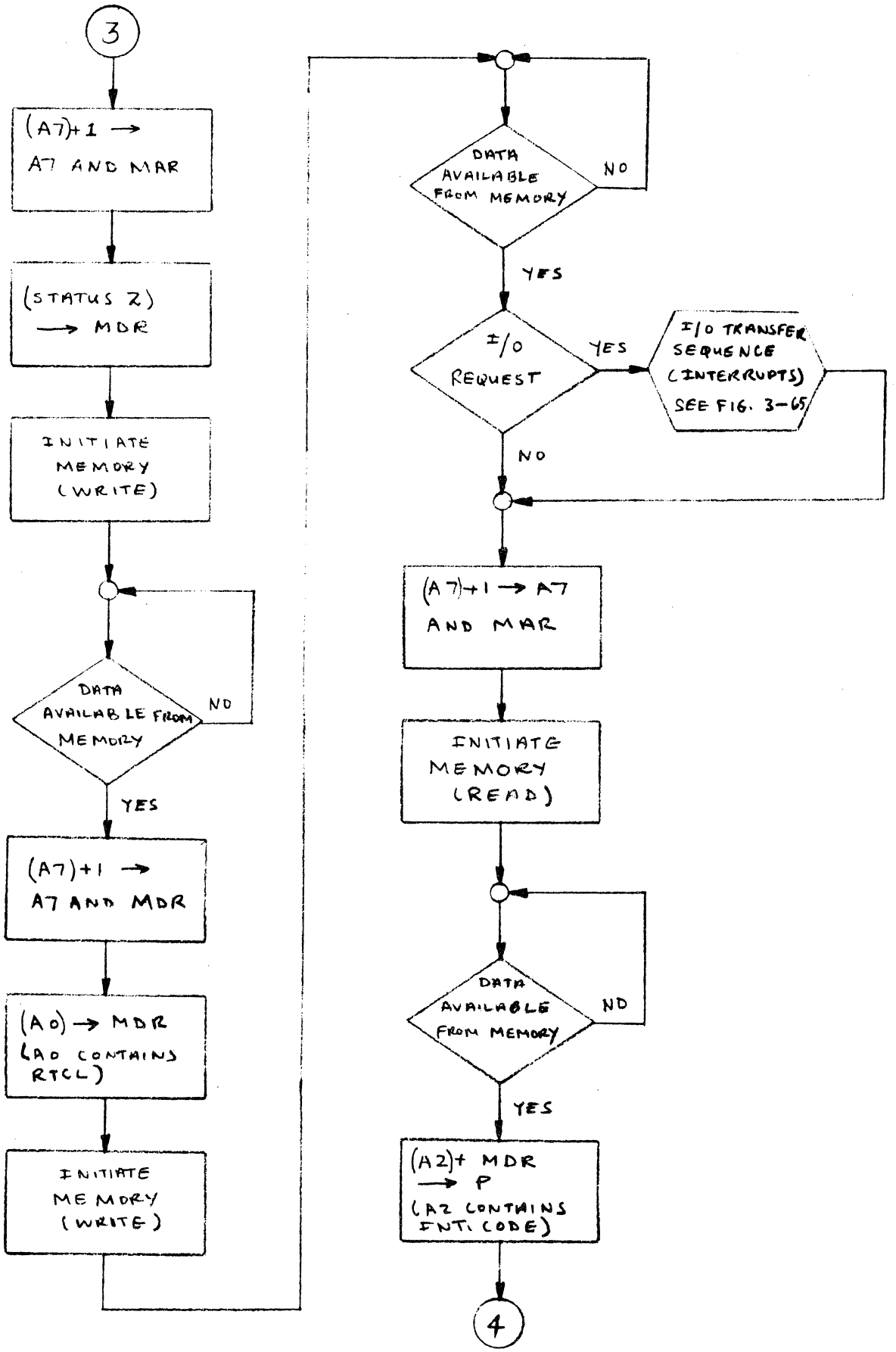


Figure 3-66. Micro Interrupt Sequence (Cont)

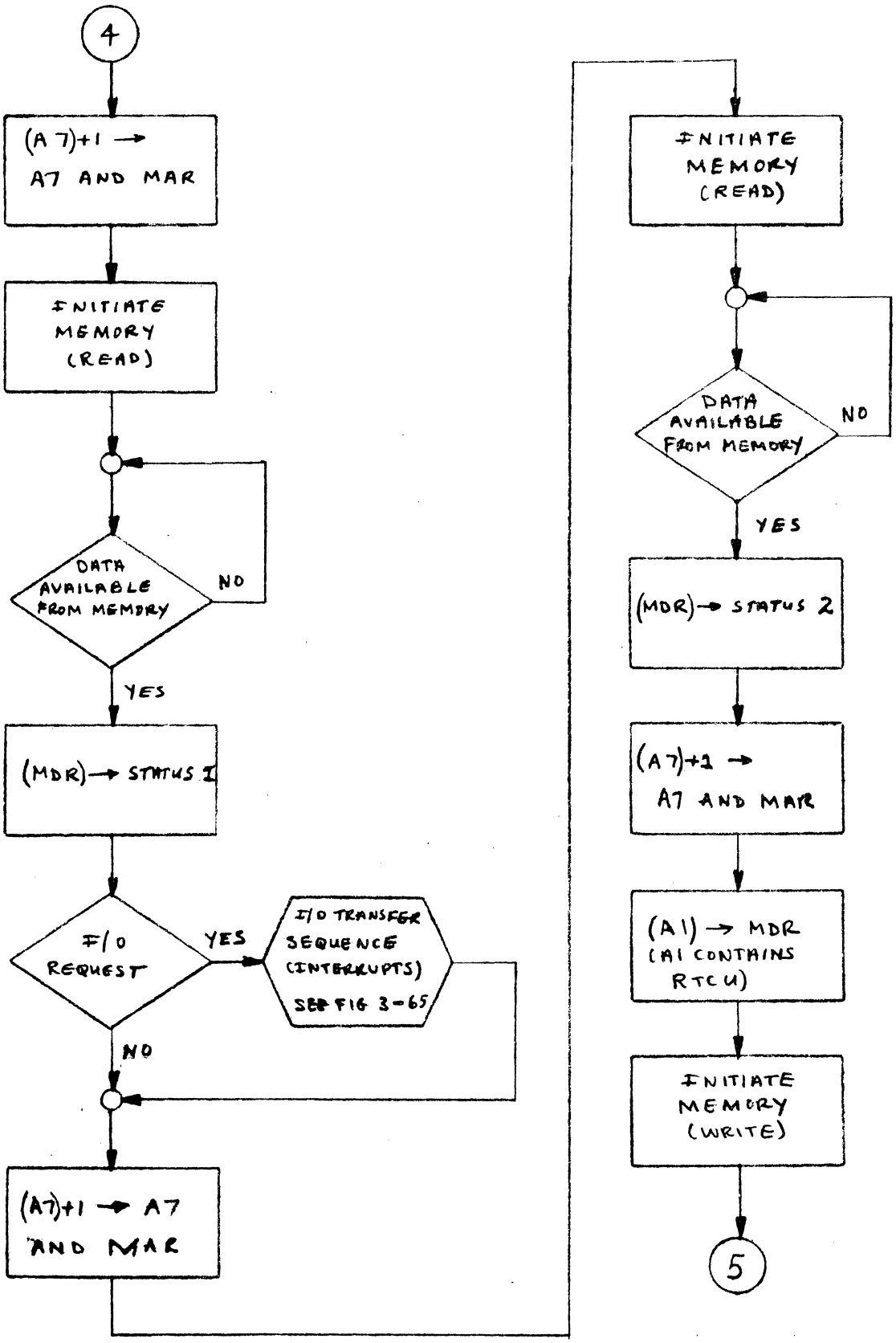


Figure 3-66. Micro Interrupt Sequence (Cont)

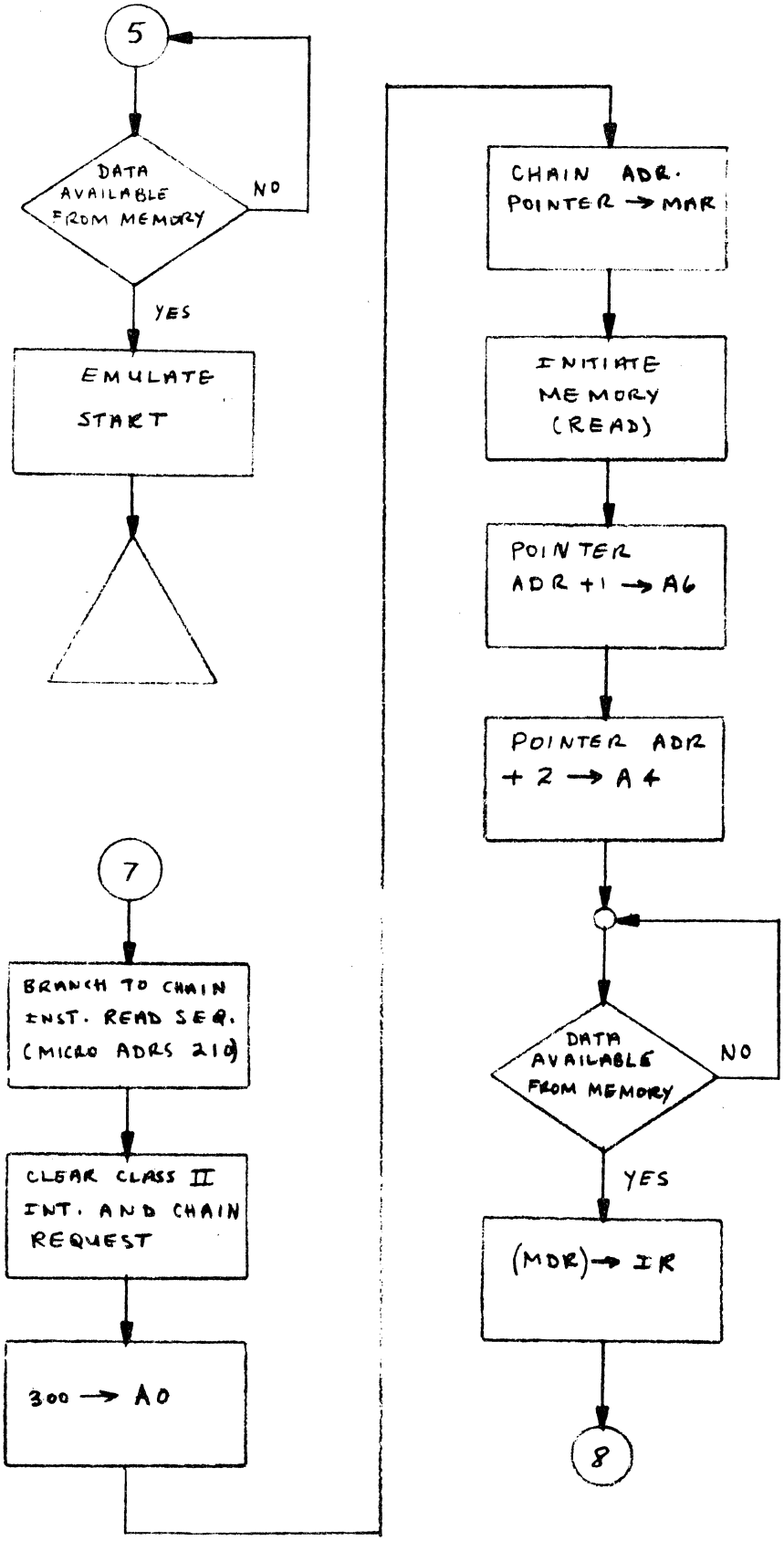


Figure 3-66. Micro Interrupt Sequence (Cont)

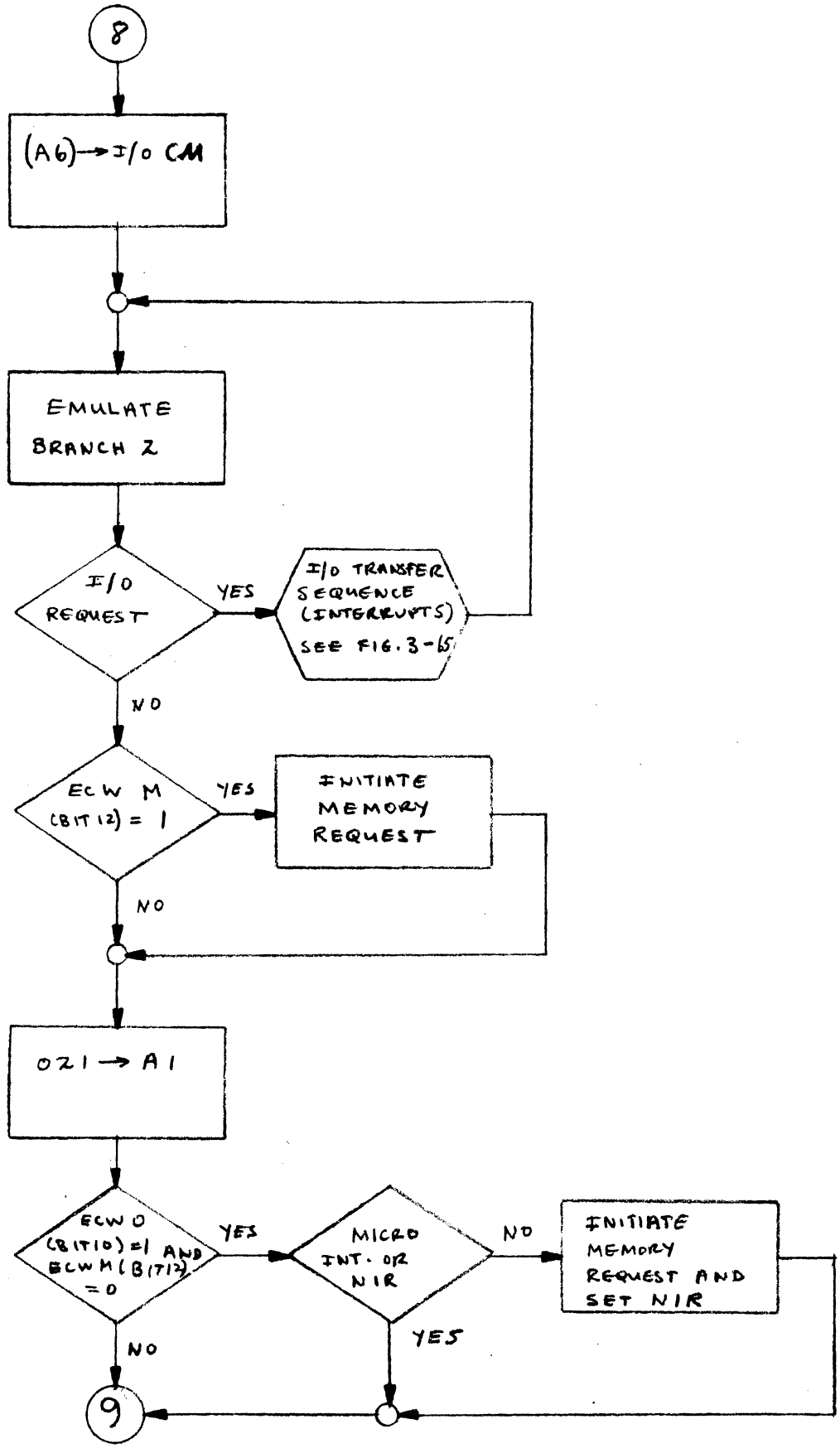


Figure 3-66. Micro Interrupt Sequence (Cont)

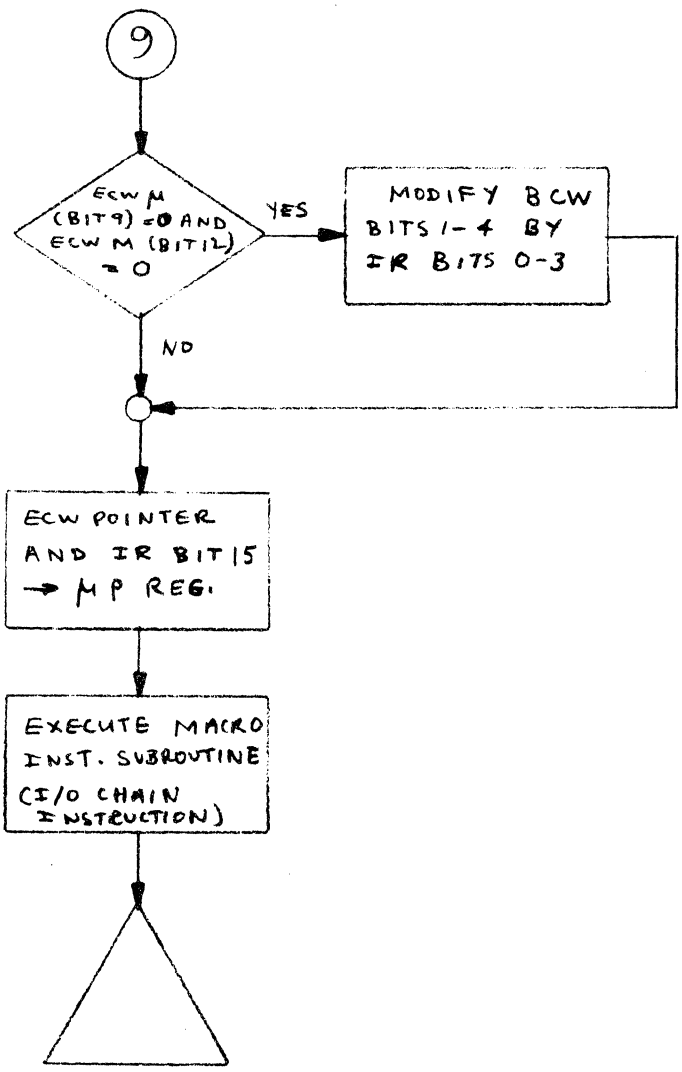


Figure 3-66. Micro Interrupt Sequence (Cont)

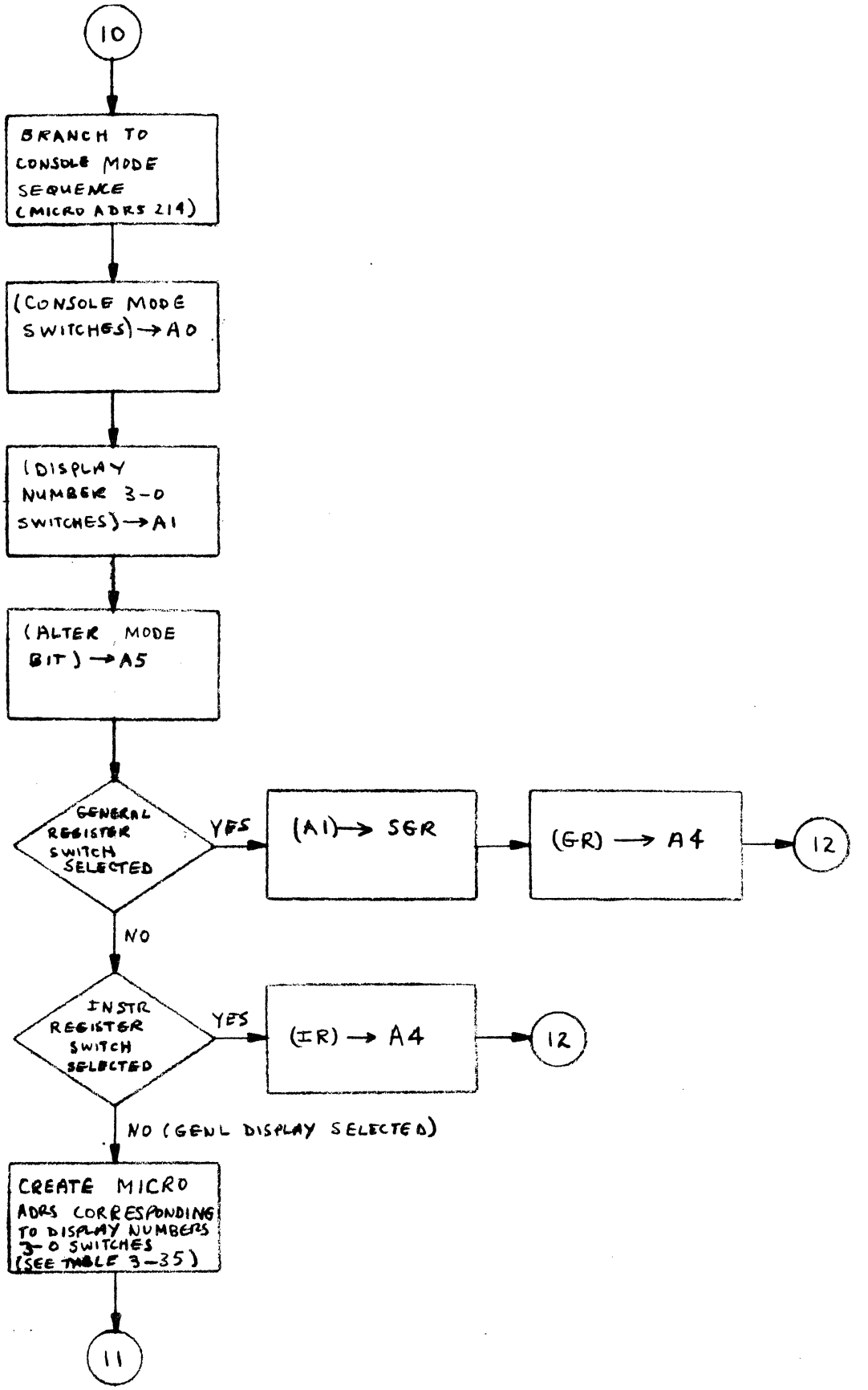


Figure 3-66. Micro Interrupt Sequence (Cont)

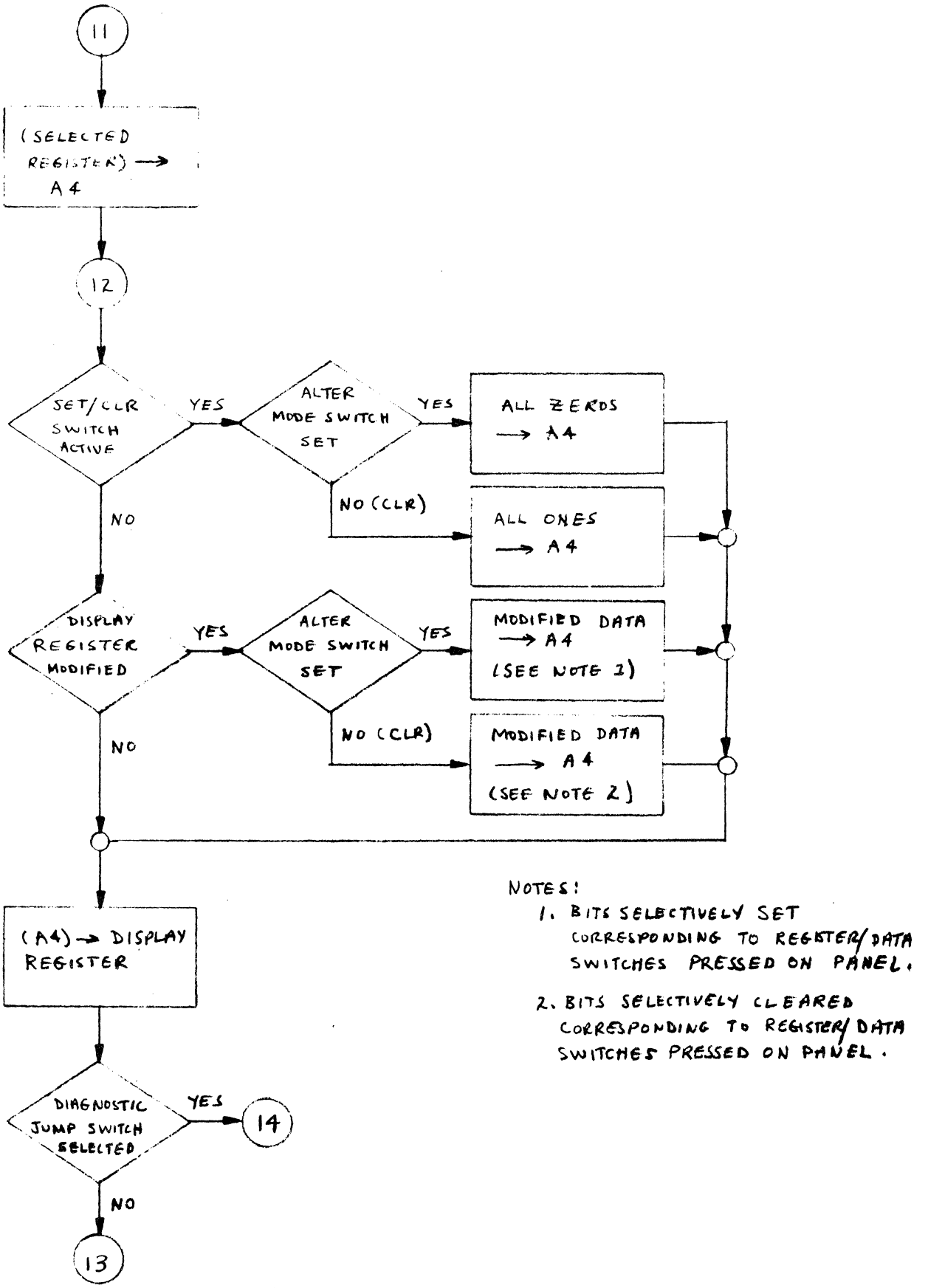


Figure 3-66. Micro Interrupt Sequence (Cont)

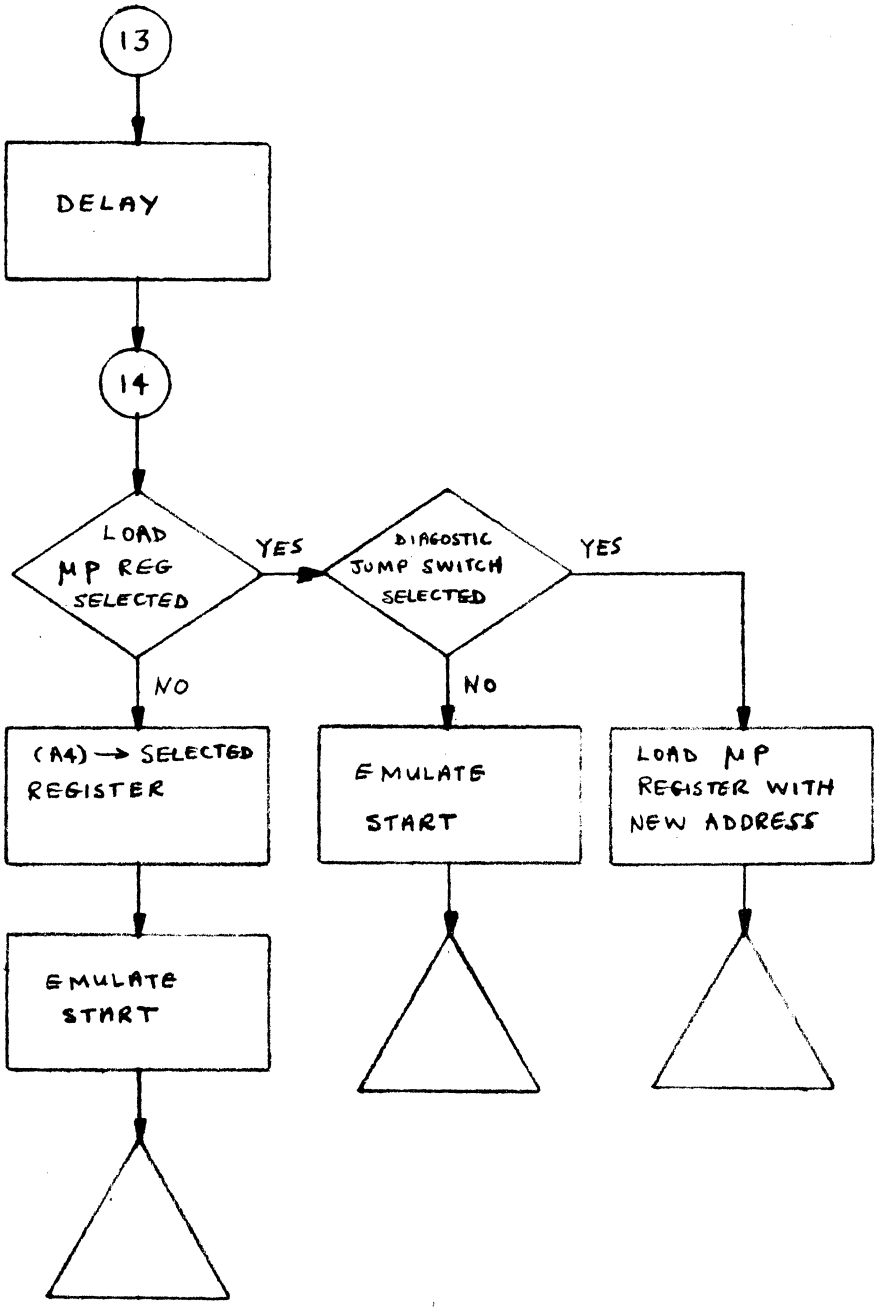


Figure 3-66. Micro Interrupt Sequence (Cont)

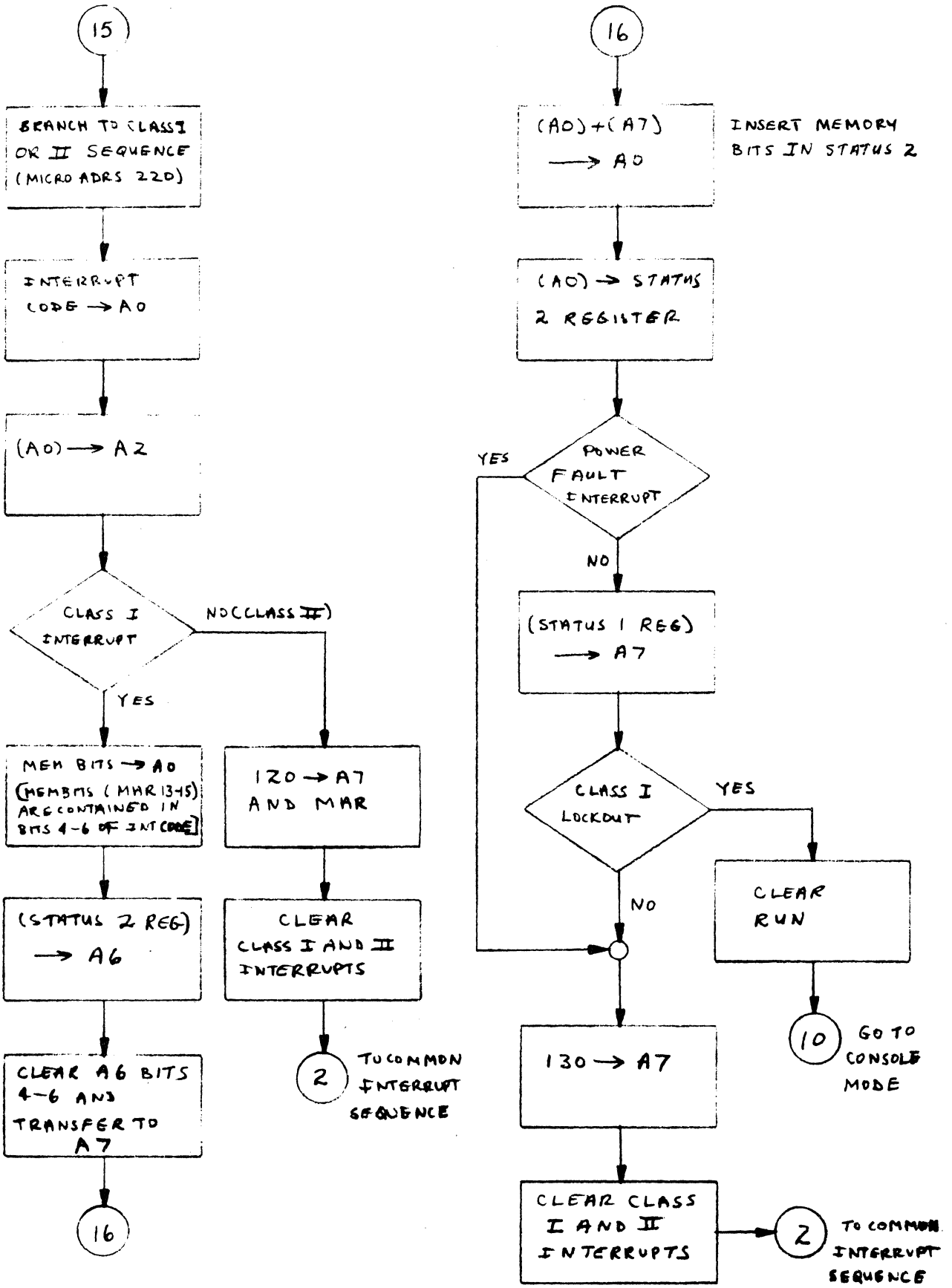


Figure 3-66. Micro Interrupt Sequence (Cont)

Table 3-35. Micro Branch Conditions For General Display

DSPL NUMBER SWITCHES 3210	ADDRESS LOADED IN MICRO P REG (OCTAL)	REGISTER OR ROUTINE SELECTED
0000	2000	P Reg
0001	2004	Status #1 Reg
0010	2010	Status #2 Reg
0011	2014	RTCL
0100	2020	RTCU
0101	2024	Breakpoint Reg
0110	2030	I/O Control Memory
0111	2034	Page Address Reg
1000	2040	Main Memory (P Reg contains address)
1001	2044	Output Data
1010	2050	Monitor Clock
1111	2036	Load μP Reg

3-199. The Load Interrupt (activated by the LOAD switch) starts the computer executing the bootstrap load program stored in NDRO memory.

3-200. The I/O Chain Interrupt executes a macroinstruction in the I/O chain and updates the chain address pointer.

3-201. The Not Run Interrupt places the DPS in the console mode. This allows the operator to monitor or change the contents of registers from the panel.

3-202. The Class I, II, and III Interrupts are macro interrupts (see paragraph 3-58). The micro program subroutine stores the contents of the P, Status Register #1, Status Register #2, RTCL, and RTCU registers in the assigned main memory locations (see Appendix D) and loads the P, Status Number 1, and Status Number 2 registers. The P register contains the starting address of the interrupt subroutine stored in main memory.

3-203. LOGIC DEVICE DESCRIPTIONS

3-204. Appendix E describes the logic devices used on the logic and memory circuit cards in the DPS. In most cases, the logic devices are contained in dual-in-line packages (DIP's). The descriptions of these devices are a valuable aid in understanding the logic schematic diagrams of Chapter 9 (Volume II) on which these logic devices appear in symbolic form.

CHAPTER 4

PREVENTIVE MAINTENANCE

4-1. INTRODUCTION.

4-2. Preventive maintenance (PM) encompasses the procedures to be followed by DPS operators or maintenance personnel to keep the equipment in optimum operating condition and to prevent a decline of productive use. Table 4-1 provides an index to the DPS PM procedures, which consist mainly of cleaning, of switch and indicator checks, and of performing a diagnostic/confidence test program. The PM procedures should be performed by a Data Systems Technician Second Class or equivalent. The procedures should be performed at regularly scheduled intervals; the frequency of the intervals may vary dependent on the operating schedules necessary to meet productive requirements. Where the DPS operates continuously, operation should be discontinued at least once a week for PM. Where DPS operation is on a daily on/off basis, the diagnostic program or other test program should be run daily as a confidence check; the other PM procedures should be performed as scheduled. The diagnostic test program is documented in Volume 3 (Chapter 10)* of this technical manual. If the diagnostic test program is not available, the Factory Acceptance Test or similar confidence test program may be used. The scheduled maintenance instructions in this manual are cancelled when the Planned Maintenance System (PMS) is implemented for this equipment aboard your ship or station.

*Not available at time of this publication.

Table 4-1. Preventive Maintenance Index

PERIODICITY	MAINTENANCE ACTION	REFERENCE
MR*	Clean Air Filter	Paragraph 4-4
SR*	Clean Cabinet	Paragraph 4-5
M	Test Indicators	Paragraph 4-6
DR**	Run Confidence Test	Paragraph 4-7

D = Daily
W = Weekly
M = Monthly
Q = Quarterly (3 mo.)
S = Semiannually (6 mo.)
A = Annually (12 mo.)
R = As specified

*More or less often depending on environmental conditions.
**May be less often, if required by system operating schedules.

4-3. PREVENTIVE MAINTENANCE PROCEDURES.

4-4. AIR FILTER CLEANING. The front panel air filter is the only item that requires regular attention. It should be cleaned monthly or when necessary by vacuum cleaning or washing in a soap or detergent solution. To remove and clean the air filter, use the following procedure. See figure 4-1.

1. Ensure power is turned off.

2. Remove eight front panel retaining screws (Figure 4-1), using a 5/32 inch Allen wrench.

3. Swing front panel open.

4. Remove two filter retaining screws (Figure 4-2), using screwdriver.

5. Vacuum the filter. If filter is to be washed:

   a. Clean filter thoroughly in hot, soapy water.

   b. Rinse, wipe with clean cloth, and vacuum dry.

6. Replace filter and filter retaining screws.

7. Swing the front panel closed.

8. Replace the eight front panel retaining screws.

4-5. CABINET CLEANING. Semiannually, or as required, the cabinet should be cleaned and visually inspected. See Figure 4-2. Electrical checks and adjustments, if required, can also be made at this time.

CAUTION

Use of forced air for cleaning is not recommended, since it may force dirt particles into critical areas. Use care not to damage or disturb wiring or components.

1. Ensure power is turned off and power cable disconnected.

2. Open the front panel of the DPS as listed in steps 2 through 3 of paragraph 4-4.

3. Using a soft bristle brush and a vacuum cleaner, clean the inside of the front panel door and the exposed side of the memory drawer.

4. With Phillips screwdriver, disengage four quick-release memory chassis fasteners. Pull out the memory chassis assembly and swing it open to the left. Vacuum the memory chassis.

5. Remove the power supply, following the removal procedure listed in Chapter 6.

6. Vacuum the cabinet space used by the power supply, the power supply itself, and the front of the individual circuit card modules, being careful not to damage components.

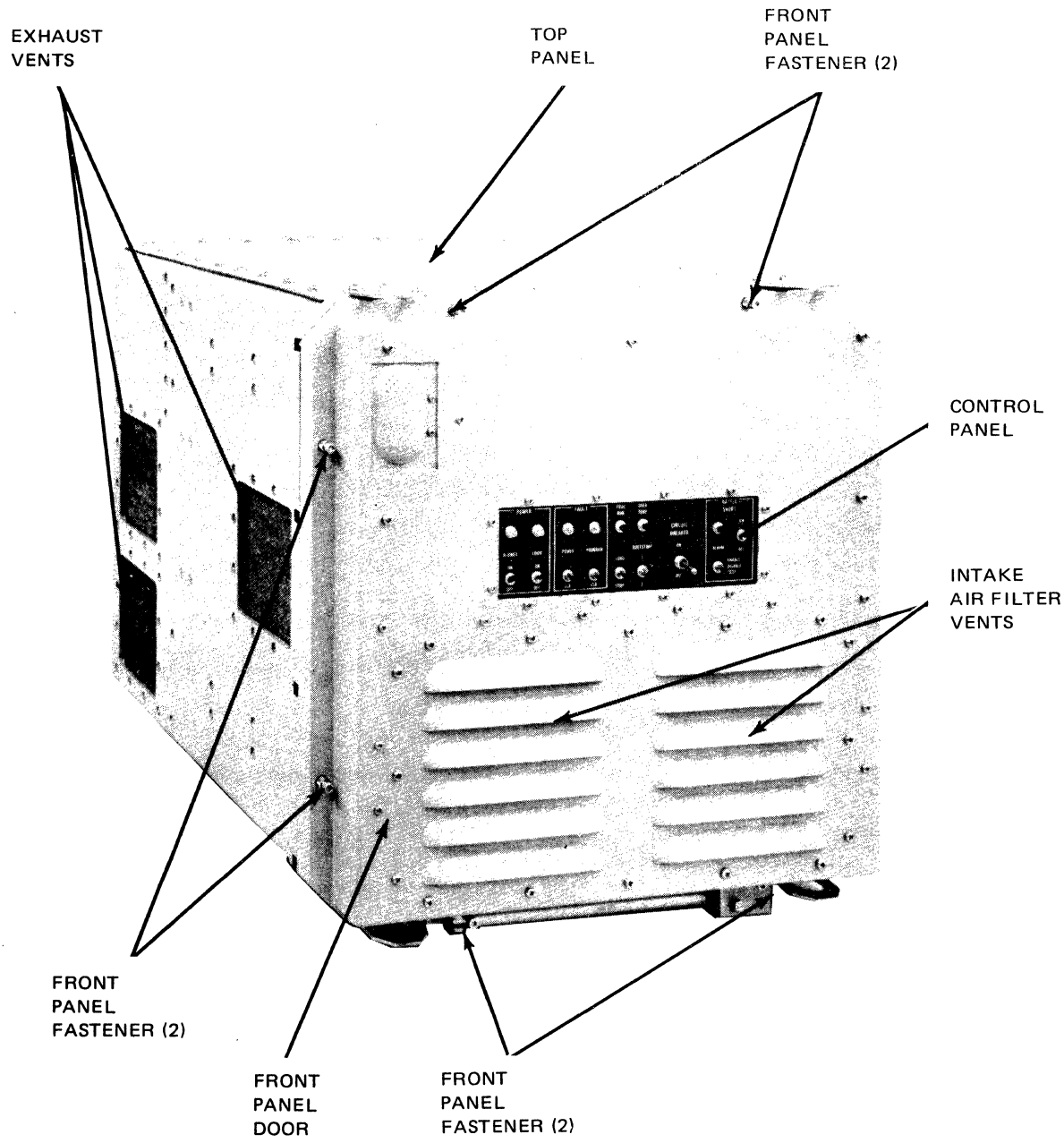


Figure 4-1. DPS Cabinet, Overall View

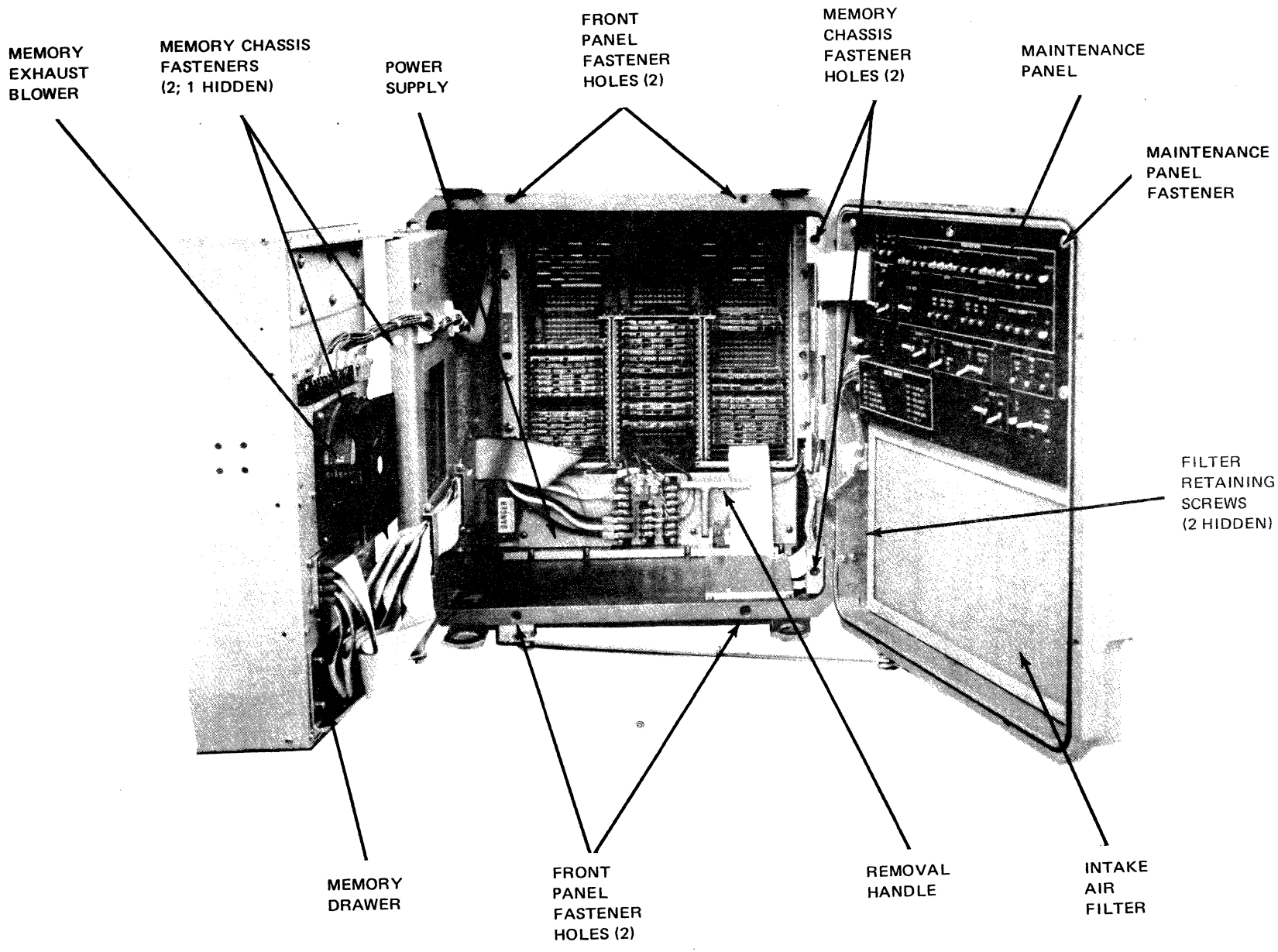


Figure 4-2. DPS Cabinet, Front Panel Open

7. Vacuum off the exhaust vent filters.

8. Visually inspect electrical components for discoloration and evidence of overheating.

9. Check terminal connections for security and insulation for cracks or deterioration.

10. Make necessary corrections for any defects discovered in the foregoing inspections.

11. Replace the power supply per procedure in Chapter 6.

12. If power supply voltages are to be checked, follow procedure in Chapter 5.

13. Replace and fasten the memory drawer.

14. Close and fasten front panel.

15. Replace power cable and apply power.

4-6. CONTROL AND MAINTENANCE PANEL INDICATORS. Table 4-2 provides a list of the DPS indicators and a method of testing them. See Figures 2-1 and 2-2.

Table 4-2. Control and Maintenance Panel Indicators

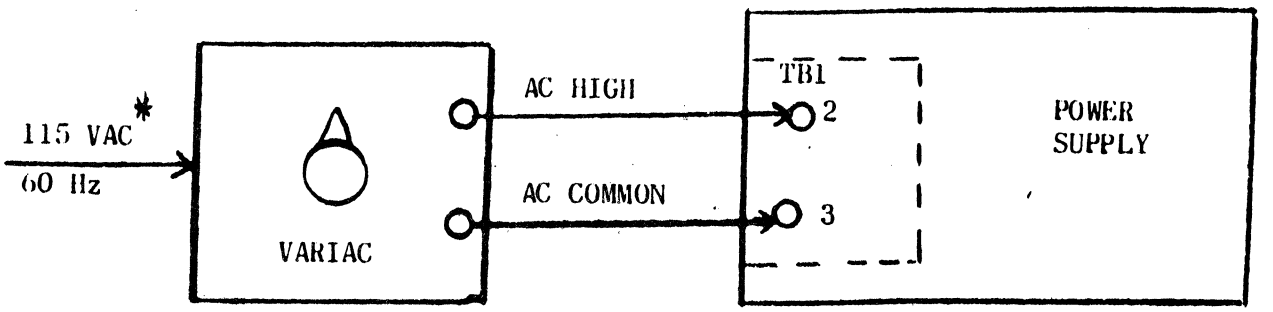
PANEL	IDENTIFICATION	FUNCTION	TEST
Control	BLOWER POWER Indicator	When lit, indicates blower power is applied and enabled.	Ensure power cable is connected and CIRCUIT BREAKER is ON. Place BLOWER POWER switch in ON position.
Control	LOGIC POWER Indicator	When lit, indicates logic power is applied and enabled.	Ensure power cable is connected, CIRCUIT BREAKER is ON, and BLOWER POWER is ON. Place LOGIC POWER switch in ON position.
Control	POWER FAULT Indicator	When lit, indicates a Power Fault Interrupt has occurred. Cleared by POWER FAULT CLR switch in CLR position.	See figure 4-3 for test set-up. Reduce input voltage until FAULT indicator lights. Return voltage to correct level and clear fault.
Control	PROGRAM FAULT Indicator	When lit, indicates the DPS has attempted to execute an illegal instruction. Cleared by PROGRAM FAULT CLR switch in CLR position.	Refer to Chapter 2, Operation, and manually set in and execute an illegal instruction. Then clear the indicator.

Table 4-2. Control and Maintenance Panel Indicators (Cont)

PANEL	IDENTIFICATION	FUNCTION	TEST
CONTROL	PROG RUN Indicator	When lit, indicates DPS is executing instructions in RUN mode.	Refer to Chapter 2 and start DPS executing instructions in RUN mode.
Control	OVERTEMP Indicator	When lit, indicates DPS internal cabinet air temperature is within 25°F of the maximum temperature at which the DPS can operate without component damage.	Place the ALARM ENABLE/DISABLE/TEST switch in the TEST position. OVER TEMP indicator lights and ALARM sounds.
Control	ALARM (Audible) Indicator	When sounding (ALARM ENABLE/DISABLE/TEST switch in ENABLE position), indicates DPS internal cabinet air temperature is within 25°F of the maximum temperature at which the DPS can operate without component damage.	Place the ALARM ENABLE/DISABLE/TEST switch in the TEST position. ALARM sounds and OVER TEMP indicator lights.
Control	BATTLE SHORT Indicator	When lit indicates BATTLE SHORT switch is in the ON position (which disables DPS overtemperature shutdown function).	Place BATTLE SHORT ON/OFF switch in ON position.
Maint.	PROG RUN Indicator-switch	When lit, indicates the DPS is executing instructions in the RUN mode.	Refer to Chapter 2 and start DPS executing instructions in the RUN mode.
Maint.	POWER FAULT Indicator-switch	When lit, indicates a Power Fault Interrupt has occurred. Pressing the indicator-switch clears the POWER FAULT indicator.	See figure 4-3 for test setup. Reduce input voltage until indicator lights. Return voltage to correct level and clear fault.
Maint.	PROG FAULT Indicator-switch	When lit, indicates the DPS has attempted to execute an illegal instruction. Pressing the indicator-switch clears the PROG FAULT indicator.	Refer to Chapter 2, Operating Instructions and manually set up and execute an illegal instruction.

Table 4-2. Control and Maintenance Panel Indicators (Cont)

PANEL	IDENTIFICATION	FUNCTION	TEST
Maint.	PROGRAM STOP Indicator	When lit, indicates a program stop condition has been satisfied.	Refer to Chapter 2, Operation, to set up a program stop.
Maint.	Time Meter	Indicates time in hours that DPS logic power has been applied and enabled.	Apply logic power and observe that meter advances.
Maint.	MICRO STEP MODE Indicator-switch	When lit indicates DPS is in Micro Step mode. Pressing indicator switch places DPS in Micro Step mode.	Activate MICRO STEP switch. To clear Micro Step mode activate DISPLAY SELECT CLR switch.
Maint.	OP STEP MODE Indicator-switch	When lit, indicates DPS is in Op Step mode or in Micro Step mode to execute a single instruction.	Activate OP STEP switch to clear RUN mode and place DPS in Op Step mode.
Maint.	RUN MODE Indicator-switch	When lit, indicates DPS is in Run mode or in Micro Step mode to execute successive instructions.	Activate RUN MODE switch to clear Op Step mode and enable Run mode.
Maint.	REGISTER/DATA 0-15 Indicator-switches	When lit, displays contents of selected register.	Set ALTER MODE SET/CLEAR switch in SET position and press REGISTER/DATA SET/CLR switch. To clear, set ALTER MODE SET/CLEAR switch in CLEAR position and press REGISTER/ DATA SET/CLR switch.
Maint.	DISPLAY SELECT MICRO ADRS MICRO INSTR NORMAL DSPL	When lit, as specified in Table 2-3, indicate REGISTER/DATA is displaying the corresponding register.	Refer to Table 2-3. Operation of any one of MICRO ADRS, MICRO INSTR, or NORMAL DSPL causes the other two to clear.
	INSTR REG GENL DSPL GENL REG	When lit, as specified in Table 2-3, indicate REGISTER/DATA is displaying the corresponding register.	Refer to Table 2-3. Operation of any one of INSTR REG, GENL DSPL, or GENL REG causes the other two to clear.
	DISPLAY NUMBER 0-3 Indicator-switches	When operated as specified in Table 2-3 these switches cause REGISTER/DATA to display the corresponding register contents.	Press DISPLAY NUMBER indicator-switches 0-3. Observe that they light. Press DISPLAY SELECT CLR switch. Observe that indicators extinguish.



*Ensure the correct voltage and frequency are used for the equipment under test.

Figure 4-3. Power Interrupt (Fault) Test Setup

4-7. CONFIDENCE TEST. The diagnostic test program, documented in Volume 3 (Chapter 10), should be run daily, or as often as practical under the processing schedules, as a performance test, to give confidence that the DPS is performing correctly. This is the only performance test required for the DPS. It attempts to exercise and test every DPS circuit and the micro control program, and to diagnose any failure it detects. If the diagnostic test program is not available,* the Factory Acceptance Test or similar program should be used; this will detect malfunctions, but not diagnose them. The recommended procedure is to load and run the program at the end of a computing day, and to run it again immediately after turning on the DPS at the beginning of the next computing day.

*Not available at time of this publication.

CHAPTER 5

TROUBLESHOOTING

5-1. INTRODUCTION.

5-2. Troubleshooting information and procedures for the DPS are based primarily on the assumption that most malfunctions will be detailed and isolated through use of the diagnostic test program* documented in Volume 3 (Chapter 10) of this technical manual.

5-3. DIAGNOSTIC TEST PROGRAM. The diagnostic test is to be run regularly as part of the normal preventive maintenance procedures; it should also be run as the primary troubleshooting tool whenever a malfunction is suspected or has been detected by some other means. The DPS has three built-in fault detectors; overtemperature, power out of tolerance, and program fault. Most faults, however, are first detected by the diagnostic or other test program, and the procedures that are included in the program documentation lead to isolation of the faulty circuit card or component.

5-4. MANUAL TROUBLESHOOTING. In some cases, where the nature of the fault is such that it prevents the loading of the diagnostic test program or prevents the DPS from successfully diagnosing itself, troubleshooting must be done manually. In many cases, manual diagnosis can be performed by replacing circuit cards in the suspected area with spare cards until the symptom disappears, or shifting multiple usage cards from one location to another to see if the symptom shifts. Table 5-1 is a list of the multiple usage cards.

5-5. Sometimes it may be necessary to troubleshoot manually by stepping through instructions in Op Step or Micro Step mode, observing the contents of displayed registers or observing the status of individual signals on an oscilloscope, and logically troubleshooting with the aid of the logic schematic diagrams in Volume 2 (Chapter 9) and the microprogram listing in Appendix C. The outer edge of all logic circuit cards contains test points, where the major signals in that card are available for checking. These test points are accessible with the maintenance panel door and the memory chassis swung open.

5-6. TROUBLESHOOTING AIDS. Additional troubleshooting aids provided in this chapter are the Troubleshooting Index, the Lamp and Relay Indexes, and the Protective Device Index, Tables 5-2 through 5-5, respectively.

CAUTION

Turn power off before removing or replacing circuit cards.

5-7. MAINTENANCE TURN-ON. No special turn-on procedures are required for maintenance purposes. Follow the procedures given with the diagnostic test program in Chapter 10 (Volume 3) or the operating procedures in Chapter 2.

* Not available at time of this publication.

Table 5-1. Multiple-Usage Circuit Cards*

CARD NO.	TITLE	LOCATIONS
7092175	ALU	B11-14
7092185	MICRO REG	A3-5
7125306	I/O CONT MEM	A20-23
7125311	P, BKPT, MAR	C5-6
7125380	STATUS REG	C13-14
7125500	SHFT MTRX	A9-10
7126125	TWO BIT MULTIPLY	A7-8
7126155	MEM INTRFC	C3-4

*The IOC has additional multiply usage cards if it has several groups of channels with identical interfaces.

Table 5-2. Troubleshooting Index

Functional Area	Troubleshooting Paragraph	Troubleshooting Diagram	Functional Description Paragraph
Blowers	5-13	Figure 9-000B	N/A
Heat Sensors	5-14	Figure 9-000B	N/A
IOC	5-3 through 5-5 and 5-16	Figure 9-200 through 9-407. Chapter 10	3-119 through 3-165
Logic (MPC and Processor)	5-3 through 5-5	Figure 9-001 through 9-115. Chapter 10	3-20 through 3-77, and 3-191
Memory	5-15	Chapter 9, diagram 7101751-399 through -461	3-78 through 3-118
Panels	5-12	Figure 9-000C	2-3 through 2-6
Power	5-9 through 5-11	Chapter 9, Figure 9-000A and B 7101840 7101875 7101880 7101885 7101990 1701995 7119455	3-166 through 3-190

Table 5-3. Relay Index (See Paragraph 5-)

Reference Description	Functional Name	Engineering Voltage	Figure Number
A2K1	Power Supply Energizing Relay	115 Vac or 240 Vac	9-000A

Table 5-4. Lamp Index (See Paragraph 5-)

Reference Description	Functional Name	Type	Engineering Voltage	Figure Number
A1DS1	Battle Short On	Neon	115 Vac	9-000A
A1DS2	Temperature Warning	Neon	115 Vac	9-000A
A1DS3	Program Run	LED	+5 Vdc	9-000C
A1DS4	Program Fault	LED	+5 Vdc	9-000C
A1DS5	Power Fault	LED	+5 Vdc	9-000C
A1DS6	Logic Power	Incand.	+5 Vdc	9-000C
A1DS7	Blower On	Neon	115 Vac	9-000A
A2DS1	Prog Stop	LED	+5 Vdc	9-000C
A2DS2	Display Bit 00	LED I/S.	+5 Vdc	9-000C
A2DS3	Display Bit 01	LED I/S.	+5 Vdc	9-000C
A2DS4	Display Bit 02	LED I/S.	+5 Vdc	9-000C
A2DS5	Display Bit 03	LED I/S.	+5 Vdc	9-000C
A2DS6	Display Bit 04	LED I/S.	+5 Vdc	9-000C
A2DS7	Display Bit 05	LED I/S.	+5 Vdc	9-000C
A2DS8	Display Bit 06	LED I/S.	+5 Vdc	9-000C
A2DS9	Display Bit 07	LED I/S.	+5 Vdc	9-000C
A2DS10	Display Bit 08	LED I/S.	+5 Vdc	9-000C
A2DS11	Display Bit 09	LED I/S.	+5 Vdc	9-000C
A2DS12	Display Bit 10	LED I/S.	+5 Vdc	9-000C
A2DS13	Display Bit 11	LED I/S.	+5 Vdc	9-000C
A2DS14	Display Bit 12	LED I/S.	+5 Vdc	9-000C
A2DS15	Display Bit 13	LED I/S.	+5 Vdc	9-000C
A2DS16	Display Bit 14	LED I/S.	+5 Vdc	9-000C
A2DS17	Display Bit 15	LED I/S.	+5 Vdc	9-000C
A2DS18	Program Fault	LED I/S.	+5 Vdc	9-000C
A2DS19	Power Fault	LED I/S.	+5 Vdc	9-000C
A2DS20	Program Run	LED I/S.	+5 Vdc	9-000C
A2DS22	Display Select 00	LED I/S.	+5 Vdc	9-000C
A2DS23	Display Select 01	LED I/S.	+5 Vdc	9-000C
A2DS24	Display Select 02	LED I/S.	+5 Vdc	9-000C
A2DS25	Display Select 03	LED I/S.	+5 Vdc	9-000C
A2DS26	General Register	LED I/S.	+5 Vdc	9-000C
A2DS27	General Display	LED I/S.	+5 Vdc	9-000C
A2DS28	Instruction Register	LED I/S.	+5 Vdc	9-000C
A2DS29	Normal Display	LED I/S.	+5 Vdc	9-000C
A2DS30	Micro Instruction	LED I/S.	+5 Vdc	9-000C
A2DS31	Micro Address	LED I/S.	+5 Vdc	9-000C
A2DS35	Run Mode	LED I/S.	+5 Vdc	9-000C
A2DS36	Op Step Mode	LED I/S.	+5 Vdc	9-000C
A2DS37	Micro Step Mode	LED I/S.	+5 Vdc	9-000C

Table 5-5. Protective Device Index (See Paragraph 5-)

Reference Description	Front Panel Marking	Rating		Circuit Protected	Figure Number
		Volts	AMPS		
A1CB1	Circuit Breaker			AC Blowers, Alarm Buzzer, Running Time Meter, and Power Supply	9-000A

5-8. TROUBLESHOOTING PROCEDURES.

5-9. POWER. When troubleshooting the power circuits, check all primary power lines, switches and other circuit elements to determine whether the source of trouble is in the power distribution system or in the power supply itself.

5-10. Power Supply. If the power supply is suspected, use the voltage and test point data given in table 5-6 to check for proper operation. In the event the power supply is found defective, it must be exchanged with a replacement unit and returned to the factory, since it is not a field repairable item.

5-11. Power Distribution. If ac power is not being delivered correctly to the power supply, or if the power supply is operating correctly but dc power does not reach its destination, use figures 9-000A and B to check the ac and dc power distribution.

5-12. PANELS. Panel functions are normally tested and diagnosed as part of the regular running of the diagnostic test program*. If an individual switch or indicator is suspected, check its operation while measuring the voltage across its terminals with a multimeter of oscilloscope. The maintenance panel is hinged at the bottom and held by five screws. Opening it provides access to its wiring and the control panel wiring. Control and maintenance panel wiring appears on figure 9-000C.

5-13. BLOWERS. If an individual blower stops operating, it may not always cause an overtemperature fault, since air will be drawn through its chassis in a reverse direction by the two operating blowers. To test blower operation, place hand at each of the three air exhaust grilles on the left side of the cabinet to verify that air is being exhausted. Or place a sheet of paper in front of each exhaust grille; it will be repelled by the air flow from operaing blower and will be drawn against the grille by air flowing backward through a non-operating blower.

5-14. HEAT SENSORS. Each chassis contains two thermostats: S1 which in each case, is normally open and provides the overtemperature warning; and S2 which, in each case, is normally closed, and provides the overtemperature cut-off. Figure 9-000B shows the thermostats may be checked with a multimeter at terminal boards on each chassis. Refer to table 5-7.

* Not available at time of this publication.

Table 5-6. Power Supply Test Data

ITEM	TEST DATA	
AC Input Power	Refer to power distribution schematic diagrams, figures 9-000A and B for applicable terminals for checking ac input power at A2TB1 behind the maintenance panel or PS1TB1 on the power supply. WARNING Dangerous voltages are encountered in this check. Voltages should be 115 Vac ± 7% for single phase power and 115 Vac ± 5% for 3 phase power. Delta inputs are measured line to line and wye inputs line to neutral.	
Logic Output Voltages	VOLTAGE/TOLERANCE	TEST POINT
	+5 Vdc ± 5% Memory	PS1-TB4-6
	+5 Vdc ± 5% Processor	PS1-E9
	-5 Vdc ± 5%	PS1-TB4-4
	-5.2 Vdc ± 5%	PS1-TB3-3
	+12 Vdc ± 5%	PS1-TB3-3
	+15 Vdc ± 2%	PS1-TB4-2
	-16 Vdc ± 5%	PS1-TB3-5

Table 5-7. Thermostat Test Point

WARNING

These terminals carry 115 Vac if power is turned on.

CHASSIS	OVERTEMP ALARM S1 (NO)	OVERTEMP CUT-OFF S2 (NC)
A2 Memory	TB1-3,4	TB1-1,2
A3 CP/IO	TB1-6,7	TB1-3,5
PS1 Power Supply	TB2-1,2	TB2-3,5

5-15. MEMORY. The memory has no test points to facilitate manual testing, because it is thoroughly tested and diagnosed by the diagnostic test program, chapter 10, and the diagnostic procedures accompanying the program. If the memory is suspected and the diagnostic test program does not determine the trouble, it may be tested by replacing circuit cards with spares, or by swapping the position of identical cards, until the symptom disappears or shifts its position.

5-16. INPUT/OUTPUT. Diagnostic testing of the I/O circuits requires a special test I/O mode card which is supplied with each DPS. This card must be inserted into the DPS in place of the normal operational I/O mode card when running the diagnostic tests. Refer to Volume 3 (chapter 10) of this manual for instructions on the use of the special card. If manually troubleshooting the I/O circuits by replacing cards in the suspected area with spare cards or interchanging the positions of identical (multiple usage) cards, be careful to interchange only cards of the same type. Cards which may be interchanged depend on the I/O options installed. In order to be interchangeable, cards must be for the same type of interface and of the same interface voltage level.

CHAPTER 6

CORRECTIVE MAINTENANCE

6-1. INTRODUCTION.

6-2. This chapter covers corrective maintenance of the DPS. Corrective maintenance consists of replacement of faulty printed circuit cards, fuses, indicators, or other components. All LRI's (lowest replaceable items) for the DPS, except memory and power supply modules, are designed to be throwaway items. No adjustments are required.

6-3. REMOVAL AND REPLACEMENT PROCEDURES.

6-4. The following paragraphs describe the chassis and assembly removal procedures. Included are connector pin and indicator-switch replacement procedures. Table 6-1 provides a list of tools required but not supplied.

Table 6-1. Special Equipment and Tools Required But Not Supplied

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Oscilloscope	Tektronix Model 545A, AN/USM-281, AN/USM-140, or equivalent	Troubleshooting and maintenance	
1	Preamplifier, Dual Trace	Tektronix 1A2 or equivalent	Required with Oscilloscope	Dual Trace
1	AC Current Probe with Passive Terminator	Tektronix P6021 (015-0140-00) or equivalent	Required with Oscilloscope for memory read/ write current testing	Current Probe
1	Voltage Probe X1	Tektronix P6028 (010-0074-00) or equivalent	Required with Oscilloscope	Voltage Probe
2	Voltage Probe X10	Tektronix P6006 (010-0127-00) or equivalent	Required with Oscilloscope	Voltage Probe X10
1	Multimeter	Tripplett Model 630, AN/PSM-4(V) or equivalent	Troubleshooting and maintenance	

Table 6-1. Special Equipment and Tools Required But Not Supplied (Cont)

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Pin Inserter and Extractor Handle	Univac No. 8839225	Remove and insert wire wrap pins and bushings for card jacks and rear connector panel	Hand Operated
1	Adapter	Univac No. 8839224	Required with handle	
1	Tip, Insertion	Univac No. 8839226	Insert pins	
1	Tip, Extraction	Univac No. ETX 861690	Remove pins	
1	Wire Stripper	Ideal 45-171	Wire repair	Hand Operated
1	Stripper Blade	Ideal L5211		16-26 gauge
1	Stripper Blade	Ideal L5436		26-30 gauge
1	Low-Voltage Soldering Iron			
	Miscellaneous Hand Tools			
1	Wire Wrap Gun	Gardner-Denver 14R2	Logic and Connector wiring	Battery Operated
1	Power Pack for Wire Wrap Gun	Gardner-Denver 503885		Rechargeable
1	Wire-Wrap Bit	Gardner-Denver 26263	Logic Wiring	24 gauge (on large pin)
1	Wire-Wrap Bit	Gardner-Denver 501381	Logic Wiring	30 gauge (on large pin)
1	Wire-Wrap Bit	Gardner-Denver 504221	Logic Wiring	30 gauge (on small pin)
1	Wire-Wrap Sleeve	Gardner-Denver 18840	Logic Wiring	24 gauge (on large pin)
1	Wire-Wrap Sleeve	Gardner-Denver 17611-2	Logic Wiring	30 gauge (on large pin)
1	Wire-Wrap Sleeve	Gardner-Denver 500350	Logic Wiring	30 gauge (on small pin)

Table 6-1. Special Equipment and Tools Required But Not Supplied (Cont)

QTY PER EQUIP	NOMENCLATURE		REQUIRED USE	EQUIPMENT CHARACTERISTICS
	NAME	DESIGNATION		
1	Unwrap Tool	Gardner-Denver 500130	Logic Wiring	20-26 gauge
1	Unwrap Tool	Gardner-Denver 505244	Logic Wiring	30 gauge

6-5. POWER SUPPLY REMOVAL PROCEDURE. Listed below is the procedure to remove and replace the DPS power supply.

1. Turn off power and disconnect the power cable from connector J35.

2. Open front panel by loosening the eight retaining screws and swinging panel open.

3. Remove Phillips screw securing left hand bracket of telescoping door stop from front bottom edge of cabinet. This allows the front panel to open wider.

CAUTION

Ensure no stress is placed on the cables (J01-J04) to the maintenance panel. In case of stress, these cables must be unplugged and/or cable clamp removed.

4. With Phillips screwdriver, disengage four quick-release memory chassis fasteners. Pull out the memory chassis assembly and swing it open to the left.

5. Remove ribbon cable cover (four Phillips screws) located on the lower right bottom of cabinet.

6. Remove memory fastening block located at lower right front corner of cabinet. It is held with four Phillips screws accessible from outside of cabinet.

7. Unplug and tag the six CP/IO chassis paddle boards (ribbon cable cards) from CP/IO chassis rows A and C, slots 1, 2, and 3. Remove ribbon cable from behind cable holder located left front of power supply.

8. Remove four bottom bolts (7/16" wrench) securing power supply to the cabinet.

9. Remove and tag all wires on TB1 through TB5, located on front of power supply. TB1 and TB2 have removable covers.

10. Remove and tag wires from terminals E9 and E10, located on front of power supply.

11. Ensure cabinet is firmly fastened down or held in place. Grasp power supply handle, located on bottom center of supply, pull unit forward, and remove from cabinet.

12. To gain access to the interior of the power supply, remove the 18 screws securing the top panel to the supply frame.

6-6. CP/IO CHASSIS REMOVAL PROCEDURE. Listed below is the procedure to remove and replace the DPS CP/IO chassis.

1. Turn off power and disconnect the power cable from connector J35.

2. Remove and tag all cables from the connector panel located on the rear of the CP/IO chassis (connectors extend through rear panel of cabinet).

3. Open front panel per paragraph 6-5, steps 2 and 3.

4. With Phillips screwdriver, disengage four quick-release memory chassis fasteners. Pull out the memory chassis assembly and swing it to the left.

5. Unplug and tag the six CP/IO chassis paddle boards (ribbon cable cards) from CP/IO chassis rows A and C, slots 1, 2, and 3.

6. Remove all cards of CP/IO chassis center row B, using card extractor. Set cards aside stacked in sequence.

7. Using a spintite, remove the four nuts holding the cover for TB1, located in row B.

8. Using a 5/16" wrench, remove the cable clamp holding the ac power wires to TB1.

9. Remove and tag all wires on TB1.

10. Remove eight Phillips head screws securing CP/IO chassis to cabinet.

CAUTION

When removing CP/IO chassis, do not let it fall into the lower part of the cabinet.

11. Pull forward on CP/IO chassis and remove it from the cabinet.

12. Replace the CP/IO chassis by reversing the above procedure.

6-7. POWER SUPPLY BLOWER REMOVAL PROCEDURE. To remove the power supply blower, use the following procedure.

1. Perform the power supply removal procedure, paragraph 6-5.

2. Remove the 12 Phillips screws around the power supply blower vent (located on lower rear portion of left side of cabinet). Pull assembly loose from cabinet.

3. Remove and tag the three power wires on the blower assembly.

4. Remove the four Phillips screws holding the blower assembly to the vent grill, and remove blower.

5. Replace the power supply blower unit by reversing steps 1 through 4 above.

6-8. CP/IO CHASSIS BLOWER REMOVAL PROCEDURE. To remove the CP/IO chassis blower, use the following procedure.

1. Perform the CP/IO chassis removal procedure, paragraph 6-6.

2. Remove the 17 screws holding the CP/IO chassis blower cover.

3. Remove and tag the power wires to the blower.

4. Remove the four screws holding the blower assembly to the CP/IO chassis.

5. To replace the blower, reverse steps 1 through 4 above.

6-9. MEMORY CHASSIS BLOWER REMOVAL PROCEDURE. To remove the memory chassis blower, use the following procedure.

1. Open cabinet and extend memory chassis per paragraph 6-5, steps 1-4.

2. Remove and tag three power wires located at lower left corner of blower assembly.

3. Remove four Phillips screws located at blower assembly corners.

4. Pull blower assembly straight out.

5. Replace blower assembly by reversing steps 1 through 4 above.

6-10. MEMORY BOARD ACCESS. To gain access to the DPS memory chassis boards, use the following procedure.

1. Open cabinet and extend memory chassis per paragraph 6-5, steps 1-4.

2. Remove the eight screws securing the chassis end panel (perforated panel facing forward); remove the panel, providing access to the boards.

3. Engage right-hand and left-hand card extractors (table 1-2) into holes at top and bottom edges of selected memory board; press to loosen and remove board.

4. To replace the unit, reverse steps 1 through 3 above.

6-11. INDICATOR-SWITCH REPLACEMENT. To replace faulty switches or indicator-switches in the maintenance panel or control panel, use the following procedure.

1. Shut off power and disconnect the power cable from connector J35.

2. Open front panel by loosening the eight retaining screws, and swinging open.

3. Loosen the five screws securing the maintenance panel to the door.

4. Pull the top of the maintenance panel forward to swing it down on its hinge, exposing the rear of both the maintenance panel and the control panel.

5. Remove and tag wires from faulty component, referring to either the wire wrap procedure or the solder procedure depending on how the wires are secured.

6. Loosen and remove the knurled ring (located on front of panel) securing the component to the panel.

7. Replace the faulty component with a new component of the same part number.

8. Reverse above procedure to close and secure panel assembly.

6-12. CP/IO CONNECTOR PIN REPLACEMENT. To replace pins in the CP/IO circuit card connectors or in the I/O connectors located on the back of the CP/IO chassis, use the following procedure.

1. Perform CP/IO chassis removal procedure, paragraph 6-6.

2. Remove CP/IO blower assembly panel per paragraph 6-8.

3. Remove screws securing CP/IO back connector panel; open panel to provide access to wire wrap side of connectors.

4. Remove the wire from the connector pin by following step 1 of wire wrap procedure, paragraph 6-15.

6. Using inserter/extractor handle (Univac No. 8839225, table 6-1), adapter (Univac No. 8839224), and extraction tip (Univac No. ETX 861690); remove the faulty pin.

7. Using inserter/extractor handle (Univac No. 8839225), adapter (Univac No. 8839224), and insertion tip (Univac No. 8839226); insert a new connector pin.

8. Follow wire wrap procedure, steps 2 through 6, to connect wire to new pin.

9. Close connector panel.

10. Replace unit by reversing procedures in steps 1 through 3 above.

6-13. WIRE WRAPPING. Wire connections to connector terminals of the DPS are made by wrapping several turns of wire around the post. Each terminal post has a rectangular cross section. The wrapped connections form helical coils on the posts, with points of contact at each of the four corners. Two connections may be made at each post, the second connection being wrapped around the upper portion (level)

of the post. If a lower level wire must be removed, remove the upper level first to gain access.

6-14. Two commercial tools are used to replace defective wires: a manually operated wire-wrap tool for removal of the old wires, and a battery-operated wire-wrap gun, with a detachable rechargeable battery which forms the handle, for installation of the new wires. The wire-wrap gun is used in conjunction with various size bits and sleeves to position the wire over the terminal post and accomplish the wrap. The size of the wire to be wrapped determines the bit and sleeve size that must be used. Refer to table 6-1 for the various size bits and sleeves.

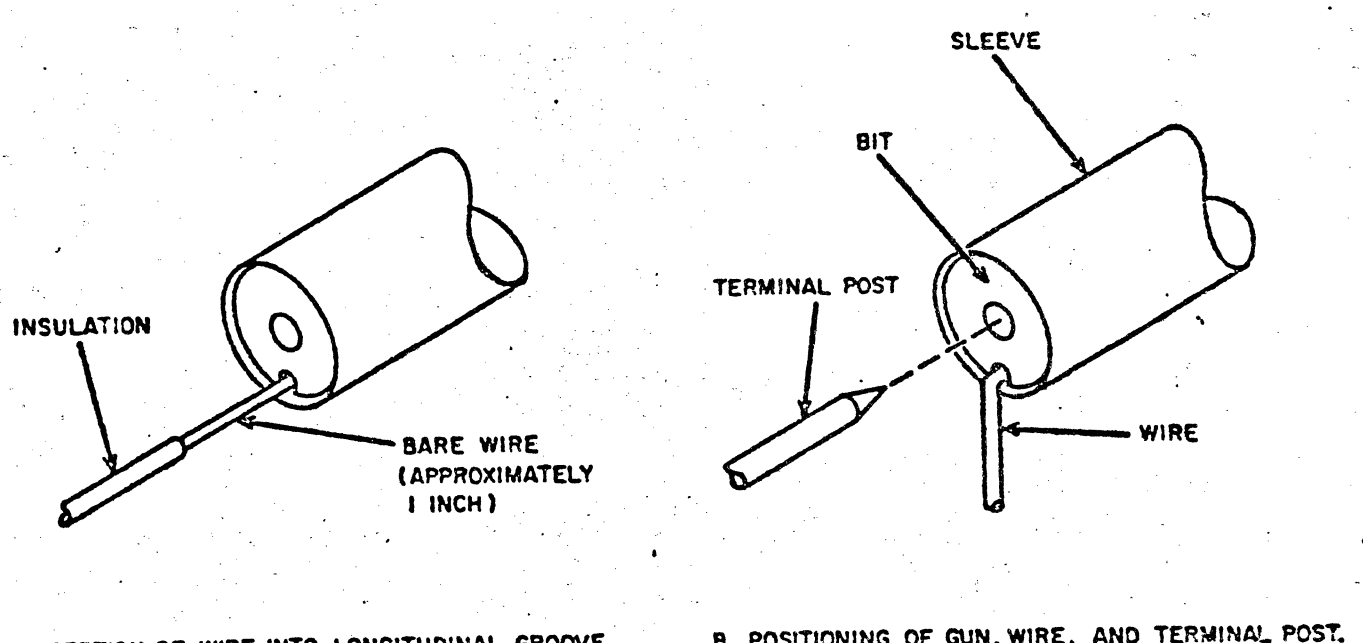
6-15. To replace defective wires, perform the following steps:

1. Remove old wire by placing barrel of wire-unwrap tool over terminal post and twisting tool in a direction opposite to that of the wire wrap.

2. Remove approximately one inch of insulation from replacement wire, being careful not to nick bare area of wire.

3. Use wire-wrap sleeve and bit corresponding to size of wire. Place sleeve and bit in wire-wrap gun.

4. Insert bare portion of replacement wire into longitudinal groove of bit. Edge of wire insulation must touch end of bit (figure 6-1).



A. INSERTION OF WIRE INTO LONGITUDINAL GROOVE.

B. POSITIONING OF GUN, WIRE, AND TERMINAL POST.

Figure 6-1. Preparation for Wire Wrapping

5. Bend wire so insulated portion is at right angle to longitudinal groove of bit (figure 6-1).

6. Position wire-wrap gun over terminal post, with terminal post inserted in bit, and press trigger. Wire-wrap gun supplies necessary power to make wrap. Complete at least four complete turns around post with wire. Wire must be evenly applied, without overlapping of turns or gaps between turns (figure 6-2).

NOTE

Do not wire-wrap with a gun that does not have fully charged batteries. Recharging the battery is accomplished by twisting the handle 90° counterclockwise and inserting it into a conventional 115 Vac, 60 Hz, single-phase electrical outlet for 12 hours.

6-16. SOLDER CONNECTIONS. Normal soldering techniques employed for electronic component replacement and repair should be applied when removing or forming solder connections.

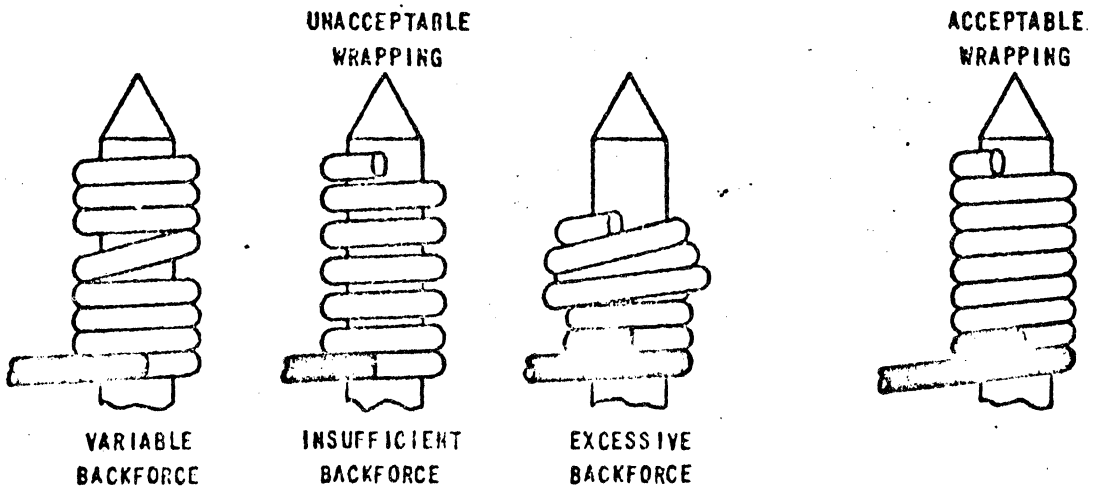


Figure 6-2. Wire Wrap Connections

CHAPTER 7

PARTS LIST

7-1. INTRODUCTION.

7-2. The Parts List identifies units, assemblies, and detail parts for the Data Processing Sets AN/UYK-20(V) and AN/UYK-20X(V). The parts list contains fifteen (15) optional units and eleven (11) kits. A given Data Processing Set does not contain all major units, therefore to aid the user in locating parts table 7-2 is subdivided into separate parts lists with identical parts repeated for each unit.

7-3. LIST OF MAJOR UNITS.

7-4. Table 7-1 is a tabular listing of the major units comprising this equipment. The first column lists the unit numbers in numerical order. Table 7-1 also provides the name of unit, designation and location of first page of its parts listing in table 7-2.

7-5. PARTS LIST.

7-6. Table 7-2 lists the units and their repairable parts. This list is divided and arranged by major units in numerical sequence. Parts attached to the unit are listed first in alpha-numerical order, followed by unit assemblies with parts also listed in alpha-numerical order. Column 1 contains the reference designations of all parts listed in sequential order. Replaceable components not reference designated are listed after their next higher assembly or at the end of each unit. The notes column is not used for this equipment. Column 3 consists of the noun name or item name and electrical or physical characteristics to identify the parts within the equipment. Following this description, part manufacturer's Federal supply code number, manufacturer's part number, contractor's Federal supply code number, contractor's drawing number or military type designation, as applicable, are included. Identical parts that are used more than five times in a given unit are listed with "Same as ___" and referenced to the item number in table 7-3 List of Common Item Descriptions. The attaching hardware, with quantity required, is identified by an assigned letter code and listed immediately following the item which they secure. The figure and item number (column 4) identifies the illustration which pictorially locates the part by listing the figure number with item number enclosed in parenthesis.

7-7. LIST OF COMMON ITEM DESCRIPTIONS.

7-8. Table 7-3 is a list of like parts that are used over five applications. The parts are grouped and arranged in alphabetical order with item numbers assigned consecutively. The description is the same as shown in table 7-2.

7-9. LIST OF ATTACHING HARDWARE.

7-10. Table 7-4 contains a list of all the attaching hardware referenced in table 7-2. These items are grouped and arranged in alphabetical order with letter codes assigned consecutively.

7-11. LIST OF MANUFACTURERS.

7-12. Table 7-5 is a list of manufacturers containing the names, addresses, and code symbol of all manufacturers supplying items for the equipment as referenced in the parts list.

7-13. PARTS LOCATION ILLUSTRATIONS.

7-14. Suitable parts location illustrations located in other chapters of the manual are referenced and not repeated. Illustrations provided only for locating parts are placed at the end of this chapter.

Table 7-1. List of Major Units

UNIT NO.	NAME OF UNIT	DESIGNATION	PAGE NO.
1	Cabinet, Electrical Equipment	CY- /UYK-20(V)	
2	Cabinet, Electrical Equipment	CY- /UYK-20X(V)	
3	Control-Maintenance Unit	C- /UYK-20(V)	
4	Control-Maintenance Unit	C- /UYK-20X(V)	
5	Power Supply	PP-7032/UYK-20(V)	
6	Power Supply	PP- /UYK-20(V)	
7	Power Supply	PP- /UYK-20(V)	
8	Power Supply	PP- /UYK-20X(V)	
9	Power Supply	PP- /UYK-20X(V)	
10	Power Supply	PP- /UYK-20X(V)	
11	Processor-Verifier Unit	CP- (P)/UYK-20(V)	
12	Processor-Verifier Unit	CP- (P)/UYK-20X(V)	
13	Core Memory Unit	MU-604/UYK-20(V)	
14	Control, Core Memory	C- (P)/UYK-20(V)	
15	Control, Core Memory	C- (P)/UYK-20X(V)	
16	Interface Kit, Fast Serial	MK- /UYK-20(V)	
17	Interface Kit, Serial Sync	MK- /UYK-20(V)	
18	Interface Kit, Serial Async	MK- (V)/UYK-20(V)	
19	Interface Kit, Serial Communications, Sync	MK- /UYK-20(V)	
20	Interface Kit, Serial Communications, Async	MK- (V)/UYK-20(V)	
21	Interface Kit, Slow	MK-1693/UYK-20(V)	
22	Interface Kit, Fast, Negative	MK-1694/UYK-20(V)	
23	Interface Kit, Fast, Positive	MK-1695/UYK-20(V)	

Table 7-1. List of Major Units (Cont)

UNIT NO.	NAME OF UNIT	DESIGNATION	PAGE NO.
24	Micro Memory Program Kit	MK- (V)/UYK-20(V)	
25	Maintenance Kit	MK- /UYK-20(V)	
26	Accessory Kit	MK- /UYK-20(V)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
Cabinet, Electrical Equipment CY- /UYK-20(V) (Unit 1)			
1		CABINET ELECTRICAL EQUIPMENT CY- /UYK-20(V): Provides mounting for units of Data Processing Set AN/UYK-20(V), designed for shipboard and ground use; mfr 90536, part no. 7101970-00.	
1B1		FAN, AXIAL: Cw rotation, aluminum case, 4.688 in. sq, 1.5 in. dia, MS 32877, part no. 810DS TYPE ST, 90536, dwg 7901420-01. (Attaching Parts) U(4), X(2), AH(2), BB(4), BC(4), BE(4), BF(6)	
1A1		CONTROL-MAINTENANCE UNIT: See unit no. 3.	
1A2		CORE MEMORY UNIT: See unit no. 13.	
1A3		PROCESSOR-VERIFIER UNIT: See unit no. 11.	
1A4		FILTER ASSEMBLY, ELECTRICAL: Contains 4 filters and 1 connector; mfr 90536, part no. 7101950-00. (Attaching Parts) BJ(8), BJ(8)	
1A4FL1 thru 1A4FL4		FILTER, RADIO FREQUENCY INTERFERENCE: T circuit rfi filter, 125vac, 12amp; mfr 56289, part no. JN17-4564A, 90536, dwg 7904734-00.	
1A4J1		CONNECTOR, RECEPTACLE, ELECTRICAL: Male 7-contact; MIL type MS3102R20-15P. (Attaching Parts) G(4), AA(4), AU(4), BB(4)	
1A5		not used	
1A6		ELECTRONIC COMPONENTS ASSEMBLY: Contains 1 capacitor, 1 terminal board, and 2 terminals; mfr 90536, part no. 7126335-00 (Attaching Parts) AH(2), BI(2)	
1A6C1		CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.0UF, ±10%, 400VDCW; mfr 56289, part no. 260P10594S2, 90536, dwg 7903001-11.	
1A6E1 1A6E2		TERMINAL, STUD: Insulated, stand off, threaded /2 turret; mfr 71279, part no. 570-3650-02-05, 90536, dwg 910185-02. (Attaching Parts) V(2)	
1A6TB1		TERMINAL BOARD: Barrier type, 3 terminals; mfr 75382, part no. 600AY3, 90536, dwg 904862-04. (Attaching Parts) I(4), AG(2), AJ(2), BC(2), BI(6)	
1A7		RESISTOR ASSEMBLY, FIXED: Contains 3 resistors; mfr 90536, part no. 7128008-00. (Attaching Parts) AH(2), BI(2)	
1A7R1 thru 1A7R3		RESISTOR, FIXED, COMPOSITION: 100K ohm, ±5%, 1/2W; MIL type RCR20G104JM.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
1 (Cont.)		CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 16AWG, 13 amp rating; mfr 81312, part no. 10051016S994, 90536, dwg 4910566-01 (8). CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 24AWG, 13 amp rating; mfr 81312, part no. 10051024S994, 90536, dwg 4910566-05 (6). CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 26 to 30AWG, 13 amp rating; mfr 81312, part no. 10051026S994, 90536, dwg 4910566-08 (4).	
Cabinet, Electrical Equipment CY- /UYK-20X(V) (Unit 2)			
2		CABINET ELECTRICAL EQUIPMENT CY- /UYK-20X(V): Provides mounting for units of Data Processing Set AN/UYK-20X(V), designed for shipboard and ground use; mfr 90536, part no. 7101970-01.	
2B1		FAN, AXIAL: Cw rotation, aluminum case, 4.688 in. sq., 1.5 in. thick; mfr 82877, part no. 682YS TYPE ST, 90536, dwg 7901420-03. (Attaching Parts) G(4), I(4), X(2), AH(2), BB(4), BC(4), BH(4), BI(6)	
2A1		CONTROL-MAINTENENCE UNIT: See unit no. 4.	
2A2		CORE MEMORY UNIT: See unit no. 13.	
2A3		PROCESSOR-VERIFIER UNIT: See unit no. 12.	
2A4		FILTER ASSEMBLY, ELECTRICAL: Contains 4 filters and 1 connector; mfr 90536, part no. 7101950-01. (Attaching Parts) AL(8), BJ(8)	
2A4FL1 thru 2A4FL4		FILTER, RADIO FREQUENCY INTERFERENCE: T circuit rfi filter, 125vac, 12amp; mfr 56289, part no. JN17-4564A, 90536, dwg 7904734-00.	
2A4J1		CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 7-contact; MIL type MS3102R20-15PZ. (Attaching Parts) G(4), AA(4), AU(4), BB(4)	
2A5		not used	
2A6		ELECTRONIC COMPONENTS ASSEMBLY: Contains 1 capacitor, 1 terminal board, and 2 terminals; mfr 90536, part no. 7126335-01. (Attaching Parts) AH(2), BI(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
2A6C1		CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.39UF, ±10%, 400VDCW; mfr 56289, part no. 260P39494S2, 90536, dwg 7903001-33.	
2A6E1 2A6E2		TERMINAL, STUD: Insulated, stand off, threaded /2 turret; mfr 71279, part no. 570-3650-02-05, 90536, dwg 910185-02. (Attaching Parts) V(2)	
2A6TB1		TERMINAL BOARD: Barrier type, 3 terminals; mfr 75382, part no. 600AY3, 90536, dwg 904862-04. (Attaching Parts) I(4), AG(2), AJ(2), BC(2), BI(6)	
2A7		RESISTOR ASSEMBLY, FIXED: Contains 3 resistors; mfr 90536, part no. 7128008-00. (Attaching Parts) AH(2), BI(2)	
2A7R1 thru 2A7R3		RESISTOR, FIXED, COMPOSITION: 100K ohm, ±5%, 1/2W; MIL type RCR20G104JM.	
		CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 16AWG, 13 amp rating; mfr 81312, part no. 10051016S994, 90536, dwg 4910566-01 (8).	
		CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 24AWG, 13 amp rating; mfr 81312, part no. 10051024S994, 90536, dwg 4910566-05 (6).	
		CONTACT, ELECTRICAL CONNECTOR: Female, removable, for rack and panel connectors, 0.764 in. long, 26 to 30AWG, 13 amp rating; mfr 81312, part no. 10051026S994, 90536, dwg 4910566-08 (4).	
Control-Maintenance Unit C- /UYK-20(V) (Unit 3)			
3		CONTROL-MAINTENANCE UNIT C- /UYK-20(V): Evaluates performance and provides control and visual monitoring of internal functions of the Data Processing Set AN/UYK-20(V), operating power 115 VAC, 400HZ, 3-phase delta or 208 VAC, 400HZ, 3-phase wye or 115 VAC, 400HZ, single phase; mfr 90536, part no. 7101985-00.	
3LS1		HORN, ELECTRICAL: With solid state oscillator, 1.7 in. dia, 30-120 volt; mfr 37942, part no. SC110Z W/ALMTGRING, 90536, dwg 7904742-00. (Attaching Parts) AC(2), BH(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
3A1		CONTROL PANEL ASSEMBLY: Contains 1 circuit breaker, 7 indicators, and 8 switches; mfr 90536, part no. 7101985-00. (Attaching Parts) R(12), AH(12), BI(12)	
3A1CB1		CIRCUIT BREAKER, MAGNETIC: 3 poles, 20 amp, 240V, 400HZ; MIL type M39019/5-80. (Attaching Part) N(1)	
3A1DS1 3A1DS2		LIGHT, INDICATOR: Neon, w/resistor, red sealed lens, RFI shielding; mfr 07137, part no. SIL8062A25, 90536, dwg 7904735-20. (Attaching Part) BF(2)	
3A1DS3		LIGHT, INDICATOR: Light emitting diode, w/resistor, sealed green lens; mfr 07137, part no. SSIL8066A33C, 90536, dwg 7904467-14. (Attaching Parts) L(1), BF(1)	
3A1DS4 3A1DS5		LIGHT INDICATOR: Light emitting diode, w/resistor, sealed clear lens; mfr 07137, part no. SSIL8059A22, 90536, dwg 7904279-12. (Attaching Parts) L(2), BF(2)	
3A1DS6		LIGHT, INDICATOR: Incandescent, w/75 ohm resistor, non-replaceable lamp, 5 V, 0.06 amp, sealed white lens; mfr 07137, part no. SIL8065A32, 90536, dwg 7904806-00. (Attaching Parts) L(1), BF(1)	
3A1DS7		LIGHT, INDICATOR: Neon, w/resistor, sealed white lens, RFI shielding; mfr 07137, part no. SIL8062A32, 90536, dwg 7904735-23. (Attaching Part) BF (1)	
3A1S1		SWITCH, TOGGLE: Minature, dpdt, sealed; MIL type MS24656-231. (Attaching Part) L(1)	
3A1S2		SWITCH, TOGGLE: Minature, dpdt, sealed; MIL type MS24656-311. (Attaching Part) L(1)	
3A1S3		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS24655-231. (Attaching Part) L(10)	
3A1S4		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS24655-271. (Attaching Part) L(1)	
3A1S5 3A1S6		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS24655-281. (Attaching Part) L(2)	
3A1S7		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS24655-221. (Attaching Part) L(1)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
3A1S8		SWITCH, TOGGLE: Subminature, sealed, 3 pole; mfr 31356, part no. T04-323, 90536, dwg 7904733-01. (Attaching Parts) L(1), BF(1)	
3A2		PANEL ASSEMBLY, MAINTENANCE: Contains 1 indicator, 4 connectors, 1 relay, 1 meter, 47 switches, and 1 terminal board; mfr 90536, part no. 7101850-00. (Attaching Parts) R(6), AH(6), BI(12)	
3A2DS1		LIGHT, INDICATOR: Light emitting diode, w/resistor, clear lens; mfr 07137, part no. SSIL8722C22, 90536, dwg 7904279-00. (Attaching Parts) K(1), BK(1)	
3A2J01 3A2J02 3A2J03		CONNECTOR BLOCK: Contains 120 terminal assemblies; mfr 90536, part no. 7101817-00. (Attaching Part) AR(4)	
3A2J04		INSULATOR, ELECTRICAL CONNECTOR: Male, rectangular, 20 contact locations; mfr 81312, part no. MRAC20PJ6-436, 90536, dwg 4911532-00.	
3A2K1		RELAY, ARMATURE: 3 SPST, 115 VAC, 400HZ; MIL type MS27418-1A.	
3A2M1		METER, TIME TOTALIZING: 115V, 400HZ, 9999 hour elapsed time, square case; MIL type MS17322-10. (Attaching Parts) P(2), AS(2), BC(2)	
3A2S1		SWITCH, PUSH: SPST normally open double break, 0.1 amp, white button; mfr 07137, part no. SBS8732B26, 90536, dwg 7904277-00. (Attaching Parts) K(3), BK(3)	
3A2S2 3A2S3 3A2S4		SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 amp, clear lens; mfr 07137, part no. SSBL8721C22, 90536, dwg 7904278-00. (Attaching Parts) K(24), BK(24)	
3A2S5 3A2S6 3A2S7		SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 amp, clear lens; mfr 07137, part no. SSBL8774C22, 90536, dwg 7904278-03. (Attaching Parts) M(7), BK(7)	
3A2S8		Same as 3A2S2 (item no. 22)	
3A2S9 3A2S10			
3A2S11		Same as 3A2S5 (item no. 23)	
3A2S12 3A2S13			

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
3A2S14		Same as 3A2S2 (item no. 22)	
3A2S15			
3A2S16			
3A2S17		Same as 3A2S5 (item no. 23)	
3A2S18		Same as 3A2S2 (item no. 22)	
3A2S19			
3A2S20		SWITCH, PUSH; SPST normally open double break, light emitting diode indicator, 0.1 amp, green lens; mfr 07137, part no. SSBL8025A33C, 90536, dwg 7904466-07. (Attaching Parts) K(1), BK(1)	
3A2S21		Same as 3A2S1 (item no. 21)	
3A2S22 thru 3A2S31		Same as 3A2S2 (item no. 22)	
3A2S32		Same as 3A1S3 (item no. 25)	
3A2S33			
3A2S34			
3A2S35		Same as 3A2S2 (item no. 22)	
3A2S36			
3A2S37			
3A2S38		Same as 3A1S3 (item no. 25)	
3A2S39			
3A2S40		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS24655-211. (Attaching Parts) K(1)	
3A2S41		Same as 3A1S3 (item no. 25)	
3A2S42			
3A2S43		SWITCH, TOGGLE: DPDT, minature, panel sealed; MIL type MS21352-351. (Attaching Parts) K(1)	
3A2S44		SWITCH, TOGGLE: Minature, single pole, panel sealed; MIL type MS21350-321. (Attaching Parts) K(1)	
3A2S45		Same as 3A2S1 (item no. 21)	
3A2S46		Same as 3A1S3 (item no. 25)	
3A2S47			
3A2TB1		TERMINAL BOARD: Barrier type, 14 terminals; mfr 71785, part no. 354-11-14-001, 90536, dwg 900125-16. (Attaching Parts) AI(2), BI(2)	
		CONTACT, ELECTRICAL CONNECTOR: Male, removable, for rack and panel connectors, 0.764 in. long, 16AWG, 13 amp rating; mfr 81312, part no. 1001016P159, 90536, dwg 4910565-01 (8).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
3 (Cont.)		CONTACT, ELECTRICAL CONNECTOR: Male, removable, for rack and panel connectors, 0.764 in. long, 24AWG, 13 amp rating; mfr 81312, part no. 1001024P159, 90536, dwg 4910565-05 (6). CONTACT, ELECTRICAL CONNECTOR: Male, removable, for rack and panel connectors, 0.764 in. long, 26 to 30 AWG, 13 amp rating; mfr 81312, part no. 1001026P159, 90536, dwg 4910565-08 (4). FILTER, AIR CONDITIONING: Aluminum, oiled type, 15.5 in. long, 9 in. wide, 0.5 in thick, type R82A; mfr 00736, part no. 124786-219, 90536, dwg 910486-20 (1). FILTER: EMI large; mfr 90536, part no. 7101913-00 (1).	
Control Maintenance Unit C- /UYK-20X(V) (Unit 4)			
4		CONTROL-MAINTENANCE UNIT C- /UYK-20X(V): Evaluates performance and provides control and visual monitoring of internal functions of the Data Processing Set AN/UYK-20X(V), operating power 115 VAC, 60HZ, 3-phase delta or 208 VAC, 60HZ, 3-phase wye or 115 VAC, 60HZ, single phase; mfr 90536, part no. 7101985-01.	
4LS1		HORN, ELECTRICAL: With solid state oscillator, 1.7 in. dia, 30-130 volt; mfr 37942, part no. SC110Z W/ALMTGRING, 90536, dwg 7904742-00. (Attaching Parts) AC(2), BH(2)	
4A1		CONTROL PANEL ASSEMBLY: Contains 1 circuit breaker, 7 indicators, and 8 switches; mfr 90536, part no. 7101985-01. (Attaching Parts) R(12), AH(12), BI(12)	
4A1CB1		CIRCUIT BREAKER, MAGNETIC: 3 poles, 20 amp, 240V, 60HZ; MIL type M39019/5-78. (Attaching Part) N(1)	
4A1DS1 4A1DS2		LIGHT, INDICATOR: Neon, w/resistor, red sealed lens, RFI shielding; mfr 07137, part no. SIL8062A25, 90536, dwg 7904735-20. (Attaching Part) BF(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
4A1DS3		LIGHT, INDICATOR: Light emitting diode, w/resistor, sealed green lens; mfr 07137, part no. SSIL8066A33C, 90536, dwg 7904467-14. (Attaching Parts) L(1), BF(1)	
4A1DS4 4A1DS5		LIGHT, INDICATOR: Light emitting diode, w/resistor, sealed clear lens; mfr 07137, part no. SSIL8059A22, 90536, dwg 7904279-12. (Attaching Parts) L(2), BF(2)	
4A1DS6		LIGHT, INDICATOR: Incandescent, w/75 ohm resistor, non-replaceable lamp, 5V, 0.06 amp, sealed white lens; mfr 07137, part no. SIL8065A32, 90536, dwg 7904806-00. (Attaching Parts) L(1), BF(1)	
4A1DS7		LIGHT, INDICATOR: Neon, w/resistor, sealed white lens, RFI shielding; mfr 07137, part no. SIL8062A32, 90536, dwg 7904735-23. (Attaching Parts) BF(1)	
4A1S1		SWITCH, TOGGLE: Miniature, dpdt, sealed; MIL type MS24656-231. (Attaching Part) L(1)	
4A1S2		SWITCH, TOGGLE: Miniature, dpdt, sealed; MIL type MS24656-311. (Attaching Part) L(1)	
4A1S3		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-231. (Attaching Part) L(10)	
4A1S4		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-271. (Attaching Part) L(1)	
4A1S5 4A1S6		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-281. (Attaching Part) L(2)	
4A1S7		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-221. (Attaching Part) L(1)	
4A1S8		SWITCH, TOGGLE: Subminiature, sealed, 3 pole; mfr 31356, part no. T04-323, 90536, dwg 7904733-01. (Attaching Parts) L(1), BF(1)	
4A2		PANEL ASSEMBLY, MAINTENANCE: Contains 1 indicator, 4 connectors, 1 relay, 1 meter, 47 switches, and 1 terminal board; mfr 90536, part no. 7101850-01. (Attaching Parts) R(6), AH(6), BI(12)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
4A2DS1		LIGHT, INDICATOR: Light emitting diode, w/resistor, clear lens; mfr 07137, part no. SSIL8722C22, 90536, dwg 7904279-00. (Attaching Parts) K(1), BK(1)	
4A2J01 4A2J02 4A2J03 4A2J04		CONNECTOR BLOCK: Contains 120 terminal assemblies; mfr 90536, part no. 7101817-00. (Attaching Part) AR(4) INSULATOR, ELECTRICAL CONNECTOR: Male, rectangular, 20 contact locations; mfr 81312, part no. MRAC20PJ6-436, 90536, dwg 4911532-00.	
4A2K1		RELAY, ARMATURE: 3 SPST, 115 VAC, 400HZ; MIL type MS27418-1A.	
4A2M1		METER, TIME TOTALIZING: 115V, 60HZ, 9999 hour elapsed time, square case, mfr 82227, part no. K19603B6, 90536, dwg 7903922-01. (Attaching Parts) P(2), AS(2), BC(2)	
4A2S1		SWITCH, PUSH: SPST normally open double break, 0.1 amp, white button; mfr 07137, part no. SBS8732B26, 90536, dwg 7904277-00. (Attaching Parts) K(3), BK(3)	
4A2S2 4A2S3 4A2S4		SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 amp, clear lens; mfr 07137, part no. SSBL8721C22, 90536, dwg 7904278-00. (Attaching Parts) K(24), BK(24)	
4A2S5 4A2S6 4A2S7		SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 amp, clear lens; mfr 07137, part no. SSBL8774C22, 90536, dwg 7904278-03. (Attaching Parts) M(7), BK(7)	
4A2S8		Same as 4A2S2 (item no. 22)	
4A2S9 4A2S10 4A2S11		Same as 4A2S5 (item no. 23)	
4A2S12 4A2S13 4A2S14		Same as 4A2S2 (item no. 22)	
4A2S15 4A2S16 4A2S17		Same as 4A2S5 (item no. 23)	
4A2S18		Same as 4A2S2 (item no. 22)	
4A2S19			

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
4A2S20		SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, 0.1 amp, green lens; mfr 07137, part no. SSBL8025A33C, 90536, dwg 7904466-07. (Attaching Parts) K(1), BK(1)	
4A2S21		Same as 4A2S1 (item no. 21)	
4A2S22 thru 4A2S31		Same as 4A2S2 (item no. 22)	
4A2S32		Same as 4A1S3 (item no. 25)	
4A2S33 thru 4A2S34			
4A2S35		Same as 4A2S2 (item no. 22)	
4A2S36 thru 4A2S37			
4A2S38		Same as 4A1S3 (item no. 25)	
4A2S39			
4A2S40		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-211. (Attaching Parts) K(1)	
4A2S41		Same as 4A1S3 (item no. 25)	
4A2S42			
4A2S43		SWITCH, TOGGLE: DPDT, miniature, panel sealed; MIL type MS21352-351. (Attaching Parts) K(1)	
4A2S44		SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS21350-321. (Attaching Parts) K(1)	
4A2S45		Same as 4A2S1 (item no. 21)	
4A2S46		Same as 4A1S3 (item no. 25)	
4A2S47			
4AT B1		TERMINAL BOARD: Barrier type, 14 terminals; mfr 71785, part no. 354-11-14-001, 90536, dwg 900125-16. (Attaching Parts) AI(2), BI(2)	
		CONTACT, ELECTRICAL CONNECTOR: Male, removable, for rack and panel connectors, 0.764 in. long, 16AWG, 13 amp rating; mfr 81312, part no. 1001016P159, 90536, dwg 4910565-01 (8).	
		CONTACT, ELECTRICAL CONNECTOR: Male, removable, for rack and panel connectors, 0.764 in. long, 24AWG, 13 amp rating; mfr 81312, part no. 1001024P159, 90536, dwg 4910565-05 (6).	
		Contact, electrical connector: Male, removable, for rack and panel connectors, 0.764 in. long, 26 to 30 AWG, 13 amp rating; mfr 81312, part no. 1001026P159, 90536, dwg 4910565-08 (4).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
Power Supply PP-7032/UYK-20(V) (Unit 5)			
5		POWER SUPPLY PP-7032/UYK-20(V): Provides power to each of the units within the data processor cabinet, operating power 115V, 400HZ, 3-phase delta; mfr 90536, part no. 7101840-00.	
5L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
5P1 5P2		CONNECTOR, PLUG, ELECTRICAL: Male; mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	
5T1		TRANSFORMER ASSEMBLY: Mfr 90536, part no. 7126376-00. (Attaching Parts) AN(6), AX(6), BE(6)	
5TB1		not used	
5TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) I(2), AI(2), AV(2), BC(2), BI(2)	
5A1		ELECTRONIC COMPONENTS ASSEMBLY: 3-phase, 400HZ, contains 3 capacitors and 1 choke; mfr 90536, part no. 7101982-00. (Attaching Parts) AN(4), AX(4), BE(4)	
5A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 680UF, ±15%, 250V; MIL type CE71C681M. (Attaching Parts) AN(2), BE(2)	
5A1C2 5A1C3		CAPACITOR, FIXED ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.	
5A1L1		PLATE ASSEMBLY, CHOKE: Mfr 90536, part no. 7101987-00. (Attaching Parts) AJ(4), AV(4)	
5A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
5A2TB1 5A2TB2 5A2TB3 5A2TB4		not used TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11. (Attaching Parts) AE(8), BC(8), BH(8)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
5A2TB5		TERMINAL BOARD: Barrier type, 4 terminals; mfr 75382, part no. 600AY4, 90536, dwg 904862-05. (Attaching Parts) AE(4), BC(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 19 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no. 7101932-00. (Attaching Parts) I(4), BI(4)	
5A3		FILTER ASSEMBLY, INPUT: 6 capacitors and 9 chokes mtd in chassis, epoxyed; mfr 90536, part no. 7101979-00. (Attaching Parts) AN(4), AX(4), BE(4)	
5A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AN(3), AX(3), BE(3)	
5A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10% 400VDCW; MIL type CV09A1KE105KM.	
5A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 07115, part no. CY20C512K, 90536, dwg 4912284-16.	
5A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ±1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), T(2), AU(2), BB(2)	
5A4R2		RESISTOR, FIXED, FILM: 20000 ohm. ±2%, 2W; MIL type M22684-04-0159.	
5A4R3		RESISTOR, FIXED WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
5A4T1		TRANSFORMER, POWER, STEPDOWN: Control, single phase, 50-400HZ; mfr 16153, part no. MC4518, 90536, dwg 7904726-00. (Attaching Parts) I(2), Y(2), AV(2), BC(2)	
5A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
5A6		CIRCUIT CARD ASSEMBLY, CONTROL: Plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
5A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 16 diodes, 6 transistors, 4 resistors, and 1 integrated circuit; mfr 90536, part no. 7101877-00. (Attaching Parts) W(2), AN(5), AX(5), BE(5)	
5A7C1		CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500VDCW; MIL type CM06FD751G03.	
5A7C2 5A7C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
5A7CR1 thru 5A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 Amp, 50VDC, mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Parts) D(8)	
5A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400VAC; MIL type 1N3893. (Attaching Parts) B(1), J(1), AX(1), BM(1)	
5A7CR6 thru 5A7CR9		Same as 5A7CR1 (item no. 20)	
5A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts) I(1), AI(1), AV(1), BC(1)	
5A7CR11 5A7CR12 5A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	
5A7CR14 5A7CR15 5A7CR16		RECTIFIER, SEMICONDUCTOR DEVICE: Unitized, 3-phase, full wave, 3 AMP, 400V piv per leg; mfr 12929, part no. 691-4, 90536, dwg 7904496-03. (Attaching Parts) Z(6), BI(6)	
5A7Q1		TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3), BN(3)	
5A7Q2		TRANSISTOR: NPN, silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
5A7Q3 5A7Q4		TRANSISTOR: NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts) A(2) I(4),AI(4), AV(4), BC(4), BL(4)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
5A7Q5 5A7Q6		Same as 5A7Q1 (item no. 31)	
5A7R1 thru 5A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm ±10%, 3W; MIL type RW69VR10.	
5A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2) CONTACT, ELECTRICAL: Male, crimp type, 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	
Power Supply PP-		/UYK-20(V) (Unit 6)	
6		POWER SUPPLY PP- /UYK-20(V): Provides power to each of the units within the data processor cabinet, operating power 208V, 400HZ, 3-phase wye; mfr 90536, part no. 7101995-00.	
6L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
6P1 6P2		CONNECTOR, PLUG, ELECTRICAL: Male; mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	
6T1		TRANSFORMER ASSEMBLY: Mfr 90536, part no. 7126376-00. (Attaching Parts) AN(6), AX(6), BE(6)	
6TB1		not used	
6TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) I(2), AI(2), AV(2), BC(2), BI(2)	
6A1		ELECTRONIC COMPONENTS ASSEMBLY: 3-phase, 400HZ, contains 3 capacitors and 1 choke; mfr 90536, part no. 7101982-00. (Attaching Parts) AN(4), AX(4), BE(4)	
6A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 680UF, ±15%, 250V; MIL type CE71C681M. (Attaching Parts) AN(2), BE(2)	
6A1C2 6A1C3		CAPACITOR, FIXED, ELECTROLYTIC: 120UF, -15%, ±30%, 150V; mfr 56289, part no. 112D127C3150M1, 90536, dwg 7901635-13.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
6A1L1		PLATE ASSEMBLY, CHOKE: Mfr 90536, part no. 7101987-00. (Attaching Parts) AJ(4), AV(4)	
6A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
6A2TB1 6A2TB2		not used	
6A2TB3 6A2TB4		TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11. (Attaching Parts) AE(8), BC(8), BH(8)	
6A2TB5		TERMINAL BOARD: Barrier type, 4 terminals; mfr 75382, part no. 600AY4, 90536, dwg 904862-05. (Attaching Parts) AE(4), BC(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 19 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no. 7101932-00. (Attaching Parts) I(4), BI(4)	
6A3		FILTER ASSEMBLY, INPUT: 6 capacitors and 9 chokes mtd in chassis, epoxyed; mfr 90536, part no. 7101979-01. (Attaching Parts) AN(4), AX(4), BE(4)	
6A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AN(3), AX(3), BE(3)	
6A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10%, 400VDCW; MIL type CWC94A1KE105KM.	
6A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K, 90536, dwg 4912284-16.	
6A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ±1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), T(2), AU(2), BB(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
6A4R2		RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.	
6A4R3		RESISTOR, FIXED, WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
6A4T1		TRANSFORMER, POWER, STEPDOWN: Control, single phase, 50-400HZ; mfr 16513, part no. MC4518, 90536, dwg 7904726-00. (Attaching Parts) I(2), W(2), AV(2), BC(2)	
6A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
6A6		CIRCUIT CARD ASSEMBLY, CONTROL: Plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	
6A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 16 diodes, 6 transistors, 4 resistors, and 1 integrated circuit; mfr 90536, part no. 7101877-00. (Attaching Parts) W(2), AN(5), AX(5), BE(5)	
6A7C1		CAPACITOR, MICA DIELECTRIC: 75 PF, ±2%, 500VDCW; MIL type CM06FD751G03.	
6A7C2 6A7C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
6A7CR1 thru 6A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 amp, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Parts) D(8)	
6A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400 VAC; MIL type 1N3893. (Attaching Parts) B(1),J(1), AX(1), BM(1)	
6A7CR6 thru 6A7CR9		Same as 6A7CR1 (item no. 20)	
6A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts) I(1), AI(1), AV(1), BC(1)	
6A7CR11 6A7CR12 6A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
6A7CR14 6A7CR15 6A7CR16		RECTIFIER, SEMICONDUCTOR DEVICE: Unitized, 3-phase, full wave, 3 AMP, 400V piv per leg; mfr 12929, part no. 691-4, 90536, dwg 7904496-03. (Attaching Parts) Z(6), BI(6)	
6A7Q1		TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3), BN(3)	
6A7Q2		TRANSISTOR: NPN, silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
6A7Q3 6A7Q4		TRANSISTOR: NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts) A(2), I(4), AI(4), AV(4) BC(4), BL(4)	
6A7Q5 6A7Q6		Same as 6A7Q1 (item no. 31)	
6A7R1 thru 6A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm, ±10%, 3W; MIL type RW69VR10.	
6A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01. (Attaching Parts) A(1), I(2), AI(2), AV(2) BC(2), BL(2)	
		CONTACT, ELECTRICAL: Male, crimp type 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	
Power Supply PP-		/UYK-20(V) (Unit 7)	
7		POWER SUPPLY PP- /UYK-20(V): Provides power to each of the units within the data processor cabinet, operating power 115V, 400HZ, single phase; mfr 90536, part no. 7101875-00.	
7L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
7P1 7P2		CONNECTOR, PLUG, ELECTRICAL: Male; mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
7TB1		not used	
7TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) G(2), AF(2), AU(2), BB(2)	
7A1		CAPACITOR ASSEMBLY: Single phase, 400HZ, contains 3 capacitors; mfr 90536, part no. 7128002-00. (Attaching Parts) AN(4), AX(4), BE(4)	
7A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 680UF, ±15%, 250V; MIL type CE71C681M. (Attaching Parts) AN(2), BE(2)	
7A1C2 7A1C3		CAPACITOR, FIXED ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.	
7A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
7A2TB1 7A2TB2		not used	
7A2TB3 7A2TB4		TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11. (Attaching Parts) BC(8), AE(8), BH(8)	
7A2TB5		TERMINAL BOARD: Barrier type, 4 terminals; mfr 75382, part no. 600AY4, 90536, dwg 904862-05. (Attaching Parts) BC(4), AE(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 Capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 19 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no 7101932-00. (Attaching Parts) I(4), BI (4)	
7A3		FILTER ASSEMBLY, INPUT: 400HZ single phase, 1 capacitor, 1 terminal board, and 2 chokes mtd in chassis; mfr 90536, part no. 7128001-00. (Attaching Parts) AN(4), AX(4), BE(4)	
7A3C1		CAPACITOR FIXED, PLASTIC DIELECTRIC: 2.5UF, ±10%, 400VDCW; mfr 56289, part no. 260P25594S2, 90536, dwg 7903001-13.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
7A3L1 7A3L2		CHOKE: Mfr 90536, part no. 7101977-15.	
7A3TB1		Same as 7TB2 (item no. 26) (Attaching Parts) AD(2), AU(2), BB(2)	
7A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AM(3), AW(3), BD(3)	
7A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10%, 400VDCW; MIL type CV09A1KE105KM.	
7A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K, 90536, dwg 4912284-16.	
7A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ±1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), T(2), AU(2), BB(2)	
7A4R2		RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.	
7A4R3		RESISTOR, FIXED WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
7A4T1		TRANSFORMER, POWER STEPDOWN: Control single phase, 50-400HZ; mfr 16513, part no. MC4518, 90536, dwg 7904726-00. (Attaching Parts) I(2), Y(2), AV(2), BC(2)	
7A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
7A6		CIRCUIT CARD ASSEMBLY, CONTROL: Plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	
7A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 14 diodes, 6 transistors, 4 resisters, and 1 integrated circuit; mfr 90536, part no. 7101877-01. (Attaching Parts) W(2), AN(5), AX(5), BE(5)	
7A7C1		CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500VDCW; MIL type CM06FD751G03.	
7A7C2 7A7C3		CAPACITOR, FIXED, CERAMIC, DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
7A7CR1 thru 7A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 AMP, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Part) D(8)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
7A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400 VAC; MIL type 1N3893. (Attaching Parts) B(1), J(1), AX(1) BM(1)	
7A7CR6 thru 7A7CR9		Same as 7A7CR1 (item no. 20)	
7A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts I(1), AI(1) AV(1), BC(1)	
7A7CR11 7A7CR12 7A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies 100VDC, 10 AMP; mfr 12969, part no. 655-083-01, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	
7A7CR14		RECTIFIER, SEMICONDUCTOR DEVICE: Single phase, full wave bridge, 25 AMP, 400V; mfr 12929, part no. 655-081-4, 90536, dwg 7903529-03. (Attaching Parts) J(1), AP(1), AX(1), BE(1)	
7A7Q1		TRANSISTOR: NPN silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3) BN(3)	
7A7Q2		TRANSISTOR: NPN silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
7A7Q3 7A7Q4		Transistor; NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts)A(2), I(4),AI(4),AV(4), BC(4), BL(4)	
7A7Q5 7A7Q6		Same as 7A7Q1 (item no. 31)	
7A7R1 thru 7A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm, ±10%, 3W; MIL type RW69VR10.	
7A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
7A8		RELAY ASSEMBLY: Contains 1 relay and 1 resistor mtd on bracket; mfr 90536, part no. 7126391-00. (Attaching Parts) AM(4), AW(4), BD(4)	
7A8K1		RELAY ARMATURE: 3 spst contacts, 115VAC, 400HZ; MIL type MS27418-1A. (Attaching Parts) AV(4)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
7A8R1		RESISTOR, FIXED, WIREWOUND: Surge limiting, 3 ohm ±1%, 5W; mfr 11502, part no. PW5446, 90536, dwg 7904765-00. CONTACT, ELECTRICAL: Male, crimp type, 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	
Power Supply PP- /UYK-20X(V) (Unit 8)			
8		POWER SUPPLY PP- /UYK-20X(V): Provides power to each of the units within the data processor cabinet, operating power 115V, 60HZ, 3-phase delta; mfr 90536, part no. 7101880-00.	
8L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
8P1 8P2		CONNECTOR, PLUG ELECTRICAL: Male, mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	
8T1		TRANSFORMER ASSEMBLY: Mfr 90536, part no. 7128010-00. (Attaching Parts) AN(6), AX(6), BE(6)	
8TB1 8TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) H(2), AF(4), AU(6), BB(2)	
8A1		ELECTRONIC COMPONENTS ASSEMBLY: 3-phase, 400HZ, contains 3 capacitors and 1 choke; mfr 90536, part no. 7101982-00. (Attaching Parts) AN(4), AX(4), BE(4)	
8A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 680UF, ±15%, 250V; MIL type CE71C681M. (Attaching Parts) AN(2), BE(2)	
8A1C2 8A1C3		CAPACITOR, FIXED, ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.	
8A1L1		PLATE ASSEMBLY, CHOKE: Mfr 90536, part no. 7101987-00. (Attaching Parts) AJ(4), AV(4)	
8A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
8A2TB1 8A2TB2		not used	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
8A2TB3 8A2TB4		TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11. (Attaching Parts) BC(8), AE(8), BH(8)	
8A2TB5		TERMINAL BOARD: Barrier type, 4 terminals; mfr 75382, part no. 600AY4, 90536, dwg 904862-05. (Attaching Parts) BC(4), AE(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 Capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 19 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no. 7101932-00. (Attaching Parts) I(4), BU(4)	
8A3		not used	
8A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AM(3), AW(3), BD(3)	
8A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF ± 10%, 400VDCW; MIL type CV09A1KE105KM.	
8A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 510PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K, 90536, dwg 4912284-16.	
8A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ± 1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), T(2), AU(2), BB(2)	
8A4R2		RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.	
8A4R3		RESISTOR, FIXED, WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
8A4T1		TRANSFORMER, POWER, STEPDOWN: Control single phase, 50-400HZ; mfr 16513, part no. MC4518, 90536, dwg 7904726-00. (Attaching Parts) I(2). Y(2), AV(2), BC(2)	
8A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
8A6		CIRCUIT CARD ASSEMBLY, CONTROL: plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	

TABLE 7-2. DATA PROCESSING SET AN/UYK -20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
8A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 16 diodes, 6 transistors, 4 resistors, and 1 integrated circuit; mfr 90536, part no. 7101877-00. (Attaching Parts) W(2), AN(5), AX(5), BE(5)	
8A7C1		CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500VDCW; MIL type CM06FD751G03.	
8A7C2 8A7C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
8A7CR1 thru 8A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 AMP, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Parts) D(8)	
8A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400VAC; MIL type 1N3893. (Attaching Parts) B(1), J(1), AX(1), BM(1)	
8A7CR6 thru 8A7CR9		Same as 8A7CR1 (item no. 20)	
8A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts) I(1), AI(1), AV(1), BC(1)	
8A7CR11 8A7CR12 8A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	
8A7CR14 8A7CR15 8A7CR16		RECTIFIER, SEMICONDUCTOR DEVICE: Unitized 3-phase, full wave, 3 AMP, 400V piv per leg; mfr 12929, part no. 691-4, 90536, dwg 7904496-03. (Attaching Parts) Z(6), BI(6)	
8A7Q1		TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3), BN(3)	
8A7Q2		TRANSISTOR: NPN, silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7004415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
8A7Q3 8A7Q4		TRANSISTOR: NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts) A(2), I(4), AI(4), AV(4), BC(4), BL(4)	
8A7Q5 8A7Q6		Same as 8A7Q1 (item no. 31)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
8A7R1 thru 8A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm, ±10%, 3W; MIL type RW69VR10.	
8A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01 (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2) CONTACT ELECTRICAL: Male, crimp type, 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	
Power Supply PP- /UYK-20X(V) (Unit 9)			
9		POWER SUPPLY PP- /UYK-20X(V): Provides power to each of the units within the data processor cabinet, operating power 208V, 60HZ, 3-phase wye; mfr 90536, part no. 7101990-00.	
9L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
9P1 9P2		CONNECTOR, PLUG ELECTRICAL: Male, mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	
9T1		TRANSFORMER ASSEMBLY: Mfr 90536, part no. 7128010-00. (Attaching Parts) AN(6), AX(6), BE(6)	
9TB1 9TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) H(2), AF(4), AU(6), BB(2)	
9A1		ELECTRONIC COMPONENTS ASSEMBLY: 3-phase, 400HZ, contains 3 capacitors and 1 choke; mfr 90536 part no. 7101982-00. (Attaching Parts) AN(4), AX(4), BE(4)	
9A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 68 UF, ±15%, 250V; MIL type CE[illegible]1C681M. (Attaching Parts) AN(2), BE(2)	
9A1C2 9A1C3		CAPACITOR, FIXED, ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.	
9A1L1		PLATE ASSEMBLY, CHOKE: Mfr 90536, part no. 7101987-00. (Attaching Parts) AJ(4), AV(4)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
9A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
9A2TB1		not used	
9A2TB2			
9A2TB3		TERMINAL BOARD: Barrier type, 7 terminals; mfr	
9A2TB4		75382, part no. 600AX7, 90536, dwg 904862-11. (Attaching Parts) AE(8), BC(8), BH(8)	
9A2TB5		TERMINAL BOARD: Barrier type, 4 terminals, mfr 75382, part no. 600AX4, 90536, dwg 904862-05. (Attaching Parts) AE(4), BC(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 13 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no. 7101932-00. (Attaching Parts) I(4), BI(4)	
9A3		not used	
9A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AM(3), AX(3), BD(3)	
9A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10%, 400VDCW; MIL type C[illegible].	
9A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K 90536, dwg 4912284-16.	
9A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ±1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), U(2), AU(2), BB(2)	
9A4R2		RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.	
9A4R3		RESISTOR, FIXED, WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
9A4T1		TRANSFORMER, POWER, STEPDOWN: Control, single phase, 50-400HZ; mfr 16153, part no. MC4515, 90536, dwg 7904726-00. (Attaching Parts) I(2), K(2), AV(2), BC(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
9A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
9A6		CIRCUIT CARD ASSEMBLY, CONTROL: Plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	
9A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 16 diodes, 6 transistors, 4 resistors, and 1 integrated circuit; mfr 90536, part no. 7101877-00. (Attaching Parts) W(2), AN(5), AX(5), BE(5)	
9A7C1		CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500 VDCW; MIL type CM06FD751G03.	
9A7C2 9A7C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
9A7CR1 thru 9A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 AMP, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Parts) D(8)	
9A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400VAC; MIL type 1N3893. (Attaching Parts) B(1), J(1), AX(1), BM(1)	
9A7CR6 thru 9A7CR9		Same as 9A7CR1 (item no. 20)	
9A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts) I(1), AI(1), AV(1), BC(1)	
9A7CR11 9A7CR12 9A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	
9A7CR14 9A7CR15 9A7CR16		RECTIFIER, SEMICONDUCTOR DEVICE: Unitized, 3-phase, full wave, 3 AMP, 400V piv per leg; mfr 12929, part no. 691-4, 90536, dwg 7904496-03. (Attaching Parts) Z(6), BI(6)	
9A7Q1		TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3), BN(3)	
9A7Q2		TRANSISTOR: NPN, silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
9A7Q3 9A7Q4		TRANSISTOR: NPN, silicon, power Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts) A(2), I(4), AI(4), AV(4), BC(4), BL(4)	
9A7Q5 9A7Q6		Same as 9A7Q1 (item no. 31)	
9A7R1 thru 9A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm, ±10%, 3W; MIL type RW69VR10.	
9A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
		CONTACT, ELECTRICAL: Male, crimp type, 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	
Power Supply PP- /UYK-20X(V) (Unit 10)			
10		POWER SUPPLY PP- /UYK-20X(V): Provides power to each of the units within the data processor cabinet, operating power 115V, 60HZ, single phase; mfr 90536, part no. 7101885-00.	
10C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 15UF, ±10%, 370VACW; mfr 56289, part no. 200P2176, 90536, dwg 7901282-08. (Attaching Parts) AN(4), AX(4), BE(4)	
10L1		CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00. (Attaching Parts) AN(2), AX(2), BE(2)	
10P1 10P2		CONNECTOR, PLUG, ELECTRICAL: Male; mfr 90536, part no. 7101883-00. (Attaching Parts) AC(4), AU(4)	
10TB1		not used	
10TB2		TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09. (Attaching Parts) G(2), AF(2), AU(2), BB(2)	
10A1		CAPACITOR ASSEMBLY: Single phase, 60HZ, contains 3 capacitors; mfr 90536, part no. 7126398-00. (Attaching Parts) AN(4), AX(4), BE(4)	

TABLE 7-2. [illegible]

Reference Designation	Notes	Name and Description	Figure Number (Item)
10A1C1		CAPACITOR, FIXED, ELECTROLYTIC: Al can, 2200UF, ±18%, 250V; MIL type CE71C222M. (Attaching Parts) AQ(2), AZ(2)	
10A1C2 10A1C3		CAPACITOR, FIXED ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.	
10A2		OUTPUT FILTER ASSEMBLY: Contains 2 capacitor boards, 1 inductor choke assy, and 3 terminal boards; mfr 90536, part no. 7101978-00. (Attaching Parts) AN(6), AX(6), BE(6)	
10A2TB1 10A2TB2		not used	
10A2TB3 10A2TB4		TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11. (Attaching Parts) AE(8), BC(8), BH(8)	
10A2TB5		TERMINAL BOARD: Barrier type, 4 terminals; mfr 75382, part no. 600AY4, 90536, dwg 904862-05. (Attaching Parts) AE(4), BC(4), BH(4)	
		CAPACITOR BOARD ASSEMBLY: 13 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101951-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		CAPACITOR BOARD ASSEMBLY: 19 capacitors and 2 resistors mtd on board, epoxyed; mfr 90536, part no. 7101952-00. (Attaching Parts) G(4), U(4), AU(4), BB(4)	
		INDUCTOR CHOKE ASSEMBLY: 8 chokes mtd on plate, epoxyed; mfr 90536, part no. 7101932-00. (Attaching Parts) I(4), BI(4)	
10A3		FILTER ASSEMBLY, INPUT: 60HZ single phase, 1 terminal board, and 3 chokes mtd in chassis, epoxyed; mfr 90536, part no. 7126397-00. (Attaching Parts) AN(4), AX(4), BE(4)	
10A3TB1		Same as 10TB2 (item no. 26) (Attaching Parts) AD(2), AU(2), BB(2)	
10A4		ELECTRONIC COMPONENTS ASSEMBLY: Contains 2 capacitors, 3 resistors, and 1 transformer mtd on bracket; mfr 90536, part no. 7101980-00. (Attaching Parts) AM(3), AW(3), BD(3)	
10A4C1		CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10%, 400VDCW; MIL type CV09A1KE105KM.	
10A4C2		CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K, 90536, dwg 4912284-16.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
10A4R1		RESISTOR, FIXED, WIREWOUND: 0.1 ohm ±1%, 20W; MIL type RE70GR100. (Attaching Parts) G(2), T(2), AU(2), BB(2)	
10A4R2		RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.	
10A4R3		RESISTOR, FIXED WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00. (Attaching Parts) P(2), S(2), BG(2)	
10A4T1		TRANSFORMER, POWER, STEPDOWN: Control, single phase, 50-400HZ; mfr 16513, part no. MC4518, 90536, dwg 7904726-00. (Attaching Parts) I(2), Y(2), AV(2), BC(2)	
10A5		TRANSFORMER COIL ASSEMBLY: 2 transformers mtd in bracket, epoxyed; mfr 90536, part no. 7101981-00. (Attaching Parts) AN(4), AX(4), BE(4)	
10A6		CIRCUIT CARD ASSEMBLY, CONTROL: Plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.	
10A7		HEAT EXCHANGER ASSEMBLY: Contains 3 capacitors, 14 diodes, 6 transistors, 4 resistors, and 1 integrated circuit; mfr 90536, part no. 7101877-01. (Attaching Parts) W(5), AN(5), AX(5), BE(5)	
10A7C1		CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500VDCW; MIL type CM06FD751G03.	
10A7C2 10A7C3		CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000PF, ±10%, 50VDCW; MIL type CK05BX473K.	
10A7CR1 thru 10A7CR4		SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30 AMP, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05. (Attaching Parts) D(8)	
10A7CR5		SEMICONDUCTOR DEVICE, DIODE: Power 12 AMP, 400VAC; MIL type 1N3893. (Attaching Parts) B(1), J(1), AX(1), BM(1)	
10A7CR6 thru 10A7CR9		Same as 10A7CR1 (item no. 20)	
10A7CR10		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00. (Attaching Parts) I(1), AI(1), AV(1), BC(1)	
10A7CR11 10A7CR12 10A7CR13		RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10 AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06. (Attaching Parts) I(3), AI(3), AV(3), BC(3)	

TABLE7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
10A7CR14		RECTIFIER, SEMICONDUCTOR DEVICE: Single phase, full wave bridge, 25AMP, 400V; mfr 12929, part no. 655-081-4, 90536, dwg 7903529-03. (Attaching Parts) J(1), AP(1), AX(1), BE(1)	
10A7Q1		TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00. (Attaching Parts) C(3), E(3), AY(3), BN(3)	
10A7Q2		TRANSISTOR: NPN, silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
10A7Q3 10A7Q4		TRANSISTOR: NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01. (Attaching Parts) A(2), I(4), AI(4), AV(4), BC(4), BL(4)	
10A7Q5 10A7Q6		Same as 10A7Q1 (item no. 31)	
10A7R1 thru 10A7R4		RESISTOR, FIXED, WIREWOUND: 0.10 ohm ±10%, 3W; MIL type RW69VR10.	
10A7U1		INTEGRATED CIRCUIT, VOLTAGE REGULATOR: Mfr 18234, part no. RC5109K, 90536, dwg 7904270-01. (Attaching Parts) A(1), I(2), AI(2), AV(2), BC(2), BL(2)	
10A8		RELAY ASSEMBLY: Contains 1 relay and 1 resistor mtd on bracket; mfr 90536, part no. 7126391-00. (Attaching Parts) AH(4), AV(4), BD(4)	
10A8K1		RELAY, ARMATURE: 3 spst contacts, 115VAC, 400HZ; MIL type MS27416-1. (Attaching Part) AV(4)	
10A8R1		RESISTOR, FIXED, WIREWOUND: Surge limiting, 3 ohm, ±1%, 5W; mfr 11502, part no. PW5446, 90536, dwg 7904765-00. CONTACT, ELECTRICAL: Male, crimp type 22AWG, blue color code, 0.56 in. long; mfr 16512, part no. 540176, 90536, dwg 7903660-01 (42).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
Processor-Verifier Unit CP- (P)/UYK-20(V) (Unit 11)			
11		PROCESSOR-VERIFIER UNIT CP- (P)/UYK-20(V): Performs the arithmetic and data processing operation as directed, operating power 115VAC, 400HZ, 3-phase delta or 208VAC, 400HZ, 3-phase wye or 115VAC, 400HZ, single phase; mfr 90536, part no. 7128031-00.	
11B1		FAN AXIAL: CW rotation, aluminum case, 4.688 in. sq, 1.5 in. thick; mfr 82877, part no. 810DS TYPE ST, 90536, dwg 7901420-01. (Attaching Parts) R(4), Y(4), BI(4)	
11C1		CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.39 UF, ±10%, 400VDCW; mfr 56289, part no. 260P394948S2, 90536, dwg 7903001-33.	
11J1 thru 11J33		not used	
11J34		CONNECTOR RECEPTACLE, ELECTRICAL: Male 5-contact; MIL type MS120E14-5P. (Attaching Parts) AC(4), BB(4), BH(4)	
11TB1		TERMINAL BOARD: Barrier type, 8 terminals; mfr 75382, part no. 410-8, 90536, dwg 4912642-07. (Attaching Parts) G(4), Q(4), AB(4), BB(4), BH(12)	
		CIRCUIT CARD ASSEMBLY: ARITHMETIC LOGIC UNIT; mfr 90536, part no. 7092175-01 (4).	
		CIRCUIT CARD ASSEMBLY: ARITHMETIC LOGIC CONTROL UNIT; mfr 90536, part no. 70902181-01 (1).	
		CIRCUIT CARD ASSEMBLY: ALU CONTROL II; mfr 90536, part no. 7125415-01 (1).	
		CIRCUIT CARD ASSEMBLY: MICRO REGISTER; mfr 90536, part no. 7092185-01 (3).	
		CIRCUIT CARD ASSEMBLY: MICRO CONTROL; mfr 90536, part no. 7092192-01 (1).	
		CIRCUIT CARD ASSEMBLY: BRANCH CONTROL; mfr 90536, part no. 7092195-01 (1).	
		CIRCUIT CARD ASSEMBLY: REPEAT CONTROL; mfr 90536, part no. 7092200-01 (1).	
		CIRCUIT CARD ASSEMBLY: SOURCE AND DESTINATION TRANS; mfr 90536, part no. 7092206-01 (1).	
		CIRCUIT CARD ASSEMBLY: MEMORY CONTROL; mfr 90536, part no. 7125665-01 (1).	
		CIRCUIT CARD ASSEMBLY: SPECIAL MEMORY INTERFACE; mfr 90536, part no. 7126155-01 (2).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20K(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
11 (Cont.)		CIRCUIT CARD ASSEMBLY: [illegible]-INPUT-[illegible] ADDRESS REGISTERS; mfr 90536, part no. 7125310-01 (2). CIRCUIT CARD ASSEMBLY: SHIFT MATRIX INPUT REGISTERS; mfr 90536, part no. 7126130-01 (1). CIRCUIT CARD ASSEMBLY: SHIFT MATRIX CONTROL; mfr 90536, part no. 7126135-01 (1). CIRCUIT CARD ASSEMBLY: [illegible] CLK; mfr 90536, part no. 7092031-01 (1). CIRCUIT CARD ASSEMBLY: MDR, PANEL INTERFACE; mfr 90536, part no. 7126145-01 (1). CIRCUIT CARD ASSEMBLY: MON CLK CONT, RESUME DUAL CHAN; mfr 90536, part no. 7126160-01 (1). CIRCUIT CARD ASSEMBLY: I/O CONT MEM & INDEXING LOGIC; mfr 90536, part no. 7125386-01 (4). CIRCUIT CARD ASSEMBLY: [illegible]; mfr 90536, part no. 7126170-01 (1). CIRCUIT CARD ASSEMBLY: I/O CNTRL 15; mfr 90536, part no. 7126190-01 (1). CIRCUIT CARD ASSEMBLY: [illegible], 20 MHz; mfr 90536, part no. 7126200-01 (1). CIRCUIT CARD ASSEMBLY: [illegible] STATUS REGR RTC + MEM SEL; mfr 90536, part no. 7125380-01 (2). CIRCUIT CARD ASSEMBLY: INSTRUCTION REGISTER 0-7; mfr 90536, part no. 7125240-01 (1). CIRCUIT CARD ASSEMBLY: EMULATE CONTROL I; mfr 90536, part no. 7125236-01 (1). CIRCUIT CARD ASSEMBLY: EMULATE CONTROL II; mfr 90536, part no. 7125385-01 (1). CIRCUIT CARD ASSEMBLY: PAGE REGISTERS; mfr 90536, part no. 7125405-01 (1). CIRCUIT CARD ASSEMBLY: I/O PRIORITY; mfr 90536, part no. 7126175-01 (1). CIRCUIT CARD ASSEMBLY: I/O PRIORITY CONTROL AND TIMING; mfr 90536, part no. 7126180-01 (1). CIRCUIT CARD ASSEMBLY: JUMP AND IA; mfr 90536, part no. 7126165-01 (1). CIRCUIT CARD ASSEMBLY: MULTIPLY CONTROL; mfr 90536, part no. 7126140-01 (1). CIRCUIT CARD ASSEMBLY: SHIFT MATRIX; mfr 90536, part no. 7125500-01 (2). CIRCUIT CARD ASSEMBLY: TWO BIT MULTIPLY; mfr 90536, part no. 7126125-01 (2). CIRCUIT CARD ASSEMBLY: U MEM BANK SELECT AND MISC; mfr 90536, part no. 7126205-01 (1). CIRCUIT CARD ASSEMBLY: I/O DATA DRIVE & MONITOR CLOCK; mfr 90536, part no. 7126150-01 (1).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
11 (Cont.)		CIRCUIT CARD ASSEMBLY: INTERRUPT STORAGE; mfr 90536, part no. 7126185-01 (1). CIRCUIT CARD ASSEMBLY: TRANSLATOR CONTROL AND TIMING; mfr 90536, part no. 7126195-01 (1).	
Processor-Verifier Unit CP- (P)/UYK-20X(V) (Unit 12)			
12		PROCESSOR-VERIFIER UNIT: CP- (P)/UYK-20X(V): Performs the arithmetic and data processing operations as directed, operating power 115 VAC, 60HZ, 3-phase delta or 208VAC, 60HZ, 3-phase wye or 115VAC, 60HZ, single phase; mfr 90536, part no. 7128031-01.	
12B1		FAN, AXIAL: Cw rotation, aluminum case, 4.688 in. sq, 1.5 in. thick; mfr 82877, part no. 682YS TYPE ST, 90536, dwg 7901420-03. (Attaching Parts) R(4), Y(4), BI(4)	
12C1		CAPACITOR FIXED, PLASTIC DIELECTRIC: 1.0UF, ±10%, 400VDCW; mfr 56289, part no. 260P10594S2, 90536, dwg 7903001-11.	
12J1 thru 12J33		not used	
12J34		CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 5-contact; MIL type MS120E14-5P. (Attaching Parts) AC(4), BB(4), BH(4)	
12TB1		TERMINAL BOARD: Barrier type, 8 terminals; mfr 75382, part no. 410-8, 90536, dwg 4912642-07. (Attaching Parts) G(4), Q(4), AB(4), BB(4), BH(12) CIRCUIT CARD ASSEMBLY: ARITHMETIC LOGIC UNIT; mfr 90536, part no. 7092175-01 (4). CIRCUIT CARD ASSEMBLY: ARITHMETIC LOGIC CONTROL UNIT; mfr 90536, part no. 7090218l-01 (1). CIRCUIT CARD ASSEMBLY: ALU CONTROL II; mfr 90536, part no. 7125415-01 (1). CIRCUIT CARD ASSEMBLY: MICRO REGISTER; mfr 90536, part no. 7092185-01 (3). CIRCUIT CARD ASSEMBLY: MICRO CONTROL; mfr 90536, part no. 7092192-01 (1). CIRCUIT CARD ASSEMBLY: BRANCH CONTROL; mfr 90536, part no. 7092195-01 (1). CIRCUIT CARD ASSEMBLY: REPEAT CONTROL; mfr 90536, part no. 7092200-01 (1).	

Reference Designation	Notes	Name and Description	Figure Number (Item)
12 (Cont.)		CIRCUIT CARD ASSEMBLY: [illegible] TR NS; mfr 90536, part no. 7092206-01 (1). CIRCUIT CARD ASSEMBLY: MEM RY C NTR L; mfr 90536, part no. 7125665-01 (1). CIRCUIT CARD ASSEMBLY: SPECIAL MEM RY INTERFACE; mfr 90536, part no. 7126155-01 (2). CIRCUIT CARD ASSEMBLY: P-BKPT-MEM ADDRESS REGISTERS; mfr 90536, part no. 7125310-01 (2). CIRCUIT CARD ASSEMBLY: SHIFT MATRIX INPUT REGISTERS; mfr 90536, part no. 7126130-01 (1). CIRCUIT CARD ASSEMBLY: SHIFT MATRIX C NTR L; mfr 90536, part no. 7126135-01 (1). CIRCUIT CARD ASSEMBLY: CL CK; mfr 90536, part no. 7092031-01 (1). CIRCUIT CARD ASSEMBLY: NDR , PANEL INTERFACE; mfr 90536, part no. 7126145-01 (1). CIRCUIT CARD ASSEMBLY: M N CLK C NT, RESUME, DUAL CHAN; mfr 90536, part no. 7126160-01 (1). CIRCUIT CARD ASSEMBLY: I/ C NT MEM & INDEXING L GIC; mfr 90536, part no. 7125306-01 (4). CIRCUIT CARD ASSEMBLY: TRANSLAT R; mfr 90536, part no. 7126170-01 (1). CIRCUIT CARD ASSEMBLY: U C NTR L 15; mfr 90536, part no. 7126190-01 (1). CIRCUIT CARD ASSEMBLY: SCILLAT R, 20 MHZ; mfr 90536, part no. 7126200-01 (1). CIRCUIT CARD ASSEMBLY: P + STATUS RGTR RTC + PSW SEL; mfr 90536, part no. 7125380-01 (2). CIRCUIT CARD ASSEMBLY: INSTRUCTI N REGISTER 0-7; mfr 90536, part no. 7125240-01 (1). CIRCUIT CARD ASSEMBLY: EMULATE C NTR L I; mfr 90536, part no. 7125236-01 (1). CIRCUIT CARD ASSEMBLY: EMULATE C NTR L II; mfr 90536, part no. 7125385-01 (1). CIRCUIT CARD ASSEMBLY: PAGE REGISTERS; mfr 90536, part no. 7125405-01 (1). CIRCUIT CARD ASSEMBLY: I/O PRI RITY; mfr 90536, part no. 7126175-01 (1). CIRCUIT CARD ASSEMBLY: I/ PRI RITY C NTR L AND TIMING; mfr 90536, part no. 7126180-01 (1). CIRCUIT CARD ASSEMBLY: JUMP AND IA; mfr 90536, part no. 7126165-01 (1). CIRCUIT CARD ASSEMBLY: MULTIPLY C NTR L; mfr 90536, part no. 7126140-01 (1).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
12 (Cont.)		CIRCUIT CARD ASSEMBLY: SHIFT MATRIX; mfr 90536, part no. 7125500-01 (2). CIRCUIT CARD ASSEMBLY: TWO BIT MULTIPLY; mfr 90536, part no. 7126125-01 (2). CIRCUIT CARD ASSEMBLY: U MEM BANK SELECT AND MISC; mfr 90536, part no. 7126205-01 (1). CIRCUIT CARD ASSEMBLY: I/O DATA DRIVE & MONITOR CLOCK; mfr 90536, part no. 7126150-01 (1). CIRCUIT CARD ASSEMBLY: INTERRUPT STORAGE; mfr 90536, part no. 7126185-01 (1). CIRCUIT CARD ASSEMBLY: TRANSLATOR CONTROL AND TIMING; mfr 90536, part no. 7126195-01 (1).	
Core Memory Unit MU-604/UYK-20(V) (Unit 13)			
13		CORE MEMORY UNIT MU-604/UYK-20(V): Electronic circuit plug-in module containing 8K magnetic core memory, used in core memory control C- (P)/UYK-20(V) and C- (P)/UYK-20X(V), connector mtd; mfr 90536, part no. 7126382-00.	
Control, Core Memory C- (P)/UYK-20(V) (Unit 14)			
14		CONTROL, CORE MEMORY C- (P)/UYK-20(V): Provides control for core memory unit MU-604/UYK-20(V), operating power 115VAC, 400HZ, 3-phase delta or 208VAC, 400HZ, 3-phase wye or 115VAC, 400HZ, single phase; mfr 90536, part no. 7128029-00.	
14B1		FAN AXIAL: CW rotation, aluminum case, 4.688 in. sq, 1.5 in. thick; mfr 82877, part no. 810DS TYPE ST, 90536, dwg 7901420-01. (Attaching Parts) AI(4), BI(4)	
14C1		CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.39UF, ±10%, 400VDCW; mfr 56289, part no. 260P3949452, 90536, dwg 7903001-33.	
14TB1		TERMINAL BOARD: Barrier type, 12 terminals; mfr 75382, part no. 600AY12, 90536, dwg 904862-15. (Attaching Parts) AI(4), BI(4)	
14TB2		TERMINAL BOARD: Barrier type, 3 terminals; MIL type 37TB-3. (Attaching Parts) AK(4), BI(4)	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
14 (Cont.)		CIRCUIT CARD ASSEMBLY: MEMORY DATA BOARD, plug-in type; mfr 90536, part no. 7101824-00 (2). CIRCUIT CARD ASSEMBLY, CONTROL DATA BOARD, plug-in type; mfr 90536, part no. 7101826-00 (2).	
Control, Core Memory C- (P)/UYK-20X(V) (Unit 15)			
15		CONTROL, CORE MEMORY C- (P)/UYK-20X(V): Provides control for core memory unit MU-604/UYK-20(V), operating power 115VAC, 60HZ, 3-phase delta or 208VAC,60HZ, 3-phase wye or 115VAC, 60HZ, single phase; mfr 90536, part no. 7128029-01.	
15B1		FAN AXIAL: CW rotation,aluminum case, 4.688 in. sq, 1.5 in. thick; mfr 82877, part no. 682YS TYPE ST, 90536, dwg 7901420-03. (Attaching Parts) AI(4), BI(4)	
15C1		CAPACITOR, FIXED, PLASTIC DIELECTRIC: 1.0UF, ±10%, 400VDCW; mfr 56289, part no. 260P10594S2, 90536, dwg 7903001-11.	
15TB1		TERMINAL BOARD: Barrier type, 12 terminals; mfr 75382, part no. 600AY12, 90536, dwg 904862-15. (Attaching Parts) AI(4), BI(4)	
15TB2		TERMINAL BOARD: Barrier type, 3 terminals; MIL type 37TB-3. (Attaching Parts) AI(4), BI(4)	
		CIRCUIT CARD ASSEMBLY: MEMORY DATA BOARD; plug-in type; mfr 90536, part no. 7101824-00 (2).	
		CIRCUIT CARD ASSEMBLY: CONTROL DATA BOARD, plug-in type; mfr 90536, part no. 7101826-00 (2).	
Interface Kit, Fast Serial MK- /UYK-20(V) (Unit 16)			
16		INTERFACE KIT, FAST SERIAL MK- /UYK-20(V): Contains 2 circuit plug-in cards required for 1 group of 2 input and 2 output channels, used in processor-verifier unit CP- (P)/UYK-20 (V) and CP- (P)/UYK-20X(V); mfr 90536, part no. 7101802-00.	
		CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7119425-01 (1).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
16 (Cont.)		CIRCUIT CARD ASSEMBLY: 2 CHANNEL RECEIVER; mfr 90536, part no. 7119430-01 (1)	
Interface Kit, Serial Sync MK- /UYK-20(V) (Unit 17)			
17		INTERFACE KIT, SERIAL SYNC MK- /UYK-20(V): Contains 2 circuit plug-in cards required for 1 group of 2 input and 2 output channels, used in processor-verifier unit CP- (P)/UYK-20 (V) and CP- (P)/UYK-20X(V); mfr 90536, part no. 7101803-00. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7119435-01 (1). CIRCUIT CARD ASSEMBLY: 2 CHANNEL RECEIVER; mfr 90536, part no. 7119440-01 (1).	
Interface Kit, Serial Async MK- (V)/UYK-20(V) (Unit 18)			
18		INTERFACE KIT, SERIAL ASYNC MK- (V)/UYK-20(V): Contains 1 receiver and 16 optional driver circuit plug-in cards required for 1 group of 2 input and 2 output channels, used in processor-verifier unit CP- (P)/UYK-20(V) and CP- (P)/UYK-20X(V); mfr 90536, part no. 7128069-00. CIRCUIT CARD ASSEMBLY: 2 CHANNEL RECEIVER; mfr 90536, part no. 7133225-01 (1). CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7123230-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133235-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133240-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133245-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133250-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133255-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133260-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133265-01.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
18 (Cont.)		CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133270-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133275-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133280-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133285-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133290-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133295-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133300-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133305-01.	
Interface Kit, Serial Communications, Sync MK- /UYK-20(V) (Unit 19)			
19		INTERFACE KIT, SERIAL COMMUNICATIONS, SYNC MK- /UYK-20(V): Contains 2 circuit plug-in cards required for 1 group of 2 input and 2 output channels, used in processor-verifier units CP- (P)/UYK-20(V) and CP- (P)/UYK-20X(V); mfr 90536, part no. 7128069-00. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7119450-01 (1). CIRCUIT CARD ASSEMBLY: 2 CHANNEL RECEIVER; mfr 90536, part no. 7119445-01 (1).	
Interface Kit, Serial Communications Async MK- (V)/UYK-20(V) (Unit 20)			
20		INTERFACE KIT, SERIAL COMMUNICATIONS, ASYNC MK- (V)/UYK-20(V): Contains 1 receiver and 12 optional driver circuit plug-in cards required for 1 group of 2 input and 2 output channels, used in processor-verifier unit CP- (P)/UYK-20(V) and CP- (P)/UYK-20X(V); mfr 90536, part no. 7118070-00. CIRCUIT CARD ASSEMBLY: 2 CHANNEL RECEIVER; mfr 90536, part no. 7133310-01 (1). CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133315-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER: mfr 90536, part no. 7133320-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133325-01.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
20 (Cont.)		CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133330-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133335-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133340-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133345-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133350-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133355-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133360-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133365-01. CIRCUIT CARD ASSEMBLY: 2 CHANNEL DRIVER; mfr 90536, part no. 7133370-01.	
Interface Kit, Slow MK-1693/UYK-20(V) (Unit 21)			
21		INTERFACE KIT, SLOW MK-1693/UYK-20(V): Contains circuit plug-in cards required for 1 group of 4 input-output channels, used in processor section of computer set; mfr 90536, part no. 7101805-00. CIRCUIT CARD ASSEMBLY: DATA LINE DRIVERS AND RECEIVERS; mfr 90536, part no. 7119395-01 (2). CIRCUIT CARD ASSEMBLY: -15V SLOW; mfr 90536, part no. 7119405-01 (1). CIRCUIT CARD ASSEMBLY: I/O ONE SHOT; mfr 90536, part no. 7125350-01 (2). CIRCUIT CARD ASSEMBLY: CONTROL LINE DRIVERS AND RECEIVERS; mfr 90536, part no. 7119400-01 (1).	
Interface Kit, Fast, Negative MK-1694/UYK-20(V) (Unit 22)			
22		INTERFACE KIT, FAST, NEGATIVE MK-1694/UYK-20(V): Contains circuit plug-in cards required for 1 group of 4 in-put-output channels, used in processor section of computer set; mfr 90536, part no. 7101806-00. CIRCUIT CARD ASSEMBLY: -3V FAST, TYPE I; mfr 90536, part no. 7119399-01 (2). CIRCUIT CARD ASSEMBLY: -3V FAST, TYPE IV; mfr 90536, part no. 7119385-01 (1).	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
22 (Cont.)		CIRCUIT CARD ASSEMBLY: LINE DRIVERS, ACK TIMING 1, 2, 3; mfr 90536, part no. 7119390-01 (1). CIRCUIT CARD ASSEMBLY: I/O ONE SHOT; mfr 90536, part no. 7125350-01 (2).	
Interface Kit, Fast, Positive MK-1695/UYK-20(V) (Unit 23)			
23		INTERFACE KIT, FAST, POSITIVE MK-1695/UYK-20(V): Contains circuit plug-in cards required for 1 group of 4 input-output channels, used in processor section of computer set; mfr 90536, part no. 7101807-00. CIRCUIT CARD ASSEMBLY: +3.5V ANEW, TYPE I AND III; mfr 90536, part no. 7119410-01 (2). CIRCUIT CARD ASSEMBLY: +3.5V ANEW TYPE IV; mfr 90536, part no. 7119415-01 (1). CIRCUIT CARD ASSEMBLY: I/O ONE SHOT; mfr 90536, part no. 7125350-01 (2). CIRCUIT CARD ASSEMBLY: +3.5V ANEW, TYPE II; mfr 90536, part no. 7119420-01 (1).	
Micro Memory Program Kit MK- (V)/UYK-20(V) (Unit 24)			
24		MICRO MEMORY PROGRAM KIT MK- (V)/UYK-20(V): Microprogramed read-only-memory control structure, 512 bit word growth capacity, used in processor-verifier unit; mfr 90536, part no. 7128071-XX (dash number determines PROGRAM). CIRCUIT CARD ASSEMBLY: PROGRAM; mfr 90536, part no. 7125130-00. CIRCUIT CARD ASSEMBLY: MEMORY GROWTH CARD; mfr 90536, part no. 7125130-01 AND UP. CIRCUIT CARD ASSEMBLY: EMULATION CONTROL WORD; mfr 90536, part no. 7125155-01. CIRCUIT CARD ASSEMBLY: EMULATION CONTROL CARD; mfr 90536, part no. 7125175-01. CIRCUIT CARD ASSEMBLY: MICRO PROGRAM CONTROL; mfr 90536, part no. 7125125-01. CIRCUIT CARD ASSEMBLY: DIAGNOSTIC CARD; mfr 90536, part no. 7125135-01. CIRCUIT CARD ASSEMBLY: MATH PACK; mfr 90536, part no. TO BE ASSIGNED.	

TABLE 7-2. DATA PROCESSING SET AN/UYK-20(V) AND AN/UYK-20X(V), PARTS LIST (CONT.)

Reference Designation	Notes	Name and Description	Figure Number (Item)
Maintenance Kit MK- /UYK-20(V) (Unit 25)			
25		MAINTENANCE KIT MK- /UYK-20(V): Supplies and provides for storing and transporting special tools and items for removing the circuit plug-in cards and for checking out the data processing set; mfr 90536, part no. 7128073-00. CARD EXTRACTOR: RIGHT, MEMORY; mfr 90536, part no. 7128052-00 (1). CARD EXTRACTOR: LEFT, MEMORY; mfr 90536, part no. 7128053-00 (1). CARD EXTRACTOR: LOGIC; mfr 90536, part no. 7100903-00 (1). CABLE, END AROUND: Mfr 90536, part no. 7126394-00 (2).	
Accessory Kit MK- /UYK-20(V) (Unit 26)			
26		ACCESSORY KIT MK- /UYK-20(V): Contains integration hardware, I/O connectors, I/O cables, and power cables; mfr 90536, part no. 7128073-00.	

TABLE 7-3. LIST OF COMMON ITEM DESCRIPTIONS

Item Number	Description
1	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 47000 PF, ± 10%, 50VDCW; MIL type CK05BX473K.
2	CAPACITOR, FIXED, ELECTROLYTIC: 120UF, -15%, +30%, 150V; mfr 56289, part no. 112D127C3150Y1, 90536, dwg 7901635-13.
3	CAPACITOR, FIXED, GLASS DIELECTRIC: 5100PF, ±10%, 300VDCW; mfr 14674, part no. CY20C512K, 90536, dwg 4912284-16.
4	CAPACITOR, FIXED, PAPER DIELECTRIC: 1.0UF, ±10%, 400VDCW; MIL type CV09A1KE105KM.
5	CAPACITOR, MICA DIELECTRIC: 750PF, ±2%, 500VDCW; MIL type CM06FD751G03.
6	CHOKE ASSEMBLY, ELECTRICAL: Mfr 90536, part no. 7101974-00.
7	CIRCUIT CARD ASSEMBLY, CONTROL: plug-in type, contains components epoxyed on printed wiring board; mfr 90536, part no. 7119455-00.
8	CONNECTOR, PLUG, ELECTRICAL: Male; mfr 90536, part no. 7101883-00.
9	FILTER, RADIO FREQUENCY INTERFERENCE: T circuit rfi filter, 125VAC, 12AMP; mfr 56289, part no. JN17-4564A, 90536, dwg 7904734-00.
10	INTEGRATED CIRCUIT, VOLTAGE REGULATOR: mfr 18234, part no. RC5109K, 90536, dwg 7904270-01.
11	RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10AMP; mfr 12969, part no. 655-082-1, 90536, dwg 7903528-00.
12	RECTIFIER, SEMICONDUCTOR DEVICE: Doubler and CT assemblies, 100VDC, 10AMP; mfr 12969, part no. 655-083-1, 90536, dwg 7903528-06.

TABLE 7-3. LIST OF COMMON ITEM DESCRIPTIONS (CONT.)

Item Number	Description
13	RECTIFIER, SEMICONDUCTOR DEVICE: Unitized, 3-phase, full wave, 3AMP, 400V piv per leg; mfr 12969, part no. 691-4, 90536, dwg 7904496-03.
14	RESISTOR, FIXED, COMPOSITION: 100K ohm, ±5%, 1/2W; MIL type RCR20G104JM.
15	RESISTOR, FIXED, FILM: 20000 ohm, ±2%, 2W; MIL type M22684-04-0159.
16	RESISTOR, FIXED, WIREWOUND: 0.1 ohm, ±1%, 20W; MIL type RE70GR100.
17	RESISTOR, FIXED WIREWOUND: 1 ohm, ±1%, 5W; MIL type RE60G1R00.
18	RESISTOR, FIXED, WIREWOUND: 0.10 ohm, ±10%, 3W; MIL type RW69VR10.
19	SEMICONDUCTOR DEVICE, DIODE: Power, 12 AMP, 400VAC; MIL type 1N3893.
20	SEMICONDUCTOR DEVICE, DIODE: Silicon, medium power, 30AMP, 50VDC; mfr 03877, part no. SR1595, 90536, dwg 7901637-05.
21	SWITCH, PUSH: SPST normally open double break, 0.1 AMP, white button; mfr 07137, part no. SBS8732B26, 90536, dwg 7904277-00.
22	SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 AMP, clear lens; mfr 07137, part no. SSBL8721C22, 90536, dwg 7904278-00.
23	SWITCH, PUSH: SPST normally open double break, light emitting diode indicator, w/resistor, 0.1 AMP, clear lens; mfr 07137, part no. SSBL8774C22, 90536, dwg 7904278-03.
24	SWITCH, TOGGLE: Miniature, dpdt, sealed; MIL type MS24656-231.

TABLE 7-3. LIST OF COMMON ITEM DESCRIPTIONS (CONT.)

Item Number	Description
25	SWITCH, TOGGLE: Miniature, single pole, panel sealed; MIL type MS24655-231.
26	TERMINAL BOARD: Barrier type, 5 terminals; mfr 75382, part no. 354-28-05-001, 90536, dwg 904862-09.
27	TERMINAL BOARD: Barrier type, 7 terminals; mfr 75382, part no. 600AY7, 90536, dwg 904862-11.
28	TRANSFORMER, POWER, STEPDOWN: Control, single phase, 50-400HZ; mfr 16513, part no. MC4518, 90536, dwg 7904726-00.
29	TRANSISTOR: NPN, silicon, power, Darlington, 80VDC; mfr 04713, part no. MJ4034, 90536, dwg 7904256-01.
30	TRANSISTOR: NPN, Silicon, power, Darlington; mfr 04713, part no. MJ1000, 90536, dwg 7904415-00.
31	TRANSISTOR: NPN, silicon, power, high voltage, 325VDC, 100W; mfr 21845, part no. SDT8821, 90536, dwg 7901448-00.

TABLE 7-4. LIST OF ATTACHING HARDWARE

Letter Code	Name and Description
A	INSULATOR, PLATE: TRANSISTOR, MICA, TO-3, 1.062 in WD, 1.655 in L, 0.002 in THK; mfr 13137, part no. 732.
B	INSULATOR, WASHER: MICA, 0.195 in ID, 0.500 in OD, 0.002 in THK; mfr 08289, part no. MW500-195.
C	INSULATOR, WASHER: MICA, 0.328 in ID, 1.000 in OD, 0.002 in THK; mfr 08289, part no. MW1-328.
D	INSULATOR, WASHER: PLASTIC, 0.260 in ID, 0.800 in OD, 0.002 in THK; mfr 13103, part no. 43-800-260.
E	NUT, PLAIN, HEX: JAM, CRES, 5/16-24UNF-2B; MS35691-15.
F	NUT, PLAIN, HEX: MACH, No. 2, 56UNC THD; MS35649-224.
G	NUT, PLAIN, HEX: MACH, No. 4, 40UNC THD; MS35649-244.
H	NUT, PLAIN, HEX: MACH, No. 4, 40UNC THD; 0.245 in WD across flats, 0.094 in thickness.
I	NUT, PLAIN, HEX: MACH, No. 6, 32UNC THD; MS35649-264.
J	NUT, PLAIN, HEX: MACH, No. 10, 32UNF THD; MS35650-304.
K	NUT, PLAIN, KNURLED: Gulmite type, aluminum, 1/4-40UNS-2B, black, onodized; mfr 07137, part no. 301241-002.
L	NUT, PLAIN, KNURLED: Gulmite type, aluminum, 1/4-40UNS-2B, clear, iridite; mfr 07137, part no. 301241-008.
M	NUT, PLAIN, KNURLED: Gulmite type, aluminum, 1/4-40UNS-2B, dark gray, onodized; mfr 07137, part no. 301241-005.
N	NUT, PLAIN, ROUND: KNURLED, aluminum, 3/8-32NEF-2, black; mfr 07137, part no. 301241-014.

TABLE 7-4. LIST OF ATTACHING HARDWARE (CONT.)

Letter Code	Name and Description
P	NUT, SELF LOCKING, HEX: CRES, 2-56UNC-3B; mfr 72962, part no. 79LH1660-26.
Q	NUT, SELF LOCKING, HEX: CRES, 4-40UNC-3B; MS21044C04.
R	NUT, SELF LOCKING, HEX: CRES, 6-32UNC-3B; MS21044C06.
S	SCREW, MACH, FLH: CRSHD, CRES, 2-56UNC-2A, 0.31 in L; MS51959-4.
T	SCREW, MACH, FLH: CRSHD, CRES, 4-40UNC-2A, 0.375 in L; MS24693C4.
U	SCREW, MACH, FLH: CRSHD, CRES, 4-40UNC-2A, 0.875 in L; MS24693C9.
V	SCREW, MACH, FLH: CRSHD, CRES, 6-32UNC-2A, 0.250 in L; MS24693C24.
W	SCREW, MACH, FLH: CRSHD, CRES, 6-32UNC-2A, 0.375 in L; MS24693C26.
X	SCREW, MACH, FLH: CRSHD, CRES, 6-32UNC-2A, 0.437 in L; MS24693C27.
Y	SCREW, MACH, FLH: CRSHD, CRES, 6-32UNC-2A, 0.500 in L; MS24693C28.
Z	SCREW, MACH, HEX HEAD: CRES, 6-32UNC-2A, 3/8 in L.
AA	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 1/2 in L; MS51957-17.
AB	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 3/4 in L; MS51957-19.
AC	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 3/8 in L; MS51957-15.
AD	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 5/8 in L; MS51957-18.
AE	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 7/16 in L; MS51957-16.

TABLE 7-4. LIST OF ATTACHING HARDWARE (CONT.)

Letter Code	Name and Description
AF	SCREW, MACH, PNH: CRSHD, CRES, 4-40UNC-2A, 9/16 in L.
AG	SCREW, MACH, PNH: CRSHD, CRES, 6-32UNC-2A, 1/4 in L; MS51957-26.
AH	SCREW, MACH, PNH: CRSHD, CRES, 6-32UNC-2A, 1/2 in L; MS51957-30.
AI	SCREW, MACH, PNH: CRSHD, CRES, 6-32UNC-2A, 5/8 in L; MS51957-31.
AJ	SCREW, MACH, PNH: CRSHD, CRES, 6-32UNC-2A, 9/16 in L.
AK	SCREW, MACH, PNH: CRSHD, CRES, 6-32UNC-2A, 11/16 in L.
AL	SCREW, MACH, PNH: CRSHD, CRES, 8-32UNC-2A, 0.375 in L; MS51957-43.
AM	SCREW, MACH, PNH: CRSHD, CRES, 8-32UNC-2A, 1/2 in L; MS51957-45.
AN	SCREW, MACH, PNH: CRSHD, CRES, 10-32UNF-2A, 1/2 in L; MS51958-63.
AP	SCREW, MACH, PNH: CRSHD, CRES, 10-32UNF-2A, 3/4 in L; MS51958-65.
AQ	SCREW, MACH, PNH: CRSHD, CRES, 10-32UNC-2A, 5/16 in L; MS51958-60.
AR	SCREW, SPECIAL FINISH: FLH, 4-40UNC-2A, 3/8 in L; mfr 90536, part no. 7056849-15.
AS	SCREW, SPECIAL FINISH: FLH, 2-56UNC-2A, 5/16 in L; mfr 90536, part no. 7056849-16.
AT	WASHSER, FLAT: ROUND, CRES, No. 2, 0.091 in ID, 0.248 in OD, 0.020 in thickness; MS15795-802.
AU	WASHER, FLAT: ROUND, CRES, No. 4, 0.128 in ID, 0.314 in OD, 0.032 in thickness; MS15795-804.

TABLE 7-4. LIST OF ATTACHING HARDWARE (CONT.)

Letter Code	Name and Description
AV	WASHER, FLAT: ROUND, CRES, No. 6, 0.150 in ID, 0.300 in OD, 0.050 in thickness; MS15795-806.
AW	WASHER, FLAT: ROUND, CRES, No. 8, 0.190 in ID, 0.443 in OD, 0.050 in thickness; MS15795-841.
AX	WASHER, FLAT: ROUND, CRES, No. 10, 0.220 in ID, 0.505 in OD, 0.050 in thickness; MS15795-842.
AY	WASHER, FLAT: CRES, 0.316 in ID, 0.56 in OD, 0.031 in thickness, mfr 00538, part no. 7126395-00.
AZ	WASHER, LOCK: INT TOOTH, No. 10, 0.200 in ID, 0.400 in OD, 0.023 in tnickness; MS35335-32.
BA	WASHER, LOCK: SPRING, CRES, No. 2, 0.092 in ID, 0.175 in OD, 0.035 in WD, 0.023 in thickness; MS35338-134.
BB	WASHER, LOCK; SPRING, CRES, No. 4, 0.120 in ID, 0.212 in OD, 0.040 in WD, 0.028 in thickness; MS35338-135.
BC	WASHER, LOCK: SPRING, CRES, No. 6, 0.146 in ID, 0.253 in OD, 0.047 in WD, 0.034 in thickness; MS35338-136.
BD	WASHER, LOCK: SPRING, CRES, No. 8, 0.172 in ID, 0.296 in OD, 0.055 in WD, 0.043 in thickness; MS35338-137.
BE	WASHER, LOCK: SPRING, CRES, No. 10, 0.200 in ID, 0.337 in OD, 0.062 in WD, 0.500 in thickness; MS35338-138.
BF	WASHER, PACKING, PREFORMED: "O" ring, oil resistant rubber, 0.239 in ID, 0.379 in WD; AN6227-5.
BG	WASHER, PLAIN: FLAT, CRES, No. 0, 0.063 in ID, 0.099 in OD, 0.016 in thickness; MS35260.

TABLE 7-4. LIST OF ATTACHING HARDWARE (CONT.)

Letter Code	Name and Description
BH	WASHER, PLAIN: FLAT, CRES, No. 4, 0.115 in ID, 0.209 in OD, 0.032 in thickness; MAS620C4.
BJ	WASHER, PLAIN: Flat, CRES, No. 8, 0.169 in ID, 0.304 in OD, 0.032 in thickness; MAS620C8.
BK	WASHER, PLAIN: FLAT, CRES, 1/4 size, 0.255 in ID, 0.468 in OD, 0.063 in thickness; MAS620C416.
BL	WASHER, SHOULDERED: FIBRE, INSULATING, flanged, No. 6, 0.138 in ID, 0.187 in ID shldr dia, 0.312 in OD; mfr 83330, part no. 2153.
BM	WASHER, SHOULDERED: FIBRE, INSULATING, flanged, No. 10, 0.190 in ID, 0.308 in ID shldr dia, 0.380 in OD; mfr 83330, part no. 2156.
BN	WASHER, SHOULDERED: PLASTIC, 5/16 size, teflon, 0.325 in ID, 0.415 in ID shldr dia, 0.500 in OD; mfr 86684, part no. 495334-6.

TABLE 7-5. LIST OF MANUFACTURERS

Vendor Code	Name	Address
00736	Filter Products, Div of North American Rockwell Corp, Air-Maze Plant	25000 Miles Road Cleveland, OH 44128
03877	Transistron Electronic Corp	168-186 Albion Street Wakefield, MA 01880
04713	Motorola Inc Semiconductor Products Division	5005 East McDowell Road Phoenix, AZ 85008
07137	TEC Inc	6700 Washington Ave South Eden Prairie, MN 55343
08289	Blirn Delbert Co., Inc., The	1678 East Mission Blvd P. O. Box 2007 Pomona, CA 91766
11502	TRW Electronic Components, IRC Fixed Resistors, Boone Div	Greenway Road Boone, NC 28607
12969	Unitrode Corp	580 Pleasant Street Watertown, MA 02172
13103	Thermalloy Co	P. O. Box 34829 2021 West Valley View Lane Dallas, TX 75234
13137	Mica Fabricating Co	55 Central Ave Rochelle Park, NJ 07662
14674	Corning Glass Works	Houghton Park Corning, NY 14830
16512	Fabri-Tek Inc, National Connector Division	9210 Science Center Drive New Hope, MN 55428
16513	Mag-Con Inc	85 2nd Ave Southeast New Brighton, MN 55112
18234	Lindgren Erik A. and Associates, Inc	4515 North Ravenswood Chicago, IL 60640
21845	Solitron Devices, Inc Transistor Division	1177 Blue Heron Blvd Riviera Beach, FL 33404
31356	J-B-T Instruments, Inc	424 Chapel Street P. O. Box 1818 New Haven, CT 06508

TABLE 7-5. LIST OF MANUFACTURERS (CONT.)

Vendor Code	Name	Address
37942	Mallory, P. R. and Co., Inc	3029 East Washington Street Indianapolis, IN 46206
56289	Sprague Electric Co	North Adams, MA 01247
71279	Cambridge Thermionic Corp	445 Concord Ave Cambridge, MA 02138
71785	TRW Electronic Components, Cinch Division	1501 Morse Ave Elk Grove Village, IL 60007
72962	Elastic Stop Nut, Division of Amerace ESNA Corp	2330 Vauxhall Road Union, NJ 07083
75382	Kulka Electric Corp	633-643 South Fulton Ave Mount Vernon, NY 10550
81312	Winchester Electronics, Division of Litton Industries Inc	Main Street and Hillside Ave Oakville, CT 06779
82227	North American Philips Controls Corp	P. O. Box 768 Fip Raod Cheshire, CT 06410
82877	Rotron, Inc	7-9 Hasbrouck Lane Woodstock, NY 12498
83330	Smith, Herman H., Inc	812 Snediker Ave Brooklyn, NY 11207
86684	RCA Corp., Electronic Components	415 South 5th Street Harrison, NJ 07029
90536	Sperry Univac, Defense Systems	Univac Park P. O. Box 3525 St. Paul, MN 55165

CHAPTER 8

INSTALLATION

8-1. INTRODUCTION.

8-2. This chapter describes the installation of the Data Processing Set (DPS) for either rack mounting or table top operation. Included are dimensional drawings, cabling information, and test procedures to facilitate the installing of the DPS.

8-3. INSTALLATION INSTRUCTIONS.

8-4. TOOLS AND MATERIALS. No special tools are required for installation.

8-5. UNPACKING AND REPACKING. Perform the following steps for unpacking.

1. Remove thinwall nails at the bottom of the crate that go into the skid.

2. Remove steel bands.

3. Lift up crate from unit.

4. Remove upper cushioning insert if it remained on top of unit.

5. Lift unit up from lower cushioning insert and skid.

6. Inspect outside of unit for physical damage. All damage should be reported.

7. If possible, retain the shipping crate and cushioning inserts for reshipment at a later date.

8-6. For repacking, perform the following steps.

1. Repacking in original shipping crate if kept.

   a. Place cushion insert on skid.

   b. Place unit on cushion insert.

   c. Place cushion insert on top of unit.

   d. Place crate over top of unit and down resting on cushion.

   e. Nail sides of crate to skid using four thinwall nails per side.

   f. Place metal strap around crate.

   g. Place label on crate.

2. Repacking in made up crate.

a. Place unit in a corrugated cardboard inner container, with corrugated cardboard spacers or one-inch polyurethane foam at front and rear to protect switches, indicators, and connectors.

b. Place inner container into a cleated panel outer container with space between filled with at least four inches of two-pound density polyurethane foam or equivalent.

8-7. PREPARATION OF FOUNDATION. The rack should be prepared to provide sufficient space to receive the DPS, and be drilled to receive the eight mounting bolts and two shock pins. Refer to figure 8-1 for the space requirements and position and size of the mounting holes. The rack must be able to support the 200 pound weight of the DPS. For table top installation, make sure the proper space is available and the table is capable of supporting the DPS's 200 pounds.

8-8. INPUT REQUIREMENTS. Refer to paragraph 1-35 and table 1-1 for input power requirements for the various options.

8-9. INSTALLATION PROCEDURES.

1. Rack Mounting

a. Use an allen wrench to loosen the eight screws that hold the maintenance panel door closed.

b. Open the maintenance panel door.

c. Remove and mark the three ribbon cable connectors from J01, J02, and J03 (upper left on maintenance panel).

d. Remove the power cable from the cable clamps on the maintenance panel door.

e. Use a slotted screwdriver to unscrew the power cable connector clamp connected to J04 (upper left on the maintenance panel.

f. Use a phillips screwdriver and remove the left holding bracket of the telescoping door stop

g. Use phillips screwdriver and remove the four screws that hold the two maintenance panel door hinges in place. Remove door.

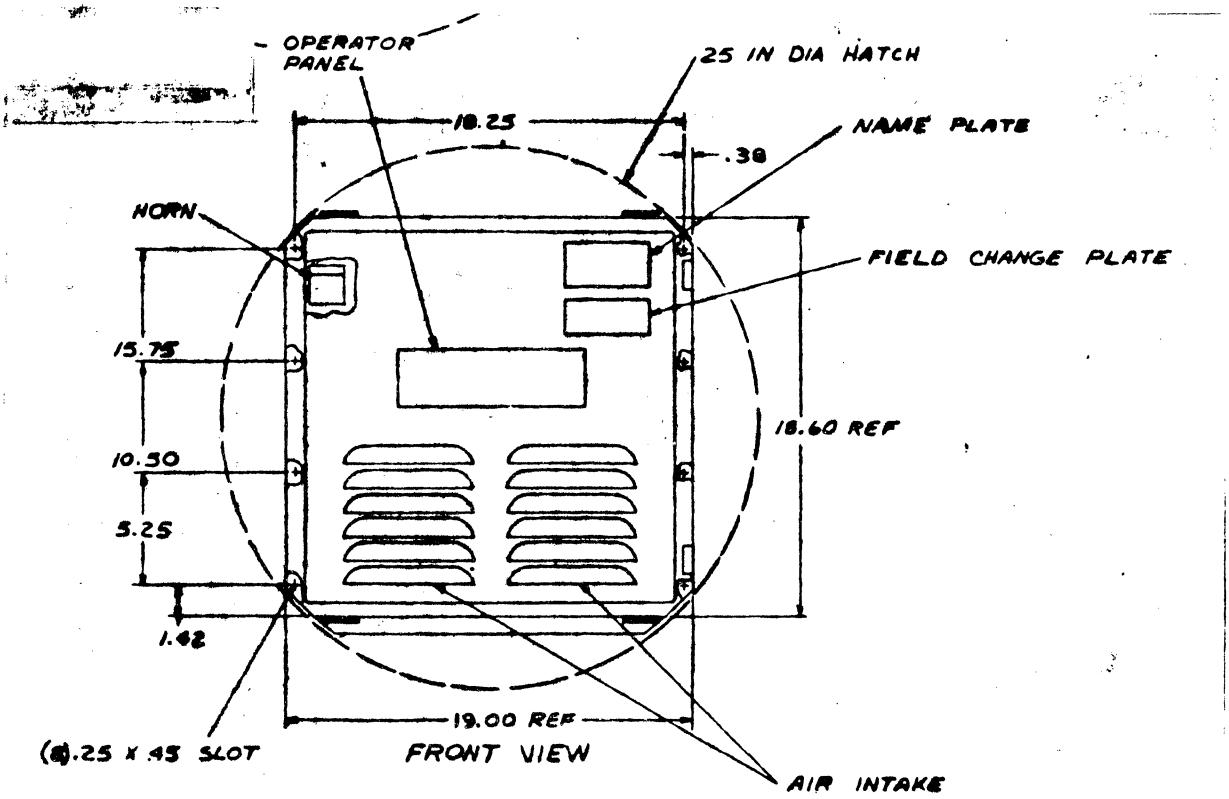
h. Lift the DPS into place in the rack.

i. Using eight bolts, bolt the DPS in place.

j. Remount the maintenance panel door using the four phillip head screws to hold the two hinges in place.

k. Remount the left holding bracket of the telescoping door stop.

l. Connect the power cable to J04.



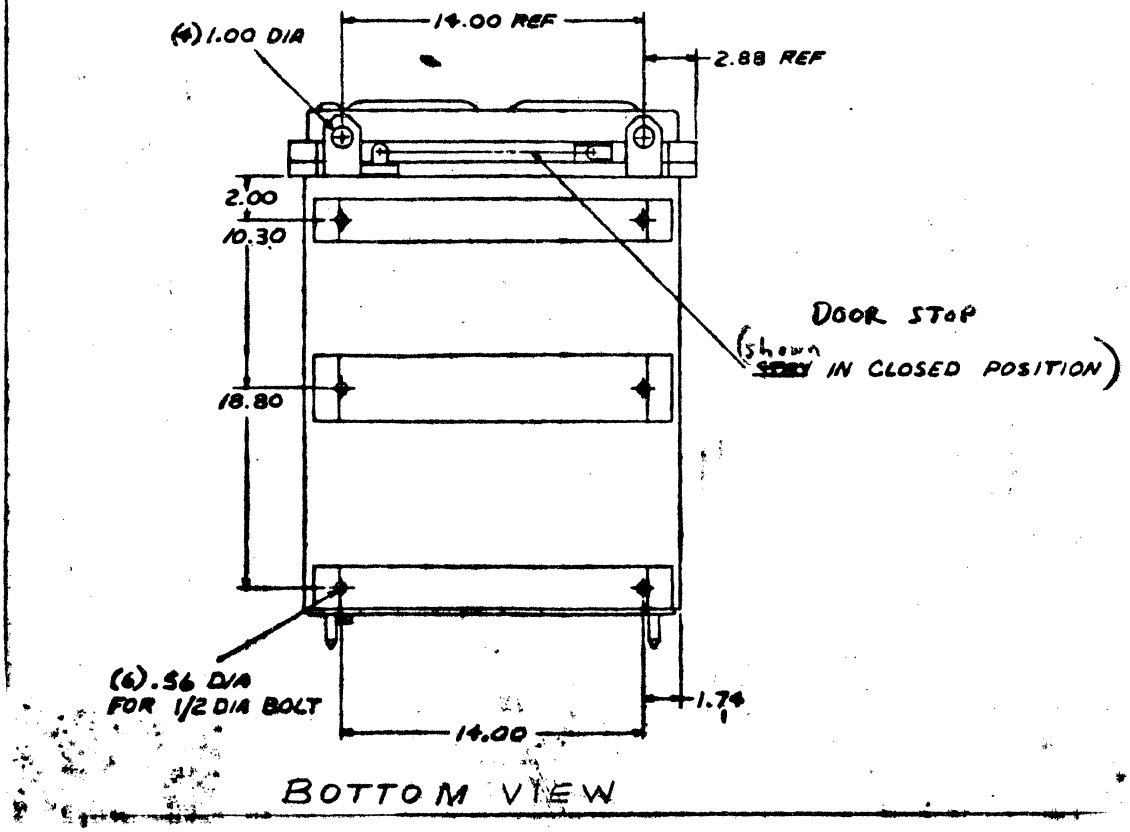


Figure 8-1a. DPS Outline Drawing

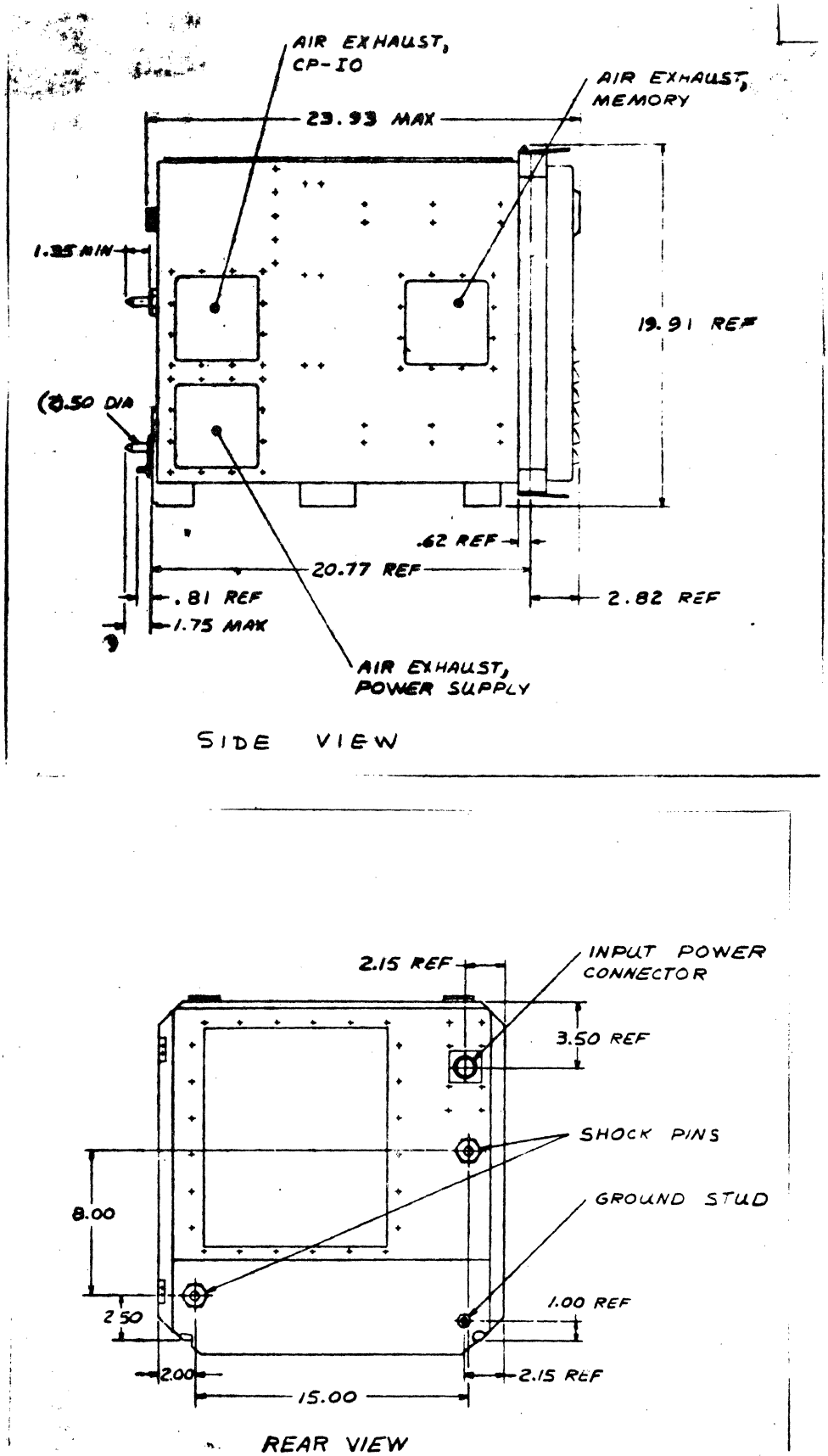


Figure 8-1b. DPS Outline Drawing

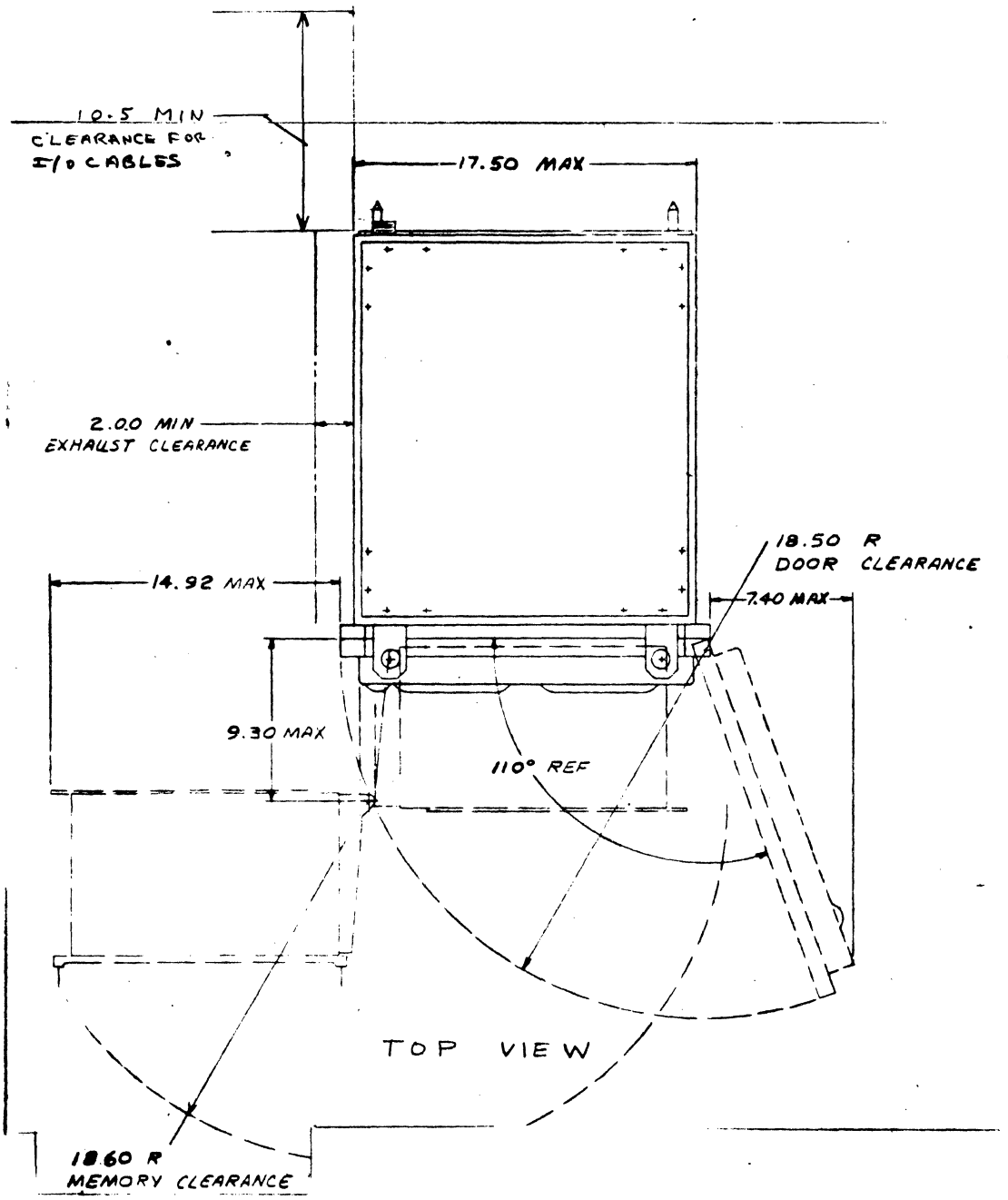


Figure 8-1c. DPS Outline Drawing (To Serial 4)

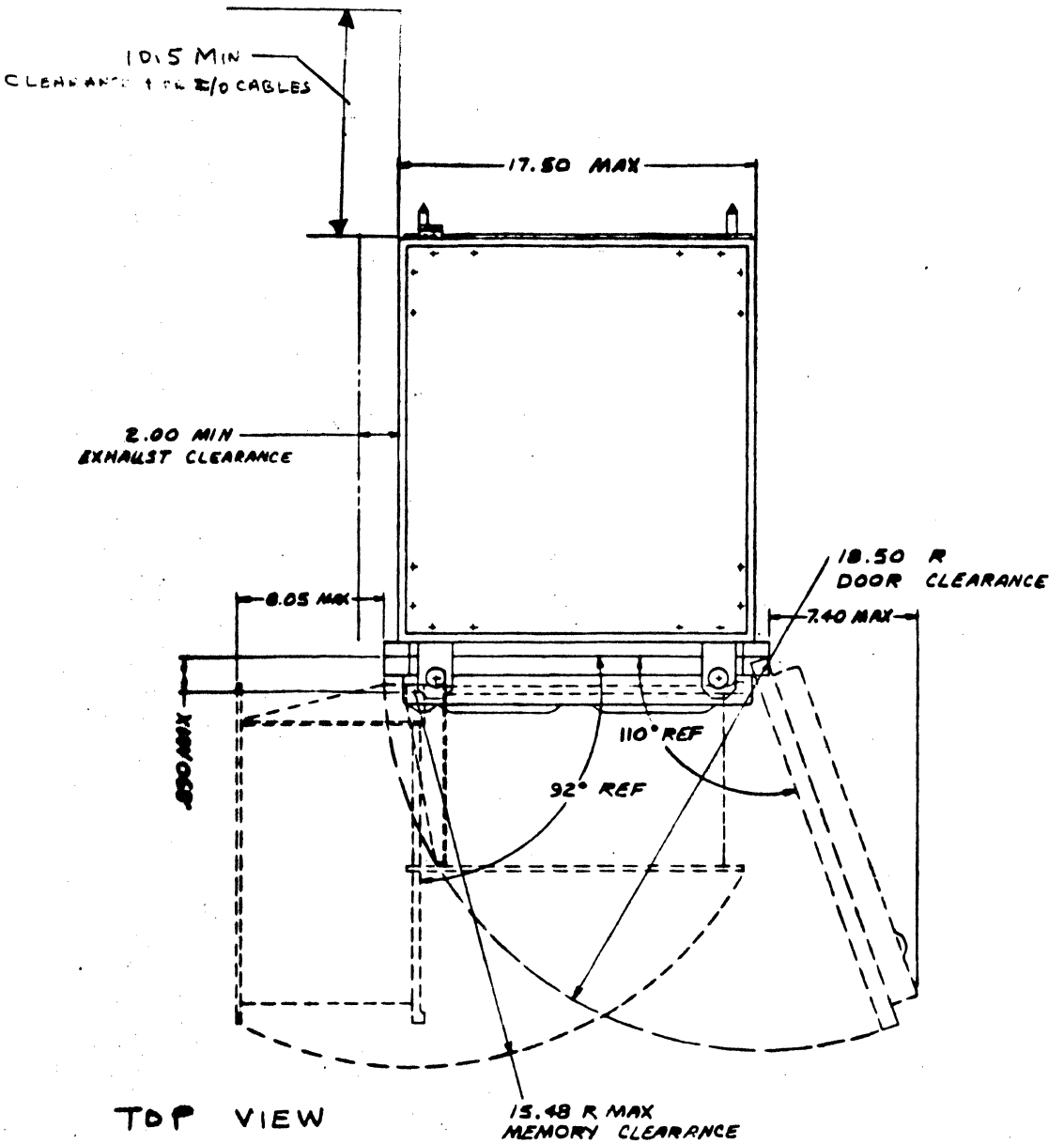


Figure 8-1d. DPS Outline Drawing (From Serial 4

m. Place the cable back in the cable clamps.

n. Replace the three ribbon cable connectors to J01, J02, and J03.

o. Unlatch the telescoping door stop and close the maintenance panel door.

p. Fasten the eight bolts to secure the door.

2. Table Mounting

a. Place DPS on table as close to final position as possible.

b. Use an allen wrench and unscrew the eight screws holding the maintenance panel door closed.

c. Open the maintenance panel door.

d. Loosen the four screws holding the memory chassis closed.

e. Slide out the memory chassis.

f. Remove the CP/IOC chassis as indicated in Chapter 6.

g. Remove the power supply chassis as indicated in Chapter 6.

h. Remove the power supply blower as indicated in Chapter 6.

i. Move DPS to align mounting holes.

j. Use the front two and back two mounting holes and mount the DPS to the table.

k. Replace the power supply blower as indicated in Chapter 6.

l. Replace the power supply chassis as indicated in Chapter 6.

m. Replace the CP/IOC chassis as indicated in Chapter 6.

n. Swing in memory chassis and push in slide.

o. Lock memory chassis in place with the four screws.

p. Close the maintenance panel door and secure with the eight screws.

8-10. INSTALLATION CHECKOUT.

8-11. INSPECTION.

1. Before connecting the power cable, use a meter to verify that the proper voltages are available. Table 8-1 shows the voltage on each pin.

2. Connect the input/output cables per system definition to the various jacks as indicated in figure 8-2. Tables 8-2 through 8-5 show I/O cable pin assignments.

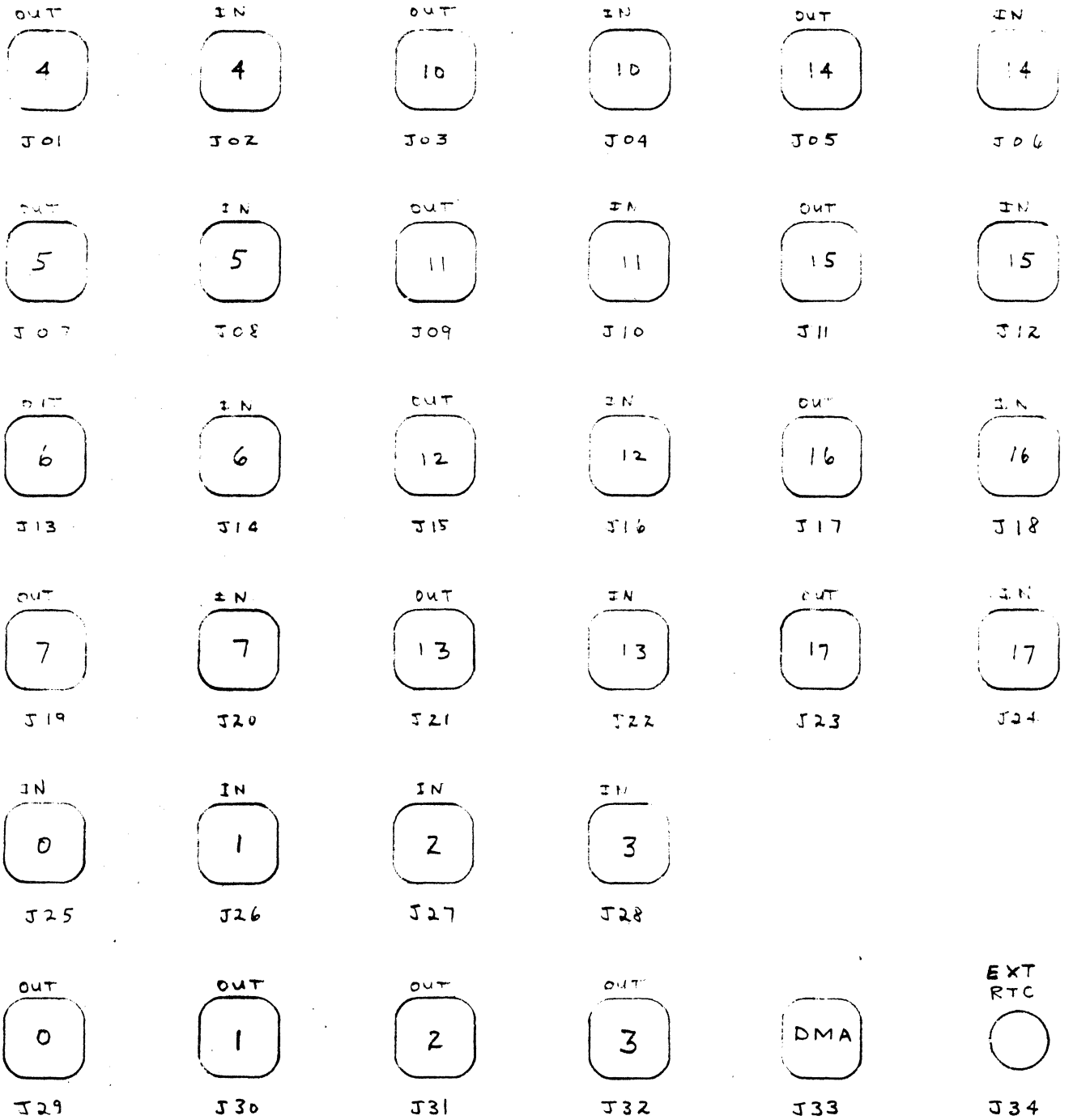


Figure 8-2. Input/Output Channel Assignments

TABLE 8-1. POWER CONNECTOR PIN ASSIGNMENTS

PIN #	1Ø	3ØY	3Ø△
A	115 Vac	115 Vac Line to Neut.	115 Vac Line to Line
B	Neutral	115 Vac Line to Neut.	115 Vac Line to Line
C	Not Used	115 Vac Line to Neut.	115 Vac Line to Line
D	Not Used	Neutral	Not Used
E	Safety Ground	Safety Ground	Safety Ground
F	Not Used	Not Used	Not Used
G	Not Used	Not Used	Not Used

TABLE 8-2. PARALLEL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS (EVEN GROUP*)

FUNCTION		CONNECTOR PIN	
INPUT	OUTPUT	SIGNAL	RETURN
Input Data Request	Output Acknowledge	B-5	A-5
Input Acknowledge	Output Data Request	B-6	A-6
External Interrupt Request	External Function Acknowledge	B-7	A-7
External Interrupt Enable	External Function Request	B-8	A-8
Data Bit 00		D-1	C-1
Data Bit 01		D-2	C-2
Data Bit 02		D-3	C-3
Data Bit 03		D-4	C-4
Data Bit 04		D-5	C-5
Data Bit 05		D-6	C-6
Data Bit 06		D-7	C-7
Data Bit 07		D-8	C-8
Data Bit 08		D-9	C-9
Data Bit 09		D-10	C-10
Data Bit 10		D-11	C-11
Data Bit 11		D-12	C-12
Data Bit 12		G-1	H-1
Data Bit 13		G-2	H-2
Data Bit 14		G-3	H-3
Data Bit 15		G-4	H-4

*Even Groups - Group 0, Channels 0-3; Group 2, Channels 10-13 (Octal)

TABLE 8-2. PARALLEL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS (EVEN GROUP*) (CONT)

FUNCTION		CONNECTOR PIN	
INPUT	OUTPUT	SIGNAL	RETURN
	Dual Channel Data Bit 16	G-5	H-5
	Dual Channel Data Bit 17	G-6	H-6
	Dual Channel Data Bit 18	G-7	H-7
	Dual Channel Data Bit 19	G-8	H-8
	Dual Channel Data Bit 20	G-9	H-9
	Dual Channel Data Bit 21	G-10	H-10
	Dual Channel Data Bit 22	G-11	H-11
	Dual Channel Data Bit 23	G-12	H-12
	Dual Channel Data Bit 24	J-1	K-1
	Dual Channel Data Bit 25	J-2	K-2
	Dual Channel Data Bit 26	J-3	K-3
	Dual Channel Data Bit 27	J-4	K-4
	Dual Channel Data Bit 28	J-5	K-5
	Dual Channel Data Bit 29	J-6	K-6
	Dual Channel Data Bit 30	J-7	K-7
	Dual Channel Data Bit 31	J-8	K-8

*Even Groups - Group 0, Channels 0-3; Group 2, Channels 10-13 (Octal)

TABLE 8-3. PARALLEL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS (ODD GROUP*)

FUNCTION		CONNECTOR PIN	
INPUT	OUTPUT	SIGNAL	RETURN
Input Data Request	Output Acknowledge	B-5	A-5
Input Acknowledge	Output Data Request	B-6	A-6
External Interrupt Request	External Function Acknowledge	B-7	A-7
External Interrupt Enable	External Function Request	B-8	A-8
	Data Bit 00	D-1	C-1
	Data Bit 01	D-2	C-2
	Data Bit 02	D-3	C-3
	Data Bit 03	D-4	C-4
	Data Bit 04	D-5	C-5
	Data Bit 05	D-6	C-6

*Odd Groups - Group 1, Channels 4-7; Group 3, Channels 14-17 (Octal)

TABLE 8-3. PARALLEL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS (ODD GROUP*) (CONT)

FUNCTION		CONNECTOR PIN	
INPUT	OUTPUT	SIGNAL	RETURN
	Data Bit 06	D-7	C-7
	Data Bit 07	D-8	C-8
	Data Bit 08	D-9	C-9
	Data Bit 09	D-10	C-10
	Data Bit 10	D-11	C-11
	Data Bit 11	D-12	C-12
	Data Bit 12	G-1	H-1
	Data Bit 13	G-2	H-2
	Data Bit 14	G-3	H-3
	Data Bit 15	G-4	H-4
Dual Channel Data Bit 00		F-1	E-1
Dual Channel Data Bit 01		F-2	E-2
Dual Channel Data Bit 02		F-3	E-3
Dual Channel Data Bit 03		F-4	E-4
Dual Channel Data Bit 04		F-5	E-5
Dual Channel Data Bit 05		F-6	E-6
Dual Channel Data Bit 06		F-7	E-7
Dual Channel Data Bit 07		F-8	E-8
Dual Channel Data Bit 08		F-9	E-9
Dual Channel Data Bit 09		F-10	E-10
Dual Channel Data Bit 10		F-11	E-11
Dual Channel Data Bit 11		F-12	E-12
Dual Channel Data Bit 12		B-9	A-9
Dual Channel Data Bit 13		B-10	A-10
Dual Channel Data Bit 14		B-11	A-11
Dual Channel Data Bit 15		B-12	A-12

*Odd Groups - Group 1, Channels 4-7; Group 3, Channels 14-17 (Octal)

TABLE 8-4. SERIAL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS

FUNCTION		CONNECTOR PIN	
MIL-STD-188	RS-232	EVEN GROUP*	ODD GROUP**
A	Loop Test	D-8	G-4
B	Ring Indicator	D-4	D-12
C	Received Line Signal Detector	C-4	C-12
D	Data Terminal Ready	C-8	H-4
E	Clear To Send	D-5	G-1
F	New Sync.	D-7	G-3
G	Request To Send	C-7	H-3
H		D-6	G-2
I		D-3	D-11
J		C-6	H-2
K	Data Set Ready	C-3	C-11
L		D-2	D-10
Transmit Clock	Transmitter Signal Element Timing	B-5	
Transmit Data	Transmitted Data	A-5	
Receive Clock	Receiver Signal Element Timing	A-7	
Receive Data	Receive Data	B-7	
Signal Ground	Signal Ground	A-6, A-8	

*Even Group - Channels 0,1; 4,5; 10,11; and 14,15 (Octal)

**Odd Group - Channels 2,3; 6,7; 12,13; and 16,17 (Octal)

TABLE 8-5. DUAL CHANNEL I/O JUMPER PLUG PIN ASSIGNMENTS

FUNCTION	ORIGIN		DESTINATION	
	SIGNAL	RETURN	SIGNAL	RETURN
Data Bit 00	D-1	C-1	F-1	E-1
Data Bit 01	D-2	C-2	F-2	E-2
Data Bit 02	D-3	C-3	F-3	E-3
Data Bit 03	D-4	C-4	F-4	E-4
Data Bit 04	D-5	C-5	F-5	E-5
Data Bit 05	D-6	C-6	F-6	E-6
Data Bit 06	D-7	C-7	F-7	E-7
Data Bit 07	D-8	C-8	F-8	E-8
Data Bit 08	D-9	C-9	F-9	E-9
Data Bit 09	D-10	C-10	F-10	E-10
Data Bit 10	D-11	C-11	F-11	E-11
Data Bit 11	D-12	C-12	F-12	E-12
Data Bit 12	G-1	H-1	B-9	A-9
Data Bit 13	G-2	H-2	B-10	A-10
Data Bit 14	G-3	H-3	B-11	A-11
Data Bit 15	G-4	H-4	B-12	A-12

TABLE 8-6. EXTERNAL REAL TIME CLOCK CONNECTOR PIN ASSIGNMENTS

FUNCTION	CONNECTOR PIN
Spare	A
Spare	B
H → External Real Time Clock	C
L → External Real Time Clock	D
Spare	E
Spare	F

3. Connect the ground strap to the ground stud. The location of the stud is shown in figure 8-1.

4. Connect the external real time clock cable to jack 34, if required. The position of this jack is shown in figure 8-2. Table 8-6 shows connector pin assignments.

8-12. INITIAL TEST.

1. Set the switches on the control panel and maintenance panel to the positions indicated in table 2-4.

2. Set the CIRCUIT BREAKER switch on the operator's control panel to the ON position.

3. Set the POWER BLOWER switch to the ON position. Make sure that the blower is discharging air from the exhaust grills on the side of the cabinet. The power blower indicator should be lit.

4. Set the POWER LOGIC switch to the ON position. The indicator should be lit. The FAULT POWER and OVERTEMP indicators should not be lit. If either one or both are lit refer to section five (troubleshooting).

5. Use a meter and check the logic voltages. Refer to table 8-7 for description of the logic voltages. The voltages on TB4 should be made in reference with processor signal ground (E10). All voltages have 5% tolerences. TB3 and 4 are located at the bottom middle on the front of the power supply.

8-13. INSTALLATION VERIFICATION TEST. Run the diagnostic tests listed in chapter 10 to verify the operation of the DPS. These tests procedd logically through the equipment using operational circuits to test the untried areas and provide corrective instructions if the results are not as specified.

8-14. INSTALLATION SUMMARY SHEET. Use the installation summary sheet shown in figure 8-3 to record the verification of each test.

TABLE 8-7. LOGIC VOLTAGES

LUG NO.	DESCRIPTION
TB3	
1	-5.2 volts
2	-5.2 volts return
3	+12 volts
4	+12 volts return
5	-16 volts
6	-16 volts return
7	Spare
TB4	
1	Spare
2	+15 volts
3	+15 volts sense
4	-5 volts
5	Memory Signal Ground
6	+5 volts memory
7	Spare
E9	
+5 volts processor	
E10	
Processor Signal Ground	

INSTALLATION SUMMARY SHEET

OPERATION	VERIFICATION CHECK	
	OK	NOT OK
Power cable voltage		
I/O cables connected to proper jacks		
DMA cable connected to jack 33		
External real time clock connected to jack 34		
Blower operating correctly		
Power came up properly		
Logic voltages correct		
Diagnostic Test		

Figure 8-3. Installation Summary Sheet

APPENDIX A

MICROINSTRUCTION REPERTOIRE

Instructions defined in this appendix are the DPS microinstructions. The format used is a 16-bit instruction divided into four equal 4-bit fields. The F-field specifies the function code. The D-field (Table A-2) defines the destination register. The S-field (Table A-1) is the source field for data. The M-field is used as a microinstruction modifier.

Symbols used in microinstructions

Symbol	Description
A_0-A_7	Scratch pad registers
D	Destination field
F	Function code
K	Constant
M	Microinstruction modifier field
P	Program address register
Ra.	The register designated by a
Rm.	The register designated by m
S	Source field
μP	Micro P register
μP Hold	Micro P hold register
( )	The contents of the location specified within the parenthesis
→	Transfer to

Table A-1. S-Designator

S VALUE	SOURCE 1 (S1)	SOURCE 2 (S2)
0	Unassigned	μP Hold Register
1	Breakpoint	Condition Register
2	P Register	Display Register
3	Memory Data Register	Normalize/Panel Select
4	Page Registers	RTC Upper
5	Indirect Address Pointer	STATUS 1 Register
6	Shift Matrix Output	STATUS 2 Register
7	Monitor Clock/Feed/Partial Product (Determined by F = 15, FII = 10)	RTC Lower
10	A0	General Register
11	A1	Cordic Table
12	A2	Instruction Register AM Sign Extended
13	A3	Instruction Register
14	A4	Class I & II Interrupt Code
15	A5	Class III Interrupt Code/I/O Translator
16	A6	Input Data
17	A7	I/O Control Memory

Table A-2. D-Designator

D VALUE	DESTINATION 1 (D1)	DESTINATION 2 (D2)
0	Unassigned	μP Register
1	Breakpoint	Condition Register
2	P Register	Display Register
3	Memory Data Register	Cycle Counter
4	General Register	RTC Upper
5	Status Register #1	Unassigned
6	Status Register #2	Unassigned
7	RTC Lower	Unassigned
10	A0/Shift Register R1/Page Address Counter	Page Registers
11	A1/Shift Register R2	Unassigned
12	A2	Instruction Register/SGR
13	A3	SGR
14	A4	CM Translator
15	A5	I/O Translator
16	A6/Shift Counter	Output Data
17	A7/Memory Address Register	I/O Control Memory (CM)

F = 00 TRANSFER

0000	D	S	M

Transfer the contents of the source register as specified by S (Table A-1) and modified by M to the destination register as specified by D (Table A-2) and modified by M. M designator usage as shown below in Table A-3.

Table A-3. M-Designator for Microinstruction F=00

M		FUNCTION
3	2 1 0	
0	X X X	Do not update the Condition register
1	X X X	Update the Condition register
X	0 X X	Transfer direct
X	1 X X	Transfer data rotated left circularly 8 bit positions
X	X 0 0	Transfer (S1) to D1
X	X 0 1	Transfer (S2) to D1
X	X 1 0	Transfer (S1) to D2
X	X 1 1	Transfer (S2) to D2

F = 01 JUMP

0001	X

Transfer (μP) to μP HOLD, Load μP with X, then execute the microinstruction at address X.

F = 02 ADD

0010	D1	S2	M

Add the contents of the source register as specified by S2 (Table A-1) to the value specified by M (Table A-4) and transfer the sum to D1 (Table A-2).

Table A-4. M-Designator for Microinstruction F=02

M		FUNCTION
3	2 1 0	
0	X X X	Do not update the Condition register
1	X X X	Update the Condition register
X	0 0 0	(S2) + (A_n)* → D1, Force carry
X	0 0 1	(S2) + (A_n)* → D1, Carry hold
X	0 1 0	(S2) + (A_n)* → D1, Carry end around
X	0 1 1	(S2) + (A_n)* → D1, No carry
X	1 0 0	(S2) + POS ZERO → D1, Force carry
X	1 0 1	(S2) + NEG ONE → D1, Carry hold
X	1 1 0	(S2) + POS ZERO → D1, Carry end around
X	1 1 1	(S2) + NEG ONE → D1, No carry

*The least significant 2 bits of D1 specify one of the registers A0-A3 as operand source.

F = 03 SHIFT

0011	D1	S1	M

Shift S1 (Table A-1) one bit position as specified by M (Table A-5) and transfer the result to D1 (Table A-2).

Table A-5. M-Designator for Microinstruction F=03

M		FUNCTION
3	2 1 0	
0	X X X	Do not update the Condition register
1	X X X	Update the Condition register
X	0 X X	Shift left 1 bit position
X	1 X X	Shift right 1 bit position
X	X 0 0	Zero fill (right or left shift)
X	X 0 1	Sign fill (right shift) or circular (left shift)
X	X 1 0	Insert the bit shifted off in previous shift operation
X	X 1 1	Insert special (reserved for serial I/O data operations)

F = 04 ADD

0100	D1	S1	M

Add the contents of the source register S1 (Table A-1) to the value specified by M (Table A-6) and transfer the sum to D1 (Table A-2).

Table A-6. M-Designator for Microinstruction F=04

M		FUNCTION
3	2 1 0	
0	X X X	Do not update the Condition register
1	X X X	Update the Condition register
X	0 0 0	(S1) + (A_n)* → D1, Force carry
X	0 0 1	(S1) + (A_n)* → D1, Carry hold
X	0 1 0	(S1) + (A_n)* → D1, Carry end around
X	0 1 1	(S1) + (A_n)* → D1, No carry
X	1 0 0	(S1) + POS ZERO → D1, Force carry
X	1 0 1	(S1) + NEG ONE → D1, Carry hold
X	1 1 0	(S1) + POS ZERO → D1, Carry end around
X	1 1 1	(S1) + NEG ONE → D1, No carry

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 05 SUBTRACT

0101	D1	S1	M

Subtract the contents of the source register S1 (Table A-1) from the value specified by M (Table A-7) and transfer the difference to D1 (Table A-2).

Table A-7. M-Designator for Microinstruction F=05

M		FUNCTION
3	2 1 0	
0	X X X	Do not update the Condition register
1	X X X	Update the Condition register
X	0 0 0	(A_n)* - (S1) → D1, Force carry
X	0 0 1	(A_n)* - (S1) → D1, Carry hold
X	0 1 0	(A_n)* - (S1)→ D1, Carry end around
X	0 1 1	(A_n)* - (S1) → D1, No carry
X	1 0 0	POS ZERO - (S1) → D1, Force carry
X	1 0 1	POS ZERO - (S1) → D1, Carry hold
X	1 1 0	POS ZERO - (S1) → D1, Carry end around
X	1 1 1	POS ZERO - (S1) → D1, No carry

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 06 LOGIC I

0110	D1	S1	M

Perform the logic function specified by M (Table A-8) and transfer the result to D1 (Table A-2).

Table A-8. M-Designator for Microinstruction F=06

M		FUNCTION	
3	2 1 0		
0	X X X	Do not update the condition register	
1	X X X	Update the condition register	
X	0 0 0	Logical Exclusive OR of $(A_n)^*$ and (S1)	$(A_n)^* \oplus (S1)$
X	0 0 1	Logical complement of the logical AND of $(A_n)^*$ and (S1)	$\overline{(A_n)^* \cdot (S1)}$
X	0 1 0	Logical AND of $(A_n)^*$ and the logical complement of (S1)	$(AX)^* \cdot \overline{(S1)}$
X	0 1 1	Logical complement of (S1)	$\overline{(S1)}$
X	1 0 0	Logical OR of $(A_n)^*$ and (S1)	$(A_n)^* + (S1)$
X	1 0 1	All ones	1
X	1 1 0	$(A_n)^*$	$(A_n)^*$
X	1 1 1	Logical OR of $(A_n)^*$ and the logical complement of (S1)	$(A_n)^* + \overline{(S1)}$

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 07 LOGIC II

0111	D1	S1	M

Perform the Logic function specified by M (Table A-9) and transfer the result to D1 (Table A-2).

Table A-9. M-Designator for Microinstruction F=07

M		FUNCTION	
3	2 1 0		
0	X X X	Do not update the Condition register	
1	X X X	Update the Condition register	
X	0 0 0	Logical AND of the logical complement of $(A_n)^*$ and (S1)	$(A_n)^* \cdot (S1)$
X	0 0 1	Logical complement of $(A_n)^*$	$\overline{(A_n)^*}$
X	0 1 0	All zeros	0
X	0 1 1	Logical complement of the logical OR of $(A_n)^*$ and (S1)	$\overline{(A_n)^* + (S1)}$
X	1 0 0	(S1)	(S1)
X	1 0 1	Logical OR of the logical complement of $(A_n)^*$ and (S1)	$\overline{(A_n)^*} + (S1)$
X	1 1 0	Logical AND of $(A_n)^*$ and (S1)	$(A_n)^* \cdot (S1)$
X	1 1 1	Logical complement of the logical Exclusive OR of $(A_n)^*$ and (S1)	$\overline{(A_n)^* + (S1)}$

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 10 ADD CONSTANT

1000	D1	K

Add the 8 bit constant K (zeros extended to 16 bits) to the accumulator (A_n)* and transfer the sum to D1 (Table A-2).

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 11 SUBTRACT CONSTANT

1001	D1	K

Subtract the 8 bit constant K (zeros extended to 16 bits) from the accumulator (A_n)* and transfer the difference to D1 (Table A-2).

*The least significant 2 bits of D1 specify one of the registers A0-A3 as the operand source.

F = 12 TRANSFER CONSTANT

1010	D1	K

Transfer the 8 bit constant K (zeros extended to 16 bits) to D1 (Table A-2).

F = 13 TRANSFER CONSTANT

1011	D2	K

Transfer the 8 bit constant K (zeros extended to 16 bits) to D2 (Table A-2).

F = 14 BRANCH

1100	FII	K

If the branch condition specified by FII (Table A-10) is satisfied, transfer (μP) to μP HOLD and load bits 0-7 of μP with K leaving bits 8-11 of μP unchanged. Then execute the microinstruction at the address in μP. If the branch condition specified by FII is not satisfied, the MPC will perform the next instruction as programmed.

Table A-10. FII Designator for Microinstruction F=14

FII				BRANCH CONDITION
11	10	9	8	
0	0	0	0	Last arithmetic operation result had negative sign (COND register bit 14 set).
0	0	0	1	Last operation had a result of zero (COND register bit 13 set).
0	0	1	0	Greater than (COND register $[2^{11} \oplus 2^{12}] \oplus 2^{10} = 1$).
0	0	1	1	Overflow, add or subtract (COND register $\overline{[2^{11} \cdot 2^{14}] + 2^{12}} = 1$)
0	1	0	0	$\overline{\text{Carry}}$ (COND register bit 10 set)
0	1	0	1	Inside limits (COND register $2^9 \cdot [(2^{11} \oplus 2^{12}) \oplus 2^{10}] = 1$)
0	1	1	0	Double precision zero (COND register $2^8 + 2^{13} = 1$)
0	1	1	1	Shift save = 0 (COND register bit 15 set)
1	0	0	0	Last operation was not zero (COND register bit 13 = 1)
1	0	0	1	Cycle count = 0
1	0	1	0	A $\neq$ M (increment instruction register AM)
1	0	1	1	Fast shift busy
1	1	0	0	Floating point interrupt enable (status register #1 $2^7 = 0$)
1	1	0	1	Floating point round (status register #1 $2^6 = 0$)
1	1	1	0	Class II I/O interrupt disable (status register #1 $2^2 = 0$)
1	1	1	1	Micro jump switch

F = 15 MICRO CONTROL

1101	FII	S	M

This microinstruction performs micro control functions as described in Table A-11. F = 10_8 controls shifting operations as follows: for single precision operations, it causes the shifting of one 16 bit register A_0. For double precision operations, it causes the shifting of two 16-bit register: A_0, the most significant 16 bits; and A1, the least significant 16 bits. The value of the 7 bit combined S and M fields is interpreted per Table A-12. The shift count uses A6. One microinstruction delay is required before the microprogram can access the shifted quantity at the shift matrix output. When using S=7, the Feed, Partial Product, or Monitor Clock Register must be selected as specified in Table A-13.

Table A-11. FII, S and M-Designators for Microinstruction F=15

FII		S		M	
11 10 9 8	FUNCTION	7 6 5 4	FUNCTION	3 2 1 0	FUNCTION
0 0 0 0	INCREMENT	not used		0 0 0 1 1 0 0 0	Decrement cycle counter by 1 Increment SGR
0 0 0 0	CLR I/O RETURN	not used		not used	
0 0 0 0	NOT USED				
0 0 0 0	NOT USED				
0 0 1 1	Select Page Enable	not used		not used	
0 1 0 0	INCREMENT	not used		0 0 0 1 1 0 0 0	Decrement cycle counter by 1 Increment SGR
0 1 0 0	MEMORY	0 0 0 X 0 0 1 X 0 1 0 X 0 1 1 X 1 0 0 X 1 0 1 X 1 1 0 X 1 1 1 X	Read Write Read odd Write odd Read Split Write 0's Read Byte Write Byte	not used	
0 1 0 1	CONDITION CODE CONTROL	X X X 0 X X X 1 X X 0 X X X 1 X X 0 X X X 1 X X 0 X X X 1 X X X	Clr 8 and 9 Set 8 and 9 on Condition Clr 10 and 11 Set 10 and 11 on Condition Compare masked Compare Double Precision Single Precision	0 X X X 1 X X X	No Shift Overflow Check Shift Overflow Check

Table A-11. FII, S and M-Designators for Microinstruction F=15 (Cont)

FII		S		M	
11 10 9 8	FUNCTION	7 6 5 4	FUNCTION	3 2 1 0	FUNCTION
0 1 1 0	NOT USED				
0 1 1 1	SGR CONTROL	0 0 X X 0 1 X X 1 0 X X 1 1 X X	A + 1 SGR A → SGR K → SGR M + 1 → SGR	not used	
1 0 0 0	SHIFT CONTROL	See Tables A12 & A13			
1 0 0 1	NOT USED				
1 0 1 0	NOT USED				
1 0 1 1	NOT USED				
1 1 0 0	MEMORY	0 0 0 X 0 0 1 X 0 1 0 X 0 1 1 X 1 0 0 X 1 0 1 X 1 1 0 X	Read Write Read odd Write odd Read Split Write 0's Read Byte	not used	
1 1 0 1	I/O CONTROL	X X X 1 X X 1 X X 1 X X	Set Chain Condition Channel Control Initiate Transfer	X X X 1 X X 1 X X 1 X X 1 X X X	Enable Out Data Sel/Clr Status Clr Interrupt Clr Chain/Interrupt Req. Halt/Interrupt
1 1 1 0	CP CONTROL	 X X X 1 X X 1 X X 1 X X 1 X X X	 Search for Sync Load Discrete Clear RUN Reset I/O, Light PROG FAULT	1 X X X 0 0 0 0 X 0 0 1 X 0 1 0 X 0 1 1 X 1 0 0 X 1 0 1 X 1 1 0 X 1 1 1	Enable power interrupt No Operation Disable RTC interrupt Enable RTC interrupt Disable monitor clock Enable monitor clock Enable RTC Count Disable RTC Count Clear class I + II interrupts
1 1 1 1	NOT USED				

Table A-12. Shift Control Commands (F=15, FII=10)

COMBINED S AND M DESIGNATORS (7 BITS)	FUNCTION	SHIFT COUNT INTERPRETATION
0000000	Double precision-Circular left shift A_1	Shift count=A6 (4 bits)
0000001	Double precision-Circular left shift A_0	Shift count=A6 (4 bits)
0000010	Double precision-Arithmetic left shift A_1	Shift count=A6 (4 bits)
0000011	Double precision-arithmetic left shift A_0	Shift count=A6 (4 bits)
0000100	Single precision-Circular left shift A_0	Shift count=A6 (4 bits)
0000101	Single precision-Arithmetic left shift A_0	Shift count=A6 (4 bits)
0000110	Extract left shifted bits of A_1	Shift count-A6 (4 bits)
0000111	Extract left shifted bits of A_0 double or single precision	Shift count=A6 (4 bits)
0001000	Double precision-Logical right shift A_1	Shift count=A6 (4 bits)
0001001	Double precision or single precision-Logical right shift A_0	Shift count=A6 (4 bits)
0001010	Double precision-Arithmetic right shift A_1	Shift count=A6 (4 bits)
0001011	Double precision or single precision-Arithmetic right shift A_0	Shift count=A6 (4 bits)
0010000	Double precision-Logical right shift A_1	Shift count=A6 (4 bits) - 1 count
0010001	Double precision or single precision-Logical right shift A_0	Shift count=A6 (4 bits) - 1 count
0010010	Double precision-Arithmetic right shift A_1	Shift count=A6 (4 bits) - 1 count
0010011	Double precision or single precision-Arithmetic right shift A_0	Shift count=A6 (4 bits) - 1 count
0011000	A_0 to shift matrix output	Shift count=0
0011001	Al to shift matrix output	Shift count=0
0100XXX	See 0000XXX	Shift count=A6 (6 bits)

Table A-12. Shift Control Commands (F=15, FII=10)

COMBINED S AND M DESIGNATORS (7 BITS)	FUNCTION	SHIFT COUNT INTERPRETATION
0110XXX	See 0010XXX	Shift count=A6 (6 bits) - 1 count
0111000	Cordic scale initialize	A6=17 for trigonometric function A6=13 for hyperbolic function
1010100	Cordic algorithm	A6-17 for trigonometric function A6=16 for hyperbolic function
1011100	Floating point-normalize A_1 to 2^{23}	A6=negative, shift right A6=positive, shift left A6=0, no shift
1001101	Floating point-normalize A_0 to 2^{23}	A6=negative, shift right A6=positive, shift left A6=0, no shift
1101011	Hexidecimal floating point positioning of A_0	Shift count=A6 (4 bits) x 4
1110010	Hexidecimal floating point positioning with round of A_1	Shift count=A6 (4 bits x 4
1110011	Hexidecimal floating point positioning with round of A_0	Shift count=A6 (4 bits) - 1 count
1111100	Hexidecimal floating point-normalize A_1 to 2^{23}	A6=negative, shift right A6=positive, shift left A6=0, no shift
1111101	Hexidecimal floating point-normalize A_0 to 2^{23}	A6=negative, shift right A6=positive, shift left A6=0, no shift

Table A-13. Feed/Partial Product/Monitor Clock Selection for $S_1 = 7$

COMBINED S AND M DESIGNATORS F = 15, FII = 10	REGISTER SELECTION
X X X X X 0 0 X	Feed Register
X X X X X 0 1 X	Partial Product Register
X X X X X 1 0 X	Monitor Clock Register

F = 16 MICRO REPEAT

1110	F11	K

This instruction establishes a repeat mode wherein the next instruction or series of instructions will be repeated as specified in the following paragraphs to accomplish the function specified. K determines the cycle count. The instruction repeat count is preset to accomplish the function specified. K determines the cycle count. The instruction repeat count is preset. The MPC transfer (μP) to μP HOLD before the repeat sequence. The contents of μP HOLD are then transferred back to μP for each repeat cycle.

Multiply single (F = 16, FII = 0000). This instruction multiplies the single length multiplicand in S1 by the multiplier in R2 and stores the most significant half (MSH) of the product in D1 and the least significant half (LSH) of the product in R1. This instruction is executed when the instruction following it is as follows:

	F	D	S	M
Add	04	D1	S1	00

The register specified by D1 must be A2 or A3 and must be cleared before executing this routine. The value of K must be one less than the number of bits of the multiplier.

Divide single (F = 16, FII = 0001). This instruction requires both the divisor and dividend to be positive. It divides the double length dividend (the MSH in register D1, the LSH in R1) by the divisor in S1. The quotient is stored in R2 and the remainder in D1. This instruction is executed when the instructions following it are as follows:

	F	D	S	M
Sub	05	D1	S1	00
Branch Neg	14	00	X	X
Add	04	D1	S1	03

The register specified by D1 must be A2 or A3. The quotient is 2's complement fractional; it will be an integer if the dividend is shifted left 1 bit before execution of the divide routine. The value of K must be one less than the number of bits of the divisor.

Multiply double (F = 16, FII = 0010). This instruction multiplies the double length multiplicand (the MSH in A8 or A6 and the LSH in A5 or A7) by the double length multiplier (the MSH in R1 and the LSH in R2). The 32 bits in the MSH of the product are in R1 and R2 with R1 containing the upper 16 bits. The 32 bits in the LSH of the product are in A2 and A3 with A2 containing the upper 16 bits. This instruction is executed when the instructions following it are as follows:

	F	D	S	M
Add	04	13	S1	10
Add	04	12	S2	01
Add Constant	10	13	0	00

The A2 and A3 registers must be cleared before executing these instructions. The value of K must be one less than the number of bits of the multiplier.

Divide double (F = 16, FII = 0011). This instruction requires both the divisor and the dividend to be positive. It divides the 64 bit dividend (the upper 16 bits of the MSH in A3 and the lower 16 bits of the MSH in A2, and the upper 16 bits of the LSH in R1 and the lower 16 bits of the LSH in R2) by the double length divisor (the MSH in A5 or A7 and the LSH in A4 or A6). The quotient is stored in R1 and R2 and the remainder stored in A2 or A3. This instruction is executed when the instructions following it are as follows:

	F	D	S	M
Sub	05	13	S1	10
Sub	05	12	S2	11
Branch Neg	14	00	X	X
Add	04	13	S1	13
Add	04	12	S2	D1

The quotient is 2's complement fractional; it will be n integer if the dividend is shifted left 1 bit before executing this instruction. The branch routine is for end correction if required. The value of K must be one less than the number of bits of the divisor.

Repeat rotate (F = 16, FII = 0100). This instruction repeats the next 3 instructions K+1 times. It is executed when the instructions following it are as follows:

	F	D	S	M
Add	02	12	11	X011

	F	D	S	M
Add	04	11	06	X011 X110
Add	04	10	06	0011 0110

Repeat vector (F = 16, FII = 0101. This instruction repeats the next 3 instructions K+1 times. It is executed when the instructions following it are as follows:

	F	D	S	M
Add	02	12	11	03
Add	04	11	06	13
Add	04	10	06	03

Repeat scale (F = 16, FII = 0110). This instruction repeats the next 2 instructions K+1 times. It is executed when the instructions following it are as follows:

		F	D	S	M
either:	Sub	05	10	06	00
	Sub	05	11	06	00
or:	Add	04	10	06	03
	Add	04	11	06	03

Square root repeat (F = 16, FII = 0111). This instruction repeats the next 2 instructions K+1 times. It is executed when the instructions following it are as follows:

	F	D	S	M
Add	04	12	06	13
Add	04	12	00	03

Repeat normal (F = 16, FII = 1000). This instruction executes the K+1 instructions following it n+1 times. K+1 shall be equal to the value in bits 3-0 of K, plus one. n+1 shall be equal to the contents of the cycle count register plus one (which must be loaded by a previous instruction).

Repeat normal, suppress last cycle (F =b16, FII = 1001). This instruction executes the K+1 instructions following it n times. K+1 shall be specified by the value in bits 3-0 of K, plus one. n shall be equal to the contents of the cycle count register (which must be loaded by a previous instruction).

F = 17 EMULATE

1111	D1	S0	M

This instruction is freeform and is interpreted as shown in Table A-14.

TABLE A-14. S and M-Designators for F=17

S		M	
7 6 5 4	FUNCTION	3 2 1 0	FUNCTION
0 X X X	Load SGR	0 0 0 0	I/O Breakpoint
1 X X X	Inhibit Load SGR	0 0 0 1	Not Assigned
		0 0 1 0	Not Assigned
		0 0 1 1	Operand Reference (Destination → MAR)
		0 1 0 0	Not Assigned
		0 1 0 1	Normal Branch 1. If bit 11 of ECW set, P → MAR. If bit 11 of ECW clear, GR → MAR.
		0 1 1 0	Not Assigned
		0 1 1 1	Normal branch 2. If bit 12 of ECW is clear, P → MAR and force read. If bit 12 of ECW is set, P → MAR, and initiate the operation selected by bits 15-13 of the ECW.
		1 0 0 0	Restart overlap. P → MAR, no advance P
		1 0 0 1	Branch 1 special. Dest → MAR, Inhibit I/O, and force read.
		1 0 1 0	Not Assigned
		1 0 1 1	Not Assigned
		1 1 0 0	Normal Start. Branch, P → MAR, P + 1 → P.
		1 1 0 1	Branch 1 special. Dest → MAR, Inhibit I/O, and force read.
		1 1 1 0	Normal start jump. Branch, Dest → MAR, P + 1 → P.
		1 1 1 1	Not Assigned

APPENDIX B
REPERTOIRE OF MACRO INSTRUCTIONS

Instructions defined in this list include the basic instruction set and those required for optional features in the computer. Users of computer configurations that do not include certain optional instructions must place those respective instructions in the "Not assigned" category and assemble programs accordingly.

The instructions are described in the following format:

(Operation Code)

(ULTRA symbol) (instruction format) (instruction name)

(Detailed descriptive text that includes special designator interpretations when applicable)

When the a- or m-designator is used as a sub-function code, the information is presented in table form.

Symbols Used In Instructions

Symbol	Description
a	The a-designator from instruction words.
d	The deviation value in a local jump instruction.
R_a	The register designated by a.
m	The m-designator from instruction words.
R_m	The register designated by m.
Y	The operand or memory address generated in the execution of an instruction.
y	The contents of the second word of an RK or RX instruction.
P	The Program Address register.
μP	The Micro Program Address Register
( )	The contents of the location specified within the parenthesis.

Operation Code 00

\- RR Format - DIAGNOSTIC RETURN
If the DIAGNOSTIC JUMP switch is in the up position, transfer the contents of General Register 17_8 to μP.

\- RI Format - Not assigned

- RK Format - Not assigned

BL RX Format - BYTE LOAD
Load the selected byte from address Y in bits 7 through 0 of R_a, clearing bits 15 through 8, and setting the Condition Code.

Address Y = y + (R_m) right shifted one place; bit 0 of R_m is the byte identifier.

Operation Code 01

LR RR Format - LOAD
Load (R_m) in R_a, and set the Condition Code (table XIII).

LI RI Format Type 2 - LOAD
Load the contents of memory address Y in R_a, and set the Condition Code (table XIII).

LK RK Format - LOAD
Load the Operand Y in R_a, and set the Condition Code (table XIII).

L RX Format - LOAD
Load the contents of memory address Y in R_a, and set the Condition Code (table XIII).

Operation Code 02

(1) RR Format - UNARY ARITHMETIC
Perform the operation specified for the m-value in Table I and then set the Condition Code according to the quantity resulting in R_a (table XIII).

LDI RI Format, Type 2 - LOAD DOUBLE
Load the contents of addresses Y and Y+1 in R_a and R_{a+1} respectively, and set the Condition Code (table XIII).

- RK Format - Not assigned

LD RX Format - LOAD DOUBLE
This instruction shall load the contents of memory address Y and Y + 1 in R_a and R_{a+1} respectively, and set the Condition Code (table XIII).

Operation Code 03

(2) RR Format - UNARY-CONTROL
Perform the operation specified in Table II for the m-value.

- RI Format - Not assigned

- RK Format - Not assigned

---

(1) See Table I
(2) See Table II

TABLE I. UNARY-ARITHMETIC INSTRUCTION m-VALUES

ULTRA Symbol	m Value	Operation	Description

PR	0	MAKE POSITIVE	If (R_a) are negative, perform the two's complement of (R_a) and store the result in R_a. When the maximum negative number* is complemented, set the overflow designator (table XIII).
			
			If (R_a) are positive, do not change (R_a).

NR	1	MAKE NEGATIVE	If (R_a) are positive and not zero, perform the two's complement of (R_a) and store the result in R_a.
			
			If (R_a) are negative or zero, do not change (R_a).

RR	2	ROUND R_a	If (R_a) are positive, add bit 15 of R_{a+1} to (R_a) and store the result in R_a.
			
			If (R_a) are negative, subtract the complement of bit 15 of R_{a+1} from (R_a) and store the result in R_a

--	3	-----	Not assigned
TCR	4	TWO'S COMPLEMENT, SINGLE	Perform the two's complement of (R_a) and store the result in R_a.
TCDR	5	TWO'S COMPLEMENT, DOUBLE	Perform the two's complement of double length (R_a, R_{a+1}) and store the result in R_a, R_{a+1}. When the maximum negative number* is complemented, set the overflow designator (table XIII).
OCR	6	ONE'S COMPLEMENT, SINGLE	Perform the one's complement of (R_a) and store the result in R_a.
--	7	-----	Not assigned
TROR	10	INCREASE R_a BY 1	Increase (R_a) by 1 and store the result in R_a.
DROR	11	DECREASE R_a BY 1	Decrease (R_a) by 1 and store the result in R_a.
TRTR	12	INCREASE R_a BY 2	Increase (R_a) by 2 and store the result in R_a.
DRTR	13	DECREASE R_a BY 2	Decrease (R_a) by 2 and store the result in R_a.
--	14-17	-----	Not assigned

*(1,000,000,000,000,000)

TABLE II. UNARY-CONTROL INSTRUCTION m-VALUES

ULTRA Symbol	m Value	Operation	Description
ER	1	STORE STATUS REGISTER #1	Store the contents of Status Register #1 in R_a.
SSOR	2	STORE STATUS REGISTER #2	Store the contents of Status Register #2 in R_a.
SCR	3	STORE RTC LOWER	Store the contents of the Real Time Clock Lower Register in R_a.
LPR	4	LOAD P	Load (R_a) in P.
LSOR	5	LOAD STATUS REGISTER #1	Load (R_a) in Status Register #1.
LSTR	6	LOAD STATUS REGISTER #2	Load (R_a) in Status Register #2.
LCR	7	LOAD RTC LOWER	Load (R_a) in the Real Time Clock Lower Register.
ECR	10	ENABLE RTC	Enable the Real Time Clock Register to increase by one for each cycle of the clock sources. Generate a RTC Interrupt when the contents of the Real Time Clock Lower Register changes from all ones to all zeros.
DCR	11	DISABLE RTC	Disable the Real Time Clock Register from advancing. The RTC Oscillator continues to operate.
---	12	LOAD AND ENABLE CLOCK MONITOR	Load (R_a) in Monitor Clock Register and enable register to decrement by one for each cycle of the clock source. Generate the Monitor Clock interrupt when the contents of the Monitor Clock Register equals zero.
---	13	DISABLE MONITOR CLOCK	Disable Monitor Clock and Monitor Clock Interrupt.
---	14	LOAD RTC DOUBLE	Load (R_a, $R_a + 1$) in the Real Time Clock Register and enable the register to increase by one for each cycle of the clock source. RTC Interrupt enable/disable condition is not affected.
---	15	STORE RTC DOUBLE	Store the contents of the Real Time Clock into R_a and $R_a + 1$.

TABLE II. UNARY-CONTROL INSTRUCTIONS m-VALUES (CONT)

ULTRA Symbol	m Value	Operation	Description
---	16	ENABLE RTC INTERRUPT	Enable generation of RTC interrupt when the contents of the Real Time Clock Lower Register changes from all ones to all zeros.
---	17	DISABLE RTC INTER-RUPT	Disable generation of the RTC Interrupt.

LM — RX Format - LOAD MULTIPLE
Load the contents of sequential memory addresses beginning at Y, in sequential registers beginning at R_a and ending at R_m. If a is greater than m, load registers in the order R_a, R_{a+1},..., R_{17}, R_0...R_m. Address Y is equal to y.

Operation Code 04

(3) — RR Format - UNARY-SHIFT (Optional Feature)
Perform the operation specified in Table III for the m-value.

\- — RI Format - Not assigned

\- — RK Format - Not assigned

BLX — RX Format - BYTE LOAD AND INDEX BY 1
Load the selected byte from memory address Y in bits 7 through 0 of R_a clearing bits 8 through 15 and setting the Condition Code (table XIII); and then increase (R_m) by 1.

Address Y = y + (R_m) right shifted one place; bit 0 of R_m is the byte identifier.

Operation Code 05

SB — RR Format - SET BIT
Set the bit in R_a specified by the m-value.

LXI — RI Format, Type 2 - LOAD AND INDEX BY 1
Load the contents of memory address Y in R_a, set the Condition Code (table XIII), and then increase (R_m) by 1.

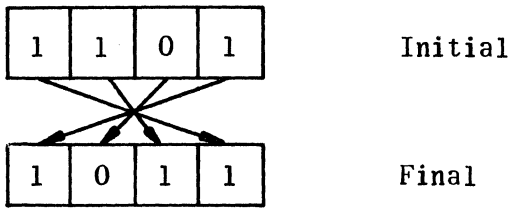
\- — RK Format - Not assigned

LX — RX Format - LOAD AND INDEX BY 1
Load the contents of memory address Y in R_a, set the Condition Code (table XIII), and then increase (R_m) by 1.

---

(3) See Table III

TABLE III. UNARY-SHIFT INSTRUCTION m-VALUE

ULTRA Symbol	m Value	Operation	Description
---	0	----	Not assigned
RVR	1	REVERSE REGISTER	Change (R_a) to the reverse order according to the 4-bit example: 
CNT	2	COUNT ONES	Count the number of one bits in (R_a), and store the count in R_{a+1}.
SFR	3	SCALE FACTOR	Shift the double length (R_a, R_{a+1}) to the left with zeros extended to fill, until bits 15 and 14 of R_a are not equal and store the shift count in R_{a+2}.
---	4-17	-----	Not assigned

Operation Code 06

ZBR — RR Format - ZERO BIT (Clear Bit)
Clear the bit in R_a specified by the m-value.

LDXI — RI Format, Type 2 - LOAD DOUBLE AND INDEX BY 2
Load the contents of memory address Y and Y + 1 in R_a and R_{a+1} respectively, set the Condition Code (table XIII), and then increase (R_m) by 2.

\- — RK Format - Not assigned

LDX — RX Format - LOAD DOUBLE AND INDEX BY 2
Load the contents of memory address Y and Y + 1 in R_a and R_{a+1} respectively, set the Condition Code (table XIII), and then increase (R_m) by 2.

Operation Code 07

CBR — RR Format - COMPARE BIT (Test Bit)
Test the bit in R_a specified by the m-value and set the Condition Code (Table XIII) if the bit is set.

LPI — RI Format, Type 2 - LOAD PSW (Program Status Word)
Load the contents of memory addresses Y, Y + 1, and Y + 2 in Program Address Register, Status Register #1, and Status Register #2, respectively. Y = (R_m).

\- — RK Format - Not assigned

LP — RX Format - LOAD PSW (Program Status Word)
Load the contents of memory addresses Y, Y + 1, and Y + 2 in the Program Address Register, Status Register #1, and Status Register #2, respectively. Y = (R_m) + y.

Operation Code 10

LRSR — RR Format - LOGICAL RIGHT SINGLE SHIFT
Shift (R_a) to the right n-places with zeros extended to fill. n is the value in bits 5-0 of R_m.

\- — RI Format - Not assigned

LRS — RK Format - LOGICAL RIGHT SINGLE SHIFT
Shift (R_a) to the right n places with zeros extended to fill. n is the value in bits 5-0 of operand Y.

BS — RX Format - BYTE STORE
Store bits 7-0 of (R_a) in the selected byte of memory address Y.
Y = y + (R_m) right shifted one place; bit 0 of (R_m) is byte identifier.

Operation Code 11

ARSR — RR Format - ALGEBRAIC RIGHT SINGLE SHIFT
Shift (R_a) to the right n places with sign extended to fill. n is the value in bits 5-0 of R_m.

SI — RI Format, Type 2 - STORE
Store (R_a) at memory address Y.

ARS — Format RK - ALGEBRAIC RIGHT SINGLE SHIFT
Shift (R_a) to the right n places with sign extended to fill. n is the value in bits 5-0 of operand Y.

S — RX Format - STORE
Store (R_a) at memory address Y.

Operation Code 12

LRDR — RR Format - LOGICAL RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the right n-places with zeros extended to fill. n is the value in bits 5-0 of R_m.

SDI — RI Format, Type 2 - STORE DOUBLE
Store (R_a) and (R_{a+1}) at memory addresses Y and Y + 1 respectively.

LRD — RK Format - LOGICAL RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the right n places with zeros extended to fill. n is the value in bits 5-0 of operand Y.

SD — RX Format - STORE DOUBLE
Store (R_a) and (R_{a+1}) at memory addresses Y and Y + 1 respectively.

Operation Code 13

ARDR — RR Format - ALGEBRAIC RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the right n places with the sign extended to fill. n is the value in bits 5-0 of R_m.

\- — RI Format - Not assigned

ARD — RK Format - ALGEBRAIC RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the right n places with the R_a sign extended to fill. n is the value in bits 0-5 of operand Y.

SM — RX Format - STORE MULTIPLE
Store in sequential memory addresses beginning at Y, the contents of sequential registers beginning at R_a and ending at R_m. If a is greater than m store registers in the order R_a, R_{a+1},..., R_{17}, R_0,..., R_m.
Y equals y.

Operation Code 14

ALSR — RR Format - ALGEBRAIC LEFT SINGLE SHIFT
Shift (R_a) to the left n places with zeros extended to fill. n is the value in bits 5-0 of R_m.

\- — RI Format - Not assigned

ALS — RK Format - ALGEBRAIC LEFT SINGLE SHIFT
Shift (R_a) to the left n places with zeros extended to fill. n is the value in bits 5-0 of operand Y.

BSX — RX Format - BYTE STORE AND INDEX BY 1
Store bits 7-0 of R_a in the selected byte at memory address Y; and then increase (R_m) by 1. Y = y + (R_m) right shifted one place; bit 0 of (R_m) is byte identifier.

Operation Code 15

CLSR — RR Format - CIRCULAR LEFT SINGLE SHIFT
Shift (R_a) circularly to the left n places. n is the value in bits 5-0 of R_m.

SXI — RI Format, Type 2 - STORE AND INDEX BY 1.
Store (R_a) at memory address Y; and then increase (R_m) by 1. Y = (R_m).

CLS — RK Format - CIRCULAR LEFT SINGLE SHIFT
Shift (R_a) circularly to the left n places. n is the value of bits 5-0 of operand Y.

SX — RX Format - STORE AND INDEX BY 1
Store (R_a) at memory address Y; and then increase (R_m) by 1.

Operation Code 16

ALDR — RR Format - ALGEBRAIC LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the left n places with zeros extended to fill. n is the value in bits 5-0 of R_m.

SDXI — RI Format, Type 2 - STORE DOUBLE AND INDEX BY 2
Store (R_a) and (R_{a+1}) at memory addresses Y and Y + 1, respectively; then increase (R_m) by 2.

ALD — RK Format - ALGEBRAIC LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) to the left n places with zeros extended to fill. n is the value in bits 5-0 of operand Y.

SDX — RX Format - STORE DOUBLE AND INDEX BY 2
Store (R_a) and (R_{a+1}) at memory addresses Y and Y + 1, respectively; and then increase (R_m) by 2.

Operation Code 17

CLDR — RR Format - CIRCULAR LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) circularly to the left n places. n is the value in bits 5-0 of R_m.

SZI — RI Format, Type 2 - STORE ZEROS
Clear memory address Y. Y = (R_m)

CLD — RK Format - CIRCULAR LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) circularly to the left n places. n is the value in bits 5-0 of Y.

SZ — RX Format - STORE ZEROS
Clear memory address Y.

Operation Code 20

SUR — RR Format - SUBTRACT
Subtract (R_m) from (R_a) and store the result in R_a; then set the Condition Code (table XIII).

SUI — RI Format, Type 2 - SUBTRACT
Subtract the contents of memory address Y from (R_a) and store the result in R_a; then set the Condition Code (table XIII). Y = (R_m).

SUK — RK Format - SUBTRACT
Subtract operand Y from (R_a) and store the result in R_a; then set the Condition Code (table XIII).

SU — RX Format - SUBTRACT
Subtract the contents of memory address Y from (R_a) and store the result in R_a; then set the Condition Code (table XIII).

Operation Code 21

SUDR — RR Format - SUBTRACT DOUBLE
Subtract the double length (R_m, R_{m+1}) from the double length (R_a, R_{a+1}) and store the result in R_a and R_{a+1}; then set the Condition Code (table XIII).

SUDI — RI Format, Type 2 - SUBTRACT DOUBLE
Subtract the double length contents of memory addresses Y, Y + 1 from the double length (R_a, R_{a+1}) and store the result in R_a and R_{a+1}; then set the Condition Code (table XIII).

\- — RK Format - Not assigned

SUD — RX Format - SUBTRACT DOUBLE
Subtract the double length contents of memory addresses Y, Y + 1 from the double length (R_a, R_{a+1}) and store the result in R_a and R_{a+1}; then set the Condition Code (table XIII).

Operation Code 22

AR — RR Format - ADD
Add (R_m) to (R_a) and store the result in R_a; then set the Condition Code (table XIII).

AI — RI Format, Type 2 - ADD
Add the contents of memory address Y to (R_a) and store the result in R_a; then set the Condition Code (table XIII).

AK — RK Format - ADD
Add operand Y to (R_a) and sto5re th result in R_a; and then set the Condition Code (table XIII).

A — RX Format - ADD
Add the contents of memory address Y to (R_a) and store the result in R_a; and then set the Condition Code (table XIII).

Operation Code 23

ADR — RR Format - ADD DOUBLE
Add the double length (R_m, R_{m+1}) to the double length (R_a, R_{a+1}) and store the result in R_a and R_{a+1}; then set the Condition Code (table XIII).

ADI — RI Format, Type 2 - ADD DOUBLE
Add the double length contents of memory addresses Y, Y + 1 to the double length (R_a, R_{a+1}) and store the result in R_a and R_{a+1}; then set the Condition Code (table XIII).

\- — RK Format - Not assigned

AD — RX Format - ADD DOUBLE
Add the double length contents of memory address Y, Y + 1 to the double length (R_a, R_{a+1}) and store the result in R_a and Ra+1; then set the Condition Code (table XIII).

Operation Code 24

CR — RR Format - COMPARE
Arithmetically compare (R_a) to (R_m), and set the Condition Code (table XIII).

CI — RI Format, Type 2 - COMPARE
Arithmetically compare (R_a) to the contents of memory address Y, and set the Condition Code (Table XIII).

CK — RK Format - COMPARE
Arithmetically compare (R_a) to operand Y, and set the Condition Code (table XIII).

C — RX Format - COMPARE
Arithmetically compare (R_a) to the contents of memory address Y, and set the Condition Code (table XIII).

Operation Code 25

CDR — RR Format - COMPARE DOUBLE
Arithmetically compare the double length (R_a, R_{a+1}) to the double length (R_m, R_{m+1}) and set the Condition Code (table XIII).

CDI — RI Format, Type 2 - COMPARE DOUBLE
Arithmetically compare the double length (R_a, R_{a+1}) to the double length contents of memory addresses Y, Y + 1 and set the Condition Code (table XIII).

\- — RK Format - Not assigned

CD — RX Format - COMPARE DOUBLE
Arithmetically compare the double length (R_a, R_{a+1}) to the double length contents of memory address Y, Y + 1 and set the Condition Code (table XIII).

Operation Code 26

MR — RR Format - MULTIPLY
Multiply (R_m) by (R_{a+1}) and store the double length result in R_a, R_{a+1}; and then set the Condition Code (table XIII).

MI — RI Format, Type 2 - MULTIPLY
Multiply the contents of memory address Y by (R_{a+1}) and store the double length result in R_a, R_{a+1}; and then set the Condition Code (table XIII).

MK — RK Format - MULTIPLY
Multiply operand Y by (R_{a+1}) and store the double length result in R_a, R_{a+1}; and then set the Condition Code (table XIII).

M — RK Format - MULTIPLY
Multiply the contents of memory address Y by (R_{a+1}) and store the double length result in R_a, R_{a+1}; then set the Condition Code (table XIII).

Operation Code 27

DR — RR Format - DIVIDE
Divide the double length (R_a, R_{a+1}) by (R_m), store he quotient in R_{a+1} and the remainder in R_a; then set the Condition Code (table XIII).

DI — RI Format, Type 2 - DIVIDE
Divide the double length (R_a, R_{a+1}) by the contents of memory address Y; store the quotient in R_{a+1} and the remainder in R_a; then set the Condition Code (table XIII).

DK — RK Format - DIVIDE
Divide the double length (R_a, R_{a+1}) by operand Y, store the quotient in R_{a+1} and the remainder in R_a; then set the Condition Code (table XIII).

D — RX Format - DIVIDE
Divide the double length (R_a, R_{a+1}) by the contents of memory address Y, store the quotient in R_{a+1} and the remainder in R_a; then set the Condition Code (table XIII).

Note: For all divides, the remainder has the same sign as the dividend and is interpreted as follows:

Remainder Sign	Divisor Sign	Remainder
+	+	Less than the divisor.
+	-	Less than the absolute value of the two's complement of the divisor.
-	+	Less than the divisor.
-	-	The absolute value of the remainder is less than the absolute value of the divisor.

Operation Code 30

ANDR — RR Format - AND
Perform the logical AND of (R_a) and (R_m), and store the result in R_a (clear bits in R_a corresponding to zeros in R_m). Set Condition Code (table XIII).

ANDI — RI Format, Type 2 - AND
Form the logical AND of (R_a) and the contents of memory address Y, and store the result in R_a (clear bits in R_a corresponding to zeros in the contents of address Y). Set Condition Code (table XIII).

ANDK — RK Format - AND
Form the logical AND of (R_a) and operand Y, and store the result in R_a (clear bits in R_a corresponding to zeros in operand Y). Set Condition Code (table XIII).

AND — RX Format - AND
Form the logical AND of (R_a) and the contents of memory address Y, and store the result in R_a (clear bits in R_a corresponding to zeros in the contents of address Y). Set Condition Code (table XIII).

Operation Code 31

ORR — RR Format - OR
Form the logical OR of (R_a) and (R_m), and store the result in R_a. Set Condition Code (table XIII).

ORI — RI Format, Type 2 - OR
Form the logical OR of (R_a) and the contents of memory address Y, and store the result in R_a. Set Condition Code (table XIII).

ORK — RK Format - OR
Form the logical OR of (R_a) and operand Y, and store the result in R_a. Set Condition Code (table XIII).

OR — RX Format - OR
Form the logical OR of (R_a) and the contents of memory address Y, and store the result in R_a. Set Condition Code (table XIII).

Operation Code 32

XORR — RR Format - EXCLUSIVE OR
Form the exclusive OR of (R_a) and (R_m), and store the result in R_a. Set Condition Code (table XIII).

XORI — RI Format, Type 2 - EXCLUSIVE OR
Form the exclusive OR of (R_a) and the contents of memory address Y, and store the result in R_a. Set Condition Code (table XIII).

XORK — RK Format - EXCLUSIVE OR
Form the exclusive OR of (R_a) and operand Y, and store the result in R_a. Set Condition Code (table XIII).

XOR — RX Format - EXCLUSIVE OR
Form the exclusive OR of (R_a) and the contents of memory address Y, and store the result in R_a. Set Condition Code (table XIII).

Operation Code 33

MSR — RR Format - MASKED SUBSTITUTE
For each bit set in (R_{a+1}), transfer the corresponding bit of (R_m) to the corresponding bit in R_a and leave the remaining bits in R_a unchanged. Set Condition Code (table XIII).

MSI — RI Format, Type 2 - MASKED SUBSTITUTE
For each bit set in (R_{a+1}), transfer the corresponding bit of the contents of memory address Y to the corresponding bit in R_a and leave the remaining bits in R_a unchanged. Set Condition Code (table XIII).

MSK — RK Format - MASKED SUBSTITUTE
For each bit set in (R_{a+1}), transfer the corresponding bit of operand Y to the corresponding bit in R_a and leave the remaining bits in R_a unchanged. Set Condition Code (table XIII).

MS — RX Format - MASKED SUBSTITUTE
For each bit set in (R_{a+1}), transfer the corresponding bit of the contents of memory address Y to the corresponding bit in R_a and leave the remaining bits in R_a unchanged. Set Condition Code (table XIII).

Operation Code 34

CMR — RR Format - COMPARE MASKED
Compare (bit by bit) the result of the logical AND of (R_a) and (R_{a+1}) to the result of the logical AND of (R_m) and (R_{a+1}) and set the Condition Code (table XIII).

CMI — RI Format, Type 2 - COMPARE MASKED
Compare (bit by bit) the logical AND of (R_a) and (R_{a+1}) to the logical AND of contents of memory address Y and (R_{a+1}) and set the Condition Code (table XIII).

CMK — RK Format - COMPARE MASKED
Compare (bit by bit) the logical AND of (R_a) and (R_{a+1}) to the logical AND of operand Y and (R_{a+1}) and set the Condition Code (table XIII).

CM — RX Format - COMPARE MASKED
Compare (bit by bit) the logical AND of (R_a) and (R_{a+1}) to the logical AND of contents of memory address Y and (R_{a+1}) and set the Condition Code (table XIII).

Operation Code 35

IOCR — RR Format - I/O COMMAND
Execute the I/O command instruction from main memory address 000140 and clear bits 14 and 15 at address 000140.

BFI — RI Format, Type 2 - BIASED FETCH
Transfer the sign (bit 15) of the contents of memory address Y to the Condition Code and then set the two most significant bits at that memory location, leaving the remaining bits unchanged.

REX — RK Format - EXECUTE REMOTE
Execute the instruction stored at memory address Y; do not change (P) when reading this instruction. Then continue with the next sequential instruction.

BF — RX Format - BIASED FETCH
Transfer the sign (bit 15) of the contents of memory address Y to Condition Code bits 8 and 9 and then set the two most significant bits at that memory location, leaving the remaining bits unchanged.

Operation Code 36 - Not assigned

Operation Code 37 - Not assigned

Operation Code 40

(4) RR Format - CONDITIONAL JUMP
Test for the condition specified in table IV for the a-value and perform one of the following:

(1) If the specified condition is met, load (R_m) in P (jump to the instruction located at the address specified in R_m). If a specified Stop, or a Stop Key condition is met, disable RTC and stop the computer. On restart, load (R_m) in P (jump to the instruction at the address specified by (R_m)).

(2) If the specified jump condition is not met, execute the next instruction. If the specified stop condition is not met, execute the jump without stopping.

LJ — RI Format, Type 1 - LOCAL JUMP
Load Y in P (jump to the instruction located at memory address Y).
$Y = (P)_i \pm d$.

(4) RK Format - CONDITIONAL JUMP
Test for the condition specified in Table IV for the a-value and perform one of the following:

(1) If the specified condition is met, load Y in P (jump to the instruction located at the address specified by operand Y). If a specified Stop, or a Stop Key condition is met, disable RTC and stop the computer. On restart, load Y in P (jump to the instruction located at the address specified by operand Y).

(2) If the specified jump condition is not met, execute the next instruction. If the specified stop condition is not met, execute the jump without stopping.

---

(4) See Table IV

TABLE IV. CONDITIONS FOR a-VALUE IN JUMP INSTRUCTIONS

ULTRA Symbol for Format			a-Value	Jump Condition	
				Condition code for Arithmetic Operation Indicates	Condition code for Compare Operation Indicates
RR	RK	RX			
JER	JE	JE	0	Zero (bit 8 = 0)	Equal (bit 8 = 0)
JNER	JNE	JGE	1	Not Zero (bit 8 = 1)	Not Equal (bit 8 = 1)
JGER	JGE	JGE	2	Positive (bit 9 = 0)	Greater Than or Equal (bit 9 = 0)
JLSR	JLS	JLS	3	Negative (bit 9 = 1)	Less Than (bit 9 = 1)
JOR	JO	JO	4	Overflow designator is set	
JCR	JC	JC	5	Carry designator is set	
JPTR	JPT	JPT	6	Power is out of tolerance	
JBR	JB	JB	7	Bootstrap 2 is selected	
JR	J	J	10	Unconditional Jump	
JSR	JS	JS	11	Stop; jump on restart	
JKSR	JKS	JKS	12	Stop if program stop key 1 is selected, jump on restart	
JKSR	JKS	JKS	13	Stop if program stop key 2 is selected, jump on restart	
----	---	---	14-17	Not assigned	

(4) RX Format - CONDITIONAL JUMP
Test for the condition specified in Table IV for the a-value and perform one of the following.

(1) If the specified condition is met, load (Y) in P (jump to the instruction located at the address specified by the contents of memory address Y). If a specified Stop, or a Stop Key condition is met, disable RTC and stop the computer. On restart, load (Y) in P (jump to the instruction located at the address specified by the contents of memory address Y).

(2) If the specified jump condition is not met, execute the next instruction. If the specified stop condition is not met, execute the jump without stopping.

---

(4) See Table IV

Operation Code 41

XJR — RR Format - INDEX JUMP
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, decrease (R_a) by 1 and load (R_m) in P (jump to the instruction located at the address stored in R_m).

(2) If (R_a) equals zero, execute the next instruction.

LJ — RI Format, Type 1 - LOCAL JUMP INDIRECT
Unconditionally jump to the address specified by the contents of memory address Y. Y = (P)$\pm$D.

XJK — RK Format - INDEX JUMP
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, decrease (R_a) by 1 and load operand Y in P (jump to the instruction located at address Y).

(2) If (R_a) equals zero, execute the next instruction.

XJ — RX Format - INDEX JUMP
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, decrease (R_a) by 1 and load (Y) in P (jump to the instruction located at the address specified by the contents of memory address Y).

(2) If (R_a) equals zero, execute the next instruction.

Operation Code 42

JLRR — RR Format - JUMP AND LINK REGISTERS
Store (P)+1 in R_a, and load (R_m) in P (jump to the instruction located at the address stored in R_m).

\- — RI Format - Not assigned

JLR — RK Format - JUMP AND LINK REGISTER
Store (P)+2 in R_a, and load operand Y in P (jump to the instruction located at the address Y).

JLK — RX Format - JUMP AND LINK REGISTER
Store (P)+2 in R_a, and load (Y) in P (jump to the instruction located at the address specified by the contents of address Y).

Operation Code 43

\- — RR Format - Not assigned

LJLM — RI Format, Type 1 - LOCAL JUMP AND LINK MEMORY
Store (P)+1 at memory address Y, and load Y+1 in P (jump to the instruction located at memory address Y+1. Y = (P)$\pm$d.

JLM RK Format - JUMP AND LINK MEMORY
Store (P)+2 at memory address Y, and load Y+1 in P (jump to the instruction located at memory address Y+1).

JLM RX Format - JUMP AND LINK MEMORY
Store (P)+2 at the address specified by the contents of address Y, and load (Y+1) in P (jump to the instruction located at the address specified by the contents of address Y+1).

Operation Code 44

JZR RR Format - JUMP REGISTER = 0
Test (R_a) and perform one of the following:

(1) If (R_a) equals zero, load (R_m) in P (jump to the instruction located at the address stored in R_m).

(2) If (R_a) does not equal zero, execute the next instruction.

LJE RI Format, Type 1 - LOCAL JUMP EQUAL
Test the Condition Code in the Status Register and perform one of the following:

(1) If bit 8 of the Condition Code is zero, load Y in P (jump to the instruction located at memory address Y). Y = (P)$\pm$d.

(2) If bit 8 of the Condition Code is not zero, execute the next instruction.

JZ RK Format - JUMP REGISTER = 0
Test (R_a) and perform one of the following:

(1) If (R_a) equals zero, load operand Y in P (jump to the instruction located at the address specified by operand Y).

(2) If (R_a) does not equal zero, execute the next instruction.

JZ RX Format - JUMP REGISTER = 0
Test (R_a) and perform one of the following:

(1) If (R_a) equals zero, load (Y) in P (jump to the instruction located at address specified by the contents of memory address Y).

(2) If (R_a) does not equal zero, execute the next instruction.

Operation Code 45

JNZR RR Format - JUMP REGISTER $\neq$ 0
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, load (R_m) in P (jump to the instruction located at the address stored in R_m).

(2) If (R_a) equals zero, execute the next instruction.

LJNE RI Format, Type 1 - LOCAL JUMP NOT EQUAL
Test the Condition Code and perform one of the following:

(1) If bit 8 of the Condition Code is one, load Y in P (jump to the instruction located at memory address Y). Y = (P)±d.

(2) If bit 8 of the Condition Code is not one, execute the next instruction.

JNZ RK Format - JUMP REGISTER ≠ 0
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, load Y in P (jump to the instruction located at the address specified by operand Y).

(2) If (R_a) equals zero, execute the next instruction.

JNZ RX Format - JUMP REGISTER ≠ 0
Test (R_a) and perform one of the following:

(1) If (R_a) does not equal zero, load (Y) in P (jump to the instruction located at the address specified by the contents of memory address Y).

(2) If (R_a) equals zero, execute the next instruction.

Operation Code 46

JPR RR Format - JUMP REGISTER POSITIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is equal to or greater than zero, load (R_m) in P (jump to the instruction located at the address stored in R_m).

(2) If (R_a) is less than zero, execute the next instruction.

LJGE RI Format, Type 1 - LOCAL JUMP GREATER THAN OR EQUAL
Test the Condition Code and perform one of the following:

(1) If bit 9 of the Condition Code is a zero, load Y in P (jump to the instruction located at memory address Y). Y = (P)±d.

(2) If bit 9 of the Condition Code is not zero, execute the next instruction.

JP RK Format - JUMP REGISTER POSITIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is equal to or greater than zero, load Y in P (jump to the instruction located at the address specified by operand Y).

(2) If (R_a) is less than zero, execute the next instruction.

JP RX Format - JUMP REGISTER POSITIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is equal to or greater than zero, load (Y) in P (jump to the instruction located at address specified by the contents of memory address Y).

(2) If (R_a) is less than zero, execute the next instruction.

Operation Code 47

JNR RR Format - JUMP REGISTER NEGATIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is less than zero, load (R_m) in P (jump to the instruction located at the address stored in R_m).

(2) If (R_a) is equal to or greater than zero, execute the next instruction.

LJLS RI Format, Type 1 - LOCAL JUMP LESS THAN
Test the Condition Code and perform one of the following:

(1) If bit 9 of the Condition Code is one, load Y in P (jump to the instruction located at memory address Y). Y = (P)$\pm$d.

(2) If bit 9 of the Condition Code is not one, execute the next instruction.

JN RK Format - JUMP REGISTER NEGATIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is less than zero, load Y in P (jump to the instruction located at the address specified by operand Y).

(2) If (R_a) is equal to or greater than zero, execute the next instruction.

JN RX Format - JUMP REGISTER NEGATIVE
Test (R_a) and perform one of the following:

(1) If (R_a) is less than zero, load (Y) in P (jump to the instruction located at address specified by the contents of memory address Y).

(2) If (R_a) is equal to or greater than zero, execute the next instruction.

Operation Code 50 - Not assigned

Operation Code 51 - Not assigned

Operation Code 52 - Not assigned

Operation Code 53 - Not assigned

Operation Code 54

- RR Format - LOAD ADDRESS REGISTER
  Load the page address register specified by (R_a) with bits 15 and 5-0 of (R_m). Only bits 0 through 5 of R_a are interpreted.

- RI Format - LOAD ADDRESS REGISTER
  Load the page address register specified by (R_a) with bits 15 and 5-0 of the contents of the memory address specified by (R_m). Only bits 0 through 5 of R_a are interpreted.

- RK Format - Not assigned

- RX Format - LOAD ADDRESS REGISTER MULTIPLE
  Load bits 15 and 5-0 of the contents of sequential memory addresses beginning at Y, into sequential page address registers beginning at the address word defined by (R_a) and continuing until the number of executions equals the count defined by (R_a). Bits 0 through 5 of R_a designate the word and bits 8 through 13 of R_a designate the count. A count of zero causes all page registers to be loaded.

Operation Code 55

- RR Format - STORE ADDRESS REGISTER
  Store the page address register specified by (R_a) in R_m. Only bits 0 through 5 of R_a are interpreted.

- RI Format - STORE ADDRESS REGISTER
  Store the page address register specified by (R_a) in the memory address specified by (R_m). Only bits 0 through 5 of R_a are interpreted.

- RK Format - Not assigned

- RX Format - STORE ADDRESS REGISTER MULTIPLE
  Store sequential page address registers beginning at the address word defined by (R_a) into sequential memory addresses beginning at Y and continuing until the number of executions equals the count defined by (R_a). Bits 0 through 5 of R_a designate the word and bits 8 through 13 designate the count. A count of zero causes all page registers to be stored.

Operation Code 56 - Not assigned

Operation Code 57 - Not assigned

Operation Code 60

- RL (00) Format - LOGICAL RIGHT SINGLE SHIFT
Shift (R_a) right n places with zero extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (01) Format - ALGEBRAIC RIGHT SINGLE SHIFT
Shift (R_a) right n places with sign extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (10) Format - LOGICAL RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) right n places with zeros extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (11) Format - ALGEBRAIC RIGHT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) right n places with sign extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

Operation Code 61

- RL (00) Format - ALGEBRAIC LEFT SINGLE SHIFT
Shift (R_a) left n places with zeros extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (01) Format - CIRCULAR LEFT SINGLE SHIFT
Shift (R_a) left circular n places. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (10) Format - ALGEBRAIC LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) left n places with zeros extended to fill. "n" is the value in bits 0-3 of the instruction m-designator.

- RL (11) Format - CIRCULAR LEFT DOUBLE SHIFT
Shift the double length (R_a, R_{a+1}) left circular n places. "n" is the value in bits 0-3 of the instruction m-designator.

Operation Code 62

- RL (00) Format - SUBTRACT
Subtract the 4-bit literal contained in the m-designator of the instruction from (R_a), store the result in R_a, and set the Condition Code (table XIII).

- RL (01) Format - SUBTRACT DOUBLE

Subtract the 4-bit literal contained in the m-designator of the instruction from the double length (R_a, R_{a+1}), store the result in R_a, R_{a+1}, and set the Condition Code (table XIII).

- RL (10) Format - ADD
Add the 4-bit literal contained in the m-designator of the instruction to (R_a), store the result in R_a, and then set the Condition Code (table XIII).

- RL (11) Format - ADD DOUBLE
  Add the 4-bit literal contained in the m-designator of the instruction to the double length (R_a, R_{a+1}), store the result in R_a, R_{a+1}, and then set the Condition Code (table XIII).

Operation Code 63

- RL (00) Format - LOAD
  Load the 4-bit literal contained in the m-designator of the instruction into R_a and set the Condition Code.

- RL (01) Format - COMPARE
  Arithmetically compare the 4-bit literal contained in the m-designator of the instruction with (R_a) and set the Condition Code.

- RL (10) Format - MULTIPLY
  Multiply the 4-bit literal contained in the m-designator of the instruction by (R_{a+1}) and store the double length result in R_a, R_{a+1}; then set the Condition Code (table XIII).

- RL (11) Format - DIVIDE
  Divide the double length (R_a, R_{a+1}) by the 4-bit literal contained in the m-designator of the instruction, store the quotient in R_{a+1} and the remainder in R_a; then set the Condition Code (table XIII).

Operation Code 64

- RR Format - Not assigned

- RI Format - Not assigned

- RK Format - Not assigned

- RX Format - BYTE SUBTRACT
  Subtract the selected byte of memory address Y from (R_a), store the result in R_a, and set the Condition Code (table XIII).

Operation Code 65

- RR Format - Not assigned

- RI Format - Not assigned

- RK Format - Not assigned

- RX Format - BYTE ADD
  Add the selected byte from memory address Y to (R_a), store the result in R_a, and set the Condition Code (table XIII).

Operation Code 66

- RR Format - Not assigned

- RI Format - Not assigned

- RK Format - Not assigned

- RX Format - BYTE COMPARE
Arithmetically compare (R_a) to the selected byte of memory address Y, and set the Condition Code (table XIII).

Operation Code 67

- RR Format - Reserved for user-designated macroinstructions.

- RI Format - Not assigned

- RK Format - Not assigned

- RX Format - BYTE COMPARE AND INDEX BY 1
Arithmetically compare (R_a) to the selected byte of memory address Y, set the Condition Code (table XIII), and increment (R_m) by 1.

Operation Code 70

(5) ACR, m — RR Format - CHANNEL CONTROL (COMMAND OR CHAINING)
Perform the operation specified by the m-designator as specified in table V on all I/O channels or the channel specified by the a-designator as specified in table V. For chaining, the a-designator is not used.

(6) IO — RX Format - INITIATE TRANSFER (CHAINING)
Load the control memory Buffer Control Word (BCW) and Buffer Address Pointer (BAP) locations with the contents of memory addresses Y and Y+1 respectively, and enable input or output transfers on the channel corresponding to the chain executing the instruction. Address Y must be even. Chaining on the channel (input or output) is disabled until transfer termination. Transfer termination results when the buffer word count decrements to zero. Chaining is re-enabled after transfer termination. The a-designator is interpreted as specified in table VI, and is applicable for both parallel and serial transfers.

Operation Code 71

ICK or OCK — RK Format - INITIATE CHAIN (COMMAND)
Initiate chaining for the channel specified by the a-designator. The m-designator specifies the chain: m = 2, input chain; m = 6, output chain. Load the corresponding Chain Pointer with the operand Y for use as the starting address for the selected chain.

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(5) See Table V
(6) See Table VI

TABLE V. CHANNEL CONTROL INSTRUCTION m-DESIGNATOR

ULTRA Symbol	m Value	Instruction
	0	*Master clear all channels (deactivate all data buffers and disable all external interrupt data and Class III interrupts).
	1	Not assigned
	2	Not assigned
	3	Not assigned
ACR	4	*Set External Interrupt Enable (EIE) lines on all channels. Accept external interrupt data on all channels. Store the data at assigned memory addresses and clear EIE on affected channel.
	5	*Clear EIE on all channels. (Do not accept external interrupt data from any channel.)
	6	*Enable external interrupt monitors on all channels. Generate the Class III, Priority 2 interrupt if any external interrupt was accepted with monitors disabled. Enable generation of Class III priority 2, 3, and 4 interrupts.
	7	*Disable generating the Class III, Priority 2, 3, and 4 interrupts for all channels.
	10	Master clear the channel specified by the a-designator.
	11	Not assigned
	12	Not assigned
	13	Not assigned
CCR	14	Set EIE line for channel specified by the a-designator. (Accept external interrupt data on the channel.) Store the data at the assigned memory address and clear the EIE.
	15	Clear EIE line for channel specified by the a-designator. (Do not accept external interrupt data on the channel.)
	16	Enable external interrupt monitor on the channel specified by the a-designator. Generate the Class III, Priority 2 interrupt if any external interrupt was accepted on the channel with monitor disabled. Enable generation of Class III priority 2, 3, and 4 interrupts on the channel.
	17	Disable generating the Class III, Priority 2, 3, and 4 interrupts for the channel specified by the a-designator.

* The a-designator must be zero.

TABLE VI. INITIATE TRANSFER INSTRUCTION a-DESIGNATOR

a. Parallel or NTDS Serial

ULTRA Symbol	a-Value	Transfer Mode
IO	0	Input data
	1	Output data
	2	External function
	3	External function with force
	4-17	Not assigned

b. MIL-STD-188 Serial

a-Value	Function
X X X 0	Serial input without monitor
X X X 1	Serial input with monitor
X X 0 X	Generate-check odd parity
X X 1 X	Generate-check even parity
X 0 X X	Disable parity
X 1 X X	Enable parity
0 X X X	Serial input without suppress
1 X X X	Serial input with suppress

(7) LCMK RK Format - LOAD CONTROL MEMORY (CHAINING)
Load the control memory location specified by the m-designator as specified in table VII with Y. The a-designator is not used.

LCM RX Format - LOAD CONTROL MEMORY (COMMAND)
Load the control memory location specified by the m-designator as specified in table VII with the contents of the memory address specified by Y. The a-designator specifies the channel.

LCM RX Format - LOAD CONTROL MEMORY (CHAINING)
Load the control memory location specified by the m-designator as specified in table VII with the contents of address Y. The a-designator is not used.

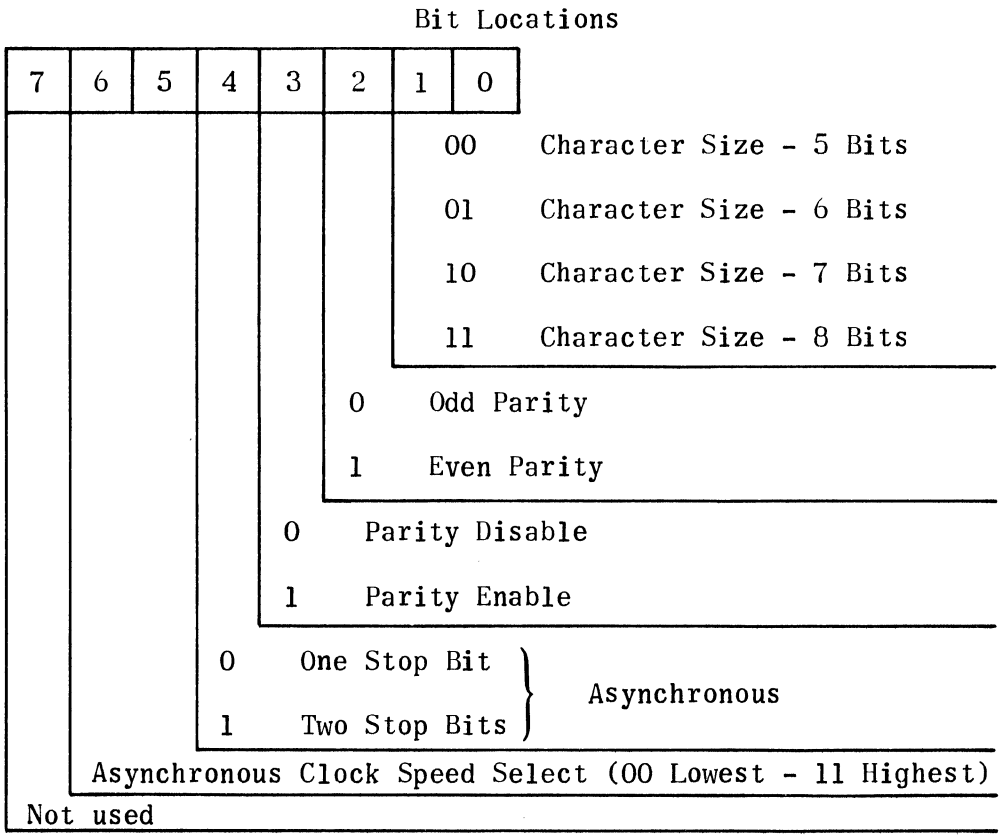
(7) See Table VII

TABLE VII. LOAD, STORE, CONTROL MEMORY VARIABLES

a. m-designator

m-Value	Location
0	TM, O, B and Buffer Word Count (IN)
1	Buffer Address Pointer (IN)
2	Chain Address Pointer (IN)
3	Not assigned
4	TM, O, B and Buffer Word Count (OUT)
5	Buffer Address Pointer (OUT)
6	Chain Address Pointer (OUT)
7	Not assigned
10	Monitor Register (MIL-STD-188 and RS-232 Serial)
11	Suppress Register (MIL-STD-188 and RS-232 Serial)
12	Serial Mode Information (MIL-STD-188 and RS-232 Serial)
13-17	Unassigned

b. Serial Mode In



Operation Code 72

RCM — RX Format - STORE CONTROL MEMORY (COMMAND)
Store the contents of the control memory location specified by the m-designator as specified in table VII at memory address Y. The a-designator specifies the channel.

SCM — RX Format - STORE CONTROL MEMORY (CHAINING)
Store the contents of the control memory location specified by the m-designator as specified in table VII at memory address Y. The a-designator is not used.

Operation Code 73

RR Format - HALT/INTERRUPT (CHAINING)
Perform one of the following as specified by the a-designator; the m-designator is not used:

HCR — (1) If a = 0, halt the chaining action.

IPR — (2) If a = 1, generate the Chain interrupt.

\- — RX Format - SET/CLEAR FLAG (CHAINING)
Set or clear the most significant two bits (flag) of the memory location specified by Y as specified by the a-designator; the m-designator is not used.

SF — (1) If a = 1, set flag.

ZF — (2) If a = 0, clear flag.

Operation Code 74

\- — RK Format - CONDITIONAL JUMP (CHAINING)
Jump to the address specified by the operand y if the condition specified by table VIII is met. If none of the conditions are met, execute the next instruction. After execution of this instruction the Monitor Flag or Suppress Flag is cleared.

TABLE VIII. CONDITIONAL JUMP INSTRUCTION a-DESIGNATOR

a-Designator	Jump Operation
0	Unconditional Jump
1	Jump if Suppress Flag Not Set
2	Jump if Monitor Flag Set

Operation Code 75

- RR Format - SEARCH FOR SYNC SET SUPPRESS, SET MONITOR (CHAINING)

(1) When bit 0 is set in the m-designator and the synchronous serial interface is in use, at each bit time the input channel compares the value of the last n bits of input data to the contents of the suppress register (n is equal to the character length of the channel). When a match occurs, the next character of n bits is compared to the suppress register. If the next character compare results in a match, the suppress designator is set and the next instruction of the chain is enabled. If the next character compare does not result in a match, the suppress designator is not set and the next instruction of the chain is enabled.

(2) When bit 1 is set in the m-designator, input data matching the character loaded into the suppress register shall not be transferred to memory. Occurrence of suppression shall cause the suppress flag to be set.

(3) When bit 2 is set in the m-designator and the interface is either the synchronous or asynchronous MIL-STD-188 or RS-232 serial interface, the last n bits of input data are compared to the monitor register. When a match occurs, the monitor flag is set and that character is input as data. The buffer is then terminated and the chain is enabled.

(4) When the m-designator equals zero, disable the search for sync function on the channel.

Operation Code 76

- RR Format - SET-CLEAR DISCRETES (COMMAND)
Set or clear the discretes associated with the MIL-STD-188 or RS-232 serial interface as specified by the m-designator. The a-designator specifies the channel. Discrete set-clear functions in the MIL-STD-188 interface are specified in table IX. Discrete set-clear functions in the RS-232 interface are specified in table X.

- RR Format - SET-CLEAR DISCRETES (CHAINING)
Set or clear the discretes associated with the MIL-STD-188 or RS-232 serial interface as specified by the m-designator. The a-designator is not used. Discrete set-clear functions are specified in table IX and table X.

- RX Format - STORE STATUS (COMMAND)
Store the data on the input data bus at the memory location specified by operand Y. The data is interpreted as specified in table XI for the MIL-STD-188 serial interface and as shown in table XII for the RS-232 serial interface. The a-designator specifies the channel.

- RX Format - STORE STATUS (CHAINING)
Shall store the data on the input data bus at the memory location specified by operand Y. The data is interpreted as shown in table XI for the MIL-STD 188 serial interface and as specified in table XII for the RS-232 serial interface. The a-designator is not used.

Operation Code 77 - Unassigned

TABLE IX. MIL-STD-188 DISCRETE SET-CLEAR FUNCTIONS

m-Designator	Function	Discrete	Line Designator
1111	Set	Outbound Control Line 1	A1
1110	Clear	Outbound Control Line 1	A1
1101	Set	Outbound Control Line 2	D1
1100	Clear	Outbound Control Line 2	D1
1011	Set	Outbound Control Line 3	F1
1010	Clear	Outbound Control Line 3	F1
1001	Set	Outbound Control Line 4	G1
1000	Clear	Outbound Control Line 4	G1
0111	Set	Outbound Control Line 5	H1
0110	Clear	Outbound Control Line 5	H1
0101	Set	Outbound Control Line 6	J1
0100	Clear	Outbound Control Line 6	J1
0011	Set	Not used	
0010	Clear	Not used	
0001	Clear	Internal Loop Test	
0000	Set	Internal Loop Test	

TABLE X. RS-232 DISCRETE SET-CLEAR FUNCTION

m-Designator	Function	Discrete
1111	Set	Loop Test
1110	Clear	Loop Test
1101	Set	Data Terminal Ready
1100	Clear	Data Terminal Ready
1011	Set	New Sync
1010	Clear	New Sync

TABLE X. RS-232 DISCRETE SET-CLEAR FUNCTION (CONT)

m-Designator	Function	Discrete
1001	Set	Request to Send
1000	Clear	Request to Send
0111	Set	Enable Ring Interrupt
0110	Clear	Enable Ring Interrupt
0101		Spare
0100		Spare
0011		Spare
0010		Spare
0001	Clear	Internal Loop Test
0000	Set	Internal Loop Test

TABLE XI. STORE STATUS BIT INTERPRETATION, MIL-STD-188 SERIAL INTERFACE

Bit	Function	Description
0	Break	The serial I/O did not detect a stop bit. Used in asynchronous mode only.
1	Overrun	The serial I/O did not transfer a data word to memory before another I/O word was received.
2	Parity Error	The serial I/O detected a parity error on an input data word.
3	E6 Active	Control Line E6 was set active by an external device.

TABLE XII. STORE STATUS BIT INTERPRETATION, RS-232 SERIAL INTERFACE

Bit	Function	Description
0	Break	The serial I/O did not detect a stop bit. Used in asynchronous mode only.
1	Overrun	The serial I/O did not transfer to memory before another I/O word was received.
2	Parity error	The serial I/O detected a parity error on an input data word.
3	Clear to Send	Clear to Send was set active by an external device.

TABLE XIII. CONDITION DESIGNATORS

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
00 RR Diagnostic Return	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Byte Load	0	0	0	X	(R_a)
01 RR Load	0	0	X	X	(R_a)
RI Load	0	0	X	X	(R_a)
RK Load	0	0	X	X	(R_a)
RX Load	0	0	X	X	(R_a)
02 RR Unary-Arithmetic					
m = 0 Make Positive	X	X	X	X	(R_a)
m = 1 Make Negative	X	0	X	X	(R_a)
m = 2 Round R_a	X	X	X	X	(R_a)
m = 3 Unassigned	NC	NC	NC	NC	
m = 4 Twos Complement Single	X	X	X	X	(R_a)
m = 5 Twos Complement Double	X	X	X	X	(R_a, R_{a+1})
m = 6 Ones Complement Single	0	0	X	X	(R_a)
m = 7 Unassigned	NC	NC			
m = 10 Increment (R_a) by 1	X	X	X	X	(R_a)
m = 11 Decrement (R_a) by 1	X	X	X	X	(R_a)
m = 12 Increment (R_a) by 2	X	X	X	X	(R_a)
m = 13 Decrement (R_a) by 2	X	X	X	X	(R_a)
m = 14 - 17	NC	NC	NC	NC	

NC: no change in the designator

0: end result is 0.

X: contingent upon the designator function for that instruction

NA: not applicable

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
RI-2 Load	0	0	X	X	(R_a, R_{a+1})
RK Unassigned	NC	NC	NC	NC	
RX Load Double	0	X	X	X	(R_a, R_{a+1})
03 RR Unary-Control					
m = 0-3	0	0	X	X	(R_a)
m = 4 - 17	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Load Multiple	NC	NC	NC	NC	
04 RR Unary-Shift					
m = 0 Unassigned	NC	NC	NC	NC	
m = 1 Reverse Register	0	0	X	X	(R_a)
m = 2 Count Ones	NC	NC	NC	NC	
m = 3 Scale Factor	NC	NC	NC	NC	
m = 4 - 17	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Byte Load & Index by 1	0	0	0	X	(R_a)
05 RR Set Bit	0	0	X	X	(R_a)
RI Load & Index by 1	0	0	X	X	(R_a)
RK Unassigned	NC	NC	NC	NC	
RX Load and Index by 1	0	0	X	X	(R_a)
06 RR Clear Bit	0	0	X	X	(R_a)
RI Load Double & Index by 2	0	0	X	X	(R_a, R_{a+1})
RK Unassigned	NC	NC	NC	NC	
RX Load Double & Index by 2	0	0	X	X	(R_a, R_{a+1})
07 RR Compare Bit	0	0	X	X	(R_a)
RI Load PSW	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Load PSW	NC	NC	NC	NC	

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
10 RR Logical Right Single Shift	0	0	X	X	(R_a)
RI Unassigned	NC	NC	NC	NC	
RK Logical Right Single Shift	0	0	X	X	(R_a)
RX Byte Store	NC	NC	NC	NC	
11 RR Algebraic Right Single Shift	0	0	X	X	(R_a)
RI Store	NC	NC	NC	NC	
RK Algebraic Right Single Shift	0	0	X	X	(R_a)
RX Store	NC	NC	NC	NC	
12 RR Logical Right Double Shift	0	0	X	X	(R_a, R_{a+1})
RI Store Double	NC	NC	NC	NC	
RK Logical Right Double Shift	0	0	X	X	(R_a, R_{a+1})
RX Store Double	NC	NC	NC	NC	
13 RR Algebraic Right Double Shift	0	0	X	X	(R_a, R_{a+1})
RI Unassigned	NC	NC	NC	NC	
RK Algebraic Right Double Shift	0	0	X	X	(R_a, R_{a+1})
RX Store Multiple	NC	NC	NC	NC	
14 RR Algebraic Left Single Shift	0	X	X	X	(R_a)
RI Unassigned	NC	NC	NC	NC	
RK Algebraic Left Single Shift	0	X	X	X	(R_a)
RX Byte Store & Index by 1	NC	NC	NC	NC	
15 RR Circular Left Single Shift	0	0	X	X	(R_a)
RI Store & Index by 1	NC	NC	NC	NC	
RK Circular Left Single Shift	0	0	X	X	(R_a)
RX Store & Index by 1	NC	NC	NC	NC	

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
16 RR Algebraic Left Double Shift	0	X	X	X	(R_a, R_{a+1})
RI Store Double & Index by 2	NC	NC	NC	NC	
RK Algebraic Left Double Shift	0	X	X	X	(R_a, R_{a+1})
RX Store Double & Index by 2	NC	NC	NC	NC	
17 RR Circular Left Double Shift	0	0	X	X	(R_a, R_{a+1})
RI Store Zeros	NC	NC	NC	NC	
RK Circular Left Double Shift	0	0	X	X	(R_a, R_{a+1})
RX Store Zeros	NC	NC	NC	NC	
20 RR Subtract	X	X	X	X	(R_a)
RI Subtract	X	X	X	X	(R_a)
RK Subtract	X	X	X	X	(R_a)
RX Subtract	X	X	X	X	(R_a)
21 RR Subtract Double	X	X	X	X	(R_a, R_{a+1})
RI Subtract Double	X	X	X	X	(R_a, R_{a+1})
RK Unassigned	NC	NC	NC	NC	
RX Subtract Double	X	X	X	X	(R_a, R_{a+1})
22 RR Add	X	X	X	X	(R_a)
RI Add	X	X	X	X	(R_a)
RK Add	X	X	X	X	(R_a)
RX Add	X	X	X	X	(R_a)
23 RR Add Double	X	X	X	X	(R_a, R_{a+1})
RI Add Double	X	X	X	X	(R_a, R_{a+1})
RK Unassigned	NC	NC	NC	NC	
RX Add Double	X	X	X	X	(R_a, R_{a+1})
24 RR Compare	X	X	X	X	Result
RI Compare	X	X	X	X	Result
RK Compare	X	X	X	X	Result
RX Compare	X	X	X	X	Result
25 RR Compare Double	X	X	X	X	Result
RI Compare Double	X	X	X	X	Result

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
RK Unassigned	NC	NC	NC	NC	
RX Compare Double	X	X	X		Result
26 RR Multiply	0	0	X	X	(R_a, R_{a+1})
RI Multiply	0	0	X	X	(R_a, R_{a+1})
RK Multiply	0	0	X	X	(R_a, R_{a+1})
RX Multiply	0	0	X	X	(R_a, R_{a+1})
27 RR Divide	0	X	X	X	(R_{a+1})
RI Divide	0	X	X	X	(R_{a+1})
RK Divide	0	X	X	X	(R_{a+1})
RX Divide	0	X	X	X	(R_{a+1})
30 RR AND	0	0	X	X	(R_a)
RI AND	0	0	X	X	(R_a)
RK AND	0	0	X	X	(R_a)
RX AND	0	0	X	X	(R_a)
31 RR OR	0	0	X	X	(R_a)
RI OR	0	0	X	X	(R_a)
RK OR	0	0	X	X	(R_a)
RX OR	0	0	X	X	(R_a)
32 RR Exclusive OR	0	0	X	X	(R_a)
RI Exclusive OR	0	0	X	X	(R_a)
RK Exclusive OR	0	0	X	X	(R_a)
RX Exclusive OR	0	0	X	X	(R_a)
33 RR Masked Substitute	0	0	X	X	(R_a)
RI Masked Substitute	0	0	X	X	(R_a)
RK Masked Substitute	0	0	X	X	(R_a)
RX Masked Substitute	0	0	X	X	(R_a)
34 RR Compare Masked	0	0	X	X	Result
RI Compare Masked	0	0	X	X	Result
RK Compare Masked	0	0	X	X	Result
RX Compare Masked	0	0	X	X	Result

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
35 RR I/O Command	NC	NC	NC	NC	
RI Biased Fetch	0	0	X	X	(Y)
RK Execute Remote	NC	NC	NC	NC	
RX Biased Fetch	0	0	X	X	(Y)
36 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
37 Unassigned	NC	NC	NC	NC	
40 - 47	NC	NC	NC	NC	
50 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
51 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
52 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
53 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
54 RR Load Address Register	NC	NC	NC	NC	
RI Load Address Register	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Load Address Register Multiple	NC	NC	NC	NC	
55 RR Store Address Register	NC	NC	NC	NC	
RI Store Address Register	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Store Address Register	NC	NC	NC	NC	
56 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
57 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
60 RL-1 Logical Right Single-Shift	0	0	X	X	(R_a)
RL-1 Algebraic Right Single-Shift	0	0	X	X	(R_a)
RL-3 Logical Right Double-Shift	0	0	X	X	(R_a, R_{a+1})
RL-4 Algebraic Right Double-Shift	0	0	X	X	(R_a, R_{a+1})
61 RL-1 Algebraic Left Single-Shift	0	X	X	X	(R_a)
RL-2 Circular Left Single-Shift	0	0	X	X	(R_a)
RL-3 Algebraic Left Double-Shift	0	X	X	X	(R_a, R_{a+1})
RL-4 Circular Left Double-Shift	0	0	X	X	(R_a, R_{a+1})
62 RL-1 Subtract	X	X	X	X	(R_a)
RL-2 Subtract Double	X	X	X	X	(R_a, R_{a+1})
RL-3 Add	X	X	X	X	(R_a)
RL-4 Add Double	X	X	X	X	(R_a, R_{a+1})
63 RL-1 Load	0	0	0	X	(R_a)
RL-2 Compare	X	X	X	X	(R_a)
RL-3 Multiply	0	0	X	X	(R_a, R_{a+1})
RL-4 Divide	0	X	X	X	(R_{a+1})

TABLE XIII. CONDITION DESIGNATORS (CONT)

Instruction	Carry Designator	Overflow Designator	Condition Code (9)	Condition Code (8)	Register
64 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Byte Subtract	X	X	X	X	(R_a)
65 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Byte Add	X	X	X	X	(R_a)
66 RR Unassigned	NC	NC	NC	NC	
RI Unassigned	NC	NC	NC	NC	
RK Unassigned	NC	NC	NC	NC	
RX Byte Compare and Index by 1	X	X	X	X	Result
67 RR Reserved	As required	As required	As required		
RI Unassigned	NC	NC	NC	NC	
RX Unassigned	NC	NC	NC	NC	
RX Byte Compare and Index by 1	X	X	X	X	Result
70 - 77	NA	NA	NA	NA	

APPENDIX C

MICROPROGRAM LISTING

The microprogram, contained in the ROM, provides internal control for the DPS and provides the microinstruction sequences for execution of each macroinstruction. Most subroutines are preceded by a title or macroinstruction function code. See the operational description near the end of Chapter 3 for an introduction to microprogram operation.

```
EFGPA.GPA8,S    TPFS,MUYK20/BASICAPE
CYCLE 01   GPA ASSEMBLED BY V-1   ON 15 OCT 73 AT    20:07:15
                                            .ULTRA    APE   .
                                                      PR8S        .
                                            .
                                            .
                          000000            S0        EQU      0  .  S1      NON-EXISTANT
                          000000            D0        EQU      0  .  D1      NON-EXISTANT
                          000001            BRKPT     EQU      1  .  D1/S1   BREAKPOINT REGISTER
                          000002            PREG      EQU      2  .  D1/S1   P REGISTER
                          000003            MDR       EQU      3  .  D1/S1   MEMORY DATA REGISTER
                          000004            PTBLS     EQU      4  .     S1   PAGE TABLE
                          000010            PTBLD     EQU    010  .     D2   PAGE TABLE
                          000006            SM        EQU      6  .     S1   SHIFT MATRIX OUTPUT
                          000007            PPROD     EQU      7  .     S1   PARTIAL PRODUCT
                          000007            MONCLK    EQU      7  .     S1   MONITOR CLOCK
                          000000            UP        EQU      0  .  D2/S2   MICRO P
                          000001            CREG      EQU      1  .  D2/S2   CONDITION REGISTER
                          000002            DREG      EQU      2  .  D2/S2   DISPLAY REGISTER
                          000003            CM        EQU      3  .     S2   CONSOLE MODE
                          000003            SHIFTS    EQU      3  .     S2   SHIFT COUNTER
                          000003            NORM      EQU      3  .  S2    NORMALIZE
                          000004            RTCU      EQU      4  .     S2   RTC UPPER
                          000005            STAT1     EQU      5  .  D1/S2   STAT 1
                          000006            STAT2     EQU      6  .  D1/S2   STAT 2
                          000007            RTCL      EQU      7  .  D1/S2   RTC LOWER
                          000010            RGRS      EQU    010  .     S2   GENERAL REGISTER STACK
                          000011            CORTBL    EQU    011  .     S2   CORDIC TABLE
                          000014            INTCOD    EQU    014  .     S2   INTERRUPT CODES
                          000014            XLTRM     EQU    014  .  D2      TRANSLATOR-M.
                          000005            IDP       EQU      5  .     S1   INDIRECT POINTER-I/O XLATOR
                          000015            XLTR      EQU    015  .  D2/S2   I/O TRANSLATOR
                          000013            IRS       EQU    013  .     S2   INSTRUCTION REGISTER
                          000012            IRD       EQU    012  .     D2   INSTRUCTION REGISTER
                          000012            IRAM      EQU    012  .     S2   I.R. A AND M FIELDS - SIGN EXTED
                          000017            IOCMR     EQU    017  .  D2/S2   I/O CONTROL MEMORY REGISTER
                          000016            IDR       EQU    016  .     S2   INPUT DATA
                          000016            ODR       EQU    016  .  D2      OUTPUT DATA
                          000004            RGRD      EQU      4  .     D1   GENERAL REGISTER STACK
                          000016            SHIFTD    EQU    016  .     D1   SHIFT COUNTER
                          000017            MAR       EQU    017  .     D1   MEMORY ADDRESS REGISTER
                          000003            CK        EQU      3  .     D2   CYCLE COUNT
                          000013            SGR       EQU    013  .     D2   S GENERAL REGISTER
                          000010            PAC       EQU    010  .     D1   PAGE ADDRESS COUNTER
                                            .
                                            .
                                            .
         00     000000  14 17 004                     BMJS 0004          . JP TO DIAG PROG IF DIAG JP SWITCH IS UP
                000001  00 17 03 01                   T     A7,CM,1      . CONSOLE MODE TO A7
                000002  01 0017                       J     MCSUB0       . JUMP TO MASTER CLEAR SEQ
                000003  15 16 00 03                   MC    016,0,3      . DISABLE MONITOR CLOCK
                000004  01 7771                       J     07771        . JUMP TO ADDRESS 7771
                000005  12 10 000                     TC1   A0,0         . TRANSFER ZEROS TO A0
                000006  01 6000                       J     06000        . JUMP TO ADDRESS 6000
                000007  06 11 10 03                   L1    A1,A0,3      . (A0)=#77777.  1'S COMP OF A0 TO A1.
                000010  01 7765                       J     07765        . LOAD MICRO HOLD REG WITH 0011
                000011  00 11 00 01                   T     A1,UP,1      . MICRO P HOLD TO A1
```

```
 56.          000012  01 7773                          J     07773          . JUMP TO DIAG RETURN ROUTINE
 57.          000013  13 13 017                       TC2   SGR,017        . SETUP SGR FOR DIAG RETURN ROUTINE
 58.                                                  .
 59.                                                  SETADR 017  .
 60.                                                  .
 61.                                                  . MASTER CLEAR SUBROUTINE
 62.                                                  .
 63.          000017  12 10 000                 MCSUB0  TC1   PAC,0          . CLR PAGE ADDRESS COUNTER
 64.          000020  13 03 077                       TC2   CK,077         . REPEAT CT
 65.          000021  16 10 001                       RN    1              . REPEAT NEXT 2 INST
 66.          000022  00 10 10 02                     T     PTBLD,PAC,2    . PAGE ADDRESS VALUE TO PAGE TABLE
 67.          000023  10 10 001                       AC    A0,1           . INC PAGE TABLE VALUE
 68.          000024  15 16 00 06                     MC    016,0,6        . CLR I/O DATA/DISABLE RTC
 69.          000025  12 11 020                       TC1   A1,020         .
 70.          000026  13 12 000                       TC2   IRD,0          .
 71.          000027  13 15 000                 MCSUB   TC2   XLTR,0       .
 72.          000030  13 03 017                       TC2   CK,15          .
 73.          000031  16 10 002                       RN    2              . REPEAT NEXT 3 INST
 74.          000032  02 15 15 03                     AS2   A5,XLTR,3      . A1 + TRANSLATOR TO A5
 75.          000033  15 15 02 00                     MC    015,2,0        . CHANNEL CONTROL
 76.          000034  00 15 15 02                     T     XLTR,A5,2      .
 77.          000035  13 12 007                       TC2   IRD,7          .
 78.          000036  01 2323                        J     LA8            .
 79.          000037  00 10 13 01                     T     A0,IRS,1       .
 80.                                                  .
 81.                                                  SETADR 040  .
 82.                                                  .
 83.                                                  .
 84.                                                  . FC=04 RR - UNARY-SHIFT
 85.                                                  .
 86.                                                  . M17 UNASSIGNED
 87.          000040  01 0265                 EMF1    J     EMIIL          .
 88.          000041  00 00 00 00                     NOOP                 .
 89.                                                  . M16 UNASSIGNED
 90.          000042  01 0265                        J     EMIIL          .
 91.          000043  00 00 00 00                     NOOP                 .
 92.                                                  . M15 UNASSIGNED
 93.          000044  01 0265                        J     EMIIL          .
 94.          000045  00 00 00 00                     NOOP                 .
 95.                                                  . M14 UNASSIGNED
 96.          000046  01 0265                        J     EMIIL          .
 97.          000047  00 00 00 00                     NOOP                 .
 98.                                                  . M13 UNASSIGNED
 99.          000050  01 0265                        J     EMIIL          .
100.          000051  00 00 00 00                     NOOP                 .
101.                                                  . M12 UNASSIGNED
102.          000052  01 0265                        J     EMIIL          .
103.          000053  00 00 00 00                     NOOP                 .
104.                                                  . M11 UNASSIGNED
105.          000054  01 0265                        J     EMIIL          .
106.          000055  00 00 00 00                     NOOP                 .
107.                                                  . M10 UNASSIGNED
108.          000056  01 0265                        J     EMIIL          .
109.          000057  00 00 00 00                     NOOP                 .
110.                                                  . M7  UNASSIGNED
111.          000060  01 0265                        J     EMIIL          .
112.          000061  00 00 00 00                     NOOP                 .
```

```
                                        • M6  UNASSIGNED
000062  01 0265                            J     EMIIL          •
000063  00 00 00 00                        NOOP                 •
                                        • M5  UNASSIGNED
000064  01 0265                            J     EMIIL          •
000065  00 00 00 00                        NOOP                 •
                                        • M4  UNASSIGNED
000066  01 0265                            J     EMIIL          •
000067  00 00 00 00                        NOOP                 •
                                        • M3  SCALE FACTOR
000070  01 1126                            J     LF7            •
000071  15 07 00 00                        MC    7,0,0          • A+1 TO SGR
                                        • M2  COUNT ONES
000072  01 2100                            J     LJ0            •
000073  13 03 017                         TC2   CK,15          •
                                        • M1  REVERSE REGISTER
000074  01 2261                            J     LI4            •
000075  13 03 017                         TC2   CK,15          •
                                        • M0  SQUARE ROOT
000076  01 0265                            J     EMIIL          •
000077  00 00 00 00                        NOOP                 •
                                    •
                                        SETADR 0100
                                    •
                                    •
                                    • FC=02 RR   UNARY-ARITHMETIC
                                    •
                                        • M17 UNASSIGNED
000100  01 0265                  EMA0      J     EMIIL          •
000101  00 00 00 00                        NOOP                 •
                                        • M16 UNASSIGNED
000102  01 0265                            J     EMIIL          •
000103  00 00 00 00                        NOOP                 •
                                        • M15 UNASSIGNED
000104  01 0265                            J     EMIIL          •
000105  00 00 00 00                        NOOP                 •
                                        • M14 UNASSIGNED
000106  01 0265                            J     EMIIL          •
000107  00 00 00 00                        NOOP                 •
                                        • M13 DECREMENT RA BY 2
000110  01 0475                            J     EMA16          • JUMP
000111  12 16 002                         TC1   A6,2           • +2 TO A6
                                        • M12 INCREMENT RA BY 2
000112  01 0500                            J     EMA18          • JUMP
000113  12 16 002                         TC1   A6,2           • +2 TO A6
                                        • M11 DECREMENT RA BY 1
000114  17 00 00 14                        E     0,0,014            • START
000115  04 04 10 17                      AS1   RGRD,A0,017      • A0 - 1 TO RGR (SS)
                                        • M10 INCREMENT RA BY 1
000116  17 00 00 14                        E     0,0,014            • START
000117  04 04 10 14                      AS1   RGRD,A0,014      • A0 + 1 TO RGR (SS)
                                        • M7  UNASSIGNED
000120  01 0265                            J     EMIIL          •
000121  00 00 00 00                        NOOP                 •
                                        • M6  ONES COMPLEMENT,SINGLE
000122  17 00 00 14                        E     0,0,014            • START
000123  06 04 10 13                      L1    RGRD,A0,013      • 1'S COMP OF A0 TO RGR (SS)
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170•                                          • M5  TWOS COMPLEMENT,DOUBLE
171•   000124  01 1111                             J     LE1              • JUMP
172•   000125  15 07 00 00          LG4            MC    7,0,0            • A+1 TO SGR
173•                                          • M4  TWOS COMPLEMENT,SINGLE
174•   000126  17 00 00 14          LG3            E     0,0,014          • START
175•   000127  05 04 10 14                         SU    RGRD,A0,014      • 0 - A0 TO RGR (SS)
176•                                          • M3  UNASSIGNED
177•   000130  01 0265                             J     EMIIL            •
178•   000131  00 00 00 00                         NOOP                   •
179•                                          • M2  ROUND RA
180•   000132  01 1425                             J     LI0              •
181•   000133  15 07 00 00                         MC    7,0,0            • RA+1 TO SGR
182•                                          • M1  MAKE NEGATIVE
183•   000134  01 0125                             J     LG4              • GO COMPLIMENT
184•   000135  14 00 315                           BN    LG5              • DONE IF RA IS NEG
185•                                          • M0  MAKE POSITIVE
186•   000136  01 0315                             J     LG5              • DONE IF RA IS POS
187•   000137  14 00 126                           BN    LG3              •
188•                                     •
189•                                     • FC=03 RR - UNARY-CONTROL
190•                                     •
191•                                          • M17 DISABLE RTC LOWER OVERFLOW INTERRUPT
192•   000140  17 00 00 14          EMA2           E     0,0,014          • START
193•   000141  15 16 00 01                         MC    016,0,1          • DISABLE RTC INTERRUPT
194•                                          • M16 ENABLE RTC LOWER OVERFLOW INTERRUPT
195•   000142  17 00 00 14          LJ3            E     0,0,014          • START
196•   000143  15 16 00 02                         MC    016,0,2          • ENABLE RTC INTERRUPT
197•                                          • M15 STORE RTC UPPER AND LOWER
198•   000144  01 1117                             J     LC1              •
199•   000145  00 04 04 01                         T     RGRD,RTCU,1      • RTC UPPER TO RA
200•                                          • M14 LOAD RTC UPPER AND LOWER
201•   000146  01 1122                             J     LC2              •
202•   000147  00 04 10 02                         T     RTCU,A0,2        • RA TO RTC UPPER
203•                                          • M13 DISABLE INTERRUPT CLOCK
204•   000150  17 00 00 14                         E     0,0,014          • START
205•   000151  15 16 00 03                         MC    016,0,3          • DISABLE INTERRUPT CLOCK
206•                                          • M12 LOAD AND ENABLE INTERRUPT CLOCK
207•   000152  01 1115                             J     LC4              •
208•   000153  00 00 10 00                         T     D0,A0,0          • RA TO DES BUSS
209•                                          • M11 DISABLE RTC
210•   000154  01 0140                             J     EMA2             •
211•   000155  15 16 00 06                         MC    016,0,6          • DISABLE RTC COUNT
212•                                          • M10 ENABLE RTC
213•   000156  01 0142                             J     LJ3              •
214•   000157  15 16 00 05                         MC    016,0,5          • ENABLE RTC COUNT
215•                                          • M7  LOAD RTC (LOWER)
216•   000160  17 00 00 14                         E     0,0,014          • START
217•   000161  00 07 10 00                         T     RTCL,A0,0        • RA TO RTC LOWER
218•                                          • M6  LOAD STATUS REGISTER 2
219•   000162  17 00 00 14                         E     0,0,014          • START
220•   000163  00 06 10 00                         T     STAT2,A0,0       • RA TO STATUS REG 2
221•                                          • M5  LOAD STATUS REGISTER 1
222•   000164  01 0262                             J     LJ4              •
223•   000165  00 05 10 00                         T     STAT1,A0,0       • RA TO STATUS REG 1
224•                                          • M4  LOAD P
225•   000166  01 1267                             J     LA13             •
226•   000167  00 02 10 00                         T     PREG,A0,0        • RA TO P-REGISTER
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227.                                        . M3  STORE RTC (LOWER)
228.        000170  17 00 00 14                    E     0,0,014          . START
229.        000171  00 04 07 01                    T     RGRD,RTCL,1      . RTC LOWER TO RA
230.                                        . M2  STORE STATUS REGISTER 2
231.        000172  17 00 00 14                    E     0,0,014          . START
232.        000173  00 04 06 01                    T     RGRD,STAT2,1     . STATUS REG 2 TO RA
233.                                        . M1  STORE STATUS REGISTER 1
234.        000174  17 00 00 14                    E     0,0,014          . START
235.        000175  00 04 05 01                    T     RGRD,STAT1,1     . STATUS REG 1 TO RA
236.                                        . M0  EXECUTIVE RETURN
237.        000176  01 2266                        J     LF9              .
238.        000177  00 10 05 01                    T     A0,STAT1,1       . GET STAT1
239.                                    .
240.                                    .
241.                                        SETADR 0200
242.                                    .
243.                                    . INTERRUPT TABLE
244.                                    .
245.                                    . RETURN
246.        000200  15 00 00 00                    MC    0,0,0            . CLEAR RETURN
247.        000201  00 00 15 02                    T     UP,A5,2          . INTERRUPT CODE TO MICRO-P
248.        000202  00 16 16 00                    T     A6,A6,0          . A6 TO A6
249.        000203  000000                         0                      .
250.                                    .
251.                                        SETADR 0204  .
252.                                    .
253.                                    .
254.                                    . BOOTSTRAP LOAD SWITCH FUNCTION
255.                                    .
256.        000204  15 16 00 07                    MC    016,0,7          . CLEAR CLASS I/II INTS
257.        000205  01 0324                        J     EMA1A            .
258.        000206  12 02 002                      TC1   PREG,2           . SETUP BOOTSTRAP LOAD ADDRESS
259.        000207  000000                         0                      .
260.                                    .
261.                                        SETADR 0210  .
262.                                    .
263.                                    .
264.                                    . CHAIN INST READ
265.                                    .
266.        000210  15 15 00 04                    MC    015,0,4          . CLR INT AND CHAIN REQ
267.        000211  01 1637                        J     LA10             . TO CONTINUATION OF SEQ
268.        000212  12 10 300                      TC1   A0,0300          . MASK FOR SET/CLR FLAG INST (73Rx)
269.        000213  000000                         0                      .
270.                                    .
271.                                        SETADR 0214  .
272.                                    .
273.                                    . RUN(BAR)
274.        000214  00 10 03 01         RUNBAR     T     A0,CM,1          . CONSOLE MODE TO A0 (SS)
275.        000215  12 11 017                      TC1   A1,017           . 17 TO A1
276.        000216  01 2153                        J     LF1              . GO TO CONTINUATION OF CONSOLE MODE
277.        000217  07 11 10 06                    L2    A1,A0,6          .
278.                                    .
279.                                        SETADR 022C  .
280.                                    .
281.                                    . CLASS I OR II
282.        000220  00 10 14 11                    T     A0,INTCOD,011    . INT CODE WD TO A0 (SS)
283.        000221  00 10 10 04                    T     A0,A0,4          . ROTATE
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284.   000222  12 12 006                    TC1   A2,6          • MASK FOR INT CODE
285.   000223  14 00 237                    BN    LH1           • JP IF CLASS I
286.   000224  07 12 10 06                  L2    A2,A0,6       • CODE BITS TO A2
287.   000225  10 12 010                    AC    A2,010        • ADD CLASS I BIT ID
288.   000226  01 1565              LH2     J     CISB          • TO COMMON INTERRUPT SEQ
289.   000227  12 17 120                    TC1   A7,0120        • CLASS II MAIN MEMORY LOCATION
290.                                        •
291.                                        SETADR 0230  •
292.                                        •
293.                                    • CLASS III
294.   000230  15 15 00 04                  MC    015,0,4       • CLR INT AND CHAIN REQ
295.   000231  12 10 377                    TC1   A0,0377       • MASK
296.   000232  00 12 15 05                  T     A2,XLTR,5     • INT CODE WD TO A2 W/ROTATE
297.   000233  07 12 10 06                  L2    A2,A0,6       • SAVE I/O INT CODE PORTION ONLY
298.   000234  15 15 00 02                  MC    015,0,2       • CLR INT
299.   000235  01 1566                     J     CISC          • TO COMMON INT SEQ
300.   000236  12 17 110                    TC1   A7,0110       • CLASS III MAIN MEMORY LOCATION
301.   000237  12 13 160             LH1     TC1   A3,0160       • MASK
302.   000240  07 10 13 06                  L2    A0,A3,6       • MEMORY BITS TO A0
303.   000241  00 16 06 01                  T     A6,STAT2,1    • STAT2 TO A6
304.   000242  07 17 16 00                  L2    A7,A6,0       • CLR MEMORY BITS
305.   000243  04 10 17 03                  AS1   A0,A7,3       • INSERT MEMORY BITS
306.   000244  00 12 12 10                  T     A2,A2,010     • CHECK FOR CLASS I POWER FAULT CODE
307.   000245  14 10 251                    BNZ   LH1A          • JP IF NOT PWR INT
308.   000246  00 06 10 00                  T     STAT2,AC,0    • LOAD STAT2
309.   000247  01 1564                     J     CISA          • TO COMMON INTERRUPT SEQ
310.   000250  00 00 00 00                  NOOP                •
311.   000251  00 17 05 01             LH1A    T     A7,STAT1,1    •
312.   000252  12 13 010                    TC1   A3,010        • MASK
313.   000253  07 17 17 16                  L2    A7,A7,016     • CHECK FOR CLASS I LOCKOUT
314.   000254  14 01 335                    BZ    FALTIC        • GO STOP AND ENTER CONSOLE SEQ
315.   000255  00 00 00 00                  NOOP                •
316.   000256  01 1564                     J     CISA          • TO COMMON INT SEQ
317.   000257  00 00 00 00                  NOOP                •
318.                                        •
319.                                    • FC=27 RR,RK - DIVIDE
320.                                        •
321.   000260  01 2217             EMK1    J     EMK1A         •
322.   000261  00 12 10 10                  T     A2,A0,010     • RA TO A2 (SS)
323.   000262  01 0324             LJ4     J     EMA1A         •
324.   000263  15 16 00 00                  MC    016,0,0       • INITIALIZE I/O INTS
325.   000264  00 00 10 02             LM2     T     UP,A0,2       • TO NEW MICRO-P
326.   000265  12 12 000             EMIIL   TC1   A2,0          • CP ILLEGAL INST INT CODE
327.   000266  00 12 13 03             EMIILA  T     IRD,IRS,3     • WAIT FOR POSSIBLE MEMORY REF,CLR NI RESID
328.   000267  00 03 03 00                  T     MDR,MDR,0     • COMPLETE POSSIBLE SPLIT CYCLE
329.   000270  14 16 335                    BCL   FALTIC        • GO STOP AND ENTER CONSOLE SEQ
330.   000271  15 16 10 00                  MC    016,010,0     • SET PROGRAM FAULT
331.   000272  01 1566                     J     CISC          • TO COMMON INT SEQ
332.   000273  12 17 120                    TC1   A7,0120       • CLASS II MAIN MEMORY LOCATION
333.                                        •
334.                                        SETADR 0274 •
335.                                        •
336.                                    • INSTRUCTION READ
337.   000274  00 12 03 02                  T     IRD,MDR,2     • MDR TO IR
338.   000275  17 16 00 05                  E     016,0,5       • BRANCH 1
339.   000276  00 10 10 11                  T     A0,RGRS,011   • RGR TO A0 (SS)
340.   000277  000000                       0                   •
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341.                                                    SETADR 0300  .
342.                                                .
343.                                                . I/O INPUT PASS GT 1
344.                                                .
345.    000300  00 03 16 01                         T     MDR,IDR,1      . INPUT DATA TO MDR
346.    000301  00 00 00 00                 LII0    NOOP                 .
347.    000302  00 00 03 00                         T     D0,MDR,0       .
348.    000303  17 00 10 14                         E     0,010,014      . START,KEEP SGR
349.    000304  00 00 00 00                         NOOP                 .
350.                                                .
351.                                                . FC=27 RI,RX - DIVIDE
352.                                                .
353.    000305  00 12 10 10                 EMK2    T     A2,A0,010      . RA TO A2 (SS)
354.    000306  01 2217                             J     EMK1A          .
355.    000307  00 16 03 00                         T     A6,MDR,0       .
356.                                                .
357.                                                SETADR 0310  .
358.                                                .
359.                                                .
360.                                                . I/O INPUT PASS 1
361.                                                .
362.    000310  00 03 16 01                         T     MDR,IDR,1      . INPUT DATA TO MDR
363.    000311  02 15 00 07                         AS2   A5,UP,7        . MICRO-P-1 TO A5
364.    000312  00 00 03 00                         T     D0,MDR,0       .
365.    000313  17 00 10 14                         E     0,010,014      . START,KEEP SGR
366.    000314  00 00 00 00                         NOOP                 .
367.    000315  00 00 00 00                 LG5     NOOP                 .
368.    000316  17 00 00 14                         E     0,0,014        . START
369.    000317  00 04 10 10                         T     RGRD,A0,010    . TRANSFER RA TO RA SET CONDITION CODE
370.                                                .
371.                                                SETADR 0320  .
372.                                                .
373.                                                .
374.                                                . I/O OUTPUT PASS GT 1
375.                                                .
376.    000320  00 00 00 00                         NOOP                 .
377.    000321  00 00 00 00                         NOOP                 .
378.    000322  00 16 03 02                         T     ODR,MDR,2      . MDR TO OUTPUT DATA
379.    000323  17 00 10 14                         E     0,010,014      . START KEEP SGR
380.    000324  00 00 00 00                 EMA1A   NOOP                 .
381.    000325  17 00 00 14                 EMA1    E     0,0,014        . START
382.    000326  00 00 00 00                         NOOP                 .
383.    000327  000000                              0                    .
384.                                                .
385.                                                SETADR 0330  .
386.                                                .
387.                                                .
388.                                                . I/O OUTPUT PASS 1
389.                                                .
390.    000330  00 00 00 00                         NOOP                 .
391.    000331  02 15 00 07                         AS2   A5,UP,7        . MICRO-P - 1 TO A5
392.    000332  00 16 03 02                         T     ODR,MDR,2      . MDR TO OUTPUT DATA
393.    000333  17 00 10 14                         E     0,010,014      . START KEEP SGR
394.    000334  00 00 00 00                         NOOP                 .
395.    000335  01 0214                    FALTIC  J     RUNBAR         . TO CONSOLE SEQ
396.    000336  15 16 04 00                         MC    016,4,0        . CLR RUN
397.    000337  000000                              0                    .
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398.
399.                                        SETADR 0340 .
400.
401.
402.                                    . INTERIM SEQUENCES
403.                                    .
404.                                    . INDIRECT BYTE MODIFY
405.  000340  00 12 16 00                       T     A2,A6,0          . A6 TO A2
406.  000341  15 07 14 00                       MC    7,014,0          . M+1 TO SGR
407.  000342  01 2760                           J     LA16             . JUMP
408.  000343  04 16 03 03                       ASI   A6,MDR,3         . A2 + MDR TO A6
409.                                    . INDIRECT BYTE NO MOD
410.  000344  00 12 16 00                       T     A2,A6,0          . A6 TO A2
411.  000345  15 07 14 00                       MC    7,014,0          . M+1 TO SGR
412.  000346  01 2760                           J     LA16             . JUMP
413.  000347  00 16 03 00                       T     A6,MDR,0         . MDR TO A6
414.                                    . INDIRECT WORD MODIFY
415.  000350  00 12 16 00                       T     A2,A6,0          . A6 TO A2
416.  000351  15 07 14 00                       MC    7,014,0          . M+1 TO SGR
417.  000352  01 2760                           J     LA16             . JUMP
418.  000353  04 16 03 03                       ASI   A6,MDR,3         . A2 + MDR TO A6
419.                                    . INDIRECT WORD NO MOD
420.  000354  00 12 16 00                       T     A2,A6,0          . A6 TO A2
421.  000355  15 07 14 00                       MC    7,014,0          . M+1 TO SGR
422.  000356  01 2760                           J     LA16             . JUMP
423.  000357  00 16 03 00                       T     A6,MDR,0         . MDR TO A6
424.                                    . NORMAL BYTE MODIFY
425.  000360  03 12 16 14                       S     A2,A6,014        . A6 RS1 TO A2 (SS)
426.  000361  04 16 03 03                       ASI   A6,MDR,3         . A2 + MDR TO A6
427.  000362  17 00 00 07                       E     0,0,7              . BRANCH 2
428.  000363  00 10 10 11                       T     A0,RGRS,011      . RGR TO A0 (SS)
429.                                    . NORMAL BYTE NO MOD
430.  000364  07 12 00 12                       L2    A2,S0,012        . ZERO TO A2 (SS)
431.  000365  00 16 03 00                       T     A6,MDR,0         . MDR TO A6
432.  000366  17 00 00 07              LA1      E     0,0,7              . BRANCH 2
433.  000367  00 10 10 11                       T     A0,RGRS,011      . RGR TO A0 (SS)
434.                                    . NORMAL WORD MODIFY
435.  000370  00 12 16 00                       T     A2,A6,0          . A6 TO A2
436.  000371  04 16 03 03                       ASI   A6,MDR,3         . A2 + MDR TO A6
437.  000372  17 00 00 07                       E     0,0,7              . BRANCH 2
438.  000373  00 10 10 01                       T     A0,RGRS,1        . RGR TO A0
439.                                    . NORMAL WORD NO MOD
440.  000374  00 00 00 00                       NOOP                   .
441.  000375  00 16 03 00                       T     A6,MDR,0         . MDR TO A6
442.  000376  17 00 00 07              LA2      E     0,0,7              . BRANCH 2
443.  000377  00 10 10 01                       T     A0,RGRS,1        . RGR TO A0
444.
445.                                    . FC=02 RI,RX - LOAD DOUBLE
446.                                    .
447.  000400  00 04 03 10              EMA3     T     RGRD,MDR,010     . MDR TO RGR (SS)
448.  000401  00 16 16 00                       T     A6,A6,0          . A6 TO A6
449.  000402  17 00 00 03                       E     0,0,3              . OP-REF, A TO SGR
450.  000403  00 00 00 00                       NOOP                   .
451.                                    .
452.                                    . FC=00 RX - BYTE LOAD
453.                                    . FC=01 RI,RX - LOAD
454.                                    .
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455.          000404  00 04 03 10          EMA4    T    RGRD,MDR,010      • MDR TO RGR (SS)
456.          000405  17 00 00 14                  E    0,0,014             • START
457.                                                •
458.                                                • FC=03 RX - LOAD MULTIPLE
459.                                                • FC=13 RX - STORE MULTIPLE
460.                                                •
461.          000406  C4 16 16 04          LA3     AS1  A6,A6,4           • A6 + 1 TO A6
462.          000407  17 00 00 03                  E    0,0,3               • OP-REF, A TO SGR
463.          000410  00 10 10 01                  T    A0,RGRS,1          • RGR TO A0
464. T        000411  14 12 0006            EMA5    BAM  LA3                • BRANCH A NE M
465.          000412  00 04 03 00                  T    RGRD,MDR,0         • MDR TO RGR
466.          000413  17 00 00 14                  E    0,0,014             • START
467.                                                •
468.                                                • FC=06 RI,RX - LOAD DOUBLE AND INDEX BY 2
469.                                                •
470.          000414  00 13 13 03          EMA6    T    SGR,IRS,3           • M TO SGR
471.          000415  02 04 10 04                  AS2  RGRD,RGRS,4        • RGR + 1 TO RGR
472.          000416  15 07 00 00                  MC   7,0,0               • A+1 TO SGR
473.          000417  00 04 03 10                  T    RGRD,MDR,010       • MDR TO RGR (SS)
474.          000420  00 16 16 00                  T    A6,A6,0            • A6 TO A6
475.          000421  17 00 00 03                  E    0,0,3               • OP-REF
476.                                                •
477.                                                • FC=04 RX - BYTE LOAD AND INDEX BY 1
478.                                                • FC=05 RI,RX - LOAD AND INDEX BY 1
479.                                                •
480.          000422  00 13 13 03          EMA7    T    SGR,IRS,3           • M TO SGR
481.          000423  02 04 10 04                  AS2  RGRD,RGRS,4        • RGR + 1 TO RGR
482.          000424  15 07 04 00                  MC   7,4,0               • A TO SGR
483.          000425  00 04 03 10                  T    RGRD,MDR,010       • MDR TO RGR (SS)
484.          000426  17 00 00 14                  E    0,0,014             • START
485.                                                •
486.                                                • FC=34 RI,RX - COMPARE MASKED
487.                                                •
488.          000427  15 07 00 00          EMA8    MC   7,0,0               • A+1TO SGR
489.          000430  00 11 10 01                  T    A1,RGRS,1          • RGR TO A1
490.          000431  07 10 11 06                  L2   A0,A1,6            • A0•A1 TO A0
491.          000432  07 11 03 06                  L2   A1,MDR,6            • A1•MDR TO A1
492.          000433  05 10 11 10                  SU   A0,A1,010          • A0 - A1 TO A0 (SS)
493.          000434  17 00 00 14                  E    0,0,014             • START
494.          000435  15 05 15 00                  MC   5,015,0             • U CONT CC
495.                                                •
496.                                                • FC=07 RI,RX - LOAD PSW
497.                                                •
498.          000436  00 02 03 00          EMA9    T    PREG,MDR,0          • Y TO PREG
499.          000437  04 16 16 04                  AS1  A6,A6,4            • Y+1 ADDRESS TO BUSS
500.          000440  17 00 00 03                  E    0,0,3               • OP-REF,A TO SGR
501.          000441  00 05 03 00                  T    STAT1,MDR,0        • Y+1 TO STATUS 1
502.          000442  04 16 16 04                  AS1  A6,A6,4            • Y+2 ADDRESS TO BUSS
503.          000443  17 00 00 03                  E    0,0,3               • OP-REF,A TO SGR
504.          000444  15 16 00 10                  MC   016,0,010          • ENABLE PWR INTERRUPTS
505.          000445  00 06 03 00                  T    STAT2,MDR,0        • Y+2 TO STATUS 2
506.          000446  17 00 00 14                  E    0,0,014             • START
507.                                                •
508.                                                • FC=12 RI,RX - STORE DOUBLE
509.                                                •
510.          000447  00 16 16 00          EMA10   T    A6,A6,0             • A6 TO A6
511.          000450  17 00 03 03                  E    0,3,3               • OP-REF, A TO SGR
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512.          000451  00 10 10 01                    T     A0,RGRS,1          • RGR TO A0
513.                                                 •
514.                                                 • FC=10 RX - BYTE STORE
515.                                                 • FC=11 RI,RX - STORE
516.                                                 • FC=17 RI,RX - STORE ZEROS
517.                                                 •
518.          000452  00 00 00 00           EMA11     NOOP               •
519.          000453  17 00 03 14                    E     0,3,014            • START S=3
520.                                                 •
521.                                                 • FC=16 RI,RX - STORE DOUBLE AND INDEX BY 2
522.                                                 •
523.          000454  00 13 13 03           EMA12     T     SGR,IRS,3          • M TO SGR
524.          000455  02 04 10 04                    AS2   RGRD,RGRS,4        • RGR + 1 TO RGR
525.          000456  00 16 16 00                    T     A6,A6,0            • A6 TO A6
526.          000457  17 00 03 03                    E     0,3,3              • OP-REF, A TO SGR
527.          000460  00 10 10 01                    T     A0,RGRS,1          • RGR TO A0
528.                                                 •
529.                                                 • FC=14 RX - BYTE STORE AND INDEX BY 1
530.                                                 • FC=15 RI,RX - STORE AND INDEX BY 1
531.                                                 •
532.          000461  00 13 13 03           EMA13     T     SGR,IRS,3          • M TO SGR
533.          000462  02 04 10 04                    AS2   RGRD,RGRS,4        • RGR + 1 TO RGR
534.          000463  17 00 03 14                    E     0,3,014            • START S=3
535.                                                 •
536.                                                 • FC=21 RR - SUBTRACT DOUBLE
537.                                                 •
538.          000464  15 07 14 00           EMA14     MC    7,014,0            • M+1 TO SGR
539.          000465  00 11 10 01                    T     A1,RGRS,1          • RGR TO A1
540.          000466  15 07 00 00           LD2       MC    7,0,0              • A+1 TO SGR
541.          000467  05 04 11 10                    SU    RGRD,A1,010        • A0 - A1 TO RGR (SS)
542.          000470  15 07 04 00                    MC    7,4,0              • A TO SGR
543.          000471  00 10 10 01                    T     A0,RGRS,1          • RGR TO A0
544.          000472  17 00 10 14                    E     0,010,014          • START
545.          000473  05 04 16 11                    SU    RGRD,A6,011        • A0 - A6 TO RGR (SS)
546.                                                 •
547.                                                 • FC=20 RI,RX - SUBTRACT
548.                                                 •
549.          000474  00 16 03 00           EMA15     T     A6,MDR,0           • MDR TO A6
550.                                                 •
551.                                                 • FC=20 RR,RK - SUBTRACT
552.                                                 •
553.          000475  17 00 00 14           EMA16     E     0,0,014            • START
554.          000476  05 04 16 10                    SU    RGRD,A6,010        • A0 - A6 TO RGR (SS)
555.                                                 •
556.                                                 • FC=22 RI,RX - ADD
557.                                                 •
558.          000477  00 16 03 00           EMA17     T     A6,MDR,0           • MDR TO A6
559.                                                 •
560.                                                 • FC=22 RR,RK - ADD
561.                                                 •
562.          000500  17 00 00 14           EMA18     E     0,0,014            • START
563.          000501  04 04 16 13                    AS1   RGRD,A6,013        • A0 + A6 TO RGR (SS)
564.                                                 •
565.                                                 • FC=21 RI,RX - SUBTRACT DOUBLE
566.                                                 •
567.          000502  05 04 03 10           EMA19     SU    RGRD,MDR,010       • A0 - MDR RGR (SS)
568.          000503  00 16 16 00                    T     A6,A6,0            • A6 TO A6
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569.  000504  17 00 00 03                    E    0,0,3          • OP-REF, A TO SGR
570.  000505  00 10 10 01                    T    A0,RGRS,1      • RGR TO A0
571.  000506  05 04 03 11                    SU   RGRD,MDR,011   • A0 - MDR TO RGR (SS)
572.  000507  17 00 00 14                    E    0,0,014          • START
573.
574.                                         •
575.                                         • FC=23 RR - ADD DOUBLE
576.                                         •
576.  000510  15 07 14 00          EMA20      MC   7,014,0        • M+1 TO SGR
577.  000511  02 14 10 13          LA4        AS2  A4,RGRS,013    • A0 + RGR TO A4 (SS)
578.  000512  15 07 04 00          LD3        MC   7,4,0          • A TO SGR
579.  000513  00 10 10 01                    T    A0,RGRS,1      • RGR TO A0
580.  000514  04 04 16 11                    AS1  RGRD,A6,011    • A0 + A6 TO RGR (SS)
581.  000515  17 00 00 14          LA5        E    0,0,014          • START, A+1 TO SGR
582.  000516  00 04 14 00                    T    RGRD,A4,0      • A4 TO RGR
583.                                         •
584.                                         • FC=23 RI,RX - ADD DOUBLE
585.                                         •
586.  000517  04 04 03 13          EMA21      AS1  RGRD,MDR,013   • A0 + MDR TO RGR (SS)
587.  000520  00 16 16 00                    T    A6,A6,0        • A6 TO A6
588.  000521  17 00 00 03                    E    0,0,3          • OP-REF, A TO SGR
589.  000522  00 10 10 01                    T    A0,RGRS,1      • RGR TO A0
590.  000523  04 04 03 11                    AS1  RGRD,MDR,011   • A0 + MDR TO RGR (SS)
591.  000524  17 00 00 14                    E    0,0,014          • START
592.                                         •
593.                                         • FC=25 RR - COMPARE DOUBLE
594.                                         •
595.  000525  15 07 14 00          EMA22      MC   7,014,0        • M+1 TO SGR
596.  000526  00 14 10 01                    T    A4,RGRS,1      • RGR TO A4
597.  000527  05 10 14 10                    SU   A0,A4,010      • A0 - A4 TO A0 (SS)
598.  000530  15 07 04 00                    MC   7,4,0          • A TO SGR
599.  000531  00 10 10 01                    T    A0,RGRS,1      • RGR TO A0
600.  000532  05 10 16 11                    SU   A0,A6,011      • A0 - A6 TO A0 (SS)
601.  000533  17 00 00 14                    E    0,0,014          • START
602.  000534  15 05 07 00                    MC   5,7,0          • U CONT CC
603.                                         •
604.                                         • FC=24 RI,RX - COMPARE
605.                                         •
606.  000535  00 16 03 00          EMA23      T    A6,MDR,0       • MDR TO A6
607.                                         •
608.                                         • FC=24 RR,RK - COMPARE
609.                                         •
610.  000536  05 10 16 10          EMA24      SU   A0,A6,010      • A0 - A6 TO A0 (SS)
611.  000537  17 00 00 14          LD4        E    0,0,014        • START
612.  000540  15 05 15 00                    MC   5,015,0        • U CONT CC
613.                                         •
614.                                         • FC=25 RI,RX - COMPARE DOUBLE
615.                                         •
616.  000541  05 10 03 10          EMA25      SU   A0,MDR,010     • A0 - MDR TO A0 (SS)
617.  000542  00 16 16 00                    T    A6,A6,0        • A6 TO A6
618.  000543  17 00 00 03                    E    0,0,3            • OP-REF, A TO SGR
619.  000544  00 10 10 01                    T    A0,RGRS,1      • RGR TO A0
620.  000545  05 10 03 11                    SU   A0,MDR,011     • A0 - MDR TO A0 (SS)
621.  000546  17 00 00 14                    E    0,0,014          • START
622.  000547  15 05 07 00                    MC   5,7,0          • U CONT CC
623.                                         •
624.                                         • FC=30 RI,RX - AND
625.                                         •
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626•          000550  00 16 03 00          EMA26    T    A6,MDR,0          • MDR TO A6
627•
628•                                                 • FC=30 RR,RK - AND
629•
630•          000551  17 00 00 14          EMA27    E    0,0,014             • START
631•          000552  07 04 16 16                   L2   RGRD,A6,016         • A0•A6 TO RGR (SS)
632•                                                 • FC=31 RI,RX - OR
633•
634•
635•          000553  00 16 03 00          EMA28    T    A6,MDR,0          • MDR TO A6
636•                                                 • FC=31 RR,RK - OR
637•
638•
639•          000554  17 00 00 14          EMA29    E    0,0,014             • START
640•          000555  06 04 16 14                   L1   RGRD,A6,014         • A0 OR A6 TO RGR (SS)
641•                                                 • FC=32 RI,RX - EXCLUSIVE OR
642•
643•
644•          000556  00 16 03 00          EMA30    T    A6,MDR,0          • MDR TO A6
645•                                                 • FC=32 RR,RK - EXCLUSIVE OR
646•
647•
648•          000557  17 00 00 14          EMA31    E    0,0,014             • START
649•          000560  06 04 16 10                   L1   RGRD,A6,010         • A0 OR A6 TO RGR (SS)
650•                                                 • FC=33 RR,RK - MASKED SUBSTITUTE
651•
652•
653•          000561  15 07 00 00          EMA32    MC   7,0,0               • A+1 TO SGR
654•          000562  00 11 10 01                   T    A1,RGRS,1         • RGR TO A1
655•          000563  06 10 11 02                   L1   A0,A1,2            • A0•COMP A1 TO A0
656•          000564  07 11 16 06                   L2   A1,A6,6            • A6•A1 TO A1
657•          000565  17 00 00 14                   E    0,0,014               • START A TO SGR
658•          000566  06 04 11 14                   L1   RGRD,A1,014        • A0 OR A1 TO RGR (SS)
659•                                                 • FC=33 RI,RX - MASKED SUBSTITUTE
660•
661•
662•          000567  15 07 00 00          EMA33    MC   7,0,0               • A+1 TO SGR
663•          000570  00 11 10 01                   T    A1,RGRS,1         • RGR TO A1
664•          000571  06 10 11 02                   L1   A0,A1,2            • A0• COMP A1 TO A0
665•          000572  07 11 03 06                   L2   A1,MDR,6           • A1•MDR TO A1
666•          000573  17 00 00 14                   E    0,0,014               • START A TO SGR
667•          000574  06 04 11 14                   L1   RGRD,A1,014        • A0 OR A1 TO SGR (SS)
668•                                                 • FC=34 RR,RK - COMPARE MASKED
669•
670•
671•          000575  15 07 00 00          EMA34    MC   7,0,0               • A+1 TO SGR
672•          000576  00 11 10 01                   T    A1,RGRS,1         • RGR TO A1
673•          000577  07 10 11 06                   L2   A0,A1,6            • A0•A1 TO A0
674•          000600  07 11 16 06                   L2   A1,A6,6            • A1•A6 TO A1
675•          000601  05 10 11 10                   SU   A0,A1,010          • A0 - A1 TO A0 (SS)
676•          000602  17 00 00 14                   E    0,0,014               • START
677•          000603  15 05 15 00                   MC   5,015,0           • U CONT CC
678•                                                 • FC=35 RK - EXECUTE REMOTE
679•
680•
681•          000604  00 12 03 02          EMC1     T    IRD,MDR,2         • GET REMOTE INSTRUCTION
682•          000605  04 16 16 04                   ASI  A6,A6,4           • INC A6
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683.            000606  17 16 00 15                     E     016,0,015          • BRANCH 1 WITH INST FROM PREVIOUS ADDRESS
684.            000607  00 10 10 11                     T     A0,RGRS,011        • RA TO A0 (SS)
685.                                                    •
686.                                                    • FC=10 RR,RK - LOGICAL RIGHT SINGLE SHIFT
687.                                                    •
688.            000610  15 10 051             EMA35   MCS   051                • SHIFT RIGHT SP LOGICAL (6-BIT)
689.            000611  17 00 00 14                     E     0,0,014            • START
690.            000612  00 04 06 10                     T     RGRD,SM,010        • RESULT
691.                                                    •
692.                                                    • FC=11 RR,RK - ALGEBRAIC RIGHT SINGLE SHIFT
693.                                                    •
694.            000613  15 10 053             EMA36   MCS   053                • SHIFT RIGHT SP ARITH (6-BIT)
695.            000614  17 00 00 14                     E     0,0,014            • START
696.            000615  00 04 06 10                     T     RGRD,SM,010        • RESULT
697.                                                    •
698.                                                    • FC=15 RR,RK - CIRCULAR LEFT SINGLE SHIFT
699.                                                    •
700.            000616  15 10 044             EMA37   MCS   044                • SHIFT LEFT SP CIR (6-BIT)
701.            000617  17 00 00 14                     E     0,0,014            • START
702.            000620  00 04 06 10                     T     RGRD,SM,010        • RESULT
703.                                                    •
704.                                                    • FC=14 RR,RK - ALGEBRAIC LEFT SINGLE SHIFT
705.                                                    •
706.            000621  15 10 045             EMA38   MCS   045                • SHIFT LEFT SP ARITH (6-BIT)
707.            000622  15 10 047                     MCS   047                • ACCESS BITS SHIFTED OFF
708.            000623  00 04 06 10                     T     RGRD,SM,010        • RETURN LS
709.            000624  00 11 06 00                     T     A1,SM,0            •
710.            000625  12 12 020                      TCI   A2,020             • MASK
711.            000626  00 13 03 04             TA1     T     A3,SHIFTS,4        • SHIFT CT W/ROTATE
712.            000627  07 12 13 16                     L2    A2,A3,016          • AND
713. T          000630  14 10 233                      BNZ   TA2X               • EXECUTE REMOTE OVF BIT SET
714.            000631  17 00 00 14                     E     0,0,014            • START
715.            000632  00 00 00 00                     NOOP                     •
716.            000633  15 05 13 00             TA2X    MC    5,013,0            • SET STATUS BITS
717.                                                    •
718.                                                    • FC=12 RR,RK - LOGICAL RIGHT DOUBLE SHIFT
719.                                                    •
720.            000634  15 07 00 00             EMA39   MC    7,0,0              • A+1 TO SGR
721.            000635  00 11 10 01                     T     A1,RGRS,1          • LS PORTION
722.            000636  15 10 050                      MCS   050                • SHIFT RIGHT DP LS LOGICAL (6-BIT)
723.            000637  01 2407                         J     TA3                • TO RESTORE
724.            000640  15 10 051                      MCS   051                • SHIFT RIGHT DP MS LOGICAL (6-BIT)
725.                                                    •
726.                                                    • FC=13 RR,RK - ALGEBRAIC RIGHT DOUBLE SHIFT
727.                                                    •
728.            000641  15 07 00 00             EMA40   MC    7,0,0              • A+1 TO SGR
729.            000642  00 11 10 01                     T     A1,RGRS,1          • LS PORTION
730.            000643  15 10 052                      MCS   052                • SHIFT RIGHT DP LS ARITH (6-BIT)
731.            000644  01 2407                         J     TA3                • TO RESTORE
732.            000645  15 10 053                      MCS   053                • SHIFT RIGHT DP MS ARITH (6-BIT)
733.                                                    •
734.                                                    • FC=16 RR,RK - ALGEBRAIC LEFT DOUBLE SHIFT
735.                                                    •
736.            000646  01 2414             EMA41   J     EMA41A             •
737.            000647  15 07 00 00                     MC    7,0,0              • A+1 TO SGR
738.                                                    •
739.                                                    • FC=17 RR,RK - CIRCULAR LEFT DOUBLE SHIFT
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740.
741.  000650  15 07 00 0C        EMA42   MC    7,0,0          . A+1 TO SGR
742.  000651  00 11 10 01                T     A1,RGRS,1      . LS PORTION
743.  000652  15 10 040                  MCS   040            . SHIFT LEFT DP LS CIRCULAR (6-BIT)
744.  000653  01 2407                   J     TA3            . TO RESTORE
745.  000654  15 10 041                  MCS   041            . SHIFT LEFT DP MS CIRCULAR (6-BIT)
746.
747.                                    . FC=26 RI,RX - MULTIPLY
748.
749.  000655  00 16 03 00        EMA43   T     A6,MDR,0       .
750.
751.                                    . FC=26 RR,RK - MULTIPLY
752.
753.  000656  00 11 16 10        EMA44   T     A1,A6,C10      . LOAD MULTIPLIER
754.  000657  15 07 00 00                MC    7,0,0          . A+1 TO SGR
755.  000660  00 11 10 01                T     A1,RGRS,1      . LOAD MULTIPLICAND
756.  000661  05 00 11 14                SU    D0,A1,014      . COMP MULTIPLICAND (SS)
757.  000662  13 03 006                  TC2   CK,6           .
758.  000663  16 10 000                  RN    0              . REPEAT NEXT INST 7 TIMES
759.  000664  15 10 0C0                  MCS   0              . SELECT LEAST
760.  000665  01 2334              LA9     J     LA9A           .
761.  000666  00 04 07 10                T     RGRD,PPROD,010 . RETURN LS
762.
763.                                    . FC=05 RR - SET BIT
764.
765.  000667  12 11 0C1        EME1    TC1   A1,1            .
766.  000670  00 16 13 01                T     A6,IRS,1       . SHIFT CT
767.  000671  15 10 002                  MCS   2              . SHIFT LEFT DP LS ARITH (4-BIT)
768.  000672  17 C0 00 14                E     0,0,014        . START
769.  0C0673  06 04 06 14                L1    RGRD,SM,014    . OR IN THE BIT
770.
771.                                    . FC=06 RR - CLEAR BIT
772.
773.  000674  12 11 0C1        EME2    TC1   A1,1
774.  000675  00 16 13 01                T     A6,IRS,1       . SHIFT CT
775.  000676  15 10 002                  MCS   2              . SHIFT LEFT DP LS ARITH (4-BIT)
776.  0C0677  17 00 0C 14                E     0,0,014        . START
777.  0C0700  06 04 06 12                L1    RGRD,SM,012    . CLR THE BIT
778.
779.                                    . FC=07 RR - TEST BIT
780.
781.  0C0701  12 11 0C1        EME3    TC1   A1,1            .
782.  000702  00 16 13 01                T     A6,IRS,1       . SHIFT CT
783.  000703  15 10 0C2                  MCS   2              . SHIFT LEFT DP LS ARITH (4-BIT)
784.  000704  00 00 C0 00                NOOP                 . WAIT
785.  000705  07 10 06 16                L2    A0,SM,016      . AND
786.  0C0706  17 00 0C 14                E     0,0,014        . START
787.  000707  15 05 11 00                MC    5,011,0        . U CONT SP
788.
789.                                    . FC=01 RR,RK - LOAD
790.
791.  000710  17 0C 00 14        EME7    E     0,0,014        . START
792.  0C0711  00 04 16 10                T     RGRD,A6,010    . RM TO RA
793.
794.                                    . FC=35 RI,RX - BIASED FETCH
795.
796.  000712  12 13 300          EMJ2    TC1   A3,0300        . MASK
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797.   000713  00 13 13 04          T     A3,A3,4        . ROTATE
798.   000714  00 10 03 10          T     A0,MDR,C10     . (SS) OF MDR FOR SETTING CONDITION CODE
799.   000715  06 03 03 04          L1    MDR,MDR,4      . SET UPPER 2-BITS AND WRITE
800.   000716  01 1206              J     EMJ1C          .
801.   000717  15 05 11 00          MC        5,011,0    . SET CONDITION CODE
802.                               .
803.                               . FC=35 RR - IO COMMAND
804.                               .
805.   000720  12 17 140     EMJ3   TC1   MAR,0140       .
806.   000721  15 14 1C 00          MC    014,C10,0      . READ SPLIT CYCLE
807.   000722  12 13 300            TC1   A3,0300        . MASK
808.   000723  00 13 13 04          T     A3,A3,4        . ROTATE
809.   000724  00 12 03 02          T     IRD,MDR,2      . SETUP IR W/WORD FROM 140
810.   000725  07 03 03 00          L2    MDR,MDR,0      . CLR UPPER 2-BITS AND WRITE
811.   000726  0C 15 13 03          T     XLTR,IRS,3     .
812.   000727  13 14 007             TC2   XLTRM,7        .
813.   000730  00 00 0C 00          NOOP                 .
814.   000731  12 11 020             TC1   A1,020         . MASK FOR 70RR
815.   000732  12 00 141             TC1   0C,0141        . ADDRESS ON LINE FOR POSSIBLE 2ND WORD
816.   000733  17 C0 00 07          E     0,0,7          . BRANCH 2
817.   000734  00 14 17 01          T     A4,IOCMR,1     . NOOP
818.                               .
819.                               SETADR 0740  .
820.                               .
821.                               .
822.                               . FC=37 RR - CORDIC
823.                               .
824.   000740  01 0265        TP1    J     EMIIL          .
825.   000741  00 C0 0C 00          NOOP                 .
826.   000742  01 0265              J     EMIIL          .
827.   000743  00 C0 0C 00          NOOP                 .
828.   000744  01 0265              J     EMIIL          .
829.   000745  C0 0C C0 00          NOOP                 .
830.   000746  01 0265              J     EMIIL          .
831.   000747  00 00 0C 00          NOOP                 .
832.   000750  01 0265              J     EMIIL          .
833.   000751  00 00 0C 00          NOOP                 .
834.   000752  01 0265              J     EMIIL          .
835.   000753  00 C0 0C 00          NOOP                 .
836.   000754  01 0265              J     EMIIL          .
837.   000755  00 C0 C0 00          NOOP                 .
838.   000756  01 0265              J     EMIIL          .
839.   000757  00 C0 00 00          NOOP                 .
840.   000760  01 3157              J     TP8            . M=7  HYPERBOLIC ROTATE W/POSTSCALE
841.   000761  15 C0 0C 1C          MC    0,0,01C        .
842.   000762  01 3176              J     TP10           . M=6  HYPERBOLIC VECTOR W/POSTSCALE
843.   000763  15 C0 0C 1C          MC    0,0,01C        .
844.   000764  01 3151              J     TP7            . M=5  HYPERBOLIC ROTATE W/O POSTSCALE
845.   000765  15 C0 00 1C          MC    0,0,010        .
846.   000766  01 3170              J     TP9            . M=4  HYPERBOLIC VECTOR W/O POSTSCALE
847.   000767  15 C0 0C 1C          MC    0,0,01C        .
848.   000770  01 3041              J     TP2            . M=3  TRIG ROTATE W/PRESCALE
849.   000771  15 00 0C 1C          MC    0,0,01C        .
850.   000772  01 3102              J     TP5            . M=2  TRIG VECTOR W/PRESCALE
851.   000773  15 00 0C 10          MC    0,0,01C        .
852.   000774  01 3042              J     TP3            . M=1  TRIG ROTATE W/O PRESCALE
853.   000775  15 00 0C 10          MC    0,0,010        .
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854.            000776  01 3103                         J    TP6            . M=0  TRIG VECTOR W/O PRESCALE
855.            000777  15 00 00 10                      MC   0,0,010        .
856.
857.                                                     SETADR 01000  .
858.
859.                                                     .
860.                                                     . FC=55 RI - STORE ADDRESS REGISTER
861.                                                     .
862.            001000  15 00 00 00          EML5       MC   0,0,0          . U CONT PAGE SEL
863.            001001  00 03 04 00                      T    MDR,PTBLS,0    . PAGE TABLE VALUE TO MDR
864.            001002  01 1021  01 1020                 J    LL3            .
865.                                                     .
866.                                                     . FC=55 RX - STORE ADDRESS REGISTER MULTIPLE
867.                                                     .
868.            001003  00 11 10 04  15 00 00 00 EML6    T    A1,A0,4        . ROTATE CT TO A1
869.            001004  15 00 00 00  00 03 04 00         MC   0,0,0          . U CONT PAGE SEL
870.            001005  00 03 04 00  00 11 10 04         T    MDR,PTBLS,0    . PAGE TABLE VALUE TO MDR
871.            001006  12 12 077                       TCI  A2,077         . MASK
872.            001007  07 11 12 16                      L2   A1,A2,016      . SAVE CT (SS)
873.            001010  01 1017                         J    LL2            .
874.            001011  00 00 03 00          LL1        T    D0,MDR,0       . NOOP W/HOLD
875.            001012  15 00 00 00  04 16 16 04        MC   0,0,0          . U CONT PAGE SEL
876.            001013  00 03 04 00  17 00 00 03        T    MDR,PTBLS,0    . PAGE TABLE VALUE TO MDR
877.            001014  04 16 16 04  00 00 00 00        ASI  A6,A6,4        . INC Y ADDRESS
878.            001015  17 00 00 03  15 00 00 00        E    0,0,3          . OP-REF
879.            001016  00 00 00 00  00 03 04 00        NOOP                .
880. T          001017  14 10 011           LL2        BNZ  LL1            . JP IF NOT DONE
881.            001020  04 11 11 17                      ASI  A1,A1,017      . DEC CT (SS)
882.            001021  17 00 03 14          LL3        E    0,3,014        . START W/HOLD
883.                                                     .
884.                                                     . FC=54 RX - LOAD ADDRESS REGISTER MULTIPLE
885.                                                     .
886.            001022  00 11 10 04          EML3       T    A1,A0,4        . ROTATE CT TO A1
887.            001023  12 12 077                       TCI  A2,077         . MASK
888.            001024  01 1032                         J    LL5            .
889.            001025  07 11 12 16                      L2   A1,A2,016      . SAVE CT (SS)
890.            001026  00 10 03 02          LL4        T    PTBLD,MDR,2    . Y TO PAG TABLE R G
891.            001027  04 16 16 04                      ASI  A6,A6,4        . INC Y ADDRESS
892.            001030  17 00 00 03                      E    0,0,3          . OP-REF
893.            001031  00 00 00 00                      NOOP                .
894. T          001032  14 10 026           LL5        BNZ  LL4            . JP IF NOT DONE
895.            001033  04 11 11 17                      ASI  A1,A1,017      . DEC CT (SS)
896.                                                     .
897.                                                     . FC=54 RI - LOAD ADDRESS REGISTER
898.                                                     .
899.            001034  01 0325  01 0324    EML2       J    EMA1           .
900.            001035  00 10 03 02                      T    PTBLD,MDR,2    . MDR TO PAGE TABLS REG
901.                                                     .
902.                                                     . FC=54 RR - LOAD ADDRESS REGISTER
903.                                                     .
904.            001036  01 0325  01 0324    EML1       J    EMA1           .
905.            001037  00 10 16 02                      T    PTBLD,A6,2     . RM TO PAGE TABLE REG
906.                                                     .
907.                                                     SETADR  01040  .
908.                                                     .
909.                                                     .
910.                                                     . FC=70 RR - CHANNEL CONTROL (COMMAND OR CHAINING)
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911.                                                    .
912.                                                    . M17 DISABLE CLASS III,PRIORITY 1 INT UNIQUE
913.          001040  01 2316                    EMH1     J     LA7                 .
914.          001041  C0 10 13 01                         T     AO,IRS,1            .
915.                                                    . M16 ENABLE EI MONITOR ON UNIQUE CHAN
916.          001042  01 2316                           J     LA7                 .
917.          001043  00 10 13 01                      T     AO,IRS,1            .
918.                                                    . M15 DO NOT ACCEPT EI DATA FROM UNIQUE CHAN
919.          001044  01 2316                           J     LA7                 .
920.          001045  C0 10 13 01                      T     AO,IRS,1            .
921.                                                    . M14 ACCEPT EI DATA FROM UNIQUE CHAN
922.          001046  01 2316                           J     LA7                 .
923.          001047  00 10 13 01                      T     AO,IRS,1            .
924.                                                    . M13 UNASSIGNED
925.          001050  01 1654                           J     EMIIIO              .
926.          001051  00 00 00 00                      NOOP                      .
927.                                                    . M12 UNASSIGNED
928.          001052  01 1654                           J     EMIIIO              .
929.          001053  00 00 00 00                      NOOP                      .
930.                                                    . M11 UNASSIGNED
931.          001054  01 1654                           J     EMIIIO              .
932.          001055  00 00 00 00                      NOOP                      .
933.                                                    . M10 MASTER CLEAR UNIQUE CHAN
934.          001056  01 2314                           J     LA6                 .
935.          001057  15 15 02 00                      MC    015,2,0             . CHANNEL CONTROL
936.                                                    . M7  DISABLE CLASS III,PRIORITY 1 INT ALL
937.          001060  01 2323                           J     LA8                 .
938.          001061  C0 10 13 01                      T     AO,IRS,1            .
939.                                                    . M6  ENABLE EI MONITOR ON ALL CHAN
940.          001062  01 2323                           J     LA8                 .
941.          001063  00 10 13 01                      T     AO,IRS,1            .
942.                                                    . M5  DO NOT ACCEPT EI DATA FROM ANY CHAN
943.          001064  01 2323                           J     LA8                 .
944.          001065  00 10 13 01                      T     AO,IRS,1            .
945.                                                    . M4  ACCEPT EI DATA FROM ANY CHAN
946.          001066  01 2323                           J     LA8                 .
947.          001067  00 10 13 01                      T     AO,IRS,1            .
948.                                                    . M3  UNASSIGNED
949.          001070  01 1654                           J     EMIIIO              .
950.          001071  00 00 00 00                      NOOP                      .
951.                                                    . M2  UNASSIGNED
952.          001072  01 1654                           J     EMIIIO              .
953.          001073  00 00 00 00                      NOOP                      .
954.                                                    . M1  UNASSIGNED
955.          001074  01 1654                           J     EMIIIO              .
956.          001075  00 00 00 00                      NOOP                      .
957.                                                    . M0  MASTER CLEAR ALL CHANNELS
958.          001076  01 0027                           J     MCSUB               .
959.          001077  12 11 020                        TC1   A1,020              .
960.                                                    .
961.                                                    . FC=55 RR - STORE ADDRESS REGISTER
962.                                                    .
963.          001100  00 13 13 03              EML4     T     SGR,IRS,3           . POINT RGR TO RM
964.          001101  15 00 00 00                      MC    0,0,0               . U CONT PAGE SEL
965.          001102  CC 04 04 CC                      T     RGRD,PTBLS,C        . PAGE TABLE VALUE TO RM
966.          001103  C1 0325                           J     EMA1                .
967.          001104  C0 00 00 00                      NOOP                      .
```

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 968.
 969.                                                    SETADR 01105 .
 970.
 971.
 972.                                                  . FC=40 RX - CONDITIONAL JUMP
 973.
 974.          001105  00 16 03 00          EMA46      T    A6,MDR,0          . MDR TO A6
 975.
 976.                                                  . FC=40 RR,RK - CONDITIONAL JUMP
 977.
 978.          001106  00 02 16 00          EMA45      T    PREG,A6,0         . A6 TO P
 979.          001107  17 00 04 16                     E    0,4,016           . START JUMP CONDITION
 980.          001110  00 00 00 00                     NOOP                   .
 981.          001111  00 11 10 01          LE1        T    A1,RGRS,1         . RA+1 TO A1
 982.          001112  05 04 11 14                     SU   RGRD,A1,014       . RA+1 COMPLIMENTED
 983.          001113  17 00 00 14                     E    0,0,014           . START
 984.          001114  05 04 10 15                     SU   RGRD,A0,015       . RA COMPLIMENTED (SS)
 985.          001115  15 16 00 04          LC4        MC   016,0,4           . ENABLE INTERRUPT CLOCK(D-BUSS TO CLOCK)
 986.          001116  17 00 00 14                     E    0,0,014           . START
 987.          001117  15 07 00 00          LC1        MC   7,0,0             . A+1 TO SGR
 988.          001120  00 04 07 01                     T    RGRD,RTCL,1       . RTC LOWER TO RA+1
 989.          001121  17 00 00 14                     E    0,0,014           . START
 990.          001122  15 07 00 00          LC2        MC   7,0,0             . A+1 TO SGR
 991.          001123  00 07 10 01                     T    RTCL,RGRS,1       . RA+1 TO RTC LOWER
 992.          001124  17 00 00 14                     E    0,0,014           . START
 993.          001125  15 16 00 05                     MC   016,0,5           . ENABLE RTC COUNT
 994.                                                  . SCALE FACTOR SEQUENCE
 995.          001126  00 11 10 00          LF7        T    A1,A0,0           . MS
 996.          001127  00 11 10 01                     T    A1,RGRS,1         . LS
 997.          001130  15 10 042                      MCS  042               . SHIFT LEFT DP LS ARITH (6-BIT)
 998.          001131  00 00 00 00                     NOOP                   .
 999.          001132  00 16 03 05                     T    A6,SHIFTS,5       . SHIFT CT W/ROTATE
1000.          001133  04 16 16 07                     AS1  A6,A6,7           . DEC A6
1001.          001134  00 00 00 00                     NOOP                   .
1002.          001135  15 10 043                      MCS  043               . SHIFT LEFT DP MS ARITH (6-BIT)
1003.          001136  00 04 06 00                     T    RGRD,SM,0         . RETURN LS
1004.          001137  00 13 06 00                     T    A3,SM,0           . MS
1005.          001140  12 10 037                      TC1  A0,037            . MASK
1006.          001141  15 00 00 10                     MC   0,0,010           . INC SGR TO RA+2
1007.          001142  07 04 16 06          L2         RGRD,A6,6              . COUNT
1008.          001143  17 00 00 14                     E    0,0,014           . START
1009.          001144  00 04 13 00                     T    RGRD,A3,0         . MS
1010.
1011.                                                    SETADR 01145  .
1012.
1013.
1014.                                                  . FC=40 RX - CONDITIONAL JUMP STOP
1015.
1016.          001145  01 1152                        J    LDO               .
1017.
1018.                                                  . FC=40 RR,RK - CONDITIONAL JUMP STOP
1019.
1020.          001146  00 16 13 05                     T    A6,IRS,5          . IR TO A6
1021.          001147  12 12 002                      TC1  A2,2              . MASK
1022.          001150  07 16 16 16                     L2   A6,A6,016         . DETERMINE IF RR OR RK
1023. T        001151  14 01 154                      BZ   LD1               . JP IF RR FORMAT
1024.          001152  15 16 04 00          LDO        MC   016,4,0           . CLR RUN STOP
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1025.          001153  04 C2 02 07                  ASI  PREG,PREG,7        . DEC P
1026.          001154  C4 C2 C2 07        LDI       ASI  PREG,PREG,7        . DEC P
1027.          001155  17 00 00 16                  E    0,0,016            . START JUMP
1028.          001156  C0 C0 00 00                  NOOP                    .
1029.                                               .
1030.                                               . FC=64 RX - BYTE SUBTRACT
1031.                                               .
1032.          001157  01 0475            EME8      J    EMA16              .
1033.          001160  00 16 03 00                  T    A6,MDR,0           .
1034.                                               .
1035.                                               . FC=65 RX - BYTE ADD
1036.                                               .
1037.          001161  01 0500            EME9      J    EMA18              .
1038.          001162  00 16 03 00                  T    A6,MDR,0           .
1039.                                               .
1040.                                               . FC=66 RX - BYTE COMPARE
1041.                                               .
1042.                                               .
1043.                                               . FC=67 RX - BYTE COMPARE AND INDEX BY 1
1044.                                               .
1045.          001163  C0 13 13 03        EME11     T    SGR,IRS,3                . M TO SGR
1046.          001164  02 04 1C C4                  AS2  RGRD,RGRS,4              . RGR + 1 TO RGR
1047.          001165  01 0536            EME10     J    EMA24              .
1048.          001166  00 16 03 00                  T    A6,MDR,0           .
1049.                                               .
1050.                                               . FC=71 RK - INITIATE CHAIN (COMMAND)/LOAD CONTROL MEMORY (CHAINING)
1051.                                               .
1052.          001167  00 17 14 02        EMH3      T    IOCMR,A4,2         . POINTER FROM CHAIN READ
1053.          001170  00 14 13 03                  T    XLTRM,IRS,3        .
1054.          001171  00 17 03 02                  T    IOCMR,MDR,2        .
1055.          001172  01 1232                      J    EMH4A              .
1056.          001173  15 15 01 00                  MC   015,1,0            . CONDITIONALLY SET CHAIN ACTIVE
1057.                                               .
1058.                                               . FC=73 RX - SET/CLEAR FLAG (CHAINING)
1059.                                               .
1060.          001174  00 15 13 01        EMJ1      T    A5,IRS,1           .
1061.          001175  07 11 15 16                  L2   A1,A5,016          . CHECK FOR IR A=1
1062.          001176  00 17 03 00                  T    MAR,MDR,0          .
1063.          001177  15 14 1C 00                  MC   014,01C,0          . READ SPLIT CYCLE
1064.          001200  00 13 1C 04                  T    A3,A0,4            . ROTATE MASK
1065. T        001201  14 1C 2C4                     BNZ  EMJ1A              . JP IF A-FIELD NE ZERO
1066.          001202  01 1205                      J    EMJ1B              .
1067.          001203  C7 03 03 C0                  L2   MDR,MDR,0          . CLR UPPER 2-BITS AND WRITE
1068.          001204  C6 C3 03 04        EMJ1A     L1   MDR,MDR,4          . SET UPPER 2-BITS AND WRITE
1069.          001205  00 17 14 02        EMJ1B     T    IOCMR,A4,2         .
1070.          001206  C0 C0 C0 00        EMJ1C     NOOP                    .
1071.          001207  01 1232                      J    EMH4A              .
1072.          001210  00 00 C0 00                  NOOP                    .
1073.                                               .
1074.                                               . FC=63 RL(RX) - DIVIDE
1075.                                               .
1076.          001211  12 12 017           EMK3      TC1  A2,C17             . MASK
1077.          001212  C0 13 12 01                  T    A3,IRAM,1          .
1078.          001213  01 0260                      J    EMK1               .
1079.          001214  07 16 13 06                  L2   A6,A3,6             . IR M TO A6
1080.                                               .
1081.                                               . FC=56 RI,RX - MULTIPLY,DOUBLE
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1082.
1083.      001215  00 14 03 10          EMD1    T    A4,MDR,010          . Y+1 TO A4 (SS)
1084.      001216  00 16 16 00                  T    A6,A6,0             . MEMORY REF TO BUSS
1085.      001217  17 00 00 03                  E    0,0,3               . OP-REF,A TO SGR
1086.      001220  00 11 10 00                  T    A1,A0,0             . RA+1 TO A1
1087.      001221  00 10 10 01                  T    A0,RGRS,1           . RA TO A0
1088.      001222  01 2117                     J    DPM0                .
1089.      001223  00 16 03 10                  T    A6,MDR,010          . Y TO A6
1090.
1091.                                          . FC=71 RX - LOAD CONTROL MEMORY (COMMAND)/LOAD CONTROL MEMORY (CHAINING)
1092.
1093.      001224  00 17 14 02          EMH4    T    IOCMR,A4,2          . POINTER FROM CHAIN READ
1094.      001225  00 17 03 00                  T    MAR,MDR,0           .
1095.      001226  15 14 00 00                  MC   014,0,0             . READ
1096.      001227  00 14 13 03                  T    XLTRM,IRS,3         .
1097.      001230  01 1232                     J    EMH4A               .
1098.      001231  00 17 03 02                  T    IOCMR,MDR,2         .
1099.      001232  17 00 00 14          EMH4A   E    0,0,014             . START
1100.      001233  00 00 00 00                  NOOP                     .
1101.
1102.                                          . FC=72 RX - STORE CONTROL MEMORY (COMMAND)/STORE CONTROL MEMORY (CHAINING)
1103.
1104.      001234  00 17 14 02          EMH5    T    IOCMR,A4,2          . POINTER FROM CHAIN READ
1105.      001235  00 14 13 03                  T    XLTRM,IRS,3         .
1106.      001236  00 17 03 00                  T    MAR,MDR,0           .
1107.      001237  15 14 02 00                  MC   014,2,0             . WRITE
1108.      001240  00 03 17 01                  T    MDR,IOCMR,1         .
1109.      001241  00 00 00 00                  NOOP                     .
1110.      001242  17 00 03 14                  E    0,3,014             . START W/HOLD
1111.      001243  00 00 00 00                  NOOP                     .
1112.
1113.                                          . FC=57 RR - DOUBLE DIVIDE
1114.
1115.      001244  15 07 14 00          EMK5    MC   7,014,0             . RM+1 TO SGR
1116.      001245  01 2511                     J    DDV0                .
1117.      001246  00 17 10 01                  T    A7,RGRS,1           . LS OF DIVISOR TO A7
1118.
1119.                                          . FC=57 RI,RX - DOUBLE DIVIDE
1120.
1121.      001247  00 17 03 00          EMK4    T    A7,MDR,0            . Y+1 TO A7
1122.      001250  00 16 16 00                  T    A6,A6,0             . MEMORY REF TO BUSS
1123.      001251  17 00 00 03                  E    0,0,3               . OP-REF,A TO SGR
1124.      001252  00 13 10 00                  T    A3,A0,0             . RA+1 TO A3
1125.      001253  01 2513                     J    DDVDA               .
1126.      001254  00 16 03 00                  T    A6,MDR,0            . Y TO A6
1127.
1128.                                          . FC=47 RX - JUMP REGISTER NEGATIVE
1129.
1130. T    001255  14 00 267           EMF2    BN   LA13                . BRANCH NEG
1131.      001256  00 02 03 00                  T    PREG,MDR,0          . MDR TO P
1132.      001257  17 00 00 14          LA12    E    0,0,014                . START
1133.      001260  00 00 00 00                  NOOP                     .
1134.
1135.                                          . FC=44 RR,RK - JUMP REGISTER = 0
1136.
1137. T    001261  14 10 273           EMA48   BNZ  LA14                . BRANCH NE 0
1138.      001262  00 02 16 00                  T    PREG,A6,0           . A6 TO P
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1139.          001263  17 00 00 16                    E    0,0,016          • START JUMP
1140.          001264  00 00 00 00                    NOOP                  •
1141.  ---------------------------------------------------------------------------
1142.                                                 • FC=44 RX - JUMP REGISTER = 0
1143.                                                 •
1144. T        001265  14 10 273           EMA49      BNZ  LA14             • BRANCH NE 0
1145.          001266  00 02 03 00          LD5        T    PREG,MDR,0       • MDR TO P
1146.          001267  17 00 00 16          LA13       E    0,0,016          • START JUMP
1147.          001270  00 00 00 00                     NOOP                  •
1148.                                                 •
1149.                                                 • FC=45 RR,RK - JUMP REGISTER NE 0
1150.                                                 •
1151. T        001271  14 10 267           EMA50      BNZ  LA13             • BRANCH NE 0
1152.          001272  00 02 16 00                    T    PREG,A6,0        • A6 TO P
1153.          001273  17 00 00 14          LA14       E    0,0,014             • START
1154.          001274  00 00 00 00                     NOOP                  •
1155.  ---------------------------------------------------------------------------
1156.                                                 • FC=45 RX -  JUMP REGISTER NE 0
1157.                                                 •
1158. T        001275  14 10 267           EMA51      BNZ  LA13             • BRANCH NE 0
1159.          001276  00 02 03 00                    T    PREG,MDR,0       • MDR TO P
1160.          001277  17 00 00 14                    E    0,0,014             • START
1161.          001300  00 00 00 00                     NOOP                  •
1162.                                                 •
1163.                                                 • FC=46 RR,RK - JUMP REGISTER POSITIVE
1164.                                                 •
1165. T        001301  14 00 273           EMA52      BN   LA14             • BRANCH NEG
1166.          001302  00 02 16 00                    T    PREG,A6,0        • A6 TO P
1167.          001303  17 00 00 16                    E    0,0,016             • START JUMP
1168.          001304  00 00 00 00                     NOOP                  •
1169.  ---------------------------------------------------------------------------
1170.                                                 • FC=46 RX - JUMP REGISTER POSITIVE
1171.  ---------------------------------------------------------------------------
1172. T        001305  14 00 273           EMA53      BN   LA14             • BRANCH NEG
1173.          001306  00 02 03 00                    T    PREG,MDR,0       • MDR TO P
1174.          001307  17 00 00 16                    E    0,0,016             • START JUMP
1175.          001310  00 00 00 00                     NOOP                  •
1176.                                                 •
1177.                                                 • FC=47 RR,RK - JUMP REGISTER NEGATIVE
1178.                                                 •
1179. T        001311  14 00 267           EMA54      BN   LA13             • BRANCH NEG
1180.          001312  00 02 16 00                    T    PREG,A6,0        • A6 TO P
1181.          001313  17 00 00 14                    E    0,0,014             • START
1182.          001314  00 00 00 00                     NOOP                  •
1183.          001315  01 0265              EMIIU      J    EMIIL            •
1184.          001316  00 00 00 00                     NOOP                  •
1185.  ---------------------------------------------------------------------------
1186.                                                 SETADR  01340  •
1187.  ---------------------------------------------------------------------------
1188.                                                 •
1189.                                                 • FC=40 RI - LOCAL JUMP
1190.                                                 •
1191.          001340  04 12 02 07          EMA55      AS1  A2,PREG,7        • P + 1 TO A2
1192.          001341  02 02 12 03                    AS2  PREG,IRAM,3      • A2 + AM TO P
1193.          001342  17 00 00 16                    E    0,0,016             • START JUMP
1194.          001343  00 00 00 00                     NOOP                  •
1195.  ---------------------------------------------------------------------------
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1196.                                          • FC=41 RR,RK - INDEX JUMP
1197.                                          •
1198. T      001344  14 01 257          EMA56   BZ   LA12              • BRANCH ZERO
1199.        001345  00 02 16 00                  T    PREG,A6,0         • A6 TO P
1200.        001346  17 00 00 16                  E    0,0,016             • START JUMP
1201.        001347  04 04 10 07                  AS1  RGRD,A0,7         • A0 - 1 TO RGR
1202.                                          •
1203.                                          • FC=41 RX - INDEX JUMP
1204.                                          •
1205. T      001350  14 01 257          EMA57   BZ   LA12              • BRANCH ZERO
1206.        001351  00 02 03 00                  T    PREG,MDR,0        • MDR TO P
1207.        001352  17 00 00 16                  E    0,0,016             • START JUMP
1208.        001353  04 04 10 07                  AS1  RGRD,A0,7         • A0 - 1 TO RGR
1209.                                          •
1210.                                          • FC=42 RR,RK - JUMP AND LINK REGISTER
1211.                                          •
1212.        001354  00 04 02 00          EMA58   T    RGRD,PREG,0       • P TO RGR
1213.        001355  00 02 16 00                  T    PREG,A6,0         • A6 TO P
1214.        001356  17 00 00 16                  E    0,0,016             • START JUMP
1215.        001357  00 00 00 00                  NOOP                   •
1216.                                          •
1217.                                          • FC=42 RX - JUMP AND LINK REGISTER
1218.                                          •
1219.        001360  00 04 02 00          EMA59   T    RGRD,PREG,0       • P TO RGR
1220.        001361  00 02 03 00                  T    PREG,MDR,0        • MDR TO P
1221.        001362  17 00 00 16                  E    0,0,016             • START JUMP
1222.        001363  00 00 00 00                  NOOP                   •
1223.                                          •
1224.                                          • FC=43 RK - JUMP AND LINK MEMORY
1225.                                          •
1226.        001364  00 03 02 00          EMA60   T    MDR,PREG,0        • P TO MDR
1227.        001365  04 02 16 04                  AS1  PREG,A6,4         • A6 + 1 TO P
1228.        001366  17 00 03 16                  E    0,3,016             • START JUMP
1229.                                          •
1230.                                          • FC=43 RI - LOCAL JUMP AND LINK MEMORY
1231.                                          •
1232.        001367  04 13 02 07          EMA61   AS1  A3,PREG,7          • P - 1 TO A3
1233.        001370  01 1377                    J    LA15               •
1234.        001371  02 17 12 03                  AS2  A7,IRAM,3         • AM + A3 TO A7
1235.                                          •
1236.                                          • FC=41 RI - LOCAL JUMP INDIRECT
1237.                                          •
1238.        001372  04 13 02 07          EMC2    AS1  A3,PREG,7          • P - 1 TO A3
1239.        001373  02 17 12 03                  AS2  MAR,IRAM,3        • A3 + AM TO MAR
1240.        001374  01 1266                    J    LD5                •
1241.        001375  15 14 00 00                  MC   014,0,0            • READ MEMORY
1242.                                          •
1243.                                          • FC=43 RX - JUMP AND LINK MEMORY
1244.                                          •
1245.        001376  00 17 03 00          EMA62   T    A7,MDR,0          • MDR TO A7
1246.        001377  00 03 02 00          LA15    T    MDR,PREG,0        • P TO MDR
1247.        001400  15 14 02 00                  MC   014,2,0            • WRITE
1248.        001401  00 00 00 00                  NOOP                   •
1249.        001402  04 02 17 04                  AS1  PREG,A7,4         • A7 + 1 TO +
1250.        001403  17 00 03 16                  E    0,3,016           • START JUMP
1251.        001404  00 00 00 00                  NOOP                   •
1252.                                          •
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1253•                                   • FC=52 RR - FLOATING POINT MULTIPLY
1254•                                   •
1255•          001405  15 07 14 00       EMG1    MC   7,014,0          • RM+1 TO SGR
1256• U        001406  01 0000                   J    FPML             • JP TO COMMON ROUTINE
1257•          001407  00 17 10 01               T    A7,RGRS,1        • RM+1 TO A7/RM IS IN A6
1258•                                   •
1259•                                   • FC=52 RI,RX - FLOATING POINT MULTIPLY
1260•                                   •
1261•          001410  00 17 03 00       EMG2    T    A7,MDR,0         • 2ND LS-OP TO A7
1262•          001411  00 16 16 00               T    A6,A6,0          • MS OP ADDRESS ON BUSS
1263•          001412  17 00 00 03               E    0,0,3            • OP-REF,A TO SGR
1264• U        001413  01 0000                   J    FPML             • JP TO COMMON ROUTINE
1265•          001414  00 16 03 00               T    A6,MDR,0         • 2ND MS-OP TO A6
1266•                                   •
1267•                                   • FC=53 RR - FLOATING POINT DIVIDE
1268•                                   •
1269•          001415  15 07 14 00       EMG3    MC   7,014,0          • RM+1 TO SGR
1270• U        001416  01 0000                   J    FPDV             • JP TO COMMON ROUTINE
1271•          001417  00 17 10 01               T    A7,RGRS,1        • RM+1 TO A7/RM IS IN A6
1272•                                   •
1273•                                   • FC=53 RI,RX - FLOATING POINT DIVIDE
1274•                                   •
1275•          001420  00 17 03 00       EMG4    T    A7,MDR,0         • 2ND LS-OP TO A7
1276•          001421  00 16 16 00               T    A6,A6,0          • MS OP ADDRESS ON BUSS
1277•          001422  17 00 00 03               E    0,0,3            • OP-REF,A TO SGR
1278• U        001423  01 0000                   J    FPDV             • JP TO COMMON ROUTINE
1279•          001424  00 16 03 00               T    A6,MDR,0         • 2ND MS-OP TO A6
1280•          001425  00 11 10 11       LI0     T    A1,RGRS,011      • DETERMINE RA+1 SIGN (SS)
1281• T        001426  14 00 247                  BN   LI2X             • EXECUTE REMOTE IF RA+1 IS NEG
1282•          001427  17 00 00 14               E    0,0,014          • START
1283•          001430  00 04 10 10               T    RGRD,A0,010      • RA IS NOT CHANGED
1284•                                   •
1285•                                   • FC=51 RR - FLOATING POINT ADD
1286•                                   •
1287•          001431  12 11 000       EMB1    TC1  A1,0             • CLR A1
1288•          001432  15 07 1  00      EMB1A   MC   7,014,0          • RM+1 TO SGR
1289•          001433  00 14 10 01               T    A4,RGRS,1        •
1290•          001434  12 12 177                  TC1  A2,0177          • MASK
1291•          001435  00 12 12 04               T    A2,A2,4          • ROTATE
1292•          001436  15 07 04 00               MC   7,4,0            • A TO SGR
1293•          001437  01 3406                   J    LB2              •
1294•          001440  06 11 16 00               L1   A1,A6,0          • CHANGE SIGN IF FP SUBTRACT
1295•                                   •
1296•                                   • FC=50 RR - FLOATING POINT SUBTRACT
1297•                                   •
1298•          001441  12 11 200       EMB3    TC1  A1,0200          • MASK FOR SIGN BIT
1299•          001442  01 1432                   J    EMB1A            •
1300•          001443  00 11 11 04               T    A1,A1,4          • ROTATE
1301•                                   •
1302•                                   • FC=51 RI,RX - FLOATING POINT ADD
1303•                                   •
1304•          001444  01 3400          EMB2    J    LB1              •
1305•          001445  12 11 000                  TC1  A1,0             • CLR A1
1306•                                   •
1307•                                   • FC=50 RI,RX - FLOATING POINT SUBTRACT
1308•                                   •
1309•          001446  12 11 200       EMB4    TC1  A1,0200          • MASK FOR SIGN BIT
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1310.  001447  01 3400                    J    LB1              .
1311.  001450  00 11 11 04                T    A1,A1,4          . ROTATE
1312.
1313.                                     . FC=56 RR - MULTIPLY,DOUBLE
1314.
1315.  001451  15 07 14 00        EMD2     MC   7,014,0          . RM+1 TO SGR
1316.  001452  00 14 10 11                 T    A4,RGRS,011      . RM+1 TO A4
1317.  001453  15 07 00 00                 MC   7,0,0            . RA+1 TO SGR
1318.  001454  00 16 16 10                 T    A6,A6,010        . RM (SS)
1319.  001455  01 2117                     J    DPM0             .
1320.  001456  00 11 10 01                 T    A1,RGRS,1        .
1321.
1322.                                     . FC=60 RL(RR) - LOGICAL RIGHT SINGLE SHIFT
1323.
1324.  001457  00 16 13 01        EMC3     T    A6,IRS,1         . SHIFT CT
1325.  001460  15 10 011                   MCS  011              . SHIFT RIGHT SP LOGICAL (4-BIT)
1326.  001461  17 00 00 14                 E    0,0,014          . START
1327.  001462  00 04 06 10                 T    RGRD,SM,010      . RESULT
1328.
1329.                                     . FC=60 RL(RI) - ALGEBRAIC RIGHT SINGLE SHIFT
1330.
1331.  001463  00 16 13 01        EMC4     T    A6,IRS,1         . SHIFT CT
1332.  001464  15 10 013                   MCS  013              . SHIFT RIGHT SP ARITH (4-BIT)
1333.  001465  17 00 00 14                 E    0,0,014          . START
1334.  001466  00 04 06 10                 T    RGRD,SM,010      . RESULT
1335.
1336.                                     . FC=60 RL(RK) - LOGICAL RIGHT DOUBLE SHIFT
1337.
1338.  001467  00 16 13 01        EMC5     T    A6,IRS,1         . SHIFT CT
1339.  001470  15 07 00 00                 MC   7,0,0            . A+1 TO SGR
1340.  001471  00 11 10 01                 T    A1,RGRS,1        . LS
1341.  001472  15 10 010                   MCS  010              . SHIFT RIGHT DP LS LOGICAL (4-BIT)
1342.  001473  01 2407                     J    TA3              . TO RESTORE
1343.  001474  15 10 011                   MCS  011              . SHIFT RIGHT DP MS LOGICAL (4-BIT)
1344.
1345.                                     . FC=60 RL(RX) - ALGEBRAIC RIGHT DOUBLE SHIFT
1346.
1347.  001475  00 16 13 01        EMC6     T    A6,IRS,1         . SHIFT CT
1348.  001476  15 07 00 00                 MC   7,0,0            . A+1 TO SGR
1349.  001477  00 11 10 01                 T    A1,RGRS,1        . LS
1350.  001500  15 10 012                   MCS  012              . SHIFT RIGHT DP LS ARITH (4-BIT)
1351.  001501  01 2407                     J    TA3              . TO RESTORE
1352.  001502  15 10 013                   MCS  013              . SHIFT RIGHT DP MS ARITH (4-BIT)
1353.
1354.                                     . FC=61 RL(RR) - ALGEBRAIC LEFT SINGLE SHIFT
1355.
1356.  001503  12 12 017        EMC7     TC1  A2,017           . MASK
1357.  001504  00 13 12 01                 T    A3,IRAM,1        .
1358.  001505  01 0621                     J    EMA38            .
1359.  001506  07 16 13 06                 L2   SHIFTD,A3,6      . IR M TO SHIFT CT
1360.
1361.                                     . FC=61 RL(RI) - CIRCULAR LEFT SINGLE SHIFT
1362.
1363.  001507  00 16 13 01        EMC8     T    A6,IRS,1         . SHIFT CT
1364.  001510  15 10 004                   MCS  4                . SHIFT LEFT SP CIRCULAR (4-BIT)
1365.  001511  17 00 00 14                 E    0,0,014          . START
1366.  001512  00 04 06 10                 T    RGRD,SM,010      . RESULT
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1367.
1368.                                   • FC=61 RL(RK) - ALGEBRAIC LEFT DOUBLE SHIFT
1369.
1370.  001513  12 12 017          EMC9    TC1  A2,017              • MASK
1371.  001514  00 13 12 01                  T    A3,IRAM,1           •
1372.  001515  01 0646                      J    EMA41               •
1373.  001516  07 16 13 06                  L2   SHIFTD,A3,6         • IR M TO SHIFT CT
1374.
1375.                                   • FC=61 RL(RX) - CIRCULAR LEFT DOUBLE SHIFT
1376.
1377.  001517  00 16 13 01          EMC1C   T    A6,IRS,1            • SHIFT CT
1378.  001520  15 07 00 00                  MC   7,0,0               • A+1 TO SGR
1379.  001521  00 11 10 01                  T    A1,RGRS,1           • LS
1380.  001522  15 10 000                    MCS  0                   • SHIFT LEFT DP LS CIRCULAR (4-BIT)
1381.  001523  01 2407                      J    TA3                 • TO RESTORE
1382.  001524  15 10 001                    MCS  1                   • SHIFT LEFT DP MS CIRCULAR (4-BIT)
1383.
1384.                                   • FC=62 RL(RR) - SUBTRACT
1385.
1386.  001525  12 12 017          EMC11   TC1  A2,017              • MASK
1387.  001526  00 13 12 01                  T    A3,IRAM,1           •
1388.  001527  01 0475                      J    EMA16               •
1389.  001530  07 16 13 06                  L2   A6,A3,6             • IR M TO A6
1390.
1391.                                   • FC=62 RL(RI) - SUBTRACT DOUBLE
1392.
1393.  001531  12 11 017          EMC12   TC1  A1,017              • MASK
1394.  001532  00 13 12 01                  T    A3,IRAM,1           •
1395.  001533  07 11 13 06                  L2   A1,A3,6             • IR M TO A1
1396.  001534  01 0466                      J    LD2                 •
1397.  001535  12 16 000                    TC1  A6,0                • CLR A6
1398.
1399.                                   • FC=62 RL(RK) - ADD
1400.
1401.  001536  12 12 017          EMC13   TC1  A2,017              • MASK
1402.  001537  00 13 12 01                  T    A3,IRAM,1           •
1403.  001540  01 0500                      J    EMA18               •
1404.  001541  07 16 13 06                  L2   A6,A3,6             • IR M TO A6
1405.
1406.                                   • FC=62 RL(RX) - ADD DOUBLE
1407.
1408.  001542  12 11 017          EMC14   TC1  A1,017              • MASK
1409.  001543  00 13 12 01                  T    A3,IRAM,1           •
1410.  001544  07 11 13 06                  L2   A1,A3,6             • IR M TO A1
1411.  001545  04 14 11 13                  ASI  A4,A1,013           • RM + RA+1 TO A4
1412.  001546  01 0512                      J    LD3                 •
1413.  001547  12 16 000                    TC1  A6,0                • CLR A6
1414.
1415.                                   • FC=63 RL(RR) - LOAD
1416.
1417.  001550  12 10 017          EME6    TC1  A0,017              • MASK
1418.  001551  00 13 12 01                  T    A3,IRAM,1           •
1419.  001552  17 00 00 14                  E    0,0,014             • START
1420.  001553  07 04 13 16                  L2   RGKD,A3,016        • IR M TO RA, SS
1421.
1422.                                   • FC=63 RL(RI) - COMPARE
1423.
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1424.          001554  12 12 017          EME5    TC1   A2,017            • MASK
1425.          001555  00 13 12 01                T     A3,IRAM,1         •
1426.          001556  01 0536                    J     EMA24             •
1427.          001557  07 16 13 06                L2    A6,A3,6           • IR M TO A6
1428.                                             •
1429.                                             • FC=63 RL(RK) - MULTIPLY
1430.                                             •
1431.          001560  12 12 017          EME4    TC1   A2,017            • MASK
1432.          001561  00 13 12 00                T     A3,IRAM           •
1433.          001562  01 0656                    J     EMA44             •
1434.          001563  07 16 13 06                L2    SHIFTD,A3,6       • IR M TO SHIFT CT
1435.                                             •
1436.                                             • COMMON INTERRUPT SEQ, CODE IN A2, MEM ADDR IN A7
1437.                                             • ENTRY FROM CLASS I OPERATION - UNIQUE
1438.          001564  12 17 130          CISA    TC1   A7,0130           • CLASS I MAIN MEMORY LOCATION
1439.                                             • ENTRY FROM CLASS II OPERATION - UNIQUE
1440.          001565  15 16 00 07        CIS8    MC    016,0,7           • CLEAR CLASS I/II INTERRUPTS
1441.                                             • ENTRY FROM CLASS III OPERATION OR PROGRAMMED TYPE OPERATION
1442.          001566  00 03 02 00        CISC    T     MDR,PREG,0        • P TO MDR
1443.          001567  15 14 02 00                MC    014,2,0           • WRITE P TO MEM
1444.          001570  00 10 07 01                T     A0,RTCL,1         • SAVE
1445.          001571  00 11 04 01                T     A1,RTCU,1         • SAVE
1446.          001572  00 00 03 00                T     D0,MDR,0          • NOOP W/HOLD FOR MEM
1447.          001573  04 17 17 04                ASI   A7,A7,4           • INC MEM ADDRESS
1448.          001574  00 03 05 01                T     MDR,STAT1,1       • STAT1 TO MDR
1449.          001575  15 14 02 00                MC    014,2,0           • WRITE STAT1 TO MEM
1450.          001576  17 00 03 00                E     0,3,0             • ALLOW I/O W/HOLD
1451.          001577  00 00 00 00                NOOP                    •
1452.          001600  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1453.          001601  00 03 06 01                T     MDR,STAT2,1       • STAT2 TO MDR
1454.          001602  15 14 02 00                MC    014,2,0           • WRITE STAT2 TO MEM
1455.          001603  00 00 03 00                T     D0,MDR,0          • NOOP W/HOLD FOR MEM
1456.          001604  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1457.          001605  00 03 10 00                T     MDR,A0,0          • RTCL TO MDR
1458.          001606  15 14 02 00                MC    014,2,0           • WRITE RTCL TO MEMORY
1459.          001607  17 00 03 00                E     0,3,0             • ALLOW I/O W/HOLD
1460.          001610  00 00 00 00                NOOP                    •
1461.          001611  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1462.          001612  15 14 00 00                MC    014,0,0           • READ P FROM MEMORY
1463.          001613  04 02 03 03                ASI   PREG,MDR,3        • INT CODE + MEMORY P TO P-REG
1464.          001614  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1465.          001615  15 14 00 00                MC    014,0,0           • READ STAT1 FROM MEMORY
1466.          001616  00 05 03 00                T     STAT1,MDR,0       • SETUP STAT1
1467.          001617  17 00 03 00                E     0,3,0             • ALLOW I/O W/HOLD
1468.          001620  00 00 00 00                NOOP                    •
1469.          001621  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1470.          001622  15 14 00 00                MC    014,0,0           • READ STAT2 FROM MEMORY
1471.          001623  00 06 03 00                T     STAT2,MDR,0       • SETUP STAT2
1472.          001624  04 17 17 04                ASI   A7,A7,4           • INC MEMORY ADDRESS
1473.          001625  00 03 11 00                T     MDR,A1,0          • RTCU TO MDR
1474.          001626  01 2215                    J     LA111             •
1475.          001627  15 14 02 00                MC    014,2,0           • WRITE RTCU TO MEMORY
1476.                                             •
1477.                                             • FC=74 RK - CONDITIONAL JUMP
1478.                                             •
1479. T        001630  14 13 233          EMF3    BS    EMF3A             •
1480.          001631  00 17 14 02                T     IOCMR,A14,2       •
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1481.  001632  00 17 03 02                    T     IOCMR,MDR,2          .
1482.  001633  17 00 03 14          EMF3A     E     0,3,014              . START W/HOLD
1483.  001634  00 00 00 00                    NOOP                       .
1484.                                         .
1485.                                         . FC=73 RR - HALT/INTERRUPT (CHAINING)
1486.                                         .
1487.  001635  01 1232              EMJ4      J     EMH4A                .
1488.  001636  15 15 00 10                    MC    015,0,010            . HALT/INTERRUPT
1489.  001637  00 17 17 01          LA10      T     MAR,IOCMR,1          . POINTER ADDRESS
1490.  001640  15 14 00 00                    MC    014,0,0              . READ I/O INST FROM MAIN MEMORY
1491.  001641  04 16 17 04                    AS1   A6,A7,4              . POINTER ADDRESS + 1 TO A6
1492.  001642  04 14 16 04                    AS1   A4,A6,4              . POINTER ADDRESS + 2 TO A4
1493.  001643  00 12 03 02                    T     IRD,MDR,2            . I/O INST TO IR
1494.  001644  00 17 16 02                    T     IOCMR,A6,2           . RELOAD UPDATED POINTER
1495.  001645  17 00 00 07                    E     0,0,7                . BRANCH 2
1496.  001646  12 11 020                     TC1   A1,020               . MASK FOR SET/CLR AND 70RR
1497.  001647  04 04 10 14          L12X      AS1   RGRD,A0,014          . INC RA (SS)
1498.                                         .
1499.                                         . FC=44-47 R1 - LOCAL JUMP
1500.                                         .
1501.  001650  04 12 02 07          EMA47     AS1   A2,PREG,7            . P - 1 TO A2
1502.  001651  02 02 12 03                    AS2   PREG,IRAM,3          . A2 + AM TO P
1503.  001652  17 00 04 16                    E     0,4,016              . START JUMP CONDITION
1504.  001653  00 00 00 00                    NOOP                       .
1505.  001654  01 0266              EMIIIO    J     EMIILA               .
1506.  001655  12 12 002                     TC1   A2,2                 . I/O ILLEGAL INST INT CODE
1507.                                         .
1508.                                         . FC=70 RX - INITIATE TRANSFER (CHAINING)
1509.                                         .
1510.  001656  00 17 03 00          EMH2      T     MAR,MDR,0            . ADDRESS
1511.  001657  15 14 00 00                    MC    014,0,0              . READ
1512.  001660  15 15 04 00                    MC    015,4,0              . INIT TRANSFER
1513.  001661  00 17 14 02                    T     IOCMR,A4,2           .
1514.  001662  13 14 000                     TC2   XLTRM,0              . POINTER
1515.  001663  00 17 03 02                    T     IOCMR,MDR,2          . BCW1
1516.  001664  04 17 17 04                    AS1   MAR,MAR,4            . INC ADDRESS
1517.  001665  15 14 00 00                    MC    014,0,0              . READ
1518.  001666  13 14 001                     TC2   XLTRM,1              .
1519.  001667  01 1232                      J     EMH4A                .
1520.  001670  00 17 03 02                    T     IOCMR,MDR,2          . BCW2
1521.                                         .
1522.                                         . FC=75 RR - SEARCH FOR SYNC
1523.                                         .
1524.  001671  00 14 13 03          EMD4      T     XLTRM,IRS,3          .
1525.  001672  01 1674                      J     EMD4A                .
1526.  001673  15 16 01 00                    MC    016,1,0              . SFS
1527.  001674  17 00 00 14          EMD4A     E     0,0,014              . START
1528.  001675  00 00 00 00                    NOOP                       .
1529.                                         .
1530.                                         . FC=76 RR - SET/CLEAR DISCRETE
1531.                                         .
1532.  001676  00 14 13 03          EMD3      T     XLTRM,IRS,3          .
1533.  001677  01 1701                      J     EMD3A                .
1534.  001700  15 16 02 00                    MC    016,2,0              . SET/CLR DISCRETE
1535.  001701  17 00 00 14          EMD3A     E     0,0,014              . START
1536.  001702  00 00 00 00                    NOOP                       .
1537.                                         .
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1538.                                          • FC=76 RX - STORE STATUS
1539.                                          •
1540.    001703  15 15 CC 01          EMD5     MC   015,0,1          • ENABLE OUT/READ STATUS
1541.    001704  00 17 03 00                    T    MAR,MDR,0        •
1542.    001705  15 14 02 00                    MC   014,2,0          • WRITE
1543.    001706  00 03 16 01                    T    MDR,IDR,1        •
1544.    001707  CC 17 14 02                    T    IOCMR,A4,2       •
1545.    001710  17 00 03 14                    E    0,3,014          • START W/HOLD
1546.    001711  00 00 00 00                    NOOP                  •
1547.                                          •
1548.                                          SETADR 02000    •
1549.                                          •
1550.                                          •
1551.                                          • JP LIST FOR CONSOLE MODE SEQUENCE
1552.                                          •
1553.    002000  01 2432              LN0      J    LNSUB            • TO DISPLAY MOD SUB
1554.    002001  00 14 02 00                    T    A4,PREG,0        • GET REGISTER DATA
1555.    002002  01 0324                        J    EMA1A            •
1556.    002003  00 02 14 00                    T    PREG,A4,0        • UPDATE REGISTER DATA
1557.    002004  01 2432              LN1      J    LNSUB            • STATUS REGISTER 1
1558.    002005  00 14 05 01                    T    A4,STAT1,1       •
1559.    002006  01 0325                        J    EMA1             •
1560.    002007  00 05 14 00                    T    STAT1,A4,0       •
1561.    002010  01 2432              LN2      J    LNSUB            • STATUS REGISTER 2
1562.    002011  00 14 06 01                    T    A4,STAT2,1       •
1563.    002012  01 0325                        J    EMA1             •
1564.    002013  00 06 14 00                    T    STAT2,A4,0       •
1565.    002014  01 2432              LN3      J    LNSUB            • RTC LOWER
1566.    002015  00 14 07 01                    T    A4,RTCL,1        •
1567.    002016  01 0325                        J    EMA1             •
1568.    002017  00 07 14 00                    T    RTCL,A4,0        •
1569.    002020  01 2432              LN4      J    LNSUB            • RTC UPPER
1570.    002021  00 14 04 01                    T    A4,RTCU,1        •
1571.    002022  01 0325                        J    EMA1             •
1572.    002023  00 04 14 02                    T    RTCU,A4,2        •
1573.    002024  01 2432              LN5      J    LNSUB            • BREAKPOINT
1574.    002025  00 14 01 00                    T    A4,BRKPT,0       •
1575.    002026  01 0324                        J    EMA1A            •
1576.    002027  00 01 14 00                    T    BRKPT,A4,0       •
1577.    002030  00 15 13 03              LN6      T    XLTR,IRS,3       • IOCMR (SETUP POINTER)
1578.    002031  01 2204                        J    LF5              •
1579.    002032  00 00 00 00                    NOOP                  •
1580.    002033  000000                        0                     •
1581.    002034  01 2400              LN7      J    LM3              • PAGE ADDRESS REGISTER
1582.    002035  00 10 13 01                    T    PAC,IRS,1        •
1583.    002036  000000                        0                     •
1584.    002037  000000                        0                     •
1585.    002040  00 17 02 00              LN10     T    MAR,PREG,0       • MAIN MEMORY DISPLAY
1586.    002041  01 2211                        J    LF6              •
1587.    002042  15 14 00 00                    MC   014,0,0          • INITIATE MEMORY READ
1588.    002043  000000                        0                     •
1589.    002044  00 15 13 03              LN11     T    XLTR,IRS,3       • OUTPUT REGISTER (SELECT CHANNEL)
1590.    002045  15 15 CC 01                    MC   015,0,1          • ENABLE OUTPUT DATA SELECT
1591.    002046  01 2107                        J    LN11A            •
1592.    002047  00 00 00 00                    NOOP                  •
1593.    002050  15 10 00 04              LN12     MC   010,0,4          • MONITOR CLOCK (ENABLE MONITOR CLOCK SOURCE)
1594.    002051  01 2113                        J    LN12A            •
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1595.          002052  00 0C 00 00                NOOP                 .
1596.          002053  000000                     0                    .
1597.          002054  01 0325            LN13    J    EMA1            . UNASSIGNED
1598.          002055  00 00 00 C0                NOOP                 .
1599.          002056  000000                     0                    .
1600.          002057  000C00                     0                    .
1601.          002060  01 0325            LN14    J    EMA1            . UNASSIGNED
1602.          002061  00 00 00 00                NOOP                 .
1603.          002062  000000                     0                    .
1604.          002063  000000                     0                    .
1605.          002064  01 0325            LN15    J    EMA1            . UNASSIGNED
1606.          002065  00 00 00 00                NOOP                 .
1607.          002066  000000                     0                    .
1608.          002067  000000                     0                    .
1609.          002070  01 0325            LN16    J    EMA1            . UNASSIGNED
1610.          002071  00 0C 00 C0                NOOP                 .
1611.          002072  000000                     0                    .
1612.          002073  000000                     0                    .
1613.          002074  01 2432            LN17    J    LNSUB           . MICRO JUMP SWITCH
1614.          002075  00 14 02 01                T    A4,DREG,1       .
1615.          002076  01 0324                    J    EMA1A           .
1616.          002077  14 17 264                  BMJS LM2             . JP IF SW SELECTED
1617.          002100  12 11 000           LJ0     TCI  A1,0            . CLR A1
1618.          002101  16 10 001                  RN   1               . REPEAT NEXT 2 INST 16 TIMES
1619.          002102  04 10 10 13                ASI  A0,A0,C13       .
1620.          002103  04 11 00 01                ASI  A1,S0,1         . ADD CARRY
1621.          002104  15 00 00 10                MC   0,0,010         . INC SGR TO RA+1
1622.          002105  17 00 10 14  01 0325       E    0,010,C14       . START A/HOLD
1623.          002106  00 04 11 00                T    RGRD,A1,0       . COUNT
1624.          002107  01 2432            LN11A   J    LNSUB           .
1625.          002110  00 14 16 01                T    A4,IDR,1        .
1626.          002111  01 0325                    J    EMA1            .
1627.          002112  00 00 00 00                NOOP                 .
1628.          002113  01 2432            LN12A   J    LNSUB           .
1629.          002114  00 14 07 00                T    A4,MONCLK       .
               002115  01 0325                    J    EMA1            .
1631.          002116  00 00 00 00                NOOP                 .
1632.                                              .
1633.                                              . PART OF DOUBLE MULTIPLY SEQUENCE
1634.                                              .
1635.          002117  12 12 000           DPM0    TCI  A2,0            . CLR FOR USE IN MULTIPLY
1636. T        002120  14 06 150                  BDZ  DPM2            . JP IF MULTIPLICAND = 0
1637.          002121  12 13 000                  TCI  A3,0            . CLR FOR USE IN MULTIPLY
1638.          002122  17 00 10 00                E    0,010,0         . ALLOW I/O
1639.          002123  15 10 031                  MCS  031             . U CONT INITIALIZE (SEL R2)
1640.          002124  16 02 037                  MD   037             . DOUBLE MULTIPLY REPEAT
1641.          002125  04 13 14 10                ASI  A3,A4,C10       . A3 + A4 TO A3,LS HALF (SS)
1642.          002126  04 12 16 11                ASI  A2,A6,C11       . A2 + A6 TO A2,MS HALF (SS)
1643.          002127  10 13 000                  AC   A3,0            . END CORRECTION FOR DOUBLE LENGTH
1644.          002130  17 00 00 10                E    0,0,010         . RESTART,A TO SGR
1645.          002131  00 04 12 00           DPM1    T    RGRD,A2,0       . A2 TO RA
1646.          002132  15 00 00 10                MC   0,0,010         . INC SGR TO RA+1
1647.          002133  00 04 13 00                T    RGRD,A3,0       . A3 TO RA+1
1648.          002134  15 00 00 10                MC   0,0,010         . INC SGR TO RA+2
1649. T        002135  14 06 145                  BDZ  DPM1B           .
1650.          002136  15 10 030                  MCS  030             . SELECT R1
1651.          002137  00 14 06 00                T    A4,SM,0         .
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1652.          002140  00 04 06 00          T     RGRD,SM,0      . TO RA+2
1653.          002141  15 00 00 10  DPM1A   MC    0,0,010        . INC SGR TO RA+3
1654.          002142  00 04 14 00          T     RGRD,A4,0      . A4 TO RA+3
1655.          002143  17 00 10 14          E     0,010,014      . START HOLD SGR
1656.          002144  15 05 01 00          MC    5,1,0          . SET U CONT CC (DP NORM)
1657.          002145  00 14 06 10  DPM1B   T     A4,SM,010      .
1658.          002146  01 2141              J     DPM1A          .
1659.          002147  00 04 06 10          T     RGRD,SM,010    . TO RA+2
1660.          002150  07 10 00 02  DPM2    L2    A0,S0,2        . CLR A0
1661.          002151  01 2131              J     DPM1           .
1662.          002152  07 11 00 02          L2    A1,S0,2        . CLR A1
1663.                                       .
1664.                                       . CONSOLE MODE SEQUENCE
1665.                                       .
1666.          002153  12 12 020   LF1     TC1   A2,020         . MASK
1667.          002154  07 12 10 06          L2    A2,A0,6        . MASK ALTER MODE BIT
1668.          002155  00 15 12 00          T     A5,A2,0        . SAVE IN A5
1669.          002156  12 12 100           TC1   A2,0100        . MASK.
1670.          002157  07 12 10 16          L2    A2,A0,016      . SS OF BIT-6 (GENERAL REG)
1671.          002160  12 12 200           TC1   A2,0200        . MASK
1672. T        002161  14 10 200           BNZ   LF4            . GO TO GENERAL REG SEQ
1673.          002162  00 13 11 02          T     SGR,A1,2       . A1 TO SGR FOR GENERAL REG SEQ
1674.          002163  07 12 10 16          L2    A2,A0,016      . SS OF BIT-7 (INST REG)
1675. T        002164  14 10 174           BNZ   LF3            . GO TO INST REG SEQ
1676.          002165  12 10 001           TC1   A0,1           . K FOR GENERAL DISPLAY SEQ
1677.          002166  00 10 10 04          T     A0,A0,4        . ROTATE FOR K OF 400
1678.          002167  06 10 11 04          L1    A0,A1,4        . CREATE RELATIVE JUMP ADDRESS
1679.          002170  03 10 10 00          S     A0,A0,0        . CREATE JP ADDRESS MOD 4 STARTING AT 2000
1680.          002171  03 10 10 00          S     A0,A0,0        .
1681.          002172  00 00 10 02          T     UP,A0,2        . GO TO PROPER AREA
1682.          002173  00 00 00 00          NOOP
1683.          002174  01 2432      LF3     J     LNSUB          . INSTRUCTION REGISTER
1684.          002175  00 14 13 01          T     A4,IRS,1       .
1685.          002176  01 0325              J     EMA1           .
1686.          002177  00 12 14 02          T     IRD,A4,2       .
1687.          002200  01 2432      LF4     J     LNSUB          . GENERAL REGISTERS
1688.          002201  00 14 10 01          T     A4,RGRS,1      .
1689.          002202  01 0325              J     EMA1           .
1690.          002203  00 04 14 00          T     RGRD,A4,0      .
1691.          002204  01 2432      LF5     J     LNSUB          .
1692.          002205  00 14 17 01          T     A4,IOCMR,1     .
1693.          002206  00 17 14 02          T     IOCMR,A4,2     .
1694.          002207  17 00 00 14          E     0,0,014        . START OR GO TO RUN SEQ
1695.          002210  00 00 00 00          NOOP                 .
1696.          002211  01 2432      LF6     J     LNSUB          .
1697.          002212  00 14 03 00          T     A4,MDR,0       .
1698.          002213  00 03 14 00          T     MDR,A4,0       .
1699.          002214  15 14 02 00          MC    014,2,0        . INITIATE MEMORY WRITE
1700.          002215  17 00 03 14  LAI11   E     0,3,014        . START/WAIT FOR MEMORY
1701.          002216  00 00 00 00          NOOP                 .
1702.          002217  15 10 031   EMK1A   MCS   031            . U CONT SHIFT INITIALIZE
1703.          002220  15 07 00 00          MC    7,U,0          . RA+1 TO SGR
1704.          002221  00 10 10 01          T     A0,RGRS,1      . RA+1 TO A0 (R1)
1705. T        002222  14 00 241           BN    LDV2           . JP IF RA IS NEG
1706.          002223  00 16 16 10          T     A6,A6,010      . A6 TO A6 (SS)
1707. T        002224  14 00 233           BN    LDV1           . JP IF Y IS NEG
1708.          002225  03 10 10 10          S     A0,A0,010      . SHIFT A0 L (RA+1)
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NOOP →

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1709•          002226  01 2276                        J     LDV4      • TO DIV/SUB SEQ
1710•          002227  03 12 12 02                    S     A2,A2,2   • SHIFT A2 L (RA)
1711• T        002230  14 00 311                     BN    LDV7X     • EXECUTE REMOTE IF OVERFLOW
1712•          002231  01 2237                        J     LDV1A     • GO STORE REM
1713•          002232  00 00 00 00                    NOOP            •
1714•          002233  01 2275              LDV1      J     LDV3      • TO DIV/SUB SEQ
1715•          002234  05 16 16 04                    SU    A6,A6,4   • COMP A6 (Y)
1716• T        002235  14 00 310                     BN    LDV6      • JP IF OVF
1717•          002236  05 04 06 14                    SU    RGRD,SM,014 • COMP QUOT (SS)
1718•          002237  17 00 00 14              LDV1A     E     0,0,014   • START
1719•          002240  00 04 12 00                    T     RGRD,A2,0 • RA RESULT (REMAINDER)
1720• T        002241  14 00 252              LDV2      BN    LDV2B     • JP IF Y AND RA NEG
1721•          002242  05 10 10 14                    SU    A0,A0,014 • COMP A0 (SS) (RA+1)
1722•          002243  05 12 12 05                    SU    A2,A2,5   • COMP A2 (RA)
1723•          002244  01 2275                        J     LDV3      • TO DIV/SUB SEQ
1724•          002245  03 10 10 10                    S     A0,A0,010 • SHIFT A0 L (SS) (RA+1) (QUOTIENT)
1725• T        002246  14 00 312                     BN    LDV8      • JP IF OVF
1726•          002247  05 04 06 14                    SU    RGRD,SM,014 • COMP QOUT (SS)
1727•          002250  17 00 00 14              LDV2A     E     0,0,014   • START
1728•          002251  05 04 12 04                    SU    RGRD,A2,4 • COMP REMAINDER
1729•          002252  05 12 12 05              LDV2B     SU    A2,A2,5   • COMP A2 (RA)
1730•          002253  05 16 16 04                    SU    A6,A6,4   • COMP A6 (Y)
1731•          002254  01 2275                        J     LDV3      • TO DIV/SUB SEQ
1732•          002255  03 10 10 10                    S     A0,A0,010 • SHIFT A0 L (SS) RA+1)(QUOTIENT)
1733• T        002256  14 00 311                     BN    LDV7X     • EXECUTE REMOTE IF OVERFLOW
1734•          002257  01 2250                        J     LDV2A     •
1735•          002260  00 00 00 00                    NOOP            •
1736•          002261  16 10 001              LI4       RN    1         • REPEAT NEXT 2 INST 16 TIMES
1737•          002262  03 10 10 10                    S     A0,A0,010 • SHIFT LEFT (SS)
1738•          002263  03 11 11 06                    S     A1,A1,6   • SHIFT RIGHT,INSERT BIT SAVED
1739•          002264  17 00 00 14                    E     0,0,014   • START
1740•          002265  00 04 11 10                    T     RGRD,A1,010 • RETURN REVERSED DATA
1741•          002266  00 04 02 00              LF9       T     RGRD,PREG,0 • P TO RA
1742• T        002267  14 16 273                     BCL   LF10      • JP IF CLASS II LOCKED OUT
1743•          002270  12 12 006                     TC1   A2,6       • INT CODE
1744•          002271  01 1565                        J     CISB      •
1745•          002272  12 17 120                     TC1   A7,0120   • CLASS II MAIN MEMORY LOCATION
1746•          002273  01 0214              LF10      J     RUNBAR    •
1747•          002274  15 16 04 00                    MC    016,4,0   • CLEAR RUN
1748•          002275  03 12 12 02              LDV3      S     A2,A2,2   • SHIFT A2 L (RA)
1749•          002276  02 15 00 04              LDV4      AS2   A5,UP,4   • MICRO-P TO A5
1750•          002277  16 01 016                        DS    016       • REPEAT DIV
1751•          002300  05 12 16 10                    SU    A2,A6,010 •
1752•          002301  04 12 16 03                    ASI   A2,A6,3   • A2 + A6 TO A2
1753• T        002302  14 00 306                     BN    LDV5      • JP IF NEG
1754•          002303  00 04 06 10                    T     RGRD,SM,010 • QUOT TO RGR (SS) (RA+1)
1755•          002304  00 00 15 02                    T     UP,A5,2   • RETURN
1756•          002305  05 12 16 00                    SU    A2,A6,0   • A2 - A6 TO A2
1757•          002306  00 00 15 02              LDV5      T     UP,A5,2   • RETURN
1758•          002307  00 00 00 00                    NOOP            •
1759•          002310  01 2237              LDV6      J     LDV1A     •
1760•          002311  15 05 02 10              LDV7X     MC    5,2,010   • SET OVF
1761•          002312  01 2250              LDV8      J     LDV2A     •
1762•          002313  15 05 02 10                    MC    5,2,010   • SET OVF
1763•          002314  13 12 017              LA6       TC2   IRD,017   •
1764•          002315  12 10 017                       TC1   A0,017    •
1765•          002316  03 10 10 00              LA7       S     A0,A0,0   • LEFT SHIFT
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1766.  002317  00 14 10 02          T     XLTRM,A0,2          .
1767.  002320  15 15 02 00          MC    015,2,0             . CHANNEL CONTROL
1768.  002321  17 00 00 14          E     0,0,014             . START
1769.  002322  00 00 00 00          NOOP                      .
1770.  002323  03 10 10 00    LA8   S     A0,A0,0             . LEFT SHIFT
1771.  002324  00 14 10 02          T     XLTRM,A0,2          .
1772.  002325  13 03 017             TC2   CK,15               .
1773.  002326  16 10 002             RN    2                   . REPEAT NEXT 3 INST
1774.  002327  02 15 15 03          AS2   A5,XLTR,3           . A1 + TRANSLATOR TO A5
1775.  002330  15 15 02 00          MC    015,2,0             . CHANNEL CONTROL
1776.  002331  00 15 15 02          T     XLTR,A5,2           .
1777.  002332  17 00 00 14          E     0,0,014             . START
1778.  002333  00 00 00 00          NOOP                      .
1779.  002334  15 10 002       LA9A  MCS   2                   . SELECT MOST
1780.  002335  15 07 04 00          MC    7,4,0               . A TO SGR
1781.  002336  00 04 07 10          T     RGRD,PPROD,010      .
1782.  002337  17 00 00 14          E     0,0,014             . START
1783.  002340  15 05 01 00          MC    5,1,0               .
1784.                              .
1785.                              SETADR 02374  .
1786.                              .
1787.                              .
1788.                              . ILLEGAL I/O INST
1789.                              .
1790.  002374  01 0266              J     EMIILA              .
1791.  002375  12 12 002             TC1   A2,2                . I/O ILLEGAL INST INT CODE
1792.                              .
1793.                              . ILLEGAL CP INST
1794.                              .
1795.  002376  01 0266              J     EMIILA              .
1796.  002377  12 12 000             TC1   A2,0                . CP ILLEGAL INST INT CODE
1797.                              .
1798.                              SETADR  02400  .
1799.                              .
1800.  002400  15 00 00 00    LM3   MC    0,0,0               . U CONT PAGE SELECT
1801.  002401  00 14 04 00          T     A4,PTBLS,0          .
1802.  002402  01 2432              J     LNSUB               .
1803.  002403  00 00 00 00          NOOP                      .
1804.  002404  00 10 13 01          T     PAC,IRS,1           . IR VALUE TO PAC
1805.  002405  01 0324              J     EMA1A               .
1806.  002406  00 10 14 02          T     PTBLD,A4,2          .
1807.  002407  00 04 06 10    TA3   T     RGRD,SM,010         . RETURN LS
1808.  002410  15 07 04 00    TA4   MC    7,4,0               . A TO SGR
1809.  002411  00 04 06 10          T     RGRD,SM,010         . RETURN MS
1810.  002412  17 00 00 14          E     0,0,014             . START
1811.  002413  15 05 01 00          MC    5,1,0               . DOUBLE PRECISION STATUS
1812.  002414  00 11 10 01  EMA41A  T     A1,RGRS,1           . LS PORTION
1813.  002415  15 10 042             MCS   042                 . SHIFT LEFT DP LS ARITH (6-BIT)
1814.  002416  15 10 043             MCS   043                 . SHIFT LEFT DP MS ARITH (6-BIT)
1815.  002417  00 04 06 10          T     RGRD,SM,010         . RETURN LS
1816.  002420  00 14 06 10          T     A4,SM,010           .
1817.  002421  15 05 01 00          MC    5,1,0               . DOUBLE PRECISION STATUS
1818.  002422  15 10 046             MCS   046                 . EXTRACT BITS SHIFTED LEFT LS (6-BIT)
1819.  002423  15 10 047             MCS   047                 . EXTRACT BITS SHIFTED LEFT MS (6-BIT)
1820.  002424  00 11 06 00          T     A1,SM,0             .
1821.  002425  00 11 06 00          T     A1,SM,0             .
1822.  002426  15 07 04 00          MC    7,4,0               . A TO SGR
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1823•          002427  00 04 14 00                    T    RGRD,A4,0          • RETURN MS
1824•          002430  01 0626                        J    TA1                •
1825•          002431  12 12 040                     TC1  A2,040             • MASK
1826•                                                 •
1827•                                                 • THIS SUBROUTINE PERFORMS TESTS TO DETERMINE IF AN OPERATOR ENTRY CAUSED A
1828•                                                 • CHANGE IN THE DISPLAY REGISTER - MODIFIES ADDR REG (A4) AND DISPLAY IF NEC
1829•                                                 • INPUT A4 = ADDRESSED REGISTER A5 = ALTER MODE STATUS
1830•                                                 • OUTPUT A4 AND DISPLAY REG LOADED WITH MODIFIED VALUES IF CHANGE ENTERED
1831•                                                 •
1832•          002432  02 16 00 04          LNSUB    AS2  A6,UP,4            • SAVE RETURN+1 IN A6
1833•          002433  00 13 02 01                    T    A3,DREG,1          • SAVE CURRENT CONTENTS OF DISPLAY REG
1834•          002434  06 12 12 05                    LI   A2,A2,5            • SET A2 TO ALL ONES
1835•          002435  00 02 12 02  01  2576          T    DREG,A2,2          • ALL ONES TO DISPLAY TO TEST FOR POSSIBLE
1836•          002436  00 00 00 00                    NOOP                    •
1837•          002437  00 10 02 11                    T    A0,DREG,011        • REG CLEAR SWITCH ACTION READ DISP SAVE STAT
1838• T        002440  14 01 062                     BZ   LNSUB2             • CLEAR SW ACTIVATED SO
1839•          002441  00 15 15 10                    T    A5,A5,010          • TEST THE ALTER MODE
1840•          002442  13 02 000                     TC2  DREG,0             • REG CLEAR SW UNCHANGED SO STROBE DISPLAY
1841•          002443  00 00 00 00                    NOOP                    •
1842•          002444  00 10 02 11                    T    A0,DREG,011        • REG FOR POSSIBLE BIT ALTERATION RD DIS SS
1843• T        002445  14 01 052                     BZ   LNSUB1             • NO MODIF SO EXIT WITH ADDR REG A4
1844•                                                 •                       • LOADED WITH ADDRESSED REG (A4) VALUE
1845•          002446  00 15 15 10                    T    A5,A5,010          • TEST THE ALTER MODE STATUS
1846• T        002447  14 10 052                     BNZ  LNSUB1             • IS SET (NORMAL) SO EXIT WITH THE BIT/BITS
1847•          002450  06 14 13 04                    LI   A4,A3,4            • SET ON DISPLAY STROBE RET OR'D INTO A4
1848•          002451  06 14 13 00                    LI   A4,A3,0            • ALTER MODE CLR SO CLEAR BIT IN A4
1849•          002452  00 02 14 02  01  2600 LNSUB1   T    DREG,A4,2          • DISPLAY AND A4 LOADED WITH MOD/UNMOD VALUE
1850•          002453  12 10 377                     TC1  A0,0377            • DELAY CT
1851• T        002454  14 17 060           LNSUBA    BMJS LNSUBB             • JP IF MICRO-JP SW SELECTED
1852•          002455  04 10 10 17                    AS1  A0,A0,017          • DEC CT
1853• T        002456  14 10 054                     BNZ  LNSUBA             • DELAY LOOP
1854•          002457  00 00 00 00                    NOOP                    •
1855•          002460  00 00 16 02          LNSUBB    T    UP,A6,2            • RETURN
1856•          002461  00 00 00 00                    NOOP                    •
1857• T        002462  14 10 052           LNSUB2    BNZ  LNSUB1             • ALTER MODE BIT IS SET SO EXIT WITH
1858•          002463  12 14 000                     TC1  A4,0               • ADDR REG SET TO ALL ZEROS
1859•          002464  01 2452                      J    LNSUB1             • ALTER MODE CLEAR SO EXIT WITH
1860•          002465  00 14 12 00                    T    A4,A2,0            • ADDR REG SET TO ALL ONES
1861•          002466  02 14 00 04          DDV8     AS2  A4,UP,4            • SAVE MICRO-P + 1 IN A4
1862•          002467  03 11 11 10                    S    A1,A1,010          • SHIFT L ZERO FILL (SS)
1863•          002470  03 10 10 12                    S    A0,A0,012          • SHIFT L WITH INSERT FROM PREVIOUS (SS)
1864•          002471  03 13 13 12                    S    A3,A3,012          • SHIFT L WITH INSERT FROM PREVIOUS (SS)
1865•          002472  03 12 12 02                    S    A2,A2,2            • SHIFT L WITH INSERT FROM PREVIOUS
1866•          002473  17 00 10 00                    E    0,010,0            • ALLOW I/O
1867•          002474  15 10 01 00                    MC   010,1,0            • U CONT SHIFT INIT
1868•          002475  16 03 037                     DD   037                • REPEAT DOUBLE DIVIDE
1869•          002476  05 13 17 10                    SU   A3,A7,010          • A3 - A7 TO A3 (SS)
1870•          002477  05 12 16 11                    SU   A2,A6,011          • A2 - A6 TO A2 (SS)
1871•          002500  17 00 10 00                    E    0,010,0            • ALLOW I/O
1872•          002501  00 00 00 00                    NOOP                    •
1873• T        002502  14 00 106                     BN   DDV8A              •
1874•          002503  00 00 00 00                    NOOP                    •
1875•          002504  00 00 14 02          DDV8AA    T    UP,A4,2            • RETURN
1876• U        002505  00 14 00 00                    T    A4,SRUS,0          •
1877•          002506  04 13 17 13          DDV8A     AS1  A3,A7,013          • A3 + A7 TO A3 (SS)
1878•          002507  01 2504                      J    DDV8AA             •
1879•          002510  04 12 16 01                    AS1  A2,A6,1            • A2 + A6 TO A2
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1880•          002511  00 13 10 00          DDV0    T     A3,AC,0        • RA+1 TO A3
1881•          002512  15 07 04 00                  MC    7,4,0          • A TO SGR
1882•          002513  00 12 10 11          DDV0A   T     A2,RGRS,011    • RA TO A2 (SS) MS OF DIVIDEND
1883•          002514  15 00 00 10                  MC    0,0,010        • INC SGR TO RA+1
1884•          002515  15 00 00 10                  MC    0,0,010        • INC SGR TO RA+2
1885•          002516  00 10 10 01                  T     A0,RGRS,1      • RA+2 TO A0
1886•          002517  15 00 00 10                  MC    0,0,010        • INC SGR TO RA+3
1887• T        002520  14 00 150                    BN    DDV4           • JP IF DIVIDEND IS NEG
1888•          002521  00 11 10 01                  T     A1,RGRS,1      • RA+3 TO A1
1889•          002522  00 16 16 10                  T     A6,A6,010      • RM TO RM (SS)
1890• T        002523  14 00 171                    BN    DDV7           • JP IF DIVISOR IS NEG
1891•          002524  05 17 17 14                  SU    A7,A7,014      • COMP DIVISOR (RM+1) (SS)
1892•          002525  01 2466                      J     DDV8           • TO DIV/SUB SEQ
1893•          002526  05 17 17 04                  SU    A7,A7,4        • COMP DIVISOR BACK (WAS NOT NEG)
1894• U        002527  00 11 00 00          DDV1    T     A1,SRLS,0      •
1895• U        002530  00 10 00 00                  T     A0,SRUS,0      •
1896•          002531  00 04 11 10          DDV2    T     RGRD,A1,010    • LS OF QUOTIENT TO RA+3 (SS)
1897•          002532  15 07 04 00                  MC    7,4,0          • A TO SGR
1898•          002533  00 04 12 00                  T     RGRD,A2,0      • MS OF REMAINDER TO RA
1899•          002534  15 00 00 10                  MC    0,0,010        • INC SGR TO RA+1
1900•          002535  00 04 13 00                  T     RGRD,A3,0      • LS OF REMAINDER TO RA+1
1901•          002536  15 00 00 10                  MC    0,0,010        • INC SGR TO RA+2
1902•          002537  00 04 10 10                  T     RGRD,A0,010    • MS OF QUOTIENT TO RA+2 (SS)
1903•          002540  00 14 14 10          DDV2B   T     A4,A4,010      • A4 TO A4 (SS)
1904•          002541  00 10 05 05          DDV2A   T     A0,STAT1,5     • STATUS 1 TO A0 W/ROTATE
1905•          002542  12 11 004                    TC1   A1,4           • K
1906•          002543  06 10 11 04                  LI    A0,A1,4        • OR A0 + A1 TO A0
1907• T        002544  14 00 147                    BN    DDV3X          • JP IF OVERFLOW TO BE SET,EXECUTE REMOTE
1908•          002545  17 00 10 14                  E     0,010,014      • START
1909•          002546  00 00 00 00                  NOOP                 •
1910•          002547  00 05 10 04          DDV3X   T     STAT1,A0,4     • MODIFIED STAT1 TO STATUS 1
1911•          002550  05 11 11 14          DDV4    SU    A1,A1,014      • COMP DIVIDEND
1912•          002551  05 10 10 15                  SU    A0,A0,015      •
1913•          002552  05 13 13 15                  SU    A3,A3,015      •
1914•          002553  05 12 12 05                  SU    A2,A2,5        •
1915•          002554  00 16 16 10                  T     A6,A6,010      • RM TO RM (SS)
1916• T        002555  14 00 164                    BN    DDV5           • JP IF DIVISOR IS NEG
1917•          002556  05 17 17 14                  SU    A7,A7,014      • COMP DIVISOR (RM+1) (SS)
1918•          002557  01 2466                      J     DDV8           • TO DIV/SUB SEQ
1919•          002560  05 17 17 04                  SU    A7,A7,4        • COMP DIVISOR BACK (WAS NOT NEG)
1920• U        002561  05 11 00 14                  SU    A1,SRLS,014    • COMP LS OF QUOTIENT
1921•          002562  01 2566                      J     DDV6           •
1922• U        002563  05 10 00 05                  SU    A0,SRUS,5      • COMP MS OF QUOTIENT
1923•          002564  01 2466          DDV5        J     DDV8           • TO DIV/SUB SEQ
1924•          002565  05 16 16 05                  SU    A6,A6,5        • COMP MS OF DIVISOR
1925•          002566  05 13 13 14          DDV6    SU    A3,A3,014      • COMP DIVIDEND
1926•          002567  01 2527                      J     DDV1           •
1927•          002570  05 12 12 05                  SU    A2,A2,5        • COMP DIVIDEND
1928•          002571  01 2466          DDV7        J     DDV8           • TO DIV/SUB SEQ
1929•          002572  05 16 16 05                  SU    A6,A6,5        • COMP MS OF DIVISOR
1930• U        002573  05 11 00 14                  SU    A1,SRLS,014    • COMP LS OF QUOTIENT
1931•          002574  01 2531                      J     DDV2           •
1932• U        002575  05 10 00 05                  SU    A0,SRUS,5      • COMP MS OF QUOTIENT
1933•            2576  01 2436                •
1934•            2577  00 02 12 02                       SETADR 02700   •
1935•            2600  01 2453                •
1936•            2601  00 02 14 02            •
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1937•                                          • J=0 FOR IA W/O BYTE (FINAL OPERAND AT Y)
1938•                                          •
1939•   002700  17 00 00 11                     E    0,0,011              • BRANCH 1
1940•   002701  00 00 00 00                     NOOP                      •
1941•   002702  01 0376                         J    LA2                  • JUMP
1942•   002703  00 16 03 00                     T    A6,MDR,0             • MDR TO A6
1943•                                          •
1944•                                          • J=1 FOR IA W/O BYTE (FINAL OPERAND AT Y + RX)
1945•                                          •
1946•   002704  17 10 00 11                     E    010,0,011            • BRANCH 1, ((RX)TO AC)
1947•   002705  00 12 10 00                     T    A2,AC,0              • AC TO A2
1948•   002706  01 0376                         J    LA2                  • JUMP
1949•   002707  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1950•                                          •
1951•                                          • J=2 FOR IA W/O BYTE (FINAL OPERAND AT Y + RM)
1952•                                          •
1953•   002710  17 00 00 11                     E    0,0,011              • BRANCH 1
1954•   002711  00 12 11 00                     T    A2,A1,0              • A1 TO A2
1955•   002712  01 0376                         J    LA2                  • JUMP
1956•   002713  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1957•                                          •
1958•                                          • J=3 FOR IA W/O BYTE (FINAL OPERAND AT Y + (RM+1))
1959•                                          •
1960•   002714  17 00 00 11                     E    0,0,011              • BRANCH 1
1961•   002715  00 12 13 00                     T    A2,A3,0              • A3 TO A2
1962•   002716  01 0376                         J    LA2                  • JUMP
1963•   002717  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1964•                                          •
1965•                                          • J=4 CASCADE IW AT Y
1966•                                          •
1967•   002720  17 00 00 11                     E    0,0,011              • BRANCH 1
1968•   002721  00 00 00 00                     NOOP                      •
1969•   002722  01 2766                         J    LA17                 • JUMP
1970•   002723  00 16 03 00                     T    A6,MDR,0             • MDR TO A6
1971•                                          •
1972•                                          • J=5 CASCADE IW AT Y + RX
1973•                                          •
1974•   002724  17 12 00 11                     E    012,0,011            • BRANCH 1, ((RX) TO A2)
1975•   002725  00 00 00 00                     NOOP                      •
1976•   002726  01 2766                         J    LA17                 • JUMP
1977•   002727  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1978•                                          •
1979•                                          • J=6 CASCADE IW AT Y + RM
1980•                                          •
1981•   002730  17 00 00 11                     E    0,0,011              • BRANCH 1
1982•   002731  00 12 11 00                     T    A2,A1,0              • A1 TO A2
1983•   002732  01 2766                         J    LA17                 • JUMP
1984•   002733  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1985•                                          •
1986•                                          • J=7 FOR IA CASCADE IW AT Y + (RM+1)
1987•                                          •
1988•   002734  17 00 00 11                     E    0,0,011              • BRANCH 1
1989•   002735  00 12 13 00                     T    A2,A3,0              • A3 TO A2
1990•   002736  01 2766                         J    LA17                 • JUMP
1991•   002737  04 16 03 03                     ASI  A6,MDR,3             • A2 + MDR TO A6
1992•                                          •
1993•                                          • J=0 FOR IA WITH BYTE (FINAL OPERAND AT Y)
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1994.
1995.                 002740  17 00 00 11                          E     0,0,011          • BRANCH 1
1996.                 002741  07 12 00 12                          L2    A2,S0,012        • ZERO TO A2 (SS)
1997.                 002742  01 0366                              J     LA1              • JUMP
1998.                 002743  00 16 03 00                          T     A6,MDR,0         • MDR TO A6
1999.
2000.                                                              • J=1 FOR IA WITH BYTE (FINAL OPERAND AT Y + RX)
2001.
2002.                 002744  17 10 00 11                          E     010,0,011        • BRANCH 1
2003.                 002745  03 12 10 14                          S     A2,A0,014        • SHIFT R1,A0 TO A2 (SS)
2004.                 002746  01 0366                              J     LA1              • JUMP
2005.                 002747  04 16 03 03                          ASI   A6,MDR,3         • A2 + MDR TO A6
2006.
2007.                                                              • J=2 FOR IA WITH BYTE (FINAL OPERAND AT Y + RM)
2008.
2009.                 002750  17 00 00 11                          E     0,0,011          • BRANCH 1
2010.                 002751  03 12 11 14                          S     A2,A1,014        • SHIFT R1,A1 TO A2 (SS)
2011.                 002752  01 0366                              J     LA1              • JUMP
2012.                 002753  04 16 03 03                          ASI   A6,MDR,3         • A2 + MDR TO A6
2013.
2014.                                                              • J=3 FOR IA WITH BYTE (FINAL OPERAND AT Y +(RM+1))
2015.
2016.                 002754  17 00 00 11                          E     0,0,011          • BRANCH 1
2017.                 002755  03 12 13 14                          S     A2,A3,014        • SHIFT R1,A3 TO A2 (SS)
2018.                 002756  01 0366                              J     LA1              • JUMP
2019.                 002757  04 16 03 03                          ASI   A6,MDR,3         • A2 + MDR TO A6
2020.
2021.                                                              • INDIRECT CONTROL 1ST PASS
2022.
2023.                 002760  17 13 00 11          LAI6            E     013,0,011        • BRANCH 1, (RM + 1 TO A3)
2024.                 002761  00 11 12 00                          T     A1,A2,0          • A2 TO A1, ((RM) TO A2)
2025.                 002762  00 13 03 02                          T     SGR,MDR,2        • MDR TO SGR, (SEL RX)
2026.                 002763  15 00 00 00                          MC    0,0,0            • ENABLE PAGE ADDR/IA SEL/CLR IO RET
2027.                 002764  00 00 05 02                          T     UP,IDP,2         • INDIRECT POINTER TO MICRO-P
2028.                 002765  04 16 16 04                          ASI   A6,A6,4          • A6 + 1 TO A6
2029.
2030.                                                              • INDIRECT CONTROL CASCADE
2031.
2032.                 002766  17 00 00 11          LAI7            E     0,0,011          • BRANCH 1
2033.                 002767  00 00 00 00                          NOOP                   •
2034.                 002770  00 13 03 02                          T     SGR,MDR,2        • MDR TO SGR, (SEL RX)
2035.                 002771  15 00 00 00                          MC    0,0,0            • ENABLE PAGE ADDR/IA SEL/CLR IO RET
2036.                 002772  00 00 05 02                          T     UP,IDP,2         • INDIRECT POINTER TO MICRO-P
2037.                 002773  04 16 16 04                          ASI   A6,A6,4          • A6 + 1 TO A6
2038.
2039.                                                              SETADR 03000   •
2040.
2041.                 003000  12 16 002            SQ              TCI   A6,2             •
2042. T               003001  14 00 037                            BN    TAIO             • OVERFLOW
2043.                 003002  03 10 10 10                          S     A0,A0,010        • SHIFT LEFT (SS)
2044.                 003003  12 11 000                            TCI   A1,0            • CLR A1
2045. T               003004  14 00 037                            BN    TAIO             • OVERFLOW
2046.                 003005  03 10 10 00                          S     A0,A0,0          • SHIFT LEFT
2047.                 003006  15 10 002                            MCS   2                • SHIFT LEFT DP LS ARITH (4-BIT)
2048.                 003007  16 07 006                            SQR   6                • REPEAT NEXT 2 INST 7 TIMES
2049.                 003010  04 12 06 13                          ASI   A2,SM,013        •
2050.                 003011  04 12 00 03                          ASI   A2,S0,3          •
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2051•          003012  17 00 10 00                    E     0,010,0     • ALLOW I/O
2052•          003013  15 07 00 00                    MC    7,0,0       • A+1 TO SGR
2053•          003014  00 10 10 01                    T     A0,RGRS,1   •
2054•          003015  16 07 007                     SQR   7           • REPEAT NEXT 2 INST 8 TIMES
2055•          003016  04 12 06 13                    ASI   A2,SM,013   •
2056•          003017  04 12 00 03                    ASI   A2,S0,3     •
2057•          003020  00 13 06 00                    T     A3,SM,0     •
2058•          003021  04 17 16 03                    ASI   A7,A6,3     •
2059• T        003022  14 07 032                     BSS   TA7         •
2060•          003023  03 13 13 04                    S     A3,A3,4     • SHIFT RIGHT ZERO FILL
2061• T        003024  14 00 034                     BN    TA8         •
2062•          003025  04 12 17 10                    ASI   A2,A7,010   •
2063•          003026  04 12 06 00            TA5     ASI   A2,SM,0     •
2064•          003027  00 04 13 00            TA6     T     RGRD,A3,0   •
2065•          003030  17 00 00 14                    E     0,0,014     • START
2066•          003031  00 04 12 00                    T     RGRD,A2,0   •
2067• T        003032  14 00 035              TA7     BN    TA9         •
2068•          003033  05 12 06 13                    SU    A2,SM,013   •
2069• T        003034  14 07 026              TA8     BSS   TA5         •
2070•          003035  01 3027                TA9     J     TA6         •
2071•          003036  03 13 17 04                    S     A3,A7,4     •
2072•          003037  17 00 00 14            TA10    E     0,0,014     • START
2073•          003040  15 05 02 10                    MC    5,2,010     • SET OVF
2074•                                                •
2075•                                                • TRIG ROTATE EXEC
2076•                                                •
2077•          003041  01 3054                TP2     J     TTSCL       • TO SCALE SUB        ENTRY FOR M=3
2078•          003042  00 11 10 01            TP3     T     A1,RGRS,1   • (X),(RA+1) TO A1   ENTRY FOR M=1
2079•          003043  15 00 00 10                    MC    0,0,010     • INC SGR TO RA+2
2080•          003044  01 3111                        J     TPTR        • TO TRIG ROTATE SUB
2081•          003045  00 12 10 11                    T     A2,RGRS,011 • (A),(RA+2) TO A2 (SS)
2082•          003046  00 04 12 00                    T     RGRD,A2,0   • W TO RA+2
2083•          003047  15 07 04 00            TP3A    MC    7,4,0       • A TO SGR
2084•          003050  00 04 10 00            TP4     T     RGRD,A0,0   • Y TO RA
2085•          003051  15 00 00 10                    MC    0,0,010     • INC SGR TO RA+1
2086•          003052  17 00 10 14                    -     0,010,014   • START/HOLD SGR
2087•          003053  00 04 11 00                    T     RGRD,A1,0   • X TO RA+1
2088•                                                •
2089•                                                • TRIG SCALE SUB
2090•                                                •
2091•          003054  02 14 00 04            TTSCL   AS2   A4,UP,4     • SAVE RETURN + 1
2092•          003055  15 10 070                     MCS   070         • CORDIC SCALE INITIALIZE
2093•          003056  03 10 10 05                    S     A0,A0,5     • SHIFT RIGHT
2094•          003057  03 11 11 05                    S     A1,A1,5     • SHIFT RIGHT
2095•          003060  17 00 10 00                    E     0,010,0     • ALLOW I/O HOLD SGR
2096•          003061  12 16 000                     TC1   A6,0         •
2097•          003062  16 06 003                     RPTS  3           • REPEAT SCALE,NEXT 2 INST 4 TIMES
2098•          003063  04 10 06 03                    ASI   A0,SM,3     •
2099•          003064  04 11 06 03                    ASI   A1,SM,3     •
2100•          003065  00 00 14 02                    T     UP,A4,2     • RETURN
2101•          003066  12 16 017                     TC1   A6,017       •
2102•                                                •
2103•                                                • HYPER SCALE SUB
2104•                                                •
2105•          003067  02 14 00 04            THSCL   AS2   A4,UP,4     • SAVE RETURN + 1
2106•          003070  16 06 001                     RPTS  1           • REPEAT SCALE,NEXT 2 INST 2 TIMES
2107•          003071  04 10 06 03                    ASI   A0,SM,3     •
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2108.  003072  04 11 06 03          ASI  A1,SM,3          .
2109.  003073  17 00 10 00          E    0,010,0         . ALLOW I/O HOLD SGR
2110.  003074  12 16 006            TCI  A6,6            .
2111.  003075  16 06 002            RPTS 2               . REPEAT SCALE,NEXT 2 INST 3 TIMES
2112.  003076  05 10 06 00          SU   A0,SM,0         .
2113.  003077  05 11 06 00          SU   A1,SM,0         .
2114.  003100  30 00 14 02          T    UP,A4,2         . RETURN
2115.  003101  00 00 00 00          NOOP                 .
2116.                              .
2117.                              . TRIG VECTOR EXEC
2118.                              .
2119.  003102  01 3054        TP5   J    TTSCL           . TO SCALE SUB        ENTRY FOR M=2
2120.  003103  00 11 10 10    TP6   T    A1,RGRS,010     . (X),(RA+1) TO A1    ENTRY FOR M=0
2121.  003104  15 00 00 10          MC   0,0,010         . INC SGR TO RA+2
2122.  003105  01 3131              J    TPTV            . TO TRIG VECTOR SUB
2123.  003106  00 12 10 01          T    A2,RGRS,1       . (M),(RA+2) TO A2
2124.  003107  01 3047              J    TP3A            . TO RESTORE SEQ
2125.  003110  00 04 12 00          T    RGRD,A2,0       . M TO RA+2
2126.                              .
2127.                              . TRIG ROTATE COMPUTATION SUB
2128.                              .
2129.  003111  02 14 00 04    TPTR  AS2  A4,UP,4         . SAVE RETURN + 1
2130.  003112  12 16 017            TCI  A6,017          .
2131.  003113  15 10 030            MCS  030             . R1,COUNT=0
2132.  003114  16 04 000            RPTR 0               . REPEATE ROTATE,NEXT 3 INST 1 TIME
2133.  003115  02 12 11 13          AS2  A2,CORTBL,013   .
2134.  003116  04 11 06 06          ASI  A1,SM,6         .
2135.  003117  04 10 06 06          ASI  A0,SM,6         .
2136.  003120  17 00 10 00          E    0,010,0         . ALLOW I/O HOLD SGR
2137.  003121  12 16 000            TCI  A6,0            .
2138.  003122  15 10 013            MCS  013             . SHIFT RIGHT SP ARITH (4-BIT)
2139.  003123  16 04 015            RPTR 13              . REPEAT ROTATE,NEXT 3 INST 14 TIMES
2140.  003124  02 12 11 13          AS2  A2,CORTBL,013   .
2141.  003125  04 11 06 03          ASI  A1,SM,3         .
2142.  003126  04 10 06 03          ASI  A0,SM,3         .
2143.  003127  00 00 14 02          T    UP,A4,2         . RETURN
2144.  003130  00 00 00 00          NOOP                 .
2145.                              .
2146.                              . TRIG VECTOR COMPUTATION SUB
2147.                              .
2148.  003131  02 14 00 04    TPTV  AS2  A4,UP,4         . SAVE RETURN + 1
2149.  003132  12 16 017            TCI  A6,017          .
2150.  003133  15 10 030            MCS  030             . R1 COUNT=0
2151.  003134  16 04 000            RPTR 0               . REPEATE ROTATE,NEXT 3 INST 1 TIME
2152.  003135  02 12 11 03          AS2  A2,CORTBL,3     .
2153.  003136  04 11 06 16          ASI  A1,SM,016       .
2154.  003137  04 10 06 06          ASI  A0,SM,6         .
2155.  003140  17 00 10 00          E    0,010,0         . ALLOW I/O HOLD SGR
2156.  003141  12 16 000            TCI  A6,0            .
2157.  003142  15 10 013            MCS  013             . SHIFT RIGHT SP ARITH (4-BIT)
2158.  003143  16 04 015            RPTR 13              . REPEAT ROTATE,NEXT 3 INST 14 TIMES
2159.  003144  02 12 11 03          AS2  A2,CORTBL,3     .
2160.  003145  04 11 06 13          ASI  A1,SM,013       .
2161.  003146  04 10 06 03          ASI  A0,SM,3         .
2162.  003147  00 00 14 02          T    UP,A4,2         . RETURN
2163.  003150  00 00 00 00          NOOP                 .
2164.                              .
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2165•                                    • HYPER ROTATE W/O SCALE EXEC                    ENTRY FOR M=5
2166•                                    •
2167•  003151  00 11 10 01   TP7     T    A1,RGRS,1        • (X),(RA+1) TO A1
2168•  003152  15 00 00 10            MC   0,0,010          • INC SGR TO RA+2
2169•  003153  01 3206                J    TPHR             • TO HYPER ROTATE SUB
2170•  003154  00 12 10 11            T    A2,RGRS,011      • (W),(RA+2) TO A2 (SS)
2171•  003155  01 3047                J    TP3A             • TO RESTORE SEQ
2172•  003156  00 04 12 00            T    RGRD,A2,0        • W TO RA+2
2173•                                    •
2174•                                    • HYPER ROTATE W/SCALE EXEC                      ENTRY FOR M=7
2175•                                    •
2176•  003157  00 11 10 01   TP8     T    A1,RGRS,1        • (X),(RA+1) TO A1
2177•  003160  15 00 00 10            MC   0,0,010          • INC SGR TO RA+2
2178•  003161  01 3206                J    TPHR             • TO HYPER ROTATE SUB
2179•  003162  00 12 10 11            T    A2,RGRS,011      • (W),(RA+2) TO A2
2180•  003163  00 04 12 00            T    RGRD,A2,0        • W TO RA+2
2181•  003164  01 3067                J    THSCL            • TO SCALE SUB
2182•  003165  12 16 004             TC1  A6,4             •
2183•  003166  01 3050                J    TP4              • TO RESTORE SEQ
2184•  003167  15 07 04 00            MC   7,4,0            • A TO SGR
2185•                                    •
2186•                                    • HYPER VECTOR W/O SCALE                         ENTRY FOR M=4
2187•                                    •
2188•  003170  00 11 10 11   TP9     T    A1,RGRS,011      • (X),(RA+1) TO A1
2189•  003171  15 00 00 10            MC   0,0,010          • INC SGR TO RA+2
2190•  003172  01 3233                J    TPHV             • TO HYPER VECTOR SUB
2191•  003173  00 12 10 01            T    A2,RGRS,1        • (W),(RA+2) TO A2
2192•  003174  01 3050                J    TP4              • TO RESTORE SEQ
2193•  003175  15 07 04 00            MC   7,4,0            • A TO SGR
2194•                                    •
2195•                                    • HYPER VECTOR W/SCALE                           ENTRY FOR M=6
2196•                                    •
2197•  003176  00 11 10 11   TP10    T    A1,RGRS,011      • (X),(RA+1) TO A1
2198•  003177  15 00 00 10            MC   0,0,010          • INC SGR TO RA+2
2199•  003200  01 3233                J    TPHV             • TO HYPER VECTOR SUB
2200•  003201  00 12 10 01            T    A2,RGRS,1        • (W),(RA+2) TO A2
2201•  003202  01 3067                J    THSCL            • TO SCALE SUB
2202•  003203  12 16 004             TC1  A6,4             •
2203•  003204  01 3050                J    TP4              • TO RESTORE SEQ
2204•  003205  15 07 04 00            MC   7,4,0            • A TO SGR
2205•                                    •
2206•                                    • HYPER ROTATE SUB
2207•                                    •
2208•  003206  02 14 00 04   TPHR    AS2  A4,UP,4          • SAVE RETURN + 1
2209•  003207  12 16 001             TC1  A6,1             •
2210•  003210  15 10 013             MCS  013              • SHIFT RIGHT SP ARITH (4-BIT)
2211•  003211  16 04 003             RPTR 3                • REPEAT ROTATE,NEXT 3 INST 4 TIMES
2212•  003212  02 12 11 13            AS2  A2,CORTBL,013    •
2213•  003213  04 11 06 03            AS1  A1,SM,3          •
2214•  003214  04 10 06 03            AS1  A0,SM,3          •
2215•  003215  17 00 10 00            E    0,010,0          • ALLOW I/O HOLD SGR
2216•  003216  12 16 004             TC1  A6,4             •
2217•  003217  16 04 011             RPTR 9                • REPEAT ROTATE,NEXT 3 INST 10 TIMES
2218•  003220  02 12 11 13            AS2  A2,CORTBL,013    •
2219•  003221  04 11 06 03            AS1  A1,SM,3          •
2220•  003222  04 10 06 03            AS1  A0,SM,3          •
2221•  003223  17 00 10 00            E    0,010,0          • ALLOW I/O HOLD SGR
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2222.           003224  12 16 015                       TC1   A6,13
2223.           003225  16 04 002                       RPTR  2                 . REPEAT ROTATE,NEXT 3 INST 3 TIMES
2224.           003226  02 12 11 13                     AS2   A2,CORTBL,013     .
2225.           003227  04 11 06 03                     AS1   A1,SM,3           .
2226.           003230  04 10 06 03                     AS1   A0,SM,3           .
2227.           003231  00 00 14 02                     T     UP,A4,2           . RETURN
2228.           003232  15 10 070                       MCS   070               . CORDIC SCALE INITIALIZE
2229.                                                   .
2230.                                                   . HYPER ROTATE SUB
2231.                                                   .
2232.           003233  02 14 00 04             TPHV    AS2   A4,UP,4           . SAVE RETURN + 1
2233.           003234  12 16 001                       TC1   A6,1             .
2234.           003235  15 10 013                       MCS   013               . SHIFT RIGHT SP ARITH (4-BIT)
2235.           003236  16 05 003                       RPTV  3                 . REPEAT VECTOR,NEXT 3 INST 4 TIMES
2236.           003237  02 12 11 03                     AS2   A2,CORTBL,3       .
2237.           003240  04 11 06 13                     AS1   A1,SM,013         .
2238.           003241  04 10 06 03                     AS1   A0,SM,3           .
2239.           003242  17 00 10 00                     E     0,010,0           . ALLOW I/O HOLD SGR
2240.           003243  12 16 004                       TC1   A6,4             .
2241.           003244  16 05 011                       RPTV  9                 . REPEAT VECTOR,NEXT 3 INST 10 TIMES
2242.           003245  02 12 11 03                     AS2   A2,CORTBL,3       .
2243.           003246  04 11 06 13                     AS1   A1,SM,013         .
2244.           003247  04 10 06 03                     AS1   A0,SM,3           .
2245.           003250  17 00 10 00                     E     0,010,0           . ALLOW I/O HOLD SGR
2246.           003251  12 16 015                       TC1   A6,13
2247.           003252  16 05 002                       RPTV  2                 . REPEAT VECTOR,NEXT 3 INST 3 TIMES
2248.           003253  02 12 11 03                     AS2   A2,CORTBL,3       .
2249.           003254  04 11 06 13                     AS1   A1,SM,013         .
2250.           003255  04 10 06 03                     AS1   A0,SM,3           .
2251.           003256  00 00 14 02                     T     UP,A4,2           . RETURN
2252.           003257  15 10 070                       MCS   070               . CORDIC SCALE INITIALIZE
2253.                                                   .
2254.                                                   SETADR 03400  .
2255.                                                   .
2256.           003400  00 14 03 00             LB1     T     A4,MDR,0          . 2ND OP(LS)
2257.           003401  00 16 16 00                     T     A6,A6,0           . 2ND OP ADDRESS TO BUSS
2258.           003402  17 00 00 03                     E     0,0,3             . OP-REF,A TO SGR
2259.           003403  12 12 177                       TC1   A2,0177           . MASK
2260.           003404  00 12 12 04                     T     A2,A2,4           . FORM CHAR MASK
2261.           003405  06 11 03 00                     LI    A1,MDR,0          . CHANGE SIGN IF FP SUBTRACT/2ND OP(MS)
2262.           003406  00 13 10 01             LB2     T     A3,RGRS,1         . RA TO A3
2263.                                                   . 2ND OP - MS PART IN A1 / LS PART IN A4
2264.                                                   . 1ST OP - MS PART IN A3 / LS PART IN A0
2265.           003407  07 15 12 06                     L2    A5,A2,6           . 2ND OP CHACTERISTIC TO A5
2266.           003410  07 12 13 06                     L2    A2,A3,6           . 1ST OP CHACTERISTIC TO A2
2267.           003411  05 16 15 10                     SU    A6,A5,010         . CHACTERISTIC DIFF (SS)
2268.           003412  17 00 00 00                     E     0,0,0             . ALLOW I/O
2269.           003413  12 12 007                       TC1   A2,7             .
2270. T         003414  14 00 145                       BN    LB11              . JP IF 2ND GT 1ST
2271.           003415  00 17 13 00                     T     A7,A3,0           . 1ST OP(MS)
2272.           003416  00 13 10 00                     T     A3,A0,0           . 1ST OP(LS)
2273.           003417  00 10 11 00                     T     A0,A1,0           . 2ND OP(MS)
2274. T         003420  14 01 153                       BZ    LB12              . JP IF CHACTERISTICS EQUAL (NO SHIFT NEEDED)
2275.           003421  00 11 14 00                     T     A1,A4,0           . 2ND OP(LS)
2276.           003422  00 16 16 04             LB3     T     A6,A6,4           . ROTATE CHAR DIFF TO LOWER
2277.           003423  05 12 16 10                     SU    A2,A6,010         . CHECK FOR CHAR DIFF GT 28 BITS
2278.           003424  17 00 00 00                     E     0,0,0             . ALLOW I/O
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2279.          003425  12 12 377                    TC1  A2,0377          • MASK
2280. T        003426  14 00 222                    BN   LB18            • JP,SHIFT CT GT 28
2281.          003427  07 00 17 17                  L2   D0,A7,017       • CHECK FOR SIGN DIFFERENCE
2282.          003430  07 1C 12 06                  L2   A0,A2,6         • SIGN/CHAR 2ND OP
2283. T        003431  14 15 245                    BFPR LB21            • JP,FLOATING POINT W/ROUND (NO RESIDUE)
2284.          003432  07 12 17 06                  L2   A2,A7,6         • SIGN/CHAR 1ST OP
2285. T        003433  14 C0 037                    BN   LB4             •
2286.          003434  15 10 152                    MCS  0152            • HEX ALIGN LEAST
2287.          003435  05 11 11 14                  SU   A1,A1,C14       • COMPLIMENT THE SMALLER
2288.          003436  05 1C 10 05                  SU   A0,A0,5         •
2289.          003437  15 10 153          LB4       MCS  0153            • HEX ALIGN MOST
2290.          003440  04 13 06 13                  ASI  A3,SM,013       •
2291.          003441  04 12 06 11                  ASI  A2,SM,011       •
2292.          003442  17 00 00 00                  E    0,0,0           • ALLOW I/O
2293.          003443  00 15 12 00                  T    A5,A2,0         •
2294. T        003444  14 06 325                    BDZ  LB29            • JP,ANSWER ZERO
2295.          003445  12 12 010                    TC1  A2,010          •
2296.          003446  05 16 16 00                  SU   A6,A6,0         • ADJUST CT FOR RESIDUE
2297.                                               • POSITION RESIDUE
2298.          003447  15 1C 140                    MCS  0140            • HEX LEFT LEAST
2299.          003450  15 10 141                    MCS  0141            • HEX LEFT MOST
2300.          003451  C0 14 06 00          LB5       T    A4,SM,0         •
2301.          003452  00 11 15 00                  T    A1,A5,0         • ACCESS NORM COUNT
2302.          003453  C0 16 06 00                  T    A6,SM,0         •
2303.          003454  17 00 00 00          LB6       E    0,0,0           • ALLOW I/O
2304.          003455  00 1C 11 C0                  T    A0,A1,0         •
2305.          003456  00 11 13 00          LB7       T    A1,A3,0         •
2306.          003457  15 10 175                    MCS  0175            • HEX NORMALIZE MOST
2307.          003460  00 12 03 01                  T    A2,NORM,1       •
2308.                                               • POSITION COUNT
2309.          003461  03 12 12 04                  S    A2,A2,4         •
2310.          003462  03 12 12 04                  S    A2,A2,4         •
2311.                                               • ADJUST COUNT
2312.          003463  12 15 002                    TC1  A5,2            •
2313.          003464  00 15 15 04                  T    A5,A5,4         • ROTATE
2314.          003465  15 C0 00 10                  MC   0,0,010         • INC SGR TO RA+3
2315.          003466  14 C0 CC0                    BN                   • JP,RESIDUE UNDERFLOW
2316.                                               • STORE RESIDUE
2317.          003467  05 12 15 00                  SU   A2,A5,0         •
2318.          003470  17 C0 00 00          LB8       E    0,0,0           • ALLOW I/O
2319.          003471  12 13 377                    TC1  A3,0377         •
2320.          003472  06 12 13 12                  L1   A2,A3,C12        • TEST FOR ZERO COUNT
2321.          003473  07 13 17 C0                  L2   A3,A7,0         • CHACTERISTIC
2322. T        003474  14 C1 267                    BZ   LB23            • JP,NO RENORMALIZING
2323.          003475  05 13 12 00                  SU   A3,A2,0         • CORRECT CHAR
2324.          003476  06 17 17 10                  L1   A7,A7,010       • TEST FOR OVER/UNDERFLOW
2325.          003477  17 00 00 00                  E    0,0,0           • ALLOW I/O
2326.          003500  00 17 16 00                  T    A7,A6,0         •
2327. T        003501  14 C0 336                    BN   UNOV            • OVF/UF ERROR
2328.          003502  00 16 12 04                  T    A6,A2,4         • ROTATE
2329. T        003503  14 15 277                    BFPR LB24            • JP,FLOATING POINT WITH ROUND
2330.          003504  06 13 06 C4                  L1   A3,SM,4         •
2331.          003505  15 10 174                    MCS  0174            •
2332.          003506  00 0C 16 14                  T    D0,A6,014       • TEST FOR R4 SHIFT 1
2333.          003507  17 00 00 00                  E    0,0,0           • ALLOW I/O
2334.          003510  12 12 010                    TC1  A2,010          •
2335. T        003511  14 00 303                    BN   LB25            • JP,R4 SHIFT
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2336.          003512  05 16 16 00                      SU    A6,A6,0          . ADJUST COUNT FOR RESIDUE
2337.          003513  00 12 06 00                      T     A2,SM,0          . LS RENORMALIZED SUM
2338.                                                   . RESIDUE TO SHIFTER
2339.          003514  00 10 17 01                      T     A0,A7,0          .
2340.          003515  00 11 14 00                      T     A1,A4,0          .
2341.                                                   . SHIFT RESIDUE INTO SUM
2342.          003516  15 10 150                        MCS   0150             . HEX RIGHT ZERO FILL LEAST
2343.          003517  15 10 151                        MCS   0151             . HEX RIGHT ZERO FILL MOST
2344.          003520  06 12 06 04                      L1    A2,SM,4          .
2345.          003521  06 13 06 04                      L1    A3,SM,4          .
2346.                                                   . REPACK AND STORE SUM
2347.          003522  00 04 13 10                      T     RGRD,A3,010      .
2348.          003523  15 07 00 00                      MC    7,0,0            . A+1 TO SGR
2349.          003524  00 04 12 00                      T     RGRD,A2,         .
2350.                                                   . ADJUST COUNT FOR FINAL RESIDUE
2351.          003525  12 12 006                        TC1   A2,6             .
2352.          003526  05 16 16 00                      SU    A6,A6,0          .
2353.                                                   . CORRECT CHAR-24
2354.          003527  00 12 12 04                      T     A2,A2,4          . ROTATE
2355.          003530  05 17 12 00                      SU    A7,A2,0          .
2356.          003531  17 00 10 00                      E     0,010,0          . ALLOW I/O,KEEP SGR
2357.          003532  12 12 377                        TC1   A2,0377          .
2358.                                                   . ACCESS FINAL RESIDUE
2359.          003533  15 10 142                        MCS   0142             .
2360.          003534  15 10 143                        MCS   0143             .
2361.          003535  00 11 06 10          LB9        T     A1,SM,010        .
2362.          003536  07 16 06 16                      L2    A6,SM,016        .
2363.          003537  07 12 17 05                      L2    A2,A7,5          . MASK CHAR
2364. T        003540  14 06 331                        BDZ   LB27             . JP,RESIDUE = 0
2365.          003541  06 13 17 10                      L1    A3,A7,010        . TEST FOR CHAR UNDERFLOW
2366.          003542  06 12 16 04                      L1    A2,A6,4          . INSERT CHAR
2367.          003543  17 00 10 14          LB10       E     0,010,014        . START,KEEP SGR
2368.          003544  00 04 11 00                      T     RGRD,A1,0        .
2369.          003545  05 16 16 04          LB11       SU    A6,A6,4          . 2'S COMP A6
2370.          003546  00 17 11 00                      T     A7,A1,0          . 2ND OP(MS)
2371.          003547  00 11 10 00                      T     A1,A0,0          . 1ST OP(LS)
2372.          003550  00 10 13 00                      T     A0,A3,0          . 1ST OP(MS)
2373.          003551  01 3422                          J     LB3              .
2374.          003552  00 13 14 00                      T     A3,A4,0          . 2ND OP(LS)
2375.          003553  12 12 377            LB12       TC1   A2,0377          .
2376.          003554  07 00 17 17                      L2    D0,A7,017        . TEST SIGNS DIFFERENT
2377.          003555  07 10 12 06                      L2    A0,A2,6          . SIGN/CHAR 2ND OP
2378. T        003556  14 00 174                        BN    LB15             .
2379.          003557  07 12 17 06                      L2    A2,A7,6          . SIGN/CHAR 1ST OP
2380.          003560  05 13 11 10                      SU    A3,A1,010        .
2381.          003561  05 12 10 11                      SU    A2,A0,011        .
2382. T        003562  14 00 177                        BN    LB16             . JP,GO COMPLIMENT SUM AND TOGGLE SIGN
2383.          003563  00 00 00 00                      NOOP                   .
2384. T        003564  14 06 325            LB13       BDZ   LB29             .
2385.          003565  12 14 000            LB14       TC1   A4,0             . CLR RESIDUE
2386.          003566  17 00 00 00                      E     0,0,0            . ALLOW I/O
2387.          003567  12 16 000                        TC1   A6,0             . CLR RESIDUE
2388. T        003570  14 15 206                        BFPR  LB17             . JP,FLOATING POINT W/ROUND
2389.          003571  00 11 12 00                      T     A1,A2,0          .
2390.          003572  01 3456                          J     LB7              .
2391.          003573  00 10 11 00                      T     A0,A1,0          .
2392.                                                   . PERFORM ADD
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2393.            003574  04 13 11 13        LB15    ASI   A3,A1,013          .
2394.            003575  01 3564                    J     LB13               .
2395.            003576  04 12 10 11                ASI   A2,A0,011          .
2396.            003577  05 15 13 14        LB16    SU    A5,A3,014          . 2'S COMP
2397.            003600  05 12 12 05                SU    A2,A2,5            .
2398.            003601  12 13 200                  TCI   A3,0200            .
2399.            003602  00 13 13 04                T     A3,A3,4            .
2400.            003603  06 17 17 00                LI    A7,A7,0            . TOGGLE SIGN BIT
2401.            003604  01 3565                    J     LB14               .
2402.            003605  00 13 15 00                T     A3,A5,0            .
2403.            003606  12 12 377          LB17    TCI   A2,0377            .
2404.            003607  07 12 11 10                L2    A2,A1,010          . TEST FOR RENORMALIZE RIGHT 4
2405.            003610  00 10 11 00                T     A0,A1,0            .
2406. T          003611  14 01 056                  BZ    LB7                .
2407.            003612  12 12 004                  TCI   A2,4               .
2408.                                               . RIGHT 4 ROUND
2409.            003613  04 13 12 13                ASI   A3,A2,013          .
2410.            003614  12 10 000                  TCI   A0,0               .
2411.            003615  04 10 11 01                ASI   A0,A1,1            .
2412.            003616  12 12 376                  TCI   A2,0376            . RIGHT SHIFT 4 COUNT
2413.            003617  00 11 13 00                T     A1,A3,0            .
2414.            003620  01 3470                    J     LB8                . TO RENORMALIZE
2415.            003621  00 12 12 04                T     A2,A2,4            . ROTATE SHIFT CT
2416.                                               . CHAR DIFF GT 28
2417.                                               . MASK OFF SIGN/CHAR
2418.            003622  07 10 12 06        LB18    L2    A0,A2,6            .
2419. T          003623  14 00 227                  BN    LB19               .
2420.            003624  07 12 17 06                L2    A2,A7,6            .
2421.                                               . COMPLIMENT SMALLER IF SIGNS DIFFERENT
2422.            003625  05 11 11 14                SU    A1,A1,014          .
2423.            003626  05 10 10 05                SU    A0,A0,5            .
2424.            003627  00 15 12 00        LB19    T     A5,A2,0            .
2425.                                               . TEST FOR GT -52
2426.            003630  12 12 013                  TCI   A2,013             .
2427.            003631  05 12 16 10                SU    A2,A6,010          .
2428.            003632  00 12 -- 00                T     A2,A6,0            .
2429. T          003633  14 00 241                  BN    LB20               .
2430.            003634  11 16 010                  SC    A6,010             .
2431.            003635  15 10 152                  MCS   0152               . POSITION RESIDUE
2432.            003636  01 3451                    J     LB5                . TO RENORMALIZE
2433.            003637  15 10 153                  MCS   0153               . POSITION RESIDUE
2434. E          003640  000000                     .CLEAR RESIDUE
2435.            003641  12 14 000          LB20    TCI   A4,0               .
2436.            003642  12 16 000                  TCI   A6,0               .
2437.            003643  01 3454                    J     LB6                . TO RENORMALIZE
2438.            003644  00 11 15 10                T     A1,A5,010          .
2439.                                               . ROUND SMALLER
2440.            003645  15 10 162          LB21    MCS   0162               . HEX ROUND LEAST
2441. T          003646  14 00 263                  BN    LB22A              .
2442.            003647  15 10 163                  MCS   0163               . HEX ROUND MOST
2443.            003650  05 11 06 14                SU    A1,SM,014          .
2444.            003651  05 10 06 05                SU    A0,SM,5            .
2445.            003652  03 10 10 15          LB22    S     A0,A0,015          . RIGHT SIGN FILL (SS)
2446.            003653  03 11 11 06                S     A1,A1,6            . RIGHT N/SHIFT SAVED
2447.                                               . PERFORM ADD
2448.            003654  04 13 11 13                ASI   A3,A1,013          .
2449.            003655  04 12 10 11                ASI   A2,A0,011          .
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2450.          003656  12 14 000                        TC1  A4,0          . CLR RESIDUE
2451.  T       003657  14 06 325                        BDZ  LB29          .
2452.          003660  12 16 000                        TC1  A6,0          . CLR RESIDUE
2453.          003661  01 3454                         J    LB6           . TO RENORMALIZE
2454.          003662  00 11 12 00                     T    A1,A2,C       .
2455.          003663  04 11 06 10          LB22A      ASI  A1,SM,010     .
2456.          003664  12 10 000                        TC1  A0,0          .
2457.          003665  01 3652                         J    LB22          .
2458.          003666  04 10 06 01                     ASI  A0,SM,1       .
OP CODE ON NEXT LINE IS ILLEGAL
2459.          003667  000000                 LB23      L    RGRD,A3,014   .
2460.  T       003670  14 15 143                        BFPR LB10          . JP,FLOATING POINT W/ROUND
2461.          003671  15 07 00 00                     MC   7,0,0         . A+1 TO SGR
2462.          003672  00 04 11 00                     T    RGRD,A1,      .
2463.          003673  00 10 16 00                     T    A0,A6,0       .
2464.          003674  00 11 14 00                     T    A1,A4,0       .
2465.          003675  01 3720                         J    LB26          .
2466.          003676  12 16 002                        TC1  A6,2          .
2467.          003677  00 04 13 10          LB24      T    RGRD,A3,010   . RESTORE SUM FOR ROUND
2468.          003700  15 07 00 00                     MC   7,0,0         . A+1 TO SGR
2469.          003701  17 00 10 14                     E    0,010,014     . START,KEEP SGR
2470.          003702  00 04 06 00                     T    RGRD,SM,0     .
2471.                                                  . R4 SHIFT
2472.          003703  00 15 06 00          LB25      T    A5,SM,0       .
2473.                                                  . STORE SUM
2474.          003704  00 04 13 10                     T    RGRD,A3,010   .
2475.          003705  15 07 00 00                     MC   7,0,0         . A+1 TO SGR
2476.          003706  00 04 15 00                     T    RGRD,A5,0     .
2477.                                                  . SAVE LOWER 4 SUM
2478.          003707  12 12 017                        TC1  A2,017        .
2479.          003710  07 11 12 06                     L2   A1,A2,6       .
2480.                                                  . MASK AND INSERT INTO RESIDUE
2481.          003711  07 12 14 00                     L2   A2,A4,0       .
2482.          003712  06 11 12 04                     L1   A1,A2,4       .
2483.                                                  . ADJUST CHAR RESIDUE
2484.          003713  00 10 17 00                     T    A0,A7,0       .
2485.          003714  12 12 006                        TC1  A2,6          .
2486.          003715  00 12 12 04                     T    A2,A2,4       .
2487.          003716  05 17 12 00                     SU   A7,A2,0       .
2488.          003717  12 16 003                        TC1  A6,3          .
2489.          003720  17 00 10 00          LB26      E    0,010,0       . ALLOW I/O,KEEP SGR
2490.          003721  12 12 377                        TC1  A2,0377       .
2491.          003722  15 10 154                        MCS  0154          . RIGHT CIR FOR RESIDUE POSITIONING
2492.          003723  01 3535                         J    LB9           .
2493.          003724  15 10 155                        MCS  0155          . RIGHT CIR FOR RESIDUE POSITIONING
2494.                                                  . RESTORE ZEROS FOR ANSWER
2495.          003725  00 04 00 10          LB29      T    RGRD,SC,010   . ZERO
2496.          003726  15 07 00 00                     MC   7,0,0         . A+1 TO SGR
2497.          003727  14 15 325                        BFPR EMA1          .
2498.          003730  00 04 00 10                     T    RGRD,SO,010   . ZERO
2499.          003731  15 00 00 10          LB27      MC   0,0,010       . INC SGR TO RA+2
2500.          003732  00 04 00 00          LB28      T    RGRD,SC,0     . ZERO
2501.          003733  15 00 00 10                     MC   0,0,010       . INC SGR TO RA+3
2502.          003734  17 00 10 14                     E    0,010,014     . START,KEEP SGR
2503.          003735  00 04 00 00                     T    RGRD,SO,0     . ZERO
2504.                                                  . FLOATING POINT UNDER/OVERFLOW SEQUENCE
2505.          003736  15 05 02 10          UNOV      MC   5,2,010       . SET OVF
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2506. T  003737  14 14 343                    BFI  UNOVB          . JP,INT TO BE GENERATED,GO CHECK LOCKOUT
2507.    003740  12 12 004                    TCI  A2,4           . INT CODE
2508.    003741  17 00 00 14          UNOVA    E    0,0,014        . START
2509.    003742  C0 0C 00 00                   NOOP               .
2510. T  003743  14 16 341           UNOVB    BCL  UNOVA          . JP,CLASS II LOCKOUT IS SET
2511.    003744  12 17 120                    TCI  MAR,0120       . CLASS II MAIN MEMORY LOCATION
2512.    003745  01 1566                       J    CISC           . TO COMMON INT SEQ
2513.    003746  00 00 00 00                   NOOP               .
2514.                                          .
2515.                                          . - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
2516.                                          .  EMULATE SECTION PROM
2517.                                          . - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
2518.                                          .
2519.                                  ESROM.  PROC .
2520.                                  ESROMF  FORM 3,1,1,1,1,9    .
2521.                                          ESROMF    ESROM(1,1),ESROM(1,2),ESROM(1,3),ESROM(1,4),;  .
2522. -                                                 ESROM(1,5),0777-(ESROM(2,1))  .
2523.                                          END  .
2524.                                          .
2525.                                          SETADR 010000  .
2526.                                          .
2527.                                          . MEM MODE-3, M-1, I-1, O-1, U-1, ECW POINTER-9
2528.                                          .
2529.                                          . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
2530.  010000  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                    FC=77   RX
2531.  010001  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2532.  010002  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2533.  010003  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RR
2534.  010004  0 1 0 1 0 074                   ESROM     0,1,0,1,0 EMDS    .                          FC=76   RX
2535.  010005  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2536.  010006  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2537.  010007  0 0 0 1 1 101                   ESROM     0,0,0,1,1 EMD3    .                                         RR
2538.  010010  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                    FC=75   RX
2539.  010011  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2540.  010012  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2541.  010013  0 0 0 1 1 10                    ESROM     0,0,0,1,1 EMD4    .                                         RR
2542.  010014  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                    FC=74   RX
2543.  010015  0 1 0 1 0 147                   ESROM     0,1,0,1,0 EMF3    .                                         RK
2544.  010016  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2545.  010017  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RR
2546.  010020  0 1 0 1 0 603                   ESROM     0,1,0,1,0 EMJ1    .                          FC=73   RX
2547.  010021  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2548.  010022  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2549.  010023  0 0 0 1 1 142                   ESROM     0,0,0,1,1 EMJ4    .                                         RR
2550.  010024  0 1 0 1 0 543                   ESROM     0,1,0,1,0 EMH5    .                          FC=72   RX
2551.  010025  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2552.  010026  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2553.  010027  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RR
2554.  010030  0 1 0 1 0 553                   ESROM     0,1,0,1,0 EMH4    .                          FC=71   RX
2555.  010031  0 1 0 1 0 610                   ESROM     0,1,0,1,0 EMH3    .                                         RK
2556.  010032  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2557.  010033  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RR
2558.  010034  0 1 0 1 0 121                   ESROM     0,1,0,1,0 EMH2    .                          FC=70   RX
2559.  010035  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RK
2560.  010036  0 0 0 0 1 123                   ESROM     0,0,0,0,1 EMIIIO  . ILLEGAL INST                            RI
2561.  010037  0 0 0 1 0 737                   ESROM     0,0,0,1,0 EMH1    .                                         RR
2562.  010040  6 1 1 0 0 614                   ESROM     6,1,1,0,0 EMEII   .                          FC=67   RX
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2563.  010041  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2564.  010042  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2565.  010043  000000                           0  •                    UNASSIGNED                       RR
2566.  010044  6 1 1 0 0 612                    ESROM  6,1,1,0,0 EME10  •                                FC=66  RX
2567.  010045  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2568.  010046  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2569.  010047  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2570.  010050  6 1 1 0 0 616                    ESROM  6,1,1,0,0 EME9   •                                FC=65  RX
2571.  010051  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2572.  010052  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2573.  010053  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2574.  010054  6 1 1 0 0 620                    ESROM  6,1,1,0,0 EME8   •                                FC=64  RX
2575.  010055  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2576.  010056  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2577.  010057  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2578.  010060  0 0 0 0 1 462  000011 566         ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=63  RLRX
2579.  010061  0 0 0 0 1 462  000011 223         ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RLRK
2580.  010062  0 0 0 1 1 223                    ESROM  0,0,0,1,1 EME5   •                                RLRI
2581.  010063  0 0 0 1 1 227                    ESROM  0,0,0,1,1 EME6   •                                RLRR
2582.  010064  2 0 0 1 1 235                    ESROM  2,0,0,1,1 EMC14  •                                FC=62  RLRX
2583.  010065  0 0 0 1 1 241                    ESROM  0,0,0,1,1 EMC13  •                                RLRK
2584.  010066  2 0 0 1 1 246                    ESROM  2,0,0,1,1 EMC12  •                                RLRI
2585.  010067  0 0 0 1 1 252                    ESROM  0,0,0,1,1 EMC11  •                                RLRR
2586.  010070  0 0 0 0 1 260                    ESROM  0,0,0,0,1 EMC10  •                                FC=61  RLRX
2587.  010071  0 0 0 0 1 264                    ESROM  0,0,0,0,1 EMC9   •                                RLRK
2588.  010072  0 0 0 0 1 270                    ESROM  0,0,0,0,1 EMC8   •                                RLRI
2589.  010073  0 0 0 0 1 274                    ESROM  0,0,0,0,1 EMC7   •                                RLRR
2590.  010074  0 0 0 0 1 302                    ESROM  0,0,0,0,1 EMC6   •                                FC=60  RLRX
2591.  010075  0 0 0 0 1 310                    ESROM  0,0,0,0,1 EMC5   •                                RLRK
2592.  010076  0 0 0 0 1 314                    ESROM  0,0,0,0,1 EMC4   •                                RLRI
2593.  010077  0 0 0 0 1 320                    ESROM  0,0,0,0,1 EMC3   •                                RLRR
2594.  010100  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=57  RX
2595.  010101  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2596.  010102  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2597.  010103  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2598.  010104  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=56  RX
2599.  010105  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2600.  010106  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2601.  010107  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2602.  010110  1 1 1 0 0 774                    ESROM  1,1,1,0,0 EML6   •                                FC=55  RX
2603.  010111  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2604.  010112  1 1 0 0 0 777                    ESROM  1,1,0,0,0 EML5   •                                RI
2605.  010113  0 0 0 0 1 677                    ESROM  0,0,0,0,1 EML4   •                                RR
2606.  010114  0 1 1 0 0 755                    ESROM  0,1,1,0,0 EML3   •                                FC=54  RX
2607.  010115  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2608.  010116  0 1 0 0 0 743                    ESROM  0,1,0,0,0 EML2   •                                RI
2609.  010117  0 0 0 0 1 741                    ESROM  0,0,0,0,1 EML1   •                                RR
2610.  010120  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=53  RX
2611.  010121  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2612.  010122  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2613.  010123  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2614.  010124  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=52  RX
2615.  010125  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2616.  010126  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2617.  010127  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2618.  010130  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    FC=51  RX
2619.  010131  0 0 0 0 1 462                    ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
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2620.  010132  0 0 0 0 1 462  ESROM  0,C,0,0,1 EMIIU  • ILLEGAL INST                    RI
2621.  010133  0 0 0 0 1 462  ESROM  0,C,0,0,1 EMIIU  • ILLEGAL INST                    RR
2622.  010134  0 0 0 0 1 462  ESROM  0,C,0,0,1 EMIIU  • ILLEGAL INST          FC=50     RX
2623.  010135  0 0 0 0 1 462  ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RK
2624.  010136  C 0 0 0 1 462  ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2625.  010137  0 0 0 0 1 462  ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2626.  010140  0 1 1 0 1 522  ESROM  0,1,1,0,1 EMF2   •                      FC=47     RX
2627.  010141  C 0 1 0 1 466  ESROM  0,0,1,0,1 EMA54  •                                RK
2628.  010142  0 0 0 0 1 127  ESROM  0,0,0,0,1 EMA47  •                                RI
2629.  010143  0 C 0 0 1 466  ESROM  0,0,0,0,1 EMA54  •                                RR
2630.  010144  0 1 1 0 1 472  ESROM  0,1,1,0,1 EMA53  •                      FC=46     RX
2631.  010145  0 0 1 0 1 476  ESROM  0,0,1,0,1 EMA52  •                                RK
2632.  010146  C 0 0 0 1 127  ESROM  0,C,0,0,1 EMA47  •                                RI
2633.  010147  0 0 0 0 1 476  ESROM  0,C,0,0,1 EMA52  •                                RR
2634.  010150  0 1 1 C 1 502  ESROM  0,1,1,0,1 EMA51  •                      FC=45     RX
2635.  010151  C 0 1 0 1 506  ESROM  0,0,1,0,1 EMA50  •                                RK
2636.  010152  0 0 0 0 1 127  ESROM  0,C,0,0,1 EMA47  •                                RI
2637.  010153  0 0 0 0 1 506  ESROM  0,C,0,0,1 EMA5C  •                                RR
2638.  010154  0 1 1 0 1 512  ESROM  0,1,1,0,1 EMA49  •                      FC=44     RX
2639.  010155  0 0 1 0 1 516  ESROM  0,C,1,0,1 EMA48  •                                RK
2640.  010156  C 0 0 0 1 127  ESROM  0,0,0,0,1 EMA47  •                                RI
2641.  010157  0 0 0 0 1 516  ESROM  0,0,0,0,1 EMA48  •                                RR
2642.  010160  C 1 1 0 1 401  ESROM  0,1,1,0,1 EMA62  •                      FC=43     RX
2643.  010161  1 1 1 0 0 413  ESROM  1,1,1,0,0 EMA6C  •                                RK
2644.  010162  0 0 0 0 1 410  ESROM  0,0,0,0,1 EMA61  •                                RI
2645.  010163  C 0 0 0 1 462  ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RR
2646.  010164  0 1 1 0 1 417  ESROM  0,1,1,0,1 EMA59  •                      FC=42     RX
2647.  010165  C 0 1 0 1 423  ESROM  0,0,1,0,1 EMA58  •                                RK
2648.  010166  C 0 0 0 1 462  ESROM  0,0,0,0,1 EMIIU  • ILLEGAL INST                    RI
2649.  010167  0 0 0 0 1 423  ESROM  0,C,0,0,1 EMA58  •                                RR
2650.  010170  0 1 1 0 1 427  ESROM  0,1,1,C,1 EMA57  •                      FC=41     RX
2651.  010171  C 0 1 0 1 433  ESROM  0,C,1,0,1 EMA56  •                                RK
2652.  010172  C 0 0 0 1 405  ESROM  0,C,0,0,1 EMC2   •                                RI
2653.  010173  0 0 0 0 1 433  ESROM  0,C,0,0,1 EMA56  •                                RR
2654.  010174  0 1 1 0 1 672  ESROM  0,1,1,0,1 EMA46  • OR + 40                FC=40     RX
2655.  010175  C 0 1 0 1 671  ESROM  0,0,1,0,1 EMA45  • OR + 40                        RK
2656.  010176  C 0 0 0 1 437  ESROM  0,C,0,0,1 EMA55  • ADDRESS BIT 5 MUST #1          RI
2657.  010177  0 0 0 0 1 671  ESROM  0,0,0,0,1 EMA45  • OR + 40                        RR
2658.  010200  0 0 0 0 1 512  ESROM  0,C,0,0,1 EMIIL  • ILLEGAL INST          FC=37     RX
2659.  010201  0 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST                    RK
2660.  010202  0 0 0 0 1 512  ESROM  0,C,0,0,1 EMIIL  • ILLEGAL INST                    RI
2661.  010203  0 0 0 0 1 512  ESROM  0,C,0,0,1 EMIIL  • ILLEGAL INST                    RR
2662.  010204  C 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST          FC=36     RX
2663.  010205  0 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST                    RK
2664.  010206  C 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST                    RI
2665.  010207  0 C 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST                    RR
2666.  010210  4 1 1 0 0 065  ESROM  4,1,1,0,0 EMJ2   •                      FC>35     RX
2667.  010211  0 1 1 0 0 173  ESROM  0,1,1,0,0 EMC1   •                                RK
2668.  010212  4 1 0 0 0 065  ESROM  4,1,0,0,0 EMJ2   •                                RI
2669.  010213  0 0 0 0 1 057  ESROM  0,0,0,0,1 EMJ3   •                                RR
2670.  010214  0 1 1 0 0 350  ESROM  0,1,1,0,0 EMA8   •                      FC=34     RX
2671.  010215  0 0 1 1 1 202  ESROM  0,0,1,1,1 EMA34  •                                RK
2672.  010216  0 1 0 0 0 350  ESROM  0,1,0,0,0 EMA8   •                                RI
2673.  010217  0 0 0 1 1 202  ESROM  0,0,0,1,1 EMA34  •                                RR
2674.  010220  0 1 1 0 0 210  ESROM  0,1,1,0,0 EMA33  •                      FC=33     RX
2675.  010221  0 0 1 1 1 216  ESROM  0,0,1,1,1 EMA32  •                                RK
2676.  010222  0 1 0 0 0 210  ESROM  0,1,0,0,0 EMA33  •                                RI
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2677.  010223  0 0 0 1 1 216  ESROM  0,0,0,1,1 EMA32  •                          RR
2678.  010224  0 1 1 0 0 221  ESROM  0,1,1,0,0 EMA30  •                FC=32     RX
2679.  010225  0 0 1 1 1 220  ESROM  0,0,1,1,1 EMA31  •                          RK
2680.  010226  0 1 0 0 0 221  ESROM  0,1,0,0,0 EMA30  •                          RI
2681.  010227  0 0 0 1 1 220  ESROM  0,0,0,1,1 EMA31  •                          RR
2682.  010230  0 1 1 0 0 224  ESROM  0,1,1,0,0 EMA28  •                FC=31     RX
2683.  010231  0 0 1 1 1 223  ESROM  0,0,1,1,1 EMA29  •                          RK
2684.  010232  0 1 0 0 0 224  ESROM  0,1,0,0,0 EMA28  •                          RI
2685.  010233  0 0 0 1 1 223  ESROM  0,0,0,1,1 EMA29  •                          RR
2686.  010234  0 1 1 0 0 227  ESROM  0,1,1,0,0 EMA26  •                FC=30     RX
2687.  010235  0 0 1 1 1 226  ESROM  0,0,1,1,1 EMA27  •                          RK
2688.  010236  0 1 0 0 0 227  ESROM  0,1,0,0,0 EMA26  •                          RI
2689.  010237  0 0 0 1 1 226  ESROM  0,0,0,1,1 EMA27  •                          RR
2690.  010240  0 1 1 0 0 472  ESROM  0,1,1,0,0 EMK2   •                FC=27     RX
2691.  010241  0 0 1 0 1 517  ESROM  0,0,1,0,1 EMK1   •                          RK
2692.  010242  0 1 0 0 0 472  ESROM  0,1,0,0,0 EMK2   •                          RI
2693.  010243  0 0 0 0 1 517  ESROM  0,0,0,0,1 EMK1   •                          RR
2694.  010244  0 1 1 0 0 122  ESROM  0,1,1,0,0 EMA43  •                FC=26     RX
2695.  010245  0 0 1 0 1 121  ESROM  0,0,1,0,1 EMA44  •                          RK
2696.  010246  0 1 0 0 0 122  ESROM  0,1,0,0,0 EMA43  •                          RI
2697.  010247  0 0 0 0 1 121  ESROM  0,0,0,0,1 EMA44  •                          RR
2698.  010250  2 1 1 0 0 236  ESROM  2,1,1,0,0 EMA25  •                FC=25     RX
2699.  010251  0 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST           RK
2700.  010252  2 1 0 0 0 236  ESROM  2,1,0,0,0 EMA25  •                          RI
2701.  010253  2 0 0 1 1 252  ESROM  2,0,0,1,1 EMA22  •                          RR
2702.  010254  0 1 1 0 0 242  ESROM  0,1,1,0,0 EMA23  •                FC=24     RX
2703.  010255  0 0 1 1 1 241  ESROM  0,0,1,1,1 EMA24  •                          RK
2704.  010256  0 1 0 0 0 242  ESROM  0,1,0,0,0 EMA23  •                          RI
2705.  010257  0 0 0 1 1 241  ESROM  0,0,0,1,1 EMA24  •                          RR
2706.  010260  2 1 1 0 0 260  ESROM  2,1,1,0,0 EMA21  •                FC=23     RX
2707.  010261  0 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST           RK
2708.  010262  2 1 0 0 0 260  ESROM  2,1,0,0,0 EMA21  •                          RI
2709.  010263  2 0 0 1 1 267  ESROM  2,0,0,1,1 EMA20  •                          RR
2710.  010264  0 1 1 0 0 300  ESROM  0,1,1,0,0 EMA17  •                FC=22     RX
2711.  010265  0 0 1 1 1 277  ESROM  0,0,1,1,1 EMA18  •                          RK
2712.  010266  0 1 0 0 0 300  ESROM  0,1,0,0,0 EMA17  •                          RI
2713.  010267  0 0 0 1 1 277  ESROM  0,0,0,1,1 EMA18  •                          RR
2714.  010270  2 1 1 0 0 275  ESROM  2,1,1,0,0 EMA19  •                FC=21     RX
2715.  010271  0 0 0 0 1 512  ESROM  0,0,0,0,1 EMIIL  • ILLEGAL INST           RK
2716.  010272  2 1 0 0 0 275  ESROM  2,1,0,0,0 EMA19  •                          RI
2717.  010273  2 0 0 1 1 313  ESROM  2,0,0,1,1 EMA14  •                          RR
2718.  010274  0 1 1 0 0 303  ESROM  0,1,1,0,0 EMA15  •                FC=20     RX
2719.  010275  0 0 1 1 1 302  ESROM  0,0,1,1,1 EMA16  •                          RK
2720.  010276  0 1 0 0 0 303  ESROM  0,1,0,0,0 EMA15  •                          RI
2721.  010277  0 0 0 1 1 302  ESROM  0,0,0,1,1 EMA16  •                          RR
2722.  010300  5 1 1 0 0 325  ESROM  5,1,1,0,0 EMA11  •                FC=17     RX
2723.  010301  0 0 1 0 1 127  ESROM  0,0,1,0,1 EMA42  •                          RK
2724.  010302  5 1 0 0 0 325  ESROM  5,1,0,0,0 EMA11  •                          RI
2725.  010303  0 0 0 0 1 127  ESROM  0,0,0,0,1 EMA42  •                          RR
2726.  010304  3 1 1 0 1 323  ESROM  3,1,1,0,1 EMA12  •                FC=16     RX
2727.  010305  0 0 1 0 1 131  ESROM  0,0,1,0,1 EMA41  •                          RK
2728.  010306  3 1 0 0 1 323  ESROM  3,1,0,0,1 EMA12  •                          RI
2729.  010307  0 0 0 0 1 131  ESROM  0,0,0,0,1 EMA41  •                          RR
2730.  010310  1 1 1 0 1 316  ESROM  1,1,1,0,1 EMA13  •                FC=15     RX
2731.  010311  0 0 1 0 1 161  ESROM  0,0,1,0,1 EMA37  •                          RK
2732.  010312  1 1 0 0 1 316  ESROM  1,1,0,0,1 EMA13  •                          RI
2733.  010313  0 0 0 0 1 161  ESROM  0,0,0,0,1 EMA37  •                          RR
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2734.  010314  7 1 1 0 1 316   ESROM  7,1,1,0,1 EMA13  .                          FC=14  RX
2735.  010315  0 0 1 1 1 156   ESROM  0,0,1,0,1 EMA38  .                                 RK
2736.  010316  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2737.  010317  0 0 0 1 1 156   ESROM  0,0,0,0,1 EMA38  .                                 RR
2738.  010320  1 1 1 1 1 366   ESROM  1,1,1,1,1 EMA5   .                          FC>13  RX
2739.  010321  0 0 1 1 1 136   ESROM  0,0,1,0,1 EMA40  .                                 RK
2740.  010322  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2741.  010323  0 0 0 1 1 136   ESROM  0,0,0,0,1 EMA40  .                                 RR
2742.  010324  3 1 1 0 1 330   ESROM  3,1,1,0,1 EMA10  .                          FC=12  RX
2743.  010325  0 0 1 1 1 143   ESROM  0,0,1,0,1 EMA39  .                                 RK
2744.  010326  3 1 0 0 1 330   ESROM  3,1,0,0,1 EMA10  .                                 RI
2745.  010327  0 0 0 1 1 143   ESROM  0,0,0,0,1 EMA39  .                                 RR
2746.  010330  1 1 1 0 1 325   ESROM  1,1,1,0,1 EMA11  .                          FC=11  RX
2747.  010331  0 0 1 1 1 164   ESROM  0,0,1,0,1 EMA36  .                                 RK
2748.  010332  1 1 0 0 1 325   ESROM  1,1,0,0,1 EMA11  .                                 RI
2749.  010333  0 0 0 1 1 164   ESROM  0,0,0,0,1 EMA36  .                                 RR
2750.  010334  7 1 1 0 1 325   ESROM  7,1,1,0,1 EMA11  .                          FC=10  RX
2751.  010335  0 0 1 1 1 167   ESROM  0,0,1,0,1 EMA35  .                                 RK
2752.  010336  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2753.  010337  0 0 0 1 1 167   ESROM  0,0,0,0,1 EMA35  .                                 RR
2754.  010340  0 1 1 0 0 341   ESROM  0,1,1,0,0 EMA9   .                          FC=07  RX
2755.  010341  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2756.  010342  0 1 0 0 0 341   ESROM  0,1,0,0,0 EMA9   .                                 RI
2757.  010343  0 0 0 1 1 076   ESROM  0,0,0,0,1 EME3   .                                 RR
2758.  010344  2 1 1 0 0 363   ESROM  2,1,1,0,0 EMA6   .                          FC=06  RX
2759.  010345  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2760.  010346  2 1 0 0 0 363   ESROM  2,1,0,0,0 EMA6   .                                 RI
2761.  010347  0 0 0 1 1 103   ESROM  0,0,0,0,1 EME2   .                                 RR
2762.  010350  0 1 1 0 0 355   ESROM  0,1,1,0,0 EMA7   .                          FC=05  RX
2763.  010351  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2764.  010352  0 1 0 0 0 355   ESROM  0,1,0,0,0 EMA7   .                                 RI
2765.  010353  0 0 0 1 1 110   ESROM  0,0,0,0,1 EME1   .                                 RR
2766.  010354  6 1 1 0 0 355   ESROM  6,1,1,0,0 EMA7   .                          FC=04  RX
2767.  010355  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2768.  010356  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2769.  010357  0 0 0 0 0 737   ESROM  0,0,0,0,0 EMF1   .                                 RR
2770.  010360  0 1 1 1 1 366   ESROM  0,1,1,1,1 EMA5   .                          FC=03  RX
2771.  010361  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2772.  010362  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2773.  010363  0 0 0 0 0 637   ESROM  0,0,0,0,0 EMA2   .                                 RR
2774.  010364  2 1 1 0 0 377   ESROM  2,1,1,0,0 EMA3   .                          FC=02  RX
2775.  010365  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2776.  010366  2 1 0 0 0 377   ESROM  2,1,0,0,0 EMA3   .                                 RI
2777.  010367  0 0 0 1 0 677   ESROM  0,0,0,1,0 EMA0   .                                 RR
2778.  010370  0 1 1 0 0 373   ESROM  0,1,1,0,0 EMA4   .                          EC=01  RX
2779.  010371  0 0 1 1 1 067   ESROM  0,0,1,1,1 EME7   .                                 RK
2780.  010372  0 1 0 0 0 373   ESROM  0,1,0,0,0 EMA4   .                                 RI
2781.  010373  0 0 0 1 1 067   ESROM  0,0,0,1,1 EME7   .                                 RR
2782.  010374  6 1 1 0 0 373   ESROM  6,1,1,0,0 EMA4   .                          FC=00  RX
2783.  010375  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RK
2784.  010376  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RI
2785.  010377  0 0 0 0 1 512   ESROM  0,0,0,0,1 EMIIL  . ILLEGAL INST                     RR
2786.                         END    .

        SRLS
        SRUS
        FPDV
        FPML
```

APPENDIX D

MAIN MEMORY ADDRESS ALLOCATION

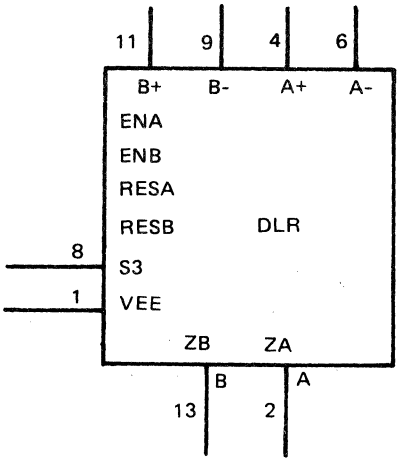
ADDRESS	FUNCTION
000000 – 000107	Unassigned
000110	CP Class III interrupt address for Store P
000111	CP Class III interrupt address for Store Status #1
000112	CP Class III interrupt address for Store Status #2
000113	CP Class III interrupt address for Store RTC Lower
000114	CP Class III interrupt address for Load P
000115	CP Class III interrupt address for Load Status #1
000116	CP Class III interrupt address for Load Status #2
000117	CP Class III interrupt address for Store RTC Upper
000120	CP Class II interrupt address for Store P
000121	CP Class II interrupt address for Store Status #1
000122	CP Class II interrupt address for Store Status #2
000123	CP Class II interrupt address for Store RTC Lower
000124	CP Class II interrupt address for Load P
000125	CP Class II interrupt address for Load Status #1
000126	CP Class II interrupt address for Load Status #2
000127	CP Class II interrupt address for Store RTC Upper
000130	CP Class I interrupt address for Store P
000131	CP Class I interrupt address for Store Status #1
000132	CP Class I interrupt address for Store Status #2
000133	CP Class I interrupt address for Store RTC Lower
000134	CP Class I interrupt address for Load P
000135	CP Class I interrupt address for Load Status #1
000136	CP Class I interrupt address for Load Status #2
000137	CP Class I interrupt address for Store RTC Upper
000140	IO Command Cell Location 1
000141	IO Command Cell Location 2
000142 – 000177	Unassigned
000200	Channel 0 EI Interrupt Storage

ADDRESS	FUNCTION
000201	Channel 1 EI Interrupt Storage
000202	Channel 2 EI Interrupt Storage
000203	Channel 3 EI Interrupt Storage
000204	Channel 4 EI Interrupt Storage
000205	Channel 5 EI Interrupt Storage
000206	Channel 6 EI Interrupt Storage
000207	Channel 7 EI Interrupt Storage
000210	Channel 10 EI Interrupt Storage
000211	Channel 11 EI Interrupt Storage
000212	Channel 12 EI Interrupt Storage
000213	Channel 13 EI Interrupt Storage
000214	Channel 14 EI Interrupt Storage
000215	Channel 15 EI Interrupt Storage
000216	Channel 16 EI Interrupt Storage
000217	Channel 17 EI Interrupt Storage
000220 – 177777	Unassigned

APPENDIX E

DEVICE DESCRIPTIONS

This appendix contains descriptions of the logic devices used on the DPS logic and memory circuit cards. These descriptions are a valuable aid in understanding the logic schematic diagrams in Chapter 9 (Volume II) on which these logic devices appear in symbolic form.



GROUND PIN – 14
VOLTAGE PIN – 07

PIN NAMES

A+, A-, B+, B-	Inputs
EN A, EN B	Enables
VEE, S3	-10 Volts Supply
RES A, RES B	Terminating Resistors
ZA, ZB	Outputs

DESCRIPTION

This integrated circuit contains two line receivers which are designed to discriminate a worst case logic swing of 2 volts from a ±10 volts common mode noise signal or ground shift. Each output is enabled by a high enable (ENA or ENB). The logic configuration is shown below.

LOGIC CONFIGURATION

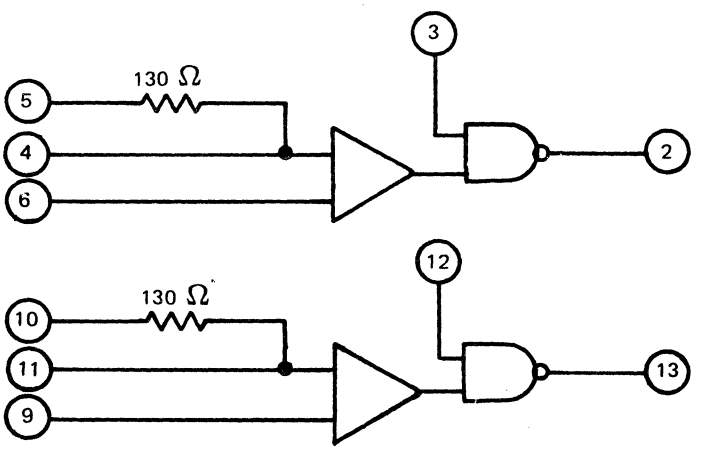
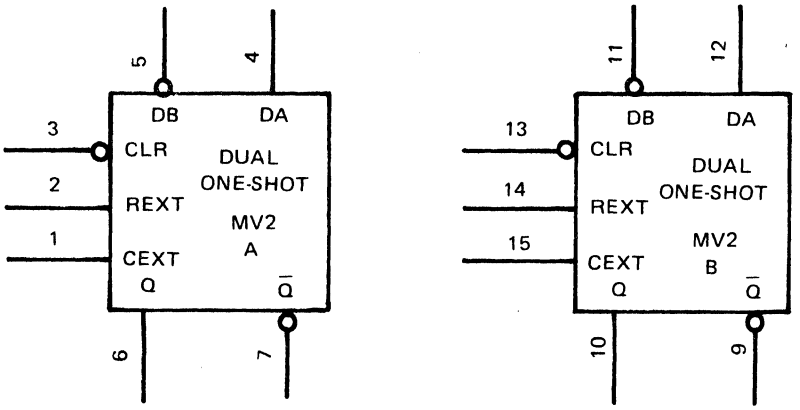


Figure E-1. Dual Line Receiver (7903776)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

DA	Trigger Input (Active High)	CEXT, REXT	External Timing
DB	Trigger Input (Active Low)	Q	Output
CLR	Master Reset (Active Low)	$\overline{Q}$	Complementary Output

DESCRIPTION

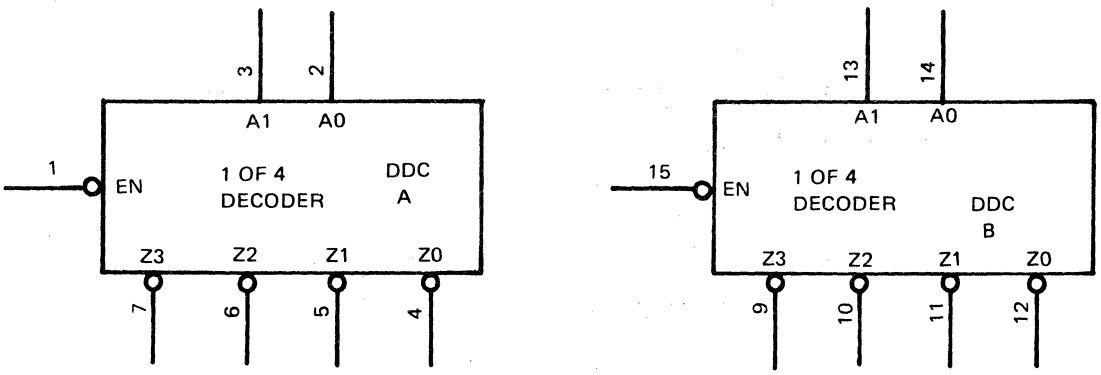
The one-shot multivibrator provides an output pulse whose duration and accuracy depends on external timing components connected to CEXT and REXT. The multivibrator has two trigger inputs, one active high (DA), and one active low (DB). This allows leading edge or trailing edge triggering. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the multivibrator and result in a continuous true output. A LOW level at the CLR input terminates the output pulse.

TRIGGERING TRUTH TABLE

DA	DB	CLR	Operation
L → H	H	H	Trigger
L	H → L	H	Trigger
X	X	L	Reset

H = High voltage level
L = Low voltage level
X = Irrelevant
H → L = High to low voltage level transition
L → H = Low to high voltage level transition

Figure E-2. Dual One-Shot Multivibrator (7903777)



GROUND PIN – 08

VOLTAGE PIN – 16

PIN NAMES

EN	Enable Inputs (Active Low)
A1, A0	Inputs
Z3, Z2, Z1, Z0	Outputs (Active Low)

DESCRIPTION

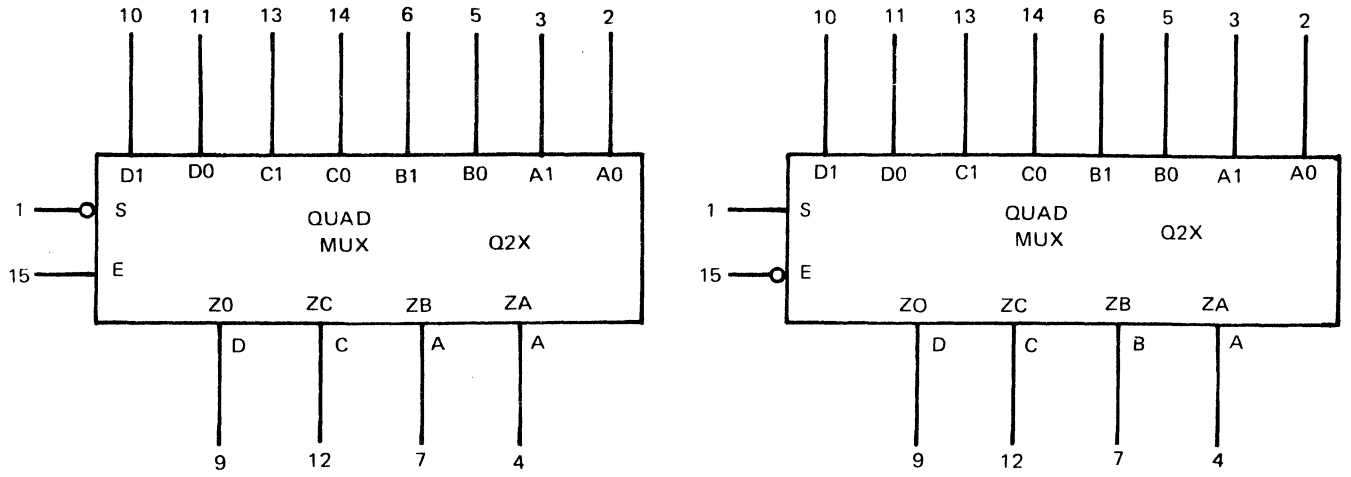
This decoder consists of two independent one-of-four decoders, each with an active low enable. The two bit input code is translated into one-of-four mutually exclusive active low outputs. The active low enable must be present to permit any output to be low.

TRUTH TABLE

	INPUTS		OUTPUTS			
EN	A1	A0	Z3	Z2	Z1	Z0
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-3. Dual One-of-Four Decoder (7903779)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

SEL	Common Select Input
EN	Enable Input (Active Low)
(A, B, C, D,)'s	Inputs
Z's	Outputs

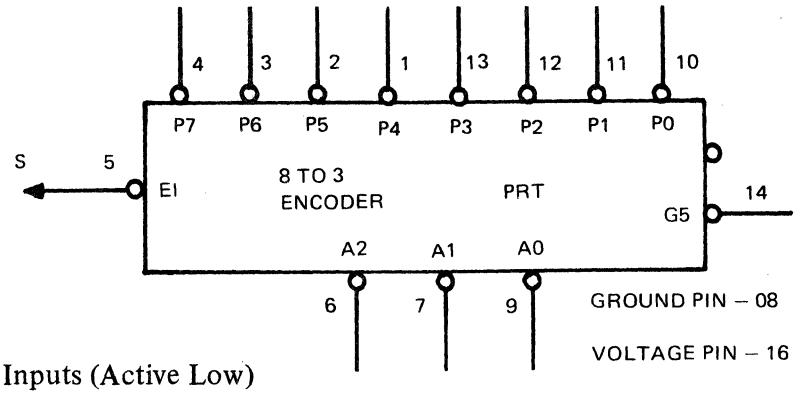
DESCRIPTION When the enable is low, this device selects 1 of 2 bits of data from each of four sources. Selection is determined by the condition of the SEL (select) input.

TRUTH TABLE FOR ONE BIT

EN	SEL	ZA
H	X	L
L	L	A0
L	H	A1

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-4. Quad Two-Input Multiplexer (7903780)



PIN NAMES

A0 – A7	Priority Inputs (Active Low)
EN IN	Enable Input (Active Low)
EN OUT	Enable Output (Active Low)
GS	Group Select Output (Active Low)
Z0, Z1, Z2	Address Output (Active Low)

DESCRIPTION

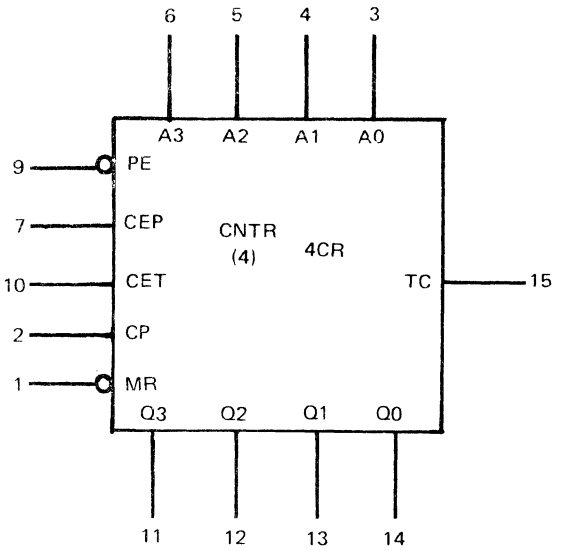
This integrated circuit accepts 8 active low inputs and produces a binary weighted output code of the highest priority input. A priority is assigned to each input such that when two or more inputs are active lows, the input with the highest priority is represented on the output. The order of priority is A7 first, A6 next, - - - -A0 last. The active low input and output enables provide the capability to expand a priority scheme to more inputs. This is accomplished by connecting the output enable of the highest priority network to the input enable of the next highest priority network.

TRUTH TABLE

EN IN	A7	A6	A5	A4	A3	A2	A1	A0	GS	Z2	Z1	Z0	EN OUT
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	X	X	X	X	X	X	X	L	L	L	L	H
L	H	L	X	X	X	X	X	X	L	L	L	H	H
L	H	H	L	X	X	X	X	X	L	L	H	L	H
L	H	H	H	L	X	X	X	X	L	L	H	H	H
L	H	H	H	H	L	X	X	X	L	H	L	L	H
L	H	H	H	H	H	L	X	X	L	H	L	H	H
L	H	H	H	H	H	H	L	X	L	H	H	L	H
L	H	H	H	H	H	H	H	L	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-5. Eight-Input Priority Encoder (7903781)



PIN NAMES

PE	Parallel Enable (Active Low) Input	MR	Master Reset (Active Low)
CEP	Count Enable Parallel Input	Q0, Q1, Q2, Q3	Parallel Outputs
CET	Count Enable Trickle Input	TC	Terminal Count Outputs
CP	Clock Pulse (Active High Going Edge) Input	A0, A1, A2, A3	Parallel Inputs

DESCRIPTION

This integrated circuit contains a high speed binary counter. The clock pulse drives four two-stage flip-flops in parallel through a clock buffer. During the low to high transition of the clock, the first stage is inhibited from further change. After the first stage is locked out, data is transferred from the first stage to the second stage and reflected at the outputs. When the clock is high, the first stage is inhibited and the data path between the first and second stage remains open. During the high to low transition of the clock, the second stage is inhibited from further change, followed by the enabling of the first stage for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, PE, CEP, and CET select the mode of operation as shown in the table below.

FUNCTION TABLE

PE	CEP	CET	MODE
L	X	X	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

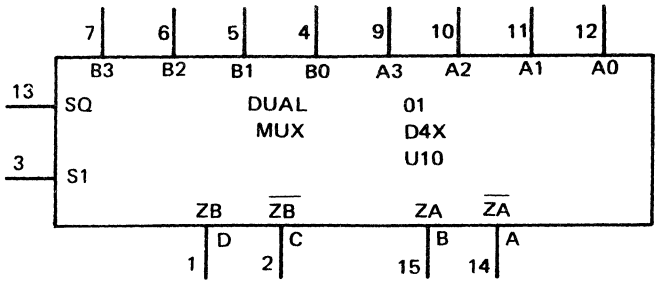
TRUTH TABLE

CET	$Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-6. High Speed Synchronous Four-Bit Binary Counter (7903782)



PIN NAMES

SEL 0, 1	Common Select Inputs
(A, B,)'s	Data Inputs
Z's	Outputs
$\overline{Z}$'s	Complementary Outputs

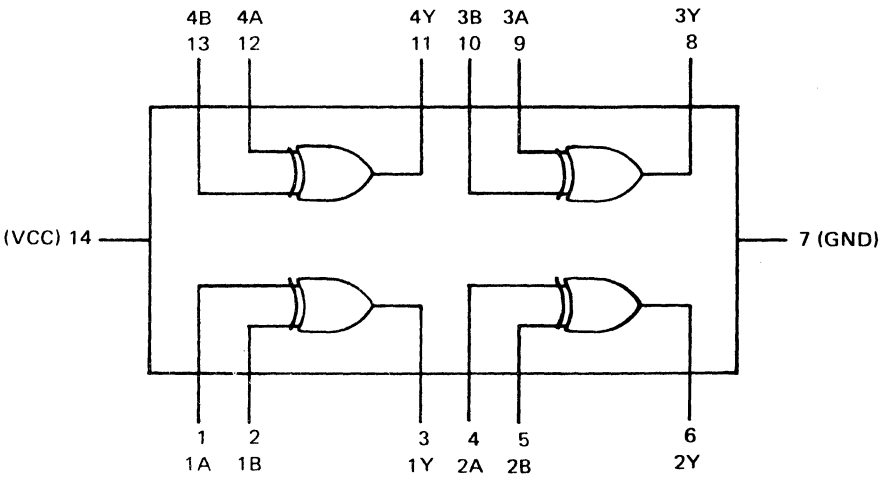
DESCRIPTION This integrated circuit selects one of four bits of data from each of two different sources. It is normally used to select data bits from one of four registers.

TRUTH TABLE

	SEL1	SEL0	ZB	$\overline{ZB}$	ZA	$\overline{ZA}$	INPUT PINS ENABLED
(00)	L	L	B0	$\overline{B0}$	A0	$\overline{A0}$	4, 12
(01)	L	H	B1	$\overline{B1}$	A1	$\overline{A1}$	5, 11
(10)	H	L	B2	$\overline{B2}$	A2	$\overline{A2}$	6, 10
(11)	H	H	B3	$\overline{B3}$	A3	$\overline{A3}$	7, 9

H = High voltage level
L = Low voltage level

Figure E-7. Dual Four-Input Multiplexer (7903783)



$Y = A + B$
$Y \neq A \cdot B$

DESCRIPTION

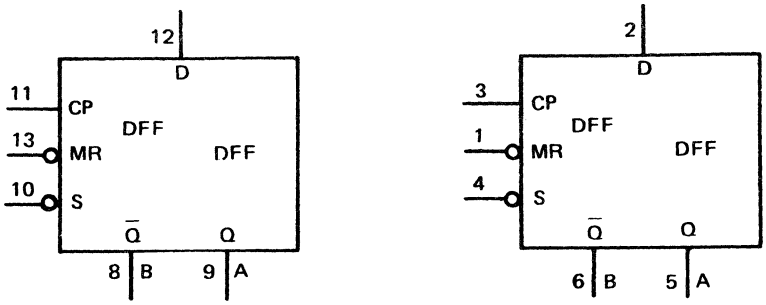
This integrated circuit contains four two-input exclusive OR gates. With an exclusive OR gate, a high on either input produces a high on the output, but a high on both inputs does not produce a high on the output, and neither does a low on both inputs.

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = Low voltage level
H = High voltage level

Figure E-8. Quadruple, Two-Input Exclusive OR (7903784)



GROUND PIN – 07
VOLTAGE PIN – 14

PIN NAMES

D	Input
CLK	Clock (leading positive edge)
MR	Master Reset (Active Low)
S	Set (Active Low)
Q	Output
$\overline{Q}$	Complementary Output

DESCRIPTION

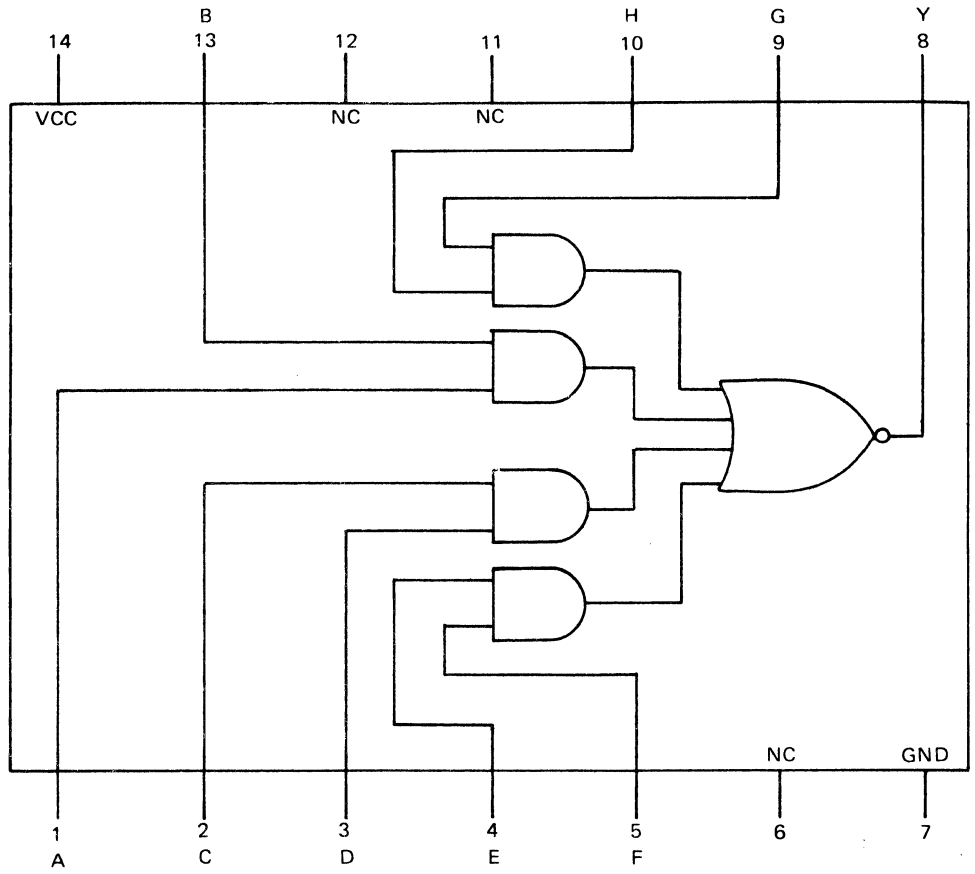
This integrated circuit contains two D type flip-flops with direct clear and set inputs and both Q and $\overline{Q}$ outputs. Information at the D input is transferred to the outputs on the positive edge of the clock pulse. The truth table shows the outputs for each input. The S and MR inputs are independent of the clock. A LOW on the S input sets Q to a HIGH. A LOW on the MR input sets Q to a low. A low on both inputs sets Q to a high and $\overline{Q}$ to a high.

TRUTH TABLE

INPUT	OUTPUTS	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = High voltage level
L = Low voltage level

Figure E-9. Dual D Flip-Flop (7903785)

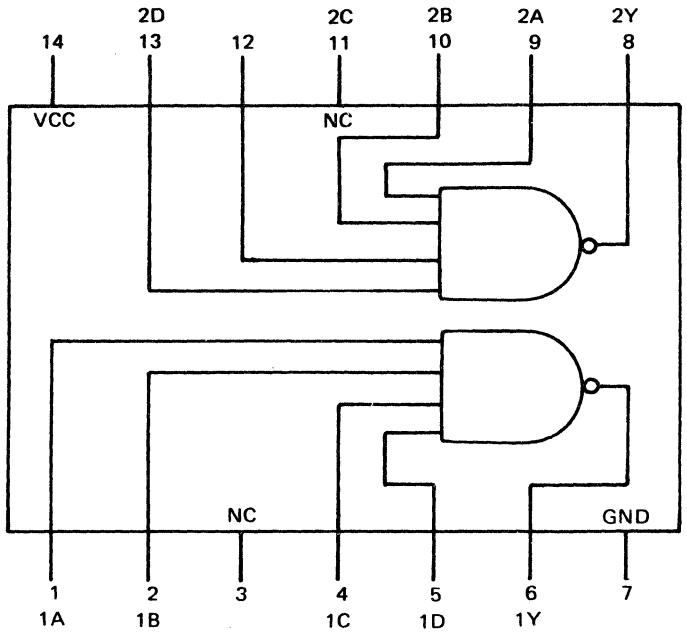


$\overline{Y}$ (LOW) = A · B + C · D + E · F + G · H

DESCRIPTION

This integrated circuit contains four two-input AND gates feeding an inverting OR gate. When any pair of inputs to the AND gates (A and B, or C and D, or E and F, or G and H) are high, the output of the OR gate (Y) is low.

Figure E-10. Four-Wide, Two-Input AND-OR Inverter (7903786)

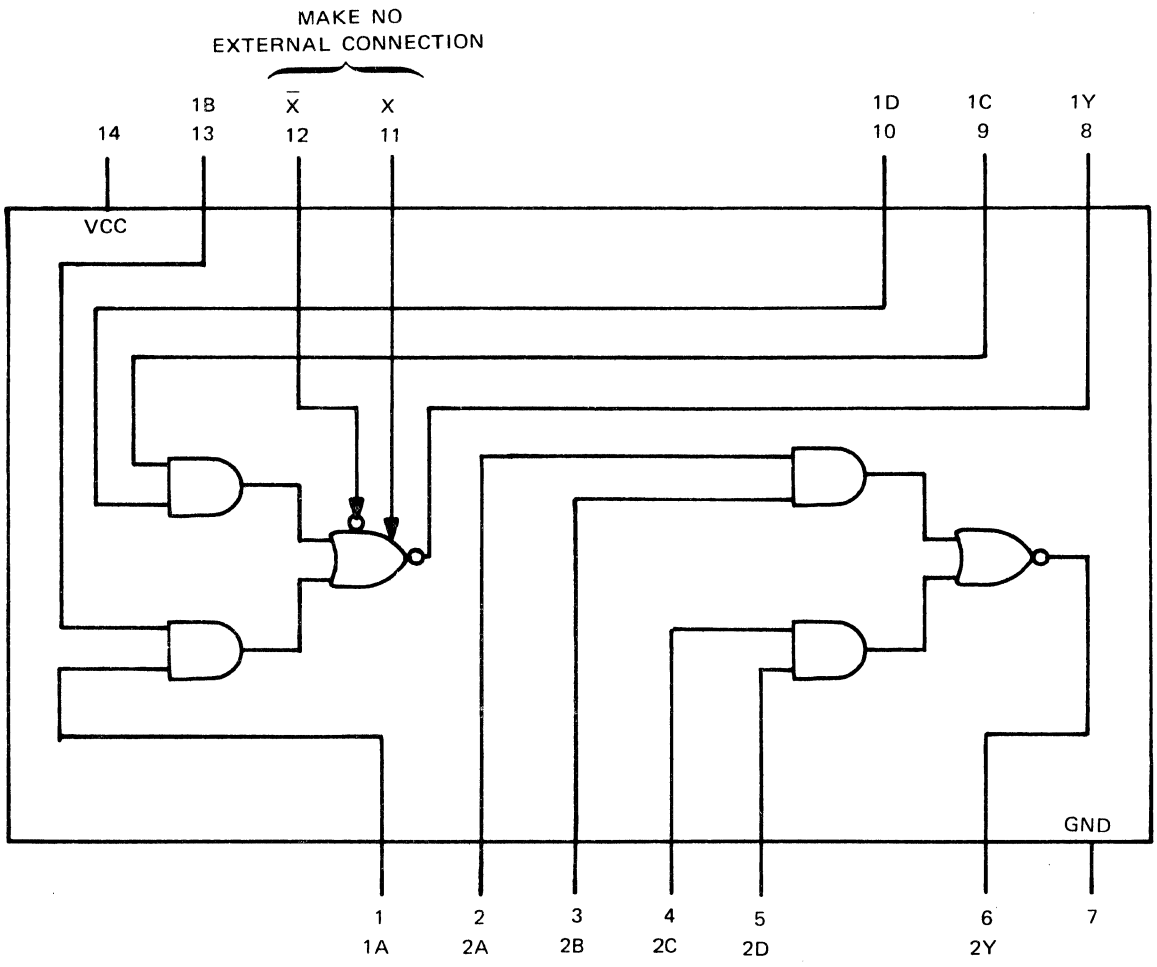


$\overline{Y}$ (LOW) = A · B · C · D

DESCRIPTION

This integrated circuit contains two four-input positive NAND gates. The NAND gate produces a low output (Y) when all four inputs (A, B, C, and D) are high.

Figure E-11. Buffer, Dual Four-Input Positive NAND (7903787)

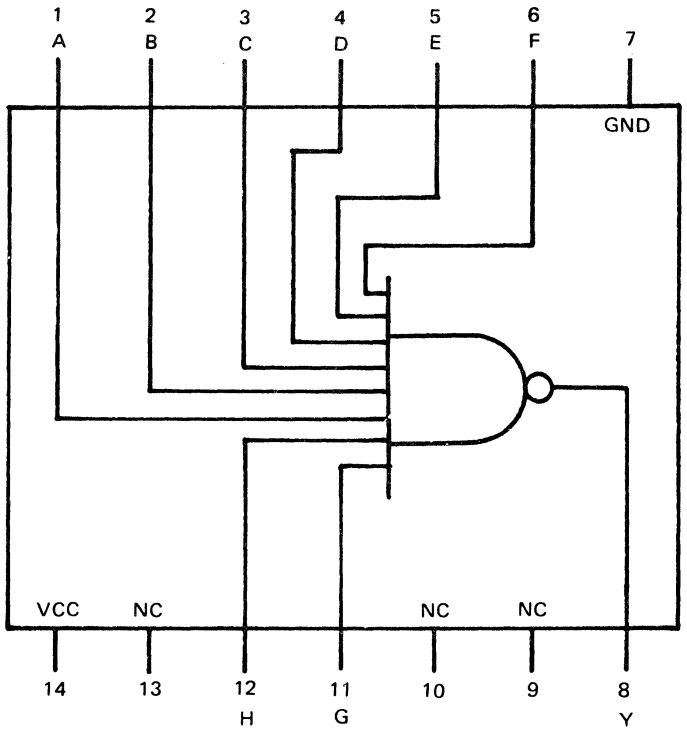


$\overline{Y}$ (LOW) = A · B + C · D

DESCRIPTION

This integrated circuit contains two two-input inverting OR gates. The inputs to each inverting OR gate are two two-input AND gates. The inverting OR gate output (Y) is low when both inputs (A and B or C and D) to either AND gate are high. The output is also low when all four inputs to the AND gates are high.

Figure E-12. Dual Two-Wide, Two-Input AND-OR Inverter (7903788)

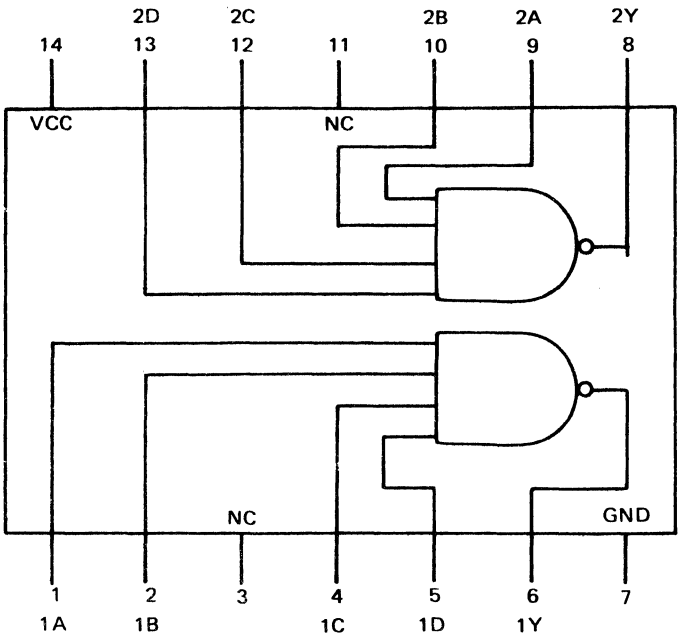


$\overline{Y}$ (LOW) = A · B · C · D · E · F · G · H

DESCRIPTION

This integrated circuit contains a positive eight input NAND gate. The output (Y) is low only when all eight inputs (A, B, C, D, E, F, G, and H) are high.

Figure E-13. Single Eight-Input Positive NAND (7903789)

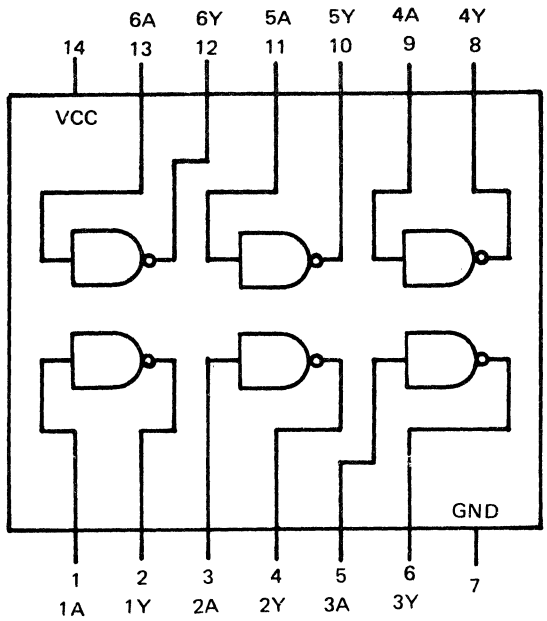


$\overline{Y}$ (LOW) = A · B · C · D

DESCRIPTION

This integrated circuit contains two four-input positive NAND gates. The output of the NAND gate (Y) is low when all four inputs (A, B, C, and D) are high.

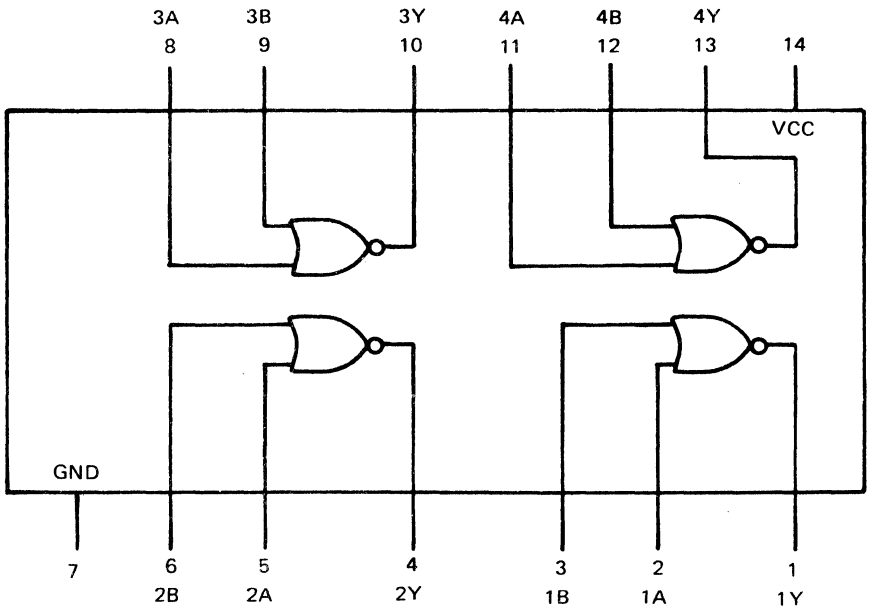
Figure E-14. Dual Four-Input NAND (7903790)



$\overline{Y}$ (LOW) = A

DESCRIPTION This integrated circuit contains six one-input inverting gates. The output (Y) is low when the input (A) is high. The output is high when the input is low.

Figure E-15. Inverter Gate, Hex, One-Input (7903791)



$\overline{Y}$ (LOW) = A + B

DESCRIPTION

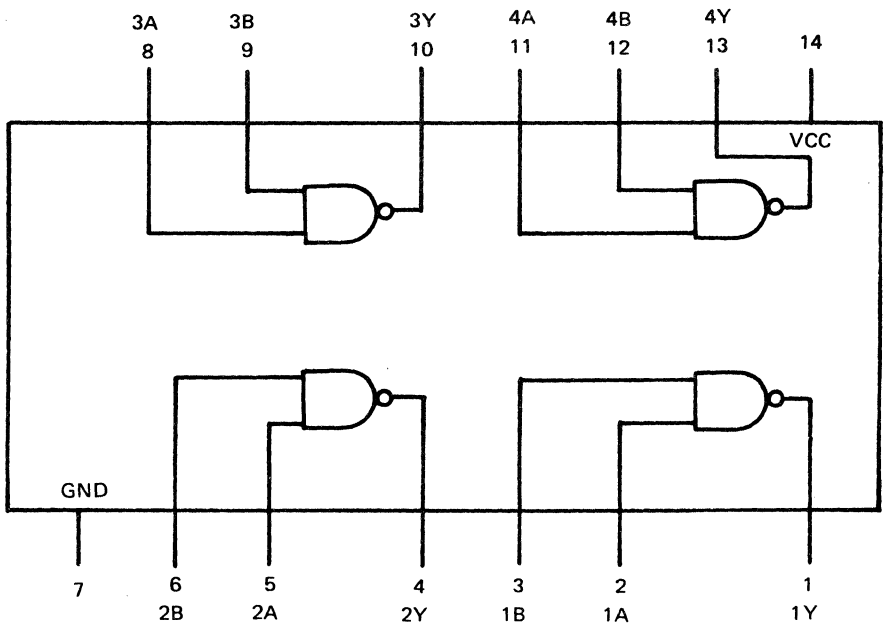
This integrated circuit contains four two-input positive NOR gates. The output (Y) is low when either or both inputs (A and B) are high.

TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

L = Low voltage level
H = High voltage level

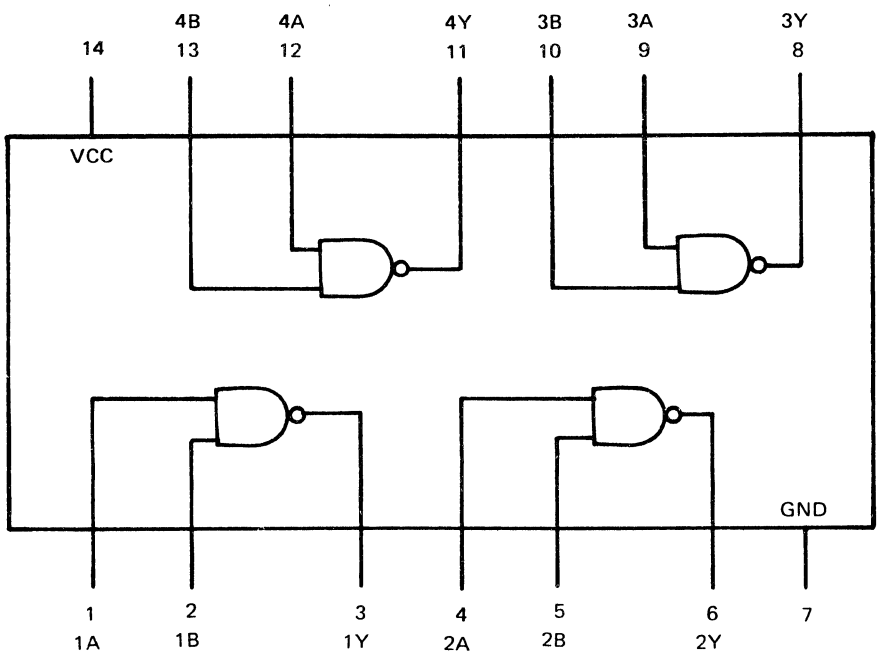
Figure E-16. Quadruple Two-Input Positive NOR (7903792)



$\overline{Y}$ (LOW) = A · B

DESCRIPTION This integrated circuit contains four two-input positive NAND gates. The output (Y) is low when both inputs (A and B) are high.

Figure E-17. Quadruple Two-Input NAND Gate with Open Collector Output (7903793)

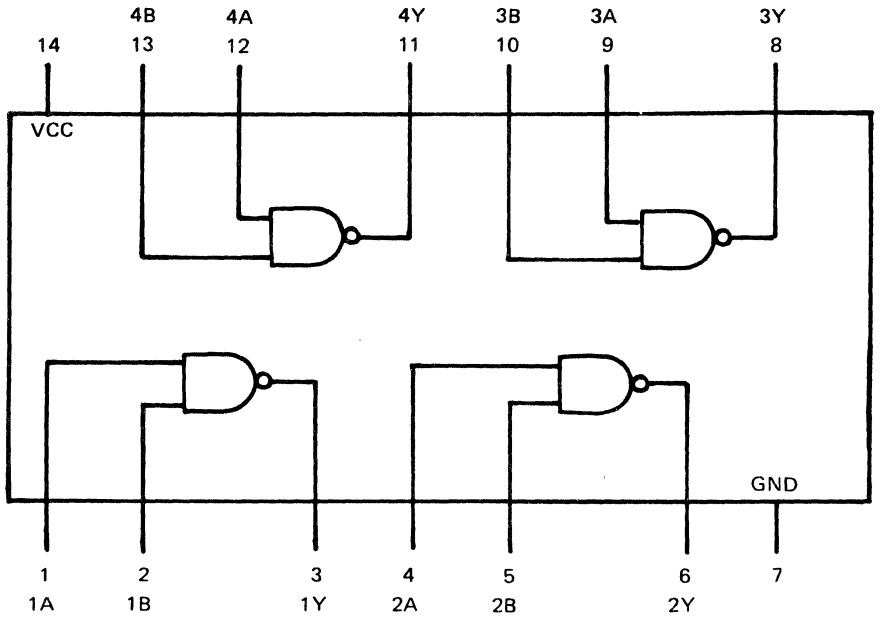


$\overline{Y}$ (LOW) = A · B

DESCRIPTION

This integrated circuit contains four two-input positive NAND gates. The output (Y) is low when both inputs (A and B) are high.

Figure E-18. Quadruple Two-Input Positive NAND (7903794)

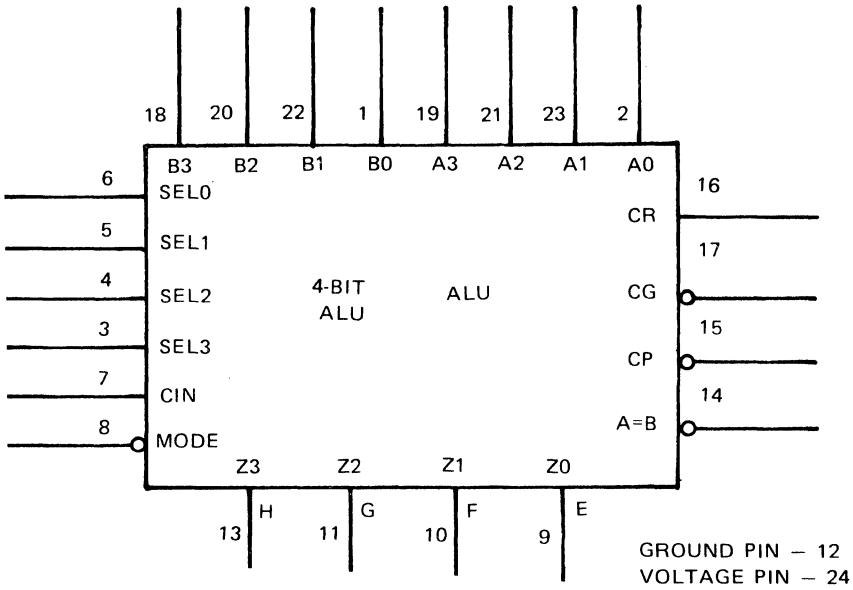


$\overline{Y}$ (LOW) = A · B

DESCRIPTION

This integrated circuit contains four two-input positive NAND gates. The outout (Y) is low when both inputs (A and B) are high.

Figure E-19. Quadruple Two-Input Positive NAND Buffer (7903795)



PIN NAMES

A3, A2, A1, A0	Word A Inputs
B3, B2, B1, B0	Word B Inputs
SEL 0 – SEL 3	Function Selection Inputs
CR IN	Carry Input
MODE	Mode Control Input (Active Low)
Z3, Z2, Z1, Z0	Function Outputs
CR	Ripple Carry Output
CR G	Carry Generate Output (Active Low)
CR P	Carry Propagate Output (Active Low)
A = B	Word A Equals Word B

DESCRIPTION

This integrated circuit is a 4-bit high-speed arithmetic logic unit capable of performing 16 different arithmetic operations and 16 different logical operations depending on the condition of the function selection inputs and the mode control inputs. The table shows the possible operations for the adder using active low inputs.

Larger (greater than 4-bit) adders can be built by cascading the less significant CR outputs to the more significant CR IN inputs. By using the CR G and CR P outputs in conjunction with the Carry Lookahead Device propagation time of the ripple carry is reduced.

A = B output goes high when outputs Z0-Z3 are high.

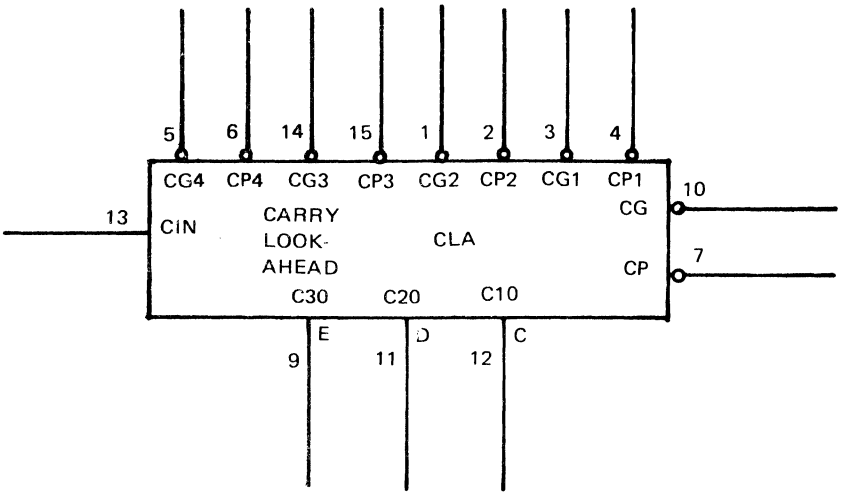
Figure E-20. Four-Bit Arithmetic Logic Unit (Adder) (7903799)

MODE SELECTION FOR ACTIVE LOW INPUT DATA

SELECTION				MODE=H	MODE=L ARITHMETIC MODE	
S E L 3	S E L 2	S E L 1	S E L 0	LOGIC MODE	CR IN = L (No Carry)	CR IN = H (With Carry)
L	L	L	L	F=$\overline{A}$	F=A MINUS 1	F=A
L	L	L	H	F=$\overline{AB}$	F=AB MINUS 1	F=A$\overline{B}$
L	L	H	L	F=$\overline{A+B}$	F=A$\overline{B}$ MINUS 1	F=A$\overline{B}$
L	L	H	H	F=1	F=MINUS 1 (2's comp)	F=ZERO
L	H	L	L	F=$\overline{A}$+B	F=A PLUS (A+$\overline{B}$)	F=A PLUS (A+$\overline{B}$) PLUS 1
L	H	L	H	F=$\overline{B}$	F=AB PLUS (A+$\overline{B}$)	F=AB PLUS (A+$\overline{B}$) PLUS 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A MINUS B MINUS 1	F=A MINUS B
L	H	H	H	F=A+$\overline{B}$	F=A+$\overline{B}$	F=(A+$\overline{B}$) PLUS 1
H	L	L	L	F=$\overline{A}$B	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H	L	L	H	F=A$\oplus$B	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	F=A$\overline{B}$ PLUS (A+B)	F=A$\overline{B}$ PLUS (A+B) PLUS 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) PLUS 1
H	H	L	L	F=0	F=A PLUS A	F=A PLUS A PLUS 1
H	H	L	H	F=A$\overline{B}$	F=A$\overline{B}$ PLUS A	F=A$\overline{B}$ PLUS A PLUS 1
H	H	H	L	F=AB	F=A$\overline{B}$ PLUS A	F=A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F=A	F=A	F=A PLUS 1

L = Low voltage level
H = High voltage level

Figure E-20. Four-Bit Arithmetic Logic Unit (Adder) (7903799) (Cont)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

CR IN	Carry Input
CG0 – CG3	Carry Generate Inputs (Active Low)
CP0 – CP3	Carry Propagate Inputs (Active Low)
C0, C1, C2	Carry Outputs
CR G	Carry Generate Output (Active Low)
CR P	Carry Propagate Output (Active Low)

DESCRIPTION

This integrated circuit is a high-speed lookahead carry generator. It is used with the 4-bit arithmetic logic unit to provide high-speed lookahead over word length of more than four bits. The lookahead carry generator accepts up to four pairs of Carry Propagate and Carry Generate signals and a Carry Input signal and provides anticipated carries (C0, C1, C2) across four groups of binary adders. The Carry Propagate and Carry Generate outputs are used for further levels of lookahead.

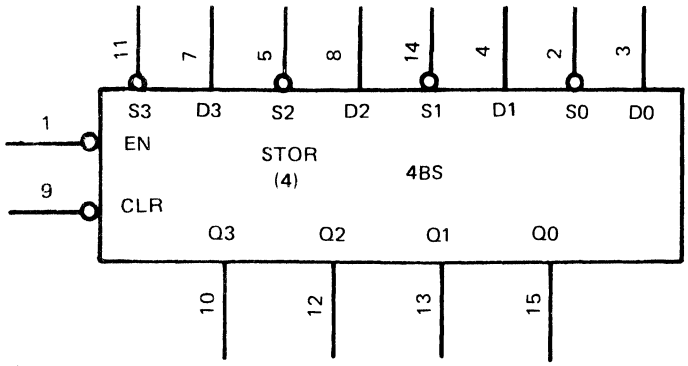
Figure E-21. Carry Lookahead Unit (7903800)

TRUTH TABLE

INPUTS									OUTPUTS				
CR IN	CG 0	CP 0	CG 1	CP 1	CG 2	CP 2	CG 3	CP 3	C 0	C 1	C 2	CRG	CRP
X	H	H							H				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

L = Low voltage level
H = High voltage level
X = Irrelevant

Figure E-21. Carry Lookahead Unit (7903800) (Cont)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

EN	Enable Input
D3 – D0	Parallel Data Inputs
S3 – S0	Set Inputs (Active Low)
CLR	Master Reset (Active Low)
Q3 – Q0	Parallel Outputs

DESCRIPTION

This integrated circuit is a 4-bit latch which can be used in applications where D type latches or set/reset latches are required.

When the common enable goes high, data present in the latches is stored and the state of the latches is no longer affected by the S and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

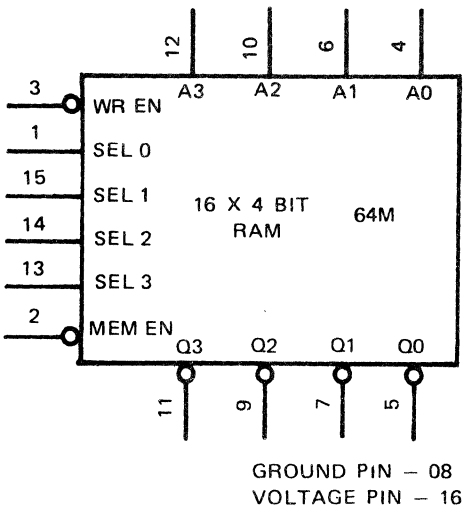
Each of the four latches can be operated either as an active low set/reset latch with reset override or, with S low, as a D type storage latch.

TRUTH TABLE

CLR	EN	D	S	QN	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	QN-1	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	QN-1	
H	H	X	X	QN-1	
L	X	X	X	L	RESET

H = High voltage level
L = Low voltage level
X = Irrelevant
QN-1 = Previous output state
QN = Present output state

Figure E-22. Four-Bit Latch (7903801)



PIN NAMES

SEL 3 – SEL 0	Address Inputs
A3 – A0	Data Inputs
MEM EN	Enable Selection (Active Low)
WR EN	Enable Writing of Data (Active Low)
Q3 – Q0	Outputs (Active Low)

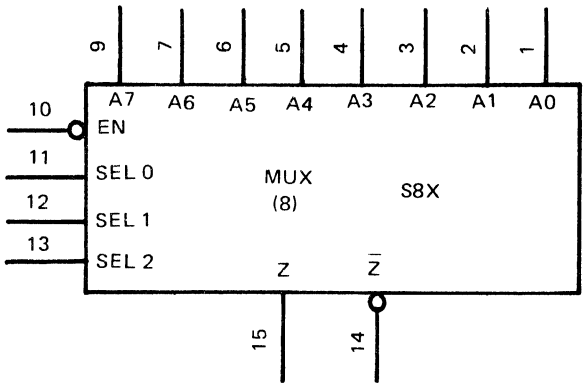
DESCRIPTION

This integrated circuit is a high-speed 64-bit read/write random access memory organized into 16 words of 4 bits.

When the WR EN is low, the data from the four A inputs is written into the memory location specified by the address formed by "SEL 3 – SEL 0."

When the MEM EN is low, the data from the memory location specified by the address (SEL 3 – SEL 0) is read and gated to the outputs.

Figure E-23. 64-Bit Memory Cell (7903802)



PIN NAMES

A7 – A0	Inputs
SEL 0, 1, 2	Select Inputs
EN	Enable Input (Active Low)
Z15	Output
Z14	Complementary Output

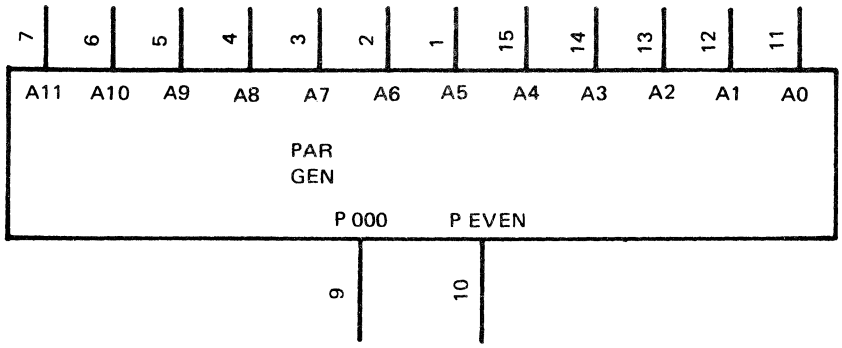
DESCRIPTION When the enable is low, this integrated circuit selects one bit of data from up to eight sources as determined by SEL inputs.

TRUTH TABLE

	EN	SEL 2	SEL 1	SEL 0	Z15	Z14
	H	X	X	X	L	$\overline{H}$
(000)	L	L	L	L	A0	$\overline{A0}$
(001)	L	L	L	H	A1	$\overline{A1}$
(010)	L	L	H	L	A2	$\overline{A2}$
(011)	L	L	H	H	A3	$\overline{A3}$
(100)	L	H	L	L	A4	$\overline{A4}$
(101)	L	H	L	H	A5	$\overline{A5}$
(110)	L	H	H	L	A6	$\overline{A6}$
(111)	L	H	H	H	A7	A7

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-24. Eight-Input Multiplexer (7903803)



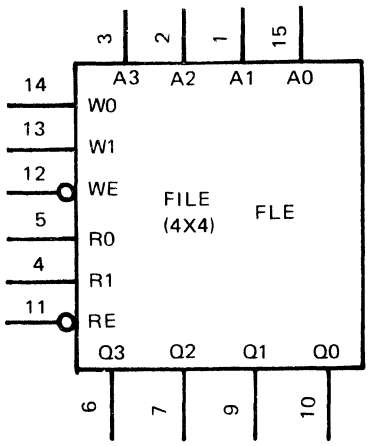
PIN NAMES

A11 – A0	Parity Inputs
P ODD	Odd Parity Output
P EVEN	Even Parity Output

DESCRIPTION

This device is a 12-bit parity checker/generator generating odd and even parity outputs. The even parity output will be high if an even number of inputs are high. The odd parity output will be high if an odd number of inputs are high.

Figure E-25. Parity Checker-Generator, SGL Twelve-Input (7903908)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A3 – A0	Inputs
W1, W0	Write Address Inputs
WE	Write Enable (Active Low)
R1, R0	Read Address Inputs
RE	Read Enable (Active Low)
Q3 – Q0	Outputs

DESCRIPTION

This integrated circuit contains 16 flip-flops used to hold four-bit words. The write address inputs (W1, W0) select the word location to store the data inputs (A3-A0). The data is gated to the selected location when the write enable (WE) is low. The read address inputs (R1, R0) select the word location to place on the data outputs (Q3-Q0). Data is gated to the outputs when the read enable (RE) is low.

TRUTH TABLES

WRITE FUNCTION

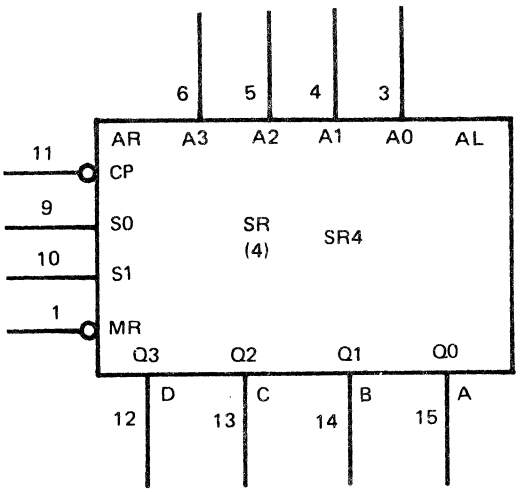
Inputs			Word Selected
W1	WO	WE	
L	L	L	Word 0
L	H	L	Word 1
H	L	L	Word 2
H	H	L	Word 3
X	X	H	No change

READ FUNCTION

Inputs			Outputs			
R1	RO	RE	Q3	Q2	Q1	Q0
L	L	L		Word	0	
L	H	L		Word	1	
H	L	L		Word	2	
H	H	L		Word	3	
X	X	H	H	H	H	H

H ≙ High voltage level
L = Low voltage level
X = Irrelevant

Figure E-26. 4 X 4 Register File (7904135)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A3 – A0	Parallel Data Inputs	S0, S1	Mode Selection Inputs
AL	Shift Left Serial Input	CLR	Master Reset Input (Active Low)
AR	Shift Right Serial Input	Q3 – Q0	Parallel Data Outputs
CLK	Clock Input (Active Low)		

DESCRIPTION

This integrated circuit is a 4-bit shift register with four modes of operation; parallel load, shift left, shift right, and hold. The mode of operation is determined by the mode selection inputs (S0, S1) as shown in the truth table. Data is loaded or shifted by the negative going edge of the clock pulse. For a left shift operation, data is shifted in the direction of Q3 toward Q0 with the contents of Q0 shifted off and the serial input (AL) loaded into Q3. For a right shift operation, data is shifted in the direction of Q0 toward Q3 with the contents of Q3 shifted off and the serial input (AR) loaded into Q0.

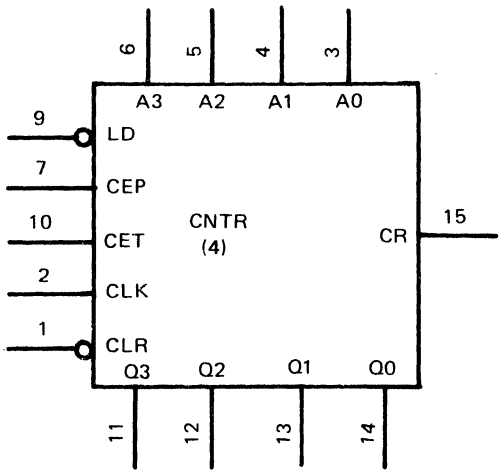
The master reset (active low) forces all outputs low.

MODE SELECTION

Inputs			Mode
CLR	S1	S0	
H	H	H	Parallel Load
H	L	H	Shift Right (in direction Q0 toward Q3)
H	H	L	Shift Left (in direction Q3 toward Q0)
H	L	L	Hold (inhibit clock)
L	X	X	Reset

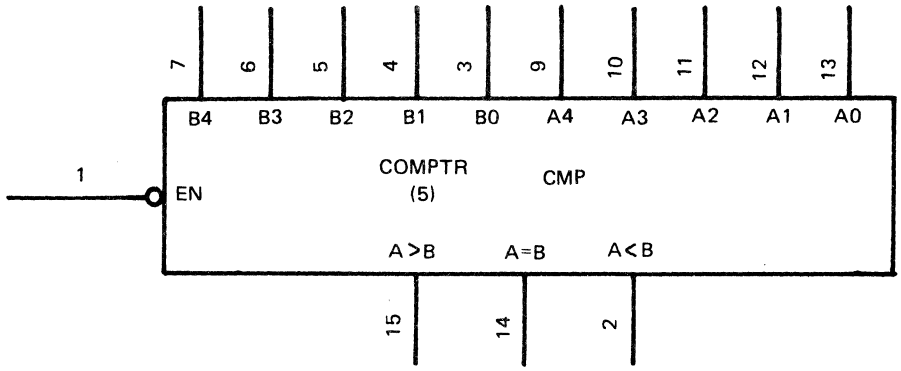
L = Low voltage level
H = High voltage level
X = Irrelevant

Figure E-27. Shift Register (7904136)



DESCRIPTION Reference Figure E-6 (7903782).

Figure E-28. Four-Bit Binary Counter (7904137)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A4 – A0	Word A Parallel Inputs
B4 – B0	Word B Parallel Inputs
EN	Enable Input (Active Low)
A > B	A Greater than B Output
A < B	A Less Than B Output
A=B	A Equal to B Output

DESCRIPTION

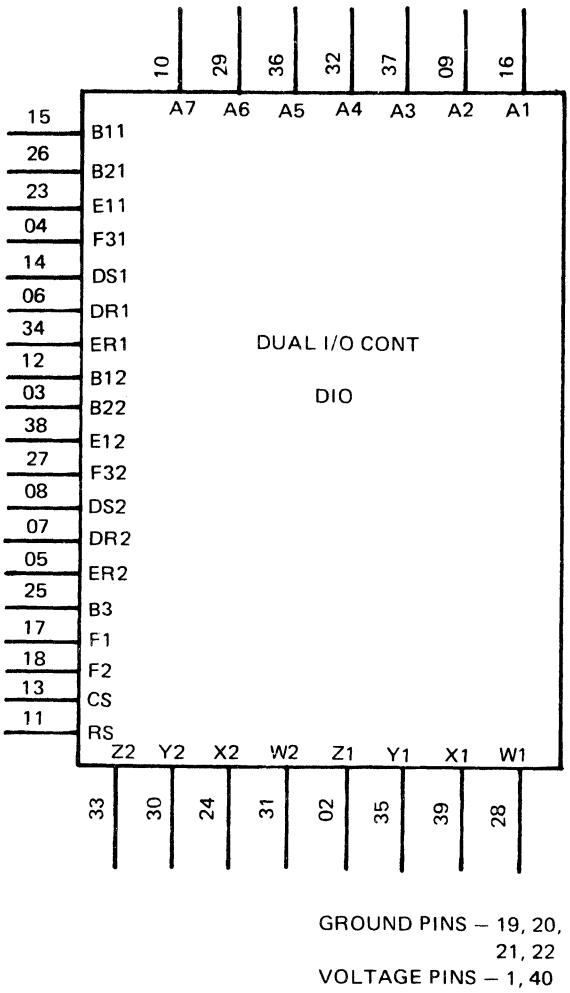
This circuit compares two 5-bit words and provides three outputs, "less than," "greater than," and "equal to." The A4 and B4 inputs are the most significant inputs and A0, B0 are the least significant. All three outputs are activated by a low enable input (EN). Connecting the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

TRUTH TABLE

EN	Word A		Word B	A>B	A < B	A=B
H	X		X	L	L	L
L	Word A	>	Word B	H	L	L
L	Word A	<	Word B	L	H	L
L	Word A	=	Word B	L	L	H

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure E-29. Five-Bit Comparator (7904164)



DESCRIPTION

This integrated circuit provides the control flip-flops (active, monitor, force, and one-shot) and associated circuits for control of one input/output channel. See accompanying schematic drawing, Figure E-31.

Figure E-30. Dual Input/Output Control Circuit (7904199)

LEGEND:

INPUTS

17	H ⇒ SCAN INT	4	H ⇒ REG $\overline{\text{AVAIL}}$ CHAN
16	L ⇒ CLR MONITOR	32	L ⇒ **SET FORCE**
11	L ⇒ MASTER CLEAR	36	L ⇒ **SET ACTIVE** 2
9	L ⇒ SET MONITOR	14	L ⇒ ID CHAN
26	PIN 39 INVERTED	34	L ⇒ ODR + EFR (JUMPERED FROM 35)
37	L ⇒ CLR MONITOR	6	H ⇒ IDR, CHAN X
15	L ⇒ EI, CHAN X	12	L ⇒ EF CHAN X
13	L ⇒ CHAN X SELECT	27	(NOT USED)
29	L ⇒ SET ACTIVE	38	H ⇒ EFR CHAN X
25	H ⇒ INT SCAN EN	3	(NOT USED)
10	L ⇒CLR ONE SHOTS	8	L ⇒OD
23	H ⇒ EIR CHAN X	5	(NOT USED)
18	L ⇒INPUT DATA AVAIL GRP 1	7	H ⇒ ODR CHAN X

OUTPUTS

31	L ⇒ EIE, CHAN X
29	L ⇒ EIR, CHAN X
33	L ⇒ DATA + CHAIN, CHAN X
30	(NOT USED)
28	(NOT USED)
39	INVERTED AND JUMPERED TO PIN 26
35	L ⇒ ODR + EFR (JUMPERED TO 34)
2	L ⇒ EF/OD CHAN

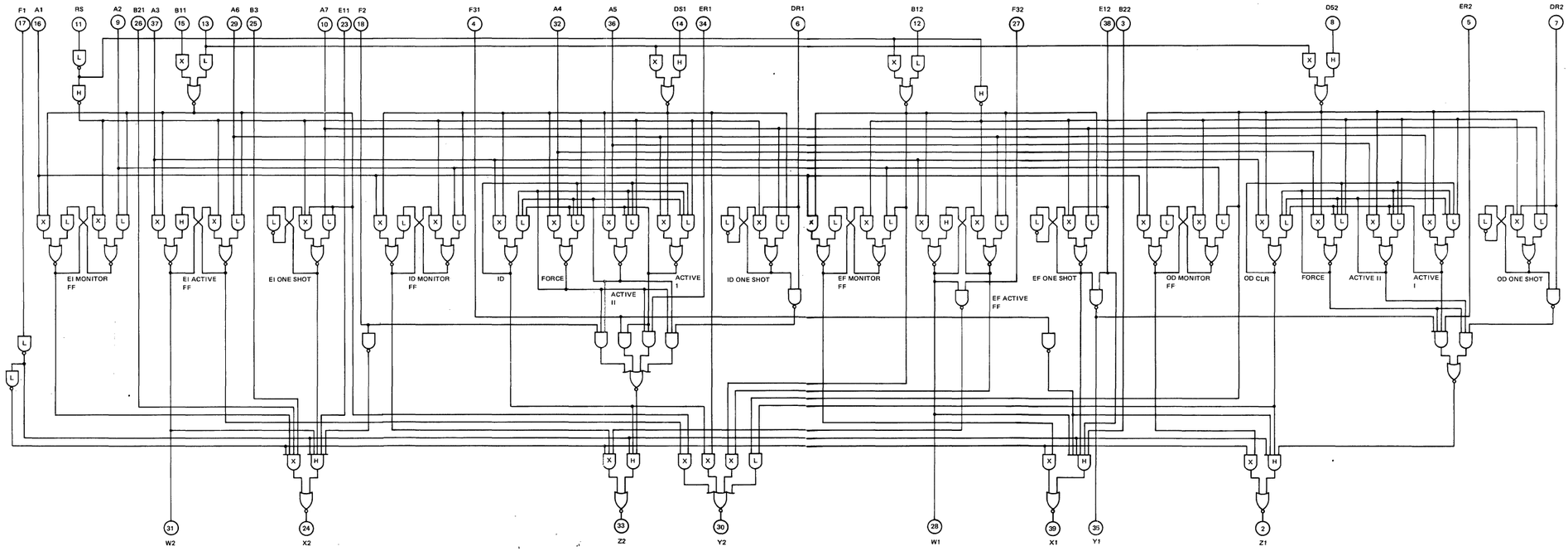
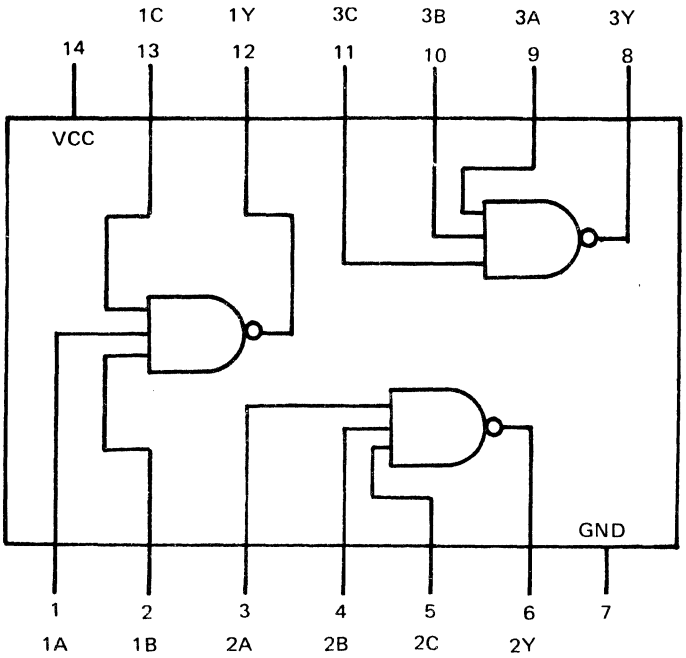


Figure E-31. Dual Input/Output Control Circuit (7904199) Schematic Drawing

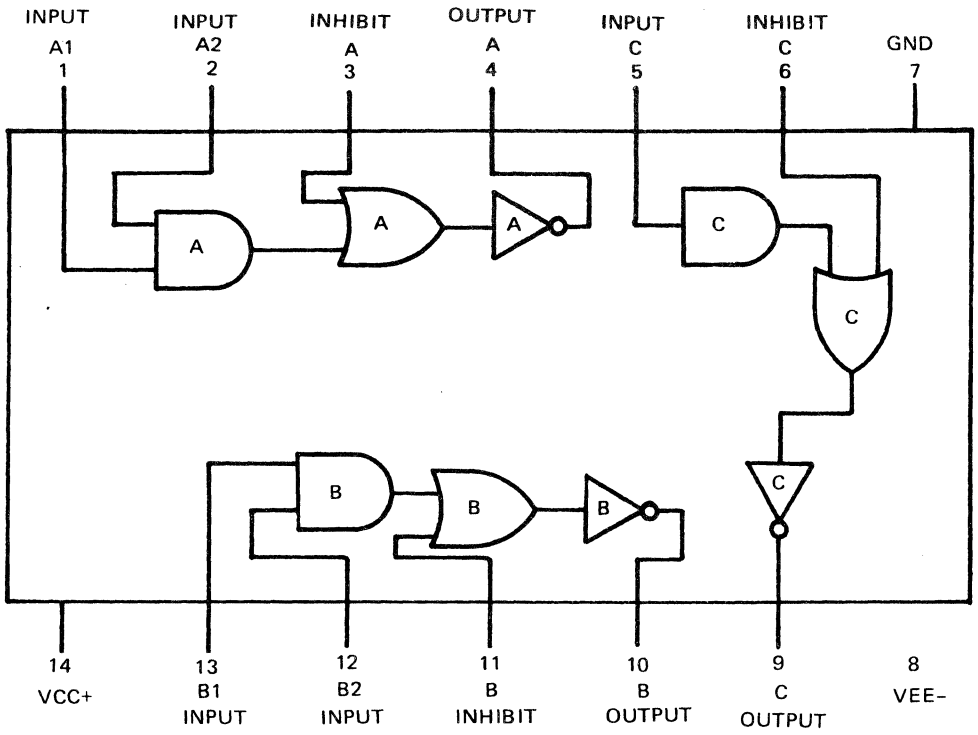


$\overline{Y}$ (LOW) = A · B · C

DESCRIPTION

This integrated circuit contains three three-input positive NAND gates. The output (Y) is low when all three inputs (A, B, and C) are high.

Figure E-32. Triple Three-Input Positive NAND (7904221)



DESCRIPTION

This integrated circuit contains three line driver circuits. Two of the circuits (A and B) contain a line driver whose input is a two-input OR gate. One input to the OR gate is a two-input AND gate, the other input is a straight input. The third line driver circuit (C) consists of a line driver whose input is a two-input OR gate. One input of the OR gate is a one-input AND gate, and the other input is a straight input. The output conditions can be seen in the two truth tables.

The line driver circuit converts TTL/DTL logic levels to EIA/CCITT levels for transmission between data terminal equipment and data communication equipment.

TRUTH TABLE FOR CIRCUITS A AND B

INPUT 1	INPUT 2	INHIBIT	OUTPUT
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

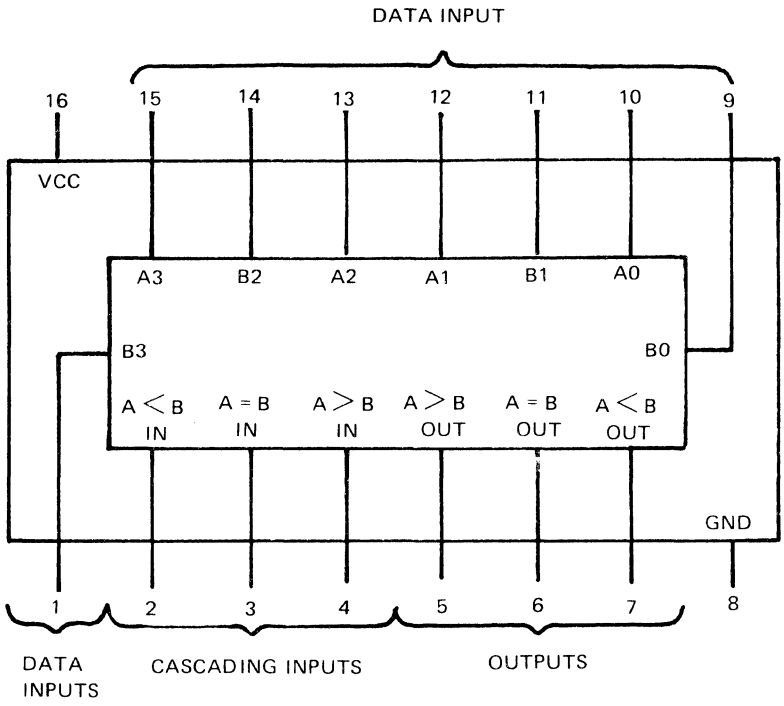
TRUTH TABLE FOR CIRCUIT C

INPUT	INHIBIT	OUTPUT
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level

L = Low voltage level

Figure E-33. Triple Line Driver (7904224)



DESCRIPTION

This unit performs magnitude comparison of straight binary and straight binary coded decimal (BCD) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs.

TRUTH TABLE

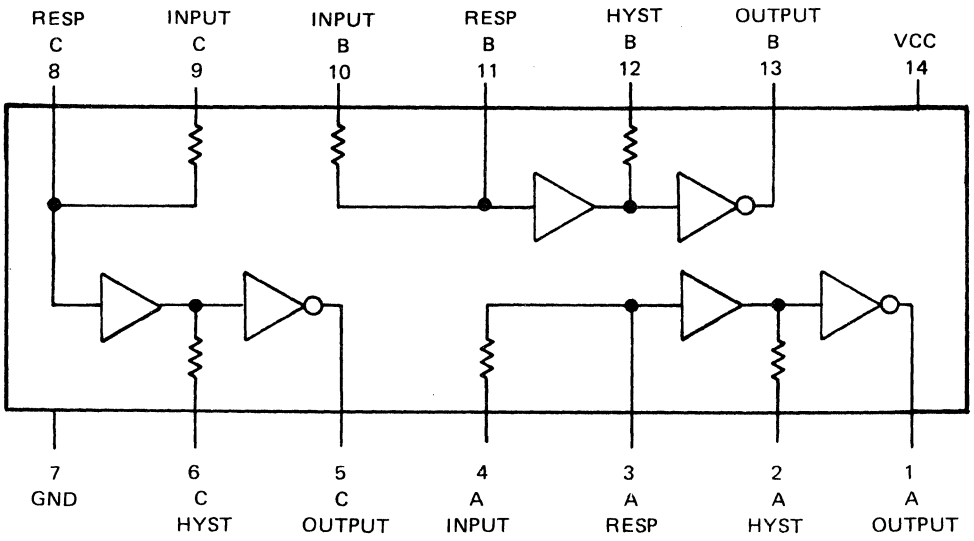
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H

H = High voltage level

L = Low voltage level

X = Irrelevant

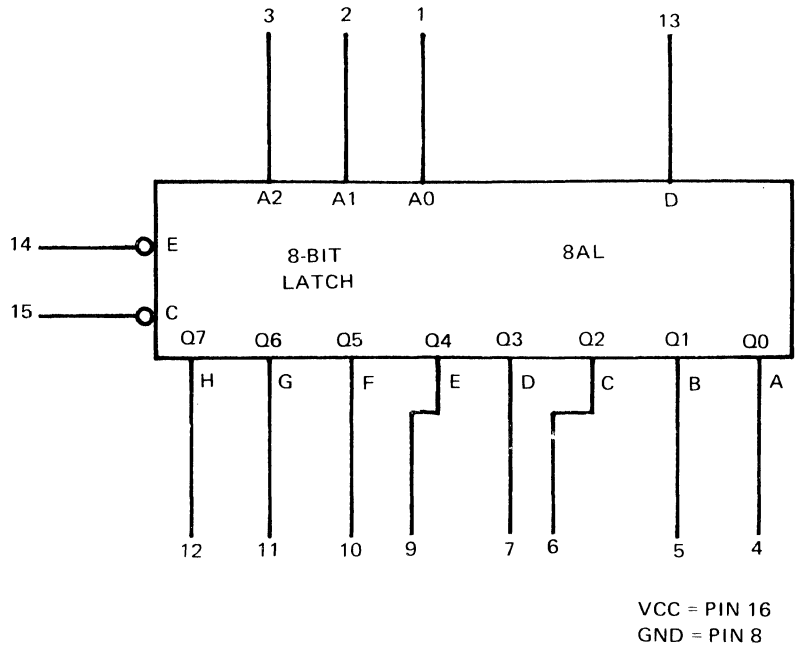
Figure E-34. Comparator, Four-Bit Magnitude (7904225)



DESCRIPTION

This integrated circuit is a triple line receiver circuit. It receives EIA/CCITT signals and converts them to TTL logic levels. The input voltage can be between +25 volts and -25 volts. Each of the three receivers can operate in either hysteresis or non-hysterisis mode, and provides fail-safe operation.

Figure E-35. Triple Line Receiver (7904226)



DESCRIPTION

This integrated circuit contains an eight-bit addressable latch. It has four modes of operation. In the addressable latch mode, data on the data line (D) is written into the addressable latch. The addressable latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. In the one-of-eight decoding or demultiplexing input mode, the addressed output will follow the state of the D input with all other outputs in the low state. In the clear mode, all outputs are low and unaffected by the address and data inputs. The selection of the four modes is shown in the Mode Selection table.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

Figure E-36. Eight-Bit Addressable Latch (7904227)

TRUTH TABLE

PRESENT OUTPUT STATES														
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.		.					.					
.	.	.		.					.					
.	.	.		.					.					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
.	.	.		.				.						
.	.	.		.				.						
.	.	.		.				.						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

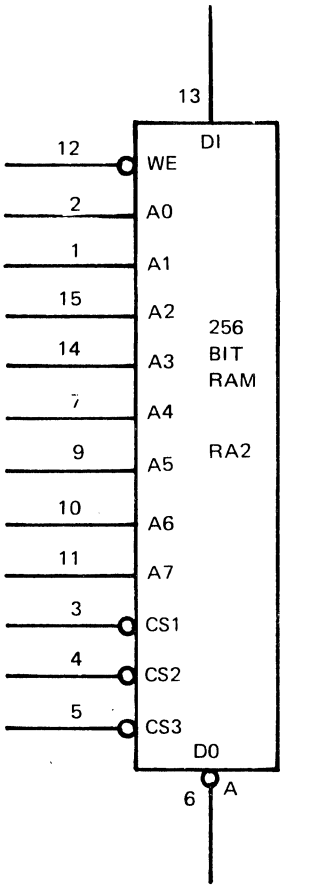
X = Irrelevant

L = Low Voltage Level

H = High Voltage Level

Q_{N-1} = Previous Output State

Figure E-36. Eight-Bit Addressable Latch (7904227) (Cont)



GROUND PIN – 08
VOLTAGE PIN – 16

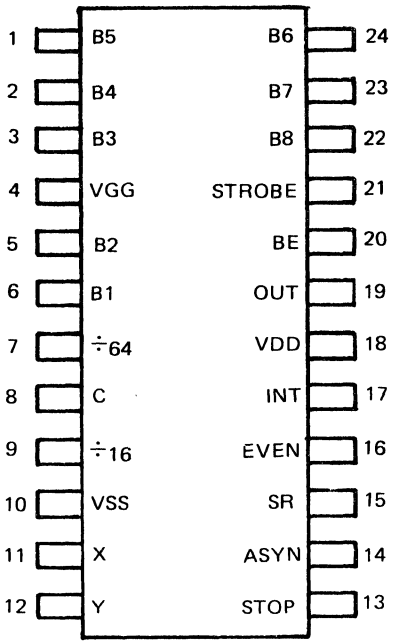
PIN NAMES

DI	Data Input
WE	Write Enable
A0 – A7	Address Input
CS1 – CS3	Memory Enable
DO	Data Output

DESCRIPTION

This device is a Read/Write memory with 256 addressable bits. The chip (memory) is enabled when all memory enable inputs are low. The read and write operations are controlled by the write enable when the chip is enabled. When the WR EN is low, the DI is written into the bit location addressed by inputs A0 through A7. When the WR EN is high, the bit location addressed by A0 through A7 is read out and placed on the output (DO) as the complement of the data written into memory.

Figure E-37. 256-Bit Random Access Memory (7904274)



DESCRIPTION

ASYNCHRONOUS OPERATION

The terminal transmitter maintains an output condition of continuous Mark bits (logic "1" or high level) in between the transmission of characters. The reset signal forces the transmitter into this mode of operation for a minimum of one character time. This state (continuous "marks" being applied to the output line) may be termed the "idling condition."

Data is presented to the buffer storage register by means of the data inputs from the system of which the terminal transmitter is a part. This data is in the form of a character with a bit length between 5 and 8 bits. The character bit length (excluding control bits such as Start and Stop bits) is defined by the Word Length Selector input. Parity is included in the total number of bits making up the word length if it is being utilized in transmission. The input data (when stable) is strobed into the buffer register by means of the Load Strobe. The Buffer Empty output line indicates that new data is in the buffer and that the system can apply a low level to the $\overline{\text{System Ready}}$ line. This low level signal enables the transfer timing logic, which clears all functional blocks except the buffer storage register, and then automatically causes a transfer of the buffer data into the shift register.

The new character (just transferred into the shift register) is automatically preceded by a Start bit (a space or logic "0") and serially transmitted to the modem as an NRZ waveform at the programmed bit rate. The internal timing counter keeps track of the character position in the shift register, provides timing control to the sequence control logic for insertion of parity (if internal parity is selected) into the last bit position of the character, and adds the Stop bit or bits. The number of Stop bits being added is determined by the 2nd Stop Bit Selector line which specifies one or two Stop bits. The transmission of the character and control bits (Start and Stop bits) is now complete, and the sequence control logic either returns the transmitter to the "idling condition" and places Marks on the output line or begins a new cycle. The new cycle automatically begins if a new character has been strobed into the buffer storage register (Buffer Empty output is low) and a low level is applied to the $\overline{\text{System Ready}}$ line.

The bit rate of the transmitted data is determined by the input frequency of the clock at the oscillator input and by the divide ratio of the counter in the internal clock generator. Three counter ratios are available: ÷1, ÷16 and ÷64. These provide compatibility with the oscillator required for the terminal receiver. The chip reset is achieved

Figure E-38. P-Channel MOS Terminal Transmitter (7904275)

when both the ÷16 Enable and the ÷64 Enable are high. The reset function will clear the internal counters and shift register to prevent extraneous data from being placed upon the output line.

SYNCHRONOUS OPERATION

Data is presented to the buffer storage register by means of the data inputs from the system of which the terminal transmitter is a part. This data is in the form of a character with a bit length between 5 and 8 bits. The character bit length (including parity if applicable) is defined by the Word Length Selector input. The input data is strobed into the buffer register by means of the Load Strobe and the Buffer Empty output line then indicates that new data is in the buffer. When the last bit of the previous character is placed on the output line, the transfer timing logic clears all functional blocks except the buffer storage register and then automatically causes a transfer of the buffer data into the shift register. The new character (just transferred into the shift register) is serially transmitted to the modem as an NRZ waveform at the programmed bit rate. The internal timing counter keeps track of the character position in the shift register and provides timing control to the sequence control logic for insertion of parity (if internal parity is selected) into the last bit position of the character. The last bit of the character is now present at the output and sequence control logic will initiate a new cycle automatically. The new cycle results in the transmission of the next character if a new character has been strobed into the buffer storage register (Buffer Empty output is low) or a character length of all Marks if no new character has been stored. Thus, character sync is maintained even though an interruption appears in the data stream.

The bit rate of the transmitted data is determined by the input frequency of the clock at the oscillator input and by the divide ratio of the counter in the internal clock generator. Three counter ratios are available: ÷1, ÷16 and ÷64. These provide compatibility with the oscillator required for the terminal receiver. The chip reset is achieved when both the ÷16 Enable and the ÷64 Enable are high. The reset function will clear the internal counters and shift register to prevent extraneous data from being placed upon the output line.

INPUTS

Data Inputs – Characters of differing bit lengths (from 5 to 8 bits including parity bit, if desired) may be entered in parallel in right justified bit positions by means of the eight Data Inputs. The data is strobed into a set of buffer latches where it is stored until transmitted. Unused Data Inputs must be maintained in the high state. (There is no inversion of the data within the circuit; therefore a high input will be transmitted as a high output.)

Load Strobe – A high level on the Load Strobe transfers the input character on the Data Inputs into the Storage Buffer latches and resets the Buffer Empty latch.

Internal Parity – A high level applied to the Internal Parity input causes the transmitter Parity Generator to replace the trailing bit of a character of any selected word length with an internally generated parity bit. A low level causes the trailing bit to be transmitted as loaded from the inputs.

Even Parity – When a high level is applied to both the Internal Parity and the Even Parity inputs, the Parity Generator places the proper bit value in the trailing bit position of a character to insure that the total number of high levels is even. Odd parity is formed by using a low level on the Even Parity input.

2nd Stop Bit Select – A high level on the Stop Bit Select input causes two STOP bits to be transmitted in the asynchronous mode. A low level will cause one STOP bit to be transmitted. This function is disabled in the synchronous mode.

tion of START and STOP bits, and causes MARK bits to appear on the output terminal between the transmission of characters. A low level on this line shortens the word length by the two or three control bits (START, STOP) and allows for automatic recycling to either transmit the next character or a character length of MARK bits.

System Ready – This input allows control of the device by the external system. A low level releases

Figure E-38. P-Channel MOS Terminal Transmitter (7904275) (Cont)

Asynchronous Mode – A high level on the Asynchronous Mode input enables the device for operation in the asynchronous mode, causes the genera- the transmitter for the next transmission cycle. This signal is normally applied after the Buffer Register has been loaded (Buffer Empty output is low). The low level should be maintained until the next cycle is initiated (the Buffer Empty output goes high), then made high until the next Data Strobe.

External Clock – This is the oscillator input that controls the transmission rate of the Terminal Transmitter.

Word Length Selector – Two inputs (X, Y) define the character bit length. The following truth table defines the character length for each input combination. (Unused Data Inputs must be maintained in the high state. This may be accomplished by leaving the unused inputs open.)

X	Y	WORD LENGTH
1	1	8 bits
0	1	7 bits
1	0	6 bits
0	0	5 bits

÷16 and ÷64 Counter Enables – These two Enable inputs provide compatibility with the oscillator frequency being utilized for the Terminal Receiver, according to the following table:

÷16	÷64	OSCILLATOR FREQUENCY AT THE EXTERNAL CLOCK INPUT
0	0	= Bit Rate
1	0	= 16 x Bit Rate
0	1	= 64 x Bit Rate
1	1	Master Reset

OUTPUTS

Data Output – This output transmits data in serial fashion with START and STOP bits (if applicable). The START bit is a SPACE (low level), the data is transmitted in positive logic, and the STOP bit or bits are MARK (high level).

Buffer Empty – A high level on the Buffer Empty output indicates that the data previously stored in the Buffer Storage latches has been transferred into the Shift Register and the latches are available for new data. The Load Strobe input automatically resets this output during the load cycle.

Figure E-38. P-Channel MOS Terminal Transmitter (7904275) (Cont)

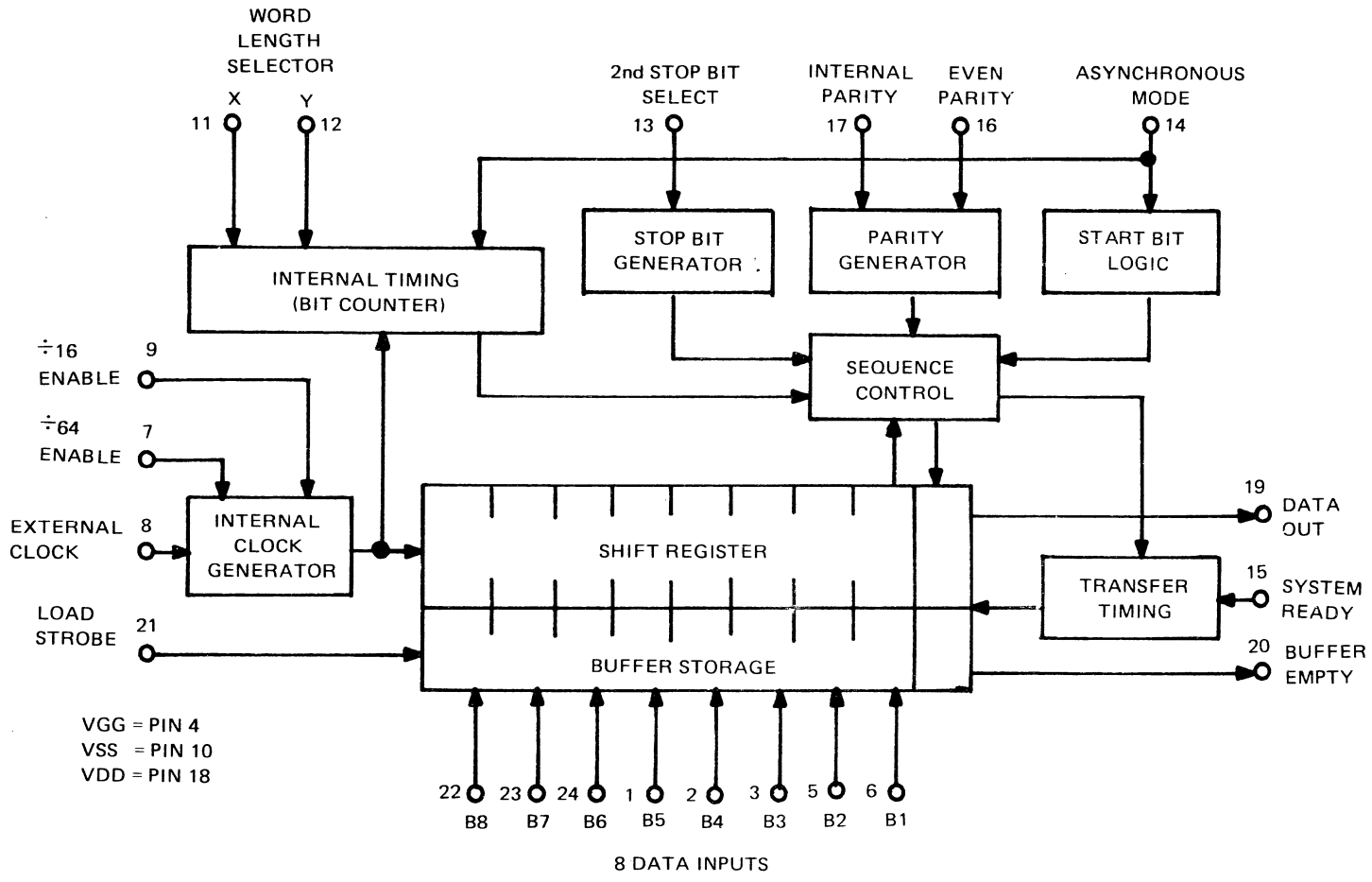
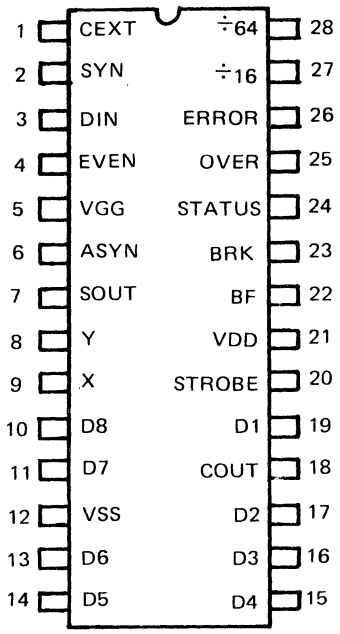


Figure E-38. P-Channel MOS Terminal Transmitter (7904275) (Cont)



DESCRIPTION

ASYNCHRONOUS OPERATION

The function of the terminal receiver is to respond to input data and synchronize with that data. The normal state of the data line during the time when no character is being transmitted is the Mark state. The initial change in state of this line occurs upon receipt of the Start bit. This "Mark-to-Space" transition (of the Start bit) causes the internal clock generator to be initialized for synchronization of the internal clock with the data. The data line is continuously monitored until the internal clock signal is generated at the midpoint of the Start bit period. This assures the presence of a valid Start bit. The synchronizing logic is then disabled until the complete character (following the Start bit) is received. If the data line returns to the Mark state (as in the case of noise) during the monitoring period, the bit is ignored and the terminal receiver resumes looking for a valid Start bit.

After the Start bit has been detected and the synchronization accomplished, data is shifted through the shift register and the Start bit appears in the Start bit flip-flop (the last stage of the shift register). The complete character is now stored in the shift register and the receiver automatically generates a transfer command to load the character in the buffer storage register. At the same time, the state of the Stop bit flip-flop is monitored to verify the presence of a Stop bit. Its absence results in an error output called Break being stored in the receiver status register.

As the character shifts through the shift register, parity for the character is accumulated. The resulting parity bit condition is compared with correct parity (odd or even) and, in the case of error, Parity Error is stored in receiver status register.

When the character is transferred to the buffer storage register, a Buffer Full signal is stored in the receiver status register. If the transfer occurs during a full buffer condition, the old character is lost and an error signal called Overrun is stored in the receiver status register. The receiver status information is retained throughout the character time until a new character is received and the new status is stored.

The access of data in the buffer storage register by means of the Data Strobe resets the buffer status output, indicating that the last character stored in the buffer storage register has been taken by the system.

The internal clock generator divides the bit time for each data bit into 16 or 24 segments, depending upon the externally selected ratio. A single cycle of the oscillator input signal is gated out of

Figure E-39. P-Channel MOS Terminal Receiver (7904276)

the clock generator at the center of a bit. This pulse is the internal clock signal which samples the data and provides the internal timing for the entire terminal receiver. The clock generator and synchronization circuitry can be bypassed by a low level on both the ÷16 Enable and the ÷64 Enable. In this case, the oscillator input signal becomes the internal clock.

A master reset is provided by means of these same two clock enable lines. When both the ÷16 Enable and the ÷64 Enable are at a high level, the chip is held in a master reset condition.

SYNCHRONOUS OPERATION

Synchronous data transmission has several characteristics which require special consideration in the synchronization of incoming data with the receiving system. Synchronous data appears as a continuous bit stream with no interval between characters and no control bits (Start and Stop bits). Therefore, synchronization must be accomplished by means of the regular characteristics of the data itself. Two degrees of synchronization are required in order to receive a valid message. These are bit synchronization (which synchronizes the internal clock of the receiving system to the data bits) and character synchronization (which establishes a character reference by means of sync codes and utilizes the fixed bit length of the characters to maintain character synchronization).

The technique of bit synchronization provided in the terminal receiver for the synchronous mode of operation utilizes each "Mark-to-Space" transition of the data. The data transition causes an incremental correction of the internal clock timing of 1/32 or 1/128 of the bit time (depending upon the counter ratio selected, ÷16 or ÷64). The process of incrementing the clock with respect to the data continues with each Mark-to-Space transition of the data until the clock signal occurs at the midpoint of the data bit. The synchronization logic continuously attempts to correct the phase error between the midpoint of the data bit and the internal clock. This results in the internal clock maintaining lock within 0.8% of the reference (÷64 clock model). The advantage of this technique is that the data transition (Mark-to-Space transition) times are averaged; therefore, signal noise pulses or other data aberrations do not cause the receiver to completely lose bit synchronization. This feature is particularly important in synchronous transmission because of the problem of maintaining character synchronization and the necessity of re-establishing character synchronization whenever bit synchronization is lost.

Character synchronization is performed external to the terminal receiver by means of a sequence of comparisons between the received data and a synchronization code (e.g., "Syn") or set of synchronization codes. The terminal receiver is designed to facilitate this external character synchronization in the following manner. When the "Syn" Detected input is low and the receiver is operating in the synchronous mode, the buffer storage register is "transparent" so that data can be monitored as it ripples through the shift register. After the first sync code has been detected, the "Syn" Detected signal is applied, which returns the buffer storage register to its normal mode of operation and initializes the character counter. The second character in the sync detection sequence is then transferred automatically to the buffer storage register when complete. This character is then accessed for verification as a sync code. The process is repeated until it has been determined that character synchronization has been achieved. (If the required sync code is not present in the buffer storage register during the synchronization comparison, the "Syn" Detected signal is removed and the process starts over.) Once the synchronization sequence is complete, the external sync comparison logic is disabled and the incoming data message is processed as data.

As the character shifts through the shift register (bypassing the Stop bit flip-flop), parity for the character is accumulated. The resulting parity bit condition is compared with correct parity (odd or even) and, in the case of error, Parity Error is stored in the receiver status register.

When the character is transferred to the buffer storage register, a Buffer Full signal is stored in the receiver status register. If the transfer occurs during a full buffer condition, the old character is lost and an error signal called Overrun is stored in the

Figure E-39. P-Channel MOS Terminal Receiver (7904276) (Cont)

receiver status register. The receiver status information is retained throughout the character time until a new character is received and a new status word is stored.

The access of data in the buffer storage register by means of the Data Strobe resets the buffer status output, indicating that the last character stored in the buffer storage register has been taken by the system.

The internal clock generator divides the bit time for each data bit into 16 or 64 segments depending upon the externally selected ratio. A single cycle of the oscillator input signal is gated out of the clock generator at the center of a bit. This pulse is the internal clock signal which samples the data and provides the internal timing for the entire terminal receiver. The clock generator and synchronization circuitry can be bypassed by a low level on both the ÷16 Enable and the ÷64 Enable. In this case, the oscillator input signal becomes the internal clock.

A master reset is provided by means of these same two clock enable lines. When both the ÷16 Enable and the ÷64 Enable are at a high level, the chip is held in a master reset condition.

INPUTS

All inputs are internally compensated (20 k Ω to V_{SS} for improved compatibility with TTL. The internal compensation biases unused inputs to V_{SS} (high state).

Data Input – The serial data from the modem or other sources is entered into the Terminal Receiver by means of this terminal. The data is not inverted within the receiver and appears at the output in the same sense as it enters.

Data Strobe – The Buffer Storage latches are sampled whenever a high level is applied to the Data Strobe input. The Data Strobe may be maintained in the high state.

Status Enable – The latches of the Receiver Status Register are sampled whenever a high level is applied to the Status Enable line. The Status Enable may be maintained in the high state.

Even/Odd Parity – A high level on the Even/Odd Parity input causes a check for an even number of high-level data bits, including the parity bit. A low level checks for odd parity in a similar manner. There is no provision to inhibit the Parity Check logic for "no parity" data transmission.

Word Length Selector – Two input lines (X, Y) are provided to define the character bit length. A character always appears at the output in a right justified bit position for the selected word lengths. The following table shows the character length for each input combination.

X	Y	WORD LENGTH (INCLUDING PARITY, IF APPLICABLE)
1	1	8 bits
0	1	7 bits
1	0	6 bits
0	0	5 bits

÷16 and ÷64 Counter Enables – These two inputs provide a means of producing the internal clock from an oscillator that is either 16 or 64 times the bit rate. Provision is also made to bring the already synchronized clock from a source such as a modem into the Terminal Receiver to act as the internal clock. Available options are shown in the following table.

÷16	÷64	OSCILLATOR FREQUENCY AT THE EXTERNAL CLOCK INPUT
0	0	= Bit Rate
1	0	= 16 x Bit Rate
0	1	= 64 x Bit Rate
1	1	Master Reset

External Clock Input – This is the oscillator input that controls the transmission rate of the Terminal Receiver.

Figure E-39. P-Channel MOS Terminal Receiver (7904276) (Cont)

Asynchronous/Synchronous Mode – A high level on the Asynchronous/Synchronous Mode input enables the device for operation in the asynchronous mode using control bits (START and STOP). The START bit is used to indicate the presence of a character and for synchronization of the internal clock with the character. The presence of a STOP bit verifies character synchronization.

A low level on this input enables the device for synchronous operation and disables all asynchronous logic. In the ÷16 or ÷64 modes, a transition monitor samples each "Mark-to-Space" transition of the data, compares the ÷16/÷64 clock counter state with the preferred coincidence state, and incrementally adjusts one-half clock step toward correct bit synchronization. In the ÷1 mode, bit synchronization must be accomplished externally. Character synchronization is handled externally by detecting a series of sync characters (e.g., "SYN").

"Syn" Detected (Synchronous Mode only) – A low level on this line holds the Buffer Storage Register latches open so that data ripples across the outputs to permit external detection of sync codes on the receiver outputs. The transition to a high level indicates to the receiver that external logic has determined character sync. A high level on this input enables the system to operate in the synchronous mode by cycling in synchronization with each character.

OUTPUTS

All used outputs require external pulldown resistors. For TTL interfacing with a fan-out of one (1), R_L = 6.8 kΩ ±5% (see Figure 1).

Data Outputs – Data is transferred to the eight parallel open-drain outputs from the Buffer Storage Register latches. The outputs are enabled by an input signal to the Data Strobe input and provide bussing capability. For character lengths of 5 to 8 bits, data appears in a right justified position.

Serial Output – The data being shifted into the shift register is simultaneously available at the Serial Output. This provides a means for externally accumulating longitudinal parity.

Receiver Status Outputs – Status information is provided by means of four open-drain outputs. These outputs are enabled by the Status Enable input for bussing capability. The functions of these Status outputs are:

1. Buffer Full – This output shows that a character is in the Buffer Storage latches and has not been sampled at the eight data outputs by using the Data Strobe input. The Data Strobe signal automatically resets the Buffer Full output. If the Data Strobe input is maintained in the high state, the Buffer Full output appears as a pulse.

2. Overrun – This output provides an indication that two or more characters have been transferred into the Buffer Storage Register latches in succession without an intervening sampling of the buffer contents by use of the Data Strobe. This means that at least one character has been lost. Use of the Data Strobe removes this indicator after the transfer of the next character into the Buffer Storage Register.

3. Parity Error – Incorrect parity for a particular character causes an error signal (high level) to be generated and made available at the Parity Error output for the period that the character is present in the Buffer Storage Register.

4. Break (Asynchronous Mode only) – The absence of a STOP bit following the character causes a Break signal to be stored in the Receiver Status Register for the character time.

Clock Output – The internal clock that has been synchronized with the data is available for external use by means of this output.

Figure E-39. P-Channel MOS Terminal Receiver (7904276) (Cont)

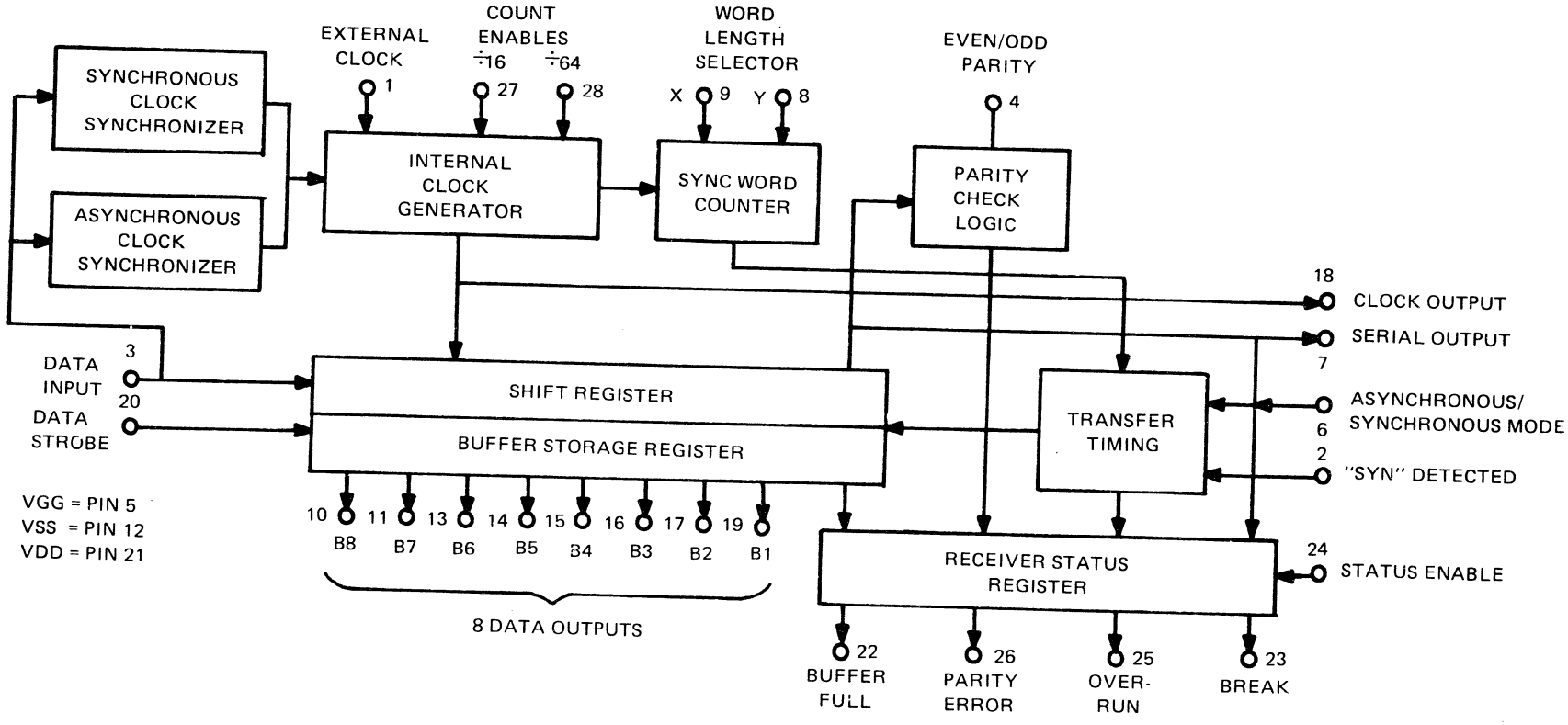
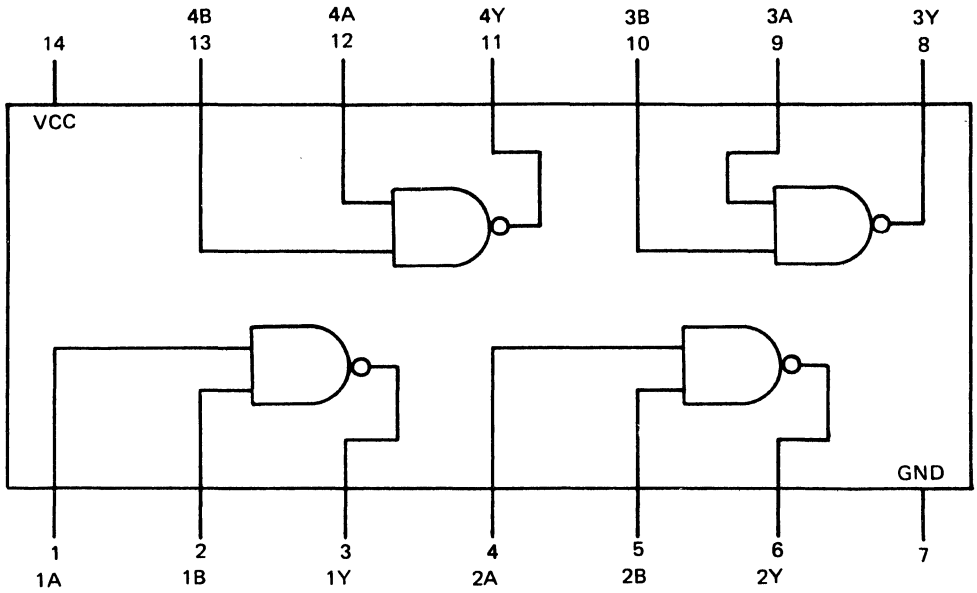
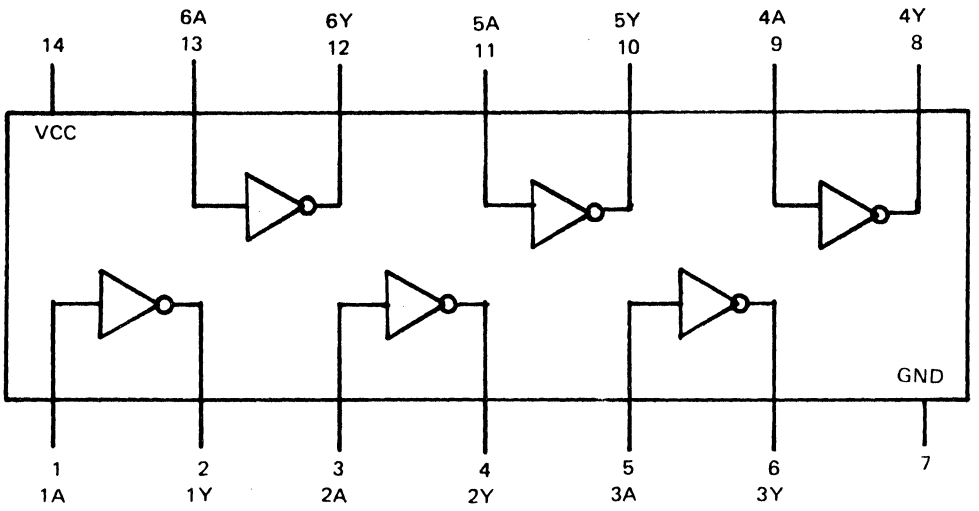


Figure E-39. P-Channel MOS Terminal Receiver (7904276) (Cont)



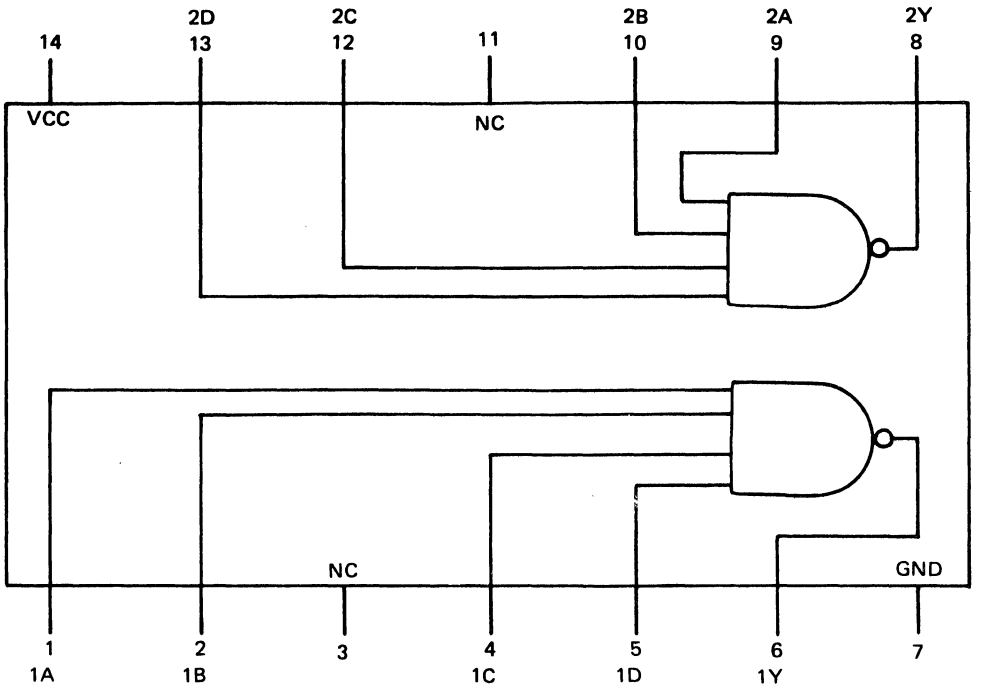
$\overline{Y}$ (LOW) = A · B

Figure E-40. Quadruple Two-Input NAND Gate (7904292)



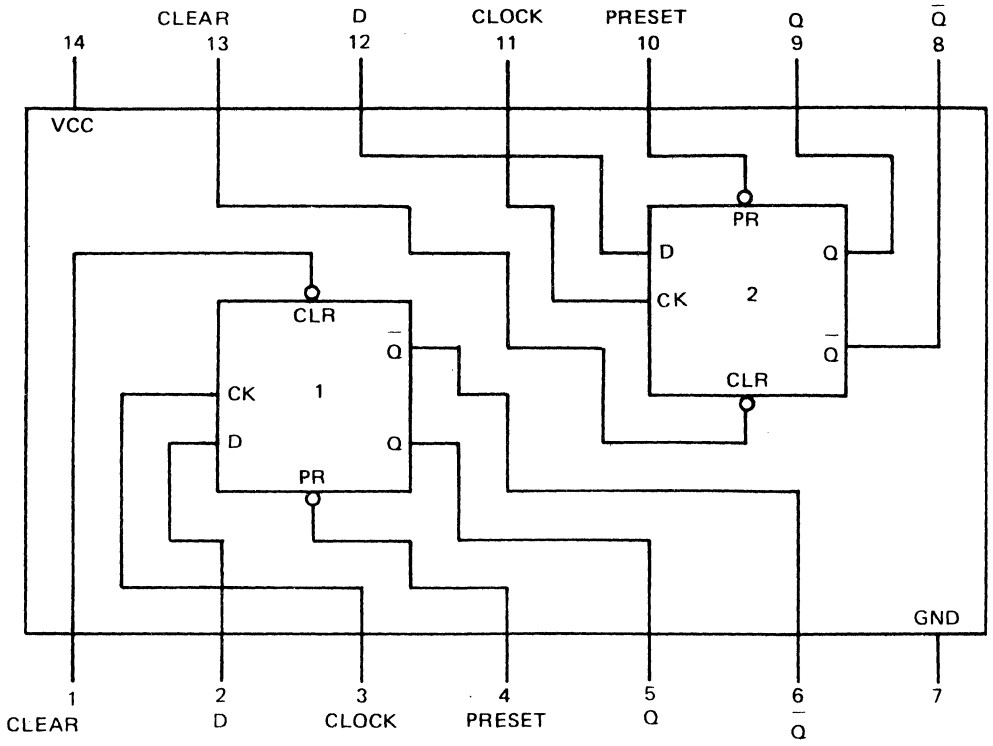
DESCRIPTION This integrated circuit contains six inverter circuits. A positive input (A) results in a negative output (Y). A negative input results in a positive output.

Figure E-41. Hex Inverter (7904293)



$\overline{Y}$ (LOW) = A · B · C · D

Figure E-42. Dual Four-Input NAND Gate (7904296)



DESCRIPTION

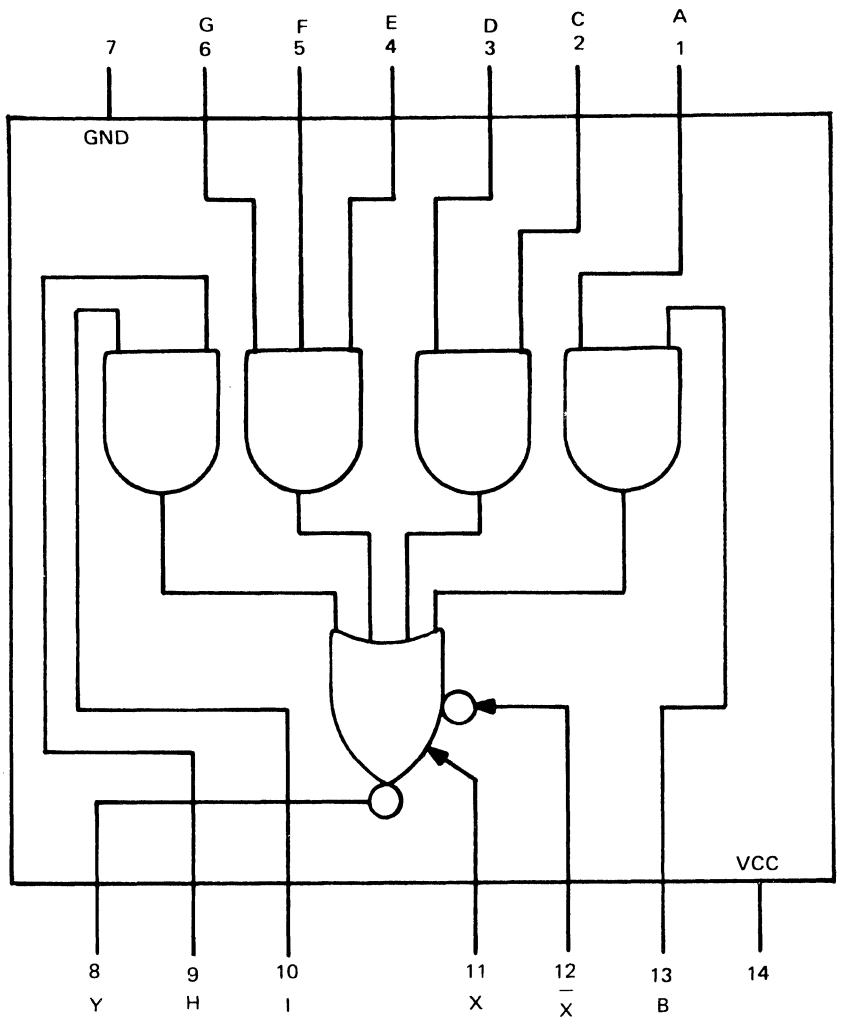
This integrated circuit contains two D type flip-flops with direct clear and preset inputs and both Q and $\overline{Q}$ outputs. Information at the D input is transferred to the outputs on the positive edge of the clock pulse. The function table shows the outputs for each input. The preset and clear inputs are independent of the clock. A low on the preset input sets Q to a high. A low on the clear input sets Q to a low. A low on both inputs sets Q and $\overline{Q}$ to a high. This is an unstable condition.

TRUTH TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Qo	$\overline{Qo}$

L = Low voltage level (steady state)
H = High voltage level (steady state)
X = Irrelevant
↑ = Transition from low to high level
Qo = The level of Q before the indicated input conditions were established
* = This configuration is not stable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure E-43. Flip-Flop, Dual D (7904298)

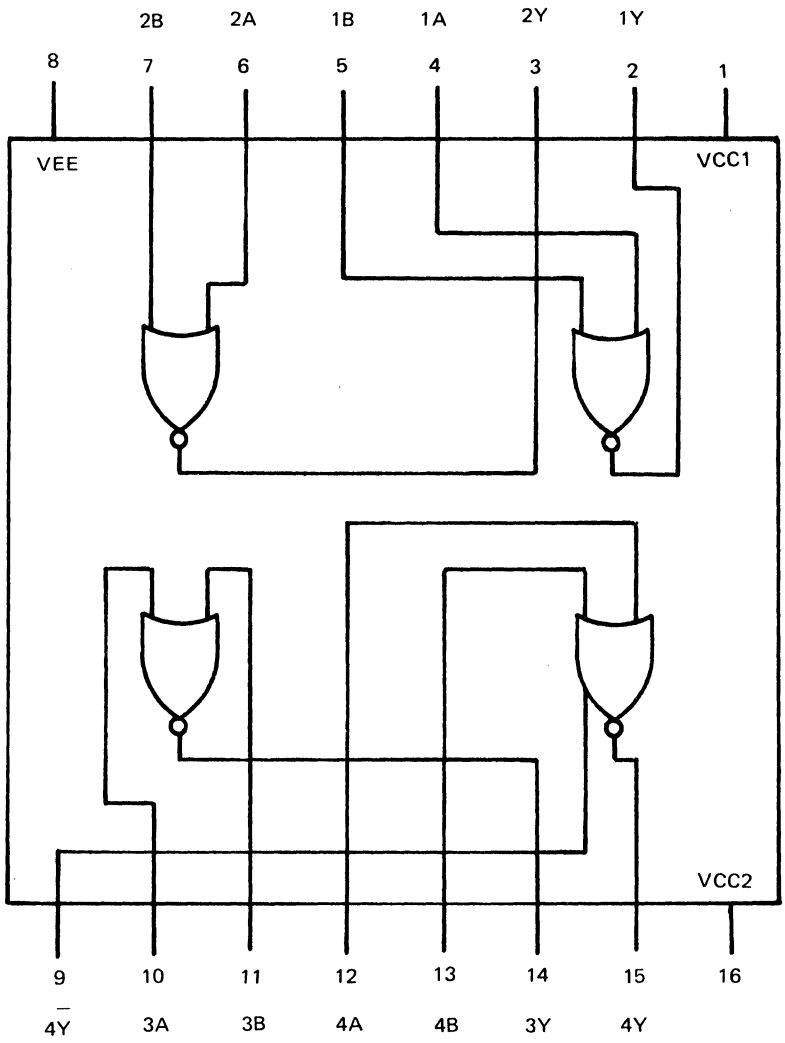


$\overline{Y}$ (LOW) = A · B + C · D + E · F · G + H · I + X + $\overline{X}$

DESCRIPTION

This integrated circuit contains an inverting OR gate which has three two-input AND gates and one three-input AND gate for inputs. The output (Y) of the OR gate is low when at least one of the AND gate outputs is high. The AND gate output will be high when all the inputs to the AND gate (A and B, or C and D, or E, F, and G, or H and I) are high. The output of the OR gate will also be low when the X input to the gate is high or the $\overline{X}$ input is low.

Figure E-44. Single 2-2-2-3 Input AND-OR Inverter (7904418)

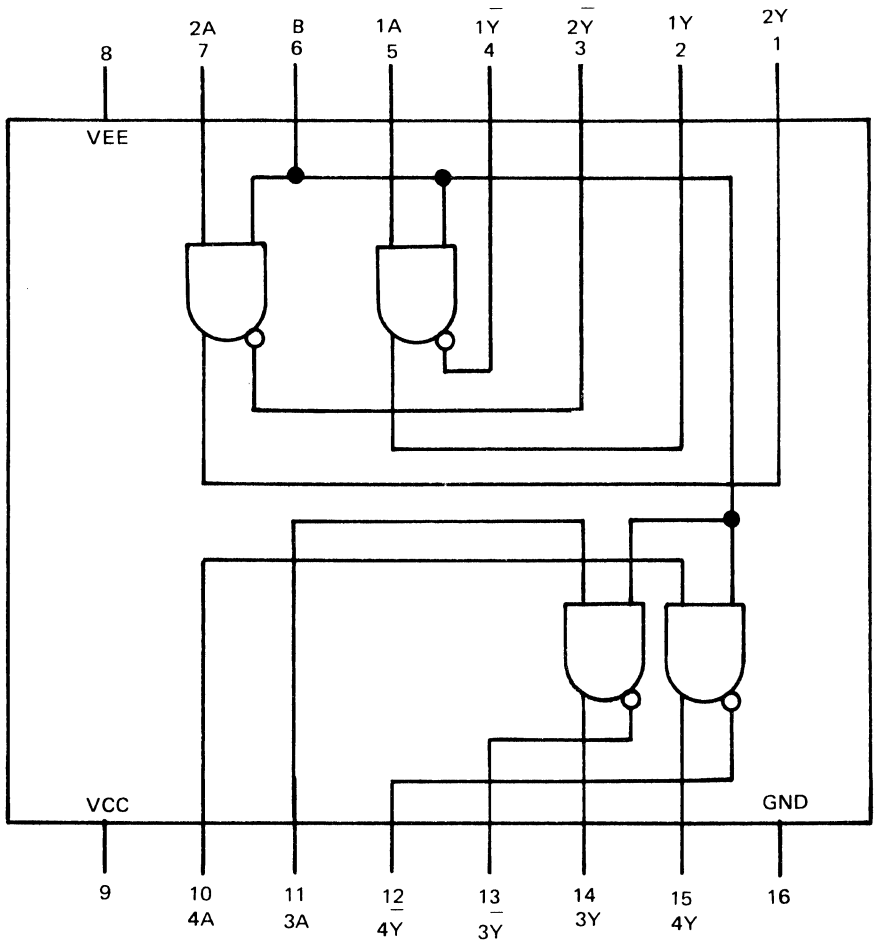


$\overline{Y}$ (LOW) = A + B

DESCRIPTION

This integrated circuit contains four two-input inverting OR gates. The output (Y) will be low when either or both inputs (A and B) are high. Pin 9 is an inverted signal of pin 15.

Figure E-45. Quadruple Two-Input NOR (7904474)



DESCRIPTION

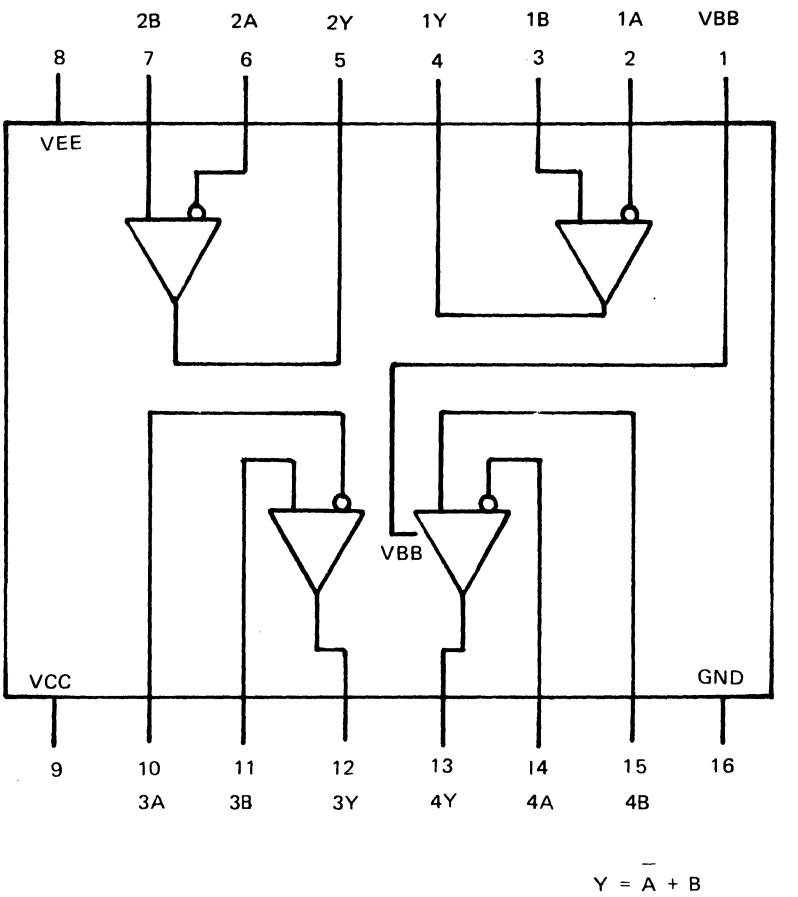
This integrated circuit contains four TTL TO ECL translators. The output (Y) will be high when both inputs (A and B) to the AND gate are high. At the same time the output ($\overline{Y}$) will be low.

TRUTH TABLE

INPUT		OUTPUT	
A	B	Y	$\overline{Y}$
L	L	L	H
L	H	L	H
H	L	L	H
H	H	H	L

L = Low voltage
H = High voltage

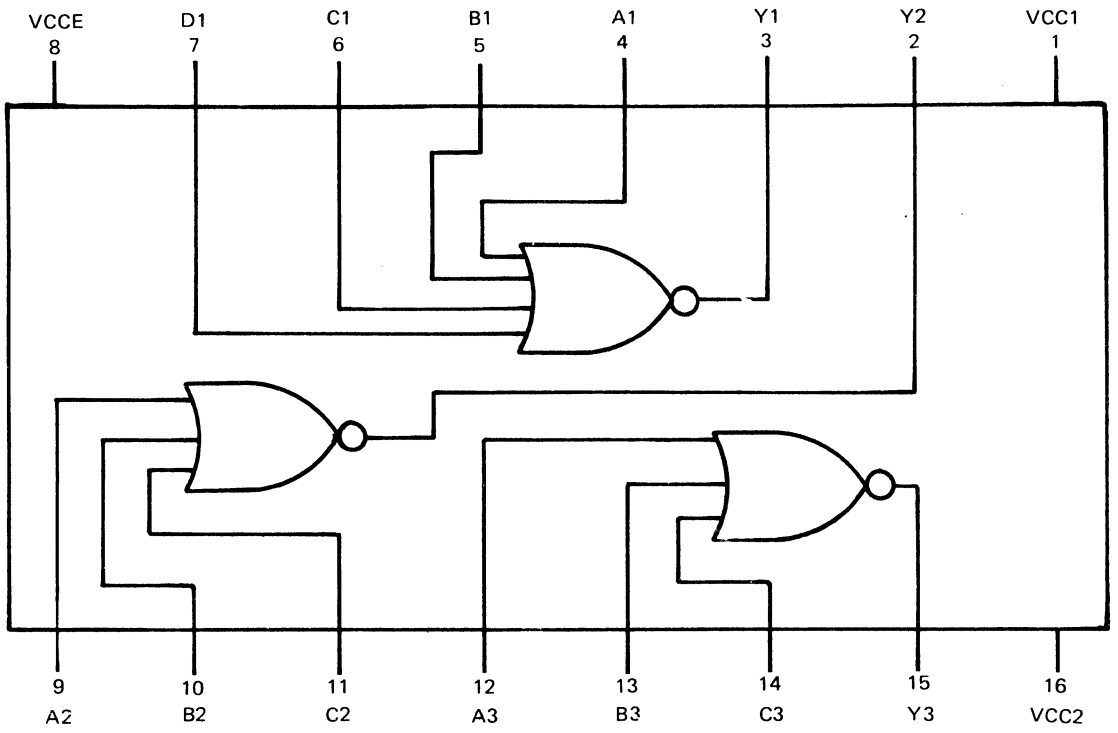
Figure E-46. Translator-Quad, TTL to ECL (7904477)



DESCRIPTION

This integrated circuit contains four ECL to TTL translators. Either input A or B will be connected to the translator. If A is connected, the output (Y) is high when the input (A) is low. If B is connected, the output (Y) is high when the input (B) is high. The VBB bins voltage input at pin 1 is intended for use of the circuit as a Schmitt trigger; it is not used in the DPS.

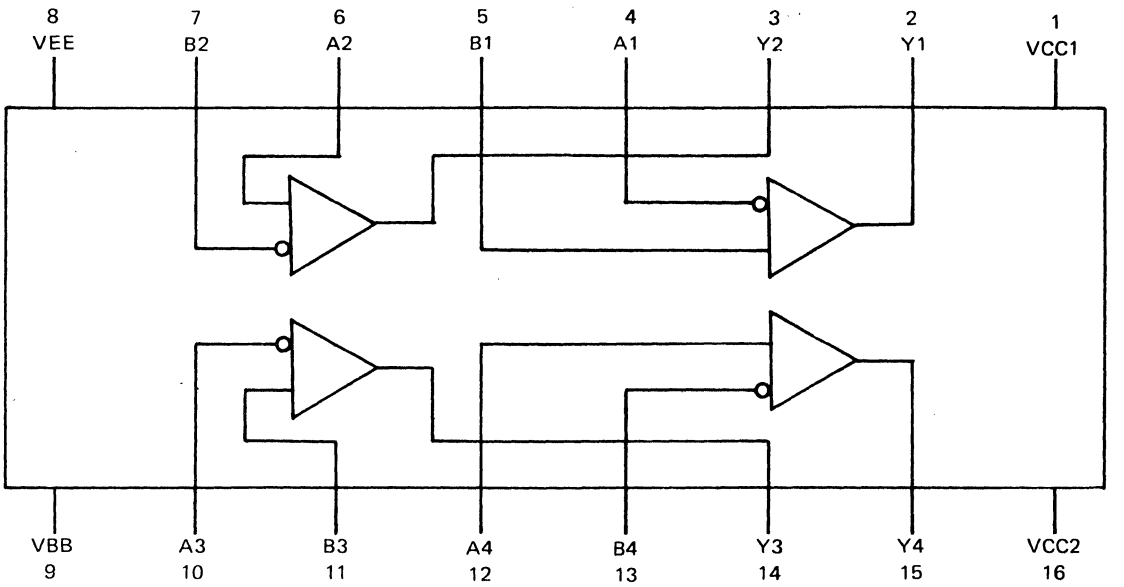
Figure E-47. Translator-Quad, ECL to TTL (7904478)



DESCRIPTION

This integrated circuit contains three inverting OR gates. Two of the OR gates have three inputs and the other one has four inputs. A high signal on any or all of the inputs (A, B, C, D) to a gate produces a low output (Y) from that gate.

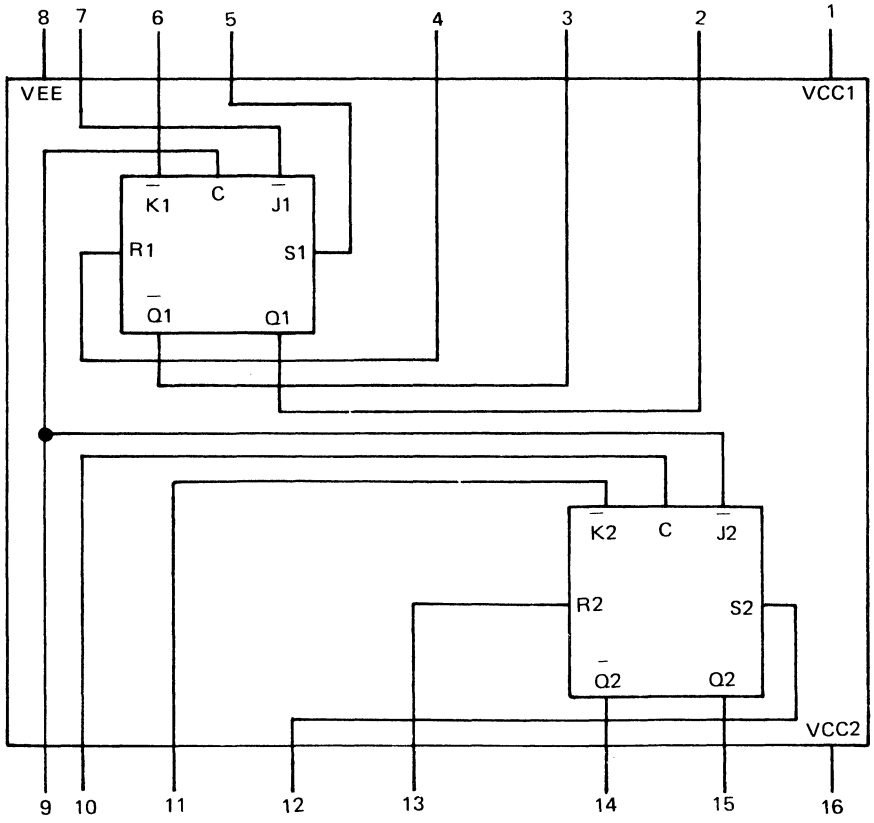
Figure E-48. Triple 4-3-3 Input NOR Gate (7904706)



DESCRIPTION

This integrated circuit contains four line receivers. The line receiver produces an output (Y) when it senses a differential voltage on the inputs (A and B). The VBB bias voltage input at pin 1 is intended for use of the circuit as a Schmitt trigger; it is not used in the DPS.

Figure E-49. Quadruple Line Receiver (7904707)



DESCRIPTION

This integrated circuit is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not affect the output.

The output states of the flip-flop change on the positive transition of the clock.

TRUTH TABLE (R-S)

R	S	QnH
L	L	Qn
L	H	H
H	L	L
H	H	N·D·

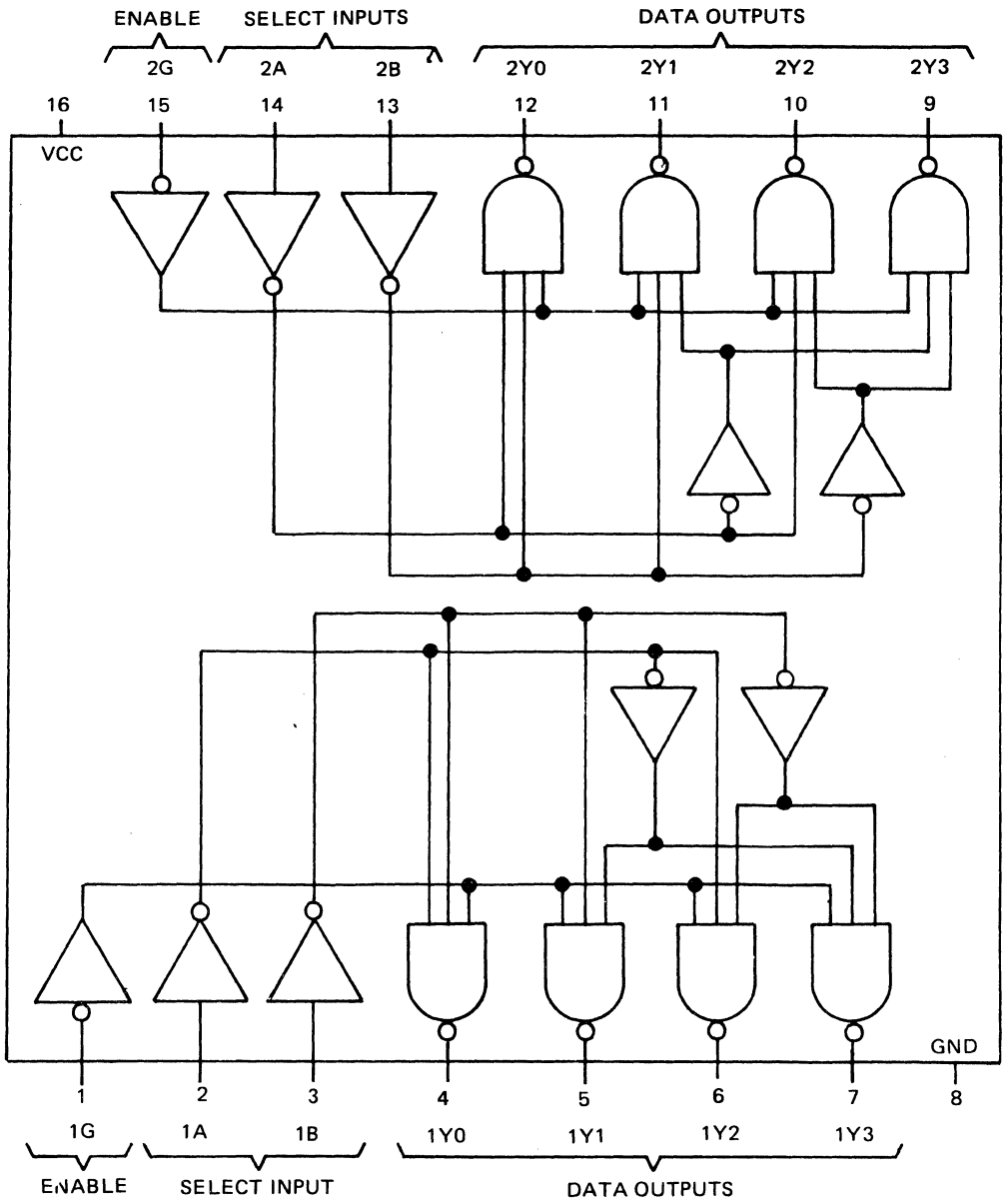
L = Low voltage
H = High voltage
N·D· = Not defined
Qn = Output
$\overline{Q}$n = Inverted output

TRUTH TABLE (J-K)

$\overline{J}$	$\overline{K}$	Qn+1
L	L	$\overline{Q}$n
L	H	L
H	L	H
H	H	Qn

Output states change on positive transition of clock for $\overline{J}$. $\overline{K}$ input condition present.

Figure E-50. Dual J-K Master Slave Flip-Flop (7904708)

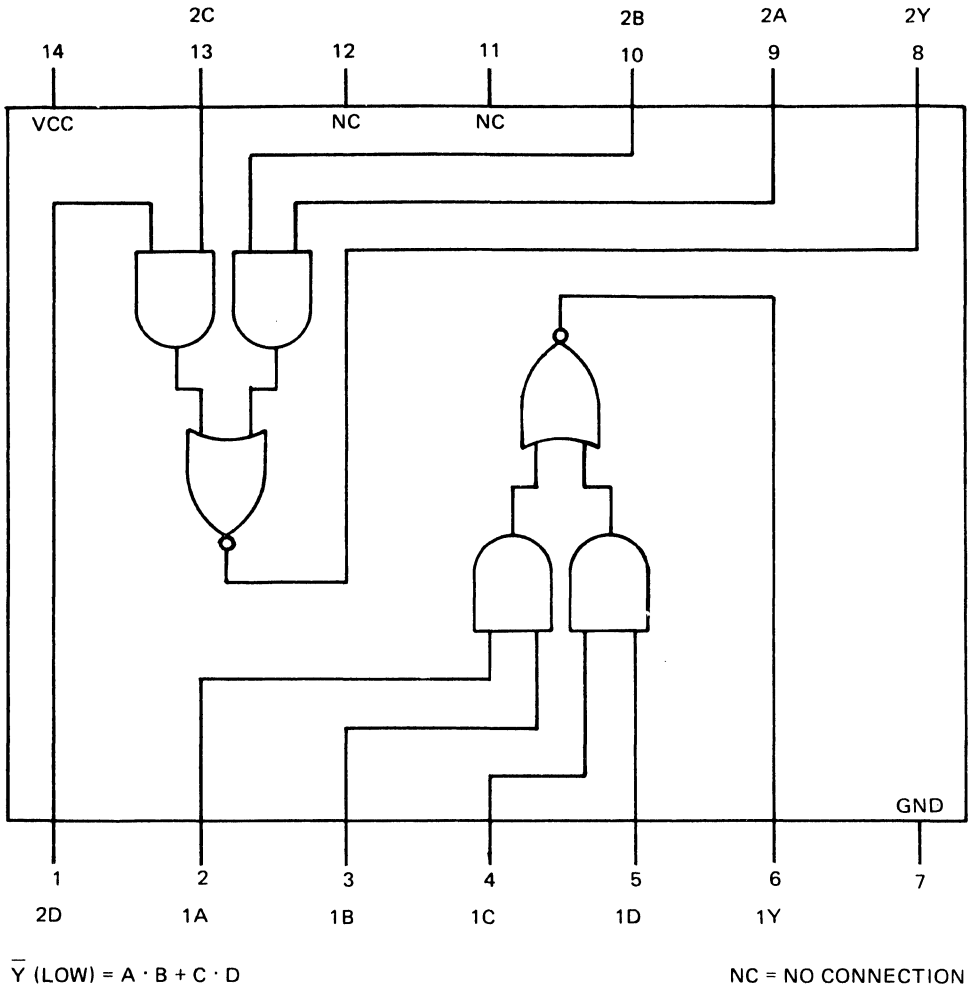


TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

Figure E-51. Dual 2 to 4 Line Decoder (7904773)



DESCRIPTION

This integrated circuit contains two two-input inverting OR gates. The input to the inverting OR gates are two two-input AND gates. The inverting OR gate output (Y) is low when both inputs (A and B, or C and D) to either AND gate are high.

Figure E-52. Dual AND-OR Inverter Gate (7904774)

GLOSSARY OF TERMS AND ABBREVIATIONS

TERM	DEFINITION
ADRS	Address
ADV	Advance
ALU	Arithmetic/Logic Unit: An adder that is also capable of performing logic functions.
Asynchronous	Not Synchronous
BAP	Buffer Address Pointer
Baud	The number of code elements per second.
BCW	Buffer Control Word
bps	Bits per second
Breakpoint	A point for breaking off program operation. The DPS stops upon reaching any address placed into the breakpoint register.
byte	A group of bits handled as a unit; DPS words may be handled as two 8-bit bytes.
C	Centigrade
CAP	Chain Address Pointer
Chip	An integrated circuit semiconductor device. Usually refers to the complete package, although theoretically referring to the semiconductor device within the package.
CLK	Clock
CLR	Clear
CM	Control Memory
CORDIC	Coordinate Rotation Digital Computer; a technique for handling trigonometric and hyperbolic computations.
CP/IO	Central Processor and Input-Output sections of the DPS.
DIP	Dual-in-line package; a rectangular semiconductor package with leads arranged in two parallel rows.
DMA	Direct Memory Access

TERM	DEFINITION
DPS	Data Processing Set
DSPL	Display
ECW	Emulator Control Word
EFA	External Function Acknowledge
EFR	External Function Request
EIA	Electronics Industries Association
EIE	External Interrupt Enable
EIR	External Interrupt Request
Emulator	The portion of a microprogram controlled processor that adapts it to perform specific functions.
EN	Enable
ESA	Externally Specified Address
ExOR	Exclusive OR
F	Fahrenheit
F-field	Format code field of macroinstruction word or function code field of microinstruction word.
Firmware	Unchangeable internal program; distinguished from hardware or changeable software.
Full Duplex	Data transmission in both directions simultaneously.
GENL	General
Half Duplex	Data transmission in only one direction at a time; also called simplex.
Hz	Hertz: cycles per second
IAW	Indirect Address Word
IC	Integrated Circuit

TERM	DEFINITION
IC Channel	Intercomputer Channel
IDA	Input Data Acknowledge
IDR	Input Data Request
IECF	Input Enable Control Frame
Indirect Addressing	A scheme in which a referenced address contains a coded word causing the referencing of another address.
INST or INSTR	Instruction
I/O	Input/Output
IOC	Input/Output Controller
IRCF	Input Request Control Frame
LED	Light Emitting Diode
LRI	Lowest Replaceable Item
LSB	Least Significant Bit
MA CLR	Master Clear
Macro Instruction	Instruction used by processor/emulator.
Macroprogram	Program of macro instructions stored in main memory.
Micro Instruction	Instruction used by MPC.
Microprogram	Program of micro instructions stored in micro memory.
MPC	Microprogrammed Controller
ms	Millisecond: $\frac{1}{1000}$ second
MSB	Most Significant Bit
NDRO	Nondestructive Readout Memory
NOP	No Operation
Normalize	To scale the mantissa of a floating point quantity so the first significant bit adjoins the sign bit and adjust the exponent accordingly.

TERM	DEFINITION
ns	Nanosecond: $\frac{1}{1,000,000,000}$ second
NTDS	Naval Tactical Data System
ODA	Output Data Acknowledge
ODR	Output Data Request
OECF	Output Enable Control Frame
ORCF	Output Request Control Frame
Paging	A system of virtual memory or relative memory addressing in which the memory is divided into groups of addresses called pages which may be interchanged under program control.
P Register	Program Address Register
PROM	Programmable Read Only Memory
PT	Point
Real Time	A term applied to processing operations that can be interrupted or controlled by events outside the system, and that can react with sufficient speed to analyze or control the external events.
Reg	Register
ROM	Read Only Memory
RTC	Real Time Clock
Scale	See Normalize
Simplex	Transmission in one direction only; also called half duplex.
Software	Data Processing Programs
Sync	See Synchronous
Synchronous	Operating at a clocked rate.

TERM	DEFINITION
TM	Transfer Mode
TP	Test Point
μI	Micro Instruction
μMem	Micro Memory
μP	Micro Program
μs	Microsecond: $\frac{1}{1,000,000}$ second
Virtual Memory (also called relative addressing)	A memory addressing system in which programs or data may be placed in different addresses, but appear to the program as though they were located in the true (virtual) addresses. Usually accomplished by modifying the address with a changeable base address. See paging.