CHAPTER 3

FUNCTIONAL DESCRIPTION

3-1. OVERALL FUNCTIONAL DESCRIPTION.

3-2. INTRODUCTION. This chapter includes a detailed analysis of the operational principles of the Input/Output Console OA-7984(V)/UYK (I/O Console) and its functions. The development of equipment inputs and outputs in each mode of operation are described. An overall description of the logic sections, units, and assemblies comprising the I/O Console are provided as follows:

a. An introduction to and description of the external and internal logic signal characteristics:

1. Signal levels used and their relative voltage levels

2. Interpretation of the word format's bit structure

b. Signals identified by their functional name (operational accomplishment)

c. Overall and functional block diagrams and descriptions

d. Logic principles described begin with an introduction to the basic logic symbology used in this manual. Each logic function described is supported by Boolean equations, truth tables, and simplified logic diagrams.

3-3. This chapter refers to and supports chapter 5 equipment diagrams and schematics. References to chapter 5 include either the functional circuit name and diagram sheet [e.g., Mode Selection I (5-5)] or the term, diagram number, and approximate zone where the circuit/term is shown [e.g., OXDO3 (5-5, 6C)]. Where terms have been assigned a common functional name, the functional name will be used in the place of the term [e.g., OFF-LINE F/F OXDO3 (5-5, 6C)].

3-4. MODES OF OPERATION.

3-5. The I/O Console normally operates in the on-line mode as an input/output device of the computer. In this operational mode, the I/O Console is controlled by the computer. The I/O Console may also be operated in the off-line mode (controlled at the I/O Console panel) for maintenance and tape preparation. A functional block diagram of the I/O Console is illustrated in figure 3-1. The main function of the I/O Console is data transfer processing. To perform this function, the I/O Console is used for both on-line and off-line operations.

3-6. ON-LINE MODE. The I/O Console control logic assembly controls the transfer of all data words and control words exchanged between the computer and the input/output devices contained in the I/O Console. When in the on-line mode of operation, the I/O Console is capable of performing any one input function specified in table 3-1 and any one output function specified in table 3-1 with one addition: The printer and paper tape punch can operate concurrently.

3-7. The I/O Console can perform on-line operations with the teletypewriter interface when the printer, keyboard, paper tape punch, and paper tape reader are in the off-line mode. The following major functional areas are used in on-line operations:

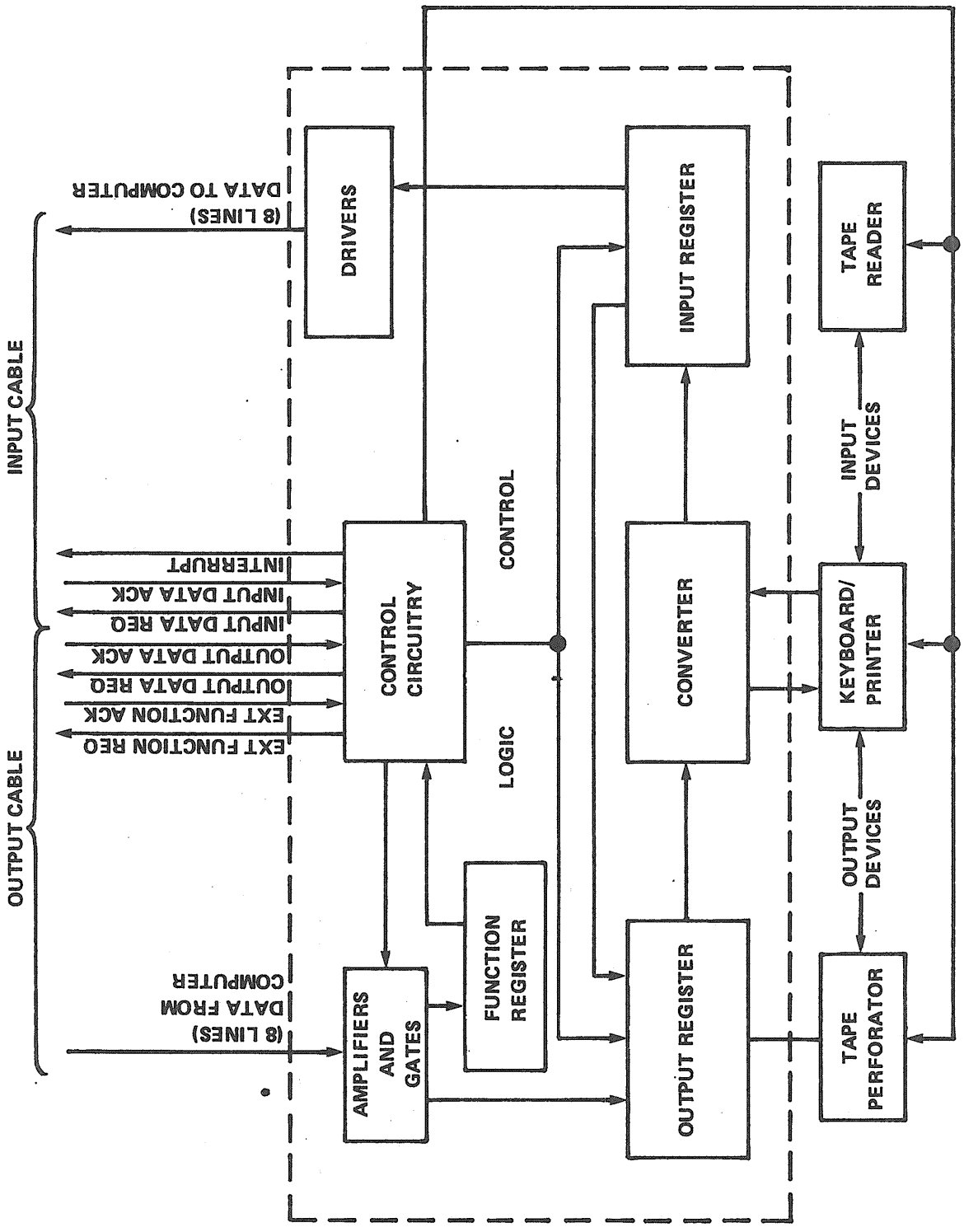


Figure 3-1. I/O Console Functional Block Diagram.

Table 3-1. I/O Console Input/Output Functions

Input Functions	Output Functions
Keyboard	Printer
Paper Tape Reader	Paper Tape Punch
	TTY Output

a. Timing circuits to generate the basic and phase timing pulses that are used to synchronize internal sequencing and generate internal subcommands.

b. Function translators to generate the necessary internal subcommands in order to process the external function words received from the computer.

c. Input/output control circuits to generate subcommands to control the operation of the input/output device currently in operation.

d. Interface circuits to receive and temporarily store data words or control signals until they are sent to their specified destination; i.e., paper tape punch, computer or other input/output device.

e. Interrupt circuits to receive, process, and transfer interrupt control signals between the I/O Console and the computer.

3-8. Keyboard/Printer. The keyboard transfers data from the keyboard to the control logic interface circuits for transfer to the computer and printer for on-line operations, or from the keyboard via the control logic interface circuits to the printer and paper tape punch during the off-line mode of operation (figure 3-2).

a. The printer receives data via the control logic interface circuits from the computer and keyboard during the on-line operations or via the control logic interface circuits from the keyboard or the paper tape reader during the off-line mode of operation (figure 3-3).

3-9. Paper Tape Reader. The paper tape reader is designed to read data from a perforated paper tape and transfer the data to the computer via the control logic for on-line operations. The paper tape reader can also transfer data to the paper tape punch and/or printer via the control logic during the off-line mode of operation (figure 3-4).

3-10. Paper Tape Punch. The paper tape punch is designed to receive data from the computer via the control logic interface circuits, and to transfer the data on to perforated paper tape. In the off-line mode, the paper tape punch will punch data received via the control logic from either the paper tape reader or the keyboard (figure 3-5).

3-11. OFF-LINE MODE. When in the off-line mode of operation, the I/O Console performs general maintenance operations of the input/output units and the following data processing operations:

a. Keyboard-to-printer

b. Keyboard-to-printer and paper tape punch

c. Paper tape reader-to-paper tape punch

d. Paper tape reader-to-printer

e. Paper tape reader-to-printer and paper tape punch.

3-12. Keyboard-to-Printer. The off-line keyboard-to-printer operation transfers data from the keyboard to the printer. The operation is initiated by pressing a keyboard key. As each key is

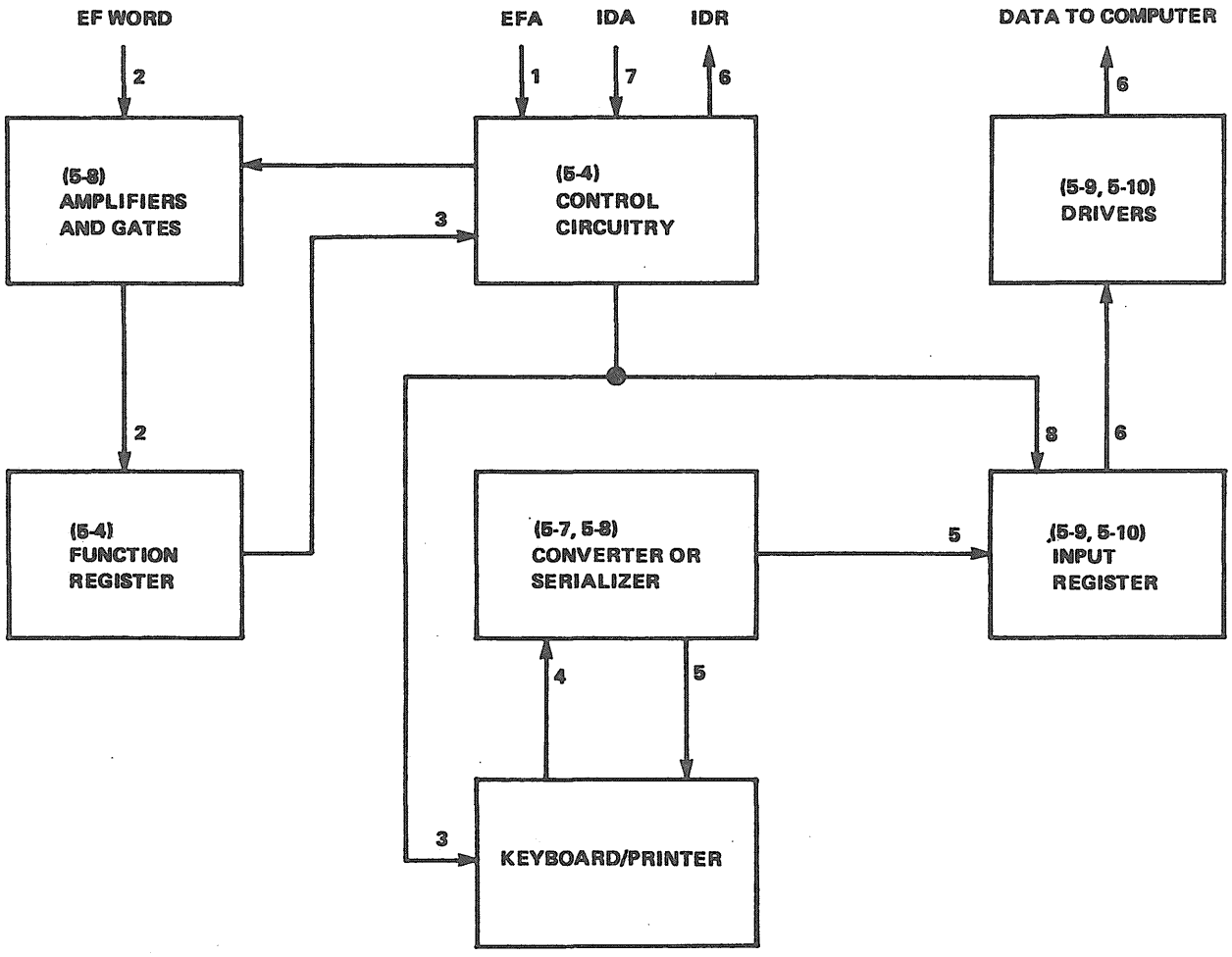


Figure 3-2. Keyboard Operation.

pressed, the corresponding seven-bit ASCII character code is transferred from the keyboard to the printer via the I/O Console control logic, and the printer prints the corresponding character as it receives each code.

3-13. Keyboard-to-Printer and Paper Tape Punch. The off-line keyboard-to-printer and paper tape punch operation transfers data from the keyboard to the printer and the paper tape punch. The operation is initiated by pressing a keyboard key. As each key is pressed, the corresponding seven-bit ASCII code is transferred to the I/O Console control logic. The I/O Console control logic then transfers the code to the printer and the paper tape punch. The printer prints the corresponding character and the paper tape punch punches each code on paper tape as it is received.

3-14. Paper Tape Reader-to-Paper Tape Punch. The off-line paper tape reader-to-paper tape punch operation transfers data from the paper tape reader to the paper tape punch for duplicating paper tape with a 5-, 6-, 7-, or 8-level format. The operation is initiated when the reader is enabled and proceeds in accordance with the following sequence:

a. The paper tape reader reads one frame of data from the paper tape.

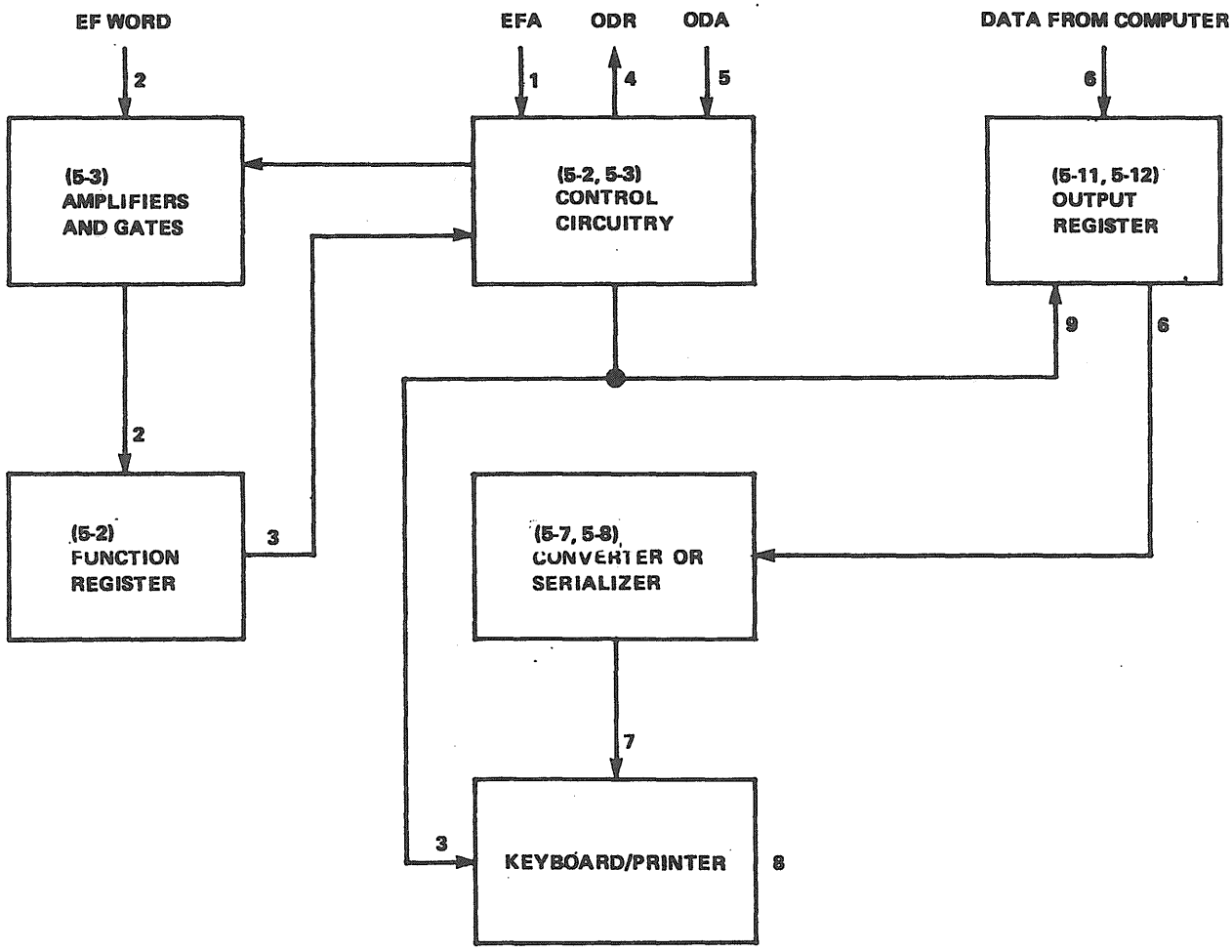


Figure 3-3. Printer Operation.

b. The I/O Console control logic transfers the data to the paper tape punch.

c. The paper tape punch punches one frame of data on paper tape.

d. The paper tape reader advances the paper tape to the next frame of data.

e. The sequence repeats.

f. The operation automatically terminates when the data from the last frame on the tape in the reader is punched on the tape in the punch, and no more feed holes are detected by the reader.

3-15. Paper Tape Reader-to-Printer. The off-line paper tape reader-to-printer operation transfers data from the paper tape reader to the printer. The operation is used to make printouts of ASCII-coded paper tape. The operation is initiated when the paper tape reader is enabled and proceeds in accordance with the following sequence:

a. The paper tape reader reads one frame of data from the paper tape.

b. The I/O Console control logic transfers the data to the printer.

c. The printer prints the corresponding character.

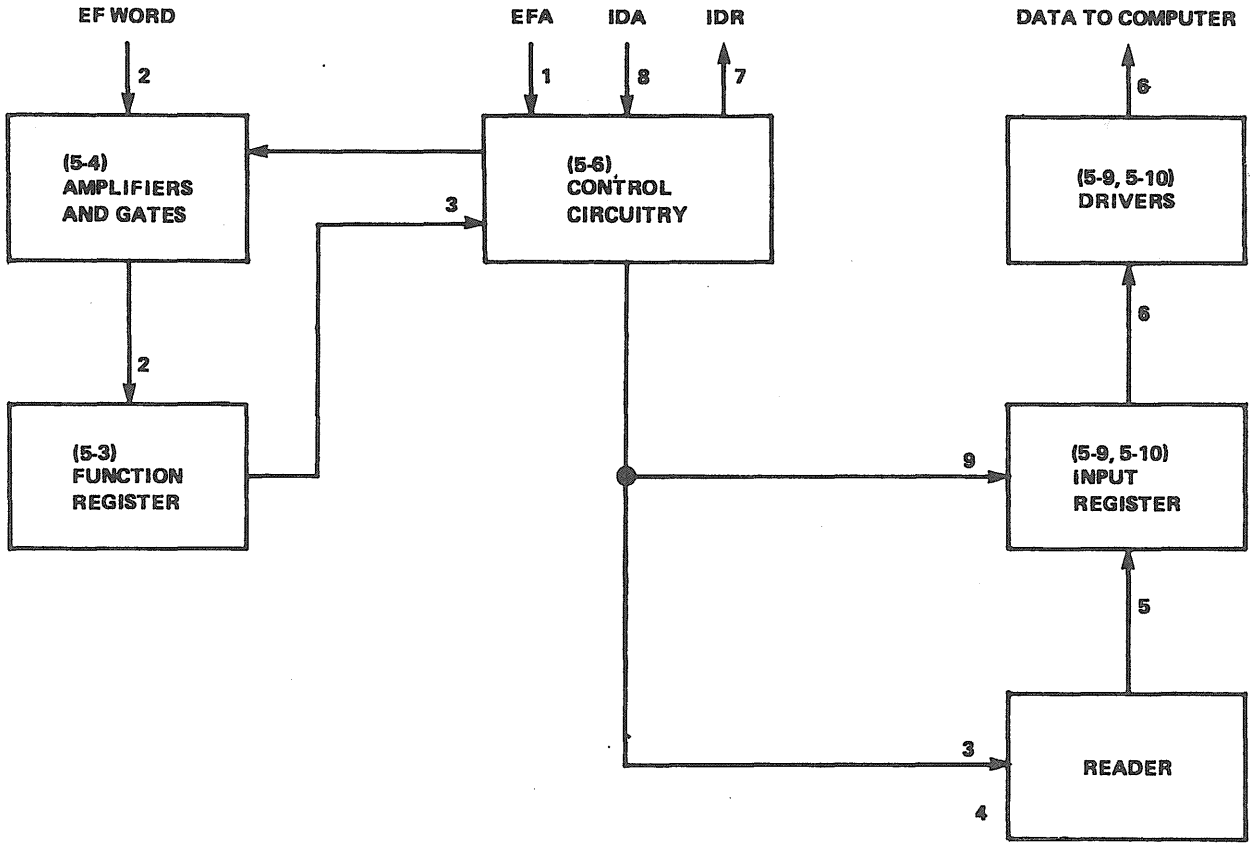


Figure 3-4. Paper Tape Reader Operation.

d. The paper tape reader advances the paper tape to the next frame.

e. The sequence repeats.

f. The operation automatically terminates when the character corresponding to the last frame of data on the paper tape has been printed, and no more feed holes are detected by the paper tape reader.

3-16. Paper Tape Reader-to-Paper Tape Punch and Printer. The off-line paper tape reader-to-paper tape punch and printer operation transfers data from the paper tape reader to the paper tape punch and printer. This operation is used to duplicate and print ASCII-coded paper tape. The operation is initiated when the reader is enabled and proceeds in accordance with the following sequence:

a. The paper tape reader reads one frame of data from the paper tape.

b. The I/O Console control logic transfers the data to the paper tape punch.

c. The paper tape punch punches one frame of data on the paper tape.

d. The I/O Console control logic transfers the data to the printer.

e. The printer prints the corresponding character.

f. The paper tape reader advances the paper tape to the next frame of data.

g. The sequence repeats.

h. The operation automatically terminates when the character corresponding to the last frame of data on the paper

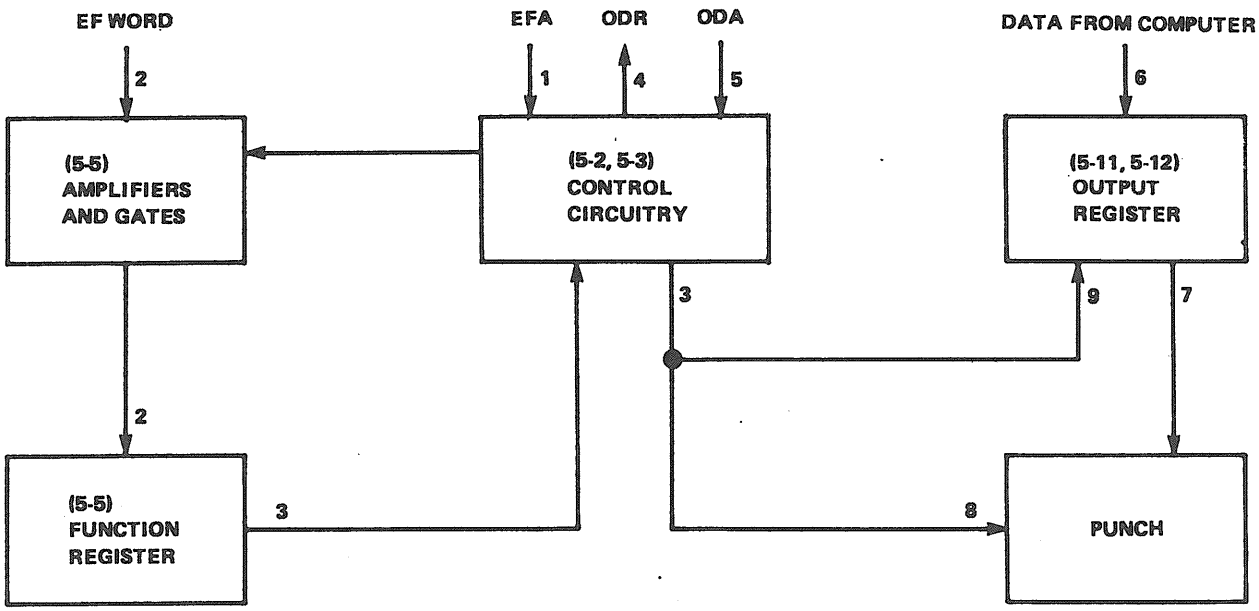


Figure 3-5. Paper Tape Punch Operation.

tape in the paper tape reader has been printed, and no more feed holes are detected by the paper tape reader.

3-17. **KEYBOARD/PRINTER OPERATION.**

3-18. MODEL 35 KEYBOARD/PRINTER. The Model 35 Keyboard Printer (keyboard/printer) is an electromechanical device that provides a convenient means for transmitting information to, and receiving responses from, the computer. Basically the keyboard/printer consists of a keyboard base, printing unit, motor unit, electrical service unit, and enclosure.

3-19. Keyboard/printer operation can be initiated either manually (via keyboard entry) or electrically (via an external source). As indicated in figure 3-6, the keyboard base converts mechanical actions into electrical signals; the converse is true for the printing unit. Each keyboard entry begins a chain reaction of mechanical movements that position code bars and transfer levers preparatory to a motor-driven cam operating a set of electrical contacts within the contact box. These make/break actions of the contacts produce a unique string of electrical pulses for each graphic or function selected. This string of electrical pulses is transmitted to the printing unit, where the selection mechanism converts the pulses into mechanical actions to position a complement of code bars. The resulting mechanical actions either cause a character to be printed, or operate a function bar in the stunt box to generate the desired function, such as line feed or carriage return. Critical timing of the mechanical actions is controlled by various levers and bails that engage and disengage several clutches at appropriate times.

3-20. Keyboard. The keyboard mounts on the cradle assembly of the cabinet pan and provides support for the motor unit, printing unit, and intermediate gear assembly. The keys are positioned in a four-row arrangement, with most punctuation marks and control symbols indicated as upper keytop characters.

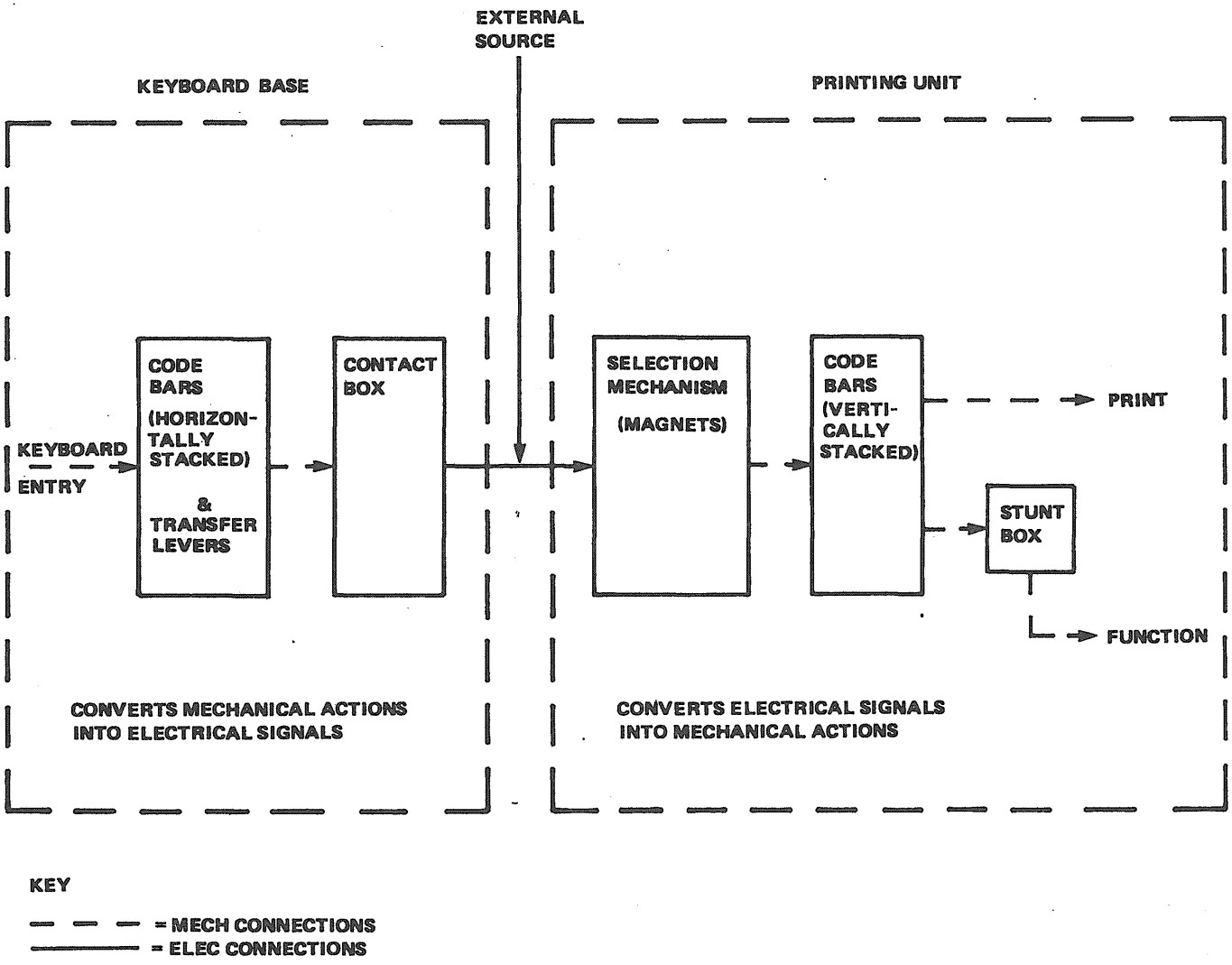


Figure 3-6. Block Diagram of Keyboard/Printer Operation.

3-21. The keyboard incorporates code-selecting and signal-generating mechanisms, and signal line and power line circuits. Motive power for activating the keyboard is derived from the motor unit and intermediate gear assembly through a gear arrangement to the printing unit main shaft.

3-22. Printing Unit. The printing unit incorporates the necessary electrical and mechanical elements to translate the signal code combinations into mechanical actions which print the messages and perform incidental functions. The printing unit is mounted centrally on the keyboard in front of the motor unit and intermediate gear assembly.

3-23. Code signals are applied to a two-coil magnet associated with a selecting mechanism which interprets the signals and controls the mechanical action involved in printing a character or performing a required function. Means are provided for orienting the selector to the received signal. The AC motor is geared to the main shaft of the printing unit by way of the intermediate gear assembly. Printing and various functional sections of the printing units are activated by individual clutches. Printing is produced by print pallets which are arranged in a small print box. In operation, the print box moves up, down, and across the paper and presents the proper print pallets to the printing hammer while the platen remains stationary. The pallets are driven forward against the inked ribbon and paper to print characters.

3-24. Paper is provided from a 5-inch diameter roll mounted between the side frames of the printing unit. The paper is friction-fed around the platen which is a cylinder free to rotate on its axis.

3-25. Motor Unit (LMU-3). The Motor Unit (LMU-3) is a complete assembly consisting of a 1/20 horsepower synchronous motor and a suitable mounting arrangement. It provides motive power for the keyboard/printer.

3-26. Electrical Service Unit. The electrical service unit is mounted on the cabinet pan directly behind the printing unit. The electrical service unit serves as the area of concentration for the wiring within the keyboard/printer, and provides mounting facilities for various electrical assemblies and components.

3-27. Enclosure. The protective enclosure surrounding the keyboard/printer consists of a base pan assembly, upper and lower covers, and shock mounts. Both covers are hinged to provide ready access for maintenance and repair. The enclosure is also equipped with a copyholder, line guide, and illuminating lamps.

3-28. TAPE READER OPERATION. The tape reader is a solid state, photoelectric, punched-tape reader that converts information on 5-, 6-, 7-, or 8-level tape into DC signal levels. The tape reader is unidirectional and reads 5- to 8-level tapes interchangeably at a slew speed of 400 characters per second. The tape reader is divided functionally into a tape read system, tape drive system, and power supply. A block diagram of the tape reader is shown in figure 3-7.

3-29. Tape Read System. A hole condition in a given channel of tape permits the passage of light from the exciter lamp to the photodiode head. The photodiodes are biased so that during a no-hole condition the data photodiode outputs will be at a positive level and the sprocket photodiode output will be at a negative level. During a hole condition, the data photodiode outputs will be at a negative level and the sprocket photodiode output at a positive level. These outputs are applied to the data and sprocket channel circuits.

3-30. There are eight identical data channel circuits each consisting of an emitter follower and a two-stage amplifier. The data channel circuits provide outputs of +5 VDC at 5mA with an 10kΩ external load for a hole condition, and 0.0±0.5 VDC for a no-hole condition (figure 3-8).

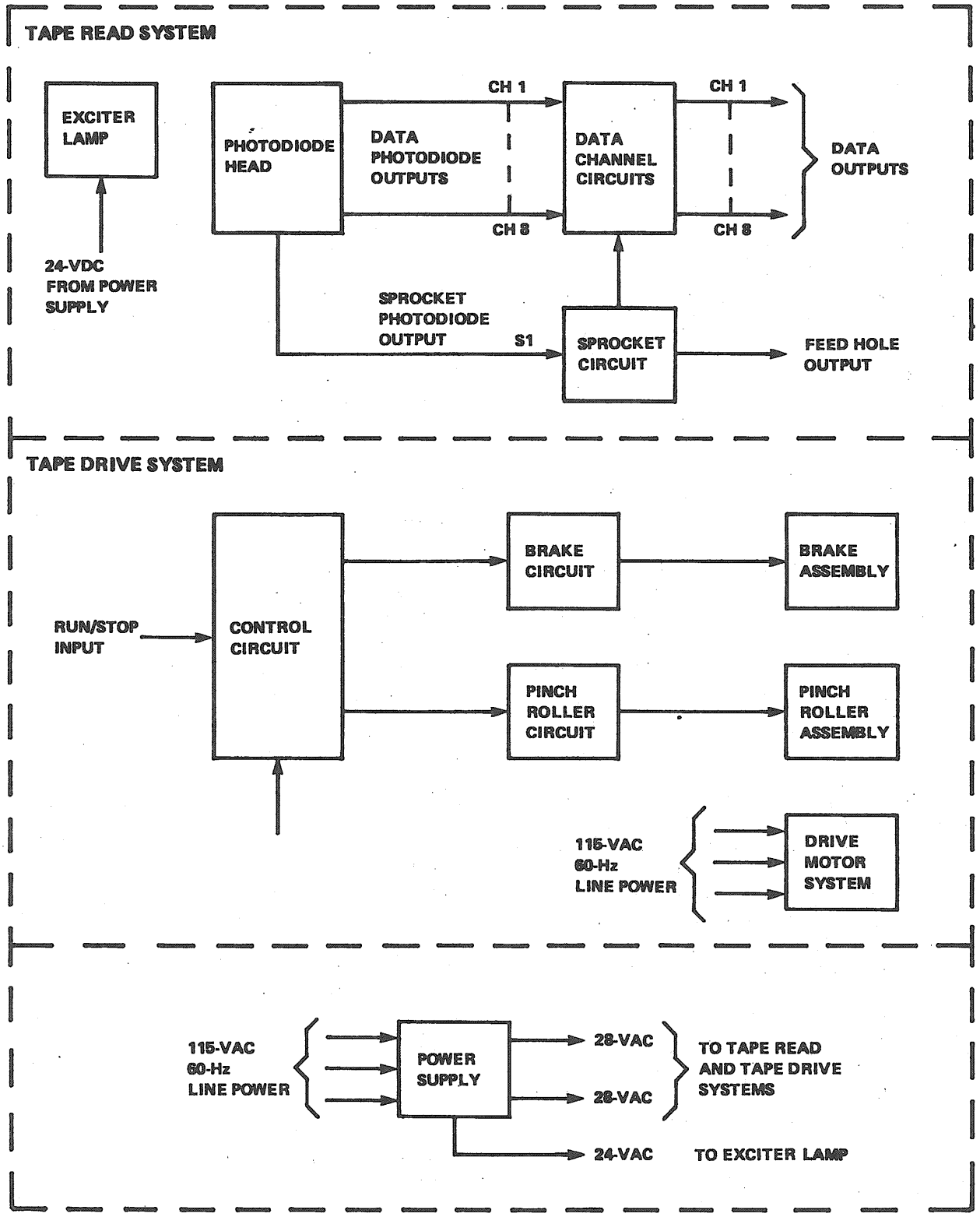


Figure 3-7. Paper Tape Reader Block Diagram.

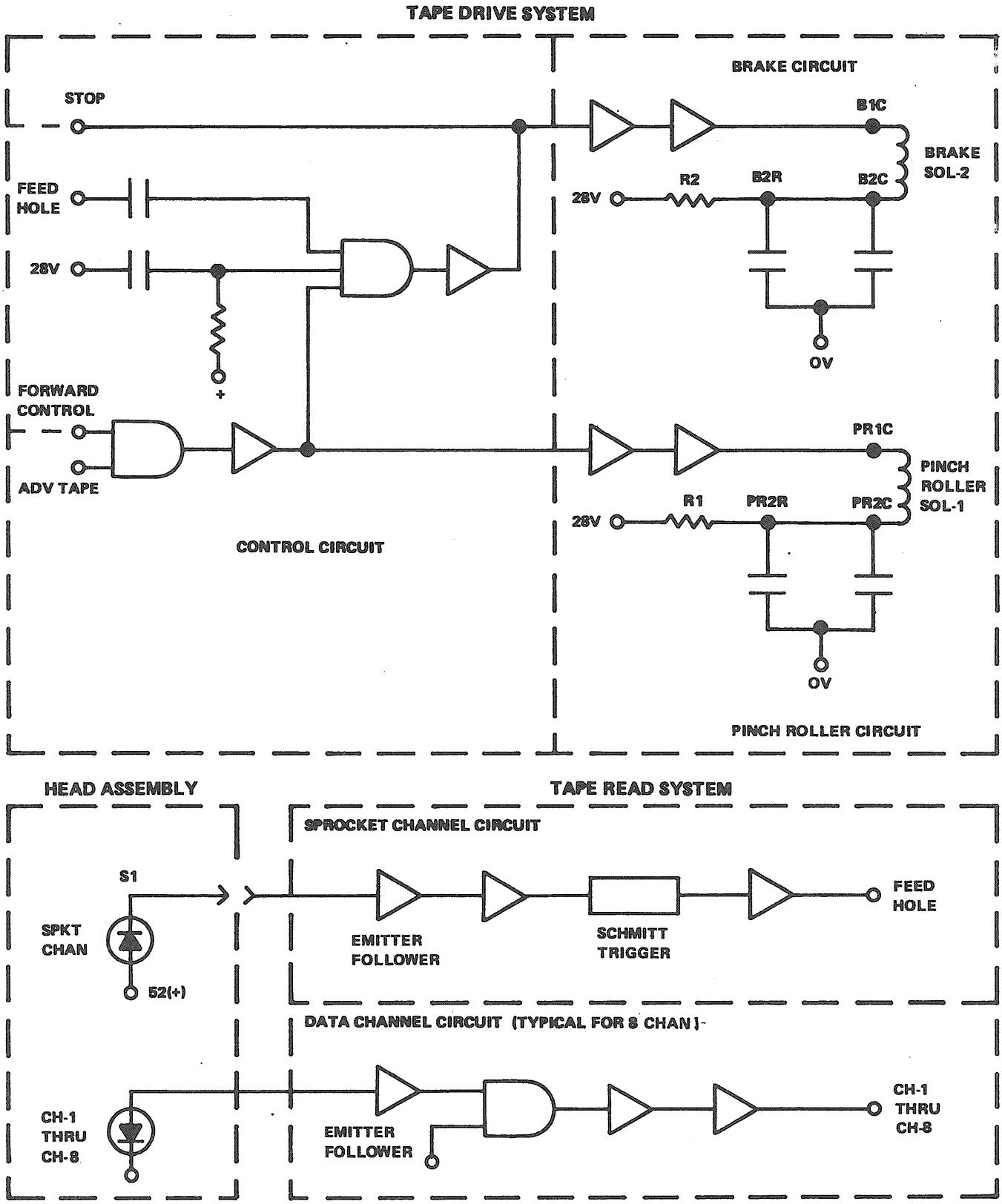


Figure 3-8. Paper Tape Reader Logic Diagram.

3-31. The sprocket channel circuit consists of an emitter follower, inverter amplifier, Schmitt trigger circuit, and a second inverter amplifier. The Schmitt trigger circuit reshapes the sprocket waveform permitting use of the sprocket to gate the data outputs. The sprocket channel output is +5 VDC at 15mA with an 1kΩ external load during a hole condition and 0.0±0.5 VDC during a no-hole condition.

3-32. Tape Drive System. The RUN and STOP control signals to the tape reader are applied to a single input line. The input connector is wired to permit external-signal run/stop control. Tape RUN/STOP control signals are applied as inputs to the pinch roller and brake circuits, controlling the starting and stopping of tape. The tape runs (slews) for the duration of a RUN signal, and stops on receipt of a STOP signal.

3-33. Pinch Roller Circuit. The pinch roller circuit is essentially a noninverting amplifier; the output is used to energize or deenergize the pinch roller solenoid. The pinch roller is controlled by inputs from the control circuit.

3-34. Brake Circuit. The brake circuit is essentially a noninverting amplifier. The output is used to energize or deenergize the brake solenoid, and is controlled by inputs from the control circuit.

3-35. Drive Motor. The drive motor runs continuously when power is applied to the reader. It imparts motion to the tape when the brake is deenergized and the pinch roller is energized.

3-36. Tape Stepping. Tape stepping is controlled by a closed-loop operation (figure 3-9). An initial run pulse is applied by the I/O Console control circuitry. Using the sprocket output (PSP) for synchronization, the I/O control circuits also apply stop signals to the reader. In this manner, the I/O Console controls both the starting and stopping of tape. The reader is capable of stepping tape at any rate up to slew speed. Due to the synchronization between the paper tape reader and the I/O Console, this capability is possible. The stepping rate can be increased to a point where the pinch roller and brake are never fully deenergized and energized respectively. At this point the tape will begin slewing. For instance, if there is no delay involved for the external equipment to process the data received from the reader, the I/O Console can generate another run pulse at the same time that data is received.

3-37. TAPE PUNCH OPERATION. The tape punch set is an electromechanical apparatus that punches information on paper tape. Information is received from external control circuits as combinations of electrical code pulses. Code pulses which enter the tape punch as electrical impulses are translated into mechanical motions that punch corresponding combinations of code holes in the tape. The code pulses are accompanied by a feed pulse which causes the equipment to advance the tape.

3-38. Information is received by the punch in the form of a binary permutation code. The units of the information (characters, numerals, etc.) are represented by combinations of binary intelligence (bits), each of which may be in one of two states, such as on or off, yes or no, 1 or 0.

3-39. Figure 3-10 illustrates a 6-level code. The code is expressed in either electrical or tape form. In electrical form, each level of the code combinations consists of either a current condition (referred to as a marking pulse) or no-current condition (spacing pulse). Figure 3-10B is a graphic representation of a 6-level code combination with alternate marking and spacing levels. In tape form, the characters are represented by combinations of code holes.

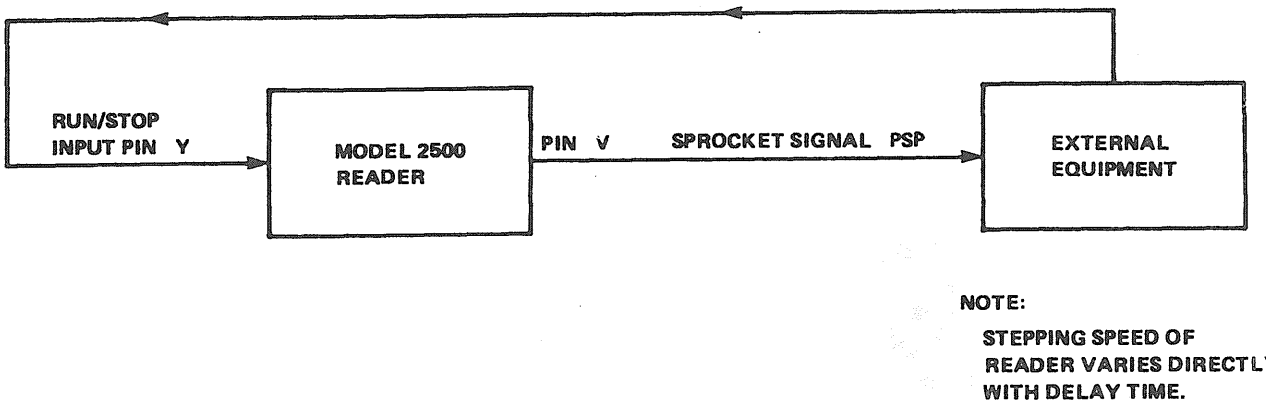


Figure 3-9. Paper Tape Stepping Control.

Each intelligence level consists of either a hole (corresponding to a marking pulse) or the absence of a hole (corresponding to a spacing pulse). The electrical combination of figure 3-10B is shown in tape form in figure 3-10C. Code and feed hole configurations for the different levels of tape are illustrated in figure 3-10D.

3-40. Since the punch cycles continuously, the feed and code pulses must be introduced at a specific time to be properly processed by the punch. The punch produces synchronizing (or clock) pulses which cause the external control circuits to apply a feed pulse and release any code combination they have in storage.

3-41. **DETAILED FUNCTIONAL DESCRIPTION.**

3-42. SYMBOLOGY. The following paragraphs discuss logic levels, circuitry, symbology and component notations used in the I/O Console. A figure accompanies each topic to aid in the explanation and understanding of that area of the symbology.

3-43. Internal Logic Levels. The internal logic levels are referred to as highs (0 volts) and lows (-4.5 VDC). If a low level is needed to satisfy a particular logic function, a circle is drawn on the input line. If a high level is needed, there is no circle. In the same manner, the presence of a circle on the output lead implies that a low level exists if the function is satisfied. The absence of a circle indicates a high level. See figure 3-11 for an illustration of circle level notation.

3-44. AND Logic Function. The AND logic function is performed by a circuit referred to as an AND gate. This gate is identified by a special symbol. To satisfy an AND gate, all of the inputs must be present at the indicated levels (circle notation). When the gate is satisfied, the indicated output level is present. See figure 3-12 for the four basic AND configurations with truth tables. These examples use only two inputs, but there can be many more. Regardless of number, the inputs must all be at the indicated level to satisfy the AND gate.

3-45. Detailed Analysis. See figure 3-13 for a schematic description of the AND gate. Current flows from the -15 VDC supply through the 2.4kΩ, 470Ω, and 6.8kΩ resistors to the 15-VDC supply. A voltage is developed across the 470Ω resistor of the polarity shown. If both inputs A and B are at low levels, the voltage applied to the transistor base

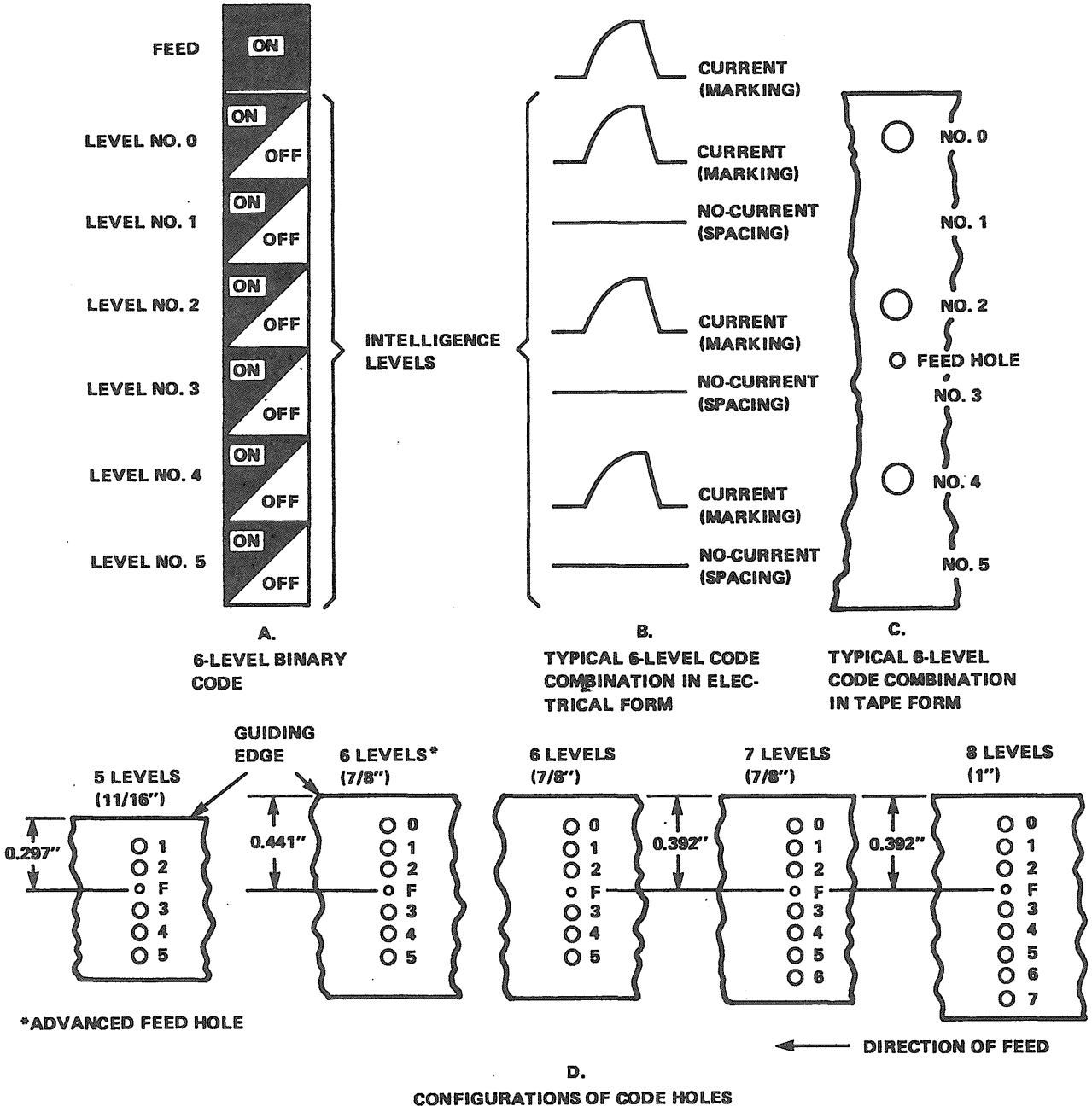


Figure 3-10. Binary Permutation Code.

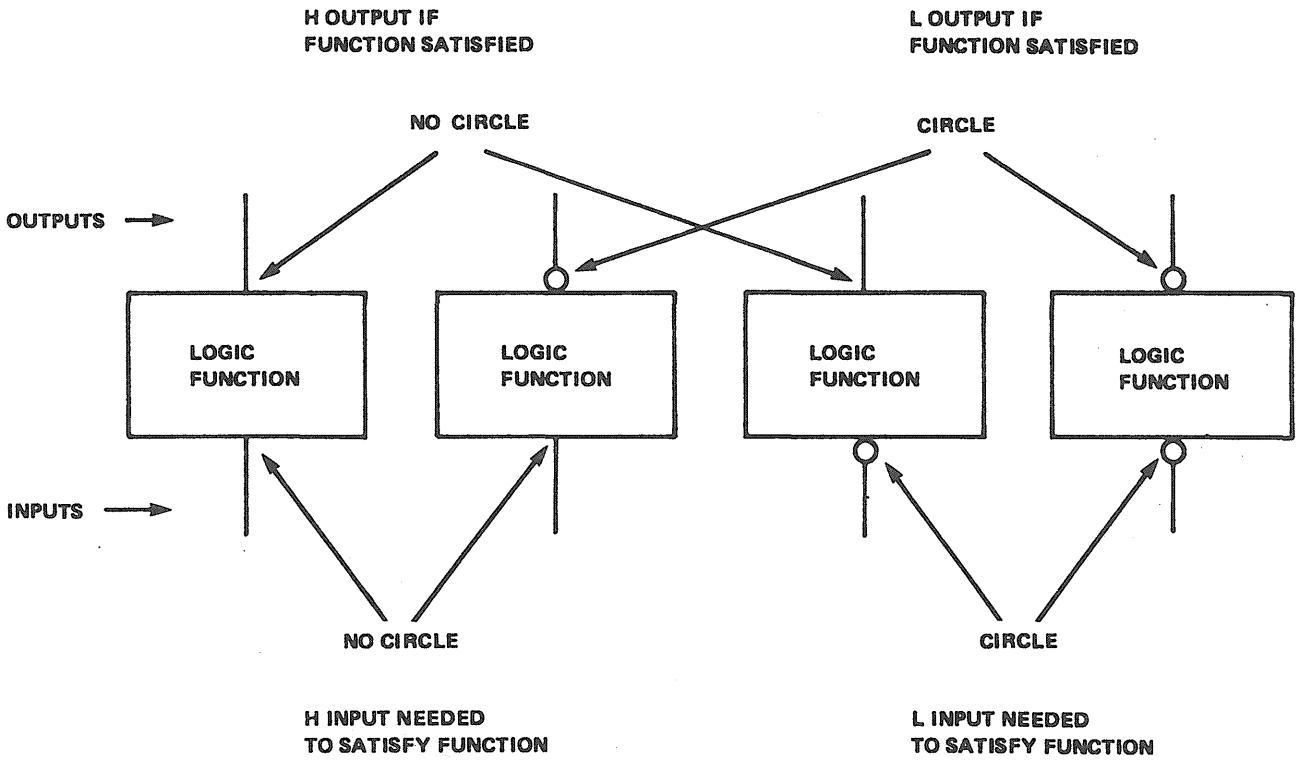
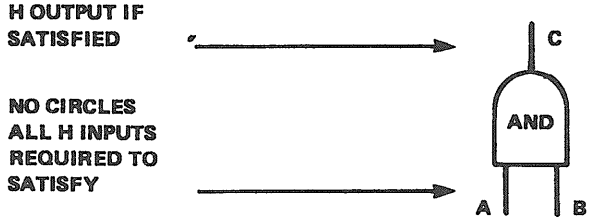


Figure 3-11. Illustration of Circle Level Notation.

with respect to emitter (ground) is negative which forward-biases the transistor. As a result, current flows from the -4.5 VDC supply through the collector to the emitter, and the to ground. In this condition, the output is at ground potential because of the low internal resistance of the collector-to-emitter path. If either A or B inputs (or both) is at a high level (ground), current flows from the -15 VDC supply through the 2.4kΩ resistor and input diode. The low internal resistance of the input diode gives an effective ground level on the left side of the 470Ω resistor. The voltage drop across this resistor of the polarity shown becomes the transistor bias which cuts off the transistor. Depending upon the load, approximately -4.5 VDC is present at the output.

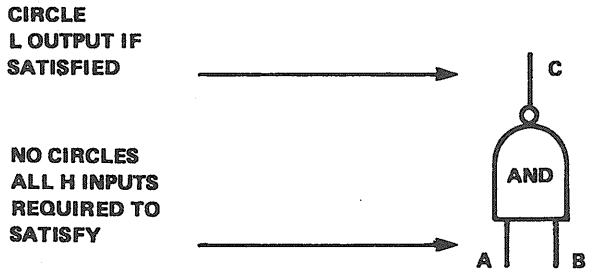
3-46. OR Logic Function. The OR logic function is performed by a circuit referred to as an OR gate. The gate is identified by a special symbol. To satisfy an OR gate, at least one of the inputs must be present at the indicated level. When the gate is satisfied, the indicated output level is present. An OR gate can be drawn as an equivalent AND gate. See figure 3-14 for the four basic configurations with truth tables and equivalent AND gates. These examples use only two inputs. There can be many more inputs. Regardless of the number, at least one input must be at the indicated level to satisfy the OR gate.

3-47. Detailed Analysis. See figure 3-15 for schematic description of the OR gate. Current flows from the -15 VDC



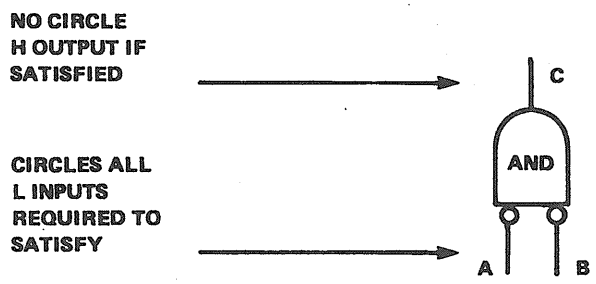
INPUTS		OUTPUT
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

A. HIGH INPUTS, HIGH OUTPUT



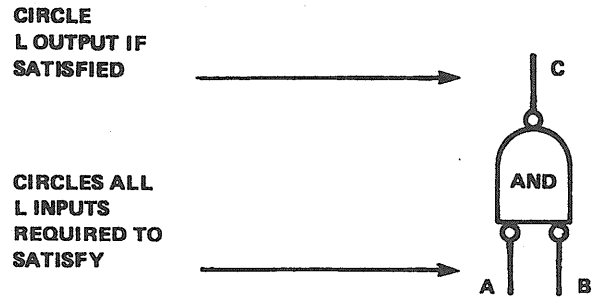
INPUTS		OUTPUT
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

B. HIGH INPUTS, LOW OUTPUT



INPUTS		OUTPUT
A	B	C
L	L	H
L	H	L
H	L	L
H	L	L

C. LOW INPUTS, HIGH OUTPUT



INPUTS		OUTPUT
A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

D. LOW INPUTS, LOW OUTPUT

Figure 3-12. Basic AND Gates.

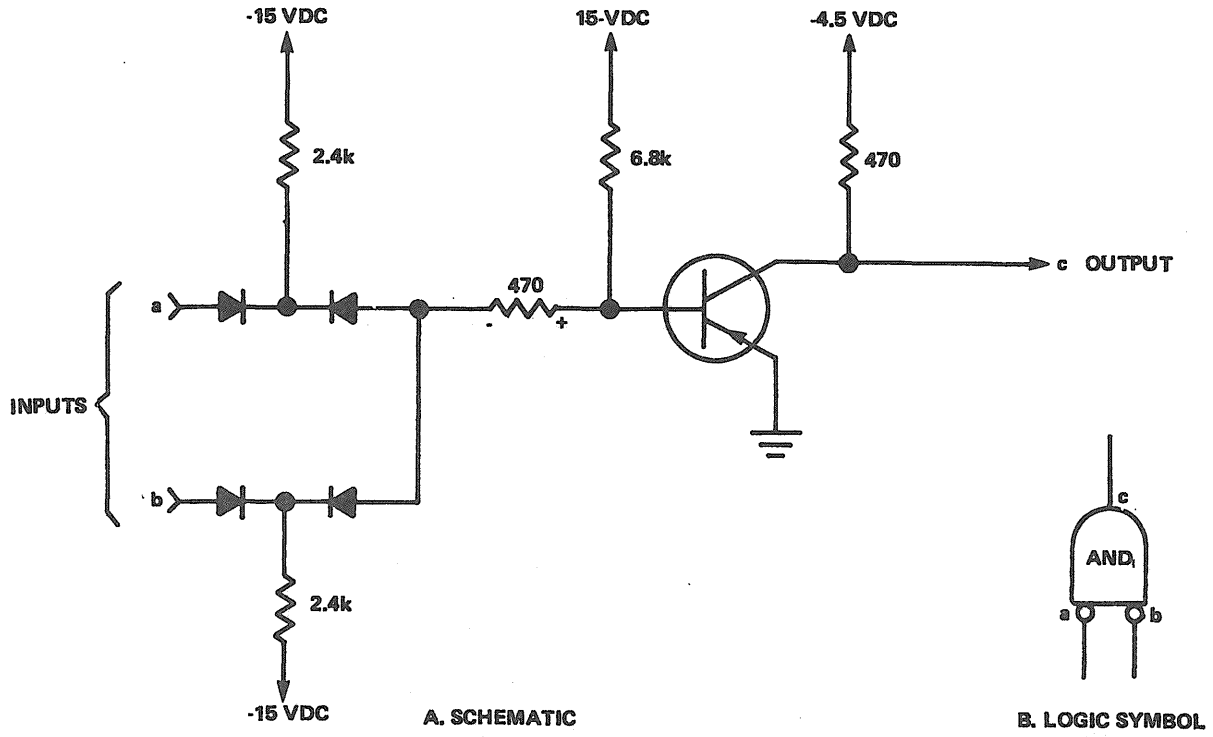
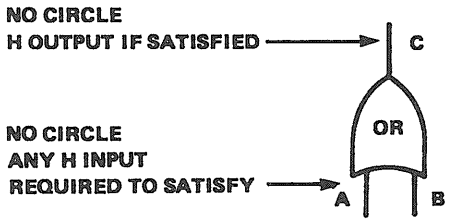


Figure 3-13. Low Input, High Output AND Gate.

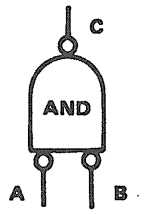
supply through the 470Ω resistor to the 15-VDC supply. A voltage is developed across the 470Ω resistor of the polarity shown. If both inputs A and B are at high levels (ground), current flows from the -15 VDC supply through the 2.2kΩ resistors and the input diodes. This ground level is applied to the left side of the 470Ω resistor which causes its voltage drop to be cut off and the -4.5 VDC supply is felt as the output. If either input is at a low level, that low level is applied to the left side of the 470Ω resistor. If a ground is applied to the other input, its coupling to the 470Ω resistor is reverse-biased and cut off. The resulting negative voltage applied to the transistor forward-biases it to cause collector-to-emitter current flow from the -4.5 VDC supply. The output is at ground level because of the relatively low internal resistance of the transistor.

3-48. AND/OR Combination Logic Function. AND and OR circuits can be combined into one gate. See figure 3-16 for an example of an AND/OR gate. Both logic symbols represent the same circuits. Circuit A performs an OR function of the AND gate inputs. That is, only one input AND gate needs to be satisfied (both inputs at low levels) to satisfy the OR function and produce a high level output. Circuit B performs the same logical operation as circuit A; except if B is satisfied (low level output), A is not satisfied (low level input). In circuit B, input gates are represented as OR functions. All input OR gates must be satisfied (either input at high level for each gate) to satisfy the output AND function. The input AND/OR gates are comprised of diode circuitry.

3-49. Flip-Flop. The flip-flop (F/F) is a bistable device. It has two stable states referred to as set and clear. Flip-flops can be used as temporary storage elements since they can retain either of these states. The set/clear condition represents the information stored. Several flip-flops (registers)

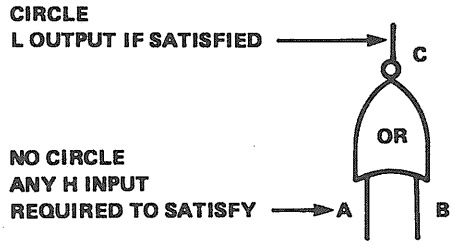


INPUTS		OUTPUT
A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

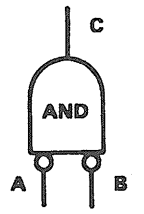


A. HIGH INPUTS, HIGH OUTPUT

EQUIVALENT GATE

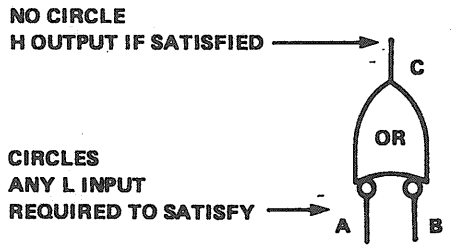


INPUTS		OUTPUT
A	B	C
L	L	H
L	H	L
H	L	L
H	H	L

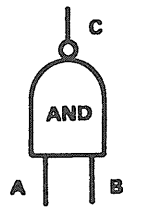


B. HIGH INPUTS, LOW OUTPUT

EQUIVALENT GATE

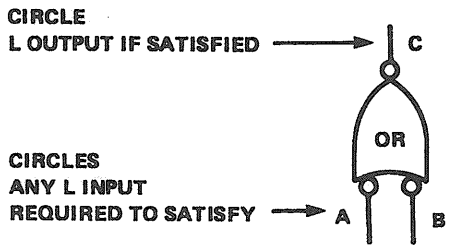


INPUTS		OUTPUT
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

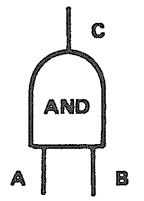


C. LOW INPUTS, HIGH OUTPUT

EQUIVALENT GATE



INPUTS		OUTPUT
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H



D. LOW INPUTS, LOW OUTPUT

EQUIVALENT GATE

Figure 3-14. Basic OR Gates.

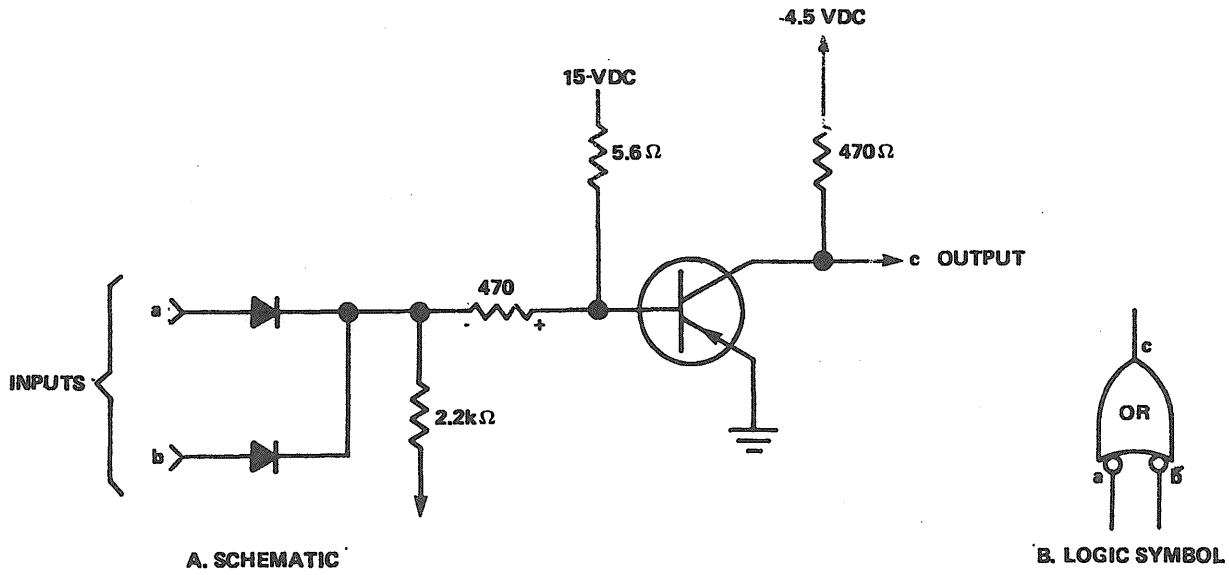


Figure 3-15. Low Input, High Output OR Gate.

can be used to hold a complete binary word. See figure 3-17 for an example of the flip-flop function. The unique circuit number for a flip-flop is slightly different as shown in figure 3-18. The flip-flops have X in their unique terms. In this example, the 1 and 0 sides are referred to by the terms 01I00 and 00I00, respectively. This particular flip-flop is stage 2° of the input register.

3-50. There are several variations concerning the set and clear inputs. If the clear input was circled, a low level would be required to clear. The clear input may also have an AND gate such that the coincidence of several conditions may be necessary to perform the clearing. If the flip-flop is to hold a binary bit, it is usually cleared first (cleared state represents 0_2) and then set (set state represents 1_2). The output conditions for the two states hold true for any flip-flop, regardless of the set and clear input configuration. The 1 side output lead is always circled to indicate a low level when set.

3-51. Component Notation. Each circuit has a unique reference number which no other circuit has. Also, the printed circuit card type number and card location within the machine is noted. See figure 3-19 for an example of logic gate notations.

3-52. PRINTED CIRCUIT MODULES. The I/O Console uses 25 or 26 different types of circuit cards, depending on the interface operation. Two unique cards are used for slow interface (-15 VDC), and three unique cards are used for fast interface (-3 VDC). Adjustment procedures for time delay (TD) cards are included in maintenance requirement cards. Descriptions and logic symbols for each card are illustrated in figures 3-20 through 3-48.

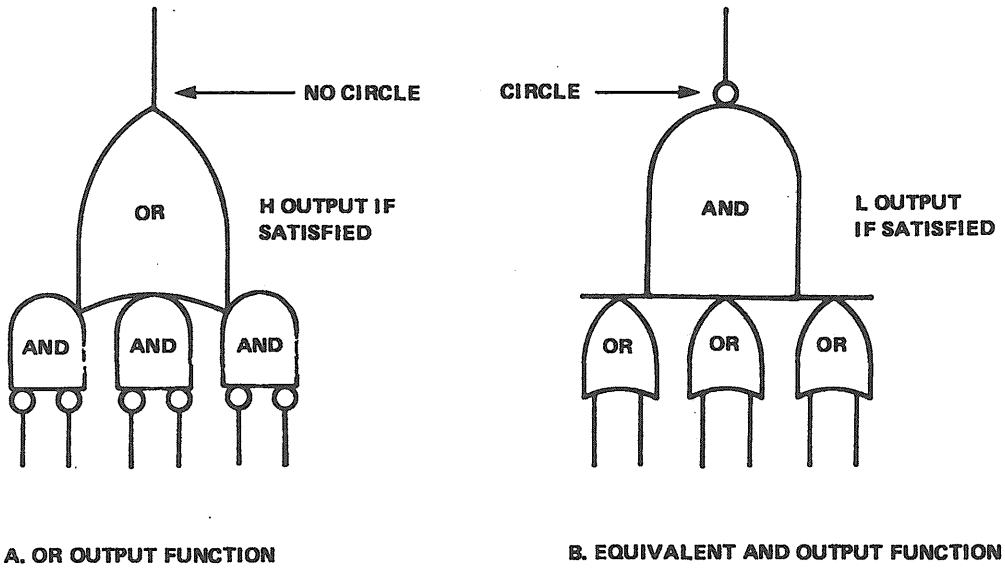


Figure 3-16. AND/OR Combination Gate.

3-53. These circuit cards, prefixed by 700, are color-coded with four bands. The code is read the same as that for resistors. The color code is applicable to the last four digits of the type number. A card with brown (1), yellow (4), gray (8), and green (5) bands would be a type 7001485 card. The dash number following the least significant digit in the card type number gives the revision of the basic card; that is, if card type 7001480 has been revised five times, it would then be listed as card type 7001480-05. Any newly revised card type can replace an old card; however, an older revision card should not be substituted for a new card. The card type numbers and the functional schematics that follow need not be updated if a newly revised card is released, since the new revision replaces the old card.

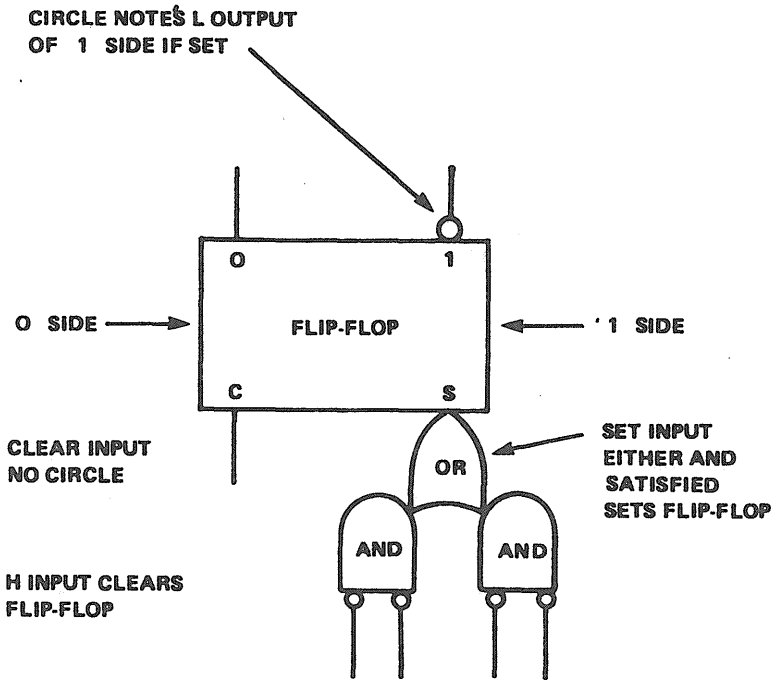
3-54. Printed Circuit Card Location. A chassis map is provided in figure 5-20 to show the layout of the printed circuit card chassis. The map illustrates location and type number of each printed circuit card used in the I/O Console. In addition, the chassis map includes the number of circuits available on each card, logic notations for those circuits that are used, spare circuits on each card, and spare connectors on the chassis. The following pertains to the printed circuit card shown in location A9 on figure 5-20:

a. Contains a type 2830 TD.

b. The card contains two circuits, labeled 18D01(5) and 52D01(6) on the functional schematics.

c. The number 5 indicates that the circuit identified is found on figure 5-5.

3-55. Functional Description of Printed Circuit Cards. Figures 3-20 through 3-48 illustrate and describe each printed circuit card used in the I/O Console. The descriptions are functional since they describe each circuit in terms of its inputs and outputs rather than its internal electronic operation. Whenever possible, inputs and outputs are defined as lows or highs. In the I/O Console, a low always implies a potential of -4.5 VDC, and a high always implies ground potential or 0.0-VDC. On the transmission lines, a high implies ground potential (0.0-VDC) and a low implies a negative potential (-3 or -15 VDC).



STATE	OUTPUT	
	0 SIDE	1 SIDE
SET	H	L
CLEAR	L	H

Figure 3-17. Flip-Flop.

3-56. Each printed circuit card description contains the following information:

a. Card name and type number

b. Symbol used to represent the card on the functional schematics

c. A logic description and a design description

d. Input and output pin numbers for each circuit on the card

e. Power requirements.

3-57. LOGIC DESCRIPTION (ON-LINE MODE).

3-58. WORD FORMATS. Requests, interrupts and data are exchanged between the computer, the I/O Console and the input/output devices via bit-position encoded words. The following paragraphs describe the interface words and reference figures showing their format.

3-59. Input and Output Data Words. To initiate an input/output operation with the I/O Console, the computer places an appropriate external function data word on the output data lines and sets the external function acknowledge line. The I/O Console circuitry samples the data word and enables the selected device. If an output device is selected, the I/O Console sets the output register line. The computer then sets the appropriate output data lines and the output acknowledge line which enables gating of data into the output register. From the output register, the data is gated either to the printer or tape perforator, or both. After each print/punch cycle, the output register is cleared and the output request line is set. This operation is repeated until all desired data is transferred to the I/O Console, at which time the computer terminates the operation.

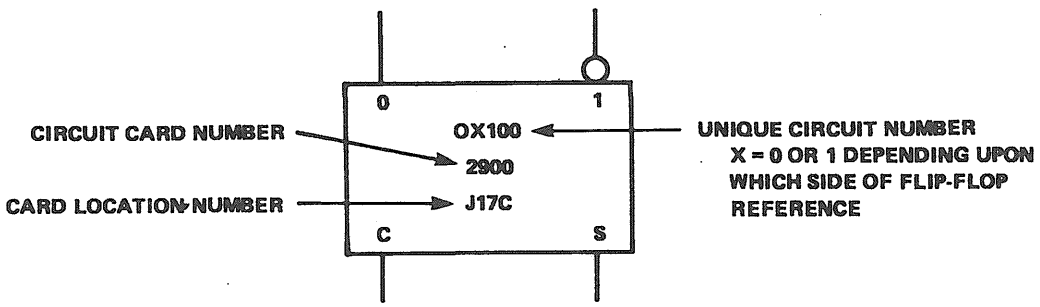


Figure 3-18. Flip-Flop Notation.

3-60. The input data is placed in the input register via the keyboard or reader, and the input request line is set. The computer detects the input request, samples the data, and sets the input acknowledge line which clears the input register. After one keyboard/reader operation, the cycle is repeated until all desired data is transferred to the computer, at which time the computer terminates the operation.

3-61. External Function Words. In the on-line mode, the I/O Console is controlled by external function words. These external function words are instruction words sent, under program control, from the computer to the I/O Console to select an output device (paper tape punch, printer) or input device (paper tape reader, keyboard) for data handling. The external function word is a seven-bit, position-encoded word composed of logic highs and lows. The position and number of highs and lows in the external function code word determine which device is to be selected. (Refer to table 3-2 for the external function code format.) For any output operation, the output control enable bit (2^0) must be set in addition to the device selection bit (bit 2^1 for the printer or bit 2^2 for the tape perforator). To disable the operation of an output device, the output control enable bit must be set, and the device selection bit cleared. Similarly, for any input operation, the input control enable bit (bit 2^3) must be set in addition to the device selection bit (bit 2^4 for the keyboard, or bits 2^5 and 2^6 for the paper tape reader). To disable the operation of an input device, the input control enable bit must be set, and the device selection bit cleared.

3-62. CONTROL LOGIC, GENERAL. Upon receipt of an external function word, control logic within the I/O Console enables the selected device or devices. The sequence of events that takes place at this time (figure 3-49) is as follows:

a. The I/O Console continuously holds the external function request line set, except when not in a condition to accept an external function message.

b. The computer detects the external function request.

c. The computer, under program control, initiates an external function buffer.

d. The computer places the external function word on the output data lines.

e. The computer sends the external function acknowledge, indicating that an external function word is ready for sampling.

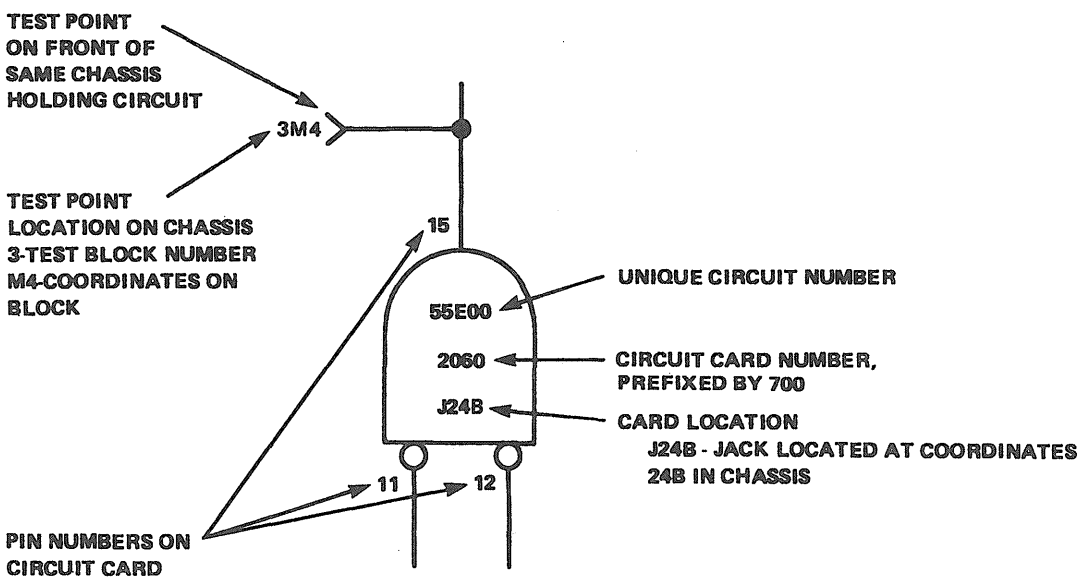


Figure 3-19. Logic Gate Notation.

f. The I/O Console detects the external function acknowledge and clears the external function request.

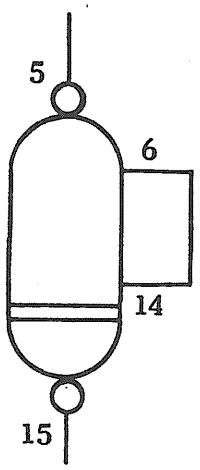
g. The I/O Console samples the external function word and enables or disables the requested input or output device.

h. The computer clears the external function acknowledge and the output lines.

3-63. CONTROL LOGIC, DETAILED. See the referenced logic diagrams for the following detailed analysis of the general on-line control circuitry. Amplifier driver card 40D00 (5-5, 3C) normally outputs 0 volts, representing an external function request (EF REQ) to the computer. The computer responds to the EF REQ and, under program control, initiates the external function buffer, places an external function word on the output data lines, and sends an external function acknowledge (EF ACK) to the I/O Console.

3-64. I/O Console Control Enables. Input amplifier 17D01 (5-5, 4B) converts the EF ACK from the computer to an I/O logic low (-4.5 VDC) and, because of delay circuit 18D01 (5-5, 4B), enables 19D01 (5-5, 4C) for 2µsec. The 2µsec high pulse from 19D01 partially enables both the set and clear sides of PUNCH F/F 0XD02 (5-5, 5D) through inverter 20D02 (5-5, 5C) and gate 20D01 (5-5, 5C) respectively. The low when EF ACK from 20D02 also partially enables both the set and clear sides of PRINT F/F 0XD01 (5-6, 7C). The high when ON-LINE AND EF ACK from 19D01 is inverted by 21D00 (5-6, 6B), KEYBOARD 28D00 (5-6, 4B) and gate 27D00 (5-C, 3C).

3-65. Clear OFF-LINE and Disable External Function Request. On figure 5-5 the low from 20D01 (5-5, 5B) clears OFF-LINE F/F 00D03 (5-5, 5D). This 2µsec pulse is stretched to 70 msec by 22D00 (5-5, 3C) and inverted by 36D00 (5-5, 3C) to disable 40D00 (5-5, 3C) and prevent an EF REQ during this time. At the end of 70 msec, the output of 22D00 goes high,



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN A LOW IS APPLIED TO PIN 15, THE OUTPUT GOES TO LOW AT THE END OF THE DELAY. WHEN THE LOW IS REMOVED FROM THE INPUT, THE OUTPUT GOES TO HIGH. WITH PIN 14 CONNECTED TO PIN 6, THE DELAY TIME IS 2 SECONDS.

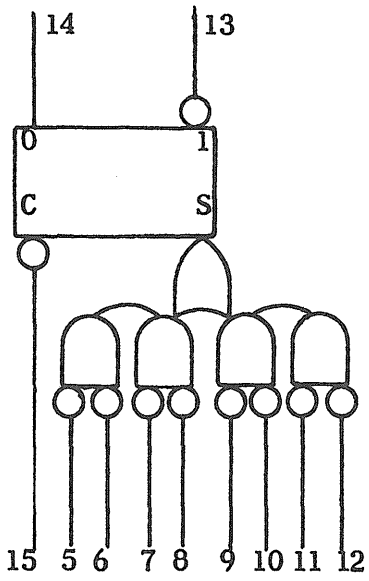
ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC and -0.4 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.8 VDC AND -5.2 VDC. THE EXCURSIONS OF THE OUTPUT PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

LOGIC			
INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER				
PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	-	-	-

Figure 3-20. Inverter, Pulse Delay Card Type 250770.



LOGIC SYMBOL

LOGIC DESCRIPTION

THE RIGHT SIDE OF THE FLIP-FLOP SYMBOL IS REFERRED TO AS THE SET SIDE, AND THE LEFT AS THE CLEAR SIDE.

A LOW INPUT ON THE LEFT SIDE WILL CAUSE A LOW OUTPUT ON THE LEFT SIDE, AND A HIGH OUTPUT ON THE RIGHT SIDE. WHEN ONE OF THE AND GATES ON THE RIGHT SIDE HAS TWO LOW INPUTS, THE OUTPUT ON THE RIGHT SIDE IS A LOW AND THE OUTPUT ON THE LEFT SIDE IS A HIGH.

NOTE

THE INPUT CONFIGURATION CAN BE REVERSED SO THAT THE MULTIPLE-INPUT INVERTER FUNCTIONS AS A SETSIDE INVERTER.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC TO -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 7.1mA. THE CIRCUIT CAN DRIVE FOUR AND GATES PLUS ONE INDICATOR-DRIVER OR 4 AND/OR GATES PLUS ONE INDICATOR-DRIVER.

THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

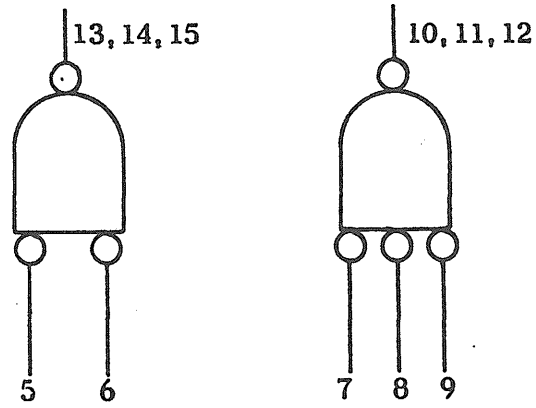
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	64	656	43

Figure 3-21. Flip-Flop, Card Type 7002000.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN ANY OF THE INPUT PINS HAS A HIGH INPUT, THE OUTPUT OF THAT CIRCUIT IS A HIGH. WHEN ALL OF THE INPUT PINS HAVE A LOW INPUT, THE OUTPUT OF THAT CIRCUIT IS A LOW.

ELECTRICAL DESCRIPTION

THE CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE EXCURSIONS BETWEEN 0.0- TO -0.5 VDC AND -3.6 TO -5.4 VDC. THE OUTPUT VOLTAGE EXCURSION IS THE SAME AS THOSE GIVEN FOR THE INPUT VOLTAGE PULSE.

THE MAXIMUM INPUT CURRENT REQUIRED IS 5.8mA. THE CIRCUIT CAN DRIVE SIX AND/OR GATES OR SIX AND GATES FROM EACH OUTPUT PIN, FOR A TOTAL OF 18 CIRCUITS.

THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED.

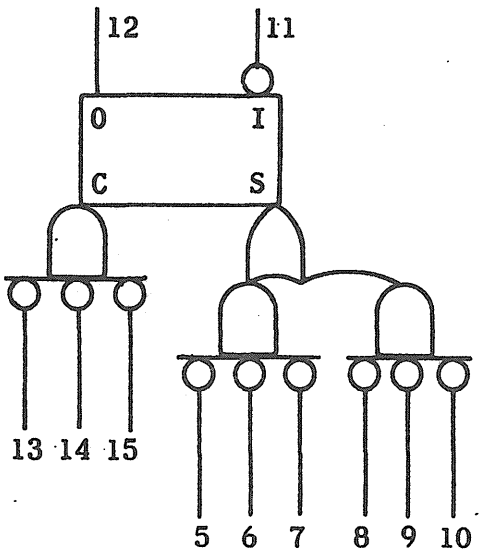
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	194	200	496

Figure 3-22. Amplifier Driver, Card Type 7002013.



LOGIC SYMBOL

LOGIC DESCRIPTION

THE RIGHT SIDE OF THE FLIP-FLOP SYMBOL IS THE SET SIDE, AND THE LEFT THE CLEAR SIDE.

WHEN AN AND GATE ON THE RIGHT SIDE HAS ALL LOW INPUTS, THE OUTPUT ON THE RIGHT SIDE IS A LOW AND THE OUTPUT ON THE LEFT SIDE IS A HIGH. WHEN THE AND GATE ON THE LEFT SIDE HAS ALL LOW INPUTS, THE OUTPUT ON THE LEFT SIDE IS A LOW AND ON THE RIGHT SIDE THE OUTPUT IS A HIGH.

NOTE

THE INPUT CONFIGURATION CAN BE REVERSED SO THAT THE MULTIPLE-AND GATES FUNCTION AS THE CLEAR SIDE.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC TO -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC TO -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 7.1mA. THE CIRCUIT CAN DRIVE FOUR AND GATES PLUS ONE INDICATOR-DRIVER.

THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

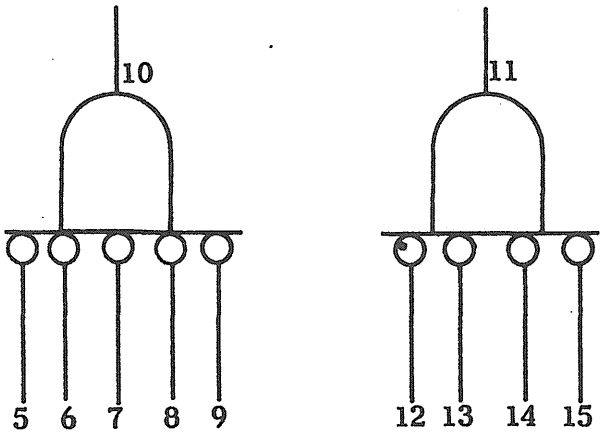
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	64	470	43

Figure 3-23. Flip-Flop, Card Type 7002020.

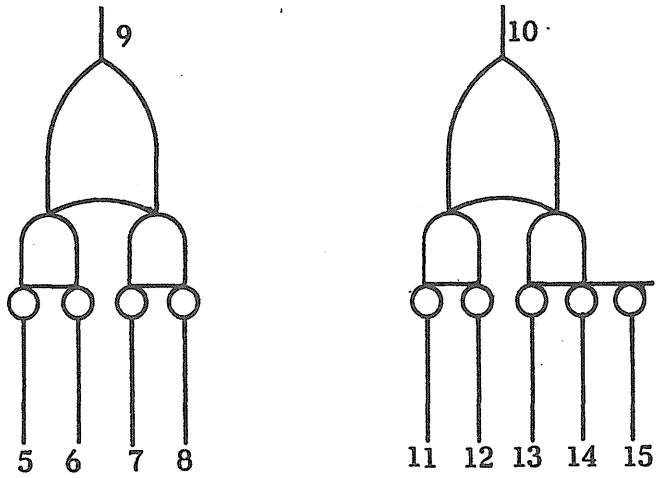


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
WHEN ONE OR MORE INPUTS ARE HIGH, THE OUTPUT IS A LOW. WHEN ALL USED INPUTS HAVE A LOW, THE OUTPUT IS A HIGH.	THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC TO -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC TO -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT. THE MAXIMUM INPUT CURRENT REQUIRED IS 5.8mA. THE CIRCUIT CAN DRIVE FIVE AND/OR GATES OR SIX AND GATES. THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-4.5
0 V	-4.5 V	0 V	-4.5 V	mW	-	80	200	86

Figure 3-24. Inverter, Card Type 7002030.

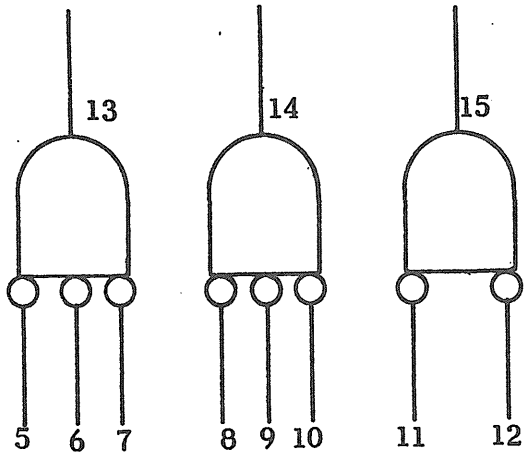


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
WHEN ALL OF THE INPUTS TO EITHER AND GATES ARE LOW, THE OUTPUT OF THE CIRCUIT IS A HIGH. WHEN AT LEAST ONE INPUT TO EACH OF THE AND GATES IS A HIGH, THE OUTPUT IS A LOW. UNUSED AND GATES MUST HAVE A HIGH INPUT.	THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES. THE MAXIMUM INPUT CURRENT REQUIRED IS 6.85mA. THE CIRCUIT CAN DRIVE SIX AND GATES OR FIVE AND/OR GATES. THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-4.5
0 V	-4.5 V	0 V	-4.5 V	mW	-	66	375	86

Figure 3-25. Inverter, Card Type 7002050.

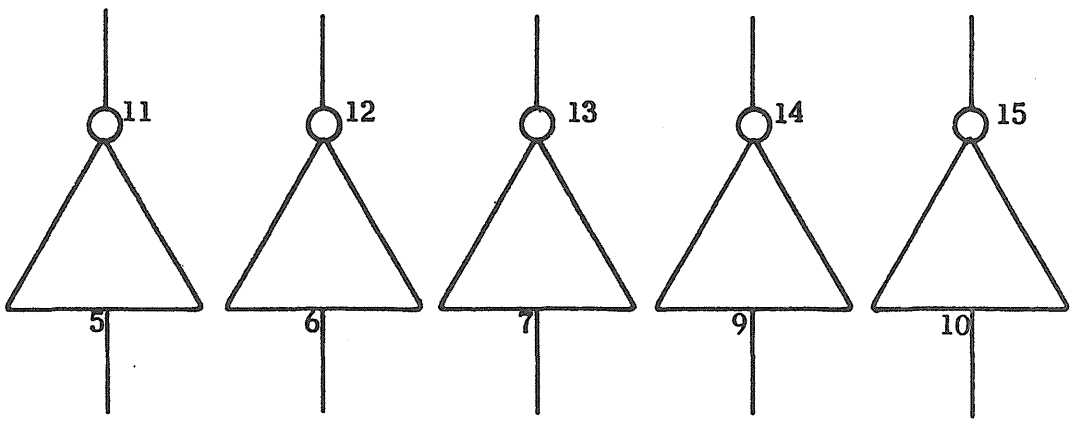


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
WHEN ALL INPUTS ARE LOW, THE OUTPUT IS A HIGH. WHEN AT LEAST ONE INPUT IS A HIGH, THE OUTPUT IS A LOW.	THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES. THE MAXIMUM INPUT CURRENT REQUIRED IS 5.8mA. THE CIRCUIT CAN DRIVE FIVE AND/OR GATES OR SIX AND GATES. THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-4.5
0 V	-4.5 V	0 V	-4.5 V	mW	-	120	300	129

Figure 3-26. Inverter, Card Type 7002060.



LOGIC SYMBOL

LOGIC DESCRIPTION

THE 7002070 INVERTER MODULE CONTAINS FIVE INVERTERS. A LOW INPUT PRODUCES A HIGH OUTPUT, AND CONVERSELY, A HIGH INPUT PRODUCES A LOW OUTPUT.

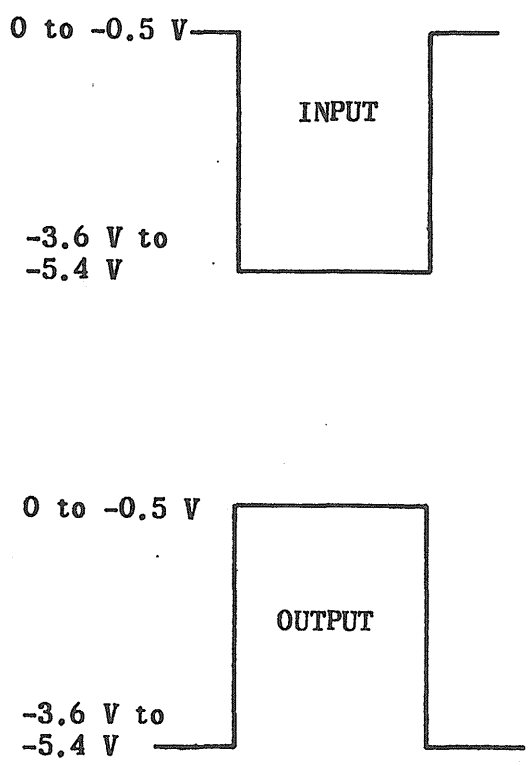
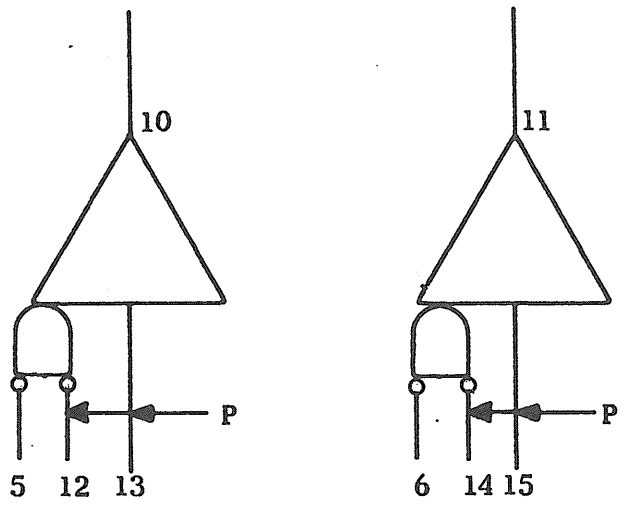


Figure 3-27. Inverter, Card Type 7002070.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THE INPUT TO PIN 12 IS -15 V, AND THE INPUT TO PIN 5 IS A LOW, THE OUTPUT IS A HIGH. WHEN THE INPUT TO PIN 12 IS 0 V AND THE INPUT TO PIN 5 IS A LOW, THE OUTPUT IS A LOW. WHEN THE INPUT TO PIN 5 IS A HIGH, THE OUTPUT IS A LOW, REGARDLESS OF THE OTHER INPUT. PIN 13 IS THE GROUNDED RETURN OF THE TWISTED PAIR.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -13.5 VDC AND -16.5 VDC. THE GATING INPUT-PULSES HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC and -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE GATING INPUT-PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 3.7mA. THE CIRCUIT CAN DRIVE TWO AND/OR GATES OR TWO AND GATES.

THIS CIRCUIT IS PRIMARILY USED FOR INTERFACE BETWEEN EQUIPMENT.

THE CIRCUIT DELAY IS 1 TO 2.2 MICRO-SECONDS.

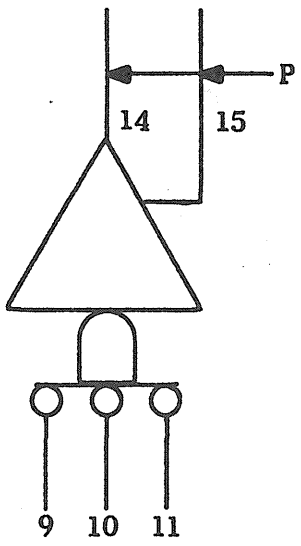
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-15 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	24	96	126

Figure 3-28. Inverter-Input, Card Type 7002090.



LOGIC SYMBOL

LOGIC DESCRIPTION

WITH AT LEAST ONE HIGH INPUT ON AN INPUT LINE, THE OUTPUT ON PIN 14 IS -13.5 V. WHEN ALL THE INPUT LINES HAVE A LOW INPUT PRESENT, THE OUTPUT ON PIN 14 IS 0 V. PIN 15 IS THE GROUNDED RETURN OF THE TWISTED PAIR.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE OUTPUT PULSES HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC and -0.7 VDC, AND NEGATIVE EXCURSIONS BETWEEN -11.0 VDC AND -15.0 VDC.

THE MAXIMUM INPUT CURRENT REQUIRED IS 2.0mA.

BOTH THE RISE AND FALL TIMES ARE CONTROLLED SO THAT THE GREATEST CHANGE IS 5 VOLTS PER MICROSECOND.

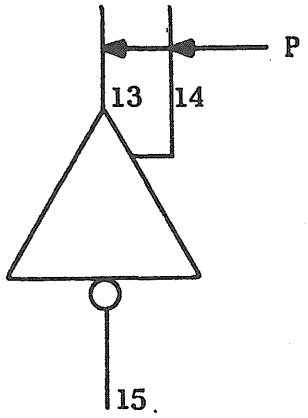
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-13.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	15	630	0

Figure 3-29. Amplifier-Control Driver, Card Type 7002130.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THE INPUT IS A LOW, THE OUTPUT AT PIN 13 IS 0 V. WHEN THE INPUT IS A HIGH, THE OUTPUT AT PIN 13 IS -13.5 V. PIN 14 IS THE GROUNDED RETURN OF THE TWISTED PAIR.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -1.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE OUTPUT PULSES HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC and -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -10.0-VDC AND -17.0 VDC.

THE MAXIMUM INPUT CURRENT REQUIRED IS 2.25mA.

THE RISE AND FALL TIMES ARE CONTROLLED TO BE LESS THAN 5 VOLTS PER MICROSECOND. THE CIRCUIT CAN DRIVE FOUR TWISTED-PAIR CABLES UP TO 300 FEET IN LENGTH.

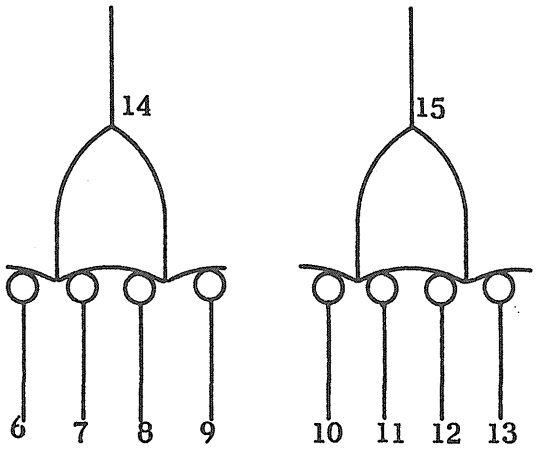
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-13.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	15	450	0

Figure 3-30. Amplifier Driver, Card Type 7002141.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN ANY INPUT IS A LOW, THE OUTPUT IS A HIGH. WHEN ALL INPUTS ARE HIGH, THE OUTPUT IS LOW.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 7.0mA. THE CIRCUIT CAN DRIVE SIX AND GATES OR FIVE AND/OR GATES.

THIS CIRCUIT'S MAXIMUM SPEED IS SUCH THAT THE SECOND OF TWO SERIES-CONNECTED CIRCUITS PRODUCES A USABLE OUTPUT BEFORE THE CLOCK-PHASE INPUT TO THE FIRST HAS EXPIRED. A NORMAL CLOCK-PHASE IS 166 NANOSECONDS LONG.

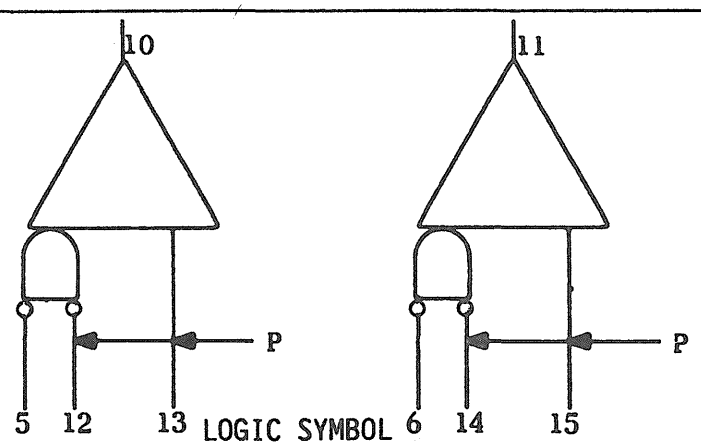
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	66	680	86

Figure 3-31. Inverter, Card Type 7002220.



LOGIC DESCRIPTION

WHEN BOTH INPUTS TO PIN 12 AND PIN 5 ARE LOW, THE OUTPUT IS A HIGH. WHEN THE INPUT TO PIN 12 IS A HIGH AND THE INPUT TO PIN 5 IS A LOW, THE OUTPUT IS A LOW.

WHEN THE INPUT TO PIN 5 IS A HIGH (DISABLE), THE OUTPUT IS A LOW, REGARDLESS OF THE OTHER INPUT. PIN 13 IS THE RETURN OF THE TWISTED PAIR.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT SIGNALS THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC TO -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.0 VDC AND -4.5 VDC.

THE OUTPUT SIGNAL HAS A POSITIVE EXCURSION BETWEEN 0.0-VDC AND -0.4 VDC AND NEGATIVE EXCURSION BETWEEN -3.8 VDC AND -5.2 VDC. THE REQUIRED GATE SIGNAL IS THE SAME AS THE OUTPUT SIGNAL. A GATE SIGNAL BETWEEN 0.0-VDC AND -0.4 VDC HOLDS THE OUTPUT NEGATIVE. THE CIRCUIT MAY BE USED WITH THE GATE OPEN IF DESIRED.

THE MAXIMUM CIRCUIT DELAY AND STORAGE IS 200 NANOSECONDS. THE MAXIMUM INPUT CURRENT REQUIRED IS 1.1mA.

THE CIRCUIT HAS HIGH COMMON-MODE NOISE-REJECTION WHEN USED WITH A TWISTED PAIR CABLE. THE INPUT IMPEDANCE IS BALANCED SO NOISE COUPLED IN ONE CONDUCTOR WILL ALSO BE COUPLED INTO THE OTHER CONDUCTOR.

THE THRESHOLD LEVEL, VOLTAGE DIFFERENCE BETWEEN INPUT CONDUCTORS, IS BETWEEN -1.1 VDC and -1.9 VDC.

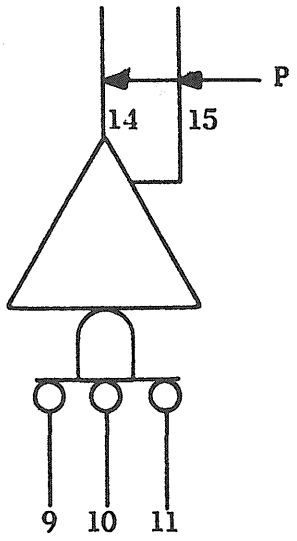
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-3 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	180	225	40

Figure 3-32. Amplifier, Differential, Card Type 7002321.

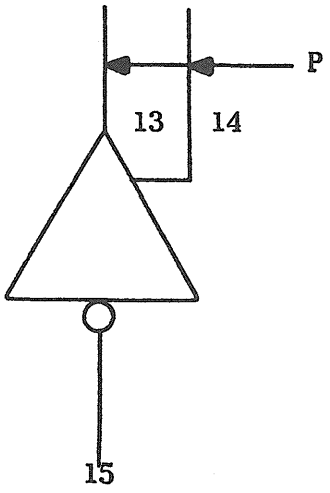


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
WHEN ALL THE INPUT LINES HAVE A LOW INPUT PRESENT, THE OUTPUT ON PIN 14 WILL BE HIGH. WITH AT LEAST ONE HIGH INPUT ON AN INPUT LINE, THE OUTPUT ON PIN 14 WILL BE LOW. PIN 15 IS THE GROUNDED RETURN OF THE TWISTED PAIR.	THIS CIRCUIT CONTAINS HIGH IMPEDANCE FEATURES WITH POWER OFF AND A NEGATIVE VOLTAGE APPLIED FROM A REMOTE SOURCE THROUGH THE CABLE INTO PIN 14. THE CIRCUIT WILL HAVE AN IMPEDANCE NOT LESS THAN 100,000 OHMS.

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-4.5
0 V	-4.5 V	0 V	-3 V	mW	-	130	500	80

Figure 3-33. Amplifier, Control Line, Card Type 7002332.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THE INPUT IS A LOW, THE OUTPUT AT PIN 13 IS 0-VDC. WHEN THE INPUT IS A HIGH, THE OUTPUT AT PIN 13 IS -3 VDC. PIN 14 IS THE GROUNDED RETURN OF THE TWISTED PAIR.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT SIGNALS THAT HAVE A POSITIVE EXCURSION BETWEEN 0.0-VDC AND 0.5-VDC, AND A NEGATIVE EXCURSION BETWEEN -3.8 VDC TO -5.2 VDC. THE OUTPUT HAS A POSITIVE EXCURSION BETWEEN 0.0-VDC and -0.5 VDC, AND A NEGATIVE EXCURSION BETWEEN -3.0 VDC AND -4.5 VDC.

THE MAXIMUM CIRCUIT DELAY AND STORAGE IS 200 NANOSECONDS. THE MAXIMUM INPUT CURRENT REQUIRED IS 4.6mA.

THE MAXIMUM RISE AND FALL TIME WITH THE TWISTED-PAIR CABLE CONNECTED TO THE OUTPUT IS 0.4µSEC BETWEEN THE 10 AND 90 PERCENT AMPLITUDE POINTS.

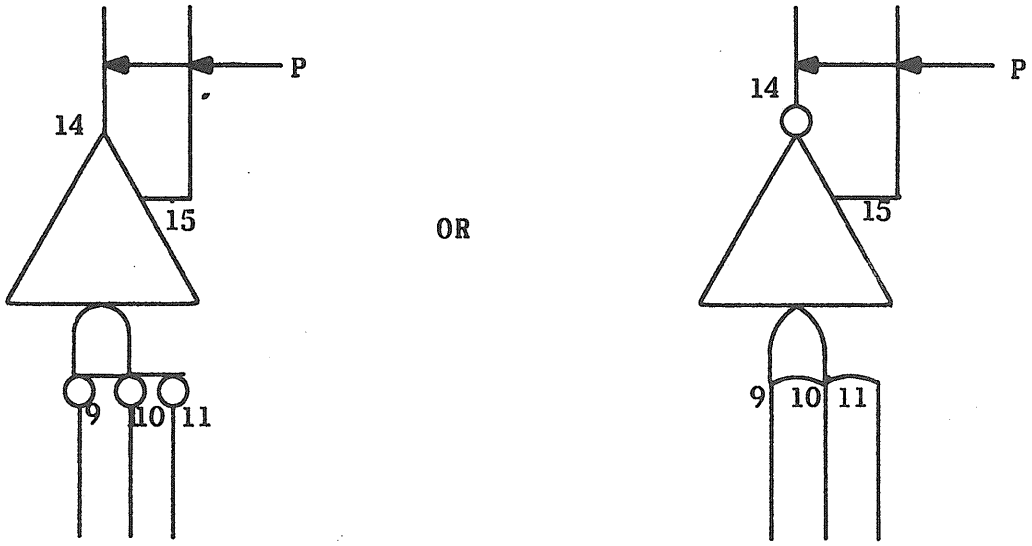
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-3 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	108	561	40

Figure 3-34. Amplifier, Data Line, Card Type 7002342.



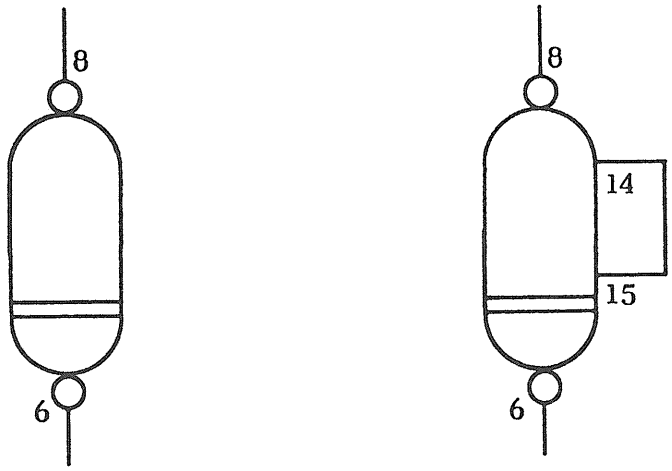
LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
THREE LOW INPUTS (PINS 9, 10, AND 11) CAUSE A HIGH OUTPUT. ANY HIGH INPUT CAUSES A LOW OUTPUT. PIN 15 IS THE GROUND RETURN PATH.	THIS AMPLIFIER OPERATES WITH INPUT PULSES THAT HAVE NOMINAL POSITIVE EXCURSIONS OF -0.3 VDC AND NOMINAL NEGATIVE EXCURSIONS OF -4.5 VDC. THE OUTPUT PULSES HAVE NOMINAL POSITIVE EXCURSIONS OF -0.5 VDC AND NOMINAL NEGATIVE EXCURSIONS OF -6.0 VDC. THE CIRCUIT REQUIRES A MAXIMUM INPUT CURRENT OF 2mA AT 0-VDC. MAXIMUM RISE AND FALL TIMES ARE 3 MICROSECONDS.

LOGIC			
INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-6 V

POWER				
PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	15	630	0

Figure 3-35. Amplifier Driver, Card Type 7002810.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THE INPUT ON PIN 6 OF THE LEFT-HAND DELAY GOES FROM HIGH TO LOW, THE OUTPUT ON PIN 8 GOES IMMEDIATELY LOW, AND RETURNS TO HIGH AT THE END OF THE DELAY PERIOD. THE DELAY IS 9.09 MILLISECONDS IN 9 CIRCUITS, AND 18.8 MILLISECONDS IN ONE CIRCUIT. THE RIGHT-HAND DELAY IN ONE CIRCUIT OPERATES IDENTICALLY EXCEPT IT IS 70 MILLISECONDS.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT AND OUTPUT PULSES THAT HAVE EXCURSIONS OF 0.0-VDC TO -0.4 VDC AND -3.8 VDC TO -5.2 VDC.

THE MAXIMUM INPUT CURRENT REQUIRED IS 3.0 MILLIAMPERES. THE CIRCUIT CAN DRIVE TWO AND/OR GATES OR TWO AND GATES.

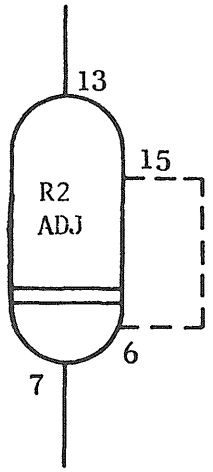
LOGIC

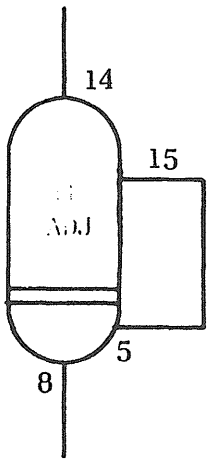
INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	372	0	45

Figure 3-36. Time Delay, Card Type 7002821.





Note: R1 on right side
R2 on left side
as viewed from front of I/O

LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THE CIRCUIT IS QUIESCENT, PIN 7 IS AT GROUND POTENTIAL (0-VDC), AND PIN 13 IS AT A -4.5 VDC POTENTIAL. WHEN A NEGATIVE VOLTAGE IS APPLIED TO PIN 7, THE TIME CONSTANT OF THE INPUT CIRCUIT ALLOWS PIN 13 TO REMAIN AT THE -4.5 VDC POTENTIAL FOR THE CHARGING DURATION. WHEN THE CHARGING OPERATION IS FINISHED PIN 13 GOES TO GROUND (0-VDC) AND REMAINS THERE UNTIL PIN 7 RETURNS TO GROUND. PIN 13 THEN RETURNS TO -4.5 VDC.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.4 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.8 VDC AND -5.2 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 7.0mA. THE CIRCUIT CAN DRIVE ONE AND GATE OR ONE AND/OR GATE.

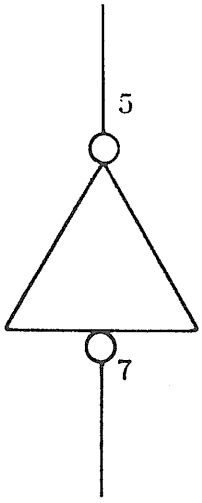
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	132	45	160

Figure 3-37. Inverter Delay, Card Type 7002830.



LOGIC SYMBOL

LOGIC DESCRIPTION

A LOW APPLIED TO PIN 7 CAUSES THE CIRCUIT TO PRODUCE A SLIGHTLY NEGATIVE OUTPUT ON PIN 5. A HIGH (0-VDC) APPLIED TO PIN 7 CAUSES THE CIRCUIT TO PRODUCE A SLIGHTLY POSITIVE OUTPUT ON PIN 5. THIS CIRCUIT SUPPLIES BASE, BIAS CURRENT TO THE POWER TRANSISTOR.

ELECTRICAL DESCRIPTION

THE OUTPUT AT PIN 5 WILL BE BETWEEN 1.2- AND 1.8-VDC MORE POSITIVE THAN THE INPUT SIGNAL OUTLINED IN THE LOGIC DESCRIPTION.

THE MAXIMUM INPUT CURRENT REQUIRED IS 83.0mA PER CIRCUIT.

THE MINIMUM OUTPUT CURRENT IS 54.0mA WITH A NEGATIVE INPUT.

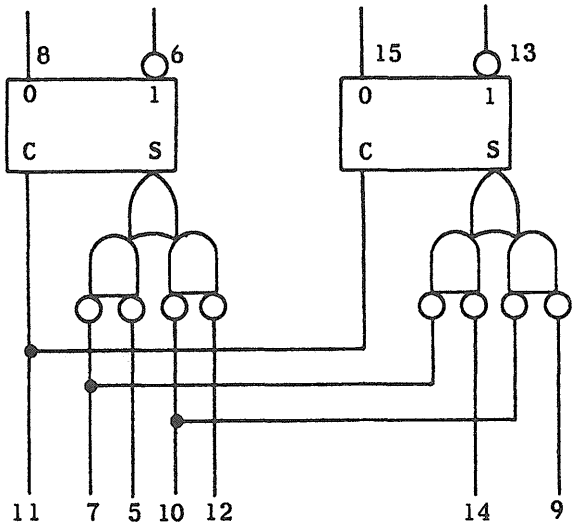
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	-	-

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	66	2W	0

Figure 3-38. Network Bias, Card Type 7002840.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN BOTH INPUTS TO EITHER SET GATE ARE LOW, THE FLIP-FLOP SETS. THE OUTPUT ON THE SET SIDE (PIN 6 & 13) GOES TO A LOW AND THE OUTPUT ON THE CLEAR SIDE (PIN 8 & 15) GOES TO A LOW. THE NORMAL INPUT ON PIN 11 IS A HIGH. WHEN THE INPUT ON PIN 11 GOES TO A HIGH, THE FLIP-FLOP CLEARS. THE OUTPUT ON THE SET SIDE GOES TO A HIGH AND TO A LOW ON THE CLEAR SIDE.

ELECTRICAL DESCRIPTION

THIS ASSEMBLY CONSISTS OF TWO FLIP-FLOP CIRCUITS EACH HAVING TWO 2-INPUT AND/OR GATES AND ONE OR GATE SHARED WITH AN INPUT PIN AND THE OTHER SIDE OF THE FLIP-FLOP. THE NOMINAL POSITIVE EXCURSION OF THE INPUT PULSE IS 0-VDC. THE NOMINAL NEGATIVE EXCURSION OF THE INPUT PULSE IS -4.5 VDC. THE POSITIVE AND NEGATIVE EXCURSIONS OF THE OUTPUT SIGNAL ARE THE SAME AS THOSE FOR THE INPUT PULSE.

THE MAXIMUM CURRENT REQUIRED AT INPUT PINS 5, 9, 12, AND 14 IS 6.85mA AND AT INPUT PINS 7, 10, AND 11 IS 13.7mA WITH THE INPUT AT 0-VDC. EACH OUTPUT PIN IS CAPABLE OF DRIVING FIVE AND OR FOUR AND/OR LOGIC CIRCUITS.

THE MAXIMUM TURN-ON AND TURNOFF TIME FOR EACH LOGIC CIRCUIT IS 50 AND 60 NANOSECONDS RESPECTIVELY.

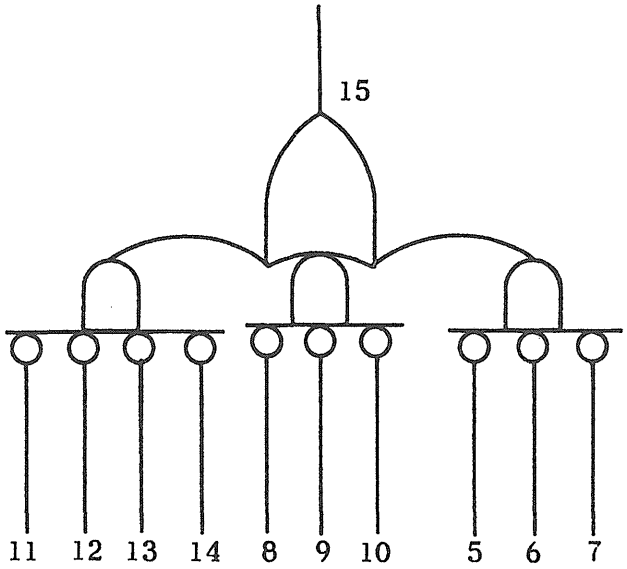
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	125	727	86

Figure 3-39. Flip-Flop, Card Type 7002900.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN ALL INPUTS TO ANY ONE OF THE AND CIRCUITS ARE LOW, THE OUTPUT OF THE CIRCUIT IS A HIGH. CONVERSLY, THE CIRCUIT PRODUCES A LOW WHEN A HIGH INPUT IS PRESENT ON AT LEAST ONE INPUT TO ALL AND CIRCUITS.

ELECTRICAL DESCRIPTION

THIS ASSEMBLY CONSISTS OF A LOGIC INVERTER HAVING THREE INPUT OR GATES. TWO OF THE THREE OR GATES HAVE 3 AND INPUTS AND THE OTHER HAS A 4 AND INPUT. THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE NOMINAL POSITIVE EXCURSIONS OF -0.3 VDC AND NOMINAL NEGATIVE EXCURSIONS OF -4.5 VDC. THE EXCURSIONS OF THE OUTPUT SIGNAL ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

THE MAXIMUM INPUT CURRENT REQUIRED IS 7.1mA AT 0 VDC INPUT. THE CIRCUIT CAN DRIVE FIVE AND/OR GATES OR SIX AND GATES.

THE MAXIMUM TURN-ON AND TURNOFF TIME IS 50 AND 60 NANOSECONDS RESPECTIVELY.

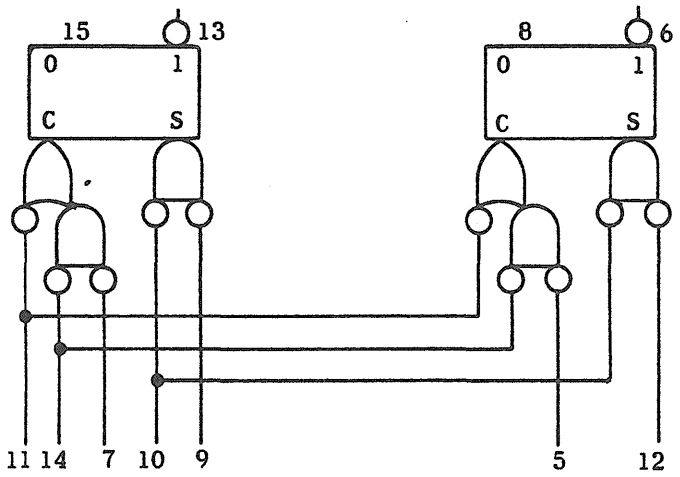
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	-	-	-

Figure 3-40. Inverter, Card Type 7002920.



LOGIC SYMBOL

LOGIC DESCRIPTION

IN THE SET CONDITION, THE OUTPUT AT PINS 13 AND 6 IS LOW; THE OUTPUT AT PINS 15 and 8 IS HIGH. IN ORDER TO SET THE FLIP-FLOP, PINS 9 AND 10, OR 10 AND 12 MUST HAVE A LOW INPUT. IN THE CLEAR CONDITION, THE OUTPUT AT PINS 15 AND 8 IS LOW. IN ORDER TO CLEAR THE FLIP-FLOP, PINS 14 AND 7, OR 14 AND 5 MUST HAVE A LOW INPUT. A LOW INPUT TO PIN 11 WILL ALSO CLEAR BOTH FLIP-FLOPS.

ELECTRICAL DESCRIPTION

THIS ASSEMBLY CONSISTS OF TWO LOGIC FLIP-FLOP CIRCUITS. ONE SIDE OF EACH FLIP-FLOP IS A TWO-INPUT AND GATE; THE OTHER SIDE IS AN OR GATE HAVING A TWO-INPUT AND GATE AND A SINGLE-INPUT AND GATE. ONE INPUT PIN OF EACH AND GATE IS COMMON INPUT TO BOTH FLIP-FLOP CIRCUITS. THE CIRCUIT OPERATES WITH A NOMINAL POSITIVE EXCURSION OF 0-VDC AND A NOMINAL NEGATIVE EXCURSION OF -4.5 VDC. THE EXCURSIONS OF THE OUTPUT SIGNALS ARE THE SAME AS THE INPUT SIGNALS.

THE MAXIMUM CURRENT REQUIRED FOR A SINGLE INPUT PIN IS 7.1mA or 14.2mA FOR A COMMON INPUT PIN AT 0-VDC INPUT. EACH OUTPUT IS CAPABLE OF DRIVING FOUR AND LOGIC CIRCUITS PLUS AN INDICATOR DRIVER, OR FOUR AND/OR LOGIC CIRCUITS PLUS AN INDICATOR DRIVER.

THE MAXIMUM TURN-ON AND TURNOFF TIMES PER LOGIC CIRCUIT ARE 50 AND 60 NANOSECONDS RESPECTIVELY.

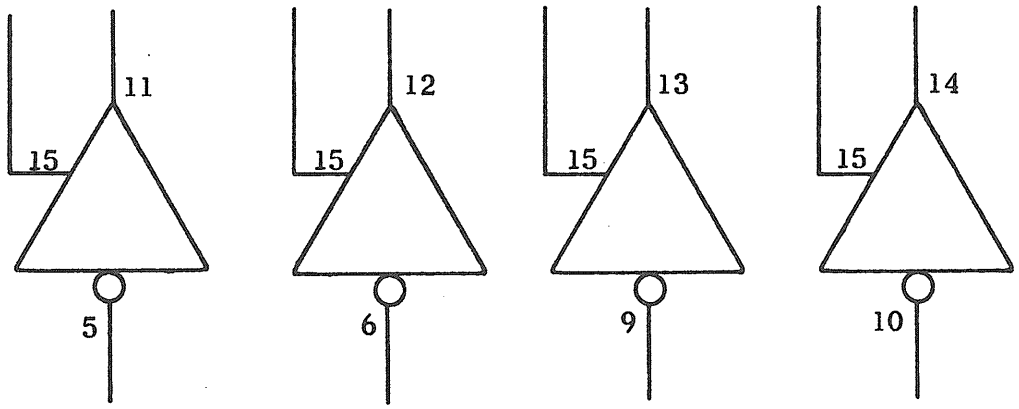
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	132	375	96

Figure 3-41. Flip-Flop, Card Type 7002930.



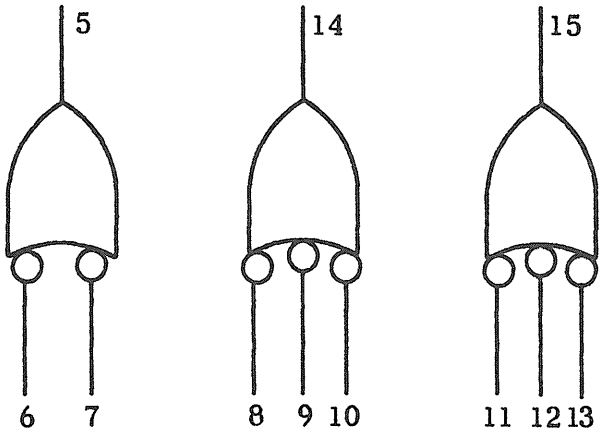
LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
WHEN THE INPUT IS A LOW, THE OUTPUT IS A HIGH. WHEN THE INPUT IS A HIGH, THE OUTPUT IS A LOW.	THE CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.5 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.6 VDC AND -5.4 VDC. THE CIRCUIT REQUIRES AN INPUT CURRENT OF 1mA THE CURRENT HANDLING CAPABILITY OF THE OUTPUT STAGE IS 180mA AT -24 VDC.

LOGIC			
INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	GROUND	OPEN

POWER				
PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	280	-	140

Figure 3-42. Amplifier Driver, Card Type 7002940.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN ALL INPUTS ARE HIGH, THE OUTPUT IS A LOW. WHEN ANY ONE INPUT IS A LOW, THE OUTPUT IS A HIGH.

ELECTRICAL DESCRIPTION

THE CIRCUIT CONSISTS OF TWO 3-INPUT AND ONE 2-INPUT OR INVERTER CIRCUITS. EACH INVERTER HAS ONE OUTPUT PIN.

THE CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE NOMINAL POSITIVE EXCURSIONS OF -0.3 VDC AND NOMINAL NEGATIVE EXCURSIONS OF -4.5 VDC.

THE MAXIMUM INPUT CURRENT REQUIRED IS 6.85mA AT 0-VDC INPUT.

THE MAXIMUM TURN-ON AND TURNOFF TIME IS 50 AND 60 NANOSECONDS RESPECTIVELY.

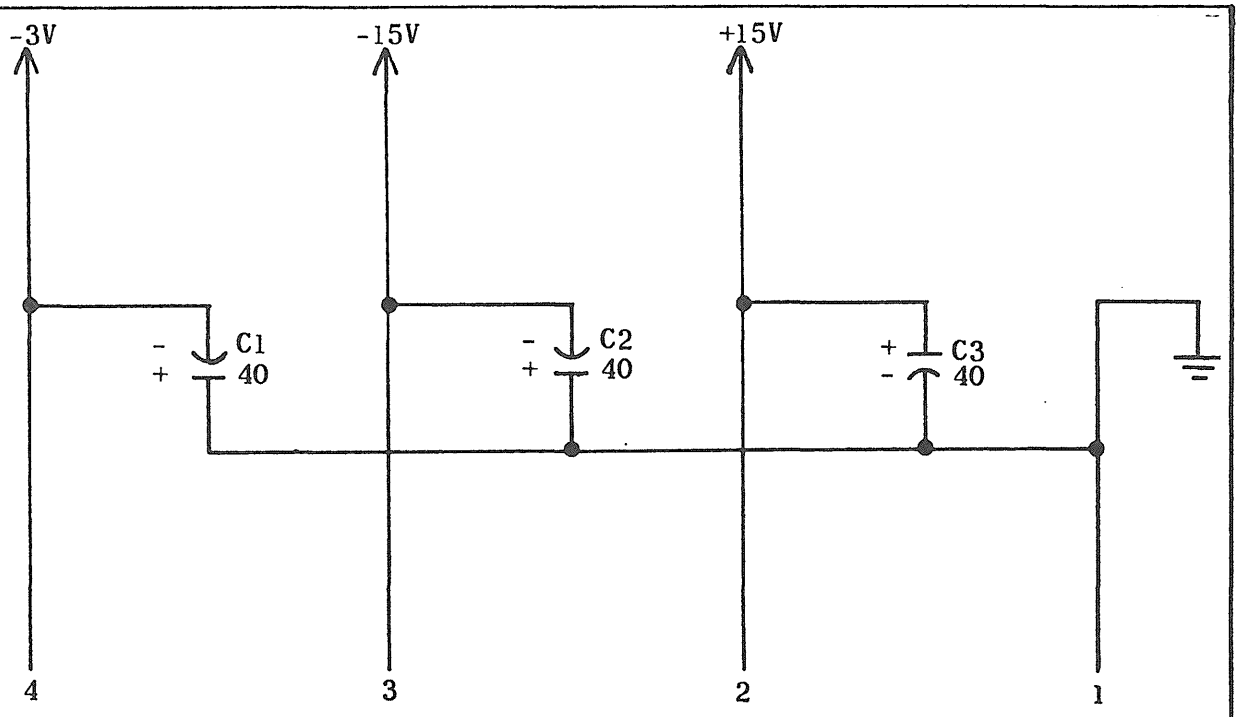
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	-	-	-

Figure 3-43. Inverter, Card Type 7002990.

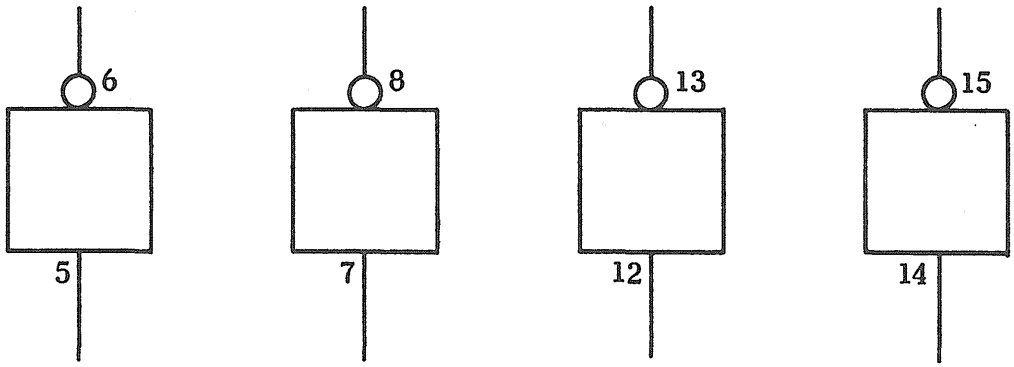


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
THE CAPACITORS ON THIS CIRCUIT CARD CONNECT TO THE VOLTAGE BUSSES AS SHOWN ABOVE. THE CHASSIS MAPS SHOW WHERE THESE CIRCUITS ARE LOCATED.	N/A

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-3
				mW	-	-	-	-

Figure 3-44. Capacitor Assembly, Card Type 7003180.

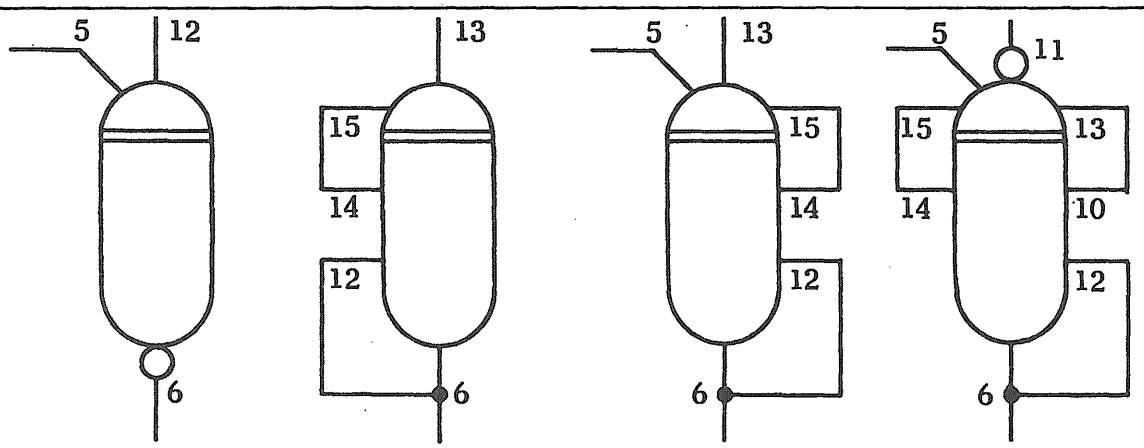


LOGIC SYMBOL

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
THE CIRCUITS OF THIS CARD ARE SINGLE-SHOT MULTIVIBRATORS USED AS PULSE SHAPERS, ACTUATED BY LOW-TO-HIGH TRANSITIONS AT THE INPUT. WHEN THE INPUT CHANGES FROM LOW TO HIGH, THE OUTPUT GOES TO LOW FOR A PERIOD OF 180 TO 300 NANOSECONDS AND THEN RETURNS TO THE NORMAL HIGH.	THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE EXCURSIONS OF 0.0-VDC TO -0.5 VDC, AND -3.6 VDC TO -5.4 VDC. THE OUTPUT PULSES HAVE EXCURSIONS OF 0.0-VDC TO -0.3 VDC, AND -4.7 VDC TO -5.6 VDC.

LOGIC				POWER				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	LOW	HIGH	LOW	VOLT	G	15	-15	-4.5
0 V	-4.5 V	0 V	-4.5 V	mW	-	-	-	-

Figure 3-45. Amplifier Driver, Card Type 7003290.



LOGIC SYMBOL

LOGIC DESCRIPTION

THIS PRINTED-CIRCUIT MODULE HAS ONE BASIC CIRCUIT WITH SEVERAL APPLICATIONS. THIS CIRCUIT PRIMARILY FUNCTIONS AS A TIME DELAY OR SINGLE SHOT.

NOTE
INPUT PINS 12 AND 13 CAN BE INTERCHANGED.

A (DELAY). A HIGH INPUT WILL PRODUCE A DELAYED LOW OUTPUT. A LOW INPUT WILL PRODUCE A HIGH OUTPUT BUT NOT EFFECTIVELY DELAYED.

B (SINGLE SHOT). A HIGH INPUT WILL PRODUCE A HIGH OUTPUT, AND AFTER THE DELAY TIME, WILL BECOME LOW AGAIN.

C (SINGLE SHOT). SAME AS APPLICATION B EXCEPT THE HIGH OUTPUT CAN BE INHIBITED BY A HIGH INPUT ON PIN 5.

D (SINGLE SHOT). SAME AS APPLICATION B EXCEPT INPUT PIN 11 IS A RESISTOR-CAPACITOR NETWORK WHICH WILL ACCEPT ONLY A LOW-TO-HIGH TRANSITION, AND A HIGH INPUT ON PIN 5 WILL PRODUCE A LOW OUTPUT REGARDLESS OF THE STATE OF THE DELAY.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE EXCURSIONS OF 0.0-VDC TO -0.5 VDC, AND -3.6 VDC TO -5.4 VDC. THE OUTPUT PULSES HAVE EXCURSIONS OF 0.0-VDC TO -0.3 VDC, AND -4.7 VDC TO -5.6 VDC.

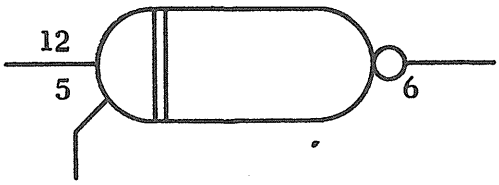
LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

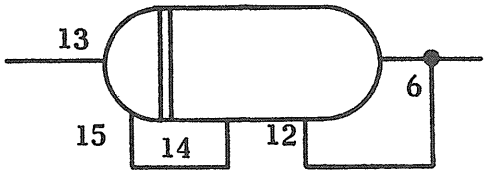
POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	217	317	45

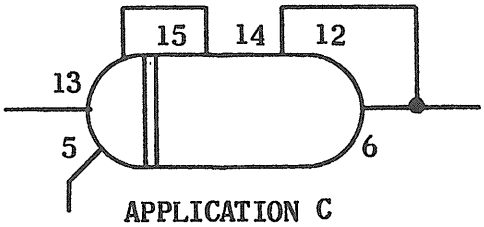
Figure 3-46. Time Delay, 1.2 to 16.5 msec, Card Type 7003480.



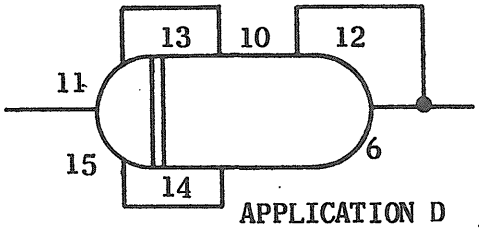
APPLICATION A



APPLICATION B



APPLICATION C



APPLICATION D

LOGIC SYMBOL

LOGIC DESCRIPTION

THIS PRINTED-CIRCUIT MODULE HAS ONE BASIC CIRCUIT WITH SEVERAL APPLICATIONS. THIS CIRCUIT PRIMARILY FUNCTIONS AS A TIME DELAY.

NOTE

INPUT PINS 12 AND 13 CAN BE INTERCHANGED.

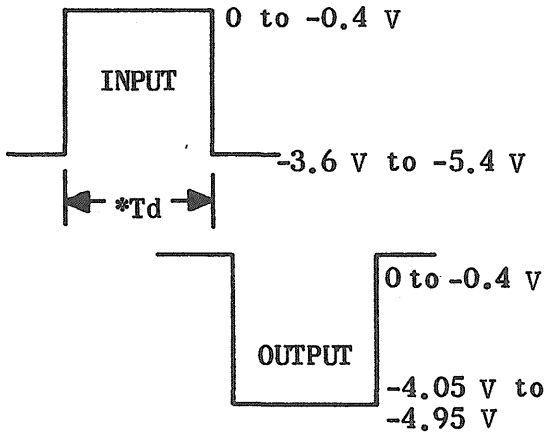
APPLICATION A. A HIGH INPUT WILL PRODUCE A DELAYED LOW OUTPUT. A LOW INPUT WILL PRODUCE A HIGH OUTPUT BUT NOT EFFECTIVELY DELAYED. A HIGH ON INPUT PIN 5 WILL PRODUCE A LOW OUTPUT REGARDLESS OF THE STATE OF THE DELAY.

APPLICATION B. A HIGH INPUT WILL PRODUCE A HIGH OUTPUT AND AFTER THE DELAY TIME WILL BECOME LOW AGAIN.

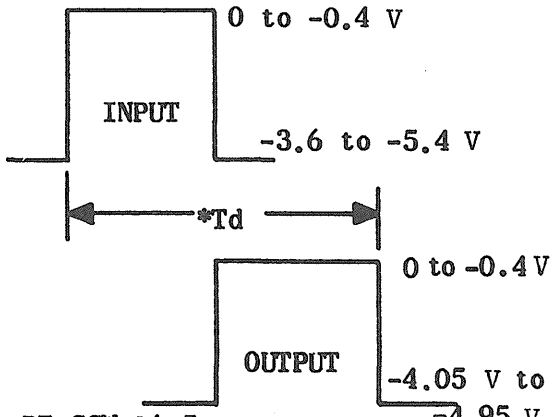
APPLICATION C. SAME AS APPLICATION B EXCEPT THE HIGH OUTPUT CAN BE INIHIBITED BY A HIGH INPUT ON PIN 5.

APPLICATION D. SAME AS APPLICATION B EXCEPT INPUT PIN 11 IS A RESISTOR-CAPACITOR NETWORK WHICH WILL ACCEPT ONLY A LOW-TO-HIGH TRANSITION.

APPLICATION A

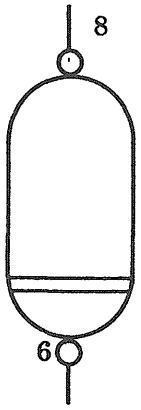


APPLICATIONS B, C, & D



*Td = R7 CCW 16.5 ms
R7 CW 1.2 ms

Figure 3-47. Time Delay, 1.5 to 15 msec, Card Type 7003580.



LOGIC SYMBOL

LOGIC DESCRIPTION

WHEN THIS CIRCUIT IS QUIESCENT, PINS 6 AND 8 ARE AT GROUND POTENTIAL (0.0-VDC).

WHEN A NEGATIVE VOLTAGE IS APPLIED TO PIN 6, PIN 8 GOES NEGATIVE FOR THE LENGTH OF THE DELAY. WHEN THE DELAY TIME EXPIRES, THE OUTPUT RETURNS TO GROUND POTENTIAL. THE DELAY TIME IS ADJUSTABLE FROM 35 TO 145 MILLI-SECONDS.

ELECTRICAL DESCRIPTION

THIS CIRCUIT OPERATES WITH INPUT PULSES THAT HAVE POSITIVE EXCURSIONS BETWEEN 0.0-VDC AND -0.4 VDC, AND NEGATIVE EXCURSIONS BETWEEN -3.8 VDC AND -5.2 VDC. THE EXCURSIONS OF THE OUTPUT VOLTAGE PULSES ARE THE SAME AS THOSE GIVEN FOR THE INPUT PULSES.

LOGIC

INPUT		OUTPUT	
HIGH	LOW	HIGH	LOW
0 V	-4.5 V	0 V	-4.5 V

POWER

PIN	1	2	3	4
VOLT	G	15	-15	-4.5
mW	-	-	-	-

Figure 3-48. Time Delay, Card Type 7105470.

Table 3-2. External Function Word Format

START READ	READ	KEYBOARD	INPUT CONTROL ENABLE	PUNCH	PRINT	OUTPUT CONTROL ENABLE	MEANING
2^6	2^5	2^4	2^3	2^2	2^1	2^0	
						0	Ignore bits 1 and 2; status of output devices remains unchanged.
						1	Enable output; perform function specified by bits 1 and 2.
				0	0		Disable printer and disable tape perforator.
				0	1		Enable printer and disable tape perforator.
				1	0		Enable tape, perforator and disable printer.
				1	1		Enable tape perforator and enable printer.
			0				Ignore bits 4, 5, and 6; status of input devices remains unchanged.
			1				Enable input; perform function specified by bits 4, 5, and 6.
0	0	0					Disable keyboard and disable paper tape reader.
0	0	1					Enable keyboard and disable paper tape reader.
0	1	0					Enable paper tape reader and disable keyboard.
0	1	1					Not used.
1	0	0					Not used.
1	0	1					Not used.
1	1	0					Enable paper tape reader, start read operation, and disable keyboard.
1	1	1					Not used.

is inverted by 36D00, and enables 40D00 to produce another EF REQ. The 70 msec high from 36D00 is routed to figure 5-6 on the low when EF REQ EN line, disabling the gate used for clearing START READ F/F OXD00 (5-6, 6C) when the tape head is up.

3-66. PRINTER OPERATION, GENERAL. For on-line printer operations, the computer sends an external function word of 003_8 (013_8 clears input functions) to the I/O Console (refer to figure 3-50 and referenced logic diagrams). When the I/O Console receives the EF word, the PRINT F/F is set, PRINT indicator lit, and power applied to the printer motor. After a half-second delay, the PRINTER READY F/F is set, the output register cleared, and an output data request (ODR) is sent to the computer. The sequence of events is described in the following steps.

a. The computer detects the ODR, places data from an assigned memory location on its output data lines (2^0 through 2^7) and transmits an output data acknowledge to the I/O Console.

b. Upon detecting the output data acknowledge from the computer, I/O Console control circuits gate the on-line ASCII coded data to the output register, drop the output data request (ODR), and initiate the serializer logic circuits. The serializer first sends a start pulse (space); serially gates the contents of the output register (bit by bit); and finally sends a stop pulse (mark) to the printer.

c. The printer then prints the character represented by the 7-bit ASCII code received from the I/O Console.

d. Control circuits in the I/O Console clear the output register and send another ODR to the computer. The action continues until the computer output buffer is empty or until the printer is deactivated by the computer program.

e. After data transmission is complete the program should deactivate the printer by sending an EF word of 001_8 (011_8 to master clear) to the I/O Console.

f. The printer operation can be stopped by depressing the PRINT CLEAR pushbutton, by depressing the MASTER CLEAR pushbutton or by the computer program.

3-67. PRINTER OPERATION, DETAILED. Refer to operational sequence flow diagram figure 3-50 and the referenced logic diagrams for the following discussion of printer operations. Steps 1 through 8 and 19 through 30 of the operational sequence flow diagram are applicable to printer operation.

3-68. External Function Acknowledge Enable. The EF acknowledge from the computer produces a 2µsec high from 19D01 (5-5, 4B). This high is inverted by 20D02 (5-5, 5C) to partially enable the set and clear sides of the PRINT F/F OXD01 (5-6, 7C).

3-69. External Function Word Conversion and Translation. For printer operation, an external function word of 003_8 (or 013_8) is received from the computer by the 20GXX gates (5-11 and 5-12). Active bits 2^0 and 2^1 are converted to I/O Console logic low levels (-4.5 VDC) by gates 20G00 (5-11, 3B) and 20G01 (5-11, 4B) and routed to figure 5-6 as the low when OUTPUT DEVICE and low when SET PRINT F/F signals respectively.

3-70. SET PRINT F/F and Start Printer Motor. On figure 5-6, the low when OUTPUT DEVICE signal further enables the set and clear sides of PRINT F/F OXD01 (5-6, 7C). The low when SET PRINT F/F fully enables the set side of PRINT F/F while disabling the clear side through inverter 30D01 (5-6, 7B). With PRINT F/F OXD01 set, the high from the clear side lights the PRINT indicator switch (DS24). This high is inverted to a low

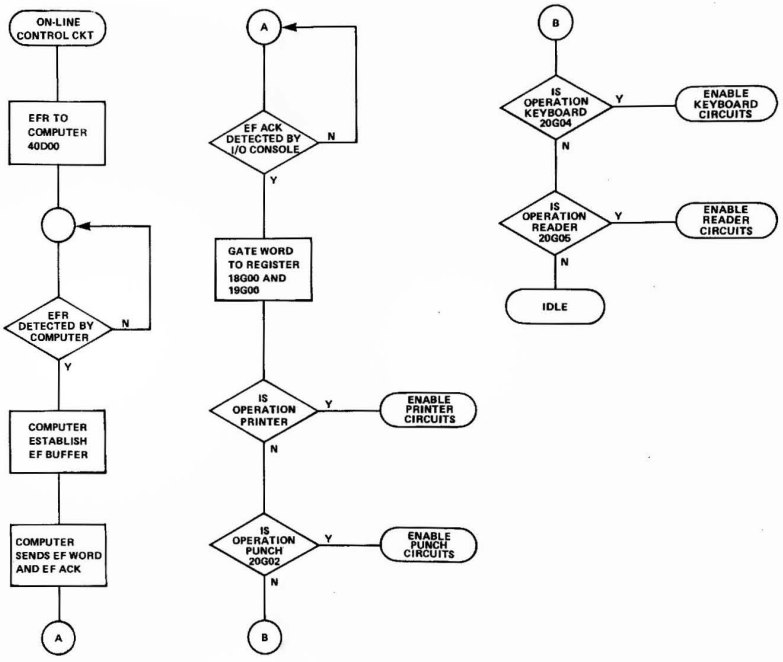


Figure 3-49. On-Line Control Circuits, Operational Flow Sequence Diagram.

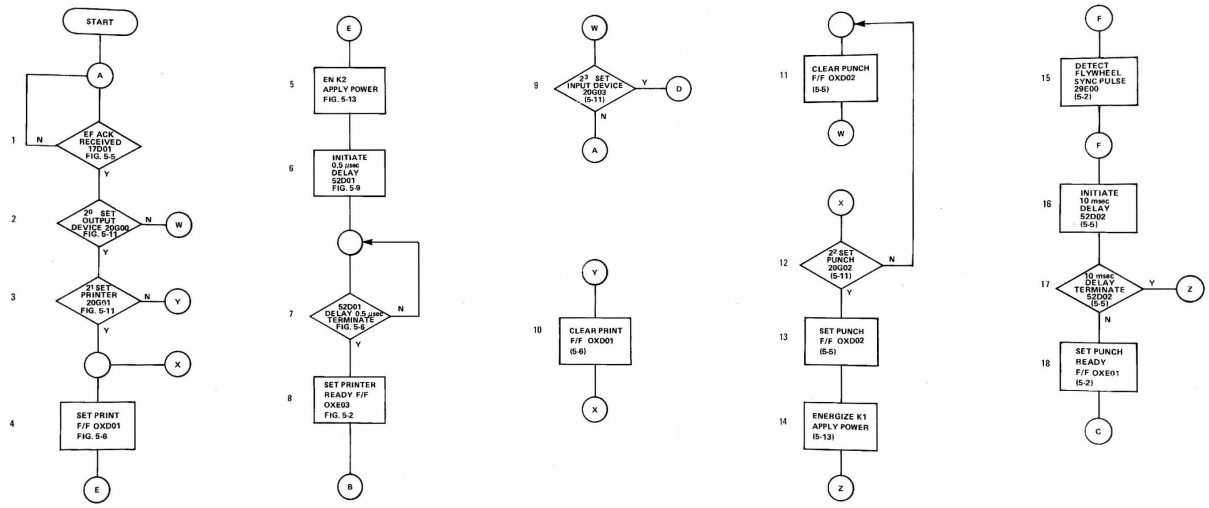


Figure 3-50. I/O Console Operational Sequence Flow Diagram (Sheet 1 of 4).

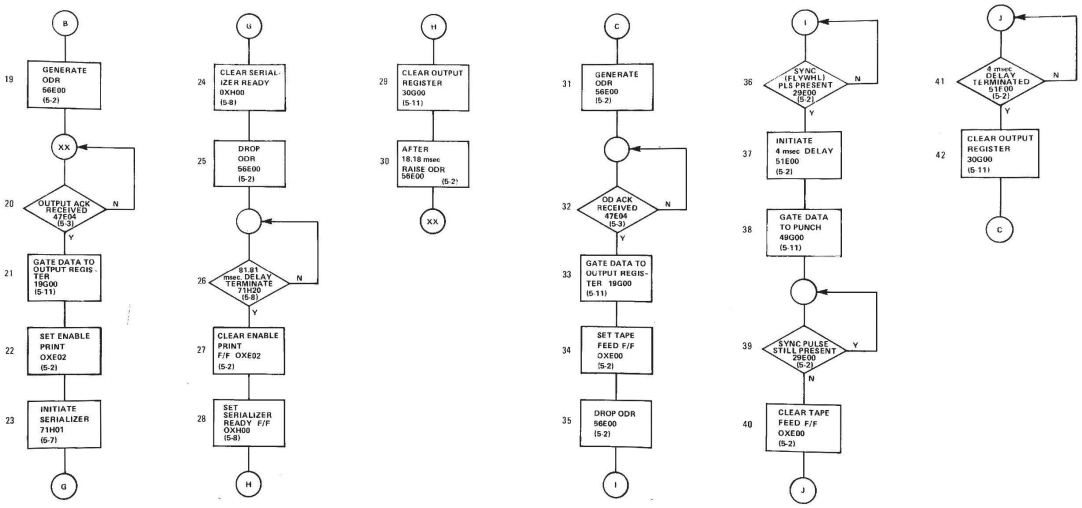


Figure 3-50. I/O Console Operational Sequence Flow Diagram (Sheet 2 of 4).

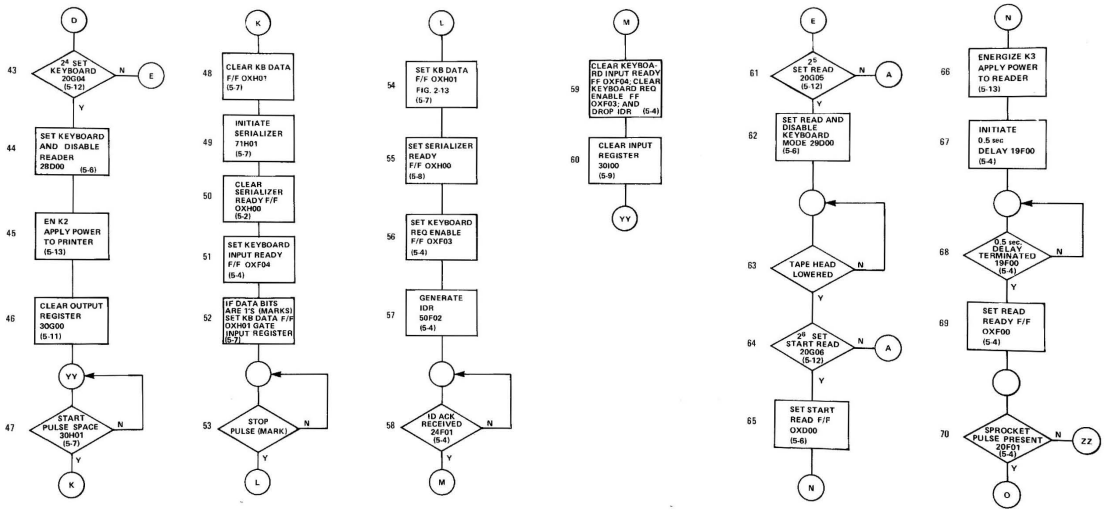


Figure 3-50. I/O Console Operational Sequence Flow Diagram (Sheet 3 of 4).

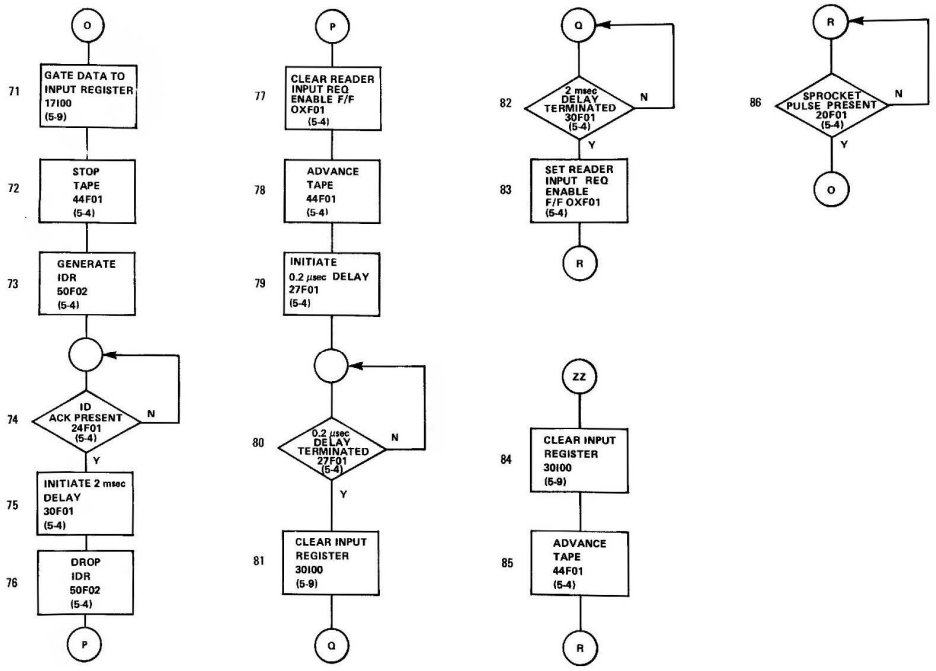


Figure 3-50. I/O Console Operational Sequence Flow Diagram (Sheet 4 of 4).

by 50D01 (5-6, 8B) to initiate the START PRINTER signal from 53D01 (5-6, 8C), which goes to energize PRINTER relay K2 (5-13, 4C). When K2 is energized, it completes a 115-VAC 60-Hz path to the keyboard/printer input A7P1-Z and starts the printer motor.

3-71. Set PRINTER READY F/F After 0.5 Second Delay. The low from the set side of PRINT F/F 0XD01 (5-6, 7C) is inverted to a high by 55D01 (5-6, 7D), removing the low when CLR PRINT RDY signal line from the clear side of PRINTER READY F/F 0XE03 (5-2, 6B). The low when EN SET PRINTER RDY from the set side of PRINT F/F 0XD01 (5-6, 7C) partially enables PRINTER READY F/F 0XE03 (5-2, 6B). The low from 50D01 (5-6, 8B), which occurs when PRINT F/F 0XD01 (5-6, 7C) is set, enables time delay 52D01 (5-6, 8C) which produces a high output after a 0.5 second delay. The 52D01 output is inverted by 54D01 (5-6, 8C) to produce a low when EN SET PRNTR RDY signal delayed 0.5 second from the initiation of the printer operation. This delayed signal is used as the final enable for setting PRINTER READY F/F 0XE03 (5-2, 6B).

3-72. Clear Output Register. Since TAPE FEED F/F 0XE00 (5-2, 4C) is clear at this time, the low from its clear side partially enables gate 53E00 (5-2, 6D). Time delay 51E00 (5-2, 3C) is normally outputting a low which further enables 53E00. Gate 53E00 is fully enabled by the low from inverter 52E02, which is present at all times except when ENABLE PRINT F/F 0XE02 is set during printer operations. Enabling 53E00 produces a high output which is inverted by 57E00 (5-2, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 is amplified by 30G00 (5-11, 8B) and used to clear output register flip-flops (5-11 and 5-12).

3-73. Generate Output Data Request. The high from 53E00 (5-2, 6D) partially enables gate 54E00 (5-2, 6C). With PUNCH F/F 0XD02 (5-5, 5D) clear, the low when CLR PUNCH READY signal from its clear side partially enables 50E02 (5-2, 6B). A second enable for 50E02 is the low when ENABLE signal from 37D00 (5-6, 4D) which is present at all times except during keyboard operations. Gate 50E02 is fully enabled by the low from the set side of PRINTER READY F/F 0XE03 (5-2, 6B). The high from 50E02 provides the final enable for 54E00 whose low output is used to partially enable OUTPUT REQ generator 56E00 (5-2, 7C). A low when EN REQ signal from 71H21 (5-8, 3C) is present at all times when the serializer is inactive. This signal is inverted by 71H22 (5-2, 7B), reinverted by OR gate 54E01 (5-2, 7C), and applied as a partial enable for 56E00 (5-2, 7C). The final enable for 56E00 is the low when EN REQ from the clear side of OFF-LINE F/F 0XD03 (5-5, 6D), which is present during all on-line operations. When 56E00 is enabled, it generates an OUTPUT REQ signal for transmittal to the computer. The output data request (ODR) is detected by the computer. The computer places ASCII-coded data from an assigned memory location on its output lines (2^0 through 2^7) and transmits an output data acknowledge (OD ACK) to the I/O Console.

3-74. Set ENABLE PRINT F/F, Remove ODR, and Gate Data to Output Register. The OD ACK from the computer is converted to a low console logic level (-4.5 VDC) by 47E04 (5-3, 3B) to enable gate 48E04 (5-3, 3C) since the low when $\overline{\text{COPY}}$ enabling signal is present during all on-line operations. The high from 48E04 is inverted to a low by 51E04 (5-3, 3C) to partially enable 53E04 (5-3, 3D). The low from 51E04 is also routed through 52E04 (5-3, 3C), which allows 53E04 to be fully enabled for 2µsec. The 53E04 output is a 2µsec low when GATE OUTPUT DATA signal which is used to partially enable setting ENABLE PRINT F/F 0XE02 (5-2, 5C). The set side of ENABLE PRINT F/F 0XE02 is fully enabled by the low from the set side of PRINTER READY F/F 0XE03 (5-2, 6B). With 0XE02 set, the low from its set side partially enables

50E06 (5-2, 5C). Gate 50E06 is fully enabled by the low on the high when KB signal line from 37D00 (5-6, 4C) which is present at all times except during keyboard operations. The high from 50E06, along with the high from the clear side of ENABLE PRINT F/F 0XE02, removes all low inputs to 51E02 causing it to produce a low output. The low is inverted by 52E02 (5-2, 6C) whose high output disables 53E00 (5-2, 6D). The low from 53E00 is inverted by 57E00 (5-2, 8C), removing the low when CLR OUTPUT REG signal from its output line. The low from 53E00 also disables 54E00 (5-2, 6C), preventing generation of an OUTPUT REQ signal. The 2µsec low when GATE OUTPUT DATA signal from 53E04 (5-3, 3D) is also used to fully enable 19G00 (5-11, 7B) since the low when $\overline{\text{COPY}}$ enabling signal is present during all on-line operations. The low from 19G00 gates the on-line data into the output register flip-flops 0XG00 through 0XG07 (5-11 and 5-12).

3-75. Enable Serializer. The high from 50E06 (5-2, 5C) is routed as the high when INIT SERIALIZER signal to figure 5-7 where it is inverted by three separate circuits: 71H00 (5-7, 8C), 72H00 (5-7, 5B) and 74H00 (5-7, 5B). The low from 71H00 partially enables 71H01 (5-7, 8C). The low from 72H00 partially enables individual AND gates for bits 0, 1, and 2, each of which provide inputs to OR gate 72H01 (5-7, 4B). This low also partially enables bit 3 AND gate 73H00 (5-7, 3B). The low from 74H00 is routed to figure 5-8, on the low when INIT SERIALIZER signal line where it partially enables individual AND gates for bits 5 and 6 and the parity bit, each of which provide inputs to OR gate 75H00 (5-8, 5C). The low when INIT SERIALIZER signal also partially enables bit 4 AND gate 74H01 (5-8, 7C). The clear side output from output register flip-flops 0XG00 through 0XG06 (figures 5-11 and 5-12) are routed to figures 5-7 and 5-8 to enable or disable their respective AND gates, depending upon the bit configuration of the stored ASCII code.

3-76. Initiate Serializer, Clear SERIALIZER READY F/F and Disable EFR. Gate 71H01 (5-7, 7C) is fully enabled by the low when SERIAL CONVERTER READY line. A low is present on this line at all times except when SERIALIZER READY F/F 0XH00 (5-8, 3C) is cleared. When 71H01 is enabled, its low output is delayed 2µsec by circuits 74H61 (5-7, 7C) and 74H62 (5-7, 7D) and routed to figure 5-8 to clear SERIALIZER READY F/F 0XH00 (5-8, 3C). With SERIALIZER READY F/F 0XH00 cleared, the high on the low when SERIAL CONVERTER READY output disables 71H01 (5-7, 7C). Gate 71H01 therefore produces a low output whenever it is enabled. This 2µsec negative pulse from 71H01 initiates the serializer action necessary for keyboard/printer operations. The high on the low when SERIALIZER CONVERTER READY line from the set side of SERIALIZER READY F/F 0XH00 (5-8, 3C) also goes to disable 40D00 (5-5, 3C), preventing generation of external function requests (EF REQ signals) while the serializer is in operation.

3-77. Basic Serializer Operations. Refer to figure 3-51 during the following discussion of serializer delay line operations. When 71H01 (5-7, 7C) is enabled, its 2µsec low output is stretched to 9.09 msec by 71H02 (5-7, 7D) and inverted by 71H03 (5-7, 7A). When the positive pulse from 71H03 terminates (goes negative), 71H04 (5-7, 7B) will produce a 9.09 msec output pulse which is delayed by 9.09 msec from the initiation of the serializer. In this manner, the 9.09 msec negative pulse travels down the delay line consisting of circuits 71H03 through 71H20. Each stage of the inverter-delay circuit delays the pulse an additional 9.09 msec.

NOTE

Each delay stage consists of an input inverter (2070 card) and a time delay (2821 card). The inverters have odd number designations and the time delays are designated by even numbers.

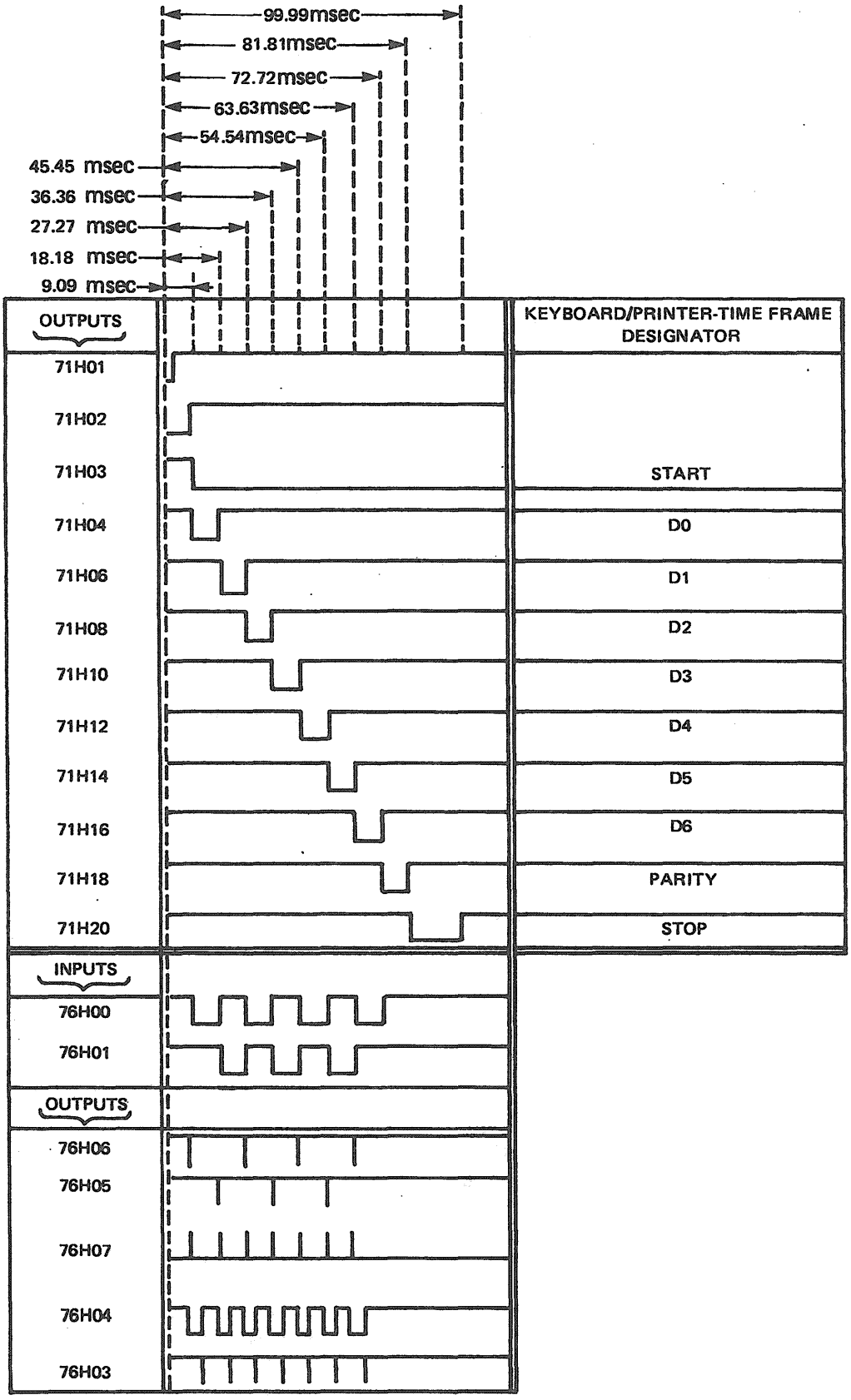


Figure 3-51. Serializer Timing Gates and Pulses.

3-78. Generation of Data to Printer Signals. In the normal state, gate 72H02 (5-7, 6C) is fully enabled since all inputs are low. Its high output is inverted to a low by 72H03 (5-7, 6C) causing a constant data to printer mark signal from 72H04 (5-7, 6C).

3-79. Start. When the serializer is initiated, the positive pulse from 71H03 (5-7, 7A) occurs during the first 9.09 msec, which is the time frame of the start pulse. Refer to figure 3-51 for an example of the pulse train configuration. This 9.09 msec high disables 72H02 (5-7, 6C) whose low output is inverted by 72H03 (5-7, 6C) to generate a DATA to PRINTER space signal from 72H04 (5-7, 6D) during the start pulse time frame.

3-80. Bit 0. The output of 71H04 (5-7, 7B) is a negative 9.09 msec pulse delayed 9.09 msec from the initiation of the serializer. This negative pulse enables bit 0 of the AND gate, which is fully enabled or disabled at this time, depending upon the state of output register F/F 0XG00 (5-11, 3C).

a. If F/F 0XG00 (5-11, 3C) is cleared (contains a space), the low on its clear side fully enables bit 0 AND gate of 72H01 (5-7, 4B) causing a high output from OR gate 72H01 (5-7, 4B). This high disables 72H02 (5-7, 6C), causing a DATA to PRINTER space signal from 72H04 (5-7, 6C) during D0 time frame (figure 3-51).

b. If F/F 0XG00 (5-11, 3C) is set (contains a mark), the high on its clear side will not enable bit 0 of the AND gate part of 72H01 (5-7, 4B), causing a low from the OR gate part of 72H01. This low keeps 72H02 (5-7, 6C) enabled, causing a DATA to PRINTER mark signal from 72H04 (5-7, 6C) during D0 time frame.

3-81. Bit 1. The output from 71H06 (5-7, 6B) is a negative 9.09 msec pulse delayed 18.18 msec from the initiation of the serializer. This negative pulse bit 1 AND gate is fully enabled or disabled during this time frame, depending upon the state of output register F/F 0XG01 (5-11, 4C). The remaining operations in the generation of a DATA to PRINTER space or mark for bit 1 are similar to those described in paragraph 3-80, steps a. and b., with the following exceptions.

a. Output register F/F 0XG01 (5-11, 4C) and bit 1 of the AND gate part of 72H01 (5-7, 4B) are referenced.

b. The DATA to PRINTER signal from 72H04 (5-7, 6C) occurs during D1 time frame (figure 3-51).

3-82. Bit 2. The output from 71H08 (5-7, 5B) is a negative 9.09 msec pulse delayed 27.27 msec from the initiation of the serializer. This negative pulse enables bit 2 AND gate, which is fully enabled or disabled during this time frame, depending upon the state of output register F/F 0XG02 (5-11, 6C). The remaining operations in generating a DATA to PRINTER space or mark for bit 2 are similar to those described in paragraph 3-80, steps a. and b., with the following exceptions.

a. Output register F/F 0XG02 (5-11, 6C) and bit 2 of the AND gate part of 72H01 (5-7, 4B) are referenced.

b. The DATA to PRINTER signal from 72H04 (5-7, 6C) occurs during D2 time frame (figure 3-51).

3-83. Bit 3. The output from 71H10 (5-7, 3B) is a negative 9.09 msec pulse delayed 36.36 msec from the initiation of the serializer. This negative pulse enables bit 3 AND gate 73H00 (5-7, 3B), which is fully enabled or disabled during this time frame, depending upon the state of bit 3 output register F/F 0XG03 (5-11, 7C).

a. If F/F OXG03 is cleared (contains a space), the low on its clear side fully enables bit 3 AND gate 73H00 (5-7, 3B) whose high output disables 72H02 (5-7, 6C), causing a DATA to PRINTER space signal from 72H04 (5-7, 6C) during D3 time frame.

b. If F/F OXG03 (5-11, 7C) is set (contains a mark), the high on its clear side disables bit 3 AND gate 73H00 (5-7, 3B) whose low outputs keep 72H02 enabled causing a DATA to PRINTER mark signal from 72H04 (5-7, 6C) during D3 time frame (figure 3-51).

3-84. Bit 4. The output from 72H12 (5-8, 8B) is a negative 9.09 msec pulse delayed 45.45 msec from initiation of the serializer. This negative pulse enables bit 4 AND gate 74H01 (5-8, 7C), which is fully enabled or disabled during this time frame, depending upon the state of bit 4 output register F/F OXG04 (5-12, 3C). The remaining operations in generating a DATA to PRINTER space or mark for bit 4 are similar to those described in paragraph 3-83, steps a. and b., with the following exceptions:

a. Output register F/F OXG04 (5-12, 3C) and bit 4 AND gate 74H01 (5-8, 7C) are referenced.

b. The DATA to PRINTER signal from 72H04 (5-7, 6C) occurs during D4 time frame (figure 3-51).

3-85. Bit 5. The output from 71H14 (5-8, 6B) is a 9.09 msec negative pulse delayed 54.54 msec from the initiation of the serializer. This negative pulse enables bit 5 AND gate, which is fully enabled or disabled during this time frame, depending upon the state of bit 5 output register F/F OXG05 (5-12, 4C).

a. If F/F OXG05 (5-12, 4C) is cleared (contains a space), the low on its clear side fully enables bit 5 of the AND gate part of 75H00 (5-8, 5C). This high disables 72H02 (5-7, 6C), causing a DATA to PRINTER space signal from 72H04 (5-7, 6C) during D5 time frame (figure 3-51).

b. If F/F OXG05 (5-12, 4C) is set (contains a mark), the high on its clear side disables bit 5 AND gate (5-8, 6C) causing a low from OR gate 75H00 (5-8, 5C). This low keeps 72H02 (5-7, 6C) enabled, causing a DATA to PRINTER mark signal from 72H04 (5-7, 6C) during D5 time frame.

3-86. Bit 6. The output from 71H16 (5-8, 5B) is a negative 9.09 msec pulse delayed 63.63 msec from the initiation of the serializer. This negative pulse enables bit 6 AND gate which is fully enabled or disabled during this time frame, depending upon the state of output register F/F OXG06 (5-12, 6C). The remaining operations in generating a DATA to PRINTER space or mark for bit 6 are similar to those described in paragraph 3-85, steps a. and b., with the following exceptions.

a. Output register F/F OXG06 (5-12, 6C) and bit 6 of the AND gate part of 75H00 (5-8, 5C) are referenced.

b. The DATA to PRINTER signal from 72H04 (5-7, 6C) occurs during D6 time frame (figure 3-51).

3-87. Parity Pulse. The output from 71H18 (5-8, 3B) is a negative 9.09 msec pulse delayed 72.72 msec from the initiation of the serializer. This negative pulse fully enables 75H00 (5-8, 5C) whose high output disables 72H02 (5-7, 6C), causing DATA to PRINTER space signal from 72H04 (5-7, 6C) during parity time frame (figure 3-51).

3-88. Stop Mark. The parity pulse is not used, however, when it terminates (81.81 msec after initiation of the serializer) gate 75H00 (5-8, 5C) is disabled. The low from 75H00 enables 72H02 (5-7, 6C) causing a DATA to PRINTER mark signal from 72H04 (5-7, 6C). This mark represents the stop signal for the character being received from the computer, and will remain on the DATA to PRINTER signal line until the next printer or keyboard operation is performed.

3-89. Set SERIALIZER RDY F/F and Clear ENABLE PRINT F/F. The output of 71H20 (5-8, 3C) is a negative 18.18 msec pulse delayed 81.81 msec from the initiation of the serializer (figure 3-51). This low sets SERIALIZER RDY F/F OXH00 (5-8, 3C) and clears ENABLE PRINT F/F OXE02 (5-2, 5C). The 18.18 msec low from 71H20 (5-8, 3B) is also inverted to a high by 71H21 (5-8, 3C) and routed on the low when EN REQ line to figure 5-2, where it is inverted by 71H22 (5-2, 7B) and reinverted by 54E01 (5-2, 7C) to disable 56E00 (5-2, 8C), preventing generation of an OUTPUT REQ signal during the 18.18 msec stop pulse time frames. With OXH00 (5-8, 3C), the low when SERIAL CONVERTER READY signal on its set side output partially enables 40D00 (5-5, 3C) permitting further EF REQ signals to be generated. The low when SERIAL CONVERTER READY signal from the set side of OXH00 also partially enables 71H01 (5-7, 8C) in preparation for receiving the next character transmission from the computer.

3-90. Clear Output Register. With ENABLE PRINT F/F OXE02 (5-2, 5C) cleared, the high from its set side disables 50E06 (5-2, 5C), since high when KB enable for this gate contains a low at all times except during keyboard operations. The low from 50E06 is inverted by 51E02 (5-2, 6B) and reinverted by 52E02 (5-2, 6B) to partially enable gate 53E00 (5-2, 6D). Since TAPE FEED F/F OXE00 (5-2, 4C) is clear, the low from its clear side further enables 53E00. Gate 53E00 is fully enabled by the low from time delay 51E00 (5-2, 3C), which is present at all times except during certain punch operations. The high from 53E00 is inverted by 57E00 (5-2, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 is amplified by 30G00 (5-11, 8B) and used to clear the output register flip-flops (5-11 and 5-12).

3-91. Generate ODR. The high from 53E00 (5-2, 6C) partially enables 54E00 (5-2, 6C). Gate 54E00 is fully enabled at this time by the high from 50E02 (5-2, 6B), which is present at all times during printer operations when PRINTER READY F/F OXE03 (5-2, 6B) is set. The low from 54E00 partially enables OUTPUT REQ generator 56E00 (5-2, 7C). At the end of the 18.18 msec stop pulse from time delay 71H20 (5-8, 3B), the low when EN REQ signal from inverter 71H21 returns to a low. This low when EN REQ signal is inverted by 71H22 (5-2, 7B) and reinverted by 54E01 (5-2, 7B) to further enable 56E00. OUTPUT REQ generator 56E00 is fully enabled at this time by the low when EN REQ which is present during all ON-LINE operations. With 56E00 enabled, an OUTPUT REQ is transmitted to the computer. The output data request is detected by the computer. The computer then places ASCII coded data from an assigned memory location on its output lines (2^0 through 2^7) and transmits an output data acknowledge to the I/O Console.

NOTE

The remaining printer operations are listed in the following paragraph.

3-92. Automatic Termination of ON-LINE Printer Operation. For automatic termination of printer operations after all data has been transmitted, the computer initiates an external function acknowledge and transmits an external function word of 001_8 to the I/O Console. When this EF ACK and EF word are received by the I/O Console, the following sequences occur:

a. The EF ACK generates a 2μsec positive pulse from 19D01 (5-5, 4B) which is inverted to a low by 20D01 (5-5, 5B) and stretched to a 70 msec negative pulse by 22D00 (5-5, 3B). The low from 22D00 is inverted by 36D00 (5-5, 3C),

disabling 40D00 (5-5, 3C) and preventing generation of another EF REQ signal for 70 msec after receiving an EF ACK.

b. The 2μsec high from 19D01 (5-5, 4B) is inverted by 20D02 (5-5, 5C) to partially enable the set side of PRINT F/F OXD01 (5-6, 7C). Bit 2^0 is converted to I/O low logic level (-4.5 VDC) by gate 20G00 (5-11, 3B) and routed to figure 5-6 as the low when OUTPUT DEVICE signal to further enable the clear and set sides of PRINT F/F OXD01. The absence of EF word bit 2^1 provides a high from 20G01 (5-11, 4B), which is routed on the low when SET PRINT F/F line to figure 5-6 where it disables the set side of PRINT F/F OXD01 and is inverted through 30D01 to fully enable the clear side.

c. With PRINT F/F OXD01 (5-6, 7C) cleared, the low from its clear side extinguishes PRINT indicator (DS 24) and is inverted to a high by 50D01 (5-6, 8B), which stops the printer motor by preventing the START PRINTER signal from 53D01 (5-6, 8C).

d. The high from the set side of PRINT F/F OXD01 (5-6, 7C) removes the low when EN SET PRNTR RDY enabling signal to PRINTER READY F/F OXE03 (5-2, 6B). The high from the set side of OXD01 is also inverted by 55D01 (5-6, 7C) to clear OXE03 (5-2, 6B).

e. With PRINTER READY F/F OXE03 (5-2, 6B) cleared, the high output from its set side disables OR gate 50E02 (5-2, 6B) and disables the set side of ENABLE PRINT F/F OXE02 (5-2, 5C). The low from 50E02 disables 54E00 (5-2, 6C) whose high output disables 56E00 (5-2, 7C), preventing further generation of OUTPUT REQ signals.

f. ENABLE PRINT F/F OXE02 (5-2, 5C) was cleared by the negative 18.18 msec low when CLR INIT SERIAL from 71H20 (5-8, 3C) when the last data word from the computer was printed. Since the high from PRINTER READY F/F OXE03 is now holding its set side disabled, OXE02 (5-2, 5C) will remain cleared until another printer operation is initiated.

g. With ENABLE PRINT F/F OXE02 (5-2, 5C) cleared, the low from its clear side is inverted by 51E02 (5-2, 6B), and re-inverted by 52E02 (5-2, 6C) to partially enable 53E00 (5-2, 6C). Gate 51E00 (5-2, 3C) is normally outputting a low (except during punch operations) which further enables 53E00 (5-2, 6C). Gate 53E00 (5-2, 6C) is fully enabled by the low from the clear side of TAPE FEED F/F OXE00 (5-2, 4C) (which is present at all times except during punch operations). With gate 53E00 (5-2, 6C) fully enabled, its high output is inverted by 57E00 (5-2, 8C), providing the low when CLEAR OUTPUT REG signal used to clear the output register (figures 5-11 and 5-12).

h. The high from the set side of ENABLE PRINTER F/F OXE02 (5-2, 5C) disables 50E06, removing its high when SERIALIZER signal output to figure 5-7. A low on the high when INIT SERIALIZER signal line is inverted by 71H00 (5-7, 8C) to disable 71H01 (5-7, 8C), preventing further initiation of the serializer. This low is also inverted by 72H00 (5-7, 5B) and 74H00 (5-7, 5B). The high from 72H00 (5-7, 5B) disables gates 72H01 (5-7, 8C) and 73H00 (5-7, 3B), causing them to produce low outputs. The high from 74H00 (5-7, 3B) is routed to figure 5-8 on the low when SERIALIZER signal line to disable 74H01 (5-8, 7B) and 75H00 (5-8, 5B), causing them to produce low outputs. The low from 74H01 (5-8, 7B) combines with the lows from 72H01 (5-7, 4C) and 73H00 (5-7, 3C) to partially enable 72H02 (5-7, 6C). The low from 75H00 (5-8, 5C) further enables 72H02 (5-7, 6C). A third enable for 72H02 (5-7, 6C) is provided by the low from 71H03 (5-7, 7A), which is present at all times when the serializer is inactive. The final enable for 72H02 (5-7, 6C) is the low from the set side of KEYBOARD DATA (F/F OXH01 (5-7, 8B), which is set at all times exept during

certain keyboard operations. With 72H02 (5-7, 6C) fully enabled, its high output is inverted by 72H03 (5-7, 6C) to disable 72H04 (5-7, 6D), producing a continual DATA-PRINTER mark signal until the next printer or keyboard operation is performed.

3-93. Manual Termination of ON-LINE Printer Operation. Various methods for manually stopping printer operations are available. These are discussed in the following paragraphs.

3-94. Depressing the PRINT CLEAR Pushbutton. On figure 5-6, when the PRINT CLEAR pushbutton (S10) is depressed, PRINT F/F OXD01 is cleared. The sequence of events occur as described in paragraph 3-92, steps c. through h..

3-95. Depressing the MASTER CLEAR Pushbutton. When the MASTER CLEAR pushbutton (S1, figure 5-3) is depressed, it produces a high when MASTER CLEAR which is routed to figures 5-2 and 5-5. The high from S1 (figure 5-3) is also inverted by 70E00 (5-3, 8B) and routed as low when MASTER CLEAR signals to figures 5-2, 5-6, and 5-8.

a. On figure 5-5, the high when MASTER CLEAR is inverted to a low by 20D01 (5-5, 5B). The low from 20D01 produces a 70 msec negative pulse from 22D00 (5-5, 3C) which is inverted by 36D00 (5-5, 3C). This 70 msec positive pulse from 36D00 (5-5, 3C) prevents an EF REQ from being generated by disabling 40D00 (5-5, 3C). However, at the end of 70 msec, 40D00 is again enabled and EF REQ signals may be generated.

b. On figure 5-6, the low when MASTER CLEAR clears PRINT F/F OXD01. The sequence of events occur as described in paragraph 3-92, steps c. through h..

c. On figure 5-2, the low when MASTER CLEAR ensures ENABLE PRINT F/F OXE02 (5-2, 5C) is cleared (in case MASTER CLEAR is initiated while the serializer is in operation).

3-96. KEYBOARD OPERATION, GENERAL. For on-line keyboard operation, the computer sends an external function word 030_8 (031_8 clears output functions) to the I/O Console. Then, at the operator's option, data or control information may be sent to the computer in one of two modes as described in the following paragraphs.

3-97. Mode 1, Keyboard Entry Via Interrupt. The operator selects the interrupt mode by depressing the INTERRUPT indicator-switch on the I/O Console control panel. Upon depressing a key, the code corresponding to that key is serially sent to the input register and to the printer. At this time, I/O Console control logic circuits generate an INTERRUPT signal to the computer. The computer detects the INTERRUPT and, consistent with its interrupt routine, stores the data on the input lines in an assigned memory location. After processing this data, the computer sends an input data acknowledge (ID ACK) to the I/O Console. Upon detecting the ID ACK, the I/O Console control circuits clear the INTERRUPT signal and the input register. To continue inputting to the computer via interrupts, the operator must manually depress the INTERRUPT indicator-switch prior to depressing a key for each character to be transmitted.

3-98. Mode 2, Keyboard Entry Via the Computer. When the keyboard operator depresses a key, the code corresponding to the selected character is sent serially to the input register and to the printer. At this time, control logic in the I/O Console generates an input data request (INPUT REQ) signal to the computer. Upon detecting the INPUT REQ, the computer stores the data on the input data lines in an assigned memory location. After processing this data, the computer sends an ID ACK to the I/O Console. When the I/O Console detects the ID ACK, control circuits clear the INPUT REQ signal and the input register. Each time an operator depresses a key, this action takes place and continues

until the program deactivates the keyboard mode by sending an external function word of 010_8 (or 011_8 master clears the I/O Console) to the I/O Console. The keyboard operation can be stopped by the computer, as described, or by the following methods:

a. Depressing the KEYBOARD CLEAR pushbutton.

b. Depressing the MASTER CLEAR pushbutton.

3-99. KEYBOARD OPERATION, DETAILED. Refer to operational flow diagram (figure 3-50) and referenced logic diagrams for the following discussion of keyboard operations. Steps 1, 2, 9, and 43 through 60 of the operational sequence flow diagram are applicable to keyboard operation.

3-100. External Function Acknowledge Enable. The EF ACK from the computer produces a 2µsec high from 19D01 (5-5, 4B). This high is inverted by 21D00 (5-6, 6B) to partially enable KEYBOARD gate 28D00 (5-6, 4B).

3-101. External Function Word Conversion and Translation. For keyboard operation, an external function word of 030_8 (or 031_8) is received from the computer by the 20GXX gates (figures 5-11 and 5-12). Active bits 2^3 and 2^4 are converted to I/O Console logic low levels (-4.5 VDC) by gates 20G03 (5-11, 7B) and 20G04 (5-12, 3B), respectively. The 20G04 output is routed directly to figure 5-6 as the low when EN KB signal, while the 20G03 (5-11, 7B) output is amplified by 21G03 (5-11, 6C) and routed to figure 5-6 as the low when INPUT DEVICE signal.

3-102. Light KEYBOARD and Start Printer Motor. On figure 5-6, the low when INPUT DEVICE and the low when EN KB signals fully enable KEYBOARD gate 28D00 (5-6, 4B) and light KEYBOARD indicator-switch (DS 23). KEYBOARD gate 28D00 (5-6, 4B) is held enabled and READ gate 29D00 (5-6, 5B) is held disabled by the interlocking action between the two gates. The high from 28D00 (5-6, 5B) is held disabled by the interlocking action between the two gates. The high from 28D00 (5-6, 4B) is inverted to a low by 33D00 (5-6, 4B). This low is inverted to a high by 34D00 (5-6, 4C), which is reinverted by 50D01 (5-6, 8B). The low from 50D01 (5-6, 8B) initiates the START PRINTER signal from 53D01 (5-6, 8C), which goes to energize PRINTER relay K2 (figure 5-13). When K2 is energized, it completes a 115-VAC 60-Hz path to keyboard/printer input A7P1-Z and starts the keyboard/printer motor.

3-103. Clear Output Register. The low from 33D00 (5-6, 4B) is inverted to a high by 37D00 (5-6, 4C) and routed to figure 5-2 as the high when KB signal to disable 50E06 (5-2, 5C) whose low output is inverted by 51E02 (5-6, 6B) and reinverted by 52E02 (5-6, 6C) to partially enable 53E00 (5-6, 6D). Gate 53E00 (5-6, 6D) is fully enabled by lows from 51E00 (5-2, 3C) and the clear side of TAPE FEED F/F 0XE00 (5-6, 4C), which are present at all times except during certain portions of punch operations. When 53E00 (5-6, 6D) is enabled, its high output is inverted by 57E00 (5-6, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 (5-11, 8B) is amplified by 30G00 (5-11, 8B) and used to clear the output register (figures 5-11 and 5-12).

3-104. Disable Output Data Request. Gate 50E01 (5-2, 7B) is disabled due to highs on the set side of PUNCH READY F/F 0XE01 (5-2, 4B) and low when OFF LINE signal line. Gate 50E02 (5-2, 6B) is disabled due to the high from the set side of PRINTER READY F/F 0XE03 (5-2, 6B). With 50E01 (5-2, 7B) and 50E02 (5-2, 6B) both disabled, their combined low outputs disable 54E00 (5-2, 6C), producing a high output to disable OUTPUT REQ generator 56E00 (5-2, 7C).

3-105. Keyboard Coding. When a key is depressed, a train of 11 pulses arrive serially from the keyboard. The train of pulses are referred to as spaces or marks. To further understand the composition of these pulse trains, refer to figure 3-52. The first pulse, or start pulse, is a space, which is followed by seven consecutive data pulses. These seven data pulses are a combination of spaces and marks, depending upon the ASCII code combination for the key depressed. Following these seven data pulses is a parity and two stop pulses. The parity pulse and stop pulses are always marking. Since each pulse is 9.09 msec in length, each complete character received from the keyboard has a coded length of 99.99 msec.

3-106. Clear KEYBOARD DATA F/F. The low when KB signal from 33D00 (5-6, 4B) partially enables gate 30H01 (5-7, 8B). When a key is depressed at the keyboard, the first pulse, or start pulse, is received by the I/O Console control circuits as a low when DATA, SPACE signal which fully enables 30H01 (5-7, 8B) to clear KEYBOARD DATA F/F 0XH01 (5-7, 8B).

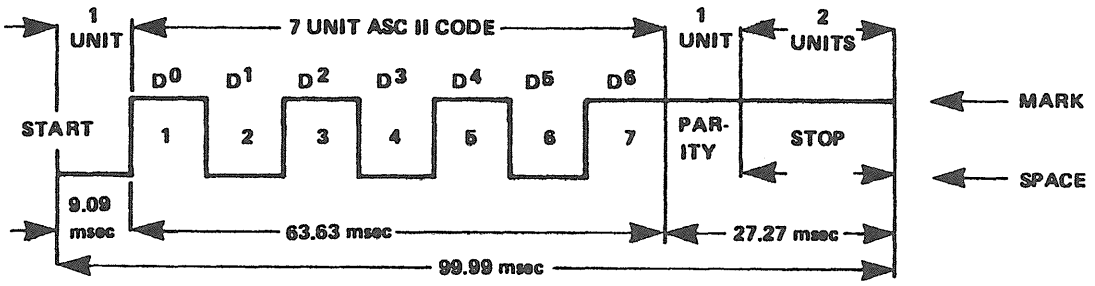
3-107. Enable Serializer. The high from KEYBOARD DATA F/F 0XH01 (5-7, 8B) is inverted by 71H00 (5-7, 8C) to partially enable 71H01 (5-7, 8C).

3-108. Initiate Serializer and Clear SERIALIZER READY F/F. Gate 71H01 (5-7, 8C) is fully enabled by the low when SERIAL CONVERTER READY line. A low is present on this line at all times except when SERIALIZER READY F/F 0XH00 (5-8, 3C), is cleared. When 71H01 (5-7, 8C) is enabled, its low output is delayed 2µsec by circuits 74H61 (5-7, 7C) and 74H62 (5-7, 7C) and routed to figure 5-8 to clear SERIALIZER RDY F/F 0XH00 (5-8, 3C). With SERIALIZER RDY F/F 0XH00 (5-8, 3C) cleared, the high on the low when SERIAL CONVERTER READY output disables 71H01 (5-7, 8C). Gate 71H01 (5-7, 8C) therefore produces a 2µsec low output whenever it is enabled. This 2µsec negative pulse from 71H01 (5-7, 8C) initiates the serializer action necessary for keyboard/printer operation.

3-109. Disable External Function Requests. The high on the low when SERIAL CONVERTER READY line from the set side of SERIALIZER RDY F/F 0XH00 (5-8, 3C) also goes to disable 40D00 (5-5, 3C), preventing the generation of external function requests (EF REQ signals) while the serializer is in operation.

3-110. Set KEYBOARD INPUT READY F/F. Gate 20F04 (5-4, 8C) is partially enabled by the low when EN GATE INPUT DATA signal from READ gate 29D00 (5-6, 5B). The high from KEYBOARD gate 28D00 (5-6, 4B) is inverted to a low by 18F04 (5-4, 8B). SERIALIZER RDY F/F 0XH00 (5-8, 3C) is cleared 2µsec after a key is depressed. The low when KB strobe from its clear side output is inverted by 20F03 (5-4, 7B) and reinverted to a low by 19F04 (5-4, 7B). When 18F04 (5-4, 8B) and 19F04 (5-4, 7B) are both producing lows, their combined outputs further enable 20F04 (5-4, 8C). Gate 20F04 (5-4, 8C) is fully enabled by the low from the clear side of KEYBOARD REQ ENABLE F/F 0XF03 (5-4, 7C) (which is cleared at this time). The low output from 20F04 (5-4, 8C) sets KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C) and is also routed to figure 5-8 and the low when GATE INPUT DATA signal where it is used to partially enable gate 70H00 (5-8, 4C). The high from the clear side of KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C) disables 50F04, removing the low when CLR INPUT REG signal output, thereby making it possible to set information into the input register flip-flops (figures 5-9 and 5-10).

3-111. Basic Serializer Operations. Refer to figure 3-51 during the following discussion of serializer delay line operations. When 71H01 (5-7, 7C) is enabled, its 2µsec low output is stretched to 9.09 msec by 71H02 (5-7, 8D) and inverted by 71H03 (5-7, 7A).



*CONFIGURATION VARIES DEPENDING ON CHARACTER BEING KEYED.

Figure 3-52. Example of Pulse Train Received from Keyboard when Key is Depressed.

When the positive pulse from 71H03 (5-7, 7A) terminates (goes negative), 71H04 (5-7, 7B) will produce a negative 9.09 msec output pulse which is delayed 9.09 msec from the initiation of the serializer. This pulse is inverted by 71H05 (5-7, 6B). When the positive pulse from 71H05 (5-7, 6B) terminates (goes negative), 71H06 (5-7, 6B) will produce a negative 9.09 msec output pulse delayed 18.18 msec from the initiation of the serializer. The 9.09 msec negative pulse travels down the delay line consisting of circuits 71H03 (5-7, 7A) through 71H20 (5-8, 3B). Each inverter-delay circuit stage delays the pulse an additional 9.09 msec.

NOTE

Each delay stage consists of an input inverter (2070 card) and a time delay (2821 card). The inverters have odd numbered designations and the time delays are designated by even numbers.

3-112. Generation of Keyboard Gating. As the 9.09 msec negative pulse travels down the delay line (figures 5-7 and 5-8), outputs from 71H04 (5-7, 7B), 71H06 (5-7, 6B), 71H08 (5-7, 5B), 71H10 (5-7, 3B), 71H12 (5-8, 8B) 71H14 (5-8, 7B), and 71H16 (5-8, 5B) are applied alternately to 76H00 (5-8, 4C) and 76H01 (5-8, 4C) whose high outputs produce 200 nanosecond negative pulse outputs from 76H06 (5-8, 4C) and 76H05 (5-8, 4C). [Alternating input to OR circuits 76H00 (5-8, 4C) and 76H01 (5-8, 4C) are necessary to prevent possible overlapping of adjacent pulses.] The negative pulses from 76H06 (5-8, 4C) and 76H05 (5-8, 4C) are inverted by OR circuits 76H07 (5-8, 4C). The output of 76H07 (5-8, 4C) is a series of seven positive pulses, approximately 200 nanoseconds in duration, whose leading edges are coincident with the leading edges of the 9.09 msec pulses from timing circuits 71H04 (5-7, 7B) through 71H16 (5-8, 5B). Timing circuit 76H02 (5-8, 4C) stretches each of the pulses to 4 msec positive pulses which are inverted by 76H04 (5-7, 7B) so that their trailing edges (positive-going) trigger 76H03 (5-8, 4C). The output of 76H03 (5-8, 4C) is a series of seven 200 nanosecond negative pulses, occurring in the approximate center of the 9.09 msec pulses from timing circuits 71H04 (5-7, 7B) through 71H16 (5-8, 5B). Pulses from 76H03 (5-8, 4C) are applied to AND circuit 70H00 (5-8, 4C) along with the low when GATE INPUT DATA signal from 20F04 (5-4, 8C). Therefore, gate 70H00 (5-8, 4C) is partially enabled for 200 nanoseconds during the approximate center of each ASCII-coded space or mark received from the keyboard. From figures 5-7 and 5-8, the delay line outputs from 71H04 (5-7, 7B) through 71H16 (5-8, 5B) (see figure 3-51) are also routed as partial enables to the set sides of input register flip-flops (5-9, 3C) 0XI00 through 0XI06 (5-10, 7C), respectively (figures 5-9 and 5-10).

3-113. Serial Transfer of ASCII Code to Input Register. A seven-unit ASCII code for the selected key follows the start pulse. Each unit is 9.09 msec wide and is either a space or a mark, depending upon the code for the character being transmitted (refer to table 3-3). Spaces from the keyboard are received on low when KB DATA, SPACE input to 30H01 (5-7, 8B) and gated to clear KEYBOARD DATA F/F OXH01 (5-7, 8B). Marks are received on the low when KB DATA, MARK line and used to set output of KEYBOARD DATA F/F OXH01 (5-7, 8B). The set output of KEYBOARD DATA F/F OXH01 (5-7, 8B) is routed to figure 5-8 on the low when KB DATA MARK signal line as the final enabling signal for gate 70H00 (5-8, 4C). When a space is received, a high on the low when KB DATA, MARK line disables 70H00 during the 9.09 msec duration of the space signal, removing the low when KB to INPUT REG output, thereby preventing the input register flip-flop, currently receiving the 9.09 msec negative enabling pulse from the delay line, from being set. Thus a binary 0 is stored in the input register flip-flop associated with this particular time frame. When a mark is received, the low when KB DATA, MARK signal fully enables 70H00 (5-8, 4C) during the 9.09 msec duration of the mark signal, producing a low when KB to INPUT REG signal to fully enable setting the input register flip-flop currently receiving the 9.09 msec negative enabling pulse from the delay line. Thus the input register flip-flop associated with this particular time frame is set, and a binary 1 is stored. In this manner, the ASCII code representing the key depressed is stored in the input register.

3-114. Set KEYBOARD DATA F/F. After the 7-bit ASCII code, a parity mark and two stop marks will be received from the keyboard (figure 3-52). Although the parity and stop marks are not gated to the input register, they assure that the KEYBOARD DATA F/F OXH01 (5-7, 8B) is in the set condition before receiving the next start pulse.

3-115. Set SERIALIZER READY F/F. The negative 9.09 msec pulse from 71H18 (5-8, 3B) is delayed 72.72 msec from the time the serializer was initiated (refer to figure 3-51). This represents the time frame when the parity mark is received from the keyboard. The pulse from 71H18 (5-8, 3B) is inverted by 71H19 (5-8, 3B). Its trailing edge causes delay 71H20 (5-8, 3B) to generate an 18.18 msec negative pulse, delayed 81.81 msec from the initiation of the serializer. This 18.18 msec pulse occurs while the two 9.09 msec stop marks are received from the keyboard. The 18.18 msec low from 71H20 (5-8, 3B) set SERIALIZER RDY F/F OXH00 (5-8, 3C) whose set output sends low when SERIAL CONVERTER READY signal to enable 71H01 (5-7, 7C) in preparation for receiving a start pulse from the keyboard when the next key is depressed.

3-116. Enable EF Request Generator. The low when SERIAL CONVERTER READY from the set side output of SERIALIZER RDY F/F OXH00 (5-8, 3C) is also used to remove the disable from EF REQ generator 40D00 (5-5, 3C).

3-117. Set KEYBOARD REQ ENABLE F/F. The high from the clear side of SERIALIZER RDY F/F OXH00 (5-8, 3C) is transmitted on the low when KB STROBE signal line to figure 5-4, where it is inverted by 20F03 (5-4, 7B) to enable setting KEYBOARD REQ ENABLE F/F OXF03 (5-4, 7C) [the other enable is provided by the low from the set side of KEYBOARD INPUT READY F/F OXF04 (5-4, 8C)]. With the OXF03 (5-4, 7C) set, its clear side output produces a high which disables 20F04 (5-4, 8C), preventing the low when GATE INPUT DATA signal to 70H00 (5-8, 4C). This disables 70H00 (5-8, 4C) and prevents further generation of low when KB to INPUT REG signals at this time.

3-118. Generate Input Data Request or Interrupt. The high from the clear side of KEYBOARD REQ ENABLE F/F OXF03 (5-4, 7C) also disables 50F03 (5-4, 7D). The low from 50F03 is delayed 4.4μsec by

Table 3-3. Keyboard Characters, Actions, and Data Codes

Key	Character or Action	Code						
		6	5	4	3	2	1	0

NOTE

Operating the CTRL key in conjunction with some other key generally does not cause a character to print, nor does any keyboard action take place, but a data word is transmitted (exceptions: CTRL and ALT MODE prints an = ; CTRL and RUB OUT prints a ?). The significance of the data words available through use of the CTRL key is determined by the computer program.

CTRL and @		0	0	0	0	0	0	0
CTRL and A		0	0	0	0	0	0	1
CTRL and B		0	0	0	0	0	1	0
CTRL and C		0	0	0	0	0	1	1
CTRL and EOT		0	0	0	0	1	0	0
CTRL and WRU		0	0	0	0	1	0	1
CTRL and RU		0	0	0	0	1	1	0
CTRL and BELL		0	0	0	0	1	1	1
CTRL and H		0	0	0	1	0	0	0
CTRL and I		0	0	0	1	0	0	1
LINE FEED	Line feed	0	0	0	1	0	1	0
CTRL and K		0	0	0	1	0	1	1
CTRL and L		0	0	0	1	1	0	0
RETURN	Carriage return	0	0	0	1	1	0	1
CTRL and N		0	0	0	1	1	1	0
CTRL and O		0	0	0	1	1	1	1
CTRL and P		0	0	1	0	0	0	0
CTRL and Q		0	0	1	0	0	0	1

Table 3-3. Keyboard Characters, Actions, and Data Codes (Contd)

Key	Character or Action	Code						
		6	5	4	3	2	1	0
CTRL and TAPE		0	0	1	0	0	1	0
CTRL and XOFF		0	0	1	0	0	1	1
CTRL and $\overline{\text{TAPE}}$		0	0	1	0	1	0	0
CTRL and U		0	0	1	0	1	0	1
CTRL and V		0	0	1	0	1	1	0
CTRL and W		0	0	1	0	1	1	1
CTRL and X		0	0	1	1	0	0	0
CTRL and Y		0	0	1	1	0	0	1
CTRL and Z		0	0	1	1	0	1	0
CTRL, SHIFT, and K		0	0	1	1	0	1	1
CTRL, SHIFT, and L		0	0	1	1	1	0	0
CTRL, SHIFT, and M		0	0	1	1	1	0	1
CTRL, SHIFT, and ↑		0	0	1	1	1	1	0
CTRL, SHIFT, and ←		0	0	1	1	1	1	1
Space Bar	Space	0	1	0	0	0	0	0
SHIFT and !	!	0	1	0	0	0	0	1
SHIFT and "	"	0	1	0	0	0	1	0
SHIFT and #	#	0	1	0	0	0	1	1
SHIFT and $	$	0	1	0	0	1	0	0
SHIFT and %	%	0	1	0	0	1	0	1
SHIFT and &	&	0	1	0	0	1	1	0
SHIFT and '	'	0	1	0	0	1	1	1
SHIFT and (	(	0	1	0	1	0	0	0

Table 3-3. Keyboard Characters, Actions, and Data Codes (Contd)

Key	Character or Action	Code						
		6	5	4	3	2	1	0
SHIFT and)	)	0	1	0	1	0	0	1
SHIFT and *	*	0	1	0	1	0	1	0
SHIFT and +	+	0	1	0	1	0	1	1
LOC LF	Continuous line feed, no code transmitted.							
LOC CR	Carriage return, no code transmitted.							
REPT	Used in conjunction with another coded key, selected character repeats continuously until REPT key is released.							
'	'	0	1	0	1	1	0	0
-	-	0	1	0	1	1	0	1
.	.	0	1	0	1	1	1	0
/	/	0	1	0	1	1	1	1
0	0	0	1	1	0	0	0	0
1	1	0	1	1	0	0	0	1
2	2	0	1	1	0	0	1	0
3	3	0	1	1	0	0	1	1
4	4	0	1	1	0	1	0	0
5	5	0	1	1	0	1	0	1
6	6	0	1	1	0	1	1	0
7	7	0	1	1	0	1	1	1
8	8	0	1	1	1	0	0	0
9	9	0	1	1	1	0	0	1

Table 3-3. Keyboard Characters, Actions, and Data Codes (Contd)

Key	Character or Action	Code						
		6	5	4	3	2	1	0
:	:	0	1	1	1	0	1	0
;	;	0	1	1	1	0	1	1
SHIFT and <	<	0	1	1	1	1	0	0
SHIFT and =	=	0	1	1	1	1	0	1
SHIFT and >	>	0	1	1	1	1	1	0
SHIFT and ?	?	0	1	1	1	1	1	1
SHIFT and @	@	1	0	0	0	0	0	0
A	A	1	0	0	0	0	0	1
B	B	1	0	0	0	0	1	0
C	C	1	0	0	0	0	1	1
D	D	1	0	0	0	1	0	0
E	E	1	0	0	0	1	0	1
F	F	1	0	0	0	1	1	0
G	G	1	0	0	0	1	1	1
H	H	1	0	0	1	0	0	0
I	I	1	0	0	1	0	0	1
J	J	1	0	0	1	0	1	0
K	K	1	0	0	1	0	1	1
L	L	1	0	0	1	1	0	0
M	M	1	0	0	1	1	0	1
N	N	1	0	0	1	1	1	0
O	O	1	0	0	1	1	1	1
P	P	1	0	1	0	0	0	0

Table 3-3. Keyboard Characters, Actions, and Data Codes (Contd)

Key	Character or Action	Code						
		6	5	4	3	2	1	0
Q	Q	1	0	1	0	0	0	1
R	R	1	0	1	0	0	1	0
S	S	1	0	1	0	0	1	1
T	T	1	0	1	0	1	0	0
U	U	1	0	1	0	1	0	1
V	V	1	0	1	0	1	1	0
W	W	1	0	1	0	1	1	1
X	X	1	0	1	1	0	0	0
Y	Y	1	0	1	1	0	0	1
Z	Z	1	0	1	1	0	1	0
SHIFT and K	[	1	0	1	1	0	1	1
SHIFT and L		1	0	1	1	1	0	0
SHIFT and M	]	1	0	1	1	1	0	1
SHIFT and ↑	↑	1	0	1	1	1	1	0
SHIFT and ←	←	1	0	1	1	1	1	1
ALT MODE		1	1	1	1	1	0	1
CTRL and ALT MODE	=	1	1	1	1	1	1	0
RUB OUT		1	1	1	1	1	1	1
CTRL and RUB OUT	?	1	1	1	1	1	1	1

51F03 (5-4, 6D) and delay gate 52F03 (5-4, 6D), which partially enables 51F02 (5-4, 6C) and 50F02 (5-4, 5C). Since READ gate 29D00 (5-6, 5B) is outputting a low during keyboard operations, its output is inverted by 31D00 and sent as the high when EN REQ signal to disable 44F02 (5-4, 6B). The low from 44F02 fully enables 45F02 (5-4, 6B), whose high output disables 46F02 (5-4, 6C). The low from 46F02 further enables 51F02 (5-4, 6C) and 50F02 (5-4, 5C).

3-119. In the computer mode of operation, the high from the set side of INTERRUPT F/F OXF02 (5-4, 6C) disables 51F02 (5-4, 6C). The low from the clear side fully enables driver 50F02 (5-4, 5C) to generate an INPUT REQ signal for transmittal to the computer. If the operator has selected the interrupt mode of operation (by depressing the INTERRUPT indicator switch on the I/O Console), INTERRUPT F/F OXF02 (5-4, 6C) will be set, and the high from the set side will disable 50F02 (5-4, 5C) and prevent the INPUT REQ signal, while the low from the set side will fully enable 51F02 (5-4, 6C) to generate an INTERRUPT signal for transmittal to the computer. When the computer receives either the input data request or interrupt, it stores the data on its input lines in a specific memory location. After processing the data, the computer transmits an input data acknowledge to the I/O Console. The generated IDR or interrupt is delayed 4.4µsec after setting of OXF03 (5-4, 7C) and will remain until receipt of an INPUT ACK.

3-120. Clear KEYBOARD INPUT READY F/F, KEYBOARD REQ ENABLE F/F, and INTERRUPT F/F. The INPUT ACK from the computer is converted to a low I/O logic level (-4.5 VDC) by 24F01 (5-4, 6B), which enables gate 25F01 (5-4, 5C). The high from 25F01 (5-4, 5C) is inverted by 26F01 (5-4, 5A) and used as a partial enable for 28F01 (5-4, 5B). The low from 26F01 (5-4, 5A) is routed through 27F01 (5-4, 5B), which allows 28F01 (5-4, 5B) to be fully enabled for 2µsec. The 28F01 (5-4, 5B) output is a 2µsec positive pulse whose leading edge is coincident with the INPUT ACK. This positive pulse is inverted by 29F01 (5-4, 5C) and used to clear KEYBOARD INPUT READY F/F OXF04 (5-4, 8C), KEYBOARD REQ ENABLE F/F OXF03 (5-7, 7C), and INTERRUPT F/F OXF02 (5-4, 6C).

3-121. Drop Input Data Request or Interrupt. When not in a read operation, gate 50F00 (5-4, 3D) outputs a low which partially enables 50F03 (5-4, 7D). With KEYBOARD REQ ENABLE F/F OXF03 (5-4, 7C) cleared, the low from its clear side fully enables 50F03 (5-4, 7D), which produces a high to disable 51F03 (5-4, 6D) and prevent one of the enabling signals for both 50F02 (5-4, 5C) and 51F02 (5-4, 6C). Observe, however, that a 4.4µsec delay 50F03 (5-4, 7D) is not effective with low inputs. With 50F02 (5-4, 5C) and 51F02 (5-4, 6C) disabled, either the INPUT REQ signal or the INTERRUPT signal is removed, depending on the mode of operation being utilized by the keyboard operator.

NOTE

The keyboard normally operates in the computer mode, communicating with the computer via INPUT REQ signals from 50F02 (5-4, 5C). To operate in the interrupt mode, the operator must depress the INTERRUPT indicator switch prior to depressing a key for each character of the transmitted message.

3-122. Clear Input Register. The low from the clear side of KEYBOARD INPUT READY F/F OXF04 (5-4, 8C) partially enables 50F04 (5-4, 7D). The low from 50F00 (5-4, 3D), which is present at all times except during reader operations, further enables 50F04 (5-4, 7D). The 2µsec positive pulse from 28F01 (5-4, 5B) is applied to the 50F04 (5-4, 7D)

input. At the end of the pulse, this signal becomes negative and provides the final enable for 5OF04 (5-4, 7D), which now provides a low when CLR INPUT REG signal to clear the input register (figures 5-9 and 5-10).

NOTE

The remaining keyboard operations are described in paragraph 3-128.

3-123. Clear Output Register. The low from the clear side of KEYBOARD INPUT READY F/F OXF04 (5-4, 8C) partially enables 5OF04 (5-5, 7D). The low from 5OF00 (5-4, 3D), which is present at all times except during reader operations, further enables 5OF04 (5-4, 7D). The 2µsec positive pulse from 28F01 (5-4, 5B) is applied to the 5OF04 (5-4, 7D) input. At the end of the pulse, this signal becomes negative and provides the final enable for 5OF04 (5-4, 7D), which now provides a low when CLR INPUT REG signal to clear the output register (figures 5-9 and 5-10).

3-124. Serial Data Transmission to Printer During Keyboard Operation. The high when KB signal from 37D00 (5-6, 4C) disables 5OE06 (5-2, 5C) during keyboard operations. The low from 5OE06 (5-2, 5C) is routed to figure 5-7 on high when INIT SERIALIZER signal line, where it is inverted to highs by 72H00 (5-7, 5B) and 74H00 (5-7, 5B). The high from 72H00 disables gates 72H01 (5-7, 3B) and 53H00 (5-7, 3B), causing them to produce low ouputs. The high from 74H00 (5-7, 5B) is routed to figure 5-8 on the low when INIT SERIALIZER signal line, where it disables gates 74H01 (5-8, 7C) and 75H00 (5-8, 5C). The low from 74H01 (5-8, 7C) goes back to figure 5-7, where it is combined with the lows from 72H01 (5-7, 4B) and 73H00 (5-7, 3B) provides one of the enables for 72H02 (5-7, 6B). The low from 75H00 (5-8, 5B) is used as a second enable for 72H02 (5-7, 6C). The positive gate from 71H03 (see figure 3-51) occurs during the 9.09 msec time frame when the start pulse (space) is being received from the keyboard. At all other times, the 71H03 (5-7, 7A) output is low, providing a third enable for 72H02 (5-7, 6C).

3-125. The final enable for 72H02 (5-7, 6C) comes directly from the set side of KEYBOARD DATA F/F OXH01 (5-7, 8B), which is cleared when a space is received from the keyboard and set when a mark is received. Therefore a space is represented by a high on the set side of OXH01, and a mark is represented by a low. In this manner, the output of OXH01 (5-7, 8B) reflects the pulse train of spaces and marks received from the keyboard when a key is depressed. A high from the set side of OXH01 (5-7, 8B) (space) disables gate 72H02 (5-7, 6B), whose low output is inverted by 72H03 (5-7, 6C) to generate a DATA to PRINTER space signal from 72H04 (5-7, 6C). A low from the set side of OXH01 (5-7, 8B) (mark) fully enables gate 72H02 (5-7, 6C), whose high output is inverted by 72H03 (5-7, 6C) to generate a DATA-PRINTER mark signal from 72H04 (5-7, 6C).

NOTE

The positive pulse from 71H03 (5-7, 7A) described above, generates a space pulse while preventing generation of a mark pulse during the first 9.09 msec (start pulse) duration of each character transmitted.

3-126. Data to Printer Signal Generation. Circuit 72H04 (5-7, 6C) is a bias network which produces a DATA to PRINTER output signal that is slightly positive when its input is positive and slightly negative when its input is negative. A positive output causes the printer to generate a space, while a negative output causes a mark to be generated. The DATA to PRINTER signal is routed to power supply input A6P1-X (5-13, 3B) as bias for PNP power transistor Q10. When

a positive signal is present, Q10 is cut off, and an open circuit is present at A6P2-W. When a negative signal is present, Q10 is allowed to conduct, and a ground circuit is present. The A6P2-W output is routed to A7P1-X on the keyboard/printer, through the selector magnet coils and back through A7P1-W to the -28 VDC line at power supply terminal A6P2-X. When current is allowed to flow through the selector magnet circuits in the keyboard/printer, a mark is generated. When no current flows, a space is generated.

3-127. Automatic Termination of On-Line Keyboard Operation. For automatic termination of the keyboard mode after data transmission is complete, the computer places an external function word of 010_8 on its output lines and transmits an external function acknowledge to the I/O Console. When the EF ACK and EF word are received by the I/O Console, the following sequences occur:

a. The EF ACK generates a 2µsec positive pulse from 19D01 (5-5, 4B) which is inverted to a low by 20D01 (5-5, 5B) and stretched to a 70 msec negative gate by 22D00 (5-5, 3B). The low from 22D00 (5-5, 3B) is inverted by 36D00 (5-5, 3C), disabling 40D00 (5-5, 3C) and preventing generation of another EF REQ signal for 70 msec after receiving an EF ACK.

b. The 2µsec positive pulse from 19D01 (5-5, 4B) is inverted by 21D00 (5-6, 6B) to partially enable 27D00 (5-6, 3D).

c. Bit 2^3 of the EF word provides a low from 20G03 (5-11, 7B) which is amplified by 21G03 (5-11, 6C) and routed as the low when INPUT DEVICE signal to figure 5-6, where it is used to partially enable AND gate 25D00 (5-6, 3C).

d. The absence of EF word bit 2^4 provides a high from 20G04 (5-12, 3B), which is routed to figure 5-6 on the low when EN KB signal line to disable gate 28D00 (5-6, 4B) and enable 24D00 (5-6, 3B).

e. With 24D00 (5-6, 3B) enabled, its low output fully enables 25D00 (5-6, 3C), producing a high which is inverted by 26D00 (5-6, 3C) to enable 27D00 (5-6, 3D). The high from 27D00 (5-6, 3D) prevents interlocking sides of KEYBOARD gate 28D00 (5-6, 4B) and READ gate 29D00 (5-6, 5B) from being enabled.

f. The low from 28D00 (5-6, 4B) extinguishes KEYBOARD indicator (DS 23); removes the KEYBOARD disable from READ gate 29D00 (5-6, 5B); and is inverted to a high by 33D00 (5-6, 4B), whose output is reinverted to a low by 34D00 (5-6, 4C). The low from 34D00 (5-6, 4C) is inverted to a high by 50D01 (5-6, 8B), which stops the printer motor by preventing the START PRINTER signal from 53D01 (5-6, 8C).

g. The low when CLR from 28D00 (5-6, 4B) is routed to figure 5-4, where it is inverted by 29F04 (5-4, 8B) and 18F04 (5-4, 7B). The high from 18F04 (5-4, 7B) disables 20F04 (5-4, 7C), whose high output removes the set signal from KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C), and disables gate 70H00 (5-8, 4C). Disabling gate 70H00 (5-8, 4C) prevents data from being transferred from the keyboard to the input register by preventing the low when KB to INPUT REG signal to the input register (figures 5-9 and 5-10).

h. The high from 29F04 (5-4, 8B) is inverted by 30F04 (5-4, 8C) and used to clear KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C) and INTERRUPT F/F 0XF02 (5-4, 6C). With 0XF04 (5-4, 8C) cleared, the high from its set side disables the set side of KEYBOARD REQ ENABLE F/F 0XF03 (5-4, 7C), preventing it from being set and allowing it to be cleared by the low from 30F04 (5-4, 8C).

i. A low from 50F00 (5-4, 3D) (present at all times except during reader operations) partially enables 50F03 (5-4, 7D) and 50F04 (5-4, 7D). The absence of ID ACK from the computer produces a low from 28F01 (5-4, 5B) which further enables 50F04 (5-4, 7D). The

low from the clear side of KEYBOARD INPUT READY F/F OXF04 (5-4, 8C) fully enables 50F04 (5-4, 7D), producing a low when CLR INPUT REG signal to clear the input register flip-flops, OXI00 through OXI07, (figures 5-9 and 5-10). The low from the clear side of KEYBOARD REQ ENABLE F/F OXF03 (5-4, 7C) fully enables 50F03 (5-4, 7D), thus disabling 51F03 (5-4, 6D) and preventing further INPUT REQ signals from 50F02 (5-4, 5C) or INTERRUPT signals from 51F02 (5-4, 6C).

j. The high from 33D00 (5-6, 4B) is routed to figure 5-7 on the low when signal line, where it is used to disable AND gate 30H01 (5-7, 8B), preventing the clearing of KEYBOARD DATA F/F OXH01 (5-7, 8B). The OXH01 (5-7, 8B) was placed in a set condition by stop pulses in the last character received from the keyboard. The low from its set side output will hold gate 72H02 (5-7, 6C) enabled, since all other inputs to 72H02 (5-7, 6C) are low at this time. The high output from 72H02 (5-7, 6C) is inverted by 72H03 (5-7, 6C) to disable 72H04 (5-7, 6C), producing a continual DATA-PRINTER mark signal to the printer until the next printer or keyboard operation is performed.

3-128. Manual Termination of On-Line Keyboard Operation. Various methods for manually stopping the keyboard are discussed in the following paragraphs.

3-129. Depressing the KEYBOARD CLEAR Pushbutton. When the KEYBOARD CLEAR pushbutton switch (S9, 5-6, 3D) is depressed, the interlocking sides of KEYBOARD gate 28D00 (5-6, 4B) and READ gate 29D00 (5-6, 5B) are disabled and the following sequences occur.

a. Refer to paragraph 3-127, steps f. through j..

3-130. Depressing the MASTER CLEAR Pushbutton. When the MASTER CLEAR pushbutton switch (S1, figure 5-3) is depressed, it produces a high when MASTER CLEAR which is routed to figure 5-5. The high from S1 is also inverted by 70E00 (5-3, 8B) and 70E01 (5-3, 8B) and routed as a low when MASTER CLEAR signal to figures 5-4, 5-6, and 5-8. The following sequences then occur:

a. On figure 5-5, the high when MASTER CLEAR is inverted to a low by 20D01 (5-5, 5B). The low from 20D01 (5-5, 5B) produces a 70 msec negative pulse from 22D00 (5-5, 3C) which is inverted by 36D00 (5-5, 3C). This 70 msec positive pulse from 36D00 (5-5, 3C) prevents an EF REQ from being generated by disabling 40D00 (5-5, 3C). However, at the end of 70 msec, 40D00 (5-5, 3C) is again enabled and EF REQ signals may be generated.

b. On figure 5-4, the low when MASTER CLEAR is inverted by OR gate 29F04 (5-4, 8B), and the series of events described in paragraph 3-127, steps f. and g., are performed.

c. On figure 5-6, the low when MASTER CLEAR is inverted to a high by 71D01 (5-6, 2D). This produces the same effect as depressing the KEYBOARD CLEAR pushbutton (S9).

d. On figure 5-8, the low when MASTER CLEAR is inverted by 77H00 (5-8, 3C), placing a high on the clear side output of SERIALIZER READY F/F OXH00 (5-8, 3C). This high sets OXH00 (5-8, 3C), whose set output is routed as a low when SERIAL CONVERTER READY signals to figures 5-5 and 5-7.

e. On figure 5-5, the low when SERIAL CONVERTER READY signal partially enables 40D00 (5-5, 3C), permitting further EF REQ signals to be generated.

f. On figure 5-7, the low when SERIAL CONVERTER READY signal partially enables 71H01 (5-7, 7C), permitting the serializer to be initiated when the next keyboard or printer operation occurs.

3-131. TAPE READER OPERATION, GENERAL. For on-line reader operation, the computer sends an external function word of

150_8 (or 151_8) to the I/O Console. With the tape correctly positioned in the reader and the tape head switch lowered I/O Console control circuits set the READ and START READ indicators and apply power to the reader motor. After a half second, the READ READY F/F is set and tape movement is initiated until the photo sensors detect a sprocket hole and associated data holes for that frame. A sprocket pulse is generated, and used to stop the tape with the current frame over the photodiode head and to gate this data frame to the input register. Then the input data request (IDR) signal is set. The computer detects the IDR, and if it has priority, stores the data on the input lines in a specified memory location. After processing this data, the computer sends an input data acknowledge (ID ACK) to the I/O Console. Upon detecting the ID ACK from the computer, the I/O Console control circuits clear the IDR signal, send an advance signal to the reader, causing the tape to move toward the next sprocket hole and, after a 2μsec delay, clear the input register. A sprocket pulse is generated and detected as previously described. This action continues until the computer input buffer is full or the reader is deactivated by the program. The program may transfer one word into the computer, process this word and reestablish a second buffer without considering timing, since the I/O Console holds each frame read until the ID ACK is detected. After data transmission is complete, the program should deactivate the reader by sending an external function word of 010_8 (or 011_8) to the I/O Console. The tape read operation can be stopped by the computer, as described under Automatic Termination of ON-LINE reader operation or by the following methods.

a. Raising the tape head.

b. Depressing the START READ CLR pushbutton.

c. Depressing the READ CLR pushbutton.

d. Depressing the MASTER CLEAR pushbutton.

3-132. TAPE READER OPERATION, DETAILED. Refer to operational flow diagram (figure 3-50) and referenced logic diagrams for the following discussion of reader operations. Steps 1, 2, 9, 43, and 61 through 86 of the operational flow diagram are applicable to reader operation.

3-133. External Function Acknowledge Enable. As previously described, the EF ACK from the computer produces a 2μsec high from gate 19D01 (5-5, 4B). This high is inverted by driver-inverter 21D00 (5-6, 6B) to partially enable gate 19D00 (5-6, 6B).

3-134. External Function Word Conversion and Translation. External function words are received from the computer by the 20GXX gates (figures 5-11 and 5-12). For a read operation, an external function word of 150_8 (or 151_8) is received. Active bits 2^3, 2^5, and 2^6 are converted to I/O Console low logic levels (-4.5 VDC) by gates 20G03 (5-11, 7B), 20G05 (5-12, 4B) and 20G06 (5-12, 6B), respectively. The 20G03 (5-11, 7B) output is amplified by 21G03 (5-11, 6C) and routed for figure 5-6 as the low when INPUT DEVICE signal. The 20G05 (5-12, 4B)and 20G06 (5-12, 6B) outputs are routed directly to figure 5-6 as the low when EN READ 29D00 (5-6, 5B) and low when EN SET START READ 19D00 (5-6, 6B) signals, respectively.

3-135. Light READ Indicator and Set START READ F/F. On figure 5-6, the low when INPUT DEVICE partially enables 19D00 (5-6, 6B) and 29D00 (5-6, 6B). The low when EN READ signal fully enables 29D00 (5-6, 5B) and lights READ indicator-switch (DS 17). The low when EN SET START READ signal fully enables 19D00, (5-6, 6B) whose high output is

inverted by 20D00 (5-6, 6C) and used to set START READ F/F 0XD00 (5-6, 6C). With 0XD00 set, START READ indicator (DS 21) lights.

3-136. Disable Keyboard Mode and Clear INTERRUPT F/F, KEYBOARD REQ ENABLE F/F, and KEYBOARD INPUT READY F/F. The high from 29D00 (5-6, 5B) prevents enabling gate 28D00 (5-6, 4B), thus disabling keyboard mode during a read operation. The low when CLR from 28D00 (5-6, 4B) is routed to figure 5-4, where it is inverted by 29F04 (5-4, 8B) and then by 30F04 (5-4, 8C), and used to clear INTERRUPT F/F 0XF02 (5-4, 6C), KEYBOARD REQ ENABLE F/F 0XF03 (5-4, 7C) and KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C).

3-137. Start Reader Motor. The high from 29D00 (5-6, 5B) causes a low output from inverter 31D00 (5-6, 4C) to initiate a START READER signal from 32D00 (5-6, 5C). The START READER signal goes to energize READER relay K3 (5-13, 4C). When K3 is energized, it completes a 115-VAC, 60-Hz path to reader input A3A1J1-C.

3-138. Set READ READY F/F. The high from 29D00 (5-6, 5B) removes the low when CLR READ RDY from READ READY F/F 0XF00 (5-4, 3C). Low when SET READ RDY from 31D00 (5-6, 4C) is delayed 0.5 second by 19F00 (5-4, 3B) and applied through 20F00 (5-4, 3B) to set READ READY F/F 0XF00 (5-4, 3C).

3-139. Clear Input Register and Advance Tape Until Sprocket Pulse is Detected. With the tape head lowered, a high when READER EN from 30D00 (5-6, 6B) is inverted to a low by 19F01 (5-4, 4B) to partially enable gates 42F01 (5-4, 4D) and 43F01 (5-4, 3C). In the absence of a sprocket pulse, a low output is produced from 20F01 (5-4, 4B) which partially enables setting READER INPUT REQUEST ENABLE F/F 0XF01 (5-4, 4C), partially enables gate 41F01 (5-4, 4C), and prevents the low when EN data to input register signal from 40F01 (5-4, 4C). With READ READY F/F 0XF00 (5-4, 4C) set, it outputs a low which partially enables gates 43F01 (5-4, 3C) and 50F00 (5-4, 3D) and sets READER INPUT REQUEST ENABLE F/F 0XF01 (5-4, 4C). The low from 0XF01 (5-4, 4C) further enables 42F01 (5-4, 4D); however, all enabling conditions for 42F01 (5-4, 4D) are not met at this time, and its output will be low. Since 41F01 (5-4, 4C) is partially enabled by the low from 20F01 (5-4, 4B), the 42F01 (5-4, 4D) output will remain low until conditions change (reader sprocket pulse detected). This low from 42F01 (5-4, 4D) fully enables 43F01 (5-4, 3C), producing a high at its output which is fed through 44F01 (5-4, 3C) as an ADVANCE TAPE signal to A3A1J2-Y of the tape reader. The high from 43F01 (5-4, 3C) also disables 50F00 (5-4, 3D) so that it produces a low to partially enable 50F04 (5-4, 7D). The low from the clear side of KEYBOARD INPUT READY F/F 0XF04 further enables 50F04 (5-4, 7D), which is fully enabled by the low from 28F01 (5-4, 5B) (due to the lack of an INPUT ACK). With gate 50F04 (5-4, 7D) fully enabled, a low when CLR INPUT REGISTER signal is sent to inverter 29I00 (5-9, 8B), amplified by 30I00 (5-9, 8B), and used to clear the input register flip-flops (figures 5-9 and 5-10).

3-140. Stop Tape and Gate Data to Input Register. When a spocket pulse is detected, 20F01 (5-4, 4B) produces a high output which is used to disable gate 41F01 (5-4, 4C). With 41F01 (5-4, 4C) disabled, its low output fully enables 42F01 (5-4, 4D), producing a high to disable 43F01 (5-4, 3C). When 43F01 (5-4, 3C) is disabled, its low output is applied to 44F01 (5-4, 3C) to remove the ADVANCE TAPE signal to the tape reader. The low from 43F01 (5-4, 3C) also fully enables gate 50F00 (5-4, 3D) to produce a high output which is used to disable 50F04 (5-4, 7D) and remove the low when CLR INPUT REG signal to the input registers. The high from 20F01 (5-4, 4B) is also inverted by 40F01 (5-4, 4C) to become a low when EN DATA INPUT REG

signal. This signal, along with the low when DATA TO INPUT signal from 31D00 (5-6, 4C), enables 17I00 (5-9, 7B). The low when READER to INPUT REG from 17I00 gates data from the reader into the input register flip-flops (figures 2-9 and 2-10).

3-141. Generate Input Request. The high from 50F00 (5-4, 3D) disables 50F03 (5-4, 7D), producing a low which is delayed 4.4µsec by 52F03 (5-4, 7D) and applied as a partial enable for 50F02 (5-4, 5C). The high when EN REQ signal from START READ F/F 0XD00 (5-6, 6C) is inverted through gate 44F02 (5-4, 6B) to enable 45F02 (5-4, 6B), whose output disables 46F02 (5-4, 6C). A low from 46F02 (5-4, 6C) further enables 50F02 (5-6, 5C). The negative output from INTERRUPT F/F 0XF02 (5-6, 6C) fully enables driver 50F02 (5-5, 6C) to generate a high when INPUT REQ signal for transmittal to the computer. The input data request is detected by the computer. The computer then stores the data on its input lines in a specific memory location. After processing the data, the computer transmits an input data acknowledge to the I/O Console.

3-142. Input Acknowledge and Clear READER INPUT REQUEST ENABLE. The ID ACK from the computer is converted to a low I/O logic level (-4.5 VDC) by 24F01 (5-4, 6B), which enables gate 25F01 (5-4, 6B). The high output from 25F01 (5-4, 6B) is inverted through 26F01 (5-4, 5A) and used as a partial enable for 28F01 (5-4, 5B). The low from 26F01 (5-4, 5A) is also routed through 27F01 (5-4, 5B), which allows 28F01 (5-4, 5B) to be fully enabled for 2µsec. The 28F01 (5-4, 5B) output is a 2µsec positive pulse whose starting edge is coincident with the ID ACK. This 2µsec positive pulse is stretched to 2 msec by 30F01 (5-4, 4A) and inverted by 31F01 (5-4, 4B). The leading edge (5-4, 4B) of the negative 2 msec pulse from 31F01 (5-4, 4B) clears READER INPUT REQUEST ENABLE F/F 0XF01.

3-143. Clear Input Register and Drop INPUT REQ. The high output from READER REQUEST ENABLE F/F 0XF01 (5-4, 4C) disables 42F01 (5-4, 4D), producing a low output which fully enables 43F01 (5-4, 3C), and a high output is produced. This high is inverted to a low when ADVANCE TAPE signal which is transmitted to the tape reader. At the same time, the high from 43F01 (5-4, 3C) disables 50F00, (5-4, 3D), which produces a low output to partially enable 50F04 (5-4, 7D). The 2µsec positive pulse from 28F01 (5-4, 5B) is applied to the 50F04 (5-4, 7D) input. At the end of the pulse, this signal goes negative and further enables 50F04 (5-4, 7D). The low from the clear side of KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C) provides the final enabling signal for 50F04 (5-4, 7D), which now provides a low when CLR INPUT REG signal to clear the input register as previously described. Also, the low from 50F00 (5-4, 3D), along with the low from the clear side of KEYBOARD REQ ENABLE F/F 0XF03 (5-4, 7C), enables 50F03 (5-4, 7D), which produces a high to disable 51F03 (5-4, 6D) and prevent one of the enabling signals for 50F02 (5-4, 5C). With 50F02 (5-4, 5C) disabled, the INPUT REQ signal is removed.

NOTE

A 4.4µsec delay 52F03 (5-4, 6D) is not effective with a low input. The low input forces the output with no delay.

3-144. Set READER INPUT REQUEST ENABLE. At the end of 2 msec, the negative pulse from 31F01 (5-4, 4B) goes positive, releasing the clear side of READER INPUT REQUEST ENABLE F/F 0XF01 (5-4, 4C). 20F01 (5-4, 4B) produces a low output until a sprocket pulse is received. This negative output, along with the low from READ READY F/F 0XF00, sets 0XF01 (5-4, 4C), providing a low output to partially enable 42F01 (5-4, 4D). However, all enabling conditions for 42F01 (5-4, 4D) are not met at this time, and

its output will remain low until conditions change (reader sprocket pulse detected). Since the output of 42F01 (5-4, 4D) does not change from its previous state, the ADVANCE TAPE signal from 44F01 (5-4, 3C) will continue until a sprocket pulse is detected.

NOTE

The remaining reader procedures are repetitions from paragraph 3-137.

3-145. Automatic Termination of ON-LINE Reader Operation. After all data transmission has been completed, the computer places an external function word of 010_8 on its output lines and transmits an external function acknowledge to the I/O Console. When the EF ACK and EF word are received by the I/O Console, the following sequences occur:

a. The EF ACK generates a 2μsec positive pulse from 19D01 (5-5, 4B) which is inverted to a low by 20D01 (5-5, 5B) and stretched to a 70 msec negative pulse by 22D00 (5-5, 3C). The low from 22D00 (5-5, 3C) is inverted by 36D00 (5-5, 3C), disabling 40D00 (5-5, 3C) and preventing generation of another EF REQ signal for 70 msec after receiving an EF ACK.

b. The 2μsec positive pulse from 19D01 (5-5, 4B) is inverted by 21D00 (5-6, 6B) to partially enable 27D00 (5-6, 3D).

c. Bit 2^3 of the EF word provides a low from 20G03 (5-11, 6B), which is amplified by 21G03 (5-11, 6C) and routed as the low when INPUT DEVICE signal to figure 5-6, where it is used to partially enable AND gate 25D00 (5-6, 3C).

d. The absence of EF word bits 2^5 and 2^6 provides highs from 20G05 (5-12, 4B) and 20G06 (5-12, 6B), which are routed to figure 5-6 to disable gates 19D00 (5-6, 6B) and 29D00 (5-6, 5B), and enable 24D00 (5-6, 3B). The low from 19D00 (5-6, 6B) is inverted by 20D00 (5-6, 6C), disabling the set signal from START READ F/F 0XD00 (5-6, 6C).

e. With 24D00 (5-6, 3B) enabled, its low output fully enables 25D00 (5-6, 3C), producing a high which is inverted by 26D00 (5-6, 3C) to enable 27D00 (5-6, 3D). The high from 27D00 (5-6, 3D) prevents interlocking sides of KEYBOARD gate 28D00 (5-6, 4C) and READ gate 29D00 (5-6, 5C) from being enabled.

f. The low from 29D00 (5-6, 5C) extinguishes READ indicator (DS 17); clears START READ F/F 0XD00 (5-6, 6C), extinguishing START READ indicator (DS 21); removes the READ disable from KEYBOARD gate 28D00 (5-6, 4C); and provides a low when CLR READ RDY signal. The low from 29D00 (5-6, 5B) is also inverted by 31D00 (5-6, 4C), which produces a high output removing the low when SET READ RDY signal from the READ READY F/F 0XF00 (5-4, 3C), allowing it to be cleared by the low when READ RDY signal from 29D00 (5-6, 5B). The high from 31D00 (5-6, 4C) prevents the transfer of data to the input register by removing the low when DATA TO INPUT, and stops the reader motor by releasing the START READER signal through 32D00 (5-6, 5C).

g. With READ READY F/F 0XF00 (5-4, 3C) cleared, its high output disables 43F01 (5-4, 3C) and 50F00 (5-4, 3D).

h. Disabling 43F01 (5-4, 3C) and 50F00 (5-4, 3D) stops tape movement by removing the ADVANCE TAPE signal to the reader from 44F01 (5-4, 3D).

i. The low from 50F00 (5-4, 3D) keeps 50F03 (5-4, 7D) enabled, thus disabling 51F03 (5-4, 6D) and preventing further INPUT REQ signals from 50F02 (5-4, 5C). The low from 50F00 (5-4, 3D) is also used to partially enable 50F04 (5-4, 7D), which is further enabled by the low from the clear side of KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C). The absence of ID ACK from the computer produces a low from 28F01, (5-4, 5B), which fully enables 50F04 (5-4, 7D), producing a low when CLR INPUT REG signal to clear the input register flip-flops (figures 5-9 and 5-10).

3-146. Manual Termination of ON-LINE Reader Operation. Various methods for manually stopping the reader are discussed in the following paragraphs.

3-147. Raising the Tape Head. When the reader tape head is raised, the high when TAPE HEAD UP signal from the reader is inverted by 30D00 (5-6, 6B) and the following occurs:

a. The low output from 30D00 (5-6, 6B) holds START READ F/F OXD00 (5-5, 6D) clear and extinguishes START READ indicator DS 21 (provided 70 msec have elapsed since the last EF ACK was received from the computer).

b. The low from 30D00 (5-6, 6B) is inverted by 19F01 (5-4, 4B) to disable 20F01 (5-4, 4B) and 43F01 (5-4, 3C).

c. Disabling 20F01 (5-4, 4B) prevents the transfer of data to the input register by removing the low when EN DATA TO INPUT REG signal from 40F01 (5-4, 4C).

d. Disabling 43F01 (5-4, 3C) and 50F00 (5-4, 3D) stops tape movement by removing the ADVANCE TAPE signal to the reader from 44F01 (5-4, 3D).

e. The low from the clear side of START READ F/F OXD00 (5-6, 6C) partially enables 44F02 (5-4, 6B). If an automatic reader operation is attempted, 29D00 (5-6, 5B) is enabled and outputting a high, which is inverted to a low by 31D00 (5-6, 4C). This low on the high when EN REG signal line fully enables 44F02 (5-4, 6B). The high from 44F02 (5-4, 6B) disables 45F02 (5-4, 6B), whose low output is inverted by 46F02 (5-4, 6C) to disable 50F02 (54, 5C) and prevent generation of an INPUT REG.

3-148. Depressing the START READ CLEAR Pushbutton. When the START READ CLEAR pushbutton (S5, figure 5-6) is depressed, the START READ F/F OXD00 (5-6, 6C) is cleared. The low from the clear side of START READ F/F OXD00 (5-6, 6C) partially enables 44F02 (5-4, 6B). If an automatic reader operation is attempted, 29D00 (5-6, 5B) is enabled and outputting a high, which is inverted to a low by 31D00 (5-6, 4C). This low on the high when EN REG signal line fully enables 44F02 (5-4, 6B). The high from 44F02 (5-4, 6B) disables 45F02 (5-4, 6B), whose low output is inverted by 46F02 (5-4, 6C) to disable 50F02 (5-4, 5C) and prevent generation of an INPUT REQ.

3-149. Depressing the READ CLEAR Pushbutton. On figure 5-6, when the READ CLEAR (S6) pushbutton is depressed, the interlocking sides of READ GATE 29D00 (5-6, 5B) and KEYBOARD gate 28D00 (5-6, 4B) are disabled, and the sequences listed below will occur.

a. The low from 29D00 (5-6, 5C) extinguishes READ indicator (DS 17); clears START READ F/F OXD00 (5-6, 6C) extinguishing START READ indicator (DS 21); removes the read disable from KEYBOARD gate 28D00 (5-6, 4C); and provides a low when CLR READ RDY signal. The low from 29D00 (5-6, 5B) is also inverted by 31D00 (5-6, 4C), which produces a high output removing the low when SET READ RDY signal from the READ READY F/F OXF00 (5-4, 3C), allowing it to be cleared by the low when CLR READ RDY signal from 29D00 (5-6, 5B). The high from 31D00 (5-6, 4C) prevents the transfer of data to the input register by removing the low when DATA TO INPUT, and stops the reader motor by releasing the START READER signal through 32D00 (5-6, 5C).

b. With READ READY F/F OXF00 (5-4, 3C) cleared, its high output disables 43F01 (5-4, 3C) and 50F00 (5-4, 3D).

c. Disabling 43F01 (5-4, 3C) and 50F00 (5-4, 3D) stops tape movement by removing the ADVANCE TAPE signal to the reader from 44F01 (5-4, 3D).

d. The low from 50F00 (5-4, 7D) keeps 50F03 (5-4, 7D) enabled, thus disabling 51F03 (5-4, 6D) and preventing further INPUT REQ signals from 50F02 (5-4, 5C). The low from 50F00 (5-4, 3D) is also used to partially enable 50404 (5-4, 7D), which is further enabled by the low from the clear side of KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C). The absence of ID ACK from the computer produces a low from 28F01 (5-4, 5B), which fully enables 50F04 (5-4, 7D), producing a low when CLR INPUT REG signal to clear the input register flip-flops (figures 5-9 and 5-10).

3-150. Depressing the MASTER CLEAR Pushbutton. When the MASTER CLEAR pushbutton (S1, figure 5-3) is depressed, it produces a high when MASTER CLEAR which is routed to figures 5-5 and 5-6. The high from S1 (figure 5-3) is also inverted by 70E00 (5-3, 8B) and 70E01 (5-3, 8B) and routed, as low when MASTER CLEAR signals, to figures 5-4 and 5-5, respectively. The following sequences then occur:

a. On figure 5-5, the high when MASTER CLEAR is inverted to a low by 20D01 (5-5, 5-B). The low from 20D01 (5-5, 5B) produces a 70 msec negative pulse from 22D00 (5-5, 3C) which is inverted by 36D00 (5-5, 3C). This 70 msec positive pulse from 36D00 (5-5, 3C) prevents an EF REQ from being generated by disabling 40D00 (5-5, 3C). However, at the end of 70 msec, 40D00 (5-5, 3C) is again enabled and EF REQ signals may be generated.

b. When the 70 msec positive pulse from 36D00 (5-5, 3C) terminates, its low when EF REQ EN output signal partially enables the clear side of START READ F/F 0XD00 (5-6, 6C).

c. On figure 5-6, the high when MASTER CLEAR is inverted by 20D00 (5-6, 6C), whose low output full enables the clearing of START READ F/F 0XD00 (5-6, 6C). The low from the clear side of START READ F/F 0XD00 (5-6, 6C) partially enables 44F02 (5-4,6B). If an automatic reader operation is attempted, 29D00 (5-6, 5B) is enabled and outputting a high, which is inverted to a low by 31D00 (5-6, 4C). This low on the high when EN REG signal line fully enables 44F02 (5-4, 6B). The high from 44F02 (5-4, 6B) disables 45F02 (5-4, 6B), whose low output is inverted by 46F02 (5-4, 6C) to disable 50F02 (5-4, 5C) and prevent generation of an INPUT REQ.

d. On figure 5-4, the low when MASTER CLEAR sets READER REQUEST ENABLE F/F 0XF01 (5-4, 4C).

e. On figure 5-6, the low when MASTER CLEAR signal is inverted to a high by 71D01 (5-6, 2D). This produces the same effect as depressing the READ CLEAR pushbutton.

3-151. TAPE PUNCH OPERATION, GENERAL. To operate the tape punch in the on-line mode, the computer sends an external function word of 005_8 (or 015_8) to the I/O Console. When the I/O Console receives the EF word, the PUNCH F/F is set, PUNCH indicator lights, and power is applied to the punch motor. The sequence of events is as follows:

a. At the punch, each rotation of the main motor shaft produces a flywheel (sync) pulse which is applied to the I/O Console control circuits.

b. When the first sync pulse is received from the punch, a 10 msec delay is initiated, which allows PUNCH READY F/F to be set on the next sync pulse (provided it occurs during the 10 msec delay period). When the PUNCH READY F/F is set, an output data request (ODR) is sent to the computer.

c. The computer detects the ODR, places data from an assigned memory location on its output lines (2^0 through 2^x), and transmits an output data acknowledge (OD ACK) to the I/O Console.

d. Upon detecting the OD ACK from the computer, the I/O Console control circuits gate the on-line data to the output register, drop the ODR, set the TAPE FEED F/F, and light the TAPE FEED indicator.

e. When the next sync pulse is received from the punch, the TAPE FEED F/F is cleared, TAPE FEED indicator extinguished, and a 4 msec gate generated to gate punch-data, and to gate a feed-hole signal from the output register to the punch. This gate also prevents generation of an ODR during this time. The data configuration is then punched into the tape and the tape advanced to the next frame.

NOTE

Each revolution of the punch drive mechanism produces a flywheel (sync) pulse. This pulse is used to gate data and a feed-hole signal from the output register to the punch. Although the punch-data and feed-hole signals are transmitted simultaneously, the mechanical timing within the punch is such that tape punching occurs before the tape is advanced to the next frame.

f. When the 4 msec gate terminates, the output register is cleared and another ODR generated. The computer detects the ODR and the cycle is repeated until the computer output buffer is empty or the punch is deactivated by the program.

g. After data transmission is complete, the program should deactivate the punch by sending an external function word of 001_8 (or 011_8) to the I/O Console.

h. The tape punch operation can be stopped by the computer, or by:

(1) Depressing PUNCH CLEAR pushbutton;

(2) Depressing MASTER CLEAR pushbutton.

3-152. TAPE PUNCH OPERATION, DETAILED. Refer to operational flow diagram (figure 3-50) and referenced logic diagrams for the following discussion of punch operations. Steps 1, 2, 3, 10, 12 through 18, and 31 through 42 of the operational flow diagram are applicable to punch operation.

3-153. External Function Acknowledge Enable. As previously described, the EF ACK from the computer produces a 2µsec high from gate 19D01 (5-5, 4B) which is inverted to a low by inverter 20D02 (5-5, 5C) to partially enable the set side of PUNCH F/F 0XD02 (5-5, 5D).

3-154. External Function Word Conversion and Translation. For a punch operation, an external function word of 005_8 (or 015_8) is received from the computer. Active bits 2^0 and 2^2 are converted to I/O Console low logic levels (-4.5 VDC) by gates 20G00 (5-11, 3B) and 20G02 (5-11, 5B) and routed to figure 5-5 as the low when OUTPUT DEVICE and low when SET PUNCH signals, respectively.

3-155. Set PUNCH F/F and Start Punch Motor. On figure 5-5, the low when SET PUNCH and low when OUTPUT DEVICE fully enable the set side of PUNCH F/F 0XD02 (5-5, 5D). With 0XD02 set, the high from the clear side lights PUNCH indicator switch (DS 18) and is inverted to a low by 50D02 (5-5, 8B) to initiate a START PUNCH signal from 53D02 (5-5, 8C). The START PUNCH signal goes to energize PUNCH relay K1 (5-13, 4C). When K1 is energized, it completes a 115-VAC, 60-Hz path to punch input A3A2J2-2.

3-156. Set PUNCH READY F/F. The high from the clear side of PUNCH F/F (5-5, 5D) removes the low when CLR PUNCH RDY signal from the clear side input of PUNCH RDY F/F 0XE01 (5-2, 4C) and the low when EN SET PUNCH RDY signal from the set side of 0XD02 (5-5, 5D) is used as a partial enable for setting 0XE01 (5-2, 4B). The high from the clear side

of PUNCH F/F 0XD02 (5-5, 5D) also enables 50D02 (5-5, 8B) which outputs a low to 53D02 (5-5, 8C) to start the punch motor and to 51D00 (5-5, 7B) time delay to allow the punch motor to get up to speed before setting the PUNCH READY F/F 0XE01 (5-2, 4B). At the punch, each rotation of the punch motor shaft produces a flywheel (sync) pulse. The negative portion of this pulse is converted to I/O Console logic levels and inverted by 29E00 (5-2, 3B).

3-157. Clear Output Register. Since TAPE FEED F/F 0XE00 (5-2, 4C) is clear at this time, the low from its clear side partially enables gate 53E00 (5-2, 6C). Time delay 51E00 (5-2, 3C) is normally outputting a low which further enables 53E00 (5-2, 6C). Gate 53E00 is fully enabled by the low from inverter 52E02 (5-2, 6C), which is presented at all times except when ENABLE PRINT F/F 0XE02 (5-2, 5C) is set. Enabling 53E00 (5-2, 6C) produces a high output which is inverted by 57E00 (5-2, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 (5-11, 8B) is amplified by 30G00 and used to clear the output register flip-flops (figure 5-11 and 5-12).

3-158. Generate Output Data Request. The high from 53E00 (5-2, 6C) partially enables gate 54E00 (5-2, 6C). With PUNCH READY F/F 0XE01 (5-2, 4B) set, its low output partially enables the set side of TAPE FEED F/F 0XE00 (5-2, 4C) and gate 50E01 (5-2, 7B). Gate 50E01 (5-2, 7B) is fully enabled by the low when CLR PRINT RDY F/F signal which is present at all times except during printer operations. The high from 50E01 (5-2, 7B) provides the final enable for gate 54E00 (5-2, 6C) whose low output is used to partially enable OUTPUT REQ generator 56E00 (5-2, 7C). A low when EN REQ signal from 71H21 (5-8, 3C) is present at all times when the serializer is inactive. This signal is inverted by 71H22 (5-2, 7B), reinverted by OR gate 54E01 (5-2, 7B), and applied as a partial enable for 56E00 (5-2, 7C). The final enable for 56E00 (5-2, 7C) is the low when EN REQ, which comes from the clear side of OFF-LINE F/F 0XD03 (5-5, 6D), is present during all on-line operations. When 56E00 (5-2, 7C) is enabled, it generates an OUTPUT REQ signal for transmittal to the computer. The output data request is detected by the computer. The computer then places data from an assigned memory location on its output line (2^0 through 2^7) and transmits an output data acknowledge (OD ACK) to the I/O Console.

3-159. Set TAPE FEED F/F, Remove ODR and Gate Data to Output Register. The OD ACK from the computer is converted to a low console logic level (-4.5 VDC) by 47E04 (5-3, 3B) to enable gate 48E04 (5-3, 3C) since the low when COPY enabling signal is present during all on-line operations. The high from 48E04 (5-3, 3C) is inverted to a low by 51E04 (5-3, 3C) to partially enable gate 53E04 (5-3, 3C). The low from 51E04 (5-3, 3C) is also routed through 52E04 (5-3, 3C), which allows 53E04 (5-3, 3C) to be fully enabled for 2µsec. The 53E04 output is a 2µsec low when GATE OUTPUT DATA signal which is used to fully enable setting TAPE FEED F/F 0XE00 (5-2, 4C). The high output from 0XE00 (5-2, 4C) lights TAPE FEED indicator-switch (DS 20) and disables gate 53E02 (5-2, 6C). The low from 53E02 (5-2, 6C) is inverted by 57E00 (5-2, 6C), removing the low when CLR OUTPUT REG signal from its output line. The low from 52E02 (5-2, 6C), whose high output disables 53E00 (5-2, 6C), preventing generation of an OUTPUT REQ signal. The 2µsec low when GATE OUTPUT DATA signal from 53E04 (5-3, 3C) is also used to fully enable 19G00 (5-11, 3C) since the low when $\overline{\text{COPY}}$ enabling signal is present during all on-line operations. The low from 19G00 (5-11, 7B) gates the on-line data into the output register flip-flops 0XG00 (5-11, 3C) through 0XG07 (5-12, 7C) (figures 5-11 and 5-12).

3-160. Gate Data to Punch. With TAPE FEED F/F 0XE00 (5-2, 4C) set, its high output partially enables 50E00 (5-2, 3B). When the next flywheel pulse from the punch is sensed by 29E00 (5-2, 3B), its high output fully enables 50E00 (5-2, 3B), whose negative output is inverted by 49E00 (5-2, 3C) and stretched into a 4 msec positive pulse by time delay circuit 51E00 (5-2, 3C). This gate is applied as a further disabling signal for gate 53E00 (5-2, 6D), which was initially disabled when TAPE FEED F/F 0XE00 (5-2, 4C) was set. The signal from 51E00 (5-11, 3C) is also inverted by 52E00 (5-2, 3D) and amplified by 49G00 (5-11, 3C) to become the low when DATA to PUNCH signal, which is used to partially enable gates 50G00 through 50G07 (figures 5-11 and 5-12). These gates will be fully enabled or disabled in accordance with the bit configuration stored in output register flip-flops 0XG00 (5-11, 7C) through 0XG07 (5-12, 7C), respectively. When a particular flip-flop is set (contains a binary 1), its associated gate will be enabled. Conversely, when a particular flip-flop is clear (contains a binary 0), its respective gate will be disabled. The 50G00 (5-11, 3C) through 50G07 (5-12, 7C) outputs are converted to punch logic levels by 51G00 (5-11, 3C) through 51G07 (5-12, 7C), respectively, and transmitted to the punch as PUNCH DATA signals.

3-161. FEED HOLE Signal to Punch. The low when DATA to PUNCH signal from 49G00 (5-11, 3B) is amplified through 40G06 (5-12, 8C) to enable 41G06 (5-12, 8C), whose output is transmitted to the punch as the FEED HOLE signal.

3-162. Clear TAPE FEED F/F. The low from 49G00 (5-11, 3C) is also routed to figure 5-2 as the low when EN CLR TAPE FEED F/F signal and used to partially enable gate 30E00 (5-2, 4B). At the end of the flywheel pulse, the 29E00 (5-2, 3B) output goes low and 30E00 (5-2, 4B) is fully enabled. The low from 30E00 (5-2, 4B) clears TAPE FEED F/F 0XE00 (5-2, 4C), extinguishing the TAPE FEED indicator (DS 20), disabling 50E00 (5-2, 3B), and partially enabling gate 53E00 (5-2, 6D).

3-163. Clear Output Register. Gate 53E00 (5-2, 6D) is fully enabled when the 4 msec positive pulse from time delay circuit 51E00 (5-2, 3C) terminates (goes low) since the low enabling signal from 52E02 (5-2, 6C) is present at all times except during printer operations. The high from 53E00 (5-2, 6D) is inverted by 57E00 (5-2, 8C) to produce the low when CLEAR OUTPUT REG signal, which is routed to inverter 29G00 (5-11, 8B). The high from 29G00 (5-11, 8B) is amplified by 30G00 5-11, 8B) and used to clear the output register.

NOTE

The remaining punch operations are listed in paragraph 3-161.

3-164. Automatic Termination of ON-LINE Punch Operation. After all data transmission has been completed, the computer initiates an external function acknowledge (EF ACK) and transmits an external function word 001_8 to the I/O Console. When this EF ACK and EF word are received by the I/O Console, the following sequences occur:

a. The EF ACK generates a 2µsec positive pulse from 19D01 (5-5, 4B) which is inverted to a low by 20D01 (5-5, 5B) and stretched to a 70 msec negative pulse by 22D00 (5-5, 3C). The low from 22D00 (5-5, 3C) is inverted by 36D00 (5-5, 3C), disabling 40D00 (5-5, 3C) and preventing generation of another EF REQ signal for 70 msec after receiving an EF ACK.

b. The 2µsec high from 19D01 (5-5, 4B) is inverted to a low by 20D01 (5-5, 5B) to partially enable the clear side of PUNCH F/F 0XD02 (5-5, 5D). Bit 2^0 is converted to an I/O low logic

level (-4.5 VDC) by gate 20G00 (5-11, 3B) and routed to figure 5-5 as the low when OUTPUT DEVICE signal to further enable the clear side of 0XD02 (5-5, 5D). The absence of EF word bit 2^2 provides a high from 20G02 (5-11, 5B) which is routed on the low when SET PUNCH signal line to figure 5-5 where it is inverted by 30D02 (5-5, 5C) to provide the final enabling signal for clearing 0XD02 (5-5, 5D).

c. With PUNCH F/F 0XD02 (5-5, 5D) cleared, the low from its clear side extinguishes PUNCH indicator (DS 18) and is inverted to a high by 50D02 (5-5, 8B) to remove the START PUNCH signal from 53D02 (5-5, 8C). Removing the START PUNCH signal deenergizes K1 (5-13, 4C) by breaking the 115-VAC, 60-Hz path in order to drop the punch input A3A2J2-2 and stop the punch motor.

d. The low when CLR PUNCH RDY signal from the clear side of PUNCH F/F 0XD02 (5-5, 5D) clears PUNCH READY F/F 0XE01 (5-2, 4B).

e. When PUNCH READY F/F 0XE01 (5-2, 4B) is cleared, its set output produces a high which disables the set side of TAPE FEED F/F 0XE00 (5-2, 4C) and also disables 50E01 (5-2,7B). The low from 50E01 (5-2, 7B) disables gate 54E00, whose high output disables 56E00 (5-2, 7C), preventing further generation of an OUTPUT REG signal (ODR).

f. With the punch motor stopped, no further flywheel (sync) pulses will be detected by 29E00 (5-2, 3B), and time delay circuit 51E00 (5-2, 3C) will be outputting a low which will prevent transfer of data from the output register to the punch by disabling the low when DATA to PUNCH output from 52E00 (5-2, 3D). The low from 51E00 (5-2, 3C) also partially enables 53E00 (5-2 6C), which is further enabled by the low from the clear side of TAPE FEED F/F 0XE00 (5-2, 4C), and fully enabled by the low from 52E02 (5-2, 6C) (which is present at all times except during printer operations).

g. With gate 53E00 (5-2, 6C) enabled, its high output is inverted by 57E00 (5-2, 8C), providing the low when CLEAR OUTPUT REG signal used to clear the output register (figures 5-11 and 5-12).

3-165. Manual Termination of ON-LINE Punch Operation. Various methods for manually stopping the punch are described in the following paragraphs.

3-166. Depressing the PUNCH CLEAR Pushbutton. On figure 5-5, when the PUNCH CLEAR pushbutton (S7) is depressed, the PUNCH F/F 0XD02 (5-5, 5D) is cleared, and the sequence of events occurs as described in paragraph 3-164, steps c. through g..

3-167. Depressing the MASTER CLEAR Pushbutton. When the MASTER CLEAR pushbutton (S1, figure 5-3) is depressed, it produces a high when MASTER CLEAR which is routed to figures 5-2 and 5-5. The high from S1 (5-3, 7B) is also inverted by 70E00 (5-3, 8B) and routed, as the low when MASTER CLEAR signal to figure 5-2 and 5-5. The following sequences then occur:

a. On figure 5-5, the high when MASTER CLEAR is inverted to a low by 20D01 (5-5, 5B). The low from 20D01 (5-5, 5B) produces a 70 msec negative pulse from 22D00 (5-5, 3C) which is inverted by 36D00 (5-5, 3C). This 70 msec positive pulse from 36D00 (5-5, 3C) prevents an EF REQ from being generated by disabling 40D00 (5-5, 3C). However, at the end of 70 msec, 40D00 (5-5, 3C) is again enabled and EF REQ signals may be generated.

b. On figure 5-5, the low when MASTER CLEAR clears PUNCH F/F 0XD02 (5-5, 5D), and the sequence of events occurs as described in paragraph 3-164, steps c. through e..

c. On figure 5-2, the low when MASTER CLEAR signal is used to ensure that TAPE READ F/F 0XE00 (5-2, 4C) is cleared.

d. Refer to paragraph 3-164, steps f. and g..

e. On figure 5-2, the high when MASTER CLEAR signal is used to ensure 57E00 (5-2, 8C) outputs the low when CLEAR OUTPUT REG signal necessary to clear the output register.

3-168. **LOGIC DESCRIPTION, OFF-LINE MODE.**

3-169. OFF-LINE MODE. The following paragraphs contain a detailed functional description of the logic circuitry in the I/O Console OFF-LINE mode of operation. Refer to operational sequence flow diagram (figure 3-53), during the following discussion of off-line control circuitry.

3-170. CONTROL CIRCUITS, GENERAL. All I/O Console operations are manually selected in the off-line mode of operation. One input device (keyboard or reader) and either one or both output devices (punch or printer) can be selected. The off-line operations explained in this manual cover selection of both the printer and the punch with each input device. Although these operations are similar to those explained for on-line operations, the I/O Console must operate independently of the computer; therefore, provision must be made for disabling all input data and requests to the computer, and all output data and acknowledgements from the computer. The input and output acknowledges normally received from the computer must be simulated within the I/O Console.

3-171. CONTROL CIRCUITS, DETAILED. See referenced logic diagrams for the following detailed analysis of the general off-line control circuitry.

3-172. Prevent Data Transfer to Output Register. When the ON-LINE/OFF-LINE switch (S4, figure 5-3) is placed in the OFF-LINE position, the high from S4-1 disables one side of 48E04 (5-3, 3C). Gate 48E04 (5-3, 3C) is fully disabled at this time since an OD ACK is not being received from the computer. The low from 48E04 (5-3, 3C) is inverted by 51E04 (5-3, 3C) to disable 53E04 (5-3, 3D), placing a high on the GATE OUTPUT DATA signal lines to figure 5-11 to disable 18G00 (5-11, 7B) and 19G00 (5-11, 7B), preventing transfer of data into the output register flip-flops (figures 5-11 and 5-12).

3-173. Disable Inputs, Interrupts, Requests, and Acknowledges. The high from S4-1 (5-3, 4C) is routed on the low when ON-LINE signal line to figures 5-4 and 5-5. On figure 5-4, the high on the low when ON-LINE signal line disables 45F02 (5-4, 6B) and one side of 25F01 (5-4, 6C). Disabling the appropriate side of 25F01 (5-4, 6C) blocks ID ACK signals from the computer. Disabling 45F02 (5-4, 6B) produces a low output, which is inverted by 46F02 whose high output prevents generation of INTERRUPT or INPUT REQ signals to the computer by disabling 51F02 (5-4, 6C) and 50F02 (5-4, 5C) respectively. On figure 5-5, the high on the low when ON-LINE signal line disables 19D01 (5-5, 4B) and 40D00 (5-5, 3C). Disabling 19D01 (5-5, 4B) blocks EF ACK signals from the computer. Disabling 40D00 (5-5, 3C) prevents generation of EF REQ signals to the computer.

3-174. Off-Line Enables and Set OFF-LINE F/F. With 19D01 (5-5, 4B) disabled, its low output is inverted by 20D01 (5-5, 5B), removing the low input signal from the clear side of OFF-LINE F/F 0XD03 (5-5, 6D), allowing it to be set as described below. The low (-4.5 VDC) from S4-2 (5-3, 4C) partially enables gate 50E04 (5-3, 4C) and is routed as low when OFF-LINE signals to figures 5-4 and 5-5. On figure 5-4 the low when OFF-LINE signal partially enables the side of 25F01 (5-4, 6C) associated with simulated input acknowledge signals. On figure 5-5, the low when OFF-LINE signal sets OFF-LINE F/F 0XD03 (5-5, 6D), lighting the COPY lamp (DS 19).

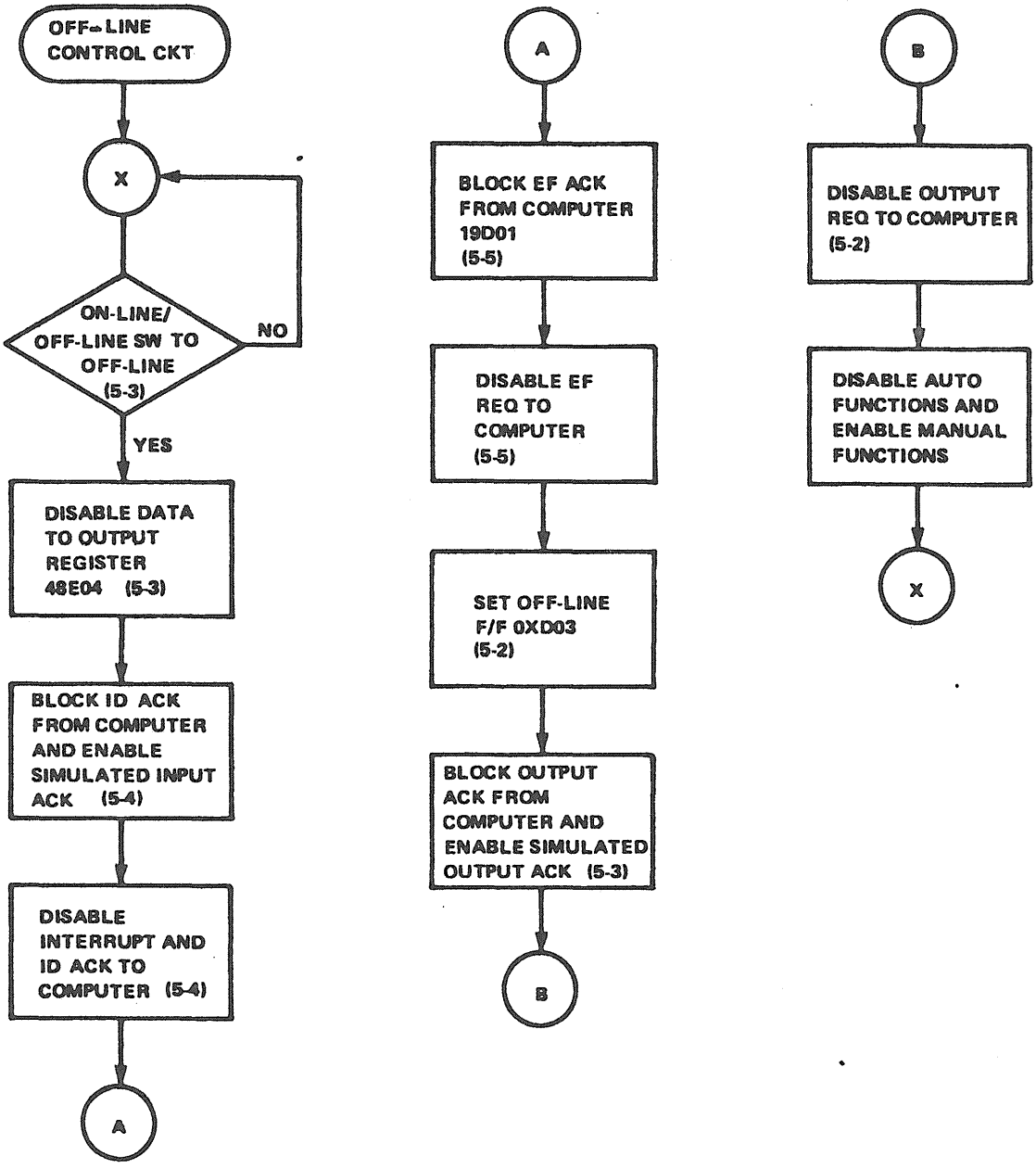


Figure 3-53. OFF-LINE Control Circuits, Operational Sequence Flow Diagram.

3-175. OFF-LINE F/F Outputs. With OFF-LINE F/F 0XD03 (5-5, 6D) set, its clear side outputs are high and its set side outputs are low. Highs from the clear side are routed to figure 5-11 on the high when GATE INPUT REG and low when $\overline{\text{COPY}}$ signal lines to figure 5-3 on the low when $\overline{\text{COPY}}$ line, and to figure 5-2 on the low when EN REQ line. Lows from the set side are routed on low when COPY lines to figures 5-3 and 5-4. On figure 5-11, the high when GATE INPUT REG signal is inverted by 17G00 (5-11, 8B) to partially enable 18G00 (5-11, 7B). The high on the low when $\overline{\text{COPY}}$ disables 19G00 (5-11, 7B). On figure 5-3, the high on

low when $\overline{\text{COPY}}$ line disables the appropriate side of 48E04 (5-3, 3C) to block OUTPUT ACK signals from the computer while the low when COPY signal partially enables the other side of 48E04 associated with circuits providing simulated output acknowledges. On figure 5-2, the high on the low when EN REQ signal line prevents generation of output request to the computer by disabling OUTPUT REQ generator 56E00 (5-6, 7C).

3-176. TAPE READER OPERATION, GENERAL. For off-line operations, the tape reader is initiated by depressing the READ, START READ, PRINT and/or PUNCH indicator switches on the I/O Console control panel. The following discussion involves off-line operations of the tape reader input with both printer and punch outputs.

3-177. When the tape head is lowered and the READ, START READ, PRINT, and PUNCH indicator switches are manually depressed, power is applied to the respective motors. When a sprocket pulse is detected, a frame is gated to the input register, the tape is stopped, OFF-LINE READ F/F sets. (If READ ONE switch is depressed, the OFF-LINE READ F/F never sets, causing only one frame to gate each time READ ONE switch is depressed.) With OFF-LINE READ ONE F/F set, a simulated output acknowledge occurs, gating the input register to the output register.

3-178. The serializer logics are enabled and TAPE FEED F/F is set. When the sync or flywheel pulse arrives from the punch, the frame in the output register is punched on tape and the TAPE FEED F/F cleared. Meanwhile the data in the input register is gated serially to the printer. After 81.81 msec, a simulated input acknowledge occurs which clears the OFF-LINE READ ONE F/F. After 18.18 msec, the OFF-LINE READ ONE F/F is set if OFF-LINE READ F/F is set. (If READ ONE switch is depressed, OFF-LINE READ F/F is cleared and the READ ONE switch must then be depressed in order to set the OFF-LINE READ ONE F/F.) This action takes place until all tape is read or until the I/O Console is manually master cleared.

3-179. TAPE READER OPERATION, DETAILED. Refer to operational flow diagram (figure 3-54) and referenced functional schematic diagrams for the following discussion of tape reader operations.

3-180. Light READ Indicator. Depressing READ indicator switch (DS 17, figure 5-6) disables one side of gate 27D00 (5-6, 3D). The other side is disabled by the high from 21D00 (5-6, 6B), which is present during all off-line operations. With 27D00 (5-6, 3D) completely disabled, its low output is applied to partially enable the interlocking side of READ gate 29D00 (5-6, 5B). Gate 29D00 (5-6, 5B) is fully enabled by the low from KB gate 28D00 (5-6, 4B), which is present at all times except during keyboard operations. Gate 29D00 (5-6, 5B) remains enabled and holds KB gate 28D00 5-6, 4B), which is present at all times except during keyboard operations. Gate 29D00 (5-6, 5B) disabled by interlocking action between the two gates. The high from 29D00 (5-6, 5B) lights READ indicator switch (DS 17).

3-181. Disable Keyboard Mode and Clear INTERRUPT F/F, KEYBOARD REQ ENABLE F/F, and KEYBOARD INPUT READY F/F. The high from 29D00 (5-6, 5B) prevents enabling gate 28D00 (5-6, 4B), thus disabling keyboard mode during a read operation. The low when CLR from 28D00 (5-6, 4B) is routed to figure 5-4, where it is inverted by 29F04 (5-4, 8B) and then by 30F04 (5-4, 8C) and used to clear INTERRUPT F/F 0XF02 (5-4, 6C), KEYBOARD REQ ENABLE F/F 0XF03 (5-4, 7C) and KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C).

3-182. Set START READ F/F. When START READ indicator switch (DS 21, 5-6, 6D) is depressed, START READ F/F 0XD00 (5-6, 6C) is set and DS 21 is illuminated.

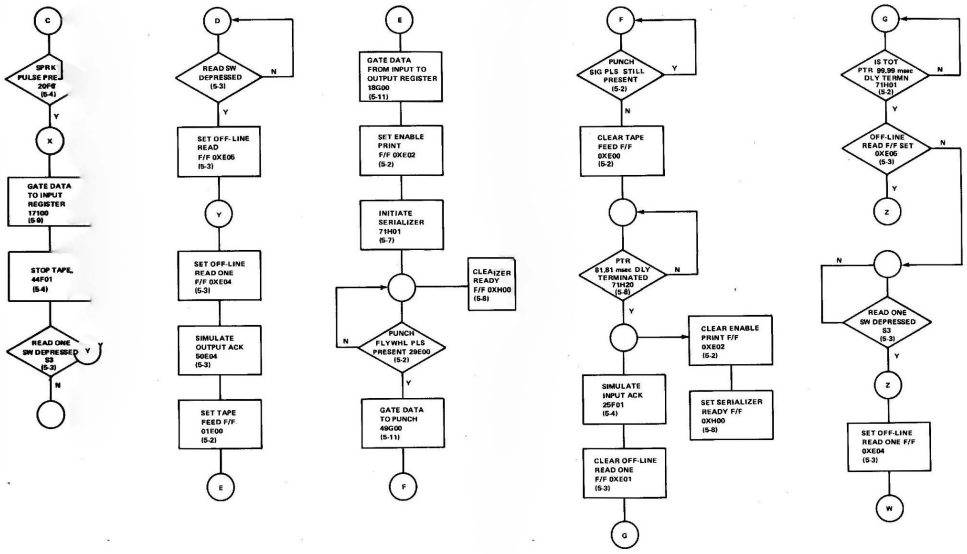


Figure 3-54. Off-Line Reader-Punch-Printer, Operational Flow Sequence Diagram (Sheet 1 of 2).

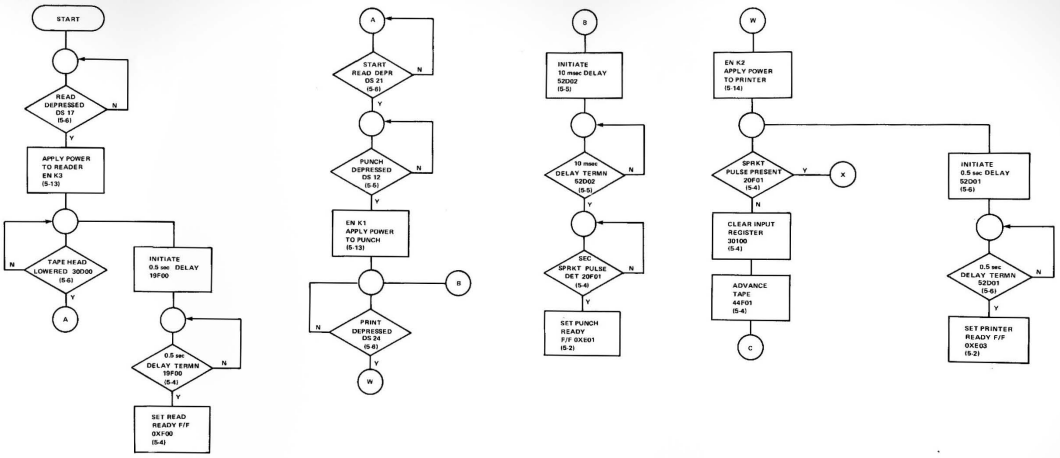


Figure 3-54. Off-Line Reader-Punch-Printer, Operational Flow Sequence Diagram (Sheet 2 of 2).

The high from the clear side of 0XD00 (5-6, 6C) remains the low when CLR OFF-LINE READ F/F signal from the clear side input of OFF-LINE READ F/F 0XE05 (5-3, 4B), while the low from the set side of 0XD00 (5-6, 6C) partially enables the set side of OFF-LINE READ ONE F/F 0XE04 (5-3, 6B).

3-183. Start Reader Motor. The high from 29D00 (5-6, 5B) causes a low output from inverter 31D00 (5-6, 5B) causes a low output from inverter 31D00 (5-6, 4C) to initiate a START READER signal from 32D00 (5-6, 5C). The START READER signal goes to energize READER relay (K3, 5-13, 3C). When K3 is energized, it completes a 115-VAC, 50-Hz path to reader input A3A1J1-C.

3-184. Set READ READY F/F. The high from 29D00 (5-6, 5B) removes the low when CLR READ RDY from READ RDY F/F 0XF00 (5-4, 3C). Low when SET READ RDY from 31D00 (5-6, 4C) is delayed 0.5 seconds by 19F00 (5-6, 3B) and applied through 20F00 to set 0XF00.

3-185. Clear Input Register and Advance Tape. With the tape head lowered, a high when READER EN from 30D00 (5-6, 6B) is inverted to a low by 19F01 (5-4, 4B) to partially enable gates 42F01 (5-4, 4D) and 43F01 (5-4, 3C). In the absence of a sprocket pulse, a low output is produced from 20F01 (5-4, 4C) which partially enables setting READER INPUT REQUEST ENABLE F/F 0XF01 (5-4, 4C), partially enables gate 41F01 (5-4, 4C), and prevents the low when EN DATA TO INPUT REGISTER signal from 40F01 (5-4, 4C).

3-186. With READ RDY F/F 0XF00 (5-4, 3C) set, a low is outputted which partially enables gates 43F01 (5-4, 3C) and sets READER INPUT REQUEST ENABLE F/F 0XF01 (5-4, 4C). The low from 0XF01 (5-4, 4C) further enables 42F01 (5-4, 4D); however, all enabling conditions for 42F01 (5-4, 4D) are not met at this time, and its output will be low. Since 41F01 (5-4, 4C) is partially enabled by the low from 20F01 (5-4, 4B), the 42F01 (5-4, 4D) output will remain low until conditions change (reader sprocket pulse detected). This low from 42F01 (5-4, 4D) fully enables 43F01 (5-4, 3C), producing a high as its output which is fed through 44F01 (5-4, 3C) as an ADVANCE TAPE signal to A3A1J2-Y of the tape reader. The high from 43F01 (5-4, 3C) also disables 50F00 (5-4, 3D) so that it produces a low to partially enable 50F04 (5-4, 7D). The low from the clear side of KEYBOARD INPUT READY F/F 0XF04 (5-4, 8C) further enables 50F04 (5-4, 7D), which is fully enabled by the low from 28F01 [(5-4, 5B) due to lack of an ID ACK]. With gate 50F04 (5-4, 7D) fully enabled, a low when CLR INPUT REGISTER signal is sent to inverter 29I00 (5-9, 8B), amplified by 30I00 (5-9, 8B), and used to clear the input register flip-flops (figures 5-9 and 5-10).

3-187. Set PUNCH F/F and Start Punch Motor. Depressing the PUNCH indicator switch (DS 18, 5-5) sets PUNCH F/F 0XD02 (5-5, 5D). With 0XD02 (5-5, 5D) set, the high from the clear side lights DS 18 and is inverted to a low by 50D02 (5-5, 8B) to initiate a START PUNCH signal from 53D02 (5-5, 8C). The START PUNCH signal energizes PUNCH relay (K1, 5-13, 4C). When K1 is energized, it completes a 115-VAC, 60-Hz path to punch input A3A2J2-2.

3-188. SET PUNCH READY F/F. The high from the clear side of PUNCH F/F 0XD02 (5-5, 5C) removes the low when CLR PUNCH RDY signal from the clear side input of PUNCH READY F/F 0XE01 (5-2, 4B) and the low when EN SET PUNCH RDY signal from the set side of 0XD02 (5-5, 5C) is used as a partial enable for setting 0XE01 (5-2, 4B).

3-189. PUNCH F/F 0XD02 (5-5, 5C) set produces a high from the clear side to input pin 6 of 50D02 (5-5, 8B), causing a low at output pin 13. The low from 50D02 (5-5, 8B) is applied to pin 15 of time delay 51D00 (5-5, 7B). Time delay

51D00 (5-5, 7B) outputs a high for 2 seconds, at which time the delay expires and the output goes low. The high from time delay 51D00 (5-5, 7B) is inverted to a low by 51D01 (5-5, 7C) to start time delay 52D02 (5-5, 7C). For 0.5 seconds, (5-5, 7C) will continue to output a low allowing the punch to get up to speed. When the delay expires, the output will go high and remain high until time delay 51D00 (5-5, 7B) expires. The high from time delay 52D02 (5-5, 7C) is inverted to a low by 54D02 (5-5, 7D). This produces the low when EN SET RDY signal, which is applied to the PUNCH F/F OXE01 (5-2, 4B) as the final enable to the set side. Two seconds after a low is applied to the input of 51D00 (5-5, 7B) the delay expires and the output of time delay 52D02 (5-5, 7C) goes low. The low from 52D02 (5-5, 7C) is inverted to a high by 54D02 (5-5, 7C), which drops the low when EN SET RDY signal to the PUNCH READY F/F OXE01 (5-5, 4B).

3-190. Clear Output Register. Since TAPE FEED F/F OXE00 (5-2, 4C) is clear at this time, the low from its clear side partially enables gate 53E00 (5-2, 6D). Time delay 51E00 (5-2, 3C) is normally outputting a low which further enables 53E00 (5-2, 3C). Gate 53E00 (5-2, 3C), which is present at all times except when ENABLE PRINT F/F OXE02 (5-2, 5C) is set. Enabling 53E00 (5-2, 3C) produces a high output which is inverted by 57E00 (5-2, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 (5-11, 8B) is amplified by 30G00 (5-11, 8B) and used to clear the output register flip-flops (figures 5-11 and 5-12).

3-191. Set PRINT F/F and Start Printer Motor. Depressing PRINT indicator switch (DS 24, 5-6, 7C) sets PRINT F/F OXD01 (5-6, 7C). With OXD01 (5-6, 7C) set, the high from its clear side lights DS 24 and is inverted to a low by 50D01 (5-6, 8B) to initiate a START PRINTER signal from 53D01 (5-6, 8C). The START PRINTER signal energizes PRINTER relay (K2, 5-13, 4C). When K2 is energized, it completes a 115-VAC, 60-Hz path to keyboard/printer input A7P1-Z and starts the printer motor.

3-192. Set PRINTER READY F/F. The low from the set side of PRINT F/F OXD01 (5-6, 7C) is inverted to a high by 55D01, removing the low when CLR PRINT RDY signal line from the clear side of PRINTER READY F/F OXE03 (5-2, 6B). The low when PRINTER RDY from the set side of OXD01 (5-6, 7C) partially enables OXE03 (5-2, 8B). The low from 50D01 (5-6, 8B) occurs when OXD01 (5-6, 7C) is set and enables time delay 52D01 (5-6, 7C) which produces a high output after a 0.5 second delay. The 52D01 (5-6, 7C) output is inverted by 54D01 to produce a low when EN SET PRINTER READY signal delayed 0.5 seconds from initiation of printer operation. This delayed signal is used as the final enable for setting OXE03 (5-2, 6B).

3-193. Stop Tape and Gate Data to Input Register. When a sprocket pulse is detected, 20F01 (5-6, 4B) produces a high output which is used to disable gate 41F01 (5-4, 4C). With 41F01 (5-4, 4C) disabled, its low output fully enables 42F01 (5-4, 4D) producing a high to disable 43F01 (5-4, 3C). When 43F01 is disabled, its low output is applied to 44F01 (5-4, 3C) to remove the ADVANCE TAPE signal to the tape reader. The low from 43F01 (5-4, 3C) also fully enables gate 50F00 (5-4, 3D) to produce a high output which is used to disable 50F04 (5-4, 7D) and remove the low when CLEAR INPUT REG signal to the input registers. The high from 20F01 (5-4, 4B) is also inverted to become a low when EN DATA INPUT REG signal. This signal, along with the low when DATA TO INPUT signal from 31D00 (5-6, 4C), enables 17I00 (5-9, 7B). The low when READER INPUT REG from 17I00 (5-9, 7B) gates data from the reader into the input register flip-flops (figures 5-9 and 5-10).

3-194. Set OFF-LINE READ F/F and/or OFF-LINE READ ONE F/F. Placing the READ ONE-READ switch (S3, 5-3, 5B) in the READ position sets OFF-LINE READ F/F 0XE05 (5-3, 4B). The low from the set side output of 0XE05 (5-3, 4B) partially enables the set side of OFF-LINE READ ONE F/F 0XE04 (5-3, 6B). The set side is fully enabled by the low when EN SET OFF-LINE READ ONE F/F signal from the 71H21 (5-8, 3C), which is present at all times when the serializer is inactive.

3-195. Simulate Output Acknowledge. The low from the set side of OFF-LINE READ ONE F/F 0XE04 (5-3, 6B) partially enables gate 50E04 (5-3, 5C). With READ ONE-READ switch (S3) in the READ position, the high from S3-3 is inverted to a low by 49E04 (5-3, 5C) to further enable 50E04 (5-3, 5C). Gate 50E04 (5-3, 5C) is fully enabled by the low from S4-2 (5-3, 4C), which is present during all off-line operations. With 50E04 (5-3, 5C) enabled, its high output simulates an output acknowledge signal.

3-196. Set TAPE FEED F/F and Remove Clear from Output Register. The high from 50E04 (5-3, 5C) is inverted by 51E04 (5-3, 3C) to partially enable 53E04 (5-3, 3D). The low from 51E04 (5-3, 3C), which allows 53E04 (5-3, 3D) to be fully enabled for 2µsec GATE OUTPUT DATA signal which is used to partially enable setting TAPE FEED F/F 0XE00 (5-2, 4C). TAPE FEED F/F 01E00 (5-2, 4C) is fully enabled at this time due to the low from PUNCH READY F/F 0XE01 (5-2, 4B), which was previously set. The high output from 0XE00 (5-2, 4C) lights TAPE FEED indicator switch (DS 20) and disables 53E00 (5-2, 6C). The low from 53E00 (5-2, 6C) is inverted by 57E00 (5-2, 8C), removing the low when CLR OUTPUT REG signal from its output line.

3-197. Gate Input Register to Output Register. The 2µsec low when GATE OUTPUT DATA signal from 53E04 (5-3, 3D) is also used to fully enable 18G00 (5-11, 7B) since 17G00 (5-11, 8B) is outputting a low enabling signal during all off-line operations. The low from 18G00 (5-11, 7B) gates all data from the input register flip-flops (figures 5-9 and 5-10) into their respective output register flip-flops (figures 5-11 and 5-12).

3-198. Set ENABLE PRINT F/F, Initiate Serializer and CLEAR SERIALIZER RDY F/F. With PRINTER READY F/F 0XE03 (5-2, 6B) set, its low output partially enables the set side of ENABLE PRINT F/F 0XE02 (5-2, 5C). When the 2µsec low when GATE OUTPUT DATA signal from 53E04 (5-3, 3D) occurs as the result of a simulated output acknowledge, the set side of 0XE02 (5-2, 5C) is fully enabled and the flip-flop is set. The high from its clear side is inverted by 51E02 (5-2, 6B) and reinverted by 52E02 (5-2, 6C) to disable 53E00 (5-2, 6D) preventing the low when CLEAR OUTPUT REG from 57E00 (5-2, 8C) during printer operations. The low from the set side output of 0XE02 (5-2, 5C) fully enables 50E06 (5-2, 5C) since its other enable is low at all times except during keyboard operations. With 50E06 (5-2, 5C) enabled, its high output is routed to figure 5-7 on the high when INIT SERIALIZER line. The high when INIT SERIALIZER signal is inverted by 71H00 (5-7, 8C) to partially enable 71H01 (5-7, 8C) and the sequence of events described in paragraph 3-76 occurs.

3-199. Gate Data to Punch and Clear TAPE FEED F/F. With TAPE FEED F/F 0XE00 (5-2, 4C) set, its high output partially enables 50E00 (5-2, 6D). When the next flywheel pulse from the punch is sensed by 29E00 (5-2, 3B), its high output fully enables 50E00 (5-2, 3B), whose negative output is inverted by 49E00 (5-2, 3C) and stretched into a 4 msec positive gate by the time delay circuit 51E00 (5-2, 3C). This gate is applied as a further disabling signal for gate 53E00 (5-2, 6D), which was initially disabled when 0XE00 (5-2, 4C) was set.

The gate from 51E00 (5-2, 3C) is also inverted by 52E00 (5-2, 3D) and amplified by 49G00 (5-11, 3C) to become the low when DATA PUNCH signal, which is used to partially enable gates 50G00 through 50G07 (figures 5-11 and 5-12). These gates will be fully enabled or disabled in accordance with the bit configuration stored in output register flip-flops 0XG00 (5-11) through 0XG07 (5-12), respectively. When a particular flip-flop is set (contains a binary 1), its associated gate will be enabled. Conversely, when a particular flip-flop is clear (contains a binary 0), its respective gate will be disabled. The 50G00 (5-11, 3C) through 50G07 (5-12, 7C) outputs are converted to punch logic levels by 51G00 (5-11, 3C) through 50G07 (5-12, 7C), respectively, and transmitted to the punch as PUNCH DATA signals.

3-200. Feed Hole Signal to Punch. The low when DATA to PUNCH signal from 49G00 (5-11, 3C) is amplified through 40G06 (5-12, 8C) to enable 41G06 (5-12, 8C), whose output is transmitted to the punch as the FEED HOLE signal.

3-201. Clear TAPE FEED F/F. The low from 49G00 (5-11, 3C) is also routed to figure 5-2 as the low when EN CLR TAPE FEED F/F signal and used to partially enable gate 30E00 (5-2, 3B). At the end of the flywheel pulse, the 29E00 (5-2, 3B) output goes low and 30E00 (5-2, 3B) is fully enabled. The low from 30E00 (5-2, 3B) is fully enabled. The low from 30E00 (5-2, 3B) clears TAPE FEED F/F 0XE00 (5-2, 4C), extinguishing the TAPE FEED indicator switch (DS 20), disabling 50E00 (5-2, 3B), and partially enabling gate 53E00 (5-2, 6D).

3-202. Basic Serializer Operations. Refer to serializer timing gates and pulses as illustrated in figure 3-51 during the following discussion of serializer delay line operations. When 71H01 (5-7, 7C) is enabled, its 2μsec low output is stretched to 9.09 msec by 71H02 (5-7, 7D) and inverted by 71H03 (5-7, 7A). When the positive pulse from 71H03 (5-7, 7A) terminates (goes negative), 71H04 (5-7, 7B) will produce a negative 9.09 msec output pulse which is delayed 9.09 msec from initiation of the serializer. This pulse is inverted by 71H05 (5-7, 6B). When the positive pulse from 71H05 (5-7, 6B) terminates, 71H06 (5-7, 6B) will produce a negative 9.09 msec output pulse delayed 18.18 msec from initiation of the serializer. In this manner, the 9.09 msec negative pulse travels down the delay line consisting of circuits 71H03 (5-7, 7A) through 71H20 (5-8, 3C). Each inverter-delay circuit stage delays the pulse an additional 9.09 msec.

NOTE

Each delay stage consists of an input inverter (2070 card) and a time delay (2821 card). The inverters have odd numbered designations and the time delays are designated by even numbers.

3-203. Generation of DATA to PRINTER Signals for Start, Bits 0 Through 6, Parity, and Stop. Refer to paragraph 3-78.

3-204. Set SERIALIZER RDY F/F and Clear ENABLE PRINT F/F. The output of time delay 71H20 (5-8, 3B) is a negative 18.18 msec pulse delayed 81.81 msec from initiation of the serializer (see figure 3-51). This low sets SERIALIZER RDY F/F 0XH00 (5-8, 3C) and clears ENABLE PRINT F/F 0XE02. The SERIAL CONVERTER READY signal from the set side of 0XH00 (5-8, 5C) partially enables 71H01 (5-7, 7C) in preparation for the next initiation of the serializer.

3-205. Clear Output Register. With ENABLE PRINT F/F 0XE02 (5-2, 5C) cleared, the high from its set side fully disables 50E06, (5-2, 5C), since the high when KB enable for this gate contains a low at all times except during keyboard operations. The low from 50E06 (5-2, 5C) is inverted by 51E02 (5-2, 5B) and

reinverted by 52E02 (5-2, 6B) to partially enable gate 53E00 (5-2, 6C). Since TAPE FEED F/F 0XE00 (5-2, 4C) is clear, the low from its clear side further enables 53E00 (5-2, 6C). Gate 53E00 (5-2, 6C) is fully enabled by the low from time delay 51E00 (5-2, 3C), which is present at all times except during certain punch operations. The high from 53E00 (5-2, 6D) is inverted by 57E00 (5-2, 8C) and routed as the low when CLEAR OUTPUT REG signal to inverter 29G00 (5-11, 8B). The high from 29G00 (5-11, 8B) is amplified by 30G00 and used to clear the output register flip-flops (figures 5-11 and 5-12).

3-206. Simulate Input Acknowledge. With 53E00 (5-2, 6C) enabled, its high output partially enables 54E00 (5-2, 6C). Since PUNCH READY F/F 0XE01 (5-2, 4B) and PRINTER READY F/F 0XE03 (5-2, 6B) are both set, the lows from their set sides enable 50E01 (5-2, 7B) whose high output provides the final enable for 54E00 (5-2, 6C). The low when SIM INPUT ACK from 54E00 enables one side of 25F01 (5-4, 6C) since the low when OFF-LINE enable is present during all off-line operations. The high from 25F01 (5-4, 6C) is inverted by 26F01 (5-4, 5A) and used as a partial enable for 28F01 (5-4, 5B). The low from 26F01 (5-4, 5A) is routed through 27F01 (5-4, 5B), which allows 28F01 (5-4, 5B) to be fully enabled for 2µsec. The 28F01 (5-4, 5B) output is a 2µsec positive pulse whose leading edge is coincident with the simulated input acknowledge, which occurs 81.81 msec after initiation of the serializer.

3-207. Clear OFF-LINE READ ONE F/F. The output from 71H21 (5-8, 3C) is an 18.18 msec high gate delayed 81.81 msec from initiation of the serializer. This gate is routed to figure 5-3 on the low when EN SET OFF-LINE READ ONE F/F signal line as one of the enables for OFF-LINE READ ONE F/F 0XE04 (5-3, 6B). The other enable is the low from the set side output of OFF-LINE READ F/F 0XE05 (5-3, 5B). The 2µsec high when CLR OFF-LINE READ ONE F/F from 28F01 (5-4, 5B) is inverted to a low by 30E04 (5-3, 6B). Since this pulse occurs while the positive 18.18 msec gate is disabling the set side of 0XE04 (5-3, 6B), the flip-flop will be cleared during this time. However, at the end of the 18.18 msec positive gate (99.99 msec after initiation of the serializer), the set side of 0XE04 (5-3, 6B) will again be enabled and the flip-flop will set. When 0XE04 (5-3, 6B) sets, the cycle repeats from paragraph 3-193 until the reader operation is terminated.

3-208. Termination of Reader Operations. Reader operations may be terminated by the following methods:

a. Automatic termination when the tape is completely read.

b. Depressing the START READ CLEAR and PRINT CLEAR switches (S5 and S10, figure 5-6) and the PUNCH CLEAR switch (S7, 5-5, 5D).

c. Momentarily setting the READ/READ ONE switch (S3, 5-3, 5B) to the READ ONE position.

d. Depressing MASTER CLEAR switch (S1 5-3, 7B).

NOTE

If the READ ONE switch (5-3, 5B) is depressed, OFF-LINE READ F/F 0XE05 (5-3, 4B) does not set and its high output disables the gate used for automatically setting OFF-LINE READ ONE F/F 0XE04 (5-3, 6B). However, depressing S3 sets 0XE04 (5-3, 6B) during any read operation, causing a simulated output acknowledge, which gates the input register to the output register. Therefore, only one frame is gated every time the READ ONE switch is depressed.