NAVSEA OP 3514 (PMS/SMS) VOLUME 2

PART 1
FIRST REVISION
CHANGE 7

DIGITAL COMPUTER MK 152 SERIES

TROUBLE ISOLATION

THIS PUBLICATION SUPERSEDES OP 3514 (PMS/SMS)
DATED 1 JANUARY 1973

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CHANGE RECORD

CHANGE NO.	DATE	TITLE AND/OR BRIEF DESCRIPTION	SIGNATURE OF VALIDATING OFFICER
7	12 JUNE 91	REPLACE PGM-241 WITH PGM-249A	Blaine Neff
3	3 Jan 91	Page 7-89, 7-90, 7-97, 7-98	DSZ Dion
5	1 APR 86	Change 5 dated 1 APR 75	ET2 Schmidt

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DEPARTMENT OF THE NAVY
NAVAL SEA SYSTEMS COMMAND
WASHINGTON, D.C. 20360

NAVSEA OP 3514 (PMS/SMS)
VOLUME 2 FIRST REVISION CHANGE 5

DIGITAL COMPUTER MK 152 SERIES
TROUBLE ISOLATION

1 April 1975

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PUBLISHED BY DIRECTION OF
COMMANDER, NAVAL SEA SYSTEMS COMMAND

After the attached enclosures have been inserted, record this CHANGE on the change record sheet.

1. The attached enclosures incorporate changes resulting from: ORDALTS 30023, 8339, 8286, 8409 and 8490; FBRs S-2189, S-1942, S-1751, S-1816, S-1539, and S-1378; CONARs and other miscellaneous sources.

2. Changes to other volumes of the manual associated with this change are: Volume 1 Change 5.

3. All holders should incorporate the attached enclosures into the technical manual in numerical sequence upon receipt.

4. Except as indicated, remove the following pages and replace with new change pages attached:

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xi and xii	xi and xii
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xxiii and xxiv	xxiii and xxiv
7-47 thru 7-50	7-47 thru 7-50
7-55 thru 7-60	7-55 thru 7-60
7-89 and 7-90	7-89 and 7-90
PART 2	
Covers and backbone	Covers and backbone
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8-477 thru 8-540	8-477 thru 8-540BB
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PART 3	
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FOREWORD

NAVSEA OP 3514 (PMS/SMS) First Revision physically and functionally describes the Digital Computer Mk 152 Series and provides all other information required by shipboard personnel for operation, installation, and maintenance of the equipment.

OP 3514 (PMS/SMS) is one of a family of Ordnance Publications (OPs) which provide comprehensive coverage of all modifications of Digital Computer Mk 152 and associated peripheral equipments. These manuals include the following:

Manual	Nomenclature of Equipment
OP 3514 (PMS/SMS) First Revision	Digital Computer Mk 152 Series
OP 3515 (PMS/SMS)	Input/Output Console Mk 77 Series
OP 3516 (PMS/SMS)	Digital Data Recorder Mk 19 Series
OP 3517 (PMS/SMS)	Control Panel Mk 298 Series
OP 3518 (PMS/SMS)	Motor Generator Set Mk 9 Series
OP 4245 (PMS/SMS)	Input/Output Console Mk 95 Series

Although not included in the foregoing list, a Signal Data Converter (SDC) is an essential part of any digital Fire Control System (FCS) which employs component parts originally designed for analog operation. The TARTAR, TALOS, and TERRIER weapon systems use SDCs Mk 72, Mk 66, and Mk 75, respectively. Gun Fire Control System (GFCS) Mk 86 uses SDC Mk 69/Mk 70 and Signal Data Translator (SDT) Mk 1 for data conversion.

The digital computer complex equipment configuration found on various gun and guided missile ships depends principally on the shipboard weapons system(s). While other factors can influence the actual configuration on board a particular ship, the following equipments are generally utilized with the missile/gun systems indicated:

Equipment	TARTAR	TERRIER	TALOS	GFCS Mk 86
Digital Computer	Mk 152	Mk 152	Mk 152	Mk 152
I/O Console	Mk 77	Mk 77	Mk 77	Mk 77
I/O Console	Mk 95	-------	-------	-------
Digital Data Recorder	Mk 19	Mk 19	Mk 19	-------
Control Panel	Mk 298	Mk 298	Mk 298	-------
Motor Generator Set	Mk 9	Mk 9	Mk 9	-------
Signal Data Converter	Mk 72	Mk 75	Mk 66	Mk 69/Mk 70
Signal Data Translator	-------	-------	-------	SDT Mk 1

This manual is applicable to Digital Computers Mk 152 Series configured as follows:

MOD NO.	IL NUMBER	UNIVAC NUMBER	MODULES (DRAWERS)	MEMORY SIZE	I/O CHANNELS
0	2652595	7049747-00	3(6)	32K	16 slow interface
1	2525383	7049747-05	2(4)	32K	8 slow interface
2	2536007	7049747-08	3(6)	32K	8 slow interface 8 fast interface
3	2687278	7049747-11	3(6)	40K	16 slow interface
4	2923042	7049747-13	3(6)	40K	8 slow interface 8 fast interface
5	3140291	7049747-14	2(4)	48K	8 slow interface

This publication consists of three volumes structured as follows:

VOLUME 1 - Description, Operation, and Maintenance
- Chapter 1. Introduction
- Chapter 2. Description
  - Section 2-1. Physical Description
  - Section 2-2. General Functional Description
  - Section 2-3. Detailed Functional Description
- Chapter 3. Operation
- Chapter 4. Installation
- Chapter 5. Maintenance

VOLUME 2 Part 1 - Trouble Isolation
- Chapter 6. Introduction
- Chapter 7. Supporting Maintenance Data
  - Section 7-1. General Troubleshooting Information
  - Section 7-2. Manual Troubleshooting
  - Section 7-3. Troubleshooting Charts
  - Section 7-4. Schematic Diagrams of Printed Circuit Cards

VOLUME 2 Part 2 and Part 2A-Trouble Isolation
- Chapter 8. Diagnostic Program

VOLUME 2 Part 3 - Trouble Isolation
- Chapter 9. Functional Schematics

VOLUME 3 - Parts List
- Chapter 10. Introduction
- Chapter 11. Replaceable Parts List

Ships, training activities, supply points, depots, Naval shipyards and supervisors of shipbuilding are requested to arrange for the maximum practical use and evaluation of NAVSEA technical manuals. All errors, omissions, discrepancies, and suggestions for improvements to NAVSEA technical manuals shall be reported to the Naval Sea Data Support Activity (NSDSA), Naval Ship Weapon Systems Engineering Station (Code 5740), Port Hueneme, CA 93043 on NAVSEA Technical Manual Deficiency/Evaluation Report,

NAVSEA Form 5600/2. To facilitate such reporting, three copies of Form NAVSEA 5600/2 are included at the end of each unclassified bound part of this technical manual being changed. All feedback comments will be thoroughly investigated and originators will be advised of action resulting therefrom. Extra copies of Form NAVSEA 5600/2 may be requisitioned from the Naval Publications and Forms Center (NPFC), Philadelphia, PA 19120.

The technical content of the manual covers Digital Computer Mk 152 Series as modified by ORDALTs 7732, 7889, 8008, 8331 Change 1, 30023, 8339, 8286, 8409, 8490, and 30094.

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SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all time observe all safety regulations. Do not replace components or make adjustments inside the equipment with the high voltage supply turned on. Under certain conditions, dangerous potentials may exist when the power control is in the off position, due to charges retained by capacitors. To avoid casualties, always remove power and discharge and ground a circuit before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter an enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation. Such information may be obtained from the Bureau of Medicine and Surgery.

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CHAPTER 6

INTRODUCTION

6-1. PURPOSE

6-2. This chapter briefly explains the planned maintenance philosophy in current usage aboard naval vessels and its applicability to the task of isolating malfunctions of the Digital Computer Mk 152 Series.

6-3. MAINTENANCE PHILOSOPHY. The Planned Maintenance System for Surface Missile Systems (PMS/SMS) is defined as a systematic approach to the accomplishment of work that will reduce the maintenance of complex equipment to simple, easily identified and managed procedures; define the minimum requirements of planned maintenance; schedule and control the performance of tasks; describe the methods, materials, tools, and personnel required; and provide for the prevention or detection of impending malfunctions.

6-4. The PMS/SMS concept involves Daily System Operability Tests (DSOT's) and/or supplemental system tests and scheduled maintenance. System tests determine the overall operability of a system, whereas scheduled maintenance is performed on individual equipment of a system to detect possible trouble areas and maintain a high degree of readiness. General guidelines for implementing PMS/SMS are contained in OPNAVINST 4790.4, ships Maintenance and Material Management (3M) Manual. PMS/SMS is a system-to-subsystem-to-equipment approach to overall maintenance, including fault isolation procedures and diagrams keyed to scheduled and corrective maintenance procedures. In addition to fulfilling the Chief of Naval Material requirements for preventive/scheduled Maintenance Requirements Cards (MRC's), PMS/SMS fulfills training requirements of the Chief of Naval Personnel, standardizes the format of SMS technical manuals, and eliminates from the manuals materials which are redundant to shipboard maintenance requirement procedures. PMS/SMS maintenance materials provide the most direct path to fault and trouble isolation procedures, which lead to appropriate alignment/adjustment or repair/replacement corrective maintenance procedures.

6-5. Scheduled maintenance which consists of all necessary preventive maintenance actions, is performed at the organizational (shipboard) level as part of PMS/SMS. It provides for planning, scheduling, and managing resources (men, material, and time) in performance of preventive maintenance actions intended to ensure that equipment operates within design standards and meets established readiness criteria. It defines uniform maintenance standards based on engineering experience, and provides simplified procedures and management techniques for job accomplishment. When installed, planned maintenance supersedes any existing preventive maintenance programs and conflicting technical directives for equipment covered. Equipment not covered under planned maintenance is to be maintained in accordance with existing procedures. During shipyard overhaul periods, planned maintenance tasks not affected by shipyard work shall continue to be accomplished by shipboard personnel.

6-6. Primary documentation utilized in PMS/SMS includes the Maintenance Index Page (MIP) and the Maintenance Requirement Card (MRC) located in the applicable equipment work centers. Facsimiles of the MIP's and MRC's have been published in the past in NAVSEA technical manuals. Those facsimilies are no longer being published within the technical manual structure of PMS/SMS OP's. However, Chapter 5 of this OP provides limited information on preventive and corrective maintenance procedures appearing on MRC's that are applicable to the Digital Computer Mk 152 Series.

6-7. Maintenance Index Page. The MIP is tailored to a specific equipment and indexes a set of MRC's for the installed equipment. The MIP for each set of MRC's will provide the following:

1. The title of the equipment concerned.
2. A Systems Command MRC Control Number to identify MRC's in library stock.
3. A brief description of each maintenance requirement.
4. The maintenance periodicity code.
5. The skill level required to perform each maintenance requirement.
6. An average time required to perform each maintenance requirement.
7. Any related maintenance action to be scheduled for simultaneous accomplishment.
8. Notations included as management aids when available and needed for selective maintenance scheduling.

6-8. Maintenance Requirement Card. The MRC defines the maintenance task in terms that allow all concerned to know that is required, who is qualified to perform the task how often, and the manhours required. The card standardizes the procedure of doing a job in the best known way, expedites accomplishment of the task by stating the tools and materials needed and the safety precautions to be observed, and provides a concise and complete work instruction to the equipment maintenance man in the work space. It is intended that the MRC be all inclusive, and reference to other publications will not be required since availability of outside references aboard ship, other than instructions posted on or near the equipment, cannot be assured. The text is factual, specific, concise, and easily readable, and instructions are presented in a step-by-step format in logical sequence for accomplishing the maintenance procedure in the most rapid and accurate manner possible.

6-9. TROUBLESHOOTING DATA. Troubleshooting information contained in this volume includes or references all tests and procedures for detecting and isolating computer casualties. Figure 6-1 is a block diagram of all available tests and includes OP volume number, OP part number, chapter or section number of the description, operating procedures, program listing and other pertinent data necessary for troubleshooting. When a malfunction is encountered in the computer, the diagnostic program is run and, if detection and isolation is successful, no other test needs to be run. However, if unsuccessful, the manual troubleshooting procedures should then be pursued. Included in the manual troubleshooting procedures are supporting maintenance data, troubleshooting charts, printed circuit (PC) cards, and the manual troubleshooting sections. The manual troubleshooting section is further divided into manual tests, program analysis and manual programing. The following maintenance plan briefly describes each of the blocks.

6-10. MAINTENANCE PLAN

6-11. DIAGNOSTIC PROGRAM. The basic tool for troubleshooting the Mk 152 computer is the diagnostic program. This program is broken down into two phases: malfunction detection and malfunction isolation. A description of the program is contained in volume 1, chapter 5. Volume 2 Part 2 contains a complete description of the sequence of diagnostic testing, malfunction isolation procedure, intermittent analysis, operating procedures, and malfunction isolation tables. Volume 2 Part 2A contains the diagnostic program listing.

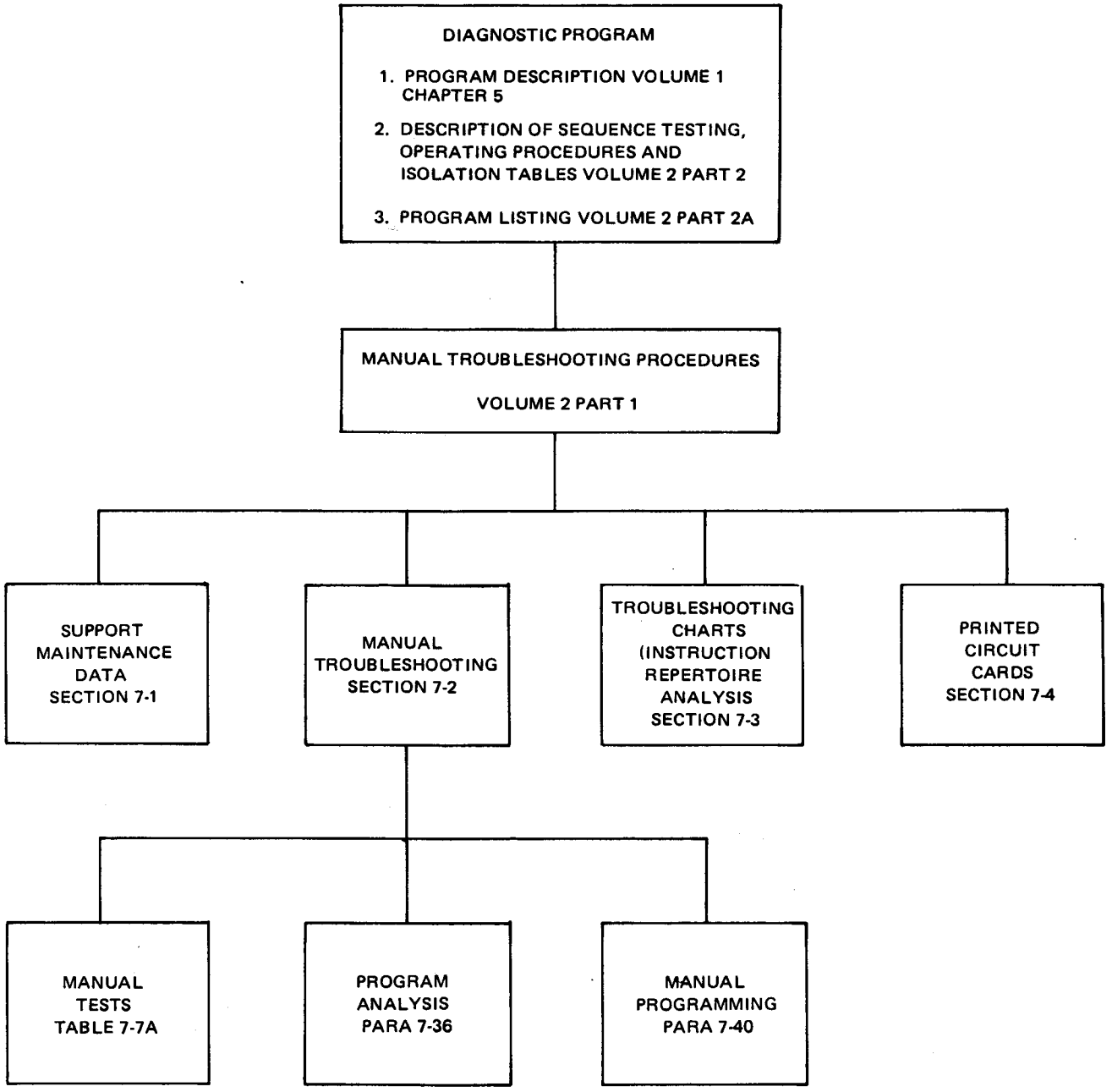

Figure 6-1 Available Troubleshooting Data

6-12. MANUAL TROUBLESHOOTING PROCEDURES. Manual troubleshooting procedures contain supporting maintenance data, manual troubleshooting section, troubleshooting charts, and PC cards.

6-13. MANUAL TROUBLESHOOTING SECTION. The manual troubleshooting section is divided into program analysis, manual programing, and manual tests.

1. PROGRAM ANALYSIS. Whenever the diagnostics program detects but fails to isolate the casualty, manual troubleshooting techniques must be used. One of the techniques is to analyze the program and determine what area of the program is failing. Section 7-2, paragraphs 7-36 and 7-44A, contains a detailed explanation of program analysis.

2. MANUAL PROGRAMING. When analyzing a program to determine the area of failure, the technician may find it necessary to write a small program and manually enter it into the computer to aid in trouble isolation. Section 7-2, paragraph 7-40, contains a detailed description for manual loading, manual reading, and a manual inspect-and-change routine.

3. MANUAL TESTS. As a further aid to isolating computer casualties, a series of manual tests are available to the technician. These tests include memory checks, voltage checks, maintenance turn-on procedures, timing checks, and all necessary adjustments to ensure an operational computer. Section 7-2 paragraph 7-35 and Table 7-7A lists and describes all available tests.

6-14. SUPPORTING MAINTENANCE DATA. Section 7-1 contains supporting maintenance data. Included in this section is a description of computer operation in various modes, a lamp and switch index, a list of test equipment and special tools, and other maintenance data of general interest.

6-15. TROUBLESHOOTING CHARTS. Section 7-3 provides a charted analysis of computer operation during execution of every instruction in its repertoire. Also included is a table that identifies allocated control memory and bootstrap address.

6-16. PRINTED CIRCUIT CARDS. Section 7-4 contains functional and schematic diagrams and gives a logic description of all PC cards used in the Mk 152 computer.

6-17. PREVENTIVE MAINTENANCE SCHEDULES. Preventive Maintenance (PM) is a term encompassing the procedures which computer operators and maintenance personnel perform to keep the equipment in optimal operating condition thereby preventing undue failures and maximizing productive use. These procedures must be performed at regularly scheduled intervals. The tests may also be run when a failure is suspected. The Maintenance Index Page for PM lists each applicable Maintenance Requirement Card and the frequency (periodicity) of performance required to maintain the computer in the best operating condition. If the need for adjustment or parts replacement becomes apparent during performance of scheduled maintenance, reference should be made to the appropriate corrective maintenance procedures.

6-18. UNSCHEDULED MAINTENANCE REQUIREMENTS. Unscheduled maintenance procedures are available on 5 by 8 Maintenance Cards (UMRC). These cards are listed on an Unscheduled Maintenance Index Page. Whenever required, cards are specially tailored to fit the specific configuration of an installation.

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Page 6-5 thru 6-8B deleted.

Individual points within a test block are identified by a two-coordinate system which uses letters from left to right and numbers from top to bottom. The first designator represents the particular test block on a given chassis. For example: TB2-B2 indicates test block 2, coordinates B and 2.

6-18. TROUBLESHOOTING MEMORY. Memory errors that occur in a logical pattern are generally caused by component failure, either in memory proper or in the associated logic circuitry. The source of error can be most readily isolated by use of the memory test program and by logical analysis. Random memory errors may indicate improperly adjusted memory-drive currents or read-strobe timing. No attempts should be made to adjust memory regulated voltages, drive currents, or strobe timing until all other possible sources of malfunction have been investigated and corrected. Refer to Chapter 7, Para 7-32, Manual Troubleshooting Procedures, for further information on troubleshooting memory casualties.

6-19. CONFIDENCE CHECK. The confidence programs consist of computer-controlled tests which may be performed to determine the functional capabilities of the computer. Procedures for running the diagnostic routines as a confidence test are on Maintenance Requirement Cards.

6-20. POWER CHECKS. Power checks are used to verify proper primary power and DC voltages in the power, logic, and memory drawers. The physical locations of these drawers are illustrated in Volume 1 figure 2-1. The main power supply contains an interlock switch which must be secured in the cabinet during voltage measurements. Actual procedures for conducting these power checks are available on MRC's.

6-21. PREVENTIVE MAINTENANCE SCHEDULES. Preventive Maintenance (PM) is a term encompassing the procedures which computer operators and maintenance personnel perform to keep the equipment in optimal operating condition thereby preventing undue failures and maximizing productive use. These procedures must be performed at regularly scheduled intervals. The tests may also be run when a failure is suspected. The Maintenance Index Page for PM lists each applicable Maintenance Requirement Card and the frequency (periodicity) of performance required to maintain the computer in the best operating condition. If the need for adjustment or parts replacement becomes apparent during performance of scheduled maintenance, reference should be made to the appropriate corrective maintenance procedures.

6-22. CORRECTIVE MAINTENANCE. Corrective maintenance procedures are now available on 5 by 8 inch Corrective Maintenance Cards (CMC's). These cards are listed on a Corrective Maintenance Index Page (CMIP). Whenever required, CMIP's are specially tailored to fit the specific configuration of an installation.

6-23. SAMPLE TROUBLESHOOTING PROBLEM.

6-24. TROUBLESHOOTING FLOW DIAGRAM. Whenever system testing indicates that an abnormal condition exists within the computer, a logical sequence of maintenance events should take place. This sequence of events is depicted in flow diagram form on figure 6-1. The flow diagram is the step-by-step procedure utilized to detect a malfunction, fault isolate to a defective module, remove and replace the faulty module, and run the diagnostic program to ensure that the malfunction has been corrected and the computer is again

operational. The following examples show how the diagnostic program is utilized to isolate malfunctions of the computer:

1. Example A. In conjunction with Digital Data Recorder Mk 19 Series, the computer is prepared for loading of the diagnostic program by performing the Maintenance Turn-On (MTO) procedure (refer to table 7-1). When attempting to load diagnostics utilizing procedures in paragraph 8-4 (refer to Volume 2 Part 2), it is determined that step 10 indications are incorrect indicating that CONTBASI failed to load. Step 10 then refers the operator to paragraph 8-5, short load procedure. The operator then proceeds with paragraphs 8-6 through 8-9. When performing paragraph 8-9, initiating load procedure, the indications for step 21 prove incorrect. This incorrect indication refers the operator to paragraph 8-71, load failures. The load failure test is successfully completed if the PROGRAM FAULT indicator is not lit and the program is not looped. Paragraph 8-71, step 2 then refers the operator to paragraph 8-89, load failure, nonloop/nonfault.

> Step 1 P Register equals 000517 which refers the operator to step 7. Computer indicator ID ACT is lit. Step 7b indicates that the following modules should be replaced:
>
> 3J27C
> 3J26A
> 7J03F
> 3J27D

When the specified modules have been replaced as directed, loading of the diagnostic program may be resumed. The preceding explanation is shown in tabular form in table 6-1 and flow diagram form in figure 6-1.

2. Example B. The computer is prepared for loading of the diagnostics by performing the Maintenance Turn-On procedure (refer to table 7-1). CONTBASI is loaded successfully utilizing procedures in paragraph 8-4. When CONTBASI is initiated it is noted that incorrect indications are recorded in step 11. These incorrect indications lead the operator to paragraph 8-188. The operator then performs steps 1 and 2 of paragraph 8-188 which lead to paragraph 8-189 and table 8-85. In step 1 the operator finds the value P=002005 in table 8-85. If there was more than one combination of AU, AL and C register given the operator would perform step 2. When steps 1 and 2 are complete, indications are that the following modules should be replaced: 3J02A and 7J02C. However, after these cards have been individually replaced and the diagnostics rerun, the same fault indications still exist. Step 3 of paragraph 8-189 then refers the operator to the Program Listing of CONTBASI. The operator finds the value of P in the listing and by looking back in the listing discovers he is in the ICEBERG subroutine of CONTBASI and the program was checking a FUNCTION 73 with B not equal to zero. The operator can now use manual troubleshooting procedures to find why a 73 instruction failed. The foregoing sample troubleshooting problem is illustrated in figure 6-1 and is shown in tabular form in table 6-2.

TABLE 6-1. SAMPLE A: LOAD FAILURE PROCEDURE

Test Program*	Step Failure	Remarks	Refer to Para. No.
8-4	10		8-5
8-5	None		8-6
8-6	None		8-7
8-7	None		8-8
8-8	None		8-9
8-9	21		8-71
8-70	2		8-89
8-89	1	P=000517	Step 7 of 8-89
	7b	Replace: 3J27C 3J26A 7J03F 3J27D	

TABLE 6-2. SAMPLE B: LOAD FAILURE PROCEDURE

Test Program*	Step Failure	Remarks	Refer to Para No.
8-4	11	P=002005 No Program Fault AU=000000 AL=400000 Program C=000000 Stop	8-188
8-188	None		8-189
8-189	2a	Replace: Does not 3J02A correct 7J02C fault.	Step 3 of 8-189
8-189 Step 3		Find P in Program Listing of CONTBASI Table 8-136 Function being tested f=73	Manual Trouble-shooting Procedures (Chapter 7-32)

* Refer to specified paragraphs of Chapter 8 in Volume 2 Part 2, Diagnostic Program, for test procedures.

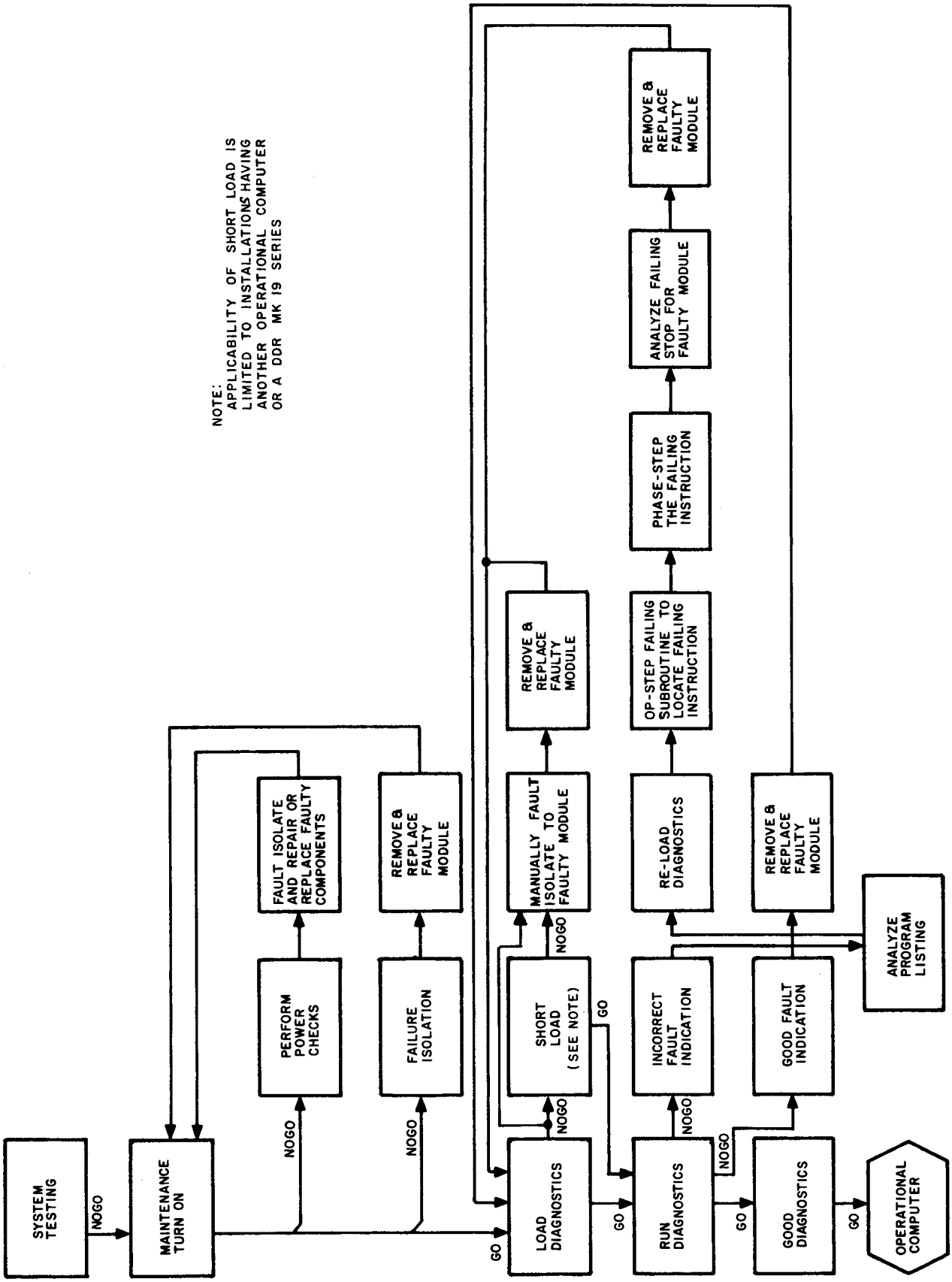

Figure 6-1. Troubleshooting Sequence, Flow Diagram

CHAPTER 7

SUPPORT MAINTENANCE DATA

Section 7-1. General Troubleshooting Information

7-1. SCOPE

7-2. This section contains supporting maintenance data including a Maintenance Turn-On procedure and a description of specific maintenance uses for front panel controls and indicators. Included in this section is any maintenance information considered useful in the task of isolating computer casualties to the level of replaceable printed circuit modules. A description of computer operation in various modes, a lamp and switch index, a recommended fault isolation module list, a comprehensive list of test equipment and special tools, and other maintenance data of general interest can be found in this section of the manual.

7-3. MAINTENANCE TURN-ON PROCEDURE.

7-4. The Maintenance Turn-On procedure (table 7-1) provides a manual means for checking computer power, indicators, switches, and front panel registers.

7-5. LAMP AND SWITCH INDEX.

7-6. The lamp and switch index (see table 7-2) is a comprehensive list which gives placarded nomenclature, reference designators, and figure references for each switch and/or indicator lamp which is physically located on any of the various computer control/indicators.

7-6A. RECOMMENDED FAULT ISOLATION MODULE LIST.

7-6B. Recommended fault isolation modules are listed in table 7-2A. The list is recommended for installations having a fault isolation cabinet. A quantity of one fault isolation module is recommended for each type of module.

7-7. MAINTENANCE CONTROLS AND INDICATORS.

7-8. In order to enhance its usefulness, the lamp and switch index is subdivided into several separate sections including: the Input/Output Panel (A1) or (A8), Control Panel 1 (A2), Control Panel 2 (A4), the Power Control Panel (A5), and a miscellaneous section. Maintenance controls and indicators located on each control/indicator panel are illustrated in figures 7-1 through 7-4. Reference should be made to Chapter 3, Operation, for detailed information concerning the exact functional purpose served by each control/indicator during operation of the computer.

7-9. MAINTENANCE EQUIPMENT.

7-10. TEST EQUIPMENT AND SPECIAL TOOLS. Test equipment and special tools recommended for use in computer maintenance are listed in tables 7-3 and 7-4. None of the listed items is supplied with the computer at delivery.

7-11. Combination Tool. A special combination tool (figure 7-5) is furnished with the computer for use in performing maintenance, service, and repair procedures.

7-12. Module Extender. A module extender (manufacturer's part no. 7009452-00) is used for extension of Type A printed circuit modules during tests. Figure 7-6 is a schematic diagram depicting the wiring scheme of the extender. Maintenance technicians should remember that Type B (memory) printed circuit modules must never be extended.

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE

Step	Procedure	Observation	Reference*
	A. Preliminary		
1.	Verify that the appropriate switches have been set to provide the following primary power to the computer: 115 VAC 3 Phase 400 Hz		
2.	At the computer, verify that the following switches are positioned as indicated: Power Panel (A5) Switch — Position POWER — Neutral DISC ALARM-RESET ALARM — Neutral BATTLE SHORT — OFF INDICATE-OFF-INDICATE/SET — INDICATE/SET Control Panel 1 (A2) Switch — Position I/O CLEAR-MASTER CLEAR — Neutral SEQ STEP-STOP — Neutral RESTART-SPEED CONTROL — Approx. CTR. RESTART-START STEP — Neutral FUNCTION REPEAT — Down PHASE REPEAT — Down AUTO RECOVERY — Down DISC ADV P — Down		

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (cont'd)

Step	Procedure	Observation	Reference*
	Behind Front Panel Switch — Position CLOCK-NARROW-NORMAL (ODD) — NORMAL CLOCK NARROW-NORMAL (EVEN) — NORMAL Control Panel 2 (A4) Switch — Position PROGRAM STOPS — Down PROGRAM SKIPS — Down EXT SYNC DISC — Up RTC DISC — Up BOOTSTRAP MODE — NDRO B. Local Turn-On		
3.	At the computer power panel (A5), momentarily position the POWER switch to the ON position.	POWER and LOCAL CONTROL lamps are lighted. Blowers are operating. Running time meter is running.	Plates P-176 and P-177.
4.	At control panel 1 (A2), verify status of ABNORMAL CONDITION indicators.	TEMP and VOLTAGE FAULT lamps are not lighted.	Plates P-176, P-177 and P-121.
5.	Momentarily push I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR,	AU, AL, ICR, SR, FII, FUNCTION CODE, P, CO, CE, SI, ZI, B and K register lamps are not lighted. SEQ DES I, I/O TRANSLATOR FUNCTION bits 0 and 1, and	Plate P-7

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (Cont'd)

Step	Procedure	Observation	Reference*
		I/O TRANSLATOR CHANNEL bits 1 and 2 indicators are lighted.	
6.	At the power panel (A5), position BATTLE SHORT switch to the ON position.	BATTLE SHORT lamp is lighted.	Plate P-176.
7.	Position BATTLE SHORT switch to the OFF position.	BATTLE SHORT lamp is not lighted.	Plate P-176.
8.	At control panel 1 (A2) push LOAD MODE indicator switch if not already in LOAD Mode.	Observe following: a. LOAD MODE and SEQ DES I indicators are lighted and RUN MODE indicator is not lighted. b. S1 register indicates 000500_8. c. I/O TRANSLATOR FUNCTION indicates 3_8. d. I/O TRANSLATOR CHANNEL indicates 06_8. e. ALL TIMING indicators are dimly lighted except for indicator 52 which should not be lighted. f. All other computer indicators are not lighted (ignore Z_h register and phase lights).	Plates a. P-3, P-13 b. P-104, 105 c. P-51 d. P-51 e. P-8, 9, 10, 11 f. Refer to appropriate plate
9.	Push OP STEP MODE indicator/switch.	OP STEP MODE and TIMING 11 indicators are lighted. All other TIMING and MODE	P-3, P-8, 9, 10, 11

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (Cont'd)

Step	Procedure	Observation	Reference*
9. (Cont'd)		indicators are not lighted. Observe that no obvious changes in the computer status have taken place.	
10.	At the control panels indicated, push each register indicator/switch listed: Control Panel — Indicator Switch 1(A2) — AU, AL, ICR, SR, FII, FUNCTION CODE, P (A1) — CO, CE, S1 2(A4) — Z1, B, K	Associated indicator is lighted.	PLATES P-97, 98 P-99-100, P-39,P-39, P-40, P-40, P-102-103, P-71-72, P-71-72, P-104-105, P-111-113, P-48-120, P-37 respectively
11.	At control panel 1(A2), push RUN MODE indicator/switch	RUN MODE indicator is lighted and OP STEP MODE indicator is not lighted.	Plate P-3
12.	Momentarily position I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.	Indicators set in Step 10 are not lighted.	Plate P-7
13.	Push OP STEP MODE indicator/switch.	OP STEP MODE indicator is lighted and RUN MODE indicator is not lighted.	Plate P-3
14.	At power panel (A5), position INDICATE-OFF-INDICATE/SET switch to INDICATE.		
15.	Ensure each register indicator/switch listed in Step 10 cannot be set.	Corresponding register indicators are not lighted.	Plate P-176.

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (Cont'd)

Step	Procedure	Observation	Reference*
16.	At power panel (A5), position INDICATE-OFF-INDICATE/SET switch to INDICATE/SET.		
17.	At control panel 1(A2), push PHASE STEP MODE indicator/switch.	PHASE STEP MODE indicator is lighted and OP STEP MODE indicator is not lighted.	Plate P-3
18.	Push RUN MODE indicator/switch.	RUN MODE indicator is lighted, PHASE STEP MODE indicator is not lighted and all TIMING indicators except 52 are dimly lighted. Observe that no obvious changes in computer status have taken place.	Plate P-3 P-8-11
19.	Momentarily position I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.		
20.	Position FUNCTION REPEAT switch to the up position.		
21.	Manually enter 40_8 in FUNCTION CODE register.	FUNCTION CODE register should equal 40_8.	Plate P-40
22.	Momentarily position RESTART-START STEP switch to START STEP.	PROGRAM RUN lamp is lighted, PROGRAM FAULT lamp is not lighted and P register is advancing through all addresses.	Plates P-3, P-54, P-121, P-176

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (Cont'd)

Step	Procedure	Observation	Reference*
23.	Momentarily position SEQ STEP-STOP switch to STOP.	PROGRAM RUN lamp is not lighted.	Plates P-3 and P-121.
24.	Momentarily position I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.		
25.	Push the FUNCTION CODE register Clear switch. Enter 77_8 in the FUNCTION CODE register.	FUNCTION CODE register and FII indicators are not lighted and then FUNCTION CODE register contains 77_8.	Plate P-40
26.	Momentarily position RESTART-START STEP switch to START STEP.	PROGRAM FAULT indicator is lighted and Fault Horn is sounding.	Plates P-54, P-121 and P-176.
27.	Momentarily position SEQ STEP-STOP switch to STOP. Position I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.	PROGRAM FAULT indicator is not lighted and Fault Horn is not sounding.	Plates P-7, P-54, P-121 and P-176.
28.	Repeat Steps 25 through 27 entering 01_8 in the FUNCTION CODE register.	Fault conditions are generated and cleared for the 01_8 illegal instruction code.	Same as for FUNCTION CODE equal to 77_8 in MTO Steps 25 through 27.
29.	Repeat Steps 25 through 27 entering 00_8 in the FUNCTION CODE register.	Fault conditions are generated and cleared for the 00_8 illegal instruction code.	Same as for FUNCTION CODE equal to 77_8 in MTO Steps 25 through 27.
30.	Position FUNCTION REPEAT switch to down position.		

TABLE 7-1. MAINTENANCE TURN-ON PROCEDURE (Cont'd)

Step	Procedure	Observation	Reference*
31.	At power panel (A5), position INDICATE-OFF-INDICATE/SET switch to OFF.	All indicator lamps on I/O panel (A1), control panel 1 (A2) and control panel 2(A4) are not lighted.	Plate P-176.
32.	Position INDICATE-OFF-INDICATE/ SET switch to INDICATE/SET.		

* References are made to test procedures provided in specific paragraphs of Chapter 8 (Volume 2 Part 2) and to the Functional Schematics (Plates) contained in Chapter 9 (Volume 2 Part 3).

TABLE 7-2. LAMP AND SWITCH INDEX

INPUT/OUTPUT PANEL (A1A3) (FIGURE 7-1)		
Panel Nomenclature	Reference Designator	Plate Number*
C_O (00-17 bits)	DS2B thru DS2J, DS1B thru DS1J	P-71, P-72
C_E (00-17 bits)	DS4B thru DS4J, DS3B thru DS3J	P-71, P-72
CHAN PRI (CHAN 0-7)	DS5J thru DS12J	P-65
EI MON (CHAN 0-7)	DS5I thru DS12I	P-61, P-62, P-63, P-64
EF MON (CHAN 0-7)	DS5H thru DS12H	P-38
OD MON (CHAN 0-7)	DS5G thru DS12G	P-61, P-62, P-63, P-64
ID MON (CHAN 0-7)	DS5F thru DS12F	P-61, P-62, P-63, P-64
EF ACT (CHAN 0-7)	DS5E thru DS12E	P-61, P-62, P-63, P-64
OD ACT (CHAN 0-7)	DS5D thru DS12D	P-61, P-62, P-63, P-64
ID ACT (CHAN 0-7)	DS5C thru DS12C	P-61, P-62, P-63, P-64
EF/OD ACK (CHAN 0-7)	DS5B thru DS12B	P-68
ID ACK (CHAN 0-7)	DS5A thru DS12A	P-68
EF MODE (C_O, C_E)	DS2A, DS4A	P-68
FUNCTION PRIORITY EI (ODD/EVEN)	DS13H, DS14H	P-66
FUNCTION PRIORITY EF (ODD/EVEN)	DS13F, DS14F	P-66
FUNCTION PRIORITY OD (ODD/EVEN)	DS13D, DS14D	P-66
FUNCTION PRIORITY ID (ODD/EVEN)	DS13B, DS14B	P-66
CHANNEL INTER-COMPUTER/NORMAL (CHAN 0-7)	S1 thru S8	P-61, P-62, P-63, P-64
CHANNEL FUNCTION (CHAN 0, 1)	S10	P-67

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

INPUT/OUTPUT PANEL (A1A3) (FIGURE 7-1) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
CHANNEL FUNCTION (CHAN 2, 3)	S9	P-67
CHANNEL FUNCTION (CHAN 4, 5)	S12	P-67
CHANNEL FUNCTION (CHAN 6, 7)	S11	P-67
CONTROL PANEL 1 (A2A3) (FIGURE 7-2)		
AU (00-17 bits)	DS2B thru DS2J, DS1B thru DS1J	P-97, P-98
AU CLEAR	S1	P-20
AL (00-17 bits)	DS4B thru DS4J, DS3B thru DS3J	P-99, P-100
AL CLEAR	S2	P-20
ICR (0-2 bits)	DS5H thru DS5J	P-39
ICR CLEAR	S4	P-38
SR (0-3 bits)	DS5B thru DS5E	P-39
SR ACTIVE	DS5F	P-39
SR CLEAR	S3	P-38
SEQ DES (BI, W, RI, I, I/O I)	DS6D thru DS6H	P-12
SEQ DES (BII, WAIT, RII, INT, I/O II)	DS7D thru DS7H	P-12
SEQ DES CLEAR	S5	P-12
TIMING (11)	DS9J	P-8
TIMING (12)	DS9I	P-8
TIMING (13)	DS9H	P-8
TIMING (14)	DS9G	P-8

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

CONTROL PANEL 1 (A2A3) (FIGURE 7-2) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
TIMING (21)	DS9F	P-9
TIMING (22)	DS9E	P-9
TIMING (23)	DS9D	P-9
TIMING (24)	DS9C	P-9
TIMING (31)	DS8J	P-10
TIMING (32)	DS8I	P-10
TIMING (33)	DS8H	P-10
TIMING (34)	DS8G	P-10
TIMING (41)	DS8F	P-11
TIMING (42)	DS8E	P-11
TIMING (43)	DS8D	P-11
TIMING (44)	DS8C	P-11
TIMING (52)	DS8B	P-11
ABNORMAL CONDITION TEMP	DS10H	P-177
ABNORMAL CONDITION VOLTAGE FAULT	DS10D	P-121
FUNCTION CODE (0-5 bits)	DS11B thru DS11G	P-40
FII (FUNCTION CODE 6th bit)	DS11I	P-40
FUNCTION CODE CLEAR	S6	P-40
P (00-15 bits)	DS13B thru DS13J, DS12B thru DS12H	P-102, P-103
P CLEAR	S7	P-21
MODE (RUN, OP STEP, PHASE STEP, LOAD)	DS14A thru DS14D	P-3
PHASE (1)	DS14J	P-4

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

CONTROL PANEL 1 (A2A3) (FIGURE 7-2) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
PHASE (2)	DS14I	P-4
PHASE (3)	DS14H	P-4
PHASE (4)	DS14G	P-4
PHASE CLEAR	S8	P-4
I/O CLEAR/MASTER CLEAR	S11	P-7
SEQ STEP/STOP	S10	P-3
RESTART SPEED CONT	A3R1	P-3
RESTART/START STEP	S9	P-3
DISC ADV P	S12	P-35
AUTO RECOVERY	S13	P-3
PHASE REPEAT	S14	P-4
FUNCTION REPEAT	S15	P-40
CONTROL PANEL 2 (A4A3) (FIGURE 7-3)		
PROGRAM STOP (0-4, 5)	XDS2 thru XDS6, XDS1	P-31
PROGRAM STOP (0-4)	S1 thru S5	P-32
PROGRAM SKIP (0-4)	S6 thru S10	P-32
S_1 (00-15 bits)	DS2B thru DS2J, DS1B thru DS1H	P-104, P-105
S_1 CLEAR	S11	P-22
Z_1 (00-17 bits)	DS4B thru DS4J, DS3B thru DS3J	P-111, P-112, P-113
Z_1 CLEAR	S12	P-23
B (00-17 bits)	DS6B thru DS6J, DS5B thru DS5J	P-118, P-119, P-120
B CLEAR	S13	P-21

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

CONTROL PANEL 2 (A4A3) (FIGURE 7-3) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
K (0-5 bits)	DS7E thru DS7J	P-37
ADV P SEQ (0-2)	DS7A thru DS7C	P-35
INTERUPT (SYNC, RTC OVERFLOW, RTC MON, RESUME FAULT, INST FAULT)	DS8F thru DS8J	P-54
EXT SYNC DISC	S15	P-54
RTC SEQ	DS8C	P-34
RTC DISC	S14	P-34
I/O TRANSLATOR (ESI, DUAL, ESA, ACTIVE)	DS9E thru DS9H	P-50, P-52
FUNCTION (0, 1)	DS10H, DS10I	P-51
CHANNEL (0-3)	DS10D thru DS10G	P-50, P-51
CHANNEL CLEAR	S16	P-49
BOOTSTRAP NDRO/MAIN MEMORY	S17	P-107
MULT/DIV SEQ (0)	DS11I	P-36
MULT/DIV SEQ (1)	DS11H	P-36
MULT/DIV SEQ (2)	DS11G	P-36
MULT/DIV SEQ (3)	DS11F	P-36
MULT/DIV SEQ (4)	DS11E	P-36
MULT/DIV SEQ (5)	DS11D	P-36
MULT/DIV SEQ (6)	DS11C	P-36
POWER CONTROL PANEL (A5) (FIGURE 7-4)		
RUNNING TIME METER	M1	P-176
POWER ON/OFF	S4	P-176

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

POWER CONTROL PANEL (A5) (FIGURE 7-4) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
POWER	XDS7	P-176
LOCAL CONTROL	XDS6	P-176
PROGRAM RUN	XDS5	P-176
PROGRAM FAULT	XDS4	P-176
DISC ALARM/RESET ALARM	S3	P-176
ABNORMAL CONDITION	XDS3	P-176
BATTLE SHORT ON/OFF	S2	P-176
BATTLE SHORT	XDS2	P-176
MARGINAL CHECK	XDS1	P-176
INDICATE-OFF-INDICATE/SET	S1	P-176
FAULT HORN	LS1	P-176
INPUT/OUTPUT PANEL (A8A3) (MOD'S 0, 2, 3, 4 ONLY) (FIGURE 7-1)		
C_O (00-17 bits)	DS2B thru DS2J, DS1B thru DS1J	P-71, P-72
C_E (00-17 bits)	DS4B thru DS4J, DS3B thru DS3J	P-71, P-72
CHAN PRI (CHAN 0-7)	DS5J thru DS12J	P-65
EI MON (CHAN 0-7)	DS5I thru DS12I	P-61, P-62, P-63, P-64
EF MON (CHAN 0-7)	DS5H thru DS12H	P-38
OD MON (CHAN 0-7)	DS5G thru DS12G	P-61, P-62, P-63, P-64
ID MON (CHAN 0-7)	DS5F thru DS12F	P-61, P-62, P-63, P-64
EF ACT (CHAN 0-7)	DS5E thru DS12E	P-61, P-62, P-63, P-64
OD ACT (CHAN 0-7)	DS5D thru DS12D	P-61, P-62, P-63, P-64
ID ACT (CHAN 0-7)	DS5C thru DS12C	P-61, P-62, P-63, P-64

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

INPUT/OUTPUT PANEL (A8A3) (MOD'S 0, 2, 3, 4 ONLY) (Cont'd)		
Panel Nomenclature	Reference Designator	Plate Number*
EF/OD ACK (CHAN 0-7)	DS5B thru DS12B	P-68
ID ACK (CHAN 0-7)	DS5A thru DS12A	P-68
EF MODE (C_O, C_E)	DS2A, DS4A	P-68
FUNCTION PRIORITY EI (ODD/EVEN)	DS13H, DS14H	P-66
FUNCTION PRIORITY EF (ODD/EVEN)	DS13F, DS14F	P-66
FUNCTION PRIORITY OD (ODD/EVEN)	DS13D, DS14D	P-66
FUNCTION PRIORITY ID (ODD/EVEN)	DS13B, DS14B	P-66
CHANNEL INTER-COMPUTER/NORMAL (CHAN 0-7)	S1 thru S8	P-61, P-62, P-63, P-64
CHANNEL FUNCTION (CHAN 0, 1)	S10	P-67
CHANNEL FUNCTION (CHAN 2, 3)	S9	P-67
CHANNEL FUNCTION (CHAN 4, 5)	S12	P-67
CHANNEL FUNCTION (CHAN 6, 7)	S11	P-67

TABLE 7-2. LAMP AND SWITCH INDEX (Cont'd)

OTHER		
Panel Nomenclature	Reference Designator	Plate Number*
POWER CONTROL RELAY	PSIK1	P-178
POWER SUPPLY INTER-LOCK SWITCH	A12S1	P-177
115° TEMPERATURE ALARM SWITCH	A12S2	P-177
140° OVERTEMPERATURE SWITCH	A12S3	P-177
115° TEMPERATURE ALARM SWITCH	A12S4	P-177
140° OVERTEMPERATURE SWITCH	A12S5	P-177
ODD CLOCK NARROW/ NORMAL SWITCH	A2A1S1	P-4
EVEN CLOCK NARROW/ NORMAL SWITCH	A2A1S2	P-4

*Refer to the functional schematics contained in Volume 2 Part 3 of this manual.

TABLE 7-2A. RECOMMENDED FAULT ISOLATION MODULE LIST

NAVSEA (UNIVAC) Part No.		Description	Quantity
2684511	(7000210)	Pulse-Delay Oscillator	1 EACH OF ALL MODULES
2684519	(7002000)	Flip-Flop	
2684520	(7002013)	Driver-Amplifier	
2684521	(7002020)	Flip-Flop	
2684522	(7002030)	Inverter	
2684523	(7002040)	Inverter	
2684524	(7002050)	Inverter	
2684525	(7002060)	Inverter	
2684526	(7002070)	Inverter	
2684527	(7002080)	Inverter	
2684528	(7002090)*	Input Amplifier	
2685118	(7002100)	Driver Amplifier	
2685119	(7002120)	Driver Amplifier	
2684529	(7002130)*	Driver Amplifier	
2684530	(7002141)*	Driver Amplifier	
2684531	(7002160)	Inverter	1 EACH OF ALL MODULES
2684532	(7002220)	Inverter	
2684533	(7002321)**	Differential Amplifier	
2684534	(7002332)**	Control Line Amplifier	
2686823	(7002342)**	Data Line Amplifier	
2685120	(7002861)	Voltage Regulator	
2685121	(7002880)	Voltage Sensor	
2684539	(7002900)	Flip-Flop	
2684540	(7002920)	Inverter	
2684541	(7002930)	Flip-Flop	
2684547	(7003480)	Time Delay	
2685122	(7003490)	Driver Amplifier	
2685123	(7003600)	Regulator Amplifier	

*For Slow Interface Only

** For Fast Interface Only

TABLE 7-2A. RECOMMENDED FAULT ISOLATION MODULE LIST

NAVSEA (UNIVAC) Part No.		Description	Quantity
2685124	(7003621)	Memory Driver	1 EACH OF ALL MODULES
2685125	(7003630)	Pulse Delay Network	
2685126	(7003640)	Emitter Follower	
2685127	(7003670)	Driver Amplifier	
2685128	(7003680)	Transformer Driver	
2685129	(7003710)	Pulse Delay Network	
2685130	(7003720)	Voltage Sensor	
2685131	(7003730)	Regulator Amplifier	
2685132	(7003740)	Control Amplifier	
2685133	(7003760)	Current Diverter	
2685134	(7003771)	Driver Amplifier	
2685135	(7003780)	Driver Amplifier	
2685136	(7003850)	Sense Amplifier	
2685419	(7500040)	Driver Amplifier	1 EACH OF ALL MODULES
2685420	(7500260)	Oscillator, Delay Line Amplifier	
2685421	(7500280)	Emitter Follower	
2685422	(7500320)	Voltage Regulator	
2685423	(7500340)	Voltage Sensor	
2685424	(7500400)	Memory Switch, Bipolar	
2685425	(7500421)	Drive Diverter	
2686800	(7500431)	Transformer Assembly	
3137506	(7500651)	Sense Amplifier	
2685428	(7500660)	Capacitor-Diode Assembly	
2685429	(7500671)	Capacitor Assembly	
2685430	(7500761)	Level Change Amplifier	
2686801	(7500781)	Voltage-Current Regulator	
2685432	(7500900)	Driver Amplifier	

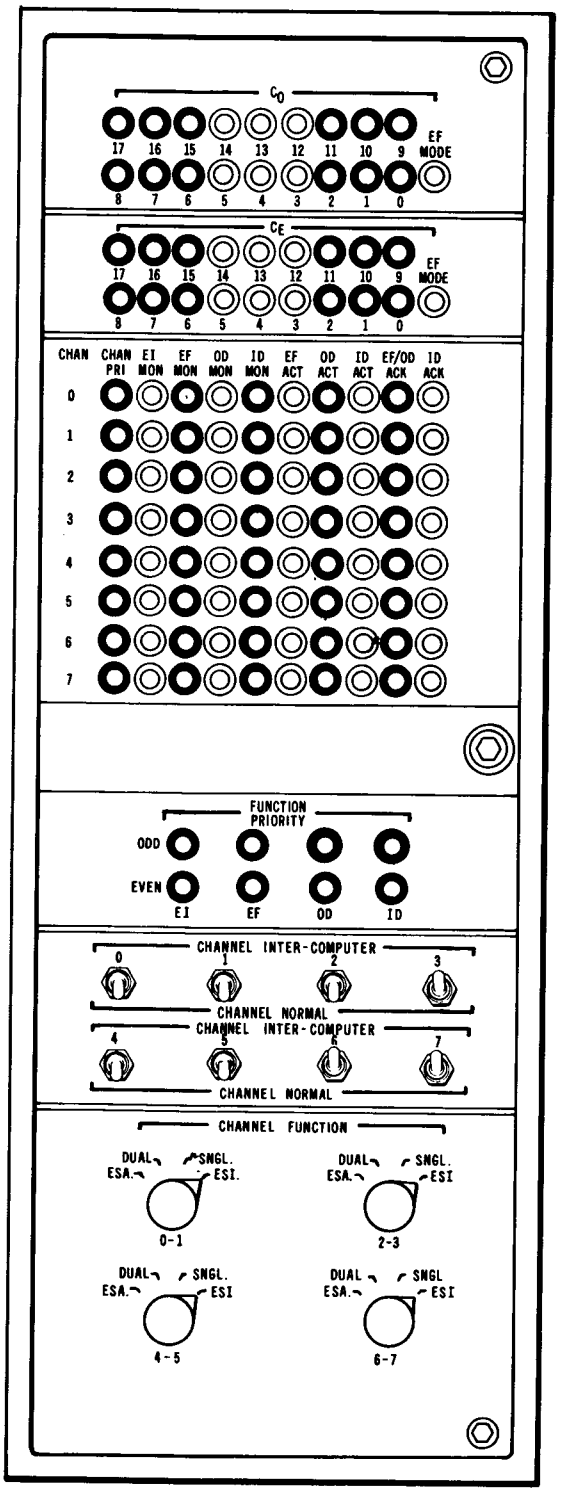

Figure 7-1. Maintenance Controls and Indicators-I/O Panel (A1 or A8)

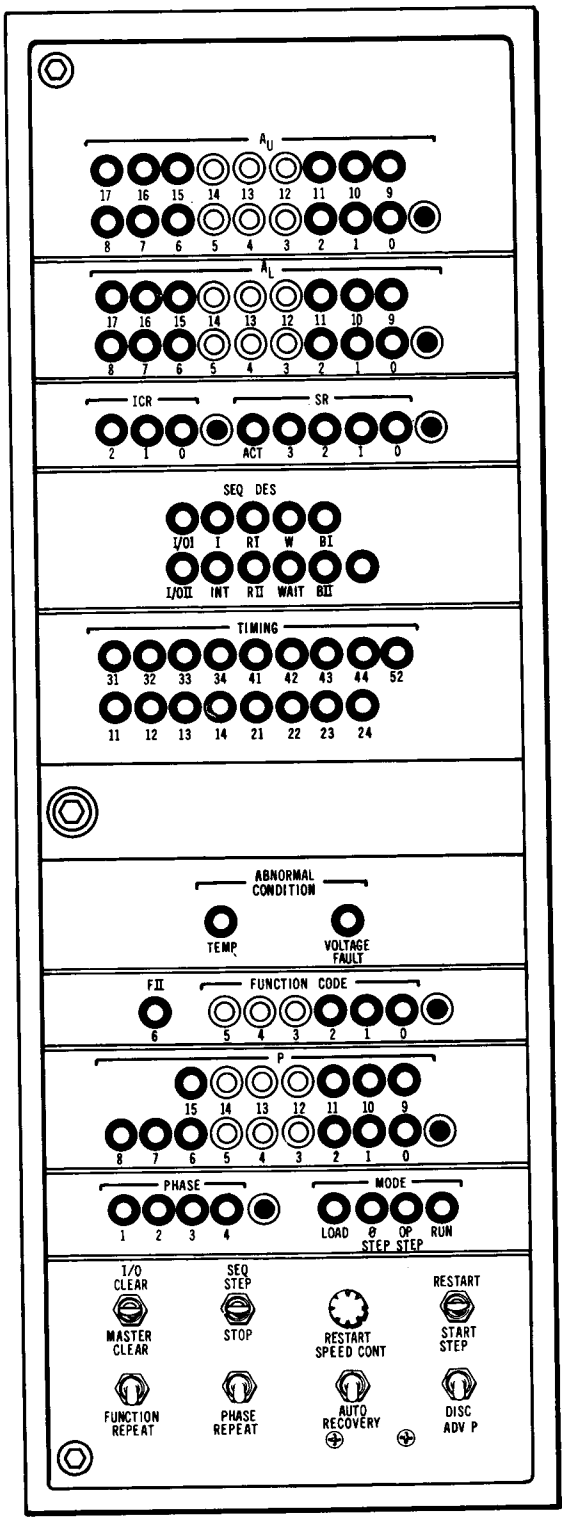

Figure 7-2. Maintenance Controls and Indicators - Control Panel 1 (A2)

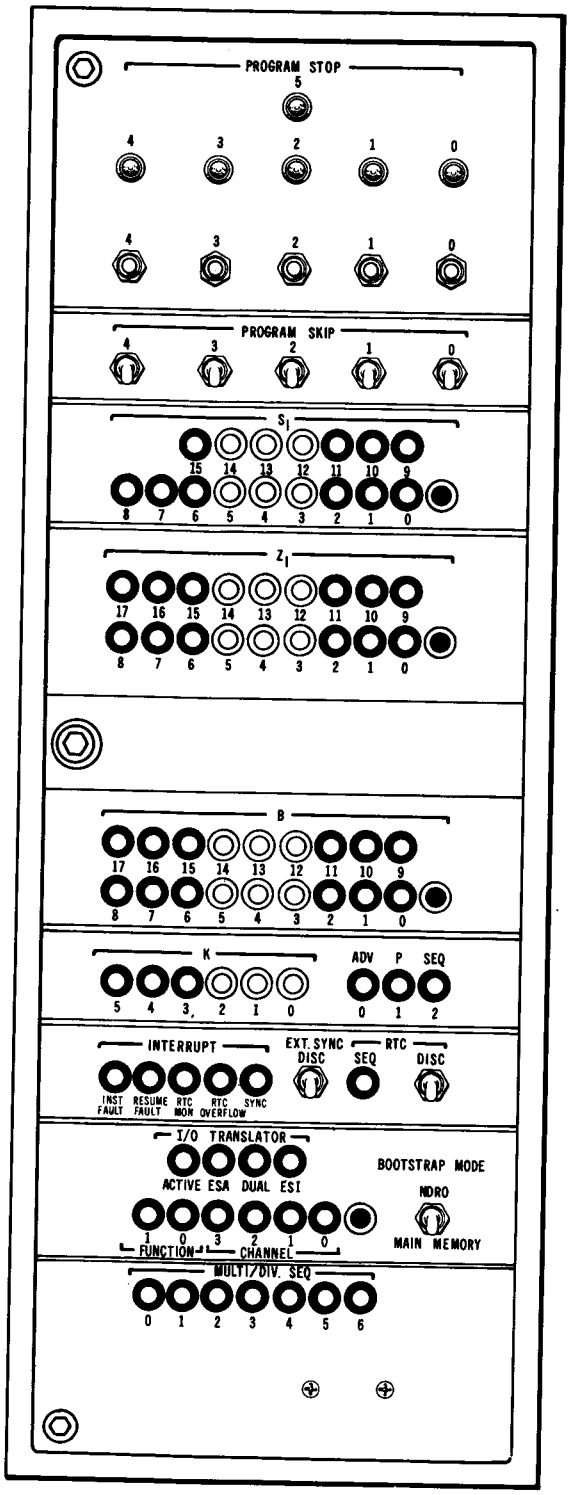

Figure 7-3. Maintenance Controls and Indicators - Control Panel 2 (A4)

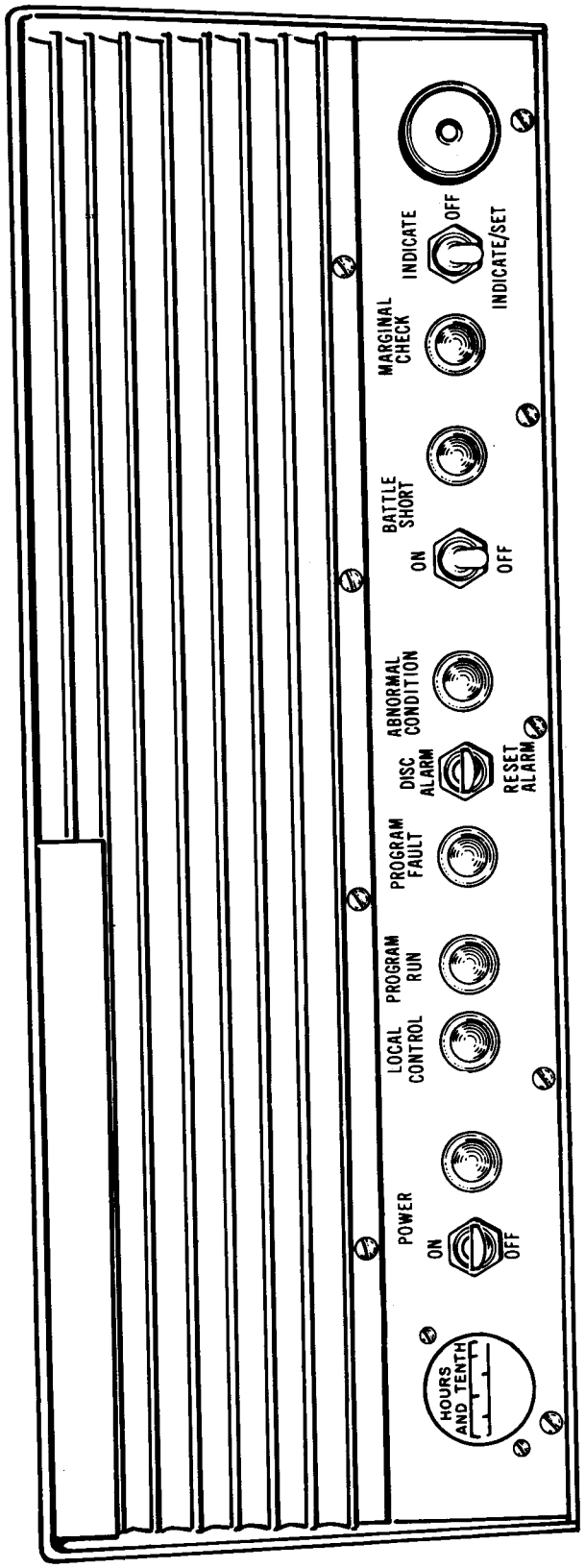

Figure 7-4. Maintenance Controls and Indicators - Power Control Panel (A5)

TABLE 7-3. TEST EQUIPMENT

	Description	Type Or Part No.	SCAT	Federal Stock Number	Function Or Usage
1	Current probe, AC, oscilloscope (with 5-ft or 9-ft cable and passive termination)	CBTV-015-0140-02 (with 5-ft cable) CBTV-015-0140-03 (with 9-ft cable)	4030/4030A		View waveforms in memory
2	Voltmeter, differential, AC-DC, solid state	CCUH-893A-01		6625-494-2954	Measure voltages
3	Multimeter	AN/PSM-4( )	4245	1N 6625-248-2052	Measure voltages & resistances
4	Oscilloscope, 30 MHz	AN/USM-281( )	4308	4G 6625-228-2201	View waveforms

TABLE 7-4. SPECIAL TOOLS

	Description	Supplier Or Manufacturer*	Part No.	Federal Stock Number	Function Or Usage
1	Taper pins, 18-20 GA (Initial Quantity: 8AV)	AMP	41652LP	9G 5940-885-4222	
2	Crimping Tool, 22-24 GA	AMP	47042	1A 5120-798-1933	Crimp taper pins to wire
3	Crimping Tool, 18-20 GA	AMP	47043	9Q 5120-662-8823	Crimp taper pins to wire
4	Crimping Tool, 16-18 GA	AMP	47044	9Q 5120-803-1223	Crimp taper pins to wire
5	Insertion Tool, taper pin	AMP	380306-2	9Q 5120-522-2714	Insert taper pins in connectors
6	Insertion Tool, taper pin	AMP	380310-3	9Q 5120-798-1934	Insert taper pins in connectors
7	Pin, insertion tip	AMP	395042	9Q 5120-986-3434	
8	Tool, extraction	AMP	91012-1	-- 5120-933-4099	
9	Gun, wire-wrap, w/3-wire cord	Gardner-Denver	14XA2-3		Fasten wires to wire-wrap pins
10	Sleeve, wrapping, 22 GA	Gardner-Denver	18640	9Q 5130-987-7059	
11	Sleeve, wrapping, 24 GA	Gardner-Denver	18840	9Q 5130-987-7057	
12	Bit, 24 GA (Mod) (u/w Slv 18840)	Gardner-Denver	26263	9Q 5120-051-3858	
13	Bit, 24 GA (Std) (u/w Slv 512056)	Gardner-Denver	26589		

TABLE 7-4. SPECIAL TOOLS (Continued)

	Description	Supplier Or Manufacturer*	Part No.	Federal Stock Number	Function Or Usage
14	Bit, 22 GA (Std) (u/w Slv 18640)	Gardner-Denver	26699	5130-018-5852	
15	Tool, wire removal (20-30 GA)	Gardner-Denver	500130	5120-104-9022	Unwrap wire-wrap connections
16	Sleeve, wrapping, 30 GA	Gardner-Denver	500350	5130-731-5941	
17	Bit, 30 GA (Mod.) (u/w Slv 512056)	Gardner-Denver	501381	5130-731-5985	
18	Bit, 28 GA (Mod.) (u/w Slv 502129)	Gardner-Denver	501389	5130-179-5651	
19	Sleeve, wrapping, 24, 28 GA	Gardner-Denver	502129	5970-179-8062	
20	Bit, 30 GA (Std) (u/w Slv 500350)	Gardner-Denver	504221	1A 5133-854-9886	
21	Tool, wire removal (Unwrap), 28-32 GA	Gardner-Denver	505244	1A 5120-854-9888	Unwrap wire-wrap connections
22	Bit, 30 GA (Mod.) (u/w Slv 500350)	Gardner-Denver	507063	5130-134-4572	
23	Sleeve, wrapping, 24-30 GA	Gardner-Devner	512056	1R 5130-419-6180	
24	Bit, 24 GA (Std) (u/w Slv 512056)	Gardner-Denver	512058		

TABLE 7-4. SPECIAL TOOLS (Continued)

	Description	Supplier Or Manufacturer*	Part No.	Federal Stock Number	Function Or Usage
25	Adapter sleeve, No. 16 (Initial Quantity: 100 ea)	Bendix	10-74696-6		
26	Extender cable, circuit card	Univac	7009452-00	6625-818-4657 YU	Extend PC Module for test

* Manufacturer	FSCM
CBTV (Tektronix)	80009
CCUH (John Fluke)	89536
AMP	00779
Gardner-Denver	24047
Bendix	77820
Univac	90536

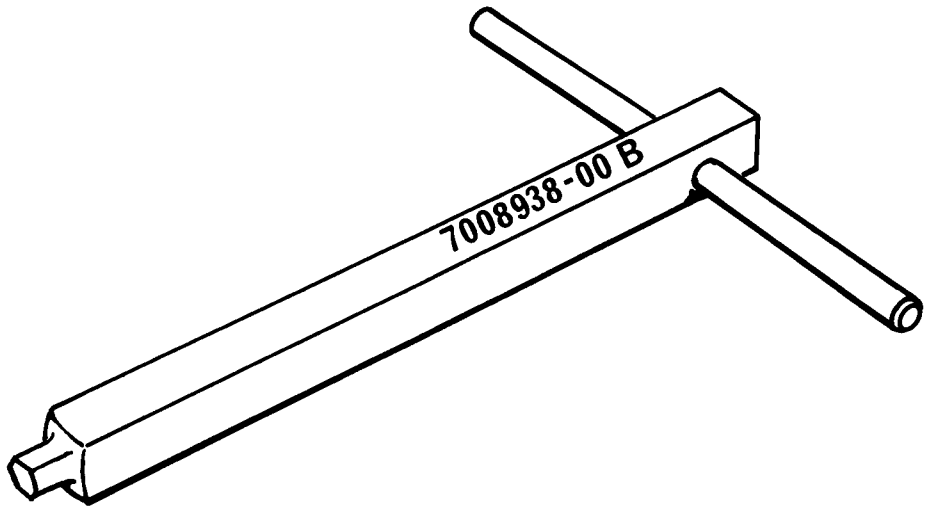

Figure 7-5. Combination Tool

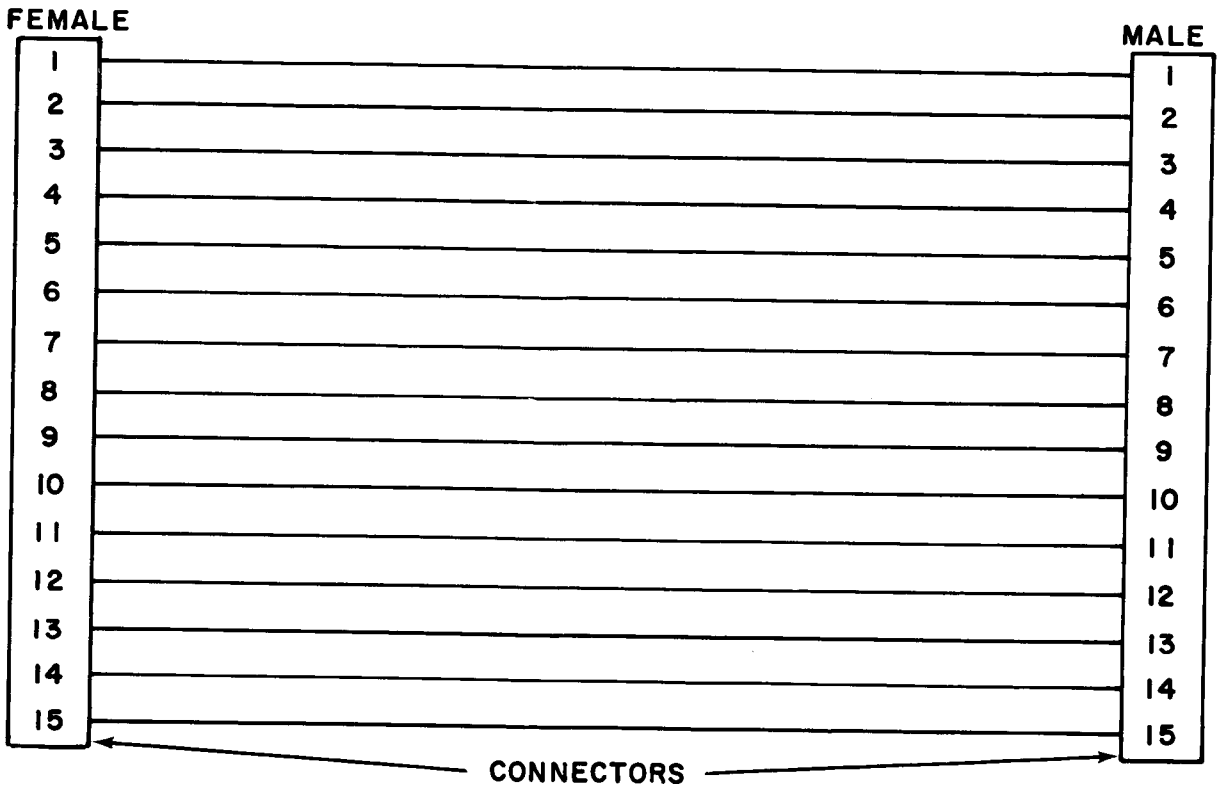

Figure 7-6. Module Extender, Wiring Diagram

7-13. REPAIR PROCEDURES.

7-14. TYPES OF CONNECTIONS. Repair procedures other than component (printed circuit module) replacement are almost entirely limited to forming soldered connections and wire-wrapped (solderless) connections.

7-15. Solder Connections. Normal techniques employed for electronic component replacement and repair should be applied when removing and forming soldered connections.

7-16. Wire-Wrapped Connections. The majority of electrical connections in the computer are mechanical, solderless connections formed by wrapping a solid wire around a pin. The wrapped connection forms a helical coil around the pin with points of contact at each of the four pin corners. Four points of contact are made for each turn of the connecting wire that encircles the pin. Figure 7-7 illustrates one acceptable and three unacceptable wire-wrapped connections.

7-17. Use of the Wire-Wrap Gun. Wire-wrap connections are formed with a wire-wrap gun (figure 7-8). This tool has a bit that rotates inside a stationary sleeve. The stationary sleeve holds the bit in place and has a slotted end that prevents the wire outside of the bit from rotating during the wrapping operation. The sleeve is held in the wire-wrap gun by a chuck. The bit has a longitudinal groove that accommodates the end of the wire to be wrapped. A hole in the end of the bit (in the center) allows the bit to be slipped over the pin on which the wire-wrap connection is to be made. The bit and sleeve used will depend on the gauge of the wire and size of the pin being wrapped. All bits are modified so that a portion of the insulation on the wire is also wrapped. Before using the wire-wrap gun, the wire should be stripped of the required amount of insulation. Then the stripped end of wire and insulation should be inserted as far as it will go into the outer hole of the bit.

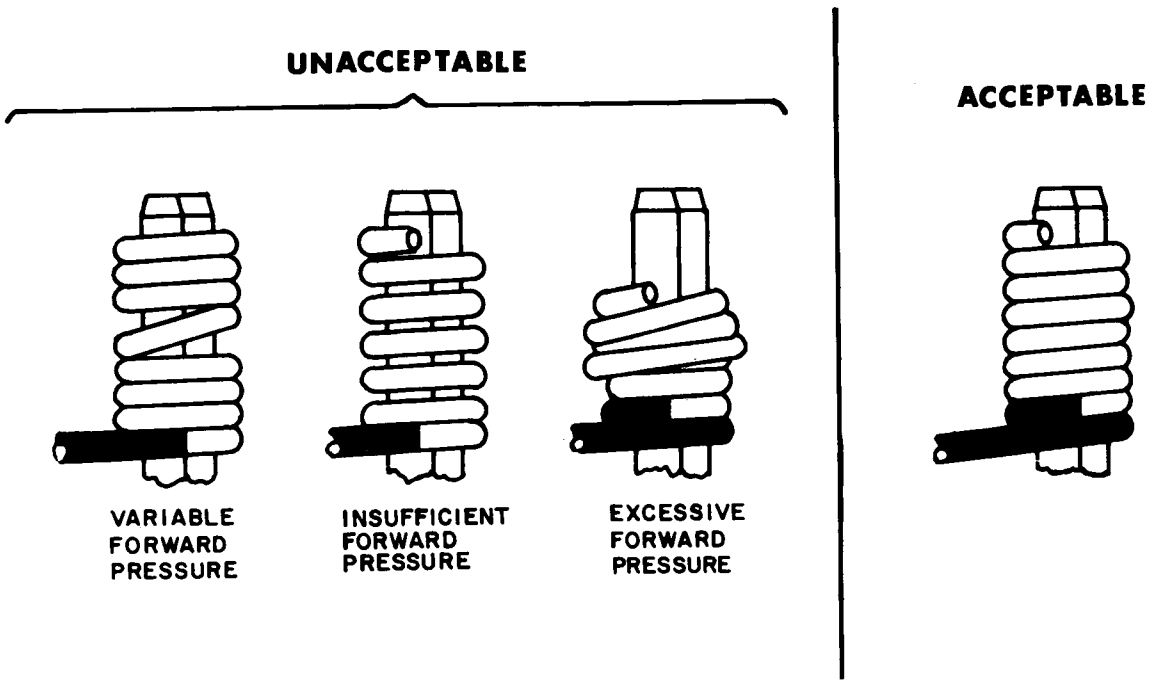

Figure 7-7. Wire-Wrap Connections

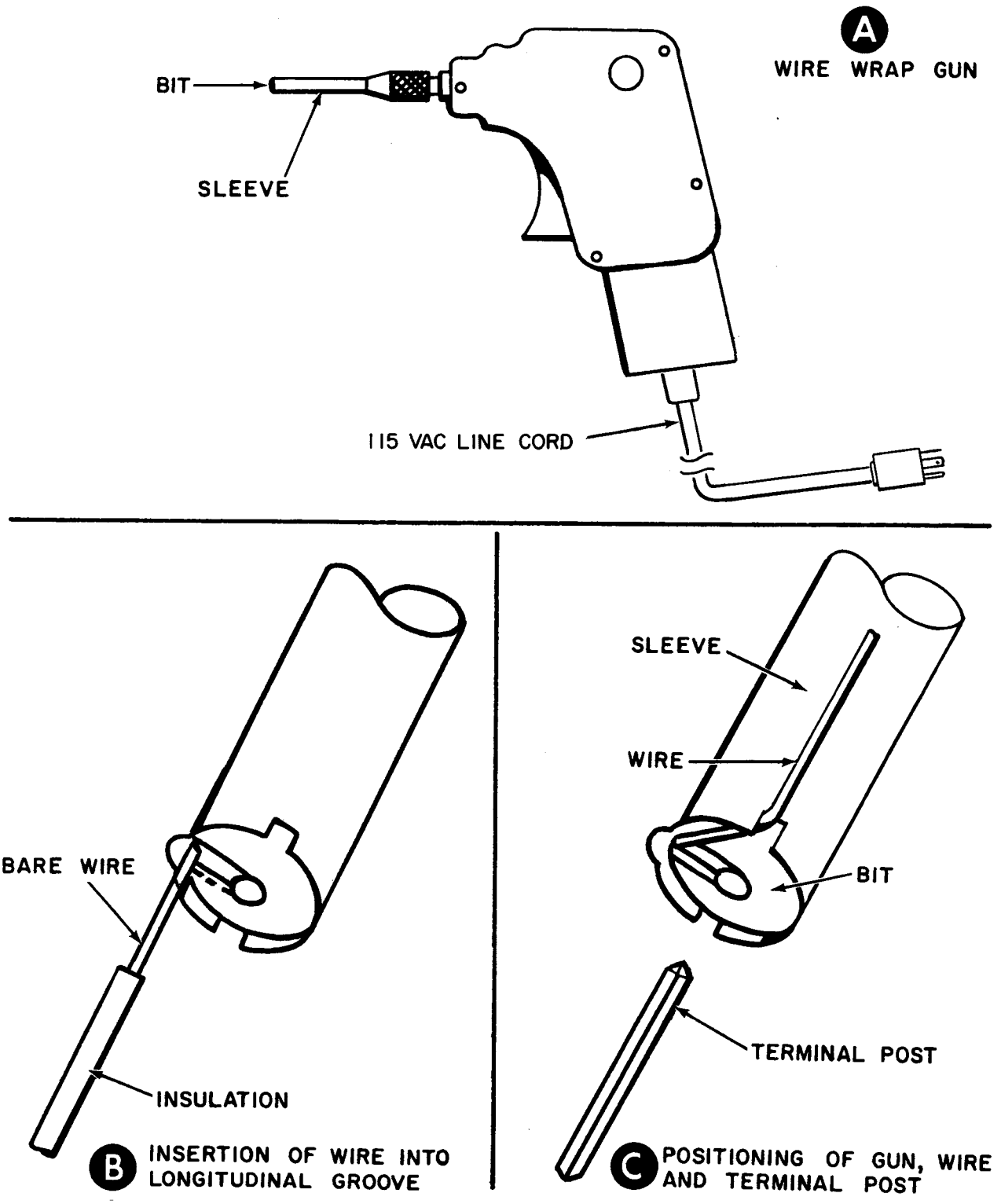

Figure 7-8. Wire-Wrap Gun

Next the wire should be bent along the side of the sleeve, ensuring the wire passes through one of two slots on the end of the sleeve. Table 7-5 specifies the length of the stripped wire and insulation to be inserted in the bit for various wire-wrapping applications. The bit should be slipped over the pin to the lowest level or the designated tab level. The wire is then wrapped around the pin by allowing the gun to come up on the pin while maintaining constant forward pressure needed to obtain an acceptable wire-wrapped connection.

NOTE: Adjacent wires may be held aside with a spring hook during the wrapping process.

The completed connection should be inspected to ensure the wire is tightly wrapped around the pin and the number of turns of stripped wire and insulated wire around the pin is correct for the application as follows:

1. 24-Gauge Wire: Five to six turns of bare wire and one-half to two turns of insulated wire are required.
2. 30-Gauge Wire: Seven to ten turns of bare wire and one-half to two turns of insulated wire are required.

The wire must be so routed that there is 1/32 inch minimum of slack between the wire and any pin or obstruction that could cause a short circuit due to electrical conduction through the insulation.

7-18. Deleted.

7-19. Use of Unwrap Tool. Removal of a wrapped wire requires use of the proper unwrap tool. This tool has a right and left handed end depending on which direction the wire is wrapped. The factory wire-wrap machine wraps one end of the wire clockwise and the other end counterclockwise. While unwrapping the ends of the wire, care should be taken not to lose, in the chassis, any pieces of wire that break off. Before removing a wire, the destination of both ends should be verified to ensure it is the right one. After unwrapping each end, one end should be cut and the other end used to pull the wire out of the chassis. A spring hook may be needed to work the wire loose. When adding a new wire, that portion of an old wire which has been previously wrapped should never be rewrapped. Occasional cleaning of the wire-wrap bit and sleeve with chlorethene and a brush will prevent excessive wear and ensure proper operation. Coating the wire-wrap gun, bits, and sleeve with a film of light oil prior to storage will prevent formation of rust.

7-20. COMPONENT REPLACEMENT AND REPAIR. If the diagnostic tests or other fault isolation procedures indicate that replacement and/or repair of malfunctioning components is necessary, reference should be made to the appropriate Unscheduled Maintenance Requirement Card (UMRC). All the UMRC's available at an installation are listed on a Maintenance Index Page (MIP). These UMRC's contain repair, replacement, and alignment procedures not duplicated in this OP. However, certain basic maintenance procedures routinely performed during both scheduled and corrective maintenance are included in this section of the manual.

7-20A. TEST POINT NOMENCLATURE. Each of the logic drawers contain four test blocks. Memory test points are on circuit cards. Individual points within a test block are identified by a two-coordinate system which uses letters from left to right and numbers from top to bottom. The first designator represents the particular test block on a given chassis. For example: TB2-B2 indicates test block 2, coordinates B and 2.

NOTE: Test blocks have been removed from the memory drawer on serial numbers 49 and higher and also on serial numbers 14 through 48 if the memory is larger than 32K. Memory test points for these computers are on circuit cards.

TABLE 7-5. WIRE-WRAPPING APPLICATIONS

Application:		Recommended Length of:	
Wear Size	Pin Size	Stripped Wire	Insulation Inserted In Bit
24 Gauge Wire	Large	1 1/2 ± 1/16"	1/8"
30 Gauge Wire	Large	1 1/2 ± 1/16"	3/16"
30 Gauge Wire	Small	1 1/8 ± 1/16"	1/8"

7-21. Test Block Location. To expose the test blocks for any logic chassis perform steps as follows:

1. Use the combination tool (figure 7-5) to turn the three panel locking screws (figure 7-9).
2. Swing out the front panel to expose the test blocks, wiring connections, and various panel indicators. Figure 7-9 shows the location of parts with the front panel open.

7-22. Drawer Extension. Extension of a drawer from the computer is accomplished by performing the following steps:

CAUTION

Prior to extending a drawer, remove power from the computer circuitry to prevent possible damage to logic modules.

1. LOGIC DRAWER

a. Turn the three panel locking screws and swing open the front panel.

b. Use the combination tool to turn the exposed drawer locking screw (figure 7-9) counterclockwise until the plugs on the rear of the drawer are disengaged from the jacks on the rear panel.

CAUTION

If the computer is not securely fastened to the deck, do not extend more than one upper drawer or two lower drawers from the cabinet at any one time. Extending more than this number may upset the balance of the cabinet and tip the cabinet forward.

c. Slowly pull the drawer forward towards its fully extended position (figure 7-10) until the slide catch which is located on the bottom rail engages. If necessary, lift the front of the drawer slightly to engage the slide catch.

NOTE: To return the extended drawer into the cabinet, release the slide catch, push the drawer into the cabinet, and use the combination tool to turn the screw clockwise until the drawer is fully seated in the cabinet.

2. MEMORY DRAWER

a. Lift each of the four latch fasteners

and rotate counterclockwise until the memory drawer is free to be extended

b. Slowly pull the drawer forward towards its fully extended position until the slide catch engages. If necessary, lift the front of the drawer slightly to engage the slide catch.

NOTE: To return the memory drawer into the cabinet, release the slide catch, push the drawer into the cabinet and rotate the latch fasteners clockwise and push down to lock.

7-23. Exposure of Chassis Wiring. When it is desired to open a chassis and expose chassis wiring, perform the following steps:

1. LOGIC DRAWER

a. Extend the drawer.

b. Release the spring clip located on the rear chassis support.

c. Slowly swing the logic chassis on its hinges to expose the wiring as shown in figure 7-10.

2. MEMORY CHASSIS

a. Extend memory drawer.

b. If memory drawer contains Chassis A3A1, release two screws and swing Chassis A3A1 open.

c. Remove 24 screws from plate on wiring side of chassis to expose wiring.

NOTE: The return of a chassis to its secured position is accomplished by performing the above steps in reverse order.

7-24. Extension of Power Supply. Extension of power supply is accomplished as follows:

1. Lift the latch fasteners (figure 7-11) and rotate 90 degrees.

2. Slowly pull the power supply assembly away from the cabinet toward its fully extended position (figure 7-11) until the slide catch engages.

7-25. Temperature-Sensing Switch Location. The temperature-sensing switches are located on the bottom plate of the main cabinet. Access to these switches is gained by removal (see CMIP for appropriate CMC) of drawer A3 from the computer cabinet. Temperature sensors can be seen with memory drawer A3 extended.

7-26. Air Filter Location. Preventive maintenance procedures are provided in MRC format for vacuum cleaning the air filter once each week. The filter is located behind the grill on the power control panel (figure 7-12). Removal of the air filter for scheduled maintenance is accomplished by unloosening the four grill-retaining screws, removing the grill, and then pulling out the filter.

7-27. Fuse Replacement. Operating power to each drawer is protected by suitably rated fuses as listed in table 7-6. The logic drawer fuses are located directly behind the drawer with which they are associated. Accessibility is obtained by extending the drawer and swinging open the chassis as shown in figure 7-10. Actual location of a fuse panel is in the computer cabinet behind the logic drawer. Figure 7-11 shows the location of the power supply fuses. Fuses for main memory power supply are readily accessible in the upper rear areas of a memory chassis memory drawer that has been fully extended or removed.

TABLE 7-6. LOCATION OF FUSES

Location	Ref. Desig.	Rating in Amperes
Drawer A1 or A8 (I/O)	F1, F4	5
	F2, F5	12
	F3, F6	4
Drawer A2 (Control)	F1	8
	F2	10
	F3	5
	F4	6
	F5	12
	F6	4
Drawer A3 Chassis A1 or A2	F1, F2, F3, F6	1
	F4, F5	20
	F7	15
	F8	8
	F9	0.5
Drawer A4 (Control)	F1, F4	6
	F2	12
	F3	3
	F5	8
	F6	5
Drawer PS1 (Power supply)	F1, F2, F3	8
	F4, F5, F6	2
	F7, F11	6
	F8, F9, F10	20
	F12, F13, F14	5
	F15, F16, F17	12
Power Control Panel (A5)	F1	12

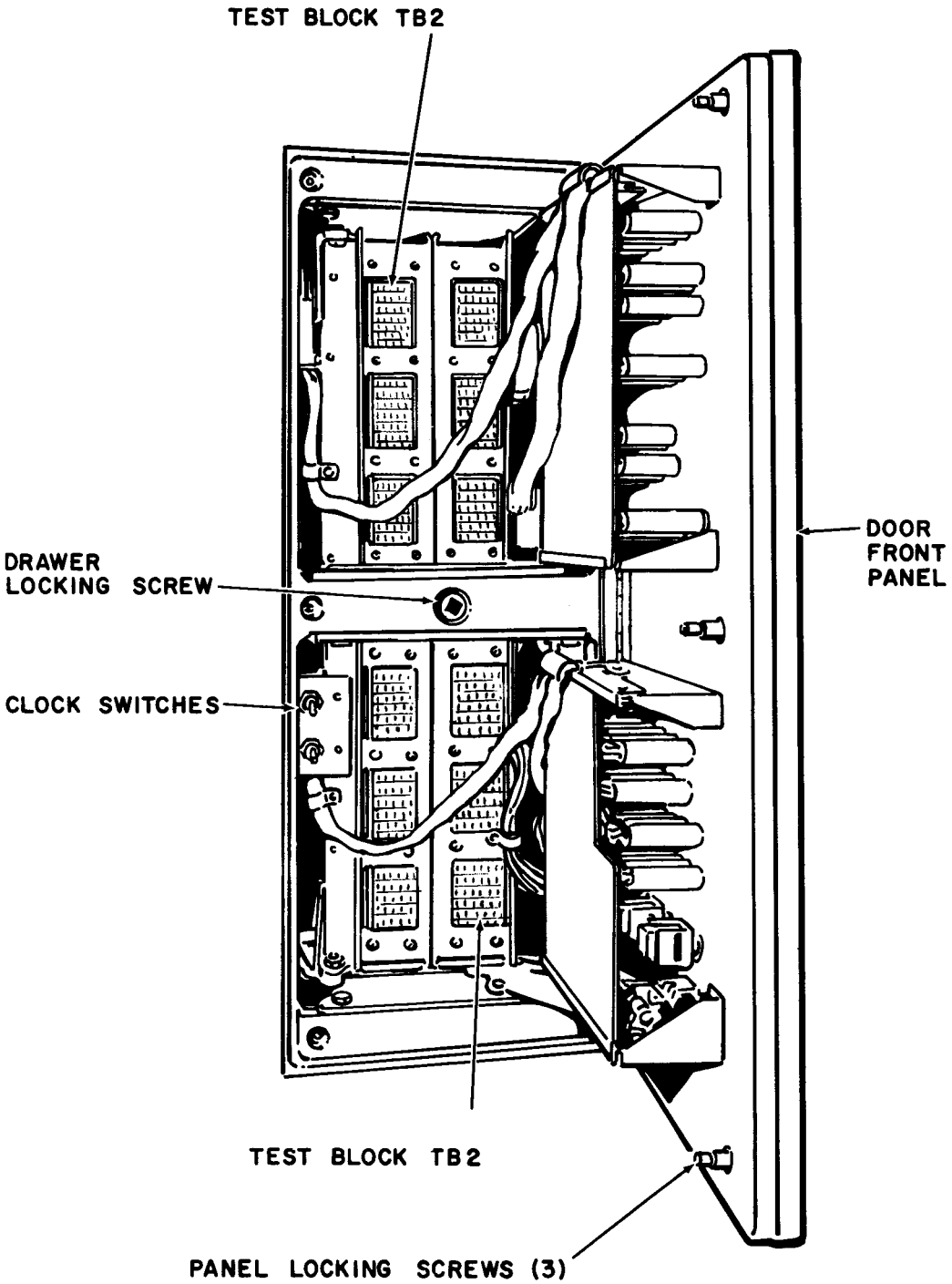

Figure 7-9. Location of Parts in Logic Drawer-Panel Opened

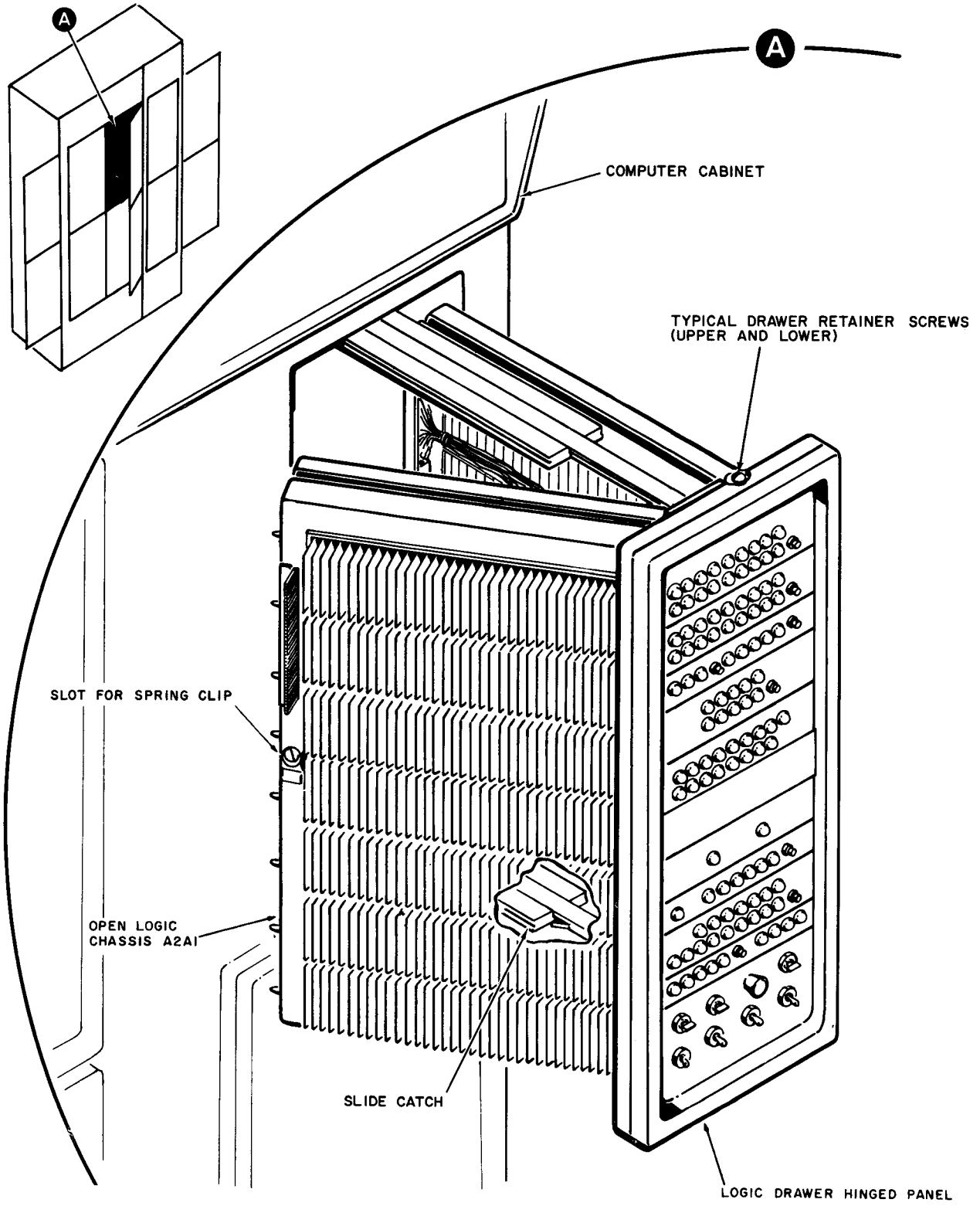

Figure 7-10. Extended Logic Drawer A2

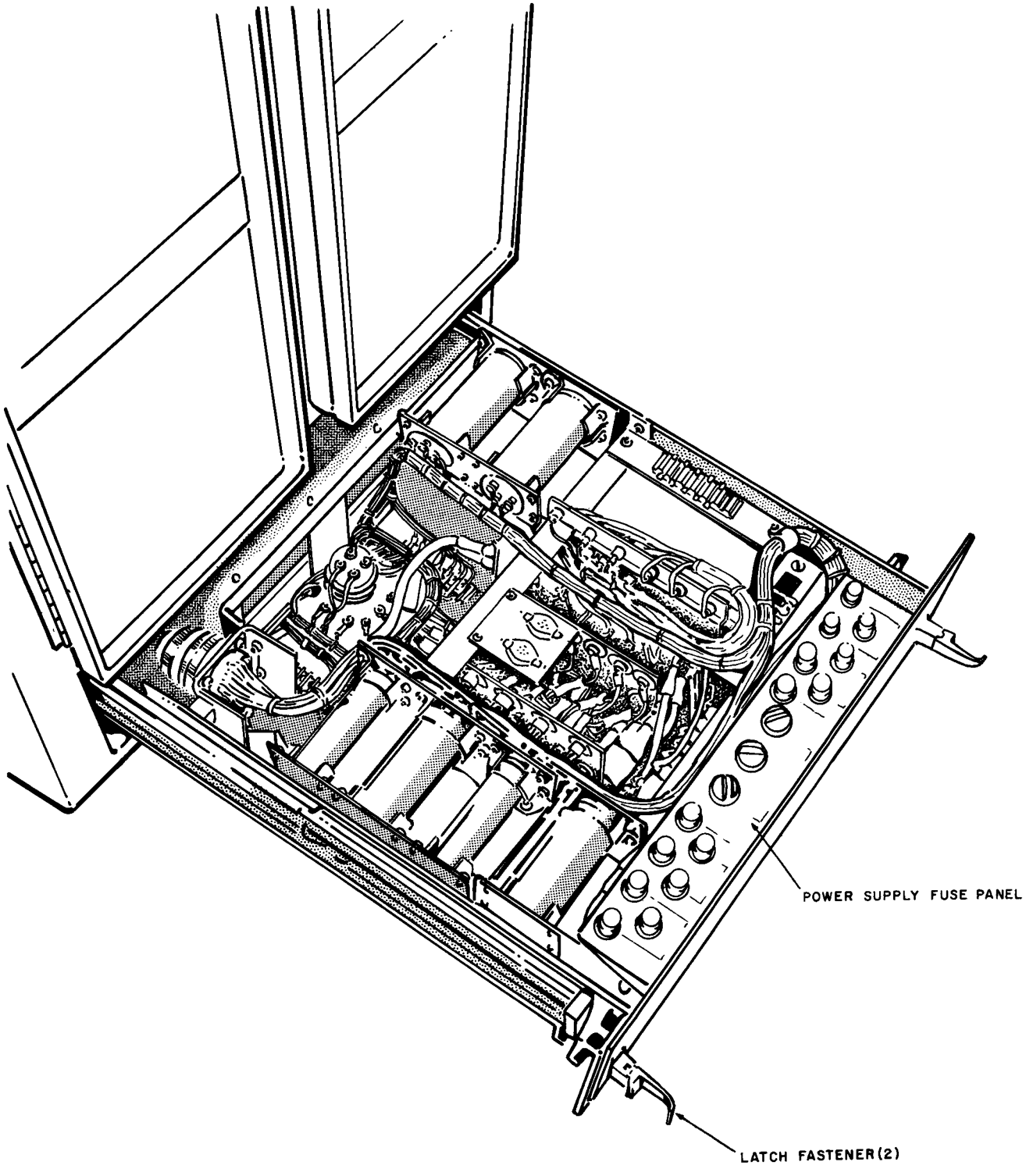

Figure 7-11. Extended Power Supply PS 1

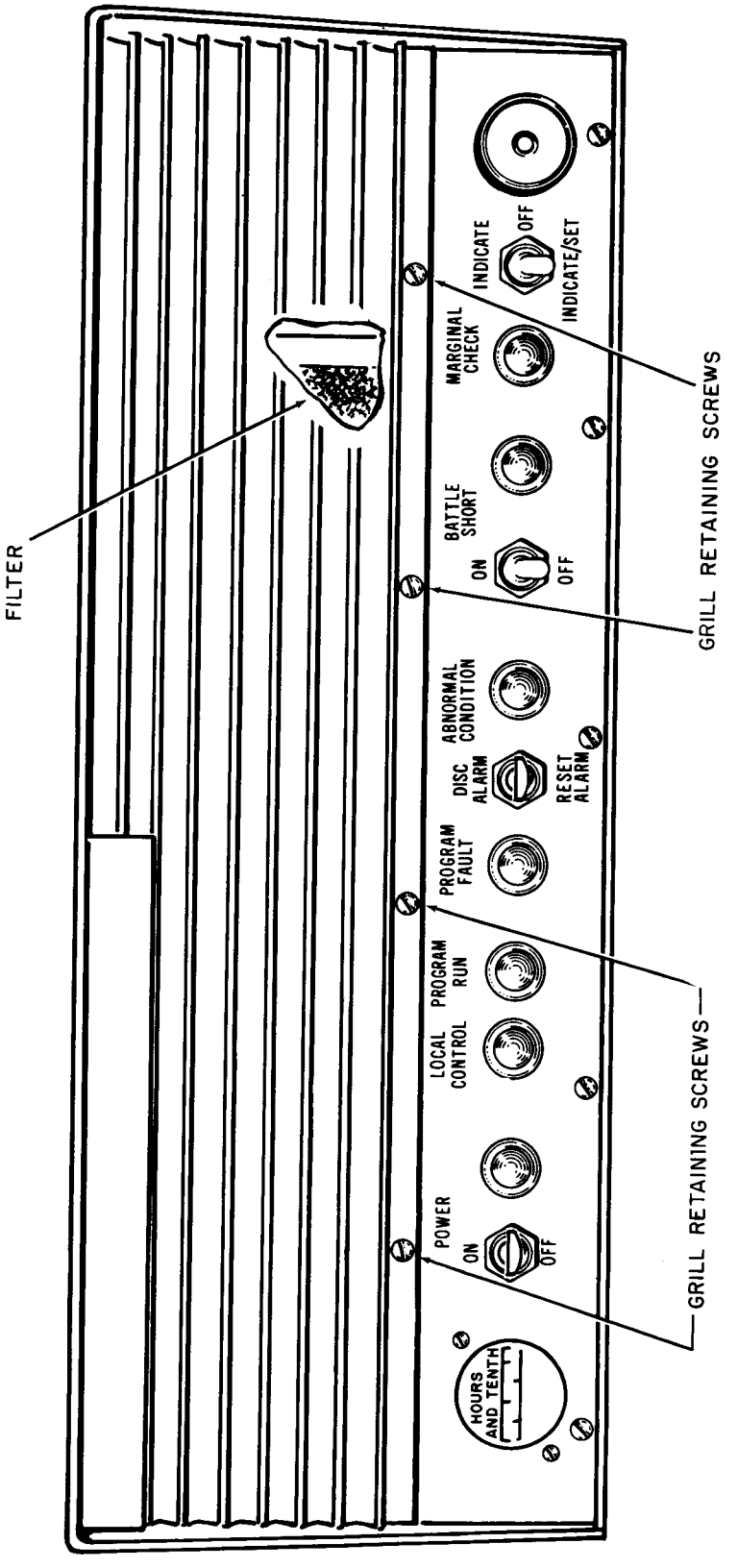

Figure 7-12. Power Control Panel

7-28. COMPUTER OPERATIONAL MODES.

7-29. LOGIC OPERATIONS. The computer performs logic operations in any one of four modes of operation which is manually selected by pushing the specific MODE button indicator on control panel 1 (A2). These pushbutton indicators are identified as: LOAD; PHASE STEP; OP STEP; and RUN (refer to figure 7-2). The interconnective logic circuitry is so designed that only one mode at a time can be selected. Logically, mode selection is made by the mode selection circuitry which enables the selected mode and disables the remaining three modes. A brief description of each operational mode (see table 7-7) is given as follows:

1. LOAD - Load mode forces the computer logic to address the first instruction of bootstrap at address 500_8; either main memory or NDRO bootstrap may be referenced, depending on the position of the BOOTSTRAP mode switch. The computer operates at the high-speed rate until after the memory referencing has occurred, and then it reverts to the normal run mode.

2. PHASE STEP - Phase step mode provides normal computer operation, including the memory circuitry, at a controlled rate of speed. Used primarily for logic malfunction isolation, phase step mode may be executed either by manually issuing each successive phase of the master clock through the START STEP position of the RESTART/START STEP switch, or by using the RESTART position of the switch and the low-speed oscillator. The RESTART SPEED CONT potentiometer controls speed of computer operation in the phase step mode. By placing the PHASE REPEAT switch in the up position and selecting a desired phase, the computer repeatedly issues the chosen pulse at a high rate of speed. If all four phases are selected, a cycle-step operation results.

3. OP STEP - In the OP step mode, the computer operates at a high rate of speed but its operation is stopped at selected intervals throughout the performance of a program and must be manually restarted. During this mode, the operator examines the contents of the various registers for accuracy at specific times throughout the execution of a program. If a malfunction is detected, the operator can determine from register content the approximate point of error in the program. Each operation of the RESTART/START STEP switch steps the computer through an instruction. If the SEQ STEP/STOP switch is off, the computer stops after the I sequence of each Format I instruction. If the switch is on, the computer stops after each major sequence of an instruciton.

4. RUN - Run mode is the normal high-speed operating mode of the computer. All operations not pertaining to malfunction isolation and program debugging are performed in run mode. Although intital program loading is performed in the load mode, the computer reverts to run mode after approximately 2 microseconds of operation.

7-30. WIRE MEMORY (BOOTSTRAP). The computer has 32_{10} bootstrap memory address locations (00500_8 through 00537_8) which contain the wired memory bootstrap program for an initial load or bootstrap program. The computer can have a bootstrap written for paper tape or magnetic tape. The wired load program provides capability to enter an intitial program which may subsequently be used to enter more sophisticated programs. These memory address locations have unique characteristics in that they operate in a special type of nondestructive read-out mode. They are not accessible to the programmer for store-type instructions.

7-31. AUTOMATIC RECOVERY MODE. If a fault condition occurs during the running of a program and the AUTO RECOVERY switch is in the up position, and interrupt addresses 00500_8 (starting address of the wired load program). This locks out all interrupts and initiates the wired load program. For paper tape input, the paper tape must have been placed in the reader (may be positioned on any leader frame) for the recovery to be completed. A fault condition occurring during the running of a program with the AUTO RECOVERY switch in the center position causes a jump to address 00000. Action continues as programmed.

TABLE 7-7. CONTROL PANEL SWITCH SETTINGS AND RELATED OPERATION

CONTROL PANEL SWITCHES					OPERATION
RESTART/ START STEP	SEQ STEP/ STOP	AUTO RECOVERY	PHASE REPEAT	FUNCTION REPEAT	
Settings With RUN Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Initiates normal computer high-speed run.
START STEP	Neutral	Up	Down	Down	Initiates normal high-speed run with bootstrap memory referenced after program fault.
START STEP	Neutral	Down	Down	Up	Repeat instruction contained in F register at computer high-speed run.
Neutral	STOP	Down	Down	Down	Stop computer high-speed operation after the execution of the I sequence of the next instruction.
RESTART	Neutral	Either	Down	Either	Restart computer operation after a stop instruction or operation of the SEQ STEP/ STOP switch.

TABLE 7-7. CONTROL PANEL SWITCH SETTINGS AND RELATED OPERATION (Continued)

CONTROL PANEL SWITCHES					OPERATION
RESTART/ START STEP	SEQ STEP/ STOP	AUTO RECOVERY	PHASE REPEAT	FUNCTION REPEAT	
Settings Wigh PHASE STEP Mode Indicator Lighted					
START STEP	Neutral	Either	Down	Either	Send indicated phase pulse to computer logic, advance phase generator, and stop.
RESTART	Neutral	Either	Down	Either	Continuously send sequential phase pulse, as indicated, to computer logic and advance phase generater.
START STEP	Neutral	Either	Up	Either	Send a continuous pulse of phase indicated to computer logic at normal high-speed rate.
Settings With OP STEP Mode Indicator Lighted					
START STEP	Neutral	Either	Down	Either	Stop computer operation after execution of I sequence of each instruction.
RESTART	Neutral	Either	Down	Either	Continuously restart computer operation after above listed stop.
START STEP	SEQ STEP	Either	Down	Either	Stop computer operation after each major sequence.
RESTART	SEQ STEP	Either	Down	Either	Continuously restart computer operation after above listed stop.
Settings With LOAD Mode Indicator Lighted					
START STEP	Neutral	Down	Down	Down	Jump to address 00500 initiate bootstrap program, clear load mode, and continue operation in run mode.

Section 7-2. Manual Troubleshooting

7-32. MANUAL TROUBLESHOOTING PROCEDURES

7-33. PURPOSE. The diagnostic program is used for rapid detection and isolation when troubleshooting computer casualties; however, when the diagnostic program fails to isolate the casualty, other methods must be used. Therefore, this section contains procedures and tests for manually troubleshooting the computer when diagnostics fail to isolate the casualty. Included in this section are manual tests, program analysis, and manual programing.

7-34. MANUAL TROUBLESHOOTING PROCEDURES. Table 7-7A(I) is a list of manual troubleshooting procedures which contain tests, checks and adjustments from both the MRCs and volume 2, part 1. The list also contains procedure for analyzing the diagnostic program and manual programing. Each procedure is listed by a procedure number, description, MRC, table or paragraph number, and plate number. Table 7-7A(II) contains all procedures listed in table 7-7A(I); however, the procedures in this table are listed by categories. Some procedures are listed more than once, such as the checkerboard memory test because it can test both main memory and control memory. When a category has more than one procedure listed, it may not be necessary to perform all procedures. As an example, the category of main memory lists memory checks and current and voltage adjustments. If the checkerboard memory test and the manual memory test check satisfactorily, current or voltage need not be adjusted.

7-35. PROCEDURE DESCRIPTION TABLE (7-7A). The following information provides a description of the procedures listed in Table 7-7A(I).

1. Verify AC power and DC voltage levels and ripple. Check the 115VAC input to PSI, the + 15, -15, and -4.5VDC in drawers A1, A2, A4 and A8, the -7 Reg, -15 Reg and + 15 Reg in chassis A4A2, and the + 6, + 15, -15, -3 and + 3VDC in drawer A3.

2. Check 104-volt memory protection circuit and check 101-volt memory protection circuit. The 104-volt circuit is checked by monitoring the AC input at PSI and then lowering the input voltage until the ABNORMAL CONDITION lamp is lit, the alarm sounds and the PROGRAM RUN lamp extinguishes. The voltage at this time should be 104VAC and memory should be disabled.

The 101-volt circuit is checked by positioning Battle Short on, monitoring the output of gJ11C-TP1 and lowering the input voltage until the output of TP1 changes voltage levels. At this time the voltage should be 101VAC and memory should be disabled.

3. Adjust main memory currents and sense bias voltage. Procedure uses an AC current probe to monitor the X Read/Write, Y Read/Write and the Inhibit currents. If required, the currents are adjusted on the 7500781 cards for each bank. The sense bias voltage is monitored and adjusted on the 7500781 cards.

4. Adjust the + 3VDC memory voltage. Procedure provides the adjustment of the voltage regulator 00VR03 used to drive Q-1 which regulates the + 3VDC to main memory.

5. Adjust 104-volt memory protection circuit and adjust 101-volt memory protection circuit. This procedure ensures that the 104-volt memory protection circuit is set up correctly by adjusting the cards at locations.

7J34E and 7J34F for a change from a low level to a high level output when the AC input is decreased to 104 volts. It also ensures the 101-volt memory protection circuit is set up correctly by adjusting the card at location gJ11C for a change from a low level to a high level when the input voltage is decreased to 101VAC.

6. Adjust control memory (initial adjustment) and adjust control memory (fine adjustment). This procedure monitors and adjusts the Regulated + V and -V voltages for the control memory digit drivers and the -7 volts sense bias to the control memory sense amplifiers. Procedure also ensures the pulse outputs of bits 0-17 of the sense amplifiers is aligned properly with the control memory strobe pulse. The procedure also checks the limits of the + and - Regulated voltages and sets up the Read and Write currents.

7. Adjust clock cycle timing and phase pulse timing. Procedure monitors the output of the odd-and-even phase generators in the master clock and adjusts the taps on delay lines 3J35C and 3J35D to ensure phases 1, 2, 3, and 4 are the correct pulse width and cycle period in the normal and marginal condition.

8. Adjust main memory strobe timing pulse. Procedure monitors the strobe enable pulse in main memory timing and the sense amplifier outputs bits 0-17 of all 7500651 cards. The taps of delay line 50MT21 at gJ25C are moved to achieve the correct width of the strobe enable and the timing between the strobe and the sense pulses.

9. Adjust slow interface I/O acknowledge timing. Procedure checks and adjusts the correct delay time of EF/OD acknowledge delay lines gJ31G and gJ32G and ID acknowledge lines gJ28G and gJ29G. A short output routine is used to provide enabling signals for checking and adjusting the delay lines. Since only an output routine is used, the ID acknowledge delays lines are adjusted in the OD acknowledge delay line locations and then reinserted in their original locations.

10. Manual method of intercomputer load. Procedure provides a manual method of rapidly transferring the contents of one Mk 152 computer to a second Mk 152 computer via an intercomputer channel. This includes the transfer of the operational program or of diagnostics and special routines.

11. Maintenance turn-on procedure. The maintenance Turn-On (MTO) procedure (table 7-1) provides a manual means for checking computer power, indicators, switches, and front panel registers.

12. Checkerboard Memory Test. This test (table 7-8) is a quick-and-easy check to determine if memory has any 651 card casualties. The test first clears memory and then stores a pattern of all one's in the odd locations. An ADD instruction is then used to add memory to AL. Since memory contains alternate positive and negative zero's, AL should remain clear. Since this test may not detect casualties in cards other than 651's it is recommended that a test to store all one's and a test to store all zero's always be run to completely check-out memory. This procedure is also essential to determine error patterns. This test should be used with the Memory Test Check Flow Chart (figure 7-13). Refer to para 7-44D for a sample memory troubleshooting problem.

13. Manual Memory Test Procedure. A test (table 7-9) that will store all one's or zero's in memory is one possible way to determine error patterns in memory. In this test, either all one's or zero's (negative or positive) are stored throughout memory. For a detailed look at the error patterns, an ENTAL (f = 12) instruction is recommended using OP STEP mode and RESTART. This test should be used with the Memory Test Check Flow Chart (figure 7-13). Refer to para 7-44D for a sample memory troubleshooting problem.

)CEDURES AND CATEGORIES

ΓE NUMBER
/DC, P-180; -7REG, +15REG, ', -15VDC, -3VDC, P-145; 115VAC,
, -151
22
66 to -174

(II)

CATEGORY		PROCEDURE
COMPUTER TURN-ON		11
POWER CHECKS		1, 3, 4, 6
MAIN MEMORY		12, 13, 3, 4, 5, 8
CONTROL MEMORY		12, 13, 6
TIMING	MAIN	7
	MAIN MEMORY	8
	CONTROL MEMORY	6
	I/O ACK	9
PC CARD TESTS		14, 15, 16
INTERMITTENT CONDITION		14, 15, 16
ABNORMAL CONDITION OR VOLTAGE FAULT		2, 5
DIAGNOSTIC PROGRAM ANALYSIS		17
INTERCOMPUTER LOAD		10
MANUAL WRITING		18
MANUAL READING		19
INSPECT AND CHANGE		20
I/O		9, 10

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14. 7002013 PCC TEST. Refer to paras 7-39A, 7-39B, 7-39C, figure 7-14A, and tables 7-9A and 7-9B.

15. 7002060 PCC TEST. Refer to paras 7-39A, 7-39B, 7-39D, figure 7-14A, and tables 7-9A and 7-9C.

16. 7002070 PCC TEST. Refer to paras 7-39A, 7-39B, 7-39D, figure 7-14A, and tables 7-9A and 7-9D.

17. Program analysis. Refer to para 7-36.

18. Manual loading (writing) into addresses. Refer to para 7-41.

19. Manual reading from addresses. Refer to para 7-42.

20. Inspect and change routine. Refer to para 7-43 and table 7-10.

7-36. PROGRAM ANALYSIS. Whenever the Diagnostics Program loads but fails to pinpoint the error location in the fault isolation tables, the operator can implement manual troubleshooting procedures. An essential step in manual troubleshooting is to analyze the program. A listing of the Diagnostics Program can be found in volume 2 part 2A and a description of the routines and subroutines can be found in volume 1 chapter 5. By studying the program listing, the operator may narrow the search to a failing routine or to an instruction. When the diagnostics detect but fails to isolate the casualty, the computer will be in one of several conditions: Program Stop, Program Run (Loop or Halt), Fault or Program Run and Fault. The following subparagraphs explain the methods used to analyze the different conditions.

1. Program Stop. Record P Register and, using program listing, determine what subroutine is failing, then analyze subroutine to determine what function of the computer is being tested. Run through subroutine in OP STEP mode by following manual troubleshooting procedures to locate faulty instruction, then phase-step the instruction to determine failure. Replace faulty module and re-run diagnostics routine.

2. Program Run (Loop). If running computer is looping, set OP STEP mode and step computer to determine looping area. Refer to program listing and determine if loop is within the address limits of the program being run. If not within address limits, attempt to determine what caused program to jump outside its limits, then reload diagnostics and rerun program. If within program limits, using program listing, determine if any instructions were changed. If instructions were changed, attempt to determine cause of instruction change (i.e., bits picked up or dropped, etc.) before reloading and rerunning the program. If, on the other hand, no instructions were changed, run through the subroutines in OP STEP mode to determine the failing instruction. Next, use PHASE STEP mode to isolate the faulty instruction and associated modules and rerun the diagnostics routine.

3. Program Run (Halt). Use Program Stop procedure.

4. Fault or Program Run and Fault. Using program listing, attempt to determine why computer faulted. If possible, try to determine which subroutine is failing and then OP STEP or PHASE STEP until an error is found.

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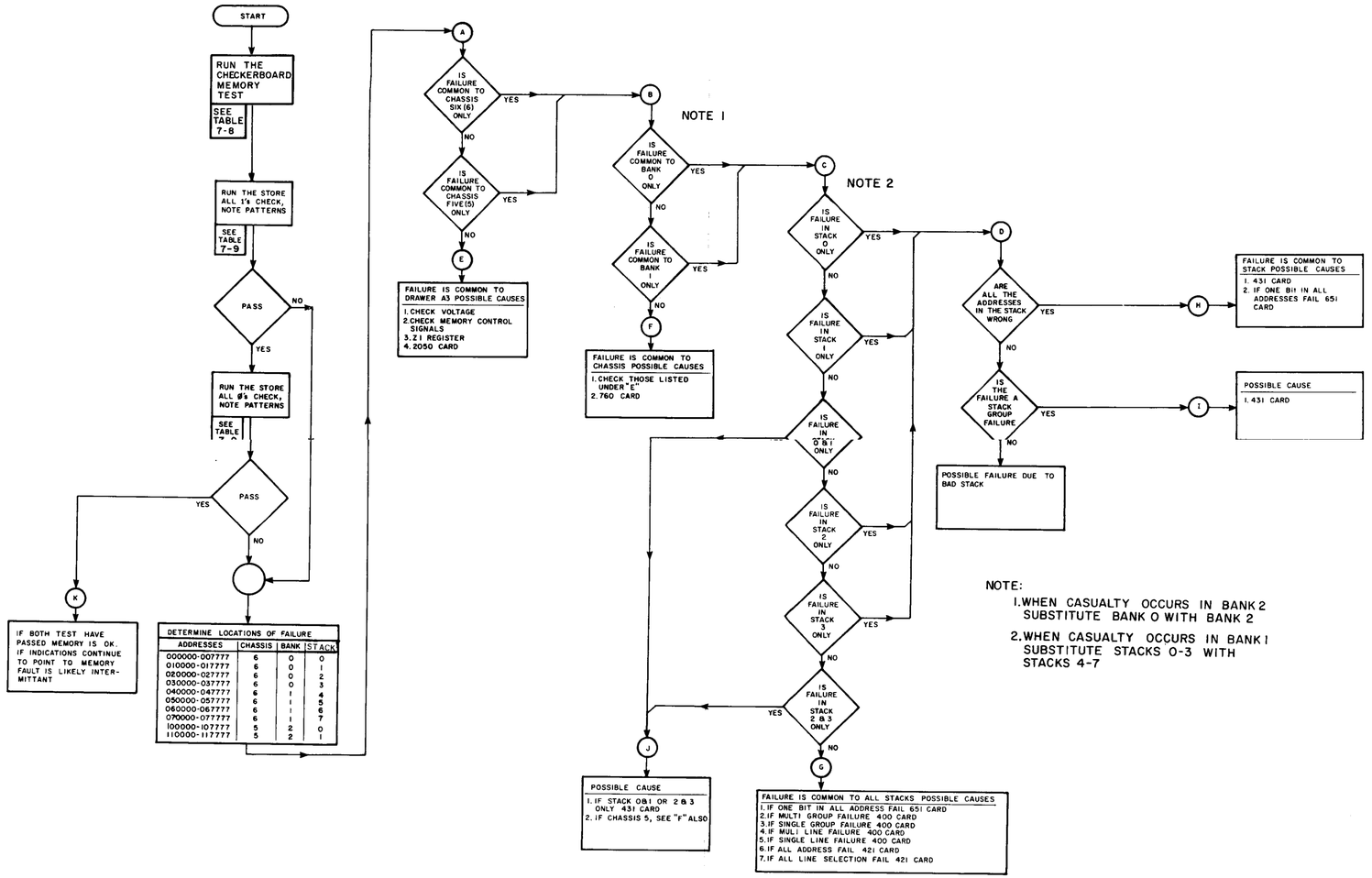


Figure 7-13. Memory Test Flow Chart

TABLE 7-8. CHECKERBOARD MEMORY TEST

Step	Procedure	Comment
1	Turn POWER ON at Power Control Panel (A5).	
2	Place INDICATE INDICATE/SET switch to the INDICATE/SET position.	Switch located in Power Control Panel (A5)
3	Place the following switches and indicator switches as shown:	
	Switch/ indicator — Position	
	BOOTSTRAP MODE — MAIN MEMORY	Control Panel 2 (A4)
	RTC DISC — DISC (UP)	Control Panel 2 (A4)
	EXT SYNC DISC — DISC (UP)	Control Panel 2 (A4)
	DISC ADV P — DISC (DOWN)	Control Panel 1 (A2)
	FUNCTION REPEAT — DOWN	Control Panel 1 (A2)
	MODE — RUN	Control Panel 1 (A2)
4	Master Clear Computer.	
5	Place f = 40 in Function Code register.	Control Panel 1 (A2)
6	Place FUNCTION REPEAT switch up.	
7	Momentarily place RESTART START STEP to START STEP.	Clear MEMORY
8	Place SEQ STEP/STOP switch to STOP.	
9	Master Clear Computer.	
10	Place f = 44 in Function Code register.	
11	Place 777777_8 in AL.	Control Panel 1 (A2)
12	Hold P register bit O.	Control Panel 1 (A2)
13	While holding P register bit O, momentarily place RESTART/ START STEP to START STEP.	Places negative zero in all odd locations.

TABLE 7-8. CHECKERBOARD MEMORY TEST (Cont'd)

Step	Procedure	Comment
14	Place SEQ STEP/STOP switch to STOP.	
15	Release P register bit 0.	
16	Master Clear Computer.	
17	Place f = 14 in Function Code register.	
18	Momentarily place RESTART/START STEP switch to START STEP. NOTE: AL should remain clear. If AL does not remain clear, run the memory tests in Table 7-9 to determine fault pattern.	
19	Place SEQ STEP/STOP switch to STOP.	
20	Master Clear Computer.	
21	Place f = 44 in Function Code register.	
22	Place 777777_8 in AL.	
23	Repeat steps 7 through 9.	Stores negative zero in memory.
24	Ensure AL is clear.	
25	Repeat steps 12 through 19.	In step 13, a positive zero will be placed in odd locations.
26	Place FUNCTION REPEAT switch down.	
27	Master Clear Computer.	

TABLE 7-9. MANUAL MEMORY TEST PROCEDURE

Step	Procedure	Observation
	PRELIMINARY	
1	Energize computer by pressing POWER switch to ON.	POWER indicator is lit.
2	Ensure the following switches are positioned as described:	
	INDICATE-OFF-INDICATE/SET	INDICATE/SET (Down)
	SEQ STEP-STOP	Neutral
	RESTART-START STEP	Neutral
	FUNCTION REPEAT	Down
	PHASE REPEAT	Down
	DISC ADV P	Down
	EXT SYNC	DISC (Up)
	RTC	DISC (Up)
	BOOTSTRAP MODE	MAIN MEMORY (Down)
3	Ensure peripheral equipments are disabled to prevent external interrupts from disturbing memory.	All I/O indicators on the I/O front panel(s) remain clear after step 4 is performed.
4	Press I/O CLEAR-MASTER CLEAR switch to MASTER CLEAR.	All I/O front panel indicators are clear.
5	Position FUNCTION REPEAT switch up.	
	STORE ONES IN MEMORY	
6	Press RUN MODE indicator.	RUN MODE indicator is lit. I SEQ DES indicator is lit.

TABLE 7-9. MANUAL MEMORY TEST PROCEDURE (Cont'd)

Step	Procedure	Observation
7	Set FUNCTION CODE Register to $44_{(8)}$.	FUNCTION CODE Register = $44_{(8)}$.
8	Set AL Register to $777777_{(8)}$.	AL-Register = $777777_{(8)}$.
9	Press RESTART-START STEP switch to START STEP.	P-Register advances at high speed. PROGRAM RUN indicator is lit.
10	Press SEQ STEP-STOP switch to STOP.	P-Register stops advancing. PROGRAM RUN indicator is extinguished.
	CHECK CONTENTS OF MEMORY	
11	Press OP STEP MODE indicator.	OP STEP MODE indicator is lit.
12	Set FUNCTION CODE Register to $12_{(8)}$.	FUNCTION CODE Register = $12_{(8)}$.
13	Clear P- and AL-Registers.	P- and AL-Registers = 0.
14	Turn RESTART SPEED CONT knob fully counter-clockwise.	
15	Position RESTART-START STEP switch to RE-START.	P-Register advances slowly. AL-Register = 1 for store ones, 0 for store zeros.
16	Adjust RESTART SPEED CONT knob as desired. NOTE: Do not advance P too rapidly or errors may not be displayed in AL-Register long enough to be observed.	P-Register advances faster when knob is turned clockwise, advances slower when turned counter-clockwise.

TABLE 7-9. MANUAL MEMORY TEST PROCEDURE (Cont'd)

Step	Procedure	Observation
17	Inspect all addresses and note locations and patterns of any failing addresses.	Contents of AL-Register should = $777777_{(8)}$ for Store One's or 000000 for store Zeroe's.
18	Return RESTART-START STEP switch to neutral.	P-Register stops advancing.
	STORE ZEROE'S IN MEMORY	
19	Press RUN MODE indicator.	RUN MODE indicator is lit.
20	Set FUNCTION CODE Register to $44_{(8)}$.	FUNCTION CODE Register = $44_{(8)}$
21	Clear AL-Register.	AL-Register = 000000.
22	Press RESTART-START STEP switch to START STEP.	P-Register advances at high speed.
23	Press SEQ STEP-STOP to STOP.	P-Register stops advancing.
	CHECK CONTENTS OF MEMORY	
24	Perform steps 11 through 18.	
25	Return all switches to normal.	

7-39A. PRINTED CIRCUIT CARD TESTS. Several Printed Circuit Card (PCC) tests are presented herein as supplementary troubleshooting aids. They are recommended for use only after normal troubleshooting practices such as diagnostic tests, maintenance turn-on procedure, and memory checks have been tried unsuccessfully to isolate a particular casualty. Each PCC test consists of a short program designed to energize pertinent logic gates so that the maintenance technician can observe and qualitively analyze the gate output waveforms on an oscilloscope. Table 7-9A specifies switch positions for the tests. Figure 7-14A presents several examples of abnormal output pulses that may be encountered during performance of these tests.

7-39B. Test Notes. The following factors can affect PCC test validity. They should be carefully considered when analyzing pulse oscilloscope waveforms.

1. Pulse Characteristics. The ideal pulse amplitude is 0 volts to -4.5 volts (negative or positive - going pulse). Unless otherwise noted, all pulse widths should be at least 0.07 usec wide and no less than 4 volts in amplitude. If a pulse does not meet these criteria, either replace the card immediately or monitor it closely as a future source of trouble. Before rejecting a card however, check to ensure that none of the inputs and outputs are the source of trouble.

2. Pulse Differences. Many of the pulses shown in the PCC test tables may appear slightly different in width or shape. Minor differences may be due to computer timing, type of oscilloscope and adjustment of equipment. However, unless otherwise noted, all pulses should meet minimum amplitude and width criteria as illustrated in the tables.

3. Procedure after Special Instruction. After each special instruction such as stopping the program, depressing a lamp, positioning a switch, or grounding a test block, always proceed as follows: Remove any ground; reposition switches to their initial position; and stop, master clear, and restart the program prior to continuing with the test.

4. Reference OP. For Test Block (TB), Plate (P) Number, and Gate, refer to OP 3514 Volume 2 Part 3, First revision.

5. Scope Settings. Slope and scale indicate suggested settings on oscilloscope. Unless otherwise noted, scale setting and pulse width are in usec measured at the 50% point.

6. Grounded Scope Probe. Ensure that the scope probe is grounded for all measurements.

7. Applicability of Tests. Each test was designed to check 16 I/O channels; however, if a particular computer has only 8 I/O channels, all references to chassis A8A1(9) and A8A2(10) can be disregarded. Unless otherwise noted, measurements are the same for all I/O chassis.

7-39C. 7002013 PCC TEST. The 7002013 PCC test (Table 7-9B) provides all necessary instructions and test points for energizing and observing the 7002013 PCC logic gate output pulses as well as waveforms for comparison. This test is especially useful for troubleshooting intermittent computer casualities. The output logic gates of a defective 7002013 PCC tend to decrease in amplitude and width. This deterioration of an enabling signal can result in intermittent troubles such as computer faults and loading problems which are difficult to isolate through use of normal troubleshooting procedures.

7-39D. 7002060 AND 7002070 PCC TESTS. Both the 7002060 PCC test (Table 7-9C) and the 7002070 PCC test (Table 7-9D) comprise a short computer program designed to energize relevant logic gates. The tests identify pertinent test points and provide all instructions necessary for monitoring the PCC output logic pulses. Waveforms are included for analysis. Neither test should be performed until after all other troubleshooting procedures such as are normally employed have failed to isolate a casualty.

7-40. MANUAL PROGRAMING. By studying the program listing, the operator can often narrow his search to one instruction or area of the computer. The operator may have to write a small program and manually enter it to aid in trouble isolation. The following subparagraphs provide:

1. Methods for manually entering programs.
2. A manual method for use in reading from memory.
3. A short inspect-and-change routine.

7-41. Manual Loading (Writing) Into Addresses. The procedure for manually entering a word into storage can be varied. One way is with a Store AL (f=44) instruction using the following procedure:

1. Press SEQ STEP/STOP switch to STOP.
2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.
3. Set the P register to one less than the address of the desired storage address.
4. Set the FUNCTION CODE register to 44_8.
5. Place FUNCTION REPEAT switch in the up position.
6. Press MODE OP STEP switch.
7. Set the word to be stored in AL register.
8. Press RESTART/START STEP switch to START STEP. (Repeat step 8 for first-time operation.)

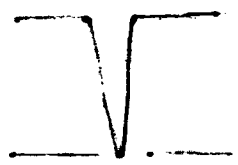
With step 8 completed, the computer stops and the word in the AL register is transferred to the desired memory location. To repeat the procedure, perform steps 7 and 8 only.

7-42. Manual Reading From Addresses. Manual reading into the AL register involves the use of the ENTER AL instruction (f=12). With this instruction, the contents of any memory address can be observed through use of the following procedures:

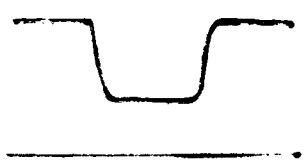
1. Press SEQ STEP/STOP switch to STOP.
2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.
3. Set the P register to one less than the address of the word to be entered into the AL register.

TABLE 7-9A. SWITCH POSITIONS FOR THE 7002013, 7002060, and 7002070 PC CARD TESTS.

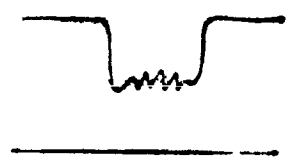
Power Panel (A5)	
SWITCH	POSITION
POWER	ON
DISC ALARM-RESET ALARM	NEUTRAL
BATTLE SHORT	OFF
INDICATE-OFF-INDICATE/SET	INDICATE/SET
Control Panel 1 (A2)	
FUNCTION REPEAT	DOWN
PHASE REPEAT	DOWN
AUTO RECOVERY	DOWN
DISC ADV P	DOWN
MODE	RUN
Control Panel 2 (A4)	
PROGRAM STOPS	DOWN
PROGRAM SKIPS	DOWN
EXT SYNC DISC	UP
RTC DISC	UP for 7002060 and 7002070 DOWN for 7002013
BOOTSTRAP	NDRO
I/O Panel (A1)	
CHANNEL INTER-COMPUTER/ CHANNEL NORMAL	CHANNEL NORMAL
CHANNEL FUNCTION	SINGLE



NARROW PULSE

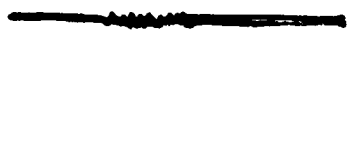


LOW AMPLITUDE



LOW AMPLITUDE AND RINGING

CHANGING AMPLITUDE



CONSTANT HIGH

CONSTANT LOW

Figure 7-14A. Abnormal Output Pulses

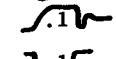
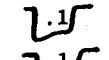
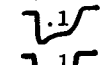
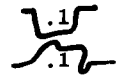
TABLE 7-9B
7002013 Printed Circuit Card Test

1. At Computer Mk 152, enter the following program (Refer to Paragraph 7-41 for loading procedures):

Location	Instruction	Location	Instruction
4000	503400	4032	000002
4001	360366	4033	000002
4002	124012	4034	124037
4003	450011	4035	040001
4004	734003	4036	444037
4005	124057	4037	501200
4006	440012	4040	000004
4007	400014	4041	000004
4010	400015	4042	124045
4011	501400	4043	040001
4012	503000	4044	444045
4013	503600	4045	502600
4014	503200	4046	504400
4015	507310	4047	505600
4016	507201	4050	510000
4017	360017	4051	020000
4020	700017	4052	614053
4021	504722	4053	240000
4022	124025	4054	260000
4023	040001	4055	734020
4024	444025	4056	344013
4025	501600	4057	764060
4026	124031	4060	000000
4027	040001	4061	400015
4030	444031	4062	501400
4031	501100	4063	544060

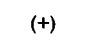
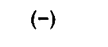
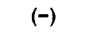
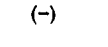
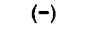
2. Position computer switches as shown in Table 7-9A.
3. Set P Register equal to 004000_8.
4. Ensure that all peripheral equipment is maintained in a strict off-line condition.
5. Momentarily set RESTART/START STEP switch to START STEP. Program RUN lamp should now be lit.
6. Use an oscilloscope to monitor and analyze pulses at the specified test blocks for abnormal indications as defined in Test Notes (para. 7-39B).

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

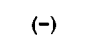
TB1	Slope	Scale	Pulse	Plate No.	Gate
12F	(-)	.1		6	9gC03
12G	(-)	.1		6	9gC02
17G	(-)	.1		6	9gN61
18F	(-)	.1		6	9gN63
20E	(+)	.1		58	g3N60
20F	(-)	.1		58	9gN62
21D	(-)	.1		58	g4N60
21F	(-)	.1		58	9gN64
31C	(+)	.1		68	3gN50

NOTE: To monitor TB1 32C press and hold FUNCTION PRIORITY indicator/switch EI ODD for chassis (1) or (9) or EI EVEN for chassis (2) or 10).

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
32C	(+)	.1		68	3gN51
32D	(-)	.1		6	8gC04
32E	(-)	.1		6	8gC03
32F	(-)	.1		6	8gC02
32G	(-)	..1		6	8gC01

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
1E	**			60	9gJ12
12G	(-)	.1		58	1gE70
13C	(-)	.1	.06 usec or greater	59A	33Gg0

** High level signal
*** Low level signal

TABLE 7-9B
7002013 Printed Circuit Card Test (Continued)

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
14B	(-)	.1	.3	59A	33Gg1
14C	(-)	.1	.1	59	31Gg0
15C	(-)	.1	.1	59A	31Gg1
16C	(-)	.1	.1	59	31Gg2
17B	(-)	.1	.4	59	33Gg2
17C	(+)	.1	.12	59	33Gg3
18B	(-)	.1	.4	59	31Gg8
18D	(-)	.1	.4	60	33Gg5
19C	(-)	.1	.1	59	31Gg3
21C	(-)	.1	.35	60	33Gg6

NOTE: To monitor TB2 23C press and hold FUNCTION PRIORITY indicator/switch EI ODD for chassis (1) or (9) or EI EVEN for chassis (2) or (10).

23C	(-)	.1	.5	58	2gN49
24C	(-)	.1	.4	58	2gN48
24D	***			60	8gJ12
26D	(+)	.5	2.0	70	63Lg0
32A	(+)	5.0	20.0	69	55Lg0

Chassis A2A1(3) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
3C	(-)	.1	.1	13	11E25
3G	(-)	.1	.1	13	00E25
3E	(-)	.1	.1	13	42E20
3F	(+)	.1	.1	13	31E20
4G	(+)	.1	.1	12	09E20
5G	(-)	.1	.1	12	12E20
6G	(-)	.1	.1	12	22E20
7B	(-)	.5	2	14	05G25
7E	(-)	.5	2	14	15G25
7G	(-)	2.0	1.5	14	11E20
8G	(-)	.1	.5	16	21T22
9A	(-)	.1	.5	16	21T42
9B	(-)	.1	.4	16	21T34
9D	(-)	.1	.4	16	21T24
9E	(-)	.1	.5	16	21T14
10D	(-)	.5	2	16	03G23

Chassis A2A1(3) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
10F	(+)	.5	2.0	16	13G22
10G	(+)	.5	2.0	16	03G22
11C	(+)	.1	.1	40	08N16
11F	(-)	.1	.1	40	29N16
11G	(-)	.1	.1	40	19N16
12F	(-)	.2	1.4	41	09F50
13F	(-)	1.0	3.5	41	09F40
13G	(-)	.2	1.4	41	09F70
14A	(-)	.2	1.4	43	03F00
15A	(+)	.2	1.4	43	02F00
15C	(+)	.5	.5 1.5	43	02F06
15D	(-)	.1	.6	42	09F01
15B	(+)	.1	.7	43	03F06
15E	(-)	1.0	3.5	42	09F23
15F	(+)	.1	.7	42	09F45
15G	(-)	.2	1.4	42	09F67
19A	**			7	05J11
19B	***			7	04J11
21B	(-)	5.0	5.0 32.0	45	21F26
23D	(-)	2.0	14.0	45	21F24
31A	(-)	.1	.1	4	71C14
32A	(-)	.1	.1	4	32J06
32D	(-)	.1	.1	4	71C04
32E	(-)	.1	.1	4	71C03
32F	(-)	.1	.1	4	71C02
32G	(-)	.1	.1	4	71C01

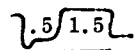
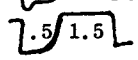
Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
6F	(-)	.1	.1	29	10E34
18G	(+)	.5	2.0	15	03G20
21G	(+)	.5	2.0	15	13G20
26G	(-)	.5	.5 1.5	15	11T34
27G	(-)	.5	.5 1.5	15	13T34
28E	(-)	.5	.5 1.5	8	03T11
29B	(-)	.5	.5 1.5	9	03T22
29F	(-)	.5	.5 1.5	15	11T44

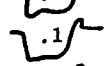
** High level signal
*** Low level signal

TABLE 7-9B
7002013 Printed Circuit Card Test (Continued)

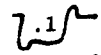
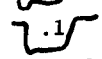
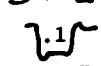
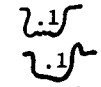
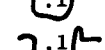
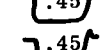
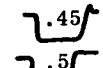
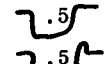
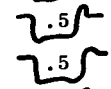
Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
29G	(-)	.5		15	11T42
30G	(-)	.5		15	13T44

Chassis A2A2(4) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
20A	(-)	.1		20	29N04
20B	(+)	.1		20	09N05
20C	(+)	.1		20	09N04
21A	(-)	.1		20	29N05
21B	(-)	.1		20	19N05
21G	(-)	.1		20	19N04
24C	(-)	.1		21	29N07
24D	(-)	.1		21	19N07
24G	(+)	.1		21	09N07

Chassis A2A4(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
12A	(-)	.1		18	38N02
12B	(-)	.1		18	39N02
12C	(-)	.1		18	49N02
12D	(-)	.1		18	29N02
12E	(-)	.1		18	19N02
12F	(-)	.1		18	09N02
19F	(+)	.1		19	09N06
19G	(-)	.1		19	09N03
22A	(-)	.1		19	49N06
22B	(-)	.1		19	49N03
22C	(-)	.1		19	39N06
22D	(-)	.1		19	39N03
22E	(-)	.1		19	29N03
22F	(-)	.1		19	19N03
24A	(-)	.1		17	59N01
24B	(-)	.1		17	79N01
24C	(-)	.1		17	49N01
24D	(-)	.1		17	39N01
24E	(-)	.1		17	29N01
24F	(-)	.1		17	19N01

Chasis A2A4(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
25A	(+)	.5		26	49N09
25B	(-)	.1		26	09N09
25C	(-)	.5		26	19N09
25F	(-)	.1		38	19E40
25G	(-)	.1		38	19E44
25D	(-)	.1		26	29N09
25E	(-)	.5		26	39N09
32C	(-)	.1		5	94C04
32D	(-)	.1		5	84C04
32E	(-)	.1		5	84C03
32F	(-)	.1		5	84C02
32G	(-)	.1		5	84C01

Chassis A4A1(7) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
1E	(-)	.1		14	51T24
1F	(-)	.1		14	51T21
1G	(-)	.1		14	51T13
2E	(-)	.1		23	18N13
2F	(-)	.1		23	19N13
2G	(-)	.1		23	09N13
3C	(-)	.1		23	39N13
3D	(-)	.1		23	29N13
3E	(-)	.1		23	11N13
3F	(-)	.1		23	17N13

NOTE: To monitor TB1 4B depress and hold FUNCTION PRIORITY indicator/switch EI ODD.

4B	(-)	.1		22	39N12
4C	(-)	.1		22	37N12
4E	(-)	.1		22	29N12
4F	(-)	.1		22	19N12
5G	(-)	.1		22	09N12
6A	(-)	.1		106	10E19
6E	(-)	.1		22	49N12
10C	(-)	.1		31	10E60
10D	(-)	.1		31	00E60

TABLE 7-9B
7002013 Printed Circuit Card Test (Continued)

Chassis A4A1(7) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
NOTE: TB1 15F will be a low level and TB1 15G will be a high level for MODs 1 and 5. There will be a pulse for MODs 0, 2, 3 and 4.					
15F				50	16V34
15G				50	17V34
23F	(-)	.5	2	14	12G19
25F	(-)	.1	.1	37	09N15
25G	(-)	.1	.1	37	19N15
26F	(-)	.1	.1	37	09N14
27E	(-)	.1	.1	37	39N14
27F	(-)	.1	.1	37	19N14
27G	(-)	.1	.1	37	29N14
30F	(-)	.1	.5	14	53T13
31D	(-)	.1	.1	6	95C04
31E	(-)	.1	.1	6	95C03
31F	(-)	.1	.1	6	95C02
31G	(-)	.1	.1	6	95C01
32D	(-)	.1	.1	6	85C04
32E	(-)	.1	.1	6	85C03
32F	(-)	.1	.1	6	85C02
32G	(-)	.1	.1	6	85C01

Chassis A4A1(7) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
3G	**			7	09J11
4B	**			7	10J15
7G	(-)	.1	.1	55	21E15
8G	(-)	.1	.1	55	20E15
NOTE: To see pulse at TB2 14F; STOP, hold MASTER CLEAR down, push priority OD ODD.					
14F	(-)	.1	.1	49	13E00
15A	(-)	.1	.1	49	33E00
15C	(-)	.1	.1	49	23EOO
15D	(-)	.1	.1	49	15EOO
15E	(-)	.1	.1	49	14EOO
15G	(+)	.1	.1	49	04EOO
19G	(-)	.1	.1	54	03N41

** High Level Signal
*** Low Level Signal

Chassis A4A2(8) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
5B	(-)	.1	.5	107	30NOO
5C	(+)	.1	.5	107	20NOO
8G	(-)	.1	.1	25	20N11
18G	(+)	.5	2.0	27	02G37
19G	(-)	.5	2.0	27	03G37
24C	(+)	.1	.1	21	09N08
24E	**			21	19N08
24F	(-)	.1	.1	21	29N08
25C	(-)	.1	.1	25	09N11
25D	(-)	.1	.1	25	11N11
25E	(-)	.1	.1	25	17N11
25F	(-)	.1	.1	25	18N11
25G	(-)	.1	.1	25	19N11
26B	(-)	.1	.1	25	29N11
26F	(-)	.1	.1	25	49N10
26D	(-)	.1	.1	25	39N11
27A	(-)	.1	.04 usec or greater	24	09N10
27C	(-)	.1	.1	24	19N10
27G	(-)	.1	.1	24	39N10
27E	**			24	29N10
32G	(-)	.1	.1	6	86C01

Chassis A4A2(8) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
10B				122	33CT10
11A	(-)	.1	.1	122	01ST10
11B	(-)	.1	.15	122	33CT11
11D	(-)	.1	.15	122	33CT13
11C	(-)	.1	.1	122	33CT12
NOTE: To monitor TB2 18G and 20E momentarily depress LOAD MODE indicator/switch.					
18G	(-)	.1	.1	25	49N11
20E	(-)	.1	.1	122	31BT10

NOTE: The 7002013 cards at the locations shown in Column A of the following PCC substitution listing do not have test points for both gates and cannot be properly monitored. However, the cards in Column A can be switched with the cards in Column B and then monitored at the TBs. All are negative-going pulses. Note that some cards have two gates to monitor.

7002013 PC Card Substitution Listing

A	B	PLATE NO.	TB	GATE	TB	GATE
3J13E	3J15F	9	TB2 29B	03T22		
3J15A	3J26A	14	TB1 7B	05G25	TB1 7E	15G25
3J19D	3J27D	12	TB1 5G	12E20	TB1 6G	22E20
3J26B	3J25E	16	TB1 8G	21T22		
3J32D	3J25D	16	TB1 10G	03G22	TB1 9E	21T14
3J32E	3J24A	15	TB2 29G	11T42		
3J33E	3J25A	15	TB2 21G	13G20		
8J2D	8J17D	25	TB1 26B	29N11		
8J16A	8J16D	24	TB1 27G	39N10		

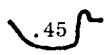
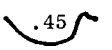
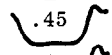
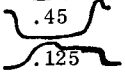
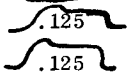
TABLE 7-9C
7002060 Printed Circuit Card Test

1. At Computer Mk 152 enter the following program (Refer to Paragraph 7-41 for loading procedures):

Location	Instruction	Location	Instruction	Location	Instruction
1000	507201	1026	714200	1054	341000
1001	507310	1027	506000	1055	000000
1002	402000	1030	162000	1056	700017
1003	121012	1031	502601	1057	441100
1004	442000	1032	222000	1060	360006
1005	101013	1033	502300	1061	131066
1006	505500	1034	341035	1062	521101
1007	504477	1035	502200	1063	511100
1010	042000	1036	341037	1064	451066
1011	241000	1037	502100	1065	731061
1012	262000	1040	341041	1066	500100
1013	062000	1041	505200	1067	501500
1014	322000	1042	752002	1070	500200
1015	360001	1043	462002	1071	501600
1016	422002	1044	761055	1072	500300
1017	142000	1045	506200	1073	501700
1020	506300	1046	641047	1074	502700
1021	502000	1047	022000	1075	571100
1022	742002	1050	501100	1076	341060
1023	532000	1051	000000	1077	551055
1024	561001	1052	000000	1100	000000
1025	722000	1053	503000	1101	777700

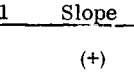
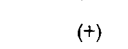
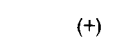
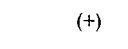
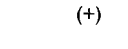
2. Position Computer switches as shown in Table 7-9A.
3. Set P Register equal to 001000_8.
4. Ensure that all peripheral equipment is maintained in a strict off-line condition.
5. Momentarily set RESTART/START STEP switch to START STEP. Program RUN lamp should now be lit.
6. Use an oscilloscope to monitor and analyze pulses at specified test blocks for abnormal indications as defined in Test Notes (para 7-39B).

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

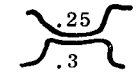
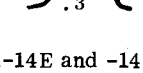
TB1	Slope	Scale	Pulse	Plate No.	Gate
4D	(-)	.1		65	11Vg0
4E	(-)	.1		65	11Vg1
6F	(-)	.1		65	11Vg2
6G	(-)	.1		65	11Vg3
19E	(+)	.1		58	g2N60
20G	(+)	.1		58	8gN65

NOTE: To monitor following TBs stop the program, press SEQ STEP/STOP switch to STOP) and position I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR. For TB1-6D and -6E, on I/O panel Al set E1 MON CHAN 1 for chassis (1) and (9) or CHAN 0 for chassis (2) and (10). For TB1-4F, set CHAN 5; and for TB1-4G and 5G, set CHAN 7 for chassis (1) and (9) or CHAN 6 for chassis (2) and (10). Always master-clear after each channel is set.

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
6D	(+)	.2		65	12Vg0
6E	(+)	.2		65	12Vg1
4F	(+)	.2		65	14Vg2
4G	(+)	.2		65	14Vg3
5G	(+)	.2		65	10Vg3

NOTE: To monitor TB1-15F and -15G, stop the program, master-clear and, on I/O Panel A1, press and hold (together) FUNCTION PRIORITY E1 ODD, E1 EVEN, OD ODD, and OD EVEN indicator switches.

15F	(-)	.1		66	10Vg4
15G	(+)	.1		66	12Vg6

NOTE: To monitor TB1-14E and -14F, stop the program, ground TB1-8F on chassis being monitored, and then master-clear.

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
14E	(+)	.1	.55	66	10Vg0
14F	(+)	.2	1.5	66	11Vg4

Chassis A1A1(1), A1A2(2), A8A1(9), and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
4E	(-)	5.0	20.0	65	54Lg0
13B	(-)	.1	.4	59A	30Gg0
15B	(-)	.1	.35	59A	30Gg1
16B	(-)	.1	.4	59	30Gg2
17D	(+)	.2	.6	60	30Gg5
19B	(+)	.1	.12	59	30Gg3
20B	(+)	.1	.12	60	30Gg4
21B	(-)	.1	.35	60	30Gg6
28C	(+)	.1	.6	69	52Lg1
28D	(-)	5.0	15	69	53Lg2
33B	(+)	.1	.12	68	3gN48

NOTE: To monitor TB2-19D, -30D, -31C, -31D, -32C, and -32D, ground TB2-E14 on chassis A4A1(7). For TB2-32D on chassis (2) and (10) also stop program and hold MASTER CLEAR.

19D	(+)	.1	.12	69	72Lg1
30D	(+)	.1	.12	69	74Lg0
31C	(+)	.1	.12	69	74Lg1
31D	(+)	.1	.12	69	74Lg2
32C	(+)	.1	.12	69	74Lg3
32D	(+)	.1	.12	69	72Lg0

NOTE: To monitor TB2-27C and -31B, stop program; on I/O Panel A1, press and hold FUNCTION PRIORITY ID ODD indicator-switch for chassis (1) and (9) or ID EVEN for chassis (2) and (10).

27C	(+)	.1	.5	68	9gN49
31B	(+)	.1	.12	68	3gN49

NOTE: To monitor TB2-22B, stop the program, master-clear and, on I/O Panel A1, press and release FUNCTION PRIORITY EI ODD or EI EVEN indicator switch.

22B	(+)	.2	1.0	60	30Gg7

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate

NOTE: To monitor the following TBs, stop the program, master-clear and, on I/O Panel A1, depress EI MON, EF MON, OD MON, and ID MON indicator switches for all channels

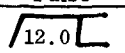
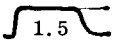
2E	(+)	.1	.5	61	22Mg0
3E	(+)	.1	.5	61	32Mg0
3F	(+)	.1	.5	61	02Mg0
5E	(+)	.1	.5	62	22Mg1
6E	(+)	.1	.5	62	32Mg1
6F	(+)	.1	.5	62	02Mg1
8E	(+)	.1	.5	63	22Mg2
9E	(+)	.1	.5	63	32Mg2
9F	(+)	.1	.5	63	02Mg2
11E chassis (1) and (9) only	(+)	.2	1.5	64	22Mg3
11E chassis (2) and (10) only	(+)	.1	.5	64	22Mg3
12E chassis (1) and (9) only	(+)	.2	1.5	64	32Mg3
12E chassis (2) and (10) only	(+)	.1	.5	64	32Mg3
12F chassis (1) and (9) only	(+)	.2	1.5	64	02Mg3
12F chassis (2) and (10) only	(+)	.1	.5	64	02Mg3
21F	(+)	.1	.5	38	12Mg0
22F	(+)	.1	.5	38	12Mg1
23F	(+)	.1	.5	38	12Mg2
24F chassis (1) and (9) only	(+)	.2	1.5	38	12Mg3
24F Chassis (2) and (10) only	(+)	.1	.5	38	12Mg3
19F	(+)	.2	1.5	66	11Vg7

NOTE: To monitor TB2-19F on chassis (2) and (10) depress only EI MON CHAN 0 indicator-switch on I/O Panel A1. Pulse will be .5 usec.

NOTE: To monitor TB2-7E, ground TB2-A14 on chassis A4A1(7) and depress and hold FUNCTION/CHANNEL clear pushbutton on Control Panel 2.

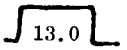
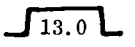
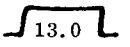
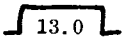
TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

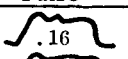
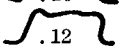
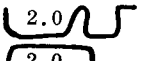
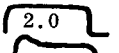
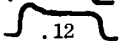
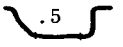
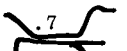
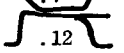
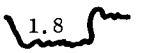
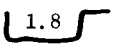
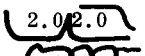
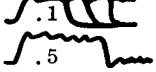
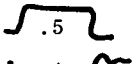
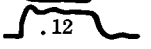
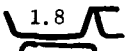
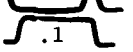
TB2	Slope	Scale	Pulse	Plate No.	Gate
7F	(+)	2.0		70	64Lg0
Chassis (1) and (9) only					
7E	(+)	.2		70	64Lg0
Chassis (2) and (10) only					

NOTE: To monitor the following TBs, connect a jumper wire from TB2-20A on chassis being monitored to TB2 on the same chassis as follows:

CAUTION: TB2-20A is a -15 volt pulse, therefore ensure jumper is connected to correct TB.

1D	(+)	5.0		61	23Rg0
Connect -20A to TB2-25E.					
4D	(+)	5.0		62	23Rg1
Connect -20A to TB2-27E.					
7D	(+)	5.0		63	23Rg2
Connect -20A to TB2-29E.					
10D	(+)	5.0		64	23Rg3
Connect -20A to TB2-31E.					

Chassis A2A1(3) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
2F	(+)	.1		13	53g20
3D	(+)	.1		13	30E20
4A	(-)	.5		14	43G20
4D	(+)	.5		12	20G24
4F	(+)	.1		12	08E20
5F	(-)	.1		12	01E20
6E	(-)	.1		12	20G20
7A	(+)	.1		14	07G25
8B	(-)	.5		14	03G25
8E	(-)	.5		14	13G25
9C	(-)	.5		16	15G23
9F	(+)	.1		16	45G20
9G	(+)	.2		16	20T14
10A	(+)	.1		27	12E33
10B	(-)	.1		40	05N16
10C	(+)	.1		40	06N16
10E	(-)	.5		16	05G22
11B	(+)	.1		40	10N16

Chassis A2A1(3) TB1

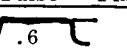
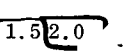
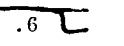
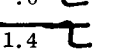
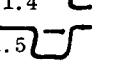
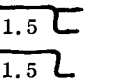
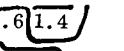
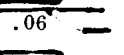
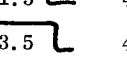
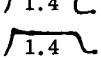
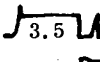
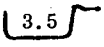
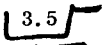
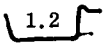
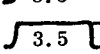
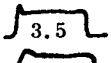
TB1	Slope	Scale	Pulse	Plate No.	Gate
12C	(+)	.1		41	95F00
13D	(+)	.5		41	08F10
14D	(+)	.1		41	08F00
14E	(+)	.2		41	08F20
14F	(+)	.5		41	08F30
14G	(+)	.2		41	08F60
16A	(+)	.2		44	16F13
16D	(+)	.5		44	61F10
16E	(+)	.2		44	42F20
17B	(+)	.1		44	16F14
17C	(-)	.5		44	47F10
17D	(+)	.1		44	20F10
17G	(+)	.5		44	20F04
18A	(+)	.2		44	20F16
18B	(+)	.2		44	40F14
18C	(+)	.5		44	20F12
18E	(+)	.2		44	44F20
18F	(-)	.5		44	31F04
19D	(+)	.2		45	16F22
19E	(+)	.2		44	92F02
19F	(+)	.5		44	20F06
19G	(+)	.2		44	40F02
20B	(+)	.5		38	10E40
20D	(+)	.2		45	16F23
20G	(-)	.2		45	97F21
21A	(+)	1.0		45	86F40
21D	(-)	.2		45	31F24
21E	(+)	.5		45	41F20
21F	(+)	.2		45	16F21
22A	(+)	.2		45	71F04
22B	(-)	1.0		45	97F26
22C	(-)	1.0		45	41F24
22G	(-)	.2		45	37F21
23B	(+)	1.0		45	26F26
23E	(+)	1.0		45	20F22
23F	(+)	.2		45	20F20

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A2A1(3) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
24D	(-)	.2		46	91F34
24G	(+)	.2		46	51F30
25A	(-)	.2		46	41F36
25B	(+)	.2		46	20F36
25C	(+)	.2		46	20F34
25D	(+)	.2		46	60F30
25E	(+)	1.0		46	20F32
26B	(-)	.5		47	41F52
26E	(-)	.5		47	31F42
26F	(+)	.5		47	20F42
26G	(-)	.2		46	41F30
27C	(-)	.5		47	27F52
27G	(-)	.5		47	91F06
28B	(+)	.5		47	10F56
28D	(+)	.5		47	10F51
28F	(+)	.5		47	10F44
28G	(-)	.5		47	51F24
29A	(+)	1.0		47	10F57
29B	(+)	1.0		47	10F56
29C	(+)	1.0		47	10F53
29D	(+)	.5		47	10F52
29E	(+)	.1	 .05 to .07	47	10F50
Low amplitude and narrow					
29F	(+)	.5		47	10F45
29G	(+)	.5		47	20F40
30F	(+)	.5		47	10F46
30G	(+)	.5		47	10F42
31D	Low Level			4	21J09
31E	Low Level			4	21J08
31F	Low Level			4	21J07
31G	Low Level			4	21J06
33A	Low Level			4	30J06

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
1C	(+)	.2		48	10F72
2A	(+)	.5		48	10F75

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
2E	(-)	.2		48	37F60
2F	(-)	.2		48	27F61
3B	(-)	.5		48	41F40
3D	(-)	.5		48	21F70
3E	(-)	.2		48	27F62
4B	(+)	.5		48	10F74
4C	(+)	.2		48	10F73
4D	(+)	.2		48	20F70
5C	(+)	.1		34	00E28
5F	(+)	.5		35	20L10
5G	(+)	.1		55	22E15
6G	(+)	.1		29	00E34
8A	(+)	.5		29	92A00
8D	(-)	.1		27	21E32
8F	(-)	.1		27	11E33
8G	(-)	.1		27	01E32
9C	(+)	.1		27	10E37
9D	(+)	.1		27	20E32
9F	(+)	.1		27	10E33
10A	(-)	.1		28	01E70
10B	(-)	.5		28	03G70
10C	(+)	.1		38	10E44
10E	(-)	.1		38	08E44
10F	(+)	.1		38	00E40
10G	(-)	.1		25	31T42
11E	(-)	.1		38	08E40
11F	(-)	.2		36	03L03
12G	(-)	.1		30	31E52
13A	(+)	.1		30	10E51
13C	(+)	.1		30	20E52
13D	(+)	.1		30	10E52
13G	(+)	.1		30	30E52
14A	(+)	.1		53	00E18
14B	(+)	.1		53	01N43
15A	(-)	.2		47	21F56
15B	(+)	.1		23	31N13
15F	(+)	.1		23	13N13

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
15G	(+)	.1	.6	23	12N13
16C	(+)	.1	.5	22	40N12
16F	(+)	.1	.5	22	20N12
17C	(+)	.1	.5	24	30N10
17F	(+)	.2	.6	24	31T31
19A	(-)	.1	.45	17	58N01
19B	(-)	.1	.4	17	78N01
19F	(-)	.1	.4	17	28N01
19G	(-)	.1	.45	17	18N01
20B	(+)	.1	.45	17	50N01
20C	(+)	.1	.45	17	90N01
20E	(+)	.1	.45	17	30N01
21C	(-)	.2	.4 .5	19	28N03
21F	(+)	.1	.5	15	10T31
22A	(+)	.2	1.5	19	40N03
22B	(+)	2.0	10.0	19	30N03
22E	(+)	.1	.45	19	00N03
22F	(+)	.1	.5	18	01N02
23B	(-)	.1	.45	18	37N02
23C	(-)	.1	.45	18	48N02
23E	(+)	.1	.3	18	17N02
23G	(-)	.1	.45	18	18N02
24D	(+)	.1	.5	18	50N02
25B	(-)	.1	.45	20	18N05
25E	(-)	.2	.3	20	18N04
25G	(+)	.2	1.0	20	20N04
26A	(+)	.2	1.0	20	20N05
26C	(+)	.1	.5	20	00N05
26D	(+)	.1	.5	20	00N04
27A	Low Level			21	10N08
27E	(-)	.1	.4	21	18N07
27F	(-)	.1	.5	21	07N07
28G	(+)	.1	.5	8	10T11
30D	High Level			3	05J10

NOTE: To monitor TB2-16A, stop the program, then depress MODE LOAD pushbutton switch.

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
16A	(+)	.5	.5	22	60N12

NOTE: To monitor TB2-32A, stop the program depress MODE OP STEP and position RESTART/START STEP switch to RESTART. Vary RESTART SPEED CONT knob.

32A	Changing high and low level			3	34J10

NOTE: To monitor TB2-30E, press SEQ DES INT switch on Control Panel 1 (A2). Program will fault.

30E	(-)	.1	.1	15	12G21

May be low in amplitude.

Chassis A2A2(4) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
21C	(+)	.1	.1	20	08N05
21F	(+)	.1	.1	20	08N04
22A	(+)	.1	.1	30	20E51
22B	(+)	.2	.8	30	21E51
22C	(+)	.1	.35	30	21G52
22D	(+)	.1	.1	30	20G52
22E	(-)	.1	.3	30	22G52
24E	(+)	.1	.1	21	08N07
24F	Low Level				
25A	(+)	.1	.12	27	02E32

Chassis A2A2(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
22G	(+)	.1	.12	19	08N06
26F	(+)	.1	.5	39	12X05
26G	(+)	.1	.12	38	09E44
27A	(-)	.1	.45	39	03G40
27B	(-)	.1	.45	39	03G41
27C	(-)	.1	.45	39	03G42
27D	(-)	.1	.45	39	03G44
27E	(+)	.1	.125	39	10G45
27G	(+)	.1	.12	38	09E40
28A	(+)	.1	1.0	101	18X06
28B	(+)	.1	.4	101	18X12

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A2A2(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
29D	(-)	.1	.3	101	17X10
29F	(-)	1.0	4.0	101	17X16
29G	(+)	.1	.35	101	18X00

Chassis A4A1(7) TB1

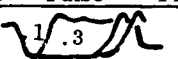
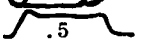
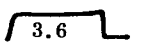
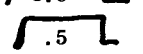
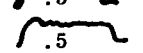
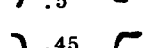
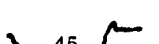
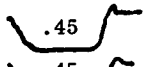
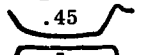
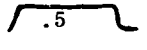
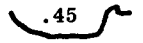
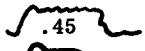
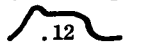
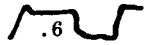
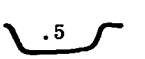
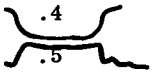
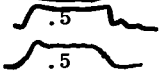
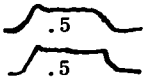
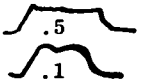
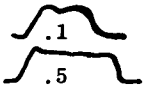
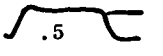
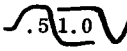
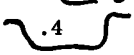
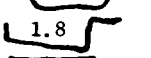
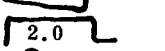
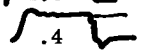
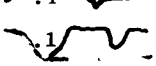
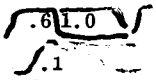
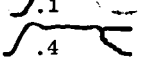
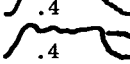
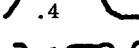
TB1	Slope	Scale	Pulse	Plate No.	Gate
2A	(+)	.1	.5	30	10G57
2B	(+)	.2	.4	30	11G57
2C	(+)	.1	.4	30	12G57
2D	(+)	.1	.35	30	13G57
3A	(-)	.1	.5	23	38N13
5C	(-)	.1	.4	22	36N12
10E	(-)	.5	1.5	31	17G50
15A	(-)	.1	.4	50	21G12
15B	(+)	.1	.6	50	21G13
16B	High level			50	05G10
16E	(+)	.1	.4	50	02G00
16F	(-)	.2	.4 1.0	50	21G10
16G	(-)	.1	.3	50	21G11
17D	(+)	.2	.4	50	20G10
17E	(+)	.1	.4	50	20G11
17F	(+)	.1	.4	50	20G12
17G	(+)	.1	.4	50	20G13
18C	High level			50	15V34
18D	Low level			50	06G10
18G	Low level			52	48G10
19C	Low level			52	44G10
19E	(-)	.5	1.8	52	43G00
19G	Low level			52	46G10
22B	(+)	.5	2.3	28	12G38
22F	(-)	.5	2.0 2.0	107	90S06
23E	Low level			35	11G19
23G	Low level			35	15G19
25D	(+)	.1	.12	37	08K00
27A	(+)	.1	.1	37	06K02
27C	(+)	.1	.1	37	06K04

Chassis A4A1(7) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
NOTE: To monitor TB1-17C, position CHANNEL FUNCTION 0-1 to DUAL on I/O Panel A1.					
17C	(+)	.1	.1	50	09G10
NOTE: To monitor the following TBs, it is necessary to move a PROGRAM STOP switch on Control Panel 2. Position switches 0 through 4 up, one at a time. As each switch is positioned up, the signal level will change from a high to a low level.					
11E		High to Low		32	20G60
11F		High to Low		32	20G61
11G		High to Low		32	20G62
10A		High to Low		32	20G63
10B		High to Low		32	20G64
NOTE: To monitor the following TBs, it is necessary to move a PROGRAM SKIP switch on Control Panel 2. Position switches 1 through 4 up, one at a time. As each switch is positioned up, the signal level will change from a high to a low.					
11A	High to Low			32	12G50
11B	High to Low			32	13G50
11C	High to Low			32	14G50
11D	High to Low			32	15G50
NOTE: To monitor TB1-18B and -19B, stop the program, master-clear, depress and hold FUNCTION PRIORITY OD ODD and OD EVEN switches on I/O Panel A1.					
18B	(+)	.1	.1	50	15V14
19B	(+)	.1	.13	52	42G05
NOTE: To monitor the following TBs, stop the program, master-clear, depress and hold FUNCTION PRIORITY OD ODD switch on I/O Panel A1.					
19D	(-)	.1	.1	52	31G09
20D	(+)	.1	.1	52	30G09
20F	(-)	.1	.1	52	42G10
18E	Low to High			50	14V14
NOTE: To monitor TB1-21G, depress I/O TRANSLATOR DUAL switch on Control Panel 2. Level will change from low to high.					
21G	Low to High			52	42G09

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

Chassis A4A1(7) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
1E	(-)	.1		36	13L00
2B	(+)	.1		26	18N09
2F	(+)	1.0		36	11L03
3A	(+)	.1		26	30N09
3B	(+)	.1		26	10N09
8C	(-)	.1		35	03L10
10G	Low level			34	85L00
11F	(-)	.1		53	02N43
11G	(-)	.1		53	01E18
12A	(+)	.1		53	00N48
12C	(-)	.1		53	01N41
13A	(+)	.1		53	00N40
13G	(+)	.1		53	00E06
15B	(+)	.1		49	32E00
15F	(+)	.2		49	00N65
16A	(-)	.1		49	22E00
16B	(-)	.1		49	12E00
16C	(+)	.1		49	00N64
16D	(+)	.1		49	00N63
16E	(+)	.1		49	00N62
16G	(+)	.1		49	02E00
17C	(+)	.1		49	21E00
17G	(+)	.1		49	01E00
18D	High level			54	15G18
20G	(+)	.5		51	20G05
21B	(-)	.1		28	25E00
22D	(-)	.5		134	05G80
22G	(+)	.5		134	35G80
26D	(+)	.1		51	20G06
26E	(-)	.1		51	20G04
26G	(+)	.2		51	21G06
27B	(+)	.1		51	20G00
27C	(+)	.1		51	20G01
27D	(+)	.1		51	20G02
27E	(-)	.1		51	20G03
27F	(+)	.1		51	03G04
27G	(+)	.1		51	20G07

Chassis A4A1(7) TB2

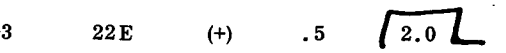
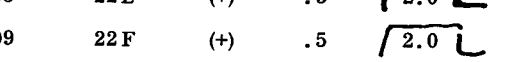
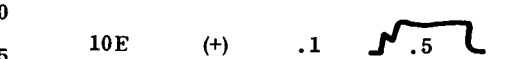
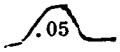
TB2	Slope	Scale	Pulse	Plate No.	Gate
NOTE: Monitor TB2-22D and -22F for approximately 1 minute, pulse will appear and disappear.					
22E	(+)	.5		134	15G80
22F	(+)	.5		134	25G80
NOTE: To monitor TB2-11A, position RTC DISC switch on Control Panel 2 down.					
11A	(+)	.1msec		34	02G29
NOTE: To monitor TB2-14A, stop the program, master-clear, depress and hold FUNCTION PRIORITY ID ODD switch on I/O Panel A1.					
14A	(+)	.1		53	00N49
NOTE: To monitor TB2-10E and -11C, stop the program, master-clear, and ground TB2-C10 on chassis A4A1(7).					
10E	(+)	.1		34	12G28
11C	(+)	.1		34	10E28
NOTE: To monitor TB2-19C, stop the program, master-clear, depress and hold RTC SEQ switch on Control Panel 2.					
19C	(+)	.1		54	10E15
NOTE: To monitor TB2-14D, depress SEQ DES INT switch on Control Panel 1. Program will fault.					
14D	(+)	.1		53	00N41
NOTE: To monitor TB2-4E and -5E, stop the program, position I/O CLEAR/MASTER CLEAR switch to I/O CLEAR. Level will change from high to low for 4E and low to high for 5E.					
4E	High to Low			7	05J12
5E	Low to High			7	04J12
NOTE: To monitor the following TBs, stop the program, master-clear, and ground the TBs in chassis A4A1(7) as follows:					
7A	(-)	.1		55	22G18
Ground TB2-7E					
7B	(-)	.1		55	22G15
Ground TB2-7C					
7D	(-)	.2		55	22G17
Ground TB2-8F					

TABLE 7-9C
7002060 Printed Circuit Card Test (Continued)

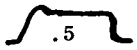
Chassis A4A1(7) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
6F	(+)	.1		5	22G16

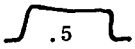
Ground TB2-7F

Pulse at -6F will be low in amplitude and narrow in width.

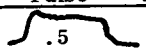
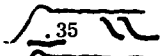
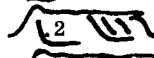
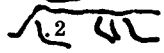
NOTE: To monitor TB2-13F, depress and hold FUNCTION/CHANNEL clear pushbutton switch on Control Panel 2.

13F	(+)	.1		53	00E04

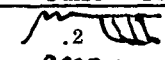
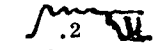
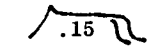
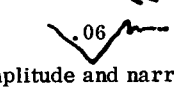
NOTE: To monitor TB2-9A, ground TB1-22B on chassis A4A1(7) and depress INTERRUPT RESUME FAULT switch on Control Panel 2 (A4).

9A	(+)	.1		35	30L10

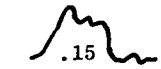
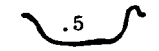
Chassis A4A2(8) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
4G	(+)	.1		107	10N00
10B	(+)	.1		118	11B02
10D	(+)	.1		118	11B04
10F	(+)	.1		118	11B06

Chassis A4A2(8) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
13B	(+)	.1		119	11B08
13D	(+)	.1		119	11B10
13F	(+)	.1		119	11B12
13G	(-)	.1		24	08N10

Pulse will be low in amplitude and narrow in width.

21G	Low level			54	10E17
24B	(+)	1		21	08N08
25A	Low level			25	00N11
26A	(-)	.1		25	28N11
32B	High level			121	92G90
33A	High level			121	00E90

Chassis A4A2(8) TB2

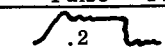
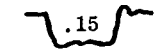
TB2	Slope	Scale	Pulse	Plate No.	Gate
9A	(+)	.1		122	31CT10
11F	(-)	.1		122	32CT11

TABLE 7-9D
7002070 Printed Circuit Card Test

1. At Computer Mk 152, enter the following program (refer to Chapter 7, para 7-41, for loading procedures):

Location	Instruction	Location	Instruction	Location	Instruction
1000	507201	1030	162000	1060	341000
1001	507310	1031	502601	1061	502400
1002	402000	1032	222000	1062	341000
1003	121012	1033	5023000	1063	000000
1004	442000	1034	341035	1064	700017
1005	101013	1035	502200	1065	441106
1006	505500	1036	341037	1066	360006
1007	504477	1037	502100	1067	131074
1010	042000	1040	341041	1070	521107
1011	241000	1041	505200	1071	511106
1012	262000	1042	752002	1072	451074
1013	062000	1043	462002	1073	731067
1014	322000	1044	761063	1074	500100
1015	360001	1045	506200	1075	501500
1016	422002	1046	641047	1076	500200
1017	142000	1047	022000	1077	501600
1020	506300	1050	501100	1100	500300
1021	502000	1051	000000	1101	501700
1022	742002	1052	000000	1102	502700
1023	532000	1053	503000	1103	571106
1024	561001	1054	506100	1104	341066
1025	722000	1055	503600	1105	551063
1026	714200	1056	503200	1106	000000
1027	506000	1057	505001	1107	777700

2. Position computer switches as shown in Table 7-9A.
3. Set P Register equal to 001000_8.
4. Ensure that all peripheral equipment is maintained in a strict off-line condition.
5. Momentarily set RESTART/START STEP switch to START STEP. Program RUN lamp should now be lit.
6. Use an oscilloscope to monitor and analyze pulses appearing at specified test blocks for abnormal indications as defined in Test Notes (para 7-39B).

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

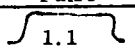
TB1	Slope	Scale	Pulse	Plate No.	Gate
7D	(+)	.1	.45	57	9gN48
7E	(+)	.1	.5	57	9gN44
8E	(-)	.1	.45	57	6gN44
8G	(+)	.1	.5	56	9gN41
10E	(-)	.1	.45	56	6gN43
12E	(+)	.1	.5	56	9gN43
13D	High Level			60	7gJ12
16G	(-)	.1	.45	58	8gN61
17E	(-)	.1	.5	58	g1N60
17F	(-)	.1	.45	58	8gN63
18E	(+)	.5	2.0	58	3gG71
19F	(-)	.1	.45	58	8gN62
21E	(-)	.1	.45	58	8gN64

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

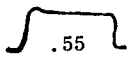
TB1	Slope	Scale	Pulse	Plate No.	Gate
NOTE: To monitor the following TBs STOP Program, master-clear and on I/O Panel A1 individually set and master-clear the following EI MON CHANS. Number in parenthesis after channel number indicates channel to be set for Chassis (2) or (10).					
3F	(+)	.2	.9	65	13Vg2
Set CHAN 5					
3G	(+)	.2	.9	65	13Vg3
Set CHAN 7					
5D	(+)	.2	1.1	65	15Vg0
Set CHAN 1(0)					
5E	(+)	.2	1.1	65	15Vg1
Set CHAN 3(2)					
7F	(+)	.2	1.1	65	15Vg3
Set CHAN 5(4)					

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB1

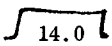
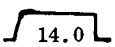
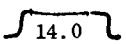
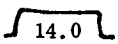
TB1	Slope	Scale	Pulse	Plate No.	Gate
7G	(+)	.2		65	15Vg3
Set CHAN 7(6)					

NOTE: To monitor TB1-14G STOP program, master-clear and on I/O Panel A1 push and release FUNCTION PRIORITY EI ODD for chassis (1) or (9) and EI EVEN for chassis (2) or (10).

14G	(+)	.1		66	8gN61

NOTE: To monitor the following TBs connect a jumper from TB2-20A to TBs on same chassis as follows:

CAUTION: TB2-20A is a -15 volt pulse.

28D	(+)	5.0		61	12Rg0
Jumper to TB1 25D					
28E	(+)	5.0		62	12Rg1
Jumper to TB1 25E					
28F	(+)	5.0		63	12Rg2
Jumper to TB1 25F					
31D	(+)	5.0		64	12Rg3
Jumper to TB1 25G					

NOTE: TB1 31A, 32A, 33A, and 33C applies to chassis (1) and (9) only.

31A	High Level		67	91Vg2
32A	High Level		67	91Vg1

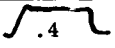
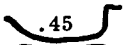
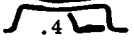
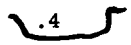
For TB1 33A a pulse should appear as each CHANNEL FUNCTION switch is set to DUAL.

33A	(+)	Variable	67	91Vg0

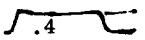
For TB1 33C the level will change from low to high as CHANNEL FUNCTION switch is set to DUAL.

33C		Low to High	67	90Vg3

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

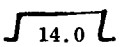
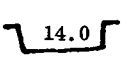
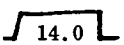
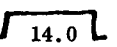
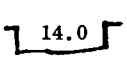
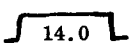
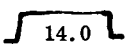
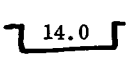
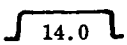
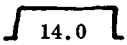
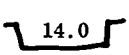
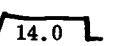
TB2	Slope	Scale	Pulse	Plate No.	Gate
13D	(+)	.1		59	32Gg8
Chassis (1) and (9) only.					
14D	(-)	.1		56	5gN43
15D	(+)	.2		60	31Gg5
16D	(-)	.1		57	5gN44

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
18C	(+)	.1		60	31Gg6
20C	(-)	.1		60	31Gg4
22C	(+)	.1		60	31Gg7
24B	(-)	.1		57	1gE06
26B	High to Low Level			70	91Vg3
Will go low when CHANNEL FUNCTION switch is set to DUAL, ESA or ESI position.					
27B	(-)	.1		69	8gT41
27D	(-)	.1		70	8gT33

NOTE: To monitor the following TBs connect a jumper from TB2 20A on chassis being monitored to TBs on same chassis as follows:

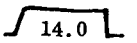
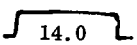
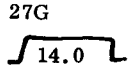
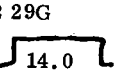
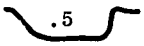
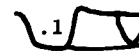
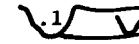
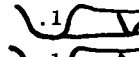
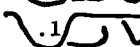
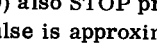
CAUTION: TB2 20A is a -15 volt pulse.

1C	(+)	5.0		61	22Rg0
13E	(-)	5.0		61	24Rg0
Jumper to TB2 25E					
2C	(+)	5.0		61	02Rg0
Jumper to TB2 25F					
4C	(+)	5.0		62	22Rg1
14E	(-)	5.0		62	24Rg1
Jumper to TB2 27E					
5C	(+)	5.0		62	02Rg1
Jumper to TB2 27F					
7C	(+)	5.0		63	22Rg2
15E	(-)	5.0		63	24Rg2
Jumper to TB2 29E					
8C	(+)	5.0		63	02Rg2
Jumper to TB2 29F					
10C	(+)	5.0		64	22Rg3
16E	(-)	5.0		64	24Rg3
Jumper to TB2 31E					
11C	(+)	5.0		64	02Rg3
Jumper to TB2 31F					

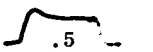
NOTE: To monitor the following TBs, two jumper wires are required. The ground jumper must be connected first and removed last for each TB. The other jumper is connected from TB2 20A on chassis being monitored as follows:

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
CAUTION: TB2 20A is a -15 volt pulse					
3C	(+)	5.0		61	32Rg0
Ground TB2 13F Jumper TB 20A to TB2 25G					
6C	(+)	5.0		62	32Rg1
Ground TB2 14F Jumper TB2 20A to TB2 27G					
9C	(+)	5.0		63	32Rg2
Ground TB2 15F Jumper TB2 20A to TB2 29G					
12C	(+)	5.0		64	32Rg3
Ground TB2 16F Jumper TB2 20A to TB2 31G					
NOTE: To monitor TB2 23B STOP program, master-clear. On I/O Panel A1 hold FUNCTION PRIORITY ID ODD.					
23B	(-)	.1		58	1gN49
NOTE: To monitor TB2 25D, ground TB2 14A on chassis A4A1(7) and depress and hold FUNCTION/CHANNEL CLEAR pushbutton on Control Panel 2.					
25D	(-)	5.0		70	63Lg1
NOTE: To monitor the following TBs ground TB2 14E on chassis A4A1(7). Pulses may be slightly lower in amplitude than other pulses but should be a minimum of 4 volts.					
2F	(-)	.1		61	75Lg0
5F	(-)	.1		62	75Lg1
8F	(-)	.1		63	75Lg2
11F	(-)	.1		64	75Lg3
33A	(-)	.1		69	73Lg1
33C	(-)	.1		69	73Lg0
For Chassis (2) and (10) also STOP program and master-clear for TB2 33C. Pulse is approximately 3 volts.					

Chassis A1A1(1), A1A2(2), A8A1(9) and A8A2(10) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
NOTE: To monitor TB2 20F STOP program, master-clear and on I/O Panel A1 set EI MON CH 1 for chassis (1) and (9) or CH 0 for chassis (2) and (10).					
20F	(+)	.1		66	12Vg7

Chassis A2A1(3) TB1

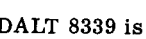
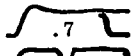
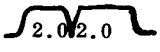
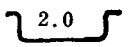
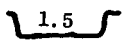
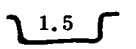
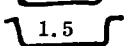
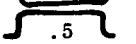
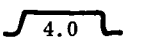
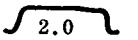
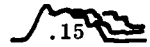
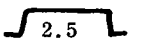
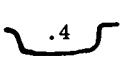
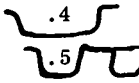
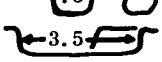
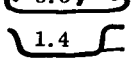
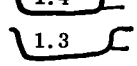
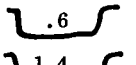
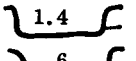
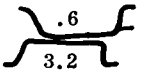
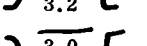
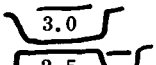
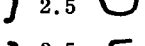
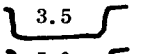
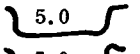
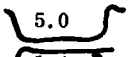
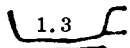
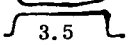
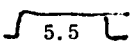
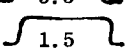
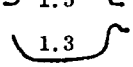
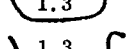
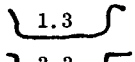
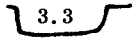
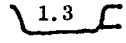
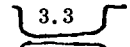
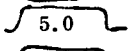
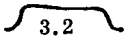
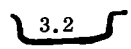
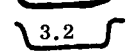
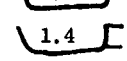
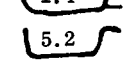
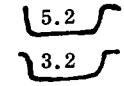
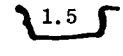
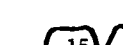
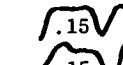
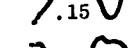
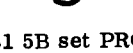
TB1	Slope	Scale	Pulse	Plate No.	Gate
1F	(+)	.5		13	54G20
Disregard TB1 3A if ORDALT 8339 is installed.					
3A	(+)	.2		13	45F20
4B	(+)	1.0		14	44G20
4C	(-)	.5		12	21G24
5A	(-)	.5		12	23G20
5C	(-)	.5		12	21G23
5D	(-)	.5		12	21G22
6F	(+)	.2		12	00E20
7D	Low Level			52	43G05
7F	(+)	.5		14	41E20
8A	(+)	.5		14	04G25
8C	(+)	.1		16	47G20
11A	(+)	.5		41	93F00
11D	(-)	.1		40	11N16
11E	(-)	.5		40	17F50
12D	(-)	.5		41	09F10
12E	(-)	.2		41	09F30
12G	(-)	.2		41	09F60
13C	(-)	.2		41	09F00
13E	(-)	.2		41	09F20
14B	(-)	.1		41	08F50
14C	(+)	.5		41	08F40
16B	(-)	1.0		44	17F14
16C	(+)	.5		44	41F14
17F	(-)	.5		44	21F06
20A	(-)	1.0		45	87F40
20C	(-)	1.0		45	43F24
20E	(+)	.2		45	40F20
20F	(-)	.2		45	43F20
21C	(+)	1.0		45	42F24
21G	(+)	.5		45	38F21
22D	(+)	2.0		45	20F24
22E	(-)	.2		45	21F22

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

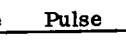
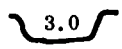
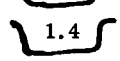
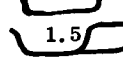
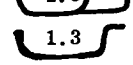
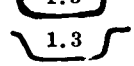
Chassis A2A1(3) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
22F	(-)	.2		45	21F20
23A	(+)	1.0		45	32F04
23C	(+)	1.0		45	20F26
24A	(+)	.5		46	42F36
24B	(-)	.2		46	21F36
24C	(-)	.2		46	21F34
24E	(-)	.5		46	21F32
24F	(-)	.2		46	31F30
26A	(-)	.5		47	11F56
25G	(+)	2.0		26	42F30
26C	(+)	.5		47	12F53
26D	(-)	.5		47	11F51
27D	(-)	.5		47	11F52
27B	(-)	.2		47	21F54
28A	(-)	1.0		47	11F57
28C	(-)	.5		47	11F53
28E	(-)	.5		47	11F50
30A	High Level			4	20J06
31B	(+)	.1		4	60C00
32B	(+)	.1		4	60C01
32C	(-)	.1		4	63C24
33C	(-)	.1		4	63C13

NOTE: To monitor TB1 5B set PROGRAM SKIP 0 up.

5B	(+)	.1		12	21G27

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
1A	(-)	1.0		48	11F75
1B	(-)	.2		48	11F73
1D	(-)	.5		48	11F72
1E	(-)	.5		48	17F62
1F	(-)	.5		48	17F61
1G	(-)	.5		48	17F60
2B	(-)	1.0		48	11F74

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
2C	(-)	.5		48	41F72
3A	(-)	.2		48	31F00
4G	(-)	.5		55	23E15
5A	(+)	.1		29	23G34
5E	(-)	.5		35	21L10
7A	(-)	.1	 4 volts	29	93A00
7C	(-)	.1		29	83A00
7D	(-)	.2		35	11G34
8C	(-)	.1		27	11E37
12A	(-)	.1		30	11E51
12F	(-)	.5		30	11G52
14D	(-)	.2		53	01N44
14E	(-)	.2		15	11T24
14F	(-)	.2		15	11T14
17G	(+)	.5		15	04G20
18A	(-)	.1		11	03T44
18B	(-)	.2		11	03T43
18D	(-)	.2		11	03T42
18E	(-)	.2		11	05T42
18F	(+)	.5		11	04T41
19C	(-)	.1		17	91N01
19D	(-)	.2		17	48N01
19E	(-)	.2		17	38N01
21A	(-)	.5		19	48N03
21B	(-)	2.0		19	38N03
23A	(-)	.2		18	36N02
23D	(-)	.2		18	58N02
23F	(-)	.2		18	28N02
25A	(+)	5.0		20	28N05
25F	(+)	5.0		20	28N04
27C	(-)	.1		21	28N07
28A	(-)	.2		8	03T14
28C	(-)	.1		8	05T13
28D	(-)	.2		8	03T13

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

Chassis A2A1(3) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
28F	(-)	.2	.45	8	11T11
29A	(-)	.2	.5	9	03T24
29D	(+)	.2	.5	9	04T21
29E	(-)	.2	.5	9	03T21
30A	(-)	.2	.5	10	03T34
30B	(+)	.5	.5	10	04T33
30C	(-)	.1	.45	10	03T31
31F	High Level			3	01J01
31G	High Level			3	03J02
32C	Low Level			3	30J10
32F	High Level			3	01J02
32G	High Level			3	01J03
33B	High Level			3	32J10
33G	Low Level			3	01J00

NOTE: To monitor TB2 9G STOP program, master-clear and ground TB2 10C on chassis A4A1(7).

9G	(+)	.1	.15	34	15G28

NOTE: To monitor TB2 30F depress SEQ DES INT on Control Panel (1) A2.

30F	(+)	.1	.15	15	03G21

Chassis A2A2(4) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
1B	(+)	.1	.15	93	21A12
1E	(+)	.1	.15	93	21A15
5A	(+)	.2	.8	96	13A14
5B	(+)	.1	.1	96	13A15
5C	(+)	.1	.85	96	13A16
5D	(+)	.1	.85	96	13A17
5E	(-)	5.0	2	33	24G30
6A	(+)	.2	.8	95	13A07
6B	(+)	.2	.8	95	13A08
6C	(+)	.2	.2	95	13A09
6D	(+)	.2	.8	95	13A10
6E	(+)	.2	.9	95	13A11
6F	(+)	.2	.85	96	13A12
6G	(+)	.1	.85	96	13A13

Chassis A2A2(4) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
7A	(+)	.2	.4	94	13A00
7B	(+)	.1	.3	94	13A01
7C	(+)	.1	.8	94	13A02
7D	(+)	.1	.12	94	13A03
7E	(+)	.2	.3	94	13A04
7F	(+)	.1	.3	94	13A05
7G	(+)	.1	.3	95	13A06
11B	(+)	.2	1.2	92	21A06
11D	(+)	.1	.2	92	21A09
12B	(+)	.1	.2	91	21A00
13A	(+)	.2	.8	96	11A14
13B	(+)	.1	.55	96	11A15
13C	(+)	.1	.9	96	11A16
13D	(+)	.1	.55	96	11A17
13F	(+)	.1	.3	91	21A03
14A	(+)	.2	.8	95	11A07
14B	(+)	.1	.5	95	11A08
14C	(+)	.1	.2	95	11A09
14D	(+)	.1	.5	95	11A10
14E	(+)	.2	.9	95	11A11
14F	(+)	.1	.9	96	11A12
14G	(+)	.1	.85	96	11A13
15A	(+)	.1	.2	94	11A00
15B	(+)	.1	.3	94	11A01
15C	(+)	.1	.4	94	11A02
15D	(+)	.1	.4	94	11A03
15E	(+)	.1	.3	94	11A04
15F	(+)	.1	.4	94	11A05
15G	(+)	.1	.2	95	11A06
21D	Low Level			20	01N05
21E	Low Level			20	01N04
25E	(-)	.5	3.3	47	11F46
25F	(-)	.5	3.3	47	11F45
25G	(-)	.5	3.3	47	11F42
29B	(-)	.5	1.5	33	01E30
30E	(+)	10.0	43.0	98	02A35
31D	(-)	1.0	1	100	02A17

TABLE 7-9C
7002070 Printed Circuit Card Test (Continued)

Chassis A2A2(4) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
31E	(+)	.1	.15	100	03A17

Chassis A2A2(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
5A	(+)	.1	.5	84	14X14
5B	(+)	.1	.5	84	14X15
5C	(+)	.1	.5	84	14X16
5D	(+)	.1	.5	84	14X17
6A	(+)	.1	.5	83	14X07
6B	(+)	.1	.5	83	14X08
6C	(+)	.1	.6	83	14X09
6D	(+)	.1	.5	83	14X10
6E	(+)	.1	.5	83	14X11
6F	(+)	.1	.5	84	14X12
6G	(+)	.1	.5	84	14X13

Chassis A2A2(4) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
7A	(+)	.1	1.0	82	14X00
7B	(+)	.1	1.0	82	14X01
7C	(+)	.1	.5	82	14X02
7D	(+)	.1	.4	82	14X03
7E	(+)	.1	.4	82	14X04
7F	(+)	.1	.4	82	14X05
7G	(+)	.2	1.0	83	14X06
27F	(-)	.1	.1 Low amplitude	39	11G45
30A	(+)	.1	.4	101	16X04
30B	(+)	.1	.4	101	16X06
30C	(+)	.1	.35	101	16X08
30D	(+)	.1	.3	101	16X10
30E	(+)	.1	.4	101	16X12
30F	(+)	.1	.3	101	16X14
30G	(+)	.1	.35	101	16X16
31F	(+)	.1	.4	101	16X00
31G	(+)	.1	.35	101	16X02

Chassis A4A1(7) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
1A	(+)	.2	1.5	30	12K03
3B	(-)	.1	.5	23	28N13
4D	(+)	.1	.45	22	79N12
4G	(+)	.1	.55	23	00N13
5B	High Level			22	38N12
5D	(-)	.1	.4	22	78N12
5E	(-)	.1	.45	22	28N12
5F	(-)	.1	.45	22	18N12
6D	(-)	.1	.45	22	48N12
8G	Low Level			31	11G60
15C	(+)	.2	.4	50	02G07
15D	(-)	.1	.3	50	03G07
16D	High Level			50	07G10
21B	(-)	.5	2.2	28	13G38
24C	(-)	.2	1.5	37	03K00
24E	(+)	.1	.5	37	03K01
24G	(-)	.1	.1	37	03K02
25B	(+)	.5	2.5	37	03K03
26A	(+)	.2	1.5	37	02K00
26B	(+)	.2	1.5	37	07K02
26C	(+)	.1	.1	37	07K03
26D	(-)	.5	.5	37	07K04
26E	(-)	.1	.45	37	07K05
28G	(-)	.1	.5	28	13T14

NOTE: To monitor TB1 6B Stop program and depress LOAD MODE.

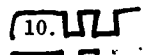
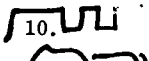
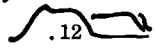
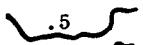
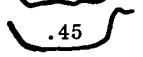
6B	(-)	.1	.45	22	68N12

NOTE: To monitor TB1 15E Stop program, master-clear, depress and release EI ODD on I/O Panel A1.

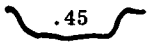
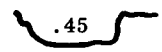
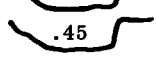
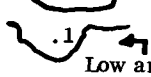
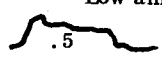
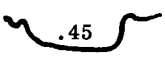
15E	(+)	.1	.5	50	16V14

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

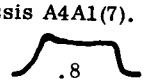
Chassis A4A1(7) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
1B	(+)	10.0		36	03L01
1C	(+)	10.0		36	03L00
1D	(+)	.1		36	14L00
1G	(-)	.1		36	11L01
2A	(-)	.1		26	08N09
3D	High Level			7	06J11
3E	Low Level			7	08J12
3F	Low Level			7	10J11
4G	Low Level			7	06J12
5B	Low Level			7	09J13
5D	High Level			7	02J11
5F	High Level			55	23G16

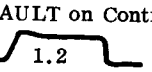
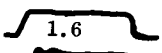
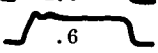
NOTE: To monitor TB2 6D, Stop program, master-clear, ground TB2 8F on chassis A4A1(7).

6D	(-)	.5		55	23G17
8D	(-)	.1		35	11L10
12G	(-)	.1		53	01N48
14B	(-)	.1		53	01N40
14G	(-)	.1	 Low amplitude	49	03E00
16F	(+)	.1		49	00N61
19A	Low Level			54	02G16
20E	Low Level			7	10J12
25D	High Level			134	12G81
26A	(-)	.1		10	03T32

NOTE: To monitor TB2 6B Stop program, master-clear, ground TB2 7C on chassis A4A1(7).

6B	(+)	.2		55	23G15

NOTE: To monitor TB2 6A, 8A, and 8B Stop program, master-clear and ground TB1 22B on chassis A4A1(7), and depress RESUME FAULT on Control Panel 2.

6A	(+)	.2		55	23G18
8A	(+)	.2		35	31L10
8B	(+)	.2		35	42L10

NOTE: To monitor TB2 10A and 17A set RTC DISC on Control Panel 2 down.

Chassis A4A1(7) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
10A	(+)	.2msec		34	03G29
17A	(-)	.1		49	41E00

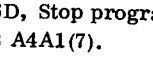
NOTE: To monitor TB2 10F and 11D, Stop program, master-clear and ground TB2 10C on chassis A4A1(7).

10F	(-)	.1		34	13G28
11D	(-)	.1		34	11E28

NOTE: To monitor TB2 11E ground TB1 29B on chassis A4A2(8).

11E	(-)	.1		53	01E12

NOTE: To monitor TB2 12B Stop program, master-clear, depress and hold FUNCTION PRIORITY EI ODD on I/O Panel A1.

12B	(-)	.1		53	01N42

NOTE: To monitor TB2 12F depress and hold CHANNEL and FUNCTION CLEAR button on Control Panel 2.

12F	(-)	.1		53	01E04

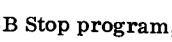
NOTE: To monitor TB2 18E Stop program, master-clear and depress RESUME FAULT on Control Panel 2.

18E	High Level			54	12G18

NOTE: To monitor TB2 18G depress INSTRUCTION FAULT on Control Panel 2.

18G	(-)	.2		54	16G14

NOTE: To monitor TB2 26F Stop program and hold master-clear.

26F	(+)	.1		51	21G07

Chassis A4A2(8) TB1

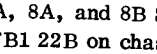
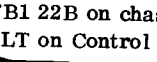
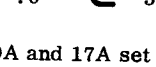
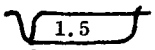
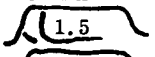
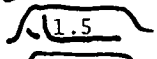
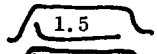
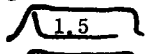
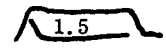
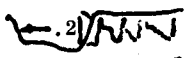
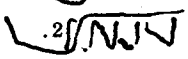
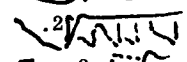
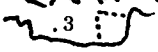
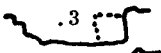
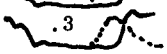
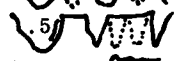
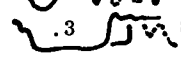
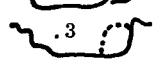
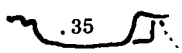
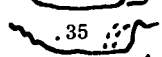
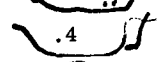
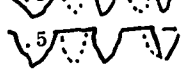
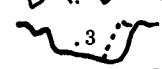
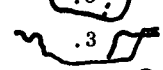
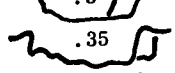
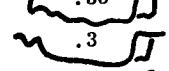
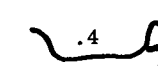
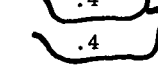
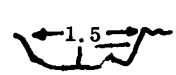
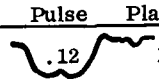
TB1	Slope	Scale	Pulse	Plate No.	Gate
4F	(+)	.1		107	92S00
5A	(-)	.1		107	11N00
9G	High Level			121	92G91
10A	(+)	.2		118	11B01
10C	(+)	.5		118	11B03
10E	(+)	.5		118	11B05

TABLE 7-9D
7002070 Printed Circuit Card Test (Continued)

Chassis A4A2(8) TB1

TB1	Slope	Scale	Pulse	Plate No.	Gate
12E	(-)	.5		119	11B11
13A	(+)	.5		119	11B07
13C	(+)	.5		119	11B09
16A	(+)	.5		120	11B13
16C	(+)	.5		120	11B15
16E	(+)	.5		120	11B17
19A	(-)	.2		79	11X00
19B	(-)	.2		79	11X01
19C	(-)	.1		79	11X02
19D	(-)	.1		79	11X03
19E	(-)	.1		79	11X04
19F	(-)	.1		79	11X05
21A	(-)	.5		80	11X06
21B	(-)	.5		80	11X07
21C	(-)	.1		80	11X08
21D	(-)	.1		80	11X09
21E	(-)	.1		80	11X10
21F	(-)	.1		80	11X11
22G	(-)	.1		81	12X15
23A	(-)	.5		81	11X12
23B	(-)	.5		81	11X13
23C	(-)	.1		81	11X14
23D	(-)	.1		81	11X15
23E	(-)	.1		81	11X16
23F	(-)	.1		81	11X17
23G	(-)	.1		81	12X17
24D	High Level			21	18N08
26C	(-)	.1		25	38N11
26G	(-)	.1		24	58N10
27D	High Level			24	28N10
27B	(-)	.2		24	18N10
27F	(-)	.1		24	38N10
31A	High Level			121	92G93

Chassis A4A2(8) TB2

TB2	Slope	Scale	Pulse	Plate No.	Gate
12C	(-)	.1		122	31EF06

4. Place FUNCTION REPEAT switch in the up position.

5. Set the FUNCTION CODE register to 12_8.

6. Press MODE OP STEP switch.

7. Press RESTART/START STEP switch to START STEP. (Repeat step 7 for first-time operation.)

With step 7 completed, the computer stops and the desired word is available for inspection in the AL register. To repeat the procedure, perform step 7 only.

7-43. Manual Inspect and Change Routine. It is often necessary to check the contents of consecutive addresses in storage. This can be done by manually loading a short program in accordance with procedures outlined in Manual Loading Into Addresses (paragraph 7-41). Such a short program is shown in Table 7-10. When the program has been loaded, consecutive memory addresses are read by use of the following procedures:

1. Press SEQ STEP/STOP switch to STOP.

2. Press I/O CLEAR/MASTER CLEAR switch to MASTER CLEAR.

3. Set P register equal to 00010_8.

4. Set the desired starting address in the AL register.

5. Press MODE RUN switch.

6. Press RESTART/START STEP switch to START STEP.

With step 6 completed, the computer stops and AU displays the contents of the address specified in AL. Each time the RESTART/START STEP switch is pressed to START STEP, AL is incremented and the computer stops with the contents of the next consecutive address displayed in AU. If, at any time, the operator decides to change the contents of an address as displayed in AU, he can make the change manually (set AU to the new value) and press the RESTART/START STEP switch to START STEP. This automatically changes the contents of that address (as specified in AL) and then displays the contents of the next consecutive address.

7-44. ISOLATING COMPUTER CASUALTIES. Computer casualties not isolated by the diagnostics can usually be isolated by following a logical sequence of steps. Scrutinizing the program listing and writing test programs (if necessary) will result in resolution of many casualties. Running of manual test from table 7-7A will also result in resolution of casualties. While there is no exact step-by-step procedure when manually troubleshooting, the following paragraphs are suggested methods for casualty isolation.

7-44A. ISOLATION BY PROGRAM ANALYSIS AND MANUAL PROGRAMING. Using procedures from paras 7-40 thru 7-43, the following is a logical sequence of steps recommended for use by the computer technician to isolate casualties.

1. Evaluate program listing and determine area of trouble.
2. If necessary, write a test program.
   a. Manually insert test program.
   b. Run test program to observe malfunction.
3. Select OP STEP and step through failing program (if program is the Diagnostic Program, OP STEP only subroutine or particular area depending on analysis of program to determine failing instruction.
4. Master clear computer.
5. Select SEQ STEP and step up to and through the failing instruction to determine the failing sequence.
6. Master clear computer.
7. Select SEQ STEP and step up to when Sequencer and P register indicate that the failing sequence is the next one to be performed.
8. Select PHASE STEP and any PHASE and step the main timing chain through one cycle.
9. Refer to volume 1 chapter 2 for timing events of failing instruction. Then PHASE STEP until a casualty is observed.

10. Select PHASE REPEAT using the following method:

a. Clear PHASE register.
b. Set PHASE REPEAT.
c. Set PHASE in register.

11. Use volume 2 part 3, Functional Schematics, to make measurements.

12. If computer seems to have failed during a previous phase, repeat steps 6 thru 10 to get that phase executing. By following the above sequence of events, the operator should be able to find all except memory casualties.

7-44B. SAMPLE TROUBLESHOOTING PROBLEM. As an example of the above method, assume that by studying the program listing the operator discovers that a BJP (f=73) instruction has failed. The operator then writes a small program to check an f=73. An example of such a program is shown in table 7-11. When entered, this program will have been run successfully if it came to a five stop. However, let us assume that the program came to a one stop. The operator would then OP STEP through program, carefully noting all indications on the control panels. When P=01006, the operator notes that the B register has an incorrect indication. This means that the instruction at P=01004 has failed. Since all instructions up to this point and the BJP(f=73) instruction have only one sequence, step 5 of the above sequence of events (para 44A) can be eliminated. The operator now selects SEQ STEP and steps the computer until P=01004. PHASE STEP is selected next and the clock is cycled once. Now the operator, using the detailed description of an f=73 instruction, phase steps through the instruction (refer to table 2-40 in volume 1 chapter 2). At time T4.2, the operator observes by taking a measurement that B $\pm$ 1 flip-flop did not set. The operator then clears the PHASE register. Next he places PHASE REPEAT switch up and pushes the PHASE 2 indicator in the PHASE register. By referring to Plate P-27, the operator then troubleshoots the B$\pm$1 flip-flop outputs and inputs and discovers that the flip-flop has pin 9 shorted. He replaces the flip-flop card and reruns his test program successfully, thus verifying that the flip-flop was the only problem.

7-44C. ISOLATION WITH MANUAL TESTS. Table 7-7A is a list of all manual tests available for troubleshooting casualties when diagnostics fail to isolate. If a certain area of the computer, such as main memory, is suspected as being the trouble then the memory tests should be run first. If the casualty does not point to any one area then the tests can be performed in the order listed in Table 7-7A.

7-44D. SAMPLE TROUBLESHOOTING PROBLEM. As an example of trouble-shooting a memory casualty, consider the following:

The Checkerboard Memory Test and the store-all-one's check are used, but fail. The failing pattern exists only when the address has a 03XXX4 form. Referring to the flow chart (figure 7-13), the operator observes that a problem exists in Stack 3 of Bank 0 in Chassis 6. By following the flow chart, the operator arrives at the question: Is the failure a stack group failure? To answer this question, the operator decides that the last three bits of the S1 register (or P register) indicate Y axis group selection (refer to figure 7-14B). Therefore, since the answer is yes, the operator procedes to I and notes that a possible cause could be a 43I card. By examing Plate P-142 in the Functional Schematics (Bank 0.Y axis group selection), the operator discovers that the 43I card suspected of being defective is located in 6J40B. Replacement of this card repairs the casualty.

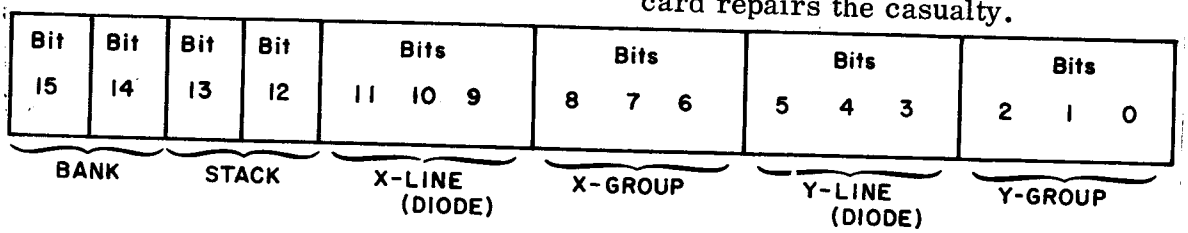


Figure 7-14B. S1 Bit Translation

TABLE 7-10. MANUAL INSPECT and CHANGE PROGRAM

Address	Instruction	Explanation
010	507201	Select address 01 for index register (B1) modification.
011	440001	(AL) → B1
012	110000	B1 → AU
013	505640	STOP
014	470000	(AU) → (B1)
015	710001	Increment AL
016	340011	Jump

NOTE: (AL) = Y
(AU) = (Y)

TABLE 7-11. SAMPLE TEST PROGRAM (f = 73)

Address	Instruction	Explanation
01000	507201	ENTICR
01001	360001	ENTBK B1 = 1_2
01002	731004	BJP B ≠ 0, B - 1 → B, Y → P B = 0, do NI
01003	505601	ZERO STOP if B = 0
01004	731006	BJP B ≠ 0, B - 1 → B, Y → P B = 0, do NI
01005	505640	Five STOP NORMAL STOP

TABLE 7-11. SAMPLE TEST PROGRAM (f=73) (Cont'd)

Address	Instruction	Explanation
01006	505602 To run program place the ZERO and one stop switch up.	One STOP if B $\neq$ 0 Program should not stop

7-46. SERVICE NOTES

7-47. The following subparagraphs provide information of a practical nature which endeavors to translate complexities of modern engineering design into concise everyday language. The troubleshooting techniques recommended herein are based on actual on-the-job experience acquired by engineering personnel responsible for maintaining the computer.

7-48. TECHNIQUES USED IN TROUBLESHOOTING INTERMITTENTS. The nature of intermittent problems is such that it is extremely difficult to prepare a set of procedures applicable to every situation. Just as there are several approaches to solving solid problems, there are different ways to go about isolating intermittents. The individual operator should experiment with various techniques and use those that appear to give the best results. However, there are some suggestions of a general nature that may prove useful in solving many problems. It is important to avoid simple mistakes that make troubleshooting intermittents more difficult. The following are provided as examples of the most common mistakes made in troubleshooting the digital computer:

1. A mass swapping of cards without first acquiring sufficient information to analyze the problem. This practice will often result in moving the problem around but will seldom succeed in eliminating it.

2. Failure to observe all indications on the maintenance panel each time a fault or error is detected. The problem can frequently be narrowed down to a small area by observation of the indicators.

3. Making memory adjustments in hopes of eliminating a problem before there is any tangible evidence that the memory is failing. This can lead to a marginal memory in addition to the original problem.

4. Failure to utilize an oscilloscope to pinpoint the problem to one circuit before turning off power and replacing a printed circuit card. When power is reapplied, the problem may disappear with no guarantee that the intermittent has been repaired.

5. Failure to keep an accurate record of all errors and faults as they occur, and the corrective action taken to rectify the problem. This is especially important where there is more than one shift working on the hardware at the installation.

6. Attempting to simultaneously track down several different indications rather than concentrating on one to determine what is wrong. It should be borne in mind that there may very well be two separate problems and confusion develops when trying to analyze the symptoms as resulting from a single casualty.

7. Using test equipment that is not in good operating condition. A defective oscilloscope has many times provided misleading information which prevented satisfactory resolution of a problem.

8. Carelessness in swapping and replacing printed circuit cards. Using the wrong card type or getting it in the wrong locations can lead to complications. If the symptoms appear different after changing cards the location where exchange took place should be carefully rechecked.

9. Ignoring an intermittent as soon as the symptoms temporarily disappear. This is pure negligence that can eventually lead to an accumulation of problems that become progressively more difficult to resolve.

7-49. If the foregoing mistakes are avoided, there is a good chance that most intermittent casualties can be located and quickly resolved. This is made possible by the fact that when a problem appears, it is usually solid for a few seconds to a few minutes provided the machine is not disturbed. It then becomes very important to make as many observations as possible in order to narrow the problem down to a specific area.

7-50. For random intermittents, a program that will cause the problem to recur at a rapid rate should be used. It is advisable to use maintenance routines with which the operator is most familiar assuming of course, that they produce recurrence of the failure. In most instances, it is obvious where a certain program has failed. It may be necessary to stop the computer immediately upon detection of a fault so as to determine exactly where the program has errored. Knowing where the program failed makes it possible to go to the listing of the program and ascertain exactly what the computer was doing. The operator should now have the problem isolated to a subroutine that can be cycled by changing a couple of instructions. If it is a long subroutine, it might be possible to rewrite it in a shorter form. With just that one subroutine cycling, the frequency of the intermittent should increase considerably.

7-51. The prime objective using this procedure is to get down to the single instruction that is failing. If one instruction is failing, it is necessary to see if anything associated with memory could possibly cause the problem. If the memory has the proper information then it can be assumed that memory is okay and that the processor I/O is failing. By observing all the registers, the operator should try to detect something that is incorrect. This is made easier in many instances by observing the instruction when it is being executed properly. If an abnormality is detected, it should lead to a sequence that caused it. Through use of the phase step mode of operation, the time and events that created the abnormal indications can frequently be pinpointed. If it appears that a specific enable was not generated, one should phase step up to that point and use phase repeat. This will allow a person to observe the enable signal on an oscilloscope. If it appears improper, all the inputs that generate the enable should be examined. It is very important that the equipment not be shut down or disturbed by pulling out a chassis until the problem is narrowed down to one or two circuits. When this has been accomplished, moving the suspected card or cards to another location will cause the problem to either move or not move. If it does not

move, examine all the wiring and connections associated with the circuit. Always check carefully for short pieces of loose wire that may be floating around in the chassis. This should be an initial step around any failing circuit. Otherwise, there is a risk that the problem will be moved around when checking the wiring thereby causing an intermittent in some other area. When checking, ensure that the routing has not left the wire pulled tight around a pin where the insulation is thin causing continuity with another circuit. This type of discrepancy is commonly called a cold-flow connection. If taper pins are used, they should be checked to ensure that they are inserted properly and that the wire has been stripped and crimped correctly. In wire wrapped machines, one should check for a tight wrap with the proper number of turns on the pin.

7-52. Recommended Techniques. When intermittent problems occur once or twice a week, it may be necessary to try one or more of the following techniques to cause the problem to manifest itself more frequently:

1. The 7002013 card has been found to cause many intermittent casualties in the Digital Computer Mk 152. When defective, the output of a gate tends to decrease in amplitude or width to a point where the enabling signal may cause intermittent problems. This type of problem is difficult to isolate using normal troubleshooting procedures such as diagnostic programs. Therefore, a mini-service program has developed that can be entered manually into the computer and will exercise all gates of all 7002013 cards. This allows the maintenance technician to observe and qualitatively analyze each signal output with the use of an oscilloscope. Refer to the MIP for the appropriate MRC to make this check.

2. Raise and lower the input power to the equipment. Be aware that some hardware can be damaged by high voltage so caution is advisable when using this method.

3. Raise and lower the input temperature, using caution and common sense to prevent damage from overheating of the equipment.

4. When the problem does occur and is obviously confined to a small area, try placing some of the cards on card extenders without allowing them to short out against the cabinet. It may then be possible to judiciously apply heat and cooling to the individual cards.

5. If memory is suspected, the currents or the bias voltage can be raised or lowered to see if the problem gets worse. However, it is recommended that the currents be accurately measured before any adjustments are made. Also, if the problem is thereby corrected, ensure that the current adjustments have not merely compensated for a marginal printed circuit card that should have been replaced before the adjustments were made.

6. With some hardware where chassis connectors and associated wiring are suspected, it is recommended that the side or back skins (panels) be removed. Then the failing programs can be run and the indications observed while moving the harness wiring. In certain instances, this can narrow the problem down to one connector. It will also help to isolate problems that are caused by replacing the side and back skins such as pinched wires and crosstalk which generates noise.

7. The main memory drawer can be extended so that the cards are accessible while power is applied.

8. In cases where timing seems to be the problem cause, speeding up the master clock may make the problem easier to find.

Care must be exercised to avoid creating new problems with this technique thereby making it more difficult to find the original source of trouble.

7-53. Troubleshooting equipment with known intermittent problems requires unlimited time. A problem should be looked into immediately upon occurrence. It is not deemed advisable to postpone action until preventive maintenance actions are scheduled. All too often, the intermittent will not recur during scheduled maintenance time.

7-54. In certain isolated cases, it will be noted that the only failing programs are those of an operational nature. These problems also demand prompt attention.

7-55. If the foregoing suggestions fail to uncover the source of a known intermittent, the following additional items should be checked as part of the fault isolation process:

1. Power supplies which are either oscillating or noisy. It is a good practice to check voltage on individual chassis with an oscilloscope. Multimeters will not detect high frequency oscillations.
2. Loose terminal lugs on terminal boards and in the power supplies.
3. Fuses and fuse holders that may have some resistance across them.
4. Motor generators that cause poor voltage and frequency regulation or produce high noise spikes.
5. Chassis covers that short card connector pins or pinch wires.
6. Test point blocks that might be pinching wires.
7. Poor wire routing in areas where timing is extremely critical.
8. P. C. Cards that are not pushed all the way into the connectors.
9. P. C. Cards that are rubbing against each other due to a missing card spacer.
10. P. C. Card jack connectors that have spread pins.
11. Hardware that uses voltage buss bars to connect the power pins together on card jacks. Check for poor solder connections to an individual connector pin. This would only be required after a problem is isolated down to one circuit. Since it is difficult to see a poor solder connection, it may be necessary to run a wire from a power pin on another card to see if this eliminates the problem.
12. The master clock is not adjusted properly. If the hardware has been running satisfactorily, this most likely would not be a problem.
13. In cases affecting I/O operations, check for foreign material lodged in the I/O connectors.
14. Chassis that are not aligned properly.
15. Poor ground system that is both internal and external to the hardware.
16. P. C. Cards or stacks whose connector pins are covered with foreign material such as epoxy.
17. Loose or missing contact wiper clip springs on 90-pin female connectors. These can be checked by taking a male pin and pushing it in. A small amount of resistance should be felt.

7-56. Records prove that a majority of intermittent problems are caused by printed circuit cards. The leading causes are overstressing of cards by external means such as overheating and internal means such as overvoltage or the pins are found to be partially coated with epoxy.

7-57. When a taper pin is causing an intermittent, identification as an under-crimp is accomplished by lightly pulling or pushing on the wire going into it. A slight give on the wire can be detected. It may be necessary to release the clamp that is gripping the insulation. On the other hand, an over-crimp

taper pin can be identified by removing the insulation on the wire in the taper pin. Usually only one or two strands of wire are attached and they will readily break off if the wire is pulled. Where faulty indicator modules are suspected, it is suggested they be disconnected from the circuit.

7-58. Since each computer has its own peculiar characteristics, it may prove worthwhile to contact the Naval Ship Weapon Systems Engineering Station concerning a particular intermittent problem. Station engineers may offer an immediate solution to the problem by virtue of having experienced the same problem on similar equipment at other installations.

7-59. TROUBLESHOOTING MEMORY PROBLEMS. There is reason to believe that many technicians troubleshooting memory problems confuse control and bootstrap addresses with main memory addresses which results in unnecessary troubleshooting and wasted time. The technician should be thoroughly familiar with the location of all memory addresses. If a memory problem is encountered in a control memory address, it is, of course, unproductive to troubleshoot in the main memory circuitry. If the BOOTSTRAP MODE NDRO/MAIN MEMORY switch is in the NDRO (Bootstrap Mode) position, the technician should realize that the bootstrap locations will contain information even though he has cleared all locations in memory.

7-60. JUMPER CABLES FOR CHECKING IOTA. Technical personnel are cautioned that care must be taken when installing or removing computer jumper cables. Unnecessary force or twisting of connectors can cause internal shorting, intermittent connections, and electrical opens in these cables.

7-61. TROUBLESHOOTING POWER FAILURES AND BLOWN FUSES. Card type 7003180 is located on all chassis except main memory. Chassis maps indicate the location of the cards. This card provides filter action for the -4.5 VDC and the ±15 VDC power supplies and should be considered as a possible source of trouble when troubleshooting power problems.

7-62. Hidden Fuses. Drawers A1, A2 and A4 all have fuses located behind them which are not visible unless the drawers are extended. There are fuses for the -4.5 VDC, the +15 VDC, and the -15 VDC power supplies. The only way to check these fuses is to remove and inspect them.

7-63. Computer Faults and Loading Problems. It is suggested that whenever the computer faults or has loading problems the input power be checked to ensure that it is at the proper level.

7-64. INDICATOR LAMPS. In the past, many technicians have experienced difficulty in locating indicator lamps as shown on the functional schematics. Plate P-1 of the functional schematics gives an example of a flip-flop with indicator DS5B. A note refers the user to Plate P-176 for details relative to the indicator and associated push button wiring.

7-65. EXTENDING 56-PIN MEMORY CARDS. A card extender should not be used with any of the 420/421 P.C. Cards. These cards have a twisted-pair matched impedance on input pins 48 and 52. If extended, either AND-gate Z5 or transistors Q1/Q3 may be damaged which is indicated by low Read/Write currents of only 350 MA instead of 720 MA P/P. Maintenance engineers have recommended that none of the cards in the

memory chassis which have a twisted pair input be extended. This includes the 780/781 and 0651 cards. It has been found that very few of the 0651 cards will run when extended.

7-66. POSSIBLE DAMAGE TO 0651 AND 0660 P.C. CARDS. Technicians who are working on the wiring side of the 0651 sense amplifiers, should never ground pins 3 or 4. Adjacent pins 1 and 2 are ground, so it is possible that they might inadvertently make contact if a scope probe is attached onto the pins or if there is tugging or pulling of the wires. Should they touch, resulting damage can affect several 0651 cards and some diodes in the 0660 card. Reference may be made to the 0651 card schematic or to the computer logic prints. Pin 4 on one card goes to pin 3 on the next card and is at about 15 volts. If either pin is grounded, the primary of transformer T1 and inductor L1 on the 0651 card cannot withstand the high current and will open. One solution is to slightly bend ground pins 1 and 2 away from pins 3 and 4 thereby reducing the chances of contact.

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Section 7-3. Troubleshooting Charts

7-67. This section of the manual discusses command timing and provides a charted analysis of computer operation during execution of every instruction in its repertoire. The five types of command sequences (Instruction, Read, Write, Buffer, and I/O) are defined and their operation described in the paragraphs that follow. Also included in this section is a table that identifies allocated control memory and bootstrap addresses.

7-68. INSTRUCTION REPERTOIRE ANALYSES

7-69. This paragraph contains a detailed analysis of each instruction in the computer's repertoire. The instructions are arranged in ascending order by OCTAL code. Tables 7-12 and 7-13 respectively provide a list of all Format I and Format II instructions and also provide descriptive analyses of the instructions. For each instruction the following information is presented:

1. OCTAL code.
2. Trim Nmemonic.
3. Name of the instructions.
4. Time required for execution.
5. A listing of the main command sequences employed in execution of the instruction and the order in which they are performed.
6. A detailed analysis of the multiply, divide, shift, and scale sequences (where applicable).

7-70. SEQUENCE TIMING CHARTS

7-71. COMMAND SEQUENCES. The computer employs five types of command sequences which are listed and defined as follows:

1. I - Instruction sequence: Reads instruction from memory.
2. R1 and R2 - Read sequences: Read operand from memory.
3. W - Write sequence: Writes operand into memory.
4. B1 and B2 - Buffer sequences: Control loading of buffer control words and activating of an I/0 channel.
5. I/01 and I/02 - Input/output sequences: Control data transfers and internal special sequences.

7-72. Command sequences are selected by the sequencer in a predetermined order necessary for proper instruction execution. The main timing chain, operating in conjunction with the sequence destination and the master clock, develops the 16 timing pulses (4.4, 1.1 1.2. 1.3, 1.4, 2.1, ..., 4.3) necessary to synchronize computer operation during the selected sequence. Not all command sequences are required to execute an instruction. In some cases, only one sequence (I) is necessary; in others, three sequences may be required for complete instruction execution. Refer to tables 7-12 and 7-13 which list each instruction with the applicable command sequences, and to the command sequence tables which provide analyses of functions performed. Command sequences of each instruction are listed in abbreviated form in table 7-14.

7-73. Command sequence tables (7-15 through 7-24) contain a phase-by-phase analysis of functions performed during each command sequence. Following each time notation,

which reflects internal computer timing in terms of cycle and phase time, is a list of commands performed at that time in the sequence. The expression in the third column following certain functions indicates a condition or conditions necessary to perform or not perform those functions. Absence of an expression in the condition column indicates that the function is performed unconditionally. The right-hand column contains the plate number of the functional schematic drawing and the gate number which controls the command. For example, in the I sequence chart, the entry T3.1 AL→Arithmetic Selector f = 71 20N01-17, is read: At 3.1 time of an I sequence for instruction 71, the contents of the AL register are transferred to the arithmetic selector under control of Gate No. 20N01 on Plate No. P-17 of the functional schematics contained in Chapter 9, Part 3 of this volume.

7-74. I Sequence. I sequence (table 7-15) is the first sequence performed during the execution of every instruction. During the I sequence, the instruction word is addressed, read out of memory, and initially operated upon.

7-75. R1 and R2 Sequence. R sequences (table 7-16) are used in instructions where it is necessary to obtain contents of a given memory address to complete the instruction.

7-76. W Sequence. W sequence (table 7-17) is used to write the results of an instruction into a specified memory location.

7-77. B Sequence. B sequences (tables 7-18 and 7-19) are used to transfer the two words in memory locations immediately following the 50:11 through 50:13 instructions into the proper control memory location, and set the active flip-flop for the proper operation and channel.

7-78. I/O Sequences. Sequence timing tables list the commands and conditions for each sequence and, in the case of the I/O sequences, the mode of operation is given. I/O sequences, I/O 1 and I/O 2, are listed in tables 7-20 and 7-21. The I/O 1 sequence is used to read the buffer control words, compare them, and then write the current address buffer control word back into control memory, as well as storing or transmitting a data word. I/O 2 sequence follows I/O 1 sequence when the computer is in the dual mode or in ESI mode, and is terminating a buffer.

7-79. Continuous Data Mode. An Analysis of the Continuous Data Mode (CDM) sequence with a listing of the times and the commands for the CDM sequence is provided in table 7-22.

7-80. Real-Time Clock. An analysis of the functions performed during the Real-Time Clock (RTC) sequence is presented in table 7-23.

7-81. Interrupt. The functions performed during the interrupt sequence are analyzed in table 7-24. The table lists the interrupt sequence which runs parallel to the I sequence when a fault interrupt has been received or when an I/O interrupt occurs. The interrupt sequence forces the computer to a specified address where the I sequence then takes over and controls the performance of the instruction which was stored at that address.

7-82. Control and Bootstrap Addresses. Table 7-25 contains the assignments of specific addresses within control memory and the location of bootstrap. All addresses not in control memory are in main memory. The bootstrap address shadows addresses in main memory which can be used if the BOOTSTRAP MODE switch is in the MAIN MEMORY position.

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTIONS

OCTAL CODE	INSTRUCTION AND ANALYSIS		
00	ILLEGAL CODE I		Execution Time: 2 usec
01	ILLEGAL CODE I		Execution Time: 2 usec
02	COMPARE (AL) WITH (Y) I R1	(CMAL)	Execution Time: 4 usec
03	COMPARE (AL) WITH (Y) I (B modified)	(CMALB)	Execution Time: 4 usec
04	SELECTIVE SUBSTITUTE I R1	(SLSU)	Execution Time: 4 usec
05	SELECTIVE SUBSTITUTE I (B modified) R1	(SLSUB)	Execution Time: 4 usec
06	COMPARE WITH MASK I R1	(CMSK)	Execution Time: 4 usec
07	COMPARE WITH MASK I (B modified) R 1	(CMSKB)	Execution Time: 4 usec
10	ENTER AU I R1	(ENTAU)	Execution Time: 4 usec

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTIONS (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS		
11	ENTER AU I (B modified) R1	(ENTAUB)	Execution Time: 4 usec
12	ENTER AL I R1	(ENTAL)	Execution Time: 4 usec
13	ENTER AL I (B modified) R1	(ENTALB)	Execution Time: 4 usec
14	ADD AL I R1	(ADDAL)	Execution Time: 4 usec
15	ADD AL I (B modified) R1	(ADDALB)	Execution Time: 4 usec
16	SUBTRACT AL I R1	(SUBAL)	Execution Time: 4 usec
17	SUBTRACT AL I (B modified) R1	(SUBALB)	Execution Time: 4 usec
20	ADD A I R1 R1R2	(ADDA)	Execution Time: 6 usec
21	ADD A I (B modified) R1 R1R2	(ADDAB)	Execution Time: 6 usec

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTIONS (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
22	SUBTRACT A (SUBA) Execution Time: 6 usec I R1 R1R2
23	SUBTRACT A (SUBAB) Execution Time: 6 usec I R1 R1R2
24	MULTIPLY AL (MULAL) Execution Time: 14 usec I R1T1.3 Set A NEG FF if AL neg, CLR D, X, W Reg .4 A1 → Selector, $\overline{\text{Selector}}$ → D R1T2.1 Set MULT/DIV SEQ (OXL01), Set K0=23_8, CLR AL if AL = neg .2 CLR K1, Adder → AL if AL = neg .3 CLR X, CLR W, [CLR D (Pass 1 only)] K0-1 → K1 CLR MILT. STORE FF Set OXL00 (First pass and K0 ≠ 0) Set Hold II FF (Hold I FF set and first pass only) .4 CLR K0, [Selector → D (Y pos), Selector → D (Y neg) (Pass 1 only)] Set MULT. STORE FF (AL Bit 0 = 1) AUR1 → X, ALR1 → W Set Y NEG FF if X = neg (Pass 1 only) .1 K1 → K0 CLR AL CLR AU .2 CLR K1 SET HOLD 1 FF (First pass only) W → AL X → AU (AL Bit 0 = 0) Adder → AU (AL Bit 0 = 1) K0 ≠ 0

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS	
24 (Cont'd)	K0 = 0	
	R1T2.3 CLR OXL00	
	Set OXL02	
	K0-1 → K1	
	CLR MULT. STORE FF	
	CLR X, CLR W	
	.4 AUR1 → X, ALR1 → W	
	R1T3.1 Set CLEAR HOLD FF	
	Set OXL03	
	CLR OXL01	
	.3 CLR X, W, D	
	Set OXL04	
	CLR OXL02	
	.4 AU → Arithmetic Selector	
	Arithmetic Selector → X	(AU or AL ≠ 0)
	Arithmetic Selector → X	(AU or AL ≠ 0)
	Arithmetic Selector → D	
	R1T4.1 CLR AU	(Comp AU)
	Set OXL05	(Signs Unlike)
	CLR OXL03	
	.2 Resume R1 Sequence here	
	Adder → AU	(Comp AU, Signs Unlike)
	CLR HOLD I FF	
	.3 CLR D	(Signs Unlike)
	Set OXL06	(Signs Unlike)
	CLR OXL04	
	.4 AL → Arithmetic Selector	(Signs Unlike)
	Arithmetic Selector → D	(Signs Unlike)

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
	NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I .1 CLR AL CLR OXL05 (Signs Unlike) .2 Adder → AL (Signs Unlike) .3 CLR HOLD II FF
25	MULTIPLY AL (MULAB) Execution time: 14 usec I (B modified) R1T2.1 Set MUL T/DIV SEQ (Same as instruction 24) T4.2 Resume R1 SEQ (Same as instruction 24) I (Same as instruction 24)
26	DIVIDE A (DIVA) Execution time: 14 usec I R1T1.3 Set A NEG FF if AU negative, CLR, D, X, W .4 AU → Arithmetic Selector, $\overline{\text{Arithmetic Selector}}$ → D R1T2.1 Set MULT/DIV SEQ (OXL01), Set K0 = 22_8, CLR AU if AU neg .2 CLR K1, Adder AU if AU neg .3 CLR X, CLR W; CLR D (first pass only) K0-1 → K1 Set OXL00 (First pass and K0 ≠ 0) Set Hold II FF (HOLD I FF set and first pass only) .4 CLR K0, $\overline{\text{Arithmetic Selector}}$ → D if Y pos (Pass 1 only) AUL1 → X, ALL1 → W, Set Y NEG FF if X neg (Pass 1 only) Arithmetic Selector → D if Y neg (First pass only)

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS	
26 (Cont'd)	.1 K1→K0	
	CLR AL	
	CLR AU	
	.2 CLR K1	
	SET HOLD 1 FF	(First pass only)
	W→AL	
	X→AU	(EAB)
	Adder→AU	(No EAB)
	If Adder→AU, set OVERFLOW FF	(Pass 1 only)
	K0 ≠ 0	
	K0 = 0	
	.3 CLR OXL00	
	Set OXL02	
	K0-1→K1	
	CLR X, CLR W	
	.4 AUL1→X, ALL1→W	
	.1 Set CLEAR HOLD FF	
	Set OXL03	
	CLR OXL01	
	.2	
	.3 CLR X, W, D	
	Set OXL04	
	CLR OXL02	
	.4 AU→Arithmetic Selector	
	Arithmetic Selector→D	
	.1 CLR AU	(Comp AU)
	Set OXL05	(Comp AU)
	CLR OXL03	(Signs Unlike)
	R1T4.2 Resume R1 Sequence here	
	Adder→AU	Comp AU
	CLR HOLD I FF	

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
26 (cont'd)	.3 CLR → D (Signs Unlike) Set OXL06 (Signs Unlike) CLR OXL04 .4 AL → Arithmetic Selector (Signs Unlike) Arithmetic Selector → D (Signs Unlike) NOTE: At this point, this instruction enters I Sequence of the next instruction to complete its operation. I .1 CLR AL (Signs Unlike) CLR OXL05 .2 Adder → AL (Signs Unlike) .3 CLR HOLD II FF
27	DIVIDE A (DIVAB) Execution Time: 14 usec I (B modified) R1T2.1 Set MULT/DIV SEQ (Same as instruction 26) T4.2 Resume R1 SEQ (Same as instruction 26) I (Same as instruction 26)
30	INDIRECT RETURN JUMP (IRJP) Execution Time: 6 usec I R1 W
31	INDIRECT RETURN JUMP (IRJPB) Execution Time: 16 usec I (B modified) R1 W

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
32	ENTER B (ENTB) Execution Time: 4 usec I R1 NOTE: At this point, this instruction enters, I sequence of the next instruction to complete its operation. I 1.1 ICR → S0 Initiate Control Memory 1.2 Z1 → Z0 1.3 Inhibit Control Memory → Z0
33	ENTER B (ENTBB) Execution Time: 4 usec I (B modified) R1 I (Same as 32)
34	DIRECT JUMP (JP) Execution Time: 2 usec I
35	DIRECT JUMP (JPB) Execution Time: 2 usec I (B modified)
36	ENTER B WITH CONSTANT (ENTBK) Execution Time: 2 usec I NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I 1.1 ICR → S0 Initiate Control Memory 1.2 Z1 → Z0 1.3 Inhibit Control Memory → Z0

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS		
37	MODIFY BI WITH CONSTANT I (B modified) I (Same as 36)	(ENTBKB)	Execution Time: 2usec
40	CLEAR Y I W	(CL)	Execution Time: 4 usec
41	CLEAR Y I (B modified) W (Same as 40)	(CLB)	Execution Time: 4 usec
42	STORE (B) I W	(STRB)	Execution Time: 4 usec
43	STORE (B) I (B modified) W (Same as 42)	(STRBB)	Execution Time: 4 usec
44	STORE AL I W	(STRAL)	Execution Time: 4 usec
45	STORE AL I (B modified) W	(STRALB)	Execution Time: 4 usec
46	STORE AU I W	(STRAU)	Execution Time: 4 usec
47	STORE AU I (B modified) W	(STRAUB)	Execution Time: 4 usec
50	See Format II instructions following instruction 77.		
51	SELECTIVE SET I R1	(SLSET)	Execution Time: 4 usec
52	SELECTIVE CLEAR I R1	(SLCL)	Execution Time: 4 usec

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
53	SELECTIVE COMPLEMENT (SLCP) Execution Time: 4 usec I R1
54	INDIRECT JUMP AND ENABLE INTERRUPTS (IJPEI) Execution time: 4 usec I R1
55	INDIRECT JUMP (IJP) Execution Time: 4 usec I R1
56	B SKIP (BSK) Execution Time: 4 usec I R1 NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I 1.1 ICR → S0 if B ≠ (Y) Initiate Control Memory 1.2 B+1 → Z0 1.3 Inhibit Control Memory → Z0
57	INDEX SKIP (ISK) Execution Time: 6 usec I R1 W
60	JUMP AU ZERO (JPAUZ) Execution Time: 2 usec I
61	JUMP AL ZERO (JPALZ) Execution Time: 2 usec I

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
62	JUMP AU NOT ZERO (JPAUNZ) Execution Time: 2 usec I
63	JUMP AL NOT ZERO (JPALNZ) Execution Time: 2 usec I
64	JUMP AU POSITIVE (JPAUP) Execution Time: 2 usec I
65	JUMP AL POSITIVE (JPALP) Execution Time: 2 usec I
66	JUMP AU NEGATIVE (JPAUNG) Execution Time: 2 usec I
67	JUMP AL NEGATIVE (JPALNG) Execution Time: 2 usec I
70	ENTER AL WITH CONSTANT (ENTALK) Execution Time: 2 usec I
71	ADD CONSTANT TO (AL) (ADDALK) Execution Time: 2 usec I
72	STORE INDEX CONTROL REGISTER (STRICR) Execution Time: 4 usec I W
73	B JUMP (BJP) Execution time: 2 usec I NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I 1.1 ICR → S0 if B ≠ 0 Initiate Control Memory 1.2 B-1 → Z0 1.3 Inhibit Control Memory → Z0

TABLE 7-12. COMMAND TIMING ANALYSIS, FORMAT I INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
74	STORE ADDRESS (STRADR) Execution Time: 4 usec I W
75	STORE SPECIAL REGISTER (STRSR) Execution Time: 4 usec I W
76	DIRECT RETURN JUMP (RJP) Execution Time: 4 usec I W
77	ILLEGAL CODE Execution Time: 2 usec I

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:00	Not Used
50:01	SET INPUT ACTIVE (SIN) Execution Time: 2 usec I
50:02	SET OUTPUT ACTIVE (SOUT) Execution Time: 2 usec I
50:03	SET EXTERNAL FUNCTION ACTIVE (SEXF) Execution Time: 2 usec I
50:04	Not Used
50:05	Not Used
50:06	Not Used
50:07	Not Used
50:10	Not Used
50:11	INPUT TRANSFER (IN) Execution Time: 6 usec I IB1 IB2 NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I 1.1 1.2 1.3
50:12	OUTPUT TRANSFER (OUT) Execution Time: 6 usec I IB1 IB2

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:12 (Cont'd)	NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation.
50:13	EXTERNAL FUNCTION (EXF) Execution Time: 6 usec I IB1 IB2 NOTE: At this point, this instruction enters I sequence of the next instruction to complete its operation. I
50:14	ENABLE REAL-TIME CLOCK MONITOR (RTC) Execution Time: 2 usec
50:15	TERMINATE INPUT (INSTP) Execution Time: 2 usec I
50:16	TERMINATE OUTPUT (OUTSTP) Execution Time: 2 usec I
50:17	TERMINATE EXTERNAL FUNCTION (EXFSTP) Execution Time: 2 usec I
50:20	SET RESUME (SRSM) Execution Time: 2 usec I
50:21	SKIP ON INPUT CHANNEL INACTIVE (SKPIIN) Execution Time: 2 usec I
50:22	SKIP ON OUTPUT CHANNEL INACTIVE (SKPOIN) Execution Time: 2 usec I
50:23	SKIP ON FUNCTION MODE INACTIVE (SKPFIN) Execution Time: 2 usec I

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:24/50:25	WAIT FOR INTERRUPT (WTFI) Execution Time: Indeterminate I WAIT
50:26	OUTPUT OVERRIDE (OUTOV) Execution Time: 6 or 8 usec I
50:27	EXTERNAL FUNCTION OVERRIDE (EXFOV) Execution Time: 6 or 8 usec I
50:30/50:31	REMOVE INTERRUPT LOCKOUT (RIL) Execution Time: 2 usec I
50:32/50:33	REMOVE EXTERNAL INTERRUPT (EXL) Execution Time: 2 usec I
50:34/50:35	SET INTERRUPT LOCKOUT (SIL) Execution Time: 2 usec I
50:36/50:37	SET EXTERNAL INTERRUPT LOCKOUT (SXL) Execution Time: 2 usec I
50:40	Not Used
50:41	RIGHT SHIFT AU (RSHAU) Execution Time: 4 usec (K0 = 0-4) 6 usec (K0 = 5-8) 8 usec (K0 = 9-12) 10 usec (K0 = 13-16) I T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:41 (Cont'd)	.3 CLR X, CLR W K0-1 → K1 Set OXL00 (First pass and K0) Set Hold II FF (First pass only) .4 CLR K0 AUR1 → X, ALR1 → W .1 K1 → K0 CLR AU Set CLEAR HOLD FF (K1=0) .2 CLR K1 X → AU K0 ≠ 0 K0 = 0 .3 CLR OXL00 Set OXL02 K0-1 → K1 CLR X, CLR W .4 AUR1 → X, ALR1 → W .1 CLR OXL01 Set CLEAR HOLD FF (Shift count)
50:42	RIGHT SHIFT AL (RSHAL) Execution Time: 4 usec (K0 = 0-4) I 6 usec (K0 = 5-8) 8 usec (K0 = 9-12) 10 usec (K0 = 13-16) T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:42 (Cont'd)	.3 CLR X, CLR W K0-1 → K1 Set OXL00 (First pass and K0 ≠ 0) Set Hold II FF (First pass only) .4 CLR K0 AUR1 → X, ALR1 → W .1 K1 → K0 CLR AL Set CLEAR HOLD FF (K1 = 0) .2 CLR K1 W → AL K0 ≠ 0 K0 = 0 .3 CLR OXL00 Set OXL02 K0-1 → K1 CLR X, CLR W .4 AUR1 → X, ALR1 → W .1 CLR OXL01 Set CLEAR HOLD FF (Shift count ≠ 0)
50:43	RIGHT SHIFT A (RSHA) Execution Time: 4 usec (K = 0-4) I 6 usec (K = 5-8) 8 usec (K = 9-12) 10 usec (K = 13-16) 12 usec (K = 17-20) 14 usec (K = 21-24) 16 usec (K = 25-28) 18 usec (K = 29-32) 20 usec (K = 33-35) T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:43 (Cont'd)	.3 CLR X, CLR W K0-1→K1 Set OXL00 (First pass and K0 = 0) Set HOLD II FF (First pass only) .4 CLR K0 AUR1 → X, ALR1 → W LOWER BIT OF AU → UPPER BIT OF W .1 K1 → K0 CLR AL CLR AU Set CLEAR HOLD FF (K1 = 0) .2 CLR K1 W → AL X → AU K0 ≠ 0 K0 = 0 .3 CLR OXL00 Set OXL02 K0-1 → K1 CLR X, CLR W .4 AUR1 → X, ALR1 → W LOWER BIT OF AU → UPPER BIT OF W .1 CLR OXL01 Set CLEAR HOLD FF (if shift count = 0)
50:44	SCALE FACTOR (SF) Execution Time: 4 usec (K = 0-4) I 6 usec (K = 5-8) 8 usec (K = 9-12) 10 usec (K = 13-16) 12 usec (K = 17-20) 14 usec (K = 21-24) 16 usec (K = 25-28) 18 usec (K = 29-32) 20 usec (K = 33-35)

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:44 (Cont'd)	T3.1 Set CLEAR HOLD FF (bit 35 ≠ bit 34) T3.4 Set HOLD 1 FF Clear SCALE FACTOR FF Bit 35 ≠ bit 34 Bit 35 = bit 34 4.1 Set OXL01 .2 Clear K1, clear HOLD I FF (bit 35 ≠ bit 34) .3 K0-1 → K1 Clear X, W Set OXL00 (First pass and K0 ≠ 0) Set HOLD II FF (Pass 1 and HOLD I FF set) .4 Clear K0 AUL1 → X ALL1 → W Set SCALE FACTOR FF (bit 34 ≠ bit 33) .1 K1 → K0 Clear AU, AL Set CLEAR HOLD FF (K1 = 0 or bit 35 ≠ bit 34) .2 X → AU W → AL Clear K1 K0 ≠ 0 AND SCALE FACTOR FF clear K0 = 0 OR SCALE FACTOR FF set .3 Clear OXL00 Set OXL02 K0-1 → K1 Clear X, W .4 AUL1 → X ALL1 → W

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:44 (Cont'd)	.1 CLR OXL01 Set CLEAR HOLD FF (K1 ≠ 0 and SCALE FACTOR FF was set or if shift count equals zero) (Complete I Sequence) W
50:45	LEFT SHIFT AU (LSHAU) Execution Time: 4 usec (K0 = 0-4) I 6 usec (K0 = 5-8) 8 usec (K0 = 9-12) 10 usec (K0 = 13-16) T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1 .3 CLR X, CLR W K0-1→K1 Set OXL00 (First pass and K0 ≠ 0) Set Hold II FF (First pass only) .4 CLR K0 AUL1→X, ALL1→W UPPER BIT OF AU→LOWER BIT OF X .1 K1→K0 CLR AU Set CLEAR HOLD FF (K1 = 0) .2 CLR K1 X→AU K0 ≠ 0 K0 = 0 .3 CLR OXL00 Set OXL02 K0-1→K1 CLR X, CLR W

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:45 (Cont'd)	.4 AUL1 → X, ALL1 → W UPPER BIT OF AU → LOWER BIT OF X .1 CLR OXL01 Set CLEAR HOLD FF (if shift count equals zero)
50:46	LEFT SHIFT AL (LSHAL) Execution Time: 4 usec (K0 = 0-4) I 6 usec (K0 = 5-8) 8 usec (K0 = 9-12) 10 usec (K0 = 13-16) T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1 .3 CLR X, CLR W K0-1 → K1 Set OXL00 (First pass and K0 ≠ 0) Set Hold II FF (First pass only) .4 CLR K0 AUL1 → X, ALL1 → W UPPER BIT OF AL → LOWER BIT OF W .1 K1 → K0 CLR AL Set CLEAR HOLD FF (K1 = 0) .2 CLR K1 W → AL K0 ≠ 0 K0 = 0 .3 CLR OXL00 Set OXL02 K0-1 → K1 CLR X, CLR W

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:46 (Cont'd)	.4 AUL1 → X, ALL1 → W UPPER BIT OF AL → LOWER BIT OF X .1 CLR OXL01 Set CLEAR HOLD FF (if shift count equals zero)
50:47	LEFT SHIFT A (LSHA) Execution Time: 4 usec (K = 0-4) I 6 usec (K = 5-8) 8 usec (K = 9-12) 10 usec (K = 13-16) 12 usec (K = 17-20) 14 usec (K = 21-24) 16 usec (K = 25-28) 18 usec (K = 29-32) 20 usec (K = 33-35) T3.4 Set HOLD I FF 4.1 Set OXL01 .2 CLR K1 .3 CLR X, CLR W K0-1 → K1 Set OXL00 (First pass and K0 ≠ 0) .4 CLR K0 AUL1 → X, ALL1 → W UPPER BIT OF AL → LOWER BIT OF X UPPER BIT OF AU → LOWER BIT OF W .1 K1 → K0 CLR AL CLR AU Set CLEAR HOLD FF (K1 = 0) .2 CLR K1 W → AL X → AU K0 ≠ 0

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS
50:47 (Cont'd)	K0 = 0 .3 CLR OXL00 Set OXL02 K0-1 → K1 CLR X, CLR W .4 AUL1 → X, ALL1 → W UPPER BIT OF AL → LOWER BIT OF X UPPER BIT OF AU → LOWER BIT OF W .1 CLR OXL01 Set CLEAR HOLD FF (if shift count equals zero)
50:50	SKIP OF KEY SETTING (SKP) Execution Time: 2 usec I
50:51	SKIP ON NO BORROW (SKPNBO) Execution Time: 2 usec I
50:52	SKIP ON OVERFLOW (SKPOV) Execution Time: 2 usec I
50:53	SKIP ON NO OVERFLOW (SKPNOV) Execution Time: 2 usec I
50:54	SKIP ON ODD PARITY (SKPODD) Execution Time: 2 usec I
50:55	SKIP ON EVEN PARITY (SKPEVN) Execution Time: 2 usec I
50:56	STOP ON KEY SETTING (STOP) Execution Time: 2 usec I
50:57	SKIP ON NO RESUME (SKPNR) I

TABLE 7-13. COMMAND TIMING ANALYSES, FORMAT II INSTRUCTION (Cont'd)

OCTAL CODE	INSTRUCTION AND ANALYSIS		
50:60	ROUND AU I	(RND)	Execution Time: 2 usec
50:61	COMPLEMENT AL I	(CPAL)	Execution Time: 2 usec
50:62	COMPLEMENT AU I	(CPAU)	Execution Time: 2 usec
50:63	COMPLEMENT A I	(CPA)	Execution Time: 2 usec
50:64 Thru 50:67	Not Used		
50:70	Not Used		
50:71	Not Used		
50:72	ENTER INDEX CONTROL REGISTER I	(ENTICR)	Execution Time: 2 usec
50:73	ENTER SPECIAL REGISTER I	(ENTSR)	Execution Time: 2 usec
50:74 Thru 50:76	Not Used		
50:77	ILLEGAL CODE I		Execution Time: 2 usec

TABLE 7-14. COMMAND SEQUENCES OF EACH INSTRUCTION

I SEQUENCES ONLY		
00	50:03	50:51
01	50:14	50:52
34	50:15	50:53
35	50:16	50:54
60	50:17	50:55
61	50:20	50:56
62	50:21	50:57
63	50:22	50:60
64	50:23	50:61
65	50:30	50:62
66	50:31	50:63
67	50:32	50:72
70	50:33	50:73
71	50:34	50:74
73	50:35	
77	50:36	
50:01	50:37	
50:02	50:50	

I AND R1 SEQUENCES		
02	12	33
03	13	51
04	14	52
05	15	53
06	16	54
07	17	55
10	32	56
11		

I, R1, AND R1R2 SEQUENCES
20
21
22
23

I AND EXTENDED SEQUENCES		
50:41	50:43	50:46
50:42	50:45	50:47

I, R1, AND EXTENDED SEQUENCES
24
25
26
27

I AND W SEQUENCES	
40	46
41	47
42	72
43	74
44	75
45	76

I, EXTENDED, AND W SEQUENCE
50:44

I AND WAIT SEQUENCES
50:24
50:25

I, R1, AND W SEQUENCES
30
31
57

TABLE 7-14. COMMAND SEQUENCES OF EACH INSTRUCTION (Cont'd)

I, IB1, AND IB2 SEQUENCES		
50:11	50:12	50:13
I, I/0 1, and (if Dual or ESI term I/0 2		
50:26	50:27	

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T4.4	CLR S1	Norm. Sequence	20N12
	Inhibit Cont Mem → Z0	Z1 → Z0•$\overline{CM \rightarrow Z0}$ (T13•I Seq. $\overline{Cont.\ Data}$ via 10N13-23)	11N11-25
T1.1	Spec. Int. Reg → S1	Int SEQ., Spec Int. Reg	70N12-22
	P → S1	Norm. SEQ	29N12-22
	Set Resume f/f	f=50:20	00E18-53
	Set Resume Fault ff	RTC Seq. B=1024• Resume not available	11G18-54
	CLR AL	f=(50:61+50:62)• T52	07N05-20
	500_8 → S1	Load Mode	60N12-22
	Enable Main Memory	Norm. SEQ	OXG80-134
	I/O XLATOR → SØ	Initiate Buffer Inst.'s	10N10-24
	ICR → SØ	f=32, 33, 36, 37+(f=56• $\overline{EQUAL}$)+ (f=73• B≠0)	40N10-24
	Initiate Cont. Mem.	(I/O/XLATOR + ICR) → SØ	OXDT10-122
	Set Increment P f/f	$\overline{Int.\ SEQ}$	10L10-35
	CLR ZØ	$\overline{Cont.\ Data\ SEQ.}$	09N11-25
	Data.REQ → Chan. Priority	Normal SEQ	00N61-49
	I/0 XLATOR → S1 (Bits 4, 5, 7)	Int. SEQ•$\overline{Spec.\ Int}$•Cont. Data	30N12-22

*Entries in this column reference the gate and plate number to be found on the applicable functional schematic contained in Chapter 9.

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.2	ADDER → AL	f=(50:61+50:62) T52	18N05-20
	B±1 → ZØ	f=(56+73) Cont. Mem. Timing	39N11-25
	S1 → P	Load Mode	20N07-21
	Z1 → ZØ $\overline{\text{Cont. Mem.}}$ → ZØ	$\overline{\text{Cont. Data SEQ.}}$	10N13-23
	Set Run 2 f/f	Run 1 f/f Set	1XJ10-3
	CLR P	Load Mode	07N07-21
T1.3	CLR Z1	Norm. SEQ	09N13-23
	CLR X W	Advance P	08N03-19
	CLR D	Advance P	08N02-18
	CLR CLR Hold ff	Hold 1 CLR	0XG38-28
	CLR Hold 2 f/f	Hold 1 CLR	2XG38-28
	CLR Parity f/f	Normal SEQ	0XG54-30
	CLR Select Stop f/f	Normal SEQ	00E60-31
	CLR EF/OD ACK Gen f/f	$\overline{\text{ACK DLY}}$	5XLg2-69
	CLR F Reg.	$\overline{\text{Initiate Buffer}}$	06N16-40
	CLR Mon. (4 Spec. Int. Reg f/f's)	Int SEQ	00N41-53
	Set 0XL11 f/f	0XL10 Set	0XL11-35
T1.4	Set Inhibit EAB f/f	Increment P f/f Set (Advance P)	18 18 27 30N02-36N02-OXG33
	PL ⟶ DL	Increment P f/f Set (Advance P)	18 18 18 30N02-36N02-38N02
	PU ⟶ DU	Increment P f/f Set (Advance P)	18 18 18 30N02-37N02-39N02

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.4 (Cont'd)	Set Parity f/f	Pairty ODD	0XG54-30
	CLR KØ	Normal SEQ	08N14-37
	Set Decrement P f/f	Force • Resume Fault	30L10-35
	Set Insert EAB f/f	Decrement P f/f Set	21E32-27
	Data REQ → Func. Priority	$\overline{I/0/} \cdot \overline{(Dual+ES1\ Term)} + \overline{C.D.\ SEQ}$	00N62-49
	Set all Int. Lockout f/f	Int SEQ	0XG70-28
T2.1	Clr Translator	$\overline{I/0/} \cdot \overline{(Dual+ES1\ Term)} + \overline{CD\ SEQ}$	00E00-49
	S1 → SØ	S1=CM or Boot Address	107 24 91S00-30N10
	CLR SEQ Desig. Lower Rank	$Run \cdot \overline{I/0} \cdot \overline{Hold\ 1}$	30E20-13
	Set Bootstrap f/f	S1=CM or Boot Address	39N10-24
	CLR CD SEQ f/f	T22	10G28-34
	CLR RTC SEQ f/f	T22	20G29-34
	CLR ZØ	$\overline{Cont.\ Data\ SEQ}$	00N11-25
	CLR Increment P ff	$\overline{T11}$	10L10-35
	Z1 → Z Sel	S1≠CM or Bootstrap Address Normal SEQ	10N00-107
	Ø's → Arith SEQ 6-11, 12-17	$\overline{Initiate\ Buffer}$	70N01-17
	Z Sel → Arith Sel	Normal SEQ	40N01-17
	MEM → Z1	$\overline{I/0} \cdot \overline{W}$	10N13-23
T2.2	SEQ Desig. Upper → Lower	$Run \cdot \overline{I/0} \cdot \overline{Hold\ 1}$	42E20-13
	CLR P	ADVANCE P	07N07-21

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T2.2 (Cont'd)	ADDER → P	ADVANCE P	19N07-21
	REQ → XLATOR	$\overline{\text{I/O} \cdot \text{Force} \cdot \text{RTC SEQ}}$	10E00-49
	Set RTC SEQ f/f	RTC REQ• $\overline{\text{I/O (f=20-23, 57) R1}}$	40E00-49
T2.3	CLR Insert and Inhibit EAB f/fs	Normal SEQ	02E32-27
	CLR X• W	Normal SEQ	08N03-19
	CLR D	Normal SEQ	08N02-18
	CLR 0XL11 f/f	0XL10 CLR	00L10-35
	CLR Main Mem Enbl f/f	Normal SEQ	11G81-134
T2.4	Arith Sel → D	Normal SEQ	18N02-18
	Arith Sel → X	Initiate Buffer (B SEQ's)	20N03-19
	$\overline{\text{Arith Sel}}$ → X	Initiate Buffer (B SEQ's)	20N03-19
	Ø Sel 0-5 → KØ	$\overline{\text{I/O SEQ}}$	29N14-37
	Ø Sel 12-17 → F	Format I• $\overline{\text{Initiate Buffer}}$	19N16-40
	Ø Sel 06-11 → F	Format II• $\overline{\text{Initiate Buffer}}$	29N16-40
T3.1	Mon Int. Req → Chan Prio	$\overline{\text{I/O}}$	00N63-49
	Drop Z1 → Ø Sel	T24 f/f CLR	10N00-107
	Z0 → Ø Sel	T24 f/f CLR	10N00-107
	ICR → SØ	Normal SEQ	48N10-24 (24) (122)
	Initiate Control Mem	ICR → SØ	49N10-01DT10

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.1 (Cont'd)	CLR Skip f/f	Normal SEQ	0XG50-31
	CLR I/0 XLATORS	Normal SEQ	21E00-49
	CLR Zø	$\overline{\text{C. D. SEQ}}$	09N11-25
	Z Sel → Arith Sel	f=00-47• ODD	40N01-17
	AL → Arith Sel	f=71	20N01-17
	AU → Arith Sel	f=50:60, 62, 63	10N01-17
T3.2	Set Skip f/f	Skip Cond. Met	0XG50-31
	f•K → I/O XLATOR	Norm SEQ	21E00-49
	CLR B	Norm SEQ	08N08-21
T3.3	CLR D	f=50:21-23, 50-55, 57, 60, 62, 63	20N02-18
	CLR ICR	f=50:72	30N02-18 10E44-38
	CLR SR	f=50:73	10E40-38
	Set RTC Mon REQ f/f	f=50:14	0XG15-54
T3.4	Arith Sel → D	f=50:60	19N02-18
	$\overline{\text{Arith Sel}}$ → D	f=50:62, 63	29N02-18
	P → D	f=50:21-23+50-55+57	30N02-18
	Set Du6 (Sign Ext.)	f=36, 37, 70, 71, & D Lower 12 Neg	50N02-18
	Mon REQ → Function Prio	$\overline{\text{I/0}}$• f≠I/0	00N64-49
	Set Hold 1 f/f	f=50:26+27+40-47	IXG38-28

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.4 (Cont'd)	SR → D 12-15	f=00-27, 32, 33, 40-47 & SR BIT 3=1	40N02-18
	PU → DU	(f≠36, 37, 70, 71) ($\overline{\text{INT SEQ}}$, B SEQS, I/O, OR HOLD 2) ($\overline{\text{SR ACT}}$+f=30, 31, 34-37 + f≠00-47)	39N02-18
	Set Ext. Int Lockout f/f	f=50:36, 37	0XG71-28
	CLR Ext Int Lockout f/f	f=50:32, 33	0XG71-28
	Chan → Input Ack	Set ID Ack • Group g	2gN49-58
	Set ID Ack	I/O • $\overline{\text{OUT+EF}}$	00N49-53
	Set Resume	50:22	00E18-53
	Arith Sel → X	Format II • f=60-63 • Set X=1's +(Format I)	18N03-19
	$\overline{\text{Arith Sel}}$ → X	Format II • f=60-63 Set X=1's	20N03-19
	Zø → B	$\overline{\text{I/O}}$ + $\overline{\text{ESA}}$	29N08-21
	Input → B	I/O + ESA	19N08-21
	Set Inhibit EAB f/f	(f=50:60 • $AU_{17} \neq AL_{17}$) + (f=50:21-23, 50-55, 57)	11E33-27 36N02-18
	Set Insert EAB f/f	f=50:60 • Set X=1 (AL=Pos) $AU_{17} \neq AL_{17}$	10E32-27
	Set All Int Lockout f/f	Format II • f=34+35	0XG70-28
	CLR All Int Lockout f/f	(f=54, 55 • f=EVEN)+(f=30, 31, 76)	00E70-28
	Sample Sel Stop f/f	f=50:56	10E60-31
	K_0 - K_2 → ICR	f=50:72	19E44-38

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.4 (Cont'd)	K_0 - K_4 → SR	f=50:73	19E40-38
	Set Inst Fault f/f	f=00, 01+77	1XG14-54
	CLR Scale Factor f/f	f=50:40-47	10L01-36
T4.1	Enable Shift SEQ	f=50:40-47	10L01-36
	CLR Run 1 f/f	Stop	25J10-3
	CLR Upper Rank SEQ Desig.	Norm SEQ	09E20-12
	Select Run	$\overline{\text{Phase Mode}} \cdot \overline{\text{OP Step Mode}} \cdot \overline{\text{LOAD}}$	00J00-3
	CLR AU	f=50:62, 63	11N04-20
	CLR AL	f=70, 71, 50:60	10N05-20
	Set Resume f/f	Test Resume via INTERCOMPUTER-NORMAL Switch (normal mode) +ODR (IA from second computer) via INTERCOMPUTER/NORMAL SWITCH + $\overline{\text{CHAN} \cdot \text{EF/OD ACK}}$	53Lg0-69
	CLR ZØ	$\overline{\text{C.D. SEQ}}$	09N11-25
	CLR B±1 f/f	Norm SEQ	0XG37-27
	CLR I/0 XLATOR	$(f \neq I/0) \cdot \overline{I/0}$	00E00-49
	CLR Compare Desig.	f≠60-67 + f≠50:60-67	00E34-29
	AL → Arith Sel	50:61, 63	20N01-17
	Set Active ff	50:01-03	00N44-53

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T4.2	Set Run f/f	Start	0XJ10-3
	Set Wait SEQ f/f	f=50:24+50:25	20G27-12
	Set B1 SEQ f/f	f=50:10-13 • $\overline{\text{B1 SEQ}}$	22G20-12
	Set W SEQ f/f	f=(40-47+72, 74-76) • $\overline{\text{Format II}}$	20G23-12
	Set R1 SEQ f/f	f=(02-33, 50-57) • Format I	20G22-12
	Set I SEQ f/f	f=Format I, Spec Int. Fault	21G21-12
	Adder → AU	f=50:62+50:63	19N04-20
	Adder → AL	f=70, 71, 50:60	19N05-20
	CLR P Adder → P	(f=50:21-23, 50-55, 57 & Skip)+ (f=34, 35, 60-67, 73 & JP)	10N07-21
	XLATOR 1 - XLATOR 2	I/0 SEQ	33E00-49
	Set B ± 1 ff	f=73+I/0 • $\overline{\text{RTC SEQ}}$ • Backward Buffer	0XG37-27
	CLR A neg & Y neg f/f's	Norm SEQ	11T42-15
	CLR Hold 1 ff	CLR Hold f/f Set	1XG38-28
	Set Overflow f/f	f=71 • (X • D POS) • $\overline{\text{Brw}}$ Bit 17 + f=71 • (X • D Neg) • Brw Bit 17	0XG52-30
	REQ → XLATOR	$\overline{\text{I/0 SEQ}}$ • f≠I/0 • $\overline{\text{SPEC INT REQ}}$	11E00-49
	Set 6XLg0 (Enbl ID ACK)	Chan → Input Ack (see T3.4)	6XLg0-70
	Set Resume f/f	Set Resume (see T3.4)	5XLg0-69
	CLR CLR Hold f/f	Hold 1 f/f CLR	0XG38-28

TABLE 7-15. I SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T4.3	Set Hold 2 f/f	Hold 1 f/f Set	2XG38-28
	CLR CLR Hold ff	Hold 1 ff CLR	0XG38-28
	CLR Insert & Enhibit EAB f/f	Norm SEQ	02E32-27
	Set Spec. Int XLATOR f/f's	$\overline{\text{Inst Fault}}$	21E15-55
	Enbl Mem Protect	Voltage Fault• $\overline{\text{Battle Short}}$	1XG81-134
	CLR D	f=50:61,63	20N02-18
	CLR ≠1	f=36,37+Initiate Buffer	09N13-23
	CLR $\overline{\text{Term}}$ f/f	Norm SEQ	0XG19-106
	CLR Active f/f's	f=50:15-50:17	01N43-53
T4.4	$\overline{\text{Arith Sel}}$ → D	f=50:61 + 50:63	20N02-18
	Adder → ≠1	f=36+37 + Initiate Buffer	39N13-23
	CLR Overflow f/f	f=50:52 + 50:53	0XG52-30
	Set $\overline{\text{Term}}$ f/f	$B_U \neq Z\emptyset + (B_{16} \& B_{17} \neq Z\emptyset_{16} \&_{17}$• RTC SEQ	0XG19-106
	CLR S1	Normal SEQ	20N12-22
	Set Cont Data SEQ f/f	I/0 SEQ• B≠Z∅• CDM Bit Set •$\overline{\text{1218 Mode}}$	03G28-34

TABLE 7-16. R SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T4.4	CLR S1	Normal SEQ	10N12-22
T1.1	Adder → S1	Normal SEQ	10N12-22
	ICR → SØ	f=56• EQ CLR + f=73• B≠0	40N10-24
	Initiate Cont. Mem.	ICR → SØ	01DT10-122
	Enable Main Mem.	Normal SEQ	0XG80-134
	CLR ZØ	C. D. SEQ	00N11-25
	AL → Arith Sel	f≠02, 03, 06, 07, 14-17, (20-23• $\overline{R2}$) 24, 25, 44, 45, 53, 74	20N01-17
	AU → Arith Sel	f=04, 05, 06, 07, 26, 27, 46, 47, 20-23• R2 SEQ	10N01-17
	Z (Sel) → Arith Sel	f=42, 43	40N01-17
	0's → Arith Sel 06-17	f=74	70N01-17
	SR + Icr+K → Arith Sel	f=40, 41, 72, 75	50N01-17
T1.3	CLR X•W	f≠57	00N03-19
	CLR D	f=04, 05, 24-27, 53	20N02-18
	Set A Neg f/f	f=(24+25)• AL Neg +f=(26+27)• A_u Neg	00E30-33
	CLR Z1	Normal SEQ	09N13-23
T1.4	Arith Sel → X	f≠24-27	10N03-19
	$\overline{\text{Arith Sel}}$ → D	f=04, 05, 24-27, 53	20N02-18

TABLE 7-16. R SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.4 (Cont'd)	CLR K0	$\overline{I/O}$	09N14-37
	Cont. Mem → Z$\emptyset$	$\overline{CD\ SEQ}$ • CM Timing • Strobe EAB	11N11-25
T2.1	CLR AU	A Neg	11N04-20
	CLR AL	f=(24,25) • A Neg	10N05-20
	Set K0=22_8	f≠X4, X5	39N14-37
	Set K0=23_8	f=X4, X5	39N14-37
	Z Sel → Arith Sel	Normal SEQ	40N01-17
	AL → Arith Sel	f=52	20N01-17
	AU → Arith Sel	f=06,07	10N01-17
T2.2	Adder → AL	A Neg	10N05-20
	Adder → AU	f=(24+25) • A Neg	11N04-20 10N04-20
T2.3	CLR D	f≠04,05,53	09N02-18
	CLR Inhibit & Insert EAB f/f	Normal SEQ	02E32-27
T2.4	Set Inhibit EAB f/f	f=20-23	10E33-27
	Set Y Neg f/f	f=(24-27) • Y Neg	1XG30-33
	Arith Sel → D	(f≠02,03,06,07,16,17,22,23,53,56) f=(24+25) • Y pos + f=(26+27) • Y Neg	18N02-18 27N02-18
	$\overline{\text{Arith Sel}}$ → D	(f=02,03,06,07,16,17,22-27,53,56) f=(24+25) • Y Pos + f=(26+27) • Y Neg	20N02-18 27N02-18
	Arith Sel → X	f=53	10N03-19

TABLE 7-16. R SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.1	ICR - SØ	f=42,43,56	40N10-24
	Initiate Control Mem.	ICR → SØ	49N10-24
	CLR ZØ	$\overline{\text{CD SEQ}}$	00N11-25
	Set Increment P f/f	f=56	10L10-35
	AL → Arith Sel	f=04,05	20N01-17
T3.2	Enbl Compare Greater • EQ f/fs	Normal SEQ	10E34-29
	CLR Increment P f/f	f=56+X≠D	0XL10-35
	Set Overflow f/f	f=26+27•Adder → AU•f≠20-23+R2	21E52-30
	CLR B	Normal SEQ	08N08-21
T3.3	CLR X • W	Increment P f/f Set	08N03-19
	CLR D	Increment P f/f Set	30N02-18
	Control Memory → ZØ	Strobe C or B Mem • $\overline{\text{C D SEQ}}$ • CM Timing	11N11-25
T3.4	ZØ → B	$\overline{\text{I/O}}$ • $\overline{\text{ESA Mode}}$	10N08-21
	Arith Sel → X	f=04,05	10N03-19
	P → D	Increment P f/f Set	30N02-18
	Set Inhibit EAB f/f	Increment P f/f Set	36N02-18
T4.1	CLR AL	f=04,05,12-17,20-23 • $\overline{\text{R2 SEQ}}$, 51-53	08N05-20
	CLR AU	f=10,11	10N04-20
	CLR Borrow Test f/f	f=20-23	0XG51-30

TABLE 7-16. R SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T4.2	CLR P		
	ADDER → P	f=54+55 + Advance P	07N07-21 18N07-21
	ADDER → AL	f=04,05,12-17, 20-23, 51-53	19N05-20
	ADDER → AU	f=10,11	10N04-20
	Set Borrow Test f/f	EAB • f=20-23	01G51-30
T4.3	CLR Z1	f=32,33	30N13-23
T4.4	ADDER → Z1	f=32,33	39N13-23
	R1/R2 SEQ		
T4.4	Inhibit CLR S1	Normal SEQ	10N12-22
T1.1	Set S1 Bit 0=1 (Starts at T2.2)	Normal SEQ	50N12-22
	AU → Arith Sel	f=20-23 + 26,27	10N01-17
T2.4	Set Insert EAB f/f	Borrow Test f/f Set • f=20-23	11E32-27
T4.1	CLR AU	f=20-23	08N04-20
	CLR Borrow Test f/f	f=20-23	10E51-30
T4.2	ADDER → AU	f=20-23	19N04-20
	Set Borrow Test f/f	EAB• f=20-23	01G51-30

TABLE 7-17. W SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T4.3	Set Spec Int XLATOR = 17	f=50:44	20E15-55
T4.4	CLR S1	f≠57	12F57-22
	Set Insert EAB f/f	f=57 • Y ≠ 0 (X≠D')	20E32-27
T1.1	ADDER → S1	f≠57	12F57-22
	Spec. Int XLATOR → S1	f=50:44	30N12-22
	ICR → SØ	f=42,43	40N10-24
	Initiate Control Mem.	ICR → SØ	01DT10-122
	CLR ~~Z~~Ø		09N11-25
	P → Arith Sel	f=30,31,76	30N01-17
	0's → Arith Sel	f=40,41,72,75	50N01-17
	~~Z~~ (Sel) → Arith Sel	f=42,43,56	40N01-17
	AU → Arith Sel	f=46,47,26,27	10N01-17
	AL → Arith Sel	f=44,45	20N01-17
	ICR → Arith Sel	f=72	50N01-17
	SR → Arith Sel	f=75	50N01-17
	K0 → Arith Sel	f=50:44	90N01-17
	Arith Sel → X	f≠24-27	10N03-19
	0's → Arith Sel 12-17	f=74	70N01-17

*Gate and plate numbers (see Functional Schematics) are referenced.

TABLE 7-17. W SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.3	CLR Z1	Norm. SEQ	09N13-23
	CLR X•W	f≠57	08N03-19
T1.4			
	Store Sel → Z1	f≠57	29N13-23
	ADDER → Z1	f=57	39N13-23
	Z1 → ZØ	f=30, 31, 40-47, 57, 76	10N13-23
T2.1	S1 → SØ	S1 - C or Boot Mem. Address	30N10-24
	CLR Z0	$\overline{\text{C D SEQ}}$	09N11-25
	Initiate Control Mem.	S1 → S0	01DT10-122
	Inhibit Strobe Main & Control Memory	f=30, 31, 40-47, 57, 76	10N13-23
	Inhibit Strobe 0-5 ZØ• $\overline{\text{Z1}}$	f=72, 74, 75, 76	13N13-23
	Inhibit Strobe 0-11 ZØ• $\overline{\text{Z1}}$	f=74	12N13-23
T2.2	CLR P	f=30, 31, 76	09N07-21
	S1 → P	f=30, 31, 76	29N07-21
T2.3	CLR Insert• Inhibit EAB f/f's	Normal SEQ	02E32-27
	CLR SR	f=75	09E40-38
T3.1	Set Increment P f/f	f=30, 31, 76, (57• $\overline{\text{SKIP}}$)	10L10-35

TABLE 7-17. W SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.3	CLR X•W	Advance P	08N03-19
	CLR D	Advance P	30N02-18
T3.4	P → D	Advance P	30N02-18
	Set Inhibit EAB ff	Advance P	36N02-18
	Arith Sel → X	f=04,05	10N03-19
T4.2	CLR P	Advance P	08N07-21
	ADDER → P	Advance P	18N07-21

TABLE 7-18. IB1 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T4.4	CLR SI	Norm SEQ	20N12-22
T1.1	P → SI	Norm SEQ	29N12-22
	Enable Main Memory	Norm SEQ	0XG80-134
	Set Increment P ff	$\overline{\text{Int. SEQ}}$	10L10-35
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
T1.3	CLR Z1	Norm. SEQ	09N13-23
	CLR X, W	Adv. P	08N03-19
	CLR D	Adv. P	08N02-18
	Inhibit CLR F Reg	Initiate Buffer	06N16-40
	Set 0XL11 ff	0XL10 Set	0XL11-35
T1.4	Set Inhibit EAB ff	Increment P ff Set	18 18 27 30N02-36N02-0XG33
	PL → DL	Increment P ff Set	18 18 18 30 N02-36N02-38N02
	PU → DU	Increment P ff Set	18 18 18 30N02-37N02-39N02
	Inhibit CLR K0	Initiate Buffer (B SEQ)	09N14-37
T2.1	CLR SEQ Desig. Lower Rank	Run·$\overline{\text{I/0·HOLD 1}}$	30E20-13
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	00N11-25
	Z1 → Z Sel	Normal SEQ	10N00-107
	Inhibit 0's Arith Sel 12-17	Initiate Buffer	70N01-17
	CLR Increment P f/f	$\overline{\text{T11}}$	10L10-35
	Z Sel - Arith Sel	Normal SEQ	40N01-17

*Gate and plate numbers (see Functional Schematics) are referenced.

TABLE 7-18. IB1 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T2.2	Sequence Designator, Upper Rank → Lower Rank	Run • $\overline{I/O}$ • $\overline{HOLD\ 1}$	42E20-13
	Set I_f ff	I_i ff set	1XG20-13
	Set $B1_f$ ff	$B1_i$ ff set	5XG20-13
	Mem. ⟶ Z1	$\overline{T13}$	10N13-23
	CLR P	Adv P	07N07-21
	Adder ⟶ P	Adv P	18N07-21
T2.3	CLR EAB f/f	Normal SEQ	02E32-27
	CLR X-W	Normal SEQ	08N03-19
	CLR D	Normal SEQ	08N02-18
	CLR 0XL11 f/f	0XL10 CLR	00L10-35
	CLR Main Mem. Enbl f/f	Normal SEQ	0XG80-134
T2.4	Arith Sel ⟶ D	Normal SEQ	18N02-18
	Arith Sel ⟶ X	Initiate Buffer (B SEQ's)	20N13-19
	$\overline{\text{Arith Sel}}$ ⟶ X	Initiate Buffer (B SEQ's)	20N13-19
	Inhibit Z Sel 0-5 ⟶ KØ	Initiate Buffer (B SEQ's)	29N14-37
	Inhibit Z Sel 12-17 ⟶ F	Initiate Buffer	19N16-40
	Inhibit Z Sel 06-11 ⟶ F	Initiate Buffer	29N16-40
T3.1	Drop Z1 ⟶ Z Sel	T24 f/f CLR	10N00-107
	Drop Z Sel ⟶ Arith Sel	T24 f/f CLR	40N01-17
	≠0 → Z Sel	T24 f/f CLR	10N00-107

TABLE 7-18. IB1 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.1 (Cont'd)	ICR → S0	Normal SEQ	48N10-24
	Initiate Control Mem.	ICR → S0	24 122 49N10-0XDT10
	CLR I/0 XLATORS	Normal SEQ	21E00-49
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
T3.2	f • K0 → I/0 XLATOR	Normal SEQ	21E00-49
T3.3			
T3.4			
T4.1	Inhibit CLR Run 1 ff	B SEQ	24J10-3
	CLR Upper Rank SEQ Desig	Normal SEQ	08E20-12
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
	CLR B $\pm$ 1 ff	Normal SEQ	0XG37-27
T4.2	Sequence Designator, Lower Rank - Upper Rank	$\overline{\text{I/0}}$	12E20-12
	Set $B2_i$ SEQ ff	$B1_f$ ff Set	6XG20-12
	Set I SEQ f/f	Normal SEQ	21G20-12
T4.3	CLR EAB f/fs	Normal SEQ	02E32-27
	CLR Z1	Initiate Buffer	31N13-23
T4.4	Adder — Z1	Initiate Buffer	31N13-23
	Clear S1	Normal SEQ	09N12-22
	Disable CM → Z0	$\overline{\text{Cont. Data SEQ}}$	10N13-23

TABLE 7-19. IB2 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T1.1	P → S1	Normal SEQ	29N12-22
	Enable Main Memory	Normal SEQ	0XG80-134
	I/0 XLATOR → S0	Initiate Buffer Inst.'s	19N10-24
	Initiate Cont. Mem.	(I/0 XLATOR) → S0	0XDT10-122
	Set Increment P f/f	$\overline{\text{Int. SEQ}}$	10L10-35
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
T1.2	Z1 → Z0	Z1 → Z0 • $\overline{\text{CM} \rightarrow \text{Z0}}$ • (f ≠ 56, 73)	29N11-25
T1.3	CLR Z1	Normal SEQ	09N13-23
	CLR X, W	Advance P	08N03-19
	CLR D	Advance P	08N02-18
	Inhibit CLR F Reg.	Initiate Buffer	06N16-40
	Set 0XL11 f/f	0XL10 Set	0XL11-35
T1.4	Set Inhibit EAB f/f	Increment P f/f Set	18 18 27 30N02-36N02-0XG33
	PL → DL	Increment P f/f Set	18 18 18 30N02-36N02-38N02
	PU → DU	Increment P f/f Set	18 18 18 30N02-37N02-39N02
	Inhibit CLR K0	Initiate Buffer	09N14-37
	Drop Disable CM → Z0	T13 Clear	10N13-23

*Gate and plate numbers (see Functional Schematics) are referenced.

TABLE 7-19. IB2 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T2.1	CLR SEQ Desig. Lower Rank	Run•$\overline{I/0}$•$\overline{\text{Hold 1}}$	30E20-13
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	00N11-25
	Z1 → Sel	Normal SEQ	10N00-107
	Inhibit 0's → Arith SEQ 12-17	Initiate Buffer	70N01-17
	Z Sel → Arith Sel	Normal SEQ	40N01-17
T2.2	SEQ Desig. Upper → Lower	Run• $\overline{I/0}$• $\overline{\text{Hold 1}}$	42E20-13
	Set I_f ff	I_i ff set	1XG20-13
	CLR P	Advance P	07N07-21
	ADDER → P	Advance P	18N07-21
	Memory → Z1	$\overline{\text{Cont. Data SEQ}}$	11N13-23
	Set $B2_f$ ff	$B2_i$ ff Set	7XG20-13
T2.3	CLR EAB f/f	Normal SEQ	02E32-27
	CLR X W	Normal SEQ	08N03-19
	CLR D	Normal SEQ	08N02-18
	CLR 0XL11 f/f	0XL10 CLR	00L10-35
	CLR Main Mem. Enbl f/f	Normal SEQ	0XG80-134
T2.4	Arith Sel → D	Normal SEQ	18N02-18
	Arith Sel → X	Initiate Buffer (B SEQ's)	18N03-19
	$\overline{\text{Arith Sel}}$ → X	Initiate Buffer (B SEQ's)	28N03-19
	Inhibit Z Sel 0-5 → K0	Initiate Buffer (B SEQ's)	29N14-37

TABLE 7-19. IB2 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T2.4 (Cont'd)	Inhibit Z Sel 12-19 → F	Initiate Buffer	19N16-40
	Inhibit Z Sel 06-11 → F	Initiate Buffer	29N16-40
T3.1	Drop Z1 → Z Sel	T24 f/f CLR	10N00-107
	ICR → S0	Normal SEQ	48N10-24 24 122
	Initiate Control Mem.	ICR - S0	49N10-0XDT1(
	CLR I/0 XLATORS	Normal SEQ	02E00-49
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
T3.2	Drop Z Sel - Arith Sel	Normal SEQ	40N01-17
	f & K0 → I/0 XLATOR	Normal SEQ	23E00-49
T4.1	Inhibit CLR Run 1 f/f	B SEQ's	24J10-3
	CLR Upper Rank SEQ Desig	Normal SEQ	08E20-12
	CLR Z0	$\overline{\text{Cont. Data SEQ}}$	09N11-25
	CLR B ± ff	Normal SEQ	0XG37-27
T4.2	Sequence Designator, Lower Rank → Upper Rank	$\overline{\text{I/0}}$	12E20-12
T4.3	Set I SEQ f/f		21G20-12
T4.3	CLR Z1	Initiate Buffer	31N13-23
	Set Active ff (as designated by f & K0)	ID, OD + EF	0XG05, 0XG04-51

TABLE 7-19. IB2 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T4.4	Adder → Z1	Initiate Buffer	31N13-23
	Disable CM → Z0	$\overline{\text{Cont Data SEQ}}$	10N13-23
	NOTE: At this point, computer enters I Sequence of Next Instruction		
T1.1	P → S1	Normal SEQ	29N12-22
	I/0 Translator → S0	Initiate Buffer	19N10-24
	Set S0 2°	B2 SEQ	50N10-24
	Enable Main Memory	Normal SEQ	0XG80-134
	Initiate Control Memory	Initiate Buffer	19N10-24
	Set INCR P ff	$\overline{\text{Int. SEQ}}$	10L10-35
T1.2	Z1 → Z0	Cont. Data SEQ (f ≠ 56, 73)	29N11-25
T1.3	CLR Z1 CLR X, W	Normal SEQ Advance P	09N13-23 08N03-19
	CLR F	$\overline{\text{Initiate Buffer}}$	06N16-40
	CLR D	Advance P	08N02-18
T1.4	Drop Disable CM → Z0	T 13 CLR	10N13-23

* Gate and Plate numbers (see Functional Schematics) are referenced.

TABLE 7-20. I/0 1 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION				REFERENCE*
		SINGLE	DUAL	ESI	ESA	
T3.1	I/0 XLATOR → S0	Not EI	Not EI	--	--	19N10-24
	ESI → S0	--	--	Not EI	--	29N10-24
	Initiate Control Memory	Not EI	Not EI	Not EI	--	19N10-24, 29N10-24
	Set S0 → 2°	x	x	x	--	50N10-24
	CLR Z0	x	x	x	x	09N11-25
T3.2	CLR B	x	x	x	x	09N08-21
T3.3	Control Memory → Z0	Not EI	Not EI	Not EI	--	11N11-25
T3.4	Z0 → B	x	x	x	--	29N08-21
	Odd Input Chan → B	--	--	--	Not EI	19N08-21
T4.1	I/0 XLATOR → S0	Not EI	Not EI	--	--	19N10-24
	ESI → S0	--	--	Not EI	--	29N10-24
	Initiate Control Memory	Not EI	Not EI	Not EI	--	19N10-24, 29N10-24
	Set B ± Desig to + 1	x	x	x	x	0XG37-27
	CLR Z0	x	x	x	x	09N11-25
	CLR XLATOR II	x	x	x	x	32E00-49
T4.2	XLATOR I → XLATOR II	x	x	x	x	33E00-49
	Set B ± 1 Desig to -1					
	If bkwd buffer bit set	Not EI	Not EI	Not EI	--	0XG37-27

*Entries in this column indicate gate and plate numbers on applicable functional schematic contained in Volume 2 Part 3.

TABLE 7-20. I/0 1 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION				REFERENCE*
		SINGLE	DUAL	ESI	ESA	
T4.3	CLR Resume FF	OD/EF	OD/EF	OD/EF	OD/EF	00N40-53
	Set Input Ack. Register	ID/EI	ID/EI	ID/EI	ID/EI	00N049-53
	CLR ID/EI req FF	ID/EI	ID/EI	ID/EI	ID/EF	4gN40-57
	Control Memory → Z0	Not EI	Not EI	Not EI	--	11N11-25
	Terminate	BU = Z0	BU = Z0	BU = Z0		0XG19-106
T4.4	Set CDM Req FF if CDM	BU = Z0	BU = Z0	BU = Z0		03G28-34
T1.1	I/0 XLATOR → S0	Not EI	Not EI	--	--	19N10-24
	ESI → S0	--	--	Not EI	--	29N10-24
	Initiate Control Memory	Not EI	Not EI	Not EI	--	19N10-24, 29N10-24
	CLR Z0	x	x	x	x	09N11-25
	Set S0 → 2°	x	x	x	x	50N10-24
	B → S1	Not EI	Not EI	Not EI	Not EI	49N12-22
	I/0 XLATOR → S1	EI	EI	EI	EI	39N12-22
	Set S1 → 2° and 2^6	EI	EI	EI	EI	58N12-22, 35N12-22
	Enable Main Memory	x	x	x	x	54MT01-136
T1.2	B ± 1 → Z0	Not EI	Not EI	Not EI	Not EI	39N11-25
	CLR OD/EF Ack Reg	OD/EF	OD/EF	OD/EF	--	3gN48-68
T1.3	CLR Z1	x	x	x	x	09N13-23
	CLR ID Active FF	Terminate	Terminate	Terminate		
		ID & CDM	ID & CDM	ID & CDM		02N43-53
	Set EI Monitor	EI	EI	EI	EI	7GN42-56

TABLE 7-20. I/O 1 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION				REFERENCE*
		SINGLE	DUAL	ESI	ESA	
T1.3 (Cont'd)	Set Monitor FF if Monitor bit set	Terminate	Terminate	Terminate	Terminate	00N42-53
	Set Terminate OD/EF FF	Terminate & CDM	Terminate & CDM	Terminate & CDM		
	Set OD/EF Ack. Reg.	OD/EF	OD/EF	OD/EF	OD/EF	00N48-53
	CLR OD/EF Req. FF	OD/EF	OD/EF	OD/EF	OD/EF	5gN40-57, 6gN40-57
T1.4	Input Channel ⟶ Z1	ID/EI	ID/EI (evn chan if bkwd, odd if fwrd)	ID (evn chan if) EI (evn chn) if bkwd odd if fwrd)	ID (evn chn) EI (odd chn)	
	Start OD/EF Ack Timing	OD/EF		OD/EF & Terminate		00E06-53
	Start ID/EI Ack Timing	ID/EI	--	ID/EI & Terminate	ID/EI	00E04-53
T2.1	S1 ⟶ S0 if S1=CM address	x	x	x	x	39N10-24
	Initiate CM if CM address	x	x	x	x	39N10-24
	CLR Z0	x	x	x	x	09N11-25

TABLE 7-20. I/O 1 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION				REFERENCE*
		SINGLE	DUAL	ESI	ESA	
T2.2	Main Memory → Z1 Set I/O 2 SEQ (Lower rank) Set CDM SEQ Z1 → Z0 if CM address	OD/EF -- CDM REQ SET ID	OD/EF x -- ID	OD/EF Terminate CDM REQ SET TERM ID	OD/EF -- -- ID	11N13-23 1XG26-13 10E28-34 29N11-25
T2.3	Control Memory → Z0 CLRC	OD/EF and S0 OD/EF	OD/EF and S0 OD/EF	OD/EF and S0 OD/EF	OD/EF and S0 OD/EF	11N11-25 g2N60-58
T2.4	Z1 → Z SELECT Z0 → Z SELECT if CM Address Z SELECT → C	OD/EF OD/EF OD/EF	OD/EF OD/EF OD/EF (odd chan if fwrd or even chan if bkwd)	OD/EF OD/EF OD/EF (both chan)	OD/EF OD/EF OD/EF (both chan)	30N00-107 20N00-107 g4N60-58

TABLE 7-21. I/O 2 SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION		REFERENCE*
		DUAL	ESI	
T3.1	I/0 XLATOR → S0	Not EI	--	19N10-24
	Initiate Control Memory	Not EI	--	19N10-24
	Set S0 → 2°	x	--	50N10-24
	CLR Z0	x	x	09N11-25
T3.2	CLR B	x	x	09N08-21
T3.3	Control Memory → Z0	Not EI	--	11N11-25
T3.4	Z0 → B	x	x	29N08-21
T4.1	I/0 XLATOR → S0	Not EI	--	19N10-24
	Initiate Control Memory	Not EI	--	19N10-24
	Set B ± 1 Desig to +1	x	x	02G37-27
	CLR Z0	x	x	09N11-25
T4.2	XLATOR I → XLATOR II	x	x	33E00-49
	Set B ±1 Desig -1 if bkwd buffer bit set	x	x	03G37-27
T4.3	Control Memory → Z0	Not EI	--	11N11-25
	CLR Resume FF	OD/EF	OD/EF	00N40-53
	Set Input Ack Register	ID/EI	ID/EI	00N49-53
	CLR ID/EI Req FF	ID/EI	ID/EI	4gN40, 7gN40-57
	Terminate	B = Z0	B = Z0	0XG19-106

*Numbers in this column represent gate and plate numbers to be found on the applicable functional schematic contained in Chapter 9.

TABLE 7-21. I/0 2 SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION		REFERENCE*
		DUAL	ESI	
T4.4	Set CDM Req FF if CDM bit set	B = Z0	B = Z0	03G28-34
T1.1	I/0 XLATOR → S0	Not EI	--	19N10-24
	Initiate CM	Not EI	--	19N10-24
	CLR Z0	x	x	09N11-25
	Set S0 → 2°	x	--	50N10-24
	B → S1	Not EI	--	49N12-22
	I/0 XLATOR → S1	EI	x	39N12-22
	Set S1 2° and 2^6	EI	x	58N12-22, 35N12-22
	Initiate Main Memory	x	x	54MT01-136
T1.2	B ± 1 → Z0	Not EI	Not EI	39N11-25
T1.3	CLR OD/EF Ack Reg	OD/EF	OD/EF	3gN48-68
	CLR Z1	x	x	09N13-23
	CLR ID Active Ff	Terminate & CDM	Terminate & CDM	02N43-53
	Set EI Monitor	EI	EI	7GN42-56
	Set Monitor FF if Monitor Bit set	Terminate	Terminate	00N42-53
	Set Terminate OD/EF	OD/EF & Terminate & CDM	OD/EF & Terminate & CDM	00E12-53
	Set OD/EF Ack Reg.	OD/EF	OD/EF	00N48-53

TABLE 7-21. I/O SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION		REFERENCE*
		DUAL	ESI	
T1.3 (Cont'd)	CLR OD/EF Req. FF	OD/EF	OD/EF	5gN40-57, 6gN40-57
T1.4	Input Chan → Z1	ID/E (odd chan if bkwd., even chan if frwd)	ID EI (odd (even chan if frwd, odd if bkwd)	29N13-23
	Start OD/EF Ack Timing	OD/EF	OD/EF	00E06-53
	Start ID/EI Ack Timing	ID/EF	ID/EF	00E04-53
T2.1	S1 → S0 if S1 = CM address	x	x	39N10-24
	Initiate CM if CM	x	x	39N10-24
	CLR Z0	x	x	09N11-25
T2.2	Main Memory → Z1	OD/EF	OD/EF	11N13-23
	Set CDM SEQ	CDM Req. FF set	CDM Req. FF set	10E28-34
	Z1 → Z0 if CM address	ID	ID	29N11-25
T2.3	Control Memory → Z0 if CM address	OD/EF	OD/EF	11N11-25
	CLR C	OD/EF	OD/EF	g2N60-58
T2.4	Z1 → Z Select Z0 → Z Select if CM address Z Select → C	OD/EF OD/EF OD/EF (even chan if frwd or odd chan if bkwd)	-- -- --	30N00-107 20N00-107 g4N60-58

TABLE 7-22. CDM SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T3.1	XLATOR → S0	CDM Seq.	19N10-24
	Set 2XG28	CDM Seq.	2XG28-34
	$1 \rightarrow S0_{00}$	CDM Seq.	50N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	CLR Z0	$\overline{(T22 + T42)} \cdot$ CDM	09N11-25
T3.2	Drop Force 03G04 + 03G06	CDM Seq.	12G28-34
	CLR B	Normal SEQ	09N08-21
T3.3	Disable CM → Z0	$(T22 + T42) \cdot$ CDM	11N11-25
T3.4			
T4.1	XLATOR → S0	CDM Seq.	19N10-24
	$1 \rightarrow S0_{00}$	CDM Seq.	50N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	Inhibit Clear Z0	$(T22 + T42) \cdot$ CDM	09N11-25
T4.2	Force 03G04 = L	CDM Seq.	12G28-34
	Force 03G06 = H	CDM Seq.	13G28-34
T4.3	Enable CM → Z0	$\overline{(T22 + T42)} \cdot$ CDM	11N11-25
T4.4			
T1.1	XLATOR → S0	CDM Seq.	19N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	XLATOR → S1	CDM Seq.	39N12-22
	CLR Z0	$\overline{(T22 + T42)} \cdot$ CDM	09N11-24

*Entries in this column indicate gate and plate numbers to be found on applicable functional schematic contained in Volume 2 Part 3.

TABLE 7-22. CDM SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.2	Drop Force 03G04 & 03G06	CDM Seq.	12G28-34
T1.3	Disable CM ➔ Z0	(T22 + T42)· CDM	11N11-25
T1.4			
T2.1	S1 ➔ S0	CM Address	39N10-24
	Clear 1XG28		1XG28-34
	Inhibit Clear Z0	(T22 + T42)· CDM	09N11-25
	Clear OXG28		OXG28-34
	Initiate Control Memory	S1 ➔ S0	39N10-24
T2.2			
T2.3	Enable CM ➔ Z0	$\overline{(T22 + T42)}$· CDM	11N11-25
	Clear 2XG28	$\overline{\text{CDM Seq.}}$	2XG28-34

TABLE 7-23. RTC SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T2.2	Set RTC Sequence FF	RTC request	40E00-49
	Set XLATOR to RTC Address	RTC request	40E00-49
	Set I/0 1 FF (Lower Rank)	RTC request	40E00-49
T3.1	XLATOR → S0 (read RTC Count)	I/0 Seq	19N10-24
	Set S0 → 2°	I/0 Seq	50N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	CLR Z0	Normal Seq	09N11-25
T3.2	CLR B	Normal Seq	09N08-21
T3.3	Control Memory → Z0	Normal Seq	11N11-25
T3.4	Z0 → B	Normal Seq	29N08-21
T4.1	XLATOR → S0 (Read RTC Monitor Word)	I/0 Seq	19N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	Set B ± Designator to +1	Normal Seq	02G37-27
	CLR Z0	Normal Seq	09N11-25
T4.2	Set I/0 I FF (Upper Rank)	I/0 Seq	1XG25-13
T4.3	Control Memory → Z0	Normal Seq	11N11-25
T4.4	Set $\overline{\text{Terminate}}$ FF	B ≠ Z0	21B00-106 21B16-106

*Entries indicate gate and plate numbers on applicable functional schematic contained in Volume 2 Part 3.

TABLE 7-23. RTC SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T1.1	XLATOR → S0 (Store RTC Count (advanced))	I/0 Seq	19N10-24
	Set S0 → 2^0	I/0 Seq	50N10-24
	Initiate Control Memory	XLATOR → S0	19N10-24
	Set Resume fault FF	Resume signal not available after 1 second or, if ORDALT 8331 installed, after 1 millisecond	1XG18-54
	CLR Z0	Normal Seq	09N11-25
T1.2	B + 1 → Z0	I/0 Seq	39N11-25
	Set RTC Monitor FF	RTC MON REQ FF set and terminate	11E15-54
	Set RTC Overflow FF	B = 777777	11E17-54
	CLR Resume Fault monitors	Resume signal not available after 1 second or, if ORDALT 8331 installed, after 1 millisecond	85L00-34
T1.3	CLR RTC Monitor Request FF	RTC MON FF set	1XG15-54
	Inhibit Control Memory → Z0	I/0 Seq	11N11-25

TABLE 7-24. INTERRUPT SEQUENCE, ANALYSIS OF FUNCTIONS

TIME	COMMAND	CONDITION	REFERENCE*
T4.2	Set INT & I FF (Upper Rank)	I/0 Int	21G21-12
T4.3	Spec Int Req → Spec Int XLATOR $\overline{\text{Instruction Fault}}$		15G14-54
T1.1	Disable Adder → S1 of I SEQ	Int SEQ & Spec Int	19N12-22
	Disable P → S1 of I SEQ	Int SEQ	29N12-22
	SPECIAL INT REQ → S1	SPECIAL INT REQ	78N12-22
	Set S1 Bit → 2°	Resume, EI or RTC OVERFLOW	58N12-22
	I/0 Translator → S1 (Bits 4, 5, & 7)	Monitor INT and SP. INT REQ	39N12-22
	S1 → S0 & Initiate CM	if S1 = Control Memory Address	39N10-24
	Disable Set INCR P FF of I SEQ	$\overline{\text{B SEQ}}$	02G21-25
	CLR Z0	Normal SEQ	09N11-25
	Initiate Main Memory	Normal SEQ	54MT01-136
T1.3	Clear Processed interrupt	SP INT REQ	--
	Clear Inst Fault FF	Clear Fault	03N41-54
	Clear processed monitor	$\overline{\text{SP INT REQ}}$	--
	Control Memory → Z0	if S1 → S0 (above)	11N11-25
T1.4	Lockout all interrupts	Int SEQ	0XG70-28
T2.2	Set INT (Lower Rank) Set I (Lower Rank)	Int SEQ	1XG21-13 1XG20-13

*Entries indicate gate and plate numbers on applicable functional schematic contained in Volume 2 Part 3.

TABLE 7-24. INTERRUPT SEQUENCE, ANALYSIS OF FUNCTIONS (Cont'd)

TIME	COMMAND	CONDITION	REFERENCE*
T3.4	Disable PU → DU of I SEQ	f ≠ 36, 36, 70, 71 and SR is not active or f = 30, 31, 34, 35. f = 00-27, 32, 33, 40-47 and SR is Active	31N02-18 40N02-18
	Disable SR → D 12-15 of I SEQ		
	Disable Reinitiation of WAIT SEQ	Int SEQ	1XG21-13

* Gate and plate numbers are referenced.

TABLE 7-25. CONTROL AND BOOTSTRAP MEMORY ADDRESS ASSIGNMENTS

MEMORY ADDRESS	ADDRESS ASSIGNMENT
00000	Fault interrupt entrance register
00001 thru 00010	Index registers (8).
00011	Resume fault interrupt entrance register.
00012	RTC monitor interrupt entrance register.
00013	RTC overflow interrupt entrance register.
00014	RTC monitor word register.
00015	RTC word register.
00016	Synchronizing interrupt entrance register.
00017	Scale factor shift count word register.
00020 thru 00037	Continuous data mode (CDM) and external function (EF) buffer control registers for I/O channels 0 thru 7.
00020	CDM/EF for channel 0, terminal address
00021	CDM/EF for channel 0, current address
00022 ↕ 00037	CDM/EF for channel 1, terminal address CDM/EF for channel 7, current address
00040 thru 00057	Output buffer control (OBC) registers for I/O channels 0 thru 7
00040	OBC for channel 0, terminal address

TABLE 7-25. CONTROL AND BOOTSTRAP MEMORY ADDRESS ASSIGNMENTS (Cont'd)

MEMORY ADDRESS	ADDRESS ASSIGNMENT
00041	OBC for channel 0, current address
00042 ↕ 00057	OBC for channel 1, terminal address OBC for channel 7, current address
00060 thru 00077	Input buffer control (IBC) registers for I/O channels 0 thru 7
00060	IBC for channel 0, terminal address
00061	IBC for channel 0, current address
00062 ↕ 00077	IBC for channel 1, terminal address IBC for channel 7, current address
00220 thru 00237	Continuous data mode (CDM) and external function (EF) buffer control registers for I/O channels 10 thru 17.
00200	CDM/EF for channel 10, terminal address
00221	CDM/EF for channel 10, current address
00222 ↕ 00237	CDM/EF for channel 11, terminal address CDM/EF for channel 17, current address
00240 thru 00257	Output buffer control (OBC) registers for I/O channels 10 thru 17.
00240	OBC for channel 10, terminal address
00241	OBC for channel 10, current address

TABLE 7-25. CONTROL AND BOOTSTRAP MEMORY ADDRESS ASSIGNMENTS (Cont'd)

MEMORY ADDRESS	ADDRESS ASSIGNMENT
00242 ↕ 00257	OBC for channel 11, terminal address OBC for channel 17, current address
00260 thru 00277	Input buffer control (IBC) registers for I/O channels 10 thru 17.
00260	IBC for channel 10, terminal address
00261	IBC for channel 10, current address
00262 ↕ 00277	IBC for channel 11, terminal address IBC for channel 17, current address
500 ↕ 537	Bootstrap Addresses

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Section 7-4. Schematic Diagram of Printed Circuit Cards

7-83. GENERAL DESCRIPTION

7-84. Digital Computer Mk 152 Series generally utilizes two types of printed-circuit cards (types A and B) to supply the required circuitry for performing logic operations within the computer. The two types differ in the number of contact connections and in circuit content. Type A contains from one to five circuits and terminates in a 15-pin connector. Type B contains from one to 16 circuits and terminates in a 56-pin connector. Type B cards are used in memory logic and control to minimize space and provide maximum memory storage capability.

7-85. CARD TYPE NUMBERS. The last four digits of the actual Univac part numbers are shown on the functional schematic diagrams of Part 3. The last significant digit in the card type number (Univac part number) indicates the revision of the basic card. For example, card type 7002013 indicates the third revision of the basic 7002010 card. Any card with a higher revision number can replace a card with a lower revision number; however, a lower revision-numbered card cannot be used as a substitute for a higher revision-numbered card. Refer to table 2-6 (Printed Circuit Module Complement, Logic Circuits) and table 2-7 (Printed Circuit Module Complement, Memory Chassis) for a list of complete Univac Part Numbers. (Tables 2-6 and 2-7 are located in Volume 1 of this publication.)

7-86. CARD COLOR CODING. Each printed-circuit card is color coded. The RETMA scheme is employed which uses standard color coding according to the last four digits of the card number as shown in the functional schematics in Chapter 9. For example, the 2013 card (7002013) is color coded red (2), black (0), brown (1), and orange (3).

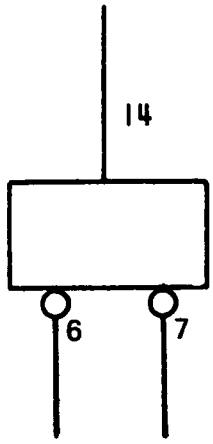
7-87. SCHEMATIC DIAGRAMS

7-88. TYPE A PRINTED CIRCUIT MODULES. Figures 7-15 through 7-61 depict the type A printed-circuit cards used in the computer. The descriptions are functional because they describe each circuit in terms of inputs and outputs rather than providing an explanation of internal electronic operation.

7-89. Computer Voltage Levels. Whenever possible, inputs and outputs are defined as lows or highs. In the computer, a low always implies a potential of -4.5, and high always implies ground potential of 0.0 volts.

7-90. The following information is contained in the card descriptions:

a. Card name and card type number.
b. Symbol used to represent the card on the functional schematics.
c. A logic description and a design description when applicable.



LOGIC SYMBOL

LOGIC DESCRIPTION

The output from this oscillator circuit is a square wave. The frequency of this output is normally controlled by the addition of an external potentiometer between pins 6 and 7. With this addition, the pulse rate may be varied between 2 and 200 Hz.

The amplitude of the output signal is from 0.0 volts to -15.0 volts.

This circuit is used to supply substitute timing pulses for maintenance and test purposes.

ELECTRICAL DESCRIPTION

The output from pin 14 is connected to the input of a 7002090 module with the ground return connected to pin 1.

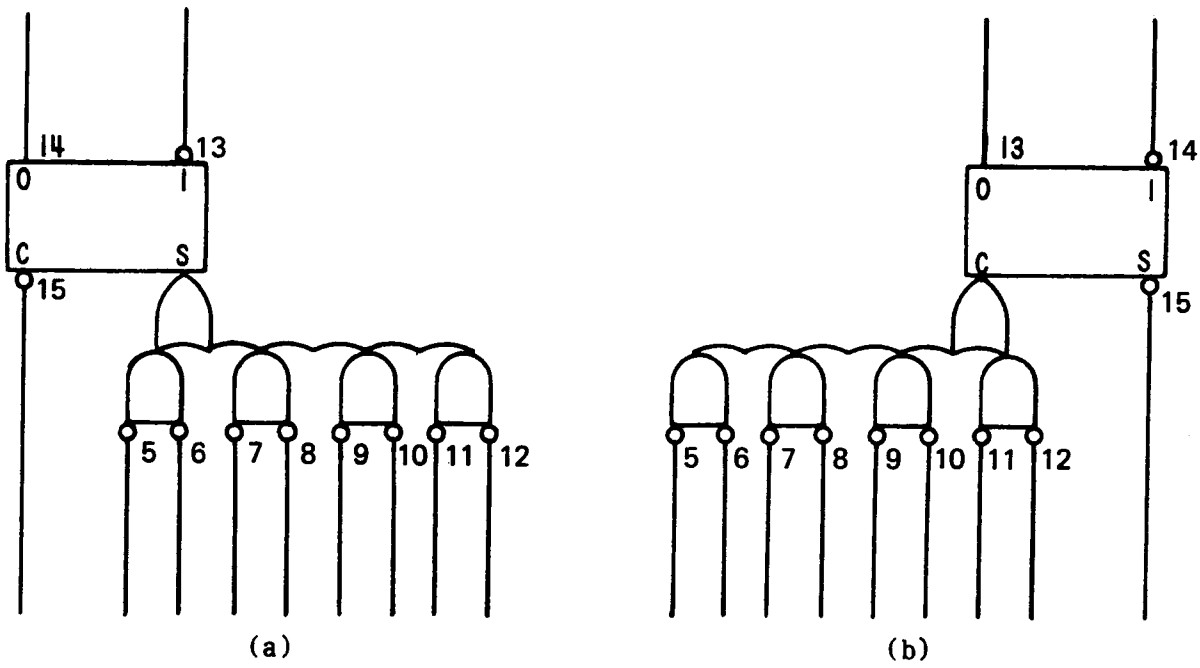
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-15.0 Volts	LOW	-15.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	-	-15.0	-
mW	-	-	200	-

Figure 7-15. Pulse-Delay Oscillator, Card Type 7000210



LOGIC SYMBOLS

LOGIC DESCRIPTION

A low input signal to pin 15, drawing (a), will clear the flip-flop with a resultant low signal at pin 14 and a high at pin 13.

When both inputs to any one AND circuit on the set side of the flip-flop are low, the flip-flop will be set to produce a low signal output at pin 13 and high at pin 14.

Drawing (b) shows a reversal of drawing (a) with a multiple clear function and a single set function.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.3 volt and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.1 milliamperes.

The circuit can drive one indicator driver plus either four AND/OR or AND gates.

The speed of the circuit is such that the second stage of two series-connected circuits will produce a usable output before the termination of a clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

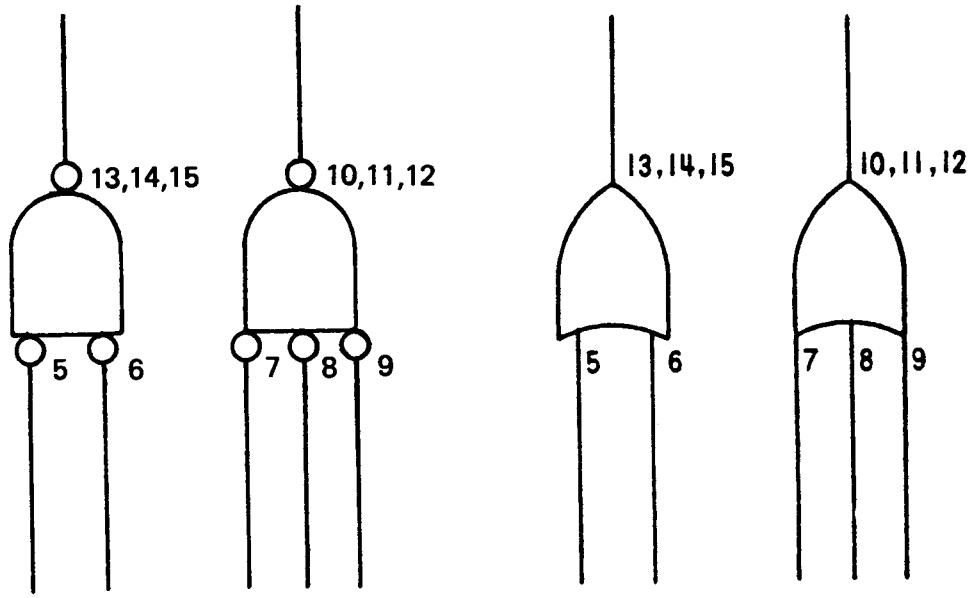
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	64	656	43

Figure 7-16. Flip-Flop, Card Type 7002000



LOGIC SYMBOLS

LOGIC DESCRIPTION

If the input signal to any one pin of a logic element is high, the output from that element will be high.

If all of the inputs to a logic element are low, the output from that element will be low.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes with 0.0 volts input.

This circuit is capable of driving six AND or AND/OR gates from each output pin for a total of 18 gates per logic element.

The speed of the circuit is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase input pulse to the first stage. The duration of a normal clock-phase pulse is 125 nanoseconds.

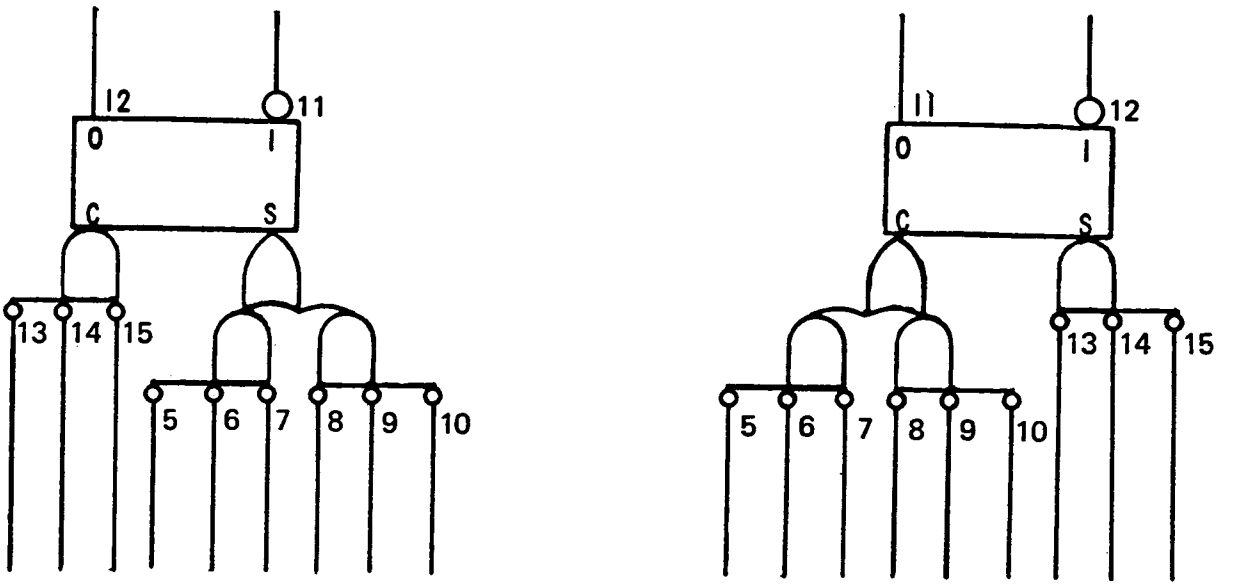
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	194	200	196

Figure 7-17. Driver Amplifier, Card Type 7002013



LOGIC SYMBOLS

LOGIC DESCRIPTION

This circuit may function in either of the two configurations shown above. In either case, all three inputs to any one AND gate must be low to perform the clear or set function.

The right side of the flip-flop is called the Set side, the left side is called the Clear side. When the flip-flop is cleared, the output from the Clear side is low. When the flip-flop is set, this output is high. The opposite is true for the Set side.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.1 milliamperes.

This logic element is capable of driving four AND gates and an indicator driver.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

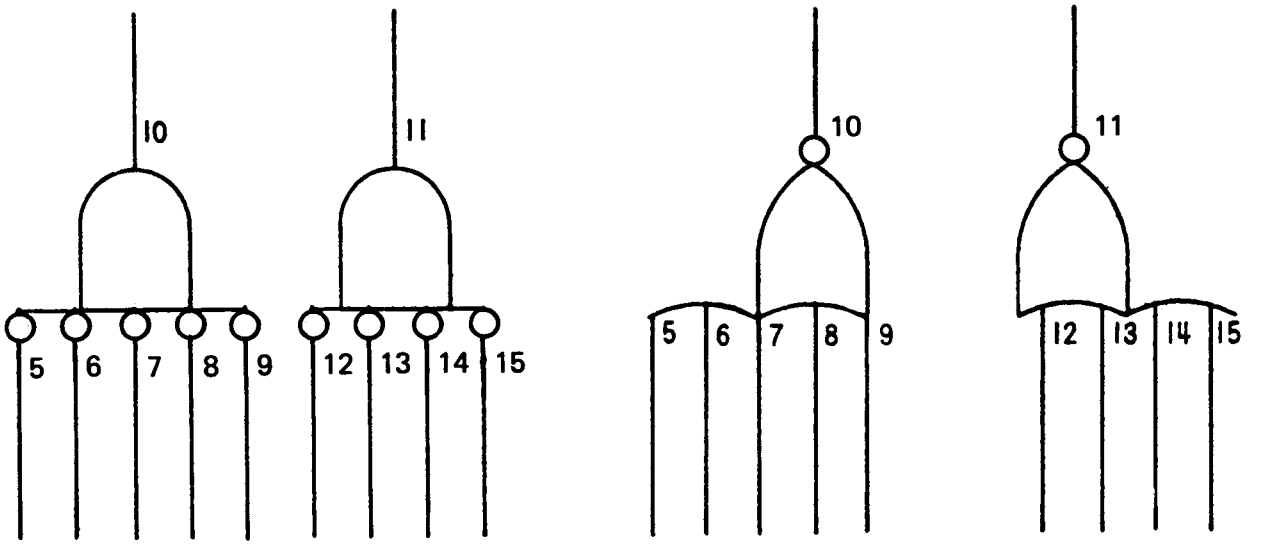
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	64	470	43

Figure 7-18. Flip-Flop, Card Type 7002020



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all used inputs to a circuit are low, the output from that circuit will be high. If any input to a circuit is high, the output will be low.

The module may be used either to AND low input signals or to OR high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. Output voltage levels are identical to input voltage levels.

This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

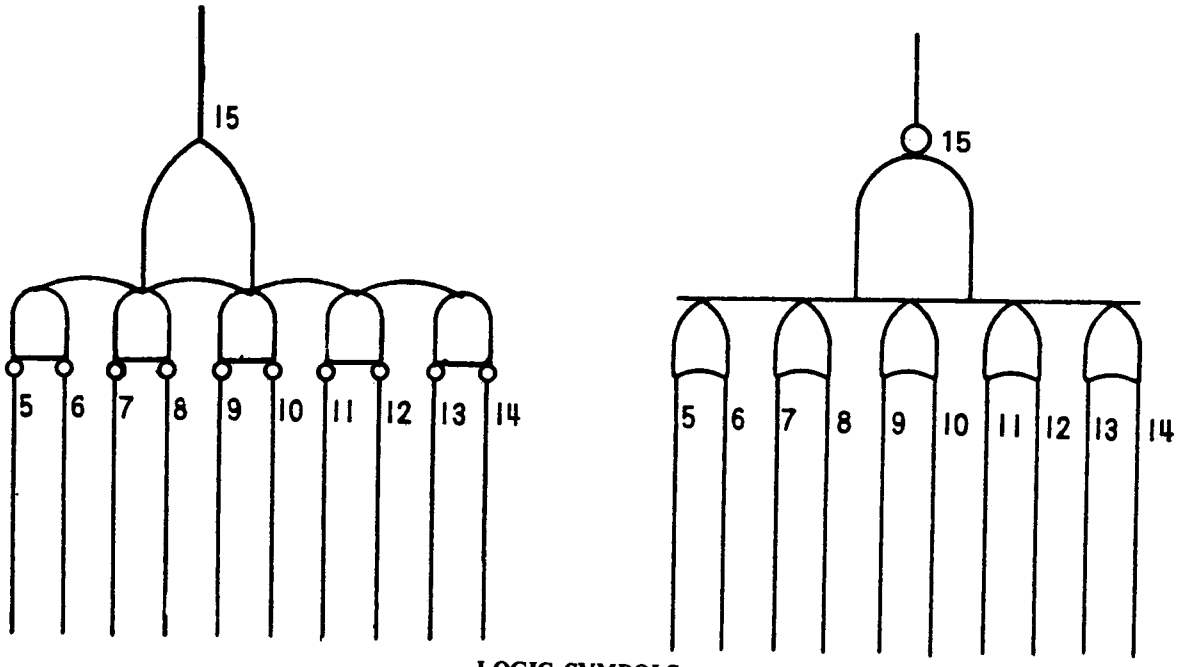
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	80	200	86

Figure 7-19. Inverter, Card Type 7002030



LOGIC SYMBOLS

LOGIC DESCRIPTION

When both inputs to any one AND circuit are low, the output of the module will be high. If at least one input to each OR circuit is high, the module output will be low.

The module may be used to either OR low input signals or to AND high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

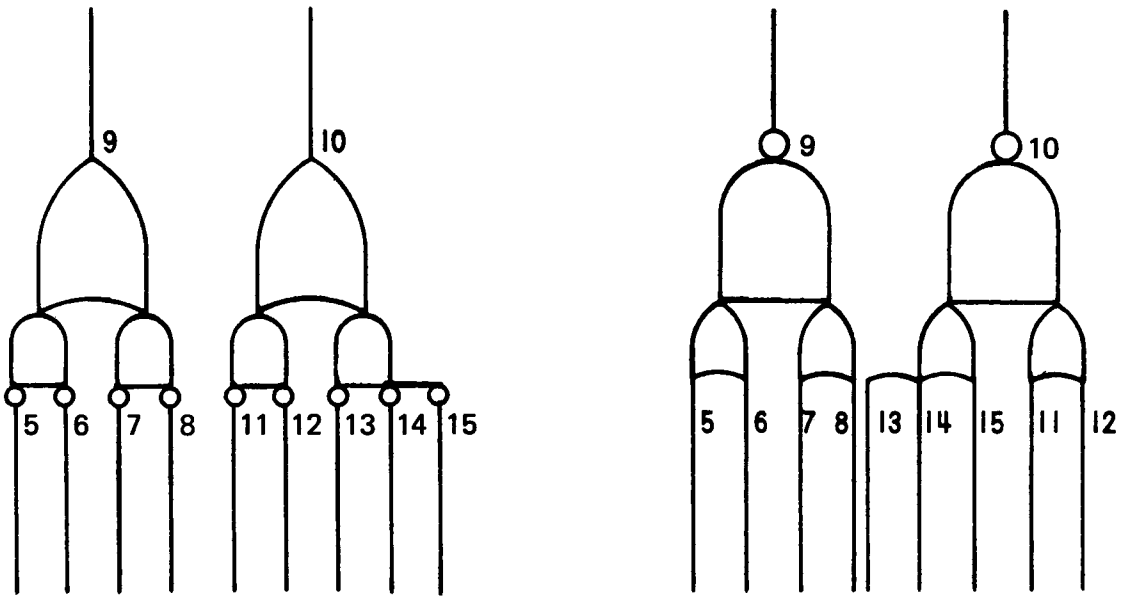
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	33	430	43

Figure 7-20. Inverter, Card Type 7002040



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all input signals to any one AND input circuit are low, the output from the logic element will be high. If at least one input to each AND input circuit is high, the logic element output signal will be low.

The module may be used to either AND low signal inputs or to OR high signal inputs.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

This logic element is capable of driving five AND/OR gates or six AND gates.

The maximum speed of this circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first circuit. The duration of the normal clock-phase pulse is 125 nanoseconds.

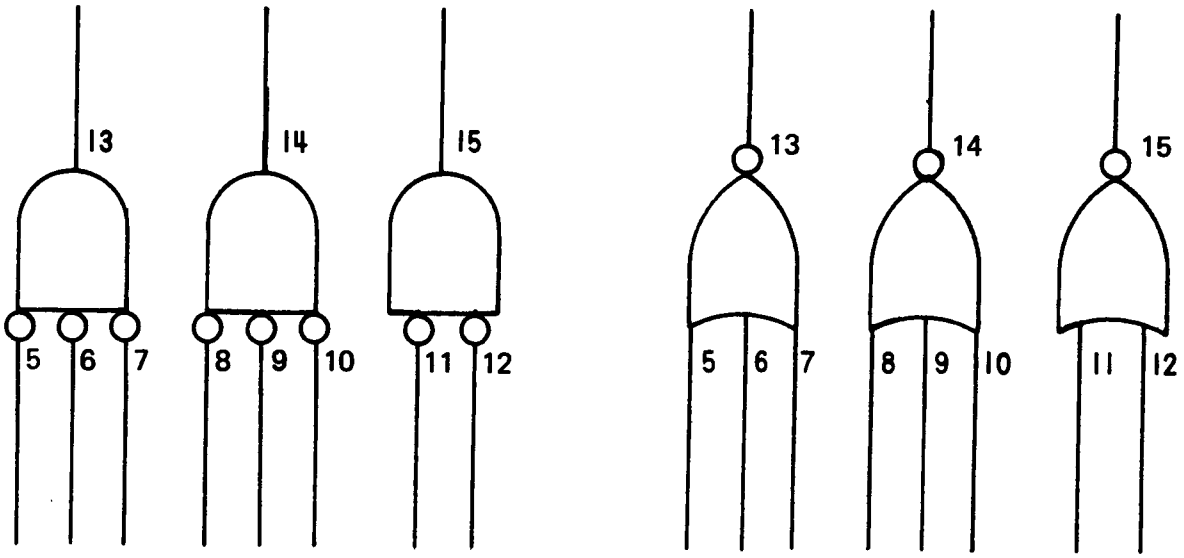
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	66	375	86

Figure 7-21. Inverter. Card Type 7002050



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to a logic element are low, the output from that element will be high. When any input to an element is high, the output from that element will be low.

The module may be used to either AND low input signals or to OR high input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes with 0.0 volts input.

The elements are capable of driving five AND/OR gates or six AND gates.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

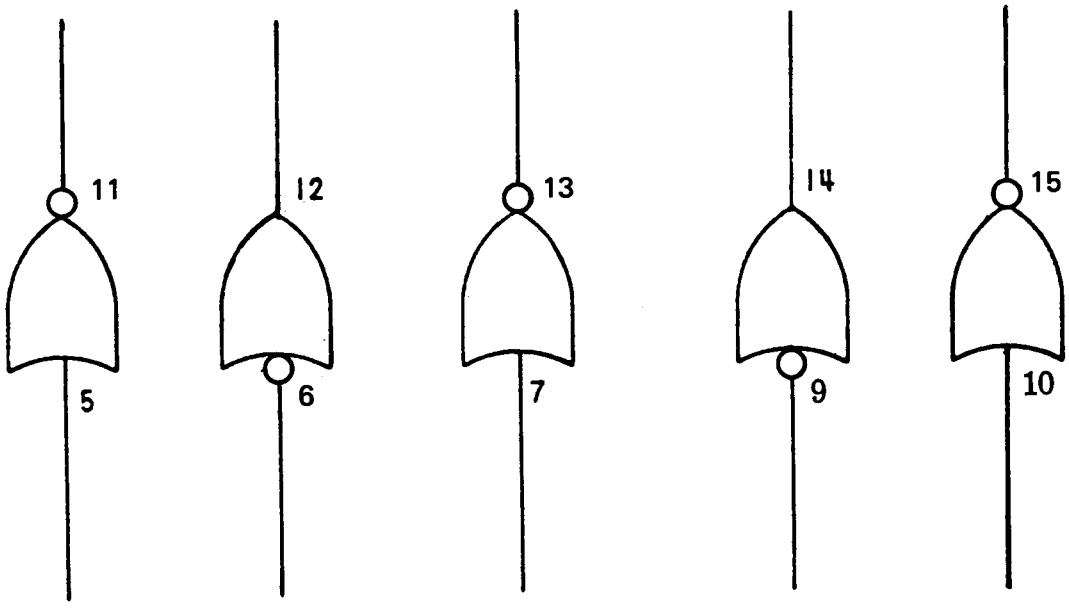
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	120	300	129

Figure 7-22. Inverter, Card Type 7002060



LOGIC SYMBOLS

LOGIC DESCRIPTION

The logic elements on this module are used to invert the input signal. If the input signal to any element is a low, the output of that element will be a high. Conversely, if the input to an element is a high, the output of that element will be a low.

Either of the two logic symbols shown above may be used to represent the logic elements and may be used interchangeably.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes with 0.0 volts input.

The elements can drive five AND/OR gates or six AND gates.

The speed of the circuit is such that the second of two series-connected circuits will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

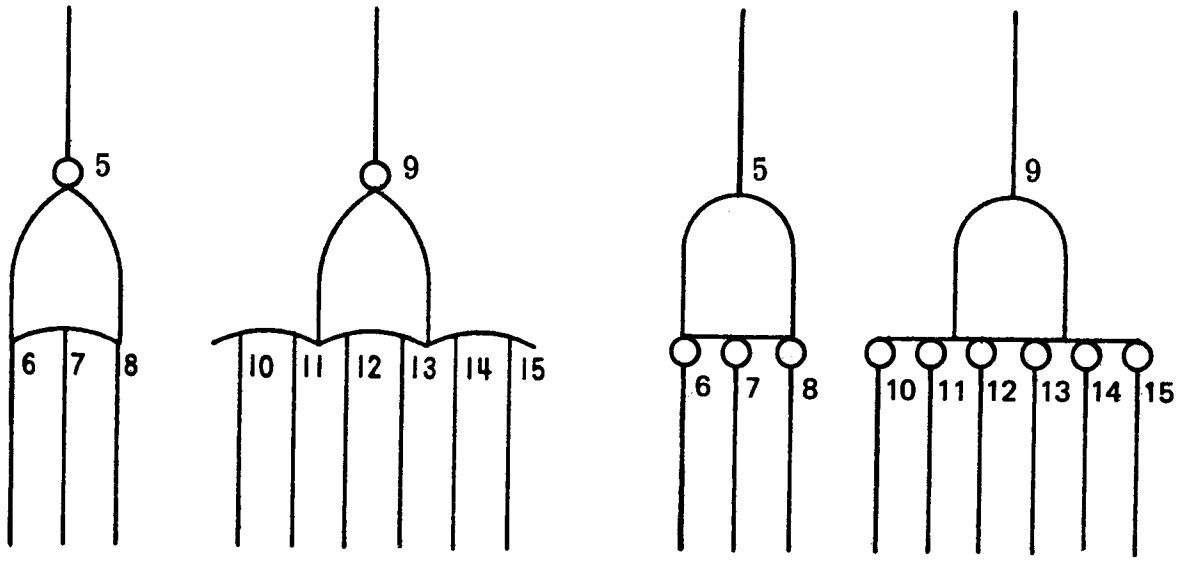
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	200	500	215

Figure 7-23. Inverter, Card Type 7002070



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one element are low, the output from that element is high.

When any one input to an element is high, the output from that element is low.

The elements on this module are used to either AND low input signals or to OR high input signals.

One element on this module has three usable input pins, the other has six.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milliamperes.

Each element can drive five AND/OR circuits or six AND circuits.

The maximum speed of each element is such that the second of two series-connected stages will produce a usable output before the termination of the clock-phase input signal to the first stage. The duration of the normal clock-phase signal is 125 nanoseconds.

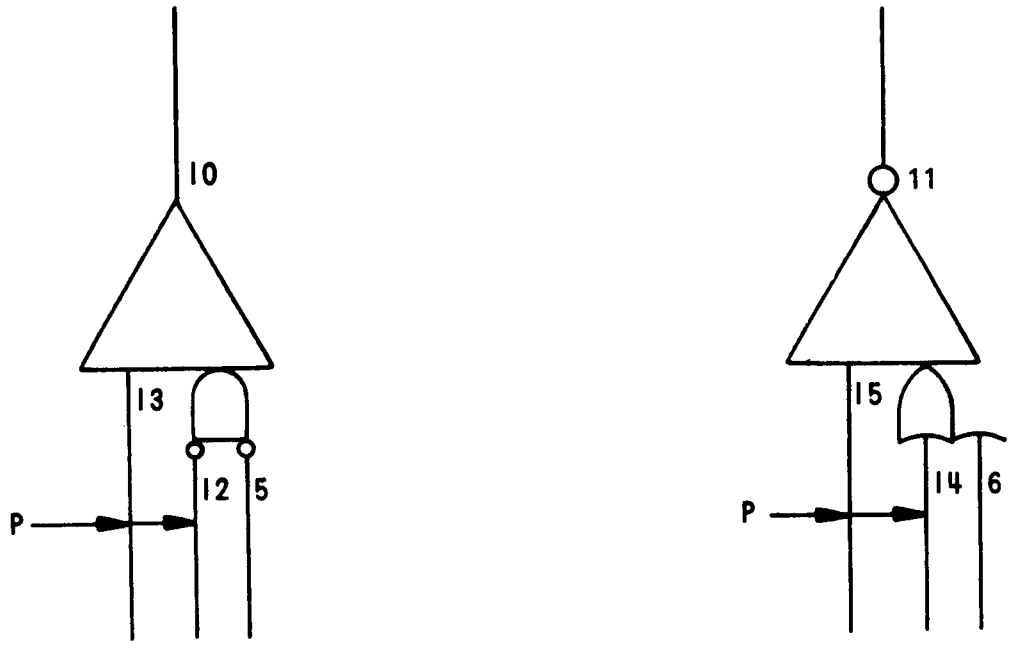
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	80	200	86

Figure 7-24. Inverter, Card Type 7002080



LOGIC SYMBOLS

LOGIC DESCRIPTION

This module provides a gated input of signals from peripheral devices working in conjunction with the computer.

If the input to pin 5 is high, the output at pin 10 will be low.

If the input to pin 5 is low and the input to pin 12 is 0.0 volts, the output will be low.

If the input to pin 5 is low and the input to pin 12 is -15.0 volts, the output will be 0.0 volts.

Pins 13 and 15 are the ground return for the twisted pair.

ELECTRICAL DESCRIPTION

Input signals must have positive voltage excursions to a level between 0.0 and 0.5 volts and negative voltage excursions between -13.5 and -16.5 volts. Input signals are applied to either pin 12 or 14.

The gating signals applied to either pin 5 or 6 have positive excursions to a level between 0.0 and -0.5 volts, and negative voltage excursions to a level between -3.6 and -5.4 volts.

Output voltage excursions are the same as those given for the gating signals.

The maximum input current required is 3.7 milliamperes.

The elements on this module are capable of driving two AND/OR gates or two AND gates.

The circuit delay is between 1.0 and 2.2 microseconds.

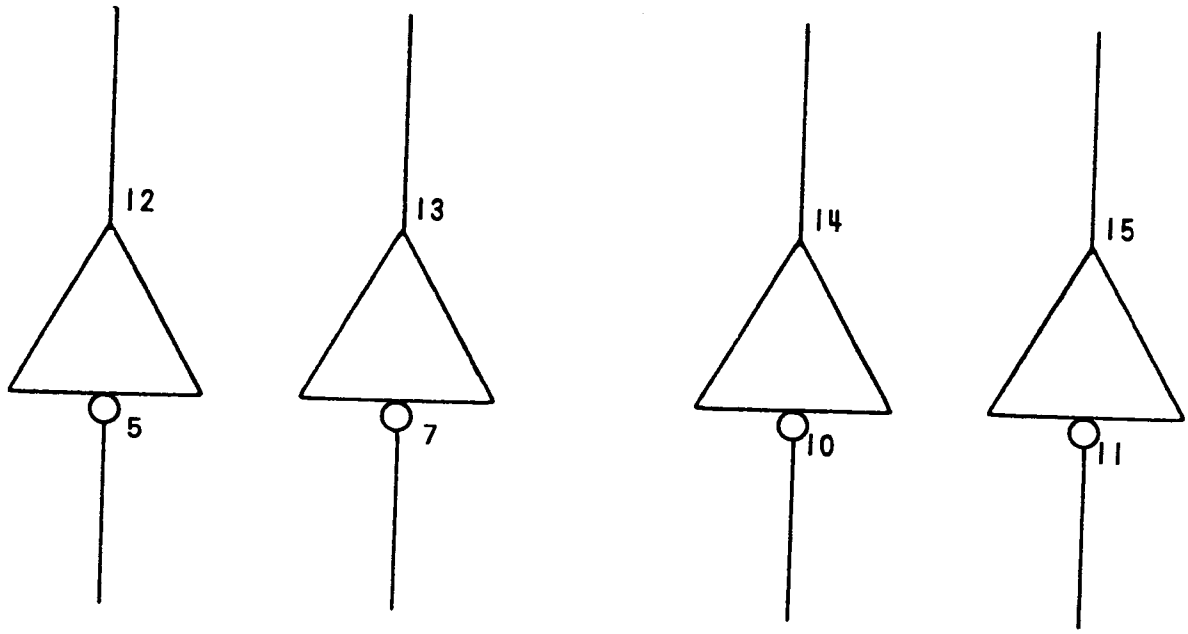
LOGIC

INPUT		OUTPUT	
LOW	-15.0 Volts	HIGH	0.0 Volts
HIGH	0.0 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	24	96	126

Figure 7-25. Input Amplifier-Inverter, Card Type 7002090



LOGIC SYMBOLS

LOGIC DESCRIPTION

Each element on this module is used to supply the current to light an incandescent indicator.

When the input to an element is low, current will be supplied to light the indicator.

When the input to the element is high, no current is supplied to light the indicator.

ELECTRICAL DESCRIPTION

Input signals to these elements mush have positive voltage excursions between 0.0 and -0.5 volts and negative voltage excursions between -3.6 and 5.4 volts.

Output voltage excursions are to a level between -13.5 and 15.0 volts.

The output load for this circuit is an incandescent lamp and a limiting resistor which limits the output current to a maximum of 50 milliamperes.

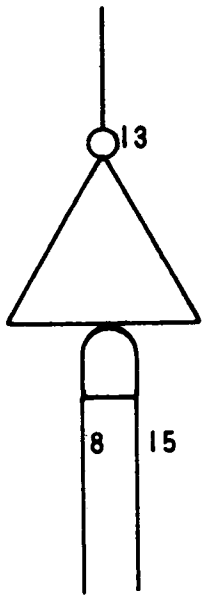
LOGIC

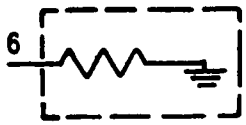
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-15.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	120	-	300

Figure 7-26. Driver Amplifier Card Type 7002100





LOGIC SYMBOL

LOGIC DESCRIPTION

If either a low is present on pin 15 or pin 15 is disconnected, the output from the module will be high.

If pin 15 is high, the output from the module will be the complement of the input to pin 8.

Pin 6 is connected to a resistor which is normally used to terminate delay line circuits.

This module is normally used in the clock circuits.

ELECTRICAL DESCRIPTION

Input pulses to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.65 milliamperes.

The maximum circuit delay is 40 nanoseconds.

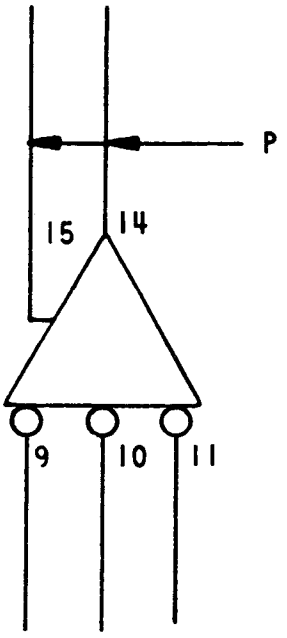
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	80	125	325

Figure 7-27. Driver Amplifier, Card Type 7002120



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signals to pins 9, 10, and 11 are low, the output signal at pin 14 will be 0.0 volts.

If any one input signal is high, the output at pin 14 will be -13.5 volts.

Pin 15 is used to provide the ground return for the twisted-pair conductors.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive and negative voltages of 0.0 volts and -4.5 volts, respectively.

Output signals from this circuit have nominal positive and negative static voltages of 0.0 volts and -13.5 volts, respectively.

The maximum input current required is 2.0 milliamperes.

The rise and fall times of this module are controlled to provide a maximum change of 5.0 volts per microsecond.

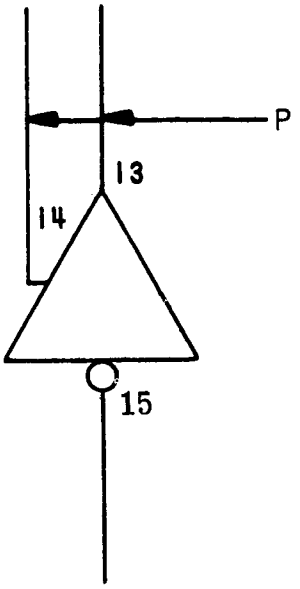
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	LOW	-13.5 Volts
LOW	-4.5 Volts	HIGH	0.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	15	630	-

Figure 7-28. Driver Amplifier, Card Type 7002130



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signal is low, the output between pins 13 and 14 is 0.0 volts. When the input signal is high, the output is -13.5 volts.

Pin 14 is the ground return for the twisted-pair conductors.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

Output signals from this circuit have nominal positive and negative static voltage excursions of 0.0 and -13.5 volts, respectively.

The maximum input current required is 2.25 milliamperes.

The output is capable of driving four twisted-pair conductors for a maximum length of 300 feet.

The rise and fall times of this module are controlled to provide a maximum change of 5.0 volts per microsecond.

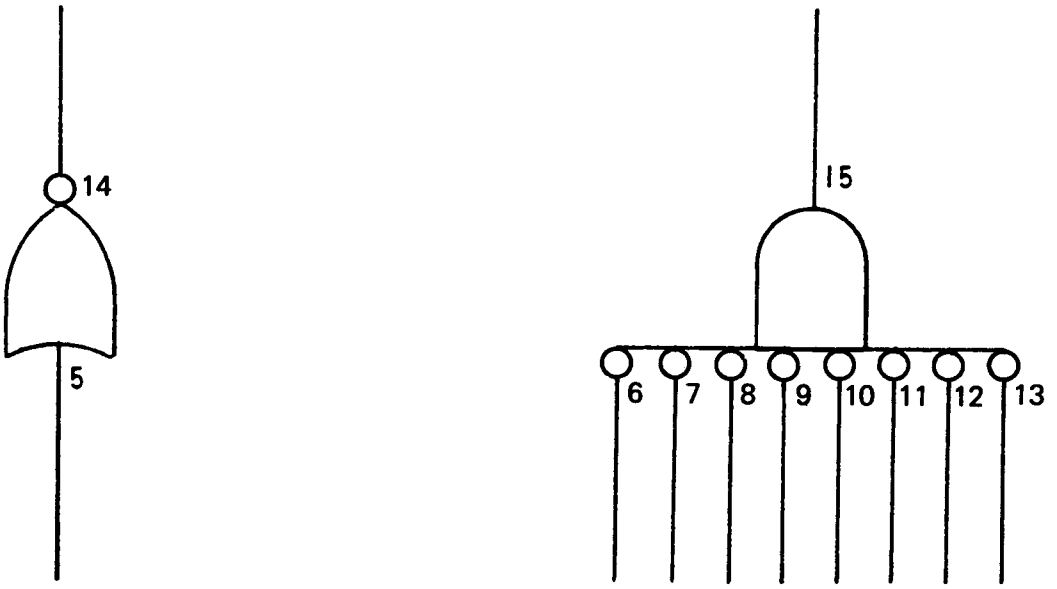
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	-13.5 Volts
LOW	-4.5 Volts	LOW	0.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	15	450	-

Figure 7-29. Driver Amplifier, Card Type 7002140



LOGIC SYMBOL

LOGIC DESCRIPTION

Any one high-signal input to the AND gate will produce a low signal as an output. When all used inputs are low, the output will be high.

This module may also be used in the OR configuration. In this case, the OR symbol is used and the input of any high will cause a low output.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive and negative voltage excursions of 0.0 volts and -4.5 volts, respectively. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 5.8 milli-amperes.

The speed of this module is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase pulse applied to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

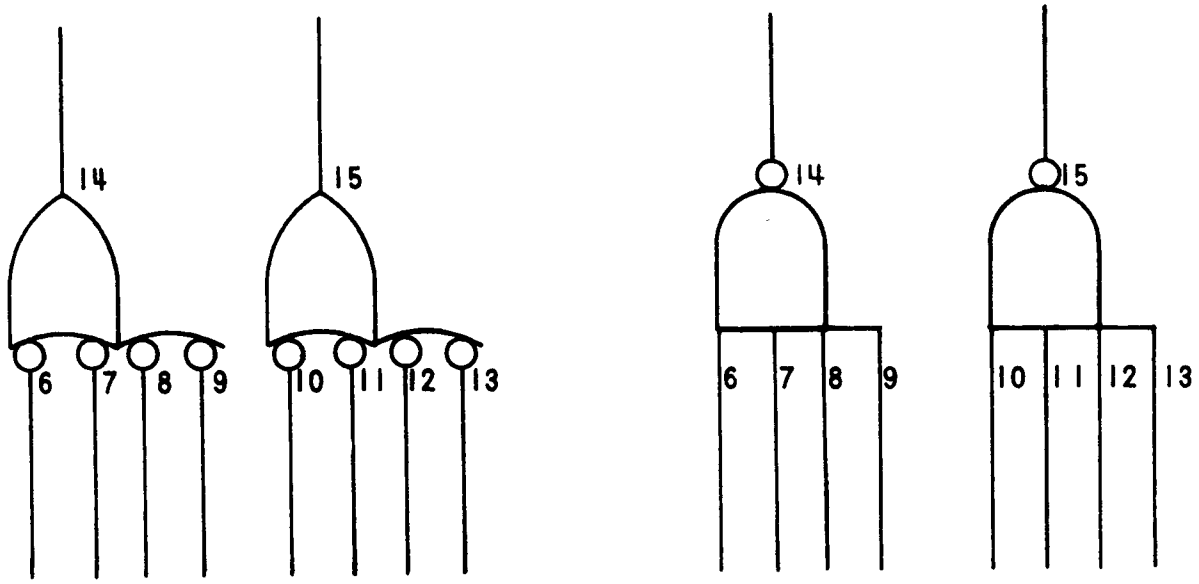
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW		80	200	86

Figure 7-30. Inverter, Card Type 7002160



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one element are high, the output from that element will be low.

If any one input to an element is low, the output from that element will be high.

The circuit is considered to AND highs or to OR lows.

ELECTRICAL DESCRIPTION

Input signals to the elements must have nominal positive excursions between 0.0 and -0.3 volts and nominal negative excursions between -3.6 and -5.4 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.0 milliamperes.

Each element is capable of driving six AND gates or five AND/OR gates.

The speed of each element is such that the second of two series-connected stages will produce a usable output before the termination of a clock-phase input signal to the first stage. The duration of the normal clock-phase pulse is 125 nanoseconds.

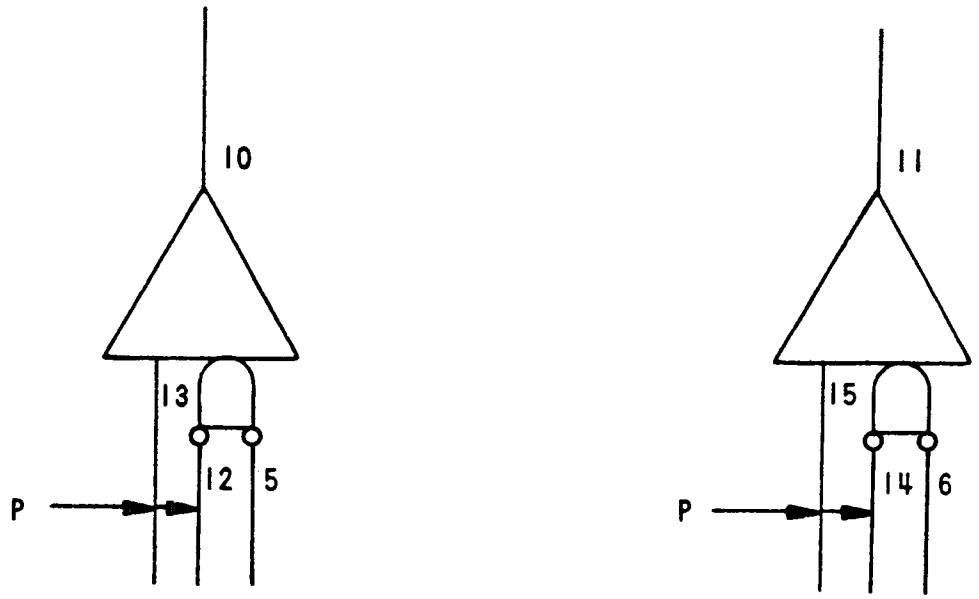
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	66	680	86

Figure 7-31. Inverter, Card Type 7002220



LOGIC SYMBOLS

LOGIC DESCRIPTION

To produce a high output from pin 10, the input to both pin 12 and 5 must be low. Pin 13 is the ground return for the twisted-pair input.

If either pin 12 or pin 5 are high, the output from pin 10 will be low.

The circuit has a high common-noise rejection when used with the twisted-pair input. The input impedance is balanced so that noise coupled into one conductor is also coupled into the other conductor and balanced out.

ELECTRICAL DESCRIPTION

Input signals to pin 12 must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -3.3 volts. Input voltages to the gate, pin 5, must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -4.5 volts.

Output voltage levels are the same as those listed for the gate voltage levels.

The maximum input current required is 1.3 milliamperes. The maximum current turn-on and turn-off time is 200 nanoseconds.

This circuit is capable of driving two AND/OR gates or two AND gates.

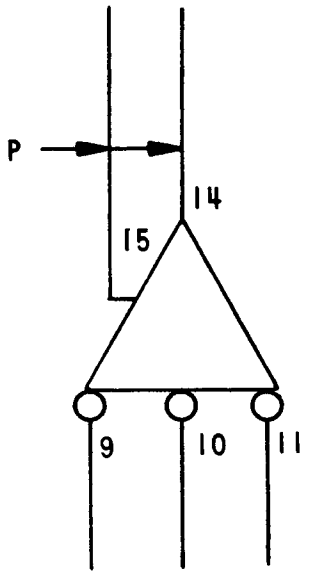
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-3.0 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	180	255	40

Figure 7-32. Differential Amplifier, Card Type 7002321



LOGIC SYMBOL

LOGIC DESCRIPTION

To produce a high output, all inputs must receive a low signal. If any one input has a high applied, the resulting output will be low.

Pin 15 is used as the ground return for the output twisted pair.

The circuit contains high impedance features. With power off and a negative voltage applied from a remote source, the input impedance is not less than 0.1 megohm.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have positive static voltage excursions of between 0.0 and -0.5 volts and negative static voltage excursions of between -3.8 and -5.2 volts.

The output shall have positive static excursions of between 0.0 and -0.5 volts and negative static excursions of between -3.0 and -4.5 volts.

The maximum circuit delay and storage is 200 nanoseconds.

The maximum input current required is 4.6 milliamperes.

This module is capable of driving four input-amplifier modules of the 7002320 type through 150 feet of cable.

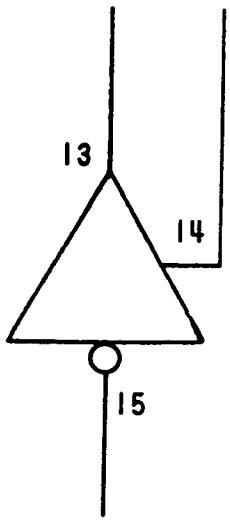
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	LOW	-3.0 Volts
LOW	-4.5 Volts	HIGH	0.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	130	500	80

Figure 7-33. Control Line Amplifier, Card Type 7002331



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input signal to pin 15 is a low, the output at pin 13 is high. When the input is high, the output is low. Pin 14 is the ground connection for the twisted-pair output line.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of -0.3 volts and nominal negative voltage excursions of -4.5 volts

Output signals from this circuit will have nominal positive voltage excursions of -0.3 volts and a nominal static negative voltage excursion between -3.0 and -4.5 volts.

The maximum circuit delay and storage is 200 nanoseconds.

Maximum input current required is 4.6 milliamperes.

This module is capable of driving four input-amplifier modules of the 7002320 type through 150 feet of cable.

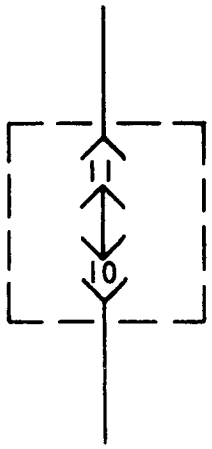
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	LOW	-3.0 Volts
LOW	-4.5 Volts	HIGH	0.0 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	108	561	40

Figure 7-34. Data Line Amplifier, Card Type 7002341

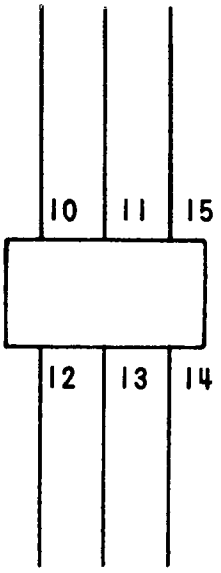


ELECTRICAL CONNECTIONS

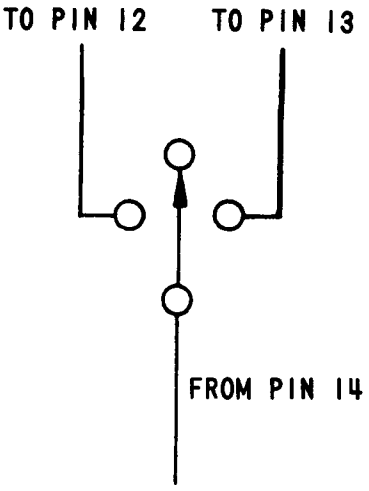
LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(Not Applicable)	This module consists of a series of jumper wires used primarily for the transition from fast to slow interface in in the input/output section of the computer.

				POWER REQUIREMENTS				
				PIN	1	2	3	4
				VOLTAGE	-	-	-	-
				mW	-	-	-	-

Figure 7-35. High-Speed Selector, Card Type 7002730



LOGIC SYMBOL



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

This module is used to provide a regulated voltage output for use by certain memory circuits.

Normal voltage output is a regulated -10 volts. Connecting pins 13 and 14 through the marginal check switch, as shown above, will provide an output at pin 15 of -11.0 volts. Connecting pins 12 and 14 will provide -9.0 volts.

The marginal check switch is used to determine the operating characteristics of the memory circuits under tolerable limit.

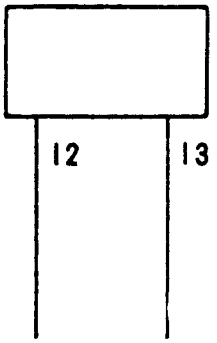
ELECTRICAL DESCRIPTION

The base of an externally-mounted, voltage-control transistor is connected to pin 11 of this module. The emitter of the transistor connects to pin 15. The collector of the transistor is connected to a -15.0 volt supply. The variable resistor is then adjusted to approximately -10.0 volts (clipping voltage) applied to the transistor. The resulting -10.0 volts are available as a regulated output at pin 15. This output voltage is adjustable between -5.0 and -12.0 volts.

The circuit is capable of supplying 500 milliamperes of current.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	N/A	HIGH	N/A	VOLTAGE	Gnd	-	-15.0	-
LOW	N/A	LOW	N/A	mW	-	-	750	-

Figure 7-36. Marginal Check Voltage Regulator, Card Type 7002861



LOGIC SYMBOL

LOGIC DESCRIPTION

For the logic description of this module, refer to the logic description of the 7003720 module (Figure B-36).

ELECTRICAL DESCRIPTION

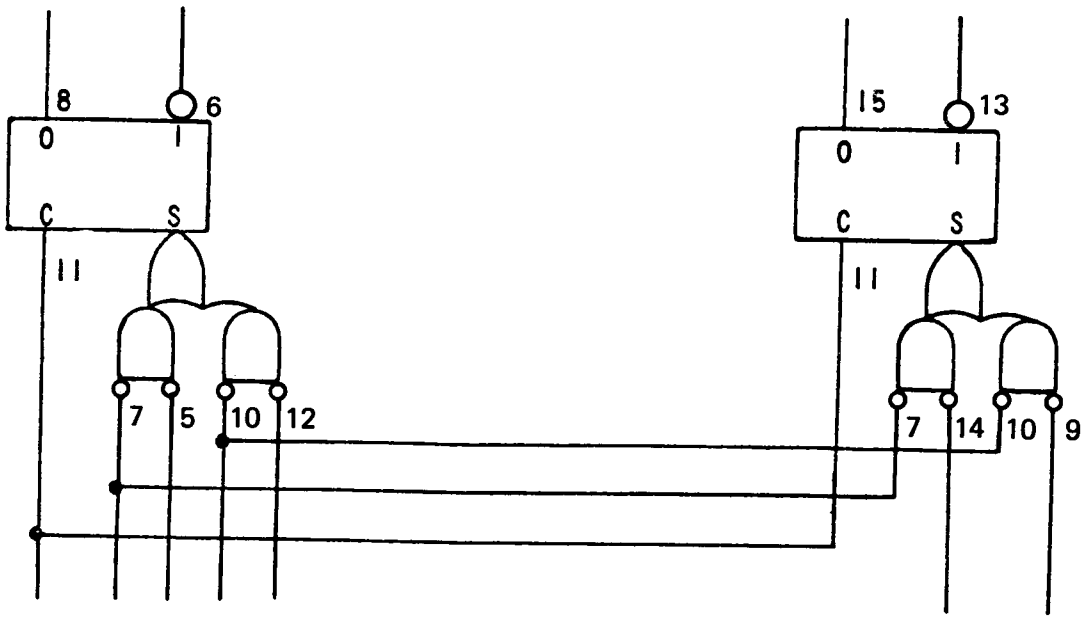
This module functions as a detection device to sense voltage failures and fluctuations greater than 10 percent in the positive and negative 15-volt supplies. The level of detection may be adjusted to any level between 12.5 and 13.5 volts.

This module is designed to be used in conjunction with the 7003720 module. Either pin 12 or 13 of this module is connected to pin 13, 14, or 15 of the 7003720 module for voltage protection.

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	175	500	40

Figure 7-37. +15 and -15 Voltage Regulator, Card Type 7002880



LOGIC SYMBOLS

LOGIC DESCRIPTION

When both input signals to either of the two input AND gates are low, the flip-flop is set, resulting in a high output at either pin 8 or 15 and a low output at either pin 6 or 13.

When the input signal to pin 11 is high, the flip-flop is cleared with a reversal in the output levels.

Each of the two AND gates for each flip-flop have two common inputs with a single unique input for each gate.

The clear input is common for both flip-flop circuits.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum current required at pins 5, 9, 12, and 14 is 6.85 milliamperes. The maximum current required at pins 7, 10, and 11 is 13.7 milliamperes.

Each output pin is capable of driving five AND circuits or four AND/OR circuits.

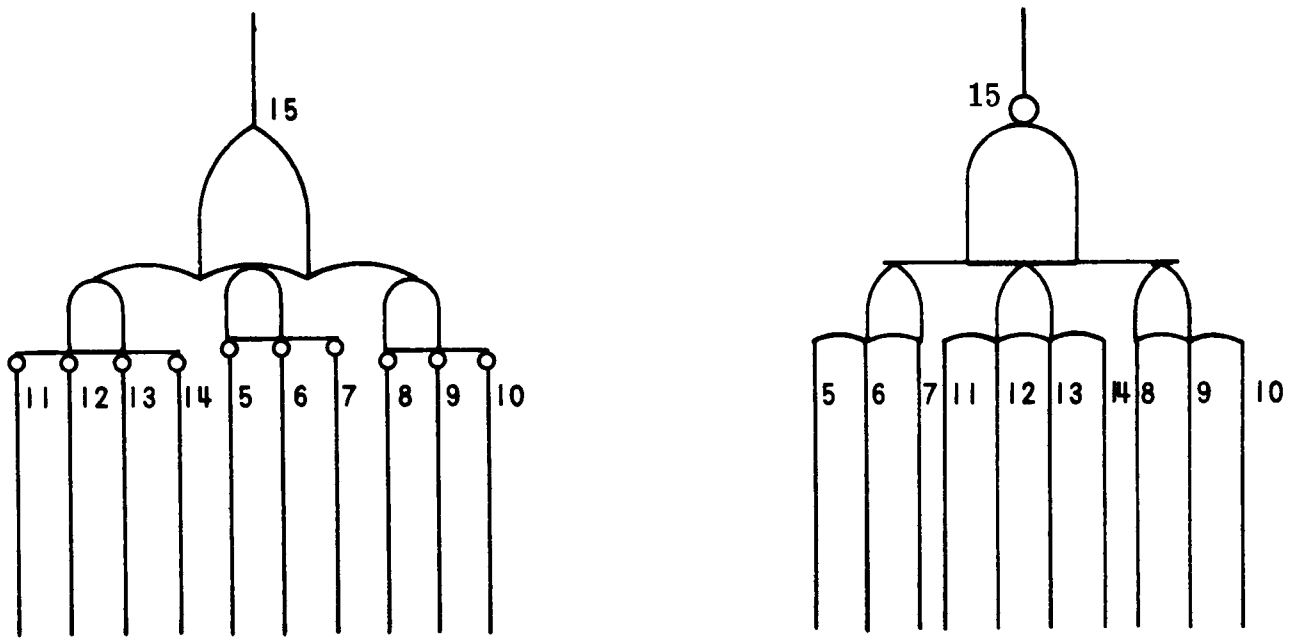
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	125	727	86

Figure 7-38. Flip-Flop, Card Type 7002900



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one AND circuit of an element are low, the output from that element will be high.

When at least one input to each OR circuit of an element is high, the output from that element will be low.

ELECTRICAL DESCRIPTION

Input signal to this circuit must have nominal positive excursions of -0.0 volts and nominal negative excursions of -4.5 volts.

The output voltage levels are identical to the input voltage levels.

The maximum input current required is 7.1 milli-amperes at 0.0 volts input.

The element is capable of driving five AND/OR gates or six AND gates.

The maximum turn-on time is 50 nanoseconds. The maximum turn-off time is 60 nanoseconds.

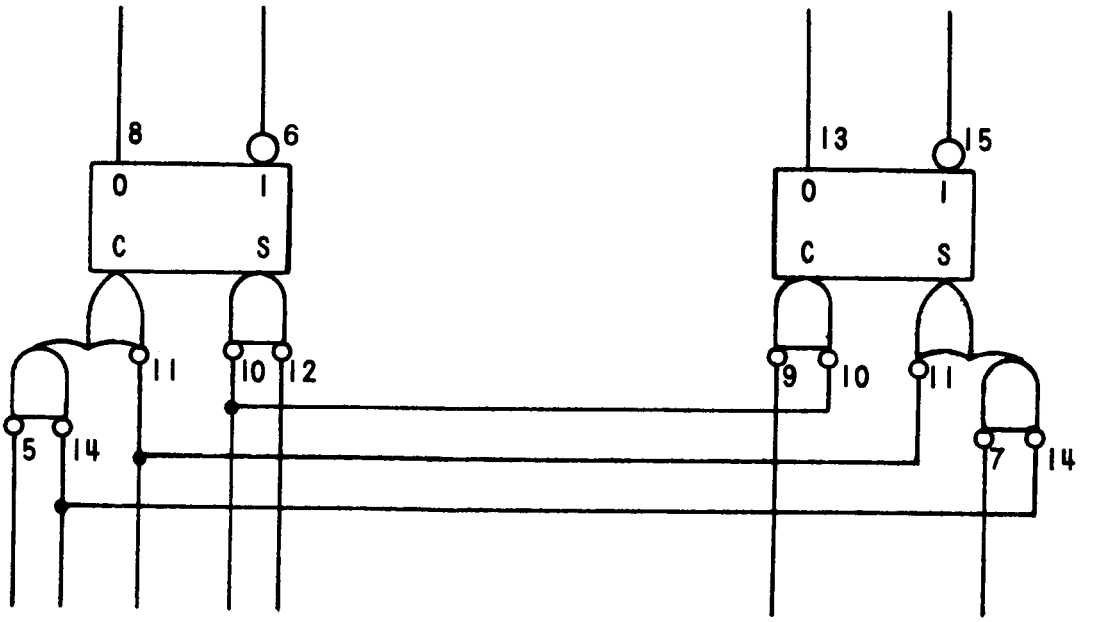
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5	LOW	-4.5

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	34.2	93.75	43.1

Figure 7-39. Inverter, Card Type 7002920



LOGIC SYMBOLS

LOGIC DESCRIPTION

A low to pin 11 will clear flip-flop (a) and set flip-flop (b). A low to pins 14 and 5 will also clear flip-flop (a) and low to pins 14 and 7 will also set flip-flop (b).

Each AND-gate input to the flip-flop requires two low signals to perform the logic function of clearing or setting.

When the flip-flop is set, the output from the "1" side will be high.

Either of the above configurations may be used to represent the logic function being performed by the flip-flop. Pins 10, 11, and 14 are common to both of the flip-flop circuits with pins 5, 7, 9, and 12 providing the unique input signals.

ELECTRICAL DESCRIPTION

Input signals to this circuit must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

The maximum input current required for a single input pin is 7.1 milliamperes. The current required for a common input pin is 14.2 milliamperes.

The maximum turn-on and turn-off time for each element is 50 and 60 nanoseconds, respectively.

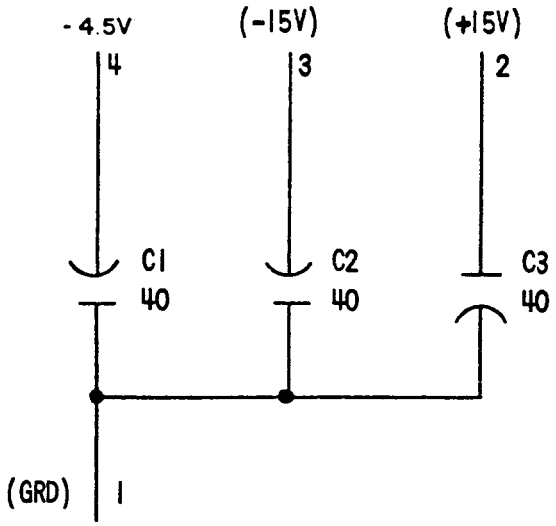
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	132	375	96

Figure 7-40. Flip-Flop, Card Type 7002930



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

(Not Applicable)

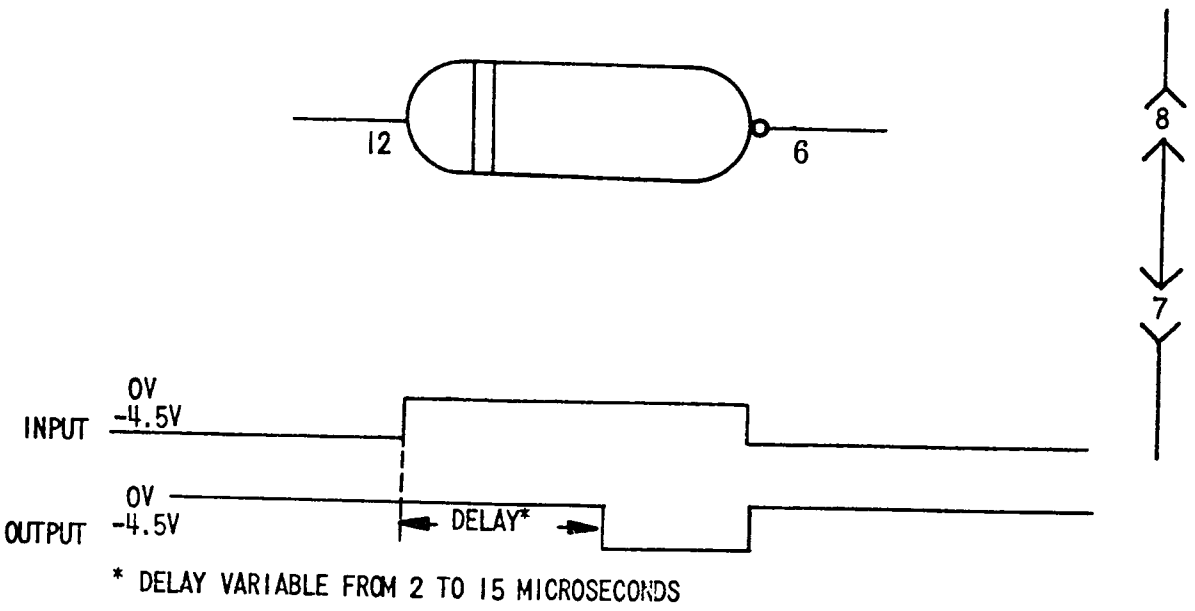
ELECTRICAL DESCRIPTION

The capacitors mounted on this module provide filter action for the voltages shown in parentheses. Chassis maps indicate the location of the cards in the computer.

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-41. Capacity Assembly - #3, Card Type 7003180



LOGIC SYMBOL

LOGIC DESCRIPTION

The transition from a logic low to a logic high at the input sets the delay. After a set interval, the output changes to a logic low. The output pulse terminates when the input pulse returns to the logic low level.

Pins 7 and 8 supply a jumper network for external circuitry.

ELECTRICAL DESCRIPTION

The time delay operates with input and output pulses that have nominal positive excursions of -0.3 volts and nominal negative excursions of -4.5 volts.

The maximum input current is 5.8 milliamperes at 0.0 volts.

The output can drive three AND or AND/OR circuits.

A variable resistor (R7) is adjusted to provide the required delay.

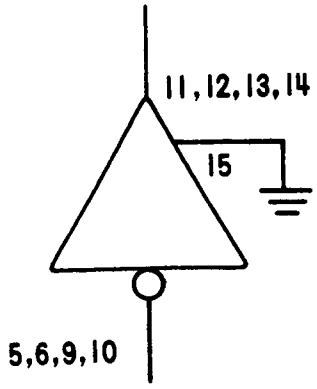
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-42. Time Delay - 2 to 15 usec, Card Type 7003480



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low at the input, the output will be high. With a high at the input, the output will reflect an open circuit.

ELECTRICAL DESCRIPTION

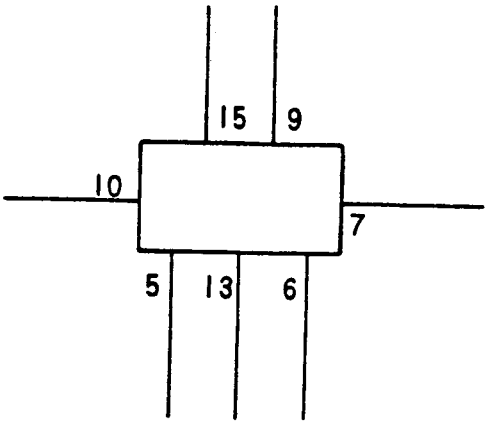
This card contains four identical circuits each of which acts as a switch in the ground lead of a panel lamp. Pin 15 is common to all four output transistors and is grounded.

When a -4.5 volts is applied to any of the four driver inputs, the respective output transistor will conduct, allowing a potential of -15 volts to be applied to the respective panel lamp, illuminating it. When the inputs have a ground applied to them, the respective output transistor will not conduct, thereby opening the circuit to the lamp.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	N/A

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Gnd	15.0	N/A	-4.5
mW	-	-	-	-

Figure 7-43. Driver Amplifier, Card Type 7003490



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

(Not Applicable)

ELECTRICAL DESCRIPTION

Pins 6 and 7 are connected to an externally mounted sensistor located in a core stack, which senses and compensates for temperature variations from 0°C (32°F) to 50°C (122°F). Pin 9 is connected to a variable resistor which is part of a voltage-divider network. It is normally adjusted for a steady state current of 4 amperes and will adjust for load changes from 1/3 to 6 amperes.

The sensing of temperature and/or load variations affects a change in the forward biasing of the input transistor and results in maintaining an output of -10 volts to within 1 percent.

The circuit is capable of steady state current of 4 amperes, and 7 amperes under pulsed conditions for periods up to 4 usec. Recovery time from full load to no load is approximately 40 usec.

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-
mW	-	-	-	-

Figure 7-44. Regulator Amplifier (-10 volt), Card Type 7003600

LOGIC SYMBOLS

LOGIC DESCRIPTION

The elements on this module are used to drive the memory currents during read and write operations involving the core memories.

To produce a low signal output, all inputs must be low. If any one input to an element is high, the output from that element will be high.

ELECTRICAL DESCRIPTION

Input signals to this module must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

Output signals from this module have nominal positive excursions of 0.0 volts and nominal negative voltage excursions of -7.5 volts for use in reading and writing operations in the core memory.

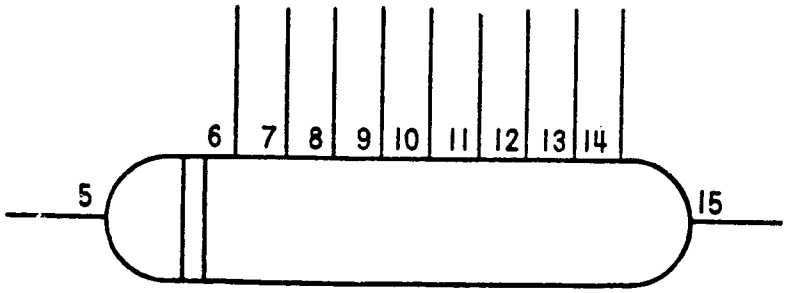
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-7.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-45. -7.5 Volt Memory Driver, Card Type 7003621



LOGIC SYMBOL

LOGIC DESCRIPTION

This module provides a delay for input signals, either high or low, for a minimum of 5 nanoseconds and a maximum of 50 nanoseconds in increments of 5 nanoseconds. The minimum delay is available at pin 6 and each successive pin provides an additional 5-nanosecond delay.

ELECTRICAL DESCRIPTION

This module, composed of coils and capacitors, operates in conjunction with the 7003640 module to produce timing and clock pulses for use throughout the computer logic.

A 200-Ohm resistor is required to terminate the output of this module. This resistor is normally provided by the 7002120 module.

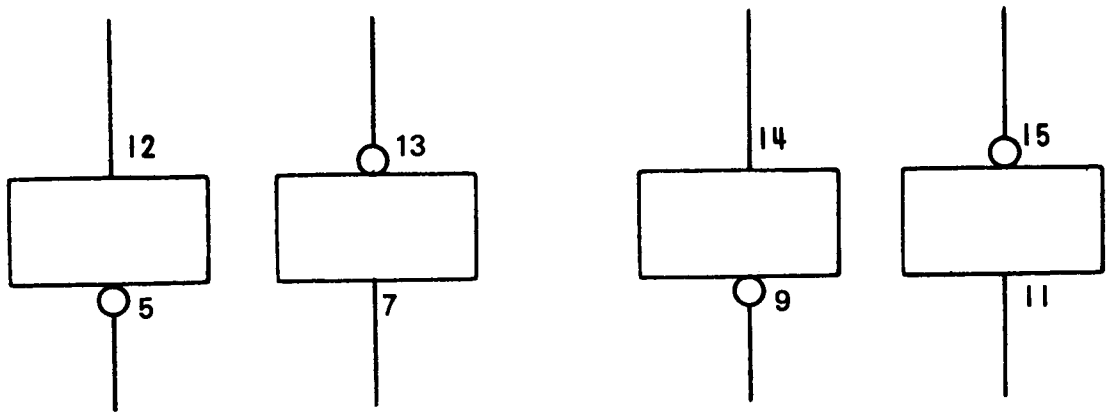
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	-	-	-	-
mW	-	-	-	-

Figure 7-46. Pulse-Delay Network, Card Type 7003630



LOGIC SYMBOLS

LOGIC DESCRIPTION

The logic elements on this module are used in conjunction with the 7003630 module to produce clock pulses for use throughout the computer for timing purposes.

Input pulses to each element are inverted through the element. The output from each element is capable of driving five AND/OR circuits or six AND circuits.

ELECTRICAL DESCRIPTION

Input signals to this module must have nominal positive voltage excursions of 0.0 volts and nominal negative voltage excursions of -4.5 volts. The output voltage levels are identical to the input voltage levels.

When used with the delay line module, the high-impedance input circuit of this module provides a minimum load to the delay line circuit to prevent reflected signals.

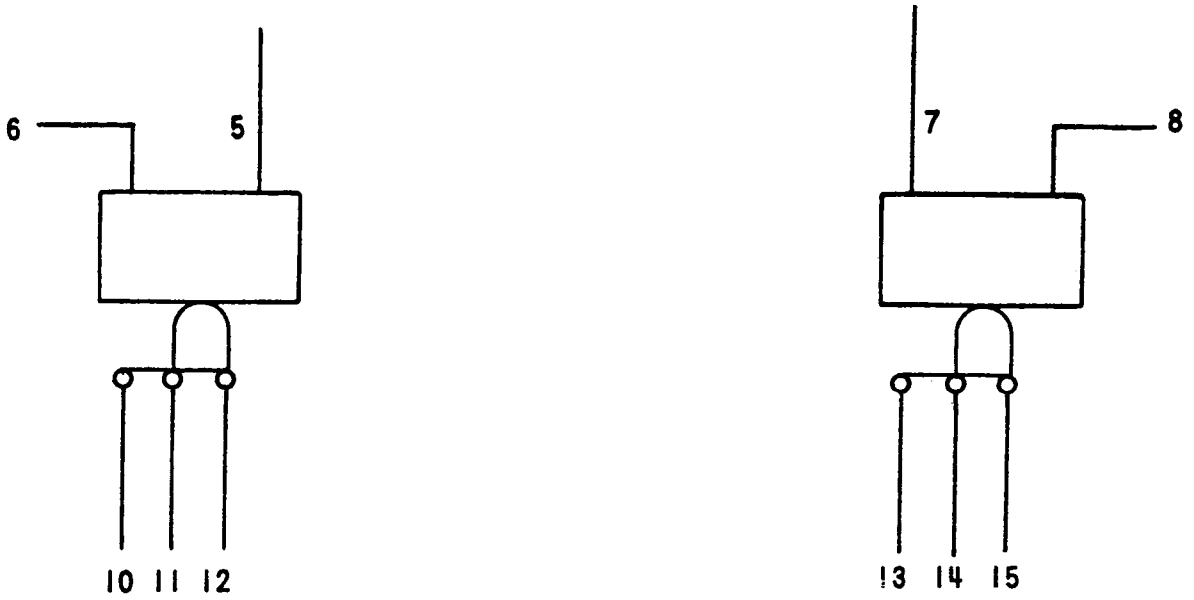
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-47. Emitter-Follower Driver, Card Type 7003640



LOGIC SYMBOL

LOGIC DESCRIPTION

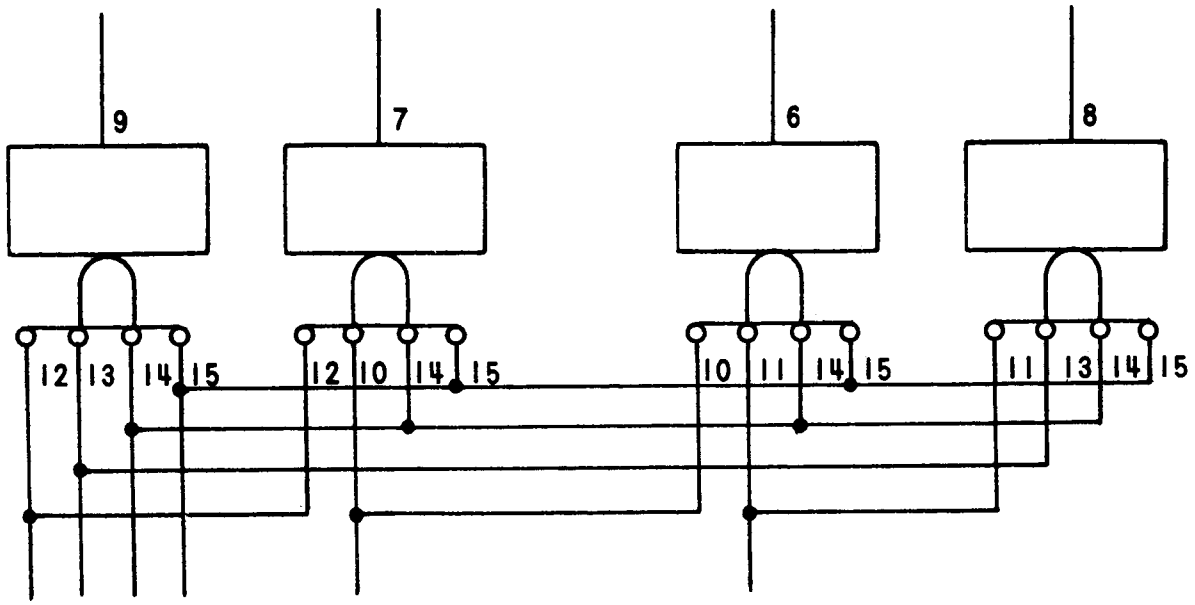
When all inputs to the AND gate are low, the output is high. When at least one input is high, the output will be a low.

ELECTRICAL DESCRIPTION

Pins 5 and 6 (7 and 8) are shorted together internally.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volts	HIGH	0.0 Volts	VOLTAGE	Gnd	+15.0	-15.0	-4.5
LOW	-4.5 Volts	LOW	-15.0 Volts	mW	-	-	-	-

Figure 7-48. Driver Amplifier, Card Type 7003670



LOGIC SYMBOL

LOGIC DESCRIPTION

Each of the elements on this module will produce a high-signal output when all inputs to that element have a low-signal input. Any one high input to an element will result in a low output from that element.

ELECTRICAL DESCRIPTION

Several common inputs to the elements on the module provide common gating of the output.

Input signals must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively. Output voltage levels are identical to the input voltage levels.

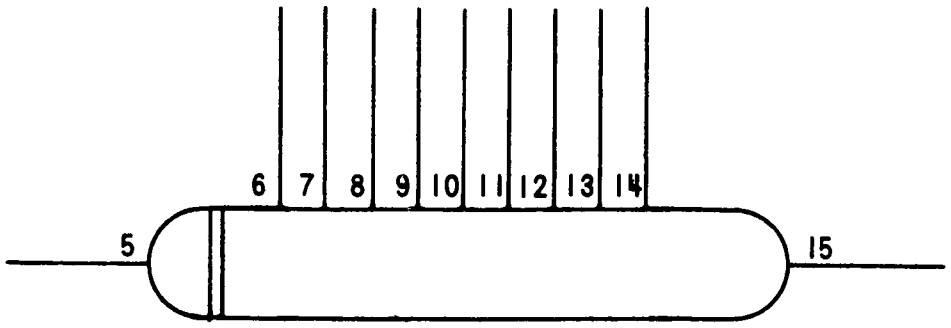
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	**HIGH**	0.0 Volts
LOW	-4.5 Volts	**LOW**	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-49. Transformer Driver, Card Type 7003680



LOGIC SYMBOL

LOGIC DESCRIPTION

This module provides a minimum delay of 20 nanoseconds and a maximum of 200 nanoseconds to an input pulse of either high or low signal characteristics.

. A minimum delay of 20 nanoseconds is provided at pin 6; a maximum delay of 200 nanoseconds is provided at pin 15. Additional delays are provided at taps in increments of 20 nanoseconds.

ELECTRICAL DESCRIPTION

This module, composed of coils and capacitors, operates in conjunction with the 7003640 module to produce timing pulses for the computer logic.

A 200-Ohm termination resistor is required and is normally supplied as a part of a 7002120 module through pin 6 of that module.

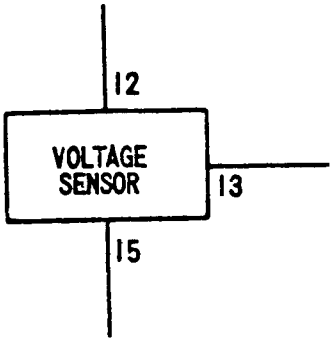
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	-	-	-
mW	-	-	-	-

Figure 7-50. Pulse-Delay Network, Card Type 7003710



LOGIC SYMBOL

LOGIC DESCRIPTION

This circuit is used in conjunction with assembly 7002880. Pin 12 of 7002880 is connected to pin 12 of this assembly. Pin 15 is connected in the reference voltage line to the memory regulator. One logic circuit is driven off pin 13. A fault in any one of the three voltages will cause the voltage at pin 13 to switch from -4.5 volts to 0.0 volts. This circuit detects the voltage levels high enough to properly operate the logic when the memory is shut down.

ELECTRICAL DESCRIPTION

This circuit is a detection device designed to sense voltage failures and tolerance decreases greater than 10 percent on the -4.5 volt supply. The level of detection may be adjusted by means of a potentiometer to any level between -3.2 volts and -4.0 volts. The circuit is designed to operate with 18 ±1.8 volts on pin 9 and is grounded through a 1K resistor on pin 8. This results in a voltage of -4.5 volts nominal on pins 13, 14, and 15 under normal operating conditions, and results in ground when the circuit detects a voltage failure.

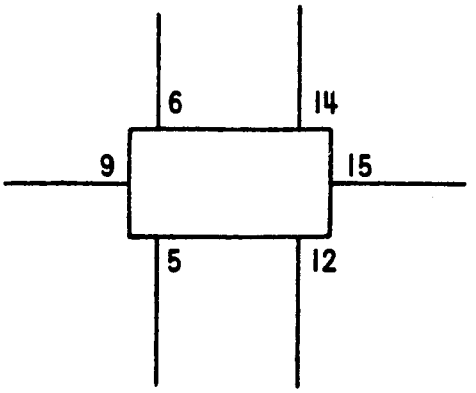
LOGIC

INPUT		OUTPUT	
HIGH	N/A	**HIGH**	N/A
LOW	N/A	**LOW**	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

 Figure 7-51. Voltage Sensor and Positive Switch, Card Type 7003720



LOGIC SYMBOL

LOGIC DESCRIPTION

An unregulated +15.0 volts is applied as a reference voltage to pins 5 and 6. This voltage, supplied through two transistors, is regulated through the use of a sensistor connected to pins 14 and 15.

Any change in temperature in the memory stack is detected and compensating voltages are developed through the transistors. The output voltage level is adjustable through a variable resistor connected between pins 5 and 12.

ELECTRICAL DESCRIPTION

The sensistor, mounted on a memory stack, controls the output voltage to give temperature compensation to the drive circuitry to ensure proper core operation through a 0°C (32°F) to 50°C (122°F) ambient temperature range.

The output voltage is regulated to within 1 percent when the input is within 10 percent. The regulator in the output stage is capable of supplying 7 amperes under pulsed conditions for periods up to 4 microseconds and steady state current of 4 amperes. The recovery time from full load to no load is about 40 microseconds.

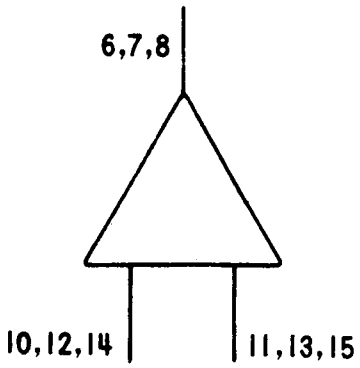
LOGIC

INPUT		OUTPUT	
HIGH	N/A	HIGH	N/A
LOW	N/A	LOW	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-
mW	-	-	-	-

Figure 7-52. Regulator Amplifier (+10 volt), Card Type 7003730



LOGIC SYMBOL

LOGIC DESCRIPTION

(Not Applicable)

ELECTRICAL DESCRIPTION

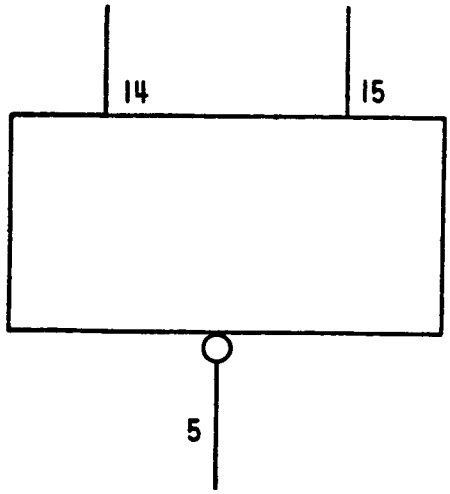
This card consists of three identical circuits. The input pins are connected to sense lines running through the cores in memory. The signal level applied to the inputs is approximately 50 to 70 millivolts. If the polarity on the sense lines is such that input pin 12 is negative, and input pin 13 is positive, the output at pin 7 will reflect a positive excursion of approximately 0.5 milliamperes. If the polarity at the inputs is reversed or zero, the output at pin 7 will reflect an open circuit.

To overcome any possibility of amplifying undesired noise that may be picked up by the sense lines, a common-mode choke is placed across the inputs offering an easy path to ground for the noise.

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-
mW	-	-	-	-

Figure 7-53. Sense-Control Amplifier, Card Type 7003740



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low input at pin 5, output at pins 14 and 15 will be high. With a high input at pin 5, output at pins 14 and 15 will be an open circuit.

ELECTRICAL DESCRIPTION

This card is normally used to divert current by passing it directly to ground or allowing it to pass on to another circuit.

With a -4.5 volts applied to input pin 5, the output transistors in this circuit are turned on and any positive potential applied to the output pins 14 and 15 is shunted directly to ground. With 0.0 volts applied at input pin 5, the output pins 14 and 15 will reflect an open circuit and infinite impedance to any applied voltage.

To protect against damage, circuits to pins 14 and 15 are connected in parallel to divide power dissipation.

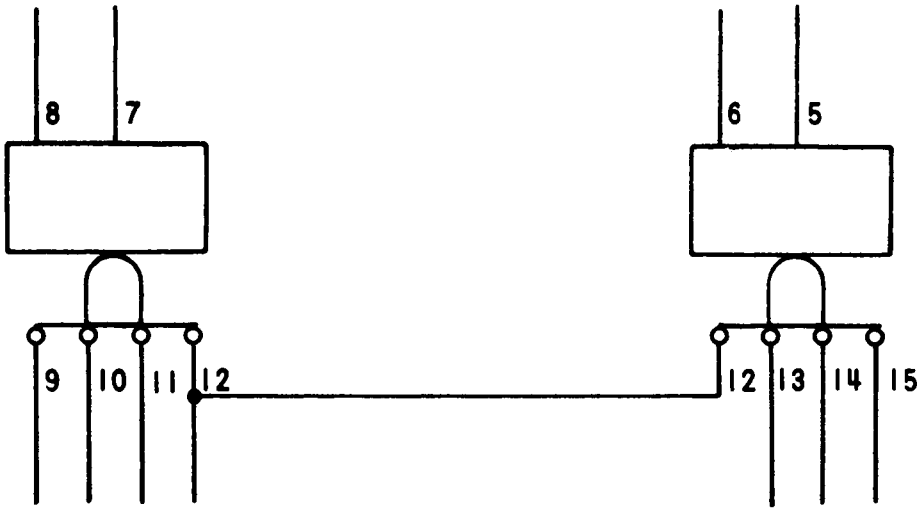
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	Open

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-54. Current-Control Diverter, Card Type 7003760



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to one logic element are low, the output transistor, located between pins 7 and 8 (6 and 5) is turned on to allow current flow between them.

If any one input is high, the transistor is cut off and current is inhibited.

ELECTRICAL DESCRIPTION

Input signals to this module must have nominal positive and negative voltage excursions of 0.0 and -4.5 volts, respectively.

The voltage applied to either pin 7 or 8 is considered the bias voltage to determine the output voltage level.

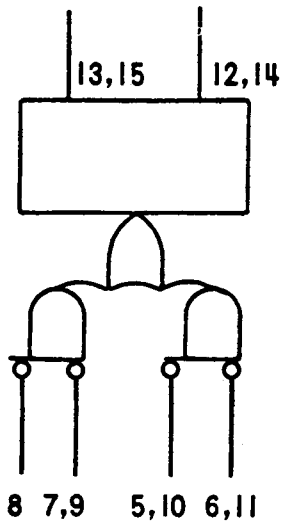
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	N/A
LOW	-4.5 Volts	LOW	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-55. Driver Amplifier, Card Type 7003771



LOGIC SYMBOL

LOGIC DESCRIPTION

With a low at both input pins of either AND gate, the output pins 14 and 15, or 12 and 13, will reflect a closed circuit. With one or more highs at both AND gate inputs, the output pins will reflect an open circuit.

ELECTRICAL DESCRIPTION

The output pins of this card are connected to a transistor that is transformer-coupled with the input circuitry of the card. When -4.5 volts is applied to both inputs of either AND gates, the circuit is enabled, inducing a voltage in the transformer secondary so the base of the output transistor will become positive and the transistor will conduct. At this time, the transistor acts as a switch to an external load providing a potential of ±18 volts. The polarity of this 18 volts depends on which half of the card is operating.

The length of time the output transistor will conduct is determined by the time constant of the transformer secondary and the resistor connected across it.

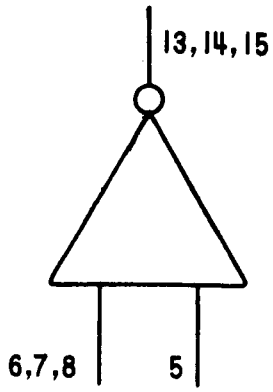
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	N/A
LOW	-4.5 Volts	LOW	N/A

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	-15.0	-4.5
mW	-	-	-	-

Figure 7-56. Driver-Digit Amplifier, Card Type 7003780



LOGIC SYMBOL

LOGIC DESCRIPTION

This circuit recevies nonlogic voltages at its inputs. However, if a sufficiently positive voltage is applied at its input (pin 6, 7, or 8), the respective output (pin 13, 14, or 15) will be a logical low. Without a sufficiently high positive voltage at the input, the respective output pin will be a logical high.

Input pin 5 has a constant non-logic bias voltage applied to it.

ELECTRICAL DESCRIPTION

This circuit is a three-stage amplifier normally used for amplifying small pulses from a core memory and contains three identical circuits and a common bias supply (pin 5). The bias voltage applied at pin 5 is -10 volts. With a positive voltage applied to one of the input pins, the forward bias to the input transistor is sufficiently reduced, cutting it off. This results in an output at the respective output pin of -4.5 volts. With an open at the input pins, the bias will be sufficient enough to allow the input transistor to conduct and, consequently, the output transistor. With the output transistor conducting, the output of the circuit is placed at 0.0 volts or ground potential.

LOGIC

INPUT		OUTPUT	
HIGH	N/A	HIGH	0.0 Volts
LOW	N/A	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Gnd	+15.0	N/A	-4.5
mW	-	-	-	-

Figure 7-57. Output-Sense Amplifier, Card Type 7003850

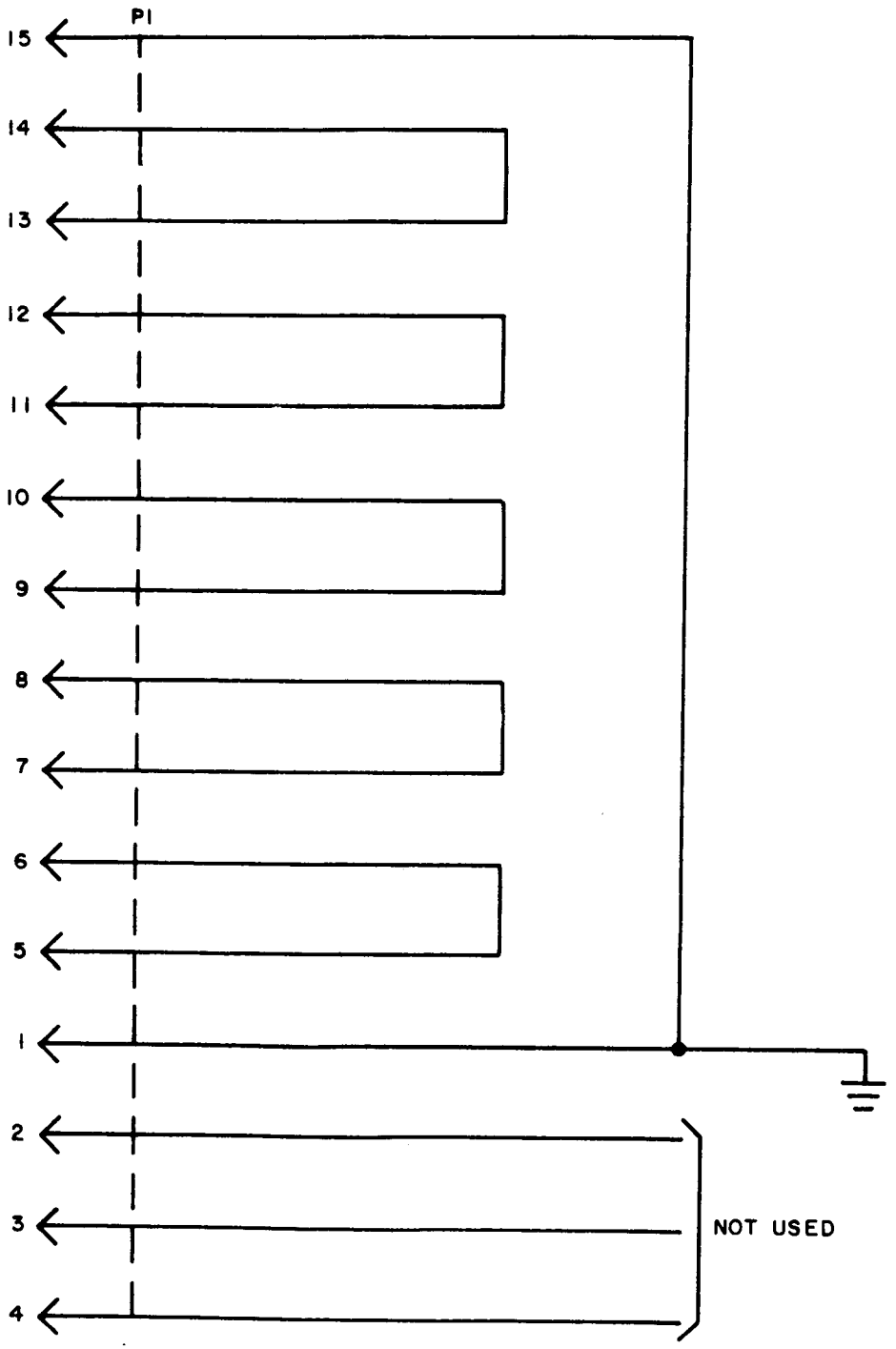


Figure 7-58. Jumper Switch Selector, Module 7104010 Schematic Diagram

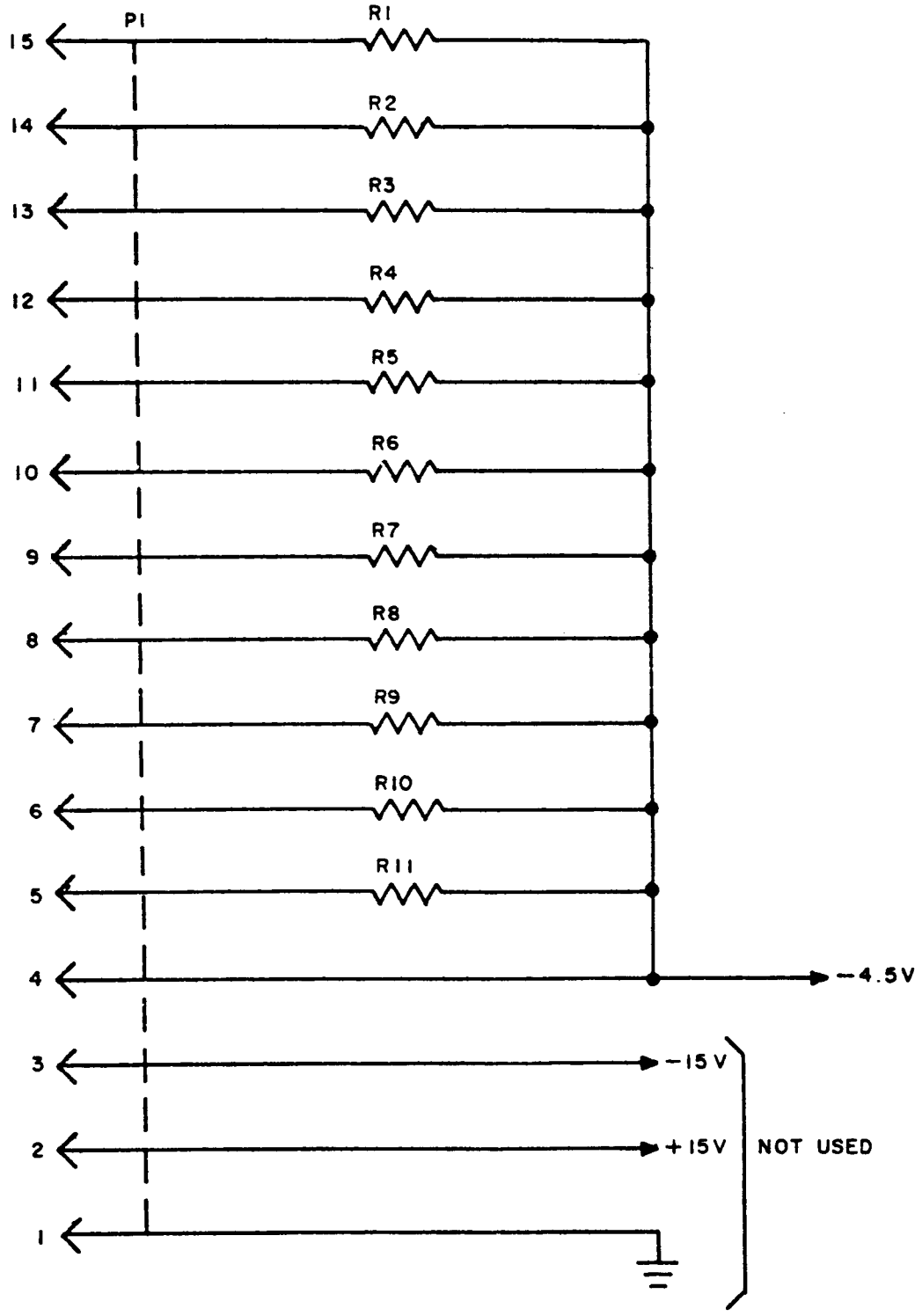
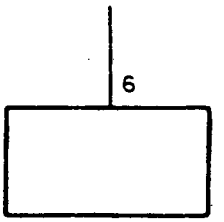


Figure 7-59. Resistor Assembly, Module 7109000 Schematic Diagram



LOGIC SYMBOL

LOGIC DESCRIPTION

When power is applied to the unit, the output, pin 6, will be high and after the R-C time constant of resistor R2 and capacitor C2, the output will become low. The low will be maintained while power is applied to the unit.

ELECTRICAL DESCRIPTION

This module contains a resistor-capacitor network made up of two resistors and two capacitors. The module is used to filter the voltages used for indicators.

LOGIC

INPUT		OUTPUT	
HIGH	-	HIGH	-
LOW	-	LOW	-

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	G	+15v	-15v	-4.5v

Figure 7-60. Capacitor - Resistor Assembly, Module 7109010

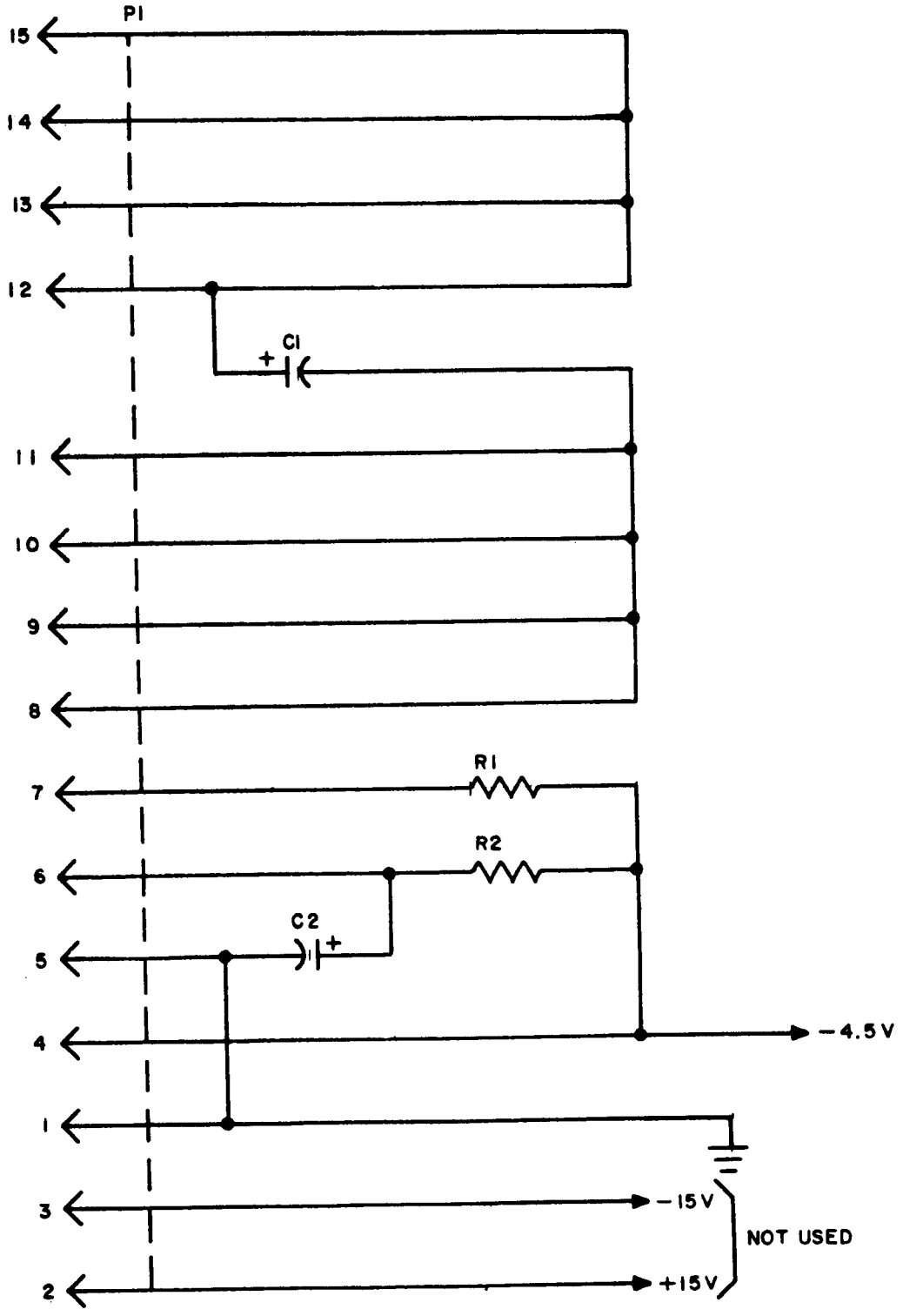


Figure 7-61. Capacitor - Resistor Assembly, Module 7109010 Schematic Diagram

7-91. TYPE B PRINTED CIRCUIT MODULES. Figures 7-62 through 7-87 depict the type B printed circuit cards. A brief functional description of these cards is given in the following subparagraphs.

7-92. Module 7500040 (Inverter, Amplifier, Driver). This module contains five identical circuits that are used for AND, OR, INVERTER AND/OR, or OR/AND functions. The module contains discrete components such as: transistors, diodes, resistors, and capacitors. These components are required, rather than flat packs, in order for each circuit to provide the necessary power to drive a large number of circuits at a propagation time unchanged by the load. Figure 7-62 shows the logic symbols and figure 7-63 shows the schematic diagram.

7-93. Two types of AND and OR functions can be performed by the 0040 module. The module functions as a high input AND or low input OR when either pin 43, 44, or 46 is grounded. When the inputs on pins 51 and 52 are high, the output is low. When either input on pins 51 and 52 is low, the output is high. When only one input is used, this circuit performs an INVERTER function. Unused pins are left open. The module functions as a low input AND or high input OR by using either pin 43, 44, or 46 for one input and either pin 51, 52, or 54 for the other input. When both inputs to this circuit are low, the output is high. When one of the inputs is high, the output is low. Unused pins are left open.

7-94. The 0040 module also performs an OR/AND or AND/OR function. When one of the inputs to pins 43, 44, and 46 is low and one of the inputs to pins 51, 52, and 54 is low, the output is high. When all the inputs to pins 43, 44, and 46 are high or all the inputs to pins 51, 52, and 54 are high, the output is low.

7-95. Module 7500260 (Oscillator, Clock Delay Line and Amplifier). This module contains an amplifier and delay line interconnected as shown in figure 7-64 to form an oscillator. The external connections between the delay line and the amplifier (pins 27 and 29) determine the cycle of the oscillator. The gate inputs (pins 19 and 20) and the individual input (pin 26) control the oscillator.

7-96. Figure 7-65 shows a schematic diagram for the 0260 module. In the quiescent state, the amplifier circuit is disabled (low is input to pin 19 or 20 and pin 26). The oscillator is disabled by the low output of the amplifier and all delay line taps are low. The circuits remain in this state until a high input is applied to pins 19 and 20 or pin 26 of the amplifier. Then the output of the amplifier goes high (+5.5 volts) and this high begins propagating down the 1 microsecond delay line. The high output from the amplifier is also coupled back to the input. This enables the oscillator to complete a cycle even if the enabling signals (high input to pins 19 and 20 or pin 26) that started the oscillator are removed. When the high signal propagating down the delay line reaches pin 6 (975 nanoseconds later), the amplifier is disabled. The output from the amplifier goes low and a low begins to propagate down the delay line. When this low signal reaches pin 3 (1 microsecond later), the amplifier is again enabled provided the high input is still present at pins 19 and 20 or pin 26. Another oscillator cycle begins.

7-97. The waveform in figure 7-64 is dependent upon the interconnections between the amplifier and delay line. For example,

the duration of the high level of the waveform is determined by the first delay line tap that connects to the amplifier. The duration of the low level is determined by the other delay line tap that connects to the amplifier. If the oscillator is disabled any time during the high level of the cycle, the oscillator completes the high level and then drops to the low level.

7-98. When the input to pin 26 is high or the inputs to pins 19 and 20 are high, the +5.5 volt level propagates through the delay line reaching an output pin every 25 nanoseconds.

7-99. The oscillator will continue to produce pulses until the enable inputs are removed. If the enable inputs are removed when the amplifier output is at the +5.5 volt level, feedback will hold the output until the +5.5 volt level of the cycle is complete.

7-100. Module 7500280 (Emitter Follower, Driver Amplifier). This module contains three distinct circuit configurations: Four circuit groups consisting of a combination of regular discrete components comprising emitter-follower input driving a gated integrated inverter-output circuit (one part of a type 1001 flat-pack); four circuit groups consisting only of discrete components comprising emitter-follower inputs; and two type 1001 flat-packs. The logic descriptions are based on the logic symbols shown in figure 7-66. Figure 7-67 shows the schematic diagram.

7-101. For the emitter follower with gated output, a low input on the emitter-follower input pin 17 produces a high input to the associated AND inverter; a coincident high gating signal produces a low output from the circuit. By applying a constant high to the gated input pin (pin 27) the circuit can be used as a non-inverting amplifier. For example, a high input to pin 17 produces a high output from pin 30.

7-102. A high input on the emitter-follower pin 9 produces a low output (approximately 0 volts) on pin 10, and a low input produces a high output.

7-103. The integrated logic circuits perform AND or OR functions. If both inputs to the circuits are high, the output is low. If one input is low, the output is high.

7-104. Module 7500320 (Voltage Regulator). This module is an adjustable voltage regulator used to drive an external high-power transistor (Q1) which regulates the +3VDC power supply in main memory. Refer to figure 7-68 for the schematic diagram of the regulator module and to figure 9-196 (plate P-179) for the schematic of the +3VDC regulator circuit. The voltage sensing input of the regulator module is at pin 34. The output of the regulator module is at pin 14; this output controls the conduction of the external power transistor which is connected as a shunt regulator across the +3VDC line.

7-105. The action of regulator module 7500320 is as follows: Module transistor Q1 acts as a constant current source supplying emitter current to transistors Q2a and Q2b which are connected together as a differential amplifier. The voltage at the base of Q2a is held constant by Zener diode CR1. Potentiometer R6 allows adjustment of the base voltage making adjustment of the +3VDC level possible. Assume that increased loading on the 3VDC

line causes a decrease in the 3VDC power supply output voltage. The voltage at pin 34 of the module and on Q2b base goes lower increasing the forward bias on transistor Q2b. The emitters of both Q2a and Q2b are connected to a constant current source. As the emitter current of Q2b increases due to increased forward bias, the emitter current of Q2a decreases correspondingly. This causes a drop in the voltage across resistor R17 and ground (pin 16) which is amplified by direct-coupled NPN transistors Q3 and Q4. Decreased conduction of Q3 and Q4 produces a voltage increase at their collectors. This voltage increase is applied through R22 and R23 to the base of PNP transistor Q5 reducing its forward bias and collector current. As collector current of Q5 decreases, the voltage across resistor R24 drops and this reduced voltage is applied to each base of parallel connected NPN transistors Q6 through Q10 thereby decreasing their conduction. These five transistors are used in parallel to provide sufficient current from pin 14 to the base of external power transistor Q1. In this example, the conduction of external transistor Q1 (see figure 9-196) is reduced because decreased base current is supplied by the regulator module. With less current being shunted through external circuit components R1 and Q1, less voltage is dropped across external series resistor R2 which tends to raise the 3VDC power supply output voltage toward its original level.

7-106. Module 7500340 (Voltage Sensor). This module contains two voltage detecting networks. Figure 7-69 shows logic symbols and figure 7-70 shows a schematic diagram of the voltage sensor circuits. Figure 9-160 shows a circuit application of the 0340 module. When the power tolerance circuit detects a loss of -6 percent in the +15 volt supply, the output goes high (pin 10). When the power failure sensor detects a failure in one of the -3, -15, +2.5, +5.5, +15 or -15 volt supplies or a loss of 9 percent in the +15 volt supply, the output goes high (pin 5).

7-107. The Voltage Sensor Module contains the following component groups:

1. Detector Output Circuit Groups. Transistors Q9 and Q13 comprise the -6 percent detector output; transistors Q3 and Q10 comprise the -9 percent detector output. In both cases, normal operation occurs with transistors Q13 (-6 percent) and Q10 (-9 percent) conducting and supplying a ground potential to the computer circuits connected to pins 10 and 5, respectively. The Q4 transistor stage is independent of -6 percent and -9 percent changes in the monitored +15 volt supply; the stage serves as a constant current source providing approximately +7.5 volts to the Q3 and Q9 emitters. When a -6 percent decrease in the monitored +15 volt supply is detected, Q9 becomes biased to cutoff, turning off Q13 and removing the ground from pin 10. The -9 percent detector circuit is controlled from the diode OR configuration of diodes CR11 and CR13. When either a voltage failure is detected (CR11), or a -9 percent decrease in the monitored +15 volt supply is detected (CR13), transistor Q3 will be biased to cutoff, turning off Q10 and removing the ground from pin 5.

2. Voltage Failure Detection Group. Transistors Q1 and Q2 comprise voltage failure detectors which monitor all power supply voltages with the exception of the +15 volt supply monitored by the voltage ratio detectors. During normal operation, transistor Q1 is conducting and Q2 is biased to cutoff. If a failure occurs in the -3 or -15 volt supply, Q2 will become forward-biased, driving Q1 to cutoff and removing

the forward bias from Q3. Transistors Q3 and Q10 will be turned off, thereby removing the ground from pin 5. A voltage failure of any of the +2.5, +5.5 or -15 - volt supplies will result in transistor Q1 being biased to cutoff; the resulting circuit operation is the same as just described.

3. Voltage Ratio Detector Group. Two similar voltage ratio detector circuits are used. Transistors Q5, Q8, and Q12 comprise the -6 percent ratio detector and Q6, Q7, and Q11 comprise the -9 percent ratio detector. Transistor Q14 is independent of -6 or -9 percent changes in the monitored +15 volt supply and serves as a constant current source for transistors Q11 and Q12. For their respective circuit groups, the dual transistors, Q5 and Q6 comprise the differential circuits; Q8 and Q7 comprise the ratio detector stages, and Q12 and Q11 comprise the output amplifiers. Transistor Q12 drives the -6 percent detector output circuits and Q11 via OR diode CR13 drives the -9 percent detector output circuits. A constant reference voltage is derived from the monitored +15 volt supply via resistors R22 and R25 and Zener diodes CR14 and CR15; potentiometer R26 is adjusted to supply the required reference voltage. The reference voltage is applied to one side of the differential stages (Q5a, Q6b) in each ratio detector with transistor Q6b supplied from voltage divider R29, R33. A voltage representative of the monitored +15 volt supply is applied to the other side of the differential stages from the junction of the voltage divider network R17 and R35. Assuming that a -6 percent ratio change occurs, the Q5a-b conduction will bias Q8 to cutoff, removing the bias from Q12. With Q12 off, its positive collector voltage biases Q9 to cutoff, which in turn biases Q13 to cutoff, removing the ground from pin 10. Assuming a -9 percent ratio change occurs, the Q6a-b conduction will bias Q7 to cutoff, removing the bias from Q11. With Q11 off, its positive collector voltage via CR13 biases Q3 to cutoff, which in turn biases Q10 to cutoff, removing the ground from pin 5. A complete failure of the monitored +15 volt supply will result in both Q10 and Q13 being biased to cutoff, removing the ground from both pins 5 and 10.

7-108. Module 7500400 (Bipolar Memory Switch). This module contains six bipolar memory switches. Each circuit is enabled by four inputs. Some of the input pins are common to several bipolar switches. Figure 7-71 shows the logic symbol of one bipolar switch, and figure 7-72 shows the schematic diagram. When the four inputs of a circuit (pins 17, 18, 20 and 28) are all high, its associated bipolar switch is turned on. Current may flow from pin 6 to pin 9 or from pin 11 to pin 54. When one of the four inputs is low, the bipolar switch is turned off. As used in the computer, two bipolar memory switches are selected for each read or write operation and together enable one drive line. Pins 6 and 54 are grounded. Each drive line is connected through a bipolar memory switch in series with two transformer secondaries, a read or write diode and each end is grounded by bipolar memory switch. The transformers induce current in the drive lines. Read current flows in the opposite direction of write current. Current can flow from ground through pin 6 to pin 9, or from pin 11 to pin 54 to ground, depending upon the polarity of the voltage induced by the transformers.

7-109. Module 7500421 (Read/Write Diverter Driver). This module contains

one read/write diverter, a read diverter driver, and a write diverter driver. Read and write diverter drivers are identical. All three circuits are enabled by a common inverter.

1. Read/Write Diverter. Figure 7-73 shows the logic symbol and 7-75 shows the read/write diverter schematic. When input to pin 44 is low and input to pin 52 is high, the read/write diverter is enabled and no current flows through X or Y drive lines. When input to pin 44 is high or input to pin 52 is low, the read/write diverter is disabled and current flows through selected X or Y drive line.

2. Read and Write Diverter Drivers. See figure 7-74 for the read and write diverter drivers logic symbol. When the input to pin 44 is low and the input to pin 48 is high, half of the drive current required by an X or Y drive line is induced in one of the secondary windings of the output transformer. The selected secondary is part of a complete circuit at this time, while the other seven secondaries are open-circuited by bipolar switches. When the input to pin 44 is high or the input to pin 48 is low, no drive current is induced in one of the secondaries. No current flows in the seven secondaries which are not enabled by the bipolar switches. Half of the current required by a drive line flows in the enabled secondary.

7-110. Module 7500431 (Read/Write Selection Matrix Transformer Assembly). This module contains two identical circuits. Each circuit has three enable inputs. The output is half of the current required by an X or Y drive line and is taken from one of the eight secondaries on the output transformer. External circuits are wired so that only one of the secondaries draws current at a time. Pairs of secondaries from the two identical circuits are connected through isolation diodes to shared pins on the connector. This conserves output pins so that two circuits can be built on one 56-pin module. Figure 7-76 shows the logic symbol of one of the circuits, and figure 7-77 shows the schematic diagram. When the inputs to pins 47, 48, and 52 are high, half of the drive current required by an X or Y drive line is induced in one of the secondaries of the output transformer. When any of the three inputs is low, no drive current is induced in any of the secondaries. When pins 47, 48, and 52 are high, pin 9 of Z10 is low. Transistor Q3 is forward biased and turns on, causing current to flow through the primary of transformer T1. Current flows in the secondary of T1 and turns on Q1. As wired in the computer, pins 25 and 36 are connected to the read and write diverter driver transformer primary circuits and pin 3 is connected to a regulator. When pins 47, 48, and 52 are high, a read or write diverter driver is enabled, and the read/write diverter is disabled. Only one of the eight secondaries is enabled by the combined action of two bipolar switches. The other seven secondaries are disabled and open circuited by fourteen other bipolar switches. Half of the current required by an X or Y drive line is induced in the selected secondary, which is connected in series with read or write diverter driver transformer secondary, a read or write diode, two bipolar switches, and an X or Y drive line.

7-111. Module 7500651 (Sense and Inhibit Amplifier). This module contains inhibit drivers, sense amplifiers, one bit of the Z

register and current overload detection circuits. Figure 7-78 shows a condensed logic symbol, and figure 7-79 shows a schematic diagram. A simplified diagram showing the stack connections is given on figure 2-79 in Volume 1 of this OP.

1. Inhibit Driver. This module contains four inhibit drivers, each of which supplies inhibit current to one of 32 planes in one of four stacks. Each inhibit circuit is enabled by one AND gate. Only one AND gate is enabled at a time. This occurs when a high is applied to one of the stack select inputs (pins 36, 40, 41, or 42), if the overload flip-flop is set, no power failure (pin 52 high), and the corresponding bit of Zm register is not set. All inhibit drivers are disabled when overload flip-flop is clear, a power failure exists, or corresponding bit of Zm register is set. A sense/inhibit line from pin 23 passes through half of the 4096 cores on one memory plane and returns to pins 25 and 26. A second sense/inhibit line from pin 24 passes through the other half of the cores and also returns to pins 25 and 26. Pin 52 is high whenever all power supply voltages are normal. When pin 52 goes low, all four inhibit drivers are disabled. After a power failure condition, computer power must be turned off and reapplied to enable the four AND gates comprising Z4.

2. Sense Amplifier. When the coincidence current switches one core in a plane of one of four stacks during a read cycle (as sensed by input pins 23 and 24, 19 and 20, 15 and 16; or 9 and 10), the output pin 32 will be positive. When no core is switched the output pin 32 will be less positive. Input pins 23 and 24 are connected to one end of a sense/inhibit line, which passes through the 4096 memory cores on a single plane. Each of the other three pairs of input pins 19 and 20, 15 and 16, and 9 and 10 are similarly connected to a single plane in a different stack. Other circuits in the memory select one of the four stacks and pulse one X line and one Y line when data is read from the memory. The content of the single core at the junction of the selected X and Y lines of the selected stack is applied across one of the pairs of input pins. If the selected core does not switch, no difference in voltage is developed across the two input pins. The noise in each sense/inhibit line is equal and cancels. If the selected core is switched, a difference in voltage (approximately 30 millivolts) is developed across the two input pins. One sense/inhibit line carries only noise and the other carries a pulse generated by the switched core. One Zm register flip-flop is associated with four sense/inhibit lines and four inhibit drivers. The Zm register flip-flop sets when the sense amplifier detects a core has switched during a read cycle (pin 34 and pin 48 high) or during the first portion of a write cycle when a bit is to be stored (pin 43 and pin 44 high). It clears when pin 47 goes low. When the flip-flop is set, the inhibit drivers are disabled so that during the write cycle the selected core is allowed to switch.

7-112. Module 7500660 (Capacitor-Diode Assembly). This module contains a series of capacitors and diodes which are required by other modules in the computer logic. No logic symbol is required for these components. Figure 7-80 shows the schematic diagram of this module.

7-113. Module 7500671 Capacitor Assembly. This module contains five capacitive filters. Figure 7-81 shows the schematic diagram of one of the networks. Each capacitor is coupled to two voltage pins and to three resistors.

Pins 7 and 8 are standard +6V pins; pins 13 and 14 are +15V; pins 37 and 38 are -15V; pins 43 and 44 are -3V; and pins 55 and 56 are +3V pins. When the module is in place on a chassis, the capacitors provide additional filtering thereby inhibiting spurious signals from being received and transmitted by the voltage pins of the other modules on the chassis. The resistors isolate the test points and output pins from the voltage source for short circuit protection. The output pins are normally used for voltage supply to voltage sensor circuits such as the 0340 module.

7-114. Module 7500761 (Level Changer Amplifier). This module contains level changers for converting both from memory voltage levels to computation logic voltage levels and vice-versa. Figure 7-82 shows the condensed logic symbol and figure 7-83 shows the schematic diagram of this module. Computation logic voltages of -4.5 or 0 volts are applied to pins 15, 16, 23, 36, 40, or 48. These are converted to 0V and +3V memory voltage levels. Plate numbers P-137, P-138, and P-175 show the logic diagrams for these conversions. Conversion from memory voltages to computation voltage levels is accomplished at pins 25 and 28, 27 and 30, 31 and 32. The gates at these inputs, drawn as AND gates on the schematic diagram, are shown as OR gates in the computer functional schematics (lower half of Plate number P-175) by interchanging the gate and negation circle symbols.

7-115. Module 7500781 (Voltage and Current Regulator). This module contains three identical current regulators and one voltage regulator. Logic descriptions of these circuits are unnecessary and not included. Figure 7-84 shows the logic symbol for one of the three current regulators and the voltage regulator and also includes the external circuits wired to the regulators. Figure 7-85 shows the schematic diagram of this module.

7-116. Module 7500900 (Amplifier, Driver-Logic, Noninverting). This module contains ten identical circuits which are represented by the logic symbols shown in figure 7-86. If a low input of 0.0 volts is applied to either pin 31 or 32, a low output of 0.0 volts will appear on both pins 21 and 22. If a high input of +2.5 volt appears on both 31 and 32, a high output will appear on both pins 21 and 22. This circuit is normally used to drive nine logic elements as a noninverting logic driver. Figure 7-87 shows the schematic diagram for this module.

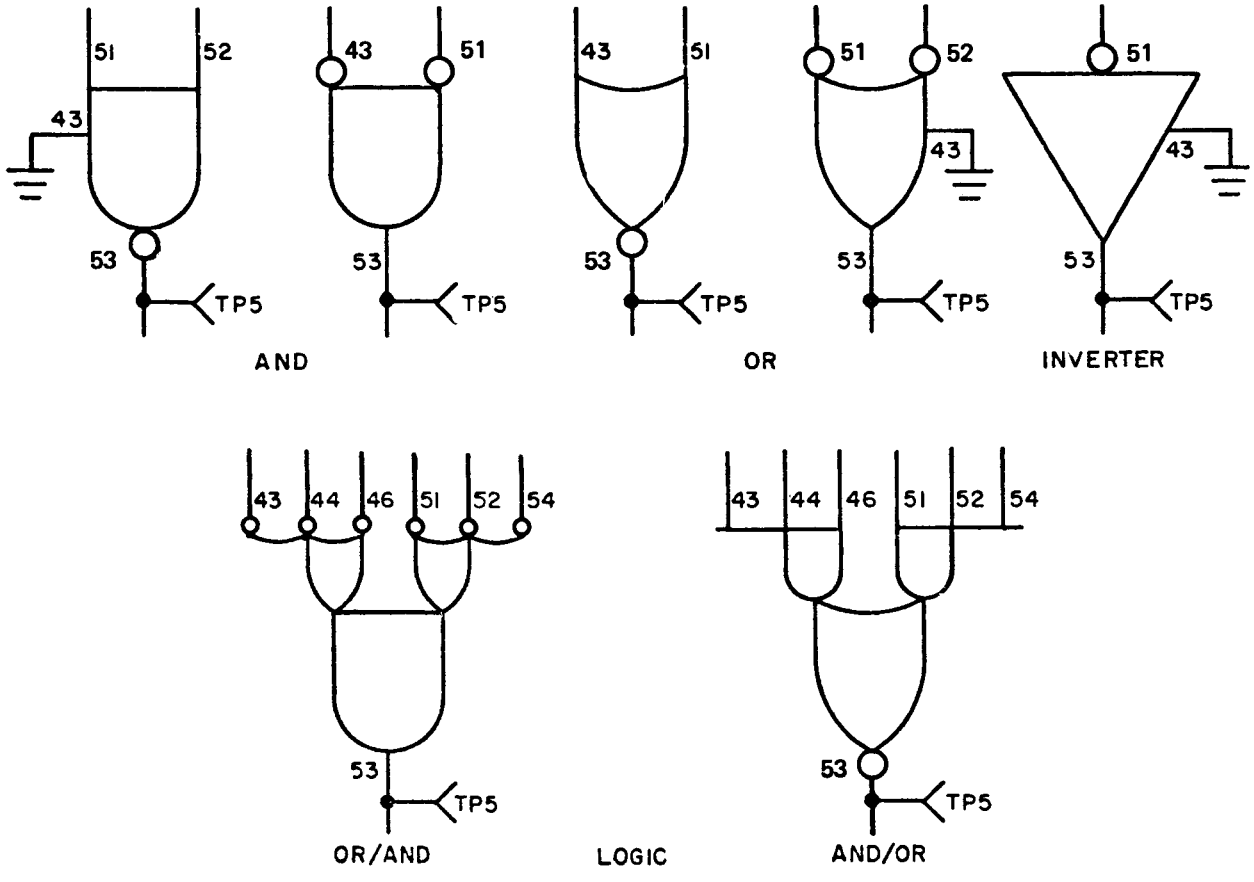


Figure 7-62. Amplifier Driver, Inverter, for Module 7500040

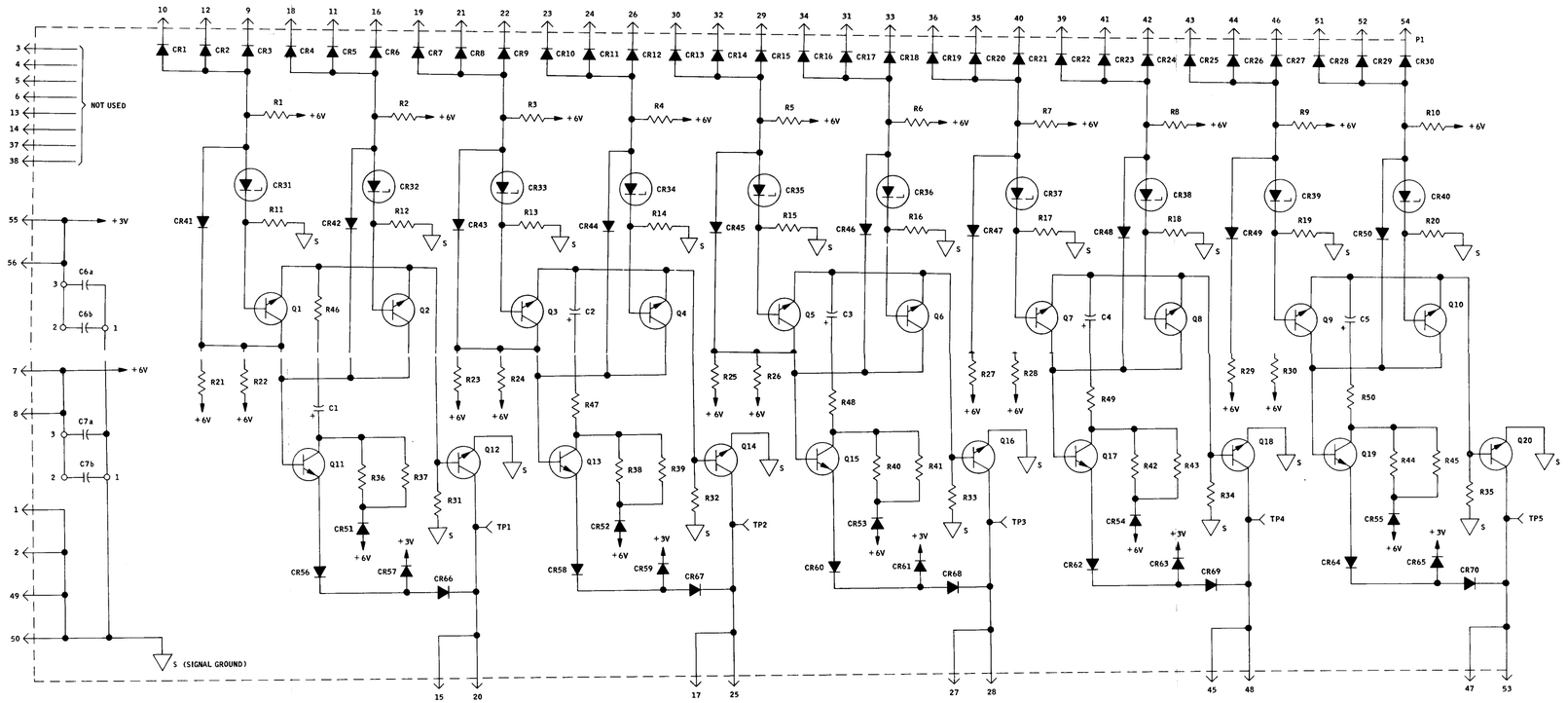


Figure 7-63. Module 7500040 Schematic Diagram

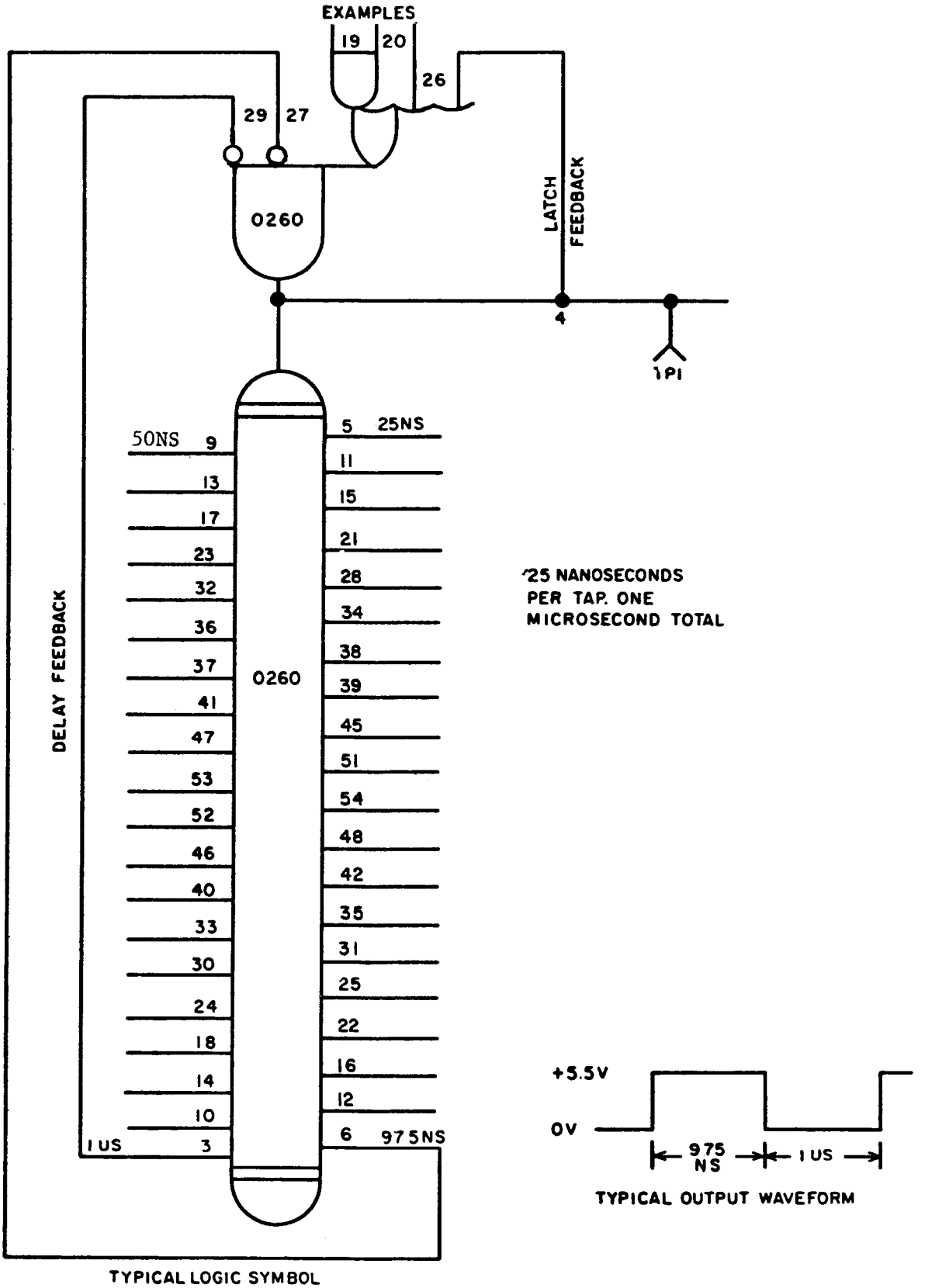


Figure 7-64. Oscillator, Clock Delay Line and Amplifier, Module 7500260

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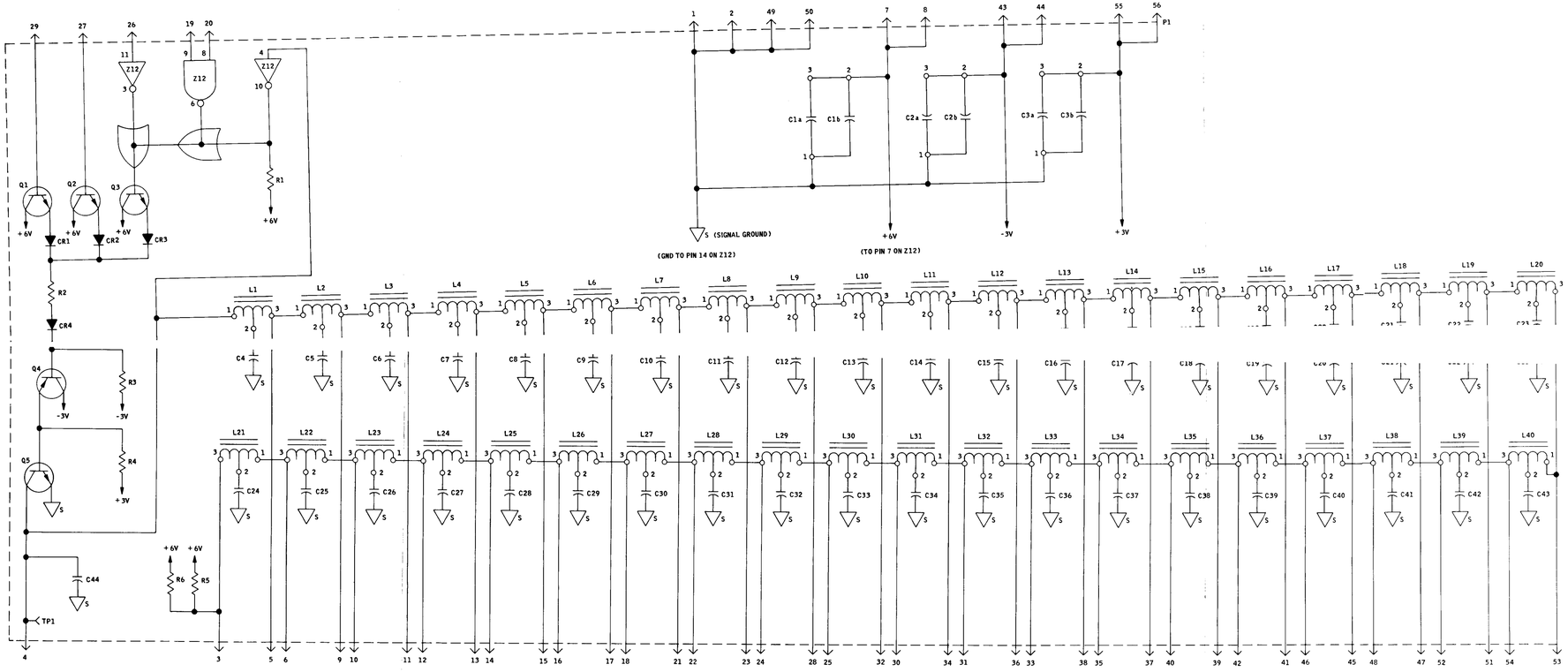

Figure 7-65. Module 7500260 Schematic Diagram

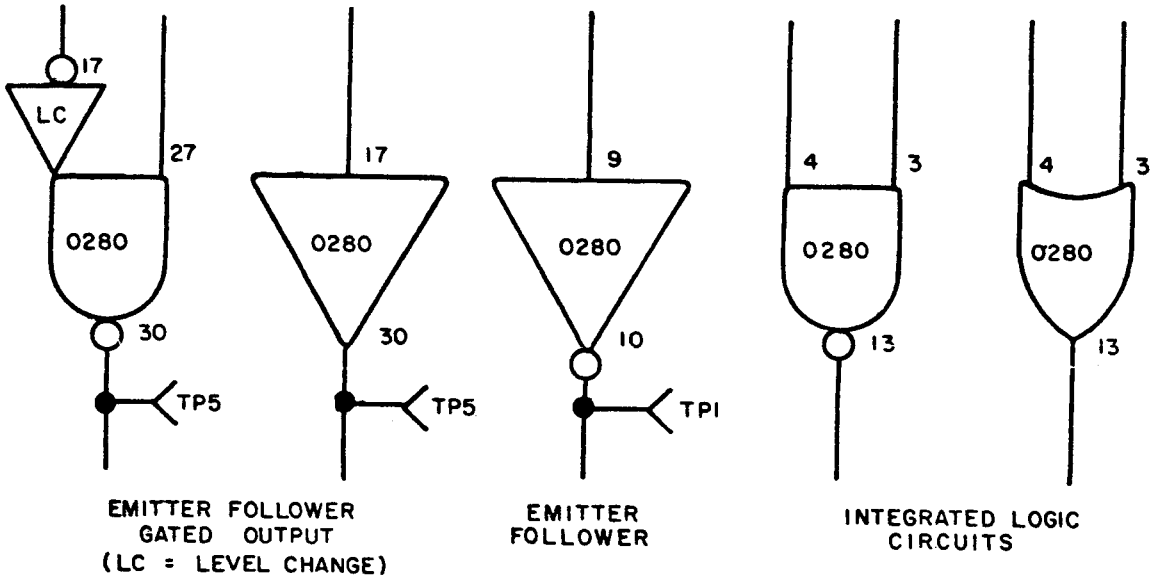

Figure 7-66. Emitter Follower, Driver Amplifier, Module 7500280

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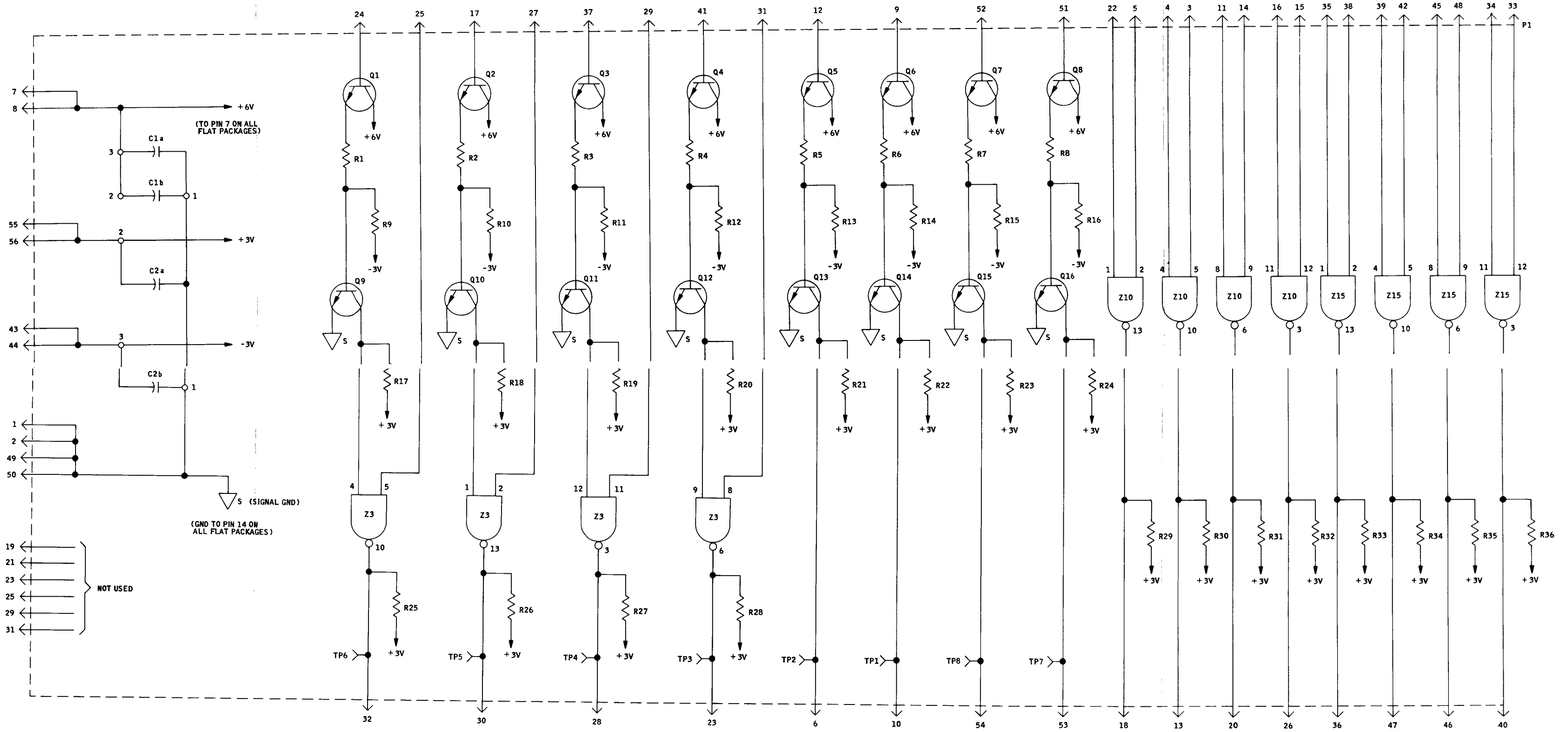

Figure 7-67. Module 7500280 Schematic Diagram

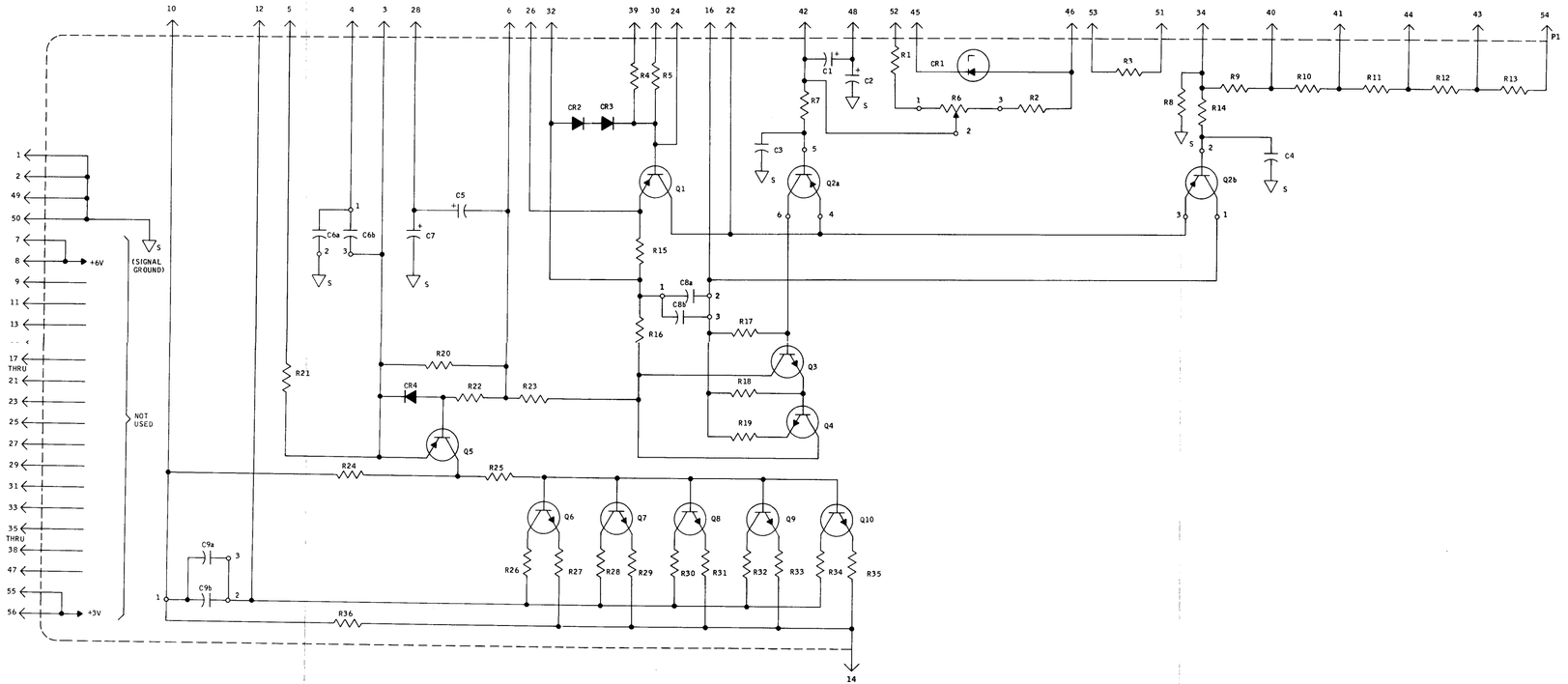

Figure 7-68. Module 7500320 Schematic Diagram

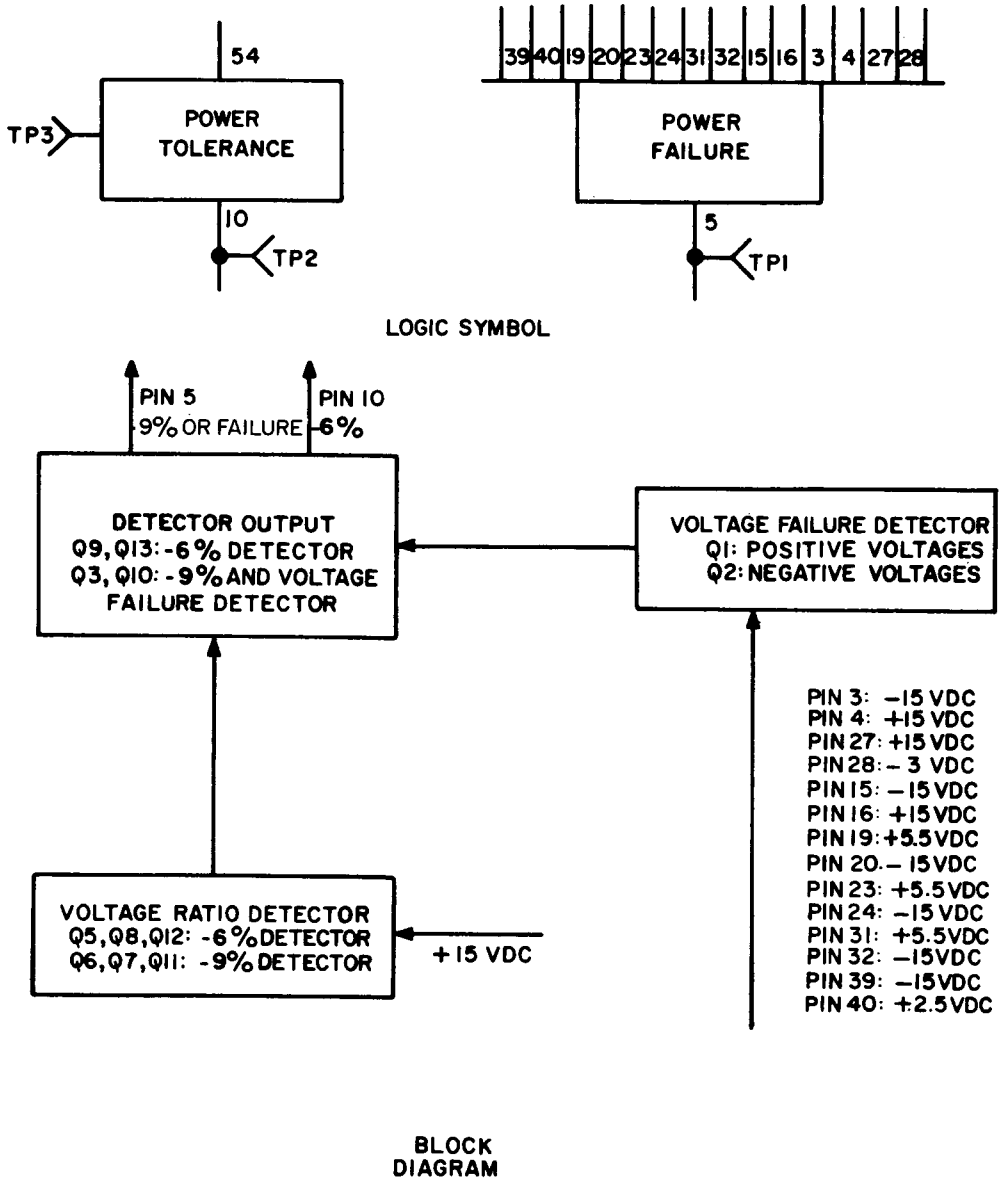

Figure 7-69. Voltage Sensor, Module 7500340

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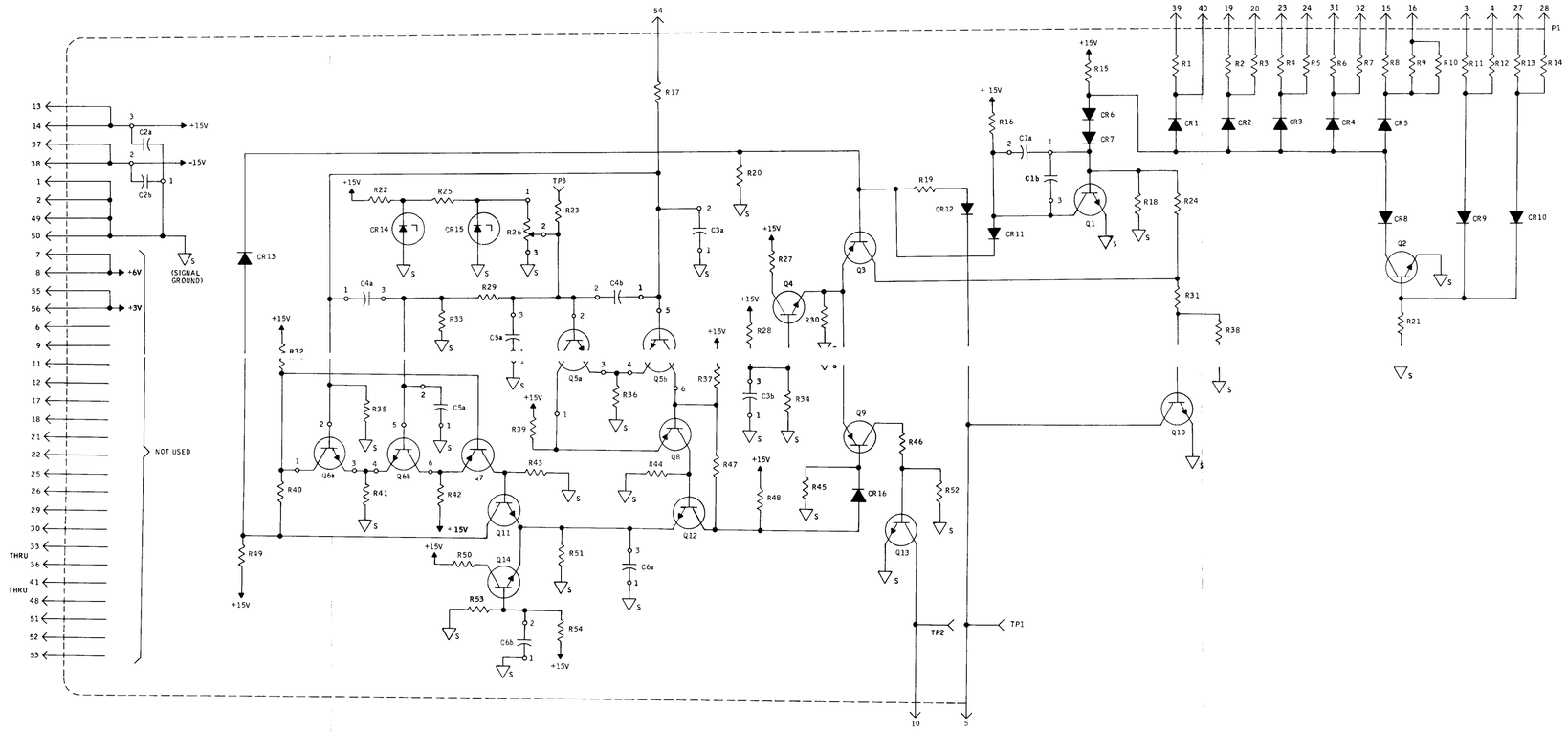

Figure 7-70. Module 7500340 Schematic Diagram

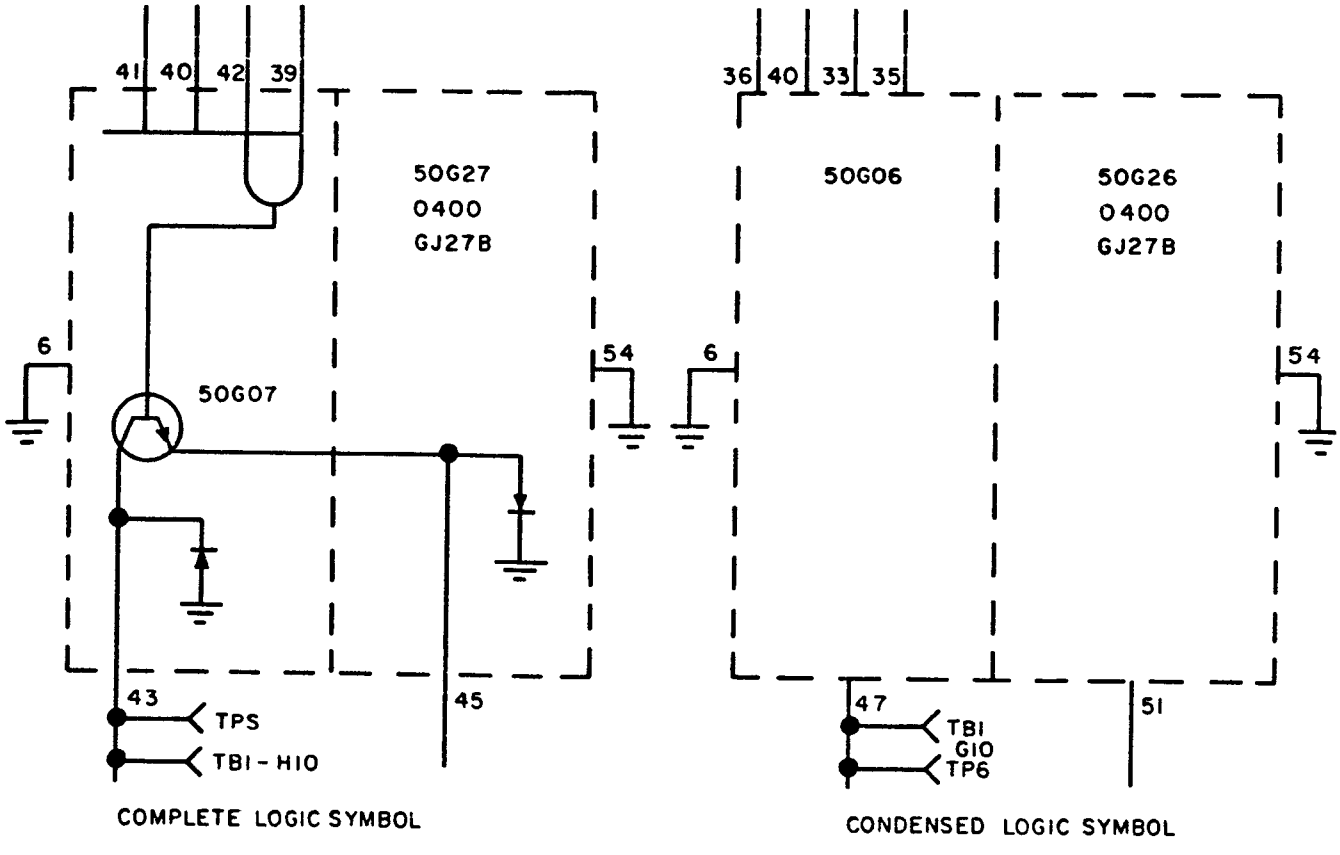

Figure 7-71. Logic Symbol of One Circuit on 7500400 Module

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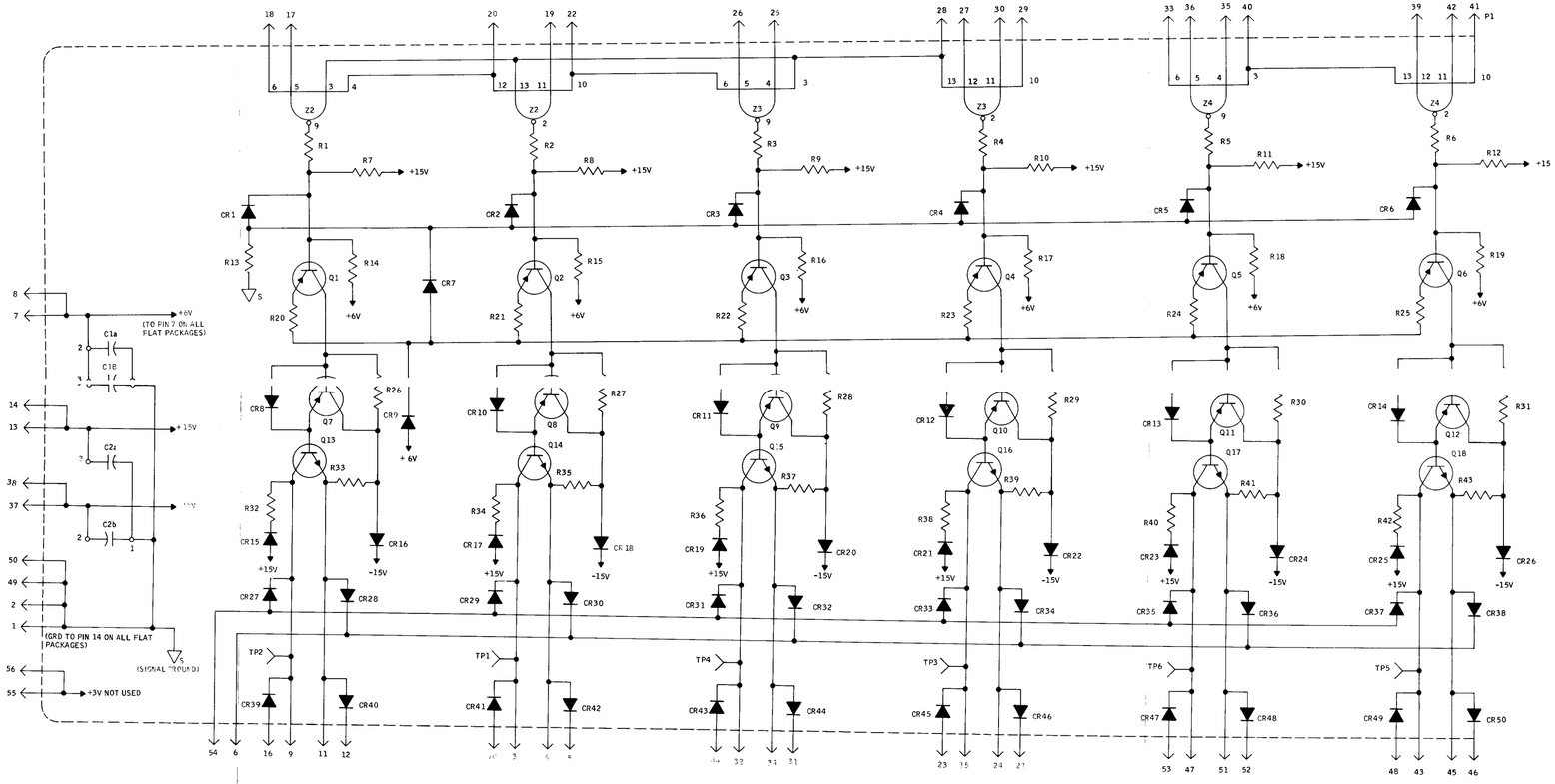

Figure 7-72. Module 7500400 Schematic Diagram

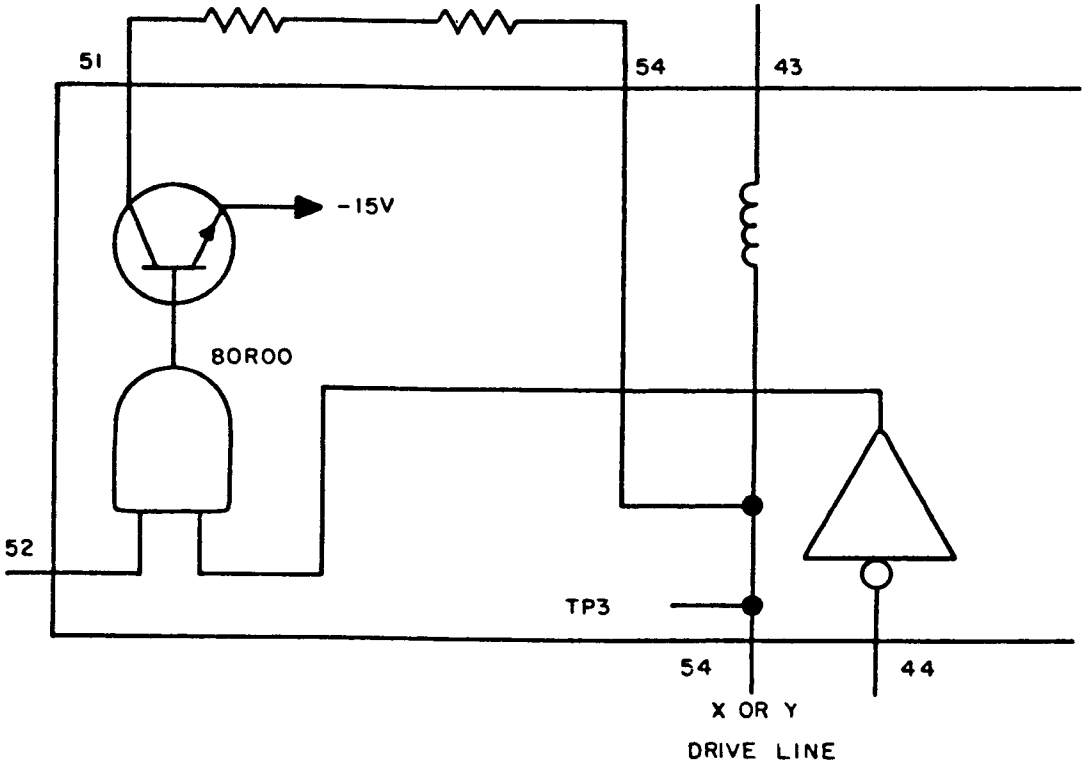

Figure 7-73. Logic Symbol of Read/Write Diverter on Module 7500421

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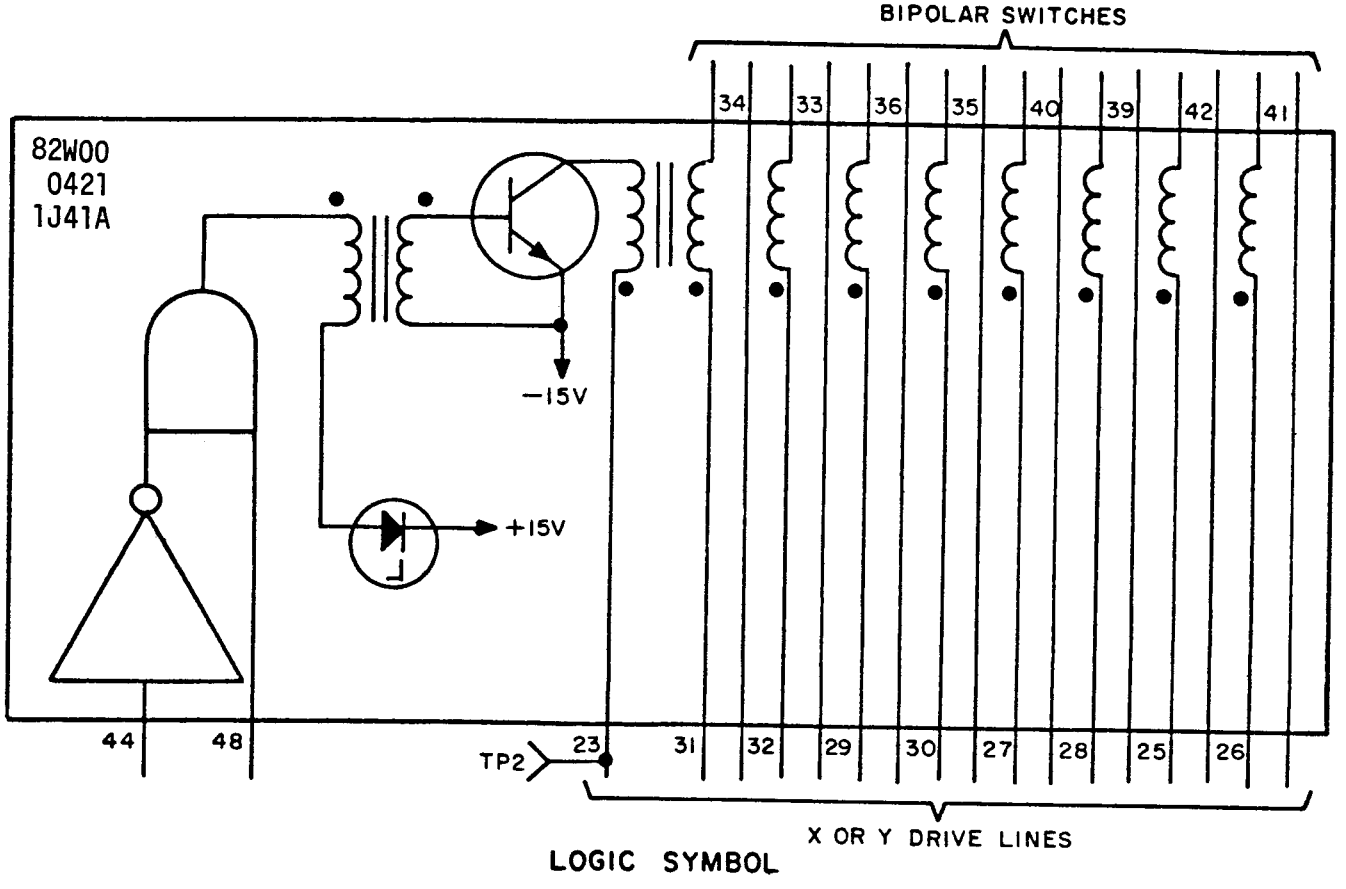

Figure 7-74. Logic Symbol of One Diverter Driver Module 7500421

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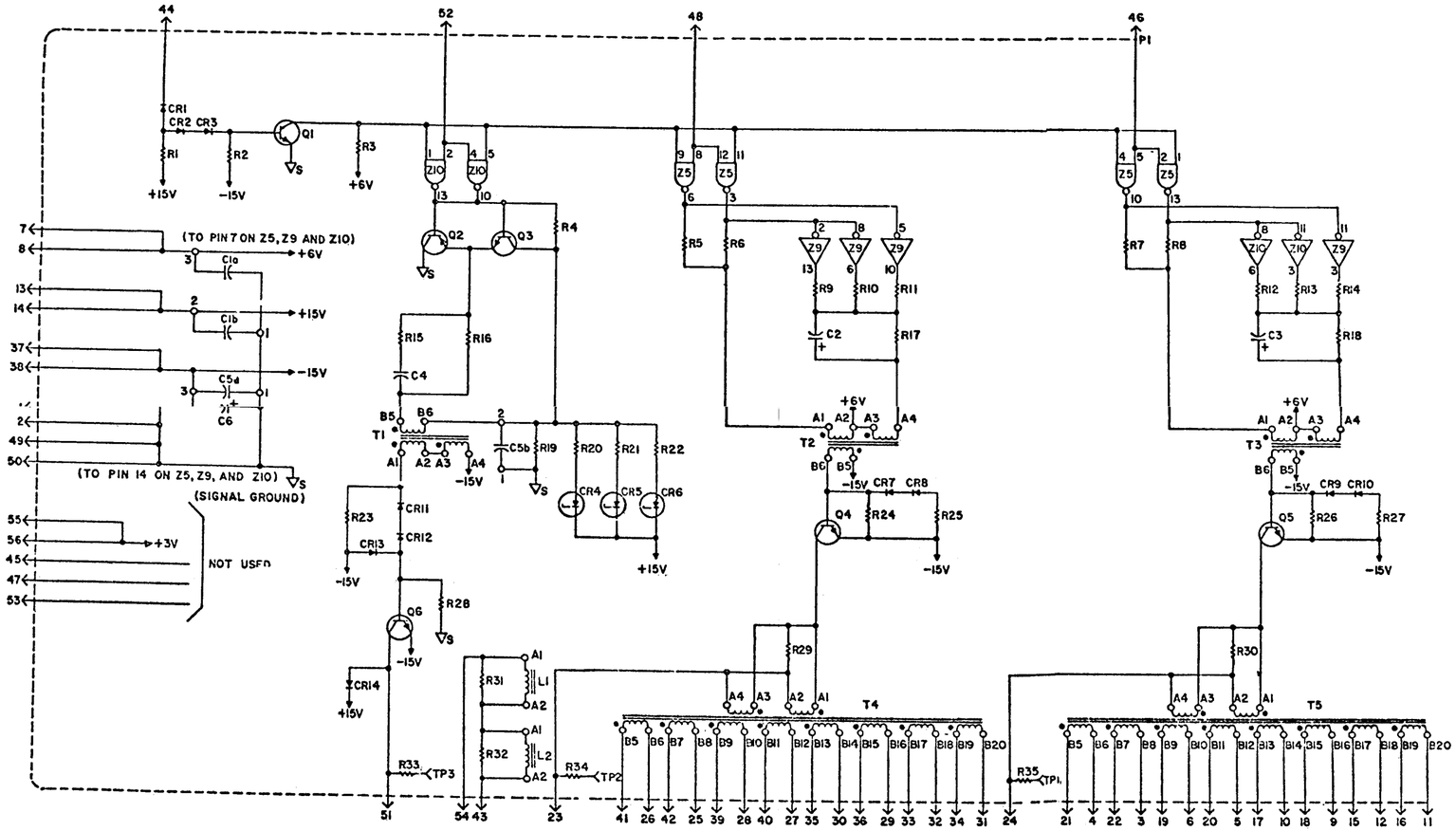
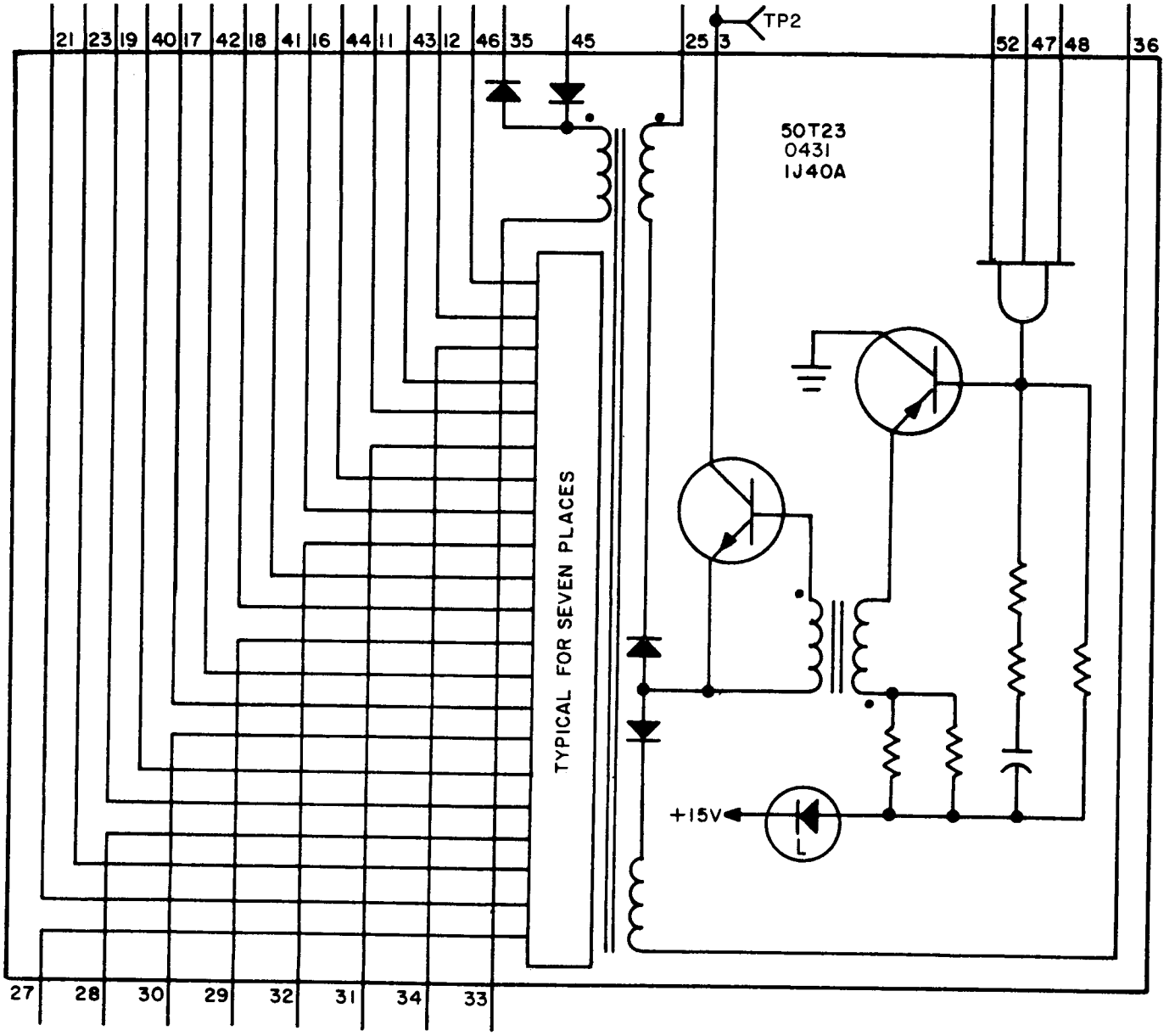


Figure 7-75. Module 7500421 Schematic Diagram



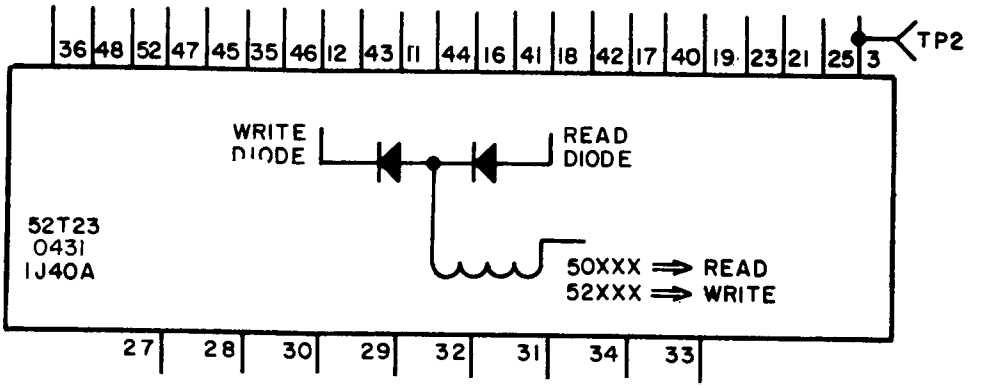


Figure 7-76. Logic Symbol of One Circuit on 7500431 Module

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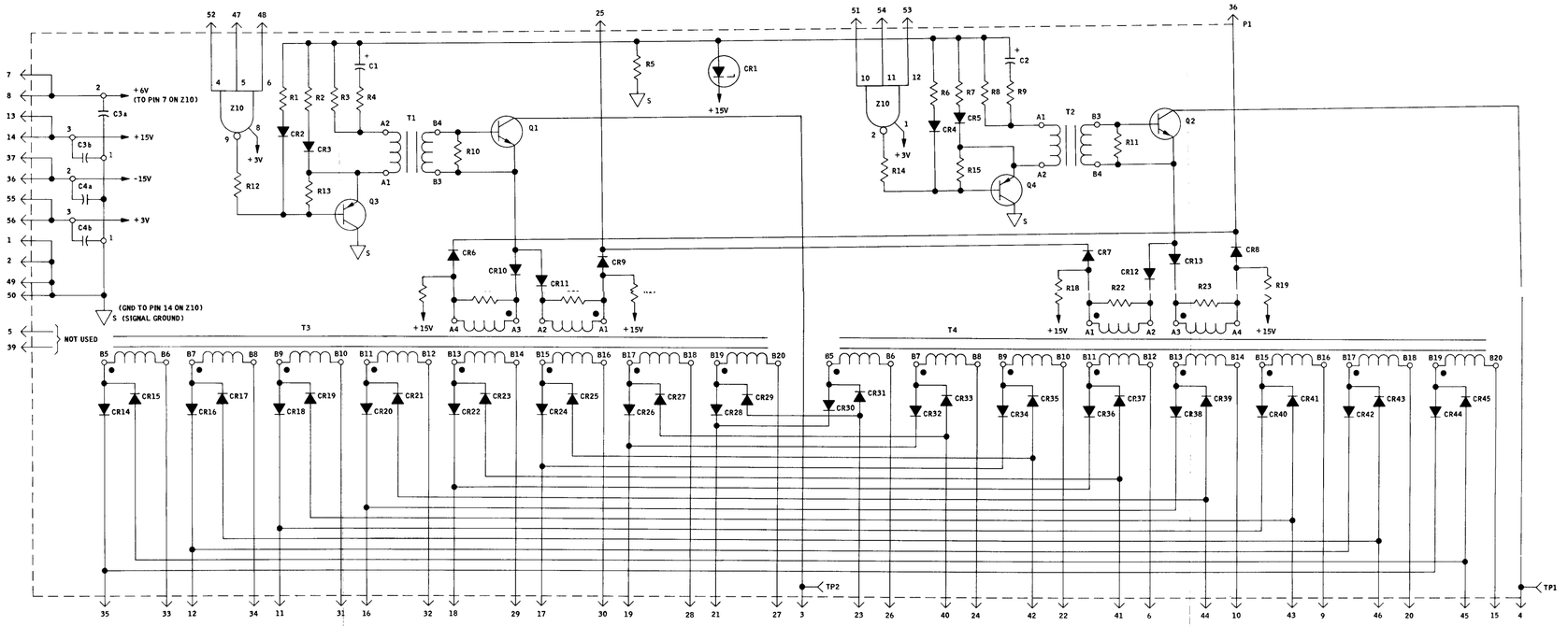
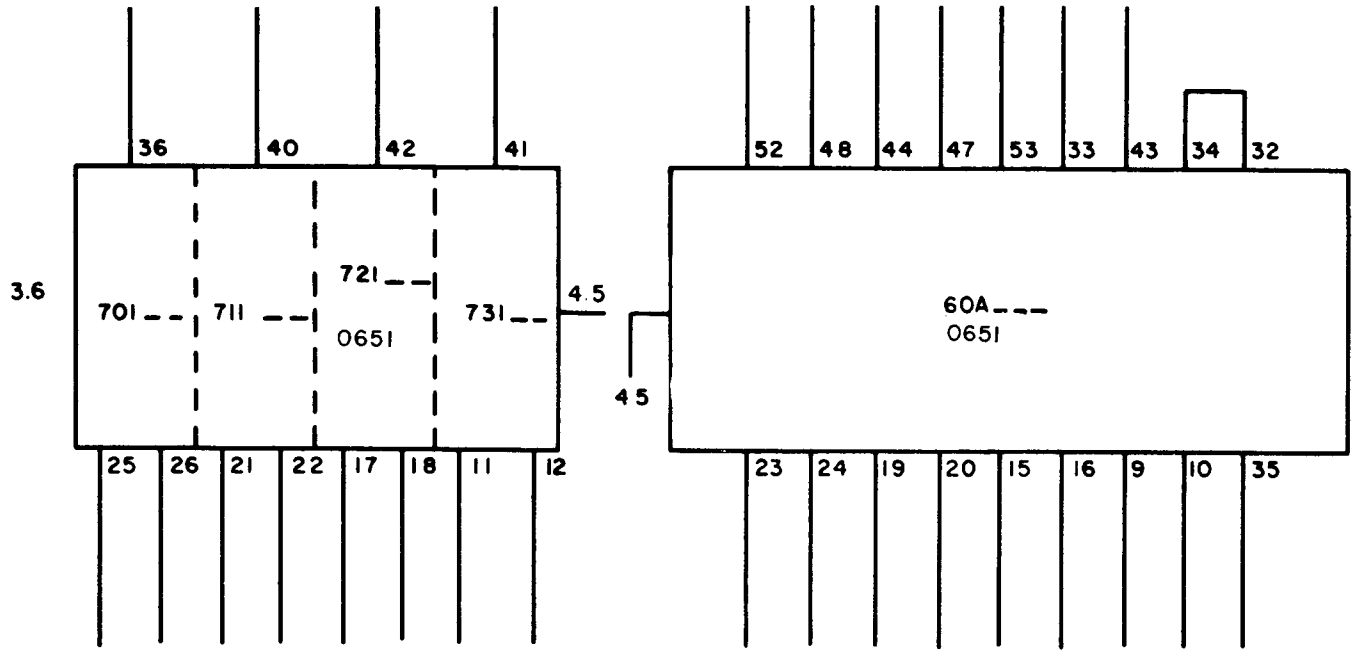


Figure 7-77. Module 7500431 Schematic Diagram



CONDENSED LOGIC DIAGRAM

Figure 7-78. Logic Symbol of Sense and Inhibit Amplifier on 7500651 Module

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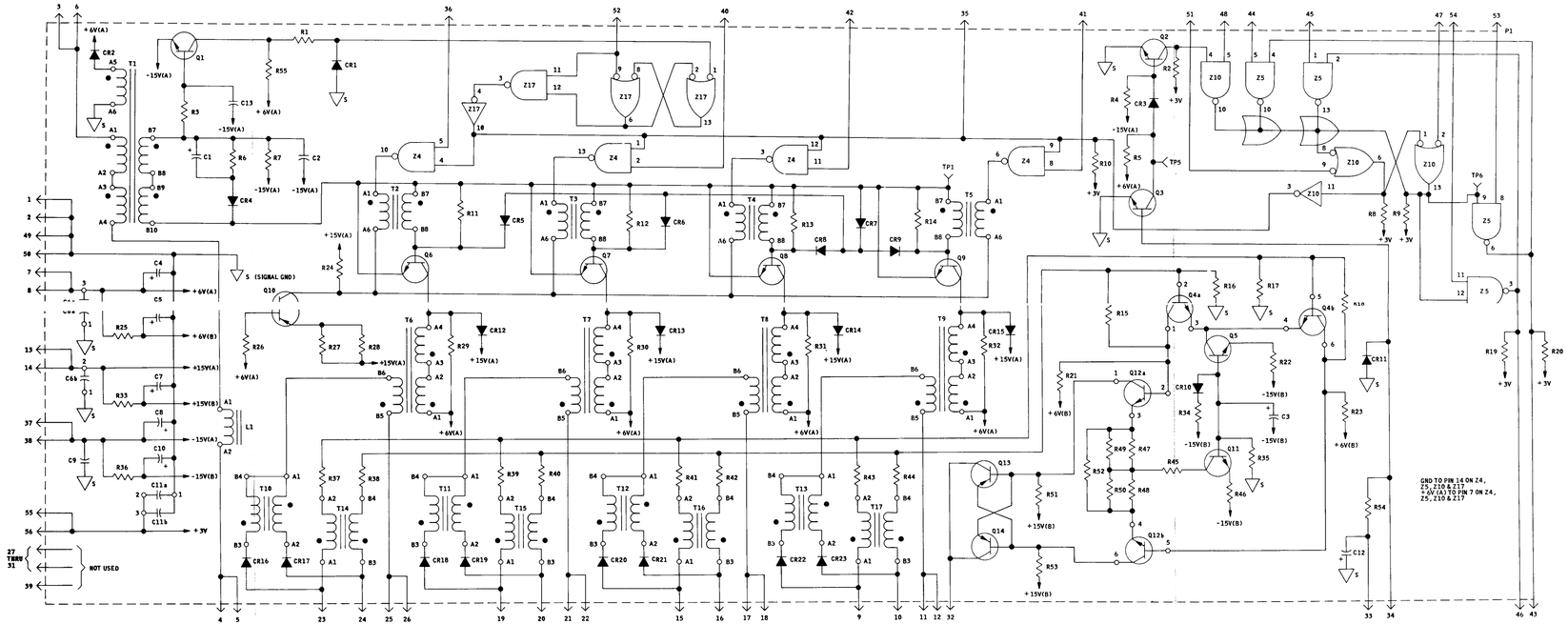

Figure 7-79. Module 7500651 Schematic Diagram

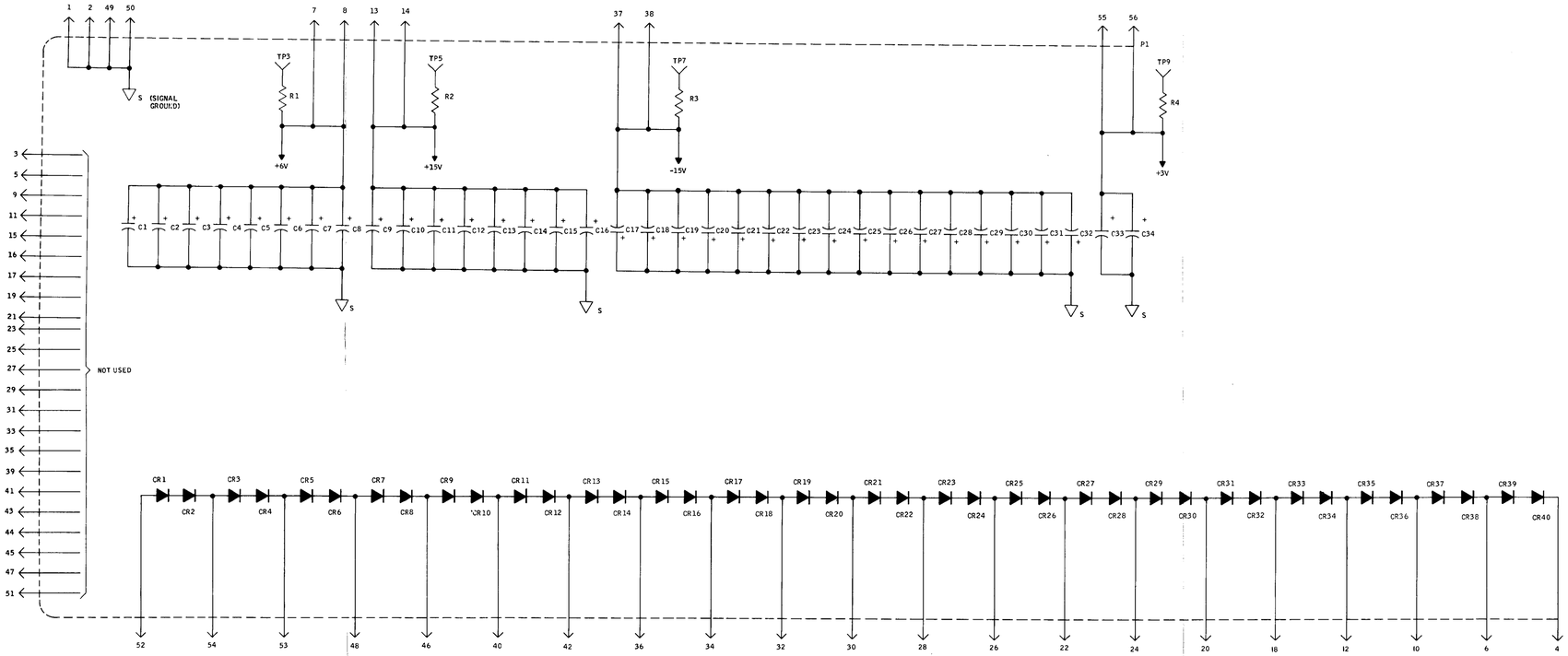

Figure 7-80. Capacitor-Diode Assembly, 7500660

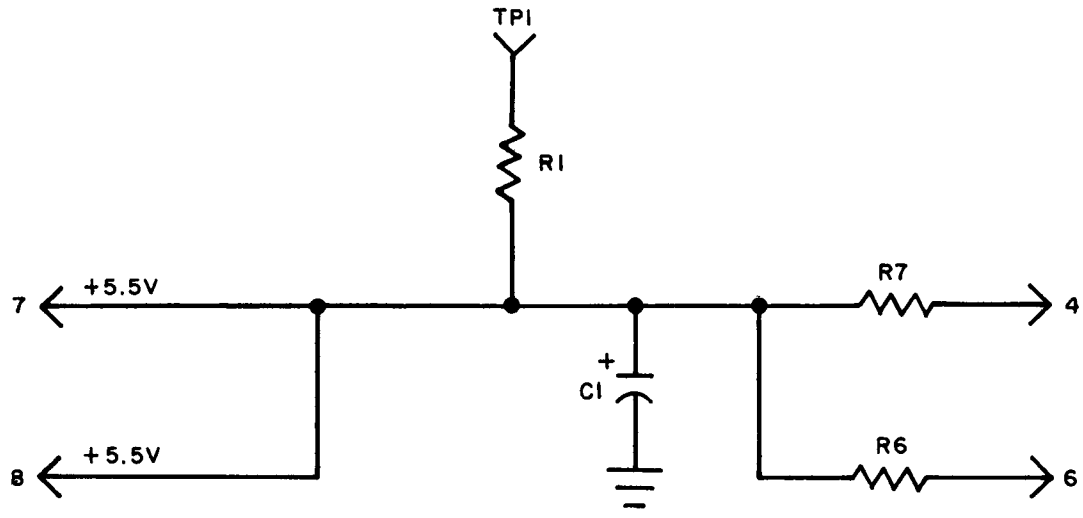

Figure 7-81. Capacitor Assembly Module 7500671, Schematic Diagram

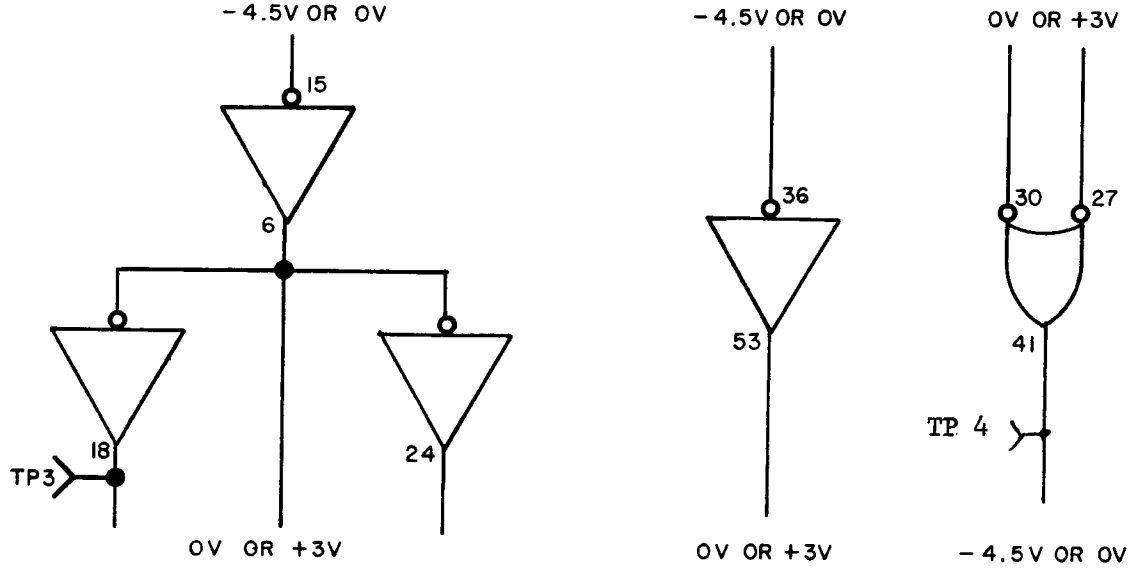

Figure 7-82. Logic Symbol of Level Changer Amplifier, Module 7500761

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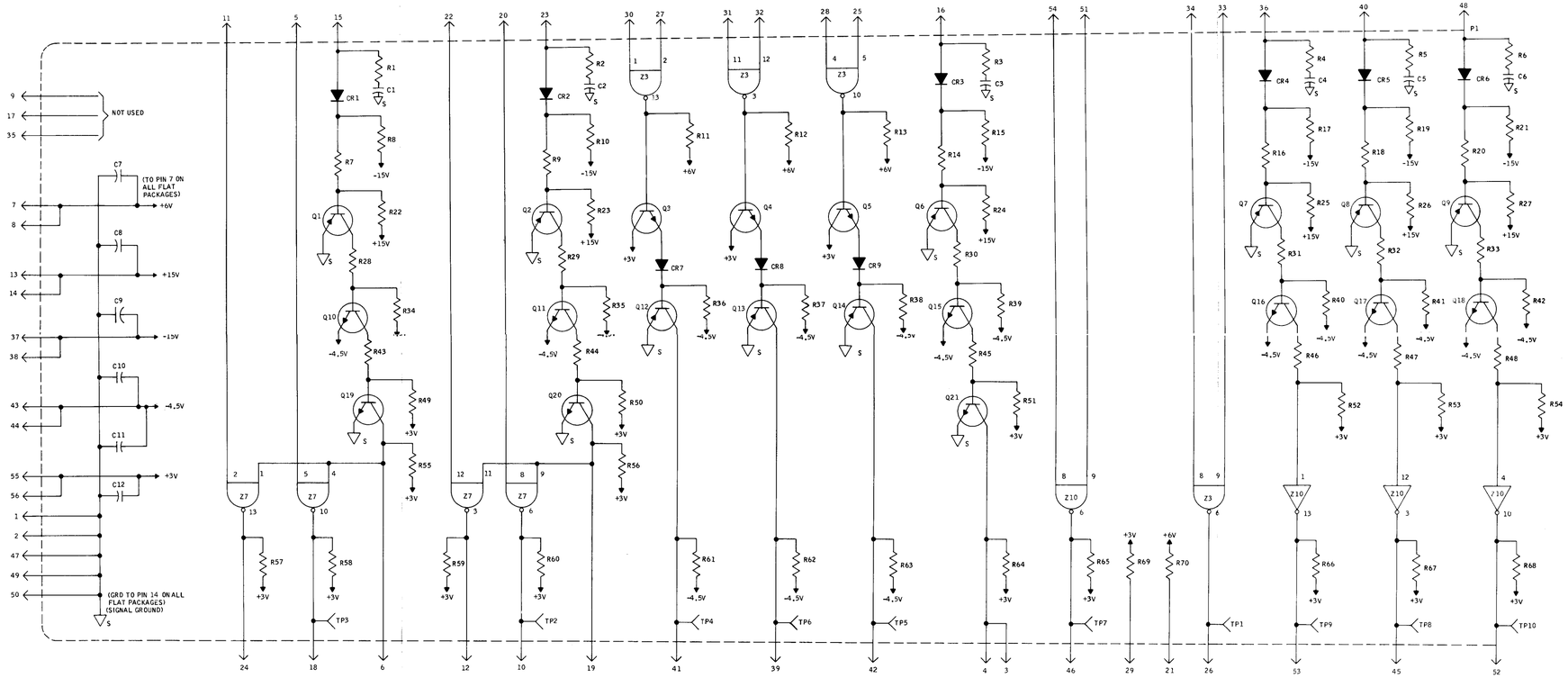

Figure 7-83. Module 7500761 Schematic Diagram

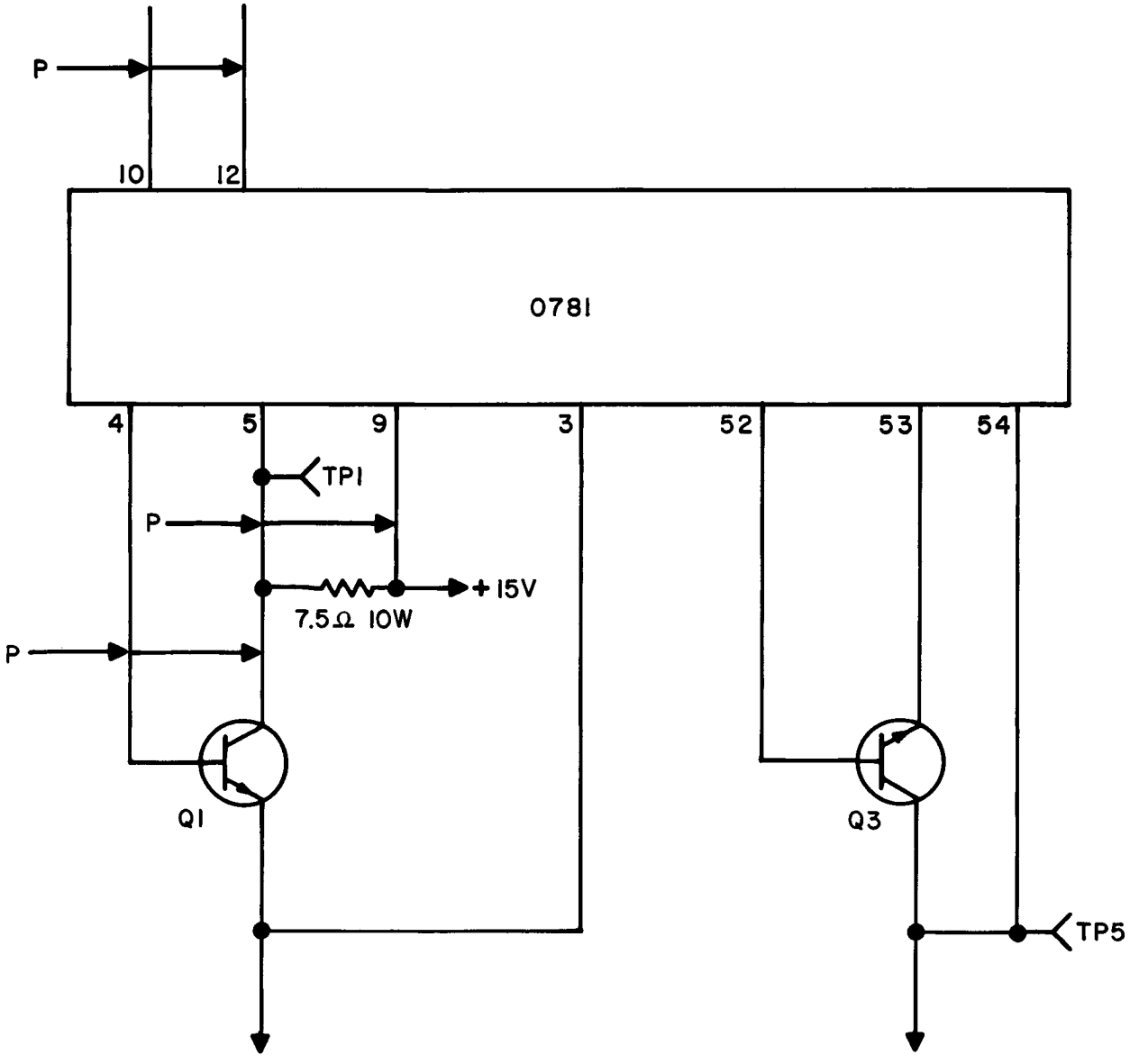

Figure 7-84. Logic Symbol of 7500781 Module

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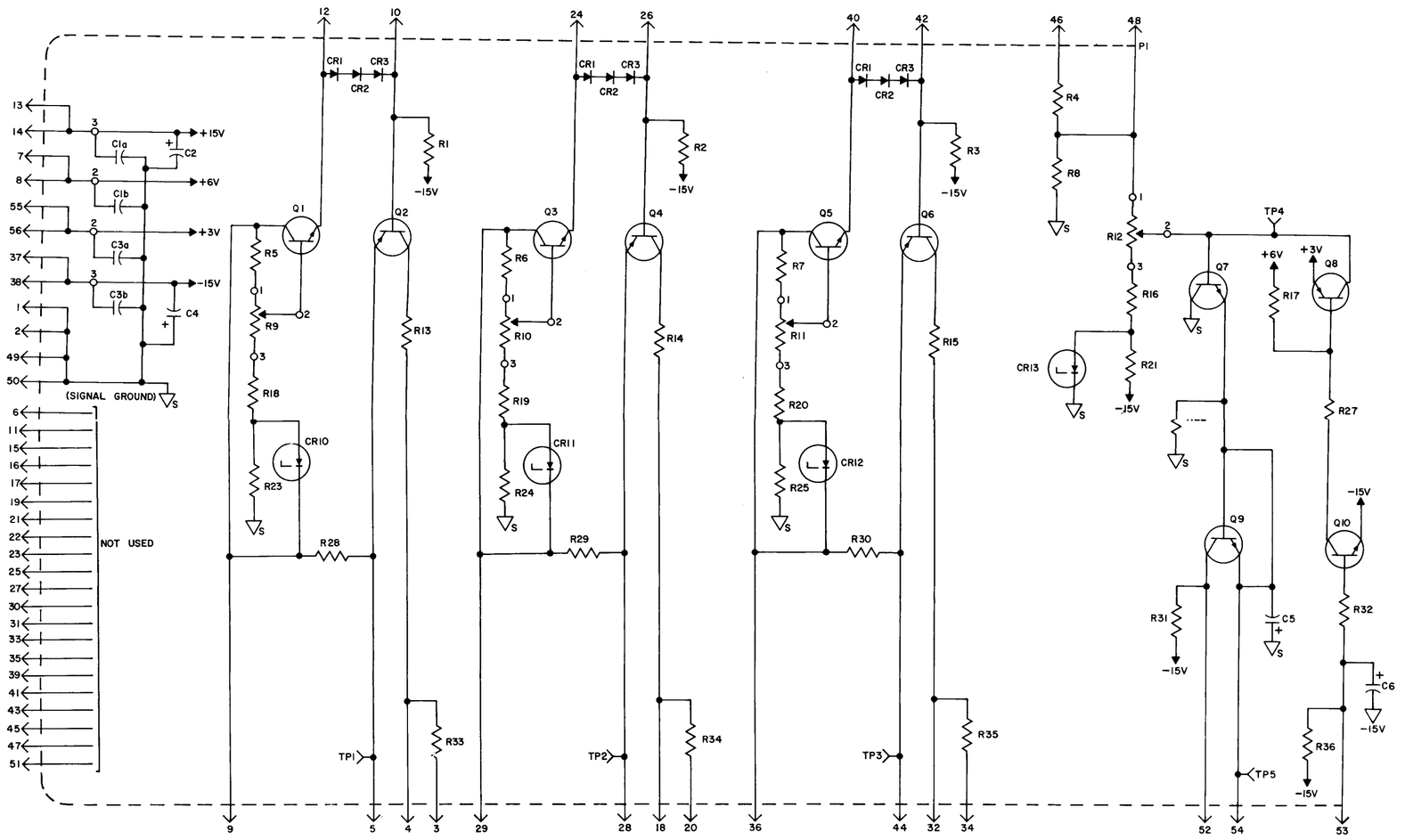

Figure 7-85. Module 7500781, Schematic Diagram

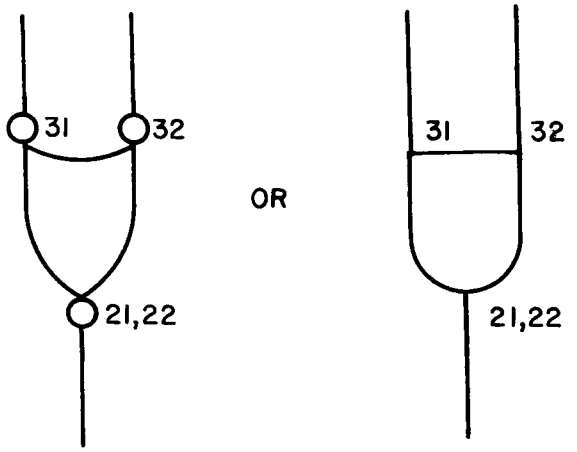

Figure 7-86. Logic Symbol of Noninverting Amplifier Driver, Module 7500900

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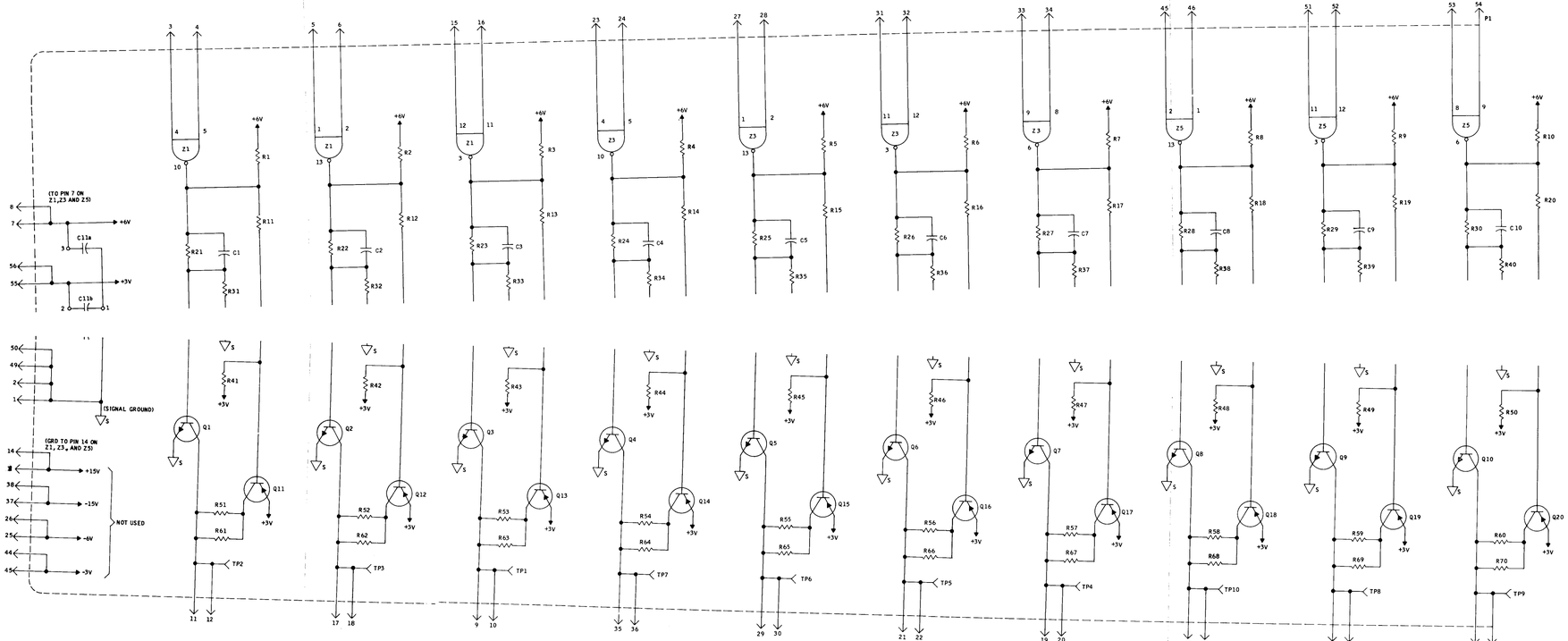

Figure 7-87. Amplifier, Driver-Logic, Noninverting, Module 7500900

GLOSSARY

DIGITAL COMPUTER TERMINOLOGY. Many terms which have an accepted meaning in the English language have a specific meaning when applied to computer operation and circuitry. This glossary is intended to delineate these terms and their specific meanings as they are written in this manual.

ABORT - A condition within the computer which results in the following sequential instruction being skipped or omitted.

ACCESS TIME - The time interval, characteristic of a memory or storage device, which exists between the instant information is requested and the instant this information is available to requesting circuitry.

ACCUMULATOR - A 36-bit addressable register, consisting of two 18-bit registers, AL and AU, used in arithmetic processes and commonly labeled the A register. A register is the principal arithmetic register and is used to hold sum, difference, product, or remainder during the final steps of arithmetic functions.

ACKNOWLEDGE - Indication of acceptance or issuance by the computer of signals on input or output lines to peripheral equipment. Abbreviated as ACK.

ADDER - A device which forms as an output the sum of two or more numbers presented as inputs. Related to the accumulator.

ADDRESS - A coded number specifically designating a computer register or a location within an internal storage device. Stored information is referenced by its address.

ADDRESSABLE - Capable of being referenced or entered by an address or instruction.

AND - A signal circuit with two or more input lines in which the output line supplies the desired signal only when all inputs are coincident signals. Synonomous with an AND gate and AND circuit.

ARITHMETIC - A section within the computer where arithmetic processes are performed and operands or results are temporarily stored.

AUXILIARY ROUTINE - A routine designed to assist in operation of the computer and in debugging other routines.

BINARY - A characteristic, property, or condition in which there are but two possible alternatives.

BINARY ARITHMETIC - A numbering system which uses two as its base and only the digits one and zero are recognized.

BINARY CELL - An information - storing element capable of two possible stable states.

BINARY NUMBER - A single digit or group of characters or symbols representing the total, aggregate, or amount of units by utilizing base two. Using the digits 1 and 0

to represent a quantity.

BINARY POINT - The radix point or root of the binary system.

BISTABLE - The capability of assuming either of two stable states; hence, capable of storing one bit of information.

BIT - An abbreviation of binary digit. A single character in a binary number representing the condition of a stage of storage within a computer. A unit of information capacity of a storage device.

BOOTSTRAP - A technique for loading the first group of instructions of a routine into storage; then using these instructions to load the remainder of the routine.

BOOTSTRAP MEMORY - A permanently wired, nondestructive readout memory containing the load routine for loading programs into storage. The program stored in nondestructive readout memory.

BORROW - An arithmetically negative carry; the additional subtraction of a one from the next partial difference. A borrow occurs in direct subtraction by raising the low order digit of the minuend by one unit of the next higher digit. A borrow occurs in binary subtraction when a digit of the minuend is a zero and the corresponding digit of the subtrahend is a one.

BUFFER - Transfer of data between the computer and peripheral equipments; intermediary storage between two data handling systems having different access times or formats.

BUFFER REGISTER - Final holding register for computer output to external devices or initial holding register for input to the computer; normally referred to as the C registers.

CAPACITY - Maximum size of a number that can be processed in the storage locations of a computer.

CARRY - A condition which arises in addition when the sum of two digits in the same digit place equals or exceeds the base of the number system in use; a digit to be added to the next digit column; the process of forwarding the carry digit.

CHASSIS - A divisional unit of the computer containing plug-in circuit cards and/or memory devices and the necessary wiring and test points for maintenance, assembly, and repair.

CHECKSUM - Sum used in a summation check.

CLEAR - To erase the contents of a storage device by replacing the contents with blanks or zeros. To reset a storage or memory device to the zero state. The signal used to perform the clear function such as master clear.

CLOCK - Basic timing or master timing device used to provide the basic sequencing pulses for the operation of the computer.

CODE - A system of symbols for meaningful communication; a machine language program.

CODED PROGRAM - Procedure for solving a given problem through use of computer logic. The coded program may vary in detail from a simple outline of the procedure to be followed to an explicit list of coded instructions.

COMPARE - To examine the representation of a quantity to discover its relationship to zero. To examine two quantities for the purpose of discovering identity or relative magnitude.

COMPILER LANGUAGE - A set of symbols used to abbreviate computer instructions and functions.

COMPLEMENT - A quantity expressed to the base N which is derived from a given quantity by a particular rule; frequently used to represent the negative of a given quantity. A complement on N, obtained by subtracting each digit of the given quantity from N-1, adding unity to the least-significant digit, and performing all resultant carrys. For example, the one's complement of 100011 is 011100; the nine's complement of 456 is 543.

CONTROL - Circuits within the computer which effect the completion of a function in the prepared sequence; the proper interpretation of an instruction and the issuance of proper commands to sequentially command computer logic to final completion of this interpretation.

CONTROL MEMORY - A storage device with assigned address locations used to hold information for control of computer logic operations.

COUNTER - A device capable of increasing or decreasing the value of its content upon receipt of coded input signals.

DEBUG - To isolate and remove all malfunctions from computer circuitry; to correct mistakes in a computer program or routine.

DIGIT - One of a set of numerical characters used as coefficients of powers of the radix in the positional notation of numbers.

ENABLE - (noun) A signal or pulse which allows other conditions to be acted upon; (verb) to apply the signal, to provide an enable signal.

EXECUTE - To perform indicated operations on specified operands.

FAULT - A condition which arises from the application of an illegal or improper signal; resulting from the detection of an improper or illegal condition.

FIXED POINT ARITHMETIC - A type of arithmetic in which operands and results of all arithmetic operations must be properly scaled so as to have a magnitude between certain fixed values. A method of calculation in which operations occur in an invariant manner and in which the computer does not consider the location of the radix point.

FLOW DIAGRAM - A graphical presentation of a sequence of events or operations; a flow chart.

FLOATING POINT ARITHMETIC - A form of number presentation in which quantities are represented by one number, the mantissa; multiplied by a power of the number base, the characteristic. A method of calculation which automatically accounts for location of the radix point.

FUNCTION CODE - That portion of the instruction word which specifies to the controlling logic the particular operation to be performed.

GATE - A circuit, which yields an output signal, that is dependent upon some function of its past or present input signals; AND gate or OR gate.

HALF-SUBTRACT - The bit-by-bit subtraction of two binary numbers with no regard for borrows, abbreviated HS. The complement for half-subtract is "half-subtract not" which is abbreviated HS.

HARDWARE - The physical equipments or devices that comprise a computer and its associated peripheral units; contrasted with software.

HOLD - The function of retaining information in a storage device after this information has been transferred to another device; contrasted with clear.

INDEX REGISTER - A register which contains a quantity that may be used for address or operand modification; sometimes referred to as B register or B box. One of seven registers contained in control memory and used for operand and address modification during specific instructions.

INFORMATION - A collection of facts or other data as derived from the processing of data.

INPUT - Information or data transferred from, or to be transferred from, a peripheral device to internal storage of the computer. To transfer data or information into the computer.

INPUT/OUTPUT - A section within the computer which provides a method of communication with peripheral equipments, abbreviated I/O.

INPUT/OUTPUT REGISTERS - Registers within the computer that are used for the storage of information to be transferred from or transferred to the computer.

INSTRUCTION - A set of characters which defines an operation to be performed by the computer and contains the required addresses, operands, and other necessary information; same as instruction word.

INSTRUCTION DESIGNATORS - Those parts which constitute an instruction word and represented by the letters f, m, k, and y. The letter f designates format or function code; m, minor function code when applicable; k, modification designator; and y, operand address.

INSTRUCTION REPERTORY - The set of instructions which a computing system or data processing system is capable of performing.

INTERFACE - A common boundary between automatic data processing systems or between parts of a single system.

INTERNAL STORAGE - Storage facilities forming an integral physical part of the computer from which instructions and operands may be processed.

INTERRUPT - 1) Internal; an internally generated signal which indicates termination of an input or output buffer or acceptance of an external interrupt. 2) External; a signal from an external device which indicates an unusual condition which requires computer attention.

JUMP - An instruction or signal which, conditionally or unconditionally, specifies the location of the next sequential instruction and directs the computer to that instruction; used to alter the normal sequential control of the computer.

LEAST-SIGNIFICANT DIGIT - The first digit of a number counter from the right; the lowest-order digit of a number.

LOAD - To enter information into the storage area of a computer; to insert information into a register; to insert a program into a computer.

LOGIC - The systematic scheme which defines interactions of signals in the design of an automatic data processing system.

LOGICAL PRODUCT - Bit-by-bit multiplication of two binary numbers.

LOGICAL SUM - Bit-by-bit addition of two binary numbers with no regard for carrys; abbreviated LS. The complement of the logical sum is the "logical sum not", abbreviated $\overline{\text{LS}}$.

MAIN MEMORY - Core storage area of the computer used for normal word or program storage. That area of the computer used for instruction storage and for addressable operands.

MALFUNCTION - A failure in the operation of the hardware of a computer; failure or casualty in an equipment which degrades its operation or causes equipment to become inoperative.

MASK - A machine word that specifies which parts of another machine words are to be operated upon.

MASKING - The process of extracting a nonword group or a field of characters from a word or string of words.

MASTER CLEAR - To clear all normal storage locations of a computer prior to an operation. To set all major flip-flops to store a zero.

MASTER CLOCK - Primary timing signals within a computer. The source of primary timing signals.

MEMORY - A device into which information may be introduced, retained, and extracted for use at a later time.

MODE - A computer system of data presentation. A selected type of computer operation such as read or write mode.

MODIFY - To alter a portion of an instruction so its interpretation and execution will be other than normal. To alter a subroutine according to a defined parameter.

MODULE - An interchangeable plug-in item containing components. A printed circuit card upon which are mounted the electronic components.

MODULUS - The maximum quantity of permissible numbers that may be used in a process or system. The modulus for the group of numbers from -15 to +15 is 31.

MOST-SIGNIFICANT DIGIT - From left, the first digit of a number other than zero; the highest-order digit of a number.

NONADDRESSABLE - Pertaining to a storage location incapable of being referenced by an instruction word.

NONDESTRUCTIVE READOUT - A memory device that stores information which has been preset at manufacturer and cannot be changed or altered; reading information from a memory device that does not destroy the contents of the device; a reading of information

from a register without changing that information within the register.

NONVOLATILE STORAGE - Storage mediums such as magnetic tapes, drums, cores, and discs, which retain information in the absence of power, and may be made available upon restoration of that power.

NUMBER - The total, aggregate, or amount of units; a figure or word, or a group of figures or words used to graphically represent an arithmetic sum or total.

OCTAL NUMBERS - A numbering system using eight symbols, 0 through 7, as its base; numbers in which the base has been set at eight.

OPERAND - A quantity entering or arising in an instruction; an argument, result, parameter, or indication of the location of the next instruction; the address portion of an instruction.

OPERATION - A defined action; action specified by a single computer instruction or group of instructions.

OPERATOR - A mathematical symbol which represents an arithmetic process to be performed upon an operand. One who operates the computer.

OUTPUT - A transfer of information from the internal storage system of the computer to peripheral devices or external storage; the process of an information transfer from the computer.

OVERFLOW - The condition that arises when the result of an arithmetic operation exceeds the capacity of the alloted storage area; overcapacity; information contained in an item which is in excess of a given or stated amount.

PAPER TAPE READER - A device capable of sensing information punched on a paper tape in the form of a series of holes. A photoelectric readout device, abbreviated PT Reader.

PARALLEL - To handle simultaneously in separate facilities; to operate on two or more parts of a word or item simultaneously; contrasted with serial.

PARALLEL TRANSFER - To transfer characters of a word simultaneously over separate lines.

PARTIAL CARRY - Execution of the carry process in which carrys that arise as a result of a carry are not transmitted to the next higher stage.

PARITY BIT - A bit, normally a one, that may be added to a word to insure the total number of ones in that word is odd.

PARITY CHECK - The process of checking the number of ones contained in a given word or group of words or instructions.

PASS - A complete cycle of reading, processing, and writing. A complete machine operation or run.

PERIPHERAL EQUIPMENT - Auxiliary machines placed under control of the central computer. Equipments used by, and in conjunction with, the main computer system.

POSITIONAL NOTATION - A method of expressing a quantity, using two or more figures wherein the successive right to left figures are interpreted as coefficients of

ascending integer powers of the radix.

PRECISION - The degree of exactness with which a quantity is stated; the degree of discrimination or detail.

PRESET - To set contents of a storage location to an initial value.

PROGRAM - A complete sequence of machine instructions, routines, and operands necessary to solve a problem.

RADIX - The number of individual characters used in a numbering system; radix for the decimal system is ten; radix for the octal system is eight; radix for binary system is two.

RADIX POINT - The period that separates the integer digits from the fractional digits of a number of the digital position involving the zero exponent of the radix from the digital position involving the minus-one exponent of the radix. The decimal point for the decimal system; the octal point for the octal system; or the binary point for the binary system.

RANDOM ACCESS - Pertaining to the process of obtaining information from or placing information into storage where the time required for such access is independent of the location of the information most recently obtained or placed in storage.

READ - To sense information; to extract information, usually from a memory location.

READER, CARD - A device capable of recognizing information in the form of holes punched in a card.

READER, MAGNETIC TAPE - A device capable of reading information recorded on magnetic tape in the form of magnetized dots.

READER, PAPER TAPE - (See paper tape reader).

REAL TIME - A measurement of elapsed time relative to a specific time or event.

REAL-TIME CLOCK - An oscillator and the associated circuitry capable of recording elapsed time measured in minutes, seconds, milliseconds, or other fractions of actual time periods.

REGISTER - A number of bistable stages used for holding or storing information. The number of stages determines the modulus of the number system which may be represented by the computing system; an addressable storage location. (See definition of accumulator, buffer register, index register, input/output register).

REPERTOIRE - Instructions or functions capable of being executed by the computer; repertoire of instruction (see definition of instruction repertory).

RESET - To clear; to set to zero; to return a device to zero or to an initial or arbitrarily selected value.

RESUME - The input acknowledge signal generated by a receiving computer upon completion of sampling input information lines.

RISE TIME - Time required for the leading edge of a generated or transmitted pulse to rise from one-tenth to nine-tenths of its final or terminal value. Rise time is proportional to the time constant of the circuit.

ROUTINE - A set of coded instructions

arranged in proper sequence to direct the computer to perform a desired operation or sequence of operations. Subdivision of a program consisting of two or more functionally related instructions.

SCALE - To shift a binary number either right or left in a register to retain the number for future computations or for later storage within the computer.

SCALE FACTOR - Coefficients used to multiply or divide quantities in a problem so they fall within a given range of magnitude such as from +1 to -1.

SCAN - A cycle or sequence which routinely interrogates all requests and interrupts; to determine priority for real-time clock; input and output on a basis of channel number and type of request.

SENSE - To examine relative to a criterion; to read information from magnetic cores.

SEQUENCE - An orderly progression of items of information or of operations in accordance with set rules.

SERIAL - One at a time; pertaining to time-sequential transmission.

SERIAL TRANSFER - To transfer words of information or bits of a word in a serial manner; to transmit bits of a word or elements of information in succession over a single line; contrasted with parallel transfer.

SET - To place a binary cell or flip-flop in the state of storing a one; to change the state of a storage device to output a value other than zero.

SHIFT - To move characters of a unit of information columnwise left or right; to multiply or divide a number by a power of the base of notation; to move information left or right in the arithmetic section of a computer.

SHIFT REGISTER - A computer register in which the contents may be shifted either left or right.

SIGN - A symbol that distinguishes negative quantities from positive quantities.

SIGN BIT - Sign digit; bit used to designate the algebraic sign of a number.

SIGNIFICANT DIGITS - A set of digits from consecutive columns beginning with the most-significant digit other than zero and ending with the least-significant digit whose value is known and considered relevant.

SINGLE ADDRESS CODE - Consisting of instructions containing a coded representation of the operation to be performed and a single address of a word in storage or an operand. The instructions of the single address code contain a maximum of one address for reference in storage.

SOFTWARE - The totality of programs and routines used to extend capabilities of computers; programs and routines such as compilers, assemblers, narrators, routines, and subroutines.

STORAGE - Pertaining to a device in which information may be placed and retained for future use; synonymous with memory.

SUBROUTINE - A set of instructions necessary to direct the computer to perform a well defined mathematical or logical operation; a subunit of a routine such as multiply

or divide subroutine.

TAG - A unit of identification whose composition differs from that of the other members of a set so that it can be used as a marker or label.

TRANSFER - Conveyance of control from one mode to another by means of instructions or signals; conveyance of data from one place to another.

TRANSLATE - To change information from one form of representation to another without significantly affecting the meaning; to transform.

TROUBLESHOOT - To search for the cause of a malfunction or erroneous program behavior to isolate and correct the malfunction or error.

VOLATILE STORAGE - A storage device in which the stored information is lost in the event of a power loss or shutdown; such as a flip-flop register.

WIRED PROGRAM - A program permanently wired into storage; see definition of bootstrap memory.

WORD - An ordered set of characters that occupies one storage location and is treated by the computer circuitry as a unit. A word is normally treated as an instruction by the control section and as a quantity by the arithmetic section. Normal word length for the computer is 18 bits.

WRITE - To record data in a register, location, or other storage medium or device; to introduce information into some form of storage.

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