Introduction to integrated semiconductor circuits

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To my mother and father

Preface

This book is intended to serve as an introductory guide for technical and management people in the electronics industry who are on the threshold of becoming involved in the new and fascinating field of Integrated Circuits. Its main purpose is to assist the engineer (and the technician, too) at the working level. The problems faced by these people closely parallel those encountered a decade or so ago, when transistors first made their tremendous impact on the electronics industry. It is assumed that the reader is generally acquainted with semiconductors but is not necessarily an experienced designer of circuits using semiconductor devices. Of course, the reader with circuit-design experience will be better equipped to appreciate the problems associated with Integrated Circuits. Current literature abounds with excellent articles and reports in this field, but the engineer who might soon be called upon to actively design circuits and equipment utilizing some of these newer devices and techniques will undoubtedly be hard-pressed for time. This book is aimed at his immediate needs and I hope he will find it a convenient source book and a suitable starting point for this new phase in his engineering work. Most of the material presented here has been reported before, scattered in technical journals, magazines, conference proceedings, internal memos, and trip reports. While not intended for people who have been actively working in this field for some time, enough material on the present state-of-the-art is included to make it a handy reference for those in this category, too.

Integrated Circuits—the new frontier of electronics—have come of age. While the field is new and a myriad of problems still remain to be solved, the advances made, to date, give ample reasons for optimism. Several equipment manufacturers are initiating programs incorporating integrated circuits, not only in their special products but also in their future standard product lines.

The broad acceptance and general application of integrated circuits is confirmed by such developments as:

- A microelectronic digital computer with capacity sufficient for ballistic missile explicit guidance has been developed by UNIVAC

(a division of Sperry Rand). This system, which weighs less than 17 pounds and occupies a volume less than 0.2 cubic feet including input-output and digital-to-analog conversion circuitry, is approximately 80% smaller than conventional designs of comparable capacity. The computer, designated the UNIVAC 1816, uses 1243 integrated semiconductor circuits and has a magnetic thin-film memory which can be programmed electrically with nondestructive read-out of stored data.

- An AIRBORNE Loran-C receiver using digital integrated circuits, which has been developed by the Sperry Gyroscope Company, is expected to provide position fixes accurate to within a few hundred feet almost anywhere over the Northern Hemisphere. The 19-pound AN/ARN-76 receiver occupies 0.47 cubic feet and is approximately 75% smaller in size and weight than a design using standard solid-state elements. It contains more than 25,000 components and is one of the first complete electronic subsystems designed specifically for integrated circuits.
- A multipurpose computer control system has been developed by Martin-Denver for prelaunch and space booster checkout. About 2000 integrated circuits are utilized in this system, which is designated as MARTAC (Martin Automatic Rapid Test and Control). The principal objective of integration, here, is cost reduction and increased reliability, rather than the more obvious inducements of size and weight reductions.

While cost is still one of the major considerations, present indications show that integrated circuits will be cost-competitive in the near future. Engineers and engineering managers involved in proposal-writing and planning new products are constantly under pressure to make decisions regarding the pros and cons of going the way of integrated circuits. Choices of various circuit types, off-the-shelf units versus custom-made circuits, vendors' present and future production capabilities, status of deliveries, expected reliability, choices between fully, partially, or hybrid integrated units, and cost projections are some of the typical considerations confronting these people. Perhaps the problem can be best exemplified by a question recently asked by an engineering manager: "Integrated circuits are fine, I'm sold on them, but can we afford them?" I sincerely hope that engineers and managers faced with these and similar problems will find answers to some of their questions in this book.

To assist the reader who may not want to read the book in sequence, the chapters are grouped in five sections, each section

covering a specific phase of the field. The first section is general and contains two chapters intended to provide the background information. Chapter 1 traces the evolution of the "Micro" concept and goes back to the Second World War to acquaint the reader with the reasons for this trend in electronics. Chapter 2 discusses some of the systems considerations associated with microsystems and the problems introduced by this technology, which integrates the traditionally separate functions of the materials, components, circuits, and systems engineers.

The second section deals with the techniques and processes involved in the functioning and the fabrication of the integrated circuits. The integrated circuit in its two fundamental forms is based on the semiconductor or the thin-film technologies, or suitable combinations of both. Chapter 3 gives a brief description of the fundamental semiconductor processes, and Chapter 4 gives the basic thin-film processes involved. Chapter 5 is essentially a word-picture of a guided tour through a typical semiconductor facility engaged in the fabrication of integrated circuits. A better understanding of the characteristics of the integrated circuits and their limitations can be obtained by a realization and an appreciation of the fabrication steps.

The third section contains the meat of the book. Various aspects of the fully integrated circuit are presented. Chapter 6 introduces the reader to the integrated circuit elements and some of the characteristics peculiar to them. Designing circuits for integrated fabrication presents some rather unique and unconventional problems. These are discussed in Chapter 7, along with a typical circuit design example, which is intended to illustrate some of the problems discussed in this chapter. Since the user of integrated circuits is continually faced with the problem of special circuits for his own particular requirements, which are not available as standard product line items, several vendors have suggested certain procedures for designing custom circuits. These are discussed in Chapter 8. The material presented in Chapters 6, 7, and 8 is intended to be used as guidelines and is based on the presently available information. These guidelines are mostly general and are applicable to most present-day vendors within reasonable limits. As the technology advances, they will undoubtedly change.

The bulk of the market for integrated circuits right now is in the digital field—largely in computing systems. It is therefore quite understandable that the vendors are actively pushing digital circuits for their standard product lines. For the engineer or the technician

who is not intimately acquainted with the various forms of transistor logic circuits, Chapter 9 provides a brief introduction. For the reader who is well acquainted with transistor logic circuits, I hope that this chapter will come in handy as a guide for occasional reference. Included in this chapter are the comparatively recent transistor-transistor-logic (TTL), the emitter-coupled-transistor-logic (ECTL), and the load-compensated diode-transistor-logic (LCDTL) circuits.

At the present time, the fully integrated circuit has several limitations, which may be serious handicaps in some applications. The fourth section presents some of the alternate schemes that are possible. The partially integrated circuit, or the chip approach as it is commonly called, offers an interim solution to some of these limitations, along with several advantages of its own. This approach is described in Chapter 10. Thin-film techniques widen the scope still further, with some unique characteristics and advantages, when used in conjunction with semiconductor active devices. This hybrid-integration approach is described in Chapter 11.

The fifth section contains several associated topics. One of the problems in this new field relates to the form factor of the container of these circuits, and the bonding of leads to the integrated circuits. These subjects are covered in Chapter 12, which also includes a description of the thermocompression bonding process.

Integrated circuits present some unique problems as far as testing and maintainability are concerned. These topics, along with reliability, are discussed in Chapter 13. This field is advancing at such a rapid pace that it is virtually impossible to include all the latest developments in a book like this. Nonetheless, an attempt is made to include some of the most significant new developments in Chapter 14, which also includes a section on price projections.

The Appendixes contain a condensed catalog of the circuits offered as standard product lines by several vendors at this time. It is realized that the vendors included do not make up a complete roster of companies engaged in this field. I attempted to include most of the vendors' lines which had readily available information at the time of this writing. This book concludes with a bibliography of literature in this field. This list is compiled from my personal file and is not the result of a detailed literature search. The categorizations are my own, intended for convenience in filing, thus several articles could have been classified under more than one heading.

This book is definitely oriented from the users' point of view and not from the manufacturers' viewpoint. It is my opinion that excellent books will soon be forthcoming, authored by engineers and

scientists actively engaged in the development and manufacture of these devices, which will present the problems and solutions from the vendors' point of view. If this book makes the transition from conventional to integrated circuitry a little smoother and easier for the equipment manufacturers' engineering personnel, it will have served its purpose.

I would like to thank several of my colleagues at UNIVAC (St. Paul) who helped me during the writing of this book, particularly Frank W. Kline and William J. Rydrych, for supplying some of the information, reading the rough draft, and making valuable suggestions relating to content and coverage of the book. I would also like to acknowledge Mrs. Teresa Tisthammer for retyping some of the revised portions of the book. Finally, I owe special thanks to my wife, Ruth, for her patience, and particularly for struggling with the original manuscript and transcribing it into an intelligible typed form.

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section 1

General information

Introduction— a historical review of microminiaturization

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The 1950's can best be described as the decade of the transistor. It was in the early 50's that the transistor emerged from a laboratory novelty to a matured component in its own right and seriously challenged the time-honored vacuum tube. The transistor was truly a revolution in the electronics industry, but it did not stop there. The advances made in semiconductor technology opened up new horizons, which are developing a further advanced technology—the integrated circuit. This new concept, which is an outcome of semiconductor development, is not only an evolution but also a revolution.

This new technology will undoubtedly revolutionize several existing concepts and thereby introduce some distasteful problems. It cuts across several engineering and scientific disciplines. Integrated circuits break down the traditional boundaries separating the functions of the components engineer, the circuits engineer, and the systems engineer and consolidate them to an extent which until now was not considered possible or even desirable. This revolution will perhaps present the industry with some of its most agonizing growing pains in this field.

1.1 DEMAND FOR MINIATURE ELECTRONICS

A natural question asked by many is, "why miniaturize electronic equipment?" To answer this question satisfactorily it is almost necessary to backtrack to the Second World War and trace its history from thereon. Broadly, the need for miniature and microminiature electronics can be categorized by military and nonmilitary needs in science and industry.

Military Needs

The Second World War imposed some stringent demands on the electronics industry. Military requirements put a constantly increasing pressure on the production of electronic equipment of smaller and lighter weight. This trend was mainly the outcome of the necessity to put more capability and higher performance in the then existing weapons and delivery vehicles. American industry met this challenge squarely by developing the miniature tube. Further demands for size

reduction were met by the subminiature tube and finally by the emergence of the transistor.

The immediate postwar years saw several problems created by these new developments. The subminiature tube and the transistor eased the demand for size and weight reduction. The termination of the war eased the pressure for higher performance. This resulted in a decrease of safety factors, which engineers normally incorporated in their designs. The inevitable outcome of this was a period of intolerable unreliability in electronic equipment. An increasing demand for reliability from the dissatisfied customer brought back the safety factors, which were earlier removed, and this produced larger equipment with reduced performance. Understandably, this met with blunt disapproval by the military, who were by then very much accustomed to miniaturized electronic equipment.

The cold war and the increasing emphasis on national defense, as well as interest in exploration of space, put a further demand on size reduction and increased performance. Today's space vehicles and satellites, while not necessarily requiring the ultimate in speed of operation, do demand a high degree of reliability for relatively long periods. On the other hand, manned aircraft as well as missile systems demand a much higher degree of performance, with increased speeds and reliability, which can only be fulfilled by complex electronic systems. Our nation's survival may well depend on the missile, which might be called upon to intercept and destroy hostile aircraft or intercontinental ballistic missiles, and which will require an absolute degree of reliability for a short period of time.

With the rise in demand for reliability of increasingly complex electronic equipment requiring enhanced performance, as well as size and weight reduction, cost becomes a very significant factor. For instance, the high cost of putting satellites into orbit may be justified, and partially offset, only if the system maintains minimum satisfactory performance over a prolonged period of time. "The ratio of payload weight to gross launch weight could be as small as one to one-thousand."[1] This means that the whole launch system could be fantastically expensive. Consequently, any reduction in the size and weight of the payload itself could result in a significant reduction of gross launch weight, and thus a substantial reduction in cost. This naturally places more pressure for microminiaturization of electronics.

The cost factor is further reflected in a different manner. Size reductions of components and subsystems make it increasingly difficult to use human operators during fabrication, thereby forcing the manufacturer into automation. Initially, automation would prove

rather costly, but the increase in reliability resulting from reduction, and possibly complete elimination later on, of human errors would certainly justify the cost. Eventually, it is conceivable that this may reach a point where the total cost of a complex system may even be less than what it would be if conventional components were used.

Nonmilitary Needs

While size, weight, reliability, and cost are sufficiently attractive reasons for miniaturization in nonmilitary applications, other incentives also exist. Space medicine is an expanding field, which presents some very challenging problems. Sensors attached to an astronaut's body for picking up reactions and responses in space environments must be small and light. Space limitations within a space vehicle impose severe restrictions on the size and weight of the equipment required for transmitting the data picked up by the sensors. Medical sciences, even in normal ground environments, have very special needs for miniaturized electronics. Diagnostic and later even corrective devices, which must be embedded in animals for experimental purposes (and later in human beings, too), obviously have very severe size and space limitations. Biological sciences will undoubtedly make good use of electronics if sufficiently miniaturized. For instance, the study of communication and navigational systems in small animals, and even insects, could be greatly facilitated if signals could be transmitted by microminiature transmitters attached to their bodies. Obviously the transmitting system must be small and light enough to ensure that it will not hamper the mobility of the subject under study.

Self-adaptive bionic systems will probably advance and reach a stage of real usefulness when miniaturization of electronics has advanced to a much greater degree. These systems, which will have synthesized neural networks, will certainly require a large amount of redundancy to meet near-perfect reliability. In space exploration, these systems will be fed large quantities of data from the various sensors. These data will have to be evaluated and analyzed, pertinent information will be sorted, and the required control signals generated and transmitted. All this must be accomplished in very short periods of time. Both the redundancy and speed requirements will only be satisfied by microminiaturization.

In the area of nonmilitary needs, the biggest spur to miniaturization will unquestionably be provided by the computer industry. In the field of commercial data processing, cost and reliability considerations will take precedence over size and weight. The latter two considerations will come as bonus by-products of miniaturization. Present

indications are that by 1964 the cost of integrated logic circuits, will not only be compatible with that of conventional component-printed circuit boards, but will be competitive as well. This will benefit both the computer manufacturer and the user. The manufacturer will be able to sell systems that will cost less to produce, with increased built-in reliability. Size reduction will make it possible to introduce higher computing speeds, larger computing capability, and more widespread use of redundancy, resulting in still greater reliability. Thus the computer user will undoubtedly benefit.

1.2 THE EVOLUTION OF "MICRO" CONCEPTS

Having established the various needs for microminiaturization, it is interesting to observe the evolution of the various concepts which have resulted in distinctly different approaches. For purposes of explanation they are divided into the following seven categories:

1. Miniaturization
2. Subminiaturization
3. Microminiaturization
4. Morphological integrated technology
5. Integration by thin-film technology
6. Integration utilizing semiconductor technology
7. Partial or hybrid integration by combination of thin-film and semiconductor technologies

The last three techniques are the ones that appear most promising for applications in the immediate future, particularly for the computer industry. For this reason this book is confined to these three approaches only. Nonetheless, we will briefly look into all seven approaches to get a coherent historical picture of the entire miniaturization phenomenon.

Miniaturization

The earliest real need for miniaturization was established during the Second World War. The first significant goal was reached when the miniature vacuum tube made its appearance, followed by the subminiature tube. As a result, pressure was put on manufacturers to reduce the sizes of other electronic components; smaller forms of conventional components were the outcome. Each component, however, retained its own discrete nature and its usual form and shape. Furthermore, the components were mounted in the usual manner, and conventional wiring and soldering were employed for assembling them

in circuits. The only advancement was the size reduction of the individual components.

Subminiaturization

Pressure for further size reduction resulted in still smaller individual components. The discrete nature of the various components was still maintained. The significant advantage now was that the weight and size of each part was reduced to a point where the component-mounting hardware became unnecessary. The wire leads themselves were sufficiently rigid to provide the mechanical support for mounting. One very important technique that evolved from this is the familiar cordwood package, in which all the components are stacked like cordwood and are held in place by printed circuit boards on both sides of the stack. The component leads protrude through holes in the boards, which are properly aligned. The leads are either soldered or welded to the printed circuit boards. Semiconductor diodes and transistors are particularly suited to this form of packaging.

Microminiaturization

Subminiaturization was followed by microminiaturization, which perhaps denotes the maximum size reduction at which the component still retains its discrete individual identity. However, at this stage the components lose their familiar forms and usually the leads are also left out. The form factor of the component is now determined by the supporting printed board or matrix. The pellet Micro-Components by Mallory and the Microseal components by Hughes are typical examples of this approach.

The three approaches described up to this point allow the circuit designer almost unrestricted choice in the selection of components for his circuit. Packaging techniques and packaging densities perhaps dictate the only restrictions.

Morphological Integrated Technology

This technology is very recent, in fact it is still in its infancy. However, it appears to hold a promising future. It is often referred to as the "functional-block" or the "molecular-electronics" approach, and is considered by many as the ultimate answer to both reliability and ultra-microminiaturization.

This approach dispenses with the traditional concept of component-and-circuit combination to obtain electronic functions. Instead, the present knowledge of the structure of matter and solid-state phenomenon is applied to synthesize functional blocks, composed and arranged in such a manner that each domain performs an electronic

function in transforming and controlling energy flow. This results in a single block of semiconductor material performing the function of a circuit or a subsystem. In such a composite block, neither the electronic components nor the circuits are identifiable as individual entities.

Integration by Thin-Film Technology

Chronologically, this technology introduced the most significant and revolutionary advance in microminiaturization. For the first time, the conventional components in discrete form are replaced by depositing them on a single substrate, either ceramic or glass. Furthermore, no wires are used for interconnecting the components. Instead, conducting film patterns are deposited such that they overlap the respective components. Currently, magnetic, insulating, and conducting thin films are successfully deposited.

At the present time, the major limitation of this approach is the fact that successful deposition of active elements, diodes and transistors is still some time away. There are several companies actively working on deposition of active devices with very encouraging results, but in the interim it is necessary to use individual discrete diodes and transistors in conjunction with deposited passive elements and thin-film interconnections.

Integration Utilizing Semiconductor Technology

This is a semiconductor-based approach in which all the components of a circuit or a subsystem form an integral part of a piece of bulk semiconductor material. In this approach, all the circuit components, both active and passive elements, are formed in the bulk material and become an indivisible and unalterable part of this material. Many presently known semiconductor technologies, such as diffusion, passivation, epitaxial growth, etc., are used to obtain the particular desired components. Interconnections between various components are obtained by deposition of conductors by thin-film technology or in some cases by ingenious juxtaposition of some of the components within the bulk material itself. Connections to the outside world are made by bonding thin wire leads to selected points on the surface of the semiconductor slice representing the required nodal points of the particular circuit configuration. We should realize that while this technique is very promising, particularly for computer applications, its future is directly linked with the advance of the semiconductor art, and its present limitations are basically the shortcomings of the semiconductor state-of-the-art.

In this book, when we talk about the "pure integrated" circuit, the "fully integrated" circuit, or just plain "integrated" circuit, we are referring to this particular approach to microminiaturization.

Partial Integration and Hybrid Integration by Combination of Thin-Film and Semiconductor Technologies

These approaches utilize thin-film technology to supplement the "pure integrated" circuit in those areas which are limited by the present state of the semiconductor art. Of all the existing forms of microminiaturization, these approaches give the widest choice of both active and passive elements and consequently offer the greatest potential flexibility to the circuit designer. The most attractive feature of either approach is that they are compatible in size and packaging densities to the "pure integrated" technique. Currently, two variations of this approach are being actively developed, and it is interesting to note the differences between the two.

HYBRID INTEGRATION. In this approach all the active elements of the circuit are diffused into the bulk semiconductor material. In one version of this approach, passive elements, such as resistors and capacitors, are deposited by successive evaporations. Interconnections between all the components are similarly deposited, and external connections are made by bonded leads. In another version of this approach, the passive elements are deposited on a separate substrate, either glass or ceramic. Interconnections between the two substrates are either by bonded leads, or sometimes the package leads of a TO-5 can are used as common nodal posts. In industry, either version is commonly referred to as the "hybrid integrated" approach; we shall use the same terminology.

THE MULTIPLE-CHIP APPROACH. In this variation, the circuit is distributed in pieces on two or more chips or substrates. All the active elements are diffused on one or more semiconductor chips. The passive elements are similarly grouped on one or more separate chips. In some cases the passive components may be diffused into separate semiconductors, or they may be deposited on some other base material, usually ceramic. The whole group of separate chips is interconnected by bonded wires, and connections for external purposes are similarly made by bonded leads. The terminology commonly used for this approach is the "chip version" of integration or the "multiple-chip approach;" these are the terms we shall use.

REFERENCE

1. H. V. Noble, "The Need for Microsystems," *Electrical Engineering*, July 1961, pp. 483–484.

Systems considerations 2

2.1 MICROSYSTEMS

Having established the need and the evolution of the phenomenon we refer to as microminiaturization, it is necessary to investigate some of the fundamental and rather broad problems which must be taken into consideration in planning and designing a microminiaturized system. Recently a new term has been added to the glossary of the electronics industry—*microsystems*. As of this writing, industry has not established a precise and widely accepted definition of this term. Many different definitions are offered, but the one characteristic common to all is small size of the subsystems and systems, and so the generic prefix *micro* is appropriate.

"Microsystems range from those using discrete but miniaturized active components and thin-film passive components (where possible), to those employing hardly distinguishable active and passive regions within single semiconductor structures."[1] This is the definition offered by H. W. Henkels of Westinghouse. It covers the entire gamut of "micro" concepts in Chapter 1.

Since this book is limited to integrated circuits using semiconductor and thin-film technologies, and combinations of the two, perhaps the most directly applicable definition would be as follows: Microsystems are electronic systems consisting of circuits and subsystems fabricated by the application of semiconductor or thin-film technologies, or suitable combinations of the two; they are packaged in present-day transistor cans, such as the TO-5 can, or in containers of other geometry of compatible or smaller volume.

2.2 ENGINEER'S ROLE IN MICROSYSTEMS

Traditional Concept of Engineering Functions

The complex nature of today's technology demands that each individual scientist and engineer specialize in a comparatively narrow area of his field of interest. Limitations in time make this a necessity. A discussion about the merits or otherwise of specialization is not intended here. Suffice it to say that it exists and that in the electronics industry it can be broadly categorized, as shown in Fig. 2.1. We can see that various engineering functions essentially form a serial chain

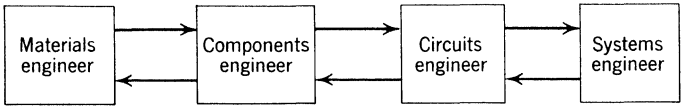

Fig. 2.1 Traditional interrelationships within engineering functions.

as far as planning and developing the ultimate product is concerned, and with regard to liaison and communications between them. The interrelations can best be understood by considering the functions of each engineering group separately.[2]

MATERIALS ENGINEER. The function of the materials engineer is clearly the development of new materials or modification of existing ones as indicated by the needs of the components engineer. His efforts in research and development are solely directed by the information fed to him by the components manufacturer. It is quite apparent that the materials man has little or no direct contact with the circuits or the systems engineer.

COMPONENTS ENGINEER. The scope of the components engineer's activities is somewhat wider than that of the materials engineer. His primary responsibility is to fulfill the needs of the circuits engineer, and so he plays the dual role of communicating with both the materials and the circuits people. Even then, his field of activity is pretty much specialized, and he seldom, if ever, has direct dealings with the systems engineer.

CIRCUITS ENGINEER. The circuit engineer's functions parallel those of the components engineer in that he has a two-way communication need with both the components and the systems engineer. He goes to the components man for the essential building blocks of his circuits, which in turn must satisfy the requirements of the systems engineer. His demands on the components man are principally dictated by the systems engineer's demands on him. In this case, his contacts with the materials engineer is via the medium of the components manufacturer, not directly.

SYSTEMS ENGINEER. In the functional chain, the efforts of the previous three are geared to the ultimate requirements of the systems engineer. The systems engineer's demands, however, are the primary concern of the circuits engineer. We should note that the systems engineer does not need to communicate his requirements directly to either the materials or the components engineer. The systems engineer, of course, has to satisfy the ultimate needs for his products.

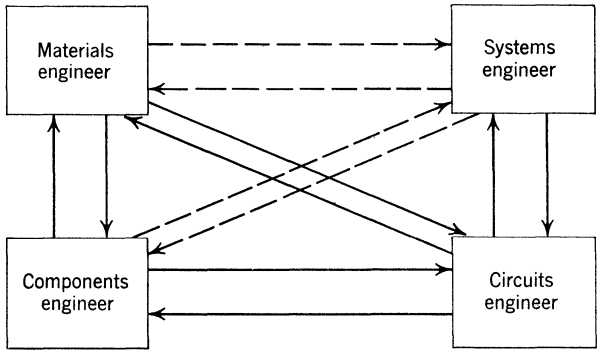

Fig. 2.2 Microsystems require interwoven relations of engineering functions.

Microsystems Integrate Engineering Functions

The natural outcome of the rigid partitioning of engineering functions is a high degree of specialization. Very often this specialization is carried to such an extent that the working engineers in each of the four categories have rather limited knowledge of the problems and workings of the functions adjacent to their own. They often have a technical language of their own. Microsystems demand much closer coordination between the aforementioned functions; in fact the barriers separating them are broken down to such a degree that they tend to merge into a coherent, interdependent, single function. Regardless of this, the serial chain of Fig. 2.1 is now modified to an interwoven complex of Fig. 2.2. The communication channels between the systems engineer and the materials and components engineers are shown by broken lines to indicate that, in microsystems, the systems engineer's principal line of communication is with the circuits engineer, with little, if any, direct contact with the other two categories.

Reasons for Interweaving of Engineering Functions

Figure 2.2 clearly shows that a much closer liaison and understanding of each function has become mandatory. Microsystems by their very nature demand this. In fact, quite frequently the functions of the components engineer now merge with those of either the materials or the circuits engineer, or both. Briefly, there are three reasons:

1. A manufacturer producing either a pure integrated or a hybrid integrated circuit or subsystem certainly combines materials and components engineering functions, and to a large extent even the circuits

engineer's functions. This is simply because he produces the desired circuit by the fabrication of active and passive components within, or on, one or more pieces of material (usually semiconductor, glass, or ceramic substrates).

2. In conventional systems, circuits and subsystems are designed around available components, both active and passive. The situation is radically different with microsystems. Now, the components which are circuits or subsystems, themselves, must be designed to systems requirements. This is the main reason why active coordination between systems engineering and the other three functions is so vital.

3. Another very compelling factor for close working relations is a purely economic reason. The production of an integrated circuit or a subsystem entails a substantial cost, particularly in the fabrication of the diffusion masks. It is therefore expensive and time-consuming to modify or replace designs. Costly redesigns can be avoided if sufficient coordination and exchange of information takes place initially between the systems engineers and the integrated circuits or subsystems suppliers. Such cooperation in the early stages of product design induces the systems engineers to formulate requirements which are within realistic capabilities of the vendor supplying the integrated circuits.

2.3 SYSTEMS PROBLEMS

In a system constructed out of integrated circuits, it is necessary to consider some of the basic problems associated with microsystems and decide on the most acceptable design trade-offs. These problems can be broadly classified in the following six areas: (1) power requirements and heat dissipation; (2) speed; (3) systems hardware layout, or topology; (4) reliability; (5) serviceability and maintenance problems; and (6) cost considerations. These areas are interrelated and in most cases cannot be considered separately. For purposes of presentation it is expedient to look at them individually.

Power Requirements and Heat Problems

In microsystems, perhaps the biggest problem confronting the design engineer is the power requirements of the circuits and subsystems which go to make up the total power requirements of the entire system. It is, of course, advantageous to keep the total consumption as low as possible, since the heat generated within the system is directly dependent on power. Since circuit components are basically temperature-limited, it is necessary that the internally generated heat be dissipated as quickly as possible. Heat dissipation, therefore, is a prime factor

in establishing the weight, volume, and packaging densities of microsystems.

Obviously, the most direct solution to the heat problem is the development and use of extremely low-power devices. But even this desirable goal has its limitations. Basically, the function of any electronic circuit or system is the transfer of energy; thus, signal-power levels, operating speeds, noise levels, component tolerances, ambient temperatures, and characteristics of power sources all tend to restrict the lower limit of power dissipation.

At the present time, perhaps the largest potential use for integrated circuits is in the area of logic circuits in digital systems. It is therefore worthwhile to briefly look at the various logic circuits and how power can affect the decision to use them. Saturating transistor circuits have several desirable features as compared to the nonsaturating types. Low power requirements and reduced number of components are the main items favoring the saturating circuit. Even in this case, power dissipation exerts a decisive influence. In a system where speed may be of prime importance, obviously resistor-transistor logic (RTL) would be a rather poor choice. If other factors dictate that RTL be used, then perhaps a speed-up capacitor may offer some solution to speed, provided reduced logical gain can be tolerated. Additional buffer stages may also be necessary to reduce transient coupling. If noise levels within the system are high, the direct-coupled-transistor-logic (DCTL) should be avoided. In view of these limitations, diode-transistor-logic (DTL) might offer an acceptable compromise.[3] (See Chapter 9 for additional information on digital logic circuits.)

Power supply and component tolerances also affect power dissipation. If tolerances for component manufacture, temperature effects, and drift due to aging, as well as power supply tolerances, can be improved, then circuits can be designed with tighter tolerances, and power can be reduced. Sometimes additional power dissipation can be traded off for looser tolerances. This trade-off may set off an inevitable chain reaction, which may be undesirable. Tolerance slack compensated by added power level may necessitate reducing the load of a circuit. Of course, this compensation may allow fanouts to be maintained, or more circuits may have to be added to maintain the desired logical performance of the system. This would increase the system complexity, as well as size and weight. It is apparent, therefore, that some of the very basic features of microsystems may be compromised.

In saturating circuits, the lower power dissipation limit is established by the low-current gain of the transistor. Also, the upper speed limit is set by the gain-bandwidth of the transistor. Consequently, these

two factors define the speed-power dissipation relation of the circuit, because, as the operating speed increases, power dissipation also increases. Another factor is prominent in this consideration: distributed capacitance loads the circuits quite significantly and slows them down. To maintain the required speed, power levels of the signal would have to be increased.

System Speed

High operating speed is one major factor associated with computing systems. While higher speeds are desirable in practically all computer applications, they become a very critical requirement in today's aerospace systems, since the fantastic speeds attained by missiles and orbiting vehicles demand exceptionally high computing speeds.

In the past, the demand for increased speeds in electronic equipment was satisfied by developing components and devices which were inherently faster and more efficient. This approach is rapidly reaching its upper limit. Speeds of components and devices will undoubtedly be improved in the future. On the other hand, in certain computer applications, a point is now reached where propagation delays in wiring become a very prominent factor in the overall speed of operation, as compared to the speed of the components. Thus it is quite evident that the physical size of a system directly limits its operating speed. In a system that has reached this speed-size ceiling, the only way that speed can be increased is by a reduction of its physical size. Microsystems offer a very substantial advantage with regard to this problem. Connecting leads between circuits can be reduced to such a degree that propagation delays may often be reduced by at least an order of magnitude. By incorporating two or more fully integrated circuits on one piece of semiconductor material, signals can be transmitted directly from one circuit element to an adjacent one, which may comprise the input element of the next circuit in the logical chain. Obviously, in such a configuration, the propagation delay can be reduced to almost zero.

Systems Hardware Layout (Topology)

Some recent studies of packaging problems of electronic systems[3] reveal that as much as 90% of the total volume of a system may be taken up by wiring, printed-circuit board connectors, mounting hardware, and cooling equipment. According to this, the volume occupied by the actual electronic components would be approximately 10%. This 9:1 proportion in conventional hardware would undoubtedly become more lopsided with microsystems, unless serious consideration is given to both circuit and system layouts.

In circuitry using conventional components, electrical problems generally dictate circuit layouts with relatively minor attention given to thermal considerations. In systems using integrated circuits, the systems layout is determined by power density, speed, and interconnections. From the circuit point of view, whether the circuit is fully integrated or partially integrated, the components must be laid out in such a manner that the temperature rise of adjacent or nearby components do not affect them adversely. Circuit reliability requires that all components operate within the allowable temperature limits. From the systems point of view the heat dissipated by the various component subsystems must be adequately sinked.

In order to insure high-speed operation, it is necessary to provide adequate shielding against external noise. In microsystems, the compact packaging of circuits greatly increases the possibilities of stray coupling between circuits. To minimize this problem, signal leads must be located away from clock pulse lines, and power lines must be properly shielded. Additional shielding may be necessary in special cases, and local ground planes may become an absolute necessity in some systems.

Reliability

The complexity of modern electronic equipment is increasing at a tremendous rate, and this applies to communications equipment, weapons systems, as well as computers. Present trends indicate that increased demands on higher performance, particularly in aerospace applications, will result in increased complexity; thus correspondingly larger quantities of components will have to function simultaneously. In terms of reliability, we appear to be approaching a limit where additional complexity can be realized only if some reliability is sacrificed. Perhaps this situation can be more graphically illustrated by a curve, as shown in Fig. 2.3, for a purely hypothetical electronic system.

In the past, electrical connections have been the largest single factor contributing to unreliability of electronic equipment. In microsystems, the number of point connections of the conventional type are reduced. Of course, connections between circuit components on a silicon block have to be made. However, in such fully integrated circuits, these connections are normally made by deposited interconnecting patterns, which are inherently more reliable than individual discrete connections. Consequently, reliability can be expected to increase significantly in microsystems.

The reliability of a system depends on both the drift and the catastrophic failures of its components and subsystems. Microsystems

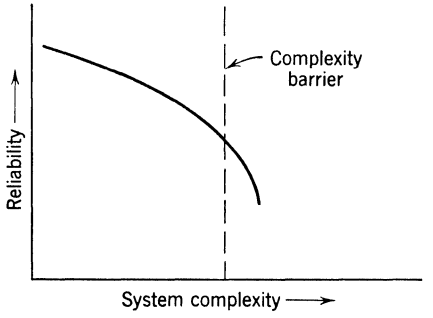

Fig. 2.3 Reliability—complexity curve for a hypothetical system.

offer a large measure of relief from catastrophic failures, but with drift failures conventional engineering considerations still largely apply. Drift failures can best be combated by introducing sufficiently wide component-tolerance margins in circuit designs. However, the price of component tolerances is increased circuit power dissipation. It is therefore quite evident that these trade-offs must be carefully weighed in terms of overall reliability in the design of a system.

One school of thought advocates redundancy as a means of handling catastrophic failures. There are three types of redundancies—(1) component, (2) logic, (3) standby—which can be used either individually or in suitable combinations. In component redundancy, a group of components can be used to perform a function that would normally be accomplished by a single component. When any component within the group fails, the external characteristics of the group naturally change, but it can still perform its intended function. This type of redundancy can be readily obtained with integrated circuitry. Logical redundancy is basically a majority-decision-type of redundancy. The logical output of a circuit block is established by the majority of the logical inputs to the block. In standby redundancy, a standby unit is always available for each subsystem. A failure of the subsystem is detected by a detection device, which then actuates a transfer device which, in turn, switches out the failed subsystem and switches in the standby unit. It is quite clear that whatever philosophy of redundancy is adopted, microsystems greatly increase both the technical and economic possibilities of incorporating them in complex systems.

Serviceability and Maintenance Problems

Servicing and maintaining a complex electronic system is a major challenge, even using conventional components. In microsystems, using integrated circuits, the problems can be compounded. Evidently, it is impossible to replace a defective component in an integrated circuit. The entire circuit must be treated as a single component, and a faulty one must be replaced by a known good component circuit. A throw-away philosophy of maintenance, therefore, appears inevitable. Since several circuits would often be combined into a module or a subsystem, it may become necessary to discard a whole subsystem. This is obviously an expensive proposition and one that merits very careful study in the early stages of systems design. To keep this cost to a minimum, it is desirable to keep the number of circuits per module as low as possible. However, to fully exploit the advantages of the smaller number of interconnections possible with microsystems, it is necessary to incorporate as large a number of circuits as possible within a module. These conflicting requirements must be resolved in such a manner that the reliability goals are satisfied within the economic boundaries of production and maintenance in the field.

Another maintenance problem is accessibility. Because integrated circuits are inherently small, physical handling becomes a very serious problem. Removing a module from a system and replacing it with a new one would require special tools and equipment which would ensure that the modules are not damaged in the process.

Cost Considerations

Initially, integrated circuits can be expected to be more expensive than similar circuits built out of conventional components. Thus the first significant applications would probably be in military-sponsored programs. Two reasons account for the high initial cost. First, the semiconductor industry has put in a sizable investment in the research and development of the various processes. This would naturally be reflected in the initial cost. Second, at the present time, the process yield is relatively low, and this means that the unit cost will be higher.

However, there is good reason for optimism too. As the processes are improved, the higher yields will bring the cost down. Furthermore, during manufacture, the same process run usually forms all or most of a certain type of circuit component on an integrated circuit substrate. This simultaneous fabrication of all diffused or deposited elements means that all elements of that run tend to be uniform. Thus, if an element is good, chances of the rest being good are pretty

high. This is a major advantage of this technique which offers possibilities of substantial price reductions. The price of integrated circuits will favorably compete with other forms of circuits very soon.

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section 2

Techniques and processes

Review of fundamental semiconductor processes

3

Engineers who design circuits for equipment manufacturers, of course, have a reasonably good understanding of the physical processes involved in semiconductor devices—diodes and transistors. By far the great majority of them have a rather limited understanding or appreciation of the various processes associated with the manufacture of these devices, mainly because this knowledge is not an absolute prerequisite for the design of conventional circuits. Data supplied by the vendors and supplemented by the user's own reliability data, test information, and past experience provide sufficient material for the design of circuits. The demands of integrated circuits are more exacting, and it is imperative that both the circuits and the systems designers acquaint themselves, to some degree, with the fabrication processes, since their design efforts will be largely influenced and directed by the manufacturer's capabilities.

The purpose of this chapter is to briefly describe most of the commonly used processes. Detailed descriptions of the processes are beyond the scope of this book. Rather, the objective is to list the processes (and their simple descriptions) in such a manner as to provide some background for the material that follows in the later chapters. To this end, the processes are divided into two major categories: (1) *semiconductor processes*—those involved in the fabrication of the semiconductor devices and the various functions associated with them; and (2) *thin-film processes*—processes which are external to the semiconductors or other substrate material.

This chapter covers only the first category. Thin-film processes are covered in the next chapter. Also, in order to facilitate the understanding of the processes from the circuits point of view, both the semiconductor and the thin-film processes are further subdivided and investigated in terms of their being able to provide the familiar functions of[3] (1) active elements, (2) resistive elements, (3) capacitive elements, (4) inductive elements, (5) conduction between circuit elements, (6) circuits and components isolation.

3.1 ACTIVE ELEMENTS

Surface Passivation and Planar Technology

The conventional mesa transistor has some serious limitations. The electronic properties of the crystal are sensitive to impurity conditions at the surface and the ambient humidity. As a result, the operating characteristics of the device suffer degradation and wide variations. Unfavorable environments introduce chemical impurities, that is, large quantities of acceptor, donor, and lifetime carriers at the surface of the semiconductor. These impurities are very loosely bound and so have high mobility as compared to the strongly bound impurities in the material which has relatively low mobility. The thin oxide layer on the semiconductor material tends to attract moisture. In ambient humidity, this produces a solution of ions and dipoles which have high mobility. The hermetically sealed package does not remedy this situation. It merely restricts these detrimental environmental factors to a confined location.

Figure 3.1 shows a cross-sectional view of the typical mesa transistor, where the base dopant is uniformly diffused in the entire top area of the silicon material, which forms the collector of the transistor. The emitter is diffused at the desired location. The chip is then etched to give the desired mesa shape. The reason for the mesa is to limit the area of the base-collector junction to the point desired by the electrical characteristics of the device. Metallic contacts are alloyed into the base and emitter areas and gold leads are attached on the metalized surfaces by thermocompression bonding. The collector is soldered to the header. As a result of the mesa etching process, both the base-

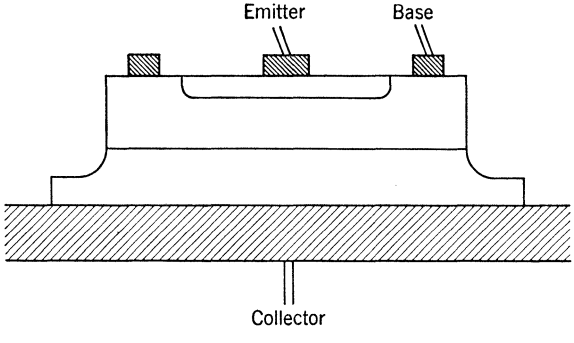

Fig. 3.1 Typical mesa transistor.

collector and the emitter-base junctions are now exposed and thus easily accessible to ambient environments or to mechanical damage in handling (Fig. 3.1). This results in degradation of electrical characteristics, such as high reverse leakage current, low breakdown voltages, high noise figure, low betas at low currents, and low power dissipation rating.

The shortcomings of the mesa process are largely reduced by the planar or surface passivation technique. In this technique, the lateral flow of the base dopant in the semiconductor is restricted from the start to the extent desired by the transistor requirements, thereby eliminating the need for mesa etching later on. The term *planar* or surface passivation can be defined as the growth of a chemical film layer on the surface of a semiconductor material which provides electrical stability of the surface and isolates the surface from the electrical and chemical conditions in the environment, which degrade device characteristics and thereby adversely affect its operating performance.

Figure 3.2 illustrates the steps involved in the fabrication of the planar transistor.[2] The basic N-type silicon substrate, is shown in Step 1 with a thin layer of silicon oxide on its surface. Using standard photo-processing techniques, the oxide is selectively etched off on a series of dots, as shown in Step 2, thereby exposing the surface of the semiconductor material. The exposed surface is subjected to a vapor of the base diffusant, such as boron for a NPN transistor or phosphorus for PNP units, at a high temperature. The oxide layer limits the lateral diffusion of the dopant, as shown in Step 3, under the original oxide, usually by an amount equal to the depth of the junction. During this operation, oxygen is introduced so that the previously exposed area is reoxidized. During formation of the base-collector junction this area was protected by the first oxide layer and this junction was not exposed to contaminating environments at any stage of the process.

In Step 4, a portion of the reoxidized base area is removed by a similar masking and etching process. In Step 5 the exposed base area is subjected to a vapor of the emitter dopant, such as phosphorus, and the emitter area is again reoxidized during the process. Once again, a junction emerges under the area of the second oxidation process and is thus protected from adverse environments. This junction is, of course, the emitter-base junction of the transistor. Following this the final oxidized layer is again etched off at specific areas as shown in Step 6. Metal contacts are deposited and alloyed in as shown in Step 7. Wire leads are attached to the metalized areas by thermocompression bonding.

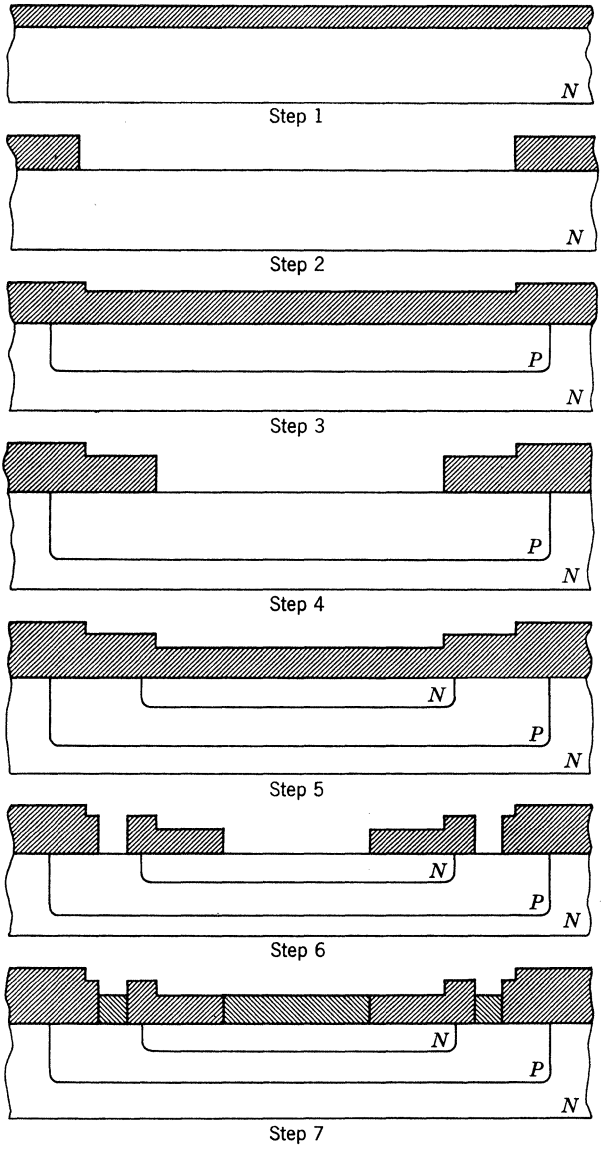

Fig. 3.2 Steps in the planar process: (1) passivated oxide layer on substrate; (2) part of oxidized layer is selectively etched; (3) *P* layer is diffused and surface is reoxidized; (4) reoxidized layer is again selectively etched off; (5) *N* layer for emitter is diffused and surface is reoxidized; (6) oxidized areas are again selectively etched off for contacts; (7) metal contacts are deposited and alloyed on the substrate at etched-off areas.

Epitaxial Techniques

The conventional mesa transistor has the advantage of high-frequency cut-off and rugged physical construction. Its principal limitation is the fact that the semiconductor material has to be relatively thick to insure physical rigidity. Since the entire piece of semiconductor material, which is several mils thick, is cut from one large crystal, it has uniform purity and, consequently, uniform conductivity throughout its entire bulk. The degree of purity of the semiconductor material is governed by the desired electrical characteristics of the device, which is diffused on the surface. The high degree of purity in that portion of the bulk material, not used for either the emitter or the base diffusions, gives added resistance in the collector of the transistor and stores electrical charges, which slow down switching speeds. Consequently, saturation resistance is high; however, it can be lowered by using lower resistivity collector material, but only at the expense of lower breakdown rating. The conventional alloy transistor has the advantage of low saturation resistance. Epitaxial transistors combine the advantages of both the mesa and the alloy transistor without any undesirable compromise.

In epitaxial transistors, the original bulk material is cut from a crystal with very high electrical conductivity. This slice is then subjected to an atmosphere of hydrogen and a gaseous compound, which may be a chloride of the same semiconductor material at high temperature. This results in the deposition of a lightly doped semiconductor material on top of the original substrate material. This epitaxial layer is grown to give the right thickness for the desired

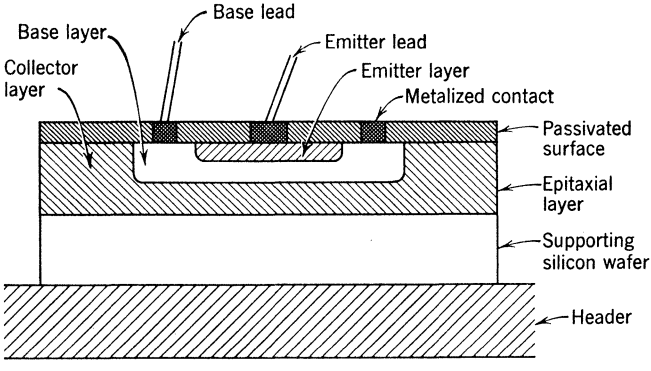

Fig. 3.3 Epitaxial planar transistor.

transistor, and is of the same conductivity type as the original substrate—either P or N-type. The transistor is then diffused in the epitaxial layer. Since the original substrate has low resistivity, it contributes very little resistance to the collector of the transistor. Consequently, more current can be passed through the transistor. The main advantage of this type of transistor is low saturation resistance and lower collector storage time, as compared to a similar non-epitaxial unit. The low saturation resistance makes the epitaxial transistor suitable for direct-coupled transistor logic (DCTL). The thin epitaxial layer has relatively high resistivity, which gives the unit a higher voltage rating. The higher resistivity of the epitaxial layer reduces the collector capacitance quite appreciably. Reduction in saturation resistance makes it possible to use devices with smaller geometries, thereby reducing the area of the emitter. These two factors greatly increase the frequency limits of the epitaxial transistor (Fig. 3.3).

3.2 RESISTIVE ELEMENTS

Substrate Resistivity (Bulk)

The easiest way to obtain resistive elements in integrated circuitry is to use the bulk resistivity of the semiconductor substrate itself. Since this resistivity can be controlled quite easily, this approach may appear very attractive and certainly very economical. However, it has some very serious shortcomings, which limit its usage in practical applications. A maximum usable resistivity of about 500 ohm-cm is possible, but this is not compatible with the present technology of fabricating either the collector or the base of the transistor. This means that it would be almost impossible to use the same substrate for both the resistors and the transistors. A more realistic upper limit is probably around 100 ohm-cm. Even then, the most compatible value would not be greater than 50 ohm-cm. Another drawback of this approach is that the bulk material has a fairly complicated temperature coefficient. Occasionally, this temperature dependence can be used advantageously for compensation in some circuits.[3]

Diffused Resistors

A very useful resistor can be obtained by diffusing a thin layer in the parent semiconductor material, and back-biasing the junction. Two major advantages of this type of resistor are (1) by ingenious layouts, the resistor can be located adjoining another element such that additional interconnection between the two components can be eliminated, and (2) by controlling the diffusion profile and the doping levels,

the temperature coefficients can be controlled such that either negative, positive, or virtually zero coefficients can be realized at room temperature.[3] Diffused resistors can be of great value in applications where tolerances are not very critical.

The two principal disadvantages of this type of resistor are (1) the resistance is sensitive to the back-biasing voltage, with wide variations resulting in practical circuits, and (2) the voltage drop in the resistor generates a self-back-biasing component, which can further affect the resistance value. This also provides a means of obtaining electrically variable resistance, which may be advantageously used in some circuit applications.

Epitaxially Grown Layers

Resistive regions with desired characteristics have been grown on semiconductor substrates using epitaxial techniques. This technique requires masking for obtaining the right geometry. Back-biasing is required, so the advantages and the disadvantages of back-biasing, which were previously discussed, apply here just as they do with the diffused resistor. However, better control of the junction characteristics is possible with the epitaxial technique, as compared to the diffusion technique.

3.3 CAPACITIVE ELEMENTS

Diffused Back-Biased Junctions

At the present time, perhaps the easiest method of obtaining capacitors in integrated circuits is by back-biasing diffused junctions. The depletion layer at the junction forms the dielectric, and values in the neighborhood of 1 v-μf/cm^2 have been successfully realized for step junctions at low voltages. It is quite apparent that the value of capacitance obtained will depend on the width of the depletion layer, thus it is important to consider the factors which affect the depletion layer width.

The width of the depletion layer is primarily determined by the impurity concentration gradient on either side of the junction, and the reverse voltage applied across the junction. The diffusion process produces a graded junction which means that, for a given value of reverse voltage, a diffused capacitor would tend to have lower values of capacitance as compared to capacitors fabricated with other techniques. The physical location of the diffused junction in the semiconductor material is sometimes very critical. If the junction is located such that current flows parallel to the junction but outside the depletion layer, then, the bias on the junction itself would not be uni-

form. This current would be particularly troublesome if it flows through the bulk resistor and if the junction in question is not biased. In such a situation, the floating junction will tend to conduct in order to stabilize the potential at one end, and in so doing it will back-bias the rest of the junction. This can also be used to advantage in some circuits.

Alloyed Back-Biased Junctions

Capacitors made by back-biasing alloyed junctions approach a step junction much more closely than do the diffused back-biased junction units. As a result, higher values of capacitance can be obtained with relatively lower back-bias voltages. This is due to the fact that the impurity concentration on one side of the junction is effectively the same as or close to that of the parent substrate material. Thus a steep impurity gradient can be readily obtained across the junction. The impurity concentration in the substrate is low, thus, at large values of reverse bias voltage, the width of the depletion layer can be as large as in the diffused junction capacitor.

Epitaxial Back-Biased Junctions

Capacitors obtained by applying back-bias to epitaxially grown junctions are still in their infancy, but work done to date promises some encouraging possibilities. In this case, the high impurity concentration of N-type on one side can approximate the step junction very closely to the high impurity concentration of P-type on the other. Consequently, at low values of reverse bias, a relatively high value of capacitance is obtainable. This means that the voltage dependence of the capacitance is reduced to some extent and it also becomes more controllable and predictable.

3.4 INDUCTIVE ELEMENTS

The Inductance Diode

Perhaps the most difficult parameter to incorporate in integrated circuitry, at the present time, is inductance. To date, no really satisfactory technique has been reported. The inductance diode is one method of obtaining this parameter. A device described by Nishizawa and Watanabe[1] has a P^+N junction in which the N region is longer than the P^+ region and has higher resistance. When the junction is forward-biased, the P^+ region injects the holes which travel toward the opposite electrode, and in doing so lowers the resistivity in the N region. A time delay is associated with the lowered resistivity. This delay is directly dependent on the length of the N region. The initial resistance of the device corresponds to an equivalent resistance parallel

to the inductance, and the final resistance corresponds to an equivalent resistance in series with this parallel combination. Such a junction diode has low inductance, the inductance being determined by the time delay, and low Q.

Inversion of Capacitance by Active Elements

If resonance is not required, inductance can be obtained by using active element networks to invert capacitance. Impedance inversion is possible with field-effect semiconductor devices. Using this principle, a low-Q capacitor can be made to appear as a high-Q inductor. This method appears to have rather limited possibilities at present.

3.5 CONDUCTION BETWEEN CIRCUIT ELEMENTS

Juxtaposition of Circuit Elements

One of the most attractive features of integrated circuit lies in the possibility to drastically reduce the number of ohmic contacts connecting one circuit component to another. It is sometimes possible to eliminate interconnecting paths completely by positioning the components such that one butts the other or just naturally merges into the other. The following simplified example will illustrate the point.

Suppose it is required to connect four transistors, two *NPN* and two *PNP*, as shown in Fig. 3.4*a*, using integrated circuit techniques. One way to eliminate the connection from the collector of one transistor to the base of the succeeding one, is to start out with basic semiconductor substrate, either P or N type, and obtain a four-layer $PNPN$ unit, as shown in Fig. 3.4*b*, either by successive diffusion of the other three layers or by successive epitaxial growth. The next step would consist of etching off the shaded portions (Fig. 3.4*c*), which now gives the desired four-transistor configuration. It is seen that the N-type collector of transistor Q_1 and the N-type base of transistor Q_2 are connected together because they are both part of the same original N-type layer. Similarly, the P-type collector of Q_2 and the P-type base of Q_3 are both part of the original P layer. The collector of Q_3 and the base of Q_4 are likewise part of the same original N-type layer. The reader should note that this particular example is not realistic from a practical point of view. It is intended only for illustration purposes.

Degenerate Regions

Intrinsic connections between components within the semiconductor substrate can be made by connection patterns in which the conductivity is increased considerably. Such regions can be produced by alloying doping impurities into the desired path patterns. The dopant

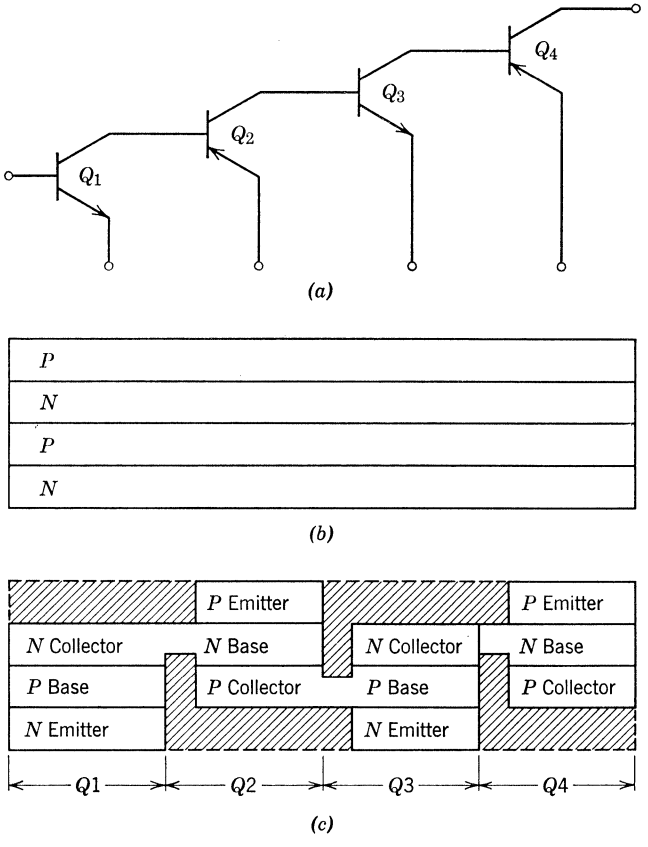

Fig. 3.4 Simplified example of conduction between circuit components by juxtaposition: (*a*) four-transistor configuration; (*b*) the *PNPN* four-layer substrate; (*c*) cross-hatched areas etched off.

concentration is such that it almost saturates the region. This method gives conducting paths usually at or near the surface of the parent material. Using this technique, resistivities in the range of 10^{-3} to 10^{-4} ohm-cm have been reported. For several applications this is a satisfactory range.

3.6 CIRCUIT AND COMPONENT ISOLATION

Back-Biased Junctions

Isolation of components is a necessity in all circuits, integrated and conventional. In integrated circuits the problem of electrical insula-

tion is particularly severe because of the close proximity of component location. Current flow and the resulting fields must be considered in the circuit layouts as otherwise interacting fields may easily result in malfunctions or total failures of components. For low-frequency applications, back-biased junctions can provide acceptable insulation with reasonable values of reverse bias voltage. This is because at low frequencies, the capacitive effects of a graded junction can be relatively insignificant.

We would normally expect complete, or almost complete, isolation between diffused components which are separated by back-biased junctions, because current flow between the components would be confined and restricted due to the large reverse impedances of the various *P-N* junctions. Unfortunately, this utopian situation seldom exists in actual units. Junction areas partitioning the circuit components are relatively large and are usually leaky, so it is very desirable to channel the leakage current into a low-impedance sink. The simplest way to do this is to apply a voltage to the header, such that it will always back-bias the *P-N* junction. This voltage would be the most negative voltage used in the circuit for a *NPN* configuration and the most positive voltage in the circuit for a *PNP* structure. Back-biased junctions also reduce some of the parasitic capacitances by shunting them to a voltage or to ground. This reduces interactions between the circuit components due to capacitive coupling.[3]

Thermal Oxidation

This method of isolation is basically the same as the surface passivation or the planar process, which was previously discussed. The oxide layer grown upon the exposed surface of the silicon substrate has excellent insulating properties which can be put to good use. Certain areas on the substrate surface, as well as *P-N* junctions, can be insulated by this method.

Isolation by Etching

Etching as a means of isolating components is a fairly easy method, which was used in the early days of the integrated circuits. Using an acid etch, the components were isolated from each other by etching through from the top of the wafer, thereby forming mesas containing the components. Sometimes the wafers were etched all the way to the header. This method is not as readily adaptable to volume production as some of the other methods and so has rather limited utility.

Intrinsic Layer by Epitaxial Growth

The epitaxial method of growing intrinsic material gives a very promising means of insulation in integrated circuits. Two regions of

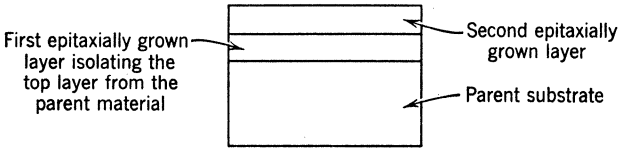

Fig. 3.5 Epitaxial method of vertical isolation.

conductive semiconductors can be isolated from each other by an epitaxial layer of intrinsic material. The resistivity of the epitaxial layer can be made such that it can effectively isolate the two regions. The epitaxial layer, by its very nature, can provide only vertical isolation between layers (Fig. 3.5), and not laterally between components diffused in the same layer. This means that, for this technique to be useful, a second epitaxial layer must be grown on top of the first one. This has been successfully done in the case of transistors and has encouraging possibilities for integrated circuitry.

Through Diffusion or Separation Diffusion

The limitations of vertical isolation by the epitaxial technique are quite obvious. Since the epitaxial layers themselves are very thin, the isolating layer must be devoid of impurities if effectively high insulation is desired. A very high degree of process control is required to ensure this. Furthermore, vertical isolation is certainly not always called for. Lateral isolation is almost always desired. Another intrinsic way of obtaining this is by through-diffusion (Fig. 3.6). As an example, if regions A and B in the N-type substrate have to be isolated, a P layer can be diffused vertically as shown. The doping of the P layer can be controlled to give higher resistivity, thereby giving effective isolation between regions A and B. There are two

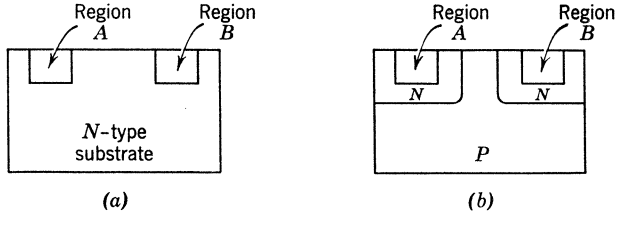

Fig. 3.6 Isolation by through diffusion: (*a*) regions to be isolated in N-type substrate; (*b*) through-diffused P layer.

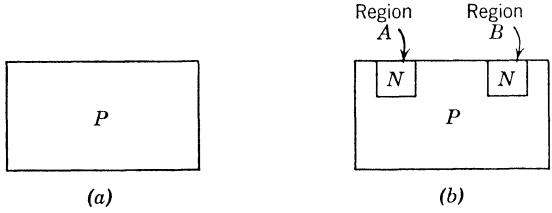

Fig. 3.7 Triple diffusion.

major drawbacks to this technique at the present time. First, the process requires the use of masks, and this is always expensive. Second, the dopant of the isolating region (P type in this case) does not diffuse into the material in a restricted vertical column but tends to spread out in all directions as it penetrates the substrate. This spreading out of the P layer is very difficult to control and so the possibility of its inundating into regions A and B is very great. Unless this process can be more accurately controlled, poor yields are likely. Also, larger areas needed, because of spreading, and larger process time required are undesirable features of this method. The main advantage of this method is that the smaller areas of the isolated islands reduce the circuit parasitics.

Triple Diffusion

In the through-diffusion method, the original substrate was N-type material. The same end result (Fig. 3.6*b*) can be obtained by the triple-diffusion method. Here, the original substrate material is P-type (Fig. 3.7*a*), and the N-type islands are diffused to form the isolated regions. These islands form the collector regions of the transistors. Subsequent P and N diffusions give the base and the emitter regions. We should note that the N-diffused islands result in a shallow diffused area, and hence much tighter control of tolerance is possible. Because of the smaller distance to be traversed by the dopant, the diffusion process takes a much smaller time and this results in considerably less fringing.

Through Diffusion in Epitaxial Layers

From our discussion it is quite apparent that all three methods—the intrinsic layering by epitaxial growth, the through-diffusion, and the triple-diffusion—have advantages and drawbacks. At the present time several efforts are made to combine the advantages of two or more of these techniques. Experimental work seems to indicate that it

would be possible to isolate components in the second epitaxially grown layer (Fig. 3.5) by a through-diffusion process. In such a case, the second epitaxial layer would be *N*-type material, and this layer would be very thin, probably less than 1 mil thick. The *P*-type diffusion for separation would have to travel a very short distance, thereby providing better control of the diffusion process and restricting the spreading out of the *P* regions.

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Review of fundamental thin-film processes

4

Integrated circuits, as they are now fabricated, invariably use deposited conducting patterns for interconnects. Thin-film techniques have been with us for some time now, and, in several applications, the circuits are designed and fundamentally built around thin films. While these circuits have certain very desirable characteristics and features, in this book we are confining ourselves mainly to thin films as they complement the integrated circuits. In other words, we are considering thin films as supporting techniques for integrated circuits—either fully, partially, or hybrid-integrated circuits. For purposes of explanation, and for conformity to the scheme of presentation established in the previous chapter for semiconductor processes, we shall discuss them in terms of the same circuit functions as before.[3]

4.1 ACTIVE ELEMENTS

Vapor Deposition of Semiconductor Active Elements

Many companies are currently working on the problem of depositing large-area, thin films of semiconductor materials on insulating substrates, and while encouraging progress is reported, these elements are not as yet available on a commercial basis. In 1961, Philco Corporation announced a metal film device, called the Metal Interface Amplifier, which consists of four elements. The substrate material used is germanium and it forms the collector of the transistor. A metal film is deposited on top of this, followed by a layer of insulation. Another layer of metal film is deposited on top of the insulator. So far, this device has been reported operational but only in the laboratory developmental stage.

It is difficult to predict what impact this technique is likely to have on integrated circuitry when it has achieved some success. It is, of course, evident that in applications, other than that of a fully integrated circuit, deposited film transistors and diodes will play a very important role.

Vapor Deposition of Nonsemiconductor Active Elements

It is possible to deposit ferroelectric and ferromagnetic materials on passive substrates and obtain effects similar to those of semicon-

ductor devices. The dielectric constant and permeability of these materials can be very easily altered by the application of electric and magnetic fields of the correct intensity. The problems involved in the deposition of uniformly coherent films of these materials are not completely solved, and thereby require some sort of compensation for nonhomogeneity in their design. When these problems are solved, we can hopefully expect newer active devices which may be suitable for use with integrated circuits.

Use of Discrete Active Elements

Since thin-film active devices are still in the future, the only way to use extrinsic diodes and transistors in thin-film circuitry is by means of discrete individual units. The active elements can be attached to passive substrates in a number of different ways. Transistors and diodes, encapsulated in conventional or microminiature packages, can be mounted on the substrate with protruding leads soldered to the corresponding pads on the deposited film circuits. Another technique involves the use of unencapsulated semiconductors. These chips are bonded to the substrate. Parts of the element's active areas are selectively masked with a layer of insulating film. Connections are then vacuum deposited over these exposed areas. The semiconductor thus becomes an integral part of the deposited circuit.

4.2 RESISTIVE ELEMENTS

Tin-Oxide Films

The resistor industry has been able to produce tin-oxide film resistors by hydrolysis for some time with quite a high degree of process development and control. The same techniques are used in producing this type of resistive elements for microcircuits. Present techniques are capable of achieving tin-oxide films with resistivity in excess of 5000 ohms/square. Resistance values from 1 kilohm to 10 megohms, with tolerances of $\pm 10\%$ and a temperature coefficient of $+300$ ppm/°C at power ratings of $\frac{1}{4}$ watt have been successfully used in hybrid-integrated circuitry.

Indium-Oxide Films

In certain instances, subjecting a substrate with partially deposited components and circuitry to high temperatures might result in irreversible changes. Indium-oxide films offer a suitable solution for depositing resistors in such cases. This is a two-step process. Relatively pure indium is first deposited in a low-pressure oxygen atmosphere. The deposited indium film is then oxidized slowly over a period of several hours at a temperature of 200°C or less.

Metal Films

Several metals and alloys have been deposited to give precision film resistors. Aluminum, titanium, and tantalum can be deposited in relatively thick films. Such a film can be trimmed to the desired value by anodizing its outer surface. The thickness of the oxide thus formed is a function of the anodizing voltage, thus the thickness of the remaining metal film can be accurately controlled. This technique has the added advantage of high reproducibility, thereby giving higher yields. Resistivity of around 2000 ohms/square with temperature coefficient of -100 ppm/°C has been achieved for titanium films, and 500 ohms/square and ± 200 ppm/°C have been reported for tantalum films.

Excellent results have also been indicated by deposited-alloy film resistors. Nickel-titanium films with resistivities varying from 750 to 2000 ohms/square and temperature coefficient of ± 200 ppm/°C have been obtained by vacuum-deposition techniques. Work done at the Royal Radar Establishment in England has yielded 300 ohms/square and $+24$ ppm/°C for nickel-chromium films 50 Å thick.[1] Also, an alloy of 20% platinum and 80% gold with a thickness of 1000 Å deposited on glass substrate gives a resistivity 60 microhms/cm and a temperature coefficient of 0.025%.

Nichrome Films

Nichrome film resistors have some desirable advantages. They exhibit very good adhesive properties when the substrate is heated to 300°C, they are highly stable, and have excellent reproducibility. The temperature coefficient varies from 50 to 150 ppm/°C, and nichrome film readily forms ohmic contacts with most other metal films. Their main disadvantage is that they have comparatively low resistivity which limits their use in applications of 500 ohms/square. The surfaces of unencapsulated nichrome films are very susceptible to oxidation and corrosion, and these limit their usage very severely.

4.3 CAPACITIVE ELEMENTS

Metal-Oxide Dielectric (Glass)

Several metal oxides have been used as dielectric material for deposited capacitors quite successfully. One of the most commonly used dielectrics is the vacuum-deposited silicon monoxide, which is sandwiched between two conducting metal layers. Some of the commonly used electrode metals are aluminum, zinc, magnesium, tin, silver, and gold. The best capacitors are formed with electrode films of noble metals. Gold is particularly suitable because of its high conductivity and inertness to oxidation. It can also be deposited with relative ease.

With silicon-monoxide dielectrics, capacitance values from 0.0019 to 0.0099 $\mu f/cm^2$ can be obtained depending on the metals used for the electrodes.[2] For dielectric thickness varying from 0.23 to 0.46 μ, dielectric constants from 5 to 7 are possible. Breakdown voltages up to 3500 volts/mil are possible. If higher breakdown voltages are desired, silicon dioxide is rather difficult to deposit because it requires heat in excess of 1700°C. Also, it absorbs very little radiant energy when heated in vacuum.

Tantalum, Titanium, Aluminum, and Niobium

Some oxidized metals can be used as dielectrics for film capacitors with desirable characteristics. Aluminum, titanium, tantalum, and niobium are most commonly used in this category. They are deposited on the substrate to the desired thickness by either sputtering or evaporation. This layer forms one conducting electrode of the capacitor. The dielectric is formed by anodizing the surface of the film. The anodizing process is very finely controlled to yield the proper thickness of the desired dielectric and to insure that no pinholes are left. Another metal layer is now deposited to give the counterelectrode of the capacitor. Gold is commonly used for this purpose, and the resulting capacitor is polar. Nonpolarized capacitors may be fabricated by using the same metal as the anodized material for the counterelectrode. Tantalum-oxide capacitors are capable of giving 0.5 to $5\mu f/in.^2$ with voltage ratings varying from 50 to 2 volts/$\mu f/in.^2$, and temperature coefficient of 250 ppm/°C. Aluminum oxide has almost twice the working voltage as that of tantalum, but its dielectric constant is only about a fourth or less than that of tantalum-oxide capacitors.

Deposited Ferroelectrics

Deposited ferroelectrics as dielectrics for thin-film capacitors offer some interesting but limited possibilities. Work in this field is still in the purely experimental stage, but its main advantage is that barium titanate has a dielectric constant which is about three orders of magnitude higher than that of silicon oxide. Deposited ferroelectric dielectrics can give nonlinearity and capacitors which can be polarized. Limited operating temperature range and unstable electrical properties are the main drawbacks.

Thermal Oxidation

A hybrid type of capacitor can be obtained by thermally growing an oxide layer on a semiconductor substrate. The semiconductor material forms one electrode of the capacitor. The other electrode is a thin metallic film deposited on the oxide.

4.4 INDUCTIVE ELEMENTS

Deposited Nickel-Iron Films

Deposited films, composed of about 80% nickel and 20% iron and thicknesses varying from 1000 to 4000 Å, have been used for storing energy from the flow of current. Logical matrices and low-frequency inductors with low-inductance values are some of the typical applications of these films. During the deposition process, it is sometimes desirable to provide a magnetic field to cause magnetic anisotropy of the film. If a drive current is applied such that the resulting magnetic field has the same direction as the "easy" magnetization of the domains, a square-loop B-H curve results. This property is utilized in logic and memory applications. If the drive current is applied such that the resulting field is normal to the "easy" direction of magnetization, a more linear B-H curve is obtained, and which is more suitable for linear applications.

Deposited Ferrites

Mixture of metal oxides, deposited by pyrolytic decomposition at near 300°C temperatures, results in ferrites which have some desirable properties for obtaining thin film inductances. Ferrites do not have the same magnetic anisotropy as nickel-iron films. Consequently, they do not need an orienting magnetic field during deposition. Frequencies up to 500 kilocycles have been achieved using manganese-zinc ferrites. Nickel-zinc ferrites have been able to extend the frequency range from 500 kilocycles to 100 megacycles. The permeability of ferrites can be varied by the application of a d-c magnetic field. This gives a convenient method of controlling the a-c magnetic field thereby providing a variable inductor.

Ferrite Substrates

Another possibility of using ferrites is to fabricate the substrate itself out of ferrites with either single or multiple apertures. The apertures serve as inductive cores with the rest of the ferrite material serving as a substrate for other thin-film components. To date, very limited work has been done with this approach.

Air-Core Geometries

This technique involves the deposition of air-core-type winding layers of thin-film conductors on substrates. High-frequency inductors with small values have been successfully deposited. It is possible to increase the total inductance by sandwiching the winding layers between thin-film insulators of low dielectric constant.

4.5 CONDUCTION BETWEEN CIRCUIT ELEMENTS

Vacuum Evaporation

At high temperatures, metals can be deposited in high vacuums by evaporation to give very satisfactory conducting paths between circuit components on substrates. To insure good adhesion of the vapor, it is necessary that the substrate be clean and that it be raised to a high temperature. Masks are used to deposit selectively along the desired paths. Either a single metal or an alloy can be deposited. One technique of depositing an alloy consists of simultaneously depositing the metals from a common source. Another method is to first deposit one metal followed by the deposition of the second one. This of course merely deposits one layer on top of the other. The substrate is then heated and the alloying of the metals takes place on the substrate itself.

Sputtering

This process is actually a glow discharge between an inert anode and a bombarded cathode of the required conducting metal. The ionized bombarding molecules are generated by the presence of a gas in high vacuum. One inherent advantage of this process over the vacuum evaporation process is that sputtering requires relatively low temperatures and this reduces the possibility of contamination from the evaporating source.

Pyrolysis

This process consists of thermal decomposition of a volatile compound into volatile and nonvolatile by-products and is usually carried out in an inert carrier gas. This process is particularly suitable for applications where the whole surface has to be coated, such as for magnetic or electrostatic shielding, or where the undesired conducting surface can be selectively removed after the initial deposition. Pyrolysis has the disadvantage that masks cannot be used during deposition.

Plating

Vapor, chemical, and electroplating are often used for the fabrication of conducting paths. Vapor plating tends to cover the entire surface area but results in a deposition with extremely high purity. One major short-coming of electroplating is its tendency for contamination.

Coating

Vapor depositions sometimes leave irregularities in conductive plates which may adversely affect the yields. These irregularities can

sometimes be readily remedied by mechanically coating the affected area. The materials most commonly used are conductive glass pastes and solders of various types. Glass pastes have the ability to bond well on several substrate materials. They also have coefficient of thermal expansion which can be made to match reasonably with those of the substrate material.

4.6 CIRCUIT AND COMPONENT ISOLATION

Anodization by Electrolysis

An insulating oxide layer can be easily formed on such metals as tantalum, titanium, aluminum, and niobium (which are commonly used in thin-film work) by electrolytic action. Since this process is very precisely controllable, it is often used in applications where the conducting base metal needs to be protected by an insulating layer. Some of the insulating layers obtained by anodization, such as tantalum films, are often used for dielectrics in film capacitors since they have a high dielectric constant.

Pyrolytic Decomposition

This is essentially the same process that was previously discussed under circuit-conducting elements. Silica, glasses, and silicone polymers are some of the materials which have insulating properties and which have been successfully deposited.

Vacuum Evaporation

Insulating layers have also been deposited by evaporation in high vacuums. The insulating material is thermally released from the evaporating source. Silica-insulating films have been produced by electron bombardment of the parent material. This technique easily lends itself to deposition by mechanical masking.

Plasma Deposition

Highly excited atomic particles of the insulating material can be deposited by spraying. High temperatures are required for the excitation, and this is the main disadvantage. However, this technique has the advantage that almost any elementary material can be deposited on most substrates by this method.

Coating

Either organic or inorganic insulating materials can be used by physical application, such as spraying. Insulating films with dielectric strengths of 10^6 volts/cm or greater with thicknesses of 10 μ or more have been deposited.

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Integrated circuit fabrication process—a brief description

5

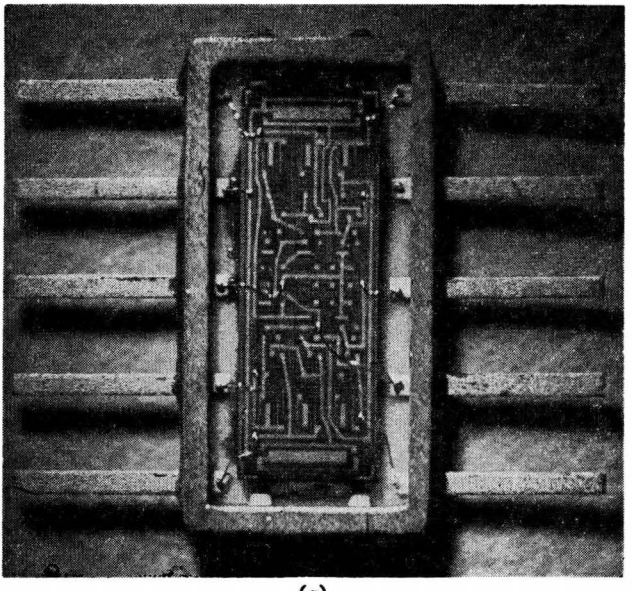
In Chapter 3, the fundamental semiconductor processes were briefly presented. The dynamic nature of this new field makes some unusual demands on the user of these units. Manufacturing and fabrication techniques play a very prominent role in the capabilities and final performance of integrated networks. It behooves the circuit and the systems engineers, particularly the newcomers to this field, to acquaint themselves with these techniques. A guided tour through one or more manufacturer's facilities would unquestionably be the most desirable procedure. Since this is hardly a practicable situation for most engineers, it is hoped that the information in this chapter will give them at least a convenient starting point. The fabrication steps presented here are basic to semiconductor integrated circuits. Figure 5.1 shows two fully integrated circuits in typical packages with caps removed, which are representative of the end products one would see on such a tour.

5.1 ZONE REFINING

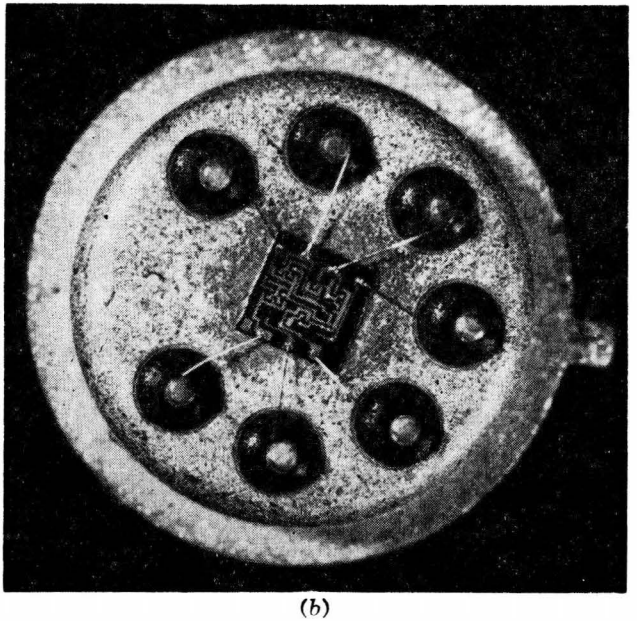
Polycrystalline silicon, used for diode and transistor manufacturing, is also the basic raw material for semiconductor networks. Since the quality and performance of the final product is greatly dependent on the purity of the intrinsic material, the contaminating impurities are segregated by the *zone-refining* technique. Initial control over the impurities is obtained by processing the raw silicon at high temperature.[1] The material is then subjected to intense heat applied by high-frequency induction-heating coils. This forces the impurities to flow toward those regions within the material which have not been exposed to the high-frequency field. At this point, conductivity measurements are made to determine the purity of the raw material.

5.2 CRYSTAL GROWING

The refined and tested material is now ready for crystal growing. This process, known as the Czochralski method,[2] consists of first melting the material at a temperature of about 1200°C in a specially equipped furnace. A small perfect "seed" of silicon crystal is attached to a chuck on a rod inside the furnace. The seed crystal is lowered in



(*a*)



(*b*)

Fig. 5.1 Typical fully integrated semiconductor circuits. (*a*) The SN511 flip-flop counter network with emitter-follower output (courtesy Texas Instruments, Incorporated). (*b*) The μLC "Micrologic" counter adapter element (courtesy Fairchild Semiconductor, Inc.).

the molten silicon. The rod is then slowly pulled out from this melt at a precisely controlled rate of withdrawal and rotation. The resulting cylindrical ingot is about 1 in. in diameter and 6 in. long. During this process, the proper dopant is introduced to make the resulting ingot have the desired *N*- or *P*-type material characteristics.

To determine the success of this process, tests are usually made at this point to establish the average time interval of the charge carriers available for conduction. By measuring the time it takes for the thermally generated mobile electrons, or holes, to recombine with the majority carriers, the lifetime of the material can be determined.

5.3 SLICING AND POLISHING

The next step consists of cutting the large single crystal ingot into wafers whose thickness is usually on the order of 8 to 10 mils. The equipment used in this operation consists of a diamond saw. Each wafer or slice is polished by a lapping process using a very fine grit abrasive, and the debris is cleaned off to prevent the possibilities of contamination.

The lapping process results in a slice with a highly polished surface and uniform thickness. The wafer is further reduced in thickness to about 3 to 5 mils by a chemical etching process. Each wafer is now subjected to a four-point testing procedure for resistance measurements. This is usually the final test for acceptance of the slices before proceeding with the diffusion process. This test consists of probing the surface of each wafer with a four-point probe for reading resistance measurements on meters.[1] A current, usually about 1 ma, is passed through the wafer by the two outer probes. The two inner probes pick up the floating potential, which is measured and read on the meters.

5.4 EPITAXIAL GROWTH AND SURFACE PASSIVATION

In the earlier versions of integrated circuits, surface passivation was not used much since the planar techniques were relatively new. However, the state-of-the-art has advanced to the point where most of the semiconductor manufacturers either have perfected the planar and epitaxial techniques, or will do so in the very near future. At this time, it is pretty well established that these two processes are indispensable to integrated circuits.

A layer of high-resistivity material is epitaxially grown on the low-resistivity substrate wafer. This wafer becomes a single crystal extension of the substrate and provides a *P-N* junction where the layers join. Several wafers, with epitaxial layers, are now placed in a

furnace containing an oxidizing atmosphere at high temperature (usually about 1200°C). The oxygen in the atmosphere combines chemically with the silicon atoms at the surface to form a stable compound of silicon dioxide. The advantages of both the epitaxial and planar processes are covered in Chapter 3 and will not be repeated here.

5.5 ISOLATION MASKING

The next step is to provide electrical isolation of the circuit components from each other. The oxidized wafers are now coated with a photoresist, a chemical which is sensitive to ultraviolet light, in a darkroom. A high-resolution mask containing the component isolation pattern is then aligned on the wafer using a stereomicroscope mounted on a fixture which is capable of positioning the wafer on two axes. The portions of the photoresist which are not covered by the mask are now exposed to ultraviolet light. To avoid misalignment of the mask on the wafer, the photoresist is exposed to the ultraviolet light through the same lens that is used in aligning the mask.

The exposed parts of the photoresist are soluble and are washed off by a solvent rinse. An acid etch is now used to dissolve the oxide coating from the area not protected by the film of photoresist. In this way, narrow bands or "windows" are photoengraved through the oxide coating. These are such that they surround the areas which will be used for components diffusion in subsequent processes.

5.6 FIRST DIFFUSION FOR ISOLATION

Several manufacturers today start out with a *P*-type substrate, and epitaxially grow an *N*-type layer which is then coated with a protective layer of silicon dioxide (Fig. 5.2). The *N*-type epitaxial layer is the one of primary interest, as that is the material in which the integrated-circuit components will be diffused.

At this point the intention is to create islands of *N*-type material in the epitaxial layer isolated by *P*-type material. The wafers with etched-away oxide coating are now placed in a special high-temperature furnace. A carrier gas flows into the furnace inlet at a controlled rate.

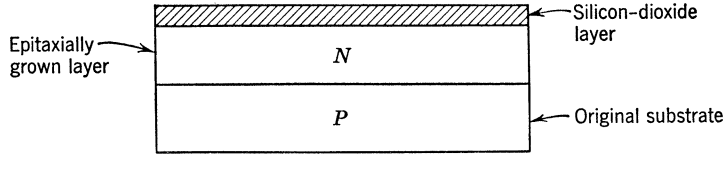


Fig. 5.2 Initial wafer for integrated circuit.

This atmosphere contains the evaporated diffusant, such as boron. The dopant diffuses into the surface of the silicon wafer at those areas which were exposed by the previous photoengraving process. By controlling the diffusion time, the dopant concentration, and the temperature within the furnace, the doping impurity can be made to penetrate to a predetermined depth. The resulting profile of the wafer is shown in Fig. 5.3*a*. For purposes of explanation only, three isolated *N* regions are shown. Actually there can be any number. During this same process, the areas where the original silicon dioxide was etched away are recoated with another new layer formed by surface oxidation. Each diffusion cycle results in a definite configuration of the various circuit areas. The results of the diffusion processes are evaluated by determining the location and width of the various *N-P* junctions penetrating the surface of the wafer by means of a hot-point probe. After each diffusion cycle, the wafers are subjected to a vapor-cleaning procedure which dissolves and removes the fine particles of foreign matter which usually accumulate during handling of the wafers.

5.7 SECOND DIFFUSION FOR TRANSISTOR BASE AND RESISTOR

The isolated *N*-type regions resulting from the previous step constitute the collectors of the transistors used in the integrated circuit. If a hypothetical circuit calls for one transistor, one diode, and one resistor, the three *N*-type regions (Fig. 5.3*a*) can be utilized for all three components from that point on. The re-oxidized wafer is again coated with photoresist, and another mask, containing the transistor base and resistor patterns, is used. The previously described process is repeated, and the resultant profile is shown in Fig. 5.3*b*. The dopant used in this second diffusion process is such that the newly diffused areas are now *P*-type. As far as transistors are concerned, these are the *P*-type regions. The doping level of the transistor base is usually such that the resistivity of the diffused area is a convenient value for use as diffused resistors. As in the first diffusion cycle, the etched-off areas of the wafer are reoxidized. Assuming that the original *N* regions were earmarked (as indicated in Fig. 5.3*a*), the *P*-type region of area 2 would be the desired resistor of the circuit, which for all practical purposes is completely isolated from both the transistor area 1 and the diode area 3 by the surrounding *N* region, which in turn is isolated by the *P* region.

5.8 THIRD DIFFUSION FOR TRANSISTOR EMITTER

The reoxidized wafer is now subjected to a third diffusion cycle, which is similar to the previous two except that a different pattern is

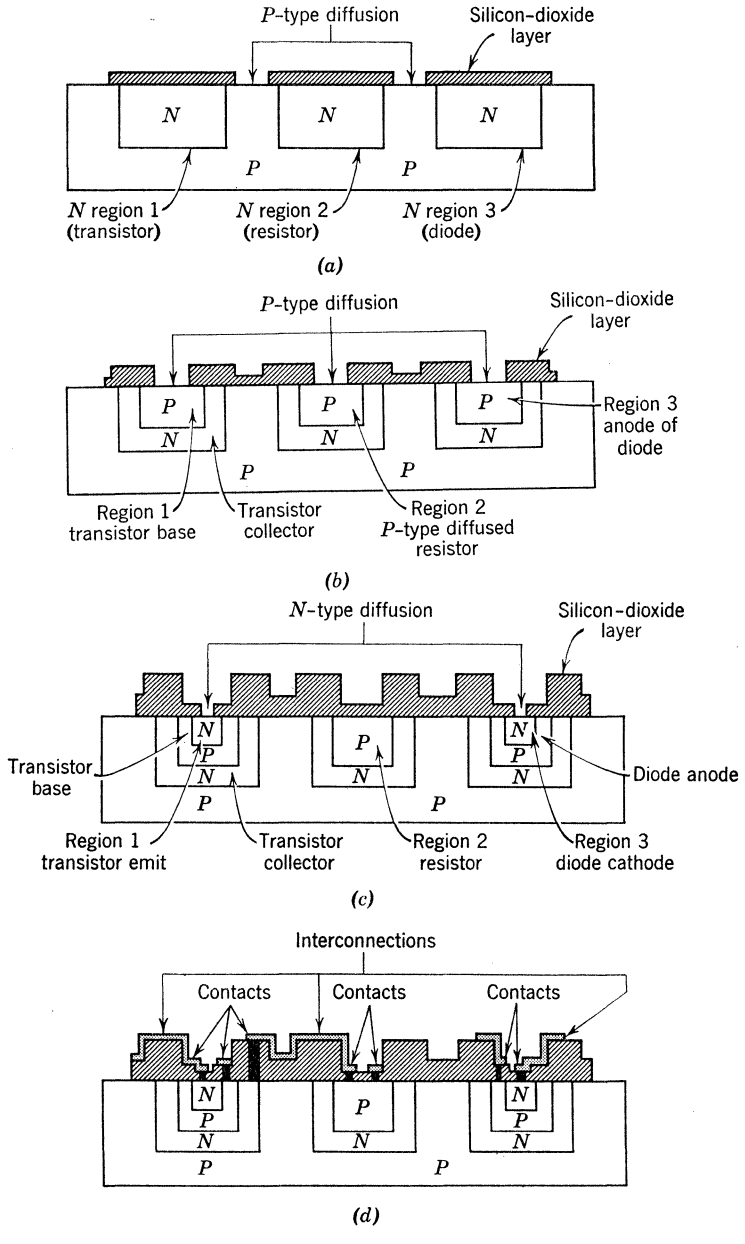


Fig. 5.3 (*a*) First diffusion process creates isolated *N* regions. (*b*) Second diffusion creates transistor base, *P*-type diffused resistor and anode of diode. (*c*) Third diffusion creates *N*-type transistor emitter and diode cathode. (*d*) Evaporated contacts and interconnection patterns.

used in the mask and the impurity used in the diffusion-process results in the formation of the *N*-type regions in the transistor and diode areas 1 and 3. The mask pattern is such that area 2 is left as it is. The newly formed *N* regions are in the emitter regions for the transistor or the cathode regions for the diodes. Once again the oxide coating is formed as the diffusion process takes place; the resulting cross section is shown in Fig. 5.3*c*.

5.9 OHMIC CONTACTS FOR INTERCONNECTIONS

Having diffused the various circuit elements in the silicon wafer, the next problem is to connect these in the desired circuit configuration and to provide some means of making the circuit nodes externally available. Using the photoengraving technique, holes are etched in the oxide coating over the appropriate locations of the circuit components. Once again a mask is positioned accurately over the wafer and the wafer is subjected to a metalization process in a high-vacuum chamber. Evaporated aluminum (and/or gold) is deposited as a thin even coating through the metal mask. Some manufacturers follow a slightly different process. Here the areas are etched off by a photoresist process. Figure 5.3*d* shows the contacts and an interconnection pattern deposited on the oxide layer.

5.10 WAFER SCRIBING AND DICING

At this stage each wafer contains a large number of integrated circuits. The wafer is now mounted on a thin steel plate which is then positioned on precision scribing equipment. Each wafer is then scribed with a gridlike pattern using a diamond scribe.[3] The wafers are then chipped or diced into individual units in a dicing machine which applies controlled mechanical pressure on the wafers. After this operation, the individual circuit devices are cleaned of debris and foreign matter and then functionally tested using micromanipulators. During these tests, the actual operating parameters are tested. Simultaneous processing of a large number of potential circuits on each wafer, and also a large number of wafers in a batch, results in fairly good yields with a high degree of uniformity, thereby increasing the volume and consequently lowering the cost.

5.11 DIE MOUNTING AND THERMOCOMPRESSION BONDING

The individual integrated circuit is now ready for packaging. At the present time, the most commonly used package for these units is the time-honored TO-5 transistor package. It is a well-designed and proven package, and one which is readily available at a fairly low cost. Several different techniques are employed for mounting the die on the

TO-5 header. In the earlier days, each die was mounted directly on the gold-plated header.[3] Some manufacturers mount the die first on a ceramic disc and then to the TO-5 header by means of a high-temperature eutectic solder.[4] Although TO-5 is a widely used package today, there are many arguments in favor of other geometries. One package, which is rapidly gaining wide acceptance, consists of a flat rectangular shape, 250 mils × 125 mils × 35 mils, with a 5 mil tolerance on each dimension. This package has 5 leads laterally protruding from each of its longest edges. The TO-5 can usually has 8 leads along the periphery of its header, although 10 leads are possible. Irrespective of the type of package used, short gold wires, usually 1 mil in diameter, are now bonded to the input, output, and power supply pads of the circuit using the thermocompression technique, which connects the lead wire to the pad under pressure at high temperature. The capillary ball-bond is widely used, although several vendors are also using the wedge-bond technique. The other ends of the gold leads are spot-welded to the header posts or the flat connection pins.

5.12 HERMETIC SEALING

Prior to final capping of the units, each unit is given a final visual inspection to insure that the die has not been damaged during the mounting and bonding operations. Then the unit is washed and dried in a vacuum chamber. This removes residual moisture and prevents it from being encapsulated in the case. In the same chamber the can, or the flat cover as the case may be, is welded on the header or the lower part of the flat package, thereby covering and sealing the unit. Electrical tests are normally conducted at this point before environmental testing of the units. Most manufacturers make environmental tests, such as temperature cycling, mechanical shock, and centrifuge-acceleration tests, to conform to military requirements. The units which meet these tests are given electrical tests, which usually contain worst-case functional operation tests.

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section 3

The fully integrated circuit

Integrated circuit elements and their characteristics

6

"I can't use the integrated circuits offered by the vendors as off-the-shelf items. My applications call for different special circuits. Can they build them?" "My present circuit is fairly complex. How can I simplify it so that vendor X can integrate it for me?" "What are the vendors' scope and limitations on what they can integrate?" "What devices can I use for my integrated circuits?" "Can they put a one ohm resistor, a one megohm resistor, and a one microfarad capacitor on the same silicon wafer?"

These questions, and other similar ones, constantly confront the circuit designer, particularly the newcomer to this field. The vendors are, of course, constantly plagued with innumerable such queries. Unfortunately for the circuit designer, no single source at the present time can satisfactorily answer such questions, since the field is still so new. To make matters worse, there are no rigid design rules that could be universally applied. Design guidelines vary from one vendor to another and, to some degree, from one application to the next. Besides, the industry is moving so fast that newer techniques and fabrication processes make several present-day concepts antiquated very rapidly. Unquestionably the circuit designers' best hope is to keep up with the state-of-the-art in the literature and backed up by close personal contacts with the vendors. This chapter and the ones following are intended to help the circuit designer get off to a good start. The material presented here is based on the currently available information and therefore should be used only as guidelines. These guidelines are general and applicable to present-day vendors within reasonable limits. The circuits offered as standard product lines of the principal vendors form the subject material of an appendix.

6.1 CIRCUIT ELEMENTS FOR INTEGRATED CIRCUITS

Transistors

SILICON PLANAR EPITAXIAL TRANSISTORS. From the discussions in the previous chapters it is self-evident that the transistor is perhaps the one circuit element most suitable for integrated networks. In fact, the entire integrated-circuit concept evolved out of transistor technology. Although the transistor is very adaptable for integrated

circuits, it also presents some problems. Regardless of whether the through-diffusion or the triple-diffusion method is employed for transistor collector isolation, the end result is a *P-N* junction, which is reverse-biased for the most effective isolation. The net effect of this is that an additional isolation diode is tied to the collector node (Fig. 6.1*a*). This diode adds an undesirable additional leakage current to the collector node, which, while usually small, may be a source of potential trouble in some circuits, thus it must be taken into consideration during circuit designing. The actual value of this leakage current can only be supplied by the vendor, since it would depend on such factors as the area of the *P-N* junctions in question and the doping levels. Often the anode of the isolation diode may be tied to ground potential, if that happens to be the most negative potential in the circuit. Since a reverse-biased diode acts like a capacitor, it is tantamount to adding a capacitor from the transistor collector to ground. This collector to header capacitance can be as large as 70 pf, although it is usually considerably lower and becomes a very critical factor in high-speed switching circuits. There is still another problem associated with transistors in integrated circuits. Previously we saw that because the anode of the isolation diode is located on the underside of the wafer, the contacts for the collectors have to be made on the top. Because of this, it is difficult to obtain low collector-to-emitter saturation voltage with integrated transistors. The principal advantage of transistors in integrated circuits is that, two or more transistors of the same circuit can be fabricated from the same process, and so their electrical characteristics can be matched very closely. The circuit designer would undoubtedly attempt to take advantage of this phenomenon and come up with some ingenious ideas. In general, we can say that the transistors available in vendors' standard product line can be readily used in integrated circuits, provided their geometries are such that they are within the size limitations of the silicon wafer.

This description is somewhat simplified and for most practical purposes is an adequate picture. A closer examination shows that a considerably more complicated equivalent circuit could be obtained. A simple *NPN* transistor (Fig. 6.2*a*) in reality becomes a four-layer *NPNP* device. The equivalent circuit model of such a device is shown in Fig. 6.2*b*.

In Fig. 6.2*a*, it is seen that regions 1, 2, and 3 form the desired transistor Q_1, while regions 2, 3, and 4 form the undesired *PNP* transistor Q_2. The collector of Q_1 obviously has the collector resistance R_{C1}. The base resistance R_{B1} of Q_1 has a distributed capacitance to its emitter, shown as C_{EB1} in Fig. 6.2*b*. Since the *N*-type collector of

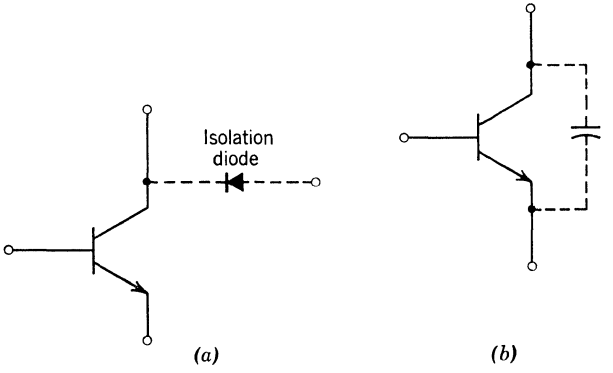

Fig. 6.1 The integrated transistor and its isolation diode: (*a*) Isolation diode tied to collector node. (*b*) Collector-to-header capacitance due to the reverse-biased isolation diode.

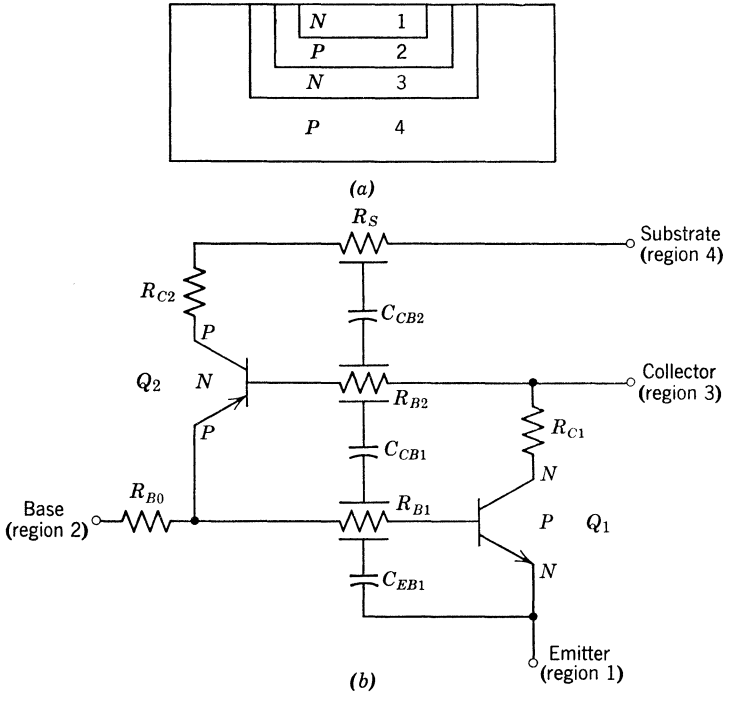

Fig. 6.2 (*a*) Simple *NPN* transistor in integrated form becomes a four-layer *NPNP* device. (*b*) A more exact equivalent circuit of the integrated *NPN* transistor (in four-layer form).

Q_1 is also the base of Q_2 (region 3), a distributed capacitor C_{CB1} also exists between R_{B1} and R_{B2}. Similarly, a distributed capacitance C_{CB2} is also present between R_{B2} (region 3) and the substrate resistance R_S (region 4).

THE UNIPOLAR OR THE FIELD EFFECT TRANSISTOR. The field effect transistor is one semiconductor device which may have some very interesting possibilities in integrated networks, particularly in logic applications for digital computers. While some experimental work in this area has been reported, the full possibilities have not yet been extensively explored by the vendors.[1] Figure 6.3 shows the field-effect transistor in its simplest form. This is one of the earliest forms of the field-effect transistor. The device of the future to be used in integrated circuits certainly will not have the etched channel, but will undoubtedly contain more sophisticated fabrication approaches. For purposes of explanation, the etched-channel form is considered here. Basically, the device consists of a *P-N* junction with a narrow channel constricted on the *N*-type layer. The *N* material on either side of the channel serves as the current source and the current drain, respectively, while the *P*-type material is the control gate. When a reverse bias is applied to the gate, the depletion layer of the *P-N* junction, which is usually less than 1 mil thick, grows and spreads onto the channel region and makes it narrower. As a result, the source to drain resistance increases. It may be as high as 100 megohms. When the reverse bias on the gate is reduced, the depletion layer reduces, thereby reducing the source to channel resistance to about 5 kilohms. This transistor is in essence a voltage-operated relay and since its high-frequency cut-off is on the order of 10 megacycles, it can be used in the high-speed logic systems. Wallmark and Marcus[1] report a four-input AND circuit consisting of four directly-coupled unipolar transistors logic (DCUTL) as shown in Fig. 6.4*b*, performing the logical function shown in 6.4*a*. The monolithic circuit consists of

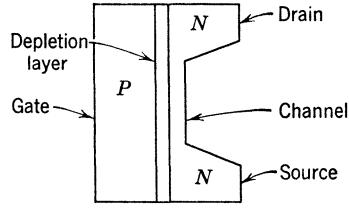

Fig. 6.3 Simplified diagram of the unipolar or the field-effect transistor.

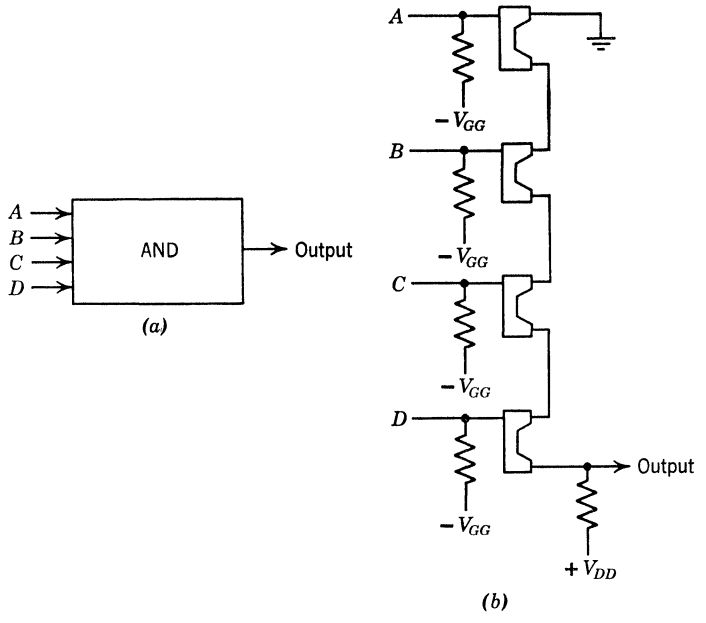

Fig. 6.4 The DCUTL multiple AND gate. (*a*) The logical function. (*b*) The circuit configuration.

four active unipolar devices and one passive element to serve as the load resistance. The operation of the circuit is simple. In the absence of gate signals, all gates are negatively biased, and thus all the transistors are OFF. When a less negative voltage is applied to any gate, the corresponding channel resistance reduces to a low value and turns that particular gate ON. The output voltage, however, remains positive. In logic systems, it is necessary to amplify and reshape the signal after it has propagated through several stages. With the unipolar transistor it is found that very little signal deterioration takes place even after several stages. Another desirable feature is that these elements inherently do not amplify signals below a certain level, thereby providing excellent noise rejection.

Diodes

THE PARASITICS ASSOCIATED WITH INTEGRATED DIODES. In integrated circuits, the diode is a very easy element to fabricate, since either the base-emitter or the base-collector junctions of the transistor can be used for the purpose. A low-voltage diode is obtained by using

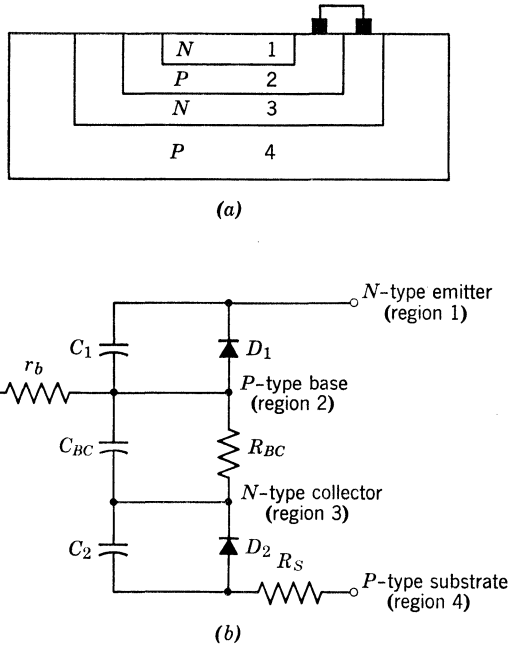

Fig. 6.5 Parasitics associated with the base-emitter type integrated diode. (*a*) Integrated diode using the base-emitter junction of the transistor. (*b*) Equivalent model of base-emitter type diode.

the base-emitter junction, whereas a medium-voltage diode is available by using the base-collector junction. Figure 6.5*a* shows the cross-sectional view of a transistor structure for obtaining the base-emitter-type integrated diode. The collector and the base of the transistor are externally shorted out. This results in a lower forward voltage drop and a relatively fast recovery time.

The equivalent circuit of the structure is shown in Fig. 6.5*b*. The collector is shorted to the base, and this is represented by an equivalent resistance R_{BC}, which is in series with the emitter-base diode D_1, and the collector-substrate diode D_2. The series resistor r_b is the same value as the r_b of the transistor. The base-emitter diode has a distributed capacitance, C_1, across its junction. Similarly, the collector-substrate diode, D_2, also has a distributed capacitance, C_2, across its junction. R_s is the series substrate resistance. Although regions 2 and 3 (base and collector) are shorted out and no direct diode action

takes place, a distributed capacitance, C_{BC}, nonetheless exists across the equivalent resistance R_{BC}.

COMMON CATHODE ARRAYS. In digital work, arrays of diodes are often required with either their anodes or their cathodes tied together. If the base-collector junctions are used, it is a simple matter to obtain an array of diodes with their cathodes tied to a common node. Irrespective of the method used for isolation, either through-diffusion or triple diffusion, common cathode arrays have only one isolation diode tied to the cathode of the array. Figure 6.6*a* shows a cross-sectional view of the silicon wafer containing a common cathode array of three diodes. Figure 6.6*b* is a schematic representation of this arrangement, together with the isolation diode. Both the N and P diffusions for the diodes' cathodes and anodes are done at the same time as the collector and base of the transistors on the same wafer.

COMMON ANODE ARRAYS. At the present time, NPN transistors are widely used in integrated circuits, although PNP transistors are, of

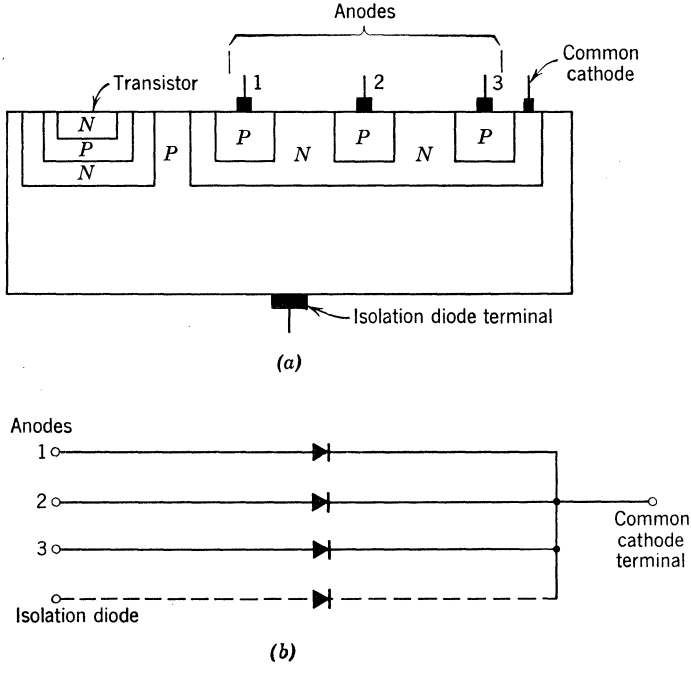

Fig. 6.6 Common-cathode diode array. (*a*) Cross-sectional view of the silicon wafer. (*b*) Schematic representation.

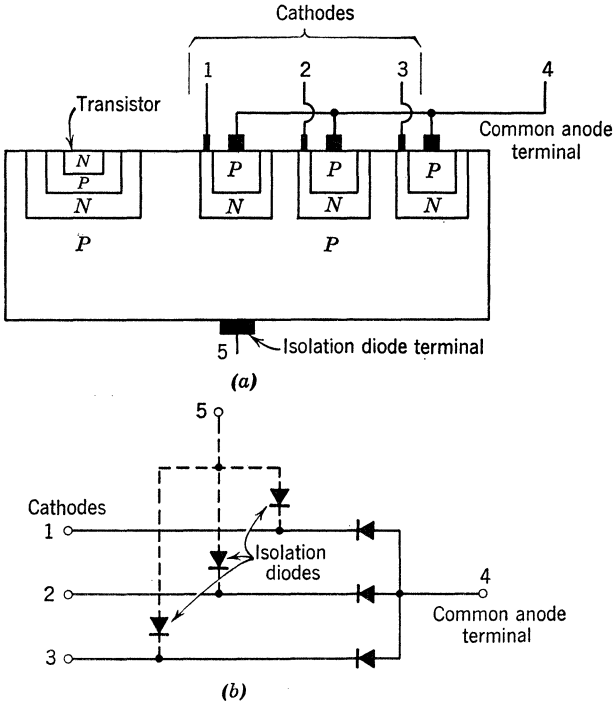

Fig. 6.7 Common-anode diode array. (*a*) Cross-sectional view of silicon wafer. (*b*) Schematic representation.

course, possible. If the N-type base diffusions are to be utilized for the fabrication of a common anode array, the problem is not quite as simple as in the previous case of the common cathode array. In this instance it would be impossible to use the N-type collector diffusion for the diode cathode and a common P-type base diffusion for the common anode of the array. To avoid all the cathodes from being tied together, it is quite apparent that each diode's cathode would have to be an individually isolated N-type region (Fig. 6.7*a*). This results in each diode having its own isolation diode and the anodes of the isolation diodes are all tied to a common terminal. The schematic representation of Fig. 6.7*b* shows this. Here, the anodes of the diode array are tied together by some means external to the silicon wafer, usually by a deposited interconnecting pattern.

Another possibility is to use the N and P diffusions of the transistor emitter and base, respectively, for the common-anode diode array

(Fig. 6.8*a*). This arrangement assumes that the base-emitter characteristics of the transistors in question are suitable for the diodes in that particular circuit application. While this method gives adequate isolation, the reader will readily realize that an additional problem is in the offing as far as the circuit designer is concerned. Regions 3, 2,

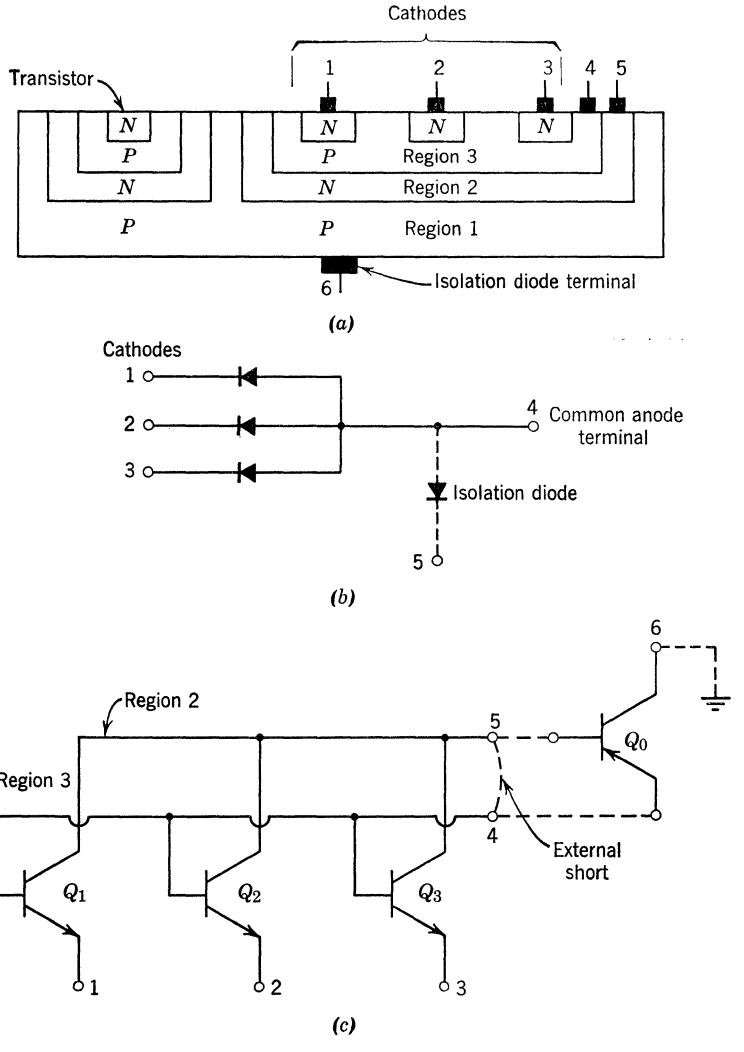

Fig. 6.8 Common-anode diode array. (*a*) Cross-sectional view of silicon wafer. (*b*) Idealized schematic representation. (*c*) Actual schematic representation.

and 1 of Fig. 6.8*a* form a *PNP* transistor. While the idealized model of this arrangement is as shown in Fig. 6.8*b*, in reality, each diode is a combination of the transistors having three separate *N*-type emitters with a common base and a common collector. Figure 6.8*c* shows this configuration. A further complication arises due to this *PNP* transistor, T_0, because its base is effectively connected to the common collectors of T_1, T_2, and T_3 while its emitter is connected to their common bases. Terminal 6 of T_0 would be normally at ground. At room temperatures, T_0 is not likely to cause any trouble, but at higher temperatures the leakage currents of T_0 may increase significantly and affect the normal operation of the common anode diodes, since the *P-N* junctions involved are relatively large. One possible solution would be to short out regions 2 and 3 externally at terminals 4 and 5. This would effectively short out the base-emitter junction of T_0 and in the worst situation, the leakage current of only one *P-N* junction (regions 1 and 2) would be involved.

Capacitors

In integrated circuits the use of capacitors is avoided, if at all possible, mainly because uniquely capacitive elements are virtually impossible to fabricate in truly integrated circuits at the present state-of-the-art. Back-biased *P-N* junctions are used as capacitors in most applications where their use is unavoidable. Deposited capacitors are beginning to be used more and more, but since they are of a hybrid nature, they are covered in a later chapter. In capacitors with back-biased junctions, the depletion layer at the junction functions as the dielectric, and the capacitance of such an element is a function of the width of this layer, the depletion layer width being a function of back-bias voltage and the junction area. Using silicon *P-N* junctions, capacitors up to 200,000 pf/cm^2 with low temperature coefficients and breakdown voltages of several hundred volts have been reported.[3] In actual integrated circuits these values are certainly not practical, since silicon wafers 1 cm^2 are completely incompatible with the commonly acceptable dimensions. More realistic values are 500 pf with 10 volts maximum, although some manufacturers have gone up to 1000 pf.

Several disadvantages are inherently present in reverse-biased junctions used as capacitors. First, the leakage currents are present, which are always undesirable. To obtain larger values of capacitance, the junction areas have to be increased. This in turn increases the leakage currents to the point that they make certain circuits unreliable or even totally inoperative. A second undesirable feature is that the

value of capacitance is dependent on the value of the reverse-bias voltage. This is due to the fact that the width of the depletion layer is a function of the applied voltage. The result is a nonlinear response which, although it can be used to advantage in some applications, is certainly not desirable in most instances. A third drawback of this type of capacitor is that it is polarized; thus it must be insured that it does not become accidentally forward-biased during circuit operation.

The junction-type capacitor has a finite ratio of total capacitance to shunt capacitance in the order of 20:1, which limits its usefulness at high frequencies.[5] In order to increase this ratio, very often a sandwich of two junctions is used. Figure 6.9*a* shows how this is done. Since the integrated transistor is fundamentally a four-layer device, the two *N*-type layers are externally shorted out, and this forms one terminal of the capacitor. The sandwiched *P*-type layer is the other terminal. Such a capacitor has a relatively large capacitance per unit area, about 1 pf/mil.[2] Figure 6.9*b* shows the equivalent model of

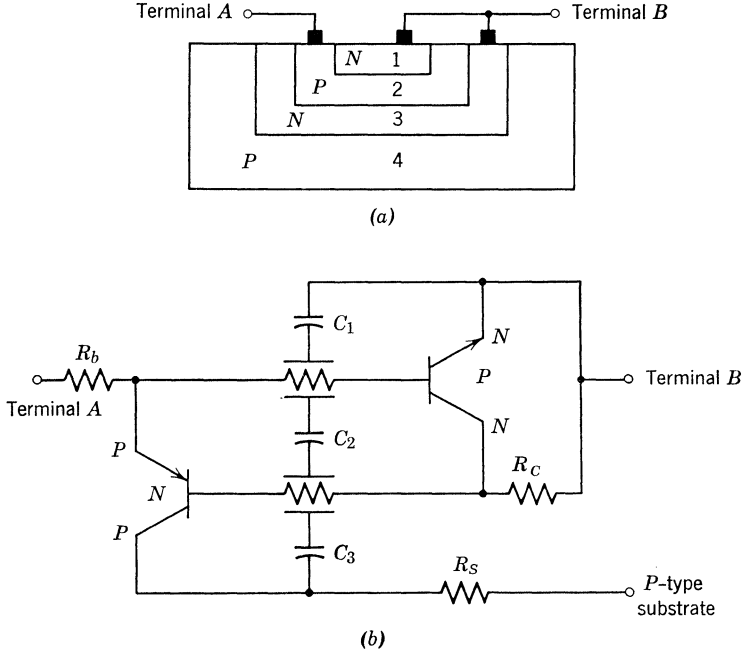

Fig. 6.9 The sandwiched junction-type integrated capacitor. (*a*) Cross-sectional view of the wafer. (*b*) Equivalent circuit.

such a capacitor. The relatively large contact resistance, R_b, reduces the Q of the capacitor.

Resistors

Ohmic contacts made on any homogeneous semiconductor material will make the region between them act like a resistor. Ordinarily, resistors in integrated circuits are made during the same diffusion processes as the emitter, base, or the collector of the transistor. The equivalent value of the resistance is a function of the resistivity of the material (which depends on the doping concentration), the length, and the cross-sectional area of the region. These resistors are linear and follow Ohm's law reasonably well for the low values of voltages normally used in transistor circuits. To obtain larger lengths of diffused areas, these resistors are made of long narrow strips, which are snaked to make maximum use of the limited surface area available on the substrates. The P-N junction formed by diffusion restricts the current flow to the desired resistive region provided the junction is adequately reverse-biased. This type of single-diffused resistor is shown in Fig. 6.10. However, it is sometimes very inconvenient to provide reverse-bias for resistors in some circuits. Also, it may be desirable to have resistors of lower values and lower temperature coefficients than those normally obtained with single diffused types. In addition to the N diffusion (Fig. 6.10), a second P-type region may be diffused in the N region (Fig. 6.11). We can easily see that now no reverse-biasing is required, since the N region provides sufficient isolation.

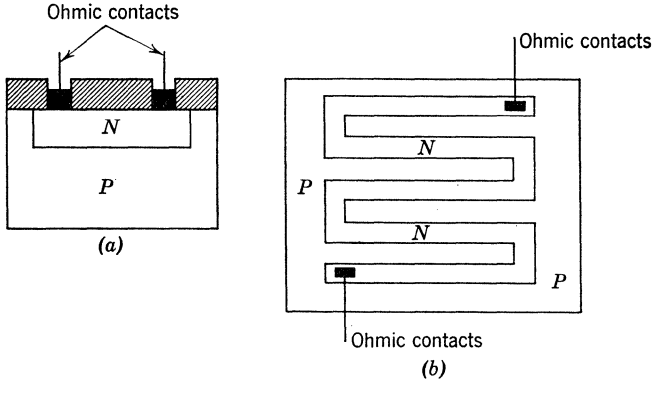

Fig. 6.10 Single diffused integrated resistor. (*a*) Cross-sectional view of substrate. (*b*) Top view showing the snaked N region diffused in a P substrate.

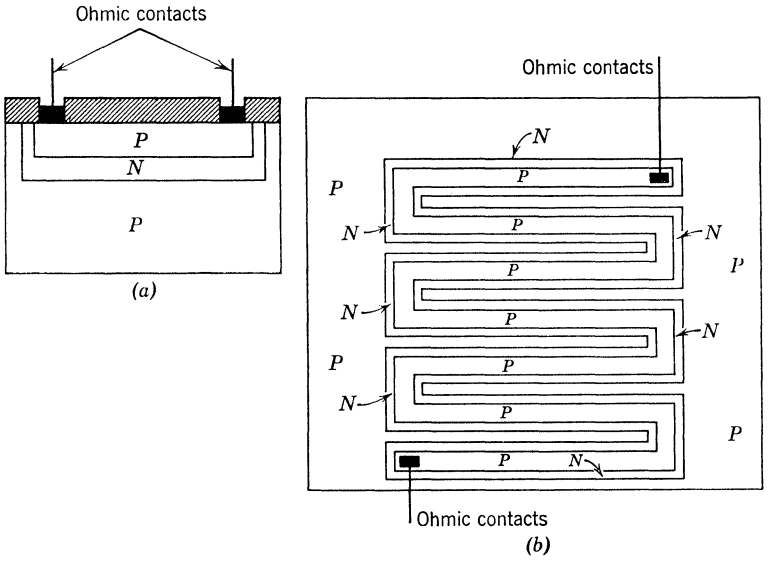

Fig. 6.11 Double-diffused integrated resistor. (*a*) Cross-sectional view of substrate. (*b*) Top view showing the snaked *P* region isolated from the *P*-type substrate by the *N* region.

The diffused resistor has several peculiar characteristics which must be taken into consideration when designing circuits using them. Resistance values in the range of 10 ohms to 100 kilohms have been reported in the literature with tolerances of $\pm 10\%$, and temperature coefficients of 0.2%/°C. A more realistic range is 100 ohms to 30 kilohms with tolerances of $\pm 20\%$ and a maximum power rating of 300 mw.

For any bulk material, the end-to-end resistance R is given by

$$R = \frac{\rho l}{A}$$

where R = resistance in ohms
ρ = resistivity of the material in ohm-cm
l = length of the material in cm
A = cross-sectional area of the material in cm^2

In diffused resistors, the depth of diffusion is very small and constant for practical considerations. Consequently, the value of the resistance is usually expressed in terms of the sheet resistance of the material R',

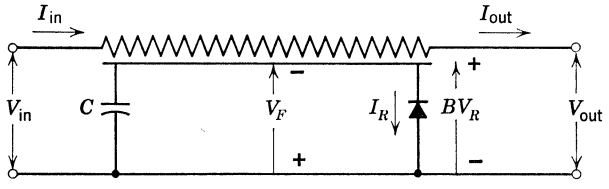

Fig. 6.12 Equivalent circuit of a single diffused integrated resistor.

measured in ohms/square, and the length to width ratio of the diffused area. In the above equation,

$$A = d \times w$$

where d = depth of diffusion in cm
w = width of the diffused area in cm

Therefore,
$$R = \frac{\rho l}{dw} = \frac{R'l}{w}$$

Although the substrate material is usually quite uniform in its properties, differences do exist and show up in diffused resistors. Even when identical geometrical patterns are diffused for two or more resistors on the same substrate, it is found that they differ in their resistance values. It is possible to hold these variations down to $\pm 1\%$, although $\pm 4\%$ is a more practical figure. These resistance changes track quite well over the temperature range. The circuit designer will find it advantageous to utilize resistance ratios rather than absolute values and thereby capitalize on this particular property of integrated resistors.

THE EQUIVALENT DIODE. Since a relatively large junction area is involved, diffused resistors have a diode and distributed capacitance associated with them. Figure 6.12 shows the equivalent circuit of a diffused resistor. According to Howard Dicken of Motorola[2] the typical characteristics of this diode are

Junction leakage current,	$I_{CO} = 10$ mμa
Forward voltage drop,	$V_f = 0.5$ volt
Reverse breakdown voltage,	$BV_R = 50$ volts

THE DISTRIBUTED CAPACITANCE. The distributed capacitance of a diffused resistor is a function of the doping concentration and the voltage across the P-N junction. The capacitance value is given by the theoretical equation

$$C = KV_R^{-1/3}$$

where C = the capacitance
V_R = the reverse bias voltage
K = a constant dependent on the impurity concentration and the diffusion area and depth.

From this equation it is quite apparent that the junction capacitance can be controlled to some extent by the reverse bias voltage applied to the substrate. For this type of a resistor the parasitic capacitance is usually in the range from 0.1 pf/mil^2 to 1 pf/mil^2. A typical 1-kilohm resistor might be 1 mil by 10 mils, giving a distributed capacitance of 1 to 10 pf. This parasitic capacitance is sometimes undesirable, particularly at higher frequencies where it is most troublesome. But in certain applications, such as logic circuits, a small speed-up capacitor is often placed across coupling resistors. The junction capacitance could very easily be used for this purpose. A simple method of doing this is to externally connect the substrate, which is of course isolated from the resistor itself, to one terminal of the diffused resistor (Fig. 6.13). Richard B. Hurley[4] has shown that, when a resistor is connected in this way, approximately one-third of the junction capacitance appears in parallel with the resistor.

TEMPERATURE COEFFICIENT OF RESISTANCE. The temperature coefficient of diffused resistors is a function of the doping concentration of a particular area. Since higher resistivity material would be used for the higher desired values of resistors, the temperature coefficients increase correspondingly. Although the circuit designer may be able to specify the desired temperature coefficients to the vendors, the normal figure quoted by most vendors at the present time is 0.2%/°C and this appears to be a convenient rule of thumb. If the circuit designer specifies the temperature coefficient, it must be remembered that more substrate area may be required for a given value of resistance. Substrate area is always at a premium, and so the circuit designer is seldom at liberty to specify a convenient value of temperature coefficient. Also, in the event of a specified value, a new diffusion may be required.

EQUIVALENT MODEL OF THE DOUBLE-DIFFUSED INTEGRATED RESISTOR. The equivalent circuit considered in Fig. 6.12 applies to the form of integrated resistor shown in Fig. 6.10, where the N-type resistive region

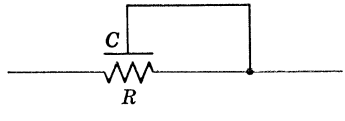

Fig. 6.13 Utilizing the junction capacitance as a speed-up capacitor.

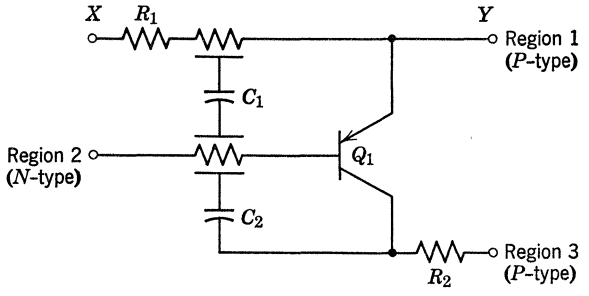

Fig. 6.14 Equivalent circuit of the double-diffused integrated resistor.

is diffused in a P-type substrate. While this is a realistic case and is used in several units, the present trend is more toward the type of resistor shown in Fig. 6.11a involving three PNP layers. The equivalent circuit is now more complicated because of the transistor action involved in such a profile. Figure 6.14 shows the equivalent model.

In this type of resistor, capacitor C_1 is the distributed capacitance of the P-N junction (regions 1 and 2). R_1 is the desired resistance of the snaked P-region 1. Similarly, C_2 is the distributed shunt capacitance of the N-P junction of regions 2 and 3. R_2 is the substrate resistance (region 3). The N-type region 2, which is used for isolating the P-type resistive region, now becomes the base of the transistor Q_1. This transistor has a relatively low beta, 0.5 to 5 according to Howard Dicken of Motorola,[5] but can cause some problems if the P-N junction of the resistor (regions 2 and 3) become accidentally forward-biased. The leakage current between the base and collector or the substrate can be multiplied by the beta of Q_1. Such a current would act like a shunt leakage between R_1 and the substrate. To prevent such an occurrence, region 2 should be maintained at the highest potential in the circuit.

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Integrated circuit design considerations

7

Is designing circuits for integrated fabrication different from designing circuits using conventional components, and if so, how does one go about handling the differences involved? Perhaps, this is the question most commonly asked by engineers who are new to this field. Such a question can hardly be answered with a firm "yes" or "no." The long-established conventional rules and procedures of circuit designing still apply, and so in this manner one could answer the above question negatively. But this is only part of the story. There are additional factors involved with integrated circuits which affect the compromises and trade-offs not normally encountered in designing circuits using discrete conventional components. The designer of integrated circuits cannot afford to ignore them, and thus viewed in this light, the previous question must be answered affirmatively.

Unfortunately, there are no pat ground rules or regulations that an engineer can apply universally to all circuit-design problems. The relative infancy of the field is one reason for this, and the techniques and processes are not yet standardized. They vary from one vendor to another, and consequently the applicable circuit-design guidelines vary. Also, the field is advancing so rapidly that many of the present circuit-design rules could soon become obsolete. It thus appears most desirable for the circuit engineer to be aware of the limitations and peculiarities associated with designing integrated circuits at the present state-of-the art and use them as convenient starting points. The purpose of this chapter is to present the most pertinent considerations involved in designing integrated circuits. The chapter concludes with a description of a typical logic circuit illustrating some of the likely problems and compromises associated with designing integrated circuits.

7.1 DESIGN PROBLEMS UNIQUE TO INTEGRATED CIRCUITS

Interrelations of Circuit Elements

From the circuit engineer's point of view, the components he specifies and uses in his conventional circuits are basically unrelated and independent of each other. Apart from economic restrictions, the circuit designer can specify any components that are optimum for the job.

The components are usually supplied by several different vendors. If the printed circuit boards are laid out properly, no direct interactions take place between the components, except through the conducting paths specified by the circuit design.

Such an ideal situation does not exist in integrated circuits. All the components, as well as the layout for interconnecting paths, are now made by the same vendor. Furthermore, the components are not manufactured independently and separately. In fact, several components are manufactured during the same process steps. For instance, the diodes required in a circuit may be made during the same diffusion process as the base-emitter or the base-collector diffusions of the transistors. Another example is where the resistive regions may be diffused at the same time as the transistor base or the emitter. It is quite apparent from this that the characteristics of the diodes or the resistors, or for that matter the capacitors, too, are not realized independently but are established by the characteristics of the transistors in question.

Fundamental Limitations of Circuit Elements

In Chapter 6, the integrated circuit elements and their inherent limitations are described in detail and will not be repeated here. We might recapitulate here some of the salient points. To date, no significant breakthroughs are reported on integrated inductors; thus the designer would do well to stay away from them. Usually the capacitors are back-biased *P-N* junctions. The capacitance range is somewhat limited and is dependent on the magnitude of the reverse voltage. Resistors are available in somewhat better ranges than they were during the earlier days of integrated circuits. However, resistance tolerances and the associated parasitics are still problems that require careful consideration. Diode characteristics are mainly determined by the transistor characteristics. It is not always possible for a vendor to duplicate all the transistors in his standard product-line in integrated forms, and therefore it is to the designer's advantage to check into the available integrated transistor-type characteristics during early stages of the design.

7.2 THE NEED FOR CIRCUIT SIMPLICITY

Importance of Component Count

COMPONENT COUNT AFFECTS RELIABILITY. One thought often associated with integrated circuits is that because of the batch process of manufacture, component counts as such lose their usual significance.

True, the very nature of the process is such that hundreds or even thousands of additional components can be manufactured with very little additional cost. However, from the circuits point of view, component count is still a major factor. For higher reliability it is always desirable to keep the number of components in a circuit as low as possible. This cardinal rule is applicable to integrated circuits as well as to discrete component circuits. Every additional component requires at least two nodal connections, which can potentially affect reliability, though not to the extent that point connections do in conventional circuits.

COMPONENT COUNTS DETERMINE YIELDS. The yields obtainable in integrated-circuits processes are directly related to component counts, particularly transistors. Low yield is one of the prime factors contributing to the relatively higher prices of integrated circuits, compared to other approaches. Improvements in the technology and better process control will undoubtedly result in better yields and lower prices. In the meantime, the circuit engineer can certainly help the situation by striving for reduced component counts in his designs.

Simplicity Means Reduced Costs

REDUCTION OF PROCESS STEPS. The number of components and the degree of circuit complexity affect costs in another manner, aside from yields. It is quite possible that the circuit engineer may specify values of some components such that they may not be capable of being fabricated during the same steps as the other components of the circuit. They might require one or more additional separate diffusions. In such cases the cost would naturally go up because of the increased number of process steps. Also, any additional steps would affect the yields adversely and thereby increase the cost still further.

SIMPLER INTERCONNECTIONS. Simpler circuits and lower component counts result in another favorable trend for the prices. The complexity of the circuit determines the layout or topology of the components and the metalized interconnecting patterns. The integrated-circuit engineer should be able to determine, prior to the release of the circuit to the vendor, if placement of his components on the substrate will necessitate crossovers in the deposited conducting patterns. Every attempt should be made to avoid such situations. If crossovers are unavoidable, the engineer must take into consideration the effects of resistance and capacitance in the design of the circuit. Once again, simpler interconnections would result in lower costs, perhaps because of smaller number of process steps and better yields.

7.3 DESIGN CONSIDERATIONS FOR TYPICAL INTEGRATED LOGIC CIRCUITS

Performance Capability Requirements

LOGICAL CAPABILITIES. Some of the material in this chapter, particularly in this section, will appear very elementary and even redundant to people in the computer field who are thoroughly familiar with logic circuits. The material is presented principally for those outside the computer field whose main areas of interest do not normally cover digital circuits.

First, the logical circuit in question should have sufficient logical capability. This means that the circuit must perform a certain Boolean operation such as the OR and the AND functions. Also, in order for the circuit to have the maximum utility in the logical organization of the system, or the subsystem, the minimum fan-in and fan-out capabilities are important.

CIRCUIT CAPABILITIES. Closely related to the logical capabilities are other capabilities which may not be directly related to logical operations but are nevertheless very important to the overall system. The noise immunity of the circuit should be large enough so that the noise signals appearing at the circuit inputs do not result in erroneous operation. For modern high-speed systems, the signal propagation delays through logic circuits are a limiting factor. These delays should be kept to a minimum, with power dissipation kept at low levels.

Conflicting Requirements and Compromises

In conventional circuit designs, the engineer usually has to satisfy several conflicting requirements, and as a result his final design winds up with acceptable compromises on several points. In integrated circuits these problems are compounded because the number of conflicting requirements is larger, and the limits on permissible compromises are somewhat tighter. These factors vary considerably from one application to another, as well as between vendors, and so it is hardly possible to establish firm cookbook-type rules. The following points are presented so that the designer may be aware of them during the early phases of the design effort.

Reliability demands that circuits be designed to operate even after component values have varied to their maximum limits in the worst-case directions due to environmental or aging effects. Customarily, this demand is met by a combination of several factors, such as adjusting the circuit specifications so that the circuit output requirements

are relaxed, specifying closer tolerances on power supplies and resistors, and using transistors with higher betas.

When designing circuits for integrated fabrication, the designer is restricted by some additional constraints. He may be able to relax the circuit output requirements to some degree. He may not be able to get the exact transistors that he would like to have. He might have to settle for somewhat lower betas. The biggest problem of course would be the resistor tolerances. Instead of the more desirable closer tolerances, the actual spread would be considerably bigger than even the normally available discrete resistor values. These adverse effects can be partially offset by specifying unusually close tolerances on power supplies. The designer's job has thus become more exacting and challenging.

Minimization of Interconnections

The desirability of reduced interconnections and the resultant advantages were previously discussed. How does one go about reducing them? Once again no fixed easy answer is possible because each circuit application has its own peculiarities and problems. One possibility is the reduction of bias and power-supply connections—in other words, again, simplicity.

Problems due to Peculiarities in Device Technology

PARASITIC COUPLING BETWEEN CIRCUIT COMPONENTS. Perhaps the biggest problem area for the designer of integrated circuits is the possibility of parasitic coupling between various circuit elements. Since the substrate itself is small, the various diffused components are naturally arranged in close proximity to each other. Interacting fields can easily result in parasitic coupling between the circuit elements either through neighboring regions or through the substrate. These coupling effects are usually of a passive nature, but they could be of an active nature also.

The problem of parasitic coupling between circuit elements can be minimized, or even eliminated in some cases, by careful placement of the various diffusion regions. If the circuit is designed such that the node at which logical connections are made has a low impedance to either the circuit ground or the substrate, the effect of parasitic coupling to the substrate can be counteracted.[1]

TEMPERATURE EFFECTS. Thermal effects normally present enough problems in conventional components, but in integrated circuits they can create problems of catastrophic proportions. For instance, the power dissipated in a resistor can generate enough heat to increase

the leakage current in a neighboring region containing a transistor to cause circuit malfunction. Low-power operation and adequate care in component placement might be the only solutions to this problem.

POWER-SUPPLY VARIATIONS. Because of the compromise dilemma faced by the designer (see earlier discussion on conflicting requirements, p. 74), it is necessary that the power supplies used with integrated circuits be stable. However, even the well-regulated power supplies will vary under certain conditions. Since this would often be unavoidable, the ingenious engineer will probably incorporate some scheme for tracking the power-supply voltages.

WIDE TOLERANCE LIMITS. This is one problem that the integrated-circuit designer has to live with, at least at the present state-of-the-art. In some limited applications it may be possible to introduce some kind of compensation or feedback such that the circuit can operate with wide tolerance margins of integrated components.

7.4 A TYPICAL EXAMPLE

This book is not intended as a detailed textbook, or even a handy reference, on circuit design. It is felt that a generalized discussion on a typical logic circuit intended for integration, which would bring out and illustrate some of the salient points discussed before, would be appropos of this book.

The Circuit

Assume that the circuit type decided upon is the low-level logic circuit, LLL, which is discussed in Chapter 9. Also, assume that the circuit requirements are such that the designer has decided to use two coupling or offset diodes, D_C and D_D, in series (Fig. 7.1). Within practical limitations, the circuit could have any number of input diodes. However, we will confine ourselves to only two input diodes

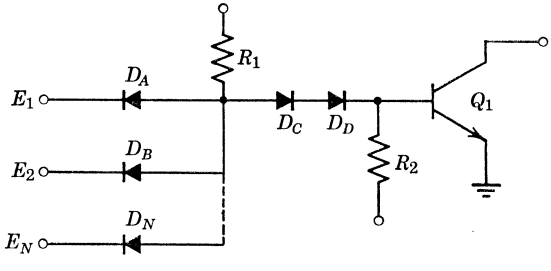


Fig. 7.1 Typical Low-Level Logic gate for integration.

for the sake of simplicity in explanation. Without going into the finer points of circuit design, we may assume that the circuit requirements are such that they are typical and readily realizable by the currently available integrated circuit techniques. We will describe and discuss some of the typical layout problems and possible solutions, which the manufacturers' designers encounter in their work of fabricating this circuit out of a monolithic silicon chip.

Effects of Isolation Diodes

It is assumed that the parameter value ranges of the transistor and the diodes, as well as the ranges of the resistor values, are first obtained by the usual worst-case design procedures within the component parameter values indicated by the vendors.

Depending on how the components are laid out on the substrate and which junctions are used for the diodes in the circuit, the associated isolation diodes will be established. Of course, more than one scheme is possible in every case. In order to determine which scheme is the optimum one for a particular case, it is best to redraw the circuit, including in it the isolation diode associated with each component. Such a procedure assists the designer in determining the following important points:

1. Assuring that none of the isolation junctions become forward-biased accidentally.
2. Assuring that the breakdown voltages of junctions are not exceeded.
3. Establishing those circuit nodes which must be isolated from each other, such as inputs from outputs and positive supplies from negative supplies.

INDIVIDUAL DIODE STRUCTURES. A look at the circuit shows that isolation diodes will be associated with the resistors and the collector of the transistor (Fig. 7.2). The isolation diodes are indicated with a prime, such as D_1'. Isolation diodes for resistors and the transistor are basically unaffected by the isolation schemes used for D_A, D_B, D_C, and D_D.

The first possibility for diode isolation is to use four distinctly separate diode areas (Fig. 7.3*a*). In this case, the diodes would be diffused at the same times as the transistor collector and base diffusions, although separate diffusions for the diodes could also be used. External connections would be made by metalized paths. When constructed in this manner, the cathodes of all the diodes have individual isolation diodes with a common anode (the P-type substrate), which is grounded. The end result is the configuration shown in

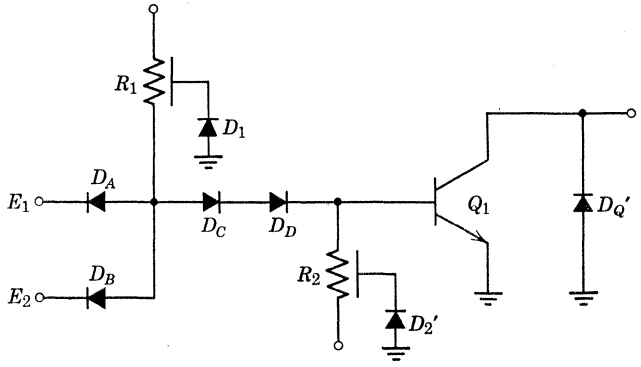


Fig. 7.2 Isolation diodes associated with resistors and transistor.

Fig. 7.3*b*. The disadvantages of this scheme are quite clear. Each isolation diode has a separate isolation capacitance associated with it, and the total isolation-junction area capacitance is quite large. The speed of the circuit is adversely affected since it is dependent upon the charge rate of this capacitor. For high-speed circuit operation com-

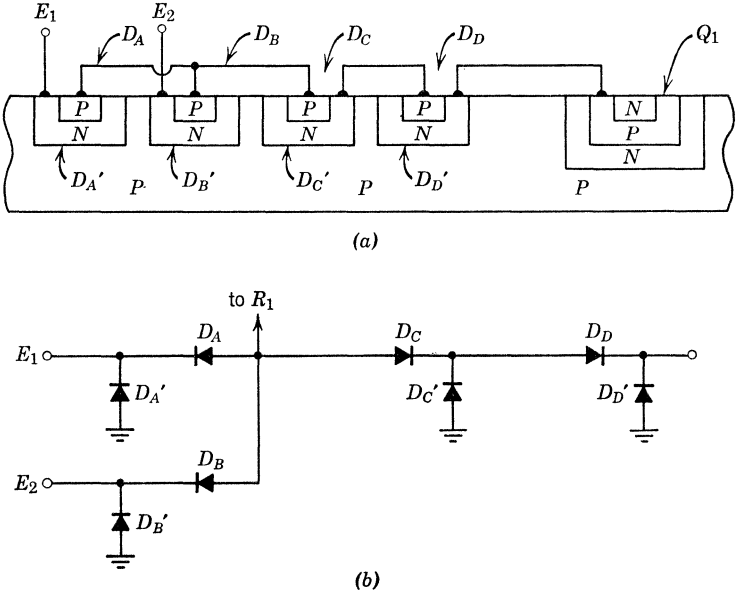


Fig. 7.3 Individual diode structures: (*a*) cross-sectional view, (*b*) circuit configuration.

bining isolation areas can reduce the total capacity. Also, the interconnection pattern would become quite complicated. In connecting the P regions of D_A, D_B, and D_C, precautions would be necessary to insure that the interconnect does not short out their respective N regions.

TRANSISTOR DIODES USING BASE-COLLECTOR JUNCTIONS. The second possibility is to have actual transistors diffused for the diodes and to use one of the junctions. With this method, several configurations are possible. One simple scheme is to use the base-collector junction of each transistor with the emitter left floating, as shown in Fig. 7.4*a*. The collector of each transistor has an isolation diode to ground through the common P-type substrate. The resultant circuit con-

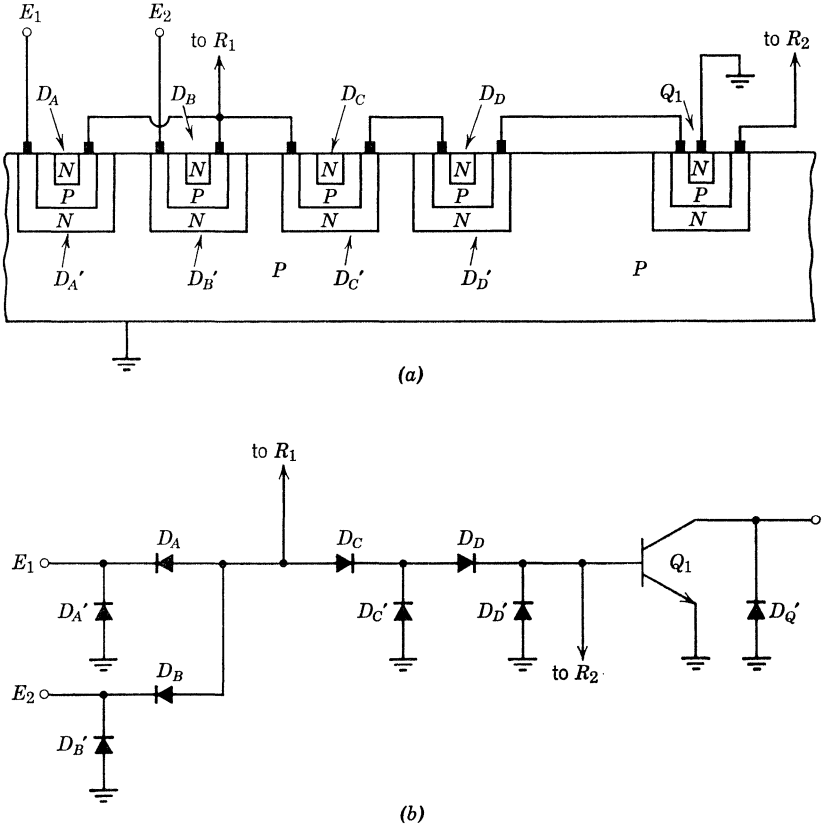


Fig. 7.4 Base-collector junction with floating emitter: (*a*) cross-sectional view, (*b*) equivalent schematic representation.

figuration is shown in Fig. 7.4*b*, which is a normal equivalent schematic representation.

The basic shortcomings of this method are the same as those of the individual diode structures discussed in the previous section. The cumulative capacitive effect of the collector to ground isolation diodes diminishes the circuit switching speed. The interconnect patterns are also complex. Another added disadvantage is that transistor structures normally require larger substrate areas than diode structures.

Another aspect about the circuit of Fig. 7.4*a* that deserves consideration is the existence of a *PNP* transistor structure, which usually has some usable gain in most integrated forms. This becomes quite obvious when Fig. 7.4*a* is redrawn using the conventional four-layer representation as shown in Fig. 7.5*a*. If the proper biases are applied, this *PNP* transistor becomes an active device connected as an emitter follower as shown in Fig. 7.5*b*. As a result, it is possible to use the

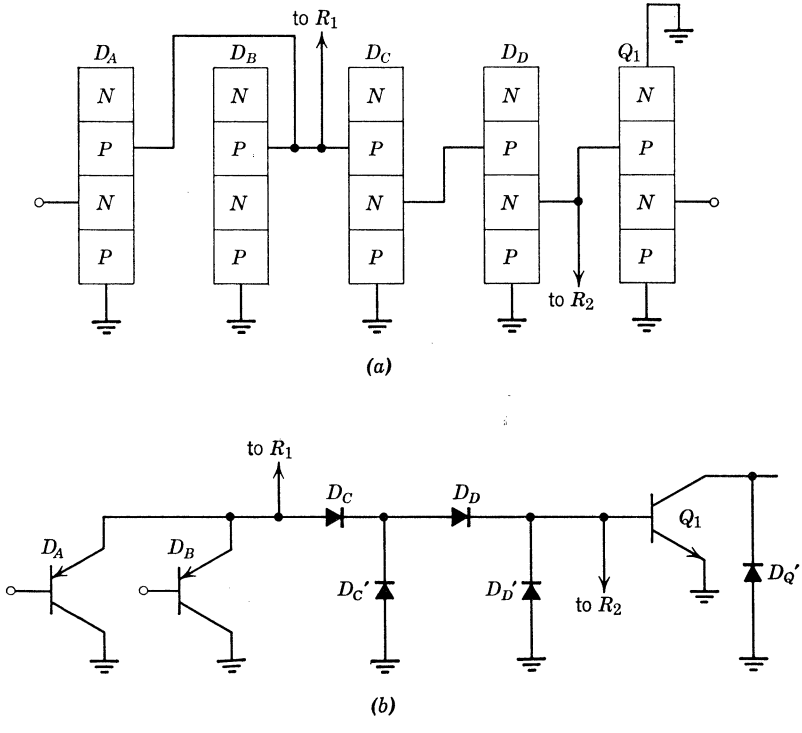


Fig. 7.5 The active device effects of the isolating region: (*a*) four-layer diode representation, (*b*) schematic representation.

isolation junction to aid the circuit during the negative-going wave fronts. Thus, improvements in circuit performance cannot always be explained without recognizing the effects of active transistors associated with the isolation regions.

TRANSISTOR DIODES USING BASE-EMITTER JUNCTIONS. The third possibility, very similar to the one just described, is to use the base-emitter junctions of the actual transistors. Figure 7.6 shows the case where the collector is left floating. However, in reality the collectors are connected to ground through their respective isolation diodes.

This scheme is capable of providing a substantial reduction in isolation junction area, thereby lowering the total capacitance and increasing the circuit speed. Since the two inputs are to the transistor emitters, and since the three bases are tied together, diodes D_A, D_B and D_C can be easily obtained by diffusing a multi-emitter transistor

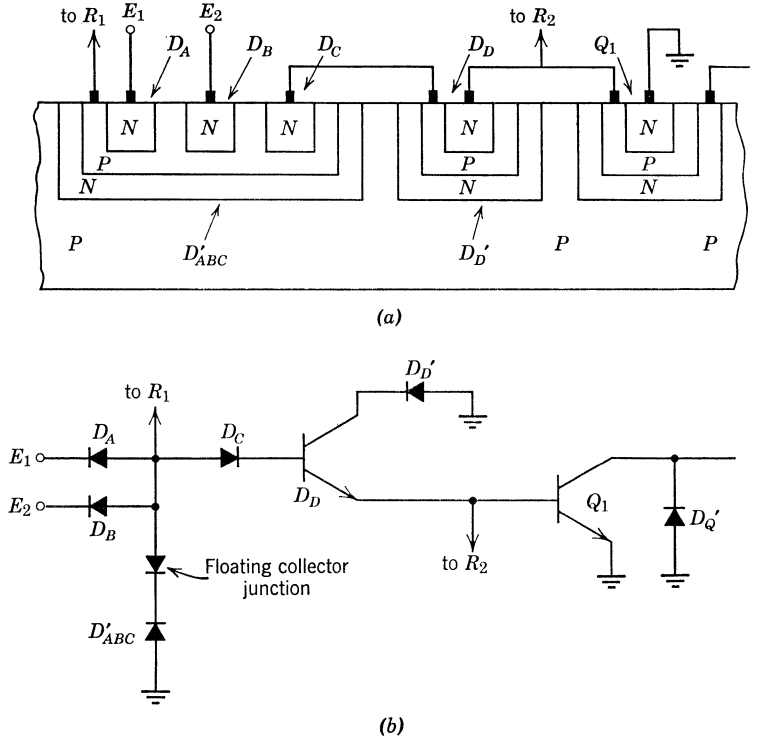


Fig. 7.6 Base-emitter diode junctions (floating collectors): (*a*) cross-sectional view, (*b*) circuit configuration.

into the substrate. This is shown clearly in Fig. 7.6*a*. Here, the three bases are naturally tied together and do not require any external means for this purpose. The interconnection pattern in this case is simpler than in the previous arrangements.

The same basic scheme could be modified to give still another isolation arrangement. From Fig. 7.6*a* it is seen that two separate transistor regions are used for diodes D_C and D_D. By using just a simple diode structure for D_C, it could be combined with the transistor used for diode D_D as shown in Fig. 7.7. The inclusion of D_C in the same region not only reduces the total junction area but results in a different interconnection pattern because now there is no need for an external connection between the cathode of D_C and the transistor collector for D_D. They are the same region. It is seen that this circuit is electrically equivalent to the original configuration of Fig. 7.3.

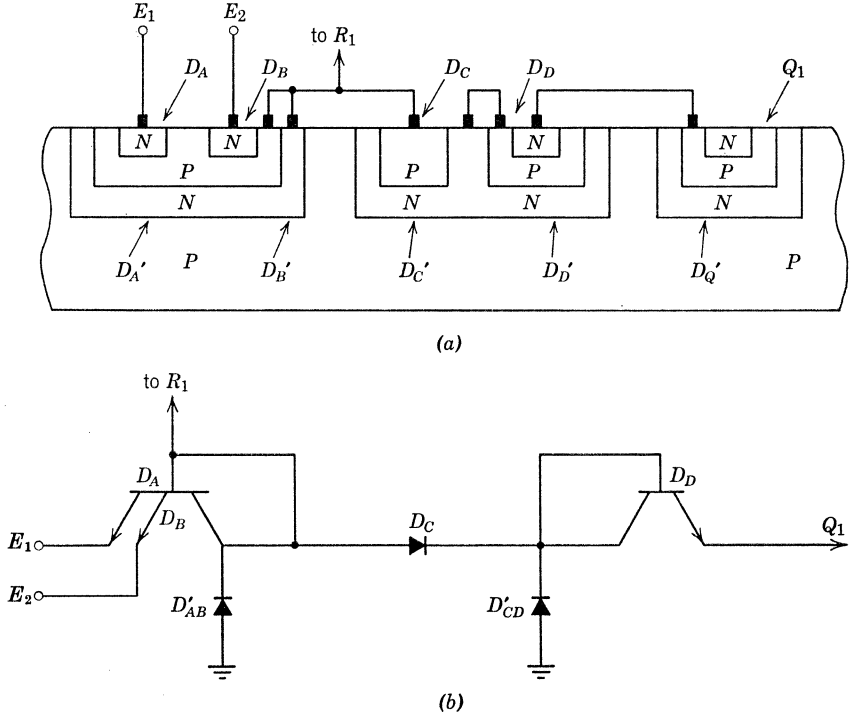


Fig. 7.7 Modified version of base-emitter junction with two common diffusion groups: (*a*) cross-sectional view, (*b*) circuit configuration.

CONCLUDING REMARKS. Figure 7.7 shows only one phase of the manufacturers' design activities, namely, some of the problems involved in component selections and layouts. This is not the whole story. While the selection of the optimum configuration, for a circuit such as the one just described, is determined by the effects of isolation capacitances, other factors must also be taken into consideration. It should be pointed out that diffusion densities increase with successive N or P type diffusions. Heavily doped junctions result in higher junction capacities and lower breakdown voltages. Junction characteristics are different for each doping level and temperature coefficients vary with doping levels. All diffusions are graded and therefore all junctions are graded junctions. Component and circuit parameters, such as transistor gain, saturation resistance, speed, etc., are affected by doping levels. This brief discussion should give the reader some appreciation of the problems involved.

REFERENCE

1. *Advanced Integrated Circuit Logic Designs,* article by Motorola Semiconductor Products, Inc.

Custom integrated circuits

8

From the previous chapters we can see that designing even simple configuration-integrated circuits can present some formidable engineering challenges. These problems are compounded when it comes to integrating specialized circuits of greater complexities. One of the objections against integrated circuits, commonly voiced by equipment manufacturers' circuit engineers, is that they abrogate their traditional prerogative of designing their own circuits—that they are stuck with the circuits designed by the vendors' engineers—if they decide to use commercially available standard integrated circuits. The off-the-shelf products described in the appendixes certainly offer a broad selection to the prospective user. Nonetheless, the contention expressed by the equipment manufacturers' engineers does merit serious consideration, since no vendors can possibly be expected to supply all the special needs of one or more customer from their standard lines.

There are several solutions to this problem. The most obvious one is to design and build equipment around the commercially available circuits. This solution is the one most distasteful to the equipment manufacturers' engineers. Another possibility is for the equipment manufacturer to specify his requirements using the traditional black-box concept. In this case, the customer would merely indicate the terminal and power-supply requirements and let the manufacturer do the circuit design. Unfortunately, this solution is unsatisfactory from the vendor's and the user's viewpoints. Primarily, the vendors are not in the circuit design business, although they are gradually forced in that direction, and so have developed a highly competent circuit design capability. Nevertheless, it would be extremely difficult, and uneconomical, for them to provide individually designed circuits for all the potential customers; thus the end-product may not be quite what the customer would desire. A third solution is that the customer designs the circuit and releases the schematic to the vendor for integrated fabrication on a direct one-to-one component basis. While this solution is fine from the customer's point of view, it creates a rather uncomfortable situation for the vendor. The reason for this is the fact that primarily the equipment manufacturer's design engineers are not semiconductor-oriented men, and hence the circuits they design

may or may not be within the vendor's existing manufacturing capabilities. Also, they may not take the advantage of the best trade-offs between circuit options and the available fabrication processes.

Undoubtedly there are several ways in which such a problem could be handled. It is quite apparent that no simple solution can be formulated which can be universally applied to all situations. One suggestion for handling this problem is to set up functional design-development groups within a company to maintain close liaison with vendors. Through personal contacts and periodic visits to vendors' manufacturing facilities, the most recent status of vendors' capabilities could be obtained, studied, documented, and disseminated to the engineers in the group. A functional design specification for the circuit would then be drawn up and the circuit designed consistent with the current information available on vendors' state-of-the-art manufacturing capabilities. Such a circuit can be breadboarded with conventional components, tested, and modified wherever necessary. The functional specification could then be released to the vendor, or vendors, concerned, along with the schematic as a suggested or recommended circuit meeting all the requirements of the specification. This approach has been tried and seems to have produced very gratifying results since it insures that both the specification and the circuit are realistically within the present-day manufacturing capabilities.

Realizing the implications of these problems, some of the vendors have taken the initiative in setting up several schemes, including in them some well-established ground rules, which would aid the customers' engineers in designing custom circuits. Some of these approaches are presented in this chapter, based on the information available at this time.

8.1 GENERAL ELECTRIC M1 MATRIX

The General Electric Company's line of standard units, called ECLO, which are described in Appendix A, are all fabricated from the same basic semiconductor wafer. This semiconductor chip contains integrated transistors and resistors in a unique matrix arrangement. By interconnecting these elements in different configurations, the various ECLO circuits are obtained. The interconnections are accomplished by depositing aluminum conducting patterns. The M1 matrix is versatile in that it enables the customers' engineers to design their own circuits within the framework of this concept on a sort of "do-it-yourself" basis by following simple basic ground rules. We will briefly describe the M1 matrix and the fundamental rules applicable for designing circuits using this approach.

Circuit Elements on the M1 Matrix

The M1 matrix basically consists of a *P*-type silicon wafer, about an inch in diameter, with an *N*-type layer (about 1 mil thick) epitaxially grown on one side of it.[1] *P*-type bases are then diffused into the *N*-type layer. This same diffusion is also used for the *P*-type resistors and element isolation lines. After this, an *N*-type diffusion in the *P*-type base regions forms the transistor emitters and a ring collector contact. Heavily doped *N* material then forms ohmic contacts with the collector, which is the original epitaxially grown *N*-layer.

THE TRANSISTORS. Figure 8.1 shows the typical transistor formed on the matrix. The areas indicated by *C* are for the collector contacts. These *NPN* transistors have characteristics very similar to those of the 2N914. The collector breakdown voltage exceeds 20 volts, and the isolation diode breakdown voltage is greater than 30 volts. The saturation resistance is less than 10 ohms. The transistor configurations can also be used as diodes. The base-collector diode can be readily used for clamping purposes since it has high breakdown voltage and low leakage current. The base-emitter diode has a breakdown voltage of approximately 7 volts, and thus can be used as a reference diode in the forward direction. The M1 matrix contains 1100 transistors on one wafer.

THE RESISTORS. Figure 8.2 shows the basic resistor pattern of the M1 matrix. It consists of a pair of resistors with each unit of resistance, $R = 2$ kilohms, when connected from contact *E* to contact *F* of the same resistor. From contact *F* to contact *G* it is $R/2 = 1$ kilohm. Therefore from contact *E* to contact *G* is 3 kilohms on the same resistor. On the matrix they are arranged in arrays of 2, 4, and 6. The resistance tolerance is approximately $\pm 20\%$ and the temperature coefficient is approximately 1000 ppm/°C. By series, parallel, and series-parallel

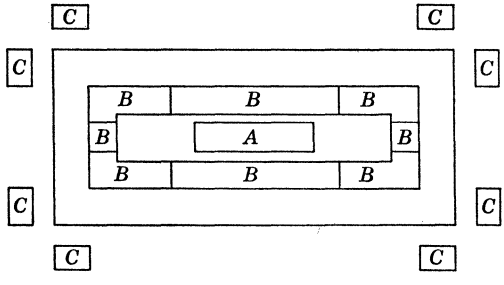


Fig. 8.1 The transistor configuration in the M1 matrix.

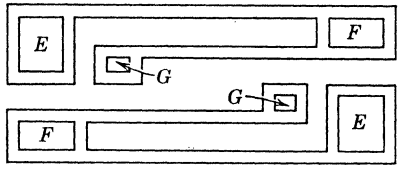


Fig. 8.2 The basic resistor pattern in the M1 matrix.

combinations of these resistor packs, a wide range of resistance values can be obtained.

Guidelines for Circuit Design

CIRCUIT DESIGN PHILOSOPHY. While the fundamental philosophy for circuit designing is up to each individual equipment manufacturer and his engineers, it should be realized that digression from traditional concepts is not only a necessity in integrated circuits but often is desirable and can sometimes result in unexpected advantages. The normal worst-case design procedure is usually cost-saving when conventional components are used. For instance, the tolerances on resistors are kept pretty small, usually $\pm 1\%$, while wide tolerances are permissible on power supplies. The cost-saving is realized because the resistors with better tolerances cost only a little more than otherwise. On the other hand, power supplies cost considerably more as tighter tolerances are specified.

In integrated circuits, component count per se, although important, is no longer a critical factor, within limitations of power dissipation and packing concepts, of course. With the high packing densities now possible, built-in redundancy for improving reliability becomes a very attractive reality. Consequently, statistical design techniques become very important. Duplication of circuitry on the same chip becomes a possibility that could be profitably exploited by the M1 matrix. In such duplication, common output wires could be shared by the circuits. Redundancy could also be used in the actual circuits to improve tolerances of elements, such as resistors. Statistically, for instance, four resistors with $\pm 20\%$ tolerances can be used individually in a series-parallel combination to give an overall tolerance of $\pm 10\%$. Such a statistical approach, of course, assumes that all units are not high or all units are not low, but spread over the tolerance range.

CIRCUIT LAYOUTS. Theoretically, the entire wafer, 1 in. in diameter, could be used as the maximum chip size. In practice this is hardly possible, because of packaging limitations. If a conventional TO-5

package is used with 10 leads, then this limits the chip to 100 × 100 mils. For circuit layout purposes, G.E. supplies a component layout worksheet on which the actual component connections can be sketched in by the engineer after he has designed the actual circuit. Each M1 matrix wafer is subdivided into blocks of 200 × 200 mils for convenience. Each block contains 88 transistors and 462 resistors. The G.E. worksheet is designed such that the 100 × 100 mil chip equals one 200 × 200 mil block cut into four parts.[2] G.E. advises that the circuit be divided into modules which can be implemented with a maximum of 10 leads. If a TO-5 package is to be used, then the maximum module components should be limited to 18 transistors and 66 resistors. G.E. also recommends smaller chip sizes for the following reasons: (1) wide applicability for the modules, (2) minimization of design and layout time, (3) systems modifications can be simplified, (4) to aid in testing, and (5) reduction of spare parts inventories. A complete step-by-step layout procedure is described in the G.E. brochure and the reader is referred to this for additional information.[2]

New Matrices from General Electric

The M1 matrix was apparently designed for G.E.'s standard-line ECLO circuits; consequently it leans more heavily toward transistors than toward resistors. As explained before, diodes are obtained by using transistor junctions. Capacitive elements can only be obtained by using back-biased diode junctions, with all their attendant shortcomings. However, the matrix approach has an inherent versatility which has tremendous application possibilities. More resistors with wider selection of values and diffused crossovers for simplifying the interconnection problem are planned for the new G.E. matrix, M2. Future plans indicate inclusion of 25 pf capacitors on the M2. This would be called the M3 matrix. Beyond the M3, G.E. is planning the M4 and the M5, which will be M2 and M3, respectively, with different combinations of components.

8.2 FAIRCHILD CUSTOM-INTEGRATED CIRCUIT BREADBOARDS

A rather novel approach is devised by Fairchild Semiconductor for integration of nonstandard circuits designed by the customer's engineers. Based on their process experience in the "Micrologic" line, Fairchild has developed and tested design rules of integrated circuits for production of other circuits. Fairchild has available a family of integrated circuit parts, which the customer can use for breadboarding and testing his circuit designs. These individual parts are packaged in standard TO-5 cans and made by the standard Micrologic fabrica-

tion processes. These units are intended to realistically duplicate the characteristics of the particular components as they would be encountered in the fully integrated circuit. At the present time the units are available with the resistors, transistors, and diode arrays, with capacitors expected to be added soon.

A data sheet is sent to the customer along with each of these elements. Using this information, and guided by the design rules indicated by Fairchild, the equipment manufacturers' engineers design the circuits and then breadboard them, using these component elements. After satisfactory testing of the breadboard, the circuit specifications along with the schematic are sent to the vendor. Fairchild suggests that the working breadboard should also be sent to them. The vendor designs the masks and the necessary test setups, which are usually checked using the customer's breadboard, if that is sent to them. The units are then produced on their regular production line. A brief description of each component, based on the currently available information, is given along with the ground rules for designing circuits. All units are available in standard TO-5 packages with 8 leads, except the transistor unit. Fairchild uses the "separation diffusion" method for component isolation. Since this method is described in detail in one of the previous chapters, it will not be repeated here. Because of this method of isolation, the back side of each wafer is *P*-type material, and the *P-N* junction formed by this layer with other components must be properly reverse-biased to insure adequate isolation.

The Standard Elements

TRANSISTOR, μE T-1. This unit consists of just one *NPN* silicon planar transistor with an isolation diode (Fig. 8.3*a*). It is packaged in a TO-5 package with 4 numbered leads (Fig. 8.3*b*). The μE T-1 transistor has the following typical characteristics at room temperature:

d-c curent gain	80 (I_C = 3.0 ma, V_{C5} = 5 v)
$V_{CE(SAT)}$	0.25 volt (I_C = 3.0 ma, I_B = 0.3 ma)
$V_{BE(SAT)}$	0.73 volt (I_C = 3.0 ma, I_B = 0.3 ma)
BV_{CBO}	30 volts (I_C = 0.01 ma, I_E = 0)
BV_{EBO}	6.6 volts (I_C = 0, I_E = 0.01 ma)
I_{CBO}	100 nanoamp (I_E = 0, V_{CB} = 10 v)
Output capacitance	5.0 pf (I_E = 0, V_{CB} = 5 v)

Fairchild mentions that for any circuit using the μE T-1, the total power dissipation should not exceed 500 mw. The typical collector to isolation breakdown voltage is 30 volts, and the typical collector to

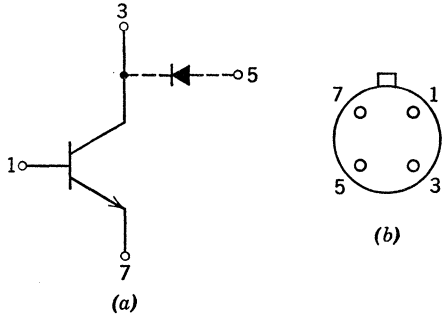


Fig. 8.3 Fairchild μE T-1 transistor unit. (*a*) The transistor with the isolation diode. (*b*) Pin numbering scheme (bottom view).

isolation leakage current is 100 nanoamps. All these figures are at room temperature, and the maximum operating case temperature is indicated at +125°C.

RESISTOR ARRAY, μE R-1. This unit consists of one continuous geometry resistor with taps such that six resistors in series are obtained (Fig. 8.4*a*). The resistive element is obtained by the *P*-type base diffusion, and consequently an equivalent diode is obtained from each resistor to the *N*-type collector region. These diodes all have a common cathode, which is then tied to the isolation diode cathode.

The maximum operating case temperature for this unit is +125°C, and the maximum power dissipation of any circuit using this unit should not exceed 500 mw. At room temperature, the typical resistor breakdown voltage is 30 volts; the typical isolation breakdown voltage

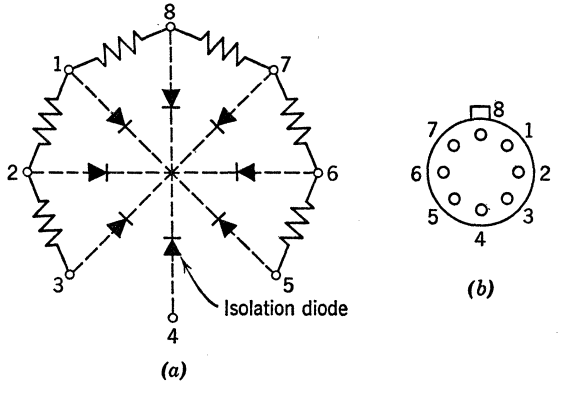


Fig. 8.4 Fairchild μE R-1 resistor unit. (*a*) The resistor array. (*b*) Pin numbering scheme (bottom view).

is also 30 volts. The temperature coefficient typically varies from 0.1%, for a range of −55°C to +25°C, to 0.2%, for a range of +25°C to +125°C. The typical leakage current in shunt with the resistor element is 0.4 μamps with pin 3 grounded and 10 v on pin 4. The typical d-c resistance values between various pins, indicated by Fairchild, are:

Pins	Resistance (ohms)
2-3	125
1-2	125
8-1	260
7-8	500
6-7	1000
5-6	4000

These are nominal values and tolerances of ±30% are to be expected in these units.

RESISTOR ARRAY, μE R-2. This unit also consists of one continuous resistor with taps giving four resistors in series (Fig. 8.5*a*). This unit is similar to the μE R-1, and has the same type of equivalent and the isolation diodes.

The maximum power dissipation of any circuit using this unit should be under 500 mw, and the maximum operating case temperature is +125°C. The typical resistor breakdown voltage, at room temperature, is 30 volts; the typical isolation breakdown voltage is also 30 volts. The temperature coefficient varies from 0.1%/°C for a range of −55°C to +125°C to 0.2%/°C for a range of +25°C to +125°C. The typical shunt capacitance is 20 pf, measured from

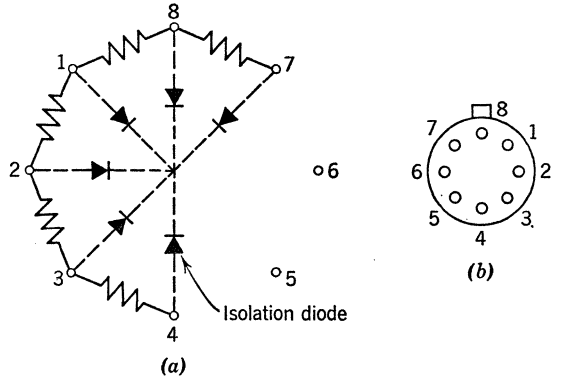


Fig. 8.5 Fairchild μE R-2 resistor unit. (*a*) The resistor array. (*b*) Pin numbering scheme (bottom view).

pin 4 to pin 3. The typical leakage current in shunt with the resistor element is 0.4 μamps. The typical d-c resistance values between various pins are indicated by Fairchild as follows. These values are nominal with tolerances of 30%:

Pins	Resistance (ohms)
2-3	1500
1-2	2500
8-1	4000
7-8	8000

COMMON CATHODE DIODE ARRAY, μE D-1. Five silicon diodes with their cathodes tied together are available in this unit. The common cathodes are formed by the transistor N-type diffusion, and the anodes are the P-type base diffusions. Thus an isolation diode is naturally tied to the common cathode point (Fig. 8.6*a*).

The maximum operating case temperature is +125°C and the maximum power dissipation of the circuit using this unit is 500 mw. The typical parameters at room temperature, given by Fairchild, are:

Diode breakdown voltage	30 volts (I_R = 0.01 ma)
Diode leakage current	10 nanoamp (V_r = 10 v)
Reverse recovery time	7 nanosec ($I_f = I_r$ = 10 ma)
Diode capacitance	4 pf ($V_R = 0, f$ = 10 mc)
Isolation capacitance	20 pf ($V_R = 0, f$ = 1 mc)
Cathode to isolation breakdown voltage	30 volts (I_R = 0.01 ma)
Cathode to isolation leakage current	0.1 μamp (V_R = −10 v)
Forward voltage	0.8 volt (I_f = 3.0 ma)

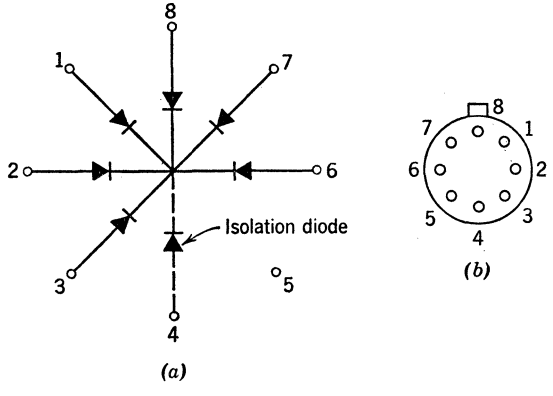


Fig. 8.6 Fairchild μE D-1 common-cathode diode array. (*a*) The diode configuration. (*b*) Pin numbering scheme (bottom view).

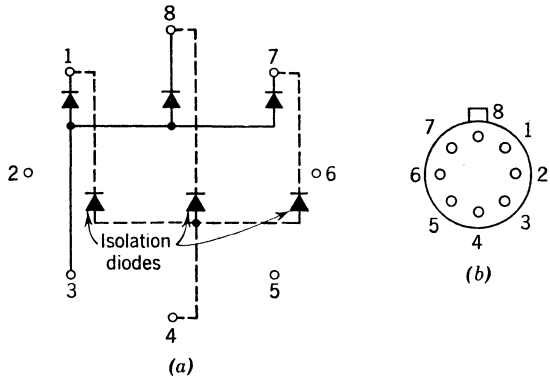


Fig. 8.7 Fairchild μE D-2 common-anode diode array. (*a*) The diode configuration. (*b*) Pin numbering scheme (bottom view).

COMMON ANODE DIODE ARRAY, μE D-2. This unit consists of three silicon diodes with their anodes tied together (Fig. 8.7*a*). Here there is no common isolation region that would also make their cathodes tied together. Consequently, each diode has its own individual isolation diode tied to its cathode. The anodes of the isolation diode are naturally tied together. The anodes of the regular diodes are connected by externally metalized strips.

The maximum operating case temperature is +125°C and the maximum power dissipation of any circuit using this unit is recommended at 500 mw. At room ambient, Fairchild indicates the following typical parameters:

Diode breakdown voltage	30 volts (I_r = 0.01 ma)
Diode leakage current	10 nanoamp (V_r = −10 v)
Reverse recovery time	7 nanosec (I_f = I_r = 10 ma)
Diode capacitance	4 pf (V_R = 0, f = 1 mc)
Isolation capacitance	7 pf (V_R = 0, f = 1 mc)
Cathode to isolation breakdown voltage	30 volts (I_R = 0.01 ma)
Cathode to isolation leakage current	0.1 μamp (V_R = −10 v)
Forward voltage	0.8 volt (I_f = 3.0 ma)

Ground Rules for Circuit Designing

COMPONENT LIMITATIONS IN CIRCUIT DESIGNING. In the Fairchild approach, as in any vendor's scheme, the size of the package and the heat dissipation restrict the number of components that can be incorporated in the circuit to be integrated. It is necessary for the equipment manufacturer's engineer to know whether the circuit he has

designed is realistic for integrated fabrication as far as components are concerned. To aid the circuit designer in this task, Fairchild has developed a point system which consists of weights assigned to each circuit component and the other parameters involved. The points are shown in Table 8.1. Since common cathode diodes and common collector transistors share the same isolation region, considerable savings in area can result from using these devices. Consequently, relatively low weights are attached to them. On the other hand, resistors occupy comparatively large areas and thus are assigned higher number of points. For instance a 1 kilohm resistor takes up as much area as a μE T-1 transistor. Input, output, and power supply terminals also need comparatively large pad areas for lead bonding, and so they are also weighted heavily.

After designing the circuit with the help of the component data sheets, Fairchild suggests that component count points be added up as indicated in Table 8.1. The total number of points should not exceed 100. At the time of this writing, the single and multiple μE T-2 transistors or any data on them were not available. Resistors with a common point may be considered as single resistors as far as the component count is concerned. For Table 8.1, K = number of kilohms, n = number of diodes or transistors, R = resistance in ohms.

TABLE 8.1

FAIRCHILD COMPONENT COUNT

Components	Points	Remarks
μE T-1 (single transistors)	5	. . .
μE T-1 (multiple transistors with common collectors)	$2(n-1)+5$	Only applicable for $n \leq 5$
μE T-2 (single transistors)	9	. . .
μE T-2 (multiple transistors with common collectors)	$5(n-1)+9$	Only applicable for ≤ 5
Diodes	4	. . .
Common cathode diodes	$(n-1)+4$	. . .
Resistors (for R = 300 ohms)	$K+4$	Resistors should all be multiples of 75 ohms
Resistors (for R = 300 ohms)	$65/R+4$	Resistors should be submultiples of 150 ohms
External connection points	4	. . .

PRECAUTIONS FOR BREADBOARDING. Since the breadboard is intended to realistically duplicate the final fully integrated circuit, it is necessary to simulate realistic parasitics, such as distributed capacitances and leakage currents. The following suggestions are indicated by Fairchild for this purpose:

1. The isolation diode terminals of all the individual units must be tied together and to the most negative supply voltage to insure that the isolation diodes are reverse-biased. This precaution is necessary because the entire underside of the Fairchild integrated circuit wafer is a *P*-type diffusion, and this region forms the anode of all the isolation diodes in the circuit.
2. While it is permissible to obtain the desired resistor values by various combinations of series and parallel connections of the available taps, a very unrealistically high parasitic capacitance can result on the breadboard. The resistance values obtained in the fully integrated circuit depend on the length of the resistive diffusion. Therefore, it is necessary that on the breadboard, the number of parallel resistive paths be kept to a minimum for the simulation of the final integrated circuit to be realistic.

8.3 TEXAS INSTRUMENTS, INCORPORATED, MASTER SLICE

For custom integrated circuits, Texas Instruments, Inc. has a standard silicon wafer, called the Master Slice, with several diffused components but without any interconnecting paths between them. These wafers are taken from Texas Instruments' regular production lines. The standard Series 51 products (see Appendix A) are also manufactured from the Master Slice. The equipment manufacturers' engineers design their circuits using the component information, which is now briefly outlined. Texas Instruments then designs the interconnection pattern and fabricates the mask. An aluminum interconnection pattern is then photoetched on the wafer. Integrated circuits fabricated in this manner are packaged in the standard Texas Instruments' flat-rectangular package, with 10 lateral leads (see Fig. 12.2), which is hermetically sealed. Since Texas Instruments' standard high-volume production facilities are directly utilized in the manufacture of the Master Slice, significant quantities can be supplied in relatively short times. According to Texas Instruments, evaluation samples can be delivered to the customer within four weeks after the circuit design is approved.[5]

The Components on the Master Slice

TRANSISTORS. There are seven transistors available on the Master Slice.[4] They are *NPN* silicon planar devices very similar to the 2N706A. At room temperature, the d-c current gain is typically 40. At 1 ma the $V_{CE(SAT)}$ is 0.3 volt and the collector-to-emitter breakdown voltage, BV_{CEO}, is 9 volts.

DIODES. Seven planar diodes, similar to the 1N914, are available on the Master Slice. The capacitance is 4 pf at 25°C. The forward voltage, V_f, is 0.7 volt at 1 ma and the reverse voltage, V_r, is 50 volts.

RESISTORS. Figure 8.8 shows the resistors available on the Master Slice. Three resistors in series are available with four taps, giving a resistance range of 1 to 5 kilohms. The temperature coefficient of these resistors is 0.5%/°C.

CAPACITORS. Two capacitors are available on the Master Slice. These capacitors are obtained by reverse-biasing two *P-N* junctions, giving typical capacitance of 120 pf. The maximum reverse voltage is 8 volts.

RESISTOR-CAPACITOR COMBINATIONS. Six combinations of a resistor and capacitor in series, with a tap between the components (Fig. 8.9), are available. The resistors are 20 kilohms diffused resistors, and the capacitors are back-biased *P-N* junctions giving a capacitance of 60 pf.

8.4 SIGNETICS CUSTOMIZED INTEGRATED CIRCUITS

Signetics is offering two distinct approaches to custom integrated circuits. The first approach, called the variFEBS approach, is very similar to TI's Master Slice and the second approach, called the preFEBS approach, is similar to the Fairchild Integrated Circuit Breadboards. Both the methods are briefly described.

variFEBS Custom Integrated Circuits

The variFEBS consist of a family of silicon substrates containing both active and passive elements without any interconnection patterns. This group contains three different substrates with three different combinations of circuit elements. These substrates are identical to

Fig. 8.8 Diffused resistors on the Texas Instruments, Incorporated Master Slice.

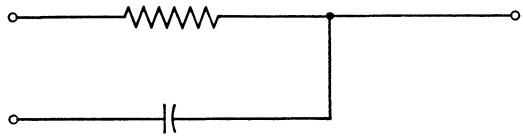


Fig. 8.9 Resistor-capacitor combination on the Texas Instruments, Incorporated Master Slice.

those used by Signetics in the fabrication of their Series SE100 digital integrated circuits standard line.

TYPICAL VARIFEBS COMPONENTS. Some of the typical values of the elements in the series of substrates are as follows:

Transistors—Type VFT1. This transistor has a gain-bandwidth of 500 mc, with h_{FE} of 30 (I_C = 5 ma, V_{CE} = 1 v), I_{CBO} of 50 mμa (V_{CB} = 5 v), and $V_{CE(SAT)}$ of 0.3 volt (I_C = 3 ma, I_B = 0.15 ma). The typical breakdown voltages are:

$$BV_{CBO} = 15 \text{ volts}$$

$$BV_{EBO} = 5 \text{ volts}$$

$$BV_{CEO} = 7 \text{ volts}$$

Diodes—Types VFD1 and VFD2. Diodes are not fabricated separately. Diode VFD1 is obtained by using the base-collector junction of transistor VFT1 and the VFD2 is obtained by using the base-emitter junction of VFT1. The following typical characteristics are mentioned by Signetics:

	VFD1 (base-collector)	VFD2 (base-emitter)
Capacitance (0 volts bias)	2 pf	3 pf
Forward voltage (I_f = 10 ma)	1.0 volt	1.2 volts
Reverse voltage (I_V = 10 μa)	10.0 volts	5.0 volts
Recovery time ($I_f = I_r$ = 2 ma)	3.0 nanosec	3.0 nanosec

Resistors—Type VFR1. These resistors have tolerances of $\pm 15\%$ with temperature coefficients of 0.1%/°C. Each resistor has taps and additional taps can usually be provided. These are all diffused resistors.

Capacitors—Type VFC1. Signetics does not use back-biased diodes for capacitors. The only capacitor available in this line is a metal-oxide-silicon capacitor of 60 pf $\pm 15\%$ with a temperature coefficient of 0.025%/°C and a working voltage of 8 volts.

THE VF101 DIE. This die is used for the Signetics SE101 and SE102 DTL NAND/NOR gates. It consists of five areas each containing the elements as follows:

Area A—A 4-kilohm resistor is in this area with a center tap, giving two 2-kilohm resistors in series. The isolation capacitance is 16 pf.

Area B—Four VFT1 transistors are in this area with their collectors tied together. The collector node-ground isolation capacitance is 12 pf.

Area C—A 20*K* VFR1 resistor in this area has a center tap of 10 kilohms. The isolation capacitance is 25 pf.

Area D—The cathode of VFD1 diode is tied to the collector of a VFT1 transistor. The collector-ground isolation capacitance is 9 pf.

Area E—This area contains a single VFT1 transistor with a collector-ground isolation capacitance of 8 pf.

THE VF120 DIE. The SE120, SE121, and the SE122 DTL binary elements are fabricated on this die, which consists of six different component groupings as follows:

Area A—There are two areas, each containing a 60 pf VFC1 capacitor with 40 pf isolation capacitance.

Area B—There are six such areas containing a VFD1 diode with an isolation capacitance of 7 pf from the cathode to ground.

Area C—This area contains two 14-kilohm resistors, and two sets of 6-kilohm resistors, each tapped at 2 kilohm/4 kilohm points. The isolation capacitance is 60 pf.

Area D—This area contains a 40 kilohm resistor with a center tap at 20 kilohms and an isolation capacitance of 45 pf.

Area E—There are two areas, each containing a VFT1 transistor with the cathode of a VFD1 diode tied to the collector. The collector-ground isolation capacitance is 8 pf.

Area F—There are two areas, each containing two VFT1 transistors with their collectors tied together. The collector-ground isolation capacitance is 9 pf.

THE VF140 DIE. This die is used for the SE140 DTL EXCLUSIVE-OR network and consists of seven different component groupings as follows:

Area A—There are six areas, each containing a VFD1 diode with cathode-ground isolation capacitance of 7 pf.

Area B—This area contains four VFD1 diodes with their cathodes tied to a node. The node-ground isolation capacitance is 10 pf.

Area C—This area has two VFD1 diodes with their cathodes tied together. The node to ground isolation capacitance is 8 pf.

Area D—This area contains a group of six 4-kilohm resistors, each with a center tap. The isolation capacitance is 60 pf.

Area E—This area contains a 20-kilohm VFR1 resistor tapped at 5.4, 4.6, 4.6, and 5.4 kilohm points. The isolation capacitance is 36 pf.

Area F—This area contains one VFD2 diode with an isolation capacitance of 7 pf.

Area G—This area has one VFT1 transistor with a collector-ground isolation capacitance of 8 pf.

SOME NOTES ON THE VARIFEBS. Signetics states a maximum operating temperature of 125°C and a maximum storage temperature of 175°C. The maximum allowable power dissipation is 100 mw. The variFEBS are available in either a modified Jedec TO-5 package, with a 10-lead header, or the standard Signetics flat-rectangular, glass-Kovar 10-lead package (see Fig. 12.3).

According to the Signetics brochure,[5] "the distributed capacitance of diffused resistors is in series with the isolation capacitance and takes precedence in design considerations." Also, "diffused resistors exhibit a distributed capacitance of the order of 0.1 pf per mm length. This capacitance may generally be ignored in digital circuits operating at 5 megacycles or less."

preFEBS Integrated-Circuit Breadboard Units

The preFEBS family consists of integrated component groupings on single silicon substrates. These units are available in 8-lead TO-5 cans. The storage temperature is −65°C to +175°C, and the operating temperature is −55°C to +125°C. Detailed component parameters are beyond the scope of this book, but the specifications sheets are readily available from the vendor. The various units available are listed below:

1. PF800T and PF801T—Both units contain a pair of closely matched transistors in each package. The transistors are high-frequency units suitable for high-speed, low-level applications.
2. PF830T—This unit contains a common-anode diode array of six diodes.
3. PF831T—This is a common-cathode diode array containing six diodes.

4. PF832T—This is a group of high-speed, medium-current diodes. Two diodes have their cathodes tied together and two others are available separately.
5. PF860T—This group consists of one 100-ohm resistor, a 200-ohm resistor, and a 1200-ohm resistor tapped at 400/800 point. The tolerance is ±15%.
6. PF861T—This group also contains three resistors, a 12, 24, and a 9 kilohm resistor tapped at 3 kilohm/6 kilohm point. These resistors also have a tolerance of ±15%.
7. PF880T—This group contains three metal-oxide-silicon fixed capacitors, 100 pf, 50 pf, and 25 pf.
8. PF881T—This group contains two metal-oxide-silicon fixed capacitors, 200 pf each.

REFERENCES

1. "High-Density Microelectronic Package Allows Do-it-yourself Circuit Design." *Electronic Equipment Engineering*, September 1962, pp. 14–16.
2. *Functional Components—M1 Matrix*, brochure by General Electric.
3. *Fairchild Semiconductor*, μE Components data sheets and brochure.
4. *Master Slice Semiconductor Networks*, brochure by Texas Instruments, Incorporated.
5. *Signetics variFEBS*, Bulletin 1001, January 1963.
6. *Signetics preFEBS*, Bulletin 8001, January 1963.

A review of digital logic circuits

9

9.1 PURPOSE OF THIS CHAPTER

The limitations of the present state-of-the art in integrated circuits impose several constraints on the circuit designer. Unusually large tolerances on individual circuit components necessarily force the engineer into designing circuits which must operate on wide margins. Digital circuits, by their very nature, can be designed to be operable over wide margins; thus it is quite natural that the initial mass market for the integrated circuit would be in the digital computer field. In view of this vast potential, it is quite understandable that the vendors are concentrating their initial efforts in the field of digital logic circuits. (Digital logic circuits offered by the various vendors as their standard product lines are presented in the Appendixes.)

The purpose of this chapter is twofold. For the engineer or the technician who is not intimately acquainted with the various forms of transistor-logic circuits, this chapter provides a brief introduction, which will, hopefully, enable him to appreciate the various types offered by the vendors today. For the reader who is well acquainted with the various transistor-logic circuits, it is hoped that this chapter will come in as a handy qualitative guide for occasional reference. No attempt is made to present detailed information on any circuit or family of circuits as far as circuit design procedures are concerned. Many excellent books and articles on the subject of logic-circuit designing are available, some of which are given as references at the end of this chapter, as well as in the bibliography. While an indefinite number of logic circuits is possible, this chapter covers only the classical logic circuits and some of the newer forms, which are principally an outgrowth of the integrated-circuit technology.

9.2 DIRECT-COUPLED TRANSISTOR LOGIC—DCTL

Basic DCTL Concept

Transistorized digital circuits basically fulfill the three logical functions of AND gating, OR gating, and signal inversion. An additional function usually performed, though not logical in nature but nevertheless a practical necessity, is signal amplification. Other

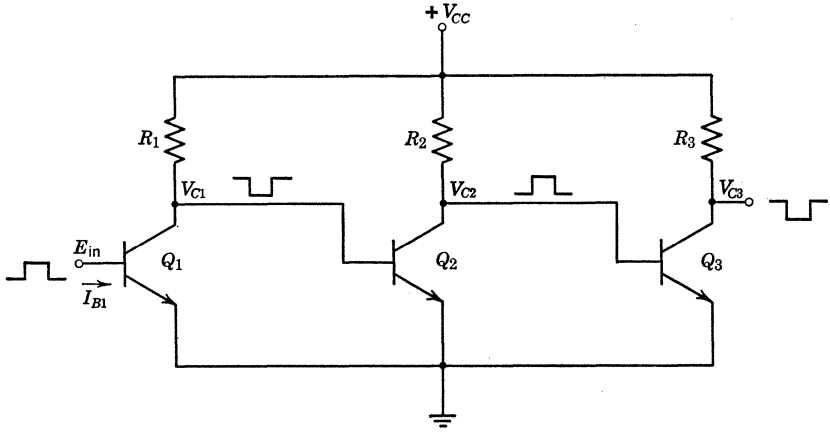


Fig. 9.1 DCTL inverters in cascade.

logical blocks, such as NOR, NAND, and flip-flops, are easily obtained using these three fundamental functional blocks. Several different circuit configurations can be used for these functional blocks. Normally these circuits are classified according to the elements used for interstage coupling or coupling between gates and inverters and amplifiers. The most commonly used coupling elements are diodes, resistors, resistor-capacitor combinations, and, more recently, transistors themselves. It is also possible to design and use circuits without any of these coupling elements. Such circuits are referred to as direct-coupled transistor-logic circuits or, more commonly, DCTL, and were first introduced by R. H. Beter et al.[1] in 1955. There are several advantages and some disadvantages of DCTL, and we consider these after discussing how this type of configuration works.

DCTL Inverters

Figure 9.1 shows three DCTL Inverters in cascade. In this circuit the collector resistors R_1, R_2, and R_3 serve as constant current sources. They supply current to their respective transistors' collectors, when they are ON or to the base of the next transistor when they are OFF. When the input voltage E_{in} to the base of Q_1 is near ground—that is at $V_{CE(SAT)}$ of the previous stage ON transistor—voltage V_{C1} tends to approach the supply voltage V_{CC}. Current is supplied to the base of Q_2 through R_1, and this turns Q_2 ON. The clamping action of the base-emitter diode of Q_2 holds V_{C1} at the value determined by V_{BE2}. Since Q_2 is ON, V_{C2} is now determined by the $V_{CE(SAT)}$ of Q_2. If Q_2

has a sufficiently low saturation drop, then V_{C2} will not be positive enough to turn Q_3 ON. The reverse situation holds true when a sufficiently positive voltage, E_{in}, turns Q_1 ON. In this case V_{C1} will maintain Q_2 OFF, which in turn will turn Q_3 ON. From this brief description several significant points are apparent. A low $V_{CE(SAT)}$ is a desirable feature of transistors used for DCTL. If the $V_{CE(SAT)}$ is high, then there is always the possibility that the next stage transistor may be erroneously turned ON. Furthermore, in order to assure that all the fan-out transistors are held OFF, the $V_{CE(SAT)}$ must be smaller than the smallest $V_{BE(ON)}$ of the succeeding transistors. It is readily seen that the supply voltage can be relatively small because the output voltage swing varies between the $V_{CE(SAT)}$ of the ON transistor and the $V_{BE(ON)}$ of the following stage transistors. Another pertinent fact is that, because of the low voltage swings, transistors with low breakdown voltage ratings can be used.

DCTL Series Gating

Figure 9.2 shows three transistors connected in series to form a DCTL-NAND gate for positive input signals A, B, and C. Stated in Boolean form, it is $A \times B \times C = \bar{D}$ for positive inputs. If any of the three transistors is OFF, the output voltage at D will be the supply voltage $+V_{CC}$ in the unloaded condition. Under loaded conditions, the voltage at D will depend on the resistor R_L and the $V_{BE(ON)}$ of the

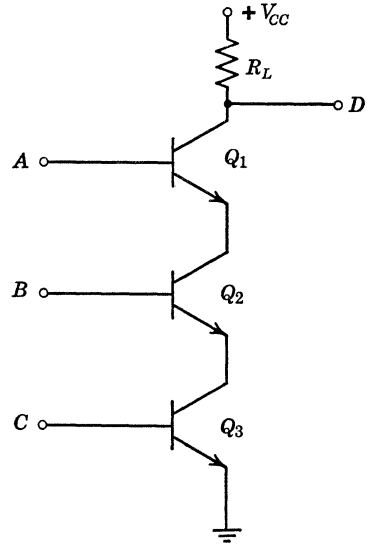


Fig. 9.2 Series DCTL gate.

next stage transistor. When all three transistors are ON, the potential at D will be closer to ground than in the previous case and will be the sum of the $V_{CE(SAT)}$ of Q_1, Q_2, and Q_3 in series. Consequently, the principal disadvantage of this configuration is the necessity to insure that the next stage transistor will be OFF when all three transistors are ON. The sum of the three $V_{CE(SAT)}$ in series must be less than $V_{BE(ON)}$ of the next stage transistor. One means of accomplishing this is to supply more base drive to Q_1, Q_2, and Q_3, thereby drawing them further into saturation and lowering the saturation resistance.[2]

DCTL Parallel Gating

Figure 9.3 shows a parallel DCTL gate, which is really the previously considered "inverter" stage with three transistors having individual inputs instead of a single transistor. Obviously, this configuration is an OR-Inverter or a NOR circuit. The Boolean expression for this function is $A + B + C = \bar{D}$ for positive-going signals. While collector leakage current is undesirable in any circuit, in this configuration it becomes particularly troublesome. The leakage currents for all three transistors is additive and is supplied by the resistor R_L. It is quite possible that this current, added to the current drawn through R_L by the load, may increase the drop across R_L such that the potential at D may not be high enough to keep the transistor of the next stage ON. Unstable operation is therefore quite likely.

DCTL Flip-Flop

A simple bistable DCTL flip-flop can be easily formed by connecting two DCTL inverters, as shown in Fig. 9.4. Suppose transistor Q_1 is

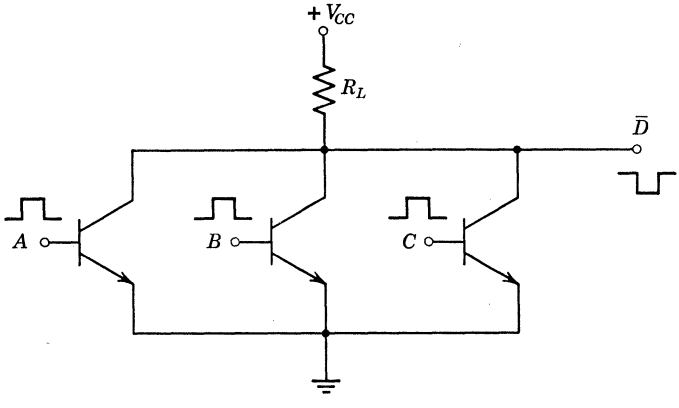


Fig. 9.3 Parallel DCTL gate.

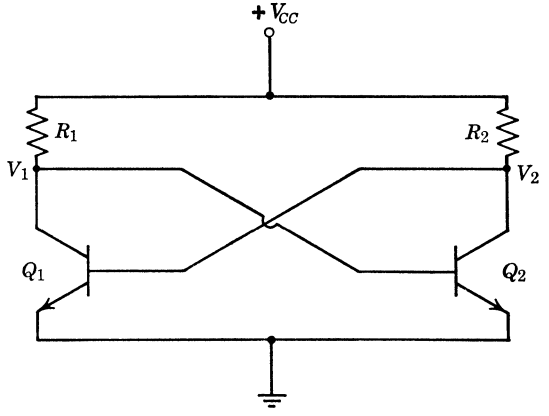


Fig. 9.4 Basic DCTL flip-flop.

ON and is saturated. Its collector, V_{C1}, is almost at ground potential, depending of course on the $V_{CE(SAT)}$ of Q_1, which turns Q_2 OFF. The current flowing through resistor R_2 is all supplied to the base of Q_1, which is therefore driven harder into saturation. The state of the flip-flop can be easily reversed by reducing the base current of the ON transistor Q_1 to zero. A very simple method of doing this is shown in Fig. 9.5.

Transistors Q_3 and Q_4 are the triggering transistors in this case. It

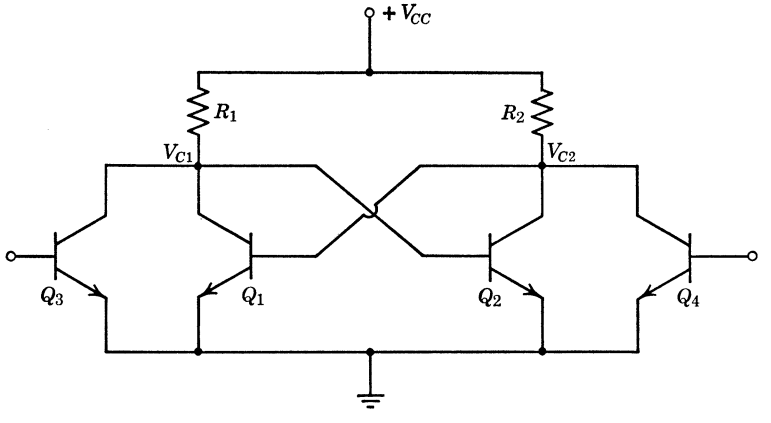


Fig. 9.5 DCTL flip-flop with triggering transistors.

was mentioned before that the ON transistor, Q_1, can be turned off by cutting off its base current supply. A positive voltage at the base of Q_4 turns Q_1 OFF. The voltage at V_{C1} tends to rise to the supply voltage V_{CC}. Resistor R_1 now supplies base current to Q_2, which now turns ON. A positive voltage at the base of Q_3 will turn it ON, and this will trigger the flip-flop to its original state by turning Q_1 ON.

Disadvantages of DCTL

CURRENT HOGGING. One of the most undesirable features of DCTL is what is commonly known as current hogging, and this phenomenon arises because of the spread in $V_{BE(ON)}$ of the various fan-out transistors. No two transistors will ever have identical input characteristics, and it is always desirable to use transistors with as small a production spread as possible on $V_{BE(ON)}$.

If the transistors Q_1, Q_2, and Q_3 in Fig. 9.6*a* have input characteristics as shown in Fig. 9.6*b*,[3] it is quite clear that the output voltage swing V_0 of transistor Q_0 will be determined by the $V_{CE(SAT)}$ of Q_0 and the maximum $V_{BE(ON)}$ of one of the fan-out transistors. Figure 9.6*b* shows that the voltage V_0 will be determined by the $V_{BE(ON)}$ of Q_3, which will draw more current from R_0 than from either Q_2 or Q_1. Since R_1 essentially acts as a constant current source, it is quite possible that the unequal currents demanded by the fan-out transistors may result in some unit hogging more current and thereby starving the other transistors, which may not get sufficient base drive to saturate them, or in some cases, even turn them ON at all. This large spread in $V_{BE(ON)}$ therefore requires that Q_0 have a relatively large h_{FE} to insure reliable operation of the fan-out transistors.

COLLECTOR LEAKAGE CURRENT. Transistors used in DCTL should have relatively low collector leakage currents. I_{CBO}, particularly when it increases at higher temperatures, is potentially a very troublesome phenomenon. Referring again to Fig. 9.6*b*, we can see that the collector current due to I_{CBO} is multiplied by some fraction of h_{FE}.[3] Because the collector current is usually low in DCTL, the drop across R_0 due to I_{CBO} may become so high that the voltage V_0 may be lowered to the point at which it may fail to turn the fan-out transistors ON. Once again, R_0, which acts as a constant current source, may not be able to supply the base drive required by the fan-out transistors, thereby starving them and resulting in unstable operation.

THE CROSSTALK OR THE NOISE PROBLEM. In any high-speed system, pulses with fast rise times are likely to produce potential differences in the ground system mainly because of ground inductances. These voltages are likely to interfere with stable operation of the system.

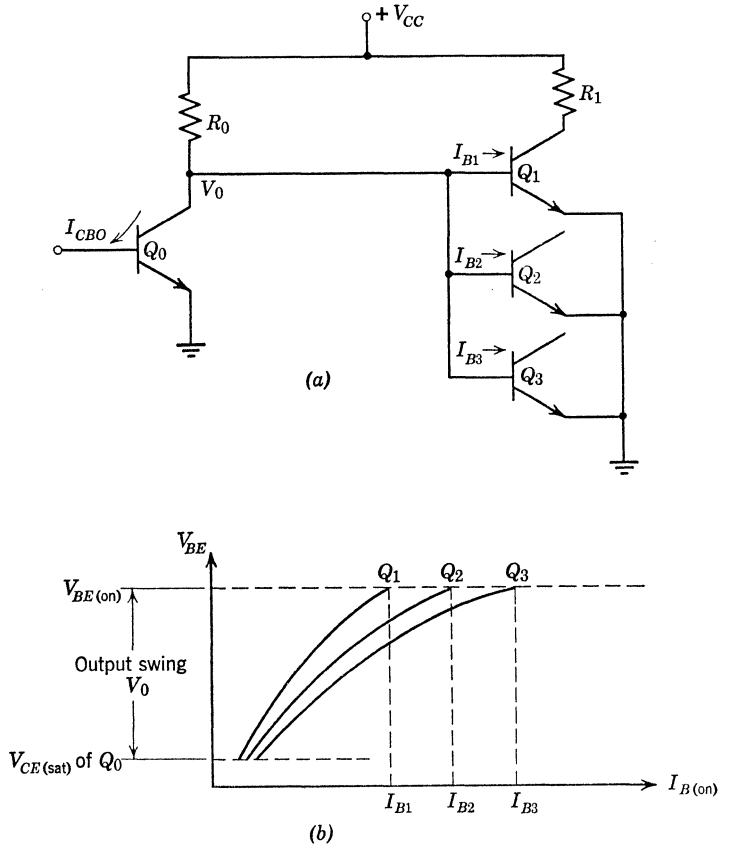


Fig. 9.6 DCTL Inverter driving a fan-out of three gates. (*a*) The circuit. (*b*) Input characteristics of the fan-out transistors.

DCTL systems are very susceptible to these noise voltages because the operating and signal voltages are naturally low in these systems. If several transistors on one end of a ground system are turned ON, the resulting pulse generated in the ground system can supply a positive or negative pulse (depending on the polarity) which can cause faulty turn-ON or turn-OFF of other transistors further down the ground system. According to Harris,[4] one solution is to mount the transistors very close together, thereby minimizing ground inductances. Besides ground noise, DCTL is also vulnerable to noise on power supplies and stray noise picked up by connecting leads. Of the various logic

schemes, DCTL has one of the lowest noise margins, typically 0.1 volt at 125°C to about 0.21 volt at room temperature, depending on the fan-out and, whether the transistor is ON or OFF.

Switching Speed

While the propagation speed of information through DCTL circuits is reasonably fast, the switching speeds are usually not. Two factors limit the switching speeds. Since the transistor is driven hard into saturation, switching speed is relatively slow. In DCTL the base drive is usually quite large, and no current is supplied for turn-OFF. Consequently, storage times are large and fall times are rather slow. Furthermore, because no reverse base current is supplied for turn-OFF, turn-ON delay time is usually quite small. It is therefore evident that the most significant factor affecting DCTL speed is the storage factor, which ideally should be as low as possible.

Advantages of DCTL

In spite of its severe limitations, DCTL still has several desirable features. Since the voltage swings involved are small, transistors with relatively low breakdown ratings can be used. The fact that only one power-supply voltage is used is a very convenient feature, and in some applications, such as aerospace digital computers, it may become a very significant advantage. Since low voltages are used, sometimes as low as 3 volts, power dissipation in both the resistors and the transistors is quite low. Although DCTL systems are expensive in the number of transistors used, the absence of interstage coupling elements, different resistors sizes, clamping diodes, and many supply voltages make them relatively simple. For integrated-circuit applications, these factors make DCTL a very attractive proposition, because transistors are cheap while resistors and capacitors are both expensive and harder to make with the desired tolerances.

Modified DCTL

Some of the disadvantages of DCTL can be remedied to some extent. Current hogging, which is perhaps the most severe limitation of this system and is the direct result of the spread in $V_{BE(ON)}$ of the fan-out transistors, can be controlled to some degree by inserting series base resistors R_{B1}, R_{B2}, and R_{B3}, as shown in Fig. 9.7*a*. In this case, the base current demanded by each transistor for saturating it does not depend on the input characteristics of the transistor alone. The base resistors are now instrumental in determining the base drives. The base resistors also enable the circuit designer to obtain a larger fan-out from Q_0, up to a limit, of course.[5] The factors affecting the

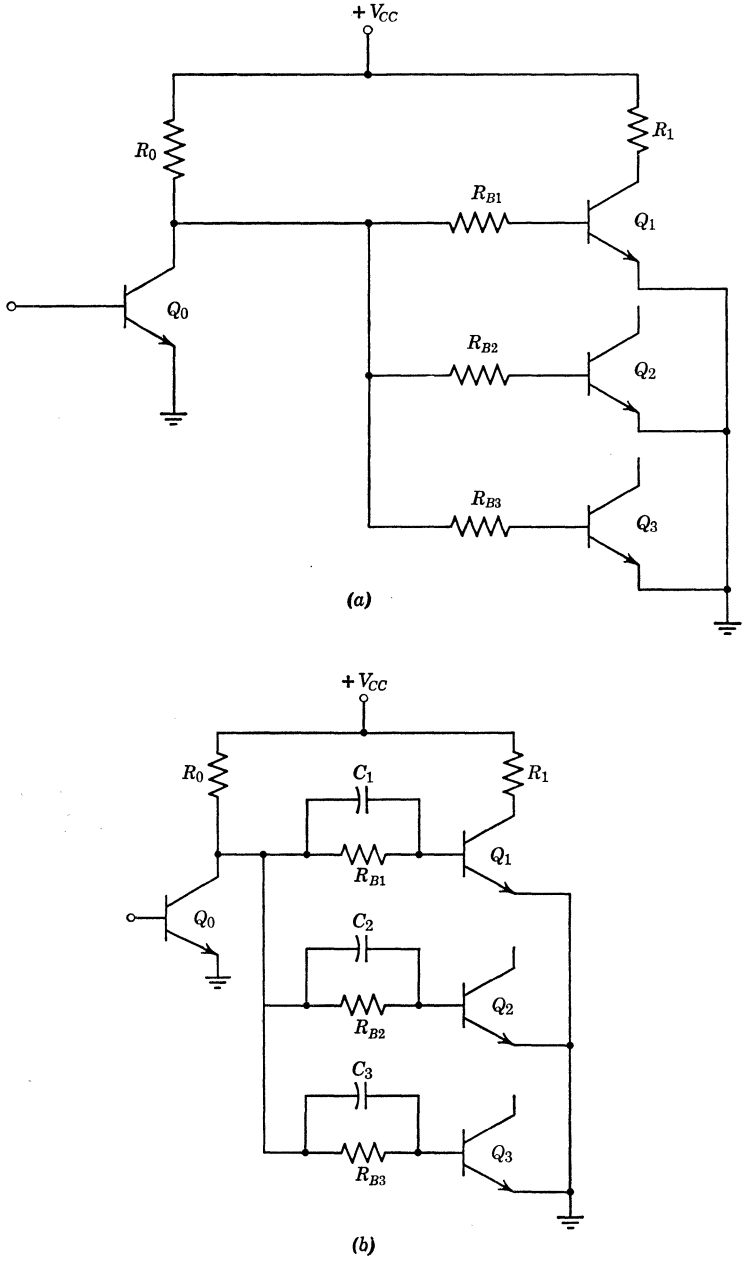


Fig. 9.7 Modified DCTL versions. (*a*) DCTL with base resistor added. (*b*) Speed-up capacitors shunting the base resistors.

switching speeds of the DCTL circuit were discussed (p. 108). Switching speeds can be significantly improved by shunting the base resistor with a speed-up capacitor (Fig. 9.7*b*). This configuration is often referred to as Resistor-Capacitor Transistor Logic or RCTL.

9.3 RESISTOR-TRANSISTOR LOGIC—RTL

Basic RTL Concept

In normal circuit work, a resistor is usually cheaper and more reliable than semiconductors—diodes and transistors. In integrated circuitry this is not necessarily true. In fact, the reverse is usually true. Nevertheless, Resistor-Transistor-Logic, commonly known as RTL, is widely used (though not necessarily in integrated circuits, particularly fully integrated) and has several advantages which merit consideration. Figure 9.8 shows a simple 3-input RTL circuit which is either a NOR or a NAND circuit, depending of course on signal definition.

The operation of the circuit is quite simple. Suppose we arbitrarily define ground level as "0" and a negative voltage as "1." When all three inputs V_1, V_2, and $V_3 = 0$ (i.e., at ground level), the voltage V_B at the base of the transistor Q_0 is slightly more positive than ground since the base is tied to a positive voltage, $+V_{BB}$ through resistor R_4. Q_0 is cut off and the output voltage V_0 tends to fall to the supply voltage $-V_{CC}$. However, V_0 is caught at $-V_{\text{clamp}}$ by the action of the clamping diode D_0. $-V_{\text{clamp}}$ is of course less negative than $-V_{CC}$. If any of the three inputs are negative, the

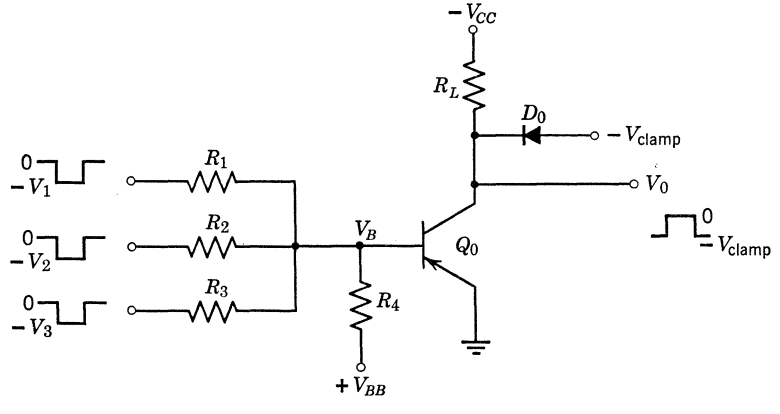


Fig. 9.8 Basic diode-clamped resistor-transistor logic circuit.

current flow through its corresponding resistor pulls the voltage V_B to some negative value. This draws current from the base of Q_0 and turns it ON and drives it into saturation. Here, the output voltage V_0 is determined by the $V_{CE(SAT)}$ of Q_0. Thus for negative-going signals, defined as "1," the circuit performs the NOR function. Conversely, for the positive-going "1" signals, it performs the NAND function.

The Reasons for Diode-Clamping

The circuit shown in Fig. 9.8 could perform the desired functions without the clamping diode D_0. However, some very worthwhile advantages are realized by using the clamp. First of all, the diode clamp enables the circuit designer to standardize the negative level of the output signal, that is, a digital "1," as we have previously defined, clearly and somewhat independently of the amount of output current drawn at that signal level. This enables us to use a higher voltage supply $-V_{CC}$ and higher R_L such that the combination is more truly a constant current source. Hence the current available for driving the fan-out stages is almost equal to the collector current when transistor Q_0 is ON.[6] Another advantage is that if the number of fan-out stages driven by Q_0 is small, then these transistors will not be saturated harder than if the number of fan-out transistors were larger. Finally, the clamp assures that the collector-to-emitter breakdown-voltage rating of the transistor will never be exceeded.

Advantages of RTL

Although the combination of R_4 and $+V_{BB}$ is not essential to the fundamental operation of RTL, it acts as a constant current source and provides the reverse-base current. This current provides the base-to-collector leakage current, and eliminates the need to reduce the base input current to zero when turning Q_0 OFF.

The use of the resistors as coupling elements allows larger signal swings, which in turn permits larger fan-ins and fan-outs. Also, because of the wider signal swings, the noise immunity of the circuit is considerably improved. The speed of RTL is basically limited by Q_0 and by limited overdrive available because of resistor current-summing logic node, but the circuit designer can improve the speed of operation to some extent by using lower values of resistors. However, if reduction in power dissipation is of greater importance, then the values of the resistors have to be larger. RTL is a simple and cheap method of logic, which is particularly well suited for low or moderate speeds of operation.

Disadvantages of RTL

RTL has several shortcomings which limit its usage, particularly in higher speed applications. First, the speed of RTL is device-limited, but improvement in speed can be achieved by using higher speed transistors. However, the circuit does not take full advantage of the speed capability of the transistor. The increase in signal swing naturally requires that transistors with higher voltage ratings be used. Also, since a turn-OFF current is provided, care must be taken not to exceed the reverse breakdown base-emitter rating of the transistor. A low $V_{CE(SAT)}$ and a high minimum $V_{BE(ON)}$ are very desirable for an RTL transistor if high fan-ins and fan-outs are to be obtained. Also, a low I_{CBO} and large h_{FE} are desirable for the same purpose.

Since the turn-OFF current is usually small, fall times and storage times are long. The worst situation for storage time happens when the transistor is turned ON by all its fan-in transistors from the preceding stages and the excess base current is the largest. The turn-OFF base current is designed for I_{CBO} at the lowest operating temperature to insure that the base-collector leakage current does not exceed I_{CBO}. Under conditions other than the highest operating temperature, the turn-OFF current may be overcompensated, thereby reverse-biasing the base-emitter junction of the transistor. As a result, the turn-ON delay may be quite appreciable. Rise times are also long in RTL. The worst case is when the transistor turns ON all of its fan-out transistors.

9.4 DIODE-TRANSISTOR LOGIC—DTL

Figure 9.9 shows the basic Diode-Transistor-Logic configuration which is a NOR circuit for a negative-going input signal or a positive NAND.

The operation of this circuit can be readily explained by defining the ground or near ground voltage as "1" and some relatively positive voltage as "0." The divider network, consisting of R_1, R_2, and R_3, is designed such that if all the input voltages V_1, V_2, and V_3 are 0, the base of Q_1 is relatively positive and Q_1 is ON. The output voltage at the collector of Q_1 is almost ground if the $V_{CE(SAT)}$ of Q_1 is reasonably low. If any of the inputs now swing to "1," that is, 0 volt, that particular diode conducts. This applies a relatively negative voltage to the base of the transistor which is now cutoff. The collector tends to rise to the supply voltage $+V_{CC}$ but is clamped at $+V_{clamp}$ by the action of the clamping diode D_0. Capacitor C_1 is used to provide an overdrive current during switching time. This reduces the switching time to some extent.

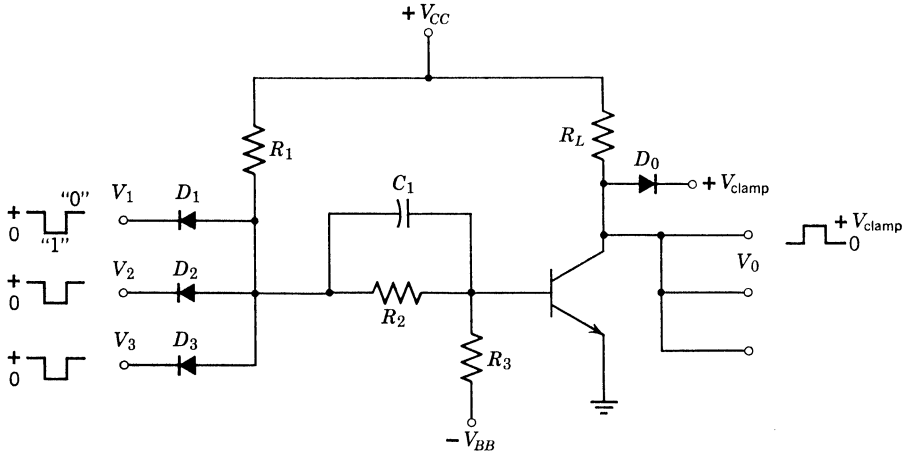


Fig. 9.9 Basic diode-transistor logic circuit (negative NOR).

The circuit shown in Fig. 9.10 is a positive NOR obtained by reversing the input diodes. The resistor divider is now adjusted such that Q_1 is cut off. With ground inputs to the diodes, the diodes do not conduct because the resistors are such that node A is also at ground. This insures that node B is negative, thereby cutting Q_1 OFF. When any of the inputs go positive, the corresponding diode or diodes conduct. Node A goes positive, making the base of Q_1 also positive. Q_1 therefore turns ON, and its collector is now close to ground poten-

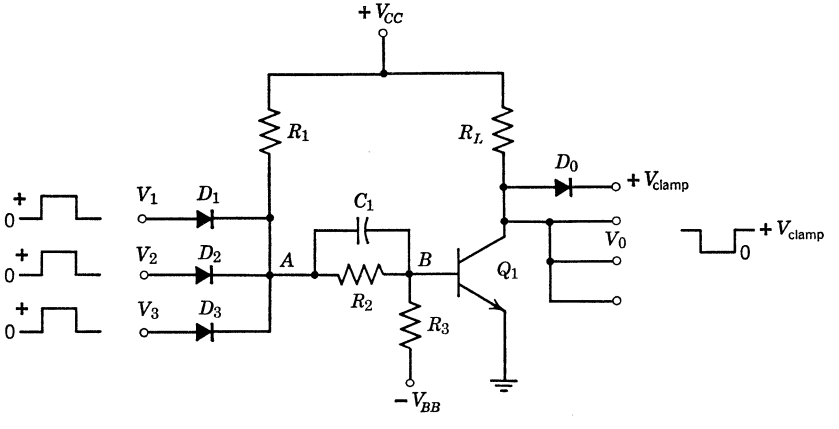


Fig. 9.10 DTL positive NOR circuit.

tial. In comparing this circuit with that of Fig. 9.9, the negative NOR circuit has a slight speed advantage over the positive NOR. In the negative NOR, the resistor-divider network can be designed so that the transistor with the lowest h_{FE} will be just saturated, thereby reducing the storage time.[7]

One of the major drawbacks of DTL is its limitation in fan-ins. Irrespective of whether the circuit is a positive or a negative NOR, when Q_1 is saturated, the following fan-out stages that it drives are OFF. The turn-OFF voltage seen by these stages' transistors is the sum of $V_{CE(SAT)}$ of Q_1 and the forward drop across the conducting gating diode of each stage. Consequently, each of the fan-out transistors demand a larger turn-OFF current from their respective R_3 and $-V_R$ source, and this limits the fan-in capability of DTL circuits. As compared to RTL or RCTL, DTL has one definite advantage in that the spread of $V_{CE(SAT)}$ and its magnitude are not quite as critical.

9.5 LOW-LEVEL LOGIC—LLL

The basic DTL circuit can be modified to good advantage by replacing the base limiting resistor R_2 and the speed-up capacitor C_1 by a simple diode as shown in Fig. 9.11. Such a configuration is commonly referred to as Low-Level Logic circuit. In the previously discussed DTL circuit the transistors are driven through the base resistors by a relatively large voltage swing from the diode gates. On closer examination, it is found that the actual voltage swing at the base required to turn the transistor ON and saturate it is comparatively small. In

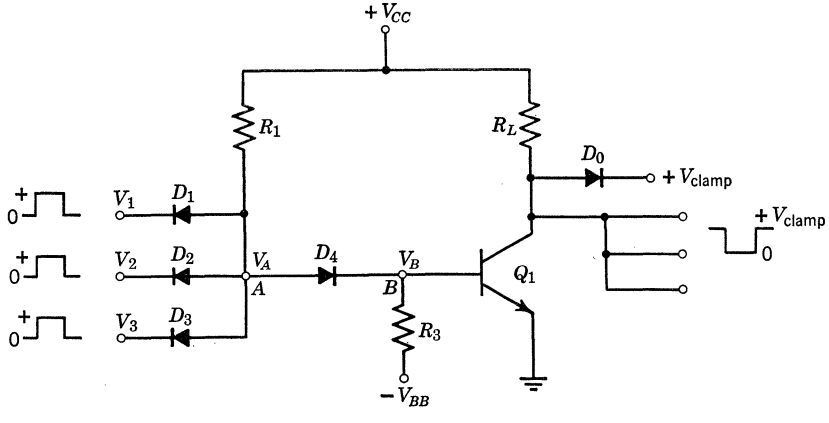


Fig. 9.11 Basic low-level logic circuit.

most cases the required voltage swing at the base is less than a volt. The LLL circuit operates by switching a constant d-c current into the base of the transistor, or out of it. This can be easily done by the diode gate having a very narrow spread of output voltage swing.

Diodes D_1, D_2, and D_3 along with resistor R_1 form a negative OR diode gate or a positive AND diode gate. Any relatively negative input (near ground), resulting from saturated transistor in the preceding stage, will clamp node A near ground potential. When all the inputs are simultaneously positive, the input diodes become reverse-biased because the inputs are more positive than the most positive voltage that node A can swing.

In the first condition, when either one or more inputs are near ground, node B is negative and causes transistor Q_1 to be cut off. The actual turn-off voltage and current are a function of the current through D_4 and R_3 less the leakage current of Q_1.

Conversely, when all the inputs are concurrently positive, node A will swing positive until all the current supplied by R_1 will flow through D_4 to R_3 and Q_1. Transistor Q_1 will now turn ON because node B will be positive. The positive voltage excursion of node A will be determined by the forward drop of D_4 and the V_{BE} drop of Q_1. To improve the noise immunity of the circuit, one or two additional diodes are used in series with D_4.

The greatest advantage of LLL over DTL is the reduction in resistors possible with this approach. With the offset diodes at D_4 it is also possible to operate R_3 returned to ground to eliminate a power supply, while still retaining much of the cut-off noise threshold. The low-voltage swing resulting from base clamping and output clamp D_0 also make it possible to operate the circuit with lower voltages and smaller resistances. Smaller and fewer resistors mean less stray capacity, and clamped signals result in operation over a smaller portion of the time-constant charging curve.

Large fan-in capability is a function of only input diode leakages. Fan-out or drive capability is a function of R_1 and its ability to saturate the transistor with its minimum beta and load resistance. Noise threshold with the transistor OFF is a function of the saturated driving transistor voltage plus the input diode ($D_1 - D_3$) drop subtracted from the forward voltage drops, V_{D4} and V_{BE} of transistor Q_1.

9.6 NONSATURATING LOGIC CIRCUITS

In the saturated transistor logic circuits, the storage time is a significant part of the signal propagation time. This part of the delay can only be reduced by avoiding operation of the transistor in the

saturation region. Nonsaturating circuits avoid this portion of the delay and thereby give much faster operating speeds. The principal disadvantages of this type of logic are the increased power dissipation requirements of the transistors, as well as the other components, and an increase in component count, which adversely affects the reliability of the circuit and increases the cost of the end product. There are several types of nonsaturating circuits used in digital computers. We are limiting our discussion only to two most commonly used types.

Current Mode Logic—CML

Figure 9.12*a* shows the fundamental configuration of the current-mode logic circuit. Basically this is a differential type split-load amplifier with the emitter follower output driving a common-base stage. This type of circuitry involves a signal swing about an operating point rather than discrete level ON and OFF switching. Since the base of transistor Q_2 is tied to ground, it is normally conducting in the active region. The current through Q_2 is determined by $+V_{CC}$, R_{L2}, R_E, and V_{EE}. The output voltage V_2 at the collector of Q_2 is at some d-c level determined by the V_{CE} drop of the transistor. This quiescent operating condition is the result of the base input of Q_1 being at a value more negative than V_E, thereby maintaining Q_1 at cutoff. The collector of Q_1 is therefore positive. The outputs of the two transistors V_1 and V_2 are complementary, and in some instances this convenience can be exploited to good advantage in the logical design of the system. If only one output is desired, then the second transistor Q_2 can be removed and the emitter of Q_1 can be clamped to ground by a diode (Fig. 9.12*b*).

The major drawback of this type of circuitry is that the quiescent operating levels of the output and input signals are different. This, of course, presents a problem when cascading similar stages in a logical chain. If identical stages must be cascaded, then it is necessary to intersperse some level restoring circuits after each stage. One simple method of doing this is shown in Fig. 9.13. The Zener diodes and the current sources in each of the collector circuits assures that the output will be at the required levels for coupling to a similar stage.[8] As a result of putting the current sources in the collectors, the changes in the Zener voltages appear at the collectors and not at the respective bases of the following stages.

Another possibility of solving the problem of input-output level incompatibility is to alternately cascade stages with complementary transistors. For instance, the *NPN* stage of Fig. 9.12*b* can be followed by *PNP* stages as shown in Fig. 9.14*a*. To increase the fan-out

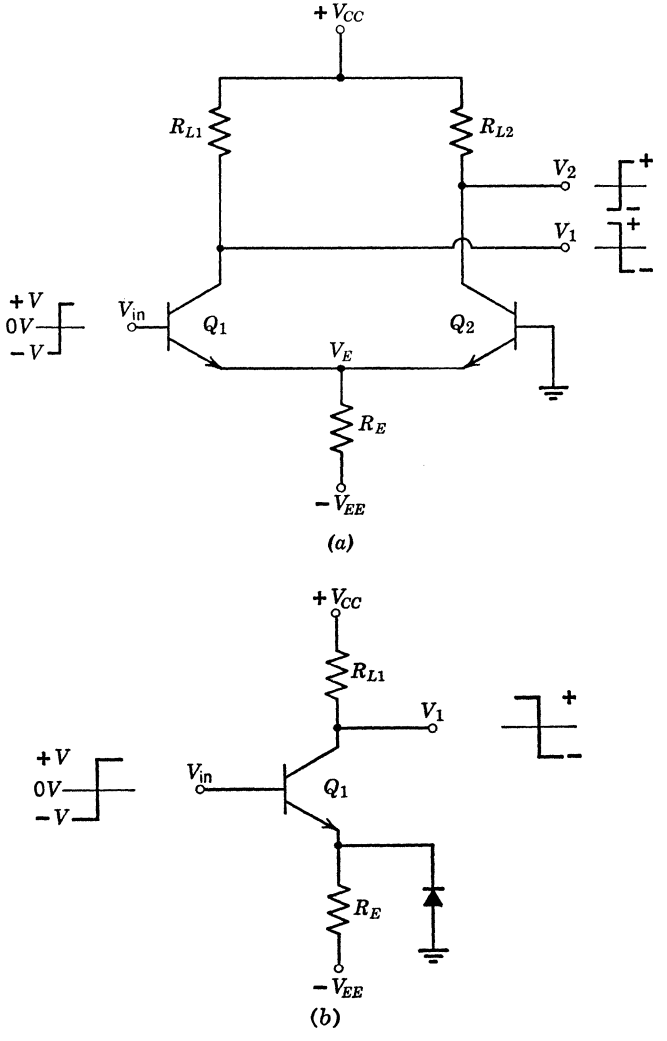


Fig. 9.12 Basic Current Mode Logic circuit. (*a*) CML circuit with complementary outputs. (*b*) CML circuit with single output.

capabilities, an emitter follower is often inserted at the output as shown in Fig. 9.14*b*.

To summarize, CML results in the following advantages:

1. Nonsaturating switching and low-impedance drive give high-speed operation.

2. Transistors with moderate h_{FE} can be used.
3. Base-emitter breakdown and $V_{CE(SAT)}$ are relatively unimportant.
4. Uniform rise, fall, and delay times are obtained because transistor parameters such as cut-off frequency, capacitances, etc., are functions of transistor geometries and not subject to wide variations.
5. By proper circuit design, d-c operation can be stabilized by making the emitter resistor larger than the base resistor.
6. Since CML circuits are very similar to differential amplifiers, the common-mode voltage gain can be made less than one. Thus, noise on the power supply lines can be attenuated and prevented from adversely affecting the signal.

Current-Inhibit Logic

The basic CML circuit of Fig. 9.12*a* can be easily modified to give another type of nonsaturating circuit logic. Such a scheme (Fig. 9.15) can perform and simplify many current-mode logic functions. The *PNP* transistor Q_0, along with resistor R_0 and diode D_0 form a simple CML circuit similar to that in Fig. 9.12*b*. When Q_0 is ON its collector current is dumped into $-V_{EE}$ supply through R_E. This, of course, inhibits the emitter currents of Q_1 or Q_2 from sinking into $-V_{EE}$.

The collector current of Q_0 must be larger than the emitter currents of Q_1 and Q_2. A double current-inhibit circuit can be constructed by inserting a *NPN* transistor in the emitter of Q_0, whose collector current

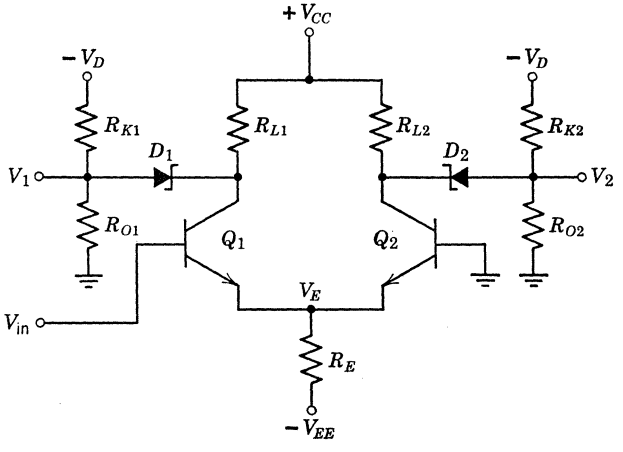


Fig. 9.13 Level restoration in CML with Zener diodes and current sources.

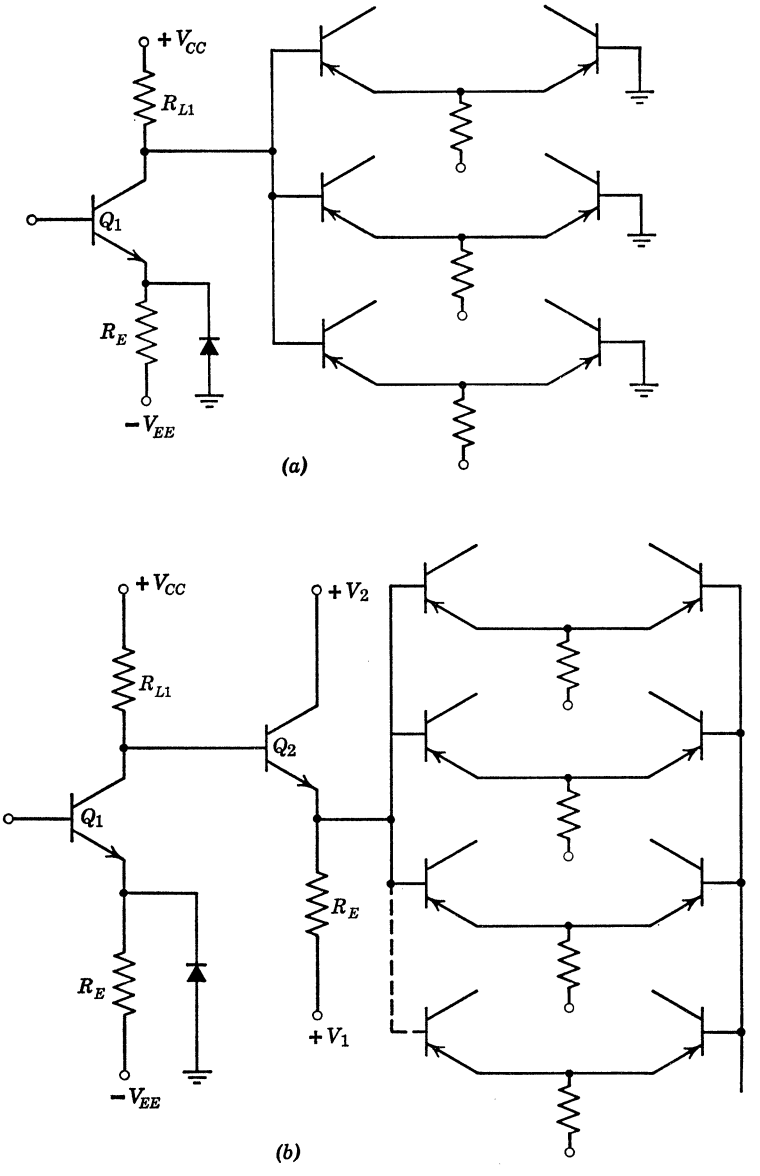


Fig. 9.14 CML cascading with complementary stages: (*a*) Current-mode stage coupling with complementary transistors. (*b*) CML with emitter-follower for high fan-out.

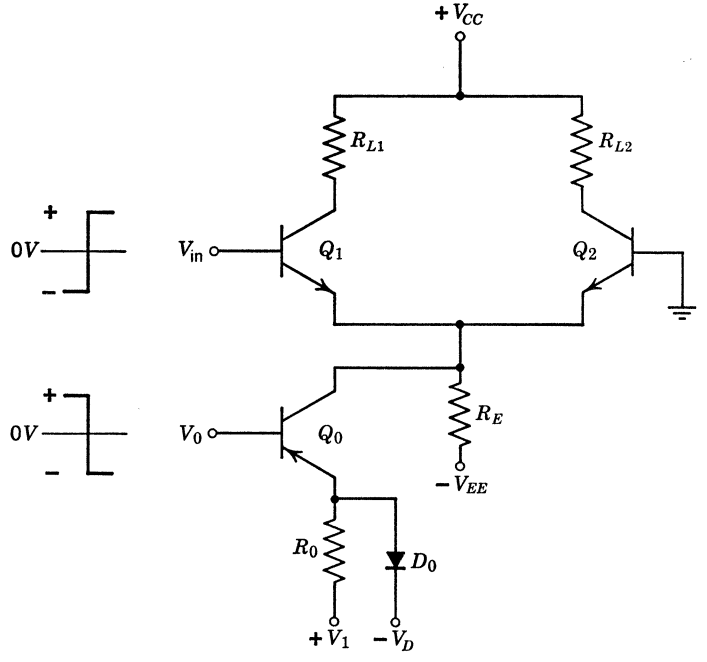


Fig. 9.15 Current-inhibit CML circuit.

would have to be still higher. The disadvantage of this type of logic is that it needs complementary transistors.

9.7 TRANSISTOR-TRANSISTOR LOGIC—TTL or T^2L

Recently a new form of low-level logic configuration has been attracting considerable attention. This circuitry, commonly referred to as TTL or T^2L, has some very promising possibilities and is particularly adaptable to integrated circuitry. TTL is really an extension of the low-level-logic (LLL) discussed earlier in this chapter. Compared to LLL, TTL offers the principal advantage of low-power and high-speed operation.

Although LLL can be made to operate at relatively low-power with only one power supply, if higher operating speeds are desired, we must provide a path for turn-off base current by including resistor R_3 and another power supply $-V_1$ as shown in Fig. 9.11. The TTL circuit (Fig. 9.16) gives us a significant advantage in this respect since only one power supply is used. Here the three transistors Q_1, Q_2, and Q_3

replace the three gating diodes D_1, D_2, and D_3 of Fig. 9.12. The logical operation of this circuit is identical to the LLL positive NAND in Fig. 9.11. Such a circuit is called a "Contiguous-Collector TTL-NAND Circuit,"[9] because the collectors of the gating transistors are all tied to a common node B.

To understand the operation of this circuit, we must assume that all the inputs are driven by similar stages and all the three transistors connected to the three inputs are OFF. The supply voltage $+V_{CC}$ and R_1 essentially provide a constant current to the node A. Since the base of all three coupling transistors are tied to A, the base current supplied to transistors Q_1, Q_2, and Q_3 turns them ON and saturates them. The collector currents of the coupling transistors all flow into node B, and the sum of these make up the base current of Q_0, which is then turned ON. Q_0 is driven into saturation.

If at least one of the input transistors is ON, say Q_4 connected to input V_3, the current flowing into node B from Q_1 and Q_2 will be diverted into the collector of Q_3, and from there into its emitter and then to ground through Q_4. The voltage is not sufficiently positive to turn Q_0 ON. In either case, the coupling transistors are saturated.

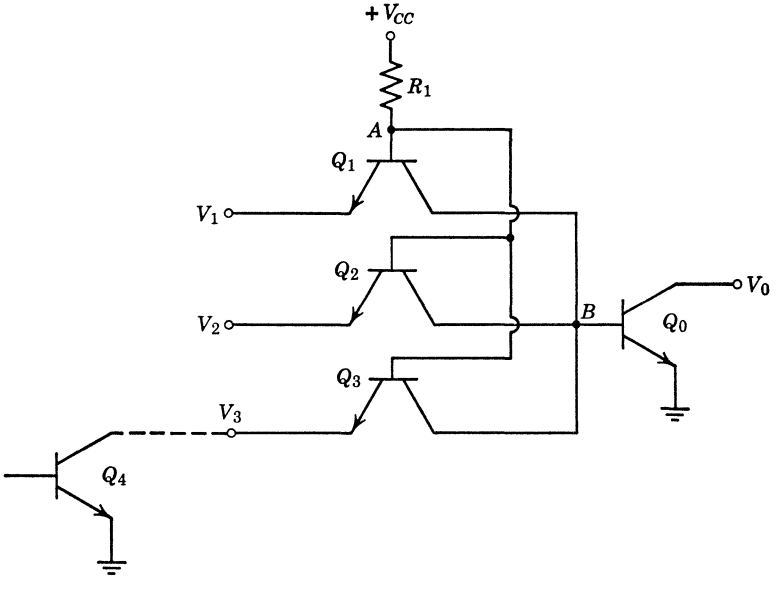


Fig. 9.16 Basic Transistor-Transistor Logic circuit (TTL) with contiguous collector.

For the circuit we have considered, the collectors of the coupling transistors were tied together while the emitters were inputs to the gates. Actually it is possible to have a contiguous-emitter configuration by tying the emitters together and using the collectors as the inputs (Fig. 9.17).

At first it appears that the fan-out capability of this circuit would be excellent since each coupling transistor is essentially supplied a constant base current. A closer examination reveals that, while this is true to some extent, current hogging can be a problem, and in practice this limits the fan-out capability. Figure 9.18 shows the inverter transistor of Fig. 9.17 driving a fan-out of 3.

With Q_0 OFF, if the $V_{BE(ON)}$ requirement of one transistor, say Q_6, is higher than that of the other two, then the coupling transistors Q_1 and Q_2 will hog the current I_3 from Q_3, thereby starving Q_6. However, in spite of this, TTL has several advantages:

1. Although it uses more transistors, the reduction in the number of other components, such as diodes and resistors, is a significant advantage, particularly in integrated circuits.
2. Only one power supply is used, and this could be a very prominent factor in some applications, such as aerospace systems.

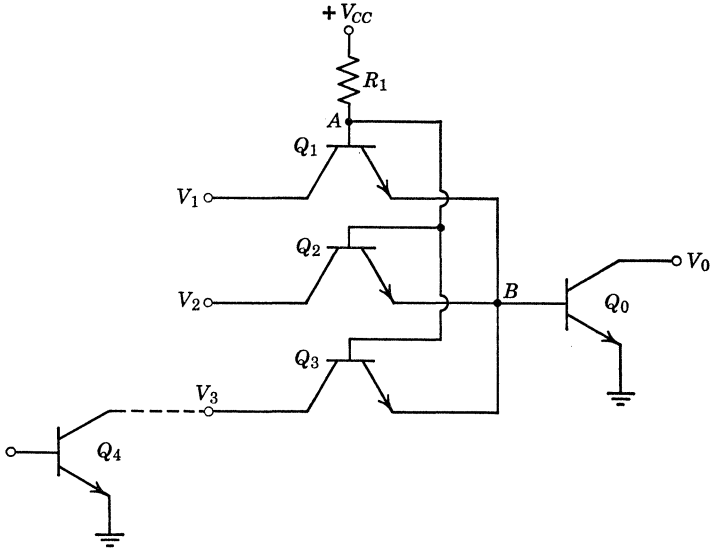


Fig. 9.17 Contiguous emitter TTL circuit.

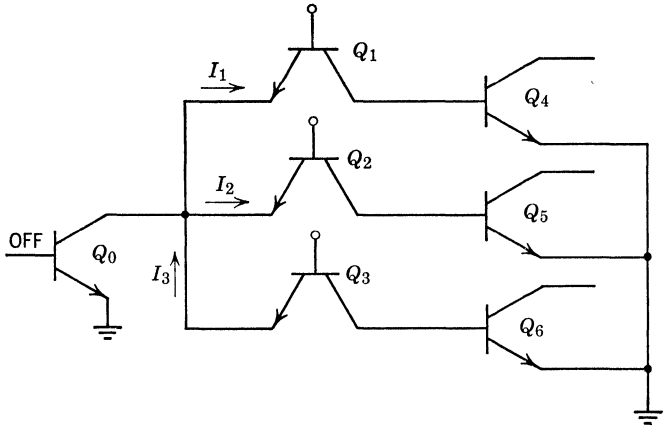


Fig. 9.18 Current hogging in TTL reduces its fan-out capability.

3. Coupling transistors are always ON. This reduces the charge storage problem, which is a speed-limiting factor in other logic circuits, and increases the speed of operation considerably. Foglesong mentions average propagation delays of 25 nanosec at 3 mw dissipation.[10]
4. Noise margins are generally lower than in other types of logic circuits, but lower operating currents reduce noise-margin requirements.
5. This type of logic is flexible in its application. Its low-level operation makes it possible to operate these circuits in conjunction with conventional DCTL circuits.[10]

9.8 EMITTER-COUPLED TRANSISTOR LOGIC—ECTL

Integrated circuits in themselves place several exacting demands and rigid constraints on the circuit designer because of their inherent limitations. Additional demands, such as higher switching speeds, shorter propagation delays at lower power dissipations, simpler circuit configurations, higher fan-in and fan-out capabilities, and better noise immunity, have prompted the search for newer circuit types and configurations. A modified version of the Current-Mode Logic has recently been considered as particularly promising for integrated circuits by some vendors. The basic circuit, called the Emitter-Coupled Transistor Logic or ECTL is shown in Fig. 9.19.

This circuit is similar to CML in many respects. Basically it is a

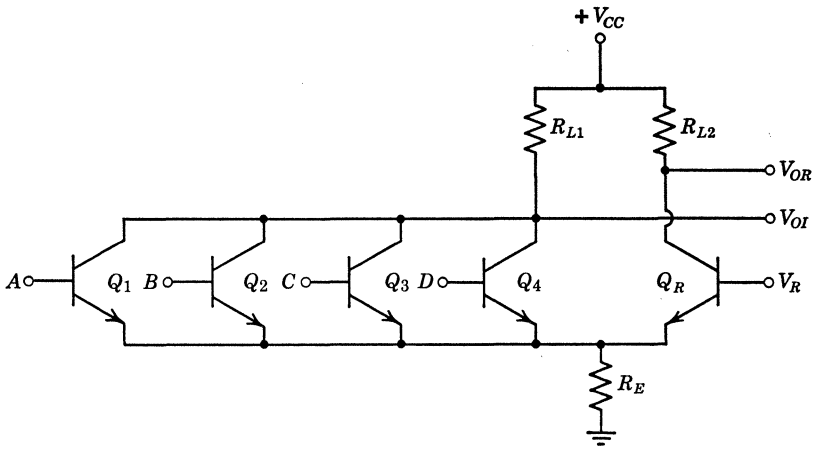


Fig. 9.19 Basic emitter-coupled transistor logic circuit.

current-mode switch operated in the nonsaturating mode. Q_R is the reference transistor with its base tied to a fixed bias such that it is always conducting when the other four transistors are OFF. The output of this transistor, V_{OR}, is at some less positive voltage determined by the $+V_{CC}$ supply, the resistors R_{L2}, and R_E. If the relatively more positive voltage is defined as a digital "1," then we can say that under the conditions a "0" is available at V_{OR}, and a "1" at V_{OI}. Now if a positive "1" signal is applied to any one or more of the bases of Q_1 through Q_4, that particular transistor (or transistors) will conduct. Since R_E, which is connected to ground (in some cases it could be tied to a negative potential), serves as a constant current source, current conduction through Q_R diminishes. The output voltage becomes relatively more positive or "1," and V_{OI} becomes relatively less positive or "0." Thus it is seen that for positive "1," the circuit is an OR if the output is taken from V_{OR}, and it becomes a NOR if the output is taken from V_{OI}. If the more positive voltage is defined as a "0" then the circuit becomes an AND and a NAND for the same respective outputs. The availability of complementary outputs is a very convenient feature which can be used to good advantage in some logical schemes. With ECTL the problem of level restoration is present and in most cases is solved by feeding the two outputs into two emitter followers and using their outputs for logical interconnections. Besides providing signal compatibility, the emitter followers serve another very useful function. The emitter

follower has a low output impedance and this gives the basic ECTL gate a much larger fan-out capability.

Some of the outstanding features of ECTL reported in current literature are:

1. Using output emitter followers, the noise and cross-talk problem is greatly minimized because[12] (*a*) the low output impedance attenuates the cross-talk between inputs due to capacitive coupling; (*b*) high input impedance results in the transmission of small currents between stages thereby reducing cross-talk between adjacent signal lines; (*c*) since the current flow in the circuit is essentially constant regardless of the logical state, noise pulses generated in supply lines and ground system are negligible.
2. Nonsaturated operation of transistors eliminates the problem of delays due to storage effects.
3. The low output impedance of the emitter followers gives a large fan-out capability.
4. The high input impedance of the gate gives it good fan-in capabilities.
5. It is possible to obtain high speed-high power operation or low speed-low power operation. Computing rates of better than 1 mc/mw power dissipation have been reported.[13]
6. As compared to DCTL circuits, ECTL is immune to current hogging, which develops because of $V_{BE(\mathrm{ON})}$ spreads of transistors.[11]
7. Although close matching of transistor characteristics is desirable for superior performance, a high degree of matching is not mandatory for satisfactory operation.
8. Since the reference transistor, Q_R, is biased separately, it is possible to provide compensation for drifts in output levels because of variations in supply voltages or temperature, by providing a self-regulating circuit for the bias network of Q_R.[12]

9.9 LOAD-COMPENSATED DIODE-TRANSISTOR LOGIC—LCDTL

The basic low-level-logic circuit, shown in Fig. 9.11, has a high operating speed at reasonably low-power levels. While only one "speed-up" diode is shown, in actual practice, two, or even three, such diodes are used in series to obtain the desired logic levels. Larger logic levels can be realized by increasing the number of series diodes. A circuit using two speed-up diodes is shown in Fig. 9.20.

Although this circuit has a relatively high-saturation resistance tolerance, the current required for turning OFF transistor Q_1 must flow either through R_3 or through diodes D_4 and D_5 as recovery current.

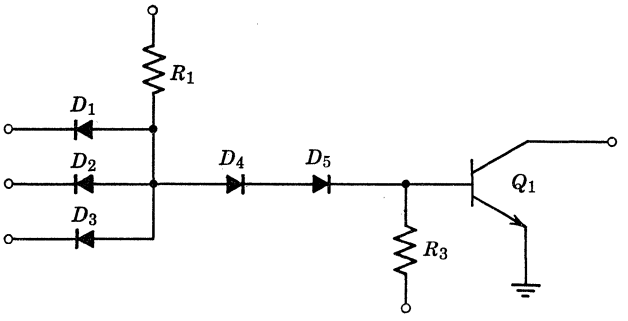
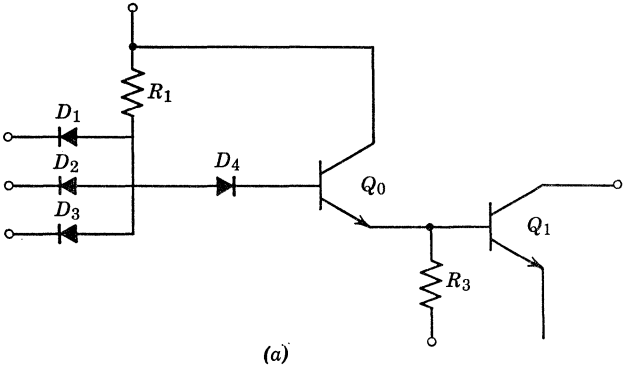
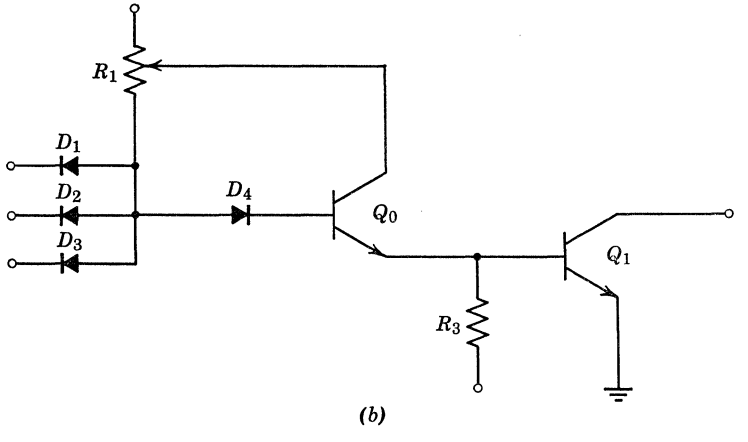


Fig. 9.20 LLL circuit with two series speed-up diodes.



(a)



(b)

Fig. 9.21 High-gain resistor-controlled LLL. (*a*) Diode D_5 is replaced by the emitter-base junction of transistor Q_0. (*b*) Power dissipation and additional gain can be resistor controlled by tapping resistor R_1.

Thus, a compromise between circuit speed and gain must be made. This problem is particularly troublesome if R_3 is grounded to avoid the use of a second power-supply voltage.

Fabricating this circuit in integrated form offers some interesting possibilities, since diodes can always be obtained from transistor structures. In this particular case, either D_4, D_5, or both can be formed by using the emitter-base junctions of transistors. Such a transistor can also be used to increase the total gain of the circuit to the point at which gain no longer presents a problem. Figure 9.21*a* shows diode D_5 replaced by transistor Q_0. It is quite obvious that Q_0 operates as an emitter-follower. The power dissipation of this circuit is high and gain dependent. By using a tapped resistor, R_1, as shown in Fig. 9.21*b*, both the power dissipation and the additional gain can be resistor controlled. In either case the overdrive is excessive at low fan-outs.

The speed-power dilemma of these circuits can be solved by using a clamping diode as a shunt around the amplifying stages, that is, Q_0 and Q_1. The circuit is shown in Fig. 9.22.

The excess current from R_1, which overdrives Q_0 in the other two circuits of Fig. 9.21 now bypasses Q_0 via the clamping diode D_C. Consequently, the emitter-follower, Q_0, draws just enough current from the power supply to maintain the current requirements of the load. Thus, overdrive at low fan-outs is prevented. As the load current increases, the drive current also increases, and thus the circuit is self-adjusting, or load-compensated. The clamping diode also restricts voltage swings and thereby reduces the effect of line capaci-

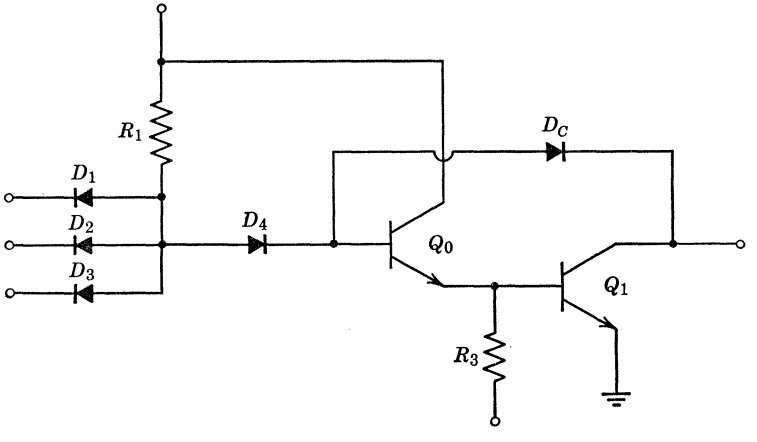


Fig. 9.22 The LLL circuit with the shunting clamp diode.

TABLE 9.1

SUMMARY OF LOGIC CIRCUITS

Circuit Type	Propagation Speed	Power	Noise Immunity	Fan-out Capability	Suitability for Integrated Fabrication	Comments
DCTL	4	4	1	2	4	Current hogging problem requires close matching of transistor V_{BE} and base resistor
RTL	1	2	2	1	2	Number of resistors and the tolerances required makes it less desirable for integrated fabrication
DTL	2	3	4	2	2	The resistor divider network and the speed-up capacitor are undesirable features
LLL	2	3	4	2	3	Replacing the resistor-capacitor combination by coupling diode facilitates integrated fabrication
TTL	4	4	1	4	4	Input leakage current is a function of reverse β
LCDTL	4	3	4	4	3	Although total component count is increased, it is still suitable for integrated circuits because the added components are diodes and transistors
CML	4	2	1	3	1	Differences in input and output quiescent levels increase the component count significantly
ECTL	4	2	1	3	1	The need for reference supply increases the component count

Legend of symbols: 4 = Excellent, 3 = Good, 2 = Moderately Good, 1 = Not so good.

tance on switching speed.[14] Signal swings similar to those of DCTL and TTL can be used with this circuit, along with the relatively high tolerance to saturation resistance of the basic DTL circuit. Although the number of components used is greater than in any of the usual single-stage circuits, the tolerances of the required components are considerably looser.[15] This, along with the fact that the additional components in this circuit are diode and transistor (and not resistors and capacitors), makes it particularly attractive for integrated circuit fabrication.

9.10 SUMMARY OF LOGIC CIRCUITS CHARACTERISTICS

It is quite apparent that no single logic circuit type is best or contains all the desirable characteristics. The selection of a circuit type naturally depends on the particular situation and the compromises or the trade-offs permissible for the application concerned. A quick reference chart, indicating the various circuit types and some of the principal pertinent characteristics would, perhaps, be helpful. In Table 9.1, only the basic circuit types are considered. The ratings given to the various parameters are not intended as comparisons of any circuits, integrated or otherwise, used or supplied by any company or vendor. The weights assigned to the circuits reflect only the author's past experiences with them or his own personal judgment. Any engineer with different experiences on the same circuits, under different conditions, would undoubtedly assign different ratings.

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section 4

The partially integrated circuit

The multiple-chip approach

10

10.1 WHY PARTIAL INTEGRATION?

The three approaches for integration of custom circuits described in Chapter 8 certainly extend the range of circuits that can be designed by the users' engineers. Within the practical and established limitations, an almost unlimited variety of circuit configurations is theoretically possible. Nevertheless all three schemes are geared to ultimate production by full integration by the particular vendor concerned, and so the inherent limitations imposed by the integrated circuit state-of-the-art technology restrict the circuit designers to comparatively simple configurations. In practice this means confining the designs mainly to digital-type logic circuits.

In some applications, mainly commercial or ground-based military equipment, it may be acceptable to use integrated units for digital circuitry while using some other approach (maybe even conventional discrete components) for more complex circuits. Such applications may benefit from characteristics other than the possible weight and volume reductions by using integrated circuits. On the other hand in some other applications, such as airborne or spaceborne systems where weight and volume assume paramount importance, such a scheme may be totally unacceptable. Here, the potential of using integrated units in all circuits, digital and linear, must be exploited to the fullest extent. Integration of just digital circuits is not enough. For instance, in an airborne or spaceborne computing system, integration of the logic circuits alone would hardly be justifiable if the memory, input-output, and other linear circuits are not integrated or reduced to compatible dimensions of weight and volume by some means. If integration of the linear and more complex circuits is not possible because of inherent limitations or undesirable compromises in performance, then an alternative method becomes a necessity. Partial integration by the multiple-chip method fills the bill nicely in some cases, and this approach is the subject matter of this chapter. There are several variations of this approach which, in contemporary microelectronic parlance, is often referred to as just "the chip approach." In this approach the circuit is constructed piece by piece on more than one chip or substrate. The active elements are diffused on one or more

semiconductor chips and the passive elements are likewise grouped on one or several chips. At the present time there are three principal techniques employed by the vendors in the design and manufacture of partially integrated circuits. We now describe them, along with their main advantages and shortcomings.

10.2 ISLANDS ON TO-5 HEADER

Description of the Island Approach

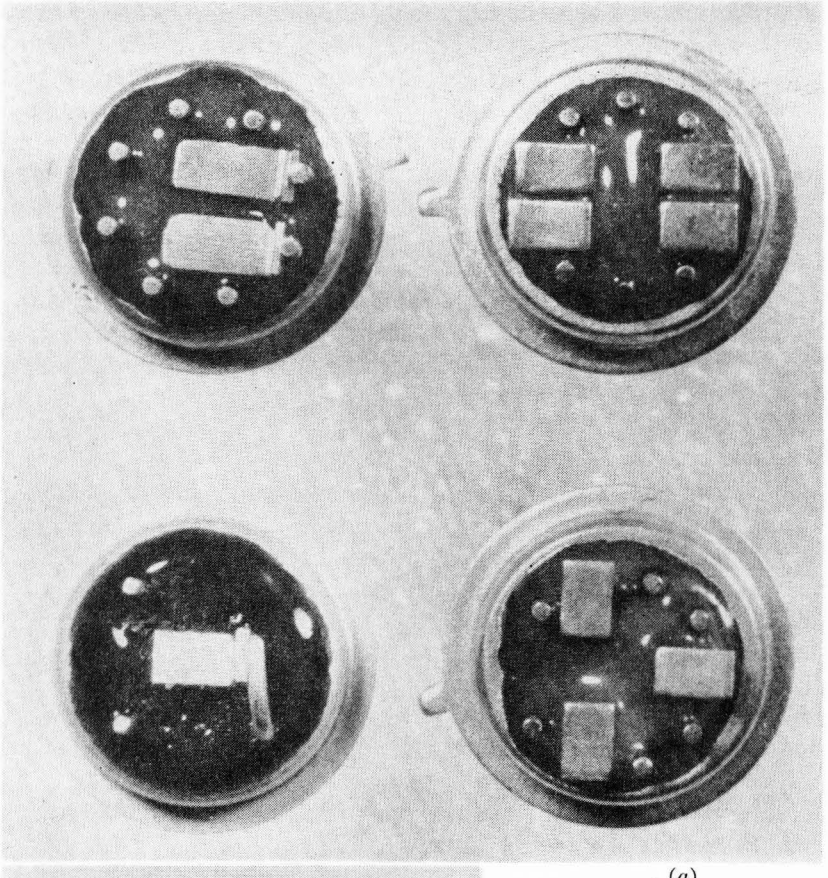
This approach consists of tiny islands mounted in TO-5 cans. The islands are directly connected to the header leads, but isolated from the header itself. Each island is a metalized land having an area of either 50 × 80 mils or 50 × 120 mils. A TO-5 can is capable of accommodating a maximum of four such islands. Separate individual semiconductor chips, containing one or more active or passive elements are mounted on the islands. The bottom surfaces of the semiconductor chips make electrical contacts with their respective islands and consequently with the leads connected to them. Figure 10.1*a* shows four TO-5 cans with the four possible island arrangements on the headers. In this picture the islands are blank, with no circuit elements mounted on them. Figure 10.1*b* shows four islands on TO-5 header with circuit chips mounted.

Typical Component Elements Used

There are theoretically no restrictions on what semiconductor chips can be mounted on the islands. Obviously the size of the chip is restricted by the land area of the island. More than one chip can be mounted on an island if the circuit configuration is such that the elements concerned are tied together at a circuit node. Some of the typical elements used in this approach are the 45 × 45 mil large geometry transistors, such as the 2N1613, and the 25 × 25 mil small geometry transistors, such as the 2N914 and the 2N917. Low-power Zener diodes and standard 25 × 25 mil silicon diodes have also been used. By using 50 × 50 mil back-biased diodes, capacitors in the range of 100 to 1000 pf have been used. One vendor indicates that resistors can be deposited directly on the islands. Such resistors have a resistance range of 10 ohms to 1 megohm with tolerances of ±10%, a temperature coefficient of ±500 ppm/°C and are capable of dissipating up to 100 mw.

Advantages of this Approach

The island approach has several desirable features which can be utilized to good advantage. Depending on the area of the silicon chips in question, any semiconductor devices available in the vendor's exist-



(*a*)

(*b*)

Fig. 10.1 The island approach. (*a*) TO-5 headers mounted with one, two, three, and four blank islands. (*b*) Circuit chips mounted on TO-5 header with four islands (courtesy Fairchild Semiconductor).

ing product lines can be readily used. If deposited resistors are used, the increase in the resistance range (as compared to the diffused resistors) gives the circuit designer greater flexibility. TO-5 cans with 10-lead headers containing 1, 2, 3, and 4 blank islands ready-mounted are stocked by the vendors, with no special tooling involved. This, along with the fact that special masks are not fabricated for the semiconductor devices, considerably reduces the final costs of the units as compared to the fully integrated circuits. Also, delivery time can be much shorter. As far as the user is concerned, perhaps the most significant advantage of this approach is the freedom to make changes in the circuit configurations and component values after the first samples are fabricated and tested. This is possible because there are no masks involved in the fabrication process.

Limitations of the Island Approach

There are some limitations to this approach and it is advisable that the equipment manufacturers' engineers be aware of them before starting on their circuit designs. Since the circuit elements can be mounted on the islands, the area between islands and the area between the header leads and the islands are, for all practical purposes, wasted. This naturally reduces the component density within a TO-5 can. A further limitation on the component count is imposed by the recommendation that at least 5 mils spacing, and preferably 10 mils, be allowed between adjacent elements on any island, regardless of whether they are diffused or deposited components.

The number of semiconductor devices that can be mounted on an island is limited to one unless the circuit in question calls for diodes with their cathodes tied together or transistors with their collectors tied together. This phenomenon imposes severe limitations on the circuit designer and is the result of the bottom surfaces of the semiconductor chips making direct electrical contacts with the islands on which they are mounted.

10.3 INDIVIDUAL CHIPS ON TO-5 HEADER

Description of the Approach

Some vendors use a method which is somewhat simpler than the island method for mounting the individual chips. In this method, TO-5 cans with some insulating material on the header are used. Individual component chips are then mounted directly on the insulating substrate, which usually consists of a ceramic disc. Bonded leads are used for interconnections between chips and from the chips to the header leads. In some cases, connections between certain chips are

made by metalized conducting paths. This method extends the possibilities of designing somewhat more complex circuits for several reasons. In the first place, advantage can be taken of the batch process of semiconductor manufacturing. Transistors of the same type can be diffused into one chip and they can be isolated from each other by "through diffusion" or their collectors can be tied together if the circuit requires this. Similarly, the diodes of the same type can be put on the same chip, isolated by "through diffusion," and either their cathodes or anodes tied to a common node if so desired. Diffused

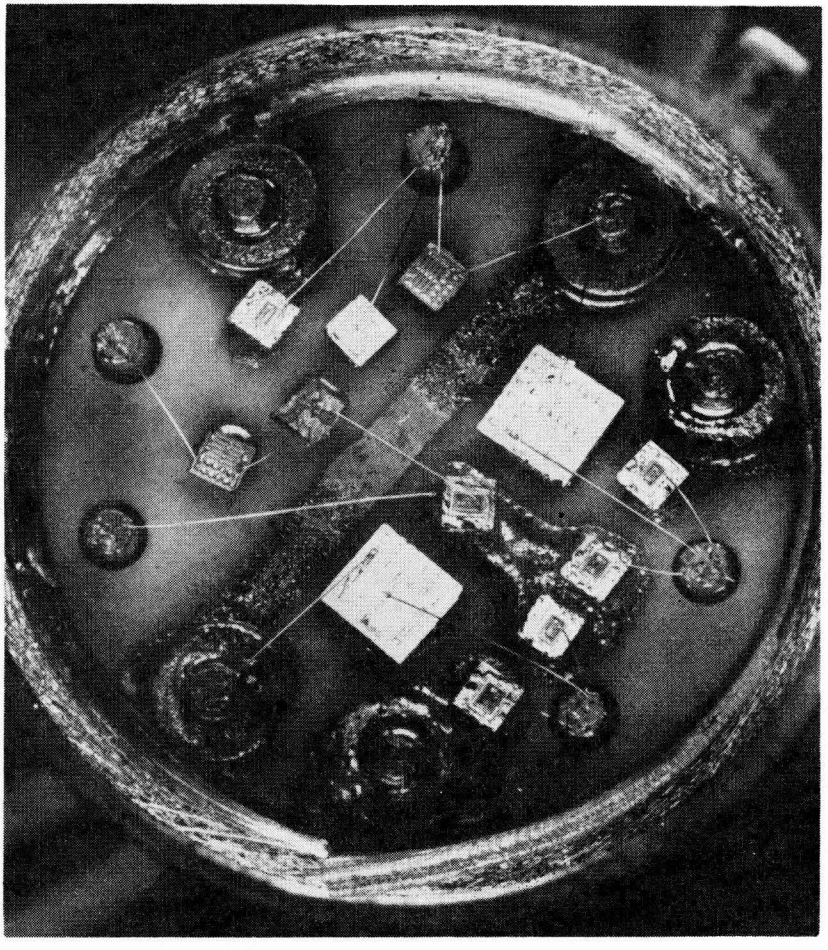


Fig. 10.2 Individual chips on TO-5 header (courtesy Motorola, Inc.).

resistors formed by back-biased diodes can be put on the same chips as the active elements or they can be on separate chips. Depending on the range of values desired, resistors can be made using one or more of the active elements' diffusion processes and can be put on the same chips, of course. The resistors can be tapped at one or more points as required. Figure 10.2 shows a driver designed by Robert C. Green of UNIVAC (St. Paul), which was fabricated to UNIVAC's specifications by one of the vendors using this method. Since each chip is mounted on an insulating material, the chips are naturally isolated from each other.

Typical Component Elements Used

Some of the typical components that have been used with this approach include high-frequency *NPN* transistors in the current range of 0.1 to 500 ma with gain-bandwidths up to 400 mc, 2-nanosec diodes with 10 ma at 1 volt, and 6 to 30 volt 0.5 watt Zener diodes. *P* or *N* type diffused resistors in the 10-ohm to 30-kilohm range with $\pm 10\%$ tolerances, power dissipation of 1/4 watt, and a temperature coefficient of +300 ppm/°C are typical. The parasitic capacitance usually associated with this type of resistor ranges from 0.1 to 1 pf/mil^2. Using back-biased diodes as capacitors, values up to 1000 pf $\pm 10\%$ at 10 to 100 volts are obtainable.

The following dimensions are indicated by one vendor for the standard chips they are presently using:

Components	Area in Mil^2
1. Type 2N834 transistor	20
2. 1/4 watt resistor	50
3. 100 mw resistors	25
4. 254 pf capacitors	50
5. Diodes (equivalent to FT100)	50
6. Diodes (equivalent to FT600)	50

This vendor also indicates that resistor chips with maximum resistance values of 1, 10, 30, and 100 kilohm are available with ten 1% taps and nine 10% taps, with the lowest value being 10 ohms. Standard capacitor chips have the capacitance values of 2, 4, 8, 16, 32, 64, and 128 pf.

Advantages and Shortcomings of This Approach

All the advantages of the island approach also apply to this approach. In comparing it with the island approach it is apparent that the header area can be utilized a little better with this method, resulting in increased component density with the can.

The outstanding advantage of this method is that the initial layout of the chips can be arranged such that a completely integrated circuit may be possible later on. For instance, using this scheme it is possible, in quite a few circuits, to realistically simulate some of the parasitics that are likely to appear later on in the fully integrated circuit. In other words, the partially integrated version can be an excellent first breadboard for the fully integrated circuit to follow.

It should be realized that although more economical use of space in the TO-5 can is possible, the number of chips that can be mounted in a can is still limited by the size of each chip. Furthermore, the number of bonded connections possible on a chip, both for internal interconnections as well as to the header leads, limits the number of chips in a can.

10.4 MULTIPLE DISCS ON TO-5 HEADER

Description of This Approach

This method, which is merely an extension of the previous one, consists of mounting the individual chips on ceramic-disc substrates. The ceramic discs have holes on their periphery, usually 10, and the header leads fit into them. Presently, a maximum of 5 such discs are stacked into a TO-5 can by one vendor. Figure 10.3 shows a TO-5 can with one disc mounted and the other unmounted. The chips on these discs are blanks intended for demonstration purposes only.

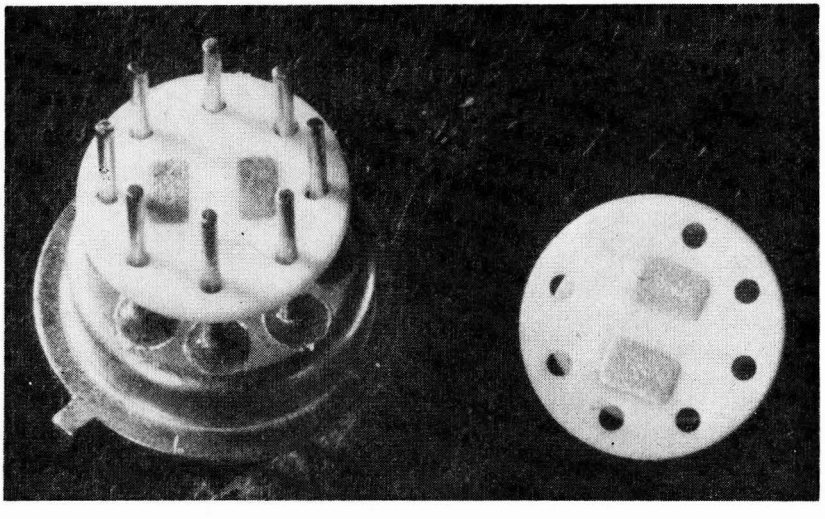


Fig. 10.3 Mutiple ceramic discs on TO-5 header.

Advantages of the Multiple Discs

In addition to the advantages discussed previously, this method has some that are worth mentioning. Chips mounted on the same discs can be internally connected either by bonding or by depositing metalized conductors. Either of these two interconnection methods can be used for connecting the elements to the supporting header leads, which provide interconnections between discs and to the outside world. The metalized conductors for interconnections certainly help in improving the reliability. The circuit designer has a wider choice of components that he can use. Also, he can now design somewhat more complex circuits. Component density is greatly increased and the problem of heat dissipation becomes an increasingly major factor limiting it.

Limitations of this Approach

Since masks are required for deposited interconnections, the cost of these units and the delivery times may increase considerably. Once the masks are made, changes in circuit configurations cannot be made very easily. Perhaps the principal disadvantage of this approach is that a complex circuit with a deck of up to five discs cannot be laid out as breadboard for the future fully integrated circuit. In applications where severe mechanical vibration and shock are likely, this approach is not very suitable. The increased mass within a can could cause serious mechanical problems.

Thin-film semiconductor hybrid integration

11

11.1 WHY THIN FILM CIRCUITS?

Fully integrated circuits certainly have a lot of advantages, particularly their weight and volume factors, which are very significant in such applications as airborne or spaceborne computing systems. But they also have several limitations which oftentimes are quite severe. While the custom-integrated and the multiple-chip approaches undoubtedly widen the horizons for the circuit designer, the inherent limitations of the semiconductor technology restrict the designer to simpler circuit configurations, such as digital circuits, in most cases. His troubles are further compounded by the rather limited range of values in the passive components that are available. Furthermore, the components have loose tolerances, typically $\pm 10\%$, going as high as $\pm 25\%$ initially. Also, these components (passive components, particularly) are relatively unstable with temperature variations, which means that circuits and systems must be designed so that they are operable over a large range of components drifts. Another problem is that it is virtually impossible to take existing proven-out circuits and translate them into integrated form on a direct one-to-one component replacement basis. Invariably, new circuits have to be designed from scratch. Thus, for complex circuits requiring component values of a rather wide range, tighter tolerances, and better temperature stability, it is certainly worthwhile to look into some alternate technology.

Recent developments in thin-film technologies have produced some interesting possibilities. Thin-film processes are briefly covered in Chapter 4, and so they will not be repeated here. Instead, we will attempt to investigate how these developments affect the microminiaturization trend with which this book is concerned. Before we go further, it is quite in order to glance backward and look into some of the reasons why this important technique has been relegated into the background until now.

11.2 PAST DRAWBACKS OF THIN FILMS

Although thin-film technologies have been with us for some time, the glamour and excitement created by integrated circuits submerged

them out of the limelight. Work on them nonetheless continued in several laboratories, resulting in some very significant developments. In spite of the fact that thin films offered better range of component values, tighter tolerances, and greater stability, as compared to integrated circuits, there were two major shortcomings which limited their usage.

In the first place, the weight and volume reduction introduced by the integrated circuit were such that the thin-film approaches just could not match them. For example, a flip-flop configuration could be contained in a flat rectangular 250 × 125 × 35 mils package using integrated-circuit techniques. Using thin-film techniques, a flip-flop circuit of comparable complexity required a typical flat package 700 × 650 × 75 mils dimensions. This, explains, then, at least one of the preferences for integrated circuits over thin films, particularly in those applications where volume is an important factor. There are, of course, other factors too.

11.3 PRESENT STATUS OF THIN-FILM CIRCUITS

A detailed description or discussion of the various advances in this technology is beyond the scope of this book, but a short presentation of some of the highlights is certainly in order.

Passive Components

MOTOROLA SEMICONDUCTOR PRODUCTS. Motorola has been active in the hybrid approach to integration for quite some time. By depositing tin oxide (SnO_2) in line widths of 1 mil, resistors in the range of 100 ohms to 100 kilohms[1] (which can go up to 10 megohms if required) have been indicated. These resistors have power dissipation of 500 mw and typical tolerances of $\pm 10\%$, with temperature coefficient of -300 ppm/°C. Resistivities range from 100 to 3 kilohms/square and the parasitic capacitance associated with such a resistor is 0.015 pf/square mil.

Glass-type (SiO_2) deposited capacitors have capacitance up to 200 pf, with a maximum voltage rating of 100 volts, a temperature coefficient of -100 ppm/°C, and a tolerance of $\pm 10\%$. Using thin-film techniques, Motorola has been able to get an inductance of up to 10 μh by means of a toroid 150 mils in diameter. This inductor has a tolerance of $\pm 10\%$, a maximum current-handling capability of 100 ma, and a figure of merit, Q, of approximately 100.

FAIRCHILD SEMICONDUCTOR. In Chapter 10, we discuss the island approach used by Fairchild. In addition to the diffused chips, Fairchild indicates use of deposited resistors. These resistors range from

10 ohms to 1 megohm and are deposited on chip sizes 50 × 50 mils. Their tolerances are normally ±10% but tolerances of ±5% can be obtained. The maximum power dissipation is 100 mw, and the temperature coefficients are either ±500 ppm/°C or ±200 ppm/°C.

PHILCO. Philco, a division of Ford Motor Company, is a newcomer to this field and recently announced the availability of their first standard-line digital circuits, which are described in Appendix C. Philco thin films use tantalum as the material for resistors, capacitors, and interconnects.[2] Some of the typical component characteristics mentioned by Philco are as follows:[3]

1. Resistors—These resistors have a resistance range of 50 ohms to 500 kilohms with temperature coefficients of −300 to +100 ppm/°C. Philco mentions a tolerance range of ±0.2 to ±10%.
2. Capacitors—For capacitance values ranging from 0.01 to 5 $\mu f/cm^2$, a breakdown voltage spread of 2 to 50 volts is mentioned, with tolerances from ±5% to ±20%. The temperature coefficient of these capacitors varies from 150 to 250 ppm/°C.

Active Devices—Developmental Work

Active devices fabricated with thin-film technologies are not presently available on the market. Several vendors are actively engaged in research in this area with rather encouraging results. The work done at Sylvania and General Electric has been recently reported, and appears very promising.

SYLVANIA ELECTRIC PRODUCTS. Sylvania forms its microcircuitry on ceramic discs 0.01 in. thick.[4] While these substrates are larger than the dimensions required for packaging in TO-5 cans, their thin-film processes have advanced to the point that experimental active elements, diodes, and transistors have been fabricated using these techniques. It has been reported that silicon diodes and transistors with relatively large junction areas have been formed on the substrates without going through the familiar preliminary fabrication steps normally required in the semiconductor technology, such as crystal growing and diffusion. Thin-film silicon transistors made by Sylvania have displayed a current gain of thirty. On a substrate smaller than a dime, 49 diodes have been formed.

GENERAL ELECTRIC COMPANY. General Electric has been doing a considerable amount of research work in this field and has recently reported very encouraging results.[5] One type of device is the space-charge-limited (SCL) triode, in which a field is established between two electrodes in such a way that space-charge neutrality does not hold. This device has high gain-bandwidth, low noise, and is relatively

insensitive to temperature. It is a voltage-controlled device with an input resistance of 1 megohm. The frequency limit is in the range of 10^8 to 10^9 cps. Its main limitation is that the grid structure, consisting of isolated fineline grid with 1 μ spacings, is very difficult to fabricate.

A second device investigated at General Electric is the "Hot Electron Triode," which consists of consecutive layers of emitter metal, emitter insulator, grid metal, collector insulator, and collector metal. Either the emitter and its insulator or the collector and its insulator, or both, can be replaced by semiconductor and ohmic contacts. This is a current-controlled device with an input resistance of 1 to 100 ohms. Its frequency limit is 10^6 to 10^7 cps, and the device is radiation resistant. Its principal limitation is noise, temperature dependence, and low operating frequencies.

The final device under development at General Electric is the "Field Effect Triode," which is presently operational. It basically consists of electrodes on semiconductor film surfaces of micron thickness. It is a voltage-controlled device with input resistance of 1 megohm and frequency limit of about 10^8 cps. It has a high gain-bandwidth and can be fabricated relatively easily. Because of critically small spacings, problems of reproducibility are rather severe.

11.4 THE CASE FOR THIN FILMS

At this point it is worthwhile to pause and consider some of the arguments in favor of the thin films and the hybrid approach to integration as put forth by their proponents. Since the active devices used in the hybrid approach are separately manufactured semiconductor chips, it is quite apparent that the circuit designer's burden is considerably lightened as far as diodes and transistors are concerned. It helps materially in the fabrication process because the active elements can be individually tested and selected. Thus it would raise the yield significantly. The overall circuit performance can therefore be greatly enhanced by selecting the active components for the desired top performance.

The capability to select the active elements has another potential advantage. The possibility of duplicating an existing conventional component circuit into the hybrid integrated form is now more readily realizable. Vendors claim that circuit performance is further improved by improved tolerances and stability of passive elements. Hybrid circuits offer the flexibility of design changes, which is a very desirable feature. Besides, they are potentially repairable, at least to the extent of replacing the active elements. Because of the reduced

dependence on semiconductor technology, the hybrid circuits offer potentially more supply sources. Vendors in this field claim low costs and therefore lower prices. If discrete thin-film component costs, such as deposited resistors, are any indication of the price trends, this claim could certainly be justifiable.

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section 5

Miscellaneous related topics

Integrated circuit packages and mechanical considerations

12

12.1 INTRODUCTORY REMARKS

Intensive research and developmental efforts have recently fructified in several significant advances in integrated circuits. However, the problems of packaging these units have not received much attention as of now and appear to be a particularly weak area. Since the field of integrated circuitry is relatively new, it is quite understandable that the vendors would concentrate their initial efforts on the development of techniques and processes primarily connected with the circuits and consider packaging as a secondarily associated area. Consequently, the TO-5 package was a natural to fall back on as a suitable container during the early days of the integrated circuits, since it represented a path of least-resistance approach. Also, because of the lack of standardization, both among the vendors and the users, the TO-5 offered some attractive features. In the first place, it is a well-proven and time-tested design. Second, it is a container that is readily available from several sources at a relatively low cost. Finally, by using the TO-5 can the vendors have been able to get around the problem of tying up their financial resources in the development of this phase and to release them for the more pressing needs of process developments.

Although the TO-5 can provided a very convenient initial package, it has some serious drawbacks. First, a close look at the size of the integrated silicon chip and the volume within a TO-5 can immediately reveals that too much space is wasted within the can and that the full size potential of integrated circuits is not utilized. Second, the axially protruding leads of the TO-5 can necessitate mounting the unit on some form of printed circuit board. Such an approach reduces the packaging densities of a system or a subsystem. A third disadvantage arises because of the round shape of the can. Because of this, a lot of space between adjacent units on the same mounting board is wasted. Last, because the leads are arranged in a circular fashion around the periphery of the header, interconnection patterns on the board become rather complicated. In spite of these shortcomings, the TO-5 can is still very extensively used and probably will continue to be used for some time in the future.

12.2 BRIEF DESCRIPTION OF THE TO-5 CAN

Mechanical Description of the Jedec TO-5 Package

The TO-5 can used for integrated circuits is the same basic package used for transistors with some modifications to suit the individual vendor's requirements. The most common variations involve the number of leads, the lead dimensions, and the lead circle diameter. For purposes of simplicity, the dimensions of the standard Jedec TO-5 transistor package are shown in Fig. 12.1. All dimensions are in inches and the package weighs approximately 0.05 oz.[1]

Encapsulation

Encapsulation is the term commonly used to include the steps involved between completion of the semiconductor wafer processes,

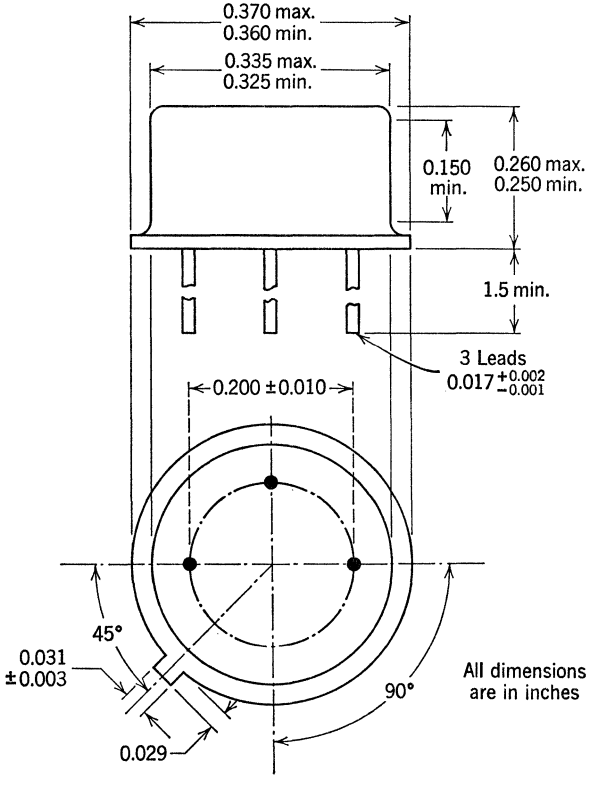


Fig. 12.1 The Jedec TO-5 transistor can.

either the transistor or the integrated circuit, and the final sealing of the unit. Since the semiconductor is likely to be subjected to mechanical damage in handling or to contamination by harmful impurities during operation, encapsulation is necessary to provide protection and insure reliability. Encapsulation plays an important part in establishing the electrical stability and the thermal ratings of the final device. In silicon-planar passivated devices, the semiconductor is usually mounted directly on the header to assure good mechanical and thermal characteristics. To obtain good hermetic sealing, a kovar metal header is usually used, and leads are thermocompression bonded for high reliability.

THE PROBLEM OF CONTAMINATION. During the encapsulation process it is necessary to insure that contaminating agents are evacuated from the package before it is sealed. Surface metals and other impurities that may have accumulated on the semiconductor wafer during manufacturing are first chemically removed and the wafer is subjected to a controlled atmosphere to prevent any further contamination. The unit is then raised to an elevated temperature to reduce, or eliminate if possible, the moisture content. The unit is then filled with a controlled atmosphere and the cap is welded on to the header.

THERMAL CONSIDERATIONS. It is important that the header lead seals be able to withstand the thermal shock of soldering. Kovar lead seals are usually used because they stand the thermal shock of soldering very well, and are still effective after thermal cycling. It is also necessary that the internal contacts not be affected by thermal cycling. Consequently, coefficients of expansion within the unit are matched to prevent strains during thermal cycling. The design of the case and the header also governs the thermal impedance of the semiconductor wafer. Smaller cases reduce the junction-to-case impedance but increase the can-to-air impedance.

HERMETIC SEALING FOR ELECTRICAL STABILITY. The stability of the electrical characteristics of the silicon devices is largely determined by their exposure to moisture. If moisture is present during the period when a transistor is warming up, after it has been subjected to low temperatures, the leakage current, I_{CO}, increases to a large value. This is a reversible change but nevertheless can be a rather troublesome problem. Good hermetic sealing can keep the external moisture from reaching the semiconductor and also keep the controlled atmosphere sealed within the can. Kovar-glass lead seals are used in transistors and integrated circuits encapsulated in TO-5 cans intended for high reliability operation.

12.3 THERMOCOMPRESSION BONDING

The Problem and Requirements of Lead Bonding

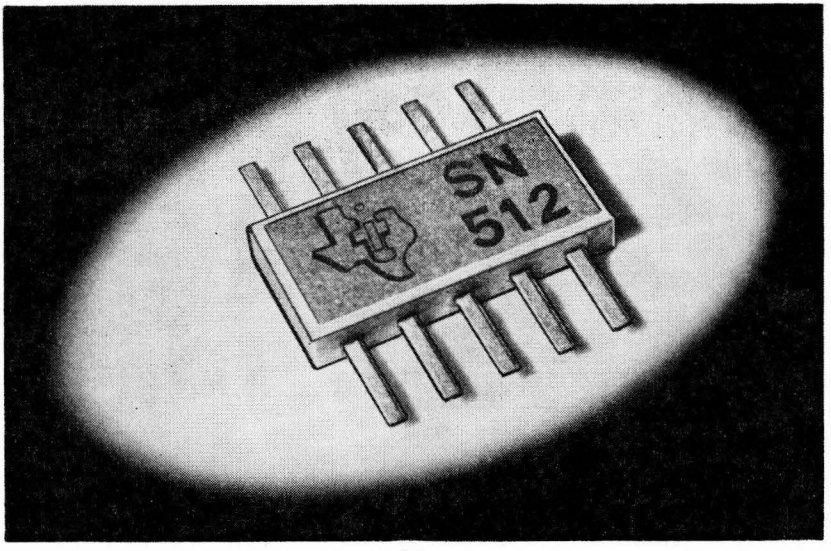
Because of their diminutive size, the areas available on an integrated circuit wafer for bonding leads, which are brought to the outside world, are extremely small and present several problems. Metal leads can be joined to metalized semiconductor surfaces by welding, soldering, or thermocompression bonding. The last-named method is a direct bonding process which means that "two primary bodies (such as an electrode and a semiconductor) are made to seize without a third intermediate phase (such as solder) and without melting."[2]

In integrated circuits it is essential that the lead-to-wafer contacts be ohmic only and not rectifying, which obviously would cause circuit malfunctions. It is also necessary that the materials involved, that is, the lead itself and the metalized wafer, both retain their original physical properties. A further requirement is that neither of the bodies to be joined should melt and overflow during the process. Because of the small sizes involved, it is very desirable to avoid the introduction of a third agent, such as solder, during the joining operation. Since semiconductors, by their very nature, are susceptible to damage by heat, moderate temperatures for bonding are essential. Also, the lead bond must have mechanical strength, particularly if the units have to meet stringent military environmental requirements for aerospace applications. Thermocompression bonding satisfactorily meets these requirements and so this process is used in present-day integrated circuits.

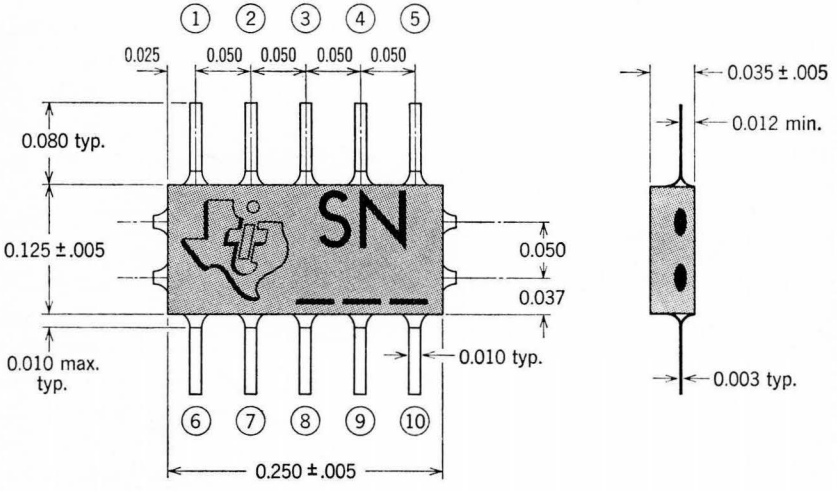
Direct Bonding Process and Its Properties

Direct bonding of metal leads to semiconductor or metalized semiconductor surfaces, requires moderate heat and moderate mechanical pressure. Surfaces of solids have tiny projections, called asperities, which deform and seize when they come in direct contact with other asperities on another surface. The degree of adhesion between the two surfaces depends on the deformation and change of the asperities under pressure. In the bonding process, the function of heat is to keep the metal soft or in the annealing range as it is brought in close contact with the semiconductor.

Experimental data indicates[2] that materials with higher coefficients of friction (both kinetic and static) have a higher coefficient of adhesion, and that for crystals, adhesion decreases as hardness increases. One significant advantage of thermocompression bonding is that it does not involve melting and does not contaminate the semiconductor.



(*a*)



Outline dimensions hermetically sealed solid circuit semiconductor network

(*b*)

Fig. 12.2 The Texas Instruments flat rectangular package. (*a*) The package. (*b*) The dimensions.

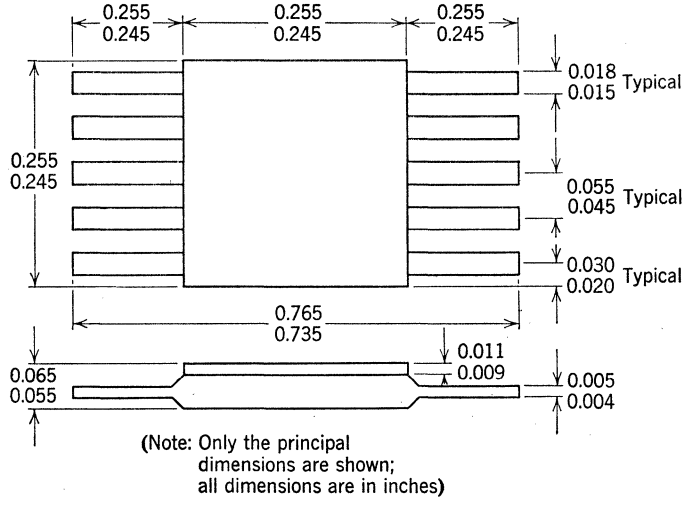


Fig. 12.3 The Signetics flat square package.

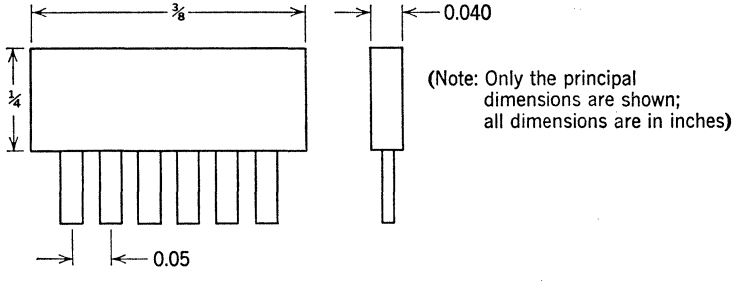


Fig. 12.4 The Westinghouse 6-lead flat rectangular package.

From the cost point of view, it is a direct and simple process which does not require special environments, and therefore can be done in open atmosphere.

12.4 THE FLAT RECTANGULAR PACKAGE

Advantages of the Flat Package

The shortcomings of the TO-5 package as a container for integrated circuits were mentioned before. Some of the vendors are packaging their off-the-shelf circuits in cases of flat rectangular geometries. Unfortunately no industry standard on integrated circuit packages

exists at this time and so the dimensions of these packages, as well as lead configurations vary with each vendor. As compared to the TO-5 case, they have certain advantages which are common to all. Since they are flat, the space within the package is better utilized than in the TO-5 case, with wastage reduced to a minimum. In each instance the leads are protruding laterally, either on one side or more. This makes for better and easier subsystem packaging and minimizing wasted space between the adjacent units, which is quite considerable in the case of the round TO-5 cans. Better schemes for heat dissipation are possible.

Commercially Available Flat Rectangular Packages

THE TEXAS INSTRUMENTS PACKAGE. Texas Instruments packages all their standard product-line circuits in a flat geometry unit (Fig. 12.2). The package is 250 × 125 × 35 mils. It weighs 0.05 gram and occupies a volume of 0.001 in.[4] A hermetic seal is created by a kovar-glass seal around the leads and a metal-to-metal bond of the package. Ten flat leads are available laterally, five on each 250-mil side of the unit. The leads which are spaced on 50 mil centers, are gold-plated, nickel-flashed kovar and are 80 × 10 × 3 mils. External connections to the leads can be made by soldering, welding, or thermocompression bonding. After final enclosure, Texas Instruments tests each package for leaks with helium tests.

THE SIGNETICS PACKAGE. Signetics packages some of their current standard product-line circuits in a flat package (Fig. 12.3). The unit is a kovar glass package which is 250 × 250 × 70 mils. There are 10 lateral leads, 5 on each side, and their dimensions are 250 × 16 × 4.5 mils. The package is hermetically sealed and designed to meet the environmental requirements of MIL-S-19500.

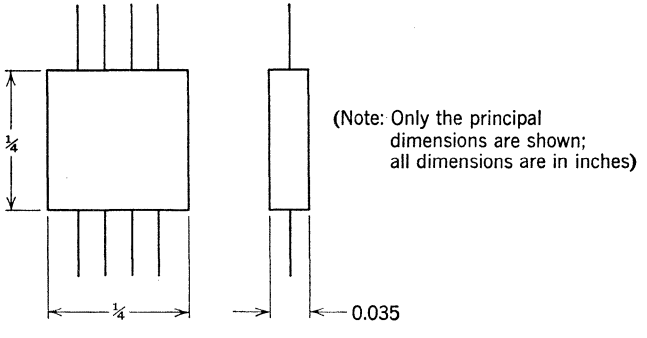


Fig. 12.5 The Westinghouse 8-lead flat square package.

THE WESTINGHOUSE FLAT PACKAGES. *The 6-Lead Flat Rectangular Package.* Westinghouse packages the WM-1108 Audio Amplifier in a flat rectangular package with all 6 leads protruding from one side. Figure 12.4 shows the principal dimensions of this unit. The top and the bottom of the unit are kovar with a matched glass-to-metal seal

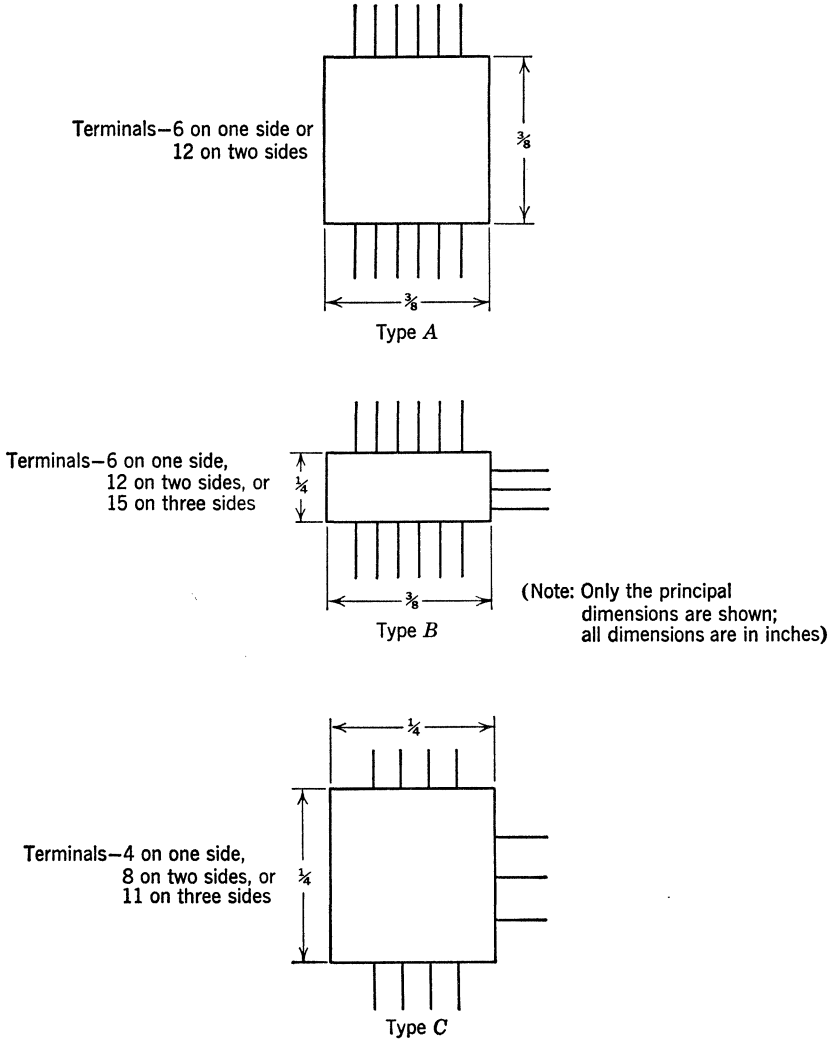


Fig. 12.6 Westinghouse family of flat packages.

insulating the leads from one another and the case. The flexible flat ribbon leads are gold-plated.

The 8-Lead Flat-Square Packages. Figure 12.5 shows the 8-lead flat square package which Westinghouse uses. Basically, the construction techniques of this unit are the same as those just described for the 6-lead flat rectangular package.

Packages of Other Geometries. Recently Westinghouse announced three types of flat rectangular packages of different dimensions with a wide choice of lead arrangements. Figure 12.6 shows the three types. All units have a ceramic or kovar base with a kovar lid. Flat kovar leads are $\frac{7}{32}$ in. long with cross-sectional dimensions of 15 × 5 mils and are spaced on 50 mil centers. All three package types are 35 mils thick.

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Testing, reliability, and maintainability

13

13.1 TESTING

The Necessity of Functional Testing

In conventional electronic circuits, the circuit engineers have always been able to test parameters of the components, both active and passive, thereby insuring conformance to their requirements. Integrated circuits deprive them of this traditional privilege. Because of their inherent characteristics, integrated circuits must be treated as black boxes. Consequently, the "transfer function" approach to testing is inevitable; in other words, the output must be some acceptable function of the input. There are three basic reasons for this.

First, the entire circuit, or part of a circuit if it happens to be a complex one, is contained in one package which is, of course, hermetically sealed. Opening the package for any reason whatsoever would destroy the hermeticity of the package. The integrated circuit itself may be subjected to undesirable environments which may adversely affect its performance, perhaps permanently. Besides, the circuit element or elements are liable to be mechanically damaged because of handling. The lead wires connecting the silicon chips to the external terminals are most susceptible to damage. At the present time, the costs of the integrated units are such that it is hardly economical to resort to destructive testing.

Second, if some units must be opened, either for inspection or testing, special equipment, such as microscopes, micromanipulators, and special test instruments are essential. Besides, an adequate supply of specially trained personnel is also necessary. All of these are expensive items.

Third, assuming that the necessary equipment and personnel are available for opening the units, testing them might still be a rough job, and in some cases might be virtually impossible. For instance, assume that a resistor in the collector of a transistor has to be tested. It is quite possible that this resistor may be fabricated such that it is an integral part of the domain diffused for the collector. Obviously, it would not be feasible to conduct any tests on this resistor individually. Within limits it is possible to provide test points at appropriate nodes

in a circuit for testing purposes such that they are made available externally. This procedure, while being desirable, is naturally limited by the number of pins available in the package in question.

The kind of tests to be performed and the test equipment required, of course, depend on the circuits concerned. A very interesting paper[1] describes the program at Fairchild Semiconductor for the testing of their Micrologic elements and an automatic test system.

Testing of Digital Logic Units

Unfortunately, at the present time, tests for integrated logic circuits are not standardized, although it is quite possible that functional tests may be standardized by the industry in the not-too-distant future. Some of the commonly tested parameters of logic circuits are as follows:

1. Determination of ON and OFF output levels at different fan-outs.
2. Switching speeds at different fan-outs with different fan-ins.
3. Determination of noise susceptibility of the circuit with the circuit parameters at their worst-case conditions.
4. Determination of signal propagation delays through the circuit at minimum and maximum fan-outs over the operating temperature range.

Testing of Linear Circuits

The tests for linear circuits are entirely dependent on the circuits concerned and their specifications. Some of the tests commonly made on linear circuits used in computing systems are:

1. Determination of signal propagation delays.
2. Determination of responses at specified inputs and loads for driving circuits.
3. In such circuits as sense amplifiers, determination of their frequency response characteristics, their differential gain, the common-mode gain, the common-mode rejection ratio, and recovery times from common-mode and the unwanted differential signals.

13.2 RELIABILITY

Inherent Reliability in Integrated Circuits

From the equipment manufacturer's point of view, reliability is one of the most attractive features of integrated circuits. Undoubtedly, in commercial and ground-based military equipment, reliability plays a very important role, but for aerospace applications its importance can hardly be overestimated. Since the field is relatively new, the amount of reliability data currently available, in terms of actual life

tests, are rather limited. However, the data available from both the vendors and equipment manufacturers are very encouraging and give ample reasons for optimistic predictions.

Because of the processes and the technology involved in their fabrication, we can, perhaps, safely state that reliability is an inherent feature of integrated circuits which, for all practical purposes, becomes a controllable feature—to some degree, of course. Several facts stand out from the experience accumulated so far in manufacturing integrated circuits. In the first place, the processes involved are well understood since they are essentially the same as those used for the silicon-planar epitaxial transistors. Second, manufacturing technology has advanced to the point where these processes are controllable to a relatively fine degree. Third, as a result of the first two factors, these processes are reproducible. This makes integrated circuits suitable for mass production with attendant reductions in cost. Fourth, the largest single factor contributing toward increased reliability is the fact that bonds and component connections can be reduced (quite drastically in some cases) in integrated circuits as compared to circuits wired with conventional discrete elements.

Reliability as Indicated by Some Vendors

FAIRCHILD SEMICONDUCTOR. In a recently published report,[2] Fairchild indicates reliability data for their Micrologic line, which is tabulated in Table 13.1.

TEXAS INSTRUMENTS, INCORPORATED. Texas Instruments conducted an extensive testing program on their Series 51 line, and the results of the first quarter of 1962 have been reported.[3] These data are based

TABLE 13.1

RELIABILITY DATA INDICATED BY FAIRCHILD FOR THEIR MICROLOGIC LINE

Test	Circuit	Sample Size	Failure Rate (% per 1000 hr)
150°C storage life	Buffer	24	0.042
	Counter	38	0.026
	Flip-flop	115	0.009
	Gate	218	0.005
Operating life at +125°C	Flip-flop	479	0.00057
	Gate	272	0.00049
	Gate	1200	0.00019

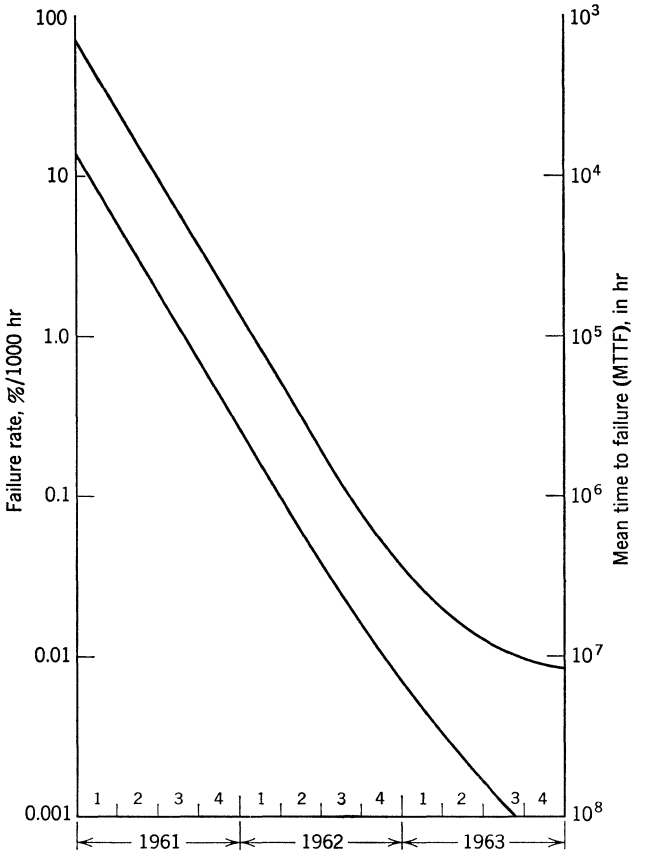

Fig. 13.1 Texas Instruments' reliability trend and prediction curves, 1961–1963.

on an integrated circuit that essentially performs the same electrical function as approximately twenty equivalent discrete components connected in a circuit in the conventional manner. The units tested to destruction by step-stress tests show ball bonding as the major cause of failure. Texas Instruments indicates accumulated network failure rates of 1.8%/1000 hr at 125°C and 5.0%/1000 hr at 200°C. Figure 13.1 shows the reliability trend established by Texas Instruments' integrated circuits over 1961 and 1962 and the reliability prediction for 1963.

UNIVAC'S Reliability Experience

The reliability experience on integrated circuits within UNIVAC (at St. Paul) can best be exemplified by the Microelectronic Arithmetic Unit, which was completed and put into operation in December 1961. This test model has approximately 200 Fairchild Micrologic units, mostly gates and half-shift elements, which have, at the time of this writing, accumulated a total operating time of about 3000 hours without a single failure. In addition, several tests have been performed (or are currently in process) for integrated units which give ample indications for optimism.

Reliability Predictions

Based on the information given in the reliability report by Texas Instruments,[3] some reasonable projections can be made for reliability of the Texas Instruments, Incorporated units for the near future. While these figures are derived from tests on Texas Instruments, Incorporated units only, one could reasonably apply them to integrated circuits in general for the sake of an overall picture.

Following the trend indicated for 1961 and 1962, a maximum failure rate of 0.008%/1000 hr and a minimum failure rate of 0.6%/1000 hr can be expected for the first quarter of 1963. For the second quarter of 1963, the expected failure rates are a maximum of 0.005%/1000 hr and a minimum of 0.3%/1000 hr.

We can say with a reasonable degree of assurance that the reliability of fully integrated circuits can be expected to be the same as that of silicon-planar epitaxial transistors. A possible objection to this statement might be that the transistor in question has only three bonded connections, whereas the integrated circuit may have eight or ten such bonded connections, and therefore the reliability comparison may not be very realistic. This is true. But, it should also be pointed out that the fully integrated circuit is no longer a circuit in the conventional sense of the term. Instead, it is now a component which can directly replace a circuit consisting of maybe twenty or more discrete components along with all their point connections.

13.3 MAINTAINABILITY

It is quite obvious that the integrated circuit by its very nature is not suitable for repair by replacement of circuit elements, because in the first place the silicon chip itself is not readily accessible without destroying the hermeticity of the package. Second, the circuit elements form an integral part of the substrate and as such are not detachable. This means that on malfunction, the entire integrated

circuit unit must be replaced by a known good one. In other words, the throw-away philosophy of maintenance is inevitable.

At first sight, the maintenance of a system using integrated circuits may appear to be a pretty expensive proposition because of the throw-away procedure. Actually, this cost can be considerably reduced by suitable packaging schemes. If several integrated circuits are put in one module, the entire module would have to be discarded because of the malfunction of a single unit, and the cost would then be excessively high. On the other hand, the system packaging can be designed such that each integrated unit can be individually tested in the system and replaced if necessary. While this may sound not too practical, it is quite feasible. This is exactly what the UNIVAC 1816 Aerospace Computer proved to be very practical.

However, the inherent reliability of integrated circuits is such that the maintenance problems should be significantly reduced.

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Recent advances and projections

14

Integrated circuitry is a young field. While very substantial progress has been made in 1961–1963, we can expect the field to grow and expand into hitherto unexplored areas. Several problem areas still remain but, with the added interest and the research and development effort going on at a continually accelerated pace, optimism is justifiable. Keeping up with the latest developments in this dynamic field is a Herculean task. A book like this would hardly be terminated if one attempted to include all the new developments and innovations. The purpose of this chapter is twofold. The first objective is to state briefly some of the recent advances which appear most significant from the futuristic point of view. Second, the prices of integrated circuits are a topic of much discussion and conjecture.

14.1 PURPLE PLAGUE

The Problem

One of the most irritating problems facing the planar transistor, and hence the integrated circuit, too, is mechanical in nature and is commonly referred to as "purple plague." The planar process is described in Chapter 3 and will not be repeated here.

In the usual planar device, the exposed silicon surface is first metalized with a thin film of deposited aluminum and then the gold wire is bonded to the aluminum layer by the previously described thermocompression bonding process. At the bond point of the gold connecting wire and the aluminum contact land, a gold-aluminum intermetallic compound, $AuAl_2$, is formed. In its advanced stages of formation, this compound is very brittle, resulting in a mechanically weak bond which is susceptible to catastrophic failure. Increase in temperature apparently accelerates the formation process. The $AuAl_2$ compound is purple in color, and hence the descriptive term "purple plague" is applied to it.

A natural question that comes up is, "Why use aluminum for the metalization and why gold for the whisker wire?" It is necessary that the metalization material be capable of being deposited on both silicon and silicon dioxide by vapor-deposition techniques, and at the same time be acceptable for bonding with the whisker lead. Aluminum

meets these requirements satisfactorily. Perhaps the next question would be, "Why not use aluminum whisker leads?" This would certainly solve the purple-plague problem at the silicon chip, but would create another problem: the other end of the whisker lead would have to be bonded to the external stem lead of the package, which would be gold plated, thus shifting the problem from purple plague on the silicon chip to purple plague on the stem leads. One might ask, "How about using aluminum stem leads?" Soldering aluminum to aluminum presents some difficulties too and so it appears that some other solution would have to be found, while still using gold whisker leads.

A Possible Solution

Recently, Philco came up with a promising solution to this problem. The metalized aluminum is no longer used. Instead, a two-layer deposition is used. The first deposited layer is chromium and the second layer, deposited on top of the chromium, is silver (Fig. 14.1). Chromium adheres strongly to both silicon and silicon dioxide, and makes a good nonrectifying ohmic contact with silicon. The gold wire is now bonded to the low-resistance silicon layer which does not form the intermetallic brittle compound, as in the case of the aluminum-gold bond.

Several units tested at Philco show very encouraging results.[1] Five

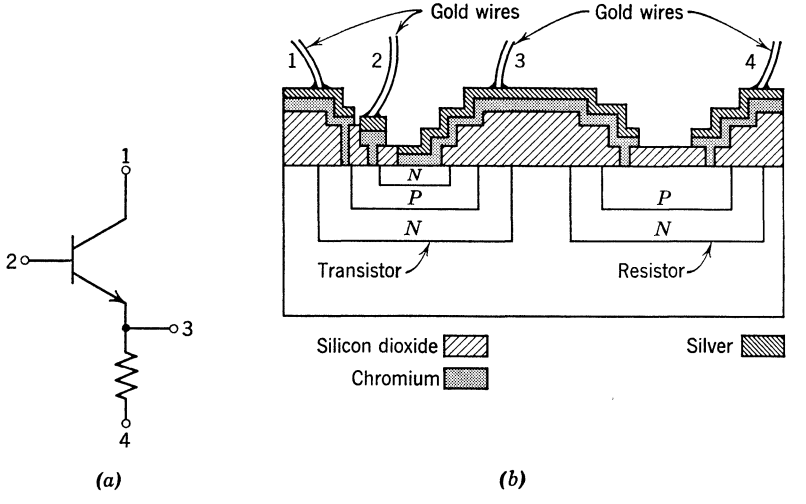

Fig. 14.1 Philco's two-layer deposited interconnection scheme. (*a*) The circuit. (*b*) Two-layer chromium silver deposition.

hundred transistors, fabricated with this technique and tested for a total of 1,129,968 hr, resulted in degradation failures of only 4 units. The observed failure rate was 0.35%/1000 hr, and there were no catastrophic failures showing physical deterioration of the bonds.

14.2 DEPOSITION OF PASSIVE COMPONENTS ON SILICON SUBSTRATES

Another promising advancement is the marriage of solid-state and thin-film technologies resulting in the deposition of passive components on the silicon-dioxide surface of passivated silicon chips. Philco recently announced[2] successful combination of tantalum thin-film, passive-element fabrication with integrated planar fabrication of active elements. Figure 14.2 shows the scheme used by Philco.

Resistors and capacitors fabricated by depositing tantalum thin films are claimed to provide improved drift characteristics, freedom from parasitics, and component tolerances not usually possible with the conventional silicon-integrated techniques. The value ranges of the passive components are greatly increased as compared to those presently obtained with diffused passive elements. According to Philco, silicon (or silicon dioxide) provides an excellent substrate for deposition of tantalum films. This technique appears to be very promising for circuits requiring close tolerances, particularly linear-type circuits.

14.3 THIN-FILM ACTIVE DEVICES

A considerable amount of research and development work has been going on in the area of deposited active devices. Such devices, when

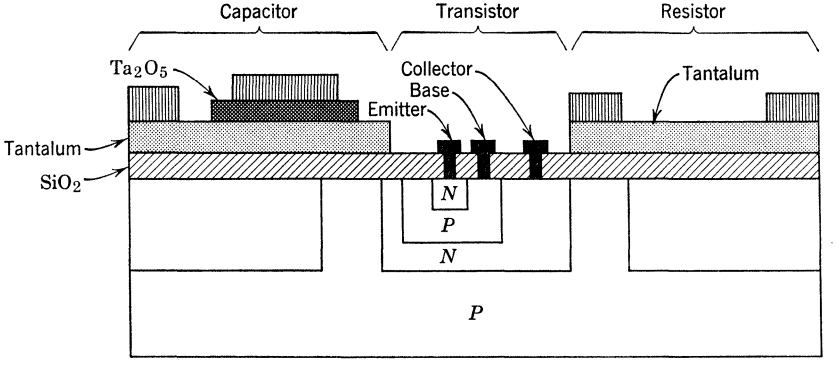

Fig. 14.2 Philco's thin-film deposition of passive components on silicon substrate.

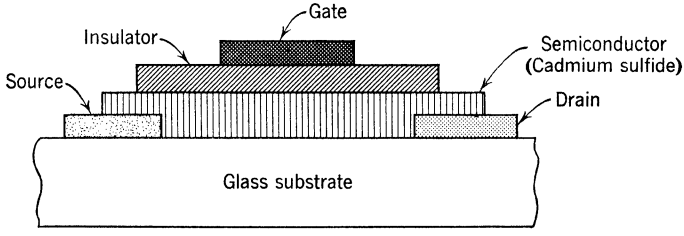

Fig. 14.3 RCA's insulated-gate TFT.

fully developed and capable of production in quantities, could conceivably antiquate the hybrid thin-film semiconductor integrated circuit presently used. The work done in this area by Sylvania and General Electric is mentioned in Chapter 11. More recently, the achievements of other similar approaches have been reported and are briefly outlined in this section.

Insulated-Gate, Thin-Film Transistors

The work done at RCA has resulted in an insulated-gate, thin-film transistor, popularly referred to as the TFT. The TFT (Fig. 14.3) is a field-effect device. Its control gate is separated from the semiconductor by an insulating film, instead of a back-biased *N-P* junction. The gate can be biased either negatively or positively without drawing appreciable gate current.[3]

On an insulating glass substrate, two gold electrodes, separated by a 10 μ gap, are deposited. These are the source and the drain electrodes. The semiconductor is an *N*-type polycrystalline film of cadmium sulfide, which is less than $\frac{1}{2}$ μ thick. An insulating layer of silicon oxide or calcium fluoride, less than $\frac{1}{10}$ μ thick, is deposited on the semiconductor layer. A gold or aluminum strip, 15 μ wide, is deposited on the insulating layer and forms the gate of the device.

The TFT can be operated in two distinct operational modes. In the enhancement mode the gate is positive, and the current between the source and the drain can be enhanced by several orders of magnitude. In this mode, gain-bandwidth products of 12×10^6 cycles/sec and transconductances above 10,000 have been achieved.[4] Because of the positive gate bias, direct coupling between successive stages is possible. With a negative bias on the gate, the TFT can be operated in the depletion mode. In this mode of operation, a useful saturated drain current is obtained with zero bias on the gate. Experimental-type TFT units show that the output resistance is inversely proportional to gate voltage at low-drain voltage, that is, below saturation. At

high-drain voltage, that is, in the saturation region, the square root of the drain current increases linearly with gate voltage, and the transconductance is proportional to the square root of the drain current. As a switching device, the TFT shows some very promising possibilities, since it consumes negligible power in the OFF state and moderate power, about 1 mw, in the ON state.

Metal Interface Amplifier

The research division of Philco has devised a novel means of obtaining amplification. The device, called the Metal Interface Amplifier, or MIA, consists of a thin-film sandwich of metal oxide and metal deposited on a germanium substrate. By applying voltages across the two metal films, electrons are transferred through the intermediate oxide layer by the quantum-mechanical tunneling process.[5] The two metal layers and the substrate act as the injector, the controlling element, and the collector, respectively, corresponding to the emitter, base, and collector of the conventional transistor. The MIA is a "majority carrier" device. At the present time not much information is available on this device.

Junction-Type Deposited Active Devices

A unique deposited junction device was discussed by Rasmanis at the 1962 NEREM Conference.[6] Using a newly developed technique called rheotaxial growth (rheos for fluid and taxis for arrangement) conventional *P-N* junction devices are deposited on ceramic substrates. Figure 14.4 shows the cross-sectional view of the rheotaxial-epitaxial diode structure.

The rheotaxial oxide layer on the ceramic substrate makes it possible to deposit single-crystal silicon. The actual device structure is formed by epitaxial growth of doped silicon over the oxide surface. The oxides used for the rheotaxial layer are fluid at the temperature at

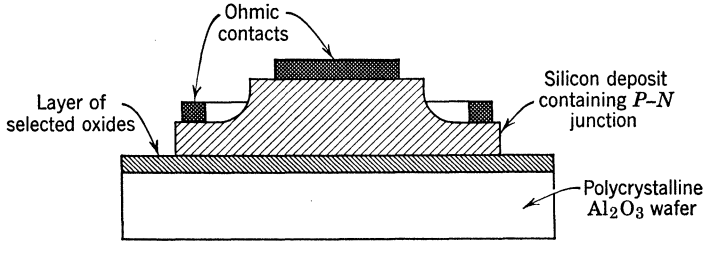

Fig. 14.4 Rheotaxial-epitaxial diode structure.

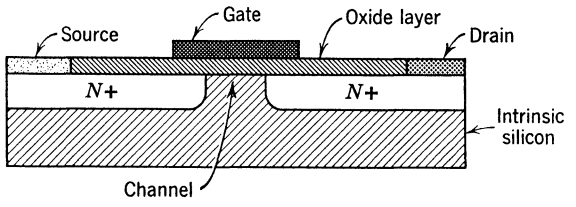

Fig. 14.5 The RCA insulated-gate field-effect transistor.

which the silicon film forms. The vapor is created by the decomposition of $SiCl_4$. The transistor geometry is similar to the diode shown in Fig. 14.4, with another concentric ring added for the base. Experimental transistors fabricated by this technique have displayed common-emitter current gains between 30 and 200 at V_{CE} of 5 volts, and I_B of 0.1 ma.[3]

14.4 INSULATED-GATE, NONJUNCTION, SEMICONDUCTOR, FIELD-EFFECT DEVICES

A significant step in device technology, announced by Radio Corporation of America, is an all-semiconductor, nonjunction, insulated-gate, field-effect transistor. This device is fabricated as metal-oxide-silicon transistor, referred to as MOS by RCA.[7] Unlike other field-effect devices, which are either semiconductor junction-types or insulated-gate, thin-film types, the MOS is neither the junction-type nor is it the conventional thin film variety. Figure 14.5 shows the cross-sectional view of this device, where two heavily doped $N+$ regions are diffused into the basic intrinsic silicon wafer. The silicon surface is then passivated by controlled oxidation process. By means of conventional masking techniques, areas above the two $N+$ regions are cut through the oxide layer. Gold electrodes are then deposited on the exposed silicon surfaces for the source and drain, and over the oxide layer for the gate. P-type devices could be made by a similar process.

The MOS is a "majority-carrier" device. In the N-type unit, the current between the source and the drain can be enhanced by several orders of magnitude when the gate is positive. It can also be operated in the depletion mode, and in this mode a significant drain current is obtained at zero gate bias. RCA reports that a typical enhancement-mode unit has an input resistance of 10^{15} ohms, input capacitance of 1 pf, g_m of 1000 μohms, cut-off bias of 6 volts, and rise time of 20 nanosec. For logic circuitry, a propagation delay of 20 nanosec per stage has been achieved. Both N and P type devices have been produced

and these can be combined in complementary circuitry. "Preliminary tests by RCA show a tenfold decrease in sensitivity to nuclear radiation for MOS units when compared to conventional transistors."[7] RCA mentions that the laboratory units are highly uniform and that yields exceed 90%. Also, "they expect this technique to lead to an order of magnitude price reduction over other integrated circuit techniques."[8]

14.5 PRICE PROJECTIONS

Factors Affecting Price

All the advantages of integrated circuits we have discussed would hardly insure a bright future for them unless they were cost-competitive with conventional components and various other approaches to microminiaturization. While cost may not be a dominant factor in some military applications, it is certainly very important for the manufacturer of commercial equipment, whether it be television receivers or large data-processing systems. Several factors enter into the cost of integrated circuits, and usually it is a complex interplay of all of them that determines the final selling price of the product. Detailed discussion of each of these factors is beyond the scope of this book, but the following three points are most significant in establishing the price and therefore will be briefly examined.

MASKS. Silicon is one of nature's most abundant materials on earth, and so it is not surprising that the cost of the basic materials involved in the fabrication of integrated circuits, is relatively low. At this time, perhaps the biggest cost item is the design and manufacture of masks. Since masks and tooling for the currently available "off-the-shelf" items are accomplished facts, it is naturally more economical for the equipment manufacturer to use these items, if they can do the job at hand. Thus, the masking and tooling costs are spread out over a number of potential users. If the standard items offered by the vendors do not satisfy a particular requirement, the next best alternative would be to try some of the vendor-suggested custom circuit approaches, such as the M1 matrix by General Electric and the Master Slice by Texas Instruments, in which cases only the interconnection deposition mask would be custom-made.

BATCH PROCESSES. One of the most attractive features of the integrated circuit lies in its suitability for mass production. It is an accepted fact that the yields from production lines are not what we would like them to be. Nonetheless, they have improved considerably, and further improvements are naturally expected in the reasonably near future. It should be realized that because of the low yields attainable, quantity orders are likely to be the only real motivation

from the vendors' viewpoint, economically speaking. In other words, the user would do well to use standard product-line circuits, wherever possible, keep the number of special circuits down to a minimum, and use a larger number of units with a smaller number of circuit types.

INCREASED COMPETITION. Competition among vendors is getting keen, and we may reasonably expect it to become intensified as we go along. Basically, all the vendors who have the planar epitaxial capability can be potential contenders in this field. It is this writer's opinion that, sooner or later, all semiconductor manufacturers will get involved in integrated circuits to some degree.

Price Indications by Vendors

At the present time, no two vendors offer identical units as standard product lines, and so the prices of course vary over quite a range. It is interesting to see what the price trends have been in 1962–1963 and what we may expect them to be in the near future. The vendors them-

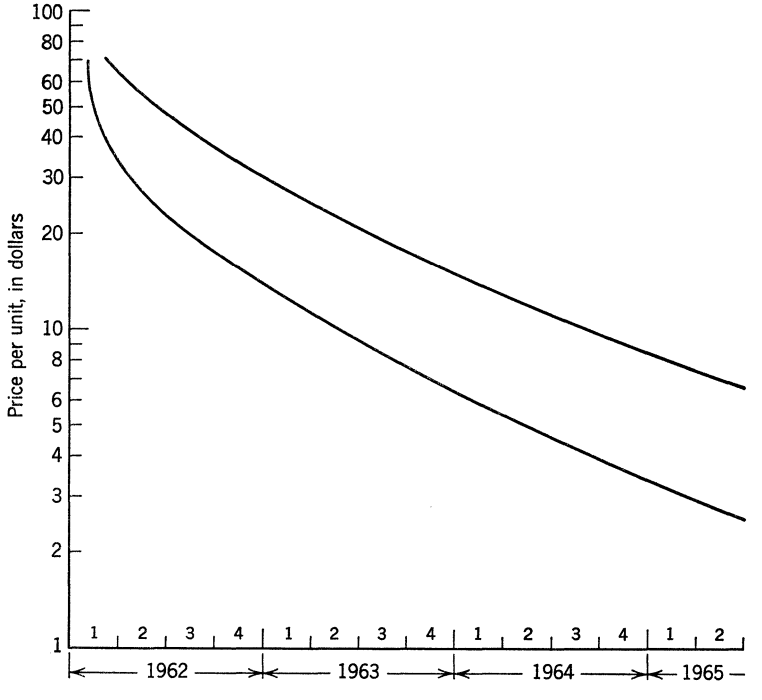

Fig. 14.6 Price trend curves as indicated by vendor with large production facilities.

selves are projecting prices, and their projections may sometimes reflect the particular vendor's relative degree of production capabilities.

Figure 14.6 shows price-trend curves as indicated by one vendor who has been in this field for some time and consequently has quite extensive production facilities. The curves refer to quantities in the tens of thousands and apply to units from the presently available standard product line in the TO-5 package. The curve is shown as a band to include the cheapest and the most expensive units in this typical vendor's standard line. These curves are typical indications of the trend projections by large-production capability vendors in the field.

Figure 14.7 shows price projection curves as indicated by a vendor who is a comparative newcomer to this field and does not have large production facilities, but who will undoubtedly have the capability in the near future. These curves are also applicable to their present standard-line products in quantities of tens of thousands, in TO-5

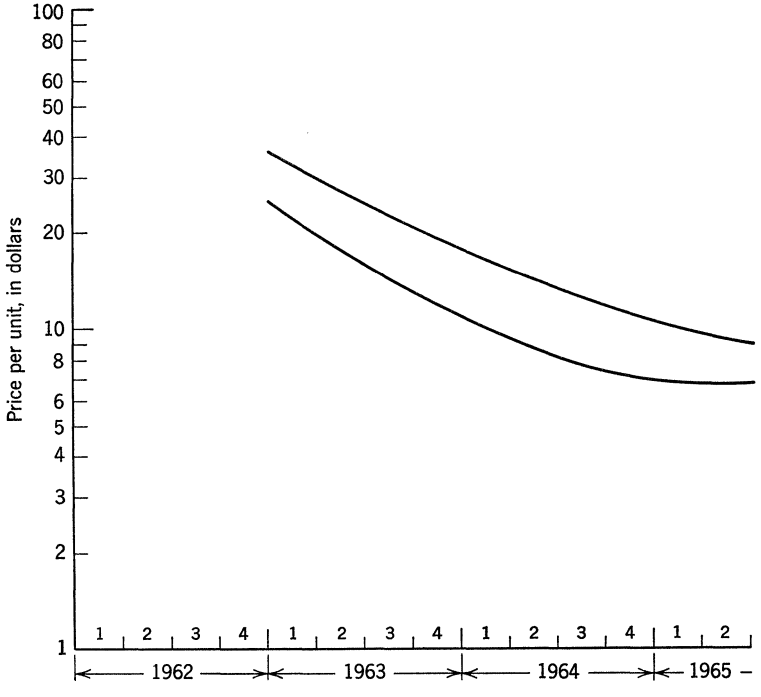

Fig. 14.7 Price trend curves as indicated by vendor with presently modest production facilities.

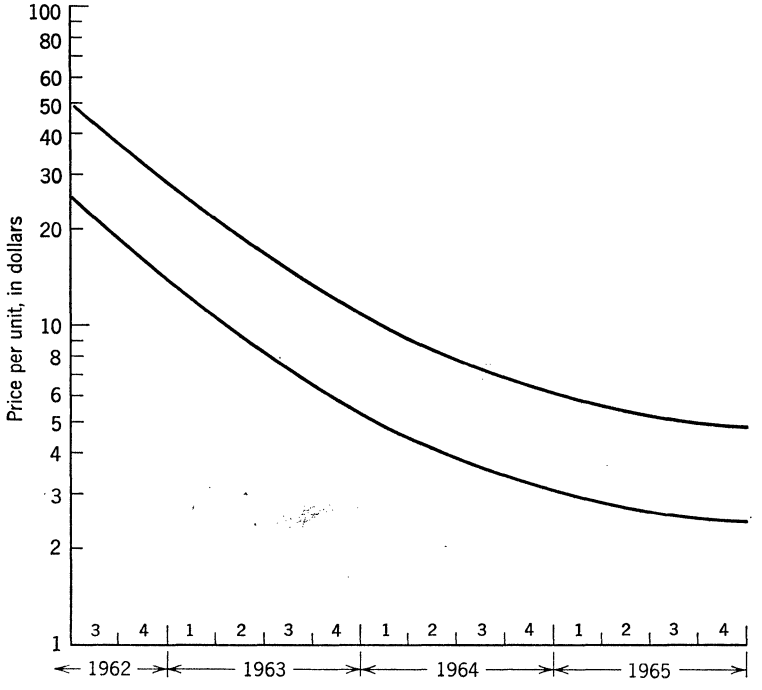

Fig. 14.8 The composite price projection curves.

packages, and are indicative of many vendors who have become actively engaged in this field quite recently.

While the two sets of curves just mentioned are interesting as relative comparisons, a set of curves incorporating the indications of both would perhaps be more meaningful from the point of view of the prospective user of integrated circuits. Two curves are shown, in Fig. 14.8, indicating the most optimistic and the most pessimistic limits based on logic circuit units in quantities of tens of thousands. In the composite curves, price variations are also reflected by several other factors, such as circuit specifications, circuit complexity, quantities involved, and the vendors concerned. These curves relate to vendors in general, and include those that have high production capabilities as well as those with modest facilities.

14.6 CONCLUDING REMARKS

Are integrated circuits the ultimate in the microminiaturization trend? One can hardly answer a question like this with a clear-cut

"yes" or "no." We can, however, safely say that this technology is probably the largest and the most significant step toward it. But, irrespective of whether it is the ultimate in microminiaturization or not, it certainly has a tremendous future, both in military and commercial applications. Apart from the various technical advantages, the possibilities of mass production with subsequent price reductions will undoubtedly bring the integrated circuit in the vast consumer market before too long—maybe radios, or television sets, or household computers handling such typical family problems as budgeting, bookkeeping of utilities bills, and, of course, the traditional annual American encounter with the income-tax returns. How soon will integrated circuits find their way into the consumer market? Estimates vary, but, the best educated guesses indicate 1965 as the most likely date.[9] Will integrated circuits replace all conventional circuits? Not very likely. It should be pointed out that attempting to integrate already existing circuits, which were designed for conventional components on a one-to-one component replacement basis, is bound to create serious problems. While time-tested and proven circuit design procedures certainly do apply to integrated circuits, we should keep in mind that there are peculiarities connected with this new field, some good and some undesirable, which must be taken into consideration when designing circuits, to get the maximum out of this new concept.

In the preface to this book reference was made to an engineering manager about integrated circuits. It is hoped that this book has been able to give him some insight into this fascinating field. Perhaps the best answer to his question, "Can we afford to go into integrated circuits?" would be another question, "Can we afford not to?" Many people in industry have wondered about the impact this new field will have on electronics in the future, and what will follow integrated circuits. Where science and progress will lead us is anybody's guess. We are on the brink of a new technological era in electronics and the end is certainly not in sight. I can imagine one of my sons, some years from now, picking up this book and wondering about the horse-and-buggy days when Dad used to dabble in the old phenomenon called "Microelectronics." After all, the real thing today is "Nanotronics," or perhaps it will be "Picotronics." Who knows?

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Appendix A
Fully integrated standard product-line circuits

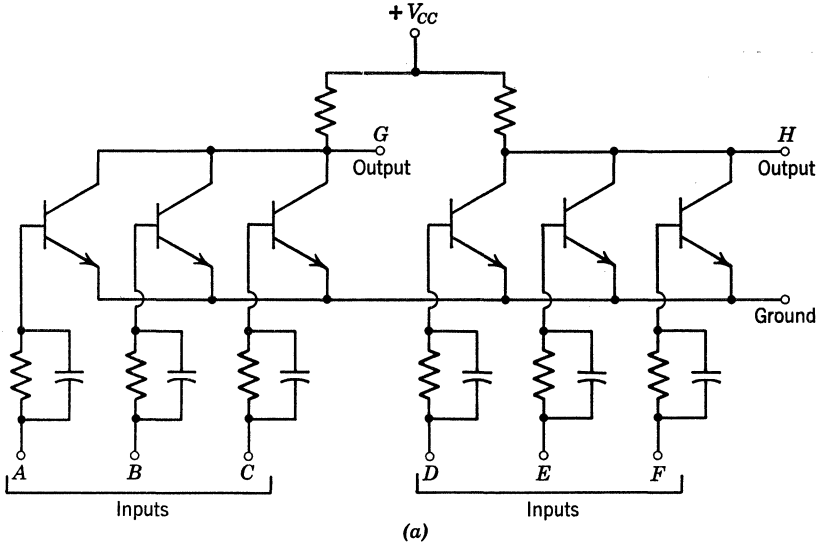
Since the integrated circuit is no longer a blue-sky dream but a practical reality, almost all the vendors in the semiconductor business are either involved in it or will be before too long. Neither the degree nor the depth of involvement is the same in any two vendors. Some vendors have been in it since its inception, but most are, relatively speaking, newcomers to this field. It is almost a certainty that no semiconductor manufacturer will be able to keep out of it for long.

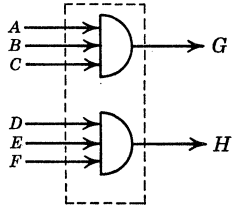
Basically, those vendors who have the planar and epitaxial techniques well in hand are, perhaps, in a favorable position to go into integrated circuits. It is only a matter of time before all vendors will have the necessary capability. The philosophy and the approach adopted by each vendor is somewhat different and fundamentally appear to be geared to their own techniques and facilities.

The purpose of this appendix is to present, in condensed form, the circuits that are offered by the vendors as standard product lines. Some of these circuits are offered by certain vendors as tangible evidence of their capabilities and not necessarily as their final standard products. These vendors indicate strong inclinations to react favorably to each customer's individual requirements. Others have taken a standard product-line approach and are offering these items in production quantities. Each vendor has selected a certain logic configuration for different reasons. Hardly any two vendors offer identical logic circuit configurations.

The information presented in this and the following two appendixes is condensed from the vendors' sales catalogs and brochures or from their advanced announcements on future products. Consequently, the figures on specifications and operational capabilities presented here are those released by the vendors themselves and were not obtained by testing or evaluation. While every attempt is made to include the most up-to-date information, some of it will, quite understandably, be out-dated by the time this book is published.

Although most pertinent points of each vendor's circuits are presented, detailed descriptions and data are beyond the scope of this book. Besides, this field is expanding so rapidly that newer products and a larger number of manufacturers will certainly be in the picture soon.





	NAND	NOR
G	$\overline{ABC}$	$\overline{A+B+C}$
H	$\overline{DEF}$	$\overline{D+E+F}$

Fig. A.1 SN514 two 3-input NOR/NAND. (*a*) The circuit diagram. (*b*) Logic symbol and truth table.

It will be observed that the logical symbols used in this book vary from one vendor to another. While it is desirable to use a uniform set of symbols, in the absence of universally accepted symbols, I have used those that the vendors have shown in their respective catalogs or brochures.

A.1 TEXAS INSTRUMENTS, INC., Dallas, Texas

In 1960, Texas Instruments announced the introduction of the earliest product line of integrated logic circuits. TI's trade name is "Solid Circuit" for this line. This family, called the series 51, utilized the Modified DCTL circuit (commonly referred to as RCTL) as their basic circuit type. Each base has a 20-kilohms resistor with a speed-up capacitor shunting it.

The Standard Series 51 Line

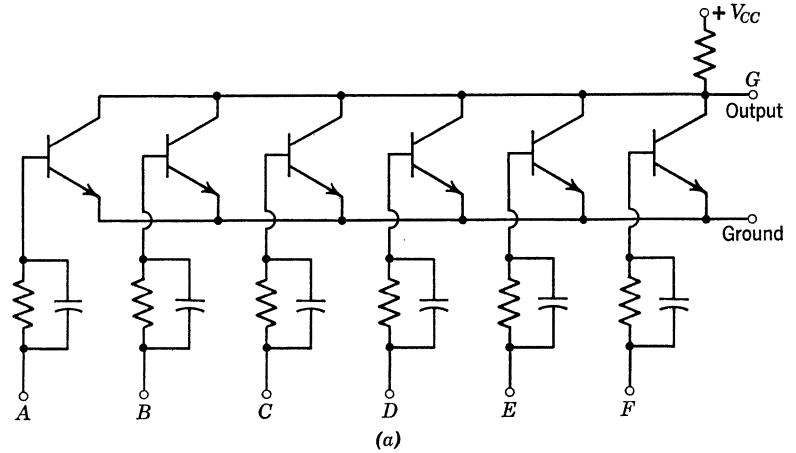
TI's Series 51 consists of a family of six digital circuits. Most of the following highlights of each of the circuits are taken from "Series 51 Application Report."

SN514, TWO NOR/NAND NETWORKS PER PACKAGE. The SN514 consists of two isolated NOR/NAND circuits, both sharing a common V_{CC} supply voltage. Figure A.1*a* shows the circuit, and A.1*b* shows the logical symbol and the truth table. TI indicates a maximum fan-out of 5 from each output terminal under all conditions. At the maximum fan-out, the typical power dissipation per stage is 2 mw for $V_{CC} = +3$ volts and 7 mw for $V_{CC} = +6$ volts.

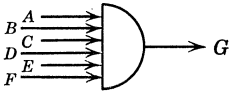
SN512, SIX-INPUT NOR/NAND, ONE PER PACKAGE. The SN512 is a six-input inverting gate with a maximum fan-out of 5. Its typical power dissipation for the maximum fan-out is the same as that of the SN512:

$$2 \text{ mw at } V_{CC} = +3 \text{ volts}$$
$$7 \text{ mw at } V_{CC} = +6 \text{ volts}$$

Figure A.2*a* shows the circuit and A.2*b* the logical symbol and the truth table.



(*a*)



	NAND	NOR
G	$\overline{ABCDEF}$	$\overline{A+B+C+D+E+F}$

(*b*)

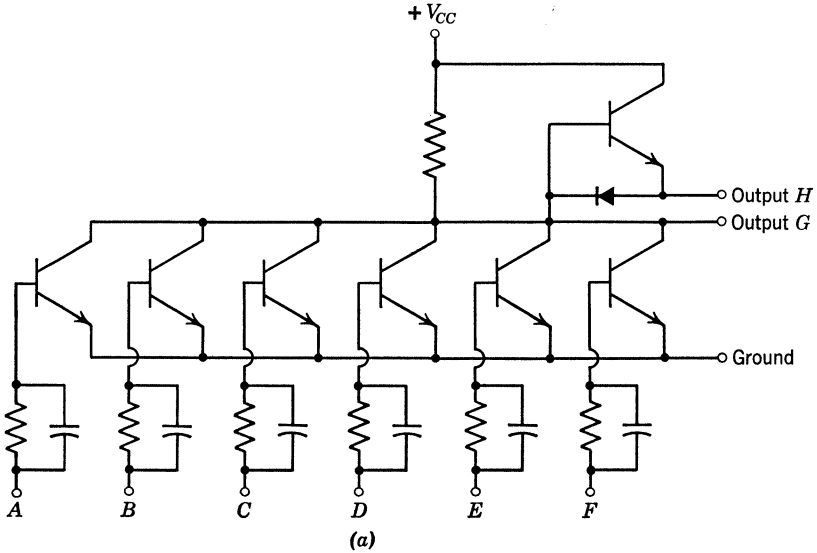
Fig. A.2 SN512 6-input NOR/NAND. (*a*) The circuit diagram. (*b*) Logic symbol and truth diagram.

SN513, SIX-INPUT NOR/NAND, ONE PER PACKAGE, WITH EMITTER-FOLLOWER OUTPUT. The SN513 is basically the same circuit as the SN512 but with a much larger fan-out capability. The output terminal G gives a fan-out of 5 but the emitter-follower output terminal gives a fan-out of 25. For fan-outs of 10, the typical power dissipations are as follows:

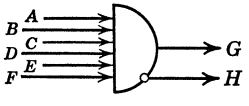
3 mw at $V_{CC} = +3$ volts
13 mw at $V_{CC} = +6$ volts

Figure A.3*a* shows the circuit diagram and A.3*b* shows the logic symbol and the truth table.

SN515 EXCLUSIVE OR NETWORK. The SN515 is an Exclusive OR circuit having two sets of complementary inputs. The fan-out capa-



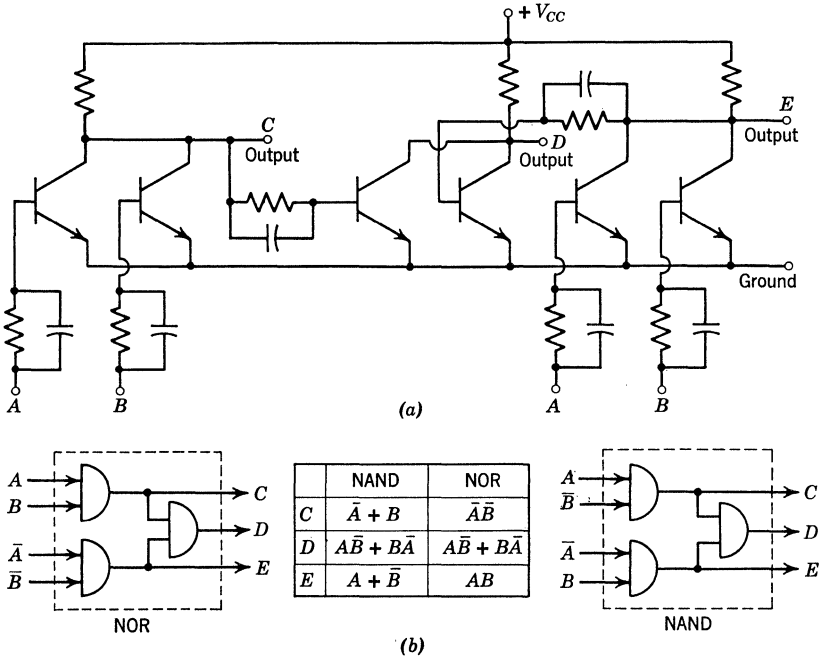
(a)



	NAND	NOR
G	$\overline{ABCDEF}$	$\overline{A+B+C+D+E+F}$
H	$\overline{ABCDEF}$	$\overline{A+B+C+D+E+F}$

(b)

Fig. A.3 SN513 NOR/NAND with emitter-follower output. (*a*) The circuit diagram. (*b*) Logic symbol and truth table.



	NAND	NOR
C	$\bar{A} + B$	$\bar{A}\bar{B}$
D	$A\bar{B} + B\bar{A}$	$A\bar{B} + B\bar{A}$
E	$A + \bar{B}$	AB

Fig. A.4 SN515 Exclusive-OR network. (*a*) The circuit diagram. (*b*) Logic symbol and truth table.

bilities are as follows:

Terminals C and E = 4 maximum
Terminal D = 5 maximum

Figure A.4*a* shows the circuit diagram and A.4*b* the logic symbol and the truth table. The typical power dissipation of this circuit for maximum fan-outs is:

3 mw at V_{CC} = +3 volts
11 mw at V_{CC} = +6 volts

SN510, FLIP-FLOP/COUNTER NETWORK, ONE PER PACKAGE. This circuit is a set/reset-type flip-flop with both the normal and the complementary outputs available. In addition, an input is available for clearing the circuit to a predetermined state. Also, an external clock pulse (which is internally capacitive-coupled) can be applied for timing purposes. The circuit is capable of a maximum fan-out of 4 from each of its outputs. The typical power dissipations for this

maximum fan-outs are:

$$2 \text{ mw at } V_{CC} = +3 \text{ volts}$$
$$7 \text{ mw at } V_{CC} = +6 \text{ volts}$$

Figure A.5*a* shows the circuit and A.5*b* gives the logic symbol.

SN511, FLIP-FLOP/COUNTER NETWORK WITH EMITTER-FOLLOWER OUTPUT. This circuit is basically the same flip-flop as the SN510. In addition to the two outputs Q and $\bar{Q}$ of Fig. A.5, this one contains two more sets of outputs Q_E and $\bar{Q}_E$ from emitter-followers tied to outputs Q and $\bar{Q}$ respectively. This increases the fan-out capability of the circuit as follows:

$$\text{Terminals } Q \text{ and } \bar{Q} = 4 \text{ maximum fan-out}$$
$$\text{Terminals } Q_E \text{ and } \bar{Q}_E = 20 \text{ maximum fan-out}$$

The power dissipations for a maximum fan-out of 10 are:

$$3 \text{ mw at } V_{CC} = +3 \text{ volts}$$
$$18 \text{ mw at } V_{CC} = +6 \text{ volts}$$

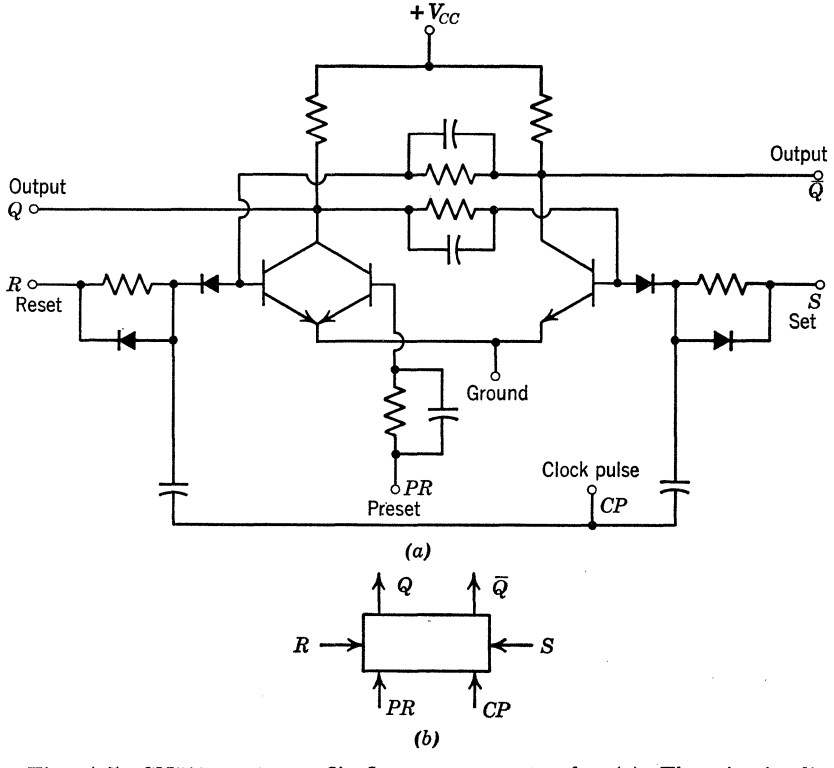


Fig. A.5 SN510 set/reset flip-flop/counter network. (*a*) The circuit diagram. (*b*) Logic symbol.

SOME CHARACTERISTICS OF THE TEXAS INSTRUMENTS, INCORPORATED SERIES 51 UNITS. TI mentions a propagation delay of 150 to 450 nanosec for $V_{CC} = +3$ volts and 75 to 225 nanosec for $V_{CC} = +6$ volts for their Series 51 units. The units are designed for d-c supply voltage of +3 to +6 volts ±10%, and their operating temperature range is −55°C to +125°C.

For component isolation, TI uses the "Triple Diffusion," which was discussed in Chapter 3. By using the relatively high-resistivity collector diffusion for the resistor elements, TI has been able to achieve up to 120 kilohms per each slice. TI uses the same basic diffusion pattern for all six members of the Series 51 family. By interconnecting the various elements by thin deposited lead patterns, the desired circuit configuration is obtained. This method is particularly well-suited to volume production with reasonably high yields.

The Standard Series 52 Line

Recently, Texas Instruments, Inc. announced circuits in their Series 52 Master Slice. These units contain the first commercially available *PNP* and *NPN* transistors diffused in the same silicon slice. Each chip contains five *NPN* transistors, two *PNP* transistors, and six resistors with values ranging from 5 to 50 kilohms. The presently available circuits consist of a basic differential amplifier intended for such applications as amplifiers in analog-to-digital converters, feedback amplifiers, integrators, differentiators, servo, and drive amplifiers.

SN521 OPERATIONAL AMPLIFIER. Figure A.6 shows the circuit schematic. Texas Instruments, Incorporated mentions the following typical operating characteristics for this unit:

Open-loop voltage gain	= 62 db
Common-mode rejection	= 60 db
Dynamic output voltage range	= ±2.5 volts
Frequency response	= d-c to 50 kc
d-c offset referred to input	= 2 mv
½-power frequency point	= 60 kc
Output impedance	= 8000 ohms
d-c drift referred to input	= 10 μv/°C
Input impedance:	
(1) differential	= 18 kilohms
(2) referred to ground	= 10 kilohms
Operating ambient temperature	= −20°C to +85°C
Supply voltages	= $++V_{CC}$ = +10 volts
	$+V_{CC}$ = +6 volts
	$-V_{CC}$ = −9 volts

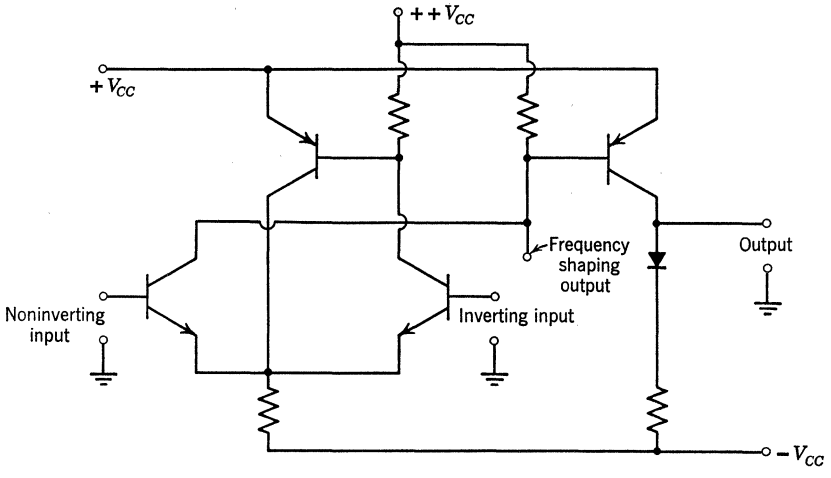


Fig. A.6 SN521 operational amplifier.

SN522 OPERATIONAL AMPLIFIER WITH EMITTER-FOLLOWER OUTPUT. Figure A.7 shows the circuit schematic. Basically it is the same amplifier but with an emitter-follower output. The operating characteristics of this circuit are the same as those of the SN521 but the output impedance is now typically 160 ohms.

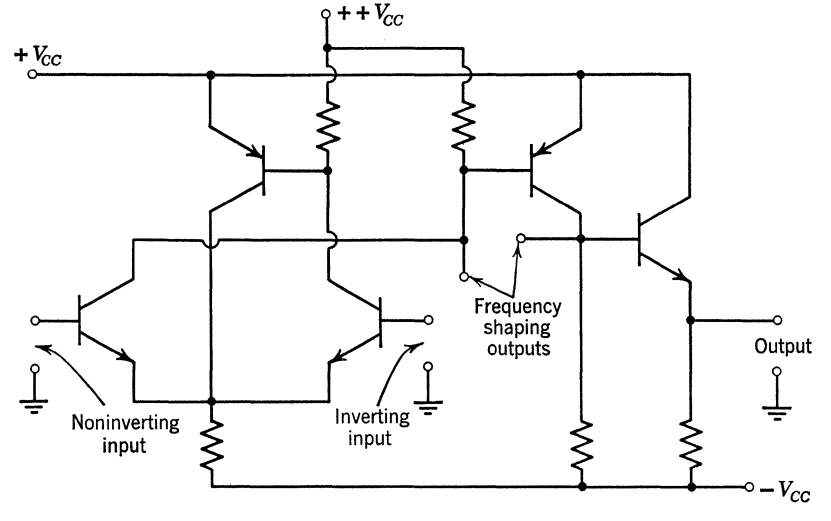


Fig. A.7 SN522 operational amplifier with emitter-follower output.

A.2 SIGNETICS CORPORATION, Sunnyvale, California

Signetics is relatively a newcomer to this field. They have utilized the DTL and TTL approaches for their standard line. The DTL line includes a NAND/NOR gate, an Exclusive-OR network, a buffer, and a binary element or trigger flip-flop. The TTL line to date consists of a NAND/NOR gate. Besides these, Signetics has a common anode-diode array available.

The DTL Standard Line

SE101 AND SE102 NAND/NOR GATES. The SE101 is a four-input gate, and the SE102 is a three-input gate. Otherwise the circuits are identical. Figure A.8*a* shows the circuit of the SE101. Signetics mentions a maximum fan-out of 5 for the full temperature range of $-55°C$ to $+125°C$, and a maximum fan-out of 10 for a restricted range near room ambient. For supply voltages of $V_C = 4$ v, $V_{BB} = 0$ v, and V_D open, the power dissipation per stage is typically 2.8 mw at an ambient temperature of 25°C and 50% duty cycle. At the same supply voltage, the average propagation delay per stage is 60 nanosec. For $V_D = 4$ v, $V_{BB} = -2$ v, and V_C open, the noise immunity is indicated as 0.5 volt.

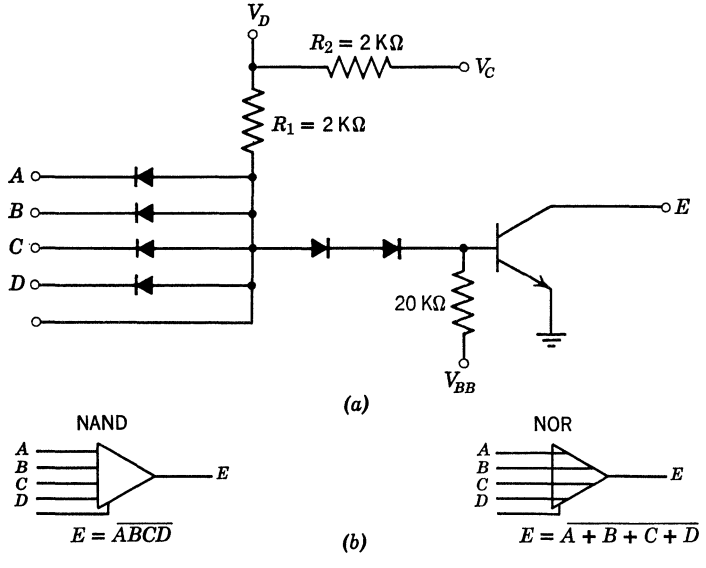


Fig. A.8 SE101 NAND/NOR gate circuit. (*a*) The circuit diagram. (*b*) Logic symbols.

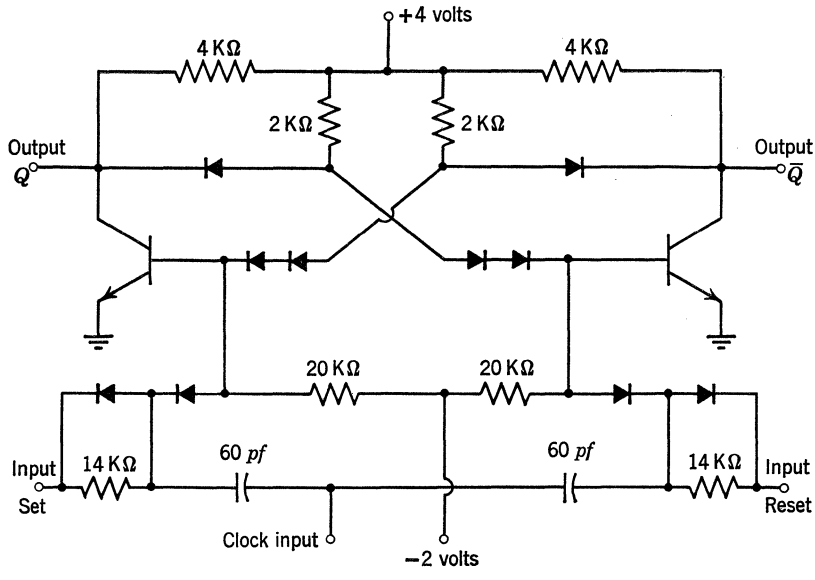


Fig. A.9 SE120 binary element flip-flop.

The circuit configuration and the pin layout of this unit is such that a certain amount of flexibility is available to the user. An extra input, pin 2, is provided without an input diode. The fan-in to the basic SE101 and SE102 gates can be increased by 6 by connecting the SE104 diode array (which is described later) to pin 2. Also, R_2, the 2-kilohm resistor between pins 4 and 6, is normally left unconnected. However, by externally connecting pin 4 to pin 3, it is possible to increase the d-c output level of the circuit for the UP or more positive condition. Another possibility is that R_2 can be connected in series with R_1 by applying V_0 at pin 4 instead of pin 6. Such a connection makes low-power operation possible. With this connection and pin 5 grounded, the driving capability of the gate is reduced. A reduction in speed also results from this type of connection.

SE120 BINARY ELEMENT. The SE120 is a high speed, low power, trigger-input flip-flop intended for Counter and Shift Register applications. The circuit is shown in Fig. A.9. For the supply voltages shown, a maximum fan-out of 4 is indicated from each output at the full temperature range of −55°C to +125°C. Typical power dissipation is 16 mw and the typical clock rate mentioned is 5 megacycles with a maximum fan-out of 4.

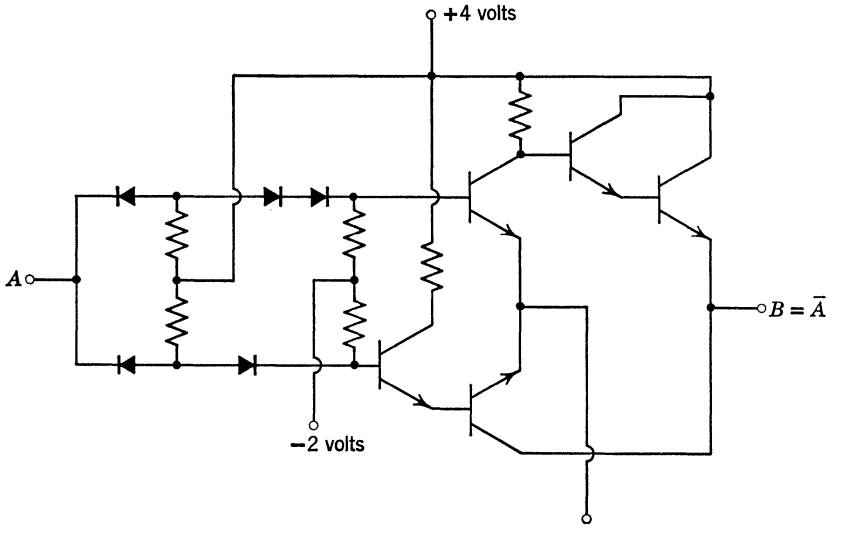


Fig. A.10 SE130 buffer element for high fan-out and line driver.

SE130 BUFFER ELEMENT. The SE130 serves as a buffer element for large fan-outs and as a driver for driving capacitive lines. Figure A.10 shows the circuit. At room temperature and with the supply voltages as shown, the circuit is capable of a maximum fan-out of 20. Under the same conditions, the typical power dissipation is 60 mw and the typical propagation delay per stage is 50 nanosec.

SE140 EXCLUSIVE-OR NETWORK. The SE140 is intended for use with SE101 and SE102 NAND/NOR gates and the SE120 Binary Element. The Exclusive-OR function is obtained by AND and OR gating. With the supply voltages as shown in Fig. A.11, the circuit

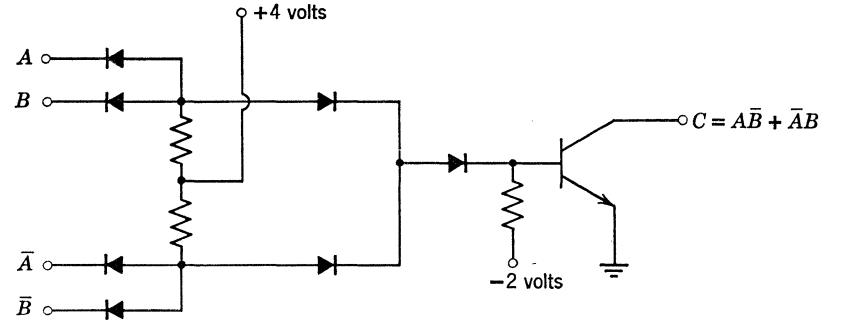


Fig. A.11 SE140 Exclusive-OR network.

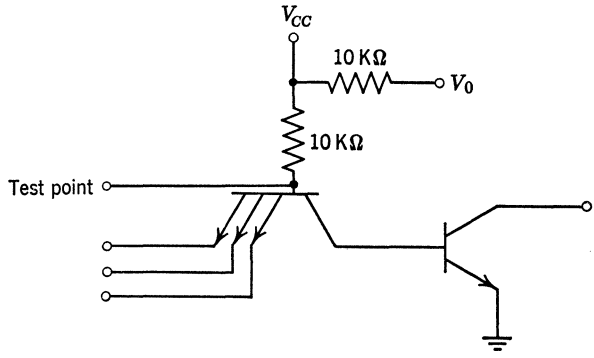


Fig. A.12 SE200 TTL/NAND circuit.

is capable of a maximum fan-out of 3 over a temperature range of $-55°C$ to $+125°C$. The typical power dissipation is 11 mw and the typical average propagation delay per stage is 35 nanosec.

The TTL Standard Line

SE200 TTL NAND GATE. SE200 is a 3-input TTL NAND gate as shown in Figure A.12. At a temperature range of $-55°C$ to $+125°C$, the circuit is capable of a maximum fan-out of 5 for supply voltages varying from 3 to 6 volts. For $V_1 = 3$ volts, the typical power dissipation is 0.6 mw and the propagation delay is 70 nanosec. For $V_{CC} = 6$ volts, the dissipation is 3 mw and the propagation delay is 30 nanosec.

SE104 Diode Array

The SE104, shown in Fig. A.13, consists of an array of six common anode diodes. The circuit could be used as an independent AND

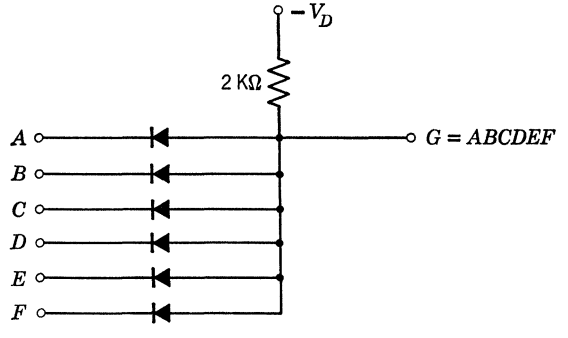


Fig. A.13 SE104 diode array.

gate. It could also be used to extend the fan-out capabilities of the SE101 and SE102 NAND/NOR gates. At room temperatures, the diodes have a recovery time of 3 nanosec from either a forward or a reverse current of 2 ma. At the same current, the diodes have a forward drop of 0.75 volt. The diode capacitance is typically 2 pf at a reverse voltage of 2 volts.

Some Characteristics of the Signetics Product Line

Signetics uses the "through diffusion" method for isolation purposes. However, they indicate that they are considering changing to a "triple diffusion" method in the future which would result in an increase in speed for the same power. Signetics uses the same diffusions and patterns for both the DTL and the TTL lines and then interconnects the elements by deposition techniques to achieve the desired circuit configurations.

A.3 AMELCO, INC., Mountain View, California

Amelco is also a comparative newcomer in the field of integrated circuits. At the time of this writing, Amelco had announced tentative specifications for only three integrated-circuit configurations. We shall briefly describe the highlights of these configurations.

MC100 Diode Logic Gate

The MC100 is a 3-input gate, as shown in Fig. A.14. Amelco states a maximum storage temperature of $-65°C$ to $+300°C$ and a maximum operating junction temperature of $-55°C$ to $+125°C$. The typical average propagation delay is 100 nanosec for $V_{CC} = +3$ v and $V_{BB} = -2$ v. A switching capability of 100 nanosec at power dissipations of 15 mw is indicated. Amelco mentions that although the

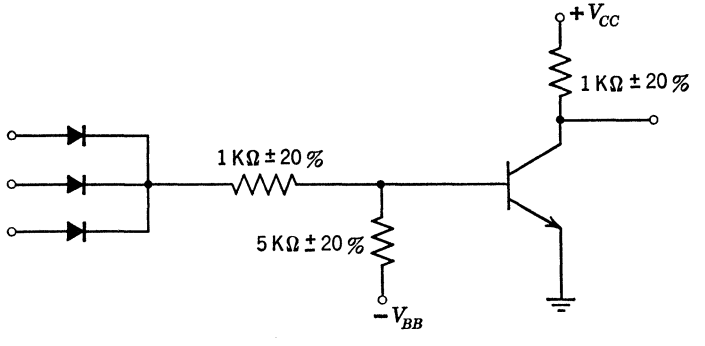


Fig. A.14 Amelco MC100 diode logic gate.

worst-case tolerance of the circuit elements is ±20%, all resistance deviations in any given circuit track within ±10%.

The SA100 Differential Amplifier Element

This assembly consists of a matched pair of isolated *NPN* silicon transistors mounted in one package and intended for applications where closely matched electrical parameters are required, such as in differential amplifiers. The d-c current gains of these units are indicated at 25 to 50 for collector currents of 10 μamps at V_{CE} of 5 volts.

SA102 Darlington Amplifier

This assembly consists of a high-gain compound transistor. The circuit is made up of two high-gain low-leakage *NPN* silicon transistors arranged in the convenient Darlington configuration. Amelco indicates a minimum d-c current gain of 5000 at collector current of 10 ma at V_{CE} of 5 volts. The total dissipation is 500 mw at 25°C ambient temperature.

Characteristics of the Amelco Line

Amelco packages all its products in the standard Jedec TO-5 or TO-18 package having an 8-lead header. The "separation diffusion" method is used for component isolation.

A.4 PACIFIC SEMICONDUCTORS, INC., Lawndale, California

Pacific Semiconductors (Division of Thompson Ramo Woolridge, Inc.) announced its first integrated circuits during the latter part of 1961. PSI is credited with having first introduced the Transistor-Transistor-Logic, or the TTL type of circuitry. PSI refers to these as Transistor-Coupled-Logic, or TCL. The first units consisted of a dual NAND circuit and a gated flip-flop. PSI subsequently expanded their product line to various logical configurations within a single unit, but basically using these two circuits. Consequently, we will confine our discussion only to these two circuits.

The Standard Line

PCG-101 DUAL NAND CIRCUIT. This transistor-coupled gate circuit is a 3-input gate, and PSI packages two of them in one unit. Figure A.15 shows the basic circuit. Actually, both a normal and a complementary output are available from this circuit. The circuit is capable of a maximum fan-out of 4 and a maximum propagation delay of 50 nanosec for one output load. The circuit is intended to operate over the temperature range of −55°C to +125°C with supply voltages from 3 to 6 volts. PSI mentions a nominal input impedance of 1 kilohm and an operating frequency of 5 mc.

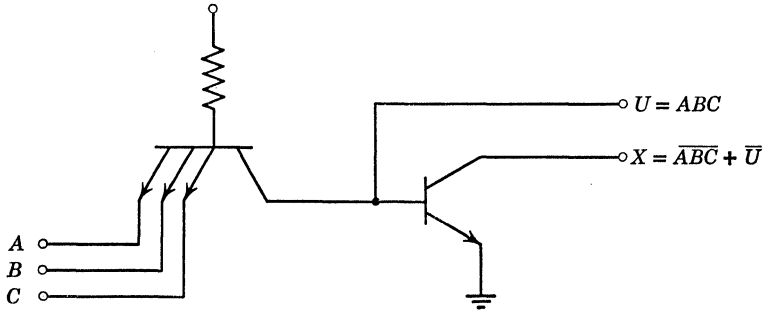


Fig. A.15 The PSI NAND circuit (basic configuration).

PCF-101 SET/RESET FLIP-FLOP. This circuit is a direct-coupled flip-flop, with multiple emitter transistors providing the input gating. Figure A.16 shows the circuit, which operates in the following manner:

Defining 0.2 volt as 0 and 0.8 volt as 1, a 1 is obtained at output Y if inputs A and C are both simultaneously 1. Similarly, output X is 1 if both inputs B and C are 1. If all three inputs are 1, then a 0 appears at both outputs X and Y. If input C is 0, the circuit will not respond to gate signals at A and B.

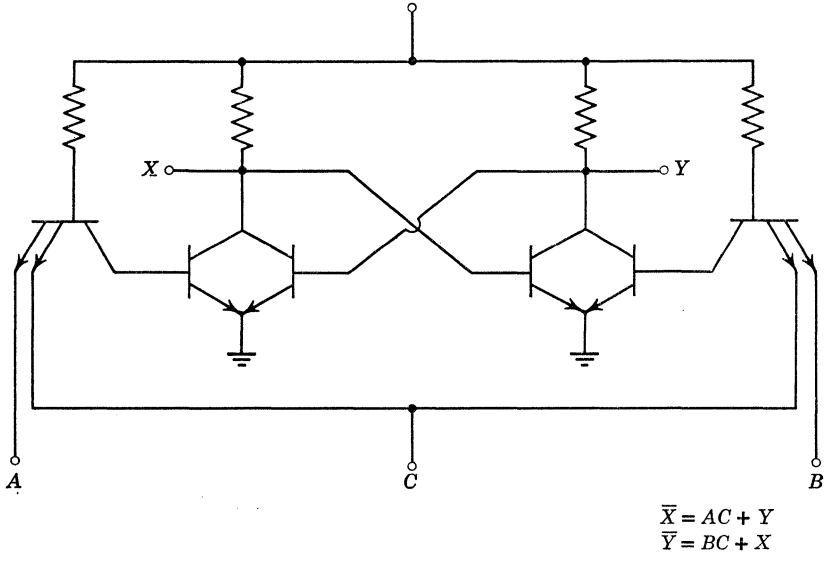


Fig. A.16 The PSI gated set/reset flip-flop.

The circuit is intended for the −55°C to +125°C operation with a maximum fan-out of 4 from either output. The propagation delay for one load output is 100 nanosec maximum, and the operating frequency is indicated at 3 mc.

Characteristics of the PSI Line

PSI units are available in either a TO-5 package with 12 leads or a TO-18 package with 8 leads. PSI uses the "triple diffusion" method for component isolation and the base diffusion for the resistive elements. A switching capability of better than 50 nanosec at power levels under 15 mw/NAND circuit is indicated.

A.5 WESTINGHOUSE ELECTRIC CORPORATION, Baltimore-Elkridge, Maryland

In the early days of the integrated circuits, Westinghouse did some very significant pioneering work. Westinghouse has again been very active in this field and has announced a very extensive array of product line, including both digital and nondigital circuits. This product line was available in production quantities during the first half of 1963. Since, in this appendix, we are concentrating our coverage of vendor products mainly to digital circuits, we shall discuss only the four digital circuits available at the time of this writing. For the benefit of those readers interested in nondigital circuits, a list of these is also included.

The Standard Digital Logic Line

WM-2101 DUAL NAND GATE. Westinghouse's digital line uses the conventional low-level-logic (discussed in Chapter 9) as the basic circuit type. The WM-2101 consists of two interconnected NAND circuits contained in one package. Each circuit has a fan-in of 3. Figure A.17 shows the configuration. The circuit is designed to

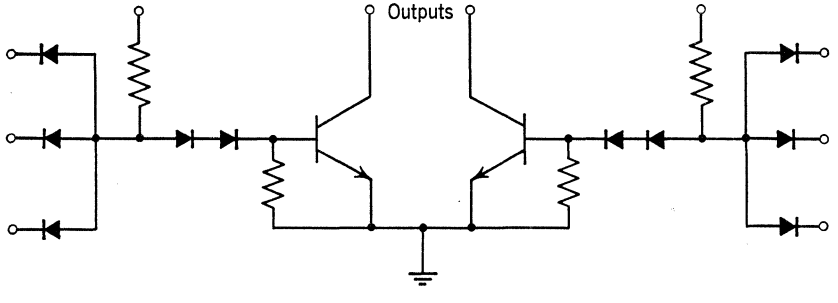


Fig. A.17 WM-2101 dual NAND gate.

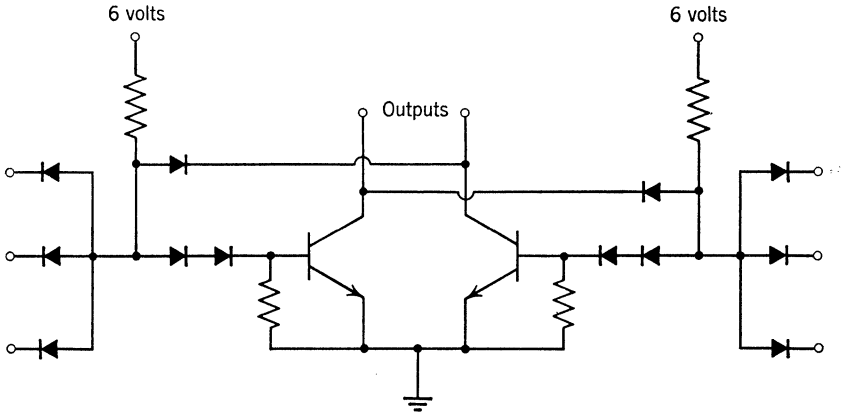


Fig. A.18 WM-2102 set/reset flip-flop.

operate over the −55°C to +125°C temperature range. The circuit (that is, each NAND individually) is capable of a maximum fan-out of 5 at typical power dissipation of 10 mw. The typical average propagation delay is 40 nanosec for a fan-out of 5. This data is indicated at 25°C. The maximum supply voltage is 7 volts.

WM-2102 SET/RESET FLIP-FLOP. This is the usual set/reset flip-flop with 3 inputs on each side. Each output is capable of a maximum fan-out of 4, at a typical power dissipation of 24 mw. The circuit has typical average propagation delay of 50 nanosec and Westinghouse mentions a maximum repetition rate of 9 mc. Figure A.18 shows the circuit.

WM-2104 SINGLE NAND GATE. The circuit is basically the same as the previously discussed WM2101 dual NAND gate except that it has

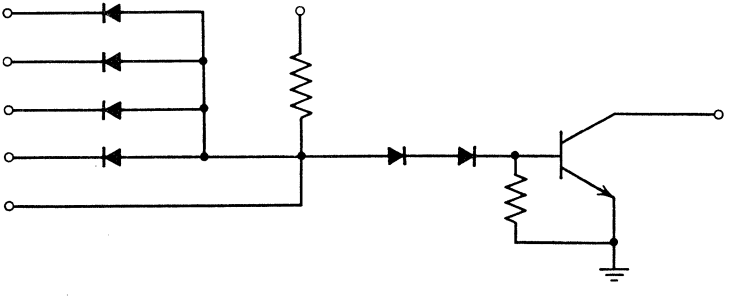


Fig. A.19 WM-2104 single NAND gate with expanded fan-in.

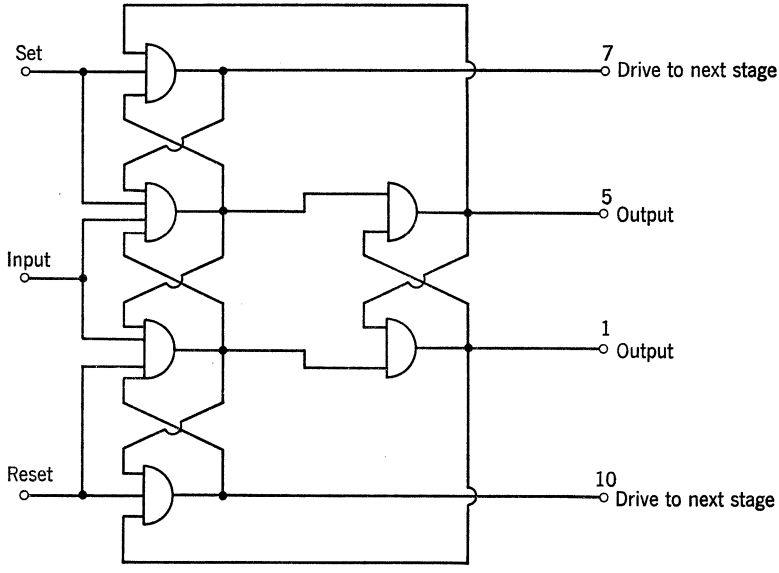


Fig. A.20 WM-2103 binary counter.

a fan-in of 4 instead of 3, and an additional pin without any input diode, which allows the user the facility of increasing the fan-in potential. The circuit is shown in Fig. A.19.

WM-2103 BINARY COUNTER. This configuration consists of six high-speed NAND gates internally connected on a single silicon chip to give a counter. The logical set-up is shown in Fig. A.20 and each individual NAND is similar to the one previously described. Westinghouse mentions a maximum counting rate of 5 mc. The circuit is d-c coupled and therefore, according to the vendor, insensitive to the rise-time of the driving signal; thus it operates as well with a sine wave as with a square wave input. The circuit operates over the temperature range of $-55°C$ to $+125°C$ and dissipates 75 mw of power. For pins 1 and 5, the fan-out capability is a maximum of 3, and for pins 7 and 10, it is 4.

The Standard Nondigital Line

For those readers who may be interested in circuits other than digital circuits, the following list of Westinghouse's standard products is given. Further information is available in their technical data sheets. Their respective numbers are also provided for handy reference.

1. RF Amplifier—WM1101: Provides a power gain of 30 db at frequencies up to 6 mc. Conventional external components provide bandpass tuning (*Technical Data 91-164*).
2. Oscillator-Mixer—WM1102: Intended for use with an external quartz crystal. Mixes RF carrier of up to 30 mc with the crystal frequency. Conversion gains of 10 db can be obtained.
3. IF Amplifier—WM1103: Gains of 30 db at frequencies up to 3 mc are obtained. Frequency tuning is done externally (*Technical Data 91-166*).
4. Audio Amplifier—WM1105: A wide band amplifier intended for Class A operation. Input resistance is greater than 1 megohm. An output of at least 3 watts is obtainable (*Technical Data 91-168*).
5. Video Amplifier—WM1106: Provides a minimum gain of 20 db with good temperature stability. Available in models having 3 db points of 6, 8, 10, and 12 mc (*Technical Data 91-169*).
6. Audio Amplifier—WM1208: A low-level amplifier with unipolar field-effect transistor input and bipolar transistor output. The input resistance is greater than 1 megohm. Can be used for isolating the load from the source (*Technical Data 91-172*).

A.6 FAIRCHILD SEMICONDUCTOR, Mountain View, California

Fairchild Semiconductor is one of the earliest companies in the integrated-circuits field. In 1961, they announced availability of a

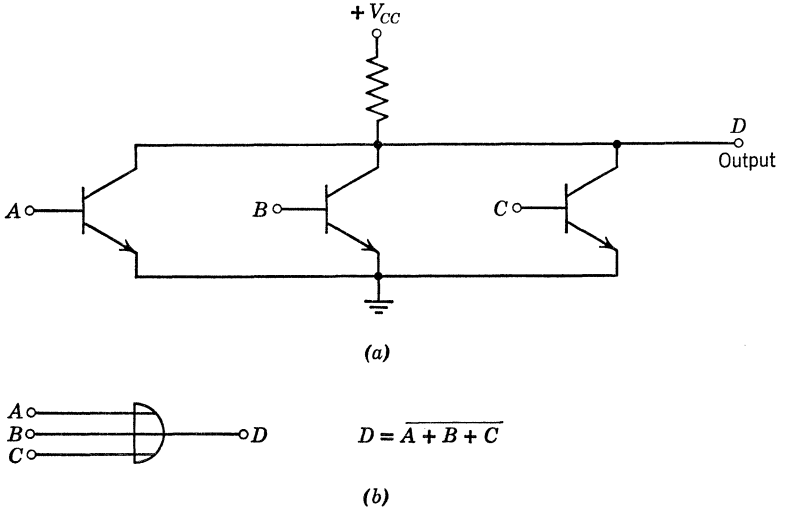


Fig. A.21 Fairchild "G" element gate. (*a*) The circuit diagram. (*b*) Logic symbol and the Boolean expression.

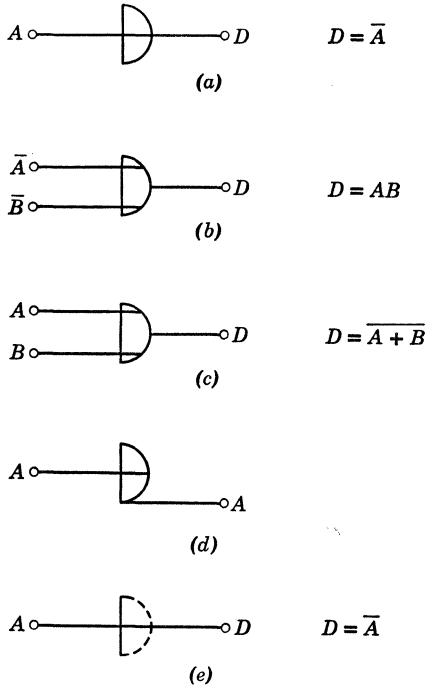


Fig. A.22 Fairchild standard logic symbols and Boolean expressions. (*a*) NOR gate used as an inverter. (*b*) NOR gate used to obtain the AND function. (*c*) NOR gate used to obtain the OR (NOT) function. (*d*) The emitter-follower. (*e*) Inverter without node resistor.

line of devices under the trade name Micrologic. Today, the Micrologic line is a family consisting of a Gate, a Flip-Flop, a Buffer, A Half Adder, a Counter, and a Half-Shift Element. The basic Micrologic circuit is a NOR circuit and this is the building block of the entire line. Consequently, in our discussion, the circuit diagram for only the gate is shown along with logic symbols. For the rest of the product line, only logical symbols, interconnected in the appropriate manner, are shown. The logical symbols are shown in Fig. A.22.

The Standard Micrologic Line

THE "G" ELEMENT, GATE. This circuit is the basic element of the Micrologic line. It consists of a three-input NOR. The circuit type used is the direct-coupled-transistor logic, or DCTL. Figure A.21*a* shows this circuit. Figure A.21*b* shows the logic symbols and the Boolean expressions that Fairchild uses for defining their entire Micrologic Series.

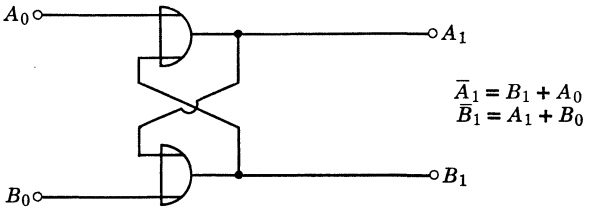


Fig. A.23 The "F" element, flip-flop.

The "G" element gate uses a supply voltage of $+3 \pm 10\%$ volts and is operable over the standard temperature range of $-55°C$ to $+125°C$. The circuit has an average propagation delay of 50 nanosec and a fan-out capability of 5 at typical power levels of 15 mw.

THE "F" ELEMENT, FLIP-FLOP. This circuit is shown in Fig. A.23 and uses two of the gate elements internally connected as flip-flop. Each output is capable of a maximum fan-out of 4, and the circuit typically dissipates 30 mw of power. The circuit has an average propagation delay of 50 nanosec and operates over the standard temperature range.

THE "B" ELEMENT, BUFFER. This configuration is basically a low-impedance, cascade emitter follower, and is primarily intended for driving long lines or clock busses. In those cases where a larger fan-out is required from the other logic elements, the "B" element can be used to supplement the fan-out. Output B_1 has a drive capability of 5, while output B_2 is a low-impedance output with a fan-out capability of 25. Outputs B_1 and B_2 may not be used concurrently. Figure A.24 shows the logical configuration. Output B_1 has an average propagation delay of 50 nanosec and B_2 of 100 nanosec. Typical power dissipation for this circuit is 25 mw.

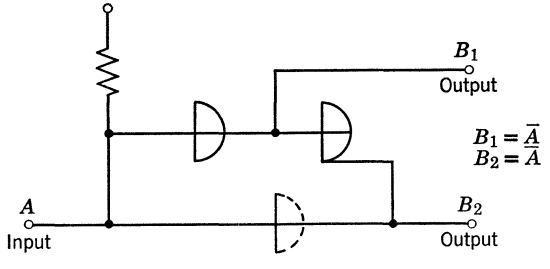


Fig. A.24 The "B" element, buffer.

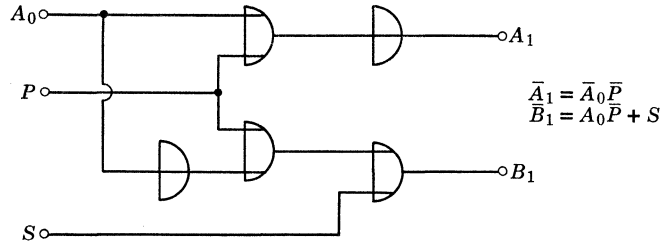


Fig. A.25 The "C" element, counter adapter.

THE "C" ELEMENT, COUNTER ADAPTER. This is a rather versatile circuit which can perform a multitude of different functions. The configuration is shown in Fig. A.25. It can be used with two "S" elements (to be discussed later), to provide the "carry" function for parallel or serial fast carry counters.[1] It can also be used to provide retimed inputs to a shift register from data busses. Input terminals A_0 and P equal two Micrologic loads and input terminal S equals one Micrologic load. Outputs A_1 and B_1 each have a fan-out capability of 5. The average propagation delay is 100 nanosec and the circuit dissipates 75 mw typically.

THE "H" ELEMENT, HALF ADDER. This element provides an "Exclusive OR" function which is widely used in adders. In addition, it also provides a true AND output for the two inputs. The S output has an average propagation delay of 100 nanosec, and the C output has one of 50 nanosec. The S output has a maximum fan-out capability of 5 and the C output a maximum fan-out of 4. Typically, the circuit dissipates 45 mw. Figure A.26 shows the circuit.

THE "S" ELEMENT, HALF-SHIFT REGISTER. Using the "master-slave" technique,[1] the "S" element performs both the counting and the shifting functions. The circuit is basically a double-gated flip-flop and an inverter and can be used as strobe gate for retiming. In adders, it can

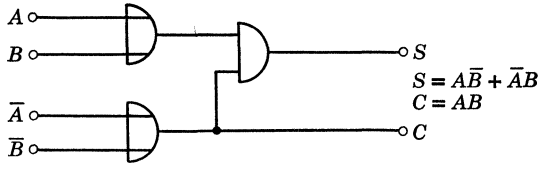


Fig. A.26 The "H" element, half adder.

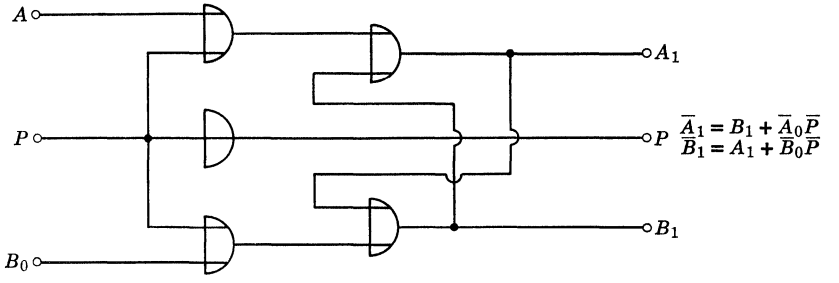


Fig. A.27 The "S" element, half-shift register.

also be used as a one bit delay. Inputs A_0 and B_0 have a fan-in of one and P has a fan-in of 3. Outputs A_1 and B_1 have a fan-out of 4 each and $\bar{P}$ has a fan-out of 5. The circuit has an average propagation delay of 100 nanosec and typically dissipates 75 mw. The circuit is shown in Fig. A.27.

Some Notes on the Micrologic Line

The entire Micrologic line to date is packaged in the standard Jedec TO packages with eight-lead headers. Fairchild uses the "separation diffusion" method for component isolation. The base diffusion is used for forming the resistive elements. Since DCTL is used, the problems associated with the Micrologic line are those basically inherent in the DCTL circuits. Mainly, these are low noise margins and current hogging. Fairchild has added a 100-ohms base resistor in their Micrologic circuits, which of course reduces the current-hogging problem but does not eliminate it. Fairchild has extensive production facilities, presently capable of producing Micrologic units exceeding 10,000 per month.

A.7 SPERRY SEMICONDUCTOR, Norwalk, Connecticut

Sperry Semiconductor has been one of the earlier companies in this field. Lately Sperry has been confining its work to special orders and basic development, and consequently has a rather limited product line. Sperry uses the Diode-Transistor-Logic (DTL) as the circuit type. Using DTL-NOR as the basic circuit, Sperry has announced four digital circuits in its standard 11S8 line, under the tradename Seminets. Besides these, two amplifier configurations are also available as standard products.

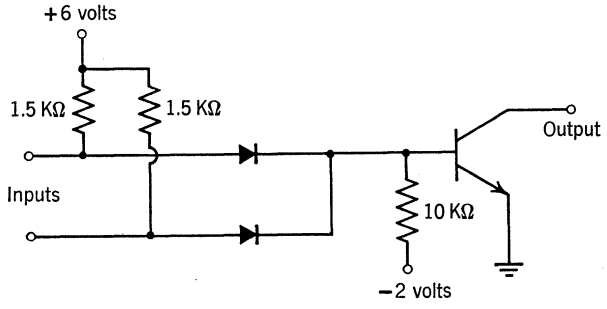


Fig. A.28 The Sperry "Semi-Net" NOR circuit with two inputs.

The Standard Digital Line

THE 2-INPUT NOR GATE, TWO PER PACKAGE. Figure A.28 shows this circuit. Two such circuits are in one package. The minimum fan-out is 4 and the typical is 6. The minimum fan-in per input is 4 and the typical is again 6 per input terminal per gate. Sperry indicates a typical propagation delay of 150 nanosec and a maximum of 500 nanosec. The circuit package dissipates a maximum total power of 150 mw.

THE 4-INPUT NOR GATE, ONE PER PACKAGE. The circuit is shown in Fig. A.29 and is basically the same as the one described in the previous paragraph. The fan-in capability of this circuit is a minimum of 4 per input (16 total per gate) and typically 6 per input (24 total per

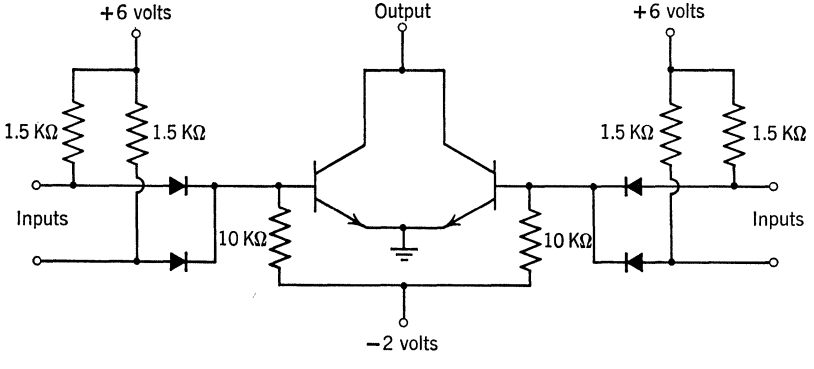


Fig. A.29 The Sperry 4-input NOR gate circuit.

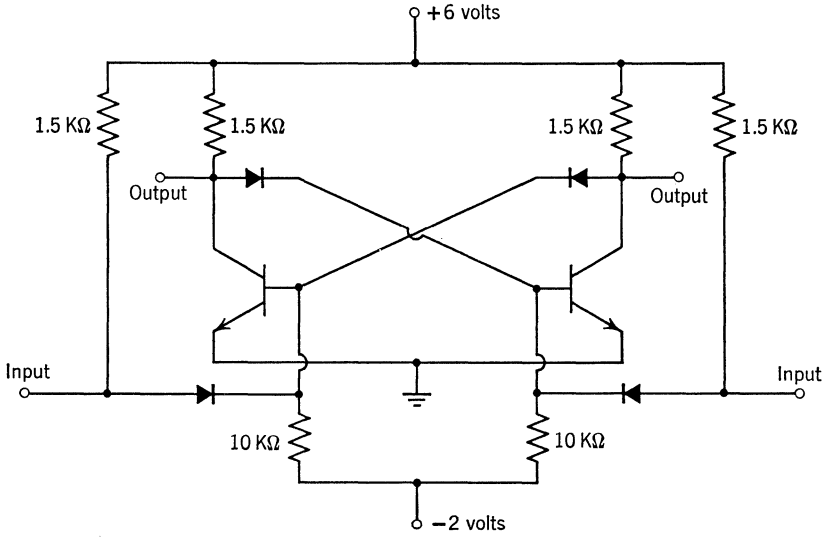


Fig. A.30 The bistable multivibrator.

gate). The fan-out is a minimum of 4 and typically 6. The propagation delay is also minimum of 150 nanosec and typically 500 nanosec.

THE BISTABLE MULTIVIBRATOR, ONE PER PACKAGE. Figure A.30 shows the flip-flop circuit which is constructed from the basic NOR circuit by internally modifying the interconnections. This circuit requires a typical trigger level of +1.5 volts and a minimum of +1.0 volt. The minimum repetition rate is indicated at 500 kc. However, Sperry mentions a typical repetition rate of 1 mc. The minimum fan-in per input is 3, and the typical is 5. Similarly, the minimum fan-out is 3 per output, and typically it is 5 per output.

COMMON-CATHODE DIODE ARRAY. The 10S4 diode array consists of 4 silicon diodes with their cathodes tied together and mounted in one package. Figure A.31 shows the configuration. The peak inverse

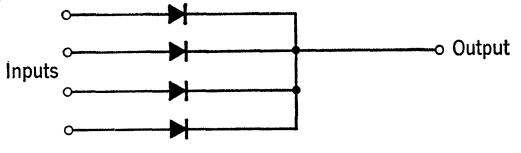


Fig. A.31 The common-cathode diode array.

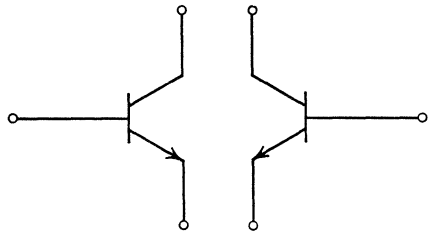


Fig. A.32 The 302S2 differential amplifier unit.

voltage is 40 volts maximum. The d-c forward current per diode is 200 ma maximum. The peak forward current pulse is indicated at 800 ma. At room temperature, the maximum total power dissipation is 800 mw, and the operating temperature range is $-65°C$ to $+200°C$. The typical reverse recovery time is 0.1 μsec, switching from a forward current of 5 ma to a reverse current of 0.5 ma (recovery to V_R of 0.2 volt).

The Standard Amplifier Line

THE 302S2 DIFFERENTIAL AMPLIFIER. This unit consists of two low-leakage *NPN* planar silicon transistors in one package, with all three terminals of each transistor available externally (Fig. A.32). The transistors are closely matched for d-c current gain and base-to-emitter voltage. The maximum V_{CE} (with base open) is 60 volts. The maximum V_{EB} is 8 volts and maximum V_{CB} is 100 volts. These ratings are at room temperature. The maximum dissipation per transistor is 500 mw at room temperature. The maximum d-c current gain is 80 (V_{CE} = 5 v, I_C = 0.1 ma) and the maximum I_{CBO} at room temperature is 2 nanoamps (V_{CB} = 80 v, I_E = 0).

THE 300S2-301S2 HIGH GAIN *NPN* COMPOUND AMPLIFIER. Figure A.33 shows the circuit configuration which is the same for both

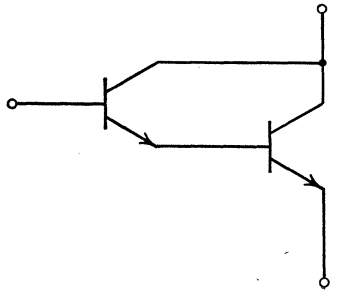


Fig. A.33 300S2 and 301S2 Darlington compound amplifier.

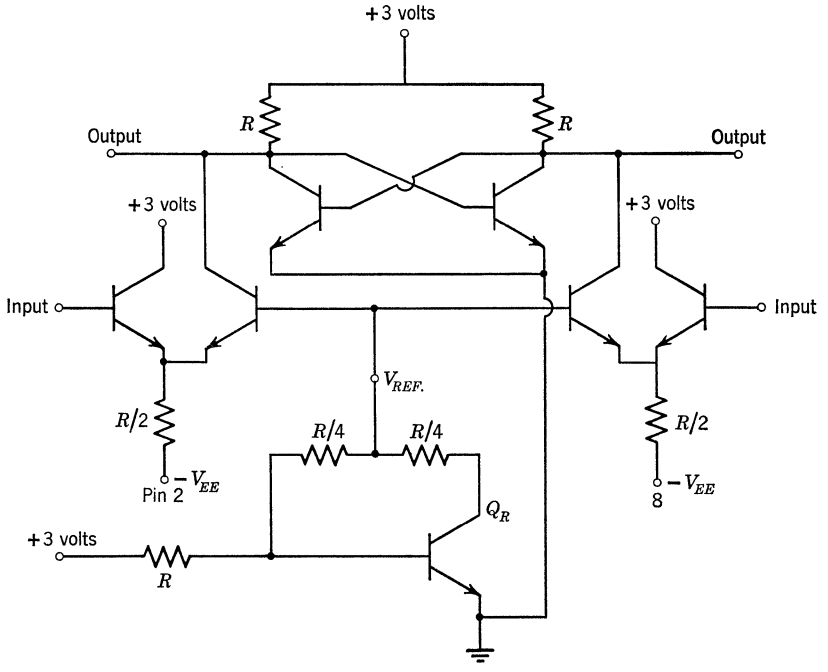


Fig. A.34 The ECLO set/reset flip-flop.

300S2 and 301S2. The circuit consists of two *NPN* planar silicon transistors connected in the familiar Darlington Compound arrangement. The 301S2 is packaged in the Jedec TO-18 unit and the 300S3 in the TO-46. At room temperature, the maximum d-c current gain is 10,000 (V_{CE} = 5 v, I_C = 10 ma), the maximum $V_{CE(SAT)}$ is 0.9 volt (I_C = 10 ma, I_B = 1 ma), the maximum $V_{BE(SAT)}$ is 1.6 volts (I_C = 10 ma, I_B = 1 ma), and the maximum I_{CBO} is 2 nanoamps (V_{CB} = 80 v, I_E = 0). Also, at room temperature, the following minimum voltages are indicated by Sperry:

$$BV_{CEO} = 60 \text{ volts } (I_C = 10 \text{ ma}, I_B = 0)$$
$$BV_{CBO} = 100 \text{ volts } (I_C = 10 \ \mu\text{a}, I_E = 0)$$
$$BV_{EBO} = 15 \text{ volts } (I_E = 10 \ \mu\text{a}, I_C = 0)$$

At room temperature, the maximum power dissipation of the 300S2 is 400 mw, and that of the 301S2 is 800 mw.

Characteristics of the Sperry Line

Sperry mentions total power dissipation of 150 mw per unit for the 11S8 digital line. Turn-on time (that is, rise plus delay time) for

these units is typically 75 nanosec, and the typical turn-off time (that is, storage plus fall time) is 150 nanosec, according to Sperry. For isolating the components, Sperry uses the "through diffusion" method.

A.8 GENERAL ELECTRIC, Syracuse, New York

General Electric heralded its entry in the integrated circuits field recently by announcing availability of its product line under the tradename of Emitter-Coupled Logic Operators, or ECLO. Utilizing a comparatively new form of logic—the emitter-coupled-transistor-logic (ECTL)—as its standard form, G.E. has introduced a family of seven logic circuits, which are available on two-weeks delivery in sample quantities.[2] The ECLO family uses planar, epitaxial *NPN* transistors of passivated construction similar to the 2N914.

The Standard ECLO Line

THE P321 SET/RESET FLIP-FLOP. Figure A.34 shows the circuit of the flip-flop. This circuit, in addition to its normal set/reset operation, can be used in conjunction with a clocking system. In this case, pins 2 and 8 are used for clocking. Normally they are connected to a d-c negative bias. The reference voltage is generated by transistor Q_R and the resistor divider network connected between its base and collector.

THE P322 AND GATE. The P322 is a 3-input AND gate as shown in Fig. A.35. Since the output is taken from the reference transistor, a noninverted output is obtained. In other words, the circuit is a

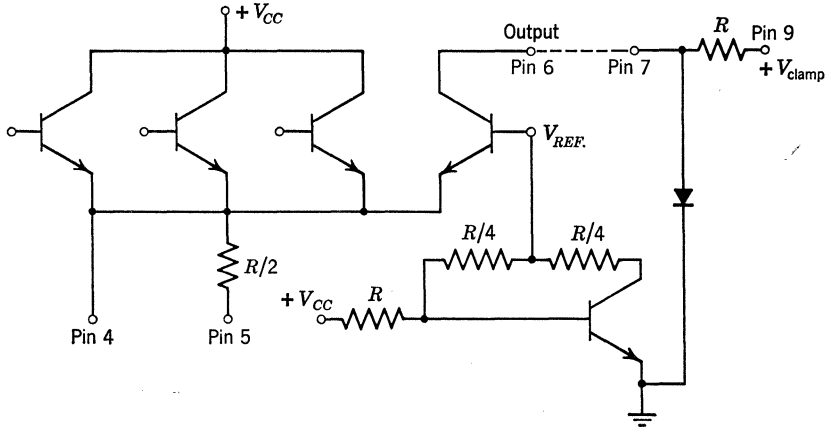


Fig. A.35 The P322 AND gate.

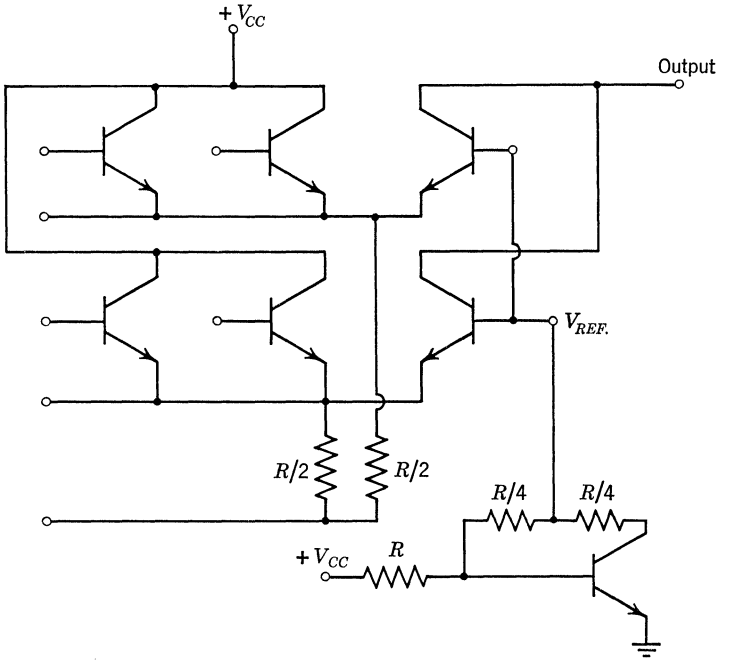


Fig. A.36 The P323 AND-OR gate.

true AND and not a NAND for positive signals. A clamped output can be obtained, if so desired, by externally connecting pins 6 and 7 together and applying a suitable positive supply voltage at pin 9. Also, the user has the choice of connecting the common emitters of the input transistors to ground or to a suitable voltage, either directly through pin 4 or via resistor $R/2$ through pin 5.

THE P323 AND-OR GATE. As shown in Fig. A.36, the P323 consists of two 2-input AND gates whose outputs are tied together to give an OR function. No provision is made for clamped output but the user does have the choice of applying ground or other potential to the two common emitter points, either directly or through the two $R/2$ resistors.

THE P324 HALF-SHIFT REGISTER. The P324, shown in Fig. A.37, is really a DCTL flip-flop with gated inputs. A straight DCTL flip-flop can be obtained by connecting pins 5 and 8 to ground. Here, the two inputs are to pins 2 and 7, and these are driven from the outputs of unclamped gates, representing complementary inputs. Pins 3 and 6 are used when series gate resistors, R and R are required either for isolation purposes or for gate terminations.

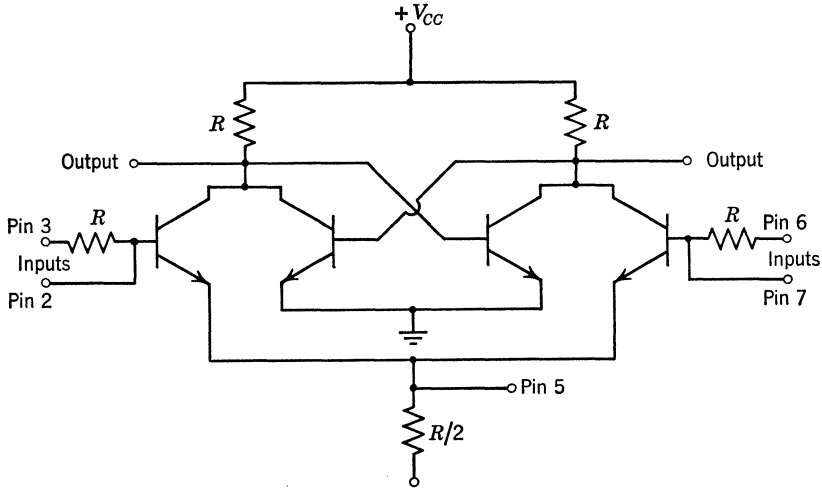


Fig. A.37 The P324 half-shift register.

THE P325 INVERTER. Figure A.38 shows the P325 circuit, which basically consists of four inverters. This configuration is very versatile and can be used for purposes other than four-inversion functions. For example, a DCTL flip-flop can be readily connected by cross-connecting the bases and collectors of two transistors and using the other two transistors for inputs by connecting their collectors, one to each of the flip-flop collectors. The base-emitter junction and the

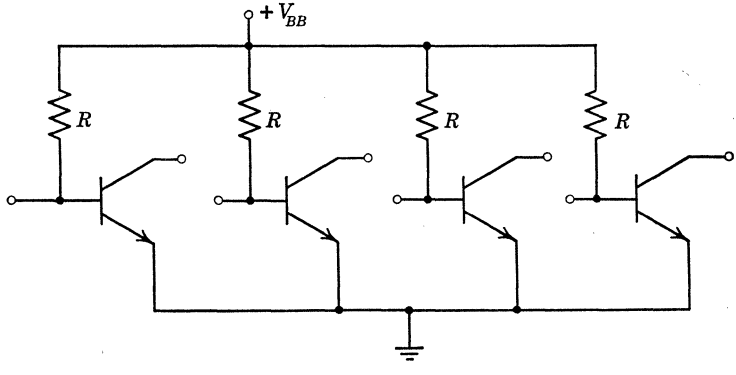


Fig. A.38 The P325 inverter.

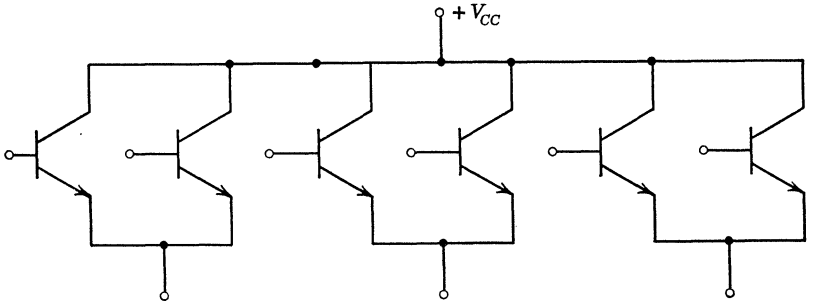


Fig. A.39 The P326 AND inputs.

resistor can be used for clamping the output of a gate or that of another inverter.

THE P326 AND INPUTS. This configuration, shown in Fig. A.39, consists of three pairs of transistors with common emitter and is intended to provide expanded fan-in capabilities for the P322 AND and the P323 AND-OR gates.

THE P327 MAJORITY GATE. Figure A.40 shows this configuration which consists of two sets of 3-input gate resistors. These gates are designed for vote redundancy applications, to be used with the P324 half-shift register.

Some Notes on the General Electric Line

G.E. packages all its ECLO circuits in standard TO-5 cans with 10 leads. At the time of this writing, detailed individual specification sheets on each circuit were not available. G.E., however, indicates the following general information, which is applicable to the entire line:

The circuits have an operating temperature of $-55°C$ to $+125°C$. The maximum repetition rate for the clock is 2 mc. The peak clock voltage, wherever used, is 3.5 volts, and the average clock supply load per circuit is 3 mw. A +3-volt power supply is used and the

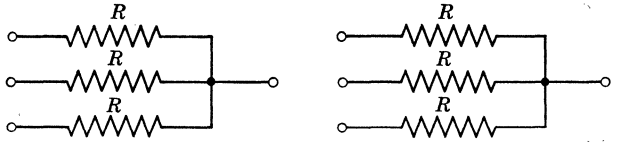


Fig. A.40 The P327 majority gate.

average power supply dissipation per circuit is 10 mw. The bias supply, wherever applicable, is −3.5 volts.

A.9 MOTOROLA SEMICONDUCTOR PRODUCTS, INC., Phoenix, Arizona

Motorola has been engaged in developmental work for quite some time. Motorola appears to have concentrated heavily in the area of nonlogic circuits of special custom design. They have also specialized in the partially or the hybrid-integrated approach for these circuits. Motorola announced that a line of off-the-shelf units in both digital and linear fields will be introduced shortly. While detailed specification sheets on these circuits were not available at the time of this

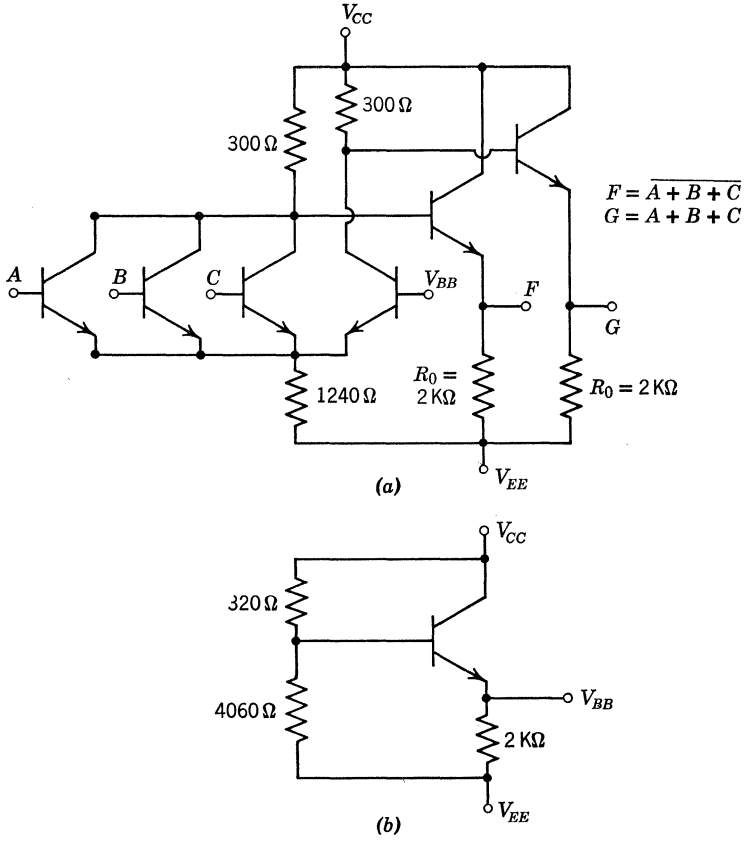


Fig. A.41 The MECL logic gate. (*a*) The basic MECL circuit. (*b*) The bias regulator circuit.

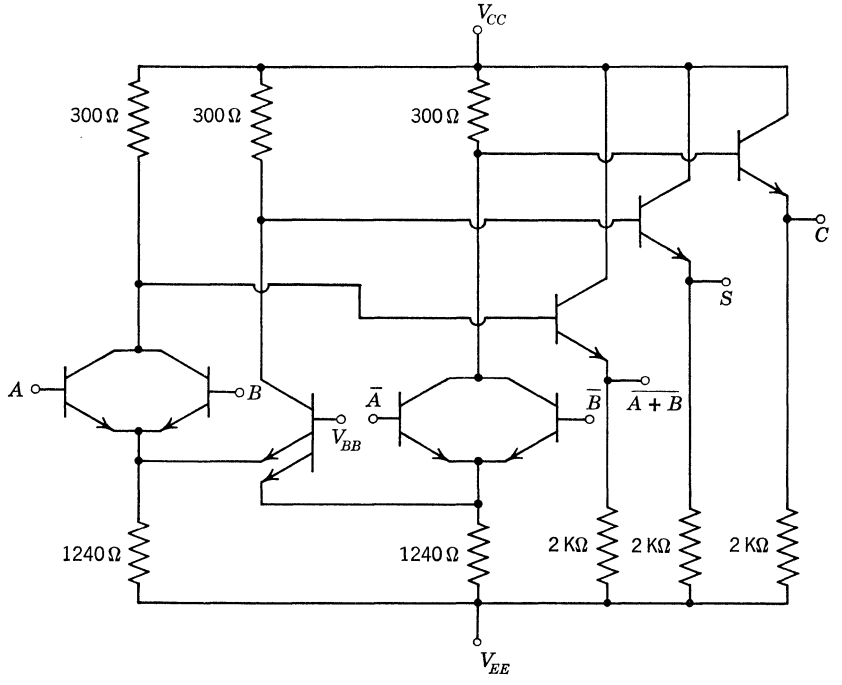


Fig. A.42 The MECL half-adder.

writing, it is indicated that Motorola will be using the nonsaturating current-mode logic as the circuit type for their digital line under the tradename, Motorola Emitter-Coupled Logic, or MECL.[3]

The MECL Standard Digital Line

THE MECL LOGIC GATE. The basic MECL logic gate is shown in Fig. A.41*a*, and the bias regulator circuit, for optimum temperature stability, in Fig. A.41*b*. The gate has a typical fan-in capability of 3 but this can be increased to 25 with an expander unit, which is also available. The typical fan-out is 6 and the maximum is 26. The circuit has a typical propagation delay of 4 nanosec. The operating range is $-55°C$ to $+125°C$. Motorola also mentions these typical parameters: rise time of 4 nanosec, fall time of 5 nanosec, power dissipation of 35 mw, input capacitance of 6 pf, noise immunity of $\pm 50\%$ of logic swing, and a power supply requirement of 5.2 volts with a tolerance of $\pm 20\%$.

THE MECL HALF-ADDER. This circuit, shown in Fig. A.42, has d-c characteristics similar to the previously discussed gate. With a fan-out of 1, the propagation delay of this circuit is 4 nanosec.

THE MECL FLIP-FLOP. Figure A.43 shows the flip-flop which basically consists of two gate circuits cross-coupled. The basic flip-flop performs the set/reset function, but a toggle-type function can also be obtained by using it in conjunction with the half-adder. In this case, the A, B, and the C outputs are connected to two inputs to the flip-flop.

Some Notes on the Motorola MECL Line

Motorola's present MECL line is available in the standard TO-5 can with 10 leads. However, it has been indicated that they are planning on a flat 0.25 in. by 0.25 in. package, 50 mils thick, with 5-mil leads on 50-mil centers. Motorola isolates the components by the "triple diffusion" method. Resistors are formed by using the base diffusion. This method improves the temperature coefficient of resistance but also limits the resistance value available per chip. The characteristics of the transistors can best be indicated as falling between the limits set by the 2N834 and the 2N709. The circuits are designed such that their d-c characteristics are dependent on resistance ratios rather than transistor characteristics.

A.10 SILICONIX INC., Sunnyvale, California

Siliconix is a comparative newcomer to the field and to date has announced sample quantity availability of a unique dual NAND/NOR

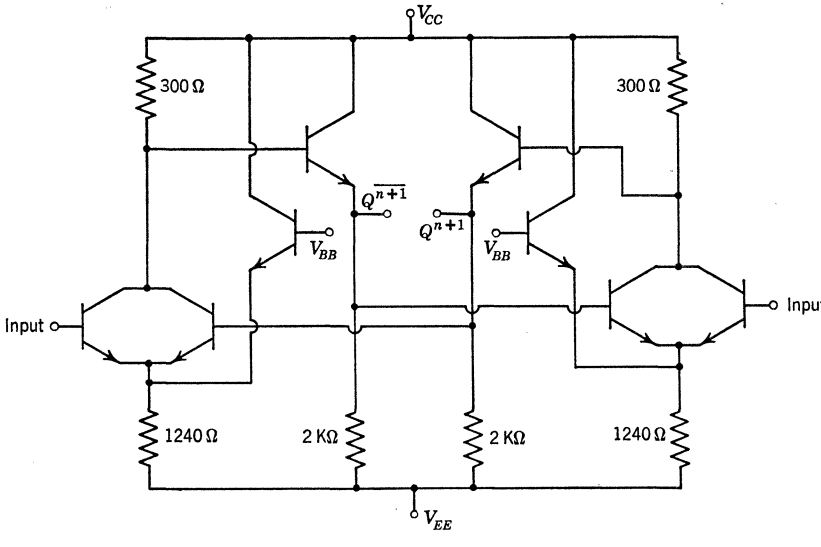


Fig. A.43 The MECL flip-flop.

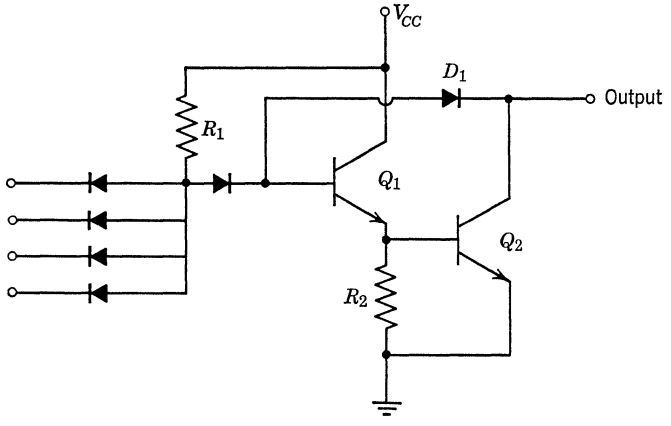


Fig. A.44 Type AO2A dual NAND/NOR gate.

gate in integrated form. The circuit is shown in Fig. A.44, and two such circuits are available in a 12-leaded TO-5 can with both circuits on the same silicon wafer.

The circuit is a modified DTL configuration which is intended to provide high-speed performance with relatively low power. The circuit is load-compensated by the emitter-follower transistor, Q_1. When each input is turned off, enough current is drawn from the power supply to keep transistor Q_2 turned on over a wide range of collector currents. Consequently, the fan-out is limited by stability requirements. Siliconix indicates the following typical characteristics for this circuit with $V_{CC} = 4$ v:

Typical power dissipation per gate at 25°C	5 mw
Maximum fan-in	4
Maximum fan-out, at 25°C	22
Maximum fan-out, at 125°C	5
Typical average propagation delay per gate at 25°C	12 nanosec
Worst-case d-c voltage stability at 125°C and fan-out = 5	100 mv minimum
Operating temperature range	−55°C to +125°C
Storage temperature range	−55°C to +200°C

A.11 OTHER VENDORS

The vendors and their product lines discussed in this appendix certainly do not comprise the complete roster of companies engaged in

this field. The following is a partial list of vendors whose microcircuits are either available or will soon be available on the market.

1. CLEVITE TRANSISTOR
2. GENERAL INSTRUMENT SEMICONDUCTOR, Division of General Instrument Corporation
3. MOLECULAR SCIENCE
4. RAYTHEON COMPANY, Semiconductor Division
5. SPRAGUE ELECTRIC COMPANY
6. SYLVANIA ELECTRIC PRODUCTS, INC.
7. TRANSITRON ELECTRONIC CORPORATION

It should be noted that some of these companies do have product lines which incorporate the hybrid or the partially integrated approach. These were not considered in this appendix since it is confined to the area of fully integrated circuits only.

A.12 ACTIVITIES IN FOREIGN COUNTRIES

While the bulk of the work in this field is carried on in the United States, several foreign firms and universities are also actively interested in it.

Tokyo University, Japan

At the annual convention of Japan's four electrical societies in April 1962, Kunio Tada of Tokyo University presented a solid-state module for DCTL circuits, using six mesa transistors formed at one end of an N-type silicon bar with their emitters tied together. Inputs are applied to individual bases, and the circuit performs AND and OR functions.[4] Using gold diffusion, a propagation delay of 0.5 μsec has been achieved.

Nippon Electric Company Ltd., Japan

Nippon Electric of Japan thinks that a hybrid approach of putting all active components on one slice in one package and passive components in another will result in significant short-term advantages.[5] The first group of logic packages will contain either six diodes or six transistors, fabricated on single silicon wafers. The reverse-biasing method will be used for isolation. The NOR packages are expected to be available in three types; (1) One 6-input NOR gate, (2) two 3-input gates, (3) three 2-input NOR gates. Operating the DCTL circuits in the saturated mode, clock rates up to 4 mc are mentioned. In addition to these, two packages with only two transistors are planned for other applications, such as differential and Darlington amplifiers. The diode units will have six diodes but will be available in three types of AND gates and four types of OR gates.

European Countries

Several countries in Western Europe are actively working with integrated circuits, either as manufacturers or as users. Unfortunately, at the time of writing of this book, details of activities in Europe were not readily available to the author. It is known that several companies in West Germany, Great Britain, France, Italy, and Sweden have programs dealing with fully integrated circuits, thin-film devices or hybrid combinations of the two. One report indicates "tremendous interest in applying integrated circuits to commercial computers and process control systems."[6] It is anticipated that several European firms will be using integrated circuits in their products in the foreseeable future.

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2. "High-Density Micrologic Package Allows Do-It-Yourself Circuit Design," *Electronic Equipment Engineering*, September 1962, pp. 14–16.
3. J. A. Narud, W. C. Seelbach, and N. Miller, "Advanced Integrated Circuit Logic Designs," Part 1—*Electronic Industries*, November 1962, pp. 118–122. Part 2—*Electronic Industries*, December 1962, pp. 111–115.
4. Charles Cohen, "Japanese Components Men Stress Integrated Circuits and Diodes," *Electronics*, May 4, 1962, pp. 20–21.
5. "Logic Blocks Offer Design Flexibility," *Electronics*, July 27, 1962, pp. 58–61.
6. "Microelectronics Around the World," Staff Report, *Electronics*, August 2, 1963, pp. 37–43.

Appendix B
Standard-line circuits using the multiple-chip approach

Any vendor who can make fully integrated circuits can certainly fabricate units with multiple chips, utilizing any one of the previously discussed techniques. However, the number of vendors offering standard product lines with multiple chips is somewhat limited at the present time. The trend appears to go fully integrated, if at all possible, resorting to multiple chips only in those cases where full integration is not readily possible or economically feasible.

B.1 THE FAIRCHILD SPECIAL PRODUCTS LINE

One of the earliest vendors to offer a broad line of chip circuits was Fairchild Semiconductor. Their Special Products line, referred to as the SP line, covers perhaps the widest choice of active elements, both transistors and diodes, ranging from simple diode arrays to multiple-transistor Darlington amplifier configurations in TO-5 or TO-18 cans. Resistors are also included in some circuit configurations. Fairchild uses the "Island" approach and, to the best of this author's knowledge, is the only vendor to employ this technique. The range of elements and configurations offered by Fairchild are too numerous to be covered here, and so the reader is referred to reference 2 at the end of this appendix for additional information.

B.2 GENERAL INSTRUMENTS NANOCIRCUITS LINE

To date, the author has seen three specification sheets on digital circuits offered by General Instruments under the tradename of Nanocircuits. The General Instruments approach has been to mount individual components, namely diodes, transistors, resistors, and capacitors on ceramic substrates which serve as microminiature printed circuit boards, with leads attached.[1]

The NC-8C Flip-Flop

Figure B.1 shows the circuit of this flip-flop which operates over a temperature range of $-55°C$ to $+125°C$. Planar-passivated epitaxial microtransistors and microdiodes, as well as planar passivated resistors, are used.

General Instruments indicates the following typical nominal design values for this circuit at 25°C with $V_{CC} = +8$ v, $V_{\text{clamp}} = +3.2$ v:

Logic levels	+0.3 and +4 volts
Maximum output current	2.5 ma at +4 volts
Maximum power dissipation	85 mw
Minimum input pulse amplitude	3 volts
Minimum input pulse width	25 nanosec
Maximum repetition rate	20 mc
Maximum fan-out	5
Output rise time	30 nanosec
Output fall time	20 nanosec

The NC-9 Flip-Flop Steering Gate

The steering-gate circuit shown in Fig. B.2 is intended for triggering the NC-8C flip-flop. Nominal design values at 25°C for this circuit are given as follows:

Minimum input pulse amplitude	= −3 volts
Minimum pulse width	= 25 nanosec
Maximum repetition rate (binary operation)	= 20 mc

The NC-10 NOR Gate

This is a saturated inverter gate with a fan-in of 3 and provision for additional fan-ins by means of an externally available node point. A clamped output is provided for defining the output level. Figure B.3 shows the circuit.

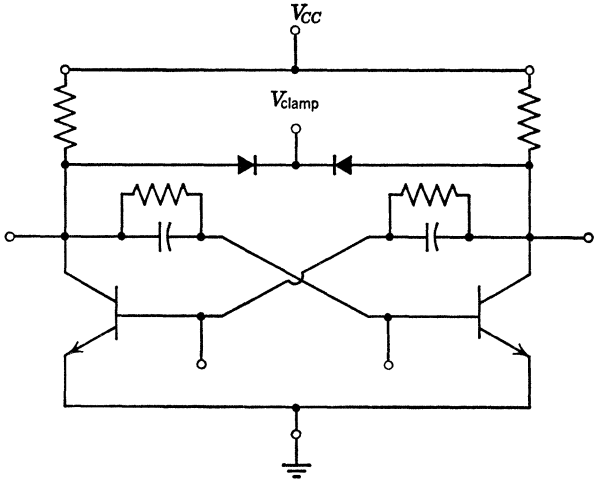

Fig. B.1 General Instrument's NC-8C flip-flop.

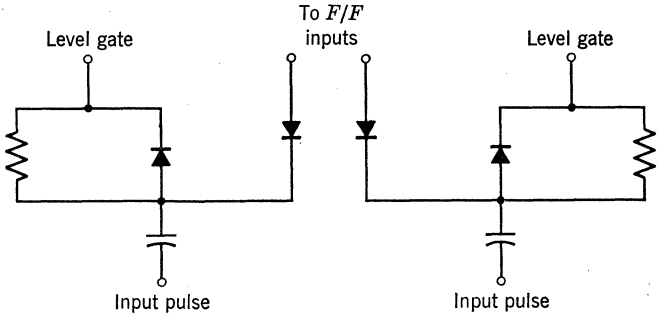

Fig. B.2 The NC-9 flip-flop steering gate.

The following typical nominal values at 25°C are given for this circuit with $V_{CC} = +8$ v, $V_{\text{clamp}} = +3.2$ v:

Maximum output current	= 3.5 ma at 4 volts
Logic levels	= −0.3 and +4 volts
Minimum pulse width	= 25 nanosec
Minimum input pulse amplitude	= +3 volts
Maximum power dissipation	= 70 mw
Maximum repetition rate	= 20 mc
Propagation delay	= 8 nanosec
Maximum fan-out	= 6 similar gates
Output rise time*	= 15 nanosec
Output fall time*	= 18 nanosec

* When driving NC-9 gate loaded with NC-8C flip-flop

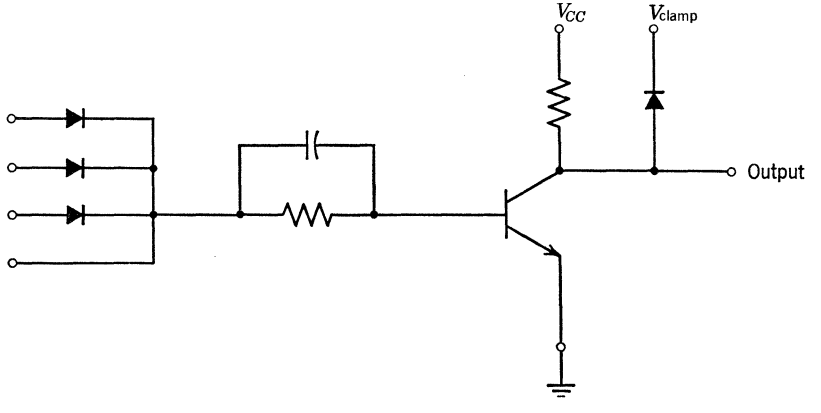

Fig. B.3 The NC-10 NOR gate.

B.3 MOTOROLA CHIP CIRCUITS

Currently, Motorola uses the partially integrated method for circuits on a custom basis. The previously described approaches of individual chips on TO-5 header and multiple ceramic discs in TO-5 cans are extensively used by Motorola. While Motorola does not presently have a standard product line using any of these approaches, they have produced several units to customers' special requirements. The circuits produced by Motorola are varied and range from simple logic gates and flip-flops to audio-amplifiers and sense-amplifiers for thin-film memories. Some of the typical components used by Motorola for this approach are:

1. Diffused resistors, 10 ohms to 30 kilohms, with temperature coefficient of 1000 ppm and power rating of 300 mw, and $\pm 10\%$ tolerance.
2. Junction capacitors of up to 500 pf at 10 volts, with tolerance of $\pm 10\%$.
3. Zener diodes of typical range 6 to 30 volts and 500 mw maximum power.
4. Standard Motorola diodes with typical speeds of 2 nanosec and 10 ma current at 1 volt.
5. Standard Motorola *NPN* high-frequency transistors with typical gain-bandwidth of 800 mc and current range of 0.01 to 10 ma.
6. Standard Motorola Star *NPN* transistors with typical gain-bandwidth of 400 mc and current range of 0.1 to 500 ma.

REFERENCE

1. *A Microminiature Flip-Flop Circuit,* Semiconductor Division, General Instruments Corporation, Hicksville, New York.
2. *"Special Products" Brochure,* Fairchild Semiconductor.

Appendix C
Product-line circuits using semiconductor thin-film hybrid-integration

C.1 THE PHILCO μ7000 LINE

Quite recently Philco announced availability of two logic circuits employing the hybrid thin-film semiconductor techniques in sample quantities. These circuits use silicon epitaxial transistors.

The μ7004 3-Input NOR Circuit

This unit consists of a 3-input resistor-transistor-logic type NOR circuit (Fig. C.1). The circuit is packaged in an 8-lead TO-5 can and has a fan-out of 3 over the temperature range of $-25°C$ to $+100°C$. A maximum turn-on time and turn-off time of 170 nanosec each is mentioned by Philco. The power dissipation is 110 mw at 100°C.

The μ7005 Flip-Flop Circuit

This is a set/reset type flip-flop using resistor-transistor-logic. Each output is intended to have a fan-out of 2 that is capable of driving two μ7004 RTL-NOR gates or two flip-flops over a temperature range of $-25°C$ to $+100°C$. The power dissipation at $+100°C$ is 100 mw. The turn-on time is a maximum of 50 nanosec and the

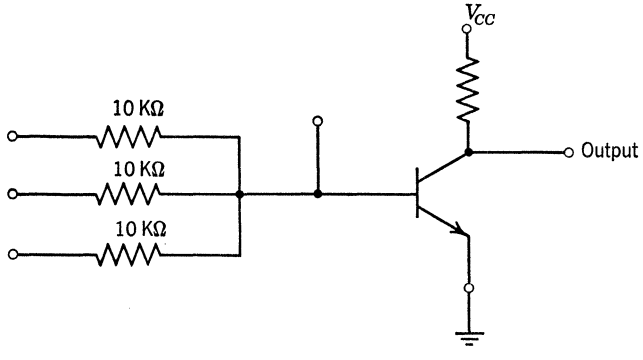

Fig. C.1 The Philco μ7004 NOR circuit.

maximum turn-off time is 160 nanosec for the set/reset configuration. The circuit is shown in Fig. C.2.

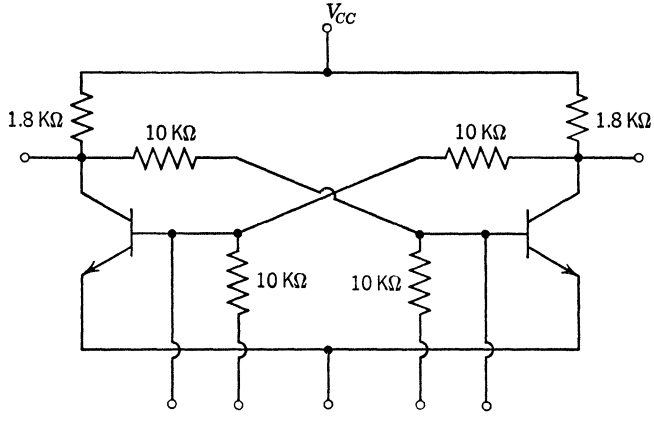

Fig. C.2 The Philco μ7005 set/reset flip-flop.

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