9140

DIGITAL COMPUTER

GENERAL DESCRIPTION

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9140 COMPUTER

GENERAL DESCRIPTION

I. INTRODUCTION

The 9140 Computer is a general purpose, stored program, real-time digital processor. It uses binary notation, is word organized, and operates with two's complement additive arithmetic. Input/output data transfers are buffered, and the computer also includes a communications multiplexer interface for buffered operations with communications devices. All memory locations are directly addressable and may be used for storage of data or instructions.

The 9140 Computer may be operated in any office type environment, and it does not require any special preparations for installation. The physical and functional characteristics of the 9140 Computer are described in the following section of this manual.

9140 COMPUTER FEATURES

- 24 BIT WORD LENGTH, 8 BIT CHARACTER INSTRUCTIONS
- THREE FAST INDEX REGISTERS
- INDIRECT ADDRESSING
- AVERAGE INSTRUCTION TIME OF 1.2 MICROSECONDS
- 0.75 MICROSECOND MEMORY CYCLE TIME
- BUFFERED I/O - OVER 3 MILLION CHARACTERS PER SECOND
- BUFFERED COMMUNICATIONS I/O
- EXTERNAL AND INTERNAL PROGRAM INTERRUPTS
- MEMORY PROTECTION FEATURE
- OPTIONAL ARITHMETIC AND CONTROL UNITS
- UPWARD PROGRAM COMPATIBLE FROM CONUS 24

II. PHYSICAL CHARACTERISTICS

The 9140 Computer, including all logic, memory, input/output channels, power supplies, and operator panel, is mounted in a single cabinet approximately 50 inches by 25 inches and 48 inches in height. Thus, the computer requires slightly over eight square feet of floor area. All wiring (power and peripheral data cables) may be brought out through the side of the cabinet at the floor level or through the bottom of the cabinet if the computer is to be used where a false floor is required or desired for other equipments.

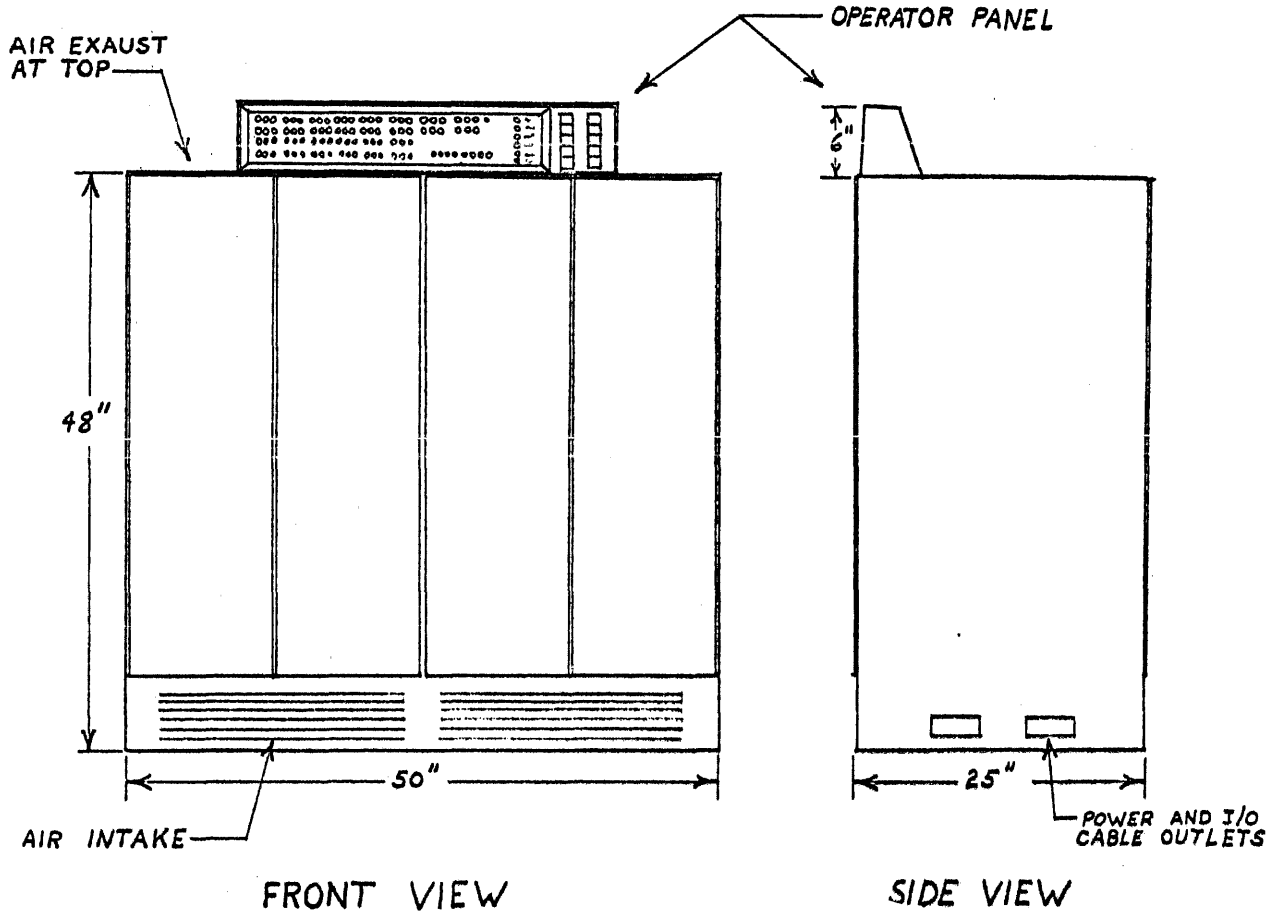
Figure 1 is a diagram of the 9140 Computer. The 9140 Computer uses forced room air for cooling and dissipates from 1,500 watts to 2,500 watts, depending upon the memory size, type of arithmetic and control unit used, and the number of input/output channels included. The front and rear doors of the computer cabinet are hinged at the sides and swing open to allow easy access to the blower, air filter, power supply, logic, and memory.

The operator panel is at a convenient height for use by an adult person, the center of the controls being approximately 51 inches from the floor. The operator panel indicators and controls are displayed on a black background, and the center portion of the panel is recessed slightly so that the neon indicators may be seen easily in high ambient light areas.

The 9140 Computer requires between 1,500 and 2,500 watts of 105-125 volt AC single phase electrical power for operation. The exact power requirements depend upon the memory, input/output, and logic options selected. The computer will operate satisfactorily in any environment suitable for office personnel.

FIGURE 1

9140 COMPUTER



III. FUNCTIONAL DESCRIPTION

The 9140 Computer has a minimum memory size of 8,192 - 24 bit words, expandable in 8,192 word increments to a maximum of 65,536 words. Figure 2 shows the relationships between word and eight bit characters in terms of the memory sizes offered.

FIGURE 2

MEMORY OPTIONS

Functional Unit Size	Minimum Size Offered	Incremental Size Offered	Maximum Size Offered
24 bit word	8,192	8,192	65,536
8 level character	24,576	24,576	196,608

Memory modules may be added to an existing installation as a field modification.

Input/Output

The basic 9140 Computer contains as standard features, four input and four output (a total of eight) fully buffered general purpose high speed channels, each capable of transmitting up to 24 bits or three, eight level characters in parallel. The maximum input or output rate allowable with any peripheral device depends on system constraints such as the number of peripheral devices which must operate concurrently. The maximum computer buffered data transfer rate, input and output, can exceed one million 24 bit words per second or over three million eight level characters per second. Normally, with concurrent processing and input/output, the average data transfer rate will be much lower.

The number of possible buffer control words is not limited by the number of input/output channels. The basic 9140 Computer Input/Output section contains fourteen address lines such that communications type peripheral equipments may specify the buffer control word addresses to be used. This feature permits automatic sorting and buffering of communications data between the 9140 Computer memory and a large number of communications facilities by use of the UNIVAC Standard Communications Subsystem.

Three additional sets of eight high speed channels (four for input and four for output), each set including an additional group of address lines, may be ordered as optional equipment and can be installed in a 9140 Computer in the field.

Buffered input/output word transfers may take one, two, or three memory cycles depending on how the transistor buffer control registers are assigned to I/O operations.

Instruction Operation

The average instruction execution time of the 9140 Computer depends on the individual program being run. The instruction times, including all memory references normally vary from a minimum of 0.75 microsecond to a maximum of 2.25 microseconds in the basic 9140 Processor. An average of 1.2 microseconds per instruction may be expected with most programs.

Figure 3 is a simplified block diagram of the 9140 Computer. The registers are identified by capital letters. One of the optional arithmetic and control units is shown in Figure 3. The operation of this optional unit is described in a separate manual. The following description of the functions of each of the registers will aid in understanding the operation of the basic 9140 Computer.

Description of Registers

S - Storage Address Register. The S Register is sixteen bits in length and is used to hold the address of the particular memory location being accessed during the memory read/write cycle. This register is displayed on the operator panel and its contents may be manually altered except when the computer is operating at high speed.

Z - Memory Data Register. The Z Register is twenty-four bits in length and, in general, is used to receive and hold the data read out of the memory cell whose address is held in the S Register. The Z, or data register, is displayed on the operator panel and its contents may be altered manually except when the computer is operating at high speed.

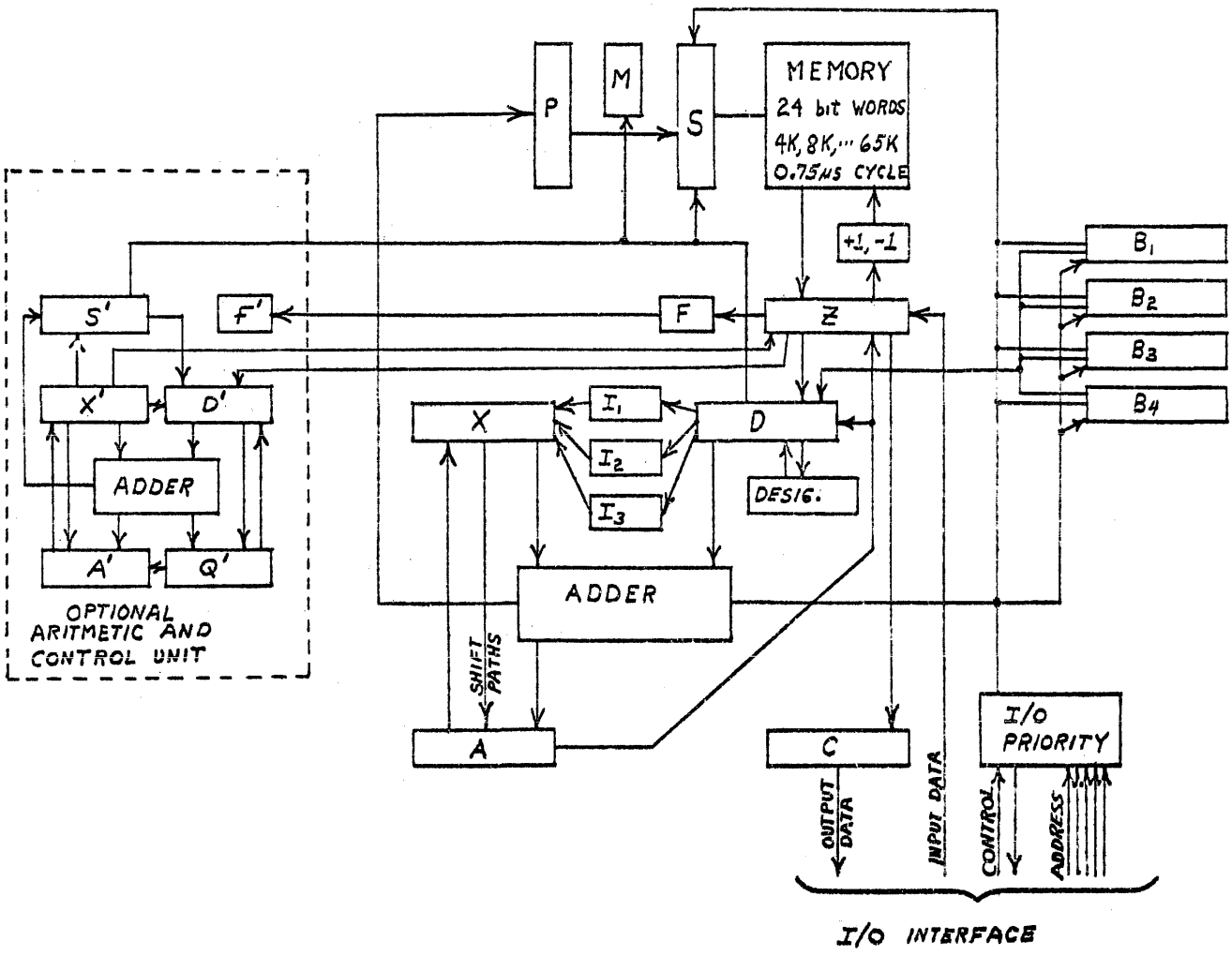
X - Auxiliary Register. The X Register is twenty-four bits in length and is used as an auxiliary arithmetic register and data register. During adder operations, the contents of the X Register are automatically added to the contents of the D Register.

F - Function Register. The F Register is eight bits in length. It is used to indicate the instruction being executed and it holds the operation or function code and instruction designators while they are being decoded and executed. The F Register is displayed on the operator panel to aid in program debugging.

C - Output Register. The C Register is twenty-four bits in length and is used to hold data which is to be transmitted to peripheral devices so that the computer can proceed with other operations simultaneously with the transmission of data to slower speed peripheral devices. This register is provided because many peripherals cannot accept data during the short memory reference time when it is offered.

FIGURE 3

TENTATIVE 9140 COMPUTER BLOCK DIAGRAM



A - Accumulator Register. The A Register is twenty-four bits in length. It is normally used to hold the results of arithmetic and logical operations between instructions. The A Register is explicitly addressable by most instructions by setting Y = 1. The A Register is implicitly addressed and automatically accessed by those instructions which specify its use. The A Register is displayed on the operator panel as an aid for progrm debugging.

P - Program Address Register. The P Register is a sixteen bit register. The P Register holds the address of the next instruction to be executed and it may be explicitly addressed in most instructions by setting Y = 0. The P Register is accessed automatically during the operation of the computer for the purposes of incrementing and obtaining the addresses of instructions to be executed. The P Register is displayed on the operator panel.

D - Auxiliary Arithmetic and Data Transfer Register. The twenty-four bit D Register is used to hold information presented to the adder. It is also used to transmit data to the index registers.

B_1, B_2, B_3, B_4 - Buffer Control Registers. Four twenty-four bit buffer control registers are provided outside of memory for use with very fast peripheral devices. These registers hold the word counts and/or data addresses during input/output operations. Core memory locations may also be used for buffer control word storage.

I_1, I_2, I_3 - Index Registers. Three eighteen bit index registers are used to hold information which can be automatically added to the y portion of each instruction before the instruction is executed.

M - Memory Protect Register. During the execution of instructions, the contents of the S Register is compared to the contents of the 8 bit M register. During instruction operations which alter the contents of operand memory locations, the alteration is only allowed if the upper bits of the address falls within the range specified by the contents of the M register. Where bits of M are set to ones, the corresponding upper bits of S must remain invarient during operand memory write cycles. Should the value in S be outside of the range specified by M, a MEMORY PROTECT INTERRUPT will occur.

Other Functions

Other functions shown in the block diagram include the input/output priority network, adder, and the memory incrementing/decrementing logic.

Adder - The adder is a parallel, two's complement twenty-four bit additive unit which adds two twenty-four bit numbers (the contents of D and X) and provides a twenty-four bit sum which is normally placed in the A Register.

Input/Output Priority - The I/O Priority network determines the next input/output function to be performed and insures that all requested I/O operations are noted and processed in an orderly manner.

Memory Incrementing/Decrementing Logic - An adder is used between the memory read and write cycles during certain instructions which require a memory location to be incremented or decremented. This unit is also used during input/output data transfers if memory contained buffer control words are accessed.

General Theory of Instruction Operation

The accessing and execution of instructions are in the form of successive sequences which are wired into the computer. Each sequence normally involves a memory reference (read/write cycle), and the duration of a sequence normally coincides with the duration of the memory cycle. The following description applies to most of the instructions.

Instructions begin with an A sequence. This sequence increments the contents of the P Register, extracts the instruction to be executed from memory, and restores the instruction in memory. During the last half of the A sequence, the function ordered by the instruction is decoded along with the indirect and index register designators in the instruction. If the indirect designator is zero, certain of the instructions may be completed during the A sequence such as LOAD, CONSTANT, JUMP, SKIP, and some I/O functions. If the use of an index register is required, the contents of the appropriate index register is added to the y portion of the instruction during the A sequence.

If the i designator in the instruction is set to one, the next sequence in order of execution is the indirect (I) sequence. This sequence places the fifteen bit address portion of the instruction (or the address obtained in the index register modification) into the S Register. The data at this address is then read from memory and restored to memory. This data becomes the effective operand address unless the binary position in this word corresponding to the i designator in this word is set to a one, the index modification and Indirect (I) sequence is repeated according to the b and i designator settings in this new word. When the i designator is found to be zero, the I sequences terminate.

The next sequence in the instruction cycle is a Y sequence. If the contents of the accumulator are to be placed at a storage location, the Y sequence is used to place this data at the address Y. If the program has set Y = 1, the contents of the Accumulator will be accessed and a Y sequence will not be used. If the contents of a memory location are to be decremented or incremented, the operation is performed by the incrementing/decrementing logic during the operand memory cycle. In these cases, the memory cycle is extended by approximately 100 nanoseconds to allow sufficient time for this modification to occur between the read and write portion of the memory cycle.

In summary, the sequences are as follows:

A - Determines the address of the next instruction, calls the instruction from memory, and adds the index register contents to the instruction address to obtain the operand address.

I - Uses the operand address to obtain the effective address of the operand. This sequence may be repeated.

Y - Extracts and/or modifies the operand.

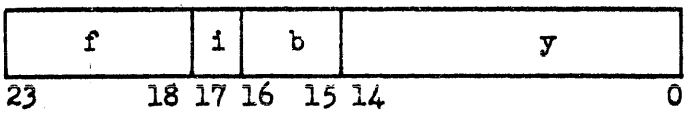
The A sequence is always used in the instruction. The I sequence is used if the corresponding designator is set and can be repeated. The Y sequence is used as necessary. The average number of sequences of memory cycles used in an average instruction would be between one and two.

IV. PROGRAMMING CHARACTERISTICS

The 9140 Computer instructions are twenty-four binary digits in length, and each instruction is contained in a single word in the computer memory. The instructions consist of a six bit function code which defines the operation to be performed, a one bit indirect addressing designator, a two bit index register designator, and a fifteen bit operand address designator. Figure 4 shows the instruction word format.

FIGURE 4

INSTRUCTION WORD FORMAT



f = function or operation code = 6 bits
i = indirect addressing designator = 1 bit
b = index register (one of three) designator = 2 bits
y = operand address designator = 15 bits

The 9140 Computer instructions are as shown in Table 5.

TABLE 5

9140 INSTRUCTION REPERTOIRE

NAME	OPERATION	NORMAL EXECUTION TIME IN MICROSECONDS
STOP	Computer stops	0.75
STORE STATUS	Store all designators at y	1.50
LOAD STATUS	Load all designators from y	1.50
EXECUTE REMOTE	$(P_{0-15}) \longrightarrow Y_{0-15}$, Execute Y + 1	1.50
EXECUTE	$(P_{0-15}) \longrightarrow Y_{0-15}$, Y P	1.50
MASK SKIP	Sense Y, Conditionals Skip NI	1.50
JUMP	$Y \longrightarrow P$	0.75
LOCKOUT	$Y_0 \longrightarrow$ Lock Designator	0.75
ADD	$(A) + (Y) \longrightarrow A$	1.50
SUBTRACT	$(A) - (Y) \longrightarrow A$	1.50
AND	$(A) \odot (Y) \longrightarrow A$	1.50
EXCL. DR	$(A) \bar{\oplus} (Y) \longrightarrow A$	1.50
STORE B	$(B)_b \longrightarrow Y$	1.50
LOAD B	$(Y) \longrightarrow B_b$	1.50
LOAD A	$(Y) \longrightarrow A$	1.50
LOAD CHAR. 1	$(Y_{0...7}) \longrightarrow A_{0...7}$	1.50
LOAD CHAR. 2	$(Y_{8-15}) \longrightarrow A_{0-7}$	1.50
LOAD CHAR. 3	$(Y_{16-23}) \longrightarrow A_{0-7}$	1.50
STORE A	$(A) \longrightarrow Y$	1.50
STORE CHAR. 1	$(A_{0...7}) \longrightarrow Y_{0...7}$	1.50
STORE CHAR. 2	$(A_{0...7}) \longrightarrow Y_{8-15}$	1.50
STORE CHAR. 3	$(A_{0...7}) \longrightarrow Y_{16-23}$	1.50

NAME	OPERATION	NORMAL EXECUTION TIME IN MICROSECONDS
INCREMENT	(Y) + 1⟶Y	1.60
LOAD CONSTANT	Y⟶A	0.75
INDEX SKIP	(Y) - 1⟶Y, Skip NI if $(Y)_f < 0$	1.60
STORE ADDRESS	$(A_0 \ldots 15) \longrightarrow Y_{0 \ldots 15}$	1.50
CHARACTER SHIFT	(Y) Left Circular 8 bits	1.60
SHIFT RIGHT	(A) Right open Y bits	0.75 + K (0.1)
SHIFT LEFT	(A) Left open Y bits	0.75 + K (0.1)
PARITY	Set designators	0.75
ESCAPE*	Define the instruction set and optional arithmetic unit designated by Y	0.75
ACTIVATE I/O	Activate Channel Y	0.75
EXTERNAL FUNCTION	(A)⟶Channel Y	0.75
STORE REMOTE	ESI or Channel Y data⟶A	0.75
MEMORY PROTECT	Y⟶M	0.75

The use of indirect addressing adds 0.75 microseconds to each instruction execution time per each indirect cycle executed. The use of the index registers does not add any additional instruction execution time.

*
This instruction selects the set of instructions which are used in conjunction with the optional arithmetic and control unit. Up to approximately 20 additional instructions may be defined for each of the optional units. Once selected, this instruction does not have to be used again until a different optional arithmetic and control section is to be activated.

The instruction repertoire for the 9140 Computer has been designed to allow easy programming of basic arithmetic, logical, and business decision operations. By storing each instruction in a 24 bit word, optimum use of the storage for instructions is realized, as there are no wasted bit positions. The use of eight level characters for alpha and numeric information provides compatibility with all common computer character codes. The ability of the 9140 Computer to address characters in groups of three (three 8 level characters per word) provides very fast operation. Note that certain instructions are provided for operating on single characters in each group of three.

The 9140 Computer can directly address 32,768 words of storage and allow indirect addressing and indexing even with its short instruction. This ability makes software much easier to write, faster, and does not introduce a great number of programming restrictions. Since all instructions are short, and since the status of the designators may be stored and loaded with a single pair of instructions, the handling of real-time interrupts can be extremely rapid, and interrupts need not be deferred for long times. This allows the 9140 Computer to handle real-time operations extremely fast.

The basic 9140 Computer instruction repertoire was designed using statistical "frequency of use" tables compiled from business, real-time, and information retrieval and storage programs in use on various other computers. Single, double, and triple address computers were studied as well as decimal and binary types of machines. The 9140 Computer, for its functional size, represents an optimum solution for batch business, real-time, and information storage and retrieval problems. Instructions which are very seldom used or needed may be programmed easily using the basic instructions provided. For applications requiring extensive scientific computation or multiword operations, the appropriate optional arithmetic and control unit may be added to the basic 9140 Computer to make an efficient application oriented processor.

Input and output

The basic 9140 Computer contains four general purpose high speed input channels and four general purpose high speed output channels. In addition, a set of address lines is provided for multiplexing a number of peripherals on to one of the high speed input and output channels.

Input/output data transfers are normally carried on by the memory of the 9140 Computer and the peripheral device in such a way that the computer program is not logically interrupted. The input/output logic operates by temporarily suspending the program for one, two, or three memory cycles during which time one twenty-four bit word is transferred to or from the peripheral device and the memory.

The 9140 Computer memory and I/O logic also monitors and controls the number of words to be transferred, the memory addresses involved, and the conditions under which the transfer of data is automatically stopped. No provisions need be made in the writing of programs for individual buffered I/O word transfers. They have no effect upon the program logic except to slow the running of the program slightly and to interrupt the program after the proper number of words have been transferred.

The rate of data word transfers between peripheral equipments and the 9140 Computer are governed by the transfer rate of the peripheral devices if they are slower than the 9140 Computer and by the 9140 Computer if they are faster.

All of the 9140 input and output channels may be active concurrently. Through the use of the address lines provided and a communications multiplexer, the number of active input and output data word buffers is limited only by the number of peripheral devices which are required and the total data transfer rate which the 9140 Computer can handle from all of the peripheral devices combined.

Buffer Control Words

The 9140 Computer requires two twenty-four bit words for each buffer operation to be established. These words are loaded initially by the program. They are then placed under control of the input/output logic for the duration of the time during which the transfers will take place. The first word associated with a buffered transfer initially holds the count of the total number of data words to be transferred. The second word holds the address of the memory cell into which the first data word is to be placed (input), or the address of where the first output data word is to be obtained from (output). The word count is decremented and the data address is incremented automatically during each data transfer by the Input/Output logic. When the count reaches zero, a monitor interrupt is generated to inform the program that the number of words called for has been transferred. At the same time, the input/output logic also deactivates the channel. The procedure to initiate a buffered transfer of N words is as follows:

1. The program loads the count location for the desired channel with the number of words N.

2 The program loads the address location for the same channel with the first data storage address to be involved in the data transfer.

3. The program executes an EXTERNAL FUNCTION instruction which directs the peripheral device to begin operation.

4. The program executes an ACTIVATE I/O instruction which transfers control of the buffer control words to the input/output logic of the channel involved. The actual transfer of data words to or from the 9140 Computer and the peripheral device then proceeds logically independent of the program. When all of the words have been transferred, a monitor interrupt will occur. This monitor interrupt will cause the computer to execute an instruction in a memory location permenently associated with the channel through which the data transfers took place. This has the effect of logically interrupting the program. Interrupts may be locked out by use of the LOCKOUT instruction which is normally used only when transferring control from one program to another under executive program control.

The buffered sequence for the transfer of a single word to or from the 9140 Computer and a peripheral device is as follows:

1. The peripheral device sends the request to the computer.

2. The computer suspends the execution of the next instruction temporarily for the next one, two, or three memory cycles.

3. The count is read out of the buffer control word location and restored decremented. If the count restored is zero, the logic for generating a monitor interrupt is activated. The transfer, however, continues in either case.

4. The data address is read out of the second buffer word location and incremented. This data address, before incrementation, is saved for the data memory cycle.

5. The data presented by the peripheral device is placed in memory at the data address (input), or the data at the address in memory is sent to the peripheral device (output). This data transfer cycle is the last operation in the buffered sequence.

6. The program automatically resumes where it was suspended and the next instruction is executed, etc.

The program will continue to run without any suspension or time interruption until the next request is received from a peripheral device.

In addition to the locations in core memory which may be used for buffer control word storage, four transistor registers are provided. These registers may be used in place of the memory contained words such that three different buffered I/O word transfer rates are possible. For example, if two of these B Registers are assigned to a

given input channel, only one memory cycle is required per input word transfer on that channel. If one B Register is assigned to a given channel, two memory cycles will be required for a single data word transfer on that channel, as the other buffer control word used will be in core memory. If none of the B Registers are assigned to a given channel, a buffered word transfer will take three memory cycles, because both of the buffer control words will be in core memory.

The four B Registers may be assigned as desired among the four I/O channels in the basic 9140 Computer as a factory option.

Arithmetic and Control Unit Interface

The 9140 Computer is designed such that it may have additional processing power added to it in the form of optional arithmetic and control units. A generalized high speed logical interface is provided such that arithmetic and control units tailored for specific applications may be used to optimize the processor for specific types of applications.

For example, a multiword operation unit may be used to provide multiword edits, compares, data moves, and BCD arithmetic. These operations may be suspended temporarily when a real-time interrupt occurs without locking out interrupts for long periods of time or storing intermediate batch processing results. In addition, long batch operations are automatically suspended for one, two, or three memory cycles to allow I/O data word transfers to occur.

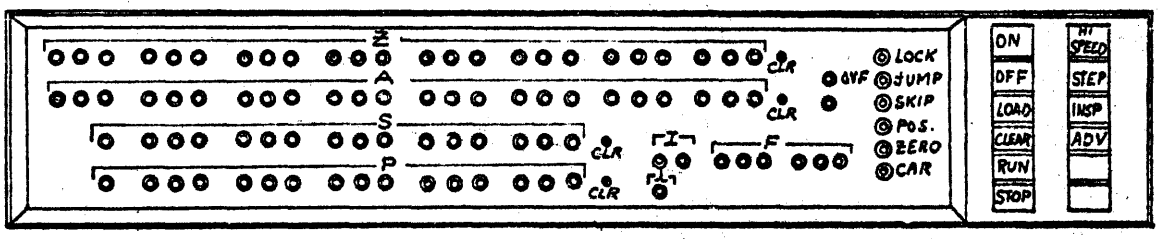
VI. OPERATOR PANEL

The operator panel on the 9140 Computer is used to start and stop the computer, enter a limited amount of information, display the contents of any memory location, aid in program debugging, and facilitate maintenance when it is required.

The layout of the operator panel is shown in Figure 6.

FIGURE 6

OPERATOR PANEL



Power is applied to the 9140 Computer by depressing the ON switch. The switch lights when power is applied. If the OFF switch is depressed, the ON switch will become dark and power is removed. The procedure to start the 9140 Computer, high speed, is as follows: 1) With the computer on, depress the CLEAR switch which master clears the computer. 2) Depress the HI SPEED switch which readies the computer for high speed operation. 3) Depress the LOAD switch. Depressing the LOAD switch conditions the compuer to accept a program starting address. 4) Enter the starting address of the program into the P Register. If a mistake is made, the register may be cleared by means of the small clear button to the right of the register. Finally, depress the RUN switch. The computer will indicate a stop by extinguishing the RUN indicator and lighting the STOP indicator.

In order to inspect any memory location and enter data or instructions directly into the 9140 Computer Memory, the CLEAR switch should be depressed and the INSPECT switch should be depressed.

Next, the LOAD switch should be depressed. This will prepare the computer to accept the first address to be inspected. The address

to be inspected should then be loaded into the Z Register. When The RUN switch is depressed, the manually inserted address will be transferred to the S Register, and the information at that address in core memory will be displayed in the Z Register. This information may be cleared out by means of the small clear button to the right of the Z register, and new information may be entered into this memory location by depressing the appropriate bit position indicator switches.

In order to inspect the next consecutive address, the ADVANCE switch should be depressed. The computer will then automatically increment the address displayed in the S Register by one and will display the contents of this new memory location in the Z Register

If a different address, not in sequence, is to be inspected, the STOP, CLEAR, and LOAD switches should be depressed again. The new address may then be entered into the S Register, and the computer may be started as before.

Step operation allows slow speed operation of a program in such a way that one instruction is executed each time that the ADVANCE switch is depressed. The 9140 Computer should be placed into the STEP mode in order to operate at slow speed. This is accomplished by depressing the CLEAR switch, followed by depressing STEP switch. The LOAD switch should then be depressed, and the starting address is entered into the P Register. The computer is then started by depressing the RUN switch. Each time that the ADVANCE switch is depressed, the 9140 Computer will execute one instruction. The Z Register and S Register will display the results of the last memory reference in the instruction just executed. The function code will be displayed in the Function Register, and the appropriate designator settings will also be displayed.

If peripheral devices are active and an I/O data transfer takes place following the instruction in the STEP mode, the last memory reference of the input or output transfer, data and address will be displayed in the Z and S Registers, respectively.

If the switches on the Operator Panel are not depressed in the correct sequence, or if they are depressed accidentally during high speed operation, no harm will result to the electrical components. Some of the program or data stored in memory may be destroyed, however, and it may be necessary to reload the mutilated information either manually or via the bootstrap program and data stored in a peripheral device such as a card reader.

The following indicators, in addition to the Z, S, and P Registers are displayed on the operator console.

A - the 24 bit accumulator register.

LOCK - indicates if the I/O Interrupt Lockout is set.

JP - indicates if a jump instruction has been executed or if the computer is conditioned to accept a starting address.

SKIP - the skip indicator indicates if a skip instruction has been executed, and the skip will be performed.

POS - the positive designator is set during certain instructions and is sensed by the SKIP instruction.

ZERO - the zero designator is set during certain instructions and is sensed by the SKIP instruction.

CAR - the carry designator is set during certain instructions when an adder carry occurs and it is sensed by use of the SKIP instruction.

OVF - the overflow designator is set during certain arithmetic instructions when adder overflow occurs. It is sensed by use of the SKIP instruction.

The neon indicators on the recessed portion of the Operator Panel indicate correctly only when they are set to one state over a long period of time or when the computer is in the INSPECT or STEP modes or when the computer is stopped. When the computer is operating at high speed, indications normally change at a rate too high for the neon indicators or eye to follow, and any indications during high speed operation are normally not useful. Possible exceptions are operations where the computer is waiting most of the time and is operation very slow speed peripherals only.

Other registers, including I/O active designators, etc., are displayed inside the 9140 cabinet for maintenance purposes.