SPERRY RAND

UNIVAC
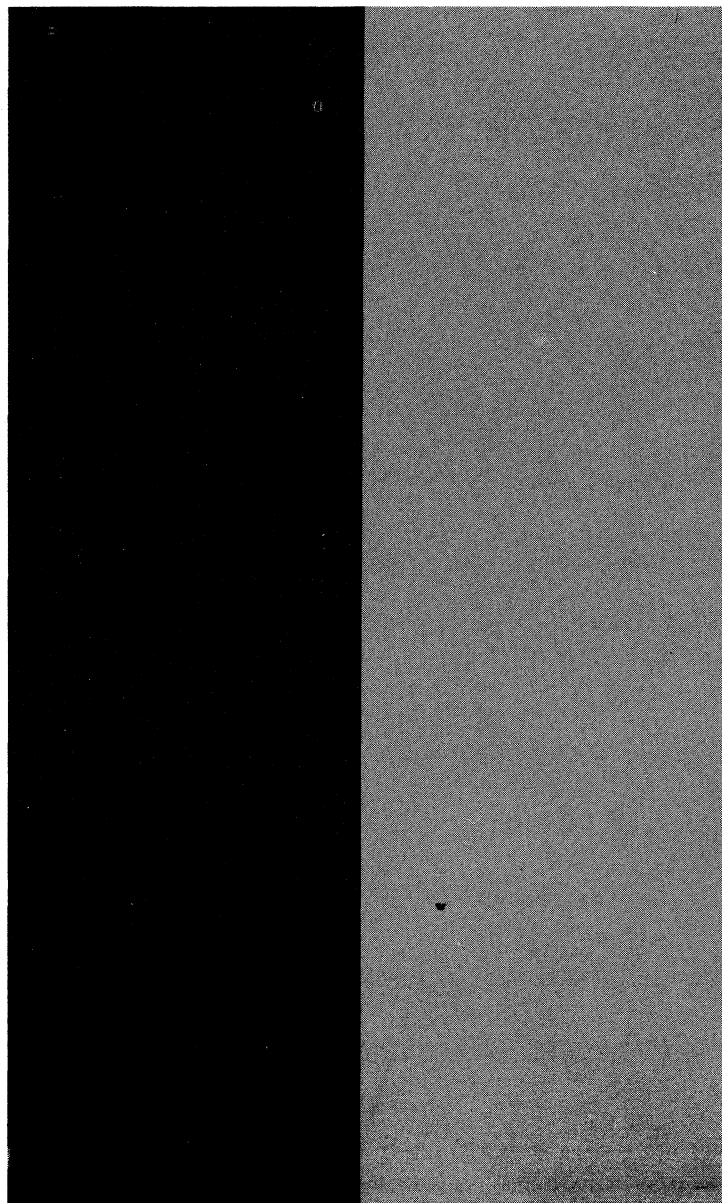# 1106 SYSTEM
1108 MULTI-PROCESSOR SYSTEM
CENTRAL GROUP

OPERATOR
REFERENCE

This document contains the latest information available at the time of publication. However, the Univac Division reserves the right to modify or revise its contents. To ensure that you have the most recent information, contact your local Univac Representative.

UNIVAC is a registered trademark of the Sperry Rand Corporation.

Other trademarks of the Sperry Rand Corporation in this publication are:

UNISCOPE
UNISERVO
FASTRAND
PAGEWRITER

PAGE STATUS SUMMARY

ISSUE: UP-7947

The following table lists the status of each page in this document and indicates the update package (if applicable).

Section	Page Number	Page Status	Update Package	Section	Page Number	Page Status	Update Package
Cover/Disclaimer		Orig.					
PSS		Orig.					
Contents	1, 2	Orig.					
1	1 thru 3	Orig.					
2	1	Orig.					
3	1 thru 26	Orig.					
4	1 thru 3	Orig.					

7947
UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

Contents 1
PAGE

CONTENTS

7947
UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

Contents 2
PAGE

FIGURES

TABLES

I. INTRODUCTION

1.1. SCOPE

This manual contains the information and procedures required for operating the UNIVAC 1106/1108 Systems Central Group (central group).

Operator information for the various peripheral subsystems which may be used in a UNIVAC 1106 System or UNIVAC 1108 Multi-Processor System is provided in the following manuals:

UP-Number	Title
UP—7810	UNIVAC Communications Terminal Module Controller (CTMC) Subsystem Operator Reference
UP—7706	UNIVAC 1106/1108 Systems Communications Terminal Synchronous Programmer/Operator Reference
UP—7672	UNIVAC 1106/1108 Systems Word Terminal Synchronous Programmer/Operator Reference
UP—7832	UNIVAC DCT 500 Data Communications Terminal Operator Reference
UP—7827	UNIVAC DCT 1000 Data Communications Terminal Operator Reference
UP—7545	UNIVAC DCT 2000 Data Communications Terminal Operator Reference
UP—7788	UNISCOPE 100 Display Terminal Operator Reference
UP—7615	UNISCOPE 300 Visual Communications Terminal Operator Reference
UP—7514	UNIVAC 1108 System Input/Output Controller Programmer/Operator Reference
UP—7562	UNIVAC 1108 System Multiple Processor Adapter Programmer/Operator Reference
UP—7506 Rev.1	UNIVAC 1108 System Punched Card Subsystem Programmer/Operator Reference
UP—7509 Rev.1	UNIVAC 1108 System High Speed Printer Subsystem Types 0751/0755/0758 Programmer/Operator Reference
UP—4063	UNIVAC 1108 System UNISERVO VI-C Magnetic Tape Subsystem Programmer/Operator Reference

UP-Number	Title
UP—4123	UNIVAC 1108 System UNISERVO VIII-C Magnetic Tape Subsystem Programmer/Operator Reference
UP—7882	UNISERVO 12/16 Magnetic Tape Subsystems Operator Reference
UP—4094	UNIVAC 1108 System FH-432 Magnetic Drum Subsystem Programmer/Operator Reference
UP—7628	UNIVAC 1108 System FH-432/1782 Magnetic Drum Subsystem Programmer/Operator Reference
UP—7517	UNIVAC 1108 System FH-880 Magnetic Drum Subsystem Programmer/Operator Reference
UP—4083	UNIVAC 1108 System FASTRAND II Subsystem Programmer/Operator Reference
UP—7801	FASTRAND II/III Magnetic Drum Subsystem Operator Reference
UP—7802	UNIVAC 8411/8414 Direct Access Subsystem Operator Reference

1.2. SUBSYSTEM DESCRIPTION

The central group (Figure 1—1) provides the principal communication between the processor system and an operator. The group comprises the type 4009—99 display console and the central processor unit (CPU). A brief description of each device follows.

Figure 1—1. UNIVAC 1106/1108 Systems Central Group and CPU Maintenance Panel

1.2.1. Display Console

The display console is used by the operator to monitor and direct the operation of the CPU. The console is always connected to I/O channel 15. It consists of the operator's control panel, the keyboard and cathode ray tube (CRT) display, and a freestanding PAGEWRITER printer.

Additional equipment that can be mounted on the display console includes aa system emergency off switch, and a loudspeaker for program and fault alarms. Communications subsystem operator's control panels can be mounted on an optional auxiliary console.

1.2.2. CPU Maintenance Panel

The CPU maintenance panel is primarily used by the Univac customer engineer to control and monitor CPU operation during corrective maintenance of the system. The information given in the following paragraphs discusses the controls and indicators which are of significance to the operator.

2. OPERATOR'S RESPONSIBILITIES

2.1. GENERAL

The operator is responsible for the following:

■   turning on and turning off the equipment as required;

■   observing and responding to indications on the various operator control panels described in this manual; and

■   loading forms into the PAGEWRITER printer and changing the PAGEWRITER printer ribbon.

2.2. REQUIREMENTS

To assume these responsibilities, the operator should be familiar with the location and use of the controls and indicators, and with the operation of the equipment.

3. CONTROLS AND INDICATORS

3.1. GENERAL

This section contains a description of the controls and indicators of the display console and of the central processor unit (CPU) maintenance panel on the UNIVAC 1106/1108 Systems Central Group (central group).

3.2. DISPLAY CONSOLE

The controls and indicators for the display console are included on the following components:

■   Operator's control panel

■   Keyboard and cathode ray tube (CRT) display

■   PAGEWRITER printer

3.2.1. Operator's Control Panel

The operator's control panel (Figure 3—1) contains the controls, displays, and indicators used by the operator to monitor and control CPU operation. Table 3—1 lists the function of each control, indicator, and display. Items marked with an asterisk appear on both the operator's control panel and the CPU maintenance panel.
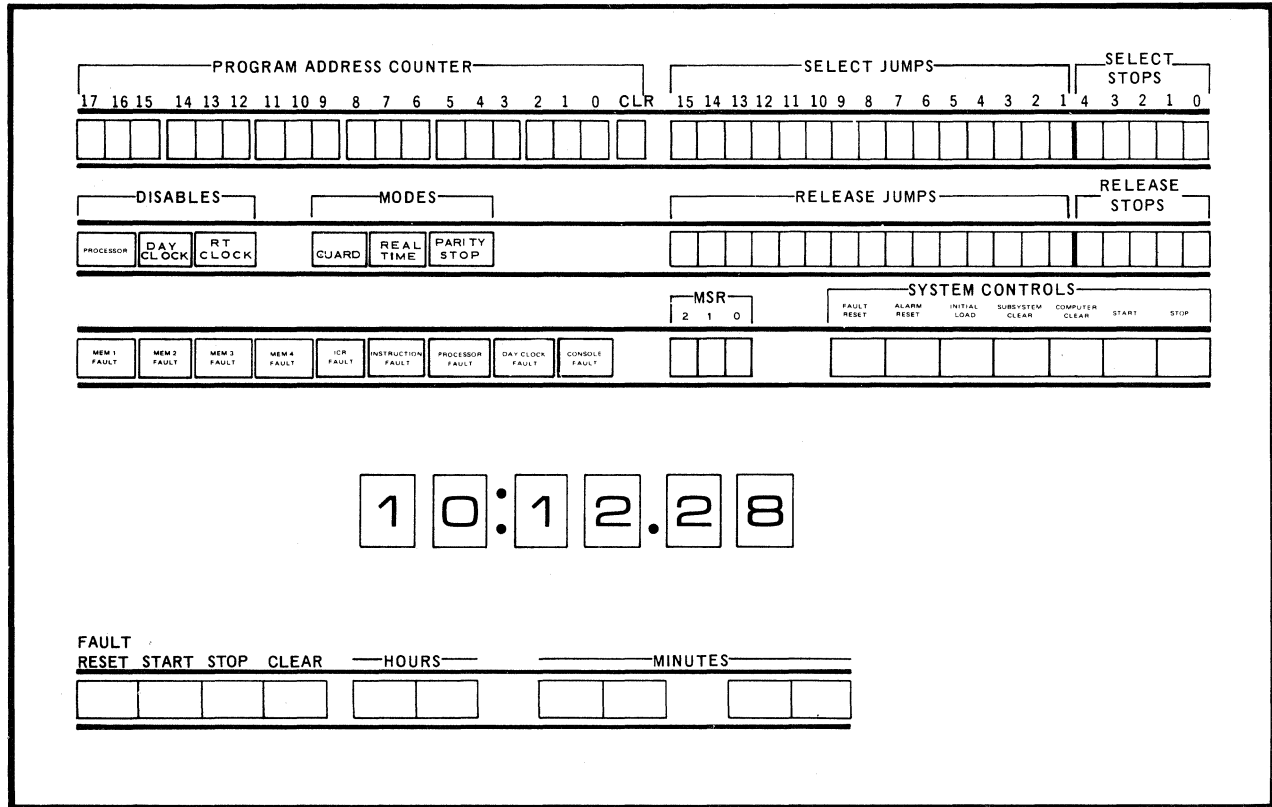
Figure 3—1. Operator's Control Panel

Control/Indicator	Function
PROGRAM ADDRESS COUNTER* (18 switch/indicators labeled 0 through 17) and CLR switch	Indicators display contents of program address counter (P-register), which holds address of next instruction to be executed. Switches can be used to alter contents of P-register. P-register is cleared to 0 when CLR switch is pressed. All switches and indicators are disabled when a program is running.
SELECT JUMPS* (15 switch/indicators labeled 1 through 15)	Used to vary program execution. Operates in conjunction with a jump-keys instruction. Pressing a SELECT JUMPS switch lights its indicator and enables corresponding jump when it is encountered in program. Programmer must inform operator which SELECT JUMPS switches are to be set for his program. Switches may be set during program execution.
SELECT STOPS* (5 switch/indicators labeled 0 through 4)	When lit, SELECT STOPS 0 indicates that a programmed unconditional stop has occurred. SELECT STOPS 1 through 4 operate in conjunction with a halt-keys-and-jump instruction. Pressing one of these switches lights its indicator and sets the conditional stop. When program halts (the a-field of instruction is 0 or equals bit configuration set with SELECT STOPS switches), corresponding RELEASE STOPS indicator lights. No stop occurs if CPU is in guard mode or real time mode, regardless of settings of SELECT STOPS switches. If CPU halts due to a conditional stop and real time mode is then set, RELEASE STOPS switches must be used to restart CPU. If the a-field of halt-keys-and-jump instruction does not equal setting of SELECT STOPS switches, or if it is not 0, or if the CPU is in guard or real time mode, program does not halt but immediately jumps to the jump-to-address specified in the instruction.

Table 3—1. Operator's Control Panel, Controls and Indicators (Part 1 of 3)

Control/Indicator	Function
DISABLES	
PROCESSOR indicator	When lit, indicates that a switch on the CPU or a main storage maintenance panel has been set to prevent normal operation.
DAY CLOCK* indicator	When lit, indicates that day clock request and interrupt lines have been disabled.
RT CLOCK* indicator	When lit, indicates that real time clock has been disabled.
MODES	
GUARD indicator	When lit, indicates that guard mode storage protection is active.
REAL TIME* indicator	When lit, indicates system is operating in real time mode. When lit, only the following switches are operative: SELECT JUMPS switches RELEASE JUMPS switches RELEASE STOPS switches Console keyboard and the eight interrupt keys
PARITY STOP* indicator	When lit, indicates that CPU will halt when a parity error is detected. This indicator is activated by STOP ON PARITY switch and is overridden by MEMORY FAULT INTERRUPT switch. (Both switches are located on CPU maintenance panel.)
RELEASE JUMPS* (15 switches not labeled)	When pressed, extinguishes corresponding SELECT JUMPS indicator and disables program jump.
RELEASE STOPS* (5 switch/indicators not labeled)	When pressed, extinguishes corresponding SELECT STOPS and RELEASE STOPS indicators. CPU restarts and executes instruction at jump-to-address specified in halt-keys-and-jump instruction.
MEM-1 FAULT*, MEM-2 FAULT*, MEM-3 FAULT*, MEM-4 FAULT* indicators	When lit, indicates a parity error in the associated main storage unit.
ICR FAULT* indicator	When lit, indicates a parity error in a control register.
INSTRUCTION FAULT* indicator	When lit, indicates an invalid function code in the next instruction to be executed.
PROCESSOR FAULT indicator	When lit, indicates a power, air flow, or temperature fault in either a CPU or a main storage unit.
DAY CLOCK FAULT indicator	When lit, indicates a voltage transient may have caused an incorrect time readout.
CONSOLE FAULT indicator	When lit, indicates an air flow fault in either the display console or an abnormal switch setting on the display console maintenance panel.

Table 3-1. Operator's Control Panel, Controls and Indicators (Part 2 of 3)

Control/Indicator	Function
MSR (3 switch/indicators labeled 0 through 2)	Used to enter a value in memory select register (MSR) or to display the contents of the MSR. The MSR value indicates the main storage module into which the executive program is loaded.
SYSTEM CONTROLS	
FAULT RESET* switch	When pressed, clears all fault indicators on operator's control panel except DAY CLOCK FAULT indicator.
ALARM RESET* switch	When pressed, silences audio alarm.
INITIAL LOAD* switch	When pressed, loads main storage with predetermined program from subsystem selected at CPU maintenance panel and initiates execution of program.
SUBSYSTEM CLEAR† switch	When pressed, clears CPU I/O section and all subsystems connected to CPU I/O channels.
COMPUTER CLEAR switch	When pressed, clears all CPU registers needed for CPU startup.
START* switch	When pressed, initiates program execution at location specified by program address counter.
STOP* switch	When pressed, halts program execution but previously specified I/O data transfers continue to completion.
DAY CLOCK (6 indicators)	Displays time of day in hours, minutes, and hundredths of minutes. Automatically recycles to 0 at midnight.
DAY CLOCK CONTROLS	
FAULT RESET switch	When pressed, extinguishes DAY CLOCK FAULT indicator.
START switch	When pressed, starts day clock.
STOP switch	When pressed, stops day clock to permit setting it, and lights DAY CLOCK FAULT indicator at console.
CLEAR switch	When pressed, resets day clock display to 0.
HOURS and MINUTES (6 switches)	Used to manually step day clock display to desired time of day.
Operational use time meter (optional item)	Displays accumulated CPU running time up to 9999.99 hours and then resets.

*Also appears on CPU maintenance panel.
†Appears on CPU maintenance panel as I/O CLEAR.

Table 3—1. Operator's Control Panel, Controls and Indicators (Part 3 of 3)

3.2.2. Keyboard and CRT Display

This unit (Figure 3—2) is used by the operator to communicate with the operating system. The keyboard enables the operator to alter program execution and to reply to messages displayed on the CRT. Table 3—2 lists the function of each operating control, indicator, and interrupt key.
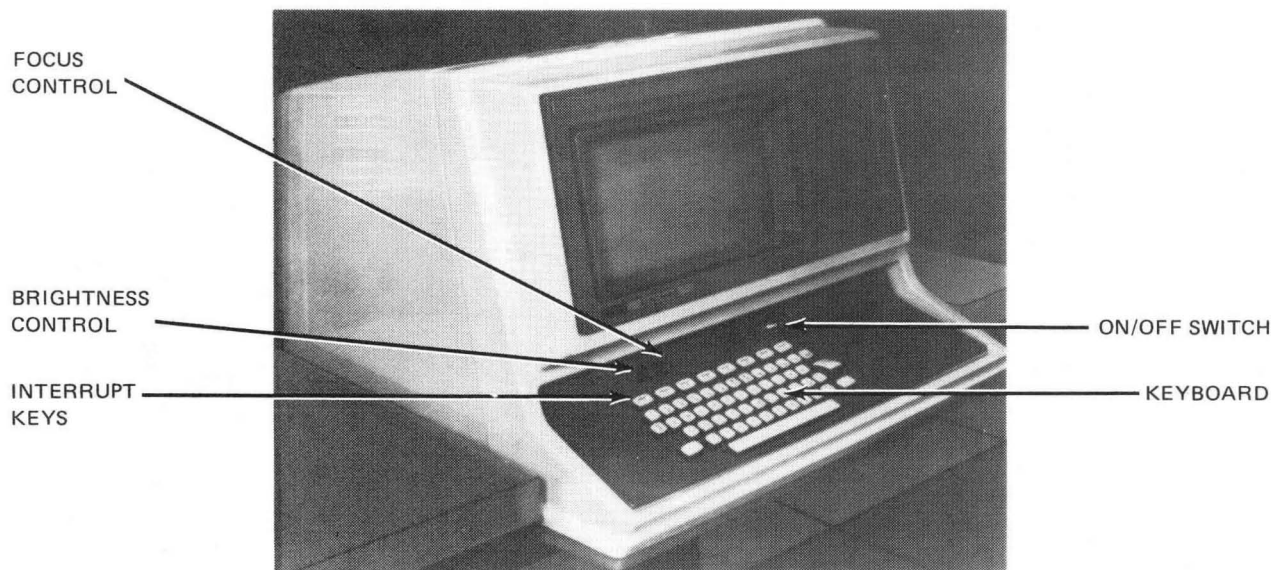

Figure 3—2. Keyboard and CRT Display

Control/Indicator	Function
FOCUS control	Controls the image focus on CRT display.
BRIGHTNESS control	Controls image intensity on CRT display.
INTERRUPT keys	INTERRUPT keys 1 and 4 through 8 are not used. INTERRUPT key 2 enables the operator to backup one character each time it is pressed. INTERRUPT key 3 signals the central processor unit (CPU) that keyboard information is ready for input when pressed.
ON/OFF switch	Controls application and removal of operating power to keyboard and CRT display unit.
Keyboard	Initiates communication with the processor and responds to messages from the processor.

Table 3—2. Keyboard and CRT Display, Controls and Indicators

3.2.3. PAGEWRITER Printer

The PAGEWRITER printer (Figure 3—3) provides the operator with a paper copy of the information appearing on the system portion (first ten lines from a total of 15 are reserved for system messages) of the CRT display.

Figure 3—3. PAGEWRITER Printer

Table 3—3 lists the function of each control and indicator. Figure 3—4 shows the PAGEWRITER printer control panel.
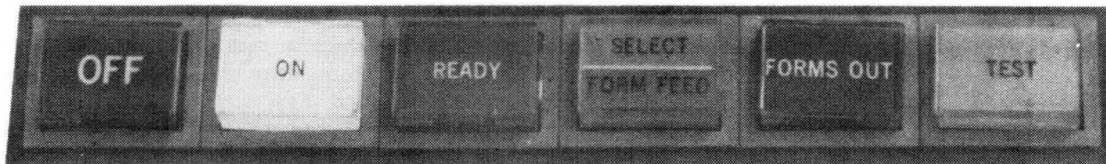

Figure 3—4. PAGEWRITER Printer, Control Panel

Control/Indicator	Function
OFF switch/indicator	When pressed, removes dc power. Indicator lights when power is removed.
ON switch/indicator	When pressed, applies dc power. Indicator lights when power is applied.
READY switch/indicator	When pressed, clears PAGEWRITER printer buffer memory. Indicator lights when PAGEWRITER printer is ready to operate. Indicator will not light if one of the following conditions is present: out of paper, power failure, interlock open, or print actuator failure.
SELECT/FORM FEED switch/split-indicator	When SELECT indicator lights, it signifies that PAGEWRITER printer has been selected for operation. When FORM FEED indicator lights, PAGEWRITER printer feed is being tested. Pressing switch/indicator initiates either select or form feed alternately.
FORMS OUT indicator	When lit, indicates that PAGEWRITER printer is out of paper.
TEST switch/indicator	When pressed, permits offline maintenance testing. Indicator lights when PAGEWRITER printer is being tested.

Table 3—3. PAGEWRITER Printer, Controls and Indicators

3.3. CPU MAINTENANCE PANEL

The CPU maintenance panel (Figure 3—5) is located on the front of the power and maintenance cabinet. The panel is divided into five zones according to general function; the zones are listed from top to bottom:

- Parameter Zone

- I/O Zone

- Arithmetic Zone

- Control Zone

- Control and Monitor Zone

A description of the controls and indicators in each zone is given in the ensuing paragraphs. A separate illustration is provided for each zone. In the accompanying tables, each item is listed according to its label on the panel, and in a left-to-right, top-to-bottom order within the respective table. Items located on both the maintenance panel and operator's control panel are marked with an asterisk.
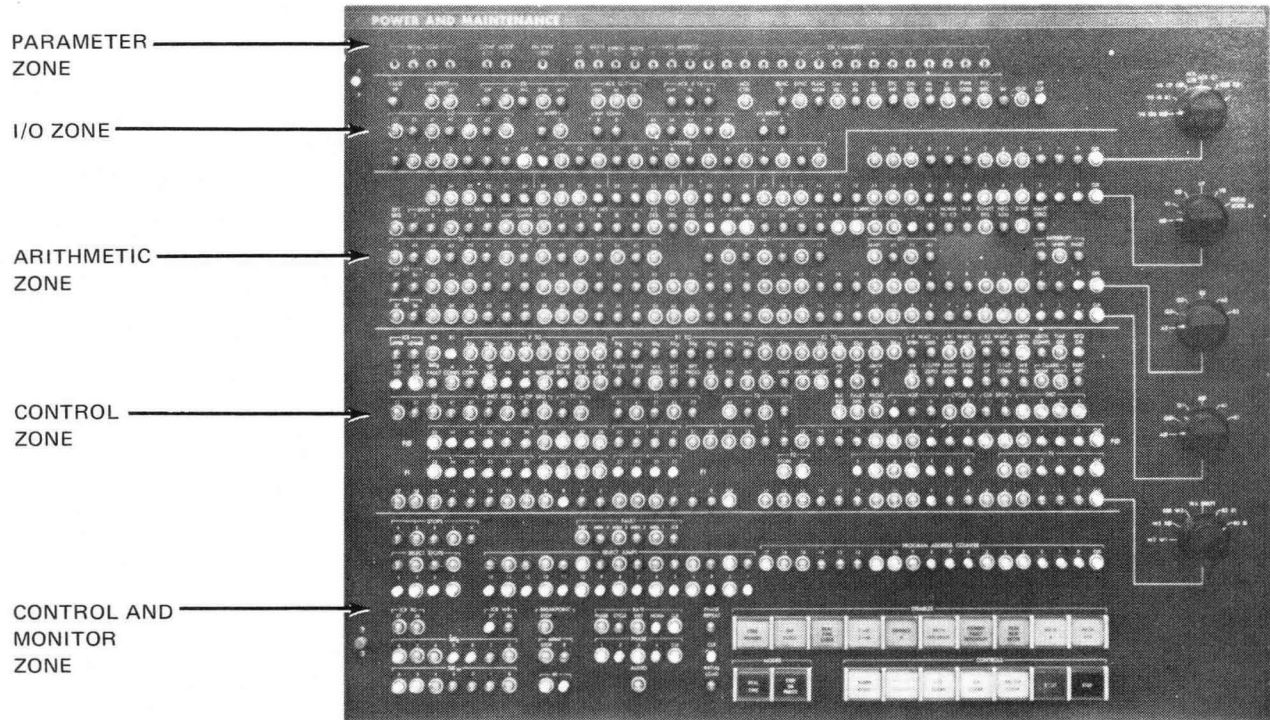
Figure 3—5. CPU Maintenance Panel

3.3.1. Parameter Zone

Figure 3—6 illustrates the parameter zone of the CPU maintenance panel. This zone contains a row of 30 toggle-type switches which are used to select the various system operating parameters. The function of each switch is described in table 3—4.
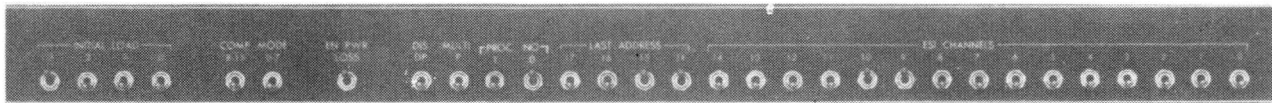

Figure 3—6. CPU Maintenance Panel, Parameter Zone

Control	Function
INITAL LOAD (0 through 3) toggle switches	Used to select I/O channel to be used during initial load operation. Channels are selected by setting a binary number with the switches (for example, setting only switch 2 to up position enters 100_2 which selects I/O channel 4).
COMP MODE (0—7 and 8—15) toggle switches	Used to select normal mode (down position) or UNIVAC 1107 System compatible mode (up position) of I/O operation. COMP MODE 0—7 switch controls I/O channels 0 through 7 and COMP MODE 8—15 switch controls I/O channels 8 through 15.
EN PWR LOSS toggle switch	When set to up position, enables power loss interrupt (if power fails, program automatically jumps to location 210_8. When set to down position, power loss interrupt is disabled.
DIS DP toggle switch	Allows disabling of all double precision instructions. When set to up position, all double precision instructions are detected as being invalid; arithmetic sequences are not initiated, and an interrupt-to-address 241_8 occurs. When set to down position, all double precision instructions are executed in normal manner.
MULTI P toggle switch	Enables an initial load to be performed through an input/output controller (IOC). When set to up position, changes the word count of the initial load buffer control word from 2000_8 to 0001_8 to be compatible with IOC. The normal switch position (without IOC) is down.
PROC NO (0 and 1) toggle switches	Used to determine the main storage for an external interrupt status word. Status word is stored in main storage location 200_8 + processor number. Switches are set as follows: Processor 0 — Both switches down (address 200_8) Processor 1 — 0 switch up and 1 switch down (address 201_8) Processor 2 — 0 switch down and 1 switch up (address 202_8)
LAST ADDRESS (14 through 17) toggle switches	Used to define the highest available address for a given main storage configuration. This address is the interrupt location for main storage parity errors in module 1. Each number represents a binary position in the main storage address system. Switches are set as follows depending on main storage capacity: 17 16 15 14 65K down down up up 131K down up up up 196K up down up up 262K up up up up
ESI Channels (0 through 14) toggle switches	Use to select externally specified index (ESI) mode of operation for I/O channels 0 through 14. (Channel 15, connected to operator's control console, does not have ESI rnode.) When set to up position, places associated I/O channel in ESI mode.

Table 3—4. CPU Maintenance Panel, Parameter Zone Controls

3.3.2. I/O Zone

The three rows of switch/indicators which make up the I/O zone are illustrated in Figure 3—7 and their functions are described in Table 3—5. This zone of the CPU maintenance panel is for use by the Univac customer engineer.
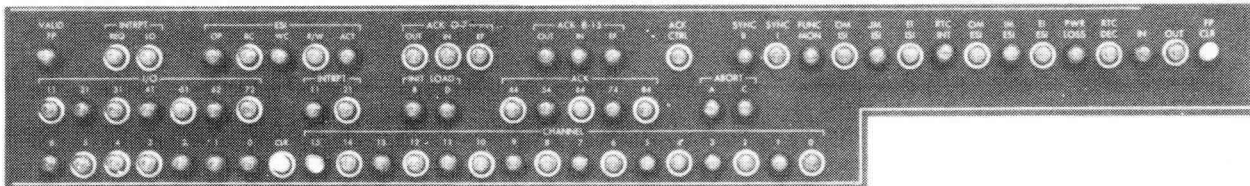
Figure 3—7. CPU Maintenance Panel, I/O Zone

Control/Indicator	Function
NOTE:	
The following switch/indicators are momentary-action switches. When pressed, the switch/indicator lights. Pressing the MASTER CLEAR switch extinguishes the indicator.	
VALID FP	Valid function priority
INTRPT	
REQ	Interrupt request
LO	Interrupt lockout
ESI	
OP	ESI operation
RC	Read control
WC	Write control
R/W	Read/write
ACT	ESI active
ACK 0—7	
OUT	Output
IN	Input
EF	External function
ACK 8—15	
OUT	Output
IN	Input
EF	External function
ACK CTRL	Acknowledge control

Table 3—5. CPU Maintenance Panel, I/O Zone, Controls and Indicators (Part 1 of 2)

Control/Indicator	Function
SYNC II	Sync II
SYNC I	Sync I
FUNC MON	Function monitor
OM ISI	Output monitor (ISI)
IM ISI	Input monitor (ISI)
EI ISI	External interrupt (ISI)
RTC INT	Real time clock interrupt
OM ESI	Output monitor (ESI)
IM ESI	Input monitor (ESI)
EI ESI	External interrupt (ESI)
PWR LOSS	Power loss
RTC DEC	Real time clock decrement
IN	Input data request
OUT	Output data request
FP CLR switch	When pressed, clears function priority.
I/O (7 switch/indicators labeled 11, 21, 31, 41, 51, 62, and 72)	Represents T8 timing chain.
INTRPT (11 and 21) switch/indicators	Indicates interrupt sequence; initiated by any interrupt that does not transfer a status word.
INIT LOAD (B and D) switch/indicators	Indicates second and fourth flip-flops in initial load timing sequence.
ACK (5 switch/indicators labeled 44, 54, 64, 74, and 84)	Represents T9 acknowledge timing chain.
ABORT (A and C) switch/indicators	Indicates first and third flip-flops in I/O abort sequence.
I/O (7 switch/indicators labeled 0 through 6, and 1 CLR switch)	Used to display I/O register selected by rotary switch 1. (Displays contents of V4, V5, V6, ACK CTR, or CSR register.) Selected register is cleared to 0 when CLR switch is pressed.
CHANNEL (16 switch/indicators labeled 0 through 15)	Used in conjunction with first rotary switch to display output acknowledge (OA), input acknowledge (IA), channel priority (CP), or acknowledge (ACK CTR, ACK C1, CSR C2) signals on I/O channels 0 through 15.
First rotary switch	Controls display of I/O registers.

Table 3—5. CPU Maintenance Panel, I/O Zone, Controls and Indicators (Part 2 of 2)

3.3.3. Arithmetic Zone

The arithmetic zone of the CPU maintenance panel contains six rows of switch/indicators for use by the Univac customer engineer. Figure 3—8 illustrates the arithmetic zone and Table 3—6 lists the functions of the switch/indicators.

ROTARY SWITCH 1

ROTARY SWITCH 2

ROTARY SWITCH 3

ROTARY SWITCH 4
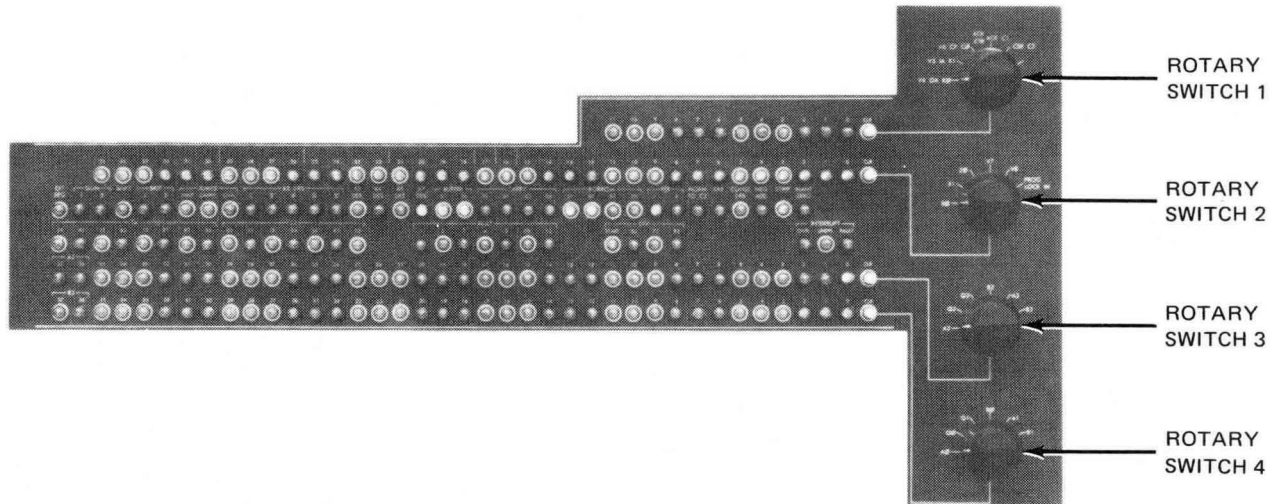
Figure 3—8. CPU Maintenance Panel, Arithmetic Zone

Control/indicator	Function
NOTE:	
The switch/indicators listed in this table are momentary-action switches. When pressed, switch/indicator lights. Pressing of the MASTER CLEAR switch extinguishes the indicator.	
Rotary switch 1	Controls display of one of the following: (1) K0 counter (2) K1 counter (3) C0 register (4) C1 register (5) C2 register (6) Not used
12 switch/indicators labeled 0 through 11, and CLR switch	Used in conjunction with rotary switch 1 to display contents of K0 or K1 counters or C0, C1, or C2 registers.
36 switch/indicators labeled 0 through 35, and CLR switch	Used in conjunction with rotary switch 2 to display contents of X0, X1, Z0, V7, V8, or program lock in register (PROG LOCK IN).

Table 3—6. CPU Maintenance Panel, Arithmetic Zone, Controls and Indicators (Part 1 of 5)

Control/Indicator	Function
Rotary switch 2	Controls display of one of the following: (1) X∅ register (2) X1 register (3) Z∅ register (4) V7 register (5) V8 register (6) PROG LOCK IN register
EXT SEQ	External interrupt sequence
SIGN I II	 Sign I Sign II
SHIFT indicator	When lit, signifies that a shift operation is being performed. Pressing the MASTER CLEAR switch extinguishes the SHIFT indicator.
SKIP I II	Skip I Skip II
JUMPS JUMP CARRY OVFL	 Jump Carry Overflow
X2 DES I II III IV V	 X2 designator I X2 designator II X2 designator III X2 designator IV X2 designator V
X3 DES	X3 designator
X4 DES	X4 designator
X6 DES	X6 designator
X7 DES	X7 designator

Table 3—6. CPU Maintenance Panel, Arithmetic Zone, Controls and Indicators (Part 2 of 5)

7947
UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

3—14
PAGE

Control/Indicator	Function
BUFFER	
36	Buffer 36
37	Buffer 37
CARRY	
S1	Carry S1
D1	Carry D1
S2	Carry S2
D2	Carry D2
BORROW	
S1	Borrow S1
D1	Borrow D1
S2	Borrow S2
D2	Borrow D2
FEB	
1	Forced end borrow 1
2	Forced end borrow 2
NORM TO C3	Normalizer →C3
EAB	Enter A and B registers
CONST DES	Constant designator →C3
NEG ADD	Negative add
STRIP	Strip
MANT ZERO	Mantissa zero
T4	Represents T4 arithmetic timing chain.
34	3.4 T4 sequence
43	4.3 T4 sequence
53	5.3 T4 sequence
63	6.3 T4 sequence
73	7.3 T4 sequence
81	8.1 T4 sequence
83	8.3 T4 sequence
93	9.3 T4 sequence

Table 3—6. CPU Maintenance Panel, Arithmetic Zone, Controls and Indicators (Part 3 of 5)

Control/Indicator	Function
T5	Represents T5 arithmetic timing chain.
02	102 T5 sequence
11	111 T5 sequence
13	113 T5 sequence
24	124 T5 sequence
34	134 T5 sequence
43	143 T5 sequence
53	153 T5 sequence
MULT	Represents T6 multiply control sequence.
1	Multiply control first
2	Multiply control second
3	Multiply control third
4	Multiply control fourth
5	Multiply control fifth
03	0.3 multiply end sequence
13	1.3 multiply end sequence
DIV	Represents T6 divide timing chain.
START	Divide start
63	6.3 divide sequence
72	7.2 divide sequence
82	8.2 divide sequence
INTERRUPT	
OVFL	Overflow
UNDFL	Underflow
FAULT	Fault
38 switch/indicators labeled 0 through 37, and CLR switch	Used in conjunction with rotary switch 3 to display arithmetic registers. (Displays contents of A2, Q2, Q3, B2, A3, or B3 register.) Selected register is cleared to 0 when CLR switch is pressed.

Table 3—6. CPU Maintenance Panel, Arithmetic Zone, Controls and Indicators (Part 4 of 5)

Control/Indicator	Function
Rotary switch 3	Controls display of one of the following: (1) A2 register (2) Q2 register (3) Q3 register (4) B2 register (5) A3 register (6) B3 register
38 switch/indicators labeled 0 through 37, and CLR switch	Used in conjunction with fourth rotary switch to display arithmetic registers. (Displays contents of A0, Q0, Q1 B0, A1, or B1 register.) Selected register is cleared to 0 when CLR switch is pressed.
Rotary switch 4	Controls display of one of the following: (1) A0 register (2) Q0 register (3) Q1 register (4) B0 register (5) A1 register (6) B1 register

Table 3—6. CPU Maintenance Panel, Arithmetic Zone, Controls and Indicators (Part 5 of 5)

3.3.4. Control Zone

The control zone contains six rows of switch/indicators. This zone of the CPU maintenance panel is for use by the Univac customer engineer. The top three rows indicate the state of the control logic designators. Each switch/indicator is labeled with an abbreviation of the name of the designator it represents. The fourth and fifth rows of switch/indicators display the F registers. The sixth row contains two groups of 18 switch/indicators and are used to display various control registers.

The control zone is shown in Figure 3—9 and the functions of the switch/indicators are described in Table 3—7.

ROTARY
SWITCH 5
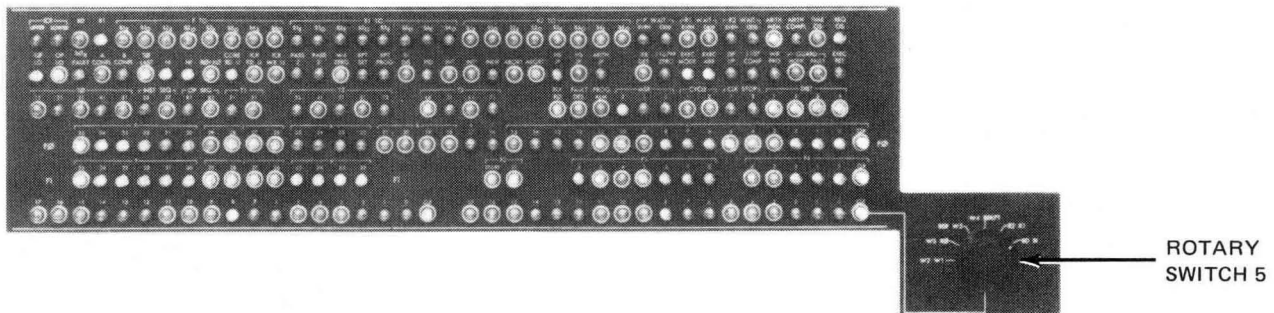
Figure 3—9. CPU Maintenance Panel, Control Zone

7947

UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

3–17

PAGE

Control/Indicator	Function
NOTE: The following switch/indicators are momentary-action switches. When pressed, switch/indicator lights. Pressing of the MASTER CLEAR switch extinguishes the indicator.	
ICR	
UPPER	Integrated circuit register (ICR) write upper
LOWER	Integrated circuit register (ICR) write lower
BD	BD designator
R1	R1 designator
P TO	
$S1_E$	P to S1 even
$S1_O$	P to S1 odd
$S2_E$	P to S2 even
$S2_O$	P to S2 odd
$S3_E$	P to S3 even
$S3_O$	P to S3 odd
$S4_E$	P to S4 even
$S4_O$	P to S4 odd
R1 TO	
$S1_E$	R1 to S1 even
$S1_O$	R1 to S1 odd
$S2_E$	R1 to S2 even
$S2_O$	R1 to S2 odd
$S3_E$	R1 to S3 even
$S3_O$	R1 to S3 odd
$S4_E$	R1 to S4 even
$S4_O$	R1 to S4 odd

Table 3–7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 1 of 6)

7947
UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

3-18
PAGE

Control/Indicator	Function
R2 TO	
$S1_E$	R2 to S1 even
$S1_O$	R2 to S1 odd
$S2_E$	R2 to S2 even
$S2_O$	R2 to S2 odd
$S3_E$	R2 to S3 even
$S3_O$	R2 to S3 odd
$S4_E$	R2 to S4 even
$S4_O$	R2 to S4 odd
P WAIT	
EVEN	P wait even
ODD	P wait odd
R1 WAIT	
EVEN	R1 wait even
ODD	R1 wait odd
R2 WAIT	
EVEN	R2 wait even
ODD	R2 wait odd
ARITH MEM	Arithmetic → memory
ARITH COMPL	Arithmetic complement → memory
TIME OS	Timeout one shot
REQ OS	I/O request one shot
T0 LO	T0 lockout
OP LO	Operand lockout
$S0_R$ FAULT	$S0_R$ fault
A CONFL	A conflict
B CONFL	B conflict
T0 LAST	T0 last
NI	Next instruction designator
NI'	Next instruction' designator

Table 3—7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 2 of 6)

7947

UP-NUMBER

UNIVAC 1106/1108 SYSTEMS

PAGE REVISION

3–19

PAGE

Control/Indicator	Function
R0 → X0	R0 → X0 designator
CORE RD U	Core read U
ICR RD U	Integrated circuit register (ICR) read U (operand address)
ICR WR U	Integrated circuit register (ICR) write U (operand address)
PASS 2	Pass 2
Pass 2'	Pass 2'
W4 ZERO	W4 = 0
RPT SET	Repeat setup
RPT PROG	Repeat in progress
EI DIS	EI disable
PID	Program interrupt disable
INT	Interrupt
INT'	Interrupt'
INDR	Indirect
ABORT	Abort
ABORT'	Abort'
HS JP	High speed jump
HS JP'	High speed jump'
ARTH JP	Arithmetic jump designator
IFR DES	Internal function register (IFR) designator
1107FP ZERO	1107 Floating point zero
EXEC MODE	Executive mode
EXEC ABR	Executive A, B, and R registers
DP UF	Block double-precision underflow
1107 COMP	1107 compatible
WR PRO	Write protection
GUARD	
MODE	Guard mode
FAULT	Guard mode fault

Table 3–7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 3 of 6)

Control/Indicator	Function
EXEC RET	Executive return
T0	
11	1.1 T0 sequence
21	2.1 T0 sequence
31	3.1 T0 sequence
41	4.1 T0 sequence
51	5.1 T0 sequence
INST SEQ	
55	5.1 instruction sequence
57	5.3 instruction sequence
OP SEQ	
81	8.1 operation sequence
83	8.3 operation sequence
T1	
21	2.1 T1 sequence
31	3.1 T1 sequence
T2	
31	3.1 T2 sequence
41	4.1 T2 sequence
51	5.1 T2 sequence
61	6.1 T2 sequence
72	7.2 T2 sequence
T3	
44	4.4 T3 sequence
51	5.1 T3 sequence
61	6.1 T3 sequence
71	7.1 T3 sequence
BLK R0	Block R0
FAULT DES	Fault designator
PROG ALM	Program alarm

Table 3—7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 4 of 6)

Control/Indicator	Function
MSR	
2	Memory select register (MSR) 02
1	Memory select register (MSR) 01
0	Memory select register (MSR) 00
CYCLE	
1	Cycle I
2	Cycle II
CLK STOP	
1	To be used for maintenance purposes.
2	To be used for maintenance purposes.
DIST	
1	Distribution 1
2	Distribution 2
3	Distribution 3
4	Distribution 4
F∅ (36 switch/indicators labeled 0 through 35, and CLR switch)	Displays contents of F∅ register. When pressed, CLR switch clears F∅ register to 0.
F1 (14 switch/indicators labeled 22 through 35)	Displays contents of F1 register.
F2	
STORE	T1 store designator
3T	3T write
F3 (7 switch/indicators labeled 0 through 6)	Displays contents of F3 register.
F4 (5 switch/indicators labeled 0 through 4, and CLR switch)	Displays contents of F4 register. When pressed, CLR switch clears registers F1, F2, F3, and F4 to 0.
18 switch/indicators labeled 0 through 17, and CLR switch	Used in conjunction with rotary switch 5 to display various control registers. (Displays contents of W2 register, W3 register, BSR (bits 9—5 of Internal Function Register, IFR), W4 register, R2 register, or BD (bits 8—0 of IFR). When pressed, CLR switch clears selected register to 0.

Table 3—7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 5 of 6)

Control/Indicator	Function
18 switch/indicators labeled 0 through 17, and CLR switch	Used in conjunction with rotary switch 5 to display various control registers. (Displays contents of W1 register, RØ register, W5 register, breakpoint register, R1 register, or BI, bits 26 through 18 of IFR.) When pressed, CLR switch clears selected register to 0.
Rotary switch 5	Controls display of one of the following: (1) W2 register; W1 register (2) W3 register; RØ register (3) BSR; W5 register (4) W4 register; breakpoint register (5) R2 register; R1 register (6) BD; BI

Table 3—7. CPU Maintenance Panel, Control Zone, Controls and Indicators (Part 6 of 6)

3.3.5. Control and Monitor Zone

The control and monitor zone contains the controls and indicators used for manual operation and control of the processor. The controls and indicators are illustrated in Figure 3—10 and are described in Table 3—8.
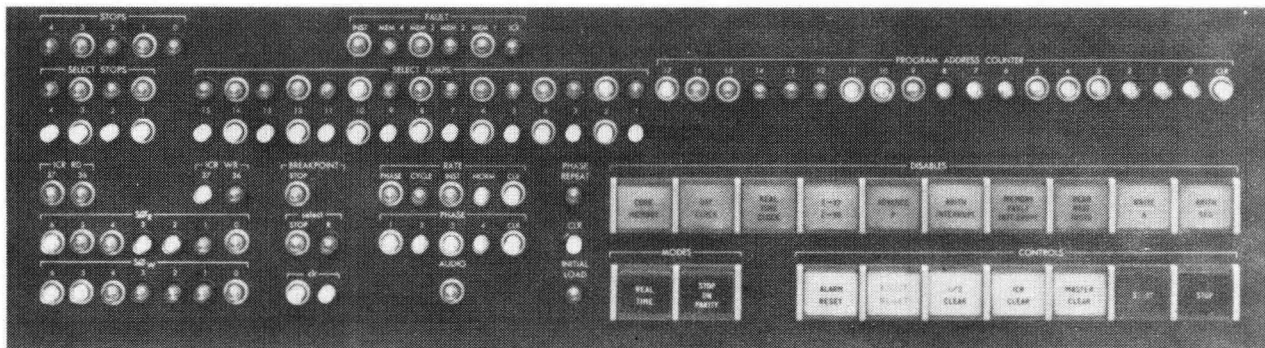

Figure 3—10. CPU Maintenance Panel, Control and Monitor Zone

Control/Indicator	Function
STOPS* (0 through 4) indicator	One of these indicators lights when one of the selected-program stops occurs. (Refer to SELECT STOPS switch/indicators.)
SELECT STOPS* (4 switch/indicators and associated clearing switches labeled 1 through 4)	Operate in conjunction with a halt-keys-and-jump instruction. Pressing one of the switch/indicators lights its indicator and sets the conditional stop. When program halts (the a-field of instruction is 0 or equals bit configuration set on SELECT STOPS switch/indicators), it is restarted by pressing corresponding CLEAR switch. Program starts at jump-to-address specified in halt-keys-and-jump instruction. If the a-field of instruction does not equal bit configuration set on SELECT STOPS switch/indicators or if it is not 0, or if CPU is in guard or real time mode, the program does not halt, but immediately jumps to the jump-to-address specified in the instruction.
FAULT	NOTE: Any one of these fault indicators can be cleared by pressing FAULT RESET switch on operator's control panel after the fault is corrected.
INST* indicator	When lit, indicates an invalid function code has been detected (CPU is not in guard mode); audible fault alarm at operator's console also sounds. When in guard mode, the fault alarm does not sound, but invalid instruction interrupt does occur, permitting debugging.
MEM 1*, MEM 2*, MEM 3*, MEM 4* indicators	When lit, indicates detection of a parity error in associated main storage unit.
ICR* indicator	When lit, indicates a parity error has been detected in a control register.
SELECT JUMPS* (15 switch/indicators and associated clearing switches labeled 1 through 15)	Used to vary program execution and in booting and dumping procedures. Operates in conjunction with a jump-keys instruction. Pressing a SELECT JUMPS switch/indicator lights its indicator and enables corresponding jump when it is encountered in program. Programmer must inform operator which SELECT JUMPS switches are to be set for his program. When a clearing switch is pressed, corresponding SELECT JUMPS switch/indicator is extinguished and program jump is disabled.
PROGRAM ADDRESS COUNTER* (18 switch/indicators labeled 0 through 17, and CLR switch)	Allows monitoring of program address and manual setting of a program address when the processor is stopped. CLR switch is used to reset counter to 0.
ICR RD (36 and 37) indicators	When lit, indicates parity bit of word being read out of a control register is a 1 bit. ICR RD 36 is the parity bit for lower half of word (bits 17—0) and ICR RD 37 is parity bit for upper half of word (bits 35—18).
ICR WR (36 and 37) indicators	When lit, indicates parity bit of word being written into a control register is a 1 bit. ICR WR 36 is the parity bit for lower half of words (bits 17—0) and ICR WR 37 is parity bit for upper half of word (bits 35—18).
$S\emptyset_R$ (0 through 6) indicators	Used to indicate control register address from which data is being read.
$S\emptyset_W$ (0 through 6) indicators	Used to indicate control register address into which data is being written.
BREAKPOINT STOP indicator	When lit, indicates processor has stopped at end of main timing chain.

Table 3—8. CPU Maintenance Panel, Control and Monitor Zone, Controls and Indicators (Part 1 of 4)

Control/Indicator	Function
Select (STOP and R) switch/indicators, and associated CLR switches	These two switch/indicators are used jointly. Pressing only the SELECT STOP switch/indicator lights its indicator and the processor stops when address in breakpoint registers equals either the P-register contents, interrupt address, indirect address, or execute remote address. If both switch/indicators are pressed, processor halts when address in breakpoint register equals read or write operand address. When pressed, the CLR switches extinguish associated switch/indicator and disable breakpoint action.
NOTE: Only one of the following RATE switch/indicators can be active at any instant. Before selecting a new rate of processor operation, CLR switch must be pressed to clear previous selection.	
RATE	
PHASE switch/indicator	When pressed indicator lights and clock phase rate of operation is selected. Starting with phase 4, one clock phase is executed each time START switch is pressed. Another rate cannot be selected unless next clock phase to be executed is phase 4.
CYCLE switch/indicator	When pressed, indicator lights and clock cycle rate of operation is selected. One clock cycle (four phases) is executed each time START switch is pressed.
INST switch/indicator	When pressed, indicator lights and instruction rate of operation is selected. One instruction is completed each time START switch is pressed.
NORM switch/indicator	When pressed, indicator lights and normal rate of instruction execution is selected. Clock pulses are issued at normal rate regardless of whether program is halted or running. MASTER CLEAR switch can also be used to select normal rate. Normal rate selection can only be cleared by CLR switch when processor is halted.
CLR switch	When pressed, clears all RATE selections.
PHASE (4 switch/indicators labeled 1 through 4, and CLR switch)	Used to select a particular clock phase and to indicate the next clock phase to be generated. Indicators denote steps 1 through 4 of the phase-step distributor. CLR switch resets the four phase-step distributor.
AUDIO switch/indicator	Used to set the audio flip-flop to enable the audio alarm. Alarm sounds and AUDIO indicator lights when guard mode circuit is set, and turns off when cleared. Guard mode is under program control. To clear the audio circuit and extinguish the AUDIO indicator, press ALARM RESET switch on CPU maintenance panel or ALARM RESET switch on console operator's control panel.
PHASE REPEAT switch/indicator and CLR switch	Switch/indicator is used to alternately set and reset the phase-repeat circuit. Phase-repeat circuit can be set only when in clock-phase-rate operation and disables advancing phase-steop distributor. Pressing the START switch once initiates a continuous generation of the particular phase selected. Pressing CLR switch stops repetitive generation of clock-phase-pulses and phase distributor advances to next phase and then stops. This switch/indicator is for use by Univac customer engineer only.
INITIAL LOAD* switch/indicator	Used to set initial load circuit which allows initiating initial load sequence by pressing START switch. Two thousand (octal) words are transferred into main storage locations 0 through 1777_8 (biased by MSR) via I/O channel selected by the setting of INITIAL LOAD switches.

Table 3—8. CPU Maintenance Panel, Control and Monitor Zone, Controls and Indicators (Part 2 of 4)

Control/Indicator	Function
DISABLES	
CORE MEMORY indicator	When lit, indicates a switch on one of the main storage unit maintenance panels has been set to test position, or power has been removed from one of the main storage units.
NOTE:	
The following switch/indicators are alternate-action switches. When pressed, switch/indicator lights and listed function is performed. When pressed again, indicator extinguishes and function action is normalized.	
DAY CLOCK* switch/indicator	When pressed, disables day clock interrupt and lights DISABLE DAY CLOCK indicator on CPU maintenance panel at console operator's control panel. This indicator can be extinguished only from CPU maintenance panel.
REAL TIME CLOCK* switch/indicator	When pressed, disables real time clock and lights DISABLE RT CLOCK indicator on console operator's control panel. This indicator can be extinguished only from CPU maintenance panel.
Z→V7/Z→V8 switch/indicator	When pressed, prevents data transmission from main storage to output register and lights PROCESSOR disable indicator on console operator's control panel.
ADVANCE P switch/indicator	When pressed, prevents initiation of advance P-register sequence and lights DISABLE PROCESSOR indicator on console operator's control panel.
ARITH INTERRUPT switch/indicator	When pressed, disables all arithmetic interrupts and lights DISABLE PROCESSOR indicator on console operator's control panel.
MEMORY FAULT INTERRUPT switch/indicator	When pressed, disables control register and main storage parity error interrupts and lights DISABLE PROCESSOR indicator on console operator's control panel.
READ NEXT INSTR switch/indicator	When pressed, prevents clearing of F0 register and Z register to F0 register data transfers, and lights DISABLE PROCESSOR indicator on console operator's control panel.
WRITE A switch/indicator	When pressed, prevents storing data in control register except when specified by the u-field address (disables the a-field write) and lights DISABLE PROCESSOR indicator on console operator's control panel.
ARITH SEQ switch/indicator	When pressed, data can be written directly into control registers from A0 registers and into main storage directly from X0 register. It also lights DISABLE PROCESSOR indicator on console operator's control panel.
MODES	
NOTE:	
These switch/indicators are alternate-action switches. When pressed, switch/indicator lights and listed function is performed. When pressed again, indicator extinguishes and function action is normalized.	
REAL TIME* switch/indicator	When pressed, disables most of the controls on console operator's control panel to prevent operator intervention during real time processing. The following controls, however, are not disabled: SELECT JUMPS, RELEASE JUMPS, RELEASE STOPS, FAULT RESET, and ALARM RESET. MODES REAL TIME indicators on CPU maintenance panel and at operator's control panel light. (Indicator at console operator's control panel only.)

Table 3—8. CPU Maintenance Panel, Control and Monitor Zone, Controls and Indicators (Part 3 of 4)

Control/Indicator	Function
MODES (continued) STOP ON PARITY* switch/indicator	When pressed, halts processor when a main storage or control register parity error interrupt occurs and lights PARITY STOP indicator on CPU maintenance panel and at operator's control panel. (Indicator at console operator's control console panel only.)
CONTROLS ALARM RESET* switch	When pressed, silences audio alarm at operator's control and indicator panel. If alarm sounds because of temperature or air flow fault, alarm cannot be silenced until fault is corrected. Alarm can be turned on by executing an initiate-interprocessor-interrupt instruction (multiprocessor only) or by pressing AUDIO switch/indicator.
FAULT RESET* switch	When pressed, clears following fault indicators: ICR FAULT, MEM-1 FAULT, MEM-2 FAULT, MEM-3 FAULT, MEM-4 FAULT, and INSTRUCTION FAULT.
I/O CLEAR switch	When pressed, sends clear signal to each peripheral subsystem if processor is halted.
ICR CLEAR switch	When pressed, sets all control registers equal to value in Z0 register of unit processor (to value on A0 register of multiprocessor unit) if processor is halted.
MASTER CLEAR switch	When pressed, clears processor and main storage registers, but not control registers, to permit program restart. Registers are cleared only if processor is halted.
START* switch/indicator	When pressed, indicator lights and processor starts. When clock phase, clock cycle, or instruction rate of operation has been selected, one clock phase, one clock cycle, or one pass through main timing chain is initiated each time START switch is pressed.
STOP* switch/indicator	When pressed, indicator lights and processor halts. Normally, processor stops at end of main timing chain (T0) and previously initiated I/O operations continue to completion. If clock-phase or clock-cycle rate of operation has been selected, indicator remains lit until instruction execution is completed.

*Also appears on console operator's control panel.

Table 3—8. CPU Maintenance Panel, Control and Monitor Zone, Controls and Indicators (Part 4 of 4)

4. OPERATION

4.1. GENERAL

It is the responsibility of the operator to turn power on and off to the printer, to ensure proper form control, and to load forms and change ribbon when needed.

Due to the complexity of the equipment and the pecularities of each installation, no turnon or turnoff procedures, recovery procedures or operator performed maintenance is given. Consult the Univac customer engineer to obtain procedures for your installation.

4.2. LOADING FORMS INTO PAGEWRITER PRINTER

To load forms into the PAGEWRITER printer (Figure 4—1), proceed as follows:

1. Press OFF switch/indicator and raise cover.

2. Expose rubber rollers by lifting paper guide rod and upper paper support.

3. Release tension of paper drag plate by sliding lever to right (lever located under control switches).

4. Remove old paper through take-up chute. If paper is on roller, remove it by lifting roller from support slots, releasing collar, and sliding roll from spindle.

5. Slide new paper roll over spindle and replace collar.

6. Place roll, with paper unrolling from back side, in slots.

    NOTE:

    If forms with edge sprockets are used, remove roller and put box under take-up chute.

7. Pull paper through take-up chute, between paper drag plate and frame, over platen assembly (if paper has holes, engage them with teeth of both sprockets), and under rollers of upper paper support.

    a. Center paper so that left side overlaps path of print wheel.

    b. Slide paper drag plate lever to left.

    c. Lower paper guide rod and upper paper support.

    d. Lift lever located a few inches behind control switches so that OFF switch/indicator lights. Release lever.

e. Press ON switch/indicator. ON and READY indicators should light.

f. Press TEST switch. Print wheel should glide across paper and print a line of E's.

g. From line of E's determine if paper needs further adjustment; if so, press OFF switch/indicator and repeat steps (a) through (f).

8. Press SELECT/FORM FEED switch to test for proper feed without jamming, slipping, and so forth.
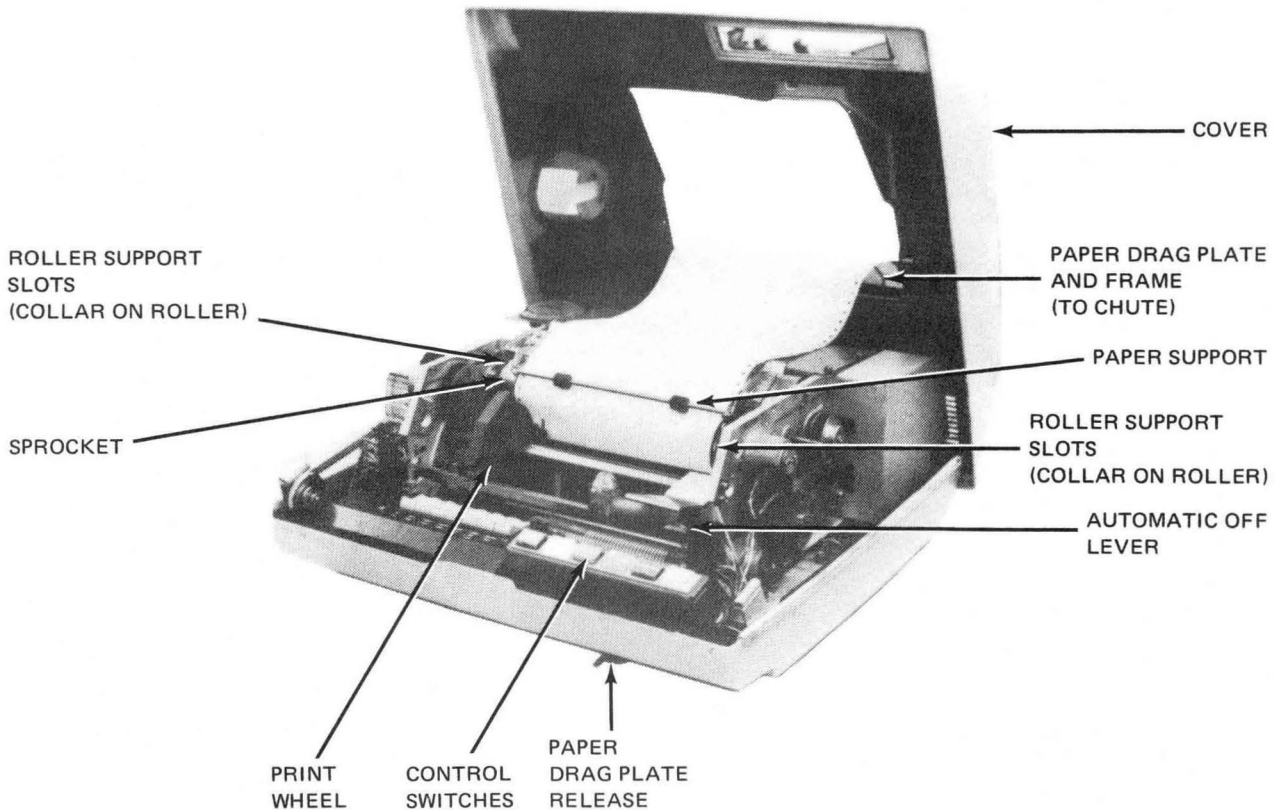
9. Close cover.

Figure 4—1. Loading Forms Into PAGEWRITER Printer

4.3. CHANGING PAGEWRITER PRINTER RIBBON

To change the ribbon in the PAGEWRITER printer (Figure 4—2), proceed as follows:

1. Press OFF switch/indicator and remove cover.

2. Slide covers from ribbon reels.

3. Snap wire guides away from reels.

4. Slip ribbon from guides on print wheel assembly and remove ribbon from both reel centers.

5. Slip new ribbon onto one reel center and replace reel cover.

6. Unwind a portion of ribbon and insert end into groove on other reel center. Replace cover.

7. Position ribbon around each wire guide and into guides on print wheel assembly so that ribbon is in front of two guides closest to print wheel and behind copper-colored strip.

8. Replace cover and press ON switch/indicator.

9. After READY indicator lights, press TEST switch/indicator to test for proper ribbon movement.
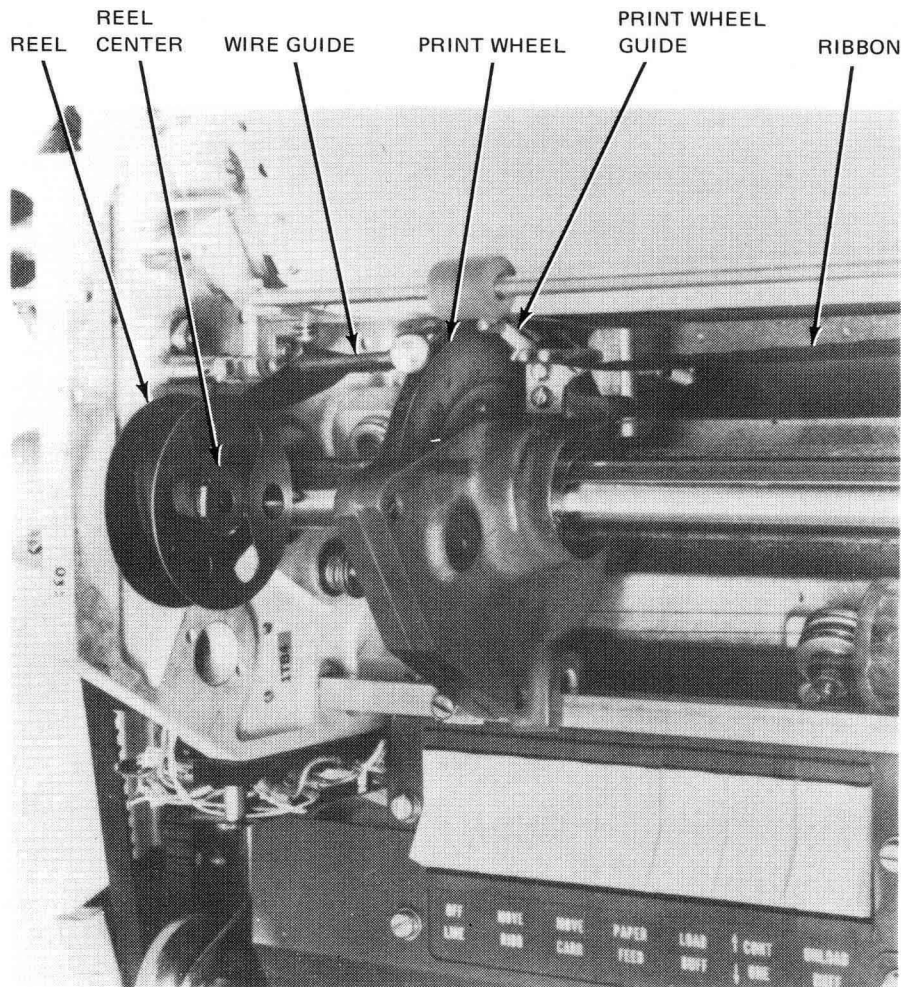

Figure 4—2. Changing PAGEWRITER Printer Ribbon