INSTALLATION AND OPERATION

WD800/WD800A Mass Storage System

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MANUAL REVISION HISTORY

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The computers, as well as the programs that TI has created to use with them, are tools that can help people better manage the information used in their business; but tools—including TI computers—cannot replace sound judgment nor make the manager's business decisions.

Consequently, TI cannot warrant that its systems are suitable for any specific customer application. The manager must rely on judgment of what is best for his or her business.

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Preface

This manual provides detailed instructions for installing and operating a WD800 or WD800A mass storage system. It also contains programming information for those users who write their own input/output routines. The information in this manual is divided into five sections and three appendixes as follows:

NOTE

The WD800 and WD800A operate in a similar manner. They primarily differ in the storage capacities of the Winchester disk drives. Unless noted otherwise, when this manual refers to the WD800, the information applies to both the WD800 and the WD800A disk units.

Section

1 WD800 System Kit Description — Briefly describes the features and major components of the WD800 system.

2 TILINE Peripheral Bus Interface (TPBI) — Describes the operation of the TPBI and explains the procedures for unpacking, installing, and programming the TPBI board.

3 WD800 Chassis Installation and Programming — Provides site requirements and step-by-step instructions for unpacking, installing, and programming the chassis.

4 WD800 System Kit Installation — Explains the kit-level installation of the WD800 system, system self-tests and diagnostics, and procedures for system checkout.

5 Operation — Describes the operator's use of the system.

Appendix

A Fault Analysis — Provides information for use in analyzing system fault conditions.

B TPBI System Command Trace Feature — Provides operating instructions for using the TPBI command trace in troubleshooting system problems.

C Sample 990 Device Service Routines — Provides instructions and sample device service routines (DSRs) for users who write their own input/output routines.

The following documents contain additional information related to the WD800 mass storage system:

Title	Part Number
Business Systems 600/800 Field Engineering Reference Handbook	2311344-9701
WD800/WD800A Mass Storage System Field Maintenance Manual	2306142-9701
Model 990/12 Computer Hardware User's Manual	2264446-9701
Model 990/12 LR Computer General Description	2268239-9701
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990/10A Computer General Description	2302633-9701
Model 990A13 Chassis General Description	2308774-9701
Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual	2270509-9701
Model 990 Computer Family Maintenance Drawings, Volume 4 — TILINE Expansion and Peripherals	945421-9704
Unit Diagnostic Handbook, Volume 1 — General 990 Unit Diagnostic Information	945400-9701
Unit Diagnostic Handbook, Volume 3 — Diagnostics for 990 Mass Storage Devices	945400-9703
Model 990 Computer TILINE Peripheral Bus Interface Depot Maintenance Manual	2306143-9701
DX10 Operating System Manual, Volume II — Operation Manual	946250-9702
DX10 Operating System Manual, Volume V — Systems Programming Guide	946250-9705
Universal ROM Loader User's Guide	2270534-9701
DNOS System Command Interpreter Reference Manual	2270503-9701
DNOS Operations Guide	2270502-9701

Title	Part Number
DNOS System Generation Reference Manual	2270511-9701
Business Systems 600/800 Installation Manual	2311341-9701

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4 — WD800 System Kit Installation

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WD800/WD800A System Kit Description

1.1 GENERAL

The Model 990 Computer WD800 and WD800A Mass Storage System Kits (Figure 1-1) provide random-access mass data storage systems for any Texas Instruments Model 990 Computer with a TILINE™, the TI asynchronous, 16-bit parallel data bus that transfers data between high-speed system elements. The WD800 systems use Winchester disk technology for the primary storage device, and provide removable backup storage with a magnetic tape cartridge. Up to four Winchester disk drives with four tape cartridge transports can be connected in a daisy-chained configuration to a single controller installed in the host system. The host system can be any 990 computer system with an interface meeting the requirements of the TILINE.

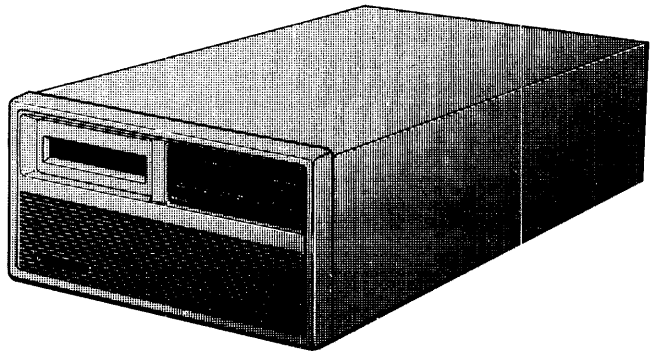
NOTE

The WD800 and WD800A operate in a similar manner. Unless noted otherwise, when this manual refers to the WD800, the information applies to both the WD800 and the WD800A disk units.

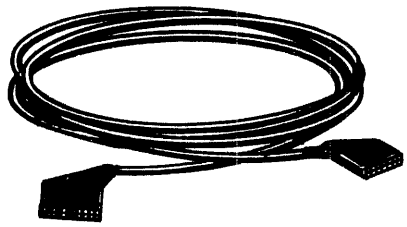
The WD800 mass storage system kit includes the following features:

- Single circuit board 990 TILINE peripheral bus interface (TPBI) controller
- Plug compatible with WD500/WD500A mass storage systems
- Compatibility with 990 computer systems
- Winchester disk with error correcting code (ECC) for error checking and correcting capability
- Microprocessor-based controller logic
- Cartridge tape removable medium
- Integral power supply
- Rackmount or tabletop configuration
- Support for all standard Texas Instruments international voltage/frequency combinations

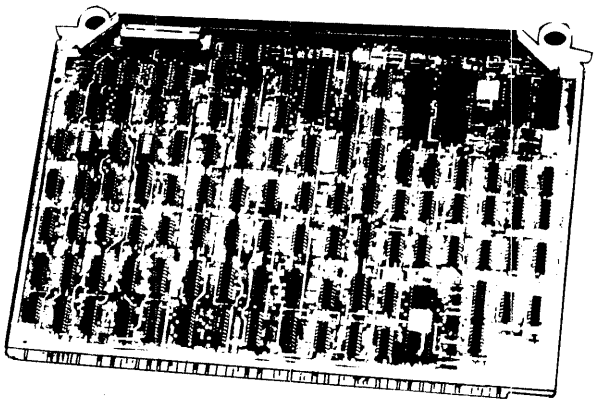
TILINE is a trademark of Texas Instruments Incorporated.



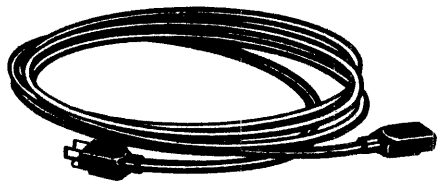
DISK UNIT



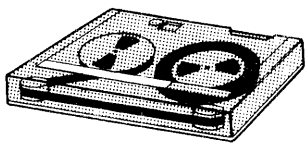
PERIPHERAL BUS
INTERFACE
CABLE



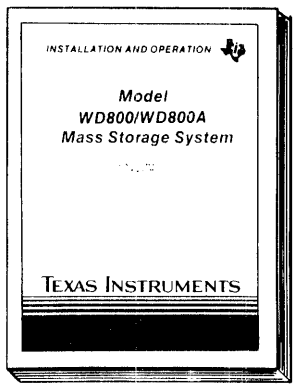
TPBI BOARD
(FOR BUSINESS SYSTEM 600/800 APPLICATIONS)



POWER
CORD



TAPE CARTRIDGE



DISK UNIT
INSTALLATION AND
OPERATION MANUAL

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Figure 1-1. WD800 System Kit

1.2 KIT COMPONENTS

The WD800 system kit consists of the following major assemblies:

- TPBI board
- Peripheral bus cable
- WD800 system chassis that includes the following:
  - — Winchester disk drive assembly
  - — Magnetic tape cartridge transport assembly
  - — Front panel controls and indicators
  - — Card cage with motherboard and printed circuit boards (PCBs) for the formatter function and the disk and tape cartridge electronics
  - — Power supply

Major system component part numbers are listed in Table 1-1.

Table 1-1. System Component Part Numbers

Component	Part Number
WD800 Storage System Chassis	2215801-XXXX[1] (Chassis mount — Not shown) or 2213097-XXXX[1] (Chassis mount — Figure 1-2) or 2213074-XXXX[1] (Table top — Figure 1-1)
WD800A Storage System Chassis	2245216-0037 through 0072[1,2] (Chassis mount — not shown) or 2245216-0001 through 0036[1,2] (Table top — not shown)
Peripheral Bus Cable Assembly	2308633-0003
TPBI Assembly	2270820-0001
Tape Cartridge Media: 137 m (450 ft)	2270391-0001

Notes:

[1] The dash number indicates the exact voltage, frequency, and disk capacity specifications of the system.

[2] Similar in appearance to the WD800.

1.2.1 TPBI Board

The TPBI board occupies one full slot in the 990 chassis and furnishes communication between the 990 system and the formatter in the WD800 system. The TPBI uses the TILINE for host system communication and the peripheral bus interface (PBI) for formatter communication.

1.2.2 Peripheral Bus Cable

The peripheral bus cable connects the TPBI board to the WD800 chassis and interconnects daisy-chained chassis. The system uses a 40-pin cable connector assembly with a metal backshell to minimize electromagnetic interference (EMI). The maximum cable length is 15 meters (49.2 feet). Cable terminator resistor packs are inside the WD800 chassis.

1.2.3 WD800 Chassis

The WD800 chassis (Figure 1-2) contains the Winchester disk drive, the magnetic tape cartridge transport, the front panel controls and indicators, the card cage, and the power supply assembly.

1.2.3.1 Winchester Disk Drive. The disk drive subassembly consists of a die-cast deck with a sealed area for heads, platters, and servo-positioning motor. The spindle motor, spindle motor brake, positioner locking mechanism, and electronics are mounted beneath the sealed housing.

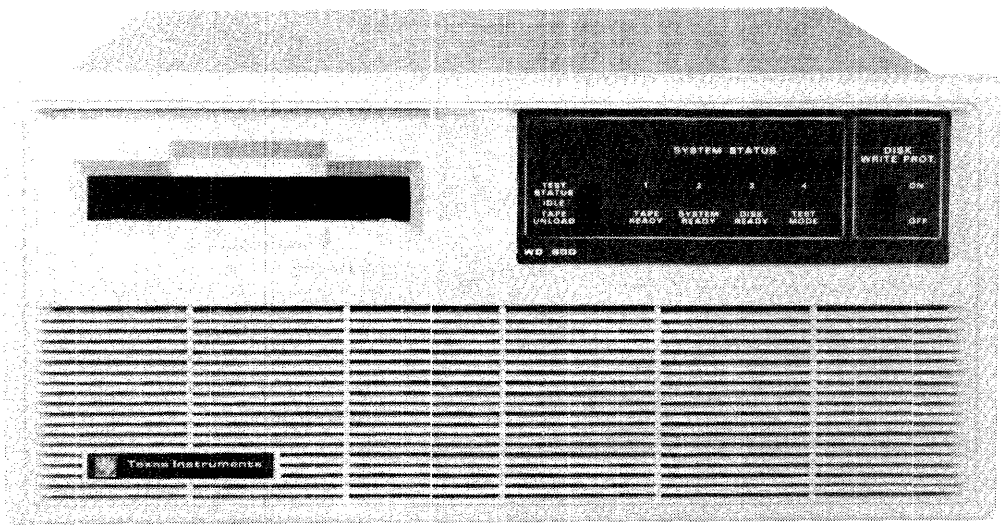

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Figure 1-2. WD800 Chassis

1.2.3.2 Magnetic Tape Cartridge Transport. The magnetic tape cartridge transport subassembly is optional in all chassis except one where it is required to provide backup. The tape transport subassembly includes the following items:

- Tape transport drive assembly that consists of the following:
  - — Transport (deck, motor, heads, sensors, and cables)
  - — Transport mounting brackets
  - — Tape subsystem analog PCB assembly
- Tape subsystem analog PCB power cable
- Transport-to-encode/decode PCB cable
- Tape encode/decode PCB assembly
- Tape control PCB assembly

1.2.3.3 Front Panel Controls and Indicators. The WD800 system chassis has three controls: the ac power switch, the TEST STATUS/TAPE UNLOAD switch, and the DISK WRITE-PROTECT switch. The ac power switch is located on the chassis rear panel. Turning on the ac power switch initializes the system. The other two switches are located on the front panel. The TEST STATUS/TAPE UNLOAD switch, a three-position, spring-loaded, momentary-action switch, selects either test status or tape unload mode. The DISK WRITE-PROTECT switch selects the write-protect mode for the disk when it is on.

The WD800 system chassis has four indicator lights on the front panel: a tape status indicator, a storage system indicator, a disk status indicator, and a test mode indicator. These lights perform three functions. Primarily, they display the operational status of the storage system. The lights can also display detected subassembly faults by toggling the TEST STATUS/TAPE UNLOAD switch up. Under certain conditions during stand-alone power-up initialization, the lights also display the unit select address.

1.2.3.4 Card Cage. The card cage contains the peripheral interface board, the processor board, the Winchester disk interface board (WD800A only), the read/write board (WD800 only), the high-speed digital board, and the servo board (WD800 only). If the chassis contains the optional tape cartridge transport subsystem, the card cage also contains the tape encode/decode board and the tape control board. A group of processes executed by these boards constitutes the formatter function of the WD800 system.

1.2.3.5 Power Supply. The WD800 chassis power supply consists of an electro-magnetic induction (EMI) filter and two power supply boards. For the power supply requirements of the WD800 chassis, see Table 3-1.

1.3 OPTIONS

The WD800 system is available with either a two-platter or a four-platter Winchester disk drive. The two-platter disk drive provides a disk storage capacity of 18.5 megabytes, and the four-platter disk drive provides a disk storage capacity of 43.2 megabytes.

The WD800A system is available with a three-platter, a five-platter, or an eight-platter Winchester disk drive. The three-platter disk drive provides a disk storage capacity of 38.4 megabytes, the five-platter disk drive provides a disk storage capacity of 69.2 megabytes, and the eight-platter disk drive provides a disk storage capacity of 114.5 megabytes.

The WD800 system kit design permits a wide variety of possible chassis configurations (Figure 1-3). At the minimum, the system consists of only one chassis with a Winchester disk drive and a magnetic tape cartridge transport installed in the chassis for backup. The maximum configuration that a single TPBI board can support consists of four daisy-chained chassis, each with a disk drive and a magnetic tape cartridge transport installed for backup.

The WD800 system also works with other peripherals. For example, you can mix WD800 and WD500/WD500A system chassis in the same system. This combination might occur when you expand the storage capacity of a smaller system by adding a WD800 system kit.

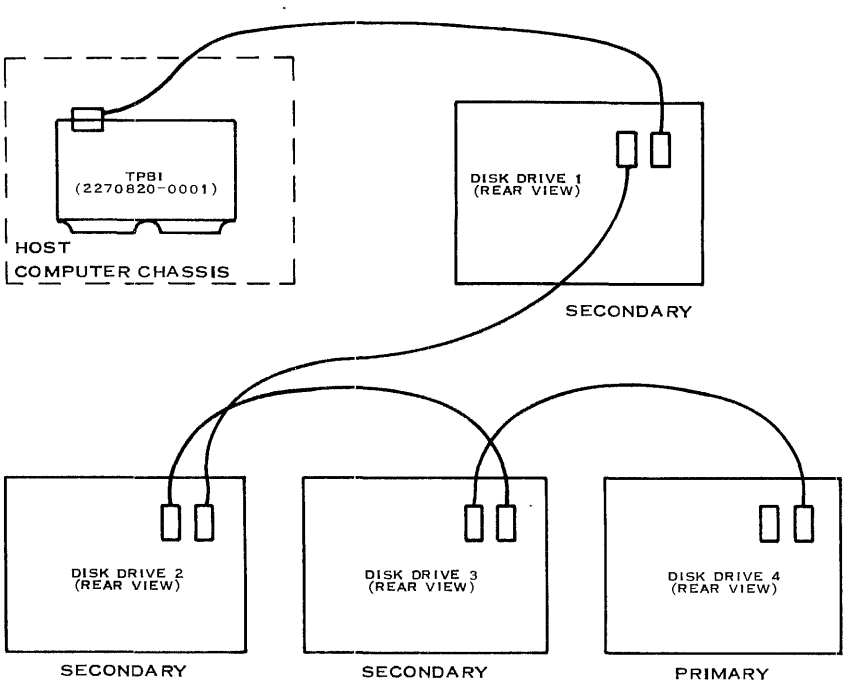


Figure 1-3. WD800 Maximum Configuration

1.4 FUNCTIONAL DESCRIPTION

The WD800 storage system consists of the host 990 system and the WD800 system. The WD800 system in turn consists of the TPBI board and the WD800 chassis with the interface cable. The WD800 chassis contains the formatter, the storage devices, and the power supply. The functioning of the WD800 storage system can be defined in terms of a series of interfaces between these component blocks.

The highest level interface connects the host system and the WD800 system. This interface is implemented by the TILINE and TPBI. Within the WD800 system, the peripheral bus interface (PBI) interconnects the TPBI and the WD800 chassis. At the lowest level, the formatter in the WD800 interprets the commands from the TPBI and controls the storage devices.

1.4.1 General

The functional diagram for the WD800 storage system (Figure 1-4) shows the series of interfaces between component blocks in the WD800 storage system.

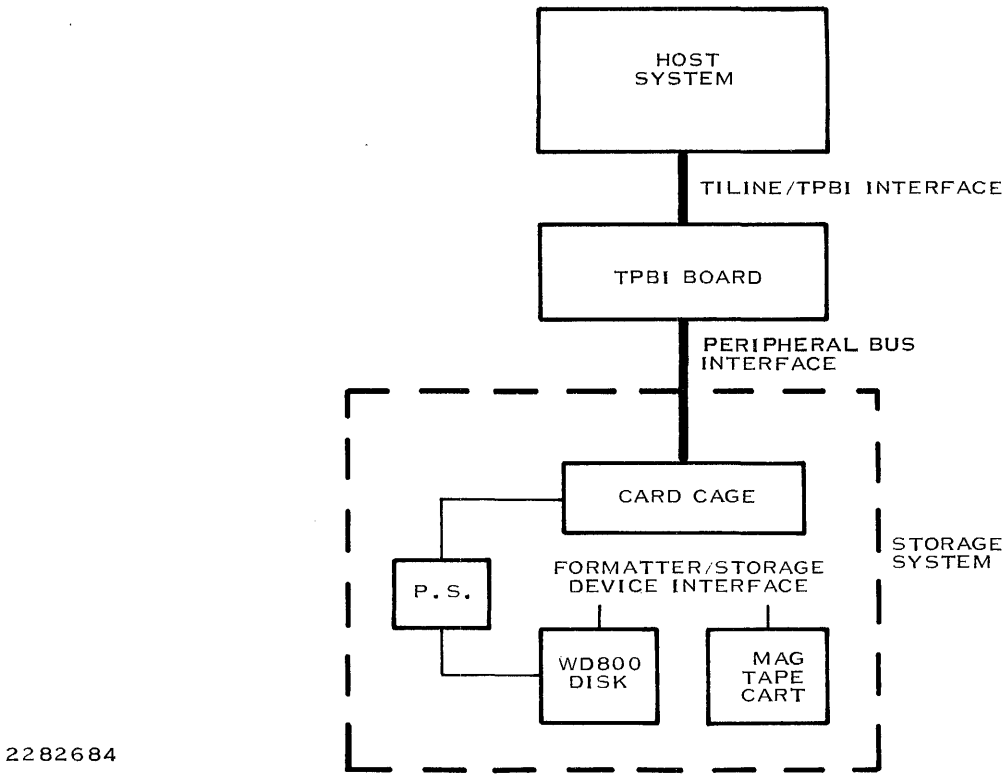


Figure 1-4. WD800 Functional Diagram

The host system issues commands to and receives status from the TPBI. The TPBI interrogates each command received from the host system and executes only those commands reserved for itself; it issues all other commands to the formatter in the WD800 system chassis. The formatter executes the commands; it also controls the storage devices.

The following paragraphs describe the elements of the host/WD800 system interface, implemented by the TILINE and the TPBI; and the TPBI/WD800 chassis interface (the PBI), implemented by the TPBI and the formatter. These paragraphs then discuss the functions of the formatter in controlling the storage devices.

1.4.2 TILINE

The TILINE is an asynchronous, 16-bit parallel data bus that transfers data between high-speed system elements such as the 990 main memory, the 990 central processing unit (CPU), and the disk drive systems. The TILINE architecture incorporates the TPBI directly into CPU addressable memory space and provides reliable, high-speed input/output (I/O) control.

Devices on the TILINE act as either masters or slaves. Master devices contend for access to and control of the TILINE; slave devices respond only when addressed by a master device. Device controllers such as the TPBI can act as either masters or slaves. Controllers act as masters when they contend for TILINE access to transfer data to or from TILINE memory; they act as slaves when they accept commands or allow status to be read from their device control registers.

1.4.3 TPBI

The TPBI is a TILINE interface device that furnishes communication between the formatter and the 990 system. The TPBI board occupies one full slot in the host 990 chassis; it uses the TILINE for host system communication and the PBI for formatter communication. The TPBI employs two sets of device control registers and two separate interrupt levels, which allow commands to be interleaved to two devices at the same time. For overlapped operations such as disk-to-tape backup, the dual-device control registers provide a significant performance improvement. While one device is writing, a second device can read, write, or seek independently without interfering with the operation in progress. Each device control register set has four device-select assignments numbered 0 through 3. Since two independent interrupt levels are provided, the overlapping disk and tape operations can signal completion without requiring elaborate software testing. For complete information on the TPBI, see Section 2 of this manual.

1.4.4 Peripheral Bus Interface (PBI)

The PBI provides the interface arrangement for the TPBI to communicate with the disk and tape cartridge. The PBI features a byte-oriented command and status structure distributed on two levels between the host and the storage device. First, the TPBI accepts a command or status request from the host TILINE and filters out those commands or requests that can be handled by the TPBI itself. The TPBI then forwards the rest of the commands and requests to the formatter in the WD800 chassis. The formatter function controls the disk drive and cartridge tape transport.

The PBI supports up to eight devices on the bus. Use of the PBI allows the computer system to be upgraded or expanded without replacing existing interface devices.

1.4.5 Formatter Function

The formatter function is performed by components distributed on several PCBs in the card cage of the WD800 chassis. The formatter subsystem consists of a microprocessor, read-only memory (ROM) and random-access memory (RAM) for resident software, RAM data storage buffers, a high-speed data transfer device, the controller interface, the disk subsystem, the tape subsystem, and the front panel controls and indicators. Functionally, the formatter is responsible for the following:

- System initialization
- Winchester disk operations:
  - — Disk head positioning
  - — Disk data encoding and decoding
  - — Disk error detection and correction by means of ECC
- Tape transport operations:
  - — Tape positioning
  - — Tape data encoding and decoding
  - — Tape error detection in both read and write operations by means of cyclic redundancy check (CRC) characters
- Status monitoring and reporting

The formatter exercises independent control of the disk drive and tape transport, thereby freeing the host system and the TPBI for other tasks.

1.4.5.1 System Initialization. The formatter function works with the TPBI to initialize the system after the TPBI confirms that the interface bus is ready. The formatter tests the bus by sending a data pattern to the TPBI and then copying it back. If no errors occur, the formatter identifies its dependent devices to the TPBI and reports their status. Normal operation of the host-to-system interface can then proceed.

1.4.5.2 Winchester Disk Subsystem Operations. The Winchester disk subsystem performs all data reading, writing, and positioning functions in response to operational commands exchanged with the formatter. The disk subsystem can be divided functionally into a positioner block, a read/write block, and an error detecting and correcting block.

Disk Head Positioning Operation. The disk drive electronics control the movement of the head carriage assembly to the desired cylinder by reading a servo surface on one of the disk platters. The WD800 disk electronics have access to the servo signal and directly control the head movement. The WD800A disk module controls the movement of the heads based on a count that is passed to it by the disk electronics.

Head selection is a part of the command parameters and determines the track on the cylinder to be accessed. The disk drive electronics also provide an index pulse and a beginning of sector indication. Command parameters that give the desired cylinder, head, and sector values are compared to the address field at the beginning of the located sector to verify that the command parameters and the field parameters correspond. A timer monitors all seek operations and reports a seek error to the host when an operation exceeds the time allowed.

Disk Read/Write Operations. The encoding system used on the Winchester disk in the WD800 is modified frequency modulation (MFM), with error checking and correction for all data and address fields transferred between the formatter and the disk.

A hardware-generated index mark occurs once each revolution. Each track is divided into 37 sectors (33 sectors for the WD800A) of 256 bytes each. Each sector contains an address field and a data field. The address field written during format commands contains a unique disk address.

Disk Error Checking and Correction. When data is read from the disk, ECC logic on the formatter examines the data and determines whether any errors occurred during the data storage process. Certain types of errors can be corrected, and if these types of errors are found, corrections are made. After an operation, the CPU can read status indicators that show whether errors occurred and whether corrections were made. If ECC is used and no status error is reported, the data transferred is guaranteed. ECC is not attempted when the burst size of the error exceeds the correction capabilities of the ECC. In such cases, data is transferred but data error status is reported.

Media Defect Handling. The WD800 and WD800A Winchester disks usually have a small number of media defects that can cause erratic system operation. These defects must be removed from the available storage area on the disk. The defects can consist of both hard and soft defects. For reliable operation all media defects must be avoided by the operating system.

Hard defects always cause an error and generally they are easily identified. Soft defects cause intermittent errors that can usually be corrected by a retry or by the hardware error-correction logic.

The WD800 relies on a track deallocation algorithm that is supported by the TI DNOS and DX10 operating systems. The operating system can deallocate up to 64 bad tracks by listing them in a special bad track map.

The WD800A reserves ten cylinders as spare track locations. The bad tracks are reallocated to these ten cylinders. You can build a bad track list either by surface analysis or by operator entry of the known media defects. Use the surface analysis procedure to reallocate as many bad tracks as possible to the spare track locations. The bad tracks that are not reallocated to the spare track locations remain deallocated.

A list of bad tracks is built in either of the following two ways:

- By performing a surface analysis using the IDS utility, the disk build utility, or the DOCS DSKSA diagnostic (SA verb).
- By entering the known media defect locations when you use the IDS utility, the disk build utility, or the DOCS DSKSA diagnostic (FC verb).

Typically, a list of known media defects are attached to the top of the disk drive. The list identifies the location of the defect by its cylinder and head number.

1.4.5.3 Tape Transport Operations. The storage system uses a 3M DC300XL cartridge tape. The DC300XL provides 137.16 meters (450 feet) of recordable tape on four tracks for an unformatted capacity of over 17 megabytes if 9600 byte records are used. For the DC300XL, formatted capacities of over 14 megabytes can be achieved with 9600-byte records, as provided in the DX10 or DNOS backup directory operations (using the block mode option of the Backup Directory command.) The use of smaller records reduces the formatted capacity of the tape cartridge.

The take-up hubs eliminate handling the tape itself and protect it from damage and contamination. One access opening allows the drive motor capstan to contact an internal belt capstan for moving the tape across the heads. Internal tape guides position the tape on the drive heads. A pivot-action door permits the drive heads to access the tape when the cartridge is inserted in the drive.

A slotted plug on the upper left corner of the cartridge can be oriented in one of two positions for either safe (write-protected) or unprotected operation. Note that the tape is write-protected only by this plug; the WRITE-PROTECT switch on the front panel applies only to the disk and does not apply to the tape. Tape position is determined by a pattern of holes that identifies the beginning-of-tape (BOT), end-of-tape (EOT), load point, and early warning for EOT.

Tape Positioning Operations. The tape can move in either the forward or reverse direction. During certain operations, it advances directly to the physical ends of the tape (BOT or EOT) at high speed (2286 millimeters per second/90 inches per second). The high-speed positioning operations include tape load (which includes an end-to-end tensioning of the tape), rewind, and unload. Read and write operations (including write forward, write end-of-file, and erase) take place at a much slower speed (723 millimeters per second/30 inches per second), as do the record skip (forward and reverse) operations. Track switching for read, write, and skip operations is accomplished at high speed. Operating at high speed, full tape positioning can be done within one minute. Operating at the slower speed, it takes three minutes for the same operation.

Tape Read/Write Operations. The tape uses an MFM encoding scheme for data. Unlike the disk, the tape does not use ECC. Instead, tape records are divided into 256-byte data blocks, each with CRC error detection. Very large media flaws (sometimes up to 200 bits long) are more likely on tape; such flaws exceed the capability of conventional ECC.

The tape is a sequential access device; thus tape records are written from the beginning of the tape each time a tape cartridge is installed. The tape records consist of a concatenation of 256-byte data blocks. In addition to CRC characters, each data block includes header information. Write operations feature read-after-write error detection with high analog thresholds to guarantee data written. Record boundaries consist of erased interrecord gaps (IRGs), typically 32 millimeters (1.26 inches) long, between records. Artificial file-mark boundaries can also be written on tape by a write end-of-file (EOF) command. Typically, an EOF record marks the end of data. Otherwise, writing to the end of the last track will force an EOT error.

Reading the tape, like writing it, starts at the beginning of the tape. Read operations report either EOF or EOT records to inform you when you have reached the end of recorded data on the tape.

Tape Error Checking and Recovery. Errors detected by CRC in reads or writes to tape must be recovered by host retries. A retry of read or write errors consists of a record skip reverse operation followed by a retry of the command that reported the error. Errors reported in read or write operations due to track switching (repositioning the tape to the beginning of the next data track) require a rewind delay followed by a retry of the aborted command.

1.4.5.4 Status Monitoring and Reporting. The formatter function is also responsible for monitoring the disk drive and tape transport and reporting the status of these devices. The formatter returns the status information to the TPBI where it can be read by the host.

1.5 SPECIFICATIONS

Table 1-2 lists the system specifications for the WD800/WD800A mass storage systems.

Table 1-3 lists the specifications for the disk subsystem. The WD800 is offered with two- or four-platter disks, and the WD800A is offered with three-, five-, or eight-platter disks.

Table 1-4 lists the specifications for the tape subsystem.

Table 1-2. WD800 Mass Storage System Specifications

Power Specifications

Chassis ac power:	WD800	WD800A (typical)
120 Vac ± 10% 50 or 60 Hz ± 3 Hz	3.0 A running 8.0 A starting (for 10 sec)	1.6 A running 2.5 A starting (for 10 sec)
or		
220 or 240 Vac ± 10% 50 Hz ± 3 Hz	1.5 A running 4 A starting (for 10 sec)	1.2 A running 1.6 A starting (for 10 sec)
TPBI dc power (from host chassis power supply)	5.0 ± 0.25 Vdc at 3.0 A (maximum)	

Environmental Specifications[1]

Operational:[2]	
Ambient temperature	10 to 40 ° C (50 to 104 ° F) with a temperature gradient less than 10 ° C (18 ° F) per hour
Relative humidity	
WD800	20% to 80% without condensation
WD800A	10% to 80% without condensation
Altitude	0 to 3000 m (0 to 9843 ft)
Nonoperational:	
Ambient temperature	– 40 to 60 ° C (– 40 to 140 ° F) with a temperature gradient less than 20 ° C (36 ° F) per hour
Relative humidity	
WD800	10% to 80% without condensation
WD800A	10% to 95% without condensation
Altitude	
WD800	0 to 12 000 m (0 to 39 372 ft)
WD800A	0 to 3000 m (0 to 9843 ft)

Physical Specifications

Length	68.6 cm (27 in)
Width	48.3 cm (19 in)
Height	22.2 cm (8.75 in)
Weight (maximum)	
WD800	38.5 kg (85 lb)
WD800A	31.3 kg (69 lb)

Notes:

[1] Environmental specifications represent worst-case conditions as determined by the most sensitive components in the storage system.

[2] Lower these temperatures by 2 ° C (3.6 ° F) for every 762 m (2500 ft) increase in altitude above mean sea level.

Table 1-3. Disk Subsystem Specifications

Performance Specifications

Capacity:

WD800:

	Two Platters	Four Platters
Unformatted data	22.3M bytes	52.1M bytes
Formatted data*	18.5M bytes	43.2M bytes
Allowance for factory media defect deallocation	189K bytes	397K bytes
Formatted data with maximum tracks deallocated	18.3M bytes	42.8M bytes

WD800A:

	3 Platters	5 Platters	8 Platters
Unformatted data	48.1M bytes	86.7M bytes	143.4M bytes
Formatted data	38.4M bytes	69.2M bytes	114.5M bytes

Disk-to-PBI burst transfer rate:

WD800	0.67M byte/s maximum
WD800A	0.80M byte/s maximum

Rotational latency:

	WD800	WD800A
Average	8.3 ms	8.3 ms
Maximum	17.1 ms	16.7 ms

Seek time (includes settling time):

Track-to-track	9 ms	8 ms (3- & 5-platter) 5 ms (8-platter)
Average	45 ms	35 ms (3- & 5-platter) 30 ms (8-platter)
Maximum	70 ms	85 ms (3- & 5-platter) 48 ms (8-platter)

Functional Specifications

Spindle speed	3600 rpm	3600 rpm
Speed variation	±3.5%	+0.5%, -1.0%
Track density	478 tpi	960 tpi (3- & 5-platter) 980 tpi (8-platter)

r)

Table 1-3. Disk Subsystem Specifications (Continued)

Cylinders:

	Total Cylinders	Available Cylinders	Reserved Cylinders
WD800:			
2-platter	657	651	Six reserved for storage system use (including two for diagnostics)
4-platter	657	651	
WD800A:			
3-platter	925	911	Four reserved for storage system use (including two for diagnostics); ten reserved to replace bad tracks
5-platter	925	911	
8-platter	918	904	

Data surfaces:

	WD800	WD800A
	3 (2-platter) 7 (4-platter)	5 (3-platter) 9 (5-platter) 15 (8-platter)
User accessible tracks	1953 (2-platter) 4557 (4-platter)	4555 (3-platter) 8199 (5-platter) 13,560 (8-platter)
Tracks reserved for defect mapping	None	50 (3-platter) 90 (5-platter) 150 (8-platter)
Sectors per track	37	33
Data bytes per sector	256	256
Total bytes per sector	313	313
Sectoring method	Hard Servo-referenced (fixed length)	Soft Servo-referenced
Encoding method	MFM	MFM
Spindle drive motor	AC induction 1/12 hp; 50/60 Hz capacitor start thermally protected	Brushless DC

Table 1-3. Disk Subsystem Specifications (Continued)

Reliability Specifications

Error rate:	
Recoverable	Less than 1 in 10^{10} bits
Nonrecoverable	Less than 1 in 10^{12} bits
Positioning	Less than 1 in 10^{6} bits

Note:

* Formatted data capacity is the maximum data storage capacity available before bad track data are subtracted. Each WD800 Winchester disk drive can have up to 20 (2-platter) or 42 (4-platter) bad tracks (media defects) when the unit ships from the factory. WD800A factory reallocated tracks are transparent to the user.

Table 1-4. Tape Subsystem Specifications

Performance Specifications

Burst transfer rate	192K bits (24K bytes) per second
Capacity:	
137 m (450 ft)	14.6M bytes (9.6K bytes/record) 3.9M bytes (256 bytes/record)
Access Time:	
Stop/start	25 ms at 762 mmps (30 ips)
Rewind:	
137 m (450 ft)	1 min at 2286 mmps (90 ips)
Read/write:	
137 m (450 ft)	3.4 min/track at 762 mmps (30 ips) continuous using 9.6K-byte records

Table 1-4. Tape Subsystem Specifications (Continued)

Functional Specifications	
Tape Speed	762 mmps (30 ips) (recording/playback) 2,286 mmps (90 ips) (rewinding/unloading)
Heads	4 tracks serial read-after-write with selectable track erase
Media:	
TI Part No. 2270391-0001	DC300XL cartridge 137.16 m long, 0.064 mm wide (450 ft long, 0.25 in wide)
Recording Specifications	
Packing density	252 bpmm (6400 bpi)
Recording code	MFM
Reliability Specifications	
Error rate*	
Recoverable	$\leq$ 1 in 10^8 bits
Nonrecoverable	$\leq$ 1 in 10^9 bits

Note:

* Errors are detected by CRC. Error recovery is achieved by retries and low read recovery thresholds.

2

TILINE Peripheral Bus Interface

2.1 GENERAL

The Texas Instruments TILINE Peripheral Bus Interface (TPBI) provides a 990 family-compatible TILINE interface to a mass storage system. The TPBI supports both disk and tape mass storage units over a byte-oriented peripheral bus. The TPBI supports two sets of eight-word slave registers and two interrupts to the host computer in a single card slot. The TPBI maintains software compatibility with previous tape and disk mass storage devices.

System features include the following:

- Single circuit board 990 TPBI
- Conformance to peripheral bus standards as a bus controller
- Usability with 990 TILINE computer systems
- Extensive on-board self-test
- Two sets of TILINE peripheral control space (TPCS) registers
- Two TILINE interrupts
- FCC compliance

Figure 2-1 shows a block diagram of the TPBI.

The TPBI board (Figure 2-2) occupies one full slot in the 990 chassis and provides communication between formatters in the mass storage systems and the host 990 system. The TPBI uses the TILINE bus for host system communication and the peripheral bus interface (PBI) for formatter communication. The TPBI transmits data and commands from the host system to the formatters, which then interpret and execute the data and commands.

2.1.1 System Operational Description

The following paragraphs describe how the TILINE, TPBI, and peripheral bus interact with the 990 computer to provide online data storage functions. Figure 2-3 is a block diagram that shows system interconnections.

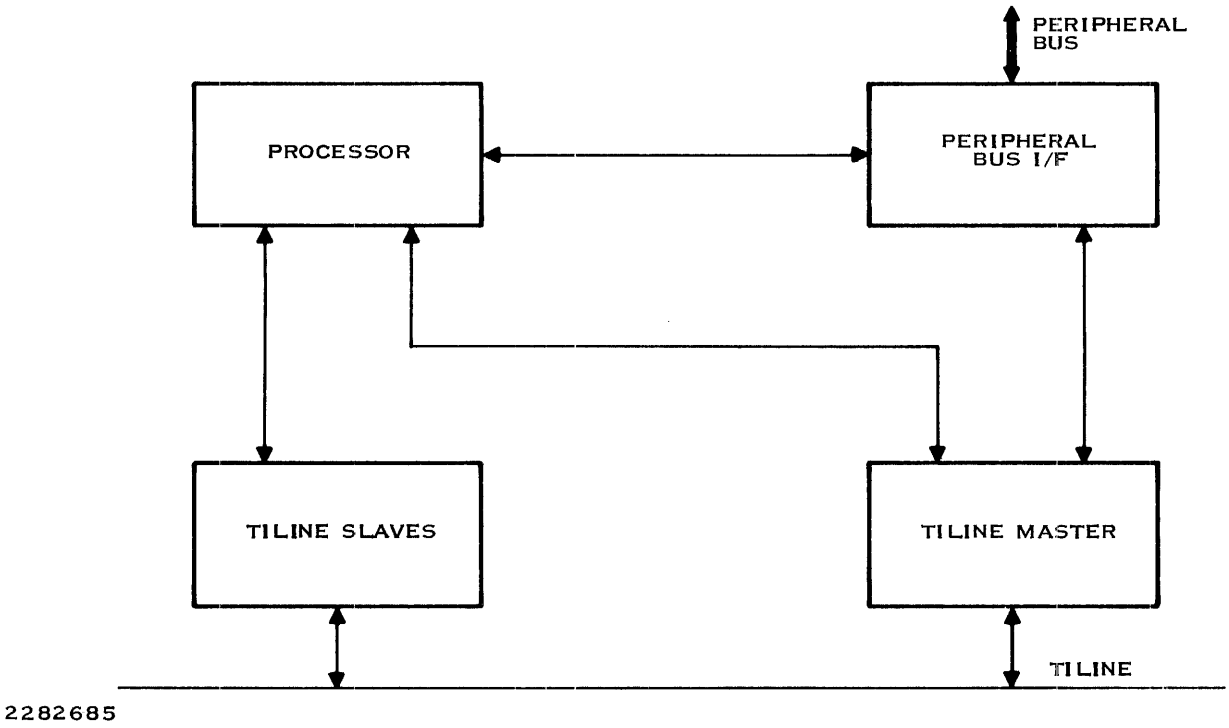


Figure 2-1. TPBI Block Diagram

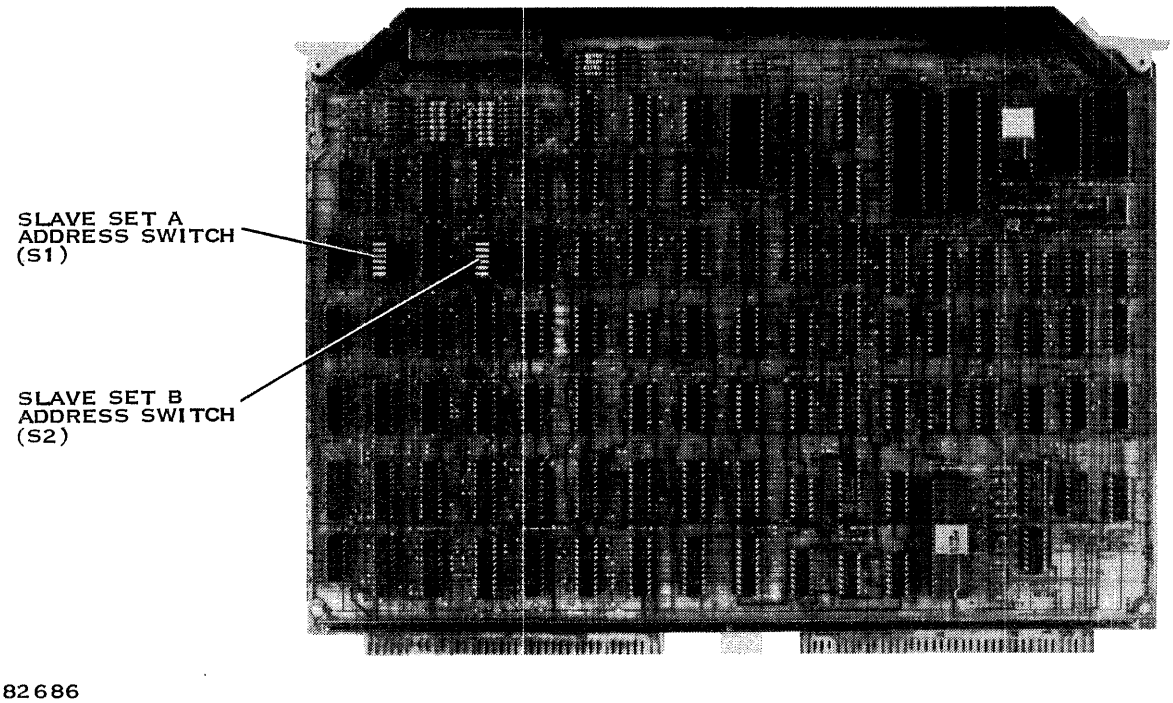


Figure 2-2. TPBI Board

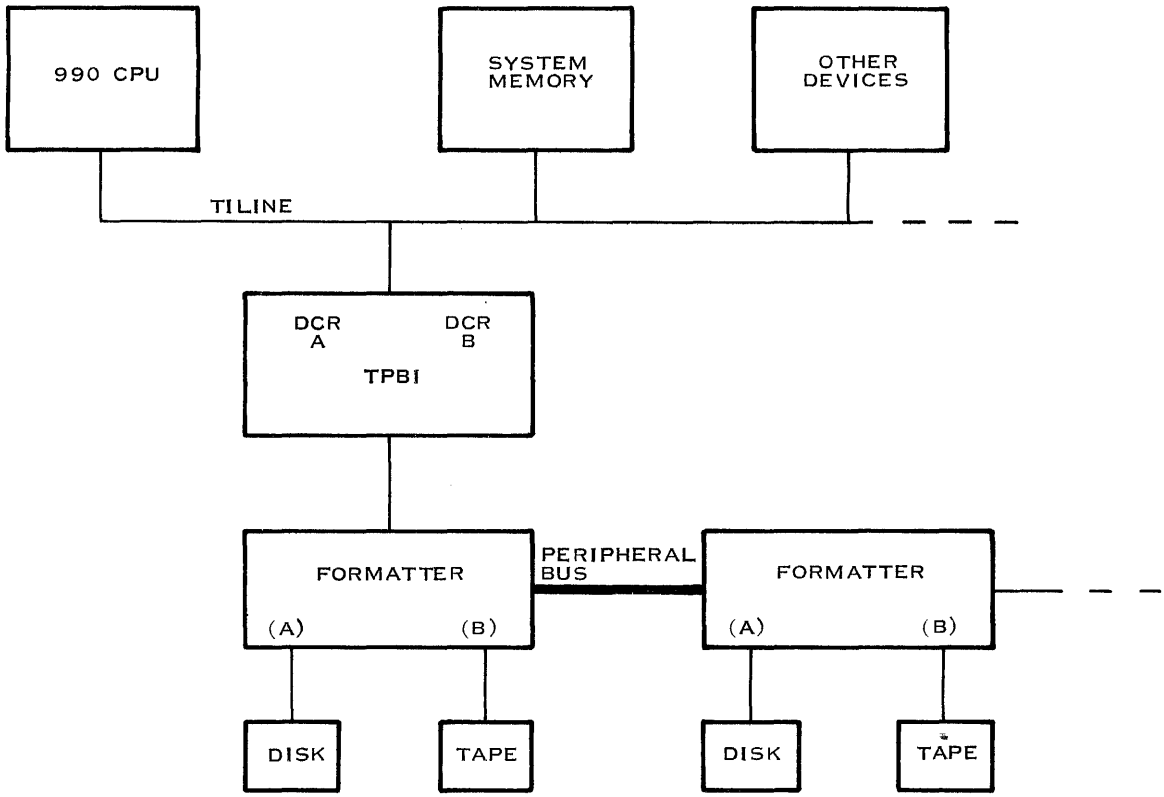


Figure 2-3. Mass Storage System Using TPBI as 990 Interface

2.1.2 TILINE

The TILINE is an asynchronous, 16-bit parallel data and 20-bit address bus that transfers data between high-speed system elements such as the 990 main memory, the 990 central processing unit (CPU), and disk drive systems. The TILINE bus architecture incorporates the TPBI interface registers directly into CPU addressable memory space and provides reliable, high-speed I/O control. Devices on the TILINE act as either masters or slaves. Master devices contend for access to and control of the TILINE, while slave devices respond only when addressed by a master device. The TPBI acts alternately as a master and slave.

2.1.3 TPBI Operations

The TPBI operates as a slave device when receiving commands from the CPU or when the CPU reads controller status. These commands direct TPBI operations and are written into TILINE memory addresses assigned to the TPBI. After a command completes, the TPBI provides status information in these same TILINE locations, which the CPU reads to obtain command completion status. While executing a command, the TPBI functions independently of the CPU. The CPU cannot write to a slave set while it is executing a command, but the CPU can query that slave set's BUSY/IDLE status to determine when the command completes. While one slave set is busy with a command, the CPU can still read or write to the other slave set. The two slave sets on the TPBI appear totally independent to the CPU.

After a command is initiated, the TPBI can be required to act as a TILINE master to access or store data in TILINE memory. Each word of data transferred to or from TILINE memory requires a separate access to the TILINE. The TPBI contends for TILINE access on a positional priority basis by cycle-stealing with the CPU and with other active TILINE master devices. After obtaining TILINE access, the TPBI transfers a 16-bit parallel data word to or from the slave it addressed, which in most cases is a computer memory board. In addition, the TPBI manipulates all of the PBI data and control lines that enable data transfer between the TPBI and the formatter.

2.1.4 Peripheral Bus Interface

The PBI provides an interface arrangement for a controller (TPBI) to communicate with different types of mass storage devices. The PBI features a byte-oriented command and status structure that is used to control and monitor the devices. Use of the PBI allows upgrading or expanding a computer system without replacing existing interface devices.

In systems using the PBI, device control resides in the formatter. The TPBI passes device operation commands to the formatter. The formatter interprets the command, initiates action according to the program contained in its firmware, monitors the device operation, and reports completion status.

The PBI allows a maximum of eight devices on the bus. TPBI constraints require that if more than four devices of the same type (that is, disk or tape) are used, then no other type device can be used on the same bus. If both tape and disk devices are both used, no more than four disks and four tapes can be used. The first storage system chassis is connected to the host system with a 40-pin shielded cable. Identical cables are used in a daisy chain from chassis to chassis if additional chassis are required.

2.2 TPBI PROGRAMMING

This paragraph contains information for programming assembly language routines that only use the TPBI. For programming the mass storage system, refer to paragraph 3.3. The programmer must be familiar with assembly language as described in the *Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual*.

Most users prefer Texas Instruments standard operating system software, including device service routines (DSRs). This software features standardized file manipulation schemes that are essentially independent of I/O device type. If you want this standard software, refer to the applicable operating system reference manual. If you want to perform direct disk I/O operations without using a standard operating system DSR, you can initiate disk commands and receive disk status as described in this section and in paragraph 3.3. An example DSR appears in Appendix C.

This paragraph is organized into following three basic parts:

1. A discussion of communication between the storage system and the host system using the TILINE.

2. Basic programming of the TPBI intercepted commands. Those commands passed directly to the formatter are described in Section 3.

3. A listing and definition of extended commands.

2.2.1 TILINE Communication

The TILINE links the 990 processor, memory boards, and high-speed peripheral controllers such as the TPBI. The TPBI is assigned two blocks of eight TILINE addresses. The 990 processor communicates with the TPBI by writing 16-bit command words into one of these blocks. After a command completes, the TPBI replaces the control words with status words. The 990 processor then reads the status words to determine command completion and device status. TPBI operations are initiated when control words containing command parameters are written into the TILINE addresses (slave registers) that are assigned to the TPBI. After initialization, the TPBI acts independently of the 990 processor and transfers data between specified TILINE memory locations and the formatter, as required. Any computer instruction that reads or modifies general memory can be used to communicate with the TPBI slave registers.

2.2.2 TILINE Peripheral Control Space Addressing

The TILINE address range from >FFC00 to >FFDFF is reserved for the command and status communication blocks of TILINE peripheral controllers, such as the TPBI. This range of addresses is called the TPCS and it is accessed by any TILINE master device that can generate addresses in this range. Model 990 Computer logical byte addresses >F800 to >FBFF are mapped by the processor hardware to TILINE addresses in the range >FFC00 to >FFDFF, if the 990 processor is operating either unmapped or in map file 0. The TPCS is also addressed through alternate map files if the mapping bias value is chosen to yield the correct TILINE address. This programmable mapping feature is standard on some 990 CPUs and optional on others.

NOTE

A value preceded by a right angle bracket (>) indicates a hexadecimal value.

The physical TILINE bus includes 20 address lines; however, each CPU byte address consists of 16 bits. When a CPU byte address falls within the TPCS, all ones are loaded automatically into the upper five bits of the TILINE address, and the least significant bit (LSB) is dropped. (This LSB is a byte selector used only within the CPU.) The remaining 15 bits form the lower 15 bits of the TILINE address. Figure 2-4 shows the conversion of a 16-bit CPU byte address to a 20-bit TILINE word address. One way to visualize this conversion is to think of a 21-bit TILINE *byte* address of >1FF800 that loses its LSB (byte selector) to become TILINE *word* address >FFC00. The 1F comes from the five ones and the >F800 comes from the original CPU byte address. The only part of this address accessible to the programmer is the CPU byte address, >F800.

Each of the two address blocks assigned to the TPBI range from an independently switch-selectable base address to base address plus seven word addresses. In this document, consecutive words of each block starting from the base address are designated word 0 (W0) through word 7 (W7).

Each base address is selected by a six-section switch on the TPBI board. Base address selection is coordinated with the operating system software during system hardware configuration and software system generation. Refer to paragraph 2.3.4 for instructions on setting the base address switches.

The TPBI is capable of communicating with TILINE memory in any range of the TILINE address space.

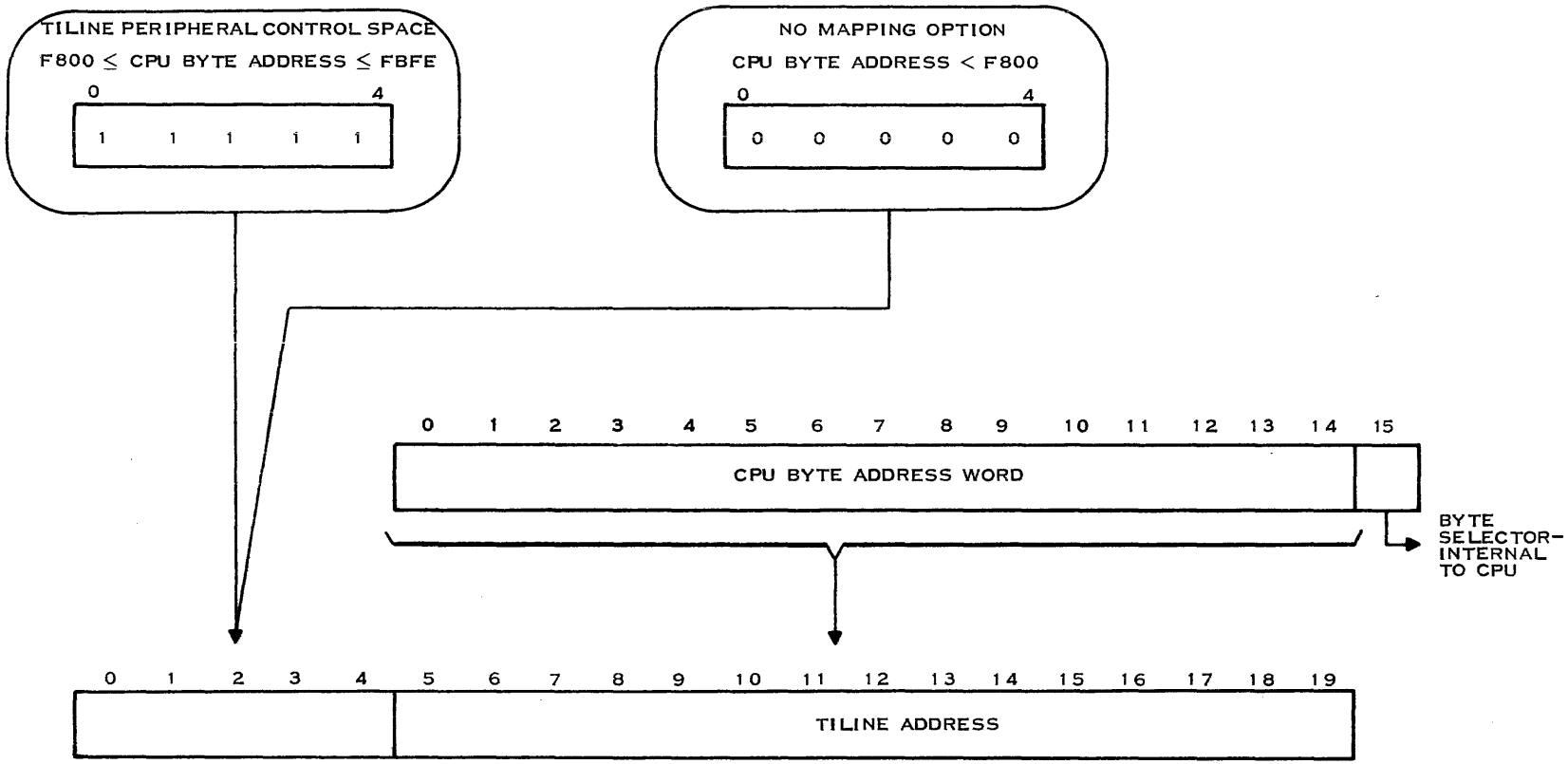


Figure 2-4. Relationship Between TILINE Address and CPU Byte Address

2.2.3 TPBI Command and Status Structure

The host CPU uses two independent sets of eight control and status words to communicate with the TPBI for system operation. To initiate a system operation, the program loads control words into one of the two sets of control and status word registers assigned to the TPBI. The order in which control words are loaded is not important except that W7 must be last. Operation initiates immediately when bit 0 of W7 is set to zero.

Transmitting a new set of control words to the TPBI wipes out the status words from the previous operation, except for the unit status fields of W0 (bits 0 through 11) that the formatter or TPBI set and that the host CPU cannot overwrite. If overwriting is attempted, the TPBI ignores bits placed in W0 status fields.

Before writing a command to the TPBI registers, the host first checks W7, bit 0 to verify that the TPBI is idle and will accept the command. If W7, bit 0 is set (TPBI idle), the host writes the command to the TPBI registers.

If the host attempts to send a control word to a TPBI slave set that is busy executing a command, the attempt appears to the TILINE to complete normally, but the contents of the addressed word do not change.

2.2.4 Command Completion

An interrupt enable bit in W7 allows the programmer to specify whether the TPBI generates an interrupt to the host upon completion of an operation. The TPBI is used with either an interrupt-driven or a polled DSR. The following paragraphs discuss these options.

2.2.4.1 Command Completion Without Interrupts. To determine command completion or TPBI availability in a polled system, periodically read status W7 and check bit 0 for idle status. A logic zero in this position indicates that the TPBI is busy; a logic one indicates that the TPBI is idle and available for commands.

Usually, the program initiates a timing loop when TPBI operation begins and checks the idle bit at timer expiration. If the idle bit is still zero, the timer restarts and the sequence repeats a preselected number of times. This method requires more program overhead than the interrupt-driven approach.

For disk units, if a seek or restore command is initiated, the disk may not be ready after the TPBI reports completion. To determine if a disk completed a seek or restore motion, the program checks the drive status bits of W0. If the disk drive completed its operation, the attention line for the selected drive is set and either the not ready bit is inactive, or the seek incomplete bit is set.

For tape units, the rewind bit for each unit is a logic one when that unit is rewinding.

2.2.4.2 Command Completion With Interrupts. The TPBI can issue two types of interrupts to the computer for each slave set. One type of interrupt is issued when the TPBI completes any command. The other type is issued when the disk drive completes an independent seek or restore operation or when the tape unit completes an independent rewind operation.

Command Completion Interrupts. For the TPBI to issue an interrupt to the 990 processor upon command completion, the interrupt enable bit in W7 must be set when the operation is initiated. When the TPBI returns to idle, the interrupt is issued to the host CPU. This interrupt is cleared by resetting the interrupt enable bit or the appropriate completion bit in W7.

Seek or Rewind Completion Interrupts. Control word 0 (W0) contains four attention bits (one for each of the drive units) and four attention mask lines. Each attention bit is set when the drive is either ready or offline. When the attention bits and mask bits for any drive unit are both set and the TPBI slave set is idle, the interrupt line to the computer is also set.

For tape units, the rewind bit clears when a rewind operation completes.

To use the drive completion interrupts during either an independent seek or restore operation for disk or a rewind operation for tape, first issue the command to the TPBI. After the TPBI reports command completion (by a TPBI command completion interrupt), set the mask bit corresponding to the desired drive. When that drive finishes the operation and the TPBI is idle, an interrupt is issued to the host CPU. This interrupt is cleared by resetting the mask bit corresponding to the interrupting drive. All TPBI interrupts are disabled while the TPBI is busy, and a reset to the TPBI resets all the mask bits.

2.2.5 TPBI Disk Control and Status Word Formats

This section describes only the control and status words intercepted by the TPBI during disk operation. Refer to Section 3 for a description of the control and status bits used for control of the drive units in the storage system chassis. As described earlier, the CPU can write control words into the TPBI slave registers to initiate operations. The CPU can also read status words in these same slave registers to determine disk status after an operation completes. Some bits in the words are used only for disk operation control, some are used only for status reporting, and some are used for both control and status. Figure 2-5 shows the complete set of disk status bits.

2.2.5.1 W0 — Attention. This word contains the attention and attention mask bits.

Attention Lines — W0, Bits 8 Through 11. TPBI controls these bits which indicate the current seek or restore status of the indicated drive. If a unit is seeking, its attention bit is zero; if it is not seeking, the attention bit is one. The attention bits derive from the individual unit status returned from the formatters as follows:

- If the not ready bit is active and the offline bit is inactive, the attention bit is inactive. Otherwise, the attention bit is active.
- The TPBI sets all the attention bits active on power-up and changes them when the formatter sends unit status. These bits are read-only for the host.

Attention Interrupt Mask (0 Through 3) — W0, Bits 12 Through 15. Bits 12 through 15 are normally under host control, but are set inactive both on power-up and as a result of a reset to the TPBI. These bits form a position-coded attention interrupt mask, so that the assigned disk unit can interrupt the host on completion of an independent seek or restore. An interrupt to the 990 processor occurs if the attention mask bit and the corresponding attention bit are both set and that slave set is idle.

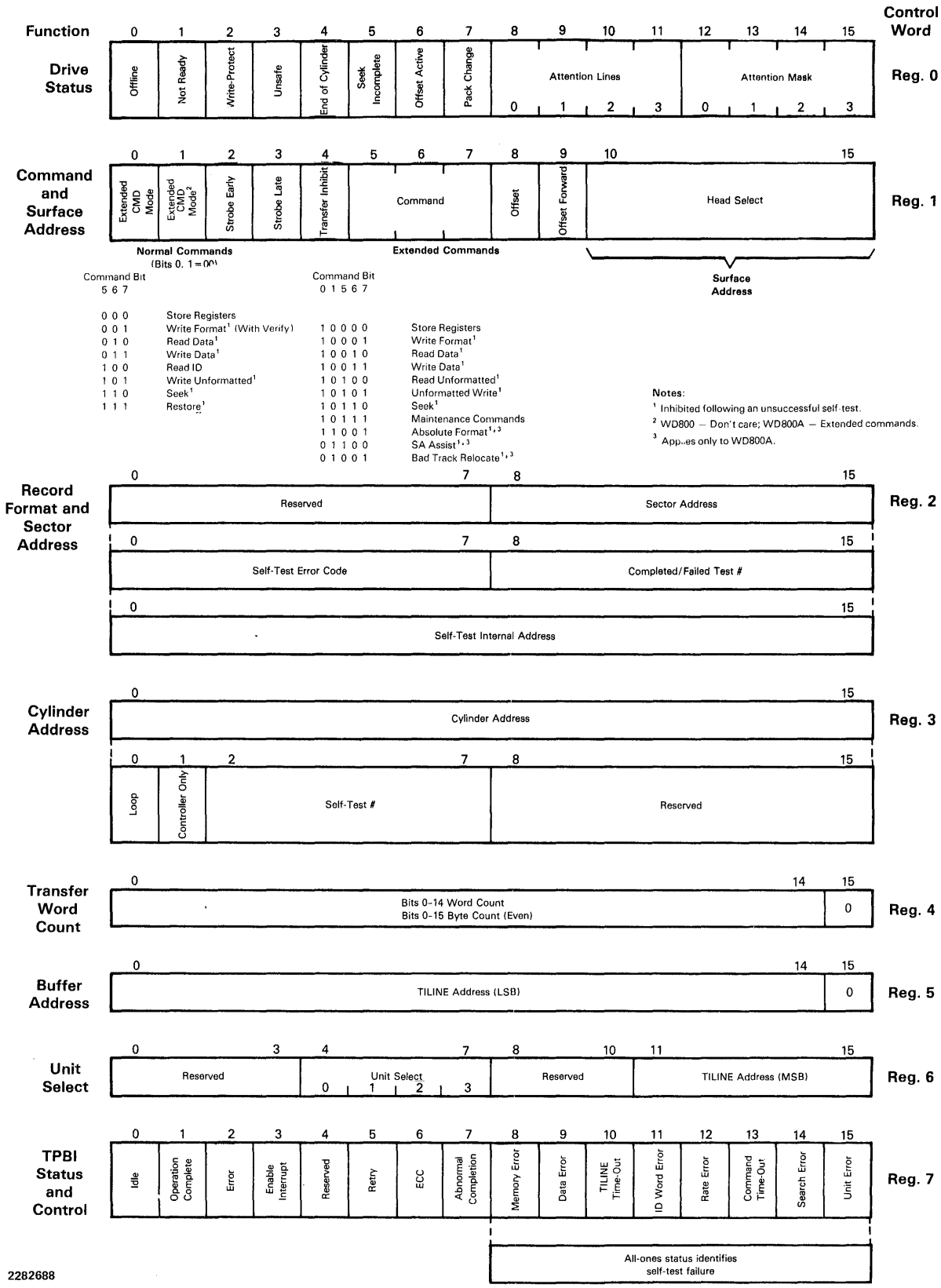


Figure 2-5. Disk Control and Status Word Formats

If multiunit operations are to overlap, the control words for subsequent operations cannot alter the attention mask, which can cause the loss of the seek or restore interrupts. Instead of using a move (MOV) instruction to write a whole new value into W0, the programmer can use some read-modify-write operation such as a set ones corresponding (SOC) or set zeros corresponding (SZC) instruction to modify bits of W0 as needed.

Since there are two possible causes for an interrupt to the CPU, do not assume that the first interrupt after initiating a restore command is an attention interrupt.

2.2.5.2 W1 — Commands. This word contains the disk command codes.

Extended Mode — W1, Bits 0 and 1. These bits are under host control. The three command code bits (W1, bits 5 through 7) allow up to eight unique commands. The extended mode bits (bits 0 and 1) are interpreted as additional command code bits, increasing the number of possible command codes to 32. If these extended mode bits are zero, bits 5 through 7 are interpreted as normal commands. These are the most commonly used commands, such as read data, write data, and store registers. If the extended mode bits are not zero, bits 5 through 7 are interpreted as extended mode commands. Refer to paragraph 3.3.4.2 for more information concerning extended mode commands.

Command Codes — W1, Bits 5 Through 7. Table 2-1 lists the normal and extended mode codes and the command names. Detailed command word descriptions and examples are given in paragraph 3.3.4. Normally, the TPBI passes all commands directly to the formatter. The TPBI performs maintenance commands (>87) if W3, bit 1 (controller only) is set. Maintenance commands are identical to the tape maintenance commands described in paragraphs 2.2.6.3 and 3.3.6.4.

Table 2-1. Command Codes

Extended Mode Bit 0	Extended Mode Bit 1[2]	Command Code Bit 5	Command Code Bit 6	Command Code Bit 7	Command
0	0	0	0	0	Store registers
0	0	0	0	1	Write format[1] (with verify)
0	0	0	1	0	Read data[1]
0	0	0	1	1	Write data[1]
0	0	1	0	0	Read ID
0	0	1	0	1	Write unformatted[1]
0	0	1	1	0	Seek[1]
0	0	1	1	1	Restore
1	0	0	0	0	Store registers
1	0	0	0	1	Write format[1]
1	0	0	1	0	Read data[1]
1	0	0	1	1	Write data[1]
1	0	1	0	0	Read unformatted[1]
1	0	1	0	1	Write unformatted[1]
1	0	1	1	0	Seek[1]
1	0	1	1	1	Maintenance commands
1	1	0	0	1	Absolute format[1,3]
0	1	1	0	0	Surface analysis assist[1,3]
1	1	0	0	1	Bad track relocate[1,3]

Note:

[1] Inhibited following an unsuccessful self-test.

[2] WD800 — don't care; WD800A — extended commands.

[3] Applies to WD800A only.

2.2.5.3 W2 — Self-Test Errors. This word contains the self-test error codes and failed self-test numbers.

Self-Test Error Code — W2, Bits 0 Through 7. This field contains an error code value produced by a self-test failure report.

Self-Test Failure Number — W2, Bits 8 Through 15. This field contains the failed self-test number if either the TPBI or the formatter reports a self-test failure status.

2.2.5.4 W3 — Maintenance Commands. This word specifies the maintenance commands.

Maintenance Command Specification Field, Bits 0 Through 7— W3. When the extended most significant bit (MSB) (W1, bit 0) is set and the primary command field (W1, bits 5 through 7) is all ones, W3, bits 0 through 7 are used as a maintenance command field. In this mode, the bits are defined as follows:

- Bit 0 — Loop bit. Setting this bit causes the specified self-test command to repeat until a reset is received. This function provides a scope loop capability for the system.

- Bit 1 — Controller only. Setting this bit causes the controller to intercept the specified command.

- Bits 2 through 7 — These bits specify an individual maintenance command to be performed. Maintenance commands for the TPBI are described in paragraph 2.2.6.3 and in Table 2-2. The TPBI maintenance commands can be issued either as disk or tape commands.

2.2.5.5 W4 — Transfer Byte Count. W4 supplies the byte count parameter from the host to the TPBI and the formatters. Formatters use this parameter to determine the number of bytes of data that are to be read from or written to the disk. For maintenance commands, this word serves as a byte count register. The formatter updates this field to indicate the remaining TILINE transfer count following data transfer operations. The TPBI uses this field to determine how many bytes of data to transfer during execution of maintenance commands. The TPBI limits any data transfer to or from TILINE memory to the count specified in this word.

2.2.5.6 W5 — Memory Address (LSB). This word supplies the least significant 15 bits of a TILINE starting address from the host to the TPBI. The TPBI ignores the LSB of this word (bit 15). The five MSBs are located in W6. If no faults occur, the address in these words is the ending TILINE memory address following command completion. If a memory error causes termination of a command, the address in this word indicates the byte address of the memory error plus two, because the TILINE address increments once before the memory error terminates the operation.

2.2.5.7 W6 — Unit Select and Memory Address (MSB). W6 contains the unit select bits and the MSBs of the TILINE buffer memory as described in the previous paragraph.

Unit Select — W6, Bits 4 Through 7. Bits 4 through 7 are a position-coded unit select field. Only one bit position in this field is set to one. The TPBI aborts any command that contains zero or multiple ones with the offline and unit error status bits set.

A time delay of up to 100 microseconds is required after the unit select field is changed before the status information in register 0 is valid for the new unit. The valid unit select codes are as follows:

W6, Bit				
4	5	6	7	Unit Selected
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3

Memory Address (MSB) — W6, Bits 11 Through 15. This field supplies the five MSBs of the 20-bit TILINE memory buffer starting address to the TPBI. The TPBI updates this field following data transfer operations to reflect the address following the last TILINE address accessed. Refer to the W5 description for additional information.

2.2.5.8 W7 — Command Completion Status. W7, as a control word, sets the interrupt enable bit (if desired) and sets the idle/busy bit that initiates TPBI operation. This word holds TPBI status at the end of an operation. Bits 8 through 15 report storage system status after a command executes. Valid error information is contained when the error bit (W7, bit 2) is set. If bits 8 through 15 are all set, a self-test failure has been detected. If the next command after a self-test failure involves a drive operation, bits 8 through 15 do not clear and the operation is inhibited. An I/O reset or power reset clears the status logic and performs a self-test.

Idle — W7, Bit 0. Bit 0 is under both host and TPBI control. The host can read or write into the registers when bit 0 is idle (bit 0 = 1). If the host reads any register while the idle bit is inactive, the register contents are provided; but the MSB of the register returned is always zero, regardless of the actual state of this bit in the register.

The host sets this bit to zero to activate any command. The command is specified by W1, bits 5 through 7. The TPBI sets this bit to one when command execution completes, either normally or as a result of an error condition. The TILINE interrupt for each slave set is active only when this bit is active.

Complete — W7, Bit 1. The TPBI sets the complete bit upon error-free completion of a command. The programmer can reset this bit as part of the interrupt service or status checking routine, or when the next block of control words is sent to the TPBI. Setting this bit to zero clears the command complete interrupt, if enabled by bit 3.

Error — W7, Bit 2. W7, bit 2 is set if an error is detected. The programmer can obtain more detailed error information by examining W7, bits 5 through 15 and W0, bits 0 through 7. The programmer can reset this bit as part of the interrupt service or status checking routine, or when the next block of control words is sent to the TPBI. Setting this bit to zero clears the command complete interrupt, if enabled by bit 3.

Interrupt Enable — W7, Bit 3. Bit 3 is set to enable the TPBI to generate an interrupt on normal completion (W7, bit 1) or error termination (W7, bit 2). Command completion interrupt occurs upon the following logical condition:

IDLE and [(COMPLETE and INTERRUPT ENABLE) or (ERROR and INTERRUPT ENABLE)]

Note that if the enable interrupt bit is set while the TPBI is idle and the complete or error bit is set, an interrupt is generated immediately. The interrupt is always selected simultaneously with resetting the idle bit when TPBI operation is initiated. Setting this bit to zero disables the command complete interrupt.

The attention interrupts (described with W0, bits 8 through 11 and 12 through 15) are independent of the interrupt enable bit. The attention interrupts are associated with completion of a disk drive operation that can overlap with operations involving different drives. The program must read and test the TPBI status words to determine the cause of an interrupt.

Abnormal Completion — W7, Bit 7. Bit 7 is set if an operation is terminated because an I/O reset, TILINE power failure warning pulse, or TILINE power reset is detected.

Memory Error — W7, Bit 8. The memory error (ME) bit is set if a TILINE memory error is detected during a command. If an ME is detected during any operation (normal or extended), the TPBI stops transferring data from the TILINE. The TPBI continues to transfer the required number of bytes to the formatter with the data bytes containing indeterminate information.

TILINE Time-Out — W7, Bit 10. To prevent an error from indefinitely hanging the TILINE, all TILINE peripheral controllers incorporate a timer that allots up to 10 microseconds for a TILINE operation. If the timer expires before completion of the TILINE cycle, the TPBI stops transferring data to or from the TILINE and sets the time-out (TO) bit. The TPBI continues to transfer the required number of bytes to the formatter with the data bytes containing indeterminate information.

The most common cause for a TILINE time-out is an attempt to read or write to a nonexistent memory location.

Command Time-Out — W7, Bit 13. The TPBI sets this bit for the following conditions:

- Peripheral bus error
- Peripheral bus time-out
- Peripheral bus parity error
- Protocol errors
- Formatter-detected peripheral bus error

Unit Error — W7, Bit 15. The TPBI sets bit 15 when an operation terminates because of a command issued to a disk drive that is not known to be present on the peripheral bus. W0 indicates that the unit is offline.

2.2.6 TPBI Tape Control and Status Word Formats

The following paragraphs describe the functions of only the bits intercepted by the TPBI for tape control. Figure 2-6 shows the complete set of tape status and control bits.

2.2.6.1 W0 — Rewind Status. This word contains the rewind status and rewind mask bits.

Rewind Status (0 Through 3) — W0, Bits 8 Through 11. TPBI controls these bits. A one in any of these bit positions indicates that the tape drive designated by the particular position is rewinding. A rewind status is set to one either on power-up or when the status returned from a formatter in W0, bit 6 indicates that a rewind is in progress. The rewind status bit is set to zero when the rewind operation completes.

Rewind Mask (0 Through 3) — W0, Bits 12 Through 15. These bits are under software control from the host, but are reset to zero by the TPBI on power-up or reset of the TPBI. An interrupt to the host processor is generated if the rewind mask bit is set to one, the corresponding rewind status bit is zero, and that slave set is idle.

If multiunit operations overlap, the control words for subsequent operations cannot alter the rewind mask, which can cause the loss of the rewind interrupt. Instead of using a MOV instruction to write a whole new value into W0, the programmer can use a read-modify-write operation such as an SOC or an SZC instruction to modify bits of W0 as needed.

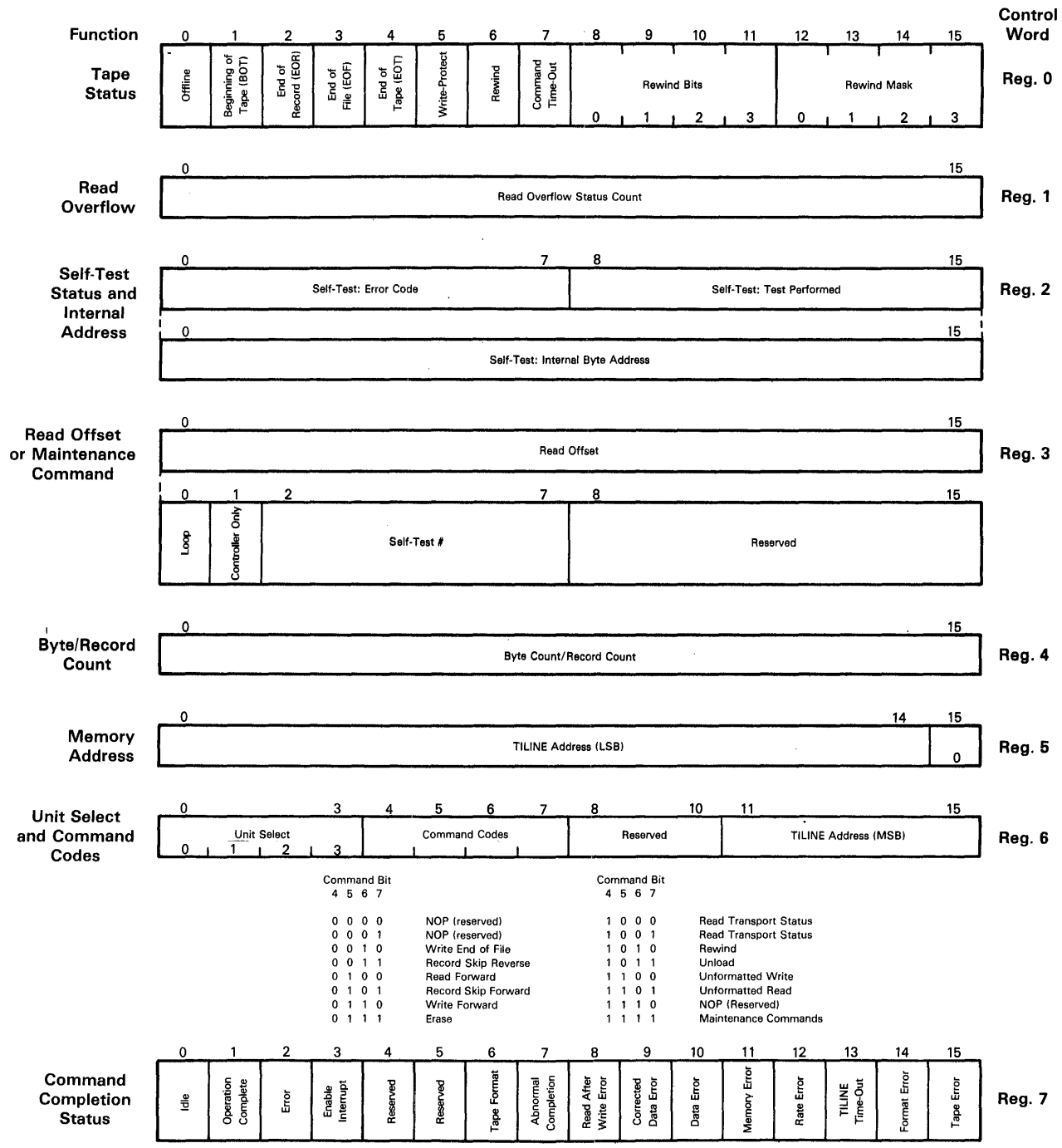


Figure 2-6. Tape Control and Status Word Formats

Since there is more than one possible cause for an interrupt to the host, do not assume that the first interrupt after initiating a rewind command is a rewind interrupt.

2.2.6.2 W2 — Self-Test Status and Internal Address. This word returns self-test error status when the right byte of W7 contains all ones (> FF). Either the formatter or the TPBI can report self-test. After power-up, the self-test of the TPBI is reported. If the TPBI fails to pass any of its self-tests, any command except self-test aborts with TPBI self-test failure status reported to the host. If a formatter fails self-test, it aborts any command except self-test commands and returns formatter self-test error status to the TPBI.

2.2.6.3 W3 — Maintenance Commands. The host uses W3 to define self-test or maintenance commands to the TPBI or a formatter.

Maintenance Command Specification Field — W3, Bits 0 Through 7. When set to one, W3, bit 0 indicates that a self-test must repeat until the device receives a reset.

When set to one, W3, bit 1 indicates to the TPBI to perform the test specified. When set to zero, the formatter performs the test.

W3, bits 2 through 7 specify a TPBI self-test or maintenance command (Table 2-2). (See Section 3 for formatter maintenance command definitions.)

Table 2-2. TPBI Maintenance Commands

Code	Name
>40	Execute all TPBI self-tests
>41 – >51	Individual TPBI self-tests
>52 – >7B	Execute all TPBI self-tests
>7C	Read peripheral parameter block
>7D	Execute peripheral memory
>7E	Write peripheral memory
>7F	Read peripheral memory

2.2.6.4 W4 — Transfer Byte Count. W4 specifies the TILINE byte count to the TPBI for the maintenance commands.

2.2.6.5 W5 — Memory Address (LSB). This word supplies the least significant 15 bits of a TILINE starting address from the host to the TPBI. The TPBI ignores the LSB of this word (bit 15). The five MSBs are located in W6. If no faults occur, the address in these words is the ending TILINE memory address following command completion. If a memory error causes termination of a command, the address in this word indicates the byte address of the memory error plus 2, because the TILINE address increments once before the memory error terminates the operation.

2.2.6.6 W6 — Unit Select and Command Codes. This word contains the unit select and command codes.

Unit Select — W6, Bits 0 Through 3. Bits 0 through 3 are a position-coded unit select field. Only one bit position in this field is set to one. The TPBI aborts any command that contains zero or multiple ones with the offline and unit error status bits set. The valid unit select codes are as follows:

W6, Bit				
0	**1**	**2**	**3**	**Unit Selected**
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3

Tape Command Codes — W6, Bits 4 Through 7. Bits 4 through 7 are under host control. Table 2-3 shows the command codes.

Table 2-3. Tape Command Codes

Command Code	Command Name
>0	NOP (reserved)
>1	NOP (reserved)
>2	Write end-of-file
>3	Record skip reverse
>4	Read forward
>5	Record skip forward
>6	Write forward
>7	Erase
>8	Read transport status
>9	Read transport status
>A	Rewind
>B	Unload
>C	Unformatted write
>D	Unformatted read
>E	NOP (reserved)
>F	Maintenance commands

Host Memory Address (MSB) — W6, Bits 11 Through 15. The five MSBs of the 20-bit TILINE memory buffer starting address occupy bits 11 through 15. Refer to the W5 description for additional information.

2.2.6.7 W7 — Command Completion Status. W7, as a control word, sets the interrupt enable bit (if desired) and sets the idle/busy bit that initiates TPBI operation. This word holds TPBI status at the end of an operation. Bits 7 through 15 report storage system status after a command executes. Valid error information is contained when the error bit (W7, bit 2) is set. Bits 8 through 15 are all on in the event of a self-test failure. If the next command after a self-test failure involves a drive operation, bits 8 through 15 do not clear and the operation is inhibited. An I/O reset or power reset clears the status logic and performs a self-test.

Idle — W7, Bit 0. Both the host and TPBI control bit 0. The host can read or write into the registers when bit 0 is idle (bit 0 = 1). If the host reads any register while the idle bit is inactive, the register contents are provided; but the MSB of the register returned is always zero, regardless of the actual state of this bit in the register.

The host sets this bit to zero to activate any tape command. W6, bits 4 through 7 specify the commands.

The TPBI sets this bit to one when command execution completes, either normally or as a result of an error condition.

The TILINE interrupt for each slave set is active only when this bit is active.

Complete — W7, Bit 1. TPBI sets the operation complete bit upon error-free completion of any command. The host can reset this bit as part of the interrupt service or status checking routine, or when the next block of control words is sent to the TPBI.

Error — W7, Bit 2. The TPBI sets W7, bit 2 if an error is detected in any operation. More detailed error information is contained in W7, bits 5 through 15 and W0, bits 0 through 7. The host may reset this bit as part of the interrupt service or status checking routine, or when the next block of control words is sent to the TPBI.

Interrupt Enable — W7, Bit 3. Interrupt enable is normally under host control, but is set inactive by the TPBI on power-up or TILINE reset. Setting bit 3 to one enables the TPBI to generate an interrupt on normal completion (W7, bit 1) or error termination (W7, bit 2). The command completion interrupt occurs upon the following logical condition:

IDLE and [(COMPLETE and INTERRUPT ENABLE) or (ERROR and INTERRUPT ENABLE)]

Abnormal Completion — W7, Bit 7. The TPBI sets bit 7 if an operation terminates because a TILINE I/O reset, TILINE power failure warning pulse, or TILINE power reset is detected.

TILINE Memory Error — W7, Bit 11. This bit is normally under TPBI control, but the host can also write it.

The TPBI sets bit 1 to one if a TILINE memory error occurs during a system memory read. When the TPBI detects a TILINE memory error, it stops transferring data from the TILINE. The TPBI continues to transfer the required number of bytes to the formatter to assure that the proper interrecord gap is written. These data bytes contain indeterminate information.

TILINE Time-Out — W7, Bit 13. This bit is normally under TPBI control, but can also be written by the host while the idle bit is active.

When the TPBI detects a TILINE time-out, it stops transferring data to or from the TILINE. The TPBI continues to transfer the required number of bytes to the formatter to assure that the proper interrecord gap is written. These data bytes contain indeterminate information.

The most common cause for a TILINE time-out is an attempt to read or write to a nonexistent memory location.

Tape Error — W7, Bit 15. The TPBI sets this bit in conjunction with the command time-out bit under certain conditions described in paragraph 3.3.6.1.

2.3 TPBI INSTALLATION

This section provides preparation, unpacking, and installation information for the TPBI.

CAUTION

Do not connect or disconnect any plug or circuit board when power is applied to the system since voltage transients may damage electronic parts.

2.3.1 Preparation for Use

The following paragraphs provide detailed instructions for preparing the TPBI for use. These instructions include unpacking, inspection, TPBI preparation, host preparation, installation in prepared slot, verification by running stand-alone tests, and the expected results of these tests.

2.3.2 Unpacking

The TPBI is shipped either packaged (Figure 2-1) or installed in a 990 chassis. Inspect packaging immediately upon receipt for evidence of abuse.

CAUTION

The TPBI contains static-sensitive electronic components. To avoid damage to these components, ensure that you discharge any accumulated static before removing or handling the printed circuit boards. This can be done by touching a grounded object before unpacking the board. Then, as a further precaution, place the board on a grounded work surface after removing it from the assembly or its protective package. Before storing or transporting the board, return it to its protective package or the assembly.

NOTE

Save the shipping cartons and packing materials for reshipment of the TPBI, if required.

CAUTION

To avoid equipment damage, use tools with care during unpacking.

2.3.3 Inspection

Inspect the TPBI for shipping damage. Contact carrier immediately upon discovery of shipping damage.

2.3.4 TPBI Board Switch Setting

The TPBI board contains two six-section, dual in-line pack (DIP) switches, ADDR A and ADDR B, that set the TILINE starting address for each of the TPCS registers. In a configuration that uses both disk and tape units connected to the TPBI, the disks are assigned to the TPCS registers whose addresses are set by switch ADDR A, and the tapes are assigned to the TPCS registers whose addresses are set by switch ADDR B. Verify switch positions according to the following paragraphs.

The CPU incorporates the TPBI into addressable memory space for access via the TILINE. Switches on the TPBI board determine the TILINE base memory addresses and must be correctly set prior to use. If the TPBI is shipped as part of a complete system, these switches are already set, but verify setting prior to operation. The following paragraphs describe this procedure.

Figure 2-2 shows the TPBI board and switch locations. Table 2-4 lists the CPU byte addresses and corresponding switch positions for each of these addresses. The standard main 990 computer chassis slot assignment for a system disk controller is slot 7 for the 13-slot chassis and slot 11 for the 17-slot chassis. The CPU byte address for the system disk controller is > F800 (all switches in the off position). The CPU byte address for the system tape controller is > F880 (all switches in the off position except switch number four).

If these switches need setting, determine the proper TILINE address according to the operating system software, and set the switches (Table 2-5).

NOTE

If the TPBI is purchased as part of a complete Texas Instruments Model 990 Computer system, computer chassis preparation (paragraphs 2.3.5 through 2.3.6) is not necessary. In this case, proceed to paragraph 2.3.7.

Table 2-4. TILINE Address Switch Configurations

Switch						
6	5	4	3	2	1	Logical Address
Off	Off	Off	Off	Off	Off	F800 (normally disks on ADDR A)
Off	Off	Off	Off	Off	On	F810
Off	Off	Off	Off	On	Off	F820
Off	Off	Off	Off	On	On	F830
Off	Off	Off	On	Off	Off	F840
Off	Off	Off	On	Off	On	F850
Off	Off	Off	On	On	Off	F860
Off	Off	Off	On	On	On	F870
Off	Off	On	Off	Off	Off	F880 (normally tapes on ADDR B)
Off	Off	On	Off	Off	On	F890
Off	Off	On	Off	On	Off	F8A0
Off	Off	On	Off	On	On	F8B0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
On	On	On	On	On	On	FBF0

2.3.5 990 Computer Chassis Preparation for the TPBI

The following paragraphs describe 990 computer preparations unique to the TPBI. This material is abstracted from the chassis preparation instructions in the computer hardware reference manuals. See the Preface for formal titles and part numbers of hardware reference manuals for the 990/5, 990/10, and 990/12 computers.

If the disk controller is shipped as part of a 990 computer system, computer chassis preparation is done at the factory. The controller is assigned a slot location, the interrupt jumpers are installed, and the TILINE access-granted (TLAG) jumpers/switches are correctly set. In this case, after the controller switch settings are verified, the hardware is compatible with the supplied software.

2.3.5.1 Selecting a Chassis Slot for the Controller. Chassis slot selection is based upon interrupt level and TILINE priority considerations. Each of the 990 packaged systems already incorporates a planned growth path that specifies preferred slot locations, interrupt levels, and TILINE base addresses for standard peripheral controllers.

NOTE

If the next lower-numbered slot contains a board that is equipped with a shield-stiffener, the plastic insulator must be removed from the shield-stiffener of the TPBI board. If the next lower-numbered slot contains a board that is not equipped with a shield-stiffener, the plastic insulator must be on the shield-stiffener of the TPBI board.

Coordinate interrupt assignments and TILINE address switch settings with the operating system software by system generation (sysgen) procedures. Refer to sysgen instructions in operating system documentation upon completion of hardware installation.

2.3.5.2 TILINE Philosophy. The TILINE is a common data path that connects to all slot positions in the 990 chassis. Users of this bus fall into two major device types: masters and slaves. Master devices address slave devices and command them to accept or transmit data. Some TILINE peripherals, including the TPBI, have both master and slave logic.

To resolve conflicts between multiple masters contending for TILINE control, a positional priority scheme is used. The TLAG signal that establishes positional priority among masters is wired along the P2 side of the computer chassis. The TILINE master installed in the highest numbered slot has the highest priority, with priority decreasing with each slot toward the central processor location (slot 1).

The TLAG signal from a higher priority master enters each master on P2, pin 6. The signal leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers are installed on the backpanel to assure line continuity across slots not occupied by masters. Additional masters can be inserted at slot positions of higher or lower priority by opening the jumper between P2, pin 5 and P2, pin 6 (TLAG) for the selected slot location. Installing a board with TILINE master logic, such as the TPBI, requires the following:

- The TLAG jumper (P2, pin 5 to P2, pin 6) must be opened for the chosen slot. Opening a TLAG jumper consists of one of the following:
  - — Physically pulling out a jumper (current 6-slot and 13-slot chassis)
  - — Cutting a jumper wire or etch (older 6-slot and 13-slot chassis)
  - — Setting a jumper switch to OFF (17-slot chassis)
- Continuity of the TLAG lines between the highest priority master and the central processor board must be preserved. This means that if an intermediate slot is assigned to a TILINE master, that master must be installed to preserve continuity and to allow the priority system to function. This also means that the jumpers must be in place (or jumper switches on) for all slots not occupied by TILINE couplers or TILINE device controllers.

2.3.5.3 Preparing a 990 Chassis Slot Location for the TPBI. Jumper locations and modification procedures differ between versions of the 990 chassis, as described in the following paragraphs.

Slot Preparation — Current Production, 6-Slot and 13-Slot Chassis. Current production units have the TLAG jumpers accessible from the connector side of the motherboard, as shown in Figure 2-7 (6-slot) and Figure 2-8 (13-slot). For these units, perform the following steps:

1. Turn off power and unplug the ac line cord.
2. Remove any circuit boards that are necessary for access by rocking the plastic ejector tabs firmly. Note the locations and orientation of the boards to reinstall them properly.
3. Remove the access-granted jumper plug for the selected location.
4. To change interrupt levels, refer to paragraph 2.3.5.4.
5. Reinstall the circuit boards in the proper locations. Check the configuration label on the chassis to ensure that the boards are installed in the correct slots.
6. Record the new slot assignment on the configuration chart affixed to the chassis.

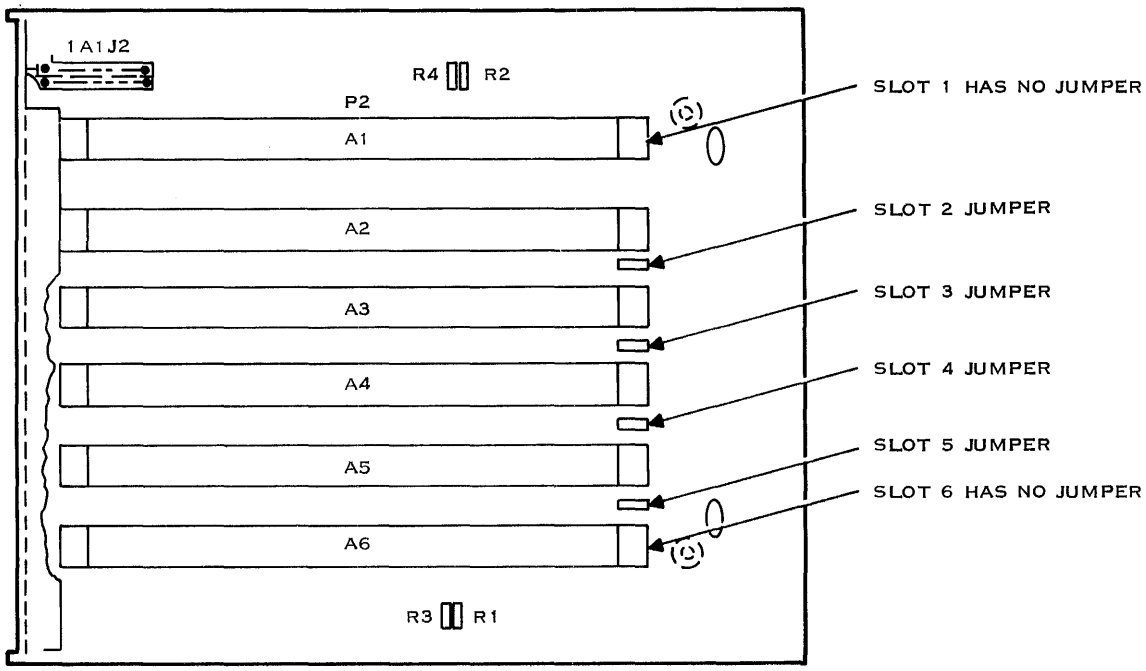


Figure 2-7. TLAG Jumper Locations for 6-Slot Chassis (Current Production)

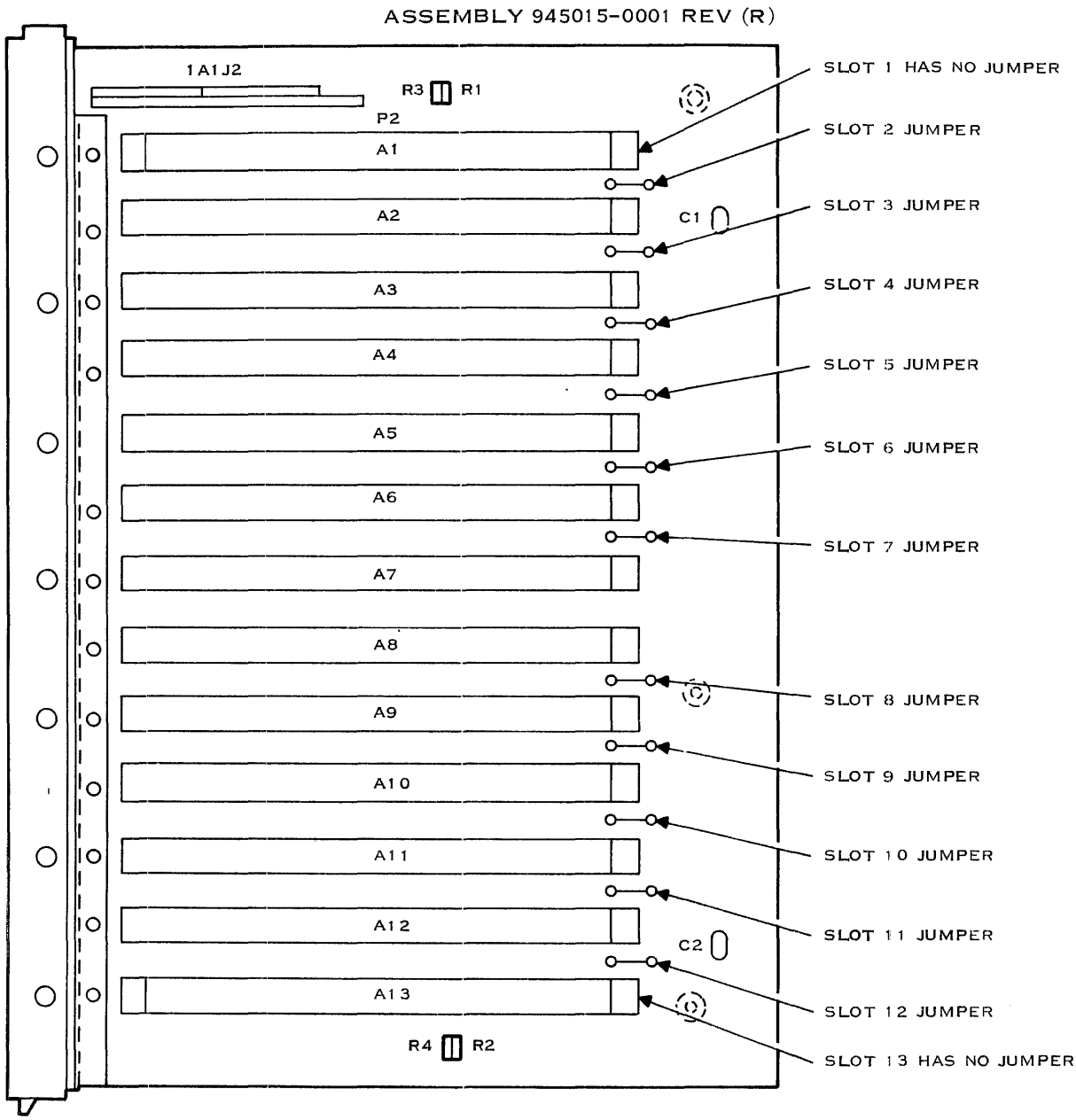


Figure 2-8. TLAG Jumper Locations for 13-Slot Chassis (Current Production)

Slot Preparation — Early Production, 6-Slot and 13-Slot Chassis. If the chassis is an early production version (that is, it does not have jumpers as shown in Figure 2-7 or Figure 2-8), remove the back cover and power supply to gain access to the TLAG jumpers. For these chassis, perform the following steps:

1. Turn off the power and unplug the ac line cord.

WARNING

Removing the access cover exposes lethal voltages. The power supply capacitor retains charges long after ac power is removed.

2. Remove the left access cover (as viewed from the front of the chassis). The cover is fastened by four or six hex-head machine screws.

3. If the chassis is a 13-slot unit with a 20-ampere power supply, slots 1 through 6 are visible above the power supply. In this case, proceed to step 5.

4. Remove the power supply as follows:

   a. Disconnect the color-coded connectors from the component side of the power supply board.

   b. Unscrew the machine screws and standoffs that secure the power supply and the radio-frequency (RF) shield to the frame and to the motherboard.

   c. Carefully pull the power supply board straight forward until the connector at the bottom center of the power supply board is disengaged from the pins protruding from the motherboard. Lift the power supply board out of the chassis.

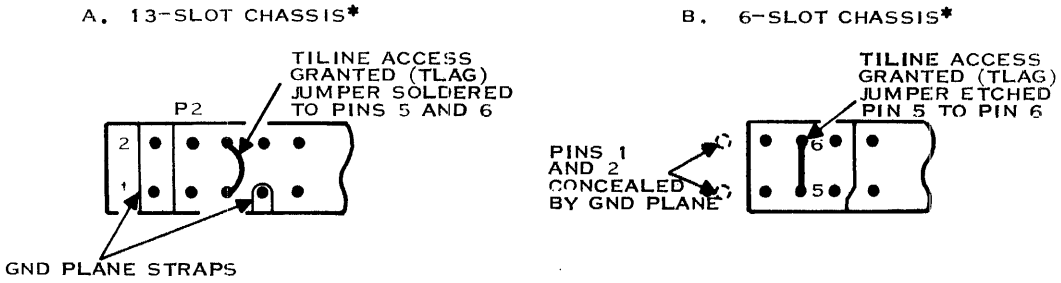
   d. Remove the RF shield.

5. The rear of the motherboard is now exposed. The P2 connectors are at the left side, closest to the fan. Figure 2-9 gives detailed views of the left end of the P2 connector in a 13-slot and 6-slot chassis.

   In a 13-slot chassis, the TLAG jumpers (P2, pin 5 to P2, pin 6) are wire loops soldered to the connector. The ground plane conceals pins 1 and 2.

   To remove a jumper in the 13-slot chassis, clip the wire loop in two places and remove the excess wire. To remove a jumper in the 6-slot chassis, cut the jumper etch at two points with a sharp knife and lift or scrape away the excess conductor.

   To install a jumper, solder a short length of #26 AWG wire between P2, pin 5 and P2, pin 6.



*NOTE THESE ARE REAR VIEWS OF THE 990 MOTHERBOARD, I.E., VIEWS FROM THE POWER SUPPLY SIDE.

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Figure 2-9. TLAG Jumpers on Early Production 6-Slot and 13-Slot Chassis

6. To reinstall the power supply, proceed as follows:

CAUTION

The male pins protuding from the lower center of the motherboard can be bent if the mating connector on the power supply is not properly aligned with these pins.

a. Slip the power supply over the cable harness and into the side of the chassis. The metal shell jumper connector (for the standby power supply) appears at the bottom center of the power supply board.

b. Align the power supply circuit boards on the two alignment pins and carefully slide the board straight back so that the pins protruding from the motherboard slip into the connector on the power supply circuit board. The power supply board blocks the view of these pins.

c. Reinstall the machine screws and standoffs that hold the power supply and RF shield in place. Do not omit the lockwashers; both mechanical and electrical connections are made by the machine screws and standoffs.

d. Reconnect the power supply to the wiring harness by installing the color-coded plastic connectors.

7. Replace the access cover and secure it with machine screws.

8. Record the new slot assignment on the configuration chart affixed to the chassis.

9. Refer to paragraph 2.3.5.4 for interrupt connections.

Slot Preparation — 17-Slot Chassis. Continuity of the TLAG jumpers in the 17-slot chassis is controlled by two socket-mounted DIP switches, each with eight individual switch sections. These switches are accessible from the rear of the 17-slot chassis (Figure 2-10). To check or set these switches, perform the following steps:

1. Turn off the power and unplug the chassis ac line cord. Allow about 30 seconds for the power supply bleeders to discharge the power supply capacitors.

WARNING

Opening the chassis rear cover (power panel) exposes lethal voltages if the ac line cord is installed in a power socket. Do not contact the large filter capacitors on the power module.

CAUTION

The wire hinges on the chassis rear cover do not allow the cover to pivot beyond 90 degrees. Attempts to open the chassis rear cover beyond 90 degrees can damage the hinge mountings.

2. Using a coin or flat-bladed screwdriver, release each of the 11 quarter-turn latches on the chassis rear cover. Pull the cover straight back 38 millimeters (1.5 inches) to extend the wire hinges, then open the cover to the 90-degree position. The hinges are on the right as viewed from the rear of the chassis.

3. Figure 2-11 shows the correspondence between switch sections and chassis slots. Set the appropriate switch segment to off for any slot that is assigned to a TILINE master device, such as the TPBI. All other switch segments are set to on.

4. Refer to paragraph 2.3.5.4 if interrupt assignments are changed.

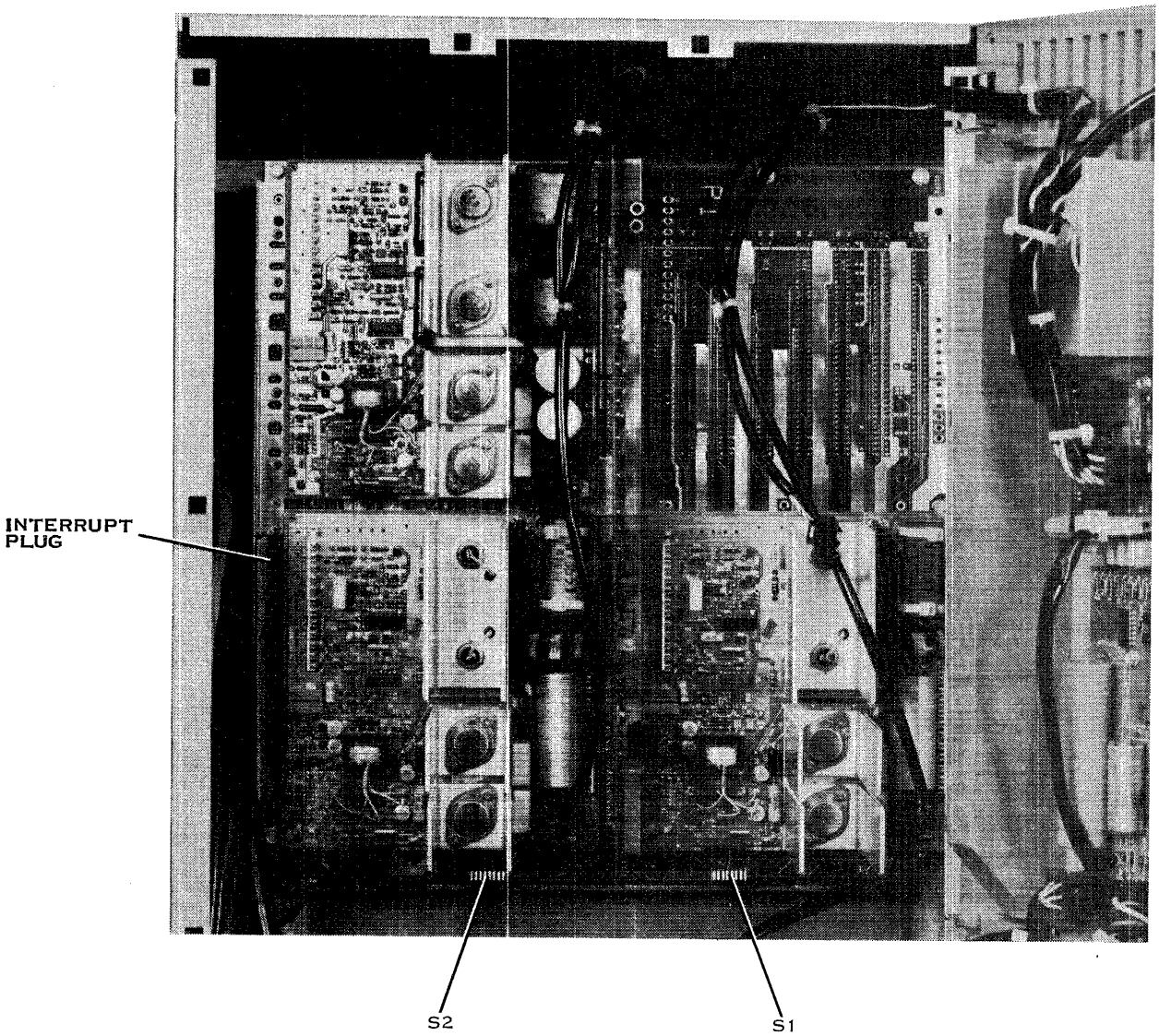

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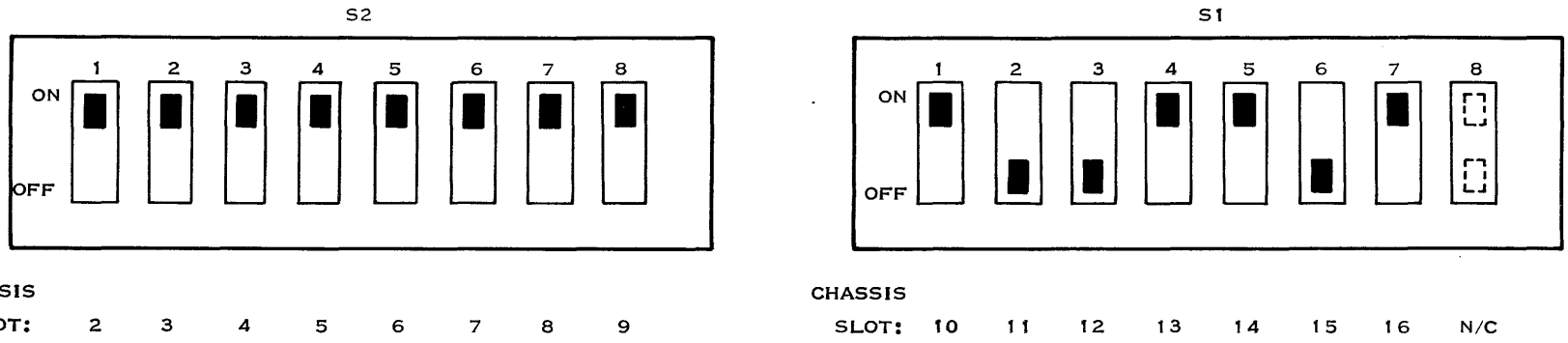
Figure 2-10. Interrupt Plug and TLAG Jumper Switches in the 17-Slot Chassis

ON = TLAG JUMPERED ACROSS SLOT (P2-6 TO P2-5)

OFF = TLAG NOT JUMPERED - CONTINUITY REQUIRES TILINE CONTROLLER



NOTES:

1. SWITCHES ARE SHOWN SET FOR:
   - SYSTEM DISK CONTROLLER - SLOT 11
   - 979A TILINE MAGNETIC TAPE CONTROLLER - SLOT 12
   - FD1000 TILINE FLEXIBLE DISK CONTROLLER - SLOT 15
2. EACH SWITCH SECTION MUST BE ON UNLESS A TILINE MASTER CONTROLLER IS INSTALLED IN THE CORRESPONDING CHASSIS SLOT. TILINE PRIORITY SYSTEM WILL NOT WORK IF SWITCHES ARE SET INCORRECTLY.
3. SLOT 17 DOES NOT REQUIRE A SWITCH.

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Figure 2-11. 17-Slot Chassis TLAG Jumper Switch Settings

CAUTION

As the door is closed, there is a possibility of interference between heat sinks in the chassis and modules mounted inside the rear access cover. Do not force the door closed you feel resistance.

5. Rotate the door to a position parallel to the rear of the chassis and to fully extend the hinges. Grasp the rear access cover at the left and right sides and push it straight back to the mounting position against the chassis.

6. Using a coin or screwdriver, lock the 11 quarter-turn latches that hold the access cover in position.

2.3.5.4 Interrupt Connections. Interrupt connections to interface peripheral equipment to the 990 processor are usually made before the system is delivered to the customer. The planned growth path for the 990 systems avoids the necessity for the customer to modify interrupt levels. Preassigned slot assignments do not require modification of the factory prewired interrupt levels. Note, however, that adding a controller to a previously existing installation requires a sysgen operation to coordinate hardware and software operation.

The information in the following paragraphs is for users who must modify existing interrupt assignments.

NOTE

Refer to the *Model 990A13 Chassis General Description Manual* or the *Business Systems 600/800 Field Engineering Reference Handbook* for interrupt information regarding the 990A13 chassis.

The 990 processor has 16 interrupt levels, numbered 0 through 15. Interrupt level 0, which is internal to the processor, has the highest priority. Interrupt levels 3, 4, and 6 through 15 are external inputs that are available for assignment to peripheral controllers installed in the chassis. The interrupt input lines are wired from chassis slot 1 to an interrupt header adjacent to slot 1.

Each of the remaining chassis slots (numbered 2 and above) has two interrupt output lines wired to the same interrupt header. Interrupt level to device assignments are made by jumper connections at the interrupt header.

NOTE

TILINE interrupt 13 is the standard interrupt for a disk designated as the system disk. Use TILINE interrupt 9 for a tape unit if it is used to boot the system via the loader ROM.

The following procedure describes how to select interrupt wiring when installing the TPBI. Refer to the following paragraphs for information on interrupt connections in the specific chassis used for the installation.

1. Check the chassis configuration label on the the chassis to ensure that the desired chassis slot is wired with two separate interrupt levels that are not shared with other devices and that meet the requirements of the previous notes. If the slot wiring is acceptable, go to step 9.

2. If using a disk drive as the system disk, wire interrupt level 13 for P2 of the slot. Then go to step 5.

3. If an unused TILINE interrupt is available, wire it to P2 of the TPBI slot. Then go to step 5.

4. Select a TILINE interrupt that is not being used by any other TILINE controller and wire it to P2 of the TPBI slot.

5. If using a tape unit to boot the system, wire interrupt 9 for P1 of the TPBI slot. Then go to step 8.

6. If a spare TILINE interrupt is available, wire it to P1 of the TPBI slot. Then go to step 8.

7. Select a TILINE interrupt that is not being used by any other TILINE controller and wire it to P1 of the TPBI slot.

8. If an interrupt is taken from any CRU device, disconnect it from the CRU device slot and provide another interrupt. Some CRU devices can share an interrupt, but the TPBI requires two unshared interrupts. Refer to the system documentation to determine what new system interrupt configuration to use.

9. Mark the chassis configuration label with any changes made to the interrupt configuration and with the TILINE addresses of the TPBI. Save any remaining interrupt jumper wires for possible future use.

Interrupt Connections for 6-Slot and 13-Slot Chassis. Figure 2-12 shows the location of the interrupt jumper header and interrupt jumper plugs in a 6-slot or 13-slot chassis. Early versions of the chassis use direct pin-to-pin jumpers without jumper plugs.

The header contains two rows of pins. The top row has 15 pins connected through the motherboard to the 15 interrupt levels of the processor. Additional pins on the top row are provided in the 13-slot chassis for special configurations, such as CRU expansion. The bottom row contains 48 pins in a 13-slot chassis or 20 pins in a 6-slot chassis. Two of these pins are wired to each of the possible circuit board interrupt outputs. This allows multiple interrupts to be connected to one interrupt level.

Figures 2-13 and 2-14 show interrupt pin assignments and views of the jumper plugs as seen from the jumper wire side. The X marks identify jumper plug positions that have no corresponding pins on the header. The O marks identify jumper plug positions that have no corresponding pins on the early production header.

The detailed procedure for assigning and changing interrupt levels is presented in the hardware reference manual for the 990 computer. The information presented here is a brief summary of that procedure.

CAUTION

Do not remove or install any circuit board or modify any jumper while power is applied to the 990 chassis.

To gain access to the interrupt jumpers, remove the circuit boards installed in slots 1 through 5. The interrupt jumpers are visible on the motherboard just above the slot 1 connectors. The interrupt output of a full-sized board is on P2 of the assigned slot location. Therefore, if slot 8 is chosen for the disk controller, the interrupt is found at 8P2 of the wire-wrap pin header. A single jumper runs from the 8P2 pin to the selected interrupt level input to the processor.

After completing any interrupt jumper modifications, carefully reinstall the removed circuit boards (component side up) according to the configuration chart attached to the top of the computer. Update the configuration chart to correspond to the interrupt jumper modifications.

Interrupt Connections for 17-Slot Chassis. Interrupt lines in the 17-slot chassis are wired to a 70-pin connector accessible from the rear of the chassis. A jumper assembly is plugged into the connector to make the interrupt level to chassis slot connections. This assembly appears at the lower left of the chassis backplane (Figure 2-10).

The jumper assembly supplied with a standard 990 system is a printed wire board (PWB), so altering the standard interrupt level assignments is not usually necessary. If it becomes necessary to change interrupt levels, either purchase a special variable jumper assembly or modify the fixed jumper card. Figure 2-15 shows the pin assignments on the interrupt connector.

To gain access to the interrupt jumper assembly, open the chassis rear cover. Remove the interrupt jumper assembly by gently rocking it up and down to loosen the connector and then pulling it straight back. When reinstalling the assembly, make sure the pins are properly aligned before applying mating force.

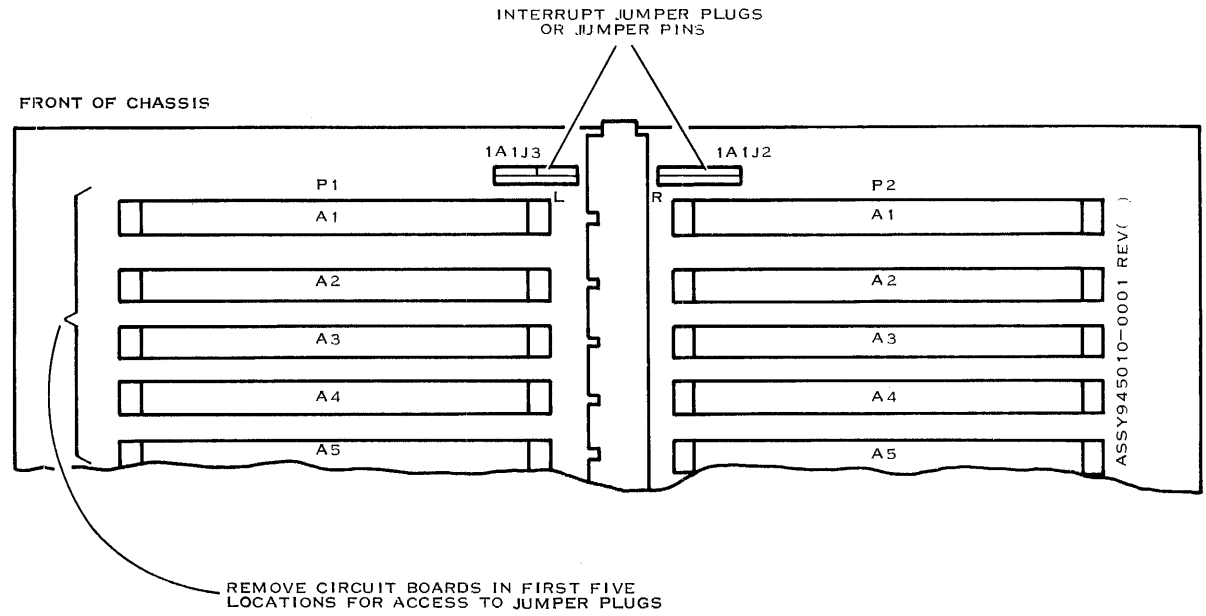

Figure 2-12. Location of Interrupt Jumpers, 6-Slot and 13-Slot Chassis

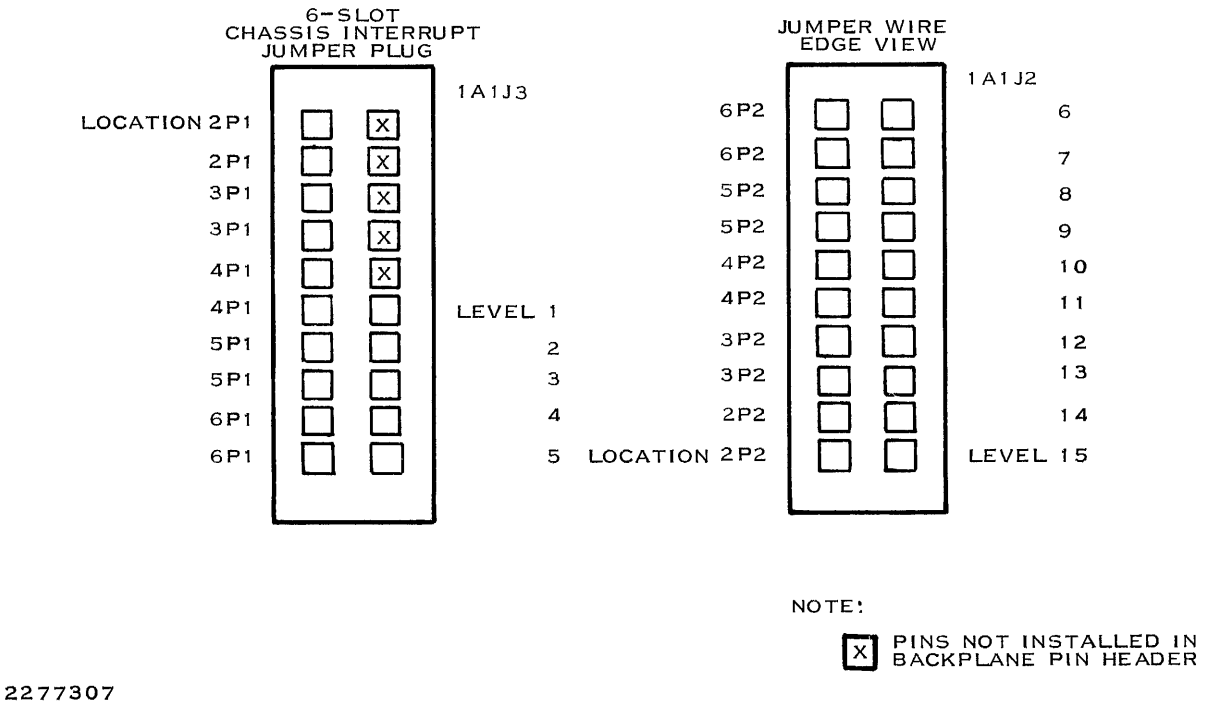

Figure 2-13. 6-Slot Chassis Interrupt Jumper Plugs

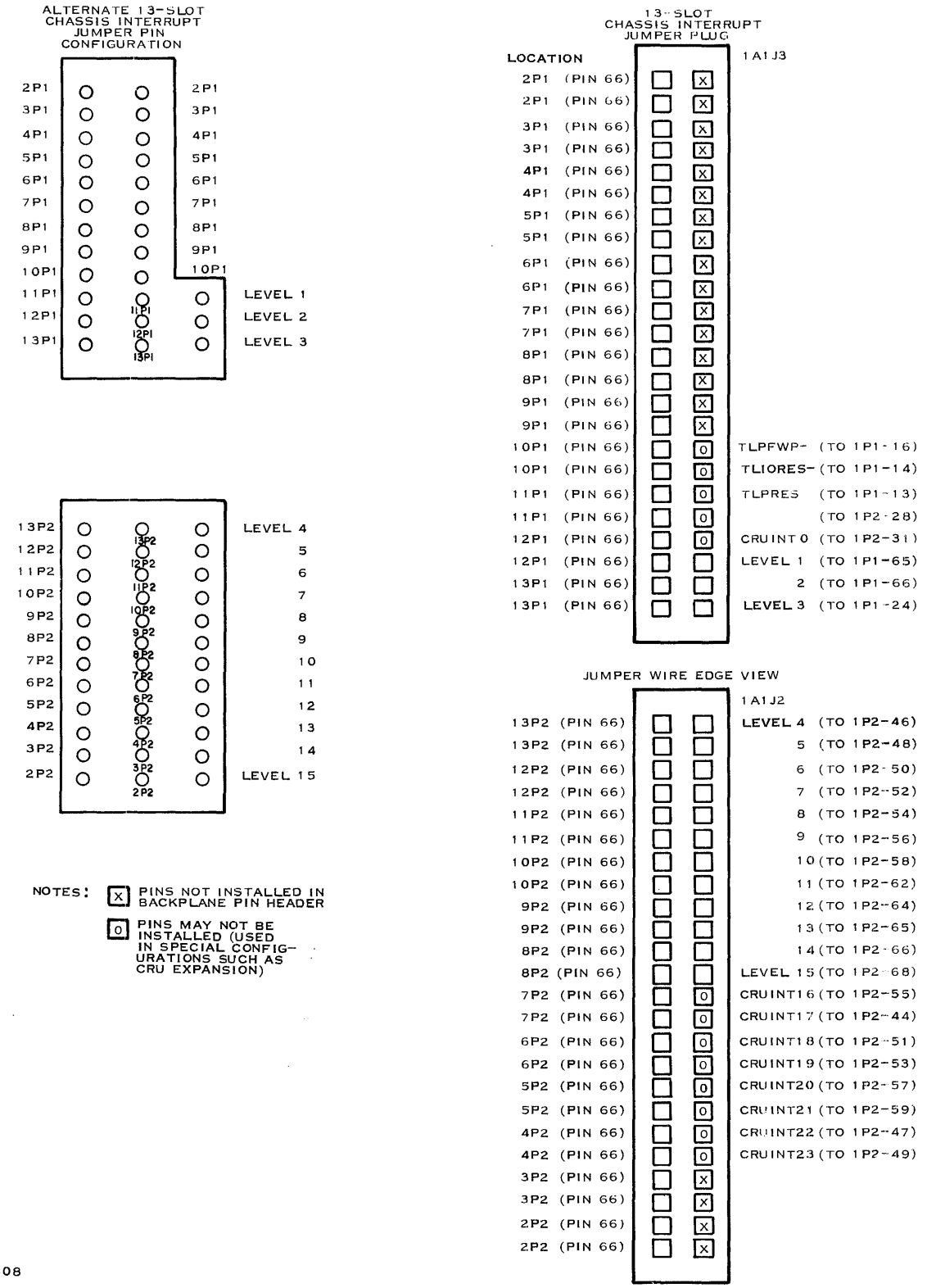

Figure 2-14. 13-Slot Chassis Interrupt Jumper Plugs

CAUTION

It is possible to install the interrupt jumper assembly upside down. Note that pin 1 is at the bottom of the interrupt connector.

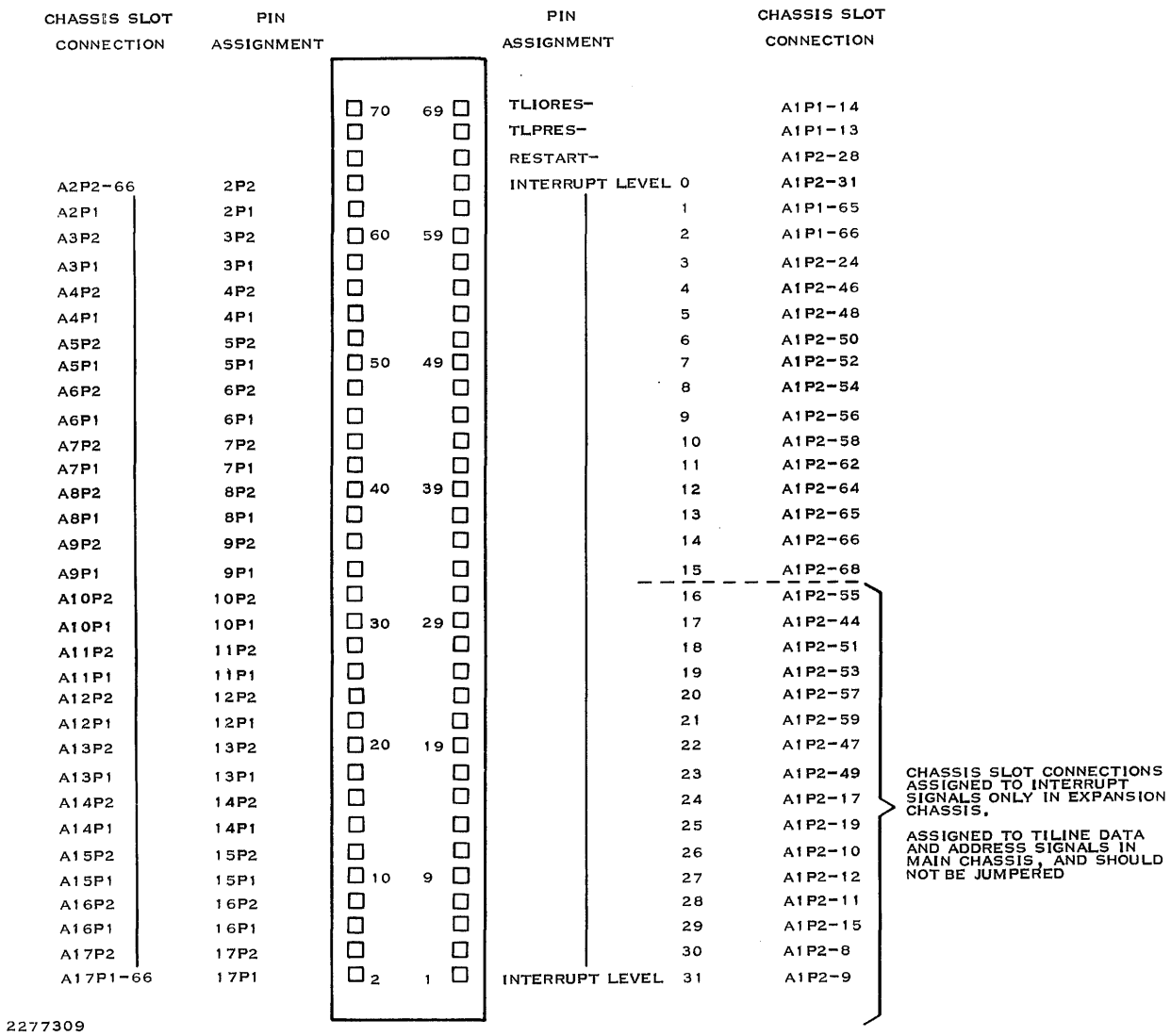

Figure 2-15. 17-Slot Interrupt Jumper Connector

2.3.6 Installation of TPBI Board in 6-Slot or 13-Slot Chassis

CAUTION

Always turn off power to the chassis before attempting logic board installation or removal. Failure to observe this precaution can result in damage to the board since connector pins are temporarily misaligned during board removal and installation.

1. With system power off, insert the TPBI board (component side up) into the assigned slot in the 990 chassis. Make sure the circuit board edge connectors mate firmly with the backpanel connectors.

2. Connect the PBI cable to connector P3 on the TPBI board.

2.3.7 Installation of TPBI Board in 17-Slot Chassis

Using the following procedures, install the TPBI board in the chassis slot prepared according to the instructions in paragraph 2.3.5.3.

1. Turn off the power and unplug the host system chassis ac line cord. Allow about 30 seconds for the power supply bleeders to discharge the power supply capacitors.

CAUTION

Always turn off the power to the chassis before attempting logic board installation or removal. Failure to observe this precaution can result in damage to the board since connector pins are temporarily misaligned during board removal and installation.

2. Push upward on the two release latches at either side of the filter panel assembly. Remove the filter panel assembly from the front of the 17-slot chassis.

3. Remove the filter panel to expose the molded access cover. Using a coin or screwdriver, turn each of six quarter-turn latches on the access cover. Then remove the access cover to expose the installed logic boards.

4. The PWB retainer is a comb-like metal structure that holds the logic boards in place. Slide the PWB retainer to its leftmost position to gain access to the chassis slots.

5. Empty slots are occupied by partitions that stabilize cooling air flow. Remove the partition from the selected slot and install the TPBI board with the component side to the right. Make sure the circuit board edge connectors mate firmly with the backplane connectors.

6. Slide the PWB retainer to the right so that all the circuit boards are locked in place.

7. Connect the PBI cable to connector P3 on the TPBI board.

8. Remove the board by reversing steps 1 through 6. Note that the access cover cannot be placed in its position until the PWB retainer has been returned to its rightmost position.

2.3.8 TPBI Verification

Before connecting the storage system chassis to the TPBI, apply power to the host system. The TPBI runs its self-test routine on power-up, and reports any errors through the fault indicators on the TPBI board and the error log messages. Appendix A explains fault analysis and suggested action. Four indicator light-emitting diodes (LEDs) on the TPBI board (Figure A-1) help to locate failures in the system.

2.3.8.1 FAULT Indicator. The red FAULT LED lights when power-up self-test is initiated. This indicator extinguishes only after self-test completes with no errors.

2.3.8.2 TILINE Indicator. The green TILINE LED lights to indicate normal operation of the TILINE access controller on the TPBI board.

2.3.8.3 Busy LEDs A and B. The green BUSY LEDs light to indicate activity by their respective slave sets. Busy indicators light when the idle status bit is set to zero due to command execution by either the TPBI or a formatter controlled by the designated slave set.

3

WD800 Chassis Installation and Programming

3.1 GENERAL

This section contains installation and programming information for the WD800 chassis. (The components of the WD800 chassis are described in Section 1.) The programming section covers that part of the system programming that applies only to the formatter in the WD800 chassis. (For kit-level installation, see Section 4; for controller installation and programming, see Section 2.)

In this section, installation and programming instructions for the **WD800A** are indicated in boldface type.

3.2 INSTALLATION

Installation procedures for the chassis as a stand-alone unit consist of site preparation, unpacking, chassis preparation, chassis mounting and ac power cabling, and initial verification (to test the WD800 chassis as a stand-alone unit before cabling the system together).

3.2.1 Site Preparation

The WD800 disk drive chassis can mount on drawer slides in an EIA standard 483-millimeter (19-inch) rack. The installation site must allow enough space for the chassis to be fully extended forward on the slides. Adequate space must also be reserved in the rack for the chassis. The chassis requires 222-millimeter (8.75-inch) panel height and 610 millimeters (24 inches) of depth behind the panel. The installation site must allow free flow of clean air to the chassis.

The WD800 disk drive must receive power from a branch circuit that provides a safety ground wire separate from the neutral wire. The disk drive may share the computer branch circuit, as long as the current rating for the circuit is not exceeded.

CAUTION

Do not put devices other than computer equipment on the branch circuit that powers the computer system (see Figure 3-1).

Table 3-1 summarizes the electrical, physical, and environmental requirements for the installation site.

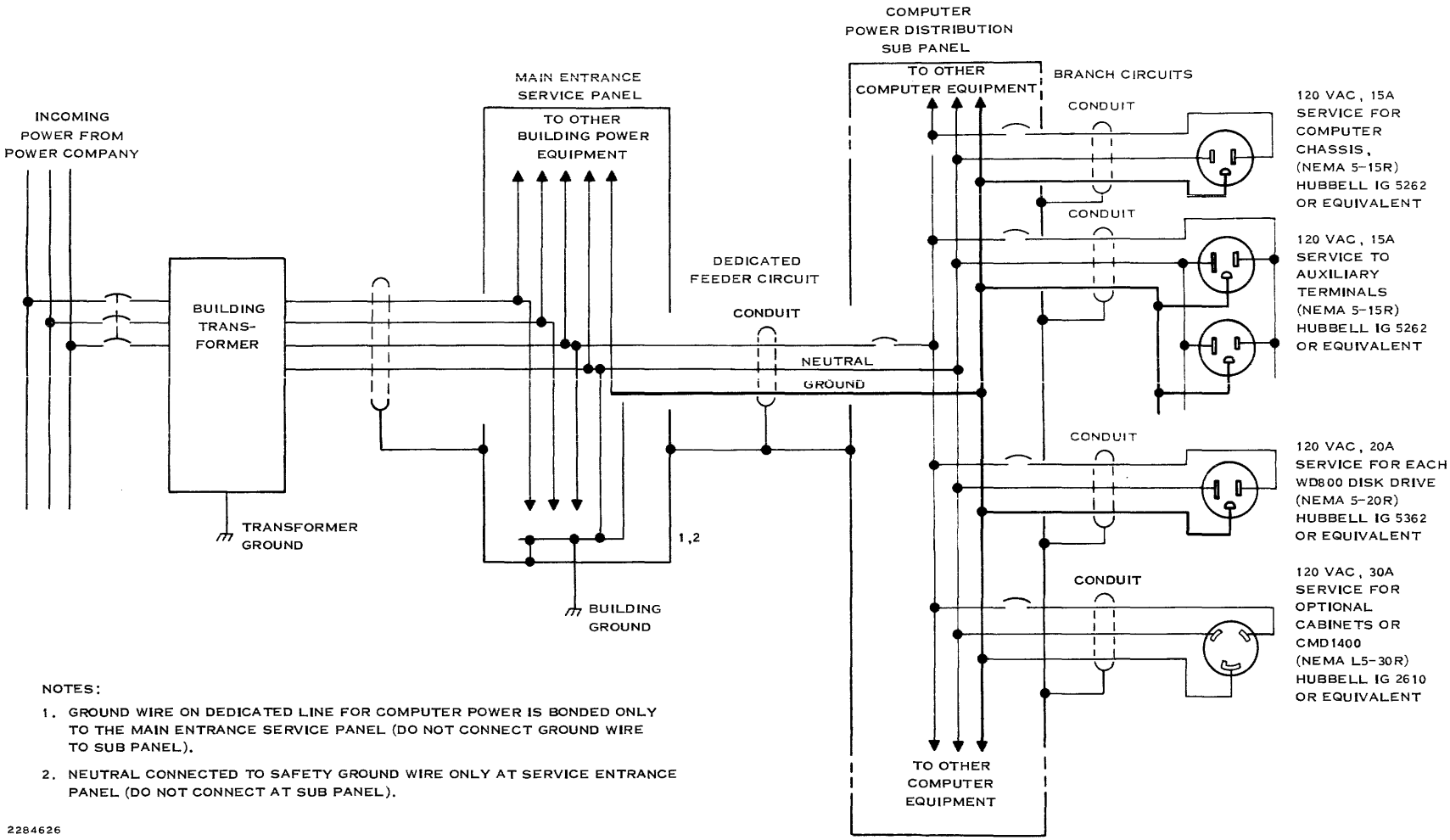

Figure 3-1. Minimum Requirement for Power Service for WD800 Equipment

Table 3-1. WD800 Subsystem Installation Requirements

Power Specifications

Chassis ac power:	WD800	**WD800A** (typical)
120 Vac ± 10% 50 or 60 Hz ± 3 Hz	3.0 A running 8.0 A starting (for 10 sec)	1.6 A running 2.5 A starting (for 10 sec)
or		
220 or 240 Vac ± 10% 50 Hz ± 3 Hz	1.5 A running 4 A starting (for 10 sec)	1.2 A running 1.6 A starting (for 10 sec)
TPBI dc power (from host chassis power supply)	5.0 ± 0.25 Vdc at 3.0 A (maximum)	

Environmental Specifications[1]

Operational[2]:	
Ambient temperature	10 to 40 ° C (50 to 104 ° F) with a temperature gradient less than 10 ° C (18 ° F) per hour
Relative humidity:	
WD800	20% to 80% without condensation
WD800A	10% to 80% without condensation
Altitude	0 to 3000 m (0 to 9843 ft)
Nonoperational:	
Ambient temperature	– 40 to 60 ° C (– 40 to 140 ° F) with a temperature gradient less than 20 ° C (36 ° F) per hour
Relative humidity:	
WD800	10% to 80% without condensation
WD800A	10% to 95% without condensation
Altitude:	
WD800	0 to 12 000 m (0 to 39 372 ft)
WD800A	0 to 3000 m (0 to 9843 ft)

Physical Specifications

Length	68.6 cm (27 in)
Width	48.3 cm (19 in)
Height	22.2 cm (8.75 in)
Weight (maximum)	
WD800	38.5 kg (85 lb)
WD800A	31.3 kg (69 lb)

Notes:

[1] Environmental specifications represent worst-case conditions as determined by the most sensitive component in the storage system.

[2] Lower these temperatures by 2 ° C (3.6 ° F) for every 762 m (2500 ft) increase in altitude above mean sea level.

3.2.2 Unpacking

The following paragraphs describe the shipping configurations of the WD800 chassis and explain the unpacking procedure.

3.2.2.1 Shipping Configuration. The WD800 chassis is shipped in one of two ways: as an individual unit (for instance, as a replacement chassis), or as part of a complete computer system. Figure 3-2 illustrates the individual unit container. When the unit is shipped as part of a complete system, the container can differ. The interconnecting cables and mounting hardware are packed either with the unit or with the computer. The shipping configurations differ in certain other respects; for example, the top of the container is indicated either by a label or by arrows on the sides that point to the top.

3.2.2.2 Unpacking Procedure. Inspect the container for evidence of abuse during shipment. If the container looks damaged, do not start the unpacking procedure; contact the carrier and report the damage. If the container passes preliminary inspection, make a visual inspection and a parts inventory when the outer carton is opened. If the unit appears damaged or if parts are missing, contact the TI sales and service office for your area. Otherwise, unpack the WD800 storage system as follows:

WARNING

Have all personnel stand clear while steel straps are being cut to avoid injury from the flying loose ends of the straps.

1. Turn the container so that the top side is up. Carefully cut the steel straps with a strap cutter and remove them.
2. Open the top of the cardboard container and remove the box containing the rackmounting slides, if present.
3. Remove the plastic bag(s) containing cables, manuals, blank tape cartridge, and mounting hardware, if present.
4. Lift the cardboard sleeve and padding up and away from the WD800.
5. Have two people lift the WD800 from the plywood skid and place it in a convenient location.
6. Save the shipping materials in case reshipment is necessary.

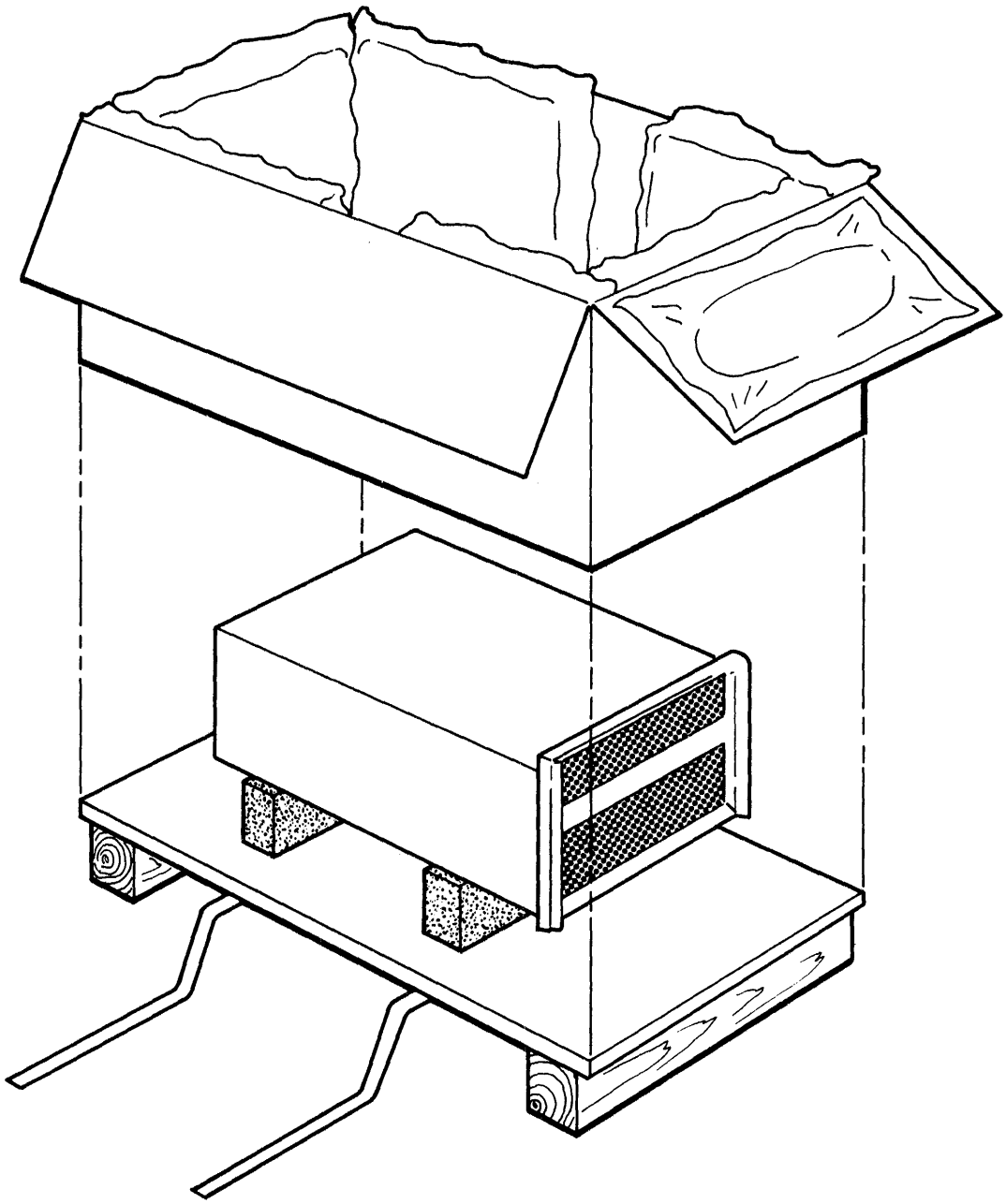

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Figure 3-2. WD800 Chassis — Individual Container

3.2.3 Chassis Preparation

Using standard handtools, prepare the chassis for installation as follows:

1. Turn the ac power switch off.

NOTE

For preparing WD800A disk units, skip steps 2 through 7.

2. To gain access to the bottom panel, turn the chassis so that it is resting on one side.

CAUTION

The chassis is unstable in this position. Be sure to stabilize it by holding it steady or by placing it against a wall or other stable surface while performing the following procedure.

3. Locate the two disk drive shipping bolts recessed into metal plates on the bottom of the chassis below the location of the disk drive unit (see Figure 3-3). The shipping bolts are 5/32 inch Allen-head bolts that screw into two shock mounts on the bottom of the drive assembly.

4. Remove the shipping bolts by loosening them alternately two threads at a time. Store them in the threaded holes next to the holes they were originally shipped in (to reinsert in case reshipment of the equipment is necessary).

5. Slide the flat blade of a screwdriver under the edge of the round, plug-in actuator lock access cover (located on the bottom of the chassis), and pry the cover off.

6. Unlock the actuator mechanism (Figure 3-4) using the following procedure:

   a. Using a 9/64-inch Allen wrench, loosen the 10-32, 9/64 socket-head cap screw a maximum of one and one-half turns.

CAUTION

Do not loosen the screw more than one and one-half turns. If turned too far, it can fall out and become lost.

   b. Insert the flat blade of a screwdriver into the slot in the center of the actuator lock positioner and turn it clockwise to unlock the actuator lock.

   c. Tighten the socket-head cap screw in the new position.

7. Replace the actuator lock access cover, and set the chassis down in its normal position.

The chassis is now ready to be mounted in the rack.

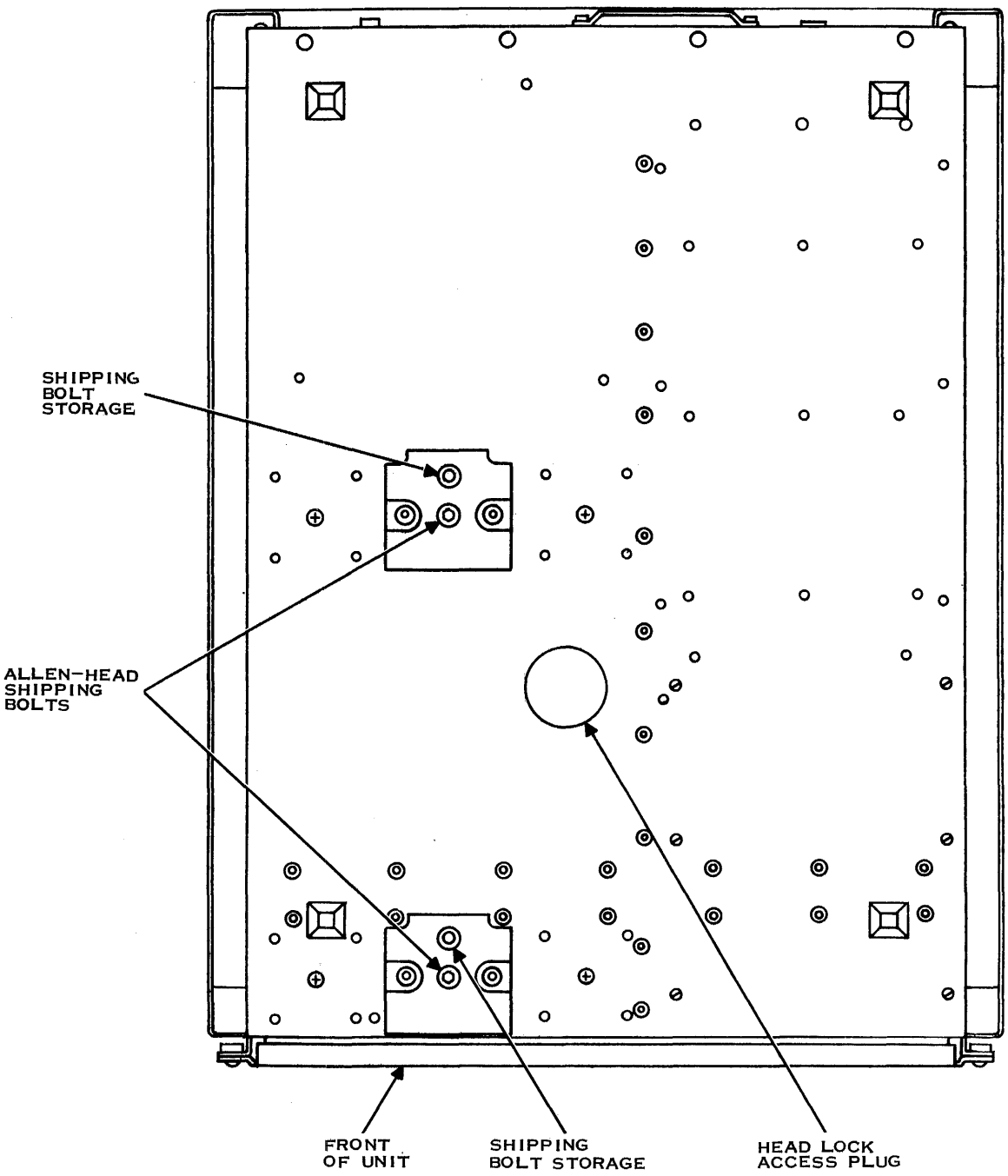

Figure 3-3. Shipping Bolt Locations (WD800 Only)

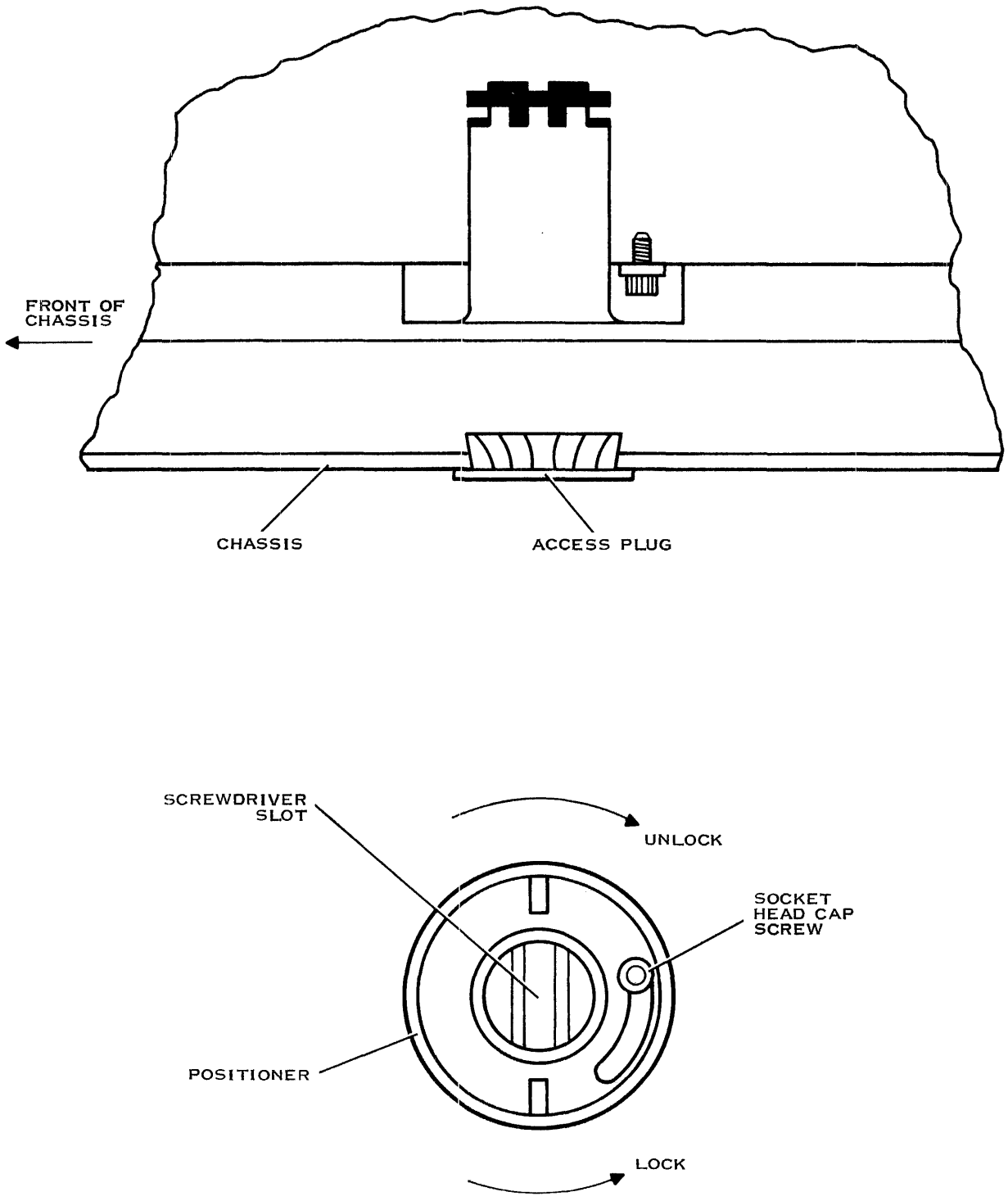

Figure 3-4. View of Actuator Lock Mechanism in Unlocked Position (WD800 Only)

3.2.4 Chassis Installation in an EIA Cabinet

The following procedure describes how to mount a WD800 chassis with a standard 990 slide kit (TI Part No. 2270865-0001). Installation of a fixed mount kit (TI Part No. 2309400-0001) is very similar; for a table top installation, skip to paragraph 3.2.5. The slide kit includes left and right telescoping slides, two adjustable-length rear mounting brackets, and four clamp or nut plates. Nut plates are threaded for use with unthreaded EIA rails; clamp plates are unthreaded for use with threaded EIA rails. The kit also includes small mounting hardware items (screws and washers).

Slide mounting consists of four operations:

1. Selecting the mounting location in the cabinet
2. Mounting the slide set in the cabinet
3. Mounting the inner slides to the chassis (Figure 3-5 and Figure 3-6)
4. Installing the inner slides (and chassis) in the cabinet (Figure 3-7).

NOTE

The intake air filter and front trim panels are not installed until after cabinet mounting is complete. The trim panels should not be used for lifting the chassis; they also interfere with extending the slides.

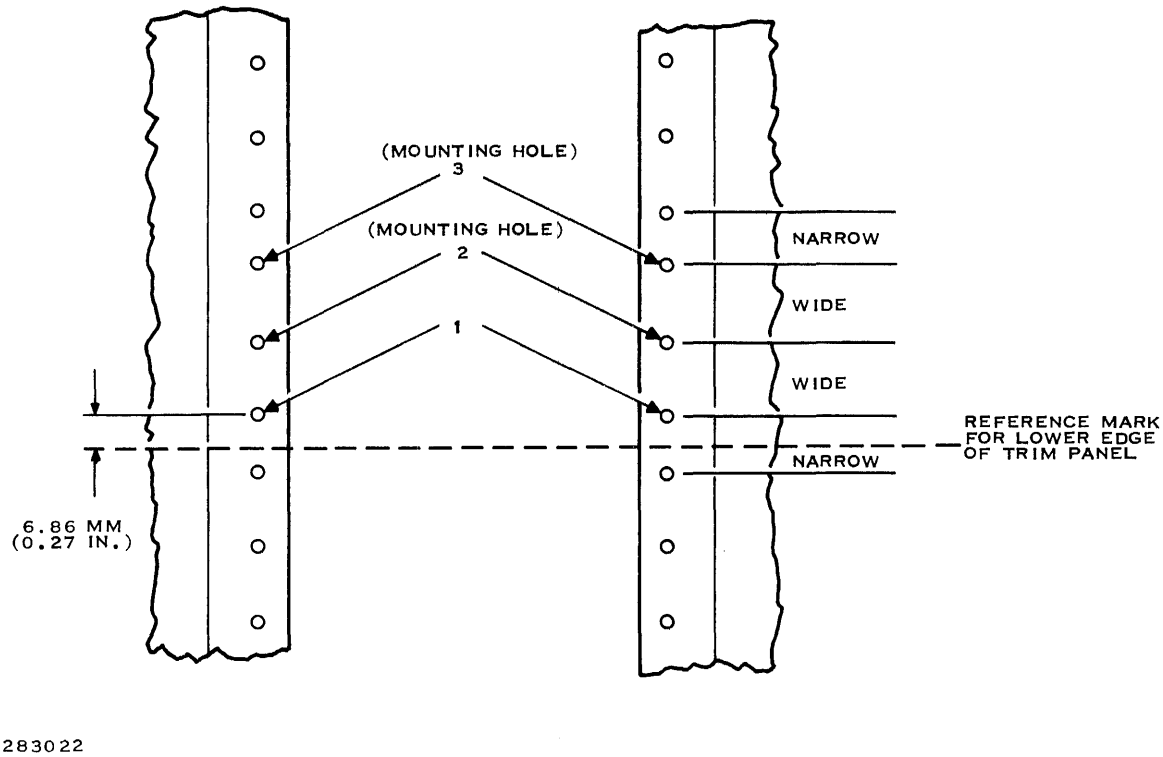

Figure 3-5. EIA Mounting Rails

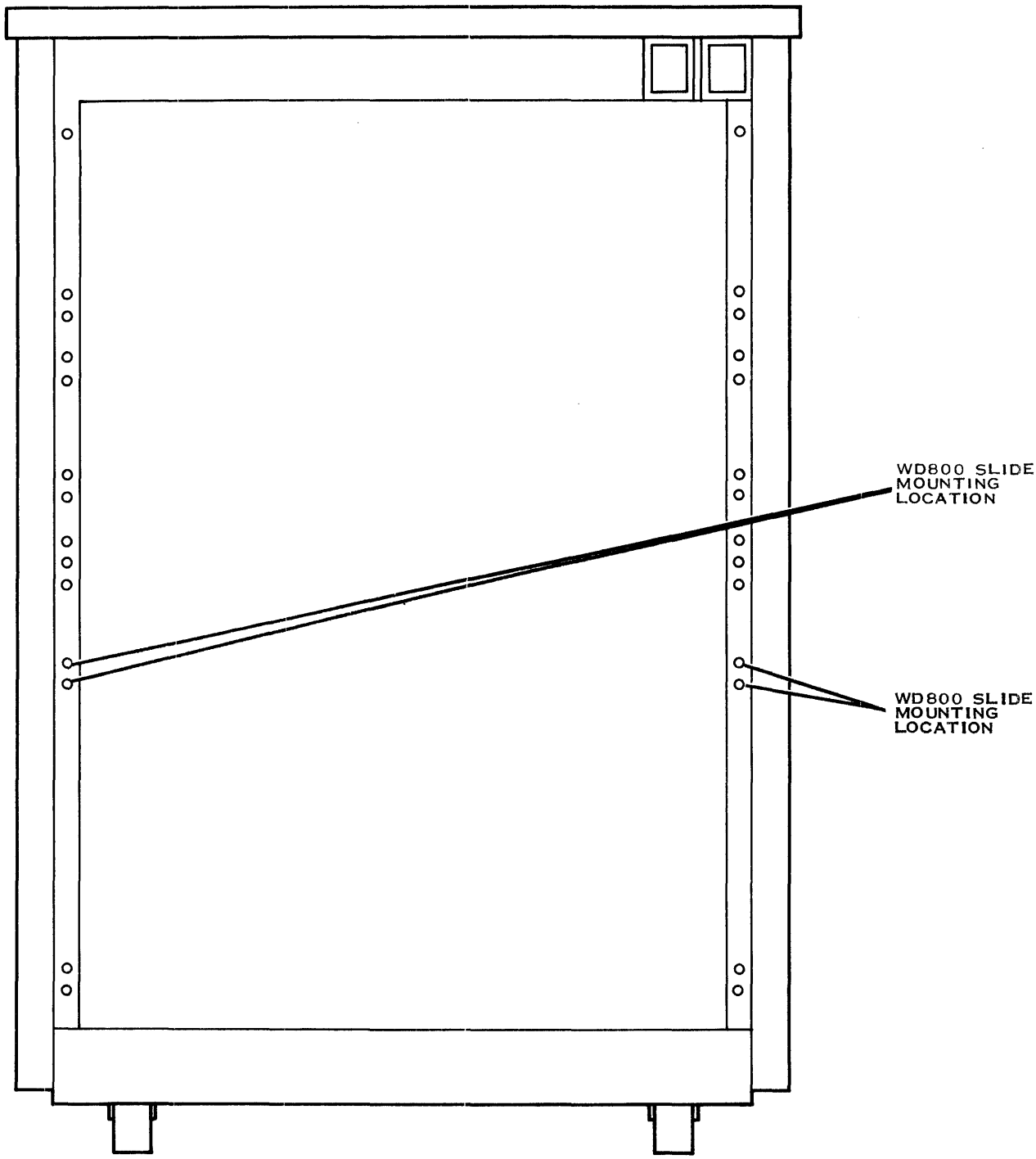

Figure 3-6. Standard 0.82-Meter (32-Inch) Cabinet

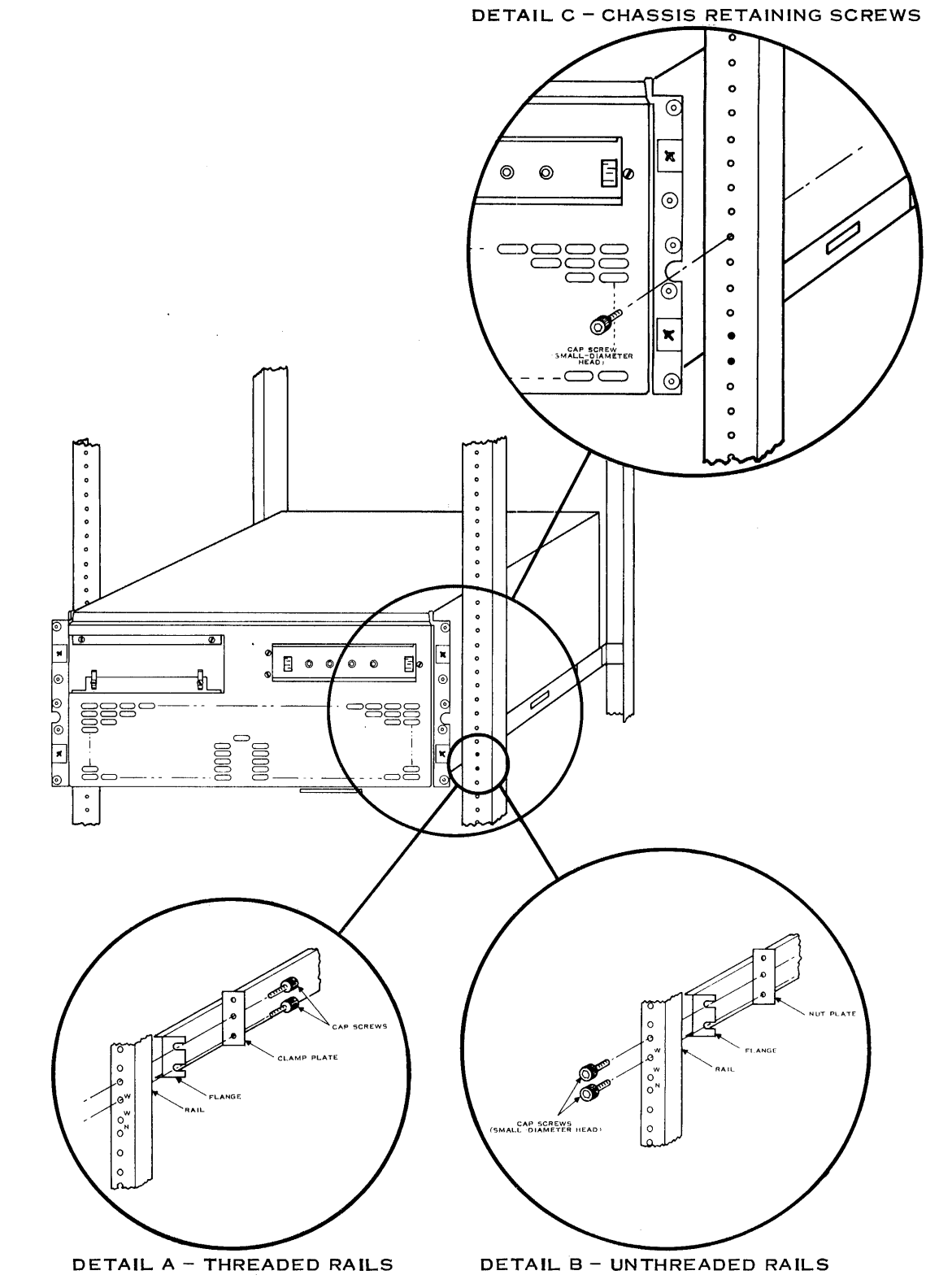

Figure 3-7. Perspective View of Slide Mounts

To mount a WD800 chassis in an EIA standard cabinet, use the following procedure:

1. The allowable spacing between the front and rear cabinet rails is 616 ± 6.35 millimeters (24.25 ± 0.25 inches). The slide set is adjustable over this range, so spacing is not critical. Move the cabinet rear rails if the spacing is outside the allowable range.

2. Determine where you want to locate the bottom edge of the lower trim panel, as shown in Figure 3-5. Refer to Figure 3-6 for 0.82-meter (32-inch) cabinet mounting. For this cabinet, the slide mounting holes are already determined.

   Make a reference mark between the set of holes with narrow spacing. By EIA standards, this mark is not centered, but is 6.86 millimeters (0.27 inches) below the center line of the upper hole. After installation, the chassis and trim panels will occupy the next 222 millimeters (8.75 inches) above the reference mark.

   Use a level or straight edge to locate the corresponding points on the rear rails.

3. Locate the slide mounting holes in the cabinet rails. Count the first hole above your reference mark as hole 1, with holes 2 and 3 as the mounting holes.

4. Each slide rear extension has a number of adjustment slots. In this step, select a set of slots for a rough adjustment. The final length adjustment and tightening come later in the procedure.

   Loosely assemble the rear extensions to the slides, so the front and rear mounting flanges fit between the cabinet front and rear rails.

5. Mount the slides in the cabinet, following the appropriate mounting details in Figure 3-7.

   If your cabinet has threaded rails, follow Detail A and mount the slides inside the front and rear mounting rails with two cap screws and a clamp plate at each mounting bracket. The cap screws enter the rails from inside the chassis, and should be hex-head or hollow-head style for positive driving.

   If your cabinet has unthreaded rails, follow Detail B and mount the slides inside the front and rear mounting rails with two cap screws and a nut plate at each mounting bracket. The cap screws enter from the rail front, and the heads will interfere with panel mounting if they are larger than 7.87 millimeters (0.31 inch) in diameter.

WARNING

Make sure that each flange is firmly clamped between the inside of a mounting rail and a clamp plate or nut plate. If you assemble the parts in the wrong order or omit a plate, the slides may fail under pressure.

NOTE

If you do not install the slides as shown in the detailed view, the chassis front trim panels may not fit properly.

6. Tighten the rear extensions to the slides.

7. Extend the slides by slightly raising the front of each slide while pulling forward. Release the inner slides by pressing the quick-disconnect buttons on the outside of the slides.

8. Each inner slide has three screw holes that align with mounting holes on the sides of the chassis. Assemble the inner slides to the chassis with three 10-32 0.500 machine screws (complete with flat washer and lock washer) per slide (Figure 3-8).

9. Insert the chassis into the extended slides, press the quick-disconnect buttons, and push the chassis into the cabinet. Work the slides several times to be sure that they operate smoothly, without binding.

10. Recheck all mounting hardware to ensure that all screws are tight.

11. After completing the air filter and front trim panel installation, check that the lower edge of the front trim panel coincides with the reference mark on the rails. If not, there may be interference with other units installed in the cabinet.

    Readjust the vertical position of the slides if necessary to obtain the correct trim panel position.

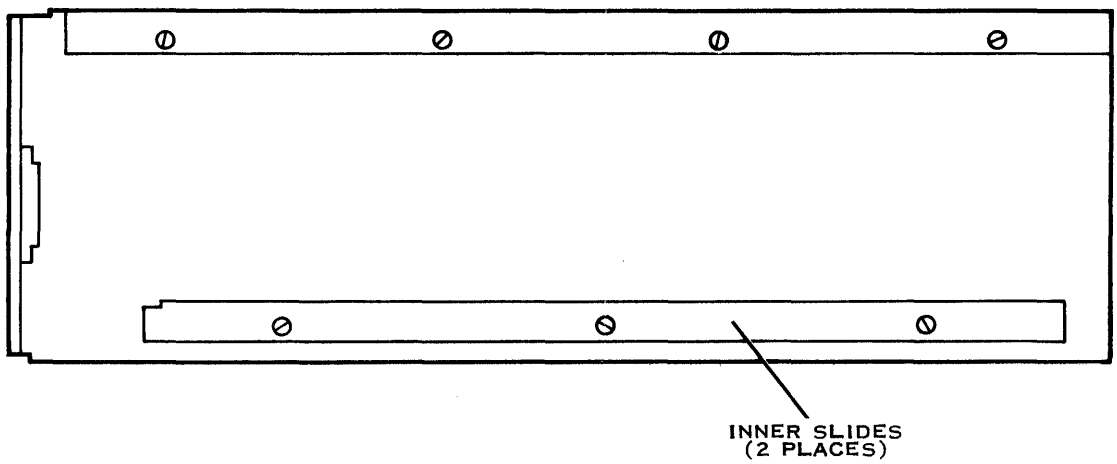

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Figure 3-8. Mounting Inner Slides to Chassis

The trim panels should not be used to lift or operate the slides. Any time that you need to pull out the slides, first remove the upper trim panel by grasping at the side and pulling straight away from the chassis.

The slides hold the chassis in the cabinet with a detent. You can release the detent by lifting slightly on the sheet metal at the top of the chassis while pulling forward.

WARNING

The detent is not sufficient if the cabinet is going to be tilted forward or moved. To secure the chassis, insert two 10-32 x 0.375 cap screws through the retaining ears into the front rail.

12. Attach three white plastic cable harness clamps (provided) to the rear panel of the chassis, oriented as shown in Figure 3-9 (WD800 only).

    The clamps have a raised ridge that forms an hourglass pattern on their surfaces. At the narrow part of the hourglass, the ridge is raised free of the surface to allow a cable tie to be inserted. Be sure to orient the clamp so that the cable tie inserts horizontally for the ac power cable, and as indicated (one horizontally, one vertically) for the clamps that hold the peripheral bus cable.

    Remove the paper backing to expose the adhesive and press the clamps into place.

13. Connect the female end of the ac power cord to the ac cord receptacle on the rear of the WD800 chassis. Dress the power cord down below and back up through the cable harness clamp located below the ac power switch cutout. Fasten the cable tie loosely (Figure 3-9). (The cable tie on the cable harness clamp is tightened later in the installation process.)

14. Dress the ac power cord out to the left vertical rack rail (viewed from the rear) and tie the cord down loosely (below the level of the chassis) on the inside of the rail. (This cable tie is also tightened later in the installation process.) Gather any extra slack in a service loop with the free end of the cord coming out the bottom. Tie down the loop on the inside of the rail.

NOTE

Be sure to isolate the ac power cord from the signal cable. In some models, you may need to route the ac power cord through the cable harness clamp and then fasten it along the top edge of the cable carrier. In these cases it is important to run the cord along the very top edge to ensure isolation from the cables along the sides of the cable carrier.

15. Plug the other end of the cord into an available ac outlet on the rail.

The chassis is now ready to be powered up.

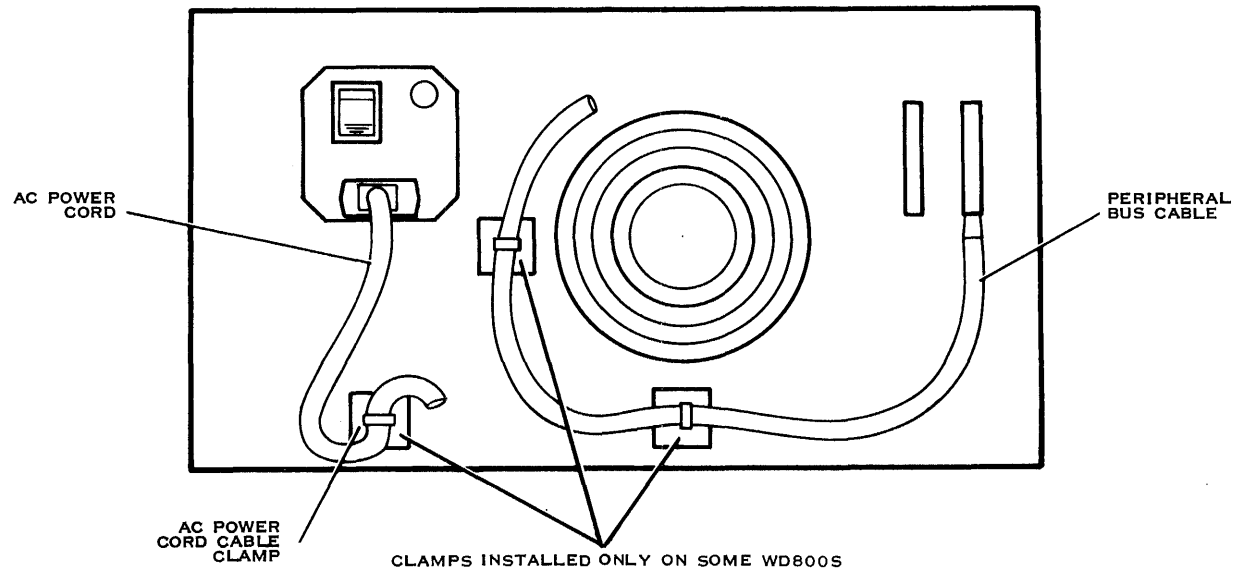

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Figure 3-9. Chassis AC Power Cord Cable Clamp

3.2.5 Chassis Stand-Alone Power-Up and Unit Select

The following procedures cover powering up the WD800 chassis (which includes automatic self-tests), verifying or changing unit selection, and verifying the tape system.

CAUTION

After unpacking and before power-up, ensure that the WD800 system has adequate time for its temperature to stabilize, particularly if it was stored at a low temperature. (See Table 1-2 for temperature gradient specification.)

3.2.5.1 Chassis Power-Up. Use the following procedure to power up the chassis:

1. Install one end of the detachable ac power cord in the rear of the WD800 chassis and the other end in an ac outlet.
2. Confirm that the PBI cable is not installed in the chassis I/O port located at the rear of the chassis.
3. Confirm that no tape cartridge is installed in the WD800 chassis.
4. Turn off the write protection on your Winchester disk drive by pressing the lower half of the write protect switch.

5. Turn the ac power switch on. The front panel status indicators respond to power-up in the following way:

   a. All four indicators turn on for about five seconds.

   b. All the indicators except TEST MODE turn off.

   c. The DISK READY indicator blinks during disk drive self-test, then stays on if the self-test is successful.

   d. The TAPE READY indicator blinks during tape drive self-test, then goes off.

   e. The SYSTEM READY indicator blinks.

   f. The test mode light goes off.

This activity indicates that the system is executing a series of self-tests. The self-tests require no operator intervention, but the progress of the self-tests can be followed by noting the activity of the status indicators.

The WD800 system formatter diagnostics first check the processor PCB to verify that it is fully functional. During this test, all indicators are on. If this self-test fails, all other testing is suspended and the indicators remain on.

If the processor self-test passes, the diagnostics go on to the disk subsystem test, at which point the system ready and tape ready indicators go off and the DISK READY indicator begins to blink. It continues to blink while the disk self-tests are performed and then turns on if the tests pass, or turns off if the tests fail. If the disk WRITE-PROTECT switch is on, the self-tests that perform disk writing will not run and will not return test failure error codes. All disk subassemblies that do not pass self-test are noted. These are displayed by the indicators in the test status mode.

If the disk self-tests pass, the self-test diagnostics go on to the optional tape subsystem. At this point the TAPE READY indicator begins to blink. The formatter then checks to see if the tape subsystem is installed. If it is not installed, the TAPE READY indicator turns off. If the tape subsystem is installed and all tape self-tests pass, the TAPE READY indicator stops blinking and turns on momentarily and then turns off. All tape subassemblies that do not pass self-test are noted. These are displayed by the indicators in the test status mode. No exercise of an installed tape cartridge occurs at this point in the diagnostics.

NOTE

After the power-up self-test completes (the test takes less than 60 seconds), the TEST MODE indicator is on and the SYSTEM READY indicator is blinking, indicating that the formatter is waiting for the formatter-to-controller interface check. This self-test cannot run because the chassis is not linked to the controller (the interface cable is not connected).

If the front panel indicators do not display the status indicated in the preceding paragraph, refer to Appendix A for further instructions.

3.2.5.2 Unit Select. To confirm a unit select address, or to change a unit select address after adding a chassis to an existing system, wait for the chassis self-test to complete the tape subsystem self-tests. At this point, the SYSTEM READY indicator begins to blink. It takes a few seconds for the formatter to enter the unit select mode.

NOTE

Once the WD800 is in the unit select mode, there is a 30-second time limit in which to update a new unit select address on the disk. During this time the SYSTEM READY light is blinking and the TEST MODE indicator is on. If the time limit is exceeded, the WD800 chassis indicators return to the normal status mode (TEST MODE indicator off).

To set the unit proceed as follows:

1. Set the disk WRITE-PROTECT switch to off.

2. To display the current unit select address on the front panel, toggle the TEST MODE/TAPE UNLOAD switch momentarily to the down (TAPE UNLOAD) position.

3. After the switch returns to the IDLE position, one of the front panel indicators is on. Refer to Table 3-2 for the unit select address corresponding to the display. (The unit select addresses are position-coded.)

4. To modify the unit select address, perform the following steps. (For a detailed discussion of the limitations on setting unit select addresses, especially in multi-chassis configurations, see the *WD800/WD800A Field Maintenance Manual*.)

   a. Toggle the TEST MODE/TAPE UNLOAD switch momentarily to the down (TAPE UNLOAD) position to change the unit select address that is displayed on the front panel indicators.

   b. Continue to toggle the TEST MODE/TAPE UNLOAD switch down to advance to the desired unit select address.

NOTE

Make sure that the disk WRITE-PROTECT switch is off before attempting to store the new unit select address.

c. To store the new unit select address, toggle the TEST MODE/TAPE UNLOAD switch momentarily to the up (TEST MODE) position. This sets the new unit select address and updates it on the disk. The front panel indicators then return to the storage system status mode.

d. To verify that the correct unit select address is stored, display the unit select address again by toggling the TEST MODE/TAPE UNLOAD switch down. If the unit select address did not change, the formatter did not update it. If the disk WRITE-PROTECT switch is on, the unit select address is not stored on the disk.

CAUTION

After the WD800 is first installed, the disk must be allowed to run for 30 minutes to provide a power-up purge cycle before attempting online system use. This period is required for proper thermal stabilization and air filtering in the sealed area of the disk assembly.

3.2.5.3 Tape System Verification. If the tape subsystem is installed, check it out using the following procedure:

1. After the front panel TEST MODE indicator turns off (approximately one minute after power-up), insert a tape cartridge.

2. Verify that the TAPE READY indicator blinks, indicating that a load operation is in progress.

3. After a delay of one to two minutes, verify that the TAPE READY indicator comes on, indicating a successful load.

If these events do not happen as described, refer to Appendix A for further information.

After completion of power-up, unit select, and tape verification, turn off all power to the chassis. This completes the stand-alone power-up checkout for the WD800 chassis.

Table 3-2. Test Status Indicators During Unit Selection

Test Status Indicators				Hex	Unit Select
1	2	3	4	(>)	Address
On	Off	Off	Off	8	Unit 0
Off	On	Off	Off	4	Unit 1
Off	Off	On	Off	2	Unit 2
Off	Off	Off	On	1	Unit 3

3.3 PROGRAMMING

This section contains the information that an assembly language programmer needs to write device service routines (DSRs) that communicate with the system. The discussion assumes that the programmer is familiar with the assembly language described in the *Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual* listed in the Preface.

Most users prefer to use Texas Instruments standard operating system software. The operating systems include DSRs and standard file manipulation schemes which are essentially independent of I/O device type. The information in this section is transparent to the operating system user. Operating system users can refer to the applicable operating system reference manual.

3.3.1 General

This section contains programming information unique to the WD800 chassis, including command descriptions and descriptions of the control and status word formats. Users wanting to perform direct disk I/O operations without using a standard operating system DSR can initiate disk commands and receive disk status as described in this section and in Section 2. The disk subsystem is discussed first, followed by the tape subsystem. Example DSRs for both tape and disk operations are given in Appendix C.

3.3.2 Disk Programming

The host communicates with the disk by means of eight words (16 bytes) that make up a control and status block (CSB). CSBs sent to the disk from the host cause the disk to perform the basic operations identified by the commands. The following paragraphs summarize the commands and the contents of the control and status words that support them.

3.3.2.1 Disk Command Summary. The disk can execute the following commands:

- Store Registers. A store registers command causes the WD800 formatter to return disk parameters (such as words per track and cylinders available per disk drive unit) to the host by means of the status words. This operation allows the operating system software to determine the parameters before using the disk system.

- Write Format. The write format command formats or reformats a disk track with header information and filler data in the data field. The write format operation is required before using unformatted disk media.

- Read Data. The read data command transfers data from a specified disk location to the formatter, which sends it on to the controller to be written in a specified location in host memory.

- Write Data. The write data command records data at a specified location on a previously formatted disk. The data is supplied to the disk by the formatter, which receives the data from a specified host memory location via the controller.

- Read ID. The read ID command returns information about a sector on the selected disk. The information is compiled from several fields of the CSB.

- Unformatted Write. The unformatted write command writes data from host memory onto the disk without regard to existing record boundaries. This command is used primarily for diagnostic purposes.

- Seek. The seek command moves the heads to a specified cylinder and then selects head 0.

- Restore. The restore command reinitializes the cylinder counter and repositions the heads of the selected drive over cylinder zero. This command is used to clear disk positioning error conditions.

- Extended Commands. The extended commands perform operations that are less commonly needed. Most extended commands perform the same operation as their non-extended equivalents. Only the read unformatted and maintenance commands differ. Read unformatted commands allow reading up to one formatter data buffer of data without checking for errors. Maintenance commands provide special fault isolation for many subsystem faults.

3.3.2.2 Disk Control and Status Block — Summary. The eight words (16 bytes) in the CSB used by the host to communicate with the WD800 chassis contain the following information:

- W0 — Disk status. Contains disk status bits.

- W1 — Command and head address. Contains command codes, head address, and control bits used during recovery operations.

- W2 — Sector. Specifies the starting sector address and number of sectors per record.

- W3 — Cylinder address. Contains the cylinder address.

- W4 — Transfer byte count. Specifies the number of bytes to be transferred between disk and host memory.

- W5 — Contains host LSB buffer address.

- W6 — Contains unit select and host MSB buffer address.

- W7 — Command Completion Status. Contains command completion status bits.

The fields of the CSB reserved for host/controller communication are not discussed in this section. The fields of the CSB that the controller exchanges with the formatter in the WD800 provide all the necessary control and status information for the disk.

3.3.3 Disk Control and Status Word Formats

This section describes the fields of the control and status word formats that apply to the disk in the WD800 chassis (Figure 3-10).

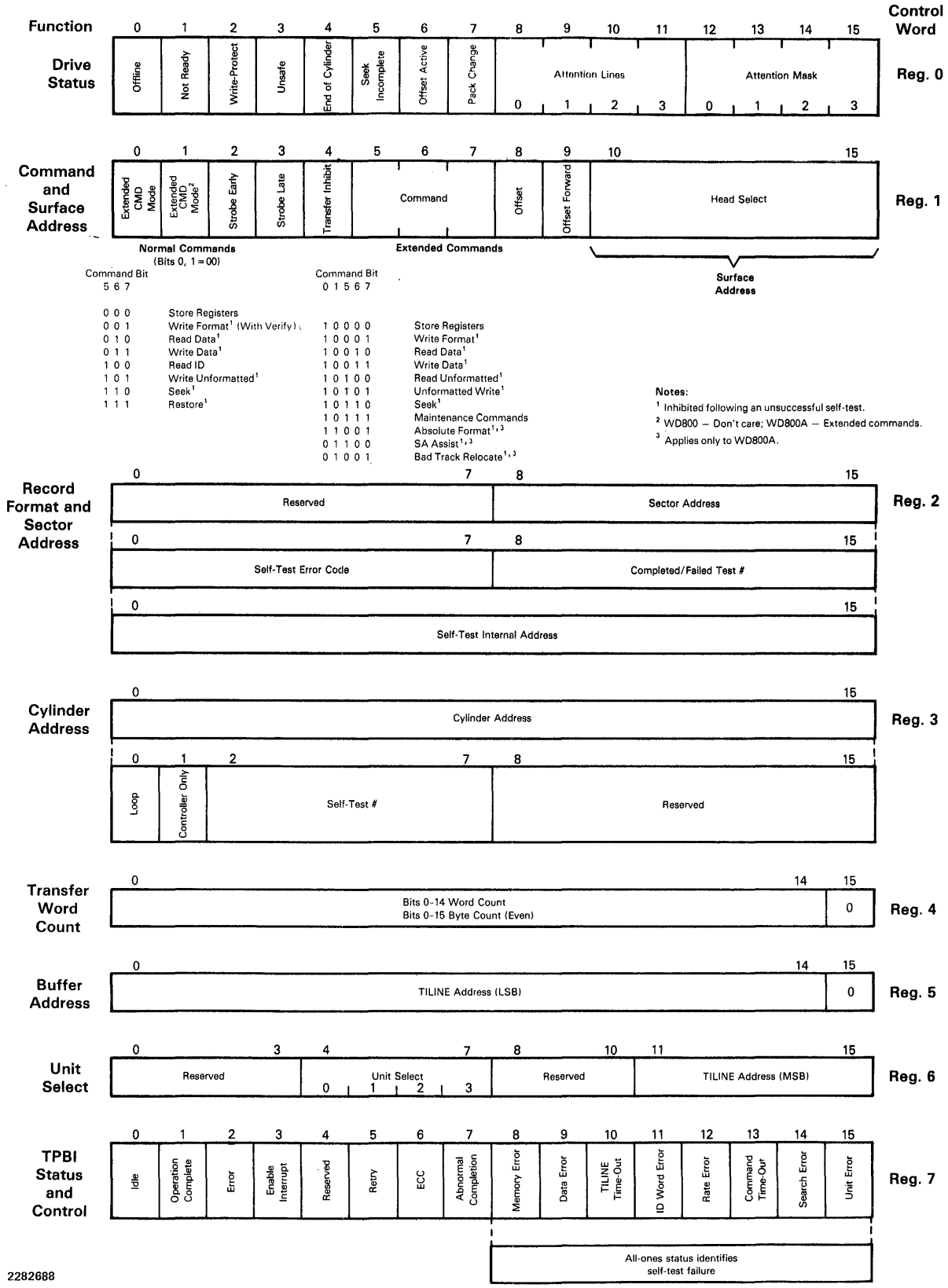


Figure 3-10. Disk Control and Status Word Formats for Direct Disk I/O Operations

3.3.3.1 W0 — Disk Status. W0 reports disk status. Only the left byte is used by the formatter; the right byte is reserved.

Offline — W0, Bit 0. The offline bit is active (1) if the drive is powered down or disconnected from the controller, or if the formatter is not in communication with the controller.

Not Ready — W0, Bit 1. This bit is active (1) when the disk is busy performing a seek or restore command. W0, bit 1 is set whenever a seek or restore command is issued (if the destination cylinder is not the current one); the resulting disk status is returned with the CSB. The bit remains set until the destination track is reached and then goes inactive (0). The updated status byte is then transferred to the controller.

Write-Protect — W0, Bit 2. Bit 2 is set when the write-protect status of the selected unit is on. The write-protect status is set with the WRITE-PROTECT switch on the WD800 front panel. When activated, the write-protect circuit inhibits disk drive write logic, and neither format information nor data can be written on the disk.

Unsafe — W0, Bit 3. A set drive unsafe bit indicates that a fault condition exists that prevents a disk operation (except for a restore operation) from being executed. This bit is set when the formatter detects a disk drive fatal error. W0, bit 3 and the pack change bit (bit 7) are both set if a command is issued for a drive unit that has not been identified previously to software by a store registers command. A power-down cycle, for example, results in unsafe status the next time the drive unit is selected. A restore and store registers command clears unsafe status if the unsafe condition no longer exists.

End of Cylinder — W0, Bit 4. The end of cylinder bit indicates that an invalid head number has been specified in the CSB.

Seek Incomplete — W0, Bit 5. The seek incomplete bit is set if the head carriage fails to locate the specified cylinder. For example, if the cylinder address is out of range, the operation fails and reports seek incomplete status. Some seek incomplete errors result from an error in the disk drive positioning logic. The system can attempt to recover from these errors by a restore operation.

Offset Active — W0, Bit 6. This bit is not supported by the WD800 system and is always set to zero by the formatter.

Pack Change — W0, Bit 7. This bit is set to 1 (with the unsafe bit) whenever the device comes online (the offline bit goes from active to inactive), or the formatter senses the loss and then regaining of CTLPRES. Pack change status is cleared only by successful execution of a restore command.

3.3.3.2 W1 — Command and Head Address. W1 contains the command codes, the head address, and control bits used during recovery operations.

Command Code — W1, Bits 0, 1, and 5 Through 7. These bits make up the command field of W1. Table 3-3 shows the valid commands for the disk and the formatter. Bits 0 and 1 contain a command select code which is used to select either the normal or the extended command set. Bits 5 through 7 provide a specific command code as defined in Table 3-3.

Table 3-3. Disk Commands

Normal Commands	Command Name	Extended Commands	Command Name
>00	Store Registers		
>01	Format Track[1]	>80	Store Registers
>02	Read Data[1,2]	>81	Format Track (With Verify)[1]
>03	Write Data[1]	>82	Read Data[1,2]
>04	Read ID	>83	Write Data[1]
>05	Unformatted Write[1]	>84	Read Unformatted[1,2]
>06	Seek[1]	>85	Unformatted Write[1]
>07	Restore[1]	>86	Seek[1]
		>87	Maintenance Commands
		>41	Bad Track Relocate[1,3]
		>44	Surface Analysis Assist[3]
		>C1	Absolute Format[3] (Without Verify)

Notes:

Hexadecimal values (preceded by >) are the values in the left byte of W1.

[1] Commands are inhibited following an unsuccessful self-test. A >XXFF is reported in W7 when self-test failure results in inhibiting a command.

[2] Read data transfer to the bus is inhibited by the formatter if the transfer inhibit (bit 4) is set (1).

[3] WD800A only.

After receiving a CSB, the formatter validates the command and the required parameter bytes and begins executing the command. When the command completes or aborts execution, the formatter updates the CSB and returns it to the controller.

The formatter can detect two types of error conditions that abort command execution: device faults and command errors. Device faults are hardware error conditions that are detected independently of commands issued by the controller (for example, motor speed errors, off track, and so on). They are reported by setting the unsafe status bit (W0, bit 3). Command errors are errors resulting from disk actions initiated by controller-issued commands (data errors, ID errors, and so on), or from illegal values within the CSB (such as illegal parameters). The formatter reports command errors by setting command status bits.

If the command issued from the controller is a seek or a restore command, the execution of the command is slightly different. After the formatter initiates the seek or the restore operation, it sets the not ready bit (if not already on the specified cylinder), and returns the CSB to the controller. The disk continues the operation until it completes. At that point, the formatter clears the not ready bit, and returns the updated disk status to the controller.

Strobe Early and Strobe Late Bits — W1, Bits 2 and 3. Bits 2 and 3 are strobe early and strobe late bits, respectively. On the WD800, these bits modify data recovery margins artificially for testing. High thresholds are selected by setting bit 2 (in which case bit 3 can be either one or zero), and low thresholds are selected by setting bit 3 (with bit 2 cleared to zero). On the **WD800A**, these bits are ignored.

Transfer Inhibit — W1, Bit 4. When transfer inhibit is set, data is read from the selected disk, but is not transferred to the host. The transfer inhibit function allows the operating system software to check data integrity of a record without having to provide a memory buffer area to hold the data. If a read error (ECC or other error) is detected, that error is reported to the host, making host data comparisons unnecessary.

Not Used — W1, Bits 8 and 9. Bits 8 and 9 are track offset bits. The WD800 does not support track offsets, so bits 8 and 9 are ignored.

Head Address (WD800) — W1, Bits 10 Through 15. Bits 10 through 15 select a read/write head and associated platter surface. Valid head addresses are 0 through 2 for two-platter WD800s and 0 through 6 for four-platter WD800s. The store registers command gives the acceptable values for each disk on the system.

Head Address (WD800A) — W1, Bits 10 Through 15. Bits 10 through 15 select a read/write head and associated platter surface. Valid head addresses are 0 through 4 for three-platter **WD800A**s, 0 through 8 for five-platter **WD800A**s, and 0 through 14 for eight-platter **WD800A**s. The store registers command gives the acceptable values for each disk on the system.

3.3.3.3 W2 — Sectors per Record and Sector Address. Control W2 determines the number of sectors per record and the address of each sector. This word is used to update the sector address during disk drive operations and can be read for diagnostic purposes.

Sectors per Record — W2, Bits 0 Through 7. Since the recording format is always one sector per record, these bits are ignored by the formatter. To ensure compatibility with other TI disk systems, however, these bits are always set to >01. If the formatter fails to pass a self-test command, it identifies the failure by reporting an error code in these bits.

Sector Address — W2, Bits 8 Through 15. These bits select the starting sector for any read or write operation. If they specify a starting sector address larger than the largest valid sector address, a command time-out status results because the formatter cannot locate the specified starting sector address. The valid sector addresses for the WD800 are 0 through 36 (>0 through >24). For the **WD800A**, the valid sector addresses are 0 through 32 (>0 through >20). The contents of bits 8 through 15 are updated by the formatter at the completion or error termination of a command.

W2 can also contain a self-test failure code or an internal memory address for certain extended commands.

3.3.3.4 W3 — Cylinder Address or Maintenance Commands. W3 selects the cylinder address to which the disk seeks for a read, write, or seek operation. Normally, this word is used only for control, but the cylinder address is updated during disk operations and can be read for diagnostic purposes.

The cylinder address of W3, combined with the head address in W1 and the sector address in W2, make up a complete address that locates a record on the disk. The user cylinder addresses for the WD800 are 0 through 650 (>0 through >289). The user cylinder addresses for the **WD800A** are 0 through 910 (>0 through >38E) for the 3- and 5-platter disks and 0 through 903 (>0 through >387) for the 8-platter disks.

An invalid cylinder address results in termination with the unit error status bit (in control word 7) set. The disk status (control word 0) then indicates seek incomplete status. During self-test, this field also specifies test numbers. (See Appendix A for further information.)

NOTE

Diagnostics can address two reserved cylinders, 652 and 653 on the WD800. For the **WD800A**, diagnostics can address reserved cylinders 921, 922, and 923 on the 3-platter and 5-platter disks and cylinders 914, 915, and 916 on the 8-platter disks.

When the maintenance commands are enabled, bits 0 through 7 of W3 have alternate definitions. In this case, bit 0 is the loop bit; it causes a self-test command to repeat (thus providing scope loops) until a reset is received. Bit 1 is the controller-only bit; it reserves the maintenance command for the controller. Bits 2 through 7 specify the individual maintenance commands that the formatter (or controller) performs. Appendix A includes a list of these commands.

3.3.3.5 W4 — Transfer Byte Count. The WD800 uses byte counts from > 0 to > FFFE. Only even byte counts are acceptable (odd byte counts are truncated by the formatter).

3.3.3.6 W7 — Command Completion Status. Bits 0 through 4 of the command completion status word are reserved. Bits 5 through 7, bit 9, bit 11, and bits 13 through 15 provide details about the completion of the last command executed.

Retry — W7, Bit 5. Bit 5 is set by the formatter to indicate that the formatter performed a retry during the last operation because an error was detected.

ECC Corrected — W7, Bit 6. When bit 6 is set, it means that the ECC algorithm attempted to correct bits somewhere in the data of the sector just read (or during the last operation, for multiple sector operations).

Abnormal Completion — W7, Bit 7. This bit is set whenever the WD800 detects a peripheral bus error in data transmission to or from the host. Section 2 discusses the remapping of this bit by the controller.

Data Error — W7, Bit 9. W7, bit 9 is set during a read operation if the ECC check detected an error but was unable to correct the data.

ID Error — W7, Bit 11. This bit is set whenever the formatter fails to find or verify the ID field of the specified sector in read or write operations (causes command termination).

Command Time-Out — W7, Bit 13. The formatter allots a predetermined amount of time for each operation performed in a command execution. If the disk fails to complete the operation before the formatter timer expires, command time-out is set and the operation terminates.

Search Error — W7, Bit 14. If the formatter does not detect a data field within a fail-safe time period after locating the correct address field, the retry bit is set, and the formatter repeats the operation. If the operation is then successful, the command continues normally. If the retry count is exceeded, bit 14 is set and the command terminates.

Summary Unit Error Status Bit — W7, Bit 15. Whenever this bit is set, the device status in W0 must be examined.

3.3.4 Detailed Disk Command Descriptions

The disk executes commands of three different types: normal commands, extended mode commands, and maintenance commands.

3.3.4.1 Normal Commands. The normal or nonextended commands are the eight commands for which the extended mode bits (W1, bits 0 and 1) are not set. These commands are store registers, write format, read data, write data, read ID, unformatted write, seek, and restore. These basic commands are used for most normal data storage and retrieval operations.

Store Registers Command (W1 = X0XX). The store registers command provides a means for the operating system software to interrogate a disk system to determine critical parameters, such as words per track and cylinders available per drive unit. This command causes the WD800 to send one, two, or three words (as specified by the transfer byte count in W4) to the host memory. The three words contain the following information:

- W1 — W1 is the total number of formatted words that can be recorded on a disk track (>1280 for the WD800, >1080 for the **WD800A**).
- W2 — W2, bits 0 through 7 specify the number of sectors per track (37 for WD800, 33 for **WD800A**), and bits 8 through 15 specify the number of bytes of overhead per record (>2500 for the WD800, >2100 for the **WD800A**).
- W3 — W3, bits 0 through 4 specify the number of heads per cylinder and bits 5 through 15 specify the number of cylinders per drive. The values for the WD800 are >1A8B for two-platter drives and >3A8B for four-platter drives. The values for the **WD800A** are >2B8F for three-platter drives, >4B8F for five-platter drives, and >7B88 for eight-platter drives.

Write Format Command (W1 = >01XX). The write format command formats a new disk or reformats a disk already in service. One complete track is formatted per command. After command initialization, the disk formatter performs the following operations:

1. Checks for unit errors by examining disk status and aborts if it encounters offline, not ready, unsafe, write-protect, or seek incomplete errors.
2. On a **WD800A**, the formatter searches the bad track map for a match with the requested track. If the requested track is bad, the relocated track replaces it.
3. Seeks to the specified cylinder.

4. Selects the specified head address.

5. The formatter on the **WD800A** verifies the header and checks for a bad track flag if the header is not verified.

The format operation consists of a full track erase followed by a write format (on the **WD800A**, erase does not precede write format) of all 37 sectors (33 sectors on the **WD800A**) in a predetermined interleave sequence.

The sector format divides the sector into two fields: an address field and a data field. The address field is written only during format commands. Each address field contains a unique disk address consisting of the following elements:

- Synchronization (sync) field (12 bytes) for synchronizing read circuits
- Address mark 1 (1 byte) for address sync
- ID bytes 1 and 2 (1 byte each) containing the head and cylinder address
- ID byte 3 (1 byte) containing the logical sector address
- ECC (4 bytes) containing the error correcting code bytes
- Postamble (7 bytes on the WD800, 6 bytes on the **WD800A**) forming a trailing guard band including 3 bytes (2 bytes on the **WD800A**) for write-over when writing data

The data field contains user data and consists of the following elements:

- Sync detect reset (1 byte) for resetting bit detector (**WD800A** only)
- Sync field (12 bytes) for synchronizing read circuits
- Address mark 2 (1 byte) indicating that a data field follows
- Data field (256 bytes) containing user data
- ECC (4 bytes) containing the error correcting code bytes
- Data field postamble (4 bytes) forming an interrecord gap and trailing guard band
- On the **WD800A** only, an additional byte containing a 2-byte write splice gap and second data postamble of 7 bytes

No erased gap is written between sectors. Any formatted area left over at the end of a sector due to timing skew appears as extra postamble and is ignored by the read circuitry.

Read Data Command (W1 = >X2XX, or >XAXX With Transfer Inhibit). The read data command words identify a record location and specify the number of bytes to be transferred from this location.

After command initialization, the formatter performs the following operations:

1. Checks for unit errors by examining disk status. The formatter aborts if it encounters off-line, not ready, unsafe, or seek incomplete.

2. On the **WD800A**, the formatter searches the bad track map for a match with the requested track. If the requested track is bad, the relocated track replaces the bad track.

3. Seeks to the specified cylinder.

4. Sets the specified head address.

5. Verifies the header. On a **WD800A**, the formatter checks for a bad track flag if the header does not verify.

6. Waits for the correct starting sector.

7. Reads the requested number of sectors, buffering the data bytes from up to four sectors at a time.

8. Checks for ECC errors on the data field of each sector that it reads. If it finds an error, the formatter rereads the sector up to three times before deciding whether ECC correction is needed or whether to report an error.

9. Transfers the data to the host if transfer inhibit is not set. (Data is transferred even if the ECC checks fail.)

A failure to verify any part of the ID field of the desired sector results in an ID error status (W7, bit 11), and terminates the read data operation.

When the formatter encounters the end of the sector, but the remaining transfer word count is nonzero, the formatter automatically continues reading data on the next sequential logical sector, if it exists.

The formatter automatically switches heads or cylinders if necessary to access the next logical sector. When the formatter encounters the end of a track and the remaining transfer word count is nonzero, the formatter does the following: increments the head address to the next track, checks the bad track map to see if the new track is bad (**WD800A** only), seeks to the relocated track if the new track is bad, waits for sector zero, and continues to read words from the disk and to transfer them to the host, if transfer inhibit is not specified. When the formatter encounters the end of a cylinder and the remaining transfer word count is nonzero, the formatter automatically increments the cylinder number, selects head address zero, checks the bad track map to see if the new track is bad (**WD800A** only), seeks to the appropriate track, waits for sector zero, and continues the normal read operation.

Write Data Command (W1 = >X3XX). The write data command causes the formatter to record data in a sector on a previously formatted track, or to write over a previously recorded sector. After command initialization, the disk formatter performs the following operations:

1. Checks for unit errors by examining disk status, and aborts if it encounters offline, not ready, unsafe, write-protect, or seek incomplete.

2. On a **WD800A**, the formatter searches the bad track map for a match with the requested track. If the requested track is bad, the relocated track replaces it.

3. Seeks to the specified cylinder.

4. Selects the specified head address.

5. Verifies the header. On a **WD800A**, the formatter checks for a bad track flag if the header does not verify.

6. Waits for the correct starting sector to pass under the head.

7. Writes the appropriate preamble and address mark preceding the data field.

8. Writes data from the specified memory location.

9. Appends ECC characters to the end of each sector as it is written.

If the ID field for the desired sector cannot be verified, the write operation is terminated with an ID status error.

Unless an error condition is encountered, data is written on the disk until the specified number of words is transferred. The data words are written on the disk sector by sector. After the last data word of the sector is written, the formatter records the ECC characters calculated for the data.

When the formatter encounters the end of a track and the remaining transfer byte count is non-zero, the formatter does the following: increments the head address to the next track in the cylinder, checks the bad track map to see if the new track is bad (**WD800A** only), seeks to the relocated track if the new track is bad (**WD800A** only), and resumes the write data operation at sector zero.

When the formatter encounters the end of a cylinder and the remaining transfer byte count is non-zero, the formatter automatically increments the cylinder number, selects head address zero, checks the bad track map to see if the new track is bad (**WD800A** only), seeks to the appropriate track, and resumes the write operation at sector zero. Cylinder, head, and sector information is updated as it changes, and the byte count decrements to zero unless an error terminates the write before completion. This procedure is typical for any read or write operation.

Read ID Command (W1 = >04XX). A read ID command transfers information about a sector on the selected disk to the controller. No action is taken on the disk drive for this command. The format of the transferred information (Figure 3-11) consists of three words that give the cylinder and head number, the number of sectors per record (always equal to one) and the sector number, and the number of data words per record (the data capacity of the sector).

Unformatted Write Command (W1 = >X5XX). An unformatted write command transfers data from a specified host address to a specified disk address until the maximum available buffer is filled or the specified byte count is exhausted. After command initialization, the formatter seeks to the specified cylinder, selects the specified head address, detects the beginning of sector, generates the sector preamble and sync field, and writes data on the disk. All data is written consecutively without regard to existing sector boundaries until the specified number of words is transferred, or until a termination condition is encountered. The maximum byte count for the WD800 unformatted write command is >03F3. The maximum byte count for the **WD800A** unformatted write command is >400.

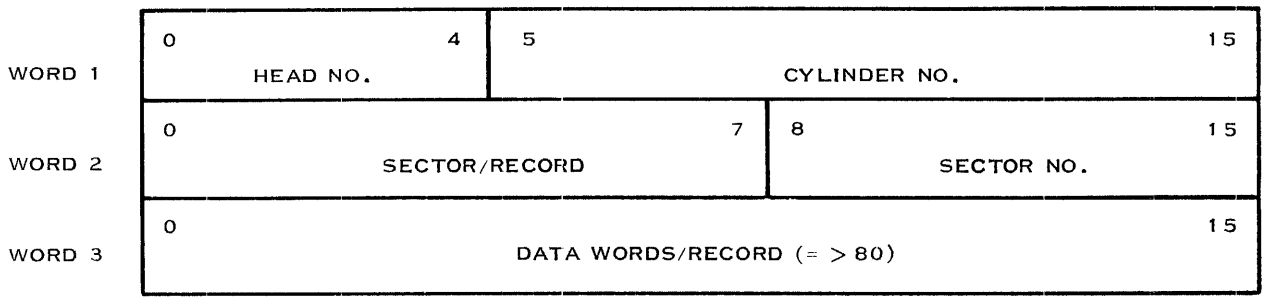


Figure 3-11. Read ID Format

Seek Command (W1 = >X6XX). The seek command moves the heads of the selected unit to a specified cylinder in anticipation of a future data transfer. On a **WD800A**, the formatter bad track map is searched for a match with the requested track before the seek is executed. If a match is found, (that is, the requested track is bad), the seek is made to the cylinder of the replacement track instead of the cylinder of the requested bad track. The seek command always selects head 0 after executing the seek.

Upon receipt of the seek command, the formatter checks status on the selected drive and initiates the physical seek operation. The formatter then returns the CSB with not ready status and waits for the seek to complete. When the seek completes or terminates with error, the formatter returns the disk status with the not ready status cleared.

Restore Command (W1 = >07XX). The restore command reinitializes the cylinder counter and repositions the heads of the selected disk drive unit over cylinder zero. The restore command is generally used to clear an unsafe condition at the disk drive. This command is required if seek incomplete or unsafe status is detected. The formatter sequence of communication with the host is the same for a restore as it is for a seek (it returns the CSB with not ready status set, waits for completion or error termination, and returns disk status with not ready cleared). An error encountered in a restore operation results in disk unsafe status.

3.3.4.2 Extended Mode Commands. The extended mode commands are those commands for which the extended mode bits (W1, bits 0 and/or 1) are set. The extended mode bit allows the command code field (W1, bits 5 through 7) to select from an additional set of commands. These commands are less commonly used during the course of data storage and retrieval operations.

Refer to Table 2-1 for the complete set of nonextended and extended mode commands. Except for the extended read unformatted command and the command used to enable the maintenance commands, extended mode commands perform functions identical to those of the nonextended commands.

Unformatted Read Command (W1 = >84XX). An unformatted read command allows the reading of a specified number of bytes (up to the number that one formatter data buffer can hold) on a track without checking for data errors. After command initialization, the formatter seeks to the specified cylinder, selects the desired head, verifies that the header is correct, detects the specified sector, and starts to read data either from the first byte of the header following the address mark (on a WD800), or from the first byte of data following the data address mark (on a **WD800A**). The formatter continues to read data until the specified number of bytes is read, or until an error condition causes the command to terminate. The maximum number of bytes that the WD800 unformatted read command can handle is >400.

If the number of bytes specified is greater than the bytes per sector, the formatter continues reading past the end of the data field.

3.3.4.3 Maintenance Commands (W1 = >87XX). This code executes the maintenance command specified by the left byte of W3. The *WD800/WD800A Field Maintenance Manual* describes all of the maintenance commands (see the Preface). For convenience, Appendix A includes a list of the test commands that are supported.

Certain maintenance commands hang the system in a test loop until an I/O reset or power reset aborts the test. Refer to the *WD800/WD800A Field Maintenance Manual* for a complete description of the maintenance command routines.

3.3.5 Tape Programming

CSBs sent to the formatter from the host cause the tape to perform the basic operations that the commands identify. The following paragraphs summarize the commands and the contents of the control and status words that support them.

3.3.5.1 Tape Command Summary. The tape transport can execute the following commands:

- Write End-of-File. The write end-of-file command causes a file mark to be written and then verified on the tape.
- Record Skip Reverse. In the record skip reverse operation, the tape is reversed over a specified number of records with no transfer of data to the controller.
- Read Forward. The read forward command reads data from a record on tape and transfers it to the controller.
- Record Skip Forward. The record skip forward operation allows records to be skipped in the forward direction without any transfer of data.
- Write Forward. The write forward command transfers data from the controller to be recorded on tape. Each write operation creates one record; the operation includes read-after-write error checking to guarantee the data written.

- Erase. The erase operation erases a length of tape corresponding to the number of bytes specified.

- Read Transport Status. The read transport status command allows the controller to read current tape status from the formatter without performing any operation on the tape.

- Rewind. The rewind command positions the tape at the beginning-of-tape (BOT) and selects the first track as the location for the next operation.

- Unload. The unload command causes the tape drive to move the tape to the unload position just outside the innermost end-of-tape (EOT) hole.

- NOP. The no-operation (NOP) command is identical to the read transport status command.

- Unformatted Write. The unformatted write command causes the formatter to write data provided by the controller directly onto the tape without first formatting it in any way beyond providing a preamble and sync character. Read-after-write error checking is inhibited in unformatted write operations.

- Unformatted Read. The unformatted read command causes the formatter to read data from the tape (without regard for normal tape format) and to transfer that data to the controller. No CRC error checking is done in unformatted reads.

- Maintenance Commands. These commands cause components of the tape storage system to perform self-tests and diagnostic commands (paragraph 3.3.7.2).

3.3.5.2 Tape Control and Status Block — Summary. The eight words (16 bytes) in the CSB used by the host to communicate with the tape transport in the WD800 chassis contain the following information:

- W0 — Tape status. W0 contains tape status bits.

- W1 — Read overflow status count. W1 indicates the number of data bytes between the last data byte requested by the controller and the last data byte in the record.

- W2 — Maintenance command status. W2 is normally used to report the self-test error code and test number when W7 reports self-test failure (>XXFF).

- W3 — Read offset or maintenance command. W3 usually specifies read offset (the number of data bytes between the beginning of a record and the first byte requested by the controller). W3 can also specify the maintenance command code.

- W4 — Byte/record count. W4 contains a count that can be interpreted as the number of bytes to read or write, the number of records to skip, or the number of data blocks to erase.

- W5 — Not used by the tape system (contains host buffer address).

- W6 — Command. W6 contains the tape system command code.
- W7 — Tape command completion status. W7 contains command completion status bits.

The fields of the CSB reserved for host/controller communication are not discussed in this section. The fields of the CSB that the controller exchanges with the formatter in the WD800 provide all the necessary control and status information for the tape system.

3.3.6 Tape Control and Status Word Formats

This section describes the fields of the control and status word formats that apply to the tape system in the WD800 chassis (Figure 3-12).

3.3.6.1 W0 — Tape Status. W0 reports tape status. The formatter uses only the left byte; the right byte is reserved for use by the controller and the host.

Offline — W0, Bit 0. The offline bit is active (1) when no tape is installed or when an unload operation is done on an installed tape. (To reset the bit, reinsert the tape and reload it.) Offline also sets to report a fatal error during command execution, which aborts the command and sets the tape error bit (W7, bit 15).

Beginning-of-Tape (BOT) — W0, Bit 1. This bit is active (1) when the tape is positioned at the physical beginning of the tape after a load or rewind operation. If set under certain circumstances by a skip reverse command, the BOT bit is considered an error bit.

End-of-Record (EOR) — W0, Bit 2. The EOR bit reports that a read operation has crossed a logical record boundary. Tape error (W7, bit 15) is also set with EOR status. This bit is reset when another tape command begins to execute.

End-of-File (EOF) — W0, Bit 3. The EOF bit reports that an operation (read, skip forward, or skip reverse) crossed a file mark, or that the tape is currently located at an EOF mark. In the former case, tape error status is reported with the EOF status; both bits clear when another tape command begins to execute.

End-of-Tape (EOT) — W0, Bit 4. This bit is set (1) when an operation (write, read, erase, or skip forward) moves forward past the EOT warning marker on the last track. This sets the tape error and EOT bits. If the tape continues forward to the physical end of the tape, the offline and tape error bits are also set.

Write-Protect — W0, Bit 5. When this bit is set, writing on the tape is not permitted; tape error status is reported if a write operation (write forward, erase, or write EOF) is attempted.

Rewind in Progress — W0, Bit 6. This bit is set when a rewind, unload, or track switch operation initiates. It is then cleared when the operation completes.

Command Time-Out — W0, Bit 7. This bit is active (1) when a command aborts because of fatal error conditions resulting from the use of improper parameters or other error conditions not covered by the other error status bits. This bit is set by read or skip commands when 10 seconds pass without finding a record on the tape. Tape error status also sets with this bit. This bit resets when another tape command begins to execute.

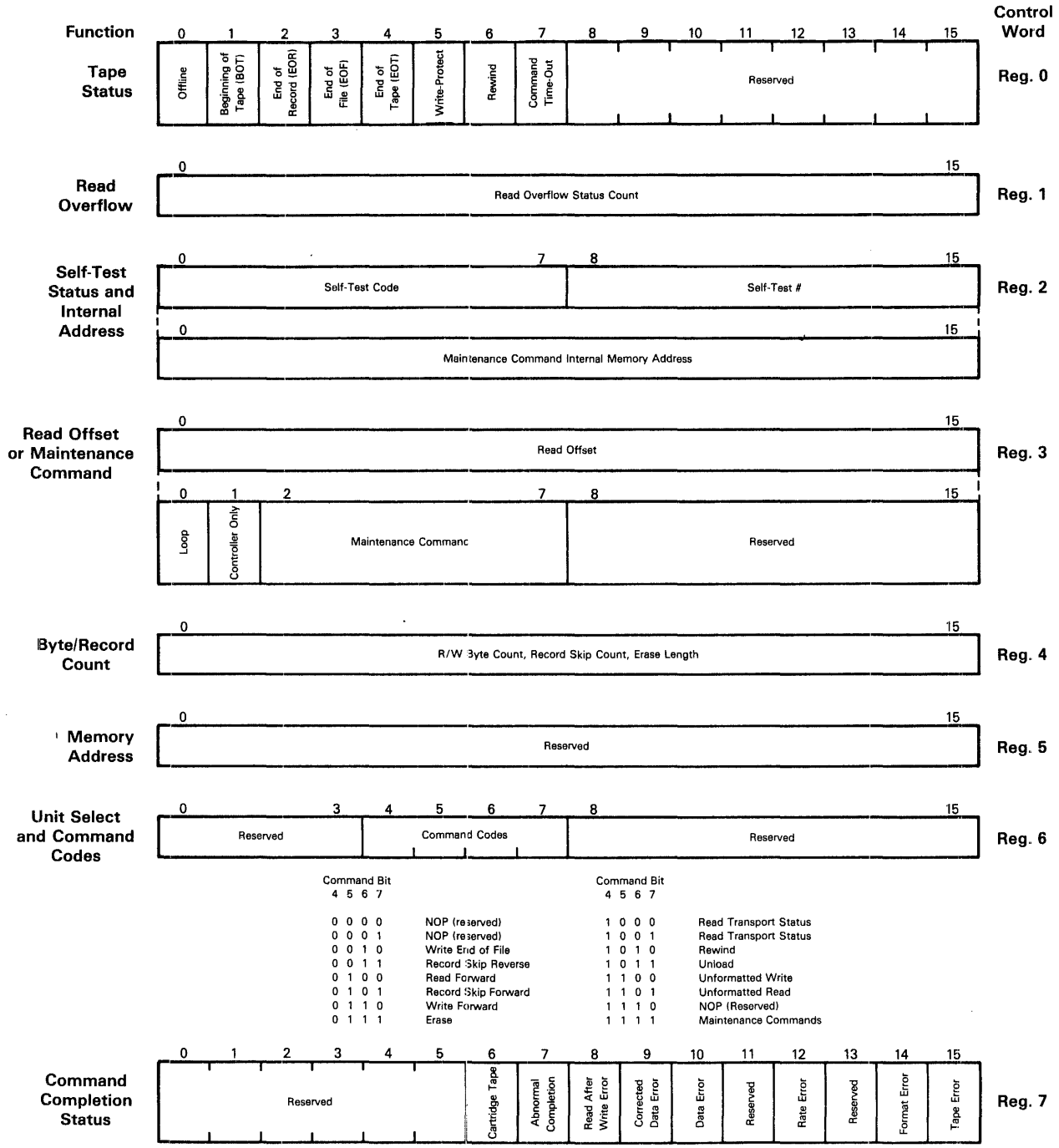


Figure 3-12. Tape Control and Status Word Formats

3.3.6.2 W1 — Read Overflow. The formatter returns the read overflow count to the controller following a read command to report the number of data bytes between the last data byte transferred and the last data byte in the record.

3.3.6.3 W2 — Self-Test Status and Internal Address. When self-test failure is reported in W7 (>XXFF), W2 reports the self-test error code and test number of the failed test. When the self-tests fail, any command except a maintenance command aborts, and self-test failure status is returned to the host. This word is also used during two maintenance commands (read and write peripheral memory) to specify a memory address internal to the formatter.

Self-Test Code — W2, Bits 0 Through 7. Bits 0 through 7 give the error code for the failed self-test.

Self-Test Number — W2, Bits 8 Through 15. Bits 8 through 15 give the number of the self-test that failed.

3.3.6.4 W3 — Read Offset or Maintenance Command. The controller normally uses W3 (bits 0 through 15) to specify the read offset (the number of data bytes between the beginning of a record and the first byte transferred to the controller). This interpretation of W3 is used with the read/write character count in W4 to pick out a segment of a tape record and send that segment to the controller.

The alternate interpretation of W3 (bit values specified in the following paragraphs) is used for maintenance commands to specify certain parameters and a six-bit command code. Only the left byte is used for maintenance commands.

Loop — W3, Bit 0. When bit 0 is set, the self-test repeats until the device receives a reset.

Controller Only — W3, Bit 1. This bit specifies whether the controller or formatter is to perform the self-test command. If this bit is zero, the formatter performs the test. If it is one, the controller performs the test.

Maintenance Command — W3, Bits 2 Through 7. These bits specify the self-test or maintenance command to be performed. If this field is all zeros, all the self-tests run that do not require operator intervention. Appendix A includes a list of the maintenance commands.

3.3.6.5 W4 — Byte/Record Count. The formatter interprets the number in this word (depending on the command) as a read operation byte count, write operation byte count, skip operation record count, or erase length. The count is updated by the formatter as the command executes and is returned with the CSB. If the operation terminates abnormally, the contents of W4 can be read to determine how much of the operation completed before termination.

W4 is normally under formatter control; however, if the controller terminates an operation because it detects a problem, the controller is responsible for a correct count representing the number of bytes or records not transferred.

3.3.6.6 W6 — Command. W6 specifies the four-bit tape system command code. Only part of the left byte is used; the rest of the word is reserved.

Reserved — W6, Bits 0 Through 3. The tape system does not use these bits.

Command — W6, Bits 4 Through 7. These bits make up the command field for the tape system. Table 3-4 shows the valid commands for the tape and formatter. Paragraph 3.3.7 discusses these commands.

Table 3-4. Tape Commands

Command Code	Command Name
>0	NOP (reserved)
>1	NOP (reserved)
>2	Write end-of-file
>3	Record skip reverse
>4	Read forward
>5	Record skip forward
>6	Write forward
>7	Erase
>8	Read transport status
>9	Read transport status
>A	Rewind
>B	Unload
>C	Unformatted write
>D	Unformatted read
>E	NOP (reserved)
>F	Maintenance commands

3.3.6.7 W7 — Command Completion Status. W7 contains status information about the tape system and command execution. The contents of W7 ought to be checked at the end of each operation to determine whether the operation succeeded, and if not, what errors occurred. This error information can be used to select a recovery scheme.

Reserved — W7, Bits 0 Through 5. The tape system does not use these bits.

Cartridge Tape — W7, Bit 6. The formatter controls this bit, but the host can also write it. The formatter sets this bit to a one to indicate that the transport media is a cartridge tape.

Abnormal Completion — W7, Bit 7. The formatter sets abnormal completion when it detects a peripheral bus error (such as a parity error) during execution of a command. See Section 2 for the controller action that results and the other uses of this bit.

Read-After-Write Error — W7, Bit 8. The formatter sets this bit when a read-after-write CRC error is detected in a write forward command. It is also set when the format error bit (W7, bit 14) reports a media dropout in a write forward operation.

Corrected Data Error — W7, Bit 9. The tape system does not support error correction. When this bit is set, a CRC error was detected during a read operation in a portion of the record not being transferred to the host (the offset or overflow regions).

Data Error — W7, Bit 10. The formatter sets this bit when a CRC error is detected in the data transferred during a read command. This bit is also set during a write EOF command if the EOF verification fails.

Reserved — W7, Bit 11. The tape system does not use this bit.

Rate Error — W7, Bit 12. This bit is set when the system does not meet the data transfer demand rate of the tape. The failure can occur for one of two reasons: either the tape data buffer overflows during a read operation because the host fails to empty it fast enough, or it runs out of data during a write operation because the tape empties it faster than the host can refill it.

Reserved — W7, Bit 13. This bit is not used by the tape system.

Format Error — W7, Bit 14. The formatter sets this bit when it detects that the format of the tape is bad (for instance, when it detects a header verification error), or coincidentally with a read-after-write error, when a media dropout is detected during write operations.

Tape Error — W7, Bit 15. Bit 15 is an error summary bit; when it is set to one, bits 0 through 7 in W0 report the exact tape error condition. If bit 15 is set, the host ought to examine W0 to determine transport status.

3.3.7 Detailed Tape Command Descriptions

The tape executes commands of two different types: normal commands and special commands, including the maintenance commands (refer to Table A-5).

3.3.7.1 Normal Commands. The normal commands include all of the usual operations performed in the course of reading from or writing to a tape.

NOP (W6 = X0XX, X1XX, XEXX). The NOP commands do not execute any tape operations. Instead, they update W0 to report the current status of the tape and report no error unless the tape is offline (which sets offline and tape error).

Write End-of-File (W6 = X2XX). The write end-of-file command marks off file boundaries by writing a record containing a unique pattern that can be read in either forward or reverse. The EOF mark pattern is written and checked by read-after-write; the tape then reverses and the heads read back across the mark to confirm that it can be detected when the tape is moving in the reverse direction. Then the tape moves forward across the mark again for a final check and stops just beyond the mark. The EOF mark includes a preceding six-inch erased gap.

The write EOF command reports errors under the following conditions:

- If the formatter cannot recognize the EOF pattern, the operation reports data error status.
- If the tape is write-protected, the operation aborts and reports write-protect and tape error status.

- If the operation must begin between the early warning (EW) hole and EOT on any track but the last one, it reports rewind and tape error status; the command can be retried after the rewind bit clears.

- If the tape crosses the EW hole on the last track, the operation continues but reports EOT and tape error status.

Record Skip Reverse (W6 = X3XX). The record skip reverse operation reverses the tape direction, skips the tape back the number of records specified in W4, and stops on the interrecord gap (IRG) that follows the last record skipped (moving toward BOT). After the last record skipped, the operation delays stopping the motor until a timer expires to give the write and erase heads time to follow the read head into the IRG. The formatter decrements the contents of W4 each time a record is skipped. If W4 is initially set to zero, the formatter attempts to skip 65 536 records and stops on BOT or EOF.

If the skip count goes to zero before the formatter encounters an EOF record or tape hole, the command completes without error and W4 is updated to show a count of zero. Otherwise, the record skip reverse operation reports the following errors:

- If the formatter determines that the record just skipped was an EOF record, it reports EOF and tape error status.

- If the load point (LP) hole on the first track is crossed, the command aborts; the formatter sets the BOT and tape error bits and moves the tape to BOT.

- If the tape is at BOT when the record skip reverse command is issued, the command is preempted and BOT and tape error are set.

- If the LP hole is detected on any track except the first track, the tape backs up to the end of the previous track for the command to continue without reporting the track switch to the host.

Read Forward (W6 = X4XX). To execute the read forward command, the formatter first finds the desired data by counting data bytes from the beginning of the record until the read offset count (W3) decrements to zero. The formatter then begins to read and to transfer the desired number of data bytes (W4) to the controller. After the transfer byte count decrements to zero, the formatter stops transferring data, but continues to count data bytes until the end of the record and stores the read overflow count in W1. The sum of the read offset count, transfer byte count, and read overflow count is equal to the total number of data bytes in the record Figure 3-13.

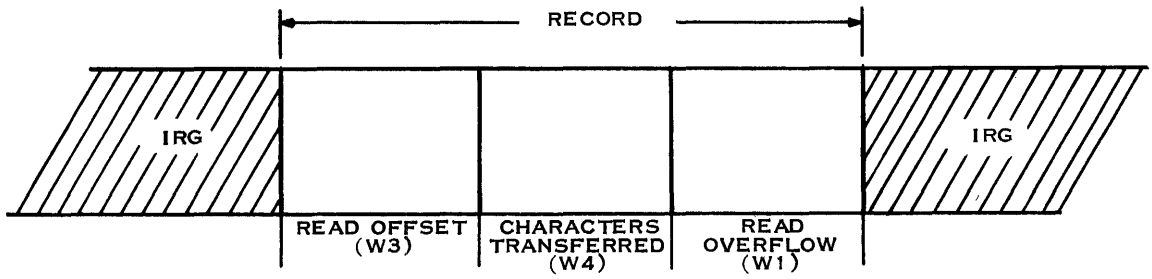


Figure 3-13. Read Offset and Overflow for Partial Record Read

The read operation reports the following errors:

- If the data transfer rate does not meet the demands of the read rate, the read operation reports a rate error (W7, bit 12).
- If the tape passes the EW hole on the last track, the operation reports EOT status and tape error; if the tape passes the EOT hole on the last track, the operation reports offline (W0, bit 0) and tape error status.
- If the transfer byte count is not decremented to zero when the end of the record is reached, the operation reports end-of-record status, or if an EOF mark is detected, EOF status. In both cases, it also reports tape error.
- If it detects a CRC error in data transferred to the host, the read operation reports data error. If it detects a CRC error in data not transferred (in offset or overflow data), it reports corrected data error.
- If the read operation crosses to the next track, the rewind and tape error bits are set. The command can be retried after the rewind bit clears.
- If header verification fails, the operation reports format error.
- If the data is not found on the tape within 10 seconds, the operation reports command time-out (W0, bit 7) and tape error.
- If a tape position error or unexpected interrupt occurs, the operation reports offline and tape error status.

Record Skip Forward (W6 = X5XX). The record skip forward command skips the tape forward the number of records specified in W4 and stops on the IRG that follows the last record skipped. The formatter decrements the contents of W4 each time a record is skipped. If W4 is initially set to zero, the controller attempts to skip 65 535 records and stops on EOT or EOF.

If the skip count goes to zero before the formatter encounters an EOF record or EOT, the command completes without error and W4 is updated to show a skip count of zero. Otherwise, the record skip forward operation reports the following errors:

- If the last record skipped was an EOF record, the skip count is decremented and the operation reports EOF and tape error status.
- If the skip forward crosses the EW hole on the last track, the command aborts and reports EOT and tape error.

Write Command (W6 = X6XX). The write command writes the number of data bytes specified in W4 in 256-byte segments fitted into data block formats 272 bytes long. Each data block consists of a preamble (four bytes), sync character (two bytes), header (six bytes), data (256 bytes), CRC (two bytes), and postamble (two bytes). The minimum number of bytes written in a record is two, to allow proper error checking. The maximum number of bytes in a record is limited by the size of W4 to 65 535 characters.

Recording on the tape begins anywhere after a point six inches inside the LP hole on the first track and ends inside the EOT hole on the last track. Records are written after the EW hole only if the record is less than 20 kilobytes long. An attempt to force-write starting after the EW hole on the first through third tracks results in an automatic erase to the EOT hole, a rewind to the BOT hole, and selection of the next logical track. (During the rewind, the rewind status bit is set when the rewind starts and is cleared when the rewind completes.) A force-write starting after the EW hole on the last track and continuing all the way to the EOT hole forces the tape to unload. To clear the offline status, the tape must be removed and reinserted.

Write operations execute at 762 millimeters (30 inches) per second, and tape rewind executes at 2286 millimeters (90 inches) per second.

The write operation includes read-after-write to check the integrity of the data just written (by means of CRC) as it passes the read head.

The write operation can report the following errors:

- If CRC fails in read-after-write, the RAW bit is set. This bit (with the format error bit) is also set if a media dropout is detected before the end of the record.
- If the data transfer rate fails to meet the demands of the write operation, the rate error bit is set.
- If the tape passes the EOT hole, if tape position faults are detected, or if unexpected interrupts occur, the operation reports offline status.

- If a write operation completes between the EW hole and the EOT on the last track, it reports EOT status.
- If the tape cartridge write-protect indicator is turned to SAFE, the command aborts and reports write-protect status and tape error.
- If the operation must cross tracks, it sets the rewind and tape error bits while the tape rewinds and the next logical track is selected. The command can be retried when the rewind bit clears.

Erase (W6 = X7XX). The erase operation removes flawed segments of data that cause errors in write commands. After the unsuccessful write and retry, a skip record reverse operation moves the tape to the beginning of the bad area, the write and erase heads for the track turn on, and the tape moves forward a distance based on the erase length in W4 to erase the data.

During an erase, tape positioning takes place just as it does during a write operation. Because of motor tolerances and creep requirements, the erase operation does not guarantee editing capability.

The erase operation reports the following errors:

- If the tape goes offline due to time-out or unexpected interrupts, the operation sets the offline and tape error bits.
- If the operation crosses the EW hole on the last track, the operation reports EOT and tape error.
- If the tape cartridge write-protect indicator is turned to SAFE, the operation sets the write-protect and tape error bits.
- If the operation crosses tracks, it sets the rewind and tape error bits during the track switch. After rewind clears, the command can complete.
- If unexpected data amplitude is detected in the erased area, the operation sets the format error bit.

Read Transport Status (W6 = X8XX, X9XX). The read transport status commands are identical to the NOP commands previously discussed.

Rewind (W6 = XAXX). The rewind command moves the tape to a point outside the BOT on the first track and stops it. After the operation initiates, it reports rewind status. When the tape has finished repositioning, the rewind bit clears and the operation reports BOT.

The rewind operation reports offline and tape errors if the tape is offline, or if time-out or unexpected interrupts occur.

Unload (W6 = XBXX). The unload command moves the tape to the unload point beyond the first EOT hole and stops it. After the operation initiates, it reports rewind status; the TAPE READY indicator begins to blink. When the tape finishes repositioning, the rewind bit clears, the operation reports offline, and the TAPE READY indicator turns off to indicate that it is now safe to remove the tape cartridge.

3.3.7.2 Special Commands. The tape system uses the special commands (unformatted write, unformatted read, and the maintenance commands) for diagnostic and troubleshooting purposes.

Unformatted Write (W6 = XCXX). The unformatted write command allows diagnostics to force a given error for test purposes. Like the write command, this command begins by writing the preamble and the sync character of a data block. However, the programmer must supply all format data (header, postamble, and so on) after the first preamble and sync bytes.

The unformatted write command reports the same errors as the write command, except for CRC errors. During an unformatted write, CRC checking is inhibited.

Unformatted Read (W6 = XDXX). The unformatted read command provides a tool for diagnostics to set up data buffers for unformatted writes to force particular errors in read-back. Like the read command, this command begins by reading the preamble and the sync character of a data block. After that, however, the command continues to read without regard to format until the transfer byte count decrements to zero.

The unformatted read command reports the same errors as the read command, except for CRC errors. During the operation, CRC checking is inhibited. The unformatted read also aborts with an EOR error if the transfer byte count requested exceeds the length of the record and thus crosses the end of the record before the count decrements to zero.

Maintenance Commands (W6 = XFXX). When the maintenance command bits are set, the self-test or diagnostic indicated in the left byte of W3 executes. Appendix A includes a list of the maintenance commands.

4

WD800 System Kit Installation

4.1 GENERAL

This section contains the kit-level installation procedures for the WD800 system kit. The kit installation procedures cover terminator configuration, cable installation, power-up, and online system verification. These procedures assume that three conditions have been met: first, that the TPBI and the WD800 chassis have been installed according to the procedures outlined in Sections 2 and 3; second, that the stand-alone self-tests have been passed and the unit select addresses have been set; and finally, that the units have not been cabled together yet.

4.2 INSTALLATION

The following paragraphs describe the kit-level installation procedures in detail.

4.2.1 General Overview

Kit-level installation consists of the following steps:

1. Recording the installation date on the configuration label located on the back of the chassis.
2. Confirming that the TPBI and WD800 chassis passed the stand-alone self-tests described in Sections 2 and 3.
3. Ensuring that the WD800 terminator packs are configured properly.
4. Ensuring the WD800 grounding configuration is correct.
5. Installing the PBI interconnecting cable.
6. Checking the installation of the ac power cord.
7. Performing power-up.
8. Running system tests.
9. Running system diagnostics (if desired).
10. Performing power-down.

CAUTION

After the WD800 is first installed, the disk must be allowed to run for 30 minutes to provide a power-on purge cycle before attempting online system use. This period is required for proper thermal stabilization and air filtering in the sealed area of the disk assembly. Failure to follow this procedure can result in damage to the disk.

The WD800 contains static-sensitive electronic components. To avoid damage to these components, ensure that you discharge any accumulated static before touching the unit. This can be done by touching a grounded object.

Before proceeding with kit-level installation, confirm that all stand-alone installation procedures (Sections 2 and 3) have been completed. Record the installation date on the configuration label locked on the back of the chassis.

4.2.2 Configuring the WD800 Terminator Packs and Grounds

If an existing system is being expanded by adding a chassis, a primary chassis may have to be converted to a secondary chassis (or vice versa). The conversion between primary and secondary configurations involves both the terminator packs and the grounds. Secondary units are required to have terminator packs removed and chassis and signal grounds open. Primary units normally have terminator packs installed and chassis ground shorted to signal ground. In some cases, primary units may require chassis and signal grounds open.

To determine whether the WD800 is a primary or secondary unit, look at the ID plate on the rear of the WD800. If the part number has an even dash number (-0002, and so on) then the unit is configured as a secondary unit. If the part number has an odd dash number, then the WD800 is a primary unit. On the WD800A, the ID/SN label at the back of the unit specifies W/O TM for secondary units. The exception to this rule is when the unit has been reconfigured in the field from a primary to a secondary unit, in which case the customer configuration label should so indicate.

4.2.2.1 Configuring the WD800 Terminator Packs. Use the following procedure to move the terminator packs:

1. Unplug the ac power cord.
2. Remove the top cover of the WD800 chassis as follows:
   a. Remove the four screws on the top back edge.
   b. Loosen the screws on the left and right sides of the chassis near the top edge.
   c. Remove the top by lifting it by the back edge so that the lip on the front edge moves out from under the front panel molding.

3. Remove the interface PCB as follows:

   a. Refer to Figure 4-1 to locate the interface PCB in the card cage in the WD800 chassis. (The PCB is green with a violet ejector tab, and has the word INTERFACE silkscreened on it. The interface PCB is in the same location in the WD800 and WD800A chassis.)

   b. Pull out the interface PCB internal ribbon cable from the outside edge of the card cage.

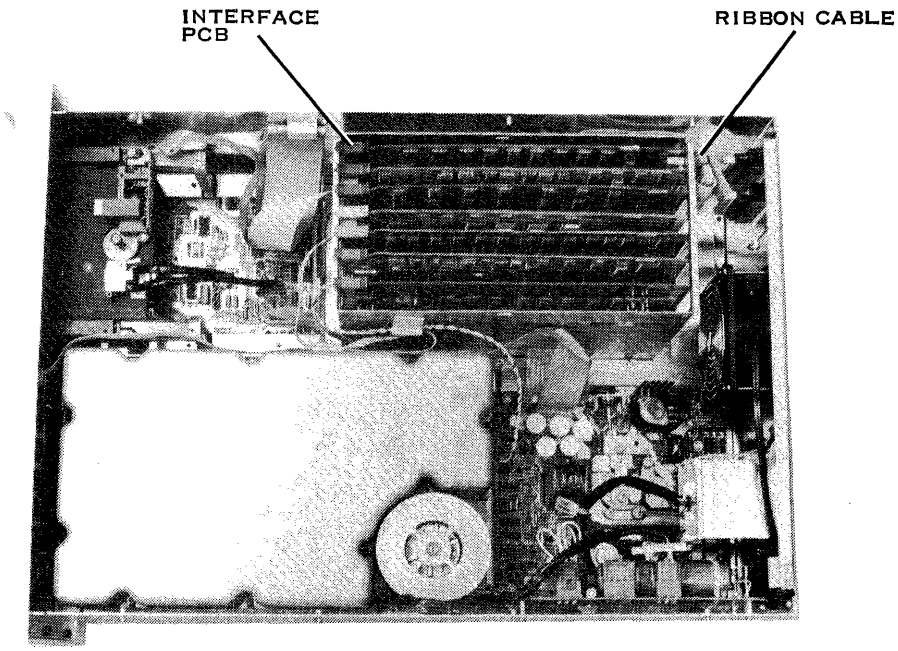
   c. Using the ejector tab, remove the interface PCB.

4. Locate the terminator pack positions on the PCB (Figure 4-2).

5. Move the terminator packs as required to either the storage position or the functioning position.

CAUTION

Orient the terminator packs as shown in Figure 4-2. (The dot on the pack indicates the location of pin 1.) Each terminator pack is a dual inline resistor pack. Improper orientation can destroy the packs or cause damage to other equipment.



2282691

Figure 4-1. Location of the Interface PCB

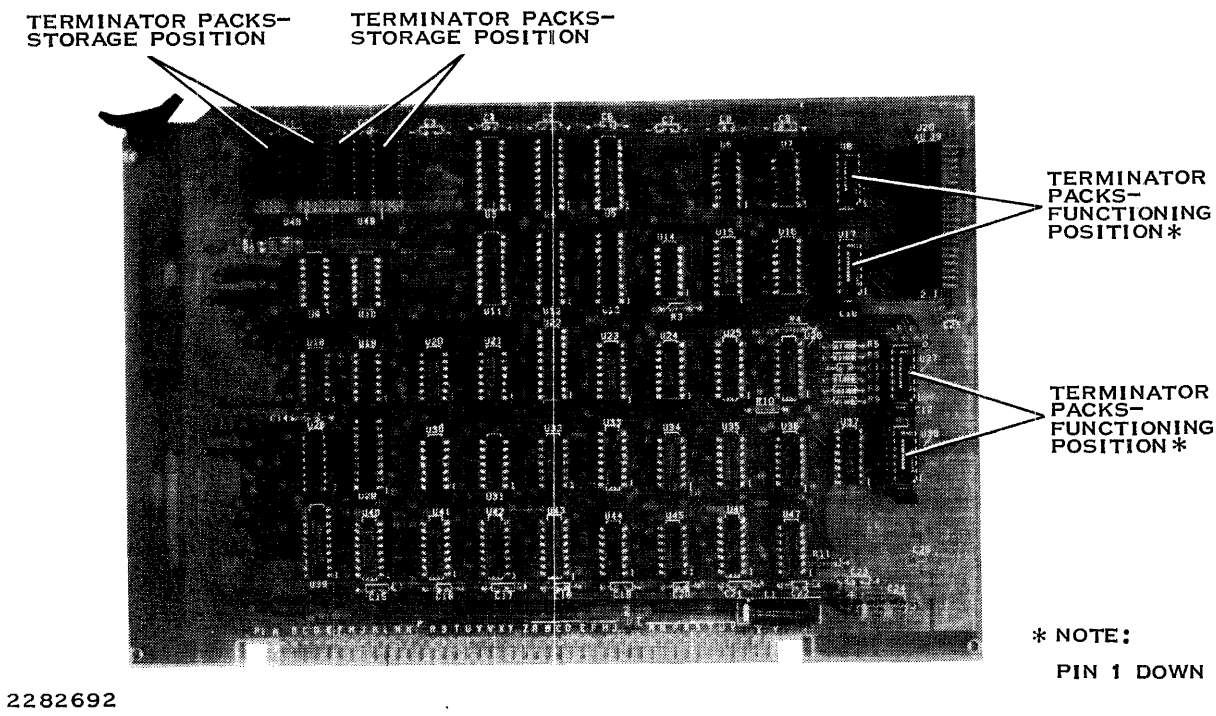


Figure 4-2. Location of Terminator Packs

6. After installing the packs, check carefully that they are seated properly.

   a. Make sure the packs are oriented properly.

   b. Make sure that none of the pins are bent under the packs.

7. Replace the interface PCB in the card cage by reversing the procedure in step 3. Be careful to orient the ribbon cable properly and ensure that it is fully inserted.

8. Proceed to the instructions for configuring the WD800 grounds.

4.2.2.2 Configuring the WD800 Grounds. WD800 grounds should be reconfigured under the following conditions:

- Whenever a primary chassis is added to an existing system, the grounds must be opened, or other equipment in the system must be modified to maintain a single-point system ground.

- Whenever a secondary chassis is reconfigured to a primary chassis, it provides the only chassis ground reference for the computer system in which it is being installed (as when an existing primary disk system is replaced by a WD800). This procedure assumes performance as a continuation of the procedure for moving terminator boards.

Use the following instructions to change the ground configuration:

1. Unplug the twisted-pair cable from the red color-coded PWB (WD800 only); unplug the 3 cables from the red color-coded PWB (WD800A).

2. Remove the three PWBs nearest the disk, color-coded orange, red, and brown (WD800 only); remove the red color-coded PWB (WD800A) and orange PWB.

3. If the motherboard includes a ground selection jumper plug (Figure 4-3), proceed to step 5.

4. This step pertains to WD800 drives only. If no ground selection jumper plug is provided on the motherboard, this unit cannot have its grounding configuration changed. In such cases, the WD800 has its chassis ground shorted to signal ground. In order to provide a single-point system ground with this WD800, the other equipment in the computer system must have their grounds isolated (open). Proceed to step 6.

5. Move the ground selection jumper plug on the motherboard (Figure 4-3) between jumpers E1 and E2 for shorted ground (primary configuration), or between E2 and E3 for open ground (secondary or add-on configuration).

6. Install all PWBs back in the card cage, and ensure that the PWB color codes match the card cage color codes.

7. Reconnect the twisted-pair cable to the red color-coded PWB (WD800 only) or the 3 cables to the red PWB (WD800A).

8. After you have completed all modifications, replace the top after you install and tighten the screws that secure it.

9. WD800 only; mark the customer configuration label (on the rear of the unit) so that it precisely shows the current system configuration. The customer configuration label provides for both terminator and grounding changes. If this modification negated a previous modification, delete the appropriate marks on the customer configuration label.

4.2.3 Installing the PBI Cable

The PBI cable is a radial cable that has symmetrical, 40-pin cable connectors on the ends. The two connectors fit into either the TPBI or the WD800 chassis plug interchangeably. Install the connector on one end of the cable on the TPBI and install the connector on the other end of the cable in one of the two I/O port connectors at the rear of the WD800 chassis. In configurations with more than one chassis, install one end of the second cable in the other I/O port, and install the other end of the second cable in one of the I/O ports on the back of the second chassis.

In constructing this daisy chain, you can install the cable connector in either I/O port on the chassis. The last chassis in the chain (designated the primary chassis) has the terminator packs in the functioning position and may have a tape drive for backup.

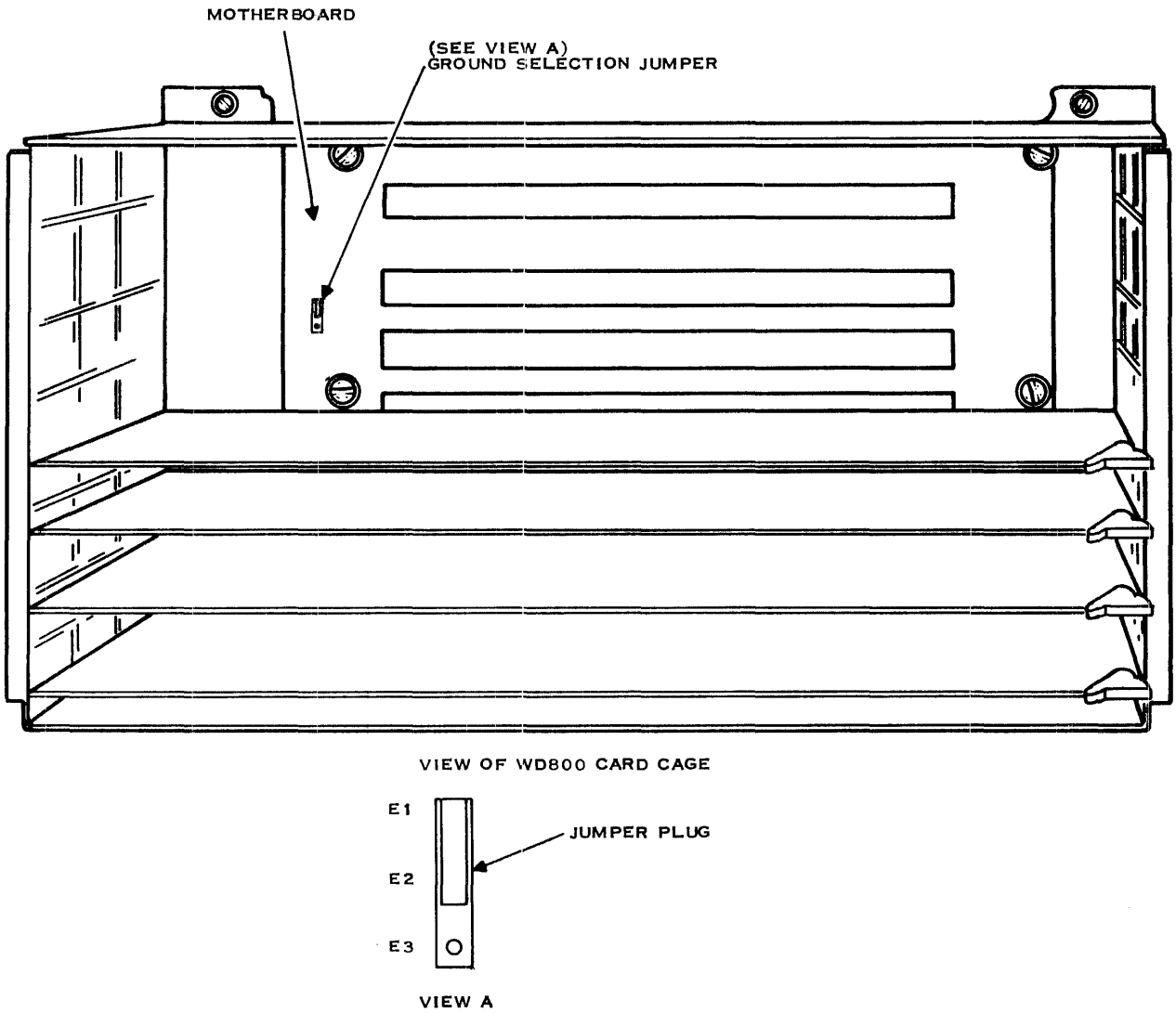


Figure 4-3. WD800 Chassis Ground Selection Jumper Plug

While referring to Figure 4-4, use the following procedure to install the cable.

1. Make sure all power is off.

2. Ensure that one end of the cable is attached to the TPBI connector P3 (refer to Section 2).

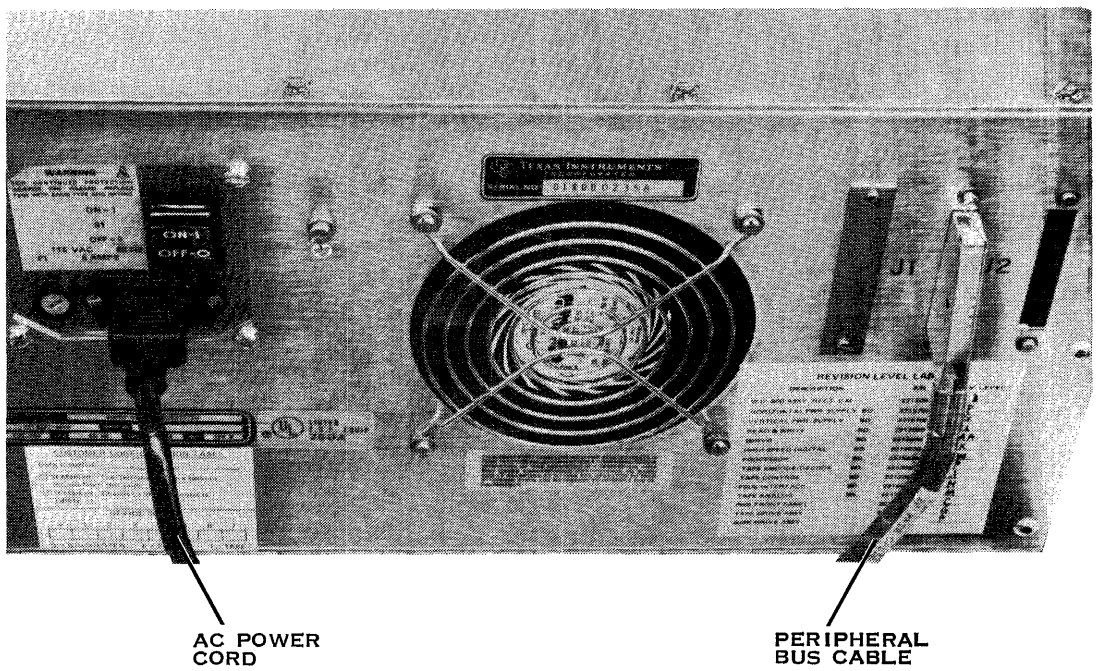


Figure 4-4. WD800 System Cabling

NOTE

The use of a cable carrier to control the arrangement of cables in the rack is strongly recommended.

3. Dress the cable toward the back of the rack and onto the cable carrier, allowing some slack. Attach the cable to the cable carrier using cable ties. Leave the ties somewhat loose for the moment. Do not cut off the cable tie ends; tuck them back under the tie to keep them from interfering with cable carrier operation.

4. To guide the cable around the hinge of the cable carrier, place a cable tie in the bottom hole of the carrier nearest the hinge on the first side of the carrier. Place a second cable tie in the top hole nearest the hinge on the second (back) side of the carrier. Attach the cable smoothly (without loops or twists) using these two cable ties.

CAUTION

The cable can tolerate a minimum bend radius of 33 millimeters (1.3 inches) to avoid being damaged by stress. The cable must not be too tight across the cable carrier hinge and must be dressed from carrier bottom edge to top edge as described in step 4.

5. Dress the cable across the back side of the cable carrier and tie it down loosely with cable ties.

6. Route the cable along the outside side of the left rail of the rack to the back of the WD800 chassis, and gather the excess length in a service loop. Ensure that the free end of the cable leaves the top of the service loop, and anchor the loop with a cable tie.

7. Fasten the cable in the two cable harness clamps provided. Do not fasten the cable clamp ties tightly at this point.

8. Plug the cable connector into the mating connector on the right of the chassis back panel (as seen from rear). Adjust the cable so that enough slack is left to permit sliding the chassis all the way forward on the rails.

9. After adjusting the cable in the ties to ensure that enough slack is left to allow the WD800 chassis to slide forward to the full extent, tighten all the cable ties.

10. Use cable ties along the rail of the rack to ensure that the cables in the rack do not become tangled.

4.2.4 Installing the Power Cord

To install the ac power cord, perform the following steps:

1. Make sure that the ac power switch is turned off.

2. Confirm that the female end of the ac power cord is connected to the ac cord receptacle located on the rear of the WD800 chassis (see the description of rackmounting, Section 3).

3. Confirm that the ac power cord is routed down through the cable harness clamp below the switch plate cutout located on the back of the WD800 chassis, and that the cable tie is fastened.

4. Dress the cord out to the left vertical rack rail and tie it down (below the level of the chassis) on the inside of the rail.

CAUTION

If the ac power cord is not routed as indicated, it can get caught between the ball stud and ball stud receptacle. The resulting stress can damage the cord and possibly the system.

5. Plug the other end of the cord into an available ac outlet on the rail.

4.2.5 Power-Up and System Test

The following paragraphs describe the power-up procedure and discuss system start-up and tests. The information presented here is only a summary. The Preface to this manual lists publications that contain detailed information; references to these manuals occur throughout the procedures in this section. Installation personnel should become familiar with the detailed discussions in the manuals referred to in the following steps.

4.2.5.1 Power-Up. To power up the system, first turn the ac power switch on.

Refer to the Preface to identify the 990 computer system manual that covers the system being used as host for the WD800 system (for example, the *990/10 Hardware Reference Manual*). Use the procedure described in that manual, including the self-tests if any are required, to bring the 990 computer online. In case of malfunction, refer to the *Unit Diagnostics Handbook*, *Volume 1 — General 990 Unit Diagnostic Information* for failure treatment.

4.2.5.2 System Start-Up. After the system is cabled together and powered up, the WD800 system automatically repeats the self-tests it performed when powered up as a stand-alone assembly, and adds self-tests of the host system interface. Operator intervention during start-up consists of only two operations:

- Turning on power
- Checking operational status indicators

The power is turned on as part of the 990 computer start-up. The front panel status indicators respond to power-up in the following way:

1. All four indicators turn on for about 5 seconds on the WD800.
2. All four indicators except TEST MODE turn off and then blink in sequence as the self-tests execute.
3. The DISK READY indicator turns on.
4. The TAPE READY indicator blinks, then turns off.
5. The SYSTEM READY indicator blinks, then turns on, indicating that communication is established with the host system; simultaneously, the TEST MODE indicator turns off.

NOTE

After the WD800 chassis completes power-up initialization, the computer system is ready to boot software or diagnostics. At this point, the operator must decide whether the loading device for the software or diagnostics will be tape or disk. If software is to be booted from disk, do *not* install a tape at this time, because some 990 loader ROMs automatically boot from an online tape, if one is present. Consult the applicable manual listed in the Preface for a detailed discussion of loading procedures.

If a tape cartridge is installed and the tape subsystem passed the self-test, the tape subsystem runs a media test and loads the tape cartridge to prepare it for use. During this procedure, the TAPE READY indicator blinks.

When the load operation (including media test) is complete on the tape cartridge, the TAPE READY indicator turns on. If the load operation fails, the TAPE READY indicator turns off.

If no malfunctions of the 990 computer or WD800 subsystem are reported, the 990 is online and the previously described subsystem self-tests ran successfully. If the self-tests fail, see Appendix A for fault analysis procedures.

4.2.5.3 System Diagnostics. The following paragraphs discuss the use of the diagnostic operational control system (DOCS) for system testing, and the procedure for system checkout in two cases: when the WD800 disk system is the system disk, and when it is not the system disk.

DOCS Tests. For information about more extensive testing of the system using DOCS, consult the general unit diagnostic information in *Unit Diagnostics Handbook, Volume 1* and the diagnostics for mass storage devices in *Volume 3* (see the Preface for part numbers). The following are the applicable tests:

- DSKCOM — A high level test common to several TI disk systems
- DSKSA — Surface analysis test
- DSKWD8 — Winchester disk tests
- TPBITS — TPBI tests
- MTCTST1 and MTCTST2 — Magnetic tape cartridge tests

The volume on *Diagnostics for 990 Mass Storage Devices* describes these tests fully. Be sure to consult the most recent revision level of these manuals.

WD800 Disk System Checkout — System Disk. If the WD800 disk is the system disk, the operating system must be installed before the system can be used. The procedure for installing the DX10 operating system is detailed in the *WD800/WD800A Field Maintenance Manual* (see Preface). The following discussion is only a summary; consult the *DX10 Operating System Manual* or *DNOS SCI Reference Manual* for a step-by-step procedure.

The operating system for a WD800 system disk is normally installed by means of a tape cartridge set. After the operating system is copied to the disk and verified, the system can be booted from the disk.

If errors occur during the process, enter an Initialize Disk Surface (IDS) command from the user terminal. The IDS command does an analysis of the disk surface, checks for flaws in the media, and marks any bad tracks. Any bad-track information on the disk when the surface is initialized is included in the bad track list put on the disk.

CAUTION

The IDS command destroys any data previously recorded on the disk.

When you enter the IDS command, the following prompts appear:

```
INITIALIZE DISK SURFACE
                    UNIT NAME:
  CONTINUE SUSPENDED IDS?:
     INITIALIZE NEW VOLUME:
       LISTING ACCESS NAME:
       EXECUTION MODE (F,B):
```

For UNIT NAME, enter the device name (DS01 or DS02) of the WD800 (see Section 3 to confirm the unit name).

If you enter NO in response to CONTINUE SUSPENDED IDS?, the following prompts appear:

```
INITIALIZE DISK SURFACE
        LENGTH OF ANALYSIS (S,M,L):
          MARK MARGINAL TRACKS:
          BAD TRACK ACCESS NAME:
 HARDWARE INTERLEAVING FACTOR:
```

If you enter YES in response to INITIALIZE NEW VOLUME? in the first set of prompts, the following prompts appear (regardless of your response to the CONTINUE SUSPENDED IDS? prompt):

```
INITIALIZE NEW VOLUME
                VOLUME NAME:
 NUMBER OF VCATALOG ENTRIES:
DEFAULT PHYSICAL RECORD SIZE:
          USED AS SYSTEM DISK?
```

Following the IDS command, repeat the operating system installation procedure. If errors still occur, consult Appendix A for fault analysis. For greater detail, consult the *DX10 Operating System Manual* or *DNOS SCI Reference Manual* and the other applicable manuals listed in the Preface.

WD800 Disk System Checkout — Not System Disk. If the WD800 subsystem disk is not the system disk, use the normal TI DNOS or DX10 operating system software to exercise the disk system. To do so, follow these steps:

1. At the user terminal, select command mode and enter the Install Volume IV command. The following prompts appear:

   ```
   INSTALL VOLUME
               UNIT NAME:
        VOLUME NAME:
   ```

   The unit name (DS01 or DS02) is the one assigned to the particulat drive when the DX10 system was generated.

CAUTION

Selection of an incorrect unit name adversely affects another unit of the same name. Check the system generation (sysgen) documents or ask the systems analyst to determine the correct unit name.

Enter the correct unit name. You determine the volume name, which can be one to eight characters in length, beginning with an alphabetic character. Choose a volume name and press the RETURN key to enter the responses.

2. Create a file directory by selecting command mode and entering the Create File Directory command (CFDIR). The following prompts appear:

```
CREATE DIRECTORY FILE
                          PATHNAME:
                       MAX ENTRIES:
    DEFAULT PHYSICAL RECORD SIZE:
```

The pathname consists of the volume name, a period (.), and a user-selected directory name. Use the same volume name assigned in step 1 and create a directory name. Press the RETURN key to enter the responses.

3. Create a sequential file by entering the Create Sequential File (CFSEQ) command in command mode. The following prompts appear:

```
CREATE SEQUENTIAL FILE
                          PATHNAME:
          LOGICAL RECORD LENGTH:
       PHYSICAL RECORD LENGTH:
             INITIAL ALLOCATION:
         SECONDARY ALLOCATION:
                     EXPANDABLE?:
                BLANK SUPPRESS?:
                    FORCED WRITE?:
```

The pathname is mandatory, and is of the form Volume Name.Directory Name.File Name. Use the volume name and directory name previously designated and create a file name. For the remaining prompts, accept the default values by pressing the RETURN key until all responses are entered.

4. Enter the text edit mode and record some data in the file as follows. Select command mode and enter the Initiate Text Editor (XE) command. The following prompt appears:

```
INITIATE TEXT EDITOR
                  FILE ACCESS NAME:
```

The file access name is the pathname used in step 5. The system response is *EOF, indicating that an end-of-file (EOF) character is the only element in the file. Press the F7 key and then the blank grey key to enter compose mode. In this mode, each pressing of the RETURN key will enter a blank line in the file. Press the RETURN key and enter a line or lines of text. The following is a sample display:

```
THIS IS A TEST OF THE
WD800 DISK SUBSYSTEM.
*EOF
```

5. Leave the text edit mode by pressing the CMD key, entering the Quit Edit (QE) command, and pressing RETURN. The first display is as follows:

```
QUIT EDIT
                ABORT?:  NO
```

Press the return key to take the default value (NO) on the ABORT? line. The next display is as follows:

```
    QUIT EDIT
OUTPUT FILE ACCESS NAME:  [Volume Name.Directory Name.File Name]
                REPLACE?:  NO
  MOD LIST ACCESS NAME:
```

The output file access name is the same as the input pathname to allow recording of the editing session results on the file. Override the default NO on the REPLACE? entry by entering Y or YES. Return through the MOD LIST ACCESS NAME. The DX10 menu reappears. At this point, the data entered during the editing session is physically recorded on the disk rather than being held in 990 main memory.

6. Check the data on the disk by entering a Show File (SF) command. The same pathname used previously appears as the default access name because that was the most recent file used. If it does not appear, enter it as the file access name. The file contents are displayed on the screen.

These operations give the selected disk drive a good workout. Although they do not replace the standard diagnostic tests, they provide a high level of confidence in the operability of the system.

If errors occur during this exercise, execute an IDS command. The IDS command does an analysis of the disk surface in which it checks for flaws in the media and marks any bad tracks found. Any bad-track information that is on the disk when the surface is initialized is included in the bad track list put on the disk.

CAUTION

The IDS command destroys any data previously recorded on the disk.

Following the IDS command, repeat the disk system checkout. If errors still occur, consult Appendix A for fault analysis. For greater detail, consult the *DX10 Operating System Manual, Volume II* or *DNOS SCI Manual*.

4.2.6 Power-Down

No special precautions are required for WD800 power-down procedures. Although the WD800 system can be turned off independently of the 990 computer system by using the ac power switch on the rear of the WD800 chassis, it is not necessary to do so. The ac power switch can be left on all the time. The 990 computer and the TPBI handle required preparation of the interface TPBI to the WD800 system, so that the TPBI is not active during system start-up or shutdown (when the lines are not stable).

5

Operation

5.1 GENERAL

This section explains the WD800 system operating procedures. The following paragraphs describe the WD800 system controls and indicators, and discuss the operating procedures and operator preventive maintenance.

5.2 CONTROLS AND INDICATORS

The WD800 system controls and indicators described in the following paragraphs provide you with a simple means of monitoring and controlling the system. All of the controls and indicators are located on the front panel (Figure 5-1) except the ac power switch.

5.2.1 Controls

The storage system has three controls for operator use: an ac power switch, a TEST STATUS/TAPE UNLOAD switch, and a DISK WRITE-PROTECT switch.

CAUTION

The WD800 contains static-sensitive electronic components. To avoid damage to these components, ensure that you discharge any accumulated static before touching the unit. This can be done by touching a grounded object.

5.2.1.1 Ac Power Switch. The ac power switch is located on the rear panel (Figure 5-2). When the switch is turned on during normal equipment installation, the system attempts to initialize.

5.2.1.2 TEST STATUS/TAPE UNLOAD Switch. The TEST STATUS/TAPE UNLOAD switch, located on the front panel near the tape cartridge cutout (Figure 5-1), is a three-position, spring-loaded, momentary-action switch. After being moved up or down and released, it automatically returns to the center position.

The center position of the switch is idle. When the TEST STATUS/TAPE UNLOAD switch is moved down, the system goes into the tape unload mode. When the switch is moved up, the system goes into the test status mode.

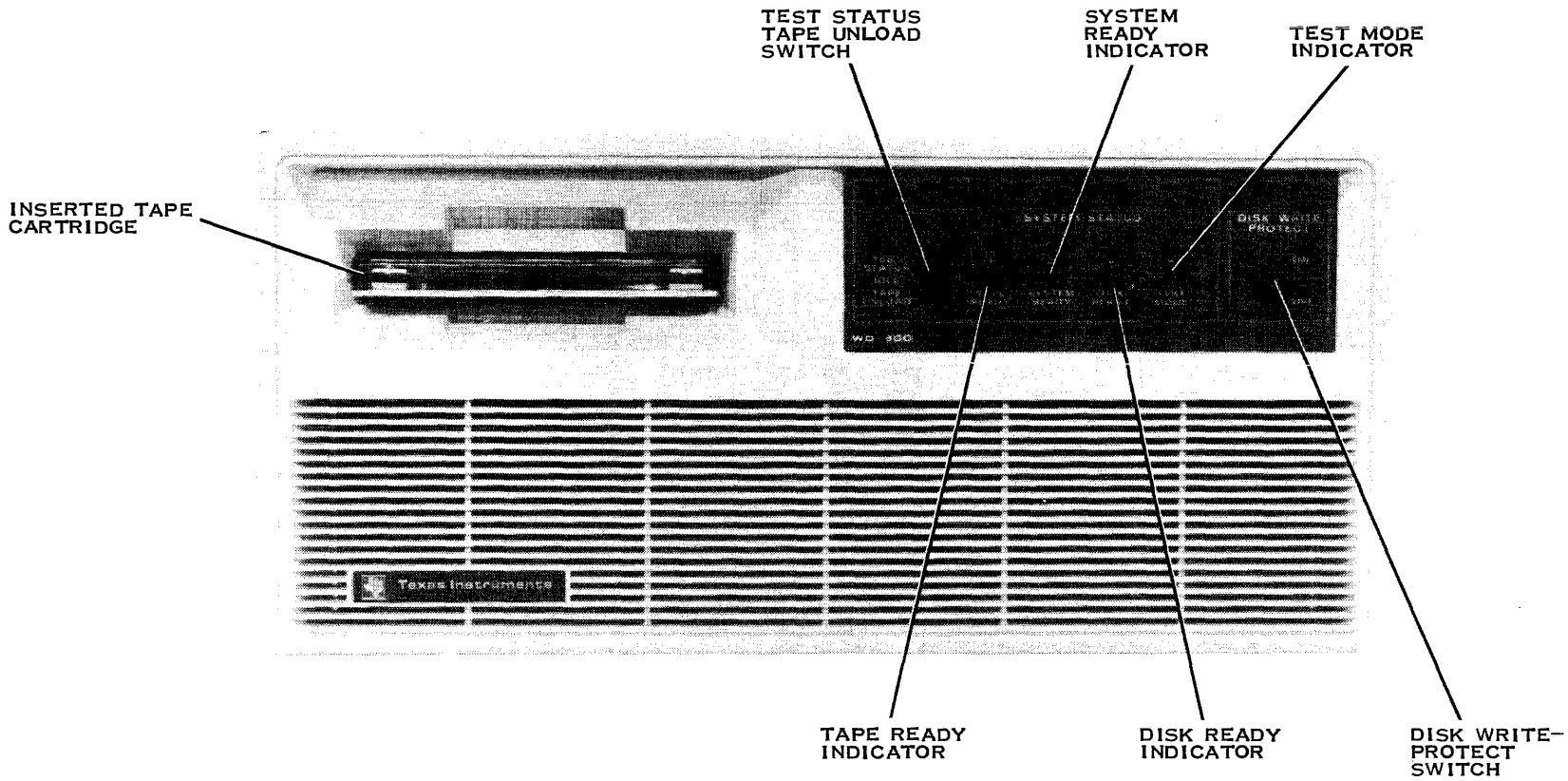


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Figure 5-1. WD800 System Front Panel

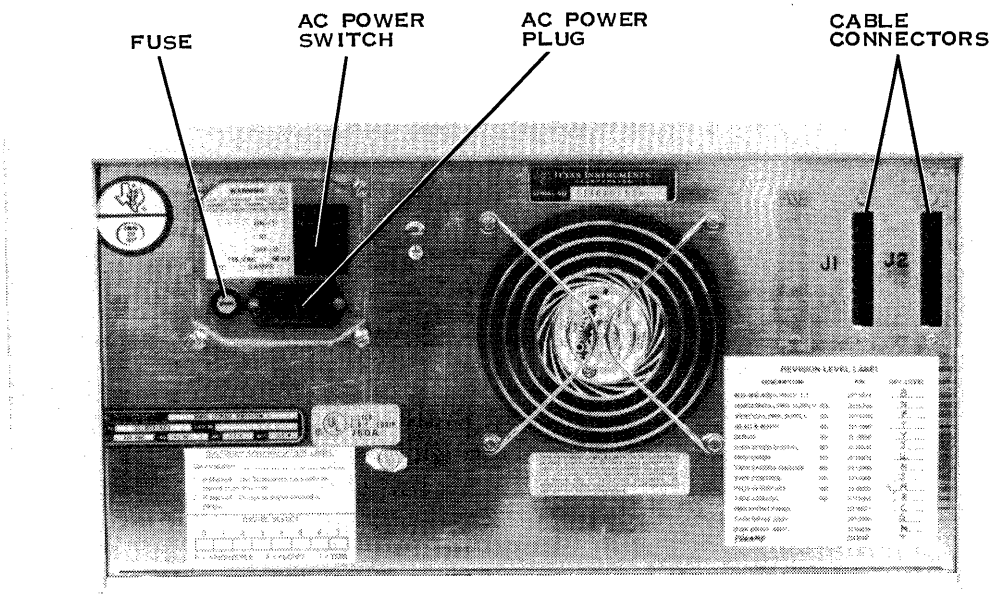

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Figure 5-2. WD800 System Rear Panel (Labels May Vary)

The tape unload mode is used to unload the tape cartridge and to choose a unit select address for the storage system. Toggling the switch down causes the storage system to advance an installed tape within its cartridge to the unload point. While tape activity is in progress (reads, writes, and other operations driven by the host system), the TAPE UNLOAD switch position is temporarily ignored by the storage system. If no tape is installed, the storage system also ignores the switch. (Paragraph 3.2.5 discusses the use of this switch to choose the unit select address.)

The test status mode position is used to display the self-test fault status code on the front panel indicators, and to set the unit select address. When the switch is toggled up, the four status indicators (paragraph 5.2.2) temporarily display a four-bit diagnostic code (corresponding to >0 through > F) that is used to indicate a possible subassembly fault. Appendix A includes a list of these codes for reference purposes.

When all four indicators are on (> F), the display is interpreted as a no-error code. Thus, to display all the storage system faults, toggle the switch to the TEST STATUS position until the no-error indication appears. Toggling the TEST STATUS switch once beyond the no-error indication returns the indicators to their primary function of showing the operational status of the system. (Paragraph 3.2.5 discusses the use of this switch to set the unit select address.)

5.2.1.3 DISK WRITE-PROTECT Switch. The DISK WRITE-PROTECT switch is located on the front panel and is a two-position switch; when it is up (on), the disk is write-protected.

NOTE

The DISK WRITE-PROTECT switch applies only to the disk. To write-protect a tape cartridge, turn the plug on the cartridge to the SAFE position.

5.2.2 Indicators

Four lights are located on the front panel of the storage system: a tape status indicator (TAPE READY), a storage system indicator (SYSTEM READY), a disk status indicator (DISK READY), and a test mode indicator (TEST MODE). These lights perform three main functions. Their primary function is to show the operational status of the storage system. The lights also display detected subassembly faults and the unit select address. The primary function is active when neither of the other two functions is active.

When the TEST STATUS/TAPE UNLOAD switch is toggled up, the indicators display detected subassembly fault codes (paragraph 5.2.2.5). When the TEST STATUS/TAPE UNLOAD switch is toggled down during certain power-up conditions, the indicators display the unit select address code (paragraph 3.2.5). Otherwise, they show system operational status. The following paragraphs describe the action of the indicators in their primary function, and then in their other functions.

5.2.2.1 Tape Status Indicator (TAPE READY). The tape status indicator shows the status of the tape subsystem as determined by the formatter. The three possible states of the indicator are as follows:

- On — Indicates that the tape subsystem powered up, initialized, and has a tape cartridge installed and ready for operation.
- Blinking — Indicates that the tape subsystem self-tests are being performed or that the formatter is loading or unloading the installed tape cartridge. This process takes a maximum of two minutes, but requires only one minute if the tape is stored in the unload position (EOT). If this indicator does not blink (remains off) when a tape cartridge is inserted, then the tape subsystem failed a self-test during power-up and initialization.
- Off — Indicates that the tape subsystem successfully performed power-up and initialization; and that a tape cartridge is either not installed or is installed and is offline (failed the load test or advanced to the unload position for removal). The tape cartridge is set to the unload point by a command from the host system or by the TEST STATUS/TAPE UNLOAD switch begin toggled down.

The other possible causes for the indicator to remain off include, but are not limited to the following: no power, formatter failure or fault, missing or blown fuse, tape cartridge self-test failure (which automatically takes the tape offline), or optional tape system not installed.

The tape status indicator also blinks upon selection of the TAPE UNLOAD switch if a cartridge is installed. If tape activity is detected within 10 seconds of TAPE UNLOAD switch selection, this indicator will cease to blink and return to the on state (indicating that the unload operation cannot be completed at this time).

5.2.2.2 System Status Indicator (SYSTEM READY). This status indicator shows the status of the formatter and interface as determined by the formatter subsystem. The three possible states of the indicator are as follows:

- On — Indicates that the storage system powered up, successfully initialized, and reported proper initialization status to the controller.
- Blinking — Indicates that the storage system is powered up and is performing initialization; has detected a formatter fault; has not been selected by the controller to report initialization status; or has detected an interface bus test fault.
- Off — Indicates that the storage system is not operational. Possible causes include, but are not limited to the following: no power, formatter failure, or missing or blown fuse.

5.2.2.3 Disk Status Indicator (DISK READY). The disk status indicator shows the status of the disk subsystem as determined by the formatter subsystem. The three possible states of the indicator are as follows:

- On — Indicates that power is on and the disk subsystem is successfully initialized.
- Blinking — Indicates that power is on and the disk self-test is in progress, or that disk activity is occurring (irregular blink).
- Off — Indicates that the disk subsystem is not operational. Possible causes include, but are not limited to the following: initialization in progress, disk self-test fault, no power, formatter failure or fault, or missing or blown fuse.

5.2.2.4 Test Status Indicator (TEST MODE). The test status indicator shows when the formatter is performing self-tests. The two possible states of the indicator are as follows:

- On — Indicates that power is on and the formatter subsystem is performing its self-test. If the formatter fails, the test status indicator does not progress to the next stage (turning off). This indicator may also turn on momentarily as a result of a reset from the host system, which initiates certain self-tests in the WD800.

NOTE

If the PBI cable is disconnected or the host is powered down, this indicator remains on after self-tests are complete for approximately 30 seconds, during which time unit selection can be examined or modified for this chassis (see Section 3).

- Off — Indicates the formatter completed the formatter self-test and is not currently performing other self-tests.

5.2.2.5 Indicator Secondary Functions. In the test status mode (TEST STATUS/TAPE UNLOAD switch toggled up), the indicators display diagnostic error codes (one error code per toggle of the switch). These codes are displayed in sequence as applicable after the TEST STATUS/TAPE UNLOAD switch is toggled to the TEST STATUS position (toggled up). (Refer to Appendix A for a detailed definition of the error codes.)

NOTE

The indicators continue to display the error code until the switch is toggled again. The test status mode is exited by toggling past error code >F (all indicator lights on), or by waiting until an internal timer automatically returns indicators to the operational status mode.

During unit selection, the indicators display the applicable unit select address when the TEST STATUS/TAPE UNLOAD switch is toggled down. The unit select addresses are position-coded; see paragraph 3.2.5.2 for details.

5.3 OPERATING PROCEDURES

The WD800 storage system requires minimal operator intervention during operation.

5.3.1 Disk Subsystem Operation

The disk subsystem requires no operator interaction. The DISK READY indicator on the front panel shows the status of the disk subsystem. When the indicator is on, the disk subsystem is initialized and is ready for operation.

NOTE

The DISK READY indicator blinks irregularly when disk activity is in progress. (This indicator turns off momentarily for each command processed to the disk.)

5.3.2 Tape Subsystem Operation

The discussion of the tape subsystem operation covers cartridge media requirements, cartridge handling, tape write-protection, cartridge insertion, cartridge unloading and removal, environmental requirements for the tape cartridge, and the power-down procedure.

5.3.2.1 Media Requirements. The tape subsystem uses a 137.16-meter (450-foot) four-track recordable tape cartridge. Use of media that does not meet TI specifications can reduce performance significantly. Service calls resulting from the use of media that is not TI-approved are billed to the customer, regardless of any service contracts in force. The TI part number for the tape cartridge is listed in Table 1-4.

CAUTION

Media that is not certified by TI can cause serious operational problems. Tests to determine media suitability are provided in the DOCS diagnostics (MTCTST1 and MTCTST2). Cartridge tape media is not error free. Up to 30 errors per tape-use can be tolerated (error code 49 in the DX10 log).

5.3.2.2 Cartridge Handling. The tape cartridge is designed to eliminate handling of the media. The supply and take-up reels are enclosed in a rugged cartridge. One access opening in the cartridge allows the drive motor capstan to contact the tape belt-drive capstan mounted inside the cartridge. A pivot action door is also provided on the cartridge for the transport heads to access the media. The transport automatically opens this door when the cartridge is inserted.

To avoid damage, handle the tape cartridge with the same care required for other magnetic media.

Use the following precautions:

- Keep the cartridge away from magnetic fields or magnetic materials. Magnetic fields distort the tape's recorded data.
- Avoid X-ray machines. The X-rays themselves do not harm the tape, but most X-ray machines generate powerful magnetic fields.
- Do not expose the cartridge to heat, direct sunlight, or moisture.
- Keep the cartridge away from sticky, oily, or abrasive substances.

5.3.2.3 Tape Write-Protection. A slotted plug on the upper left corner of the cartridge can be turned in either of two directions for write-protected or unprotected operation (Figure 5-3). The write-protected position is marked SAFE on the cartridge housing.

5.3.2.4 Cartridge Insertion. To insert the cartridge, orient it rightside up (clear plastic up, metal base down) (Figure 5-4). Then guide it into the slot in the front panel until it latches in place.

The front panel TAPE READY indicator shows the state of the transport. When the TAPE READY indicator is off, you can safely insert or remove a cartridge. Once a cartridge is inserted, it goes through an initial tensioning and positioning, followed by a media test operation. During the load operation, the TAPE READY indicator blinks. When the tape is tensioned and positioned for use, the TAPE READY indicator goes on.

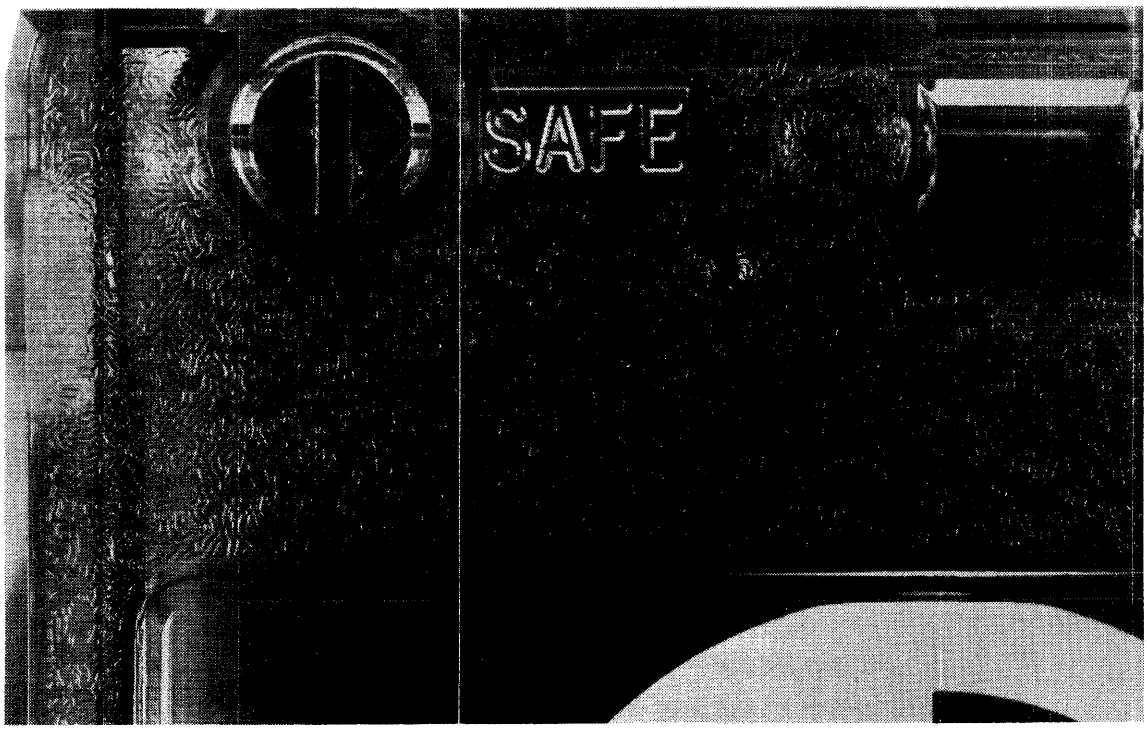

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Figure 5-3. Tape Write-Protection Plug

NOTE

If the load operation fails, the TAPE READY indicator turns off. If previously recorded data must be retrieved from a tape that fails the load operation, write-protect the tape and reinsert it. The tape media test is bypassed for write-protected tapes to allow whatever data recovery is possible.

The TAPE READY indicator remains on while the tape is in use until an unload sequence is initiated by the host system or by the operator.

5.3.2.5 Cartridge Unloading and Removal. When an unload operation is initiated either by command or by the unload switch, the tape inside the cartridge is moved to EOT to protect the data from contamination or other physical damage during tape removal and storage. During the unload operation, the TAPE READY indicator blinks. When the unload sequence is complete, the TAPE READY indicator turns off to indicate that it is safe to remove the cartridge and to insert another.

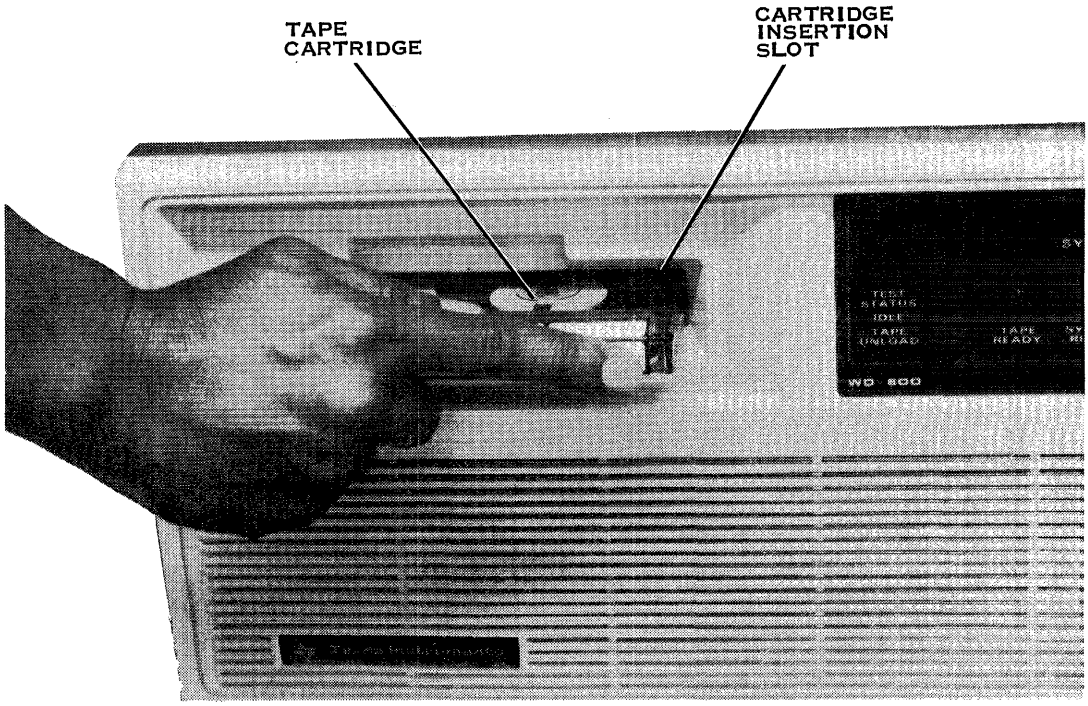

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Figure 5-4. Cartridge Insertion

Once a cartridge completes an unload sequence, it remains not ready even though physically installed in the transport. Its status is changed to ready only by removing the cartridge and reinserting it, which starts another tape load operation. The TEST STATUS/TAPE UNLOAD switch on the front panel can be used instead of an unload command from the host to unload a tape.

The TEST STATUS/TAPE UNLOAD switch is ignored if it is toggled while tape activity is in progress (reads, writes, and other operations driven by the host system).

NOTE

There is a 10-second delay between the toggling of the TAPE UNLOAD switch and the point at which an unload actually begins. This allows time to ensure that the host is not initiating tape activity.

CAUTION

To minimize the accumulation of dust on tape heads and sensors, leave a tape cartridge in the access slot at all times. Do not push this tape cartridge in so far that it latches. Leaving the cartridge latched can cause flat places on the capstan roller in the drive, because the capstan applies pressure to the tape.

Some models of the WD800 subsystem have a door over the access slot (Figure 5-8). This caution does not apply to those models.

5.3.2.6 Environmental Requirements for the Tape Cartridge. The tape is housed in a rugged cartridge for maximum reliability. Like all other magnetic media, however, tape is sensitive to its environment. Extreme temperatures, humidity, and strong magnetic fields can cause temporary or permanent loss of data. Contamination by dust or other particles can ruin the tape. Therefore, a clean, well-controlled environment where tape cartridges are stored and used is imperative.

Table 1-2 lists the specific environmental requirements for the WD800 system. The requirements represent worst-case conditions as determined by the most sensitive component in the storage system, so that an environment that meets the conditions can be assumed to be safe for tape cartridge use or storage.

5.3.2.7 Power-Down Procedure. Remove the tape cartridge from the WD800 before powering down the system.

5.4 OPERATOR PREVENTIVE MAINTENANCE

Preventive maintenance (PM) consists of cleaning the tape heads, the capstan, and the air filters.

Customer neglect of PM can lead to problems that only a service call can solve. If the TI customer representative (CR) corrects the problem by performing PM or corrective maintenance necessitated by neglect of PM, the customer is billed for that call regardless of any maintenance contracts in force.

5.4.1 Tape Transport Head, Capstan, and Sensor Cleaning

Clean the tape head, tape cleaner, and tape capstan with a cotton swab dampened with denatured alcohol at least once a week or more often if necessary. Use compressed dry air (available at photographic supply stores) to blow dust out of the sensor area underneath the tape lamp, which is located to the left of the capstan.

To gain access to the heads, capstan, tape cleaner, and sensors, remove the tape cartridge from the cartridge insertion slot. This permits access through the cartridge slot to the tape head, tape cleaner, and capstan assemblies (Figure 5-5). Insert the cotton swab through the slot and apply to each assembly. Use the compressed dry air to clean the sensor area.

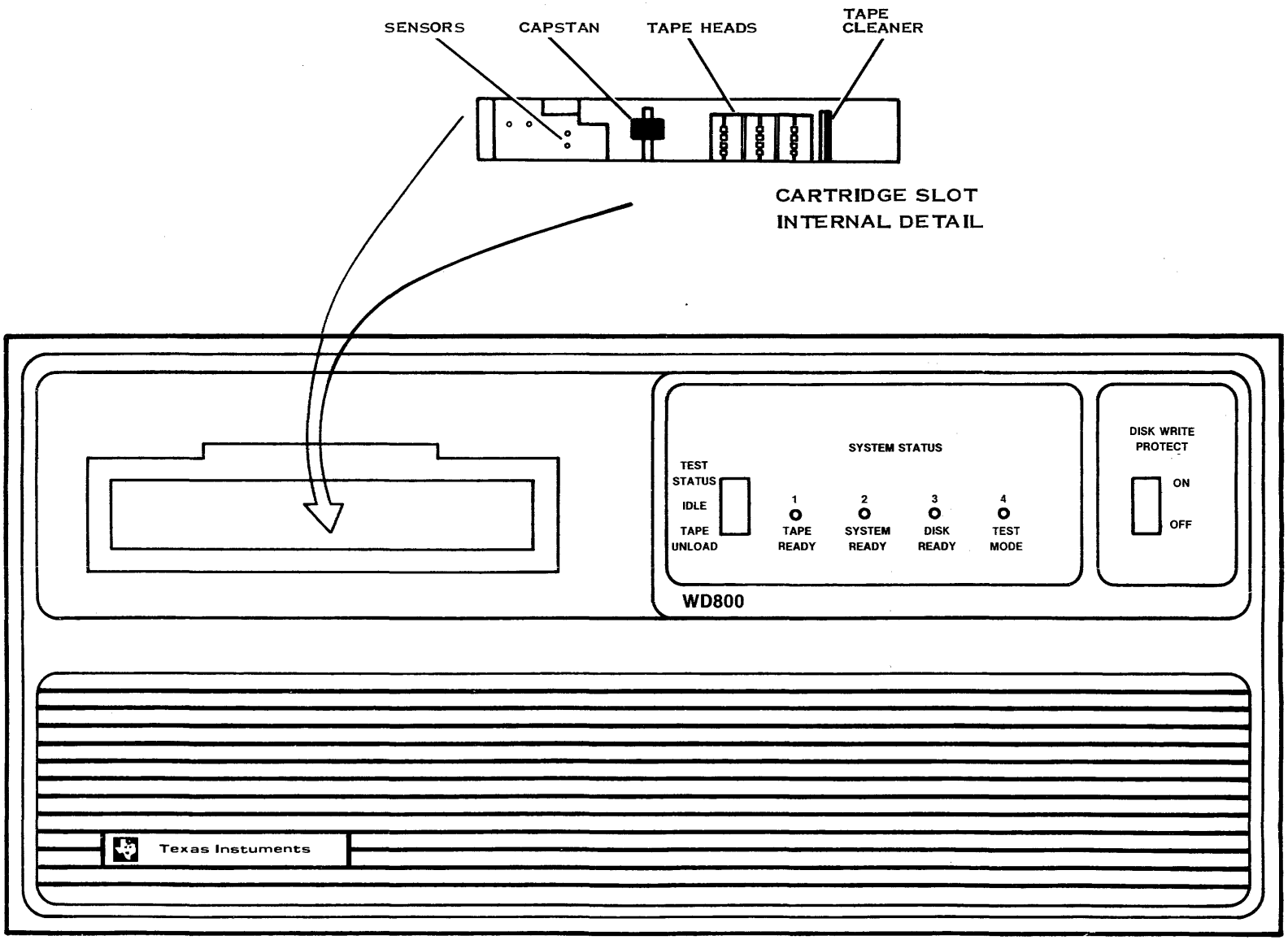

Figure 5-5. Tape Heads, Cleaner, Capstan, and Sensors

CAUTION

Failure to keep the heads, capstan, and sensors clean can result in degraded error rates, media interchange problems, or permanent damage to the media (including tape run-off).

5.4.2 Air Filter Cleaning

The cleanliness of the air that enters the WD800 subsystem chassis affects the lifetime of the subsystem. Keep the chassis and the general area clean and dust-free.

CAUTION

Do not use strong solvents to clean the front panel of the chassis. Use a mild detergent and water on a lint-free cloth.

Cooling air for the disk drive and electronic modules passes through a filter behind the front panel. This filter requires periodic PM as follows:

- Remove and vacuum the air filter every six weeks.
- Discard the old filter and replace with a new filter every six months.

Unsnap the entire front panel to remove the filter (Figure 5-6).

NOTE

An alternate front panel design (Figure 5-7) has snap-in filters in the front panel. The filters snap into and out of the front panel cutouts.

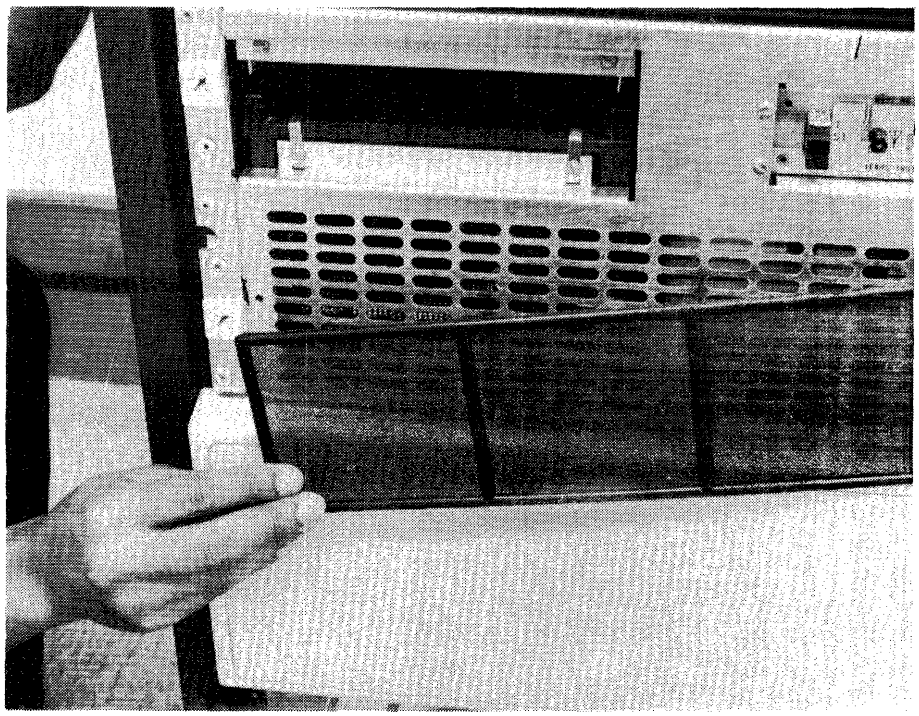

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Figure 5-6. Air Filter Removal

Operation

Figure 5-7. Alternate Front Panel Filter Removal

Appendix A

Fault Analysis

A.1 TPBI STAND-ALONE TEST

The following paragraphs describe self-test errors that occur when testing the TPBI board with the WD800 chassis disconnected from the PBI cable.

A.1.1 TPBI Indicators

There are four indicator LEDs on the TPBI board that help to locate failures in the system.

A.1.1.1 FAULT Indicator. The red FAULT LED (Figure A-1) lights when the self-test is initiated and extinguishes only after the self-test completes with no errors.

Continuous illumination of the FAULT LED indicates that a fault is detected, but the fault may not be in the TPBI board itself. A PBI cable or TILINE fault can cause this indication. Disconnect the PBI cable and repeat the self-test.

Blinking illumination of the FAULT LED indicates that a PBI error has been detected during operation. This condition is a warning that the system integrity is questionable. The condition can occur as a result of improper configuration procedures.

A.1.1.2 TILINE Indicator. The green TILINE LED Figure A-1 lights to indicate normal operation of the TILINE access controller on the TPBI board. If this indicator does not light, it indicates a TILINE failure. The following possibilities exist:

- Host backpanel configuration problem:
  - — TILINE access granted (TLAG) jumper open or improperly connected
  - — Fault in another TILINE device used in the host system
- TILINE bus fault

A.1.1.3 BUSY LEDs A and B. The green BUSY LEDs (Figure A-1) light to indicate activity by their respective slave sets. BUSY indicators light when the idle status bit is set to zero due to TPBI command execution.

A.1.2 TPBI Maintenance Commands

The TPBI maintenance commands are specified in the left byte of W3. The *WD800/WD800A Field Maintenance Manual* describes all of the maintenance commands. For convenience, Table A-1 lists the TPBI maintenance commands.

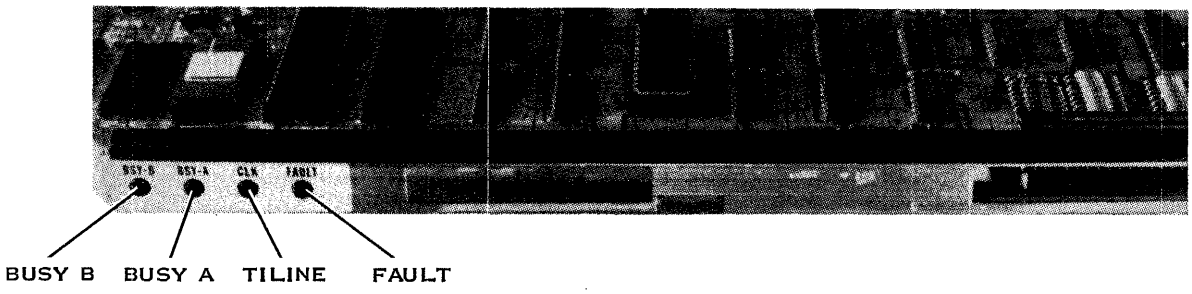

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Figure A-1. TPBI Indicators

Table A-1. TPBI Maintenance Commands

Test Number (Left Byte of W3)	Name
>40	Execute all stand-alone self-tests
>41	4K Read only memory (ROM)
>42	Random access memory (RAM)
>43	PBUS control
>44	TILINE address counters
>45	Register file A
>46	Register file B
>47	TILINE interrupt logic A
>48	TILINE interrupt logic B
>49	PIO data port
>4A	CTC and Z80 interrupt
>4B	Interface bus data and parity
>4C	PBUS control
>4D	TILINE master to slave set A write
>4E	TILINE master to slave set B write
>4F	TILINE master from slave set A read
>50	TILINE master from slave set B read
>7C	Read peripheral parameter block
>7D	Execute peripheral memory
>7E	Write peripheral memory
>7F	Read peripheral memory

A.2 WD800 CHASSIS STAND-ALONE TEST

The following descriptions apply to errors occurring at initial power-up with the PBI cable to the host system disconnected. Refer to Section 4 for a description of the normal front panel indicator sequence on power-up.

- All WD800 chassis indicators fail to light. Possible causes are:
  - — Power not applied to chassis
  - — Fuse defective
  - — Power supply defective
  - — Internal cable to indicators disconnected
  - — Processor PWB defective
- WD800 indicators fail to properly cycle through test mode. Possible causes are:
  - — Defective processor PWB
  - — Defective tape control PWB
- DISK READY indicator fails to light continuously after blinking. A possible cause is that the disk failed self-test (refer to Table A-2).
- TAPE READY indicator fails to blink when loading tape. Possible failures are:
  - — Stand-alone power-up delay not complete; wait for completion (TEST MODE indicator off)
  - — Tape failed self-test (refer to the error code table)
- TAPE READY indicator fails to turn on after loading complete. Possible failures are:
  - — Tape media defective; replace with known good media
  - — Tape hardware defective; use diagnostic to confirm

A.2.1 WD800 Error Code Analysis

The WD800 contains extensive self-test capability and performs these tests on power-up and system reset. When the self-test detects any failure in the system, read the error codes from the front panel indicators using the following procedure:

1. Momentarily position the TEST STATUS/TAPE UNLOAD switch to the up position.

2. The WD800 indicators display a binary-coded error from 0000 to 1111. Code 1111 means no error has been detected.

3. By momentarily positioning the TEST STATUS switch up in succession, you can read the self-test error codes for the WD800. When the displayed code reaches 1111, the list of failures is complete. The next time the TEST STATUS switch is positioned up, the normal system status is displayed on the WD800 front panel. Table A-2 lists the meaning of the error status codes for the WD800 system.

Table A-2. WD800 System Chassis Front Panel Error Codes

Error Code	Cause of Error
0000	Processor, interface, or motherboard PWBs; or power supply defective
0001	Processor, interface, or motherboard PWBs; or power supply defective
0010	Processor, interface, or motherboard PWBs; or power supply defective
0011	Tape control PWB defective
0100	Tape encode PWB defective
0101	Tape drive/analog assembly or cables defective
0110	Tape drive option not present or motherboard defective
1000	Disk HSD PWB defective
1001[1]	WD800: Disk servo defective WD800A: Disk interface PWB or cables defective or formatter test cylinders not found
1010	Disk read defective
1011	Disk write defective
1100	Disk not present
1110[2]	Host PBI cable disconnected or no TPBI present
1111	No fault

Note:

[1] On the WD800A, code 1001 is expected the first time the unit is powered up if the disk has not been initialized.

[2] Code 1110 is expected for stand-alone power-up verification.

A.2.2 Disk Maintenance Commands

The disk maintenance commands are specified in the left byte of W3. The *WD800/WD800A Field Maintenance Manual* describes all of the maintenance tests (see the Preface). For convenience, Table A-3 lists the test commands that the WD800 supports.

Table A-3. Disk Maintenance Commands

Test Number (Left Byte of W3)	Name
>00	Execute all disk self-tests (>01->13)
>01	Interface PCB presence test
>02	Interface first-in, first-out (FIFO) and port test
>03	Interface parity and attention register test
>04	Processor ROM CRC test
>05	Processor RAM address test
>06	Processor CTC test
>07	Processor PIO test
>08	Processor DMA and I/F test
>09	Processor wait generator test
>10	Servo test (WD800 only) Disk I/F test (WD800A only)
>11	HSD test
>12	Read test
>13	Write test
>14	WD800A test (tests >10 - >13)
>15	Reformat test cylinders
>16	Disk exerciser (WD800 only)
>17	Threshold control active (WD800 only) Alternate precompensation selection (WD800A only)
>18	Threshold control inactive Return to normal precompensation (WD800A only)
>19	Initialize formatter bad track map in RAM (WD800A only)
>1A	Read absolute header (WD800A only)
>3B	Pbus loop-back self-test
>3C	Read disk parameter block
>3D	Execute peripheral memory
>3E	Write peripheral memory
>3F	Read peripheral memory

Only the read disk parameter block command (Test >3C) is described in this manual. The read disk parameter block command transfers data in the disk parameter block that is useful for diagnostic and troubleshooting from WD800 memory to host memory. Table A-4 gives a summary of the information in this block. The command returns disk memory addresses for each parameter except the first parameter, which is two ASCII characters representing the firmware revision level. For this command, a transfer byte count of 22 (>16) for the WD800 or 34 (>22) for the WD800A must be specified.

Table A-4. Disk Parameter Block

Bytes	Parameter
2	Disk firmware revision level (two ASCII characters)
2	Retry count
2	Time-out count
2	Command inhibit flag
2	Program counter
2	Maximum addressable cylinder
2	Seek settling count (in WD800A)
2	Logical cylinder zero
2	Error block
2	Exerciser error count
2	First unused RAM space
2*	Start of formatter bad track map in RAM (WD800A only)
2*	Address of the following error pointer
1*	Pointer to last error that occurred
1*	Number of search errors
1*	Number of ID ECC errors
1*	Number of ID header not found errors
1*	Number of data errors
1*	Number of unsafe errors
1*	Number of seek incomplete errors

Note:

* WD800A only

Certain maintenance commands hang the system in a test loop until an I/O reset or power reset aborts the test. Refer to the *WD800/WD800A Field Maintenance Manual* for a complete description of the self-test routines.

A.2.3 Tape Maintenance Commands

The tape maintenance commands are specified in the left byte of W3. The *WD800/WD800A Field Maintenance Manual* describes all of the maintenance tests. For convenience, Table A-5 lists the test commands that are supported.

Table A-5. Maintenance Commands for the WD800 Tape System

Code	Name
>00 – >1F	Execute all tape self-tests (>01 – >09, >20 – >24)
>01 – >09	See Table A-3
>20	Tape test all
>21	Tape presence test
>22	Tape control test
>23	Tape encode/decode test
>24	Tape analog test
>29	Extended tape load
>2A	Go-to-early-warning-hole command
>2B – >3A	Execute all tape self-tests
>3B	Peripheral bus loop-back
>3C	Read peripheral parameter block
>3D	Execute peripheral memory
>3E	Write formatter memory
>3F	Read formatter memory

A.2.3.1 Execute All Stand-Alone Self-Tests (>00 through 1F and >2B through 3A). This maintenance command causes the formatter to execute all the stand-alone self-tests (those not requiring operator intervention) implemented in the peripheral device, and then to report status. If a self-test fails, the command aborts and reports status >XXFF in W7 and the failing test number and error code in W2.

NOTE

Test codes not used for self-test or device-unique special commands default to execute all stand-alone self-tests.

A.2.3.2 Tape-Unique Tests (>20 Through >24). The commands >20 through >24 are tape-specific self-tests, including all stand-alone self-tests. Specific definitions of these tests can be consulted in the *WD800/WD800A Field Maintenance Manual.*

A.2.3.3 Tape-Unique Special Commands (>29 and >2A). The WD800 tape system supports two special commands for diagnostic use: the extended tape load command and the extended go-to-early-warning-hole command. Details about these commands are in the *WD800/WD800A Field Maintenance Manual.*

A.2.3.4 Peripheral Bus Loop-Back Test (>3B). This command initiates a two-way transfer of known data across the peripheral bus between the formatter and the controller, which tests the validity of the bus. This command sends the bus test data to the controller and requests that the test data be sent back in one control status block (CSB) operation. The sequence of execution is identical to that used in bus initialization, except that a CSB is returned when the formatter finishes execution of the second part of the operation.

A.2.3.5 Read Peripheral Parameter Block (> 3C). This command transfers the data in the peripheral parameter block from the peripheral memory to the host memory. The tape parameter block provides useful diagnostic and troubleshooting information. Table A-6 gives a summary of this block. Note that the block is read-only, although the parameters with pointer addresses are both readable and writeable. Each entry in the parameter block is two bytes long. The tape parameter block contains 12 words.

Table A-6. Tape Peripheral Parameter Block

# Bytes	Parameter
2	Tape firmware revision level (two ASCII characters)
2	Retry count (not implemented)
2	Time-out count (not implemented)
2	Command inhibit flag
2	Program counter
6	Tape status bytes
6	Tape hardware register status
26	Tape interrupt status
2	Tape track
6	Tape test data patterns
12	Tape transfer count status
820	Tape buffer area

A.2.3.6 Execute Peripheral Memory (> 3D). This command forces the formatter to begin execution of the code starting in the address pointed to by the peripheral parameter program counter.

A.2.3.7 Write Peripheral Memory (> 3E). This command transfers the number of bytes specified in W4 from the host memory (starting at the address specified in W2) to the peripheral memory location.

A.2.3.8 Read Peripheral Memory (> 3F). This command transfers the number of bytes specified in W4 from the formatter memory (starting at the address specified in W2) to the host memory. This command is mainly used for reading peripheral parameters.

A.3 SYSTEM OPERATING PROBLEMS AND SUGGESTED ACTIONS

The following items assume that the PBI cable is connected to both the TPBI in the host system and the WD800 system chassis.

- TPBI red LED blinking — Peripheral BUS (PBUS) error.
  - — Check the chassis cabled to the TPBI, and see if the front panel indicators show an error.
  - — Check for unit selection overlap between multiple chassis. Refer to Section 3 for the proper unit selection procedure.

- — Check daisy chain cable termination. Ensure that only the last chassis has terminators installed.

- TPBI red LED on — Self-test fault.
  - — Turn off 990 power, disconnect cable at TPBI, and power up 990.
    - ... If red LED turns off, then either a WD800 chassis or cable fault exists.
    - ... If red LED stays on, then either a TPBI or 990 chassis fault is indicated.
  - — Chassis faults to check: TILINE access granted jumper.
  - — TPBI/configuration faults to check: TILINE address switches.
- WD800 system ready LED blinking — No communications with TPBI.
  - — Check cable connection at both ends.
  - — Check WD800 error code for interface PWB fault.
- WD800 front panel indicators show unusual status.
  - — Check test status switch — the indicators may be displaying test status. (Flip switch up repeatedly until all indicators light, then flip once more.)
  - — Possible symptoms include:
    - ... DISK READY does not flicker when disk activity in progress.
    - ... TAPE READY does not blink when tape inserted but tape moves.
    - ... Test mode indicator on, but system not in test mode.
    - ... All indicators on.
- Nothing happens when tape is inserted — TAPE READY indicator off but no tape movement.
  - — Tape self-test fault — See error code table.
- Tape unload switch does not respond — TAPE READY stays on.
  - — System activity locked out the unload; try again later.
- While using tape, TAPE READY turned off without unload.
  - — Tape media fatal error detected; replace cartridge with a known good tape.

Table A-7 provides examples of error status reports from the system log of the host 990 computer for disk; Table A-8 provides the same information for tape. These error messages are valid for both TPBI stand-alone testing and complete system operation.

Table A-7. Example 990 Disk Error Status Reports From System Log

DX10 System Log Report Format

```
160:  1432 + DS01   Err = 18  IID = 56  L = 04  A = 80F0  0600  0000  0000  0006  0B8E  0800  9801
                    ST02  RID = 57  F = 07  B = 0001  0400  0000  0000  0006  0B8E  0800  1000

Day  Time  Device Name        WD0 Disk Status  WD1 CMD/ HD#  WD2 Sec# S/T#  WD4 Byte Cnt/ Special  WD7 CMD Status
```

SVC Code	Disk Error Status	Explanation of Error Report
00	W7 status = 9400	Retries used, marginal track number in W3
00	W7 status = 9600	ECC correction, marginal track number in W3
10*	W7 status = 9100	I/O reset caused abnormal completion
11	W7 status = 9010	ID error, bad format on track number in W3
13*	W7 status = 9004	Command time-out, probable bus error
14*	W7 status = 9080	TILINE memory error
15	W7 status = 9440	Data error, bad or marginal track number in W3
16	W7 status = 90X0	Rate error
17	W7 status = 9002	Search error, bad sector number in W2
18*	W0 status = 80X0 W7 = 90FF	Disk offline, check power/cable TPBI failed self-test, error code in W2
19	W0 status = 40X0	Disk not ready
1A	W0 status = 20X0	Disk write-protected
1B	W0 status = 11X0	Unit lost power or cable disconnected on first access after power-up
1B	W0 status = 10X0	Disk unsafe due to device fault
1C	W0 status = X8X0	End of cylinder error
1D	W0 status = 04X0	Disk seek incomplete

Note:

* SVC codes marked with an asterisk could be TPBI/990 induced. All others are either software or WD800 induced.

Table A-8. Example 990 Tape Error Status Reports From System Log

DX10 System Log Report Format

```
160:  1432 + MT01   Err = 49  IID = 08  L = 04  A = 0070  0000  0000  0000  11FF  15CA  8604  8282
                    ST02  RID = 49  S = 03  B = 0000  0000  0000  0000  1FFF  07CA  8604  1000

Day   Time  Device Name                    WD0 Tape Status   WD2 S/T = Status   WD6 CMD   WD7 CMD Status
```

SVC Code	Tape Error Status	Explanation of Error Report
40	W0 status = 01X0	Command time-out, probable bus error
42	W0 status = 08X0	End-of-tape
43*	W0 status = 80X0	Tape offline/failed load/fatal media error
	W7 = 80FF	TPBI failed self-test, error code in W2
	W7 = 82FF	Tape failed self-test, error code in W2
44	W0 status = 04X0	Tape write-protected
45	W7 status = 8280	Tape media fault, write error
45	W7 status = 8220	Tape media fault; if write EOF, WD6 = X2XX. If read error, WD6 = X4XX
46*	W7 status = 8X04	TILINE memory error
47*	W7 status = 8100	I/O reset caused abnormal completion
48*	W7 status = 8X10	TILINE time-out
49	W7 status = 8282	Tape media fault — Dropout, write error
4A*	W7 status = 8208	System rate error, configuration problem

Note:

* SVC codes marked with an asterisk could be TPBI/990 induced. All others are either software or WD800 induced.

NOTE

Cartridge tape media is not error-free, so errors should be tolerated. If there are excessive media faults in a cartridge (more than 30 per use), take it out of service and replace it.

A.4 SERVICE CALL PROCEDURES

Before placing a service call, obtain the following information to relay when placing the call:

- Serial number of computer system
- Serial number of WD800 mass storage system
- Status indicated by front panel indicators
- Error codes displayed in front panel indicators in test status mode

Appendix B

TPBI Command Trace Feature

0.1 TPBI COMMAND TRACE BUFFER

The TPBI command trace buffer has the capability to store the most recent 16 commands executed by the TPBI as an aid to fault analysis and program development. A knowledge of 990 assembly language, as described in the *Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual*, is required to use the TPBI command trace feature. Commands are stored in the buffer in a circular fashion. When the end of the available buffer is reached, the trace returns to the beginning of the buffer and begins writing new commands over the commands previously stored. A command trace pointer also is provided to indicate the position occupied in the buffer by the most recent command executed. Figure B-1 is a sample assembly language program to initialize and to enable the command trace buffer.

```
***     CALL TO TRACE ENABLE    BLWP @TRCENA
***                             (R1=TPBI ADDRESS)
***     CALL TO READ TRACE      BLWP @TRREAD
***                             (R1=TPBI ADDRESS)
TRCENA DATA TRCWP          TRACE ENABLE WORKSPACE
       DATA TRCPC          TRACE ENABLE ENTRY POINT
TRREAD DATA TRCWP          TRACE READ WORKSPACE
       DATA TRRPC          TRACE READ ENTRY POINT
TRCWP  BSS  32             TRACE WORKSPACE
TRCNOW DATA >4100          VALUE TO LOAD INTO TPBI TO ENABLE TRACE
TRCNEW DATA >0000          RETRIEVED VALUE OF TRACE POINTER
***          COMMAND TO ENABLE TRACE IN TPBI
TRCENC DATA >0000          WD0 = NO ATTENTION MASK BIT SET
       DATA >8700          WD1 = DISK MAINTENANCE COMMAND
       DATA >4086          WD2 = INTERNAL TPBI ADDRESS
       DATA >7E00          WD3 = WRITE TO TPBI MEMORY COMMAND
       DATA >0002          WD4 = WRITE 2 BYTES (1 WORD)
       DATA TRCNOW         WD5 = TILINE ADDRESS = "TRCNOW"
       DATA >0F00          WD6 = TAPE MAINTENANCE COMMAND
       DATA >0000          WD7 = CLEAR IDLE BIT
***          COMMAND TO READ TRACE BUFFER
TRRCM1 DATA >0000          WD0 = NO ATTENTION MASK BIT SET
       DATA >8700          WD1 = DISK MAINTENANCE COMMAND
       DATA >4100          WD2 = INTERNAL TPBI ADDRESS
       DATA >7F00          WD3 = READ FROM TPBI MEMORY COMMAND
       DATA >0100          WD4 = READ 256 BYTES (16 COMMANDS)
       DATA BUFFER         WD5 = TILINE ADDRESS = BUFFER
       DATA >0F00          WD6 = TAPE MAINTENANCE COMMAND
       DATA >0000          WD7 = CLEAR IDLE BIT
```

Figure B-1. Routine to Enable TPBI Command Trace (Sheet 1 of 2)

```
***          COMMAND TO READ CURRENT TRACE POINTER VALUE
TRRCM2 DATA >0000          WD0 = NO ATTENTION MASK BIT SET
       DATA >8700          WD1 = DISK MAINTENANCE COMMAND
       DATA >4086          WD2 = INTERNAL TPBI ADDRESS
       DATA >7F00          WD3 = READ FROM TPBI MEMORY COMMAND
       DATA >0002          WD4 = READ 2 BYTES (1 WORD)
       DATA TRCNEW         WD5 = TILINE ADDRESS = TRCNEW
       DATA >0F00          WD6 = TAPE MAINTENANCE COMMAND
       DATA >0000          WD7 = CLEAR IDLE BIT
TRCPC  MOV  @2(R14),R1     GET TPBI ADDRESS FROM CALLING WORKSPACE
       LI   R2,TRCENC      GET ADDRESS OF TRACE ENABLE COMMAND
       BLWP @ISSUE         ISSUE COMMAND TO TPBI
***                        R1= TPBI ADDRESS
***                        R2= ADDRESS OF COMMAND TO BE ISSUED
       RTWP                DONE, RETURN TO CALLING ROUTINE
TRRPC  MOV  @2(R14),R1     GET TPBI ADDRESS FROM CALLING WORKSPACE
       LI   R2,TRRCM1      GET ADDRESS OF COMMAND TO READ TRACE BUFFER
       BLWP @ISSUE         ISSUE COMMAND TO TPBI
***                        R1= TPBI ADDRESS
***                        R2= ADDRESS OF COMMAND TO BE ISSUED
       LI   R2,TRRCM2      GET ADDRESS OF COMMAND TO READ TRACE POINTER
       BLWP @ISSUE         ISSUE COMMAND TO TPBI
***                        R1= TPBI ADDRESS
***                        R2= ADDRESS OF COMMAND TO BE ISSUED
       RTWP                DONE, RETURN
***          BUFFER NOW CONTAINS COMMAND TRACE TABLE FROM TPBI
***          TRCNEW NOW CONTAINS COMMAND TRACE POINTER FROM TPBI
```

Figure B-1. Routine to Enable TPBI Command Trace (Sheet 2 of 2)

Figure B-2 is a flowchart of the routine to enable the TPBI command trace.

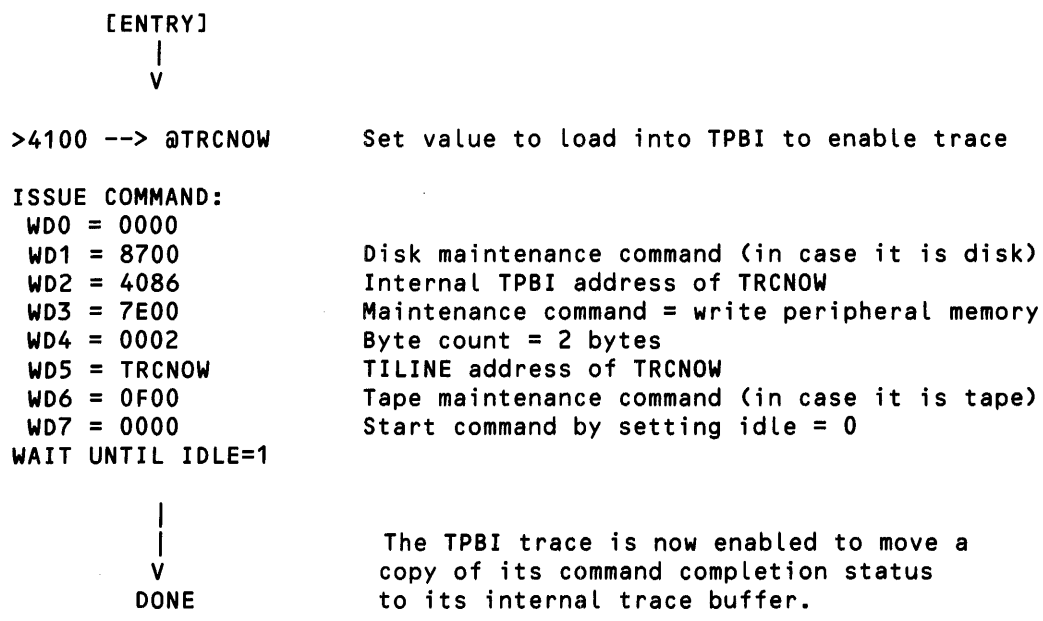

Figure B-2. Flowchart of Routine to Enable TPBI Command Trace

Figure B-3 is a flowchart showing how to read the TPBI command trace.

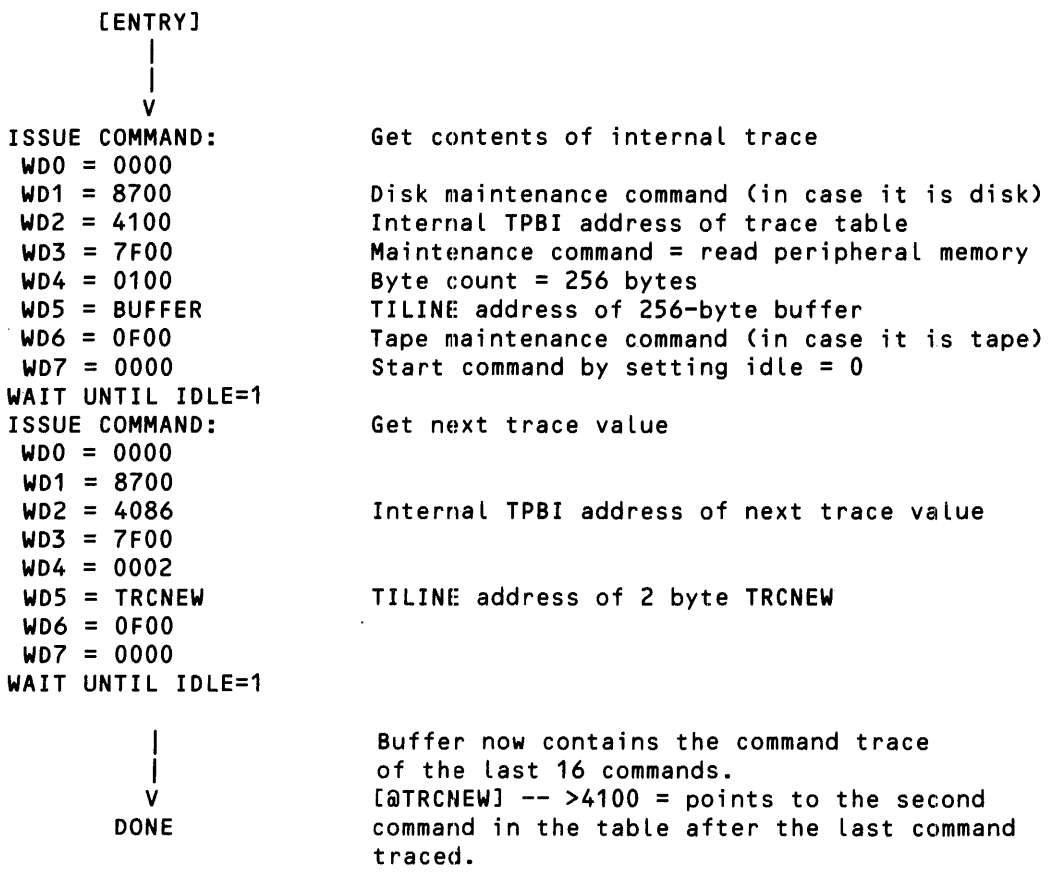

Figure B-3. Flowchart of Routine to Read TPBI Command Trace

Figure B-4 is a flowchart of the routine to disable the TPBI command trace.

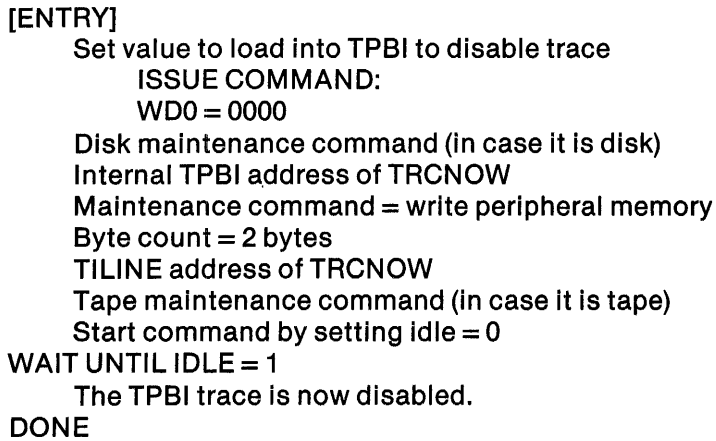

Figure B-4. Flowchart of Routine to Disable TPBI Command Trace

Figure B-5 is an example of the contents of a trace buffer.

```
     Start of buffer  --> BUFFER+000     WD0 CMND N-2
                          BUFFER+002     WD0 CMND N-2
                          BUFFER+004     WD0 CMND N-2
   Two commands ago  -->   :              :   :   :
                          BUFFER+00E     WD7 CMND N-2
                          BUFFER+010     WD0 CMND N-1
Command before last  -->   :              :   :   :
                          BUFFER+01E     WD7 CMND N-1
                          BUFFER+020     WD1 CMND N
      Latest command  -->   :              :   :   :
                          BUFFER+02E     WD7 CMND N
                          BUFFER+030     WD1 CMND N-15
                           :              :   :   :
                          BUFFER+03E     WD7 CMND N-15
  [@TRCNEW] - >4100   --> BUFFER+040     WD1 CMND N-14
                           :              :   :   :
                          BUFFER+04E     WD7 CMND N-14
                          BUFFER+050     WD0 CMND N-13
                           :              :   :   :
                          BUFFER+05E     WD7 CMND N-13
                           :              :   :   :
                           :              :   :   :
                          BUFFER+0F0     WD0 CMND N-3
                           :              :   :   :
End of buffer             BUFFER+0FE     WD7 CMND N-3
```

Figure B-5. Example of Trace Buffer Contents

Appendix C

Sample 990 Device Service Routines

C.1 CONTROL WORD EXAMPLES

The individual bits of the eight control words used to command the TPBI and mass storage subsystem are described in Section 2 and Section 3. Table C-1 shows the contents of these control words for a tape write operation and Table C-2 shows the contents of the control words for a tape rewind operation.

Table C-1. Example of Control Words for Tape Write Operation

Word Number	Word	Comments
0	>0000	No rewind interrupt
1	>0000	
2	>0000	
3	>0000	
4	>0050	Character count = >50 (decimal 80)
5	>00B3	TILINE memory byte address
6	>8600	Select unit 0; command = write
7	>0000	Reset status bits, interrupts not used; initiate operation

Table C-2. Example of Control Words for Tape Rewind Operation

Word Number	Word	Comments
0	>0000	No rewind interrupt
1	>0000	
2	>0000	
3	>0000	
4	>0001	Skip count = 1 record
5	>0000	TILINE memory byte address not used
6	>8300	Select unit 0; command = skip reverse
7	>0000	Reset status bits, interrupts not used; initiate operation

C.1.1 Sample Tape Program

Figure C-1 is a sample program that demonstrates the operation of the TPBI and the cartridge tape drive. This program is written in 990 assembly language. For descriptions of the assembly language instruction set, refer to the *Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual*. Most users will prefer to use the device service routine (DSR) supplied by Texas Instruments rather than writing assembly language I/O routines.

The sample program writes 80 characters on the tape, backspaces, and reads the same 80 characters from the tape. The program does not use interrupts at command completion. A status checking loop within the program monitors the idle bit (W7, bit 0) of the controller status word to detect command completion. This approach simplifies the coding of the program, but is inefficient in terms of central processor time.

The program listing is organized into seven columns as shown in the following example:

Input Line Number (Decimal)	Relocatable Memory Address (Hex)	Machine Operation Code (Hex)	Symbolic Address Label	Instruction Mnemonic	Operands (Decimal, Hex or Symbolic)	Comment Field
0033	0026 0028	0202 0028		LI	2, 40	COUNTER

```
SDSMAC 3.4.0 81.117    17:13:09 TUESDAY, MAR 02, 1982
                                                        PAGE 0002

0001 0000
0002                ************************************************************
0003                *              SAMPLE TAPE PROGRAM
0004                *
0005                * THIS PROGRAM SEGMENT WRITES 80 CHARACTERS ON TAPE,
0006                * BACKSPACES AND READS THE 80 CHARACTERS.
0007                *
0008                ************************************************************
0009       0000'    TAPEWP EQU  $              WORKSPACE REGISTERS
0010 0000 0000           DATA 0               REGISTER 0
0011 0002 0000           DATA 0               REGISTER 1
0012 0004 0000           DATA 0               REGISTER 2
0013 0006 0000           DATA 0               REGISTER 3
0014 0008 0000           DATA 0               REGISTER 4
0015 000A 0000           DATA 0               REGISTER 5
0016 000C 0000           DATA 0               REGISTER 6
0017 000E 0000           DATA 0               REGISTER 7
0018 0010 0000           DATA 0               REGISTER 8
0019 0012 0000           DATA 0               REGISTER 9
0020 0014 0000           DATA 0               REGISTER 10
0021 0016 0000           DATA 0               REGISTER 11
0022 0018 0000           DATA 0               REGISTER 12
0023 001A 0000           DATA 0               REGISTER 13
0024 001C 0000           DATA 0               REGISTER 14
0025 001E 0000           DATA 0               REGISTER 15
0026 0020 F880    TIADDR DATA >F880           TILINE ADDRESS OF TAPE
0027       0022' START  EQU  $
0028 0022 02E0           LWPI TAPEWP          SET UP WORKSPACE
     0024 0000'
0029 0026
0030                *
0031                * INITIALIZE BUFFERS
0032                *
0033 0026 0202           LI   2,40             COUNTER = BUFFER LENGTH IN WORDS
     0028 0028
0034 002A
0035 002A 0203           LI   3,OUTBUF         REG 3 = ADDRESS OF OUTPUT BUFFER
     002C 00B8'
0036 002E
0037 002E 0204           LI   4,INBUF          REG 4 = ADDRESS OF INPUT BUFFER
     0030 0108'
0038 0032
0039 0032 0205           LI   5,>1234          REG 5 = OUTPUT DATA
     0034 1234
0040 0036
0041 0036         INIT
0042 0036 CCC5           MOV  5,*3+            PUT 1234 IN OUTBUF
0043 0038 04F4           CLR  *4+              CLEAR INBUF
0044 003A 0602           DEC  2                DECREMENT LOOP COUNTER
0045 003C 16FC           JNE  INIT             IF NOT DONE JUMP BACK
0046                *
0047                * SET UP FOR WRITE TO TAPE
0048                *
0049 003E C0A0           MOV  @TIADDR,2        REG 2 = TILINE ADDRESS OF TAPE
     0040 0020'
0050 0042
0051 0042 C0C2           MOV  2,3              REG 3 = TILINE ADDRESS OF TAPE
0052 0044 0204           LI   4,WRITE          REG 4 = ADDRESS OF WRITE COMMAND
     0046 0088'
0053 0048
```

Figure C-1. Assembly Language Programming Sample for TPBI and WD800 Cartridge Tape Drive (Sheet 1 of 3)

```
          SDSMAC 3.4.0 81.117   17:13:09 TUESDAY, MAR 02, 1982.
                                                          PAGE 0003

0054 0048 0209          LI   9,8            REG 9 = LOOP COUNTER = 8
     004A 0008
0055 004C
0056 004C C209          MOV  9,8            REG 8 = LOOP COUNTER = 8
0057 004E         WRITE1
0058 004E CCF4          MOV  *4+,*3+        MOVE COMMAND TO TILINE
0059 0050 0608          DEC  8              DECREMENT LOOP COUNTER
0060 0052 16FD          JNE  WRITE1         IF NOT DONE, JUMP BACK
0061 0054 06A0          BL   @STATCK        IF DONE, GO CHECK STATUS
     0056 0074'
0062 0058
0063                    *
0064                    * SET UP FOR BACKSPACE COMMAND
0065                    *
0066 0058 C0C2          MOV  2,3            REG 3 = TILINE ADDRESS OF TAPE
0067 005A C209          MOV  9,8            REG 8 = LOOP COUNTER = 8
0068 005C         BS1
0069 005C CCF4          MOV  *4+,*3+        MOVE COMMAND TO TILINE
0070 005E 0608          DEC  8              DECREMENT LOOP COUNTER
0071 0060 16FD          JNE  BS1            IF NOT DONE, JUMP BACK
0072 0062 06A0          BL   @STATCK        IF DONE, GO CHECK STATUS
     0064 0074'
0073 0066
0074                    *
0075                    * SET UP FOR READ COMMAND
0076                    *
0077 0066 C0C2          MOV  2,3            REG 3 = TILINE ADDRESS OF TAPE
0078 0068         READ1
0079 0068 CCF4          MOV  *4+,*3+        MOVE COMMAND TO TILINE
0080 006A 0609          DEC  9              DECREMENT LOOP COUNTER
0081 006C 16FD          JNE  READ1          IF NOT DONE, JUMP BACK
0082 006E 06A0          BL   @STATCK        IF DONE, GO CHECK STATUS
     0070 0074'
0083 0072
0084 0072         DONE
0085 0072 0340          IDLE                WE ARE DONE, GO INTO IDLE
0086 0074
0087                    *
0088                    * SUBROUTINE TO CHECK TAPE STATUS
0089                    *
0090      0074' STATCK  EQU  $
0091 0074 C062          MOV  @14(2),1       REG 1 = R7 TAPE STATUS
     0076 000E
0092 0078
0093 0078 0A11          SLA  1,1            HAS COMMAND FINISHED EXECUTING
0094 007A 17FC          JNC  STATCK         IF NO, CONTINUE CHECKING
0095 007C C062          MOV  @14(2),1       REG 1 = R7 TAPE STATUS
     007E 000E
0096 0080
0097 0080 0281          CI   1,>C800        DO WE HAVE AN ERROR ?
     0082 C800
0098 0084
0099 0084 16F6          JNE  DONE           IF ERROR, GO TO IDLE
0100 0086 045B          RT                  RETURN AND EXECUTE NEXT COMMAND
0101                    *
0102                    * WRITE COMMAND
0103                    *
0104 0088 0000  WRITE   DATA 0              NO REWIND INTERRUPT
0105 008A 0000          DATA 0
0106 008C 0000          DATA 0
```

Figure C-1. Assembly Language Programming Sample for TPBI and WD800 Cartridge Tape Drive (Sheet 2 of 3)

```
          SDSMAC 3.4.0 81.117    17:13:09 TUESDAY, MAR 02, 1982.
                                                          PAGE 0004

 0107 008E 0000          DATA 0              NO OFFSET
 0108 0090 0050          DATA 80             CHARACTER COUNT
 0109 0092 00B8'         DATA OUTBUF           ADDRESS TO BE WRITTEN FROM
 0110 0094 8600          DATA >8600          UNIT = 1 AND COMMAND = WRITE
 0111 0096 0000          DATA 0              NO INTERRUPT
 0112              *
 0113              * BACKSPACE COMMAND
 0114              *
 0115 0098 0000  BS      DATA 0              NO REWIND INTERRUPT
 0116 009A 0000          DATA 0
 0117 009C 0000          DATA 0
 0118 009E 0000          DATA 0
 0119 00A0 0001          DATA 1              SKIP REVERSE 1 RECORD
 0120 00A2 0000          DATA 0
 0121 00A4 8300          DATA >8300          UNIT = 1 AND COMMAND = SKIP REV
 0122 00A6 0000          DATA 0              NO INTERRUPT
 0123              *
 0124              * READ COMMAND
 0125              *
 0126 00A8 0000  READ    DATA 0              NO REWIND INTERRUPT
 0127 00AA 0000          DATA 0
 0128 00AC 0000          DATA 0
 0129 00AE 0000          DATA 0              NO OFFSET
 0130 00B0 0050          DATA 80             CHARACTER COUNT
 0131 00B2 0108'         DATA INBUF          ADDRESS TO BE WRITTEN INTO
 0132 00B4 8400          DATA >8400          UNIT = 1 AND COMMAND = READ
 0133 00B6 0000          DATA 0              NO INTERRUPT
 0134 00B8       OUTBUF  BSS  80             80 CHARACTER OUTPUT BUFFER
 0135 0108       INBUF   BSS  80             80 CHARACTER INPUT BUFFER
 0136                    END
NO ERRORS,      NO WARNINGS
```

Figure C-1. Assembly Language Programming Sample for TPBI and WD800 Cartridge Tape Drive (Sheet 3 of 3)

Hexadecimal operands are identified by a greater than sign (>) preceding the number, as in >F880. Incorporate comments in the listing by inserting a preceding asterisk and a blank, as in:

```
* INITIALIZE BUFFERS.
```

Those machine operation codes followed by a prime mark (') are those that change when the program is relocated. For example, if the sample program is loaded beginning at location 1000_{16}, then the value 00B8' becomes $00B8_{16} + 1000_{16} = 10B8_{16}$.

Lines 9 through 25 are used to define a symbolic address for the program workspace (TAPEWP), to initially clear 16 workspace registers, and to define the TILINE base address for the TPBI control words. Line 28 loads the workspace pointer and is the first instruction to actually execute when the program runs. Lines 33 through 45 are used to initialize the memory buffer areas required for the program. A buffer length of 40 words corresponds to 80 characters. A loop loads all zeros into the input buffer locations and hexadecimal 1234 in all the output buffer locations.

Lines 49 through 56 set up the write operation. To perform the operation, the program sends the eight write control words from lines 104 through 111 to the controller. The first control word, W0, is sent to the base address, TIADDR. An auto-incrementing MOV statement selects successive write control words and sends them to successive TILINE addresses.

After the last control word is sent, the program branches to the status check subroutine (STATCK) of lines 90 through 100. The control acquires the TILINE and transfers the data from the output buffer to the tape. The status check subroutine checks the idle bit (W7, bit 0) of the controller status word until the idle bit goes to 1, indicating completion. At this point, the status check subroutine tests the status word by comparing it to an error mask. If no errors are indicated, the status check subroutine returns control to the program.

The backspace command is performed in a similar manner. The control words (lines 115 to 122) are transmitted to successive TILINE addresses, and then the program branches to the status check subroutine. Upon normal completion of the backspace operation, control returns to the main program.

The read segment, lines 77 through 82, transfers the read command words, lines 126 through 133, to the controller, then branches to the status check routine. The computer returns to the idle state (IDLE indicator lit) upon completion.

C.2 CONTROL WORD EXAMPLES

The individual bits of the eight control words used to command the TPBI and mass storage subsystem are described in Section 2 and Section 3. Table C-3 shows the contents of these control words for a disk seek operation, and Table C-4 shows the contents of the control words for a disk read operation.

Table C-3. Example of Control Words for Disk Seek Operation

Word Number	Word	Comments
0	>0000	Clear attention and attention mask bits
1	>0600	Seek command
2	>0000	Sectors/record and sector address not used
3	>000C	Cylinder address = >C (decimal 12)
4	>0000	Transfer byte count = 0
5	>0000	TILINE memory byte address not used
6	>0400	Select unit 1; TILINE address MSB not used
7	>0000	Reset status bits, interrupts not used; initiate operation

Table C-4. Example of Control Words for Disk Read Operation

Word Number	Word	Comments
0	>0000	Clear attention and attention mask bits
1	>0200	Read command
2	>0105	1 sector/record; sector 5
3	>000C	Cylinder address = >C (decimal 12)
4	>0050	Transfer byte count = >50 (decimal 80)
5	>00DA	TILINE memory byte address
6	>0040	Select unit 1; TILINE address MSB
7	>0000	Reset status bits, interrupts not used; initiate operation

C.2.1 Sample Disk Program

Figure C-2 is a sample program that demonstrates the operation of the TPBI and the Winchester or flexible disk drive. This program is written in 990 assembly language. For a description of the assembly language instruction set, refer to the *Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual*. Most users prefer to use the DSR supplied by Texas Instruments rather than writing assembly language I/O routines.

CAUTION

Do not use this sample program with an operating system. It is a stand-alone program for demonstration purposes only and cannot be used with any other real-time control processes.

The sample program commands a drive restore operation. The restore command clears the initial device status after power-up; it also clears failure status if the condition that caused the failure no longer exists. Restore also establishes a reference position for the head carriage assembly at track 00. All other head positioning operations are based on cumulative inward and outward steps that occur after the restore operation.

After the attention interrupt (and a successful status check), the program writes 40 words onto the disk and reads the same 40 words from the disk. A status checking loop monitors the idle bit (W7, bit 0) to detect command completion.

Lines 10 through 26 define a symbolic address for the program workspace (DISKWP), clear 16 workspace registers initially, and define the TILINE base address for the TPBI. Line 38 loads the workspace pointer and is the first instruction executed.

Line 41 activates the controller busy test (BUSYT), lines 124 through 128. If the controller is available, it issues restore command by moving eight control words (lines 132 through 140, RESTOR) to the controller via a loop (SEND1).

Line 64 initiates a subroutine (lines 113 through 120) that waits for the TPBI controller to become idle, then checks to see if the restore command initiates properly. Lines 67 through 69 wait for the restore command to complete. This is signified by the clearing of the not ready bit in the TPBI. If the restore command does not initiate properly, the program jumps to an idle instruction at DONE (line 108).

Lines 73 to 82 initialize the data buffer areas in memory. The output buffer (40 memory words) is loaded with >1234 in each location and the input buffer is cleared to all zeros. Upon successful completion of the programs, the input buffer (INBUF) is also filled with >1234 data.

The write set-up instructions are in lines 86 through 90, and the write (WRITE1) starts on line 92. Lines 144 through 151 show the eight control words for this command. The program spins in the status check (STATCK) subroutine until the controller returns to the idle state. The 40 words are stored on the disk when the controller returns to idle. If no errors are detected, the program sets up the read command. READ1 (lines 100 through 106) transmits the control words (READ, lines 155 through 162) to the controller. The program again spins in the status check loop until the controller transfers the 40 words into memory and returns idle.

The computer then returns to idle (DONE, line 108).

```
           SDSMAC 3.5.0 82.130    10:31:12 WEDNESDAY, AUG 03, 1983.
ACCESS NAMES TABLE                                                    PAGE 0001
SOURCE ACCESS NAME=      DS02.ENGR.REP029.TS
OBJECT ACCESS NAME=      DS02.ENGR.REP029.TO
LISTING ACCESS NAME=     DS02.ENGR.REP029.TL
ERROR ACCESS NAME=
OPTIONS=                 XREF
MACRO LIBRARY PATHNAME=
           SDSMAC 3.5.0 82.130    10:31:12 WEDNESDAY, AUG 03, 1983.
                                                                      PAGE 0002
0001               ************************************************************
0002               *             SAMPLE DISK PROGRAM
0003               *
0004               * THIS PROGRAM SEGMENT PERFORMS A RESTORE TO THE DISK.
0005               * IT THEN WRITES 40 WORDS ON A DISK
0006               * AND READS THE 40 WORDS FROM THE DISK TO A
0007               * MEMORY BUFFER AREA.
0008               ************************************************************
0009 0000                RORG
0010       0000' DISKWP EQU  $             WORKSPACE REGISTERS
0011 0000 0000         DATA 0             REGISTER 0
0012 0002 0000         DATA 0             REGISTER 1
0013 0004 0000         DATA 0             REGISTER 2
0014 0006 0000         DATA 0             REGISTER 3
0015 0008 0000         DATA 0             REGISTER 4
0016 000A 0000         DATA 0             REGISTER 5
0017 000C 0000         DATA 0             REGISTER 6
0018 000E 0000         DATA 0             REGISTER 7
0019 0010 0000         DATA 0             REGISTER 8
0020 0012 0000         DATA 0             REGISTER 9
0021 0014 0000         DATA 0             REGISTER 10
0022 0016 0000         DATA 0             REGISTER 11
0023 0018 0000         DATA 0             REGISTER 12
0024 001A 0000         DATA 0             REGISTER 13
0025 001C 0000         DATA 0             REGISTER 14
0026 001E 0000         DATA 0             REGISTER 15
0027               *
0028               *       ASSUME ADDRESS OF >F800, DISK UNIT 1
0029               *
0030               *       NOTE: THIS SAMPLE PROGRAM OPERATES WITHOUT
0031               *       INTERRUPTS.  FOR OPTIMUM SYSTEM PERFORMANCE
0032               *       IT IS RECOMENDED TO USE DEVICE INTERRUPTS.
0033               *       REFER TO THE APPROPRIATE DX10 PROGRAMMING
0034               *       GUIDE EXPLAINING DSR STRUCTURE.
0035               *
0036 0020 F800   TIADDR DATA >F800         TILINE ADDRESS OF DISK
0037       0022' START  EQU  $
0038 0022 02E0         LWPI DISKWP         SET UP WORKSPACE
     0024 0000'
0039               *
```

Figure C-2. Assembly Language Programming Sample for TPBI and WD800 Disk Drive (Sheet 1 of 4)

```
0040 0026 C0A0          MOV  @TIADDR,2
     0028 0020'
0041 002A 06A0          BL   @BUSYT
     002C 009C'
0042                 *
0043                 * SET UP FOR RESTORE TO DISK DRIVE
0044                 *
0045                 *       THE RESTORE COMMAND OPERATES AS FOLLOWS:
0046                 *       A RESTORE COMMAND IS ISSUED TO THE TPBI
0047                 *       AND THE TPBI GOES BUSY.  THE DISK SYSTEM RECEIVES
0048                 *       THE RESTORE COMMAND, SETS THE 'NOT READY' STATUS
0049                 *       BIT AND RETURNS THE CSB.  THE TPBI WILL THEN GO
0050                 *       IDLE.  WHEN THE RESTORE COMMAND COMPLETES IN THE
0051                 *       DISK SYSTEM, IT WILL SEND A STATUS BYTE TO THE TPBI
0052                 *       CLEARING THE 'NOT READY' STATUS .
0053                 *
0054                 *
0055 002E C182          MOV  2,6             REG 6 = TILINE ADDRESS OF DISK
0056 0030 0207          LI   7,RESTOR        REG 7 = ADDRESS OF RESTORE COMMAND
     0032 00A6'
          SDSMAC 3.5.0 82.130    10:31:12 WEDNESDAY, AUG 03, 1983.
                                                                  PAGE 0003
0057 0034 0208          LI   8,8             REG 8 = LOOP COUNTER = 8
     0036 0008
0058                 *
0059      0038' SEND1   EQU  $
0060 0038 CDB7          MOV  *7+,*6+         MOVE COMMAND TO TILINE
0061 003A 0608          DEC  8               DECREMENT LOOP COUNTER IN R8
0062 003C 16FD          JNE  SEND1           IF NOT DONE, JUMP BACK
0063                 *
0064 003E 06A0          BL   @STATCK         WAIT FOR THE TPBI TO GO IDLE
     0040 0088'
0065                 *                       AND SEE IF CSB RETURNED IS GOOD
0066                 *
0067 0042 C052  WAITNR MOV   *2,1            GET COPY OF SLAVE REGISTER 0
0068 0044 0A21          SLA  1,2             0: IS THE 'NOT READY' BIT SET
0069 0046 18FD          JOC  WAITNR           * YES, WAIT FOR IT TO CLEAR
0070                 *
0071                 * INITIALIZE BUFFERS
0072                 *
0073 0048 0202          LI   2,40            COUNTER = BUFFER LENGTH IN WORDS
     004A 0028
0074 004C 0203          LI   3,OUTBUF        REG 3 = ADDRESS OF OUTPUT BUFFER
     004E 00D6'
0075 0050 0204          LI   4,INBUF         REG 4 = ADDRESS OF INPUT BUFFER
     0052 0126'
0076 0054 0205          LI   5,>1234         REG 5 = OUTPUT DATA
     0056 1234
0077                 *
0078      0058' INIT    EQU  $
0079 0058 CCC5          MOV  5,*3+           PUT 1234 IN OUTBUF
0080 005A 04F4          CLR  *4+             CLEAR INBUF
0081 005C 0602          DEC  2               DECREMENT LOOP COUNTER
0082 005E 16FC          JNE  INIT            IF NOT DONE JUMP BACK
0083                 *
0084                 * SET UP FOR WRITE TO DISK
0085                 *
0086 0060 C0A0          MOV  @TIADDR,2       REG 2 = TILINE ADDRESS OF DISK
     0062 0020'
```

Figure C-2. Assembly Language Programming Sample for TPBI and WD800 Disk Drive (Sheet 2 of 4)

```
0087 0064 C0C2          MOV   2,3          REG 3 = TILINE ADDRESS OF DISK
0088 0066 0204          LI    4,WRITE      REG 4 = ADDRESS OF WRITE COMMAND
     0068 00B6'
0089 006A 0209          LI    9,8          REG 9 = LOOP COUNTER = 8
     006C 0008
0090 006E C209          MOV   9,8          REG 8 = LOOP COUNTER = 8
0091                *
0092       0070' WRITE1 EQU   $
0093 0070 CCF4          MOV   *4+,*3+      MOVE COMMAND TO TILINE
0094 0072 0608          DEC   8            DECREMENT LOOP COUNTER
0095 0074 16FD          JNE   WRITE1       IF NOT DONE, JUMP BACK
0096 0076 06A0          BL    @STATCK      IF DONE, GO CHECK STATUS
     0078 0088'
0097                *
0098                * SET UP FOR READ COMMAND
0099                *
0100 007A C0C2          MOV   2,3          REG 3 = TILINE ADDRESS OF DISK
0101                *
0102       007C' READ1  EQU   $
0103 007C CCF4          MOV   *4+,*3+      MOVE COMMAND TO TILINE
0104 007E 0609          DEC   9            DECREMENT LOOP COUNTER
0105 0080 16FD          JNE   READ1        IF NOT DONE, JUMP BACK
0106 0082 06A0          BL    @STATCK      IF DONE, GO CHECK STATUS
          SDSMAC 3.5.0 82.130   10:31:12 WEDNESDAY, AUG 03, 1983.
                                                                    PAGE 0004
     0084 0088'
0107                *
0108       0086' DONE   EQU   $
0109 0086 0340          IDLE               WE ARE DONE, GO INTO IDLE
0110                *
0111                * SUBROUTINE TO CHECK DISK STATUS
0112                *
0113       0088' STATCK EQU   $
0114 0088 C062          MOV   @14(2),1     REG 1 = R7 DISK STATUS
     008A 000E
0115 008C 0A11          SLA   1,1          HAS COMMAND FINISHED EXECUTING
0116 008E 17FC          JNC   STATCK       IF NO, CONTINUE CHECKING
0117 0090 C062          MOV   @14(2),1     REG 1 = R7 DISK STATUS
     0092 000E
0118 0094 0281          CI    1,>C000      DO WE HAVE AN ERROR?
     0096 C000
0119 0098 16F6          JNE   DONE         IF ERROR, GO TO IDLE
0120 009A 045B          RT                 RETURN AND EXECUTE NEXT COMMAND
0121                *
0122                * SUBROUTINE TO TEST TPBI BUSY
0123                *
0124       009C' BUSYT  EQU   $
0125 009C C062          MOV   @14(2),1     REG 1 = R7 DISK STATUS
     009E 000E
0126 00A0 0A11          SLA   1,1
0127 00A2 17FC          JNC   BUSYT
0128 00A4 045B          RT
0129                *
0130                * RESTORE COMMAND
0131                *
0132       00A6' RESTOR EQU   $
0133 00A6 0000          DATA  >0           NO ATTENTION INTERRUPTS ENABLED
0134 00A8 0700          DATA  >0700        STORE REGISTERS COMMAND
```

Figure C-2. Assembly Language Programming Sample for TPBI and WD800 Disk Drive (Sheet 3 of 4)

```
0135 00AA 0000          DATA >0000
0136 00AC 0000          DATA >0000
0137 00AE 0000          DATA >0000
0138 00B0 0000          DATA >0000
0139 00B2 0400          DATA >0400        SELECT UNIT 1
0140 00B4 0000          DATA >0000        ACTIVATE TPBI
0141              *
0142              * WRITE COMMAND
0143              *
0144 00B6 0000  WRITE   DATA 0            NO ATTENTION INTERRUPTS ENABLED
0145 00B8 0300          DATA >0300        WRITE CMD
0146 00BA 0105          DATA >0105        ONE SECTOR/RECORD,SECTOR5
0147 00BC 000C          DATA >000C        CYLINDER C(HEX)=12(DEC)
0148 00BE 0050          DATA 80           BYTE COUNT...80(DEC)=40 WORDS
0149 00C0 00D6'         DATA OUTBUF         ADDRESS TO BE WRITTEN FROM
0150 00C2 0400          DATA >0400        UNIT = 1
0151 00C4 0000          DATA 0            NO INTERRUPT ENABLED
0152              *
0153              * READ COMMAND
0154              *
0155 00C6 0000  READ    DATA 0            NO ATTENTION INTERRUPT ENABLED
0156 00C8 0200          DATA >0200        READ CMD
0157 00CA 0105          DATA >0105
0158 00CC 000C          DATA >000C        CYLINDER C (HEX)
0159 00CE 0050          DATA 80           BYTE COUNT = 80(DEC)
0160 00D0 0126'         DATA INBUF        ADDRESS TO BE WRITTEN INTO
0161 00D2 0400          DATA >0400        UNIT = 1
          SDSMAC 3.5.0 82.130   10:31:12 WEDNESDAY, AUG 03, 1983.
                                                                  PAGE 0005
0162 00D4 0000          DATA 0            NO INTERRUPT ENABLED
0163 00D6       OUTBUF  BSS  80           80 BYTE OUTPUT BUFFER
0164 0126       INBUF   BSS  80           80 BYTE INPUT BUFFER
0165      0022'         END START
NO ERRORS,      NO WARNINGS
          SDSMAC 3.5.0 82.130   10:31:12 WEDNESDAY, AUG 03, 1983.
LABEL     VALUE   DEFN  REFERENCES                                  PAGE 0006
$         0176'         0010  0037  0059  0078  0092  0102  0108  0113  0124
                        0132
BUSYT     009C'   0124  0041  0127
DISKWP    0000'   0010  0038
DONE      0086'   0108  0119
INBUF     0126'   0164  0075  0160
INIT      0058'   0078  0082
OUTBUF    00D6'   0163  0074  0149
READ      00C6'   0155
READ1     007C'   0102  0105
RESTOR    00A6'   0132  0056
SEND1     0038'   0059  0062
START     0022'   0037  0165
STATCK    0088'   0113  0064  0096  0106  0116
TIADDR    0020'   0036  0040  0086
WAITNR    0042'   0067  0069
WRITE     00B6'   0144  0088
WRITE1    0070'   0092  0095
```

Figure C-2. Assembly Language Programming Sample for TPBI and WD800 Disk Drive (Sheet 4 of 4)

Index

This index lists key topics of this manual and specifies where each topic appears, as follows:

- Sections — Section references appear as *Section n*, where *n* represents the section number.
- Appendixes — Appendix references appear as *Appendix Y*, where *Y* represents the appendix letter.
- Paragraphs — Paragraph references appear as alphanumeric characters separated by decimal points. The first character refers to the section or appendix containing the paragraph, and any other numbers indicate the sequence of the paragraph within the section or appendix. For example:
  - *3.5.2* refers to Section 3, paragraph 5.2.
  - *A.2* refers to Appendix A, paragraph 2.
- Figures — Figure references appear as *Fn-x* or *FY-x*, where *n* represents the section and *Y* represents the appendix containing the figure; *x* represents the number of the figure within the section or appendix. For example:
  - *F2-7* refers to the seventh figure in Section 2.
  - *FG-1* refers to the first figure in Appendix G.
- Tables — Table references appear as *Tn-x* or *TY-x*, where *n* represents the section and *Y* represents the appendix containing the table; *x* represents the number of the table within the section or appendix. For example:
  - *T3-10* refers to the tenth table in Section 3.
  - *TB-4* refers to the fourth table in Appendix B.
- See and See also references — *See* and *See also* direct you to other entries in the index. For example:

  Logical Unit Number ..... *See* LUNO

  Device ..... *See also* individual device names or numbers

Page numbers that correspond to these index references appear in the Table of Contents.

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