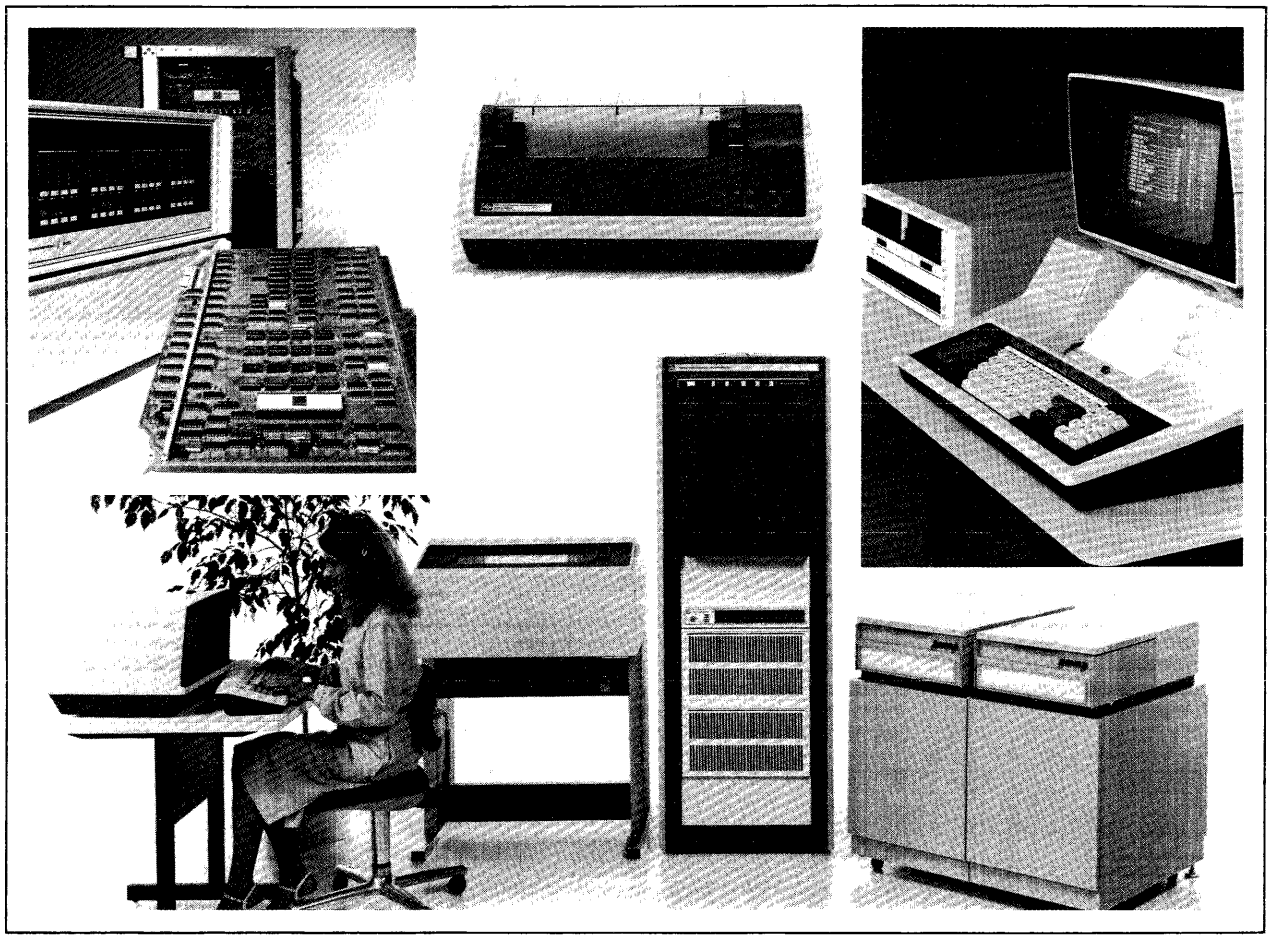
Model 990 Computer
Model FD1000 Flexible Disk Controller
and International Chassis Power Supply



Depot Maintenance Manual
Volume I

Part No. 2261885-9701 **
15 January 1981

TEXAS INSTRUMENTS

MANUAL REVISION HISTORY

Model 990 Computer Model FD1000 Flexible Disk Controller and International Chassis Power Supply Depot Maintenance Manual, Volume I (2261885-9701 **)

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Preface

This manual contains the theory of operation and depot-level maintenance information for the following components of the FD1000 Flexible Disk System:

Device	Part Number
TILINE Flexible Disk Controller (multilayer)	2261690-0001
TILINE Flexible Disk Controller (fineline)	2267295-0001
International Chassis Power Supply	2261695-0001
Buffered International Chassis Power Supply	2269979-0001

The TILINE Flexible Disk Controller (TFDC) is a major component of the Model FD1000 Flexible Disk System (with domestic chassis) and the Model FD1000A/B Flexible Disk System (with international chassis). The International Chassis Power Supply is a major component of the international chassis that is supplied with the FD1000A/B disk system.

Volume I of this manual contains Sections 1, 2, and 3. Volume II contains the appendixes. The sections and appendixes are:

Section

1 General Description — Standard equipment interconnections, physical descriptions, control and status word summary, diskette formats.

2 Theory of Operation — Detailed theory of operation, proceeding from the basic block diagram level to the logic diagrams, state diagrams and timing diagrams. Includes description of control program firmware.

3 Maintenance — Checkout, troubleshooting, and fault isolation based on self-tests, extended self-tests, and diagnostic software.

Appendix

A 9900 Control Program Flowcharts

B 9900 Control Program Listing

C Signature Dictionary — Power Supply/Interface Board

D Signature Dictionary — TFDC Board

E Diagrams — TFDC

F Diagrams — Power Supply/Interface Board

The following documents contain additional information related to FD1000 and FD1000A/B systems:

Title	Part Number
Model 990 Computer Model FD1000 Flexible Disk System Installation and Operation	2261886-9701
Model 990 Computer Model FD1000 Flexible Disk System with International Chassis Installation and Operation	2250698-9701
Model 990 Computer Model FD1000 Flexible Disk System Field Maintenance Manual	0945419-9703
Model 990 Computer Unit Diagnostics Handbook	
Volume 1 General 990 Unit Diagnostic Information	0945400-9701
Volume 3 Diagnostics for 990 Mass Storage Devices	0945400-9703
Model 990 Computer Family Maintenance Drawings	
Volume I Computer Chassis and Enclosures	0945421-9701
Volume II Processors and Memories	0945421-9702
Volume IV TILINE Expansion and Peripherals	0945421-9704
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	0943441-9701
Model 990/12 Computer Assembly Language Programmer's Guide	2250077-9701

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2 — Theory of Operation

3 — Maintenance

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GENERAL DESCRIPTION

1.1 GENERAL

The Model FD1000 Flexible Disk System provides on-line mass storage and convenient off-line archival storage to supplement the main memory of a Model 990 Computer with TILINE* parallel data bus. This manual provides an overview of the flexible disk system and detailed depot maintenance information for the following system components:

Component	Part Number
TILINE Flexible Disk Controller (multilayer version)	2261690-0001
TILINE Flexible Disk Controller (fineline version)	2267295-0001
International Chassis Power Supply	2261694-0001
Buffered International Chassis Power Supply	2269977-0001

An FD1000 system includes either the multilayer or the fineline version of the TILINE Flexible Disk Controller (TFDC). These two logic boards differ in component layout, but operate in a nearly identical manner.

FD1000 systems may include either the domestic chassis with a standard commercial power supply or the international chassis with either the International Chassis Power Supply or the Buffered International Chassis Power Supply. Either version of the international power supply performs signal interface functions in addition to providing dc power. For this reason, the term "power supply/interface board" is used in this manual to refer to either version of the international chassis power supply.

Double-sided, double-density (DSDD) diskettes are the standard storage media for the flexible disk system. These diskettes store up to 1.2 megabytes of data (formatted) with a record format directly compatible with the DX10 operating system file structure. FD1000 systems also accept single-sided, single-density (SSSD) diskettes for transportability to Texas Instruments FD800 and IBM 3740 systems. Utility programs (provided in DX10) are required to perform file translation to or from single-sided diskettes. Note also that any software that includes FD800 device-dependent code will not self-load in an FD1000 system.

* Trademark of Texas Instruments Incorporated

FD1000 system features include:

- Single-board controller that operates up to four drives with any mix of single-sided and double-sided diskettes
- Automatic diskette type detection and operating mode selection
- Positive write protect (ANSI standard)
- Programmable interlacing capability that allows disk system response to be optimized to a user's software system
- Remote drives up to 300 feet from the controller board (international chassis only)
- Automatic self-test and extensive on-board diagnostic test capability
- International chassis version meets international regulatory agency requirements for safety, electromagnetic radiation, and design practice.

FD1000 systems may include either the domestic chassis or the international chassis. Either chassis provides physical mounting and dc power for one or two diskette drive units in a tabletop or rackmount configuration. Cabling provisions differ, as the domestic chassis uses a local daisy-chain bus cable and the international chassis uses a remote serial interface. Parallel/serial conversion in the international chassis is performed by the power supply/interface board.

The FD1000 flexible disk system with international chassis is compatible with any Model 990 Computer that incorporates the TILINE data bus. The international version meets the safety, radiation, and design practice requirements of the major international regulatory agencies, such as UL, VDE, and CSA.

The domestic chassis contains a standard modular power supply that does not incorporate signal interface functions. The domestic chassis is not compatible with the 17-slot computer chassis due to restrictions against flat cables in that chassis. The domestic chassis has been phased out of production in favor of the international chassis.

NOTE

The international chassis with DSDD drives is designated as Model FD1000A or FD1000B to distinguish it from the domestic chassis.

1.2 SUBSYSTEM DESCRIPTION

Figure 1-1 is a block diagram of the flexible disk system with the domestic chassis. Note that all drive units are connected along a single bus. Figure 1-2 is the corresponding block diagram for the FD1000A/B international chassis. One controller cable is required by each international chassis. An intrachassis parallel bus (internal to the chassis) serves one or two drives.

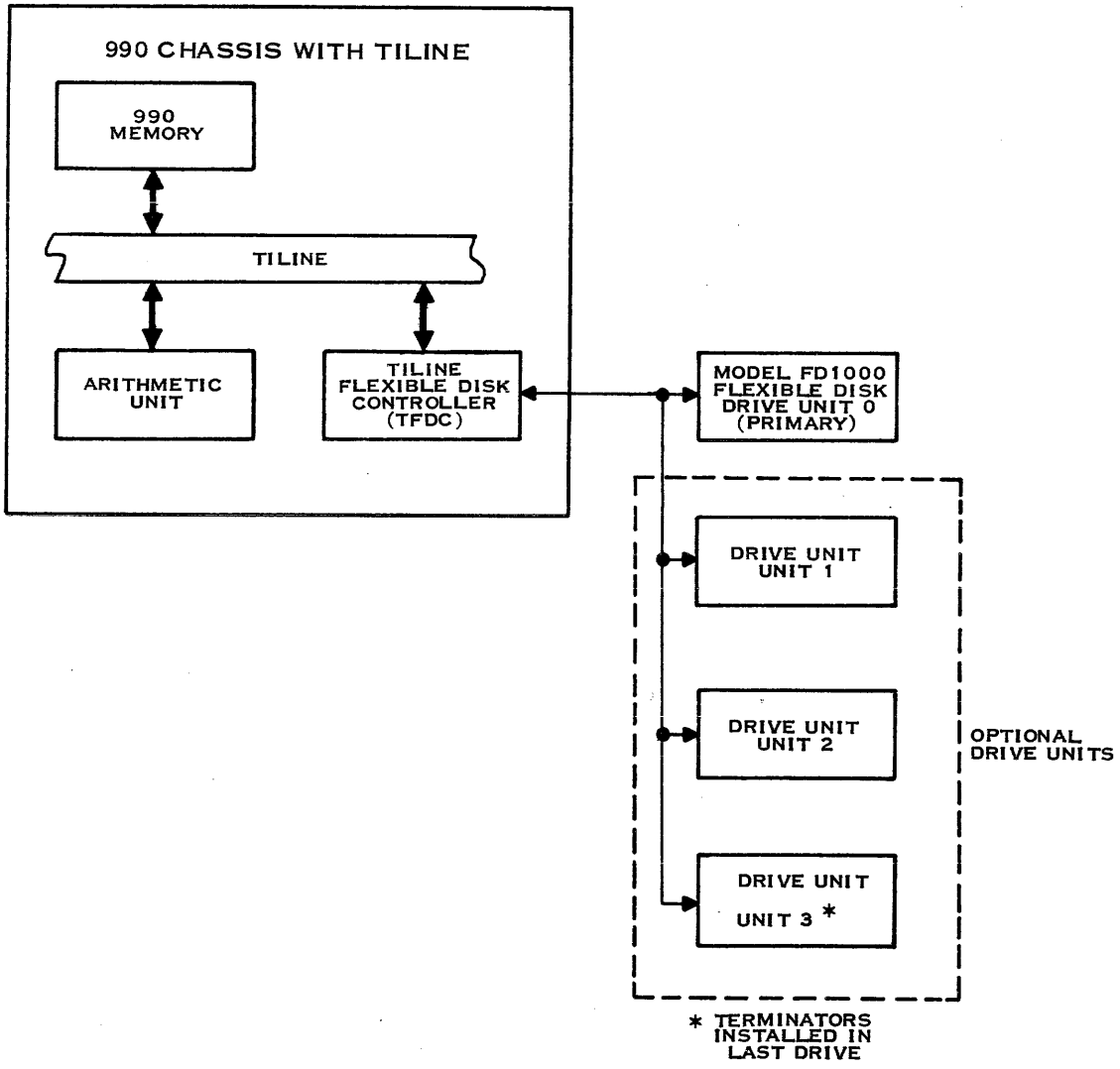

Figure 1-1. Simplified Diagram of Flexible Disk System with Domestic Chassis

The TFDC is a full-width circuit board occupying one full slot in the 990 computer chassis or TILINE expansion chassis. The 990 central processor unit (CPU) initiates, controls, and checks the status of TFDC operations via a block of eight reserved TILINE addresses. Once the operation has been initiated, the TFDC manages the necessary record location, control/status signal interchange, TILINE memory access, data transmission, error checking, and format conversion operations. Upon completion of the operation, the 990 CPU may read back one or all of the control word addresses that now contain controller, drive, and operation status information. This is the same control/status scheme used by the DS31, DS10, and DS25/DS50 hard-disk systems.

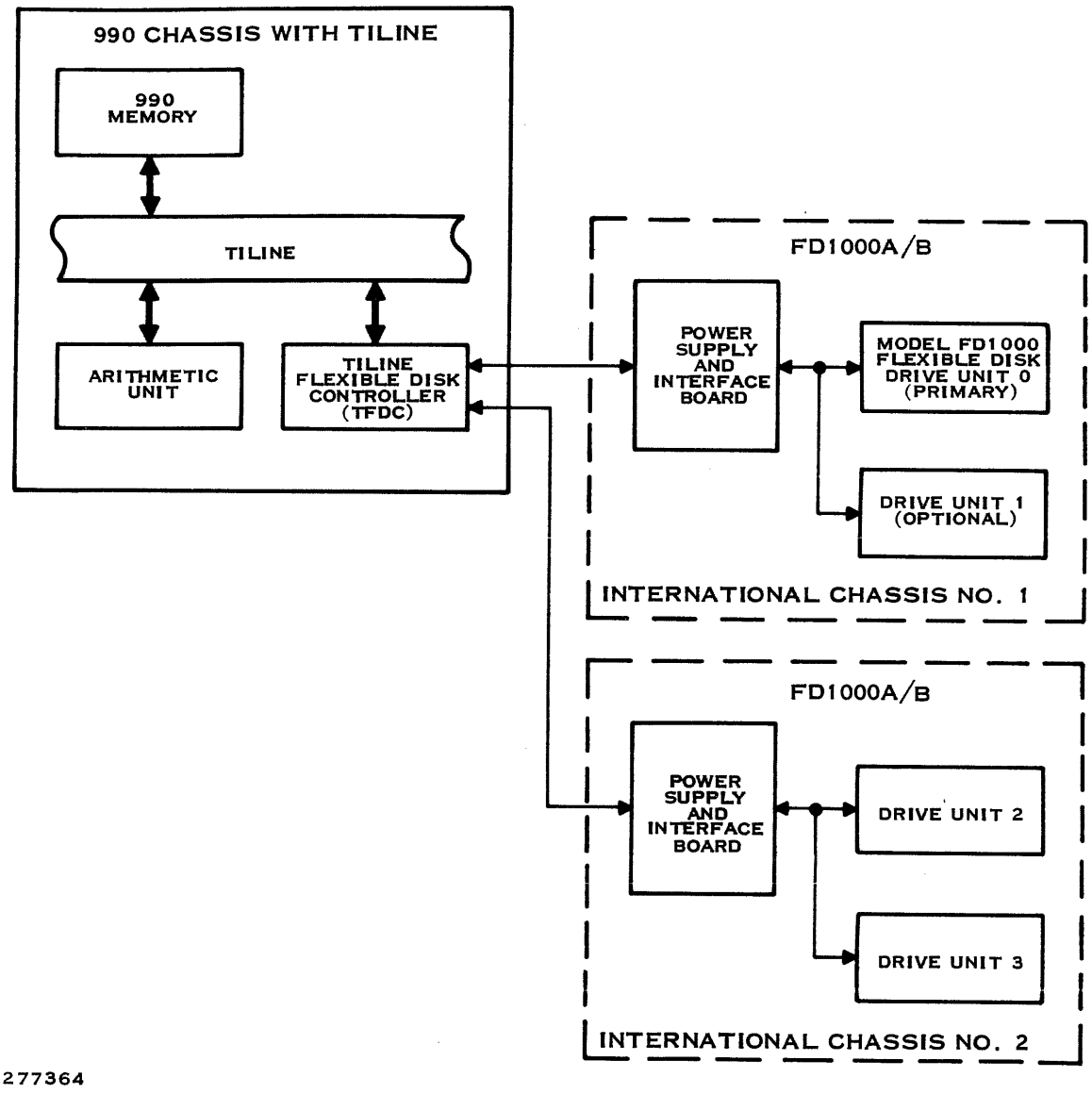

Figure 1-2. Simplified Diagram of Flexible Disk System with International Chassis

The control words are transmitted to or from the controller using any of the 990/9900 instructions that involve memory data transfer, such as MOV. The control word scheme is transparent to the user of a Texas Instruments operating system because the device service routine (DSR) handles all of these details. Maintenance personnel may need to enter commands via the 990 programmer panel or the diagnostic operation control system (DOCS) batch stream verbs.

The controller may select any one of four drive units for operation. Individual drive select signals to the drive units enable the interchange of control, status, and data signals between the selected drive and the controller. Data between the controller and the selected drive is exchanged over serial read data and write data lines. Data is recorded in frequency-modulated (FM) mode for a single-sided diskette and modified FM (MFM) mode for a DSDD diskette. Sensors in each drive automatically sense the type of diskette installed. A status signal from the selected drive unit to the controller identifies the diskette type.

1.3 SYSTEM CONFIGURATION

The controller has two remote input/output connectors and one local connector. The local input/output connector is used with the domestic chassis, and the remote connectors are used with the international chassis.

1.3.1 FD1000 Domestic System Configuration

The domestic chassis, marked "FD1000" on the chassis rear panel nameplate, requires a 50-pin, flat, daisy-chain cable as shown in Figures 1-3 through 1-5. Notice that the daisy-chain cable connects directly to edge connectors on the drive units in the domestic chassis. The flat cable connectors are not keyed, so it is possible to accidentally reverse a cable connector. The red index stripe goes to the right of the drive connector as viewed from the rear of the drive.

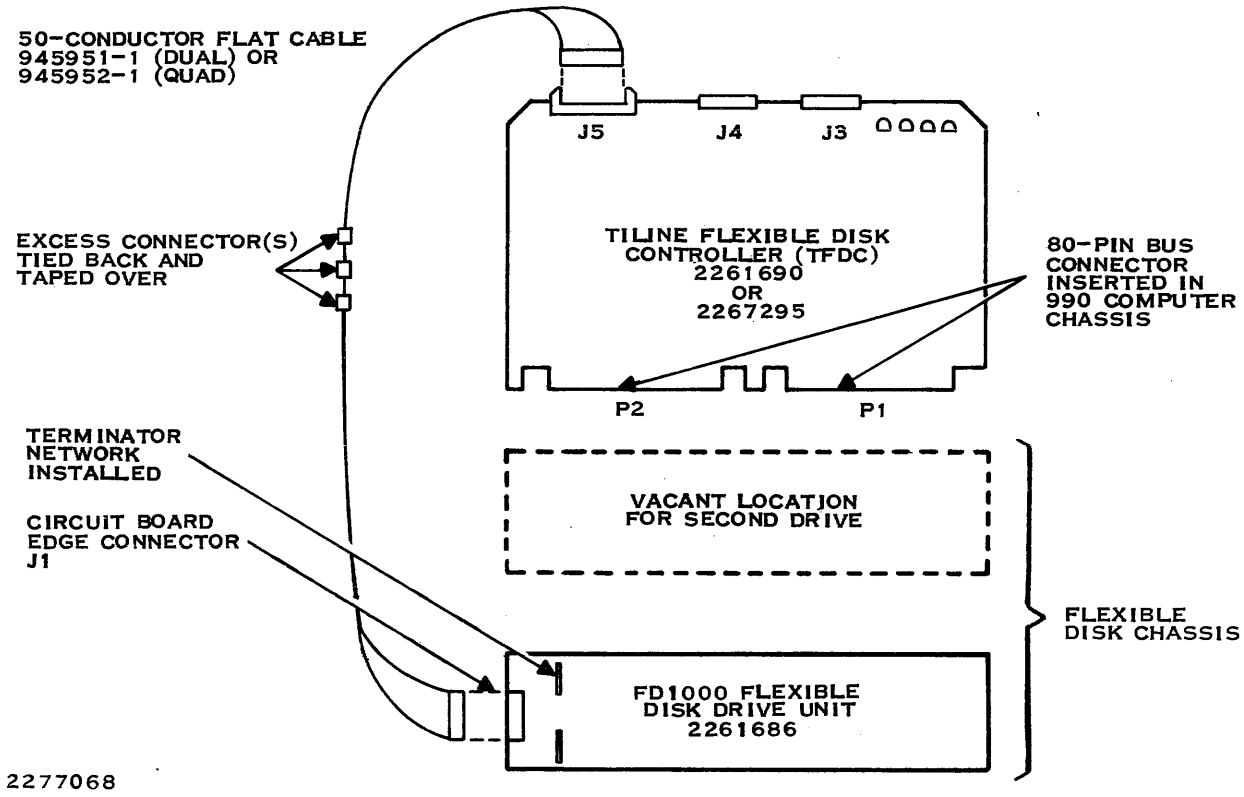

Figure 1-3. Domestic FD1000 System Configuration — Single Drive

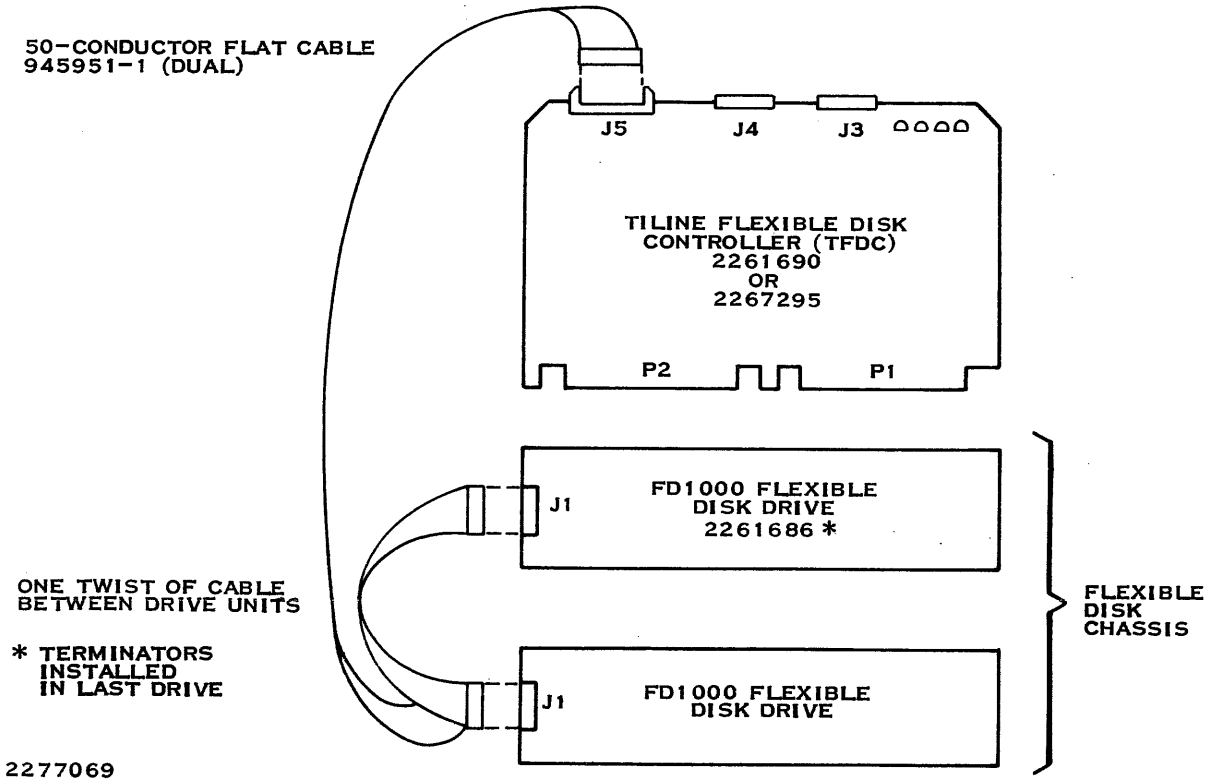

Figure 1-4. Domestic FD1000 System Configuration — Dual Drives

The flat cable used with the domestic chassis is limited to 3.06 meters (10 ft) maximum, measured from the controller to the last chassis.

Regardless of the number of drives on the daisy-chain bus (up to a maximum of four), only the last drive on the bus requires terminators. Excessive bus loading will occur if more than one drive on the bus is equipped with terminators.

1.3.2 FD1000A International System Configuration

An FD1000A configuration is identified by the FD1000A nameplate on the international chassis rear panel. Figures 1-6 through 1-8 show the cabling configurations for FD1000A systems that include the international chassis and the 2261695 power supply/interface board. These systems use the 15-pin remote connectors on the controller board and a shielded, multiple twisted-pair cable.

The standard remote cable length for the international chassis is 5 meters. Extension to 100 meters (328 ft) maximum is permitted.

The remote interface between the controller and the international chassis uses multiplexed control and status signals to reduce the number of wires in the interface cable. Since the remote interface uses differential line drivers and receivers, cable lengths up to 100 meters are possible. The power supply/interface board in the international chassis performs the status signal multiplexing and control signal demultiplexing necessary to adapt the drive units to the remote bus.

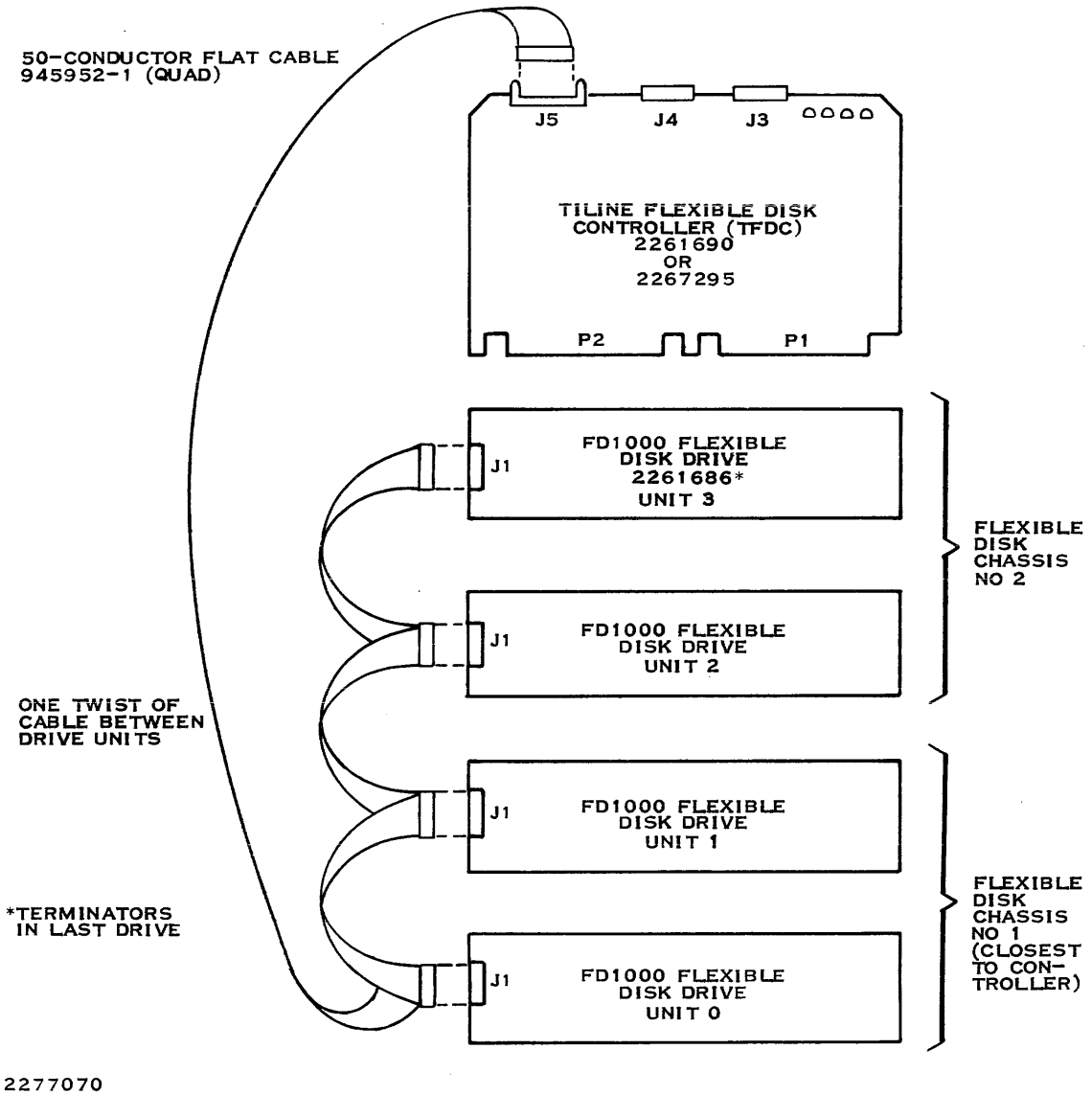

Figure 1-5. Domestic FD1000 System Configuration — Four Drives

One disk drive in each FD1000A international chassis must have terminators installed in order to properly terminate the intrachassis bus that connects the drive units to the power supply/interface board. This drive is the one on the left (as viewed from the front).

Drive unit number selection is determined by individual jumpers on the drive electronics boards. A jumper cap is set to the DS1, DS2, DS3, or DS4 position. No two jumpers may be set for the same drive select number. Note that the unit number selection code in the TFDC control words runs from 0-3, corresponding to jumper positions DS1-DS4 respectively.

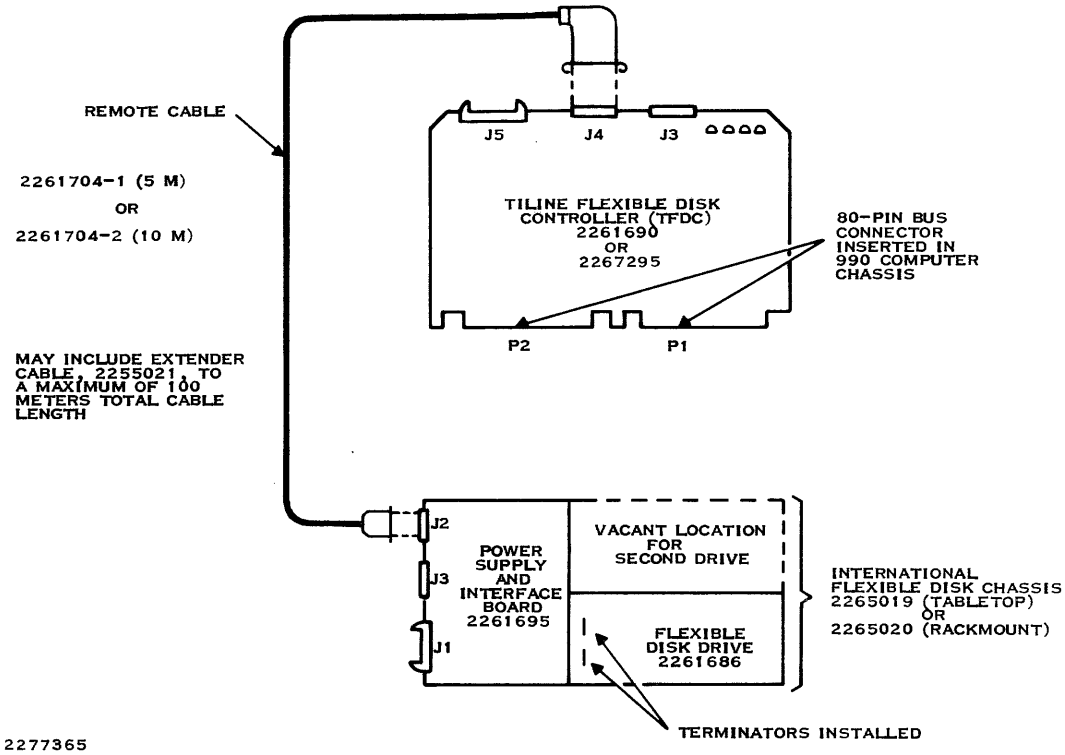

Figure 1-6. FD1000A International Configuration — Single Drive

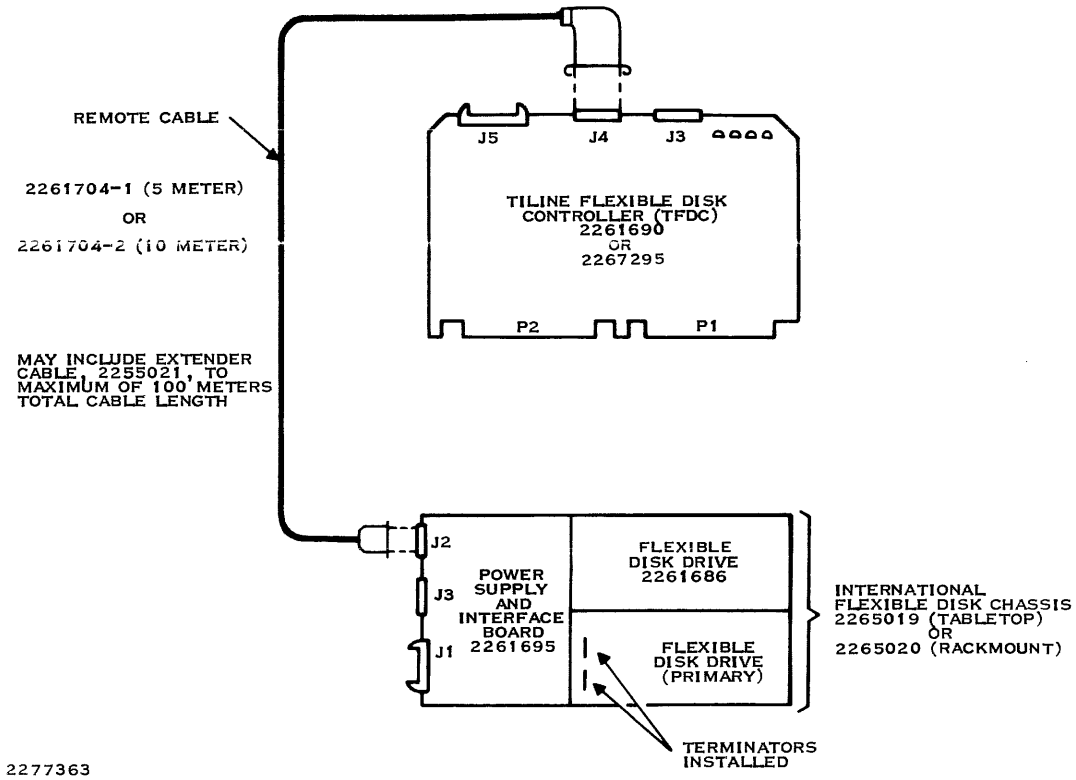

Figure 1-7. FD1000A International Configuration — Dual Drives

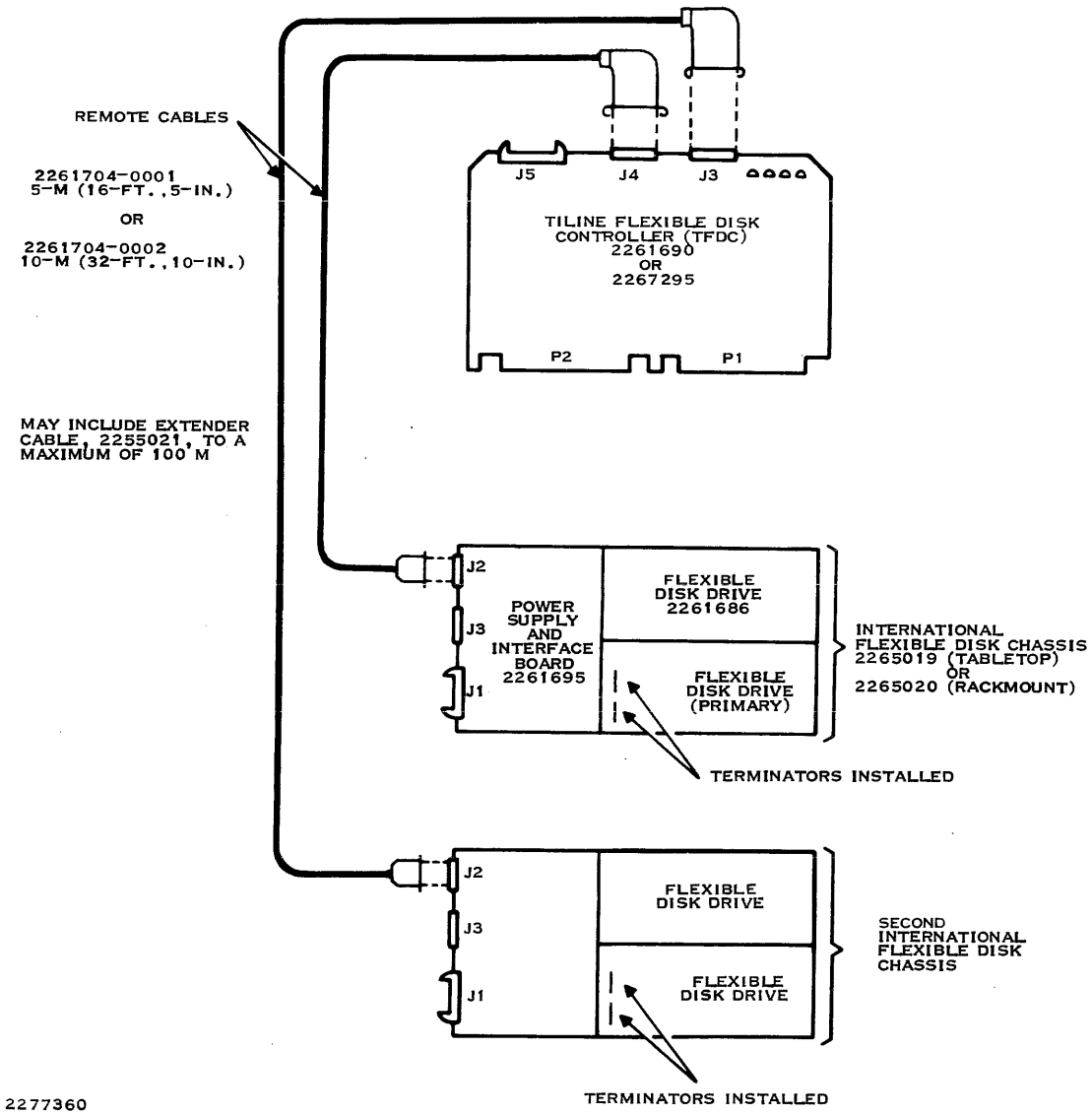

Figure 1-8. FD1000A International Configuration — Four Drives

1.3.3 FD1000B International System Configuration

An FD1000B configuration is identified by the FD1000B nameplate on the rear panel of the international chassis. Figures 1-9 through 1-11 show the cabling configurations for FD1000B systems that include the international chassis and the 2269977 buffered power supply/interface board. This is the newest version of the flexible disk system.

This system uses the 15-pin remote connectors on the controller board and a shielded, multiple twisted-pair cable.

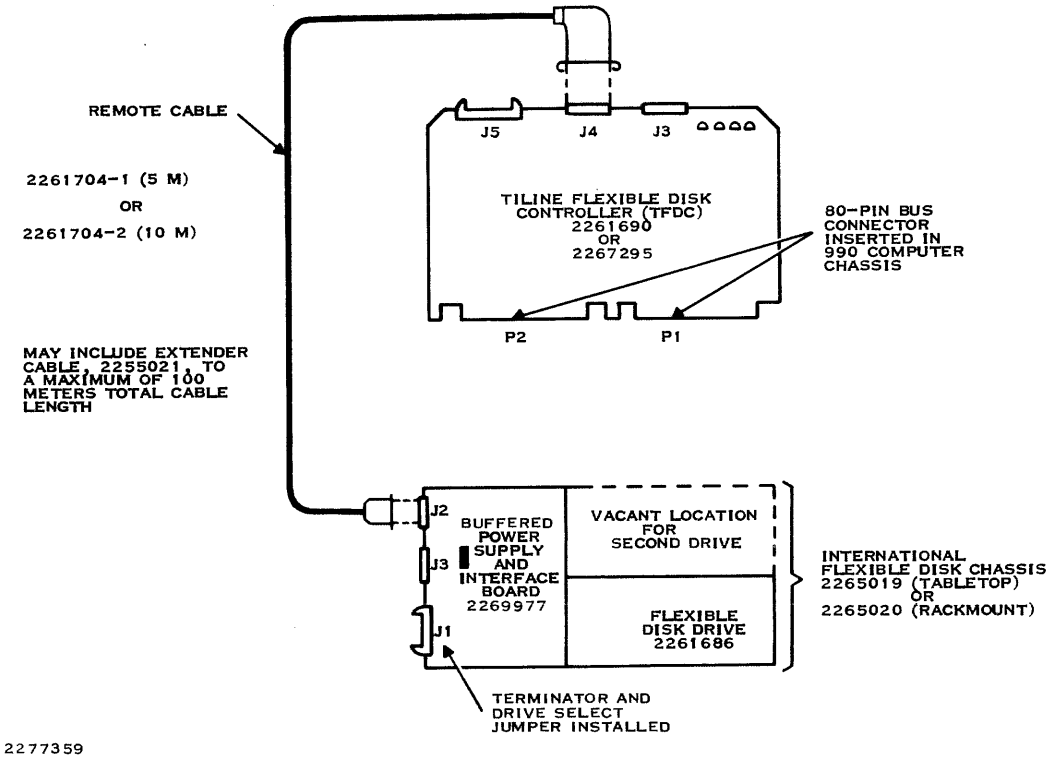

Figure 1-9. FD1000B International Configuration — Single Drive

The remote interface between the controller and the international chassis uses multiplexed control and status signals to reduce the number of wires in the interface cable. Since the remote interface uses differential line drivers and receivers, cable lengths up to 100 meters are possible. The buffered power supply/interface board in the international chassis performs the status signal multiplexing and control signal demultiplexing necessary to adapt the drive units to the remote bus.

The buffered power supply/interface board (2269977) must have a 972141-21 line terminator installed in order to properly terminate the intrachassis bus. This intrachassis bus connects the drive units to the buffered power supply/interface board. Terminators are *not* installed in any drive units.

Jumper caps on the drive electronics boards are always set to the DS1 position (left drive as viewed from front) or DS2 position (right drive). The actual drive unit select numbers are determined by two jumper caps on the buffered power supply/interface board:

Jumper Positions	Unit Select
E1-E2	DS1
E4-E5	DS2
E2-E3	DS3
E5-E6	DS4

Note that the unit selection code in the TFDC control words runs from 0-3, corresponding to DS1-DS4 respectively.

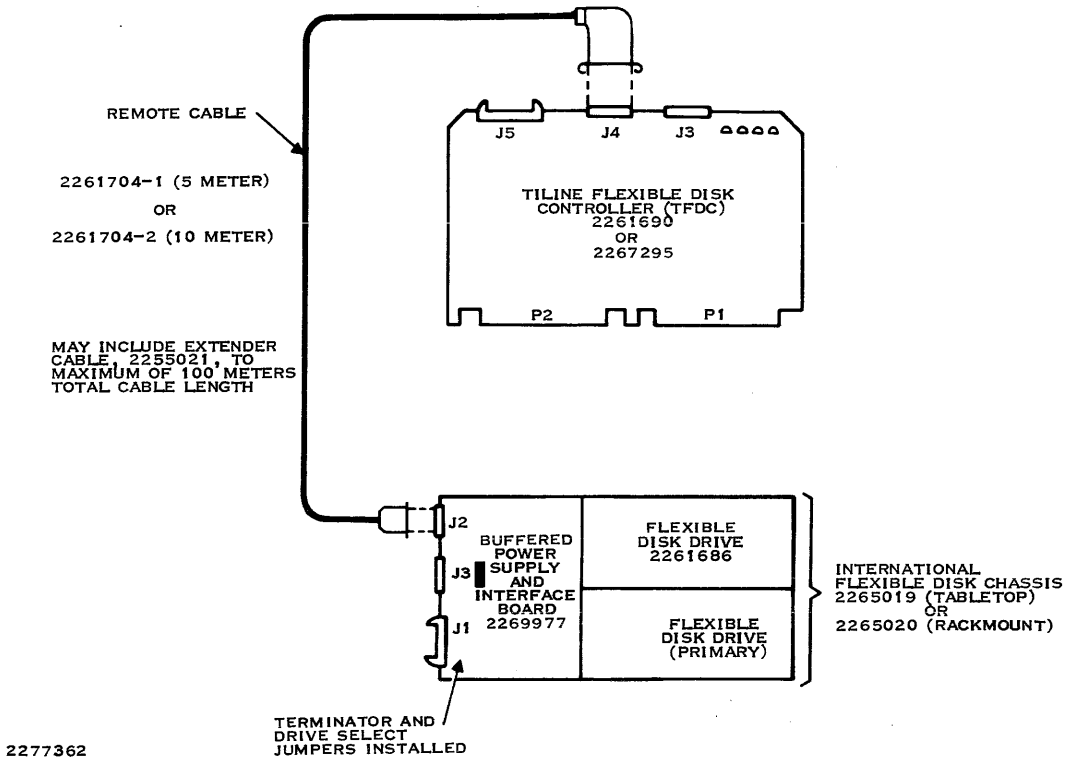

Figure 1-10. FD1000B International Configuration — Dual Drives

1.4 DISK CONTROLLER PHYSICAL CHARACTERISTICS

Figure 1-12 and Figure 1-13 show the multilayer (2261690) and fineline (2267295) versions of the TFDC board. The following description applies equally to both logic boards. Subsequent paragraphs describe differences in component layout. The 50-pin male connector (J5) at the top left edge of the TFDC circuit board mates with the local daisy-chain cable. Note that the ribbon cable and the on-board connector are not positively keyed. The molded arrowheads on the connector bodies must be aligned to assure that the cable is properly mated. The remote connectors, J3 and J4, are positively keyed by the shape of the connector body.

The TILINE base address for the disk controller board is determined by the setting of a five-section dual in-line package (DIP) switch at the lower left of the logic board. At system generation, the operating system software is provided with a base address for each TILINE controller. The operating system uses that base address any time a command (such as Read Data) is to be sent to the controller. If the address used by the operating system software does not agree with the setting of the on-board switches, the controller will not respond and a TILINE timeout error will be indicated by the CPU. If the FD1000 is the system disk and if the switches on the controller are incorrectly set, it will be impossible to load the operating system. Switch settings are described in Section 2 of this manual.

A set of light-emitting diode (LED) indicators on the upper right edge of the board provides a quick method of determining controller status. In general, these indications apply only to the internal operating state of the controller; they do not provide information about the condition of the drive units.

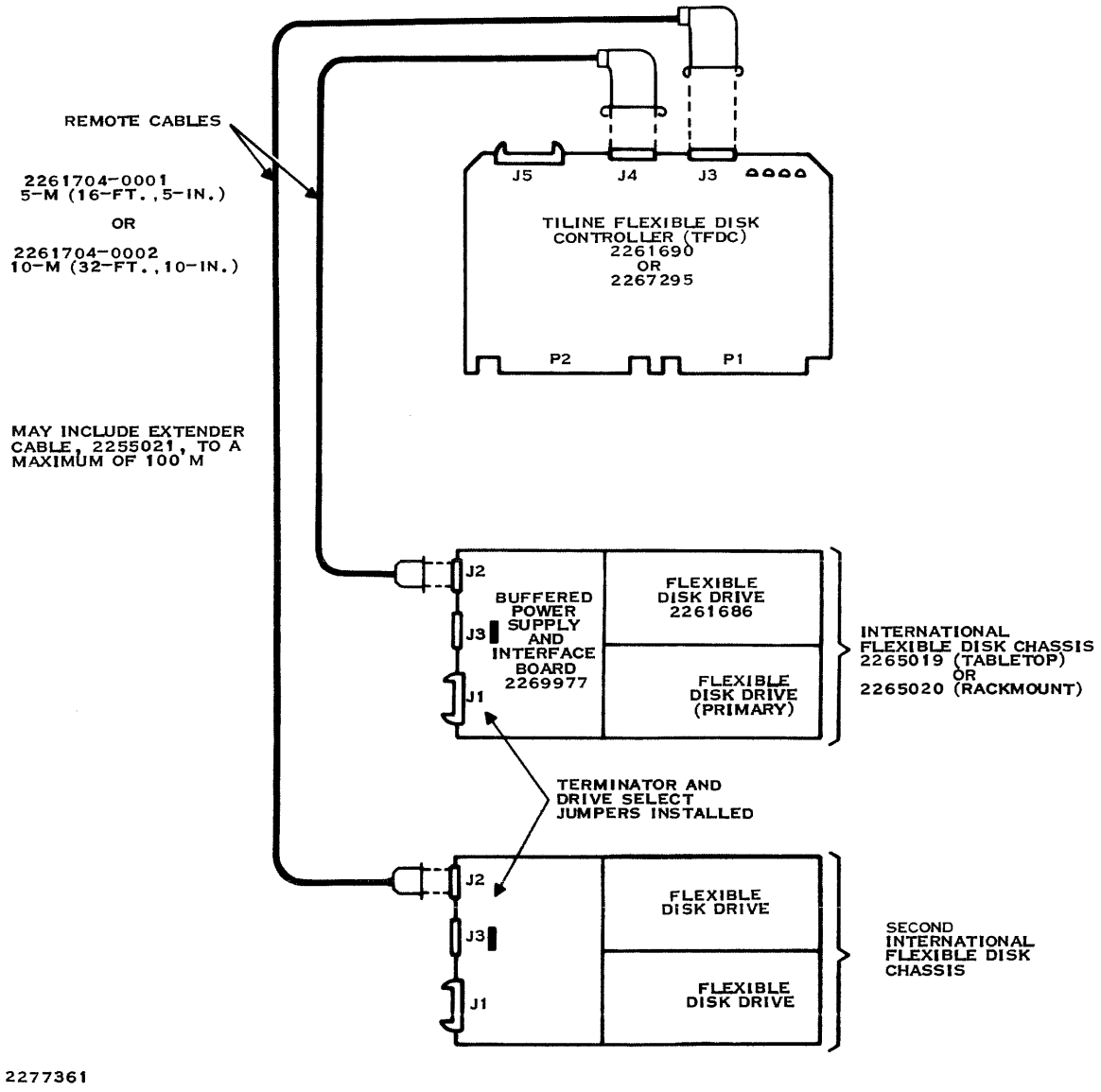

Figure 1-11. FD1000B International Configuration — Four Drives

The four LED indicators are arranged in a single row on the multilayer (2261690) board. On the fineline board (2267295), three indicators are arranged in one row, with the fourth indicator adjacent to the ejector tab. The left-to-right order on either board is FAULT (red), INT, BUSY, and CLOCK.

The red FAULT LED is turned on at the beginning of the controller self-test and remains on until cleared by successful completion of the test. This is a matter of one or two seconds. Failure of the self-test leaves the FAULT indicator illuminated and inhibits any operation that involves reading from or writing to the disk unit. An I/O reset or power-up reset initiates the self-test. If the self-test fails, the hardware configuration and/or the controller should be investigated.

The interrupt (INT) LED is used to display the state of the interrupt line from the disk controller to the 990 computer. When this indicator is lit (green), the controller has issued an interrupt, and the computer has not yet responded. Interrupts should be issued and answered so quickly that the eye cannot detect the indicator flash. If the indicator is brightly lit, an error has occurred, leaving the controller hung in the interrupt-active condition (typically due to improper software interrupt assignment).

The BUSY LED is used to tell when the controller is executing a command. When the light is out, the controller is not executing any commands and is cycling on its internal idle loop. When the controller is executing a command, the BUSY light will illuminate and stay on until the command is complete. The apparent brightness of this indicator is quite variable, depending on the type of operation being performed or the frequency of sequential operations.

The CLOCK indicator remains lit at all times except when the TILINE master access logic of the controller is controlling a TILINE data transfer. The transfer of the eight control words to the controller, or TILINE traffic not involving the controller, has no effect on this indicator.

Controller dc power requirements (from the 990 chassis power supply) are:

+5.0 ±0.1 Vdc at 4.4 A (max)
+12.0 ±0.1 Vdc at 0.1 A (max)
−5.0 ±0.05 Vdc at 0.01 A (max)

1.4.1 Component Layout — Multilayer TFDC Board (2261690)

Refer to the board photograph, Figure 1-12. Device locations on this board are based on a horizontal 100-mil grid (1000 mils = 1 inch) and 18 alphabetic rows in the vertical direction. The board is marked with a horizontal grid reference number every ten 100-mil increments (every inch) along the lower stiffener. The rows are marked with alphabetic characters along the left and right edges of the board.

Devices are identified by a one or two character device type code and the alphanumeric device location. The device codes are:

- U Integrated circuit (IC) network
- C Capacitor
- R Resistor
- L Inductor
- CR Diode
- Y Crystal
- VR Voltage regulator
- X Socket for removable device

Devices are located by the alphabetic row and by the 100-mil grid coordinate at the left edge of the device. For example, UB062 is an IC located in row B with the left edge two 100-mil increments to the right of the 060 reference label.

The coordinate layout is shown along the bottom and right edges of the board photograph.

1.4.2 Component Layout — Fineline TFDC Board (2267295)

Refer to the board photograph, Figure 1-13. Device locations on this board are based on a 100-mil grid (1000 mils = 1 inch) in both the horizontal and vertical directions. The horizontal grid is represented by a three-digit number, starting with 000 at the left edge of the green overlay and continuing to 139 at the right edge of the overlay.

The vertical 100-mil grid is represented by two alphabetic characters. The first alphabetic character represents an increment of one inch (1000 mils), measured from the lower board stiffener. This character lies in the range of A (bottom) to K, limited by the board height. The second alphabetic character represents an increment of 0.1 inch (100 mils). This character ranges from A (0 mils) to J (900 mils).

Devices are identified by a one or two character device type code and the alphanumeric device location. The device codes are:

- U Integrated circuit (IC) network
- C Capacitor
- R Resistor
- L Inductor
- CR Diode
- Y Crystal
- K Voltage regulator
- X Socket for removable device

Devices are located by the alphabetic row and by the 100-mil grid coordinate at the left edge of the device. For integrated circuits, this left edge is the pin 1 position of the device. As an example, UDF029 is an integrated circuit (U) located with pin 1 in row DF, at the 029 horizontal reference label.

The coordinate layout is shown along the bottom and right edges of the board photograph.

Notice that the columns of integrated circuits are arranged with pin 1 positions at the 003, 016, 029, 043, 058,... 129 horizontal grid positions. Coordinates are marked as needed on the face of the board. Each major row or column for IC location is marked. Passive components are marked with an R, L, C, CR, or Y.

The TMS 9900 microprocessor, TMS 9901 peripheral interface adapter, and all read-only memory (ROM) devices are socket-mounted. All other IC devices are soldered to eyelets in the board.

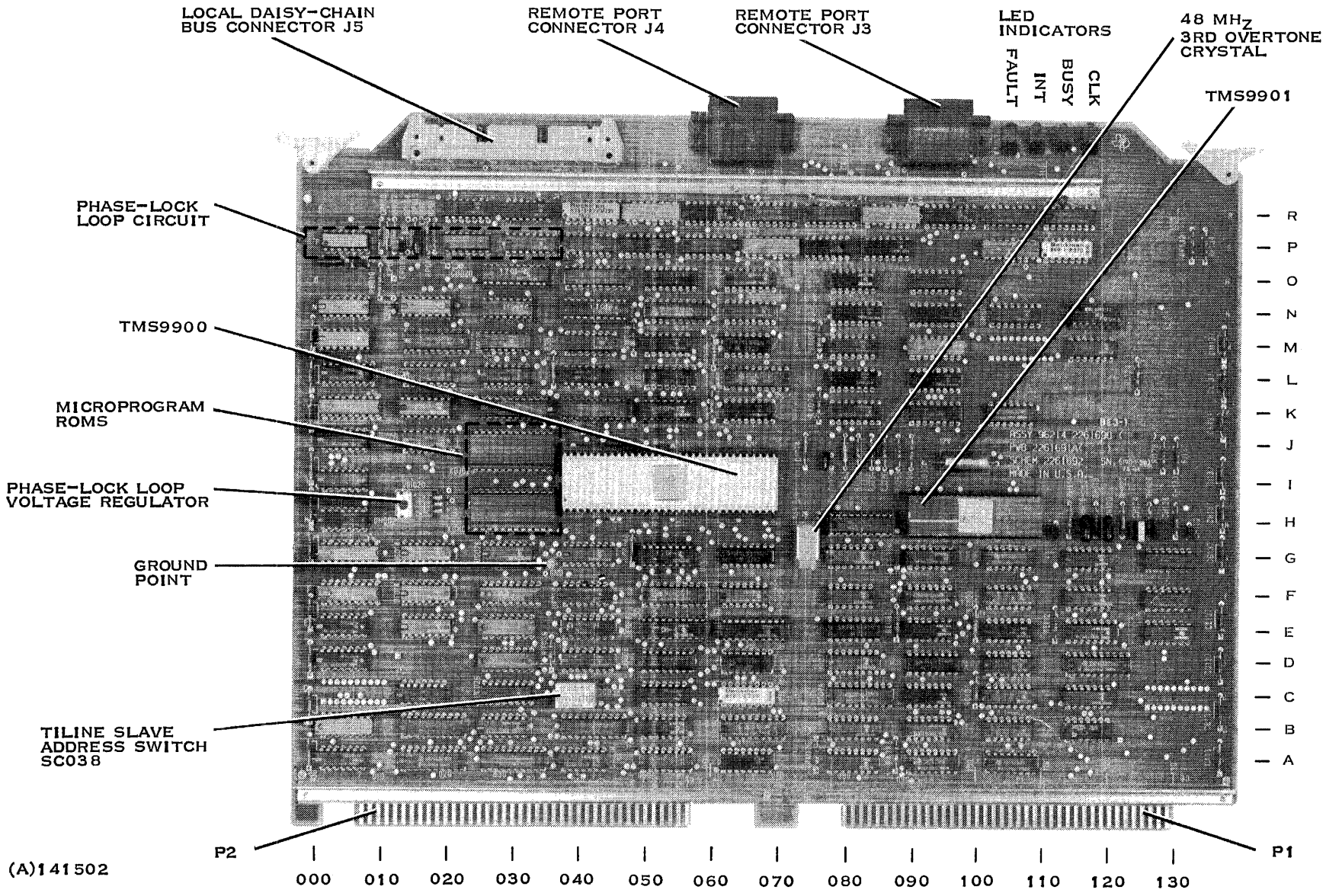

Figure 1-12. TILINE Flexible Disk Controller (2261690)

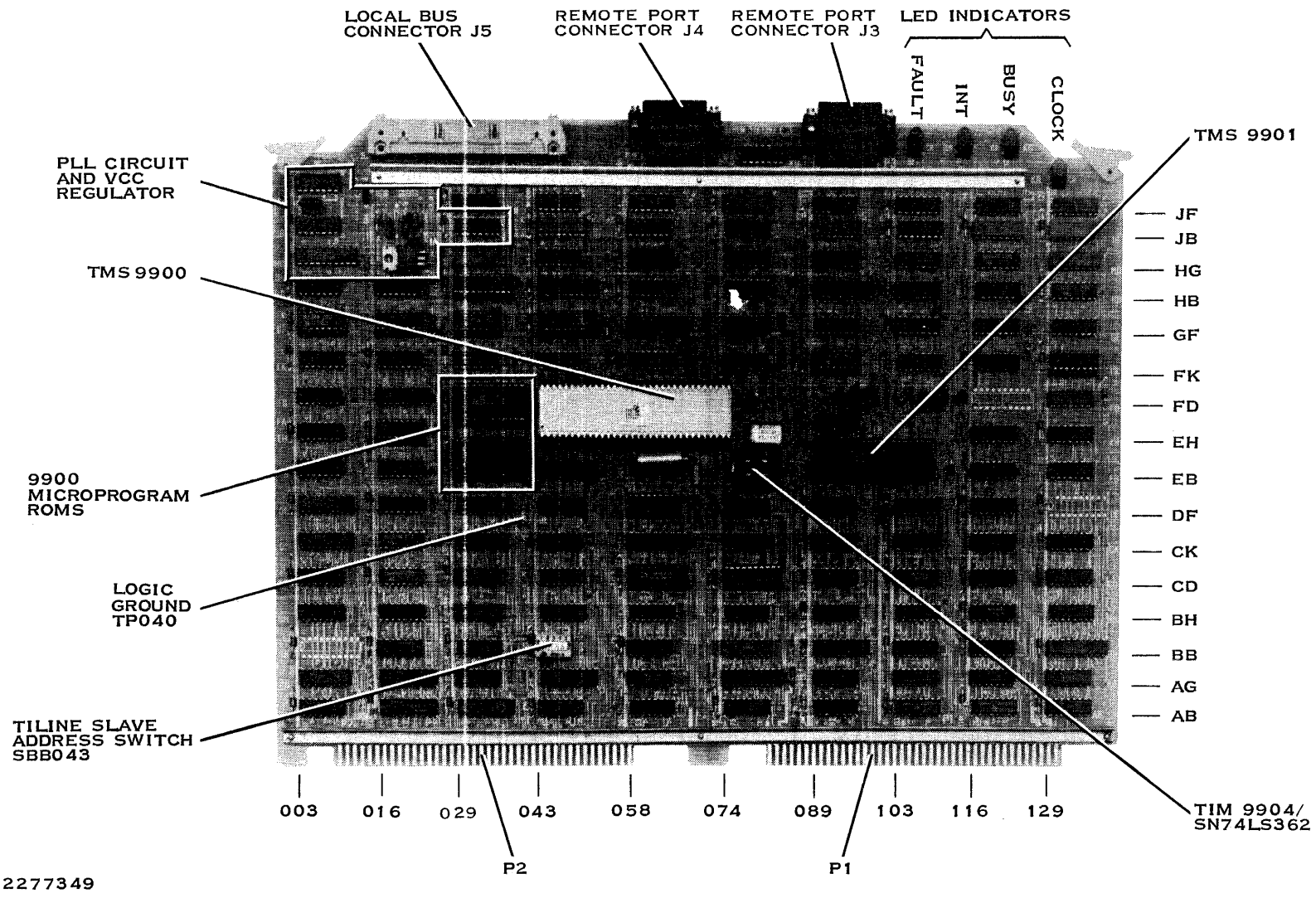

Figure 1-13. TILINE Flexible Disk Controller (Fineline — 2267295)

1.5 FD1000 DOMESTIC CHASSIS PHYSICAL CHARACTERISTICS

Figure 1-14 shows the rackmount version of the domestic chassis. Two large openings in the front panel allow diskettes to be installed in the drive units. The small door release buttons allow the operator to remove diskettes that are not currently active. A door lock on the drive prevents opening the door while the drive is in use.

A red POWER indicator in the front panel lights when ac operating power is applied to the chassis.

The ON/OFF toggle switch for ac power and the ac fuseholder are located on the rear lip of the chassis. The dc power supply is a vendor item and is not described in this manual.

Signal connections to the drives are made directly to the drive I/O connectors by the flat daisy-chain cable that runs from the controller to all drives.

Domestic chassis ac requirements are shown in Table 1-1.

Table 1-1. Domestic Chassis Ac Requirements

100/115 Vac ± 10% 50/60 Hz ± 0.5Hz	0.4 A running, per drive unit 0.8 A starting, per drive unit 0.4 A dc power supply
or	
230 Vac ± 10% 50 Hz ± 0.5 Hz	0.3 A running, per drive unit 0.6 A starting, per drive unit 0.2 A dc power supply

1.6 FD1000A/B INTERNATIONAL CHASSIS PHYSICAL CHARACTERISTICS

Figure 1-15 shows the rackmount version of the international chassis with the cover removed. The drives, transformer, power supply/interface board, ac power module, and fan are mounted on a removable adapter assembly.

The red POWER indicator is centered in the lower part of the front panel. Two snap-in, disposable, air-intake filters occupy cutouts flanking the POWER indicator. Symmetrical cutouts in the front panel allow access to the two drive units. The large openings allow room for the diskette installation door, and the small cutouts are for the door release buttons.

The ac power module mounts behind a cutout at the right side (as viewed from the rear) of the adapter rear panel. The power module includes the ac power ON/OFF switch, ac line fuse, and a three-prong recessed male connector for the ac power cord. The ac power ON/OFF switch is also labeled 1 for ON and 0 for OFF. This conforms to international requirements for power switch labeling. The fuseholder cap requires a flat-bladed screwdriver for removal, also in conformance with international requirements.

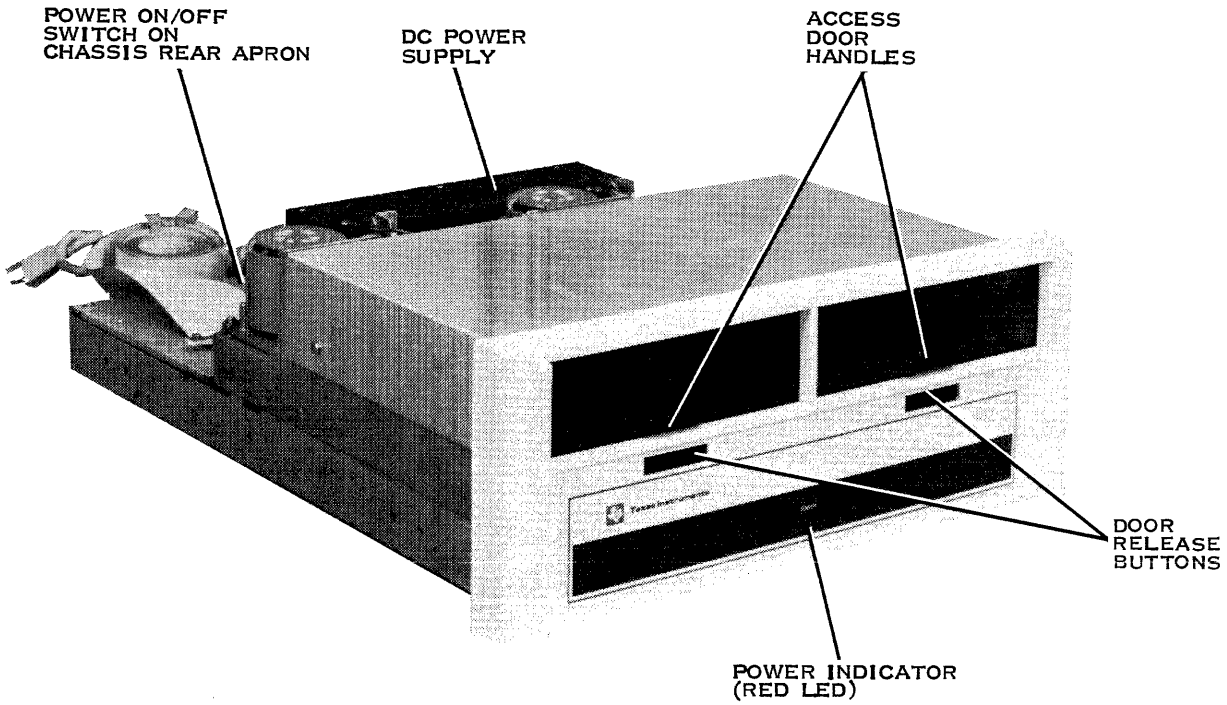

Figure 1-14. FD1000 Domestic Chassis, Front View

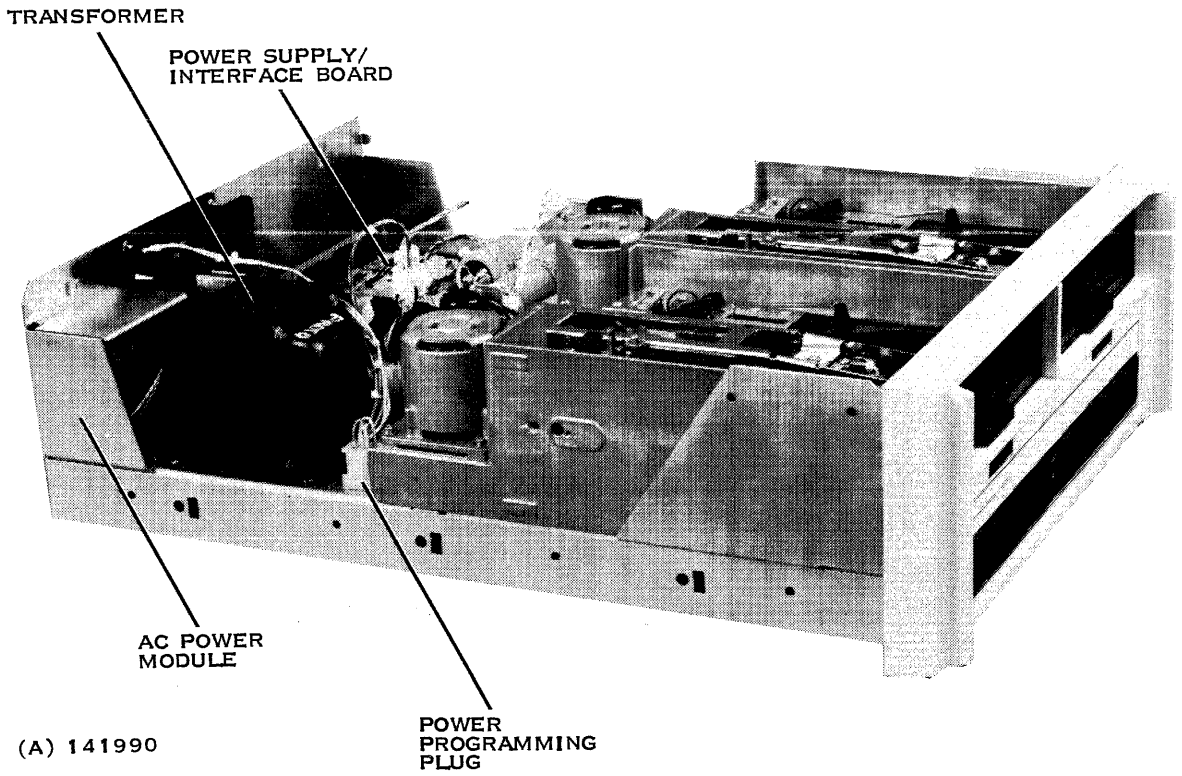

Figure 1-15. International Chassis, Cover Removed

The power supply/interface board occupies the left rear of the adapter. Heat sinks for the series regulator transistors are aligned with airflow through the fan. The power supply/interface board is mounted on insulating standoff posts by six machine screws. Signal connectors, power connectors, and test points are accessible with the cover removed. The three chassis input/output signal connectors are also accessible through a slot in the chassis adapter rear panel. The connector that is used in FD1000A and FD1000B systems is the 15-pin, D-type connector at the left end of the slot (viewed from the rear).

The power programming plug next to the transformer contains wiring that selects the proper combination of transformer taps to supply 115 volts ac to the ac input of the power supply/interface board.

The tabletop version of the international chassis has a slightly different cover and a set of molded side panels. Four nonskid feet are attached to the chassis bottom for tabletop mounting.

CAUTION

Do not stack tabletop chassis units or place heavy objects on the cover of a tabletop chassis. The molded side panels on this chassis are for trim and for sealing against dust. They are not rigid structural members.

International chassis ac power requirements are shown in Table 1-2.

Table 1-2. International Chassis Ac Power Requirements

100 Vac + 10% 50/60 Hz ± 0.5 Hz	
	0. 4 A running, per drive unit 0. 8 A starting, per drive unit 0. 6 A dc power supply and fan
or	
120 VAC ± 10% 60 Hz ± 0.5 Hz	
220 Vac ± 10% 50 Hz ± 0.5 Hz	
	0. 3 A running, per drive unit 0. 6 A starting, per drive unit 0. 3 A dc power supply and fan
or	
240 Vac ± 10% 50 Hz ± 0.5 Hz	

1.6.1 Power Supply/Interface Board Physical Description

There are two versions of the power supply/interface board, the International Chassis Power Supply (2261695) and the Buffered International Chassis Power Supply (2269977). These two boards are shown in Figure 1-16 and Figure 1-17, respectively. This description applies to both versions except where otherwise noted. Subsequent paragraphs describe the differences in component layout.

Component identifiers are silk-screened onto the boards, so coordinate grids for parts location are not provided.

A pair of large heat sinks dissipate the heat generated within the +24-volt dc and +5-volt dc series regulator transistors. A smaller heat sink for the rectifier bridges is located at the lower right corner of the board.

Three signal input/output connectors are located on the lower left corner of the board. The 50-pin flat ribbon connector is a parallel interface provided for FD800 systems, which are also available in the international chassis.

The 25-pin connector is provided for communication with the CRU-based flexible disk controller in DS990 Model 1 and 771 systems. The CRU-based controller is not described in this manual.

The 15-pin connector at the lower left corner is the remote interface connector for use with the TFDC. Logic circuitry located primarily in the lower left quadrant performs status and control signal multiplexing/demultiplexing for the remote interface.

The two pendant cables at the top of the photograph connect the drive electronics boards to an intrachassis local (parallel) bus. This bus carries all drive input and output signals.

Plugs P7, P8, P9, and P10 are three-pin connectors that are connected in parallel. One is connected to the 115-volt ac output of the power transformer and the others are used to power the exhaust fan and the spindle motors of the drive units. The selection of connectors is based on convenience in cable routing. Pin assignments for the high-voltage ac connectors are:

Voltage	Input/Output Connector (P7, P8, P9, P10) Pins
115 Vac	Pin 1 - Pin 3
Chassis Ground	Pin 2

Low voltage ac power from the power transformer is supplied through P6. This low voltage ac power is rectified to supply the dc outputs. The ac inputs are:

Voltage	Input Connector (P6) Pins
7.5 Vac	Pin 1 - Pin 2
26.5 Vac	Pin 3 - Pin 4
15.0 Vac	Pin 5 - Pin 6

The dc power output pin connections are shown in Table 1-3.

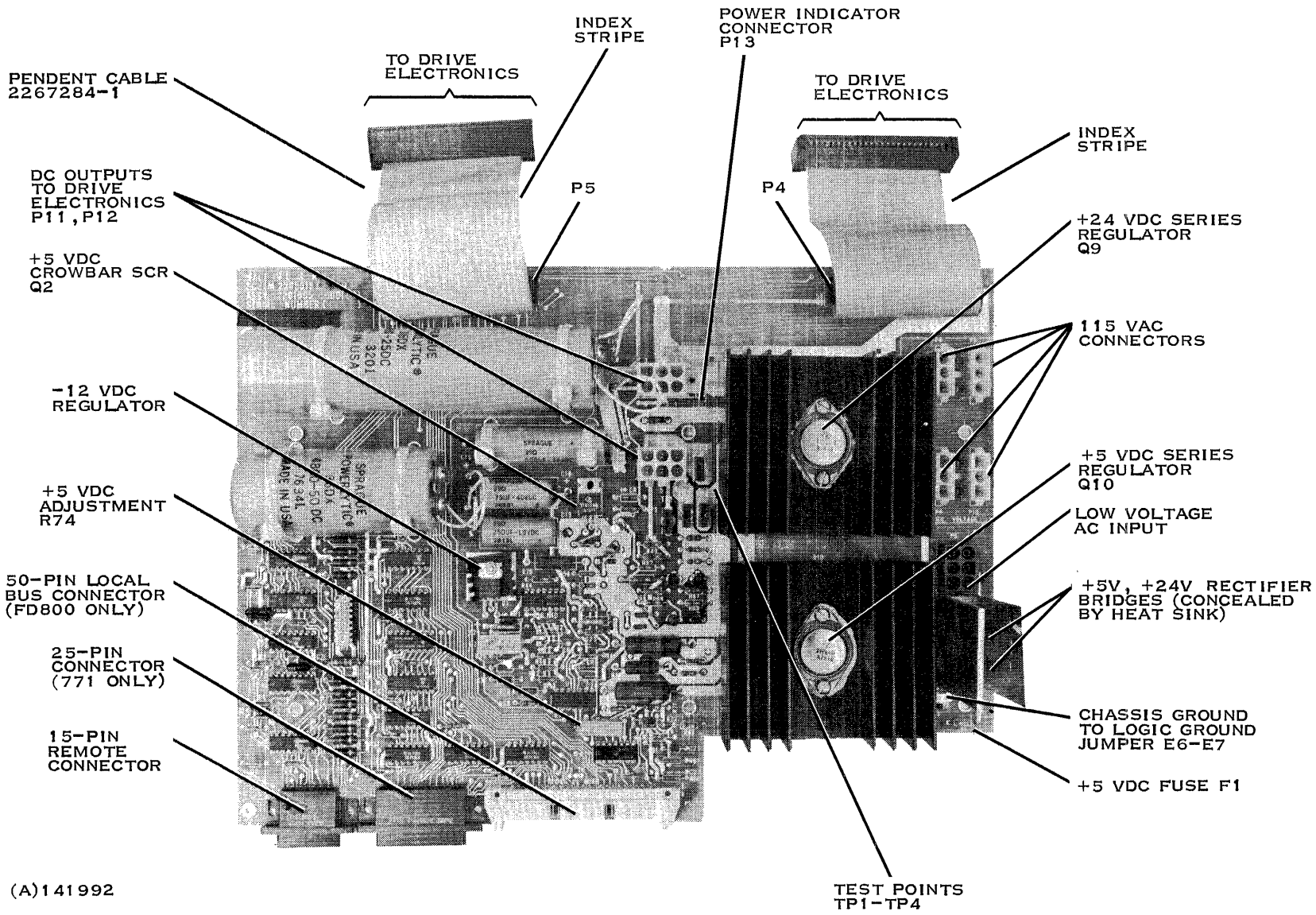

Figure 1-16. Power Supply/Interface Board (2261695)

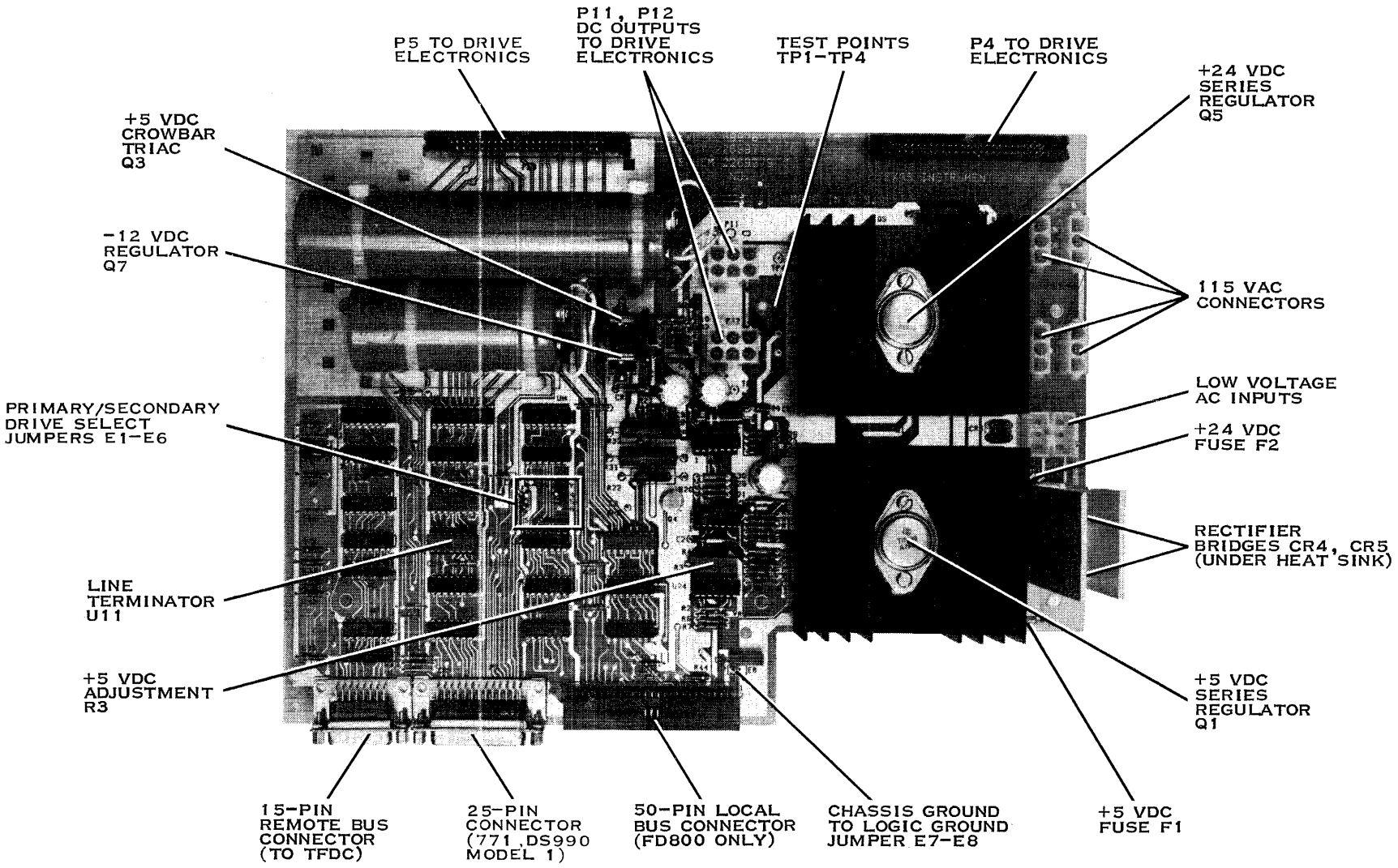

Figure 1-17. Power Supply/Interface Board (2269977)

Table 1-3. International Power Supply Output Connections

Voltage	Current (max)	Test Point	Output Connector (P11, P12) Pin No.
+ 5 Vdc ±2.5%	4 A	TP2	Pin 5
+24 Vdc ±5%	2.2 A	TP4	Pin 1
−12 Vdc ±6%	0.5 A*	TP1	Pin 4
Logic ground		TP3	Pins 2, 3, 6

Note:

* The −12 Vdc output is not required by the Qume DT/8 drive.

1.6.1.1 Component Layout of the 2261695 Power Supply/Interface Board. As shown in the board photographs, the differences in board layout are very slight. This version does not include any provision for on-board line termination or drive unit number selection.

NOTE

DS990 Model 1 systems equipped with this version must also include a piggyback DS1 Interface (2271670). The piggyback board is not required for use with the TFDC. If the piggyback board is installed, terminators must be removed from the drive unit. Termination at the end of the cable is provided by a 972141-21 terminator on the piggyback board (U3).

Also, drive unit selection jumpers in the drives must be set to DS1 (left unit, viewed from front) and DS2 (right unit). Jumpers E1-E2 and E4-E5 on the piggyback board select DS1 and DS2 respectively. Jumpers E2-E3 and E5-E6 select DS3 and DS4 respectively.

1.6.1.2 Component Layout of the 2269977 Buffered Power Supply/Interface Board. The buffered version of the power supply/interface board provides the following features not incorporated in the original design:

- Additional noise immunity via a rank of CMOS buffers and TTL drivers
- Drive unit number selection via on-board jumpers
- Signal line termination via on-board terminator
- Power supply redesign for improved producibility and reduced parts count

Although the layouts of the boards are similar, the component designators differ. For example, the series regulator transistors are Q5 and Q1 on the buffered board as opposed to Q9 and Q10 on the original board. Physical locations of these transistors are unchanged.

Line termination is provided by a 972141-21 resistor network installed at U11. This terminator is always installed for use with the TFDC and the remote interface. In DS990 Model 1 systems or FD800 systems, the terminator is only installed in the chassis at the end of the flat cable.

Drive unit selection jumpers in the drive units are always set to DS1 in the left drive (viewed from front) and DS2 in the right drive. Final drive unit number selection is determined by jumpers on the power supply:

Chassis	Jumpers	Unit No
1	E1-E2	DS1
	E4-E5	DS2
2	E2-E3	DS3
	E5-E6	DS4

Line termination and drive unit number selection on the power supply/interface board allow changes in configuration without requiring access to the drive electronics.

1.7 PROGRAMMING THE DISK CONTROLLER

Texas Instruments disk-based operating systems contain device service routines that manage the interaction between the Model 990 Computer and the Model FD1000 Flexible Disk System. The operating system presents the programmer with a standard set of displays and data that are more characteristic of the operating system than of the disk system hardware. Users who need this type of information should refer to the operating system documentation.

The programming information presented here is useful to those who wish to control disk system operations from the Model 990 Programmer Panel and to anyone who needs to understand the operating concepts of the disk system.

The Model 990 Computer prepares the disk controller by writing a group of eight control words, W0-W7, over the TILINE to the disk controller. These control words specify the operation to be performed, precondition the controller, and supply parameters to the controller. These parameters include the disk logical unit number, the number of words to be read or written, track, head and starting sector addresses, and the starting address of the assigned 990 memory buffer area.

The last control word, W7, initiates disk controller operations. The disk controller operates under control of an internal program to perform the specified operation. The controller rejects any attempt to write or read back control words while an operation is in progress.

For a disk write operation, the controller TILINE master logic acquires control of the bus and reads data from the specified area of 990 memory. Other controller logic converts the data to serial form and transmits it to the disk drive for recording. For a disk read operation, the controller reads data back from the selected diskette, checks data integrity, and converts the data back to 16-bit parallel form. The controller TILINE master logic acquires control of the TILINE and transfers the data to 990 memory.

The control words initially supplied to the controller are modified during the course of the operation. At the completion of the operation, the control words contain status information that may be read back by the 990 computer to determine if the operation completed normally. If the operation did not complete normally, the status words identify the errors detected during the attempted operation.

1.7.1 Control Word Addresses

Standard conventions built into the hardware and software of the Model 990 Computer reserve CPU byte addresses $F800_{16}$ to $FBFD_{16}$ for control and status communication with TILINE peripheral controllers, and reserves $FBFE_{16}$ as the TILINE timeout test address. This range is called the TILINE peripheral control space (TPCS). Addresses in this range may be mapped by the processor hardware to TILINE addresses in the range $FFC00_{16}$ to $FFDFF_{16}$. This mapping requires the 990 processor to be operating in map file 0. The TPCS can also be addressed through alternate map files if the mapping bias value is chosen to yield the correct TILINE address.

The disk controller is assigned a block of eight consecutive TILINE word addresses. These addresses run from a base address to base address +7 word addresses. The base address is dedicated to control and status word W0, base address +1 is dedicated to W1, up through base address +7 is dedicated to W7.

The base address is selected by a five-section switch on the disk controller board. This allows for 32 different base addresses in the range F800 to $F9FE_{16}$. Base address selection must be coordinated with the operating system software. Texas Instruments standard operating system software includes specific operator entries at system generation to inform the operating system of the TFDC base address. Figure 2-15 in Section 2 supplies the details of base address switch setting.

Any 990 instruction that reads or modifies memory can be used to communicate with the controller when the proper CPU byte address is used. One simple way to send a block of control words to the controller is to store the eight control words at sequential addresses in 990 memory. Then, an auto-incrementing move (MOV) instruction should be used to transfer the control words to the disk controller. The programmer panel may be used for manual entry via the MA ENTER, MD, MDE, and MAI controls.

1.7.2 Command Initiation

The usual procedure followed in programming the controller is to initially read status word W7 from the controller and then to check W7, bit 0. If W7, bit 0 is a one (controller idle), the remaining status bits are valid and may be checked prior to transmitting the control words.

There are seven basic controller commands: Store Registers, Write Format, Read Data, Write Data, Read ID, Seek, and Restore. An additional eight extended mode commands are provided for less common operations and for controller diagnostics. All of these commands are described in more detail in this section (paragraphs 1.9 through 1.10).

With the exception that W7 must be last, the order in which the control words are transmitted to the TFDC is not critical. W7 contains the interrupt enable/disable bit that determines if an interrupt is to be generated upon completion, it also contains the idle/busy bit that initiates the controller operation when forced to 0.

Any attempt to send a control word to the TFDC after it has been forced to the busy state will be aborted by the controller, which will issue an immediate TILINE terminate.

An attempt to read a status word from a busy controller will not result in a TILINE error. However, the word returned by the controller will be a simulated W7 word in which bit 0 is a zero (busy) and bits 1-15 are meaningless. This feature allows the controller to be polled for idle/busy status without interference to any on-going controller operations.

With one important exception, transmitting a new set of control words to the TFDC wipes out the status words from the previous operation. The disk status fields of word W0 are controlled by the selected flexible disk drive and cannot be modified by overwriting with a new control word. The controller ignores those fields of the new control word and accepts the word normally, writing over the attention mask bits (only).

1.7.3 Command Completion Without Interrupts

To determine command completion or controller availability in a polled system, it is necessary to periodically read status word W7 and check bit 0 for idle status. If the controller is idle (W7, bit 0 = 1), the remaining bits of W7 may be checked. W7, bit 1 is one for a normally completed operation, and W7, bit 2 is one if an error was detected during the operation. The other status words may be read back to get more detailed status information.

Normally, a programmer would initiate a timing loop when the controller operation was initiated and would check the idle bit at timer expiration. If the idle bit is still zero, the timer may be restarted and the sequence repeated for a preselected number of attempts. This method involves a considerably larger amount of programming overhead than the interrupt-driven approach.

1.7.4 Command Completion with Interrupts

In order to have the controller issue an interrupt to the 990 processor upon completion, interrupt enable (W7, bit 3) must be set when the operation is initiated. However, command completion is not the only condition that may initiate a 990 interrupt from the TFDC. It is the programmer's responsibility to determine the cause of the interrupt. The possible interrupt conditions are:

- Interrupt on normal completion
- Interrupt on error termination
- Attention interrupt on completion of drive Seek or Restore.

1.8 TFDC CONTROL AND STATUS WORD FORMATS

The following paragraphs describe each of the control and status words. These descriptions are based on Figure 1-18.

1.8.1 Word 0 — Drive Status

Word 0 is used by the programmer to enable/inhibit the attention interrupts, to determine which of the possible drives initiated an attention interrupt, and to determine the status of the selected drive.

Bits 0-3 and bit 5 are controlled by the status of the selected drive and are not modified when a new word 0 is written to the controller. These bits may be changed as a result of performing a drive operation or selecting a different drive. Bits 8-11 are controlled by drives 1-4, respectively, regardless of which drive is currently selected.

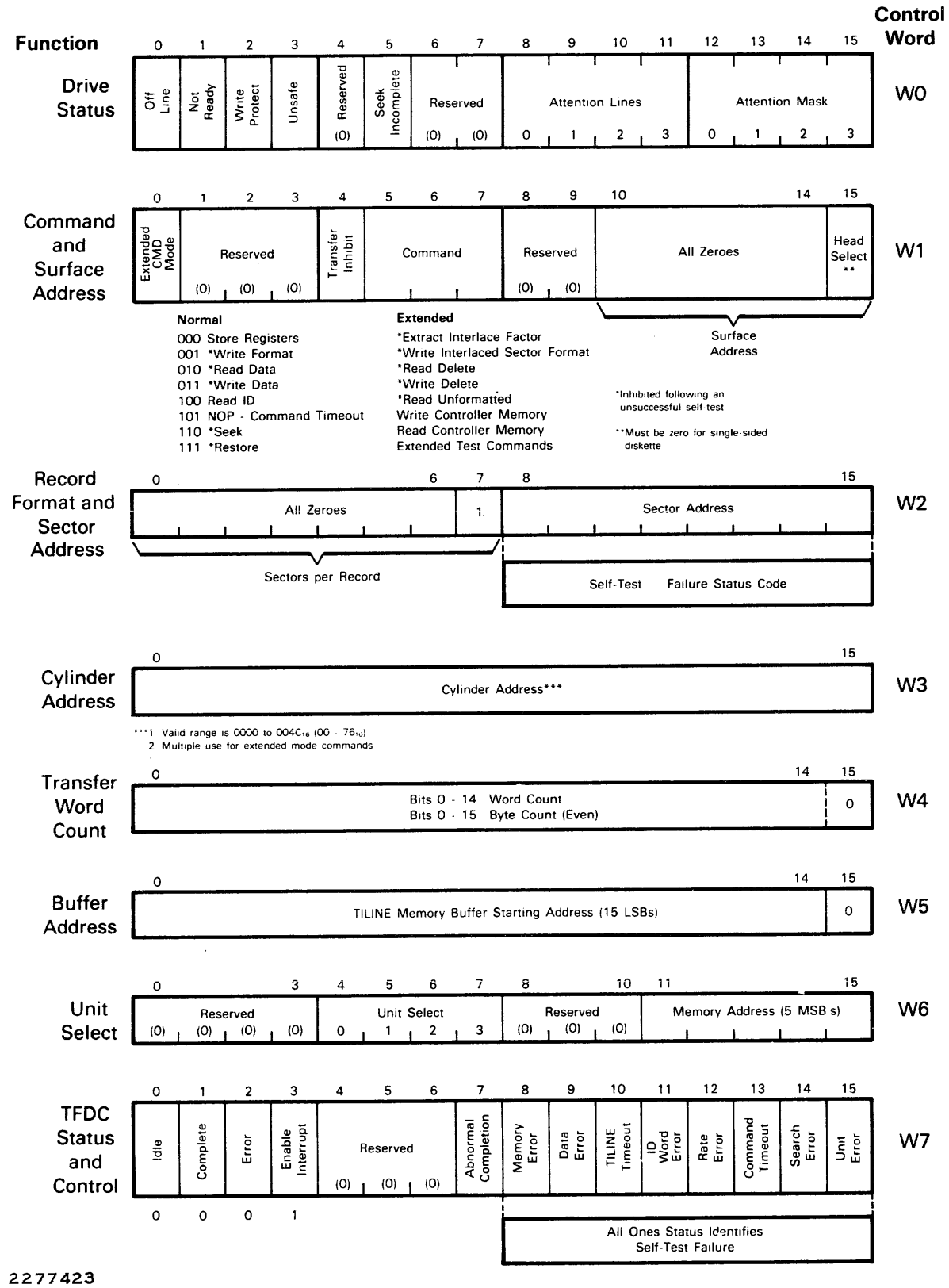

Figure 1-18. TFDC Control and Status Word Formats

1.8.1.1 Off-line — W0, Bit 0. The Off-line bit = 1 indicates that the selected unit is not available for operation due to one or more of the following reasons:

- Invalid unit number
- Diskette not installed
- Door not latched
- Drive not powered or not cabled to controller
- Index pulses not sensed - indicates a faulty drive, faulty diskette, or an incorrectly installed diskette.

During a power-down state, off-line and not ready will both be reported. Upon power-up, off-line should clear itself within two revolutions.

1.8.1.2 Not Ready — W0, Bit 1. This bit is 1 whenever the selected drive is off-line (W0, bit 0) or is in the process of performing a Seek or Restore operation.

1.8.1.3 Write Protect — W0, Bit 2. This bit is set to 1 if the diskette installed in the selected drive is write protected. Data cannot be recorded or modified on a write-protected diskette. Write protection is determined by physical means on the diskette. A notch on the outer edge of the diskette write protects the diskette. An optical sensor detects the presence or absence of the notch. If the notch is present, the drive write electronics are inhibited and a write protect indication is sent to the controller. Write protection may be defeated by placing an opaque tab over the write protect notch. This tab must be in place to format a diskette or to record any type of data on the diskette.

1.8.1.4 Unsafe — W0, Bit 3. This bit will be set to 1 if a command is issued for a drive that has not been previously identified to the software by a Store Registers command. It will also be generated if there has been some parameter change since the last Store Registers command. For example, a diskette change or a power-down cycle will result in unsafe status the next time the drive is selected. A Store Registers or Restore command clears unsafe status.

1.8.1.5 Seek Incomplete — W0, Bit 5. Seek incomplete indicates that the head carriage has failed to locate the specified cylinder. For example, if the cylinder address in W3 is out of range (greater than $4C_{16}$), the operation fails and seek incomplete status is reported. If a Restore operation has not been performed since the last power cycle or diskette change, an attempt to read, to write, or to seek on that drive results in seek incomplete status.

The Restore command is supposed to move the head carriage away from the spindle, step by step, until the track 00 signal becomes active. If track 00 is not sensed within 80 steps, seek incomplete is reported and the operation fails.

Seek incomplete results if the ID words read from the diskette disagree with the cylinder number that the controller was commanded to locate.

Some seek incomplete errors may be due to an error in the controller track counter. Such errors are unlikely if the self-test executes with no errors. These errors may be cleared by a Restore operation and a retry. There is also a slight possibility that a diskette formatted by a miscalibrated drive might be causing seek incomplete status. IBM 3740 format diskettes with bad tracks may cause the controller to exceed the allowed number of retries to find the cylinder. This type of error also results in a seek incomplete indication.

Seek incomplete is also reported if the heads reach the end of the last recording surface on the diskette but the transfer word count has not decremented to zero.

1.8.1.6 Attention Lines (0-3) — W0, Bits 8-11. The Seek and Restore commands initiate relatively slow electromechanical operations.

In order to speed up system throughput, overlapped, independent Seek and Restore capabilities are included. The attention lines (combined with the interrupt mask of bits 12-15) provide a means of notifying the 990 processor that the operation has completed.

One attention line is dedicated to each drive. The attention line for a drive is held high unless the drive is performing a Seek or Restore operation. The line returns high upon completion of the operation.

The Seek or Restore, once initiated, proceeds independently of other controller or 990 processor operations. Read, write, or other operations may proceed on any drive except those that are occupied with Seek or Restore.

Two methods are available for the 990 processor to determine that a Seek or Restore operation has completed. The first method is polling. The second method involves use of an interrupt. If polling is used, the programmer sets up a timer and initiates it when command word W7 is sent to the controller. When the timer expires, the program should read W7 to make sure the controller is idle and should then read W0 to check the attention line. If the attention line is still low, the timer should restart and repeat for some predetermined number of polling cycles. The polling cycle could also check the drive not ready bit (W0, bit 1).

Use of the attention interrupt to determine Seek/Restore completion is described with the attention mask in the next paragraph.

1.8.1.7 Attention Mask (0-3) — W0, Bits 12-15. Bits 12-15 form a position-coded attention interrupt mask. An interrupt to the 990 processor will be generated if the attention mask bit and the corresponding attention line are both set (ones) and the controller is idle.

To detect completion of a Seek or Restore operation with an interrupt, the programmer should set the attention mask bit corresponding to the drive with a Set Ones Corresponding (SOC) command after the controller returns to idle. When the positioning operation completes, the attention line for that drive returns high, and the interrupt is generated.

If operations are to be overlapped, it is important that the control words for subsequent operations not write over the attention mask bit, or the interrupt will never occur. Thus, instead of using a move (MOV) instruction to write a whole new value into W0, the programmer should use a SOC or Set Zeros Corresponding (SZC) instruction to modify bits of W0 as needed.

There are three possible causes for an interrupt from the controller: completion of the controller cycle, completion of a Seek/Restore, or an error detected by the controller. The programmer must read and check W7 and W0 to determine the cause of the interrupt.

1.8.2 Word 1 — Command Code and Surface Address

Control word W1 contains the command code that specifies the operation that the controller is to perform. It also specifies the diskette surface, if applicable. Bits 1-3 and 8-9 are reserved, and should be forced to zeros.

1.8.2.1 Extended Mode — W1, Bit 0. The three command code bits (W1, bits 5-7) allow up to eight unique commands. The extended mode bit is interpreted by the controller as an additional command code bit, increasing the number of possible command codes to 16. If the extended mode bit is zero, bits 5-7 are interpreted as the normal commands. These are the commonly used commands such as Read Data, Write Data, and Store Registers. If the extended mode bit is 1, bits 5-7 are interpreted as the extended commands. These less commonly used functions, include the IBM-compatible Read Delete and Write Delete operations, Write Interlaced Sector Format, Extract Interlace Factor and Read Unformatted operations. Refer to paragraph 1.10 for individual descriptions of the extended mode commands.

1.8.2.2 Transfer Inhibit (TIH) — W1, Bit 4. If the TIH is set to 1 in conjunction with a Read Data command, the controller performs the specified read operation, including the cyclic redundancy check (CRC), but does not transfer any data to the 990 memory.

The TIH bit allows a check on the integrity of a record without the necessity of providing a memory buffer area to hold the data. If the CRC character recorded with the data does not correspond to the CRC character calculated during the read operation, the controller generates an error interrupt.

The TIH bit may be used with the Read Data and Read Delete commands.

1.8.2.3 Command Code — W1, Bits 5-7. Table 1-4 lists the normal and extended mode codes and the command names. A thorough description of the commands requires information about all of the control words, so the command word descriptions are deferred to paragraphs 1.9 and 1.10.

1.8.2.4 Surface Address — W1, Bits 10-15. The control scheme that is common to the hard disk systems and the flexible disk system allots a six-bit field to surface address selection. The diskette may contain a maximum of two recording surfaces that are selected by the least significant bit (LSB) (bit 15). Bits 10-14 should be all zeros or the controller will report command timeout for an illegal address. Bit 15 is zero for all single-sided diskettes, zero for side 0 of a double-sided diskette (lower surface), and one for side 1.

Note that the record address that is supplied in the control words is a starting address. The number of records in the data buffer may exceed the track capacity. For a double-sided diskette, the controller automatically switches heads from a filled track on surface 0 to the corresponding track on surface 1. This is called a cylinder operation. If a track on surface 1 is filled and more data

is to be transferred, the controller moves the heads to the next higher numbered cylinder and selects surface 0.

If a track is filled on a single-sided diskette, the head carriage steps to the next higher track location to complete the data buffer.

Table 1-4 W1 Command Codes

Extended Mode Bit 0	Code Bit 5 6 7	Command
0	0 0 0	Store Registers[1]
0	0 0 1	Write Format[2]
0	0 1 0	Read Data[1,2]
0	0 1 1	Write Data[2]
0	1 0 0	Read ID[1]
0	1 0 1	No-op(command timeout)
0	1 1 0	Seek[2]
0	1 1 1	Restore[2]
1	0 0 0	Extract Interlace Factor[1,2]
1	0 0 1	Write Interlaced Sector Format[2]
1	0 1 0	Read Delete[1,2]
1	0 1 1	Write Delete[2]
1	1 0 0	Read Unformatted[1,2]
1	1 0 1	Write Controller Memory
1	1 1 0	Read Controller Memory
1	1 1 1	Extended Test Commands

Notes:

[1] Operation preceded by TILINE memory test to verify 990 memory integrity before data transfer.

[2] Operation inhibited after self-test failure.

1.8.3 Word 2 — Record Format and Sector Address

1.8.3.1 Sectors Per Record — W2, Bits 0–7. One sector per record is the only legal format for the FD1000 system. This corresponds to 288 bytes per record on a double-density diskette, or 128 bytes per record on a single-density diskette. Bits 0-7 are ignored by the controller.

1.8.3.2 Sector Address (or Self-Test Failure Code) — W2, Bits 8–15. This field selects the starting sector for any type of read or write operation except format or interlaced sector format. These formatting commands start writing the first sector following the index pulse from the drive. The valid range for sector addresses is $00\text{–}19_{16}$ ($0\text{–}25_{10}$) for double-density or single-density diskettes. The controller automatically adds 1 to each sector address for single-sided diskettes.

The disk controller automatically performs a sequence of self-tests on power-up or on a 990 computer reset. Also, extended self-tests are available that can be initiated via control words. In either case, a self-test failure causes all ones (FF) to be reported in the right byte of W7 and an eight-bit failure code in bits 8-15 of W2. The self-test failure codes are described in Table 3-4.

1.8.4 Word 3 — Cylinder Address

This word selects the cylinder address to which the disk will Seek for a read or write operation. The valid number range is 0000 through 0076_{16} or 0000 through $004C_{16}$. This field is also used for Read Controller Memory and Write Controller Memory to specify a test number.

The surface address (head address) in W1, the sector address in W2, and the cylinder address of W3 form a complete address that uniquely locates a record on the diskette.

1.8.5 Word 4 — Transfer Word Count

This field selects the number of 16-bit data words that will be transferred between the disk and the TILINE. The byte selector, bit 15, must be zero. The word count range is limited by the available TILINE memory and by disk memory from the starting disk address to the last sector of the last track. A transfer from nonexistent TILINE memory will result in a TILINE timeout controller status.

NOTE

If a read with transfer inhibit is selected, this count specifies the number of logically sequential words on the diskette to be checked for integrity.

1.8.6 Word 5 — TILINE Buffer Address

During read or write operations, the TFDC acts as a TILINE master and stores data in, or reads data from, a buffer area in 990 memory. For a diskette write operation, the programmer assumes responsibility for placing the data in a contiguous area of TILINE memory before initiating the operation. The programmer informs the TFDC how many data words are to be transferred (W4), and the starting (lowest) address of the data in TILINE memory (W5 and 5 least significant bits of W6).

The disk controller assumes responsibility for controlling the TILINE transfers, for keeping track of the number of words transferred, and for incrementing the TILINE address after each data word transfer.

Similarly, for a disk read operation, the programmer assumes responsibility for assuring that the memory contains a contiguous data buffer large enough to accept the proposed transfer without overwriting needed information. The programmer specifies the word count and starting address via the control words.

The TILINE starting address is 20 bits in length. The 15 LSBs occupy bits 0-14 of control word W5. W5, bit 15 should be zero. The five most significant bits of the address are in bits 11-15 of W6.

The TILINE address W5 and W6 is updated in one-sector increments, that correspond to 128 (80_{16}) or 288 (120_{16}) bytes.This status information can be useful for diagnostic purposes if the operation terminates prematurely.

1.8.7 Word 6 — Unit Select and MSB Memory Address.
Bits 0-3 and 8-10 are reserved and should be set to zero.

1.8.7.1 Unit Select — W6, Bits 4-7. Bits 4-7 are a position-coded unit select field. One (and only one) bit position in this field should be set to one. Any other code will result in an off-line status report, and no drive operation will be performed. Some of the extended mode commands that do not involve a drive operation ignore the unit select field.

The valid unit select codes are:

Bit 4	5	6	7		Hexadecimal Digit
1	0	0	0	Unit 0	8
0	1	0	0	Unit 1	4
0	0	1	0	Unit 2	2
0	0	0	1	Unit 3	1

The unit number assigned to a drive is determined by jumper options on the drive assembly or on the buffered power supply/interface board. Jumper selections DS1 through DS4 correspond to unit 0 through unit 3, respectively.

1.8.7.2 TILINE Memory Address MSBs — W6, Bits 11-15. The five MSBs of the 20-bit TILINE memory buffer starting address occupy bits 11-15. Refer to the W5 description for additional information.

1.8.8 Word 7 — TFDC Status and Control.
W7 contains control bits from the 990 processor at the beginning of an operation and contains controller status data at the completion of the operation.

NOTE

W7 is the last word loaded during operation setup because the idle/busy bit (W7, bit 0) initiates controller operation when forced low by the processor. W7 must also be the first status word checked after an operation.

The bits in W7 are shown in Table 1-5.

Table 1-5. Control/Status Word W7 Bit Assignments

Bit	Function	Bit	Function
0	Idle/Busy	8	Memory Error
1	Operation Complete	9	Data Error
2	Error	10	TILINE Timeout
3	Enable Interrupt	11	ID Error
4	(reserved spare)	12	Rate Error
5	(reserved spare)	13	Command Timeout
6	(reserved spare)	14	Search Error
7	Abnormal Completion	15	Unit Error

W7, bits 8-15, when all set (FF_{16}), indicates that a self-test failure has been detected.

1.8.8.1 Idle/Busy Control/Status — W7, Bit 0. The controller must be in the idle mode (W7, bit 0 = 1) for the 990 processor to load the control words into the controller or to read any status other than the idle/busy status bit. This prevents interference to the operation in progress.

The programmer should read W7 and should check bit 0 prior to sending command words. If the controller is busy, a simulated W7 word (with bit 0 = zero) is returned. Bits 1-15 are meaningless in this case. If the controller is idle, bits 1-15 provide meaningful status for the previous operation and the other status words may be read if desired.

After verifying that the controller is idle, the programmer may send control words W0-W6 to the controller. The controller operation is initiated when control word W7 (with a zero in bit 0) is transmitted to the controller. The low idle/busy bit forces the controller to initiate its command decode and operation cycle.

1.8.8.2 Complete — W7, Bit 1. The complete bit is set by the controller upon normal completion of a command with no errors detected. The programmer may reset this bit as part of the interrupt service or status checking routine, or may leave it alone until the next block of control words is sent to the controller.

1.8.8.3 Error — W7, Bit 2. W7, bit 2 is set if any error is detected. The programmer may obtain more detailed error information by examining W7, bits 7-15 and W0, bits 0-5. Diagnostic programmers will also want to examine W2, bits 8-15 if W7, bits 8-15 are FF_{16}.

1.8.8.4 Enable Interrupt — W7, Bit 3. The enable interrupt bit, if desired, is set by the programmer when initiating controller operations. This bit enables the controller to generate an interrupt on normal completion (W7, bit 1) or on error termination (W7, bit 2). The enable interrupt bit is used for interrupt-driven device service routines. The enable interrupt bit should be cleared as part of the device service routine.

Note that attempts to set the enable interrupt bit at one time and to activate the controller at another time will result in false interrupts. Therefore, the interrupt selection should be part of the same W7 word that activates the controller.

The attention interrupts (described with W0, bits 8-11 and 12-15) are independent of the enable interrupt bit. The attention interrupts are associated with the completion of disk drive Seek and Restore operations that may be overlapped with operations involving different drives. It is the programmer's responsibility to read and to test the controller status words to determine the cause of an interrupt.

1.8.8.5 Controller Status Field — W7, Bits 7-15. W7, bits 7-15 are used to report controller status after a command has been executed. These bits contain valid error information when the error bit (W7, bit 2) is set. Bits 8-15 are all on (FF_{16}) in the event of a self-test failure. If the next command after a self-test failure involves a drive operation, bits 8-15 will not clear and the operation will be inhibited. A successful self-test must be performed to escape from this condition. An I/O reset or power reset will clear the controller logic and perform a self-test.

1.8.8.6 Abnormal Completion Error — W7, Bit 7. The abnormal completion bit sets if an operation is terminated as the result of a reset from the 990 chassis. This reset may be an I/O reset, power failure warning pulse, or power reset.

1.8.8.7 Memory Error — W7, Bit 8. The TILINE memory boards in the 990 chassis are capable of detecting parity errors during a memory read operation and of informing the other circuit boards of the error. If this TILINE parity error occurs during a Write Data or Write Format operation (normal or extended), it is an indication that bad data may have been read from memory and recorded on the diskette. The memory error and error bits (bits 8 and 2) will be set when the operation completes.

The controller performs an automatic TILINE read/write test prior to executing the following commands: Store Registers, Read Data, Read ID, Extract Interlace Factor, Read Delete, and Read Unformatted. The memory error and error bits set if the automatic read/write test fails. Memory error due to read/write test failure does abort the operation.

1.8.8.8 Data Error — W7, Bit 9. The data error bit indicates that an error was detected in the process of reading data from the diskette.

This bit is interpreted in several ways, depending on the type of operation, type of diskette in the selected unit, and whether or not the ID word error (W7, bit 11) is also set. Table 1-6 summarizes the conditions that can set the data error bit.

Table 1-6. Data Error Summary

Diskette Type	Operation	ID Word Error	Cause of Data Error
SD, DD	Read Data	No	CRC error on a sector persisting beyond controller automatic retries
SD	Read Delete	No	Same
SD	Read Delete/Read Data	Yes	Opposite type address mark detected
SD, DD	Write Format	No	Surface analysis failure, data field compare error or CRC error
SD, DD	Write Format	Yes	Surface analysis failure and ID field check error

A data error forces termination of the operation. If the CRC character in the record ID fails to compare, the controller sets the ID word error (W7, bit 11) rather than the data error bit.

Note that the data CRC character cannot be checked until after the sector of data has been transferred to TILINE memory. The programmer assumes responsibility for taking appropriate action on the bad data when data error status is detected. The programmer should build in at least three software retries in addition to the automatic retries performed by the controller.

1.8.8.9 TILINE Timeout — W7, Bit 10. In order to prevent an error from indefinitely hanging the TILINE, all TILINE peripheral controllers incorporate a timer that allots up to 10 ± 2 microseconds for a TILINE operation. If the timer expires before completion of the TILINE cycle, the controller operation is terminated, the TILINE interface logic is cleared, and the TILINE timeout bit is set.

The most common cause for a TILINE timeout is an attempt by the controller to read or to write to a nonexistent TILINE memory location. This type of error can occur during any operation in which the controller initiates a TILINE data transfer. The Seek and Restore operations cannot cause a TILINE timeout.

1.8.8.10 ID Word Error — W7, Bit 11. Diskettes for the FD800 and the FD1000 flexible disk systems are soft-sectored, with a one sector per record format. A set of record identification words are recorded at the start of each sector. It is necessary to read these sector ID words in order to locate a particular record for reading or writing. This sector ID read and compare operation is automatically performed as part of a Read Data, Read Delete, Write Data, Write Delete, or Read Unformatted operation.

A failure to locate the desired sector within four diskette revolutions will set the ID error status bit and will terminate a Read Data, Read Delete, Write Data, or Write Delete operation. Read Unformatted is a special case. Refer to the command descriptions.

ID word error will be set in conjunction with data error if a delete data mark is detected during a Read Data operation, or if a normal data mark is detected during a Read Delete operation.

1.8.8.11 Rate Error — W7, Bit 12. The data transfer rate from the disk during a read operation (Read Data, Read Delete, Read Unformatted) is fixed by the inertia of rotating components, while the TILINE data transfer rate from controller to memory is determined by bus activity and priority. Under severe conditions of bus overload, the TILINE may not be able to keep up with the disk interface. This condition will corrupt the data transferred to memory. A rate error sets the rate error status bit and terminates the operation.

In a similar manner, a TILINE overload during a Write Data or Write Delete operation will corrupt the data recorded on the diskette and will cause a rate error.

1.8.8.12 Command Timeout — W7, Bit 13. The controller is allotted a predetermined amount of time for each command. If the controller fails to complete the operation (or to otherwise terminate) before the timer loop expires, command timeout is set and the operation is terminated.

Illegal command parameters will also cause command timeout and will terminate the operation. Command code 101 (nonextended) is a no-op code that results in termination with command timeout status.

1.8.8.13 Search Error — W7, Bit 14. Each data record on a diskette is preceded by a synchronization field and a data address mark. During read operations, the controller locates the record by reading and comparing ID words. It then starts monitoring for the data mark. If the data mark is not detected within the allotted window (one millisecond), the controller automatically retries the cycle up to five times. If the last retry fails, the command terminates with search error status.

Search error on a Read Unformatted command is a special case. Refer to the command descriptions for additional information.

1.8.8.14 Unit Error — W7, Bit 15. An error associated with the selected disk unit terminates the operation, sets the appropriate status bits in W0, and sets the error and unit error summary bits in W7.

After detecting unit error status, the programmer should read W0 to determine the error cause and the recovery strategy.

The following errors are included under the unit error category:

- The selected unit is write protected and a Write Format, Write Interlaced Sector Format, Write Data, or Write Delete operation is attempted. All of these operations write information on the disk. Certain extended test commands can cause this type of error, as described in Section 3.

- The selected unit is not ready (W0, bit 1) or is off-line (W0, bit 0) and any operation involving the disk is attempted. These operations are Write Format, Read Data, Write Data, Read ID, Seek, Restore, Extract Interlace Factor, Write Interlaced Sector Format, Read Delete, Write Delete, or Read Unformatted. Some of the extended test commands can cause this error, as described in Section 3.

- The selected unit is unsafe (W0, bit 3) and any operation other than Store Registers or Restore is issued. The unsafe error bit is intended to inhibit disk data transfer operations when the 990 software is not informed of the most recent change in disk unit status. For example, if the diskette has been changed and no subsequent Store Registers command performed, the 990 device service software does not know whether a single-density or double-density diskette is installed in the unit.

- A seek incomplete error occurs due to inability to locate the specified track, or due to a diskette change without proper initialization (including a Restore command).

- A seek incomplete error occurs after a Restore command. The error occurs if track 00 is not sensed at completion of the disk drive restore cycle. Since Seek operations are based on the cumulative history of head carriage moves since a restore to track 00, failure to properly restore will result in erroneous seek operations.

- A Seek operation is attempted to a cylinder that is out of bounds (greater than $4D_{16}$), resulting in a seek incomplete error. This includes the case where a read or write operation attempts to transfer data beyond the end of the last cylinder.

1.9 NORMAL COMMANDS

The normal (nonextended) commands are the eight commands for which the extended mode bit (W1, bit 0) is not set. These commands are Store Registers, Write Format, Read Data, Write Data, Read ID, NOP (command timeout), Seek, and Restore. These are the basic commands most commonly used for normal data storage and retrieval operations.

1.9.1 Store Registers (000)

The DSRs in Texas Instruments standard disk-based operating systems have been generalized to work with a number of different disk storage systems. These include the FD1000 flexible disk and the DS10, DS25, DS50, and DS200 disk systems. Although the control word structure for all of these systems is basically the same, disk operating parameters such as words per track and cylinders available per logical unit vary from system to system. The operating system needs access to these operating parameters in order to properly format records and to manage the task roll-in and roll-out sequences.

The Store Registers command provides a means for the operating system software to interrogate a disk system to determine the critical parameters of the systems.

A Store Registers command causes the disk controller to send one, two, or three words to 990 memory, starting at the memory address specified by the control words. The number of words sent to memory is specified by the word count in W4. The three words, Figure 1-19 , contain the following information:

- Word 1. This word contains the total number of formatted words that can be recorded on a disk track. The numbers are:

  Single-Density — $1664_{10} = 0680_{16}$
  Double-Density — $3744_{10} = 0EA0_{16}$

- Word 2. This word contains the sectors per track and the number of words of overhead per record to be used in the calculations of the format parameters. For single- or double-density:

  Sectors per track — 26_{10} = $1A_{16}$
  Overhead per record — 0

Therefore, Store Registers word 2 = $1A00_{16}$ for either diskette type.

- Word 3. This word contains the number of tracks per cylinder and the number of cylinders per logical unit. Each individual diskette drive is a logical unit. Word 3 parameters are:

Item	Bits	SSSD/DSDD
Tracks per cylinder	0-4	1/2
Cylinders per logical unit	5-15	77/Same (hex 4D)

Therefore, word 3 = $084D_{16}$ for single-density and $104D_{16}$ for double-density.

The Store Registers operation determines the operating parameters for the selected disk drive by reading them from the disk controller. Store registers does not actually read any information from the drive itself. However, the controller must check a sense line that detects whether a single-density or a double-density diskette is installed in the drive.

A Restore command and a Store Registers command should be performed for any disk unit that shows unsafe in status word W0. The Restore operation clears the drive electronics and positions the head carriage at track 00. The Store Registers command identifies the current recording parameters to the 990 software. A diskette change is the most common reason for an unsafe condition.

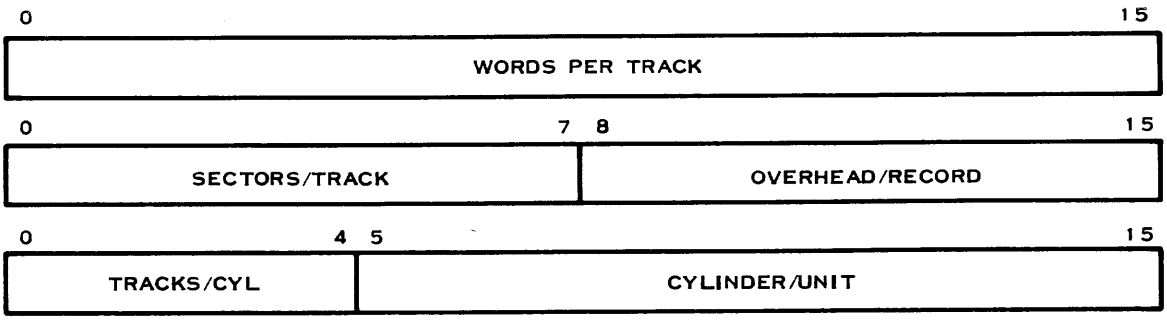

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Figure 1-19. Store Registers Data Format

Table 1-7 is an example of an eight-word control block that will cause the disk controller to perform a store registers operation.

Table 1-7. Example of Control Words for Store Registers Command

Word	Hexadecimal Data	Comments
0	0000	Clears the attention mask bits
1	0000	Command = Store Registers. Head select is irrelevant
2	0000	Not used
3	0000	Not used
4	0006	Three words (six bytes)
5	357A	Put words in memory starting at CPU byte address 357A (number in W5 is always an even byte count)
6	0800	Unit 0*
7	1000	Interrupt enabled on completion. Controller status from previous operation zeroed out

Note:

* If the selected unit is not on-line, the TFDC supplies the double-density values by default.

1.9.2 Write Format (001)

The Write Format command is used for verifying and for formatting a new diskette or for reformatting an existing diskette. One complete track is formatted per command.

CAUTION

The Write Format operation destroys any data that may have been previously recorded on the specified track.

After initialization, the controller performs the following operations:

1. Check drive status and Seek to specified track.
2. Perform surface analysis of track by writing and reading back test data pattern.
3. Fills record ID words at the start of each sector and record data fields with a temporary filler word specified by the programmer.

If the surface analysis fails, the controller returns data error status upon completion. Regardless of a surface analysis failure, the controller attempts to format the track.

Prior to initiating a Write Format command, the programmer must store a filler word at a known TILINE memory address. This address is supplied to the controller, which accesses that location and uses the contents repeatedly to fill all the data record areas on the track.

Table 1-8 is an example of the control words required for a Write Format command.

The word count in W4 is not applicable. The controller internally selects the maximum possible number of words per record, based on diskette type. The selected number is 64 words per record (single-density) or 144 words per record (double-density). This is the number of times that the filler word is recorded in each sector.

Table 1-8. Write Format Command Example

Word	Data	Comments
0	0000	
1	0100	The command is Write Format; the surface address = 0
2	0100	Sectors per record is treated as a "don't care" field; sector address does not apply, as operation always starts from first sector
3	0049	Track $73_{10} = 49_{16}$
4	0000	Word count not applicable (controller internally selects maximum value, based on diskette type)
5	3BFE	CPU byte address of the filler word to be stored repetitively in all data fields
6	0400	Unit 1 selected. 5 address MSBs are zeros
7	1000	Interrupt on completion

The 20-bit TILINE memory address of the filler word is contained in bits 11-15 of W6 and bits 0-14 of W5. The unit select field is position-coded, so the hexadecimal equivalent of the unit select field is not equal to the selected unit number.

1.9.3 Read Data (010)

The Read Data command identifies a record location, specifies how many words are to be transferred from this record, and gives the starting address of a memory buffer area that is to receive the data from the diskette. Table 1-9 is an example of the control words for a Read Data command.

After initialization, the controller performs the following basic operations:

1. Check drive status (not ready and seek incomplete bits)
2. Seek to specified cylinder
3. Read ID words until the specified starting sector is located. Check ID CRC character to verify ID
4. Read data from diskette and transmit to TILINE memory. Check data CRC character at end of record
5. Continue until word count is decremented to zero or the end of the diskette recording area is reached.

NOTE

The data transfer to memory may be suppressed by the TIH bit in W1. A Read Data command with transfer inhibited after a Write Data command checks the integrity of the newly written record without tying up memory space or TILINE access time.

The Read Data operation is inhibited if the status check of the selected drive shows a not ready, unsafe, or seek incomplete condition. An unsuccessful self-test also inhibits operations to the failing drive.

The drive must seek (move the head assembly) to the specified track location. A seek is automatically performed as part of the Read Data operation. To increase throughput in a multidrive system, it may be desirable to use the independent, overlapped seek capabilities of the Seek command (110) to position the heads before initiating a Read Data operation. The Seek command also loads the heads for a one second interval after reaching the cylinder.

Once the heads are determined to be at the correct cylinder location, the controller starts monitoring the ID words from the diskette. A unique address mark precedes each ID header for synchronization purposes and to distinguish between data and ID words. ID word formats are described with the Write Format command.

The ID words provide an independent cross-check on the track positioning, head selection, and sector determination functions. A disagreement between the hardware-derived values and the corresponding ID header values indicates that the hardware has malfunctioned or that the diskette was misformatted. Either case represents an error condition. If the automatic retries are unsuccessful, the operation is terminated with ID error status. Seek incomplete status is also returned if the track information is wrong.

Table 1-9. Example of a Read Data Command

Word	Data	Comments
0	0000	Clear the attention mask bits
1	0201	Read Data, surface 1 (side B of double-density diskette)
2	0109	One sector per record, start on sector 9
3	001B	Cylinder $1B_{16} = 27_{10}$
4	1144	1144_{16} bytes = 08A2 words = 2210_{10} words
5	3577	CPU byte address = 3576 (bit 15 is truncated)
6	0100	Unit 3, TILINE address MSBs are all zeros
7	0000	Initiate operation; do not interrupt on completion.

The starting record location specified in the control words should match with a record ID header within one disk revolution. The controller retries for up to four revolutions searching for an ID match. If a match is not found, the operation is terminated with ID error and seek incomplete status.

When the specified starting sector rotates under the head (as indicated by an ID compare), the controller turns off the read data separation for a gap period following the header and reenables it prior to the data area. Upon recognizing the data address mark, the controller starts reading composite serial data from the diskette, separating clock and data bits, assembling it into 16-bit parallel words, and transferring them to TILINE memory.

When the controller encounters the end of a record, but the remaining transfer word count is nonzero, the controller automatically continues reading on the next logical record of the track if it exists. The new record ID is checked before the read operation continues. The next logical record is the next sequential sector unless the diskette is formatted with interlacing. Refer to the Write Interlaced Sector Format extended mode command for information about interlacing.

For a double-density diskette, if the controller encounters the end of a track on surface 0, but the transfer word count is nonzero, the controller automatically increments the head address to surface 1. After ID checks, the read operation on surface 1 starts from sector 00 and continues until the word count is decremented to zero. Surfaces 0 and 1 at a given head position form a two-track cylinder.

For a single-density diskette, the terms track and cylinder have identical meanings because only one side is used.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder and selects head address 0 for the new track. After ID checks, the read operation proceeds from sector 00. If the last cylinder is read and the transfer word count is still nonzero, the operation terminates with unit error and seek incomplete status.

Consider the case in which the transfer word count reaches zero before the end of a physical record. In this case, the TILINE data transfers stop when the word count reaches zero, but the controller reads to the end of a record in order to read and verify the CRC character. The programmer should check status to verify the transferred data.

1.9.4 Write Data (011)

The Write Data command causes the controller to record data on a previously-formatted track or to write over a previous record.

The basic operations performed during a Write Data Command are as follows:

1. Check drive not ready, seek incomplete, unsafe, and write protect status of selected drive.
2. Seek to specified cylinder and load heads.
3. Read ID words, searching for starting sector.
4. Write gap, and data address mark.
5. Transfer words from TILINE memory buffer area to controller and record on diskette.
6. Record CRC character at end of last physical record.
7. If word transfer count has not reached zero, continue to next sector and start at step 3.

The Write Data operation is inhibited if the selected drive shows not ready, seek incomplete, unsafe, or write protect status, or if a self-test failure has occurred.

A seek to the cylinder address specified in W3 is performed as part of the Write Data operation. If the head carriage is not already at that cylinder, the operation will be delayed by the amount of time required to position the head carriage and load the heads to the disk surface. To increase throughput in a multidrive system, it may be desirable to use the independent overlapped seek capabilities provided by the Seek command (110). The Seek command also loads the heads for a one-second interval.

After head positioning and loading, the controller reads each sector ID on the track, searching for the starting sector specified in W2. Recall from the track format description that each ID field is preceded by a synchronization field and ID address mark. The synchronization field, ID address mark, ID words, and ID cyclic redundancy check (CRC) word are all recorded on the diskette by a Write Format command.

The controller performs retries for up to four revolutions while searching for a valid ID field (no CRC error) that matches the specified starting address. Also, the controller attempts a home-in operation on SSSD diskettes, to accomodate IBM bad tracks. A failure to locate a specified ID returns ID error status and terminates the operation. A track number error returns seek incomplete status.

When the correct sector is located, the controller writes a standard pattern in the ID gap, followed by a synchronization field, a data address mark character, and the first data word.

The transfer word count is decremented each time the controller retrieves a new data word with a TILINE master cycle. The controller writes data onto the diskette until the word count reaches zero. When the specified number of words is greater than the number of words per sector, the controller continues to the next logically sequential record, reads the ID words, and continues writing the data.

The controller continues over sector, head, and cylinder boundaries until the word count reaches zero. Note that the next logically sequential record is determined by diskette type and interlace factor (if any), as well as by the location of the initial sector.

If the track was initially formatted with a Write Interlaced Sector Format command, the next logically sequential record is separated from the current record by a number of sectors equal to the interlace factor minus 1.

If the end of the track is reached on side 0 of a double-sided disk, the upper head is selected and the operation continues on the upper half (side 1) of that cylinder. When the end of the cylinder is reached, the head carriage steps to the next track (cylinder) position and the lower head is selected.

If the initial word count was an even multiple of the number of words per sector, the last sector will be completely filled (64 or 144 words), and the CRC word for that sector will be recorded following the last data word.

In the more common case, the word count is not an even multiple of the number of words per sector. The controller fills the remainder of the last record with zeros and then places the CRC character at the end of the record.

A Write Data command with an initial transfer word count of zero does not write anything on the diskette.

Table 1-10 is an example of a Write Data command.

Table 1-10. Example of a Write Data Command

Word	Data	Comments
0	0000	Clear attention mask bits
1	0301	Write Data, surface 1 (side B of double-density diskette)
2	0109	One sector per record, start on sector 9
3	001B	Cylinder $1B_{16} = 27_{10}$
4	1144	1144_{16} bytes = $08A2_{16}$ words = 2210_{10} words
5	3578	CPU byte address of TILINE buffer = 3578_{16}
6	0800	Unit 0, part of TILINE buffer address
7	0000	Initiate operation, do not interrupt on completion

1.9.5 Read ID (100)

The Read ID command is provided for compatibility with the device service routines for the hard disk systems. The hard disk controllers respond to this command by actually reading the record ID words from the disk and transferring up to three words to TILINE memory.

The TFDC develops two ID words from the parameters supplied with the Read ID command and a third word (word count per record) for the diskette type. The ID values are not verified by a read operation to the drive, but a unit error is reported if the drive is off-line or not ready.

Figure 1-20 shows the format of the Read ID words transferred to memory. The transfer word count for the Read ID command should be in the range 1-3. If the word count is 0, no words are transferred. If the word count is greater than 3, only 3 words are transferred. Table 1-11 is an example of a Read ID command.

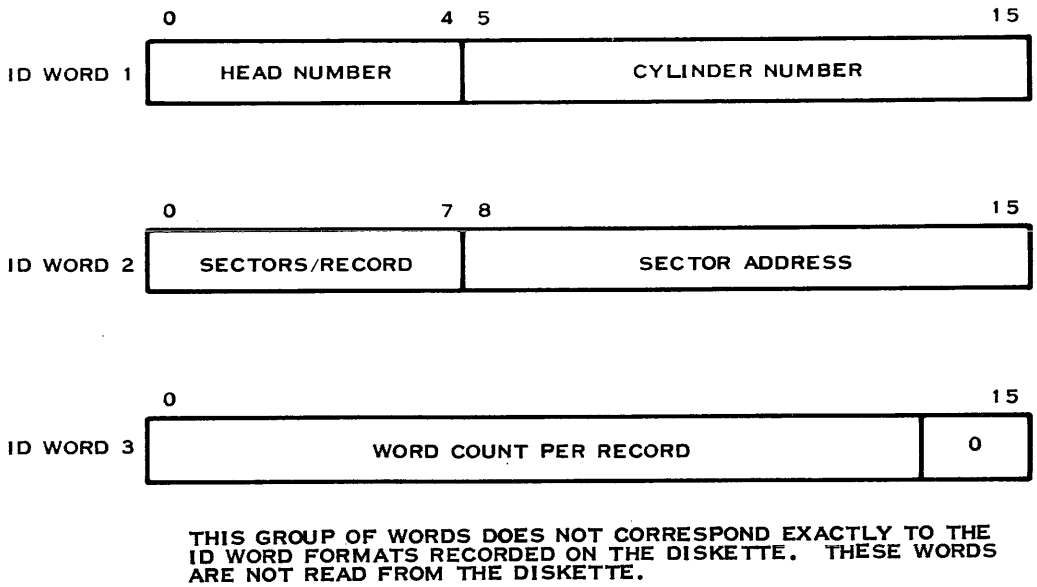

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Figure 1-20. Read ID Format

1.9.6 No-Operation — NOP (101)

Command code 101 is used by the hard disk controllers to initiate an unformatted write operation. Unformatted writing is not supported by the TFDC. The controller terminates the operation and returns command timeout status.

1.9.7 Seek (110)

The Seek command allows the programmer to command the head assembly of the selected unit to move to a specified track and to load the heads in anticipation of a future data transfer command. Seek operations to the four (maximum) drives are independent and may be overlapped.

The disk controller does not remain busy for the duration of the Seek operation. Upon receipt of the command words, the controller checks status on the selected drive and initiates the physical Seek operation. This forces the attention bit for the affected disk become go inactive (low). If the drive returns not ready, unsafe, or seek incomplete status, the operation aborts with unit error status. If no errors occur, the disk controller terminates normally and becomes idle while the Seek is still in progress. The disk controller is free to accept any type of command for any drive except the one that is Seeking.

The attention line for that drive remains at zero until the specified cylinder is located. The attention bit goes to one and if the associated mask bit is set and the controller is idle, an interrupt is sent to the 990 CPU. If the controller is busy, the interrupt waits until the controller becomes idle again.

The heads remain loaded to the disk surface for approximately one second after the cylinder is located. This allows ample time for the controller to generate the attention interrupt. It also allows time for the 990 processor to determine that the interrupt resulted from Seek completion and to send the write or read-type command.

Table 1-11. Read ID Command Example

Word	Data	Comments
Command:		
0	0000	Clear attention mask bits
1	0401	Read ID, surface 1
2	0109	One sector per record, sector 9
3	001B	Cylinder 1B (hex) = 27
4	0006	6 bytes = 3 words (maximum for this command)
5	4BF0	CPU byte address of TILINE buffer = 4BF0, equivalent to TILINE word address 025F8
6	0800	Unit 0, part of TILINE address
7	1000	Initiate operation, enable interrupt on completion
Returned (CPU Byte Address):		
4BF0	081B	Head No. 1, Cylinder 1B (hex) = 27
4BF2	0109	One sector per record, sector 9
4BF4	0120	120_{16} = 288 bytes = 144 words (double-density diskette in selected unit)

Use of the Seek command allows the physical head movement to be performed without keeping the controller busy for the duration of the electromechanical operation. This is a significant advantage in terms of system throughput if two or more drives are operated from one controller.

1.9.8 Restore (111)

The Restore command positions the heads of the selected unit to cylinder 00 of the diskette and loads the heads for a one-second period. A Restore or a Store Registers operation must be performed to clear unsafe (W0, bit 3) or seek incomplete (W0, bit 5) drive status. Restore operations, like Seek operations, may be overlapped.

The Restore command places the head carriage in a home base position. The controller issues step commands to position the head carriage. It also keeps track of current cylinder location by a cumulative tally of positive (inward) and negative (outward) steps. A Restore command reestablishes the reference location for positioning.

A Restore operation is required whenever a system reset has occurred or whenever a diskette has been removed or swapped from the selected drive. The system reset is identified by error and abnormal completion status. A diskette change is identified by unit error and unsafe status. Restore is also required to clear seek incomplete status for the specified drive.

Upon receipt of the Restore command, the controller performs the following operations:

1. Check ready status of selected unit.

2. If ready, immediately return controller to idle status with operation complete.

3. Start stepping the drive heads in the negative direction (away from the center of the diskette) while monitoring the track 00 signal line. A maximum of 80 steps is allowed. The drive attention bit goes to zero during the positioning operation.

4. Cease stepping when track 00 signal from drive goes active. At this point the heads are positioned and loaded at cylinder 00. Seek incomplete status is reported if track 00 is not reached within 80 steps.

5. If the attention mask bit for the unit is set, an attention interrupt is generated when the attention line returns high (assuming the controller is idle). There is no other notification of completion, as the operation complete status was activated on receipt of the command.

If the selected unit is not ready when the Restore command occurs, the operation is aborted (idle and error). Unit error is loaded into the controller status register, and off line, not ready, unsafe, and seek incomplete are loaded into the disk status register. Thus, there is not an immediate normal operation complete if the drive is not ready when the operation is initiated.

If the operation starts normally (selected unit ready), the controller sets the idle and operation complete status bits and starts stepping the head carriage. If track 00 is not detected within 80 steps, seek incomplete is loaded into the disk status register (W0) along with the associated drive attention bit. Note that the idle and operation complete bits remain set.

If the associated attention mask bit is set, an attention interrupt occurs when the drive attention line returns high (controller idle). This interrupt occurs whether the attention line returns high for a successful or an incomplete positioning operation.

1.10 EXTENDED MODE COMMANDS

The extended mode commands are those commands for which the extended mode bit (W1, bit 0) is set. The extended mode bit allows the command code field (W1, bits 5-7) to select from an additional set of eight commands. These are the commands that are less commonly used during the course of data storage and retrieval operations.

1.10.1 Extract Interlace Factor (000 — Extended)

It is possible to format a diskette so that the logical order in which sectors are read or written is not the same as the physical order of sectors on the diskette. For example, a diskette may be formatted with sequential logical records on alternate physical sectors. A large data buffer would be recorded on physical sectors 0, 2, 4, 6,...22, 24, 1, 3, 5,...23, 25 of a double-density diskette. Two diskette revolutions are required to fully record the track.

The interlace factor is a whole number that describes the relationship of physical and logical sector order. For the example above, sequential logical records are on every second physical sector, and the interlace factor is two. In general, for an interlace factor of n, sequential logical records are on every nth physical sector, and n diskette revolutions are required to record or to read a full track. Another way of looking at this is that there are n-1 sectors between logically sequential sectors. For convenience, an interlace factor of zero is defaulted to an interlace factor of one (physical and logical record order correspond with no skipped sectors). Refer to the Write Interlaced Sector Format description, paragraph 1.10.2, for additional information.

The Extract Interlace Factor command may be used to determine the interlace factor of a diskette installed in the selected unit. This is basically a diagnostic command that is typically entered by an operator who needs to know the characteristics or to make a duplicate of an unknown diskette. Note that the Read Data and Write Data commands automatically adapt to the interlace factor formatted on the diskette.

The Extract Interlace Factor command always returns one word. The word count in the command words is ignored by the controller.

The interlace factor is determined by reading ID words from the disk drive, so drive unit status is checked, and the heads are positioned to the correct cylinder and loaded to the diskette surface. The interlace factor is calculated in the controller and returned to TILINE memory at the specified address. The interlace factor returned is in the range 1 to 19_{16} ($1-25_{10}$) for a single or double-density diskette.

The error and ID error status bits are set if the controller is unable to determine the interlace factor. Such a case could occur with a defective or unformatted track.

Table 1-12 is an example of an Extract Interlace Factor command.

1.10.2 Write Interlaced Sector Format (001 — Extended)

In some cases it is desirable to format a diskette so that logically sequential records are not placed in physically adjacent sectors. For example, the software might have to read a record and might spend a considerable amount of time processing the data before reading the next record. If this time delay extends into the time that the heads reach the next physical sector, this second record cannot be read until a full revolution (166.67 milliseconds) later. However, if the diskette is formatted to skip a sector between logically sequential records, this delay would be reduced to less than 6.27 milliseconds.

Table 1-12. Extract Interlace Factor Example

Word	Data	Comments
Command:		
0	0000	Clear interrupt mask
1	8000	Extended mode, command code 0, surface 0
2	0100	
3	004A	Cylinder 74
4	0002	Byte count = 2, word count = 1
5	41BA	CPU byte address 41BA, equivalent to TILINE word address 020DD
6	0800	Unit 0, part of TILINE address
7	0000	Initiate operation, no interrupt on completion
Returned (CPU Byte Address):		
41BA	0001	Interlace Factor = 1 (no interlacing)

The interlace factor is an integer that describes the relationship between physical and logical sector order. For the example above, sequential logical records are located on every second physical sector, so the interlace factor is two. In general, for an interlace factor of n, sequential logical records are located on every nth physical sector and n revolutions are required to completely read a track.

Selection of interlace factors may be used to tune the flexible disk storage system for best throughput with specific software. This is described in the installation and operation manual. For example, an original equipment manufacturer (OEM) may be using a high-speed Texas Instruments disk-based hardware/software system as a manufacturing facility to produce formatted or fully recorded diskettes for a flexible-disk based product. The interlacing capabilities allow the OEM to supply flexible disk storage that is properly mated to the product's software capabilities and requirements. Interlacing may be specified when a diskette is initialized by the DX10 Initialize New Volume (INV) command.

Note that the Read Data or Write Data operations automatically locate the correct logically sequential records regardless of the interlace factor. All records on a track are formatted with the same interlace factor; the first logical record of the track is always in sector 00.

The Write Interlaced Sector Format command is very similar to the Write Format command. It is used for verifying and formatting a new diskette or for reformatting an existing diskette. One complete track is formatted per command.

CAUTION

The Write Interlaced Sector Format operation destroys any data that may have existed on the specified track.

Prior to initiating the command, the programmer must store two words in sequential TILINE word addresses. The first address must be loaded with a filler word. The address of the filler word is supplied to the controller as part of the control words. During the formatting operation, the controller reads this address and stores the word temporarily. This word is later used repetitively to fill all of the data areas of the formatted track. The second address must be loaded with the interlace factor. The valid range is $0000\text{-}0019_{16}$ ($0\text{-}25_{10}$). Note that the value zero is automatically defaulted to one within the controller (no interlacing).

After initialization, the controller performs the following operations:

1. Check drive status and Seek to specified track.
2. Perform surface analysis of track by writing and reading back a test data pattern.
3. Using the interlace factor read from TILINE memory, record ID words on correct physical sectors (starting at physical sector 00 for double-density, physical sector 01 for single density). Fill the data area of each record with the filler word previously read from TILINE memory.

If the surface analysis fails, the controller returns data error status upon completion. Regardless of a surface analysis failure, the controller attempts to format the track.

Table 1-13 is an example of the control words for a Write Interlaced Sector Format command.

1.10.3 Read Delete (010 — Extended)

The Read Delete and Write Delete commands are provided for compatibility with IBM formats on the SSSD diskette. Control information or other privileged data may be recorded in a manner that is inaccessible to an ordinary Read Data command. A special data mark precedes each field of privileged data. The sector is called a deleted sector, and the data mark is called a delete data mark.

1.10.4 Write Delete (011 — Extended)

The Write Delete command is provided for compatibility with IBM formats for the SSSD diskette. The Write Delete command allows the programmer to write a sector of data that is inaccessible to an ordinary Read command. A special deleted data address mark is written at the start of the data field. This mark, which replaces the usual data address mark, cannot be interpreted by an ordinary Read Data command, so reading of such a sector is privileged. A Read Delete command (paragraph 1.10.3) is required to read a deleted record. The Write Delete command is similar to the Write Data command (paragraph 1.9.4) with these exceptions:

- Write Delete is valid only for single-density diskettes.
- A Write Delete command automatically defaults to a Write Data command for a double-density diskette.

1.10.5 Read Unformatted (100 — Extended)

The Read Unformatted command allows the programmer to read a track and to examine a specified number of words without regard to CRC errors, interlacing, or standard record formatting. This is primarily a diagnostic feature.

The programmer specifies a sector of the selected track to start the read process. Once a valid ID address mark is detected, the controller checks the second ID word (sector address) looking for a match with the specified starting sector number. Once the sector is located, the controller starts reading the specified number of words to TILINE memory, starting with the ID 2 word (sector number).

ID words, CRC words, gap data, address marks, and data fields are read and transferred to memory as though they were all data words. There are normally glitches in the gaps. These glitches are due to write head turnon and turnoff transients, and the fact that the write clock phases recorded during formatting and write operations differ. These glitches may cause apparent shifting of word boundaries.

A timeout feature in the Read Unformatted command limits the operation to a maximum of two diskette revolutions, even if the transfer word count has not decremented to zero. Such large word counts are uncommon. The Read Unformatted command reads deleted sectors (those recorded with the special delete address mark preceding the data) without error.

The controller returns an ID error if no valid ID address mark can be found. This might occur, for example, on a track that never was formatted.

NOTE

If the specified starting sector is not found within four revolutions, a search error is reported.

The programmer may deliberately specify a nonexistent starting sector address (such as $1A_{16}$), in which case the controller starts reading from the first valid ID address mark and continues until the transfer word count decrements to zero or the operation times out after two revolutions.

Table 1-13. Write Interlaced Sector Format Example

Word	Data	Comments
0	0000	
1	8100	Extended mode, command 001, surface 0
2	0100	
3	0049	Cylinder $49_{16} = 73_{10}$
4	0000	Word count not applicable (controller internally chooses maximum value, depending on diskette type).
5	30CC	CPU byte address for the filler word. Interlace factor word is stored at next even byte address (30CE for this example).
6	0400	Unit 1 selected. Five address MSBs are zeros.
7	1000	Interrupt on completion.

The Write Delete command (paragraph 1.10.4) is used to record each sector of deleted data on a single-density diskette. The data is said to be deleted because the special data mark removes it from the range of a Read Data command. A Read Delete command is required to read a deleted sector.

The Read Delete command is similar to the Read Data command (paragraph 1.9.3) with the following exceptions:

- Read Delete is valid only for single-density diskettes.
- A Read Delete command will automatically default to a Read Data command for a double-density diskette.

The controller returns both data error and ID error if the programmer attempts to read a deleted sector with a Read Data command or to read an ordinary sector with a Read Delete command. The read command type must match the data type.

1.10.6 Write Controller Memory (101 — Extended)

This command is reserved for diagnostic purposes. It has no operational uses. This command makes it possible to write data words from the 990 computer to the scratchpad RAM on the controller. The cylinder address field in W3 serves as the internal address value for this operation. The address map in Table 1-14 shows the allowable address ranges. The starting address of the main memory buffer area and the word count are specified as in any other read or write operation.

CAUTION

The contents of the on-board scratchpad RAM are coordinated with the 9900 control program ROM and real-time controller operations. Possible side effects of modifying these locations include destruction of files on the diskette. Do not use this command unless specifically authorized and guided by TI engineering.

The Write Controller Memory command can be used to install special user-defined commands in the controller RAM. The applicable RAM address assignments are shown in Table 1-14.

Table 1-14. RAM Address Assignments (Partial List)

RAM Location	Assignment*
8000-80DC	Workspace and RAM variable storage locations
80CA	RAM starting address for command code 5. Normally assigned for command timeout routine
80CC	Location for inhibiting command trace option by loading zeros. Inhibiting the trace option frees locations 8140-81FE for other uses
80DE-80FE	Unused RAM space
8100-8134	Scratchpad for sector numbering table used by Write Format and Write Interlaced Sector Format commands
8140-81FE	Command trace table; may be freed by writing zeros to address 80CC

Note:

* Any controller reset or self-test execution forces all addresses back to default assignments.

To install a user-defined command, the programmer should:

1. Code the new command and reduce to 9900 machine language form. Count the number of locations required for the machine and decide how to map it into the available RAM space. Note the command should return the controller to the idle sequence by using a BLWP instruction to hexadecimal address 54 (IDLVEC). Examine the 9900 control program listing for other program segments that may be useful in implementing the special command.

2. Use the Write Controller Memory command to;

   a. Write the starting address for the special command code to location 80CA.

   b. Write zeros to controller RAM location 80CC (steps a and b may be performed with a single Write Controller Memory command).

   c. Transfer the machine code to RAM, starting at the address loaded into location 80CA.

3. Execute the special command using command code 5.

4. Use the Read Controller Memory command to assist in checking out the new command. An AMPL test system, if available, is also very useful for checking out the details of command execution.

1.10.7 Read Controller Memory (110 — Extended)

This command is reserved for diagnostic purposes. It is used to read back values from the controller on-board ROM and RAM locations. An address map in Section 2 of this manual shows on-board memory assignment; the control program listing in Appendix B provides detailed information about memory assignments.

The cylinder address in control word W3 serves as the internal address field for this operation. Word count and 990 main memory (TILINE) buffer address control are similar to a Read Data operation.

1.10.8 Extended Test Commands (111 — Extended)

This command causes the controller to execute one of its extended self-test sections, as specified by a value in W3. Failure of a self-test is indicated by all ones (FF), returned in the right byte of W7, and an error code in the right byte of W2. The self-tests are:

Hexadecimal Test Number	Description
0000	Microprocessor
0001	On-board RAM
0002	ROM
0003	PIA
0004	Slave register
0005	TILINE master/busy slave
0006	Data separator/encoder

Hexadecimal Test Number	Description
0007	Drive interface
0008	TILINE interrupt
0009	Extended disk I/F (loopback)
000A	VCO adjust
000B	Drive head test
000C	Tap test
000D	Diagnostic Delay

CAUTION

Certain of these extended test commands will hang the controller in a test loop until an I/O reset or power reset aborts the test. Also, some of these tests are capable of destroying diskette data.

Refer to Table 3-4 for additional self-test information.

1.11 RECORDING FORMAT

The recording media is a 200-mm (7.88-in.) diameter flexible plastic disk which is coated on one or both surfaces with a thin layer of magnetic oxide. The disk is permanently encased in a 203 millimeter (8 inch) square plastic protective jacket. An inner-surface coating in the jacket wipes the disk clean of dust as it rotates within the jacket. A large central cutout in the jacket allows the drive spindle to clamp the disk for rotation. The whole package is called a diskette.

A manufacturer's tag identifies the top of the diskette and is used to select orientation for installing the diskette (see Section 2). Oval top and bottom cutouts allow the read/write heads access to the recording surface. The recording surface of a single-sided diskette, surface 0, is the bottom surface of the rotating disk. On a DSDD diskette, the lower surface is called surface 0, (to be consistent with the single-sided diskette) and the upper surface is side 1.

A round cutout in the diskette jacket allows an optical transducer in the drive to generate a pulse when a smaller hole in the disk rotates past the cutout. This index pulse occurs once per revolution. It is used to verify that the disk is rotating, and it serves as a reference for formatting soft sectors on the disk.

The position of the index hole cutout in the diskette jacket identifies the type of diskette. As shown in Figure 1-21, the index hole cutout of a single-sided diskette is very close to the imaginary diskette centerline that runs through the center of the oval recording cutout and the spindle center point. The cutout is displaced about 16 millimeters (5/8 inch) to the right of the centerline for a DSDD diskette.

The FD1000 drive has index sensors at both positions and determines diskette type by which sensor detects index holes when the disk is spinning. A diskette type status signal from the drive to the controller selects the correct recording format.

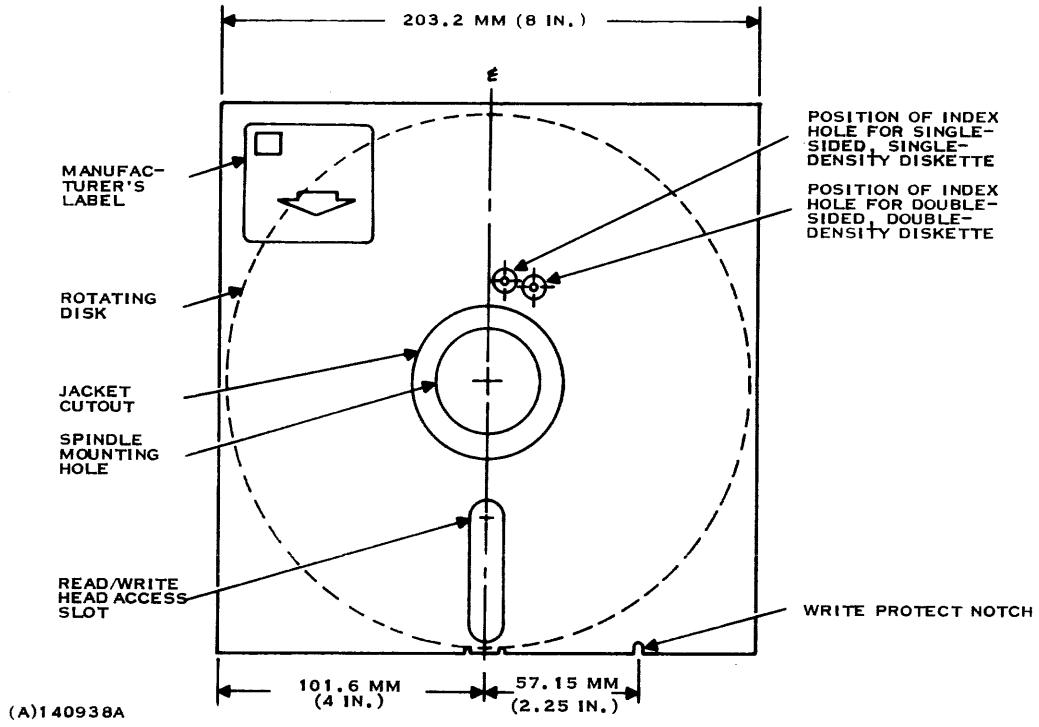


Figure 1-21. Single-Sided and Double-Sided Diskettes

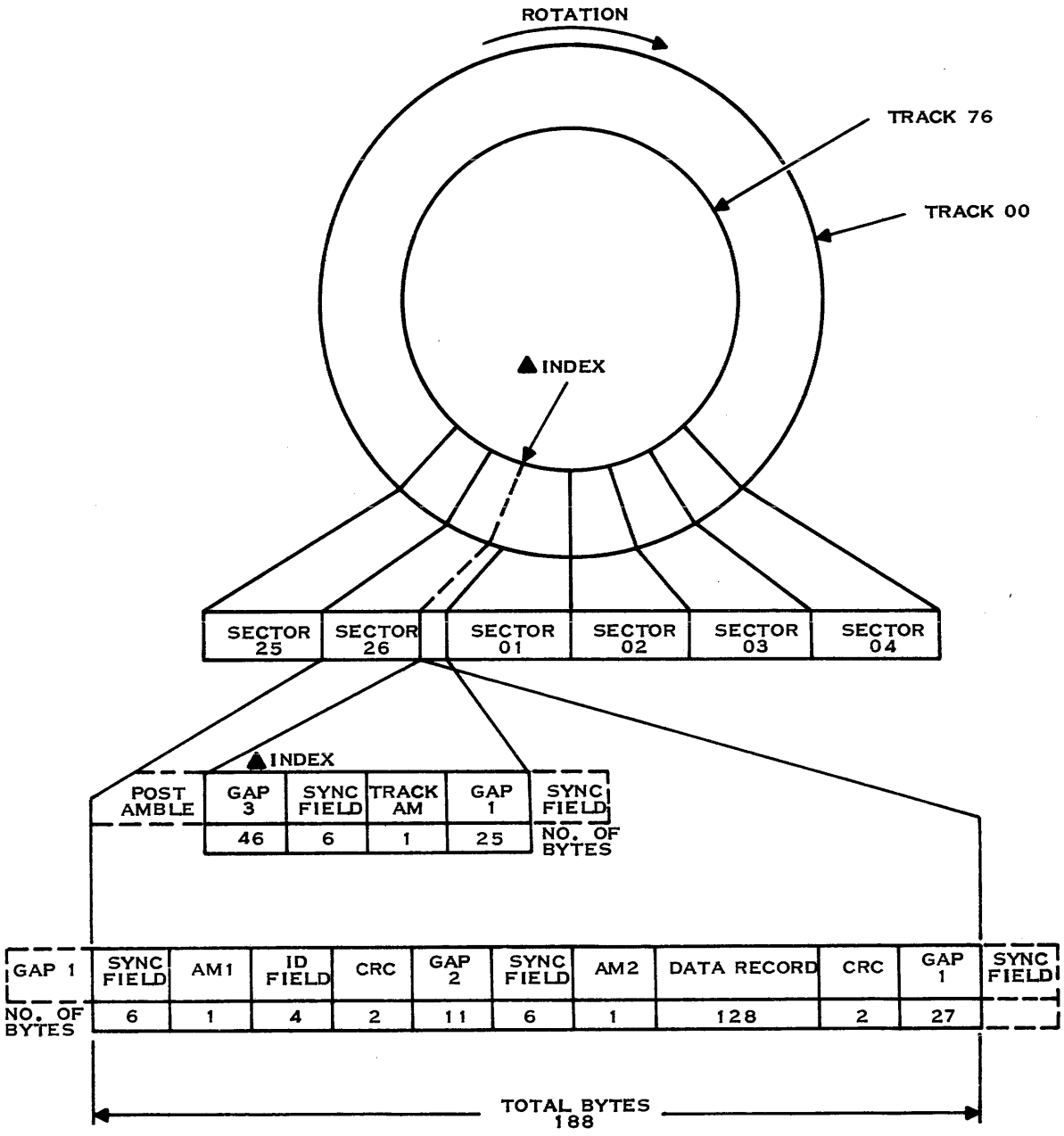
A single hardware-generated index mark occurs on each revolution. Each of the 26 sectors starts with an identification (ID) header which includes a read synchronization pattern, ID address mark, and two ID words that identify the track, surface, record number, and the number of data bytes in the record. A third header word contains a CRC word that checks the integrity of the two ID words.

A diskette is write protected by means of a notch or hole in the diskette jacket 57 millimeters (2.25 inch) from the read/write head access slot. If the hole is open, the disk is write protected and may not be written upon. A small tab (supplied with a pack of diskettes) may be taped over the hole or notch to enable writing on the diskette.

1.11.1 Single-Density Diskette Format

The FD1000 flexible disk system records SSSD diskettes using frequency modulation (FM) techniques. SSSD diskettes are interchangeable with diskettes recorded in an FD800 floppy disk system. Each track and each record is recorded in the standard IBM 3740 (128 byte/sector) format. Track allocation and use is a function of the operating system software. Texas Instruments operating system software does not allocate tracks per the IBM conventions. IBM conversion utilities included in the TI operating systems allow the user to transport diskettes between IBM and TI systems.

Track formatting of the single-sided diskette is illustrated in Figure 1-22. The diskette is initialized with 77 tracks (00 to 76), each segmented into 26 sectors (1 to 26) of 128 data bytes.



(A) 140937

Figure 1-22. Single-Density Diskette Format

A gap separates the end of the header and the beginning of the data. The data area consists of a read synchronization pattern, a data address mark, 128 data bytes (64 words), and a CRC word that checks the integrity of the data. An interrecord gap follows the data field. The SSSD format is summarized in Table 1-15.

1.11.2 Double-Density Diskette Format

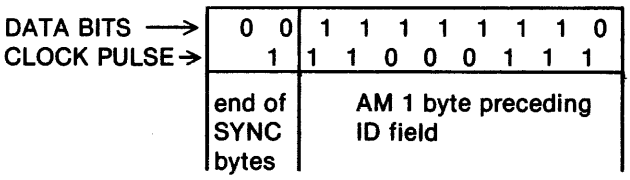
The flexible disk system records DSDD diskettes using modified FM (MFM) encoding techniques. The diskette is recorded in a Texas Instruments format, Figure 1-23. The diskette is organized into 77 cylinders that consist of a track on the lower surface (side 0) and the corresponding track on the upper surface (side 1).

A single hardware-generated index mark occurs during each revolution. Each of the 26 sectors starts with an ID header that includes a read synchronization pattern, ID address mark, and three words that identify the surface, cylinder, number of records per track (26), record number, and byte count per record (288 bytes/record). A CRC word verifies the integrity of the header.

A gap separates the data area from the end of the ID header. The data area consists of a read synchronization pattern, a data address mark and 288 bytes (144 words) of data followed by a CRC word that verifies data integrity. The DSDD format is summarized in Table 1-16.

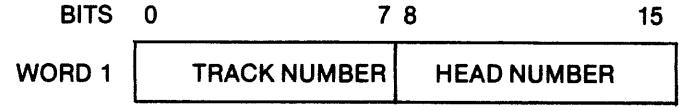
Table 1-15. FD800 Diskette Recording Format Summary

Field	Explanation
SYNC (Synchronization)	Each SYNC field contains six bytes of zeros. The SYNC field synchronizes the disk drive circuitry to the information being read from the diskette.
AM 1 (ID Address mark)	Address mark 1 consists of a unique byte that violates the normal FM encoding rules. AM 1 precedes the ID field and has missing clock pulses as indicated by zeros in the clock pattern of the following diagram.



Data pattern = >FE Clock pattern = >C7

ID (Identification)	The ID field contains four bytes (two words) that identify the address and size of the sector. These four bytes are as follows:



In word 1, the track number will be a maximum of 76, or >00 to >4C. The head number will always be 00.

Table 1-15. FD800 Diskette Recording Format Summary (Continued)

Field	Explanation
	BITS 0 7 8 15 WORD 2 | RECORD NUMBER | RECORD LENGTH In word 2, the record number will be a maximum of 26, or >01 to >1A. The record length is 128 bytes and is indicated as 00.
CRC (Cyclic redundancy check)	There are two CRC words, one following the ID field and one following the data record. The CRC word following the ID field is generated when formatting the diskette. The contents of this CRC word is determined by the header data, AM 1 thru ID 2. The contents of the data CRC word is determined by the data address mark (AM 2) and the data record. CRC words are recalculated during a read operation. The results of each recalculation are checked against the recorded CRC words. If the CRC words compare, the ID or data record was read correctly.
GAP 2 (Intrarecord gap)	The GAP 2 field consists of 11 bytes of >00s.
AM 2 (Data address mark)	The AM 2 field is either >FB or >F8. Field >FB identifies the field that follows as a data record. Field >F8 identifies the field that follows as a control record (IBM deleted data). AM 2 has missing clock pulses as indicated by zeros in the clock pattern of the following diagram. DATA BITS → 0 0 1 1 1 1 1 0 X X CLOCK PULSE → 1 1 1 0 0 0 1 1 1 end of SYNC bytes | AM 2 byte preceding data field XX = 11 for >FB, 00 for >F8 Clock pattern = >C7

Table 1-15. FD800 Diskette Recording Format Summary (Continued)

Field	Explanation
DATA RECORD	The DATA RECORD field contains 128 bytes of data or control records. In a control record, the first byte is used to indicate defective or deleted records as follows: , = Defective Record (Alternate Physical Record Relocation) D = Deleted Record F = Defective Record (Sequential Physical Record Relocation)
GAP 1	The GAP 1 field consists of two bytes of >00s followed by a variable number of >00 bytes depending on the diskette speed and record length.
GAP 3	The GAP 3 field consists of a variable number of >00 bytes (nominally 46 bytes).
AM 3 (Track address mark)	The AM 3 field is always >FC. It identifies the start of a track (referenced to the index hole in the diskette). AM 3 has missing clock pulses as indicated by zeros in the clock pattern of the following diagram. DATA BITS ⟶ 0 0 1 1 1 1 1 1 0 0 CLOCK PULSE⟩ 1 1 1 0 1 0 1 1 1 end of SYNC bytes | AM 3 byte Data pattern = >FC Clock pattern = >D7

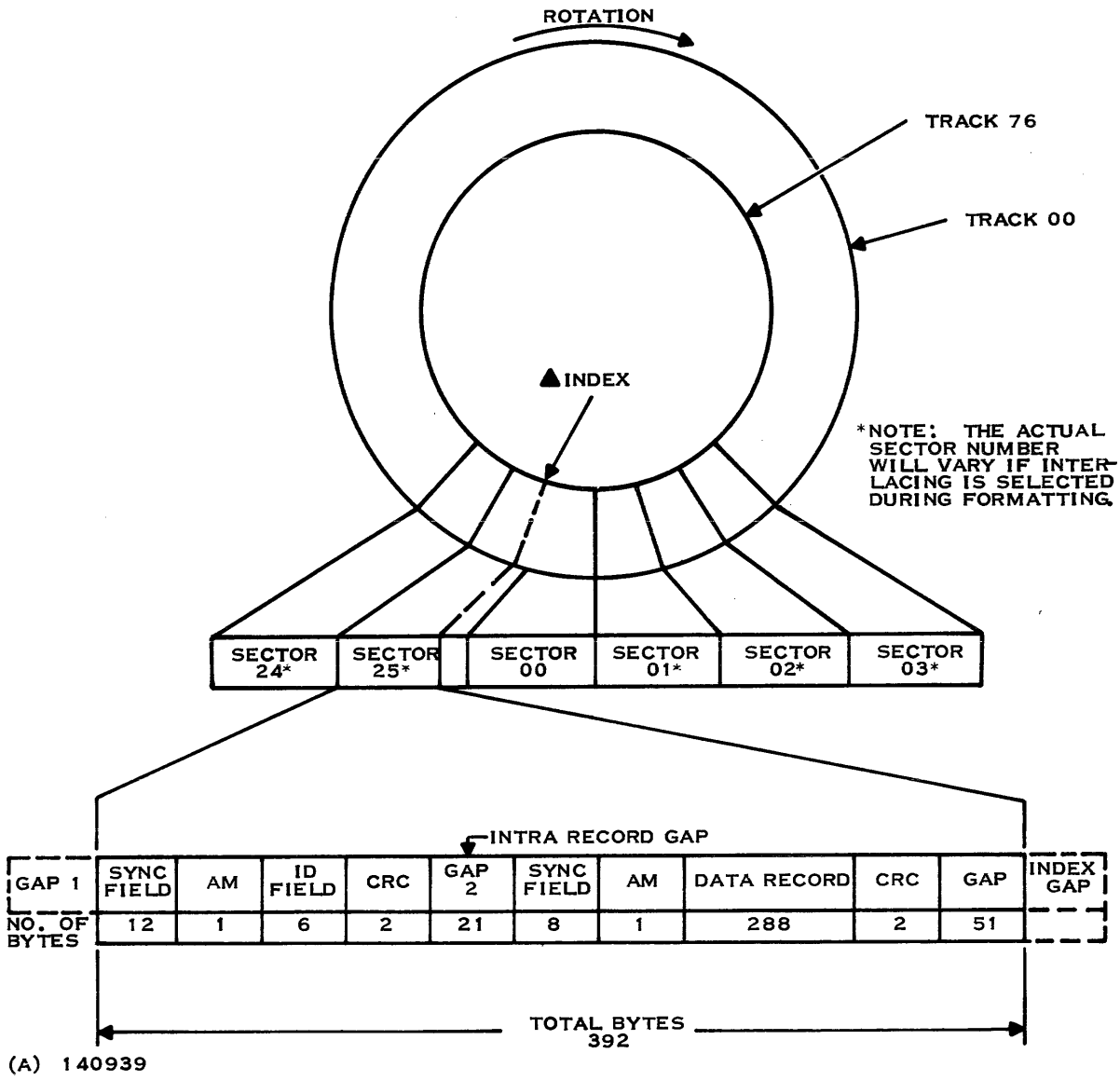
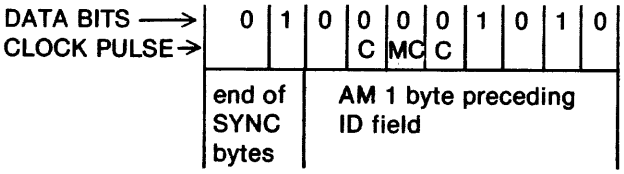


Figure 1-23. Double-Density Diskette Format

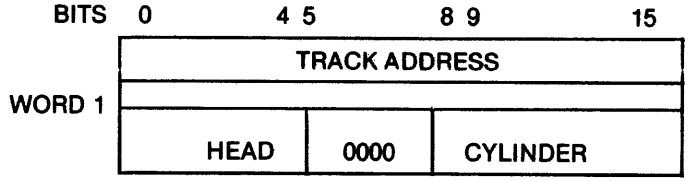
Table 1-16. FD1000 Diskette Recording Format Summary

Field	Explanation
SYNC (Synchronization)	There are two synchronization fields, a 12-byte SYNC field for the sector ID header and an 8-byte SYNC field for the data record. Separate SYNC fields are required because sector headers and data are written at different times (and possibly on different machines). There is no predictable phase relationship between clocks generated at these different times. The SYNC fields provide a clock/data pattern to lock the data separator phase lock loop to the records on the diskette. The SYNC pattern is 01010101 (>55).
AM 1 (Address Mark 1)	Address mark 1 consists of one unique byte that violates the normal MFM encoding rules to allow synchronization on both bit and byte levels. AM 1 precedes the ID field and has a data value of 00001010 with no transition for the third zero marked MC in the following diagram.

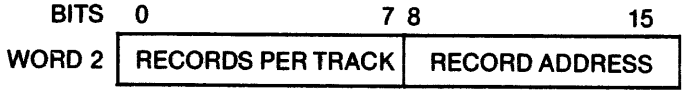


C = clock pulse MC = missing clock pulse normally provided for MFM encoding

ID (Identification)	The identification field contains six bytes (three words) as follows:



Word 1 is the track address on which this ID is recorded. The head address is in bits 1 through 4 and the cylinder address is in bits 9 through 15. Bits 5 through 8 are always zero.



Word 2 contains the number of records (sectors) per track and the record address. The maximum record address is >19.

Table 1-16. FD1000 Diskette Recording Format Summary (Continued)

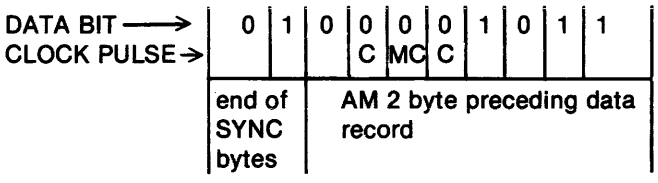
Field	Explanation
	Word 3 contains the byte counter that defines the size of the record following the recorded ID. All records on a track are of the same fixed length of 288 bytes. The byte counter of the ID word will be checked by the controller as part of the ID location check during any data transfer operation.
CRC (Cyclic Redundancy Check)	The CRC character is the 16-bit remainder value generated, on a WRITE DATA or FORMAT operation, by performing a polynomial division of the string of bits that includes the address mark and the data field. The polynomial divisor is selected to provide the best error detection probability. The selected divisor is the standard CRC-CCITT polynomial described with the CRC logic (Section 2). To further reduce the possibility of a false CRC error, a partial remainder value of >FFFF is preset into the CRC generator prior to any CRC generation or checking operation. During an ID location or READ DATA data field transfer operation, the address mark and following data, including the previously written CRC value are again divided by the divisor polynomial. If the data does not contain any errors, the resulting remainder value in the CRC generator will be 0000. Any other value indicates that the data integrity has been lost.
GAP 2 (Intrarecord gap)	An intrarecord gap consisting of 21 bytes of >55 occurs after a WRITE FORMAT command. The gap can pick up undefined bits after write data commands because the write turn-on transition occurs in this gap.
AM 2 (Address mark 2)	Address mark 2 consists of one unique byte that violates the normal MFM encoding rules to allow synchronization on both bit and byte levels. AM 2 precedes the data record and has a data value of 00001011 with no transition for the third zero (marked MC on the following diagram).  C = clock pulse MC = missing clock pulse normally provided for MFM encoding
DATA RECORD	The data is recorded as 16 bit words following the data address mark. The data length is fixed at 144 words (288 bytes). The data is always followed by a CRC field.

Table 1-16. FD1000 Diskette Recording Format Summary (Continued)

Field	Explanation
GAP 3 (Interrecord gap)	Gap 3 is an interrecord gap called the postamble. This gap compensates for rotation speed timing tolerances and prevents writing into the ID area of the next record. When the FORMAT command is executed, the controller writes 51 bytes of >55 (816 microseconds) in the gap.
INDEX GAP (Gap 1)	The index gap length depends upon the actual speed of the drive. This gap compensates for the speed tolerance.

2

Theory of Operation

This section describes the theory of operation for the Model FD1000 Flexible Disk Controller (TFDC) and the International Chassis Power Supply. Two versions of the TFDC exist, the multilayer version (2261690-1) and the fineline version (2267295-1). The International Chassis Power Supply also exists in two versions, the original version (2261695-1) and the buffered version (2269977-1).

Descriptions in this section are based on the following drawings in Appendixes E and F:

Device	Assembly Drawing	Logic Drawing
Multilayer Controller	2261690	2261695
Fineline Controller	2267295	2267297
Int. Chassis Power Supply	2261695	2265018
Buffered Int. Chassis Power Supply	2269977	2269979

The differences between versions of the TFDC are basically layout changes due to a different logic board construction. There is only a minor functional difference, due to one added flip-flop (F/F) in the fineline TFDC. The logic diagrams correspond sheet-for-sheet. Logic diagram sheet references in the figures or text apply to both controllers, unless specified otherwise.

The differences between versions of the International Chassis Power Supply are more extensive. The changes involve a redesign of the power supply and changes in line termination, drive selection options and signal buffering. The logic drawing sheet numbers do not correspond. Due to the magnitude of the differences, separate descriptions are provided at the detailed theory level.

2.1 TFDC INTERFACES

There are two types of FD1000 flexible disk systems: those with the domestic chassis, and those with the international chassis. The signals exchanged between the controller and the 990 computer are identical for either system. A domestic system uses a daisy-chain local bus for drive/controller communication as shown in Figure 2-1. The control and data signal paths run directly between the drive electronics and the controller.

An international system, Figure 2-2, uses one or both of the controller remote ports. Status and control signals are multiplexed into serial pulse streams for transmission over the remote bus. The power supply/interface board in the international chassis performs status signal multiplexing and control signal demultiplexing for one or two drive units. A local intrachassis bus connects the drives to the power supply/interface board. Except for the names, these signals are identical to the local bus signals of a domestic system. These signals are described in more detail in the logic descriptions of the TFDC input/output circuits.

2.1.1 Controller to 990 Computer Interface

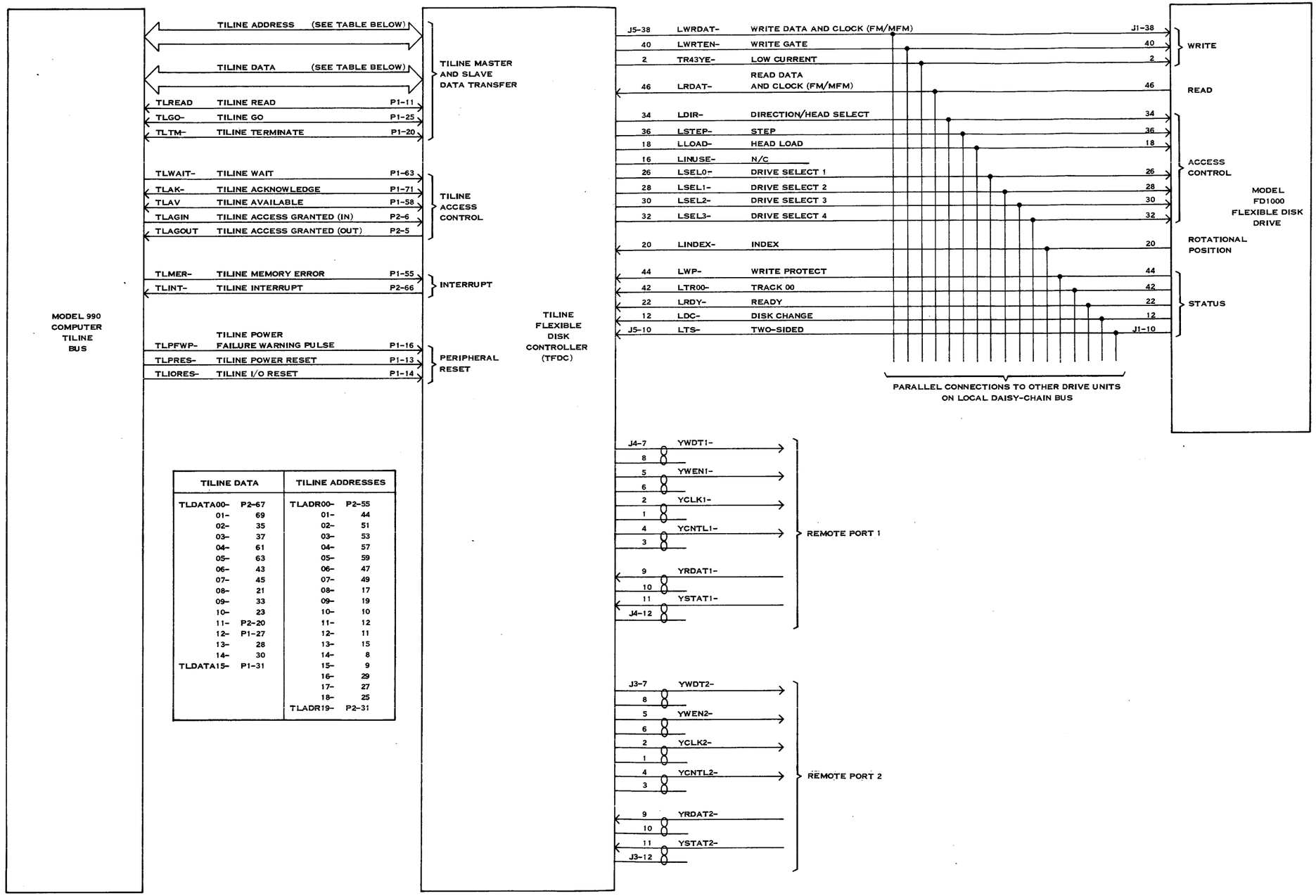
Refer to the left side of either Figure 2-1 or Figure 2-2 which shows the TILINE signal flow between the 990 computer and the disk controller. The drawing shows these signals grouped according to function.

The TILINE master and slave data transfer signals include:

- TILINE Address. Twenty bidirectional address lines used to define the memory location of data for a read or write operation.
- TILINE Data. Sixteen bidirectional lines used to transfer data between the TILINE and the controller.
- TILINE Read. This signal commands a read when high and a write when low. It is provided by the TILINE master device that currently has control of the bus.
- TILINE Go. Data transfers between the TILINE and the disk controller are initiated by the high to low transition of this signal.
- TILINE Terminate. A signal that is generated by a slave device to indicate completion of the operation.

The TILINE access control signals coordinate the orderly sharing of bus resources among competing TILINE master devices. These signals include:

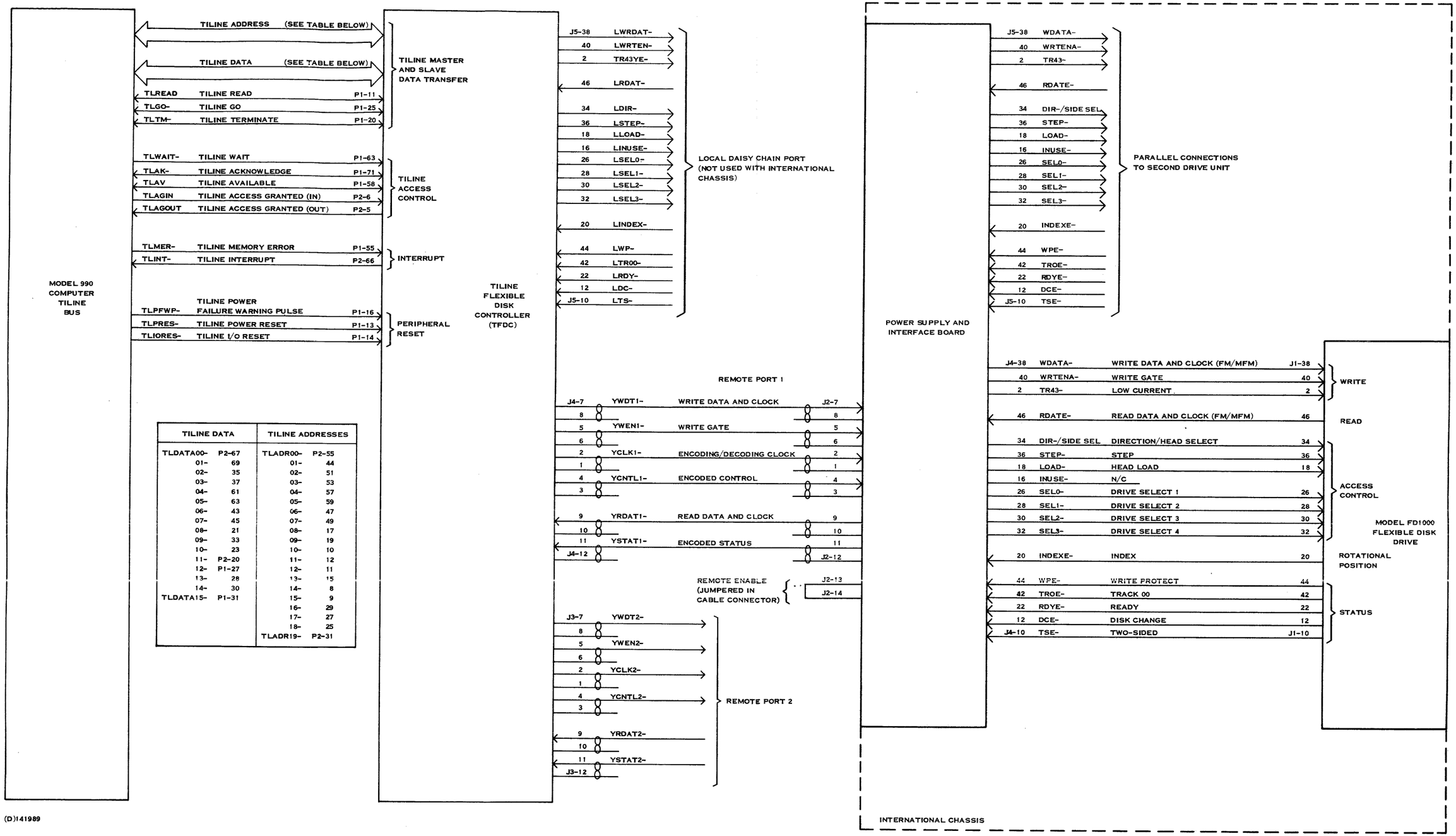
- TILINE Wait. The TILINE wait signal temporarily suspends the controller from using the bus.
- TILINE Acknowledge. When low, this signal indicates that some device has requested bus access, has acquired the next available cycle, and is waiting for the bus to become available. When high, it indicates that the next bus cycle is not reserved.
- TILINE Access Granted (in). When high, this signal indicates that no higher priority master has requested use of the TILINE. When low, it prevents the controller from gaining access to the bus.
- TILINE Access Granted (out). When low, this signal indicates that the controller, or a higher priority controller, is requesting use of the bus, preventing any lower priority controller from starting a bus request cycle.



TILINE DATA		TILINE ADDRESSES	
TLDATA00-	P2-67	TLADR00-	P2-55
01-	69	01-	44
02-	35	02-	51
03-	37	03-	53
04-	61	04-	57
05-	63	05-	59
06-	43	06-	47
07-	45	07-	49
08-	21	08-	17
09-	33	09-	19
10-	23	10-	10
11-	P2-20	11-	12
12-	P1-27	12-	11
13-	28	13-	15
14-	30	14-	8
TLDATA15-	P1-31	15-	9
		16-	29
		17-	27
		18-	25
		TLADR19-	P2-31

(C)141501

Figure 2-1. Interface Signals — FD1000 System with Domestic Chassis



TILINE DATA		TILINE ADDRESSES	
TLDATA00-	P2-67	TLADR00-	P2-55
01-	69	01-	44
02-	35	02-	51
03-	37	03-	53
04-	61	04-	57
05-	63	05-	59
06-	43	06-	47
07-	45	07-	49
08-	21	08-	17
09-	33	09-	19
10-	23	10-	10
11-	P2-20	11-	12
12-	P1-27	12-	11
13-	28	13-	15
14-	30	14-	8
TLDATA15-	P1-31	15-	9
		16-	29
		17-	27
		18-	25
		TLADR19-	P2-31

(D)141989

Figure 2-2. Interface Signals — FD1000 A/B System with International Chassis

There are two data interrupts related to controller operation:

- TILINE Interrupt. This is the general interrupt from the controller slot location to the 990 processor.

- TILINE Memory Error. This interrupt is generated by 990 main memory if an uncorrectable error is detected during a memory read operation. The TFDC generates a TILINE memory error if the TILINE data transfer test fails preceding a disk read operation.

The peripheral reset signals clear the controller and the drives to safe states in the event of an I/O reset or a power shutdown. These signals are:

- TILINE Power Failure Warning Pulse. This signal is a pulse preceding the power reset that indicates a power shutdown is in progress.

- TILINE Power Reset. This signal goes low to reset the controller and all other devices in the 990 chassis. It is generated as part of the computer power-down and power-up sequences.

- TILINE I/O Reset. When this signal is low, it halts and resets all input/output devices. This signal is developed by the 990 processor.

2.1.2 Drive Unit Interface Signals

The drive unit has the same input/output signal characteristics whether it is connected to the TFDC local bus port or to the intrachassis bus of the international chassis power supply/interface board. The drive input/output signals fall into five groups; write, read, access control, diskette rotational position (index), and drive status.

The write signals include:

- Write Data. This is a pulse waveform that is encoded to produce either FM or MFM data recording on the diskette. The code is self-clocking.

- Write Gate. This is a control signal that allows the write drivers to supply current to the read/write heads

- Low Current. This write signal commands the drive to reduce the amount of drive current. It is used to improve data recovery margins when recording on the inner tracks.

The read signal is a serial bit stream that represents encoded data (including clock pulses) read from the diskette.

The access control signals include the signals necessary to select a drive unit, select a head, and step the head carriage to the desired track. These signals are:

- Direction/Head Select. This is a dual-purpose signal that determines the direction (in or out) of a step signal when positioning the heads, and also selects the lower or upper head when reading or writing.

- Step. A single-step command, this signal moves the heads by one step in the direction determined by the direction/head select signal.

- Drive Select 1-4. This signal selects one of the four possible drives for control, status, and data signal interchange.

The rotational position signal is:

- Index. This signal is a single pulse indicating that the index mark has passed the index sensor. It serves as the initial reference for soft-sectoring of the diskette.

The drive status signals are:

- Write Protect. This signal indicates that the write protect notch of the diskette is exposed, inhibiting write current.
- Track 00. This signal indicates that the head carriage is positioned at track 0, and serves as a physical reference for track positioning.
- Ready. This signal indicates that the selected drive is ready to accept read, write, or positioning commmands.
- Disk Change. The disk change signal indicates that the drive has gone to a not ready condition when not selected. Indicates that the drive power has been cycled or that the drive door has been opened.
- Two-sided. This is a diskette type-identification signal (SSSD or DSDD).

2.1.3 Remote Port Interface Signals

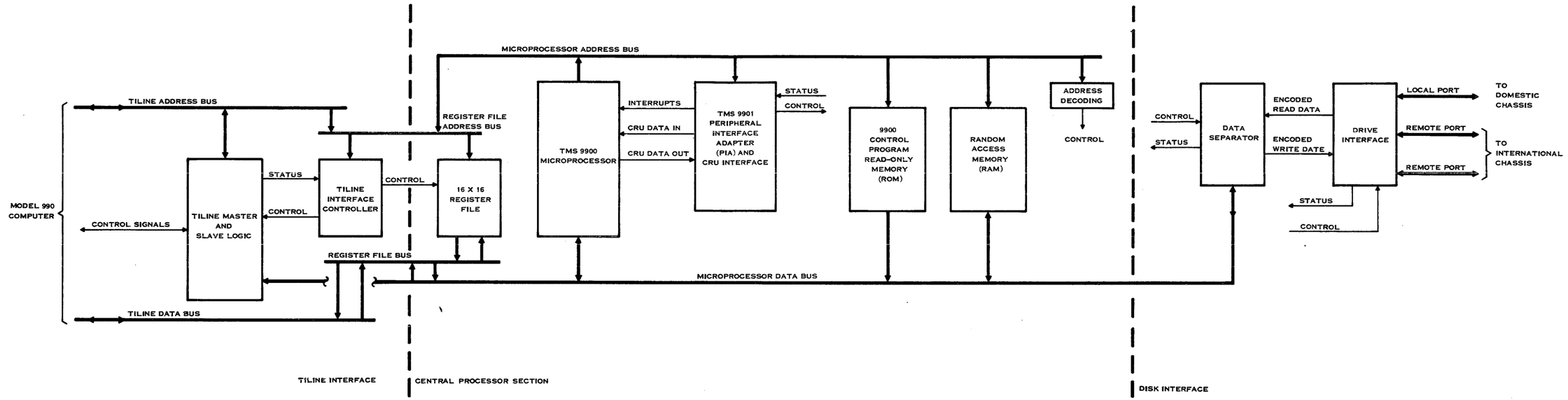
The remote port interface signals are exchanged between the TFDC remote port and the international chassis remote port. These signals are multiplexed/demultiplexed to local bus equivalent signals in the ports. The remote port interface signals are:

- Write Data. Differential driver version of serial write data encoded for FM or MFM recording on the diskette.
- Read Data. Differential driver version of serial read data and clock.
- Write Enable. Differential driver version of write gate.
- Multiplexed Control Signal. Serially-encoded control signals.
- Multiplexed Status Signal. Serially-encoded drive status.
- Multiplexer/demultiplexer Clock. Reference clock for serially encoded signals.

2.2 TFDC BASIC BLOCK DIAGRAM

The TFDC is a microprocessor-based controller that manages disk control and data transfers independently of the Model 990 Computer after accepting a group of control parameters.

Figure 2-3 shows that the disk controller logic may be partitioned into three major functional groups; the TILINE interface, the central processor section, and the disk interface logic.



(D)142733

Figure 2-3. TILINE Flexible Disk Controller Simplified Block Diagram

2.2.1 TILINE Interface

The TILINE interface consists of the TILINE slave logic, the TILINE master access logic, the TILINE interface controller, and the line drivers and receivers. The slave logic is activated when the 990 processor addresses one of the eight TILINE slave addresses that are assigned to the controller. These slave addresses are dedicated to status and control words W0-W7, and are used to load control words into the register file (slave write), or to request status words from the register file (slave read). The term "slave" applies to these operations because the controller responds to an externally-supplied address and a read/write command.

The TILINE master access logic is activated by the 9900 control program to transfer data from the controller to a specified area of 990 memory. The TILINE master access logic requests and attains access to the bus and manages the handshaking interchange of control signals that accompanies each word transfer. The TILINE interface controller is a ROM-based state controller that works with the discrete logic of the master access logic and slave logic for TILINE cycle control. The TILINE interface controller also controls access to the register file and to the register file bus.

2.2.2 Central Processor Section

The central processor section uses a TMS 9900 microprocessor, associated circuits, and a permanent, on-board 9900 control program that controls execution of the operations specified by W0-W7.

The heart of the central processor section is the TMS 9900 16-bit microprocessor. The basic architecture and instruction set for the TMS 9900 apply to all computers in the 990 family. The communications register unit (CRU) input/output bus and the memory-mapped input/output capabilities of the microprocessor are used for operating sequence control. The microprocessor controls data transfer through the controller logic and over the controller internal buses, but the data path does not go through the microprocessor. The microprocessor reads drive and controller internal status information, and initiates and controls operating cycles.

The TMS 9901 peripheral interface adapter (PIA) serves as a timer, interrupt encoder, and CRU input/output register for the microprocessor.

The control program is burned into a read-only memory. This program is written in TMS 9900/990 machine language, and is documented in this manual by flowcharts, routine/subroutine descriptions, and an assembly language listing with comments.

The random access memory provides the workspace registers and temporary scratchpad storage locations required by the 9900 control program.

2.2.3 Disk Interface

The disk interface may be divided into two major blocks, the data separator and the drive interface. The drive interface consists of the line drivers and receivers that transmit and receive data, status, and control signals at the I/O ports. The drive interface also includes the remote port control signal multiplexers and status signal demultiplexers.

The data separator performs the clock recovery, bit synchronization, word synchronization, and serial-to-parallel conversion necessary to convert the serial data stream from the drive unit to the parallel format that is required by the controller internal buses and the TILINE. The data separator checks the integrity of each sector address and of the data in each sector read from the disk.

During write operations, the data separator performs parallel-to-serial conversions and the clock/data encoding to produce a serial data stream for the drive unit. The data separator also appends an error check word to each sector of data.

2.3 BUS ORGANIZATION

As shown in the TFDC basic block diagram (Figure 2-3), the controller is organized around several major buses: the TILINE address bus, TILINE data bus, register file address bus, register file data bus, microprocessor address bus, microprocessor data bus, and communications register unit (CRU) data bus.

The 20-bit TILINE address bus and the 16-bit TILINE data bus are used for all data and control word transfers between the 990 computer and the disk controller. This high-speed asynchronous bus is controlled by arbitration between competing TILINE master devices. There is no centralized bus control.

The 16-bit register file data bus is used for all TFDC data transfers to and from the TILINE data bus. A 16-word register file, addressed by the 4-bit register file address bus, may accept data from the bus or supply data to the bus. Bus gating logic allows the register file address bus to be supplied by the TILINE address bus, the microprocessor address bus, or a default (0000) address. The register file and the register file bus transfers are controlled by the TILINE interface controller.

The 15-bit microprocessor address bus is the memory address bus of the TMS 9900 microprocessor. This bus is always supplied by the microprocessor address output. The microprocessor address bus also serves as the address bus for the serial CRU bus system. The 16-bit microprocessor data bus is a bidirectional I/O bus that may be driven from several sources including the data shift register and the register file data bus, as well as the microprocessor and the memories. The TMS 9900 microprocessor controls the bus, but may be suspended by external control.

The CRU bus is a serial bus that is used by the microprocessor for relatively slow status read and control signal write operations. There is no communication between the on-board CRU bus and the 990 computer CRU bus. The microprocessor controls the CRU bus by executing special CRU input/output instructions.

The local daisy-chain bus and the remote buses used for communication with the drives and the international chassis are described with the TFDC interfaces in paragraph 2.1.

2.4 BASIC DATA FLOW

The following paragraphs describe data flow through the TFDC for three important operations.

2.4.1 Data Flow — Loading Command Words

Figure 2-4 shows the data flow involved in loading command words W0-W7 into the controller. Each command word is sent from the 990 computer central processor as a TILINE data word. The 990 processor acts as a TILINE master during these operations. It acquires control of the TILINE, supplies the TILINE address, the read/write control signal, and the word to be transmitted. The TFDC acts as a TILINE slave, decoding the address and responding to the read/write control signal by accepting the word.

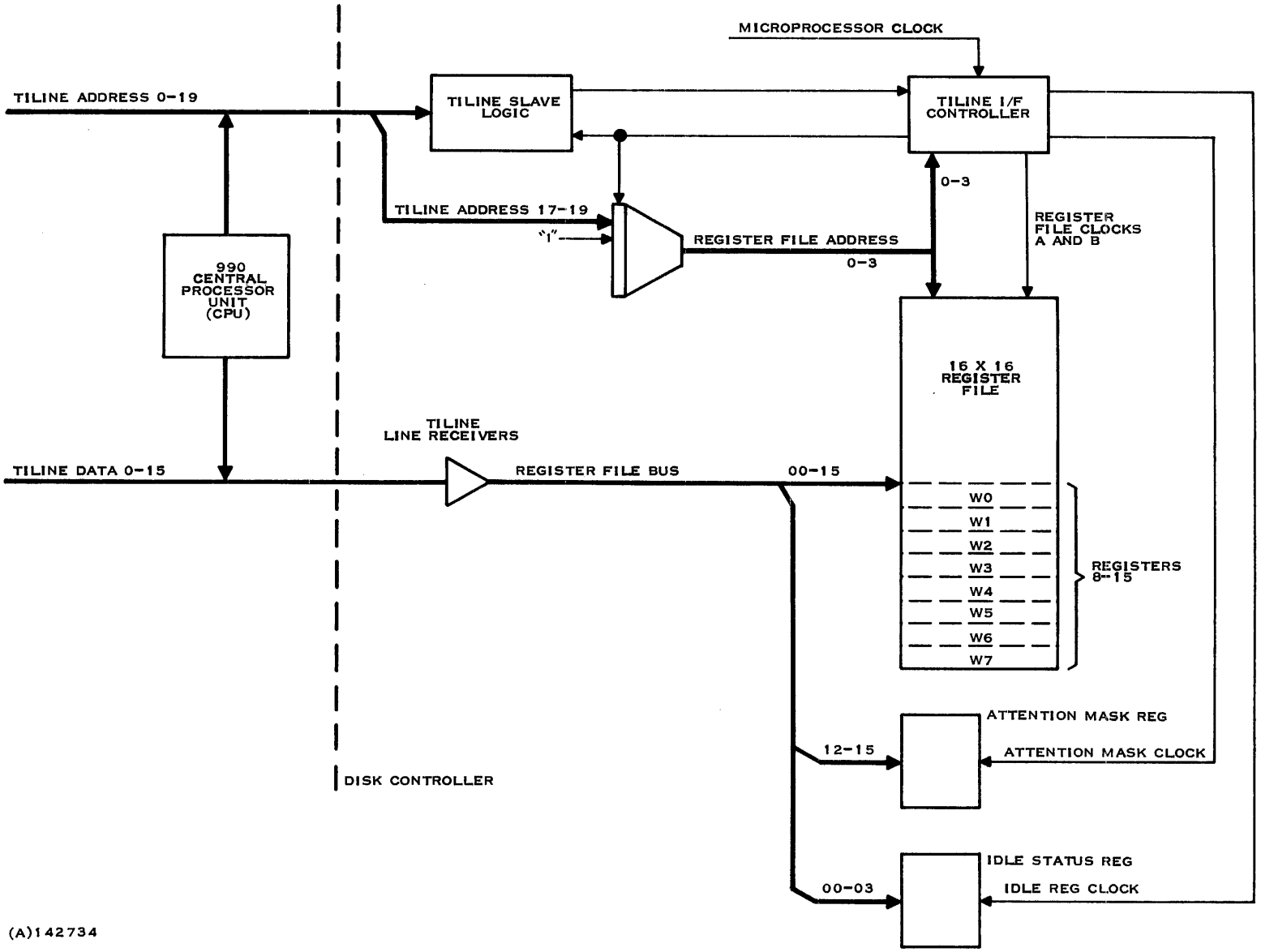


Figure 2-4. Simplified Data Flow — Loading Command Words into the TFDC

Each of the eight command words is assigned a unique TILINE address ranging from the TILINE base address to base address + 7 word addresses. The three least significant TILINE address bits are used to select one of eight registers in the 16-bit by 16-word register file. The register file address is biased by eight so that W0–W7 are stored in registers 8–15, respectively.

Two registers external to the register file are dedicated to storage of specific blocks of control information. These blocks are the four-bit attention mask from W0 and the most significant four bits of W7. These bits must be available to the controller logic at all times. The registers which store these critical values are the attention mask register and the idle status register.

Register file transfers and register file clocking are controlled by the TILINE interface controller. The TILINE interface controller may clock all of a word from the register file bus into the register file, or it may clock parts of the word into the register separately. The TILINE interface controller controls the loading of the attention mask register and the idle status register.

2.4.2 Data Flow for Disk Write Operations

The simplified data flow for a Write Data command is shown in Figure 2-5. During this write operation, the TFDC is operating under its internal control program using previously-stored command words W0–W7 as parameters.

NOTE

During a Write Data operation, the controller reads back and verifies each sector identification header prior to recording any data in that sector. Data flow for the sector ID check is omitted from the figure.

The TFDC acts as a TILINE master to read each data word from 990 memory and store it in register 0 of the register file. The initial TILINE address and the transfer word count for the operation are parameters supplied by the control words. The TMS 9900 microprocessor reads the starting address from the register file, changes the format, and loads it into the TILINE address register/counter as part of the write operation setup. The TILINE interface controller increments the address register/counter as each data word is transferred.

The operation of requesting and obtaining TILINE access, transferring one data word, and relinquishing control is called a TILINE master access cycle. Master cycles are initiated by the 9900 control program based on whether the previous data word has been loaded into the data shift register and whether the word count has been decremented to zero.

The one-word buffer provided by register 0 of the register file adapts the TILINE data transfer timing to the disk interface timing. TILINE operations are asynchronous and timing is heavily dependent on bus priorities and current bus activity levels. Disk interface timing is based on a crystal-controlled reference for write operations.

Due to the relatively slow data transfer rate of the diskette, which demands one word transfer every 32 microseconds, only one word of buffer storage is provided.

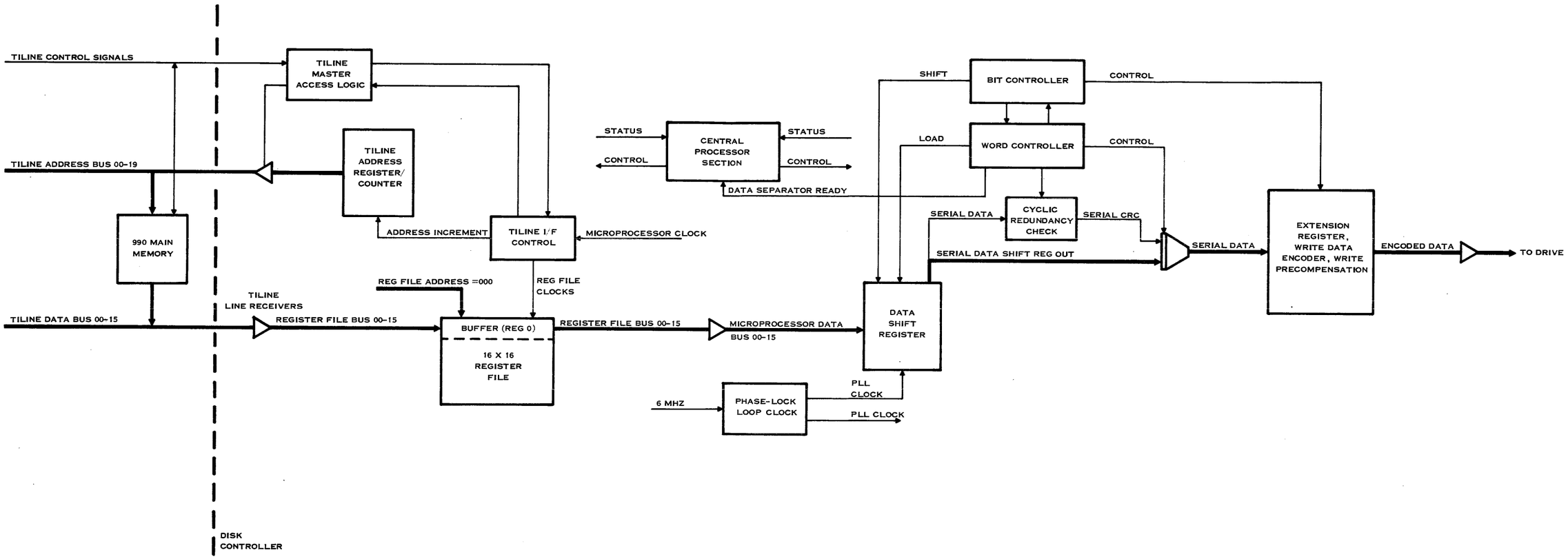


Figure 2-5. Simplified Data Flow — Disk Write Operation

Each data word is read from the register file and transferred over the microprocessor data bus to the data shift register which performs a parallel-to-serial conversion. The serial output is applied to both the CRC logic and the write data encoding logic. At the end of each data sector, the 16-bit CRC character is encoded and transmitted instead of data.

Under control of the bit and word controller, the write data encoding logic encodes the data and write clock into a format suitable for FM or MFM recording on the diskette.

2.4.3 Data Flow for Disk Read Operations

Figure 2-6 shows the simplified data flow for Read Data and Read Data Unformatted operations.

NOTE

During a Read Data operation, the TFDC reads back and verifies each sector identification header prior to reading the data from that sector. The data flow for reading the sector ID is omitted from the figure.

The data recorded on a diskette sector is preceded by a synchronization pattern and a data mark, sometimes called a data address mark. The synchronization pattern serves to lock the TFDC phase lock clock to the incoming waveform, and the data mark serves to identify the start of data.

The TFDC bit controller and word controller work together to separate clock from data and to properly divide the serial waveform into 16-bit data words.

Each data word is transferred from the data shift register to the register file. A TILINE master access cycle is initiated to transfer the word to 990 main memory.

A CRC calculation is performed on the incoming data and is compared with the CRC character recorded at write time. If they compare, the data is valid. A CRC error indicates that a problem has occurred somewhere in the writing, storing, or reading of a sector of data.

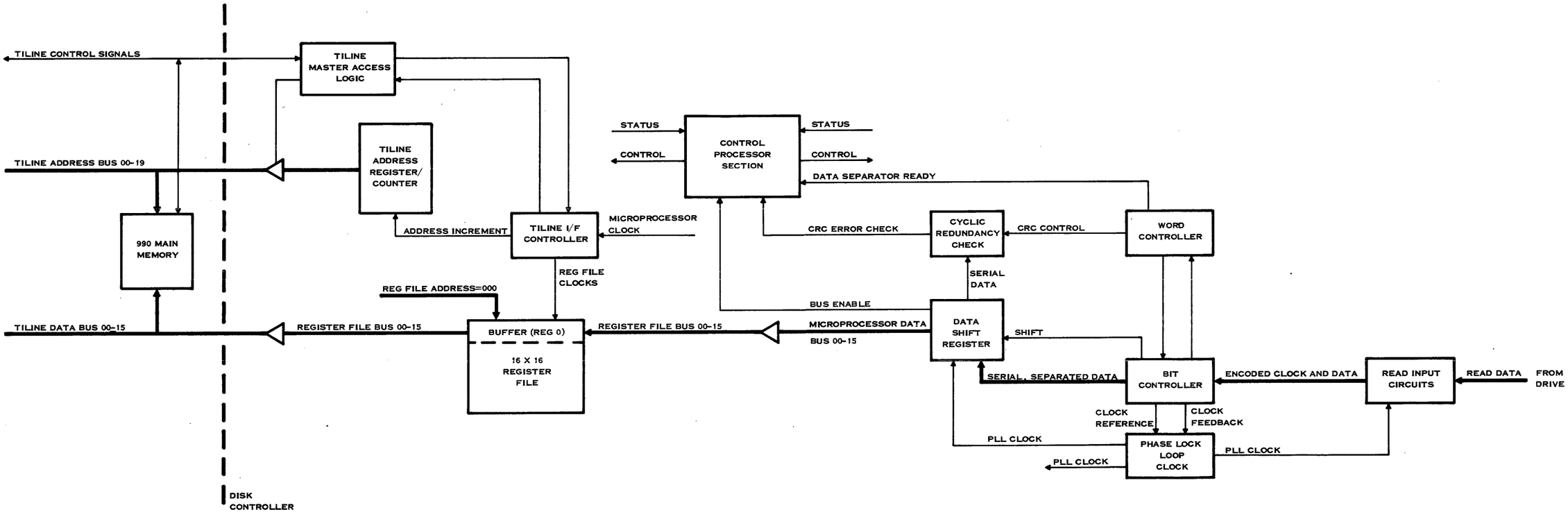
2.5 TILINE OPERATION

The TILINE high-speed data bus architecture is used to incorporate the TFDC directly into the addressable memory space of the Model 990 host computer. The TILINE is an asynchronous, high-speed, 16-bit data transfer bus with the associated control lines which transfer data between high-speed elements of the system. These elements include the CPU, the memory, the disk files and the magnetic tape transports.

Data is transferred along the TILINE data bus as 16-bit parallel words accompanied by 20-bit word addresses. The TILINE is capable of transferring approximately 50 million bits per second.

2.5.1 Master-Slave Concept

Two classes of devices connect to the TILINE: TILINE master devices that initiate data transfers, and TILINE slave devices that generate or accept data in response to some master device. Data transfers in either direction always occur between one master and one slave. The 990 CPU is an example of a master device and a memory module is an example of a slave device.



(D)142736

Figure 2-6. Simplified Data Flow — Disk Read Operation

A master device initiates data transfers on the bus, which may consist of reading data words from a slave device or writing data words to a slave. Master devices must compete with each other for access to the TILINE. A positional priority scheme is used to resolve conflicts between masters. A scheduling scheme allows a master to reserve the next TILINE access during the current operation. This overlapping reduces the overhead time to transfer bus control between masters. When a master gets access to the bus, it must place a 20-bit address on the TILINE and exchange handshaking control signals for each data word transferred to or from a slave device.

Each slave device recognizes a specific range of addresses and is activated only when the 20-bit TILINE address falls within that range. Pencil switches on the logic board of the slave device set the starting address, called the TILINE base address. The slave device accepts TILINE addresses that range from the TILINE base address to an upper limit determined by the nature of the slave. For example, an 8K memory module would respond to addresses from the TILINE base address to the base address + 1FFF.

The TFDC is both a master and a slave device. It acts as a slave when the computer reads or writes control words W0–W7. These control words specify the parameters of an operation and initiate the operation when they are written to the TFDC. They supply disk and previous operation status when read from the controller. Control words W0–W7 are assigned eight consecutive TILINE addresses, from the switch-selected TILINE base address to TILINE base address + 7.

The controller acts as a master when it performs the disk-to-memory or memory-to-disk data transfers specified by the control words. Once the controller operation has been initiated, it operates independently and competes with other masters for bus access each time it has to transfer a data word to or from memory.

2.5.2 TILINE Peripheral Control Space (TPCS)

The TPCS is a range of TILINE slave addresses reserved for assignment to peripheral device controllers such as the TFDC. The range includes 512 word addresses, extending from FFC00 to FFDFF. These addresses correspond to CPU byte addresses F800 to FBFE.

A CPU byte address in this range may be easily converted to a TILINE address by preceding the CPU byte address by 1F (e.g., F800 to 1FF800), converting to binary, deleting the LSB, and reconverting to hexadecimal form.

Each peripheral controller is assigned a block of addresses in the TPCS. These addresses are used for the control and status words which set up and monitor the peripheral controller operations. The flexible disk controller only requires eight slave addresses for control and status words W0–W7.

2.5.3 TILINE Interface Signals

The 48 signals comprising the TILINE interface are shown in Figure 2-7 and defined in Table 2-1.

2.5.4 TILINE Bus Timing-Write Cycle

Figure 2-8 is a timing diagram for a TILINE write cycle. It applies to any TILINE master and slave device but does not include the operations necessary for the master to achieve access to the bus.

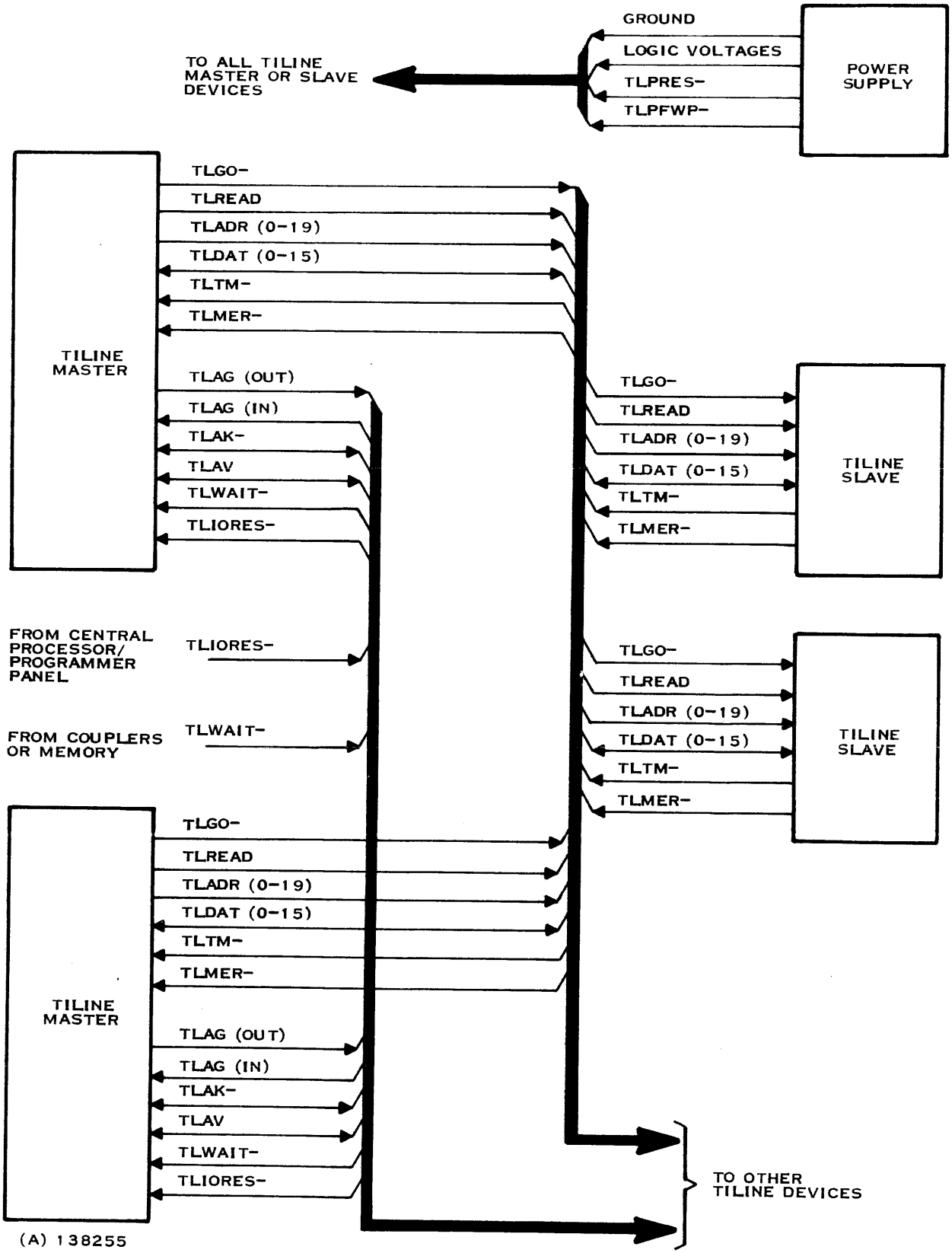


Figure 2-7. TILINE Interface Signals

Table 2-1. TILINE Signal Definitions

Signature	Pin No.	Definition
TLGO–	P1-25	TILINE Go: Initiates all data transfers when transition from high (3.0V) to low (1.0V) occurs. See note 1.
TLREAD	P1-11	TILINE Read: When high (3.0V) designates a read from SLAVE operation; when low (1.0V) designates a write to SLAVE operation. See note 1.
TLADR00–	P2-55	TILINE Address to define the location of data during a fetch or store operation. When high (≥2.0V) the corresponding address bit is a zero; when low (≤0.8V) the corresponding address bit is a one. See note 2.
01–	P2-44	
02–	P2-51	
03–	P2-53	
04–	P2-57	
05–	P2-59	
06–	P2-47	
07–	P2-49	
08–	P2-17	
09–	P2-19	
10–	P2-10	
11–	P2-12	
12–	P2-11	
13–	P2-15	
14–	P2-8	
15–	P2-9	
16–	P2-29	
17–	P2-27	
18–	P2-25	
TLADR19–	P2-31	
TLDAT00–	P2-67	TILINE Data: Bidirectional data lines that when high (≥2.0V) represent zero data bits, and when low (≤0.8V) represent one data bit. See note 2.
01–	P2-69	
02–	P2-35	
03–	P2-37	
04–	P2-61	
05–	P2-63	
06–	P2-43	
07–	P2-45	
08–	P2-21	
09–	P2-33	
10–	P2-23	
11–	P2-20	
12–	P1-27	
13–	P1-28	
14–	P1-30	
TLDAT15–	P1-31	
TLTM–	P1-20	TILINE Terminate: When low (1.0V) indicates that the SLAVE device has completed the requested operation. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 2-1. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLMER–	P1-55	TILINE Memory Error: When low (≤0.8V) indicates that a nonrecoverable error has occurred during a memory read operation. See note 2.
TLAG (in)	P2-6	TILINE Access Granted: When high (≥2.0V), this signal indicates that no higher priority device has requested use of the TILINE. When low (≤0.8V), this signal prevents the receiving device from gaining access to the TILINE bus.
TLAG (out)	P2-5	TILINE Access Granted: When high (≥2.0V), this signal indicates that neither the sending device nor any higher priority device is requesting use of the TILINE. When low (≤0.8V), this signal indicates that either the sending device or some higher priority device is requesting use of the TILINE bus and prevents all lower priority devices from gaining access to the bus.
TLAK–	P1-71	TILINE Acknowledge: When high (3.0V), this signal indicates that no TILINE device has been recognized as the next device to use the TILINE. When low (1.0V), this signal indicates that some TILINE device has requested access, has been recognized, and is waiting for the bus to become available. See note 1.
TLAV	P1-58	TILINE Available: When high (3.0V), this signal indicates that no TILINE device is using the bus. When low (1.0V), this signal indicates that the TILINE bus is busy. See note 1.
TLWAIT–	P1-63	TILINE Wait: A normally high (3.0V) signal that when low (1.0V), temporarily suspends all TILINE MASTER devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest priority user. See note 1.
TLIORES–	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2.0V) signal that when low (≥0.8V), halts and resets all TILINE I/O devices. This signal is a 100 to 500 nanosecond pulse generated by the RESET switch on the control console or by the execution of a Reset (RSET) instruction in the AU. Driven by SN7437; Received by 2 (maximum standard SN74- loads per slot).
TLPRES–	P1-13 P2-13	TILINE Power Reset: A normally high (≥2.0V) signal that goes low (≥0.8V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 microseconds before dc voltages begin to fail during power-down, and until dc voltages are stable during power-up. Driven by 80-milliampere open-collector driver (160 milliamperes with 40-ampere power supply).
TLPFWP–	P1-16 P2-16	TILINE Power Failure Warning Pulse: A 7.0 millisecond pulse preceding TLPRES—(2.0 millisecond in 17-slot chassis). When low (≤0.8V), this signal indicates that a power-down sequence is in progress, allowing the AU to perform its power failure interrupt subroutine. Driven by SN7437; received by two, maximum, standard SN74- loads per card slot.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 2-1. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLHOLD–	P2-26	TILINE Hold Signal: A normally high (3.0V) signal that goes low (1.0V) to assert that a central processor is executing an ABS instruction. TILINE Hold prevents interference from another processor on the TILINE while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multi-processor systems. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

The master places the 20-bit slave address and the data word on the lines and sets TLREAD low to specify a write operation. The master then asserts TLGO- to initiate the operation and holds TLGO- low for the duration of the write cycle.

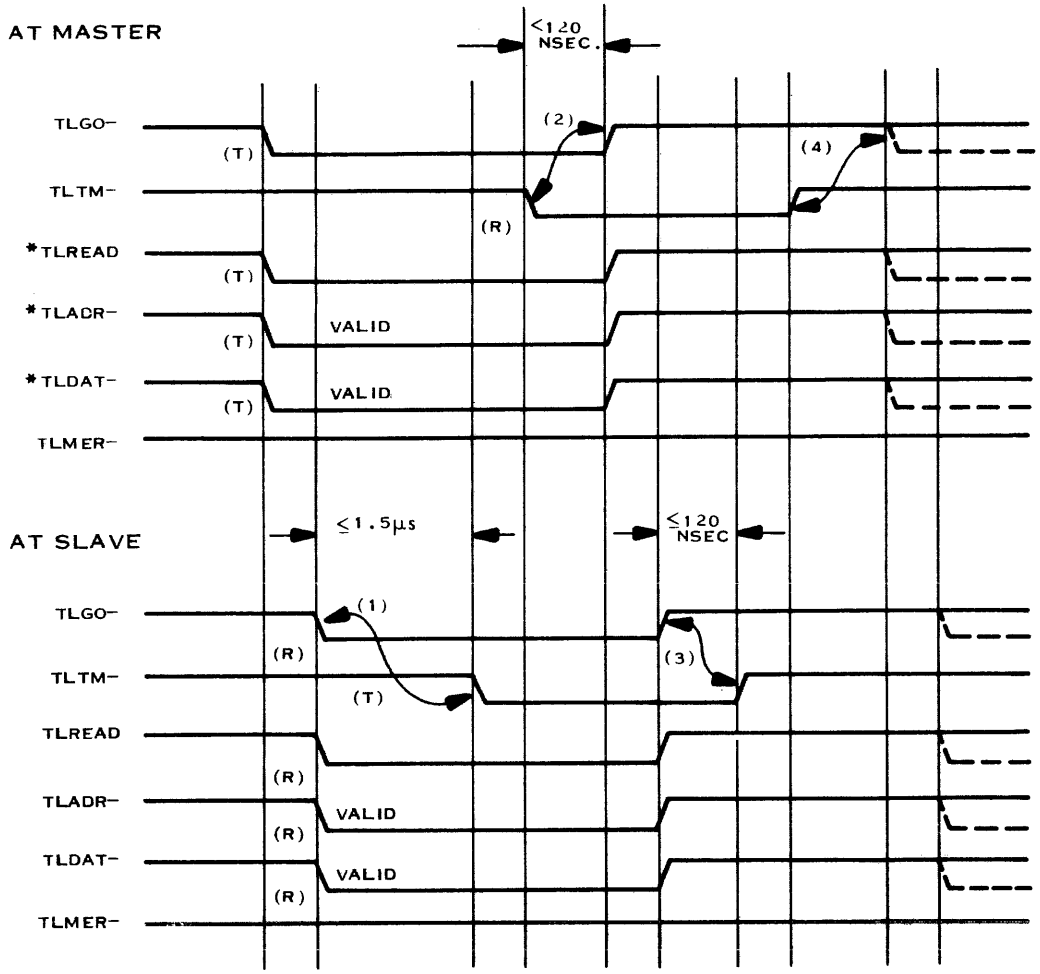
All slave devices on the TILINE receive TLGO- transmitted by the master. Each slave device must decode the address to determine if it is being addressed. The slave generates a delayed go signal (using a timer circuit) and uses that signal to strobe for a valid address decode. It is the responsibility of the slave device to delay go for a time sufficient to accommodate the worst case address decode time and the 20 nanosecond worst case TILINE skew.

When the slave device has delayed go and decoded the address as valid, it performs the write cycle and then asserts TLTM-. At the time the slave device asserts TLTM-, it must be finished with the TLDAT-, TLADR, and TLREAD signals from the TILINE. The action just described occurs during time one. This time is defined as the slave access time and should be less than 1.5 microseconds for all TILINE slaves except the TILINE coupler. When the TILINE master receives the asserted TLTM-, it must release TLGO-, TLREAD, TLADR-, and TLDAT- within 120 nanoseconds. This occurs during time two on the timing diagram.

At this time, the master device may relinquish the TILINE to another master device. When the slave receives the release of TLGO-, it must release TLTM- within 120 nanoseconds as shown in time three. When the master device receives the release of TLTM-, it may begin a new cycle if it has not relinquished the TILINE to another master device. This is shown as time four. Most TILINE masters, including the TFDC, perform only one read or write cycle per bus access.

2.5.5 TILINE Bus Timing-Read Cycle

Figure 2-9 is a timing diagram for a TILINE read cycle. It applies to any TILINE master and slave device but does not include the operations necessary for the master to gain access to the bus.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT.
(TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED
(R) = RECEIVED
*TLREAD, TLADR-, AND TLDAT- MUST BE STABLE AT THE TIME (OR BEFORE) TLGO- IS ASSERTED.

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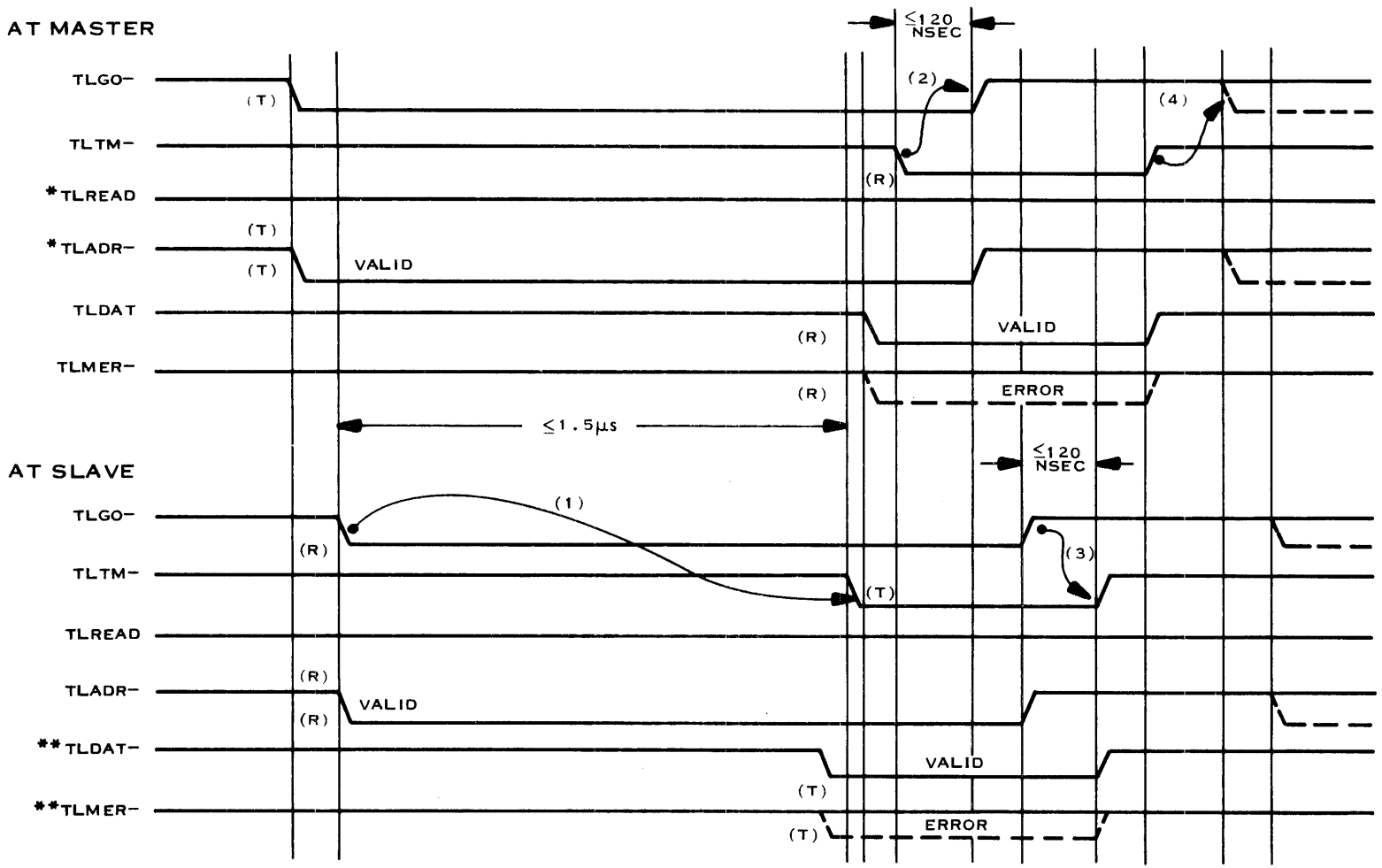
Figure 2-8. TILINE Master-to-Slave Write Cycle Timing Diagram

The master asserts TLGO- and at the same time generates a valid address (TLADR-) and TLREAD signal. All slave devices on the TILINE receive the TLGO- transmitted by the master. The slave devices delay the go signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsibility of the slave device to delay TLGO for a time sufficient to accommodate the worst case TILINE skew (defined as 20 nanoseconds maximum) and worst case address decode time. When this has been done and the address is decoded as valid, the slave device begins to generate read data. In the case of a memory module, this means starting a read cycle. When read data is valid, the slave device asserts TLTM- and at this time must have finished using TILINE signals TLADR- and TLREAD. If a read error is detected during a read cycle, the read error (TLMER-) signal is asserted by the slave. This signal must have the same timing as read data. This action occurs during time one.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT. (TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED (R) = RECEIVED
*TLREAD AND TLADR- MUST BE STABLE AT THE TIME (OR BEFORE) TLGO- IS ASSERTED
**TLDAT- AND TLMER- MUST BE STABLE AT THE TIME (OR BEFORE) TLTM- IS ASSERTED

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Figure 2-9. TILINE Master-to-Slave Read Cycle Timing Diagram

When the master receives the asserted TLTM-, it must release TLGO- and TLADR- within 120 nanoseconds as shown in time 2. At this time, the master may release the TILINE to another master device. When the slave receives the release of TLGO-, it must release TLTM- within 120 nanoseconds as shown in time 3. The data from the slave is no longer enabled onto the data bus after time 3. When the master device receives the release of TLTM- and if it has not released the TILINE (time 4), it may begin a new cycle as shown by the dotted lines.

2.5.6 Organization of TFDC TILINE Interface Logic

The TILINE interface logic is organized into three functional blocks:

- TILINE interface control
- TILINE master access logic
- TILINE slave logic

The TILINE interface control logic controls the sequence of operations necessary to perform the following:

- TILINE slave read cycle
- TILINE slave write cycle
- TILINE master read cycle
- TILINE master write cycle
- Microprocessor read from register file
- Microprocessor write to register file

The TILINE interface controller consists of a ROM-based state generator and output decoding logic. The state generator advances from state to state depending on the current state and control/status input signals. The decoded outputs are also determined by the current state and the input signals. This type of circuitry is ideally suited to the control of operations which follow well-defined sequences, such as the TILINE input/output operations. The TILINE interface controller relieves the 9900 microprocessor of these repetitive tasks, allowing the microprocessor to work in parallel with TILINE operations.

The TILINE interface controller accepts decoded control signals from the microprocessor address bus to specify the operation. The combination of the present state with inputs from the TILINE master access and slave logic determine interface controller outputs. These outputs control bus access, multiplexer steering, register input clocking, and provide sequence control to the TILINE master access and slave logic.

The TILINE interface controller is described in greater detail in paragraph 2.5.9.

The TILINE master access logic, together with the TILINE interface controller, performs the actions necessary to gain access to the TILINE, transfer the data word, and release control of the bus. This sequence of operations is called a TILINE master cycle.

The TILINE slave logic, together with the TILINE interface controller, performs the operations necessary to decode and recognize a TILINE address within the 8-word slave address space of the TFDC and to respond by accepting a data word (slave write) or by supplying a data word (slave read). Slave words are stored in the upper eight positions of the 16-word register file.

2.5.7 TILINE Master Operation of the TFDC

The TFDC acts as a TILINE master when transferring data from disk to 990 memory or from 990 memory to disk. The TILINE I/F control logic on the TFDC performs a single TILINE master cycle for each word transferred on the bus. The master cycle consists of the actions necessary to acquire access to the bus, transfer the data word, and release control of the bus.

A TILINE master read or write cycle is initiated by the TFDC microprogram as the result of a need to transfer a data word between the TFDC and 990 main memory. The word count and TILINE starting address are parameters which are supplied in the control words that initiated the TFDC operation. These parameters are stored in the register file.

If the controller were commanded to perform a Read Data operation with a word count of 50, it would have to read 50 words from the disk and achieve access to the TILINE 50 times. Prior to the first TILINE master cycle, the TFDC microprogram must load the 20-bit TILINE starting address into the TILINE address register/counter. This transfer is performed in two steps, due to the 16-bit limit of the microprocesssor data bus. The TILINE interface controller performs the housekeeping chore of updating the TILINE address after each transfer, and the TFDC microprogram counts down the word count. The process continues until the word count reaches zero, indicating that all words have been transferred.

TLAGIN (from a higher priority master) enters each master on P2, pin 6 and TLAGOUT leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers or jumper switches on the backpanel ensure line continuity across slots not occupied by TILINE masters.

The master access logic of any TILINE master is based on a standard four-state access sequence. These states include: Idle, Device Access Request, Device Acknowledge, and Device Access, as shown in the master access flowchart, Figure 2-11.

2.5.7.1 Master Device TILINE Acquisition. Access to the TILINE is competitive between the TILINE masters on the bus; there is no centralized bus control logic. Conflicts between competing masters are settled by a positional priority system and a bus reservation scheme. The master device in the highest numbered chassis slot has the highest priority. Priority ranking decreases with each chassis slot toward the 990 central processor, which has the lowest priority. The TLAG signal that runs through each TILINE master establishes the priority as shown in Figure 2-10.

If the TILINE master has no data to transfer, the master access logic remains in the Idle state, and TLAG is passed on to lower priority masters. The Idle state is the rest state of the master access logic when it is not attempting to gain access to the bus and transfer a word.

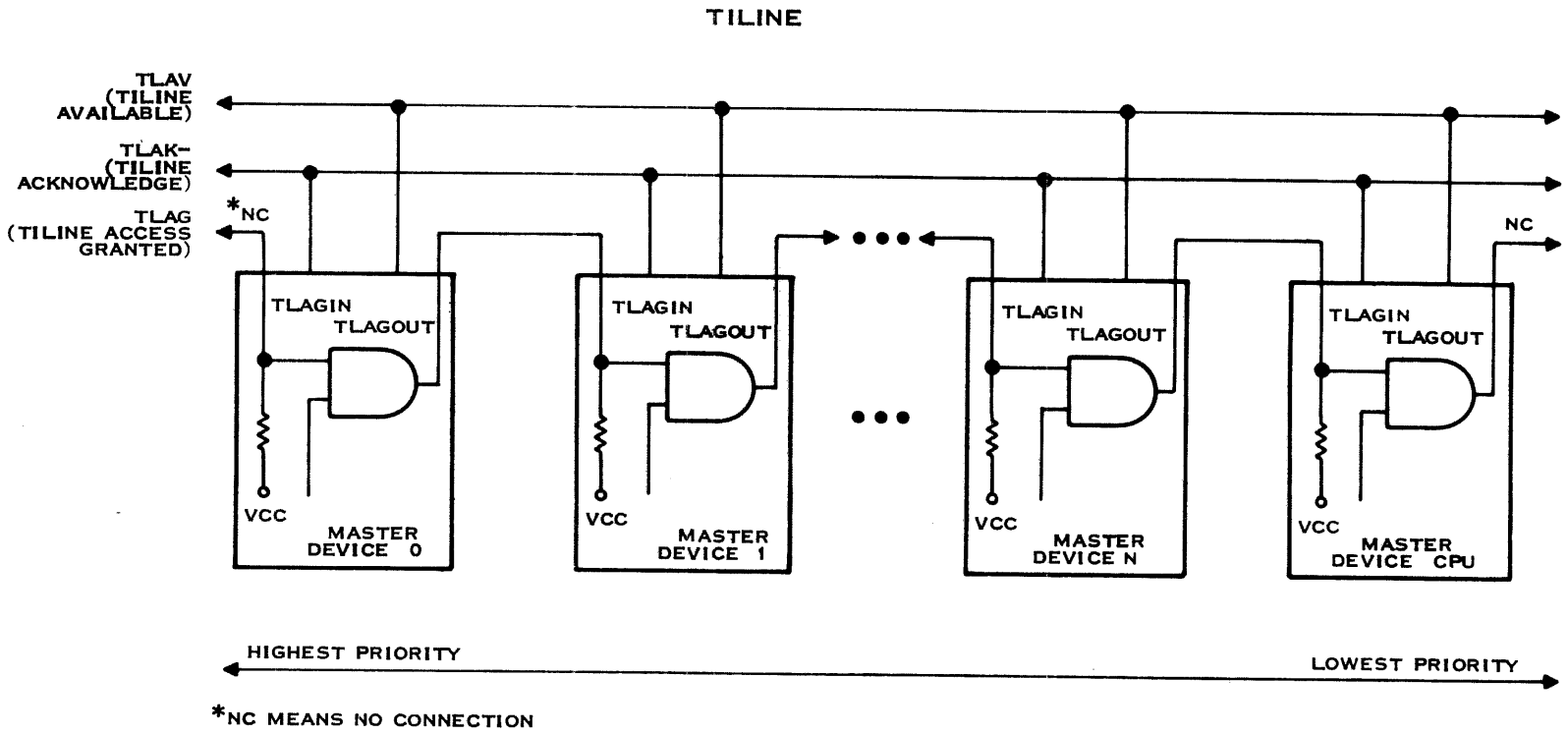

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Figure 2-10. TILINE Master Device Priority Interconnections

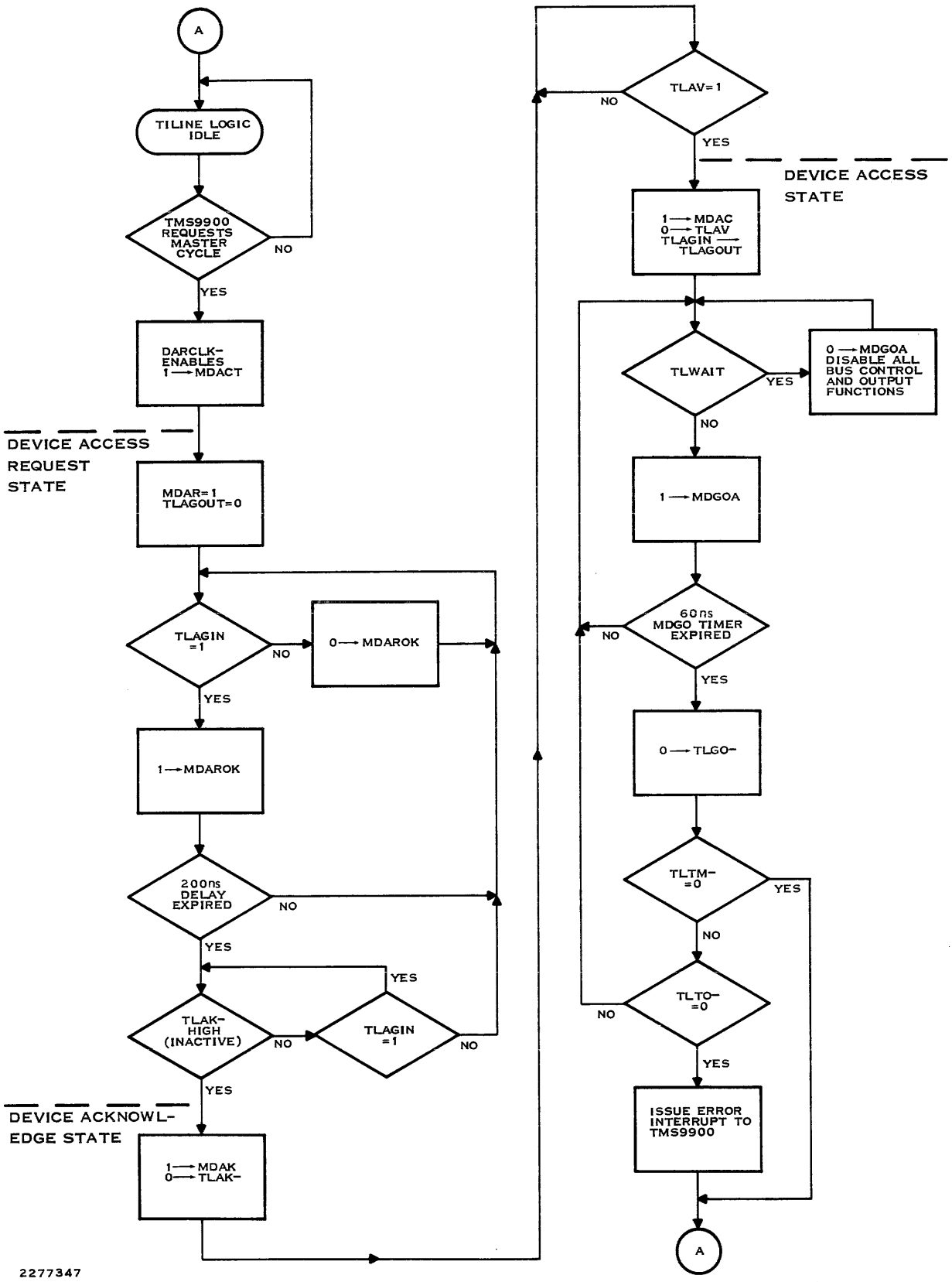


Figure 2-11. TILINE Master Access Flowchart

When the master requires access to the bus, it goes into the Device Access Request state and blocks TLAGOUT to the lower priority masters. While in the Device Access Request state, the controller monitors TLAGIN. If TLAGIN is high, the controller can monitor TLAK- after a 200-nanosecond delay. A high TLAK- signal indicates that no other controller is in the Device Acknowledge state. This signal allows the controller to go into the Device Acknowledge state. The Device Acknowledge state is a confirmed reservation for the next available bus access. The overlap of the current operation with reservations for the next operation reduces bus dead time and increases throughput.

In the Device Acknowledge state, the master access logic pulls TILINE acknowledge low to prevent any other controller from going into the Device Acknowledge state. It continues to disable TLAGOUT and monitors TILINE available. When TLAV goes high, the access logic advances to the Device Access state and initiates the read or write cycle. TLAGOUT is enabled so the next controller can prepare for access. At the end of the read or write cycle, the access logic clears the Device Access state, sending TILINE available to the other controllers. It then returns to the Idle state.

2.5.7.2 Detailed Operation of TILINE Master Access Logic. This discussion of how the TILINE access control logic functions is based on Figure 2-12 and logic drawing (2261692 or 2267297) sheet 13.

The device access request clock (DARCLK-) from the TILINE interface controller is the first event of a TILINE master cycle. DARCLK-, which is synchronized to the microprocessor clock (CLK3-), sets the master device active F/F. If the master access logic is not in the Device Access state and master device complete is inactive (MDAC-, MDCMP- high), the logic enters the Device Access Request state. MDAR is inverted and combined with TILINE access granted in (TLAGIN) to disable TLAGOUT to lower priority masters. MDAC- and MDAR, which are both high, are combined with TLAGIN at the input to another AND gate to monitor for TLAGIN to go high.

If a higher priority master is blocking the TILINE access granted signal, there will be a wait until TLAGIN goes high. When TLAGIN goes high, the master device access request OK signal (MDAROK) is set high. MDAROK is delayed 200 nanoseconds to produce active-low MDARDLY-. MDARDLY- is applied to the input of an OR gate with TLAK to monitor for TILINE acknowledge (TLAK) to go low. TLAK is the output of an inverting line receiver which monitors the TLAK- signal. When TLAK goes low, it indicates that no other controller is in the Device Acknowledge state and allows the TFDC controller to proceed into that state.

When TLAK goes low, MDAKSET- goes low to set the device acknowledge latch. This zero-setting latch was held clear until the master access logic reached the Device Access Request state. MDAK is sent to the TLAK- receiver/driver to pull TLAK- low and inform other controllers that the Device Acknowledge state is occupied. This corresponds to a reservation for the next available bus access cycle. MDAK- is applied to the input of a NAND gate with TLAV- to monitor for the TILINE to become available.

The controller monitors TLAV- until the TILINE becomes available. When the TILINE becomes available, TLAV- goes low, and when combined with MDAK-, sets MDACSET- low. MDACSET- low sets the device access F/F and advances the controller to the Device Access state. This is the state in which the controller achieves access to the bus.

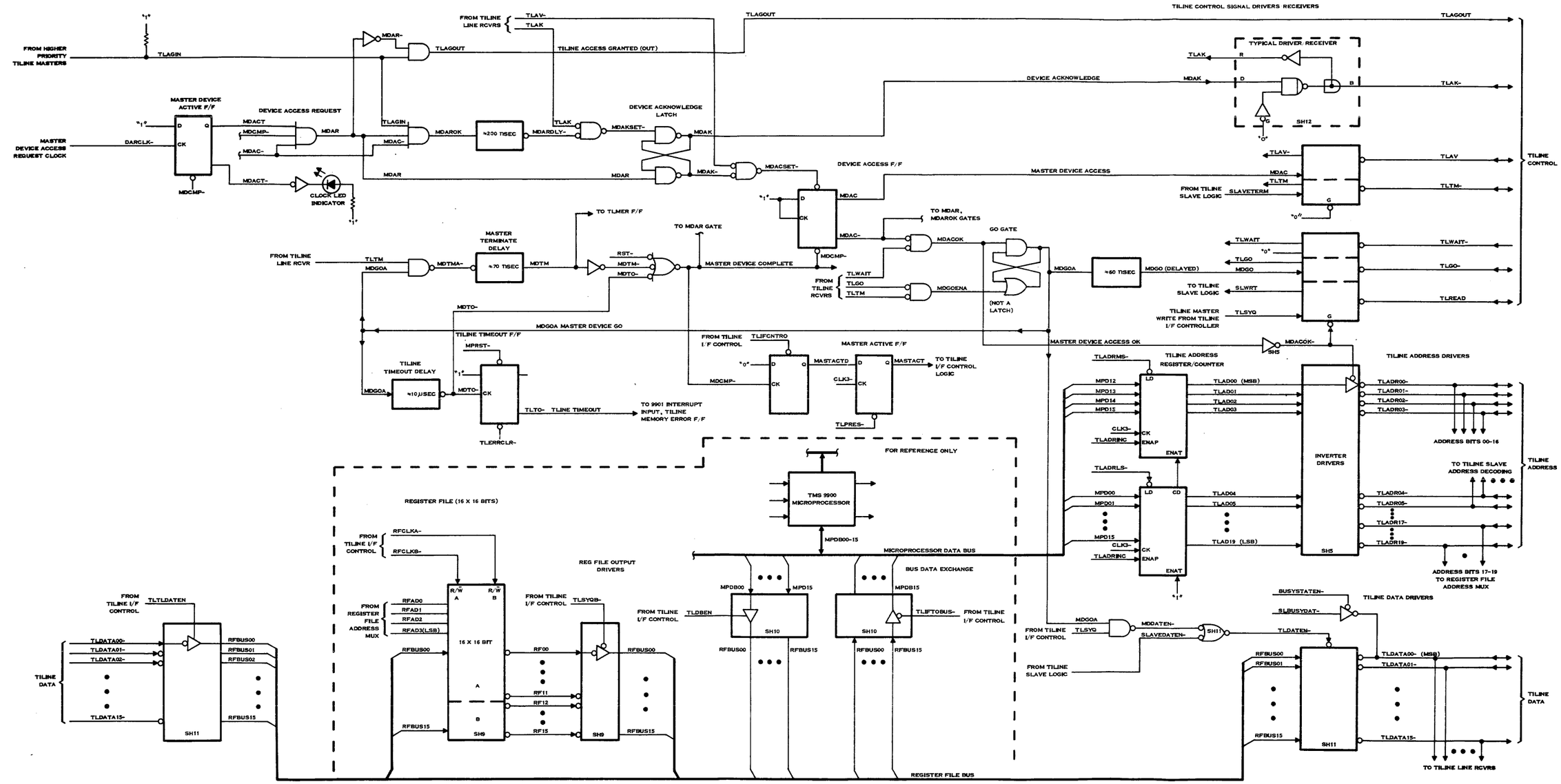


Figure 2-12. TILINE Master Access Logic

MDAC from the Q output of the device access F/F is applied to the TLAV driver, forcing TLAV low to indicate that the TILINE is not available (busy). MDAC- from the Q- output of the device access F/F is used to perform a number of tasks. It is used to disable MDAR, gating TLAGOUT to lower priority masters so they may prepare for access. MDAR low also clears the device acknowledge latch, so other masters may enter the Device Acknowledge state.

MDAC- also releases the MDAROK input to the device access time delay. MDAC- is combined in an OR gate with TLWAIT. TLWAIT allows operations to be suspended without a timeout error on request by a TILINE coupler. The TLWAIT- signal from the coupler is inverted in the line receiver, causing TLWAIT to go high and holding MDACOK high until the coupler has released TLWAIT-. In the more usual case, TLWAIT is inactive (high) and setting the master device access F/F results in an immediate master device access OK (MDACOK).

MDACOK is inverted and is used to strobe the line drivers for TLREAD and TLGO- and to enable the outputs of the TILINE address register/counter (TLAD00-19) onto the external TILINE address bus (TLADR00-19)-. Note that while the address and read/write control signal are supplied to the bus, TILINE go (TLGO) is still inactive, so no slaves are activated.

The MDGOA gate is a compound gate made up of an AND gate cross-coupled to an OR gate. Despite the resemblance, the MDGOA gate is not a latch. The inputs to the MDGOA gate are MDGOENA and MDACOK.

MDGOENA is set to logic 1 by the combination of TLTM and TLGO low. TLTM is high until the slave device involved in the previous operation releases TLTM- to indicate the termination of the operation. TLGO is at logic 1 until the master device involved in the previous operation releases TLGO-, allowing TLGO to go low. This is how the controller is forced to wait for the previous cycle to complete before setting MDGOENA high to enable a new cycle.

With MDGOENA high, MDACOK enables the output of the MDGOA gate, master device go. MDGOA is used for a number of purposes. After a delay of approximately 60 nanoseconds to allow the TILINE addresses and TILINE read/write signal to stabilize, MDGO enables the TILINE go (TLGO-) signal. This is a command for all slaves to decode the address and (for the selected slave) to perform the read or write operation. The slave must respond with a TILINE terminate signal within approximately 10 microseconds, or the master access logic will terminate the operation with a TILINE timeout error. Nominal response time is 1.5 microseconds.

For a write operation (TLSYQ high), TLSYQB- gates the register file output onto the register file bus (RFBUS00-15) and MDGOA is ANDed with TLSYQ to enable the register file bus to the TILINE. Register file address 0 is used for TILINE master write cycles.

MDGOA is combined with TLTM at the input to an AND gate to monitor for termination of the current operation. Assuming a normal operation, the slave pulls TLTM- low to indicate that the operation is complete. TLTM then goes high. After a 60- to 70-nanosecond delay, TLTM, in combination with MDGOA, sets the master device terminate (MDTM) signal high. Master device terminate is inverted and ANDed with controller general reset (RST-) and master device timeout (MDTO-). For normal termination, MDTM- enables the active low master device complete (MDCMP-) output.

Master device complete (MDCMP-) completes the TILINE master cycle and clears the TILINE master access logic in preparation for the next master cycle. MDCMP- is responsible for the following operations:

1. It holds the device access request gate disabled (MDAR low) during termination of a master cycle while MDAC is reset for the next master cycle.

2. It clears the master device active F/F, preparing it for the next device access request. The CLK LED indicator lights. MDACT low holds the device access request gate in the disabled state after MDCMP- returns high.

3. It clears the device access F/F, causing MDAC to go low and allow TLAV to indicate that the TILINE is now available. TLMER is also clocked at this time, as described in the next paragraph. Clearing the device access F/F also sets MDAC- high, which disables MDACOK-, causing it to clear the MDGOA gate and release TLGO- and TLREAD. Disabling MDACOK- removes the enable from the TILINE address drivers and clearing the MDGOA gate disables the TILINE data drivers (master write only). Clearing the MDGOA gate also prevents expiration of the TILINE timeout delay.

4. The slave responds to the loss of TILINE go (TLGO) by releasing TILINE terminate (TLTM- returns high). The inverted output (TLTM) of the line receiver forces MDTMA- high and, after the master terminate delay, forces master device terminate (MDTM) low.

5. As MDCMP- returns to logic 1, the positive edge of the pulse clears the MASTACTD F/F and on the next CLK3-, the master active (MASTACT) F/F clears. MASTACT is a sequence control input to the TILINE interface controller.

Assume now that the slave device does not issue a TILINE terminate before the TILINE timeout timer expires. Master device timeout (MDTO-) goes low 10 microseconds after master device go (MDGOA). MDTO- issues a master device complete (MDCMP-), which clears the master logic just like a normal termination. However, MDTO- also sets the TILINE timeout F/F. The Q- output of the F/F is an interrupt input to the 9901 PIA, informing the 9900 microprogram of the error. The 9900 must clear the error via the CRU bus (TLERRCLR-) before attempting another master cycle. The most common cause of TILINE timeout errors is attempting to read or write to a nonexistent TILINE address.

If the operation is a TILINE master read operation, the slave memory may detect a nonrecoverable error in the data. In this case, the slave generates a TILINE memory error (TLMER-) signal before issuing TILINE terminate. The TLMER output of the line receiver sets the TILINE memory error F/F when the TLTM signal goes high. The TLMER F/F is clocked at the same time as MDCMP- clears MDAC. The Q- output of the F/F serves as an interrupt input to the 9901 PIA, informing the 9900 microprogram of the error. As in the case of a timeout error, the 9900 must clear the error (TLERRCLR) via the CRU bus.

2.5.8 TILINE Slave Logic

The TFDC acts as a TILINE slave when the 990 computer loads a control word (W0-W7) into the register file or reads register file contents. Slave read and write operations are processed by interrupt routines in the 990 microprogram. The microprogram must be cycling in the idle loop to process a slave read or write to the register file. W7, bit 0 is the only bit that may be read when the controller is busy, as described in paragraph 2.5.8.2.

2.5.8.1 TILINE Slave Read with Idle Controller. The TILINE slave logic is shown in Figure 2-13 and on sheet 12 of the logic diagrams. For this description, assume that the controller is idle and the 990 computer requests the contents of control/status word W0. The 990 computer, acting as a TILINE master, requests the word by sending a 20-bit TILINE address, a TILINE read signal, and, after a short delay for address stabilization, the TILINE go strobe.

The TILINE slave address comparator checks 17 bits of the incoming address (TLADR00- through TLADR16-) against the TILINE base address of the TFDC. This address, which is partially hard-wired and partially switch-selected, determines if the TILINE slave operation is directed to the TFDC. TLADR17- through TLADR19- are not involved in the base address comparison, as shown in Figure 2-14. Figure 2-15 shows the switch settings for selecting the TILINE base address. The address comparator monitors the TILINE address lines at all times, but no actions are initiated until the TILINE master sends the TILINE go (TLGO- low) signal. Figure 2-16 shows the timing of events in this cycle, from TLGO- to termination.

The inverted output of the TILINE go line receiver clocks the slave idle F/F, removes the constant clear from the slave active F/F, and removes the constant preset from the slave write F/F. If the TFDC is idle (IDLE output of the idle status register set), TLGO sets the slave idle F/F. TLGO is delayed approximately 100 nanoseconds to assure that the address lines and the slave address comparator output have stabilized. The delayed output is called slave go delay (SLGODLY).

If the address comparison is good (SLADROK high) at the end of the delay, the slave active F/F sets. The slave go delay also clocks the slave write F/F to follow the slave write (SLWRT) signal from the TLREAD line receiver. Note the sense of the outputs of the slave write F/F. The Q output is SLRD-, and the Q- output is SLRD (slave read). The SLRD output of the slave write F/F goes to the TILINE interface control logic, where it is synchronized to microprocessor clock (CLK3-) and sent to one input of the state generator input multiplexer as SLRDQ. SLRD is active for a slave read cycle.

The SLAVEACT and SLVIDLE signals from the slave active and slave idle flip-flops are ANDed to supply SLAVESTART to the slave cycle F/F. SLAVESTART sets the slave cycle F/F on the next CLK3- pulse. The SLAVE output is sent to two different inputs of the state generator input multiplexer in the TILINE I/F control logic. SLAVE initiates the state generator operations associated with a TILINE slave operation (state 18), and SLRDQ selects read or write operations (state 19 or 1A, respectively) on the next CLK3- cycle.

The SLAVE and SLRD signals are ANDed within the slave logic to produce slave read data (SLRDDAT), which is combined with SLAVEACT to produce the active-low slave data enable (SLAVEDATEN-) signal. SLAVEDATEN- low (or MDDATEN- low) forces TILINE data enable (TLDATEN-) low to gate the register file bus output to the TILINE data line drivers. The data is not stable at this point in time, but it does not have to be stable until just before the slave terminate is issued.

The TILINE I/F controller is responsible for the multiplexer steering, register file operation control, and bus gating necessary to read the selected control word (W0 for this example) from the register file and place it on the register file bus. Register file bus gating to the TILINE drivers is controlled by TLDATEN- from the slave logic.

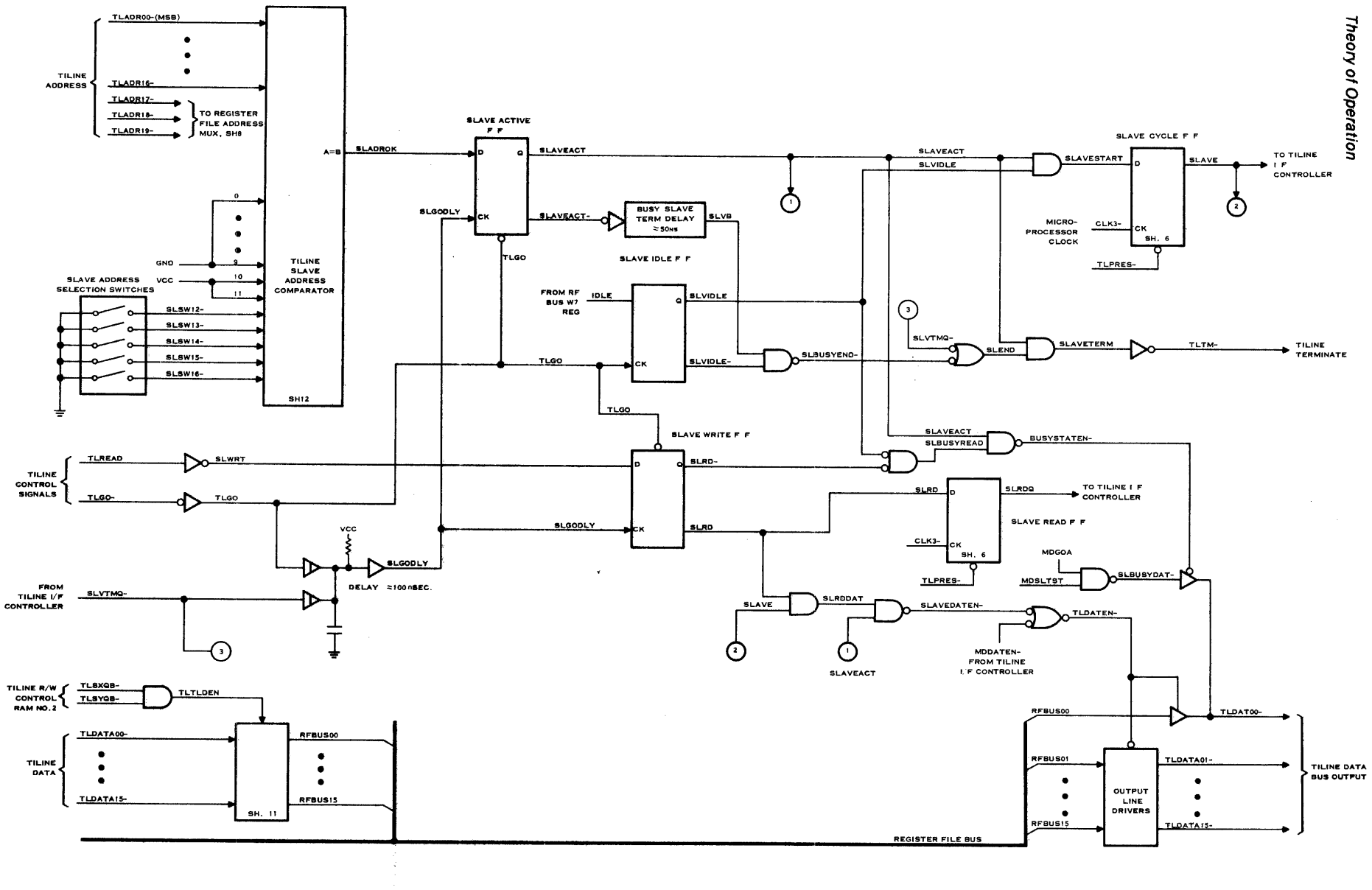


Figure 2-13. TILINE Slave Logic

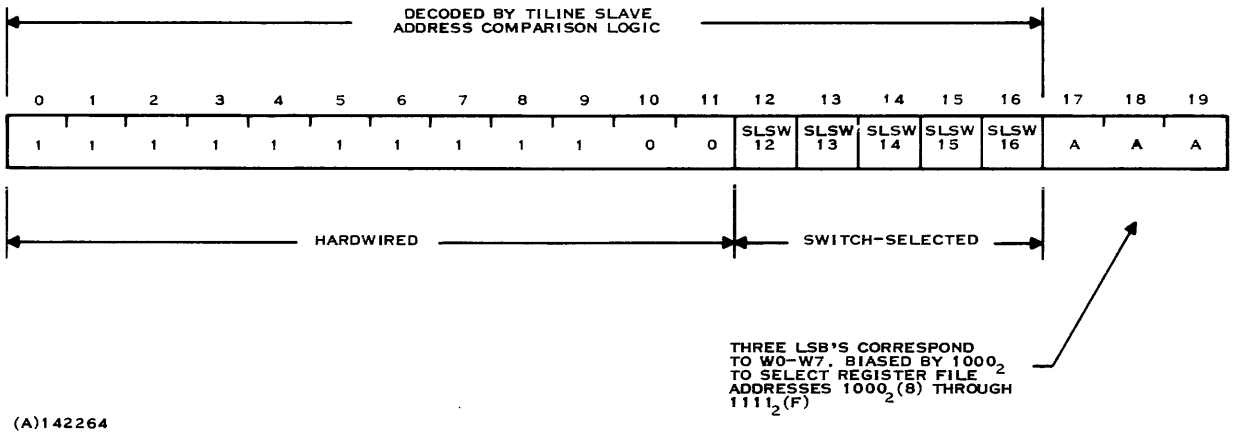


Figure 2-14. TILINE Slave Address Comparison

The RFMASTAD (register file master address) and RFTLAD (register file TILINE address) signals from the TILINE interface control logic control the register file address multiplexer. RFMASTAD low enables the multiplexer to select an address other than 0000. RFTLAD high steers the multiplexer to select the active-high form (SLADR17 through SLADR19) of the least significant TILINE address bits. A hardwired 1 in the MSB position biases the actual register file address by eight. The next microprocessor clock pulse stores the multiplexer outputs in the register file address register. The four register file address bits (RFAD0-RFAD3) are routed to the register file, and RFAD1-RFAD3 are routed to the decoder ROM in the TILINE I/F control logic.

The TILINE interface control logic enables the register file outputs onto the register file bus with TLSYQB- one clock time after selecting the register file address.

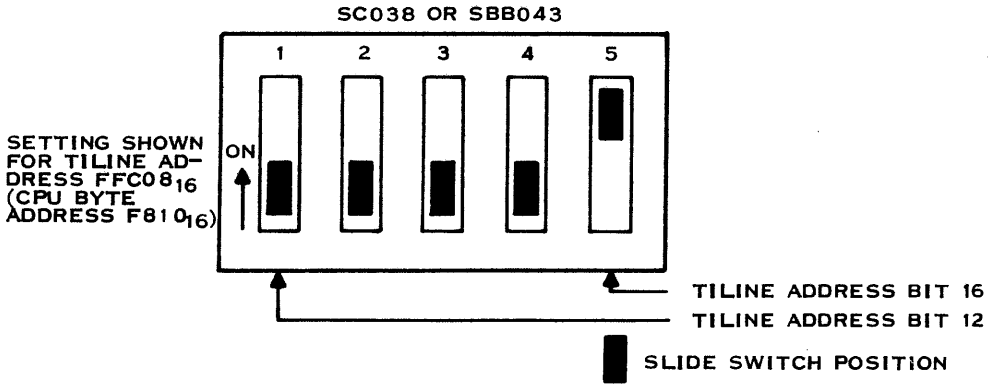
The interface control logic maintains the contents of the slave word on the TILINE drivers and issues a slave terminate command (SLVTMQ-) in state 19. SLVTMQ-, when low, enables slave end (SLEND), which is ANDed with SLAVEACT to produce slave terminate (SLAVETERM) to the TILINE terminate line driver. Note that a TILINE terminate, when issued by a slave being read, indicates that the data is available and stable on the TILINE data lines.

The SLVTMQ- signal also holds the slave go delay (SLGODLY) stable to delay the next slave cycle until the current slave cycle is completed.

The 990 computer, after accepting the data word, releases TILINE go, which clears the slave active F/F and the (previously clear) slave write F/F. Clearing the slave active F/F disables the TILINE data drivers via high SLAVEDATEN- and TLDATEN- signals. This action also clears the slave cycle F/F on the next CLK3- pulse.

With the SLAVE signal now low, the TILINE I/F state generator returns to state 00 and removes the TILINE terminate command. This completes the slave read cycle.

2.5.8.2 TILINE Slave Read with Busy Controller. Before issuing a set of command words to the TFDC, the 990 computer must check TFDC idle/busy status by reading and testing W7, bit 0. If W7, bit 0 is a one, the controller is idle, and is ready to accept control words. If W7, bit 0 is a zero, the controller is busy and cannot accept TILINE slave words.



HEXADECIMAL ADDRESS		TILINE ADDRESS SWITCHES				
TILINE	CPU BYTE	1	2	3	4	5
FFC00	F800	OFF	OFF	OFF	OFF	OFF
FFC08	F810	OFF	OFF	OFF	OFF	ON
FFC10	F820	OFF	OFF	OFF	ON	OFF
FFC18	F830	OFF	OFF	OFF	ON	ON
FFC20	F840	OFF	OFF	ON	OFF	OFF
INCREMENTS OF 08_{16}	INCREMENTS OF 10_{16}	STRAIGHT BINARY SEQUENCE				
FFCF0	F9E0	ON	ON	ON	ON	OFF
FFCF8	F9F0	ON	ON	ON	ON	ON

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Figure 2-15. TILINE Base Address Switch Settings

The slave idle F/F and associated logic allow the disk controller to respond with a simulated W7 word if the controller is busy. This simulated W7 word has a zero at bit 0 to identify busy status, and bits 1-15 are meaningless. No register file operations are performed, and the on-going controller operation is not disrupted.

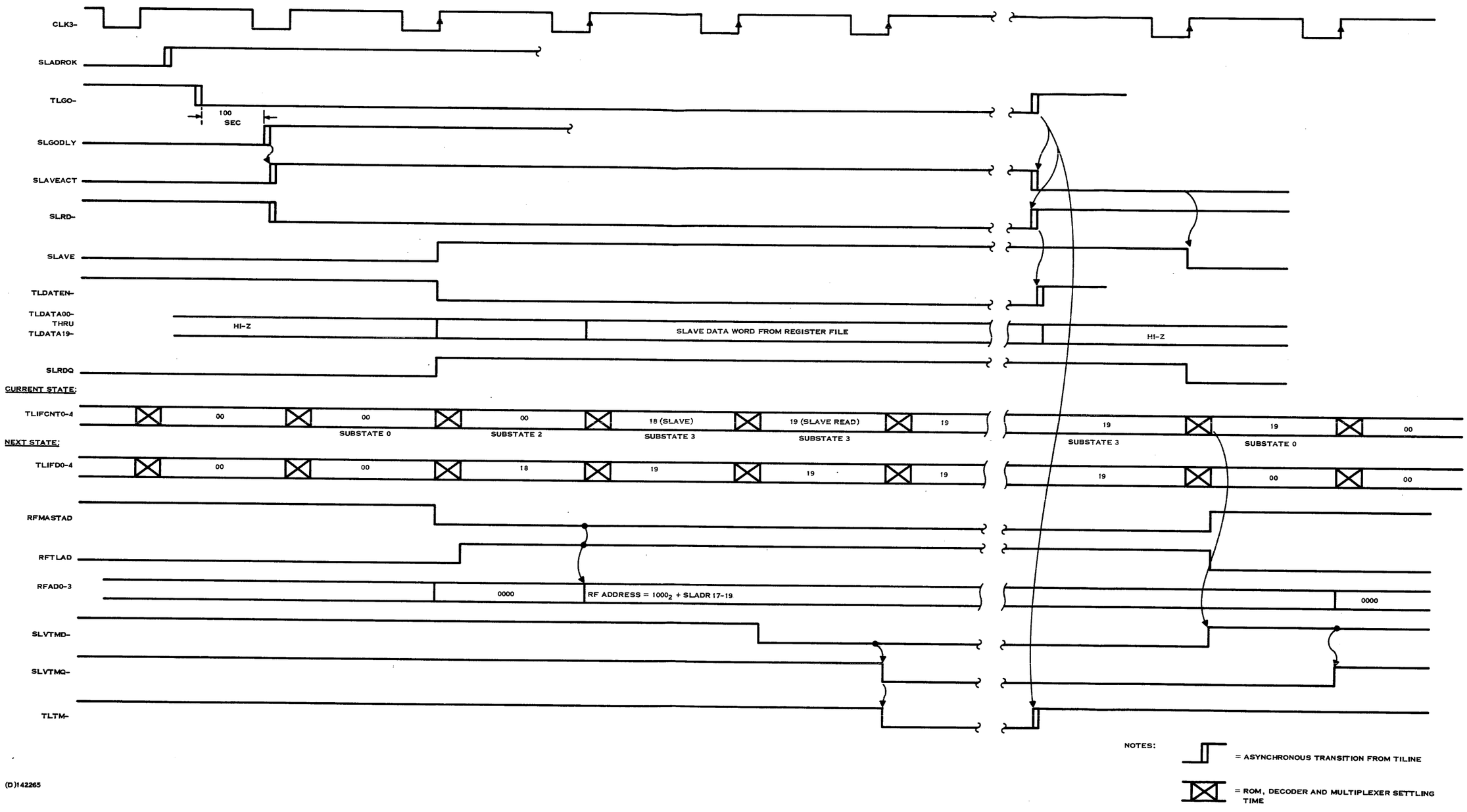

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Figure 2-16. Slave Read Timing for Slave Logic and Interface Control

NOTE

No matter which slave word is requested, a busy controller always responds with a simulated W7 word in which bits 1-15 are don't cares. It is, therefore, the programmer's responsibility to read W7 and to test bit 0 before attemping to read W0-W6 or to interpret W7, bits 1-15. It is also the programmer's responsibility to read and check W7, bit 0 before attemping to write control words to the TFDC. The device service routines (DSRs) supplied with DX10, DX5, and other TFDC-compatible operating systems incorporate these requirements in a manner transparent to the user program.

Assume that the 990 computer attempts to read W7 while the controller is busy. The idle F/F in the idle status register and the slave idle F/F are both reset (SLVIDLE = IDLE = 0). The 990 computer places the 20-bit TILINE slave address and the TILINE read signal on the lines, followed by TILINE go. The upper 17 bits of the TILINE address are decoded to produce SLADROK. The three least significant bits are routed to the input of the register file input multiplexer. These three bits are not decoded if the TFDC is busy.

After the slave go delay expires, the slave active F/F sets and the slave write F/F remains reset. SLAVEACT- (reset output of the slave active F/F) initiates the slave active delay. When that delay expires, SLBUSYEND- low and SLAVEACT high enable a TILINE terminate (TLTM-) output to the 990 computer. TLTM- signals completion of the slave cycle, and indicates that the 990 computer should accept the data word on the TILINE data lines. Development of that data word is described in the following paragraphs

The SLVIDLE signal holds SLAVESTART low, so the SLAVE F/F remains reset. With SLAVE low, the normal (controller idle) slave cycle is not initiated. SLAVE low holds SLRDDAT low, thus holding the TILINE data enable (TLDATEN-) inactive (high). The SN74LS242 TILINE data drivers remain in the high-impedance state.

The low SLVIDLE signal and the low SLRD- signal combine to produce slave busy read (SLBUSYREAD). The slave busy read and slave active signals combine to develop the active-low busy status enable (BUSYSTATEN-) signal. BUSYSTATEN- enables a slave busy data line driver, which feeds the TLDAT00- data output line. The input to this noninverting driver, SLBUSYDAT- is held high, as MDSLTST is low except during self-tests of the master and slave logic. The high output on TLDAT00- corresponds to a zero idle/busy data bit in W7.

2.5.8.3 TILINE Slave Write. The TFDC control words are loaded into the register file by slave write operations, one slave write cycle for each word transfer. Operation of the TILINE slave logic is similar to slave read operations except for the state of the slave write F/F and the direction of TILINE data flow. The TILINE interface controller goes through a different set of states for the slave write operation.

Assume that the TFDC is idle and that the 990 computer sends a control word W1 over the TILINE. The slave address comparator checks the 17 most significant TILINE address bits against the board address. The TILINE go (TLGO-) signal from the 990 computer removes the constant clear from the slave active F/F and the constant preset from the slave write F/F. The 100-nanosecond slave go delay assures that the address comparator output is stable before clocking the slave active, slave idle, and slave write flip-flops.

Assuming that the address compares and that the TFDC is currently idle (IDLE from idle status register high), the slave active, slave write, and slave idle flip-flops set when SLGODLY goes high. Note that the Q output of the slave write F/F is SLRD-, and the Q- output is SLRD. SLRD low holds the TILINE data drivers disabled. SLRD also goes to the TILINE interface control logic where it is synchronized to the microprocessor clock (as SLRDQ) to serve as one input to the state generator input multiplexer.

SLAVEACT and SLVIDLE are ANDed to provide SLAVESTART to the input of the slave cycle F/F. The output, SLAVE, is synchronized to microprocessor clock and serves as a second input to the state generator input multiplexer. SLAVE initiates the state generator operations associated with slave cycles (state 18) and, on the next CLK3- pulse, SLRDQ selects slave write operations (state 1A).

The TILINE I/F control logic is responsible for the multiplexer steering, register file operation control, and bus gating necessary to accept the TILINE data word and store it in the register file. The I/F control logic also initiates the slave terminate after the word is stored.

The RFMASTAD (register file master address) and RFTLAD (register file TILINE address) outputs from the TILINE I/F control logic select and steer the register file address multiplexer. RFMASTAD low enables the multiplexer outputs and RFTLAD steers the multiplexer to select the active high form (SLADR17 through SLADR19) of the TILINE LSB address bits. A hardwired 1 at the multiplexer input biases the actual register file address by eight. The next CLK3- pulse stores the multiplexer outputs in the register file address register. The four register file address bits (RFAD0-RFAD3) are routed to the register file, and RFAD1-RFAD3 are routed to the decoder ROM in the TILINE I/F control logic.

Outputs TLSXD and TLSYD from the TILINE I/F decoding ROM are both low in state 1A. These outputs are latched and synchronized to CLK3- and then inverted as TLSXQB- and TLSYQB-. These two high signals are ANDed to produce TLTLDATEN, which gate the TILINE line receiver outputs onto the register file bus.

The active-low register file write signals (RFWRTA- and RFWRTB-) are latched at the end of state 1A. They serve as strobes to the register file clock multiplexers to gate CLK3- to the register files as RFCLKA- and RFCLKB-. RFCLKA- and RFCLKB- are write control signals that write the control word into the selected register file location. This is address 1001 for control word W1. RFCLKA- is disabled whenever a slave write to control word W0 is performed. Suppressing RFCLKA- prevents the 990 CPU from writing over disk status bits 0-11 of W0.

The I/F controller advances to the next state (1B) and issues a slave terminate (SLVTMQ-) signal at the end of the state. SLVTMQ- holds the slave go delay stable to prevent premature reclocking of the slave active and slave write flip-flops on the next slave cycle. SLVTMQ- is inverted to produce slave end (SLEND), which is ANDed with SLAVEACT to enable SLAVETERM. SLAVETERM sends TILINE terminate to the 990 computer.

The TILINE terminate for a write operation is a signal to the master that the slave (TFDC) has accepted the data word. The 990 computer releases the TILINE go and, after a short delay, releases the data and address lines.

When the active-low TLGO- returns high, TLGO goes low, clearing the slave active F/F. SLAVEACT low removes the TILINE terminate from the TILINE. On the next CLK3- pulse, the slave cycle F/F output, SLAVE, goes low to inform the TILINE I/F control logic that the slave cycle is complete. The I/F controller returns to state 00, the rest state.

2.5.9 TILINE Interface Control Logic

The TILINE interface controller controls bus gating, register file read/write operations, TILINE master and slave cycles, and data entry into the attention mask and idle status registers.

2.5.9.1 Introduction to ROM-based State Controllers. A state controller accepts input signals and produces decoded outputs based on both the current inputs and an internal state. The internal state is determined by the allowable state changes built into the controller and the past history of the input signals. State controllers may be built up from flip-flops and logic gates. The condition (set or reset) of all the flip-flops is the state of the controller. The flip-flops record the present state. The combinational logic gates produce output signals that are determined by the flip-flop outputs in combination with the input signals. Combinational logic also determines which flip-flops will set on the next clock pulse, based on the input signals and which flip-flops are currently set (current state).

For a sequence with many inputs, outputs, and internal states, a state controller based on flip-flops and gates becomes very complex. However, a state controller based on two read-only memories and a register can control very complicated sequences with very simple hardware. Refer to part A of Figure 2-17, which is a block diagram of the simplest form of a ROM-based state controller. The current state, which is latched in the register, and the input signals determine the ROM address. Burned into the ROM at that address is a word which contains the next state and encoded control bits.

The next clock pulse loads the word into the register, and the address inputs to the ROM change. The input variables are also synchronized to the clock so that the entire ROM address is stable. After the access time of the ROM, the next word is available at the ROM outputs.

A ROM decoder uses the current state and the encoded control bits to generate the control outputs. The ROM decoder performs in one device decoding functions which would otherwise require a large array of interconnected logic gates.

Part B of the figure shows two additions to the basic ROM state controller. A clocked register is added so that the control outputs are synchronized to the system clock. Adding a synchronization register delays the control signal outputs by one clock period minus the ROM access time, but assures stability of the outputs. Variations in ROM access time will not cause any problem, as long as the access time is shorter than the clock period.

Part B shows the spare address inputs of the ROM decoder used to decode additional input signals. These inputs do not affect the state controller sequence of states. The additional inputs provide more versatility in the output decoding, but do not waste state ROM address inputs with signals that have no effect on the state sequence.

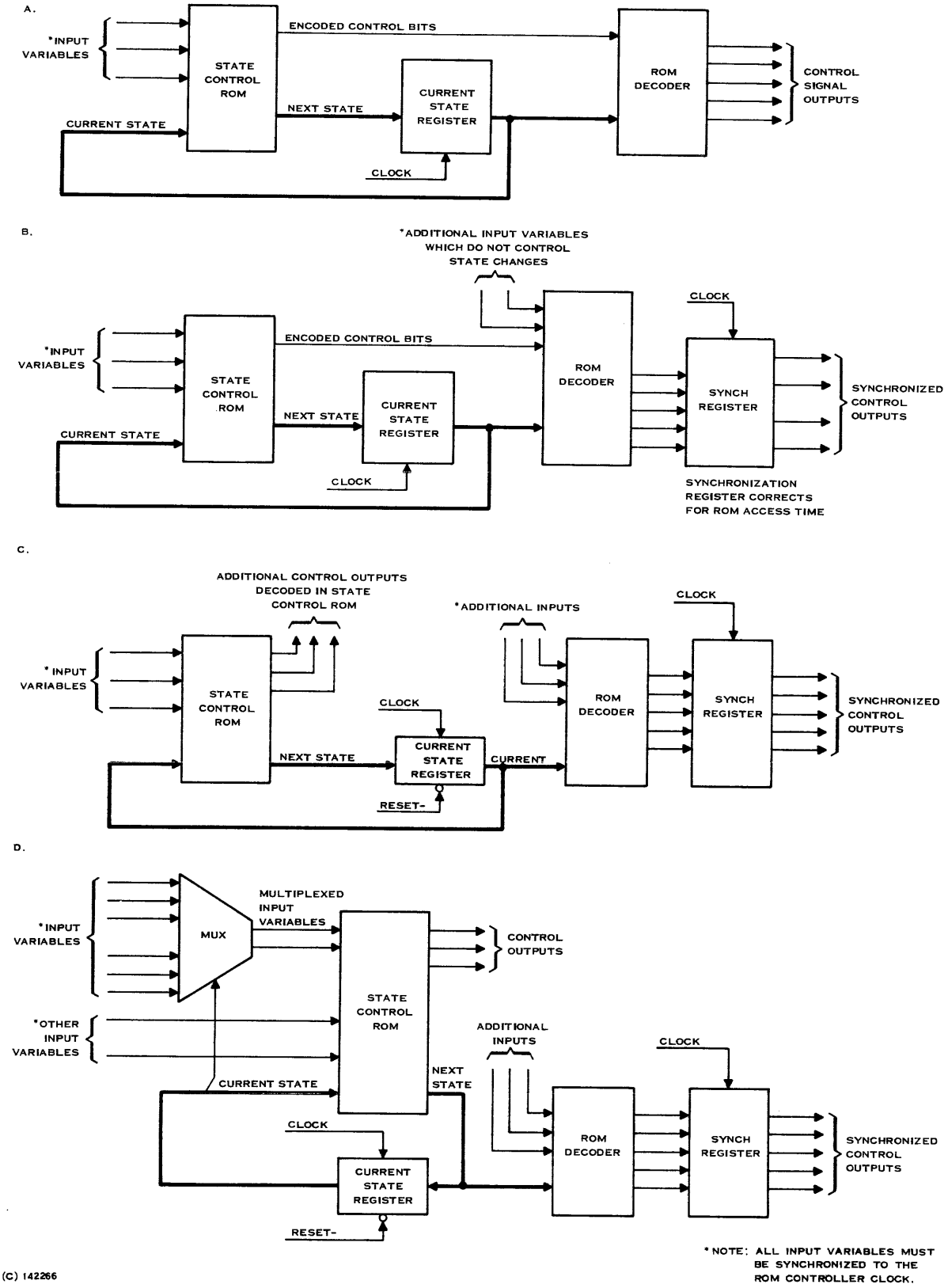

Figure 2-17. ROM-Based State Controllers

Part C shows control outputs directly from the state control ROM. For this circuit, some of the decoding functions have been moved from the ROM decoder to the state control ROM. This type of scheme makes less efficient use of the available bit positions in the state control ROM, but it allows use of a smaller decode ROM. The control outputs must be synchronized with the system clock, either in the synchronization register or at the point of use. The control outputs from the state control ROM (after synchronization) are available a full clock period before the control outputs from the ROM decoder.

There must be a way to force the state controller to an initial state when power is first applied or when a logic reset occurs. Part C shows a reset input to the current state register that forces the controller to the 0000 state. The controller sequences end with a return to this rest state. The state controller program may also include error returns to the rest state for illegal combinations of input signals and current state.

Part D shows the type of state controller connection used in the TILINE I/F control logic. This connection uses a multiplexer at the input to the state control ROM. The multiplexer allows more controller input variables without requiring more ROM address input pins. The current state register supplies the multiplexer steering signals. The current state determines which of the input variables are selected. The input variables that are "don't cares" for this state are not gated through the multiplexer. Note also that it is the next state outputs (rather than current state) that are sent to the ROM decoder inputs. This eliminates one stage of delay. No timing problems are introduced because all inputs and outputs are synchronized to clock timing.

2.5.9.2 TILINE I/F Controller Logic. Figure 2-18 is a block diagram of the TILINE I/F controller logic. The input and output signals are described in Table 2-2. Gate designators in parentheses refer to the 2267295 fineline TFDC board.

All of the input variables are stored in flip-flops clocked by MPU clock, CLK3-, so they are stable and synchronized to CLK3-. Figure 2-19 is a simplified timing diagram that shows relative timing between groups of signals. Use the block diagram to follow this description and the timing diagram to clarify the timing relationships. Detailed logic of the TILINE I/F controller is shown in Figure 2-20 and on sheets 6 and 7 of the logic drawing.

The inputs to the state control ROM are the current state (TLIFCNTR0-4), and input variables MPTLIF, TLIFVAR0, and TLIFVAR1. TLIFVAR0 and TLIFVAR1 (TILINE interface variables 0 and 1) are multiplexed input variables, with selection controlled by the two most significant bits of the current state. The current state selects a block of eight word addresses in the ROM, and the three input variables select a specific word from the group of eight words.

After the ROM access time delay (approximately 50 nanoseconds), the selected word appears at the ROM output. Five bits of the output word (TLIFD0-4) represent the next state of the controller. The other three output bits are control signals to the register file and the TILINE slave logic. Note that the only immediate action due to any of these outputs is a change in address at the input to the TILINE and register file read/write control ROM. The outputs of this second ROM stabilize after an additional access time delay. The sum of these two ROM delays (approximately 100 nanoseconds) is less than one microprocessor clock period (333.3 nanoseconds).

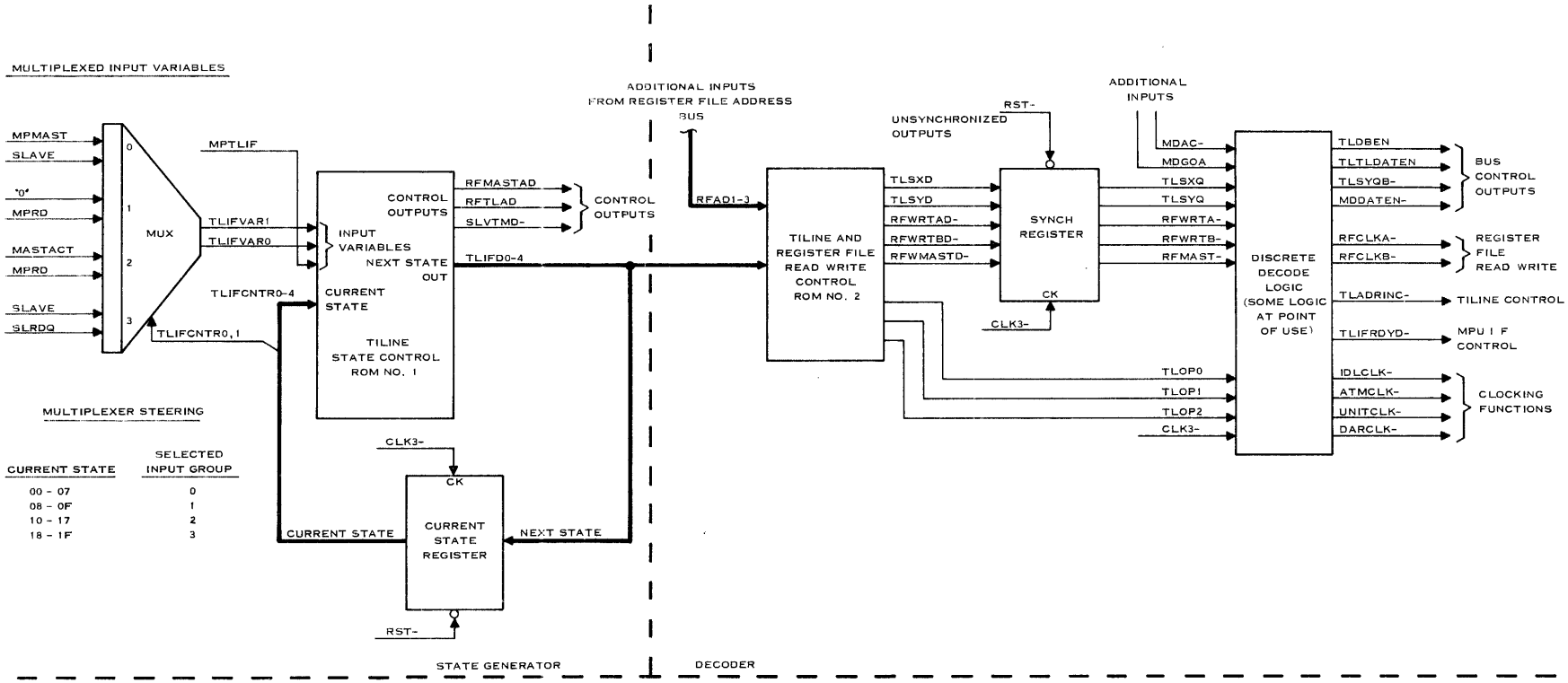

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Figure 2-18. Simplified Diagram of TILINE I/F Controller

Table 2-2. TILINE I/F Controller Input/Output Signals

Signature	Sheet	Gate*	Description
Inputs:			
MASTACT	6	UD114-12 (UBB129)	Master active. Set when I/F Controller goes to idle (state 0). Cleared at completion of TILINE master access cycle by MDCMP- to allow termination of the cycle and set up for next master cycle.
MDAC-	13	UD102-6 (UBH116)	Master device access. Unsynchronized signal which is low when the TILINE master logic is in the device access state. Used for register file write control during TILINE master read operation.
MDGOA	13	UE026-3 (UCD029)	Master device go. Unsynchronized output of go gate in TILINE master access logic. Used during TILINE master write to gate RF bus data to TILINE line drivers.
MPMAST	3	UD114-6 (UBB129)	Microprocessor master cycle. 9900 micro-program command to initiate a TILINE master cycle. Decoded from 9900 address bus.
MPRD	3	UD114-9 (UBB129)	Microprocessor read. 9900 microprogram command to read register file data to MPU or to read TILINE data (TILINE master read).
RFADD1, RFADD2, RFADD3,	8 - -	UB026-6 UB026-15 UB026-2 (UAG029)	Register file address bits 1-3. Controlled by TILINE address bits 17-19 during slave operations, otherwise, by microprocessor address bus.
SLAVE	6	UD114-19 (UBB129)	Slave. Synchronized version of SLAVEACT, which enables slave read and slave write operations. SLAVE informs I/F controller that a normal slave operation is in progress.
SLRDQ	6	UD114-16 (UBB129)	Slave read. Identifies type of slave operation (read or write) to I/F controller.
Outputs (latched on trailing edge of CLK3-, unless specified otherwise):			
ATMCLK-	7	UE078-5 (UCD089)	Attention mask clock. Loads attention mask (W0, bits 12-15) from RF bus into attention mask register in the TILINE inperrupt logic. ATMCLK- occurs in coincidence with a CLK- pulse when addressing W0.
DARCLK-	7	UE078-7 (UCD089)	Device access request clock. Command output which clocks the master device active F/F to initiate a TILINE master cycle. DARCLK- coincides with a low CLK3- pulse.

Table 2-2. TILINE I/F Controller Input/Output Signals (Continued)

Signature	Sheet	Gate*	Description
IDLCLK-	7	UE078-6 (UCD089)	Idle clock. Loads TFDC status bits from RF bus into idle status register in the TILINE interrupt logic. IDLCLK- coincides with a low CLK3- pulse when W7 is addressed.
MDDATEN-	13	UC090-3 (UBB103)	Master device data enable. Active (low) when MDGOA and TLSYQ are both high. Enables RF bus to TILINE data drivers.
RFCLKA-, RFCLKB—,	7 -	UD062-9 UD062-7 (UBH074)	Register file clock A and B. Read/writecontrol signals to the register file. RFCLKA- controls register file bits 0-11, RFCLKB- controls bits 12-15. This split control allows independent update of the two sections of the register file. The register file clocks coincide with a low CLK3- or MDAC- signal. RFCLKA- is disabled on slave write cycles to W0.
RFMASTAD	6	UE050-6 (UCD058)	Register file master address. Strobe signal which enables register file address multiplexer. Multiplexer output is 0000 when RFMASTAD is high. RFMASTAD low enables RFTLAD to steer the multiplexer. RFMASTAD is not synchronized to CLK3-.
RFTLAD	6	UE050-7 (UCD058)	Register file TILINE address. Steering input to register file address multiplexer. With RFMASTAD low, RFTLAD low selects bits 11-15 of the microprocessor data bus, and RFTLAD high selects TILINE slave address bits 17-19 (biased by 1000). RFTLAD is not synchronized to CLK3-, but the address multiplexer outputs are latched into a register on the trailing edge of CLK3-.
SLVTMQ	6	UF050-12 (UCK058)	Slave terminate. Synchronized version of SLVTMD- output of state control ROM. Commands termination of TILINE slave read or write operation.
TLADRINC-	7	UE078-10 (UCD089)	TILINE address increment. Increments the 20-bit address stored in the TILINE address register between successive master read or write operations. Occurs in state 17 of a master cycle after MASTACT is cleared.
TLDBEN	10	UA078-10 (UAB089)	Gates microprocessor data bus output to register file bus.

Table 2-2. TILINE I/F Controller Input/Output Signals (Continued)

Signature	Sheet	Gate*	Description
TLIFRDY	6	UD114-2 (UBB129)	TILINE interface ready. Indication to 9900 microprocessor (via MPREADY) that register file is ready to read or write during next clock cycle. Used during TILINE master cycles and when transferring data between the 9900 and the register file. TLIFRDY is kept false while data is stabilized on the register file bus for transfer.
TLSXQ, TLSYQ	7 -	UB062-9 UB062-12 (UAG074)	Encoded bus control signals. Latched and synchronized versions of TLSXD and TLSYD. Used for directing data between microprocessor, TILINE, and register file.
TLSYQB-	9	UA078-13 (UAB089)	Enable register file output to register file bus. Inverted form of TLSYQ.
TLTLDATEN	11	UA078-6 (UAB089)	TILINE input data enable. Enables TILINE line receiver outputs onto RF bus. Decoded from inverted forms of TLSXQ, TLSYQ.

Note:

* Gate locations listed with pin numbers apply to assembly 2261690-1. Gate locations in parentheses apply to fineline assembly 2267295-1.

The SLVTMD- control output of the state control ROM has no actual effect until the rising (trailing) edge of the next CLK3- pulse. This signal is clocked into the SLVTMQ- flip-flop at the point of use. Similarly, the next state outputs are not clocked into the next state register until the trailing edge of the CLK3- pulse. Therefore, the minimum length of a state is one clock period. The state generator may remain in a given state indefinitely, as long as the next state bits from the ROM are the same as the current state. The state is updated once every clock period, but does not necessarily change when updated.

The RFMASTAD and RFTLAD outputs are the register file address multiplexer strobe control and steering control, respectively. These two signals are not synchronized to CLK3-. They select the multiplexed address input to the register file address latches, which are clocked by CLK3-. Therefore, the register file address does not change until the trailing edge of CLK3-.

The decoder ROM (TILINE and register file read/write control ROM) uses the next state address bits to select a block of eight addresses. The three least significant bits of the register file address select one word from the group of eight. When the register file address is 1000, the slave operation involves control word W0. For a slave write to WO, the decoder must generate an attention mask clock (ATMCLK-) to load the attention mask into an attention mask register that is separate from the register file.

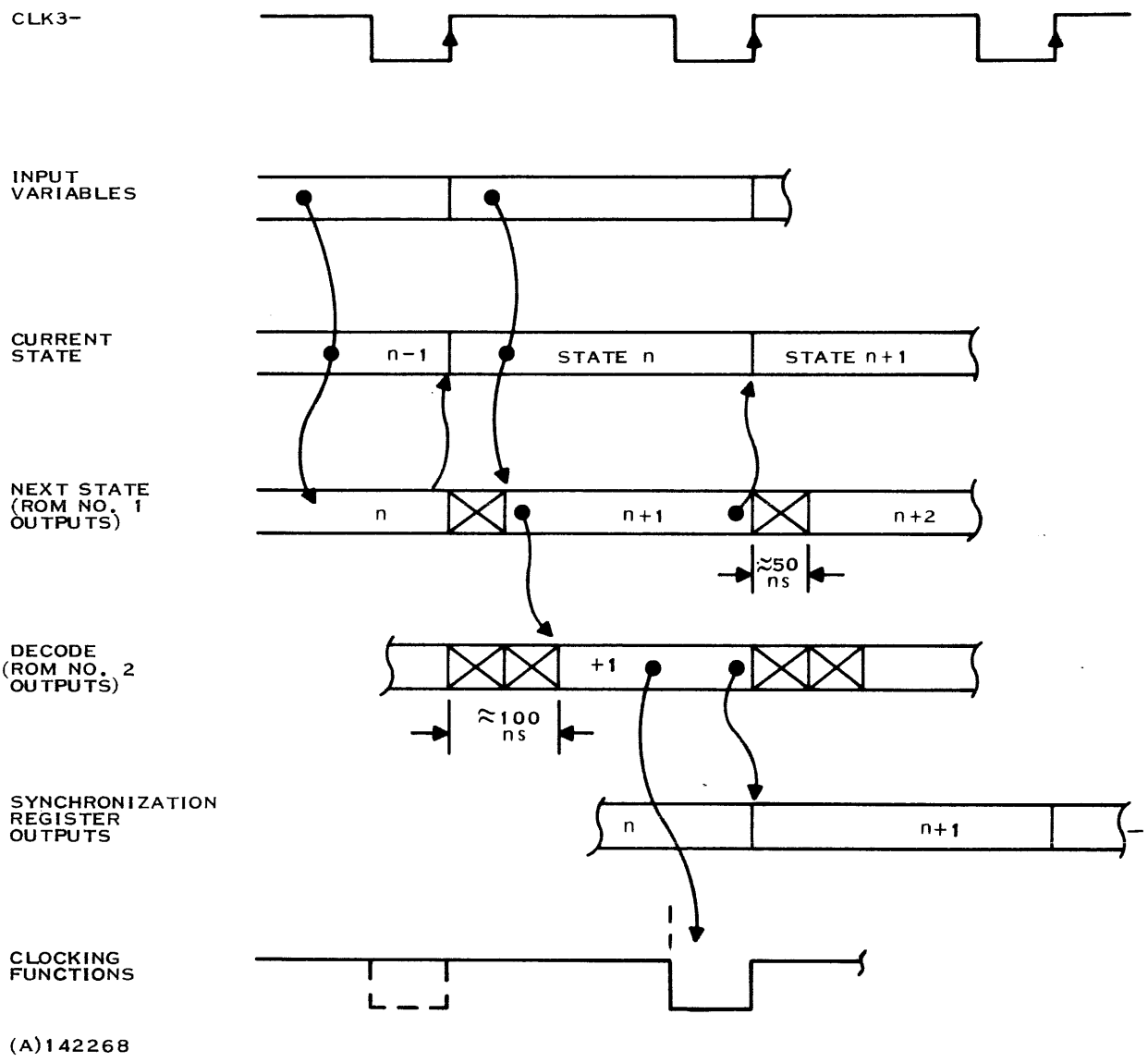

Figure 2-19. Simplified Timing for TILINE I/F Controller

The decoder ROM outputs are divided into a group of five outputs that are clocked into the synchronization register and a group of three outputs (TLOP0-2) which are not synchronized at this point. Those signals wired to the synchronization register are clocked on the trailing edge of CLK3-. Because the clock period is longer than the combined access time of the two ROMS, the synchronized versions of the outputs from both ROMs become available simultaneously.

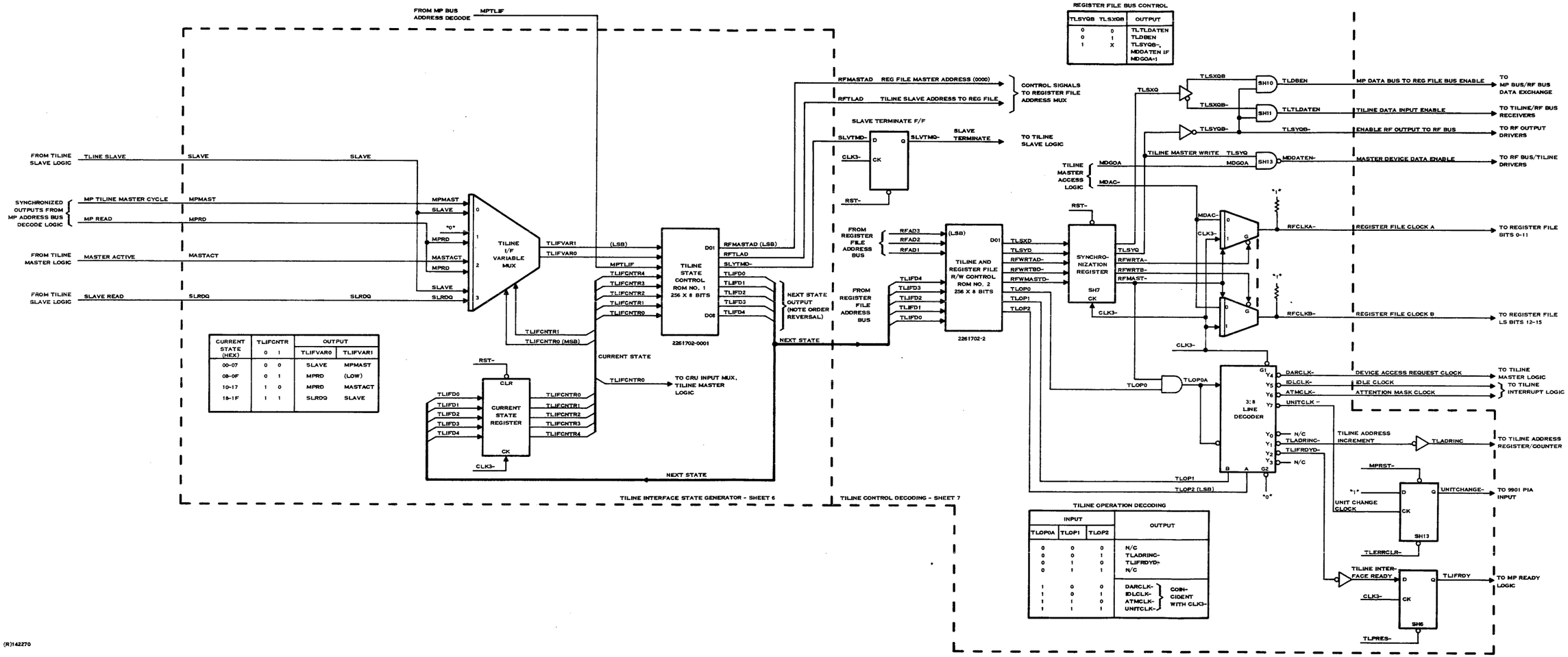

Figure 2-20. TILINE Interface Controller Logic

The decoder ROM does not have enough input or output bits to fully decode all of the outputs, so additional discrete decoding logic is required. The "clocking functions", DARCLK-, IDLCLK-, ATMCLK-, and UNITCLK- , are decoded from RFMAST- and the unsynchronized TLOP0-2 outputs of the decoder ROM. The clocking functions are strobed to coincide with the low CLK3- pulse and are available about 83 nanoseconds before the synchronized decoder outputs. TLADRINC- and TLIFRDYD- are decoded from TLOP0-2 and synchronized to CLK3- at the point of use. The other decoder outputs are synchronized to the trailing edge of CLK3- by the action of the synchronizing register.

2.5.9.3 TILINE I/F Controller Flowchart/State Diagram Description. Figure 2-21 is a combination flowchart and state diagram of I/F controller operations. Each rectangular block represents a state. The state number represents TLIFCNTR0-4, the five most significant address inputs to the state control ROM. The most important control functions performed in the state are also given.

Diamond-shaped decision blocks represent input variable conditions that determine the next state. The signature of the input variable appears in the decision block. If the input is true (high), the next state is determined by following the T (true) path out of the decision block. Otherwise, the F (false) path determines the next state. Up to three decision blocks may appear together because there are three input variables (MPTLIF and the two multiplexed variables, TLIFVAR0,1) for any state. If a variable is a don't care, no decision block appears for that variable. All state changes occur at the trailing edge of the next CLK3- pulse.

TLIFVAR0,1 multiplexer gating is controlled by two bits of the current state so that the variables which must be tested during any state are available during that state.

The flowchart may be divided into four major operations;

1. Idle loop — state 00
2. Microprocessor read/write register file — states 08-0C
3. TILINE slave read/write — states 18-1C
4. Microprocessor-initiated TILINE read/write master cycle — states 10-17

In the idle state, the input multiplexer address is 00 so the three least significant address inputs to the state control ROM are MPTLIF, SLAVE, and MPMAST (LSB). The next address output (TLIFD0-4) is always 00 unless one or more of the input variables are high, so the state controller loops on idle with an update each clock period.

The combination of input variables that occurs during the idle state determines the next state and the control outputs. The effects of the control outputs are included in the rectangle with the next state because they are latched at the same clock time as the state change.

The TILINE slave read or write cycle (state 18) is initiated by detecting a high SLAVE signal when the TILINE I/F controller is idle. SLAVE is the result of receiving a TILINE address that agrees with the base address of the TFDC and a TILINE go signal while the TFDC is in idle mode. A slave operation is initiated by an external master (990 CPU) if the right conditions exist in the TFDC. TILINE slave cycles are limited to register file addresses $10\text{-}1E_{16}$. The other sequences shown in the flowchart are initiated and controlled from within the TFDC.

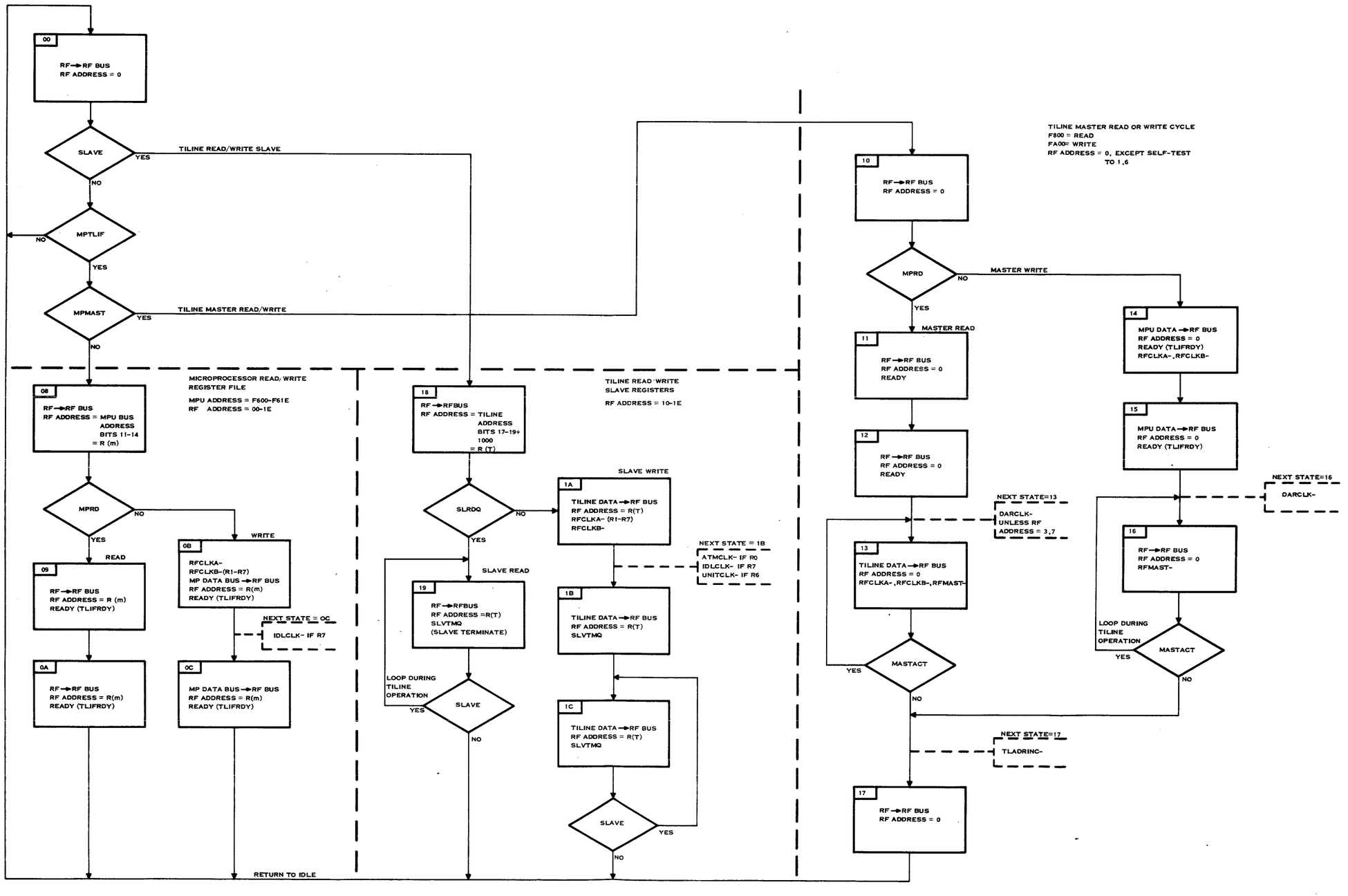

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Figure 2-21. TILINE I/F Controller Flowchart

The microprocessor read or write slave register operation (state 08) and the TILINE master read or write cycle (state 10) are initiated by the 9900 microprogram. Part of the 9900 address space is used to initiate and control these operations. ROM decoders detect memory references to the reserved addresses and issue the necessary control signals. For example, the MPTLIF (microprocessor - TILINE interface) and MPMAST (microprocessor master cycle) signals that select register file operations (state 08) or TILINE master cycle operations (state 10) are decoded from the 9900 address space and synchronized to CLK3-. The MPRD (microprocessor read) signal is decoded from the reserved addresses and the 9900 bus read/write control signals.

Addresses F600-F61E are used for read/write communication with the register files. The two least significant hexadecimal digits of the 9900 address select the individual register file address (00-1E), and read or write is selected based on the 9900 read/write control signals. Register file addresses 10-1E correspond to control words W0 through W7. Register file address 00 is a data transfer buffer address.

Address F800 selects a TILINE master read cycle, while FA00 selects a write cycle. Register file default address 00 is used for both read and write operations. Notice that a TILINE master write cycle involves two register file bus operations: transferring a word from MPU memory to the register file address and then reading the word out of the register file for transmission on the TILINE. On a master read cycle, the data is first read from the register file, and then TILINE data is loaded into the register file. Therefore, the data read from the register file is from the previous master cycle. The TILINE address register is incremented on completion of the master cycle.

2.5.9.4 TILINE Interface Controller ROM Listings. The TILINE interface controller is based on two ROM devices: TILINE state control ROM #1, P/N 2261702-1, and TILINE and register file R/W control ROM #2, P/N 2261702-2. Both of these ROMs are SN74S471 PROM devices (256 words x 8 bits) that are permanently programmed (burned) at the TI factory.

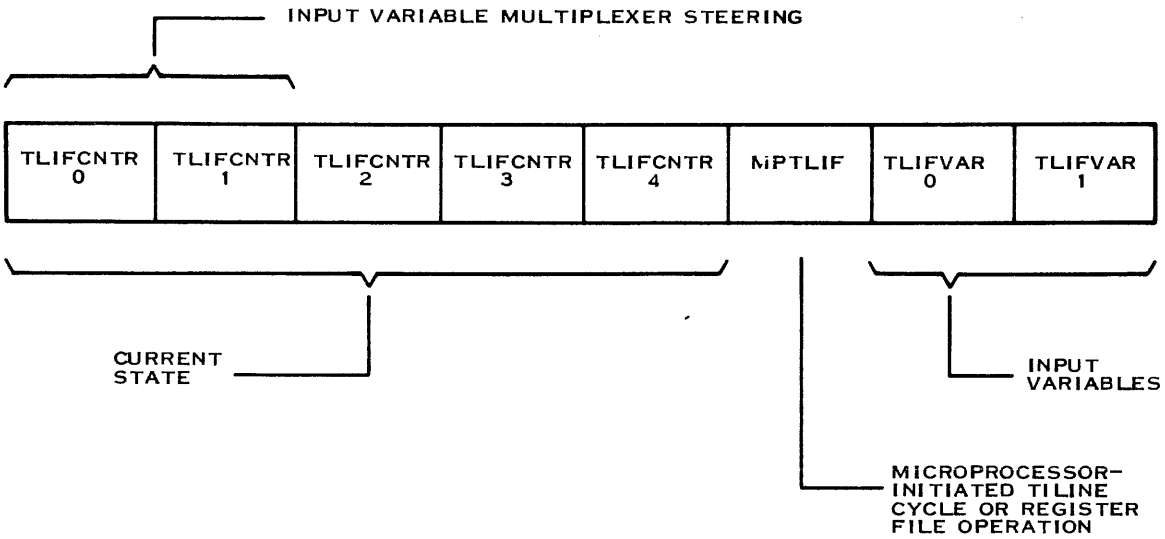
Refer to the HI-LO listing for the state control ROM, Table 2-3, and to the input and output word formats, Figure 2-22. Part A of the figure shows the input word (ROM address) format. The five most significant address bits are the current state, TLIFCNTR0-4. The remaining three bits are the input variables, MPTLIF, TLIFVAR0, and TLIFVAR1. TLIFVAR0 and TLIFVAR1 are multiplexed, with selection controlled by TLIFCNTR0 and TLIFCNTR1.

Each state corresponds to a block of eight words, which occupies two rows in the listing. State 00, for example, corresponds to addresses 000 through 007. The input variables, MPTLIF, TLIFVAR0, and TLIFVAR1 select one word from the block of eight. These input variables may be considered as a three-bit substate address. MPTLIF determines whether the selected output word is in the upper row (MPTLIF = 0), or the lower row (MPTLIF = 1). The listing is organized into four columns, 00, 01, 10, and 11, which correspond to the multiplexed variables, TLIFVAR0 and TLIFVAR1.

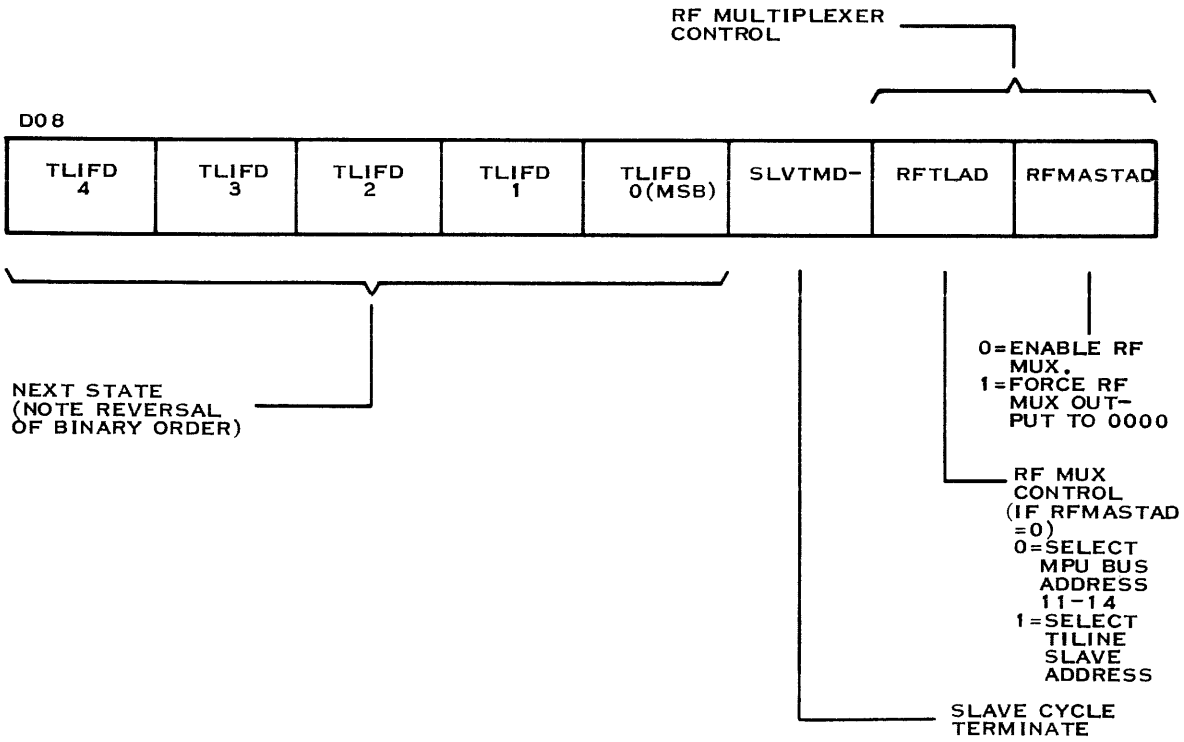
As an example, assume that the controller is in state 00 (idle), MPTLIF = 1, and TLIFVAR0,1 = 11. State 00 specifies the first two rows of the listing, and MPTLIF = 1 selects the second row. TLIFVAR0,1 = 11 selects the last column. The ROM output for these input conditions is LLLHHHHL.

All eight output words of a particular state may be identical or they may be different, depending upon the number of output paths and the control requirements. No generalizations are possible; it is necessary to check the listing to determine the exact output for a given set of input conditions.

A. INPUT (ADDRESS) FORMAT



B. OUTPUT FORMAT



(A)142271

Figure 2-22. TILINE State Control ROM Input/Output Formats

Table 2-3. TILINE State Control ROM Listing

State	Input Address	TLIFVAR0,1 00	01	10	11	
	000-003	LLLLLHLH	LLLLHHLH	LLLHHHHL	LLLHHHHL	MPTLIF = 0
00	004-007	LLLHLHLL	LLLLHHLH	LLLHHHHL	LLLHHHHL	MPTLIF = 1
	008-011	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
01	012-015	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	016-019	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
02	020-023	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	024-027	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
03	028-031	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	032-035	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
04	036-039	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	040-043	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
05	044-047	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	048-051	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
06	052-055	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	056-059	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
07	060-063	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	064-067	HHLHLHLL	HHLHLHLL	HLLHLHLL	HLLHLHLL	
08	068-071	HHLHLHLL	HHLHLHLL	HLLHLHLL	HLLHLHLL	
	072-075	LHLHLHLL	LHLHLHLL	LHLHLHLL	LHLHLHLL	
09	076-079	LHLHLHLL	LHLHLHLL	LHLHLHLL	LHLHLHLL	
	080-083	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
0A	084-087	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
	088-091	LLHHLHLL	LLLLLHLL	LLHHLHLL	LLLLLHLL	
0B	092-095	LLHHLHLL	LLLLLHLL	LLHHLHLL	LLLLLHLL	
	096-099	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
0C	100-103	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
	104-107	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
0D	108-111	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	112-115	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
0E	116-119	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	120-123	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
0F	124-127	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	

TMS 9900 Read/Write Register File

Table 2-3. TILINE State Control ROM Listing (Continued)

	128-131	LLHLHHLL	LLHLHHLL	HLLLHHLH	HLLLHHLH	
10	132-135	LLHLHHLL	LLHLHHLL	HLLLHHLH	HLLLHHLH	
	136-139	LHLLHHLH	LHLLHHLH	LHLLHHLH	LHLLHHLH	
11	140-143	LHLLHHLH	LHLLHHLH	LHLLHHLH	LHLLHHLH	
	144-147	HHLLHHLH	HHLLHHLH	HHLLHHLH	HHLLHHLH	
12	148-151	HHLLHHLH	HHLLHHLH	HHLLHHLH	HHLLHHLH	
	152-155	HHHLHHLH	HHLLHHLH	HHHLHHLH	HHLLHHLH	
13	156-159	HHHLHHLH	HHLLHHLH	HHHLHHLH	HHLLHHLH	
	160-163	HLHLHHLL	HLHLHHLL	HLHLHHLL	HLHLHHLL	TILINE Master Cycle
14	164-167	HLHLHHLL	HLHLHHLL	HLHLHHLL	HLHLHHLL	
	168-171	LHHLHHLH	LHHLHHLH	LHHLHHLH	LHHLHHLH	
15	172-175	LHHLHHLH	LHHLHHLH	LHHLHHLH	LHHLHHLH	
	176-179	HHHLHHLH	LHHLHHLH	HHHLHHLH	LHHLHHLH	
16	180-183	HHHLHHLH	LHHLHHLH	HHHLHHLH	LHHLHHLH	
	184-187	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
17	188-191	LLLLLHLH	LLLLLHLH	LLLLLHLH	LLLLLHLH	
	192-195	LHLHHHHL	LHLHHHHL	HLLHHHHL	HLLHHHHL	
18	196-199	LHLHHHHL	LHLHHHHL	HLLHHHHL	HLLHHHHL	
	200-203	LLLLLHLH	HLLHHLHL	LLLLLHLH	HLLHHLHL	
19	204-207	LLLLLHLH	HLLHHLHL	LLLLLHLH	HLLHHLHL	
	208-211	HHLHHLHL	HHLHHLHL	HHLHHLHL	HHLHHLHL	TILINE Slave Read/Write
1A	212-215	HHLHHLHL	HHLHHLHL	HHLHHLHL	HHLHHLHL	
	216-219	LLHHHLHL	LLHHHLHL	LLHHHLHL	LLHHHLHL	
1B	220-223	LLHHHLHL	LLHHHLHL	LLHHHLHL	LLHHHLHL	
	224-227	LLLLLHLH	LLHHHLHL	LLLLLHLH	LLHHHLHL	
1C	228-231	LLLLLHLH	LLHHHLHL	LLLLLHLH	LLHHHLHL	
	232-235	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1D	236-239	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	240-243	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1E	244-247	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	248-251	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1F	252-255	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	

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A number of states are unused and are not addressed by any valid combination of input signals. These states are all filled with zeros. Unused states are 01 through 07, 0D through 0F, and 1D through 1F.

The listing is organized into four major blocks of addresses, one block for each of the major types of operations controlled by the TILINE I/F controller. Recall that the two most significant bits of the current state control the steering of the TLIFVAR0,1 input multiplexer. Multiplexer selection ranges are states 00-07, 08-0F, 10-17, and 18-1F, as shown in Table 2-4.

Table 2-4. TILINE Interface Variable Multiplexer Steering

Current State	TLIFCNTR 0	TLIFCNTR 1	Output TLIFVAR0	Output TLIFVAR1
00 - 07	0	0	SLAVE	MPMAST
08 - 0F	0	1	MPRD	0
10 - 17	1	0	MPRD	MASTACT
18 - 1F	1	1	SLRDQ	SLAVE

Refer to the state control ROM output format, part B of Figure 2-22. The first five bits are TLIFD4 through TLIFD0, the next state address (in reverse bit order). To read the next state address, start at the fifth bit from the left and read right to left, substituting 0 for L and 1 for H. The next state forms part of the input address of the TILINE and register file R/W control ROM (decoder ROM) and becomes the current state on the next CLK3- pulse.

The three least significant bits of the state control ROM output are SLVTMD-, RFTLAD, and RFMASTAD. Note that SLVTMD- is active low, so an L in this bit position corresponds to a slave terminate command. RFTLAD is the steering input to the register file address multiplexer. RFTLAD has no effect unless RFMASTAD is low (L). RFMASTAD is the active low strobe input to the multiplexer. IF RFMASTAD is high (H), a default register file address of 00 appears at the multiplexer outputs. With RFMASTAD low, RFTLAD = L selects microprocessor address bits 11-14, and RFTLAD = H selects TILINE slave address bits 17-19, biased by a hardwired 1000.

Most of the state control ROM outputs have no effect until the trailing edge of the next CLK3- pulse. The multiplexer control takes place immediately, but the RF address multiplexer output feeds a clocked register, so the actual register file address is unchanged until CLK3-. The next state output does, however, go directly into the decoder ROM without synchronization.

Refer to the HI-LO listing for the TILINE and register file R/W control ROM, Table 2-5. Also refer to the input/output word formats, Figure 2-23. The five most significant address bits are the next state, TLIFD0-4. Note that the bits are in binary order. The three least significant bits are register file address bits RFAD1-3.

The next state (TLIFD0-4) selects a block of eight word addresses, and the register file address selects one of the eight words for output.

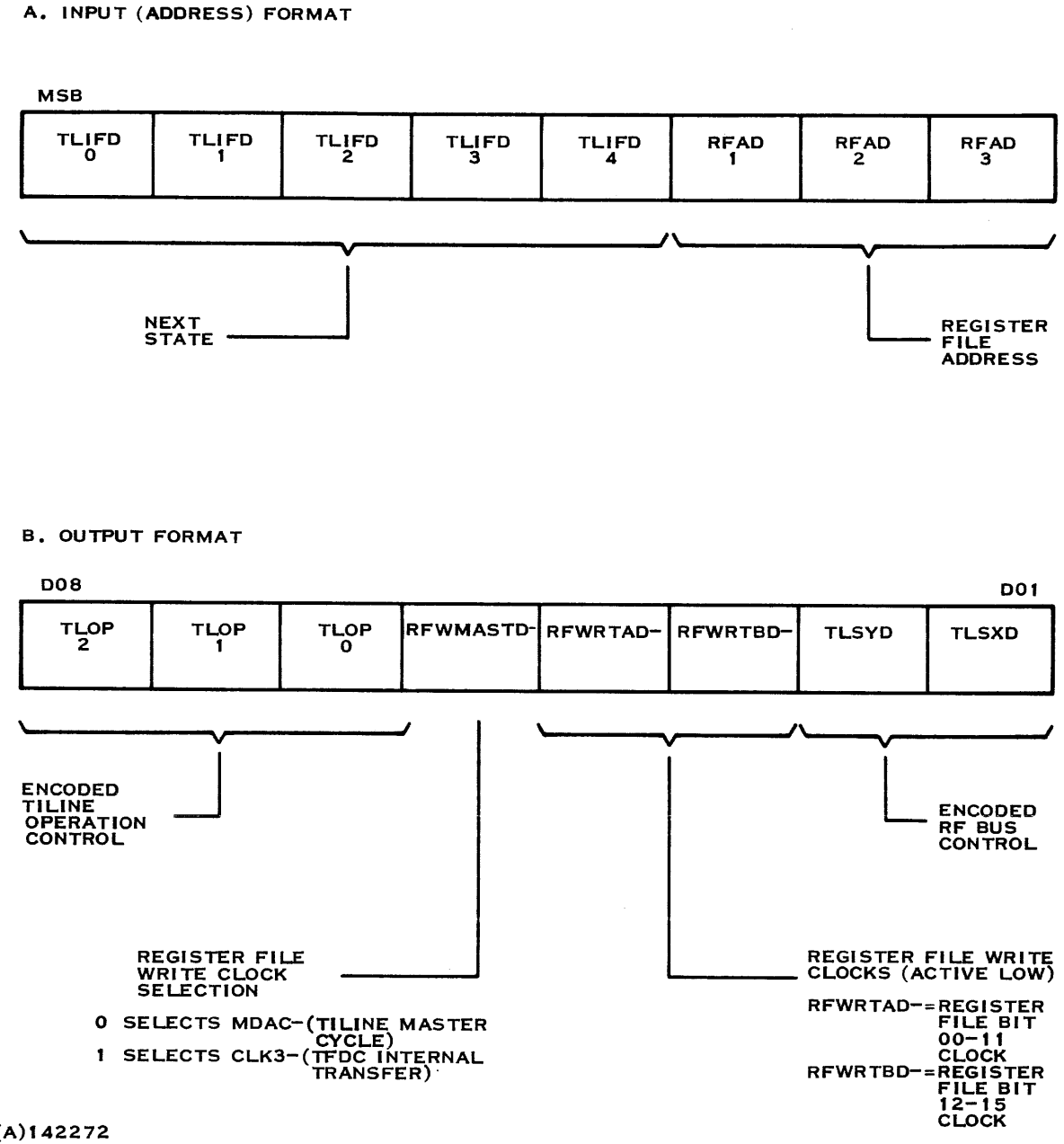

Figure 2-23. TILINE and Register File R/W Control ROM Word Formats

The eight output words of a particular state may be all identical, or may be different, depending upon the number of output paths and the control requirements. If all eight words are identical, the register file address is not considered in determining the control outputs.

A number of states are unused. These states do not appear in the next state output of the state control ROM. Unused states are 01-07, 0D-0F, and 1D-1F. The unused states are programmed with all zeros.

Table 2-5. TILINE and Register File R/W Control ROM Listing

Next State	Input Address				
	000-003	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL
00	004-007	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL
	008-011	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
01	012-015	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	016-019	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
02	020-023	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	024-027	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
03	028-031	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	032-035	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
04	036-039	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	040-043	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
05	044-047	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	048-051	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
06	052-055	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	056-059	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
07	060-063	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	064-067	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL
08	068-071	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL
	072-075	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL
09	076-079	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL
	080-083	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL
0A	084-087	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL
	088-091	LHLHHLLH	LHLHLLLH	LHLHLLLH	LHLHLLLH
0B	092-095	LHLHLLLH	LHLHLLLH	LHLHLLLH	LHLHLLLH
	096-099	LLLHHHLH	LLLHHHLH	LLLHHHLH	LLLHHHLH
0C	100-103	LLLHHHLH	LLLHHHLH	LLLHHHLH	HLHHHHLH
	104-107	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0D	108-111	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	112-115	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0E	116-119	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
	120-123	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0F	124-127	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL

Idle

TMS 9900 Read/Write Register File

Table 2-5. TILINE and Register File R/W Control ROM Listing (Continued)

	128-131	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
10	132-135	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
	136-139	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL	
11	140-143	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL	
	144-147	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL	
12	148-151	LHLHHHHL	LHLHHHHL	LHLHHHHL	LHLHHHHL	
	152-155	LLHLLLLL	LLHLLLLL	LLHLLLLL	LHLLLHHL	
13	156-159	LLHLLLLL	LLHLLLLL	LLHLLLLL	LHLLLHHL	
	160-163	LHLHLLLH	LHLHLLLH	LHLHLLLH	LHLHLLLH	TILINE Master Cycle
14	164-167	LHLHLLLH	LHLHLLLH	LHLHLLLH	LHLHLLLH	
	168-171	LHLHHHLH	LHHHHHLH	LHLHHHLH	LHLHHHLH	
15	172-175	LHLHHHLH	LHLHHHLH	HHHHHHLH	LHLHHHLH	
	176-179	LLHLHHHL	LLHLHHHL	LLHLHHHL	LLHLHHHL	
16	180-183	LLHLHHHL	LLHLHHHL	LLHLHHHL	LLHLHHHL	
	184-187	HLLHHHHL	HLLHHHHL	HLLHHHHL	HLLHHHHL	
17	188-191	HLLHHHHL	HLLHHHHL	HLLHHHHL	HLLHHHHL	
	192-195	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
18	196-199	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
	200-203	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
19	204-207	LLLHHHHL	LLLHHHHL	LLLHHHHL	LLLHHHHL	
	208-211	LLLHLHLL	LLLHLLLL	LLLHLLLL	LLLHLLLL	TILINE Slave Read/Write
1A	212-215	LLLHLLLL	LLLHLLLL	LLLHLLLL	LLLHLLLL	
	216-219	LHHHHHLL	LLLHHHLL	LLLHHHLL	LLLHHHLL	
1B	220-223	LLLHHHLL	LLLHHHLL	HHHHHHLL	HLHHHHLL	
	224-227	LLLHHHLL	LLLHHHLL	LLLHHHLL	LLLHHHLL	
1C	228-231	LLLHHHLL	LLLHHHLL	LLLHHHLL	LLLHHHLL	
	232-235	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1D	236-239	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	240-243	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1E	244-247	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
	248-251	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1F	252-255	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	

Refer to the output word format, part B of Figure 2-23. The first three bits of the output word are the encoded TILINE operation control bits, TLOP2-TLOP0. TLOP0 is externally ANDed with RFMAST- to produce TLOP0A. TLOP0A, TLOP1, and TLOP2 are decoded as shown in Table 2-6.

Table 2-6. TILINE Operation Control Decoding

Inputs			Output	Use	Occurrence
TLOP0A	TLOP1	TLOP2			
0	0	0	None		
0	0	1	TLADRINC-	Increments TILINE address counter/register.	Next state = 17
0	1	0	TLIFRDYD-	Enables 9900 MPREADY during TILINE cycles.	States 9,A,B,11, 12,14.
0	1	1	None		
1	0	0	*DARCLK-	Initiates a TILINE master cycle.	Next state = 13
1	0	1	*IDLCLK-	Latches interrupt and W7 interrupt generation bits.	W7 only, next state = 0C,1B.
1	1	0	*ATMCLK-	Latches attention mask bits for interrupt logic.	W0 only, next state = 1B.
1	1	1	*UNITCLK-	Generates unit change interrupt to 9900 for update of W0 unit status.	W6 only, next state = 15,1B.

Note:

* = coincident with CLK3- pulse

Notice that the bit order shown in the decoding chart is the reverse of the order in the ROM output word. The order shown corresponds to the hardware decoding scheme.

The remaining five bits of the output word are synchronized to the trailing edge of CLK3- before use.

The fourth bit of the ROM output word is the active-low RFMASTD- signal which is latched on the trailing edge of CLK3- to become RFMAST-. RFMAST- selects either CLK3- (RFMAST- = H) or MDAC- (RFMAST- = L) as the register file clocking signal (RFCLKA-, RFCLKB-). RFWRTBD- must be low to write to register file bits 12-15, and RFWRTAD- must be low to write to register file bits 00-11. RFWRTBB- is disabled when writing to W0 from the TMS 9900; RFWRTAD- is disabled when writing to W0 from the TILINE.

The last two bits of the output word are the encoded register file bus control bits, TLSYD and TLSXD. These signals are synchronized (as TLSYQ and TLSXQ) to CLK3- and decoded as shown in Table 2-7.

Table 2-7. Register File Bus Control Decoding

Inputs		Output	Description
TLSYQ	TLSXQ		
0	0	TLTLDATEN	TILINE data input enable
0	1	TLDBEN	MPU data bus to RF bus enable
1	X	TLSYQB-	Register file to RF bus enable
1	X	MDDATEN- if MDGOA = 1	RF bus to TILINE enable (TFDC master write)

The two ROM listings and a knowledge of current inputs are necessary to follow the operations of the TILINE interface controller. The current state (TLIFCNTR0-3) restricts the state controller ROM to a particular block of eight addresses. This current state also steers the TILINE I/F variable multiplexer to select a pair of input variables. Input variables MPTLIF, TLIFVAR0, and TLIFVAR1 may be regarded as a "substate". The input variable conditions uniquely select one of the eight possible addresses. The word stored at that address appears at the ROM output after the ROM settling time.

The word at the output of the state control ROM selects the next register file address and issues a slave terminate if required. This word also determines the next state. Note that the next state address appears in reverse order, least significant bit first.

The next state selects a block of eight word addresses in the TILINE and register file R/W control ROM, and the current register file address selects the individual word. Use Table 2-6 to find the control outputs of the second ROM. The outputs of this second ROM are stable after the sum of the two ROM access times, which is considerably less than one clock period. Therefore, the outputs of the ROM are simultaneously available for most of the clock cycle. The clocking outputs (DARCLK-, IDLCLK-, ATMCLK-, UNITCLK-) are active for the duration of the low CLK3- pulse. The other control outputs of both ROMs are effective on the trailing (rising) edge of CLK3-. This clock edge also advances the state controller to the next state.

Decoding tables for the encoded control functions are provided in this paragraph. The flowchart provides an overview of TILINE I/F controller operations and may serve as a check while following the ROM listings.

2.6 TFDC CENTRAL PROCESSOR SECTION

The TFDC is essentially a special purpose computer with an instruction set of eight normal mode commands and eight extended mode commands. The normal mode commands are Store Registers, Write Format, Read Data, Write Data, Read ID, No-op, Seek, and Restore. The extended mode commands are Extract Interlace Factor, Write Interlaced Sector Format, Read Delete, Write Delete, Read Unformatted, Write Controller Memory, Read Controller Memory, and Extended Test. These 16 macroinstructions are implemented in hardware and in a fixed control program burned into a read-only memory (ROM). The central processor section executes the instructions in the control program, based on setup parameters from control words W0–W7, and status/control/data inputs from the TILINE interface and the drive interface.

2.6.1 Introduction to Processor Organization

The processor is based on the TMS 9900 microprocessor and the TMS 9901 peripheral interface adapter (PIA). Refer to Figure 2-24, a block diagram that shows the organization of the processor section and the major buses.

2.6.1.1 Microprocessor Introduction. The TMS 9900 microprocessor is a 16-bit processor with a 15-bit address output bus and a 16-bit data input/output bus. The microprocessor also has a serial, bit-addressable input/output system which shares the address bus. This serial I/O system is used for control outputs and status inputs to/from the logic external to the microprocessor.

2.6.1.2 Timing and Reset Introduction. The TMS 9900 requires four nonoverlapping clock phases to control the internal sequence of operations for execution of 9900 machine language instructions. The timing logic provides four crystal-controlled clock phases at 3 MHz. It also provides a separate microprocessor clock output to synchronize external logic operations to the microprocessor operating cycle. The reset logic provides synchronized and unsynchronized reset outputs to the TFDC logic. These resets are initiated by an I/O reset from the 990/5, 990/10 or 990/12 processor or by power failure warning or power reset from the 990 chassis power supply. Microprocessor clock and reset outputs are supplied by the TIM 9904/SN74LS362 four-phase clock oscillator.

2.6.1.3 TMS 9901 Peripheral Interface Adapter (PIA) Introduction. The TMS 9901 PIA serves as an external interrupt priority encoder (with maskable interrupts), a multiport input and output register for the serial interface, and an interval timer.

2.6.1.4 Communications Register Unit (CRU) I/F Logic Introduction. The CRU I/F logic performs input data selection and output data routing for the serial CRU interface.

2.6.1.5 Read-Only Memory (ROM) Introduction. A TMS 9900 control program is permanently stored in the read-only memory. This control program operates whenever power is applied to the TFDC. All TFDC operations are controlled by the operating sequences stored in the ROM. The program is written in 9900 machine language.

2.6.1.6 Random-Access Memory (RAM) Introduction. The RAM provides 256 words of read/write memory for workspace storage and temporary variable storage.

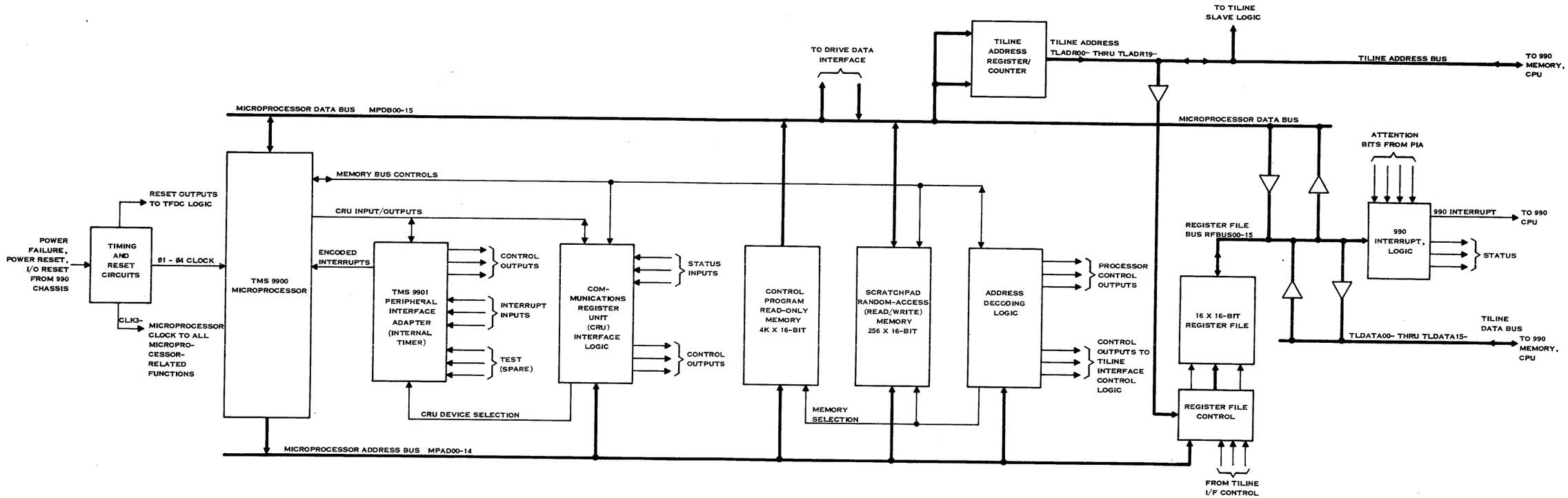

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Figure 2-24. Basic Block Diagram of TFDC Central Processor Section

2.6.1.7 Address Decoding Logic. The control program ROM and the scratchpad RAM occupy a very small percentage of the address space available on the TMS 9900 memory bus. Some of the otherwise unused addresses are used for memory-mapped input/output and special function control. Memory-mapped I/O assigns memory addresses to I/O devices so that the TMS 9900 microprocessor can send and receive data using normal memory data transfer instructions, such as MOV (move).

2.6.1.8 Register File Introduction. The register file is a high-speed, 16-word memory which is used for storage of control words W0-W7 (SLVWD0-SLVWD7). These contain the TFDC setup parameters which are sent to the TFDC to initiate disk operations. These control words are updated as status words during the course of an operation. They may be read back by the 990 processor after the operation terminates. The register file also serves as a one-word storage buffer for data transfers between the 990 memory and the disk. The register file bus (RFBUS00-15) provides register file I/O and data connections to the TILINE data and microprocessor data buses.

2.6.1.9 990 Interrupt Logic Introduction. TFDC interrupts to the host 990 processor (not the TMS 9900 microprocessor) are generated by the 990 interrupt logic. This logic includes the attention interrupt mask register and the idle status register. These registers are loaded from the register file bus.

2.6.1.10 TILINE Address Register/Counter. TILINE master access cycles initiated from the TFDC require the TFDC to provide the 20-bit TILINE address. The TILINE address register/counter is loaded (by two separate microprocessor data bus cycles) as part of the TILINE operation setup. The counter is incremented on successive TILINE data transfers by the TILINE I/F control logic.

2.6.2 TMS 9900 Microprocessor

This paragraph describes the TMS 9900 microprocessor device, without regard to its use in the TFDC. Subsequent paragraphs describe the way that the TMS 9900 device is used in the TFDC and the organization of the control program for the TMS 9900. Readers who are familiar with this device may wish to skip ahead to the paragraphs that describe TMS 9900 operation in the TFDC.

The TMS 9900 is a 16-bit microprocessor on a chip which, when combined with an external memory and four-phase clock source, functions as a general-purpose computer. The TMS 9900 microprocessor architecture includes vectored interrupts and memory-located workspace registers for efficient context switching. There are two microprocessor I/O channels, a bit-oriented, command-driven Communications Register Unit (CRU) and a 16-bit memory channel with 64K bytes of memory address space. The memory channel may be used for direct memory access (DMA) I/O with the addition of external DMA logic. Or, it may be used as a memory-mapped I/O channel. Memory-mapped I/O assigns addresses in memory space to input/output devices and transfers data with normal memory access instructions, such as move (MOV).

The TMS 9900 features a flexible set of 64 instructions with 8 addressing modes. A summary of TMS 9900 microprocessor characteristics is provided in Table 2-8. A simplified block diagram of the TMS 9900 internal structure is shown in Figure 2-25.

Table 2-8. TMS 9900 Microprocessor Characteristics

Item	Characteristic
Word size	16 bits
Maximum memory	32K words
Clock rate	3 MHz
Instruction cycle time	Average-5 microseconds Minimum-2 microseconds Maximum-31.5 microseconds
Addressing modes	Immediate Workspace register Workspace register indirect Symbolic memory (direct) Indexed memory Workspace register indirect auto-increment Program Counter Relative CRU Relative
Interrupts	16 capability
Registers	16
Input/Output	Direct (CRU) and direct memory access (DMA)
Address bus	15 bits
Data bus	16 bits
Power	+ 12 Vdc, ± 5 Vdc
Package	64 pins, dual-in-line package
Technology	N-channel silicon gate
Instruction set	64 instructions, including hardware multiply and divide

2.6.2.1 Architecture. The memory word of the TMS 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits each. The instruction set of the TMS 9900 allows both word and byte operands. All memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte. The memory space is 65 536 bytes or 32 768 words. Word and byte formats are shown in Figure 2-26.

Registers and Memory. The TMS 9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspaces replace internal hardware registers as program data registers. Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented.

The status register (ST) contains the interrupt mask level and status information pertaining to the instruction operation. Each bit in the register signifies a particular function or condition that exists in the microprocessor. Figure 2-27 illustrates the status bit assignments. Some instructions use the status register to check for a condition. Others affect the values of individual status bits, and others load the entire status register with a new set of parameters. The *Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide* details the effect of each instruction on the status register.

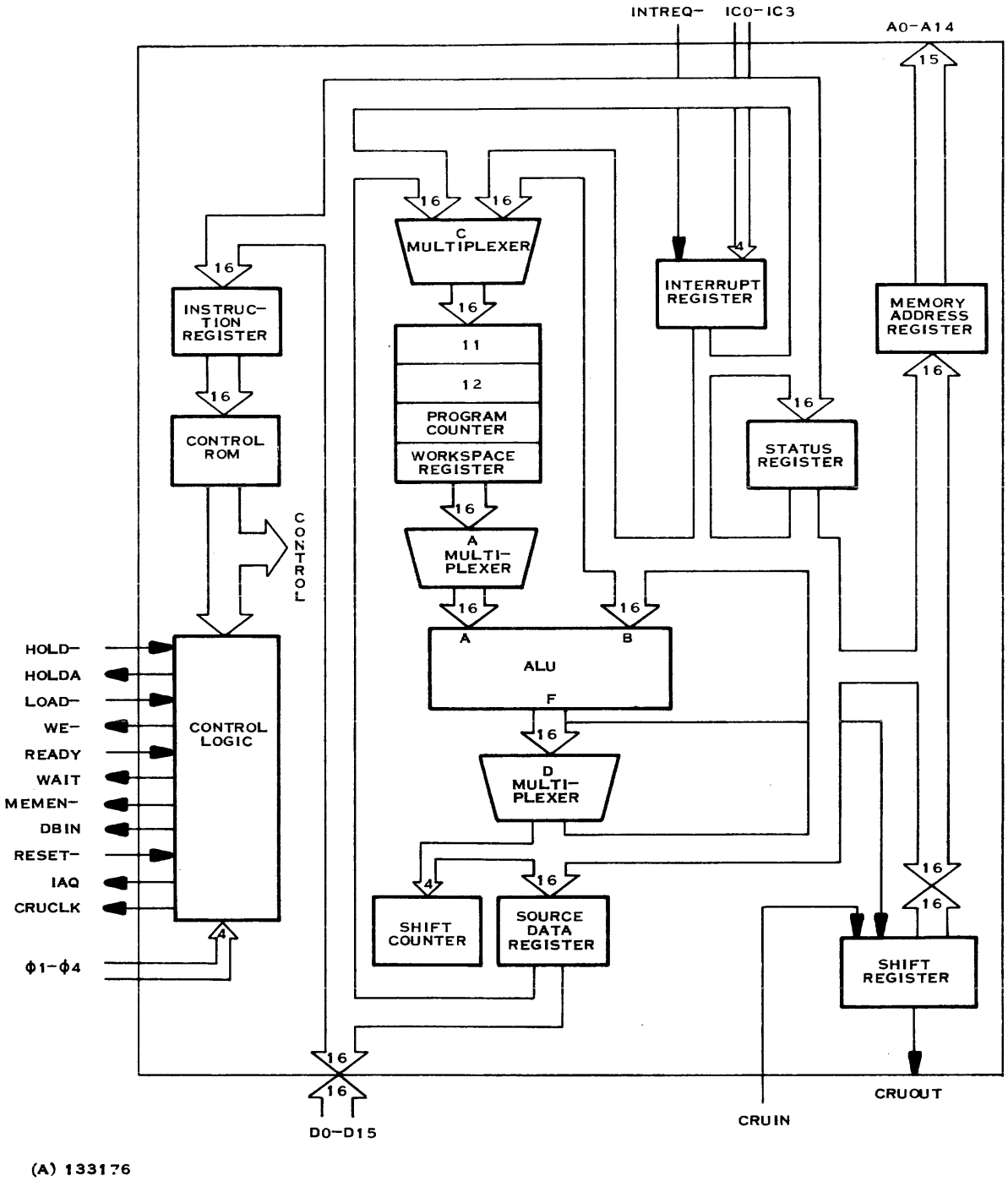


Figure 2-25. TMS 9900 Microprocessor Architecture

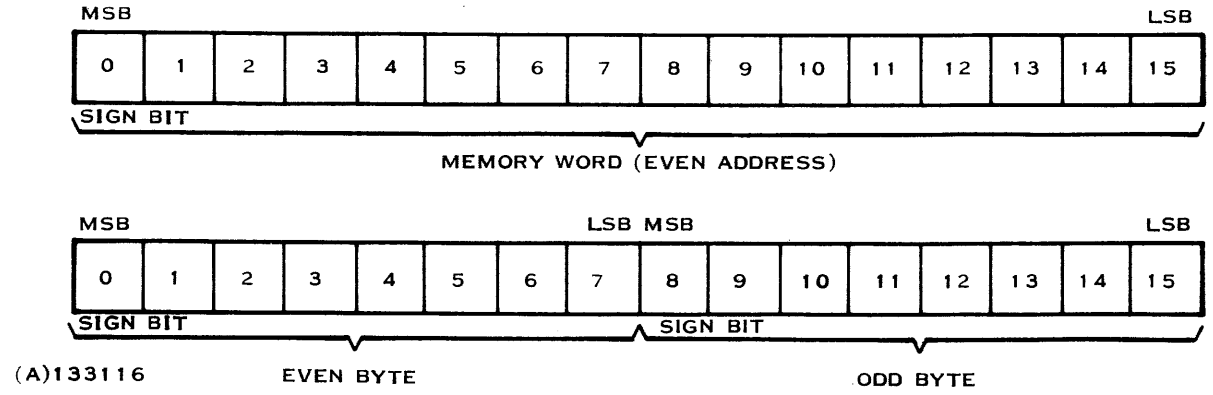


Figure 2-26. Microprocessor Word and Byte Format

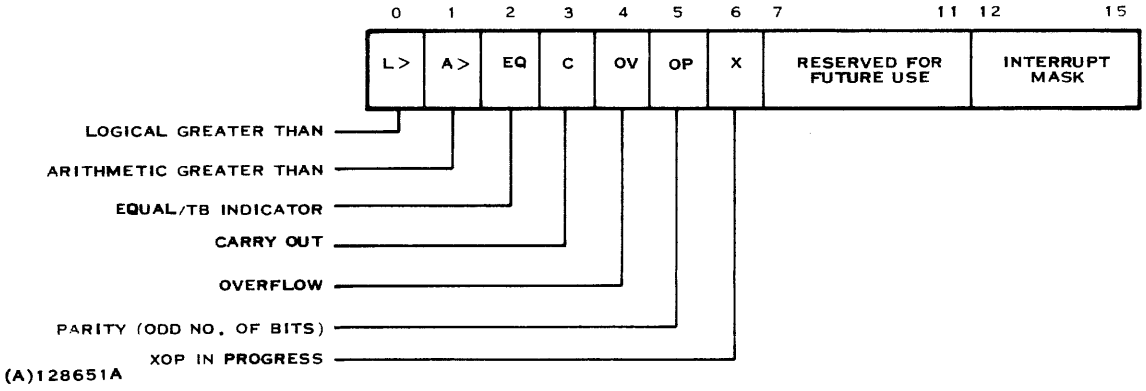


Figure 2-27. Status Register Bit Assignments

The workspace pointer register (WP) contains the address of the first word in the currently active set of workspace registers. A workspace register set occupies 16 contiguous memory words in the general memory area. Each workspace register may hold data or addresses and function as an operand register, accumulator, address register, or index register. Some workspace registers take on special significance during execution of certain instructions. Table 2-9 lists each of these dedicated workspace registers and the instructions that use them. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer as shown in Figure 2-28.

Table 2-9. Dedicated Workspace Registers

Register		Contents Used During
0	Shift count (optional)	Shift instructions (SLA,SRA, SRC and SRL
11	Return address	Branch and Link Instruction (BL)
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrrupt, LOAD, and RESET)
14	Saved PC register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
15	Saved ST registers	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)

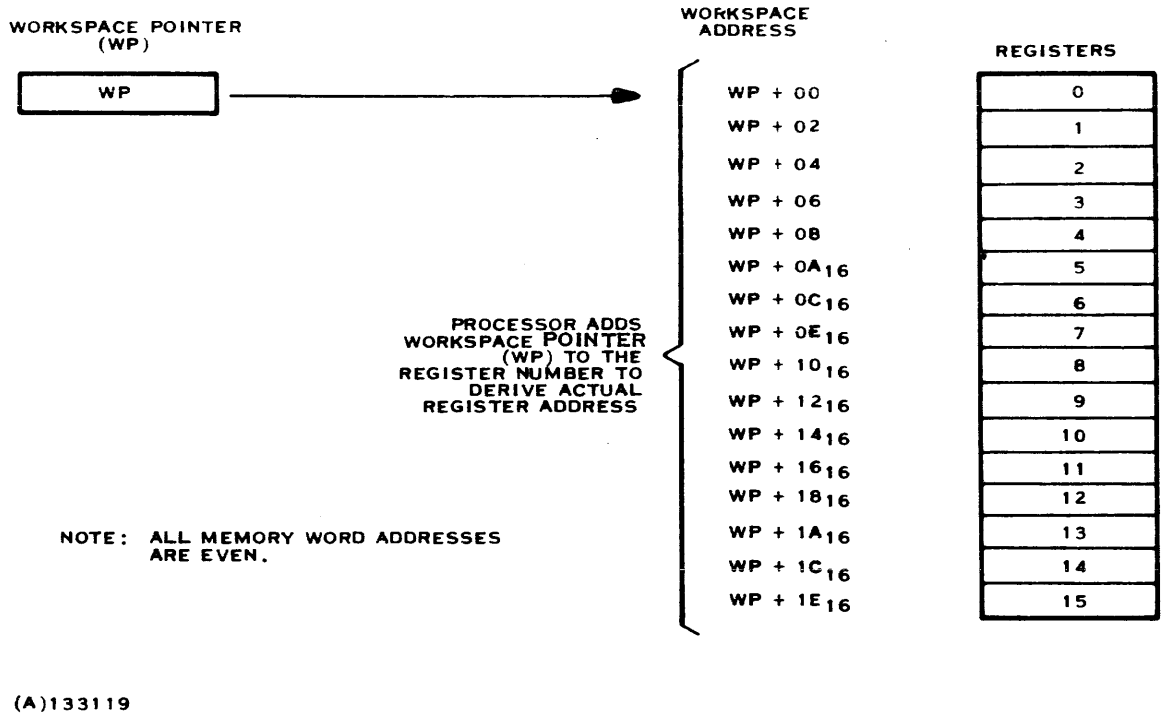


Figure 2-28. TMS 9900 Workspace Pointer and Registers

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). Such an operation using a conventional multiregister arrangement requires that at least part of the contents of the register set be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the contents of the program counter, status register, and workspace pointer, the microprocessor accomplishes a complete context switch with only three store cycles and two fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use by the new routine. The contents of the WP, PC, and ST registers from the previous routine have been saved in new workspace registers 13, 14, and 15, respectively. A corresponding saving in time occurs when the original context is restored. Instructions in the microprocessor that result in a context switch include:

- Branch and Load Workspace Pointer (BLWP)
- Return with Workspace Pointer (RTWP)
- Extended Operation (XOP)

The device interrupts RESET- and LOAD- also cause a context switch by forcing the microprocessor to trap to a service subroutine.

Interrupts. The TMS 9900 microprocessor can accommodate 16 interrupt levels with the highest priority level 0 and the lowest level 15. Level 0 is reserved for the RESET- function, and all other levels may be used for external devices.

When the interrupt request signal (INTREQ-) is active, the microprocessor compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the microprocessor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace.

The microprocessor then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for a level 0 interrupt that loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The microprocessor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur.

All interrupt requests should remain active until recognized by the microprocessor as part of the device service routine. The individual service routines must reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to complete processing of the lower priority interrupt. All interrupt subroutines should terminate with the return instruction (RTWP) to restore original program parameters.

Input/Output. The TMS 9900 microprocessor uses a versatile direct command-driven I/O interface called the Communications Register Unit (CRU). The CRU provides up to 4096 directly-addressable input bits and 4096 directly-addressable output bits. Input and output bits can be addressed individually or in fields of from 1 to 16 bits. The microprocessor employs three dedicated

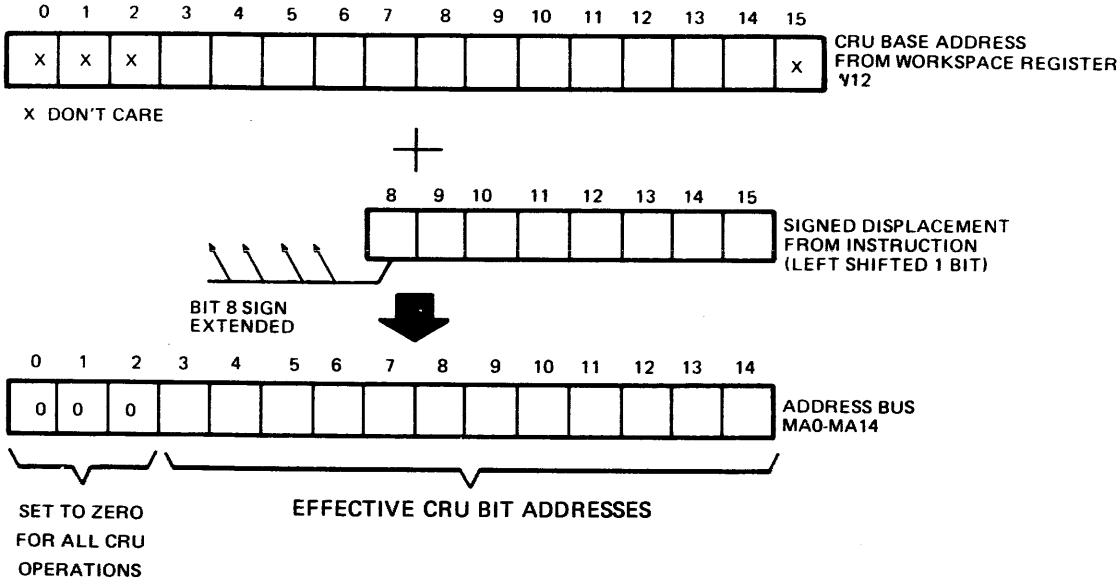
I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus as the interface to the CRU system. The microprocessor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transaction operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The microprocessor performs three single-bit CRU functions: Test Bit (TB), Set Bit to One (SBO), and Set Bit to Zero (SBZ). To identify the bit to be tested or modified, the microprocessor develops a CRU bit address and places it on the address bus, A3 to A14. A0–A2 are forced to zero for all CRU operations.

For the two output operations (SBO and SBZ), the microprocessor places bit 7 of the instruction word on the CRUOUT line and generates a CRUCLK pulse to load the bit into the CRU device. Bit 7 is a one for SBO and a zero for SBZ. The test bit instruction is an input operation that transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (equal bit).

The microprocessor develops a CRU-bit address for the single-bit operations from the CRU base address contained in workspace register 12 (W12) and the signed displacement contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from bits 3–14 in workspace register 12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 2-29 illustrates the development of a single-bit CRU address.



(A)133120

Figure 2-29. TMS 9900 Single-Bit CRU Address Development

The microprocessor performs two multiple-bit CRU operations: Store Communications Register (STCR) and Load Communications Register (LDCR). These operations transfer data between the CRU field and the memory address specified in the instruction. Any number of bits from 1 to 16 may be transferred by one instruction.

The LDCR instruction includes a memory address for the source operand, a displacement (relative to the CRU base address in R12), and a bit count. This instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, these bits come from the right-justified field within the addressed byte of the memory word. This is the upper byte (0-7) for even addresses and the lower byte (8-15) for odd addresses. If the LDCR involves nine or more bits, these bits come from the right-justified field within the whole memory word.

Refer to Figure 2-30, which summarizes an LDCR operation. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

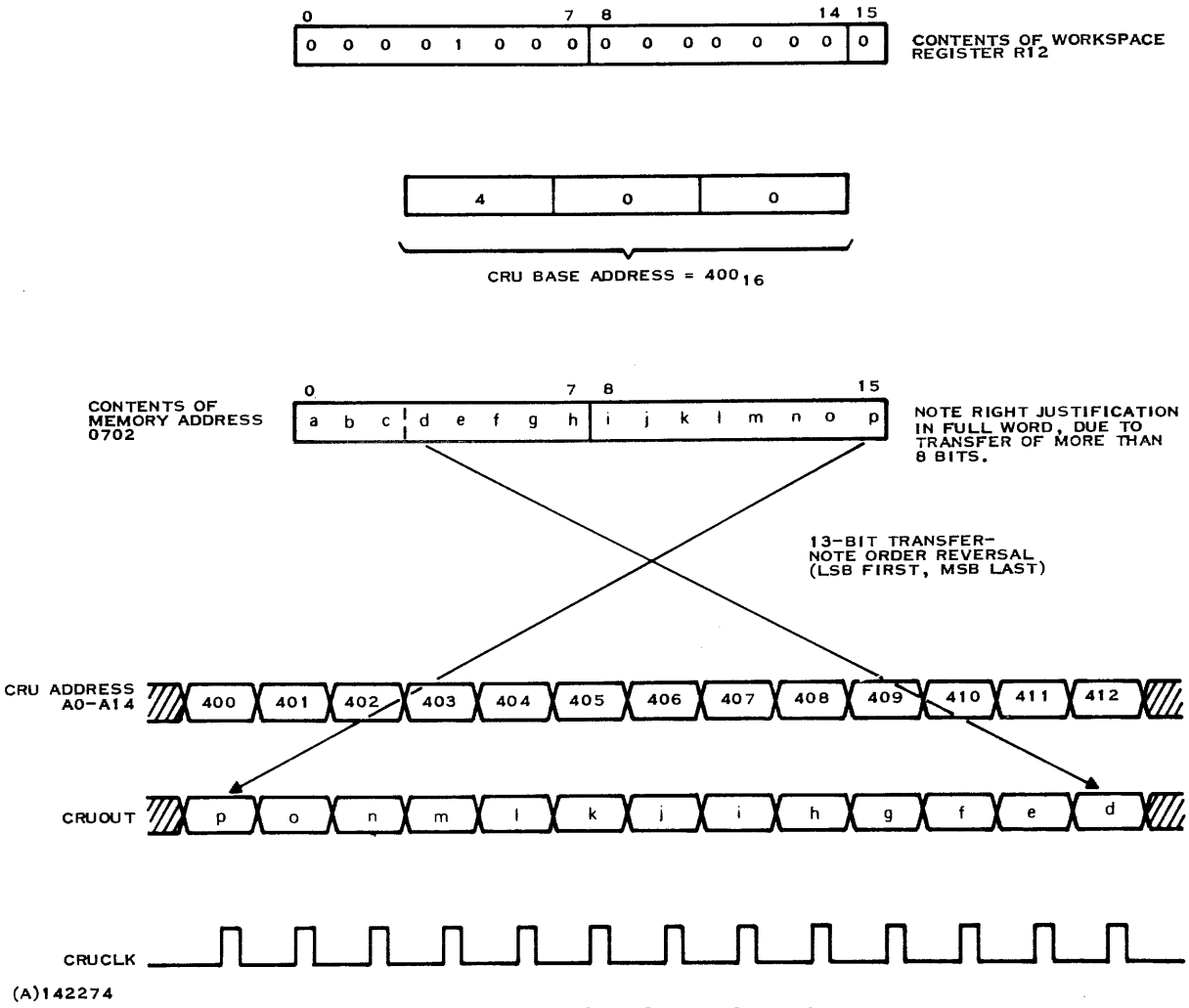
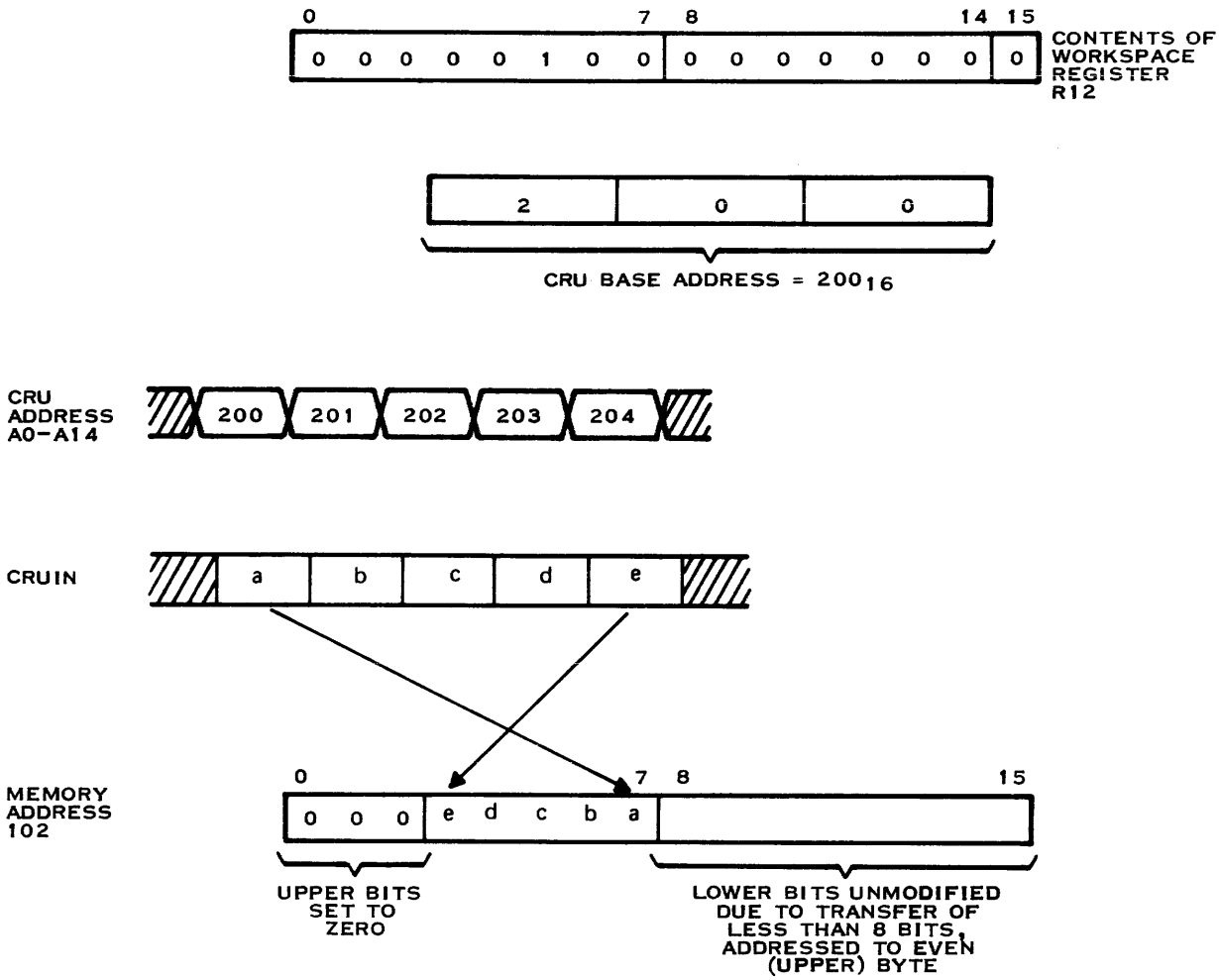


Figure 2-30. Multiple-Bit CRU Output Operation — LDCR

An STCR instruction, Figure 2-31, transfers data from the CRU to memory. An STCR instruction includes a memory destination address, a displacement from the CRU base address, and a bit count. If the operation involves eight bits or less, the transferred data is stored right-justified in the addressed memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

2.6.2.2 Interface Signals. TMS 9900 microprocessor pin assignments and interface signal functions are described in Figure 2-32 and Table 2-10.

2.6.2.3 Timing. A basic memory read and write cycle, a hold operation, and a CRU operation are discussed in the following paragraphs with emphasis placed on the timing of the interface signals involved in each operation.



(A)142275

Figure 2-31. Multiple-Bit CRU Input Operation — STCR

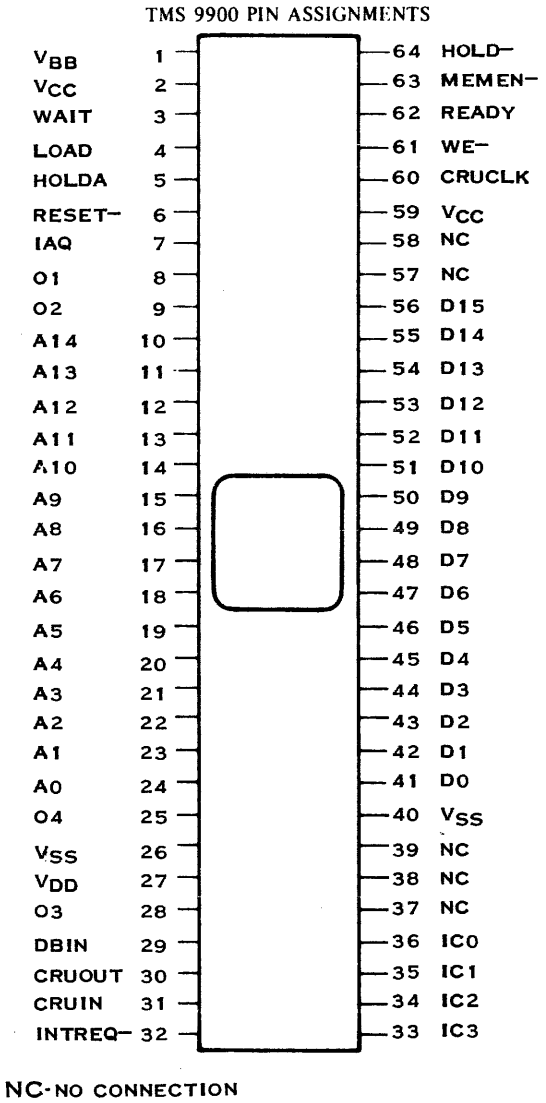


Figure 2-32. TMS 9900 Pin Assignments

Memory Read Timing. A memory read cycle with no wait states is shown in Figure 2-33. Memory enable (MEMEN-) and data bus in (DBIN) go active at the start of the machine cycle, on the leading edge of phase 2 clock. The memory address appears on address bus bits A0 through A14. The TMS 9900 data output drivers, D0-D15, are disabled to prevent conflicts with the input data. The memory write signal (WE-) remains inactive (high) during a read cycle. If the read cycle is also an instruction acquisition cycle, IAQ goes active (high) during the cycle.

The READY input is sampled on phase 1 of clock cycle 1 and must be high if no wait states are desired. Input data from the memory is sampled on phase 1 of clock cycle 2.

Table 2-10. TMS 9900 Pin Assignments and Functions

Signature	Pin	I/O	Description
			Address Bus
A0(MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vector to the external memory system when MEMEN- is active and I/O-bit addresses and external-instruction addresses to the I/O system when MEMEN- is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A1	23	OUT	
A2	22	OUT	
A3	21	OUT	
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14(LSB)	10	OUT	
			Data Bus
D0(MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when MEMEN- is active. The data bus assumes the high-impedance state when HOLDA is active.
D1	42	I/O	
D2	43	I/O	
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15(LSB)	56	I/O	
			Power Supplies
V_{SS}	26, 40		Ground reference
V_{BB}	1		Supply voltage (– 5 V NOM)
V_{CC}	2, 59		Supply voltage (5 V NOM)
V_{DD}	27		Supply voltage (12 V NOM)
			Clocks
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

Table 2-10. TMS 9900 Pin Assignments and Functions (Continued)

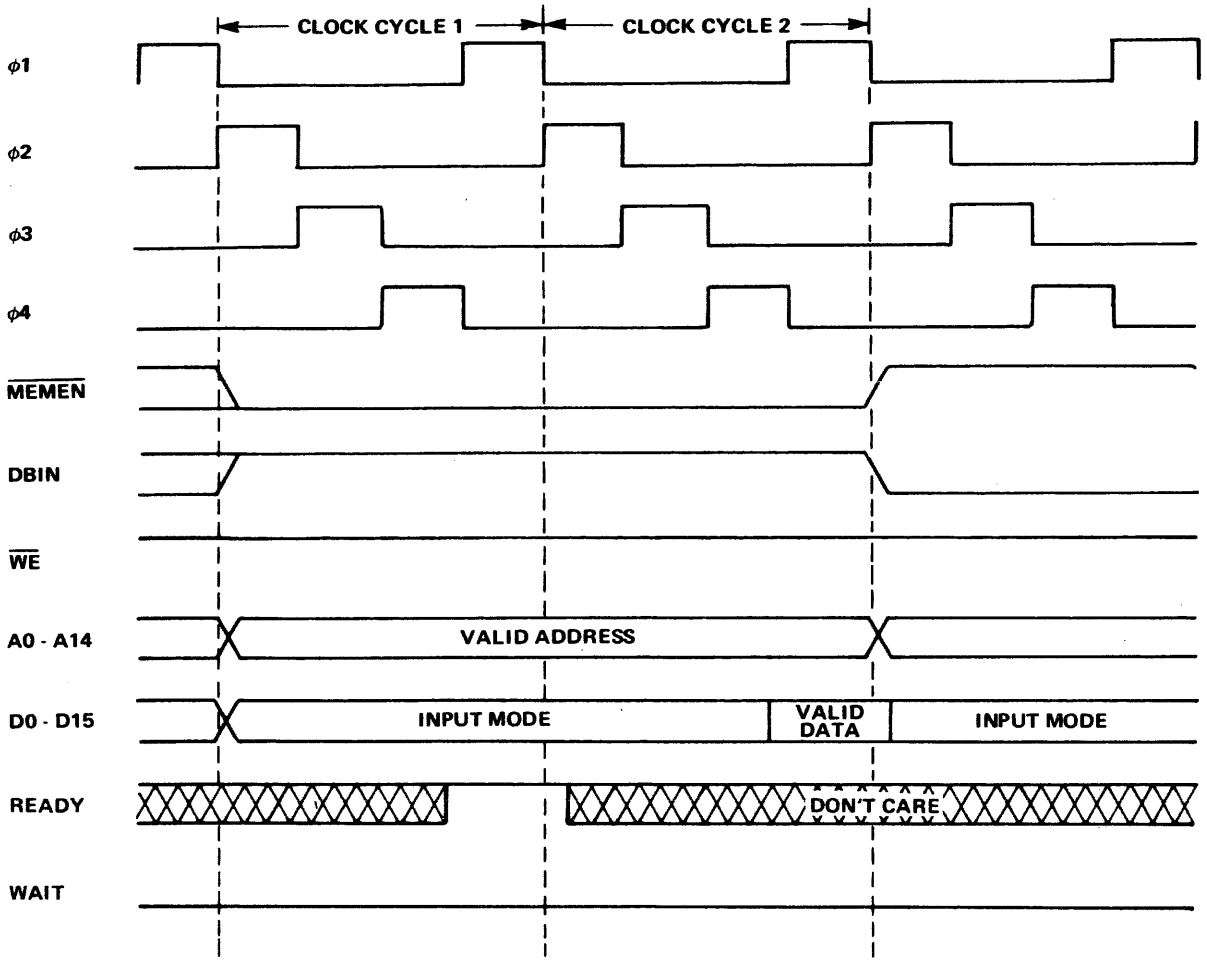
Signature	Pin	I/O	Description
			Bus Control
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the TMS 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN-. DBIN remains low in all other cases except when HOLDA is active.
MEMEN-	63	OUT	Memory enable. When active (low). MEMEN- indicates that the address bus contains a memory address.
WE-	61	OUT	Write enable. When active (low), WE- indicates that memory-write data is available from the TMS 9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			Interrupt Control
INTREQ-	32	IN	Interrupt request. When active (low), INTREQ- indicates that an external interrupt is requested. If INTREQ- is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal to or less than status register bits 12 through 15), the TMS 9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTREQ- should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the requested interrupt.
IC0(MSB) IC1 IC2 IC3(LSB)	36 35 34 33	IN IN IN IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when INTREQ- is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.

Table 2-10. TMS 9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			Memory Control
HOLD-	64	IN	Hold. When active (low), HOLD- indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle or CRU output. The processor then places the address and data buses in the high-impedance state (along with WE-, MEMEN-, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When HOLD- is removed, the processor returns to normal operation. This pin is tied to *VCC* on the TFDC.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs (WE-, MEMEN-, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory. This pin is not used on the TFDC.
			Timing and Control
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the TMS 9900 is acquiring an instruction. IAQ can be used to detect illegal op codes. This pin is not used on the TFDC.
LOAD-	4	IN	Load. When active (low), LOAD- causes the TMS 9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. LOAD- will also terminate an idle state. If LOAD- is active during the time RESET- is released, then the LOAD- trap will occur after the RESET- function is completed. LOAD- should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations. This pin is tied to *VCC* on the TFDC.

Table 2-10. TMS 9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
RESET-	6	IN	Reset. When active (low), RESET- causes the processor to be reset and inhibits WE- and CRUCLK. When RESET- is released, the TMS 9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. RESET- will also terminate an idle state. RESET- must be held active for a minimum of three clock cycles.



2277419

Figure 2-33. TMS 9900 Memory Read Timing

At the end of the read cycle, MEMEN- and DBIN go inactive (high and low, respectively). The address bus may also change at this time. A memory read cycle is never followed immediately by a memory write cycle. Thus, the microprocessor data output drivers, D0–D15, remain disabled for at least one additional clock cycle.

Figure 2-34 shows a memory read cycle with one wait state. For this case, READY is low when sampled at clock cycle 1, phase 1. The WAIT output goes high, and all other operations are suspended until a high READY signal is sensed on a subsequent phase 1. Thus, operations may be suspended for an integral number of clock cycles while waiting for a slow memory or a slow memory-mapped input process.

Memory Write Timing. A write cycle with no wait states is shown in Figure 2-35. MEMEN–, the address output, and the data output go active at the beginning of the operation (phase 2 of clock cycle 1). DBIN (data bus in) remains inactive for the entire machine cycle. Write enable (WE–) goes active on phase 1 of clock cycle 1. The delay before activating WE- allows the memory time to decode the address and meet input data setup time requirements. The READY signal is also sampled on phase 1 of clock cycle 1. An inactive READY signal does not prevent the generation of WE–. WE- goes inactive on phase 1 of clock cycle 2, and the address and data lines may change states on the next phase 2 pulse. This makes sure that the data is properly clocked into memory before the address and data lines change.

Figure 2-36 shows a write cycle with one wait state. READY is inactive (low) when sampled at phase 1. All microprocessor outputs, including the active WE- signal, are held constant until an active READY is sensed on a subsequent phase 1. This allows operations to be slowed by an integral number of clock cycles to accommodate a slow memory or memory-mapped output device.

CRU Operation. Interface timing for the CRU bus is shown in Figure 2-37 and Figure 2-38. During a CRU-bit output operation, the CRU-bit address is placed on the address bus A0 through A14 and the actual bit data on the CRUOUT line. MEMEN- and DBIN remain low for the duration of the operation. During the second clock cycle, a CRU clock pulse (CRUCLK) loads the CRUOUT signal into the destination device. This process is repeated until the number of bits specified by the instruction have been transferred. During a CRU input operation, the microprocessor supplies an address on A0–A14. Decoders in the external CRU devices gate the selected bit onto the CRUIN line. The data bit is clocked into the microprocessor on phase 1 of clock cycle 2.

2.6.3 Processor Timing and Reset

The TMS 9900 microprocessor requires clock inputs consisting of four nonoverlapping phases. Although all other TMS 9900 input/output signals are TTL-compatible, the clock inputs must be 12-volt MOS (metal-oxide semiconductor) levels. These levels are;

Logic 0 = 0.0 to +0.25 V typical

Logic 1 = +10.0 to +12.6 V typical

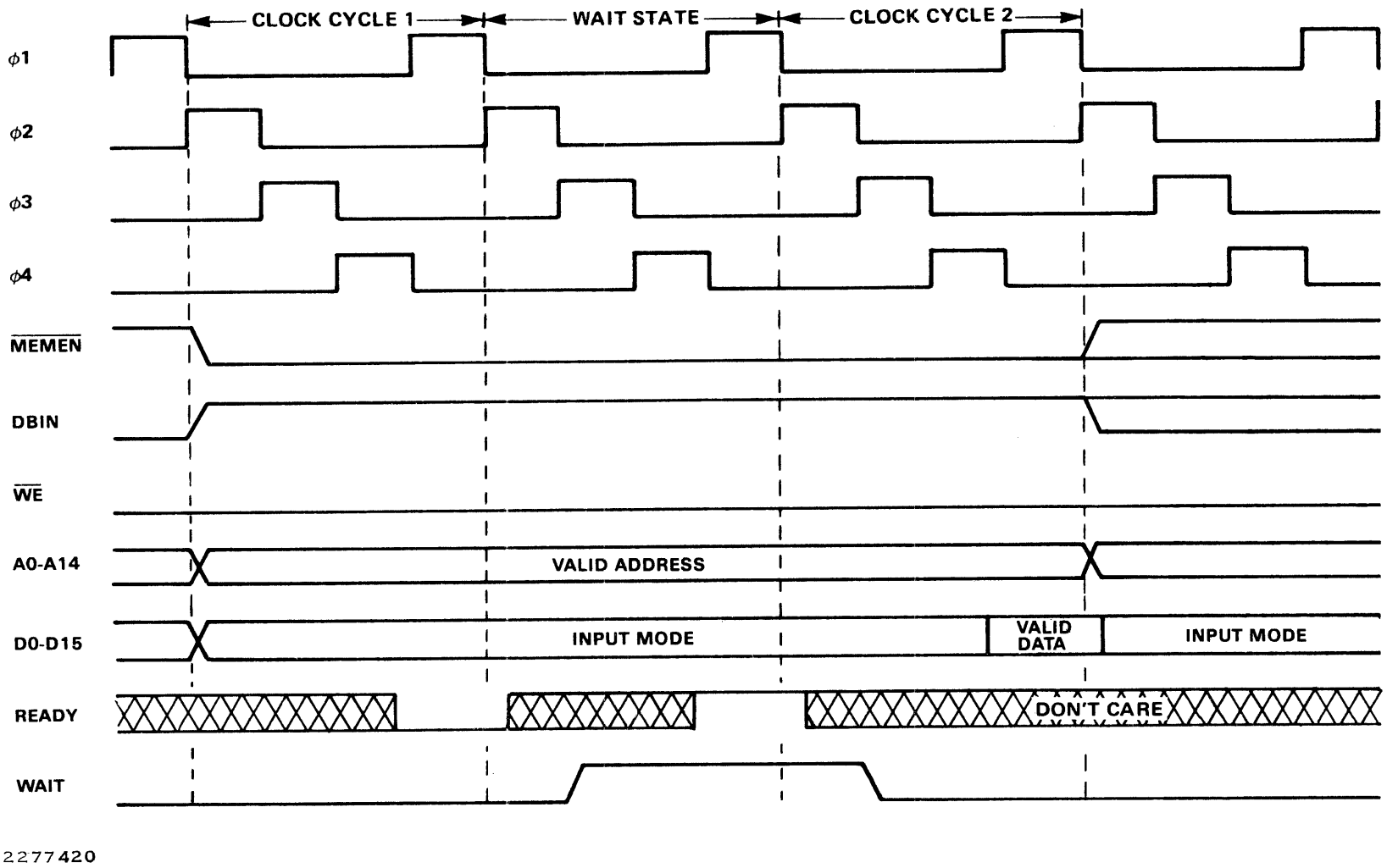


Figure 2-34. TMS 9900 Memory Read Cycle Timing with One Wait State

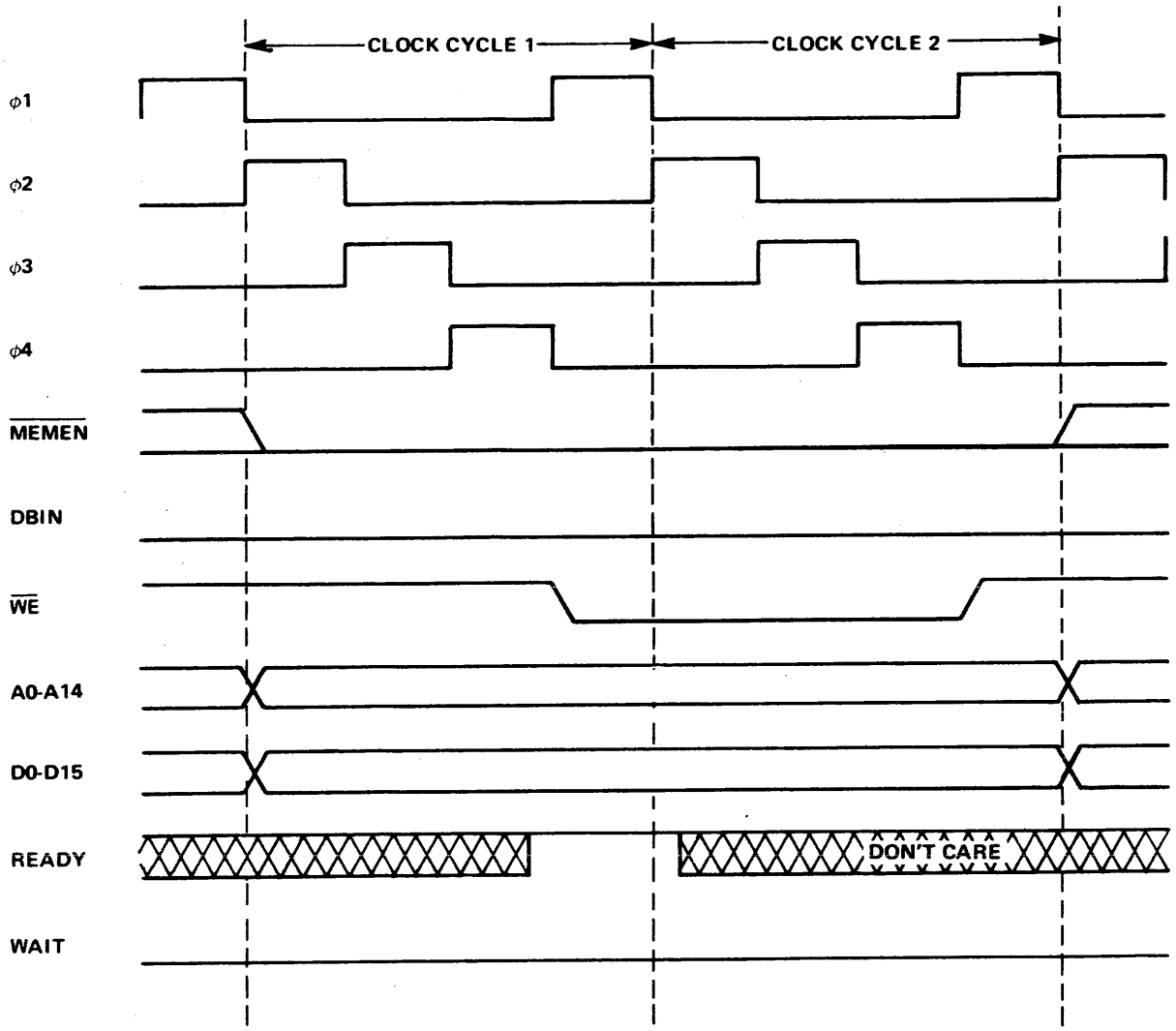


Figure 2-35. TMS 9900 Memory Write Cycle Timing

Microprocessor timing is provided by a TIM 9904/SN74LS362 four-phase clock generator. The reset description is included with the timing description because a spare Schmitt trigger and flip-flop in the TIM 9904/SN74LS362 device are used in the development of the microprocessor reset signal. The reset and microprocessor clock logic is shown in Figure 2-39.

2.6.3.1 TIM 9904/SN74LS362 Four-Phase Clock Generator. The internal block diagram of the clock generator is shown within the dotted outline of the TIM 9904/SN74LS362 device. When the external oscillator input, OSCIN, is held high, the internal oscillator operates at a clock frequency determined by the external components at the XTAL1,2 and TK1,2 inputs. As used in the TFDC, a 48-MHz third-overtone crystal and a tuned 48-MHz tank circuit are used as the frequency control elements. The oscillator operating frequency must be 16 times the desired clock phase frequency. The oscillator output is shaped to a square wave for input to the divider circuits.

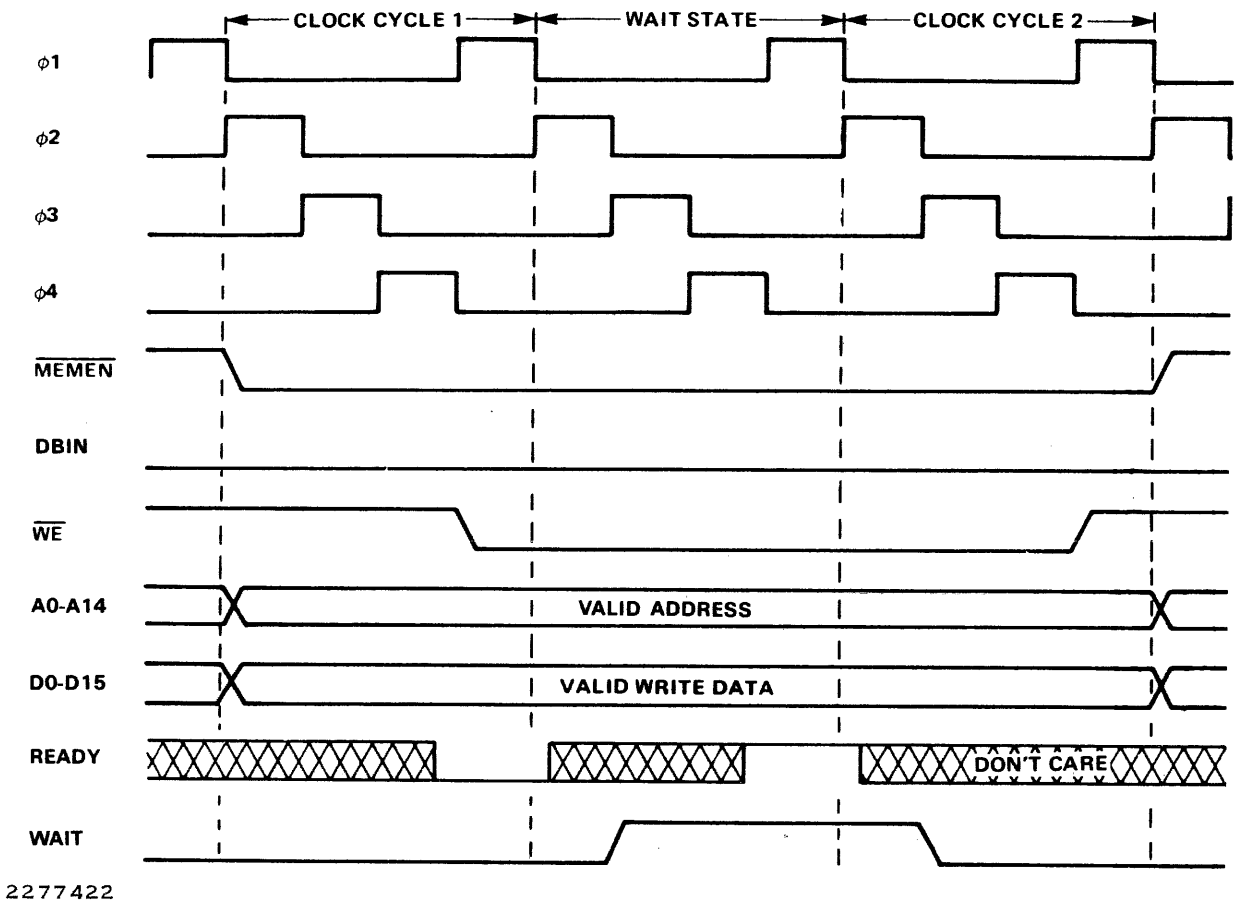


Figure 2-36. TMS 9900 Memory Write Cycle Timing with One Wait State

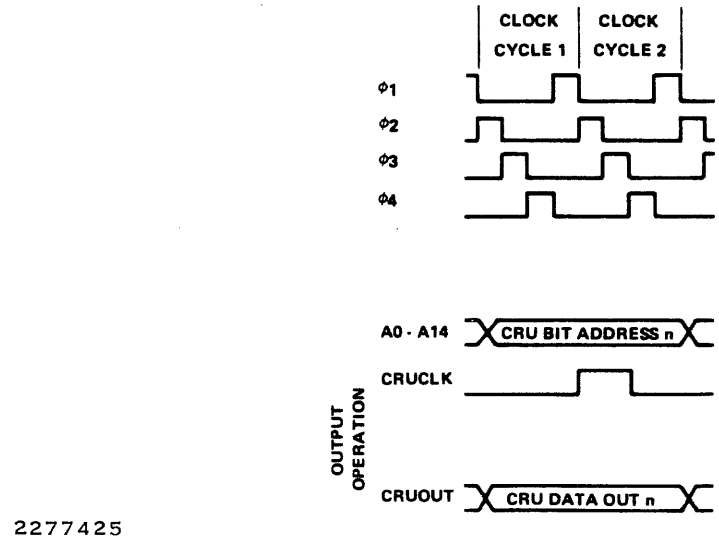


Figure 2-37. CRU Output Machine Cycle Timing

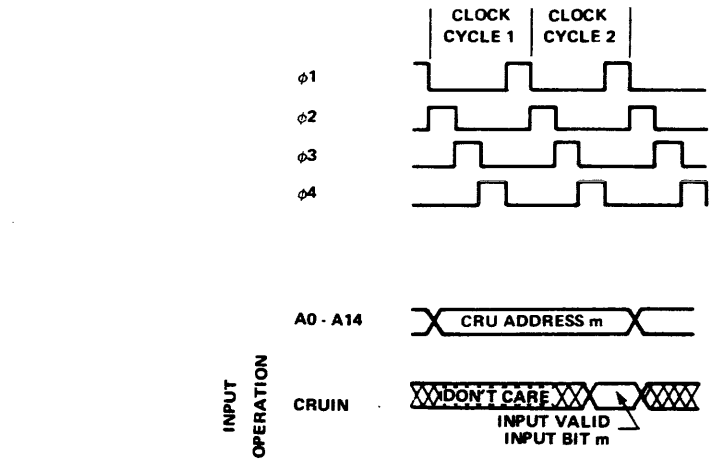


Figure 2-38. CRU Input Machine Cycle Timing

Timing waveforms for the TIM 9904/SN74LS362 outputs are given in Figure 2-40, which should be used to supplement the block diagram. The output of the first divide-by-four network is an asymmetric waveform with a frequency of 12 MHz. The period of the waveform is 83.333 nanoseconds, and the pulse width is 20.833 nanoseconds (one period of OSCIN).

A driver provides the divide-by-four output (OSCOUT) to the TFDC. The 12-MHz OSCOUT signal is divided to 6 MHz and 500 kHz in the read data simulator logic. The 6-MHz signal is used as a simulated read clock. It is also routed to the phase-lock loop (PLL) clock circuits, where it serves as a crystal-controlled write clock signal. The 500-kHz signal is used in the remote drive interface as a timing reference for control and status signal multiplexing/demultiplexing.

The phase generator circuit produces four individual, nonoverlapping phases, which are routed to the TMS 9900 by MOS drivers. Notice on the timing chart that a phase pulse is always enabled on the trailing edge of OSCOUT and is disabled on the next leading edge of OSCOUT. This assures that there is always one pulse width of the OSCOUT waveform (20.833 nanoseconds) between successive phases. This scheme completely prevents phase overlap and reduces the output pulse width to 62.5 nanoseconds (83.333–20.833).

The four output clock phases are routed to the TMS 9900 microprocessor via 15-ohm isolation resistors, which minimize clock overshoot and undershoot. The four individual phases are used within the microprocessor to control individual events in an instruction execution sequence. Timing examples are provided in the CRU and memory descriptions.

CAUTION

The four-phase timing signals provided by the MOS drivers are not short-circuit protected. Any probing into this circuitry must be done with caution to avoid irreversible damage to the TIM 9904/SN74LS362 clock generator device.

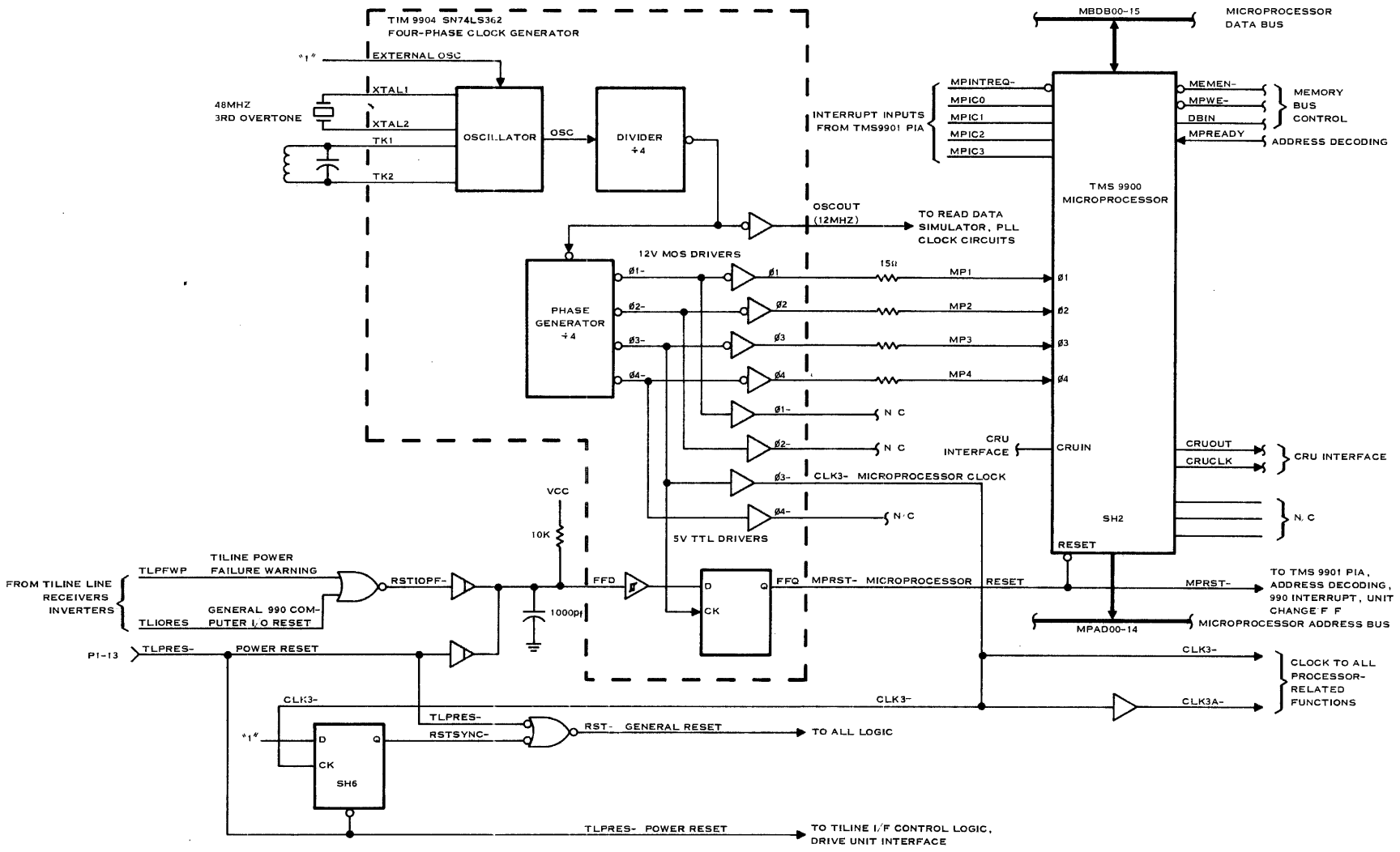


Figure 2-39 Microprocessor Clock and Reset Logic

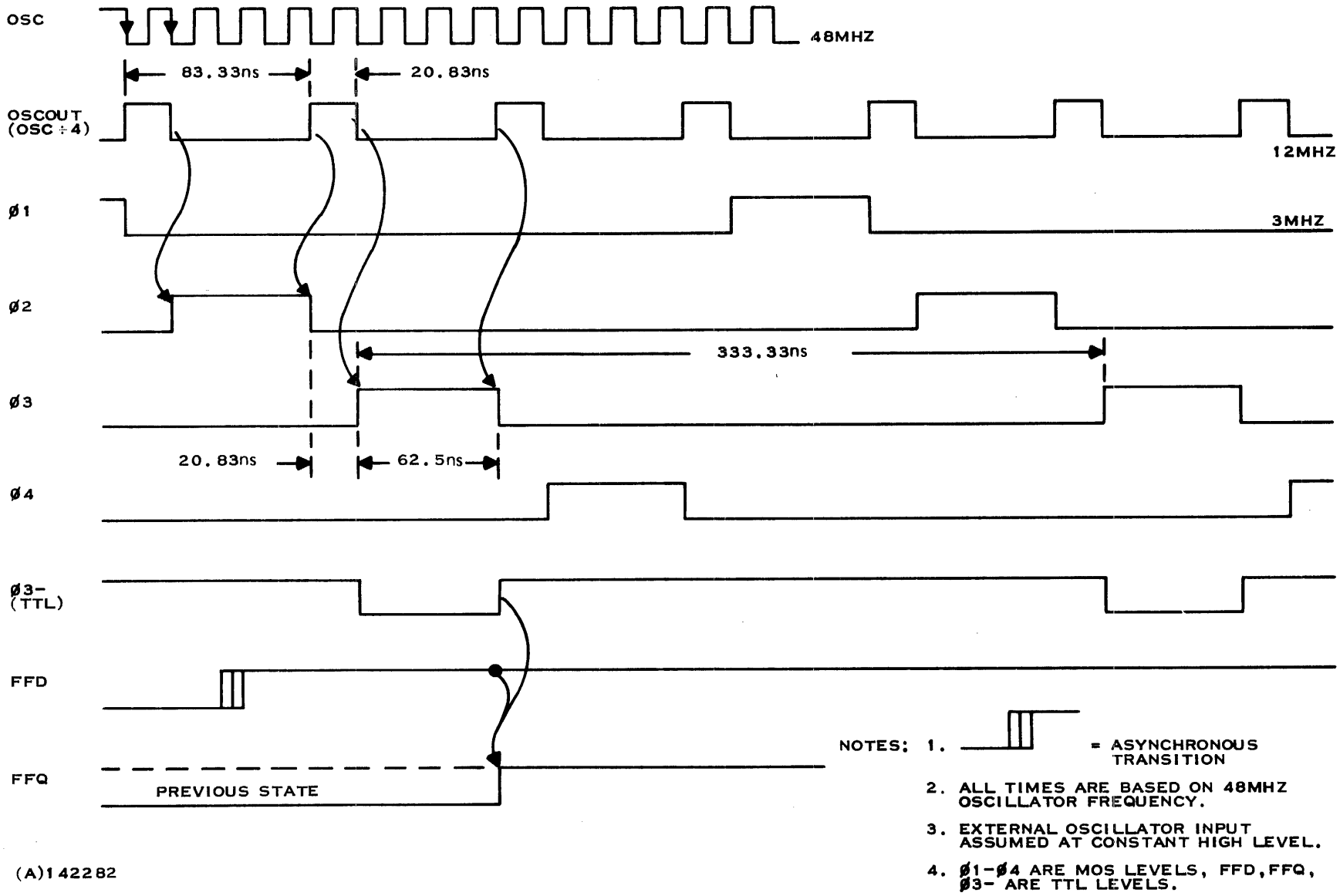


Figure 2-40. TIM 9904/SN74LS362 Clock Generator Timing

The four clock phases, in active low form, are also supplied by TTL-compatible output drivers. The TTL outputs are provided for synchronization of external logic functions to the TMS 9900 operating cycle. The TFDC requires phase 3 to synchronize TMS 9900 I/O functions. The active low phase 3 microprocessor clock signal, CLK3-, is the basic timing reference for all processor-related functions in the TFDC.

CLK3- is one of the two major timing signals used throughout the TFDC. The TILINE slave logic and master access logic are asynchronous, but the ROM-based TILINE I/F control logic is synchronized to CLK3-. Basic timing for the drive interface logic is PLLCLK-, which is phase-locked to incoming data for read operations and derived from OSCOUT for write operations.

2.6.3.2 Reset Logic. Three signals from the 990 backplane which can cause a TFDC reset. These signals are shown in Table 2-11.

Table 2-11. TFDC Reset Signals

Signature	Description
TLIORES-	TILINE I/O reset. A 100- to 500-nanosecond active low pulse that resets all I/O controllers in the 990 chassis. This signal is generated by the 990 processor as the result of the Programmer Panel RESET being depressed or the Reset (RSET) instruction being executed.
TLPFWP-	TILINE power failure warning pulse. An active low pulse that precedes a power loss. The power failure warning pulse is generated by the 990 chassis power supply. The leading edge of TLPFWP- precedes the power loss by at least 7 milliseconds in the 6-slot or 13-slot chassis, and 2 milliseconds in the 17-slot chassis.
TLPRES-	TILINE power reset. A normally high signal that goes low to reset all I/O controllers and force critical external device control lines to safe states. TLPRES- goes low at least 10 microseconds before power loss. It then remains low during power recovery until dc voltages are available and stable. TLPRES- is generated by the 990 chassis power supply.

Refer to the microprocessor clock and reset block diagram. The TLPFWP- and TLIORES- signals are inverted to active-high form by the TILINE line receivers. TLPRES- enters the reset logic directly, with no inversion.

Either an I/O reset or a power failure warning will force RSTIOPF- (reset I/O or power failure) low at the input of an SN7407 open-collector driver. The driver output is wire-ANDed with a TLPRES- driver. The RC network at the driver output serves as a pulse stretcher to satisfy the TMS 9900 minimum reset pulse width. The TMS 9900 requires a reset pulse of at least three clock cycles (approximately 1 microsecond at 3 MHz). The component values shown stretch the microprocessor reset pulse to approximately 3 microseconds.

The output of the RC network is wired to a Schmitt-trigger gate and flip-flop in the TIM 9904/SN74LS362 clock generator. This Schmitt trigger and flip-flop combination is specifically designed for resetting the TMS 9900 microprocessor. The flip-flop is clocked on the trailing edge of the phase 3 clock. The flip-flop output, MPRST-, is wired to the reset inputs of the TMS 9900 microprocessor, the TMS 9901 PIA, and to related logic such as the address decoders, 990 interrupt logic, and unit change flip-flop.

In the absence of a reset input, the capacitor is maintained at a logic 1, approximately 5 volts. A reset signal causes one of the output drivers to rapidly drain charge from the capacitor through the open-collector output transistors, dropping to logic 0. The flip-flop in the clock generator, FFQ, resets on the trailing edge of the next phase 3 clock, activating the microprocessor reset, MPRST-.

The RC-network output remains low for the input pulse duration, and then starts rising at a rate limited by the capacitor charging rate through the 10K resistor. When the voltage reaches the threshold level of the Schmitt trigger gate, the flip-flop input goes to one. The microprocessor reset returns high on the trailing edge of the next phase 3 clock. The Schmitt trigger provides reliable sensing of the input threshold without introducing output noise or jitter.

A microprocessor reset is a level 0 nonmaskable interrupt to the TMS 9900 device. MPRST- resets the microprocessor and inhibits the write enable (MPWE-) and CRU clock (CRUCLK) outputs. Releasing MPRST- forces a vectored interrupt at memory location 0000. The workspace pointer and program count for the reset interrupt service routine (PWRENT) are stored at locations 0000 and 0002 in the control program ROM. This is a recovery routine which cleans up the loose ends of any aborted operation, updates the controller status word, reloads default parameters in the RAM, executes TFDC self-test, and returns to idle.

In addition to causing a microprocessor reset, the TILINE power reset (TLPRES-) resets the TILINE I/F control logic and the drive unit interface logic. (TLPRES-) also enables a general reset (RST-) to the TFDC logic. The trailing edge of RST3- is synchronized to the trailing edge of the microprocessor clock (CLK3-) by the RSTSYNC- flip-flop.

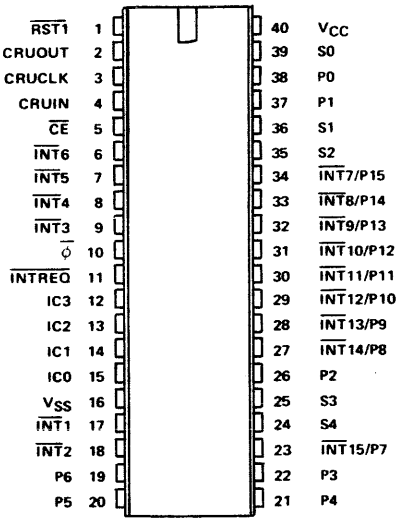
2.6.4 TMS 9901 Peripheral Interface Adapter (PIA)

The TMS 9901 peripheral interface adapter is a multifunction integrated circuit which provides interrupt handling, CRU input/output port expansion, and interval timer capabilities to the TMS 9900 microprocessor. Table 2-12 shows the TMS 9901 device pin assignments, and Figure 2-41 is a basic functional block diagram of the PIA. Some documents refer to the TMS 9901 as a programmable systems interface (PSI). The logic drawings for the TILINE flexible disk controller use the term PIA, as does this description.

The PIA has six dedicated interrupt input lines and an additional nine lines that may be programmed to operate as interrupt inputs or CRU ports. The PIA monitors the interrupt inputs and checks the active interrupts against an interrupt mask to determine if they are enabled. Priority logic selects the highest priority active interrupt, encodes the interrupt, and issues an active low interrupt request. The interrupt request and interrupt code outputs match the TMS 9900 interrupt input requirements.

Table 2-12. TMS 9901 Pin Assignments and Functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INTREQ}$	11	OUT	INTERRUPT Request. When active (low) $\overline{INTREQ}$ indicates that an enabled interrupt has been received. $\overline{INTREQ}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0–IC3 = (1,1,1,1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{CE}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{CE}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RST1}$	1	IN	Power Up Reset. When active (low) $\overline{RST1}$ resets all interrupt masks to "0", resets IC0 – IC3 = (0, 0, 0, 0), $\overline{INTREQ}$ = 1 disables the clock, and programs all I/O ports to inputs. $\overline{RST1}$ has a Schmitt-triger input to allow implementation with an RC circuit as shown in Figure 7.
V_{CC}	40		Supply Voltage. +5 V nominal.
V_{SS}	16		Ground Reference
$\bar{\phi}$	10	IN	System clock ($\bar{\phi}3$ in TMS 9900 system, $\overline{CKOUT}$ in TMS 9980 system).
$\overline{INT1}$	17	IN	Group 1, interrupt inputs. When active (Low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	18	IN	
$\overline{INT3}$	9	IN	
$\overline{INT4}$	8	IN	
$\overline{INT5}$	7	IN	
$\overline{INT6}$	6	IN	
$\overline{INT7}$/ P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{INT8}$/ P14	33	I/O	
$\overline{INT9}$/ P13	32	I/O	
$\overline{INT10}$/P12	31	I/O	
$\overline{INT11}$/P11	30	I/O	
$\overline{INT12}$/P10	29	I/O	
$\overline{INT13}$/P9	28	I/O	
$\overline{INT14}$/P8	27	I/O	
$\overline{INT15}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	



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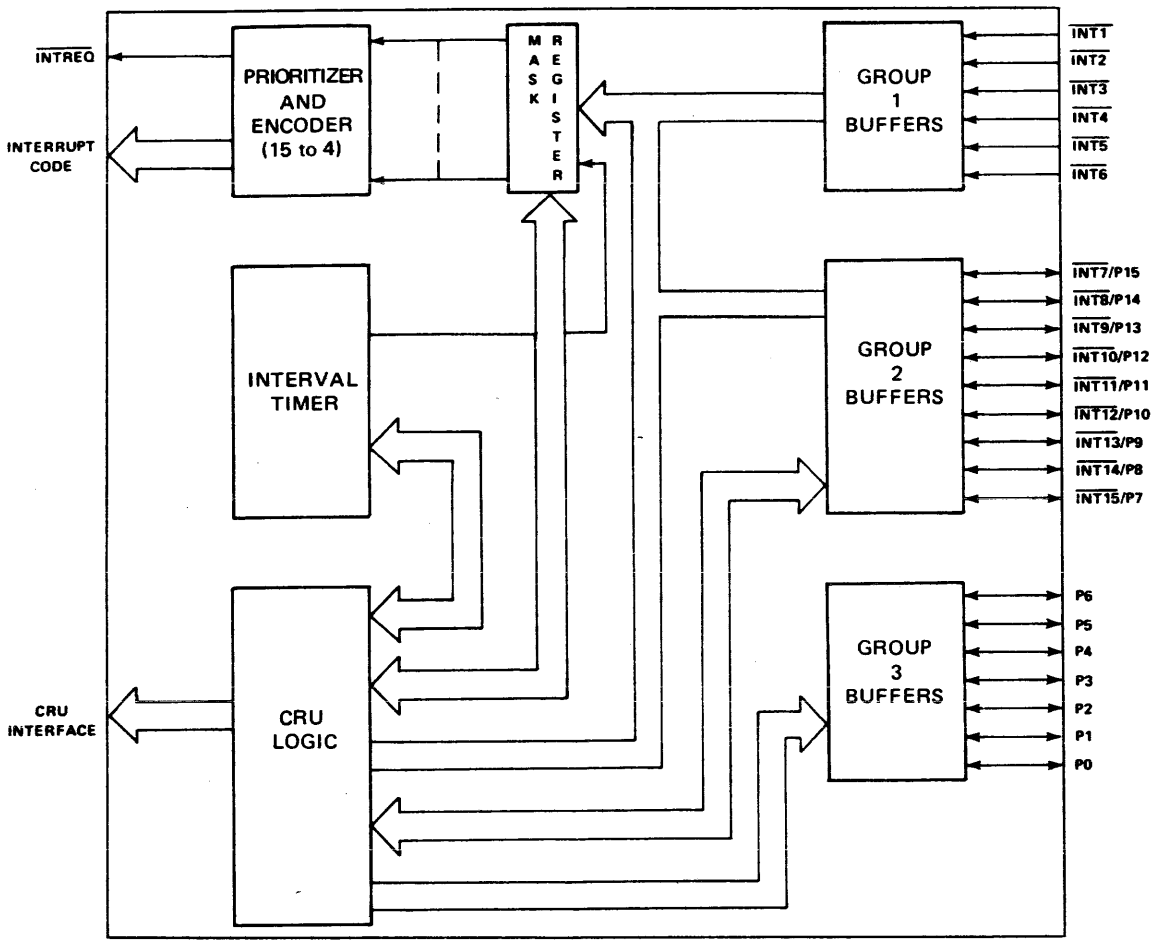

Figure 2-41. TMS 9901 PIA Block Diagram

The PIA contains seven dedicated CRU ports. The TMS 9900 may write to a port or read from a port by executing a CRU instruction such as SBO (Set Bit to One), SBZ (Set Bit to Zero), LDCR (Load CRU), STCR (Store CRU), or TB (Test Bit). Any 9900 CRU instruction uses a CRU base address in workspace register 12 (bits 03-14) to develop an output address (0 to 4096) on the memory address bus. This address specifies the CRU bit to be read or written. For read operations, the PIA responds by placing the bit on the CRUIN line. For write operations, the TMS 9900 places the bit on the CRUOUT line and strobes it into the PIA with a clock pulse, CRUCLK. During multibit transfers, the TMS 9900 increments the output address after each bit transfer.

Nine of the PIA I/O lines are individually programmable to function either as active low interrupt inputs (INT7- through INT15-) or as CRU input/output ports. This programming must be performed by the TMS 9900 after any power-up or microprocessor reset.

The CRU is used to program the PIA internal logic and to check PIA internal status. For example, the interrupt mask bits are assigned CRU bit positions. Interrupt mask bits are set via the CRU, and the interrupt mask may be read in the same manner.

The PIA is clocked by inverted phase 3 (CLK3-) of the TMS 9900 four-phase clock. An interval timer in the PIA counts pulses until a specified number is decremented to zero, generates a level 3 interrupt, and reloads the initial number. The initial number that sets the interval is loaded into the PIA over the CRU.

2.6.4.1 Microprocessor/PIA CRU Communication. The TMS 9901 occupies 32 bits in CRU read space and 32 bits in CRU write space, as shown in Table 2-13. Many of these are multiple-use bits, with functions determined by current PIA operating mode.

The TMS 9901 CRU interface consists of five address select lines, S0-S4, and the three CRU lines, CRUIN, CRUOUT, and CRUCLK. Select lines S0-S4 are connected to the five least significant bits of the microprocessor address bus, MPAD10-14, respectively. The chip enable (CE-) signal is decoded from microprocessor address bits MPAD01, MPAD08, and MPAD09 during a CRU cycle.

There are a maximum of 4096 possible CRU addresses in a TMS 9900 microprocessor system. The CRU and the memory system share the microprocessor address bus. A CRU operation is specified if the three MSB address bits (MPAD00-02) are zeros and the memory enable output of the TMS 9900 is inactive (MEMEN- high). The other memory control lines, DBIN and WE-, are also inactive for CRU operations.

2.6.4.2 Interrupt Operations. The PIA has six dedicated interrupt lines and nine more multifunction lines which may serve as interrupts or CRU ports. All of these lines are latched into a synchronizing register on the leading (falling) edge of the active low phase 3 clock input, CLK3-. The latch outputs are inverted and ANDed with the corresponding outputs of a mask register. On the trailing edge of CLK3-, the priority and encoding logic starts the process of detecting and encoding the highest priority active interrupt. The microprocessor interrupt request (MPINTREQ-) and the four-bit interrupt code are latched into an output register on the leading edge of the next CLK3- pulse.

Once an interrupt input goes low, it must remain low until the interrupt condition is serviced and cleared by the 9900 control program. The TMS 9900 clears an interrupt by a CRU write to a command bit dedicated to that interrupt. The exception is level 0, which clears itself after the specified delay.

The interrupt mask bits may be individually set (interrupt enabled) or reset (interrupt disabled) by CRU write operations to the mask bits. Any of the multipurpose lines which are used as data ports rather than as interrupt inputs must be masked off to prevent false interrupts. Also, any interrupt lines which are unused (including multipurpose lines) should be masked off to prevent noise-induced interrupts.

CRU bits 1-15 are shared between the interrupt logic and the interval timer logic. The operating mode of the PIA determines the function of these bits. To write to the interrupt mask, the PIA must be in interrupt mode (bit 00 = 0). The operating mode may be determined by a CRU read to bit 00. It may be changed by a write to bit 00. The mask may be loaded by a single TMS 9900 instruction (LDCR) or by individual SBO and SBZ instructions.

2.6.4.3 Data Ports. The TMS 9901 includes seven dedicated data ports and nine multipurpose ports that may be individually selected to serve as interrupt inputs or data ports. The interrupt mask bits must be reset for all multipurpose lines that are used as data ports. Otherwise, the data will generate false interrupts.

Table 2-13. Select Bit Assignments for 9901 PIA

Select Bit	S0	S1	S2	S3	S4	CRU Read Data	CRU Write Data
0	0	0	0	0	0	PIA mode[1]	Set PIA mode
1	0	0	0	0	1	INT1-/CLK1[2]	MASK1/CLK1[3]
2	0	0	0	1	0	INT2-/CLK2	MASK2/CLK2
3	0	0	0	1	1	INT3-/CLK3	MASK3/CLK3
4	0	0	1	0	0	INT4-/CLK4	MASK4/CLK4
5	0	0	1	0	1	INT5-/CLK5	MASK5/CLK5
6	0	0	1	1	0	INT6-/CLK6	MASK6/CLK6
7	0	0	1	1	1	INT7-/CLK7	MASK7/CLK7
8	0	1	0	0	0	INT8-/CLK8	MASK8/CLK8
9	0	1	0	0	1	INT9-/CLK9	MASK9/CLK9
10	0	1	0	1	0	INT10-/CLK10	MASK10/CLK10
11	0	1	0	1	1	INT11-/CLK11	MASK11/CLK11
12	0	1	1	0	0	INT12-/CLK12	MASK12/CLK12
13	0	1	1	0	1	INT13-/CLK13	MASK13/CLK13
14	0	1	1	1	0	INT14-/CLK14	MASK14/CLK14
15	0	1	1	1	1	INT15-/INTREQ[7]	MASK15/RST2-[4]
16	1	0	0	0	0	P0 Input	P0 Output[5,6]
17	1	0	0	0	1	P1 Input	P1 Output
18	1	0	0	1	0	P2 Input	P2 Output
19	1	0	0	1	1	P3 Input	P3 Output
20	1	0	1	0	0	P4 Input	P4 Output
21	1	0	1	0	1	P5 Input	P5 Output
22	1	0	1	1	0	P6 Input	P6 Output
23	1	0	1	1	1	P7 Input	P7 Output
24	1	1	0	0	0	P8 Input	P8 Output
25	1	1	0	0	1	P9 Input	P9 Output
26	1	1	0	1	0	P10 Input	P10 Output
27	1	1	0	1	1	P11 Input	P11 Output
28	1	1	1	0	0	P12 Input	P12 Output
29	1	1	1	0	1	P13 Input	P13 Output
30	1	1	1	1	0	P14 Input	P14 Output
31	1	1	1	1	1	P15 Input	P15 Output

Notes:

[1] 1 = interrupt mode
0 = clock mode

[2] Data present on INT- pin or clock value will be read regardless of mask value.

[3] Mask bit may be used to enable or disable the corresponding interrupt (interrupt mode only).

[4] Writing a zero to bit 15 (in clock mode) executes a software reset.

[5] Output data on a port may be read by the CRU.

[6] Writing data to the port programs the port for output.

[7] INTREQ is the inverted form of an interrupt request output.

A hardware reset (RST1-) forces all interrupt mask bits to zero and forces all data ports (dedicated or multipurpose) to input operation (high impedance). Therefore input operation is the default condition of these lines. The software reset (RST2-) is a CRU bit that forces all ports to input operation, but does not reset the interrupt mask.

To force a port to function as an output, the TMS 9900 must write an output data bit (one or zero) to that CRU address. The write operation programs that port to operate as an output until the next hardware or software reset. A read operation to an output port samples the present output (one or zero), but does not change the operation of the port. No external input signals may be connected to an output port.

2.6.4.4 Interval Timer Operation. The interval timer divides the input clock frequency by 64 and uses the low frequency clock to count down a 14-bit register. When the decrementer register contents reach zero, a level 3 interrupt is issued (if interrupt mask bit 3 is set), and the decrementer reloads and starts the count down cycle again.

The specified interval may be written into the clock register when the PIA is in the clock mode. This value is not destroyed because the interval timer uses separate clock and decrementer registers. For 3 MHz CLK3-, the clock register LSB represents a 21.3 microsecond interval, and the maximum interval is 349 milliseconds, plus or minus 21.3 microseconds. During programming, the decrementer restarts with an updated value after each interval bit is written. This allows a single CRU bit to restart the timer.

The interval timer may be disabled by writing a zero interval to the clock register. Clock interrupts are disabled by writing a zero to the level 3 interrupt mask bit.

The contents of the decrementer register are copied into a read register. The contents of the read register may be read back by placing the PIA in the clock mode and reading bits 1-15. The read register is not updated while in the clock mode, so the clock value read back represents the decremented count at the time of the mode change (to clock mode).

2.6.5 9900/9901 Interrupt and CRU Interface

The preceding paragraphs describe the TMS 9901 peripheral interface adapter as a device, without regard to the way the device is connected in the TFDC. The PIA, a dual decoder, two 8:1 multiplexers, and an 8-bit addressable latch serve the TMS 9900 interrupt input and CRU input/output requirements in the TFDC.

2.6.5.1 Interrupts. Refer to Figure 2-42, which is a detailed block diagram of the interrupt and CRU I/O logic. The nonmaskable RESET- input of the TMS 9900 is wired to the microprocessor reset (MPRST-) signal from the microprocessor clock and reset logic. All of the other TMS 9900 interrupts are supplied via the TMS 9901 PIA. The active-low interrupt inputs to the PIA are listed in Table 2-14.

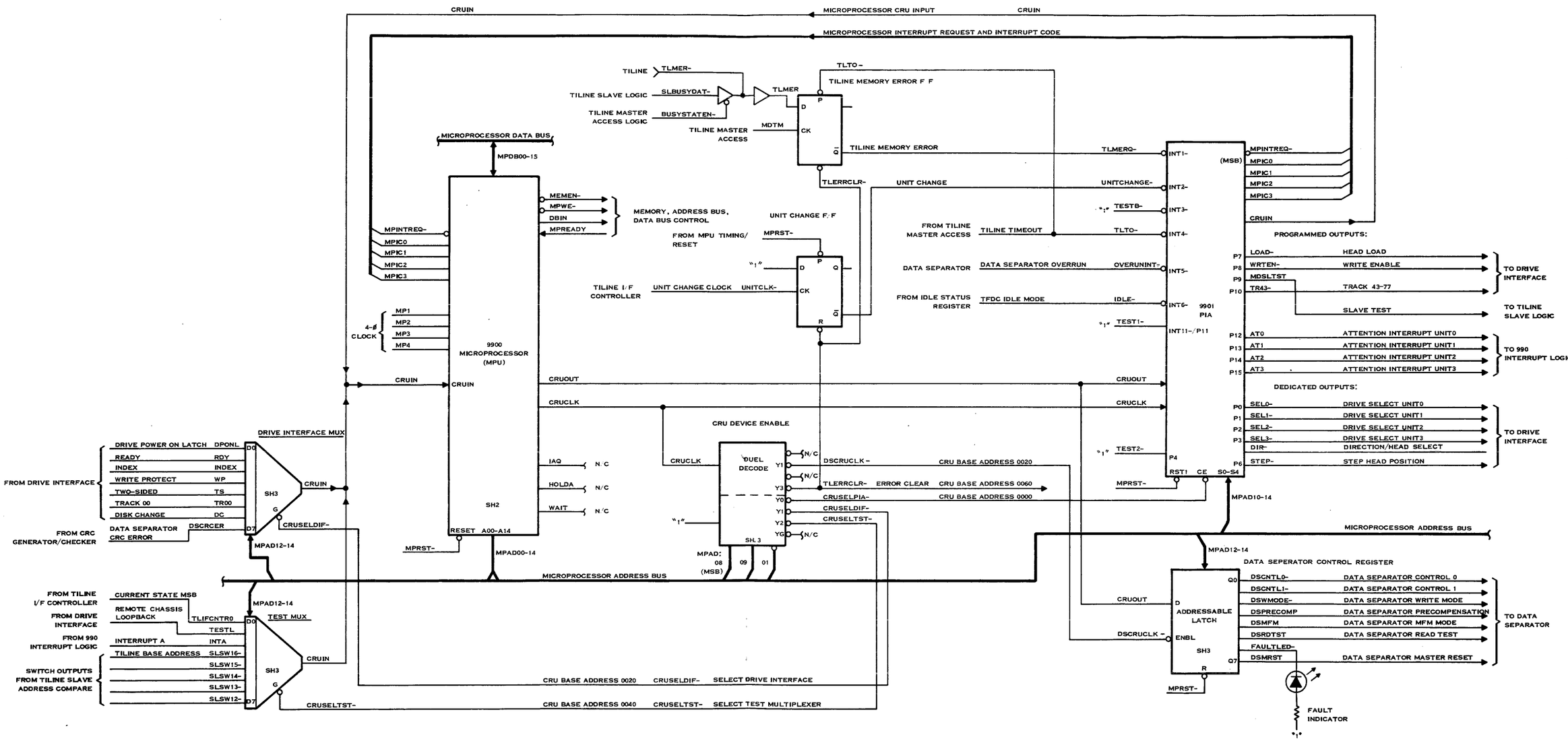

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Figure 2-42. TMS 9900 Microprocessor/TMS 9901 PIA Interrupts and CRU Input/Output

Table 2-14. PIA Interrupt Inputs

Level	Signature	Description
1	TLMERQ-	"TILINE memory error." A TILINE memory error signal is generated by an error-detecting memory if that memory detects a noncorrectable error on a TILINE read. TLMERQ- is cleared within the TFDC by TILINE error clear (TLERRCLR-).
2	UNITCHANGE-	Unit change. A change of drive selection (or any other external slave write to W6) or a microprocessor reset latches the UNITCHANGE- interrupt. A TILINE error clear, generated as a CRU output, is required to assure that the interrupt has been serviced.
3	TESTB- (clock)	External input is hardwired to logic 1. Level 3 clock interrupt is generated internally by PIA programmable interval timer logic on expiration of a specified interval. Clock interrupt may be cleared by microprocessor reset or by writing a zero to 9901 interrupt mask bit 3.
4	TLTO-	TILINE timeout. Timeout from TILINE master access logic that indicates that a slave unit addressed by the TFDC did not respond in the allotted time. Cleared by TLERRCLR-. To achieve a high interrupt priority, the TLTO- interrupt is hardwired to set TLMERQ-. CRU interrogation determines whether the interrupt was caused by a timeout or a memory error.
5	OVERUNINT-	Data separator overrun. Indicates that the TILINE has not transferred data fast enough to meet the data separator I/O transfer requirements (rate error). May occur when reading from the diskette if the TILINE cannot transfer word n before word n + 1 is ready at the data separator output. May occur when writing to the diskette if the TILINE does not supply word n + 1 fast enough for it to be properly recorded in relation to word n. Cleared by data separator master reset (after synchronization to PLLCLK).
6	IDLE	Idle/busy interrupt. IDLE goes low when a control word W7 with a 0 in the bit 0 position is received by the TFDC. This is a command to initiate controller operations, using the parameters previously supplied in control words W0 - W6. Cleared by microprocessor reset, MPRST-, or by loading a one in the idle status register via the register file bus. This is the lowest priority interrupt.

Refer to Figure 2-43, the timing diagram for a typical interrupt and interrupt clear cycle. The active low interrupt input to the 9901 is asynchronous to CLK3-, such as the TILINE timeout (TLTO-) interrupt. The leading edge of the first CLK3- pulse gates this interrupt (and any other active interrupts) into the PIA interrupt synchronization register. The trailing edge of CLK3- enables the priority encoding logic.

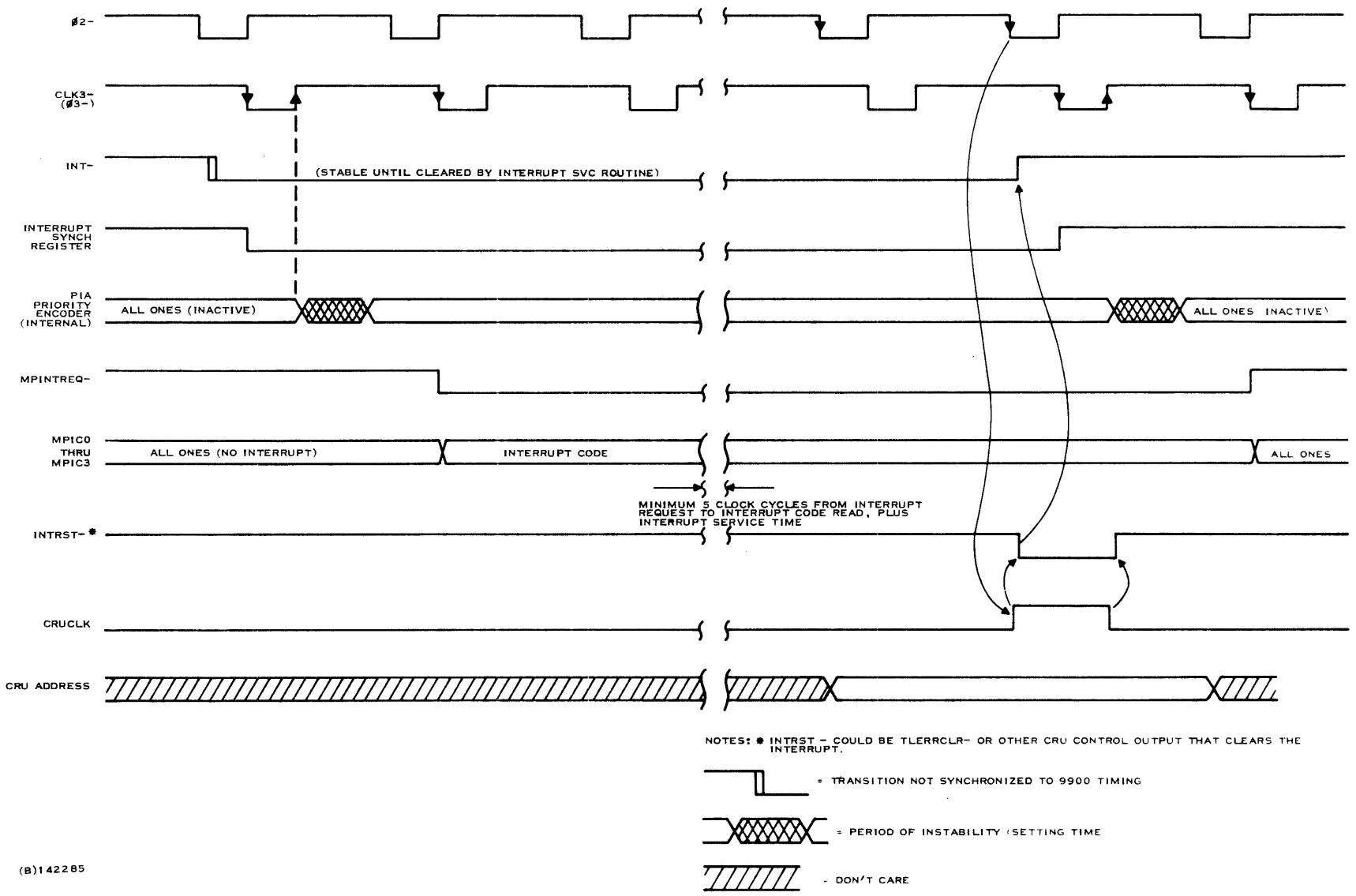


Figure 2-43. Typical Interrupt and Interrupt Clear Timing

Assume that the interrupt mask bit for this interrupt is set (interrupt enabled). Also assume that there are no other interrupts of higher priority which are both active and enabled by the mask register. The priority encoding logic must select the highest priority active interrupt and develop the 4-bit interrupt code and the interrupt request. This is a relatively slow operation, so a settling time is shown in the timing diagram. The settling time is internal to the PIA; no outputs change until the next CLK3- pulse.

On the leading edge of CLK3-, the PIA latches the interrupt request (MPINTREQ-) and the interrupt code (MPIC0-3) on the output lines to the TMS 9900 microprocessor. MPIC0 is the MSB of the interrupt code.

The MPU response time to an active interrupt request is determined by the operation in progress, and whether this interrupt level is currently enabled in the TMS 9900 status word. The minimum time between recognizing the active interrupt request and accepting the interrupt code is 3 clock cycles for RESET-, 5 clock cycles for other interrupts.

It is absolutely essential that the interrupt not disappear during the critical interval between recognizing the interrupt request and accepting the interrupt code. TFDC interrupts are latched to prevent this problem.

The break in the timing chart represents the time required by the TMS 9900 to accept the interrupt code and proceed through the interrupt service routine to the point of clearing the interrupt. Most of the interrupts, such as TILINE timeout, are cleared via a CRU operation.

CRU output address selection is synchronized to the leading edge of phase 2 microprocessor clock. The CRU clock pulse (CRUCLK-) has a leading edge synchronized to phase 2 and a trailing edge synchronized to the trailing edge of phase 3 (CLK3-). Phase 2 clock (inverted) is also shown on the timing diagram.

The CRU address associated with the interrupt clear (TLERRCLR-) appears on the microprocessor address bus at phase 2. The address steers the dual decoder to gate the CRUCLK input to the Y3 output (inverted form). When CRUCLK goes high, the active low decoder output (TLERRCLR-) unconditionally clears the interrupt. The CRU releases the address bus at the next phase 2.

The PIA operation for releasing the interrupt code and the interrupt request is synchronized to CLK3-. The timing diagram assumes that no other interrupt input is active, so MPINTREQ- returns high, and MPIC0-3 return to the all ones state.

2.6.5.2 CRU Operations. Listed below are the CRU input/output devices other than the TMS 9900 microprocessor:

- Drive interface multiplexer (input only)
- Test multiplexer (input only)
- 9901 PIA (input and output)
- Data separator control register (output only)

A CRU operation is addressed to a specific bit in the 4096-bit range allotted to the CRU. The address decoding in the TFDC is separated into device enable decoding (from the most significant bits) and individual bit addressing within the devices.

Refer to the detailed interrupt and CRU input/output block diagram, Figure 2-42. An SN74LS155 dual decoder, labeled "CRU device enable," decodes address bits MPAD01, MPAD08, and MPAD09. MPAD01, which must be zero for any CRU operation, serves as the decoder output strobe. A hardwired one into section 2 of the decoder generates the device enable signals as shown in Table 2-15.

Table 2-15. CRU Device Enable Decoder Outputs

MPAD08,09	Signature	Meaning
0 0	CRUSELPIA-	TMS 9901 PIA device select
0 1	CRUSELDIF-	Select disk interface
1 0	CRUSELTST-	Select test interface
0 1	*DSCRUCLK-	Active low enable to data separator control register.
1 1	*TLERRCLR-	Active low interrupt clear to TLTO, TLMER, UNITCHANGE flip-flops.

Note:

* Active low output that coincides with the CRU clock pulse.

The base address for the PIA is 0000, which enables CRUSELPIA-. The individual bits are addressed in terms of displacements from the base address, as shown in Table 2-16. This table is derived from the PIA select bit table in the PIA description.

Table 2-16. CRU Bit Assignments for 9901 PIA

Memory Bus Address*	MPAD (08,09 = 00) 10 11 12 13 14	CRU Read Data	CRU Write Data	9900 Program Mnemonic
0000	0 0 0 0 0	PIA mode[1]	Set PIA mode	PIA
0001	0 0 0 0 1	TLMERQ-/CLK1[2]	MASK1/CLK1[3]	TLMER[7],CLK1
0002	0 0 0 1 0	UNITCHANGE-/CLK2	MASK2/CLK2	UNITCH[7]
0003	0 0 0 1 1	CLKINT-/CLK3	MASK3/CLK3	CLKINT
0004	0 0 1 0 0	TLTO-/CLK4	MASK4/CLK4	TLTO[7]
0005	0 0 1 0 1	OVERUNINT-/CLK5	MASK5/CLK5	DSOVRN
0006	0 0 1 1 0	IDLE-/CLK6	MASK6/CLK6	IDLE

Table 2-16. CRU Bit Assignments for 9901 PIA (Continued)

Memory Bus Address*	MPAD (08,09 = 00) 10 11 12 13 14	CRU Read Data	CRU Write Data	9900 Program Mnemonic
0007	0 0 1 1 1	Spare/CLK7	MASK7/CLK7	-
0008	0 1 0 0 0	Spare/CLK8	MASK8/CLK8	-
0009	0 1 0 0 1	Spare/CLK9	MASK9/CLK9	-
000A	0 1 0 1 0	Spare/CLK10	MASK10/CLK10	-
000B	0 1 0 1 1	TEST1-/CLK11	MASK11/CLK11	-
000C	0 1 1 0 0	Spare/CLK12	MASK12/CLK12	CLKC
000D	0 1 1 0 1	Spare/CLK13	MASK13/CLK13	-
000E	0 1 1 1 0	Spare/CLK14	MASK14/CLK14	CLKF
000F	0 1 1 1 1	Spare/INTREQ[4]	MASK15/RST2-	PIARST
0010	1 0 0 0 0	Spare[5]	SEL0-	SEL0
0011	1 0 0 0 1	Spare	SEL1-	SEL1
0012	1 0 0 1 0	Spare	SEL2-	SEL2
0013	1 0 0 1 1	Spare	SEL3-	SEL3
0014	1 0 1 0 0	Spare	Spare	-
0015	1 0 1 0 1	Spare	DIR-	DIR
0016	1 0 1 1 0	Spare	STEP-	STEP
0017	1 0 1 1 1	Spare	LOAD-	LOAD
0018	1 1 0 0 0	Spare	WRTEN-	WRTEN
0019	1 1 0 0 1	Spare	MDSLTST[6]	MDSLTS
001A	1 1 0 1 0	Spare	TR43-	TR43
001B	1 1 0 1 1	TEST1-	Spare	-
001C	1 1 1 0 0	Spare	AT0	AT0
001D	1 1 1 0 1	Spare	AT1	AT1
001E	1 1 1 1 0	Spare	AT2	AT2
001F	1 1 1 1 1	Spare	AT3	AT3

Notes:

* Memory bus address is derived within the TMS 9900 as the sum of a CRU base address in workspace register 12 (bits 3-14) and a signed displacement in the instruction word, bits 8 - 15. The CRU base address loaded into R12 must be twice the lowest memory bus address.

For this table, R12 = 2 × 0000.

[1] 1 = interrupt mode
0 = clock mode

[2] Interrupt mode function/clock mode function.

[3] Mask bit may be used to enable or disable the corresponding interrupt input (interrupt mode only). Mask bit 1, the exception, is set in the PIA.

[4] INTREQ is inverted form of interrupt request, MPINTREQ-.

[5] Inputs/outputs 0010 - 001F established by programming PIA after reset.

[6] 0 = slave words 1XXX XXXX XXXX XXXX
1 = slave words 0XXX XXXX XXXX XXXX

[7] Error clear (TLERRCLR) at CPU address 0060 removes TLTO, TLMER, UNITCH error conditions.

It is also possible to assign a CRU base address to some block of bits within the PIA. For example, it is desirable to treat the attention mask outputs (AT0-3) as a single block. The hardware base address for this group is the hardware base address of the PIA plus the displacement to the lowest numbered bit in the group. The hardware base address for the attention mask is 0000 + 001C = $001C_{16}$. A value twice as large (0038_{16}) must be loaded into TMS 9900 workspace register R12 because the LSB of the software CRU base address is dropped in the addressing process.

For MPAD08, MPAD09 = 01, which corresponds to 0040_{16} in workspace register 12, the data separator control register and the drive interface multiplexer are selected by the CRU device enable decoder. The data separator control register is an SN74259 8-bit addressable latch.

A CRU output instruction (SBO, SBZ, LDCR) places an address on the bus and the output data bit on the CRUOUT line at the leading edge of phase 2. It then enables CRU clock 333 nanoseconds later, on the next phase 2. The CRU clock is inverted in the CRU device enable decoder and is sent to the addressable latch as DSCRUCLK-. The low DSCRUCLK- signal enables the addressable latch to select an individual latch (based on LSB address bits MPAD12-14) and to load CRUOUT into the latch. The address and CRUOUT line are active for a total of 666.6 nanoseconds (two clock cycles at 3 MHz).

For a multibit output instruction, the cycle repeats with incremented addresses until the specified number of CRU bits are loaded into the register. Notice that the device interface multiplexer is also enabled during this cycle. The CRUIN output of the multiplexer is not sampled during an output cycle, so enabling the multiplexer has no effect on the operation.

A CRU input instruction (TB, STCR) places an address on the bus on phase 2 clock and samples the CRUIN line 250 nanoseconds later, on the trailing edge of the second phase 4 pulse. If the CRU base address in R12 is 0040_{16} and the displacement is 7 or less, the drive interface multiplexer steers an input to the CRUIN line. The inputs to the drive interface multiplexer, with the exception of DSCRCER and DPONL, are status inputs from the selected drive unit as received and decoded from the remote drive interface logic. Drive power on (DPONL) is a chassis status bit that specifies if a remote chassis is on line. These signals are described with the drive interface logic. DSCRCER is an error check signal that may be generated when reading back a sector header or a data record from the diskette. This signal is described with the cyclic redundancy check (CRC) logic.

Table 2-17 shows the CRU input and output bit assignments for the data separator control register and the drive interface multiplexer.

The TFDC on-board self-test programs require some data that is not otherwise required by controller operations. The test multiplexer provides eight additional input lines as shown in Table 2-18.

Table 2-17. CRU Bit Assignments for Disk Drive and Data Separator

Memory Bus Address*	MPAD (08,09 = 01) 10 11 12 13 14	CRU Read Data	CRU Write Data	9900 Program Mnemonics	
0020	0 0 0 0 0	DPONL	DSCNTL0-	DPONL	DSCNT0
0021	0 0 0 0 1	RDY	DSCNTL1-	RDY	DSCNT1
0022	0 0 0 1 0	INDEX	DSWMODE-	INDEX	DSWMOD
0023	0 0 0 1 1	WP	DSPRECOMP[1]	WP	DSPREC
0024	0 0 1 0 0	TS	DSMFM[2]	TS	DSMFM
0025	0 0 1 0 1	TR00	DSRDTST	TR00	DSTSTM
0026	0 0 1 1 0	DC	FAULTLED-	DC	FLTLED
0027	0 0 1 1 1	DSCRCER	DSMRST-	DCRCER	DSMRST

Notes:

* Memory bus address is derived within the TMS 9900 as the sum of a CRU base address in workspace register 12 (bits 3-14) and a signed displacement in the instruction word, bits 8 - 15. The CRU base address loaded into R12 must be twice the lowest memory bus address.

For this table, R12 = 2 × 0020 = 0040 (hex).

[1] 0 = write normal
1 = write precompensated

[2] 0 = FM mode
1 = MFM mode

Table 2-18. Test Multiplexer Inputs

Signature	Description
TLIFCNTR0	MSB of current state, from TILINE I/F controller. High for any TILINE operation.
TESTL	Loopback test bit. Sent from the TFDC (as DIR) to the power supply/interface board in the international chassis and looped back through the remote interface to the TFDC drive interface.
INTA	Interrupt A. High if an interrupt to the 990 computer is active, or if an interrupt is waiting for the controller idle status to become active.
SLSW16- through SLSW12-	TILINE base address switch settings for the TFDC.

Table 2-19. CRU Bit Assignments for Self-Test

Memory Bus Address*	MPAD (08,09 = 10) 10 11 12 13 14	CRU Read Data	9900 Program Mnemonics
0040	0 0 0 0 0	TLIFCNTR0	TLIFC0
0041	0 0 0 0 1	TESTL	TESTL
0042	0 0 0 1 0	INTA	INTA
0043	0 0 0 1 1	SLSW16-	SLSW16
0044	0 0 1 0 0	SLSW15-	SLSW15
0045	0 0 1 0 1	SLSW14-	SLSW14
0046	0 0 1 1 0	SLSW13-	SLSW13
0047	0 0 1 1 1	SLSW12-	SLSW12

Notes:

* Memory bus address is derived within the TMS 9900 as the sum of a CRU base address in workspace register 12 (bits 3-14) and a signed displacement in the instruction word, bits 8 - 15. The CRU base address loaded into R12 must be twice the lowest memory bus address.

For this table, R12 = 2 × 0040 = 0080_{16}.

The CRU base address (R12) is 0080_{16} for the test inputs. Self-test CRU bit assignments are shown in Table 2-19.

2.6.6 9900 Memory Bus Communication

The TMS 9900 memory bus consists of the microprocessor address bus (MPAD00-14), the microprocessor data bus (MPDB00-15), and control lines (MPREADY, MEMEN-, DBIN, MPWE-). The memory bus is used for the following types of communication:

- ROM instruction read
- RAM read/write
- TILINE address register/counter loading
- Register file read/write
- Special-purpose control functions

2.6.6.1 Memory Address Space. The address space of a TMS 9900 microprocessor covers 32 768 word addresses, or 65 536 byte addresses. Byte selection, where used, is internal to the TMS 9900 microprocessor. The memory bus always works with 16-bit words. Each word address is on an even byte boundary. The memory address space is described in terms of CPU byte addresses because these are the addresses which appear in the assembly language and machine language instructions sets of the microprocessor.

Figure 2-44 is a map of the memory address space in the TILINE flexible disk controller. The addresses (in hexadecimal format) run from 0000 to FFFE. The first 4096 (0-1FFE) words of the address space are control program read-only-memory (ROM) addresses. The permanent program stored in the ROM controls, directly or indirectly, all of the TFDC operations, based on command words W0-W7 and inputs from the TILINE and the drive units.

The first 14 ROM words are interrupt vectors for servicing the interrupts described in the interrupt and CRU I/O description. An interrupt vector consists of two values, a pointer to the workspace associated with that interrupt, and a starting address for the interrupt service subroutine. These two values must be stored in order. The workspace pointer (WP) should be followed by the program counter (PC). The program counter points to an address within the control program ROM, but the workspace pointer must point to an address in the read/write (RAM) memory, as workspaces are dynamic scratchpads.

The next 30 ROM words are vectors that call self-test routines, special test routines, and the idle routine. As with the interrupt vectors, each routine call vector is a WP-PC pair. These routines can be considered as software external operations (XOPs) added to the basic TMS 9900 instruction set.

The next group of ROM addresses contains tables of constants which are used throughout the control program. For example, these constants include the form of the data marks and address marks for FM and MFM recording, delay constants, masks, and test patterns.

One group of addresses is dedicated to commonly used, single-bit CRU instructions for control of unit selection bits and attention mask bits. Grouping these commonly used functions so that they may be identified by a label, or a label and a small displacement, saves many ROM locations.

The main control program starts at CPU byte address 00EC, and continues to the end of the ROM address space.

CPU byte addresses 2000 to 7FFE are currently unused.

The 256-word scratchpad RAM extends from address 8000 through 81FE. Many of the scratchpad addresses are labeled for dynamic storage of specific variables. The workspaces associated with execution of control program routines and subroutines share the scratchpad with the variables. The upper end of the scratchpad RAM is used for an instruction trace of the previous 12 command word groups (W0-W7) from the 990 computer.

The block of addresses from 8200 through 8FFE are in the RAM address space (as specified by the RAM chip select, RAMDBEN-) but are not currently implemented by memory devices.

Most of the rest of the address range up to FFFE is unused. These ranges of address space that are not required by memory may be used for special purpose control functions. For example, a read operation to address F800 is decoded to initiate a TILINE master read operation, and a write operation to address FA00 initiates a TILINE master write operation. The use of spare addresses for control functions is described in more detail with address decoding.

2.6.6.2 Address Decoding. The memory address space of the TMS 9900 covers a 64-kilobyte range from CPU byte address 0000 to FFFF. The 9900 control program requires 8 kilobytes in the range 0000 to 1FFE, and the scratchpad RAM requires 256 bytes in the range 8000 to 81FE. The remaining memory addresses are either unused or reserved for special control functions.

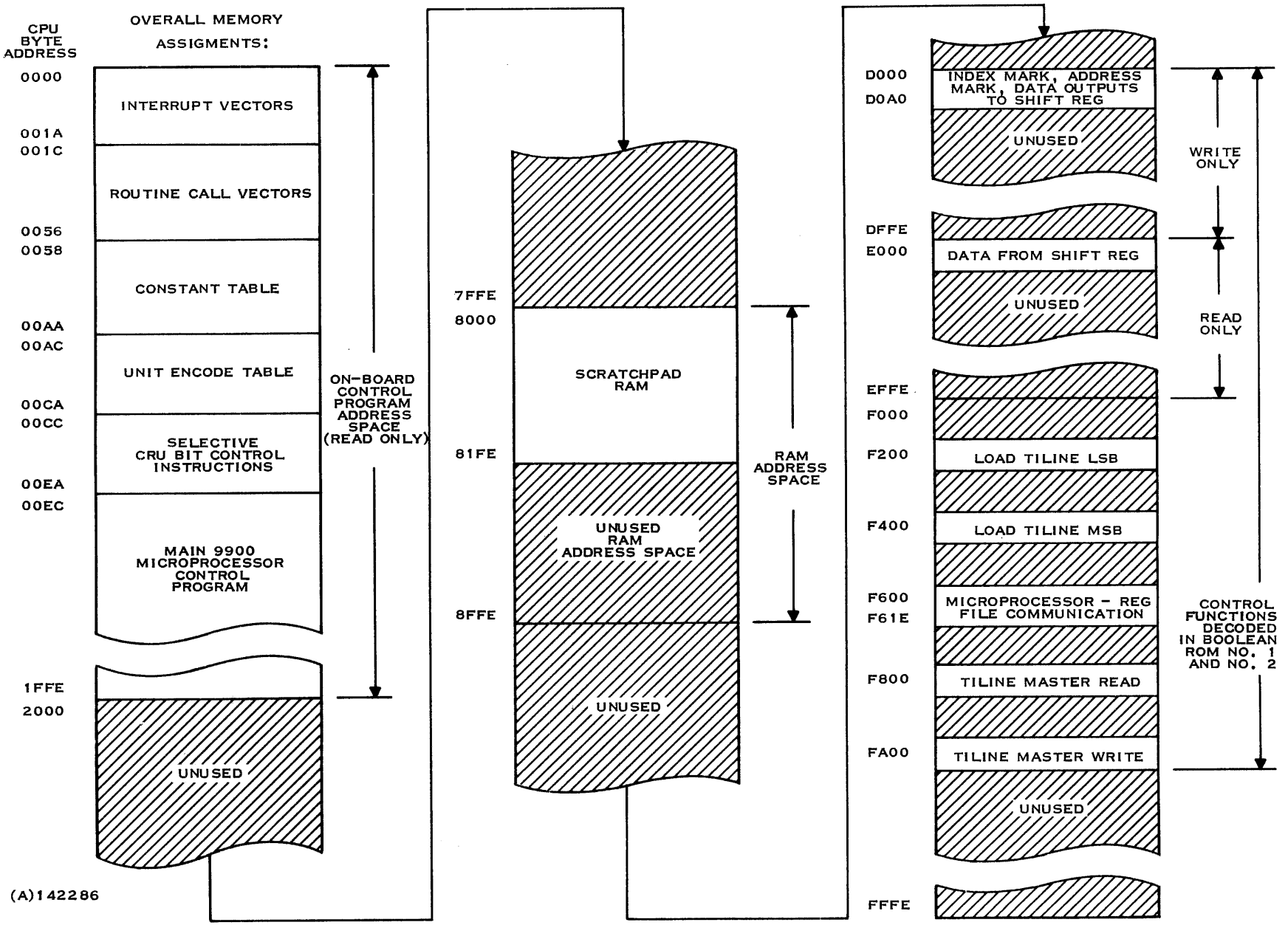


Figure 2-44. TFDC Central Processor Address Space Map

The microprocessor address bus (MPAD00-15) is driven by the address output of the TMS 9900 microprocessor. The address placed on the bus is determined by the instruction currently being executed by the microprocessor. The control program ROM is the ultimate source of the address, as it supplies the instructions executed by the 9900.

The address bus is shared between CRU operations and memory operations. The control signals which accompany an address identify the type of operation. The memory enable (MEMEN-) signal is active (low) for any memory operation, and the CRU clock (CRUCLK) is active (high) for CRU operations.

Access to the microprocessor data bus (MPDB00-15) is controlled by the data bus in (DBIN) control signal from the microprocessor. DBIN, when low, indicates that the TMS 9900 data output drivers are actively driving the data bus. Therefore, a low DBIN signal, with MEMEN- low, identifies a memory write operation. This "write" operation may also be a data transfer from the microprocessor data bus to another bus in the controller. These interbus transfers are treated like a memory operation, with an address dedicated to the bus transfer operation.

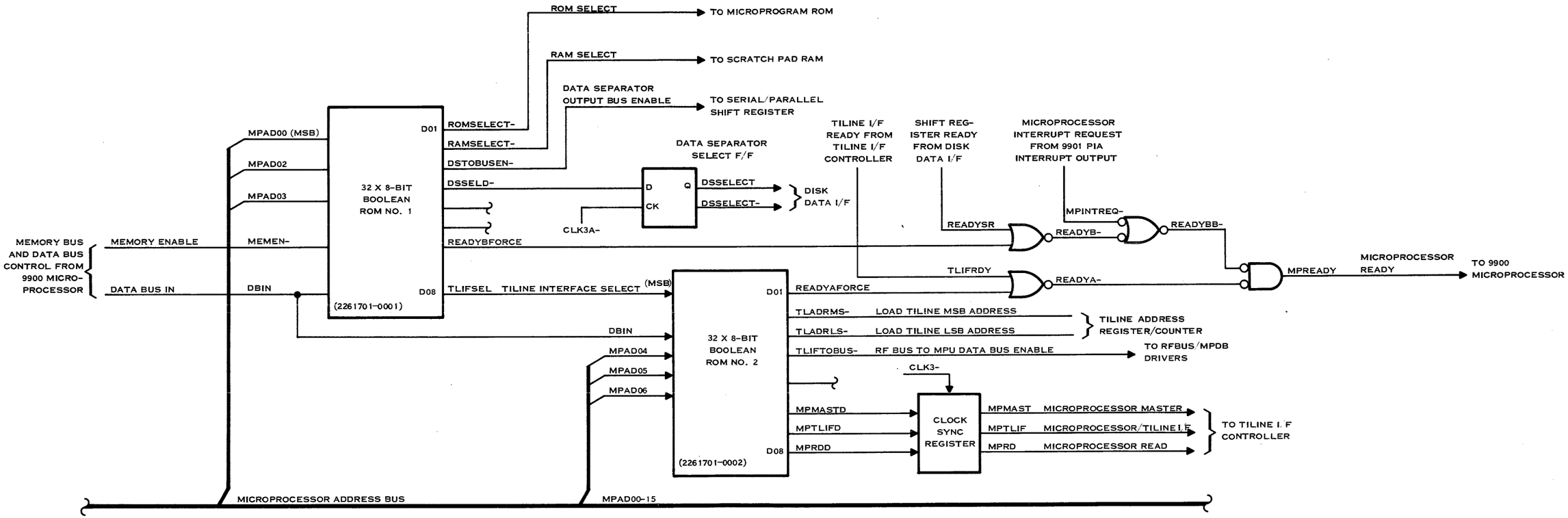
DBIN, when high, indicates that the TMS 9900 data bus drivers are disabled so that a memory (or other data source) may place data on the data bus lines. This "read" operation may be a transfer of data from another bus to the MPU data bus rather than an actual read from ROM or RAM. As stated in the previous paragraph, interbus transfers may be treated as ordinary memory operations at a dedicated address.

Refer to the address decoding logic, which is shown in Figure 2-45 and on sheet 3 of the TFDC logic diagram. The address decoding logic monitors the higher order address bits to determine within which of the preassigned ranges an address fits. Based on this range and the states of the DBIN and MEMEN- control signals, the address decoding logic issues memory enable or control strobe signals.

Most of the work of the address decoding logic is performed by two SN74S288 devices, Boolean ROM #1 and Boolean ROM #2. These ROM devices are operated in partial cascade, with the TLIFSEL output of ROM #1 serving as the MSB address input of ROM #2.

Table 2-20 and Table 2-21 summarize the address ranges and corresponding decoded outputs for the Boolean ROMs.

Boolean ROM #1 outputs are used to enable the control program ROM, scratchpad RAM, data separator or the TILINE/register file interface (via ROM #2). Notice that MPAD00, MPAD02, and MPAD03 are utilized in the decoding, but MPAD01 is not connected to the ROM inputs. This makes it appear that the ROM would respond identically to two addresses which differ by 16K bytes. Because the dedicated addresses are chosen so that they are not separated by exactly 16K bytes no actual problem occurs. Also notice that the data separator select signal is synchronized to the trailing (rising) edge of CLK3- by a flip-flop. Synchronization to CLK3- eliminates skew due to ROM access time.



(C)142287

Figure 2-45. Address Decoding Logic

Table 2-20. Boolean ROM #1 Decoded Outputs

CPU Byte Address Range	Output	Description
0000 - 1FFE	ROMDBEN-	ROM data bus enable. Chip select signal which enables the 9900 control program ROM outputs onto the data bus.
8000 - 8FFE	RAMSELECT-	Chip select signal which enables the scratchpad RAM. The 256-word RAM occupies the range 8000 - 81FE. Addresses from 8200 - 8FFE are not used.
E000 - EFFE	DSTOBUSEN-	Data separator output bus enable. Enables data from the data separator onto the microprocessor data bus.
D000 - EFFE	DSSELD-	Data separator select. Select data separator shift register for input/output. Addresses used are: D000 Send data to data separator D020 Send MFM address mark D0A0 Send FM index mark D0E0 Send FM address mark E000 Accept from data separator (coincides with DSTOBUSEN- for data read)
F000 - FFFE	TLIFSEL	TILINE interface select. Effectively an enabling signal to Boolean ROM #2, which decodes addresses associated with TILINE input/output. Connected to MSB address input of ROM #2.
All except D000 - EFFE	READYBFORCE	READYBFORCE from Boolean ROM #1 and READYAFORCE from Boolean ROM #2 force a microprocessor ready (MPREADY) under most conditions. READYBFORCE low is an interlock which holds off MPREADY when transferring data to/from the data separator. Under these conditions, a shift register ready (READYSR) is required to enable the MPU in synchronism with the data separator operation. An MPU interrupt (MPINTREQ-) will also enable MPU operation.

Table 2-21. Boolean ROM #2 Decoded Outputs

CPU Byte Address Range	Output	Description
All Except	READYAFORCE	READYAFORCE from Boolean ROM #2 and F600, FA00, READYBFORCE from Boolean ROM #1 F800 force a microprocessor ready (MPREADY) condition for most conditions. READYAFORCE low is a timing interlock used during TILINE operations to hold off the microprocessor until TILINE interface ready (TLIFRDY) reenables the MPU. READYA- and READYB- must both be active to enable MPREADY.
F200	TLADRLS-	Load TILINE address LSBs. Loads 16-bit MPU data word into the 16 least significant bit positions of the TILINE address register/counter.
F400	TLADRMS-	Load TILINE address MSBs. Loads least significant four bits from MPU data word into the four most significant bit positions of the TILINE address register/counter.
F600, F800	TLIFTOBUS-	TILINE interface to bus. Gates register file bus (RFBUS00-15) outputs onto microprocessor data bus.
F800, FA00	MPMASTD	MPU select TILINE master cycle. Low to permit TILINE slave operations.
F600, F800, FA00	MPTLIFD	MPU-initiated TILINE interface or register file operation.
F600, F800	MPRDD	Microprocessor read. High for MPU read from TILINE or register file.

Boolean ROM #2 outputs are dedicated to control of TILINE and register file operations. The MEMEN- signal is not wired to ROM #2, but is implicitly included in the decoding because MEMEN- active (low) is a required condition to enable TLIFSEL. The MPMAST, MPTLIF, and MPRDD outputs of ROM #2 are used to initiate and direct operations of the TILINE I/F controller. These signals are synchronized to the trailing (rising) edge of CLK3- before they are sent to the TILINE I/F controller. Synchronizing these control signals eliminates any possible skewing due to the access times of the Boolean ROMs.

Notice the discrete logic gates and input signals that enable MPREADY (microprocessor ready). MPREADY indicates to the MPU that the memory will be ready to read or write during the next clock cycle. If MPREADY is low and the instruction being executed refers to memory, the MPU enters a wait state and suspends internal operations until MPREADY returns high. All MPU outputs (except the WAIT line) are unchanged during the wait. On a write operation, the write data is held on the microprocessor data bus so that a slower device may accept the data during the wait period. On a read operation, the input data is not clocked into the MPU until after the wait. This allows a slower device to delay MPU operation until the data is available at the MPU inputs.

Microprocessor operations are synchronous with the four-phase crystal-controlled clock generator that produces CLK3-, microprocessor clock. The TILINE interface is asynchronous, timing being dependent on such variables as slot position and current TILINE activity. The data separator/encoder data rate is based on the time required for serial-parallel conversions of 16-bit words and the allowable word spacing on the disk. Control of MPREADY allows the microprocessor to read or write data that is not synchronized to the microprocessor clock.

READYBFORCE is high for all operations except those that involve data transfer to or from the data separator. READYBFORCE low disables MPREADY and suspends microprocessor operation until the shift register ready (READYSR) occurs. READYSR allows the MPU to resume synchronous operation as if no delay had occurred. An interrupt condition such as a data separator overrun will also restart the microprocessor.

READYAFORCE is high for all operations except those that involve TILINE data transfer. READYAFORCE low disables MPREADY and puts the MPU in a wait state until the TILINE interface ready (TLIFRDY) occurs. The variable-length wait state adapts the MPU read or write cycle to the TILINE interface.

Tables 2-22 and 2-23 are the HI-LO listings of the Boolean ROMs. Input and output signal names have been added to clarify the listings. The corresponding CPU byte addresses have been placed on each row in which an important control output is active. The listings apply to part numbers 2261701-0001, rev **, and 2261701-0002, rev **. If your unit has a different revision level, use the standard listings, 2261891-9002 and 2261891-9003.

2.6.6.3 Microprocessor/ROM Communication. Figure 2-46 is a detailed block diagram which shows the 9900 memory bus organization. The TMS 9900 reads an instruction or data word from the control program ROM by placing an address in the range 0000 - 1FFE on MPAD00-14, issuing a memory enable (MEMEN- low) and disabling the TMS 9900 output data drivers (DBIN high). The address decoding logic responds by issuing a ROM to data bus enable (ROMDBEN- low). The TMS 4732 ROM devices respond by placing the accessed word on the data bus.

Timing for this operation is shown in Figure 2-47. The microprocessor initiates the read cycle on the leading edge of phase 2 clock by placing the address on the MPAD00-14 lines, forcing MEMEN- low, and setting DBIN high. Microprocesssor write enable remains inactive (MPWE- high). The address decode logic generates ROMDBEN-, enabling the ROM output drivers. The access time of the TMS 4732 is approximately 450 nanoseconds after address selection.

Table 2-22. Boolean ROM -1 Listing

Address Binary	Hex	MPAD00	MPAD02	MPAD03	MEMEN-	DBIN	TLIFSEL	READYBFORCE			DSSELD	DSTOBUSEN-	RAMSELECT-	ROMDBEN-	CPU Byte Address
00000	00	L	L	L	L	L	L	H	H	H	H	H	H	H	
00001	01	L	L	L	L	L	L	H	H	H	H	H	H	(L)	0000-0FFE
00010	02	L	L	L	L	L	L	H	H	H	H	H	H	H	
00011	03	L	L	L	L	L	L	H	H	H	H	H	H	H	
00100	04	L	L	L	L	L	L	H	H	H	H	H	H	H	
00101	05	L	L	L	L	L	L	H	H	H	H	H	H	(L)	1000-1FFE
00110	06	L	L	L	L	L	L	H	H	H	H	H	H	H	
00111	07	L	L	L	L	L	L	H	H	H	H	H	H	H	
01000	08	L	L	L	L	L	L	H	H	H	H	H	H	H	
01001	09	L	L	L	L	L	L	H	H	H	H	H	H	H	
01010	0A	L	L	L	L	L	L	H	H	H	H	H	H	H	
01011	0B	L	L	L	L	L	L	H	H	H	H	H	H	H	
01100	0C	L	L	L	L	L	L	H	H	H	H	H	H	H	
01101	0D	L	L	L	L	L	L	H	H	H	H	H	H	H	
01110	0E	L	L	L	L	L	L	H	H	H	H	H	H	H	
01111	0F	L	L	L	L	L	L	H	H	H	H	H	H	H	
10000	10	L	L	L	L	L	L	H	H	H	H	H	(L)	H	8000-8FFE
10001	11	L	L	L	L	L	L	H	H	H	H	H	(L)	H	8000-8FFE
10010	12	L	L	L	L	L	L	H	H	H	H	H	H	H	
10011	13	L	L	L	L	L	L	H	H	H	H	H	H	H	
10100	14	L	L	L	L	L	L	(L)	H	H	(L)	H	H	H	D000-DFFE
10101	15	L	L	L	L	L	L	H	H	H	H	H	H	H	
10110	16	L	L	L	L	L	L	H	H	H	H	H	H	H	
10111	17	L	L	L	L	L	L	H	H	H	H	H	H	H	
11000	18	L	L	L	L	L	L	H	H	H	H	H	H	H	
11001	19	L	L	L	L	L	L	(L)	H	H	(L)	(L)	H	H	E000-EFFE
11010	1A	L	L	L	L	L	L	H	H	H	H	H	H	H	
11011	1B	L	L	L	L	L	L	H	H	H	H	H	H	H	
11100	1C	(H)	L	L	L	L	L	H	H	H	H	H	H	H	F000-FFFE
11101	1D	(H)	L	L	L	L	L	H	H	H	H	H	H	H	F000-FFFE
11110	1E	L	L	L	L	L	L	H	H	H	H	H	H	H	
11111	1F	L	L	L	L	L	L	H	H	H	H	H	H	H	

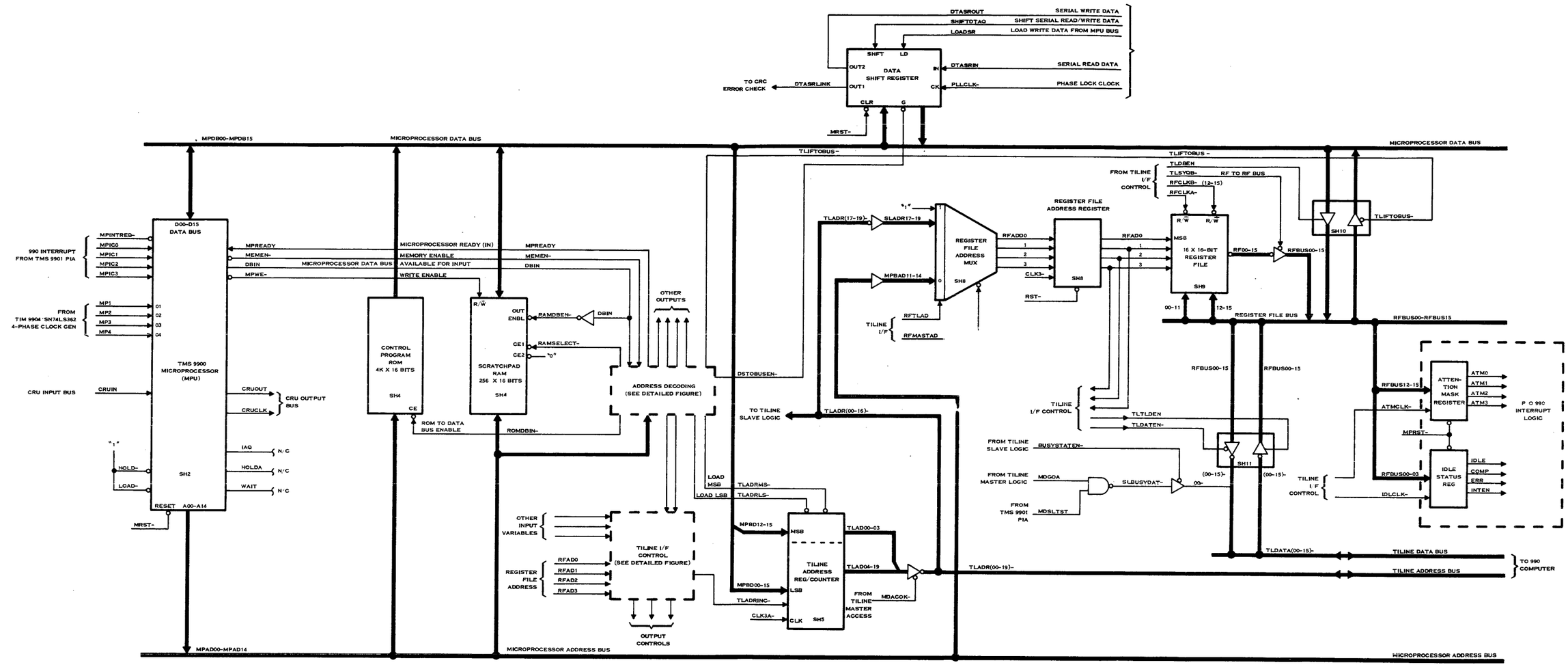
The memory data is not loaded into the TMS 9900 until the second phase 1 pulse after cycle initiation. The data must be stable at least 40 nanoseconds before the phase 1 pulse leading edge, and 20 nanoseconds after the trailing edge. The phase 2 clock releases the bus control signals, and ROMDBEN- returns high. The total time for this memory read cycle is approximately 666.6 nanoseconds, or two clock cycles.

Table 2-23. Boolean ROM -2 Listing

Address Binary	Hex	MPRDD	MPTLIF	MPMASTD	N/C	TLIFTOBUS-	TLADRLS-	TLADRMS-	READYAFORCE	CPU Byte Address
00000	00	L	L	L	H	H	H	H	H	
00001	01	L	L	L	H	H	H	H	H	
00010	02	L	L	L	H	H	H	H	H	
00011	03	L	L	L	H	H	H	H	H	
00100	04	L	L	L	H	H	H	H	H	
00101	05	L	L	L	H	H	H	H	H	
00110	06	L	L	L	H	H	H	H	H	
00111	07	L	L	L	H	H	H	H	H	
01000	08	L	L	L	H	H	H	H	H	
01001	09	L	L	L	H	H	H	H	H	
01010	0A	L	L	L	H	H	H	H	H	
01011	0B	L	L	L	H	H	H	H	H	
01100	0C	L	L	L	H	H	H	H	H	
01101	0D	L	L	L	H	H	H	H	H	
01110	0E	L	L	L	H	H	H	H	H	
01111	0F	L	L	L	H	H	H	H	H	
10000	10	L	L	L	H	H	H	H	H	
10001	11	L	L	L	H	H	(L)	H	H	F200
10010	12	L	L	L	H	H	H	(L)	H	F400
10011	13	L	(H)	L	H	H	H	H	(L)	F600
10100	14	L	L	L	H	H	H	H	H	
10101	15	L	(H)	(H)	H	H	H	H	(L)	FA00
10110	16	L	L	L	H	H	H	H	H	
10111	17	L	L	L	H	H	H	H	H	
11000	18	L	L	L	H	H	H	H	H	
11001	19	L	L	L	H	H	H	H	H	
11010	1A	L	L	L	H	H	H	H	H	
11011	1B	(H)	(H)	L	H	(L)	H	H	(L)	F600
11100	1C	(H)	(H)	(H)	H	(L)	H	H	(L)	F800
11101	1D	L	L	L	H	H	H	H	H	
11110	1E	L	L	L	H	H	H	H	H	
11111	1F	L	L	L	H	H	H	H	H	

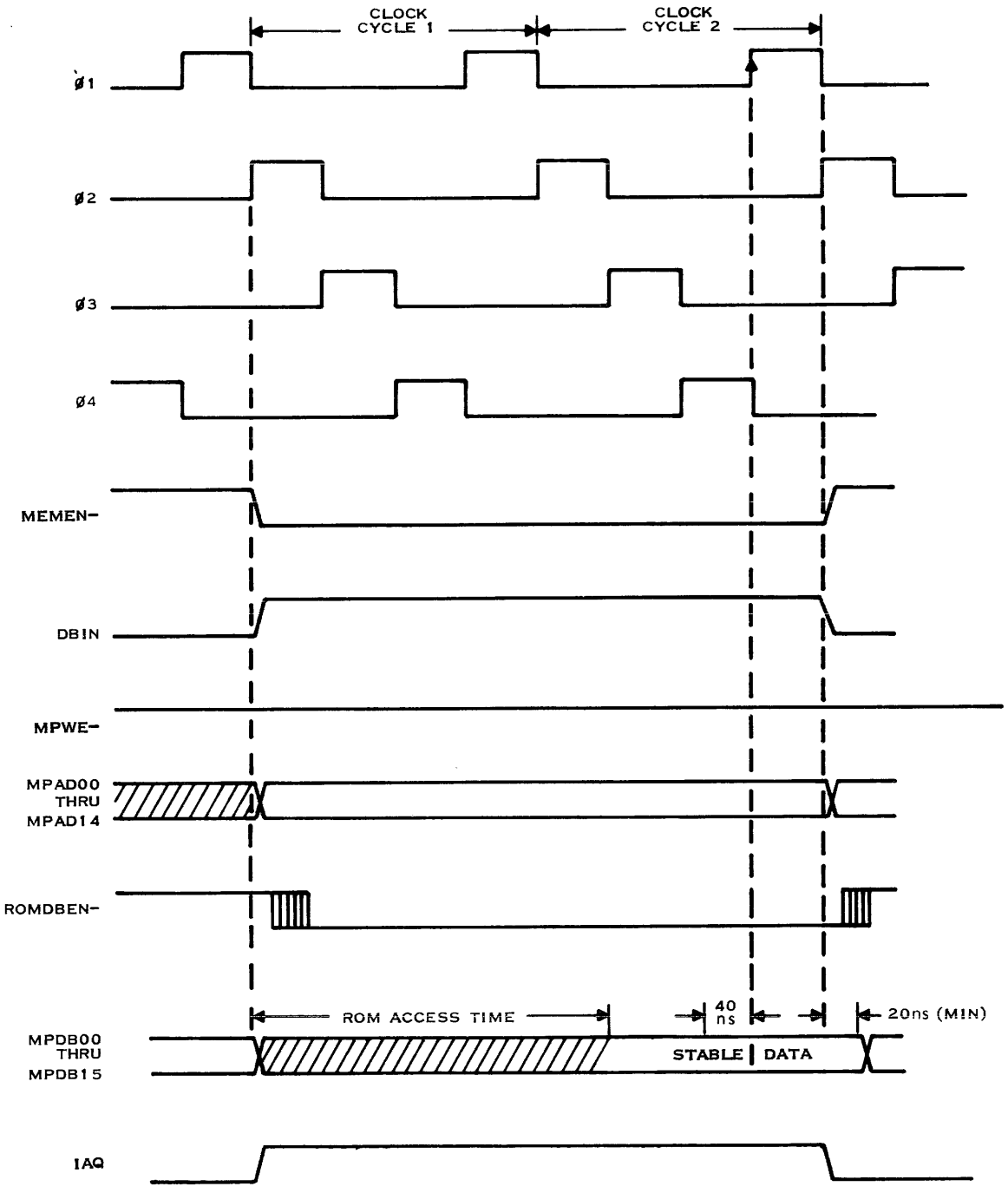
TLIFSEL, DBIN, MPAD04, MPAD05, MPAD06

2.6.6.4 Microprocessor to Scratchpad RAM Communication. Refer back to the detailed block diagram of memory bus communications, Figure 2-46 The scratchpad RAM is comprised of four TMS 4042-2 (256 by 4-bit) devices. The RAMSELECT- signal from the address decoding logic selects the RAM for operation, and the RAMDBEN- signal enables the RAM output drivers for read operations. The MPWE- signal, wired direct from the microprocessor write enable (WE-) output, controls read/write selection.



(R)142288

Figure 2-46. TMS 9900 Memory Bus and Register File Communication



NOTES: 1. ACCESS TIME FROM ADDRESS = 450 ns FOR TMS 4732 ROM

2. DATA MUST BE STABLE 40 ns BEFORE AND 20 ns AFTER PHASE 1 PULSE

(A)142289

Figure 2-47. Read Timing Cycle — Control Program ROM

Timing for the scratchpad RAM read operation (Figure 2-48) is virtually identical to the ROM read timing. The main difference is that RAM access time is measured from the RAMSELECT- signal. ROM access time is measured from the input address change, with ROMDBEN- active to enable the output. The RAMDBEN- signal must be low (DBIN high), and the active low write enable (MPWE-) must be high. As shown on the ROM/RAM read timing diagram, the bus control signals are activated on phase 2 clock, and the data is loaded into the microprocessor on the second phase 1 pulse. The read cycle occupies two microprocessor clock cycles. MPREADY is high when sampled, as MPREADY is high throughout all TFDC RAM read/write cycles.

NOTE

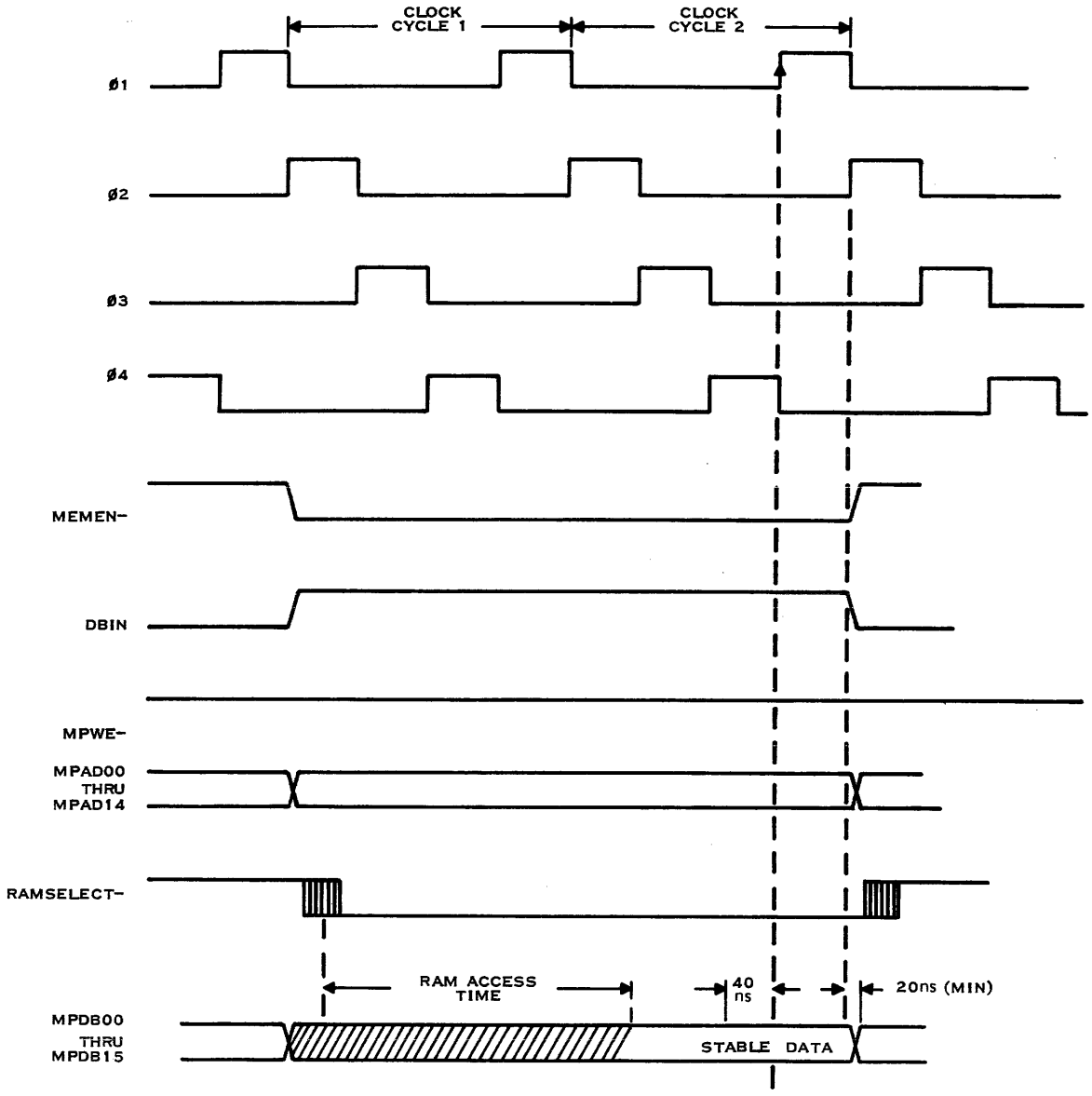
There are several versions of the TMS 4042 RAM device available. Access times range from 1000 nanoseconds to 450 nanoseconds. The 450-nanosecond version, TMS 4042-2, must be used in the TFDC, as there is no provision for wait states to accommodate slower RAM devices.

Figure 2-49 shows timing for a RAM write cycle. The memory cycle starts on the trailing edge of phase 1 with an address and memory enable (MEMEN-) low. DBIN remains low, as this is a microprocessor output cycle. The address decoding logic enables the RAM cycle with RAMSELECT-. The MPREADY signal is always high for RAM read/write cycles. Microprocessor write enable (MPWE-) goes active (low) on the leading edge of the next phase 1 pulse after RAMSELECT-. The RAM must accept the data by the leading edge of the next phase 1 pulse, when MPWE- returns high. The other control signals return to inactive states on the trailing edge of phase 1. The RAM write cycle, like the read cycle, requires two microprocessor timing cycles (approximately 666.6 nanoseconds overall).

2.6.6.5 Microprocessor to TILINE Address Register/Counter. The TILINE address register/counter holds the 20-bit TILINE address required for TILINE master cycle operations. Recall that a buffer area is established in TILINE memory for any data transfer to or from the disk. For a read-type operation, (Read Data, Read Data Unformatted) this is the buffer where the TFDC sends the data read from the disk. For a write-type operation (Write Data, Write Format), this is the buffer which contains the data to be recorded. The starting address of this buffer is sent to the TFDC slave registers as part of the setup parameters.

The starting address must be loaded into the TILINE address register/counter as part of the operation setup. A subroutine in the microprocessor control program reads the slave register words into the TMS 9900 workspace registers, modifies them to fit the TFDC internal format, and sends them to the address register counter with a pair of successive MOV operations.

Because the 16-bit microprocessor data bus is not large enough for the 20-bit address, the loading operation must be completed in two separate load cycles. The four most significant TILINE address bits (TLAD00-03) are loaded from the least significant bits of the data bus in one instruction, and the remaining 16 bits are loaded in another instruction. Separate loading strobes are issued by the address decoding logic.



NOTES: 1. ACCESS TIME FROM RAMSELECT – ≈ 450ns FOR TMS4042-2 RAM

2. DATA MUST BE STABLE 40 NANOSECONDS BEFORE AND 20 NANOSECONDS AFTER PHASE 1 PULSE

(A)142290

Figure 2-48. Read Timing Cycle — Scratchpad RAM

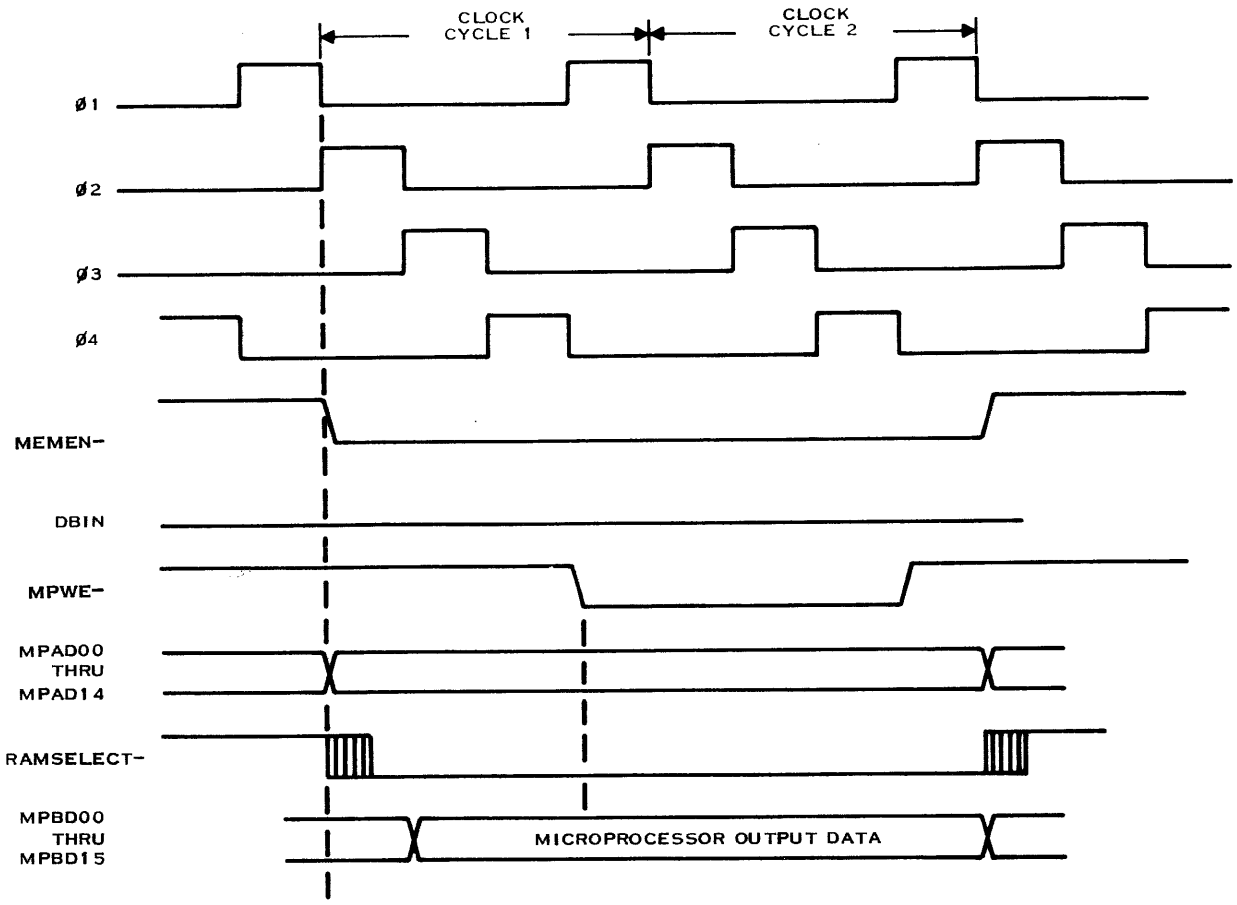


Figure 2-49. Write Timing Cycle — Scratchpad RAM

A single MOV instruction to load one of the two operands in the address register/counter requires seven TMS 9900 machine cycles. Each machine cycle is two clock cycles. The first machine cycle reads the MOV instruction from the control program ROM into the microprocessor. The second cycle is an ALU internal cycle, which is followed by a read to fetch the contents of the workspace register from the scratchpad RAM. The fourth cycle is an ALU internal cycle. The fifth cycle is a read operation addressed to the eventual destination (F200 or F400). The MOV operation ignores whatever it reads back on this cycle, which is good, because there is no input data path. The sixth cycle is an ALU internal cycle. The seventh cycle is a write to the TILINE address register/counter, address F200 or F400.

Memory address F200 is a special function address reserved for the load TILINE LSB function. F200 is not implemented in memory. A memory write operation directed to F200 causes the address decoding logic to produce the active low TLADRLS- strobe about 50 nanoseconds after the address bus stabilizes. At this point, the 15-bit data word is stable and available at the parallel load inputs of the address register/counter. The data word is clocked in on the rising (trailing) edge of CLK3-. The timing for this operation is shown in Figure 2-50. The timing is identical for the load TILINE MSB function. The only changes are the signature of the load command, TLADRMS-, and the CPU byte address, F400.

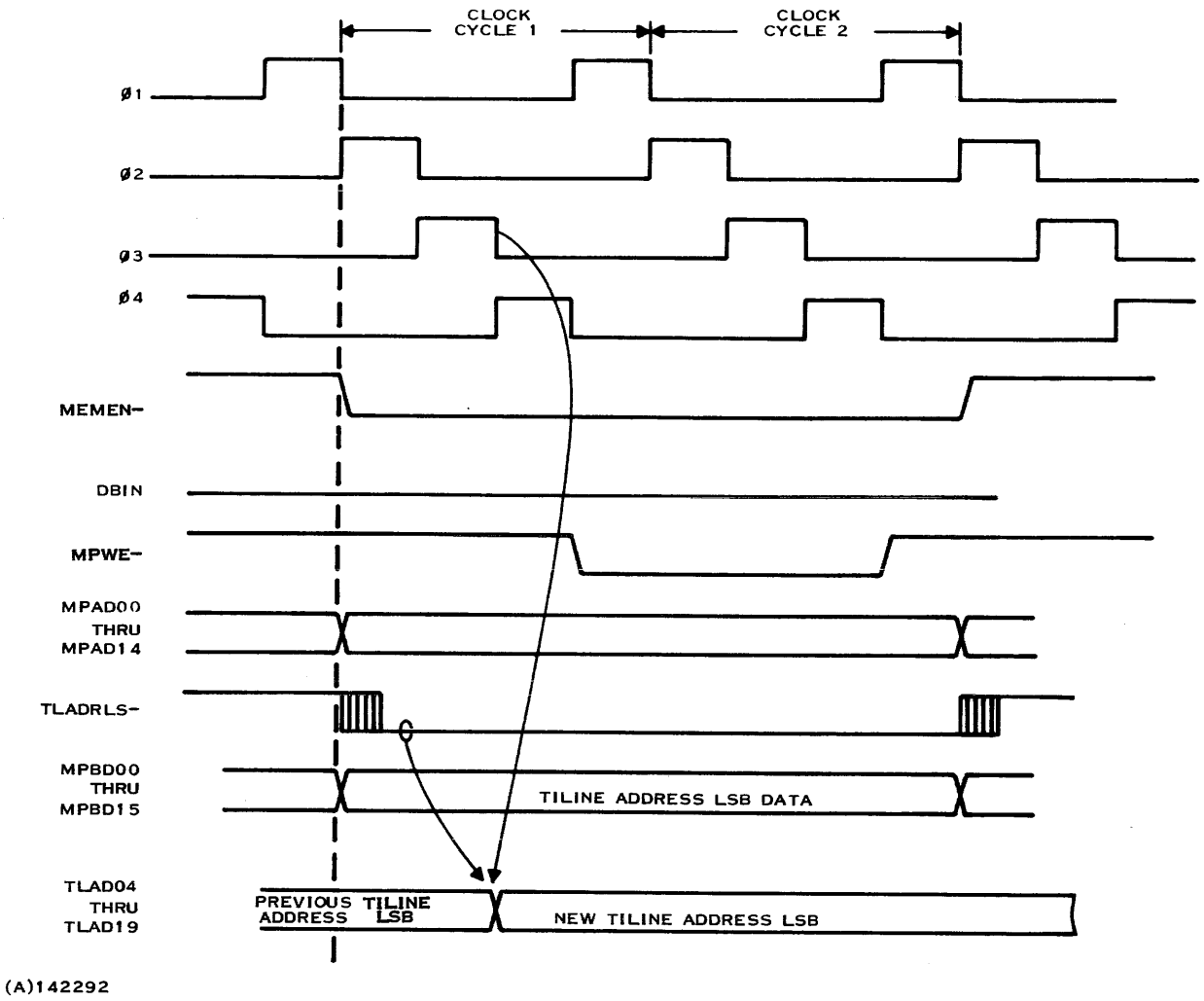


Figure 2-50. Write Timing Cycle for Loading TILINE Address Register/Counter

The TILINE address register/counter increments the 20-bit TILINE address after each master cycle, on command (TLADRINC) from the TILINE I/F control logic.

2.6.6.6 Register File Communication. The register file is a 16 by 16-bit fast RAM comprised of four SN74S189 bipolar Schottky devices. Typical access time (read or write) for this device is 25 nanoseconds. The upper eight addresses in the register file (register files 8-15) are the slave word registers that store TFDC control words W0-W7. Register file 0 is the transfer file that holds disk data words moving between the TILINE and the data separator/encoder logic.

The 16-bit register file bus (RFBUS00-15) supplies data inputs to, and accepts outputs from, the register file. The register file bus may exchange data with either the TILINE data bus (TLDATA00- through TLDATA15-) or with the microprocessor data bus. The TILINE I/F control logic controls all of these interbus transfers except register file bus to microprocessor data bus transfers. The TILINE I/F control logic also controls address selection, write clocking, and output gating of the register file.

The register file address multiplexer, under control of the TILINE I/F control logic, selects a four-bit register file address. This address (RFADD0-3) is synchronized to CLK3- in an address register. The latched and synchronized register outputs (RFAD0-3), are connected to the register file address inputs.

The RFMASTAD (register file master address) signal is connected to the active low strobe input of the register file address multiplexer. During a TILINE master read or write cycle, the TILINE I/F controller sets RFMASTAD high, disabling the multiplexer. The multiplexer outputs go to 0000, which selects register file 0 on the next CLK3- pulse. All TILINE master cycles use register file 0 as a transfer register.

Note that a TILINE master read cycle is initiated by the control program. A read to CPU byte address F800 causes the address decoding logic to specify a master cycle (MPMAST), specify a read operation (MPRDD), and initiate the TILINE I/F control logic (MPTLIFD). These control signals are sent to the TILINE I/F control logic, which directs the sequence of events.

A TILINE master write cycle is initiated by the control program in a similar manner, with a write to CPU byte address FA00. In this case, the MPRDD output of the address decoder is inactive (low), and TLIFTOBUS- is high. The RFMASTAD and RFTLAD outputs are supplied by the TILINE I/F control logic, which is directly responsible for register file and register file bus control.

For any register file operation other than a TILINE master read or write cycle, RFMASTAD remains low, and RFTLAD (register file TILINE address) steers the address multiplexer. RFTLAD is high for TILINE slave read or write operations. RFTLAD selects the three least significant bits of the TILINE slave address (in active high form, SLADR17-19) and a hardwired "1" in the MSB address position. The hardwired "1" biases the register file address by eight so that slave address 000 refers to register file 8, 001 refers to register file 9, . . . and 111 refers to register file 15.

TFDC control words W0-W7 are loaded into register file 8-15 by TILINE slave write cycles and may be read back as status words by slave read cycles. Slave read or write cycles are initiated by the 990 computer in which the TFDC is installed. The TILINE slave logic on the TFDC recognizes the operation and informs the TILINE I/F control logic. The TMS 9900 microprocessor is not involved in this operation.

For a slave read operation, the contents of the register file selected by the slave address bits are gated onto the register file bus (TLSYQB- low), and the register file bus to TILINE drivers are enabled by TLDATEN-.

For a slave write operation, addressing is identical to the slave read operation. TILINE data (inverted to active high form) is gated to the register file bus by TLTLDEN. A register file write requires register file clock inputs. Clocking is split, with RFCLKA- loading data into RF00-11 and RFCLKB- loading data into RF12-15. The TILINE interface control logic uses the register file address and the next state to determine if one or both clocks should be enabled. Split clocking of the register file is required because the attention mask bits (W0, bits 12-15) must not be modified by a TFDC internal operation, and the drive status bits (W0 bits 0-11) must not be modified by a slave write from the 990 computer. Split clocking allows separate updates to these fields.

Notice that the attention mask register and the idle status register are fed by the register file bus. The attention mask register is loaded from the four least significant bits of control word WO. The idle status register is loaded from the four most significant bits of control word W7. These registers are clocked by the attention mask clock (ATMCLK-) and the idle clock (IDLCLK-), respectively. These hardware registers are loaded during the slave write sequence on the next TILINE I/F controller state after the register file is loaded.

The TMS 9900 microprocessor has access to all 16 registers in the register file, by reference to dedicated CPU byte addresses F600 (register file 0) through F61E (register file 15). A register file access to one of these dedicated addresses causes the address control logic to inititiate TILINE I/F controller operation (MPTLIF) and specify read or write (with MPRDD). For a read operation, the address decode logic also gates the register file bus to the microprocessor data bus (TLIFTOBUS-).

The TILINE I/F controller sets MPMASTD low to enable the register file address multiplexer. RFTLAD low selects the four least significant bits of the microprocessor address bus (MPAD11-14). This address is clocked into the address register on the trailing edge of the next CLK3- pulse. For a register file read, the TILINE I/F control logic enables the register file output onto the bus (TLSYQB-) and the address decoding gates the register file bus to the microprocessor data bus with TLIFTOBUS-.

A register file write requires register file clock inputs. Clocking is split, with RFCLKA- loading data into RF00-11, and RFCLKB- loading data into RF12-15. The TILINE interface control logic uses the register file address to determine if one or both clocks should be enabled. For a microprocessor write to register 0, RFCLKA- gates bits 00-11 into the register file, but the microprocessor is not allowed to modify bits 12-15.

2.6.7 Attention Mask, Status Register, and 990 Interrupt Logic

The TFDC has the capability to issue interrupts to the 990 processor if interrupts are enabled. Interrupts may be enabled as part of the operation setup or by a previous attention mask. An interrupt from the TFDC indicates that the flexible disk system has completed some operation and is currently idle.

2.6.7.1 Interrupt Introduction. TFDC interrupts are enabled by the control words that set up the operation. A logic 1 in W7, bit 3 enables the operation complete interrupt. This interrupt is generated when the TFDC completes the commanded operation (normally or abnormally) and returns to the idle mode. Control/status word W7 in the TFDC register file contains updated controller status from the completed operation.

The least significant four bits of control word W0 from the 990 computer is a position-coded attention interrupt mask. Each attention mask bit is associated with a drive unit. There is also an attention bit (generated within the TFDC) associated with each drive unit. These attention bits are position-coded in bits 8-11 of drive status word W0. The TMS 9900 sets the attention bit to indicate that the selected drive has a condition that may require attention by the 990 processor. If the attention bit associated with a given drive goes active, and the corresponding attention mask bit is set, an interrupt is generated when the TFDC returns to the idle mode.

The independent overlapped seek capability of the TFDC is a typical example of the use of the attention mask and the attention bits. The 990 processor may, for example, command drive 3 to seek to track 46 and may also enable the operation complete interrupt. The TFDC initiates the seek, and returns to the idle mode, generating an interrupt. The drive 3 attention bit goes inactive when the physical seek starts. After determining that this is a TFDC operation complete interrupt, the 990 processor sets the unit 3 attention mask bits. While the seek is still in progress, the 990 processor may initiate an operation to another drive. When the seek completes, the attention bits are updated and an attention interrupt is generated (controller idle). Notice that an attempt to set the attention mask bit in the same control words that start the seek will cause a premature interrupt. This is because the attention bit is high until the drive starts an operation.

The TFDC interrupt output is wired from P2-66 of the chassis slot location to interrupt level jumpers. It is wired from there to the assigned interrupt level input of the processor board (chassis slot 1). The TFDC interrupt competes for 990 processor attention with interrupts from other slot locations. These are vectored interrupts, with priorities assigned (by jumpers) to each slot. Interrupt masks (in the 990 status register) control which levels are serviced.

The existence of the active TFDC interrupt is not enough information for the 990 processor to determine the cause of the interrupt. The 990 processsor must read back the controller status word, W7. If the contents of W7 indicate a unit error, or if the 990 processor has previously issued a seek command, the 990 processor must also read back the drive status word, W0.

If interrupt enable was set in W7, the interrupt indicates a return to idle. The 990 computer should turn off the interrupt enable when setting up a Seek operation.

2.6.7.2 Interrupt Logic. Refer to Figure 2-51, which shows the attention mask register, idle status register, and 990 interrupt generation gates. The register file bus provides four-bit inputs to the attention mask register and the idle status register.

The attention mask is loaded into the attention mask register as part of the slave write operation that loads control word W0 into the TFDC. The control word from the 990 computer is gated from the TILINE line receivers to the register file bus. The TILINE I/F control logic recognizes (from the register file address) that control word W0 is on the register file bus. W0 is loaded into the register file, and then the lower 4 bits (12-15) are loaded into the attention mask register.

The register file is clocked by RFCLKA-, and the attention mask register is clocked by the attention mask clock, ATMCLK-. These clocks are generated during successive states 1A and 1B of the TILINE I/F control logic. The ATMCLK- pulse coincides with the CLK3- pulse. Refer to the TILINE I/F control logic description for information on the sequence of states in a TILINE or register file bus operation.

The 9900 control program has no requirement to read or modify the attention mask. The program does control generation of the attention bits (AT0-3) via CRU output from the microprocessor to the TMS 9901 PIA. If the attention mask bit associated with a drive is set and the attention bit for the same drive goes high, INTA goes high. INTA goes to the CRU input multiplexer as a status bit (for self-test purposes) and partially enables the 990 interrupt. If the TFDC is idle, TLINT- goes active, interrupting the 990 processor. If the TFDC is not idle, INTA remains active (unless the control program drops the attention bit) and TLINT- is generated the next time the TFDC goes idle.

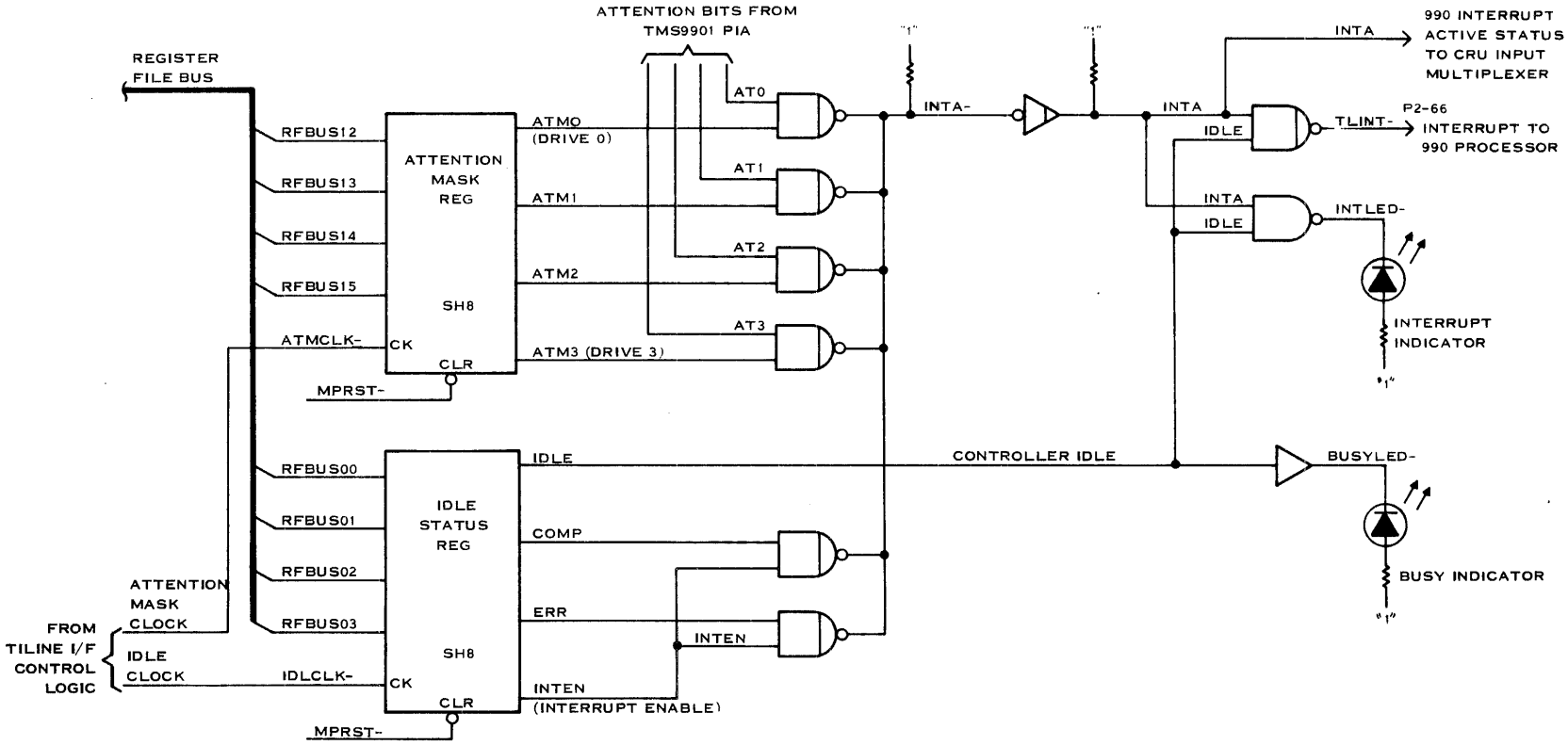


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Figure 2-51. Attention Mask Register, Idle Status Register, and 990 Interrupt Generation

The idle status register contents may be loaded with bits 00-03 of control word W7. Control word W7 is loaded into the TFDC by a slave write operation as the last part of the operation setup. W7 must be the last control word sent to the TFDC because W7, bit 0 (idle/busy) is the control bit that forces the TFDC out of the idle loop to execute an operation.

The control word from the 990 computer is gated from the TILINE line receivers to the register file bus. The TILINE I/F control logic recognizes (from the register file address) that control word W7 is on the register file bus. All 16 bits of W7 are loaded into the register file. Then the upper 4 bits (RFBUS00-03) are loaded into the idle status register. The register file clocks (RFCLKA-, RFCLKB-) and the idle status register clock (IDLCLK-) are generated during successive states 1A and 1B of the TILINE I/F control logic.

The idle status register is updated during the course of a TFDC operation by the 9900 control program. The control program updates the status bits with a Set Zeros Corresponding (SZC) or a Set Ones Corresponding (SOC) instruction. SZC and SOC instructions involve two memory bus operations. First, the microprocessor reads the contents of the specified location. For an SZC or SOC addressed to the register file, the TILINE I/F control logic goes through a microprocessor read to register file cycle, states 08-0A. The TMS 9900 masks the word from the register file against the operand of the SZC/SOC instruction to generate the altered word. The microprocessor then initiates a write to register file cycle to restore the word with the specified bits updated. The TILINE I/F controller loads the register file in state 0B and, recognizing the SLVWD7 address, loads the idle status register in state 0C. This read-modify-write cycle allows selective update of any of the status bits.

W7, bit 3 is the interrupt enable bit. The 990 computer sets this bit to enable the TFDC to generate an interrupt upon normal or error completion. This bit does not affect the attention interrupts. W7, bit 3 is loaded into the idle status register as INTEN. With INTEN high, INTA goes active when the microprocessor sets either COMP (normal completion) or ERR (error completion). The interrupt to the 990 processor (TLINT-) is enabled when the TFDC returns to idle and sets the idle/busy bit. The idle/busy bit is stored in the idle status register as IDLE.

2.6.7.3 INT and BUSY Indicators. The INT (interrupt) and BUSY indicators are light-emitting diode (LED) devices mounted adjacent to the board ejection tab. An LED lights when a logic 0 is placed on the cathode by the NAND driver. The anode is hardwired to logic 1 with a resistor to the + 5 volt supply.

The INT driver is connected in parallel with the TLINT- driver. The LED remains lit from the time that the 990 interrupt is generated until the interrupt is cleared by the 990 sending a new W7 control word. The INT LED appears dimly lit during periods of heavy disk activity. The LED flash may be too fast to detect during a single, isolated operation. If the LED burns brightly, the controller is "hung" with an unserviced active interrupt.

The BUSY indicator is driven from the IDLE output of the status register through a noninverting driver. The busy condition is the complement of the idle condition, and the indicator lights when the IDLE is low. The 990 interrupt is disabled while the BUSY indicator is lit. The BUSY indicator appears dimly lit during periods of heavy disk activity. If the BUSY indicator appears brightly lit, the controller is either being heavily used or is hung in an indefinite delay.

2.6.8 9900 Control Program Organization

The 9900 control program controls, directly or indirectly, all of the TFDC operations based on control words W0-W7 and inputs from the TILINE and drive units. The control program runs whenever power is applied to the TFDC, although operations may be temporarily suspended (MPREADY low) during data transfers over the TILINE or drive interface. The control program is burned in ROM storage occupying the first 4K word addresses of the TMS 9900 address space (CPU byte addresses 0000-1FFE). Workspace register and general scratchpad storage for the control program is provided by the 256-word RAM (CPU byte addresses 8000-81FE).

The 9900 control program stored in the ROM is in the form of 9900 machine language instructions. This binary machine language program was generated from a 9900 assembly language source program. The control program is documented by flowcharts (Appendix A) and by the assembly language listing (Appendix B) produced by the DX10 assembler program, SDSMAC.

The assembly language listing is much easier to follow than the equivalent machine language high-low listing. The assembly language listing includes symbolic addresses (statement labels) and comments that describe program operation and clarify program organization. In addition to the labels, instruction mnemonics, and operand fields of the assembly language source program, the listing includes the output CPU byte address and machine language instructions (in hexadecimal form).

The 9900 control program is divided into five interrupt service routines, thirteen command processor routines, and a pool of service subroutines. Each routine/subroutine is identified by a five- or six-letter mnemonic, as summarized in Table 2-24. The mnemonic is a label that appears in the assembly language listing of the program and serves as an entry point to the routine/subroutine. Some routines have more than one entry point. For example, the read data and read delete command processor has one entry point (REDENT) for the normal-mode Read Data command and a separate entry point (RDDENT) for the extended mode Read Delete command.

Table 2-24. Mnemonics for Control Program Routines and Subroutines

Mnemonic	Routine/Subroutine Name
ABTCHK	Command abort subroutine
CIMENT	MFM check ID subroutine
CIFENT	FM check ID subroutine
CMDENT	Command decode (idle interrupt service)
DITENT	Disk interface test*
DLYENT	Diagnostic delay*
DSOENT	Data separator overrun interrupt service
DSTENT	Data separator test*
ESTENT	Extended self-test*

Table 2-24. Mnemonics for Control Program Routes and Subroutines (Continued)

Mnemonic	Routine/Subroutine Name
FILENT, FMTENT	Format command (Extended entry = FILENT) (Normal entry = FMTENT)
FMTWAT	Data separator shift register word count loop
HDTEST	Drive head test*
HOMENT	Home-in subroutine (for IBM diskettes with bad tracks)
IDLENT	Idle routine
IFTEST	Extended disk I/F test*
INQTYP	Inquire type subroutine
INTENT	TILINE interrupts test*
MPTENT	9900 MPU test*
MPTENT	9900 MPU test*
MSTENT	TILINE master/slave test*
PITENT	PIA 9901 test
POSENT	Drive positioning subroutine
PWRENT	Reset interrupt service
RATENT	RAM test*
RCMENT	Read controller memory
RDDENT, REDENT	Read delete (delete data mark) Read data (normal data mark)
RESENT	Restore command
RIDENT	Read ID command
ROTENT	ROM test*
RUFENT	Read unformatted
SEKENT	Seek command
SEKS00	Seek setup routine
SLTENT	Slave test*
STPENT	Process unit subroutine

Table 2-24. Mnemonics for Control Program Routines and Subroutines (Continued)

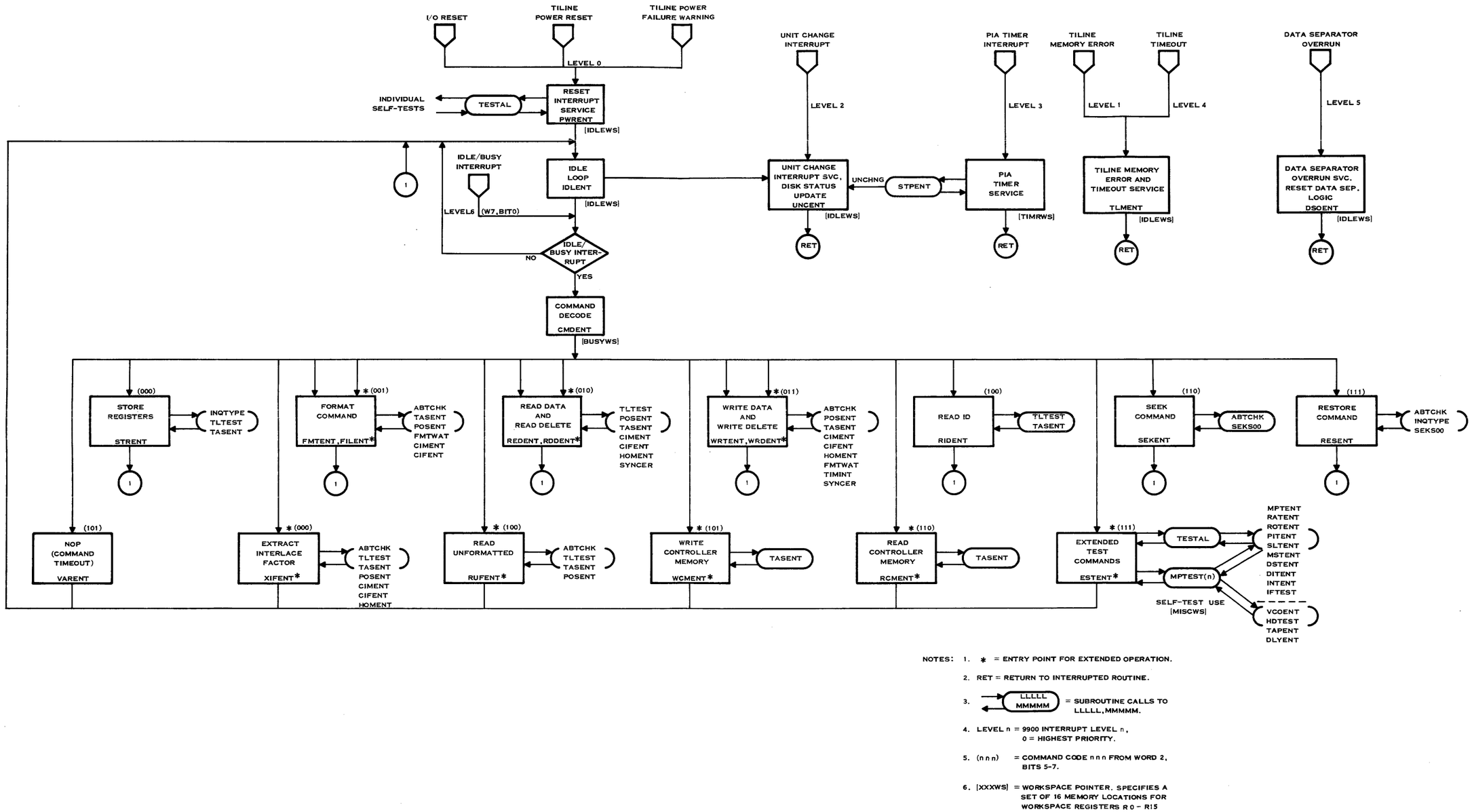
Mnemonic	Routine/Subroutine Name
STRENT	Store registers
TAPENT	Tap test*
TASENT	TILINE address setup
TESTAL	Full self-test*
TLMENT, TLTENT	TILINE memory error, TILINE timeout interrupt service
TLTEST	TILINE test subroutine
TMENT	Timer interrupt service
UNCENT	Unit change interrupt service
VCOENT	VCO adjust test*
WCMENT	Write controller memory
WRTENT, WRDENT	Write data (normal data mark entry) Write delete (delete data mark entry)
XIFENT	Extract sector interlace factor

Note:

* Self-test routine. See Section 3

Refer to Figure 2-52, the principal flowchart of the 9900 control program. There are three non-maskable level 0 interrupts, the I/O reset interrupt, power failure warning interrupt, and the power reset interrupt. Any of these interrupts initiates a hardware microprocessor reset (MPRST-). An interrupt vector at address 0000 directs execution to the reset interrupt service routine (PWRENT) when the external reset is removed.

All other interrupts are maskable and are encoded by the TMS 9901 PIA for input to the TMS 9900 microprocessor. All of the maskable interrupts except the level 3 PIA timer interrupt are the result of external interrupt signals that are latched and wired to the PIA interrupt inputs. The level 3 PIA timer interrupt is generated within the PIA at the expiration of a previously specified programmable interval. Refer to the TMS 9901 PIA description for additional information.



NOTES:
1. * = ENTRY POINT FOR EXTENDED OPERATION.
2. RET = RETURN TO INTERRUPTED ROUTINE.
3. LLLLL / MMMMM = SUBROUTINE CALLS TO LLLLL,MMMMM.
4. LEVEL n = 9900 INTERRUPT LEVEL n, 0 = HIGHEST PRIORITY.
5. (n n n) = COMMAND CODE n n n FROM WORD 2, BITS 5-7.
6. [XXXWS] = WORKSPACE POINTER. SPECIFIES A SET OF 16 MEMORY LOCATIONS FOR WORKSPACE REGISTERS R0 - R15

Figure 2-52. 9900 Control Program Principal Flowchart

After power is applied and the PWRENT interrupt service routine has finished, control program execution moves on to the idle loop, IDLENT. The program continues to loop on idle until the TFDC is commanded out of the idle mode by a control word W7 with bit 0 = 0. Notice that the loading of control words into the TFDC (by TILINE slave write operations) does not require any control program action until the idle/busy interrupt.

Each of the register file addresses associated with storage of the control words is assigned a symbolic address, SLVWD0-7. The command decode routine examines the extended mode bit (bit 0) and the command code (bits 5-7) stored in SLVWD1 to select the appropriate command processor from a table of command processor entry points.

On the flowchart, the command code associated with a particular command processor routine is shown in parentheses at the top of the operation block. Extended mode operations are identified by an asterisk (*). Some of the extended mode operations have a dedicated command processor, such as the extract interlace factor processor, XIFENT. Other extended operations are very similar to the corresponding normal mode operations and share a command processor routine by using a different entry point.

The format commands, read commands and write commands share processors between normal and extended mode operations. Both entry points are shown on a shared processor routine. An extended mode entry point is identified by an asterisk such as WRDENT*. It is important to note that the asterisk is used only for clarity on the flowchart and does not appear in the program listing.

Refer to the command word descriptions in Section 1 of this manual for detailed information on control words W0-W7 and the command codes in W1.

Each command processor routine (except the NOP "processor") calls one or more service subroutines from the subroutine pool. The subroutines perform such common functions as setting up the TILINE address in the TILINE address register/counter, positioning the read/write heads, checking MFM or FM sector ID fields, or testing TFDC functions. An oval outline is used to identify the subroutines on the flowchart. If a processor routine calls so many subroutines that the names cannot fit in a closed oval, only the curved ends of the oval are shown.

TESTAL is a subroutine that calls all of the normal mode self-tests from the pool of available self-test subroutines. TESTAL is called as part of the reset interrupt service routine, PWRENT, and may also be called by the extended self-test command processor, ESTENT. Individual self-tests may be called up by MPTEST(n), where n is provided right-justified in control word W3. Error codes are returned to the 990 computer in the right byte of W2, in the same manner as for TESTAL. Some special purpose self-tests, such as the VCO adjustment test, are accessible only by number and not by TESTAL. Additional information on TFDC self-test capabilities is provided in Section 3 of this manual.

Table 2-25 contains a brief summmary of each control program routine or subroutine with the exception of self-test routines. Each summary includes an overall description of the routine/subroutine function, a list of workspace register assignments (including mnemonics for the major variables), and a list of subroutines called. If the routine/subroutine has error or status reporting capability, these outputs are listed. These summaries are extracted from the lengthy assembly language listing and are combined here for convenience.

Self-test routines are described in Section 3.

Table 2-25. Control Program for TFDC Operation

```
*************************************************************
    PWRENT - Reset interrupt service

    This routine is entered on power up, I/O reset,
    or power failing pulse. It functions to abort
    any operation already in progress and then to set
    all sections of the logic into a safe condition.
    A complete self-test is performed on the micro-
    processor, ROM, RAM, PIA, slave interface, TILINE
    master and slave, data interface, disk control/status
    interface, and TILINE interrupt logic.
    After self-tests are successful, all
    controller RAM parameters are initialized to their
    default values and control is passed to the idle
    routine.

    Subroutines called:
         TESTAL        Controller self-test

    Status reported:
         Abnormal completion  (power up or I/O reset)

*************************************************************
    ABTCHK - Command Abort Subroutine

    This subroutine is called by all commands which select
    the disk drives. It checks for the command inhibit
    flag which is set on power-up, I/O reset, etc.
    This flag is cleared only after successful completion
    of the full self-test. If the flag is still set when
    this routine is called, 'FF' is written into the right
    byte of W7 and the command is aborted to
    the Idle routine. Commands requiring data transfer to or
    from the disk are also checked for an appropriate
    head value.

    Errors reported:
         Cmd timeout          Head value invalid
                              from data transfer command
                              parameters
         'FF' in SLVWD7       Indicates self-test failed,
                              cannot execute this command


*************************************************************
    IDLENT - Idle Routine

    This section prepares the slave words and
    internal interrupts for controller idle mode  It
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    then enters an idle condition during which
    timer and unit change services are performed.
    When the host CPU sets the idle bit in
    W7 to zero, a busy interrupt will switch
    the controller into the command processing mode.

    A command trace log is also stored in RAM locations
    8140-81FE (up to 12 commands) each time this routine
    is entered from the command just processed. This
    provides a trace of all slave register contents
    from the last 12 commands processed since a reset.

     Note: The idle, op complete, and error bits are not logged.
           Errors must be interpreted from bits in W7 and W0.
           Because the host might write over the registers once
           idle is set,  the trace option may be
           software-inhibited by writing into RAM location >80CC
           with zeros after power-up or I/O reset (e.g., for use
           of that RAM for a user-defined program).

    Subroutines called:
         UNCHNG        Drive status update routine

    Errors reported:
         Error bit in W7    If any of right byte non-zero
         Drive unsafe       If disk change status on drive

*************************************************************
    CMDENT - Command Decode

    This is the entry for all command processing.
    It shall be activated by the host CPU writing to
    W7 with a zero in the idle bit, which
    causes a busy interrupt of the idle controller.
    This routine modifies the controller mode by setting
    the timer to the command mode.  It then decodes the
    command in W1 to select the appropriate
    command routine.

    Errors reported:
         None               See ABTCHK

*************************************************************
    STRENT - Store Registers        (Cmd code = 0)

    This routine transfers to memory up to three words
    that describe the characteristics of the diskette
    installed in the specified unit. The words trans-
    fered contain the following data:

    Bit: 0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
   Word
    1   [     words/track    (FM=>680,    MFM=>EA0)        ]
    2   [ sectors/track =>1A    ][    overhead/track =0   ]
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    3   [  heads/cyl  ]I      cylinders/drive = >4D     ]

    Subroutines called:
         INQTYP        Check drive status for double density
         TLTEST        Test TILINE read/write I/F
         TASENT        TILINE address setup

    Errors reported:
         None*         TILINE memory error may be reported
                       from TLTEST

*************************************************************
    TLTEST - TILINE Master Cycle Test Subroutine

    This test is accessed by branch and link from any of
    the command routines that  must use the TILINE I/F
    for data transfers to the TILINE memory (read operations).
    A's and 5's are written to the
    TILINE address specified in W5 and W6.  A TILINE
    read without master cycle verifies the data written.
    Any errors are reported as a memory error in W7.
    If an error is detected, a BLWP is performed to idle.

    Subroutines called:
         TASENT        TILINE address setup

    Errors reported:
       Memory error    Failure of TILINE read/write test

*************************************************************
    TASENT - TILINE Address Setup Subroutine

    This subroutine converts the 21-bit byte address
    passed in the slave registers ( words 5 and 6 )
    into a 20-bit TILINE word address.  It then loads
    this value into the TILINE address counters.

*************************************************************
    XIFENT - Extract Sector Interlace Factor   (Ext cmd code = 0)

    This command is an extended maintenance command
    provided to allow an operator to determine the
    interlace factor (displacement of consecutive
    logical sectors around a track) of a previously
    formatted diskette.

    This command begins by getting the unit and cylinder numbers
    specified by the user.  After positioning the desired
    drive head to the specified track, the firmware completes
    a TILINE I/F test and sets up the TILINE address for
    transferring the interlace factor.  Next it completes
    an ID check for sector 0 (sector 1 for FM).  When the ID
    check returns with a good check, the firmware increments
    the sector number and goes to the check ID routine again.
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
For each wrong sector return from check ID
(within the timeout limits per sector), the interlace
factor count is incremented by 1. Any sync errors
reported will be retried within the allotted timeout
period (if a timeout occurs, the ID retry count is
decremented and the firmware goes back to find sector 0
again, reinitializing the interlace factor to 1). When a
good ID check is finally returned for the second sector,
the interlace factor count is written to the specified
TILINE address.

Subroutines called:
     ABTCHK        Check command inhibit flag (errors
                   include: FF in right byte of W7)
     TLTEST        TILINE I/F test
                   (errors include: TILINE memory error)
     TASENT        TILINE address setup
     POSENT        Command head positioning routine
                   (errors include: UE, OL, NR, SI)
     CIMENT        MFM check ID
     CIFENT        FM check ID
     HOMENT        FM positioning home-in subroutine
                   (errors include: UE, SI)

Errors reported:
     Unit error (UE)   Invalid unit number, unreported drive
     Seek
     incomplete (SI)   Wrong cylinder number for MFM, seek
                       out of bounds
     ID error          Retries used up while searching for
                       1st or 2nd sector.

************************************************************
    FMTENT
    FILENT - Format Command          (Cmd code = 1)

    The Format command writes a full track format on
    the specified disk. Options include interlaced sector
    placement according to a factor passed by the user,
    FM or MFM recording (determined by disk type), and
    a 16-bit data word value passed by the user to be
    written in all data fields on the track.

    The Extended Format command provides interlaced sector
    capability using a factor (from 1 to n-1 sectors)
    read from the TILINE address following the  specified
    location of the data word for use in the data fields.

    On entry to the format routine, a flag is set to indicate
    whether interlaced sectors are desired. Next, the
    TILINE address for the user-specified data is fetched
    and the data word is saved. If the interlaced sector
    flag is set, the controller then fetches the user-
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
specified factor.

A table is then prepared in RAM with the logical
sector number sequence for formatting the track. Next,
command parameters and disk status are checked. Then
the controller seeks to the specified physical track
and does a surface evaluation. Finally, the track is
formatted and then verified. Errors from the surface
analysis and the format verification are reported as
data errors.  However, the track is formatted anyway.

Subroutines called:
     ABTCHK       Check for command inhibit flag (errors
                  include: FF in right byte of W7)
     TASENT       TILINE address setup
     POSENT       Command head positioning routine
                  (errors include: UE, OL, US, NR,
                  and Si)
     FMTWAT       Read/write word delay for gaps
     CIMENT       MFM check ID
     CIFENT       FM check ID

Errors reported:
     Command
     timeout      Illegal interlace factor, data separator
                  overrun, wrong side selected on FM
                  diskette, timer interrupt in data
                  field (drive still ready)
     Unit Error   invalid unit number, drive unreported, write
     (UE)         protected diskette, drive not ready

     Data Error   Surface analysis error (4 retries)
                  data field CRC error (5 retries),
                  data compare error in verification
     ID error     False syncs (1K retries nom), timeout on
                  ID syncs (106 retries), wrong cylinder read
                  (106 retries), wrong sector information (106
                  retries)
     Search       Timeout on data mark (5 retries) or
     error        data mark wrong (5 retries)

Note: Retries are initialized before the surface analysis
      and before each sector verification. Good
      ID checks also reinitialize ID and sync retries,
      while wrong sectors from the ID check only reinitialize
      sync retries. Data error retries may be
      forced to zero by making RETRYK = -1, then ID
      retries = 26.

*****************************************************
POSENT - Position Subroutine

This subroutine positions the specified unit to the
specified cylinder, allowing overlapping of stepping
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    by other already active units. Upon successful
    completion, the head will be loaded and ready for
    data transfer.

    Subroutines called:
         SEKSOO        Seek set up subroutine
                       (errors include: UE, SI, NR)

    Errors reported:
         Unit error    Drive not ready, off line, unsafe,
                       or seek incomplete
         Not Ready     Temporary while head unloaded
         (NR)
**********************************************************
    CIMENT -  MFM Check ID Subroutine

    This subroutine is called by branch and link from any
    of the diskette read/write command routines. It puts
    the data separator in the read mode and checks the
    ID field from the address mark (AM)
    through the CRC word.

         Returns:
            False sync (compare error on AM, CRC, or ID3)
            Good return
            Wrong cylinder (compare error on ID1, CRC ok)
            Wrong sector (compare error on ID2, CRC ok)

**********************************************************
    CIFENT -  FM Check ID Subroutine

    This subroutine is identical to the MFM check ID
    subroutine except for the compare value for the AM
    (and lack of ID3). Entry conditions and returns are
    identical to the MFM version.

**********************************************************
    RDDENT, REDENT -
    Read Data and Read Delete    (Cmd code = 2)

    These commands check for illegal command parameters,
    test the TILINE, position the drive to the selected
    cylinder, check ID fields until the specified
    sector is reached, and then transfer data to the TILINE
    until the TILINE word count is depleted. During this
    operation various error conditions may cause retries
    to occur. If the end of a sector is reached with a
    nonzero TILINE word count, the next sequential
    logical sector is found and data transfer continues.

    If the last logical sector of a track is completed
    and the word count is nonzero, and if the diskette is
    double-sided (and therefore MFM), and the current
    head is head 0 , then head 1 is selected and reading
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    is continued on the first logical sector. If the
    last logical sector of a track is completed on
    head 1 of a double-sided diskette or side 0 of a
    single-sided diskette
    and the word count is still nonzero, the drive
    is stepped to the next logical cylinder (skipping
    bad tracks in FM mode) and reading is continued on
    the next logical track.

    Subroutines called:
         TLTEST        TILINE I/F test
                       (errors include: TILINE memory error)
         POSENT        Command head positioning routine
                       (errors include: UE, NR, US, OL,
                       and SI)
         TASENT        TILINE address setup
         CIMENT        MFM check ID
         CIFENT        FM check ID
         HOMENT        FM positioning home-in routine
                       (errors include: UE, SI)

    Errors reported:
         Command
         timeout       Illegal sector number, data separator
                       overrun during check ID,
                       illegal head number for FM
         Unit error    Unreported drive, invalid unit number,
                       seek incomplete
         Seek
         Incomplete    ID1 wrong from check ID (MFM only)
         Rate error    Data separator overrun
         Data error    Data field CRC error
         ID error      Sync error (1K retries), wrong sector number
                       (106 retries)
         ID & data     FM: delete data mark detected in regular read or
                       or regular data mark detected in read delete
         Search
         Error         Data mark error

    Note: Retry counts for ID and data errors are the
          same as for format (106/1K and 5 nominal)

************************************************************
    HOMENT - Home-In Subroutine

    This subroutine is used by the read and write
    routines to reposition the heads on a FM diskette
    after finding that the cylinder read from the
    ID fields on a track do not match the desired
    track.  This can occur because of a drive stepping
    error, but will generally be experienced due to
    having crossed a bad track as defined by IBM
    format.  This subroutine assumes that the cylinder
    value as found in the ID is passed in R0. This
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
     home-in is effected by adjusting the disk logical
     position value to allow the positioning routine
     to move the heads toward the desired track.

     Errors reported:
          Seek          Failed to find desired
          incomplete    cylinder in 6 retries
          and           (Retries may be reduced to 0)
          Unit
          Error

*************************************************************
     WRTENT, WRDENT
     Write Data and Write Delete   (Cmd code = 3)

     These commands check for illegal command parameters,
     position the drive to the selected cylinder, check
     ID fields until the specified sector is reached, and
     then transfer data from the TILINE
     to the drive until the TILINE word count is depleted.

     Various error conditions may cause retries to occur
     during an operation. If an end of sector is reached
     with a nonzero TILINE word count, the next sequential
     logical sector is found and data transfer continues.

     If the last logical sector of a track is completed
     and the word count is nonzero for a double-sided
     (MFM) diskette, and the current
     head is head 0, then head 1 is selected and writing
     is continued on the first logical sector.

     If the last logical sector of a track is completed on
     head 1 of a double-sided diskette or side 0 of a
     single-sided (FM) diskette
     and the word count is still nonzero, the drive
     is stepped to the next logical cylinder (skipping
     bad tracks in FM mode) and writing is continued on
     the next logical track.

     Subroutines called:
          ABTCHK        Check command inhibit flag (errors
                        include:  FF in right byte of W7)
          POSENT        Command head positioning routine
                        (errors include: UE, NR, US, OL,
                        and SI)
          TASENT        TILINE address setup
          CIMENT        MFM check ID
          FMTWAT        Data I/F word boundary wait routine
          TIMINT        Timer service between sector ID checks
                        (this routine may modify: NR, US,
                        OL, WP, and SI)
          CIFENT        FM check ID
          HOMENT        FM head position home-in routine
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
                    (errors include: UE, SI)

    Errors reported:
         Unit error    Invalid unit number, drive unreported,
                       diskette write protected, seek incomplete
         Command       Illegal sector number, timeout in data
         Timeout       field, data separator overrun in ID field,
                       illegal head number (FM)
         Seek
         Incomplete    ID1 compare error (MFM)
         ID error      ID2 compare error (106 retries nom)
                       sync error (1K retries)
         Rate error    data separator overrun

**********************************************************
    RIDENT - Read ID Command       (Cmd code = 4)

    This command transfers to TILINE memory up to
    Three words that are exact images of the ID that
    would be read from an actual hard disk.  The drive is
    not accessed to execute this command.  The
    format of these words is as follows:

    Bit  0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
  ------------------------------------------------------
  WD0  = [     head #    ][       cylinder #             ]
  WD1  =  0  0  0  0  0  0  0  1 [     sector #           ]
  WD2  = [       words/sector  (FM=64, MFM=144)           ]

    Subroutines called:
         TLTEST        TILINE I/F test
                       (errors include: TILINE memory error)
         TASENT        TILINE address set up

    Errors reported:
         Unit error    Invalid unit number, drive unreported
         TILINE
         timeout       TILINE timeout during data transfers

**********************************************************
    RUFENT - Read Unformatted        (Ext cmd code = 4)

    This routine allows reading of a specified number of
    words on a desired track without checking for CRC
    errors.

    The user specifies which sector number to begin reading.
    Once a valid address mark is read, the second word in
    the ID field is read and compared with the desired
    sector number.  If this ID2 word is not the desired one,
    a retry count is decremented and the search is restarted.

    Once the desired sector is found, the controller
    begins writing the specified number of words
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    from diskette to TILINE (at the address specified in
    W5 and W6).

    Note: By entering an invalid sector number in the
          in the command, the unformatted read will bypass
          the sector number check and begin reading
          after the first valid address mark.

          If no valid address mark is found, the controller
          returns an ID error status. If the desired sector
          is not found in 128 retries (nominal), a search
          error is reported.

    Subroutines called:
         ABTCHK       Check command inhibit flag (errors
                      include: 'FF' in right byte of W7)
         TLTEST       TILINE I/F test
                      (errors include: TILINE memory error)
         POSENT       Command head positioning routine
                      (errors include: UE, NR, OL,
                      and SI)
         TASENT       TILINE address set up

    Errors reported:
         Command
         timeout      Data separator overrun, too long
                      in reading**
         Unit error   Invalid unit number, drive unreported
         ID error     Timeout on syncs (1K retries),
                      AM compare error (106retries)
         Search error ID2 compare error (106 retries)

    Note: **The controller will timeout after 348 milliseconds
          of reading unformatted data (2+ revolutions) and
          report command timeout. This timeout applies
          only after the desired sector has been found.

**********************************************************
    WCMENT - Write Controller Memory     (Ext cmd code = 5)

    This command transfers data from TILINE memory
    to the controller memory space, starting at the
    address specified in W3  The number of
    words to transfer is passed in W4.


    Subroutines called:
         TASENT   TILINE address setup

**********************************************************
    RCMENT - Read Controller Memory      (Ext cmd code = 6)

    This command transfers data from the on board
    memory space to external TILINE memory. The address
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
    is passed to the controller in W3 and the
    number of words to transfer in W4.


    Subroutines called:
         TASENT        TILINE address setup

**********************************************************
    SEKENT - Seek Command              (Cmd code = 6)

    This command checks the validity of the cylinder
    value passed by the host CPU and if not valid
    returns seek incomplete error status.
    The seek setup subroutine is called to set up
    the disk parameters to reflect distance of the
    seek and direction (DSKDIF) and enables eventual
    settling of the heads (DSKSTL). Then control is
    passed to the idle routine.

    Subroutines called:
         ABCHK3        Check command inhibit flag (errors
                       include: 'FF' in right byte of W7
         SEKS00        Seek setup
                       (errors include: SI, UE, NR)

    Errors reported:
         Unit error    Invalid unit number, drive unreported

**********************************************************
    SEKS00 - Seek Setup Subroutine

    This subroutine sets up paramaeers for use by STPENT
    in positioning drive heads to the desired cylinder.

    Errors reported:
         Drive
         not ready     Temporary til seek completed
         Seek
         incomplete    Disk head position unknown, illegal
                       cylinder number illegal or resulting
                       physical position illegal when logical
                       position off due to bad seeks or
                       FM bad tracks
         Unit error    Unit busy, seek incomplete

    Status bits cleared:
         Attention     Seek operation in progress

**********************************************************
    RESENT - Restore Command           (Cmd code = 7)

    This command inquires about disk type, allowing
    clearing of the unsafe condition. It then sets up the
    timer parameters of the drive to restore the heads
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
     to track 0.

     Subroutines called:
          ABCHK3        Check command inhibit flag (errors
                        include: 'FF' in right byte of W7
          INQTYP        Get diskette type if unreported
                        (this routine may reset unsafe)
          SEKS00        Seek setup
                        (errors include: NR, UE, SI)

     Errors reported:
          Unit error    Drive unsafe, off line, or seek
                        incomplete after INQTYP call

     Status bits cleared & why:
          Seek
          Incomplete    Indicates restore command initiated

*************************************************************
     INQTYP - Inquire Type Subroutine

     If the drive type is currently unreported this
     subroutine will
     select the command unit, determine current type,
     and reset unsafe drive status if drive is ready.

     Subroutines called:     None

     Errors reported:
          Unsafe(reset)      Unsafe is reset if drive was
                             previously unreported and is now
                             ready (as after disk change)

*************************************************************
     TLMENT, TLTENT
     TILINE Memory Error and Timeout Interrupt Service
        . .                    (interrupt levels 1, 4)

     This interrupt service is activated by a TILINE
     memory error or timeout detected in a TILINE
     cycle. The interrupt flag is cleared, TILINE memory
     error status or TILINE timeout status as appropriate
     is  placed in W7, and program
     control is returned to the TILINE error return.
     This error return is displaced one word below
     the timing error return
     specified in R9 of the interrupted program.

     Errors reported:
          TILINE
          Timeout       Interrupt occurred, TLTO CRU bit = 1

          TILINE
          memory

          error         Interrupts occurred, TLTO not set
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
*************************************************************
    UNCENT - Unit Change Interrupt Service
                                    (Interrupt level 3)

    This routine updates the disk status value in
    W0 and derives a new encoded unit value
    from the bit value in W6. It is
    actuated by a unit change interrupt when the
    host CPU writes into W6 (possibly
    changing units) or may be called as a service
    any time disk status update is required.


*************************************************************
    TMENT - Timer Interrupt Service      (Interrupt level 3)

    This routine provides the services of timing the
    stepping, settling, and head loading and unloading
    of up to four disk drives in an independent manner.
    It also keeps track of the current status of the
    individual drives including drive type, on-line
    status, and disk change status.

    When not used in the stepping mode, this routine
    provides a timeout function to allow the micro-
    processor to escape from a "not ready" wait condition
    while waiting for address mark sync, or while
    transferring data.

    Subroutines called:
         STPENT        Unit multiple step process subroutine
                       (this routine may modify: NR, CL,
                       WP, unsafe, SI)
         UNCHNG        Current unit status update

*************************************************************
    DSOENT - Data Separator Overrun Interrupt Service
                                    (Interrupt level 5)

    This interrupt service is activated by a data
    interface overrun condition, indicating loss
    of data to or from the drive. This shall occur
    if the microprocessor is not able to maintain
    the data rate of the disk interface. Processing
    shall be returned to a designated "data overrun"
    entry in the interrupted program.  The data overrun
    entry shall equal the old workspace register 9
    value plus 4.

*************************************************************
    STPENT - Process Unit Subroutine

    This subroutine processes a disk unit by determining
```

Table 2-25. Control Program for TFDC Operation (Continued)

```
        if head load is appropriate, selecting the drive,
        interrogating disk status (updating drive status
        word), issuing a step command as necessary, and
        waiting for the head to settle if all stepping is
        complete.

        Errors reported:
             Not ready     Temporary while head not loaded or
                           not settled,
                           reset when head loaded and settled and
                           drive on-line
             OL and NR     Drive not ready
                           (off-line is reset when drive ready)
             Unsafe        Drive unreported or disk change set
             Seek
             Incomplete    Desired track = 0, steps complete but
                           TRK00 status from drive not set
             Write
             protect       Write protect status from drive set
                           (reset when WP bit not set)
*************************************************************
```

2.7 DISK INTERFACE

The disk interface logic performs those functions that are directly involved in transmitting data to a drive unit for recording and retrieving data previously recorded on a drive unit. These functions include:

- Selecting the drive unit for the operation
- Transferring control signals to the selected drive unit
- Accepting and transferring drive status and diskette sector address information
- Converting parallel data to serial form, encoding in FM or MFM format, and transmitting data to the selected drive unit
- Separating serial clock and data in either FM or MFM format and converting data to parallel form for transfer to 990 main memory
- Error checking of data and sector ID information read from the drive unit

Disk interface operations are initiated and controlled by the 9900 control program via the TMS 9900 microprocessor. Control outputs to the disk interface logic are generated by the 9900 address decoding logic, PIA outputs, and the data separator control register. Control functions from the address decoding logic are activated by reference to reserved memory locations in the 9900 address space. The PIA and the data separator control register are CRU devices, so those control outputs are activated by CRU instructions.

The TMS 9900 microprocessor performs such functions as reading drive status and data separator status, and controlling data transfer. The microprocessor develops sector identifiers and track format patterns to format the diskette and checks the sector identifiers during read and write operations. However, read and write data transferred between 990 main memory and the drive does not pass through the TMS 9900.

The write data path goes from the 990 main memory over the TILINE bus, register file bus, through a one-word buffer in the register file, over the register file bus, the microprocessor data bus to the data shift register, through the write data encoding logic to the drive interface line drivers.

One TILINE master read cycle is required to get the data from the 990 main memory to the register file. A microprocessor read register file operation, initiated by the microprocessor and executed by the TILINE interface controller, reads the data back onto the register file bus. The address decoding logic gates the data onto the microprocessor data bus, and the shift register load command is issued from within the data separator. This entire operation is performed during a single 9900 memory-to-memory move (MOV) instruction. The arguments of the MOV instruction are a symbolic address for the desired word in 990 main memory and a symbolic address for the data separator shift register.

The read data path goes from the drive interface line receivers into the data separator, through the data shift register to the microprocessor data bus, over the register file bus to a one-word buffer in the register file, then over the register file bus, over the TILINE to 990 main memory. The shift register output is gated onto the microprocessor data bus by a signal from the address decoder. The data is stored in the register file by a microprocessor write register file cycle initiated by the TMS 9900 and executed by the TILINE interface controller. The data is moved from the register file to the 990 main memory by a TILINE master write cycle. The data transfer from the data shift register to the register file and from the register file to the destination in 990 main memory is performed during a single MOV instruction.

Three different clock rates are involved in these data transfers. The TILINE operates at an asynchronous, variable word rate that is determined by the level of activity on the bus. The TMS 9900 and all of the central processor logic operates at a 3 MHz rate determined by the outputs of the TIM 9904/SN74LS362 clock oscillator (MPCK- and phases one through four). The disk interface operates at a disk read or write clock rate which is typically 500 kHz per bit for MFM data and 250 kHz per bit for FM data.

For write operations, the disk clock is a 6 MHz crystal-controlled signal divided down from the 12 MHz output of the TIM 9904/SN74LS362 oscillator. For read operations, clock transitions in the incoming data are recovered and used as the timing reference for the phase lock loop (PLL) circuit. Any variation in disk rotational speed varies the PLL clock rate. The PLL output frequency is 12 times the bit rate for MFM and 24 times the bit rate for FM data.

The one-word buffer provided by the register file adapts the asynchronous TILINE master cycle timing to disk interface timing. TILINE delays longer than one disk word time will cause a data separator overrun error. The TILINE interface cannot outrun the disk interface because a separate TILINE master cycle operation is required to transfer each data word. The 9900 control program does not inititate the master cycle until the data separator is ready.

Read Data and Write Data operations (on previously formatted tracks) are the most commonly performed disk functions. Each record on a formatted track has a sector ID header that must be read and verified before the data is read or written. The sector ID is preceded by a special sector mark that is recognized within the data separator and confirmed by reading it into the TMS 9900 for comparison against a table value. The ID words are also read into the TMS 9900 for comparison, and the CRC error bit is tested. If the ID words compare and the sector ID CRC shows no error, the read or write operation may continue, following the data path described in the previous paragraphs.

2.7.1 Disk Interface Logic Block Diagram

Figure 2-53 is a simplified block diagram of the disk interface. The two major divisions of the disk interface logic are the data separator and the drive interface circuits. The drive interface circuits include line drivers, line receivers, and the remote port control multiplexers and status demultiplexers.

The data separator circuitry includes dedicated read data input circuits and write data encoding circuits with the remaining circuits shared between read and write operations. These circuits include the data shift register, bit controller, word controller, phase lock loop clock, address mark generator/detector, and CRC generator/checker.

The data shift register performs parallel-to-serial conversion for transfers from the microprocessor bus to the data separator, and serial-to-parallel conversion for transfers to the microprocessor data bus. The remainder of the data separator logic processes serial data.

The CRC generator/checker processes serial write data through an error checking calculation and attaches the resulting CRC word to the end of the record. Data read from the disk is processed through the same calculation. If the newly calculated CRC word differs from the CRC word read from the diskette, an error has occurred somewhere in the storage/retrieval process.

Address marks are special bit patterns that do not follow the normal FM or MFM encoding rules. They may be recognized by predefined data patterns and corresponding patterns of missing clock pulses. The address mark detection logic includes a clock shift register that shifts separated read clock into parallel form. It also includes logic gates that check for the predefined missing clock patterns. Address mark missing clock patterns are loaded into the shift register in parallel and shifted out serially when formatting or writing data on a diskette.

The bit controller and the PLL clock circuit work together during read operations to develop a read clock from the incoming unseparated clock and data stream and to separate the clock pulses from the data pulses. Outputs from the bit controller during read operations include the separated data stream, reference and feedback pulse trains to the PLL clock circuit, and shift commands to the data shift register. During write operations, the bit controller works with the write data encoding logic to develop the encoded clock/data pulse stream for transmission to the drive unit.

The word controller organizes serial read data into 16-bit words, and loads 16-bit words into the data shift register for conversion to serial format. The load signal for the data shift register and for the clock shift register in the address mark detector/generator are generated by the word controller. The data separator ready signal from the word controller allows restart of microprocessor operations suspended for a data word transfer. The data separator overrun interrupt and the control signals for the CRC logic also originate in the word controller.

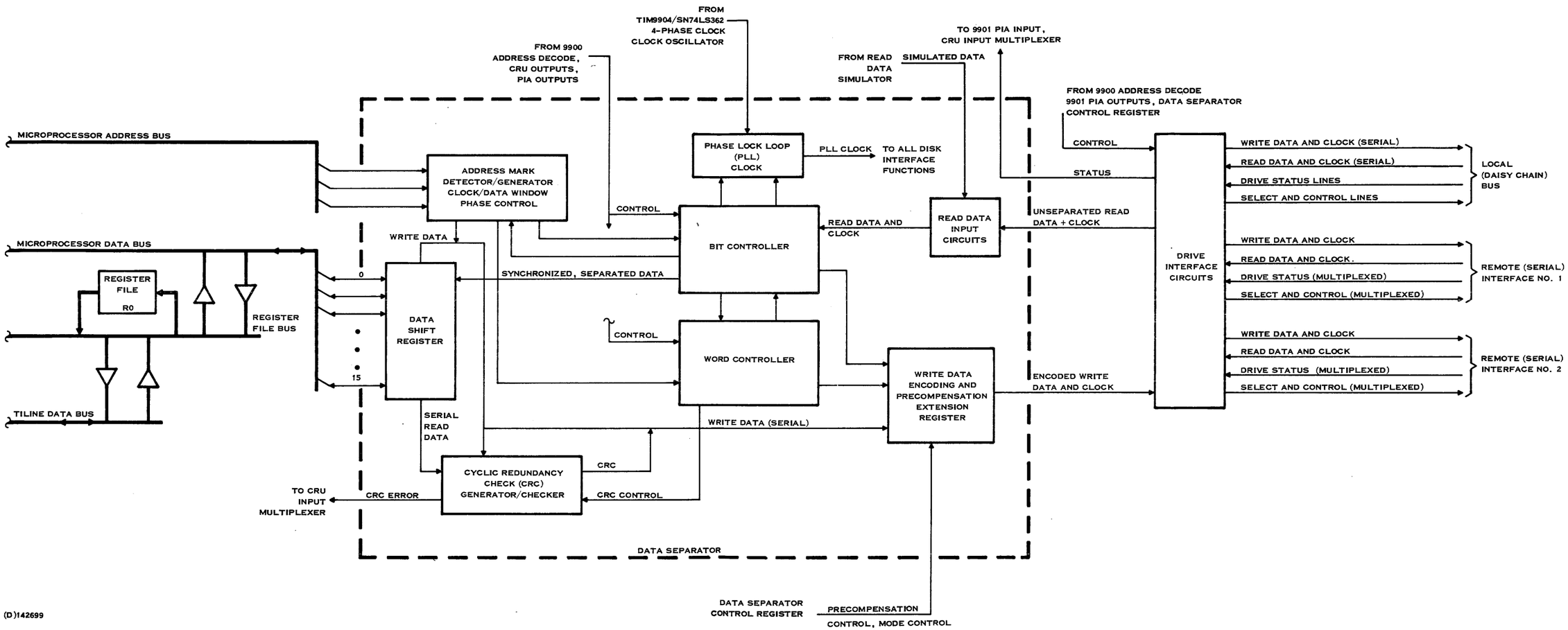


Figure 2-53. Disk Interface Simplified Block Diagram

Bit synchronization and data/clock separation are performed by the bit controller. Word controller operation is independent of the data recording mode (FM or MFM). Word controller operation is divided into modes including reset, read, write gap recirculating, write data, write gap without recirculating, and write CRC register.

High density recording, such as MFM recording on the inner tracks of a double-sided, double-density diskette, can lead to bit shifting effects. These effects are predictable, and may be precompensated as part of the recording process. Precompensation requires knowledge of the present pulse, the previous pulse, and the next pulse. The write data encoding logic includes an extension to the data shift register to allow data look-back and look-ahead. The write data encoding logic includes a ROM with the normal encoding rules and the precompensation rules. Write data encoding is essentially an extension of the bit controller functions for write operations.

The read data input circuits accept unseparated clock and data pulses from the disk drive and produce output pulses to the bit controller. These output pulses are synchronized to PLLCLK–, the main clock for all disk interface operations. Note that the read data input circuits work even when the PLL clock is not locked to the incoming clock/data stream. The read data input circuits function as pulse synchronizers to prevent glitching between the input pulse stream and the synchronous logic of the data separator.

2.7.2 Data Formats

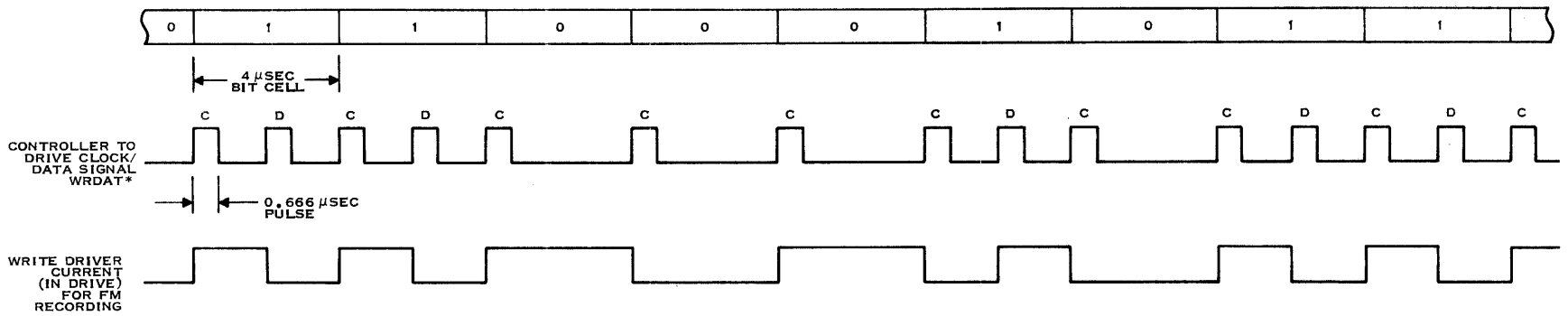
Data is recorded in FM format on SSSD diskettes, and in MFM format on DSDD diskettes. Both formats are self-clocking, although the MFM format requires much more sophisticated data separation techniques than does FM. Diskette type information is returned to the controller by the selected drive unit.

2.7.2.1 FM Data Format. Figure 2-54 shows both FM and MFM data formats. Part A of the figure shows the FM data format for a typical data pattern. The first line of the drawing shows the data pattern as it appears in the data shift register. The second line shows the double-frequency FM code in which data is transferred between the controller and the drive electronics. This code features nominal 666.6 nanosecond pulses, and a 4-microsecond bit cell. The timing accuracy of these pulses is crystal-controlled at write time, but readback accuracy is affected by many factors, especially the diskette rotation speed.

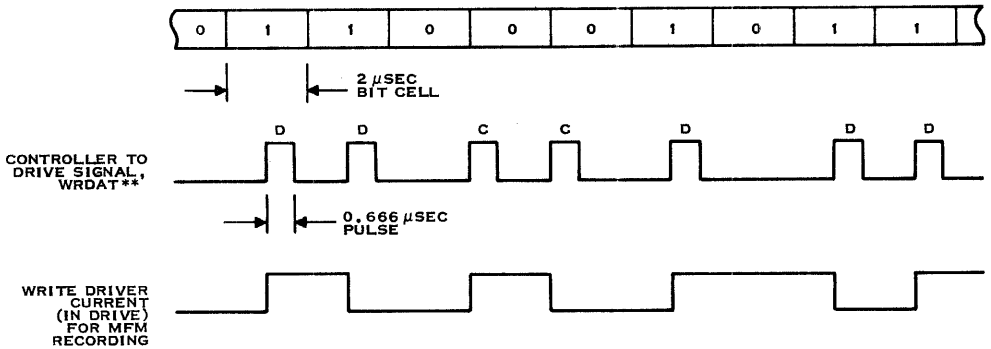
A clock pulse occurs at the beginning of each bit cell, regardless of the data value. A data one causes a data pulse at the midpoint of the bit cell, and a data zero results in no pulse at the midpoint of the cell. The code is self-clocking. The clock is simple to recover, because a clock pulse is included in every bit cell.

The next line of the illustration shows the write current as it would appear at the write current drivers in the drive unit. A flux transition is recorded for each pulse of the input waveform. On readback, the drive electronics inserts a pulse in the output waveform for each detected flux transition. The apparent frequency of the recorded FM waveform varies directly with the number of ones transmitted, from a low of 250 kHz (clock only, no data) to 500 kHz (clock and all ones data)

A. FM RECORDING



B. MFM RECORDING



NOTE: * WRITE DATA/READ DATA ENCODING FOR FM RECORDING:
1. CLOCK PULSE AT START OF EACH BIT CELL.
2. DATA PULSE IN CENTER OF BIT CELL FOR "1" DATA.

** WRITE DATA/READ DATA ENCODING FOR MFM RECORDING:
1. DATA PULSE AT CENTER OF BIT CELL FOR "1" DATA.
2. CLOCK PULSE AT BIT CELL BOUNDARY BETWEEN CONSECUTIVE "0" DATA BITS ONLY.

(B)142700

Figure 2-54. FM and MFM Waveforms for Identical Data Patterns

2.7.2.2 MFM Data Format. Part B of the figure shows MFM encoding for the same bit pattern described in part A. The first line shows the bit pattern as it exists in the data shift register. The second line shows the encoded form of write data and clock (or read data and clock) used for controller/drive data transfer for MFM recording. Technically, this is a Miller-code equivalent for the MFM signal, and the term "MFM" really only applies to the read or write current waveform of line 3. However, by convention, this manual uses the term "MFM" rather than "Miller" to describe this code.

MFM recording uses a two-microsecond bit cell, half the bit cell time for FM recording. The individual clock and data pulses remain at a nominal 666.6 nanosecond duration. The MFM encoding rules call for a pulse at the bit cell midpoint for a data one and no pulse at the bit cell midpoint for a data zero. Clock pulses are transmitted only on the bit cell boundary between consecutive data zeros. Eliminating so many clock pulses allows the available bandwidth to be used for data, but requires a phase lock clock circuit to regenerate and separate the clock signal.

Line 3 shows the resulting MFM waveform at the write driver output. Each pulse of the code in line 2 results in a flux transition on the diskette. The efficiency of MFM recording allows twice as much recorded data as FM encoding, with the same peak number of flux changes per inch.

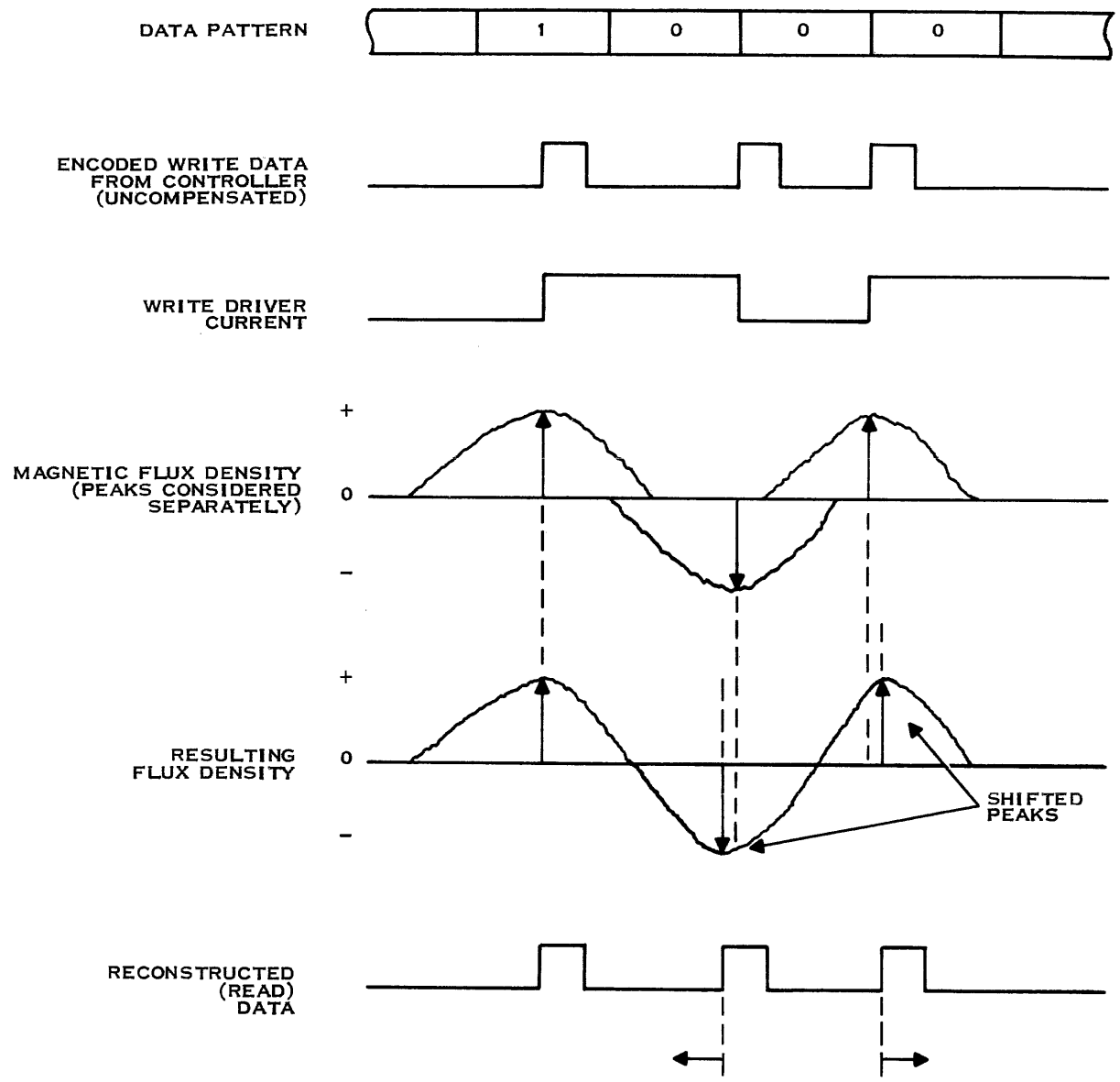
MFM is sometimes called delay modulation or triple-frequency modulation (TFM). The term "triple-frequency modulation" comes from the fact that the MFM waveform has components at a basic frequency (250 kHz), at 4/3 of the basic frequency (333.3 kHz), and at twice the basic frequency (500 kHz). These frequencies correspond to the possibility of pulses spaced by two bit cells (101), 3/2 bit cell (100), or one bit cell (000).

2.7.2.3 Peak Shifting and Write Precompensation for MFM. If the size and number of records per sector are constant, as they are on a diskette, the bit density must increase on the inner tracks, because there is a shorter physical length available than on an outer track. In fact, the bit density on the innermost track sets the basic limit for the amount of data that may be stored in a sector.

Digital magnetic recording works on the principle of a saturation write current aligning magnetic domains in a magnetic oxide. At high densities, adjacent flux transitions tend to repel each other and to spread out so that the read current peaks shift away from each other. Figure 2-55 shows a high-density pattern in which the peaks shift.

The effect is pattern-sensitive. Peak shift does not occur in the center of a closely packed group of pulses, because pulse shifting in the center is opposed from both sides. Peak shifting does occur if two closely spaced pulses are preceded or followed by a wider space. The pulse closest to the wide space tends to shift toward the wide space.

Peak shift problems show up in clock/data separation, in which shifted clock may fall into the data window, or shifted data may fall into the clock window. Even with the same amount of peak shifting, some recording techniques are less sensitive to clock/data errors than others. FM-recorded SSSD diskettes are not as sensitive to peak shift as DSDD diskettes recorded in MFM mode, even though maximum flux density (6816 flux changes/inch) is the same.



(A)142701

Figure 2-55. Example of Peak Shifting (MFM, Inner Track)

Peak shifting is the predictable result of certain data patterns; therefore, it is possible to compensate for peak shift while encoding the data for a write operation. This precompensation consists of delaying those pulses that will be peak shifted forward in time, and advancing those pulses that will be delayed by peak shift. The object is for the amount of precompensation to offset the peak shift and to simplify the task of the clock/data separation circuits. The TFDC uses write precompensation only on the inner tracks (43-76) of DSDD diskettes.

Additional information on peak shifting and precompensation is provided with the detailed description of the write data encoding and precompensation logic, paragraph 2.7.3.7.

2.7.3 Data Separator

The data separator logic performs data encoding, clock/data separation and decoding, error checking, address mark generation/detection, and gap recording functions.

2.7.3.1 Data Separator Operating Concepts. The data separator has six basic operating modes; reset, read, write data, write CRC register, write gap, and write gap recirculate. Also, depending on the diskette type, either FM or MFM format is selected. The data separator modes do not correspond one-to-one with the command codes in control word W1, as the TFDC central processor section and the data separator work together in performing the commanded operation.

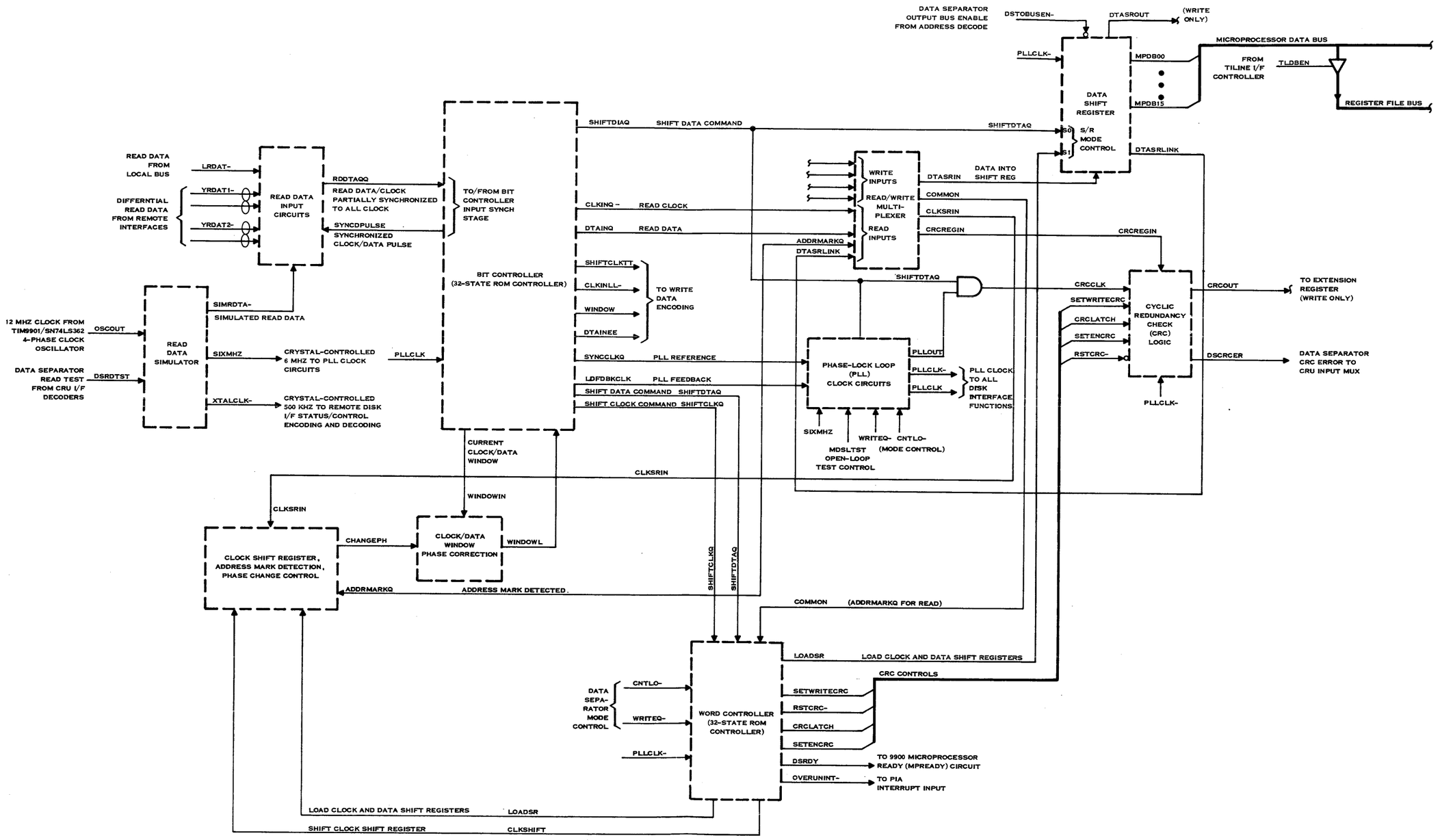
For example, a Write Data command (code 011) requires the data separator to operate in read mode while checking the sector ID, in write gap recirculate mode prior to the record, in write data mode while writing the data address mark and the data record, and in write CRC mode after the last data word. Data separator mode selection is determined by the 9900 control program through the CRU bus.

A track on a diskette is recorded in a carefully defined format as shown in Figure 1-22 (FM) and Figure 1-23 (MFM). In simplest terms, the data separator accepts parallel data words from the microprocessor data bus and records the data on the diskette track in the prescribed format, or it accepts serial input data in that format and translates it into parallel words on the microprocessor data bus.

Read Operating Concepts. Refer to Figure 2-55A, the data separator block diagram, for read operations. Read operations require the data separator to develop a clean, jitter-free clock signal (PLLCLK) that has the same relationship to the read data as the original write clock had with the original write data. This reconstituted clock is used for synchronization of all data separator logic. PLLCLK and PLLCLK- are generated by the phase lock loop clock circuits.

The data separator must accept an incoming read data stream that consists of data and clock recorded in FM or MFM mode, and must separate the clock and data. The bit controller, clock shift register, and the clock/data window phase correction ROM work together to distinguish between clock and data and to keep the PLL clock circuitry correctly locked to the incoming bit stream. This process involves some lock-in time because it is iterative.

The bit controller sets up a clock window and a data window and then samples incoming pulses to determine where they fall in with respect to the clock or data window. The bit controller issues frequency correction pulses to the PLL clock circuitry to keep incoming pulses centered in the window. It also issues shift pulses to the data and clock shift registers.



(D)142704

Figure 2-55A. Data Separator Block Diagram for Read Operations

In the worst case, the clock and data window are reversed, so that incoming data is treated as clock and incoming clock is treated as data. The clock shift register detects missing clock pulses. If four successive clock pulses are missing, the clock/data window phase correction ROM issues a signal that toggles (interchanges) the clock and data windows. These lock-in and window phase correction operations start during the gaps that precede blocks of data so that the windows and the clock are properly synchronized before the first meaningful data.

In addition to separating clock from data, the data separator must determine word boundaries so that the data separator ready output goes active when a 16-bit data word is correctly positioned in the data shift register. The read data would be meaningless if the data separator could not establish the correct word boundaries. The word controller and the address mark detection ROM work together to determine the word boundaries.

The diskette track format identifies the start of a sector ID header or the start of a data record by a special character that violates the normal FM or MFM recording rules. These characters are called "address marks." A sector ID is preceded by an ID address mark and a data record is preceded by a data address mark. The IBM format conventions for an SSSD (FM) diskette also require an index address mark on each track, and allow a special delete data address mark to precede control records. The important feature of an address mark is that it immediately precedes the first bit of the ID or data record and establishes the word boundary. Once the address mark has been detected, the word controller determines subsequent boundaries by tallying up bit shifts into groups of 16 bits.

An address mark is a single byte that contains a predetermined data value and violates the FM or MFM encoding rules by omitting selected clock pulses. An 8-bit clock shift register in the address mark detection logic supplies the pattern of missing clocks to a ROM that identifies the address mark. This is the same ROM that is used for clock/data window phase correction. The clock/data window phase is not toggled until four missing clocks are detected to prevent an address mark (up to three missing clocks) from changing the window.

The transfer of each data word out of the data separator to the register file (data) or the TMS 9900 microprocessor (sector ID) is accompanied by a handshaking exchange of data separator select and data separator ready signals between the data separator and the microprocessor. Microprocessor operations are suspended during the interval between data separator select and data separator ready.

The last word of a sector ID or a data record is a 16-bit CRC word that was calculated and recorded at write time. The serial read data (after clock/data separation) is processed through the same CRC logic and should leave an all zeros remainder at the end of the record. Anything other than all zeros indicates that a recording or transmission error has occurred. A CRC error signal notifies the microprocessor so that the control program may initiate retries in an attempt to correctly read the data.

Write Operating Concepts. The data separator writes gap patterns, sector ID headers, address marks, data and CRC words on a diskette. The encoding mode and the details of the address marks and gap patterns are determined by the MFM/FM mode control signal.

A stable, accurate clock is required for write data encoding in order to simplify reading from the diskette and to allow diskette transportability between flexible disk systems. Logic in the PLL clock circuit selects a crystal-controlled 6 MHz output and distributes this clock through the PLL clock output drivers to the data separator logic.

The bit controller, write data encoding logic, and (if required) the precompensation logic are involved in the encoding of bit patterns onto the disk. The bit controller establishes clock and data windows and shifts data from the data shift register. Data encoding is straightforward for FM. MFM encoding is more complex, particularly if precompensation is specified. The 9900 control program specifies write precompensation for MFM encoding on the inner tracks (43–76).

Write precompensation involves deliberately delaying or advancing the positions of clock and data pulses depending on the data pattern. Precompensation requires a capability to look back at the two previous data bits and to look forward to the next data bit after the current bit. A ROM detects the critical patterns and selects on-time, early, or late pulse outputs from the bit controller.

The write encoding logic must also be capable of recording address marks on the diskette. The data word for an address mark and a missing clock pattern are supplied by the microprocessor to the write encoding logic. The missing clock pattern is shifted through the clock shift register as part of the encoding process. This is the same register that is used in detecting address marks during read operations.

The missing clock pulse outputs must go to the bit controller because they affect the details of the MFM or FM data pattern being generated. Also, if precompensation is specified, missing clock information must be accounted for in the precompensation ROM. Precompensation is disabled for those bits of an MFM address mark that are adjacent to a missing clock.

The word controller is again in charge of word boundaries, rather than the details of data pattern encoding. In fact, the word controller logic does not have an input that specifies FM or MFM encoding. The word controller tallies shift pulses and controls the loading of new 16-bit words from the microprocessor data bus into the data shift register.

Data and sector ID words are processed through the CRC generation logic as they are shifted through the data separator. At the end of the sector ID or data record (as identified by the microprocessor) the word controller switches the data source so that the last word encoded is the CRC word.

The diskette format requires gaps of specified length on the diskette. These gaps are not empty; standard patterns must be recorded in the gaps. The word to be written in the gap is determined by the 9900 control program and is supplied to the data separator over the microprocessor data bus. The data separator has two modes for writing gap patterns. The write gap recirculate mode continually cycles the same word through the data shift register and writes that pattern on the diskette. The write gap mode does not recirculate the gap word, and so a new gap word must be loaded from the microprocessor data bus every 16 bit times. A CRC word is not recorded at the end of a gap.

Gaps are written as part of a diskette formatting operation (Write Format) that also writes ID address marks, sector ID headers, and an index address mark (FM only).

Gap words allow synchronization of the bit controller and PLL clock logic prior to reading any type of address mark, sector ID, or data record. The section of the gap that precedes a data address mark and data record is rewritten as part of the Write Data operation. The rewrite operation is necessary because the exact clock phase and frequency that existed during the Write Format operation is not the same as that which may be written many revolutions, days, or disk insertions later. There is inevitably a glitch in the gap at the point where the predata rewrite starts. In the read mode, firmware timing holds the data separator reset, keeping the PLL clock locked to a 6 MHz reference until after the rewrite glitch.

2.7.3.2 Phase Lock Loop (PLL) Clock Circuitry. There are three major timing schemes in the TFDC; asynchronous timing for the TILINE interface, microprocessor clock timing for the central processor logic, and PLL clock for the disk interface. TILINE interface timing and microprocessor clock timing are described in previous paragraphs. This paragraph describes the development of the PLL clock outputs, PLLOUT, PLLCLK, and PLLCLK–, that clock all disk data transfer functions between the data shift register and the drive units. Depending on the disk operation, these clock outputs may be supplied by a fixed reference frequency or by the variable-frequency output of a phase lock oscillator.

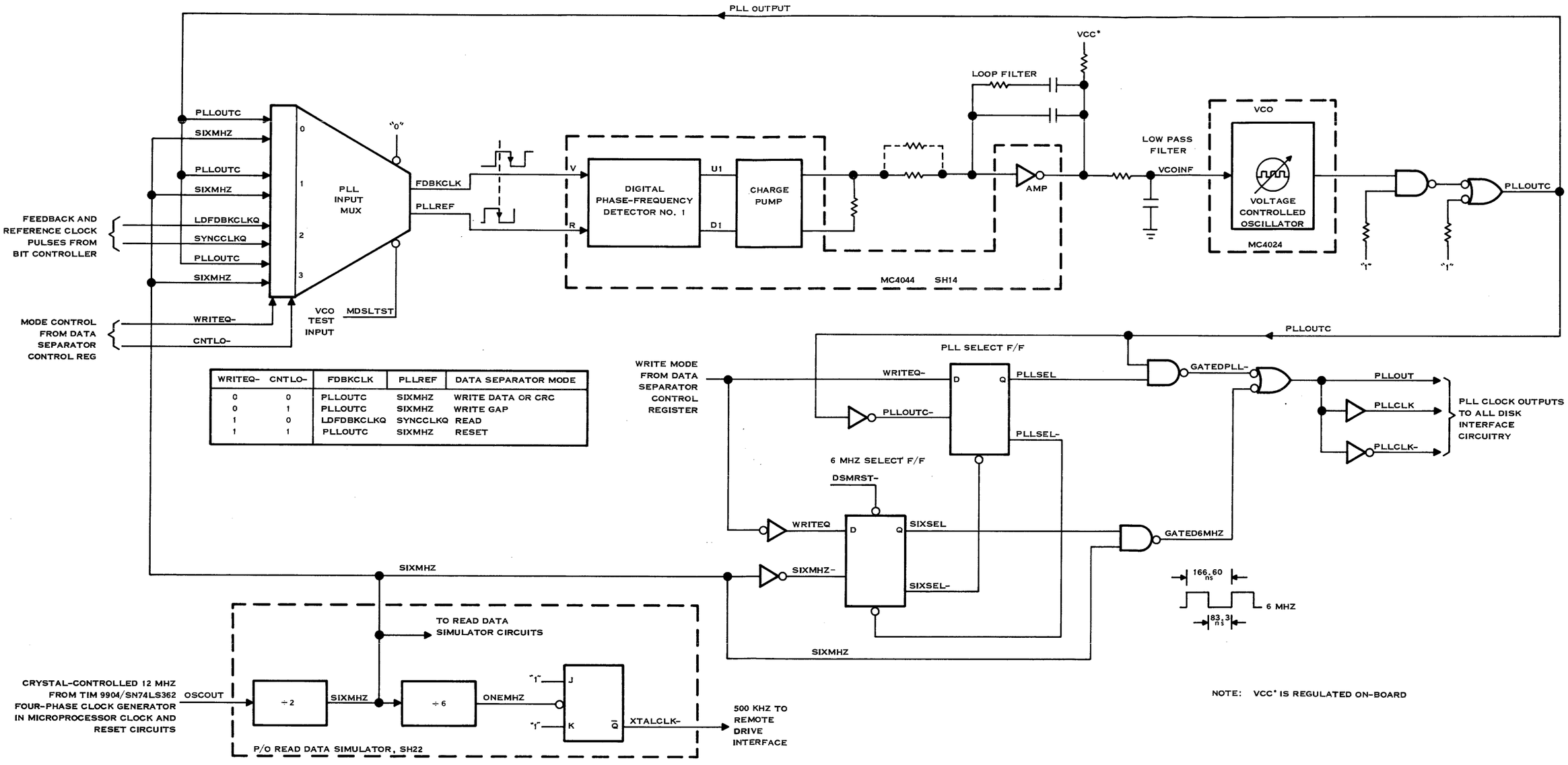
A fixed, 6-MHz crystal-controlled clock reference is always selected for writing on the disk. This is true whether the controller is writing gap patterns, synchronization patterns, address marks, sector ID headers, or data. A stable and accurate write clock makes reading easier and enhances drive-to-drive transportability of diskettes.

The data stream read from a disk drive includes unseparated clock and data encoded in FM or MFM format. The original clock and relationship between clock and data must be regenerated in order to properly separate clock from data and to convert the serial data stream into the same 16-bit words that were originally recorded. The frequency and phase of the read clock is affected by frequency variations in the original write clock, pulse spacing variations due to mechanical imperfections in disk rotation during the write process, media limitations, and rotation imperfections during the read process. A phase lock loop is the only practical means of regenerating the clock for MFM recovery. It is possible to recover FM data without using phase lock techniques, but phase lock circuits provide superior performance.

The PLL circuit and the bit synchronizer work together to develop a PLL clock waveform, synchronize the clock frequency to the incoming clock, determine the clock/data windows, and separate data from the incoming clock/data waveform. The PLL oscillator operates at a multiple of the incoming clock rate for high resolution. PLL damping averages out clock jitter and other short-term variations.

The PLL clock circuitry is shown in Figure 2-56. The PLL circuitry is at the top of the drawing, the fixed/variable clock selection flip-flops and gates are in the center, and the fixed frequency divider circuits are in the lower left corner.

Recall from the description of the microprocessor clock generation circuits (paragraph 2.6.3) that the four-phase clock oscillator uses a 48-MHz crystal as the basic timing control, and provides a 12-MHz output, OSCOUT, to dividers in the read data simulator logic. These dividers are shown in the lower left corner of the figure. OSCOUT is divided by two to produce SIXMHZ, the frequency reference for write operations and for read data simulation.



WRITEQ-	CNTLO-	FDBKCLK	PLLREF	DATA SEPARATOR MODE
0	0	PLLOUTC	SIXMHZ	WRITE DATA OR CRC
0	1	PLLOUTC	SIXMHZ	WRITE GAP
1	0	LDFDBKCLKQ	SYNCCLKQ	READ
1	1	PLLOUTC	SIXMHZ	RESET

(D)142702

Figure 2-56. Phase Lock Loop (PLL) Clock Generation

The PLL clock source selection circuitry consists of the PLL select flip-flop (F/F), the 6-MHz select F/F, and some gates. The PLL select and 6-MHz select F/F are cross-connected (from Q-outputs to unconditional reset inputs) so that only one of the flip-flops may be set. Clock pulses appear either at the GATEDPLL- output or the GATED6MHZ- output.

The inverted form of the read/write mode control signal (WRITEQ-) sets the 6-MHz select F/F for any write to the disk, whether a gap, synch pattern, address mark, sector header, or data record write.

WRITEQ- high sets the PLL select F/F for any read operation, including the sector address mark and sector ID reads necessary to locate a sector during a Write Data operation. Notice that SIXMHZ- clocks the 6-MHz select F/F, and that PLLOUTC- clocks the PLL select F/F. This synchronous control of the F/Fs assures glitch-free selection of the clock source.

The WRITEQ- signal is derived from the data separator write mode signal (DSWMODE-) after two stages of clock delay. DSWMODE- is an output of the data separator control register, an 8-bit addressable latch loaded from the microprocessor CRU output.

The variable-frequency clock generator includes the PLL input multiplexer, MC4044 phase-frequency detector and the MC4024 voltage-controlled oscillator (VCO). These components form a digital phase lock loop that locks the MC4024 oscillator output to the phase of an incoming reference signal.

The MC4044 has four basic circuits in one 14-pin dual inline package (DIP). These circuits are: phase-frequency detector #1, quadrature phase-frequency detector #2 (not used), a charge pump, and a Darlington amplifier stage.

Phase-frequency detector #1 is a digital phase meter that examines the negative(1-0) transitions of a reference input R and a variable or feedback input V. The circuit responds only to transitions; therefore, the phase-error signals developed are independent of input waveform duty cycle or magnitude variations.

The phase-frequency detector has two output lines, U1 and D1. If the reference voltage transitions lead the variable voltage transitions, D1 is held high and a pulse train is gated out on U1. The pulse width of the active-low U1 pulses is proportional to the phase difference between R and V. This situation corresponds to the reference having a phase lead.

If the reference voltage transitions lag the variable voltage transitions, U1 is held high and a pulse train is gated out on D1. The pulse width of the active low pulses is proportional to the phase difference between R and V. This corresponds to the reference having a phase lag.

If the negative transitions of R and V coincide, U1 and D1 remain at the high level.

If R is higher in frequency than V, the U1 output waveform varies at a rate proportional to the frequency difference because a phase difference is noted on each negative reference edge.

The U1 and D1 outputs of phase-frequency detector #1 are connected to the inputs of the MC4044 built-in charge pump. The charge pump output voltage is connected through a voltage divider to an amplifier circuit.

The internal Darlington amplifier is combined with external RC components to control the loop

response characteristics. A low-pass filter section and an integrator are combined to eliminate the high-frequency components and to average the charge pump output into a dc control voltage. The averaging, which occurs over a number of input data frames, prevents short-term read jitter from affecting the VCO output clock frequency.

The dc control voltage (VCOINF) ranges from 1.5 volts (loop unlocked, no input transitions) to 4.5 volts (unlocked, excess input transitions). In the locked condition, the control voltage is approximately 4 volts.

The dc control voltage (VCOINF) is applied to one half of an MC4024 dual voltage-controlled oscillator. The output of the MC4024 is a square wave (PLLOUT) with the frequency determined by the magnitude of VCOINF. The frequency of PLLOUT is nominally 6 MHz, but it can be varied by the control voltage.

PLLOUTC is applied to the variable (V) input of the phase-frequency detector. The feedback loop corrects the VCO frequency to keep the feedback pulse (FDBKCLK) locked in phase with the PLL reference pulse (PLLREF).

The FDBKCLK and PLLREF signals are supplied by the PLL input multiplexer. The WRITEQ- and CNTL0- data separator mode control signals select the multiplexer inputs. For all operations except read, PLLOUTC is selected as FDBKCLK and SIXMHZ is selected as PLLREF, so that PLLOUTC is locked to the 6-MHz fixed frequency.

Notice that if WRITEQ- is low, GATED6MHZ- is selected as the PLL clock source, and PLLOUTC is not used external to the phase lock loop. However, PLLOUTC is kept locked to the 6 MHz reference, to prevent the loop from drifting away from the nominal operating frequency. Also, if WRITEQ- is high, and CNTL0- is also high (data separator reset mode), PLLOUTC is kept locked to the 6 Mhz reference. PLLOUTC (locked to 6 MHz) serves as the PLL clock in this mode. However, the read data input circuits are held reset, so no data can be processed.

Data separator read mode is always preceded by the reset mode. Data separator read mode (WRITEQ- = 1, CNTL0- = 0) uses feedback clock and reference pulses generated by the bit controller ROM rather than PLLOUTC and SIXMHZ. These pulse signals, LDFDBKCLQ and SYNCCLKQ, are generated as a result of bit controller decisions concerning the relative timing of the input pulses and the clock and data windows established by the bit controller.

The bit controller subdivides the data frame into smaller windows. The bit controller examines each unseparated clock/data input pulse (SYNCDPULSE), and determines into which subwindow that pulse fits. Based on whether the input pulse falls early or late in the subwindow, and whether the pulse is to be considered clock or data, a decision is made in the bit controller to speed up the PLL clock (issue SYNCCLKQ before LDFDBKCLQ), slow down the PLL clock (issue LDFDBKCLKQ before SYNCCLKQ), or leave the PLL clock alone (simultaneous outputs or no output).

These bit controller decisions are based on the encoding mode, and upon a complex state sequence built into the bit controller. The details of LDFDBKCLKQ and SYNCCLKQ control are described with the bit controller flowcharts. The important things to note at this point are that the MC4044 device will develop an error voltage that tends to drive the MC4024 VCO output frequency up or down to minimize the phase difference between FDBKCLK and PLLREF. An integrating filter damps the error voltage and averages the VCO response, so that it does not jitter or get thrown off frequency by occasional contradictory or missing input pulses. The VCO operates at an integer multiple of the frame rate to provide high resolution of the read clock/data stream.

The PLL circuitry is particularly sensitive to voltage variations and noise on the +5 Vdc supply line. An on-board voltage regulator and filter provide five-volt power, Vcc1*, to the MC4044, the MC4024, and the pullup resistor on the VCOIN line. Special analog grounds are provided for the analog loop amplification and filtering circuits.

2.7.3.3 Data Separator Control. The TMS 9900 microprocessor issues control signals to the data separator via the CRU bus and the address bus decoding logic, as shown in Figure 2-57. The data separator control register is an eight-bit addressable latch that is loaded from the CRU bus and is synchronized with CRU clock. Address bus decoding is performed by a ROM, and the outputs are delayed behind the memory cycle by the ROM access time.

Any of the control outputs that affect critically timed data separator operations are resynchronized to the trailing edge of PLL clock. The data separator mode control signals, WRITEQ-, CNTL0-, and CNTL1- are synchronized through two F/F stages. Data separator mode selection is shown in Table 2-26.

2.7.3.4 Read Data Input Circuits. Refer to Figure 2-58, the simplified diagram of the read data input circuits. The read data input circuits accept an unseparated clock/data waveform from the selected drive unit and synchronize the input pulses to data separator phase lock clock, PLLCLK-.

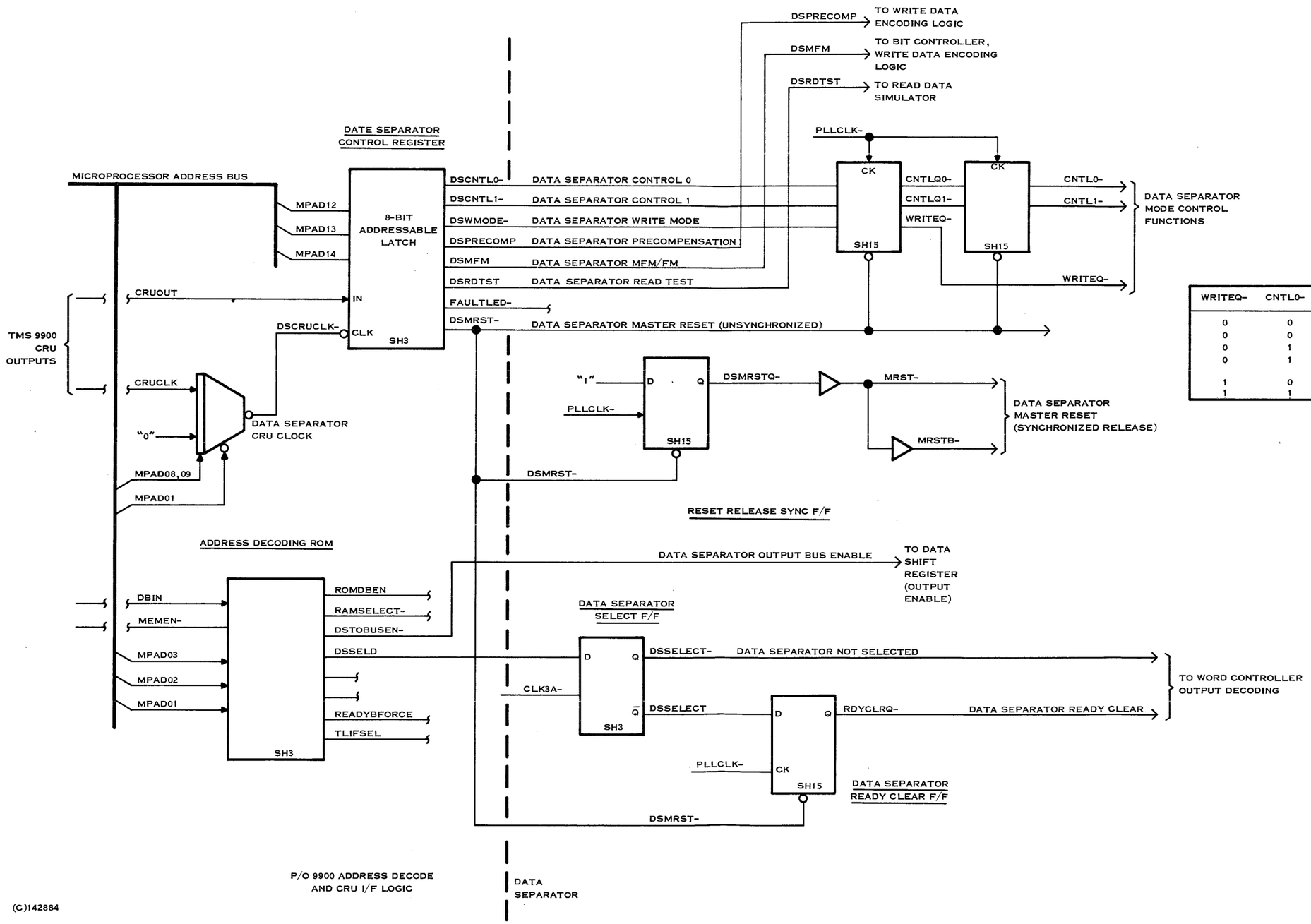
Input data may come from the local disk interface (LRDATB-), one of two remote chassis interfaces (RDAT1-, RDAT2-), or the on-board read data simulator.

An asynchronous (with respect to the data separator) input pulse from the drive sets the input F/F (RDDTAQ) immediately. The RDDTAQ flip-flop sets on the next trailing (positive-going) edge of PLLCLK- to synchronize the input to the rest of the data separator logic. The SYNCDPULSE F/F provides a second level of synchronization to assure that no input pulses are lost.

The synchronized data pulse (SYNCDPULSE) wraps around and unconditionally sets the RDDTAQ and RDDTAQQ F/FS. SYNCDPULSE clears on the next PLL clock pulse. The PLLCLK- frequency is a multiple of the incoming data rate: 12 times the data rate for MFM, and 24 times the data rate for FM. Even if the PLL is not yet properly locked, the PLL clock rate is so much faster than the incoming clock/data rate that no pulses are missed. The PLL clock rate is nominally 6 MHz, but it varies to keep the data and clock windows centered on the incoming data. SYNCDPULSE is one PLL clock period in duration, so it is 1/12 of a bit cell for MFM, or 1/24 of a bit cell for FM. SYNCDPULSE goes from the read data input circuits to the bit controller which must determine whether each individual pulse represents encoded clock or data. The bit controller also must determine where the pulse occurs with respect to the current data or clock window, in order to correct the PLL and keep the windows accurately centered on the incoming data stream.

The CNTL0- signal allows the read data input circuits to operate when the data separator is in the read mode, write data mode, or write CRC mode. However,the bit controller ignores the SYNCDPULSE input during write data or write CRC operations, so there is no interference*. CNTL0- high disables the read data input circuits during the write gap, write gap recirculate or reset mode. The reset mode always precedes the read mode, so the flip-flops start the read operation in the cleared state.

* SYNCDPULSE is also ignored in some states of the read mode to eliminate reaction to illegal pulse positions (Tables 2-28, 2-29).



WRITEQ-	CNTL0-	CNTL1-	MODE
0	0	0	WRITE CRC REGISTER
0	0	1	WRITE DATA
0	1	0	WRITE GAP
0	1	1	WRITE GAP RECIRCULATE
1	0	X	READ
1	1	X	RESET

Figure 2-57. Data Separator Control

Table 2-26. Data Separator Mode Selection

WRITEQ-	CNTL1-	CNTL0-	Mode
0	0	0	Write CRC register
0	0	1	Write gap
0	1	0	Write data
0	1	1	Write gap recirculate
1	X	0	Read
1	X	1	Reset

2.7.3.5 Bit Controller. For read operations, the bit controller performs the functions associated with separating encoded clock and data pulses supplied by the read data input circuits. These functions include:

- Establishing a clock window and a data window for deciding whether an incoming pulse represents clock or data
- Dividing the clock and data windows into sampling subwindows to accurately determine input pulse position with respect to the nominal clock or data window
- Adjusting window size so that it remains proportional to the incoming data rate
- Adjusting the window phase via the PLL clock circuit, so that the window is kept centered on the average incoming data pulse position, even in the presence of input data jitter
- Issuing the reference and feedback pulses to the PLL clock circuit to keep the PLL clock accurately locked to the incoming clock
- Sending reconstituted clock and data pulses and the corresponding shift pulses to the clock and data shift registers
- Sending shift data and shift clock pulses to the word controller for use in determining word boundaries.

For write operations, the bit controller performs a slightly different group of functions, as follows:

- Developing clock and data shift pulses for the clock and data shift registers and the word controller

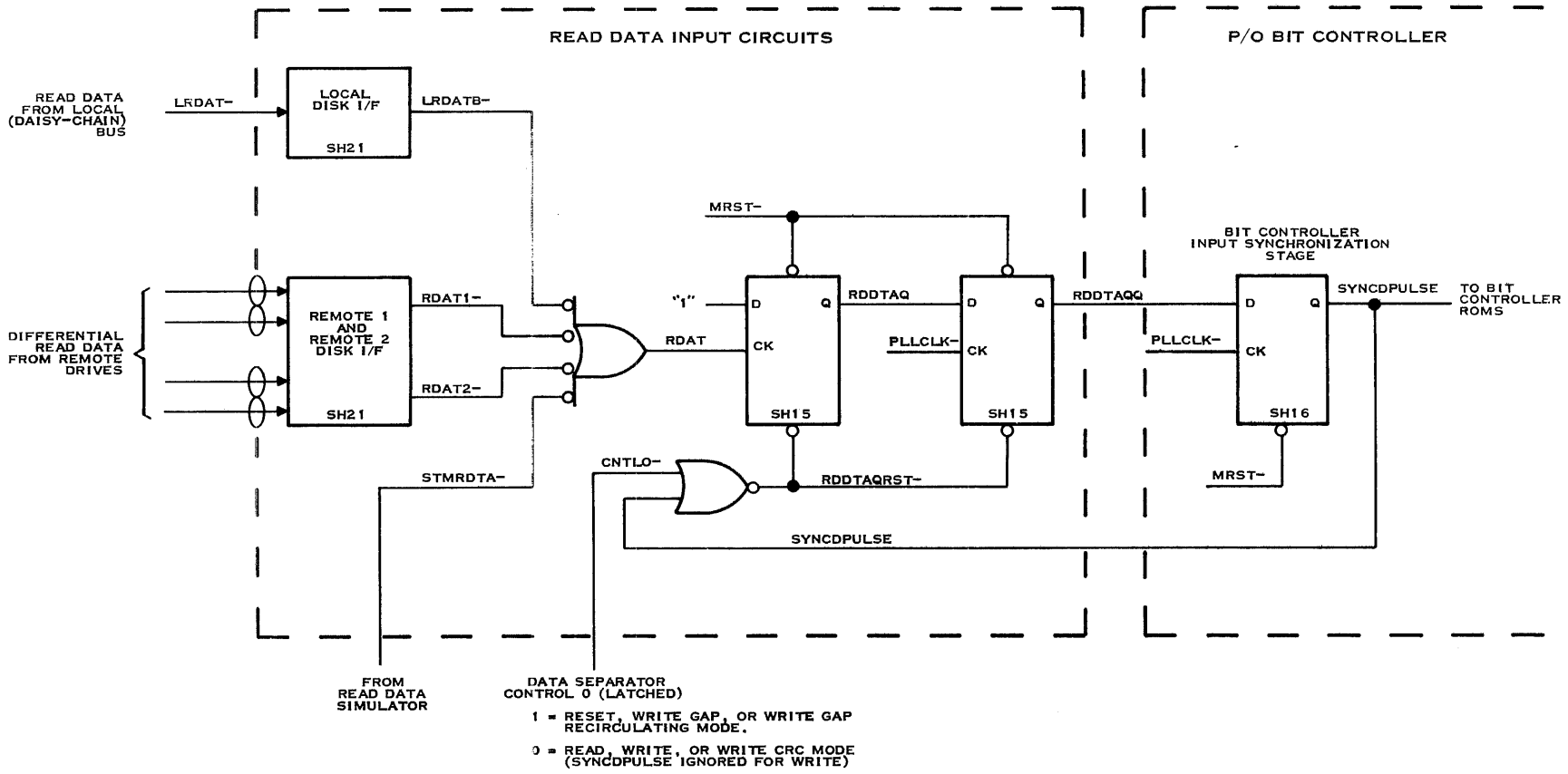


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Figure 2-58. Read Data Input Synchronization Circuits

- Providing the pulse outputs and an identifying clock/data window signal to the write data encoding logic. For the case of MFM, which may require precompensation, supplies output pulses that are early, late, and on-time with respect to the nominal center of the clock or data window.

The bit controller, clock/data window control logic, and read/write multiplexer are shown in Figure 2-59. The bit controller is a ROM-based state controller, similar to the TILINE I/F controller. A general introduction to ROM-based state controllers is provided with the TILINE I/F controller description (paragraph 2.5.9.1). Basically, this type of machine uses its current state (latched in a register) and one or more input variables as address inputs to a ROM. Based on the ROM address inputs, the codes burned into the ROM determine the next state and the values of output variables. A particular state involves multiple ROM words.

The bit controller includes two ROMs, an SN74S287 (part number 2261700-4) and an SN74S472 (part number 2261703-1). The smaller SN74S287 provides only next state bits, while the SN74S472 ROM provides the LSB of the next state and all the bit controller outputs. State changes occur in synchronism with PLL clock because it is PLLCLK- that loads the next state into the current state register.

The access time of the bit controller ROM (typically 55 nanoseconds) determines when the bit controller outputs are stable. An output synchronization register, clocked by PLLCLK-, provides synchronous, deglitched outputs delayed by one clock period. These outputs remain stable for a minimum of one clock period (166.6 nanoseconds nominal for write).

Bit controller input and output signals are described in Table 2-27.

Bit Controller ROM Listings. The bit controller has four operating modes, selected by the DSWMODE and WRITEQ- control signals. These are the two most significant bits (MSBs) of the bit controller ROM addresses, so they divide the ROM contents into four major groups, one per mode. The bit controller operating modes are write FM, write MFM, read FM, and read MFM.

The bit controller operations are described by state diagrams. These operations are controlled by the contents of the bit controller ROM devices. The ROM input/output bit assigments and listings are presented here for reference.

Figure 2-60 shows the input (address) and output bit assignments of the two bit controller ROMs. This figure may be used with the SN74S287 ROM listing of Table 2-28 and the SN74S472 ROM listing of Table 2-29 for detailed analysis of bit controller operation. It is important to remember that the individual ROM word selected for output (addressed) depends on the current state of the bit controller (BITCNTLQ1-4) and the input variables.

These tables are derived from the HI-LO listing of the data used to program the devices. The first column shows the bit controller current states, which are not shown in the HI-LO listing. These state numbers are in hexadecimal form. The input addresses, in decimal form, are in the next column. The ROM words stored at these addresses are given in the remaining columns.

The SN74S287 ROM listing shows eight four-bit words per row, and the SN74S472 listing shows four eight-bit words per row. The rows are grouped together in blocks for easier reading. For example, the first four rows of the SN74S287 listing correspond to the write FM mode with the unseparated clock/data input (SYNCDPULSE) equal to zero. The individual word address selected in that group depends on the current state, given in the first column.

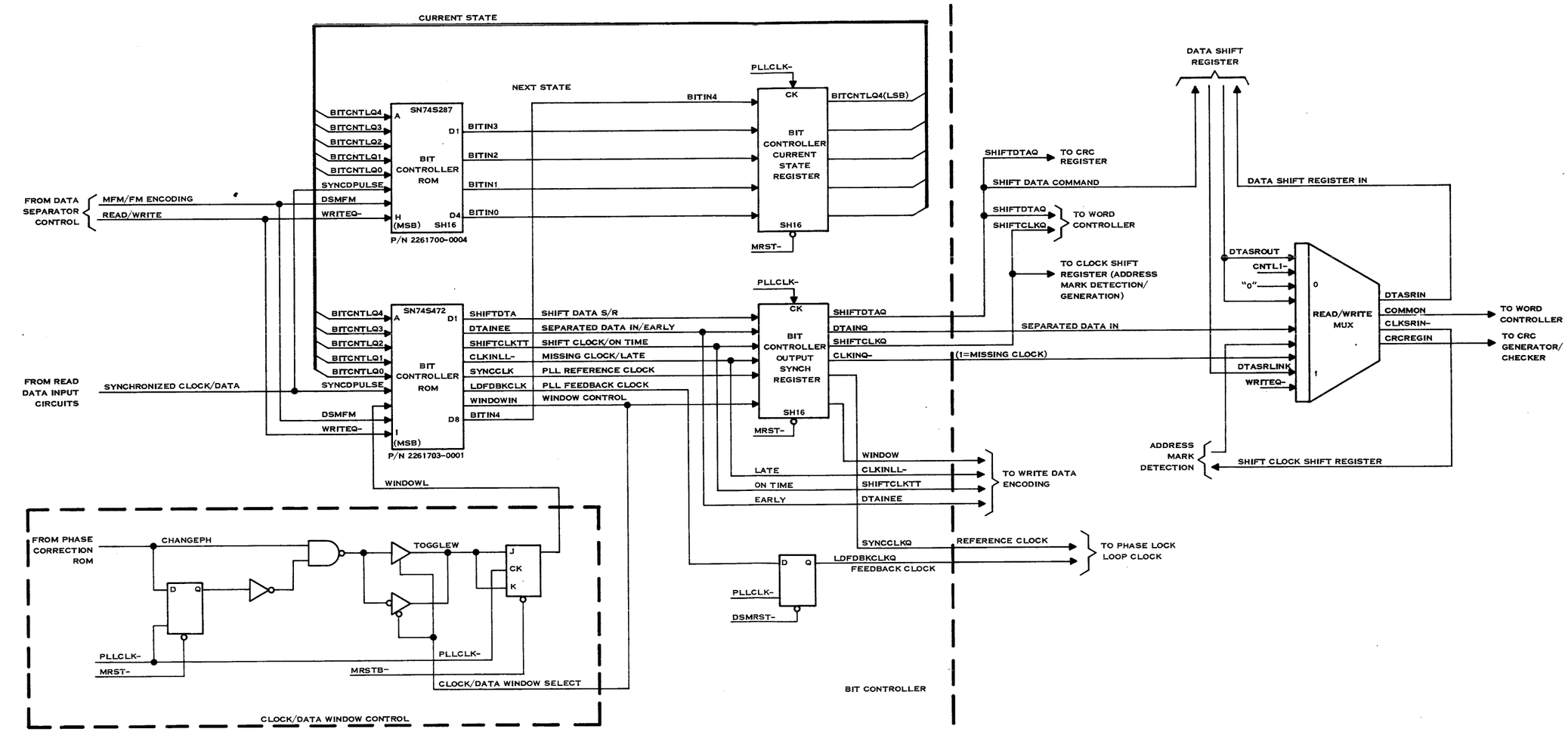


Figure 2-59. Bit Controller and Read/Write Multiplexer Logic

Table 2-27. Bit Controller Input/Output Signals

Signature	Sheet	Gate*	Description
Inputs:			
BITCNTLQ(0-4)	16	UM014 (UHG003)	Bit controller current state (latched)
DSMFM	3	UK062-9 (UEK089)	Data separator MFM. High for MFM encoding/decoding, low for FM.
SYNCDPULSE	16	UO050-7 (UHB058)	Synchronized data pulse. Unseparated clock and data stream from read data input circuits, synchronized to PLL clock for operation with bit controller.
WINDOWL	15	UO090-5 (UHB116)	Window latch. Current clock/data window. FM: High = clock window Low = data window MFM: High = data window Low = clock window
WRITEQ-	15	UL062-6 (UHB089)	Write mode. Low for write, write gap, write gap recirculate, or write CRC mode. High for read or reset mode.
Outputs:			
BITIN(0-4)	16	UN014, UO026 (UGF016, UHB029)	Bit controller next state.
CLKINLL-	16	UO026-9 (UHB029)	Missing clock/late pulse. Read: High = missing clock Low = clock pulse Write: late pulse
CLKINQ-	16	UO050-12 (UHB058)	Latched and synchronized version of CLKINLL-
DTAINEE	16	UO026-7 (UHB029)	Data in/early pulse Read: separated data Write: early pulse
DTAINQ	16	UO050-15 (UHB058)	Latched and synchronized version of DTAINEE.

Table 2-27. Bit Controller Input/Output Signals (Continued)

Signature	Sheet	Gate*	Description
LDFDBKCLK	16	UO026-12 (UHB029)	Load feedback clock (read only).
LDFDBKCLKQ	15	UL062-16 (UHB089)	Latched and synchronized feedback clock output to PLL clock (read only). Considered active low for MFM.
SHIFTDTA	16	UO026-6 (UHB029)	Shift data command.
SHIFTDTAQ	16	UO050-5 (UHB058)	Latched and synchronized shift data command to data shift register, CRC circuit and data controller.
SHIFTCLKTT	16	UO026-8 (UHB029)	Shift clock/on time. Read: shift command Write: on time pulse to data encoding logic
SHIFTCLKQ	16	UO050-2 (UHB058)	Latched and synchronized version of SHIFTCLKTT.
SYNCCLK	16	UO026-11 (UHB029)	PLL reference clock.
SYNCCLKQ	16	UO050-10 (UHB058)	Latched and synchronized PLL reference clock output (read).
WINDOWIN	16	UO026-13 (UHB029)	Bit controller ROM output that controls the window F/F to select either the clock window or the data window depending on bit controller state and present inputs. Keeps the window positioned with respect to the incoming data. WINDOWIN = 1 causes the window F/F to toggle in read mode.

Note:

* Gate numbers in parentheses refer to 2267295 fineline board. Pin numbers correspond.

State Diagram Introduction. A state diagram is the clearest way to describe the operation of a ROM-based state machine such as the bit controller or the word controller. A state diagram consists of nodes (circles) representing the states, and directed lines between the nodes representing all the possible transitions. Each node is identified with a state number (current state). Complex sequences that depend on past history and present inputs can be represented on a state diagram.

The outputs that are active as the result of a particular state or transition are shown on the diagram. The inactive outputs are omitted to simplify the diagram and highlight the important changes. The inputs that cause a particular state-to-state change are usually shown, unless they are understood. For example, the bit controller changes state on every PLL clock pulse, following a numerical sequence unless some input causes a branch out of numerical order. In this case, only the input that caused the branch is shown. The PLL clock pulses that cause the changes from state 2 to state 3 to state 4 are not shown.

Bit controller operations are described by four separate state diagrams, one for each bit controller mode (write FM, read FM, write MFM, read MFM). A single state diagram covering all modes would be unnecessarily complex.

Bit Controller Write FM State Operation. Refer to Figure 2-61, the bit controller write FM state diagram. Also, it may be helpful to refer back to Figure 2-54, which describes FM data encoding.

Bit controller operations for FM are straightforward. There are 24 individual states, numbered from 0 to 17_{16}. The states are linked in a straight numerical sequence, 0,1,2,...,F,10,...,17,0. There are no branches on this diagram.

The bit controller advances one state on the trailing edge of each PLLCLK- pulse. The state changes once every 166.667 nanoseconds, as PLLCLK- is a crystal-controlled 6 MHz waveform for data separator write operations. The entire sequence of 24 states is completed once every 4 microseconds, which is one bit frame for FM data. The 24 states of the bit controller divide an FM bit frame into 24 subwindows.

The bit controller determines the clock and data windows, which lag one PLL clock time behind the WINDOWIN control output. WINDOWIN is low from state B_{16} through state 16_{16} and high in state 17_{16} and states 0 through A_{16}. The WINDOWIN signal, which lags one clock time behind WINDOWIN, is used by the write data and precompensation ROM to select the source of WDATA-.

Following the state sequence shows that SHIFTCLKTT is high for 8 states (1.3333 microseconds), low (active) for 4 states, (0.6667 microseconds), high for another 8 states, and low for the last 4 states of the bit controller cycle. Thus, SHIFTCLKTT is an asymmetrical waveform with a two-microsecond period.

The states with SHIFTCLKTT low (states 8-B and 14-17) are important for the encoding of FM data. If the data being written is not an address mark (there are no missing clocks specified), the data encoding multiplexer selects SHIFTCLKTT as the data source during the clock window. The data encoding multiplexer output, WDTA-, is active low, so SHIFTCLKTT low (states 8-B) is the 0.6667 microsecond clock pulse at the beginning of the FM bit frame.

During the data window, SHIFTCLKTT is again selected for output if the PRESENT data bit at the extension register output is a 1. Therefore, SHIFTCLKTT low during states 14-17 is the output data pulse if a data 1 is being recorded. If the PRESENT bit is a 0, a high level (no pulse) is gated through the data encoding multiplexer. The SHIFTDTA pulse is issued at state 16 and latched (SHIFTDTAQ) at state 17. SHIFTDTAQ shifts the CRC register, the data shift register, and the extension register, moving the next data bit to the PRESENT position of the extension register.

SHIFTCLKQ (the synchronized version of SHIFTCLKTT) and SHIFTDTAQ serve as inputs to the word controller, which shifts the clock shift register and keeps track of word boundaries.

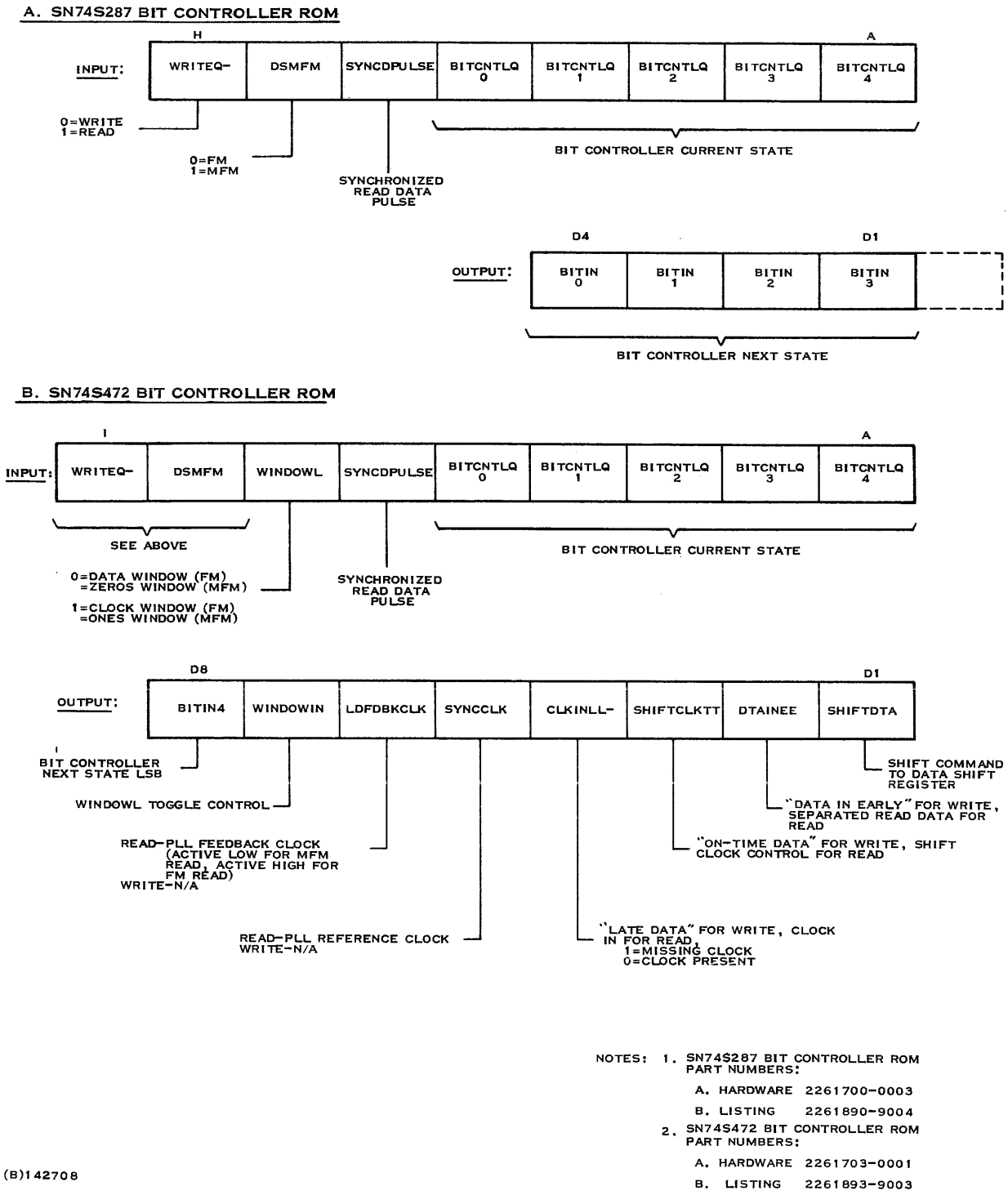


Figure 2-60. Input and Output Bit Assigments for Bit Controller ROMs

Table 2-28. Bit Controller SN74S287 ROM Listing

Hex State	Input Address									
00-07	000-007	LLLL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	008-015	LHLL	LHLH	LHLH	LHHL	LHHL	LHHH	LHHH	HLLL	Data
10-17	016-023	HLLL	HLLH	HLLH	HLHL	HLHL	HLHH	HLHH	LLLL	0
18-1F	024-031	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
										Write FM
00-07	032-039	LLLL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	040-047	LHLL	LHLH	LHLH	LHHL	LHHL	LHHH	LHHH	HLLL	Data
10-17	048-055	HLLL	HLLH	HLLH	HLHL	HLHL	HLHH	HLHH	LLLL	1
18-1F	056-063	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
00-07	064-071	LLLL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	072-079	LHLL	LHLH	LHLH	LLLL	LLLL	LLLL	LLLL	LLLL	Data
10-17	080-087	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	0
18-1F	088-095	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
										Write MFM
00-07	096-103	LLLL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	104-111	LHLL	LHLH	LHLH	LLLL	LLLL	LLLL	LLLL	LLLL	Data
10-17	112-119	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	1
18-1F	120-127	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
00-07	128-135	LLLL	LLLH	LLHL	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	136-143	LHLL	LHLH	LHLH	LHHL	LHHL	LHHH	LHHH	HLLL	Data
10-17	144-151	HLLL	HLLH	HLLH	HLHL	HLHL	HLHH	HLHH	HHLL	0
18-1F	152-159	HHLL	HHLH	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
										Read FM
00-07	160-167	LLLH	LLLH	LLHL	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	168-175	LHLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLH	Data
10-17	176-183	LLLH	LLLH	LLLH	LLLH	LLLH	LLLL	LLLL	LLLL	1
18-1F	184-191	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
00-07	192-199	LLLL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	200-207	LHLL	LHLH	LHLH	LHHL	LHHL	LHHH	LHHH	HLLL	Data
10-17	208-215	HLLL	HLLH	HLLH	HLHL	HLHL	HLHH	HLHH	HHLL	0
18-1F	216-223	HHLL	HHLH	HHLH	HHHL	LLLL	LLHH	HHHH	LHLL	
										Read MFM
00-07	224-231	LLHL	LLLH	LLLH	LLHL	LLHL	LLHH	LLHH	LHLL	
08-0F	232-239	LHLL	LLLH	LLLH	LLLH	LLLH	LLLH	LLLH	LLHL	Data
10-17	240-247	HHHL	HHHH	LLLL	LLLH	LLLH	LLHL	HHHL	LLHL	1
18-1F	248-255	LLLL	LLLH	LLLH	LLHL	HHHL	LLHH	HHHH	LHLL	

Figure 2-62 is a timing diagram for the write FM operation. At the transition between bit controller states 17 and 0, there are a number of switching operations. SHIFTDTAQ shifts the next data bit into the PRESENT output of the extension register. CLKSHIFT from the word controller shifts the missing clock pattern in the clock shift register. For this example, all zeros (no missing clocks) are assumed in the clock shift register. The synchronized clock/data also switches states. All of these signals are inputs to the write data encoding ROM. The ROM outputs, PATHSELA and PATHSELB steer the write data encoding multiplexer. These outputs are not stable until all ROM inputs are stable and the ROM access time expires.

Table 2-29. Bit Controller SN74S472 ROM Listing

Hex State	Input Address	Write FM Submachine				
00-03	000-003	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
04-07	004-007	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
08-0B	008-011	HHLLLLLL	LHLLLLLL	HHLLLLLL	LLLLLLLL	
0C-0F	012-015	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
						Data = 0
10-13	016-019	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
14-17	020-023	HLLLLLLL	LLLLLLLL	HLLLLLLH	LHLLLLLL	
18-1B	024-027	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	028-031	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
						WINDOWL = 0
00-03	032-035	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
04-07	036-039	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
08-0B	040-043	HHLLLLLL	LHLLLLLL	HHLLLLLL	LLLLLLLL	
0C-0F	044-047	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
						Data = 1
10-13	048-051	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
14-17	052-055	HLLLLLLL	LLLLLLLL	HLLLLLLH	LHLLLLLL	
18-1B	056-059	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	060-063	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
00-03	064-067	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
04-07	068-071	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
08-0B	072-075	HHLLLLLL	LHLLLLLL	HHLLLLLL	LLLLLLLL	
0C-0F	076-079	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
						Data = 0
10-13	080-083	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
14-17	084-087	HLLLLLLL	LLLLLLLL	HLLLLLLH	LHLLLLLL	
18-1B	088-091	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	092-095	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
						WINDOWL = 1
00-03	096-099	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
04-07	100-103	HHLLLHLL	LHLLLHLL	HHLLLHLL	LHLLLHLL	
08-0B	104-107	HHLLLLLL	LHLLLLLL	HHLLLLLL	LLLLLLLL	
0C-0F	108-111	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
						Data = 1
10-13	112-115	HLLLLHLL	LLLLLHLL	HLLLLHLL	LLLLLHLL	
14-17	116-119	HLLLLLLL	LLLLLLLL	HLLLLLLH	LHLLLLLL	
18-1B	120-123	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	124-127	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	

Table 2-29. Bit Controller SN74S472 ROM Listing (Continued)

Hex State	Input Address	Write MFM Submachine*		
00-03	128-131	HLLLHHLL LLLLHLLL HLLLXLLL LLLLLLLL	Data = 0	WINDOWL = 0
04-07	132-135	HLLLLLHL LHLLLHHL HHLLHHLL LHLLHLLL		
08-0B	136-139	HHLLXLLL LHLLLLLL HHLLLLHH LLLLLHHL		
0C-0F	140-143	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
10-13	144-147	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
14-17	148-151	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
18-1B	152-155	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	156-159	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
00-03	160-163	HLLLHHLL LLLLHLLL HLLLXLLL LLLLLLLL	Data = 1	
04-07	164-167	HLLLLLHL LHLLLHHL HHLLHHLL LHLLHLLL		
08-0B	168-171	HHLLXLLL LHLLLLLL HHLLLLHH LLLLLHHL		
0C-0F	172-175	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
10-13	176-179	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
14-17	180-183	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
18-1B	184-187	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1B	188-191	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
00-03	192-195	HLLLHHLL LLLLHLLL HLLLXLLL LLLLLLLL	Data = 0	WINDOWL = 1
04-07	196-199	HLLLLLHL LHLLLHHL HHLLHHLL LHLLHLLL		
08-0B	200-203	HHLLXLLL LHLLLLLL HHLLLLHH LLLLLHHL		
0C-0F	204-207	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
10-13	208-211	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
14-17	212-215	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
18-1B	216-219	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	220-223	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
00-03	224-227	HLLLHHLL LLLLHLLL HLLLXLLL LLLLLLLL	Data = 1	
04-07	228-231	HLLLLLHL LHLLLHHL HHLLHHLL LHLLHLLL		
08-0B	232-235	HHLLXLLL LHLLLLLL HHLLLLHH LLLLLHHL		
0C-0F	236-239	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
10-13	240-243	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
14-17	244-247	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
18-1B	248-251	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	252-255	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		

Note: * ROM locations marked with an X are low for the ROM used on TFDC 2261690, high for the ROM used on fineline TFDC 2267295. The high output, with SN74LS74 F/F UKD077 (sh 17) provides 250 nsec precompensation.

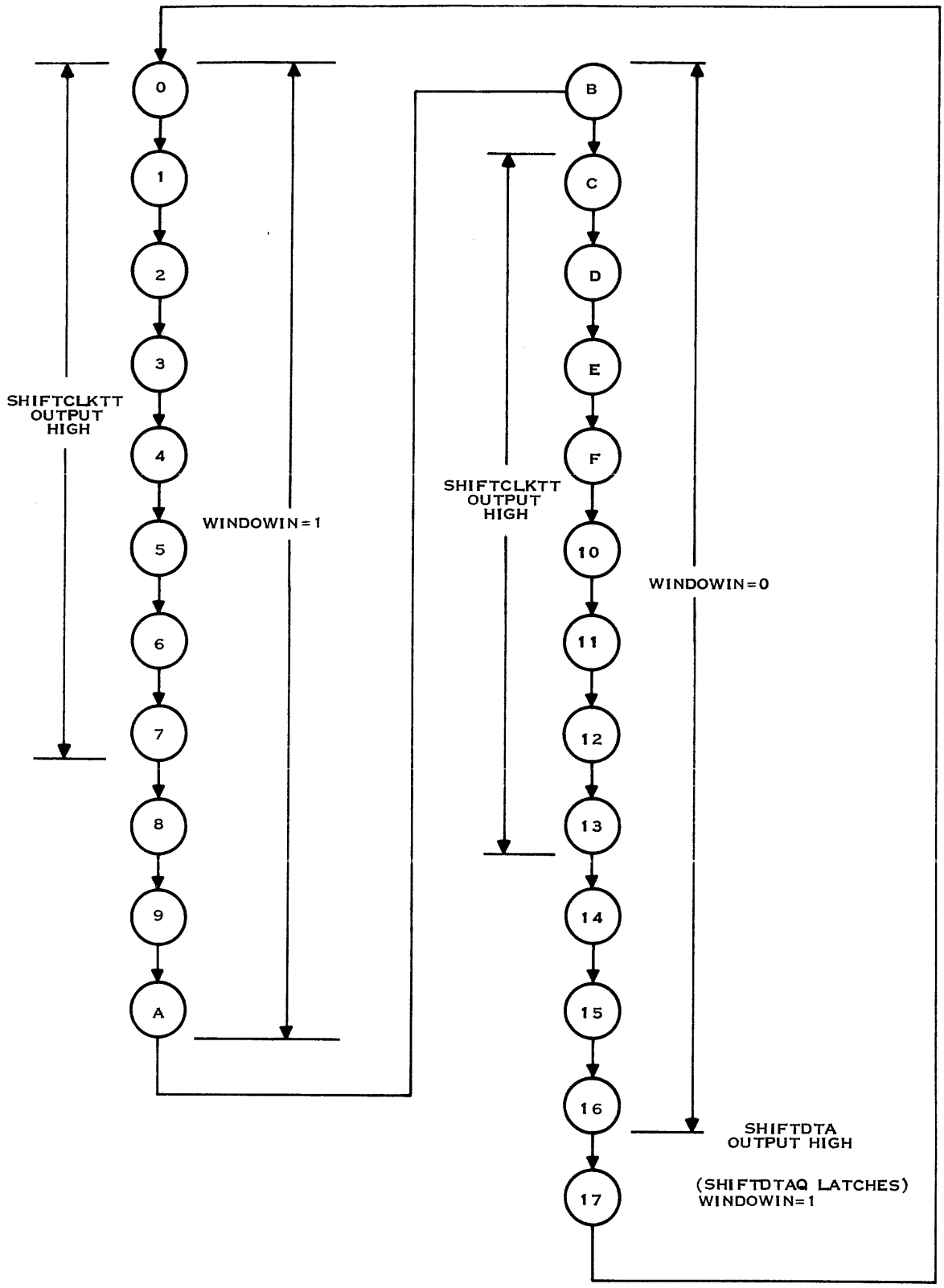
Table 2-29. Bit Controller SN74S472 ROM Listing (Continued)

Hex State	Input Address	Read FM Submachine				
00-03	256-259	LLLLLLLL	LLLHLLLL	HLHLLLLL	LLHLLLLL	WINDOWL = 0, Data = 0
04-07	260-263	HLLHLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
08-0B	264-267	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
0C-0F	268-271	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
10-13	272-275	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
14-17	276-279	HHLLLLLH	LLLLLLLL	HLLLLLLL	LLLLLLLL	
18-1B	280-283	HLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	284-287	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
00-03	288-291	HHLLLLHH	LLLHLLLL	HLHLLLLL	LLHLLLLL	WINDOWL = 0, Data = 1
04-07	292-295	HLLHLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
08-0B	296-299	HLLLLLLL	HHLLLLHH	HHLLLLHH	HHLLLLHH	
0C-0F	300-303	HHLLLLHH	HHLLLLHH	HHLLLLHH	HHLLLLHH	
10-13	304-307	HHLLLLHH	HHLLLLHH	HHLLLLHH	HHLLLLHH	
14-17	308-311	HHLLLLHH	HHLLLHHH	HHLLLHHH	HHLLLLHH	
18-1B	312-315	HHLLLLHH	HHLLLLHH	HHLLLLHH	LLLLLLLL	
1C-1F	316-319	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
00-03	320-323	LLLLLLLL	LLLHLLLL	HLHLLLLL	LLHLLLLL	WINDOWL = 1, Data = 0
04-07	324-327	HLLHLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
08-0B	328-331	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
0C-0F	332-335	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
10-13	336-339	HLLLLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
14-17	340-343	HHLLHHLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
18-1B	344-347	HLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
1C-1F	348-351	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	
00-03	352-355	HHLLLHLL	LLLHLLLL	HLHLLLLL	LLHLLLLL	WINDOWL = 1, Data = 1
04-07	356-359	HLLHLLLL	LLLLLLLL	HLLLLLLL	LLLLLLLL	
08-0B	360-363	HLLLLLLL	HHLLLHLL	HHLLLHLL	HHLLLHLL	
0C-0F	364-367	HHLLLHLL	HHLLLHLL	HHLLLHLL	HHLLLHLL	
10-13	368-371	HHLLLHLL	HHLLLHLL	HHLLLHLL	HHLLLHLL	
14-17	372-375	HHLLLHLL	HHLLLHLL	HHLLLHLL	HHLLLHLL	
18-1B	376-379	HHLLLHLL	HHLLLHLL	HHLLLHLL	LLLLLLLL	
1C-1F	380-383	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL	

Table 2-29. Bit Controller SN74S472 ROM Listing (Continued)

Hex State	Input Address	Read MFM Submachine				
00-03	384-387	LLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
04-07	388-391	HLLLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
08-0B	392-395	HLHLLLLL	LLHLLLLL	HLHLLHLH	LLHLLLLL	
0C-0F	396-399	HLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
						Data = 0
10-13	400-403	HLHLLLLL	LHHLLLLL	HLHLLLLL	LLHLLLLL	
14-17	404-407	HLHLLLLL	LLHLLLLL	HLHLLLLL	LHHLLLLL	
18-1B	408-411	HLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
1C-1F	412-415	LLHLLLLL	LLHHLLLL	HLHLLLLL	LLHHLLLL	
						WINDOWL = 0
00-03	416-419	LLLHLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
04-07	420-423	HLLLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
08-0B	424-427	HLHLLLLL	LLHHLLLL	LLHHLLLL	LLHHLLLL	
0C-0F	428-431	HLHHLLLL	LLHHLLLL	HLHHLLLL	LLLHLLLL	
						Data = 1
10-13	432-435	HLLLLLLL	LLLLLLLL	HLHHLLLL	LLHHLLLL	
14-17	436-439	HLHHLLLL	LLLHLLLL	HLLLLLLL	LLLHLLLL	
18-1B	440-443	HLHHLLLL	LLHHLLLL	HLHHLLLL	LLLHLLLL	
1C-1F	444-447	HLLLLLLL	LLHHLLLL	HLHLLLLL	LLHHLLLL	
00-03	448-451	LLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
04-07	452-455	HLLLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
08-0B	456-459	HLHLLLLL	LLHLLLLL	HLHLLHHH	LLHLLLLL	
0C-0F	460-463	HLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
						Data = 0
10-13	464-467	HLHLLLLL	LHHLLHLH	HLHLLLLL	LLHLLLLL	
14-17	468-471	HLHLLLLL	LLHLLLLL	HLHLLLLL	LHHLHHLH	
18-1B	472-475	HLHLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
1C-1F	476-479	LLHLLLLL	LLHHLLLL	HLHLLLLL	LLHHLLLL	
						WINDOWL = 1
00-03	480-483	LLLHLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
04-07	484-487	HLLLLLLL	LLHLLLLL	HLHLLLLL	LLHLLLLL	
08-0B	488-491	HLHLLLLL	LLHHLLLL	LLHHLLLL	LLHHLLLL	
0C-0F	492-495	HLHHLLLL	LLHHLLLL	HLHHLLLL	LLLHLLLL	
						Data = 1
10-13	496-499	HLLLLLLL	LLLLLLLL	HLHHLLLL	LLHHLLLL	
14-17	500-503	HLHHLLLL	LLLHLLLL	HLLLLLLL	LLLHLLLL	
18-1B	504-507	HLHHLLLL	LLHHLLLL	HLHHLLLL	LLLHLLLL	
1C-1F	508-511	HLLLLLLL	LLHHLLLL	HLHLLLLL	LLHHLLLL	

SHIFTCLKTT is gated through the multiplexer as the WDTA- output. There is one more stage of synchronization to eliminate the period of multiplexer instability from the output waveform, WRDAT-. SHIFTCLKTT and the clock/data window both change on the state B to C transition. The active-low WDTA- multiplexer output is the clock pulse that marks the beginning of an FM bit frame. Assuming that the data bit to be recorded (PRESENT) is a 1, the write data encoding multiplexer continues to select SHIFTCLKTT after the clock/data window transition. SHIFTCLKTT goes low at state 14 to supply the data pulse, and remains low until state 0. The synchronized WDATA- output lags one PLL clock period (one state) behind the multiplexer output.



(A)142711

Figure 2-61. Bit Controller Write FM State Diagram

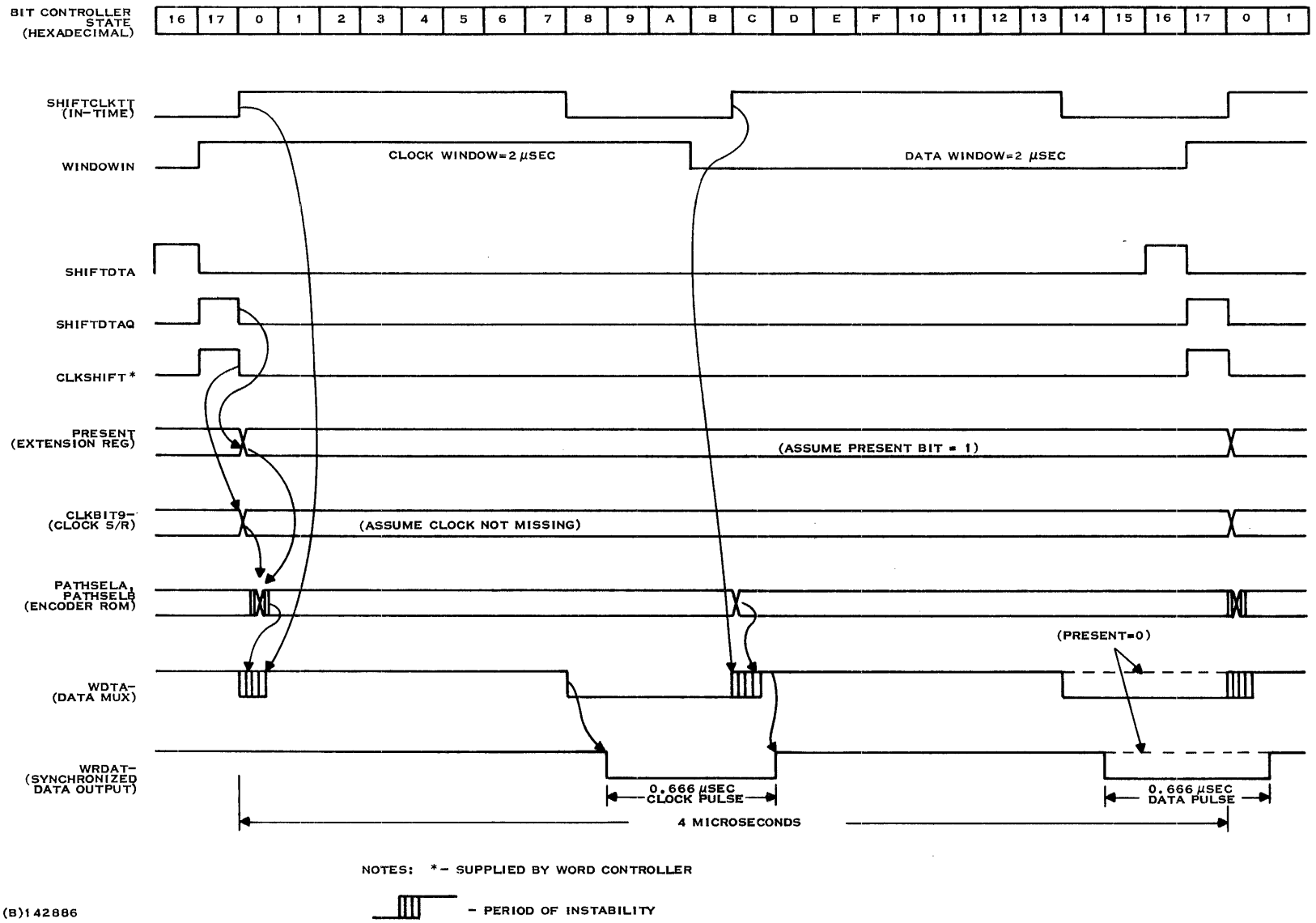


Figure 2-62. Write FM Timing

Bit Controller Write MFM State Diagram. Refer to Figure 2-63, the write MFM state diagram, for this description. It may also be helpful to refer back to part B of Figure 2-54, which shows the MFM data encoding rules.

Twelve bit controller states are used for MFM write operations. The 12 states, numbered 0-B, follow a straight numerical sequence (0,1,2, ... B,0) with no branches. The state advances on the trailing edge of each PLL clock pulse. Each state is active for 166.66 nanoseconds (minus ROM access time), at the crystal-controlled 6 MHz clock frequency. A complete cycle of 12 states occupies 2 microseconds.

The important bit controller outputs for MFM encoding are; WINDOWIN, DTAINEE, SHIFTCLKTT, CLKINLL-, and SHIFTDTA. WINDOWIN is the clock/data window (WINDOWL) control signal. DTAINEE, SHIFTCLKTT, and CLKINLL- are the early, on-time, and late pulses required for encoding and precompensation of MFM clock and data. SHIFTDTA is the data shift command. SHIFTDA is synchronized as SHIFTDTAQ, which shifts the data shift register, the extension register, and the CRC generator.

WINDOWIN is high for states 5 through A_{16}, forcing WINDOW high for states 6 through B. For MFM, the write data and precompensation ROM decodes WINDOW high as the data window. WINDOW low is the clock window.

The DTAINEE, SHIFTCLKTT, and CLKINLL- outputs are asymmetric waveforms that are phased one state (166.66 nanoseconds) apart. SHIFTCLKTT and DTAINEE are identical except for phasing. Each of these waveforms is high for 2 states (333.33 nanoseconds) and low for four states (666.66 nanoseconds). The waveform of CLKINLL- differs between versions of the logic board. In the original 2261690 board, CLKINLL- is identical to DTAINEE and SHIFTCLKTT, except for phasing. In the 2267295 fineline board, CLKINLL- is high for 3 states (500 nanoseconds) and low for three states.

The fineline TFDC (2267295) provides 250-nanosecond precompensation when writing MFM data. The program of the SN74S472 ROM (UHB029) delays the active-low CLKINLL- by one extra state (from 01 to 02 and from 07 to 08). Also, SHIFTCLKTT is delayed 83 nanoseconds in an SN74LS74 F/F (UKD077). The delayed shift clock output is SHIFTCLKTP. The 83-nanosecond delay of SHIFTCLKTP and the 166-nanosecond delay of CLKINLL combine to provide 250 nanoseconds of early or late precompensation.

DTAINEE, SHIFTCLKTT (or SHIFTCLKTP), and CLKINLL- are inputs to the write data encoding multiplexer. Since the output of this noninverting multiplexer is the active low WDTA- signal, the low periods of these signals are of interest in data/clock encoding.

Refer to Figure 2-64, the write MFM timing diagram. The bit controller states are shown at the top. The next three entries are the late (CLKINLL-), on-time (SHIFTCLKTT), and early (DTAINEE) waveforms that are generated as the bit controller cycles through the write MFM sequence. These three waveforms (and a hardwired 1) are available at the write data encoding multiplexer inputs. Dotted lines on the CLKINLL- waveform represent the additional one-state delay on the fineline board.

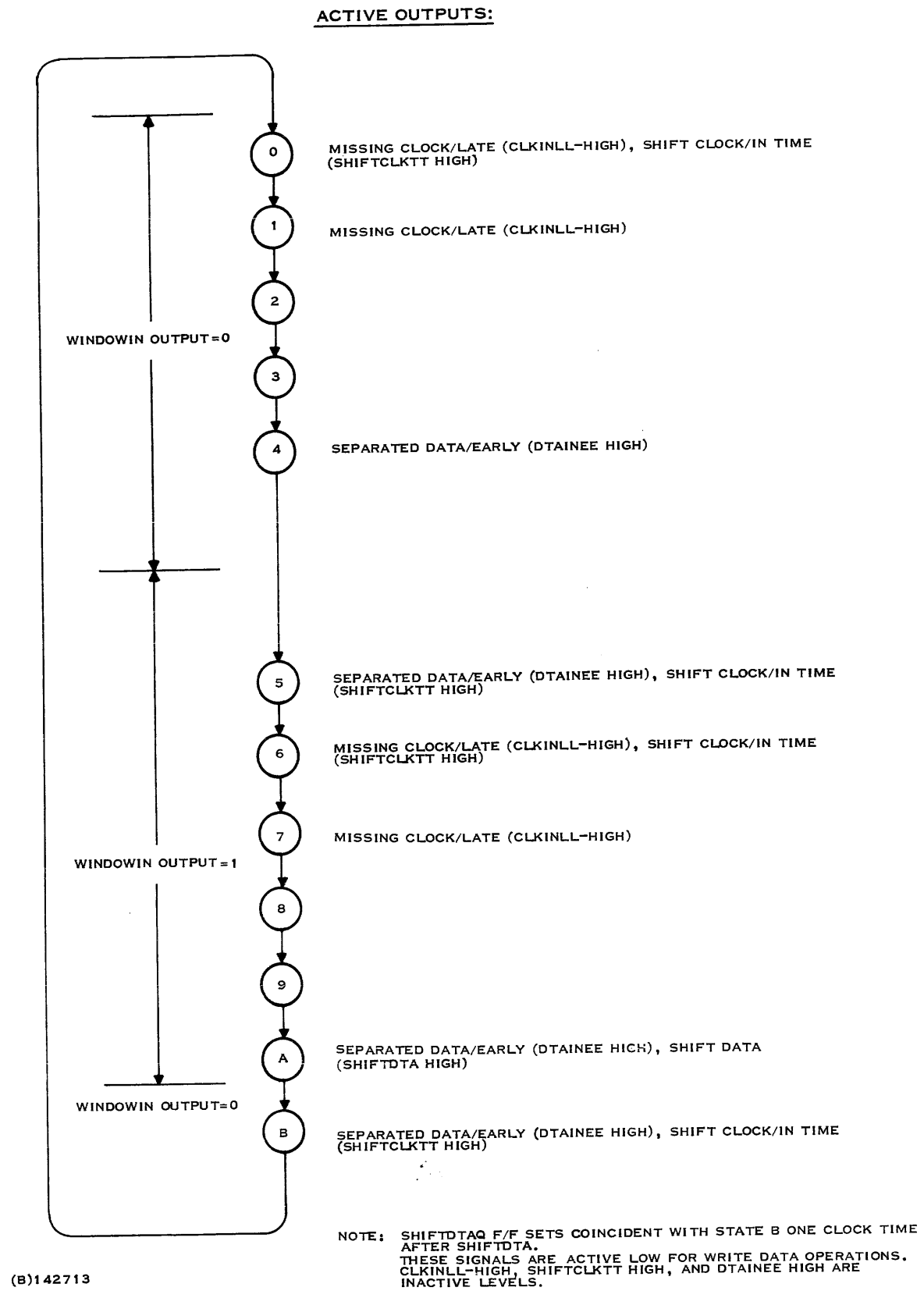
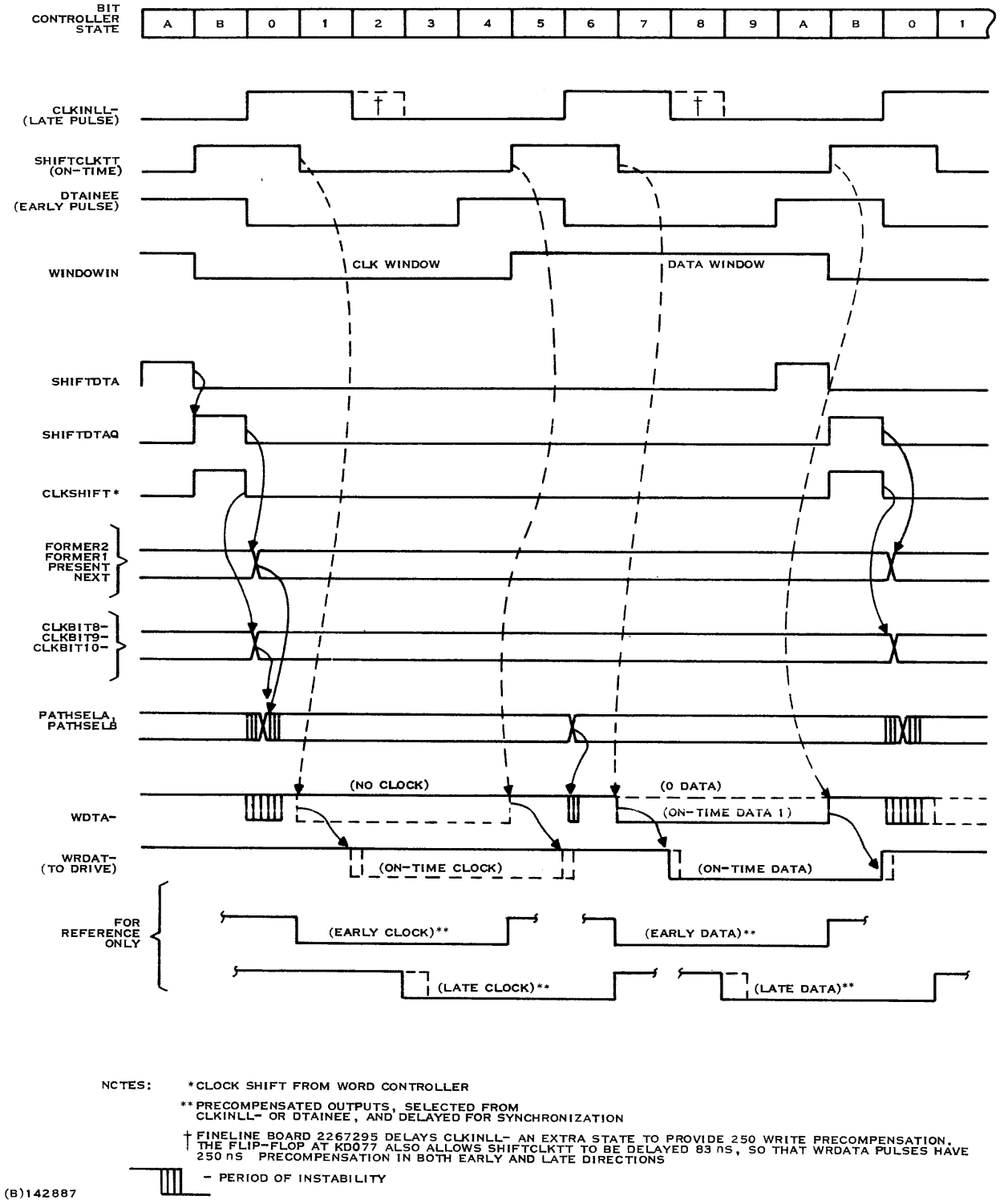


Figure 2-63. Bit Controller Write MFM State Diagram



NOTES: *CLOCK SHIFT FROM WORD CONTROLLER

**PRECOMPENSATED OUTPUTS, SELECTED FROM CLKINLL- OR DTAINEE, AND DELAYED FOR SYNCHRONIZATION

† FINELINE BOARD 2267295 DELAYS CLKINLL- AN EXTRA STATE TO PROVIDE 250 WRITE PRECOMPENSATION, THE FLIP-FLOP AT KD077 ALSO ALLOWS SHIFTCLKTT TO BE DELAYED 83 nS, SO THAT WRDATA PULSES HAVE 250 nS PRECOMPENSATION IN BOTH EARLY AND LATE DIRECTIONS

- PERIOD OF INSTABILITY

(B)142887

Figure 2-64. Write MFM Timing

A SHIFTDTA pulse is issued every state A, and is synchronized (SHIFTDTAQ) one clock time later. The SHIFTDTAQ pulse right-shifts the extension register, changing the FORMER2, FORMER1, PRESENT, and NEXT data bit inputs to the write data encoding and precompensation ROM. The clock/data window (WINDOW), controlled by WINDOWIN, is another input to the write data encoding and precompensation ROM.

A CLKSHIFT pulse from the word controller shifts the missing clock pattern (if any) in the clock shift register. In the absence of missing clocks (not writing an address mark), CLKBIT(8–10)– remain low. The DSPRECOMP signal, which is omitted from the diagram, is either high or low for the whole track. It does not change during the course of encoding data.

The PATHSELA and PATHSELB outputs of the write data encoding and precompensation ROM control the selection of the hardwired 1 (no pulse), early, on-time, or late. PATHSELA and PATHSELB do not stabilize until all the ROM inputs have stabilized and the access time has expired. Thus, there is glitching on the WDTA– line, which is eliminated by synchronization in the WRDAT– F/F.

The path selection also changes on the clock/data window change at the center of the bit frame. The write data waveforms may have either a clock pulse or a data pulse in the bit frame, but not both. The MFM encoding rules allow a clock pulse only between successive data zeros. In the absence of precompensation, an on-time clock pulse or an on-time data pulse, or no pulse may occur. With precompensation, the clock or the data pulse may appear early, on-time, or late.

The timing diagram shows an on-time clock pulse, with an on-time data pulse shown as a dotted outline. The positions of the other possible output pulses are also shown, and are labeled "for reference only". More information on write data encoding and precompensation is given with the description of these circuits.

Read FM State Diagram. The bit controller operating sequences for read FM and read MFM are not as simple as the write sequences. The bit controller must proceed numerically through the sequence in the absence of an input pulse (SYNCDPULSE) and must branch when the pulse occurs. The bit controller branch determines whether an input SYNCDPULSE represents clock or data, in order to correctly shift the clock or data shift register. Also, the bit controller determines where the input pulse falls with respect to the clock or data window, and issues the PLL reference and feedback pulses that keep the PLL clock at the proper frequency. An accurate PLL clock and the window controls issued by the bit controller keep the clock/data window phase centered on the incoming waveform. Erroneous reversal of the clock/data window is corrected by the phase correction ROM based on missing clocks detected by the bit controller.

Refer to the bit controller read FM state diagram, Figure 2-65. The bit controller divides the incoming bit frame into a two-microsecond window and a four-microsecond window. An incoming pulse (SYNCDPULSE) is never on-time. It is either early in the two-microsecond window, late in the two-microsecond window, early in the four-microsecond window or late in the four-microsecond window. These windows are all measured from the previous SYNCDPULSE.

Any SYNCDPULSE that occurs early in either window causes the bit controller to branch to state 1 and to follow an X-1-2-5 sequence. A SYNCDPULSE that occurs late in a window causes the bit controller to branch to state 3 and to follow an X-3-4-5 sequence. "X" represents the bit controller state at the time that the SYNCDPULSE occured. The early and late entry paths are dedicated to controlling the PLL clock by issuing the reference pulse (SYNCCLK) and the feedback pulse (LDFDBKCLK). These outputs are synchronized to PLL clock as SYNCCLKQ and LDFDBKCLKQ, and are sent to the MC4044 digital phase detector.

Refer to Figure 2-66 which shows the PLL control signals and the resulting pumping action by the MC4044 device. Part A shows the waveforms for an early entry. An early entry means that the SYNCDPULSE was detected early in the window, implying that the clock is running slow. The bit controller issues SYNCCLK at state 1 and LDFDBKCLK at state 2. The synchronized outputs go to the MC4044 after a one clock period delay.

The MC4044 compares the negative-going (trailing) edges of the reference and feedback pulses. The reference leads; therefore, the D1 output (PU00) remains inactive (high), and the U1 output (PD00) goes low for the period between the reference edge and the feedback edge. This output is an active-low frequency pump-up signal that tends to drive the frequency upward.

Part B of Figure 2-66 shows the effects of a late entry in the window. SYNCDPULSE late in the window implies that the PLL clock is running too fast and advancing the window phase with respect to the incoming waveform. LDFDBKCLKQ is issued one state before SYNCCLKQ for an early entry. The U1 output (PD00) remains high and the low D1 output (PU00) tends to drive the frequency downward.

Damping in the phase lock loop slows down the loop frequency response so that the control voltage to the VCO represents an average of the pump-up and pump-down pulses. If early entries exceed late entries on the average, the VCO output frequency (PLLCLK) increases and advances the window. If late entries exceed early entries, the window is retarded.

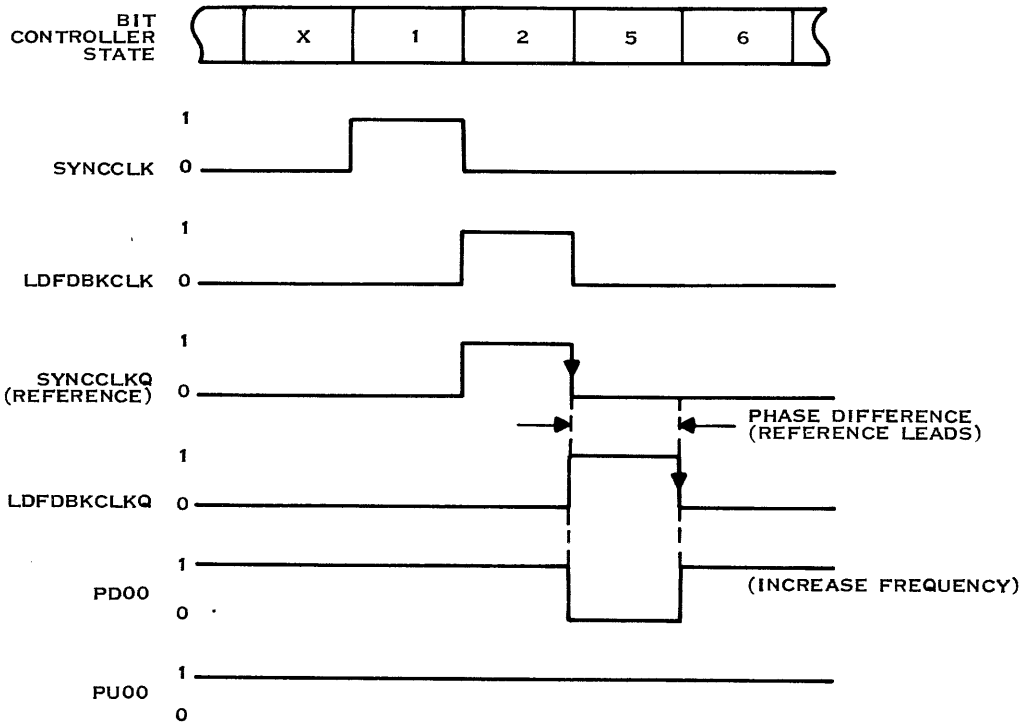
Refer back to the read FM state diagram. Note that the states are divided into groups of six. If the PLL clock is running at exactly six MHz, a group of six states represents a one-microsecond interval.

Any SYNCDPULSE that occurs during a 1-2-5...8 or a 3-4-5...8 interval is ignored. The six states of either path represent the first microsecond after a data or clock pulse. Valid FM pulses cannot have a spacing that small.

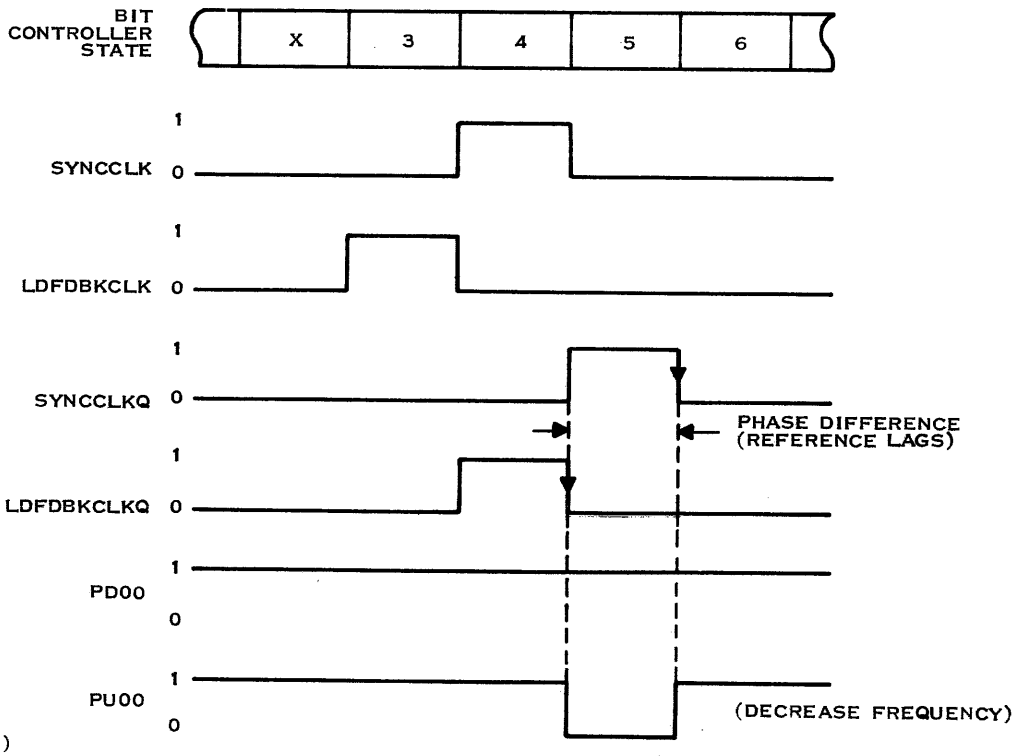
States 9 through E are the early half of the two-microsecond window, as measured from the previous SYNCDPULSE. The bit controller steps through one state per clock pulse in the absence of a SYNCDPULSE. Any SYNCDPULSE in the early half of this window forces a branch to the early entry point. The bit controller outputs that go active on this branch are identical for states 9 through E.

For this branch, the SHIFTCLKTT output is equal to WINDOWL, and the SHIFTDTA output is WINDOWL complemented. Therefore, a clock shift is issued during a clock window or a data shift is issued during a data window. An output of WINDOWIN = 1 toggles the window (unless the phase correction ROM issues a CHANGEPULSE).

A. EARLY ENTRY

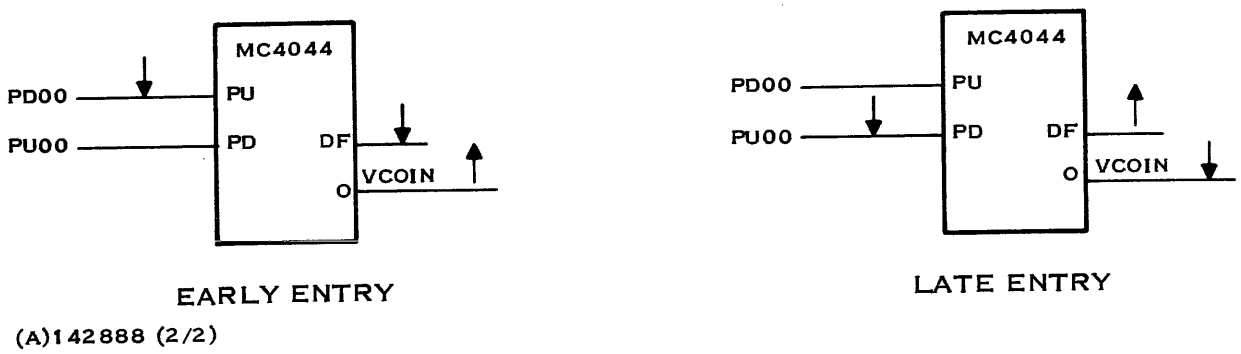


B. LATE ENTRY



(A)142888(1/2)

Figure 2-66. PLL Corrections for Read FM (Sheet 1 of 2)



(A)142888 (2/2)

Figure 2-66. PLL Corrections for Read FM (Sheet 2 of 2)

The separated data output, DTAINEE, is 1; but this has no effect unless accompanied by a SHIFTDTA pulse. Similarly, the missing clock pulse signal, CLKINLL-, is forced to 0 (clock pulse present), which has no effect unless SHIFTCLKTT is also 1.

From this description, it is clear that the clock/data window determines the treatment of any SYNCDPULSE that occurs during the first half of the two-microsecond window. The clock or data pulse causes the clock/data window to toggle, and branches back to state 1 of the bit controller sequence (early entry).

States F through 14_{16} represent the second half of the two-microsecond window. Any SYNCDPULSE detected during this window causes a branch to state 3 (late entry). Bit controller outputs for this branch include SHIFTCLKTT = WINDOWL, SHIFTDTA = WINDOWL-, DTAINEE = 1, CLKINLL- = 1, and WINDOWIN = 1. These are the same control outputs as generated from the early half of the window. The only differences between the early and late window halves are in the destination of the SYNCDPULSE branch and in what happens if no SYNCDPULSE is detected.

If the sequence reaches the end of the two-microsecond window (state 14) with SYNCDPULSE = 0, either a zero data pulse has been read or a clock bit is missing. Bit controller state 14 outputs are; SHIFTCLKTT = WINDOWL, SHIFTDTA = WINDOWL-, DTAINEE = 0, and CLKINLL- = 1. Both the zero data pulse and the missing clock (CLKINLL-) are developed by the bit controller. The output that is accepted is determined by the clock/data window. The window is not toggled, and the sequence continues to state 15.

States 15 through 1A represent the early part of the four-microsecond window. States 15 and 16 are special cases. A SYNCDPULSE detected during either of these states causes CLKINLL- = 0 (no missing clock) to be unconditionally shifted into the clock shift register. This is a "fix" that assures that a pattern of 5, 6, or 7 missing clock pulses can correct the clock/data phase under a coincidence of worst-case conditions.

The other bit controller outputs for an early entry from state 15 or state 16 are; SHIFTDTA = W!NDOWL-, DTAINEE = 1, and WINDOWIN = 1. Thus, if the clock/data window is low, a data one is shifted and the clock/data window is toggled.

A SYNCDPULSE detected during states 17-1A causes a clock shift only during the clock window (SHIFTCLKTT = WINDOWL). A data one is shifted if the data window is active (WINDOWL = 0). The window is toggled in preparation for the next sequence.

If the bit controller reaches the end of the sequence (state 0) with no SYNCDPULSE, it enters a self-loop until a SYNCDPULSE finally occurs. The exit from this self-loop is treated as a late entry from the four-microsecond window. A data one (DTAINEE = 1) or clock present (CLKINLL- = 0) signal is shifted, depending on the clock/data window, and then the window is toggled to the opposite phase.

Refer to Figure 2-67, which shows sample timing for a read FM operation. This timing diagram assumes a certain set of input pulse positions, and shows the sequences executed for these pulses. Different pulse patterns and spacings will cycle through different bit controller states. For example, if the pulse shown at state 1A had arrived any later, it would have been treated as a late clock pulse. No matter what the position of the pulse, it always restarts the bit controller sequence at state 1 or state 3. Notice that the bit controller only toggles the clock/data window; it does not ever force it to a specified state. The phase change command from the address mark detection and phase correction logic corrects window errors, based on missing clock pulses.

Bit Controller Read MFM State Diagram. Refer to Figure 2-68, the bit controller read MFM state diagram. This sequence requires all of the 32 possible bit controller states. In the absence of an input pulse (SYNCDPULSE), the bit controller steps through the states in numerical order, one state per PLL clock pulse. The last state (state 0) is a wait state that, if reached, self-loops until an active SYNCDPULSE occurs.

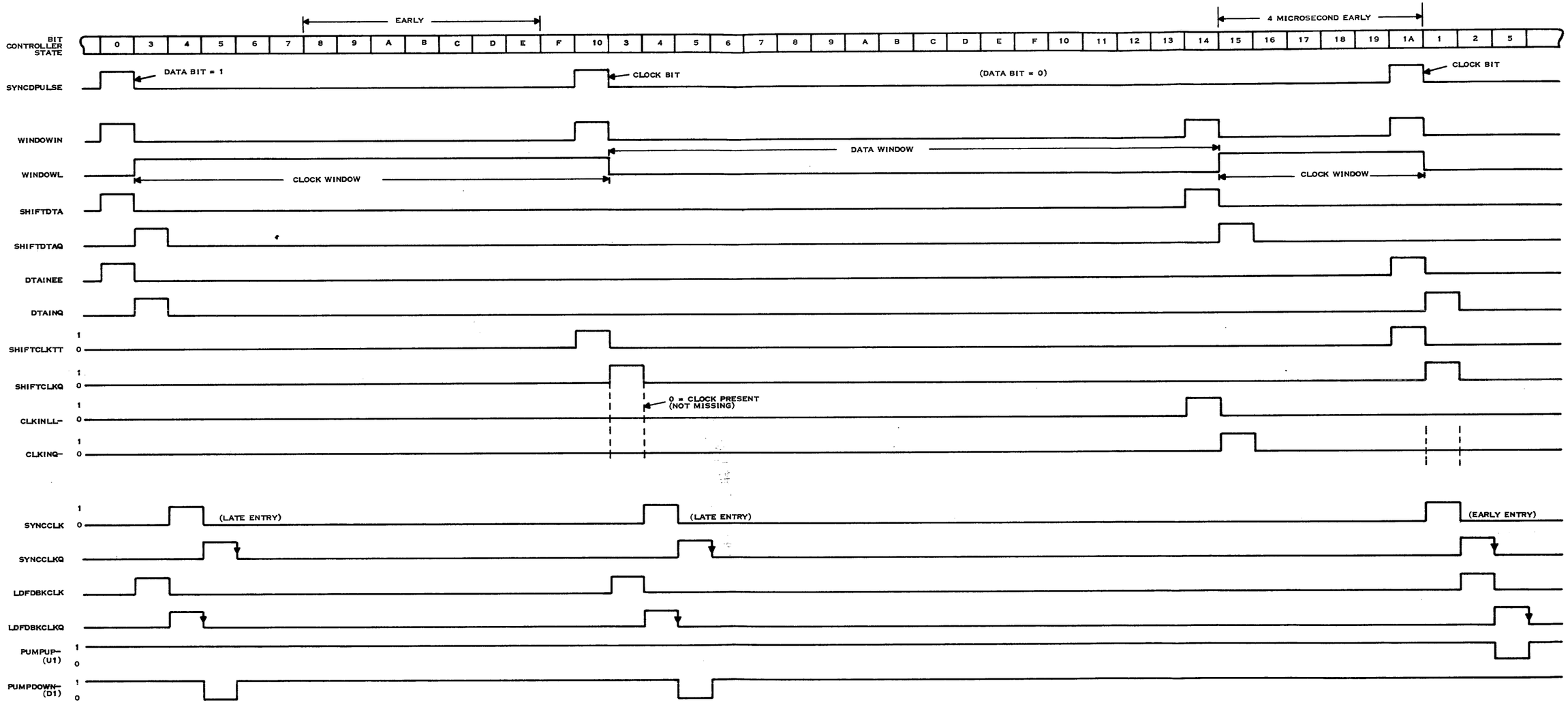
A pulse on the SYNCDPULSE input is an unseparated clock or data pulse from the read data input circuits. An active SYNCDPULSE causes a branch from the main sequence back to one of the entry points. The entry point determines what frequency corrections are issued to the PLL clock circuit; the individual branch determines what control, clock, and separated data outputs are issued.

The bit controller sequence is divided into a two-microsecond window, a three-microsecond window, and a four-microsecond window. Each window consists of six states. Unlike FM read operations, each state within a window has an individual branch back to one of the entry points. The bit controller outputs depend on both the window and the individual state within the window when the SYNCDPULSE occurs.

There is no on-time condition for an incoming data pulse. The pulse is always considered to fall into one of the early or late positions within the window. Each position refers control back to one of the entry points. Corrections to the PLL clock circuit are determined by the entry point. These corrections are described in subsequent paragraphs.

There are six entry points in the bit controller sequence as follows:

Entry	State
Early 1 (E1)	3
Early 2 (E2)	2
Early 3 (E3)	1
Late 1 (L1)	4
Late 2 (L2)	1D
Late 3 (L3)	1E



(D)142889

Figure 2-67. Read FM Timing

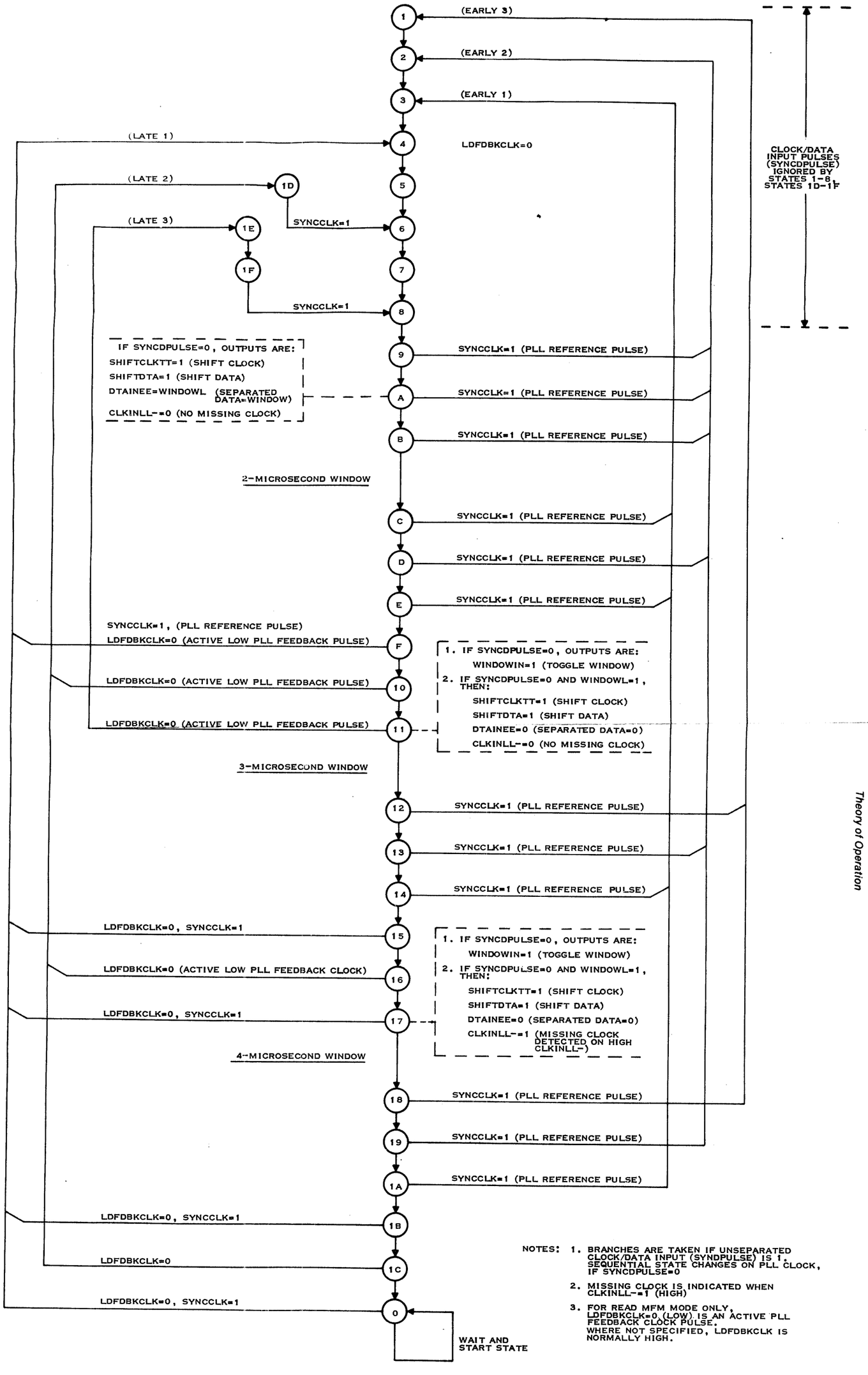


Figure 2-68. Bit Controller Read MFM State Diagram

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Do not assume that each window is necessarily divided into E1, E2, E3, L1, L2, and L3 branches. The window partitions are not treated symmetrically because of bit-shifting effects and because of MFM encoding rules. Detailed reasons for the asymmetrical division of windows are provided with the individual window descriptions.

SYNCDPULSE inputs are not recognized during states 1-8 or states 1D through 1F. These states represent, at maximum, less than 1.34 microseconds since the previous pulse. Two valid MFM pulses cannot occur within that interval.

Notice that state 8 is always executed, regardless of entry point. Also, note that the number of states executed between entry and state 8 differs between the entry points. These differences are;

Entry	Number of states
E3	7
E2	6
E1	5
L1	4
L2	3
L1	2

These differences are important because they provide a means for adjusting the whole bit controller sequence in time, depending on when the last SYNCDPULSE occurred. This means that the starting point of the two-microsecond window may be adjusted by up to a microsecond (six states), with a corresponding adjustment to the three- and four-microsecond windows.

All branches to an early entry include a SYNCCLK = 1 output that enables a reference pulse to the PLL circuit (at the next clock time). Also, all of these branches force the sequence to pass through state 4, enabling a LDFDBKCLK = 0 output. One clock time later, the synchronized LDFDBKCLKQ feedback pulse goes low.

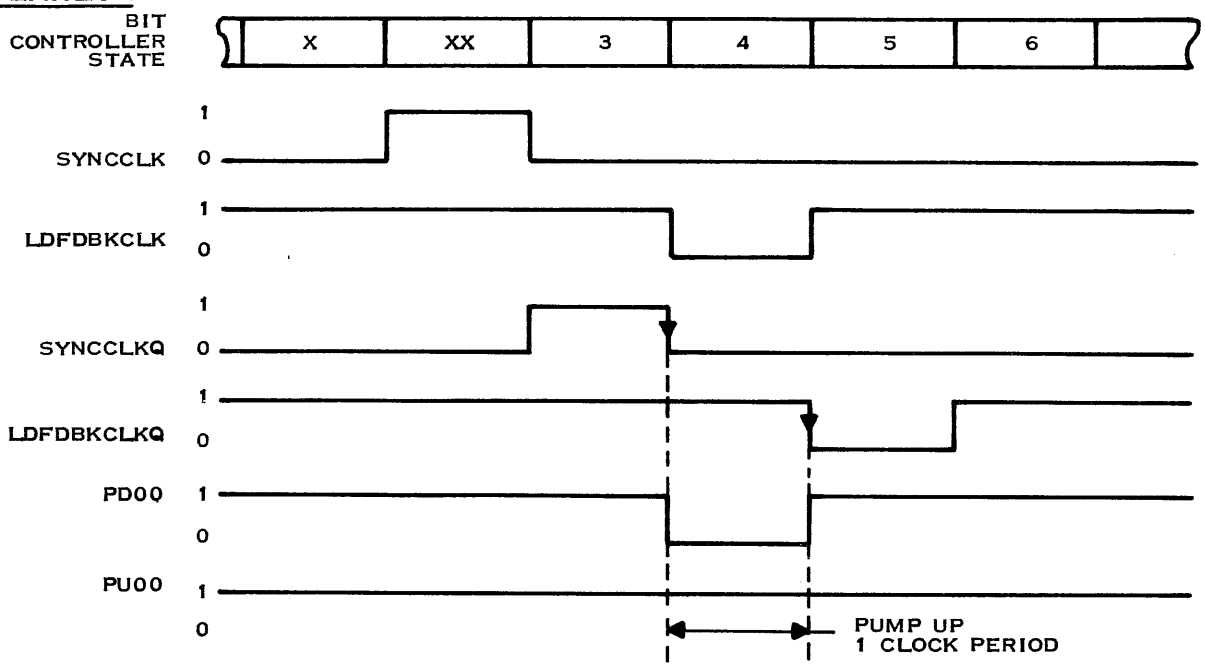
The MC4044 device measures phase between negative-going (falling) edges of SYNCCLKQ and LDFDBKCLKQ. For read MFM, this phase difference is measured between the trailing edge of the SYNCCLKQ pulse and the leading edge of the low LDFDBKCLKQ pulse. Thus, LDFDBKCLKQ may be considered active low during the read MFM sequence.

All branches to a late entry include a LDFDBKCLK = 0 output that enables a low feedback pulse on the next clock pulse. Branches to the late 1 (L1) entry point supply a simultaneous reference pulse, SYNCCLK. Entry points L2 and L3 provide a SYNCCLK output after one or two states, respectively.

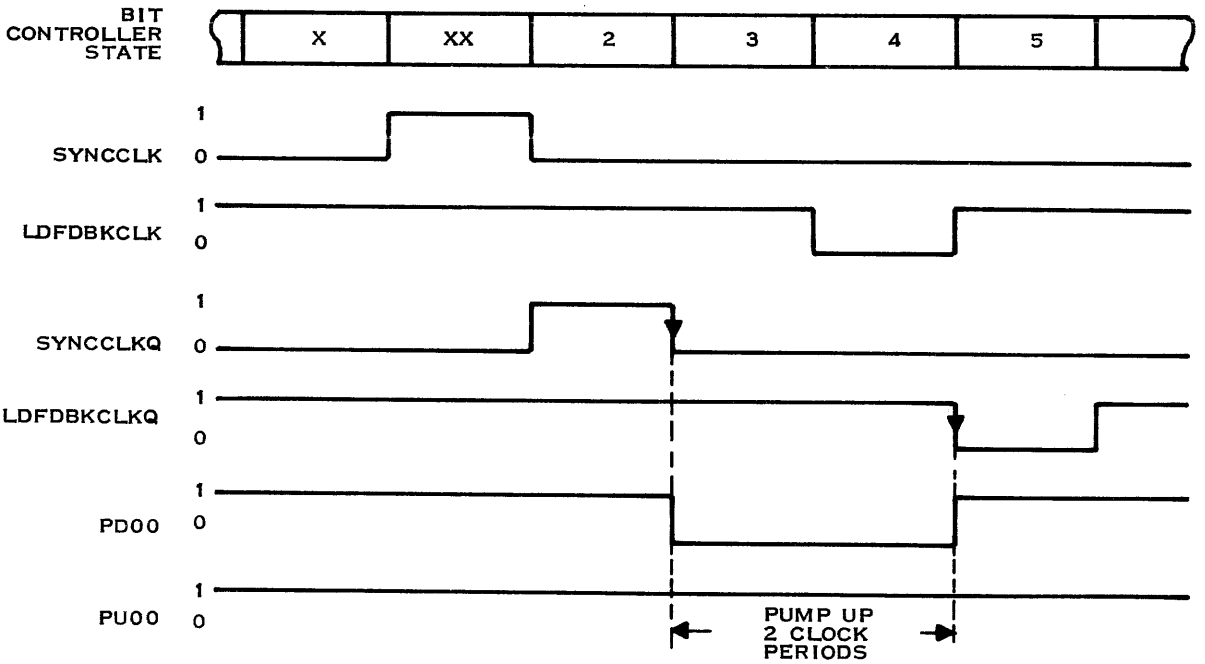
Refer to Figure 2-69. This figure is divided into parts A-F with each part showing the PLL corrections associated with one of the read MFM entry points. In each case, state XX is the bit controller state at the time SYNCDPULSE occurs, and state X is the previous state.

If a SYNCDPULSE causes a branch to the early 1 (E1) entry point, a one clock period pump-up pulse is issued. A branch to E2 enables a two-period pump-up pulse, and a branch to E3 enables a three-period pump-up pulse. Branches to L1, L2, and L3 enable a one, two, or three-period pump-down pulse, respectively.

A. EARLY 1



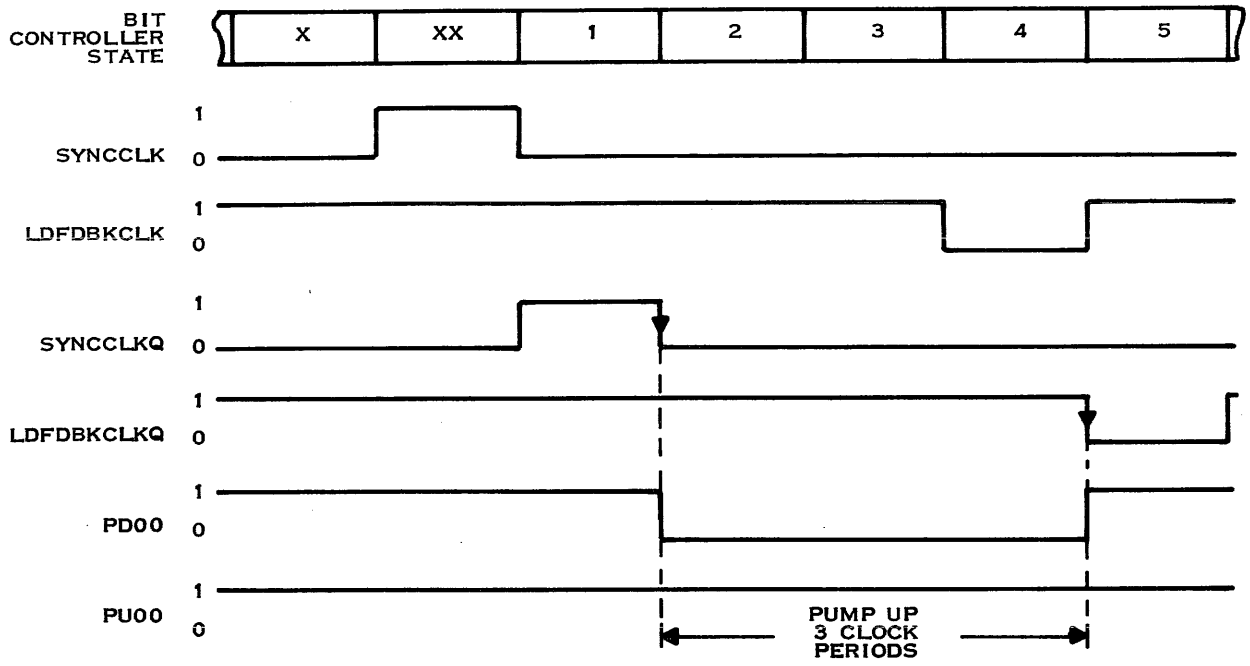
B. EARLY 2



(A)142890 (1/4)

Figure 2-69. PLL Corrections for Read MFM (Sheet 1 of 4)

C. EARLY 3



D. LATE 1

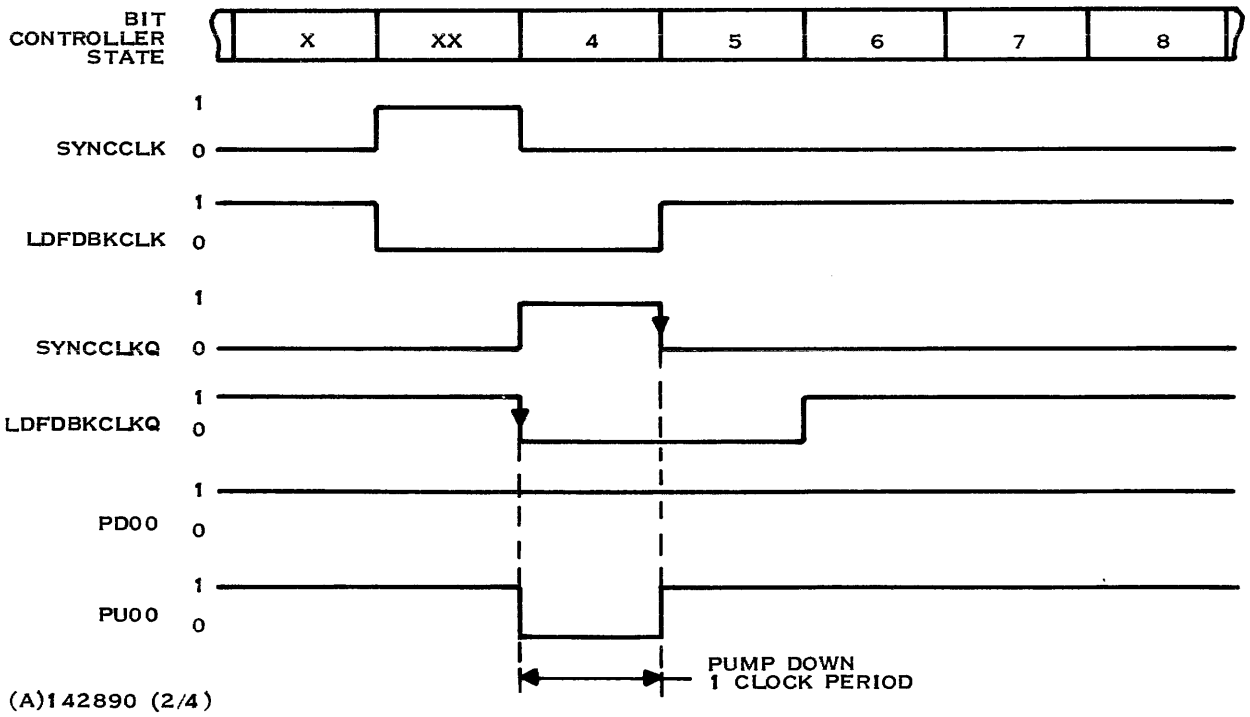
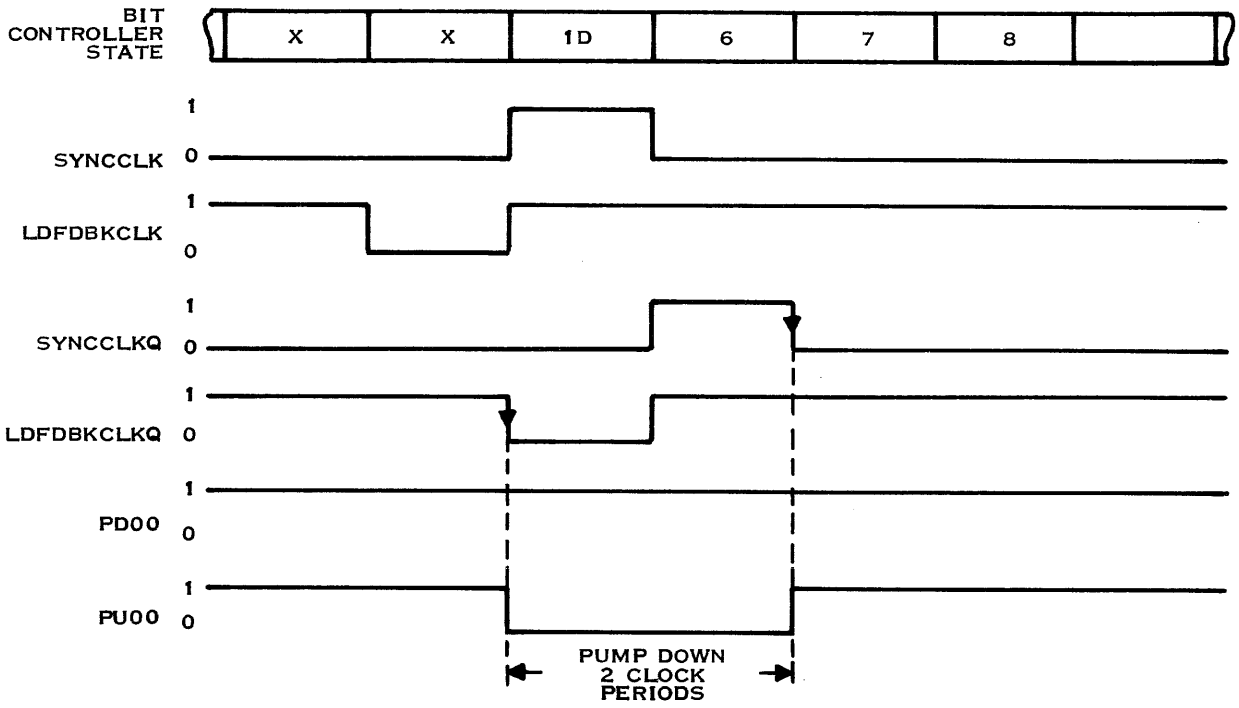
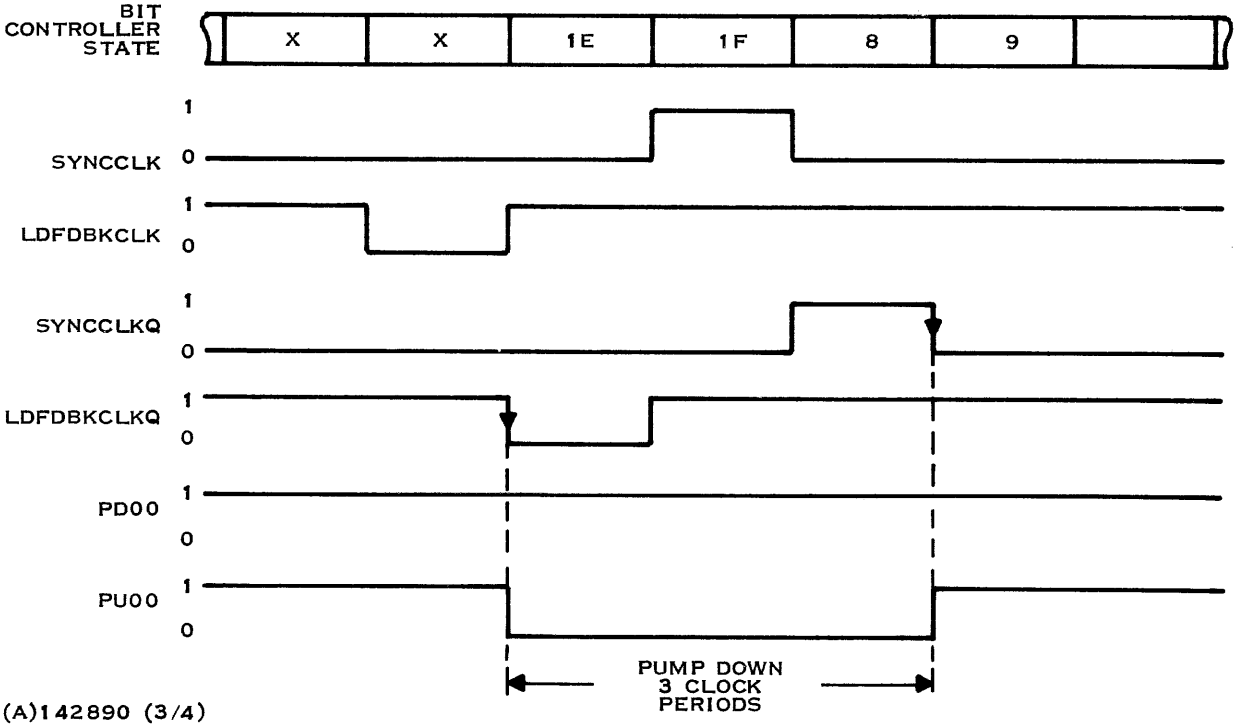


Figure 2-69. PLL Corrections for Read MFM (Sheet 2 of 4)

E. LATE 2



F. LATE 3



(A)142890 (3/4)

Figure 2-69. PLL Corrections for Read MFM (Sheet 3 of 4)

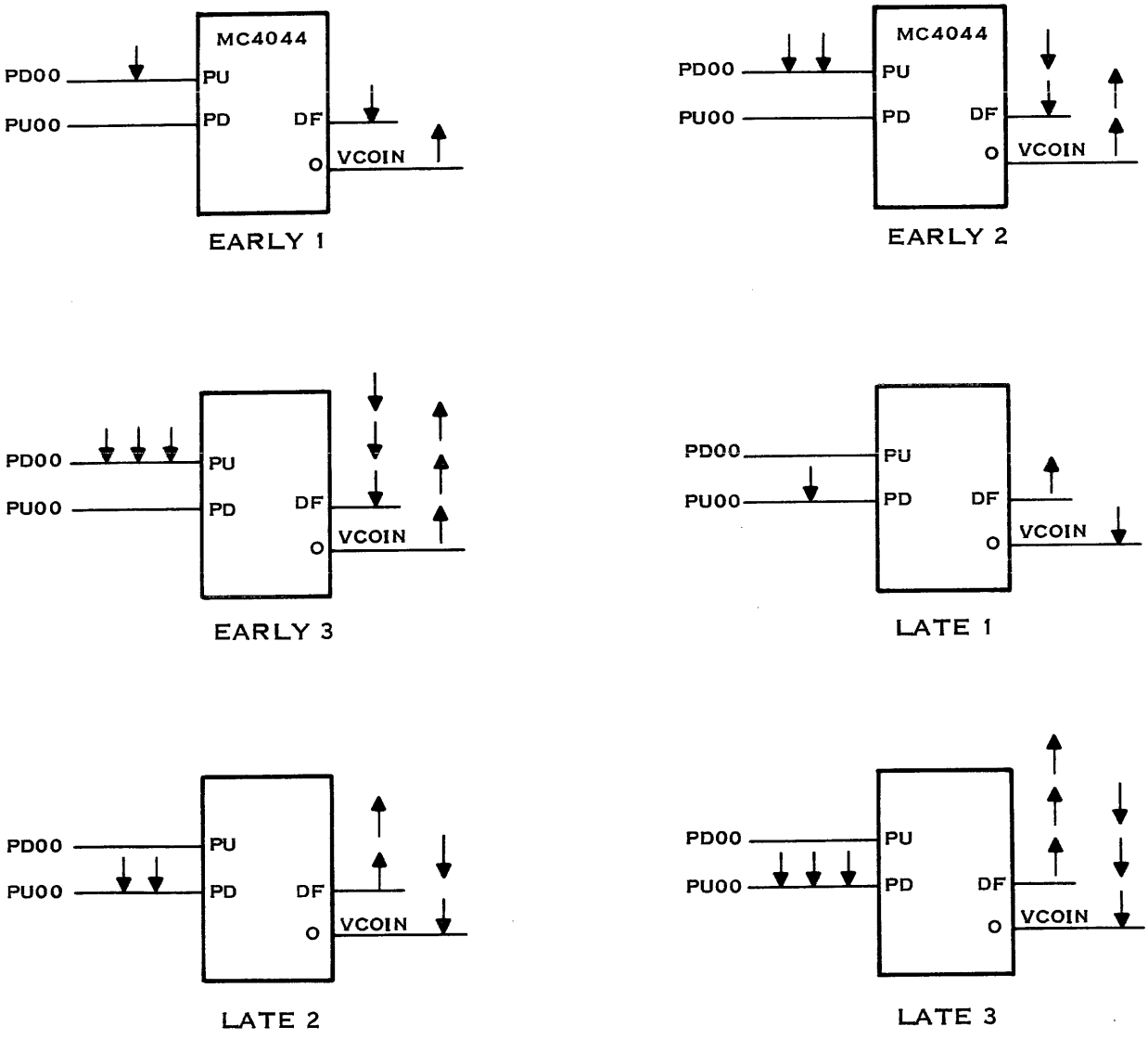


Figure 2-69. PLL Corrections for Read MFM (Sheet 4 of 4)

The reasons for the clock corrections are described in greater detail with the two, three, and four-microsecond windows in the following paragraphs.

Two-microsecond Window. Refer back to part B of Figure 2-54, which shows MFM encoding of a typical data pattern. Notice that there are only two possible ways for two valid MFM pulses to occur within two microseconds; if they are both clock pulses (data pattern 000...), or if they are both data ones. Therefore, if a SYNCDPULSE occurs in the two-microsecond window, the value of the input data bit is identical to the previous data bit. For this reason, the clock/data window is not changed if a pulse occurs in the two-microsecond window.

Regardless of bit value, a pulse that is recorded within two microseconds of the previous pulse can either not be affected by bit shift, or be shifted away from the previous bit. If a legitimate bit shift occurred, the pulse must fall in the late part of the window.

If a pulse occurs in the early part of the two-microsecond window (states C, D, or E), the PLL frequency is too low, and a PLL pump-up condition is generated.

If the pulse occurs in state D (E2), that pulse position may have been caused by jitter, by low PLL frequency, or both. Due to the possibility of jitter, the two-microsecond window is not realigned, but a double-width pump-up pulse is generated.

If the SYNCDPULSE occurs in state C (E1), it is an indication of a large window center misalignment combined with a low PLL frequency and cannot be a bit shift. In this case, the window is realigned and a one clock period pump-up pulse is issued.

A SYNCDPULSE in the second half of the two microsecond window (states F, 10, or 11) can be due to one or both of the following reasons:

1. The incoming pulse is legitimately shifted late because the following pulse (which is not known yet) is spaced three or four microseconds from the current input pulse.

2. The bit controller is cycling too fast (PLL frequency is high).

The possibility of a bit shift delay requires that the window centering not be changed. This means that the entry point must be selected so that the center of the next two-microsecond window is exactly 12 clock periods (two microseconds) from the present window center. Taking state E as the window center and following the L1, L2, and L3 outputs from states F, 10, and 11 shows that in each case, the total delay back to state E is 12 clock periods (one data frame).

The second possibility, PLL frequency too high, requires pump-down of the PLL frequency. The width of the pump-down pulse increases as the SYNCDPULSE occurs later in the window. The pump-down pulse width is one, two, or three clock periods, for a SYNCDPULSE occurring in state F, 10, or 11 respectively. This may apear inappropriate because the late occurrence can be caused by a bit shift. However, the damping of the PLL will not allow the PLL output frequency to change instantaneously. Also, it is not possible for two consecutive pulses to be shifted in the same direction.

A momentary over-pump condition does not significantly change the window center and the PLL frequency, if the PLL is sufficiently damped. Pump output proportional to the amount of shift is needed for the case when an all-shifted pattern occurs in the data stream. In this case, the variable pump amount keeps the center of the window at nominal and prevents window drift.

State 11 is a cleanup state that takes care of the various possibilities that can cause the bit controller to complete the two-microsecond window without a SYNCDPULSE input. The state of the clock/data window (WINDOWL) determines which outputs are enabled.

If the data window is active (WINDOWL = 1), and if no SYNCDPULSE occurrs during the two-microsecond window, the data bit must be a 0 following a 1 data bit. Therefore, a 0 is shifted into the data shift register (DTAINEE = 1 and SHIFTDTA = 1). The clock/data window is toggled at the end of state 11.

If the clock window is active (WINDOWL = 0), and if no SYNCDPULSE is detected during the two-microsecond window, bit controller decisions must be deferred to the three-microsecond window. The possibilities are that the present data bit is a zero followed by a one that will be detected in the three-microsecond window, or that the present bit is a zero followed by another zero with a missing clock bit between. There is not enough information available at state 11 to make that decision. In any case, the clock/data window is toggled at the end of state 11.

Three-microsecond Window. The predicted bit shift for the three-microsecond window is usually toward the previous bit. A SYNCDPULSE during the first three states causes an amount of PLL frequency pumping proportional to the amount of shift detected, with no window realignment. That is, for a SYNCDPULSE detected at state 12, 13, or 14, the next three-microsecond window will be 18 states (three microseconds) later.

A SYNCDPULSE in states 15 or 16 does not realign the bit controller window. However, a SYNCDPULSE detected in the last state (17) of the three-microsecond window indicates misalignment of the window. The branch to L1 delays the bit controller window by two clock periods.

When SYNCDPULSE occurs in the three-microsecond window and WINDOWL is high, the data bit value is 1 (the case of a 01 data pattern). If the WINDOWL is low, the bit is 0. This is the case of a 100 data pattern where the first 0 frame has no clock pulse, as given by the MFM encoding rule.

State 17 is a cleanup state that issues the necessary control outputs if no SYNCDPULSE occurs in the three-microsecond window.

If no pulse occurred in the window and WINDOWL = 0, no action needs to be taken with respect to the data bit. This is the case of a 101 data pattern, in which a mandatory 1 pulse (data pulse) must occur in the four-microsecond window. Note that the data = 0 pulse was shifted in state 11_{16} at the end of the two-microsecond window.

If no pulse occurred and WINDOWL = 1, a missing clock is indicated and a 1 is shifted into the clock shift register. Because it was a zero data frame (even with missing clock) a 0 is shifted in the data shift register.

The missing clock may be part of a legitimate address mark or may be due to the fact that at the start of the read operation, the bit controller clock/data window phase was reversed. Both conditions are detected by the missing clock detector and if a wrong window phase is detected, the window is toggled to the right phase by the CHANGEPULSE output of the detector. WINDOWL is toggled at the end of state 17.

Four-microsecond Window. This is a window in which a pulse should always occur if the data is correctly encoded and the bit controller is tracking properly. The predicted bit shift for this window and the action taken for a SYNCDPULSE are identical to the three-microsecond window, with the exception of the last state (state 0). State 0 is also a wait state. If no SYNCDPULSE signals occur, the bit controller waits in this state for the first pulse to occur. This may also be considered to be the start state.

Figure 2-70 shows bit controller timing for read MFM operations. This diagram summarizes the operations for a typical input pattern without missing clocks.

2.7.3.6 Word Controller. The word controller performs four main functions:

- Determination of word boundaries in the serial read data stream
- Management of handshaking control signals between the data separator and the central processor section
- Detection of data overrun (rate error) conditions
- Control of CRC logic
- Selection of data source (CRC generator or data shift register) for write data encoding logic

For read operations, the bit controller is responsible for converting encoded data into separated clock and data bits. Using the address mark as the initial reference, the word controller keeps track of 16-bit word boundaries. Word controller operations are independent of FM or MFM encoding because the word controller treats data in 16-bit blocks, either before encoding (write) or after decoding (read).

The data shift register transfers data between the microprocessor data bus and the data separator. Each parallel data word transferred into or out of the data separator is accompanied by an exchange of data separator select and data separator ready signals between the TMS 9900 microprocessor and the word controller logic. A handshaking exchange is necessary because central processor operations are timed by microprocessor clock and the data separator runs on the PLL clock. The word controller generates the shift register load commands and the data separator ready signals that coordinate the word transfers.

The word controller monitors each parallel data transfer to detect overrun conditions in which the parallel data is not transferred fast enough to keep up with the fixed-rate serial data flow.

The word controller issues the preset, enable, and error latch signals that control CRC generation and checking. The word controller writes the CRC word at the end of a sector ID or data record by selecting the CRC generator output.

Figure 2-71 shows the word controller and associated logic. The word controller is a ROM-based state controller and is very similar to the bit controller. A general description of ROM-based state controllers is included with the TILINE interface controller in paragraph 2.5.9.1. The word controller consists of two ROM devices and a current state register. The ROM addresses depend on the current state latched in the register and the values of the input variables. Codes programmed in the ROM devices determine the next state and the values of the control outputs.

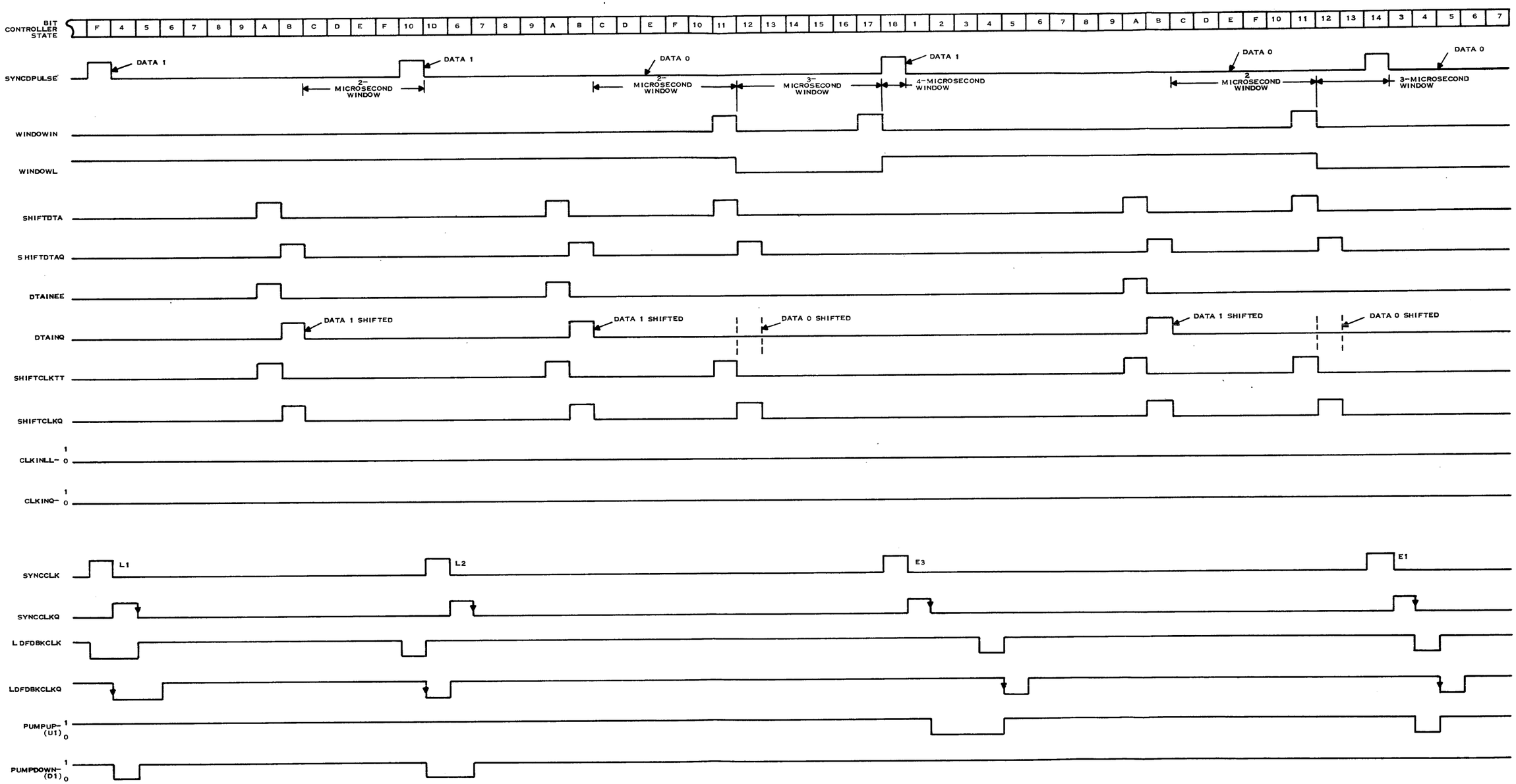
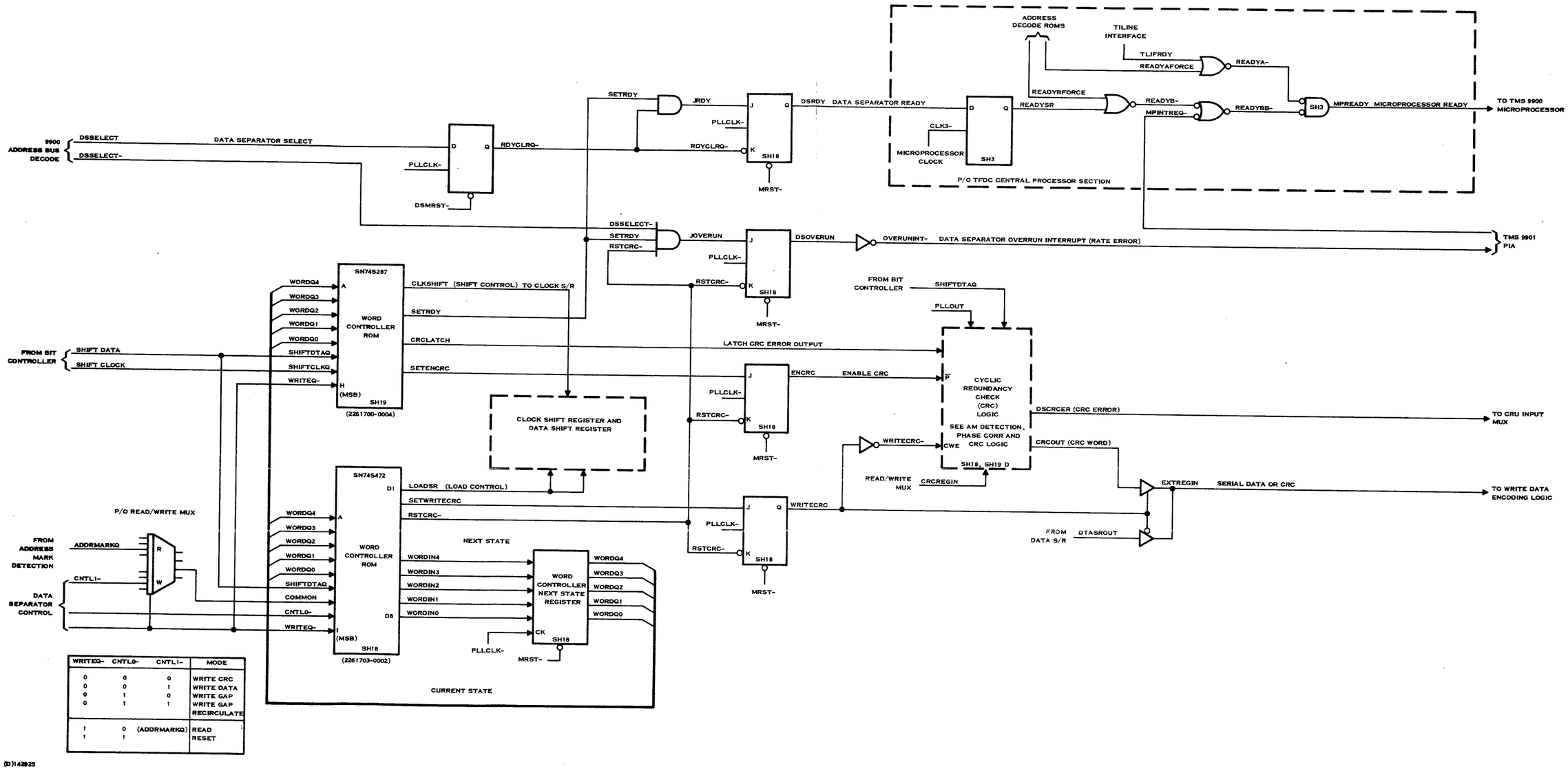


Figure 2-70. Read MFM Timing



WRITEQ-	CNTL0-	CNTL1-	MODE
0	0	0	WRITE CRC
0	0	1	WRITE DATA
0	1	0	WRITE GAP
0	1	1	WRITE GAP RECIRCULATE
1	0	(ADDRMARKQ)	READ
1	1		RESET

Figure 2-71. Word Controller

The word controller operating modes are: write CRC, write data, write gap, write gap (recirculate), read, and reset. The word controller mode is determined by WRITEQ-, CNTL0-, and CNTL1- from the data separator control register. These are latched CRU outputs from the TMS 9900 microprocessor. WRITEQ- and CNTL0- are direct inputs to the word controller. CNTL1- is gated through the read/write multiplexer (as COMMON) by a low WRITEQ- signal. For all of the write operations COMMON = CNTL1-. WRITEQ- is high for read and reset, selecting COMMON = ADDRMARKQ. ADDRMARKQ is the latched and synchronized address mark that serves as the initial reference for determination of word boundaries.

The other two input variables to the word controller are SHIFTDTAQ and SHIFTCLKQ from the bit controller. SHIFTDTAQ is a latched and synchronized shift command to the data shift register and extension register. During read operations, SHIFTDTAQ is issued once every bit frame to shift a recovered data bit (DTAINQ) into the data shift register. During write operations, SHIFTDTAQ shifts the data shift register and the extension register to perform the parallel-serial conversion and data encoding functions. SHIFTDTAQ is the basic timing term which forces the word controller to step from state to state in its operating sequence. After an address mark, the word controller tallies SHIFTDTAQ pulses in groups of 16 to determine word boundaries.

SHIFTCLKQ does not effect the word controller operating sequence. During read operations, SHIFTCLKQ is passed on to the clock shift register as CLKSHIFT. CLKSHIFT shifts the missing clock pattern by one bit and shifts the bit controller CLKINLL- output into the register LSB. The word controller ignores SHIFTCLKQ during write operations and issues CLKSHIFT at times determined by the word controller sequence.

The word controller marks word boundaries by issuing a set ready (SETRDY) output. If the ready clear is inactive (RDYCLR- = 1), JRDY sets the data separator ready F/F. Data separator ready (DSRDY) is a notification from the data separator to the central processor section that the data separator is ready for a one-word transfer. For read operations, DSRDY high means that the incoming data word is fully established in the data shift register and is available for transfer to the register file or microprocessor. For write operations, DSRDY high means that the last data bit of the previous word is in the SN74LS194 extension register; therefore, the data shift register is ready to accept another data word.

The data separator ready signal is resynchronized to the microprocessor clock as READYSR. READYSR is one of the inputs to the microprocessor ready circuits. As stated in the TMS 9900 description, a low microprocessor ready (MPREADY) signal suspends microprocessor operations with all output and control signals held constant. A high MPREADY signal allows the microprocessor to resume operation.

The microprocessor operations should be suspended during periods when the microprocessor is waiting for action from a slower interface. For example, reading or writing a single data word takes a full word time (32 microseconds for MFM or 64 microseconds for FM). The microprocessor cannot do any useful work until the completion of the cycle, indicated by data separator ready. Rather than forcing the microprocessor to cycle through self-loops, the microprocessor operation is suspended in mid-instruction by a low MPREADY input.

The first part of the MOV instruction is a read from the data shift register. When E000 appears on the output address lines, the address decoder ROMS set READYBFORCE low, disabling MPREADY. The data separator select F/F sets on phase 3 microprocessor clock. RDYCLRQ- goes high on the next clock pulse, allowing the DSRDY F/F to monitor for the next word boundary. The SETRDY output of the word controller indicates that the word in the data shift register is available. The data separator ready F/F sets, and MPREADY goes active on the next phase 3 clock. Execution of the MOV instruction continues and the data word is temporarily stored in the microprocessor, pending the TILINE master write cycle.

When the microprocessor restarts and changes the address output, READYBFORCE returns high, holding the microprocessor enabled regardless of data separator ready. DSSELECT resets on the next microprocessor clock, RDYCLRQ- goes low on the next PLL clock and data separator ready goes low on the second PLL clock pulse.

The data separator overrun F/F indicates a rate error if the word controller reaches a word boundary and data separator is not selected. This condition occurs if the data words cannot be moved into or out of the data separator fast enough to keep up with the serial data rate. The microprocessor should always be awaiting the next available cycle when the word boundary is reached. Note that the reset CRC (RSTCRC-) output of the word controller can prevent an overrun indication.

Word Controller ROM Listings. The word controller outputs are determined by the ROM address inputs and by the output word programmed at each address. The ROM input/output bit assignments and listings are presented here for reference.

Figure 2-72 shows the input and output bit assigments. This figure may be used with the SN74S287 listing of Table 2-30 and the SN74S472 listing of Table 2-31 for analysis of word controller operation. It is important to remember that the individual ROM word selected for output (addressed) depends on both the current state (WORDQ0-4) and the input variables.

These tables are derived from the HI-LO listings of the data programmed into the devices. The first column shows the word controller current states in hexadecimal form. These states are not shown in the HI-LO listing. The input addresses, in decimal form, are in the next column. The ROM output words are given in the remaining columns.

The SN74S287 ROM listing shows eight four-bit words per row, and the SN74S472 shows four eight-bit words per row. The rows are grouped into blocks for easier reading.

State Diagram Introduction. A state diagram is the clearest way to describe the operation of a ROM-based state machine such as the bit controller or the word controller. A state diagram consists of nodes (circles) that represent the states, and directed lines between the nodes that represent all the possible transitions. Each node is identified with a state number (current state) in hexadecimal notation. Complex sequences that depend on past history and present inputs can be represented on a state diagram.

The outputs that are active as the result of a particular state or transition are shown on the diagram. The inactive outputs are omitted to simplify the diagram and highlight the important changes. Outputs that remain constant for the entire sequence are described in the notes.

Table 2-30. Word Controller SN74S287 ROM Listing

State	Input Address	Word Controller Write (Data, CRC, Gap, Gap Recirculating)	
00-07	000-007	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	008-015	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTDTAQ = 0
10-17	016-023	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
18-1F	024-031	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTCLKQ = 0
00-07	032-039	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	040-047	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLHH	SHIFTDTAQ = 1
10-17	048-055	LLLL LLLL LLLL LLLL LLLL LLLL LLLL HLLL	
18-1F	056-063	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
00-07	064-071	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	072-079	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTDTAQ = 0
10-17	080-087	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
18-1F	088-095	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTCLKQ = 1
00-07	096-103	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	104-111	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLHH	SHIFTDTAQ = 1
10-17	112-119	LLLL LLLL LLLL LLLL LLLL LLLL LLLL HLLL	
18-1F	120-127	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
		Word Controller Read and Reset	
00-07	128-135	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	136-143	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTDTAQ = 0
10-17	144-151	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
18-1F	152-159	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	SHIFTCLKQ = 0
00-07	160-167	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
08-0F	168-175	LLLL LLLL LLLL LLLL LLLL LLLL LLLL HHHL	SHIFTDTAQ = 1
10-17	176-183	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	
18-1F	184-191	LHLL LLLL LLLL LLLL LLLL LLLL LLLL LLHL	
00-07	192-199	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	
08-0F	200-207	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	SHIFTDTAQ = 0
10-17	208-215	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	
18-1F	216-223	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	SHIFTCLKQ = 1
00-07	224-231	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	
08-0F	232-239	LLLH LLLH LLLH LLLH LLLH LLLH LLLH HHHH	SHIFTDTAQ = 1
10-17	240-247	LLLH LLLH LLLH LLLH LLLH LLLH LLLH LLLH	
18-1F	248-255	LHLH LLLH LLLH LLLH LLLH LLLH LLLH LLHH	

The word controller runs much slower than the bit controller. Most of the controller state changes are caused by SHIFTDTAQ output pulses from the bit controller. These pulses occur once per bit cell as the recovered data bit shifts into the data shift register.

A single state diagram covering all word controller operating modes would be unnecessarily complex. The word controller sequences are described in four diagrams: read, write CRC, write data, write gap and write gap recirculate.

Table 2-31. Word Controller SN74S472 ROM Listing (Continued)

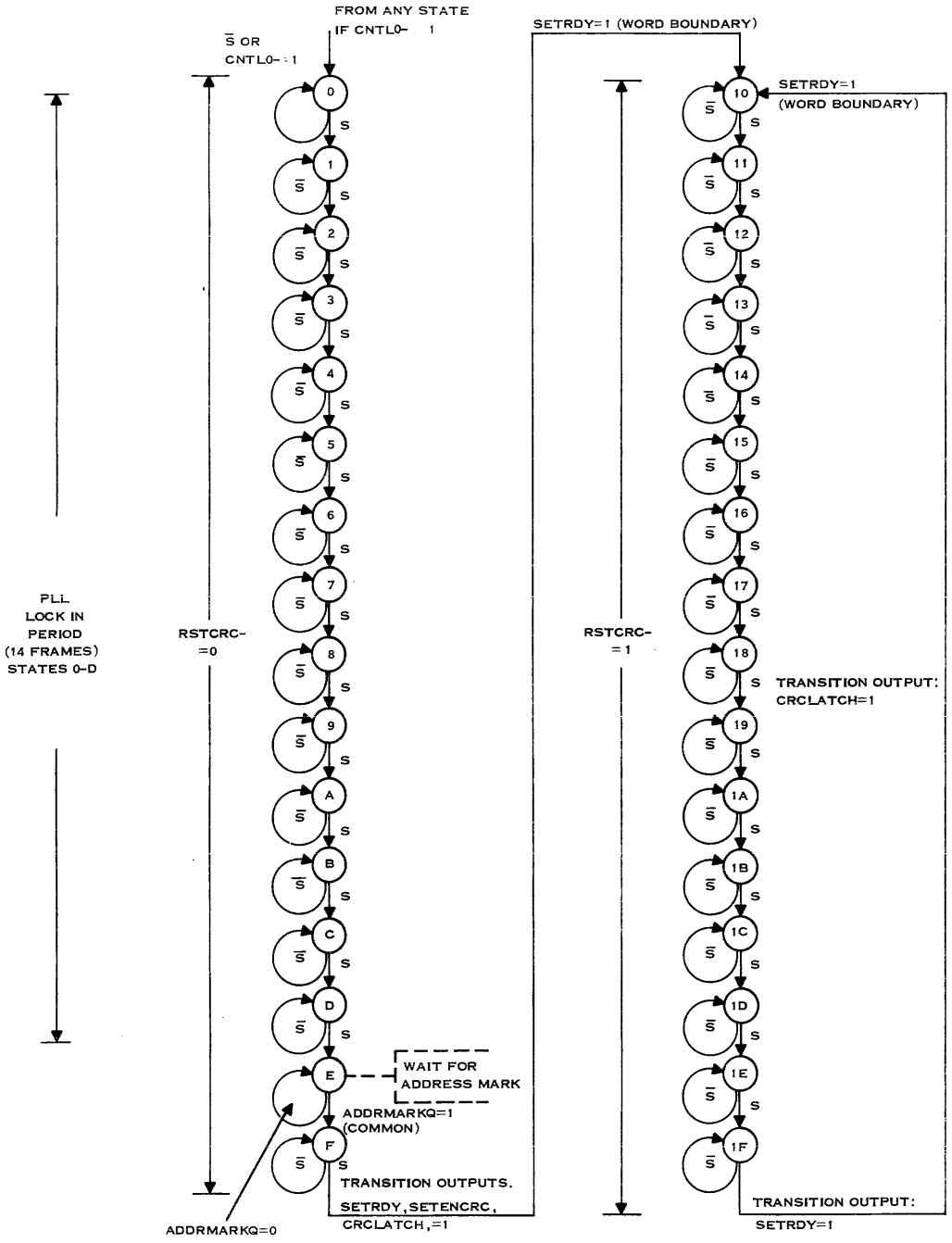
State	Input Address	Word Controller Write Gap and Write Gap Recirculate		
00-03	128-131	LLLLLHLL LLLLHHLL LLLHLHLL LLLHHHLL		
04-07	132-135	LLHLLHLL LLHLHHLL LLHHLHLL LLHHHHLL		
08-0B	136-139	LHLLLHLL LHLLHHLL LHLHLHLL LHLHHHLL		
0C-0F	140-143	LHHLLHLL LHHLHHLL LHHHLHLL LHHHHHLL	SHIFTDTAQ	
10-13	144-147	HLLLLHLL HLLLHHLL HLLHLHLL HLLHHHLL	= 0	
14-17	148-151	HLHLLHLL HLHLHHLL HLHHLHLL HLHHHHLL		
18-1B	152-155	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	156-159	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		WRITE GAP
00-03	160-163	LLLLHHLL LLLHLHLL LLLHHHLL LLHLLHLL		
04-07	164-167	LLHLHHLL LLHHLHLL LLHHHHLL LHLLLHLL		
08-0B	168-171	LHLLHHLL LHLHLHLL LHLHHHLL LHHLLHLL		
0C-0F	172-175	LHHLHHLL LHHHLHLL LHHHHHLL LLLLLLLH	SHIFTDTAQ	
10-13	176-179	HLLLHHLL HLLHLHLL HLLHHHLL HLHLLHLL	= 1	
14-17	180-183	HLHLHHLL HLHHLHLL HLHHHHLL LHLLLHLL		
18-1B	184-187	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	188-191	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
00-03	192-195	LLLLLHLL LLLLHHLL LLLHLHLL LLLHHHLL		
04-07	196-199	LLHLLHLL LLHLHHLL LLHHLHLL LLHHHHLL		
08-0B	200-203	LHLLLHLL LHLLHHLL LHLHLHLL LHLHHHLL		
0C-0F	204-207	LHHLLHLL LHHLHHLL LHHHLHLL LHHHHHLL	SHIFTDTAQ	
10-13	208-211	HLLLLHLL HLLLHHLL HLLHLHLL HLLHHHLL	= 0	
14-17	212-215	HLHLLHLL HLHLHHLL HLHHLHLL HLHHHHLL		
18-1B	216-219	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	220-223	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		WRITE GAP (RECIRCULATE)
00-03	224-227	LLLLHHLL LLLHLHLL LLLHHHLL LLHLLHLL		
04-07	228-231	LLHLHHLL LLHHLHLL LLHHHHLL LHLLLHLL		
08-0B	232-235	LHLLHHLL LHLHLHLL LHLHHHLL LHHLLHLL		
0C-0F	236-239	LHHLHHLL LHHHLHLL LHHHHHLL LLLLLLLL	SHIFTDTAQ	
10-13	240-243	HLLLHHLL HLLHLHLL HLLHHHLL HLHLLHLL	= 1	
14-17	244-247	HLHLHHLL HLHHLHLL HLHHHHLL LHLLLHLL		
18-1B	248-251	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		
1C-1F	252-255	LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL		

Table 2-31. Word Controller SN74S472 ROM Listing (Continued)

State	Input Address	Word Controller Reset			
00-03	384-387	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
04-07	388-391	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
08-0B	392-395	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0C-0F	396-399	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
10-13	400-403	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
14-17	404-407	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
18-1B	408-411	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
1C-1F	412-415	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
00-03	416-419	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
04-07	420-423	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
08-0B	424-427	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0C-0F	428-431	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
10-13	432-435	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
14-17	436-439	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
18-1B	440-443	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
1C-1F	444-447	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
00-03	448-451	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
04-07	452-455	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
08-0B	456-459	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0C-0F	460-463	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
10-13	464-467	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
14-17	468-471	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
18-1B	472-475	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
1C-1F	476-479	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
00-03	480-483	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
04-07	484-487	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
08-0B	488-491	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
0C-0F	492-495	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
10-13	496-499	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
14-17	500-503	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
18-1B	504-507	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL
1C-1F	508-511	LLLLLLLL	LLLLLLLL	LLLLLLLL	LLLLLLLL

Word Controller Read Mode State Diagram. Word controller operations are independent of the data encoding mode, FM or MFM. Word controller read mode corresponds to bit controller read FM or read MFM mode. Word controller and bit controller modes are selected by the same WRITEQ-, CNTLO-, and CNTL1- outputs of the data separator control register, but the DSMFM (MFM/FM) control signal is not wired to the word controller.

The read mode is always preceded by the reset mode (WRITEQ-, CONTL0- = 1). The reset mode prevents the read data input circuits from recognizing any input pulses, and allows the bit and word controllers to reach state 0. The reset mode also holds the PLL clock circuit locked at a nominal six MHz frequency to prevent frequency drift while input data pulses are disabled.



NOTES:

INPUT	OUTPUT
S MEANS SHIFTDTAQ = 1 (SHIFT DATA) $\overline{S}$ MEANS SHIFTDTAQ = 0 (NO SHIFT) WRITEQ- = 1 (H) CNTL0- = 0 FOR READ MODE (CNTL0- = 1 FORCES TO RESET, STATE 0) COMMON = ADDRMARKQ	LOADSR = 0 SETWRITECRC = 0 CLKSHIFT= SHIFTCLKQ

(C) 142878

Figure 2-73. Word Controller Read Mode State Diagram

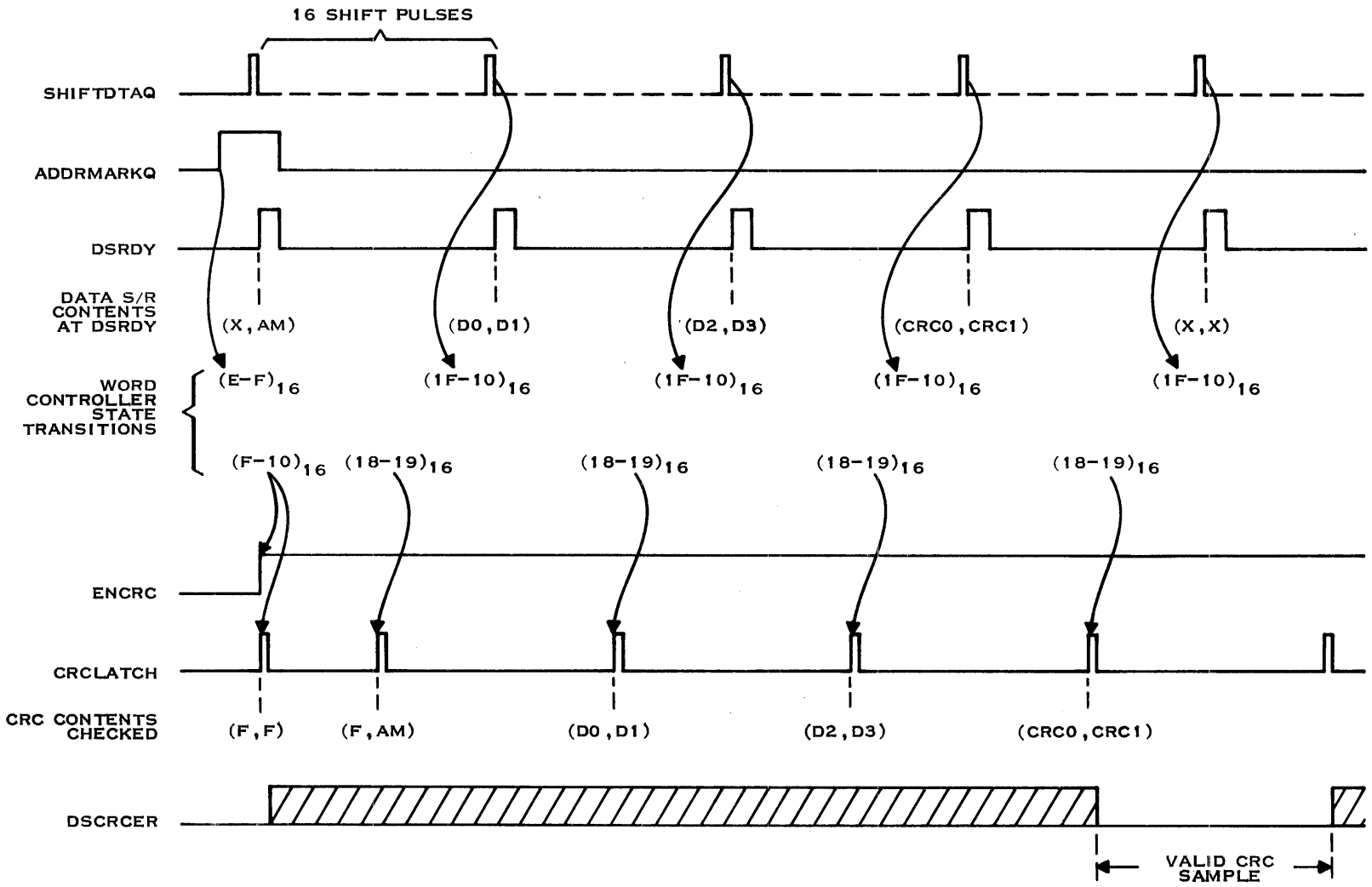
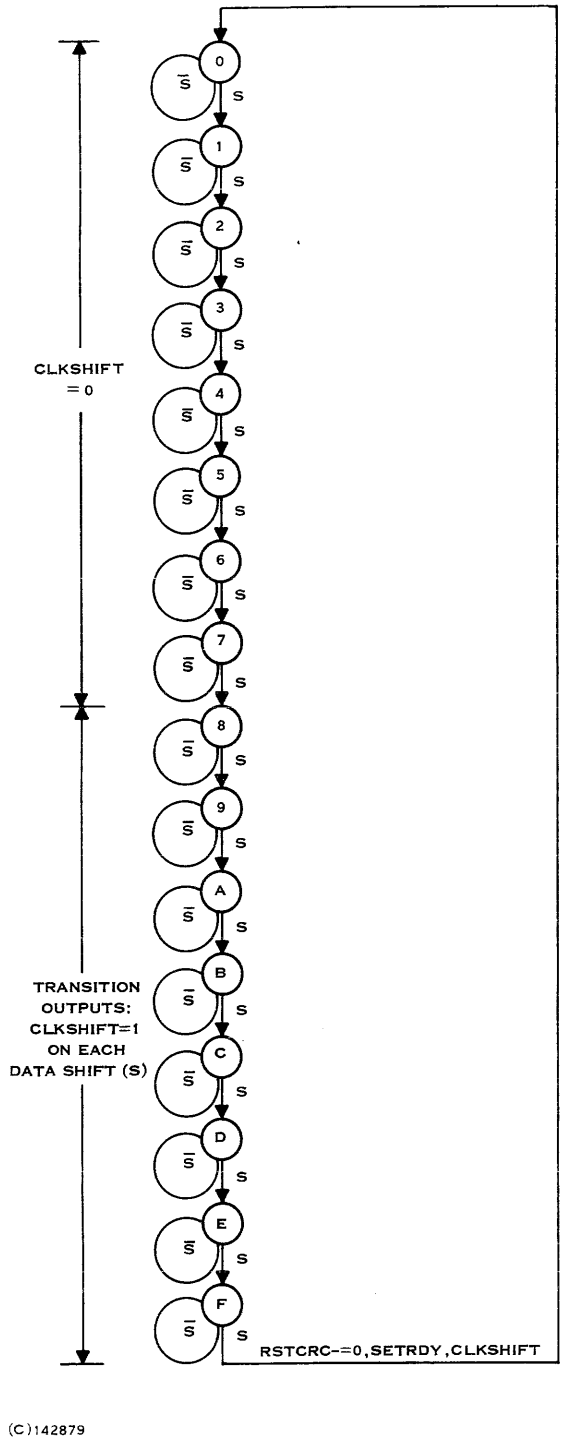


Figure 2-74. Word Controller Read Timing



NOTES:

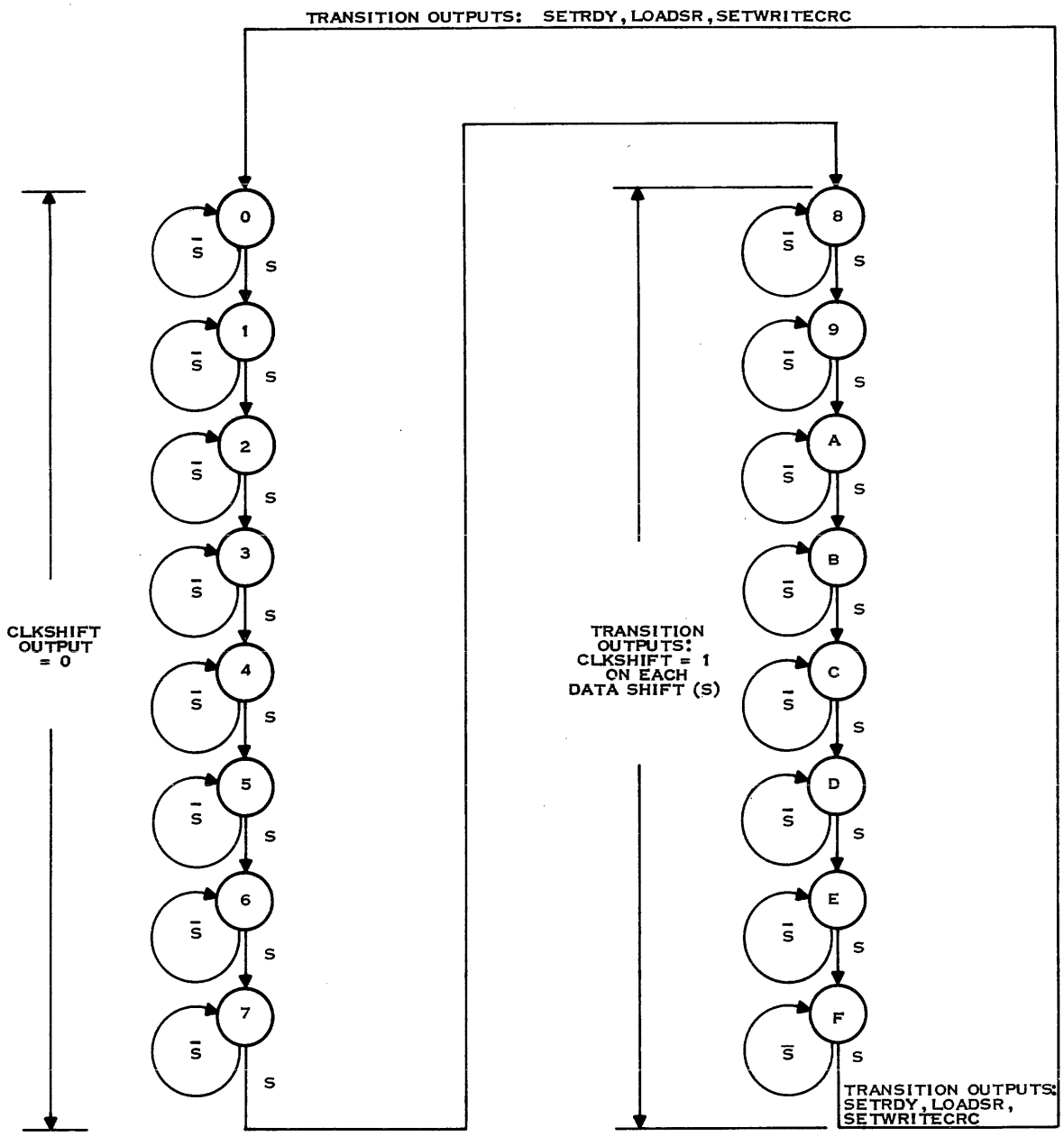
INPUTS	OUTPUTS
S MEANS SHIFTDTAQ = 1 (SHIFT DATA) S̄ MEANS SHIFTDTAQ = 0 (NO SHIFT) SHIFTCLKQ = X WRITEQ- = 0 (L) CNTL0- = 1 COMMON = CNTL1- = 0 WRITE GAP OR CNTL1- = 1 WRITE GAP RECIRCULATE	CRCLATCH = 0 SETENCRC = 0 SETWRITECRC = 0

LOADSR (LOAD CLOCK AND DATA SHIFT REGISTORS) = 1
FOR WRITE GAP (CNTL1-=0)

LOADSR = 0 FOR WRITE GAP RECIRCULATE (CNTL1-=1)

(C)142879

Figure 2-75. Word Controller Write Gap and Write Gap Recirculate State Diagram



NOTES:

INPUTS	OUTPUTS
S MEANS SHIFTDTAQ = 1 (SHIFT DATA) S MEANS SHIFTDTAQ = 0 (NO SHIFT) SHIFTCLKQ = X (IRRELEVANT) WRITEQ− = 0 (L) CNTL0− = 0 (L) COMMON CNTL1− = 0	RSTCRC− = 1 (H) SETENCRC = 0 (L) CRCLATCH = 0 (L) STATES 10−1F NOT USED

(A)142881

Figure 2-77. Word Controller Write CRC State Diagram

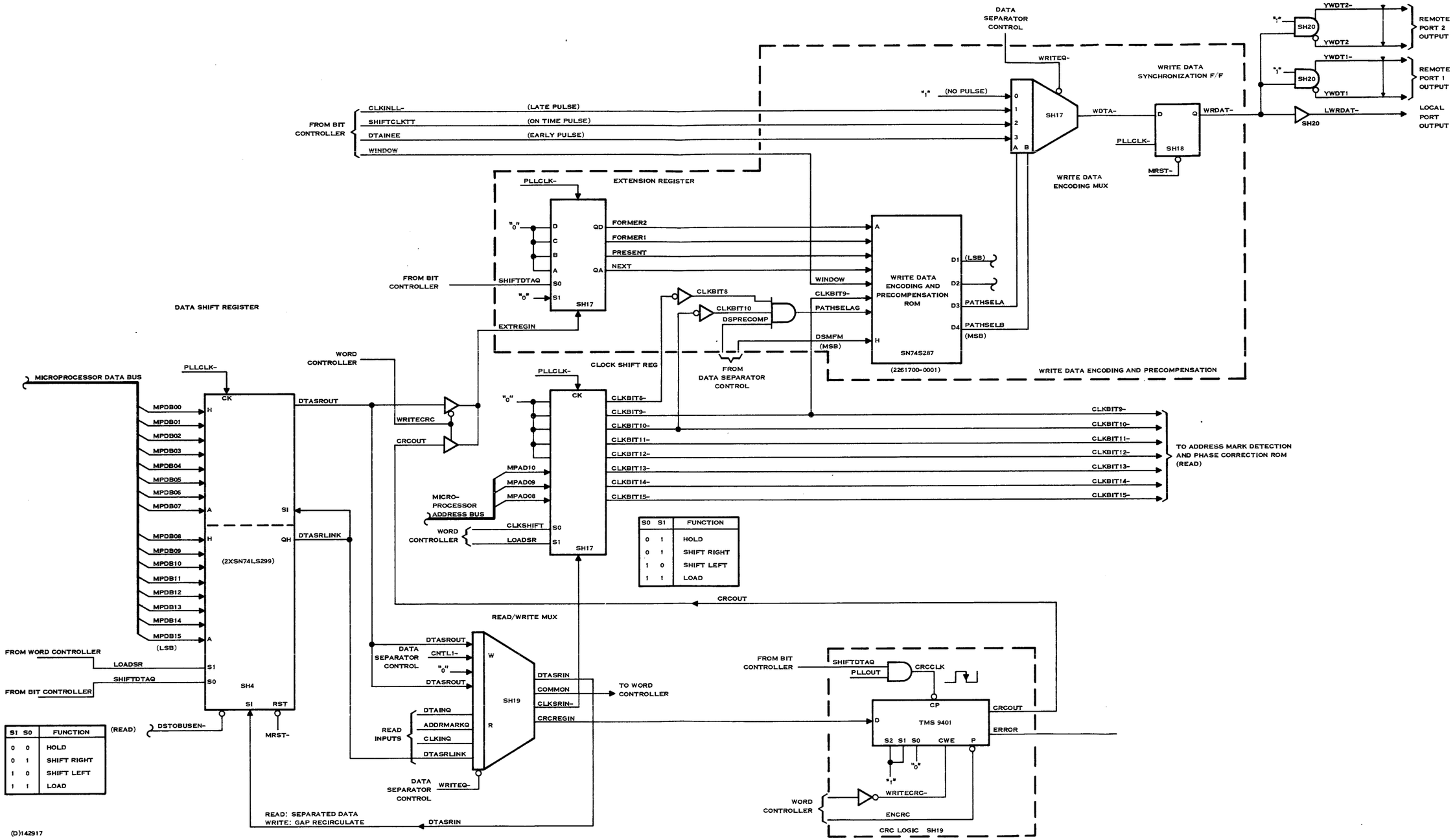


Figure 2-78. Write Data Encoding Logic

The missing clocks in any address mark always occur in the third through the fifth bits of the eight-bit byte as shown in Figures 2-79 and 2-80. When writing an address mark, the TFDC always loads one final byte of the gap pattern into the first half (MSB) of the data shift register with the address mark in the second byte. Considering the MSB of the 16-bit word as bit 0, the missing clock bits occur in the bit 10, 11, and 12 positions.

The clock shift register is an eight-bit shift register that identifies any missing clocks that have occurred (read), or specifies which clocks are to be omitted (write). A logic 1 in the clock shift register is a pointer to a missing clock. A logic 0 means no missing clock. The upper five bits are hardwired to load with zeros. The lower three bits are loaded from the microprocessor address bus (MPAD8-10). The bits provided by the microprocessor are zero except for an address mark.

Data and Clock Shifts for Data/Address Mark Encoding. Figure 2-81 shows the relationship between the extension register contents, the data shift register contents, and the clock shift register contents for a complete word shifting/encoding cycle. This figure shows the contents of these registers at load time and after shifting by SHIFTDTAQ and CLKSHIFT.

Time "t" at the top of the drawing represents a register load enabled by the word controller. With SHIFTDTAQ and CLKSHIFT high, LOADSR loads a new data word (D0-D15) from the microprocessor data bus into the data shift register. The four bits of the extension register are the last four bits from the previous operation and are unaffected by the load operation. Five hardwired zeros and three missing clock control bits are loaded into the clock shift register. The clock register stages, CLKBIT(8-15)-, are labeled 8 through 15.

Note that the bit presently being encoded for transmission is the extension register PRESENT bit, indicated as "P" on the figure.

One SHIFTDTAQ pulse later, at t + 1, the new data word MSB shifts into the extension register NEXT bit and back into the LSB position of the data shift register (DTASRIN input). The last bit of the previous word shifts to the extension register PRESENT position for encoding.

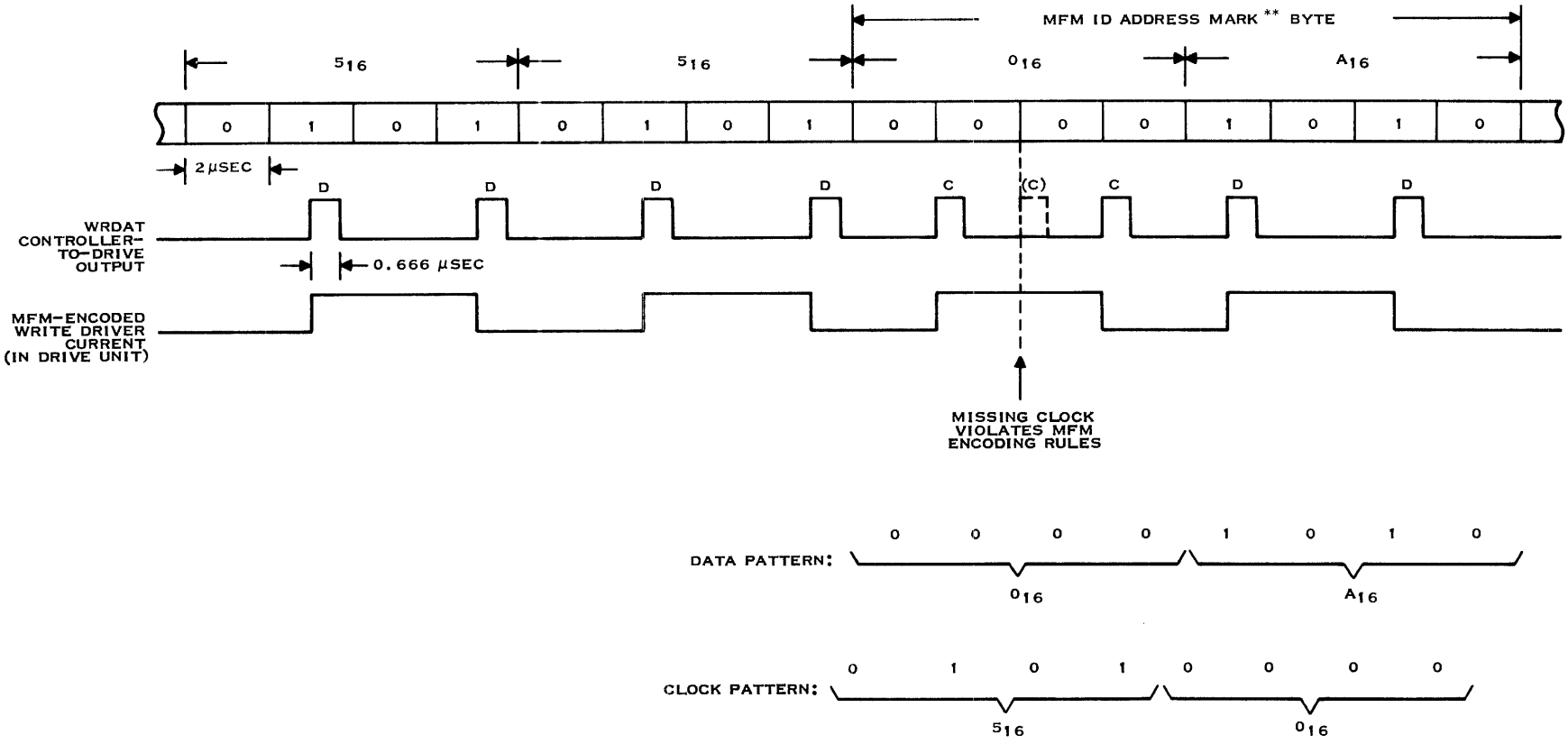
The important thing to notice about times t + 1 through t + 8 is that the clock shift register is not shifted. Missing clocks are never included in the first byte of an output word.

At t + 2, the MSB of the data word reaches the PRESENT position of the extension register and is encoded in FM or MFM format. Note the two-bit time delay between loading the data word and encoding the first bit.

At t + 8, the data word is shifted halfway through the data shift register, and the missing clock pointers are aligned with the data bits that may be affected by missing clocks. These data bits are D10, D11, and D12. Therefore, the missing clock pointers are labeled C10, C11, and C12.

The clock register and the data register shift together for the rest of the word shift. At t + 16, the LSB of the data word is loaded in the extension register. The data and clock shift registers may be reloaded or, for write gap recirculate, the recirculated word may be the next data word. The write gap recirculate never includes missing clocks, so zeros cycle through the clock shift register.

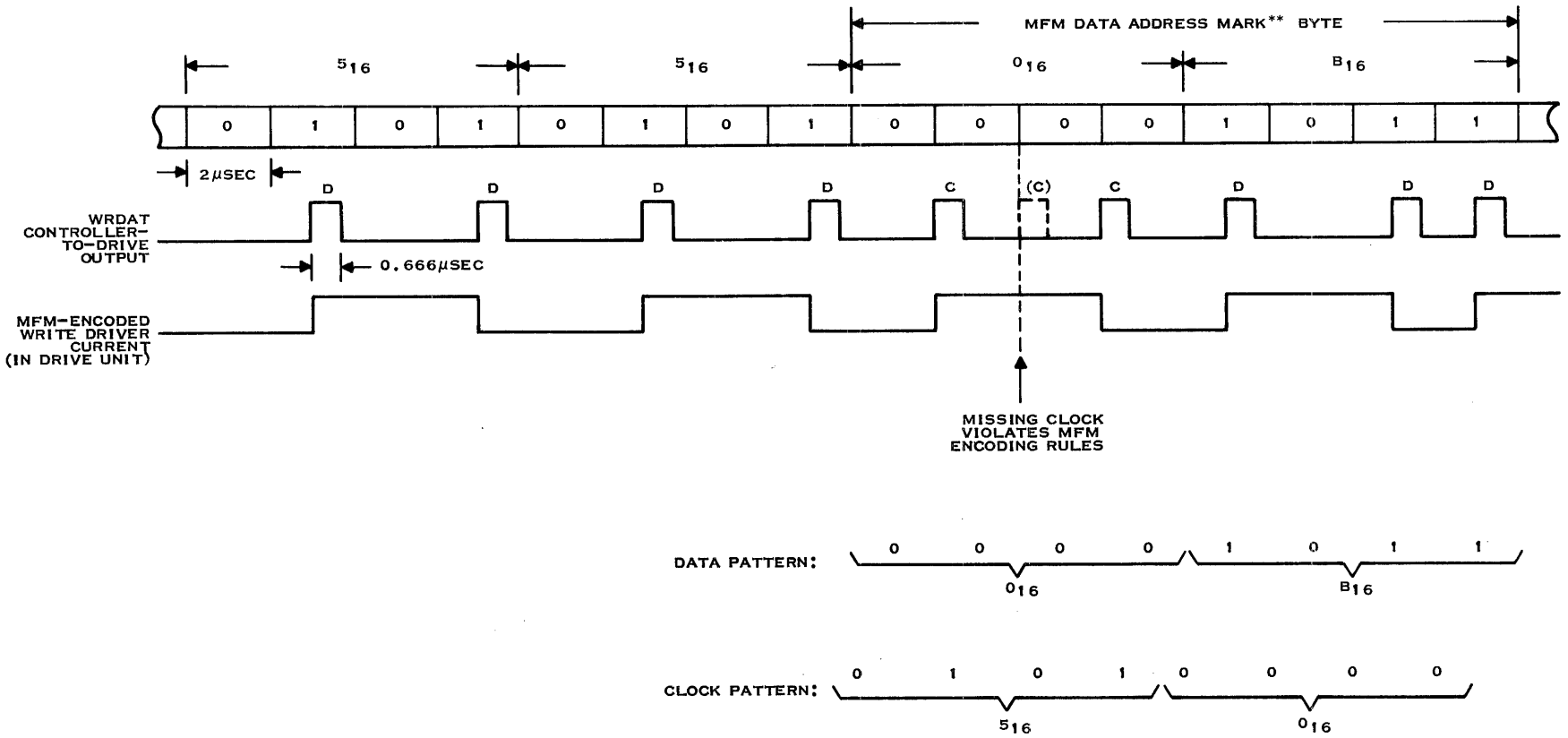
Write Data Encoding and Precompensation ROM. Refer back to Figure 2-81. The outputs of the write data encoding and precompensation ROM are multiplexer steering commands (PATHSELA, PATHSELB) that select the early, on time, late, or no pulse inputs of the write data encoding multiplexer.



NOTE: ** ID ADDRESS MARK IS SOMETIMES CALLED "ID MARK" OR "ADDRESS MARK"

(B)142705 (1/2)

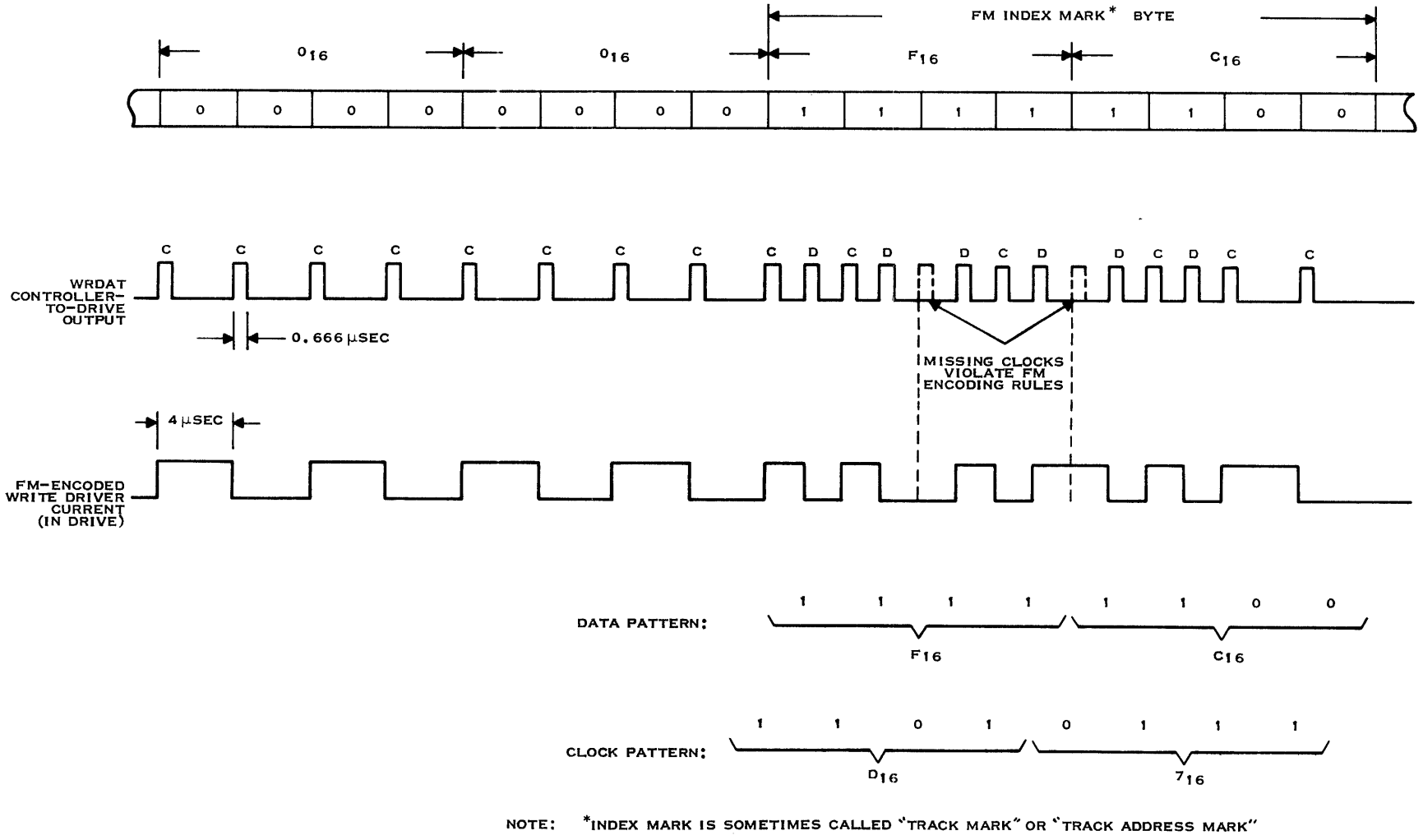
Figure 2-79. MFM Address Marks (Sheet 1 of 2)



NOTE:** DATA ADDRESS MARK IS SOMETIMES CALLED "DATA MARK"

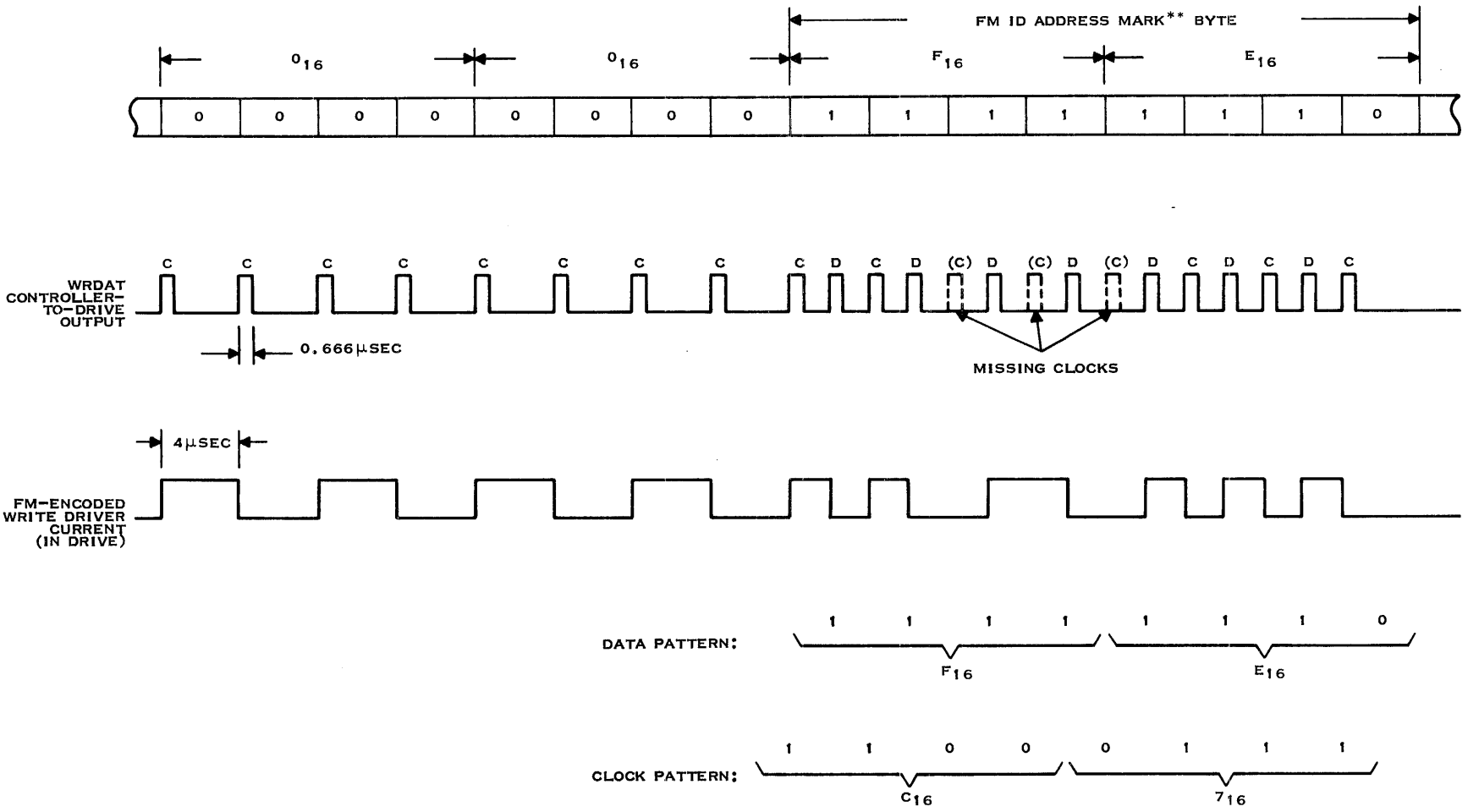
(B)142705 (2/2)

Figure 2-79. MFM Address Marks (Sheet 2 of 2)



(B)142706 (1/4)

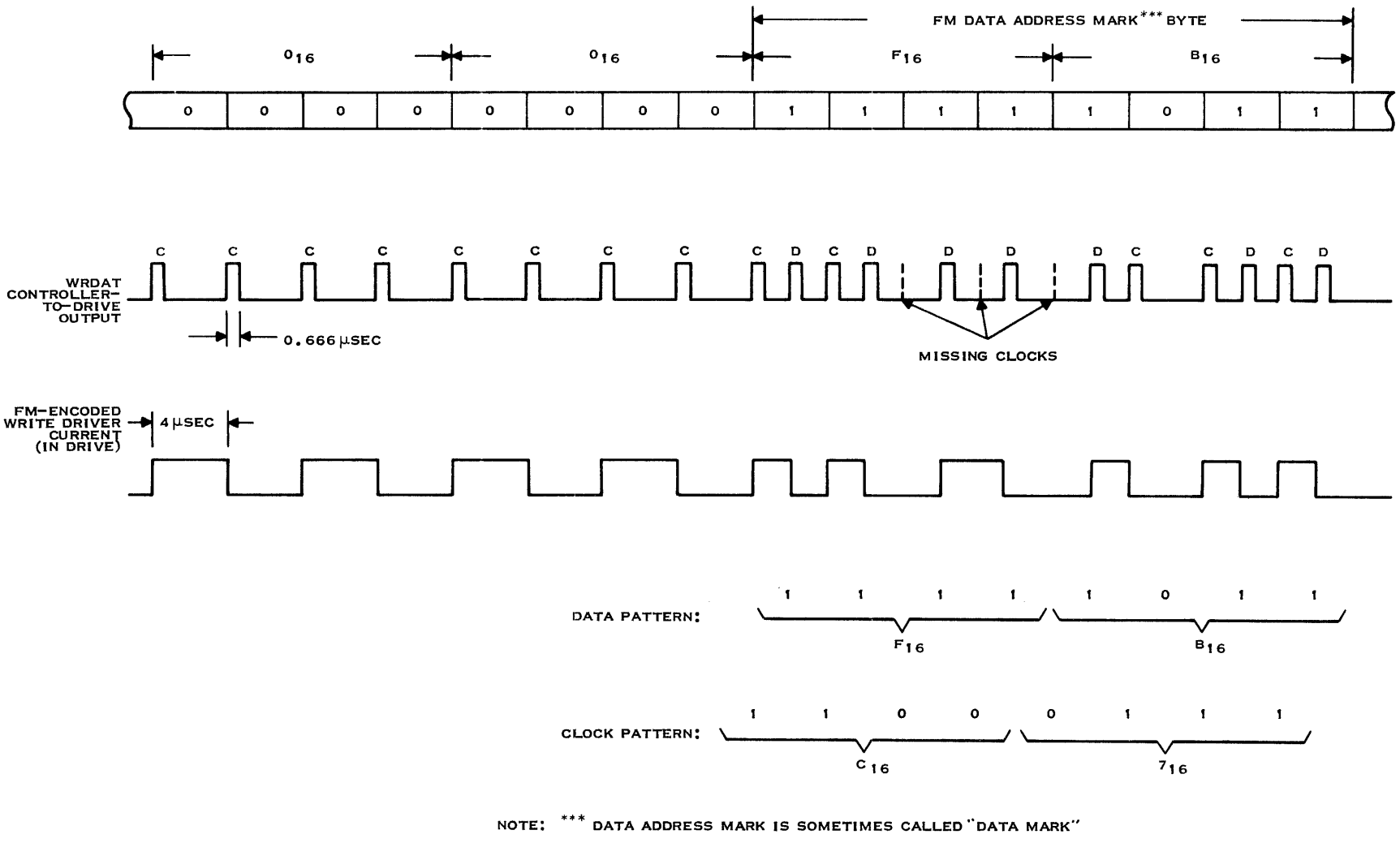
Figure 2-80. FM Address Marks (Sheet 1 of 4)



NOTE: ** ID ADDRESS MARK IS SOMETIMES CALLED "ID MARK"

(B)142706 (2/4)

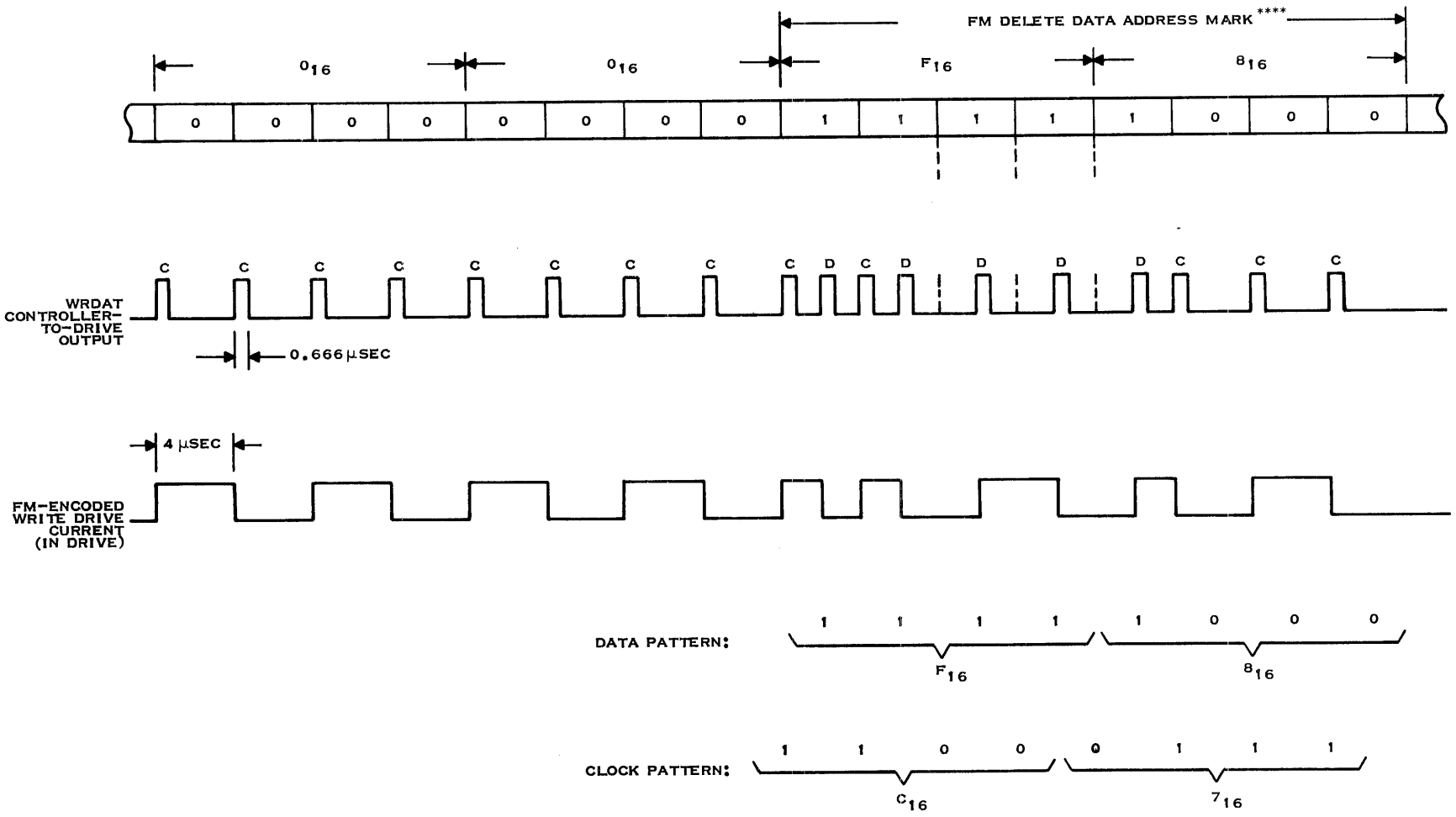
Figure 2-80. FM Address Marks (Sheet 2 of 4)



NOTE: *** DATA ADDRESS MARK IS SOMETIMES CALLED "DATA MARK"

(B)142706 (3/4)

Figure 2-80. FM Address Marks (Sheet 3 of 4)



NOTE: **** DELETE DATA ADDRESS MARK IS ALSO CALLED "DELETE DATA MARK" OR "CONTROL RECORD MARK"

(B)142706 (4/4)

Figure 2-80. FM Address Marks (Sheet 4 of 4)

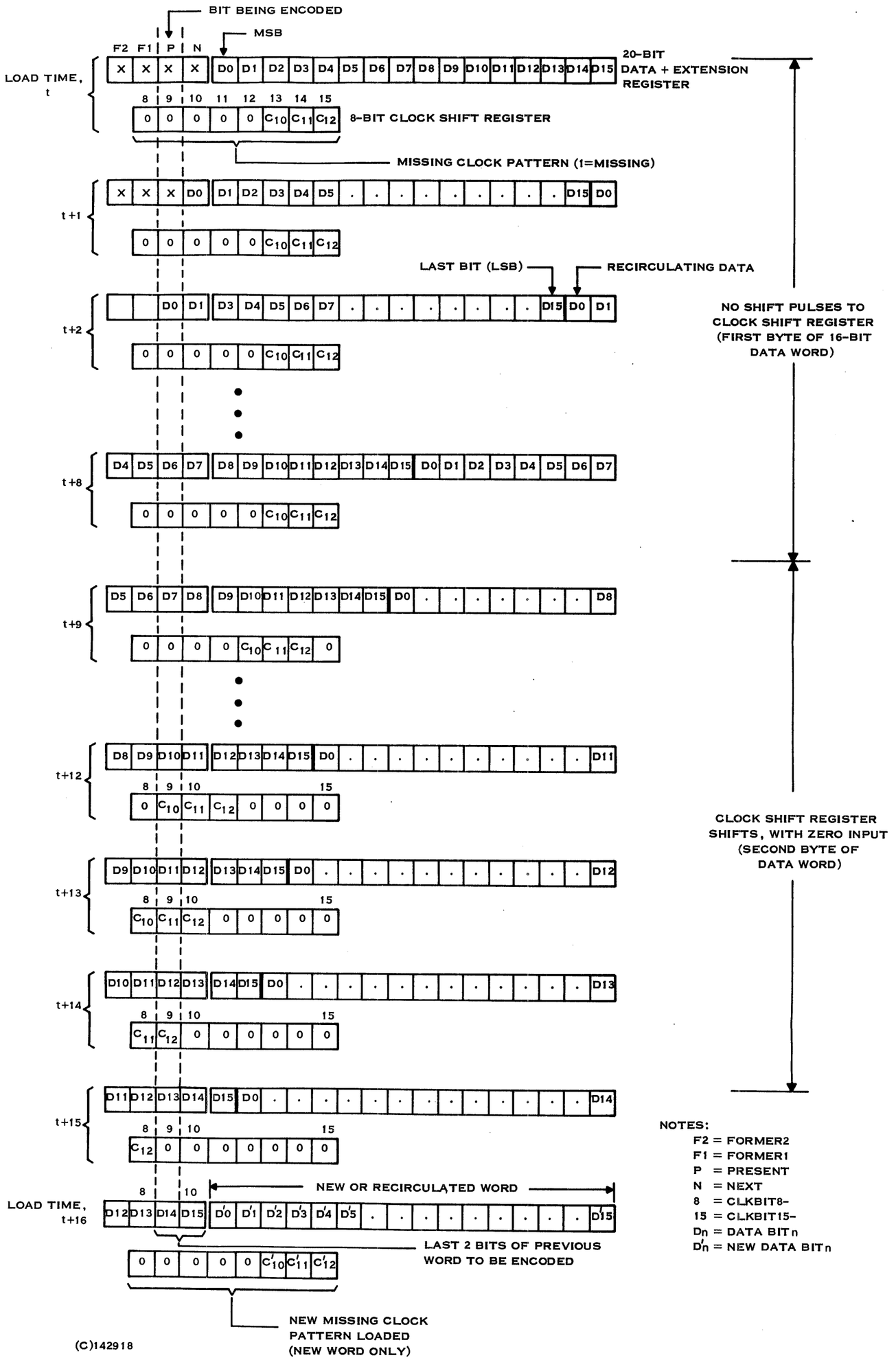


Figure 2-81. Write Data and Missing Clock Shifts

The encoding rules for uncompensated FM and MFM formats are described in paragraphs 2.7.2.1, 2.7.2.2, and in Figure 2-54. Peak shifting and precompensation against peak shifting are briefly described in paragraph 2.7.2.3 and Figure 2-55.

Peak shifting refers to the tendency of closely spaced magnetic transitions to influence the apparent peak positions of the adjacent domain areas. Peak shifting effects are much more pronounced on the inner tracks of a disk or diskette. Constant size records are recorded in shorter physical lengths on the inner tracks so that bit density increases. The effect of peak shifting is to shift data bits read from the diskette. In the worst case, clock pulses could be shifted into the data window or data pulses could be shifted into the clock window. MFM is more sensitive to these shifting effects than is FM.

Precompensation techniques offset the effects of peak shifting by writing data with intentional shifts that oppose the predicted shifts. Precompensation allows the data separator to work more efficiently and with less chance of error when the data is read from the diskette. The 9900 control program enables precompensation with a DSPRECOMP command when writing MFM data on tracks 43–76.

There are six MFM pulse patterns that are effected by peak shifts enough to require precompensation. These patterns, which are shown in Figure 2-82, are:

0011	0110
1011	1110
1000	0001

In each of these cases, the predicted shift of a clock or data pulse is from the closely packed bits toward the wider space. Precompensation involves moving the pulse in the opposite direction to the bit shift. The amount of compensation differs between versions of the TFDC assembly:

Precompensation	**TFDC Assembly**
166.66 nanoseconds	2261690-0001
250 nanoseconds	2267295-0001

The four data values that must be known for precompensation are the two preceding bits, the bit being encoded and (if required) compensated, and the next bit to be encoded. These bits are the FORMER2, FORMER1, PRESENT, and NEXT outputs of the extension register.

In the special case of an address mark, missing clock pulses can modify the precompensation requirements. If either the preceding clock bit (CLKBIT8–) or the following clock bit (CLKBIT10–) is missing, there is no need to precompensate the present bit.

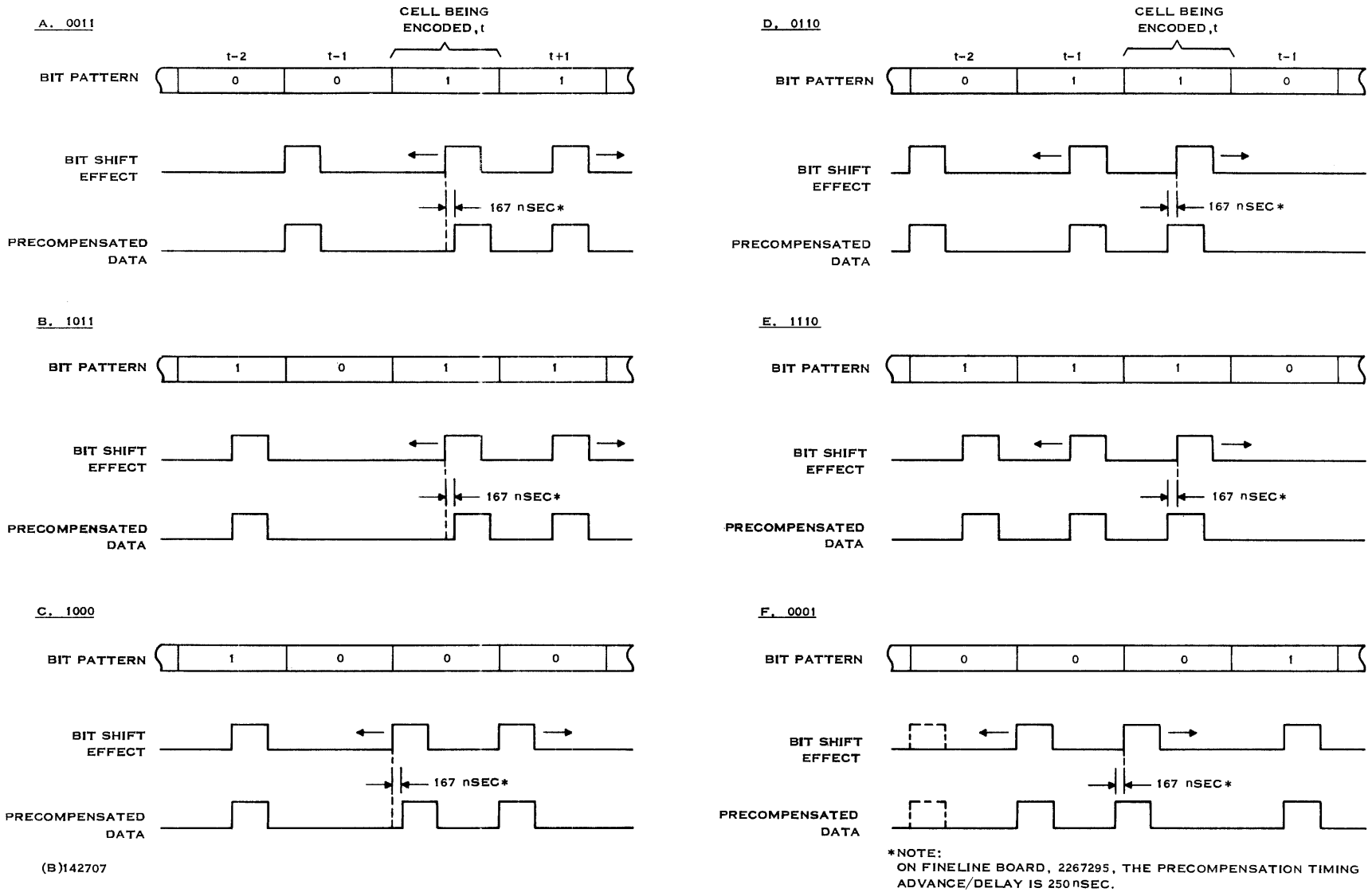


Figure 2-82. Bit Shifting and Precompensation

Refer back to the write data encoding logic, Figure 2-78. The bit controller develops the late (CLKINLL-), on time (SHIFTCLKTT), and early (DTAINEE) inputs to the write data encoding multiplexer. SHIFTCLKTP, delayed from SHIFTCLKTT by 83 nanoseconds, replaces SHIFTCLKTT on the 2267295 fineline board. The signatures of these signals do not reflect this use because they perform entirely different functions during read operations. SHIFTCLKTT, and DTAINEE are identical, asymmetric waveforms that are phased 166.66 nanoseconds (one bit controller state) apart. The CLKINLL- waveform differs between the two versions of the TFDC board. CLKINNL- in the 2261690 board is an asymmetric waveform similar to SHIFTCLKTT and DTAINEE. CLKINLL- is delayed one state from SHIFTCLKTT.

CLKINLL- in the 2267295 board is a symmetric waveform with the falling edge delayed two bit controller states (333.33 nanoseconds) from SHIFTCLKTT. The rising edge phase is identical on both boards.

Notice that the write data encoding multiplexer does not invert the selected input, but the write data output, WDTA-, is active low. It is the low periods of CLKINLL-, SHIFTCLKTT (or SHIFTCLKTP), and DTAINEE that generate active encoded clock and data pulses. The hardwired one at the multiplexer input is selected for no output pulse.

The address inputs to the write data encoding and precompensation ROM come from many sources, and there is an uncertainty in the ROM access time and the multiplexer settling. For this reason, an additional synchronization and deglitching F/F provides the final encoded clock and data output signal, WRDAT-. Differential line drivers (SN75113) transmit data to each remote international chassis power supply/interface board via twisted pairs in shielded cables. An SN7407 provides drive to the local bus.

Figure 2-83 shows the input and output bit assignments for the write data encoding and precompensation ROM. Table 2-32 is a HI-LO listing of the ROM contents.

The DSMFM control signal is the most significant bit of the ROM address. The upper half of the table (DSMFM = 0) is dedicated to FM encoding during write data, write gap, and write gap recirculate operations of the data separator. The lower half of the table (DSMFM = 1, decimal addresses 128-255) is dedicated to MFM encoding for the same operations.

PATHSELAG is the precompensation enable signal, given by PATHSELAG = (DSPRECOMP)(CLKBIT8)(CLKBIT10). DSPRECOMP is a data separator control signal that is fixed by the track and the encoding mode. CLKBIT8 and CLKBIT10 change dynamically during the course of writing an address mark, disabling precompensation for MFM bits preceded by or followed by a missing clock. For FM encoding, identical code appears in the ROM for PATHSELAG equals 0 or 1. PATHSELAG is thus a "don't care" input for FM encoding.

CLKBIT9- = 1 for a missing clock pulse associated with the present data bit. This signal is required for encoding of FM and MFM address marks. WINDOW determines whether a clock pulse (WINDOW = 1) or a data pulse is being encoded.

The values of the four most significant ROM address bits, DSMFM through WINDOW, narrow the choice of ROM output words to 16 words. Notice that the table is partitioned into 16-word (two-row) groups for clarity. The individual word selected for output is determined by the four-bit data pattern in the extension register.

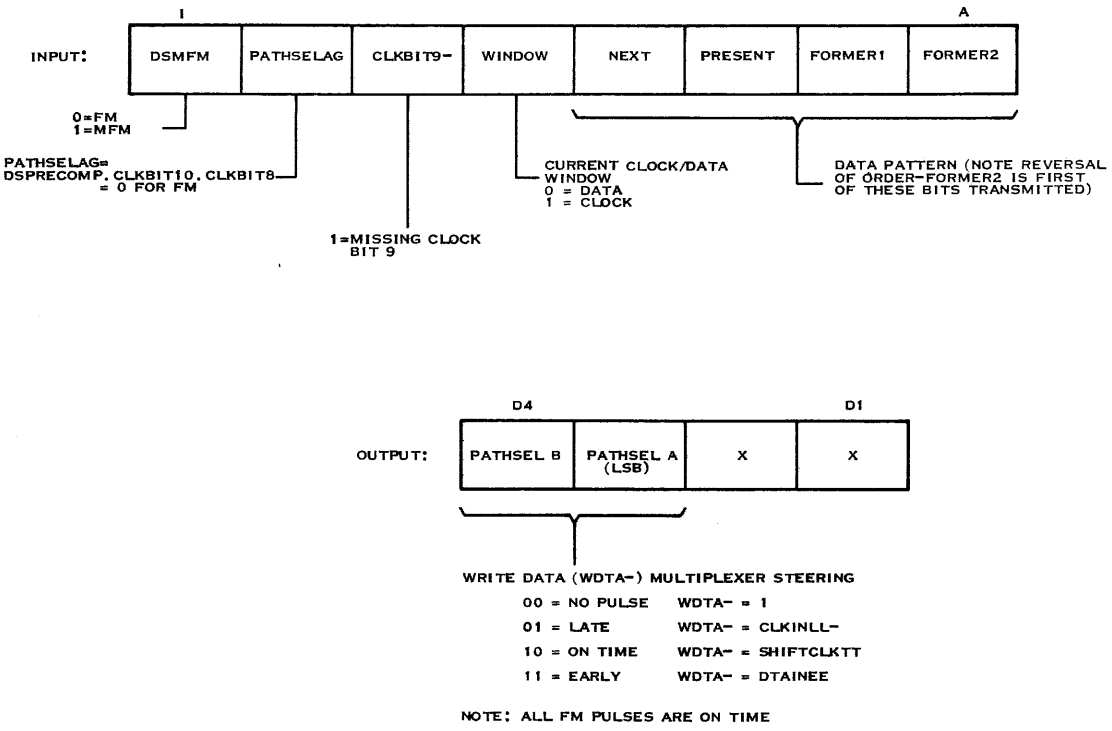


Figure 2-83. I/O Bit Assignments for Write Data Encoding and Precompensation ROM

Notice that the order of the extension register outputs in the ROM address is the reverse of the order of transmission to the drives. The order of the address bits is NEXT, PRESENT, FORMER1, and FORMER2 (address LSB). Therefore, to locate the ROM output word selected for a given pattern, reverse the bit order from the order of transmission. Table 2-33 shows the critical patterns for precompensation in normal and reversed form.

2.7.3.8 Address Mark Detection and Phase Correction. Two types of synchronization are required to recover data from the serial data stream recorded on a diskette. Bit synchronization allows the read logic to correctly distinguish clock pulses from data pulses, and word synchronization divides the incoming data along the correct word boundaries. All gaps on a diskette are filled with a standard gap data pattern to synchronize the clock/data bit separation circuitry at read time. Address marks identify the beginning of sector identification (ID) headers and data fields. Address marks define the initial word boundary and the type of record. The first data bit after the address mark is the first bit of the first data or ID word. An address mark is a predefined data byte that violates the FM or MFM encoding rules by omitting up to three clock pulses.

Table 2-32. Write Data Encoding and Precompensation ROM Listing

Hex Pattern	Input Address	FM Write	CLKBIT9-	PATHSELAG	PATHSELA
00-07	000-007	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 0	= 0	= 1
08-0F	008-015	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	016-023	HLLL HLLL HLLL HLLL HLLL HLLL HLLL HLLL	= 1		
08-0F	024-031	HLLL HLLL HLLL HLLL HLLL HLLL HLLL HLLL			
00-07	032-039	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 0	= 0	= 1
08-0F	040-047	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	048-055	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	= 1		
08-0F	056-063	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL			
00-07	064-071	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 0	= 0	= 1
08-0F	072-079	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	080-087	HLLL HLLL HLLL HLLL HLLL HLLL HLLL HLLL	= 1		
08-0F	088-095	HLLL HLLL HLLL HLLL HLLL HLLL HLLL HLLL			
00-07	096-103	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 0	= 0	= 1
08-0F	104-111	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	112-119	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	= 1		
08-0F	120-127	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL			
		MFM Write			
00-07	128-135	HLLL HLLL LLLL LLLL LLLL LLLL LLLL LLLL	= 0	= 0	= 1
08-0F	136-143	HLLL HLLL LLLL LLLL LLLL LLLL LLLL LLLL			
00-07	144-151	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 1		
08-0F	152-159	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	160-167	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	= 0	= 0	= 1
08-0F	168-175	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL			
00-07	176-183	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL	= 1		
08-0F	184-191	LLLL LLLL LLLL LLLL HLLL HLLL HLLL HLLL			
00-07	192-199	HLLL LHLL LLLL LLLL LLLL LLLL LLLL LLLL	= 0	= 0	= 1
08-0F	200-207	HHLL HLLL LLLL LLLL LLLL LLLL LLLL LLLL			
00-07	208-215	LLLL LLLL LLLL LLLL HLLL HLLL HHLL HHLL	= 1		
08-0F	216-223	LLLL LLLL LLLL LLLL LHLL LHLL HLLL HLLL			
00-07	224-231	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL	= 0	= 0	= 1
08-0F	232-239	LLLL LLLL LLLL LLLL LLLL LLLL LLLL LLLL			
00-07	240-247	LLLL LLLL LLLL LLLL HLLL HLLL HHLL HHLL	= 1		
08-0F	248-255	LLLL LLLL LLLL LLLL LHLL LHLL HLLL HLLL			

Table 2-33. Critical Patterns for Precompensation

Data Pattern (F2 F1 P N)	Reversed Pattern (N P F1 F2)	Reversed Hexadecimal	Compensating Correction
0 0 1 1	1 1 0 0	C	Data late
1 0 1 1	1 1 0 1	D	Data late
1 0 0 0	0 0 0 1	1	Clock late
0 1 1 0	0 1 1 0	6	Data early
1 1 1 0	0 1 1 1	7	Data early
0 0 0 1	1 0 0 0	8	Clock early

ROM output bits D4 and D3 are a two-bit code that steers the write data encoding multiplexer as follows:

ROM Output D4 D3 D2 D1	Multiplexer Output
0 0 X X	Hardwired 1 (no pulse)
0 1 X X	CLKINLL- (late)
1 0 X X	SHIFTCLKTT or SHIFTCLKTP (on time)
1 1 X X	DTAINEE (early)

The phasing of the bit controller output signals is described in the following diagrams:

Write FM state diagram	Figure 2-61
Write FM timing	Figure 2-62
Write MFM state diagram	Figure 2-63
Write MFM timing	Figure 2-64

The standard address marks (in hexadecimal format) are:

Address Mark	Data Pattern	Clock Pattern
FM Index	FC	D7
FM ID	FE	C7
FM Data	FB	C7
FM Delete		
Data	F8	C7

Address Mark	Data Pattern	Clock Pattern
MFM ID	0A	Missing clock after second zero
MFM Data	0B	Same
Read Data Simulator	0D	Same

Address marks are also described with the write data encoding logic, paragraph 2.7.3.7, with clock/data patterns illustrated in Figure 2-79 and Figure 2-80.

Figure 2-84 shows the read data path from the output of the bit controller to the microprocessor data bus, as well as the address mark detection, phase correction, and CRC logic. The clock shift register, data shift register, and CRC logic are shared between read and write operations.

The phase correction logic provides a gross (180-degree) correction to the clock/data window and the bit controller/PLL clock circuitry provides fine correction. The address mark detection logic provides a starting reference point for the word controller. The word controller determines the word boundaries for the remainder of the record. The CRC logic recalculates the cyclic redundancy check word and checks it against the previously recorded CRC word.

Address mark detection and phase correction are both based on detecting missing clock patterns at the clock shift register output. A logic 1 in the clock shift register is a pointer to a missing clock pulse in the input data stream. The shift register outputs serve as address inputs to the address mark detection and phase correction ROM. The DSMFM control signal (address LSB) identifies the type of encoding.

If the missing clock pattern agrees with one of the predefined patterns for that encoding mode, the ADDRMARK output goes high. After one stage of clock synchronization, ADDRMARKQ is routed through the read/write multiplexer (as COMMON). The address mark input allows the word controller sequence to proceed from a reference point (state E) and cycle repetitively for the remainder of the record. Refer to the word controller read mode description for additional information. The important thing is that the address mark provides an initial word boundary reference, and the word controller derives the remaining word boundaries by keeping track of bit controller shift data (SHIFTDTAQ) outputs.

Address marks are limited to three missing clock pulses in an eight-bit byte. If four clock pulses are missing, the clock/data window is reversed, and the window F/F should be toggled by a CHANGEPULSE signal.

The window is also toggled by the bit controller WINDOWIN output as a normal part of the clock/data separation cycle. The window toggle pulse (TOGGLEW) is an exclusive-OR of the WINDOWIN and CHANGEPULSE signals.

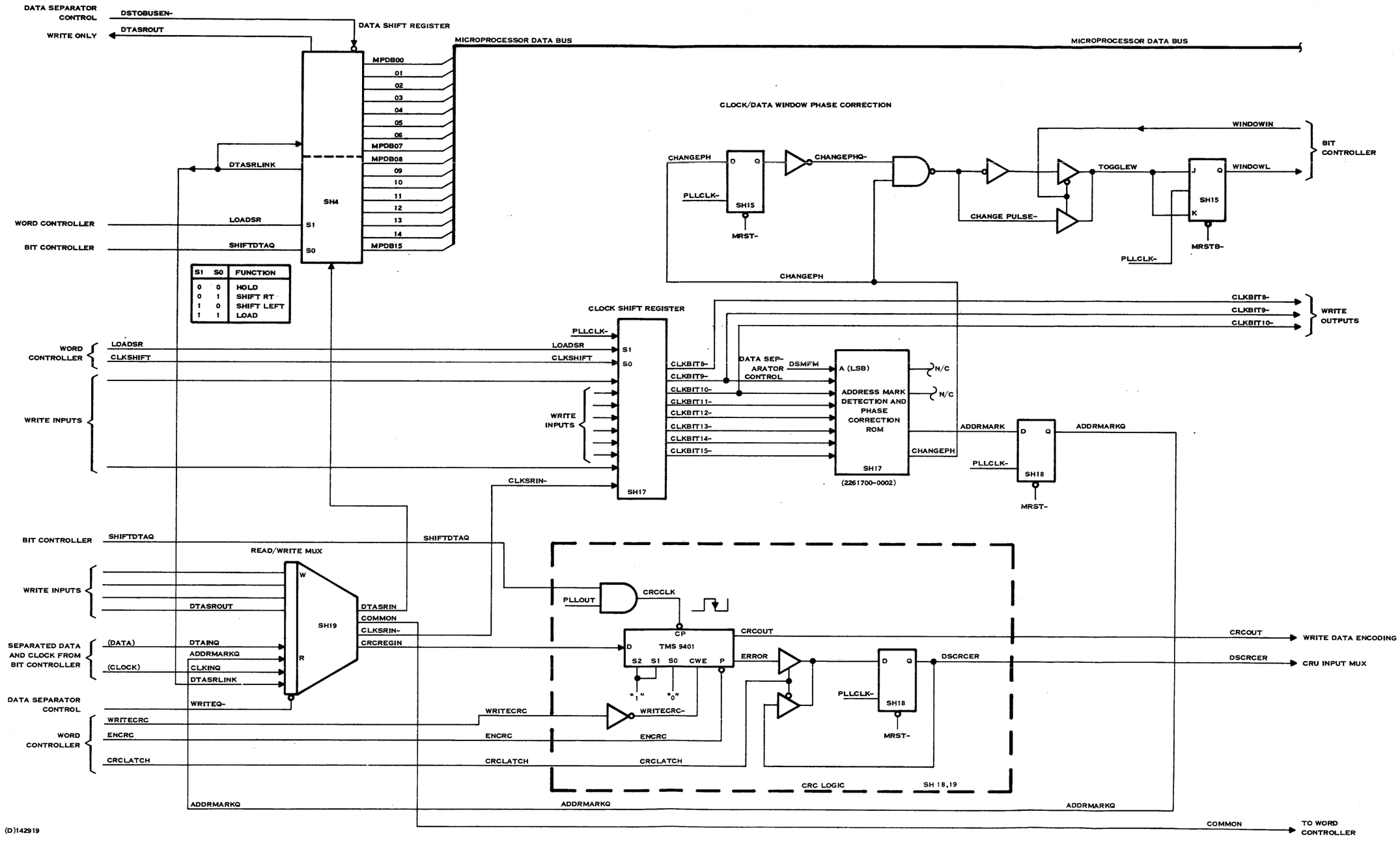


Figure 2-84. Address Mark Detection, Phase Correction, and CRC Logic

The duration of the CHANGEPULSE signal is less than a full PLL clock period. The exact duration is dependent on the switching time of the clock shift register and other F/Fs, the ROM access time, and gate delays. The trailing edge of PLL clock shifts the critical pattern to the output of the clock shift register, and CHANGEPH goes high after the ROM access time. The switching time plus the access time is on the order of 60 nanoseconds. CHANGEPULSE- goes low after the NAND gate delay (10 nanoseconds) and CHANGEPULSE goes high after another gate delay. CHANGEPULSE and its complement remain active until after the trailing edge of the next PLL clock pulse sets the CHANGEPHQ F/F. The same PLL clock edge loads the final output (TOGGLEW) into the J and K inputs of the WINDOWL F/F.

Figure 2-85 shows the input and output bit assignments for the address mark detection and phase correction ROM. This figure also shows the critical missing clock patterns that identify window errors or address marks. Note that the ROM is not programmed to recognize an FM index address mark. The TFDC takes no special action at the index mark, and there is no data word recorded at the index.

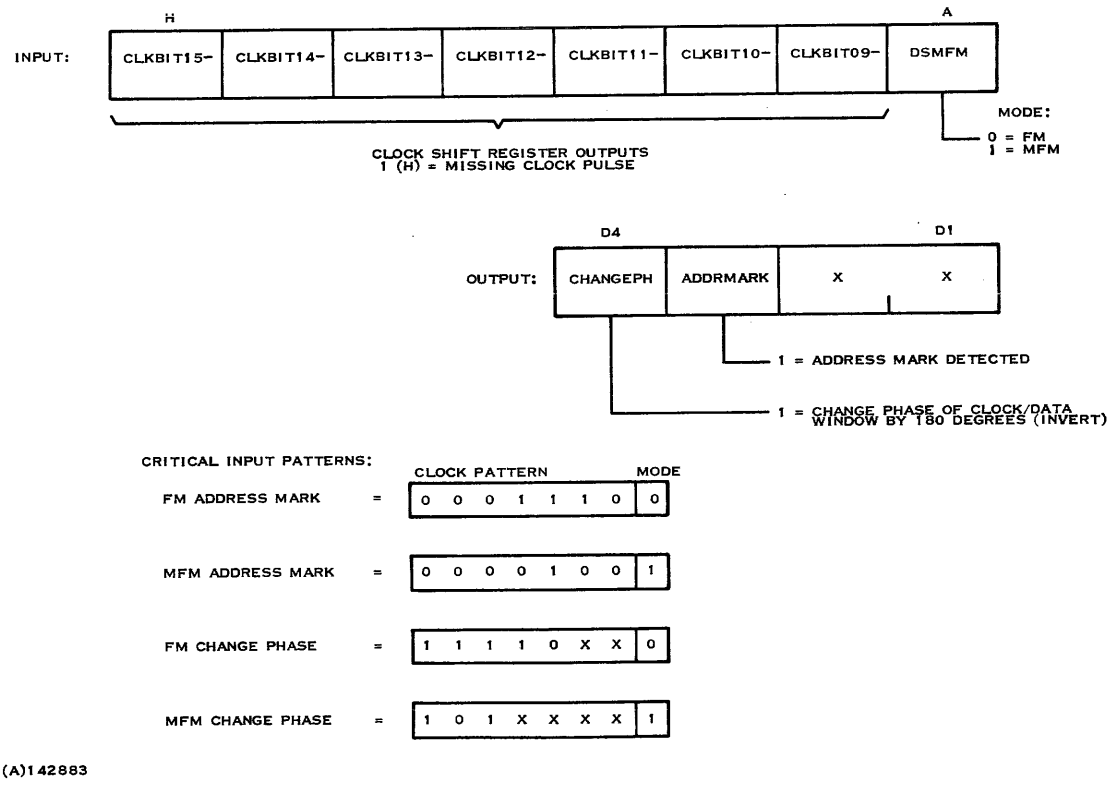


Figure 2-85. Input/Output Bit Assignments for Address Mark Detection and Phase Correction ROM

Table 2-34 is a listing of the ROM contents. The listing is divided into alternate FM and MFM columns, as DSMFM is the address LSB.

Table 2-34. Address Mark Detection and Phase Correction ROM

Input* (Hex) Address	Input (Decimal) Address	FM	MFM	FM	MFM	FM	MFM	FM	MFM	
00-07	00-007	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
08-0F	08-015	LLLL	LHHH	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	MFM Address Mark
10-17	16-023	LLLL	LLLL	LLLL	LLLL	LLHH	LLLL	LLLL	LLLL	
18-1F	24-031	LLLL	LLLL	LLLL	LLLL	LHLH	LLLL	LLLL	LLLL	FM Address Mark
20-27	32-039	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
28-2F	40-047	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
30-37	48-055	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
38-3F	56-063	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
40-47	64-071	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
48-4F	72-079	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
50-57	80-087	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
58-5F	88-095	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
60-67	96-103	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
68-6F	104-111	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
70-77	112-119	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
78-7F	120-127	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
80-87	128-135	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
88-8F	136-143	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
90-97	144-151	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
98-9F	152-159	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
A0-A7	160-167	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	MFM
A8-AF	168-175	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	Change
B0-B7	176-183	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	Phase
B8-BF	184-191	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	Outputs
C0-C7	192-199	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
C8-CF	200-207	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
D0-D7	208-215	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
D8-DF	216-223	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
E0-E7	224-231	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
E8-EF	232-239	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	
F0-F7	240-247	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	HLLL	LLLL	FM Change
F8-FF	248-255	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	LLLL	

Note: * Convert hex input address to missing clock pattern by converting to binary and omitting LSB (MFM/FM select)

Figure 2-86 and Figure 2-87 show phase correction timing for FM and MFM read operations. Figure 2-88 and Figure 2-89 show timing for FM and MFM address mark detection.

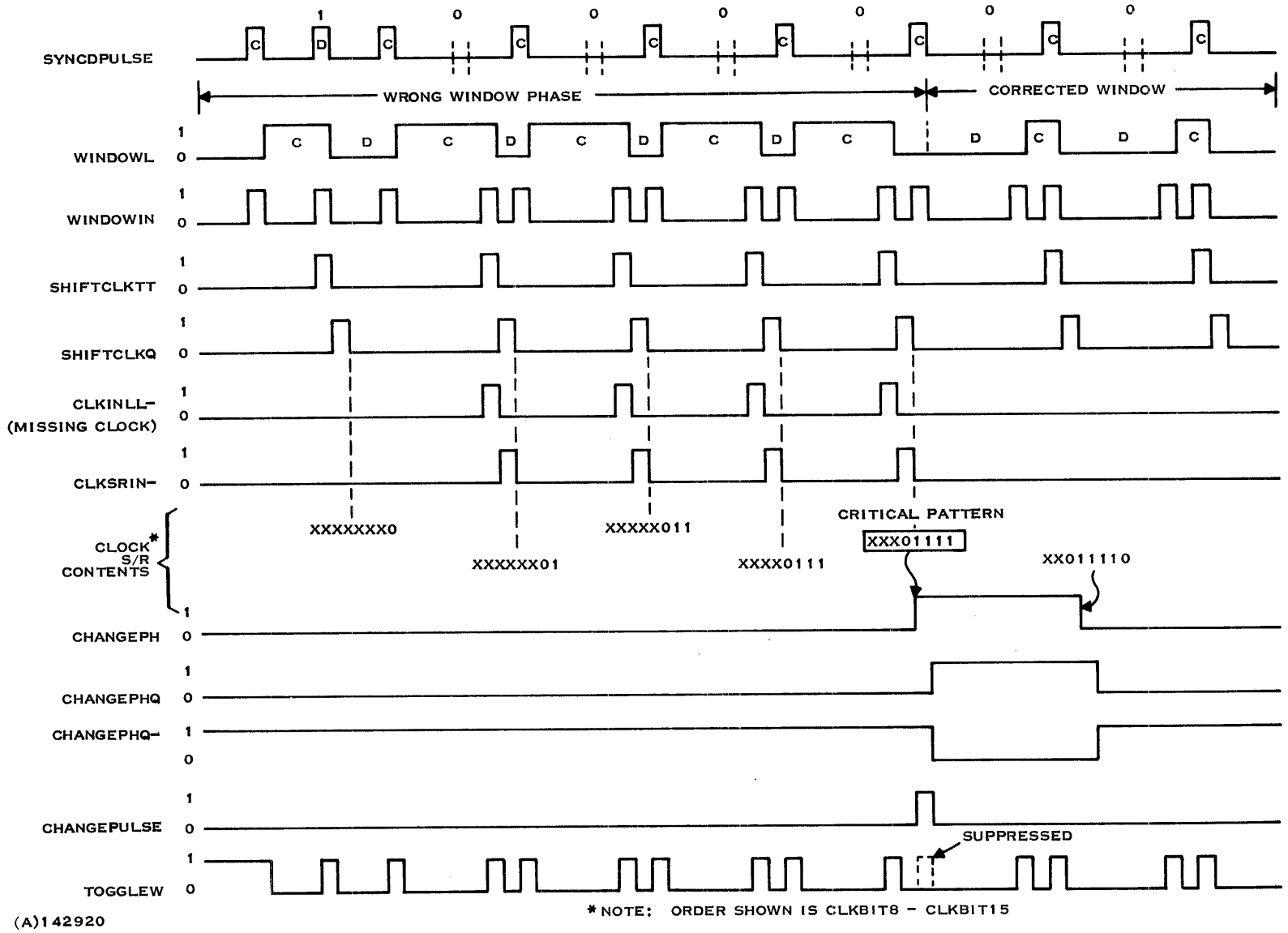


Figure 2-86. FM Phase Correction Timing

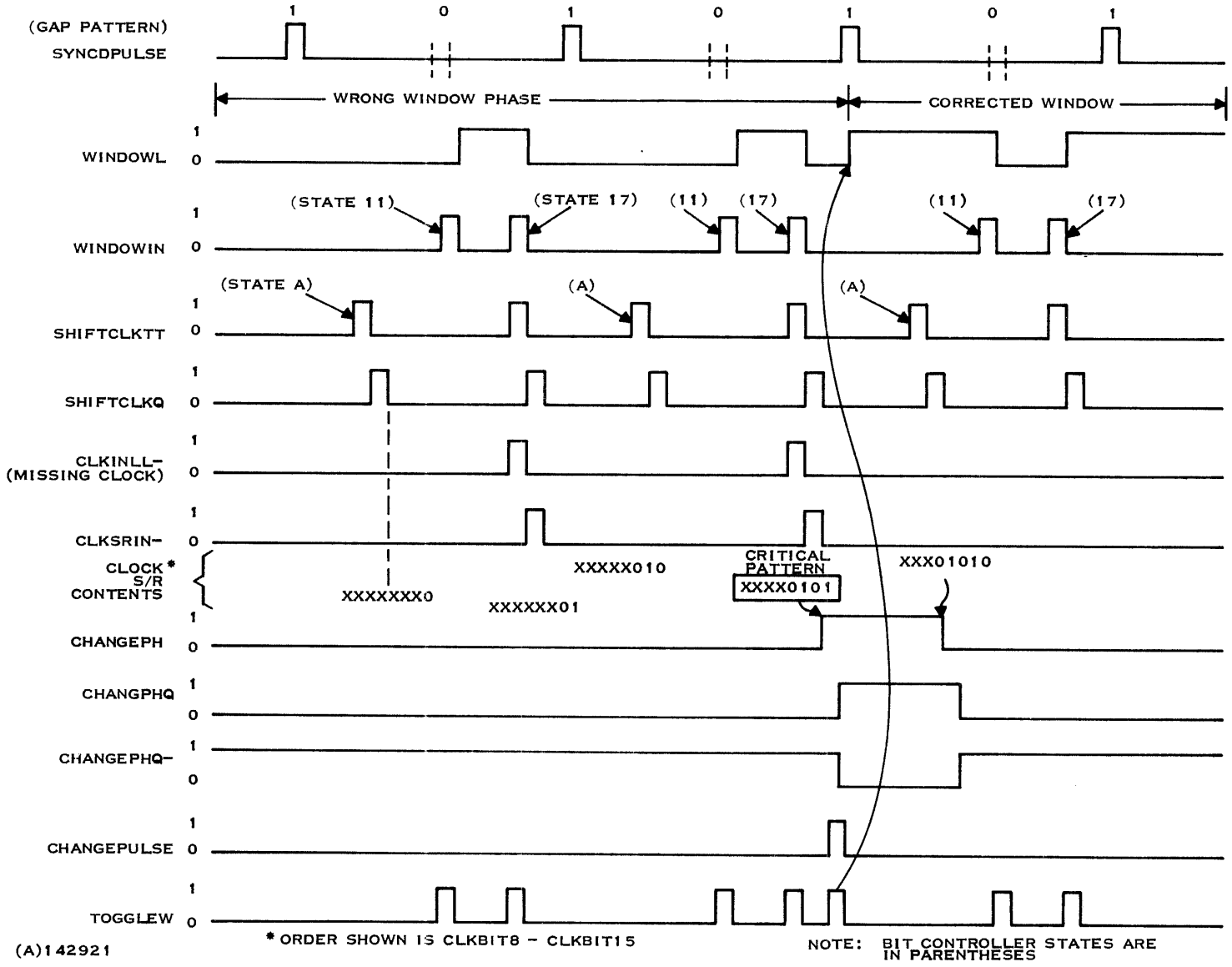


Figure 2-87. MFM Phase Correction Timing

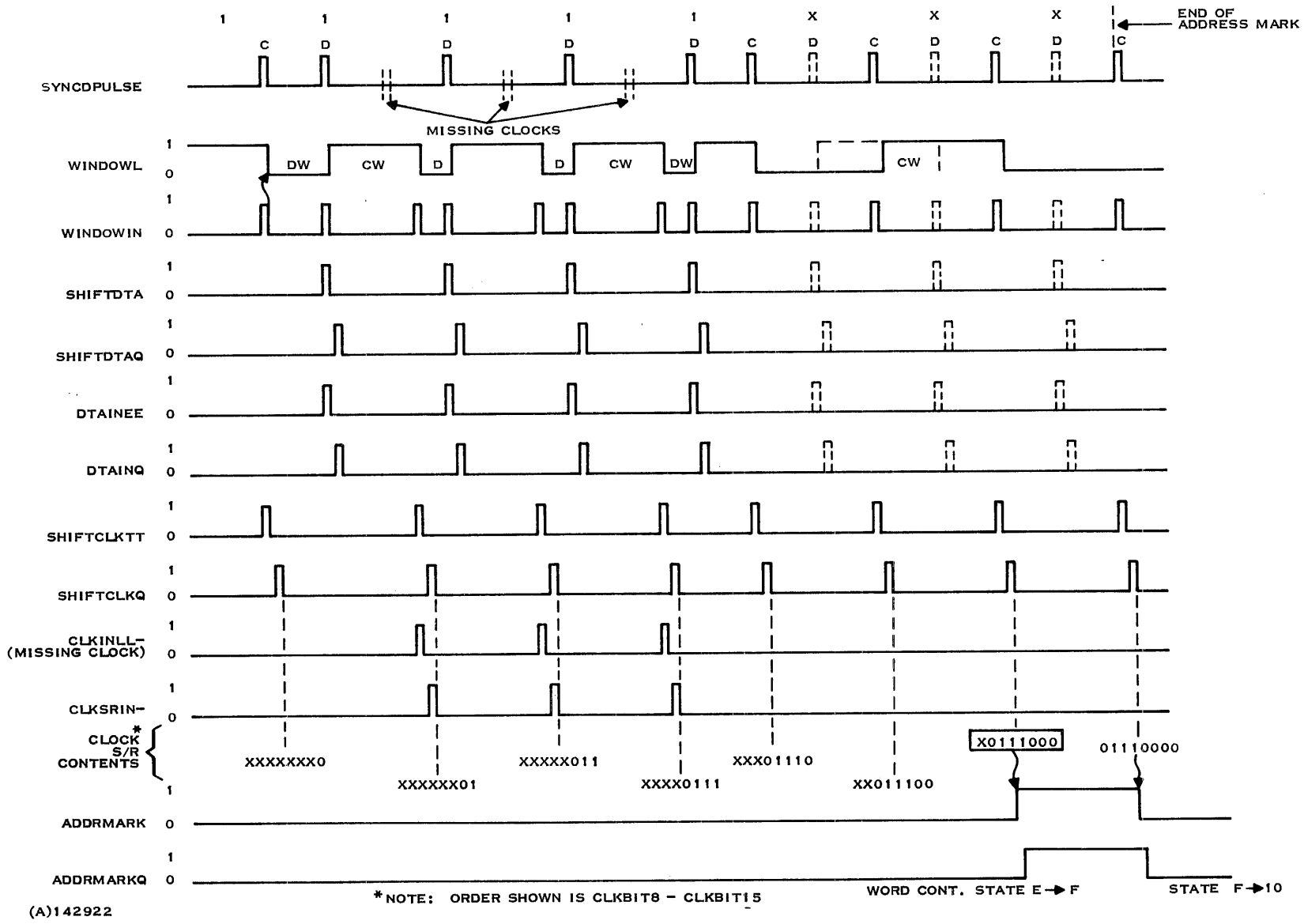


Figure 2-88. FM Address Mark Detection Timing

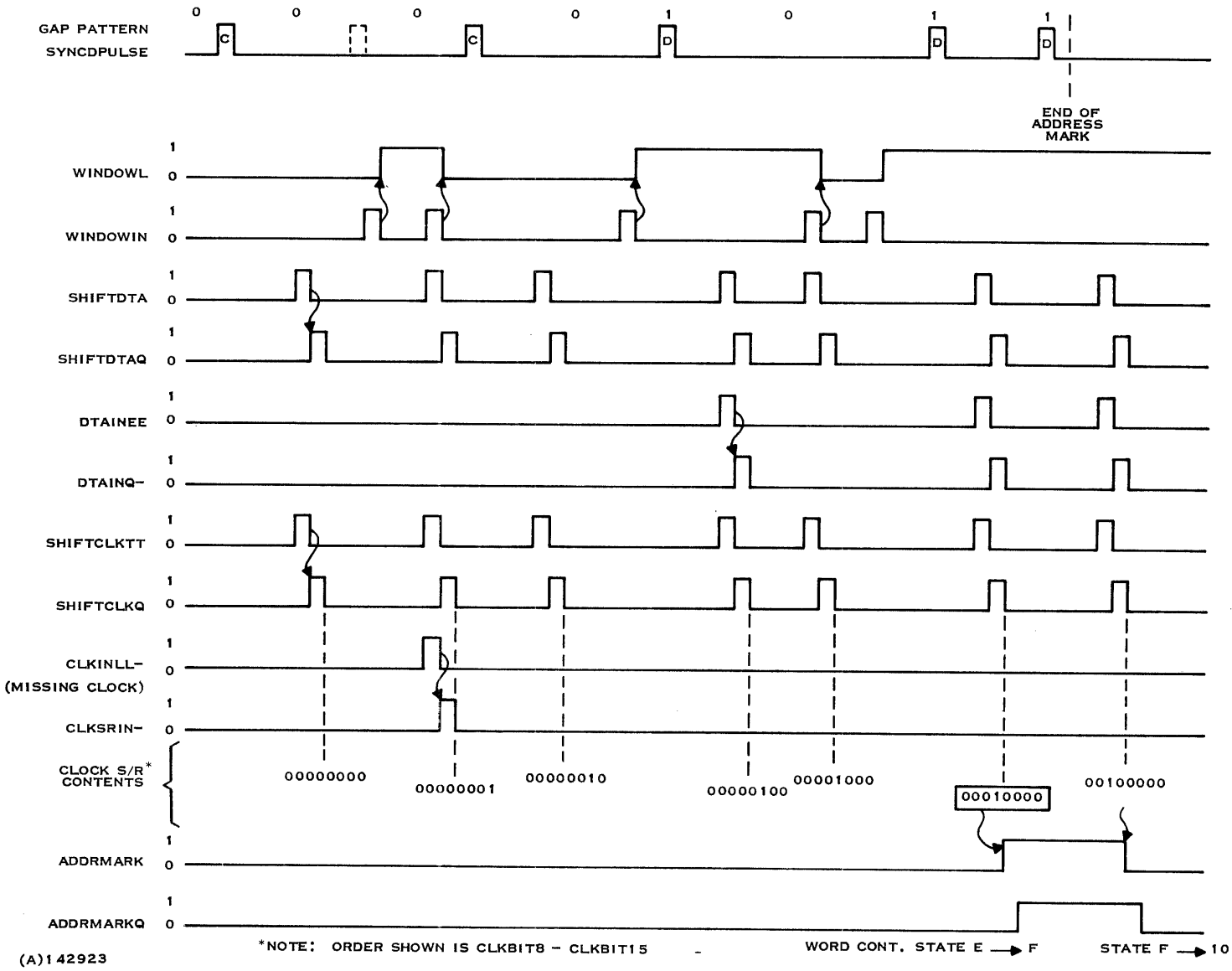


Figure 2-89. MFM Address Mark Detection Timing

2.7.3.9 Cyclic Redundancy Check (CRC) Circuitry. The CRC provides a rigorous method of error detection over the course of an entire data record. All the serial data in a record is processed by an error-checking algorithm as it is transmitted to the disk drive. The result of the CRC calculation is a 16-bit CRC character that is transmitted at the end of the record. When the record is read back, the read data is reprocessed according to the same checking algorithm. At the end of the record, the CRC character calculated during the read operation must compare to the CRC character recorded at write time or an error has occurred.

The disk controller uses a 9401 programmable CRC generator/checker. The programming inputs are hardwired to permanently select the CRC-CCITT algorithm. This algorithm divides the write data stream by the polynomial $X^{16} + X^{12} + X^5 + 1$. The CRC character is the remainder left after that modulo 2 division. During read operations, the record is again divided by the polynomial. When the recorded CRC is shifted into the 9401, the new remainder and the recorded CRC character should cancel, leaving all zeros in the CRC generator internal register.

The important thing to know about the CRC is that it is much superior to a simple parity check. A parity check can only detect odd numbers of errors. The CRC algorithm used in the disk controller can detect:

- All odd numbers of error bits
- All 16-bit or shorter error bursts
- More than 99.9% of all 17-bit and longer error bursts

These error burst figures assume a single error burst in the transmission.

Figure 2-90 is the equivalent circuit for the 9401 CRC generator/checker as used in the disk controller. The CRC generator has flip-flop stages connected as a feedback shift register. The exclusive-OR gates in the feedback chain correspond to the terms of the CRC polynomial.

All stages in the 9401 must be preset to ones just before processing a write or read data record. A low ENCRC signal holds the generator preset at all times when it is not calculating, transmitting, or checking the CRC word.

WRITECRC- must be high to allow read or write data to be shifted into the CRC generator. For write operation, WRITECRC- must go low at the end of the record to allow the CRC character to be shifted out of the CRC generator. WRITECRC- is controlled by the SETWRITECRC output of the word controller ROM and is synchronized to PLLCLK in the output register and synchronizer.

CRCREGIN is the serial read or write data input to the CRC generator/checker. CRC clock, CRCCLK, loads the data on the negative-going (trailing) edge. This corresponds to the trailing edge of PLL clock.

The CRC character is serially transmitted out of the 9401 on the CRCOUT line. The ERROR output is valid at the end of a read operation, at which time the CRC generator/checker internal registers should contain all zeros.

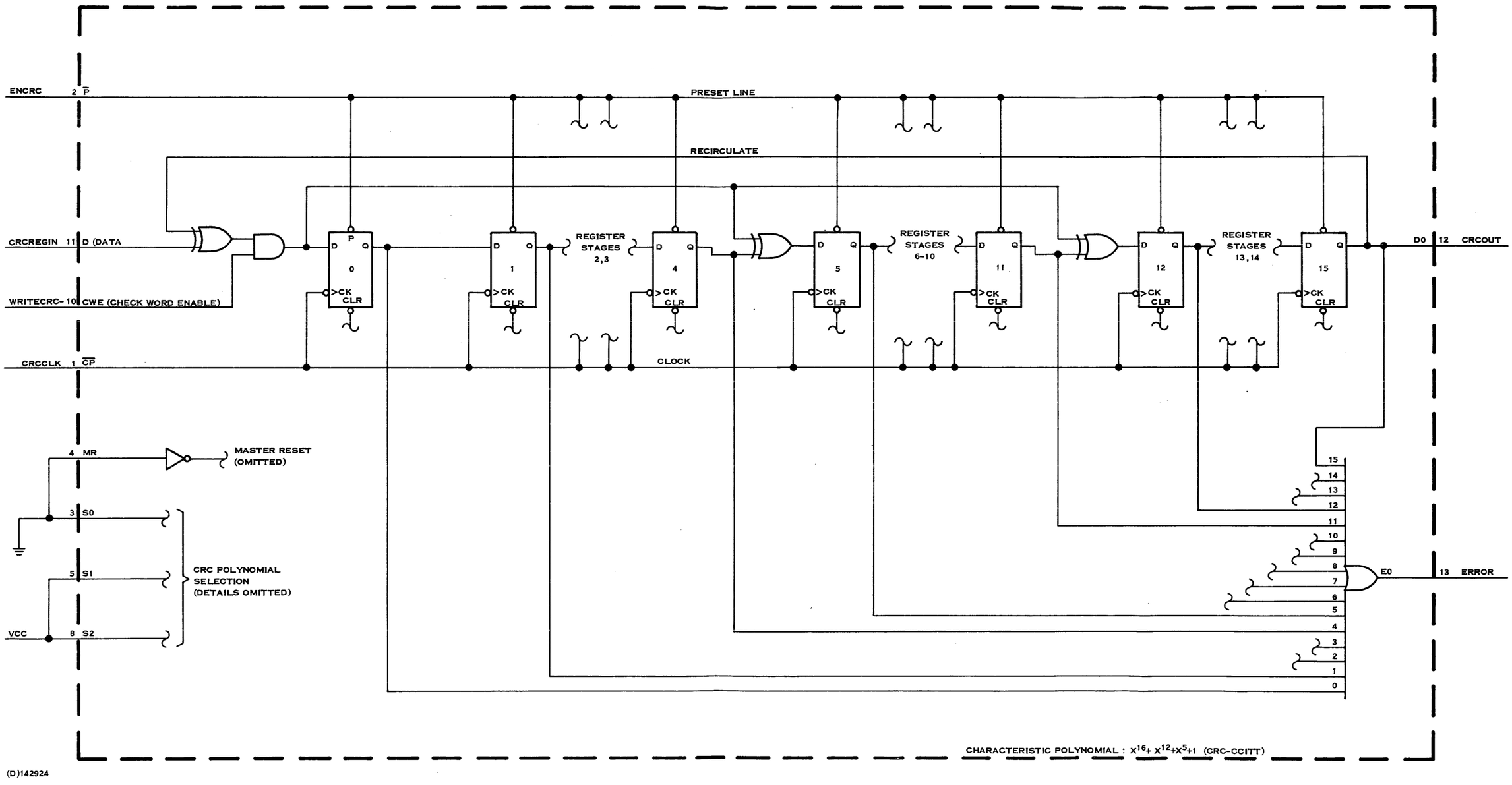


Figure 2-90. Equivalent Circuit for CRC Generation

Figure 2-84 shows the CRC generator/checker and the read/write multiplexer. The multiplexer selects read data (DTASRLINK) or write data (DTASROUT) as the data input, CRCREGIN. DTASRLINK is taken from an intermediate point in the data shift register, and lags the input word by eight bits. DTASROUT is the MSB output of the shift register that goes to the extension register input and to the CRC generator.

The word controller holds the CRC internal register preset (all ones) during the write gap operation. The first word of a write data operation contains the gap pattern in the first byte and an ID address mark or data address mark in the second byte. The word controller holds the CRC generator preset (ENCRC = 0) for the eight bit times required to shift the gap pattern out of the data shift register. After eight bit times the SETENCRC output of the word controller is enabled, and the ENCRC F/F sets on the next PLL clock.

For the next eight bit times and for the remainder of the data record, the word controller cycles through a 16-state loop (states 8–17) with the CRC logic enabled (ENCRC = 1, WRITECRC = 0). Thus, the address mark is included in the CRC calculation.

At the end of the data record, the data separator control logic commands the word controller to switch from the write data to the write CRC sequence. A sequence switch can only be performed on a word boundary. The write data sequence halts on word controller state F. The write CRC sequence starts at state F and continues for the 16 states necessary to shift the CRC word. The SETWRITECRC output at state F sets the WRITECRC F/F, which selects the CRCOUT line as the extension register data input.

At the end of the write CRC sequence, the data separator switches back to a write gap or write gap recirculate operation. If the data separator simply stopped at this point, the two shift pulses necessary to get the last bit encoded (to the extension register PRESENT output) would not be generated.

During data read operations, the CRC logic processes input data tapped from the midpoint (DTASRLINK) of the data shift register. The ERROR output is sampled and latched once every 16 bit times as DSCRCER. DSCRCER becomes a valid error check 1.5 word times after the last data word is ready at the shift register output. DSCRCER is a CRU input to the TMS 9900 microprocessor. A detected CRC error causes a preprogrammed number of read retries by the 9900 control program. If the retries are unsuccessful, the controller sets the data error and error summary bits in status word W7. Additional retries may be programmed into the device service routine (DSR) of the operating system.

2.7.4 Drive Interface (Local and Remote I/O Ports)

The drive interface circuitry is responsible for communication with the drive chassis. This circuitry includes line drivers, line receivers, bus terminators, and control/status signal encoding and decoding logic.

2.7.4.1 Local and Remote Port Introduction. The TILINE flexible disk controller may be used with drives packaged in the domestic chassis or in the international chassis. Drives installed in the domestic chassis communicate with the controller over a local bus that includes a 50-pin flat daisy-chain cable connected in parallel to all drive units.

FD1000A and FD1000B systems are supplied with the international chassis. The international chassis is capable of operating with the local bus or with the remote bus. However, all standard FD1000A/B systems with international chassis use one or both of the TFDC remote bus ports. The controller board and the international chassis communicate via one of the 15-pin remote bus connectors on the controller board and a shielded, multiple twisted-pair cable.

The basic signals needed for control and operation of a flexible disk drive are supplied directly over the local bus to drives installed in a domestic chassis, as shown in Figure 2-1. In the international chassis, the power supply/interface board connects to the drives via an intrachassis bus. The power supply/interface board performs the necessary signal conversions between the remote bus and the intrachassis bus, as shown in Figure 2-2.

The drive input/output signals fall into five groups; write, read, access control, diskette rotational position (index), and drive status. These signals are described in Table 2-35. Signal names (signatures) that apply to the intrachassis bus are given in parentheses.

Table 2-35. Drive Unit Interface Signals

Signal Name*	Drive Pin Number	Description
		Controller to Disk
LWRDAT- (WDATA-)	P1 - 38	Write data and clock. Encoded in FM mode for single-sided diskettes, modified FM (MFM) mode for double-sided diskettes. Each transition from the inactive state to the active (low) state causes a flux reversal on the diskette.
LWRTEN- (WRTENA-)	40	Write gate. Low to enable write current and to disable head motion circuits. High to enable read operations.
TR43YE- (TR43-)	2	Low current. When low, this signal reduces write current by 20% allowing greater read resolution on the inner tracks (43-76). Should be high when writing on tracks 0 through 42.
LDIR- (DIR-/SIDE SEL)	34	Direction/head select. This dual purpose line is used to control the direction of head motion when the write gate is off. When LDIR- is high, each stepping pulse (LSTEP-) moves the head assembly one track toward the outer edge of the diskette. When LDIR- is low, each stepping pulse moves the heads one track in toward the center of the diskette. In the absence of stepping pulses, this signal is high to select head 0 (lower surface) and low to select head 1 (upper surface). Note that stepping pulses never occur during read/write operations.
LSTEP- (STEP-)	36	Step pulse. Each active low stepping pulse moves the head assembly one track position in or out, depending on the level on the LDIR- line.

Table 2-35. Drive Unit Interface Signals (Continued)

Signal Name*	Drive Pin Number	Description
LLOAD- (LOAD-)	18	Head load. When the disk drive is ready (LRDY- low), a low head load signal will load the heads onto the diskette surface. Head load is strapped to the In Use signal within the drive so that head load also latches the drive door lock. This prevents inadvertent removal of a diskette during read/write operations. Head load is latched in the drive on the leading edge of drive select, to allow overlapped operations between drives without the penalty of head load settling times.
LINUSE- (INUSE-)	16	In use. Provided to latch the drive door lock, but unnecessary with the standard jumper options provided. (See head load, pin 18.)
LSEL0- LSEL1- LSEL2- LSEL3- (SEL0- through SEL3-)	26 28 30 32	Drive select one through drive select four. A disk drive may not accept any signals from the controller or supply any outputs unless an active low drive select input corresponds to the position of the drive select jumper in that drive. Note that the input signals are labeled from 0 through 3 and the jumper positions are labeled from 1 through 4.
		Disk to Controller
LINDEX- (INDEXE-)	20	Index pulse. Generated once per diskette revolution when the index hole rotates under the index cutout in the diskette jacket. The leading (negative-going) edge of this 1.8 millisecond pulse serves as the reference for the beginning of the track.
LRDAT- (RDATE-)	46	Read data and clock from the diskette, after amplification, shaping, and other processing in the disk drive electronics. Encoded in FM mode for single-sided diskettes; MFM mode for double-sided diskettes.
LWP- (WPE-)	44	Write protect. When low, indicates that the diskette jacket has an uncovered write protect notch so that writing to the diskette is inhibited.
LTR00- (TR0E-)	42	Track 0. When low, indicates that the read/write heads are positioned over diskette track 00. Used by the controller to check satisfactory execution of the Restore command.
LRDY- (RDYE-)	22	Drive ready. When low, indicates that the drive is selected, power is applied to the drive, a diskette is installed, the door is closed, and the disk is rotating. Remains active (low) as long as all these conditions are met.

Table 2-35. Drive Unit Interface Signals (Continued)

Signal Name*	Drive Pin Number	Description
LDC- (DCE-)	12	Disk change. A low output that indicates that the drive has gone to a not ready (door open) condition while not selected. Disk change will also be active the first time the drive is selected after power-up. Therefore, if a drive, when selected, indicates both ready (READY-) and disk change, it is necessary to deselect the drive and then reselect it. Usually a Restore command and a Store Register command are used when disk change is detected. Restore ensures physical position of the heads after a power cycle or a diskette change, and Store Registers identifies the diskette type (SSSD/DSDD).
LTS- (TSE-)	10	Two-sided. Low if a double-sided diskette is installed; high if a single-sided diskette is installed. The drive and drive electronics automatically detect the diskette type by the position of the index hole cutout in the diskette jacket.

Note:

* Signal names in parentheses apply to drive I/O signals in the international chassis (intrachassis bus).

Each of the two remote ports may serve one international chassis with one or two drive units. Remote bus signals are transmitted between the controller and the international chassis power supply/interface board by differential line driver/receiver pairs and balanced, twisted-pair lines. A grounded shield that surrounds the remote cable suppresses electromagnetic radiation and pickup. Cable lengths of up to 100 meters are practical with the remote bus.

The clock, read data, write data, and write gate signals each require a twisted pair in the remote cable. The other control and status signals required for controller-drive communication do not have such severe timing requirements. The control signal outputs to the international chassis are multiplexed into a composite control signal and transmitted over a single twisted pair. The power supply/interface board demultiplexes the composite signal and supplies the reconstituted signals to the drives over the intrachassis bus.

In a similar manner, the power supply/interface board multiplexes drive status signals from the intrachassis bus into a composite status signal for transmission to the controller. The remote port logic in the controller decodes the incoming status signals and connects the outputs in parallel with the local bus inputs.

The outputs of both controller remote ports are identical except that they are provided by different line drivers. Only the drive specified by the drive select signal may accept write data and commands (other than drive select) from the chassis local bus. Similarly, the selected drive is the only

one that may supply read data and status outputs for transmission to the controller. Drive selection is determined by the drive select output of the controller and the position of the drive select jumper in the drive unit. There is no restriction as to which drive unit numbers must be assigned to a particular port.

Table 2-36 contains brief descriptions of the remote interface signals. Refer back to Table 2-35 for descriptions of the local bus signals.

Table 2-36. Remote Interface Signals

Signal Name	Pin Number	Description
		Controller to Chassis
YWDT1- YWDT2-	J4-7 J3-7	Write data and clock. Encoded in FM mode for single-sided diskettes, modified FM (MFM) mode for double-sided diskettes. Differential pair version of LWRDAT-.
YWEN1- YWEN2-	J4-5 J3-5	Write gate. Differential pair version of LWRTEN-.
YCLK1- YCLK2-	J4-2 J3-2	Multiplexer/demultiplexer clock. 500 kHz clock used for encoding and decoding control and status signals. Every ninth clock pulse is omitted to synchronize the TFDC and the power supply/interface.
YCNTL1- YCNTL2-	J4-4 J3-4	Multiplexed control signal. Includes a two-microsecond synchronization period followed by eight time slots of two microseconds each for the following control signals: TR43- SEL0- SEL1- SEL2- SEL3- DIR-/SIDE SELECT STEP- LOAD-
		Chassis to Controller
YRDAT1- YRDAT2-	J4-9 J3-9	Read data and clock from the diskette, after amplification, shaping, and other processing in the disk drive electronics. Encoded in FM mode for single-sided diskettes, MFM mode for double-sided diskettes. Differential pair version of LRDAT-.

Table 2-36. Remote Interface Signals (Continued)

Signal Name	Pin Number	Description
YSTAT1- YSTAT2-	J4-11 J3-11	Multiplexed drive status signals timed by YCLK1- (or YCLK2-) from controller. Includes a two-microsecond synchronization interval, followed by eight time slots of two microseconds each, as follows: DPON- Disk power on RDYE- Ready INDEXE- Index TR0E- Track 00 WPE- Write protect TESTL- Loopback test, derived from DIR- DCE- Disk change TSE- Two sided

2.7.4.2 Drive Interface Logic. Refer to Figure 2-91, which shows the TFDC local and remote port logic. Read data and status inputs are shown on the left side of the figure, while write data, clock, and drive control outputs appear on the right side.

All the drive-controller interface signals are transmitted in active low form for better noise immunity and bus response. Local bus status and data inputs are resistively terminated by voltage divider networks close to the I/O connector. Decoded remote status inputs are inverted to active-low form by open-collector drivers and are paralleled with the local status inputs. The resulting local/remote status inputs are inverted by standard TTL inverters and sent to the CRU input multiplexer for sampling by the TMS 9900 microprocessor.

Read data inputs from the read data simulator, the local bus, and the remote bus 1 and 2 differential line receivers feed a single four-input NAND gate to produce the RDAT signal. Only one source may produce read data at a given time, so the NAND effectively acts as an inverter for the one active read data source. RDAT is the unseparated clock and data input to the read data input circuits of the data separator.

Drive control outputs are supplied by output ports on the TMS 9901 PIA device. These active-low signals are supplied in parallel to the remote status encoding multiplexer and the single-ended TTL local bus drivers. Critical signals, such as the head load command (LOAD-), the write gate (WRTEN-), and the four drive select lines are tied back to the +5 volt supply through pull-up resistors. This assures that these outputs are at a safe (inactive) level unless specifically commanded otherwise.

The write gate and head load outputs to either the local or remote bus are disabled by a TILINE power reset (TLPRES-) signal. TLPRES- low will force the drives to a safe state just before a dc power failure and will hold the safe state for a short delay time after power recovery.

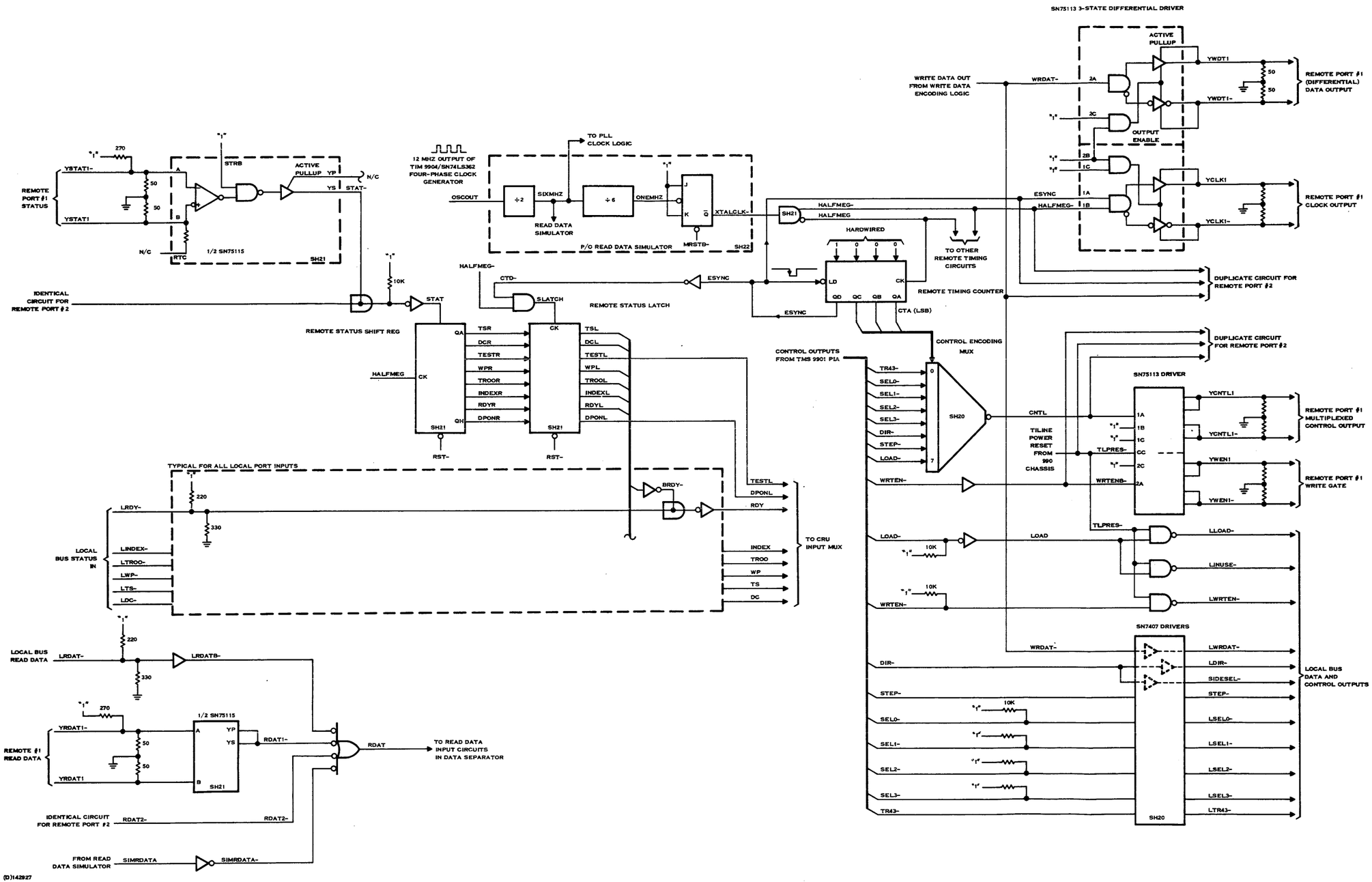


Figure 2-91. Drive Interface Circuits (Local and Remote I/O Ports)

The key to all remote bus control encoding and status decoding is the timing logic shown in the upper center of Figure 2-91. The 12-MHz OSCOUT pulse train from the four-phase microprosessor clock generator is divided to produce the 500-kHz complementary square waves, HALFMEG and HALFMEG-.

HALFMEG drives the SN74LS163 remote timing counter to produce three counter outputs (CTA, CTB, CTC) and a synchronization output, ESYNC. These counter outputs and the synchronization pulse define eight unique control frames and one synchronization frame. The count selects a control signal output to the remote control driver during each frame time. The synchronization frame allows the international chassis to decode the control signals in the correct order.

A composite synchronization and 500-kHz timing signal, YCLK1-, is transmitted to the international chassis. The synchronization term, which consists of one missing clock period, provides a starting point for the frame encoding/decoding logic of the international chassis. The international chassis reconstitutes the counter terms from the YCLK1- input, and uses them for decoding, sampling, and encoding multiplexed signals.

2.7.4.3 Remote Timing. Refer to the remote port timing diagram, Figure 2-92. The remote timing counter runs constantly while power is applied to the TFDC board. This is an SN74LS163 counter with synchronous load. The counter changes state on the low-to-high transition of HALFMEG. The normal binary counter cycle is modified by a feedback connection from the most significant bit output (ESYNC) to the synchronous load input. Each time the counter saturates, it rolls over normally to 0000 for one clock period and then preloads to eight (binary 1000) instead of advancing to state 0001. Therefore, the counter cycle is 0000, 1000, 1001, ...1110, 1111, 0000, 1000, and so forth.

The three least significant counter outputs, CTA, CTB, and CTC are the steering inputs to the 8:1 control signal encoding multiplexer. The multiplexer cycle is 000, 000, 001, 010,..., 111, 000, 000. The resulting encoded control signal, CNTL, has the track 43 signal selected for two frame times and each of the other inputs selected for one frame time. The double-width frame is important in synchronizing the decoder logic of the international chassis.

The composite clock and synchronization pulse train, YCLK1-, has clock pulses suppressed for the duration of ESYNC (two microseconds). This suppressed period plus the normal inactive period of the waveform adds up to a total of three microseconds. The YCLK1- signal and the YCNTL1- signal are transmitted over different twisted pairs in the same cable. Any skew between these two signals should be insignificant compared to the three-microsecond synchronization period. One-shots and counter circuitry in the international chassis reconstitute the timing for decoding control and for encoding drive status signals.

The SLATCH signal shown on the timing diagram applies only to decoding status signals returned from the international chassis. Encoded status signals from the international chassis are clocked into the remote status shift register on the positive-going edge of HALFMEG. SLATCH causes a parallel load from the remote status shift register to a latching register when a full status word is properly established in the shift register. The SLATCH pulse is delayed one half clock period (one microsecond) from the last shift pulse because SLATCH is derived from HALFMEG- . Shift timing is shown in Figure 2-93. The serial decoding scheme used here assumes that the overall clock delay to and from the international chassis is less than one microsecond (one half of a clock period). At the 100 meter maximum cable length, the round-trip delay is on the order of 700–800 nanoseconds.

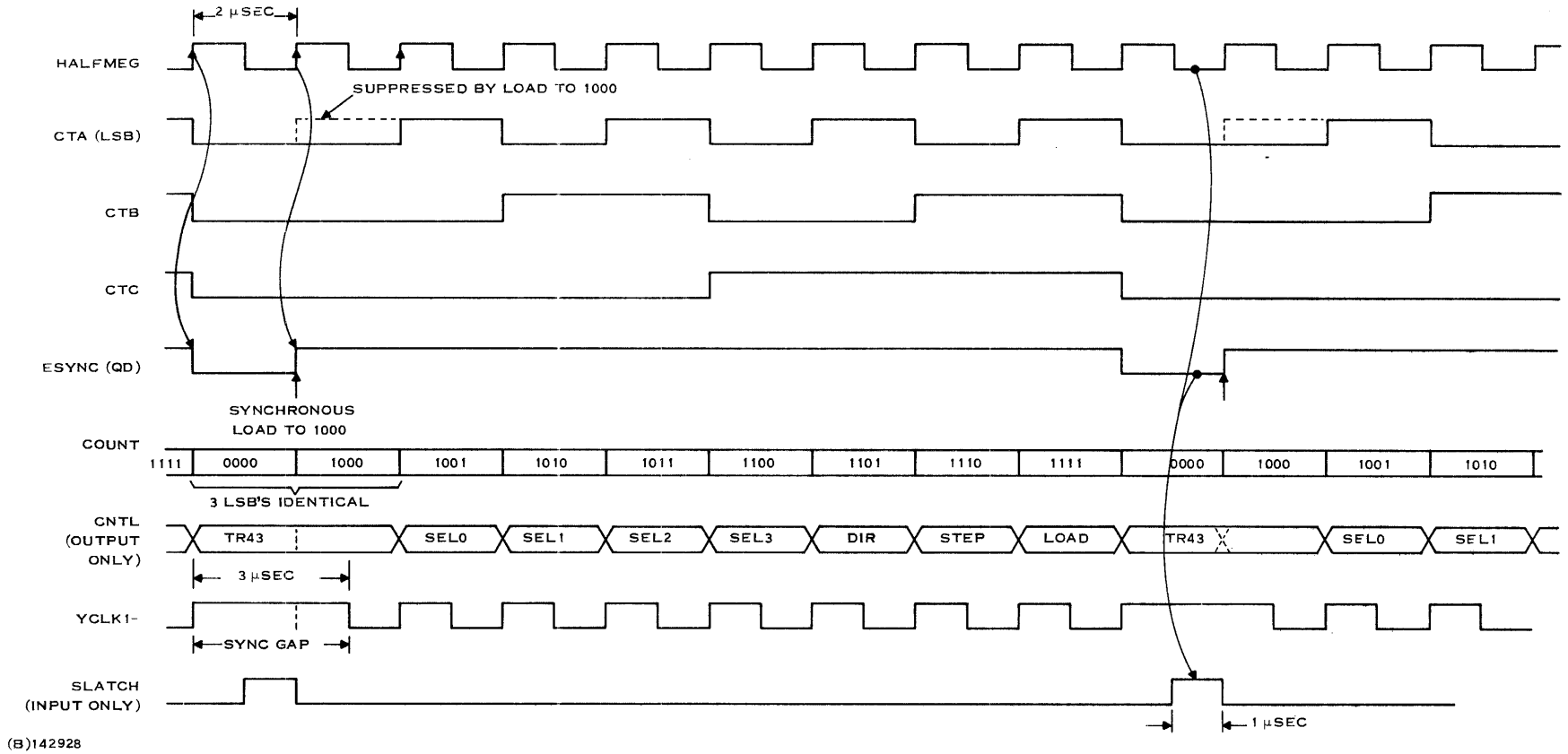


Figure 2-92. Remote Port Timing

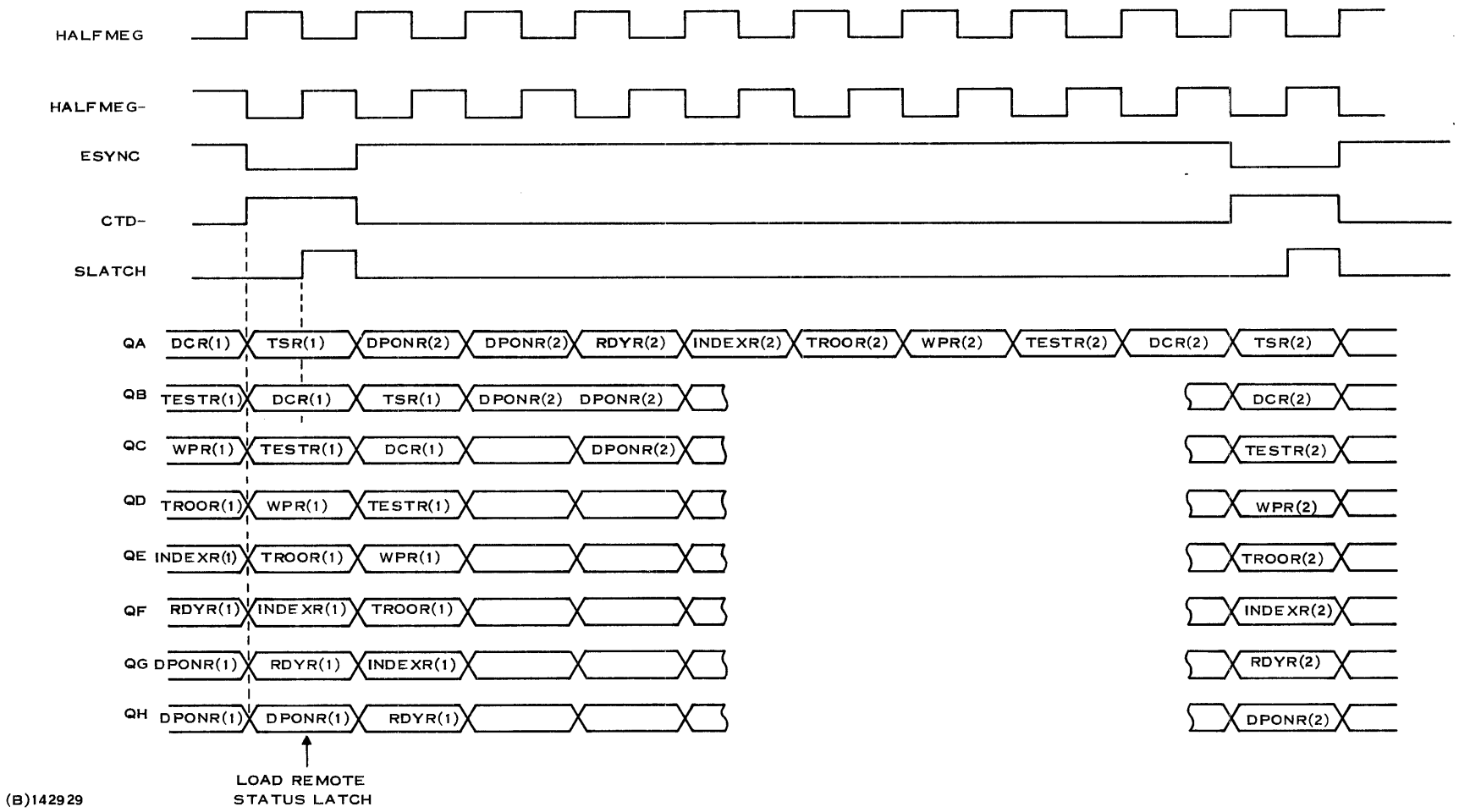


Figure 2-93. Remote Port Read Status Timing

The status values latched in the register are connected in parallel with the corresponding remote bus status inputs. No interference occurs because only one drive in the FD1000 system (the selected drive) can supply status outputs to the controller.

2.8 READ DATA SIMULATOR

The TFDC board automatically executes a self-test sequence in response to a reset. One of the self-tests is a data separator test which checks the ability of the data separator logic to properly decode a simulated MFM data pattern. The read data simulator provides an MFM data pattern that includes synchronization fields, a forced phase change, an address mark, five data words, and a simulated CRC word. This simulated data pattern feeds the front end of the data separator, checking all of the read logic except the input line receivers. Recall from the data separator description that most of the data separator logic is shared between the read and the write functions. This logic sharing makes the self-test even more comprehensive.

Additional information on the data separator self-test (DSTENT) is included in Section 3 and in Appendix B (9900 Control Program Listing).

2.8.1 Read Data Simulator Logic

The read data simulator logic is shown on sheet 22 of the logic drawing. The logic basically consists of a group of timing dividers (shared with the PLL and remote drive interface circuits), an address sequence counter, the read data simulator ROM, ROM output decoder, and an eight-bit parallel-to-serial shift register. The pulse train out of the shift register represents unseparated clock and data pulses. Pulse spacings, which are used to detect data, clock, and missing clock pulses, are determined by the contents of the ROM. Pulse widths are different than read data, but the read data input circuits of the data separator convert all incoming pulse widths to a standard width (one PLL clock period).

The SN74LS163 binary counter divides the 6-MHz input frequency (SIXMHZ) down to a 750-kHz address clock (ADDRCLK). ADDRCLK, in turn, drives the SN74LS393 address sequence counter. A straight binary sequence ($00-FF_{16}$) steps the ROM through addresses $000-255_{10}$ at a rate of one address every 1.3333 microseconds.

A four-bit word is stored at each ROM address. The MSB of the word (PULSEN) is an enabling signal to the SN74LS138 3:8 decoder. If PULSEN is low, the decoder output is forced to all ones (FF_{16}). If PULSEN is high, the decoder is enabled, and a 0 appears on the output line (Y0-Y7) that corresponds to the number on PULSENC0-3. All other decoder output lines remain high.

A shift register load pulse (SIMLD-) is issued once every 1.3333 microseconds to load the decoder output into the eight-bit SN74LS166 shift register. Shifting occurs on the positive-going edge of SIXMHZ. Eight of the 166.667 nanosecond SIXMHZ shifting pulses occur every 1.3333 microseconds, so the shift register cycles continuously with a new word loaded as the last bit shifts out of the shift register. Each bit appears on the output for 166.667 nanoseconds.

Note that it is the spacing of the zeros in the shift register output that determines the timing of the simulated data pulses. Recall that the bit controller uses windows relative to the previously-detected pulse to decide if the present input pulse is a data one, a clock, a data zero, or a missing clock. The spacing of any two consecutive zeros is determined by the PULSENC0-2 codes of the two words that enable the decoder, and by the number of intervening words that disable the decoder. Pulse spacing and timing are described in greater detail in the following paragraphs.

2.8.2 Read Data Simulator ROM Listing

Table 2-37 is a listing of the read data simulator ROM contents. Input addresses are supplied by an eight-bit binary counter and step in numerical order from 000 to 255. A simulated output data pulse (low) is generated by any output word that has an H in the MSB position (PULSEN = 1). The code in the next three bits represents the position of the pulse with respect to the end of a 1.3333 microsecond window. Any word with an L in the MSB position represents a 1.3333 microsecond delay, and the remaining three bits of that word are meaningless.

Table 2-37. Read Data Simulator ROM Listing

Input Address								
000-007	LLLL	LLLL	HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL
008-015	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL
016-023	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL
024-031	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL
032-039	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL
040-047	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL
048-055	LLLL	LLLL	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL
056-063	4.0HLLL	LLLL	LLLL	4.0HLLL	LLLL	LLLL	3.1HHLH	LLLL
064-071	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH
072-079	LLLL	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	LLLL
080-087	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	3.0HLHH	LLLL	LLLL
088-095	4.0HLHH	LLLL	2.7HLHH	LLLL	2.7HLHH	LLLL	LLLL	3.3HHHH
096-103	2.3HLLH	LLLL	2.0HHLH	2.0HLLH	LLLL	2.0HHLH	2.0HLLH	LLLL
104-111	2.0HHLH	2.0HLLH	LLLL	2.3HLHH	LLLL	2.3HHLH	LLLL	2.3HHHH
112-119	2.0HLHH	LLLL	2.0HHHH	2.0HLHH	LLLL	2.0HHHH	2.0HLHH	LLLL
120-127	2.3HHLH	LLLL	2.7HHLH	LLLL	LLLL	4.0HHLH	LLLL	2.7HHLH
128-135	LLLL	2.7HHLH	LLLL	2.7HHLH	LLLL	LLLL	4.0HHLH	LLLL
136-143	LLLL	4.0HHLH	LLLL	2.7HHLH	LLLL	2.7HHLH	LLLL	2.3HHHH
144-151	2.3HLLH	LLLL	2.0HHLH	2.0HLLH	LLLL	2.0HHLH	2.0HLLH	LLLL
152-159	2.0HHLH	2.0HLLH	LLLL	2.3HLHH	LLLL	2.7HLHH	LLLL	3.0HLLH
160-167	LLLL	LLLL	3.0HHHH	LLLL	3.3HHLH	LLLL	LLLL	4.0HHLH
168-175	LLLL	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	3.0HLHH
176-183	LLLL	3.0HLLH	LLLL	LLLL	3.0HHHH	LLLL	3.0HHLH	LLLL
184-191	LLLL	4.0HHLH	LLLL	3.0HLHH	LLLL	3.0HLLH	LLLL	LLLL
192-199	3.0HHHH	LLLL	3.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	3.0HLHH
200-207	LLLL	2.7HLHH	LLLL	2.7HLHH	LLLL	LLLL	3.7HHLH	LLLL
208-215	LLLL	4.0HHLH	LLLL	3.0HLHH	LLLL	2.7HLHH	LLLL	2.3HHLH
216-223	LLLL	2.3HHHH	LLLL	3.7HLLH	LLLL	LLLL	4.0HLLH	LLLL
224-231	LLLL	4.0HLLH	LLLL	2.7HLLH	LLLL	2.3HLHH	LLLL	2.3HHLH
232-239	LLLL	2.7HHLH	LLLL	2.7HHLH	LLLL	2.7HHLH	LLLL	2.7HHLH
240-247	LLLL	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	LLLL
248-255	4.0HHLH	LLLL	LLLL	4.0HHLH	LLLL	LLLL	4.0HHLH	HLLL

Notice that a number has been entered into the table next to each word that enables a pulse. This number represents the pulse spacing from the previous pulse. The number is determined by the code that generated the previous pulse, the number of intervening words, and the code (PULSENC0-2) of the current word. Consider ROM addresses 8-11 as an example. The word at address 8 generates a pulse in the last bit position of an eight-bit frame specified by the LLL code. The next two ROM words, addresses 9 and 10, are 1.3333 microsecond delay terms. The word at address 11 also generates a pulse, and the code is also LLL. With the same code, the pulse

spacing is eight bit times (1.3333 microseconds) plus the intervening delays (2.66667 microseconds) for a total pulse spacing of 4.0 microseconds.

Notice that pulse spacings of 2, 2.3, 2.7, 3, 3.1, 3.7, and 4 microseconds are required to represent the various data, clock, and missing clock conditions of the simulated input pattern. The simulator hardware is capable of 166.6667 nanosecond resolution (one clock period at 6 MHz).

The data pattern (in hex form) simulated is:

5555	
5555	
5555	
5505	Phase change at 05
550D	Address mark (unassigned)
FF00	
5151	
FF25	
5252	
5353	
AA11	CRC word

Figure 2-94 shows the output pulse spacing for the simulated data segment from the phase change to the first byte after the address mark. Note that the address mark data pattern (0D, with missing clock in third byte) is one that is recognized by the address mark and phase correction circuitry, but does not correspond to an MFM data address mark or ID address mark.

2.8.3 Read Data Simulator Timing

Timing for the read data simulator is illustrated on two diagrams. The first diagram shows the special case of simulator start-up, and the second diagram shows a typical segment of the operating cycle.

2.8.3.1 Start-up Timing. Figure 2-95 shows the start-up cycle for the read data simulator. Data separator read test (DSRDTST) is initially low, holding the address clock counter, the address sequence counter, and the shift register reset. The simulator is enabled when the TMS 9900 CRU bus sets the DSRDTST output of the data separator control register. The SN74LS163 counter starts on the next positive-going edge of SIXMHZ. The shift register starts shifting out the zeros from the prior reset. Logic ones are shifted into the shift register serial input. After eight shifts the register contents are FF.

After the first eight shifts, the address sequence counter LSB (SIMADDR0) changes state to select address 1. Address selection precedes loading of the decoded address by eight bit times (1.3333 microseconds). The initial word (address 0) is not used on start-up, because the first load pulse occurs in 16 clock times. All other load pulses occur at eight clock-time intervals.

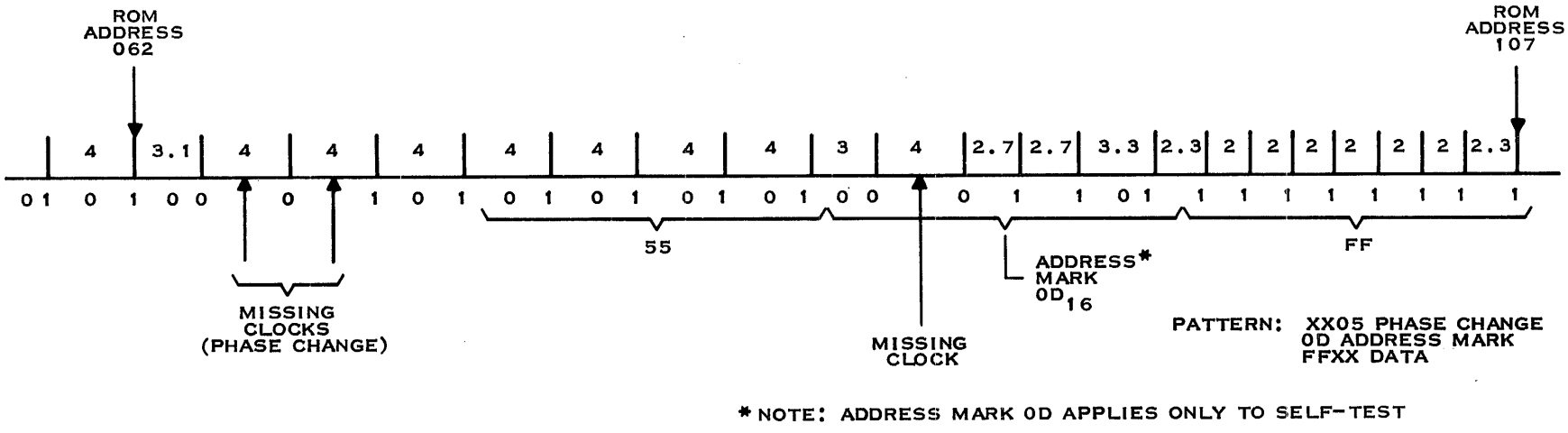


Figure 2-94. Simulated Phase Change and Address Mark Spacing

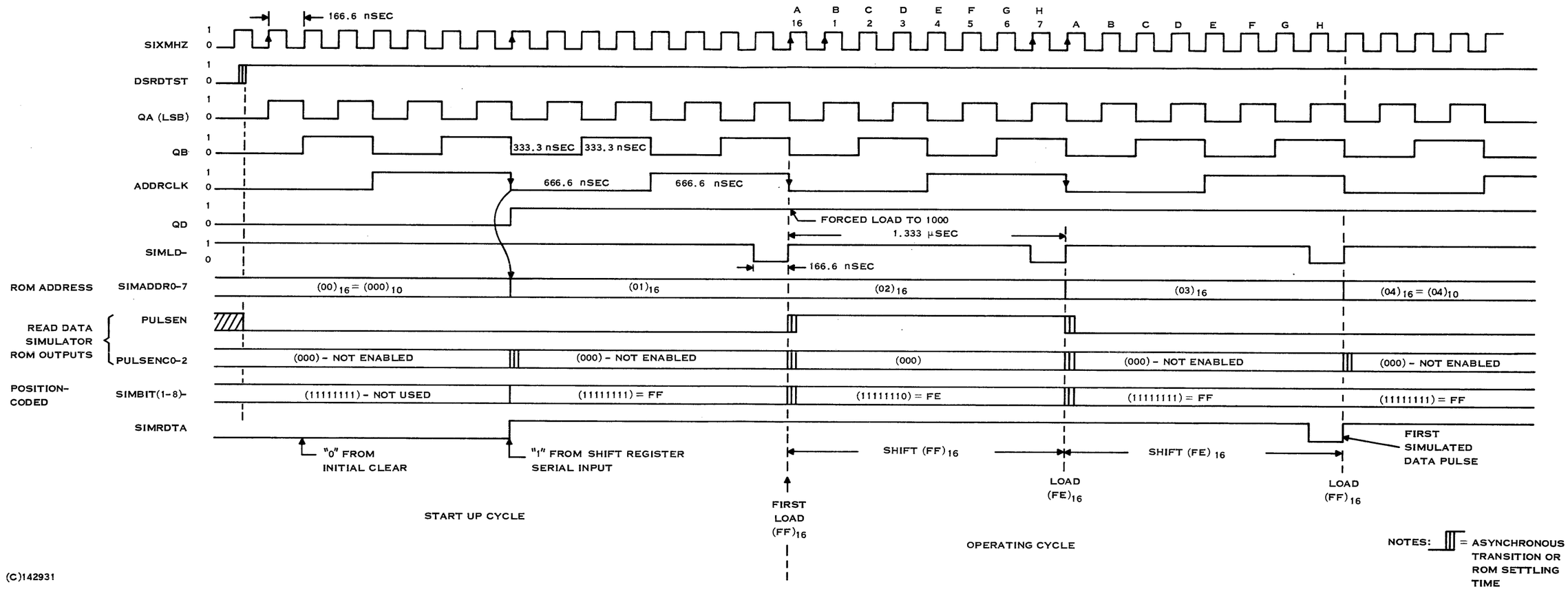


Figure 2-95. Read Data Simulator Startup Timing

2261885-9701

On start-up, the SN74LS163 address clock counter counts to 15 before issuing the ripple carry output. The ripple carry output is inverted (as SIMLD-) and is used as a counter preload and shift register load command. The counter and the shift register are both synchronous-loading devices that accept parallel inputs on the positve-going edge of SIXMHZ. A hardwired 1000 input to the counter preloads it to eight. For every cycle after start-up, the counter follows a 1000, 1001, ..., 1111, 1000 sequence. This eight-bit sequence corresponds to the eight-bit (one byte) capacity of the shift register.

During the first eight bit times of the starting sequence, the shift register ouput is all zeros (from the reset). During the second eight bit times, the output is all ones (from the hardwired serial shift input). The simulator load (SIMLD-) command goes active low as the last bit appears at the shift register output. The decoder output, SIMBIT(1-8)-, is clocked in on the next SIXMHZ shift pulse. As shown in the ROM listing and the timing diagram, the ROM word at address 1 does not enable the decoder, so a default code of FF is loaded on the first SIMLD- pulse. The address sequencer steps to the next ROM address on the clock edge that loads the decoded ROM output. The shift register load is complete before the counters, ROM, and decoder can respond to the clock edge.

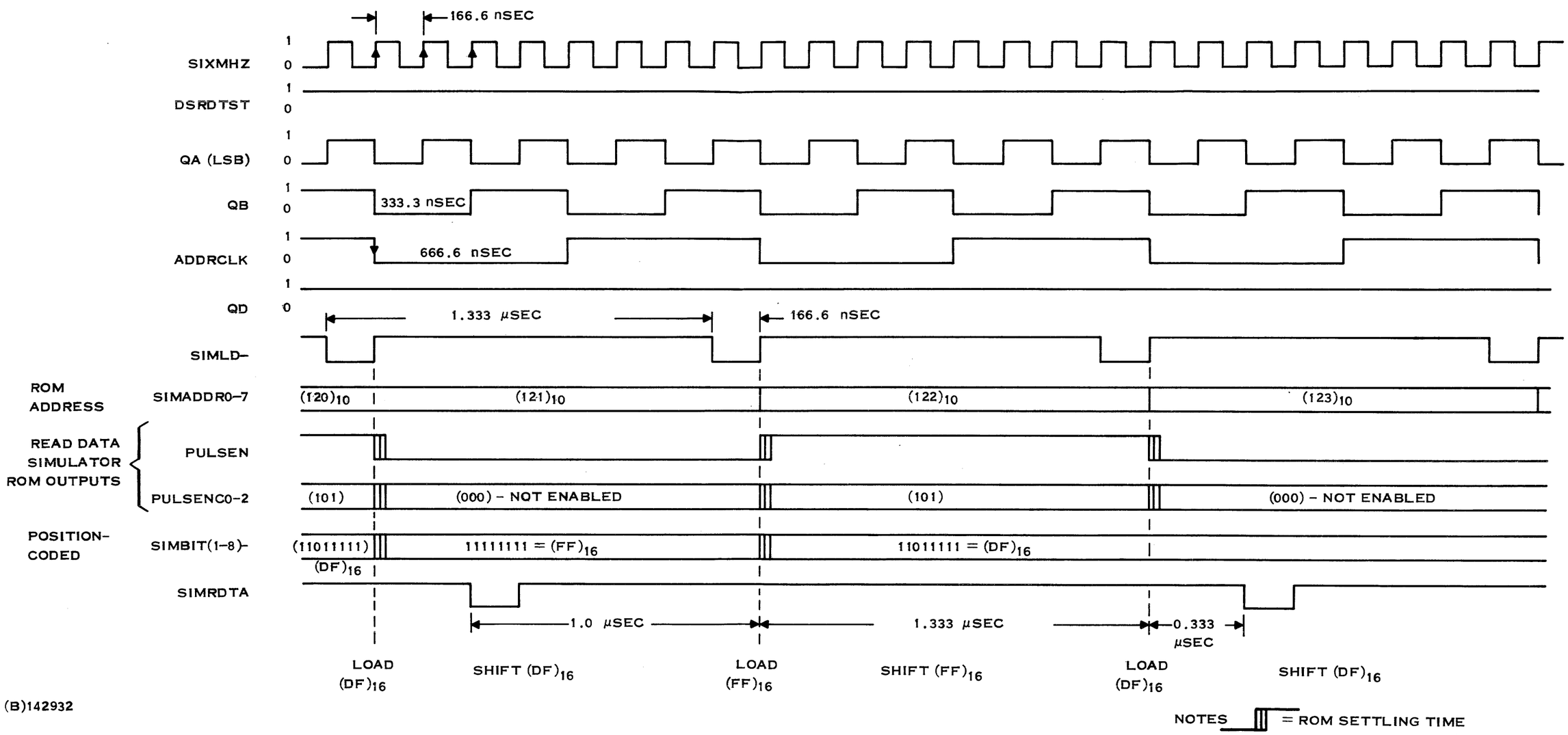
This first SIMLD- pulse finishes the startup cycle. All subsequent simulator cycles are eight-bit cycles with shift register outputs determined by the ROM contents. The address clock counter preloads to 1000 once every eight clock cycles, so the counter MSB (QD) does not return to zero until DSRDTST low disables the simulator.

2.8.3.2 Operating Cycle. Figure 2-96 shows the operations required to generate two pulses with 2.6667 microsecond timing.

This operation starts with the ROM at address 120 (decimal). The pulse enable (PULSEN) is high and the ROM code is HLH (binary 5), thus the SN74LS138 decoder output is 11011111. The decoder output is loaded into the shift register on the positive-going SIXMHZ edge at the end of the simulator load pulse (SIMLD-). The decoder MSB is immediately available on the QH (SIMRDTA) shift register output (at that point). The zero appears at the output for the period between the third and fourth clock edges after load, and the remaining five bits are ones. Note that the ROM code (binary 101 = decimal 5) corresponds to the third bit position in the eight-bit frame. A ROM code of 111 would correspond to the first bit position in the frame (01111111). A ROM code of 000 would correspond to the eighth (last) position in the frame (11111110). The rule to use is that the position number (1-8) of the zero bit is 1000-XXX, where XXX is the ROM output code.

As the last bit of this word is shifted out, the next decoder output is loaded. Note that the ROM output MSB is low for the word at address 121_{10}; therefore, the all ones decoder default is loaded. When this word is shifted, it gives a 1.3333 microsecond delay.

The next ROM word is fetched and decoded as the delay word shifts out of the shift register. The word at address 122_{10} enables the decoder, and the code is five. On the next SIMLD- pulse, 11011111 is loaded into the shift register and the SIMRDTA output pulse goes low two clock times (333.333 nanoseconds later). Adding up 1.0 microseconds from the leading edge of the first pulse to the end of the cycle, a 1.333 microsecond delay cycle, and 0.3333 microseconds to the leading edge of the second pulse gives a pulse spacing of 2.6667 microseconds.



(B)142932

Figure 2-96. Read Data Simulator Timing — 2.7 Microsecond Spacing

The SIMRDTA pulses are inverted to SIMRDTA- for input to the inverting RDAT gate. The read data synchronizer logic catches the positive-going edge of each RDAT pulse (trailing edge of low SIMRDTA pulse) to produce an active-high synchronized data pulse (SYNCDPULSE). Thus, although SIMRDTA appears inverted with respect to actual input data, normal operation of the read data synchronizer logic properly catches the simulated data pulses. Refer to Figure 2-97 for a comparison of received and simulated data waveforms (idealized).

2.9 INTERNATIONAL CHASSIS POWER SUPPLY (2261695)

This description applies to the unbuffered power supply/interface board supplied in an international chassis marked "FD1000A" on the rear panel. The description is based on the logic drawing, 2265018, and the power supply interconnection drawing, 2267251 (Appendix F).

Skip to paragraph 2.10 for a description of the buffered version of the power supply/interface board, 2269977, found in an FD1000B chassis.

The power supply/interface board distributes 115-volt ac power from the power transformer secondary to the chassis cooling fan and to the disk drive spindle motors. The power supply/interface board also accepts low voltage ac outputs from the power transformer secondary and develops filtered, regulated dc voltages for the drive electronics boards.

The interface circuits include an intrachassis parallel bus that provides signal input/output connections for one or two drive units. Three connectors are provided for controller/international chassis communication: a 50-pin local bus connector, a 25-pin 771/DS990 Model 1 connector, and a 15-pin remote bus connector. The 50-pin local bus connector provides a straight connection from the intrachassis bus to the controller local (daisy-chain) bus. The 771/DS990 Model 1 connection (not described in this manual) is isolated from the intrachassis bus through line drivers and line receivers.

The remote bus is the standard communications path between the TILINE flexible disk controller and the FD1000A international chassis (Figure 2-2). Shielded, twisted-pair cables and differential line drivers/receivers provide sufficient noise immunity to allow cable lengths of up to 100 meters.

2.9.1 Interface Logic

The drive input/output signals are described with the TFDC local bus port in Table 2-35. The fundamental purpose of the interface logic is to transfer these signals between the TFDC drive interface and the drives on the intrachassis bus. This purpose remains unchanged whether the interface is providing copper connections only (local bus), line drivers/receivers (771), or status and control signal multiplexing/demultiplexing (remote bus).

The controller remote port logic and the international chassis interface logic play complementary roles in the remote bus signal exchange. The controller multiplexes drive control signals and a synchronization gap for transmission to the international chassis. The power supply/interface logic demultiplexes the control signal input and latches the resulting outputs into a control register. The control register outputs (after the transmission and multiplexing/demultiplexing delays) duplicate the parallel control signals in the controller.

The remote interface logic of the power supply/interface board also multiplexes the drive status outputs onto a single status line for transmission to the TFDC. The TFDC remote interface logic

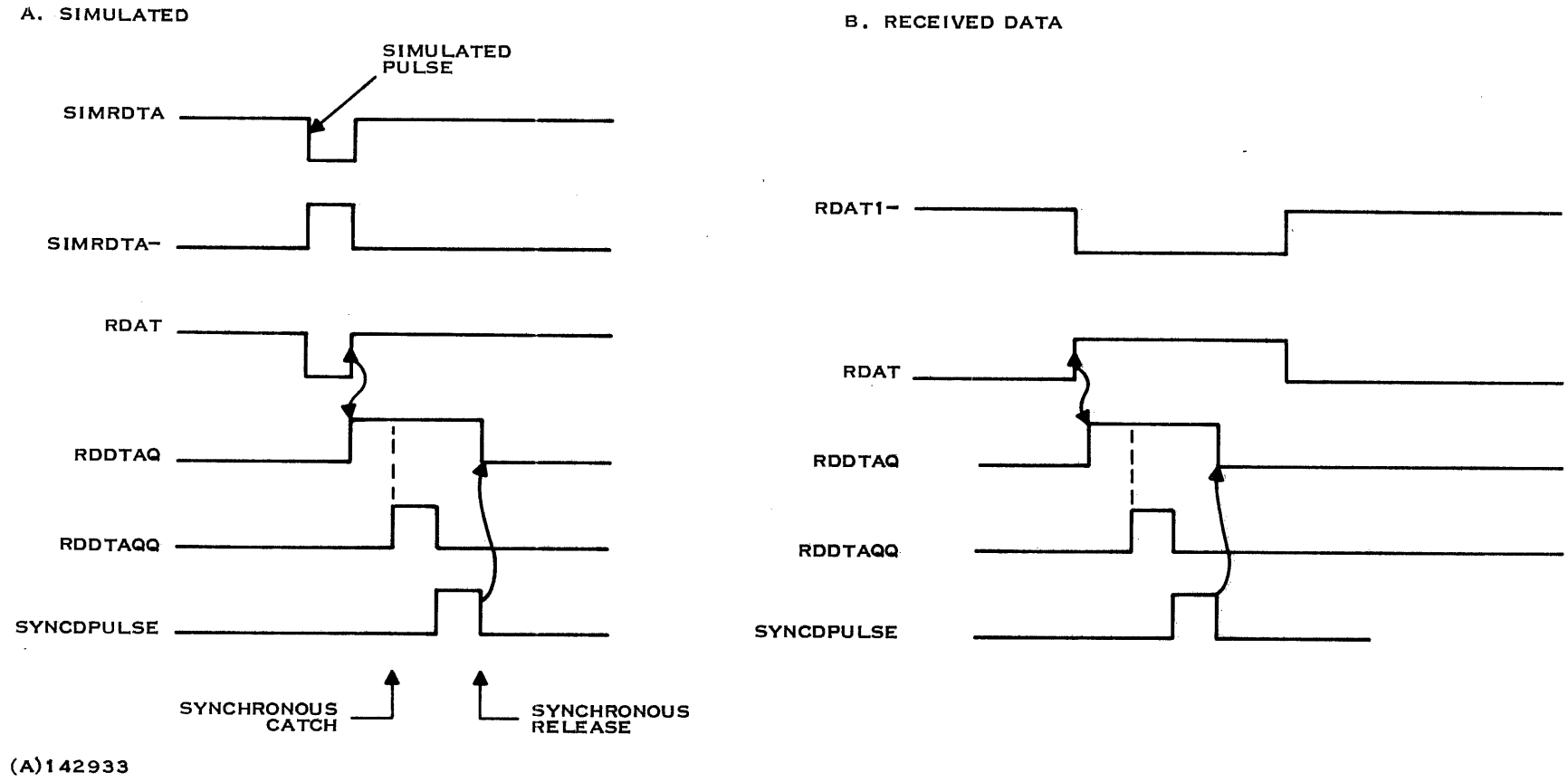


Figure 2-97. Comparison of Simulated and Received Data

must demultiplex the status signals. After the transmission and multiplexing/demultiplexing delays, the resulting status signals in the TFDC duplicate the status signals on the intrachassis bus.

The remote interface signals are described with the TFDC remote bus ports in Table 2-36. The signals that are unique to the remote bus are the multiplexer/demultiplexer clock (YCLK1, YCLK1-), the multiplexed control signal (YCNTL, YCNTL1-), and the multiplexed status signal (YSTAT1, YSTAT1-). The other remote bus signals are simply differential-pair versions of the corresponding local bus signals.

The signal connectors on the power supply/interface board are:

- J1 50-pin flat connector, local bus
- J2 15-pin D-type connector, remote bus
- J3 25-pin D-type connector, 771/DS990 Model 1
- J4,J5 50-pin flat connectors intrachassis bus (to drives)

Refer to sheet 3 of logic drawing 2265018. Control outputs to the drives are shown at the right side of the sheet. The control outputs from the 771 bus, the local bus, and the remote interface logic are connected in parallel to the intrachassis bus. Notice that the control outputs from the remote interface logic are supplied by SN7438 open-collector gates. Pull-up resistors on the drive electronics boards supply the +5-volt termination required by the open-collector outputs.

The remote bus inputs and terminators are shown at the lower left of sheet 3. The remote interface logic is enabled by a jumper built into the D-type connector at the end of the remote bus cable. When the remote bus cable is installed, the jumper grounds the active-low (RTENAB-) signal line. RTENAB- is inverted to become the active-high remote enable signal, RTENAB. RTENAB high enables the control register, the clock regeneration circuitry, and the SN75115 write gate line receiver.

A reset input from the power supply regulators (RESET-) holds the remote enable low and disables all the remote interface control and write data drivers. During a power up cycle, the reset remains active for at least 10 milliseconds after the +5-volt and +24-volt power supplies reach 90 percent of full voltage. During a power failure or a power down cycle, the reset signal goes active when either supply falls below 90 percent of full voltage.

2.9.1.1 Clock Regeneration and Control Demultiplexing. Refer to the timing diagram, Figure 2-98 and sheet 3 of the logic diagram for this description. The encoded control signal and the multiplexer/demultiplexer clock signals are converted from differential-pair line voltages to active-high TTL levels (ENCNTL, ECLK) by two sections of an SN75115 line receiver device. The clock signal and the encoded control signal experience identical transmission delays, so skew between the clock and control signals is negligible.

The ECNTL signal is encoded into seven periods of two microseconds each, and one period of four microseconds. An overall control signal frame (complete update of the control register contents) requires 18 microseconds. Control signal changes correspond to positive-going transitions of the ECLK signal.

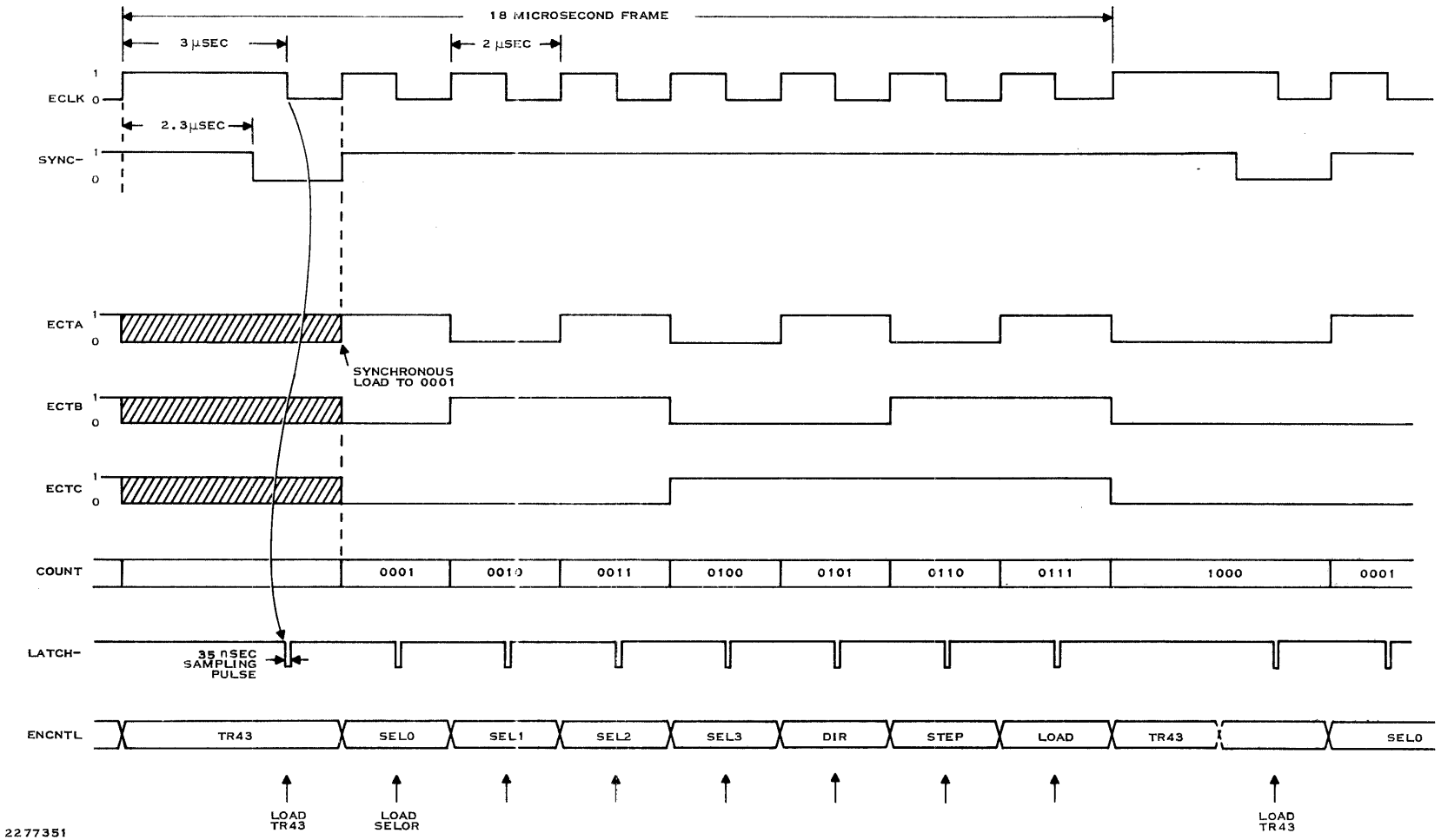


Figure 2-98. Remote Clock Regeneration and Control Decoding

ECLK is a 500-kilohertz clock waveform with one suppressed clock period in every eight periods. The resulting waveform is shown at the top of the timing diagram. The one wide clock out of every eight clock pulses is a synchronization pulse that marks the beginning of a control signal frame.

An SN74LS123 dual retriggerable one-shot provides loading pulses (SYNC-) for the clock counter and latch enable pulses (LATCH-) for the control register. These functions are considered separately. The SYNC- one-shot is triggered (low-to-high) by a positive-going edge of ECLK-. The RC components of this one-shot section are selected to provide a three-microsecond (approximate) delay before SYNC- drops low. However, if another positive-going clock edge occurs before the delay expires, the one-shot retriggers. Retriggering the one-shot restarts the delay period. As long as the interval between retriggering pulses is less than the RC delay, the one-shot does not time out (SYNC- remains high).

At the start of each frame, there is a four-microsecond interval between positive-going edges of ECLK. The three-microsecond RC delay expires, and SYNC- goes low until the next positive-going ECLK pulse.

The clock counter is an SN74LS163 synchronous binary counter. The low SYNC- pulse loads a hardwired 0001 into the clock counter on the first positive-going ECLK edge. This is the same edge that retriggers the SYNC- one-shot. The counter increments on each ECLK pulse, following a 0001, 0010,...0111, 1000 sequence. Notice that the counter MSB output is not used.

The ECTA, ECTB, and ECTC counter outputs serve as address inputs to the control register, an SN74259 eight-bit addressable latch. ECTA is the LSB of the address. A count of 001 directs the ENCNTL signal to the input of the SEL0R latch. The latch contents are not actually changed until the active-low LATCH- pulse enables the latch.

On each positive-going ECLK pulse, the count changes and the ECNTL input signal is steered to the next latch. Latch 0 is the last latch selected, but the clock is not issued until the next frame.

The LATCH- signal that enables the control register latches is produced by the second section of the SN74LS123 one-shot. The very small RC components produce a 35-nanosecond, active-low pulse on each negative-going ECLK edge.

The active-high outputs of the control register are inverted by open-collector NAND gates and are connected to the intrachassis bus. Note that the parallel connections on the intrachassis bus make it possible to monitor the remote interface outputs at the local bus connector. Note that either a RESET- signal or absence of the remote enable forces all the gate outputs high.

The DIRR signal is inverted (TESTL-) and looped back to the TFDC via the encoded status line. Toggling this signal at the controller output and reading it back at the drive status inputs provides a check on the presence and the integrity of the remote international chassis.

2.9.1.2 Status Signal Encoding. Refer to sheet 2 of the logic drawing. Status signals from the drive electronics boards come into the power supply/interface board via J4 or J5, depending on which drive (if any) is selected. The status signals are connected directly to the local bus connector and are routed to the 771/DS990 Model 1 port via open-collector drivers. The status signals are also wired to the inputs of an SN74LS151 8:1 multiplexer.

Multiplexer steering is controlled by the regenerated clock count, ECTA, ECTB, and ECTC as described in the previous paragraph. The result is a single serial status output that is divided into an 18-microsecond frame, with seven 2-microsecond subframes and one 4-microsecond subframe (ground). The order of outputs is:

- Logic 0 (remote chassis on status)
- RDYE-
- INDEXE-
- TROE-
- WPE-
- TESTL-
- DCE-
- TSE-

This is the same multiplexing scheme that is used in the TFDC to produce the multiplexed control signal described in the previous paragraphs.

The encoded multiplexer output, ESTAT-, is transmitted to the TFDC by one section of an SN75113 line driver. The drive ready (RDYE-) signal serves as a strobe to enable the output status and read data line drivers.

2.9.2 Power Distribution

Refer to the power supply interconnection drawing, 2267251, for this description of ac and dc power distribution within the international chassis. Notice that the power supply/interface board is connected to the secondary of the chassis power transformer. A voltage selection plug in the transformer primary chooses primary taps for operation at 100, 120, 220, or 240 volts ac.

The power supply/interface board provides 115-volt ac distribution through four connectors, P7-P10, that are wired in parallel. One of them is connected to the 115-volt ac output of the power transformer, and the others are used to power the exhaust fan and the spindle motors of the drive units. The selection of connectors is based on convenience in cable routing. Pin assignments for the high-voltage ac connectors are:

Voltage	I/O Connector P7-P10
115 Vac	Pin 1-Pin 3
Chassis Ground	Pin 2

Low voltage ac power from the power transformer is supplied through P6. This low voltage ac power is rectified to supply the dc outputs. The ac inputs are:

Voltage	Input Connector P6
7.5 Vac	Pin 1–Pin 2
26.5 Vac	Pin 3–Pin 4
15.0 Vac	Pin 5–Pin 6

The dc power output pin connections are shown in Table 2-38. Convenient probe-tip test points are provided for each dc output voltage.

All dc voltages produced by the power supply are referenced to a logic ground that is independent of chassis ground. Logic ground may be connected to chassis ground by an E6-E7 jumper as shown on 2265018, sheet 3. The grounding jumper may be changed to combat noise pickup or ground loop problems.

Table 2-38. International Power Supply Output Connections

Voltage	Current (max)	Test Point	Output Connector P11, P12
+ 5 Vdc ±2.5%	4.0 A	TP2	Pin 5
+24 Vdc ±5%	2.2 A	TP4	Pin 1
−12 Vdc ±6%	0.25 A*	TP1	Pin 4
Logic ground		TP3	Pins 2, 3, 6

Note:

* The −12 Vdc output is not required by the Qume DT/8 drive.

2.9.2.1 Power Supply Circuitry. Refer to sheet 4 of drawing 2265018, the dc power supply circuit schematic. The power supply circuits may be divided into groups according to function. These groups of circuits are:

- +5-volt regulated supply and crowbar
- +24-volt regulated supply
- −12-volt regulated supply
- +12-volt internal supply
- TTL Reset

SN72723/uA723C Voltage Regulators. The +5-volt and +24-volt regulators are based on IC voltage regulators combined with series-pass transistors. The SN72723/uA723C voltage regulators each include a built-in reference voltage source and reference amplifier, an error amplifier, a current limiter, a 150-milliampere series-pass output transistor, and a 6.2-volt zener diode. Figure 2-99 is a simplified block diagram of the IC voltage regulator. The regulators are packaged as standard 14-pin DIP circuits.

+5-Volt Regulated Supply. The circuits for the +5-volt supply are shown in the upper left quadrant of 2265018, sheet 4. This supply features a highly regulated adjustable output with current limiting and an overvoltage crowbar.

The 7.5-volt ac input is rectified by a full-wave bridge rectifier (CR10) rated at 400 peak inverse volts (PIV) and 10 amperes of forward current. This bridge rectifier shares a heat sink with CR9 and CR11, the other two bridge rectifiers. The output of CR10 is capacitively-filtered (C15) and fused at 5 amperes by an on-board fuse.

The dc voltage passes through Q10, the series-pass regulator transistor, and through R59, the 0.1 ohm current sensing resistor. The final regulated dc output is available at the junction of R59 and C19, the output filter capacitor. Series-pass transistor Q10, although shown as a conventional NPN transistor, is actually an integrated Darlington-pair transistor, with beta (forward current gain) of approximately 1000. Q10 is a TIP640 NPN transistor, and Q9 (in the 24-volt regulator) is a TIP645 PNP Darlington. These series-pass transistors generate large amounts of heat in normal operation, and are mounted on massive finned heat sinks.

Series-pass transistor Q10 is controlled by the SN72723/uA723C voltage regulator IC (U14) and associated circuits. The voltage regulator is powered (Vcc+ and Vc) by +12 volts from the zener-regulated internal power supply.

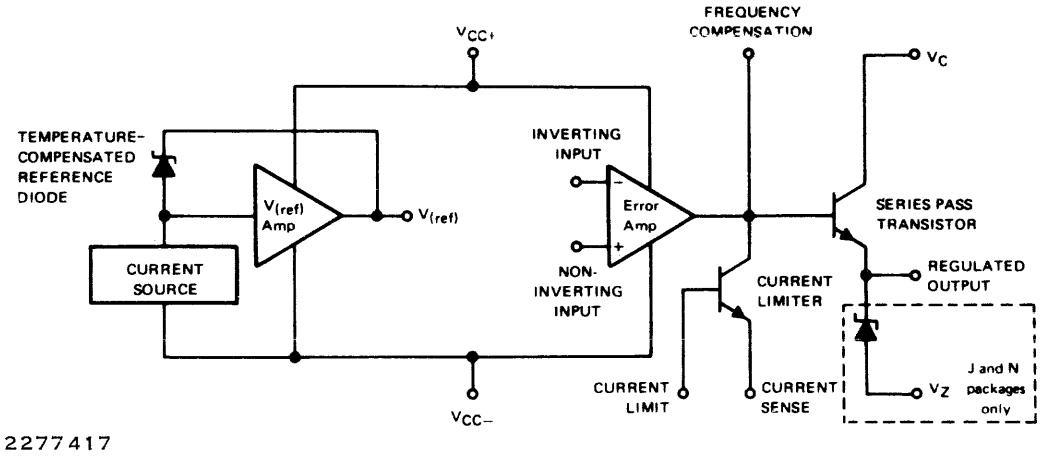


Figure 2-99. SN72723/uA723C Voltage Regulator Block Diagram

Voltage regulator operation is based upon sensing the final output voltage, comparing this voltage to a stable, accurate reference voltage, and developing an error signal that corrects the regulated output voltage by controlling the resistance of a series-pass element. The current requirements placed on the power supply far exceed the power dissipation capability of the IC regulator so Q10, the high power Darlington-pair transistor, is used as the series-pass element. The IC regulator output controls base drive to Q10, varying the resistance in series with the power supply output.

The +5-volt output is sensed through R62, which is connected from the output side of current-sensing resistor R59 to the inverting input (II) of the regulator IC. The noninverting input (N-II) is connected to an adjustable voltage divider network (R73, R74, R72) on the regulator reference voltage output. The reference voltage output (VREF) is stable but the voltage varies from device to device due to unavoidable production variations. Manufacturer's specifications call for a nominal 7.15 volt reference with upper and lower limits of 6.8 and 7.5 volts, respectively.

A difference between the sensed output voltage and the 5-volt output at the slider of R74 represents an error in the regulated output voltage. The voltage difference drives the regulator circuit to correct the regulated output and drive the error voltage to zero. In practice, R74 is adjusted to produce 5 volts at the power supply output (test point TP2) under load. This method of adjustment automatically compensates for any voltage offset in the error amplifier. The adjustable reference voltage at the R74 wiper is also used as the basic reference voltage by the 24-volt regulator circuit. A precision voltage divider at the sense point divides the +24-volt output down for comparison to the reference voltage. A voltage follower provides isolation between the circuits.

A 6.2-volt zener diode, CR6, provides an upper limit of 6.2 volts on the noninverting input to the regulator. The 6.2-volt limit provides over-voltage protection when power is initially applied to the system. The zener also provides protection against gross misadjustment of the reference voltage divider, R74.

The SN72723/uA723C regulator controls series-pass transistor Q10 by supplying base drive through R71. The resistor limits the base drive to protect the base-emitter junction of Q10 from burnout. Capacitors C31 and C25 bypass high-frequency spikes and compensate the output amplifier frequency response.

The voltage regulator IC includes circuitry that reduces the output drive to protect against excessive load current. When driven into conduction by an external input (CL), a shunt transistor reduces drive to the output transistor. Reducing drive to the IC output transistor reduces the base drive to Q10, increasing the series resistance and dropping the output voltage.

Resistor R59 serves as the output current sensing resistor. The voltage at the input side of R59 is tapped off by a voltage divider consisting of R60 and R61. The divider output feeds the noninverting input of an LM324 amplifier section. The voltage at the output side of R59 is tapped off by another voltage divider, R46 and R47. The divided output voltage is applied to the inverting input of the LM324 amplifier (pin 2). As output current increases, the voltage dropped across R59 increases. At a current threshold determined by the divider networks (4.5 amperes), the amplifier output starts limiting the output current. Short circuit output current is limited to 1.0 amperes.

A base-emitter short is one of the more common failure modes of any transistor series regulator. This type of failure may be catastrophic to the logic powered by the supply, as the output voltage rises to the unregulated level at the rectifier output. The circuitry at the lower right corner of sheet 4 is a crowbar circuit that provides over-voltage protection. During normal operation, triac Q2 is

cutoff and there is no significant current drain on the + 5-volt output. At output voltages less than the zener voltage of CR4 (5.6 volts), the base to emitter voltage is zero, and Q4 is cutoff. As the power supply output voltage increases beyond 5.6 volts, Q4 conducts, raising the gate voltage of triac Q2 to the firing level. Capacitor C30 bypasses noise spikes on the gate input of Q2 and determines the speed of the crowbar response.

When Q2 fires, the power supply output is shorted to ground through R59 and Q2. Q2 is rated at 12 amperes continuous current, 100 amperes surge current, and is capable of withstanding any current the remainder of the power supply can provide.

If the 5-volt regulators are operable, the 5-volt supply will go into foldback current limiting. This condition may be cleared by turning off the power supply, removing the fault, and turning on the power supply. However, if the regulator is not working (typically due to emitter-collector short in series-pass transistor Q10) the supply will not foldback, and fuse F1 will blow.

CAUTION

Replacing fuse F1 with an incorrectly rated fuse can result in burnout of bridge rectifier CR10, series-pass transistor Q10, and/or current-sensing resistor R59 when the crowbar is activated. Use only the specified replacement fuse, part number 0537399-12 (Littlefuse 276005).

+ 24-Volt Regulated Supply. The + 24-volt power supply is also based upon an SN72723/uA723C integrated circuit regulator device controlling a high power, series-pass transistor. The series-pass element for this supply is Q9, a PNP Darlington-pair transistor. Base drive for Q9 is provided by Q3, a 2N2222A NPN general-purpose transistor.

The + 24-volt regulator uses the same basic reference voltage as the + 5-volt regulator circuit. The reference output of the SN7273/uA723C regulator in the 5-volt circuit (U14) is applied to a voltage divider consisting of potentiometer R74 and resistors R73 and R72. The voltage at the wiper arm of R74 is the reference voltage for both power supplies. Zener diode CR6 limits this reference to + 6.2 volts, providing protection against gross misadjustment of R74.

The adjustable reference voltage is applied to one input of the LM324 quad operational amplifier. This section of the LM324 (pins 5, 6, 7) is connected as a unity-gain voltage follower. One output of the voltage follower is applied through R70 to the noninverting input of the 24-volt regulator.

The 24-volt output voltage is sensed by a voltage divider (R55, R56) at the output of the series-pass transistor. The divider output is applied to the inverting input of the regulator. The regulator output (from the internal zener diode) drives the 2N2222A regulator driver to control the conduction of Q10 and to keep the voltage at the R55-R56 tap equal to the reference voltage.

The + 24-volt regulator includes foldback current limiting, although the circuitry differs from the + 5-volt current limiter. The + 24-volt power supply has an onboard return that is separate from the + 5-volt and − 12-volt returns. This return is identified by an open triangle symbol or by a + V2RTN signature. A 0.1 ohm, 5-watt resistor (R57) connects the 24-volt return to logic ground, which is the only return available to the external load circuits. R57 provides current sensing because any current supplied to an external 24-volt load must return through logic ground and through R57 to the

rectifier bridge (+ V2RTN). The + V2RTN point is at zero volts (with respect to logic ground) only if there is no load current drawn from the 24-volt supply. Any current drawn from the + 24-volt output pulls + V2RTN more negative than logic ground.

The current-limiting circuit consists of an LM324 amplifier stage (U15, pins 12, 13, 14) with associated components and a shunt transistor in the regulator IC. When conducting, the shunt transistor reduces base drive to the output transistor, as shown in the regulator block diagram, Figure 2-99. The CL input of the regulator is the base lead of the current-limiting transistor, CS is the emitter lead, and FC is the collector lead.

The inverting and noninverting inputs of the LM324 amplifier stage are connected to voltage dividers that establish an operating point. They are only indirectly involved in the limiting output current. The ground reference for the output stages of the LM324 is connected to + V2RTN, while the emitter of the current-limiting transistor is referenced to logic ground. Increasing current from the 24-volt supply pulls the emitter more positive with respect to the base input and increases conduction. Increased conduction reduces the regulator output and increases the resistance of the series-pass transistor, Q9. Increasing output current beyond the current-limiting threshold (4.5 amperes) reduces the output voltage (foldback limiting).

0C26 and R54 form a high-frequency bypass from the shunt transistor collector (FC) to an ac low impedance point. C23 and R42 form another high-frequency bypass. These circuits prevent load transients from causing the current limiter to oscillate. There is no crowbar provided for the + 24-volt supply. Diode CR8 (rated at one ampere) protects series-pass transistor Q9 from any externally applied positive voltage and from the power-down discharge of capacitor C18.

– 12-Volt Supply. The negative 12-volt supply is regulated by a single uA79M12 three terminal voltage regulator device. This device has an input connection to the rectifier bridge, a regulated output connection, and a ground (logic ground) connection. Diode CR1 protects the regulator from the effects of an externally supplied negative voltage. Maximum recommended output current for the regulator device is 250 milliamperes.

+ 12-Volt Internal Power Supply. The internal power supply for regulator operation is tapped from the output of the + 24-volt bridge rectifier. This supply consists of dropping resistor R58, 12-volt zener diode CR5, and high-frequency filter capacitor C24. Low-frequency filtering is provided by C16 at the + 24-volt bridge rectifier output.

The internal supply provides + 12-volt dc power for the LM324 quad operational amplifier (U15) and for the SN72723/uA723C regulators in the + 5-volt and + 24-volt supplies.

NOTE

An open circuit in dropping resistor R58 or a short in CR5 will shut down all the regulators and amplifiers, leaving only the – 12-volt supply operable.

Reset Circuit. The logic reset circuitry consists of one section of an LM324 amplifier (U15, pins 9, 10, 8), an RC network, and five discrete transistors (Q5Q8, Q11). The purpose of this circuitry is to hold the digital interface logic reset for a short interval after power-up, and to reset the interface logic if the 5-volt or 24-volt power supply fails. The final output of the reset logic is a TTL-compatible, active-low RESET- signal.

The inverting input of the amplifier is supplied by the reference voltage follower (U15 pin 7). The noninverting input is supplied by the + 24-volt regulated output through a voltage-divider network, R35, R36, and R41. The voltage at the node of R35, R36, and CR3 is 7.72 volts if CR3 is not conducting. CR3 limits the node voltage to the diode forward voltage drop plus the unregulated input voltage to Q10. This unregulated voltage is approximately 7.5 volts, and the diode forward voltage drop is 0.2 volts; therefore, the effect of the CR3 connection is negligible as long as the 5-volt supply is working.

The R36-R41 voltage divider places 0.667 of the R35-R36 node voltage at the amplifier noninverting input. With the R35-R36 node voltage at 7.72 volts, the amplifier pin 10 input is 5.15 volts. The other input is the 5-volt reference. The amplified voltage difference charges C22. Under steady-state conditions, the voltage at U15-8 is positive, Q7 is turned on, and the amplifier output current (except that necessary to maintain C22 charged) returns to ground through R45, the base-emitter junction of Q7, and R68. The RESET- output is inactive (high).

When power is interrupted or turned off, C22 discharges into the output stage of the LM324 amplifier. Diode CR2 bypasses charging resistor R40 to speed the discharge. With C22 essentially at ground potential, Q7 cuts off and the RESET- output of Q11 goes active (low). With all power cutoff, RESET- remains low.

When power is restored, C22 is initially discharged and Q7 is off. When power is restored, the LM324 amplifier section starts charging C22. The rate of voltage increase is determined by the amplifier current capabilities and by the RC time constant of R40-C22. After a few milliseconds of charging time, Q7 turns on and the RESET- output is released (returns high). With Q7 saturated, most of the charging current is diverted through R45, Q7, and R68.

Assume that the power supply is at steady-state and that the five-volt fuse (F1) blows, either as a result of crowbar action or some other overload. The 7.5-volt level that was holding diode CR3 balanced, drops to zero. CR3 becomes forward-biased and pulls the R35-R36 junction toward zero volts. With the amplifier inputs unbalanced, C22 discharges into the amplifier output stage. RESET- goes low as Q7 is cut off (and also because the 5-volt supply to Q11 failed). When power is restored, C22 is in the discharged state, and must be charged (through R40) before the RESET- output can return high. This hold-off action assures that the voltage outputs have stabilized before the digital logic is enabled.

If the 24-volt supply fails, the same node (R35-R36) drops to zero volts for lack of a supply, the amplifier unbalances, C22 discharges, and RESET- goes active (low). Because the 5-volt power is still available, RESET- goes low as the result of cutting off Q7, rather than as a result of losing the digital voltage output. When 24-volt power is restored, the discharged capacitor holds RESET- active until the charging voltage reaches the switching threshold of Q7.

2.10 BUFFERED INTERNATIONAL CHASSIS POWER SUPPLY (2269977)

This description applies to the buffered version of the power supply/interface board installed in an international chassis marked "FD1000B" on the chassis rear panel.

The description of the buffered power supply/interface board is based on the logic drawing, 2269979, and the power supply interconnection drawing, 2267251 (Appendix F).

The power supply/interface board distributes 115-volt ac power from the power transformer secondary to the chassis cooling fan and to the disk drive spindle motors. The power supply/interface board also accepts low voltage ac outputs from the power transformer secondary and develops filtered, regulated dc voltages for the drive electronics boards.

The interface circuits include an intrachassis bus that provides signal input/output connections for one or two drive units. Three connectors are provided for controller/international chassis communication: a 50-pin local bus connector, a 25-pin 771/DS990 Model 1 connector, and a 15-pin remote bus connector.

The 50-pin connector connects via a flat cable to the controller local (daisy-chain) bus. The local bus is used only in FD800 systems.

The 771/DS990 Model 1 connector connects to a 771 intelligent terminal or DS990 Model 1 via a ribbon cable. The CRU-based controller for 771/DS990 Model 1 is not described in this manual.

The remote bus is the standard communications path between the TILINE flexible disk controller and the FD1000B international chassis (figure 2-2). This bus uses a multiplexing/demultiplexing scheme to transmit status and control signals on a smaller number of wires. Shielded, twisted-pair cables and differential line drivers/receivers provide sufficient noise immunity to allow cable lengths of up to 100 meters.

2.10.1 Interface Logic

The drive input/output signals are described with the TFDC local bus port in Table 2-35. The fundamental purpose of the interface logic is to transfer these signals between the TFDC drive interface and the drives on the intrachassis bus. This purpose remains unchanged whether the interface is providing buffering and copper connections only (local bus, 771/DS990 Model 1) or status and control signal multiplexing/demultiplexing (remote bus). Line termination and drive selection options are also provided on this version of the power supply/interface board. Line terminator U11 is always installed for use with the remote bus.

The controller remote port logic and the international chassis interface logic play complementary roles in the remote bus signal exchange. The controller multiplexes drive control signals and a synchronization gap for transmission to the international chassis. The power supply/interface logic demultiplexes the control signal input and latches the resulting outputs into a control register. The control register outputs (after the transmission and multiplexing/demultiplexing delays) duplicate the parallel control signals in the controller.

The remote interface logic of the power supply/interface board also multiplexes the drive status outputs onto a single status line for transmission to the TFDC. The TFDC remote interface logic must demultiplex the status signals. After the transmission and multiplexing/demultiplexing delays, the resulting status signals in the TFDC duplicate the status signals on the intrachassis bus.

The remote interface signals are described with the TFDC remote bus ports in table 2-36. The signals that are unique to the remote bus are the multiplexer/demultiplexer clock (YCLK1, YCLK1-), the multiplexed control signal (YCNTL, YCNTL1-), and the multiplexed status signal (YSTAT1, YSTAT1-). The other remote bus signals are simply differential-pair versions of the corresponding local bus signals.

The signal connectors on the power supply/interface board are;

- J1 50-pin flat connector, local bus
- J2 15-pin D-type connector, remote bus
- J3 25-pin D-type connector, 771/DS990 Model 1
- J4,J5 50-pin flat connectors intrachassis bus (to drives)

Refer to sheet 2 of logic drawing 2269979. Control outputs to the drives are shown at the right side of the sheet. The control outputs from the 771 bus, the local bus, and the remote interface logic are connected in parallel at the SN7438 driver outputs.

Pull-up resistors in the line terminator IC (U14) supply the +5-volt termination required by the open-collector SN7438 devices and the input lines. A bank of MC14584 complementary metal-oxide-semiconductor (CMOS) receivers and SN74S240 drivers buffer the outputs to the intrachassis bus. These buffers provide an improved noise margin for the 771/DS990 Model 1 and local bus input signals.

Terminator U11 is always installed for use with the TFDC and the remote bus. However, when this chassis and power supply are used in FD800, 771, or DS990 Model 1 systems, U11 is only installed in the last chassis on the bus. This is because these systems use a daisy-chain signal cable.

Series resistor pack U10, diodes CR8-CR11 and resistors R42-R45 prevent interaction problems between chassis on a daisy-chain bus. Assume that terminator U11 is installed in chassis 2 and not installed in chassis 1. (Ignore the protective networks for the time being). There are no difficulties as long as power is applied to both chassis. However, if power is turned off in chassis 2 (with the terminator) the lines are no longer properly terminated to Vcc. Noise spikes could occur on the lines, possibly leading to noise on the diskette. Also, the MC14584 CMOS receivers include protective diodes that could supply current into the unpowered terminator of chassis 1. The result would be heating in the MC14584 input stages.

A bank of 1 kilohm series resistors (U10) limits the back current supplied by the MC14584 input stages. This prevents any device overheating. Head load (LOAD) and write enable (WRTENA-) are critical with respect to noise transients and spikes. A secondary terminator consisting of a 2.7 kilohm resistor to Vcc, a diode, and 6.2 kilohm resistor to ground establishes an input level in the absence of a powered terminator. The diodes (CR8-CR11) prevent interaction between the Vcc supplies of the two chassis.

The drive select jumpers on the drive electronics boards are always positioned to DS1 and DS2 respectively, connecting the DRIVE1- or DRIVE2- signal input. Final drive select assigments are determined by jumpers on the buffered power supply/interface board. Drive select jumpers in a primary chassis are connected from E1 to E2 and E4 to E5. Drive select jumpers in a secondary chassis are connected from E2 to E3 and E5 to E6.

The remote bus inputs and terminators are shown at the lower left of sheet 2. The remote interface logic is enabled by a jumper built into the D-type connector at the end of the remote bus cable. When the remote bus cable is installed, the jumper grounds the active-low (RTENAB-) signal to logic ground. RTENAB- is inverted to become the active-high remote enable signal, RTENAB. RTENAB high enables the control register, the clock regeneration circuitry, and the SN75115 write gate line receiver.

A reset input from the power supply regulators (RESET-) holds the remote enable low and disables all the remote interface control and write data drivers. During a power up cycle, the reset remains active for at least 10 milliseconds after the + 5-volt and + 24-volt power supplies reach 90 percent of full voltage. During a power failure or a power down cycle, the reset signal goes active when either supply falls below 90 percent of full voltage.

2.10.1.1 Clock Regeneration and Control Demultiplexing. Refer to the timing diagram, Figure 2-98 and sheet 2 of the logic diagram for this description. The encoded control signal and the multiplexer/demultiplexer clock signals are converted from differential-pair line voltages to active-high TTL levels (ENCNTL, ECLK) by two sections of an SN75115 line receiver device. The clock signal and the encoded control signal experience identical transmission delays, so skew between the clock and control signals is negligible.

The ECNTL signal is encoded into seven periods of two microseconds each, and one period of four microseconds. An overall control signal frame (complete update of the control register contents) requires 18 microseconds. Control signal changes correspond to positive-going transitions of the ECLK signal.

ECLK is a 500-kilohertz clock waveform with one suppressed clock period in every eight periods. The resulting waveform is shown at the top of the timing diagram. The one wide clock out of every eight clock pulses is a synchronization pulse that marks the beginning of a control signal frame.

An SN74LS123 dual retriggerable one-shot provides loading pulses (SYNC-) for the clock counter and latch enable pulses (LATCH-) for the control register. These functions are considered separately. The SYNC- one-shot is triggered (low-to-high) by a positive-going edge of ECLK-. The RC components of this one-shot section are selected to provide a three-microsecond (approximate) delay before SYNC- drops low. However, if another positive-going clock edge occurs before the delay expires, the one-shot retriggers. Retriggering the one-shot restarts the delay period. As long as the interval between retriggering pulses is less than the RC delay, the one-shot does not time out (SYNC- remains high).

At the start of each frame, there is a four-microsecond interval between positive-going edges of ECLK. The three-microsecond RC delay expires, and SYNC- goes low until the next positive-going ECLK pulse.

The clock counter is an SN74LS163 synchronous binary counter. The low SYNC- pulse loads a hardwired 0001 into the clock counter on the first positive-going ECLK edge. This is the same edge that retriggers the SYNC- one-shot. The counter increments on each ECLK pulse, following a 0001, 0010,...0111, 1000 sequence. Notice that the counter MSB output is not used.

The ECTA, ECTB, and ECTC counter outputs serve as address inputs to the control register, an SN74259 eight-bit addressable latch. ECTA is the LSB of the address. A count of 001 directs the ENCNTL signal to the input of the SEL0R latch. The latch contents are not actually changed until the active-low LATCH- pulse enables the latch.

On each positive-going ECLK pulse, the count changes and the ECNTL input signal is steered to the next latch. Latch 0 is the last latch selected, but the clock is not issued until the next frame.

The LATCH- signal that enables the control register latches is produced by the second section of the SN74LS123 one-shot. The very small RC components produce a 35-nanosecond, active-low pulse on each negative-going ECLK edge.

The active-high outputs of the control register are inverted by SN7438 open-collector NAND gates. Note that the parallel connection of the input buses make it possible to monitor the remote interface outputs at the local bus connector. Note that either a RESET- signal or absence of the remote enable forces all the gate outputs high.

The DIRR signal is inverted (TESTL-) and looped back to the TFDC via the encoded status line. Toggling this signal at the controller output and reading it back at the drive status inputs provides a check on the presence and the integrity of the remote international chassis.

2.10.1.2 Status Signal Encoding. Refer to sheet 3 of the logic drawing. Status signals from the drive electronics boards come into the power supply/interface board via J4 or J5, depending on which drive (if any) is selected. The status signals are connected directly to the local bus connector and are routed to the 771/DS990 Model 1 port via open-collector drivers. The status signals are also wired to the inputs of an SN74LS151 8:1 multiplexer.

Multiplexer steering is controlled by the regenerated clock count, ECTA, ECTB, and ECTC as described in the previous paragraph. The result is a single serial status output that is divided into an 18-microsecond frame, with seven 2-microsecond subframes and one 4-microsecond subframe (ground). The order of outputs is:

- Logic 0 (remote chassis on status)
- RDYE-
- INDEXE-
- TROE-
- WPE-
- TESTL-
- DCE-
- TSE-

This is the same multiplexing scheme that is used in the TFDC to produce the multiplexed control signal described in the previous paragraphs.

The encoded multiplexer output, ESTAT-, is transmitted to the TFDC by one section of an SN75113 line driver. The drive ready (RDYE-) signal serves as a strobe to enable the output status and read data line drivers.

2.10.2 Power Distribution

Refer to the power supply interconnection drawing, 2267251, for this description of ac and dc power distribution within the international chassis. Notice that the power supply/interface board is connected to the secondary of the chassis power transformer. A voltage selection plug in the transformer primary chooses primary taps for operation at 100, 120, 220, or 240 volts ac.

The power supply/interface board provides 115-volt ac distribution through four connectors, P7-P10, that are wired in parallel. One of them is connected to the 115-volt ac output of the power transformer, and the others are used to power the exhaust fan and the spindle motors of the drive units. The selection of connectors is based on convenience in cable routing. Pin assignments for the high-voltage ac connectors are:

Voltage	I/O Connector P7-P10
115 Vac	Pin 1-Pin 3
Chassis Ground	Pin 2

Low voltage ac power from the power transformer is supplied through P6. This low voltage ac power is rectified to supply the dc outputs. The ac inputs are:

Voltage	Input Connector P6
7.5 Vac	Pin 1-Pin 2
26.5 Vac	Pin 3-Pin 4
15.0 Vac	Pin 5-Pin 6

The dc power output pin connections are shown in Table 2-39. Convenient probe-tip test points are provided for each dc output voltage.

All dc voltages produced by the power supply are referenced to a logic ground that is independent of chassis ground. Logic ground may be connected to chassis ground by an E7-E8 jumper as shown on 2269979, sheet 2. The grounding jumper may be changed to combat noise pickup or ground loop problems.

2.10.2.1 Power Supply Circuitry. Refer to sheet 4 of drawing 2269979, the dc power supply circuit schematic. The power supply circuits may be divided into groups according to function. These groups of circuits are:

- +5-volt regulated supply and crowbar
- +24-volt regulated supply
- −12-volt regulated supply
- +12-volt internal supply
- TTL Reset

Table 2-39. International Power Supply Output Connections

Voltage	Current (max)	Test Point	Connector P11, P12
+ 5 Vdc ±2.5%	4.0 A	TP2	Pin 5
+24 Vdc ±5%	2.2 A	TP4	Pin 1
−12 Vdc ±6%	0.25 A*	TP1	Pin 4
Logic ground		TP3	Pins 2, 3, 6

Note:

* The -12 Vdc output is not required by the Qume DT/8 drive.

SN72723/uA723C Voltage Regulators. The +5-volt and +24-volt regulators are based on IC voltage regulators combined with series-pass transistors. The SN72723/uA723C voltage regulators each include a built-in reference voltage source and reference amplifier, an error amplifier, a current limiter, a 150-milliampere series-pass output transistor, and a 6.2-volt zener diode. Figure 2-99 is a simplified block diagram of the IC voltage regulator. The regulators are packaged as standard 14-pin DIP circuits.

+5-Volt Regulated Supply. The circuits for the +5-volt supply are shown in the upper left quadrant of 2269979, sheet 4. This supply features a highly-regulated adjustable output with current limiting and an overvoltage crowbar.

The 7.5-volt ac input is rectified by a full-wave bridge rectifier (CR4) rated at 400 peak inverse volts (PIV) and 10 amperes of forward current. This bridge rectifier shares a heat sink with CR5. The output of CR4 is capacitively-filtered (C12) and fused at 5 amperes by on-board fuse F1.

The dc voltage passes through Q1, the series-pass regulator transistor, and through R8, the 0.1 ohm current sensing resistor. The final regulated dc output is available at the junction of R8 and C4, the output filter capacitor. Bypass diode CR1 protects Q1 from the effects of externally applied test voltages and from the power-down discharge of capacitor C4.

Transistor Q1, although shown as a conventional NPN transistor, is actually an integrated Darlington-pair transistor, with beta (forward current gain) of approximately 1000. Q1 is a TIP640 NPN transistor, and Q5 (in the 24-volt regulator) is a TIP645 PNP Darlington. These series-pass transistors generate large amounts of heat in normal operation, and are mounted on massive finned heat sinks.

Series-pass transistor Q1 is controlled by the SN72723/uA723C voltage regulator IC (U24) and associated circuits. The voltage regulator is powered (Vcc+ and Vc) by +12 volts from the zener-regulated internal power supply (VR1).

Voltage regulator operation is based upon sensing the final output voltage, comparing this voltage to a stable, accurate reference voltage, and developing an error signal that corrects the regulated output voltage by controlling the resistance of a series-pass element. The current requirements

placed on the power supply far exceed the power dissipation capability of the IC regulator so Q1, the high power Darlington-pair transistor, is used as the series-pass element. The IC regulator output controls base drive to Q1, varying the resistance in series with the power supply output.

The +5-volt output is sensed through R5, which is connected from the output side of current-sensing resistor R8 to the inverting input (INV) of the regulator IC. Capacitor C3 bypasses noise spikes and compensates the regulator frequency response. The noninverting input (NON-INV) is connected to an adjustable voltage divider network (R2, R3, R4) on the regulator reference voltage output.

The reference voltage output (VREF) is stable but the voltage varies from device to device due to unavoidable production variations. Manufacturer's specifications call for a nominal 7.15-volt reference with upper and lower limits of 6.8 and 7.5 volts, respectively.

A difference between the sensed output voltage and the 5-volt output at the slider of R3 represents an error in the regulated output voltage. The voltage difference drives the regulator circuit to correct the regulated output and drive the error voltage to zero. In practice, R3 is adjusted to produce 5 volts at the power supply output (test point TP2) under load. This method of adjustment automatically compensates for any voltage offset in the error amplifier.

The voltage regulator IC includes circuitry that reduces the output drive to protect against excessive load current. When driven into conduction by an external input (CL), a shunt transistor reduces drive to the output transistor. Reducing drive to the IC output transistor reduces the base drive to Q1, increasing the series resistance and dropping the output voltage.

The voltage at the input side of current-sensing resistor R8 is tapped off and resitively summed with the reference voltage (VREF) by precision resistors R6 and R7. The summed voltage is applied to the current limit (CL) input of the regulator device. This is the base input of the internal shunt regulator transistor. The emitter of that transistor (CS) is connected to the output side of R8.

As output current increases, the voltage dropped across R8 increases, and the sum voltage at CL increases. At a current threshold determined by the resistor network (4.5 amperes), current limiting action begins. Output current under a full short-circuit condition is limited to 1.0 amperes (foldback limiting).

A base-emitter short is one of the more common failure modes of any transistor series regulator. This type of failure may be catastrophic to the logic powered by the supply, as the output voltage rises to the unregulated level at the rectifier output. The circuitry at the upper right of sheet 4 is a crowbar circuit that provides overvoltage protection. During normal operation, triac Q3 is cutoff and there is no significant current drain on the +5-volt output. At output voltages less than the zener voltage of VR2 (5.6 volts), the base to emitter voltage is zero, and Q2 is cutoff. As the power supply output voltage increases beyond 5.6 volts, Q2 conducts, raising the gate voltage of triac Q3 to the firing level. Capacitor C5 bypasses noise spikes on the gate input of Q3 and determines the speed of the crowbar response.

When Q3 fires, the power supply output is shorted to ground through R8 and Q3. Q3 is rated at 12 amperes continuous current, 100 amperes surge current, and is capable of withstanding any current the remainder of the power supply can provide.

If the 5-volt regulator is working, the overcurrent will lead to foldback limiting, and no damage will result. This condition can be cleared by cycling the ac input power off and on. If the regulators are not functioning (typically an emitter-collector short in series-pass transistor Q1), the overload will blow fuse F1.

CAUTION

Replacing fuse F1 with an incorrectly rated fuse can result in burnout of bridge rectifier CR4, series-pass transistor Q1, and/or current-sensing resistor R8 when the crowbar is activated. Use only the specified replacement fuse, part number 0537399-12 (Littlefuse 276005).

+24-Volt Regulated Supply. Input power for the +24-volt power supply is provided by a 26.5-volt winding on the chassis power transformer. Full-wave bridge rectifier CR5 and filter capacitor C13 provide an unregulated dc input to the regulator circuits. Overload protection is provided by 5-ampere fuse F2. Fuses F2 and F1 are identical.

CAUTION

Use only the specified replacement fuse, part number 0537399-12 (Littlefuse 276005).

The +24-volt power supply is based upon an SN72723/uA723C integrated circuit regulator device controlling a high power, series-pass transistor. The series-pass element for this supply is Q5, a PNP Darlington-pair transistor. Base drive for Q5 is provided by Q6, a 2N2222A general-purpose NPN transistor.

The +24-volt regulator output is based upon the adjustment of the +5-volt power supply. The output of current-sensing resistor R8 (in the +5-volt supply) is applied through resistor R28 to the non-inverting input of regulator U22. This connection eliminates the need for separate adjustment of the +5-volt and +24-volt supplies. Note that a failure in the +5-volt supply may shut down the +24-volt supply.

The nominal +24-volt output at the collector of series regulator Q5 appears across precision voltage divider R23, R24. Divider values are selected to develop 4.97 volts across R24 for 24.00 volts across the divider. R24 is connected to the inverting input of the SN72723/uA723C regulator. Regulator output VZ (from the internal zener diode) drives the 2N2222A regulator driver to control the conduction of Q5. Regulator action attempts to keep the voltage at the R23-R24 tap equal to the 5-volt reference tapped from the +5-volt supply.

The +24-volt regulator includes foldback current limiting, although the circuitry differs from the +5-volt current limiter. The +24-volt power supply has an onboard return that is separate from the +5-volt and −12-volt returns. This return is identified by a +V2RTN signature. A 0.5 ohm compound resistor (R31 and R32 connected in parallel) connects the 24-volt return to logic ground,

which is the only return available to the external load circuits. R31/32 provides current sensing because any current supplied to an external 24-volt load must return through logic ground and the resistor pair to the rectifier bridge.

The +V2RTN point is at zero volts (with respect to logic ground) only if there is no load current drawn from the 24-volt supply. Any current drawn from the +24-volt output pulls logic ground more positive than +V2RTN.

The current-limiting circuit in the regulator IC is a shunt transistor, as shown in the regulator internal block diagram, Figure 2-99. The current limit (CL) input of the regulator (base lead of the shunt transistor) is connected directly to logic ground. Precision voltage divider R29, R30 is connected from the +24-volt output to bridge return +V2RTN. The divider establishes a bias point for the shunt transistor emitter, CS.

Increasing current from the 24-volt supply pulls the base input more positive with respect to the emitter. Once the base voltage reaches a threshold value (determined by the divider R29, R30) the shunt transistor starts conducting. Conduction through the shunt reduces the regulator output and increases the resistance of the series-pass transistor, Q5. Increasing output current beyond the current-limiting threshold (4.5 amperes) reduces the output voltage (foldback limiting).

C8 and R27 form a high-frequency bypass from the shunt transistor collector (FC) to an ac low impedance point. This circuit prevent load transients from causing the current limiter to oscillate.

There is no crowbar provided for the +24-volt supply. Diode CR2 (rated at one ampere) protects series-pass transistor Q5 from any externally applied positive voltage and from the power-off discharge of capacitor C7.

–12-Volt Supply. The negative 12-volt supply is regulated by a single uA79M12C three-terminal voltage regulator device. This device has an input connection to the rectifier bridge, a regulated output connection, and a ground (logic ground) connection. Diode CR3 protects the regulator from the effects of an externally supplied negative voltage. Maximum recommended output current for the regulator device is 250 milliamperes.

+12-Volt Internal Power Supply. The internal power supply for regulator operation is tapped from the output of the +24-volt bridge rectifier. This supply consists of dropping resistor R1, 12-volt zener diode VR1, and high-frequency filter capacitor C1. Low-frequency filtering is provided by C13 at the +24-volt bridge rectifier output.

The internal supply provides +12-volt dc power for the SN72723/uA723C regulators in the +5-volt and +24-volt supplies.

NOTE

An open circuit in fuse F2 or dropping resistor R58 or a short in VR1 will shut down the regulators, leaving only the –12-volt supply operable.

Reset Circuit. The logic reset circuitry consists of LM339 quad voltage comparator U23, 2N2905 transistor Q4, capacitor C6 and resistors R15 through R22. These circuits are in the lower right corner of logic sheet 4.

The purpose of this circuitry is to hold the digital interface logic reset for a short interval after power-up, and to reset the interface logic during power-down. The reset prevents the logic circuits from writing transient pulses on the diskette, and assures that the logic circuits do not start in random states. The output of the reset logic is a TTL-compatible, active-low RESET- signal at the collector of transistor Q4.

An LM339 device consists of four independent differential voltage comparators. A comparator acts like a very high-gain differential amplifier that is either cutoff or saturated if the differential input voltage exceeds a few millivolts.

The output stage of an LM339 comparator section is the collector of an NPN transistor. The open-collector output stage is cutoff (nonconducting) if the (+) input is more positive than the (−) input. The output stage is turned on when the (+) input is less positive than the (−) input. A pullup resistor to a positive source supplies collector current for the output stage. Note that the supply voltage for the LM339 device is +24 Vdc, not +5 Vdc.

The following paragraphs provide a detailed analysis of reset circuit operation during a power-up cycle.

When ac power is initially applied to the regulator bridges, the unregulated dc voltages at the filter capacitors (C12, C13) come up first. The RESET- output initially increases toward a positive level of a few millivolts, due to the voltage divider action of R13, R14, R15, and R22. RESET- and the collector of Q4 are prevented from going negative.

As the unregulated +24-volt level reaches the 12-volt level, the internal +12-volt power supply (VR1, R1) starts supplying regulated operating power to the SN72723/uA723C devices. The reference voltage (VREF) goes to the nominal 7.15-volt level and is divided across R2, R3, R4. The wiper of potentiometer R3 is the adjustable 5-volt reference for both the +24-volt and +5-volt regulated supplies. The RC time constant of R2, part of R3, and C2 delays the reference slightly, to provide a soft start for the regulated outputs.

As the +5-volt adjustable reference reaches the final level, both the +24-volt and +5-volt supplies go into regulation. The +24-volt output powers the LM339 comparators and starts charging capacitor C6 through R18. Voltage divider resistors R13 and R14 divide the unregulated source voltage from 7 volts to slightly more than 5 volts. The divider output must exceed the adjustable +5-volt reference level. Note that due to the time delays in reaching regulation and the RC delay (R2, R3, C2), the divider output stabilizes before the reference level.

Comparator input U23-7 (+) from the divider exceeds the +5-volt reference level, so the open-collector output (U23-1) is forced to cutoff. With no current flowing into the collector, C6 continues to charge.

Initial voltage at C6 started at zero, and is still well below the +5-volt reference level when the comparators start operating. Therefore, comparator input U23-5 (+) is less than the reference at U23-4 (−). The output stage is turned on, drawing saturation current through pullup resistor R19. Open-collector output U23-2 is essentially at ground level, differing by the drop across the 60-ohm (approximate) collector saturation resistance.

The last two comparator stages are connected in parallel. Comparator output U23-2 holds inputs U23-8, 10 (–) at ground, while inputs U23-9,10 are at the +5-volt reference level. Both comparator outputs are cutoff. The absence of significant current flowing through R20 (and R21) means that the base-emitter voltage of Q4 is approximately zero, and transistor Q4 is cutoff.

Notice that the emitter of Q4 is connected to the +5-volt supply and that the collector is connected to logic ground through 22-ohm collecter load resistor R22. This is a common-emitter circuit with collector-driven output.

With Q4 cutoff, the RESET- output goes to ground (logic zero), the collector supply voltage. The duration of the low RESET- is determined by the charging time of capacitor C6.

Recall that U23-1 is cutoff, and the comparator input at U23-5 (+) follows the voltage on C6. When the voltage at U23-5 exceeds the +5-volt reference level, U23-2 cuts off. With U23-2 no longer clamping to ground level, parallel inputs U23-8, 10 (–) rise toward +24 volts. Open-collector outputs U23-13, 14 go into saturation and conduct heavily.

Heavy conduction through R20, R21 pulls the base of transistor Q4 negative with respect to the emitter, turning Q4 on. With Q4 on, the +5-volt regulated supply output appears across R22. RESET- high enables the logic and line drivers in the signal interface circuitry.

Capacitor C6 continues to charge until it reaches the 24-volt supply level, and is maintained at +24 volts for the duration of powered operation. Recall that it is the charging characteristics of C6 through R18 that control the duration of the power-up reset. If C6 opens, no reset will occur. If C6 becomes leaky or shorts out, the reset may remain active (RESET- low) indefinitely.

The reset circuitry also issues a reset during normal power-down operations, again to prevent the writing of noise on the diskette. The following paragraphs describe the normal power-down sequence.

Before the shutdown begins, the following conditions exist:

1. The output of divider R13, R14 exceeds the adjustable +5-volt reference, so comparator output U23-1 is cutoff.

2. C6 is maintained at approximately 24 volts.

3. Comparator output U23-2 is also high, pulled up by R19.

4. Parallel comparator outputs U23-13, 14 are saturated, keeping transistor Q4 on.

5. RESET- (across R22) is a TTL logic one (high).

When the power supply shuts down, the unregulated voltages decay first. The regulator circuits are able to compensate for decreasing input voltages until the regulation limits are reached. Decay times are dependent upon external power supply loading.

The + 5-volt unregulated source voltage is nominally about 7 volts to allow a margin of operation for the series regulator. Divider R13, R14 divides the unregulated voltage down to slightly more than 5 volts at the comparator input, U23-7.

When the divider output decays to about 4.75 volts, comparator U23-1 switches to the conducting state. Capacitor C6 rapidly discharges (from + 24 volts) through the 60-ohm saturation resistance of the collector circuit.

When input U23-5 drops below the adjustable 5-volt reference level, U23-2 switches to the conducting state, pulling the node at R19, R17 to ground.

As inputs U23-8, 10 drop below the reference level, U23-13, 14 cutoff and are pulled to the level of the unregulated 5-volt source. The absence of significant current flow through R20 allows the base voltage of Q4 to rise. Q4 cuts off, and RESET- drops to approximately ground level (TTL logic zero). RESET- low forces the signal interface logic to a safe stage. As all voltages continue to decay, the logic goes to indeterminate states. By this time there is insufficient energy remaining to write a glitch on the diskette.

3

Maintenance

3.1 GENERAL

This section describes depot-level maintenance for the TILINE Flexible Disk Controller (2261690 or 2267295) and for the International Chassis Power Supply (2261695 or 2269977). Depot maintenance includes fault isolation to the component (IC, gate, transistor) level. This is in contrast to field maintenance, which includes fault isolation to the adjustment or board replacement level.

This section does not cover the flexible disk drive units. Disk drive maintenance to the adjustment level is described in *Model 990 Computer Model FD1000 Flexible Disk System Field Maintenance Manual*, part number 945419-9703. Depot-level troubleshooting and repair procedures for the drives are described in vendor manuals for the Qume* DataTrak 8.

Signal interface circuitry in the International Chassis Power Supply is tested with the disk controller. The regulated dc power supply circuits and the logic reset circuits are manually tested. Test descriptions are provided in paragraph 3.5 (2261695 assembly) and in paragraph 3.6 (2269977 assembly - FD1000B).

3.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the disk controller is based on dynamic testing with drive units in a "hot mockup" or other operating 990 computer system. Testing follows a progressive sequence in which each level of testing is more comprehensive than the previous level. Testing incorporates the normal and extended-mode capabilities of the on-board self-tests, the DOCS diagnostic software, and (if available) the AMPL test system.

3.3 DIAGNOSTIC TOOLS

The tools available for detection and isolation of faults include:

- Controller built-in self-tests and LED indicators. Normal-mode self-tests are performed as part of each power-up, I/O reset, or command initiation cycle. Extended-mode self-tests may be initiated through programmer panel commands or DOCS test verbs.
- Controller built-in command trace feature.

* Qume, DataTrak, and DataTrak 8 are trademarks or registered trademarks of Qume Corporation.

- Diagnostic software. The TILINE flexible disk system diagnostic test, DDFLOP, runs under control of the Diagnostic Operational Control System (DOCS) software. DOCS and DDFLOP provide:

  — A progressive isolating structure which starts with controller-only tests and proceeds in graduated steps to exhaustive tests of the controller, power supply/interface board, drive, and diskette.

  — Prompting displays to assist in setting up and running the tests.

  — Error message and controller status printouts.

  — General test verbs (under DOCS) and specific flexible disk system verbs (under DDFLOP) which allow interactive control of the testing process.

  — Single execution or looping on manually-entered command sequences or extended self-test sequences.

- AMPL test system (if available), featuring:

  — Emulation of on-board TMS 9900 microprocessor, with execution control through AMPL test language commands.

  — Substitution of emulator memory for 9900 control program ROM, using preloaded program.

  — Substitution of emulator memory for on-board scratchpad RAM.

  — Examination of on-board memory locations, including command trace locations.

  — Prestored or interactive test sequences.

3.3.1 Test Equipment

The special tools, test equipment, and documentation required for corrective maintenance are listed in Table 3-1.

Table 3-1. Special Test Equipment and Documentation

Item	Part Number
Equipment:	
DSDD Diskette	2261687-0001
SSSD Diskette	0945970-0001
Double-slot Extender Board	975170-0001
Dual-trace Oscilloscope	Tektronix 465 or equivalent

Table 3-1. Special Test Equipment and Documentation (Continued)

Item	Part Number
Equipment:	
Logic Analyzer	HP 1600A, Biomation 810D, or equivalent
990/10 Hot Mockup System	N/A
Double-Density Flexible Disk Assembly (international chassis)	
Rackmount, 2 Drives	2265020-0002
or	
Tabletop, 2 Drives	2265019-0002
Local Cable (for use with international chassis)	2267294-0001
or	
Local Cable (supplied with domestic chassis)	0945951-0001
Remote Cable (supplied with international chassis)	2261704-0001
AMPL System with 9900 Emulator	N/A
Loop-back Test Connector local	2264845-0001
Loop-back Test Connector remote	2264846-0001
Diagnostic Kit, 990 (includes DOCS and individual diagnostic test, DDFLOP)	0937782-0001 (DOCS cassette), or 0937782-0004 (DOCS DS31), or 0937782-0005 (DOCS DS25), or 0937782-0005 (DOCS DS50), or 0937782-0010 (DOCS DS10), or 0937782-0021 (DOCS DSDD)
Documentation:	
Model 990 Computer Diagnostics Handbook Volume 1	0945400-9701
Volume 3	0945400-9703
Assembly Drawing and List of Materials (LM) DS/DD I/F, 990 TILINE (multilayer version)	2261690, LM2261690
or	
Assembly Drawing and List of Materials DS/DD TILINE Floppy I/F (fineline version)	2267295, LM2267295

Table 3-1. Special Test Equipment and Documentation (Continued)

Item	Part Number
Documentation:	
Logic Diagram, DS/DD Floppy Disk Interface, 990 TILINE or Logic Diagram, DS/DD TILINE Floppy I/F (fineline)	2261692 (see appendixes) 2267297 (see appendixes)
9900 Control Program Listing	2250975-9901 (see appendixes)
ROM HI-LO Listings	(see Section 2)
Signature Dictionary	N/A (see appendixes)

3.3.2 Hot Mockup Configuration

The hot mockup system should be connected as shown in Figure 3-1.

CAUTION

System power must be removed, both at the 990 computer and at the international chassis, before removing or replacing any logic boards, connectors, cables, or jumpers.

The 990/10 computer should have at least 24 kilobytes of memory to accomodate DOCS and DDFLOP. A programmer panel is required for manual control and status checks, especially if a failure prevents loading DOCS and DDFLOP.

Either a Model 733 ASR Terminal or a Model 911 Video Display Terminal may be used for operator interaction with the DOCS and DDFLOP software.

Some means must be provided to load the DOCS and DDFLOP software into 990/10 memory. This may be an MDDS box, a 733 cassette transport, a hard disk system, or a flexible disk system. In any case, the 990/10 loader ROM must be compatible with the loading device and the test media.

A standby power supply is required in order to perform the power-down, power-up data integrity checks in the diagnostic test.

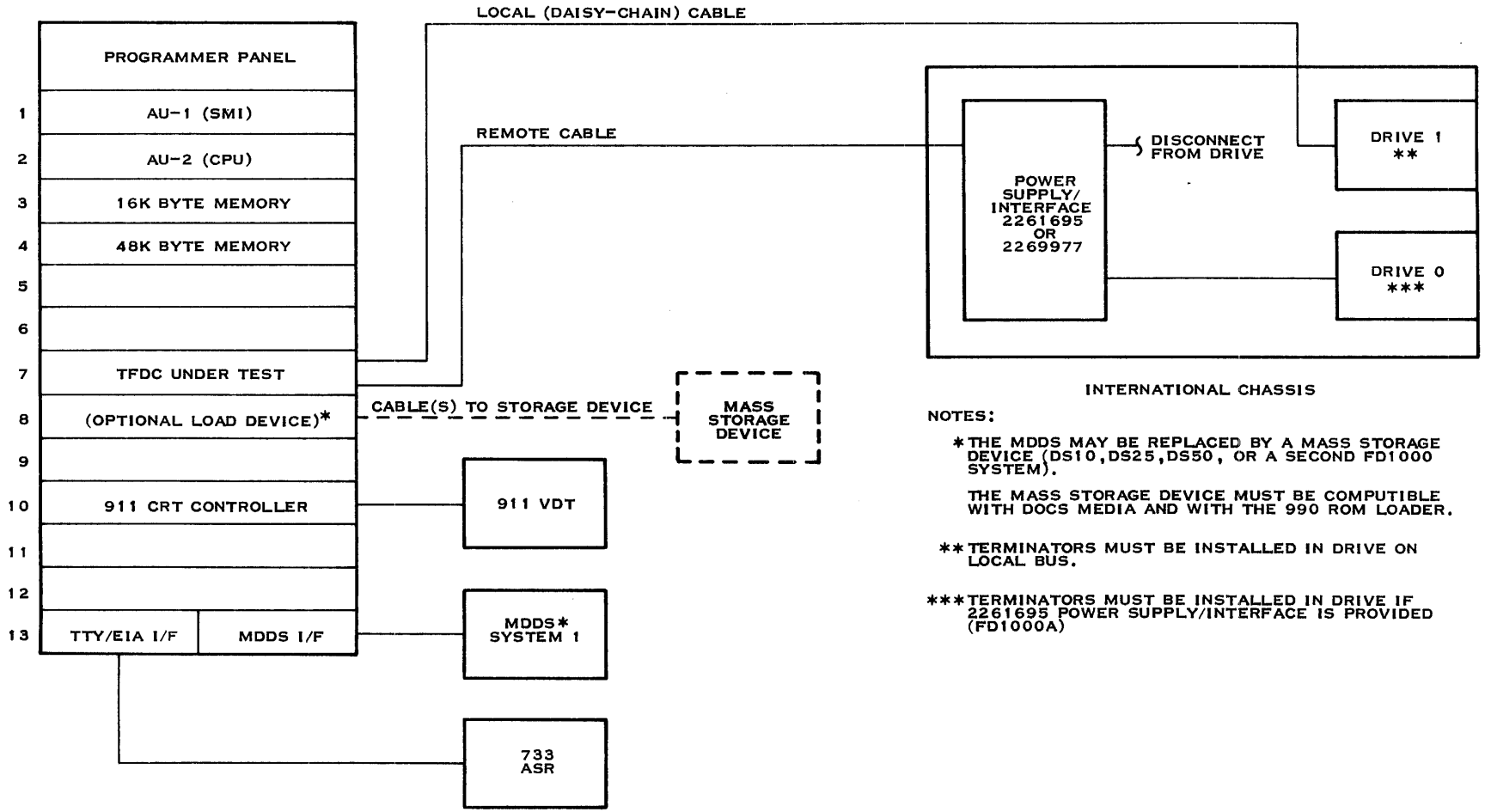


Figure 3-1. Hot Mockup System Configuration

The TFDC is a TILINE device, and must be installed in a chassis slot that has an open TILINE access granted (TLAG) jumper, with TLAG integrity from the controller slot to slot 1. The extender board makes the TFDC accessible for use of oscilloscope probes or an AMPL emulator/buffer.

The DDFLOP diagnostic test procedures require both a remote drive and a local drive. The least expensive way to get this combination is to use a dual-drive international chassis. Keep one drive connected to the remote logic through the intrachassis bus, and disconnect the pendant cable from the second drive, replacing the pendant cable with a local bus cable from the controller. Terminators must be installed in both drive units if the 2261695 power supply/interface board is used (FD1000A chassis). For the 2269977 power supply/interface board, the terminator at U11 is required, and an additional terminator must be installed in the drive that is connected to the local bus.

Install drive select jumpers to designate the remote drive as unit 1 and the local drive unit as unit 2.

3.4 CONTROLLER OPERATIONAL CHECKOUT AND FAULT DETECTION

The maintenance philosophy for the TFDC is based upon the controller operating in a 990/10 computer system. Therefore, all other items of the test station must be verified as being properly connected and operational prior to beginning test and fault isolation procedures.

NOTE

These procedures apply to both the multilayer and the fineline versions of the TFDC board. Each version has its own assembly drawing and component location scheme.

A reference to a logic drawing sheet number applies to both the multilayer board logic drawing (2261692) and the fineline board logic drawing (2267297). The logic drawings are virtually identical, except for component designators.

References to TFDC components common to both controllers specify first the location on the multilayer version, followed by the location on the fineline board. For example, UH090/UEB089 refers to the TMS 9901 PIA device designated UH090 on the multilayer version and UEB089 on the fineline version. The initial U is a device type identifier for integrated circuit networks. The letters H and EB are row identifiers. Notice that the multilayer board designators always start with two letters, while fineline designators start with three letters, including the device type identifier. Refer to Section 1 for board photographs and descriptions of the component designator schemes.

3.4.1 TFDC Preliminary Checkout

Prior to starting test and fault isolation procedures, perform the following steps:

CAUTION

Be sure all power is removed from system components before removing or installing any circuit boards or connectors.

1. Set the dual inline package (DIP) switches on the controller to the correct setting. The default address assumed by the DDFLOP diagnostic is CPU byte address F800 (all switches OFF). Switch setting details are shown in Figure 2-15.

2. Verify that the correct interrupt level and TILINE access granted connections are made at the selected chassis slot. The default interrupt level assumed by the DDFLOP diagnostic is $0D_{16}$.

NOTE

The TILINE address and interrupt level are specified to the diagnostic software when executing an initialize test (IT) verb. Non-default values may be specified by operator entries in response to IT prompts.

3. Using the extender board, install the controller board in the selected slot and install the remote and local bus cables.

4. Remove any data or system diskettes from the drive units. Replace with scratch diskettes.

5. Apply power to the drive chassis and allow a brief warm-up and stabilization period.

6. Observe the TFDC LED indicators and apply power to the 990 computer. Application of chassis power should cause the controller to reset and perform a power-up self-test. Continue to the next step, even if the test fails. Successful completion of the self-test is indicated if:

   a. CLOCK LED remains lighted. The clock indicator is controlled by TILINE master device active (MDACT), and remains lighted except when the TFDC is controlling a TILINE data transfer. An extinguished indicator means the controller is hung in a master cycle, or 5-volt dc power is off.

   b. INT LED remains extinguished.

   c. BUSY LED lights for approximately one second (as test executes) and then extinguishes. BUSY indicates that the controller is executing a command. The apparent brightness of the indicator is determined by the type and frequency of commands.

d. Red FAULT LED lights for approximately one second (as test executes) and then extinguishes. Self-test failure is indicated if the LED remains lighted. Self-test failure inhibits any command which involves the drive units (reading, writing, head positioning).

7. Observe the TFDC on-board LED indicators and depress HALT/SIE and RESET on the 990 programmer panel. This action resets the controller logic and initiates the controller self-test sequence. Successful completion of the self-test is indicated as in the previous step. Go on to the DDFLOP diagnostic if the self-test passes.

3.4.2 Controller Self-Test Failure

If the controller cannot pass power-up and reset self-tests, it will not perform any operation which involves the drive units. This means that parts 2-9 of the DDFLOP diagnostic will not execute. The options at this point are:

1. Preliminary manual troubleshooting.
2. Diagnostic testing with DDFLOP part 1.
3. Extended self-testing (not involving drives) under control of DDFLOP verbs.
4. Detailed manual troubleshooting with oscilloscope and 990 programmer panel status/control.
5. AMPL testing.

3.4.2.1 Physical Checks. If the controller fails the self-test on power-up, but passes after a programmer panel reset, the fault may be in the 990 chassis power supply, which develops the power-up reset command. Another possible reason for one or both tests to fail is improper seating of the controller connectors. Check seating as follows;

1. Remove ac power from the 990 computer and the drive chassis.
2. Remove and replace the controller board. Don't forget that the problem could be in TFDC-extender seating, extender-chassis seating, or a defective extender.
3. Apply ac power to the drives. Observe the TFDC LED indicators and apply power to the 990 chassis.

3.4.2.2 Clock and Reset Timing Checks. If reseating the boards does not help, use a dual-trace oscilloscope to check timing in the controller board as follows;

1. Check the 12-Mhz output of the TIM 9904/SN74LS362 four-phase clock oscillator at UH078/UEB074-16. Refer to Figure 3-2 for a typical waveform. If the 12-Mhz OSCOUT waveform is not present, the problem may be due to;

   a. 48-Mhz crystal

   b. LC tank circuit (LI080/LFD081, CI078/CFD079)

c. TIM 9904/SN74LS362 device (UH078/UEB074)

d. 12-volt power. As the 12-Mhz signal is the basis for the four-phase clock, microprocessor clock, and data separator clock (most modes), do not proceed until the OSCOUT waveform is verified or restored.

2. Use two single-pin fault isolation probes to check all four clock phases, two phases at a time, as listed below.

CAUTION

The four-phase timing signals provided by the MOS drivers are not short-circuit protected. Any probing into this circuitry must be done with care to avoid damaging the TIM 9904/SN74LS362 device.

Figure 3-3 shows the parameters to be checked, and Table 3-2 gives typical values and limits for these parameters. It is critical that no two successive clock phase pulses overlap. Figure 3-4 shows an acceptable relationship between successive phases. Use this figure as a reference and check the clock phases as follows;

a. Channel 1 probe to MP1 (RI082/RFD083) and channel 2 probe to MP2 (RI084/RFD085)

b. Channel 1 probe to MP2 (RI084/RFD085) and channel 2 probe to MP3 (RI086/RFD087)

c. Channel 1 probe to MP3 (RI086/RFD087) and channel 2 probe to MP4 (RI088/RFD089)

d. Channel 1 probe to MP4 (RI088/RFD089) and channel 2 probe to MP1 (RI088/RFD083)

3. Verify the presence of the TTL-compatible active-low microprocessor clock waveform CLK3A- by probing at UG090/UDF103-8.

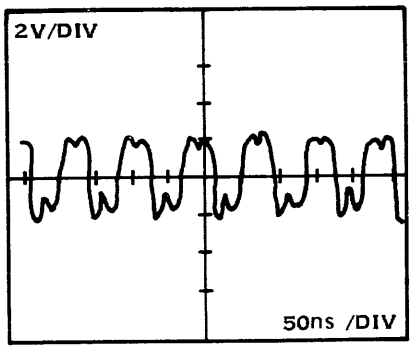


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Figure 3-2. TIM 9904/SN74LS362 OSCOUT (12 Mhz) Waveform

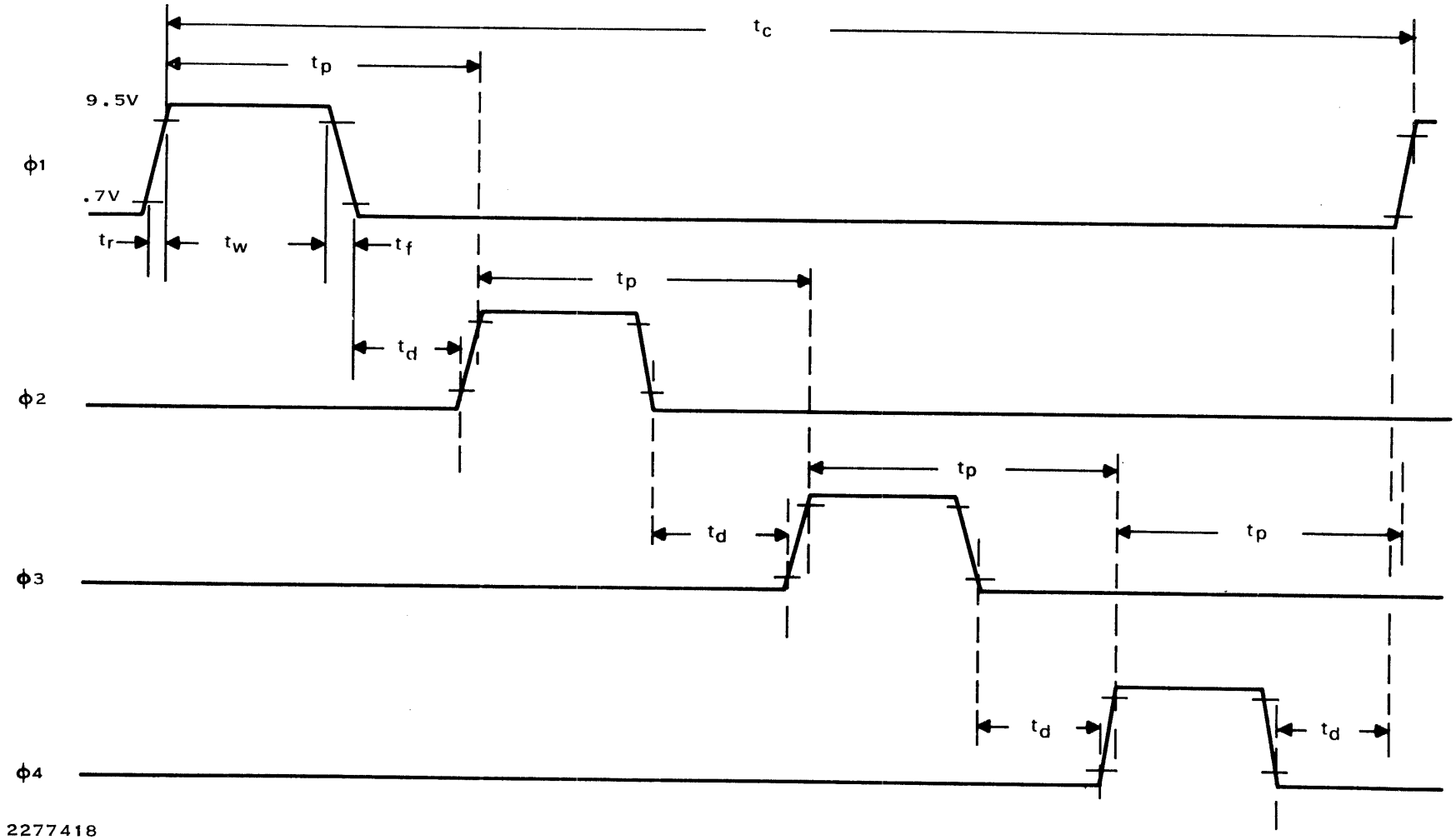


Figure 3-3. TMS 9900 Four-Phase Timing

Table 3-2. TMS 9900 Clock Requirements

Parameter	Min (ns)	Nom (ns)	Max (ns)
Cycle time, Tc	300	333	500
Rise time, Tr	5	12	20
Fall time, Tf	10	12	20
Pulse width, Tw	40	45	100
Delay time, Td	0	5	15
Phase time, Tp	73	83	

If the basic clock timing checks out, verify that the duration of the active-low microprocessor reset (MPRST-) is greater than 1.0 microseconds. Probe the MPRST- signal at the TIM 9904 output (UH078/UEB074-04), and use the following programmer panel routine to initiate the reset:

Memory Address (MA)	Data (MDE)
8000	0360
8002	1000
8004	1000
8006	1000
8008	10FB

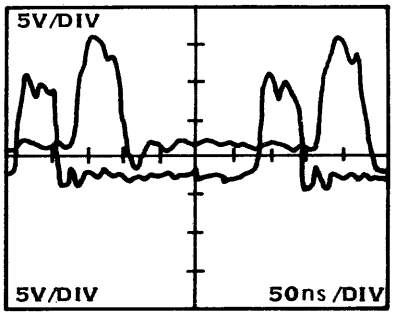
Then enter;

8000 into PC
(WP entry not required)

Depress RUN.

3.4.3 TILINE Checks

The TFDC must be capable of accepting command words and returning status words before starting any extended self-tests or running the DDFLOP diagnostic. The TILINE interface must be checked to determine if it is responding at all, and if it is working within specifications. Refer to the waveforms of Figure 3-5 for reference while performing these checks.



2277356

Figure 3-4. Two Phases of TMS 9900 Clock (No Overlap Permitted)

3.4.3.1 Slave Read Check. Check the TILINE response by attempting to read status word W7 from the controller. With an assumed base address of F800, attempt to read location F80E from the 990 front panel:

Depress HALT/SIE	for single instruction execution.
Enter F80E	(binary 1111 1000 0000 1110) on data entry switches
Depress ENTER MA	to load the adddress into MA register
Depress MDD	to display the "memory" location

Interpret the W7 status code as shown in Table 3-3.

If the returned status code does not agree with any of the given responses, the controller may not have responded to the command. Check the controller slave go delay SLGODLY relative to TILINE go (TLGO-) as follows:

1. Refer to sheet 12 (sh 12) of logic drawing 2261692/2267297.
2. Set oscilloscope sweep to 0.05 microseconds/div, negative trigger (from channel 1).
3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.
4. Connect oscilloscope channel 1 probe to TLGO- at UA090/UAB101-9.
5. Connect channel 2 probe to SLGODLY at UG102/UDF116-6.
6. Attempt to read W7 (CPU byte address F80E) as previously described or by 990 machine code loop.
7. Verify that the delay from the falling edge of TLGO- (chan 1) to rising edge of SLGODLY (chan 2) is 100 ± 10 nanoseconds.

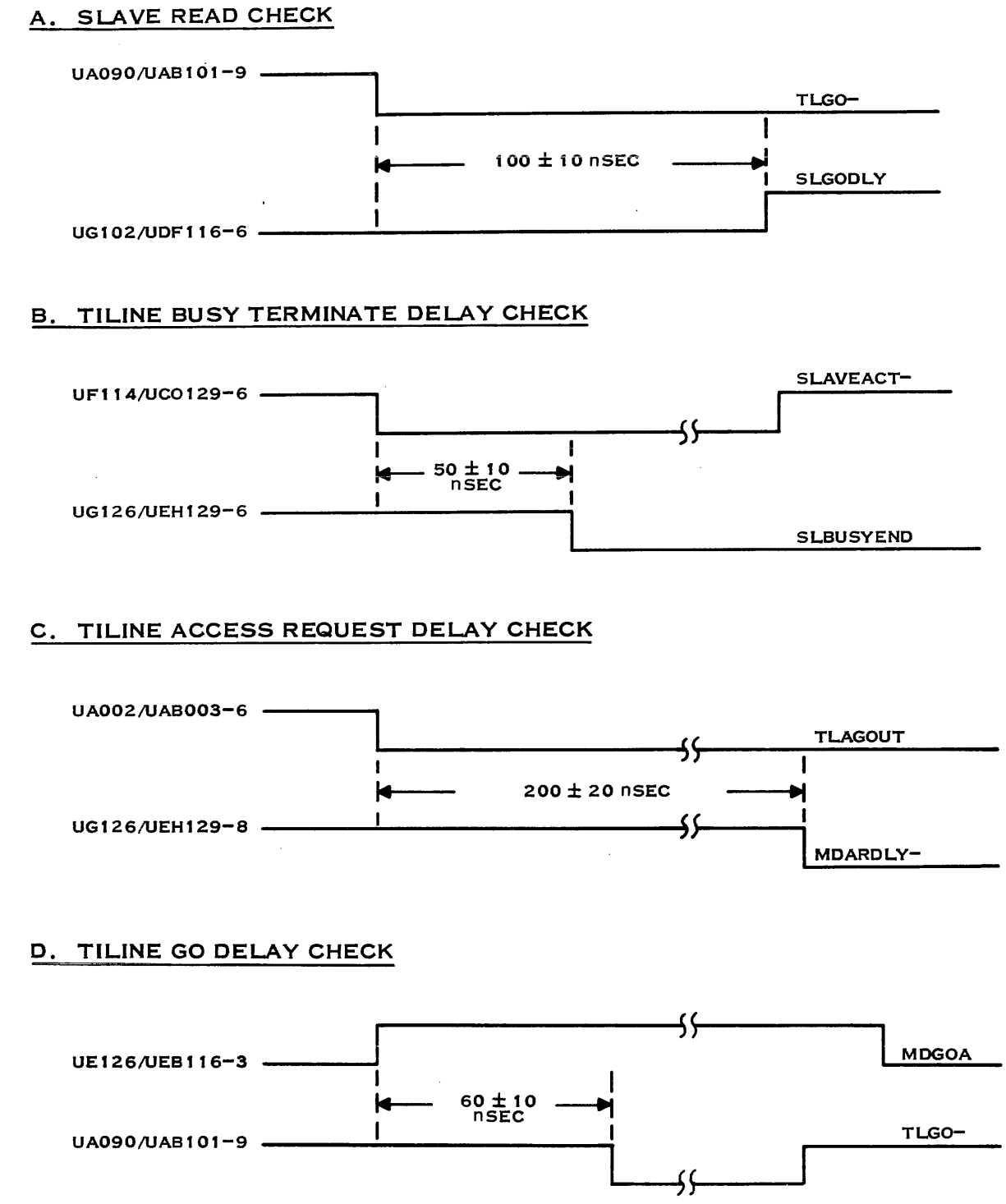


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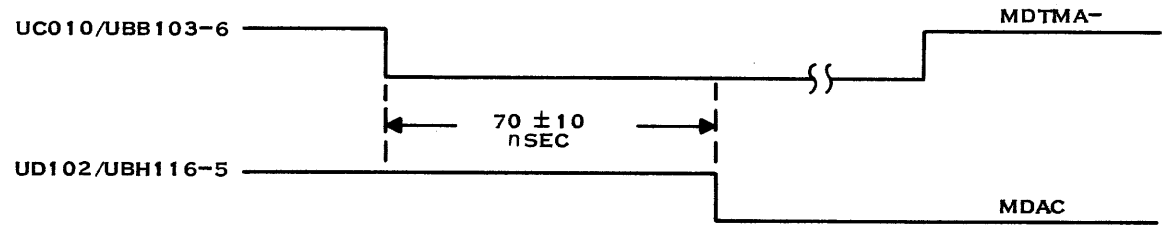
Figure 3-5. TILINE Timing Check Waveforms (Sheet 1 of 2)

E. TILINE MASTER DEVICE TERMINATE DELAY CHECK



F. TILINE TIMEOUT DELAY CHECK

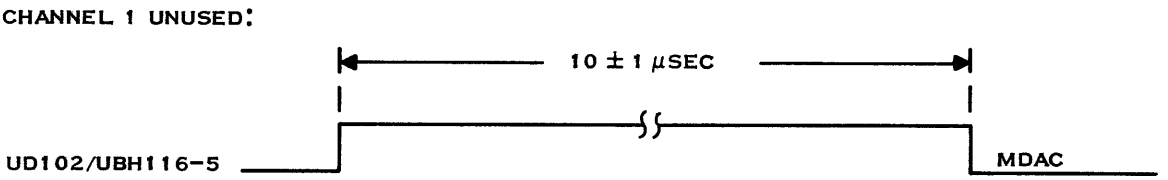


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Figure 3-5. TILINE Timing Check Waveforms (Sheet 2 of 2)

8. If the delay is out of specification, investigate the SLGODLY circuitry. Primary suspects are value changes in the RC components at SLGORC.

9. If SLGODLY is not occurring at all, move the channel 2 probe to SLADROK (UD026/UBH029-9) to determine if the TFDC is decoding the slave address. SLADROK should be issued each time the read request is sent to the TFDC. If SLDROK is not occurring, suspect:

   a. Human error in entering TFDC address at 990 computer

   b. TFDC on-board address switches set wrong

   c. Defective switch section (UC038/SBB043)

   d. Defective DM8136 comparator stage UD026/UBH029 UB002/UAG003, or UE026/UCD029

10. If SLADROK is occurring, trace out the signal flow (sh 12, sh 6) to localize the fault. If the slave is idle (SLVIDLE, UF114/UCD129-9 high) but SLVTMQ- is remaining inactive (high) at UF050/UCK058-12, suspect the TILINE I/F control ROM, UE050/UGD038, and the other circuitry of the TILINE I/F control state machine. The TILINE I/F control ROM (like all TFDC ROMs) is seated in a socket. Remove and reinsert the ROM to check seating problems. Replace with a new ROM if necessary.

Table 3-3. Controller and Drive Status Interpretation

TFDC Status Codes (W7)	Problem
0XXX	Controller busy (hung)
A001	Unit error: see disk status (W0)
A002	Search error: R/W command
A004	Cmd timeout: operator error
A008	Rate error: TILINE transfer problem
A010	ID error: R/W channel
A020	TILINE timeout: memory address problem
A040	Data error; R/W command
A050	ID & data error: format R/W problem, IBM invalid record type
A080	Memory error: main memory bad
AXFF	Self-test error (See W2 for self-test diagnosis)
A100	Abnormal completion: I/O reset detected, self-test complete without errors
C0B0	No error, operation complete

Disk Status Codes (W0)	Problem
CXXX	Illegal drive
DXXX	Unit off line
1XXX	Unsafe (need store registers)
X4XX	Seek incomplete (need restore)
2XXX	Diskette write protected.

Note:

X = don't care

There is little else that can be done until the slave logic operates correctly, as all DDFLOP and extended self-test commands must enter the TFDC via TILINE slave operations. Detailed manual troubleshooting with logics, oscilloscope, and logic analyzer are required. Normal operation of the TILINE I/F is described in Section 2.

Once the TILINE logic of the TFDC can accept commands over the TILINE, it becomes convenient to load DOCS and DDFLOP into the 990 computer. The DDFLOP verbs can be used to enable extended self-tests that are in the on-board 9900 control program ROMS. DDFLOP verbs may also be used to control execution of the DDFLOP diagnostic tests.

DOCS loading and DOCS verbs are described in volume 1 of *Model 990 Computer Unit Diagnostics Handbook*, 945400-9701. DDFLOP and the DDFLOP verbs are described in volume 3 of the diagnostics handbook, 945400-9703.

Table 3-4 is a summary of the extended self-tests in the 9900 control program of the TFDC. Note that the table also summarizes the possible error status words generated by the self-test. An error status word will be found in W2 whenever AXFF status is reported in W7. Any of the self-tests may be activated by sending the following command words to the TFDC:

1. W0 0000 Clear previous drive status
2. W1 8700 Extended self-test command
3. W2 0100 Clear previous self-test status
4. W3 000n Test number n, right justified (see table).
   Use C00n to loop on test n. Use an I/O reset to clear the test loop
5. W4 0000 except where specified otherwise (see table)
6. W5 — Part of TILINE address (if required — see table)
7. W6 — Unit select, TILINE address (if required)
8. W7 0000 Initiate operation, interrupt not enabled

Refer to the 9900 control program listing (Appendix B) for additional information on the self-tests.

3.4.3.2 TILINE Busy Terminate Delay Check. Use the DDFLOP ST (self-test) verb to command test number C005, without a status check. This test causes the TFDC to loop on the TILINE master/slave test (MSTENT).

Check the controller slave busy end (SLBUSYEND-) delay relative to slave active (SLAVEACT-) as follows:

1. Refer to sheet 12 (sh 12) of logic drawing 2261692/2267297.
2. Set oscilloscope sweep to 0.05 microseconds/div, negative trigger (from channel 1).
3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.
4. Connect oscilloscope channel 1 probe to SLAVEACT- at UF114/UCO129-6.
5. Connect channel 2 probe to SLBUSYEND- at UG126/UEH129-6.
6. Verify that the delay from the falling edge of SLAVEACT- (chan 1) to rising edge of SLBUSYEND- (chan 2) is 50 ± 10 nanoseconds.
7. If the delay is out of tolerance, adjust by changing RH130/RFD111 or CH132/CFE114.

8. If SLAVEACT- or SLBUSYEND- is not changing state, the self-test may not be executing or there is a fault in the slave logic or TILINE I/F control logic. Trace out signals with oscilloscope and logic drawings. If the self-test will not execute, and no human error is involved, it may be necessary to resort to AMPL testing of the TMS 9900, 9900 control program ROMs, and associated logic.

9. Once this check is succesfully completed, go on to the next check without changing the test setup. If no other checks are planned, terminate the loop with an I/O reset (RESET on 990 front panel).

3.4.3.3 TILINE Access Request Delay. This check and the following checks involve the TILINE master access logic. The primary circuits involved are the TILINE I/F control logic (state machine) on logic sheet 6 and the logic on sheet 13. The TMS 9900 processor logic must be operating for any TILINE master access operation (or any self-test) to be properly executed.

Use the same test loop as the previous test (DDFLOP ST verb initiating self-test C005). The TFDC is looping on the TILINE master/slave self-test (MSTENT). Check the delay of MDARDLY- with respect to the falling edge of TLAGOUT as follows:

1. Refer to sheet 13 of logic drawing 2261692/2267297.

2. Set oscilloscope sweep to 0.05 microseconds/div, negative trigger (from channel 1).

3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.

4. Connect oscilloscope channel 1 probe to TLAGOUT at UA002/UAB003-6.

5. Connect channel 2 probe to MDARDLY- at UG126/UEH129-8.

6. Verify that the delay from the falling edge of TLAGOUT (chan 1) to falling edge of MDARDLY- (chan 2) is 200 ±20 nanoseconds.

7. If the delay is out of tolerance, change RH122/RFD107 or CH124/CFD109 to adjust the delay.

8. Once this check has been performed successfully, go on to the next check without changing the test loop. To exit the loop, execute an I/O reset.

3.4.3.4 TILINE Go Delay (Master Cycle). This check involves the TILINE master access logic. The primary circuits involved are the TILINE I/F control logic (state machine) on logic sheet 6 and the logic on sheets 12 and 13. The TMS 9900 processor logic must be operating for any TILINE master access operation (or any self-test) to be properly executed.

Use the same test loop as the previous test (DDFLOP ST verb initiating self-test C005). The TFDC is looping on the TILINE master/slave self-test (MSTENT). Check the delay of TLGO- with respect to the rising edge of master device go (MDGOA) as follows:

1. Refer to sheets 12 and 13 of logic drawing 2261692/2267297.

2. Set oscilloscope sweep to 0.05 microseconds/div, positive trigger (from channel 1).

3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.

4. Connect oscilloscope channel 1 probe to MDGOA at UE126/UEB116-3 , the MDGOA gate output.

5. Connect oscilloscope channel 2 probe to TLGO- at UA090/UAB101-9.

6. Verify that the delay from the rising edge of MDGOA to the falling edge of TLGO- is 60 ± 10 nanoseconds.

7. If the delay is out of tolerance, adjust MDGORC by changing RE088/RCD101 or CG088/CDF101.

8. Leave the loop running and go on to the next check. If no check is to be performed, terminate the loop with an I/O reset.

3.4.3.5 TILINE Master Device Terminate Delay Check. This check involves the TILINE master access logic. The primary circuits involved are the TILINE I/F control logic (state machine) on logic sheet 6 and the logic on sheet 13. The TMS 9900 processor logic must be operating for any TILINE master access operation (or any self-test) to be properly executed.

Use the same test loop as the previous test (DDFLOP ST verb initiating self-test C005). The TFDC is looping on the TILINE master/slave self-test (MSTENT). Check the delay between the assertion of master device terminate access (MDTMA- falling edge) and the end of the master device access cycle (MDAC falling edge) as follows:

1. Refer to sheet 13 of logic drawing 2261692/2267297.

2. Set oscilloscope sweep to 0.05 microseconds/div, negative trigger (from channel 1).

3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.

4. Connect oscilloscope channel 1 probe to MDTMA- at UC090/UBB103-6.

5. Connect oscilloscope channel 2 probe to MDAC at UD102/UBH116-5.

6. Verify that the delay from the falling edge of MDTMA- to the falling edge of MDAC is 70 ± 10 nanoseconds.

7. If the delay is out of tolerance, adjust MDTMRC by changing the value of CH112/CFD113.

8. The self-test loop is not required for the next check. Terminate the loop with a DOCS .IS (initialize system) verb.

9. Disconnect the oscilloscope channel 1 probe, but leave the channel 2 probe in position (on MDAC) for the next check.

Table 3-4. Controller Program Extended Self-Tests

```
 ************************************************************
TESTAL - TFDC Self-Test
This test group contains self-test for the following:
  9900 MPU  -- Instruction tests
  RAM       -- Walking ones and zeros test
  ROM       -- Checksum test
  9901 PIA  -- Input, output, timer, and interrupt test
  Slave reg -- Read after write of W0-W7
  TILINE master/slave logic -- Read/write busy slave
  Data generator/separator -- Simulate data skew
  Disk drive I/F -- Read/write control/status bits
  TILINE interrupts -- Check interrupt logic

On power-up, the fault LED is turned on by RST-
and self-test begins after the PIA and CRU are
initialized. Each test loads R0 with a number
indicating the test part and intermediate progress.
Successful completion of all tests results in the
fault LED being turned off, and '00' in the right byte
of W2. All self-test routines utilize the miscellaneous
work space (MISCWS). Interrupts are disabled except
for  tests 3,5,6, and 8.

Failure of any test halts further testing. The FAULT
LED remains on, the processor goes to idle routine,
the contents of R0 are written in W2, and 'FF' is
written in the right byte of W7 (controller status).

************************************************************
MPTENT   9900 MPU Test

This test exercises all instructions practical to
test in a power up test. No CRU instructions are
exercised at this time in self-test (see the PIA
test for the first CRU operations). After
preliminary testing, the MPU test performs successive
loops of various arithemetic and other tests
using two variables which are tested with
64x19 different values.

Status returned:

00   Failure of LI, INCT, or JNO
01   Failure of MOV, SRA, SRL, CI, or JNE
02   Failure of ANDI, BL, XOR, INC, or B
03   Failure of ORI
04   Failure of interrupt mask bits
05   Failure of BLWP or status returned in RTWP
06   Failure of other tests in loop

 Note: R0=0006 for any errors detected in this test

************************************************************
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
    RATENT - RAM Test

    This test begins by clearing and then writing all
    ones to each RAM location used for workspace
    register or firmware variables (excluding
    the test workspace). The original values must be
    be restored since this test can be called from
    ext command.

    The test then writes a walking ones pattern to
     RAM above the workspace and variable locations.
    After verification, this test is repeated with
    walking zeros. Finally, an address check is performed
    by writing an incrementing pattern to addresses
    8100-81FE (tests address lines 14-08).

    Status returned:

    10   RAM #1 or #2 bad  (bits 8-15)
    11   RAM #3 or #4 bad  (bits 0-7)
    12   Failed address line test (ADR08-14)

************************************************************
    ROTENT - ROM Test

    This test performs a checksum on the contents
    of the controller ROM.


    Status returned:

    20   Checksum error

     Note:  Checksum remainder is written into W3 if not 0.

************************************************************
    PITENT - PIA 9901 Test

    This test begins by writing to the PIA output bits
    in the clock mode. The output bits will then be
    checked and input bits read for expected
    values. The last test combines a check on the timer
    clock and interrupts.


    Status reported:

    30   Failure to load PIA clock count
    31   Failure on first control outputs pattern
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
    32   Failure on second control outputs pattern
    33   Failure on write enable active
    34   Failure on write enable inactive
    35   Failure on attention bit 5's pattern
    36   Failure on attention bit A's pattern
    37   Failure on attention bit F's pattern
    38   Clock frequency too fast
    39   Clock frequency too slow
    3A   Clock counter did not go to zero or intrpt
    3B   Clock counter did not restart after intrpt
    3D   Illegal data separator overrun
    3E   TILINE error encountered

**********************************************************
    SLTENT - Slave Test
    This test writes a test pattern to all slave registers
    (W0-W7) and then verifies the contents. Each slave
    register will be tested with all of the following
    test patterns:
             A0A0    0A0A
             5050    0505
             2828    8282
             1414    4141

     Note: the MSB of W7 will be zero throughout this
           test. All registers will be cleared at end of
          test if completed successfully.

    Status reported:

    40   Slave registers failed first test pattern
    41   Slave registers failed second test pattern
    42   Slave registers failed third test pattern
    43   Slave registers failed forth test pattern
    44   Slave registers failed fifth test pattern
    45   Slave registers failed sixth test pattern
    46   Slave registers failed seventh test pattern
    47   Slave registers failed eighth test pattern

**********************************************************
    MSTENT - TILINE Master/Slave Test

    This test sets up the controller TILINE address
    based on the onboard switches. It then checks for
    TILINE interface idle (TLIFCO = 0), followed by
    eight TILINE master cycles (read and write) and a
    a read without master cycle.

    Interrupts are enabled to make sure TLTO is ok
    with eight master cycles. A TILINE memory error is
    error is also forced to check that
    also forced to check that portion of the controller
    interrupt handling.
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
     Status reported:

     50   TILINE I/F controller not idle at beginning of test
     51   Failed on read after write of A's
     52   Failed forced MSB = zero, MDSLTST set to zero
     53   Failed on read after write of 5's
     54   Failed while writing F's to TILINE data
     55   Failed while writing 0's to TILINE data
     56   Failed on read w/o master cycle, data not equal to 0.
     57   Failed forced MSB = one, MDSLTST set to one
    *58   Failed forced TILINE memory error, got TLTO (status s/b 5)
     59   Failed forced TILINE memory error, no interrupt
     5E   Illegal data separator overrun
     5F   Illegal TILINE timeout

**********************************************************
     DSTENT - Data Separator Test

     This test checks simulated data generated by the
     data separation logic representing worst case
     bit skew from the disk. During the data simulation
     CRC is checked for 1 until CRC word is read and 0
     after CRC word. Data separator overrun is also tested.
     is also tested. The PIA timer interrupt
     The PIA timmer interrupt provides a timeout abort
     for failure of MPREADY during reads or DSOVRN in the
     overrun test.

     Status reported:

     60   Simulated data compare failed on 1st word (sync)
     61   Simulated data compare failed on 2nd word
     62   Simulated data compare failed on 3rd word
     63   Simulated data compare failed on 4th word
     64   Simulated data compare failed on 5th word
     65   Simulated data compare failed on 6th word
     66   Simulated data compare failed on 7th word
     68   Data separator overrun failed to come true
     6b   Data separator overrun early
     6c   DCRCER failed to go to zero after CRC word read
     6e   Illegal TLTO or TLMER
     6f   DCRCER not equal 1 before CRC word read

**********************************************************
     DITENT - Disk Interface Test
     This test checks any available remote (radial I/F)
     drives buffer I/F by toggling a multiplexed test
     bit on and off. A remote drive is determined to be
     active by sensing 'DPONL'. Any selected drive which
     does not return 'DPONL' is ignored. Following the
     remote test, all status CRU input bits are verified
     to be false.

      Note: Failure of the remote I/F test will report an
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
          error code to W2, but the controller FAULT
          LED will not be affected by such an error.

    Status reported:


    70   'TESTL' toggle test failed (remote drive 0, on-line per  DPONL)
    71   'TESTL' toggle test failed (remote drive 1, on-line per  DPONL)
    72   'TESTL' toggle test failed (remote drive 2, on-line per  DPONL)
    73   'TESTL' toggle test failed (remote drive 3, on-line per  DPONL)

         General status:
    74   Remote test failed and status bits not all zeros
         with no drives selected
    75   Local status bits not all zeros with no drives
         selected

**********************************************************
    INTENT - TILINE Interrupt  Test      (self-test #8)

    This test checks TILINE interrupts associated with
    W0 (attention bits and attn masks), W6 (unit
    change interrupt), and W7 (idle, complete, error, and
    interupt enable). Tiline master cycles (up to 5) are
    required to toggle the interrupt logic involved.

    Status reported:

    80   IDLE active when should be inactive
    81   INTA active when should be inactive
    82   INTEN and/or ERR stuck at zero
    83   ERR and/or COMP stuck at one
    84   Complete or interrupt enable stuck at zero
    85   Interrupt enable stuck at one
    86   Attention mask bits stuck at zero
    87   At least one attention bit stuck at one
    88   AT0 stuck at zero
    89   AT1 stuck at zero
    8A   AT2 stuck at zero
    8B   AT3 stuck at zero
    8C   At least one attention mask bit stuck at one
    8D   Forced unit change failed interrupt test
    8E   Illegal TILINE or reset interrupt

**********************************************************
    ESTENT - Extended Self-Test          (extended cmd = 7)

    This routine provides the capability to execute individual
    self-tests on the controller. The selected test number
    is stored in slave register 3 (W3), right justified.
    Test numbers correspond to the order of the power up
    self-tests.  Any value beyond these bounds will call up
    all tests.
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
          W7      Test
          0        9900 test
          1        RAM  test
          3        ROM  test
          4        PIA  test
          5        Slave test
          6        Master/slave test
          7        Disk I/F test
          8        TILINE Interrupt test
          9        External disk I/F (local/remote) test
          A        VCO adjust test
          B        Drive head oscillation test
          C        Tap test
          D         Delay diagnostic command

    Error codes are the same as TESTAL.  The left byte of W7 is
    returned as given on test entry. The FAULT LED will not be
    affected by these extended tests, except for test 9 (loopback),
    unless the full power up test is run.

     Note: In order to loop on the specified test, enter
           code 'COOX' in W3. The test will be repeated
           until an I/O reset or equivalent stops it. In
           the meantime, no status will be available to the
           front panel because the controller is busy. The
           "loop on" mode is helpful for scope loops in checkout.

    Subroutines called:
         TESTAL        Full self-test
         MPTEST(R2)    Individual tests per W3 code

    Errors reported:
         W2            Per individual test fail codes
         W7            'FF' in right byte; error detected

**********************************************************
    IFTEST - Extended Disk I/F Test       (ext cmd = 7)

    This test provides a local/remote disk I/F loop-back
    test. Special loop-back connectors must be used
    (one at a time only!) to loop back disk con-
    trol pulses through either the local I/F connector
    (P5) or one of the two remote I/F connectors (P3, P4).
    The local I/F loop-back connector may also be used
    on a remote I/F board cabled to one of the controller
    remote I/F connectors.

    This test starts by setting up a zeros FM data
    stream from the data separator, looped-back through
    the connector read data signal. A scope may be used
    to look at RDDAT and verify a 4-microsecond pulse train
    generated at WRDAT and looped-back to RDDAT. This
    pattern is enabled throughout the test.
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

Next, write enable is toggled to provide a scope sync for observing the rest of the test loop patterns. If any errors were detected in the previous test (as when looping on the test), write enable (WRTEN) is toggled twice and the FAULT LED is turned on. Following WRTEN, a series of low pulses are issued from the disk control logic to be looped-back through the appropriate connector.

Variations exist between the local and remote (added DIR/TESTL loop-back and presence of DPONL when TR43 is low with standalone remote, and whenever a remote I/F has RDY true). Each status line is tested for active and inactive sense (except for DPONL on remote I/F - tested previously). The sequence of the test pulses is given below and error reporting is explained in the following table.

Order of control/status loop-back pulses:

1.	WRTEN	Low (scope sync pulse, 2 if err)
2.	SEL0/RDY	Low/high (remains for full test)
3.	TR43/DPONL	Low/high for remote (dponl not Looped back on local)
4.	DIR/TESTL	Low/high for remote (testl not Looped back on local)
5.	SEL1/INDEX	Low/high
6.	SEL2/TR00	Low/high
7.	SEL3/WP	Low/high
8.	STEP/DC	Low/high
9.	LOAD/TS	Low/high

Registers used:

	R0	Miscellaneous
	R1	Flag for standalone remote
	R2	Index for CRU base assignments
	R3	IFTWAT count
	R11	Link vector
	R12 CRUBAS	CRU base address

Subroutines called:

IFTWAT	53 microsecond delay

Errors reported (via W2):

This test reports individual bit errors by setting the following bits in W2:

Bit 15	Ready	stuck (SEL0- loop-back)
bit 14	INDEX	stuck (SEL1- loop-back)
bit 13	TR00	stuck (SEL2- loop-back)
bit 12	WP	stuck (SEL3- loop-back)
bit 11	TESTL	stuck (DIR- loop-back)
bit 10	DC	stuck (STEP- loop-back)

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
     bit 09      TS     stuck ( LOAD- loop-back )
     bit 08      DPONL  stuck ( TR43- loop-back )

      Note: * Bits 07 through 00 should always be zero.

*************************************************************

     VCOENT - Vco Adjust Test          (Ext cmd code=7, part a)

     This routine is accessible only by the extended self
     test command (W3 = A). It holds the data separator
     in reset while turning on and off the crystal
     6 mhz reference to the VCO. This results in a ramp
     pattern on the VCO input which can be observed on a
     scope for the specified damping range indicated by
     the VCO input ramp. This routine is a closed loop, so
     I/O reset must be used to get out of it. No status is
     reported from this routine and no interrupts are en-
     abled.

     Ramp up = 0.6 milliseconds
     Ramp down = 0.45 milliseconds

     Registers used:
          R0            delay count for ramp period
          R1            Flag for which state of VCO ref
          R12  CRUBAS   CRU base addr

*************************************************************
     HDTEST - Drive Head Test    (Ext cmd = 7 (#B))

     This test writes a full track of unformatted data
     (specified by the user) to the cylinder of the last
     seek operation. The side is specified in W0 of
     the command. After writing a full track, the controller
     loops on a continuous read of the data from the
     disk.

      Note: For read-only scope loop on a pre-written
            diskette use a sector number value greater than
            or equal to 1B in W2. This is useful for alignment
            and other checks.

           For continuous write operation, use sector
           number 1A. The controller will write the specified data
           to the selected unit until a reset aborts the test.

     An oscilloscope may be used to monitor the data
     stream coming off of the diskette to check jitter
     caused by bit shift, speed variation, etc. The phase
     lock loop circuit on the controller may also be
     monitored for observation during the read. A suspect
     drive (from data errors found in formatting or in
     the PDT tests) should be tested for both heads to see
```

Table 3-4. Controller Program Extended Self-Tests (Continued)

```
     if the bit variations are excessive. Data = FFFF is
     best for observing speed variations and bit asymmetry
     while data = B6DB produces the worst case bit shift
     pattern. Data = DB67 is the most challenging pattern
     for the data separator to track.

     Registers used:
          R0             miscellaneous
          R3   type      diskette type (one or two sided)
          R8   cylndr    diskette cylinder position of test
          R9             interrupt return vector
          R10  unit      unit # of selected drive
          R11            link vector
          R12  CRUBAS    CRU base addr

     Subroutines called:
          POSENT         Load heads at current position
                         (errors include: UE, OL, US, NR,
                         and SI.

     Errors reported:
          Unit error     Invalid unit number, drive unreported,
                         diskette write protected
          Command        Wrong side selected on a single-sided
          timeout        diskette

*************************************************************
     TAPENT - Tap Test          (Ext cmd #7   (test# C))

     This test is implemented for the purpose of doing a
     media incoming wear test. The test alternately loads
     and unloads the heads on the desired unit every time
     index is detected from the drive. This synchronous
     loading and unloading causes maximum wear on one
     spot of the diskette being tested. An I/O reset is
     required to abort this test.

     Registers used:
     R0                  miscellaneous
     R10   unit          unit # of user spec'd drive
     R11                 link vector

*************************************************************
     DLYENT - Diagnostic Delay         (Ext cmd #7, (test C))

     This routine takes the word count from the command
     register (W4) and uses it as a decrement count
     value while the controller processes timer interrupts.
     The purpose of this command is to allow syncronous
     operations to a drive or drives involving head
     load or seek operations; for example, timing
     to allow a write operation
     immediately after head load on consecutive
     revolutions of the diskette.

     Registers used:
     R0                  Decrement register

*************************************************************
```

3.4.3.6 TILINE Timeout Delay. This check verifies that the on-board TILINE timeout circuit will detect the fact that a slave device (such as main memory) has failed to respond to an attempted master read/write operation. All TILINE master devices have such a timeout circuit to abort a failed master cycle and prevent a TILINE lockup.

The check is performed by initiating a store registers operation with a nonexistent address for the returned words. The device access state (MDAC) should terminate within 10 microseconds.

1. Refer to sheet 13 of logic drawing 2261692/2267297.
2. Set oscilloscope sweep to 2.0 microseconds/div, positive trigger (from channel 2).
3. Set vertical gain to 2 volts/div or other convenient scale for TTL logic levels.
4. Connect oscilloscope channel 2 probe to MDAC at UD102/UBH116-5. (It should already be there).
5. Enter the following command program via the DOCS .MM (memory modify) verb and then execute via the DDFLOP LO (loop on) verb. The loop may be aborted by a DOCS .IS verb.

Address	Data	
X000	0000	(W0)
X002	0000	
X004	0000	
X006	0000	
X008	0002	
X00A	FBFE	
X00C	001F	
X00E	0000	(W7)

6. Verify that the positive pulse width of MDAC is 10 ± 1 microseconds.
7. If the delay is out of tolerance, adjust MDTORC by changing the value of RH126/RFD105 or CH128/CXXXXX.
8. After the pulse width has been verified, abort the command loop with a DOCS .IS verb.

3.4.4 DOCS and DDFLOP Diagnostics

DOCS (Diagnostic Operational Control System) is a small operating system that supports tests requiring operator interaction. DOCS also supports a set of general-purpose test verbs, such as initialize system (.IS), modify memory (.MM), go to user-specified address (.GO) and others. These verbs always consist of a period (.) and two upper-case alphabetic characters.

DDFLOP is a multipart progressive diagnostic test that tests the FD1000 flexible disk system. The philosophy of testing is to start with very limited tests of the controller only, and expand the scope and comprehensiveness of testing as each subsequent part is executed. Each test part has a set of error messages that may be generated as the result of a failure. TFDC status words may be read back and printed as each test completes.

DDFLOP includes a set of test verbs that are specifically designed for FD1000 testing. These verbs include test control verbs, such as execute test 1 (E1), execute all tests (EA) and a number of utility verbs. The utility verbs, such as display controller status (DC), execute self-test part n (STn), and loop on multiple commands (LO) are very useful in detailed troubleshooting.

One of the most powerful troubleshooting tools available is the combination of the DOCS and DDFLOP verbs with the on-board extended self-tests (Table 3-4). This is the final combination used to isolate a fault detected by the DDFLOP tests.

DOCS/DDFLOP testing of the TFDC, signal logic of the power supply/interface board, drive units, and disk media are described in the following two volumes:

Model 990 Computer Unit Diagnostics Handbook Volume 1 General 990 Unit Diagnostic Information, 945400-9701

Model 990 Computer Unit Diagnostics Handbook Volume 3 Diagnostics for 990 Mass Storage Devices, 945400-9703

DOCS general theory and organization, DOCS verb capabilities, and DOCS loading techniques are described in Volume 1 of the diagnostics handbook. Test descriptions, error message descriptions, operating instructions, and DDFLOP verb descriptions are given in Volume 3 of the diagnostics handbook. That information is not duplicated in this manual.

3.4.4.1 General Procedure for Testing with DOCS/DDFLOP Diagnostics. The general procedure to be followed is:

1. Execute the DDFLOP test parts 1-7 in order and record all error messages.

2. If no errors occur, go on to interactive test parts 8 and 9.

3. If errors occur, start over and repeat the first (lowest part number) test to fail. Use the display controller (DC) verb to display status from slave registers 0-7 (W0-W7). Refer back to the control and status word formats (Figure 1-18) to interpret the status bits and attempt to determine the general type of error.

4. Refer back to the extended self-test descriptions in Table 3-4. Select applicable self-tests from the table and initiate them with the DDFLOP STn verb. Self-test diagnostic error codes are returned to the 990 in status word W2. Refer to the table for error code interpretation.

5. Use the ST verb with a test number of C00n to loop on test n. The loops are very convenient for oscilloscope investigation of waveform relationships in the TFDC logic.

6. Perform the margin tests and PLL tests described in subsequent paragraphs. These tests are particularly useful if the TFDC passes the DDFLOP tests but has an excessive error rate in actual operation.

7. If nothing can be made to work properly, it may be necessary to go to AMPL testing.

3.4.4.2 Margin Test. The following description applies to revision C (and above) of the DDFLOP diagnostic, to be used with multilayer controllers 2261690 revision F (and above) as well as all fineline (2267295) controllers. The test requires a good DSDD diskette.

The TFDC uses built-in write precompensation on MFM to reduce the burden on the data recovery circuits during read operations. The net effect of write precompensation is to reduce the possibility of data errors from the disk. Automatic read retries are initiated by the TFDC upon detection of read errors. The margin test allows the operator to defeat these safeguards and to quickly estimate an overall error rate. The idea is that write precompensation and controller retries may mask a subtle degradation in performance. The margin test provides a measure of the entire system error margin. Media, drive, power supply/interface board and TFDC are all involved in this test.

A margin test is initiated by a DOCS MT verb. Prompts allow the operator to independently enable or disable controller retries and write precompensation. Some errors are to be expected when these features are disabled. Once the test has been initiated, retries and write precompensation options are fixed until a reset occurs or the test completes normally (with or without errors).

NOTE

If the margin test is aborted by the operator, the RS (reset) verb must be executed before going on to other tests.

The margin test (with retries and write precompensation disabled) should execute for 80_{16} loops with no more than 8_{16} errors. If the margin test fails, one possible cause is a fault in the test system (drive, power supply/interface board, diskette) or an electrically noisy environment. If the drive/media combination has a bit shift error greater than 650 nanoseconds, the margin test may be run with write precompensation enabled. With write precompensation enabled, no errors are allowed in 80_{16} loops. Detection of test system bit shift errors is described with data separator troubleshooting in paragraph 3.4.6.2.

3.4.5 Testing with Extended Self-Tests

Refer back to Table 3-4, which summarizes the error messages and the functions performed by the extended self-tests. A basic group of self-tests is invoked each time a reset is performed. More extensive self-tests can be invoked by transmitting the proper control words over the TILINE to the controller. As shown in the TFDC status and control word formats (Figure 1-18), an extended self-test is commanded by W3 with the extended mode bit set and a command code of 111.

The following command words are required to activate a self-test:

1. W0 0000 Clear previous drive status
2. W1 8700 Extended self-test command
3. W2 0000 Clear previous self-test status
4. W3 000n Test number n, right justified (see table)
   Use C00n to loop on test n. Use an I/O reset to clear the test loop

5. W4 0000 except where specified otherwise (see table)
6. W5 — Part of TILINE address (if required — see table)
7. W6 — Unit select, TILINE address (if required)
8. W7 0000 Initiate operation, interrupt not enabled

These commands may be manually entered into memory via the 990 computer front panel if necessary. Alternatively, they may be set up in memory via the DOCS memory modify (.MM) verb. The most convenient means of entering the commands and executing the self-tests is the DDFLOP self-test (STn) verb.

Self-test failure is indicated by controller status AXFF in status word W7. When this code is returned in W7, the error code is in W2. Error codes are given in the table. Each code identifies the self-test that failed in addition to specifying the error detected. The DDFLOP display controller status (DC) verb provides a hexadecimal-format printout of the contents of W0-W7 from the TILINE slave registers.

Self-tests may be looped by preceding the test number with C00, as in C005 or C00A. Loops may be terminated by a reset such as that issued by the DDFLOP RS verb.

Refer to the 9900 control program flowcharts and the listing (Appendix A, Appendix B) for additional information concerning the self-tests.

3.4.6 Data Separator Troubleshooting Hints

The data separator logic is effectively tested by any operation that involves recovery of recorded data from a diskette. Two of the onboard extended self-tests are particularly valuable for data separator troubleshooting. These tests are:

Test	9900 Control Program Mnemonic	Self-Test Number
Data separator test	DSTENT	6
VCO adjust test	VCOENT	A

The margin test (DDFLOP verb MT) is useful for detecting marginal operation of the data separator logic and PLL.

Failure of the data separator self-test can be the result of failures in several different parts of the disk interface logic. Although the phase-lock loop is one of the more critical circuits for data recovery, it is not valid to automatically assume that the fault must lie with the PLL. It is necessary to work through the logic diagrams (2261695/2267297) and the signal flow to isolate the source of the problem.

Self-test number 6 uses the read data simulator (paragraph 2.8) to generate an MFM bit stream that exercises the data separator logic. The 9900 control program enables the read data simulator with DSRDTST (logic sh 22). The simulated data output (SIMRDTA) is merged with the normal incoming data path as RDAT. The PLL (sh 14) provides the reference clock (PLLCLK-) for all the data separator logic.

The bit synchronization logic starts separating clock and data and issuing pulses to lock the PLL to the incoming clock rate. The address mark detector and phase correction logic (sh 17) looks for a recognizable address mark to mark the first valid word boundary. When ADDRMARK sets, the word controller starts on a word boundary and notifies the 9900 (with a DSRDY) each time a new word is fully shifted into the data shift register.

Operations continue in this manner, with the bit controller issuing shift pulses to the data shift register and the word controller notifying the TMS 9900 logic when a word is ready for transfer to the transfer register (register file 0).

The key signals for data separator troubleshooting are given in Table 3-5.

Table 3-5. Key Signals for Data Separator Troubleshooting

Signal	Logic Gate	Sheet	Function
DSRDTST	UN090/UGF116-9	22	Enables simulated read data
SIMRDTA	UN090/UGF116-13	22	Simulated MFM data
PLLCLK-	UN062/UHB074-13	14	Phase-lock clock — varies with incoming data rate on read, locked to SIXMHZ for all other
SYNCDPULSE	UO050/UHB058-7	16	Data synchronized to PLLCLK-
ADDRMARK	UK014/UEH016-10	17	Address mark detected. About 130 microseconds from start of data
MPINTREQ-	UH090/UEB089-32	2	9900 interrupt if timeout on ADDRMARK
DSRDY	UK078/UFK103-12	19	Data separator ready for word transfer
SHIFTDTAQ	UK038/UDF029-1	4	Shift data clock for SN74LS299 data shift register
DSTOBUSEN-	UK038/UDF029-2	4	Data separator output enable to 9900 bus
DSCRCER	UM014/UHG003-9 UL038/UFK074-13	18 19	CRC error latch

If the PLLCLK- waveform is suspicious, terminate the test with an RS (reset) verb and allow the controller to return to idle. PLL output signal PLLOUTC at UP029/UJB029-6 (sh14) should be locked in phase with SIXMHZ at pin 10 of the same SN74LS153 multiplexer. If not, check PLLREF and FDBKCLK (same IC device). Both inputs must be present for phase lock to occur. In idle operation, the nominal conditions are PLLCLK- frequency = 6 Mhz, and the VCO control voltage (VCOIN) = 4.0 volts. Other PLL troubleshooting hints follow.

3.4.6.1 PLL Troubleshooting with the VCO (Damping) Adjust Test. The phase-lock loop (PLL) circuits of logic sheet 14 consist of a digital phase comparator, loop amplifier, RC components for filtering and damping, and a voltage-controlled oscillator (VCO). An input multiplexer selects the two input waveforms to the phase comparator.

VCOENT (extended self-test part A) checks the PLL response by holding the data separator reset and turning the 6-Mhz crystal-controlled reference on and off. When the reference waveform is turned on, the VCO control voltage (VCOINF) ramps up from a near ground level to a level that phase-locks the PLL output to 6 MHz. The ramp time is an indication of how fast the loop would lock to an incoming bit stream.

The magnitude of the VCO control voltage under locked conditions is a measure of how close to the nominal design center the PLL is operating. The ramp down time is a measure of how fast the loop returns to quiescent conditions after the loss of signal.

Perform the VCO adjust test as follows:

1. Refer to sheet 14 of logic diagram 2261692/2267297.

2. Initiate the VCO adjust test via the DDFLOP ST verb, test number A.

NOTE

The VCO adjust test self-loops, so an I/O reset (such as DDFLOP RS verb) must be used to escape from the loop.

3. Connect oscilloscope channel 1 probe to monitor VCOINF at UP002/UJJ003-2 (or at the junction of RO010-CP006/RHE014-CJG014). Trigger the sweep from channel 1 (positive trigger) or from MDSLTST at UP029/UJB029-15 (positive trigger).

4. Set the sweep time at 1 millisecond/div and change as necessary to get the desired resolution. Make sure that the sweep is calibrated.

5. Set the vertical gain of channel 1 at 1 volt/div and switch as necessary to get the desired accuracy. Make sure the vertical gain is calibrated.

6. Compare the observed waveform to Figure 3-6 and note any deviations. The following symptoms may be observed:

   a. Ramp falls off too fast — Replace MC4044 phase detector

b. Ramp up is too slow — Add trim resistor in parallel with 4.7K resistor RP017/RJB022. The trim resistor is designated RP014/RJB019

c. Excessive noise on VCOIN — Check noise pickup on VCC1* at output of on-board regulator VRI020/KHG024. Also see step 8.

7. Without changing the oscilloscope connections, return the TFDC to idle by entering a DDFLOP RS verb. After the reset and self-test, the controller returns to idle. In this mode, the PLL is locked to SIXMHZ. Verify that the level of VCOINF is 4.0 ± 0.2 volts. The level is a function of the output frequency and the capacitance across the MC4024 1X1 and 2X1 inputs (CO006/CJG006). If the level is incorrect:

   a. Verify that capacitor CO006/CJG006 is marked 39 pf.

   b. Replace the MC4024

   c. Replace the capacitor if changing the IC does not correct the problem.

8. Loop on the data separator self-test (DDFLOP verb ST, test number C006). Measure the amount of 6-MHz noise coupled onto the VCOINF line. Be sure to ground the probe shield to prevent ac pickup. Use the high frequency reject if data feedback pumps are obvious. The 6-Mhz noise level should be less than 40 millivolts. Most boards will exhibit approximately 20-30 millivolts of 6-MHz noise.

3.4.6.2 Verifying the PLL after Margin Test Failure. The data separator and PLL logic are specified to handle data with bit shift up to 650 nanoseconds from nominal. If the DDFLOP margin test fails, it may be due to excessive bit shift in the drive unit or diskette, rather than data separator error.

The following procedure sets up a scoping loop in which the bit shift due to media and drive may be checked. If the bit shift is excessive, the drive/media should be replaced and the new drive/media verified. After verifiying acceptable bit shift, rerun the margin test.

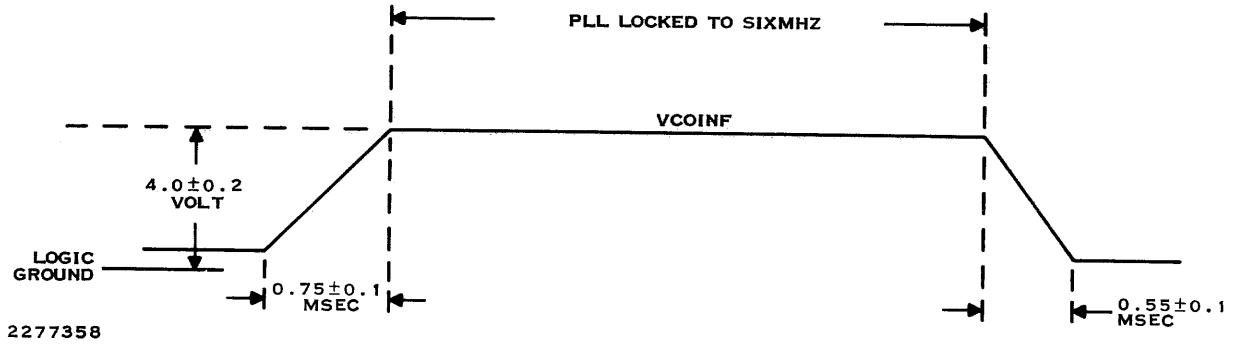

Figure 3-6. Voltage-Controlled Oscillator (VCO) Ramp Characteristics

1. Disable the MFM write data precompensation as follows:

   a. Initiate the margin test via the DDFLOP MT verb, specifying write precompensation off (0) and 80 read loops.

   b. Leave write precompensation off by aborting the margin test with an @ (at sign) entry while the controller is looping on read operations. Do not issue a reset.

2. Use the DDFLOP issue command (IC) verb to command a seek to track 4C.

3. Activate the drive head test (HDTEST) by entering the following program into memory (.MM) and looping on it via the DDFLOP LO verb:

Address	Data	
8000	0000	W0
8002	8701	
8004	0000	
8006	000B	
8008	B6DB	
800A	8008	
800C	0800	
800E	0000	W7

4. Set up the oscilloscope to synchronize on incoming data, RDTA, at UP083/UJF103-8 (sh 21).

5. Verify that the delay between the first and fourth data pulse of each oscilloscope trace is between 3.35 and 4.0 microseconds. If the spacing is less than 3.5 microseconds, bit shifting is excessive in the drive/media combination.

6. Clear the read loop (and the precompensation disable) with a DDFLOP reset (RS) verb.

3.4.7 Remote Interface Troubleshooting Hints

The normal self-test executed upon reset includes a loopback test of the TFDC remote interface and the power supply/interface board in the international chassis. The direction/side select control signal is encoded in the TFDC remote interface logic and transmitted in the assigned time slot of YCNTL1 and YCNTL2 (2261692/2267297, sh 20)

Refer to the control signal decoding logic of the power supply/interface board (2265018, sh 3 or 2269979, sh 2). The encoded control signal is decoded as DIRR and sent to the status signal encoding logic as TESTL-. TESTL- is encoded again (2265018, sh 2 or 2269979, sh 3) by an SN74LS151 multiplexer and transmitted back to the TFDC in an assigned time slot of the YSTAT signal.

As shown on sheet 21 of TFDC logic drawing 2261692/2267297, the multiplexed status signal (STAT) is once again demultiplexed to a single line and sent to the TMS 9901 PIA (sh 4) as TESTL. If the drive is on line, as indicated by DPONL, the self-test program checks to determine if TESTL is present.

Passing this self-test (DITENT) is a pretty good indicator that the entire control/status encoding and decoding operation is working. Failing this test, on the other hand, does not pin the fault down even to the unit (chassis or controller) level. There is an extended self-test (IFTEST, test part 9) that can help isolate the problem.

The first order of business is to check out the TFDC parallel I/F with a 50-pin loopback connector to verify operation of the simplest logic. After that, the TFDC remote logic is checked. Once these are vertified, troubleshooting efforts switch to the power supply/interface board.

1. Install the 50-pin loopback connector on the TFDC parallel port.

NOTE

Only one loopback connector may be used at a time.

2. Use the DDFLOP ST verb to initiate extended self-test 9. The red FAULT LED extinguishes each time the self-test executes successfully.

3. If errors occur, loop the test with an ST verb and a test code of C009. Use an oscilloscope and the test listing to isolate the control or status fault.

4. Once the parallel logic is verified, remove the 50-pin loopback connector. Ignore the failure indication of the FAULT LED until step 5 is completed.

5. Install the 15-pin remote I/F loopback connector on the TFDC.

6. Observe the FAULT LED, which should extinguish on each successful execution of the self-test.

7. If errors occur, loop on the test (verb ST, test number C009). Use an oscilloscope, TFDC logic drawings, and a test listing to troubleshoot this logic. Refer to the drive interface operating theory and the timing diagrams given in Section 2 (paragraph 2.7.4).

8. Once the TFDC remote interface has been verified, reset the self-test to clear the test loop.

9. Remove the 15-pin loopback connector and reconnect the remote cable to the international chassis. Connect the 50-pin loopback connector to the 50-pin connector on the international chassis.

10. If self-test C009 still fails, check the cables and the power supply interface board.

To troubleshoot the power supply/interface board, loop on verb ST, test number C009.

1. Use an oscilloscope to investigate the control signal demultiplexing logic. Trace the signals through, from YCNTL and ENCNTL (multiplexed serial signals) through DIRR, TESTL-, and back out as ESTAT and YSTAT.

2. Display ENCNTL on scope channel 1 and ESTAT on channel 2 to verify that relative pulse positions are stable.

3. Note that the most likely faults involve the SN74LS123 one-shot devices and associated RC components.

4. Refer back to the power supply/interface board remote i/F theory in Section 2 (paragraphs 2.9,1, 2.10.1) and troubleshoot the timing circuits in detail.

3.4.8 AMPL Testing

An AMPL test and development system provides a window on TFDC operation from the viewpoint of the TMS 9900 microprocessor. The onboard microprocessor (UI038/UEH043) is replaced by a TMS 9900 emulator connector that is controlled from the AMPL system. The emulator has full access and full breakpoint capabilities for any function on the TMS 9900 data bus, memory address bus, or CRU bus. The emulator also has access to encoded interrupt outputs from the TMS 9901 PIA.

An operator may choose to breakpoint operations of the 990 control program ROMs, or to substitute for the ROMs altogether by executing from internal emulator memory. For example, if the control program ROMs are suspect, a known good version of the program could be loaded into emulator memory. If previously observed failures clear up, one or the other ROM is defective.

AMPL may be used with a standard logic analyzer or with an AMPL trace module option. AMPL is particularly useful for faults that are so devastating that the TFDC cannot communicate on the TILINE or execute self-tests.

AMPL has the capability for storing and executing a library of advanced test programs provided by the user. No such "canned" AMPL programs for the TFDC are currently released.

Refer to the following manuals for additional AMPL information:

Model 990 Computer AMPL System Tutorial, 949621-9701

Model 990 Computer AMPL Microprocessor Prototyping System Operation Guide, 946244-9701

3.5 INTERNATIONAL CHASSIS POWER SUPPLY (2261695) TROUBLESHOOTING

These procedures cover the power supply and reset circuitry of the original 2261695 power supply/interface board. The local and remote signal interface circuitry should be tested in a hot mockup with drives, a TFDC board, 990 computer with TILINE bus, and DOCS diagnostic (DDFLOP). Refer back to the TFDC testing procedures.

Skip to paragraph 3.6 for troubleshooting the buffered power supply/interface board 2269977.

Table 3-6 summarizes the checks, adjustments, and troubleshooting procedures for the 2261695 power supply/interface board.

Table 3-6. Maintenance Procedures for 2261695 Power Supply

Procedure	Paragraph
Preliminary Checks	3.5.1
+5-Volt Output Check and Adjustment (no load)	3.5.2.1
+24-Volt Output Check (no load)	3.5.2.2
-12-Volt Output Check (no load)	3.5.2.3
+24-Volt Ripple and Loaded Output Checks	3.5.3.1
+5-Volt Ripple and Loaded Output Checks	3.5.3.2
-12-Volt Ripple and Loaded Output Checks	3.5.3.3
Logic Reset Voltage Level Checks	3.5.4.1
Logic Reset Voltage Trigger and Recovery Checks	3.5.4.2 thru 3.5.4.5
+5-Volt Current Limit Internal Check	3.5.5.1
+5-Volt Regulator (uA723) Internal Gain Check	3.5.5.2
+24-Volt Regulator (uA723) Internal Gain Check	3.5.5.3
+24-Volt Overload Current Limit (Foldback) Check	3.5.6.1
+5-Volt Overload Current Limit (Foldback) Check	3.5.6.2
+5-Volt Overvoltage Crowbar Check	3.5.7

A thorough test of the power supply circuitry requires the test equipment and documentation described in Table 3-7.

CAUTION

Attempts to troubleshoot a defective power supply in a chassis with drives may result in damage to the drive or the drive electronics. Use load resistors, not drives, for testing under loaded conditions.

Table 3-7. Test Equipment and Documentation for 2261695 Power Supply Testing

Item	Part Number
Test Equipment:	
Digital Multimeter	Fluke 8020A or equivalent
Oscilloscope, Dual-trace with calibrated sweep	Tektronix 465 or equivalent
DC ammeter or multimeter (0-10A) optional	Simpson 260 or ammeter
International Chassis (without drives) or test jig made from international chassis transformer, programming plug, ac power module, RFI filter and power wiring harness	
Adjustable Power Supply 0–10 Vdc, 0–10 A with output current meter, adjustable overcurrent protection	
Adjustable load (1–4 A, 100 W) or load resistors for light and normal load testing (see procedures)	
Test resistors: Ohms Watts 0.4 63 1.0 53 1.25 20 1.67 15 2.5 10 3.0 72 5.0 5 12.0 1.2 12.0 48 14.1 41 16.0 36 24.0 25 86.0 2 4.7K 0.5	
Cooling fan	

Table 3-7. Test Equipment and Documentation for 2261695 Power Supply Testing (Continued)

Item	Part Number
Documentation:	
Assembly drawing, List of Materials	2261695, LM2261695
Schematic	2265018

3.5.1 Preliminary Checks

Perform the following preliminary checks:

1. Carefully examine the board for physical defects including:
   a. Bent connector pins
   b. Broken component leads
   c. Hairline cracks, solder bridges, or other defects in printed circuit traces
   d. Discolored or burned areas on the board
   e. Bulging or leaking capacitors
2. Use the multimeter to check continuity across fuse F1

3.5.2 Basic No-Load Checks and Troubleshooting with Ac Inputs

These basic checks verify the presence and voltage tolerances of the +5-volt, +24-volt, and -12-volt dc outputs under no-load conditions.

These checks require a test setup that is equivalent to normal use of the power supply. Use an international chassis (without drives) or a special test rig made from the power components of the international chassis.

Disconnect any drive unit ac or dc power cables from the unit under test. Do not connect dummy loads for this portion of the test.

Disconnect all 115-Vac cables from the segment of the board marked HIGH VOLTAGE. Provide an external cooling fan or jumper the chassis blower to the 115-Vac output of the power transformer.

WARNING

Use insulating tape to tape over the 115-Vac output connector of the international chassis wiring harness and any 115-Vac jumpers provided. This prevents an unnecessary shock hazard.

WARNING

Fault currents may cause defective components, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, smoke, burnt smell or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

NOTE

The following procedures suggest possible causes for observed faults, but do not attempt to exhaust every possibility. Refer to the schematic drawing to follow the logic of the checks and to determine other fault possibilities.

3.5.2.1 + 5-Volt Output Check and Adjustment. This adjustment is performed under no-load conditions, with all low-voltage ac inputs applied to the UUT. Perform the adjustment as follows:

1. Verify that the power programming plug is wired to select the correct transformer taps for 115 Vac operation.
2. Verify ac power is off, and connect the low-voltage ac inputs from the transformer to P6 of the unit under test.
3. Connect the DMM to measure the + 5-volt output of the UUT:
   a. DMM negative (-) lead to logic ground (TP3)
   b. DMM positive (+) lead to 5-volt test point (TP2)
4. Turn on ac power and allow 2 minutes for device warmup.
5. Adjust potentiometer R74 for a measured voltage of + 5.000 Vdc. The allowable range for this adjustment is 4.875 to 5.125 Vdc. This is 5.000 ± 2.5 percent.
6. If this adjustment cannot be performed within tolerance, the possible causes include:
   a. Defective test setup
   b. Ac input voltages incorrect
   c. Defective bridge rectifier CR10
   d. Fuse F1 blown
   e. Crowbar triggered due to overvoltage output or crowbar fault or transient
   f. Value shift in resistive divider networks

g. "Dead spot" or other defect in R74

h. Internal 12-Vdc regulator/op amp power supply voltage (Vcc*) inaccurate

i. Defective current limit operational amplifier section U15-1

j. Defective uA723 regulator device U14

k. Defective series-pass transistor Q10

l. Open current sensing resistor, R59.

7. Investigate and repair this problem before attempting to proceed, as the 24-volt power supply output is based on the 5-volt adjustment. It may be helpful to apply a light load to the output, in order to better judge the operation of series-pass transistor Q10. A 2.5 ohm, 10 W resistor will provide a 2 A load.

3.5.2.2 +24-Volt Output Check. If the previous adjustment is performed correctly, measure the +24 Vdc output as follows:

1. Set the DMM range to a 30-volt scale.

2. Verify that the DMM negative lead is connected to logic ground and move the DMM positive lead to TP4. The allowable range for this voltage is 24.0 ±5% (22.8 to 25.2 Vdc).

NOTE

The +24-volt supply voltage is adjusted by the +5-volt power supply adjustment. This measurement is not valid unless the +5-volt adjustment is performed within the specified limits.

3. If the +24-volt output is out of range, the fault may be one of the following:

a. Defective bridge rectifier CR9

b. Incorrect ac input to bridge rectifier

c. Defective zener diode, CR6

d. Voltage follower U15-7 with nonunity gain

e. Open current-sensing resistor R57 (in return line)

f. Defective current limiter operational amplifier, U15-14

g. Defective uA723 regulator device U16

h. Defective driver transistor Q3 or series-pass transistor Q9

i. Value shift in resistive voltage divider networks.

4. Investigate and repair any defects detected during this procedure. It may be helpful to apply a light load (1 A) to the 24-volt output. This will give more insight into the current handling capability of the rectifier bridge and the series-regulator circuits. A 24 or 25 ohm, 25W resistor is a satisfactory load for this check.

5. Upon successful repair of a fault, return to the previous procedure and repeat the 5-volt and 24-volt checks (in order).

3.5.2.3 -12-Volt Output Check.

1. Connect the DMM positive lead to logic ground (TP3) and the negative lead to TP1.

2. Measure the nominal -12 Vdc output at TP1 (-) and TP3 (ground). This voltage should be in the range between -12.7 and -11.3 Vdc. Note that the -12-volt output is independent of the +5-volt and +24-volt outputs.

3. If this voltage is out of range, the fault possibilites include:

   a. Shorted CR1 or short in bridge rectifier CR11

   b. Defective voltage regulator Q1

   c. Shorted or leaky capacitor C17, C20, or C21

   d. Transformer fault

3.5.3 No-Load/Normal Load Ripple and Loaded Output Checks

These procedures check no-load ripple, verify the output voltage levels under loaded conditions, and check ripple under normal load. A failure of dc output (such as crowbar triggering under normal load) must be cleared before the ripple checks can be properly completed.

Although these measurements are performed with a DMM set to read ac voltage, an oscilloscope is very helpful in troubleshooting excessive ripple.

3.5.3.1 +24-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 10 millivolts and loaded ripple less than 100 millivolts under 1.6 A load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.

2. Set the DMM for 2 Vac full scale and connect the leads as follows (polarity required for step 10):

   Negative lead TP3 (logic ground)

   Positive lead TP4 (+24 Vdc)

CAUTION

Make sure the meter is set up for ac measurements before selecting the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.

4. The no-load ripple should be less than 10 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check)

5. Turn off ac power. Connect a 1.6 A load (15 ohm, 40W) to the +24-volt output pins, using insulated, twisted leads.

6. Turn on ac power and measure the ac ripple again.

7. The loaded ripple level should be less than 100 millivolts. Record the ripple level if unsatisfactory.

8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Capacitor C16, high equivalent series resistance (ESR). Test by connecting new capacitor of same rating in parallel with on-board capacitor while monitoring output ripple on oscilloscope.

   d. Bad bypass, C28. Check as in previous item.

   e. Capacitor C18, high ESR. Check in same manner as C16.

NOTE

The negative lead of C18 is connected to the 24-volt rectifier bridge return (+ V2RTN), not to logic ground.

f. Capacitor C24 (high ripple on Vcc* regulator supply).

NOTE

Ripple on the + 24-volt supply can induce ripple on the + 5-volt supply, as the 12 Vdc internal regulator power (Vcc*) is derived from the + 24-volt line.

9. It may be helpul to proceed to the + 5-volt and -12-volt ripple checks to determine the extent of a ripple problem. Use the oscilloscope to determine if the ripple frequency is 120 Hz (characteristic of bridge rectifier circuits) or 60 Hz (characteristic of stray pickup or induction from transformer).

10. Disconnect one DMM input lead and change the DMM scale to + 30 Vdc. Verify the lead polarity and measure the dc output voltage. The output should be in the range betweeen + 22.8 and + 25.2 volts.

11. If the dc voltage is out of range, troubleshoot + 24-volt regulator circuitry. Suspect the following:

    a. Premature current foldback of + 24-volt supply

    b. Other 24-volt regulator circuits (Refer back to fault list in corresponding no-load output check)

    c. Rectifier bridge CR9 (high internal resistance)

    d. Series-pass transistor Q9 (high internal resistance)

3.5.3.2 + 5-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 20 millivolts and loaded ripple less than 50 millivolts under 3 A load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.

2. Set the DMM for 2 Vac full scale and connect the leads to test points TP2 and TP3 as follows (polarity required for step 10):

   Negative lead TP3 (logic ground)

   Positive lead TP2

CAUTION

Make sure the meter is set up for ac measurements before setting to the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.

4. The no-load ripple should be less than 20 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check).

5. Turn off ac power. Connect a 3.0 A load (1.67 ohm, 5 W) to the + 5-volt output pins, using insulated, twisted leads.

6. Turn on ac power and measure the ac ripple again.

7. The loaded ripple level should be less than 50 millivolts. Record the ripple level if unsatisfactory.

8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Capacitor C15, high ESR (test by connecting new capacitor of same rating in parallel with on-board capacitor while monitoring output ripple on oscilloscope)

   d. Bad bypass, C29. Check as in previous item.

   e. Capacitor C19, high ESR

   f. Capacitor C24 (high ripple on Vcc* regulator supply)

   g. Capacitor C16 (high ripple on Vcc* regulator supply from 24-volt supply)

9. If problem is not cleared, proceed to investigate ripple problems on + 24-volt supply as well as the + 5-volt supply. Although it is unlikely that the -12 Vdc supply is causing the ripple problem, proceeding to that check will determine the extent of the ripple problem.

10. Disconnect one lead of the DMM and set the range to read 5 Vdc. Verify polarity and reconnect the lead. The dc output voltage should be between + 4.875 and + 5.125 Vdc.

11. If the output voltage is not within range, suspect the following:

    a. Premature foldback of + 5-volt supply

    b. Crowbar circuit triggered by transient or fault

    c. Bridge rectifier CR10 (high internal resistance)

    d. Other regulator circuits (refer back to fault list in no-load procedure)

12. Recheck ripple after clearing an output fault

3.5.3.3 – 12-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 10 millivolts and loaded ripple less than 22 millivolts under a 140 milliampere load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.

2. Set the DMM for 2 Vac full scale and connect the leads as follows (Polarity required for step 10):

   Positive lead TP3 (logic ground)

   Negative lead TP1

CAUTION

Make sure the meter is set up for ac measurements before setting to the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.

4. The no-load ripple should be less than 10 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check).

5. Turn off ac power. Connect a 140 milliampere load (86 ohm, 2 W) to the -12-volt output pins, using insulated, twisted leads.

6. Turn on ac power and measure the ac ripple again.

7. The loaded ripple level should be less than 22 millivolts. Record the ripple level if unsatisfactory.

8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Filter capacitor C17, high ESR

   d. Filter capacitor C20 or C21, high ESR

   e. Ripple on logic ground

9. Troubleshoot and repair ripple problems before proceeding to reset checks.

10. Disconnect one of the DMM input leads and change the scale to 15 Vdc. Verify lead polarity and measure the output voltage. The output voltage should fall in the range between -11.3 and -12.7 volts. If not, suspect the three-terminal regulator device, Q1.

11. Recheck the ripple after clearing any fault on the loaded output.

3.5.4 Power Supply Logic Reset Checks

Operational amplifier section U15-8, R40, C22, transistors Q5 through Q8 and Q11 develop a TTL-compatible reset signal for the remote interface logic. The logic reset signal (RESET-) should go active (low) as either the + 5-volt or + 24-volt output drops below limits. The reset signal should remain low for a specified period after all power is restored, to assure a proper reset to the remote I/F logic.

NOTE

A dc-coupled dual trace oscilloscope is necessary for these checks.
A two-channel counter is convenient but not required.

3.5.4.1 Logic Reset Voltage Level Checks. These checks verify that the active and inactive levels of the RESET- signal are TTL-compatible voltages. Perform these checks as follows:

1. Verify ac power off.
2. Connect nominal loads to UUT outputs:
   a. +5 volt 2 A (2.5 ohm, 5 W)
   b. +24 volt 1 A (24 ohm, 25 W)
   c. -12 volt 100 mA (120 ohm, 1.2 W)
3. Apply ac power and allow 15 seconds to stabilize.
4. Use the DMM to measure the RESET- voltage across R76. This voltage may also be measured (with respect to logic ground, TP3) at U11-2.
5. Verify that the RESET- output voltage is between +3.8 and +4.6 Vdc, which corresponds to a TTL 1 (high).
   a. If the RESET- voltage is in the 0- to 1-volt range, use the DMM to verify that the +5 and +24-volt outputs are present and in specified limits (see individual tests for limits).
   b. If the RESET- voltage is just slightly out of range, suspect high leakage or a short in C22, a value shift in the resistive biasing networks, or a low beta transistor.
6. Turn off ac power, and jumper a 4.7 kilohm resistor across R55 (3.83 kilohm). When ac power is restored the resistor will imbalance the +24-volt regulator, and force an undervoltage output of approximately 13.2 Vdc on the +24-volt output. This error should trigger the RESET- circuit.
7. Turn on ac power and verify undervoltage at the +24-volt output. Measure the RESET- voltage as in the previous step. The active RESET- voltage should be in the range from 0.0 to +0.5 volts. Record the reading if it is in error.
8. Remove the jumper resistor from R55.
9. An out of range reading for the active RESET- level may be due to:
   a. Faulty op amp stage U15-8 (high resistance in output stage)
   b. CR2 defective
   c. Value shift in resistive biasing networks
   d. Defective (low beta) transistor

3.5.4.2 Logic Reset Trigger on 24-Volt Undervoltage. This check removes ac power from a lightly loaded supply and verifies that RESET- goes low at least 2 milliseconds before the power supply output drops below +21.6 Vdc.

1. Verify all loads connected as in previous check and jumper resistor removed. Set up oscilloscope to monitor RESET- on channel A and the +24-volt test point (TP4). Set the sweep to trigger on negative transitions of RESET- at 2.2 Vdc. It may be necessary to perform the next step several times to get a good sweep and an accurate measurement. Set up the time base for 1 millisecond per division.

2. Apply ac power and allow outputs to stabilize. Turn off ac power and verify that the RESET- transition (measured at 2.2-volt point) occurs at least 2 milliseconds before the 24 Vdc level drops to 21.6 Vdc. Repeat as necessary for a good reading.

3. Possible causes for a fault include:

   a. CR3 defective

   b. Resistive divider network (R35, R36, R41) error

   c. CR2 defective

   d. Resistive biasing network error

   e. Transistor with low beta

   f. Defective amplifier stage U15-1 (insufficient current sinking)

3.5.4.3 Logic Reset Recovery from 24-Volt Undervoltage. This check makes sure that the reset remains low for at least 20 milliseconds after the 24-volt supply rises to 21.6 Vdc. Perform this check as follows:

1. Use the previous test connections and loads. Trigger the oscilloscope sweep from the rising transition of the 24-volt supply. Set up the sweep for 5 milliseconds per division. It may be necessary to repeat the next step several times to get a good sweep and an accurate reading.

2. Apply ac power, and measure the time between the 21.6-volt point on the rising power supply output and the 2.2-volt level on the rising RESET- signal. The time delay should be 20 milliseconds minimum.

3. If the delay is shorter than 20 milliseconds, suspect:

   a. CR2 shorted or leaky

   b. CR3 shorted

   c. R40 value shift

d. Defective amplifier stage U15-8 (short to Vcc*)

e. Value shift of resistive divider network (R35, R36, R41)

3.5.4.4 Logic Reset Trigger on 5-Volt Undervoltage. This check removes ac power from a lightly loaded supply and verifies that RESET- goes low at least 2 milliseconds before the power supply output drops below +4.5 Vdc.

1. Verify all loads connected as in previous check and jumper resistor removed. Set up oscilloscope to monitor RESET- on channel A and the 5-volt test point (TP2). Set the sweep to trigger on negative transitions of RESET- at 2.2 Vdc. It may be necessary to perform the next step several times to get a good sweep and an accurate measurement. Set up the time base for 1 millisecond per division.

2. Apply ac power and allow outputs to stabilize. Turn off ac power and verify that the RESET- transition (measured at 2.2-volt point) occurs at least 2 milliseconds before the 5 Vdc level drops to 4.5 Vdc. Repeat as necessary for a good reading.

3. Possible causes for a fault include:

   a. CR3 defective

   b. Resistive divider network (R36, R41) error

   c. CR2 defective (open)

   d. Resistive biasing network error

   e. Transistor with low beta

   f. Defective amplifier stage U15-1 (insufficient current sinking)

3.5.4.5 Logic Reset Recovery from 5-Volt Undervoltage. This check makes sure that the reset remains low for at least 20 milliseconds after the 5-volt supply rises to 4.5 Vdc. Perform this check as follows:

1. Use the previous test connections and loads. Trigger the oscilloscope sweep from the rising transition of the 5-volt supply. Set up the sweep for 5 milliseconds per division. It may be necessary to repeat the next step several times to get a good sweep and an accurate reading.

2. Apply ac power, and measure the time between the 4.5-volt point on the rising power supply output and the 2.2-volt level on the rising RESET- signal. The time delay should be 20 milliseconds minimum.

3. If the delay is shorter than 20 milliseconds, suspect:

   a. CR2 shorted or leaky

   b. CR3 shorted

c. R40 value shift

d. Defective amplifier stage U15-8 (short to Vcc*)

e. Value shift of resistive divider network (R35, R36, R41)

3.5.5 Internal Gain and Current Limit Checks

These are optional diagnostic checks of the regulation and current limit circuitry. They may be omitted for a supply that has been observed to properly regulate voltage and to foldback during overcurrent conditions.

3.5.5.1 + 5-Volt Current Limit Internal Check. This is an internal check of the current foldback circuitry. It does not involve the crowbar or application of an external overload. Perform the check as follows:

1. Use the ac input connections of the previous test setup.

2. Turn off ac power, and allow 15 seconds for capacitors to discharge.

3. Connect the DMM to the + 5-volt output, negative lead to logic ground (TP3) and positive lead to the 5-volt test point (TP2).

4. Use a jumper to short the inverting input of the current limiter operational amplifier to ground (U15-2 to ground).

5. Apply ac power and measure the output voltage. The short should cause the op amp to drive the uA723 internal shunt transistor into conduction, in turn causing Q10 to shut off. The output voltage in this current-limiting mode should be in the range 0 to + 1.0 volt.

6. If the output voltage exceeds the allowable value, suspect the following:

   a. Inadequate gain in operational amplifier section U15-1

   b. Defective uA723 regulator device U14

   c. Defective (shorted or low beta) series-pass transistor Q10

   d. Open (or value shift) in resistor R60

   e. Short (or value shift) in resistor R61.

7. Investigate and repair any defects detected during this check. A variable external load may be useful in investigating the problem, after the U15-2 short is removed. After clearing the problem, verify that the U15-2 shorting jumper is removed, then go back to the 5-volt adjustment procedure and restart the checks.

8. Upon successful completion of this check, remove the shorting jumper from the board.

CAUTION

Inadvertantly leaving the shorting jumper in place may lead to unnecessary replacement of components when other checks fail. Verify that the jumper is removed before proceeding.

3.5.5.2 + 5-Volt Regulator (uA723) Internal Gain Check. This is an internal check of the ability of the uA723 device to control the dc output voltage.

1. Use the ac power setup from the previous checks.
2. Turn off ac power and connect the DMM leads to the 5-volt test points as in the previous check.
3. Allow about 30 seconds for capacitor discharge and install a shorting jumper from the uA723 noninverting input U14-5 to ground.
4. Turn on ac power and read the voltage on the DMM. The shorting jumper unbalances the uA723 internal voltage regulation amplifier, and the uA723 cuts off Q10. The output voltage (TP2 to TP3) should be less than 1.0 Vdc under these imbalanced conditions.
5. If the voltage is out of range, the fault may be:
   a. Resistor R62 open
   b. Defective uA723 device U14
   c. Resistor R71 open
   d. Defective series-pass transistor Q10 (shorted or low beta).
6. Investigate and repair any faults detected before proceeding. A variable load may be helpful if the shorting jumper is removed. Once the defect is repaired, remove the shorting jumper and restart the ac procedures at the 5-volt adjustment.
7. If this check passes, remove the jumper and proceed to the next check.

3.5.5.3 + 24-Volt Regulator (uA723) Internal Gain Check. This procedure checks the ability of uA723 regulator device U16 to control the 24-volt output.

1. Turn off ac power. Use the ac power connections from the previous checks.
2. Connect the DMM leads to measure the + 24-volt output between logic ground (TP3) and the 24-volt test point (TP4).
3. Connect alligator clips to a 4.7-kilohm resistor and jumper the resistor in parallel with R55 (3.83 kilohm).
4. Apply ac power to the circuit and read the DMM. Remove power upon obtaining a stable reading. This voltage should be approximately 13.2 Vdc.

5. Remove the resistive jumper.

6. If the resistive jumper did not significantly lower the output voltage, the uA723 is not capable of regulating the output voltage. Possible causes for this fault include:

   a. Defective uA723 regulator U16

   b. Defective regulator driver transistor Q3

   c. Defective series-pass transistor Q9 (low beta or internal short)

   d. Resistive value change in voltage divider networks R44, R53, R55, R56.

7. A variable load on the 24-volt output may be helpful in troubleshooting a fault detected during this test. Do not go on to the next check until any failure is corrected and this check is performed successfully.

3.5.6 Detailed Checks Under Normal Load and Overload with Ac Inputs

These checks under loaded and overloaded conditions require the same ac power inputs as the previous checks. A cooling fan should be provided, as significant amounts of heat are dissipated during these tests.

CAUTION

Do not use drives as power supply loads for suspected or known defective units.

WARNING

These checks involve application of heavy currents to external loads. Such currents may cause defective components in the UUT, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, smoke, burnt smell or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

WARNING

Some of these tests involve significant overload to the power supply. Be careful not to touch high-dissipation components, as a painful burn could result. High-dissipation components include heatsinks, the cases of any transistors mounted on heatsinks (especially Q9, Q10), and the load resistors.

CAUTION

Use a cooling fan to keep a continuous flow of air across the heatsink fins and the load resistors. Overheating may cause failures where none previously existed.

3.5.6.1 +24-Volt Overload Current Limit (Foldback) Check. This procedure checks the ability of the 24-volt supply to protect against overloads by reducing the output voltage.

CAUTION

Overloads should be applied for the minimum time required to obtain a reading from previously-connected test probes. Do not leave power applied while meditating upon test results.

Perform this check as follows:

1. Turn off ac power.
2. Connect the DMM leads to measure the +24-volt output, negative lead to logic ground (TP3), positive lead to the 24-volt test point (TP4).
3. Set the adjustable dummy load to maximum resistance and connect the dummy load to the 24-volt outputs, P11-2 (logic ground) and P11-1 (+24 Vdc).
4. Turn on ac power.
5. Record the DMM measurement at each of the following loads:
   a. 1.0 A (24 ohm, 24 W dissipation)
   b. 1.5 A (16 ohm, 36 W dissipation)
   c. 2.0 A (12 ohm, 48 W dissipation)
   d. 2.2 A (11 ohm, 52.8 W dissipation)
6. Turn off ac power.
7. All of the recorded readings should fall in the range from +22.8 to +25.2 Vdc. If all the readings are out of range by the same amount, there may be an offset error in the 24-volt regulator circuitry. If the voltage drops significantly (by a volt) as the loading increases, the power supply is current limiting prematurely. Either type of fault should be investigated and repaired before proceeding. Go back to the beginning of this procedure after any such repair.
8. Verify ac power off and DMM connected to measure 24-volt output as in previous steps. Verify previous checks passed.

9. With 11-ohm (2.2 A) load connected, turn on ac power and read DMM.

10. Turn off ac power. If the reading from the previous step is not in the range between +22.8 and +25.2 volts, some defect has prevented the power supply from coming on while under load. Investigate and repair any faults before proceeding. After any repair, return to the beginning of this procedure.

11. Possible causes for the power supply not coming up under load include:

    a. Rectifier bridge CR9 (high internal resistance)

    b. Premature foldback — possible value shift of resistor R57

    c. Regulator transistors Q3, Q9

    d. Resistive value shifts in regulator/current limiter amplifier input voltage dividers.

NOTE

The +24-volt return of the rectifier bridge (+V2RTN) is isolated from logic ground (also output circuit return) by current-sensing resistor R57. The effect of this difference increases with increasing load current.

12. Verify ac power is off. Connect a 3 A load (8 ohm, 72 W) to +24-volt output. This overload represents 136 percent of rated maximum load.

CAUTION

This overload will cause high dissipation in the output transistors, especially if the foldback current limiting should fail. Do not leave the power supply turned on under this overload for more than 30 seconds at a time.

13. Turn on ac power. Record DMM measurement as soon as conditions stabilize, then turn off ac power.

14. The overload should have caused the 24-volt supply to go into the current limiting (foldback) mode, with reduced output voltage. The voltage reading should be in the range +11.0 to +17.0 Vdc.

15. Investigate and repair if the foldback does not occur. Fault possibilities include:

    a. Value shift in current sensing resistor R57

    b. Dc offset or insufficient gain in current limiter op amp U15-14.

c. Bias point shift on U15 due to value shift by resistor R38

d. Low internal regulator supply voltage (Vcc*)

e. Regulator driver Q3 defective (low beta)

f. Series-pass transistor Q9 defective (shorted, open base, or low beta)

g. Short to from C18 negative lead to logic ground.

16. Induce current limiting again by turning on ac power while overload is connected. After verifying the foldback, shut off power, immediately remove load and turn on ac power. Verify that the output voltage returns to the nominal +22.8- to +25.2-volt range.

17. If the voltage remains low, the power supply never recovered from the foldback condition. Investigate fault possibilities and repair.

3.5.6.2 +5-Volt Overload Current Limit (Foldback) Check. The concept of this test is identical to that of the +24-volt overload current limit check. This check is somewhat more comprehensive than the +5-volt current limit internal check.

CAUTION

Overloads should be applied for the minimum time required to obtain a reading from previously-connected test probes. Do not leave power applied while meditating upon test results.

1. Verify ac power is off. Connect the DMM to read the 5-volt output, negative lead to logic ground (TP3), positive lead to 5-volt output (TP2).

2. Set adjustable load to maximum resistance (minimum current) and connect to 5-volt output, negative lead to P11-2, positive lead to P11-5. Polarity is not important for a resistive (passive) load.

3. Turn on ac power.

4. Record the DMM measurement at each of the following loads:

   a. 1.0 A (5.0 ohm, 5 W)

   b. 2.0 A (2.5 ohm, 10 W)

   c. 3.0 A (1.67 ohm, 15 W)

   d. 4.0 A (1.25 ohm, 20 W)

5. Turn off ac power. All DMM readings from the previous step should be in the range +4.875 to +5.125 Vdc. If all the readings are out of range by the same amount, there may be an offset error in the 5-volt regulator circuitry. If the voltage drops significantly (by 0.5 volt) as the loading increases, the power supply is current limiting prematurely. Another fault possibility is an incorrect crowbar trigger. Either type of fault should be investigated and repaired before proceeding. Go back to the beginning of this procedure after any such repair.

6. Normal load fault possibilites include:

   a. Rectifier bridge CR10 (high internal resistance)

   b. Current-sensing resistor R59 value shift

   c. Defective series-pass transistor Q10 (high internal resistance)

7. Verify ac power off. Connect a 12.5 A load (0.4 ohm, 62.5 W) to the 5-volt outputs. This overload represents slightly more than 300 percent of rated load current. Verify that the DMM leads are properly positioned to measure the 5-volt output (TP2-TP3).

8. Turn on ac power and read the DMM when conditions stabilize (less than 30 seconds). Turn off ac power.

9. The overload should have induced an output voltage reduction (foldback). The voltage read in the previous step should be in the range +1.5 to +3.5 Vdc.

10. If the output voltage did not foldback to the specified range, investigate and repair the board. Fault possibilities include:

    a. Value shift in current sensing resistor R59

    b. Value shift in resistive dividers

    c. Dc offset or insufficient gain in current limiter op amp U15-1

    d. Deadband in current limiter op amp U15-1

    e. Low internal regulator supply voltage (Vcc*)

    f. Series-pass transistor Q10 defective (shorted, open base, or low beta)

    g. Defective uA723 regulator device U14.

WARNING

Do not leave power supply on under overcurrent conditions for periods of more than 30 seconds, to reduce the possibility of a component explosion or component failure induced where no fault previously existed.

11. Induce current limiting again by turning on ac power while overload is connected. After verifying the foldback, shut off power, immediately remove load and turn on ac power. Verify that the output voltage returns to the nominal +4.9- to +5.1-volt range.

12. If the voltage remains low, the power supply never recovered from the foldback condition. Investigate fault possibilities and repair.

3.5.7 +5-Volt Overvoltage Crowbar Check

This check requires a heavy-duty lab supply that is adjustable from 0 to +10 Vdc, with a current meter and adjustable current limiting up to 10 amperes.

The crowbar check determines whether the crowbar circuit is capable of protecting the load circuit from overvoltage conditions on the +5-volt output line. The check also detects short circuits on the output side of series-pass transistor Q10.

WARNING

This check involves application of heavy currents. Such currents may cause defective components, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

Check the crowbar circuit as follows:

1. Disconnect the low voltage 7.5-Vac input to the unit under test.

2. Remove the logic ground to chassis ground shorting jumper (E6-E7) if installed.

3. Adjust R74 fully counterclockwise.

CAUTION

This step deliberately misadjusts the power supply output voltages. Do not return to service without performing the +5-volt adjustment procedure of paragraph 3.5.2.1 on the unit under test (UUT).

4. Adjust the overcurrent limit on the lab power supply to 7 amperes at 6.8 volts, and then reduce the output voltage to zero.

5. Turn off the lab power supply, and connect the lab power supply outputs to unit under test as follows:

   a. Positive (+) lead to P11-5 (UUT +5-volt output)

   b. Negative (-) lead to P11-6 (UUT logic ground)

6. Connect the DMM across Q2, with positive lead to the cathode (TP2) and negative lead to the anode (logic ground TP1). Set up the DMM to read dc voltages, 10 Vdc full scale.

NOTE

The following steps require the technician to increase the dc voltage applied to the UUT + 5-volt output, while monitoring the current meter for a sudden increase. The voltage just prior to the current surge is the trigger point of the crowbar circuit. This voltage trigger point is to be recorded. It may be necessary to repeat these steps several times to accurately determine the trigger point.

7. Turn on the lab power supply.

8. Gradually increase the lab power supply output voltage from 0 volts toward + 6.9 volts, while monitoring for a current surge. Upon occurrence of the current surge (crowbar trigger point), reduce the lab power supply output to 0 volts. Upon reaching + 6.9 volts without any discernible current increase, reduce the output voltage to zero volts.

9. Record the DMM voltage measurement at the crowbar trigger point. Repeat the previous step as necessary to get a reading or determine that the crowbar is not functioning.

10. Turn off the lab power supply. The trigger point voltage should be between + 5.3 volts and + 6.8 volts. The possibilities include:

    a. Output current increased linearly with increasing input voltage, at least up to the overcurrent limit set on the lab power supply. This indicates a short from the + 5-volt line to ground, or else the crowbar is always on. A short is not necessarily in the crowbar circuit. Fault possibilities include C19, triac trigger control transistor Q4, zener diode CR4, triac Q2, or a solder bridge. If the crowbar is always on, or comes on at a very low voltage, the fault may be in Q4, R48, R49, R50, R63, or CR4.

    b. Output current remained low over the entire 0–6.8 volt range. This indicates that the triac never triggered. Fault possibilities include zener CR4 open, Q4 open, C30 shorted, defective resistor, or Q2 defective.

    c. Triac triggered between 0.5 and 6.2 volts. Fault possibilities include Q4 or resistance value shift in voltage divider and biasing resistors R50, R63, R48, R49. Other possibilities include Q2 or CR4 shorted.

11. If this check fails, investigate and repair defect. Repeat the check.

12. The power supply is misadjusted at this point. Readjust the + 5-volt output and recheck the + 24-volt output before returning the unit to service.

3.6 BUFFERED INTERNATIONAL CHASSIS POWER SUPPLY (2269977) TROUBLESHOOTING

These procedures cover the power supply and reset circuitry of the buffered 2269977 power supply/interface board. The local and remote signal interface circuitry should be tested in a hot mockup with drives, a TFDC board, 990 computer with TILINE bus, and DOCS diagnostic (DDFLOP). Refer back to the TFDC testing procedures.

Refer back to paragraph 3.5 for troubleshooting the original power supply/interface board 2261695.

Table 3-8 summarizes the checks, adjustments, and troubleshooting procedures for the 2269977 power supply/interface board.

Table 3-8. Maintenance Procedures for 2269977 Power Supply

Procedure	Paragraph
Preliminary Checks	3.6.1
+5-Volt Output Check and Adjustment (no load)	3.6.2.1
+24-Volt Output Check(no load)	3.6.2.2
-12-Volt Output Check (no lead)	3.6.2.3
+24-Volt Ripple and Loaded Output Checks	3.6.3.1
+5-Volt Ripple and Loaded Output Checks	3.6.3.2
-12-Volt Ripple and Loaded Output Checks	3.6.3.3
Logic Reset Voltage Level Checks	3.6.4.1
Logic Reset Voltage Trigger on 5-Volt Undervoltage	3.6.4.2
Logic Reset Recovery from 5-volt from 5-Volt Undervoltage	3.6.4.3
+5-Volt Regulator (uA723) Internal Gain Check	3.6.5.1
+24-Volt Regulator (uA723) Internal Gain Check	3.6.5.2
+24-Volt Overload Current Limit (Foldback) Check	3.6.6.1
+5-Volt Overload Current Limit (Foldback) Check	3.6.6.2
+5-Volt Overvoltage Crowbar Check	3.6.7

A thorough test of the power supply circuitry requires the test equipment and documentation described in Table 3-9.

CAUTION

Attempts to troubleshoot a defective power supply in a chassis with drives may result in damage to the drive or the drive electronics. Use load resistors, not drives, for testing under loaded conditions.

Table 3-9. Test Equipment and Documentation for 2269977 Power Supply Testing

Item	Part Number
Test Equipment:	
Digital Multimeter	Fluke 8020A or equivalent
Oscilloscope, Dual-trace with calibrated sweep	Tektronix 465 or equivalent
DC ammeter multimeter (0-10 optional)	Simpson 260 or ammeter
International Chassis (without drives) or test jig made from international chassis transformer, programming plug, ac power module, RFI filter and power wiring harness	
Adjustable Power Supply 0–10 Vdc, 0–10 A with output current meter, adjustable overcurrent protection (for crowbar check)	
Adjustable load (1-4 A, 100 W) or load resistors for light and normal load testing (see procedures)	
Test resistors: Ohms Watts 0.4 63 1.0 53 1.25 20 1.67 15 2.5 10	

Table 3-9. Test Equipment and Documentation for 2269977 Power Supply Testing (Continued)

Item	Part Number
Test resistors: Ohms Watts 3.0 72 5.0 5 12.0 1.2 12.0 48 16.0 36 86.0 2 4.7K 0.5	
Cooling fan	
Documentation:	
Assembly drawing, List of Materials	2269977, LM2269977
Schematic	2269979

3.6.1 Preliminary Checks

Perform the following preliminary checks:

1. Carefully examine the board for physical defects including:
   a. Bent connector pins
   b. Broken component leads
   c. Hairline cracks, solder bridges, or other defects in printed circuit traces
   d. Discolored or burned areas on the board
   e. Bulging or leaking capacitors
2. Use the multimeter to check continuity across fuses F1 and F2

3.6.2 Basic No-Load Checks and Troubleshooting with Ac Inputs

These basic checks verify the presence and voltage tolerances of the +5-volt, +24-volt, and -12-volt dc outputs under no-load conditions.

These checks require a test setup that is equivalent to normal use of the power supply. Use an international chassis (without drives) or a special test rig made from the power components of the international chassis.

Disconnect any drive unit ac or dc power cables from the unit under test. Do not connect dummy loads for this portion of the test.

Disconnect all 115-Vac cables from the segment of the board marked HIGH VOLTAGE. Provide an external cooling fan or jumper the chassis blower to the 115-Vac output of the power transformer.

WARNING

Use insulating tape to tape over the 115-Vac output connector of the international chassis wiring harness and any 115-Vac jumpers provided. This prevents an unnecessary shock hazard.

WARNING

Fault currents may cause defective components, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, smoke, burnt smell, or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

NOTE

The following procedures suggest possible causes for observed faults, but do not attempt to exhaust every possibility. Refer to the schematic drawing to follow the logic of the checks and to determine other fault possibilities.

3.6.2.1 +5-Volt Output Check and Adjustment. This adjustment is performed under no-load conditions, with all low-voltage ac inputs applied to the UUT. Perform the adjustment as follows:

1. Verify that the power programming plug is wired to select the correct transformer taps for 115-Vac operation.

2. Verify ac power is off, and connect the low-voltage ac inputs from the transformer to P6 of the unit under test.

3. Connect the DMM to measure the +5-volt output of the UUT:

   a. DMM negative (-) lead to logic ground (TP3)

   b. DMM positive (+) lead to 5-volt test point (TP2)

4. Turn on ac power and allow 2 minutes for device warmup.

5. Adjust potentiometer R3 for a measured voltage of +5.000 Vdc. The allowable range for this adjustment is 4.875 to 5.125 Vdc. This is 5.000 ±2.5 percent.

6. If this adjustment cannot be performed within tolerance, the possible causes include:

   a. Defective test setup

   b. Ac input voltages incorrect

   c. Defective bridge rectifier CR4

   d. Fuse F1 blown

   e. Crowbar triggered due to overvoltage output or crowbar fault or transient

   f. Value shift in resistive divider networks

   g. "Dead spot" or other defect in R3

   h. Internal 12-Vdc regulator supply voltage (Vcc*) inaccurate

   i. Defective uA723C regulator device U24

   j. Defective series-pass transistor Q1

   k. Open current sensing resistor, R8

7. Investigate and repair this problem before attempting to proceed, as the 24-volt power supply output is based on the 5-volt adjustment. It may be helpful to apply a light load to the output, in order to better judge the operation of series-pass transistor Q1. A 2.5 ohm, 10 W resistor will provide a 2 A load.

3.6.2.2 + 24-Volt Output Check. If the previous adjustment is performed correctly, measure the + 24 Vdc output as follows:

1. Set the DMM range to a 30-volt scale.

2. Verify that the DMM negative lead is connected to logic ground and move the DMM positive lead to TP4. The allowable range for this voltage is from 22.8 to 25.2 Vdc. This is 24.000 ± 5 percent.

NOTE

The + 24-volt supply voltage is adjusted by the + 5-volt power supply adjustment. This measurement is not valid unless the + 5-volt adjustment is performed within the specified limits.

3. If the + 24-volt output is out of range, the fault may be one of the following:

   a. Defective bridge rectifier CR5

   b. Incorrect ac input to bridge rectifier

c. Defective zener diode, VR1

d. Capacitor C9 shorted or leaky

e. Open current-sensing resistor R31 or R32 (in return line)

f. Defective uA723 regulator device U22

g. Defective driver transistor Q6 or series-pass transistor Q5

h. Value shift in resistive voltage divider networks.

4. Investigate and repair any defects detected during this procedure. It may be helpful to apply a light load (1 A) to the 24-volt output. This will give more insight into the current handling capability of the rectifier bridge and the series-regulator circuits. A 24 or 25 ohm, 25 W resistor is satisfactory for this check.

5. Upon successful repair of a fault, return to the previous procedure and repeat the 5-volt and 24-volt checks (in order).

3.6.2.3 – 12-Volt Output Check.

1. Connect the DMM positive lead to logic ground (TP3) and the negative lead to TP1.

2. Measure the nominal -12 Vdc output at TP1 (-) and TP3 (ground). This voltage should be in the range between -12.7 and -11.3 Vdc. Note that the -12-volt output is independent of the + 5-volt and + 24-volt outputs.

3. If this voltage is out of range, the fault possibilites include:

   a. Shorted CR3 or short in bridge rectifier CR6

   b. Defective voltage regulator Q7

   c. Shorted or leaky capacitor C10 or C11

   d. Transformer fault

3.6.3 No-Load/Normal Load Ripple and Loaded Output Checks

These procedures check no-load ripple, verify the output voltage levels under loaded conditions, and check ripple under normal load. A failure of dc output (such as crowbar triggering under normal load) must be cleared before the ripple checks can be properly completed.

Although these measurements are performed with a DMM set to read ac voltage, an oscilloscope is very helpful in troubleshooting excessive ripple.

3.6.3.1 + 24-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 10 millivolts and loaded ripple less than 100 millivolts under 1.6 A load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.
2. Set the DMM for 2 Vac full scale and connect the leads as follows (polarity required for step 10):

   Negative lead TP3 (logic ground)

   Positive lead TP4 (+24 Vdc)

CAUTION

Make sure the meter is set up for ac measurements before selecting the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.
4. The no-load ripple should be less than 10 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check).
5. Turn off ac power. Connect a 1.6 A load (15 ohm, 40 W) to the +24-volt output pins, using insulated, twisted leads.
6. Turn on ac power and measure the ac ripple again.
7. The loaded ripple level should be less than 100 millivolts. Record the ripple level if unsatisfactory.
8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Capacitor C13, high equivalent series resistance (ESR). Test by connecting new capacitor of same rating in parallel with on-board capacitor while monitoring output ripple on oscilloscope.

   d. Bad bypass, C9. Check as in previous item.

e. Capacitor C7, high ESR. Check in same manner as C13.

f. Capacitor C1 (high ripple on Vcc* regulator supply).

NOTE

Ripple on the + 24-volt supply can induce ripple on the + 5-volt supply, as the 12-volt internal regulator power (Vcc*) is derived from the + 24-volt line.

9. It may be helpful to proceed to the + 5-volt and -12-volt ripple checks to determine the extent of a ripple problem. Use the oscilloscope to determine if the ripple frequency is 120 Hz (characteristic of bridge rectifier circuits) or 60 Hz (characteristic of stray pickup or induction from transformer).

10. Disconnect one DMM input lead and change the DMM scale to + 30 Vdc. Verify the lead polarity and measure the dc output voltage. The output should be in the range between + 22.8 and + 25.2 volts.

11. If the dc voltage is out of range, troubleshoot + 24-volt regulator circuitry. Suspect the following:

    a. Premature current foldback of + 24-volt supply

    b. Other 24-volt regulator circuits (Refer back to fault list in corresponding no-load output check)

    c. Rectifier bridge CR5 (high internal resistance)

    d. Series-pass transistor Q5 (high internal resistance)

3.6.3.2 + 5-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 20 millivolts and loaded ripple less than 50 millivolts under 3 A load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.

2. Set the DMM for 2 Vac full scale and connect the leads to test points TP2 and TP3 as follows (polarity required for step 10):

   Negative lead TP3 (logic ground)

   Positive lead TP2

CAUTION

Make sure the meter is set up for ac measurements before setting to the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.

4. The no-load ripple should be less than 20 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check).

5. Turn off ac power. Connect a 3.0 A load (1.67 ohm, 5 W) to the + 5-volt output pins, using insulated, twisted leads.

6. Turn on ac power and measure the ac ripple again.

7. The loaded ripple level should be less than 50 millivolts. Record the ripple level if unsatisfactory.

8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Capacitor C12, high ESR (test by connecting new capacitor of same rating in parallel with on-board capacitor while monitoring output ripple on oscilioscope)

   d. Capacitor C4, high ESR

   e. Capacitor C1 (high ripple on Vcc* regulator supply)

   f. Capacitor C13 (high ripple on Vcc* regulator supply from 24-volt supply)

9. If problem is not cleared, proceed to investigate ripple problems on + 24-volt supply as well as the + 5-volt supply. Although it is unlikely that the -12 Vdc supply is causing the ripple problem, proceeding to that check will determine the extent of the ripple problem.

10. Disconnect one lead of the DMM and set the range to read 5 Vdc. Verify polarity and reconnect the lead. The dc output voltage should be between + 4.875 and + 5.125 Vdc.

11. If the output voltage is not within range, suspect the following:

    a. Premature foldback of +5-volt supply

    b. Crowbar circuit triggered by transient or fault

    c. Bridge rectifier CR4 (high internal resistance)

    d. Other regulator circuits (refer back to fault list in no-load procedure)

12. Recheck ripple after clearing an output fault

3.6.3.3 -12-Volt Ripple and Loaded Output Checks. This procedure supplies ac input power to the board and verifies no-load ripple less than 10 millivolts and loaded ripple less than 22 millivolts under a 140-milliampere load. The procedure also verifies the output voltage under normal load.

NOTE

Ripple measurements are extremely sensitive to induced errors caused by stray pickup and faulty test setup.

Perform these checks as follows:

1. Verify that ac power is off and remove any external load from the power supply.

2. Set the DMM for 2 Vac full scale and connect the leads as follows (polarity required for step 10):

   Positive lead TP3 (logic ground)

   Negative lead TP1

CAUTION

Make sure the meter is set up for ac measurements before setting to the 2-volt range.

3. Apply ac power and read the DMM. Adjust the scale as necessary to get the desired resolution.

4. The no-load ripple should be less than 10 millivolts. Record the ripple level if unsatisfactory, and proceed to the next step (loaded ripple check).

5. Turn off ac power. Connect a 140 milliampere load (86 ohm, 2 W) to the -12-volt output pins, using insulated, twisted leads.

6. Turn on ac power and measure the ac ripple again.

7. The loaded ripple level should be less than 22 millivolts. Record the ripple level if unsatisfactory.

8. Troubleshoot for ripple problems if either ripple figure is out of limits. In practice, successful troubleshooting for ripple requires an oscilloscope that is sensitive in the 10-millivolt ac range. Possible faults include:

   a. Ground loops in test setup

   b. Leads too close to transformer

   c. Filter capacitor C10 or C11, high ESR

   d. Ripple on logic ground

9. Troubleshoot and repair ripple problems before proceeding to reset checks.

10. Disconnect one of the DMM input leads and change the scale to 15 Vdc. Verify lead polarity and measure the output voltage. The output voltage should fall in the range between -11.3 and -12.7 volts. If not, suspect the three-terminal regulator device, Q1.

11. Recheck the ripple after clearing any fault on the loaded output.

3.6.4 Power Supply Logic Reset Checks

LM339 comparator U23, resistors R15-R22, C6, and transistor Q4 develop a TTL-compatible reset signal for the remote interface logic. The logic reset signal (RESET-) should go active (low) as part of the power supply turnoff procedure. The reset signal should remain low for a specified period after all power is restored, to assure a proper reset to the remote i/F logic.

NOTE

A dc-coupled dual trace oscilloscope is necessary for these checks.
A two-channel counter is convenient but not required.

3.6.4.1 Logic Reset Voltage Level Checks. These checks verify that the active and inactive levels of the RESET- signal are TTL-compatible voltages. Perform these checks as follows:

1. Verify ac power off.

2. Connect nominal loads to UUT outputs:

   a. +5 volt 2 A (2.5 ohm, 5 W)

   b. +24 volt 1 A (24 ohm, 25 W)

   c. -12 volt 100 mA (120 ohm, 1.2 W)

3. Apply ac power and allow 15 seconds to stabilize.

4. Use the DMM to measure the RESET- voltage across R22. This voltage may also be measured (with respect to logic ground, TP3) at U15-5 (SN7414 inverter, logic sheet 2).

5. Verify that the RESET- output voltage is between +3.8 and +4.6 Vdc, which corresponds to a TTL 1 (high).

   a. If the RESET- voltage is in the 0- to 1-volt range, use the DMM to verify that the +5 and +24-volt outputs are present and in specified limits (see individual tests for limits).

   b. If the RESET- voltage is just slightly out of range, suspect a value shift in the resistive biasing networks or a low beta transistor.

6. Turn off ac power, and jumper a 4.7-kilohm resistor across R4 (2.15 kilohm). When ac power is restored the resistor will imbalance the +5-volt regulator, and force an undervoltage output less than 4.5 Vdc on the 5-volt output. This error should trigger the RESET- circuit.

7. Turn on ac power and verify undervoltage at the 5-volt output. Measure the RESET- voltage as in the previous step. The active RESET- voltage should be in the range from 0.0 to +0.5 volts. Record the reading if it is in error.

8. Remove the jumper resistor from R4.

9. An out of range reading for the active RESET- level may be due to:

   a. Faulty comparator U23

   b. Value shift in resistive biasing networks

   c. Defective (low beta) transistor Q4

3.6.4.2 Logic Reset Trigger on 5-Volt Undervoltage. This check removes ac power from a lightly loaded supply and verifies that RESET- goes low at least 2 milliseconds before the regulated power supply output drops below +4.5 Vdc.

1. Verify all loads connected as in previous check and jumper resistor removed. Set up oscilloscope to monitor RESET- on channel A and the 5-volt test point (TP2). Set the sweep to trigger on negative transitions of RESET- at a 2.2 Vdc level. It may be necessary to perform the next step several times to get a good sweep and an accurate measurement. Set up the time base for 1 millisecond per division.

2. Apply ac power and allow outputs to stabilize. Turn off ac power and verify that the RESET- transition (measured at 2.2-volt point) occurs at least 2 milliseconds before the 5 Vdc level drops to 4.5 Vdc. Repeat as necessary for a good reading.

3. Possible causes for a fault include:

   a. U23 defective

   b. Resistive divider network (R13/R14) error

c. Resistor R15 shifted value

d. Resistor networks R16–R19 shifted value or open

e. Resistive biasing network error

f. Transistor with low beta (Q4)

3.6.4.3 Logic Reset Recovery from 5-Volt Undervoltage. This check makes sure that the reset remains low for at least 20 milliseconds after the 5-volt supply rises to 4.5 Vdc. Perform this check as follows:

1. Use the previous test connections and loads. Trigger the oscilloscope sweep from the rising transition of the 5-volt supply. Set up the sweep for 5 milliseconds per division. It may be necessary to repeat the next step several times to get a good sweep and an accurate reading.

2. Apply ac power, and measure the time between the 4.5-volt point on the rising power supply output and the 2.2-volt level on the rising RESET- signal. The time delay should be 20 milliseconds minimum.

3. If the delay is shorter than 20 milliseconds, suspect:

   a. C6 shorted or leaky

   b. R18 value shift

   c. Defective comparator U23

   d. Value shift of resistive divider network (R13, R14)

3.6.5 Internal Gain Checks

These are optional diagnostic checks of the regulation circuitry. They may be omitted for a supply that has been observed to properly regulate voltage and to foldback during overcurrent conditions.

3.6.5.1 + 5-Volt Regulator (uA723) Internal Gain Check. This is an internal check of the ability of the uA723 device to control the dc output voltage.

1. Use the ac power setup from the previous checks.

2. Turn off ac power and connect the DMM leads to the 5-volt test points as in the previous check.

3. Allow about 30 seconds for capacitor discharge and install a shorting jumper from the uA723 noninverting input U24-5 to ground.

4. Turn on ac power and read the voltage on the DMM. The shorting jumper unbalances the uA723 internal voltage regulation amplifier, and the uA723 cuts off Q1. The output voltage (TP2 to TP3) should be less than 1.0 Vdc under these imbalanced conditions.

5. If the voltage is out of range, the fault may be:

   a. Resistor R5 open

   b. Defective uA723 device U24

   c. Defective series-pass transistor Q1 (shorted or low beta)

6. Investigate and repair any faults detected before proceeding. A variable load may be helpful if the shorting jumper is removed. Once the defect is repaired, remove the shorting jumper and restart the ac procedures at the 5-volt adjustment.

7. If this check passes, remove the jumper and proceed to the next check.

3.6.5.2 + 24-Volt Regulator (uA723) Internal Gain Check. This procedure checks the ability of uA723 regulator device U22 to control the 24-volt output.

1. Turn off ac power. Use the ac power connections from the previous checks.

2. Connect the DMM leads to measure the + 24-volt output between logic ground (TP3) and the 24-volt test point (TP4).

3. Connect alligator clips to a 4.7 kilohm resistor and jumper the resistor in parallel with R23 (3.83 kilohm).

4. Apply ac power to the circuit and read the DMM. Remove power upon obtaining a stable reading. This voltage should be approximately 13.2 Vdc.

5. Remove the resistive jumper.

6. If the resistive jumper did not significantly lower the output voltage, the uA723 is not capable of regulating the output voltage. Possible causes for this fault include:

   a. Defective uA723 regulator U122

   b. Defective regulator driver transistor, Q6

   c. Defective series-pass transistor Q5 (low beta or internal short)

7. A variable load on the 24-volt output may be helpful in troubleshooting a fault detected during this test. Do not go on to the next check until any failure is corrected and this check is performed successfully.

3.6.6 Detailed Checks Under Normal Load and Overload with Ac Inputs

These checks under loaded and overloaded conditions require the same ac power inputs as the previous checks. A cooling fan should be provided, as significant amounts of heat are dissipated during these tests.

CAUTION

Do not use drives as power supply loads for suspected or known defective units.

WARNING

These checks involve application of heavy currents to external loads. Such currents may cause defective components in the UUT, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, smoke, burnt smell or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

WARNING

Some of these tests involve significant overload to the power supply. Be careful not to touch high-dissipation components, as a painful burn could result. High-dissipation components include heatsinks, the cases of any transistors mounted on heatsinks (especially Q1, Q5), and the load resistors.

CAUTION

Use a cooling fan to keep a continuous flow of air across the heatsink fins and the load resistors. Overheating may cause failures where none previously existed.

3.6.6.1 +24-Volt Overload Current Limit (Foldback) Check. This procedure checks the ability of the 24-volt supply to protect against overloads by reducing the output voltage.

CAUTION

Overloads should be applied for the minimum time required to obtain a reading from previously connected test probes. Do not leave power applied while meditating upon test results.

Perform this check as follows:

1. Turn off ac power.
2. Connect the DMM leads to measure the +24-volt output, negative lead to logic ground (TP3), positive lead to the 24-volt test point (TP4).

3. Set the adjustable dummy load to maximum resistance and connect the dummy load to the 24-volt outputs, P11-2 (logic ground) and P11-1 (+24 Vdc).

4. Turn on ac power.

5. Record the DMM measurement at each of the following loads:

   a. 1.0 A (24 ohm, 24 W dissipation)

   b. 1.5 A (16 ohm, 36 W dissipation)

   c. 2.0 A (12 ohm, 48 W dissipation)

   d. 2.2 A (11 ohm, 52.8 W dissipation)

6. Turn off ac power.

7. All of the recorded readings should fall in the range from +22.8 to +25.2 Vdc. If all the readings are out of range by the same amount, there may be an offset error in the 24-volt regulator circuitry. If the voltage drops significantly (by a volt) as the loading increases, the power supply is current limiting prematurely. Either type of fault should be investigated and repaired before proceeding. Go back to the beginning of this procedure after any such repair.

8. Verify ac power off and DMM connected to measure 24-volt output as in previous steps. Verify previous checks passed.

9. With 11-ohm (2.2 A) load connected, turn on ac power and read DMM.

10. Turn off ac power. If the reading from the previous step is not in the range between +22.8 and +25.2 volts, some defect has prevented the power supply from coming on while under load. Investigate and repair any faults before proceeding. After any repair, return to the beginning of this procedure.

11. Possible causes for the power supply not coming up under load include:

    a. Rectifier bridge CR5 (high internal resistance)

    b. Premature foldback — possible open in R31 or R32 (parallel)

    c. Regulator transistors Q6, Q5

    d. Resistive value shifts in regulator/current limiter amplifier input voltage dividers.

NOTE

The +24-volt return of the rectifier bridge (+V2RTN) is isolated from logic ground (also output circuit return) by parallel current-sensing resistors R31/R32. The effect of this difference increases with increasing load current.

12. Verify ac power is off. Connect a 3 A load (8 ohm, 72 W) to + 24-volt output. This overload represents 136 percent of rated maximum load.

CAUTION

This overload will cause high dissipation in the output transistors, especially if the foldback current limiting should fail. Do not leave the power supply turned on under this overload for more than 30 seconds at a time.

13. Turn on ac power. Record DMM measurement as soon as conditions stabilize, then turn off ac power.

14. The overload should have caused the 24-volt supply to go into the current limiting (foldback) mode, with reduced output voltage. The voltage reading should be in the range + 11.0 to + 17.0 Vdc.

15. Investigate and repair if the foldback does not occur. Fault possibilities include:

    a. Open in current sensing resistor R31 or R32

    b. Low internal regulator supply voltage (Vcc*)

    c. Regulator driver Q6 defective (low beta)

    d. Series-pass transistor Q5 defective (shorted, open base, or low beta)

16. Induce current limiting again by turning on ac power while overload is connected. After verifying the foldback, shut off power, immediately remove load and turn on ac power. Verify that the output voltage returns to the nominal + 22.8- to + 25.2-volt range.

17. If the voltage remains low, the power supply never recovered from the foldback condition. Investigate fault possibilities and repair.

3.6.6.2 + 5-Volt Overload Current Limit (Foldback) Check. The concept of this test is identical to that of the + 24-volt overload current limit check. This check is somewhat more comprehensive than the + 5-volt current limit internal check.

CAUTION

Overloads should be applied for the minimum time required to obtain a reading from previously connected test probes. Do not leave power applied while meditating upon test results.

1. Verify ac power is off. Connect the DMM to read the 5-volt output, negative lead to logic ground (TP3), positive lead to 5-volt output (TP2).

2. Set adjustable load to maximum resistance (minimum current) and connect to 5-volt output, negative lead to P11-2, positive lead to P11-5. Polarity is not important for a resistive (passive) load.

3. Turn on ac power.

4. Record the DMM measurement at each of the following loads:

   a. 1.0 A (5.0 ohm, 5 W)

   b. 2.0 A (2.5 ohm, 10 W)

   c. 3.0 A (1.67 ohm, 15 W)

   d. 4.0 A (1.25 ohm, 20 W)

5. Turn off ac power. All DMM readings from the previous step should be in the range +4.875 to +5.125 Vdc. If all the readings are out of range by the same amount, there may be an offset error in the 5-volt regulator circuitry. If the voltage drops significantly (by 0.5 volt) as the loading increases, the power supply is current limiting prematurely. Another fault possibility is an incorrect crowbar trigger. Either type of fault should be investigated and repaired before proceeding. Go back to the beginning of this procedure after any such repair.

6. Normal load fault possibilites include:

   a. Rectifier bridge CR4 (high internal resistance)

   b. Current-sensing resistor R8 value shift

   c. Defective series-pass transistor Q1 (high internal resistance).

7. Verify ac power off. Connect a 12.5 A load (0.4 ohm, 62.5 W) to the 5-volt outputs. This overload represents slightly more than 300 percent of rated load current. Verify that the DMM leads are properly positioned to measure the 5-volt output (TP2-TP3).

8. Turn on ac power and read the DMM when conditions stabilize (less than 30 seconds). Turn off ac power.

9. The overload should have induced an output voltage reduction (foldback). The voltage read in the previous step should be in the range +1.5 to +3.5 Vdc.

10. If the output voltage did not foldback to the specified range, investigate and repair the board. Fault possibilities include:

    a. Value shift in current sensing resistor R8

    b. Value shift in resistive dividers

    c. Low internal regulator supply voltage (Vcc*)

d. Series-pass transistor Q10 defective (shorted, open base, or low beta)

e. Defective uA723 regulator device U24.

WARNING

Do not leave power supply on under overcurrent conditions for periods of more than 30 seconds, to reduce the possibility of a component explosion or component failure induced where no fault previously existed.

11. Induce current limiting again by turning on ac power while overload is connected. After verifying the foldback, shut off power, immediately remove load and turn on ac power. Verify that the output voltage returns to the nominal +4.9 to +5.1-volt range.

12. If the voltage remains low, the power supply never recovered from the foldback condition. Investigate fault possibilities and repair.

3.6.7 +5-Volt Overvoltage Crowbar Check

This check requires a heavy-duty lab supply that is adjustable from 0 to +10 Vdc, with a current meter and adjustable current limiting up to 10 amperes.

The crowbar check determines whether the crowbar circuit is capable of protecting the load circuit from overvoltage conditions on the +5-volt output line. The check also detects short circuits on the output side of series-pass transistor Q10.

WARNING

This check involves application of heavy currents. Such currents may cause defective components, such as capacitors and glass-enclosed diodes, to explode. Wear safety glasses at all times and be alert for hissing, fizzing, smoke, burnt smell, or other signs of imminent overheating. Shut off all power sources to the board immediately upon detecting such symptoms.

Check the crowbar circuit as follows:

1. Disconnect the low voltage 7.5-Vac input to the unit under test.

2. Remove the logic ground to chassis ground shorting jumper (E7-E8) if installed.

CAUTION

The next step deliberately misadjusts the power supply output voltages. Do not return to service without performing the +5-volt adjustment procedure of paragraph 3.6.2.1 on the unit under test (UUT).

3. Adjust R3 fully counterclockwise.

4. Adjust the overcurrent limit on the lab power supply to 7 amperes at 6.8 volts, and then reduce the output voltage to zero.

5. Turn off the lab power supply, and connect the lab power supply outputs to unit under test as follows:

   a. Positive (+) lead to P11-5 (UUT +5-volt output)

   b. Negative (–) lead to P11-6 (UUT logic ground)

6. Connect the DMM across Q2, with positive lead to the cathode (TP2) and negative lead to the anode (logic ground TP1). Set up the DMM to read dc voltages, 10 Vdc full scale.

NOTE

The following steps require the technician to increase the dc voltage applied to the UUT +5-volt output, while monitoring the current meter for a sudden increase. The voltage just prior to the current surge is the trigger point of the crowbar circuit. This voltage trigger point is to be recorded. It may be necessary to repeat these steps several times to accurately determine the trigger point.

7. Turn on the lab power supply.

8. Gradually increase the lab power supply output voltage from 0 volts toward +6.9 volts, while monitoring for a current surge. Upon occurrence of the current surge (crowbar trigger point), reduce the lab power supply output to 0 volts. Upon reaching +6.9 volts without any discernible current increase, reduce the output voltage to zero volts.

9. Record the DMM voltage measurement at the crowbar trigger point. Repeat the previous step as necessary to get a reading or determine that the crowbar is not functioning.

10. Turn off the lab power supply. The trigger point voltage should be between +5.3 volts and +6.8 volts. The possibilities include:

    a. Output current increased linearly with increasing input voltage, at least up to the overcurrent limit set on the lab power supply. This indicates a short from the +5-volt line to ground, or else the crowbar is always on. A short is not necessarily in the crowbar circuit. Fault possibilities include C4, triac trigger control transistor Q2, zener diode VR2, triac Q3, or a solder bridge. If the crowbar is always on, or comes on at a very low voltage, the fault may be in Q2, R9, R10, R11, R12, or V2.

b. Output current remained low over the entire 0-6.8 volt range. This indicates that the triac never triggered. Fault possibilities include zener VR2 open, Q2 open, C5 shorted, defective resistor, or Q3 defective.

c. Triac triggered between 0.5 and 6.2 volts. Fault possibilities include Q2 or resistance value shift in voltage divider and biasing resistors R9, R10, R11, R12. Other possibilities include Q3 or VR2 shorted.

11. If this check fails, investigate and repair defect. Repeat the check.

12. The power supply is misadjusted at this point. Readjust the +5-volt output and recheck the +24-volt output before returning the unit to service.

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

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  Tx-yy

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  Fx-yy

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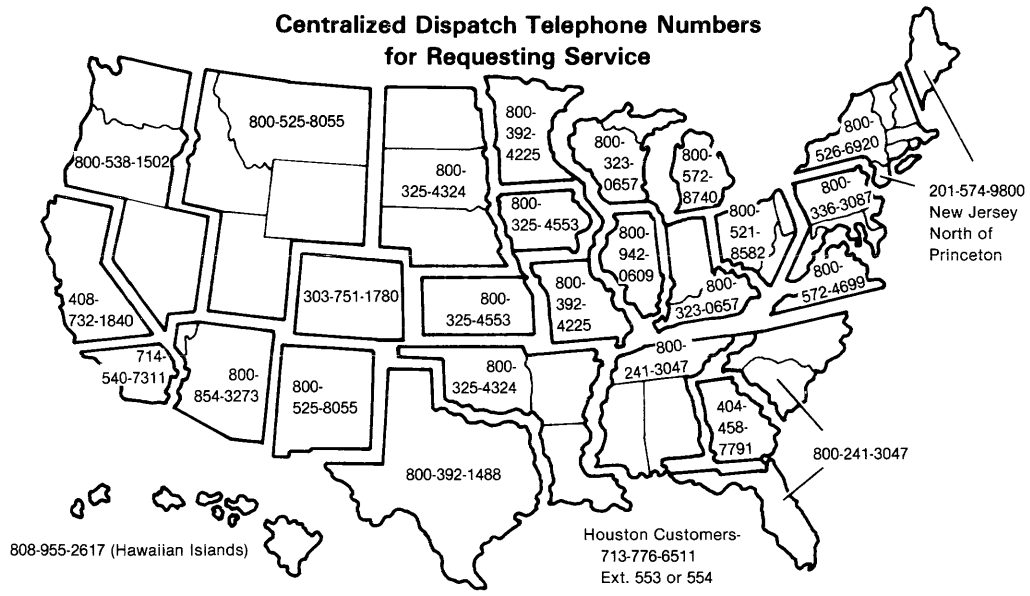

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