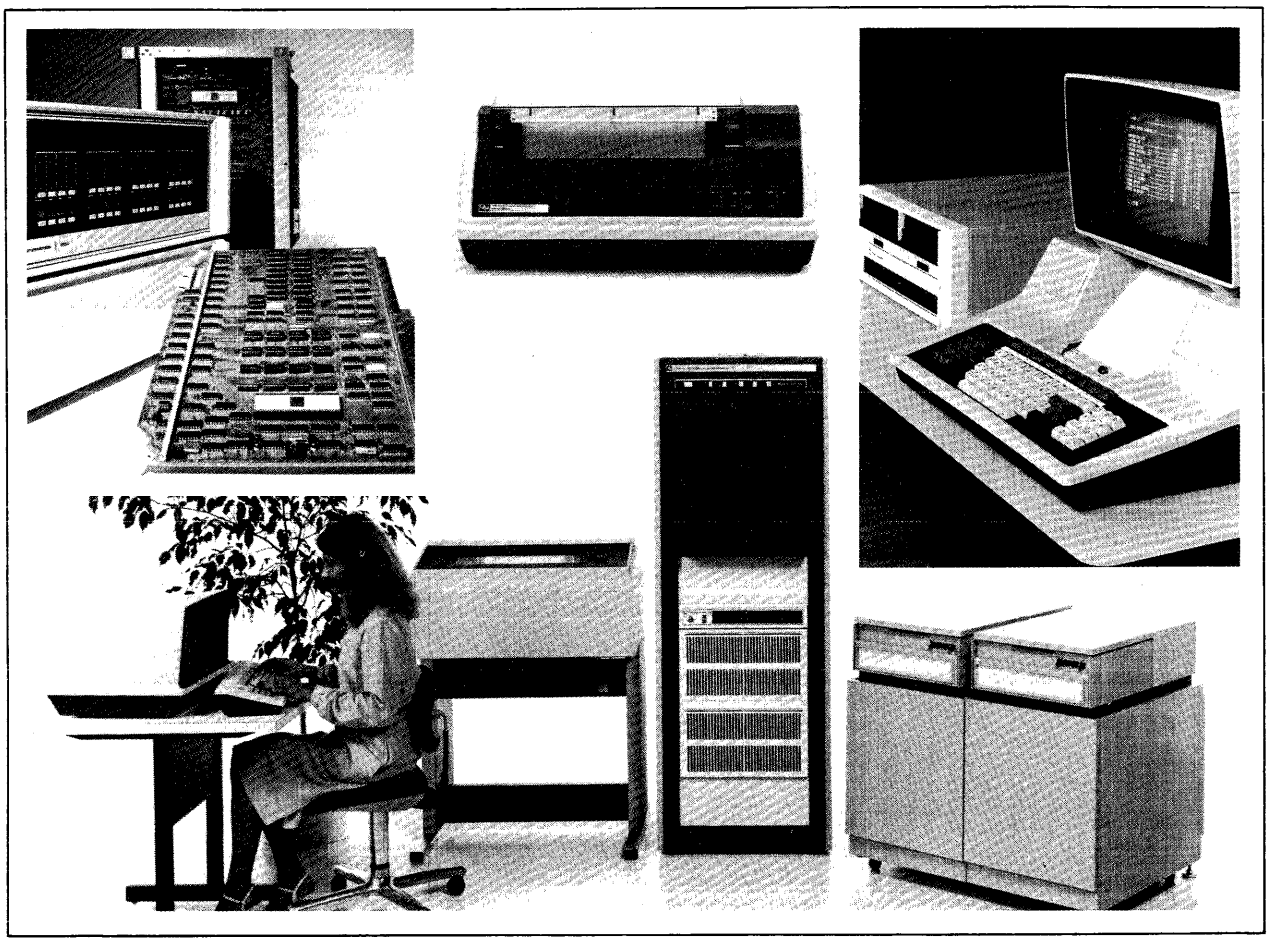
Model 990 Computer
DS10 Cartridge Disk Controller
Depot Maintenance Manual



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PREFACE

This manual contains operating theory and maintenance information for the Model DS10 Disk Controller, part number 937505-1 or 2262100-1 (fine line), a major component of the Model DS10 Cartridge Disk System, part number 937500-xxxx.

The maintenance philosophy of this manual is based on an operating 990 computer with associated peripherals (hot mock-up) and a diagnostic program. The test configuration allows the use of standard test equipment, such as oscilloscopes and logic analyzers, as well as special test equipment, such as the state board.

This manual contains three major sections and seven appendixes as follows:

Section

1 General Description — Standard equipment configurations, physical description, control and status word summary, disk formats.

2 Theory of Operation — Detailed theory of operation, proceeding from the basic block diagram level to the logic diagrams. Includes descriptions of microinstruction formats and internal control firmware routines.

3 Maintenance — Checkout, troubleshooting, and fault isolation based on the hot mock-up system, diagnostic program, and controller self-test provisions.

Appendix

A Installation Data and Switch Settings

B PWB Signal Dictionary

C Fine Line Signal Dictionary

D Microcode Flowcharts

E Microcode Listing

F Controller I/O Connector P3 and P4 Pin Connections and Signal Flow

G Logic and Assembly Drawings

Other manuals which are related to the Model DS10 Disk Controller and the Model DS10 Cartridge Disk System are:

Title	Part Number
Model 990 Computer Model DS10 Cartridge Disk System Installation and Operation	946261-9701
Model 990 Computer Model DS10 Cartridge Disk System Field Maintenance Manual	945419-9702

Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990 Computer Unit Diagnostics Handbook	
Volume 1, General 990 Unit Diagnostic Information	945400-9701
Volume 3, Diagnostics for 990 Mass Storage Devices	945400-9703

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SECTION 1

GENERAL DESCRIPTION

1.1 GENERAL

The Model DS10 Cartridge Disk Controller (part number 937505-1) and Fine Line Disk Controller (part number 2262100-1) described in this manual are major components of the Model DS10 Cartridge Disk System. This system is compatible with any Model 990 Computer which incorporates Texas Instruments high-speed TILINE* data bus. The Model DS10 Cartridge Disk System provides high-speed, nonvolatile mass storage to supplement the semiconductor main memory in the Model 990 Computer.

A Model DS10 Cartridge Disk System consists of a Model DS10 Cartridge Disk Controller or Fine Line Disk Controller, one or two DS10 dual disk drives, and the necessary interconnecting cables. Each DS10 dual disk drive uses two disk platters for data recording. One of the platters is built into the disk drive; the other is contained in a 5440-type removable disk cartridge. Each platter has an unformatted storage capacity of 6.3 megabytes, and a formatted storage capacity of 4.7 megabytes (at one sector per record).

The disk system features include:

- Single-board controller that occupies one slot in the 990 chassis.
- One fixed and one removable cartridge disk platter per drive unit for a total of 9.4 megabytes (formatted) or 12.6 megabytes (unformatted) per disk drive.
- Up to two disk drives per controller.
- Automatic track-switching across head and cylinder boundaries.
- Variable record formats, from one sector per record to one track (20 sectors) per record, for most efficient disk utilization.
- 312K byte per second data transfer rate.
- Controller automatic self-test prior to data transfer.

Figure 1-1 is a functional block diagram that illustrates the relationship between the major functional blocks of the Model DS10 Cartridge Disk System.

The TILINE data bus is the control and data path between the 990 memory, the 990 central processor, and the disk controller. The 990 central processor initiates a disk operation by sending a block of eight control and parameter words to the disk controller. The disk controller performs the specified operation, including data transfers to and from the 990 memory, without additional control.

The fixed and removable disk platters within a disk drive are treated as separate logical units; i.e., a separate block of control words is used to control data transfers to each platter. There is no automatic "spillover" of data from one platter to another. Also, because of the common read/write head carriage shared by the two platters, there is no independent overlapped seek operation in a DS10 system.

* TILINE is a registered trademark of Texas Instruments Incorporated.

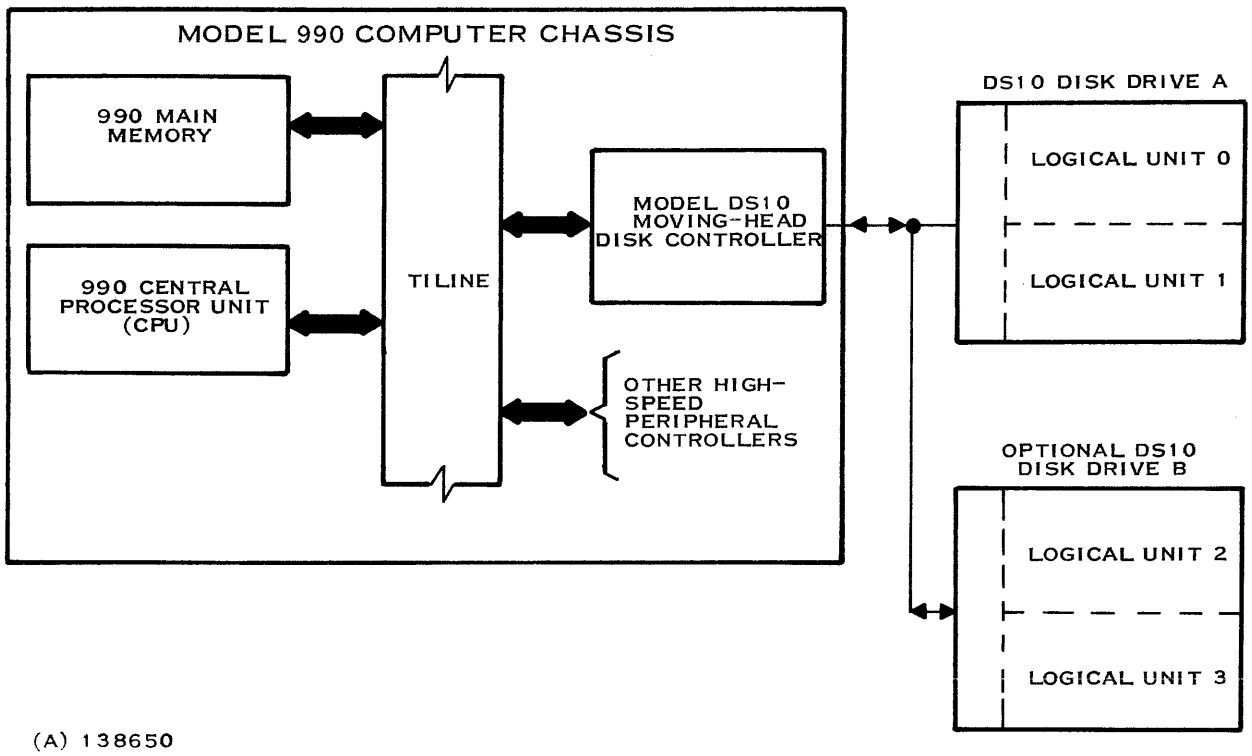


Figure 1-1. DS10 Cartridge Disk System Functional Diagram

1.2 TILINE

The powerful TILINE high-speed data bus architecture is used to incorporate the disk controller directly into the addressable memory space of the 990 computer. The TILINE is an asynchronous, high-speed, 16-bit data transfer bus that transfers data between high-speed system elements. These elements include the CPU, the memory, the disk files, and the magnetic tape transports.

Data is transferred along the TILINE data bus as 16-bit parallel words, accompanied by 20-bit word addresses. The TILINE is capable of transferring approximately 50 million bits per second. This speed helps minimize the overhead time for data transfer to and from the disk drive.

Two classes of TILINE devices interface with the TILINE bus. Users of the bus are called TILINE masters and the respondents are called TILINE slaves. The disk controller is both a master and a slave. It is a slave when receiving commands from the CPU, and a master when contending for the TILINE bus to transfer data to or from the memory.

Multiple users of the TILINE contend for access to the bus in a positional priority scheme. When a device controller has data to transfer over the TILINE, the TILINE master logic of the controller must gain access to the TILINE and then may address a slave device, such as memory, and read or write data.

1.3 DS10 CARTRIDGE DISK CONTROLLERS

The Model DS10 Cartridge Disk Controllers, figures 1-2 and 1-3, are single circuit boards which occupy full-slot positions in a 990 computer chassis or TILINE expansion chassis. The controllers operate one or two disk units, each with a fixed and a removable platter which are assigned individual logical unit numbers.

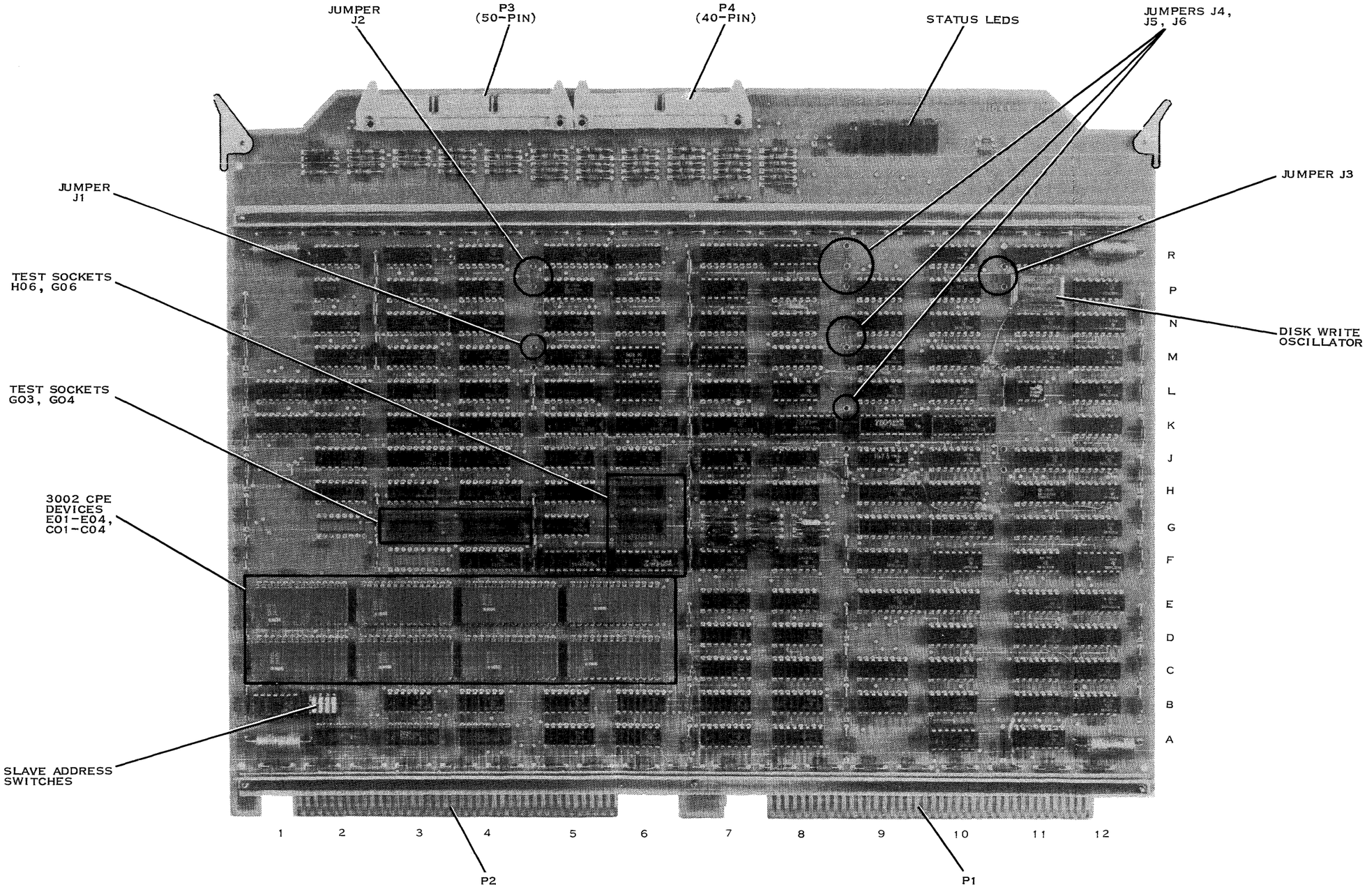
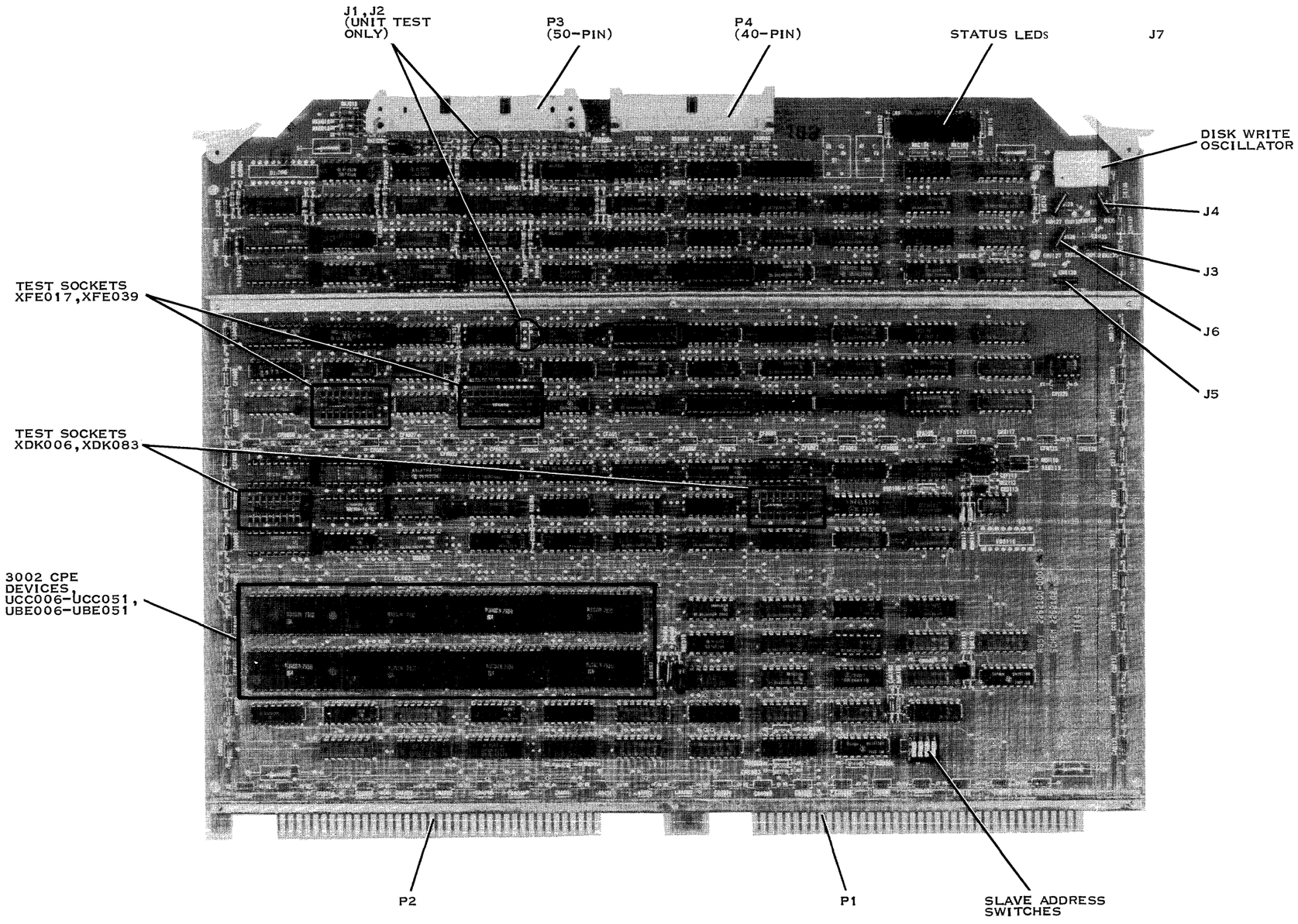


Figure 1-2. Model DS10 Moving-Head Disk Controller (PWB)



2278539

Figure 1-3. Model DS10 Moving-Head Disk Controller (Fine Line)

The disk controller performs the following major functions:

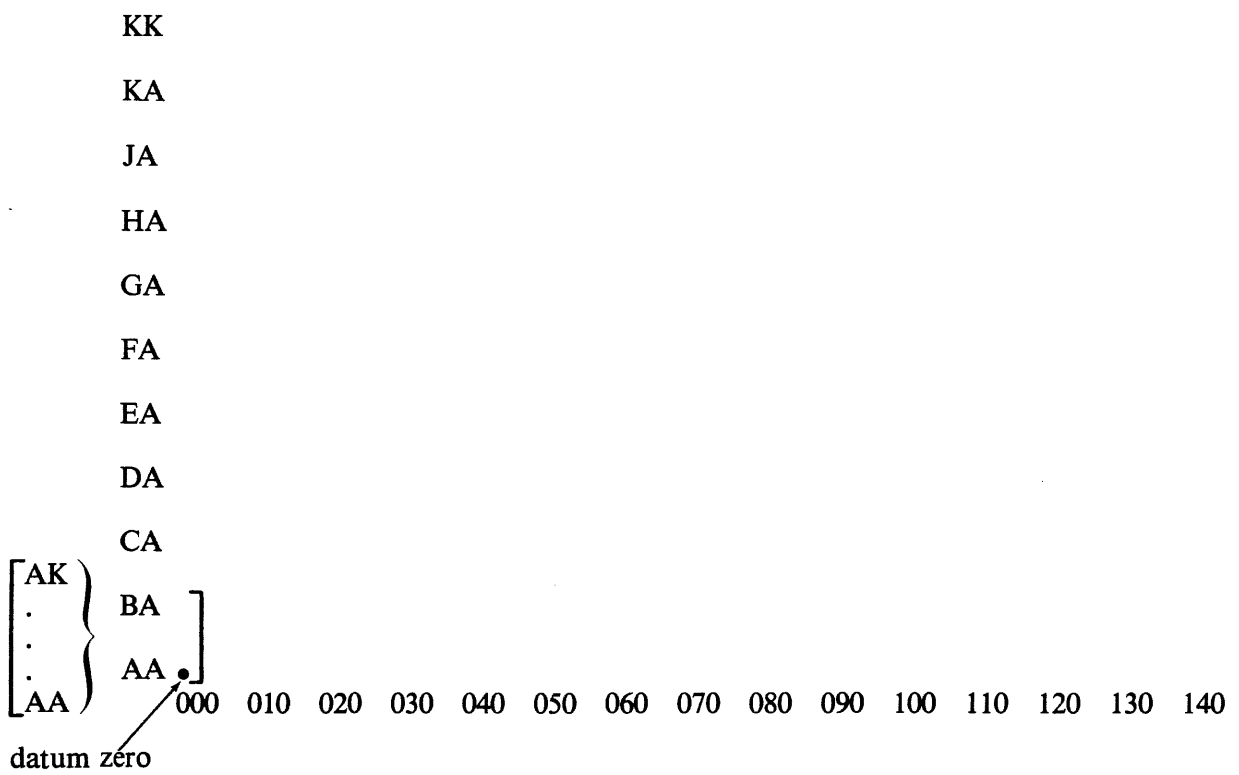
- Acts as a TILINE slave device to accept setup commands from the 990 processor and to supply status information to the processor.
- Acts as a TILINE master device to acquire control of the bus and transfer data between the selected disk and the memory.
- Issues the disk drive control signals and monitors the disk drive status output signals.
- Performs serial/parallel data format conversions, data rate buffering and error checking on data transferred between the computer memory and the disk drive.
- Performs extensive self-testing to ensure data transfer integrity.

1.3.1 DS10 CARTRIDGE DISK CONTROLLER PHYSICAL DESCRIPTION. Edge connectors P2 and P1 at the bottom of the logic board mate with the 990 motherboard connectors. The 100 mil grid molded plastic connectors P3 and P4 at the top edge of the board mate with the controller/disk drive cables.

IC device locations on the board are organized into 12 columns and 15 rows. Neglecting the oversized sockets for the 3002 devices, the row-column organization (component side) is:

	1	2	3	4	5	6	7	8	9	10	11	12
R												
P												
N												
M												
L												
K												
J												
H												
G												
F												
E	*	*	*	*	*	*						
D	*	*	*	*	*	*						
C	*	*	*	*	*	*						
B												
A												

On the fine line board, the row-column organization is as follows:



On the vertical axis, there is one inch between AA and BA, and the second letter in the designation increments each tenth of an inch. Thus, the starting point (datum zero) is AA, 0.1 inch equals AB, 0.2 inch equals AC, etc. (Note that the letter I is omitted; the counting moves from H to J.) On the horizontal axis, the columns are marked in tenths of an inch, so that the starting point (datum zero) is 000, 0.1 inch is 010, 0.2 inch is 020, and so on. The reference designator for a device (for example UDE073) begins with the device code (for instance, U for integrated chip or R for resistor), followed by two letters locating the row occupied by the bottom pins of the device, and ending with three numbers indicating the column occupied by the leftmost pin of the device.

The asterisks represent the board space occupied by the 28-pin double-width sockets for the 3002 central processing element (CPE) devices. These devices are organized as follows:

E01	E02	E03	E04		UCC006	UCC021	UCC036	UCC051
C01	C02	C03	C04	or	UBE006	UBE021	UBE036	UBE051
(PWB)					(Fine Line)			

The TILINE base address selection switch, B02, is located below CPE device C01 (lower left corner of board). On the fine line board, the TILINE base address selection switch, located at UAE104, at the lower right corner. Switch setting information is given in Section 2 with the TILINE slave logic description.

Resistive line terminators are located in the space between the P3, P4 I/O connectors and the upper stiffener bar.

A group of light-emitting diode (LED) indicators in the upper right corner display the operational status of the board. Interpretation of these indicators is described in Section 3 of this manual.

Disk controller physical dimensions are 362 millimetres (14.25 inches) by 266.7 millimetres (10.5 inches) by 12.7 millimetres (0.5 inch). The controller draws 5.5 amperes at 5 volts dc and 0.03 amperes at -12 volts dc from the 990 chassis power supply via the 990 motherboard.

1.4 DISK DRIVE

The DS10 disk drive is available in a rack-mount version, figure 1-4, or in a quietized (acoustically suppressed) pedestal-mounted version, figure 1-5. The rack-mount version mounts on slides in any standard 19-inch EIA cabinet, such as the office-style desk enclosure supplied with Texas Instruments DS990 commercial computer systems. The slides are a necessity because the 5440-type removable disk cartridge is installed and removed from the top of the unit.

The quietized pedestal supports the DS10 disk drive at a convenient height for changing disk packs. A hinged dust cover protects the disk cartridge from environmental contamination. The quietized pedestal features acoustic noise suppression measures which make it particularly suitable for the office environment.

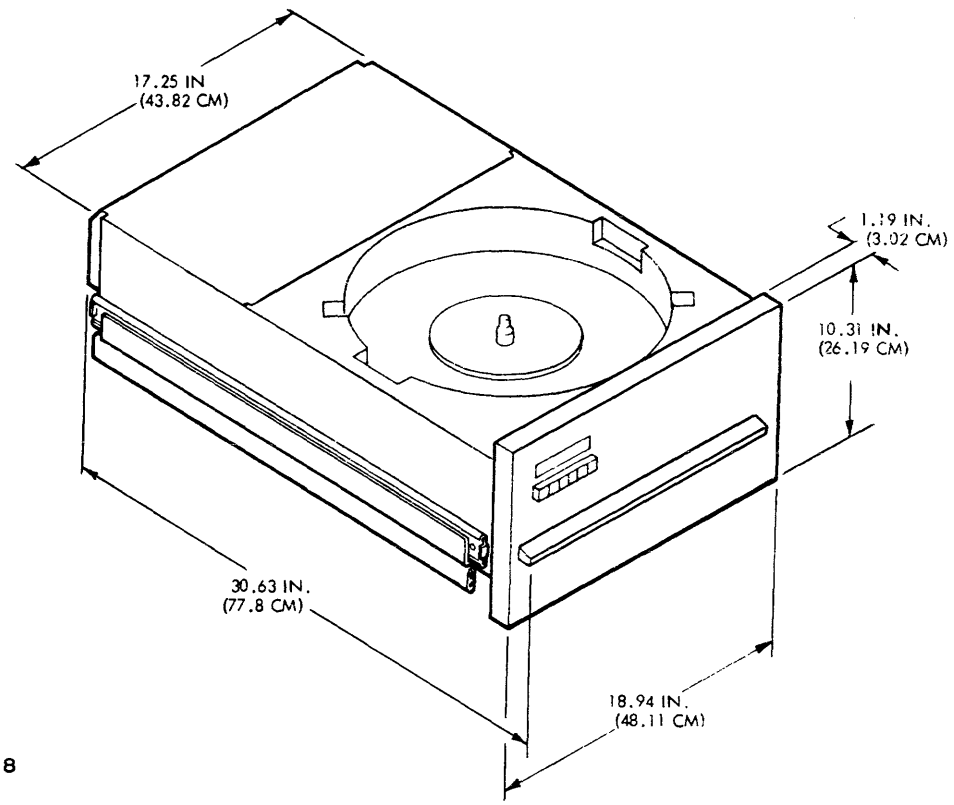


Figure 1-4. Rack-Mount Disk Drive

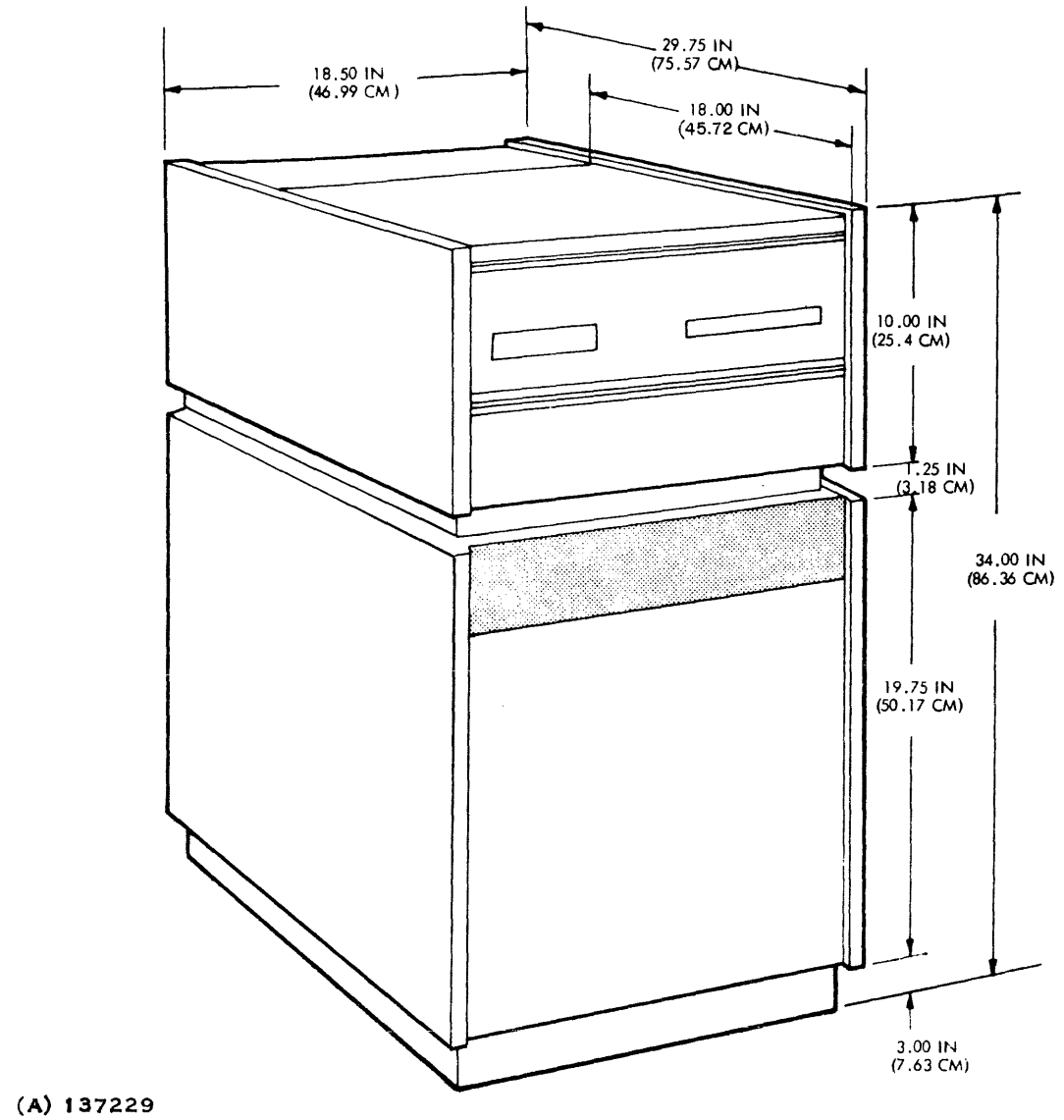


Figure 1-5. Cabinet-Mount Disk Drive

Six operating controls and indicators are located on the front panel of the disk drive, as shown in figure 1-6 and described in table 1-1. A brush automatically extends to sweep the disk surfaces when the disk drive is turned on. A slot indicator on top of the drive indicates whether the brush is extended into the disk area or retracted. The brush must be in the retracted position when changing disk cartridges.

Table 1-2 is a summary of the disk drive specifications.

1.5 DISK SYSTEM CONFIGURATION AND INTERCONNECTION

Table 1-3 lists the part number assignments for the components of a Model DS10 cartridge disk system. Both rack-mount and quietized pedestal-mounted versions are listed in the table.

A cable adapter is required at the input to each disk drive. The cable adapter adapts the 3M-type cable connectors to the Winchester-type connectors on the disk drive. Figure 1-7, the rear view of the rack-mount disk drive, clearly shows the Winchester I/O board.

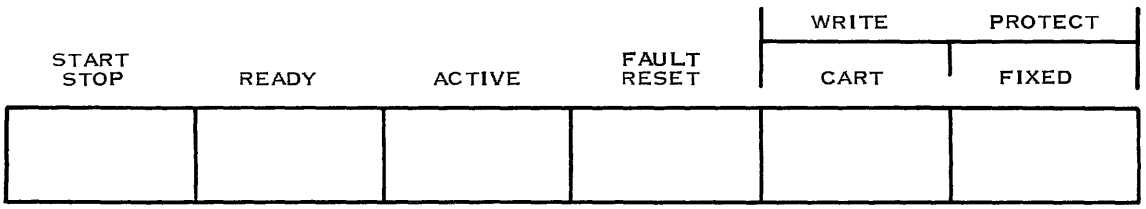


Figure 1-6. DS10 Front Panel Switches and Indicators

Figure 1-8 is a detail view of the Winchester connectors and the Winchester I/O board. The resistive terminators, XRM1 - XRM12, must be installed in the last disk drive on the bus. They must be removed from drive A if the bus is extended to drive B.

The switches on the Winchester I/O board select various optional features of the drive. These switch settings are given in *Model 990 Computer, Model DS10 Cartridge Disk System Installation and Operation,* part number 946261-9701. They are also included in the documentation package supplied with the disk drive.

Table 1-1. DS10 Disk Drive Controls and Indicators

Control/Indicator	Description
START/STOP	This control permits starting and stopping of the disk drive motor to initiate or stop disk operation. The push button is lighted when the disk drive motor is running.
READY	This indicator lights to show that the disk drive motor has reached operating speed, the heads are loaded, and the drive is ready for data transfer.
ACTIVE	This indicator lights when the disk drive is actively engaged in any operation.
FAULT	The FAULT indicator lights to indicate the occurrence of a nondamaging fault such as more than one read/write head selected simultaneously, simultaneous read and write instruction, or other fault. Pressing the lighted FAULT indicator clears the fault logic and extinguishes the indicator.
W/PROT CART and W/PROT FIXED	These switches allow the operator to protect either the fixed or cartridge disk against writing of data. The active indicator lights to indicate the condition.

Table 1-2. Disk Drive Specifications

Item	Specification
Spindle speed	2400 rpm with ±2% speed variation with input frequency ±0.5 hertz and input voltage +10% - 15%
Cylinders per drive	408, numbered 0 through 407
Tracks per drive	1,632
Tracks per cylinder	4
Sectors per drive	32,640
Sectors per track	20
Heads per cylinder	2
Heads per drive	4
Recording surfaces per drive	4
Recording mode	Double frequency (FM)
Track density	200 tracks per inch
Recording density	1524 bits per inch (outer track) 2200 bits per inch (inner track)
Bits per disk platter	50,000,000 nominal
Bits per cylinder	250,000 nominal
Bits per track	62,500 nominal
Bits per sector	3,125
Capacity (unformatted)	12.6 megabytes
Words per sector	144
Format overhead	48 words
Bit rate	2.5 megahertz
Average access time	35 milliseconds
Average latency time	12.5 milliseconds
Track-to-track access time	7 milliseconds
Maximum access time	60 milliseconds

Table 1-3. Model DS10 Cartridge Disk System Components

Component	Part Number
Model DS10 disk controller (PWB)	937505-0001
Model DS10 disk controller (fine line)	2262100-0001
Model DS10 disk drive, rack mount	937513-0001
Model DS10 disk drive, pedestal mount	937513-0005
Disk cartridge	937507-0001
40-pin, 20-foot bus cable assembly	937515-0001
50-pin, 20-foot bus cable assembly	937516-0001
Cable adapter	937510-0001
40-pin, 6-foot daisy chain cable assembly	937515-0002
50-pin, 6-foot daisy chain cable assembly	937516-0002

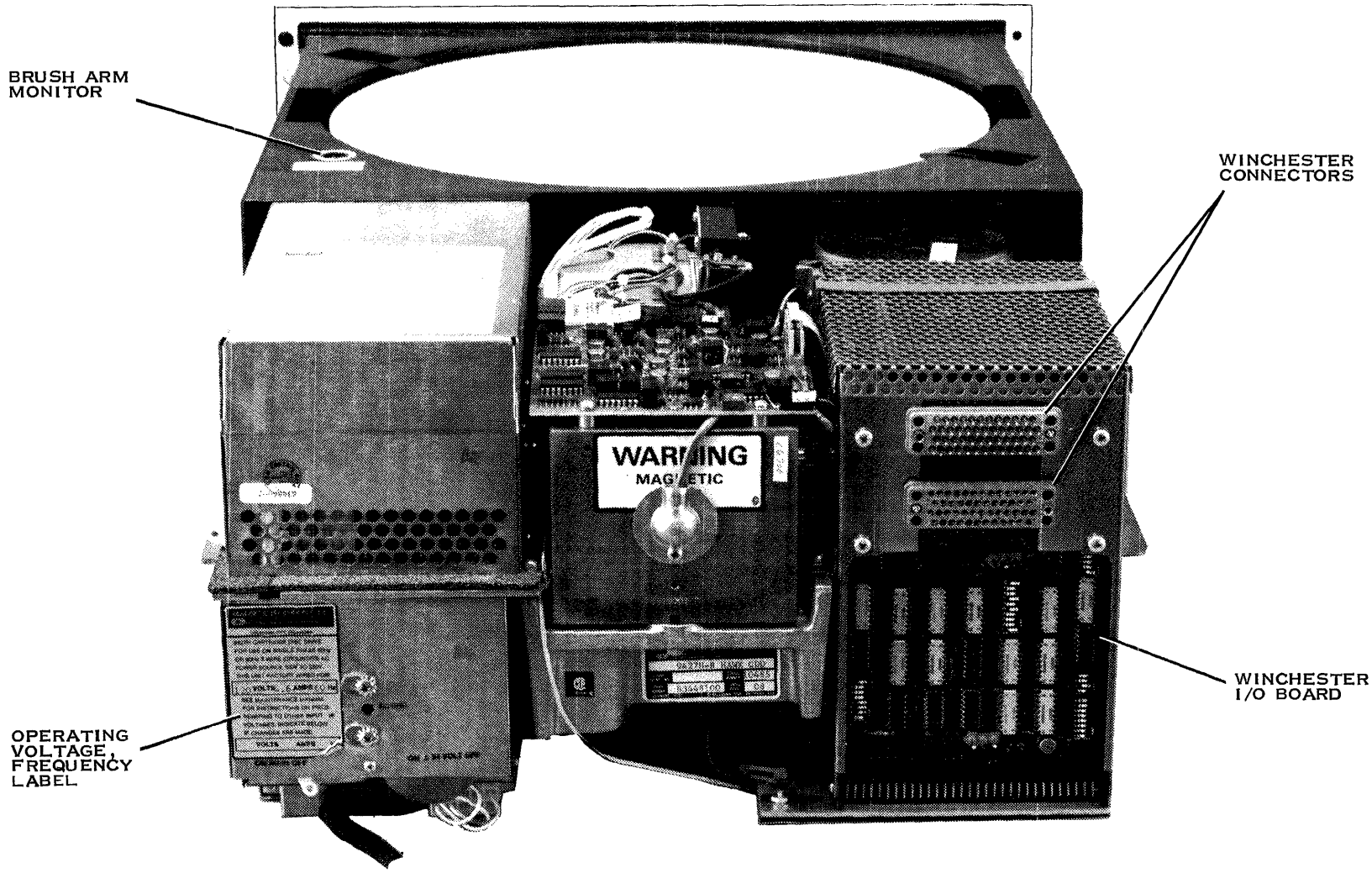
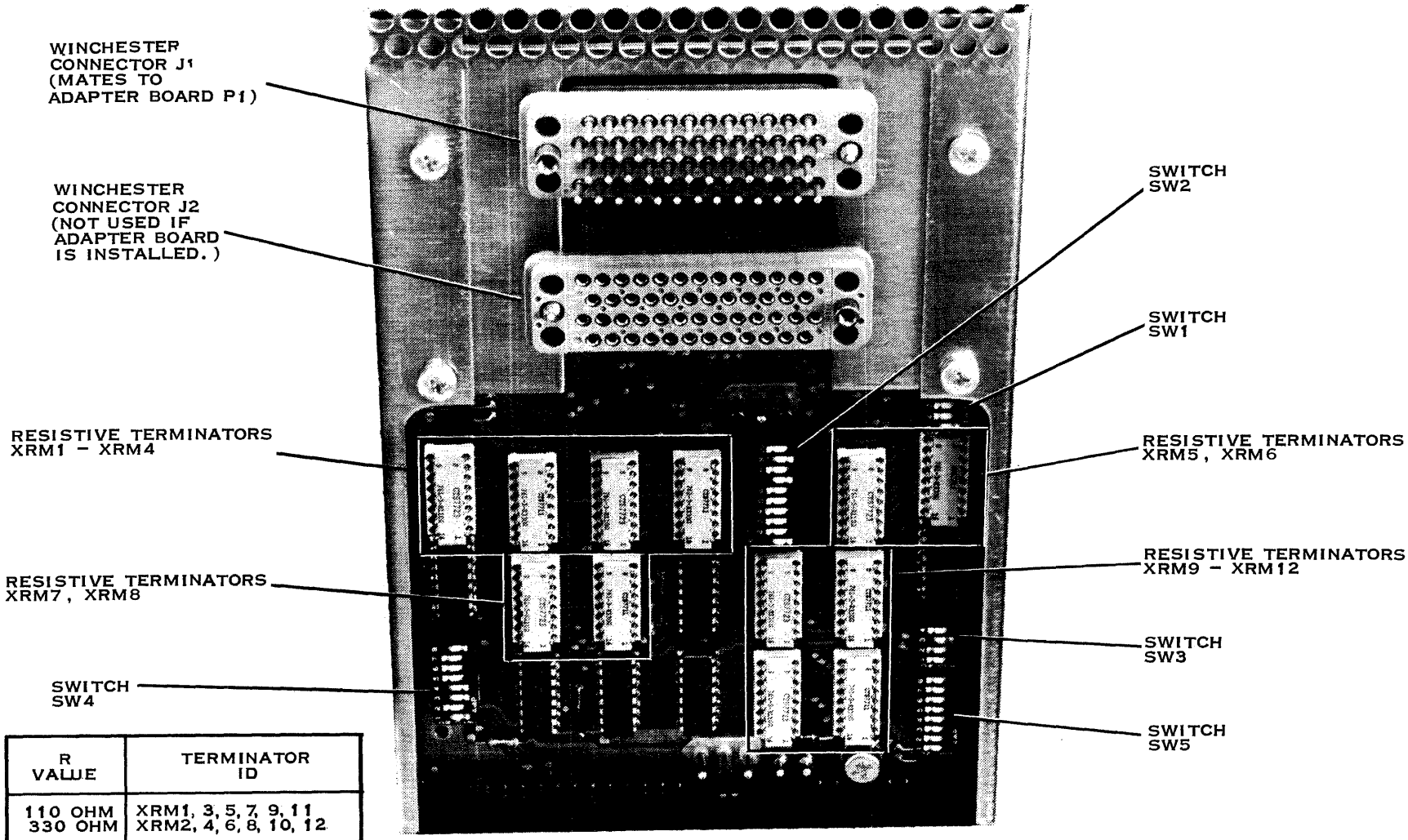


Figure 1-7. Rear View of DS10 Rack-Mount Disk Drive



R VALUE	TERMINATOR ID
110 OHM 330 OHM	XRM1, 3, 5, 7, 9, 11 XRM2, 4, 6, 8, 10, 12

(A) 137637 (990-977-35-6)

Figure 1-8. Expanded View of Winchester I/O Board

Figure 1-9 is a detail view of the cable adapter, part number 937510-0001, mounted on the Winchester connectors at the back of a rack-mount disk drive. The cable adapter schematic, drawing number 937512, shows that the 50-pin connectors are wired in parallel, as are the 40-pin connectors.

A jumper option on the cable adapter board makes it possible to reverse the logical unit numbers assigned to the fixed and to the removable cartridge disk. For the first disk drive (drive A), the normal configuration is unit 0, fixed and unit 1, removable. Installing the jumper from J1 to J3 reverses this assignment.

For the second drive (drive B), the normal configuration is unit 2, fixed and unit 3, removable. Installing the jumper from J1 to J4 reverses this designation.

CAUTION

Exchanging cable adapters (with reversing jumpers) between drives may cause inadvertent changes in system configuration.

1.5.1 DISK SYSTEM CABLING. Figure 1-10 shows the cabling configuration for a single DS10 rack-mount disk drive and controller. The cable adapter is mounted to the Winchester connectors at the rear of the disk drive, and the terminator IC networks are installed in the Winchester I/O board.

Figure 1-11 shows the cabling for two rack-mount disk drives and a controller board. Note that the terminator IC networks are removed from the drive in the middle of the bus, and installed in the second drive.

CAUTION

The 3M-type cable connectors use an embossed arrowhead as a polarity symbol. When installing any 3M-type cable connector, verify that the arrowheads on jack and plug match before applying mating pressure.

Figure 1-12 is a cutaway view of a pedestal-mounted DS10 disk drive. Unlike the rack-mounting version, the pedestal-mounting disk drive has 3M connectors and a 3M I/O board. Flat 3M cables from the rear of the disk drive are connected to a 3M-Winchester adapter in the lower bay of the pedestal. The 937510 cable adapter mounts on the Winchester connectors in the lower bay. The mounting position is 90 degrees clockwise from that used with rack-mount disk drives.

1.6 PROGRAMMING THE DISK CONTROLLER

Texas Instruments disk-based operating systems contain device service routines which manage the interaction between the Model 990 computer and the Model DS10 Cartridge Disk System. The operating system presents the programmer with a standard set of displays and data which are more characteristic of the operating system software than the disk system hardware. Users who need this type of information should refer to the operating system documentation.

The programming information presented in this section is useful to three main groups of users: those who wish to write their own 990 assembly-language device service routines, those who wish to control disk system operations from the Model 990 control panel, and anyone who needs to understand the basic operating concepts of the disk system.

The Model 990 computer sets up the disk controller by writing a group of eight control words, W0-W7, over the TILINE to the disk controller. These control words specify the operation to be performed, precondition the controller, and supply parameters to the controller. These parameters include the disk logical unit number, the number of words to be read or written, cylinder, head and starting sector address, and the starting address of the assigned 990 memory buffer area.

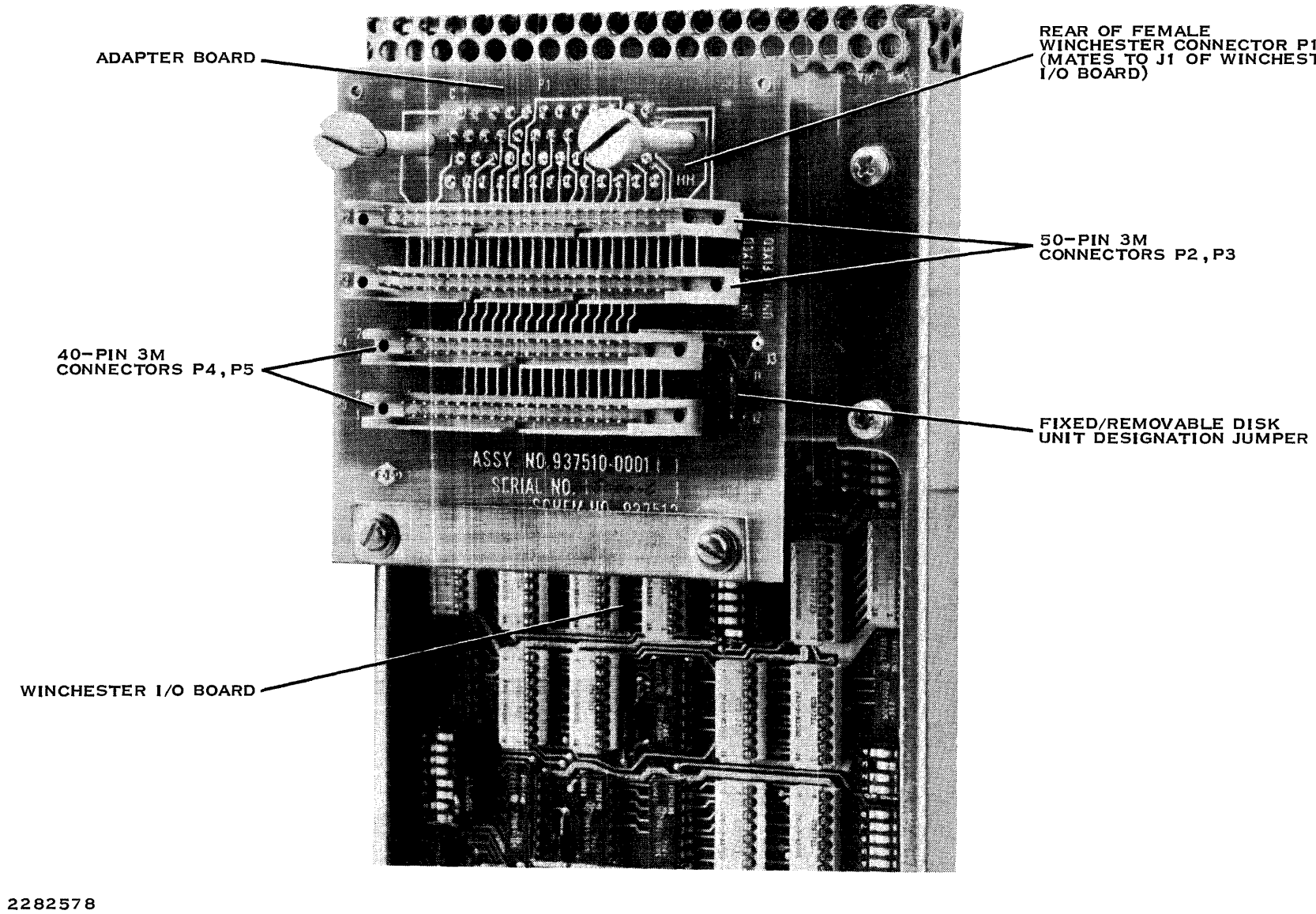
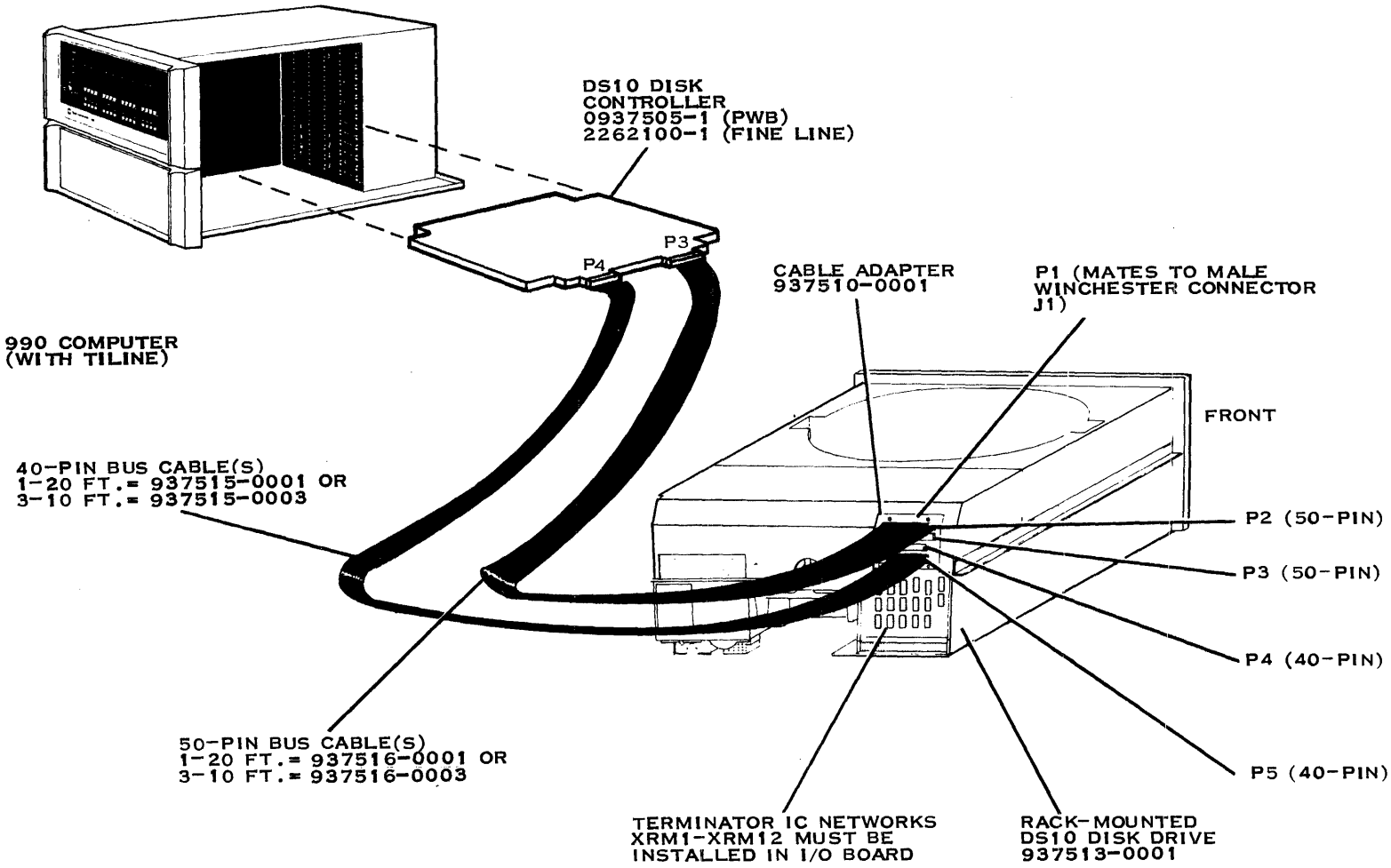


Figure 1-9. Cable Adapter Installed on Winchester I/O Board



(A) 137630B

Figure 1-10. Cabling for Rack-Mount DS10 Disk Drive

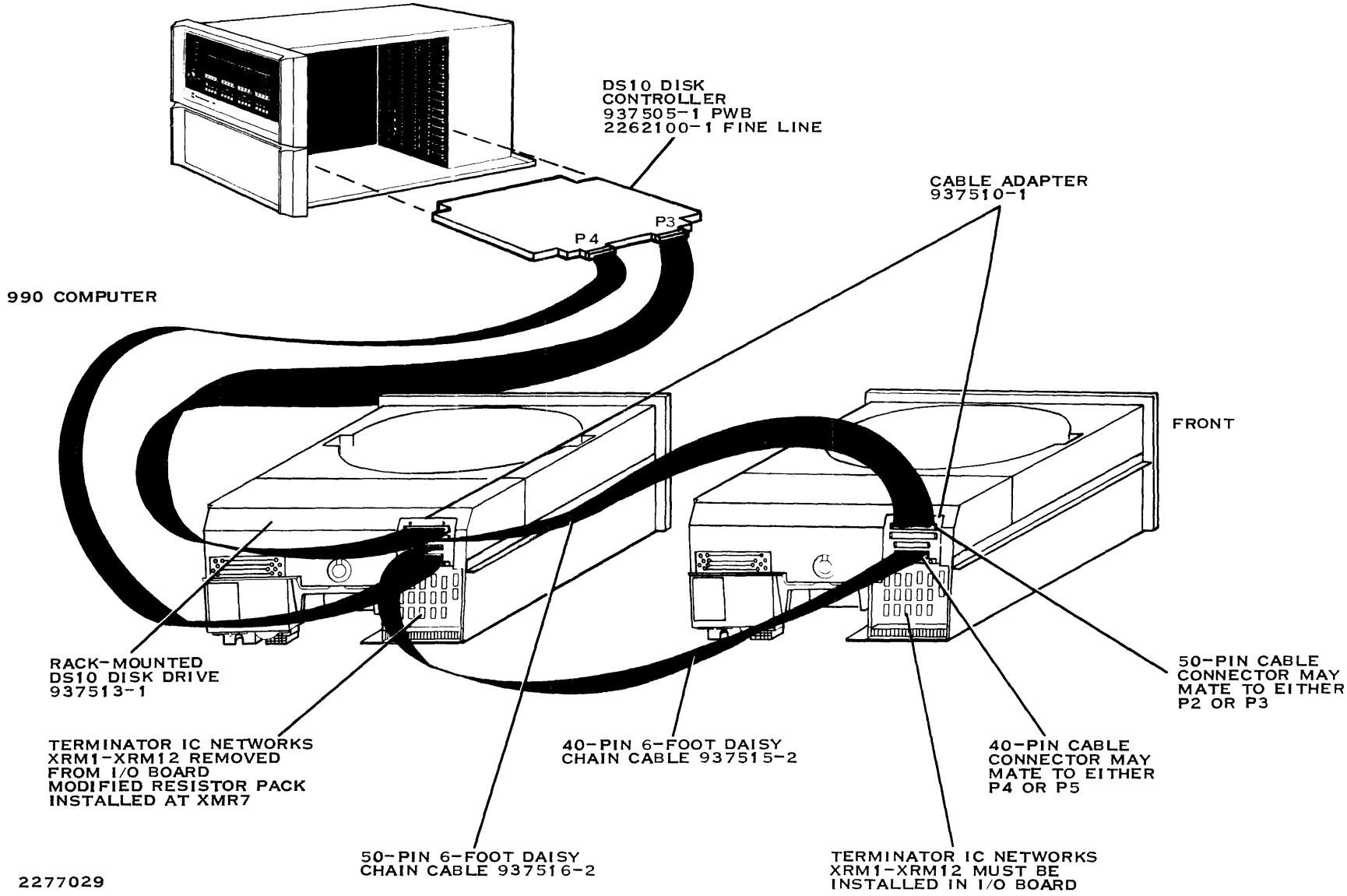


Figure 1-11. Cabling for Daisy-Chained DS10 Disk Drive

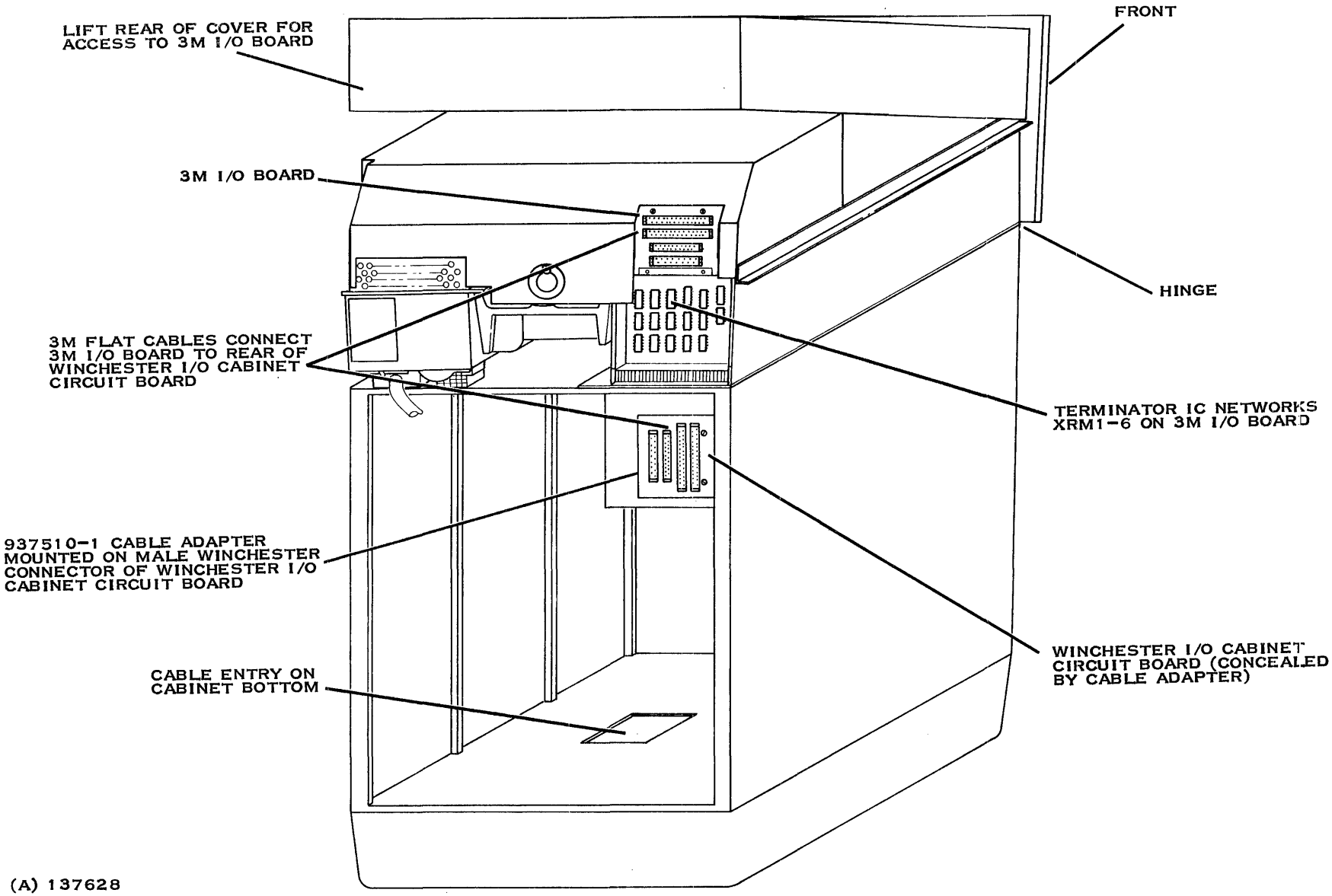


Figure 1-12. Pedestal-Mounted DS10 Disk Drive — Rear View

The last control word, W7, initiates disk controller operations. The disk controller operates under control of an internal microprogram to perform the specified operation. The controller rejects any attempt to write or read back control words while an operation is in progress.

For a disk write operation, the controller TILINE master logic acquires control of the bus and reads data from the specified area of 990 memory. Other controller logic converts the data to serial form and transmits it to the disk drive for recording. For a disk read operation, the controller reads data back from the selected disk platter, checks data integrity, and converts the data back to 16-bit parallel form. The controller TILINE master logic acquires control of the TILINE and transfers the data to 990 memory.

The control words initially supplied to the controller are modified during the course of the operation. At the completion of the operation, the control words contain status information which may be read back by the 990 computer to determine if the operation completed normally. If the operation did not complete normally, the status words identify the errors detected during the attempted operation.

1.6.1 CONTROL WORD ADDRESSES. Standard conventions built into the hardware and software of the Model 990 computer reserve CPU byte addresses $F800_{16}$ to $FBFF_{16}$ for control and status communication with TILINE peripheral controllers, such as the magnetic tape and disk controllers. This range is called the TILINE peripheral control space (TPCS). Addresses in this range may be mapped by the processor hardware to TILINE addresses in the range $FFC00_{16}$ to $FFDFF_{16}$. This mapping requires the 990 processor to be operating in map file 0. The TPCS can also be addressed through alternate map files if the mapping bias value is chosen to yield the correct TILINE address.

The disk controller is assigned a block of eight consecutive TILINE word addresses. These addresses run from a base address to base address +7 word addresses. The base address is dedicated to control and status word W0, base address +1 is dedicated to W1, and so on through base address +7, dedicated to W7.

The base address is selected by a four-section switch on the disk controller board, allowing multiple controllers in one system. Base address selection must be coordinated with the operating system software. Texas Instruments standard operating system software includes specific operator entries at system generation to inform the operating system of the disk controller base address.

The preferred base address for use as the system disk with Texas Instruments standard software is $FFC00_{16}$, which corresponds to CPU byte address $F800_{16}$. Table 2-3 in Section 2 supplies the details of base address switch setting.

Any 990 instruction which reads or modifies memory can be used to communicate with the controller, using the proper CPU byte address. One simple way to send a block of control words to the controller is to store the eight control words at sequential addresses in 990 memory, and then to use an auto-incrementing move (MOV) instruction to transfer the control words to the disk controller. The programmer panel may be used for manual entry via the MA ENTER, MD, MDE, and MAI controls.

1.6.2 COMMAND INITIATION. A three-bit command field in control word W1 (figure 1-13) specifies the basic operation which the controller is to perform. The commands are: STORE REGISTERS, WRITE FORMAT, READ DATA, WRITE DATA, READ UNFORMATTED, WRITE UNFORMATTED, SEEK, and RESTORE. The operation is not initiated until control word W7 is loaded into the controller. W7, bit 0 is the controller Idle/Busy bit. A zero in this position forces the controller out of the idle mode, to decode and execute the command.

CONTROL WORD	CPU ADDRESS	TILINE ADDRESS	FUNCTION
0	F800	FFC00	DISK STATUS
1	F802	FFC01	COMMAND
2	F804	FFC02	FORMAT AND SECTOR
3	F806	FFC03	CYLINDER
4	F808	FFC04	COUNT
5	F80A	FFC05	ADDRESS
6	F80C	FFC06	SELECT AND MSB ADDRESS
7	F80E	FFC07	CONTROLLER STATUS

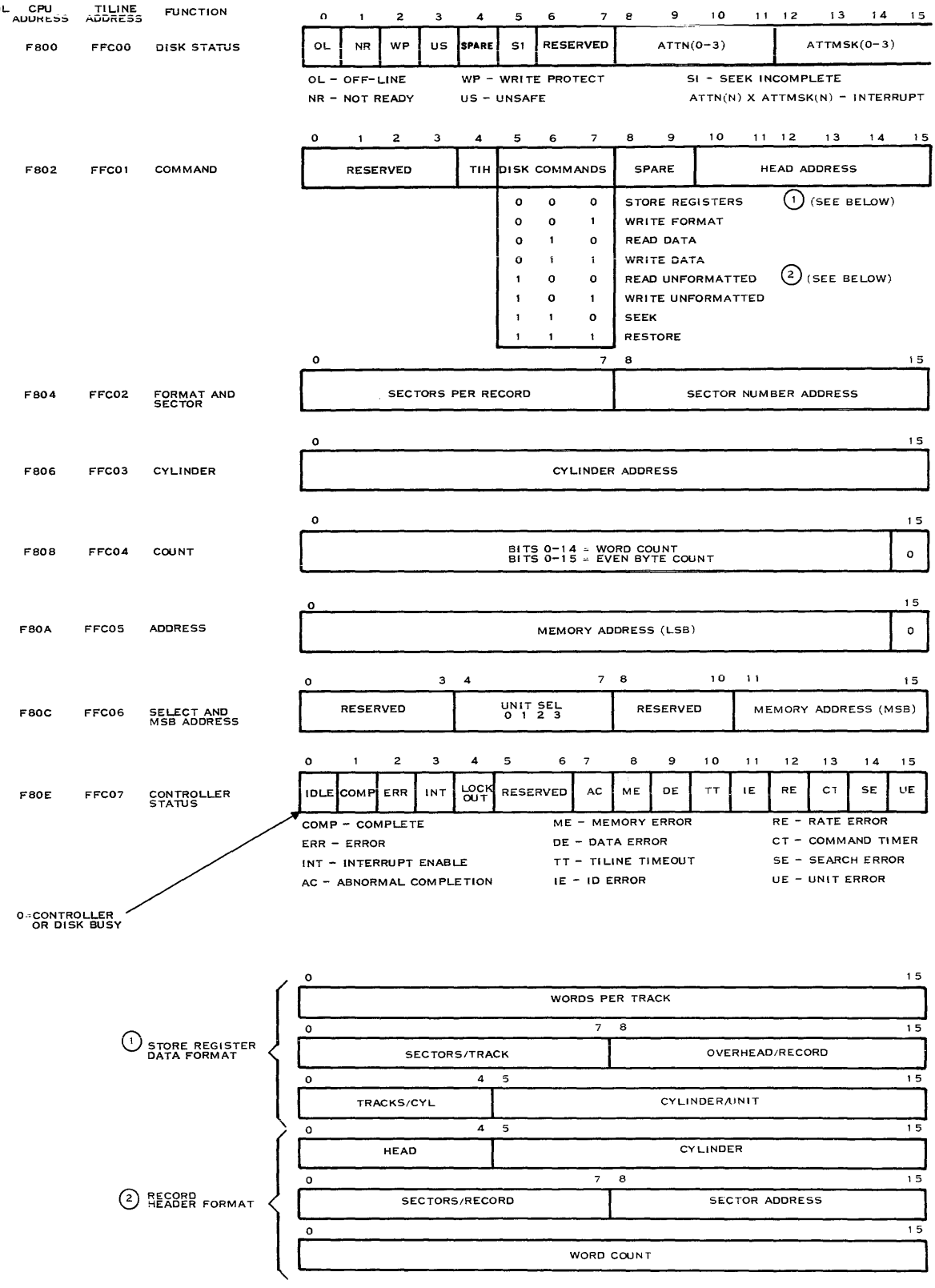


Figure 1-13. Model DS10 Disk System Status and Control Word Formats

Any attempt to write a control word to the controller after the operation has been started will be rejected with an immediate TILINE terminate signal from the TILINE slave logic in the controller. The attempt will not disturb the operation in progress.

Any attempt to read any status word from a busy controller will be answered by a simulated W7 word in which bits 1-15 are meaningless, and bit 0 is a logic zero, indicating that the controller is busy. The attempt to read from a busy controller does not interfere with controller operations. In fact, common programming practice is to read or attempt to read W7 before issuing any command words to the controller. If the returned status word has a one in the MSB position, the controller is idle, bits 1-15 are meaningful status from the previous operation, and the controller is available to accept control words. The act of reading W7 from an idle controller sets a lockout bit which informs any other processor (in multiprocessor systems) that the next disk operation has been reserved.

1.6.3 COMMAND COMPLETION WITHOUT INTERRUPTS. One of the parameters determined by the control words is whether or not an interrupt (to the 990 computer) is to be issued upon completion of the operation. If interrupts are not used, the 990 computer program can determine if the controller has finished by periodically reading control/status word W7. When the command is complete, W7 bit 0 (Idle) is set, and either the normal completion bit (W7, bit 1) or the abnormal completion bit (W7, bit 7) is set.

Normally a programmer would initiate a software timing loop when starting the disk operation, and would read W7 at time expiration. If the Idle bit is still zero, the timer may be restarted and the sequence repeated for a preselected number of attempts. This method involves a considerable larger amount of CPU overhead time than using an interrupt would entail.

1.6.4 COMMAND COMPLETION WITH INTERRUPTS. An operation complete interrupt may be enabled by putting a one in W7, bit 3 when the operation is initiated. At completion, an interrupt is sent to the Model 990 computer, which may read W7 to verify successful completion of the operation.

There are other conditions which can cause the controller to generate an interrupt. The seek complete and restore complete interrupts are incorporated in the DS10 disk controller primarily for software compatibility with other disk storage systems. For example, a DS31 disk storage system may have four drive units, each with an independent head carriage assembly and cylinder address control electronics. With the DS31, it is possible to have multiple, independent seek operations occurring simultaneously. That is, the head carriages are commanded to seek to specified cylinder addresses, and the DS31 controller operation stops while the electromechanical carriage assemblies are moving. Individual attention signals from the drives notify the controller when the seek operation is complete. Attention mask bits (12-15) in control word W0 specify whether an interrupt should be generated when the corresponding attention line goes high. The same description applies to the DS31 return to zero seek (restore) operations, which can be overlapped among four drives. Again, an attention line from each drive notifies the DS31 controller when the physical movement is complete, and an interrupt is generated if the corresponding interrupt mask bit is set.

Independent seek operations are not possible in a DS10 disk drive because logical units share common head carriages. The DS10 disk controller accepts attention interrupt mask bits, and supplies simulated attention bits only for software compatibility with the other drives. An attention interrupt will occur any time the disk controller is IDLE and one or more attention mask bits are set.

The RESTORE command initiates a disk drive clear operation which includes clearing all fault latches in the drive, and driving the head carriage to the fully extended and then the track 0 position. The restore operation is performed on the drive if either of the two logical units in the drive is the selected unit. The controller allots about one-half second for the physical operation, issues an interrupt (if any attention mask bit is set), and returns to the idle mode.

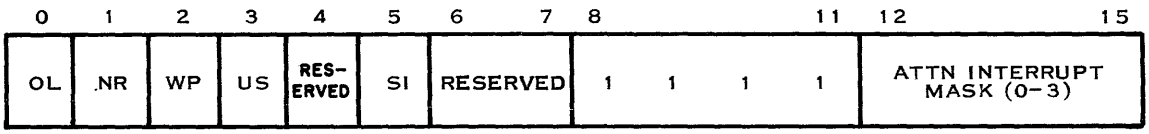
The SEEK command is a dummy command for the DS10 disk controller. The disk controller performs a self-test and if any attention mask bit is set, generates an interrupt. No disk drive operations are performed.

1.7 CONTROL AND STATUS WORD FORMATS

Figure 1-13 shows the formats of the disk controller's control and status words. The CPU addresses and TILINE addresses shown along the left side assume a TILINE base address of $FFC00_{16}$. This preferred base address corresponds to all sections of the TILINE slave address selection switch being in the OFF position.

Data formats for the store registers operation and the record header are shown at the bottom of the figure.

1.7.1 DISK STATUS, W0. When the controller is not busy, the disk status of W0 can be used. Figure 1-14 shows the bits of W0 (disk status). The only bits of W0 which can be written into by the 990 computer are the attention mask bits (12-15).



(A) 133992A

Figure 1-14. Control Word W0

Bits 0 through 5 of W0 contains individual status indicators from the selected disk drive. Bits 8 through 11 are forced to logic 1. The bits are defined as follows:

Bit 0 — Offline
Bit 1 — Not ready
Bit 2 — Write protect
Bit 3 — Unsafe
Bit 4 — Spare (reserved)
Bit 5 — Seek incomplete

1.7.1.1 Bit 0, Offline (OL). When bit 0 is set, it indicates that there is no power to the selected disk drive, that the drive is not at the proper speed, that a disk cartridge is not loaded, no drive corresponds to the selected unit number, or that an unsafe condition exists.

1.7.1.2 Bit 1, Not Ready (NR). When bit 1 is set, it indicates that the selected disk drive is in the process of performing a seek operation, or that the heads are not loaded.

1.7.1.3 Bit 2, Write Protect (WP). When bit 2 is set, it indicates that the write protect status (W/PROT CART switch or W/PROT FIXED switch) of the selected disk drive is on. When this switch is on, it inhibits the write logic within the disk drive.

1.7.1.4 Bit 3, Unsafe (US). When bit 3 is set, it indicates that the selected disk drive is unsafe. This means that the safety circuits that protect the recorded information are unsafe, and the unsafe condition must be removed before any more commands are attempted. If an unsafe condition occurs, the FAULT switch on the selected disk drive can be used to clear the fault condition provided the condition has ceased. A RESTORE command can also be issued to clear the fault condition. The RESTORE command may be manually entered from the programmers panel, or it may be issued by the program running in the 990 computer.

1.7.1.5 Bit 5, Seek Incomplete (SI). When bit 5 is set, it indicates that the selected disk drive has failed to complete a seek operation because of a disk malfunction or detection of an illegal cylinder address (illegal address interlock). When this status is detected, the software must initiate a RESTORE command before attempting to execute any other command.

1.7.1.6 Bits 8 through 11. Bits 8 through 11 are not used and are forced to logic 1.

1.7.1.7 Bits 12 through 15, Attention Interrupt Mask (0 - 3). These bits cause an interrupt when set to logic 1. The TILINE interrupt is set when any attention interrupt mask bit is on and the controller is idle. Software can disable this interrupt source by clearing the interrupt mask bits.

1.7.2 COMMAND CONTROL, W1. Control word W1 is used for disk commands and surface selection. Figure 1-15 shows the bits of W1. The bits of W1 are defined in the following paragraphs.

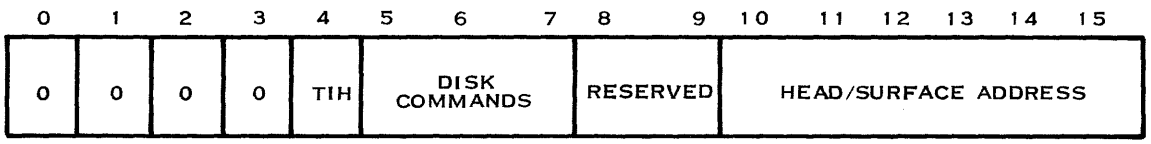


Figure 1-15. Control Word W1

1.7.2.1 Bits 0 through 3. Bits 0 through 3 are reserved, and should be logic 0.

1.7.2.2 Bit 4, Transfer Inhibit (TIH). When bit 4 is set, the controller will not transfer any disk words into memory when a READ DATA command is specified. The purpose of this bit is to allow data verification by relying on the cyclical redundancy check (CRC) without having to provide a buffer in memory for the specified block. After the READ DATA command is completed, this bit is reset by the controller.

1.7.2.3 Bits 5 through 7, Command. These three bits designate a command (one of the eight commands illustrated in figure 1-13). The bits and the commands they specify are listed in table 1-4 and described in detail in the following paragraphs.

NOTE

Details of the contents, format, and programming procedures for the disk commands are provided later in this section. Refer to paragraph 1.8.

Table 1-4. Disk Command Bits

Bits 5 6 7	Command
0 0 0	STORE REGISTERS
0 0 1	WRITE FORMAT
0 1 0	READ DATA
0 1 1	WRITE DATA
1 0 0	READ UNFORMATTED
1 0 1	WRITE UNFORMATTED
1 1 0	SEEK
1 1 1	RESTORE

STORE REGISTERS (000). The STORE REGISTERS command is used to supply disk system parameters to the Model 990 computer.

WRITE FORMAT (001). This command formats or reformats a single track.

READ DATA (010). This READ DATA command reads formatted data from disk and transfers the data to the specified TILINE address.

WRITE DATA (011). Data is transferred from a TILINE address and formatted data being written on disk is controlled by the WRITE DATA command.

READ UNFORMATTED (100). This command reads data from disk without regard to record ID or record boundaries and transfers the data to the specified TILINE address.

WRITE UNFORMATTED (101). The UNFORMAT WRITE command transfers data from a TILINE address and writes the data on the disk without regard to record boundaries.

SEEK (110). The SEEK command is a dummy command that is accepted and completed normally but does not actually move heads.

RESTORE (111). Positions the head over cylinder 0. A restore is implemented by a full stroke movement by the head carriage.

1.7.2.4 Bits 8 and 9. Bits 8 and 9 are reserved and should be logic 0.

1.7.2.5 Bits 10 through 15, Head Address. The field consisting of bits 10 through 15 selects one of the two read/write heads.

1.7.3 FORMAT AND SECTOR, W2. Control word W2 is used to indicate the number of sectors per record and the address of the sector. The bits of this control word are shown in figure 1-16 and defined in the following paragraphs.

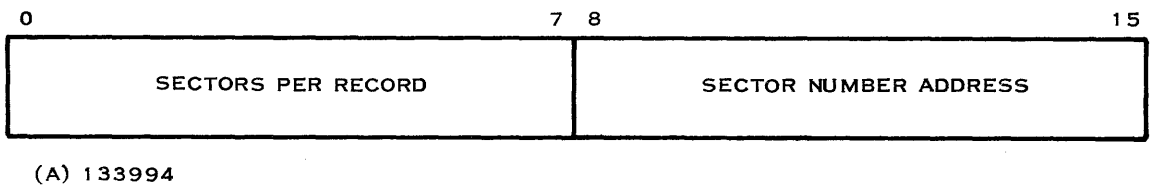


Figure 1-16. Control Word W2

1.7.3.1 Bits 0 through 7, Sectors Per Record. A disk can be formatted into variable length data records with a fixed number of sectors per record for a given track. Bits 0 through 7 specify the number of sectors per record. The number of sectors per record multiplied by the number of records per track will not exceed the fixed number of sectors per track of a particular disk drive.

1.7.3.2 Bits 8 through 15, Sector Address. This field selects the sector number at which the controller starts a read or write operation. The controller adds the sectors per record (bits 0 through 7) to the starting record address to calculate the address of subsequent data records on a track when multiple records are transferred. The range of sector addresses is 00_{16} through 13_{16}.

NOTE

If the sectors per record for a track does not equal one, then the programmer must be sure that sector addresses that correspond to record boundaries are used.

A sector address larger than the maximum sector address results in a timeout status because the controller cannot find a starting sector number at which to start executing the command. A SECTORS PER RECORD command exceeding maximum track size will be detected on initialization and will cause the controller to trap to command timeout status.

1.7.4 CYLINDERS, W3. The cylinder address is selected by bits 0 through 15 of W3. Figure 1-17 illustrates W3. The valid number range is 0000_{16} through 0197_{16}. An invalid cylinder address results in a termination and unit error controller status being set. The disk status (W0) will indicate seek incomplete.

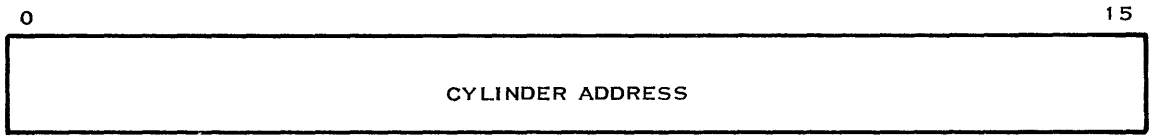


Figure 1-17 Control Word W3

1.7.5 WORD COUNT, W4. The word count is controlled by control word W4 as shown in figure 1-18. For data commands, this field selects the number of 16-bit data words to be transferred between the disk and the TILINE. The number of words is limited by the available TILINE memory and the disk memory from the starting disk address to the last sector of the last track. An attempt to transfer from a nonexistent TILINE memory results in a TILINE timeout status for the controller. For a WRITE FORMAT command, this field specifies the record word count.

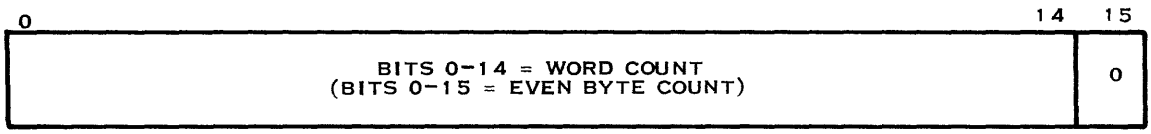


Figure 1-18. Control Word W4

1.7.6 LSB MEMORY ADDRESS, W5. The LSB memory address is determined by W5 (figure 1-19). By the use of this control word, the software selects the 15 least significant bits (LSBs) of the TILINE memory address for the starting address of a data transfer. The controller fetches or stores data through the TILINE bus at sequential addresses until the word count decrements to zero. The CPU byte selection bit (bit 15) is ignored by the controller.

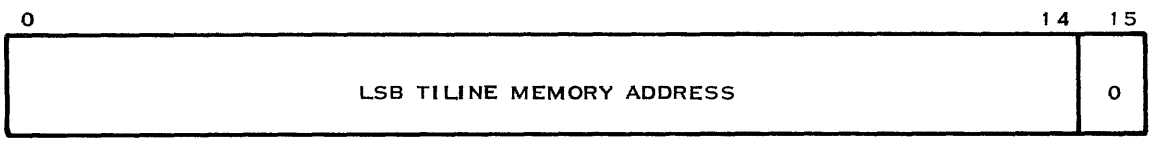


Figure 1-19. Control Word W5

1.7.7 UNIT SELECT AND MSB MEMORY ADDRESS, W6. Refer to figure 1-20. A disk controller may operate two drives, each with two disk platters (one fixed, one removable cartridge). Each platter is assigned an individual logical unit number. Even though the two platters in one disk drive share the same spindle, head carriage, and disk drive electronics, they are treated as distinct units from a programming point of view. Thus, there is no spillover of records from one platter to another, though there is automatic surface and cylinder switching within each platter. Record spillover between a fixed and a removable platter would inhibit transportability of programs and data.

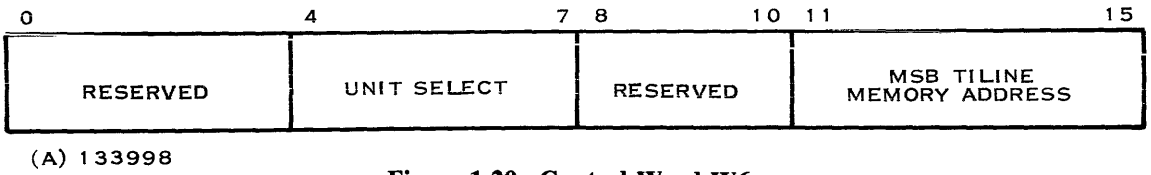


Figure 1-20. Control Word W6

1.7.7.1 Bits 4 through 7, Unit Select. The position-coded bits in the unit select field (W6, bits 4-7) specify the platter selected for the current operation. Only one platter can be selected at a time, as follows:

Logical Unit Number	Bit	Selected Disk Platter*
0	4	Disk drive A, fixed disk
1	5	Disk drive A, cartridge disk
2	6	Disk drive B, fixed disk
3	7	Disk drive B, cartridge disk

*These are the standard assignments. A jumper option allows logical unit number reversal between the two platters of a drive.

1.7.7.2 Bits 11 through 15, MSB Memory Address. This field selects the five most significant bits (MSBS) of the TILINE memory address. These five bits are prefixed to the 15 LSBs of memory address in W5 to complete the 20-bit TILINE address.

1.7.8 INTERRUPT AND CONTROLLER STATUS, W7. The interrupt and controller status field, shown in figure 1-21, provides error information and controller status information to the TILINE bus. Bits 0 through 4 are used primarily to report controller completion and error information. Bits 7 through 15 are used to convey the error status information about the controller. The following paragraphs describe individual bits and their functions.

1.7.8.1 Bit 0, Idle. Bit 0 is logic zero when the controller is busy (performing a sequence, etc.). The software clears bit 0 to activate the disk controller and to start execution of the command bits (bits 5 through 7) of W1. When a command is successfully completed, or terminated because of an error condition, the disk controller sets bit 0 to logic one. At the same time, the controller sets bit 1 of this field for a successful completion, or sets bit 2 if the operation is terminated as the result of an error condition.

1.7.8.2 Bit 1, Complete. Bit 1 is set when a command is completed without encountering an error. The bit may be reset by the software when servicing the interrupt.

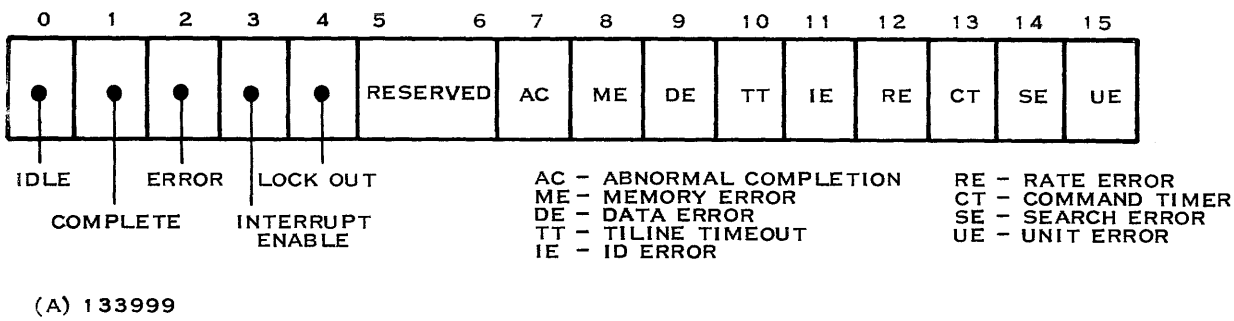


Figure 1-21. Control Word W7

1.7.8.3 Bit 2, Error. Bit 2 is set by the controller when an operation is terminated as the result of an error condition. This bit may be reset by software when servicing the interrupt or the status that was generated.

1.7.8.4 Bit 3, Interrupt. Bit 3 enables the controller interrupt when the complete bit (bit 1) or the error bit (bit 2) is set. This interrupt enable does not affect the unit attention interrupts which are controlled by the attention mask of W0.

1.7.8.5 Bit 4, Lockout. Bit 4 is set to logic one by the controller after W7 is read while the controller is idle. This bit is intended for use with multiprocessor systems, to notify other processors that the next disk operation is reserved.

Bits 5 and 6 are reserved.

1.7.8.6 Bits 7 through 15, Controller Status. Bits 7 through 15 of W7 are controller status bits that represent the status of the controller after a command has been executed. The bits contain valid information when the error bit (bit 2) is set. A special case exists when a self-test error is detected. When a self-test error occurs, all error status bits of R7 (bits 7 through 15) are set.

Bit 7, Abnormal Completion Error (AC). Bit 7 is set if a disk operation is terminated because an I/O reset, power failure warning, or master power reset was detected on the TILINE bus. (This bit is set when the 990 computer is powered-up.)

Bit 8, TILINE Memory Error (ME). This bit is set after completion of one of three disk commands: WRITE DATA, WRITE FORMAT, or WRITE UNFORMATTED, when it has been determined that a memory error occurred during the time that data was being transferred from the TILINE bus to the disk controller. (This is normally a parity error.)

Bit 9, Data Error (DE). This bit is set during a disk read operation if any of the calculated cyclic redundancy check (CRC) characters do not match the check character read from the disk data record(s). This means the CRC did not compare because of a parity error on the disk. All data transfer operations are terminated after a data error is encountered.

Bit 10, TILINE Timeout Error (TT). This bit is set if the controller addresses a nonexistent memory address, if a slave fails to respond or the controller cannot get bus access. TILINE timeout causes command termination. The timeout period is 20 ± 2 microseconds from the time TILINE access is requested.

Bit 11, ID Word Error (IE). This bit is set when an ID word comparison error occurs during ID verification of a READ DATA or WRITE DATA command. Verification includes comparison of ID words 1 and 2 and CRC checking of the three words. One hardware retry is attempted if an ID error occurs. If the retry fails, the command is aborted and error status is set.

Bit 12, Rate Error (RE). This bit is set when a timing error is encountered in the transfer of data between the TILINE master control and the disk interface:

1. During a read operation, the disk interface exceeds the capacity of the first-in, first-out (FIFO) data buffer.

2. During a write operation, the disk interface empties the FIFO data buffer before completing the writing of a data sector.

Bit 13, Command Timer Timeout (CT). This bit is set when the 200 ± 20 millisecond command timer expires before an operation is completed. The timer acts as a dead-man timer which is reset by the controller during normal execution of lengthy operations or while cycling in the IDLE loop.

Bit 14, Search Error (SE). Bit 14 is set when the controller does not detect a sync character ($6E_{16}$) within one physical sector while attempting to read from the disk. The controller attempts one retry before commanding abortion.

Bit 15, Unit Error (UE). The unit error status bit (bit 15) is set when an operation is terminated because of a disk drive error. The disk status word, W7, can be examined by software to determine the cause of the unit error. The following may cause a unit error:

a. Unit not ready

b. Unit off-line

c. Unit unsafe

d. Seek incomplete

e. Write operation is attempted on write-protected unit.

1.8 DISK CONTROLLER BASIC COMMANDS

A three-bit field in control word W1 specifies the basic operation which the controller is to perform. The basic commands are:

- STORE REGISTERS
- WRITE FORMAT
- READ DATA
- WRITE DATA
- READ UNFORMATTED
- WRITE UNFORMATTED
- SEEK
- RESTORE

These commands are not actually executed until the last word (W7) of the control block is loaded into the disk controller, and a controller self-test is performed.

1.8.1 STORE REGISTERS. The device service routines in Texas Instruments standard operating systems have been generalized to work with a number of different disk storage systems including the DS31, DS10, DS25, DS50, and DS200. Although the control word structure for all these systems is basically the same, disk operating parameters, such as words per track and cylinders available per logical unit, vary from system to system. The operating system needs access to these operating parameters in order to properly format records and manage the task roll-in and roll-out sequences.

The STORE REGISTERS command provides a means for the operating system software to interrogate a disk system to determine the critical parameters of the system.

A STORE REGISTERS command causes the disk controller to perform an extended self-test and then send three words to 990 memory, starting at a memory address specified by the control words. The three words, figure 1-22, contain the following information:

- Word 1. This word contains the total number of formatted words that can be recorded on a disk track. The number is $3840_{10} = 0F00_{16}$.

- Word 2. This word contains the sectors per track and the number of words of overhead per record to be used in the calculations of the format parameters. Bits 8 through 15 of this word specify the number of overhead words per record. This is equal to $48_{10} = 30_{16}$ for the disk drive. Bits 0 through 7 of this word specify the number of sectors per track, which is $20_{10} = 14_{16}$.

  For a DS10 disk system then, store registers - word 2 is 1430_{16}.

- Word 3. This word contains the number of tracks per cylinder and the number of cylinders per logical unit. A logical unit is equivalent to one fixed disk platter or one removable disk cartridge. Each DS10 disk drive contains two logical units.

Item	Bits	Value for DS10
Tracks/Cylinder	0-4	$02_{10} = 02_{16}$
Cylinders/logical unit	5-15	$408_{10} = 198_{16}$

The composite content of word 3 is 1198_{16}.

Table 1-5 is an example of an eight-word control block which will cause the disk controller to perform a store registers operation.

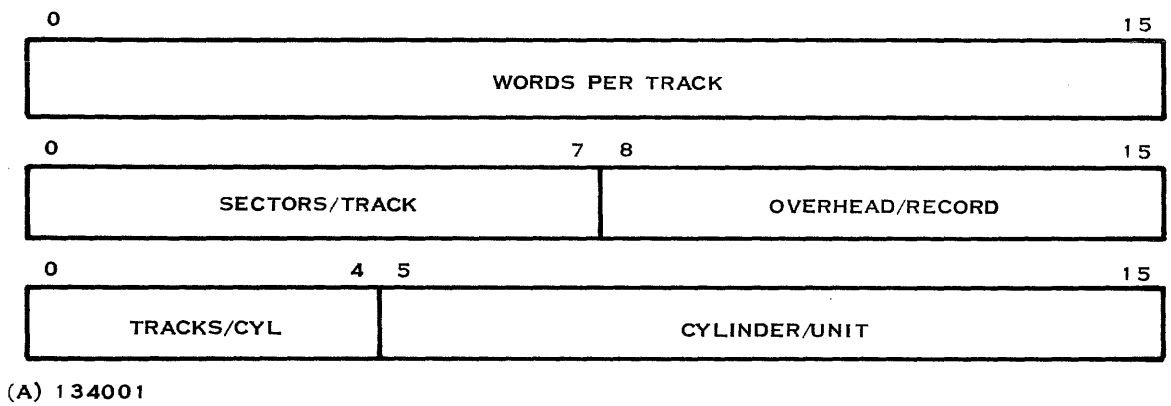


Figure 1-22. Store Registers Data Format

Table 1-5. Example of Control Words for STORE REGISTERS Command

Word	Data	Comments
0	0000	Clears the attention mask bits
1	0000	Command = STORE REGISTERS
2	0000	Not used
3	0000	Not used
4	0006	Three words
5	1000	Put three words into memory starting at TILINE address 0080_{16}
6	0800	Unit 0[1]
7	0800	Set lockout. Reset idle and all status bits (1800_{16} may be used if a command termination interrupt is desired.)

Note:
[1]A unit does not have to be selected; but if no unit is selected, the disk status after the command is complete will have the Not Ready and Off Line status bits set.

1.8.2 WRITE FORMAT COMMAND. The WRITE FORMAT command is used for formatting a new disk or for reformatting an existing disk. One complete track is formatted per command.

Formatting a track consists of writing record identification headers and temporary filler data on the track. A sector is the smallest unit of storage which can be assigned to a record. If the sectors per record parameter (W2, bits 0-8) specifies one sector per record, then the write format operation records a record identification header at the beginning of every sector on the track. If two sectors per record are specified, the operation writes headers at the beginning of alternate sectors, and so on.

The selection of a sectors-per-record parameter is a trade-off between the amount of disk overhead, which is a maximum at one sector per record, and the amount of disk space which is wasted by records which are shorter than the allocated storage space.

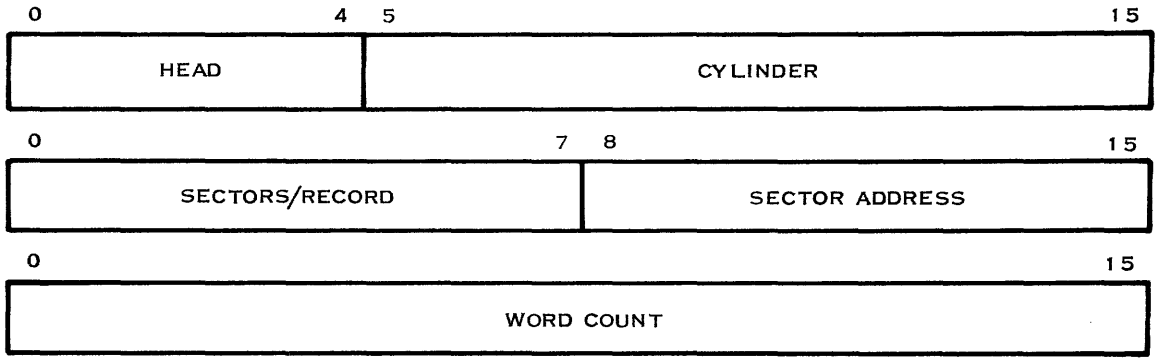
The head address (0 or 1), cylinder address (0-407), sectors per record (1-20), and maximum record size (word count) are supplied to the controller in the block of control words. A write format operation always starts at sector 0, so the sector address (W2, bits 8-15) is ignored.

The TILINE memory address (W5 and part of W6) gives the controller a memory location for the filler word which is to be written into all the data record areas.

Figure 1-23 shows the format of the three-word record identification headers. The sector address is derived dynamically from the drive as the disk rotates, and a different value is placed in each header. The head address, cylinder address, sectors per record parameter and word count are the same for all identification headers for a track.

The disk controller records a gap of all clock pulses and a synchronization character before each identification header and data record. It also appends a cyclic redundancy check (CRC) character to the end of each header and data record.

The controller automatically reads back the record identification header and verifies it against the CRC character and the current record parameters before performing a read data or write data operation in the specified sector(s).



(A) 134002

Figure 1-23. Record Header Data Format

Table 1-6 is an example of the control words required for a WRITE FORMAT command.

Table 1-6. WRITE FORMAT Command Example

Word	Data	Comments
0	0000	
1	0101	The command is WRITE FORMAT; the surface address is = 1
2	0300	The record will be three sectors long. The sector address is zero (0000)
3	00CA	Cylinder address selected is CA_{16}
4	03D8	Word count = Maximum for three sectors/record
5	1000	Memory address
6	0800	Unit 0
7	1800	Use interrupts and leave lockout set.

1.8.3 READ DATA COMMAND. The READ DATA command identifies a record location, specifies how many words are to be transferred from this record, and gives the starting address of a memory buffer area that is to receive the data read from the disk.

After performing the self-test, the controller checks disk drive status, seeks to the specified cylinder address (W3), selects the head (W1, bits 10-15), and searches for the starting sector address (W2, bits 8-15). When the starting sector comes under the heads, the controller reads the record identification header, verifies the CRC character, checks the first two header identification words against the parameters in the READ command, and stores the record word count (ID header word 3).

The read head is turned off during the gap period following the header, and is reenabled preceding the data area. When the synchronization character is detected, the controller starts assembling 16-bit data words and transmitting them to 990 memory, starting at the address specified in W5 and part of W6.

NOTE

The data transfer to memory may be suppressed by the transfer inhibit (TIH) bit in W1.

As each word is transferred, the record word count originally supplied in W4 is decremented.

When the controller encounters the end of a record but the remaining transfer word count is nonzero, the controller automatically continues reading data on the next sequential record of the track if it exists. The new record ID is checked before continuation of data gathering.

When the remaining transfer word count is zero but the controller has not encountered the end of a record, the controller stops transferring data words across the TILINE bus but continues to read data from the disk until the end-of-record is encountered so that the CRC character can be checked before loading status.

When the controller encounters the end of a track and the remaining transfer word count is nonzero, the controller automatically increments the head address to the next track; reads the ID words for the first sector (00) of that track; verifies the contents of ID words 1 and 2; stores the contents of ID word 3; and verifies the CRC character following the ID words. It then looks for the sync character, continues reading data from disk, and begins transferring data over the TILINE bus again.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, the controller automatically seeks to the next cylinder and selects head address zero for the new track. It then reads the ID words for sector 00, verifies the contents of ID words 1 and 2, and stores the contents of ID word 3. Next it verifies the CRC character following the ID words, looks for the sync character and continues to read words from the disk and transfer them to the TILINE bus if Transfer Inhibit is not specified. If the end of the last cylinder is reached, and the remaining word count is nonzero, the operation will terminate with Unit Error.

Table 1-7 is an example of the control words associated with a read data command.

Table 1-7. Example of READ DATA Command

Word	Data	Comments
0	0000	Clear the attention mask bits
1	0200	Read surface 0
2	0300	Three sectors/record, start on sector 0
3	0000	Cylinder 0
4	2000	1000_{16} words
5	0000	TILINE memory address = $F8000_{16}$
6	021F	Unit 2
7	0	Do not use interrupts or lockout

Note:
In this example, the format of all of the tracks read must be three sectors per record or an error will be flagged.

1.8.4 WRITE DATA COMMAND. The WRITE DATA command causes the controller to record data on a previously formatted track, or to write over a previous record.

After self-test, the controller uses the unit select, head address, cylinder address and sector address parameters from the control words to locate the starting sector of the record.

The controller reads the three-word record ID header and checks the header CRC character. The address and sectors per record parameters in header words one and two are checked against the parameters supplied with the WRITE DATA command. The record word count is stored for later use. If the ID words fail to compare, the operation is terminated with an ID error status bit.

Assuming that the ID comparison is correct, the controller disables the read head, and after a delay, enables the write and straddle erase heads. A predetermined gap of all clock pulses is recorded followed by a synchronization character which identifies the beginning of the data area. Then the data is written on the disk.

The data words are read from 990 memory, starting at the TILINE address supplied in W5 and part of W6. The word count specified by W4 is decremented each time a 16-bit data word is transferred from memory to the disk controller. The record word count read from header ID word 3 is also decremented.

Data is written on the disk until the specified number of words have been transferred unless a terminate condition is encountered. When the number of words to be transferred is greater than the number of words per record, the controller continues to the next sequential record. The next sequential record starts at the sector number whose value is equal to the beginning sector number of the last record plus the number of sectors per record.

When the transfer word count is less than the record word count, the controller fills the remainder of the record with zeros until the record word count has been decremented to zero.

When the controller encounters the end of a track for a cylinder and the remaining transfer word count is nonzero, it automatically increments the head address to the next track, starts reading ID of sector zero, verifies the contents of ID words 1 and 2, and stores the contents of ID word 3. It then verifies the CRC character following the ID words and continues the write operation after the appropriate delay.

When the controller encounters the end of a cylinder and the remaining transfer word count is nonzero, it automatically seeks to the next cylinder and selects head address zero for the new track. The controller starts reading the ID for sector zero, verifies the ID words, and continues the write operation at sector zero.

1.8.5 READ UNFORMATTED COMMAND. The READ UNFORMATTED command allows the 990 computer to read whatever is recorded on the disk, without regard to sector boundaries, record formats, record boundaries, or end of track boundaries. READ UNFORMATTED is primarily a diagnostic tool.

Starting at a disk address specified in the control words, the READ UNFORMATTED command causes the controller to read data and transfer it to main memory until the word count (W4) is decremented to zero. A check for the CRC character is performed at the end of the operation. If the CRC is not correct, error status will be reported.

One useful application of the READ UNFORMATTED command is in determining the format of an unknown track. For this case, the command words should specify the track address and select sector 0 with a word count of three. If a write format operation has ever been performed on that track, there will be a three-word record ID header and a CRC character at the beginning of sector 0. The READ UNFORMATTED command will transfer the three header words to 990 memory and correctly perform the CRC check.

A CRC error is to be expected during a READ UNFORMATTED operation, except for two special cases. These cases are:

- If the track was recorded with a WRITE UNFORMATTED command with parameters corresponding exactly to the read unformatted operation
- The special case of record-header checking previously described above.

Table 1-8 shows an example of a READ UNFORMATTED command used to read the three header words and the header CRC character to 990 memory.

Table 1-8. READ UNFORMATTED Command Example

READ UNFORMATTED Command

Word	Data	Comments
0	0000	
1	0400	Unformatted read
2	0001	Sector/record not used. Sector address = 1
3	0000	Cylinder 0
4	0006	3_{10} words
5	1000	TILINE memory address = 00800_{16}
6	0400	Unit = 1
7	1800	Use interrupts and lockout

Data Received from Command

Word	Data	Comments
0	0000	Track 0
1	0101	Sector/record = 1, sector = 1
2	0002	4 bytes, 2 words

1.8.6 WRITE UNFORMATTED COMMAND. A WRITE UNFORMATTED command transfers data onto the disk, starting at the specified sector, without regard to the record header formats described previously. That is, the controller does not read or check any record headers. This operation is not used with Texas Instruments standard operating system software. The WRITE UNFORMATTED command could be used in disk track verification. In this case, the programmer would use a WRITE UNFORMATTED command to write on the entire track, and a READ UNFORMATTED command to verify that the data can be recovered without any errors.

A data CRC character is recorded during a WRITE UNFORMATTED operation.

1.8.7 SEEK COMMAND. The SEEK command causes the disk controller to implement initialization and run a short diagnostic self-test. The command does not issue the new cylinder address to the disk drive. Instead, the command executes to termination and completes normally if no error conditions are detected. The actual seek is not performed because the heads for the fixed and removable disks move together as a unit on the same head carriage assembly. Independent seeks that would be issued in the overlapped mode between the two head assemblies are a physical impossibility. By accepting the command but not issuing it to the disk drive, the software command structure remains compatible with other disk systems. Table 1-9 is an example of the SEEK command.

Table 1-9. Example of a SEEK Command

Word	Data	Comments
0	0000	
1	0600	Seek surface is not used
2	0000	Sector/record and sector and address are not used
3	0003	Cylinder = 3
4	0000	Word count is not used
5	0000	Memory address is not used
6	0100	Unit = 3
7	1800	Use controller interrupts and lockout

1.8.8 RESTORE COMMAND. The RESTORE command is required if a seek incomplete disk status is detected by software or if an unsafe disk status occurs. The RESTORE command positions the heads of the selected disk drive over cylinder zero, and clears the fault logic in the drive.

Before issuing the RESTORE command, the off-line status is checked. If the drive is off-line, the RESTORE command is aborted and the unit error status in R7 is set. If the drive is on-line, the RESTORE command is issued to the drive and the controller executes a 0.5-second delay loop. Following the delay, the controller issues an interrupt to the computer if either the interrupt bit is set or one of the attention mask bits is set. Overlapped restores are not allowed between the fixed and cartridge disks because the heads are attached to the same carriage assembly and move together as a unit.

1.9 DISK DATA CONFIGURATION

Each disk platter has two surfaces for data recording, as shown in figure 1-24. The upper platter is the top-loading 5440-type disk cartridge and the lower platter is the fixed disk which is built into the DS10 disk drive.

Figure 1-25 shows the organization of one recording surface. A sector/index transducer provides the disk drive electronics with one index mark and 20 sector marks per revolution. The disk drive electronics uses the sector and index marks to develop a sector address which identifies the sector which is under the read/write heads. The sector mark, index mark, and sector address are supplied to the disk controller, which uses these inputs for organizing and locating disk data.

A track is the data path which rotates under a read/write head, with the head carriage stationary. Head carriage motion toward and away from the spindle divides the recording surface into 408 tracks (0-407) with empty guard bands between tracks to prevent crosstalk. The head carriage follows a precision scale to determine track location.

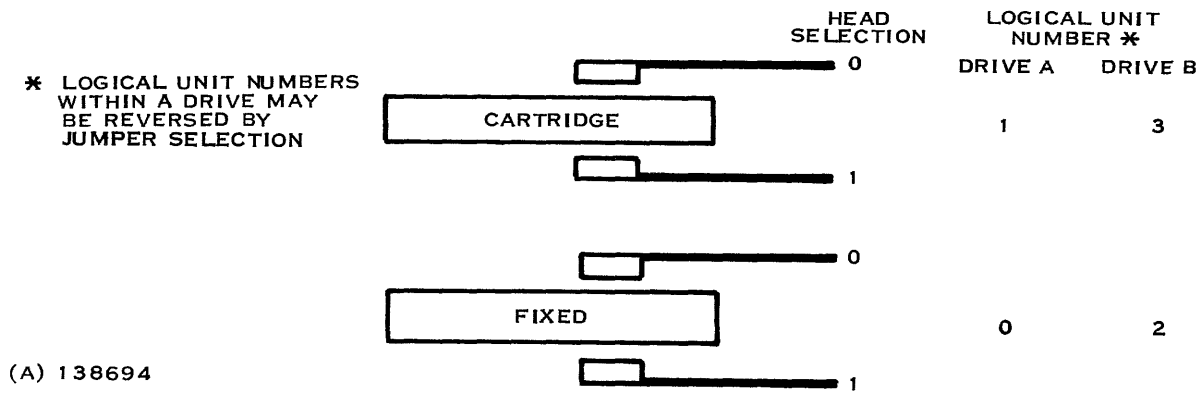


Figure 1-24. Disk Platter and Read/Write Head Organization

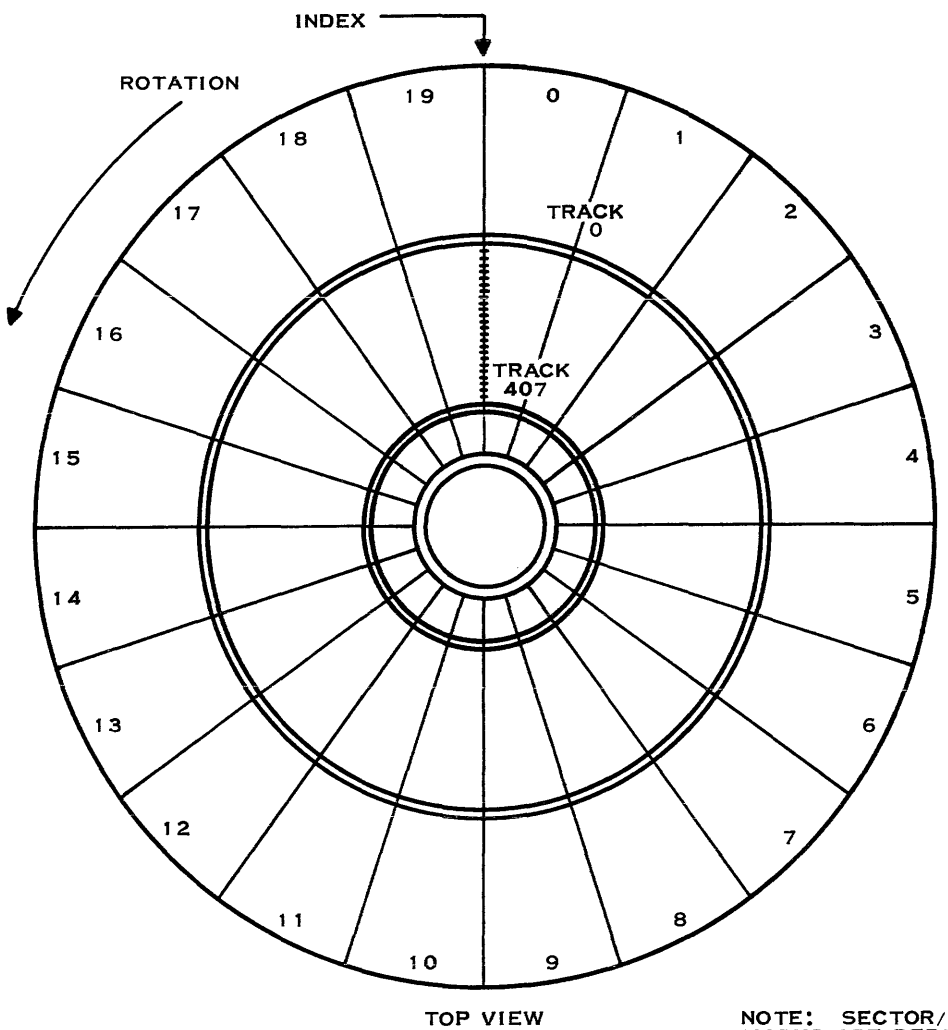


Figure 1-25. Sector and Track Organization

The term "track" refers to a single surface. The term "cylinder" refers to all the tracks which could be recorded by electrically switching heads without moving the head carriage. For the DS10 disk drive, a cylinder consists of two tracks, one on the upper surface of the platter, and one on the lower surface.

A track number and a sector number specify the smallest unit of disk storage which can be allocated to a data record. With the track organized into one sector per record, 288 data bytes may be recorded in one sector, and 5760 data bytes may be recorded on the track.

There is some formatting "overhead" associated with each record. The total space devoted to track overhead may be reduced by organizing the data into several sectors (20 maximum) per record. Sector per record formats may vary from track to track, but they remain constant within a track.

Figure 1-26 shows the organization of a record which is formatted as one sector per record. All records must start at a sector mark, no matter what the sector per record organization may be. The first 78 microseconds is devoted to the preidentification gap (gap 1), also referred to as the preamble. An all-zeros pattern (clock with no data pulses) is recorded in this gap. The gap compensates for any mechanical variations in sector transducer positioning or read/write head skew due to misalignment. The clock pattern synchronizes the phase-locked clock/data separator in the disk drive electronics. A $6E_{16}$ (01101110) synchronization character notifies the controller that the gap has ended and that valid data has started. The controller starts grouping serial read data into 16-bit words upon detection of the synchronization character. Three record identification words and an error check word follow the synchronization character. This record identification header was placed on the disk when the disk was formatted. It is not changed during read data or write data operations. It is read in order to verify that the controller, disk drive, and the disk agree on the parameters of the record.

Another gap (gap 2) separates the header and the beginning of the data record. Gap 2 consists of 88 zeros, approximately 35.2 microseconds of all clock pulses. Write head turn-on transients may be picked up in this gap, so there is a window in which the read circuits are inhibited.

The clock pulses at the end of gap 2 are rerecorded during a write operation, in order to properly synchronize the clock/data separator during a future read operation.

Another $6E_{16}$ synchronization character identifies the start of the data. At one sector per record, 144 words may be recorded. Much larger records may be stored if the record spans multiple sectors. The last word is a cyclic redundancy check character, which is used during read operations to verify the integrity of the entire data storage and recovery operation.

A third gap, called gap 3 or the post-record gap, follows the data record. Gap 3 compensates for possible sector transducer and read/write head misalignment. Gap 3 prevents the end of the current record from overlapping the start of the next record.

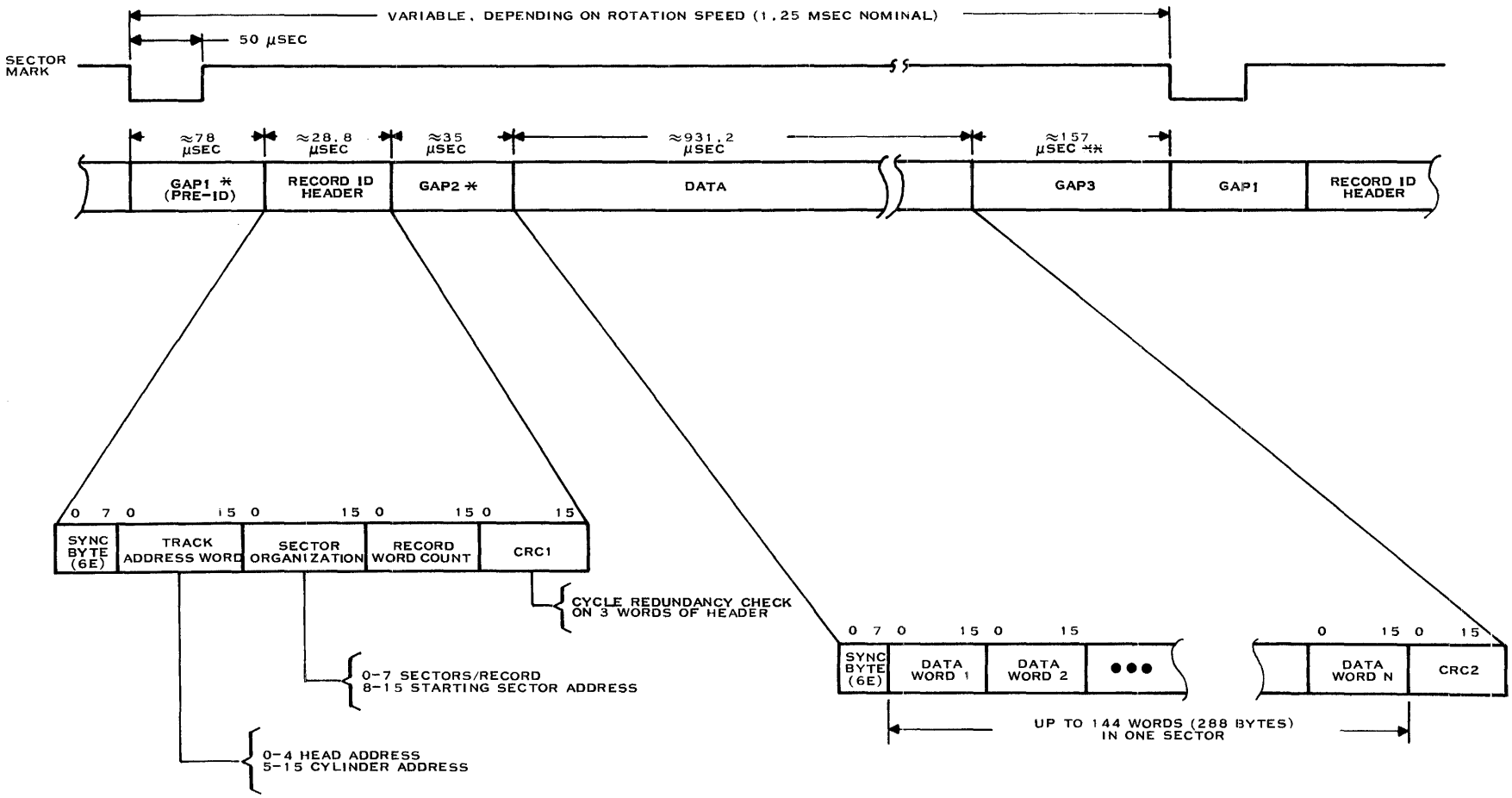


Figure 1-26. Sector Format — One Sector per Record

SECTION 2

THEORY OF OPERATION

This section describes the theory of operation for the Model DS10 Cartridge Disk Controller, part number 937505-1 (PWB) or part number 2262100-1 (fine line). Detailed circuit descriptions in this chapter are based on logic drawings 937502 (PWB) and 2262102 (fine line), which are included in Appendix G.

2.1 DISK CONTROLLER INTERFACES

Figure 2-1 shows the disk controller interface signals, grouped according to function. The left side of the figure shows the interface between the disk controller and the TILINE bus that runs through the 990 computer chassis.

The TILINE master and slave data transfer signals include:

- TILINE Address. Twenty bidirectional address lines used to define the location of data during a read or write operation.
- TILINE Data. Sixteen bidirectional data lines used to transfer data between the TILINE and the controller.
- TILINE Read. This signal is a read control signal when high, and a write control signal when low. It is developed by the TILINE master device that is in control of the bus.
- TILINE Go. Initiates data transfers between the TILINE and the controller on the high to low transition.
- TILINE Terminate. Indicates the operation of a TILINE slave has been completed.
- TILINE Memory Error. Indicates that a nonrecoverable error has occurred during a memory read operation.

The TILINE access control signals are used to coordinate the orderly sharing of bus resources among competing TILINE master devices. These signals include:

- TILINE Wait. Temporarily suspends the controller from using the TILINE.
- TILINE Acknowledge. When low, this signal indicates that some device has requested access to the TILINE, has acquired the next available access cycle, and is waiting for the bus to become available. When high, this signal indicates the next TILINE access is not reserved.
- TILINE Available. When low, this signal indicates that the TILINE is busy. When high, it indicates that no device is using the TILINE.
- TILINE Access Granted In. When high, this signal indicates that no higher priority TILINE master has requested use of the TILINE. When low, this signal prevents the controller from using the TILINE.
- TILINE Access Granted Out. This signal, when low, indicates the controller is requesting use of the TILINE and prevents all lower priority master devices from using the bus.

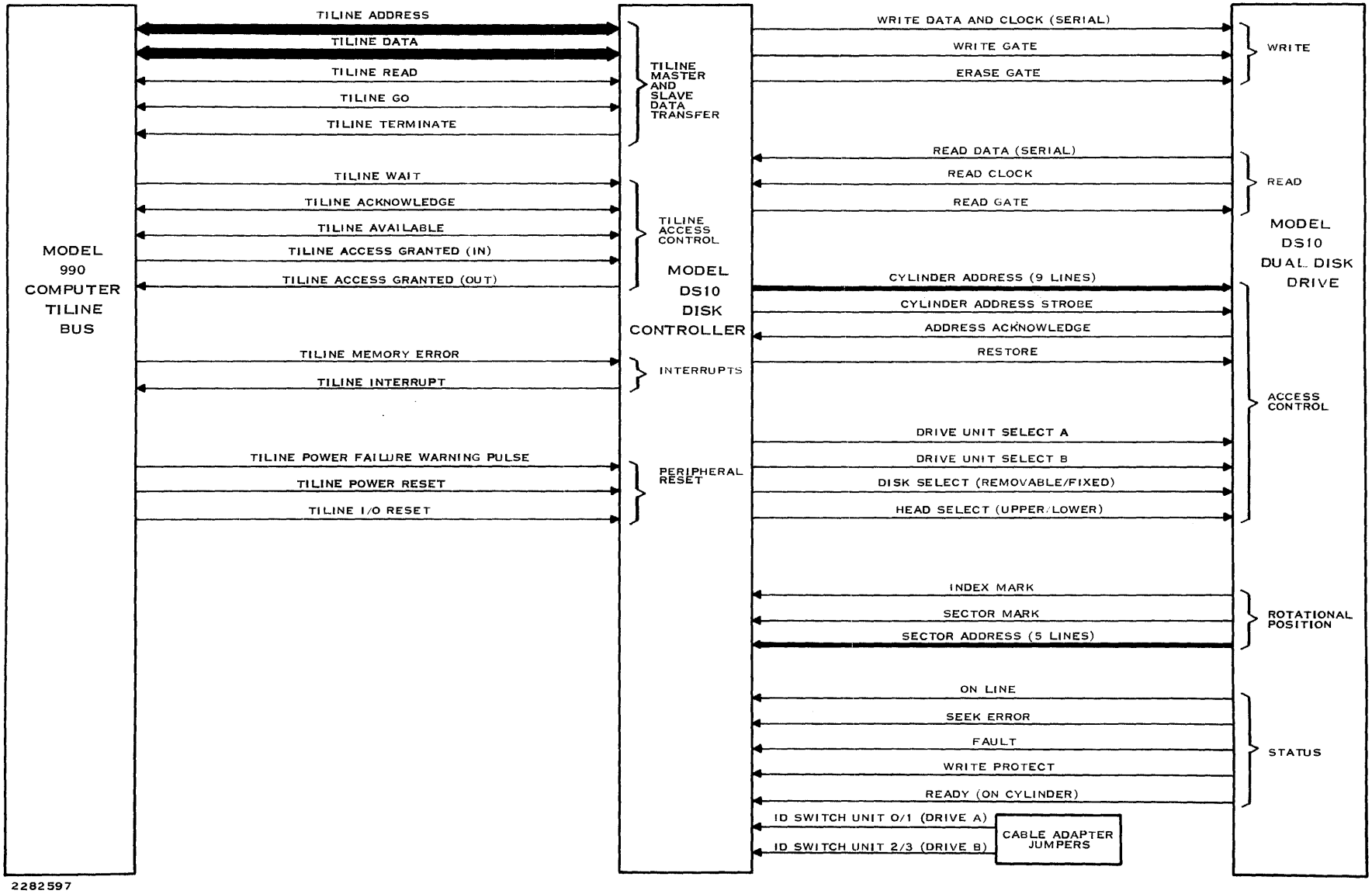


Figure 2-1. DS10 Disk Controller Interface Signals

There is one data interrupt related to controller operation:

- TILINE Interrupt. This is the general interrupt from the controller slot location to the 990 processor.

The peripheral reset signals clear the controller and the disk drive to safe states in the event of an I/O reset instruction or a power shutdown. These signals are:

- TILINE Power Failure Warning Pulse. A signal preceding TLPWRES- that indicates a computer power-down sequence is in progress.
- TILINE Power Reset. This signal line goes low to reset the controller and all other TILINE devices. It is generated as part of the computer power-down and power-up sequences.
- TILINE I/O Reset. When this signal is low, it halts and resets all TILINE I/O devices. This signal is developed by the 990 processor.

The signals exchanged between the disk controller and the disk drive(s) fall into five categories; write, read, access control, disk platter rotational position, and drive status.

The write signals include:

- Write Data and Clock. Serial double-frequency (FM) waveform in which data and clock pulses are multiplexed on one signal line.
- Write Gate. An enabling command that allows the drive to supply write current to the specified read/write head.
- Erase Gate. An enabling command that turns on erase current to the straddle erase heads.

The read enabling signals include:

- Read Data. A serial bit stream separated from the clock bit stream by a clock/data separator circuit in the disk drive electronics.
- Read Clock. Clock pulses from the previously recorded write data and clock bit stream.
- Read Gate. Enables the disk drive read heads and read electronics.

The access control signals include all the signals necessary to select a drive unit, platter, head and track. These signals include:

- Cylinder Address. Nine lines that specify the required position of the head carriage.
- Cylinder Address Strobe. A pulse that loads the cylinder address into the disk drive electronics.
- Address acknowledge. Confirmation by the drive that a valid (0-407) cylinder address was accepted.
- Restore. A master clear command that clears the disk drive fault latches and address register, and runs the head carriage through a full stroke (forward to track 407, back to track 0).

- Drive Unit Select A and B. Lines that specify the first or second disk drive.
- Disk Select. Specifies the fixed or the removable disk drive.
- Head Select. Specifies the upper or lower surface of the disk platter.

The rotational position signals are used to keep track of the disk position as it rotates under the heads. It is important to note that the sector/index marks are sensed separately on the fixed and on the removable platter. The sector encoder for the fixed disk is hard-mounted on the spindle. The sector slots for the removable cartridge are built into a ring within the individual cartridge. The rotational position signals (which apply to the platter currently selected) are:

- Index Mark. Pulse that occurs once per revolution, at the beginning of sector 0.
- Sector mark. Pulse that occurs at the start of each sector (20 times per revolution). Serves as a timing reference and indicates that the current sector address is stable and valid.
- Sector address. Five-bit binary sector address supplied by the disk drive electronics derived from sector pulses.

The status signals from the selected disk are:

- On-Line. Drive power applied, disk up to speed, and other conditions (described with the disk interface logic).
- Seek Error. Fault detected in head carriage positioning.
- Fault. Generalized fault indication.
- Write Protect. Selected disk platter protected from write operations by WRITE PROTECT-FIXED or WRITE PROTECT-CART switch on disk drive front panel.
- Ready. Ready to start read or write with head carriage at specified cylinder, no faults detected.

The interface figure (figure 2-1) also shows the logical unit number reversing jumpers on the cable adapters.

2.2 DISK CONTROLLER BASIC BLOCK DIAGRAM DESCRIPTION

The Model DS10 Cartridge Disk Controller is a microprocessor-based "smart" controller that manages disk control and data transfers independently of the Model 990 computer after accepting a group of control parameters.

Figure 2-2 shows that the disk controller logic may be partitioned into three major functional groups: the TILINE interface, the microprocessor-based sequence controller (microcontroller), and the disk interface logic.

2.2.1 TILINE INTERFACE. The TILINE interface consists of the TILINE slave logic, the TILINE master logic, and the line drivers and receivers. The slave logic is activated when the 990 processor addresses one of the eight TILINE slave addresses that are assigned to the controller. These eight TILINE slave addresses are dedicated to control and status words W0-W7, and are used to load control words (TILINE slave write operation) or to request status words (TILINE slave read operation). The term "slave" is applied to these operations because the controller responds to an externally-supplied address and to a read/write command, much like a memory.

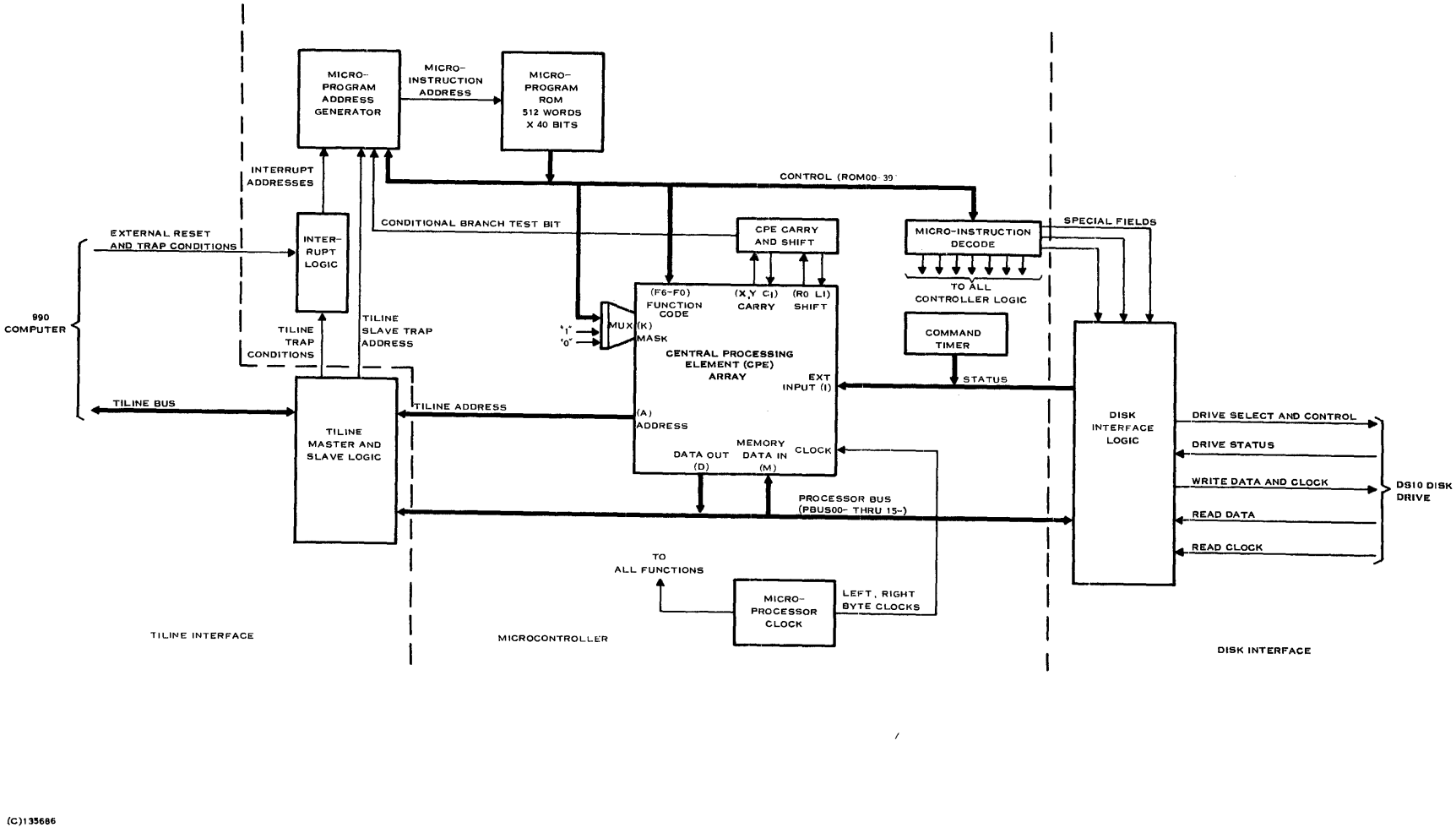


Figure 2-2. DS10 Disk Controller Simplified Block Diagram

The TILINE master logic is activated to transfer data between the disk drive and a specified (by control words) buffer area of 990 memory. The TILINE master logic requests and attains bus control, and manages the "handshaking" exchange of signals necessary to transfer each word.

2.2.2 MICROCONTROLLER. The microcontroller uses a 16-bit processor and a permanent on-board microprogram to control execution of the operations specified by control words W0-W7.

The processor is an array of eight 3002 central processing element (CPE) devices. Each high-speed, bipolar CPE is organized as a two-bit slice of a complete processor, including input buses, output buses, internal storage registers, and an arithmetic/logic unit. The CPEs are connected with external shift and look-ahead carry logic, in an array that can process eight-bit bytes or 16-bit words. The CPEs perform the add, subtract, complement, shift, store, mask and logical operations required by the microprogram.

The CPE array uses internal registers for storage of control word W0-W7 and also for the scratchpad storage necessary to maintain loop counters and store other operands and intermediate results. The CPE array does not have access to an external read/write memory for scratch pad purposes.

The main data transfer path through the disk controller is the 16-bit processor bus (P-bus), which links the TILINE line drivers/receivers, the CPE array and the disk interface. The CPE array can accept data from the processor bus or place CPE accumulator data on the bus, as commanded by the microprogram.

Disk controller internal status and disk drive status are supplied to the CPE array on the external input (I-bus) lines. The masking and bit-testing capabilities of the CPE array are used by the microprogram to sense the progress of ongoing operations and steer microprogram execution based on current conditions. A separate disk status word is available over the processor bus for the same purposes.

The mask input (K-bus) of the CPE array is used by the microprogram to load constants and masks into the CPE array.

The CPE address (A-bus) outputs are used to supply 16 bits of the 20-bit TILINE address during TILINE master cycles; i.e., when the controller is acting as a master to control data transfers to and from 990 memory.

The disk controller microprogram is burned into a group of 512-word read-only-memory (ROM) devices. Each microprogram instruction or microinstruction is 40 bits wide. The microinstruction is divided into multiple fields, each of which controls some aspect of TILINE interface, microcontroller, or disk interface operation. Fields within the microinstruction select processor bus sources and destinations, clock generation, CPE array left byte/right byte/full word mode, CPE function code, CPE mask inputs, disk drive control signals, and microinstruction address selection. This is only a partial list, but serves to emphasize the fact that the microinstructions are intimately involved in all aspects of disk controller operation.

The microprogram address generator selects each microinstruction from read-only-memory. The address generator can step through sequential addresses, branch conditionally or unconditionally, link to subroutines, and return conditionally or unconditionally to addresses stored in a four-word stack, or branch to predefined interrupt trap locations.

2.2.3 DISK INTERFACE. The disk interface logic performs the operations necessary to convert between the serial recording format required by the disk drive and the parallel formats imposed by the processor bus and TILINE bus, compensates for clock and data rate differences, checks data integrity, supplies drive control signals and monitors drive status and rotational position signals.

Figure 2-3 shows the major functional blocks of the disk interface. The 16-word first-in, first-out (FIFO) buffer compensates for the differences in data transfer rates between the TILINE (or the CPE array) and the disk. This is necessary because the TILINE is shared between multiple users and is not always instantly available, while the disk data rate is inflexibly fixed by the inertia of a rotating mass.

The serial/parallel shift register, like the FIFO, is used on both read and write operations. During disk read, the shift register assembles serial data into 16-bit parallel words. During disk write, the shift register accepts 16-bit parallel data from the FIFO and converts it to serial form.

The cyclic redundancy check (CRC) generator calculates a data integrity code during write operations, and transmits that code following the last data word of the record. During read operations, the CRC code is recalculated and checked against the previously recorded value. If they compare, the integrity of the entire write, store, and read operation is verified.

2.3 BASIC DATA FLOW

The following paragraphs describe data flow through the disk controller for five important cases.

2.3.1 DATA FLOW — LOADING COMMAND WORDS INTO THE DISK CONTROLLER. Refer to figure 2-4, which shows the data flow involved in loading command words W0-W7 into the disk controller. Each command word is sent from the 990 processor to the controller as a TILINE data word. The 990 processor acts as a TILINE master during these operations. It acquires control of the TILINE, supplies the TILINE address, the read/write control signal and the word to be sent to the controller. The controller acts as a TILINE slave, decoding the address and responding to the read/write signal by accepting a 16-bit word.

Each of the eight command words is assigned a unique TILINE address ranging from the TILINE base address to the base address +7 word addresses. The addresses are assigned in order; i.e., control word W0 is assigned the base address, W1 is assigned the base address +1 word address, and so on.

The disk controller microprogram has eight unique trap addresses assigned to write operations on control words W0-W7. The decoded TILINE address initiates the slave write trap for the particular command word. The microinstructions in the trap routine steer the TILINE data word onto the processor bus and command the CPE array to store the control word in the correct CPE scratch pad register. CPE scratch pad registers R0-R7 are assigned to store control words W0-W7, respectively.

The microprogram disables the TILINE slave logic after receiving a control word W7 with a zero in the idle bit, which initiates decoding and execution of the command.

The slave logic remains disabled until the controller has completed the commanded operation. Therefore, control words W0-W6 may be transmitted in any order, but W7 must be the last word.

2.3.2 DATA FLOW FOR DISK WRITE OPERATIONS. Refer to figure 2-5, which shows the simplified data flow for the disk write operations, write data and write unformatted. During a write data or a write unformatted operation, the disk controller is operating under its internal microprogram, using previously stored command words W0-W7 as parameters.

NOTE

During a write data operation, the controller reads back and verifies the record header prior to recording any data. That data flow is shown in figure 2-8. The data flow in this paragraph also does not apply to the write format operation.

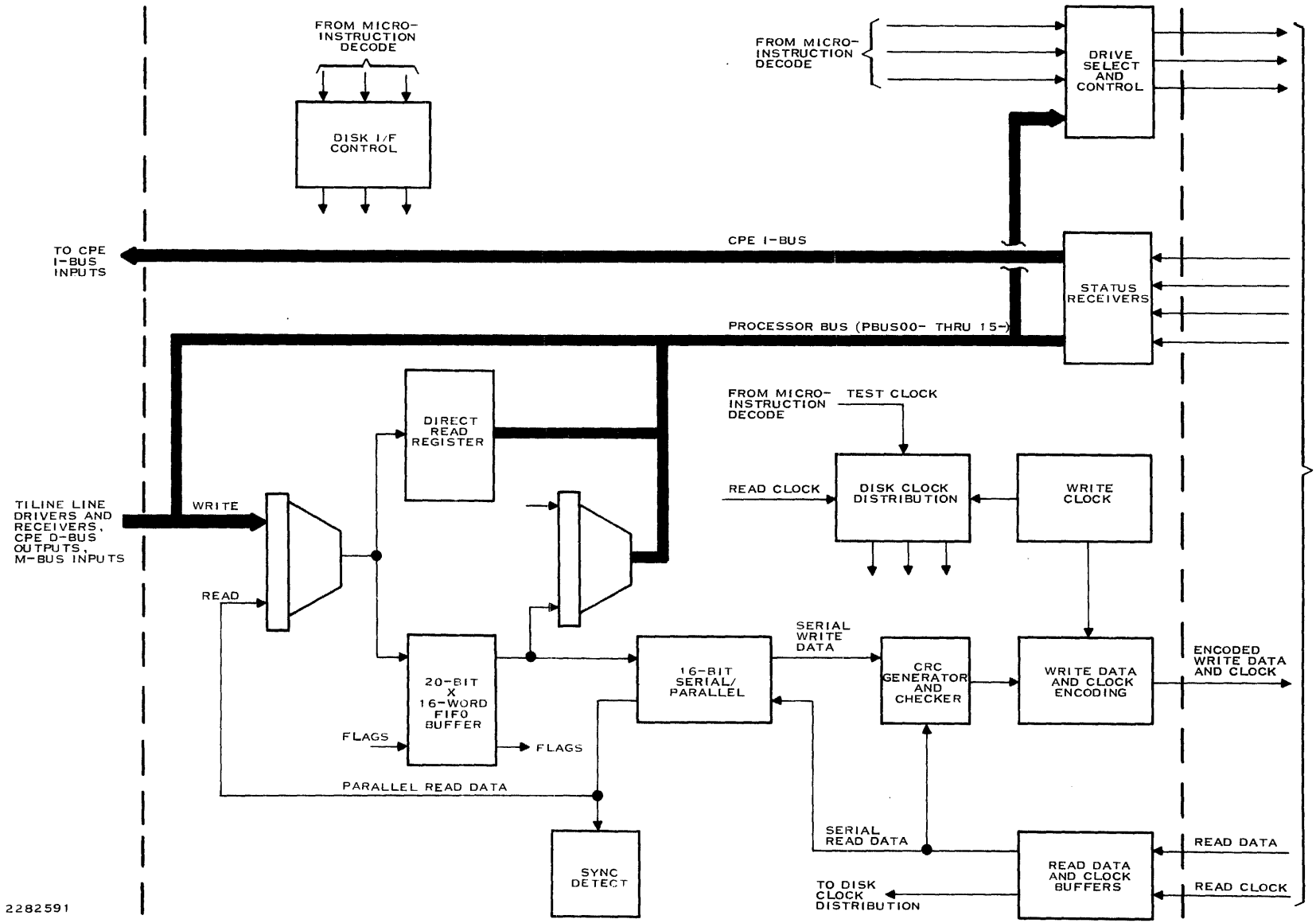


Figure 2-3. Disk Interface Simplified Block Diagram

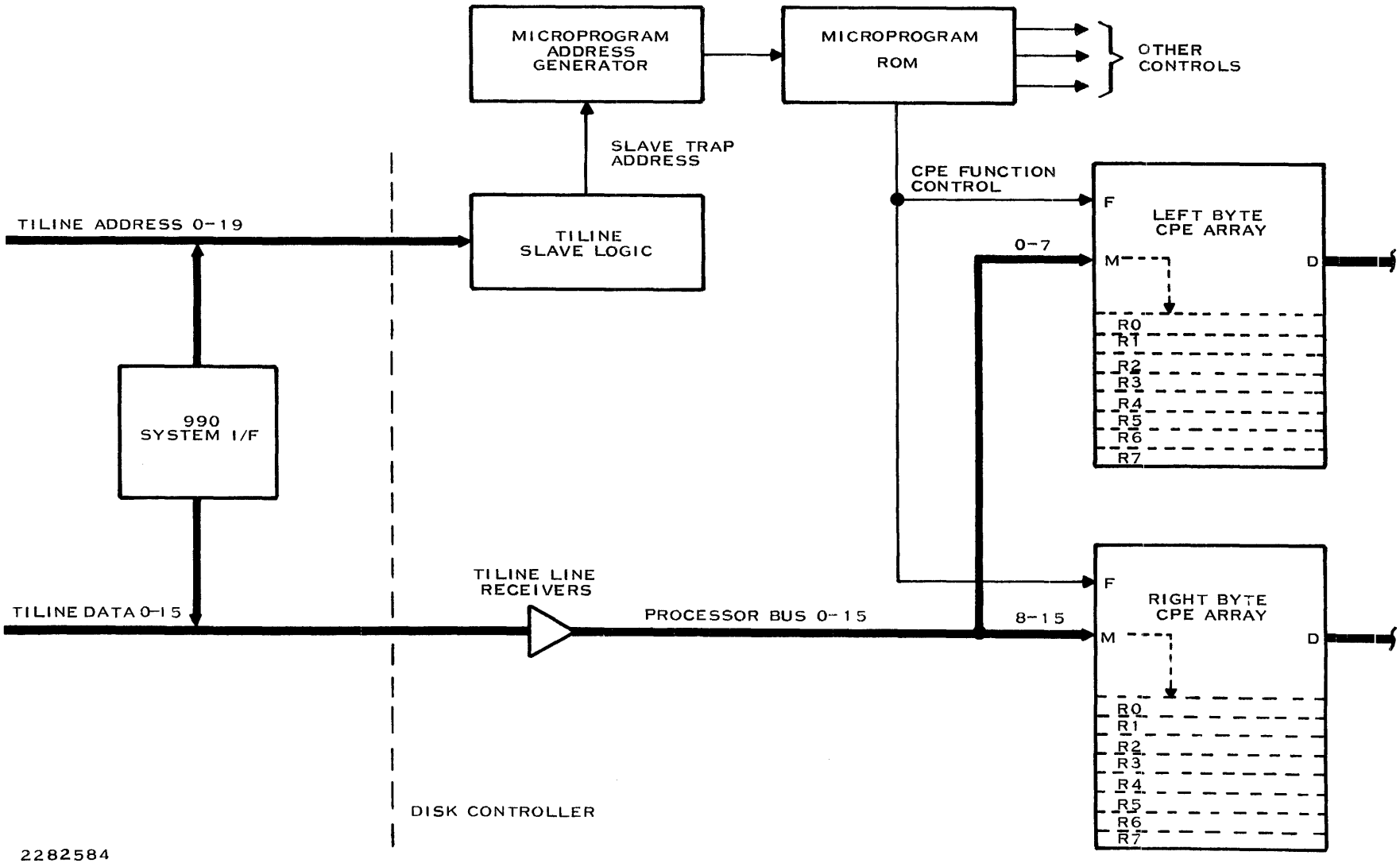


Figure 2-4. Simplified Data Flow — Loading Command Words Into the Disk Controller

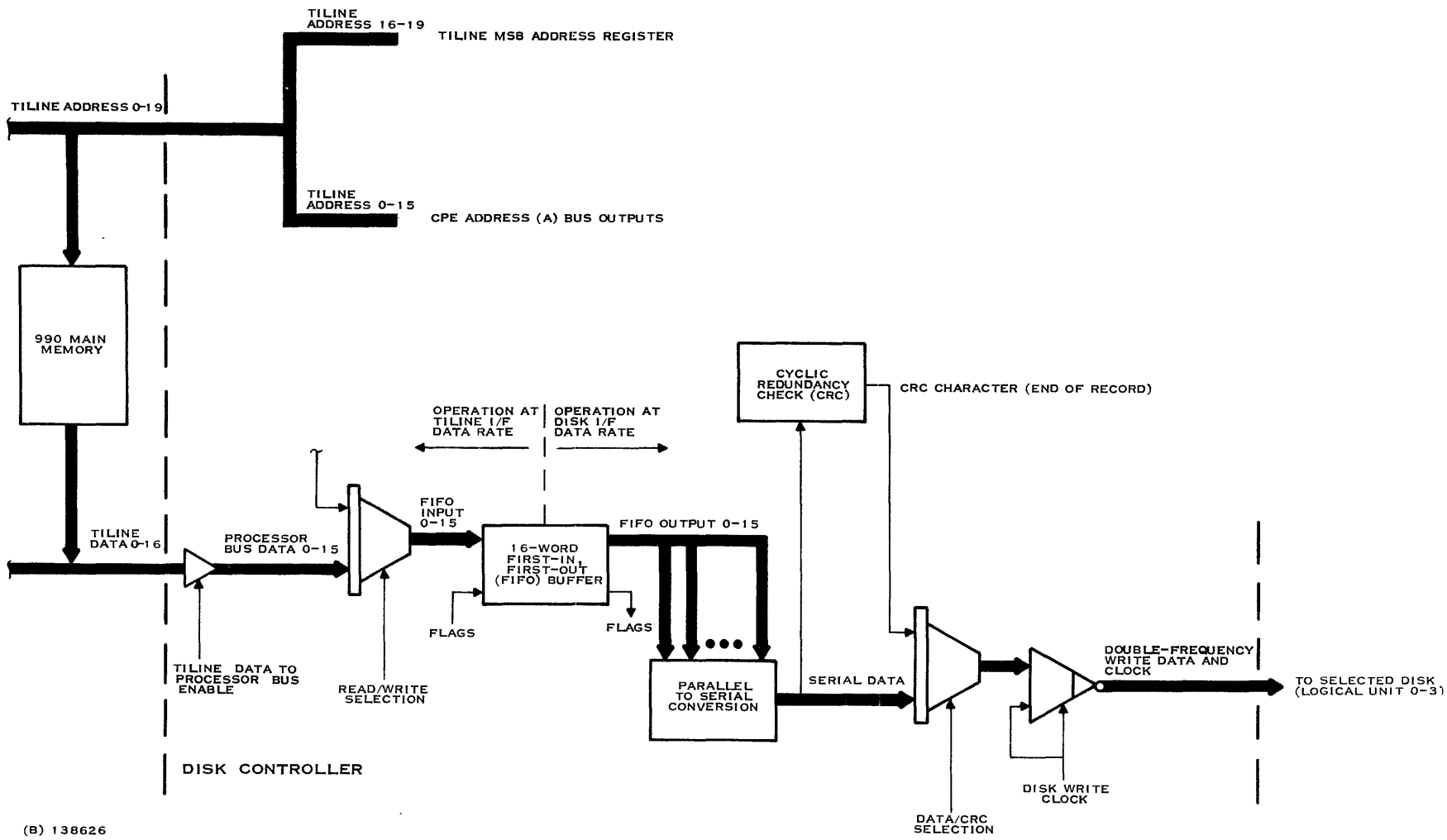


Figure 2-5. Simplified Data Flow for Disk Write Operation

The disk controller acts as a TILINE master to read the data from 990 memory and load it into the 16-word FIFO buffer. The initial TILINE address and the transfer word count for this operation are parameters supplied by the control words. The CPE array updates the TILINE address and decrements the word count as the operation proceeds.

The operation of requesting and obtaining access to the TILINE, transferring data, and relinquishing control of the TILINE, is called a TILINE master cycle. One TILINE master read cycle is performed for each data word that is to be recorded. Master cycles are initiated by the microprogram, based on such conditions as whether there is space available in the FIFO and whether the word count has been decremented to zero.

The FIFO serves as a buffer to adapt the variable data rate of the TILINE to the fixed data rate of the disk. All operations from the FIFO output to the encoded write data and clock output are synchronized to a crystal-controlled write clock oscillator.

The parallel-to-serial conversion occurs in the serial/parallel shift register. The CRC logic operates on this serial bit stream and, at the end of the transmission, the 16-bit CRC character is shifted out instead of serial data.

2.3.3 DATA FLOW FOR DISK READ OPERATION. Figure 2-6 shows the simplified data flow for the disk read operations, read data and read unformatted.

NOTE

The data flow in this paragraph does not apply to reading and verifying a record header prior to reading the record.

After the specified track and sector are located by the drive and the record header is checked against parameters supplied in the control words, the disk controller turns off the read gate for a short time to eliminate transient pickup, and then reenables it.

Read data and clock are supplied to the disk interface on separate lines by a phase-locked clock/data separator in the disk drive electronics. The all-clock (data zeros) waveform in the prerecord gap locks in the clock/data separator.

Read clock from the disk is used to clock all data operations between the read data buffer F/Fs and the FIFO input.

The shift register shifts serial data in, but no additional operations occur until the $6E_{16}$ synchronization character is recognized. At that point, the CRC generator is preset, a 16-bit counter is cleared, and the FIFO accepts the next 16-bit word assembled by the serial/parallel shift register.

The microprogram is notified (via the CPE I-bus) that data is available for transmission to 990 memory. The microprogram initiates a TILINE master write cycle each time there is a data word available in the FIFO when the I-bus bit is checked, as long as the transfer word count has not been decremented to zero.

If the transfer word count reaches zero before the end of the record, the controller microprogram stops requesting TILINE master cycles, but continues to read the complete record in order to verify the CRC character.

If the transfer inhibit bit (W1, bit 4) were set, the controller would read the entire record, but would not request any TILINE master cycles, preventing any data flow to the 990 memory. The CRC would be checked at the end of the operation. This is a means of checking a previously recorded record without tying up the TILINE with unnecessary data transfers.

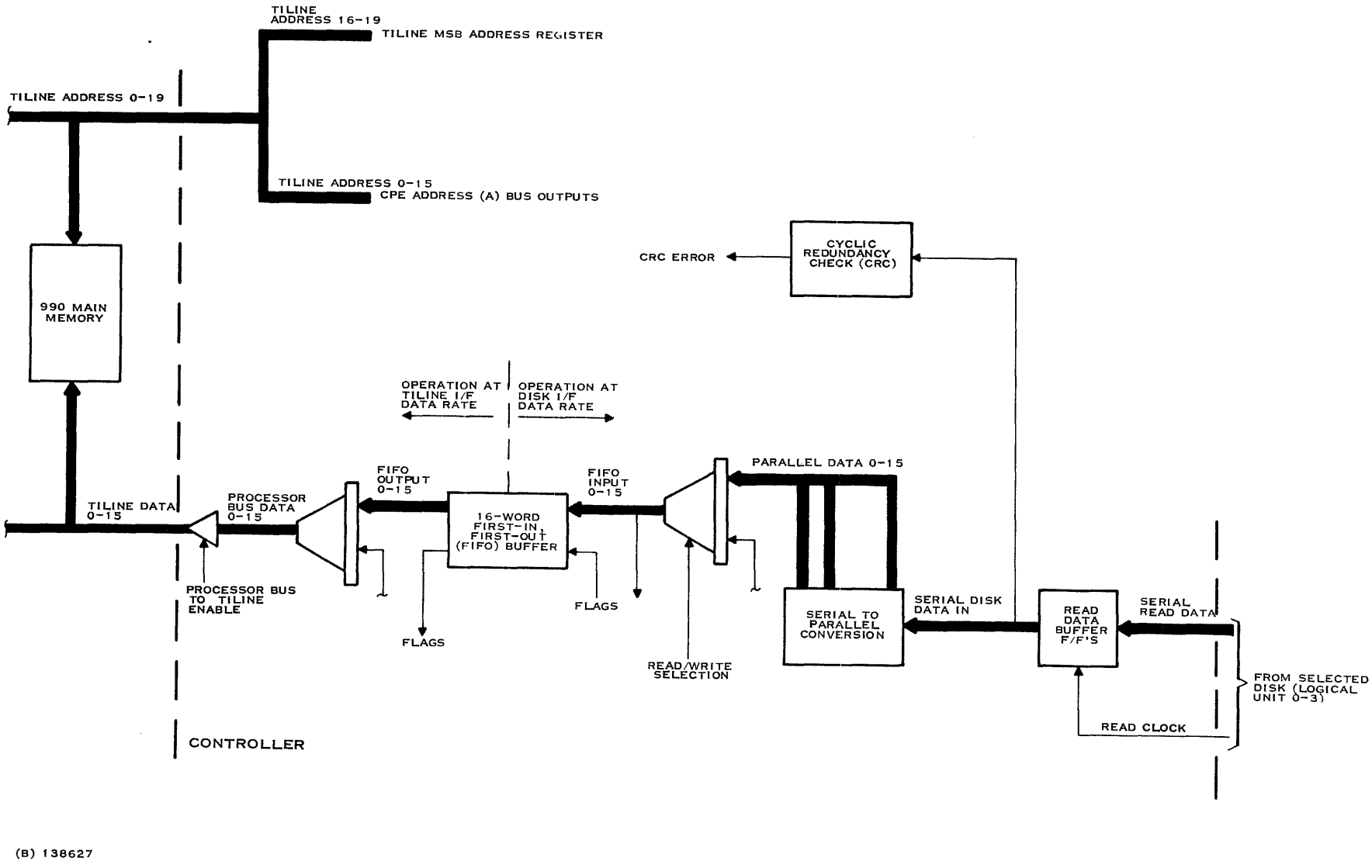


Figure 2-6. Simplified Data Flow for Disk Read Operation

2.3.4 DATA FLOW FOR A WRITE FORMAT OPERATION. Refer to figure 2-7, which shows data flow for a write format operation.

The write format operation is performed on every eligible sector of the specified track starting at sector 0. If the specified format is one sector per record, every sector is eligible to serve as the start of a record. For a two sectors per record format, sectors 0, 2, 4 . . . 18 are eligible.

The write format operation records an all-zeros preamble, a synchronization character, a three-word record identification header, and a CRC character at the beginning of every eligible sector.

The data necessary to select the sectors and develop the record identification headers is included in control words W0-W7 so that information is stored in the CPE internal registers.

The write format operation also requires that the controller fill each prerecord gap with clock pulses, record a synchronization character, fill each data area with repeated copies of a filler word, and store the CRC character at the end of each record.

The control words include a TILINE address which is the location of the filler word. The first data flow cycle of a write format operation retrieves the filler word from 990 memory (with a TILINE master read cycle) and gates it into the direct read register for temporary storage. It is then gated onto the processor bus and stored in one of the CPE internal scratch pad registers.

The remaining data transfer cycles involve data flow from the CPE accumulator (D-bus) output to the FIFO input via the processor bus, and from the FIFO output to the disk over the same data path described in paragraph 2.3.3.

2.3.5 DATA FLOW FOR A VERIFY RECORD HEADER OPERATION. The read data and write data operations require that the record identification header be checked before reading or writing the data record. This operation provides a 3-way check between the format recorded on the disk, the record parameters specified by the control words, and the physical track and sector location of the read/write heads.

The desired track location is supplied by the control words, and the disk controller commands the disk drive to move the head carriage to that physical location and select the proper recording surface. When the seek is complete, the disk controller monitors for sector marks, and reads each sector address, waiting for the specified sector to rotate under the read/write heads. It is important to note that this sector address supplied to the controller is not read from the record identification headers. It is developed by the disk drive electronics by tallying sector marks from index mark to index mark.

When the sector address supplied in the control words agrees with the sector address sampled from the disk drive, the controller enables the read gate, monitors for the synchronization character, and then reads the three-word header into the CPE array and checks the CRC character.

If the record header compares correctly to the parameters supplied in the control words, it indicates that the format previously recorded on the disk is correct and recoverable, that the disk drive accessing electromechanical and electronic components are working, and that the parameters of the record as specified for the read/write operation agree with the parameters of the physical record on the disk platter.

Figure 2-8 shows the data flow for reading a record header. Between the disk drive and the output of the serial/parallel shift register, the data flow is identical to a read data or read unformatted operation.

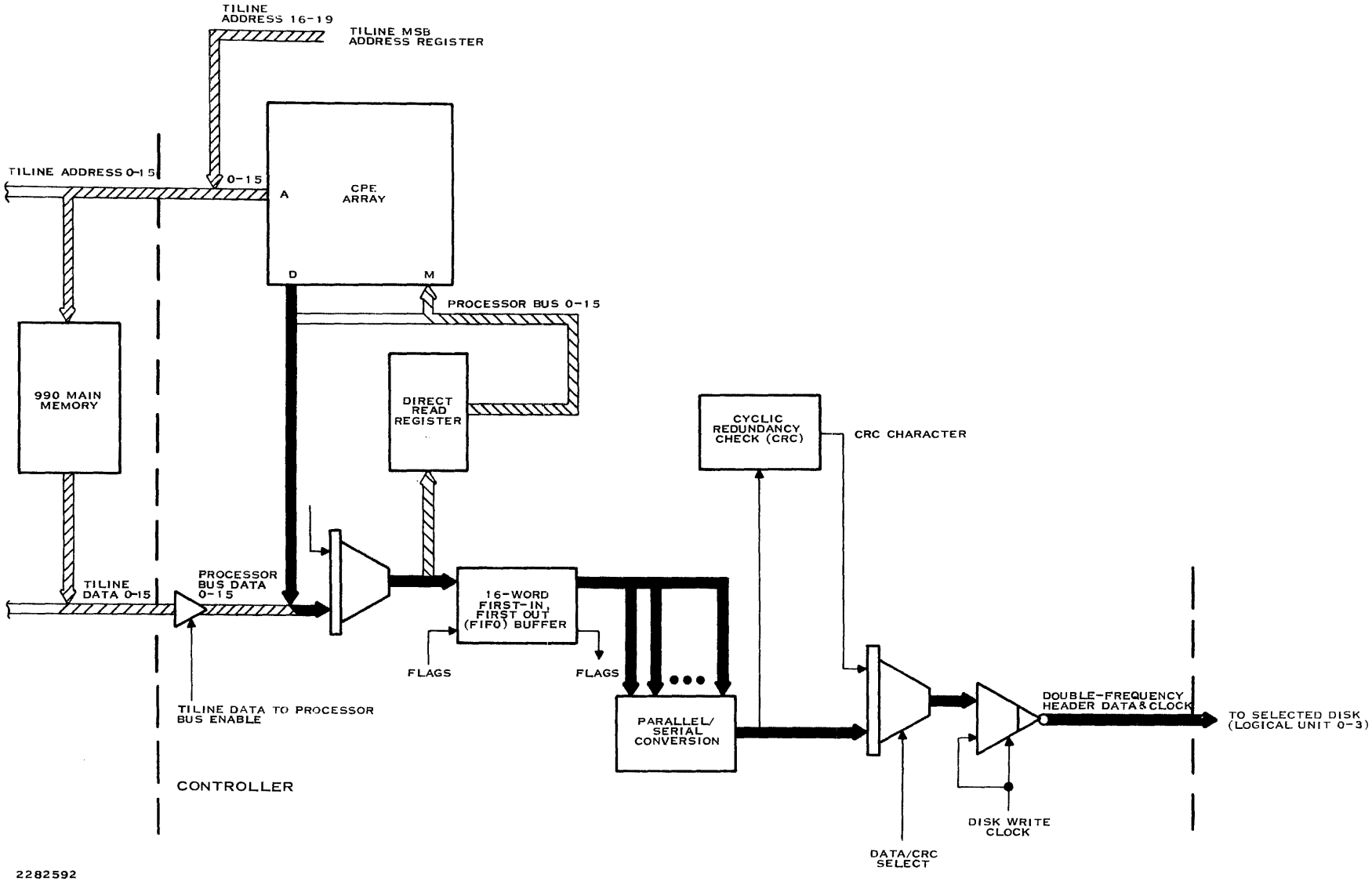


Figure 2-7. Simplified Data Flow for Write Format Operation

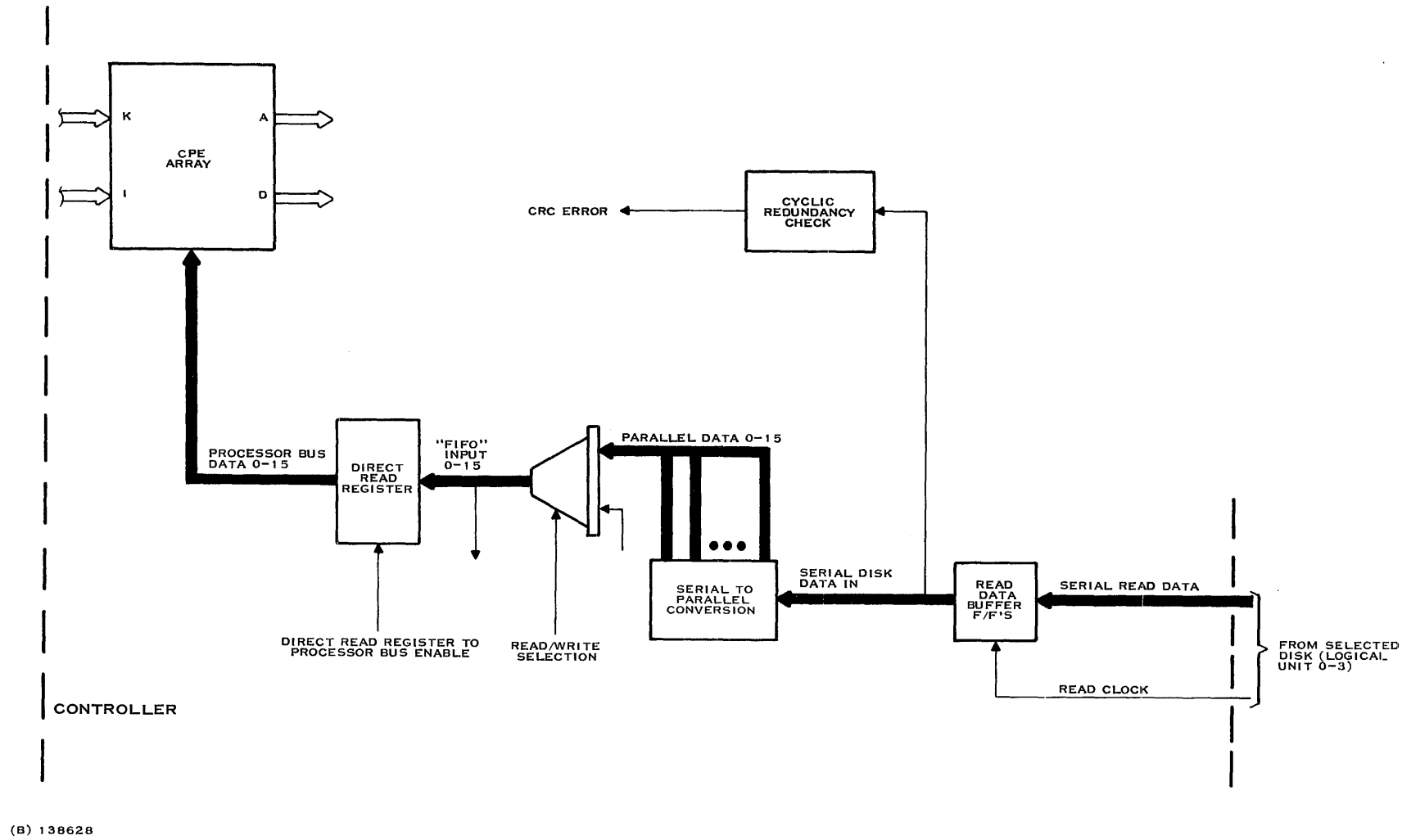


Figure 2-8. Simplified Data Flow for Verify Record Header Operation

The FIFO buffer is not used while reading record headers. Instead, each word is loaded into the direct read register and then transferred over the processor bus to the M-bus inputs of the CPE array. The data and clock inputs to the direct read register are wired in parallel with the FIFO input.

The FIFO buffer is not required when reading record headers because there are no TILINE data transfers required. It is the variable data rate of the TILINE, which is shared by multiple, competing masters, which imposes the need for a FIFO in the disk controller. The microprogram and the CPE array operate much faster than the disk data rate, so the FIFO is not needed for this operation.

2.4 DISK CONTROLLER MICROPROGRAM CONTROL

The 512-word microprogram is always running when power is applied to the controller. The microprogram consists of 40 routines and subroutines which perform internal "housekeeping" operations, control the acceptance of W0-W7, run controller self-tests, and execute the operations specified by the control words.

2.4.1 MICROINSTRUCTION FORMAT. The 40 output bits of the microprogram read-only memory, ROM00-39 are collectively called the ROM bus. These microinstruction bits control every aspect of disk controller operations, including clock control, bus source/destination control, initiation of TILINE master cycles, initiation of disk interface operations, control of CPE array arithmetic, and logical and bit testing functions, among others.

NOTE

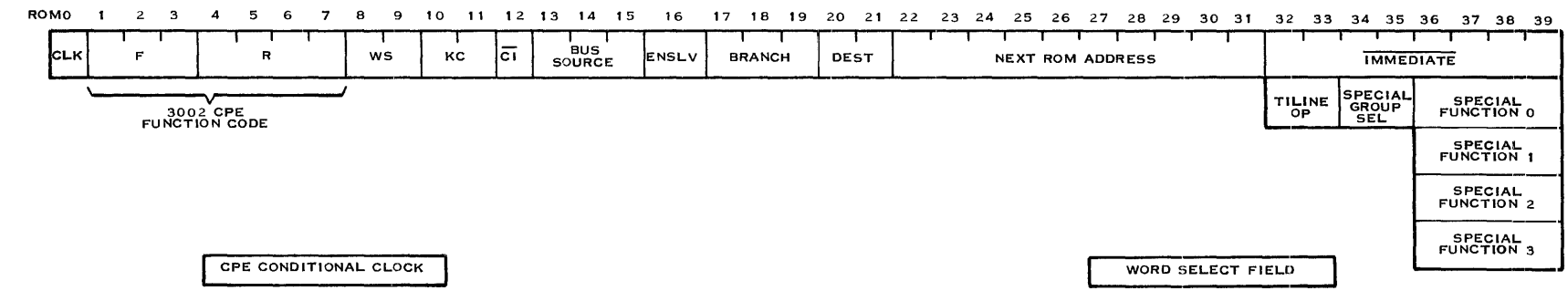
Because the microinstructions control so many functions distributed throughout the controller logic, and because of their critical importance in directing operations, a thorough understanding of microinstruction capabilities and format is necessary to understand the disk controller logic.

The microinstruction format is shown in figure 2-9. The first sheet of this drawing shows the overall functional grouping of microinstruction bits into 12 main fields and six subfields (special fields). Detailed breakdowns of each field describe the function performed by each possible bit combination within the field.

Each microinstruction field is briefly described below.

2.4.1.1 CPE Conditional Clock — ROM0. Bit 0 is the CPE conditional clock control. It may be used to stop the CPE clock so the CPE can perform nondestructive testing of data. No CPE register contents are changed in the absence of the clock pulse. The CPE clock is stopped as part of a conditional branch or conditional return instruction. The test bit is checked during the interval that the CPE clock is stopped, and the test bit determines the next microprogram address. Note that only the clock input to the CPE array is stopped. Clock pulses to the other microcontroller logic, including the microprogram address generator, remain enabled.

2.4.1.2 CPE Function Control Field (F and R Fields) — ROM01-07. The CPE function control field controls the function code inputs, F6-F0, of the 3002 CPEs. The function code consists of a three-bit function field and a four-bit register field. The function field selects one of the eight F-groups, or function groups, of the 3002 CPE. The F-group determines the type of CPE operation. The four-bit register field selects one of the 12 CPE internal registers for the operation. The CPE registers are divided into three R-groups, R-Groups I, II and III. The transfer and accumulator registers are the only registers in R-Group II and R-Group III. They are also included in R-Group I. Refer to the detailed 3002 CPE data for the CPE instruction set.



CPE CONDITIONAL CLOCK

CLK BIT 0	FUNCTION	COMMENT
0	NOP	NO FUNCTION – CLOCK REMAINS ENABLED
1	CLKSTP	STOPS CLOCK INPUT TO CPE SO THAT OUTPUTS OF CARRY, SHIFT AND LOOK-AHEAD CIRCUITRY MAY BE USED FOR NON-DESTRUCTIVE TESTING OF DATA. NO CPE REGISTER CONTENTS ARE CHANGED IN THE ABSENCE OF THE CLOCK PULSE.

WORD SELECT FIELD

WS FIELD BITS8, 9	FUNCTION	COMMENT
0 0	WORD	CPE CARRIES ARE CONFIGURED FOR FULL 16-BIT WORD OPERATIONS
0 1	SHIFT WORD	CPE SHIFT LINES CONFIGURED FOR FULL WORD RIGHT SHIFT
1 0	LEFT BYTE	CPE LEFT BYTE OPERATIONS (INCLUDING SHIFT)
1 1	RIGHT BYTE	CPE RIGHT BYTE OPERATIONS (INCLUDING SHIFT)

F-FIELD

F-GROUP	ROM01 (F6)	ROM02 (F5)	ROM03 (F4)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

THE 7-BIT FUNCTION CODE FOR THE 3002 CPE CONSISTS OF A 3-BIT FUNCTION FIELD AND A 4-BIT REGISTER FIELD. THE FUNCTION FIELD SELECTS 1 OF THE 8 FUNCTION GROUPS. THE REGISTER FIELD SELECTS ONE OF THE 11 CPE SCRATCHPAD REGISTERS (R0-R9, T) OR THE CPE ACCUMULATOR REGISTER (AC). THE CPE REGISTERS ARE DIVIDED INTO 3 GROUPS. THE T AND AC REGISTERS MAY BELONG TO ANY GROUP, DEPENDING ON THE CODE USED IN THE R-FIELD.

THE OPERATION PERFORMED BY THE CPE IS DETERMINED BY THE F-GROUP, THE R-GROUP, AND THE MASK DATA ON THE K-BUS. REFER TO THE CPE INSTRUCTION SET DESCRIPTION.

NOTE THAT THE PROCESSOR CONTROL BUS NUMBERING ROM01-07, RUNS COUNTER TO THE MICRO-FUNCTION BUS NUMBERING, F6-F0, WITHIN THE CPE DEVICES.

R-FIELD

BIT POSITIONS

R-GROUP	CPE REGISTERS	ROM04 (F3)	ROM05 (F2)	ROM06 (F1)	ROM07 (F0)	HEXADECIMAL EQUIV.
I	R0	0	0	0	0	0
	R1	0	0	0	1	1
	R2	0	0	1	0	2
	R3	0	0	1	1	3
	R4	0	1	0	0	4
	R5	0	1	0	1	5
	R6	0	1	1	0	6
	R7	0	1	1	1	7
	R8	1	0	0	0	8
	R9	1	0	0	1	9
	T	1	1	0	0	C
	AC	1	1	0	1	D
II	T	1	0	1	0	A
	AC	1	0	1	1	B
III	T	1	1	1	0	E
	AC	1	1	1	1	F

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K-BUS CONTROL FIELD

KC FIELD BITS10 11	FUNCTION	COMMENT
0 0	FFFF → K, ENSPEC	LOADS ALL ONES INTO CPE K-BUS INPUTS. ALSO ENABLES DECODING OF SPECIAL FIELDS (TILINE OP SPECIAL GROUP, AND SPECIAL FUNCTION) IN BITS32-39.
0 1	0000 → K, ENSPEC	LOADS ALL ZEROS INTO CPE K-BUS INPUTS, ALSO ENABLES DECODING OF SPECIAL FIELDS (TILINE OP, SPECIAL GROUP, AND SPECIAL FUNCTION) IN BITS 32-39.
1 0	$\overline{IM}$ → K	LOADS INVERTED IMMEDIATE OPERAND FIELD INTO CPE K-BUS INPUTS.
1 1	$\overline{IM}$ → K	

KC IS A 2-BIT FIELD WHICH SELECTS THE INPUT TO THE MASK (K) BUS OF THE 3002 CPE. THE 8-BIT IM FIELD IS LOADED INTO THE LEFT OR RIGHT BYTE BEING PROCESSED AT THAT POINT IN THE PROGRAM.

CARRY IN FIELD

$\overline{CI}$ BIT 12	FUNCTION	COMMENT
0	1 → CI CARRY/ONE-FILL	CONTROLS THE CARRY INPUTS TO THE CPE DEVICES AS SPECIFIED BY THE WS FIELD. SELECTS ZERO-FILL (BIT12=1) OR ONE-FILL FROM LEFT DURING RIGHT SHIFTS.
1	0 → CI NO CARRY/ZERO-FILL	

Figure 2-9. Microinstruction Format

PROCESSOR BUS SOURCE FIELD

BITS 13 14 15	BUS SOURCE	COMMENT
0 0 0	ZEROS	ALL ZEROS TO PROCESSOR BUS (PBUS00-15)
0 0 1	CPE WORD	CPE LEFT BYTE TO PBUS00-07, RIGHT BYTE TO PBUS08-15
0 1 0	EXTERNAL	FLOATING BUS - NO DATA TRANSFER VIA PBUS
0 1 1	TILINE	TILINE DATA TO PROCESSOR BUS
1 0 0	DSKDATA	DISK DATA FROM FIFO TO PROCESSOR BUS (FROM DIRECT READ REGISTER IF DIRECT MODE SET BY SPECIAL FIELD 01)
1 0 1	UNDEFINED	
1 1 0	DSKSTATUS	STATUS BITS FROM DISK DRIVE TO PROCESSOR BUS
1 1 1	UNDEFINED	

TILINE SLAVE CONTROL

ENSLV BIT 16	FUNCTION	COMMENT
0	NOP	DISABLE TILINE SLAVE
1	ENSLV	ENABLE SLAVE FLIP-FLOPS TO EXECUTE A SLAVE CYCLE IF REQUESTED BY AN EXTERNAL TILINE MASTER, SUCH AS THE 990 PROCESSOR.

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BRANCH CONTROL FIELD

BC BITS 17 18 19	FUNCTION	COMMENT
0 0 0	UNCONDITIONAL INCREMENT TO CURRENT ADDRESS + 1	
0 0 1	UNCONDITIONAL BRANCH TO NEXT ROM ADDRESS (NRA)	
0 1 0	CONDITIONAL BRANCH IF TRUE TO NEXT ROM ADDRESS (NRA)	TESTBITQ TRUE TO ENABLE BRANCH, OTHERWISE INCREMENT ADDRESS
0 1 1	CONDITIONAL BRANCH IF FALSE TO NEXT ROM ADDRESS (NRA)	TESTBITQ FALSE TO ENABLE BRANCH, OTHERWISE INCREMENT ADDRESS
1 0 0	UNCONDITIONAL BRANCH AND LINK TO NEXT ROM ADDRESS (NRA)	CURRENT ADDRESS +1 TO STACK
1 0 1	CONDITIONAL RETURN IF TRUE, BRANCH TO NRA IF FALSE	RETURN TO THE ADDRESS STORED IN THE STACK OF THE SN74S482 MCU ADDRESS GENERATOR IF TESTBITQ IS TRUE. FOR TESTBITQ FALSE, BRANCH TO NRA.
1 1 0	CONDITIONAL RETURN IF FALSE, BRANCH TO NRA IF TRUE	RETURN TO THE ADDRESS STORED IN THE STACK OF THE SN74S482 MCU ADDRESS GENERATOR IF TESTBITQ IS FALSE. FOR TESTBITQ TRUE, BRANCH TO NRA.
1 1 1	UNCONDITIONAL RETURN	RETURN TO THE ADDRESS STORED IN THE STACK OF THE SN74S482 MCU ADDRESS GENERATOR.

THE MICRO-PROGRAM ADDRESS (MCUADR1-9) IS DETERMINED BY SN74S482 NEXT ADDRESS GENERATOR DEVICES. THE DEVICE CONTAINS A 4-WORD PUSH/POP STACK, ADDER, MULTIPLEXER AND OUTPUT REGISTER. REFER TO THE SN74S482 AND BRANCH CONTROL ROM DESCRIPTIONS.

THE OCCURRENCE OF A TRAP WILL STORE THE BRANCH ADDRESS DETERMINED ABOVE IN THE STACK AND CAUSE A JUMP TO THE TRAP ADDRESS, WHICH REPLACES THE NRA FIELD.

PROCESSOR BUS DESTINATION FIELD

BITS 20 21	FUNCTION	COMMENT
0 0	NOP	NO FUNCTION
0 1	UNITLOAD *	LOAD DISK UNIT SELECT SIGNALS INTO THE UNIT SELECT REGISTER
1 0	FIFO*	LOADS CPE OUTPUT WORD INTO FIFO FOR TRANSMISSION TO DISK. NOT REQUIRED FOR TILINE TO DISK TRANSFER
1 1	CYL ADDR*	LOADS CPE OUTPUT WORD INTO DISK ADDRESS SELECT REGISTER

* COMMAND IS STROBED ON NEXT MICROPROCESSOR CLOCK (MPCK-) PULSE.

Figure 2-9. Microinstruction Format (Sheet 2 of 4)

IMMEDIATE OPERAND FIELD

KC = 1 0 OR 1 1

IM FIELD BITS 32—39	COMMENT
	THE 8-BITS OF THE IMMEDIATE OPERAND FIELD ARE APPLIED TO THE K-BUS (MASK) INPUTS OF THE ACTIVE CPE BYTE. EACH BIT OF THE IM FIELD IS INVERTED BY THE CPE K-BUS INPUTS.

NEXT ROM ADDRESS FIELD

NRA
22 23 24 25 26 27 28 29 30 31

THE NEXT ROM ADDRESS FIELD, ROM22-31, IS USED TO SUPPLY BRANCH ADDRESSES AS DESCRIBED WITH THE BRANCH CONTROL FIELD. BIT 22 IS A SPARE. WHEN A TILINE SLAVE TRAP OCCURS, THE NRA BITS ARE REPLACED AS FOLLOWS:

NRA 23	24	25	26	27	28	29	30	31
0	TILINE SLAVE ACTIVE(1)	1	1	1	READ-	TILINE ADDRESS, 3 LSB		

WHEN AN INTERRUPT TRAP OCCURS, THE NRA BITS ARE REPLACED AS FOLLOWS:

NRA 23	24	25	26	27	28	29	30	31
0	TILINE SLAVE ACTIVE(0)	INTERRUPT ADDRESS			0	0	0	0

TILINE CONTROL FIELD

KC = 00 OR 01

BITS 32 33	FUNCTION	COMMENT
0 0	NOP	NO FUNCTION
0 1	SLVTRM	TILINE SLAVE OPERATION TERMINATE, CAUSES TILINE SLAVE LOGIC TO ISSUE TILINE TERMINATE (TLTM-) SIGNAL
1 0	MSTRD	TILINE MASTER READ, CAUSES TILINE MASTER LOGIC TO GAIN ACCESS TO THE BUS AND READ ONE WORD FROM COMPUTER MEMORY.
1 1	MSTWT	TILINE MASTER WRITE, CAUSES TILINE MASTER LOGIC TO GAIN BUS ACCESS AND WRITE ONE WORD TO COMPUTER MEMORY

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Figure 2-9. Microinstruction Format (Sheet 3 of 4)

GROUP SELECT AND SPECIAL FUNCTION FIELDS

KC = 00 OR 01

BIT 36 37 38 39	SPECIAL FUNCTION 0 (BITS 34, 35 = 00)	SPECIAL FUNCTION 1 (BITS 34, 35 = 01)	SPECIAL FUNCTION 2 (BITS 34, 35 = 1 0)	SPECIAL FUNCTION 3 (BITS 34, 35 = 11)
0 0 0 0	NOP	RST TESTMODE	RST SPAREOUT1	
0 0 0 1	CLK STOP MASTER	SET TESTMODE	SET SPAREOUT1	
0 0 1 0	CLR DSK I/F*	SET TESTCLK	RST RESTORE	BIT 36 = 1 ENABLES CRC
0 0 1 1	MSB ADDR LD	RST TESTCLK	SET RESTORE	OUTPUT TO DISK.
0 1 0 0	STOP I/F CONTROLLER*	RST I/F WRT	RST ERASE	BIT 37 = 1 PRESETS THE CRC
0 1 0 1	MSB ADDR INCREMENT*	SET I/F WRT	SET ERASE	CHARACTER GENERATOR TO ALL 1'S.
0 1 1 0	CLR SECT/INDEX F/F'S*	RST DIRECT MODE	RST WRITE GATE	
0 1 1 1	NOP	SET DIRECT MODE	SET WRITE GATE	BIT 38 = 1 LOADS A SPECIAL FLAG BIT INTO THE FIFO TO DETECT
1 0 0 0	START I/F CONTROLLER*	RST TILINE INT	RST READ	WHEN A STOP CONDITION IS PRESENT.
1 0 0 1	NOP	SET TILINE INT	SET READ	
1 0 1 0	TRIGGER TIMER RESET	SET BUSY	RST SPAREOUT2	BIT 39 IS A SPARE FLAG BIT
1 0 1 1	NOP	RST BUSY	SET SPAREOUT2	
1 1 0 0	RST DIRECT READY*	SET FAULT	RST HEADSEL	
1 1 0 1	NOP	RST FAULT	SET HEADSEL	
1 1 1 0	CLR DISK CONTROL	SET DIAG FAULT	RST ADDSTB	
1 1 1 1	NOP	RST DIAG FAULT	SET ADDSTB	

ROM 36 – 39 ARE MULTIPLE PURPOSE CONTROL BITS. THEY ARE USED PRIMARILY FOR CONTROLLING OUTPUTS TO THE DISK DRIVE.
BITS 34 AND 35 STEER THESE 4 OUTPUT BITS TO THE CORRECT GROUP OF CONTROL GATES AND FLIP-FLOPS.

* COMMAND IS STROBED ON NEXT MICROPROCESSOR CLOCK (MPCK–) PULSE

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Figure 2-9. Microinstruction Format (Sheet 4 of 4)

2.4.1.3 Word Select Field — ROM08, 09. The CPE array is subdivided into two eight-bit blocks, the left byte and the right byte. The interconnection between the bytes and the carry and shift logic is controlled by the word select field. This field also controls the CPE clock modes and the K-bus configuration. The word select field can configure the array for left byte, right byte, full word, or right-shift word operations.

2.4.1.4 K-Bus Control Field — ROM10-11. The K-bus control field selects the input to the mask bus (K-bus) inputs of the CPE array. That input may be a hardwired all zeros or all ones code, or it may be an eight-bit immediate operand (IM-) from ROM32-39. If the immediate operand is not selected, ROM32-39 may be used for the special function subfields described in subsequent paragraphs.

2.4.1.5 Carry In Field — ROM12. This field controls the least significant carry-in bit of the active CPE array, as determined by the word select field. It also selects zero-fill or one-fill into the most significant active stage during right shifts.

2.4.1.6 Processor Bus Source Field — ROM13-15. The three-state processor bus (P-bus) is the main data flow path in the microcontroller. The bus may be driven from any one of multiple sources. ROM13-15 enables the three-state outputs of one source to drive the bus. There are three codes which allow the bus to float during operations which do not require bus transfers. These codes were used during development to allow an external RAM board to control the bus.

2.4.1.7 TILINE Slave Enable Field — ROM16. This bit is set to enable the TILINE slave logic to execute a slave cycle, if requested by an external master such as the 990 processor. This slave cycle either loads a control word into a CPE register or reads a status word from a CPE register. The controller microprogram sets the slave bit while it is idling. After accepting control words and initiating the operation, slave cycles are disabled to prevent interference to the current operation.

2.4.1.8 Branch Control Field — ROM17-19. The branch control field of the currently executing microinstruction specifies how the next microinstruction is to be selected. The next microinstruction may be at the next sequential address, or at a branch address (specified in ROM22-31) that is selected unconditionally or on the basis of a bit test in the CPE array. The next microinstruction may be at a return address stored during some previous branch. Returns may be unconditional, or they may be selected as the result of a bit test within the CPE array.

2.4.1.9 Processor Bus Destination Field — ROM 20, 21. The processor bus destination field enables one of three registers to accept data from the processor bus. These registers are the disk unit select register, the FIFO input stage and direct register, and the cylinder address register.

2.4.1.10 Next ROM Address Field — ROM22-31. The next ROM address field supplies the branch address for conditional or unconditional branches specified in ROM17-19.

2.4.1.11 Immediate Operand Field — ROM32-39. The eight bits of the immediate operand field are supplied to the mask (K) bus inputs of the active CPE byte. Each bit is inverted by the CPE K-bus. To enter a mask of FF_{16}, 00_{16} must appear in ROM32-39.

If the entire 16-bit CPE array is active, the immediate operand is loaded into the right (less significant) byte and the sign (MSB) is extended to the left byte K-bus inputs.

Typical applications of the immediate operand field include supplying constant numerical values, loading initial loop counts or shift counts, and masking status words to test specific bits.

If the K-bus control field commands all zeros or all ones into the CPE K-bus inputs, no immediate operand value is needed. This frees bits 32-39 to serve as subfields of the microinstruction. These fields are: TILINE operation control, special group select, and four special function fields, as described below.

2.4.1.12 TILINE Control Field — ROM32-33. This field controls the initiation of TILINE master read or write cycles, and the termination of TILINE slave cycles.

2.4.1.13 Special Group Select Field — ROM34-35. This field selects one of the four special function decoders that operate on the ROM36-39. In other words, the group select bits specify which special function (1-4) occupies the last four bits of the microinstruction.

2.4.1.14 Special Function Fields (0-3) — ROM36-39. These fields control a variety of individual signal lines and control flip-flops, primarily for interface control. Refer to the last sheet of the format drawing for a detailed breakdown of these functions.

2.4.2 MICROPROGRAM ORGANIZATION. The disk controller microprogram is organized into 13 major routines and a large number of subroutines which may be accessed repeatedly or nested within the course of executing a major routine.

Each routine or subroutine is assigned a three-letter mnemonic, as shown in table 2-1. Flowcharts for these program segments are included in Appendix C, and a complete microcode listing is in Appendix D. Both the listing and the detailed flowcharts use the mnemonic and a two-digit instruction number to uniquely identify each microinstruction. Microinstruction addresses are also supplied on the listing and the flowcharts.

Figure 2-10 is the principle flowchart, which shows the overall program organization and the relationship between the major routines.

In the absence of any current operation, the controller microprogram continually executes the idle (IDL) loop. The idle loop takes about 1.5 microseconds for each pass (5 microinstructions at 300 nanoseconds per clock cycle). The enable slave bit is set during the entire loop, so that a control word may be loaded (or status word read) via a TILINE slave cycle. The idle/busy bit is checked on each pass to determine if a controller operation has been commanded (W7, bit 0 = 0).

When the 990 computer addresses the disk controller with a write operation, and a slave operation (ROM 16) is enabled, the controller jumps to a trap address and executes a slave write (SWR) routine. There are eight different slave write routines, one for each control word address. When the control word has been loaded into the CPE internal register, the slave write routine issues a slave terminate command and returns to the idle loop. In the special case of a W6 control word, the slave write routine performs logical unit selection before returning to the idle loop.

The 990 computer may also read any of the eight slave registers, causing the controller microprogram to jump to one of the eight slave read (SRD) routines. When the controller has enabled the data word into the TILINE, it issues a slave terminate signal.

As a typical example, assume that a slave write 7 routine has loaded a control word with the idle bit reset. On the next pass through the idle routine, a mask and bit test instruction detects the state of the idle bit, and causes a branch to the initialize routine.

The initialize routine (INI) sets the busy latch and resets the slave enable. Any subsequent attempt to perform a slave write will be rejected, and a slave read will be answered by a simulated W7 word. The INI routine proceeds to clear the interrupt latch and controller status in W7 (except the interrupt enable bit). The microprogram then branches to the self-test routine, ZDT. The self-test is not shown on the principle flowchart. Any mnemonic which starts with a capital Z, (ZDT, ZER, ZEH and so on) identifies a self-test instruction.

Table 2-1. Mnemonics for Microprogram Routines and Subroutines

Mnemonic	Routine/Subroutine Name
CCS	Check CRC and Stop
DST	Delay Start
DWS	Disk Write Start
HCU	Head/Cylinder Update
INC, FAV	Increment AC and FIFO Available
IDL	IDLE
INI	Initialize
INT	Interrupt Traps
LTC	Long Test Check
RDD	Read Data
RDU	Read Unformatted
RST	Restore
RUP	Record Update
SDS	Search, Delay, Start
SKS	Seek Subroutine
SRD	Slave Read
SWR	Slave Write
SRG	Store Registers
SRW	Store Registers Write
SSS	Start Sector Search
SSX	Secondary Start Transfer
STX	Start Transfer
TRM	Terminate Routine
VID	Verify ID Words
WCS	Write CRC and Stop
WFT	Write Format Track
WHD	Write Header
WRD	Write Data
WRU	Write Unformatted
WST	Write Stop
ZAC	Z Abort Check
ZDR	Z Direct Register
ZDT	Z Diagnostic Test
ZER	Z Error Routine
ZRF	Z Register Fill
ZRH	Z Read Header
ZRT	Z Register Test
ZSU	Z Status Update
ZTC	Z Test Clock

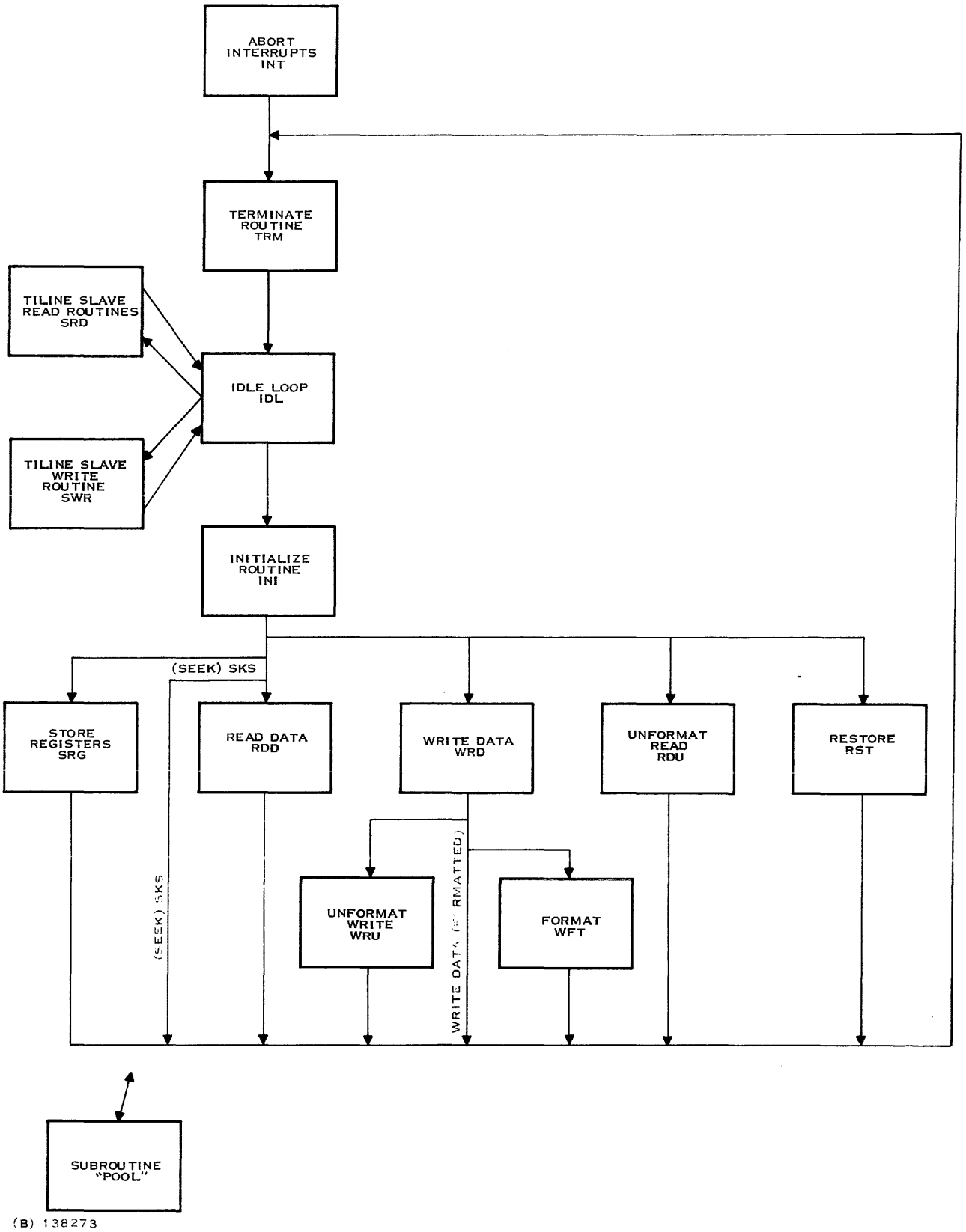


Figure 2-10. Microprogram Principal Flowchart

Upon successful completion of the self-test, control returns to the INI routine, which performs those operations that are common to all the disk commands. When this common segment is finished, INI decodes the command (W1, bits 5-7) and branches to the store registers, read data, write data, read unformatted or restore routine. A SEEK command causes a branch to the terminate routine.

Each of the major command routines ends at the terminate routine, which performs common housekeeping functions, then updates the disk controller status word, W7, before returning to the idle loop.

2.5 CONTROLLER TIMING

Microprocessor clock, MPCK-, is one of two principle timing terms used in the DS10 disk controller. Microprocessor clock and its derivatives are used for clocking, gating, enabling, and synchronizing the controller functions which do not directly interface with the disk drive. MPCK482-, for example, is the timing term which causes the microprogram address generator to fetch the next 40-bit microinstruction from control memory. Disk interface timing is described with the disk interface logic.

2.5.1 MICROPROCESSOR CLOCK — GENERAL. The clock pulse, MPCK-, is an 80-nanosecond active-low pulse. The results of CPE operations are stored in the CPE registers on the leading (negative-going) edge. The TTL logic external to the CPEs is clocked on the trailing (positive-going) edge of the pulse. The period between successive MPCK- pulses is determined by the type of operation in progress.

The microprocessor clock logic has three operating modes: free-running, TILINE-triggered, and test. The free-running clock consists of a constant-period waveform with a period of 300 nanoseconds. The TILINE-triggered clock has a variable period which is determined by the completion of TILINE operations. The test mode allows the clock to be held inactive by an external state board.

During normal operations, the controller clock changes from free-running to TILINE-triggered to free-running with no hitches or cycle losses. If the controller operated solely on a free-running clock, there would be, on the average, one half of a clock period wasted for each TILINE transfer. The TILINE-triggered clock avoids this time waste by restarting the clock immediately at the end of the TILINE transfer. Also, holding off the clock during a TILINE cycle prevents waste of controller states during the message operation.

The timing circuit is based on three RC delay timers, a latch and associated gating circuitry. The time delays inherent in the TTL gates and those due to the three delay timers determine the pulse width and period of the MPCK- waveform. The timing circuit is very similar to the main timing circuit on the 990/10 AU2 board.

Figure 2-11 is the schematic of a typical delay timer circuit. With a low input signal, the SN7407 open-collector buffer holds the capacitor close to zero volts. When the input signal goes high, the capacitor starts charging (through the resistor) toward +5 volts. When the capacitor voltage reaches the positive-going threshold voltage of the SN74132 Schmitt-trigger NAND gate, the circuit output goes low. The time between this negative transition at the output and the positive transition at the input is the timer delay.

The timer output remains low until the input signal drops low. The output goes high as fast as the SN74132 can switch. The capacitor is discharged through the open collector output circuit of the SN7407. This discharge time, which is much faster than the charge time, determines the minimum retrigger time for a reliable delay. Notice that the input pulse must be longer than the delay time to get an output from the circuit.

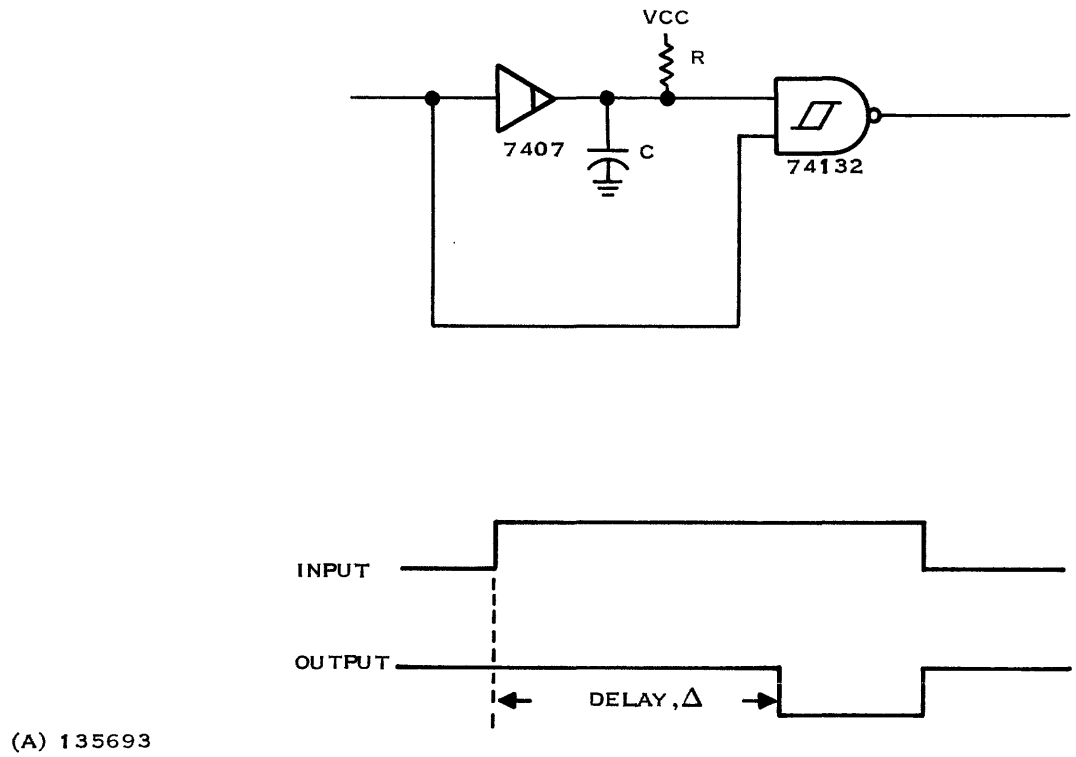


Figure 2-11. Delay Timer Circuit

2.5.2 DETAILED DEVELOPMENT OF MPCK-. This description of microprocessor timing development is keyed to the simplified logic drawing, figure 2-12, and the timing diagram, figure 2-13. The description starts at a convenient point in the timing cycle and continues until the same conditions are reached.

Assume that CLKT2- is high so that it will be possible to set the clock on latch, and that the clock circuit is not inhibited by the CLKINH or SLTMA- signal. CLKT3- from delay 3 goes low to enable CLKEN and CLKSTRT-. The CLKON output of the clock latch goes high and, since CLKT2- is high, the clock latch sets.

The CLKON signal performs the following three functions:

- Disables the CLKSTRT- signal via the CLKOFF inverter and the output gate of the delay 3 timer (delay 3 is not initiated yet). The pulse width of CLKSTRT- is approximately 55 nanoseconds, all due to gate delays.
- Combines with CLKT1- to enable the MPCK-, MPCK, and MPCK482- timing pulses. These pulses remain active until delay 1 expires.
- Initiates delay 1, which determines clock pulse width.

Delay 1 expires (CLKT1- goes low) 80 nanoseconds after the clock on latch sets. When delay 1 expires, the clock pulse has been produced and all the remaining operations are concerned with setting the period of the clock waveform.

The inverted form of CLKT1- initiates the delay 2 timer, which clears the CLKON latch after approximately 20 nanoseconds. An external test input to the delay 2 timer allows the clock to be held for single stepping.

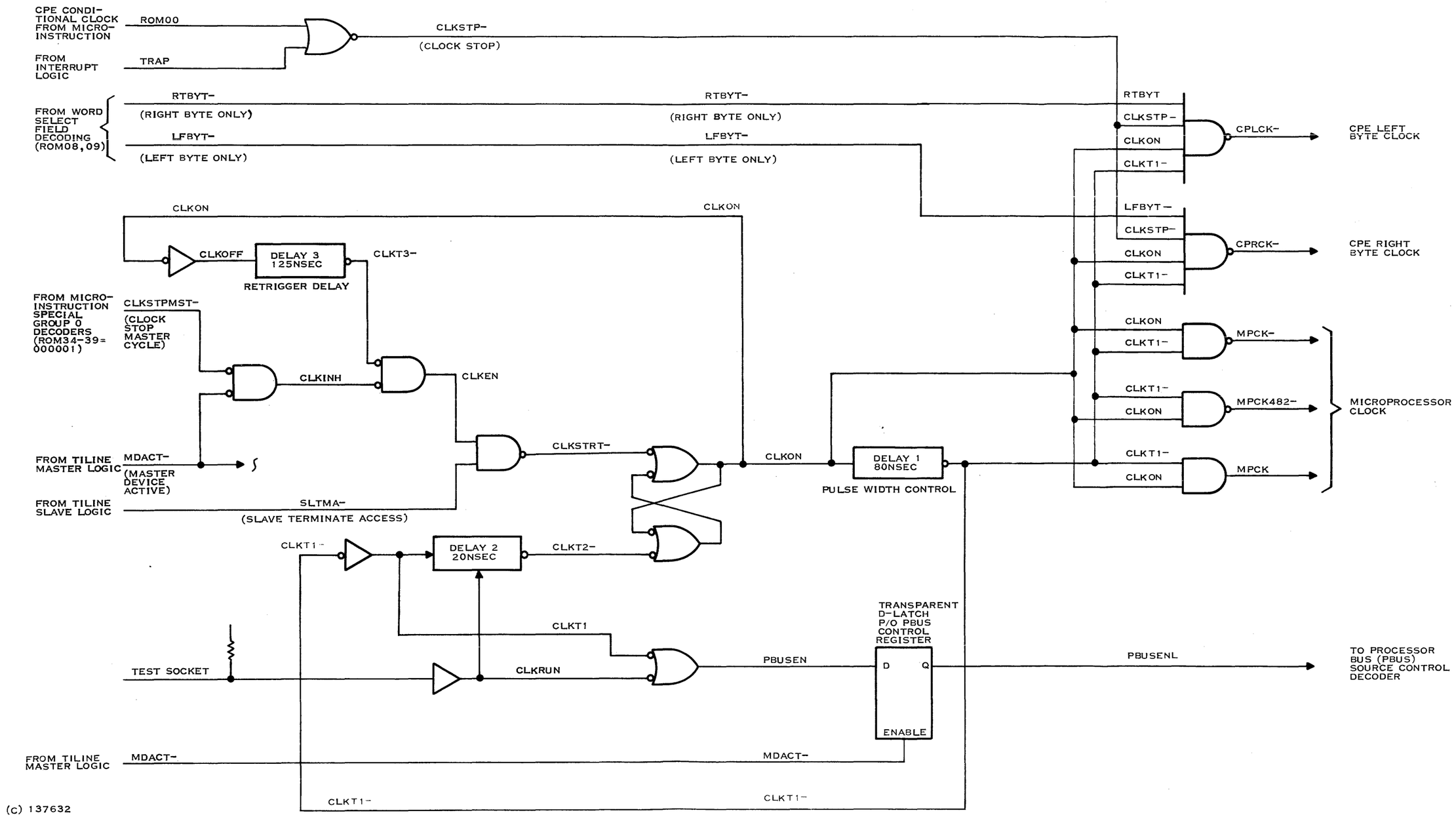


Figure 2-12. Microprocessor Clock (MPCK-) Logic Simplified

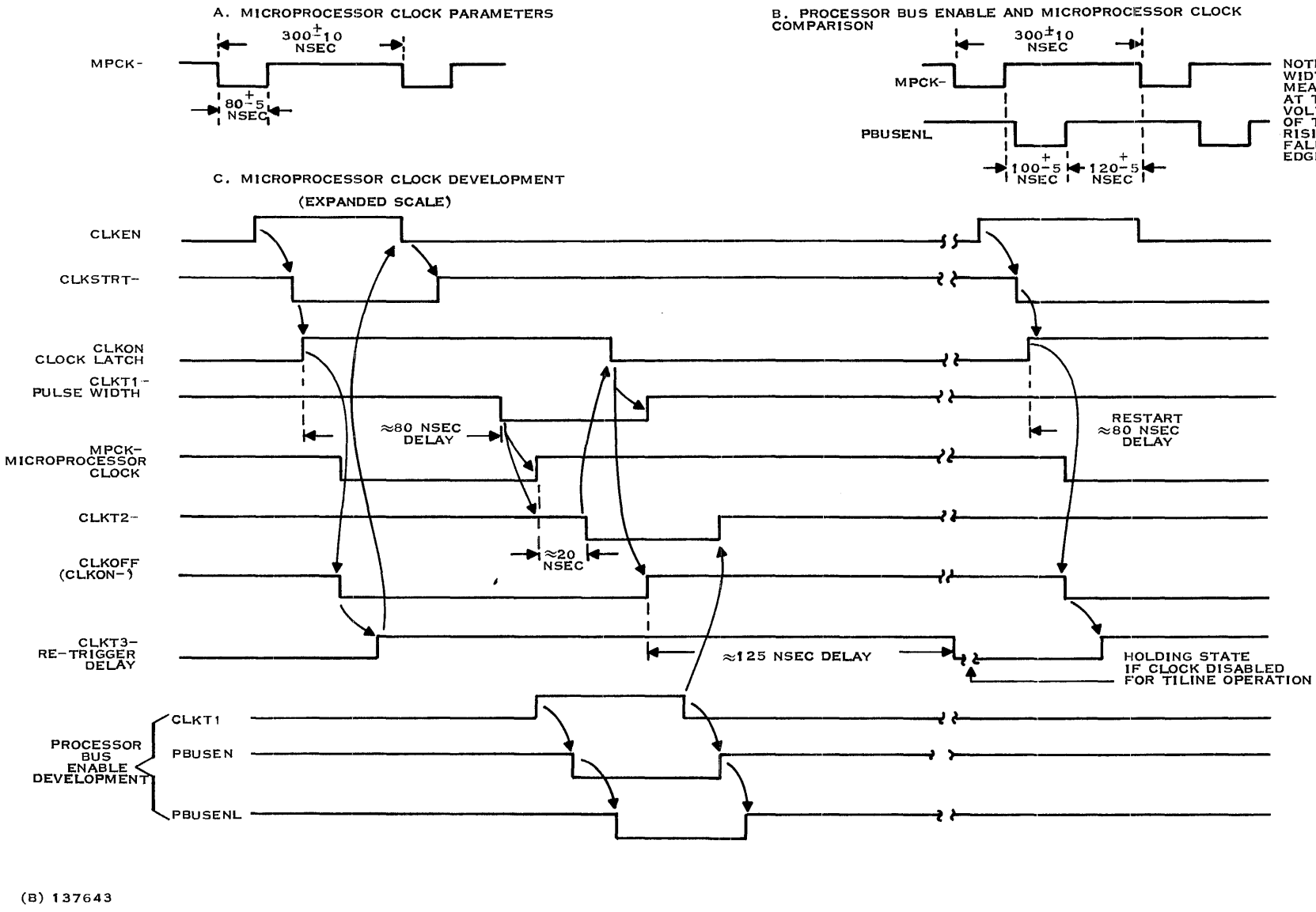


Figure 2-13. Timing Diagram — Microprocessor Clock

When the CLKON latch clears, delay 3 (125 nanoseconds) is initiated. The clock circuit cannot retrigger until delay 3 expires to partially enable the CLKEN gate. Delay 3 guarantees that there is adequate time for the capacitors in delays 1 and 2 to return to the initial (discharged) state.

At the expiration of delay 3, the circuit is back in the initial state. If the clock is not inhibited by CLKINH or SLTMA-, the clock circuit retriggers when CLKT3- goes low (free-running mode).

If the clock is inhibited, the circuitry remains in the holding state until the inhibiting condition is removed. This is the TILINE-triggered mode. The effect of a TILINE cycle on the clock waveform is shown in figure 2-14.

2.5.2.1 TILINE-Triggered Mode. Microprocessor clock may be inhibited and then restarted during either a slave or a master cycle. In either case, the inhibiting signal is controlled by a field in the 40-bit microinstruction, and logic conditions in the TILINE interface.

A TILINE slave operation is initiated by the 990 CPU in an attempt to load a control word into a CPE register (slave write) or read a word from a CPE register (slave read). The controller responds to the slave read or write request if the ENSLV bit (ROM16) of the microinstruction is set and the TILINE address compares to the slave address switch settings. The controller microprogram traps to a slave read or slave write routine.

During a slave read, for example, the requested data is moved from the CPE register to the accumulator and enabled out to the TILINE drivers. At this point, the microprogram issues a slave terminate command (ROM 32, 33 = 00). The SLVTRM- output of the decoder stops the microprocessor clock by forcing the slave terminate access (SLTMA-) signal low, and also sends a TILINE terminate (TLTM-) signal to the 990 CPU. The controller state remains fixed, with the data on the output lines, until the 990 CPU indicates that the transfer is complete by disabling the TILINE go (TLGO-) signal. Microprocessor clock is restarted when the TLGO- forces SLTMA- high again, and the microprogram begins executing again.

The operation is similar for a slave write, except that the TILINE data is loaded into the CPE accumulator, transferred to the proper register, and then the slave terminate is issued. Microprocessor clock stops until the 990 CPU acknowledges completion of the transfer by disabling TLGO-.

Microinstruction bits 32 and 33 enable a master read or master write cycle. The MSB address register is updated and the CPE devices place the lower 16 address bits on the TILINE address drivers. The data path between the TILINE drivers/receivers and the FIFO is established. The microprocessor clock is suspended by special field 00 = (ROM 36-39) = 0001, which enables CLKSTPMST-. The clock remains inhibited until the word is transferred and MDACT- (master device active) goes high.

A 20-microsecond timer is initiated at the start of each TILINE master cycle. If the TILINE operation hangs, the timer expires, clearing the TILINE logic and restarting the clock circuit.

2.5.2.2 Microprocessor Clock Output Gating Logic. Refer to the timing outputs at the right side of the simplified timing logic diagram. CPLCK- and CPRCK- are the gated clock outputs to the CPE left byte clock and CPE right byte clock, respectively. When enabled, the CPRCK- and CPLCK- outputs coincide with microprocessor clock, MPCK-.

The 3002 CPE devices are connected to perform left byte, right byte, or full word operations, as specified by the 40-bit microinstruction. The word select field of the microinstruction determines whether the left byte clock, right byte clock, or both should be enabled. The word select field, ROM 8, 9 is decoded to produce the RTBYT- and LFTBYT- signals. The RTBYT- signal, when low, disables the left byte clock, so that only the right byte CPEs are clocked. The LFTBYT- signal, when low, disables the right byte clock.

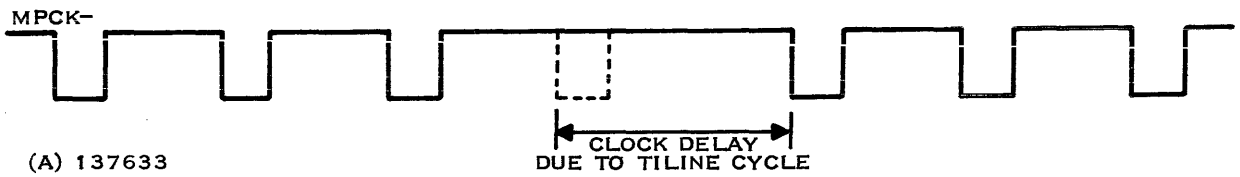


Figure 2-14. Microprocessor Clock Delay Due to TILINE Cycle

The clock stop bit of the microinstruction (ROM02) can disable the CPE clock pulse during a microcycle. This is generally done as part of a conditional branching microinstruction, in which the important result is the branch (or nonbranch), rather than the value calculated by the CPE. Refer to the CPE detailed description for more information on nondestructive data testing and conditional clocking.

The TRAP signal into the NOR gate disables the CPE clock pulse while the address generator retrieves the new microinstruction at the trap address.

2.5.2.3 Processor Bus Enable Timing. The processor bus enable-latched (PBUSENL) output of the timing circuits is used to enable the processor bus source decoder. The time delay between the rising (trailing) edge of microprocessor clock, MPCK-, and the rising edge of PBUSENL is a critical timing parameter. The rising edge of MPCK- clocks the microprogram address generators, and the microinstruction outputs become unstable until after the settling time of the address generators and the microinstruction ROM. PBUSENL remains low, disabling the PBUS source decoder during this period, and keeping noise off of the processor bus. A 100-nanosecond setting time is allotted, and then PBUSENL goes high, enabling the PBUS source decoder. Approximately 120-nanoseconds remain before the leading edge of the next MPCK- pulse. This is adequate set-up time for all devices which accept data from the processor bus.

The bottom three lines of the timing diagram show the development of PBUSENL, which is essentially a delayed version of CLKT1. The PBUS control register is a "transparent" D-latch. As long as MDACT- remains high (no TILINE master operation in progress), PBUSENL follows PBUSEN or (CLKT1-, fine line) with only a gate delay. A TILINE master operation latches the PBUSENL output.

2.5.2.4 Controller Timing Adjustments. The waveforms shown in part B of the timing diagram illustrate the critical timing parameters. The RC component values in delays 1, 2, and 3 may be changed to meet the parameters. The adjustments (in order) are:

1. Pulse width of MPCK-, controlled by delay 1.

2. Delay from MPCK- rising edge to PBUSENL rising edge, adjusted by delay 2. The capacitor in this delay is omitted at manufacture. It may be installed if the gate delays alone are insufficient.

3. Period of MPCK-, adjusted by delay 3.

2.6 TILINE BUS

The powerful TILINE high-speed data bus architecture is used to incorporate the disk controller directly into the addressable memory space of the 990 system. The TILINE is an asynchronous, high-speed, 16-bit data transfer bus, with the associated control lines which transfer data between high-speed system elements. These elements include the CPU, the memory, the disk files, and the magnetic tape transports.

Data is transferred along the TILINE data bus as 16-bit parallel words, accompanied by 20-bit word addresses. The TILINE is capable of transferring approximately 50-million bits per second.

2.6.1 MASTER-SLAVE CONCEPT. There are two classes of devices that connect to the TILINE: TILINE master devices that initiate data transfers, and TILINE slave devices that generate or accept data in response to some master device. Data transfers in either direction always occur between one master and one slave. The central processor is an example of a master device, and a memory module is an example of a slave device.

A master device initiates data transfers on the bus, which may consist of reading data words from a slave device or writing data words to a slave. Master devices must compete with each other for access to the TILINE. A positional priority scheme is used to resolve conflicts between masters. A scheduling scheme allows a master to reserve the next TILINE access during the current operation. This overlapping reduces the overhead time to transfer bus control between masters. When a master gets access to the bus, it must place a 20-bit address on the TILINE and exchange "hand-shaking" control signals for each data word transferred to or from a slave device.

Each slave device recognizes a specific range of addresses, and is activated only when the 20-bit TILINE address falls within that range. Pencil switches on the logic board of the slave device set the starting address, called the TILINE base address. The slave device accepts TILINE addresses that range from the TILINE base address to an upper limit determined by the nature of the slave. For example, an 8K memory module would respond to addresses from the TILINE base address to base address +1FFF.

The DS10 disk controller is both a master and a slave device. It acts as a slave when the computer reads or writes control words W0-W7. These control words provide disk and previous command status, specify the parameters of a disk operation and initiate the operation. Control words W0-W7 are assigned eight consecutive TILINE addresses, from the switch-selected TILINE base address to TILINE base address +7. The controller acts as a master when it performs the disk-to-memory or memory-to-disk data transfers specified by the control words. Once the controller operation has been initiated, it operates independently of the 990 processor, and competes with other masters for bus access each time it has to transfer a data word to or from memory.

2.6.2 TILINE PERIPHERAL CONTROL SPACE (TPCS). The TILINE peripheral control space is a range of TILINE slave addresses reserved for assignment to peripheral device controllers, such as the disk controller. The range includes 512 word addresses, extending from $FFC00_{16}$ to $FFDFF_{16}$.

Each peripheral controller is assigned a block of up to 16 addresses in the TPCS. These addresses are used for the control and status words which are used to set up and monitor the peripheral controller operations. The disk controller only requires eight slave addresses for control and status words W0-W7.

The 990 processor contains a hardware mapping function which maps 16-bit CPU byte addresses $F800_{16}$ through $FBFF_{16}$ into the TILINE peripheral control space. This hardware mapping is performed if CPU status register bit 8 is 0, indicating that map file 0 is in use.

2.6.3 TILINE INTERFACE SIGNALS. Figure 2-15 shows the TILINE interface signals in the 990 computer chassis, and table 2-2 defines each of the TILINE signals.

2.6.4 TILINE BUS TIMING — WRITE CYCLE. Figure 2-16 is a timing diagram for a TILINE write cycle. It applies to any TILINE master and slave devices. It does not include the operations necessary for the master to achieve access to the bus.

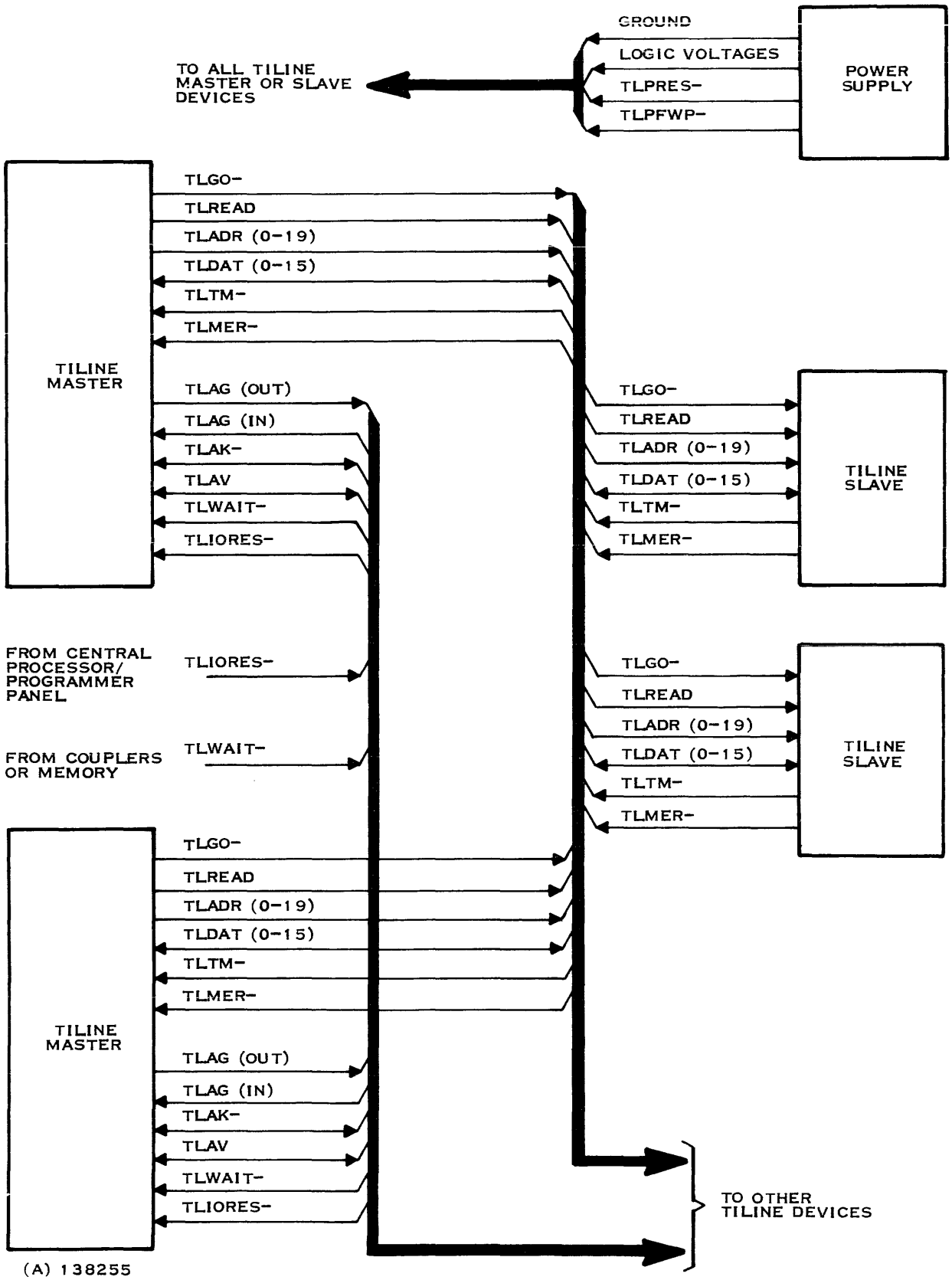


Figure 2-15. TILINE Interface Signals

Table 2-2. TILINE Signal Definitions

Signature	Pin No.	Definition
TLGO–	P1-25	TILINE Go: Initiates all data transfers when transition from high (3.0V) to low (1.0V) occurs. See note 1.
TLREAD	P1-11	TILINE Read: When high (3.0V) designates a read from SLAVE operation; when low (1.0V) designates a write to SLAVE operation. See note 1.
TLADR00–	P2-55	TILINE Address to define the location of data during a fetch or store operation. When high (≥2.0V) the corresponding address bit is a zero; when low (≤0.8V) the corresponding address bit is a one. See note 2.
01–	P2-44	
02–	P2-51	
03–	P2-53	
04–	P2-57	
05–	P2-59	
06–	P2-47	
07–	P2-49	
08–	P2-17	
09–	P2-19	
10–	P2-10	
11–	P2-12	
12–	P2-11	
13–	P2-15	
14–	P2-8	
15–	P2-9	
16–	P2-29	
17–	P2-27	
18–	P2-25	
TLADR19–	P2-31	
TLDAT00–	P2-67	TILINE Data: Bidirectional data lines that when high (≥2.0V) represent zero data bits, and when low (≤0.8V) represent one data bit. See note 2.
01–	P2-69	
02–	P2-35	
03–	P2-37	
04–	P2-61	
05–	P2-63	
06–	P2-43	
07–	P2-45	
08–	P2-21	
09–	P2-33	
10–	P2-23	
11–	P2-20	
12–	P1-27	
13–	P1-28	
14–	P1-30	
TLDAT15–	P1-31	
TLTM–	P1-20	TILINE Terminate: When low (1.0V) indicates that the SLAVE device has completed the requested operation. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 2-2. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLMER–	P1-55	TILINE Memory Error: When low (≤0.8V) indicates that a nonrecoverable error has occurred during a memory read operation. See note 2.
TLAG (in)	P2-6	TILINE Access Granted: When high (≥2.0V), this signal indicates that no higher priority device has requested use of the TILINE. When low (≤0.8V), this signal prevents the receiving device from gaining access to the TILINE bus.
TLAG (out)	P2-5	TILINE Access Granted: When high (≥2.0V), this signal indicates that neither the sending device nor any higher priority device is requesting use of the TILINE. When low (≤0.8V), this signal indicates that either the sending device or some higher priority device is requesting use of the TILINE bus and prevents all lower priority devices from gaining access to the bus.
TLAK–	P1-71	TILINE Acknowledge: When high (3.0V), this signal indicates that no TILINE device has been recognized as the next device to use the TILINE. When low (1.0V), this signal indicates that some TILINE device has requested access, has been recognized, and is waiting for the bus to become available. See note 1.
TLAV	P1-58	TILINE Available: When high (3.0V), this signal indicates that no TILINE device is using the bus. When low (1.0V), this signal indicates that the TILINE bus is busy. See note 1.
TLWAIT–	P1-63	TILINE Wait: A normally high (3.0V) signal that when low (1.0V), temporarily suspends all TILINE MASTER devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest priority user. See note 1.
TLIORES–	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2.0V) signal that when low (≤0.8V), halts and resets all TILINE I/O devices. This signal is a 100 to 500 nanosecond pulse generated by the RESET switch on the control console or by the execution of a Reset (RSET) instruction in the AU. Driven by SN7437; Received by 2 (maximum) standard SN74- loads per slot.
TLPRES–	P1-13 P2-13	TILINE Power Reset: A normally high (≥2.0V) signal that goes low (≤0.8V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 microseconds before dc voltages begin to fail during power-down, and until dc voltages are stable during power-up. Driven by 80-milliampere open-collector driver (160 milliamperes with 40-ampere power supply).
TLPFWP–	P1-16 P2-16	TILINE Power Failure Warning Pulse: A 7.0 millisecond pulse preceding TLPRES–. When low (≤0.8V), this signal indicates that a power-down sequence is in progress, allowing the AU to perform its power failure interrupt subroutine. Driven by SN7437; received by two, maximum, standard SN74- loads per card slot.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table 2-2. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLHOLD–	P2-26	TILINE Hold Signal: A normally high (3.0V) signal that goes low (1.0V) to assert that a central processor is executing an ABS instruction. TILINE Hold prevents interference from another processor on the TILINE while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multi-processor systems. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

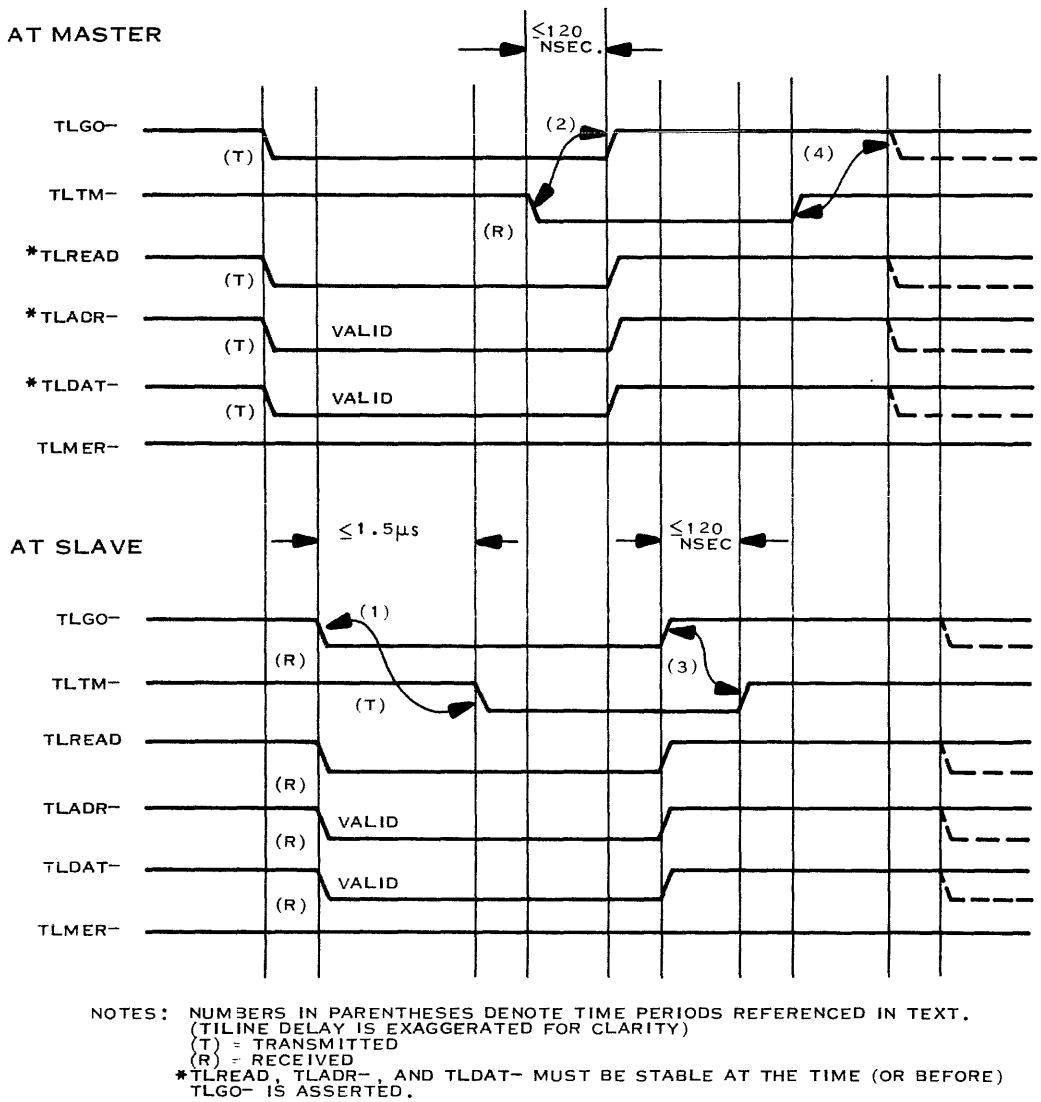


Figure 2-16. TILINE Master to Slave Write Cycle Diagram

The master places the 20-bit slave address and the data word on the lines, with TLREAD low to specify a write operation. It asserts TLGO- to initiate the operation, and holds TLGO- low for the duration of the cycle.

All the slave devices on the TILINE receive TLGO- transmitted by the master. The slave devices must decode the address to determine which slave is being addressed. The slave generates a delayed go signal (using a timer circuit) and uses that signal to strobe for a valid address decode. It is the responsibility of the slave device to delay go for a time sufficient to accommodate the worst case address decode time and the 20-nanosecond worst case TILINE skew.

When the slave device has delayed go and decoded the address as valid, it performs the write cycle and then asserts TLTM-. At the time the slave device asserts TLTM-, it must be finished with the TLDAT-, TLADR, and TLREAD signals from the TILINE. The action just described occurs during time one. This time is defined as the slave access time and should be less than 1.5 microseconds for all TILINE slaves except the TILINE coupler. When the TILINE master receives the asserted TLTM-, it must release TLGO-, TLREAD, TLADR-, and TLDAT- within 120-nanoseconds. This occurs during time two. At this time, the master device may relinquish the TILINE to another master device. When the slave receives the release of TLGO-, it must release TLTM- within 120-nanoseconds as shown in time three. When the master device receives the release of TLTM-, it may begin a new cycle if it has not relinquished the TILINE to another master device. This is shown as time four. Most TILINE masters, including the disk controller, only perform one read or write cycle per bus access.

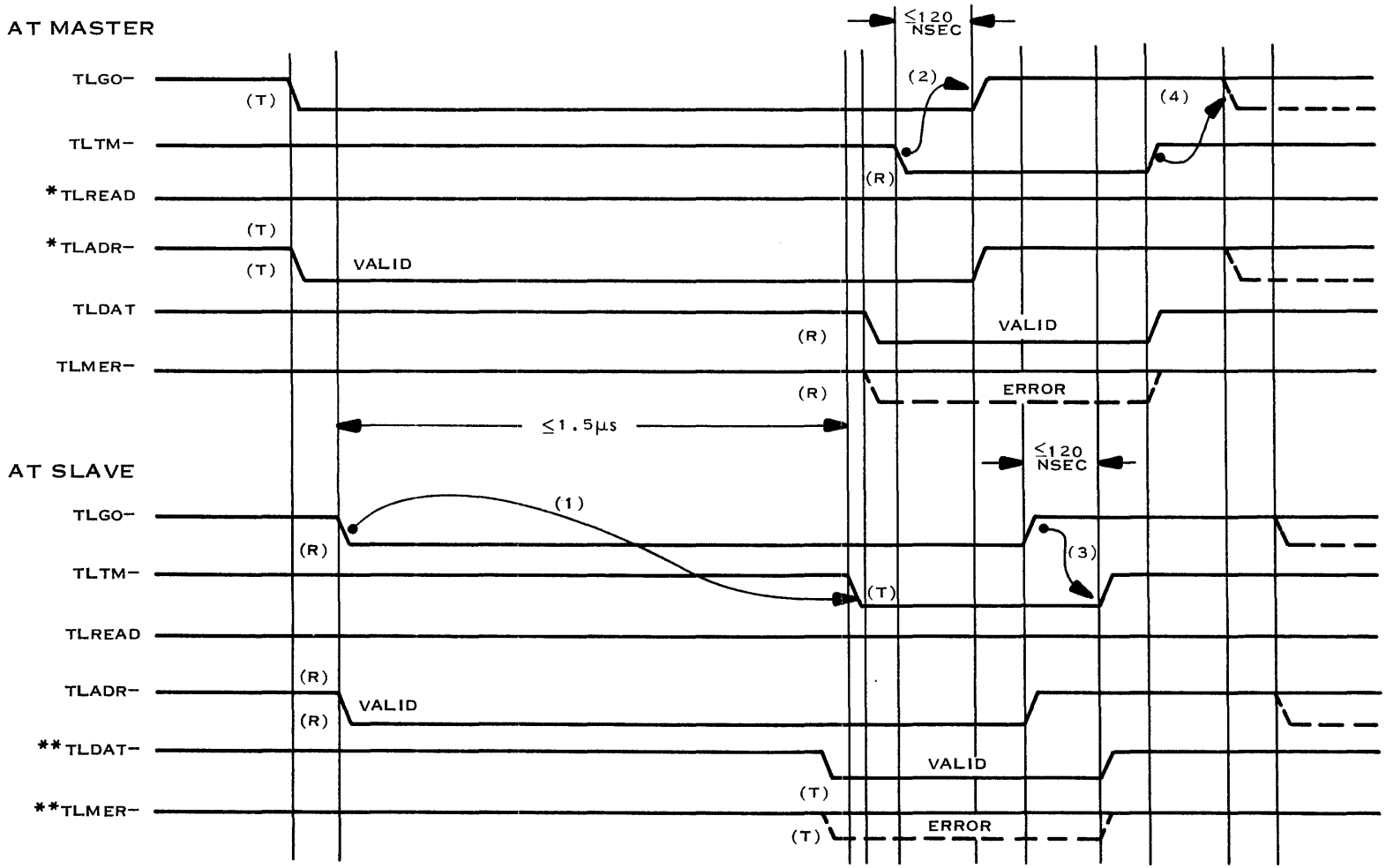
2.6.5 TILINE BUS TIMING — READ CYCLE. Figure 2-17 is a timing diagram for a TILINE read cycle. It applies to any TILINE master and slave devices and does not include the operations necessary for the master to get access to the bus.

The master asserts TLGO- and at the same time generates a valid address (TLADR-) and TLREAD signal. All slave devices on the TILINE receive the TLGO- transmitted by the master. The slave devices delay the go signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsibility of the slave device to delay go for a time sufficient to accommodate the worst case TILINE skew (defined as 20-nanoseconds maximum) and worst case address decode time. When this has been done and the address is decoded as valid, the slave device begins to generate read data. In the case of a memory module, this means starting a read cycle. When read data is valid, the slave device asserts TLTM- and at this time must have finished using TILINE signals TLADR- and TLREAD. If a read error is detected during a read cycle, the READ ERROR (TLMER-) signal is asserted by the slave. This signal must have the same timing as read data. This action occurs during time one.

2.6.6 TILINE MASTER OPERATION OF DS10 CONTROLLER. The DS10 disk controller acts as a TILINE master when transferring data from 990 main memory to disk, or from disk to 990 memory. The controller performs a single TILINE master cycle for each word transferred on the bus. The master cycle consists of the actions necessary to acquire access to the bus, transfer the data word, and release bus control. The TILINE master cycle is controlled by the TILINE master access logic (logic drawing 937502, PWB, or 2262102, fine line) and by designated fields in the controller microinstructions.

A TILINE master read or master write cycle does not represent a trap condition, unlike a slave read or write, because the master cycles are initiated by the controller as the result of a need to transfer a data word. The code segments that control TILINE master cycles are incorporated directly into the major microcode routines, such as Read (RDD), Read Unformatted (RDU), Store Registers (SRG), Write Data (WRD), Write Unformatted (WRU), and Write Format (WFT).

Each of the major command routines is initiated by a series of control words, W0-W7, from the 990 processor. These control words supply the command code and parameters for executing that



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT. (TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED (R) = RECEIVED
*TLREAD AND TLADR- MUST BE STABLE AT THE TIME (OR BEFORE) TLGO- IS ASSERTED
**TLDAT- AND TLMER- MUST BE STABLE AT THE TIME (OR BEFORE) TLTM- IS ASSERTED

(A)133123

Figure 2-17. TILINE Master to Slave Read Cycle Timing Diagram

command. These control words are stored in the 3002 CPE scratchpad registers by a series of TILINE slave write operations. One of the parameters supplied in the control words is the starting TILINE memory address of any data transfers from the controller to 990 memory or memory to controller. The least significant 15 bits of the TILINE address are stored in CPE register R6, and the most significant 5 bits are stored in R5.

If the controller were commanded to perform a Read Data operation with a word count of 50, it would have to read 50 words from the disk and achieve access to the TILINE 50 times, once for each data word. The control words contain only the starting address of the 50-word buffer, so part of the microprogram must be concerned with the "housekeeping" details of maintaining the correct TILINE address as the buffer operation proceeds. Prior to the first TILINE master cycle, the CPEs must load the four most significant bits of the TILINE address into an external (to the CPEs) MSB address register. If the TILINE address crosses a 64K word boundary, the MSB address register must be incremented. The MSB address register is controlled by four bits in special function group 0 of the microinstruction, as follows:

ROM	36	37	38	39	OPERATION
	0	0	1	1	MSB Address Load
	0	1	0	1	Increment MSB Address Register

2.6.6.1 Master Device TILINE Acquisition. Access to the TILINE is competitive between the TILINE masters on the bus; there is no centralized bus control logic. Conflicts between competing masters are settled by a positional priority system and a bus reservation scheme. The master device in the highest-numbered chassis slot has the highest priority. Priority ranking decreases with each chassis slot toward the 990 central processor, which has the lowest priority. The TLAG signal that runs through each TILINE master, establishes the priority, as shown in figure 2-18.

TLAGIN (from a higher priority master) enters each master on P2, pin 6, and TLAGOUT leaves the master on P2, pin 5. Logic on the master allows it to block the output to lower priority masters. Jumpers on the 990 backplane are installed to insure line continuity across slots not occupied by TILINE masters.

The master access logic of any TILINE master is based on a standard four-state access sequence. These states are: Idle, Device Access Request, Device Acknowledge, and Device Access, as shown in the master access flowchart, figure 2-19.

If the TILINE master does not have any data to transfer, the master access logic remains in the Idle state, and TLAG is passed on to lower priority masters. Do not confuse the Idle state of the master access logic with the idle mode of the DS10 controller. The idle mode of the controller refers to the controller operating on the idle loop of the microprogram ready to accept control words. The Idle state of the master access logic is the rest state of the access logic when it is not attempting to gain bus access and transfer a data word.

When the master requires access to the bus, it goes into the Device Access Request state and blocks TLAG to the lower priority masters. While in the Device Access Request state, the controller monitors TLAGIN. If TLAGIN is high, the controller can monitor TLAK- after a 200-nanosecond delay. A high TLAK- signal indicates that no other controller is in the Device Acknowledge state, and allows this controller to go into the Device Acknowledge state. The Device Acknowledge state is essentially a confirmed reservation for the next available bus access. The overlap of the current operation with reservations for the next operation reduces bus dead time and increases throughput.

In the Device Acknowledge state, the master access logic pulls TILINE acknowledge low to prevent any other controller going into the Device Acknowledge state. It continues to disable TLAGOUT,

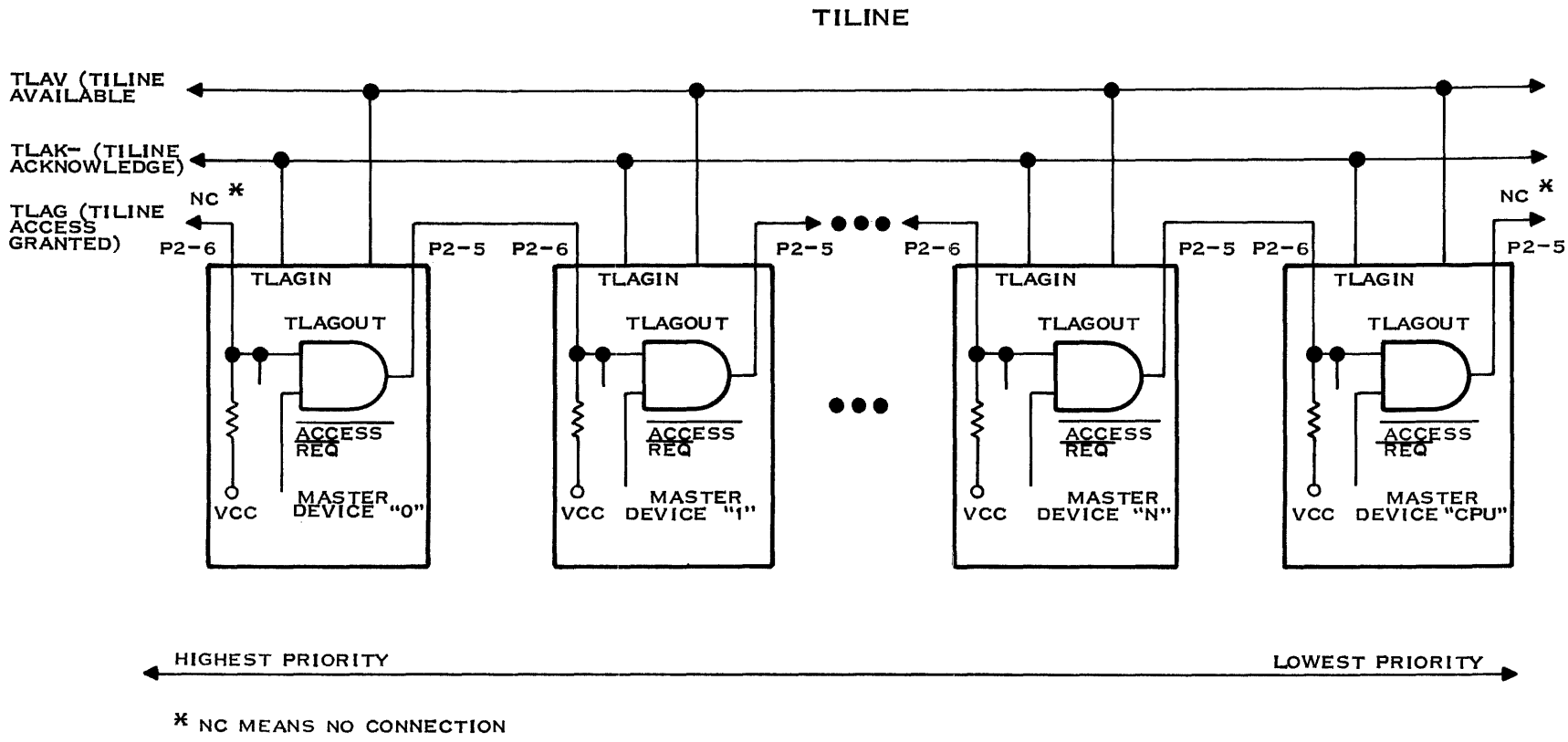


Figure 2-18. TILINE Master Devices Priority Interconnections

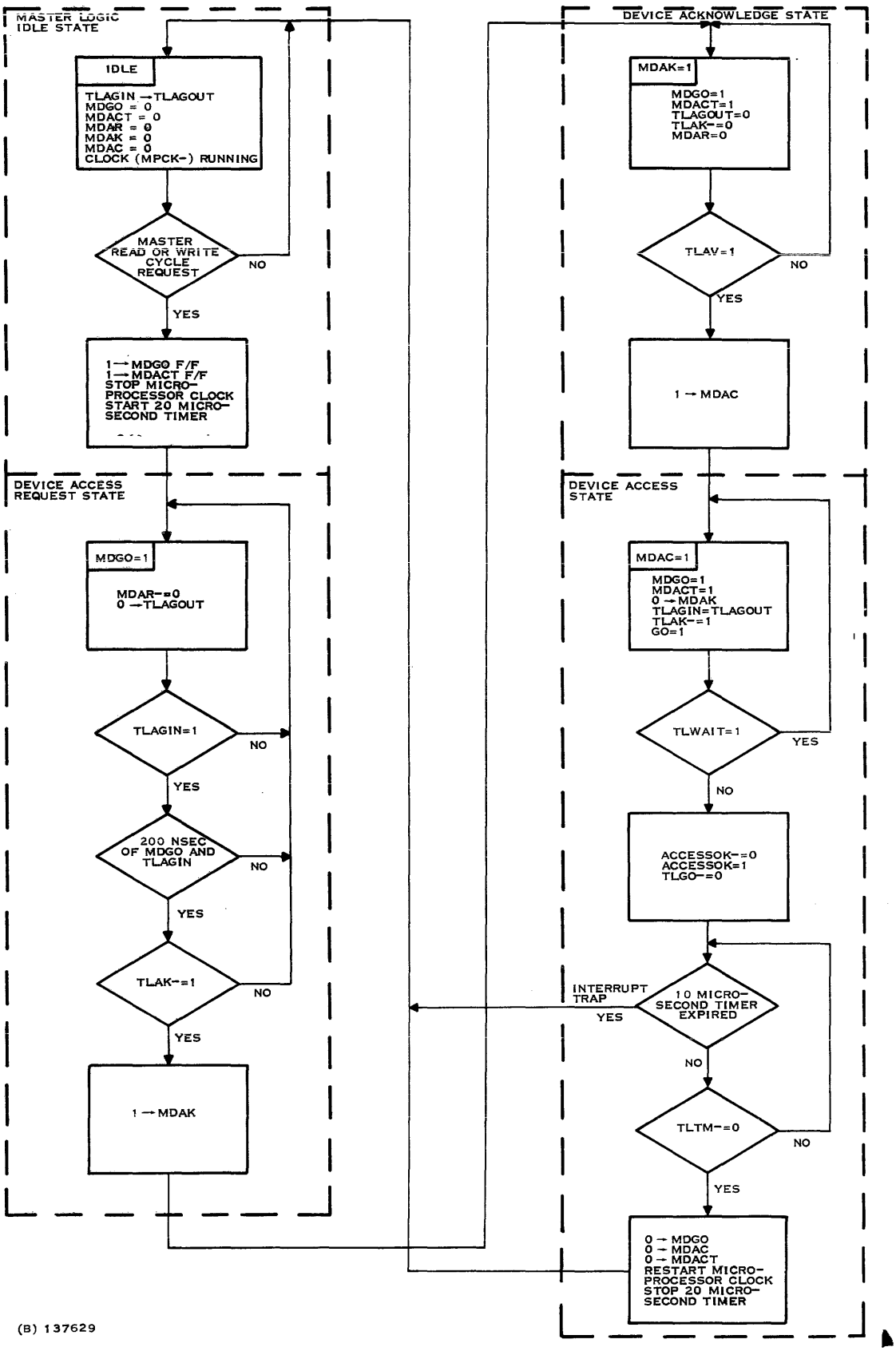


Figure 2-19. TILINE Master Access Flowchart

and monitors TILINE available. When TLAV goes high, the access logic advances to the Device Access state and initiates the read or write cycle. TLAGOUT is enabled so the next controller can prepare for access. At the end of the read or write cycle, the access logic clears the Device Access state, sending TILINE available to the other controllers, and returns to the Idle state.

2.6.6.2 Detailed Operation of TILINE Master Access Logic. Figure 2-20 shows the TILINE master access logic, and the flowchart of figure 2-19 shows the simplified sequence of operations.

TILINE master access operations are initiated by the TILINE control field of the microinstruction, bits 32 and 33, when the special field decoders are enabled by the K-bus control field, bits 10 and 11. The TILINE control field bits are decoded as follows:

ROM	32	33	Operation
	1	0	TILINE Master Read
	1	1	TILINE Master Write

Refer to the input of the master device go F/F at the left edge of the figure and assume that the new microinstruction specifies a TILINE master read or write. The resulting MSTSTB signal sets the master device go (MDGO) F/F that immediately sets the master device active (MDACT) F/F.

The microprogram disables the microprocessor clock (MPCK-) via the clock stop master special field combined with MDACT. Microprogram control of the clock allows the controller to suspend operations until the TILINE master cycle is completed. Clearing MDACT restarts the clock and allows program operations to continue.

The accessor signal active F/F initiates a 10-microsecond (approximate) TILINE timer. The 10-microsecond delay timer prevents a TILINE data transfer failure from hanging up TILINE and DS10 controller operations indefinitely. The timer is reset if a TILINE wait has been asserted by a TILINE bus coupler. The master device active F/F outputs also latch up the P-bus control register, and prepare the FIFO or direct register to accept or supply the data word.

The set output of the master device go F/F (MDGO) combines with the high MDAC- signal to disable the TILINE access granted output to lower priority TILINE masters.

If a higher priority master is holding TLAGIN low, there is a wait until that master lets TLAGIN return high. The high TLAGIN signal and the inactive (high) MDAK- signal enable MDAREN-. MDAR goes high, indicating that the access logic is in the device access request state. MDAR initiates a 200-nanosecond (approximate) delay, which determines the minimum time to advance to the next state.

If no other TILINE master is in the device acknowledge state, the low TILINE acknowledge (TLAK) signal and the delay output, MDAROK- combine to set the device acknowledge F/F. This advances the master access logic to the device acknowledge state.

The MDAK- signal disables MDAR, but MDAR- remains low, and continues to disable TLAGOUT to lower priority masters. The MDAK output to the TLAK- line driver prevents any other controller entering the device acknowledge state. At this time, the master access logic has an acknowledged reservation for the next available access. If another controller is in the device access state transferring data, there is a wait until the TILINE is available. When the TILINE becomes available, the TLAV- and MDAK- signals set the device access F/F, and the logic advances to the device access state.

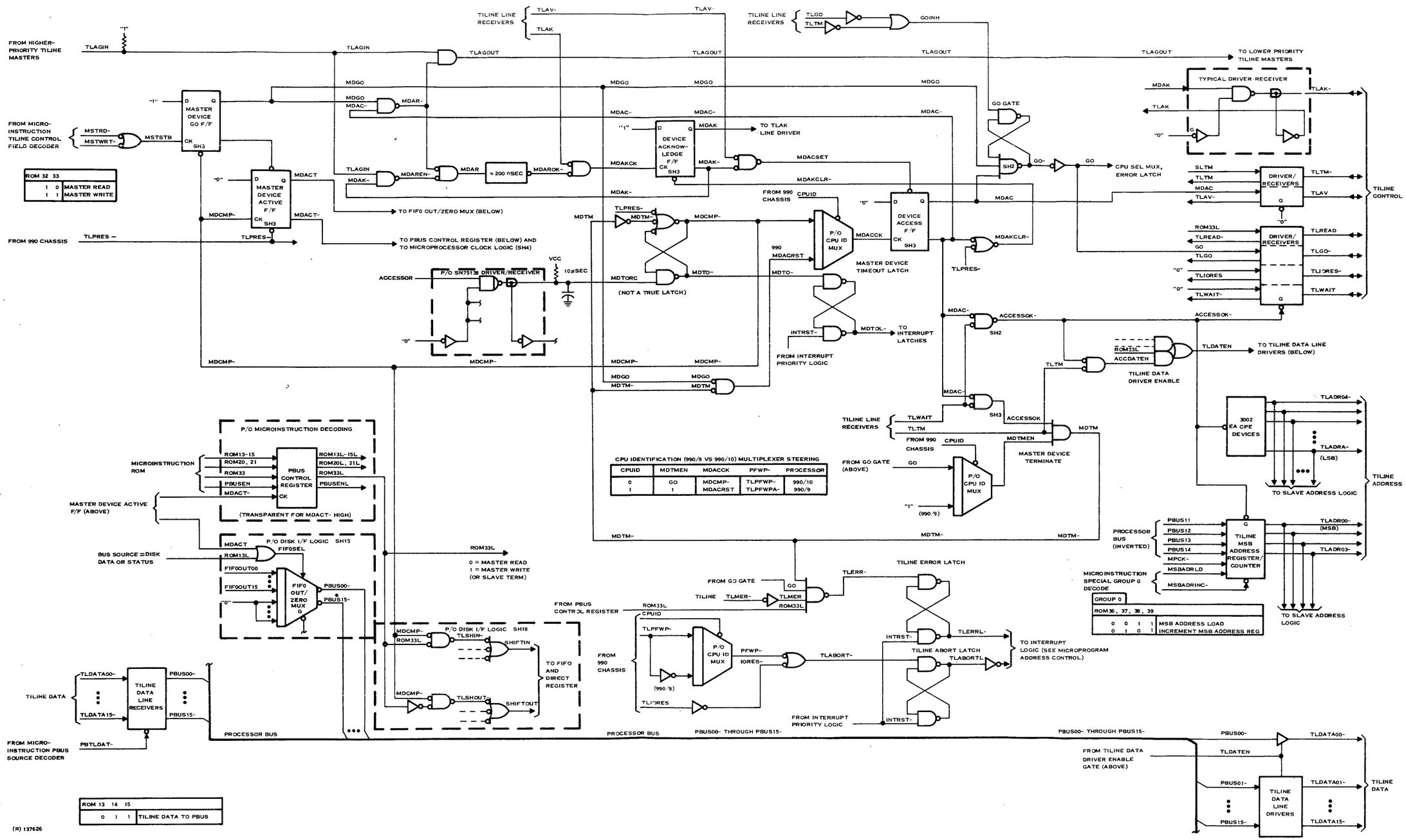


Figure 2-20. TILINE Master Access Logic

The MDAKCLR- signal clears the device acknowledge F/F, and the MDAC- signal reenables the TILINE access granted output so that lower priority masters may reserve the next bus access. The MDAC signal to the TILINE available line driver prevents any other master from entering the device access state.

The GO gate is a dual NAND latch which must be set to enable the GO output to the TLGO- line driver and other parts of the master access logic. An active TLGO- or TILINE terminate from another TILINE device will inhibit the setting of the latch, and prevent the DS10 controller from issuing a TLGO- to initiate the data transfer cycle.

Assume that the GO inhibit, GOINH, is low before MDAC sets. Both latch outputs are high. When MDAC sets, all three inputs to the GO- NAND gate are high, enabling the GO- output and setting the latch. Subsequent pulses on the GOINH line have no effect.

In the absence of a wait condition, MDAC- enables the ACCESSOK and ACCESSOK- gates. The ACCESSOK- signal serves as a strobe to enable the TLREAD and TLGO- line drivers. The TLREAD line driver is controlled by a latched version of microinstruction bit 33, ROM33L. This bit, which was latched in the PBUS control register by MDACT-, is zero for a master read and one for a master write operation. The TLGO- line driver is controlled by the GO output of the GO gate. The TLGO- driver tells all TILINE slave devices to decode the TILINE address. The addressed slave, after a protective slave go delay, will accept the data or supply the requested data, and issue the TILINE terminate (TLTML-) signal.

The ACCESSOK- signal also serves as a strobe to enable the 20-bit TILINE address outputs. The least significant 16 bits, TLADR04- through TLADR19-, are supplied by the memory address register outputs of the 3002 CPE array. The most significant four bits of the address, TLADR00- through TLADR03-, are supplied by a separate MSB address register/counter. The contents of the MSB address register are loaded (or incremented) by a previous microinstruction.

For a TILINE master write operation, TLDATEN gates the processor bus outputs, PBUS00- through PBUS15-, onto the data lines, TLDATA00- through TLDATA15-. TLDATEN is enabled by ACCESSOK- and ROM33L, until TILINE terminate (TLTM) occurs. ROM33L is a latched version of microinstruction bit 33.

The bus source is determined by latched versions of the microinstruction source control field, ROM13L-15L, as follows:

ROM	13L	14L	15L	Operation
	0	0	1	CPE data outputs to PBUS
	0	1	1	TILINE input to PBUS (master read or slave write)
	1	0	0	Disk data (from FIFO) to PBUS

The source selection was established by the same microinstruction which initiated the TILINE access.

For a TILINE master read operation, TLDATEN is not activated and instead, PBTLDAT- signal gates the TILINE line receiver outputs onto the processor bus.

The ACCESSOK and MDTMEN signals allow the logic to monitor the TILINE terminate signal and issue a master device terminate (MDTM) signal when it occurs. Notice that MDTMEN is supplied by a CPU ID multiplexer. The multiplexer is required because of minor timing differences between the 990/9 and 990/10 TILINE.

For a master read operation (ROM33L- = 1, GO =1), the master device terminate signal allows the TILINE error latch to monitor for a memory parity error signal (TLMER-) from the 990 memory. A parity error sets the TILINE error latch, which sends TLERRL- to the interrupt logic. When the CPU clock restarts, the controller microprogram will jump to the appropriate interrupt trap routine.

The MDTM signal is inverted to enable the master device complete (MDCMP-) signal. There are two important items to note at this point. First, the configuration of the MDTO- and MDCMP- gates is not a latch, despite the resemblance in configurations. A latch requires two inverting (NOR or NAND) gates. The MDCMP gate is an AND gate, and the gate pair cannot latch up. The second important item is that many of the functions controlled by MDTM are not activated until the trailing edge.

When MDTM initially goes high, MDCMP- goes low and performs two functions. A low MDCMP- signal forces the master device timeout (MDTO-) signal high, so that the master device timeout latch cannot set. Also, MDCMP- unconditionally clears the master device go F/F.

Clearing the MDGO F/F resets the GO gate, disabling the TILINE Go output to the slave (TILINE memory). The remaining operations are concerned with clearing the Device Access state and returning to the Idle state.

At this point, it is necessary to consider the timing differences between a 990/9 TILINE and a 990/10 TILINE. A chassis pin connection identifies the chassis type and steers the CPU ID multiplexer to select the appropriate terms.

First, in the 990/10 operation, from the time that MDGO resets and GO becomes inactive (low), the following things occur. The master device terminate enable (MDTMEN) equals GO, and MDTM drops immediately when the GO gate resets. This trailing edge of MDTM forces MDCMP- inactive (high), clocking both the master device active (MDACT) and device access (MDAC) flip-flops. Both flip-flops have hardwired logic zeros on the D inputs, and reset when clocked. With the TILINE master not active (MDACT = 0), the microprocessor clock cycle restarts and the microprogram starts executing on the next MPCK- pulse.

Clearing the Device Access state disables the ACCESSOK, ACCESSOK- and TLDATEN signals.

In the 990/9 operation, from the time that MDGO reset and GO went inactive (low) clearing of the device access state must wait until the slave (TILINE memory) responds to the loss of TILINE GO by dropping the TILINE terminate.

When TLTM goes low, MDTM also goes inactive (low). The low MDGO and MDTM signals enable MDACRST (master device access reset) which clocks the device access F/F. The clock pulse resets the device access F/F, disabling ACCESSOK, ACCESSOK- and TLDATEN. These signals disable data, address, and some control signal line drivers.

The trailing (falling) edge of MDTM forces MDCMP- high, clocking the master device active F/F. With the TILINE master not active (MDACT = 0), the microprocessor clock cycle restarts, and the microprogram starts executing on the next MPCK- pulse.

2.6.7 TILINE SLAVE OPERATION OF DS10 CONTROLLER. The DS10 disk controller acts as a TILINE slave when the 990 processor loads a control word (W0-W7) into the CPE internal registers or reads CPE register contents. Slave read and slave write operations are processed by trap routines in the DS10 controller microprogram. The microprogram must be cycling in the idle loop, with slave traps enabled, to process a slave read or write operation. In other words, the 990 processor cannot communicate with the CPE internal registers while the controller is busy.

2.6.7.1 TILINE Slave Read with Idle Controller. Figure 2-21 shows the logic dedicated to TILINE slave operations. For this description, assume that the controller is idle and the 990 processor requests the contents of slave word register R1 in the CPE array. The 990 processor, acting as a TILINE master, requests the word by sending a 20-bit TILINE address, a TILINE read signal, and the TILINE go strobe.

The TILINE slave address comparator checks 17 bits of the incoming address against the TILINE base address of the controller board. This address, which is partially hardwired and partially switch-selected, determines if the TILINE operation is addressed to the disk controller board. The three least significant bits of the TILINE address, TLADR17- through TLADR19-, are not involved in the comparison, as shown in figure 2-22. Table 2-3 shows the switch settings for selecting the TILINE base address.

NOTE

The physical layout of the switches does not follow binary order. Refer to the table for translation between switch settings and TILINE base addresses.

Table 2-3. TILINE Slave Address Switch Settings and Address

TILINE Address (Hex)	CPU Address (Hex)	Switches 1	2	3	4
FFC00	F800	Off	Off	Off	Off
FFC08	F810	Off	Off	Off	On
FFC10	F820	On	Off	Off	Off
FFC18	F830	On	Off	Off	On
FFC20	F840	Off	On	Off	Off
FFC28	F850	Off	On	Off	On
FFC30	F860	On	On	Off	Off
FFC38	F870	On	On	Off	On
FFC40	F880	Off	Off	On	Off
FFC48	F890	Off	Off	On	On
FFC50	F8A0	On	Off	On	Off
FFC58	F8B0	On	Off	On	On
FFC60	F8C0	Off	On	On	Off
FFC68	F8D0	Off	On	On	On
FFC70	F8E0	On	On	On	Off
FFC78	F8F0	On	On	On	On

The TLGO strobe is delayed approximately 100 nanoseconds to assure that the address has stabilized on the lines before the comparison. If the comparison is good (SLADOK = 1) at the end of the slave go delay, the slave transfer F/F sets. The slave go delay also clocks the slave write F/F to follow the TLREAD signal.

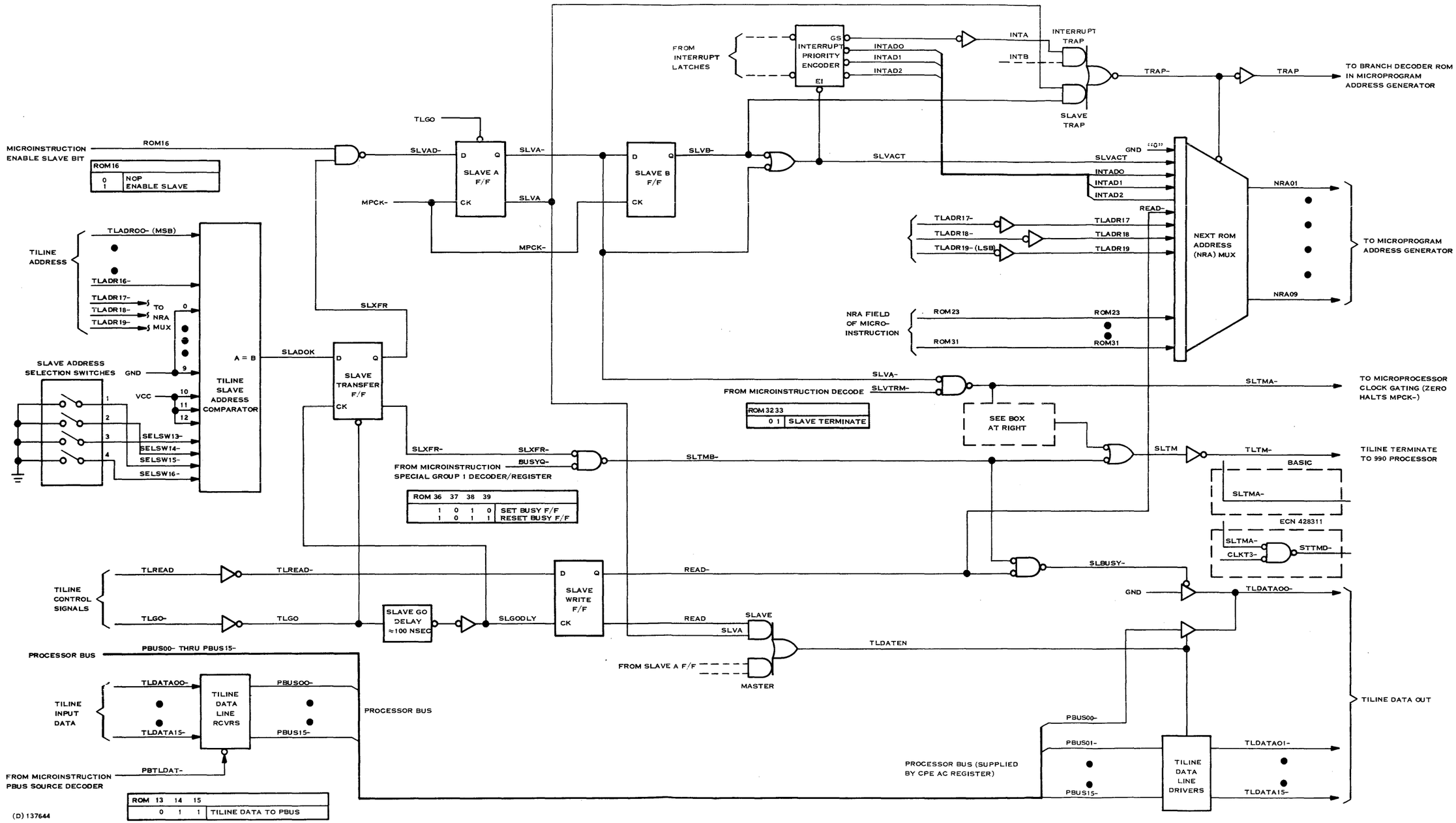


Figure 2-21. TILINE Slave Logic

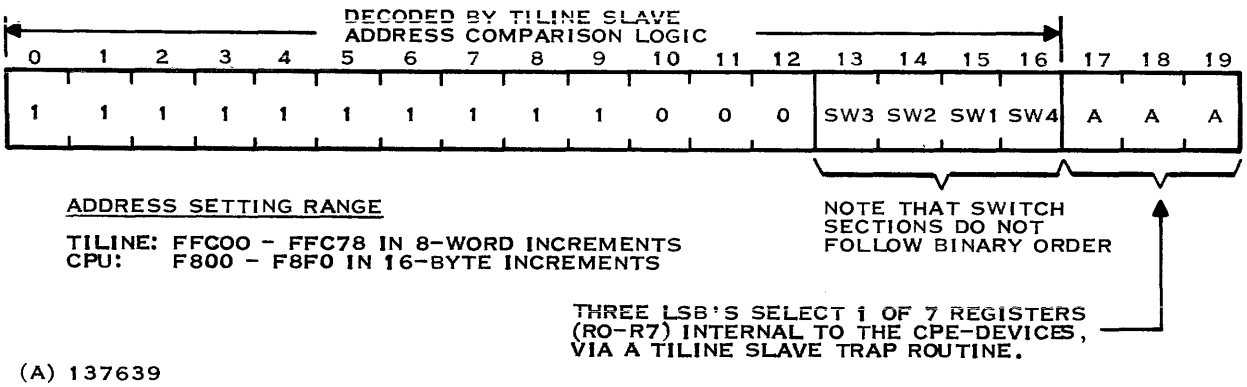


Figure 2-22. TILINE Slave Address Comparison

ROM 16, the enable slave clock bit, serves as a lockout to prevent a slave trap operation when the disk controller is not in the idle mode. The slave A F/F resets on the trailing edge of the first microprocessor clock pulse, forcing the interrupt priority encoder outputs, INTA- and INTAD0-2, to all ones and enabling TRAP-. Slave B resets on the next clock pulse to limit TRAP- to a single clock period.

The TRAP signal to the branch decoder ROM causes the microcode address generator to store the current address in the return stack and jump to the trap address selected by the next ROM address (NRA) multiplexer.

The TRAP- signal steers the NRA multiplexer to select the trap address as follows:

Address		Operation	
0F0	Slave Read	CPE Scratchpad	Register 0
0F1			1
0F2			2
0F3			3
0F4			4
0F5			5
0F6			6
0F7	Slave Read	CPE Scratchpad	Register 7
0F8	Slave Write	CPE Scratchpad	Register 0
0F9			1
0FA			2
0FB			
0FC			4
0FD			5
0FE			6
OFF	Slave Write	CPE Scratchpad	Register 7

The three least significant bits of the TILINE address in combination with the READ- and SLVACT signals select the appropriate trap address.

The slave read trap routine typically consists of two microinstructions. The first microinstruction transfers the selected CPE register contents into the CPE accumulator (AC) register in preparation for the transfer. The second microinstruction loads the AC contents onto the processor bus (PBUS00- through PBUS15-), and commands the TILINE slave operation terminate (ROM32, 33 = 01). This microinstruction also contains the return which directs the microprogram back to the idle loop. Both microinstructions hold the enable slave bit set.

The TLDATEN- signal enables the TILINE data line drivers when the slave A F/F is set, but the PBUS data is not meaningful at that time. The TILINE slave operation terminate in the last microinstruction is decoded to produce the SLVTRM- signal.

The SLVTRM- and SLVA- signals combine to produce the active low slave terminate access signal, SLTMA-. The slave terminate access signal stops the microprocessor clock and enables slave terminate (SLTM) to the TLTM- line driver. If ECN 428311 is installed, CLKT3- delays TLTM- approximately 115 nanoseconds after SLTMA-. TLTM- serves as a strobe to notify the TILINE master that valid slave data is currently available on the TILINE data lines. The master accepts the data and ends the TILINE cycle by releasing the TLGO- command.

When TLGO drops low, it clears the slave transfer F/F and presets the slave A F/F. The slave A outputs disable the TILINE data line drivers and the TILINE terminate signal, and restart the microprocessor clock.

The last microinstruction of the slave read operation continues active on the ROM 00 - 39 lines until the first clock pulse (MPCK-) from the restarted clock loads the return address from the stack in the microprogram address generators. This same MPCK- pulse clocks the slave B F/F, returning the slave logic to the original state and enabling the interrupt priority encoder. The one-state delay imposed by slave B assures that the microprogram executes at least one instruction in the idle loop before jumping to any pending interrupt trap routine.

2.6.7.2 TILINE Slave Read with Controller Not Idle. Before issuing a set of command words to the disk controller, the 990 computer must check the idle/not idle status of the controller by reading and testing W7, bit 0. If W7, bit 0 is a one, the controller is not busy with some operation, and the controller microprogram is cycling in the idle loop ready to accept commands. If W7, bit 0 is a zero, the controller is busy (not idle), and cannot execute a slave trap operation.

The busy F/F and logic allow the disk controller to respond wtih a simulated W7 word if the controller is busy. This simulated W7 word has a 0 at bit 0 to identify not idle status, and bits 1-15 are meaningless. No slave read trap operations are performed, and the on-going controller operation is not disrupted.

Assume that the controller has been commanded to perform some operation, so that the microprogram branches from the idle loop to the initialize routine. The first microinstruction of this routine (INI00, location 02E) disables the slave traps (ROM 16 = 0) and sets the busy F/F. Special field one of the microinstruction controls the busy F/F as follows:

Group Select			**Special Field 1**					
ROM	34	35	ROM	36	37	38	39	
	0	1		1	0	1	0	Set Busy F/F
	0	1		1	0	1	1	Reset Busy F/F

The busy F/F is one stage of the SN74LS259 8-bit addressable latch that comprises the special group 1 decoder register. The busy F/F remains set (busy- = 0) until the last instruction of the terminate routine (TRM25, location 0DF) is executed. This instruction also includes a branch to the Idle routine.

Assume that the 990 computer attempts to check the idle/not idle status with a TILINE read operation addressed to CPE scratchpad register 7. The TLREAD- output of the TILINE line receiver is 0 to identify a read operation, and the slave address compares (SLADOK = 1) to the board address. At the expiration of the slave go delay, the slave transfer F/F sets and the slave write F/F resets.

The enable slave bit (ROM 16) is zero, so the slave A and slave B F/Fs are not allowed to enter a trap cycle. TLDATEN is held low, disabling the line drivers for TLDATA01- through TLDATA15-, and disabling one of the two TLDATA00- line drivers. The outputs of the slave transfer and busy flip-flops combine to enable the active low slave terminate-busy (SLTMB-) gate. SLTMB- enables an immediate TILINE terminate signal to the 990 computer. The SLTMB- signal combined with the READ-signal enables the hardwired TLDATA00- driver. The line driver output of the driver corresponds to a 0 in the bit 0 position of the simulated W7 word, indicating that the controller is busy. The bit 0 line driver remains active until the 990 computer signals the end of the TILINE cycle by releasing the TLGO. The low TLGO signal clears the slave transfer F/F, disabling the TILINE terminate and data bit 0 line drivers.

Microprocessor clock is not stopped and microprogram execution is not affected by this cycle.

The three LSBs of the TILINE address are not decoded. This means that a read operation addressed to any of the eight slave registers will be treated as though it were addressed to R7, if the controller is busy. It is the responsibility of the device service routine programmer to assume that idle status is checked before attempting to read R0-R7.

If the 990 computer attempts a write operation to the disk controller while it is busy, the SLTMB- gate issues an immediate terminate signal and the controller does not accept the word. Again, it is the responsibility of the device service routine programmer to check idle status before attempting to transmit control words to the disk controller. The device service routines supplied wtih DX10 and other DS10 disk-compatible operating systems perform this check in a manner transparent to the user program.

2.6.7.3 Slave Write. The DS10 disk control words are loaded into the CPE registers during a sequence of eight slave write operations. Operation of the TILINE slave logic is similar to slave read operations except for the state of the slave write F/F and the direction of TILINE data flow.

Assume that the DS10 disk controller is in the idle mode and the 990 computer sends a control word W1 over the TILINE. The slave address comparator compares the 17 most significant TILINE addresses against the board address. The 100-nanosecond slave go delay assures that the address and TILINE data word are stable before clocking the slave transfer and slave write flip-flops. The enable slave bit (ROM 16) is set, enabling the slave A flip-flop to initiate the slave trap operation.

The trap address is determined by the three least significant bits of the TILINE address, the READ- signal (READ = 1) and the slave active (SLVACT = 1) signal. Trap address assignments are included with the slave read description.

A slave write trap routine contains a minimum of two microinstructions. The slave write traps for R0 and R6 are longer because they perform additional functions, but the operation of the TILINE slave logic remains the same. The bus source field (ROM 13-15) of the first microinstruction gates the

incoming TILINE data word onto the processor bus. The PBTLDAT- signal from the PBUS source decoder enables the line receiver outputs onto the bus. The CPE function code (ROM 01 - 07) commands the CPE array to read the PBUS contents into the accumulator. The enable slave bit (ROM 16) remains set for both microinstructions.

The second microinstruction transfers the data word from the accumulator to the specified scratchpad register, R0 - R7. The TILINE operation field (ROM 32, 33) commands TILINE slave operation terminate (SLVTRM-).

The SLVTRM- signal combines with the output of the slave A F/F to disable the microprocessor clock (SLTMA-) and issue a TLTM- signal. If ECN 428311 is installed, TLTM- is delayed approximately 115 nanoseconds by CLKT3-. The microprocessor clock remains in the holding state until the 990 computer releases the TLGO, ending the TILINE cycle. The low TLGO signal clears the slave transfer F/F and presets the slave A F/F, so microprocessor clock is restarted.

The next microprocessor clock pulse returns microprogram execution to the point in the idle loop where the slave trap occurred. It also clocks the slave B F/F, which returns the slave logic to the initial state and enables the interrupt logic.

2.7 3002 CENTRAL PROCESSING ELEMENTS (CPEs)

The disk controller uses an array of eight 3002 bit-slice central processing elements controlled by a permanent on-board microprogram to execute the disk control commands. The CPE array is organized as 8-bit left and right bytes. Each 3002 device is a 2-bit slice of a general-purpose processor. The principle features of a 3002 CPE are:

- Eleven scratchpad registers (R0-R9 and T)
- A full-function accumulator register (AC)
- Independent memory address output register (MAR)
- Two 3-state, fully buffered output buses (A, D)
- Three independent input buses (M, I, K)
- Full look-ahead and ripple carry
- Two's complement arithmetic
- Logical AND, OR, NOT, exclusive-NOR
- Left shift or right shift
- Bit testing and zero detection
- Single clock input, which may be conditional for nondestructive bit and word testing.

2.7.1 3002 CPE BLOCK DIAGRAM. Refer to figure 2-23 which is a functional block diagram of a single 3002 device. Note that the three input data buses (M, I, K) and the two output data buses (A, D) use an active-low signal level to represent a data one. That is, a data one is represented by a voltage level less than 0.8 volts, and a data zero is represented by a voltage greater than 2.8 volts. The bubbles on the device outline identify the active low input and output lines. Table 2-4 lists the CPE input and output signals.

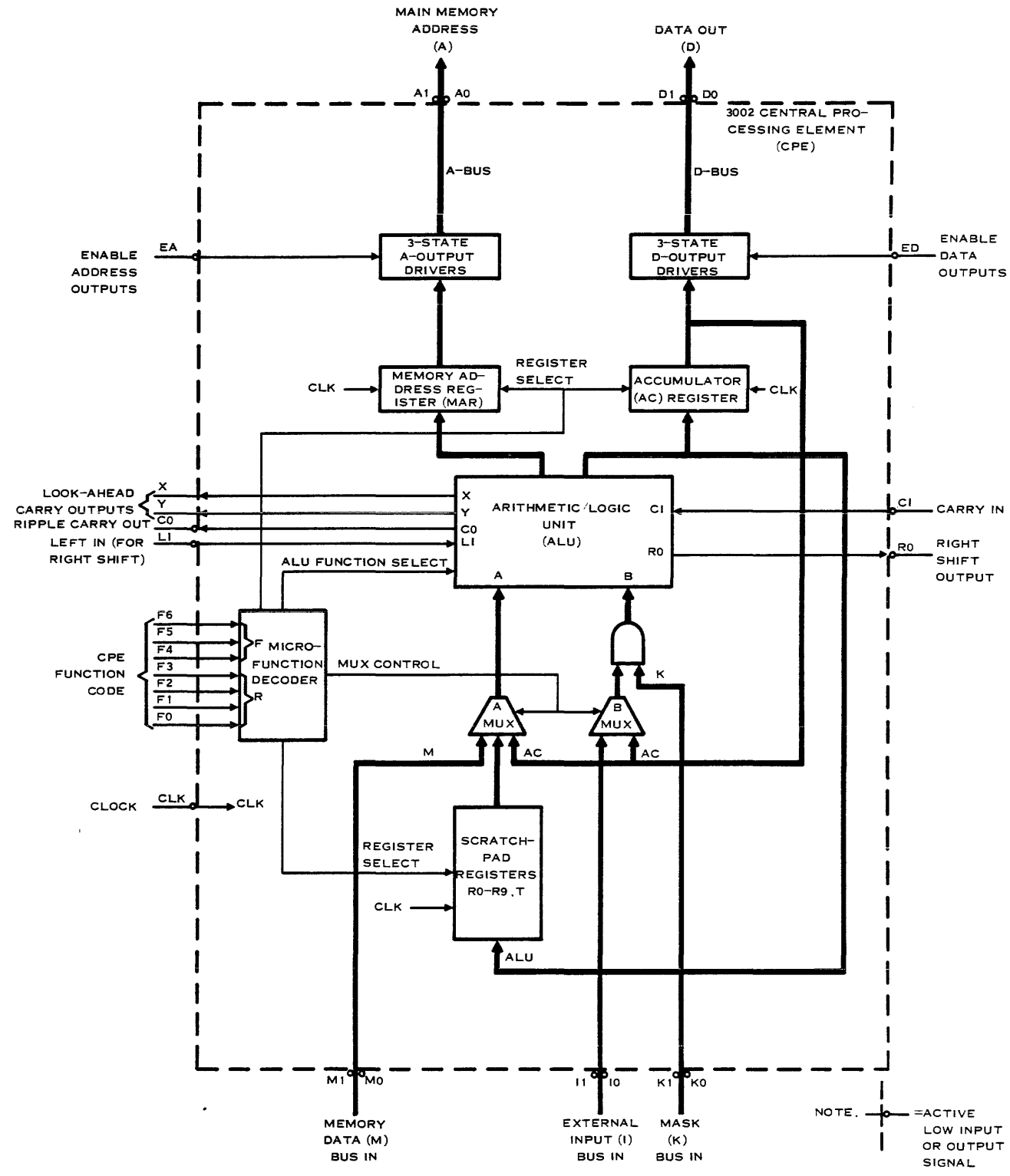


Figure 2-23. 3002 CPE Block Diagram

The three input data buses (M, I, K) are shown at the bottom of the figure. The M-bus is the main data input of the CPE as used in the disk controller. The M-bus inputs are connected to the processor bus (PBUS), which is the main data path through the controller. The I-bus is used for reading flags into the CPE array. The K-bus is also known as the mask bus, because the K-bus inputs are ANDed, bit-for-bit, with the ALU B-input operand. For some instructions, the B-multiplexer output is set to all ones, so the K-bus data can be used as an immediate operand.

There are 11 general purpose scratchpad registers (R0-R9, T) in the CPE. Each of these registers may be individually loaded with data from the ALU output and the contents of any of these registers may be selected as an ALU input operand. Scratchpad registers R0 through R7 are used as TILINE slave registers. They are used to store control words W0 - W7, respectively, from the 990 processor.

Two multiplexers select the operand inputs to the arithmetic/logic unit (ALU). The inputs to multiplexer A are accumulator register (AC), the selected scratchpad register, and the M-bus inputs. The inputs to multiplexer B are the accumulator register or the I-bus inputs. The outputs of multiplexer B are ANDed bit-for-bit with the K-bus inputs, allowing the K-bus contents to be used to mask the I-bus inputs or the accumulator contents. Multiplexer B outputs can be selected to all ones, gating the K-bus inputs into the ALU.

Table 2-4. 3002 CPE Input and Output Functions

CPE Pins	CPE Bus	Controller Signal	Name and Description	Type Signals
1, 2	I_0 - I_1		External bus input. The external bus input provides a separate input port for external input devices.	Active low
3, 4	K_0 - K_1	CPK(00 - 15)–	Mask bus input. The mask bus input provides a separate input port for the microprogram memory, to allow mask or constant entry.	Active low
5, 6	X, Y	CPX(0-7), CPY(0-7)	Standard carry look-ahead cascade outputs.	Active high
7	CO		Ripple carry output. The ripple carry output is only disabled during shift right operations. Not used.	Active low Three-state
8	RO	CPSHIFT(N)–	Shift right output. The shift right output is only enabled during shift right operations.	Active low Three-state
9	LI	CPSHIFT(N)–	Shift right input.	Active low
10	CI	CARRY(0-6)–	Carry input.	Active low

Table 2-4. 3002 CPE Input and Output Functions (Continued)

CPE Pins	CPE Bus	Controller Signal	Name and Description	Type Signal
11	EA	ACCESSOK–	Memory address enable input. When in the low state, the memory address enable input enables the memory address outputs, TLADR(04-19)–.	Active low
12, 13	A_0 - A_1	TLADR(04-19)–	Memory address bus output. The memory address bus output is the buffered output of the memory address register (MAR).	Active low Three-state
14	GND		Ground.	
15-17	F_6 - F_0	ROM(01-07)	Microfunction bus input. The microfunction bus input controls ALU function and register selection.	Active high
18	CLK	CPRCK– or CPLCK–	Clock input.	
19, 20	D_0 - D_1	PBUS(00-15)–	Data bus output. The data bus output is the buffered output of the full function accumulator register.	Active low Three-state
21, 22	M_0 - M_1	PBUS(00-15)–	Data bus input. The data bus input provides a separate input port for data.	Active low
23	ED	PBCPE–	Data enable input. When low, the data enable input enables the data output, PBUS(00-15)–.	Active low

The arithmetic/logic unit (ALU) performs a variety of arithmetic and logic operations on the input operands, including two's complement addition, incrementing, shifting, logical AND, logical OR, exclusive-NOR and logical complements. The ALU has provisions for a carry input (CI) from a less significant stage, and both ripple (CO) and look-ahead (X, Y) carry outputs to more significant stages. The ALU has a right-shift output (RO) and a left-bit input (LI) for right shift operations.

The ALU has two sets of output lines, one to the MAR, and one to the AC and the scratchpad registers. The accumulator contents may be used as operand inputs for the next operation, or gated out of the CPE via the three-state D-bus output drivers. The output drivers are gated by the enable data (ED) input. In the disk controller, all the CPEs are simultaneously enabled by the PBCPE- signal on the ED inputs.

The MAR outputs may be gated out of the CPE by the three-state A-bus output drivers. The drivers are enabled by the enable address (EA) input. In the disk controller, the TILINE access OK

(ACCESSOK-) signal enables the A-bus outputs, which supply 16 bits of the TILINE address for master operations.

The microfunction decoder provides the register selection, ALU input multiplexer steering, and ALU function control signals based on a seven-bit CPE function code, inputs F6-F0. The CPE function code is supplied by seven bits (ROM 01 - 07) of the 40-bit microinstruction ROM. Note that the numbering of the ROM bus function code runs counter to the F6-F0 numbering on the device.

The clock input is used to load the results of an ALU operation into the selected registers. Clocking occurs on the negative-going transition of the external clock. The CPEs in the left byte are clocked by the CPE left byte clock (CPLCK-) and the right byte CPEs are clocked by CPE right byte clock (CPRCK-). The CPRCK- and CPLCK- signals are in phase with microprocessor clock (MPCK-), but are gated by the word select field and clock stop bit of the 40-bit microinstruction.

The ALU function control, register output selection and multiplexer steering are not clocked. It is possible to command operations and test the results via the nonclocked carry or right shift output without altering the contents of any CPE registers. The clock pulse which would store the results of the operation is omitted under microprogram control. During nonarithmetic operations, the carry circuits perform a wordwise inclusive-OR of the ALU output bits. This can be used to test the results of an ALU operation or register contents for a nonzero value. If masking is also specified, individual bits or bit groupings may be tested. Bit testing is described in detail with the CPE carry and shift logic.

Figure 2-24 summarizes the CPE internal operating sequence in flowchart form.

2.7.2 CPE INSTRUCTION SET INTRODUCTION. During each microinstruction, a CPE function code on the ROM bus, ROM (01-07), is applied to the function code (F-bus) inputs of the 3002 CPEs. These inputs on the F-bus are decoded within the 3002 CPEs by the microfunction decoder. Within the CPEs, the operands are selected by the A and B multiplexers, the appropriate scratchpad registers are addressed, and the specified operation is performed by the ALU. The result of the ALU operation may be loaded into the AC, the MAR, or one of the scratchpad registers.

The conditional branching and return microinstructions use the results of CPE internal bit or register tests to control the branch, as described with the CPE carry and shift logic. The clock input to the CPE may be omitted (under control of ROM 00) during these conditional operations. This allows the unclocked carry and shift outputs to be used for testing without altering the CPE register contents.

CPE operations for each of the microinstructions are documented in the flowchart descriptions of the microprogram, Appendix C, and microinstruction listing, Appendix D.

2.7.3 FUNCTION CODE FORMATS. The most significant three bits of the function code, ROM (01-03), specify one of seven F-groups, as shown in table 2-5. Each F-group determines a type of operation. The other four bits, ROM (04-07), are used for register selection as shown in table 2-6. The registers are divided into three groups, R-group I, R-group II, and R-group III. The register group number modifies the function specified by the F-group. R-group I contains scratchpad registers R0-R9, T, and AC (designated R_n for convenience). R-groups II and III contain only the T and AC registers. Reference to the table shows that there are three individual codes which select the T register: C_{16} (R-group I), A_{16} (R-group II), or E_{16} (R-group III). The AC register may also be selected by any of three codes: D_{16} (R-group I), B_{16} (R-group II), or F_{16} (R-group III). The CPE function descriptions in the next paragraph are keyed to this F-group and R-group scheme.

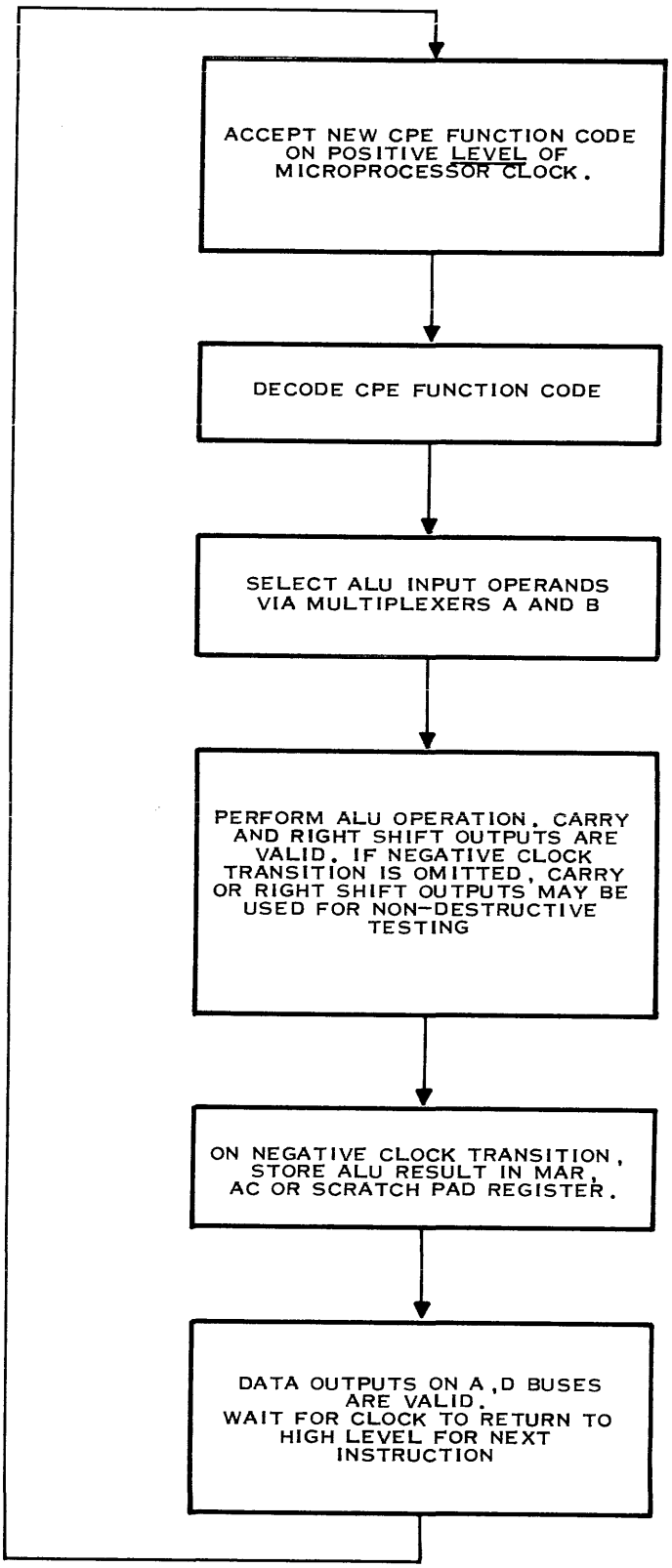


Figure 2-24. CPE Internal Operating Sequence

Table 2-5. Function Group (F-group) Format

F-Group	ROM 01 (F6)	ROM 02 (F5)	ROM 03 (F4)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 2-6. Register Group (R-group) Format

R-Group	Registers		ROM 04 (F3)	ROM 05 (F2)	ROM 06 (F1)	ROM 07 (F0)	Hexadecimal Code
	R_0		0	0	0	0	0
	R_1		0	0	0	1	1
	R_2		0	0	1	0	2
	R_3		0	0	1	1	3
	R_4		0	1	0	0	4
I	R_5	R_n	0	1	0	1	5
	R_6		0	1	1	0	6
	R_7		0	1	1	1	7
	R_8		1	0	0	0	8
	R_9		1	0	0	1	9
	T		1	1	0	0	C
	AC		1	1	0	1	D
II	T		1	0	1	0	A
	AC		1	0	1	1	B
III	T		1	1	1	0	E
	AC		1	1	1	1	F

2.7.4 CPE FUNCTIONS. Table 2-7 is a summary of the 3002 CPE functions. The summary is in generalized form, with no assumptions about the data on the mask bus. If the K-bus contents are 00 or 11, the general Boolean expressions are considerably simplified. Each F-group/R-group combination is briefly described below.

In step 1 of table 2-7 (F-group 0, R-group I), the contents of the AC are logically ANDed with the data on the K-bus. The result of this ANDing is added to the contents of R_n and also to the value of the carry input (CI). The sum is placed in R_n and AC.

In step 2 (F-group 0, R-group II), the contents of AC are logically ANDed with the data on the K-bus. The result is added to the data on the M-bus and also added to CI (carry input). The sum is deposited in AC or T, as specified.

Step 3 (F-group 0, R-group III), if the K-bus contents are zero, shift AC or T-register one bit to the right. The lower-order bit is shifted out on R_0, and the higher order bit is filled from LI. If the K-bus contents are nonzero, the shift is a function of both the I-bus and K-bus contents.

In step 4 (F-group 1, R-group I), the data on the K-bus is logically ORed with the contents of R_n. The result is placed in the MAR. Also, the contents of R_n is added to the data on the K-bus and to carry in (CI). The result is deposited in R_n.

In step 5 (F-group 1, R-group II), the data on the K-bus is ORed with the data on the M-bus. The result is deposited in the MAR. Also, the data on the M-bus is added to the data on the K-bus and to CI. The sum is deposited in AC or T, as specified.

In step 6 (F-group 1, R-group III), the complement of the contents of AC or T, as specified, is ORed with the data on the K-bus. The result is added to the logical AND of the specified AC or T-register and the data on the K-bus. The sum is added to CI and the result is deposited in AC or T, as specified.

In step 7 (F-group 2, R-group I), the contents of AC are ANDed with the data on the K-bus. The value of 1 is subtracted from the result and the difference is added to CI. The sum is deposited in R_n.

In step 8 (F-group 2, R-group II), the data on the K-bus is ANDed with the contents of AC. The value of one is subtracted from the result and the difference is added to CI. The sum is deposited in AC or T, as specified.

In step 9 (F-group 2, R-group III), the data on the I-bus is ANDed with the data on the K-bus. One is subtracted from the result and the difference is added to CI. The sum is deposited in AC or T, as specified.

In step 10 (F-group 3, R-group I), the contents of AC are ANDed with the data on the K-bus. The result is added to the contents of R_n and to CI. The sum is deposited in R_n.

In step 11 (F-group 3, R-group II), the contents of AC are ANDed with the data on the K-bus. The result is added to the data on the M-bus and to CI. The sum is deposited in AC or T, as specified.

In step 12 (F-group 3, R-group III), the data on the I-bus is logically ANDed with the data on the K-bus. Add the result to AC or T as specified, and to CI. Deposit the sum in AC or T, as specified.

In step 13 (F-group 4, R-group I), logically AND the data on the K-bus with the contents of AC. Logically AND the result with the contents of R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.

Table 2-7. Summary of CPE Microfunctions

Step	F-Group	R-Group	Microfunctions	
1		I	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	
2	0	II	$M + (AC \wedge K) + CI \rightarrow AT$	
3		III	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$	$LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)] \vee [AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$
4		I	$K \vee R_n \rightarrow MAR$	$R_n + K + CI \rightarrow R_n$
5	1	II	$K \vee M \rightarrow MAR$	$M + K + CI \rightarrow AT$
6		III	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	
7		I	$(AC \wedge K) - 1 + CI \rightarrow R_n$	(See Note (1))
8	2	II	$(AC \wedge K) - 1 + CI \rightarrow AT$	
9		III	$(I \wedge K) - 1 + CI \rightarrow AT$	
10		I	$R_n + (AC \wedge K) + CI \rightarrow R_n$	
11	3	II	$M + (AC \wedge K) + CI \rightarrow AT$	
12		III	$AT + (I \wedge K) + CI \rightarrow AT$	
13		I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \wedge (AC \wedge K) \rightarrow R_n$
14	4	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \wedge (AC \wedge K) \rightarrow AT$
15		III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \wedge (I \wedge K) \rightarrow AT$
16		I	$CI \vee (R_n \wedge K) \rightarrow CO$	$K \wedge R_n \rightarrow R_n$
17	5	II	$CI \vee (M \wedge K) \rightarrow CO$	$K \wedge M \rightarrow AT$
18		III	$CI \vee (AT \wedge K) \rightarrow CO$	$K \wedge AT \rightarrow AT$
19		I	$CI \vee (AC \wedge K) \rightarrow CO$	$R_n \vee (AC \wedge K) \rightarrow R_n$
20	6	II	$CI \vee (AC \wedge K) \rightarrow CO$	$M \vee (AC \wedge K) \rightarrow AT$
21		III	$CI \vee (I \wedge K) \rightarrow CO$	$AT \vee (I \wedge K) \rightarrow AT$
22		I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \,\overline{\oplus}\, (AC \wedge K) \rightarrow R_n$
23	7	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \,\overline{\oplus}\, (AC \wedge K) \rightarrow AT$
24		III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \,\overline{\oplus}\, (I \wedge K) \rightarrow AT$

NOTE: (1) 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

LEGEND:

Symbol	Meaning
I, K, M	Data on the I, K, and M buses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group 1)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
+	2's complement addition
-	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
$\rightarrow$	Deposit into
H	As a subscript, refers to the higher order bit of the 2 bits in a CPE device
L	As a subscript, refers to the lower order bit of the 2 bits in a CPE device

In step 14 (F-group 4, R-group II), logically AND the data on the K-bus with the contents of AC. Logically AND the result with the data on the M-bus. Deposit the final result in AC or T, as specified. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the CO line.

In step 15 (F-group 4, R-group III), logically AND the data on the I-bus and the data on the K-bus. Logically AND the result with the contents of AC or T, as specified. Deposit the final result in the specified register, AC or T. Logically OR CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the CO line.

In step 16 (F-group 5, R-group I), logically AND the data on the K-bus with the contents of R_n. Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on the CO line.

In step 17 (F-group 5, R-group II), logically AND the data on the K-bus with the data on the M-bus. Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on the CO line.

In step 18 (F-group 5, R-group III), logically AND the data on the K-bus with the contents of AC or T, as specified. Deposit the result in the specified register, AC or T. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on the CO line.

In step 19 (F-group 6, R-group I), logically OR CI with the word-wise OR of the logical AND of AC and the data on the K-bus. Place the result of the carry OR on the CO line. Logically OR the contents of R_n with the logical AND of AC and the data on the K-bus. Deposit the result in R_n.

In step 20 (F-group 6, R-group II), logically OR CI with the word-wise OR of the logical AND of AC and the data on the K-bus. Place the value of the carry OR on the CO line. Logically OR the data on the M-bus with the logical AND of AC and the data on the K-bus. Deposit the final result in AC or T, as specified. Deposit the final result in the specified register, AC or T.

In step 21 (F-group 6, R-group III), logically OR CI with the word-wise OR of the logical AND of the data on the I-bus and the data on the K-bus. Place the value of the carry OR on the CO line. Logically AND the data on the I-bus with the data on the K-bus. Logically OR the result with the contents of AC or T, as specified. Deposit the final result in the specified register, AC or T.

In step 22 (F-group 7, R-group I), logically OR CI with the word-wise OR of the logical AND of the contents of R_n and AC and the data on the K-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the contents of AC. Exclusive-NOR the result with the contents of R_n. Deposit the final result in R_n.

In step 23 (F-group 7, R-group II), logically OR CI with the word-wise OR of the logical AND of the contents of AC and the data on the K-bus and the M-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the contents of AC. Exclusive-NOR the result with the data on the M-bus. Deposit the final result in AC or T, as specified.

In step 24 (F-group 7, R-group III), logically OR CI with the word-wise OR of the logical AND of the contents of the specified register (AC or T) and the data on the I-bus and the K-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the data on the I-bus. Exclusive-NOR the result with the contents of AC or T, as specified. Deposit the final result in the specified register, AC or T.

2.7.5 CPE ARRAY

The DS10 disk controller uses an array of eight 3002 central processing elements to perform masking, shifting, logic, and arithmetic operations on status, control, and data words. The CPE array is organized into an eight-bit left byte and an eight-bit right byte, each comprised of four CPEs.

The CPE array may operate in left byte mode, right byte mode or full word mode, as determined by the WS field (ROM08, 09) of the current microinstruction. The WS field controls gating of the left byte clock (CPLCK-), right byte clock (CPRCK-) and the routing of CPE carry and shift signals.

Typical full word operations include accepting a control word (W0 - W7) from the TILINE during a slave write trap generation, supplying a status word to the TILINE during a slave read trap, supplying a header word to the disk drive, and performing calculations with 16-bit control words and housekeeping data in the CPE internal registers. Note that the main disk to 990 memory or 990 memory to disk data flow does not go through the CPE array. After the initial header set-up/check, the main buffer operation takes place over the PBUS. The CPE array does, however, perform housekeeping calculations and tests between successive TILINE master cycles. Recall from the description of the TILINE master access logic that a separate TILINE master cycle is required for each word transfer.

Typical left-byte operations include masking and testing the flag bits connected to the I-bus inputs of the left-byte CPEs, performing calculations and tests on control word fields which lie in the left byte (0-7) of the CPE internal registers, and loading data into the unit select register.

Typical right-byte operations include masking and testing the flag bits connected to the I-bus inputs of the right byte CPEs, performing calculations and tests on control word fields stored in the right byte (8-15) of the CPE internal registers, and loading the most significant TILINE bits into the TILINE MSB address register.

This list of typical operations is not intended to be exhaustive, but to illustrate that in many cases it is possible to conserve CPE internal register space by performing byte rather than full word operations. The flowcharts of Appendix C are clearly annotated to identify left byte, right byte, and full word operations.

Refer to figure 2-25, the simplified diagram of the CPE array inputs and outputs. The diagram shows the relationship between the microprogram ROM, the CPE array, the CPE carry and shift logic, and the CPE input and output buses.

All the CPE devices receive the same function code on bits 1-7 of the ROM bus, but do not store the results in the internal registers until the negative-going transition of the clock pulse. The clock pulse to both bytes may be disabled by the CPE conditional clock bit (ROM00). Also, left byte clock is disabled for right byte operations (ROM08, 09 = 11) and right byte clock is disabled for left byte operations (ROM08,09 = 10). Both CPE left and right byte clocks are gated versions of MPCK-.

The three-state D-bus output drivers are driven by the CPE accumulator AC register contents and enabled on a full-word basis. The CPE to P-bus enable signal (PBCPE-) is connected in parallel to the enable data (ED) inputs of all the CPEs. It is possible to enable the 16 data outputs during a left or right byte operation. For example, loading the four most significant TILINE address bits into the TILINE MSB address register is a right-byte operation involving PBUS 11-14. All 16 CPE accumulator output bits are placed on the P-bus. The MSB address load signal, decoded from the special group 00 of the microinstruction, loads the applicable four bits into the MSB address register. The unused 12 bits appear on the bus, but do not affect operations.

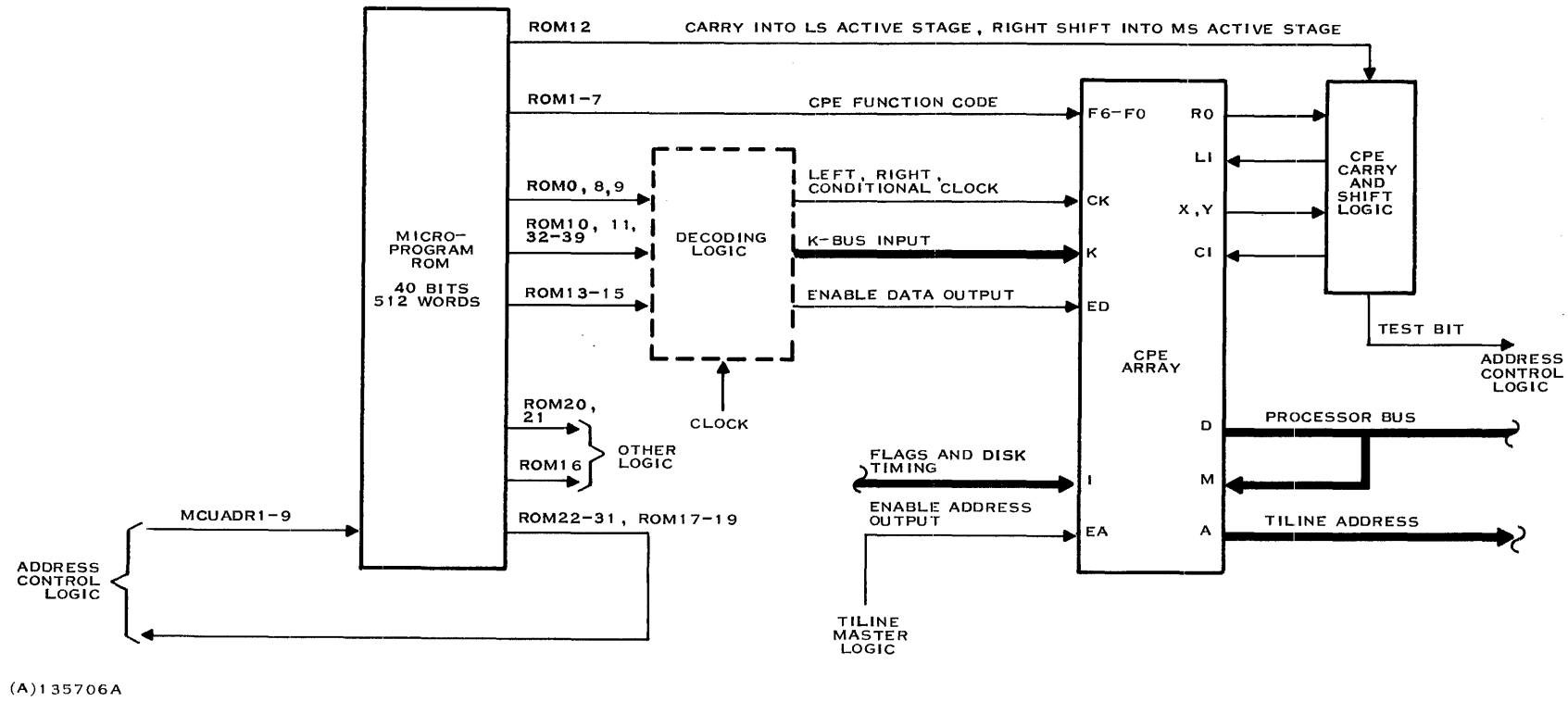


Figure 2-25. CPE Array Simplified Inputs and Outputs

The address (A-bus) outputs are enabled on a full-word basis by the TILINE access OK output of the TILINE master logic. The A-bus outputs supply the 16 least significant bits (TLADR04- through 19-) of the TILINE address during a TILINE master cycle operation. This is the only use of the CPE A-bus outputs.

The CPE array has three input buses, the I-bus, K-bus, and the M-bus. Bit assignments for these buses are given in figure 2-26. The I-bus inputs, which represent disk timing and flag inputs, are fixed (hardwired) inputs. The M-bus and K-bus inputs are controlled by the currently active microinstruction. The M-bus inputs are wired to the processor bus, PBUS (00-15)-, so that the M-bus input data is determined by the processor bus source field, ROM13-15. The use which the CPE makes of the M-bus input, if any, is determined by the function code, ROM 01-07.

The K-bus inputs to the CPE array are supplied by multiplexers which are steered by the KC field of the active microinstruction. The multiplexer output may be all ones, all zeros, or the eight-bit immediate operand field of the active microinstruction. The K-bus inputs are active low, so selecting all ones with the KC field puts low levels on CPK00- through CPK15-. The K-bus inputs are used to mask one of the ALU inputs.

Each individual CPE has a carry input, and two look-ahead carry outputs. The CPE carry and shift logic contains an array of multiplexers and SN74S182 look-ahead carry generators. These carry generators supply the carries which are required from one two-bit CPE to the next higher significant CPE. The multiplexers are steered to handle the carries on a left byte, right byte, or full word basis.

The right-shift inputs and outputs within the bytes are hardwired from CPE to CPE. The source of the right shift input (LI) to the most significant stage of a byte, and the destination of the right-shift output of the byte are dependent upon the mode selected, left byte, right byte, or full word. The CPE carry and shift logic performs the shift steering between bytes for these modes.

The conditional branch/return test bit is incorporated in the CPE carry and shift logic. This test bit controls the execution of the conditional branches and returns specified by ROM 17-19, the BC field of the microinstruction. Some nonarithmetic CPE instructions use the carry output as an auxiliary bit to identify the results of a bit or word test. The carry output from the most significant active stage controls the TESTBITQ flip-flop, which in turn controls execution of conditional branches and returns. For example, an F-group 5, R-group III microfunction causes the contents of the AC or T register to be ANDed with the K-bus input, and ORed with the carry input. A carry output is generated if the result of the word-wise inclusive-OR is nonzero. The latched carry out, TESTBITQ, may be used to select one of two possible microprogram paths. The carry and shift operates with or without the microprocessor clock.

The microinstruction which sets up the test and conditional branch may stop the CPE clock (via ROM 00), so that the contents of the CPE registers are not modified. Omitting the CPE clock allows the bit or word testing to be nondestructive.

2.7.6 CPE ARRAY AND PROCESSOR BUS. Figure 2-27 is a detailed block diagram of the CPE array and the processor bus. This figure shows all the important signals associated with control of the processor bus and the left/right byte CPE arrays. The CPE carry and shift logic is not included in the diagram.

A. CPE K-BUS (MASK) INPUTS

WS FIELD (ROM08, 09)	KC FIELD (ROM10, 11)	CPK0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15
XX	00	ALL ONES * (SEE NOTE)	ALL ONES
	01	ALL ZEROS*	ALL ZEROS
FULL WORD WORD SHIFT OR RIGHT BYTE (ANY CODE EXCEPT 10)	10	EXTENDED SIGN BIT (ROM32)	$\overline{IM}$ (ROM32--39)
	11	EXTENDED SIGN BIT (ROM32)	$\overline{IM}$ (ROM32--39)
LEFT BYTE	10	$\overline{IM}$ (ROM32-39)	$\overline{IM}$ (ROM32--39)
10	11	$\overline{IM}$ (ROM32-39)	$\overline{IM}$ (ROM32--39)

SPECIAL FIELD DECODING ALSO ENABLED

B. CPE I-BUS FLAG INPUTS

0	1	2	3	4	5	6	7
SECTOR MARK	READY STATUS	$\overline{DISK\ START}$	READY DIRECT STATUS	$\overline{ADDRESS\ ACKNOWLEDGE}$	READ	DIAGNOSTIC FAULT	$\overline{TEST\ MODE}$

8	9	10	11	12	13	14	15
INDEX MARK	$\overline{STOP\ FLAG}$	$\overline{SPARE\ OUT1}$	CRC ERROR	$\overline{SPARE\ IN2}$	$\overline{SPARE\ IN1}$	$\overline{FIF00UT18}$	$\overline{FIF00UT19}$

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Figure 2-26. CPE Input Buses (Sheet 1 of 2)

C. PROCESSOR BUS (CPE M-BUS) INPUTS

BUS SOURCE FIELD ROM 13 14 15	SELECTED SOURCE	PBUS0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0 0 0	ZEROES	0*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0 0 1	CPE OUTPUT WORD (AC REGISTER)	CPE 0	1	2	3	4	5	6	7	CPE 8	9	10	11	12	13	14	15
0 1 0	HI-Z (FLOATING BUS)																
0 1 1	TILINE	TLDATA 0	1	2	3	4	5	6	7	TLDATA 8	9	10	11	12	13	14	15
1 0 0	DISK** DATA (INDIRECT MODE)	FIFO OUT 0	1	2	3	4	5	6	7	FIFO OUT 8	9	10	11	12	13	14	15
	DISK DATA (DIRECT MODE)	DIRECT REG 0	1	2	3	4	5	6	7	DIRECT REG 8	9	10	11	12	13	14	15
1 0 1	NOT DEFINED	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1 1 0	DISK STATUS	OFFLINE	NOTRDY	WP (WRITE PROTECT)	WCHK (WRITE CHECK)	SPAREING	SKIC (SEEK INCOMPLETE)	$SPARE_{IN-}$	$SPARE_{IN-}$	SWBIN (DRIVE B FIXED/ REMOVABLE)	SWAIN (DRIVE A FIXED/ REMOVABLE)	SPAREIN4	SECTORB 16	SECTORB 08	SECTORB 04	SECTORB 02	SECTORB 01
1 1 1	NOT DEFINED	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

NOTES.

*THE DATA INPUT AND OUTPUT BUSES FOR THE 3002 CPE ARE ACTIVE LOW. THUS, WHEN THE PBUS IS COMMANDED TO "ALL ZEROES", THE VOLTAGE LEVELS ON PBUS00- THROUGH PBUS15- ARE HIGH ($\geq$2.8 VOLTS).

**DISK READ DATA IS CONVERTED FROM SERIAL TO PARALLEL (PARDAT00 THROUGH PARDAT15) AND ROUTED TO THE DIRECT READ REGISTER AND FIRST IN-FIRST OUT (FIFO) BUFFER INPUTS. OUTPUT SELECTION IS CONTROLLED BY THE DIRECT/INDIRECT MODE F/F, WHICH IS SET OR RESET BY SPECIAL GROUP 01 OF THE MICROINSTRUCTION.

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Figure 2-26. CPE Input Buses (Sheet 2 of 2)

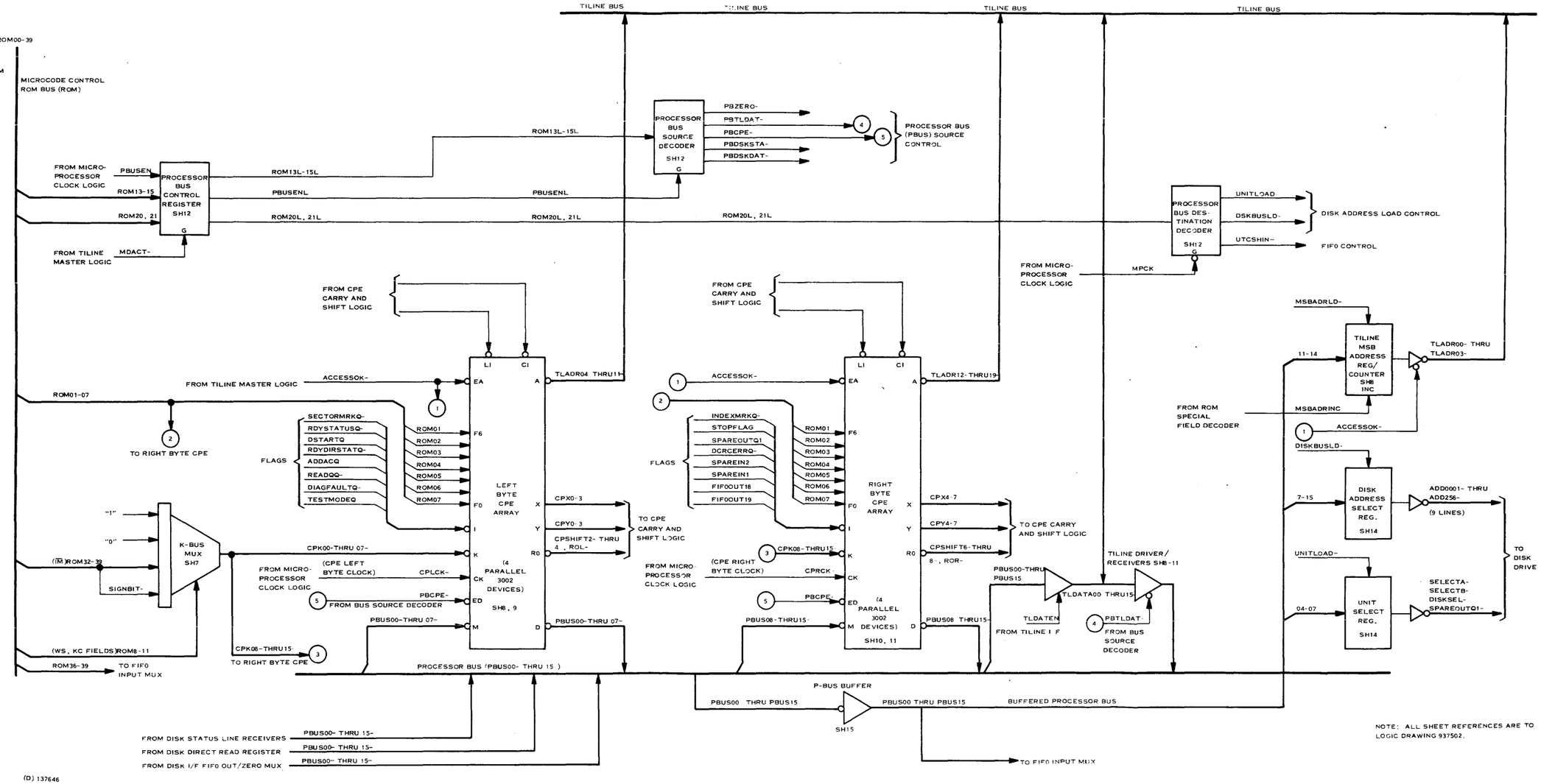


Figure 2-27. CPE Array and Processor Bus (PBUS) Block Diagram

The three-state processor bus is the main data transfer path within the DS10 disk controller. The processor bus, under microinstruction control, can transfer data from any bus source to any bus destination. The following are typical examples:

PBUS Source	Destination
CPE	TILINE output drivers Disk, via FIFO and parallel/serial shift register Test data shift register, via FIFO and parallel/serial shift register Disk (sector) address register Unit select register
TILINE line receivers	CPE M-bus inputs Disk, via FIFO and parallel/serial shift register
Disk Data (indirect)	TILINE output drivers, via FIFO CPE M-bus inputs, via FIFO
Disk Data (direct)	CPE M-bus inputs via direct read register TILINE output drivers via direct read register
Disk Status	CPE M-bus inputs
All Zeros	Any of the above

The bus source field of the microinstruction (ROM 13-15) determines which data is gated onto the processor bus. The bus source decoder ROM, which is described with microinstruction decoding, supplies the source control signals. These signals are:

Signal	Description
PBZERO-	Enable zeros (from FIFOOUT/Zero mux) onto P-bus.
PBCPE-	Enable CPE D-bus outputs.
PBTLDAT-	Enable TILINE line receivers.
PBDSKDAT-	Enable direct read register or FIFO output, depending on state of direct/indirect F/F.
PBDSKSTA-	Enable disk status line receivers.

The processor bus source decoder is strobed by PBUSENL, which is a delayed version of MPCK-. Figure 2-28 shows the timing relationship between microprocessor clock and PBUSENL. The address generator selects a new microinstruction on the rising (trailing) edge of MPCK-. There is an unsettled period as the ROM outputs change and the new microinstruction is decoded. The low PBUSENL signal delays P-bus source decoding until 100 nanoseconds after the rising edge of MPCK-. This delay allows conditions to stabilize before any data is gated to the P-bus, preventing noise bursts on the bus.

The ROM 13L-15L and PBUSENL signals are supplied to the decoder by the processor bus source control latch. This latch is transparent unless a TILINE master cycle is in progress. That is, the ROM 13L-15L and PBUSENL outputs follow the ROM 13-15 and PBUSEN or CLKT1-, fine line

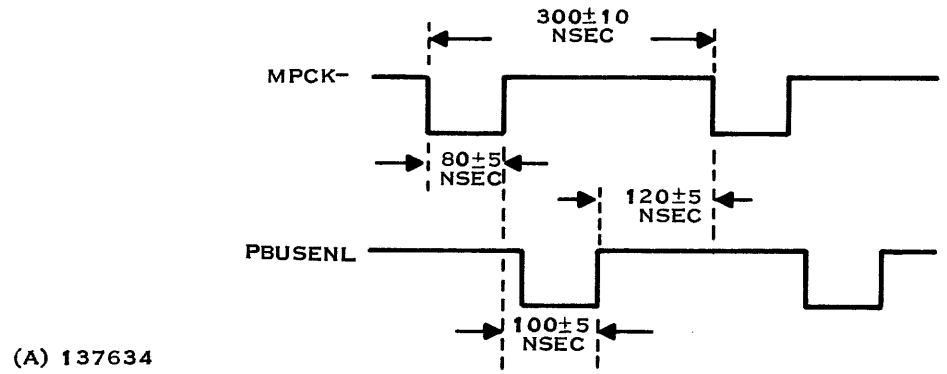


Figure 2-28. Microprocessor Clock and PBUS Enable

inputs with only a gate delay, unless the TILINE master device active (MDACT-) signal goes active (low). A low MDACT- signal latches up the states which existed on the negative MDACT- transition.

CPE output data may be routed to one of several destinations. Recall that the CPE output data (D-bus) is supplied by the AC register in the CPE. CPE data may be sent to the TILINE line drivers and on to the 990 memory during a slave read trap operation or a STORE REGISTERS command. CPE data may be sent to the disk, via the FIFO and serial/parallel register when updating header information, or as part of a TRACK FORMAT command. Data is transferred to a test data shift register as part of the controller self-diagnostic tests. The path to the test data shift register is identical to the write data path, except that the serial data is gated into a shift register rather than a disk I/F line driver.

CPE output data is loaded into the unit select and disk address select registers as part of any command which involves data transfer to or from the disk (READ DATA, READ UNFORMATTED, WRITE DATA, WRITE UNFORMATTED, or WRITE FORMAT).

CPE output bits 11-14 must be loaded into the TILINE MSB address register before any series of TILINE master cycles. The MSB address register supplies TILINE address bits 0 - 3, and the CPE A-bus outputs supply address bits 4 - 19. The CPEs keep track of the number of words transferred and increment the MSB address register each time a 64K word boundary is passed.

The TILINE line receivers supply a data word to the CPE M-bus inputs on each TILINE slave write cycle initiated by the 990 computer. The eight DS10 control words, W0-W7, are loaded into the CPE scatchpad registers by a sequence of eight slave write cycles. Also, during a disk write operation, the DS10 controller, acting as a TILINE master, reads data words from the 990 memory to the disk via the TILINE, the FIFO buffer, and the serial/parallel converter.

Data read from the disk is converted from serial to parallel form and routed to the inputs of the read direct register and the first in, first out (FIFO) buffer. The direct register is selected to supply data to the CPE in the case of checking header words. However, when a buffer from disk to 990 memory is required, the FIFO is selected in order to allow for data rate differences between the disk and the TILINE.

Disk status words are routed from the status line receivers to the CPE M-bus inputs. The sector addresses and other disk status information in these words must be checked repeatedly during any operation which involves data transfer to or from the disk.

2.8 CPE CARRY AND SHIFT LOGIC

The functions of the CPE carry and shift logic include:

- Carry generation for arithmetic operations in left byte, right byte, and full-word groups
- Test bit generation for the conditional branching microinstructions
- Conventional right-shifting of 16-bit words

Each 3002 CPE processes a two-bit slice of data on the I, M, and/or K-bus inputs. Each device has the necessary internal interconnections for shift and carries within the device. In order to process eight-bit bytes or 16-bit words, carry and right shift interconnections are made between the devices. Each device must be connected to accept a carry input, send a carry output, right shift a bit and accept a right-shifted bit from another stage. The CPEs are grouped to operate in right byte, left byte, and full-word modes.

Figure 2-29 shows the CPE carry and shift circuitry. The CPE data input, output, and function control signals are omitted for clarity. The CPE signals involved in carry and shift operations are:

CI	Carry input
CO	Ripple carry output (not used)
X,Y	Carry propagation and operation outputs for high-speed look-ahead carry
RO	Right shift output (three-state, enabled only during right shift operations)
LI	Right shift input from the adjacent (more significant) state. Also called "left input".

In addition to the ordinary arithmetic functions, the carry outputs are used during comparison operations to indicate the result of a comparison. For example, the TZR instruction (F-group 5, R-group 1, K=11) will test the specified register for zero contents, and force a carry output if the register is nonzero. The carry is used to set a test bit flip-flop, which steers the execution of conditional branch instructions. This is the way in which execution is steered through alternate paths in the microcode program.

2.8.1 THE TEST BIT F/F AND CONDITIONAL BRANCHING. The branch control (BC) field of a microinstruction specifies how the controller is to select the next microinstruction. There are four conditional branch control codes:

ROM 17,	18,	19	Description
0	1	0	Conditional branch (if TESTBITQ true) to next ROM address (NRA) else RA + 1
0	1	1	Conditional branch (if TESTBITQ false) to next ROM address (NRA) else RA + 1
1	0	1	Conditional return (if TESTBITQ true) to address stored in stack of address generator else NRA
1	1	0	Conditional return (if TESTBITQ false) to address stored in stack of address generator else NRA

These conditional branches/returns all use the output of the test bit flip-flop, TESTBITQ, as the test condition.

The test bit flip-flop monitors a number of conditions, depending on the CPE operation commanded by the microinstruction. For any CPE operation other than shift, the test bit F/F monitors the carry output of the most significant CPE state. For shift operations, the test bit F/F monitors the right shift output of the least significant CPE stage. The carry and shift multiplexers select the carries/shifts from the left or right byte, as specified by the microinstruction WS field. Table 2-8 gives a complete listing of test bit F/F inputs.

Table 2-8. Test Bit Flip-Flop Inputs

CPE Functions	Byte/Word Selection	TESTBIT-Source
Shifts:		
	Left byte	Right shift output of left byte LSB (ROL-)
	Right byte	Right shift output of right byte LSB (ROR-)
	Word shift	Right shift output of word LSB (ROR-) from right byte
Arithmetic Operations or Bit Testing:		
	Left byte	Carry output of left byte MSB
	Right byte	Carry output of right byte MSB (CIL-)
	Word	Carry output of MSB (left byte)

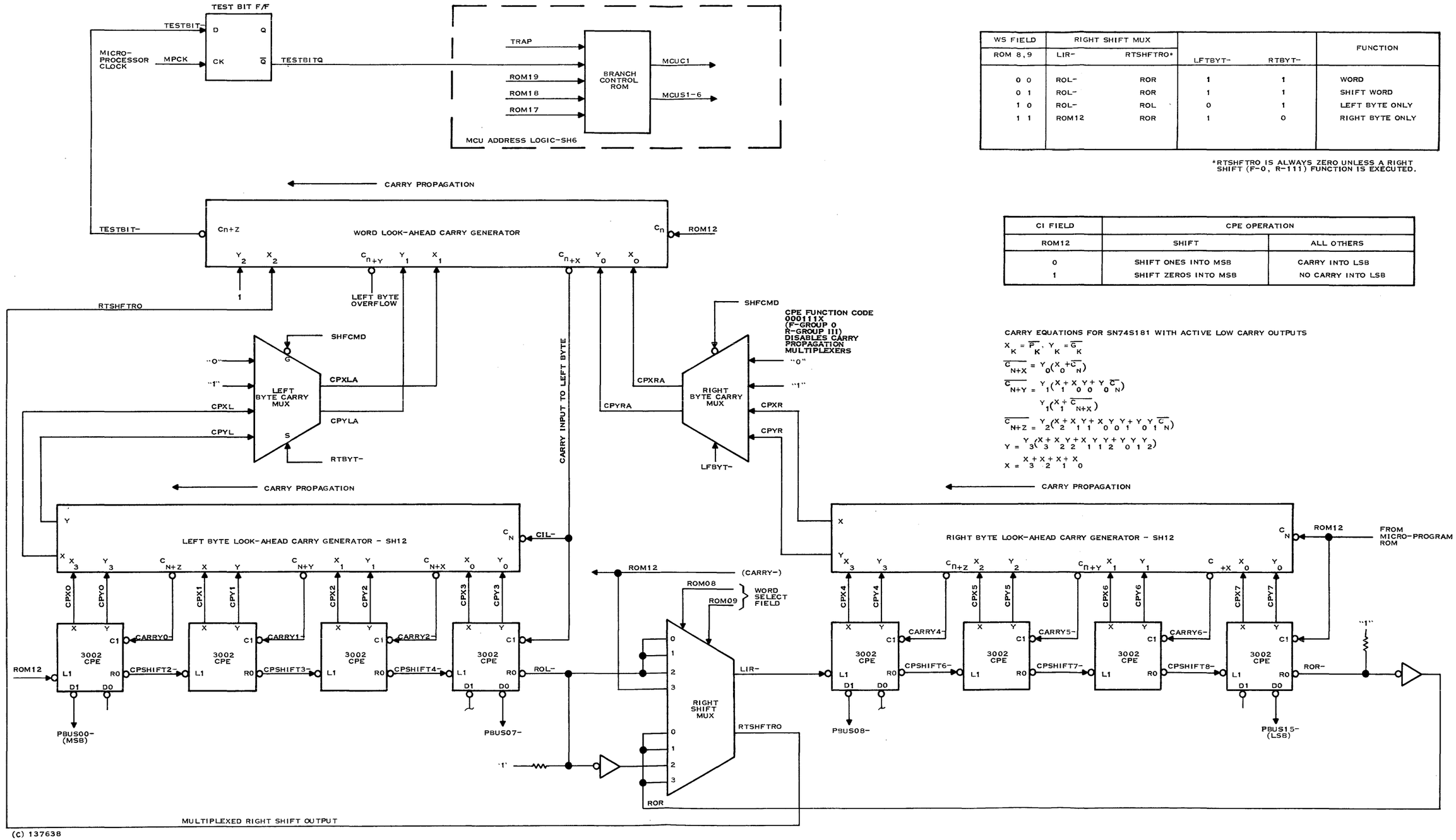
The output of the test bit flip-flop, TESTBITQ, the TRAP signal, and the branch control field of the microinstruction, ROM 17-19, supply the address input to the branch control ROM. This ROM supplies control signals to the address generator based on the BC field and the test condition, or on the existence of a trap.

The 3002 CPE has a number of nonarithmetic instructions which use the carry lines to indicate the results of a data test. Refer to the CPE instruction set for a complete list. The ANM instruction, for example, logically ANDs the M-bus input of the CPE with the accumulator contents. A carry is generated if the result is nonzero, and the result is placed in the accumulator or T-register. A carry input from the adjacent (less significant) stage will also cause a carry out. Each CPE tests a two-bit slice, but the carry circuitry makes the carry output of the MSB valid for the whole byte or word.

For right byte operations with an ANM instruction (F-group 4, R-group II, K-bus = 11), a carry output from the right byte indicates that the eight-bit result is nonzero.

The zero or nonzero result of the data test is often much more important than the eight or 16-bit value. By omitting the CPE clock pulse, it is possible to perform the data test without storing the result. The ALU, carry, carry look-ahead and right shift logic of the CPEs is not controlled by the CPE clock. The CPE registers do not accept the result of the operation until the negative-going edge of the CPE clock pulse.

The CPE conditional clock bit (ROM00) allows the microinstruction to inhibit the CPE clock for nondestructive testing. This may be done in conjunction with one of the conditional branching microinstructions. The CPE performs the operation specified in ROM 01 - 07, and the test bit flip-



WS FIELD	RIGHT SHIFT MUX				FUNCTION
ROM 8,9	LIR-	RTSHFTRO*	LFTBYT-	RTBYT-	
0 0	ROL-	ROR	1	1	WORD
0 1	ROL-	ROR	1	1	SHIFT WORD
1 0	ROL-	ROL	0	1	LEFT BYTE ONLY
1 1	ROM12	ROR	1	0	RIGHT BYTE ONLY

*RTSHFTRO IS ALWAYS ZERO UNLESS A RIGHT SHIFT (F=0, R=111) FUNCTION IS EXECUTED.

CI FIELD	CPE OPERATION	
ROM12	SHIFT	ALL OTHERS
0	SHIFT ONES INTO MSB	CARRY INTO LSB
1	SHIFT ZEROS INTO MSB	NO CARRY INTO LSB

CARRY EQUATIONS FOR SN74S181 WITH ACTIVE LOW CARRY OUTPUTS

$X_K = \overline{P_K}$; $Y_K = \overline{G_K}$

$\overline{C_{N+X}} = Y_0(X_0 + \overline{C_N})$

$\overline{C_{N+Y}} = Y_1(X_1 + X_0 Y_0 + Y_0 \overline{C_N})$

$Y_1(X_1 + \overline{C_{N+X}})$

$\overline{C_{N+Z}} = Y_2(X_2 + X_1 Y_1 + X_0 Y_0 Y_1 + Y_0 Y_1 \overline{C_N})$

$Y = Y_3(X_3 + X_2 Y_2 + X_1 Y_1 Y_2 + Y_0 Y_1 Y_2)$

$X = X_3 + X_2 + X_1 + X_0$

Figure 2-29. CPE Carry and Shift Logic

flop monitors the test result (carry output). The conditional branch is performed, based on the test results, and the next microinstruction is fetched. The eight or 16-bit result is not stored.

The CPE right shift outputs are supplied by three-state drivers which are enabled when a right shift function (F-group 0, R-group III) is specified. The test bit flip-flop monitors the right shift output from the least significant state of the left or right byte. This allows the LSB to be used to control conditional branching. If the CPE conditional clock bit (ROM 00) is set, the register contents do not actually shift, and the test is nondestructive.

2.8.2 SN74S182 LOOK-AHEAD CARRY GENERATORS. Look-ahead carry generation is based on the fact that it is possible to use combinational logic on the data inputs to an adder circuit to determine in advance if that stage will generate a carry or allow a carry from a lower stage to propagate through as a carry. The carry propagate and generate function outputs from individual stages are combined to determine the anticipated carries for all the stages and to supply those carries. As word lengths become longer, carry look-ahead becomes much faster than ripple carry.

The look-ahead scheme does require that the adder contain the additional logic necessary to develop the carry generate and propagate functions. Carry look-ahead can be used to combine multibit adder circuits which have internal ripple carry.

The SN74S182 is a four-stage look-ahead carry generator which provides rapid carry generation for four binary stages or groups of stages. The most significant stage of the SN74S182 develops carry propagate and generate outputs which may be connected to the inputs of another SN74S182. These devices may be cascaded in this manner to perform full look-ahead across n binary stages.

The SN74S182 can be used in either active high or active low carry propagation schemes. The 3002 CPE generates active high look-ahead outputs, X and Y, and requires active low carry inputs. The carry equations in this form are:

$$C_{n+x} = Y_o(X_o + C_n\text{-})$$

$$C_{n+y}\text{-} = Y_1(X_1 + X_oY_o + Y_oC_n\text{-})$$

$$= Y_1(X_1 + C_{n+x}\text{-})$$

$$C_{n+z}\text{-} = Y_2(X_2 + X_1Y_1 + X_oY_oY_1 + Y_oY_1C_n\text{-})$$

$$= Y_2(X_2 + C_{n+y}\text{-})$$

The group carry look-ahead outputs from the SN74S182 are:

$$X = X_3 + X_2 + X_1 + X_0$$

$$Y = Y_3(X_3 + X_2Y_2 + X_1Y_1Y_2 + Y_0Y_1Y_2)$$

Note that the group carry look-ahead outputs, X and Y, are developed only from the individual X and Y inputs, and do not incorporate the ripple carry input, C_n-. When 'S182 generators are cascaded, the ripple carry input must be routed to all the carry generators.

As shown in figure 2-29, a single SN74S182 device provides carries for the left byte CPEs, and another one serves the right byte CPEs. An additional 'S182 is used to link the left and right bytes during full word operations. This unit is also used in the conditional branching operations.

2.8.3 CARRY AND SHIFT LOGIC CONTROL. The carry and shift logic is controlled by the processor control microinstructions, either directly or through decoders. The word select field, ROM 08, 09 determines whether the CPEs operate in word, word shift, left byte, or right byte modes. Refer to the WS field decoding table incorporated in figure 2-24.

ROM 08 and 09 are used to steer the right shift multiplexer. These two bits also control the left byte (LFBYTE-) and right byte (RTBYTE-) signals as shown. The LFBYTE- signal steers the right byte carry multiplexer, and the RTBYTE- signal steers the left byte carry multiplexer. The LFBYTE- signal, when low, disables the CPE right byte clock signal, CPRCK-. The RTBYTE- signal, when low, disables the CPE left byte clock, CPLCK-.

ROM 12 controls the carry input, CI, to the least significant active CPE. For right byte or full word operations, this carry is directly wired to the least significant bit of the right byte. For left byte operations, the carry is routed through the word look-ahead carry generator to the LSB of the left byte. The CPE interprets ROM 12 as follows:

ROM 12

0 = carry or one fill for shift operations
1 = no carry or zero fill for shift operations

The right shift output of a CPE, RO-, is a 3-state output which is enabled only when the CPE function code specifies a right shift operation. The CPE performs right shifts for F-group 0, R-group III function codes. The processor control bits which supply this function code are:

ROM 01	02	03	04	05	06	07	
	0	0	1	1	1	X	X = 0, shift T-register X = 1, shift AC (accumulator) register

These bits are also decoded external to the CPEs to produce the shift command (SHFCMD) signal. The SHFCMD signal is used to disable the left and right byte carry multiplexers during shift operations.

2.8.4 RIGHT BYTE CARRY OPERATIONS. A carry may be generated by a CPE as the result of a two's complement arithmetic operation or a bit test operation. Assume that the processor control microinstruction (ROM 00-39) specifies an arithmetic operation on the right byte. The right shift interconnections and the entire left byte may be ignored for this description.

ROM 12 is the carry input to the least significant stage of the right byte and the 'S182 carry generator. The 'S182 generates the interstage carry signals, CARRY6-, CARRY5-, and CARRY4-, as required.

Assume that there is a carry overflow from the most significant stage of the right byte. The right byte look-ahead carry outputs, CPXR and CPYR, go through the right byte carry multiplexer as CPXRA and CPYRA. These signals are the X_0, Y_0 inputs to the word carry look-ahead generator. The carry bit, ROM 12, from the processor control microinstruction is wired to the C_n- input. The output of the first stage of the word look-ahead carry generator is:

CIL- = CPYRA (CPXRA + ROM12-)

CIL- is not used by the left byte for this example but it is used in carry propagation within the 'S182.

The left byte multiplexer is steered by the RTBYTE signal to select the hardwired 0 and 1 levels for CPYLA and CPXLA, respectively. These levels are selected to allow a carry from the first 'S182 stage (CIL-) to continue through the 'S182.

The output of the second stage of the 'S182, C_{n+y}-, is not used external to the carry generator. The operation for this term is:

$$C_{n+y}\text{-} = \text{CPYLA (CPXLA + CIL-)}$$

For this example, C_{n+y}- = CIL-, and the carry, if any, goes to the third stage of the carry generator.

The external inputs to the third stage of the 'S182 are a hardwired logic 1 and RTSHFTRO. RTSHFTRO is the right shift output of the right byte, as selected by the right shift multiplexer. For a right byte (only) operation, ROM 8, 9 = 11, which selects ROR, the right shift output of the right byte. In the absence of a shift command, ROR- is pulled high and ROR is a logic 0.

The general equation for the TESTBIT- signal is:

$$\text{TESTBIT-} = 1\ (\text{RTSHFTRO} + C_{n+y}\text{-})$$

For this example, the equation reduces to:

$$\begin{aligned}\text{TESTBIT-} = \text{CIL-} &= \text{CPYRA (CPXRA + ROM12-)}\\ &= \text{CPYR (CPXR + ROM12-)}\end{aligned}$$

The TESTBIT- output of the 'S182 is clocked into the test bit flip-flop on the positive-going edge of the microprocessor clock signal, MPCK. The TESTBITQ output of the flip-flop goes to the branch control ROM. If a conditional branch was specified as part of the microinstruction (ROM 17, 18, 19), TESTBITQ determines whether the branch occurs.

2.8.5 LEFT BYTE CARRY OPERATIONS. Assume that the processor control microinstruction specifies a left byte only operation (ROM 8, 9 = 10), and CPE operation is not a right shift. The right shift interconnections and the entire right byte may be ignored for this description.

The ripple carry input to the left byte, CIL-, is ROM12 for the left byte operations. This allows the microinstruction to command a carry into the LSB of the active byte. ROM 12 is gated to CIL- through the first (least significant) stage of the word look-ahead carry generator.

The outputs of the right byte carry multiplexer, CPXRA and CPYRA are steered to 0 and 1, respectively, by the LFBYTE- signal. This combination gates the carry in bit, ROM12-, through the 'S182 as follows:

$$\begin{aligned}C_{n+z}\text{-} = \text{CIL-} &= \text{CPYRA (CPXRA + ROM12-)}\\ &= \text{1 (0 + ROM12-)}\\ &= \text{ROM12-}\end{aligned}$$

The left byte look-ahead carry generator uses the ROM12 ripple carry input and the X and Y outputs of the individual CPEs to produce the required left byte carries.

Assume that there is a carry overflow from the most significant bit of the left byte. The left-byte look-ahead carry outputs, CPXL and CPYL, go through the left byte carry multiplexer as CPXLA and CPYLA, and are wired to the X_1 Y_1 inputs of the 'S182.

The output of this stage of the 'S182 is:

$$\begin{aligned}C_{n+y}\text{-} &= Y_1(X_1 + C_{n+x}\text{-})\\ &= \text{CPYLA(CPXLA + ROM12-)}\end{aligned}$$

C_{n+y}- is not used external to the 'S182, but it is an input term to the next stage of the look-ahead carry generator.

The external inputs to the third stage of the 'S182 are a hardwired logic 1 and RTSHFTRO. RTSHFTRO is the right shift output of the left byte, as supplied by the right shift multiplexer. It is 1 for this example. This combination sets the C_{n+z}- output equal to the C_{n+y}- output.

The TESTBIT- output of the 'S182 is determined as follows:

$$\begin{aligned} \text{TESTBIT-} &= 1\ (\text{RTSHFTRO} + C_{n+y}\text{-}) \\ &= C_{n+y}\text{-} \\ &= \text{CPYLA}\ (\text{CPXLA} + \text{ROM12-}) \\ &= \text{CPYL}\ (\text{CPXL} + \text{ROM12-}) \end{aligned}$$

The TESTBIT- signal is loaded into the test bit flip-flop and used to control conditional branching.

2.8.6 FULL 16-BIT WORD CARRY OPERATIONS. Full 16-bit arithmetic requires the ability to propagate carries from the right byte into the left byte. For a full word operation, ROM 8, 9 = 0, 0, which makes LFTBYT- = RTBYTE- = 1.

The ripple carry input to the left byte is controlled by the carry bit of microinstruction. The right byte look-ahead carry generator (SN74S182) uses ROM 12 and the X and Y outputs of the CPE stages to develop CARRY6-, CARRY5-, and CARRY4- as required. The look-ahead outputs of the right byte carry generator, CPXR and CPYR, are cascaded (via the right byte carry multiplexer) to the X_0, Y_0 inputs of the word look-ahead carry generator. ROM12 is also wired to the ripple carry input of the word look-ahead carry generator. This is not a duplication, because the ripple carry input is not incorporated in the logic equations for CPXR and CPYR.

The carry input to the left byte, CIL- is:

$$\begin{aligned} \text{CIL-} &= Y_0(X_0 + C_n\text{-}) \\ &= \text{CPYR}(\text{CPXR} + \text{ROM12-}) \end{aligned}$$

The left byte carry generator uses the CIL- input and the X, Y outputs of the CPE to develop CARRY2-, CARRY1-, and CARRY0- inputs to the CPEs as required.

The look-ahead outputs of the left byte carry generator, CPXL and CPYL are cascaded to the X1, Y1 inputs of the word look-ahead carry generator. C_{n+y}-, which is not wired externally to the 'S182, is given by:

$$\begin{aligned} C_{n+y}\text{-} &= \text{CPYLA}\ (\text{CPXLA} + \text{CIL-}) \\ &= \text{CPYL}\ (\text{CPXL} + \text{CIL-}) \end{aligned}$$

The X_2 and Y_2 inputs to the next stage are 0 and 1 respectively, which has as the effect of transferring the C_{n+y}- output, unmodified, to the C_{n+z}- output.

The equations are:

$$\begin{aligned} \text{TESTBIT-} &= Y_2(X_2 + C_{n+y}\text{-}) \\ &= 1\ (\text{RTSHFTRO} + C_{n+y}\text{-}) \\ &= C_{n+y}\text{-} \\ &= \text{CPYL}\ (\text{CPXL} + \text{CIL-}) \end{aligned}$$

RTSHFTRO is always 0 unless a CPE right shift function code (F-group 0, R-group III) is executed.

The TESTBIT- signal is loaded into the test bit flip-flop on the next positive-going transition of microprocessor clock, MPCK. The TESTBITQ signal from the flip-flop goes to the branch control ROM, where it may be used to control conditional branching.

2.8.7 RIGHT SHIFT OPERATIONS — GENERAL. The 3002 CPE performs a one-bit right shift in response to an F-group 0, R-group III function code. This is a simple right shift (SRA) if the K-bus contents are all zeros. The contents of the accumulator (AC) or T-register are shifted one place to the right. The previous low-order bit is placed on the right shift output, R0-, and the high order bit is filled from the right shift input, LI-. Note that an individual right shift microinstruction is required for each desired one-bit shift. If the K-bus contents are nonzero, the right shift includes a combination of masking and right-shifting. The equations for this case are included in the detailed 3002 CPE description.

The right shift output, RO-, of the 3002 is supplied by a three-stage driver which is only enabled when the CPE executes a right shift operation. Within the left or right byte, the RO- outputs are wired directly to the adjacent LI- inputs. Multiplexers and control circuitry configure the CPEs to perform left byte shift, right byte shift, full word shift, or CRC shift.

The test bit flip-flop may be used to monitor the right shift output of the least significant stage and to control conditional branching.

2.8.7.1 Full Word Right Shift Operations. Full word right shift operations are selected when ROM01 - 07 = 000111X (F-group 0, R-group III) and ROM 8, 9 = 01. The function code commands the CPE operation and the WS field steers the multiplexers. The carries from the CPEs are irrelevant during shift operations, and the left and right byte carry multiplexers are disabled (all zeros out) by the SHFCMD signal.

A word shift to the right creates a vacancy at the MSB position. The ROM12 signal from the microinstruction selects zero-fill or one-fill, as follows:

ROM12	
0	one-fill MSB
1	zero-fill MSB

ROM12 is directly wired to the LI- input of the left byte. Bits are right-shifted between two-bit CPEs by CPSHIFT2-, CPSHIFT3, and CPSHIFT4-. ROL- is the right shift output of the left byte. It is pulled high during any operation except left byte or full word right shift. For a full word shift, ROM8,9 steer ROL- through the right shift multiplexer. The multiplexer output, LIR-, is the left input to the right byte.

Bits are right-shifted through the right byte on the CPSHIFT6-, CPSHIFT7-, and CPSHIFT8- lines. ROR- is the right shift output of the right byte. It is pulled high during any operation except right byte, CRC, or full word shift. ROR- is inverted and routed through the right shift multiplexer as RTSHFTRO.

RTSHFTRO is the right shift output of the least significant right-shifted stage. It is routed to the X_2 input of the word look-ahead carry generator, and the Y_2 input is hardwired to 1. The X_0, Y_0, X_1 and Y_1 inputs to the 'S182 are all zeros, because SHFCMD disables the left and right byte carry multiplexers. Under these conditions, TESTBIT- is simply RTSHFTRO in inverted form:

TESTBIT- = RTSHFTRO

For the case of full word or right byte shifts, TESTBIT- = ROR-. Notice that the ROM12 input to the 'S182 has no effect on TESTBIT- for right shift operations.

2.8.7.2 Left-Byte Right Shift Operations. An F-group 0, R-group III function code with ROM8,9 = 10, commands a right shift of the left byte (only). ROM12 supplies the right shift input to the MSB position, as described with full word shifts. The right shift output of the left byte, ROL-, is inverted and steered through the right shift multiplexer as RTSHFTRO, right shift output of the LSB. The LIR- output of the right shift multiplexer has no effect for left byte shifts.

RTSHFTRO is routed to the word look-ahead carry generator to develop the TESTBIT- signal, as described with full word shifts:

TESTBIT- = RTSHIFTRO
= ROL- (left byte shifts)

The test bit flip-flop stores the TESTBIT- signal and may be used to control conditional branching.

2.8.7.3 Right Byte Right Shift Operations. The word select field ROM8,9 selects the right byte with an 11 code. The right shift multiplexer selects ROM12 as the left input to the right byte, LIR-. This allows the microinstruction to select zero-fill (ROM12 = 1) or one-fill into the MSB position.

The right shift output of the right byte, ROR-, is inverted and selected by the right shift multiplexer as RTSHIFTRO.

The TESTBIT- output of the word look ahead carry generator is:

TESTBIT- = RTSHIFTRO
= ROR- (right byte or full word shifts)

2.9 MICROPROGRAM ADDRESS CONTROL

The branch control (BC) and next ROM address (NRA) fields of the current microinstruction determine the address of the next microinstruction to be executed. The branch control field, ROM 17-19, provides conditional and unconditional address control functions. All the conditional address control functions use the test bit flip-flop output, TESTBITQ, as the test condition. The test bit flip-flop is described with the CPE carry and shift logic.

The branch control functions are:

ROM 17	18	19	Function
0	0	0	Unconditional increment to current address +1
0	0	1	Unconditional branch to next ROM address (NRA)
0	1	0	Conditional branch (if test bit true) to NRA, else RA +1
0	1	1	Conditional branch (if test bit false) to NRA, else RA +1
1	0	0	Unconditional branch and link to NRA (RA +1 to stack)
1	0	1	Conditional return (if test bit true) to address stored in stack of address generator. Otherwise, branch to NRA.
1	1	0	Conditional return (if test bit false) to stack address. Otherwise, branch to NRA.
1	1	1	Unconditional return to stack address.

The branch control functions, test bit, and trap functions are decoded by a branch control ROM, as shown in the simplified block diagram, figure 2-30. The function control and carry outputs of the branch control ROM control the operations of the address generator. The NRA field of the

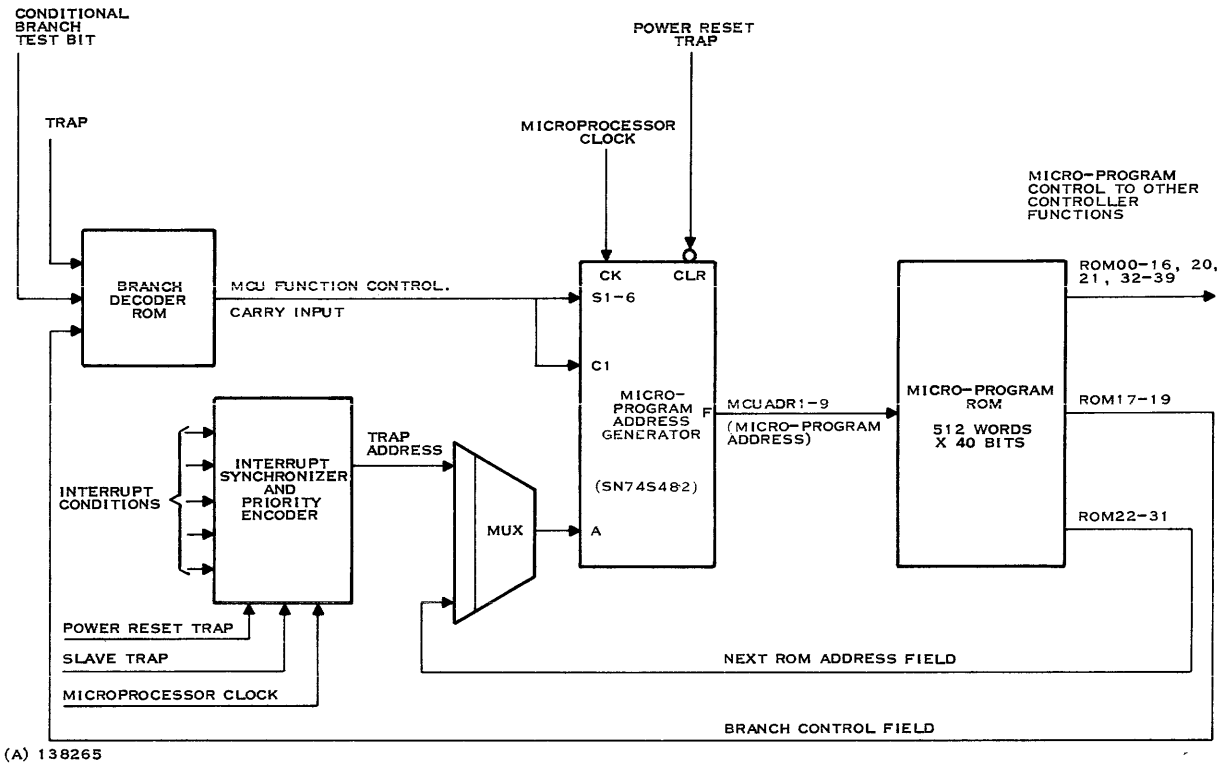


Figure 2-30. Microprogram Address Control — Simplified Block Diagram

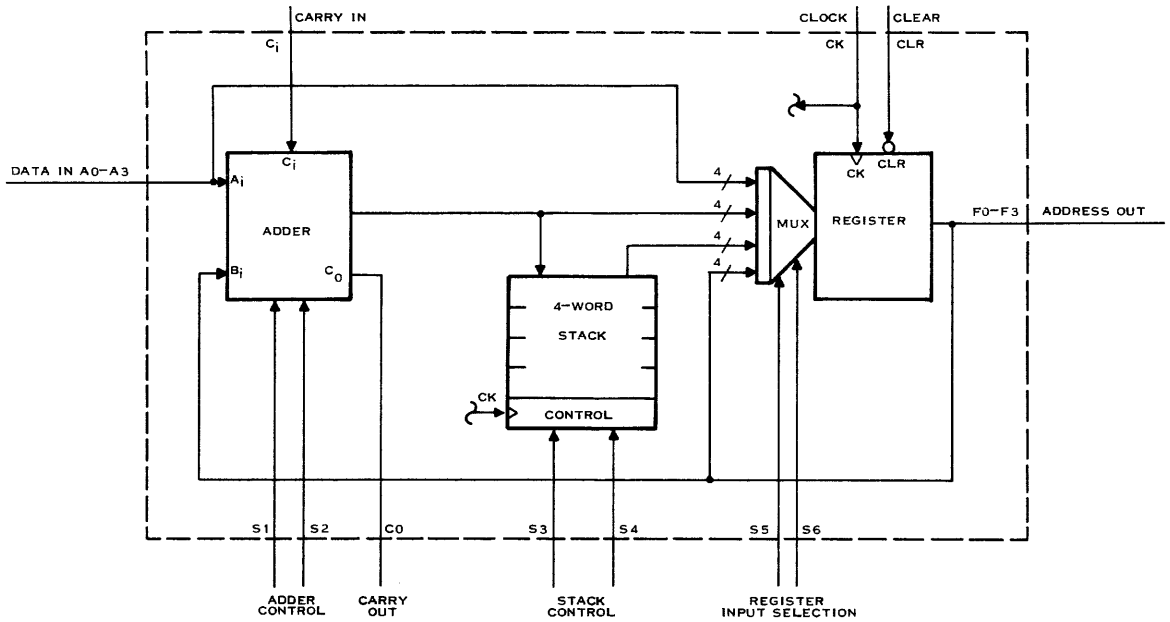
microinstruction supplies a nine-bit address input in the absence of a trap or interrupt. The output of the address generator, MCUADR1-9, fetches the next microinstruction from microprogram memory.

2.9.1 ADDRESS GENERATOR. The address generator is based on the SN74S482 expandable control element. Each SN74S482 controls a four-bit slice of the address. An internal full adder, four-word push/pop stack, output register multiplexer and clocked output register provide straightforward and versatile address control.

Figure 2-31 is a functional block diagram of a single SN74S482 device. The address output register is clocked on the positive-going edge of the clock signal (MPCK-). The output register source, controlled by S5 and S6, may be the current address, the stack output, the adder output, or the direct data-in address.

The push/pop stack can be used for nesting up to four levels of program return addresses. The stack control functions, controlled by S3 and S4, are load, push, pop, and hold. In the load mode, the adder output is loaded into the top of the stack, replacing the previous stack output. In the push mode, all addresses are moved down one location, and the adder output is loaded on top of the stack. The bottom word is lost. In the pop mode, the words in the stack are moved up one location on each clock pulse. The top word is lost. The bottom word remains, and is duplicated in the adjacent stage. After three pop commands, the bottom word would be duplicated in all four stack locations. The hold function causes no change in stack contents.

The adder function is controlled by S1 and S2. The adder output may be equal to carry in, carry in + current output, carry in + direct data in, or carry in + current output + direct data in.



(A)135711

Figure 2-31. SN74S482 Functional Block Diagram

Tables 2-9, 2-10 and 2-11 summarize the function control inputs S1-S6 of the address generator. The three control groupings are independent, so that multiple address control functions may be performed on the next clock transition. For example, it is possible to select the branch address and store the incremented current address in the stack on the same clock pulse. This branch and save operation requires carry in = 1, S1, S2 = 10, S3, S4 = 11, and S5, S6 = 00. Up to four branches may be nested, with the return addresses stored in the stack.

Table 2-9. Address Generator Adder Control

MCU	S1,	S2	Adder Output	Comment
	0	0	Bi + Ai + Cin	Current address + next ROM address field + carry
	0	1	Ai + Cin	Next ROM address field + carry
	1	0	Bi + Cin	Current address + carry
	1	1	Cin	MCU carry

Table 2-10. Address Generator Stack Control

MCU	S3,	S4	Stack Function	Comment
	0	0	Hold	No stack change
	0	1	Load	Store word at top of stack, writing over previous top word
	1	0	Pop	Move stack up one position, losing top word
	1	1	Push	Store word at top of stack, move stack down one position, losing bottom word

Table 2-11. Address Generator Output Control

MCU	S5,	S6	Output Register Source	Comment
	0	0	Data in	NRA field
	0	1	Adder output	
	1	0	Stack output	
	1	1	Output register	Current address
	X	X	Clear = 0	Forces register outputs to all zeros

2.9.2 BRANCH DECODER ROM. Table 2-12 is a listing of the contents of the SN74S288 branch decoder ROM. In this application, the ROM is being used as a decoder to produce seven address generator control functions. Four ROM words are dedicated to each of the eight basic branch commands. The condition of the test bit and trap inputs determine which specific word is selected.

In the BRANCH CONDITIONAL IF TRUE command, refer to the address generator control tables to interpret the branch decoder ROM words. If there is no trap, and test bit is false, the carry is high, the adder output is current address + 1, and the adder is selected for output. The address generator selects the next sequential microinstruction.

If the test bit is high, and no trap occurs, the adder selects the NRA field, no stack functions are performed, and the output register selects the adder output. Thus, the test bit causes a straightforward branch.

Careful examination of the branch decoder ROM listing shows that the ROM output is identical for any trap, regardless of the test bit or the branch control field of the current microinstruction.

If a trap occurs, regardless of the test bit, the adder passes the current address, which is pushed into the stack. The output register selects the direct data input, in which the trap address has replaced the NRA field of the microinstruction. Thus, the trap routine is performed before the current instruction. At the end of the trap routine, the program gets back to the trap point by accessing the stack.

2.9.3 ADDRESS CONTROL LOGIC. Figure 2-32 is a simplified logic drawing of the address control logic. This paragraph and subsequent paragraphs describe the address control operations involved in normal microinstruction accessing, TILINE slave trap processing, microcode interrupt processing, power and I/O reset trap processing.

Table 2-12. Branch Control ROM Listing

BC-Field ROM 17, 18, 19	Test Bit	Trap	Outputs MCU S1	MCU S2	MCU S3	MCU S4	MCU S5	MCU S6	MCU CI1	Unused	Comment
	L	L	H	L	L	L	L	H	H	X	
LLL	L	H	H	L	H	H	L	L	L	X	Increment
(000)	H	L	H	L	L	L	L	H	H	X	Unconditional
	H	H	H	L	H	H	L	L	L	X	
	L	L	L	L	L	L	L	L	L	X	
LLH	L	H	H	L	H	H	L	L	L	X	Branch
(001)	H	L	L	L	L	L	L	L	L	X	Unconditional
	H	H	H	L	H	H	L	L	L	X	
	L	L	H	L	L	L	L	H	H	X	
LHL	L	H	H	L	H	H	L	L	L	X	Branch
(010)	H	L	L	H	L	L	L	H	L	X	Conditional If
	H	H	H	L	H	H	L	L	L	X	Test Bit True
	L	L	L	H	L	L	L	H	L	X	
LHH	L	H	H	L	H	H	L	L	L	X	Branch
(011)	H	L	H	L	L	L	L	H	H	X	Conditional If
	H	H	H	L	H	H	L	L	L	X	Test Bit False
	L	L	H	L	H	H	L	L	H	X	
HLL	L	H	H	L	H	H	L	L	L	X	Branch and Link
(100)	H	L	H	L	H	H	L	L	H	X	Unconditional
	H	H	H	L	H	H	L	L	L	X	
	L	L	L	L	L	L	L	L	L	X	
HLH	L	H	H	L	H	H	L	L	L	X	Conditional
(101)	H	L	L	L	H	L	H	L	L	X	Return If
	H	H	H	L	H	H	L	L	L	X	Test Bit True
	L	L	L	L	H	L	H	L	L	X	
HHL	L	H	H	L	H	H	L	L	L	X	Conditional
(110)	H	L	L	L	L	L	L	L	L	X	Return If
	H	H	H	L	H	H	L	L	L	X	Test Bit False
	L	L	L	L	H	L	H	L	L	X	
HHH	L	H	H	L	H	H	L	L	L	X	Unconditional
(111)	H	L	L	L	H	L	H	L	L	X	Return
	H	H	H	L	H	H	L	L	L	X	
	L	L	L	L	H	L	H	L	L	X	
HHH	L	H	H	L	H	H	L	L	L	X	Unconditional
(111)	H	L	L	L	H	L	H	L	L	X	Return
	H	H	H	L	H	H	L	L	L	X	

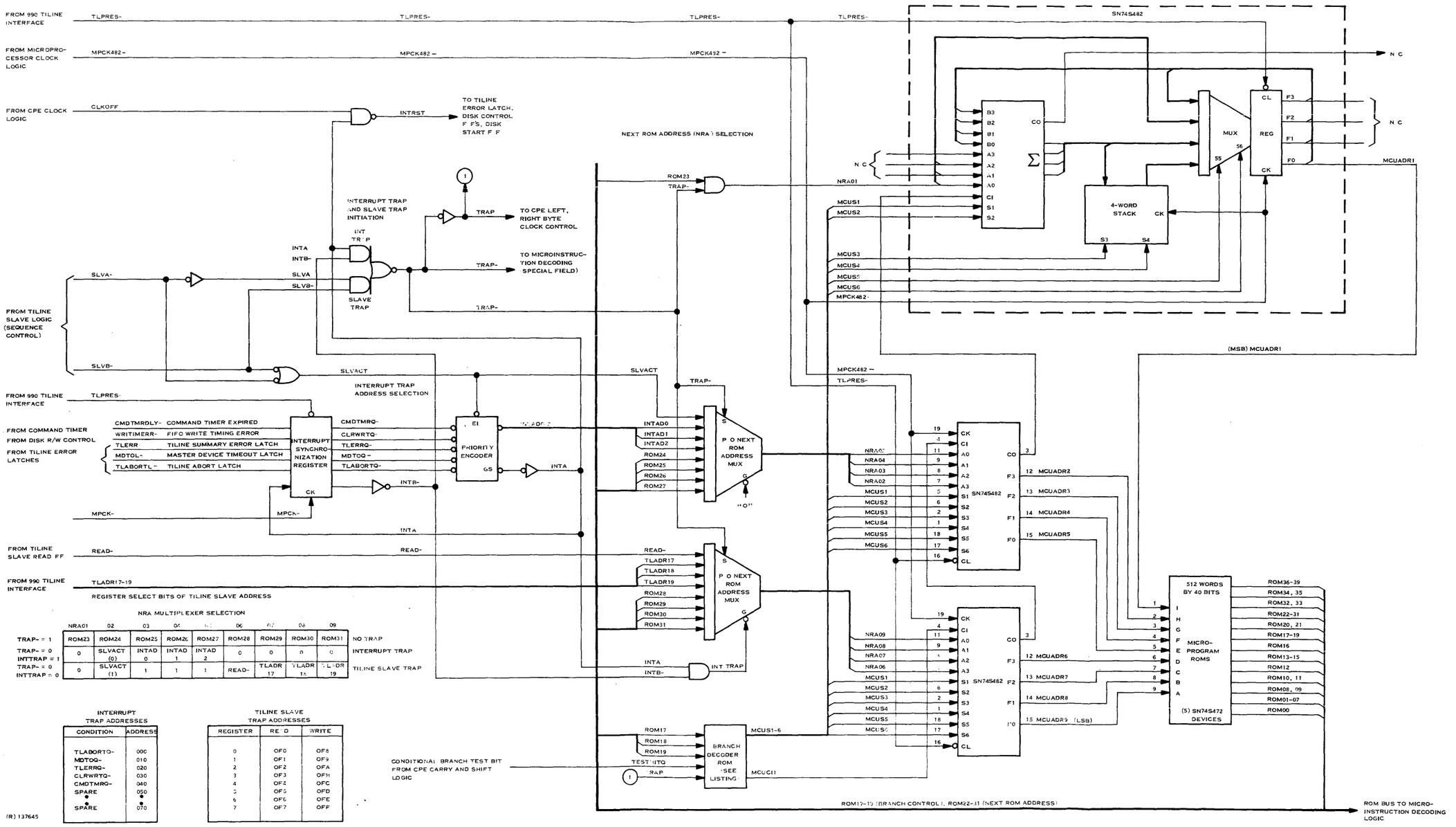


Figure 2-32. Microprogram Address (MCUADR) Control

The three SN74S482 devices have a combined addressing capability of 12 lines, but only nine lines are required by the microprogram ROMs. The addresses selected are determined by the address select code and address carry from the branch control ROM, and by the input from the next ROM address (NRA) multiplexers. The TILINE power reset, TLPRES-, is the single exception. TLPRES- is directly wired to the clear input of the address generator output registers, and causes an asynchronous jump to trap vector address 000_{16}.

In the absence of any trap conditions, the currently executing microinstruction determines which instruction is to be executed next as shown in the detailed timing diagram, figure 2-33. For conditional instructions, such as conditional branches or conditional returns, the test bit is used to select one of the two possible alternative instructions. This information is carried in the branch control (ROM 17-19) and next ROM address (ROM 23-31) fields of the current microinstruction. The next ROM address field is routed through the next ROM address multiplexers (in the absence of a trap) to the address generator inputs. The branch control ROM decodes ROM 17-19, the test bit and the trap input to determine the address selection code and address carry.

The address generators are clocked on the trailing (positive-going) edge of microprocessor clock. The SN74S482 devices require a fast-rising edge for proper triggering. This sharp edge is provided by MPCK482-, which is an isolated and lightly loaded version of microprocessor clock, MPCK-. MPCK482- is dedicated to the three SN74S482 devices; no other devices are clocked by MPCK482-. The rising (trailing) edge of MPCK482- clocks the address generators to place a new nine-bit microinstruction address (MCUADR 1-9) on the microprogram ROM input lines.

2.9.3.1 Trap Operation of Address Logic. Trap operations can be divided into three types for purposes of description. These types are:

- TILINE slave traps
- Microcode interrupt traps
- Power and I/O reset traps

TILINE Slave Traps. A TILINE slave trap allows the 990 central processor to load a control word into one of the TILINE slave registers, R0-R7, or to read a status word from one of these registers. The TILINE slave registers are scratchpad registers R0-R7 of the 3002 CPE devices. Reading from a CPE register, or writing into it, requires at least two CPE instructions.

The TILINE slave traps can be enabled or disabled under microprogram control. Bit 16 of the microinstruction is the enable slave bit. If it is a logic 0, the slave logic is disabled, and the controller rejects the attempted operation. Refer to the TILINE slave logic description for the details. In order to prevent a slave trap from interfering with an on-going operation, bit 16 is not enabled unless the microprogram is in the idle loop, or is in the process of executing a previously initiated slave trap.

Assume that the controller microprogram is in the idle loop, and the 990 processor initiates a slave read or write operation. The SLVA and SLVB- signals from the TILINE slave logic combine to enable the TRAP, TRAP-, and SLVACT signals, as shown in the timing diagram, figure 2-34. The TRAP signal into the branch control ROM causes the address generator to store the current instruction address in the stack for later return.

The TRAP- signal to the next ROM address multiplexers takes control of the NRA field away from the microprogram ROM and gates the slave trap address onto these lines.

TRAP- forces NRA01 to zero and selects SLVACT and INTAD0-2 to supply NRA02-05. SLVACT is high, disabling the interrupt priority encoder, so INTAD0-2 are also high. Thus, the two most significant (hexadecimal) digits of the trap address are always $0F_{16}$.

TRAP- steers the NRA multiplexer to select READ-, TLADR17, 18, 19 to supply NRA 06-09. TLADR17-19 are the three least significant TILINE address bits, which select the individual register. The TILINE read slave trap addresses for R0-R7 are 0F0-0F7, respectively. The write slave trap addresses for R0-R7 are 0F8-0FF, respectively.

Microcode Interrupt Traps. The microcode interrupt traps are initiated by error conditions which require immediate attention at the expense of the on-going operation, if any. Unlike the slave read and write traps, the interrupt traps cannot be disabled under microprogram control. The interrupt trap conditions, in order of priority, are:

- TILINE Abort (TLABORTL-)
- TILINE Master Device Timeout (MDTOL-)
- TILINE Error (TLERRL-)
- FIFO Write Timing Error (WRITIMERR-)
- Command Timer Delay Expired (CMDTMRDLY-)

The so-called TILINE abort is a special case which is actually a power failure, power reset or general I/O reset trap. These conditions affect the controller logic in a way different than the other microcode interrupt traps, so they are described under the heading "Power and I/O Reset Traps", following.

Figure 2-35 is a timing diagram for the interrupt trap and return. The trap conditions occur asynchronously, but are synchronized to the trailing edge of MPCK- in an SN74LS174 register. A priority encoder assigns an address (INTAD0-2) to the highest priority active interrupt and enables the TRAP, TRAP- and INTTRAP signals.

The TRAP- signal forces NRA01 to zero, and steers the next ROM address multiplexer to select SLVACT (which is zero) and INTAD0-2 as the NRA 02-05 inputs to the address generator. The INTTRAP- signal forces NRA06-09 to all zeros. The resulting trap address assignments are:

TILINE Abort	000
TILINE Master Device Timeout	010
TILINE Error	020
FIFO Write Timing Error	030
Command Timer Delay Expired	040
Spares	050-070

The TRAP signal steers the branch control ROM to a standard trap instruction. The MCUS1-6 outputs of the branch control ROM cause the address generator to store the current output address in the stack, and select NRA01-09 on the next positive going edge of microprocessor clock.

The instruction that is on the ROM00-39 lines when the TRAP- goes active (low) is arbitrarily called instruction N. In the absence of a trap, the results of instruction N would be stored in the CPE internal registers on the negative- going edge of microprocessor clock. However, the TRAP signal suppresses the CPE clock inputs, CPRCK- and CPLCK-.

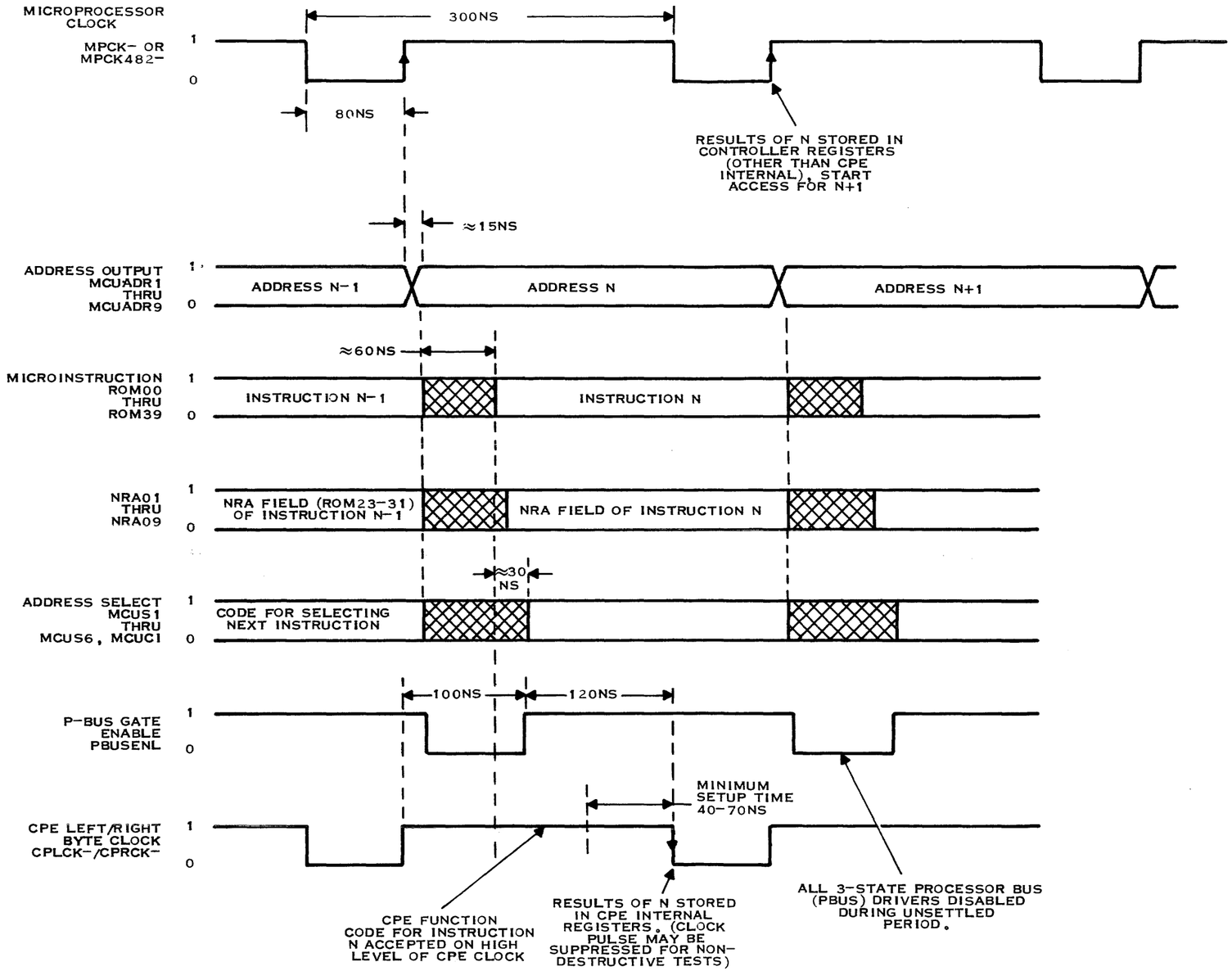


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Figure 2-33. Detailed Timing Diagram of Normal Microinstruction Access Cycle

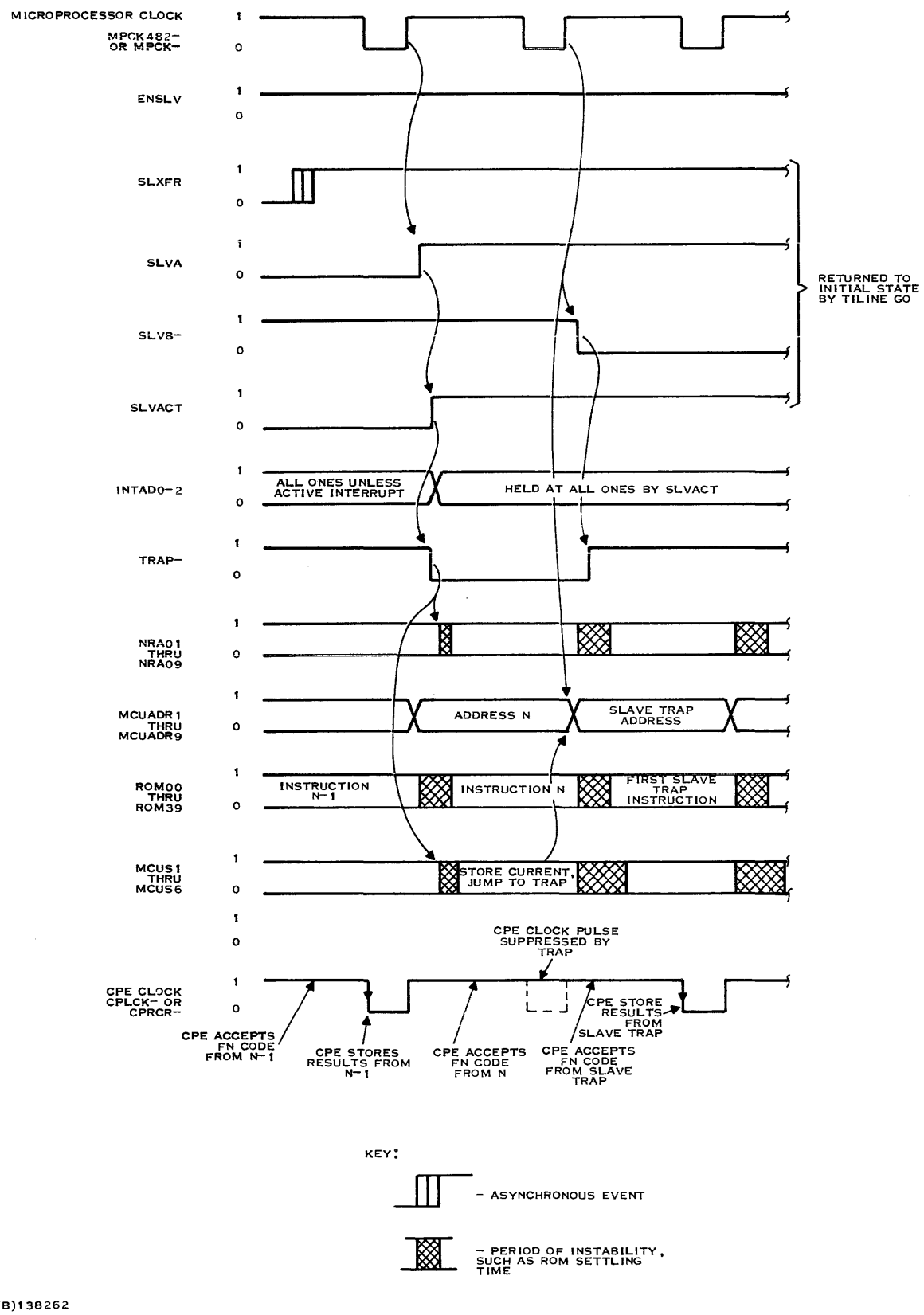


Figure 2-34. Detailed Timing Diagram for TILINE Slave Trap

Clock inputs to the address generator are not suppressed, so the microprogram jumps to the interrupt trap address on the positive-going (trailing) edge of microprocessor clock. INTB- goes low on this same edge, disabling TRAP, TRAP- and INITRAP. Microprocessor clock to the CPE inputs is enabled, and the address control logic reverts to a nontrap mode. The second instruction in the trap sequence will be selected according to the branch control and NRA fields of the first trap instruction.

After the initial jump to the first trap address, the remainder of the trap sequence executes like any other code sequence. The branch control field of the last trap instruction commands a return to the address stored in the SN74S482 stack register, the address of instruction N. On the next positive-going clock edge, instruction N is read from the microcode ROMs and placed on output lines ROM00-39. Instruction N executes normally, and the microprogram advances to instruction N+1.

NOTE

N-1, N, and N+1 refer to the planned instruction sequence in the interrupted segment of microcode. They are not necessarily located at sequential addresses.

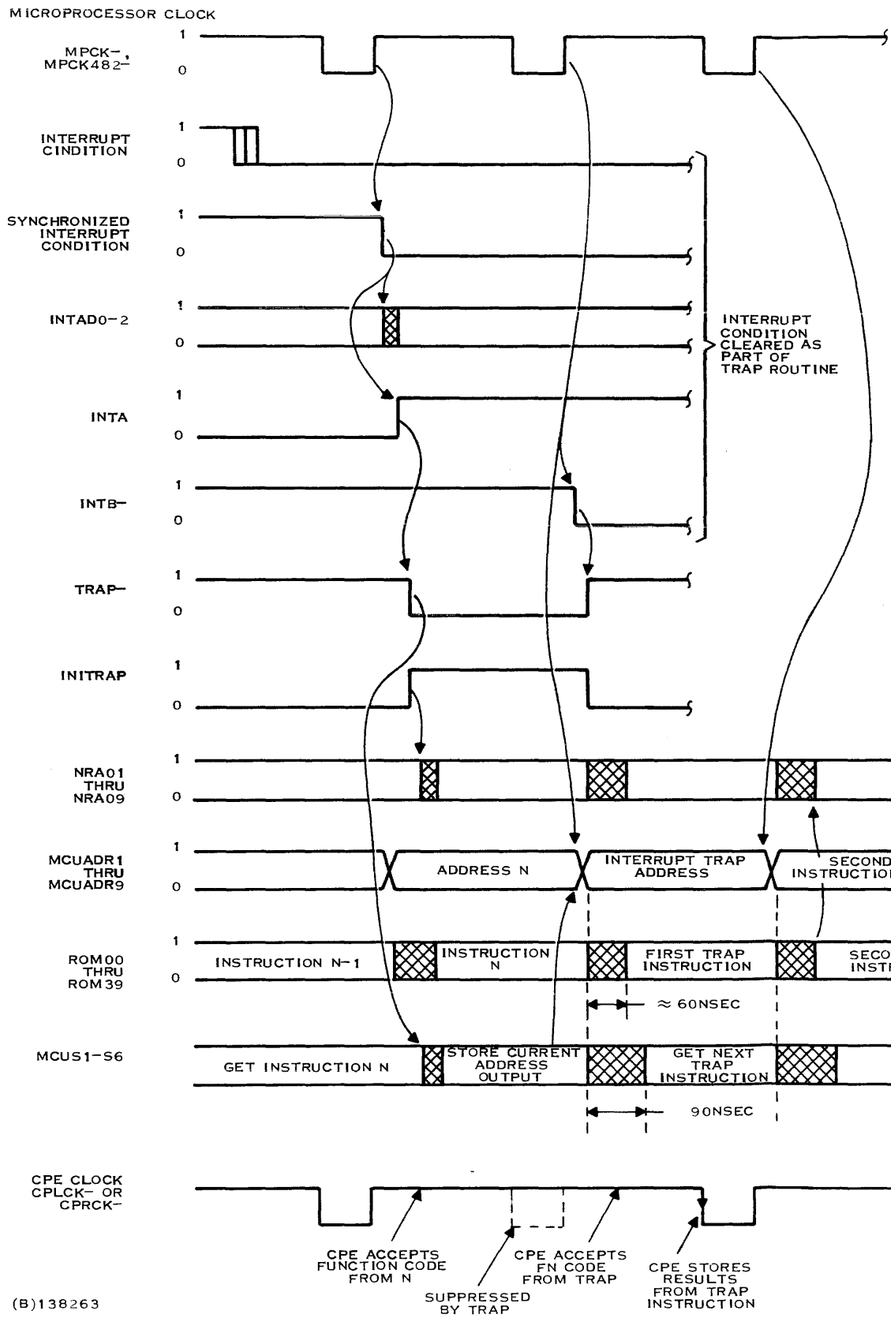
Power and I/O Reset Traps. The power and I/O reset trap may be initiated by any of three signals from the 990 backplane to the controller. These signals are: TILINE power failure warning pulse (TLPFWP-), TILINE power reset (TLPRES-), and TILINE I/O reset (TLIORES-). Each signal affects the controller logic in a slightly different way, but they share a common microcode trap routine.

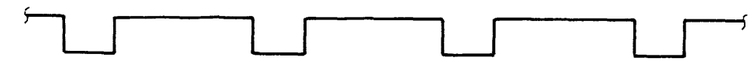
The TLPRES is a normally high signal from the 990 chassis power supply that goes low at least 10 microseconds before a normal or fault shutdown of dc power. TLPRES- remains low during a power failure and is not released until all dc voltages from the power supply are up and stable. TLPRES- is a protective signal that resets all peripheral device controllers and the 990 CPU. Logic in each peripheral device controller forces the device control signals to a safe state, so that the peripheral does not damage itself while the controller and CPU are down. The TLPFWP is a normally high signal (except in 990/9) from the 990 chassis power supply. The occurrence of this low pulse is a warning that a power shutdown is in progress, and that a TILINE power reset is imminent. This early warning signal goes low at least 7 milliseconds before the power reset, allowing the CPU time to execute a power shutdown routine before the logic reset. The power failure warning pulse remains active until the power reset (TLPRES-) occurs.

The TLIORES is a control signal from the 990 CPU. TLIORES- goes low to halt and reset all input output devices and controllers. It is a 100- to 500-nanosecond low pulse generated as the result of the CPU executing a reset (RSET) instruction. The RSET instruction may be written into a program, or it may be generated as a result of depressing the RESET button on the programmer panel.

All three of these trap conditions share the same microcode trap sequence, shown in the flowchart of figure 2-36. Note that these trap routines end in the idle (IDL) routine, and do not return to the interrupted sequence. The occurrence of any of these traps will abort any on-going operation and set the abnormal completion bit in the controller status register (CPE internal register R7). Notice that the trap routine uses the long diagnostic test check (LTC), Z diagnostic test (ZDT) and terminate (TRM) sequences as subroutines.

Refer to the simplified logic drawing and to the detailed timing diagram for I/O reset, figure 2-37. The TLIORES- input occurs asynchronously with respect to microprocessor clock (MPCK-) in the disk controller. The general reset signals, RST, RST1, are isolated versions of TLIORES- which





KEY:

- PERIOD OF INSTABILITY SUCH AS ROM OR PRIORITY ENCODER SETTLING TIME
- ASYNCHRONOUS EVENT

INSTRUCTIONS N-1, N, N+1 REFER TO THE PLANNED SEQUENCE OF INSTRUCTIONS. THEY ARE NOT NECESSARILY AT SEQUENTIAL ADDRESSES.

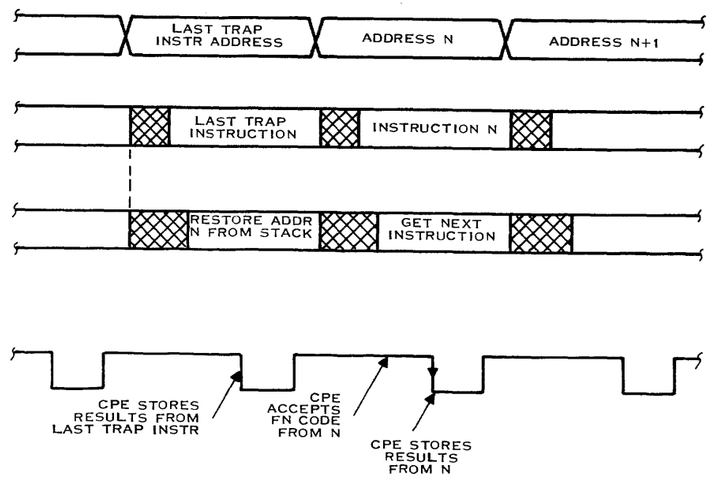


Figure 2-35. Detailed Timing Diagram for Interrupt Trap and Return

unconditionally force the interface control logic to a safe state. TLIORES- is latched (as TLABORTL-) and then synchronized with microprocessor clock as TLABORTQ-. From this point on, the logic operation is identical to that for any of the microcode interrupts.

The synchronized TLABORTQ- signal into the priority encoder enables the group select output, INTA, that in turn enables the TRAP- signal. The address outputs of the encoder INTAD0-2 go to 000. The TRAP- signal forces NRA0 low and steers the NRA multiplexers to select INTAD0-2 as the source for NRA02-05. INITRAP, which is simply an active high version of TRAP-, puts all zeros on the NRA06-09 lines. The resulting address input to the address generators is 000 (hex), but the jump is not made until the next microprocessor clock pulse (trailing edge).

At the time that TLIORES- occurred, the controller was executing some instruction, which is arbitrarily labeled instruction N-1 in the timing diagram. The first clock pulse steps the address generator to instruction N on the trailing (positive-going) edge. After a brief ROM settling time, instruction N is on microcode ROM output lines ROM00-39. However, the active TRAP- signal disables CPE left and right byte clocks. Therefore, the CPE operations associated with instruction N are not executed. The function code, ROM01-07, is loaded into the CPEs, but the leading (negative-going) edge which would store the results in the CPE registers does not occur. If this were a regular microcode interrupt, it would be necessary to return to instruction N and execute it when the trap sequence completed. However, the power and I/O reset traps all end in the idle routine, rather than with a return to the interrupted sequence.

During the time that TRAP- is selecting an address input to the address generators, TRAP is determining the address selection code, MCUS1-6, via the branch control ROM. Regardless of any other inputs to the branch control ROM, the TRAP signal fetches a standard trap code from the ROM; MCUS1-6 = 101100 and MCUCI1 = 0. This code causes the address generator to put the current-output address (the address of instruction N) into the push-down return address stack, and to select the input address (NRA01-09 = 000_{16}) as the next output address. These actions are performed on the next positive-going (trailing) edge of microprocessor clock, MPCK482-. (The trap signal does not disable the general microprocessor clock, MPCK-, or the isolated version, MPCK482-, which clocks the SN74S482 address generators.)

The clock pulse which forces the jump to trap address 000 also disables TRAP, TRAP-, and INITRAP via the INTB- output of the interrupt synchronizing register. The active duration of TRAP- is one clock period, about 300 nanoseconds, between successive trailing edges of microprocessor clock.

Refer to the I/O and power reset trap flowchart, figure 2-36. The I/O reset has caused a jump to the first instruction, INT00, of this trap routine. CPE left and right byte clocks are reenabled so that the operation shown in the INT00 box is actually performed on the next clock pulse. That clock pulse advances the address generator to the address specified by the branch control and NRA fields of microinstruction INT00. The dotted box may be ignored because a power reset is not involved. The second instruction of the trap sequence is LTC01, which is part of the long diagnostic jumper check (LTC) subroutine. This is a branching control subroutine which tests a jumper to determine whether the diagnostic test (ZDT) should be performed. Like all the conditional branching microinstructions, LTC01 sets the clock stop bit (ROM00) and suppresses the next CPE clock pulse, as shown on the timing diagram.

The remainder of the trap routine executes like any other sequence of microinstructions. The TLIORES- pulse that initiated the trap is approximately 250 nanoseconds wide. When TLIORES- is released, the INTA and CLKOFF signals combine to reset the interrupt latch with the INTRES- pulse. The CLKOFF signal assures that the interrupt reset does not occur too close to the clock pulse to meet setup time requirements. The next two clock pulses clear the interrupt logic to its initial state.

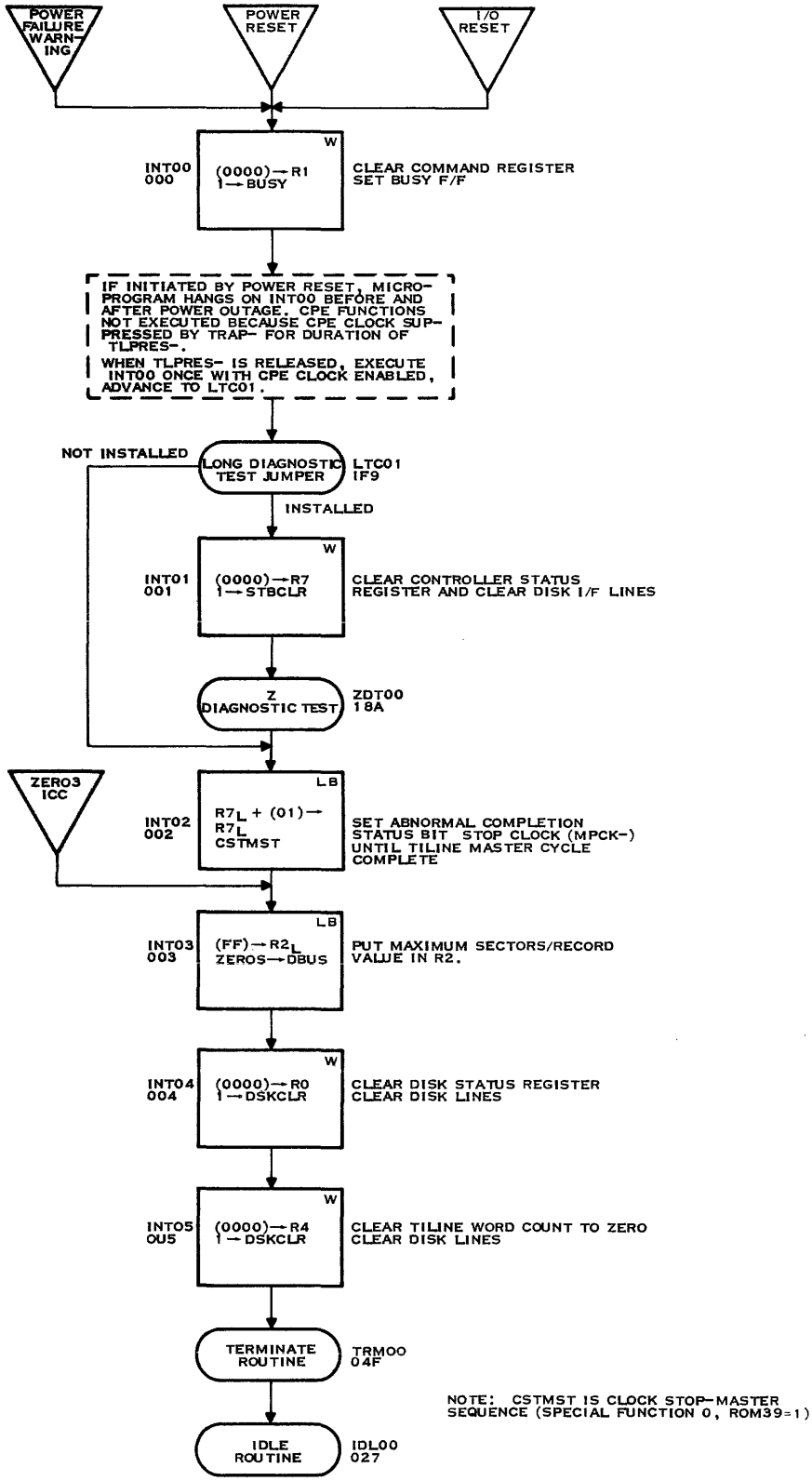
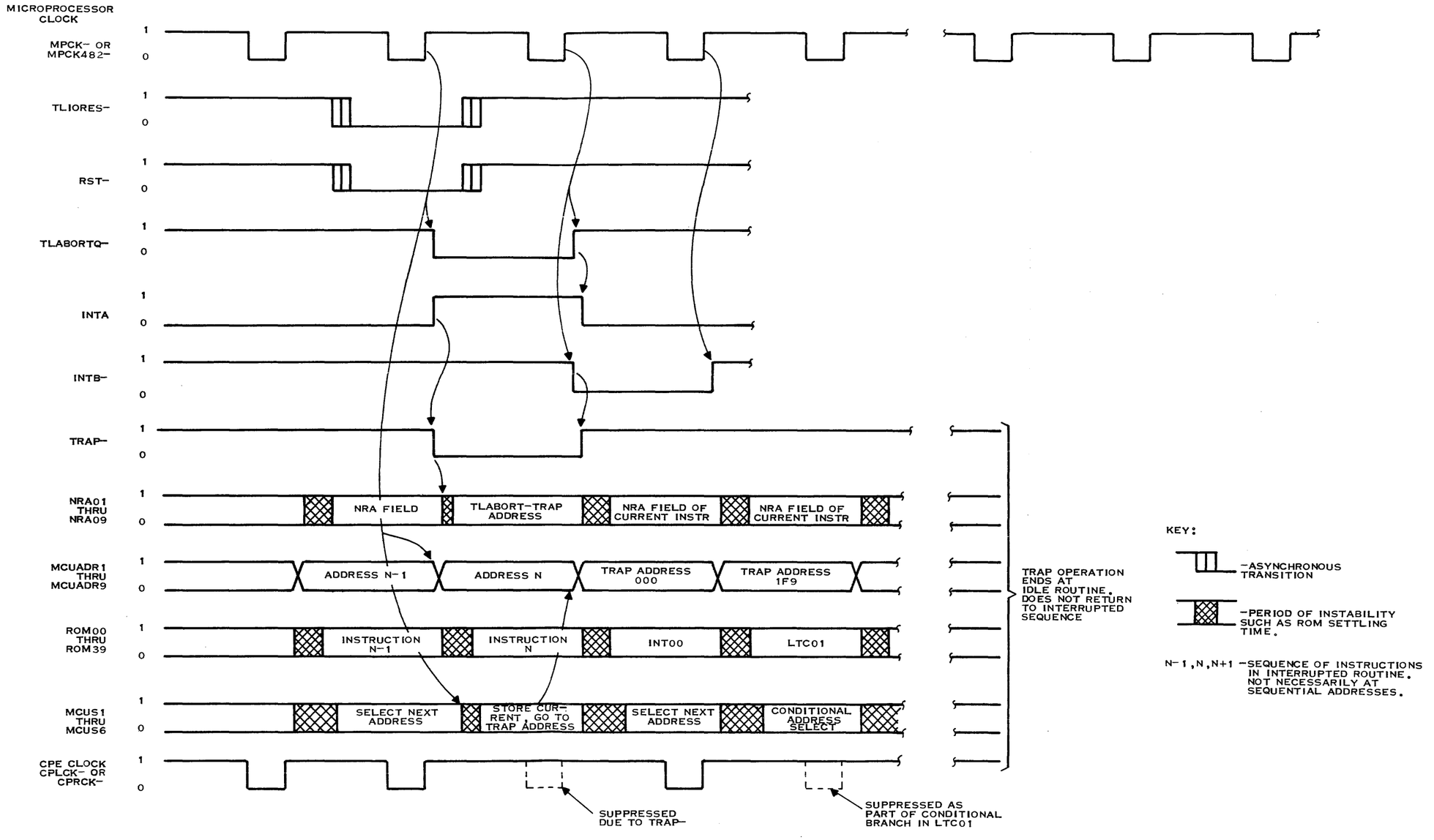


Figure 2-36. I/O and Power Reset Flowchart



(B)138259

Figure 2-37. Detailed Timing Diagram for TILINE I/O Reset (TLIORES-) Trap

Refer to the simplified logic diagram and the detailed timing diagrams for the power failure warning trap, figure 2-38. The TLPFWP- input to the controller occurs asynchronously with respect to microprocessor clock. The power failure warning is latched as TLABORTL-, and synchronized with MPCK- as TLABORTQ-. Unlike the I/O reset or the power reset, the power failure warning does not issue a general reset to the controller interface logic. The power failure warning trap is executed like the other microcode interrupt traps (TILINE master device timeout, TILINE parity error, clear write, command timer expired), except that it has first priority.

The trailing (positive-going) edge of MPCK- synchronizes the power failure warning as TLABORTQ-. The SN74148 priority encoder develops the interrupt address (INTAD0-2 = 000) and the group select output (INTA) enables TRAP- and INITRAP. INITRAP and TRAP- cause an address of 000_{16} to appear at the inputs of the address generator. The TRAP- signal to the branch control ROM fetches a standard trap command, MCUS1 - S6= 101100 and MCUCI1 = 0. This code causes the address generator (on the next positive-going MPCK482- edge) to store the current output address in the internal pushdown stack and to latch the trap address as the new address output.

The TRAP- signal also disables microprocessor left and right byte clocks, CPLCK- and CPRCK-. This prevents the microprocessor-related operations of the current microinstruction from being executed. In the absence of an active TRAP- signal, the active CPEs would have accepted the CPE function code (ROM01-07) on the high level of microprocessor clock, and would have executed on the rising (trailing) edge of the clock. The TRAP- signal suppresses the clock pulse (holds CPRCK-, CPLCK- high) so the CPEs do not execute instruction N.

Note that TRAP- only disables the clock into the CPE array, not the general microprocessor clock, MPCK-, or the isolated version which clocks the address generators, MPCK482-. The same clock pulse which clocks the address generators to jump to the trap address also clears the TRAP- signal by latching INTA into the synchronizing register as INTB. INTB, after inversion, disables the TRAP- signal, so that the duration is only one clock period, 300 nanoseconds. If TRAP- were not released in this manner, the microcode program would remain hung up on the initial trap vector instruction at address 000 (hex).

After the initial jump, the trap sequence executes like any other sequence of microinstructions. The trap sequence involves setting safe values into some of the CPE internal registers, and executing an automatic self-diagnostic routine. At the end of the trap sequence, the controller goes into the idle routine.

The power failure warning pulse remains active for at least seven milliseconds and is not released until after the TILINE power reset occurs. TLABORTL- and TLABORTQ- remain active, but have no effect, since the duration of TRAP- is set by microprocessor clock, not by the duration of the power failure warning.

The time between the onset of the power failure warning and the power reset, approximately seven milliseconds, is very large with respect to the time required to execute the trap routine, so the controller will be idling when the power reset occurs. The right side of the timing diagram shows the initial operations of the power reset cycle. See the power reset description in the next paragraph.

Refer to the simplified logic drawing and the detailed timing diagram for the TILINE power reset operation, figure 2-39.

Recall that TLPRES- goes active (low) before a power failure, remains low during the power failure and remains low until all dc voltages are up and stable. The TLPRES- signal is directly wired to the clear inputs of the SN74S482 address generators. Therefore, TLPRES-, unlike any other trap

condition, can asynchronously disrupt an on-going microinstruction and force an immediate jump to the trap vector, location 000_{16}. All other trap conditions are serviced after synchronization with microprocessor clock.

The power reset should be preceded by a power failure warning, TLPFWP-, so that when TLPRES- occurs, the controller should be idling and the TLABORTL-, TLABORTQ-, INTA, and INTB- signals should be as shown at the left edge of the timing diagram. If any of them are in alternate states, as shown by the dotted lines, TLPRES- corrects them asynchronously.

TLPRES- is wired to the direct clear input of the SN74S164 interrupt synchronizing register. When TLPRES- occurs, it forces all outputs of the synchronizing register low so INTB- goes high. With all its inputs forced low, the priority encoder selects the highest priority input (TLABORTQ-) and gates out an address of 000, and a group select output. The address is not meaningful at the moment, because TLPRES- unconditionally resets the address generators.

TLPRES- forces INTA and INTB- high so that TRAP- and INITRAP remain active until the first clock pulse after the power reset releases. TRAP- suppresses CPE left and right byte clock so that no CPE operations are performed for the duration of the power reset.

The microcode program remains hung at address 000 (instruction INT00) for the duration of the power reset. The register clear operation shown on the trap flowchart at instruction INT00 is not executed, because CPE clock is disabled.

When the power reset is finally released, the logic performs a normal trap to location 000. That is, the TRAP- and INITRAP signals continue to provide an all zeros address on NRA01-09, and the trap select code from the branch control ROM (MCUS1-6) is no longer over-ridden by TLPRES-. The address generator steps through the rest of the trap operation like any other microcode sequence, and ends at the idle routine.

2.10 ROM BUS AND MICROINSTRUCTION DECODING

The disk controller operates under the control of a permanent microinstruction program. This microprogram consists of 512 microinstructions of 40 bits each which are burned into five SN74S482 devices. The microprogram-controlled operations, with particular emphasis on CPE operations, are summarized in the flowcharts of Appendix D. A complete listing is provided in Appendix E.

The outputs of the microprogram read-only memory devices, ROM00-39, are collectively called the ROM bus. The ROM bus signals are distributed throughout the disk controller. Decoding of the different microinstruction fields is distributed throughout the controller rather than being centralized in one giant decoder. Figure 2-9, which shows the microinstruction format, is useful for understanding the decoding scheme.

Figure 2-40 shows the ROM bus and the highlights of microinstruction decoding. Branch control decoding and next ROM address control are omitted from this figure and included with the microprogram address control logic.

2.10.1 PROCESSOR BUS SOURCE AND DESTINATION FIELDS. The processor bus source field (ROM13-15) determines which data is gated onto the three-state processor bus, PBUS00-15. This is the main data transfer bus within the disk controller. The processor bus destination field, ROM20 and 21, selects one of several registers to accept data from the processor bus.

These two microinstruction fields, along with ROM 33 and a P-Bus enable signal (or CLKT1-, fine line), are connected to the inputs of the processor bus control register. It is the register outputs which are actually decoded. The processor bus control register is an SN74S373 transparent D-latch

register. As long as the enable input (MDACT-) to the register is held high, the register outputs follow the register inputs with no latching action. This is the transparent mode of operation. MDACT-, master device active, is high for any controller operation except a TILINE master access cycle. Therefore, unless a TILINE master read or master write cycle is in progress, PBUSENL is identically PBUSEN (or CLKT1-, fine line), ROM13L-15L is identically ROM13-15, ROM33L is identically ROM33, and ROM 20L and 21L are identically ROM20 and ROM21.

Operation during a TILINE master cycle is described below, after the general description of bus source and destination decoding.

The processor bus source decode is an SN74S138 3:8 decoder/multiplexer. The decoder is enabled by PBUSENL. PBUSENL is basically a delayed form of microprocessor clock. PBUSENL goes low immediately after a new microprogram address (MCUADR1-9) is selected and disables bus source decoding until 100 nanoseconds after the trailing edge of microprocessor clock. This prevents any device from putting data onto the processor bus until the ROM bus transients have settled, and ROM00-39 are stable on the lines. Refer to the detailed timing diagram (figure 2-33) for a normal microinstruction access cycle and for more information on PBUSENL timing.

With PBUSENL high, ROM13L-15L are decoded as follows:

ROM13L-15L	Decoder Output Signal	Definition
000	PBZERO-	All zeros (high levels) on P-bus
001	PBCPE-	CPE D-bus outputs on P-bus
010	(none connected)	No P-bus activity
011	PBTLDAT-	TILINE line receiver outputs on P-bus
100	PBDSKDAT-	Disk data from FIFO (or direct read register) on P-Bus
101	(none connected)	No P-bus activity
110	PBDSKSTA-	Disk drive status on P-bus
111	(none connected)	No P-bus activity

The processor bus destination decoder is an SN74S139 2:4 decoder. In addition to the destinations enabled by this decoder, one of the special function encoders enables loading of the TILINE MSB address register from PBUS11-14. ROM20L, 21L are decoded as follows:

ROM20L, 21L	Decoder Output Signal	Definition
00	(none connected)	
01	UNITLOAD-	Loads disk unit select code from PBUS04-07 into the disk select register
10	UTCSHIN-	Shifts CPE output word into FIFO for transmission to disk. Not required for TILINE to disk transfers
11	DSKBUSLD-	Loads PBUS07-15 into disk address select register.

ROM33L from the processor bus control register does not perform any function unless a TILINE master cycle is in progress.

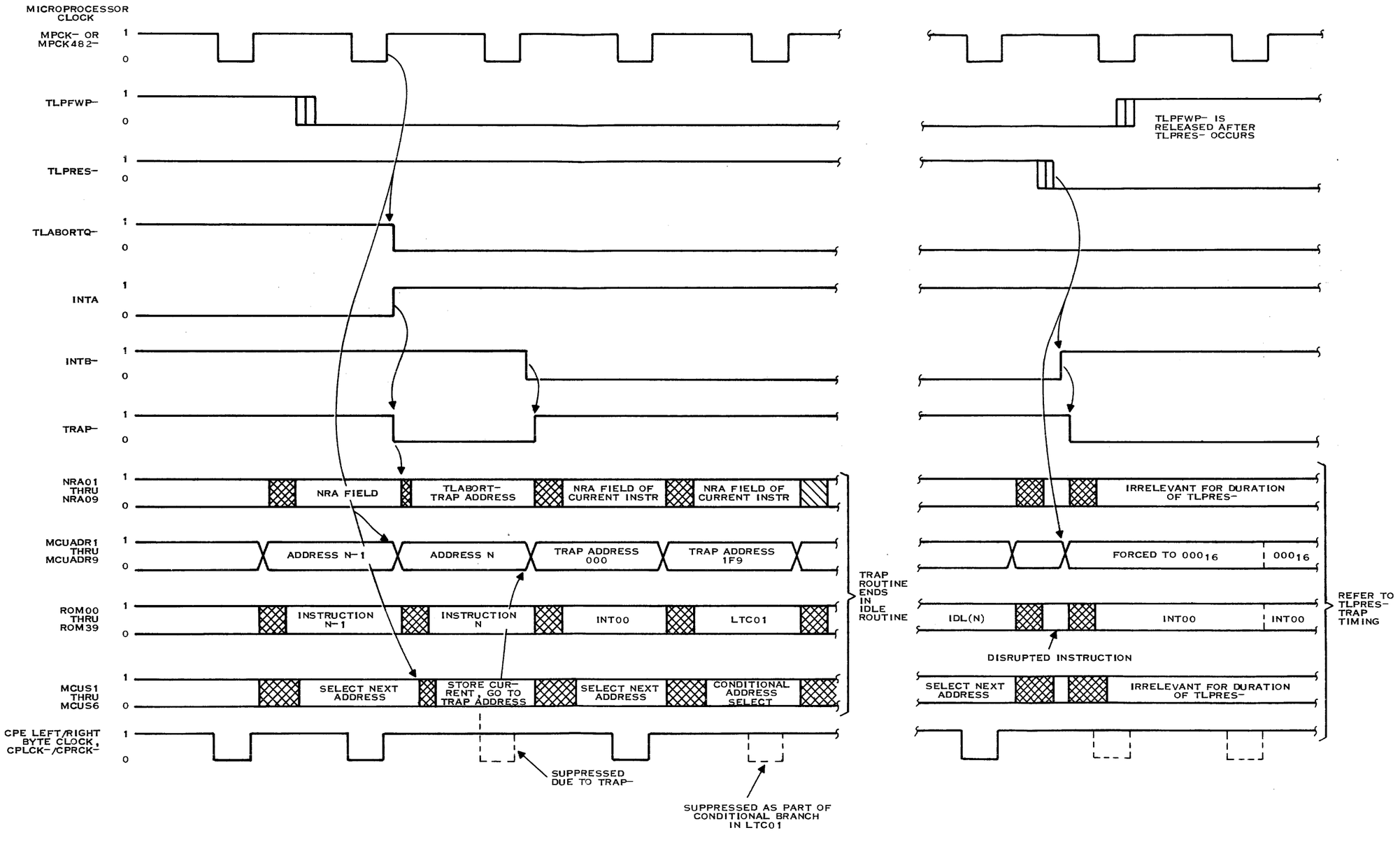


Figure 2-38. Detailed Timing Diagram for TILINE Power Failure Warning (TLPFWP-) Trap

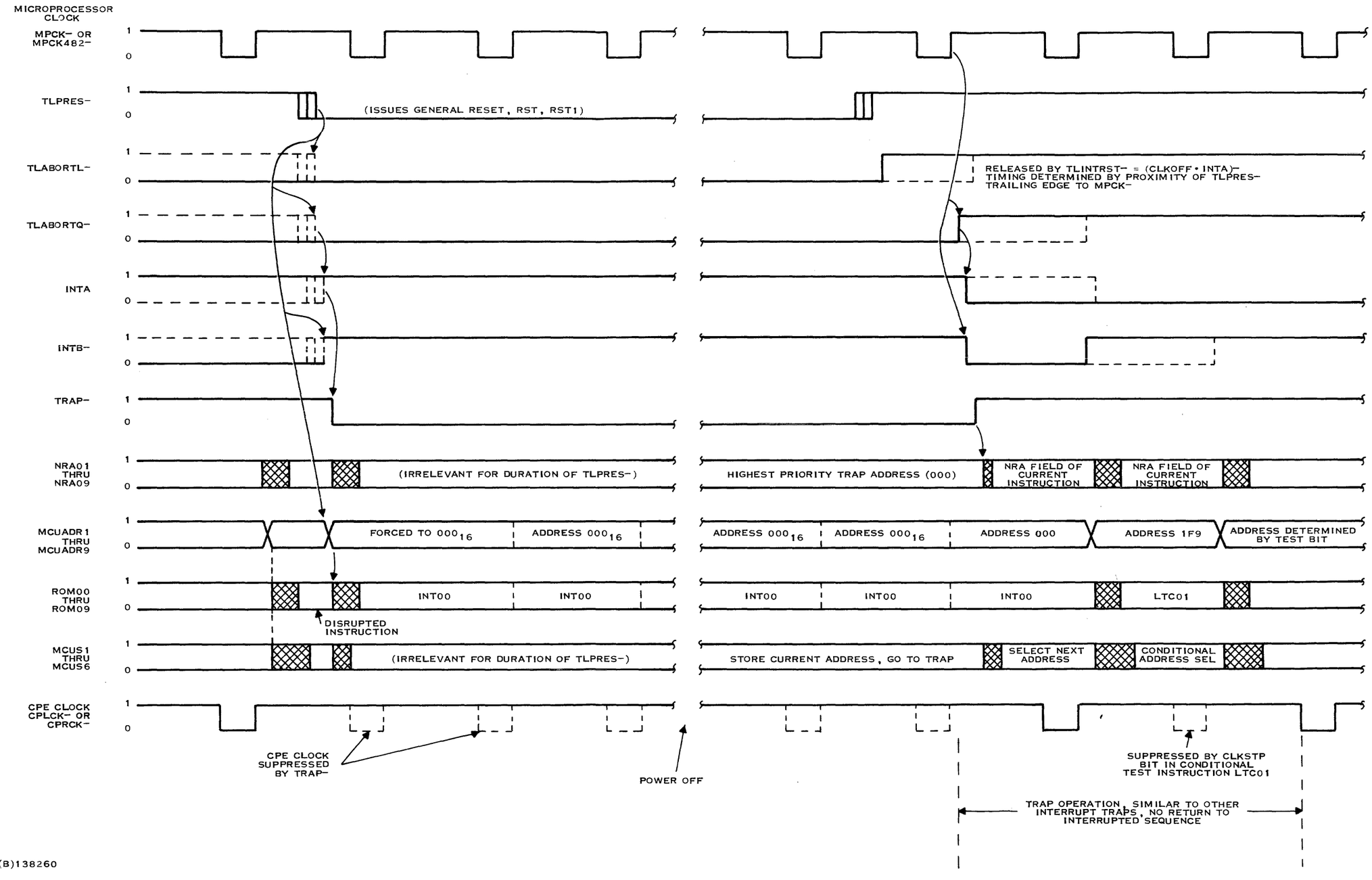


Figure2-39. Detailed Timing Diagram for TILINE Power Reset (TLPRES-) Trap

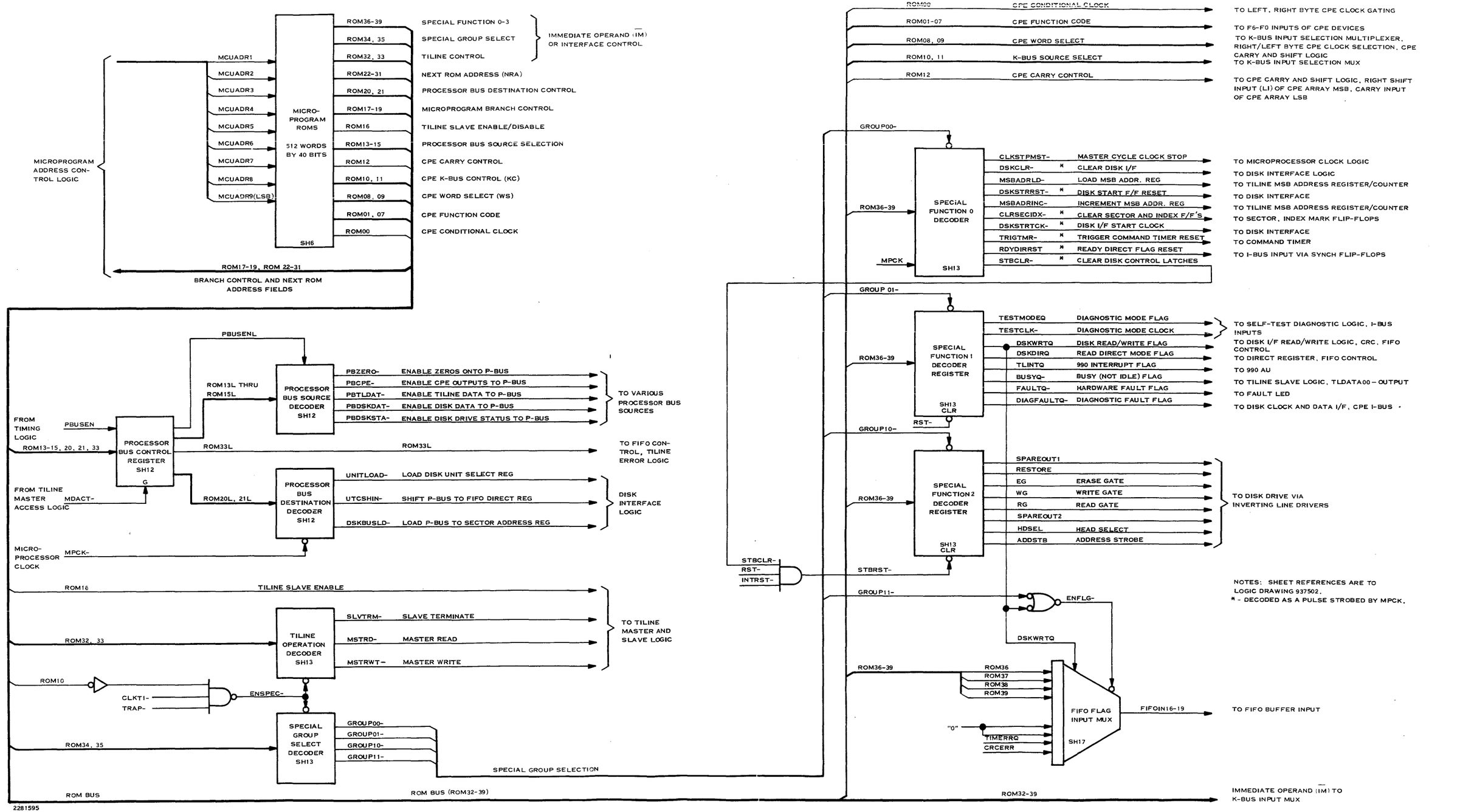


Figure 2-40. ROM Bus and Microinstruction Decoding

The TILINE master cycle is initiated by a microinstruction. If the master cycle was initiated for a disk-to-memory or a memory-to-disk data transfer, the controller CPEs are not involved in the transmission. The initiating microinstruction establishes whether it is a master read or master write operation (ROM32,33) and establishes the data path on the P-bus with the P-bus source and destination fields (ROM13-15L, ROM20,21L). The master device active F/F sets at the beginning of the master cycle, and MDACT- goes low to latch the processor bus control register. With these outputs latched, the controller is free to execute other microinstructions independently of the TILINE master cycle. As long as these microinstructions do not require any P-bus data transfers, there is no interference between the parallel operations. The controller uses this time for bookkeeping within the CPE devices, such as updating the TILINE word count maintained in register R4.

2.10.2 IMMEDIATE OPERAND/TILINE OPERATION/SPECIAL FUNCTION FIELD. ROM32-39 is a multiple-purpose field of the microinstruction. If the K-bus control (KC) field which controls CPE mask bus inputs is 10 or 11, ROM32-39 serves as an eight-bit immediate operand to the K-bus inputs of both CPE bytes. The K-bus inputs are active low, so the contents of ROM32-39 are effectively inverted. A typical use for an immediate operand is to AND the left or right byte of a status word with the eight-bit immediate operand to test an individual status bit. The result of the test is used to control a conditional branch in the microprogram.

If the KC field is 00 or 01, a constant value ($FFFF_{16}$ or 0000_{16}) is loaded into the CPE K-bus inputs, and TILINE and special function decoders are enabled. These decoders are shown at the right side of the decoding block diagram.

The enable special fields (ENSPEC-) signal is enabled if ROM10 = 0 (KC field = 0X), no trap operation is in progress, and the CLKT1- signal is high. CLKT1- is used as a hold-off signal to prevent decoding of ROM32-39 before the ROM outputs have settled.

ROM 32 and 33, the TILINE control field, are decoded as follows:

ROM32,33	Decoder Output Signal	Definition
0 0	(none connected)	NOP
0 1	SLVTRM-	Terminate slave operation
1 0	MSTRD-	Master read cycle
1 1	MSTWRT-	Master write cycle

ROM 34 and 35 are used as a special function group select field. The code in ROM34,35 determines whether ROM36-39 are decoded as special function 0, 1, 2, or 3. The outputs of the special function group decoder enable one of the four special function decoders. This is a straight numerical decode as follows:

ROM 34, 35	Decoder Output
0 0	GROUP00-
0 1	GROUP01-
1 0	GROUP10-
1 1	GROUP11-

Refer to the timing diagram for special function decoding, figure 2-41. The trailing (positive-going) edge of CLKT1- starts the decoding chain. ENSPEC- goes low after one gate delay, and the appropriate function group select (GROUP00- through GROUP11-) goes active after a short decoding delay.

There are two distinct classes of functions included in special function 0 if it is selected. All of the odd opcodes are decoded in one decoder which is unclocked. The output signals are asserted as soon as the decoder delays have expired, about 85 nanoseconds from the trailing edge of MPCK-. This delay is important because it is the trailing edge of MPCK- that triggers the address generator to select a new microinstruction. If the special field were decoded before the ROM outputs settle, false decodes could occur. The trailing edge of CLKT1- may be delayed by addition of capacitor C2, as shown on sheet four of logic drawing 937502 (PWB) or on drawing 2262102 (fine line), to correct this problem if it arises. Normally the inherent gate and decoding delays are long enough to prevent the problem.

The even opcodes in the special function 0 field are strobed functions, and the output signals are developed by a clocked decoder. The inverted form of microprocessor clock, MPCK, serves as a decoding strobe. If the microinstruction is selected by clock pulse n, the strobed output signal corresponds to clock pulse n + 1, plus about 30 nanoseconds of decoder delay inherent in the SN74LS138 device. With the exception of the command timer trigger (TRIGTMR-), the strobed outputs are disk interface control signals. Table 2-13 summarizes the special function 0 decoding.

Special function fields 1 and 2 control the inputs to a pair of SN74LS259 eight-bit addressable latches. The addressable latches act as decoders and as registers. The group select signal (GROUP01- or GROUP10-) enables one of the SN74LS259 devices. ROM36-38 serve as an address to select one of the addressable latches, and ROM39 serves as the set/reset (D) input to the selected latch. Tables 2-14 and 2-15 summarize the special field 1 and 2 decoding.

Special function field 2 is used to assert control signals to the disk drive. This register can be cleared by a general reset (RST-), an interrupt reset (INTRST-), or a strobe clear from the special function 0 decoder (STBCLR-). Special function field 1 is dedicated to controller internal functions, and the register can be cleared by a general reset (RST-).

The disk interface first-in, first-out (FIFO) buffer has 16 bits dedicated to disk read/write data, and four bits dedicated to flags. The four flag inputs to the FIFO, FIFOIN16-19, are selected by the FIFO flag input multiplexer. Special function field 3 allows the active microinstruction to set any of these four flag bits during a disk write operation.

Unlike the other special function fields, special function field 3 is positionally coded, with each bit dedicated to a specific flag, as follows:

ROM 36	37	38	39	FIFO Input Bit	Flag Register Output	Definition
			1	FIFOIN19	(no connection)	Spare flag bit
		1		FIFOIN18	STOPFLAG	Flag that accompanies last word of a TILINE-to-disk transfer through the FIFO, and notifies CPEs that the write buffer is done.
	1			FIFOIN17	CRCPREFLAG	Preset CRC generator to all ones.
1				FIFOIN16	CRCENFLAG	Enable CRC output to disk.

The decoding diagram covers only the highlights of decoding and the routing of microinstruction bits to other circuits within the controller. The functions of these bits are included in the individual functional block descriptions.

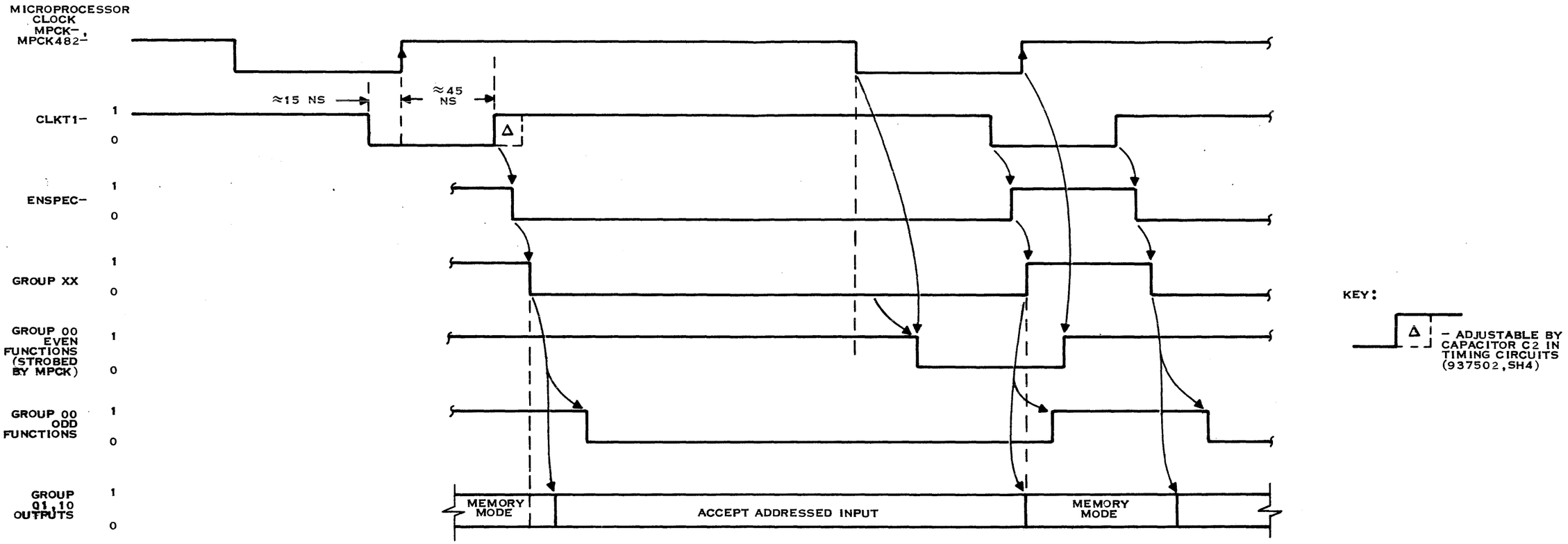


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Figure 2-41. Detailed Timing Diagram for Microinstruction Special Function Decoding

Table 2-13. Special Function 0 Decoder Outputs

(KC Field) ROM 10, 11	(Function Group) ROM 34, 35	ROM 36, 37, 38, 39	Signal Output	*Synchronized/ Unsynchronized	Definition
0 X	0 0	0 0 0 0	(none)	–	No operation.
0 X	0 0	0 0 0 1	CLKSTPMST–	U	Microprocessor clock (MPCK–) stop until TILINE master cycle complete.
0 X	0 0	0 0 1 0	DSKCLR–	S	Disk clear strobe– clears FIF0, disk start, and disk timing error logic.
0 X	0 0	0 0 1 1	MSBADRLD–	U	Enable load of four most significant TILINE address bits from PBUS11– 14 into MSB address register.
0 X	0 0	0 1 0 0	DSKSTRRST–	S	Disk start transfer latch reset (disk stop). Stop disk transfer. Similar to DSKCLR– above, but does not clear the FIFO.
0 X	0 0	0 1 0 1	MSBADRINC–	U	Increment TILINE MSB address register.
0 X	0 0	0 1 1 0	CLRSECIDX–	S	Clear sector mark and index mark detection latches.
0 X	0 0	0 1 1 1	(none)		
0 X	0 0	1 0 0 0	DSKSTRTCK–	S	Disk start transfer clock.
0 X	0 0	1 0 0 1	(none)		
0 X	0 0	1 0 1 0	TRIGTMR–	S	Retrigger (reset) command timer to prevent expiration of 190-200 millisecond delay and consequent interrupt trap operation.
0 X	0 0	1 0 1 1	(none)		
0 X	0 0	1 1 0 0	RDYDIRRST–		Reset ready direct status latch.
0 X	0 0	1 1 0 1	(none)		
0 X	0 0	1 1 1 0	STBCLR–	S	Clear drive control outputs of group 2 decoder/ register.
0 X	0 0	1 1 1 1	(none)		

Note:

*Synchronized outputs are strobed by next (inverted) microprocessor clock pulse, MPCK. Synchronized outputs are delayed approximately 150 nsec with respect to unsynchronized outputs.

Table 2-14. Special Function 1 Decoder/Register Outputs

KC Field ROM 10,11	Function Group Sel. ROM 34, 35	Latch Selection ROM 36,37,38	Data ROM 39	Latch Output	Description
0 X	0 1	0 0 0	0	TESTMODEQ = 0	Disk interface diagnostic mode flag.
			1	TESTMODEQ = 1	ROM 39 = 1 selects the test mode.
0 X	0 1	0 0 1	0	TESTCLK– = 0	Disk interface diagnostic clock, TESTCLK–, cycles data into or
			1	TESTCLK– = 1	out of the 264-stage test data shift register. Shifting occurs on the positive-going edge of TESTCLK–.
0 X	0 1	0 1 0	0	DSKWRTQ = 0	Disk interface read/write flag.
			1	DSKWRTQ = 1	ROM 39 = 1 Selects write mode.
0 X	0 1	0 1 1	0	DSKDIRQ - 0	Disk read direct mode flag.
			1	DSKDIRQ = 1	ROM 39 = 1 enables a read from the direct register, bypassing the FIFO.
0 X	0 1	1 0 0	0	TLINTQ = 0	Controller interrupt "TILINE interrupt" to the 990 CPU.
			1	TLINTQ = 1	ROM 39 = 1 lights the interrupt LED indicator and enables the interrupt to the 990 processor.
0 X	0 1	1 0 1	0	BUSYQ– = 0	Controller busy flag. ROM 39 = 0,
			1	BUSYQ– = 1	lights the BUSY indicator, and causes the controller to respond to any attempted slave read operation with a simulated controller status word in which the idle/busy bit indicates that the controller is busy.
0 X	0 1	1 1 0	0	FAULTQ– = 0	Controller hardware fault flag.
			1	FAULTQ– = 1	ROM 39 = 0 lights the FAULT indicator.
0 X	0 1	1 1 1	0	DIAGFAULTQ– = 0	Controller diagnostic fault flag.
			1	DIAGFAULTQ– = 1	ROM 39 = 0 lights the fault indicator and serves as a CPE I-bus flag input.

Table 2-15. Special Function 2 (Drive Control) Decoder/Register Outputs

KC Field ROM 10, 11	Function Group Sel. ROM 34, 35	Latch Selection ROM 36,37,38	Data ROM 39	Latch Output	Description
0 X	1 0	0 0 0	0	SPAREOUT1 = 0	Spare bit which is used to generate an
			1	SPAREOUT1 = 1	oscilloscope sync pulse each time the diagnostic self-test performs a disk status update. Used for troubleshooting, in conjunction with scope delayed sweep.
0 X	1 0	0 0 1	0	RESTORE = 0	Restore disk head carriage to
			1	RESTORE = 1	cylinder zero. Also called "return to zero seek (RTZS)". ROM 39 = 1 initiates the restore operation.

Table 2-15. Special Function 2 (Drive Control) Decoder/Register Outputs (Continued)

KC Field ROM 10, 11	Function Group Sel. ROM 34, 35	Latch Selection ROM 36,37,38	Data ROM 39	Latch Output	Description
0 X	1 0	0 1 0	0	EG = 0	Erase gate. Enables erase current during a write operation. ROM 39 = 1 enables the erase gate.
			1	EG = 1	
0 X	1 0	0 1 1	0	WG = 0	Write gate. Enables write current during a write operation. ROM 39 = 1 enables the write gate.
			1	WG = 1	
0 X	1 0	1 0 0	0	RG = 0	Read gate. Enables read data and read clock out of the drive to the controller.
			0	RG = 1	
0 X	1 0	1 0 1	0	SPAREOUT2 = 0	Spare bit
			1	SPAREOUT2 = 1	
0 X	1 0	1 1 0	0	HDSEL = 0	Head select. Selects one of the two read/write heads on a disk drive. ROM 39 = 1 (HDSEL = 1) selects the lower (fixed disk) head. ROM 39 = 0 selects the upper (removable cartridge) head.
			1	HDSEL = 1	
0 X	1 0	1 1 1	0	ADDSTB = 0	Address strobe (also called cylinder strobe). Strobes the address on the ADD001– through ADD256– outputs into the disk drive cylinder address register.
			1	ADDSTB = 1	

Note:

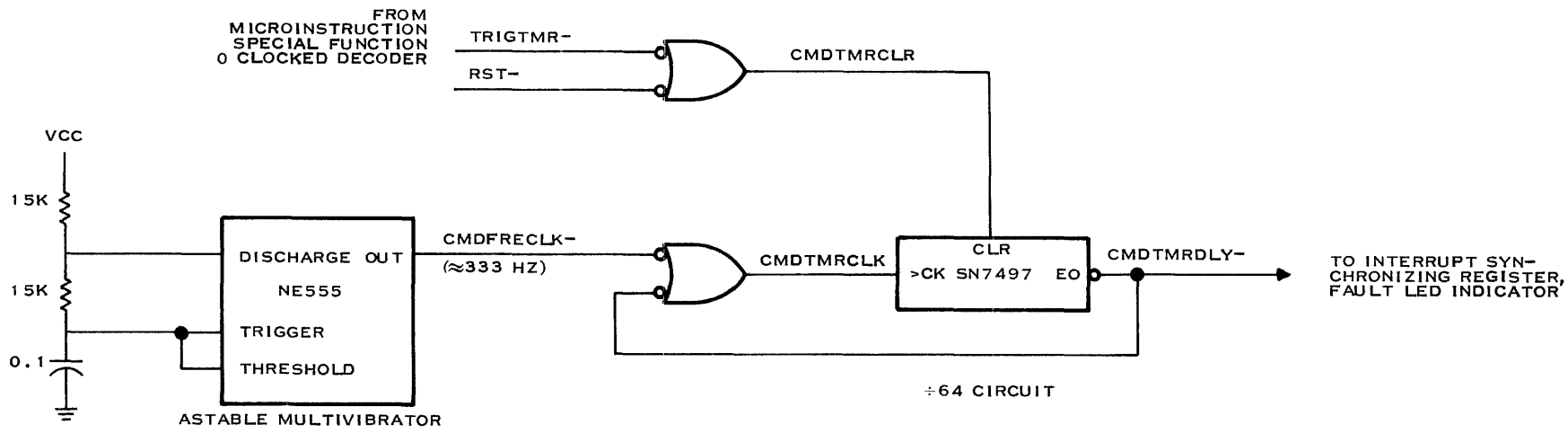
*All the drive control outputs are inverted for transmission to the disk drive. Erase gate, write gate, and address strobe are disabled by a TILINE power reset (TLPRES–).

2.11 COMMAND TIMER

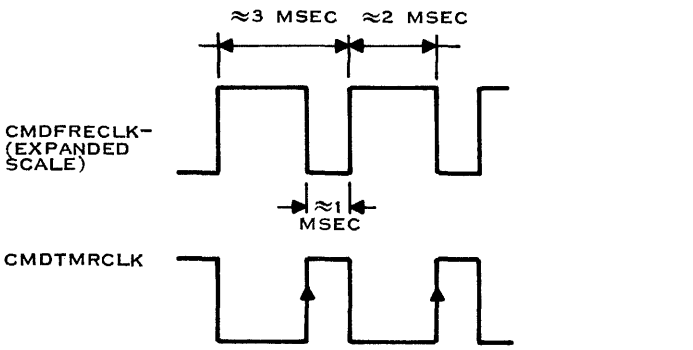
Occasionally, a hard or soft failure will occur in a drive or in a controller, preventing normal completion of an operation. If there is a specific microcode interrupt associated with the condition, such as the write timing or TILINE parity error, the controller traps to an interrupt routine and the controller can execute retries or notify the 990 AU of a hard failure. The command timer provides a catch-all microcode interrupt to detect any condition which prevents completion of an operation within about 190-200 milliseconds. The command timer prevents the controller from hanging up in some error state without at least notifying the controller microprogram that a problem exists.

Figure 2-42 summarizes command timer operations. An NE555 timer is used as an RC-controlled digital oscillator, with an output frequency of approximately 320-340 HZ. The oscillator output clocks an SN7497 binary rate multiplier device, which is used as a ÷ 64 counter. While the controller is cycling in the idle loop, a stream of clear pulses prevents the counter from saturating and generating a command timer delay signal. Each clear pulse (TRIGTMR-) is decoded from special function group 0 of a microinstruction.

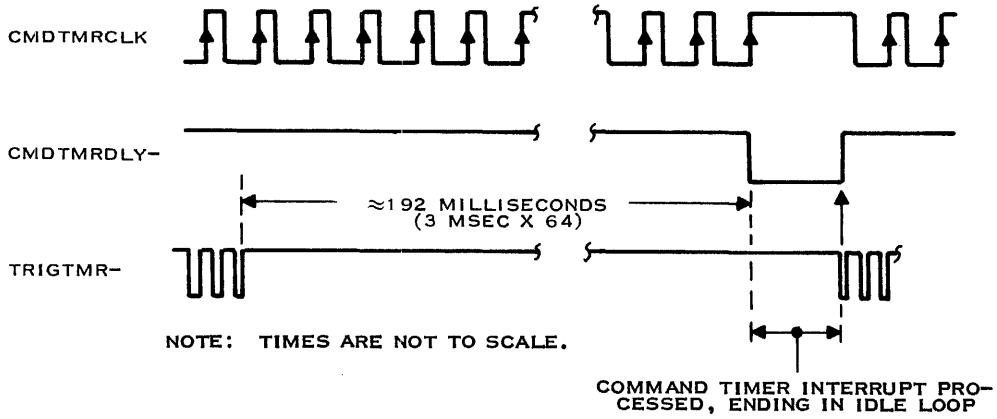
When the controller leaves the idle loop to perform an operation, the stream of clear pulses stops, and the SN7497 counts toward saturation. If the operation by design takes more than about 150 milliseconds, a command timer clear will be included in the operation microcode. When the operation completes, the controller returns to the idle loop, and a stream of clear pulses prevents expiration of the command timer delay.



A. COMMAND TIMER CIRCUIT



B. COMMAND TIMER EXPANDED WAVEFORMS



C. COMMAND TIMER EXPIRATION

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Figure 2-42. Command Timer

Assume that a fault condition hangs up the operation. Approximately 190-200 nanoseconds after the last command timer reset, the counter reaches saturation and CMDTMRDLY- goes active (low). CMDTMRDLY- shuts off the clock input (CMDTMRCLK), to latch up the counter output in the active state. CMTMRDLY- is connected to the input of the interrupt synchronizing latch, and initiates a command timer delay microcode trap. Refer to the instruction access logic for a detailed description of microcode interrupt traps. CMDTMRDLY also lights the FAULT light-emitting diode indicator.

The interrupt trap routine executes, and ends in the idle routine. The idle routine sends command timer reset pulses to the counter. The first TRIGTMRS- pulse clears the CMDTMRDLY- signal, and subsequent pulses retrigger the counter as previously described.

A general reset, initiated by either TLIORES- or TLPRES-, will also clear the command timer.

2.12 DISK INTERFACE

The disk interface logic performs those functions which are directly involved in transmitting data to a disk drive for recording and retrieving data previously recorded on a disk drive. These functions include:

- Selecting the disk drive logical unit for the operation
- Controlling the selected disk drive unit
- Addressing a specific recording area (cylinder, head) on the disk
- Processing and transferring disk unit status and rotational position (sector address, sector mark) information
- Formatting, buffering, and transferring read and write data to and from the disk unit
- Error checking of data and header information read from the disk unit.

Disk interface operations are initiated and controlled by the 512-word ROM microcode program. The group select (ROM34, 35) and special function fields (ROM36-39) of the 40-bit microinstruction are primarily used for disk interface control. The 16-bit CPE array under microinstruction control performs such functions as reading the disk status word from the processor bus, monitoring other status bits on the I-bus, supplying the disk logical unit selection code via the processor bus, and supplying the cylinder address selection code via the processor bus. The CPE array is not in the data path for read or write operations. The write data path goes from the 990 main memory, over the TILINE, the processor bus, through a first-in, first-out (FIFO) buffer and parallel/serial converter in the disk interface, and out to the selected drive. One TILINE master read cycle is required to transfer each 16-bit word from the 990 memory to the disk interface. Each TILINE master cycle is initiated under microinstruction control, and the TILINE address is supplied by the TILINE MSB address register and the address (A) bus outputs of the CPE array.

The read data path goes from the selected disk unit through a serial/parallel converter and FIFO in the disk interface, over the processor bus and into the 990 main memory over the TILINE. A TILINE master write cycle is required to transfer each 16-bit word from the disk interface to the 990 main memory. Again, the master cycle is initiated under microinstruction control, and each TILINE address is supplied by the MSB address register and the CPE address outputs.

Three different clock rates are involved in this transfer. The TILINE interface operates at an asynchronous, variable word rate which is partly determined by activity on the bus. The microinstruction ROM, CPE array and associated processing operate at the microprocessor clock

rate set by MPCK-. This clock may be stopped and restarted in order to communicate over the TILINE. The disk interface operates at a disk read or write clock rate. For disk write operations, this clock is developed by an oscillator in the disk interface, and multiplexed into the data stream written on the disk. For read operations, this clock is recovered and separated by the disk drive electronics and supplied to the disk interface. Any variation in disk rotational speed varies the read clock rate. The 16-word FIFO averages out short-term differences between disk and TILINE data rates. Excessive delay in the TILINE interface, beyond the 16-word capacity of the FIFO, will cause a FIFO timing error (rate error) microcode interrupt during write operations. For read operations, bad status will be reported at the end of the operation. The TILINE interface, however, cannot outrun the disk interface because each TILINE word is transferred by a separate TILINE master cycle operation. The microcode program initiates the master cycle only when the disk interface is ready.

Formatted read and formatted write operations are the most commonly performed disk operations. For a formatted track, each record has a sector identification header which must be read and verified before the data is read or written. The data flow path for the verify sector header operation goes from the disk, through the serial to parallel converter, and into the direct read register (rather than the FIFO). The direct read register contents are transferred over the processor bus (P-bus) to the CPE M-bus inputs. The actual values read from the disk header are compared to expected header values. If these values compare, the read or write operation proceeds, using the data paths previously described.

The write format operation writes the sector headers on a disk, and prefills all the sectors on a given track with the same data word. Two data paths through the disk I/F are used during the course of a write format operation. A write format command is sent to the DS10 controller in the form of eight successive slave write operations, as described in Section 1. The parameters supplied to the controller include a TILINE address, a record word count, number of sectors per record, and the header parameters for all the records on the specified track. At the start of the write format operation, the CPEs request the data word which is stored at the TILINE address supplied by W5 and W6. The data word is read from 990 memory, gated onto the processor bus, and temporarily stored in the direct read register. At a later point in the sequence, this word is transferred over the processor bus and into a CPE internal register. This TILINE-processor bus-direct read register-CPE data path is exercised only once, at the beginning of the write format operation. Each time a new record comes under the read/write head, the CPE transmits three sector header words via the processor bus, FIFO, parallel/serial converter and serial data path to the disk. The CRC generator appends a 16-bit cyclic redundancy check character to the header data transmission. After the gap time has expired, the CPE starts filling the data area of the sector with repeated copies of the one specified word, which is stored in the CPE. When the record word count expires, a CRC character is written. The operation repeats at each sector mark which corresponds to the beginning of a record until the entire track is formatted.

Figure 2-43 is a detailed functional block diagram of the disk interface logic. Some portions of the block diagram, such as disk selection and status monitoring, are very straightforward. These sections of logic perform simple functions and operate in only one manner. Other logic, such as the serial/parallel shift register and FIFO buffer are shared between read and write operations with differing signal flow for these operations. The multiple possible data routes in these logic areas make the block diagram representation more complex. The simplified data flow diagrams, figures 2-5 through 2-8, are helpful in keeping track of the data flow.

2.12.1 DISK INTERFACE LOGIC. Each section of logic shown on the disk interface block diagram is described in subsequent paragraphs.

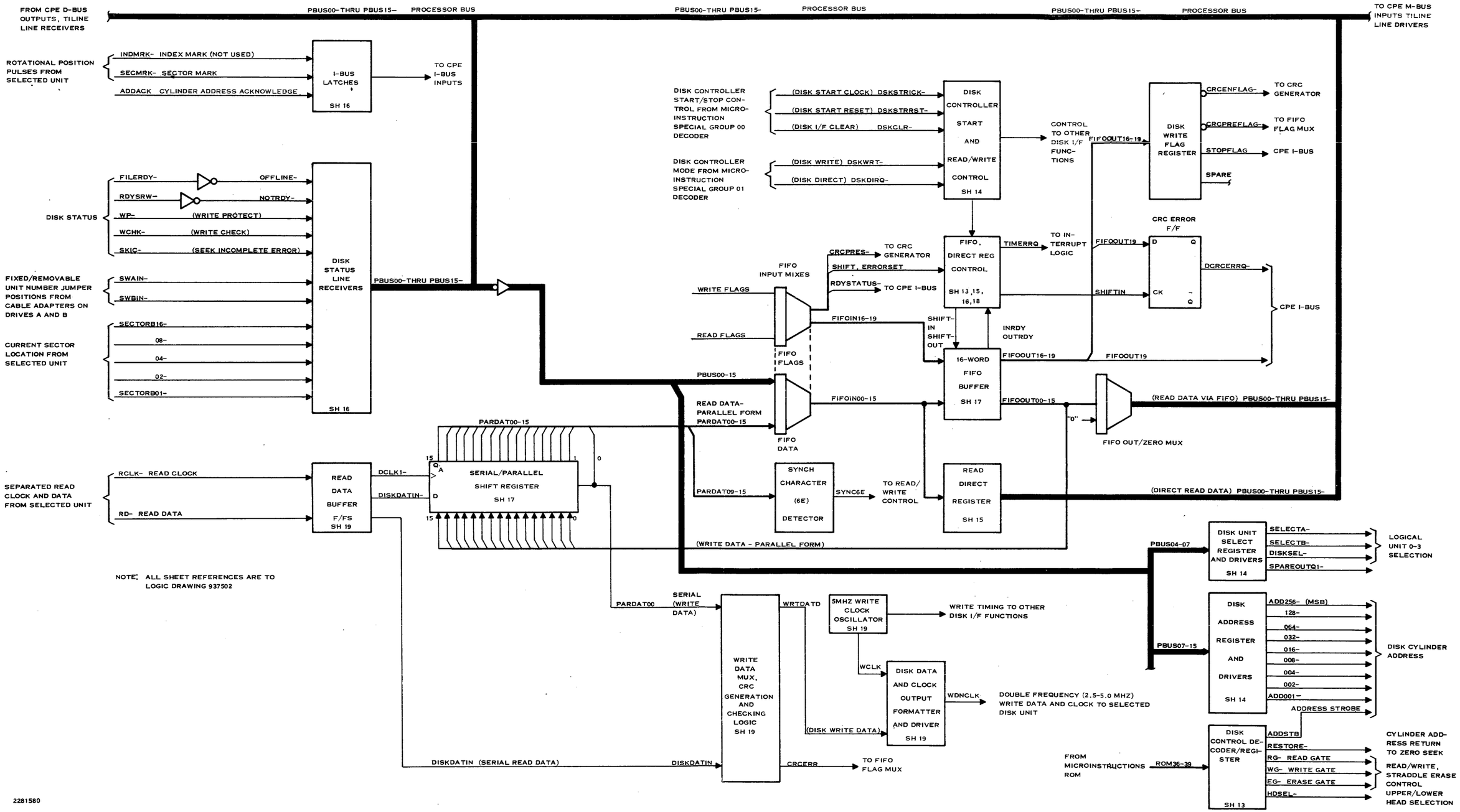


Figure 2-43. Disk Interface Block Diagram

Table 2-16 lists all the signals interchanged between the disk controller and the disk drive unit(s). These are the signals which the disk interface logic must either control or monitor during disk operations. A brief description of each signal is included in the table. The reader should be familiar with the contents of the table before continuing with this description. Appendix F contains detailed pin assignments for the controller-disk drive I/O connectors, P3 and P4.

2.12.1.1 Disk Unit Select, Disk (Cylinder) Address and Disk Control Decoder Registers. The controller to disk drive output signals, except the write data and clock (WDNCLK-) signal, are isolated in figure 2-44. The disk unit select register and disk address register are shown on sheet 14 of logic drawing 937502 (PWB) or 2262102 (fine line), and the disk control decoder/register is shown on sheet 13.

Disk unit selection is a necessary prerequisite for any operation which involves the drives. A disk unit must be selected before it can accept any data or control inputs (except the select inputs). It must also be selected before it can supply data or status outputs to the disk controller.

Table 2-16. Disk I/F and Disk Drive Interface Signals

Signal Name in Controller	Description
Controller to Disk Signals:	(Active in the low voltage state unless otherwise specified.)
ADD001- ADD002- ADD004- ADD256-	Cylinder address. Valid when cylinder address strobe, ADDSTB, is high. A read or write operation need not load a new cylinder address unless the heads must seek to a new track.
ADDSTB-	Cylinder address strobe. Loads cylinder address into disk drive electronics when low. For read or write seeks, ADDSTB remains active until Address Acknowledge (ADDAK-) is issued. For Restore-, strobe remains active for at least one microsecond.
SELECTA-	Select disk drive A. When low, selects the dual disk drive which is designated "A". The select line must be active (low) to allow the drive unit to accept data or any other control signals, and to generate any control status signals except seek error and unit ready. This line selects a drive which contains two independent logical units. The select line and disk select signal are both required to uniquely specify logical unit 0 or 1.
SELECTB-	Select dial disk drive B. When low, selects the disk drive which is designated "B". The select line and the disk select signal are both required to uniquely specify logical unit 2 or 3. See SELECTA-, above.
DISKSEL-	Disk select. Selects one of the two platters within a disk drive. When low, DISKSEL- selects the fixed disk, when high selects the removable disk. The controller must check the position of the fixed/removable logical unit reversing jumper (SWAIN- or SWBIN-) before setting the polarity of DISKSEL-.

Table 2-16. Disk I/F and Disk Drive Interface Signals (Continued)

Signal Name in Controller	Description
HDSEL-	Head Select. Selects the read/write head on the upper surface (HDSEL- low) or the lower surface (HDSEL- high) of the selected fixed or removable disk platter. HDSEL- is stable for at least 10 microseconds before the leading edge of a write gate, and remains stable for the duration of a read or write operation.
RG-	Read gate. Enables read data and clock through the disk drive electronics to the controller. Leading edge of read gate enables phase-lock circuitry in disk drive electronics clock/data separator.
WG-	Write gate. Enables write current during a write operation.
EG-	Erase gate. Enables erase current during a write operation, so the erase heads can "shear" flux splatter at the outer track edges (straddle erase).
WDNCLK-	Double-frequency encoded write data and clock to the disk unit. Minimum pulse width is 100 nanoseconds, with a rise/fall time less than 50 nanoseconds.
RESTORE-	Restore to Track Zero, also known as Return to Zero Seek (RTZS-). Causes the head carriage to advance to the forward limit of travel and then return to the home (track 000) position. Also clears disk cylinder address registers and counters, and clears disk unit fault latches. Essentially a master clear to the selected disk drive. Cylinder Address Strobe (ADDSTB-) must be low for the disk to accept the RESTORE command.
Disk to Controller Signals:	
ADDAK-	Address Acknowledge. Acknowledges acceptance and validity of cylinder address loaded into the disk drive electronics. Addresses greater than 407 are considered invalid.
FILERDY-	Disk File Ready. Active (low) if the disk cartridge is installed, disk spindle is up to speed, heads are loaded, dc voltages are within tolerance, unit selected, no fault latches set, terminator and terminator power present. Inverted within the disk controller as OFFLINE-.
RDYSRW-	Ready to start Read/Write (also called "on cylinder"). Indicates that the head carriage has reached the specified cylinder address, and the heads are stable. Also incorporates all file ready conditions. Inverted within the disk controller as NOTRDY-.
SKIC-	Seek Incomplete (also called seek error, SKER). Indicates that the disk drive failed to properly seek to the desired cylinder address. This condition may be cleared by a Restore operation.

Table 2-16. Disk I/F and Disk Drive Interface Signals (Continued)

Signal Name in Controller	Description
INDMRK-	Index Mark. A reference pulse which occurs once every disk revolution when sector 0 rotates under the R/W heads. The controller has the logic to monitor INDMRK-, but the controller microprogram makes no use of it. The controller depends instead upon the sector address supplied by the selected disk unit. Generated separately for the fixed and removable disks.
SECMRK-	Sector Mark. A rotational position pulse (50 microseconds) which identifies the start of each disk sector. The leading edge is used as the timing reference for starting read or write operations. Generated separately for the fixed and removable disks.
SECTORB01- SECTORB02- SECTORB04- SECTORB08- SECTORB16- SECTORB32-	Sector Address. The disk drive electronics has a sector counter which uses the index and sector marks to keep track of the current rotational position of the selected disk. The disk controller compares this current sector address to the desired sector address to determine whether the desired sector is under the read/write heads. The sector address is updated at the end of a sector, about four microseconds before the next sector mark. It is stable when the sector mark occurs, and remains stable until four microseconds before the next sector mark.
RD-	Read Data. A clock/data separator in the disk drive electronics uses phase-lock techniques to separate the double-frequency recorded clock and data stream into separate clock and data outputs to the controller. Nominal pulse width is 100 nanoseconds, with variations allowable from 50-150 nanoseconds. Leading edge is the reference.
RCLK-	Read Clock. Clock recovered from disk which is used as basic disk I/F clock for read operations. Recovered from recorded double-frequency clock data stream by phase lock techniques. Nominal pulse width is 100 nanoseconds, with allowable variations from 50-150 nanoseconds. Leading (falling) edge is the timing reference.
WP-	Write Protect. Indicates that data may not be written onto the the selected disk because the associated WRITE PROTECT switch on the disk drive control panel is on.
WCHK-	Write Check (also called Fault). Indicates that the disk drive electronics has detected a fault condition and inhibited the write and erase currents. Fault conditions which may be cleared by a restore signal, if temporary, include: 1. More than one head selected 2. Read and write gates simultaneously active (low) 3. Read and erase gates simultaneously active (low) 4. Erase gate active without write gate for more than 20 microseconds.

Table 2-16. Disk I/F and Disk Drive Interface Signals (Continued)

Signal Name in Controller	Description
	5. Write or erase gate on when not on cylinder (RDYSRW- high) 6. Low dc voltages in disk drive 7. Emergency retract condition, such as motor under speed.
Cable Adapter to Controller:	
SWAIN-	Position of fixed/removable disk logical unit number reversing jumper for 1st dual disk drive (disk drive A). SWAIN- high means that the reversing jumper is not installed, so that the removable disk cartridge is logical unit 1 and the fixed disk is logical unit 0. This is the normal situation. SWAIN- low means that the reversing jumper is installed, so that the removable disk is changed to logical unit 0 and the fixed disk is changed to logical unit 1.
SWBIN-	Position of fixed/removable disk logical unit number reversing jumper for the second dual disk drive (disk drive B). SWBIN- high means that the reversing jumper is not installed, so that the removable disk cartridge is logical unit 3 and the fixed disk is logical unit 2. This is the normal situation. SWBIN- low means that the reversing jumper is installed on the cable adapter, so that the removable disk is changed to logical unit 2 and the fixed disk is changed to logical unit 3. The disk controller senses the state of SWAIN- or SWBIN- before setting the DISKSEL- output level. The controller microprogram forces the DISKSEL- polarity to the correct level to select the disk specified in the logical unit select field of control word R6. The reversing jumpers are physically located on the cable adapter board.

A DS10 disk drive has two disk platters (one fixed, one removable cartridge). These disk platters are treated by the disk controller as though they were two entirely distinct disk units, each with its own logical unit number. This is true even though both platters share basically the same set of read/write/control electronics, and rotate on the same spindle. A single read/write head carriage assembly moves the four read/write/erase heads to the proper disk cylinder. One consequence of this is that independent, overlapped seek operations may not be performed on DS10 drives. With two DS10 disk drives daisy-chained to one controller, there are four distinct logical unit numbers available for selection. It would be confusing to assign numbers to drives and to logical units, so this manual will refer to the first disk drive on the daisy chain as drive A. Drive A contains logical units 0 and 1. The second disk drive, if any, is called drive B, and contains logical units 2 and 3. The standard configuration (in the absence of optional reversing jumpers) is:

Drive A	Drive B
Fixed disk — logical unit 0	Fixed disk — logical unit 2
Removable disk — logical unit 1	Removable disk — logical Uuit 3

The reversing jumpers are mounted on printed circuit board cable adapters mated to the drive input/output connectors. The controller senses the jumper positions to determine the appropriate

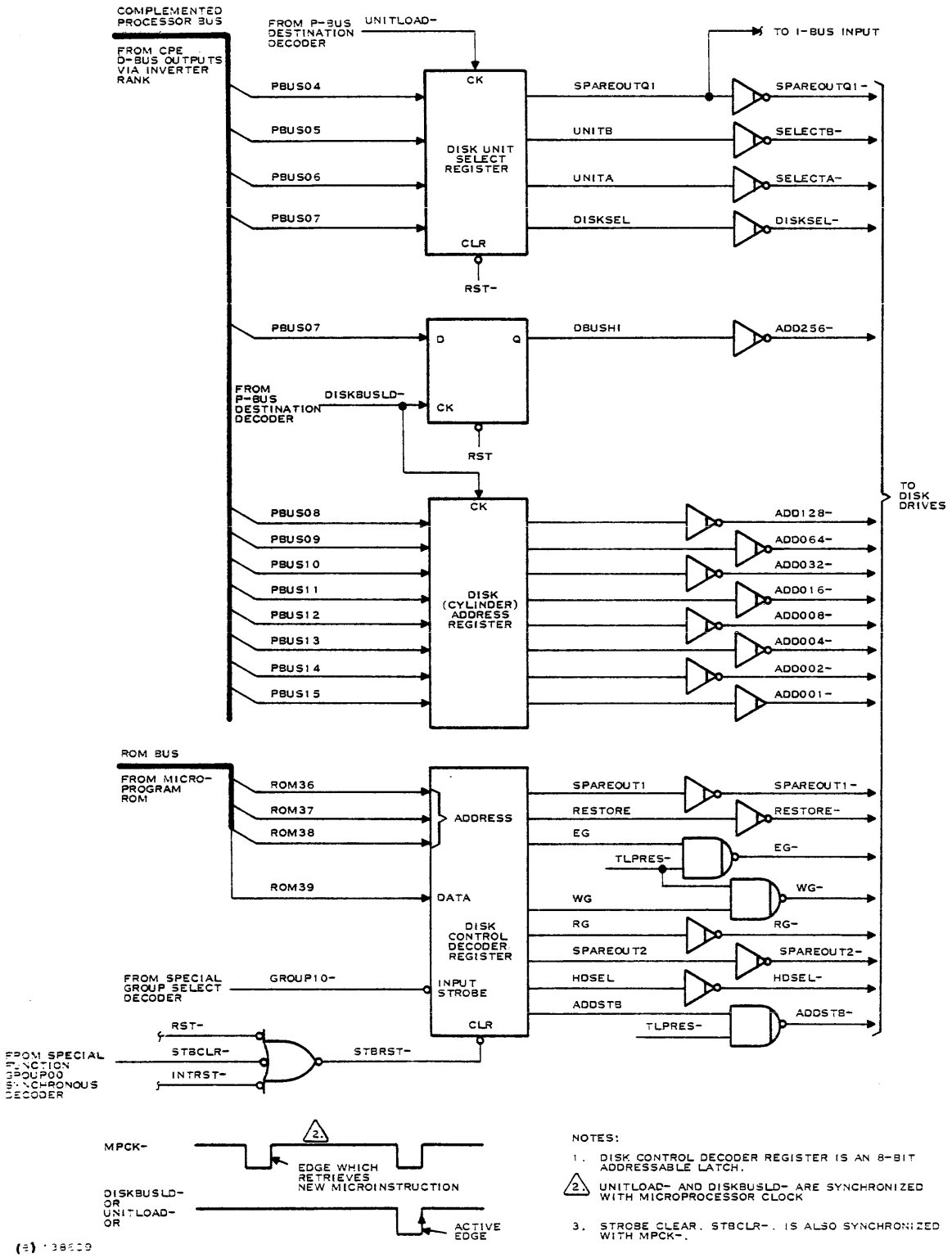


Figure 2-44. Disk Unit Select, Disk (Cylinder) Address Select, and Disk Control Decoder/Register Logic

disk unit selection code. This code is placed on the processor bus by the left byte CPEs and strobed into the disk unit select register by UNITLOAD-. UNITLOAD-, which is a pulse synchronized to microprocessor clock, is decoded from the P-bus destination field (ROM20,21) of the active microinstruction.

Open-collector driver/inverters transmit the selection code to the disk drive(s). SELECTA-, when low, selects the first disk drive, and SELECTB-, when low, selects the second disk drive. DISKSEL- is the signal which determines whether the fixed disk platter or the removable disk cartridge is selected. DISKSEL- low selects the fixed disk platter, and DISKSEL- high selects the removable disk cartridge. Table 2-17 summarizes the logical unit selection outputs of the disk controller. Upper/lower head selection is described with the disk control decoder/register outputs.

Table 2-17. Logical Unit Selection

		Without Reversing Jumpers				With Both Reversing Jumpers			
Logical Unit	Controller Unit Select Code Input (Positional Code) (R6, bits 4-7)	Controller Select Code Outputs SELECTA–	SELECTB–	DISKSEL–	Platter Type	Controller Select Code Outputs SELECTA–	SELECTB–	DISKSEL–	Platter Type
0	1 0 0 0	L	H	H	Fixed	L	H	L	Cartridge
1	0 1 0 0	L	H	L	Cartridge	L	H	H	Fixed
2	0 0 1 0	H	L	H	Fixed	H	L	L	Cartridge
3	0 0 0 1	H	L	L	Cartridge	H	L	H	Fixed

The contents of the disk address register determine the physical position of the head carriage. The head carriage is at cylinder 0 of both platters when it is at the read/write track farthest from the spindle. The carriage is at cylinder 407 when it is closest to the spindle (farthest into the disk). The head carriage servo uses a current position register to compare with the specified address to control the direction and rate of head carriage movement. The operation is called seeking or track seeking.

The cylinder address is supplied to the controller in one of the eight initial control/parameter words. As part of the read or write sequence, the CPEs supply the cylinder address over the processor bus, and DISKBUSLD- strobes the address into the nine-bit disk address register. The DISKBUSLD pulse is decoded from the processor bus destination select field (ROM20,21) of the microinstruction and synchronized with MPCK-. The nine-bit cylinder address is transmitted to the disk drive as ADD001-, ADD002-, ADD004-, through ADD256-. This address is actually loaded into the disk drive electronics by an address strobe developed by the disk control decoder/register.

The disk unit select register and the disk address register both accept CPE output data from the processor bus. The disk control register/decoder is an eight-bit addressable latch which is controlled by special group 2 of the controller microinstructions. Each control signal output is set up by a separate microinstruction. ROM36-38 addresses one of the eight internal latches, and ROM39 either sets or resets the specified latch, as described with the microinstruction format. The input strobe, GROUIP10-, is supplied by ROM34,35 through the special group select decoder. All eight register stages are simultaneously cleared by an STBRST- (strobe reset) signal. The strobe reset may be part of a general controller reset, an interrupt reset, or a specific strobe clear (STBCLR-) command from a controller microinstruction. The strobe reset allows rapid clearing of the drive control signals to inactive states. For example, if a TILINE power reset (TLPRES-) occurs, it is undesirable to leave erase current and write current enabled. TLPRES- directly disables the output drivers, and the general reset clears out the latch contents.

Outputs of the disk control decoder/register drivers are: SPAREOUT1-, RESTORE-, EG-, WG-, RG-, SPAREOUT2-, HDSEL- and ADDSTB-. ADDSTB-, the cylinder address strobe, enables the disk drive to accept a new cylinder address from the ADD001- through ADD256- lines. HDSEL-, the head select signal selects either the upper (HDSEL- low) or the lower (HDSEL- high) surface of the disk. RG-, the read gate, allows the disk drive electronics to synchronize the phase-locked clock/data separator to the read data and clock data stream read from the disk.

The read gate is enabled in advance of the actual data read operation, to allow synchronization of the phase-locked clock-data separator. The write gate and erase gate (WG- and EG-) are both enabled during a write operation. The write gate allows write current to flow, so that data may be written on the disk. The write gate is actually enabled during the gap before a record. All zeros (clock without data) are written into the gap. On read, the clock pulses recorded in the gap are used to synchronize the clock/data separator circuits. The erase gate allows current to flow in the straddle erase circuits. Straddle erase head gaps follow the write head gap and shear the flux splatter on both track edges.

The RESTORE- signal initiates a disk drive return to zero seek (RTZS) operation. This operation moves the head carriage to the fully extended position, return it to the track 0 position, and performs a general reset of the disk drive address control and fault detection logic.

2.12.1.2 Disk Status Inputs to Processor Bus and I-bus. Figure 2-45 is a block diagram which shows the disk status inputs to the controller disk interface logic. All disk status signals are sampled by the CPEs. There are two basic paths for the disk status signals to reach the CPEs: the CPE I-bus or the processor bus.

The I-bus is a group of 16 individual signals which are connected to the I-bus inputs of the 16-bit CPE array. Each of these signals comes from a single source and has a single destination. Many of the I-bus lines are used to monitor internal progress of disk controller operations. For example, a special stop flag is written into the FIFO after the last word in a disk write buffer. The controller microprogram monitors this flag bit at the FIFO output (STOPFLAG) to determine if the disk write buffer is complete. Typically, this monitoring is done with a single microinstruction which activates the left byte or the right byte CPEs, stops CPE clock, and forces the CPEs to AND eight-I-bus input lines with an 8-bit immediate operand on the K-bus. The result of the AND operation steers a conditional branch. The branch or nonbranch is determined by the masked I-bus input signal. The single-byte limitation on I-bus monitoring is due to the availability of only eight bits of mask information in the microinstruction immediate operand field.

The disk rotational position pulses, sector mark and index mark, are connected to I-bus inputs, as are the disk address acknowledge signal and two spare signals. The disk controller microprogram does not make use of the index mark, but the monitoring capability is available. Sector and index marks are generated when a sector slot or index slot rotates past a fixed transducer in the disk drive. The fixed disk slot transducer is hardmounted to the spindle. The disk cartridge contains slots in a sector rim built into the cartridge. An index mark identifies the beginning of sector 0, and a sector mark identifies the beginning of each sector.

Referring to the diagram, the sector and index mark flip-flops are cleared by the clear sector/index pulse (CLRSECIDX-) pulse decoded from special group 0 of the microinstruction. When a sector slot on the selected platter comes under the transducer, the low SECMRK- pulse sets the sector F/F. The F/F output, SECTORMRK-, is synchronized with microprocessor clock in the I-bus latches, and SECTORMARQ- at the CPE I-bus input goes active (low). The controller microprogram clears the sector and index F/Fs after masking the left byte I-bus inputs with 80_{16} to test for the sector mark. Note that the CPE devices use a logic convention of 1 = 0 volts and 0 = +2.8 volts, so any low input is interpreted as a data 1, and any high input is interpreted as a data 0.

Figure 2-46 shows typical microprogram flow chart segments for I-bus bit testing. The functions monitored by the left byte CPEs are: sector mark, ready status, disk start, direct register ready,

address acknowledge, diagnostic fault and test mode. To test for the presence of one of these bits, the left byte CPEs are commanded to AND the I-bus inputs bit-by-bit with an 8-bit immediate operand from the microinstruction. The CPE clock is stopped, so that no CPE internal register contents are modified. The left byte carry output is used as a test bit to determine if the result of the AND operation is zero (CO = 0) or nonzero (CO = 1).

The carry output is latched in the test bit F/F. The test bit controls a conditional branch, causing the microprogram to continue to look for the status bit or to advance to a new segment. The figure shows the immediate operands (in hexadecimal form) which are used as selection masks for each of the I-bus input signals. These immediate operands are supplied by ROM32-39, the IM field, to the K-bus inputs of the CPE array. The polarity of the I-bus input signal determines which output of the decision block represents "condition detected." Notice that the entire bit test operation is complete within one microinstruction, and does not require access to the processor bus.

In addition to monitoring selected disk status bits on the I-bus, the microprogram can gate a 16-bit disk status word over the processor bus to the CPE M-bus inputs. The bus source field of the microinstruction (ROM13-15 = 110) enables the status line receiver outputs onto the processor bus. The first 11 bits of the disk status word are individual, independent signals which may be masked and tested as shown in figure 2-47. The bit testing operation is very similar to the I-bus testing described in the preceding paragraphs. The last 5 bits of the disk status word form the current sector address. This sector address becomes valid approximately four microseconds before the sector mark, and remains valid until approximately four microseconds before the next sector mark. If the disk controller is commanded to perform a read or write operation starting at sector 6, it starts sampling the I-bus for the sector mark. At each sector mark, the controller checks the disk status word looking for a sector address of 6. When the addresses compare, the read or write sequence proceeds to completion.

SWAIN- and SWBIN- identify the presence or absence of the fixed/reversible disk logical unit reversing jumpers. SWAIN- is pulled high (on the controller) unless a grounding jumper is installed between J1 (gnd) and J3 of the cable adapter at drive A.

2.12.1.3 Disk I/F Start and Read/Write Control Logic. Figure 2-48 is a simplified version of the disk I/F start and R/W control logic (drawing 937502, PWB or 2262102, fine line). This logic initiates read or write transfer operations when commanded by the special function field of the controller microinstruction.

A write or read data transfer is specified by the DSKWRTQ (disk write latched) output of the special group 1 decoder/register. The state of the DSKWRTQ signal is set up before the transfer is initiated, and, since it is latched, remains at that state until specifically changed by a microinstruction.

DSKWRTQ is high to specify a write data transfer. DSKWRTQ high places a constant (STRTREAD-) on the read F/F and a constant preset on the sync character detection F/F. DSKWRTQ high partially enables the input to the write F/F.

DSKWRTQ is low for a read data transfer, and disables the WRITEQD input to the write F/F, while allowing the sync F/F and read F/F to operate normally.

Remember that a write data operation (R6, bits 5-7 = 011) involves reading the sector header before writing the data. Therefore, the state of DSKWRTQ will be low while the sector header is verified, and will switch high during the write header gap.

The microprogram commands the disk interface logic to start with a DSKSTRTCK- (disk start transfer clock) pulse decoded from special group 0 of the microinstruction. The DSKSTRTCK- pulse is synchronized with the microprocessor clock pulse, MPCK-. The trailing (rising) edge of

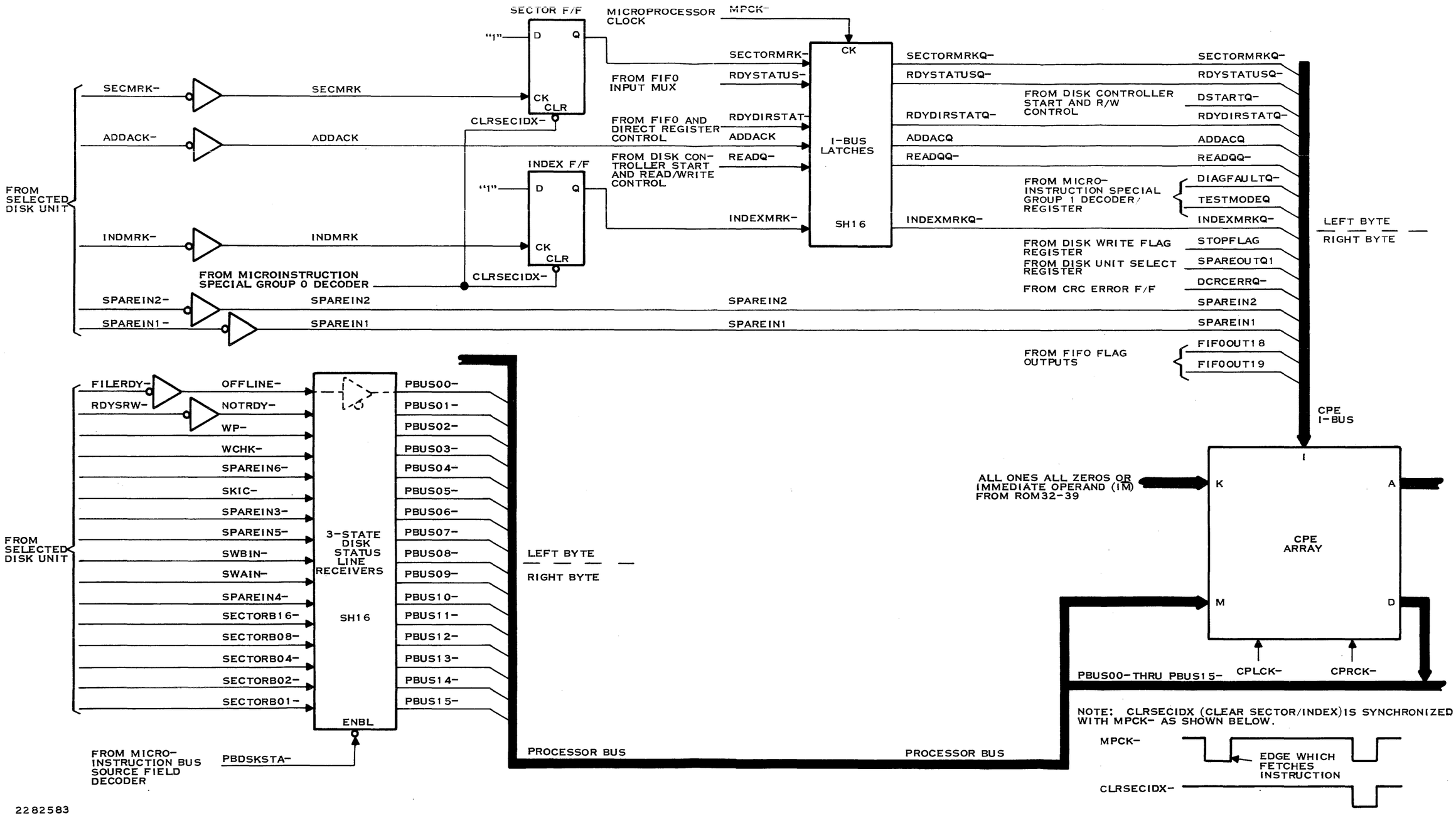
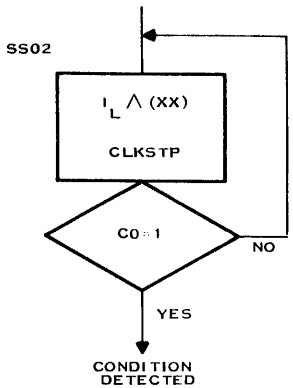
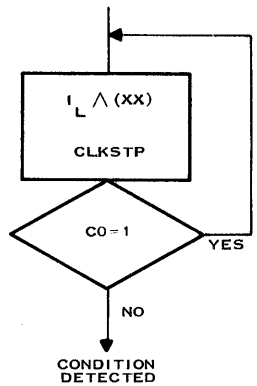


Figure 2-45. Disk Status Inputs to I-Bus and Processor Bus

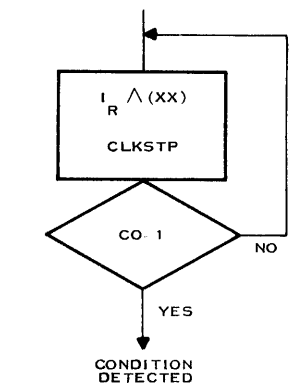


A. ACTIVE LOW INPUT SIGNAL (XYXY-), LEFT BYTE

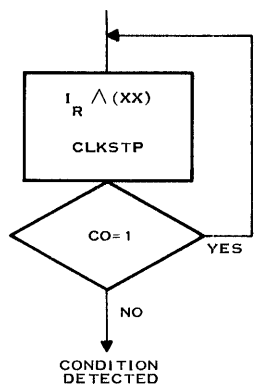


B. ACTIVE HIGH INPUT SIGNAL (XYXY), LEFT BYTE

FUNCTION	SIGNAL NAME	LEFT BYTE MASK	CO FOR CONDITION PRESENT
SECTOR MARK	SECTORMRKQ-	XX=80 $_{16}$	YES
READY STATUS	RDYSTATUSQ-	40 $_{16}$	YES
DISK START	DSTARTQ-	20 $_{16}$	YES
READY DIRECT	RDYDIRSTATQ-	10 $_{16}$	YES
ADDRESS ACKNOWLEDGE	ADDAKQ	08 $_{16}$	NO
READ	READQQ-	04 $_{16}$	YES
DIAGNOSTIC FAULT	DIAGFAULTQ-	02 $_{16}$	YES
TEST MODE	TESTMODEQ	01 $_{16}$	NO



C. ACTIVE LOW INPUT SIGNAL (XYXY-), RIGHT BYTE



D. ACTIVE HIGH INPUT SIGNAL (XYXY), RIGHT BYTE

FUNCTION	SIGNAL NAME	RIGHT BYTE MASK	CO FOR CONDITION PRESENT
INDEX MARK	INDEXMRKQ-	XX=80 $_{16}$	YES
STOP FLAG	STOPFLAG	40 $_{16}$	NO
SPAREOUTQ1	SPAREOUTQ1	20 $_{16}$	NO
DELAYED CRC ERROR	DCRCERRQ-	10 $_{16}$	YES
SPARE IN 2	SPAREIN2	08 $_{16}$	NO
SPARE IN 1	SPAREIN1	04 $_{16}$	NO
FIF0 18 OUT	FIF0OUT18	02 $_{16}$	NO
FIF0 OUT 19	FIF0OUT19	01 $_{16}$	NO

NOTES: $\wedge$ = LOGICAL AND

(XX) = HEXADECIMAL CONSTANT

CO = TEST BIT F/F OUTPUT, SUPPLIED BY CARRY OUTPUT OR RIGHT SHIFT OUTPUT FROM CPE ARRAY. FOR NON-ARITHMETIC OPERATIONS, THE CARRY OUTPUT IS OFTEN USED TO INDICATE THAT THE 8-BIT OR 16-BIT RESULT OF A LOGICAL OPERATION IS NON-ZERO.

CLKSTP = CPE CLOCK STOP (ROM00). INHIBITING THE CLOCK ALLOWS THE CPE'S TO PERFORM NON-DESTRUCTIVE TESTS ON DATA VALUES.

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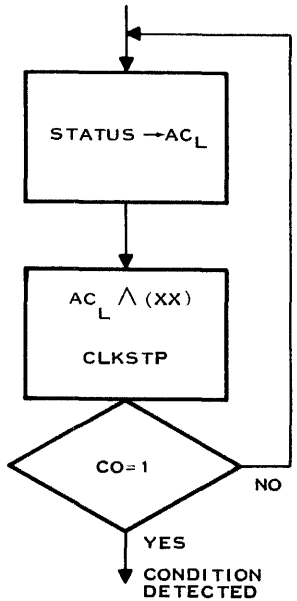
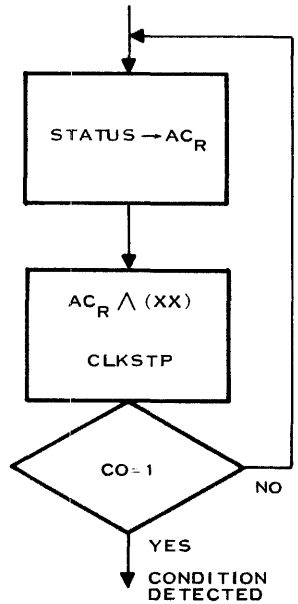
Figure 2-46. Bit Testing — I-Bus





NOTES:

AC	= CPE ACCUMULATOR
L	= LEFT BYTE (SUBSCRIPT)
R	= RIGHT BYTE (SUBSCRIPT)
∧	= LOGICAL BIT-BY-BIT AND
(XX)	= HEXADECIMAL CONSTANT -8 BITS
CLKSTP	= CPE CLOCK STOP- INHIBITS CPE CLOCK INPUT SO NO REGISTER CONTENTS ARE CHANGED. DOES NOT AFFECT MAIN MICROPROCESSOR CLOCK.
CO	= CARRY OUTPUT USED IN NON-ARITHMETIC OPERATIONS TO TEST ZERO OR NON-ZERO CONTENTS OF A REGISTER.

DISK STATUS WORD, LEFT BYTE

FUNCTION	SIGNAL NAME	MASK	CO FOR CONDITION PRESENT
DISK OFF LINE	OFFLINE-	XX=80$_{16}$	YES
NOT READY	NOTRDY-	40$_{16}$	YES
WRITE PROTECT	WP-	20$_{16}$	YES
WRITE CHECK	WCHK-	10$_{16}$	YES
SPARE	SPAREIN6-	08$_{16}$	YES
SEEK INCOMPLETE	SKIC-	04$_{16}$	YES
SPARE	SPAREIN3-	02$_{16}$	YES
SPARE	SPAREIN5-	01$_{16}$	YES

DISK STATUS WORD, RIGHT BYTE

FUNCTION	SIGNAL NAME	MASK	CO FOR CONDITION PRESENT
REVERSING JUMPER B INSTALLED	SWBIN-	XX=80$_{16}$	YES
REVERSING JUMPER A INSTALLED	SWAIN-	40$_{16}$	YES
SPARE	SPAREIN4-	20$_{16}$	YES
SECTOR ADDRESS 2^4	SECTORB16-	10$_{16}$	YES
SECTOR ADDRESS 2^3	SECTORB08-	08$_{16}$	YES
SECTOR ADDRESS 2^2	SECTORB04-	04$_{16}$	YES
SECTOR ADDRESS 2^1	SECTORB02-	02$_{16}$	YES
SECTOR ADDRESS 2^0	SECTORB01-	01$_{16}$	YES

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Figure 2-47. Bit Testing — Disk Status Word

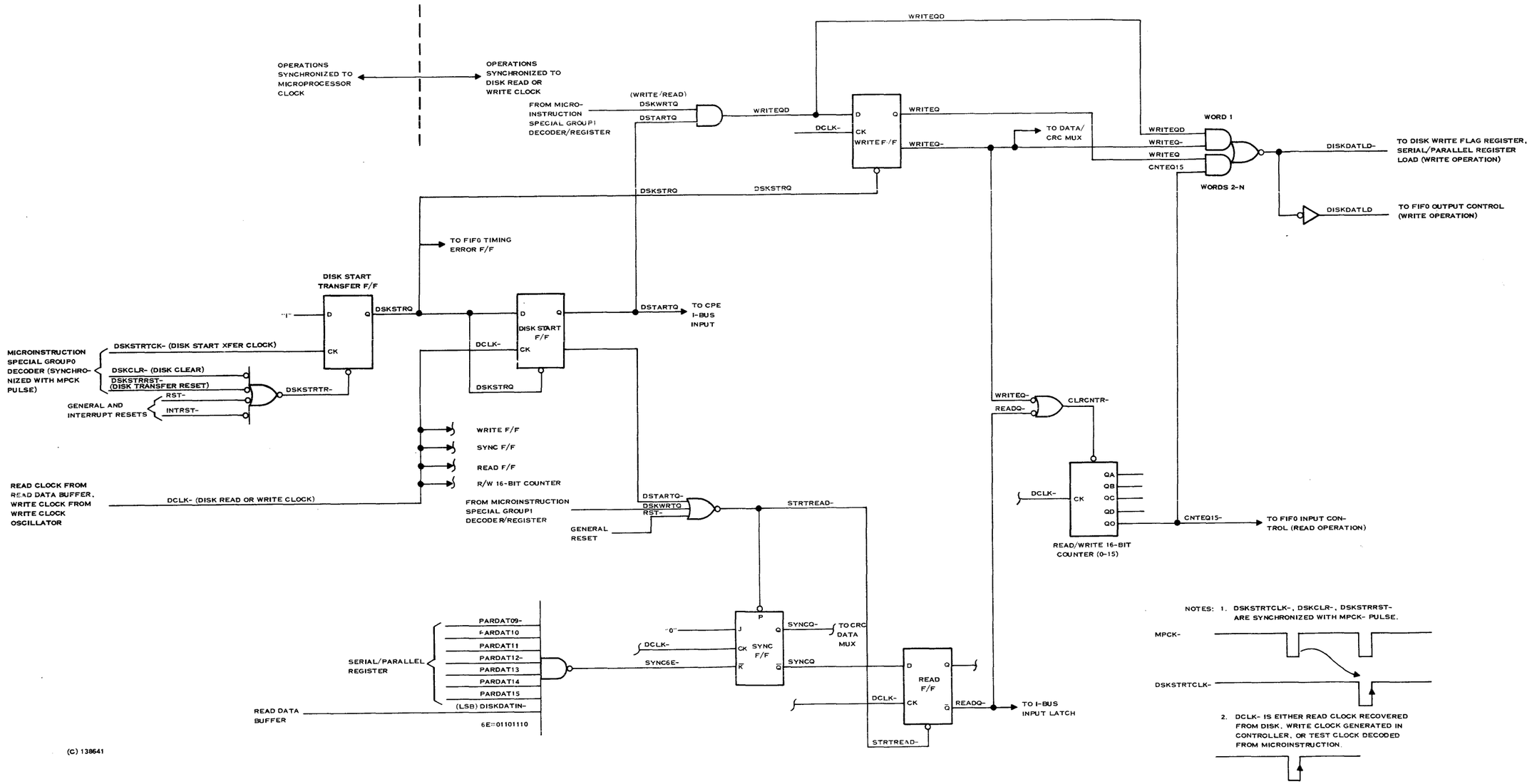


Figure 2-48. Simplified Disk I/F Start and Read/ Write Control Logic

DSKSTRTCK- clocks the disk start transfer F/F, which supplies DSKSTRQ. DSKSTRQ releases the constant reset on the write F/F and supplies the D input to the disk start F/F. Nothing happens until the first disk clock pulse, DCLK-.

DCLK- is read from the disk (for read operations) or supplied by the controller's on-board write clock oscillator, depending on the state of DSKWRTQ.

The first DCLK- pulse sets the disk start F/F, resynchronizing operations to disk clock. The disk start F/F output, DSTARTQ, notifies the CPEs via the I-bus that the commanded operation has started and partially enables the read, sync and write F/F inputs.

For a write transfer, the previously enabled DSKWRTQ and the DSTARTQ signal load the first write data word from the FIFO into the parallel/serial shift register (DISKDATLD-). The write F/F sets on the second disk clock pulse. The WRITEQ output removes the constant clear (CLRCNTR-) from the read/write 16-bit counter and allows it to tally disk clock pulses starting with the third one. Each disk clock pulse corresponds to one bit shifted out at the parallel/serial shift register and transmitted to the selected disk unit. When the counter saturates (CNTEQ15 goes high), it is time to load another 16-bit from the FIFO into the parallel/serial shift register (DISKDATLD-).

For a read transfer, the low DSKWRTQ signal and DSTARTQ allow the sync character to start monitoring for the 01101110 ($6E_{16}$) pattern which precedes either the header or the data. The sync detector gate monitors the parallel outputs of the serial/parallel shift register until it recognizes a $6E_{16}$ pattern. The SYNC6E- signal clears the sync pulse F/F on the next disk clock pulse, indication that a sync pattern has occurred.

The Sync F/F outputs, SYNCQ- and SYNCQ, enable the CRC generator/checker to start monitoring downstream data and set the read F/F on the next disk clock pulse. READQ- notifies the I-bus of the controller operation and enables the read/write counter to monitor the number of received bits. The CNTEQ15- signal loads the FIFO input when a 16-bit word is available on the parallel outputs of the serial/parallel converter.

The disk operation may be terminated by a disk start transfer reset (DSKSTRRST-) or a disk clear (DSKCLR-) microinstruction, by a general reset, or by an interrupt reset. Any of these inputs forces DSKSTRTR- low, which unconditionally forces the logic to a reset state.

2.12.1.4 First In, First Out (FIFO) Buffer. A FIFO buffer is a special memory device which is commonly used to transfer data between devices with differing clock rates. If a FIFO is initially empty, the first word entered into the FIFO falls through to the output where it is available for unloading. If words are unloaded at a slower instantaneous rate than they are loaded, the data words stack up in the order of entry. FIFOs are sometimes referred to as silo memories because of the similarity to the operation of a top-loading hay feeder. The cows at the bottom get the hay in the order that it was pitched into the silo, and the rate at which the cows consume the hay is unrelated to the rate the hay is pitched in as long as the silo is neither depleted nor overfilled.

FIFOs can be loaded and unloaded at asynchronous rates and can adjust for short-term differences in the input and output data rates as long as the FIFO capacity is not exceeded.

The disk controller uses an array of SN74S255 five-bit by 16-word FIFO devices to form a composite 20-bit by 16-word FIFO. Sixteen of the bits in a FIFO word are used for data, and the other four bits are used for flags. The FIFOs adjust for the difference in data rates between the disk interface and the TILINE interface or the microprocessor clock cycle.

Figure 2-49 is a simplified block diagram for an SN74S255 device. For any operation requiring a FIFO, DISKDIRECT- is inactive (high), qualifying the SHIFTIN input. The low to high transition

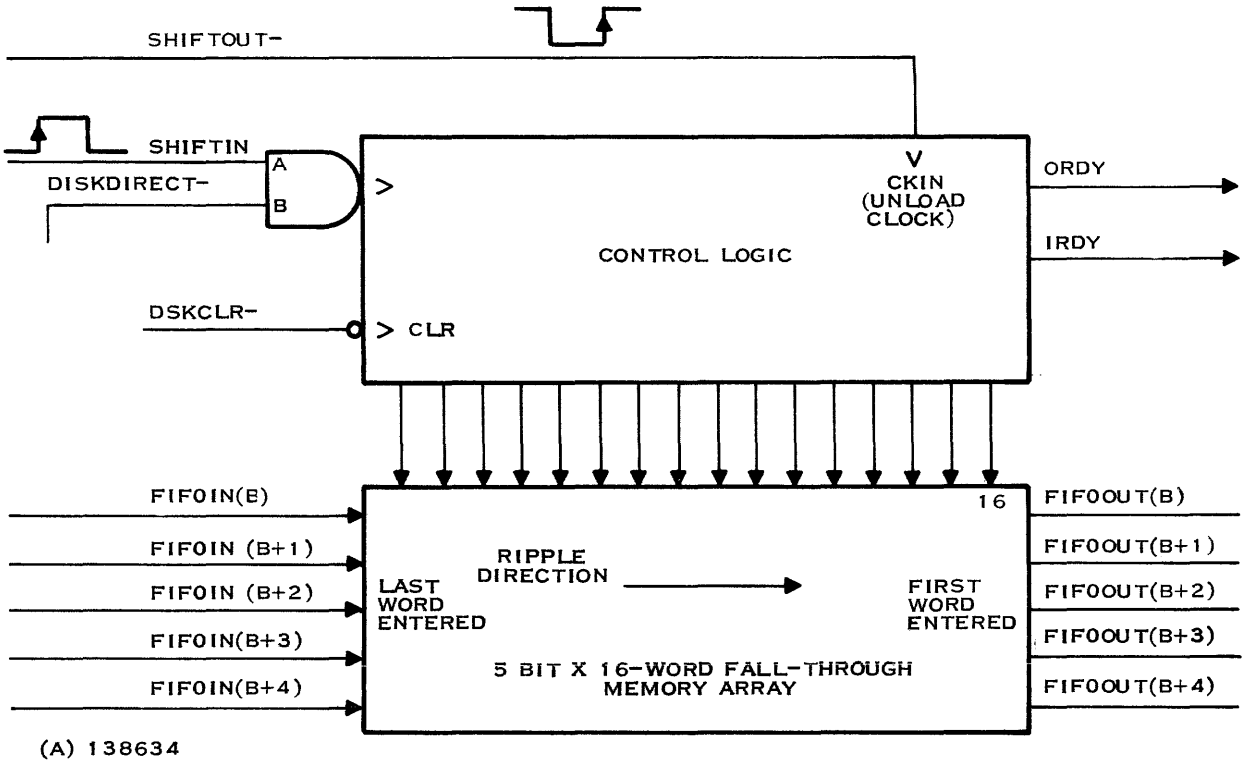


Figure 2-49. SN74S255 FIFO Device Internal Block Diagram

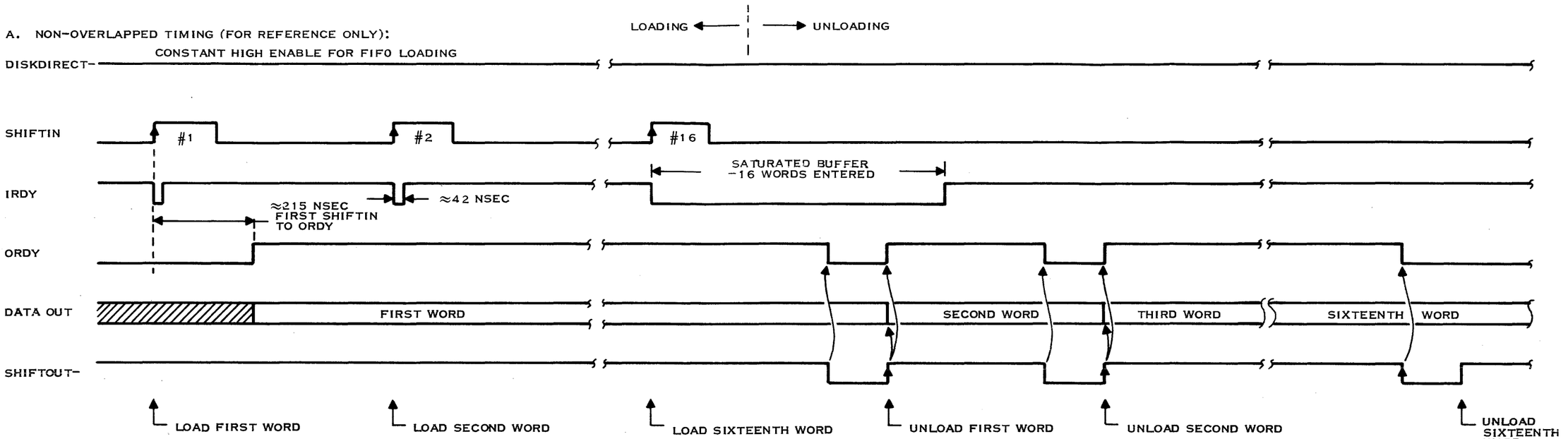
of SHIFTIN loads the five FIFOIN (B) bits into the first stage of the FIFO. The five bits are rippled through the FIFO (by internal clock pulses) to the end of the output queue. The input ready (IRDY) signal goes low for 42-65 nanoseconds as each data word is loaded into the buffer, but it returns high unless the FIFO is filled to its 16-word capacity.

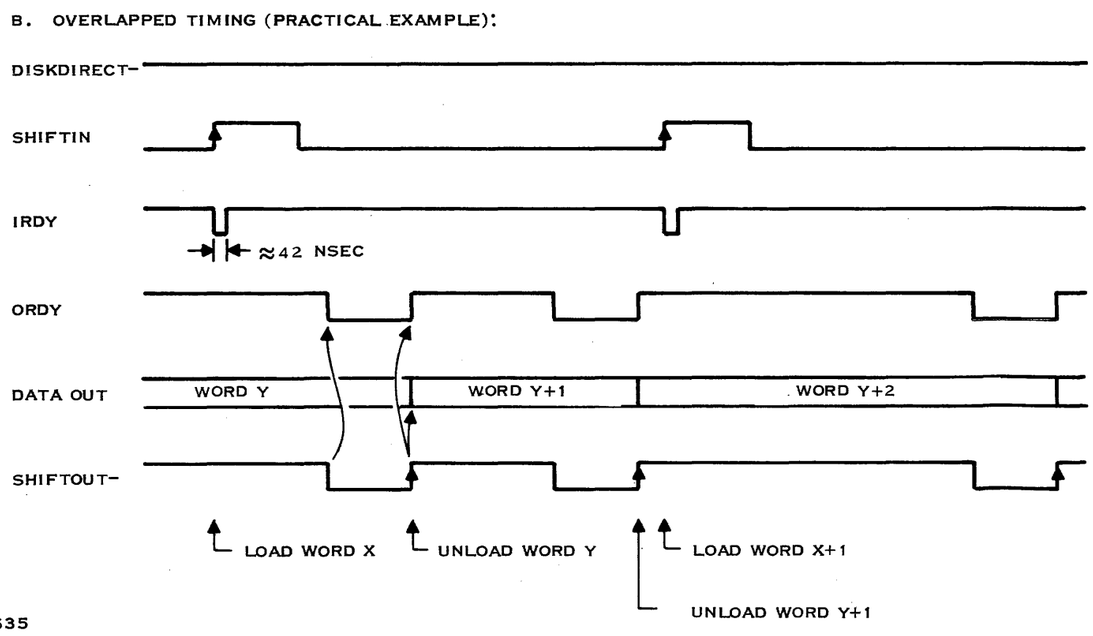
The output ready (ORDY) signal is high when data is available for output. ORDY is delayed approximately 215 nanoseconds from the first shift in signal while the data word shifts through the intermediate stages to the output. The output ready signal indicates that valid data is available at the FIFO output. After accepting the data word, the external circuitry unloads the word from the FIFO with a SHIFTOUT- signal. The positive-going (trailing) edge of SHIFTOUT moves the next word in line to the FIFO output stage. The ORDY output is held low for the duration of the SHIFTOUT signal, but returns high unless the entire FIFO has been unloaded.

The clear input (DSKCLR-) clears the control logic on the negative-going (leading) edge, and forces the output ready (ORDY) low. The clear does not actually clear out all the internal memory locations in the FIFO, but the output ready remains low, indicating invalid data, until new data is loaded into the FIFO and shifted to the output stage.

Figure 2-50 shows timing relationships for an SN74S255 FIFO device. Part A of the figure shows the simplest possible case, fully loading the FIFO and then unloading it, with no overlapping of input and output operations. This case is shown only to show the differences between input and output operations.

Part B of the diagram shows the conditions which actually occur within the controller. In this example, load and unload operations are both going on at differing rates. The ORDY and IRDY outputs are used externally to prevent conflicts between input and output operations. Arbitrary





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NOTE: X-Y ≤ 15

Figure 2-50. SN74S255 FIFO Basic Timing

numbers X and Y are used to represent the input and output data words, respectively. The 133rd word in the data sector might be X, and Y might be the 126th word of the data sector. The important parameters are that X is greater than or equal to Y, because it is not possible to unload a word before loading it, and that the difference (X-Y) must be less than or equal to 15, or the 16-word storage capacity of the FIFO is exceeded.

Figure 2-51 is a detailed block diagram which shows the FIFO array and the related input, output, and control logic. The FIFO array consists of four SN74S225 devices with common control inputs.

The input ready outputs of the four devices, IRDYA-IRDYD, are combined to produce a summary INRDY- signal for the FIFO array. Similarly, the output ready signals, ORDYA-IRDYD are combined to produce the summary output ready, ORDY-.

It is important to note that the disk controller must adapt to the data rate of the disk, and not the other way around. On disk read operations, for example, the data rate from the disk is determined by the rotational speed of a physical platter. This speed may vary somewhat due to mechanical imperfections, but inertia prevents any effective data rate control on a bit-to-bit or word-to-word basis. Therefore, on disk read operations, the disk loads the FIFO at a rate independent of the controller and the operating microprogram. The controller must adapt to that rate by reading and unloading the FIFO fast enough to prevent the FIFO from being saturated.

On disk write operations, the data rate from the FIFO output to the disk is fixed by a crystal-controlled oscillator. Therefore, the rate of FIFO unloading is fixed (within the drift limits of the oscillator) and the controller must adapt to that data rate by loading the FIFO fast enough to prevent being "outrun" by the disk.

The summary INRDY- and OUTRDY- signals play a key role in adapting the controller data rate to the disk and detecting any FIFO errors which do occur.

During a disk read operation, the controller must unload the FIFO and initiate TILINE master write cycles fast enough to prevent the FIFO from overloading but without attempting to read when no data is ready. The OUTRDY- signal is steered through a multiplexer and supplied to the CPE I-bus input as RDYSTATUS-. RDYSTATUS- low informs the controller microprogram that the data is available so it can initiate a TILINE master cycle. The SHIFTOUT- signal is issued by the TILINE master logic upon completion of each single-word TILINE data transfer.

The FIFO capacity is exceeded if a SHIFTIN is issued while INRDY- is high, indicating a full buffer. These signals, steered through the multiplexer as ERRORSET and SHIFT, control the FIFO timing error flip-flop.

During a disk write data operation, the controller must load the FIFO fast enough to keep up with the disk. The summary INRDY- signal is steered through the multiplexers as RDYSTATUS-. RDYSTATUS- low informs the controller microprogram that space is available in the FIFO. The controller microprogram responds by initiating a TILINE master read cycle to obtain a data word. The TILINE master logic shifts the word into the FIFO upon completion of the cycle. For this case, a FIFO timing error would consist of a SHIFTOUT command from the disk interface with no FIFO output word available (OUTRDY- high). OUTRDY- and SHIFTOUT are selected by the multiplexers to control the FIFO timing error F/F.

NOTE

For a FIFO timing error detected during a disk write operation, TIMERRQ generates a vectored interrupt to the controller microprogram. The interrupt is not generated if the FIFO timing

error occurs during a disk read operation. Instead the TIMERRQ signal is routed to the bit 18 input of the FIFO flag multiplexer. The timing error flag is appended to the next data word shifted into the FIFO, as FIFOIN18.

The corresponding output bit, FIFOOUT18, is monitored by the CPE I-bus. Therefore, when that data word reaches the FIFO output, the controller microprogram is notified that a FIFO timing error occurred on the previous data word.

The data inputs to the FIFO, FIFOIN00-15, are supplied by a group of FIFO input multiplexers. The disk I/F read/write signal, DSKWRTQ, selects either processor bus data (DSKWRTQ = 1) or parallel read-back data (DSKWRTQ = 0). Notice that the 16 data inputs to the FIFO are also connected to the inputs of the direct read register. The same SHIFTIN signal which loads a data word into the FIFO also loads it into the direct read register. The three-state outputs of this register are not enabled unless direct mode has been selected by a previous microinstruction, and the transfer is enabled by the bus source field of the current microinstruction. The direct read register is used when verifying sector headers in a formatted read or write operation.

Four of the FIFO inputs, FIFOIN16-19, are devoted to flags. Signal selection for the flag inputs is performed by the FIFO flag multiplexer. This multiplexer is enabled (ENFLAG-) during read operations, or for special group 3 microinstructions. For other cases, the multiplexer supplies all zeros at the output.

The FIFO flag multiplexer outputs are:

Read Operation (DSKWRTQ=0)	Special Group 3 Microinstruction Bits	Other	Outputs
0	ROM36	0	FIFOIN16
0	ROM37	0	FIFOIN17
TIMERRQ	ROM38	0	FIFOIN18
CRCERR	ROM39	0	FIFOIN19

The four flags are routed into a FIFO device, and are effectively appended as extra bits to an incoming data word. With the exception of FIFOIN19, these flags perform no function until they reach the FIFO output.

The CRC error flip-flop is directly controlled by FIFOIN19, so that the CRC character in a sector header can be checked in read direct mode. The output of the CRC error flip-flop is monitored by the CPE I-bus input for read direct operations. For other read operations, FIFOIN19 is monitored by the CPE I-bus when it reaches the FIFO output (FIFOOUT19).

When FIFOIN16, 17, and 18 reach the FIFO output (FIFOOUT16, 17, and 18), they are stored in the disk write flag register by a disk clock pulse. FIFOOUT16 controls the CRC enable flag, CRCENFLAG and CRCENFLAG-. For a read operation, the hardwired 0 into the FIFO input multiplexer reaches the disk write flag register (as FIFOOUT16) and holds CRCENFLAG low, so that read data may enter the CRC generator/checker to be monitored for CRC read-back errors (CRCERR). For a write operation, bit 36 (ROM36) of a special group 3 microinstruction controls the flag. CRCENFLAG must be held low for the duration of the data transmission, to calculate the CRC character. ROM36 changes the flag as the last data word enters the FIFO. When that data word and the flag reach the FIFO output, CRCENFLAG goes high to disable additional CRC inputs and gate the CRC character through the write data/CRC multiplexer to the disk.

FIF0 INPUT AND FLAG MUX SELECTION

ENFLAG-=1	READ (DSKWRTQ=0)	WRITE (DSKWRTQ=1)	OUTPUTS
NO EFFECT	PARDAT00-15	PBUS00-15	FIF0IN00-15
0	0	ROM36	FIF0IN16
0	0	ROM37	FIF0IN17
0	TIMERRQ	ROM38	FIF0IN18
0	CRCERR	ROM39	FIF0IN19

FIF0 TIMING AND CRC PRESET MUX SELECTION

READ	WRITE	OUTPUTS
INRDY- OUTRDY- SHIFTIN SYNCQ	OUTRDY- INRDY- SHIFTOUT CRCPREFLAG-	ERRORSET RDYSTATUS- SHIFT CRCPRES-

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Figure 2-51. First In, First Out (FIFO) Buffer and Related Logic

Notice that CRCENFLAG is always low at the beginning of a read or write transfer, because the disk write flag register is held reset until the disk start F/F sets.

Flag bit 17 controls the CRC preset flag output of the disk write flag register. The CRC generator internal registers must be preset to all ones before starting to calculate or check a CRC character. For write operations, ROM37 of a special group 3 microinstruction is sent through the FIFO (FIFOOUT17) before the first data word. ROM37 high sets the CRC preset flag stage of the register, and the inverted output CRCPREFLAG- is selected by a multiplexer and sent to the CRC generator as CRCPRES-.

For read operations, the state of CRCPREFLAG- is irrelevant, because a multiplexer selects the synchronization detector output, SYNCQ, as the source for CRCPRES-. SYNCQ holds the CRC generator constantly preset until the synchronization character ($6E_{16}$) is detected.

Flag bit 18 controls the stop flag (STOPFLAG) for write operations. A special group 3 microinstruction loads a stop flag into the FIFO with the last data word. When the data word reaches the FIFO output, the stop flag informs the microprogram that the data transmission is complete.

For read operations, flag bit 18 is used to inform the microprogram of FIFO timing errors. FIFO timing errors are detected by the FIFO timing error flip-flop (TIMERRQ). For read operations, TIMERRQ is gated through the FIFO flag multiplexer and through the FIFO, and monitored (FIFOOUT18) by the CPE I-bus.

FIFO Input Loading. Two inputs, DISKDIRECTIN- and SHIFTIN, control the loading of data and flags into the FIFO. DISKDIRECT- acts as a constant (high) enable when the controller is not in the direct mode. The direct mode is used when the controller verifies sector headers from the disk. Since this operation does not require the TILINE, there is no need to use the FIFO. The controller uses the direct read register for verifying sector headers. For all other operations involving data transfer to or from the disk, the FIFO is used, and DISKDIRECT- is held inactive (high).

The SHIFTIN signal is the strobe which actually loads data into the direct read register, the FIFO, the CRC error F/F and (for read operation only) the FIFO timing error F/F. Data is shifted in on the positive-going (leading) edge of SHIFTIN.

A SHIFTIN signal is generated if TLSHIN-, UTCSHIN-, or DSKSHIN- is active (low). TLSHIN-, TILINE shift in, is generated during write data or write data unformatted operations (R1, bits 5-7 = 011 or 101). During these operations, the disk controller, acting as a TILINE master, reads words from 990 memory and transfers them over the TILINE and the processor bus to the FIFO input. ROM33L, a latched version of microinstruction bit ROM33, is low to command a TILINE master read cycle. The master device complete (MDCMP-) pulse shifts the data word into the FIFO and restores the TILINE master access logic to its initial state.

UTCSHIN- is generated to load a word from the CPE outputs into the FIFO. UTCSHIN- is generated by a microinstruction which specifies the FIFO as the processor bus destination (ROM20, 21 = 10).

As an example of this type of operation, consider the gap and synchronization character which must precede a header or a data record on the disk. The disk electronics includes a phase-locked read clock/data separator. In order to phase lock the disk drive variable frequency oscillator (VFO) before reading the record, the prerecord gap must be filled with clock pulses as part of the write operation. This is equivalent to saying that the disk controller must write an all-zeros record into the gap which precedes the data record. Also, the last eight bits of the gap must be a $6E_{16}$ synchronization character, to notify the controller to start reading data and start performing the CRC calculation.

NOTE

There cannot be any phase jumps or discontinuities between the end of the all-zeros (clock only) record written in the gap and the actual data record. For this reason, if a record is to be rewritten (as in an update) the preceding gap and sync character must also be rewritten. There will be glitches at the very beginning of the rewritten area of the track, but this is an area which is not monitored during read operations.

The CPE array supplies the all-zero words and the 006E word which marks the end of the gap and the beginning of the data record or header. Each of these words is strobed into the FIFO by a microinstruction which specifies the FIFO as the processor bus destination (ROM20, 21 = 10). The controller requests data words via the TILINE and loads them into the FIFO while the write gap operation is in progress.

As another example, CPE output data is loaded into the FIFO and transmitted to the disk during a write format operation (R1, bits 5-7 = 001). This operation writes the record headers on a track, and fills the data area with a data word. The sectors per record parameter determines which sectors get record headers. There are no TILINE to disk transfers during a write format operation.

Data read from the disk is converted to parallel form in the serial to parallel shift register, and loaded into the FIFO (or direct read register) by a DSKSHIN- pulse. DSKSHIN- is generated during read operations (DSKWRTQ- high) when a full 16-bit word has been shifted into the serial/parallel shift register (CNTEQ15 high). A disk clock pulse (DCLK) strobes the command on the leading edge. The first bit of the next data word is shifted into the shift register on the trailing edge of disk read clock.

FIFO Output Unloading. Output data is unloaded from the FIFO on the trailing (rising) edge of SHIFTOUT-.

NOTE

FIFO output data is valid and available before the SHIFTOUT- pulse. The external circuitry (CPE input, serial/parallel shift register or 990 main memory) accepts or stores the FIFO output before the SHIFTOUT- pulse.

The SHIFTOUT- pulse allows the next word in line to reach the FIFO output stages and, after ripple-through time, frees an input word location for reuse. The output ready signal is disabled for the duration of the FIFO unload (SHIFTOUT-) pulse.

Three signals, TLSHOUT-, UTCSHOUT-, and DSKSHOUT-, can enable a SHIFTOUT- pulse. TLSHOUT- (TILINE shift out) occurs during read data or read unformatted operations. During these operations, data is read from the disk and stored in 990 memory by a series of TILINE master write cycles. ROM33L- is low to command a TILINE master write cycle. A low master device complete (MDCMP-) pulse occurs upon completion of the master write operation. MDCMP- returns the TILINE master access logic to a reset state and enables TLSHOUT-.

In some cases it is desirable to read data from the disk through the FIFO and over the processor bus without transferring the data over the TILINE.

For example, during closed-loop self-testing of the controller, data is transferred out through the FIFO to a test memory and then transferred back through the FIFO to the CPE inputs. The UTCSHOUT- pulse is used during the read-back operation to unload the FIFO.

The DSKSHOUT- pulse causes a FIFO unload pulse (SHIFTOUT-) each time a data word is loaded into the serial/parallel shift register for transmission to the disk. The parallel data is loaded into the serial/parallel shift register on the leading edge of the DISKDATLD- pulse. The next disk clock pulse enables the DSKSHOUT- pulse. The trailing edge of that disk clock pulse disables DISKDATLD- and performs the FIFO unload function.

During read operations, FIFO output data is routed to the processor bus via the FIFOOUT/zero multiplexer. This multiplexer supplies all data zeros (high levels to the active low processor bus) when commanded by the P-bus source field of a microinstruction. It is in the high impedance state if neither zeros or FIFO data are required. If disk data is required for a TILINE master cycle or for CPE input, FIFO data is gated through the multiplexer. When no source of data is selected, the PBUS is in the high impedance state, and can be manipulated by an external source such as a RAM board.

During write operations, FIFO output data is loaded into the serial/parallel shift register by the trailing edge of a DISKDATLD- pulse from the disk I/F start and read/write control logic. Subsequent disk clock pulses shift the data serially through the register and clock/data encoding logic to the selected disk unit.

2.12.1.5 Cyclic Redundancy Check (CRC) Circuitry. The cyclic redundancy check provides a rigorous method of error detection over the course of an entire data record. All the serial data in a record is processed by an error-checking algorithm as it is transmitted to the disk drive. The result of the CRC calculation is a 16-bit CRC character which is transmitted at the end of the record. When the record is read back, the read data is reprocessed according to the same checking algorithm. At the end of the record, the CRC character calculated during the read operation must compare to the CRC character recorded at write time or an error has occurred.

The disk controller uses a 9401 programmable CRC generator/checker. The programming inputs are hardwired low to permanently select the CRC-16 algorithm. This algorithm divides the write data stream by the polynomial $X^{16} + X^{15} + X^2 + 1$. The CRC character is the remainder left after that modulo 2 division. During read operations, the record is again divided by the polynomial. When the recorded CRC is shifted into the 9401, the new remainder and the recorded CRC character should cancel, leaving all zeros in the CRC generator internal registers.

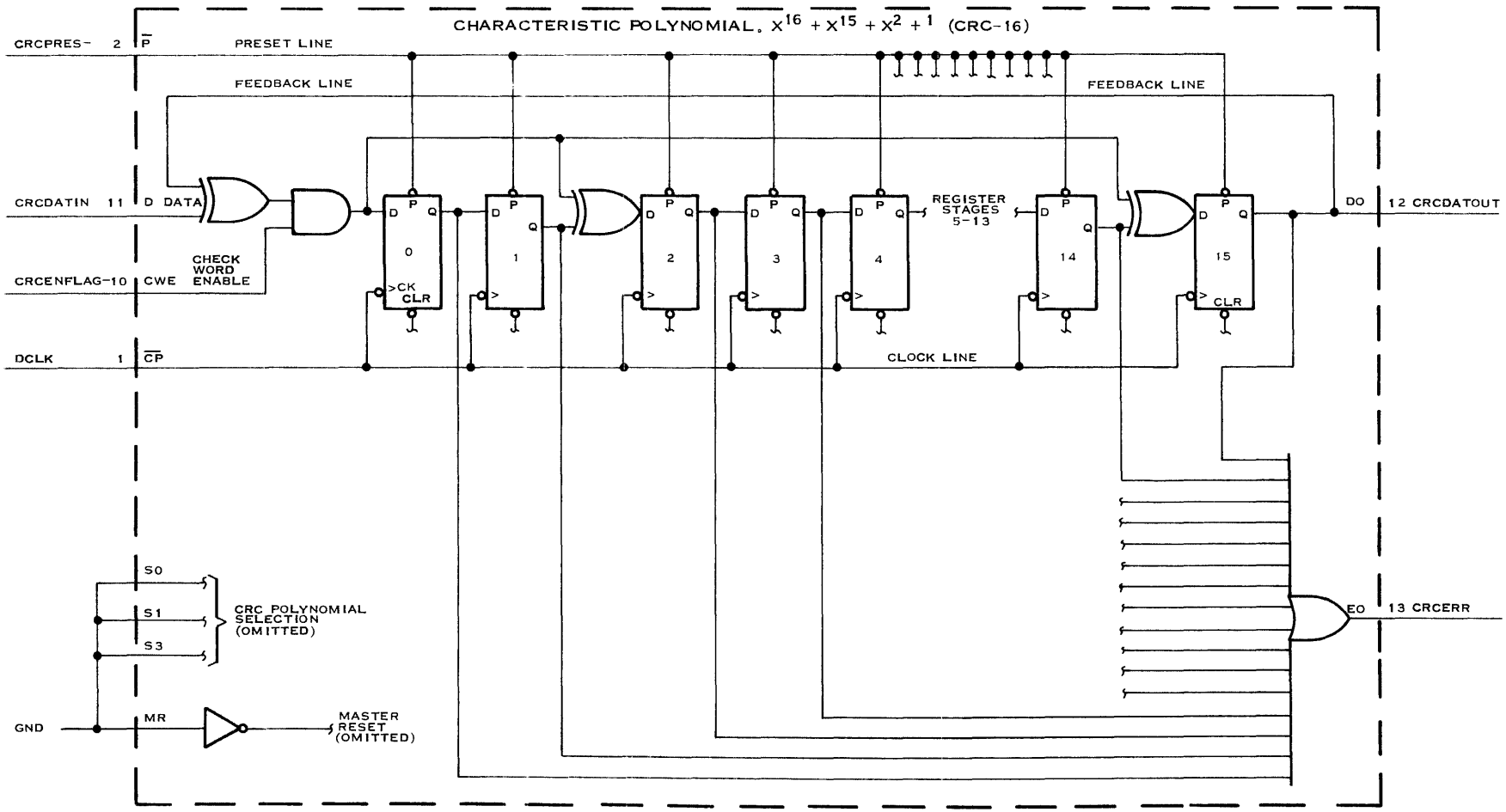
The important thing to know about the cyclic redundancy check is that it is much superior to a simple parity check. A parity check can only detect odd numbers of errors. The CRC algorithm used in the disk controller can detect:

- All odd numbers of error bits
- All 16-bit or shorter error bursts
- 99.9969% of all 17-bit error bursts
- 99.9984% of all longer error bursts.

These error burst figures assume a single error burst in the transmission.

Figure 2-52 is the equivalent circuit for the 9401 CRC generator/checker as used in the disk controller. The CRC generator has flip-flop stages connected as a feedback shift register. The exclusive-OR gates in the feedback chain correspond to the terms of the CRC polynomial.

All stages in the 9401 must be preset to ones just before processing a write or read data record. A low CRCPRES- signal presets the generator. CRCPRES- is supplied by the FIFO timing and CRC



NOTES: 1. THE CHECK WORD ENABLE (CWE) INPUT, WHEN HIGH, ALLOWS THE CRC GENERATOR TO PROCESS THE SERIAL READ OR WRITE DATA STREAM. CWE MUST BE HELD LOW TO SHIFT OUT THE RESULTING CRC CHARACTER (WRITE) OR TO GIVE A VALID CRC ERROR INDICATION (READ).

2. THE ERROR OUTPUT (EO) IS VALID AFTER THE CRC GENERATOR HAS PROCESSED THE ENTIRE READ DATA STREAM AND ACCEPTED THE LAST BIT OF THE CRC CHARACTER WHICH WAS APPENDED AT WRITE TIME. EO REMAINS VALID UNTIL THE NEXT NEGATIVE-GOING CLOCK TRANSITION.

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Figure 2-52. Equivalent Circuit for CRC Generation

preset multiplexer. CRCPRES- is developed as the result of detecting the synchronization character (read) or as the result of a CRC preset flag which is enabled by a special group 3 microinstruction, shifted through the FIFO in advance of the transmission, and latched in the disk write flag register.

CRCENFLAG- must be high to allow read or write data to be shifted into the CRC generator. For a write operation, CRCENFLAG- must go low at the end of the record to allow the CRC character to be shifted out. CRCENFLAG- and its complement CRCENFLAG are controlled by a special group 3 microinstruction. ROM36 of the microinstruction is routed through the FIFO flag multiplexer and through the FIFO (FIFOOUT16), and latched in the disk write flag register.

CRCDATIN is the serial read or write data input to the CRC generator/checker. Disk clock, DCLK, loads the data on the negative-going (trailing) edge.

The CRC character is serially transmitted out of the 9401 on the CRCDATOUT line. The CRCERR output is valid at the end of a read operation, when the CRC generator/checker internal registers should contain all zeros.

Figure 2-53 shows the CRC generator/checker and the associated multiplexers. The CRC read/write multiplexer selects read data (DISKDATIN) or write data (PARDAT00) as the data input, CRCDATIN. During write operations, the serial output of the serial/parallel shift register feeds the write data encoding circuits until the CRC enable flag gates the CRC character through the data/CRC multiplexer.

2.12.1.6 Read Data Buffers and Disk Read/Write Clock Distribution. Figure 2-54 shows the read data buffers and disk read/write clock selection circuitry. The figure also shows the sections of the CRC logic which apply to read operations. This description also requires reference back to figure 2-48, disk I/F start and read/write control.

Data is serially recorded on the disk in double frequency FM form, that is, with clock and data pulses multiplexed into the same bit stream. The time between the leading edges of the successive clock pulses is a bit cell. To record a data one on the disk, a pulse is recorded in the middle of the bit cell; and to record a data zero, no pulse is recorded in the middle of the bit cell. The instantaneous frequency of the waveform is determined by the data being recorded. If all zeros are recorded, as in gap 1 or gap 2, only clock pulses appear on the track, and the frequency is 2.5 Mhz. If all ones are recorded, the frequency is 5Mhz. During typical operations, the frequency varies with the data pattern between these limits.

A phase-locked clock/data separator in the disk drive electronics supplies clock (RCLK-) and data (RD-) to the disk controller on separate lines. For read operations, RCLK- serves as the source for the disk clock signals (DCLK, DCLK-, DCLK1-, DATCLK) distributed through the disk interface circuits of the controller.

Read buffer timing is shown in figure 2-55. The top two signals in this diagram are disk clock (read clock) and read data. The diagram clearly shows that the read data pulses fall in the middle of the bit cells defined by DCLK-. DCLK and DCLK- are used to time all read data operations up through FIFO loading. FIFO unloading is asynchronous to disk clock during read operations.

The disk clock pulse at the beginning of a data cell clears the read 1 F/F in preparation for the data pulse. The read pulse width is specified between 50 and 150 nanoseconds, with 100 nanoseconds nominal. The time between two successive disk clock leading edges (400 nanoseconds, nominal) defines a sampling window for the data pulse. The data pulse (RD-), if any, asynchronously sets the read 1 F/F. The disk clock pulse which ends the sampling period transfers the data bit to the read 2 F/F, and prepares read 1 for another input.

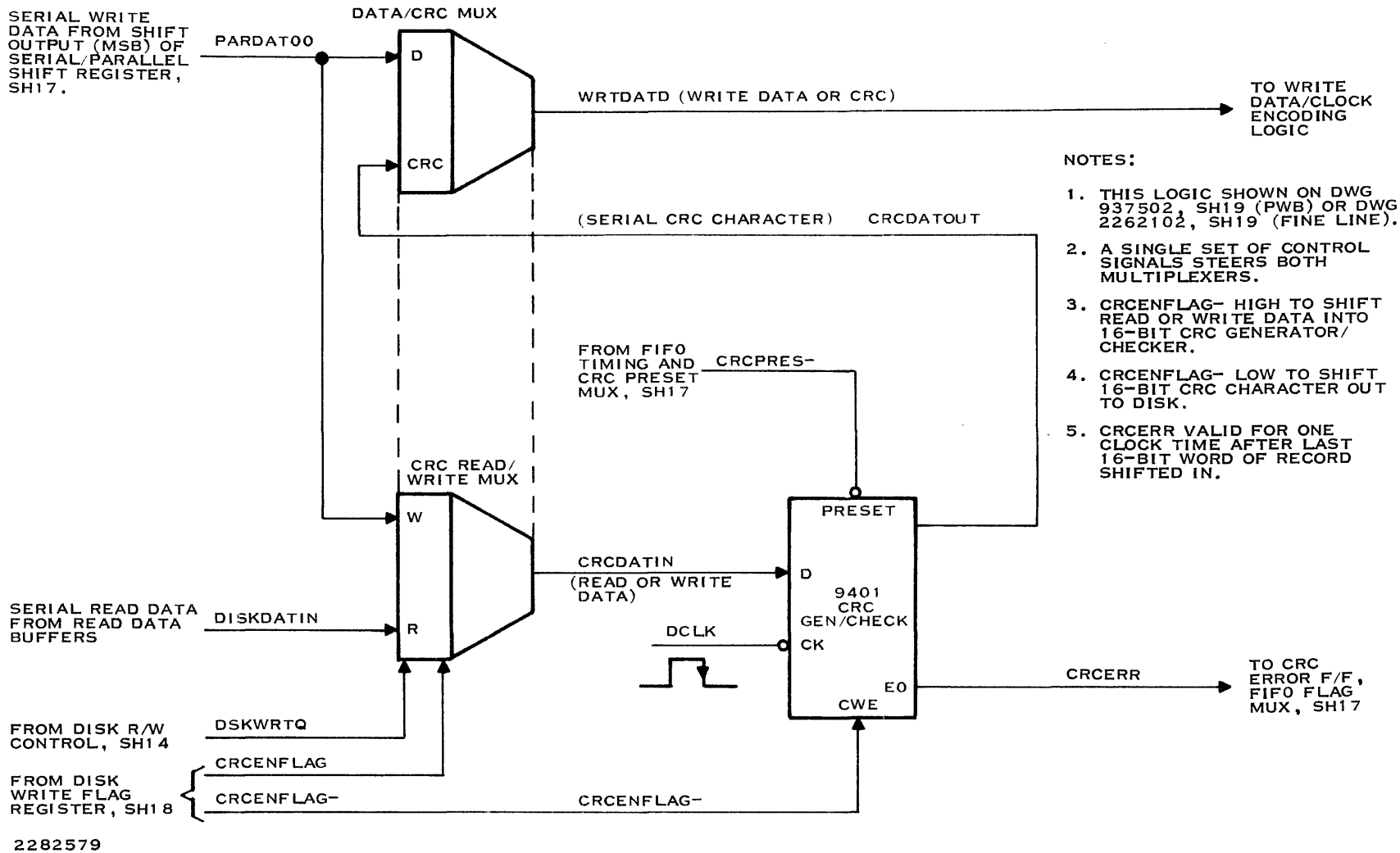


Figure 2-53. CRC Generator/Checker Input/Output Connections

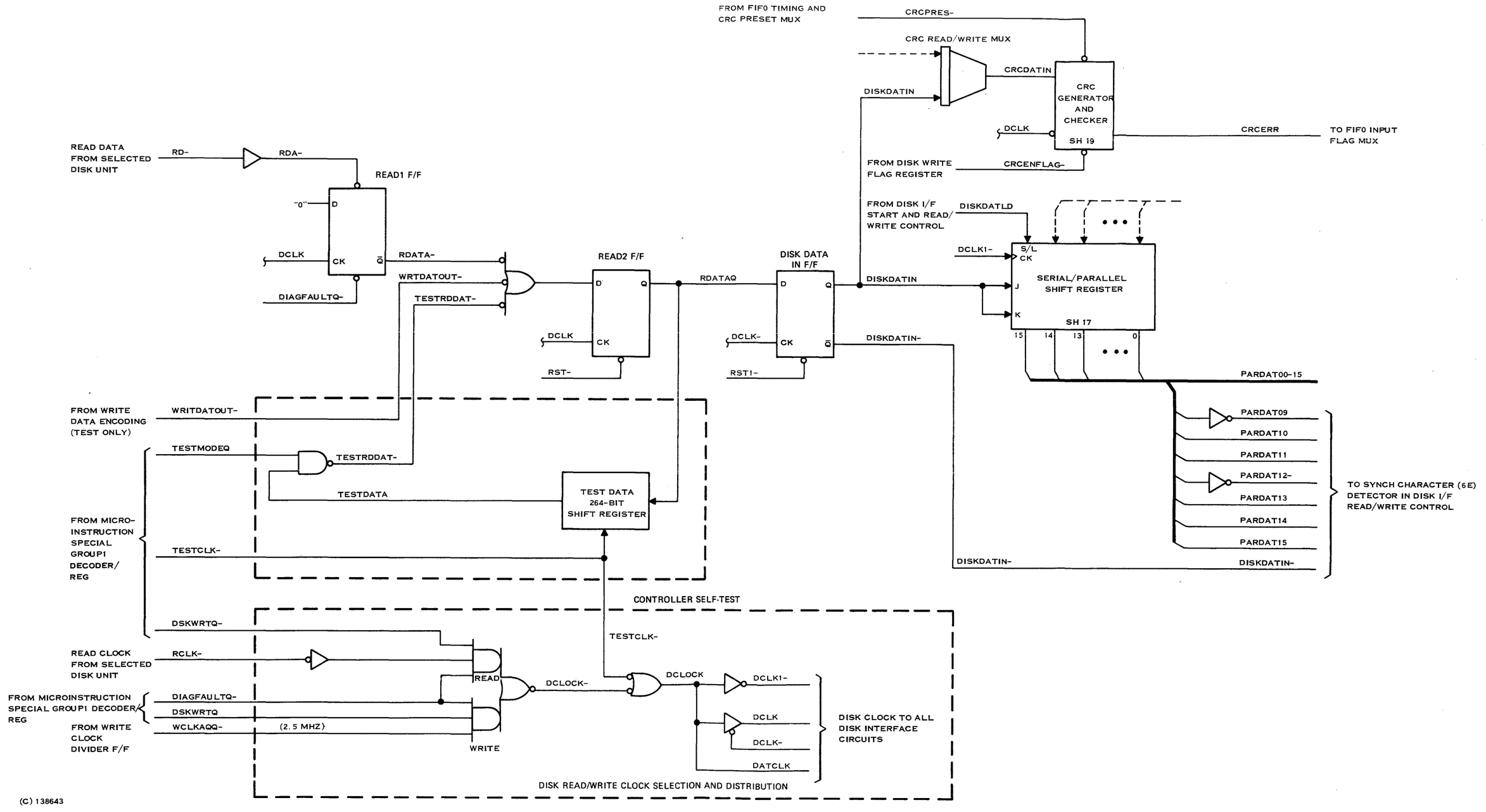
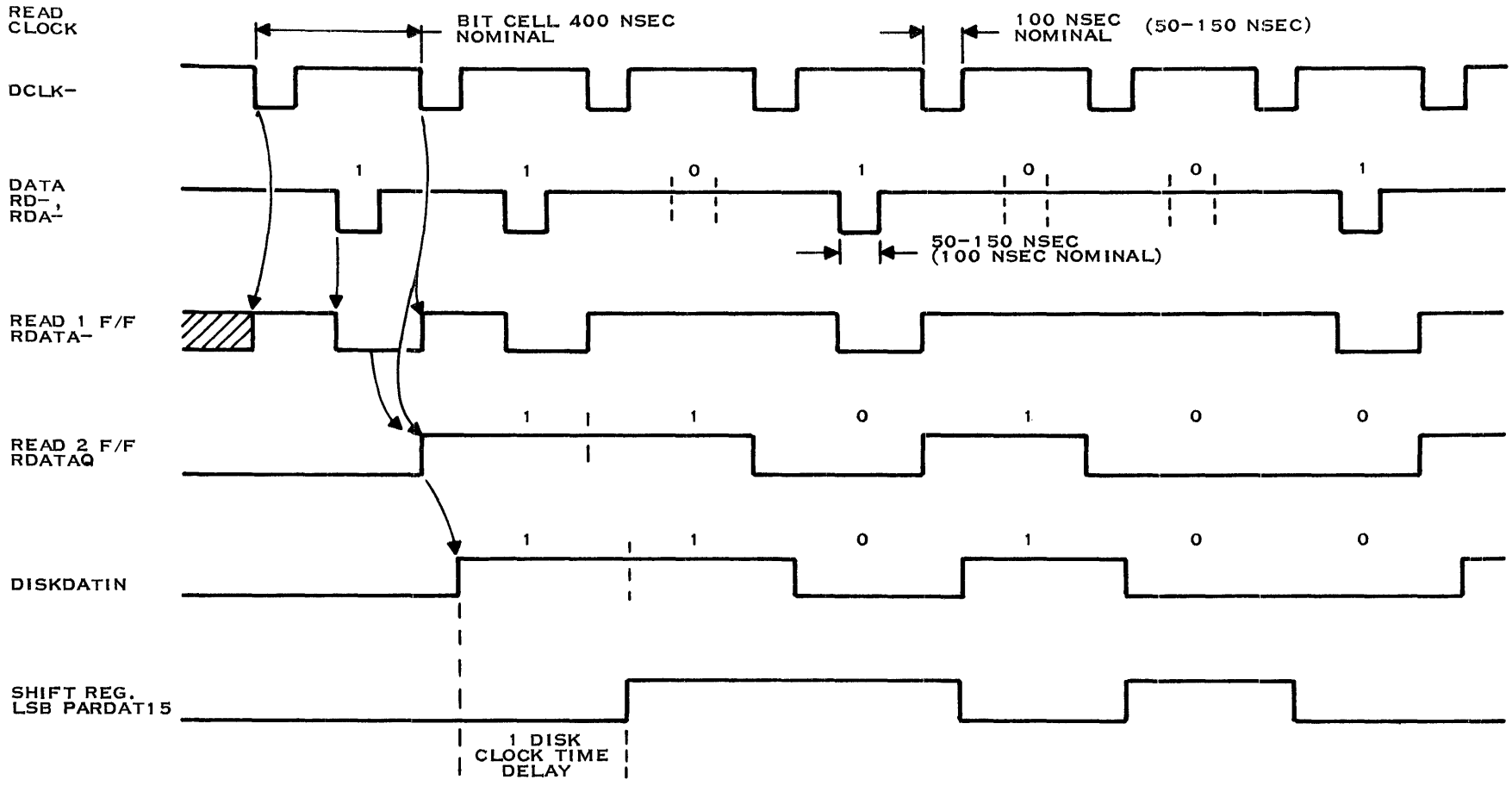


Figure 2-54. Read Data and Clock Buffers, Self-Test, and Disk Clock Distribution



(A) 138632

Figure 2-55. Read Buffer Timing

The read 2 F/F converts the incoming data from bit-cell format to nonreturn to zero (NRZ) format. This format (see RDATAQ) is the most natural for serial data processing. There is a disk clock pulse width delay (approximately 100 nanoseconds) between the RDATAQ and DISKDATIN waveforms, as RDATAQ is clocked on the leading edge of disk clock, and DISKDATIN is clocked on the trailing edge.

DISKDATIN is routed to the CRC logic for error checking, and to the shift register for serial to parallel conversion. DISKDATIN- is used in synchronization character detection, described later in this section.

DISKDATIN is loaded into the least significant stage of the shift register (PARDAT15) on the next disk clock trailing edge. Subsequent disk clock pulses shift the data until a full 16-bit word is available on the PARDAT00-15 lines. A disk clock pulse counter in the disk I/F start and read/write control logic tallies these shifts so 16-bit data is correctly loaded into the FIFO and direct register.

Figure 2-56 is a detailed timing diagram which shows the principle events which occur at the beginning of a read operation. These events include the disk interface start command, reception and recognition of the synchronization character, and shifting of the first data word into the FIFO buffer/direct register. In addition to the read buffer logic of figure 2-54, refer back to the disk interface start and read/write control logic, figure 2-48.

This description applies to reading data as part of a read data or read unformatted operation, and also to reading sector ID headers as part of a read data or a write data operation. This description assumes that the read gate (RG-) to the disk has previously been asserted, and that the read gate delay has been counted down in the controller microprogram. This is equivalent to saying that the clock/data separator logic has been enabled for a period sufficient to lock on to the disk clock. Recall that disk clock is recorded in the preheader and prerecord gaps (gap 1, gap 2) to make this synchronization possible.

The disk read/write command, DSKWRTQ, must be low for the duration of the operation. This signal is supplied by the microinstruction special group 1 decoder/register, and the state is latched, so that a specific microinstruction must be used to change read or write mode. This disk I/F start logic is initiated by a disk start transfer clock (DSTRTCK-) pulse. This pulse is synchronized to the microprocessor clock pulse, and sets the disk start transfer F/F (DSKSTRQ).

The next disk clock pulse resynchronizes the operation to disk clock by setting the disk start F/F (DSTARTQ). All remaining disk interface operations, up to the point of loading the FIFO/direct register, are synchronized to the clock pulses recovered from the disk.

During the gap prior to the header or first data word, the read buffer and serial/parallel shift register cycle on all zeros, waiting for the hexadecimal 6E synchronization character which serves as a pointer to the first header or data word. The synchronization detector monitors the shift register parallel outputs, looking for the following combination:

PARDAT						PARDAT	
09	10	11	12	13	14	15	DISKDATIN
0	1	1	0	1	1	1	0

Note that the shift direction for data entry is from DISKDATIN to PARDAT15, to PARDAT14, . . . toward PARDAT00. The sync pulse (SYNC6E-) is actually generated one disk clock cycle before the sync character is fully shifted into the shift register. The synchronization F/F, SYNCQ, clocks as the last bit of the sync character shifts into the shift register. Note that the sync F/F is connected in an upside-down configuration.

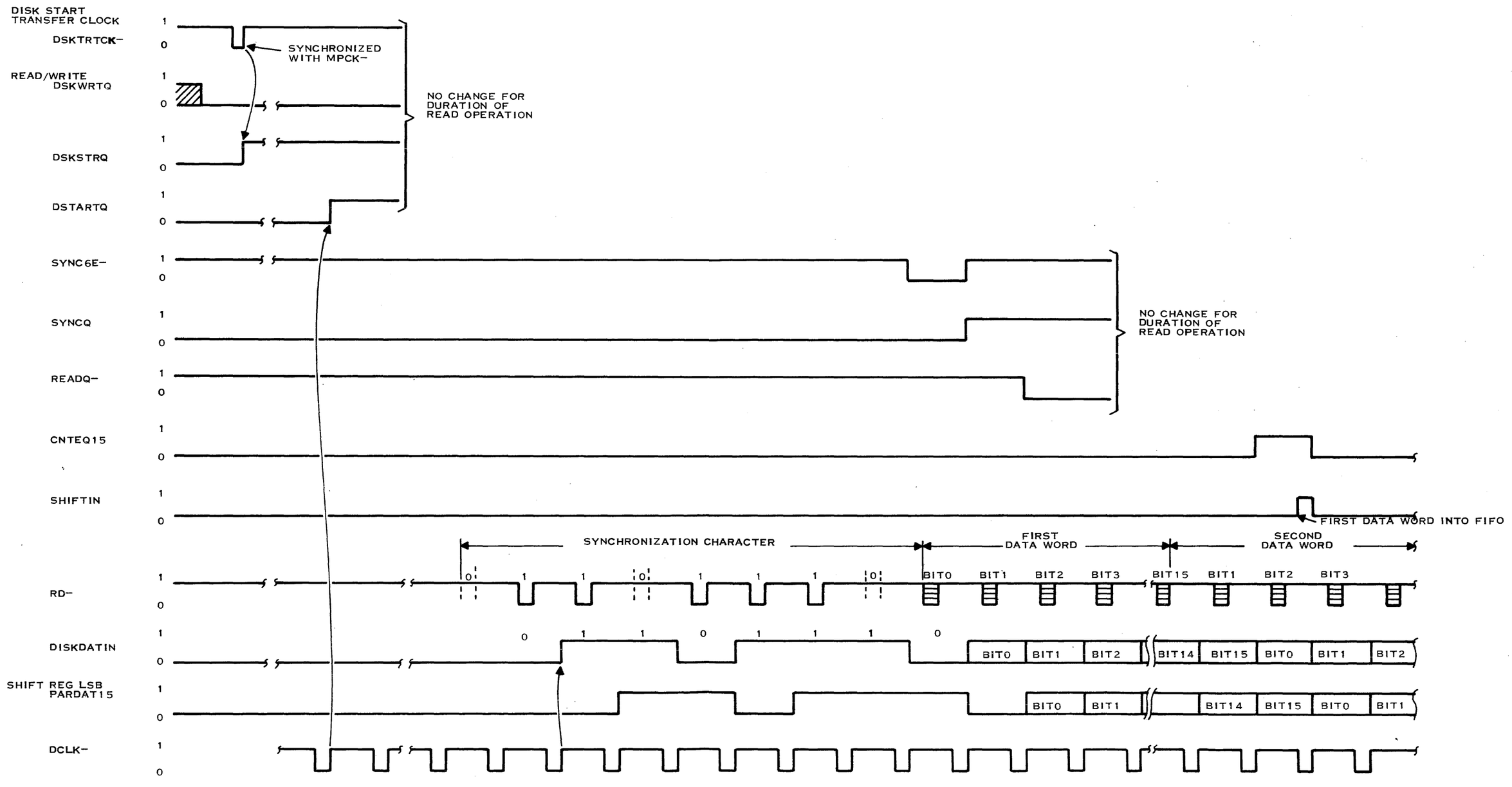


Figure 2-56. Timing for Synchronization Character Detection and FIFO Loading

The read F/F sets on the next disk clock pulse, removing the constant clear input to the bit counter. The bit counter starts at 00 as the first data bit enters the shift register. The next clock pulse advances the bit counter to 01 as the register shifts in the second data bit.

The sixteenth shift pulse enters the last data bit into the shift register, and the bit counter indicates saturation (CNTEQ15) for the next disk clock period.

The trailing edge of disk clock is used for shifting the data. The SHIFTIN pulse is enabled on the leading edge of disk clock when CNTEQ15 is high, so that stable data is loaded into the direct read register or FIFO input. The trailing edge of the disk clock pulse shifts in the first bit of the next data word, and rolls the bit counter over to 00, so CNTEQ15 is disabled. Successive disk clock pulses shift the register until the next 16-bit data word is assembled on the PARDAT00-15 output lines. The shift, count, and load to FIFO/direct read register sequence repeats until the entire record is read.

2.12.1.7 Write Data and Clock Encoding. Figure 2-57 summarizes disk write clock generation and write data/clock encoding. The basic timing reference for write operations is a crystal-controlled 5 Mhz square-wave oscillator. The oscillator runs constantly, although the output, DSKOSC, may be gated off by external clock stop signals (WOSCTST-, WOSCSTOP-). A controller fault detected during self-test also will disable the clock output. In this case, a special group 1 microinstruction disables the oscillator output and lights the FAULT indicator with the DIAGFAULTQ- signal.

The output of the oscillator gating logic is the 5 Mhz write clock signal, WCLK. A divide-by-two circuit produces a 2.5 Mhz square wave, WCLKAQQ-. WCLKAQQ- is used in write data encoding, as described in this section. Also, reference back to the disk clock distribution circuits of figure 2-54 (Read Data Clock Buffers, Self-test, and Disk Clock Distribution) shows that WCLKAQQ- serves as the source for disk clock during write operations. DCLOCK, DATCLK and DCLK are (except for gate delays) identical to, and in phase with, WCLKAQQ- if disk write (DSKWRTQ) is high and no fault is detected.

Notice that disk clock, DCLK, is a symmetrical wave train with a 50% duty cycle for write operations, while disk clock has a 25% duty cycle for read operations.

Figure 2-58 is a timing diagram which shows the write data and clock encoding. This timing diagram assumes that a parallel data word has been loaded into the shift register and is available for transmission. The complete operation, including the details of shift register loading, is described on another timing diagram in this section.

Serial data is shifted to the MSB output of the serial/parallel shift register, PARDAT00, on the trailing edge of disk clock (rising edge of DCLK-). One-half clock time (200 nanoseconds) later, the data bit is loaded into the write data out F/F. WRTDATOUT- and WCLKAQQ- are combined in a NAND gate to produce write data and clock enable, WDNCLKEN.

WDNCLKEN serves as a gating signal to gate 100-nanosecond WCLK pulses through the write data and clock (WDNCLK-) NAND gate/driver to the selected disk drive. Whenever WDNCLKEN is high, write clock (WCLK) pulses are inverted and transmitted to the drive. WDNCLKEN drops low for 200 nanoseconds in the middle of a bit cell if a zero data bit is to be transmitted. The low WDNCLKEN signal blocks transmission of the mid-bit cell pulse. WDNCLKEN returns high before the end of the bit cell, to enable the output clock pulse which marks the start of the next bit cell. If a data one is to be transmitted, WDNCLKEN remains high in the middle of the bit cell, and the 100 nanosecond data pulse is transmitted in the middle of the bit cell.

Figure 2-59 is a large, detailed timing diagram which shows disk interface operations for a write data operation. This description assumes that the read direct operation (for record header verification) has already been performed.

Refer back to the disk I/F start and read/write control logic, figure 2-48. The disk interface is commanded to write mode (DSKWRTQ=1) by a special group 1 microinstruction. The operation is initiated by a disk start transfer clock pulse (DSKSTRTCK-), decoded from a special group 0 microinstruction and strobed by MPCK-. The disk start transfer F/F sets on the trailing (rising) edge of DSKSTRTCK-, releasing the constant reset from the disk start and write F/Fs.

The disk start F/F resynchronizes the operation to disk clock on the next rising (trailing) edge of DCLK-. The write F/F sets one clock time later. The first disk data load (DISKDATLD) pulse of the operation is enabled in the interval between the rising edge of DSTARTQ and WRITEQ. DISKDATLD loads the first data word into the serial/parallel shift register. The first disk data load pulse is a special case; the remaining DISKDATLD pulses are generated at 16-bit intervals when CNTEQ15 from the bit counter goes high.

The first data words are all zeros. They are written into the gap prior to the data record to provide synchronization inputs to the disk drive read clock/data separator circuits. The all-zeros data words cause only clock pulses to be recorded on the disk. Timing loops in the controller microprogram determine the duration of clock-only output.

The synchronization word, $006E_{16}$, is recorded immediately following the end of the gap. The last eight bits represent the 6E synchronization character. The encoded bit stream which represents the 6E character is shown in the middle of the timing diagram.

As the last bit of the synchronization character is transmitted, the first data word is loaded into the serial/parallel register and unloaded from the FIFO.

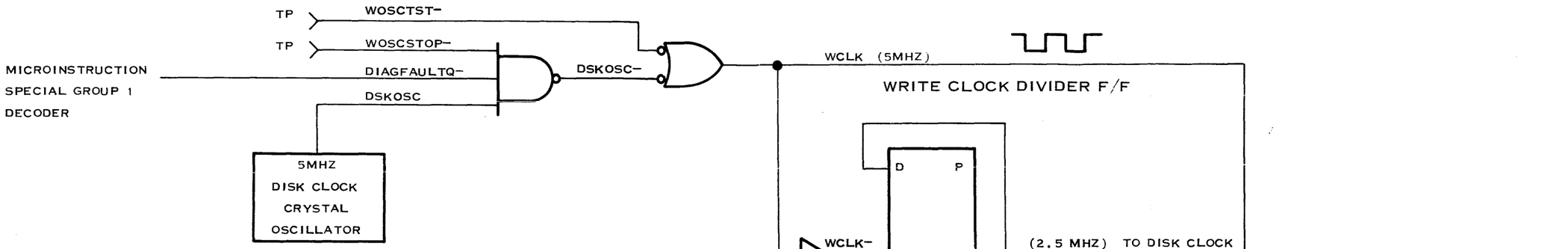
Data transmission takes place in the sequence previously described, with the disk interface shifting a word out of the FIFO every 16 disk clock times, and the processor initiating TILINE master read cycles to supply FIFO input data.

When the record word count maintained by the CPEs expires, all the data words have been loaded into the FIFO. The processor loads an all zeros data word with the CRC enable flag (bit 16) set, and then another all zeros word with the stop flag (bit 18) set. These words stack up in the FIFO until the disk interface transmits the last word of the record. The CRC enable flag (CRCENFLAG) changes the steering of the write data/CRC multiplexer and enables the CRC generator to shift out a 16-bit check character. When the last bit of the CRC character is transmitted, the all-zeros word with the stop flag is shifted out of the FIFO, and the stop flag is latched up in the disk write flag register. The stop flag informs the CPEs that the last data word has been transmitted. The microprogram terminates the operation with a disk clear pulse, changes DSKWRTQ to zero, and disables the write gate, stopping the write operation at the disk drive.

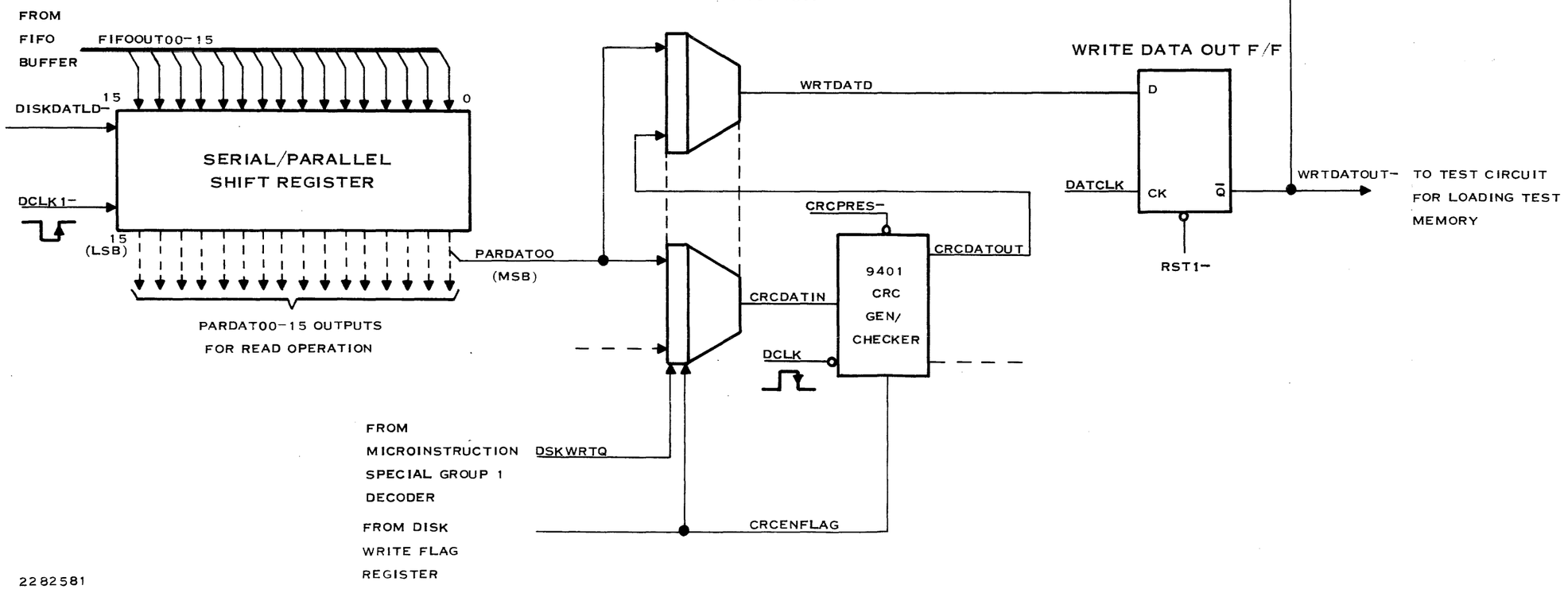
2.12.1.8 Self-Test. A self-test capability built into the controller provides verification of controller integrity and aids in troubleshooting. The self-test has two forms, short and long. The short self-test verifies the read and write data paths, including the processor bus, FIFO, parallel/serial converter, CRC generator/checker, sync character detection, direct register, and parts of the read and write data I/O circuits. The long self-test performs all the short test checks, plus command timer and CPE internal register checks. A status count is maintained as the self-test executes. If the test fails, the status count may be used to determine how far the test executed before the failure.

The short self-test is performed each time a new controller operation is specified by control words W0-W7. The long test is performed if the specified command is Store Registers (W1, bits 5-7 = 000). The short self-test is also executed on power up or I/O reset, as part of the TILINE abort interrupt trap routine. For controller test purposes only, the long test jumper, J2, causes the controller to execute the long test on power up or I/O reset. The long test jumper should not remain in place when the controller is returned to normal service.

WRITE CLOCK GENERATION AND CONTROL



DATA/CRC MUX



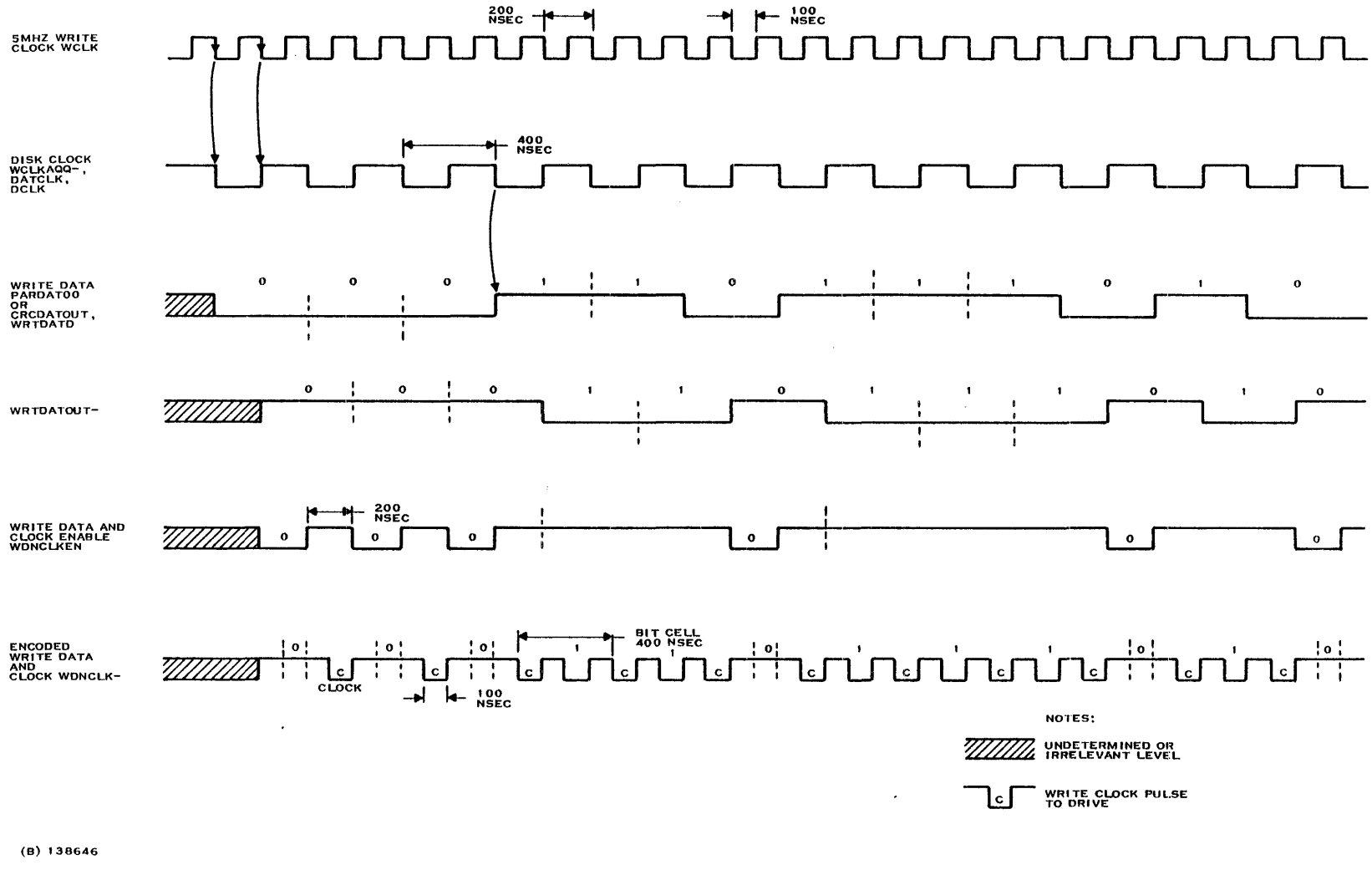


Figure 2-58. Timing Diagram for Write Data and Clock Encoding

Figure 2-60 is a simplified data flow diagram for self-test operations. The self-test operation is performed under control of the Z diagnostic test (ZDT) and subordinate routines in the controller microprogram.

No data is transferred over the TILINE during the course of a self-test operation. Test data patterns are supplied in the immediate operand field (ROM32-39) of the microinstruction and loaded into the CPE via the K-bus.

Test write data is transferred over the processor bus and loaded into the FIFO input. FIFO output data is converted to serial form and sent to the CRC generator and the write data logic. Instead of being encoded and sent to the disk, the data is loaded into a TMS 3129 serial test memory.

After the simulated transmission into the test memory, the data is read back through part of the read data buffers, and into the serial/parallel shift register. The CRC character is checked during the read operation. The data follows the normal read data path through the FIFO and onto the processor bus. The CPE accepts the data and checks it against the previously transmitted values.

This closed-loop test verifies the integrity of most of the read and write data paths. It does not test the encoding circuitry which converts write data into bit cell form, and it does not test the read data buffer which converts data from bit cell form to NRZ form. It tests the disk clock drivers, but not the disk clock generation circuits. Various data patterns (0000, FFFF, 5555, AAAA) are used in this loop-back test to detect pattern sensitivity and stuck bits.

The short self-test also includes direct register read and write operations, to verify the ability of the direct register to accept and store data.

A microprogram-controlled test clock supplies disk clock (DCLK, DCLK-, DCLK1-, DATCLK) during test operations. Special group 1 microinstructions control the test clock (TESTCLK-) waveform. A diagnostic test subroutine, Z test clock, controls the on time and off time of the test clock waveform.

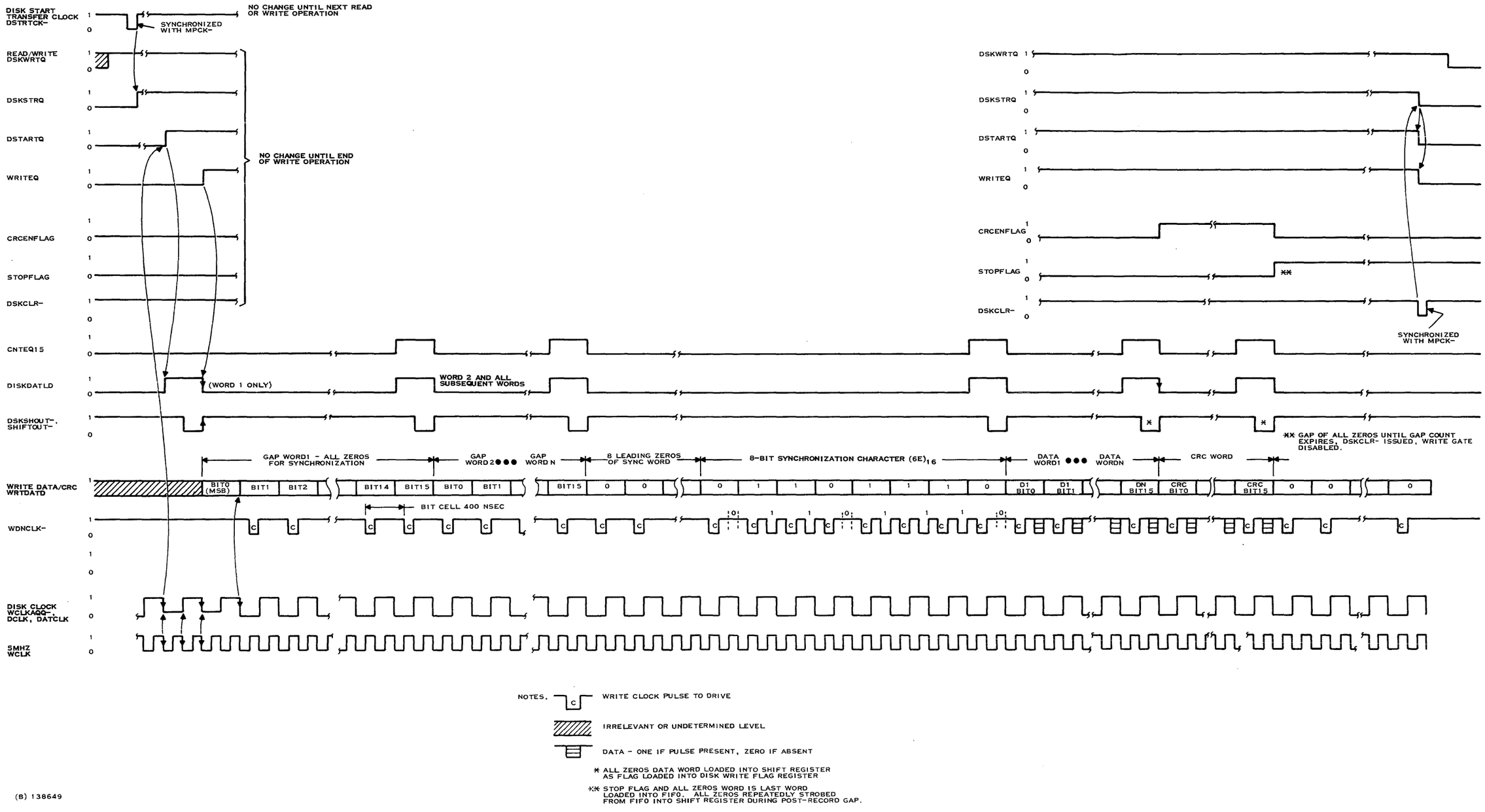
The period of the test clock waveform is approximately 1.2 microseconds (833.33 KHz). This corresponds to two microprocessor clock cycles with test clock on, and two cycles with test clock off. Test clock is slower than the normal (2.5 MHz) read or write clock due to the speed limitations of the TMS 3129 serial memory device.

Self-Test Logic. Refer to figure 2-54, which shows the read data and clock buffers, self-test logic, and disk clock distribution. The TESTCLK- signal from the microinstruction special group 1 decoder/register replaces the read or write disk clock (DCLOCK-) as the source for disk clock distribution.

For write test operations, the WRTDATOUT- signal from the write data encoding circuits is routed through the read 2 F/F (RDATAQ) and stored in the TMS 3129 shift register memory. TESTCLK- serves as the shift register clock.

During read test operations, the TESTMODEQ signal gates test data into the read 2 F/F again. This time, the output of the read 2 F/F goes through the normal read data path, through the disk data in F/F, and into the serial/parallel shift register.

If the controller microprogram detects a fault during self-test, it sets the diagnostic fault F/F, lights the FAULT indicator, and inhibits distribution of normal read or write disk clock. The DIAGFAULTQ- signal also holds the read 2 F/F in the reset state.



NOTES.

- C — WRITE CLOCK PULSE TO DRIVE
- IRRELEVANT OR UNDETERMINED LEVEL
- DATA - ONE IF PULSE PRESENT, ZERO IF ABSENT
- * ALL ZEROS DATA WORD LOADED INTO SHIFT REGISTER AS FLAG LOADED INTO DISK WRITE FLAG REGISTER
- ** STOP FLAG AND ALL ZEROS WORD IS LAST WORD LOADED INTO FIFO. ALL ZEROS REPEATEDLY STROBED FROM FIFO INTO SHIFT REGISTER DURING POST-RECORD GAP.

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Figure 2-59. Detailed Timing for Write Data Operation

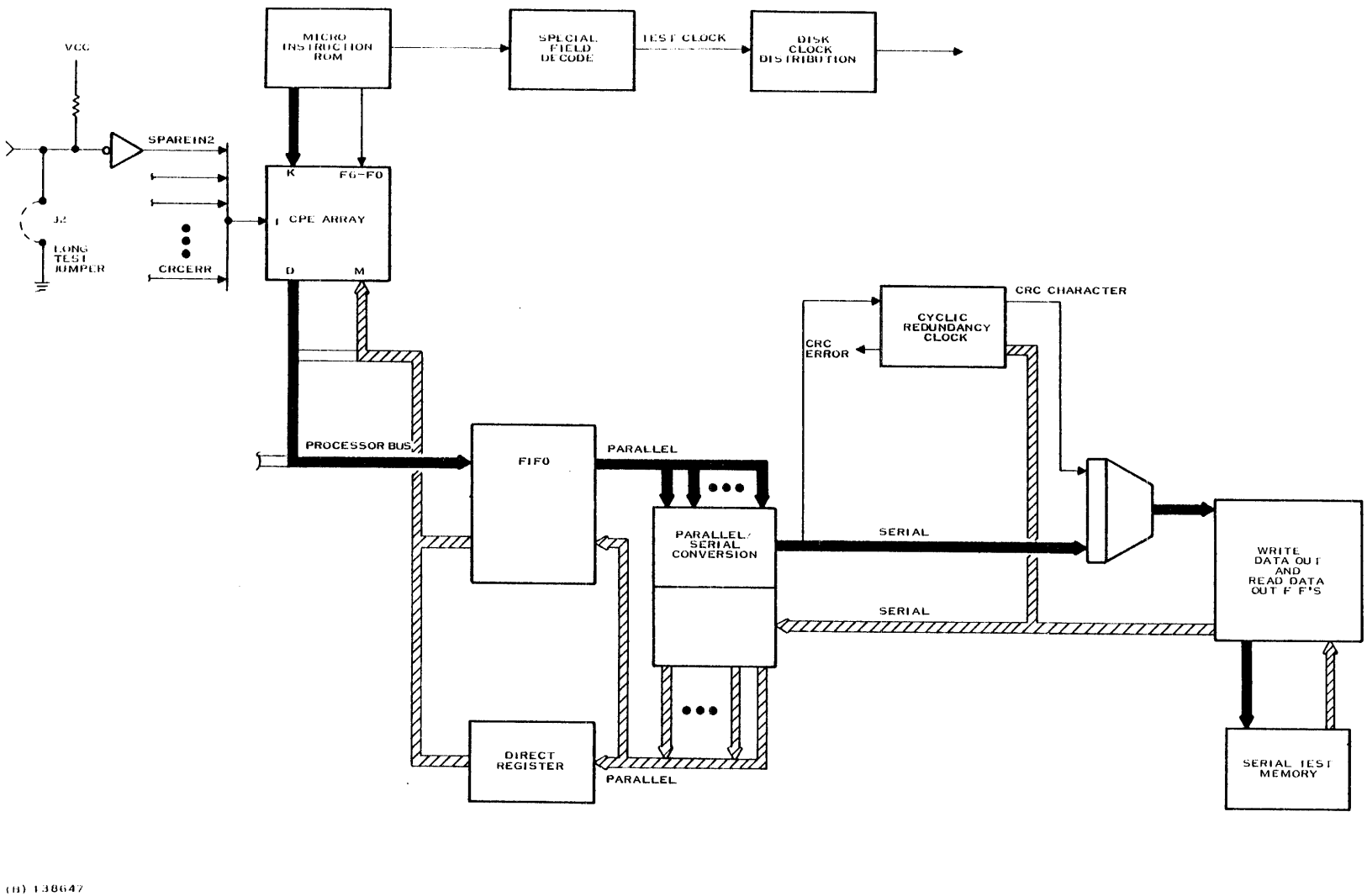


Figure 2-60. Controller Self-Test Data Flow

The DIAGFAULTQ- remains latched to prevent a faulty controller from writing data to a disk or reading from the disk. The test mode and diagnostic fault signals also serve as controller status inputs to the microprogram, via the CPE I-bus inputs.

To clear a diagnostic fault indication, a general reset (power reset or I/O reset) must be executed. The self-test is executed as part of the reset recovery, so if a hard fault exists, it will be detected again by the self-test, and read/write operation will be inhibited again.

Status Count and Status Update Strobe. The controller self-test uses CPE internal register R9 to maintain a status count. The status count starts at zero, and is incremented as various parts of the self-test are successfully completed. Thus the status count tracks the progress of the self-test.

When an error occurs, the test is aborted, but the status count is preserved. The count serves as a pointer to the last successfully executed test segment. The self-test microprogram flowcharts, at the end of Appendix D, are annotated with status count values at the points where they are updated.

Any error discovered during self-test steers the microprogram to the standard self-test error termination routine (Z error routine). This routine moves the status count from CPE register R9 to R2, where it is available for reading over the TILINE to the 990 CPU or the programmer panel (address F804 if CPU base address is F800). The error routine also places the status count on the processor bus so that it may be observed with a logic analyzer. It is also loaded into the disk address register. Table 3-3 in Section 3 is a summary of the self-test status counts and their meanings.

The error routine loads all ones (FF) into the right byte of R7 to identify a self-test error, and terminates.

The status update strobe is issued each time the status count in R9 is updated. An otherwise unused output, SPAREOUT1, from the microinstruction special group 1 decoder (logic drawing 937502, sheet 13, PWB, or 2262102, sheet 13, fine line), is used as the status update strobe. The SPAREOUT1 signal, or its complement, may be used as a synchronization source for a logic analyzer or oscilloscope.

Section 3 includes a detailed description of troubleshooting the disk controller with the self-tests.

SECTION 3

MAINTENANCE

3.1 GENERAL

This section describes depot-level maintenance for the DS10 Disk Controller when operating in a system with a 10-megabyte disk drive. Fault isolation procedures are given to the IC, gate or signal level. Detailed instructions for connecting the disk system to an operating 990 computer system, and general procedures for performing diagnostic test procedures are given in the related publications listed in the preface of this manual. Troubleshooting and repair procedures for the 10-megabyte, disk-drive units are contained in the *Peripheral Equipment Field Maintenance Manual,* and in *Control Data® Cartridge Disk Drive Model 94274 Hardware Maintenance Manual.* The program description document for the diagnostic test is drawing number 2250113-9901.

3.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the disk controller, in conjunction with the compatible disk drive units, is based upon the use of a hot mock-up system or an operating 990 computer and the use of the self-diagnostic capability of the controller board. Typical drive system components are listed in table 3-1. The interconnection for a typical hot mock-up system, based on the use of a Model 990 computer system, is shown in figure 3-1. In addition to the interface connector for the disk-drive units, the controller also provides a test connection that can accommodate a state display, or more sophisticated test equipment, such as a logic analyzer. A list of special test equipment is given in table 3-5.

3.2.1 STATE DISPLAY. The state display is a locally-manufactured item originally designed as factory test equipment. This state display is useful in troubleshooting and fault isolation. Local manufacture details are given in figures 3-2 and 3-3. Figure 3-2 is an illustration of typical front panel controls and indicators, and figure 3-3 provides a logic diagram of the unit. Figure 3-4 shows the interconnecting wiring from the test connector of the disk controller to the state display, along with signal names used in associated test procedures.

Table 3-1. System Components for Disk Controller and 10-Megabyte Disk Drive

Disk Drive System Components	Part Number
10-Megabyte Disk Drive	937513-00XX
50-Wire Cable	937516-0001
40-Wire Cable	937515-0001
Cable Adapter Board	937510-0001

Table 3-2. List of Special Test Equipment and Documentation

Equipment	Part Number
Double-Slot Extender Board	975170-0001
Scratch Cartridge	937507-0001
Drive System Components	Table 3-1
State Display	974846-0001

Table 3-2. List of Special Test Equipment and Documentation (Continued)

Equipment	Part Number
Logic Analyzer	Hewlett-Packard Type 1600A or equivalent
Dual Trace Oscilloscope	Tektronix Model 475 or equivalent
Diagnostics (under DOCS)	
Cassette	2250113-0001
Operating Procedure	2250113-9920 (OP)
Program Description	2250113-9901 (PD)
Fiche Kit (Depot)	2250113-0009 (SP)
DS10 PD, Linked Test	2250113-1006 (FLO)
Documentation	
Model 990 Computer Family Maintenance Drawings, Volume IV, Peripherals	945421-9704
Logic Diagram, 10-Megabyte Disk Controller	937502-0001 (PWB) 2262102 (fine line)
Model 990 Computer Peripheral Equipment Maintenance Manual	945419-9701
Control Data® Cartridge Disk Drive Model 9427H Hardware Maintenance Manual	937517-9701

NOTE

UG06 is the standard test connector provided on the disk controllers and is wired as shown in figure 3-4.

The state display facilitates gate-level troubleshooting of the controller in conjunction with TILINE interface controls, disk drive unit controls, and internal functions of the controller. The state board can provide the following functions:

- Clock stop
- Clock run
- Single step clock
- Locate breakpoint
- Loop on breakpoint.

The state display is connected to three clock functions of the controller:

- MPCKMNT is synchronous and simultaneous with the controller master clock (MPCK-)
- CLKT2- is delayed 20 nanoseconds from the master clock
- CLKRUN can stop the operation of the controller clock at any desired state by manipulation of the state display control switches.

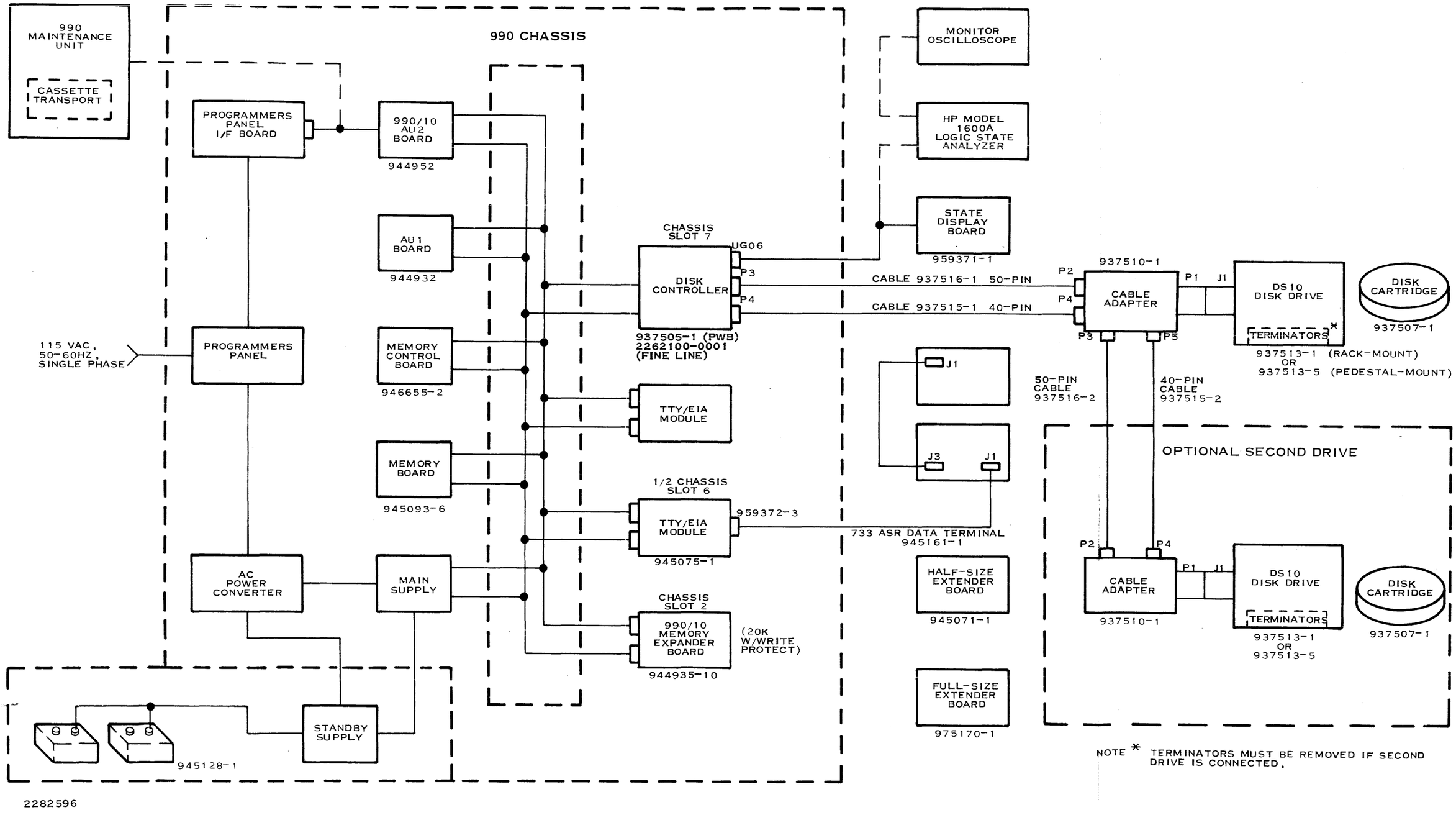


Figure 3-1. Typical Hot Mockup System for Disk Controller and DS10 Disk Drive

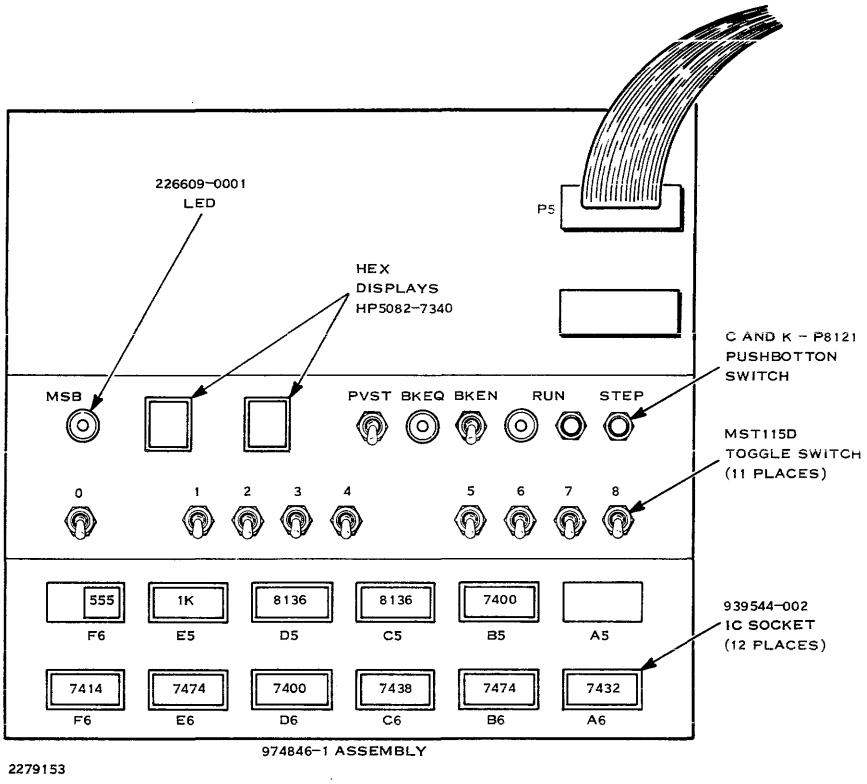


Figure 3-2. Typical Front Panel of State Display Board

Also, the nine bits of the microprogram address, MCUADR1-9, are connected to the state board where they are gated via bus comparators with individual toggle switches on the state display board. This feature allows the operator to locate the address of a particular state and to establish a breakpoint at any desired state. The output of the comparator logic can be used as a scope sync point when the controller passes through the selected microstate.

Referring to figure 3-2, the hexadecimal displays provide a combination of LEDs that correspond to the associated bit position of MCUADR2-9. (The indicator to the left of the LEDs is the MSB, MCUADR.) These indicators will indicate a significant microprogram address when the clock is stopped or when a breakpoint is reached in the program. The combinations of LEDs represent a hexadecimal number which is the microprogram address. This address correlates directly to the hexadecimal address of the microcode (Appendix E). By referring to the microcode for the selected address, the user can verify what each bit position should be for the corresponding 40-bit ROM control word, or the logic can be checked for correct conditioning in the selected state.

On the right of the state display are two pushbutton switches, labeled RUN and STEP. If the clock is running, pressing the STEP pushbutton will stop the clock. If the clock is not running, pressing the STEP pushbutton generates a single clock pulse. The RUN pushbutton, when pressed, starts the clock and lights the RUN lamp.

The nine toggle switches, labeled 0 through 8, control the breakpoint state. When a switch is up, it represents a 1 (high true); a down position represents 0 (low false). The desired breakpoint address is entered on the nine toggle switches, and the position of the BKEN switch controls the activation of the breakpoint. When the BKEN switch is up, the clock stops before the clock occurs for the next state. Depending upon the position of the PVST switch, one of two different states will be displayed by the hexadecimal displays, NEXT STATE or PREVIOUS STATE. When the PVST switch is down, the next state following the breakpoint state will be displayed. When the PVST switch is up, the state preceding the breakpoint state is displayed.

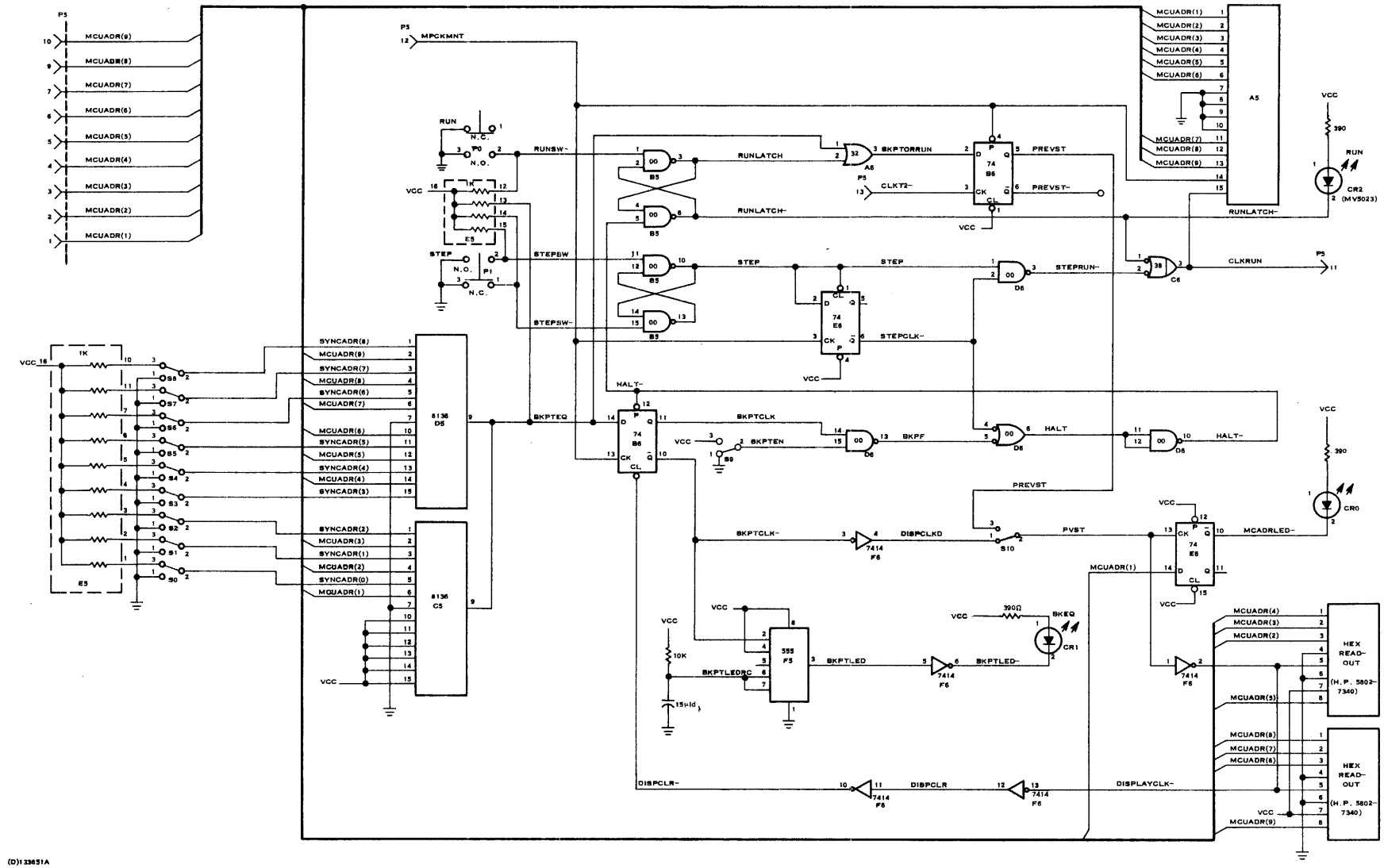


Figure 3-3. Logic Diagram of Typical State Display

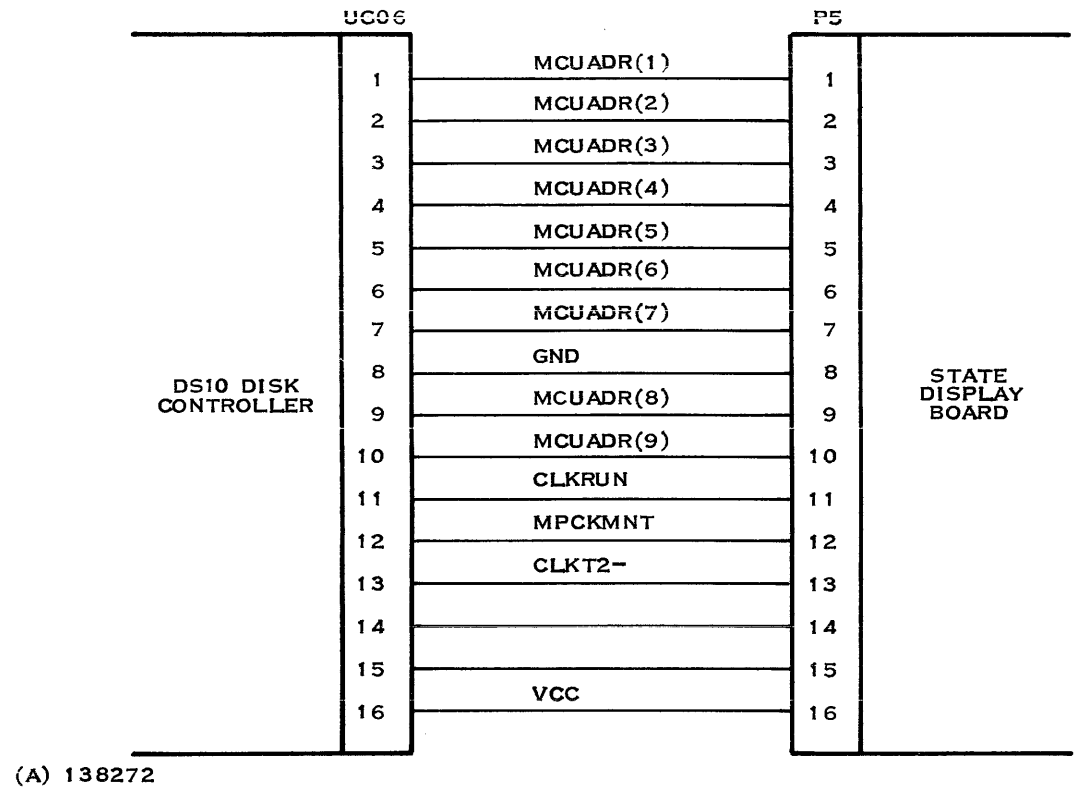


Figure 3-4. Controller to State Board Test Connections

If the BKEN switch is down, the clock will not stop when the current state equals the breakpoint state. But when this comparison occurs, and the PVST switch is down, the state following the breakpoint state is displayed. When the PVST switch is up, the display is continuously updated with each state except the breakpoint state. This is particularly useful if the controller hangs in an unknown state.

3.3 OPERATIONAL CHECKOUT AND FAULT DETECTION

As previously stated, the maintenance philosophy of this manual is based upon the controller operating in a 990 computer system. Therefore, before beginning any fault isolation procedures on the controller, all other items of the test station must be verified as being properly connected and in good operating condition.

3.3.1 PRELIMINARY CHECKOUT. Prior to beginning test and fault isolation procedures, perform the following steps.

CAUTION

Before connecting or disconnecting the power plug at the disk drive units, the power supply must be off. Also, be sure all power is removed from system components before installing or removing circuit boards or cable connectors.

NOTE

Details required for performing some of these procedures are given in the manuals listed in the preface.

1. Verify that the dual inline package (DIP) switches on the controller are set to the correct TILINE address positions as shown in Appendix A.

2. Verify that the jumpers are installed properly (figure A-6).

3. Verify that the correct interrupt level and access granted connections have been made in the computer chassis. Refer to *Model 990 Computer Model DS10 Disk System Installation and Operation.*

4. Using the double-slot extender board, install the controller on the extender in the designated computer chassis slot and install the interface cables as described in the installation and operation manual.

5. Remove the system disk, since it may have valuable data transcribed on it, and install a scratch disk to be used during test and troubleshooting.

6. Apply power to all equipment and allow a brief warm-up and stabilization period.

7. Bring the disk drive spindle up to speed so that the heads load. This is done by pressing the START/STOP button.

NOTE

Signal or gate-pin call-outs in the following paragraphs have double references. The first reference in the text will be followed by (PWB) referring to the PWB version of the disk controller. The second reference will be followed by (fine line) referring to the fine line version of the disk controller.

For additional information concerning the signal interpretation for the disk controller, consult Appendix B (PWB) and C (fine line) of this manual.

3.3.1.1 WHAT TO DO WITH A DEAD BOARD. If the controller is inoperative and does not respond to any manipulation of controls and switches, several actions are possible to localize the cause of the problem. Perform the following steps:

1. Pull out the controller (and/or extender board) and reinsert it in the chassis slot to assure it is properly installed.

2. Check that the DIP switches on the controller are set to valid positions as given in Appendix A.

3. Attach a scope probe to F08 pin 8 (PWB) or UDE083-8 (fine line) on the controller and verify that the microprocessor clock, MPCK-, corresponds to the pulse train of figure 3-5. Attach a scope probe to E09 pin 2 (PWB) or UBE028 pin 2 (fine line), and verify that the PBUSENL pulse goes positive 100 ± 5 nanoseconds after the rising edge of MPCK-.

4. Attach the scope probe to L10 pin 8 (PWB) or UHJ116-12 (fine line) on the controller and verify that the pulse train is symmetrical and matches the pulse train of figure 3-6. (This is the write oscillator clock, DSKOSC-.)

5. Check that each ROM is correctly installed in its socket; i.e., pin 1 in pin 1, etc.

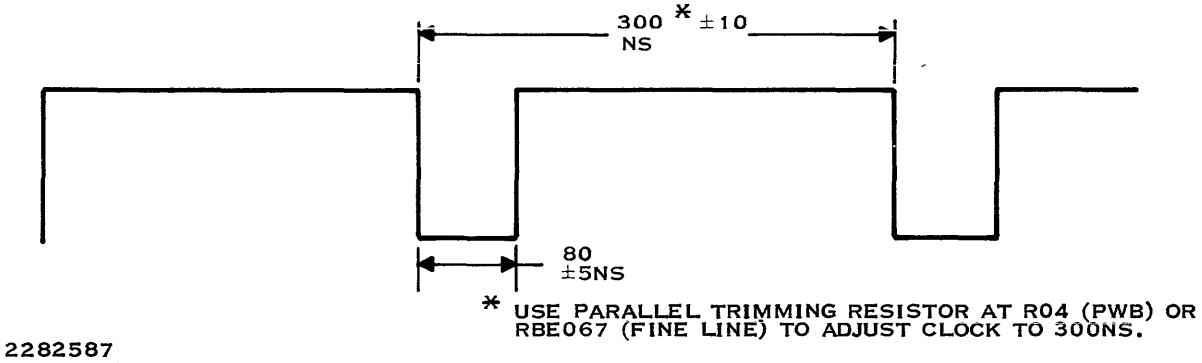


Figure 3-5. Pulse Train of Microprocessor Clock (MPCK- or MPCKMNT)

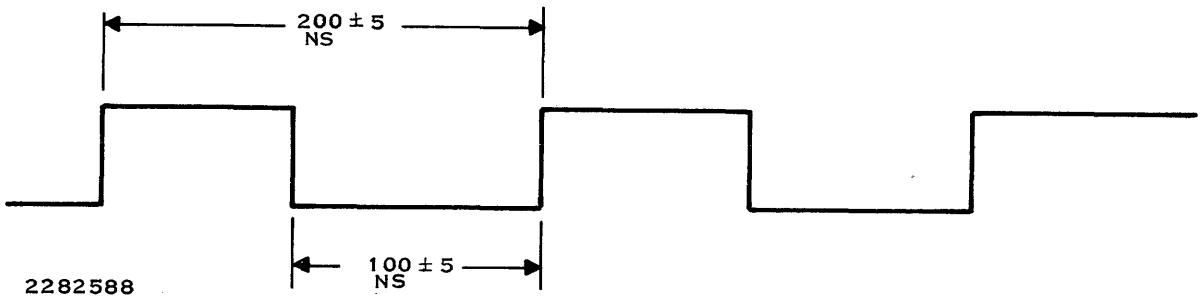


Figure 3-6. Write Oscillator Clock, DSKOSC

6. If the controller causes the computer memory to be inoperative, check all TILINE interface lines (data, address, control) for shorts and opens.

7. Verify that the controller is responding to the TILINE slave request and that an IORESET condition has been detected by the controller.

Use the programmer panel controls and indicators of the Model 990 computer to verify the following memory locations:

$F80E_{16}$ contains A100 or A900 (see note).

NOTE

If an IORESET condition occurred, A100 will be displayed in device register 7. A100 represents an idle bit, an error bit, and abnormal complete. If A900 is displayed, it indicates the lockout bit is set. (This happens after the first reading of device register 7.)

NOTE

If the state board shows that the controller is hung up in state 000, then check these signals:

TLPFWP- on A10 pin 1 (PWB) or UAK105-2 (fine line)
TLIORES- on A08 pin 7 (PWB) or UAE094-7 (fine line)
TLPRES- on E12 pin 12 (PWB) or UDE094-3 (fine line)

If these appear to be abnormal, pull out the controller circuit board slightly (after the power has been removed from the 990 Computer) and be sure the board and extender are installed in the correct guide slots and are properly seated.

Also, check the signal at A11, pin 1 (PWB) or UAK105 pin 1 (fine line) (CPUID) and ensure that it is a low for a 990/5, 990/10 or 990/12, and a high for a 990/9.

8. Using the state board, make sure the controller is executing the idle loop as given in the microcode listing and the flowcharts, Appendixes D and E. If the controller is functioning (as indicated by the address generator stepping through different states) but does not enter the idle loop, then most likely one or more of the ROMs is faulty. If practical, check the ROMs before substituting new ones and attempt to determine what caused the initial failure.

CAUTION

It is possible to install the ROMs incorrectly in their sockets. Be sure device pin 1 is inserted in socket pin 1 and that each device is fully seated.

9. If the controller is properly executing the idle loop, but fails to respond to slave commands, check the following signals.

ROM 16 on M11 pin 1 (PWB) or UEE006 (fine line) should be a logic high during the idle loop.

SLADOK on M09 pin 2 (PWB) or UAE028, UAE050, and UAE083 pin 9 (fine line) should go high when controller address is enabled onto the TILINE.

SLGODLY on M09 pin 3 (PWB) or UDK050-6 (fine line) should go high approximately 100 nanoseconds after TLGO is activated.

If these signals are not operating properly, trace the signals back through the logic until the problem is isolated. If these signals are functioning properly but the controller fails to execute a slave cycle, the slave logic should be probed and it should be verified that a trap is forced at the address generators. To verify this, trace the following signals:

SLVA- and SLVA
SLVB-
TRAP-
NRA(01-09)
MCUS(1-6)

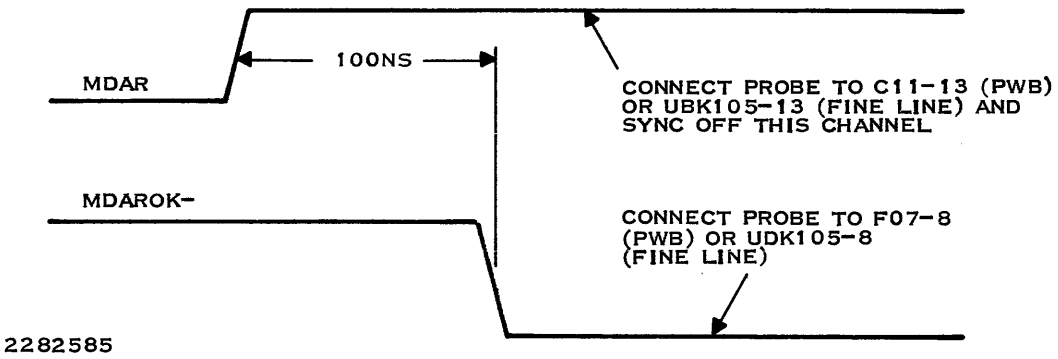
10. If the controller still does not work properly, check all lines on the MCUADR bus (MCUADR 1-9) for shorts and opens.

11. If the controller causes the TILINE to be inoperative, then the problem exists with the slave or master interface signals. Refer to the timing diagram, figure 3-8, 3-9 and use the logic diagrams to trace these circuits. If the problem seems to be caused by the controller when a master cycle is in progress but the command timer keeps taking the controller off the TILINE, then it may be advantageous to disable the TILINE timer so it stays in the hung state. To do this, ground the input pin on chip F07 pin 5 (PWB) or UBE105 pin 9 (fine line). This will prevent the timer from terminating the master cycle and thereby will allow us to probe the interface signals. Be sure to check the address and data lines as well as the control signals.

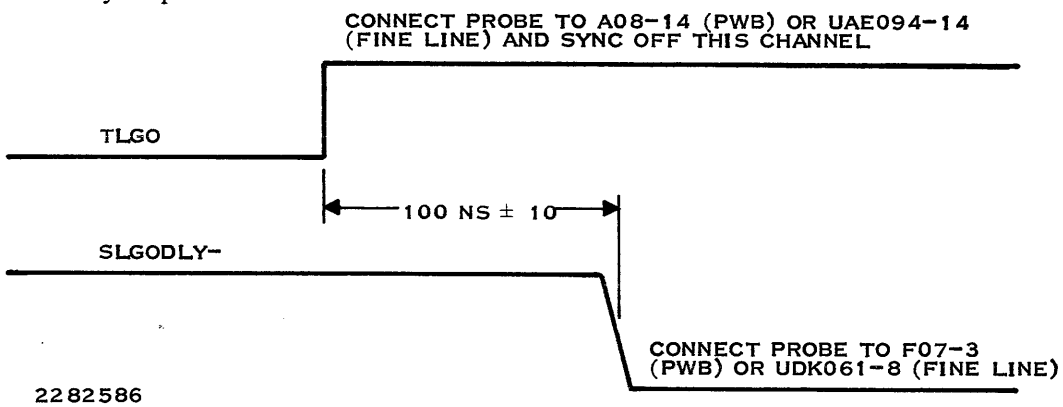
3.4 MASTER/SLAVE TIMING ADJUSTMENTS

Once the controller is able to do master and slave cycles, the following signals should be checked to insure that the delays associated with TILINE activity are of proper duration.

1. Check the delay of MDAR by monitoring the signals as shown in the figure below.



2. The delay to start the slave cycle should also be checked to insure that enough time is allowed for the address to be decoded and become stable before the compare results are sampled. To check this delay, probe the signals as shown below and insure that the proper delay is present.



3.5 GENERAL FAULT AND CORRECTION ANALYSIS

The trouble shooting philosophy of the next two sections revolves around the use of the self-diagnostic capability of the controller and LED status indicator interpretation. The use of the diagnostic test in finding problems is explained in paragraph 3.7. This section uses the error messages of the tests to aid in finding the problem. Examples of error message printouts are explained to help find the problem, along with the use of commands, built-in memory and the use of the various verbs. In both sections, certain basic practices for fault isolation should be observed, as described in the following paragraphs.

This paragraph contains descriptions of various types of faults and presents suggestions for quick isolation and correction. In the troubleshooting procedures, each fault is described, and the logical checks are indicated. The normal operating conditions at each checkpoint are described. When one of these conditions is not met, the signal exhibiting the failure should be traced until the fault is found, which will usually be one of the following types:

- A bad IC
- Broken component lead

- Cold solder joint
- Broken wire on circuit board
- Short between circuits
- Poor connection or broken pin at connector
- Loose wire or lead
- Bent pin in IC socket
- Loose IC in socket

In all cases where signals, signal levels, or voltages are direct inputs from interconnecting cables, sockets, plug-in circuit boards, etc., make sure the signal level meets the threshold values and is within tolerance. In other words, do not use a logic probe to simply detect the presence or absence of a high or low signal, but use an oscilloscope (with calibrated voltage) to ascertain that the signal level is the correct value and within tolerance.

Once a specific error has been diagnosed, the first step is to make sure that the error is in the controller and not in the cable or disk drive. In some cases, this is not directly or immediately possible.

The second step is to start at a point known to be in error and then work backwards until the error is no longer present. The cause of the error is then between the last two points checked. Further isolation is accomplished by probing all inputs to that location. If one of the inputs is at the wrong logic level or not within the specified normal operating voltage range, this signal should be tracked backwards until the problem is found. Once the final source of the problem is located, further actions should be a matter of replacing a chip, repairing a solder joint or solder bridge, etc.

3.6 SELF-DIAGNOSTIC TROUBLESHOOTING

3.6.1 GENERAL. The controller has the built-in capability to perform various tests on itself to check for faulty conditions that may exist on the controller. There are two forms of self-test on the controller. The short test is run every time a command is issued to the controller (goes out of the idle state). The long test is executed every time the controller does a STORE REGISTERS command or a level 0 interrupt (I/O Reset, Power Reset or Power Fail Warning). The long test is only executed on level 0 interrupts provided a special jumper is installed at J02 (PWB) or UKC038 (fine line) on the controller. If this jumper is not installed, an interrupt level 0 will not run any self diagnostics and will set the appropriate status bits and enter the idle loop in the controller. This jumper is normally not installed and will cause problems if left in when the controller is installed in an operating system. The short test is included within the long test. The long test adds a CPE register test and causes the controller to do a command timer check. This adds approximately 200 milliseconds to the cycle time of the controller self-test.

3.6.2 INTERPRETING SELF-DIAGNOSTIC STATUS. For purposes of this example, the controller will be set up to operate at TILINE slave address F800. Any other address possible can be used as long as special attention is given to the address assignments.

Register 2 within the CPE (TILINE address F804) is used to report self-diagnostic status. When the controller is running the self-diagnostic test, a status bit is added to register 9 every time the controller successfully completes a portion of the test. When an error occurs, the self-diagnostic aborts all further testing, sets certain status bits, and returns to the idle state. The status count developed in register 9 is put in register 2, so it can be read by the computer to be printed on an ASR, displayed by a CRT, or shown on the front panel.

When a STORE REGISTERS command is completed successfully, register 2 (F804) will be all zeros. When an interrupt 0 completes normally, a value of FF00 will be displayed in Register 2. When an error is encountered on interrupt 0, the controller clears the FF bits in the left byte and loads the status count in the left byte. Whenever a normal command is executed, the contents of register 2 remain unchanged unless an error is detected and the command is aborted. Again the status count will be loaded into register 2 when this happens. In addition to setting the status count in R2, the controller puts all ones (FF) in the right byte of register 7 (R7). Whenever the system operator notices an error in the system and the controller status register has all ones in the right byte, he should note the status count in register two (R2) and use this to help solve the controller problem.

A listing of the possible self diagnostic failures is given in table 3-3. The status count will be different between the long and short test because of the different tests involved and the different sequence. Special attention should be given when interpreting the status chart. The type of operation which causes the error must be known so the proper column of status counts can be read (long test or short test).

NOTE

Once a self diagnostic error is detected, a fault latch is set. At the beginning of each command, when the controller enters the diagnostic routine, a check is made to see if the diagnostic latch has been set by a previous error. If the latch has not been set, the diagnostic test will start executing; but if the latch had been set previously, a check is made to see if the command is anything other than a STORE REGISTERS command. If the command is STORE REGISTERS, the diagnostic test will be executed, but if it is any other type command, the diagnostic test and command are aborted and the controller goes back to the idle loop. When a level 0 interrupt trap is detected, the command register (R1) is cleared to all zeros, forcing a STORE REGISTERS command. This means that the only way to execute the self test or clear the diagnostic latch is to either do a STORE REGISTERS or to give the controller an I/O Reset.

Table 3-3. Status Error Decode

STORE REGISTERS OR LEVEL 0 INTERRUPT FOR LONG TEST

Status Count		
Short Test	**Long Test**	**Decode**
NA	0001	The CPE chips have successfully written and have read back a pattern of all FIVES in the internal registers.
NA	0002	The CPE chips have successfully written and have read back a pattern of all A's in the internal registers.
NA	0003	The CPE chips have successfully right-shifted a bit down the AC register and have obtained a right-out at the proper time.

Table 3-3. Status Error Decode (Continued)

STORE REGISTERS OR LEVEL 0 INTERRUPT FOR LONG TEST

Status Count		
Short Test	Long Test	Decode
0001	0004	The CPE chips have successfully left-shifted a bit down the AC register and have obtained a CARRY OUT at the proper time.
0002	0005	The controller loaded the FIFO with header information using data patterns of fives, A's and zeros. It also checked to assure that the FIFO was not available when it was full of data.
0003	0006	The ability to toggle the start latch and read it on the I-bus has been successfully tested.
0004	0007	The FIFO has been cleared and has been put in the read mode. The FIFO available has been checked to assure that it is not available. The ability to set latch TESTMODEQ and detect it at the I-bus has been assured.
0005	0008 1ST HEADER	The test clock has been pulsed until sync should have occurred. The detection of the sync character which sets the READQ was checked on the I-bus. Also, the FIFO was checked to assure that it has not become available yet.
0009	000C 2ND HEADER	
000D	0010 3RD HEADER	
0006	0009 1ST HEADER	The test clock has been pulsed until a word has been loaded into FIFO. The FIFO available has been then checked to see that it has become available. The CRC error flag was checked to verify that it was not set. The first two words of the header have gated out of FIFO and the third word (all 5s) has been compared with all A's in the AC. The resultant has been stored in the AC.
000A	000D 2ND HEADER	
000E	0011 3RD HEADER	
0007	000A 1ST HEADER	A check for miscompares of any data bits of the third header word has been made. The rate error flag has been checked to see that no rate error has occurred during the unload.
000B	000E 2ND HEADER	
000F	0012 3RD HEADER	
0008	000B 1ST HEADER	The CRC character has been pulled out and a check has been made to see that a CRC error or a rate error has not occurred.
000C	000F 2ND HEADER	
0011	0013 3RD HEADER	

Table 3-3. Status Error Decode (Continued)

STORE REGISTERS OR LEVEL 0 INTERRUPT FOR LONG TEST

Status Count		
Short Test	Long Test	Decode
0011	0014	The direct register has been loaded with ones. The data stored has been compared to the AC data and the resultant stored in the AC. The READY direct latch has been checked to see that it became set.
0012	0015	A check on the comparison of the ones loaded into the direct register has been successful and the ability of the READY direct flag to be cleared has been assured.

NOTE

The following is not applicable to the short test.

If an error occurs after status 0015 above is reported the following items are checked by the controller.

1. The contents of the direct register is tested to assure that it will pass a pattern of all zeros.

2. The Ready direct latch is checked to see that it clears when the Ready Direct reset is issued.

3. The command timer along with the interrupt logic is checked for proper operation. This is done by putting the controller in a delay loop that is longer in duration than the command timer. When the command timer times-out, it forces a vectored interrupt to the command timer interrupt routine. This routine tests whether the controller is in the test mode. If the controller is found to be in the test mode, the test mode latch is reset and the interrupt routine branches back to the diagnostic routine. The controller then checks to see if test mode has been reset by the interrupt routine. If it has, it takes the controller out of the diagnostic routine and goes through the terminate routine and into the IDLE state. If test mode is not cleared the controller branches to the error routine because the count must have been completed before a command timer occurred.

3.6.3 HARDWARE INDICATORS. There are four light emitting diodes (LEDs) on the top right corner of the controller. These indicators can be used when troubleshooting the controller to give some idea of what it is doing or what may be wrong. The LED configuration for each disk controller version is illustrated in figure 3-7.

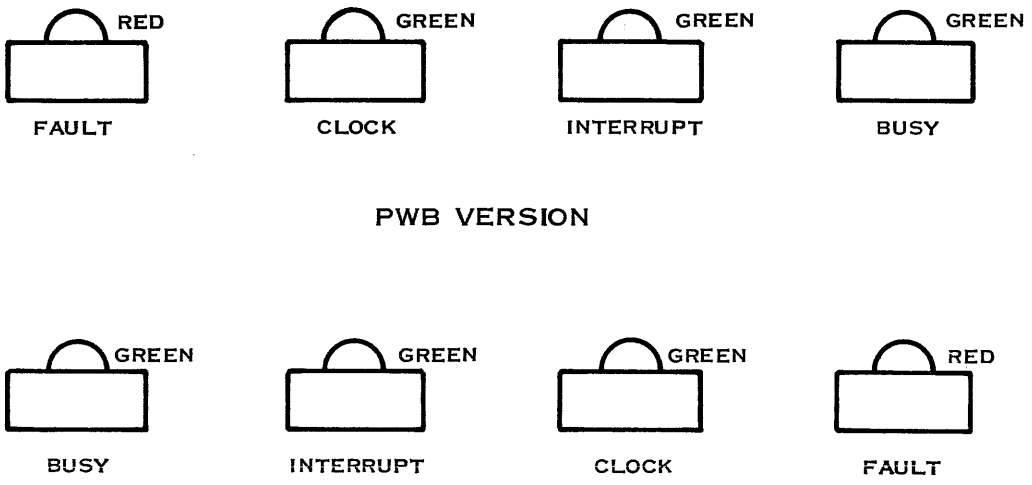


Figure 3-7. Disk Controller LED Configuration

The following description of each LED should be used to interpret controller operation.

3.6.3.1 Clock LED. The clock LED is used to designate the state of the controller clock circuitry. There are three distinct states that this LED could indicate:

- OFF — Light extinguished
- ON — Bright, clock hung in ON state
- RUNNING — Dimly lighted, showing that the clock is running.

3.6.3.2 Busy LED. This LED is used to tell when the controller is executing a command. When the light is off (extinguished) the controller is not executing any commands and is in the idle loop. When the controller is executing a command, the busy light will illuminate and stay on until that command is terminated, at which time it will become extinguished again.

3.6.3.3 Interrupt LED. This LED is used to display the state of the interrupt line from the disk controller to the 990 computer. When this light is on (illuminated) the controller has issued an interrupt to the computer. This light will stay on until the interrupt condition is reset by the computer.

3.6.3.4 Fault LED. This LED is used to display two different things. This light will be turned on by the command timer reaching its maximum count. When this happens, the LED (red) will be illuminated and will remain on until cleared by proper sequencing through the microcode terminate routine. This LED is also set (illuminated) at the beginning of the self diagnostic test and cleared (turned off) at the successful completion of the diagnostic test.

3.6.4 FAULT ISOLATION USING LED INDICATORS. If the controller seems to be dead and will not run, a quick check of the LEDs should be made. The first thing to note is the state of the controller clock. If the clock LED is OFF or constantly ON without toggling, then there may be a problem with the clock circuit or the associated control circuitry. If the LED is always ON, an oscilloscope should be connected to chip location F08 pin 6 (PWB) or UDE083-6 (fine line) (clock on) and the level or waveform checked. If this signal is a constant logic high, the loop should be traced until the fault is found. This circuitry is shown on the 10-megabyte controller logic drawing (number 937502, PWB, or 2262102, fine line). If the clock LED is always OFF, the clock inhibit signal at F11 pin 4 (PWB) or UCE072 pin 4 (fine line) should be checked and if high, it should be traced backwards through logics until the reason is found.

3.6.5 FAULT ISOLATION USING SELF-DIAGNOSTICS. How to use the self diagnostics for fault isolation is explained in this section. For test purposes, the jumper at J2 (PWB) or UKC038 (fine line) will be installed and the long diagnostic test will be used for testing. The first thing to be done when troubleshooting in this mode is to issue an I/O Reset to the controller, causing it to execute the self-test. This is done by pushing the RESET switch on the front panel of the computer.

After that, register 2 in the controller should be read for its status count. This is done by entering F804 on the front panel and then depressing switches MA, ENTER and DD. The contents of register 2 should be displayed in the front panel (provided controller was assigned to address F800). The value displayed gives a status count that had been reached before the diagnostic test was aborted. The count reached was the last successful test to pass so the next status count description from table 3-3 describes the failed segment. If status register R2 contains a count of FF05, then the error occurred in status test 6 and the description listed in table 3-3 should be read. This description should give a good idea of what the controller was trying to do when the error occurred; thus, the logic circuitry to start probing should be identified. A more detailed description of what the controller was executing at the time of the failure may be obtained from the self-test flowcharts.

NOTE

The status count loaded into register 2 of the controller is also loaded into the Disk Address Register (D-bus). These lines are labeled ADD(01-256) in the logics (sheet 14) and can be probed with an oscilloscope to determine the error count if a front panel is not available or is inoperative.

Every time the status count is updated, the controller toggles an otherwise unused control line, SPAREOUT1- at R04-2 (PWB) or SPAREOUT1 at UJD061 pin 4 (fine line). This is done to provide a sync point to aid in the troubleshooting of the controller. These pulses may be counted following RESET to determine the error count.

By tracing through the diagnostic subroutine titled Z Diagnostic Test (ZDT) listed in Appendix D, a detailed account of tests is given. It should be noted that the status count is updated in the Z status update (ZSU) subroutine. The status count made by each update is shown. This allows the test personnel to skim through the flowcharts until the desired status count is found. Then a detailed analysis of the failing test can be made.

A good troubleshooting method is to use the state board to breakpoint to the starting address of the diagnostic test where the error occurred. Once this has been done, the clocks can be single-stepped and the erroring hardware can be probed for proper sequence, levels, etc. To do this, the command timer interrupt and TILINE timeout interrupt must be disabled.

If a scoping loop is desired while the logic signals are probed, the following command may be entered on the front panel. This set of commands will issue an I/O Reset, poll the controller until it goes not busy and then issue another I/O Reset and continue in this loop until halted by the HALT/SIE switch on the front panel.

Memory Address	Data	Comments
6000_{16}	0360_{16}	Issue an I/O Reset
6002_{16}	0201_{16}	Load W1 with delay count
6004_{16}	$FFFD_{16}$	Delay count
6006_{16}	0581_{16}	Increase count by one
6008_{16}	$17FE_{16}$	Jump if no carry back one
$600A_{16}$	$C093_{16}$	Load disk status in W7
$600C_{16}$	$0A12_{16}$	Shift W2 left one place
$600E_{16}$	$18F9_{16}$	Jump on carry to 6000 (Idle Set)
6010_{16}	$10F9_{16}$	Jump unconditional to 6002
7004_{16}	0000_{16}	Disk status register
7006_{16}	$F80E_{16}$	Disk status address

Put 7000_{16} in workspace pointer (WP)
Put 6000_{16} in program counter (PC)

Once this information has been entered, the RUN switch should be pressed and the computer will start executing.

3.6.6 CHECKLIST FOR EACH STATUS COUNT IN THE LONG DIAGNOSTIC TEST. The following paragraphs give a list of places to probe for each possible error status observed in the long diagnostic test.

3.6.6.1 Status Count FF00 (R2) and R7 Right Byte is FF. This indicates that the CPEs failed to write and read back (compare) a data pattern of fives. The following items must be checked:

- Each CPE has a good clock signal pin 18 of each chip
- Check I bus (pins 1 and 2) on each CPE and assure that alternate 1's and 0's are present
- Check ROM 12 (carry in) on CPE C02 pin 10 and on look ahead carry logic D07 pin 13 (PWB) or UCC021, UAK006 (fine line).
- Check all the X, Y inputs from the CPEs into the look ahead carry logic chip D07 and C07 on logic sheet 12
- Check TESTBITQ for proper level
- Check ROM bits 1-7 (function decode) on each CPE for proper level.

3.6.6.2 Status Count FF01 (R2). This status count indicates that the CPE failed to write a pattern of A's in the registers and to read back (compare) this data. This is the complemented data pattern of the previous paragraph, so all troubleshooting steps of the previous paragraph (3.6.6.1) should be repeated.

3.6.6.3 Status Count FF02 (R2). This test puts a 1 in the MSB (bit 00) of the CPE accumulator and all zeros in the rest of the bit locations. The controller then does right shifts and checks to see that a right shift out (ROR) occurs at the proper number of shifts. The following fault isolation procedure should be followed:

- Insure that the right output is passed from one CPE to the next via the left input (LI).

NOTE

It will take two shift pulses to pass the bit from the input to the output of each CPE (RO is pin 8, LI is pin 9).

- Ensure that the bit is passed across byte boundaries properly. Check signal ROL- on E07 pin 4, 5 and 6 (PWB) or UDE050 pin 4, 5, and 6 (fine line), and verify that it is gated to the output (LIR-) at pin 7 of that chip and goes to the left input of the right byte MSB.

Again the right shift output should be traced through the right byte. The final output (ROR-) should then be traced through the look-ahead carry circuitry. Check chip E07, pin 9 (PWB) or UDE050 (fine line), and assure that it goes high at the appropriate time. Ensure that this signal is passed through chip D08 (PWB) or UAK072 (fine line) (logic sheet 12) and is negative at pin 9 (TESTBIT-). Check signal (SHFCMD) at E11 (PWB) or UCE072 (fine line) pin 1, on logic sheet 12, and verify that this signal is high during the shift command, thereby disabling the normal carry logic for the shift operation. Insure that this signal becomes latched by chip M09 (PWB) or UBK072 (fine line) (TESTBITQ). If the levels and signals all look good but the controller is still reporting an error, the problem is probably associated with the MCU address decode. Probe the lines of the address generator (MCU) chips at G09, G10, and H09 on the PWB version or UHJ006, UHD006, and UGE006 on the fine line version of the disk controller for shorts and opens.

3.6.6.4 Status Count FF03 (R2). This section of the diagnostic test checks the ability of the CPEs and support circuitry to do a left shift and get a carry out at the desired time. The test is accomplished by loading a shift count in the T register. Then starting with data of 0001 in the accumulator, the data is added to itself, thereby doing a left-shift. The count is decremented on each shift, and if a carry out is obtained before the count has gone to zero, an error is reported. Likewise, if a carry out does not occur at the expected time, an error is reported.

To isolate this problem, the following items should be checked:

- The look ahead outputs of each CPE should be checked (pins 5 and 6).

- The first stage of the look ahead carry should be probed for proper values. These chips are located at C07 and D07 on the PWB version or UAK050 and UAK006 on the fine line version of the disk controller. The carry outputs (CARRY0- through CARRY6-) should be traced to CPE carry in input pin 10 and verified to be good.

- The second stage of the look ahead carry should be probed next. This stage comprises the chips located at C08 and C09 (PWB) or UAK061 and UAE072 (fine line) on the controller.

- The third and last stage of the look ahead carry should be checked. Special attention should be given to output signal CIL-. This signal feeds back to first stage to connect byte boundaries and also goes to the least significant bit of the left byte (CI).

- If the problem has not been discovered by this probing sequence, the CPE input function code and the microprogram address generator (MCU) function generation should be checked.

3.6.6.5 Status Count FF04 (R2). In this test, the controller puts a data pattern of all 5's in CPE register eight and calls the write header routine. This routine loads the sync character into FIFO along with the contents of registers R3, R2 and R8 (5's). The contents of R8 are complemented and the write header routine is called again. After this, register 8 is cleared and again the write header routine is called and five more words are put in the FIFO. The controller then loads a word of zeros into the FIFO, filling it to its maximum capacity (16 words). The controller then checks the FIFO available status to see if it is available. The status should show that FIFO is not available because it has been filled with words.

To troubleshoot this problem, the following items should be checked:

- On logic sheet 16, probe the output signal at chip K02 (PWB) or UFE061 (fine line) pin 6. This signal (INRDY-) should go high and stay high after the 16th word was loaded into FIFO. If this signal is high at microprogram address (logic state) 196 (ZDT12), but an error is reported, then this signal should be traced to find why the wrong status was reported. Check chip L02 (PWB) or UFK072 (fine line) input pin 3 and output pin 4 for proper levels. If output pin 4 (RDYSTATUS) is high (good) then the signal should be traced through the I-bus latch (sheet 16 of logics). If the output of the I-bus latch, J05 (PWB) or UAK039 (fine line) pin 15, is high (good), then the signal should be checked at the input to the CPE chip located at C03 (PWB) or UCC036 (fine line) pin 1. If the input is high but the controller is detecting an available condition and going to the error status routine, then the function bits and K-bus signals should be checked for that chip (C03) (PWB) or UCC036 (fine line).

- If K02 (PWB) or UFE061 (fine line) pin 6 (INRDY-) remains low after the 16th word was loaded into FIFO, then some or all of the FIFO devices did not load the words properly. By checking the input pins to this gate, it can be determined if the problem is one or all FIFO devices. If all inputs are high, then all FIFOs failed to input the words properly; but if just one or two are high, then part of the FIFOs loaded properly. If one of the FIFOs is always ready, then that chip may be bad or one of its input signals may be bad. If all the inputs to chip K02 (PWB) or UFE061 (fine line) were high, then the most likely problem would be the input control circuitry. Check the following signals on the FIFO logic (sheet 17 in logic diagrams):

  DSKCLR-. This signal should remain high while words are being shifted into FIFO.

  DSKDIRECT-. This signal should remain high during this portion of the self test. This signal will only become active (low) when the diagnostic direct register test is being executed or when the controller is executing a verify ID command.

SHIFTIN. This pulse causes the data on the input to be loaded into FIFO. This signal should be a string of 16 pulses if monitoring it on an oscilloscope. If the signals are not present, the signal should be traced back and the operation of the P-bus destination decoder should be carefully scrutinized.

SHIFTOUT. This signal is used to pull words out of FIFO on each pulse. During this portion of the self-diagnostic test, no pulses should be occurring. If they exist, then the reason for the pulses should be traced down and the problem corrected.

3.6.6.6 Status Count FF05 (R2). This test checks the ability of the controller to turn on the start circuitry used to activate the disk sequencing. This start signal is selected by a microcode command, and the disk clock (DCLK) is used to synchronize the controller start command to the disk clock. The DSTARTQ signal is first checked to see that it is not active, then the start command is issued and the test clock is pulsed. When the test clock is pulsed, the DSTARTQ flip-flop becomes set and the status at the CIE I-bus becomes active (high). While the test clock is pulsing, the data in the FIFO is shifted out and put in a special serial shift register (test memory). At the completion of the test clock pulse sequence, the controller checks the DSTARTQ signal to see if it has become active and gone high. If this signal is correct, the controller goes and starts the next test. If this signal is wrong, the test is aborted and the status count is loaded into R2. If this test should fail, the following should be checked on the controller:

- Check the start latch at R11 (PWB) or UJJ116 (fine line) on the controller (logic sheet 14). Output pin 9 (DSKSTRQ) should go high during this test. If it fails to do so, check R11 (PWB) or UJJ116 (fine line) pin 13 (DSKSTRTR-). This signal should be a logical high level during this portion of the test. Check R11 (PWB) or UJJ116 (fine line) pin 11 (DSKSTRTCK-). This should pulse when the start command is given in microcode.

- If the latch at R11 (PWB) or UHJ094 (fine line) (logic sheet 14) has become set, then the next stage (synchronization) should be probed. Check R11 (PWB) or UHJ094 (fine line) pin 2, which should have been set to a logic high by the start command. If pin 2 was high, then check pin 3 to ensure that it pulses during the test portion. This signal is generated by the controller during self-test to simulate a disk clock. This signal should be 600 nanoseconds on and 600 nanoseconds off. If no clock pulses are occurring during this portion of the test, scope chip N08 (PWB) or UJD105 (fine line) pin 5 (logic sheet 19). While in the self-test, this signal (DCLOCK-) should always be high and the clock signals should be gated on N08 (PWB) or UJD105 (fine line) pin 4. If no clock pulses are occurring at this point, the generation of the TESTCLK- signal should be checked at chip H11 (PWB) or UFK050 (fine line) pin 5 (logic sheet 13) and all input signals should be probed until the fault is isolated.

- If R11 (PWB) or UHJ094 (fine line) pin 5 (DSTARTQ) went high as intended, then the input to CPE chip E03 (PWB) or UBE036 (fine line) pin 2 should be checked. If this signal is high and controller still makes the decision of not being in the start state, the input function pins should be checked and the look ahead carry and address selection logic should be checked.

3.6.6.7 Status Count FF06 (R2). This portion of the test checks several things. The controller issues a disk clear command which turns off the disk circuitry and also clears the FIFO of any data that may be stored in it. The controller then puts itself in the test mode. This allows data from the serial register to be gated through the read data circuitry and put in the serial/parallel shift register. The controller also clears the disk write logic, thereby putting it in the read mode.

The first thing the controller checks is the FIFO available status. The status should show that the FIFO is not available. It should be not available in the read mode because the disk clear should have cleared all words and ready flags in the FIFO. The controller next tests the status of TESTMODEQ to see that it was set properly when the command was issued. For troubleshooting purposes, which test failed must be determined before the fault isolation process can be started. The test person should use the state display board or a logic analyzer to determine the failing test. An address of 1A3 should be set as the breakpoint and the address following this will show which of the failures occurred.

If the next MCU address is 1C9, then the FIFO available test failed and this circuitry should be probed. If the next MCU address is 1A0, then the controller reported an error in the test mode status check.

If the failure was caused by FIFO available status failure, then the following should be checked:

- DSKCLR-. Check this signal at chip K03 (PWB) or UFE072 (fine line) pin 18 and insure that the signal pulses low during this portion of the test. If it fails to do so, trace back through the logics until problem is found. If this signal is good, then the output (ORDYA-D) flags of the FIFOs should be checked and traced until problem is isolated.
- If the failure was caused by test mode status not being set, check signal TESTMODEQ at E04 (PWB) or UBE051 (fine line) pin 1 (logic page 9). This signal should become a logical high during this portion of the test and remain on for most of the remaining diagnostics.

3.6.6.8 Status Count FF07 (R2). In this portion of the self diagnostics, the test clock is pulsed a number of times and the FIFO available is again checked to see if any words are available. No sync character should have been detected so no words should have been loaded; thus, FIFO should not be available. The controller branches to the diagnostic read header routine. In this portion of the diagnostics, the disk interface is activated (DSKSTRT) and test clock is pulsed again. After the test clock was pulsed the READQQ- signal is checked to see that the sync character was detected and the read circuitry was turned on. The FIFO ready status is again checked to insure that no words have been loaded into the FIFO.

In troubleshooting this test portion, which failure caused the error must be ascertained before fault isolation can begin. Use the state board or logic analyzer to determine where in the code the error occurred. Breakpoint on address 1A3 and check what the following address is. If the next address is 1C9, then a FIFO available error occurred. Next, breakpoint on address 1DD and check the next address that it is going to. If it goes to address 1C9, then the error was caused by a sync pulse not being detected properly. If the next address is 1DE, then the error reported was caused by a faulty FIFO available status. Once the type of error has been determined, the items described in the following paragraphs should be checked.

If the error was caused by FIFO available showing that a word has been loaded into FIFO and the word was available on the output, the most likely cause of the problem is the occurrence of an extra, unwanted SHIFTIN pulse. Before pursuing this investigation, check the ORDY(A-D) signals to assure that a word was loaded and that the problem was not caused by an error in sensing the proper status.

If the problem was caused by not detecting a sync character and getting the interface activated, the following items should be checked:

- Check L11 (PWB) or UFK127 (fine line) pin 3 (TESTDATA), logic sheet 19, to insure that data is shifted out when TESTCLK- is pulsed. If no data changes occur, trace the input back until the cause of no write data is found. If there is data being shifted out of this register, trace this data through the read circuitry and into the serial/parallel register. Insure that this data is shifted properly through this register (logic sheet 17). If this register is working properly, then the sync character decode circuitry on logic sheet 14 should be checked. Monitor chip N02 (PWB) or UJD083 (fine line) pin 8 (SYNC6E) and see if it goes low. If it does, this signal should be traced by monitoring SYNCQ-, N12 (PWB) or UGE094 (fine line) pin 9, READQ-, L12 (PWB) or UHD094 (fine line) pin 8, and READQQ-, J05 (PWB) or UFK039 (fine line) pin 7.

3.6.6.9 Status Count FF08 (R2). This part of the test pulses the test clock until words from the special test shift register are stored in FIFO. Once this has been done, the controller checks FIFO available status and looks for words being available on the output of the FIFO. The CRC error flag is checked next for error status. The CRC status bit should be inactive at this time. To determine which type of error occurred, set the state display board or the logic analyzer to address 1E1. If the next state is 1C9, the error was caused by FIFO not having a word available. If the next address is 1E2, then the error was caused by a CRC error status.

If the error was caused by FIFO not available, then the SHIFTIN pulse that loads FIFO with data from the special serial register is missing. Check signal SHIFTIN at K05 (PWB) or UHD028 (fine line) pin 1 (sheet 17 of the logics) for pulses that load words into FIFO. If this signal does not pulse properly, trace it back until the problem is found. When loading data into FIFO in this mode, the SHIFTIN pulses are generated by the DSKSHIN- logic (sheet 18 of logic). Probe chip P09 (PWB) or UHD116 (fine line) for proper levels, with special attention given to CNTEQ15, which should go positive once every 16 DCLK- pulses.

If the error was caused by a CRC error status, the problem should be isolated by tracing back from CPE I-bus input, chip C02 (PWB) or UCC021 (fine line) pin 1. This signal should be traced until erroring circuitry is isolated. When testing the CRC status, it should read an error unless it is the final output of data and CRC character combined. If the CRC status shows no error read, something is wrong with this status signal.

3.6.6.10 Status Count FF09 (R2). In this test, two words are pulled out of the FIFO but not tested. The third word is loaded into the CPEs and a test is made to see if the data pattern read from the FIFO compares with the known data pattern in register 8 (R8) of the CPEs. After the successful completion of this test, the controller interrogates the rate error status to see if a FIFO timing error occurred. The type of error causing the problem needs to be determined before proceeding. This can be done by breakpointing on MCU address 1E8 with the state board or logic analyzer. By advancing to the next stage and monitoring the address that the controller branches to, the type of error can be determined. If the next address is 1C9, then the error was caused by a miscompare between the FIFO output and the CPE register. If the next address is 1E9, then the failure resulted from a rate error being detected.

If the error was caused by a data miscompare, the controller should be stopped via the state board at address 1E7 and the data bits out of the FIFO into the CPE M-bus should be checked. These bits should have a data pattern of 5s enabled onto the M-bus. If this pattern is not present, the data path should be traced back through the read data path until the error bit or control signal is isolated. If the input data to the CPEs was of the proper value, then the controller should be stopped at address 1E8, where the results of the compare are tested. The inputs to the look ahead carry should be tested for any active carry out signals from the CPEs. Check input pins on chip C07 (PWB) or UAK050 (fine line) and D07 (PWB) or UAK006 (fine line) on logic sheet 12. If any one of these signals is active, the signal can be traced back until the reason it became active is found.

If a rate error was the cause of the failure, the latch that holds the error condition should be probed (logic sheet 14). Scope chip N12 (PWB) or UGE094 (fine line) pin 6 (TIMERRQ) and insure that it goes high during this test sequence. This latch will be cleared as soon as the controller detects the error and aborts any further testing. If the latch fails to set but an error is reported, the latch output should be traced through the FIFO input multiplexer, FIFO and into the I-bus input of the CPEs. If the latch becomes set, the inputs to the latch should be probed. Special attention should be given to the waveform of the clock input (SHIFT). This signal should go active every time 16 DCLK- pulses occur. If this signal is not pulsing properly, then it should be traced back through the FIFO input multiplexer and back to the FIFO control logic (sheet 18 of logic diagrams). This SHIFTIN signal should be generated by DSKSHIN- so the inputs on P09 (PWB) or UHJ116 (fine line) should be probed. If the shift pulses are occurring properly, then the other path to follow would be the data input to the TIMERRQ latch. Trace signal ERRORSET back through the FIFO input mux (M02, PWB, or UGE072, fine line, pin 12) and insure that INRDY- is going negative before the shift pulse occurs. If this signal fails to do so, then trace INRDY- back until fault is found.

3.6.6.11 Status Count FF0A (R2). In this test, the test clock is pulsed 16 times so that another word is loaded from the test shift register into the FIFO. Once this has been accomplished, the rate error status is again checked. After this test the CRC error check is again made. To determine which type of error occurred, set the state display or logic analyzer to 1EC and then observe the next address state. If the controller branches to 1C9, then the error resulted from a rate error. If the next address is 1ED, then the fault was generated by a CRC error. To find these errors, the same fault isolation procedure of the previous two sections should be repeated.

3.6.6.12 Status Count FF0B (R2). This test reenters the diagnostic read header routine and checks the ability of the controller to detect the sync character properly and to have FIFO status correct. The fault isolation process for this error status should be the same as described in paragraph 3.6.6.8 (FF07).

3.6.6.13 Status Count FF0C (F2). This is a repeat of the same test that gave an error status count of FF08 (paragraph 3.6.6.9). The same troubleshooting procedure should be followed for this error status.

3.6.6.14 Status Count FF0D (R2). This is a repeat of the same test that gave error status count FF09 (paragraph 3.6.6.10). The same fault isolation procedure given in that paragraph should be repeated for this status count. The only difference that exists for this test and the one in paragraph 3.6.6.10 is the data pattern that is checked. The data for this test is all A's instead of all 5's.

3.6.6.15 Status Count FF0E (R2). This is a repeat of the same test that gave error status count FF0A (paragraph 3.6.6.11). The same fault isolation described in that paragraph should be repeated for this error status.

3.6.6.16 Status Count FF0F (R2). This test reenters the diagnostic read header routine and checks the third header word written into the special serial shift register. This error status should be troubleshot with the same procedure given in paragraph 3.6.6.8 (FF07).

3.6.6.17 Status Count FF10 (R2). This is a repeat of the same test described in paragraph 3.6.6.9 (FF08). When troubleshooting this error status the fault isolation description in paragraph 3.6.6.9 should be followed.

3.6.6.18 Status Count FF11 (R2). This is a repeat of the same test that gave error status count FF09 (paragraph 3.6.6.10). The same fault isolation procedure given in that paragraph should be repeated for this status count. The only difference that exists for this test and paragraph 3.6.6.10 is the data pattern that is checked. The data for this test is all 0's instead of all 5's.

3.6.6.19 Status Count FF12 (R2). This is a repeat of the same test that gave error status count FF0A (paragraph 3.6.6.11). The same fault isolation described in that paragraph should be repeated for this error status.

3.6.6.20 Status Count FF13 (R2). This portion of the diagnostics puts the controller in the write mode and calls the write header routine (puts five words in FIFO). The controller then puts itself in the direct mode and branches to the diagnostic direct register test. In this portion of the test the controller checks the ready direct status signal to see if it was set. This latch (flag) should have become set when the SHIFTIN pulses in the write header routine were active or when the direct register was loaded from the CPE accumulator. If this test fails, the direct status latch located at chip N04 (PWB) or UJD107 (fine line), logic sheet 13, should be probed. If pin 9 is low, then the latch is setting at the proper level. The signal should then be traced through the I-bus latch and into the CPE input to determine where the error is occurring. If the signal was high, then the inputs should be probed for a faulty signal. Ensure that pin 10 is not always low and that pin 11 is pulsing at proper time.

3.6.6.21 Status Count FF14 (R2). This is a continuation of the direct register test. The contents of the direct register (loaded prior to test) are compared with a known value in the CPE accumulator. If there are any miscompares, the test will be aborted and no further testing will result. If the test passes, the controller again checks the ready direct status flag that was cleared a few states earlier. The status should now show that the latch is in the clear state. The controller then exits the direct subtest and puts all ones in the controller CPE accumulator. The controller then reenters the direct register subroutine. The ones in the accumulator are loaded into the direct register, thereby causing the direct status flag to be set. The controller then checks this status bit, again ensuring that it has become set.

The first thing in troubleshooting this status error count is to determine which test failed. This can be done by using a logic analyzer or state display board. Breakpoint on address 1C7 and see what is the next address the controller goes to. If the next address is 1C9, then the error resulted from a miscompare of the data out of the direct register with the known data in the accumulator (zeros). Breakpoint at address 1C4 and probe the direct register inputs (logic sheet 15) and assure that all zeros are being loaded into the register. Also ensure that the enable and clocking signals on the direct register are active. If the data and enables show proper levels, breakpoint the controller at 1C6 and check the output signals of the direct register. If the output is bad, then the erroring bit should be traced until the problem is found.

The output of the direct register is connected to the PBUS; thus another device on the bus may be causing the output to be bad. It may be necessary to lift the output pin to see if it is functioning properly when disconnected from the bus. If the outputs all look good, but an error is reported, then the problem may lie with the CPE K-bus inputs or the look-ahead carry circuitry. Breakpoint at address 1C7 and probe the K-bus inputs to assure that they are all at a logic 1 level (low). If these are good, check chip M09 (PWB) or UBK072 (fine line), pin 12 (TESTBIT-) and ensure that this is a logic high level. If not, trace this signal back through until the failure is found.

If the next address following breakpoint 1C7 was 1C8, then the controller should be checked to see where the next address goes. If the next address is 1C9, then the controller failed to detect the clear status on the direct register flag. This problem should be investigated by probing direct status latch at N04 (PWB) or UJD107 (fine line) (logic sheet 13). Breakpoint at address 1C6 and probe pin 9 to see if it has gone to a logic high level. If this signal is not high, check pin 10 and ensure that it is a logic low. If it is not low, then this signal should be traced back until the fault is found. If pin 10 was a logical high, then the controller should be stepped (via the state board) until address 1C8 is reached. The output pin (pin 10) should be monitored while stepping to this address. If this signal goes low at any time during this sequence, the controller should be stopped and the cause should be investigated until the source of the failure is found. If the controller reaches address 1C8 and the status latch remains high, the signal should be traced through logics and checked at the CPE input.

If the controller did not report an error because of the previous two checks, then the error was caused by the direct status check upon reentry of the direct test. This is a repeat of the test described in paragraph 3.6.6.20 and the same troubleshooting procedure for this error should be followed as described in that paragraph.

3.6.6.22 Status Count FF15 (R2). This test repeats the first two tests described in paragraph 3.6.6.21. The data tested is all ones instead of all zeros. In addition to these tests the controller forces the controller into a command timer failure. It does this by loading a long delay count that exceeds the command timer delay count. If the count reaches zero before a command timer interrupt has occurred, then the command timer or interrupt circuitry is not working properly and an error is reported. If the controller detects the command timer interrupt, it goes through this interrupt routine and in the final addresses of this routine, it checks to see if the controller is in the test mode. If the controller is in the test mode, the TESTMODE latch is cleared and the controller goes back to the diagnostic test. Upon reentry of this test, the controller checks again to see if TESTMODE is active. If TESTMODE is reported active, then an error is reported and the test is aborted. If TESTMODE has become cleared, the controller returns to the initialization routine and completes the command and returns to idle.

When troubleshooting an error with this status count, the first thing is to determine which of the tests caused the failure. Use a logic analyzer or state board and determine which address the controller branched to the error status routine from. If the controller branched to error status routine at 1C9 from either 1C7 or 1C8, then the error was caused by the same test described in the previous paragraph, with the exception of all ones data instead of all zeros. If the error was caused by one of these two tests, then the troubleshooting steps of paragraph 3.6.6.21 should be followed.

If the problem was not caused by one of these two failures, then the error was a result of the command timer failure. To troubleshoot this failure, use a logic analyzer or state board to breakpoint at address 1BE. Then look back one state and determine the previous address. If the previous address was 1BD, the controller failed to detect the command timer interrupt and/or act upon it. To find this problem the command timer chip should be probed. Put a probe on chip R02 (PWB) or UJD050 (fine line) pin 3 and insure that this signal is pulsing approximately every three milliseconds (logic sheet 5). If it is pulsing but at a very slow rate, then the timing resistor and capacitor values should be checked. If the signal is pulsing properly, it should be traced to the input of the counter chip at J07 (PWB) or UFE105 (fine line) pin 9. Check J07 (PWB) or UFE105 (fine line) pin 13 (CMDTMRCLR) and insure that this signal is not a constant high. If these signals appear to be working properly, the output signal should be checked. Scope J07 (PWB) or UFE105 (fine line) pin 7 and see if it ever goes low during the diagnostic test (long test). This may be hard to see on an oscilloscope, so the best way to troubleshoot this would be breakpoint at an address (1BE, for example) and see that this signal goes low and stays low. If it does not, recheck the inputs or change the chip. If this signal does go low, step the controller one clock cycle and check to see that this status was latched in the interrupt latch (F09, PWB, or UEE094, fine line, pin 12 goes low).

Check the interrupt decode chip at F10 (PWB) or UFE094 (fine line) for proper outputs. F10 (PWB) or UFE094 (fine line) pin 14 (INTA) should go low and F10 (PWB) or UFE094 (fine line) pin 6 should go high with pins 7 and 9 staying low. Once this has been verified, the controller should be advanced one more clock state and the INTA signal should become latched in the interrupt latch. Check F09 (PWB) or UEE094 (fine line) pin 15 and insure that it has gone high. The controller should have been forced to the command timer interrupt address (040) at this time. If not, repeat the procedure just described while monitoring the trap logic and multiplexer outputs. Also insure that the J09 (PWB) or UFK006 (fine line) chip is forced to a trap state and gives the MCU chips the proper selection values. Once it has been determined that the controller is trapping to the interrupt, the controller should be set to breakpoint on address 00A and the clear on the TESTMODE latch should be checked. Probe H11 (PWB) or UFK050 (fine line) pin 4 and insure that it has gone low during this state. If not, probe inputs and trace the faulty input until problem is found.

If the TESTMODE latch is being cleared, then the controller should be set to breakpoint on address 1BE and the testmode bit at the input of CPE E04 (PWB) or UCC021 (fine line) pin 1 should be probed. If this signal is high, then the signal should be traced back through the logics until the fault is found. If the signal was low but an error was reported, the problem would be associated with the CPEs (K-bus, function input, or carry out) circuitry.

3.6.6.23 Status 0000 (R2) Red LED Lighted. If the controller runs the self-diagnostics without reporting an error but the red LED indicating a hardware failure remains on, several possible causes of the problem could exist. To find this problem, check chip G05 pins 3 and 11 (PWB) or VEE105, pins 9 and 8 (fine line) (logic sheet 13) with an oscilloscope and see which one is a logic low causing the indicator to become lighted. If G04 (PWB) or XFE039 (fine line) pin 11 is low, probe chip L09 (PWB) or VFK094 (fine line) pins 1 and 2 to see if one or both of these signals is causing the LED to remain lighted. Both of these signals become set (low) during the self-diagnostic test, but are cleared upon the successful completion of the diagnostic test. If these signals are not cleared, the controller should be set to breakpoint at address 1C0. Check H11 (PWB) or UFK050 (fine line) pin 11 and see that it has gone high (FAULTQ-). If it has failed to do so, probe the inputs and trace the faulty signals back through the logic until fault is isolated. If DIAGFAULTQ- was causing the LED to remain lighted, the controller should be set to breakpoint at address 1C3 and the output of H11 (PWB) or UFK050 (fine line) pin 12 should be checked. If this signal has not become a logic high, trace it back through the logic until the problem is isolated.

3.7 DIAGNOSTIC TEST USAGE FOR FAULT ISOLATION

The following sections describe the usage of the diagnostic test and the error message interpretation along with the associated hardware problems that would give the error status reported.

3.7.1 OPERATOR CONVENTIONS USING DIAGNOSTIC TEST PROGRAM. Operator action is required for test initialization, for setting up parameters at the beginning of the test, and for making certain decisions that are required during the execution of part 6 of the diagnostic. Otherwise, operator intervention during the execution is not needed unless the system halts upon the detection of an error and an error message is printed.

The diagnostic test is divided into six major parts. Each part can be executed separately or in automatic sequence (see paragraph 3.7.2). The diagnostic program also contains verbs which can be executed by manual entry on the terminal (such as the keyboard of the 733 data terminal). A list of execution-type verbs that may be entered at user option is contained in table 3-4.

Table 3-4. List of Verbs for Diagnostic Execution

Verb	Function
E1	Execute Part 1
.	.
.	.
E6	Execute Part 6
EA	Execute all 6 parts
L1	Loop on Part 1
.	.
.	.
L5	Loop on Part 5
LA	Loop on Parts 1-5
C2	Loop on Part 2 and change drives
C3	Loop on Part 3 and change drives
C4	Loop on Part 4 and change drives
C5	Loop on Part 5 and change drives
CA	Loop on Parts 2-5 and change drives
ET	Execute a subtest
LT	Loop on subtest

NOTE

There are no verbs to loop on Part 6.

The utility verbs should be used as tools in the fault isolation process if failures or errors occur (table 3-5). Special note should be taken in regard to the ET and LT verbs. By selecting these verbs, subtests of the major test can be executed. This allows the operator to execute smaller test segments and will, thereby, make it easier when troubleshooting a particular failure.

Table 3-5. List of Utility Verbs

Verb	Function	Comment
IC	Issue one command	Option to check status.
IM	Issue multiple commands	Option to check status.
LO	Loop on multiple commands	Option to check status.
DC	Display current controller status	Shows contents of controller registers.
DT	Display trace table	Display the returned status from the last 10 commands issued.
CD	Compare data	Compare two blocks of data.
SR	Store registers	Shows the disk controller parameters and the self-test status. (Should be 0000 if error-free).

Table 3-5. List of Utility Verbs (Continued)

Verb	Function	Comment
FD	Format the whole disk	Format disk at one sector/record.
RD	Read only	Execute read only of formatted disk and report any errors.
RS	Reset	Issue hardware I/O reset command and clear the DT table.
AL	Disk alignment	Issue seek(s) until interrupted.
IT	Initialize	Initialize diagnostic parameters.

If the error message option is selected during initialization, controller failure will be reported by error messages on the printout of the output device (see paragraph 3.7.3). Once an error message is reported, a fault isolation process should be started.

Following is a list of operator conventions to be used when conducting the diagnostic test:

1. Whenever the system is ready to have a verb mnemonic entered by the operator, the test will print VERB?-. Any legal two-character verb can be entered. If a verb is entered that is not in the list of available verbs, a message ILLEGAL VERB will be printed.
2. When a dash "-" is printed, it means the system is waiting for an operator response.
3. All input is ended by entering a space (pressing the space bar on the interactive device).
4. Whenever a question is printed out alone with the current value of the parameter, and if the value of the parameter is correct (i.e., accepted as one not to be altered), the operator should enter a space.
5. Entering a "?" will erase an input and allow it to be reentered.
6. Entering an "@" will cause the sytem to return to the verb decoder.
7. All numbers printed by the test, as well as those entered, are hexadecimal, not decimal.
8. Whenever a number is entered, it is checked to make sure it is a legal hexadecimal value. If it is not a legal hexadecimal value, a message is printed. Then the operator can reenter the correct number.
9. All YES/NO questions are answered by using the following convention: 1=YES; 0=NO. These values are checked for answers to YES/NO questions, and if they are not 0 or 1, an error message is printed and the operator can reenter the answer.
10. Whenever messages are being printed on the 733 ASR, they can be stopped by pressing any key on the 733 keyboard.

3.7.2 PARTS OF THE DIAGNOSTIC TEST. The following sections describe Part 1 through Part 6 of the diagnostic. These parts are broken into subtests described below. Each subtest can be executed or looped on independently. Most commands that are issued to the controller are issued using the command issuer subroutine. The commands issued are eight words written to the TILINE peripheral control space.

3.7.2.1 Part 1 — Quick Controller Test. Part 1 is a quick test of the controller. It is not necessary to have a disk unit attached for the execution of this part. If this part of the test fails there is a problem with the controller and the rest of the test will probably not run correctly.

Part 1 is made up of subtests 1-3.

Subtest 1

All of the bits in the slave logic that can be written to and read from are tested by writing and reading them under a mask. The 16 patterns are 0, 1111, 2222, . . ., FFFF. If miscompares occur during the read portion of the test, an error message will be printed.

Subtest 2

All of the unit select lines in word 6 of the controller slave registers are set to zero, deselecting the unit. The disk status is then checked. The returned status should be C000, OFFLINE and NOT READY bits set. Then a reset command is executed in the 990 and the controller status is checked. The returned status should be A100, IDLE, ERROR and ABNORMAL COMPLETION bits set. If the expected status from either operation is not returned an error message will be printed.

Subtest 3

A store registers command is issued to the controller with the status checked after the command. The descriptor parameters read from the controller are then checked against a parameter table for the disk. If the descriptor words read do not compare with the table an error message is printed. After this, word 2 of the slave logic registers, which holds the returned self-test status, is checked for errors. An error message will be printed if the expected status is not returned.

3.7.2.2 Part 2 — Quick Controller and Disk Test. Part 2 contains several subtests which check for special conditions in the controller status and disk status registers. The general procedure for these subtests is to issue commands that will force the error bits in the status registers to set, and then to verify that the correct bits were set.

The status bits checked in this part are:

Status Bit	Definition	Subtest
TIH	Transfer Inhibit	>8
IE	Header ID Error	>9
SE	Search Error	>A
DE	Data Error	>B
CT	Command Time-Out	>C
SI	Seek Incomplete	>D
UE	Unit Error	>E
IDLE	Idle Bit	>F
TT	TILINE Time-Out	>10
RE	Rate Error	>11

Part 2 consists of subtests >4 through >13.

Subtest 4

This test issues seek commands to cylinders 0, 10, 20, 30, and 40 and checks the controller status, register 7, to see if the idle and complete bits have been set. After each seek command is issued and the correct status has been returned the attention interrupt mask for the unit under test is set. With the controller idle this should cause an interrupt. Checks are made to ensure that an interrupt did indeed occur, and then a restore command is issued.

Subtest 5

This subtest verifies that unformatted writes and reads can be done. A write unformatted specifying 16 words is issued to the disk, after which a read unformatted with interrupts enabled is issued also specifying 16 words. The data written is compared with the data read. Any miscompares will generate an error message. A total of ten writes and reads are issued, using this pattern: 0, >1111, >2222, >4444, >8888, >5555, >AAAA, >3333, >CCCC, >6666, >9999, >7777, >EEEE, >BBBB, >DDDD, >FFFF.

Subtest 6

This subtest verifies that the write format command can be done. A write format command is issued to different tracks on the disk. After each write a read unformatted command is issued and the format read is checked against the correct format. If any miscompares occur an error message will be generated. Ten writes and reads are issued during this subtest.

Subtest 7

This subtest verifies that write and read data commands can be performed. This is done by formatting a cylinder, issuing a write data command specifying 16 words, issuing a read data command specifying 16 words, and then comparing the data written with that read. Any miscompares that occur will cause an error message to be printed. This sequence is looped on 32 times and issued to different cylinders.

Subtest 7 also verifies the auto retry code on the controller. One track is formatted at one sector per record and maximum word count. A write data command is issued to that track specifying one full track of data for the word count. This write data command is timed so as to allow only one retry of the command (the controller standard) on each sector. If the command is not finished within the allowed time an error message is generated. This sequence is looped on for ten passes.

Subtest 8

Subtest 8 tests for the correct operation of the transfer inhibit bit. To check this, track 0 on the disk is formatted with sectors per record = 1, word count = 4 and the data = 0000. An area in memory in then initialized with the data >AAAA. A read command is issued to the disk with the transfer inhibit bit set specifying the previously initialized memory area. The memory area is then checked to ensure that it still contains >AAAA. If not, an error message is printed.

Subtest 9

Subtest 9 verifies that an ID header error (IE) can be generated and detected by the controller. To do this, a write format command is issued to a track on the disk. A read unformatted command is issued to obtain the header parameters. The test then changes each of the three words of the header and the CRC one at a time, and, using an unformatted write command, replaces the good header information on the disk with the modified header values. The test then issues a write data command using the good header information, which should cause an ID error. After the write data command completes, the returned controller status is checked to see if an ID error was reported. If not, an error message is printed.

Subtest >A

Subtest >A verifies that a search error (SE) can be generated and detected by the controller. This is done by issuing a write format command to a track specifying two sectors per record. A read data command is then issued starting at sector one, where there is no header information. The controller is then checked to verify that a search error was detected by the controller. After this, a write format command is issued to the same track as before starting with sector 0, which will write over the header information of sector 0. A read data command is issued to sector 0 of the track. The controller is checked to verify that a search error was detected. If not, an error message will be printed.

Subtest >B

Subtest >B checks to ensure that a data error can be generated and detected by the controller. A write format command is issued to a track on the disk specifying a word count of 80. Then an unformatted read is issued to the same track to get the header information. The returned word count, in word 3 of the header information, is changed to a value of two. The new word count is used along with the other header values to generate a new CRC character value. These are then written to the disk using an unformatted write. The test then issues a read data command specifying a word count of two. A CRC error should result and the DE bit should be set.

Subtest >C

Subtest >C verifies that a command time-out (CT) can be caused and that the controller can detect its occurrence. This is done by issuing a read data command specifying a sector address equal to the maximum address plus six. The controller is then checked to ensure that the CT bit is set. If not, an error message will be printed.

Subtest >D

Subtest >D verifies that a seek incomplete (SI) error can be generated and that the SI bit will set upon its occurrence. This is done by:

1. Formatting the last track on the disk with the sectors per record = maximum and the word count = 100 words.

2. Doing a write to the last track with the word count = 101 words.

3. Checking the controller and disk status. The controller status should be >A801. Disk status should be >04XX where XX is an indeterminate value.

4. After the write, issuing a restore to clear the disk.

Subtest >E

Subtest >E verifies that no data will be transferred during a write operation with a word count = 0. It also verifies that the destination record of the write gets set to all zeros. This is done by issuing the following commands:

1. A write format command is issued to track 0 specifying sectors per record = 1 and word count = 2.

2. A write data command is issued with the word count = 0 and data initialized to >1234.

3. A read data command is issued with a word count = 2. The data read back is checked to ensure that it has all been set to zeros.

Subtest >F

Subtest >F checks for the correct operation of the idle bit. A state of 0 means the controller is busy, and a state of 1 means the controller is idle. The check is made by issuing a write data command using the TILINE address in the memory address portion of the write command word. Since the controller should be busy while the write is being done, the most significant bit of the controller status should be set to 0. Use the following commands:

1. Issue write format to track 0 with word count = 12.

2. Issue a write data with the word count = 8 and the TILINE address equal to the address of the controller.

3. Issue a read data with a word count = 8. Check the most significant bit of the controller status word. It should be 0. If not, an error message will be generated.

Subtest >10

Subtest >10 verifies that a TILINE time-out can occur and that the controller can detect its occurrence. This is done by issuing a store registers command with an illegal memory address specification. As soon as the idle bit sets to a 1, controller idle, the controller status is checked to confirm that the TILINE time-out bit (TT) is set. If it is not set, an error message will be generated.

Subtest >11

Subtest >11 verifies that a rate error can occur and that the controller can detect its occurrence. After issuing a write format command to a track, a read data command is issued. The timing is deliberately thrown off during the read by moving data from a nonexistent memory location >800 times. The controller status is checked to see if the rate error bit (RE) is set. If not, an error message is printed. The expected controller status = >A008.

This test is valid only on DS10 controller boards of revision R or later. Boards before this time cannot generate predictable rate errors.

Subtest >12

Subtest >12 verifies that the disk drive can correctly switch heads from the maximum cylinder of head 0 to cylinder 0 of head 1. First a write format command is issued specifying 1 sector per record and a maximum word count. After this, a write data command is issued with a word count of >4096, enough words to cause the controller to switch heads. After the write data command is completed, the controller status is inspected for a status of >C800. If this status is not detected, an error message will be printed.

Subtest >13

Subtest >13 verifies that the controller can read successfully when it is forced to switch heads and cylinders. Use the following commands:

1. Issue a write format command to cylinder >FF, head 0, last sector, with a word count = 10.

2. Issue a write format command to cylinder >100, head 1, beginning with sector 0, with a word count = 10.

3. Issue a write data command to cylinder >FF, head 0, last sector, with a word count = 20. Use various data.

4. Issue a read data command to cylinder >FF, head 0, last sector, with a word count = 20.

5. Compare the data written with the data read. If any miscompares are found, issue an error message.

3.7.2.3 Part 3 — Disk Addressing Test. Part 3 of the diagnostic checks the controller's and disk's ability to address every record on a track and every track on the disk. Part 3 is composed of subtests >14 through >16.

Subtest >14

Subtest >14 verifies that the controller can address all of the sectors on one track correctly. To do this it goes through the following sequence:

1. Issues a write format command to track 0 with sectors per record = 1 and word count = 8.

2. Issues a write data command specifying eight words of data to each sector on the track. The write is done in reverse sector order, with the last sector written first and the sector address decremented to 0. This is done so that if a write modifies the next sector, the following write will not cover up the error. The data word used is the number of sectors per record and sector address. After this, a read data command is issued and the data read is checked against what was written. The read starts at the first sector on track 0.

3. Checks the controller for improper sector selection in the disk drive or an incorrect cartridge. This is done by issuing a write unformatted command to sector >15, the maximum sector number plus one. The controller status register is examined to see if the CT error bit has been set. If not, an error message is printed.

Subtest >15

Subtest >15 verifies that the controller can address every track on the disk. To do this it goes through the following sequence:

1. Formats the whole disk with sectors per record = 1 and words per record = 8.

2. Issues a write data command specifying eight words to the first record on each track. The data is equal to the cylinder address.

3. Issues a read data command and compares the data read to the data written. In reading the data back, the test starts at the middle cylinder, then increments by one and decrements by two, increments by three and decrements by four, etc., until all cylinders are read.

4. Performs 2000 random read data commands on the disk. The controller is checked to see that each command completes successfully. If not, an error message is printed.

Subtest >16

Subtest >16 verifies that the controller can do writes and reads with variable sectors per record and auto increments. To do this it goes through the following sequence:

1. Issues a write format command to the first 80 tracks of the disk with sectors per record = x (where x goes from 1 to the maximum allowed) and the word count = 1 word per record. The data used is the sectors per record value.

2. Issues a read data command with the word count equal to >50 words, and checks the data read. If any miscompares occur an error message is printed.

3. Increments sectors per record count and reexecutes the test. This is done until the sectors per record count = maximum.

3.7.2.4 Part 4 — Memory Addressing Test. Part 4 of the diagnostic tests the ability of the controller to address all of TILINE memory. At least 4K words of memory past the end of the diagnostic must be available for the subtests to run.

Part 4 consists of subtests >17 and >18.

Subtest >17

Subtest >17 tests the controller's ability to read and write to unmapped memory. Unmapped memory includes every memory location from the end of the diagnostic to the end of memory or the end of the first 32K block of memory, whichever comes first. All of this memory is used as the read/write buffer for the tests. The test first verifies that there is at least 4K words of memory available for its buffer. If a total of 4K words is not available then INSUFFICIENT MEMORY will be printed and the subtest will be skipped. If sufficient memory is available then the address is written as data into each buffer location. The whole buffer is then written to disk and the buffer is cleared. The data is then read back from the disk into the buffer and each buffer location is checked to verify that it contains its own address as data. If any miscompares occur an error message will be printed.

Subtest >18

Subtest >18 verifies the controller's ability to read and write to memory locations in mapped memory. If there is no mapped memory a message will be printed stating this and the subtest will be skipped. The test first verifies that there is at least 4K words of memory available for its buffer. If 4K words are not available then INSUFFICIENT MEMORY will be printed and the subtest will be skipped. If sufficient memory is available then the first >80 bytes of each 4K-word block of mapped memory will be written to and read from. Every two words of data in each >80-byte block will contain the processor address and the mapped bias used by the processor to address the mapped buffer. The block is then written to disk and the buffer is cleared. The data is then read back from disk to its mapped buffer area and each data pair is checked to verify that it contains the correct address and bias. All mapped memory is checked in this way. If any part of a 4K-word segment fails to initialize, that 4K-word segment is skipped.

3.7.2.5 Part 5 — Media Integrity Test. The media integrity test uses the CRC character to verify the recording reliability of the disk using four different data patterns. Part 5 consists of subtest >19.

Subtest >19

Subtest >19 uses the CRC character to verify data written to the entire disk. It does this in the following way:

1. A write format command is issued to the entire disk with the sectors per record = maximum (1 record per track) and the word count = maximum.

2. A read data command with the word count = 1 is done from each track. The word that is read is checked and if a bit is bad anywhere on the track a status error should be reported with the DE error bit set. If the data word that is read back is incorrect, the read is executed ten times and the number of failures in ten tries is added to the data error count. (It is not possible simply to read back all of the words from the disk and check them, because it would take a very long buffer to accommodate the data.) The disk is formatted and read four times with different data each time. The four data patterns used are 0000, FFFF, AAAA, and 5555. When the disk is being formatted, each track gets a data pattern different from that on the track before. The pattern of data used goes as follows:

Loop	Track	Data
1	0	0000
	1	FFFF
	2	AAAA
	3	5555
	4	0000
	:	:
	Max	
2	0	FFFF
	1	AAAA
	2	5555
	3	0000
	4	FFFF
	:	:
	Max	
3	0	AAAA
	1	5555
	2	0000
	3	FFFF
	4	AAAA
	:	:
	Max	
4	0	5555
	1	0000
	2	FFFF
	3	AAAA
	4	5555
	:	:
	Max	

3.7.2.6 Part 6 — Interactive Write-Protect Test. Part 6 verifies that a power cycle of both the computer and the disk unit will not cause the data on the disk to be modified. Part 6 also tests the write-protect function of the drive. Because Part 6 requires the operator's intervention, there are no verbs to loop on in it. Part 6 consists of subtest >1A.

Subtest >1A

Subtest >1A uses the data written during Part 5 to verify that a power cycle will not modify data on the disk. Because of this it is necessary to execute Part 5 before executing this subtest. When the test starts execution it asks the operator if Part 5 (subtest >19) has been run. If the operator enters a 0 (no) a message will be output asking him to run Part 5. If a 1 (yes) is entered the test will output a message asking if the power has been cycled. If the answer is 0 (no) the test will output a message telling the operator to cycle power. To do so, the operator does the following:

1. Turn off power to the computer.
2. Turn off power to the disk.
3. Turn power on to the disk.
4. Turn power on to the computer.

If the answer is 1 (yes), the test verifies that the data on the disk has not been modified by the power cycle.

NOTE

When the question asking if the system power has been cycled is answered with 0, the computer should go into an idle state. If the operator does not want to cycle the system's power, the operator can get back to the DOCS verb decoder by depressing the HALT/SIE button and then depressing the RUN button.

This should cause the diagnostic to return to the verb decoder. The return will be signaled by the prompt VERB?- being displayed on the I/O device.

Upon completion of the power cycle test the write-protect function of the disk drive is tested. This is done by having the operator first put the drive in the write-protect mode. The diagnostic then attempts to write data out to the disk drive. The area where the write was issued is then read to see if it has been modified. If the data on the disk has been modified then a error message is generated. If not, the operator is asked to depress the write-protect switch again to put the drive in the read/write mode. The controller is then checked to verify that the write-protect bit has been cleared and the drive can be written to.

The messages that appear to the operator are:

WRITE-PROTECT THE DISK DRIVE CURRENTLY UNDER TEST.
HIT RETURN WHEN READY —

UNPROTECT THE DISK DRIVE CURRENTLY UNDER TEST, PUT IT IN READ/WRITE MODE. HIT RETURN WHEN READY —

3.7.3 DIAGNOSTIC TEST INITIALIZATION. Refer to the *Model 990 Computer Diagnostics Handbook* for loading procedures.

NOTE

Before conducting the disk diagnostic test program, always install a scratch disk cartridge in the drive and write protect the fixed disk if user information or operating system is installed.

NOTE

Loading the diagnostic into the computer from the cassette tape requires about seven minutes.

3.7.4 ERROR MESSAGES. All of the error messages contained within the DS10PD diagnostic are explained in this section. When an error occurs in the execution of any part or subtest of the diagnostic, an error message will be printed out, provided that the print error flag = 1.

The error message will be preceded by a line indicating the subtest number in which the error occurred. This line will print out for both part executions and subtest executions (for example: ERROR IN SUBTEST #12).

The error in subtest line will end with the error number. The error number is a two-digit hexadecimal number. The numbers do not run consecutively from part to part because of the format of the number. The first digit of the error number can be either 1-6 or the hexadecimal (hex) digit >C. The first digit designates the part of the diagnostic generating the error message. The digit >C is used to designate the common error-generating subroutines (the command issuer subroutine and the status checker subroutine). The second digit designates the message number within the part represented by the first digit. An error number of 42 represents the second error message in that list of error messages unique to part 4.

Following the error message number will be the text of the error message. The error message will generally list these three things:

1. What was happening at the time of the error.
2. The specific incident which caused the error to occur.
3. The expected data and/or status and the received data and/or status condition.

3.7.4.1 Part 1 — Error Messages. The error messages that can be generated in Part 1 are as follows:

ERROR #	MESSAGE
>11	DID A WRITE AND READ OF ALL BITS IN THE CONTROLLER REGISTERS. EXPECTED THE SAME DATA READ AS WAS WRITTEN. DATA READ = XXXX DATA WRITTEN = XXXX CONTROLLER REGISTER (0-7) = XX
>12	SET ALL UNIT SELECT LINES IN REG. 6 OF THE CONTROLLER =0. EXPECTED THE OL AND NR BITS IN REG. 0 TO BE SET. STATUS EXPECTED = XXXX STATUS RETURNED= XXXX
>13	DID AN I/O RESET AND READ THE CONTROLLER STATUS, REG. 7. EXPECTED THE IDLE, ERR AND AC BITS IN REG. 7 TO BE SET. STATUS EXPECTED = XXXX STATUS RETURNED = XXXX
>14	DID TWO READS OF THE CONTROLLER STATUS, REG. 7. EXPECTED THE LOCKOUT BIT TO BE SET. STATUS EXPECTED = XXXX STATUS RETURNED = XXXX
>15	SELF-TEST ERROR AFTER ISSUING A STORE REGISTERS COMMAND REG. 2 OF THE CONTROLLER WAS CHECKED FOR THE SELF-TEST RETURN STATUS. STATUS EXPECTED = XXXX STATUS RETURNED = XXXX (Consult paragraph 3.7.4.3 for status error definitions before continuing the diagnostic.)
>16	STORE REGISTERS ERROR DID A STORE REGISTERS COMMAND AND EXPECTED THE 3 WORDS RETURNED TO COMPARE WITH THE TABLE OF KNOWN VALUES. VALUE RETURNED = XXXX VALUE EXPECTED = XXXX INCORRECT VALUE IS WORD # XX NOTE: Store register values should equal: >0F00, >1430, >1198

3.7.4.2 Part 2 — Error Messages. The error messages that can occur in Part 2 are as follows:

ERROR #	MESSAGES
>20	WITH THE CONTROLLER IDLE BIT SET TO 1, (CONTROLLER IDLE), THE ATTENTION INTERRUPT MASK BIT IN REG. 0 WAS SET TO CAUSE AN INTERRUPT. THE EXPECTED INTERRUPT WAS NOT RETURNED WITHIN 3 SECONDS.
>21	DID A WRITE TO AND THEN A READ FROM THE DISK USING 16 PATTERNS. EXPECTED THE PATTERNS READ TO COMPARE WITH THE PATTERNS WRITTEN. PATTERNS READ XXXX — PATTERNS WRITTEN XXXX
>22	DID A WRITE FORMAT TO AND THEN AN UNF. READ FROM A SPECIFIED TRACK. EXPECTED THE FORMAT READ TO COMPARE WITH THE FORMAT WRITTEN. DATA REC. XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX DATE EXP. XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
>23	RETRY LOOP ERROR ISSUED A WRITE DATA COMMAND AND TIMED IT TO ALLOW ONLY ONE RETRY (THE CONTROLLER STANDARD) PER SECTOR. THE CONTROLLER WAS STILL RETRYING THE COMMAND WHEN IT TIMED OUT.
>24	A READ FROM AN AREA ON DISK CONTAINING ZEROS TO A MEMORY AREA CONTAINING AAAA'S WAS ISSUED WITH THE TRANSFER INHIBIT BIT SET. DID NOT EXPECT THE MEMORY AREA TO BE CHANGED. DATA RECEIVED XXXX — DATA WRITTEN XXXX
>25	ID WORD ERROR AFTER CHANGING ID WORD #1 OF A TRACK WITH AN UNF. WRITE DID A WRITE DATA TO THE SAME TRACK. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED. R7 STATUS EXP = XXXX REC = XXXX
>25	ID WORD ERROR AFTER CHANGING ID WORD #2 OF A TRACK WITH AN UNF. WRITE DID A WRITE DATA TO THE SAME TRACK. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED. R7 STATUS EXP = XXXX REC = XXXX

>25 ID WORD ERROR
AFTER CHANGING ID WORD #3 OF A TRACK WITH AN UNF. WRITE DID A WRITE DATA TO THE SAME TRACK. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>25 ID WORD ERROR
AFTER CHANGING THE HEADER CRC OF A TRACK WITH AN UNF. WRITE DID A WRITE DATA TO THE SAME TRACK. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

NOTE:

The above 4 errors all share the same error number because they are all ID errors. The error generating routines are all unique.

>26 SEARCH ERROR
DID A WRITE OVER THE SYNC CHARACTER WITH AN UNF. WRITE AND THEN DID AN UNF. READ. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>27 DATA ERROR
AFTER CHANGING THE HEADER CRC OF A TRACK WITH AN UNF. WRITE DID A READ DATA OF THE SAME TRACK. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>28 COMMAND TIME ERROR
ISSUED A FORMATTED READ COMMAND WITH THE SECTOR ADDRESS = MAX+6 TO CAUSE A COMMAND TIMER TIME-OUT. RECEIVED THE TIME-OUT BUT THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>29 SEEK INCOMPLETE ERROR
AFTER FORMATTING THE LAST TRACK WITH S/R = MAX AND THE WORD COUNT = 100 A WRITE PAST THIS ADDRESS WAS ATTEMPTED AND THE EXPECTED STATUS WAS NOT RECEIVED.

R0 STATUS EXP = 04XX , REC = XXXX

R7 STATUS EXP = A801 , REC = XXXX

>2A A WRITE COMMAND WITH A BYTE COUNT = 0 WAS ISSUED TO VERIFY THAT NO DATA WOULD BE TRANSFERRED, BUT DATA WAS WRITTEN TO THE DISK.

>2B BUSY FLAG SET ERROR
AFTER WRITING THE TPC REG. TO DISK AND READING BACK, THE IDLE BIT IN REG. 7, MSB OF THE LAST WORD WRITTEN, SHOULD NOT BE SET SINCE THE CONTROLLER WAS EXECUTING THE COMMAND WHEN REG. 7 WAS WRITTEN. REG. 7 (MSB SHOULD BE 0) WAS XXXX.

>2C TILINE TIME-OUT ERROR
ISSUED A STORE REGISTERS COMMAND TO A NONEXISTENT MEMORY LOCATION. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>2D WRITE AMP RECOVERY ERROR
AFTER FORMATTING TRACKS 0 AND 1, A WRITE WAS ISSUED SPECIFYING 4096 WORDS, WHICH SHOULD HAVE CAUSED THE CONTROLLER TO SWITCH HEADS. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>2E HEAD SWITCHING ERROR
AFTER FORMATTING MAX HEAD, CYL FF AND CLEARING HEAD 0, CYL 100 A WRITE DATA AND A READ DATA COMMAND WERE ISSUED TO CAUSE THE CONTROLLER TO SWITCH HEADS.

DATA RECEIVED	DATA WRITTEN
XXXX	XXXX

>2E HEAD SWITCHING ERROR
AFTER FORMATTING MULTIPLE SECTORS AND TRACKS A READ WAS DONE TO CAUSE THE CONTROLLER TO SWITCH HEADS AND THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP =XXXX REC = XXXX

>2F RATE ERROR
ISSUED A READ DATA COMMAND AND THEN CAUSED AN INTENTIONAL ERROR IN THE TIMING. SHOULD HAVE FORCED A RATE ERROR BUT THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

3.7.4.3 Part 3 — Error Messages. The Part 3 error messages are as follows:

ERROR #	MESSAGES
>31	DID A WRITE OF DATA PATTERN TO EACH SECTOR ON TRACK 0. EXPECTED DATA READ BACK TO COMPARE TO DATA WRITTEN.

DATA RECEIVED	DATA WRITTEN
XXXX	XXXX

>32	ISSUED A WRITE COMMAND TO THE MAXIMUM SECTOR NUMBER + 1, (21 DECIMAL), AND EXPECTED THE COMMAND TO TIME OUT ON THE ILLEGAL SECTOR NUMBER. THE EXPECTED CONTROLLER STATUS WAS NOT RECEIVED.

R7 STATUS EXP = XXXX REC = XXXX

>33	DISK ADDRESSING ERROR DID WRITE OF 8 WORDS OF DATA TO 1ST SECTOR OF EACH TRACK USING THE CYL NUMBER AS DATA. EXPECTED THE DATA READ TO COMPARE TO THE DATA WRITTEN.

DATA RECEIVED	DATA WRITTEN
XXXX	XXXX

>34	DID A WRITE FORMAT AND THEN A READ DATA ON THE FIRST 100 TRACKS INCREMENTING THE SECTOR/RECORD VALUE FROM 1 TO >15. THE EXPECTED SEC/REC VALUE WAS NOT RETURNED.

DATA RECEIVED	DATA WRITTEN
XXXX	XXXX

3.7.4.4 Part 4 — Error Messages. The error messages that can occur in Part 4 are as follows:

ERROR #	MESSAGE
>41	INSUFFICIENT MEMORY ERROR NEED TO HAVE AT LEAST 4K WORDS OF MEMORY BEYOND THE END OF THE DIAGNOSTIC TO RUN THIS TEST.
>42	MAPPED MEMORY SUBTEST TIPPED DID WRITE OF ADDRESS THEN BIAS TO CONSECUTIVE MEMORY LOCATIONS WITH MAP ENABLED. EXPECTED BIAS VALUE TO BE CONVERTED TO THE ADDRESS OF THE LOCATION. ADDRESS = XXXX BIAS VALUE = XXXX
>43	ERROR IN ADDRESSING UNMAPPED MEMORY THE CONTROLLER IS SET UP TO READ AND WRITE EVERY ADDRESS INTO ITSELF FROM THE END OF THE DIAGNOSTIC TO THE END OF THE 1ST 32K BLOCK OF MEMORY. THIS ADDRESS DID NOT CONTAIN ITS OWN ADDRESS AS DATA. DATA RECEIVED XXXX — DATA WRITTEN XXXX
>44	ERROR IN ADDRESSING MAPPED MEMORY THE CONTROLLER IS SET UP TO READ AND WRITE MAPPED ADDRESSES FROM MEMORY. A COMPARE IS THEN MADE. THE FOLLOWING ADDRESSES DID NOT COMPARE. MAP ADDR = XXXX MAP BIAS = XXXX TILINE ADDR = XXXXXX EXP DATA = XXXX REC DATA = XXXX

3.7.4.5 Part 5 — Error Message. The error message for Part 5 is as follows:

ERROR #	MESSAGES
>51	MEDIA INTEGRITY ERROR DID A WRITE FORMAT USING MAX SEC/REC AND MAX WORD COUNT WHILE WRITING VARIABLE DATA PATTERNS. THEN DID A READ TO VERIFY DATA INTEGRITY.

BAD TRACK LIST (IN HEXADECIMAL)

CYL	HEAD	DATA WRITTEN	DATA READ	# OF ERRORS IN >A RETRIES
XXX	XX	XXXX	XXXX	X

3.7.4.6 Part 6 — Error Messages. The error messages in Part 6 are as follows:

ERROR #	MESSAGES
>61	DID A READ OF THE DATA PATTERNS WRITTEN DURING PART 5 EXPECTING THE DATA READ TO COMPARE WITH WHAT WAS WRITTEN BEFORE THE POWER CYCLE.

DATA WRITTEN	DATA READ	CYL ADDR	HEAD ADDR
XXXX	XXXX	XXX	XX

>62	****WARNING**** THE DS10 CONTROLLER IS UNABLE TO SET THE WRITE-PROTECT BIT, BIT 2, IN THE CONTROLLER STATUS REGISTER, REG. 0. THE DRIVE CANNOT BE WRITE-PROTECTED.
>63	ISSUED A WRITE AND THEN A READ DATA COMMAND TO THE UNIT UNDER TEST WITH THE WRITE-PROTECT BIT SET IN THE CONTROLLER STATUS REGISTER. THE DRIVE WAS WRITE-PROTECTED, DATA ON THE DISK WAS MODIFIED. THE DISK IS NOT PROTECTED WITH THE WRITE-PROTECT SWITCH SET.
>64	****WARNING**** THE WRITE-PROTECT BIT IN THE CONTROLLER STATUS REGISTER CANNOT BE CLEARED. THE DISK DRIVE CANNOT BE PUT INTO THE READ/WRITE MODE.

3.7.4.7 Common Error Messages. The following are common error messages:

ERROR #	MESSAGES
>C1	AFTER ISSUING A COMMAND THE CONTROLLER FAILED TO GO TO IDLE WITHIN 20 SECONDS.
>C2	UNEXPECTED DISK INTERRUPT AT LOCATION XXXX.
>C3	THE CONTROLLER HAS TIMED OUT WHILE WAITING FOR THE IDLE BIT TO SET AFTER AN INTERRUPT WAS GENERATED USING THE ATTENTION INTERRUPT MASK BITS.
>C4	**STATUS CHECKER ERROR** CONTROLLER STATUS COMP = X ERR=X IDLE=X

3.7.5 SYSTEM ERROR MESSAGE ANALYSIS. When the diagnostic test program detects a fault and reports this fault as a printout, the printed error message should be carefully analyzed for information that will provide a key to the problem and indicate a direction toward fault isolation. There are two basic types of error messages generated by the diagnostic test program. One is a specific error generated by a specific test condition and the other is a general error message created when an error occurs which does not fall into the same area being tested by the diagnostic.

After a fault has been reported by the diagnostic test program, the procedure is to analyze the reported error message, set up a scoping loop, and proceed to isolate the fault. Faults can be classified into various types of failures, which can be associated with specific logic sections of the controller. In the following paragraphs, the faults are described and what to look for and where to trace in the logic is explained.

3.7.5.1 TILINE Time-out Error (System TILINE Time-out). A system TILINE time-out error message can be caused by any failure of controls or signals between the computer TILINE and the associated circuits on the controller. An example of a TILINE time-out error message is shown below:

```
TILINE TIMEOUT
Work Pointer PC And Status At Time Of Error
WP=1B38   PC=1B72   ST=240F
```

NOTE

This type of TILINE timeout error message has nothing to do with a TILINE timeout reported by the controller in status register 7 (W7). The message reported in W7 is due either to a wrong address specified by a read or write operation or to a malfunction of the master part of the controller. This type of error will be considered later.

The first step is to find out what instruction caused the error. With the aid of a diagnostic listing, identify the previous legitimate opcode before the instruction identified by PC printed out in the error message.

This is not necessarily the previous address, because the previous instruction may be a two- or three-word instruction or the instruction may have caused a branch. After the instruction has been located (it must be a memory reference instruction), the next step is to compute the effective address. This should be done by using WP and the opcode of the instruction. Two situations may occur: either the address points to a nonavailable memory location, or an address points to one of the eight control-word addresses in the controller.

Address Points To A Nonavailable Memory Location. If the address points to a nonavailable location, then the diagnostic has been altered. There is no reason that the diagnostic would be modified if all the other components of the system (memory, AU boards, etc.) work properly, unless a previous read operation of the controller has deposited some words in an area where the diagnostic resides. Unless there is some doubt about the system, the fault is due to the controller.

1. Turn the computer off and unplug the controller.
2. Check TLADR00- through TLADR14- for shorts to GND and VCC or for open connections.
3. Plug the controller board back into the extender board and turn the computer on.

4. Reload the diagnostic.

CAUTION

After the diagnostic has been loaded, DO NOT run any parts of E0 through E6 because the program may be altered in the same way as the previous case when the error was reported.

5. Be sure a scratch disk is installed and is ready to be activated.

6. Set the following command sequence in an available area of memory (for example, at address 8000) using the MM verb:

Memory Address	Data
8000	0000
8002	0100
8004	0100
8006	0000
8008	0060
800A	8100
800C	0400
800E	0000
8100	F0F0

This is a write format command of >30 words.

7. Loop on this command and check the TILINE interface signals as per figure 3-8. (Use the logic diagrams to locate the signal lines on the board.) At the question: CHECK STATUS?, respond with a 0.

8. Stop the cycling of the command by depressing the space bar on the 733 ASR.

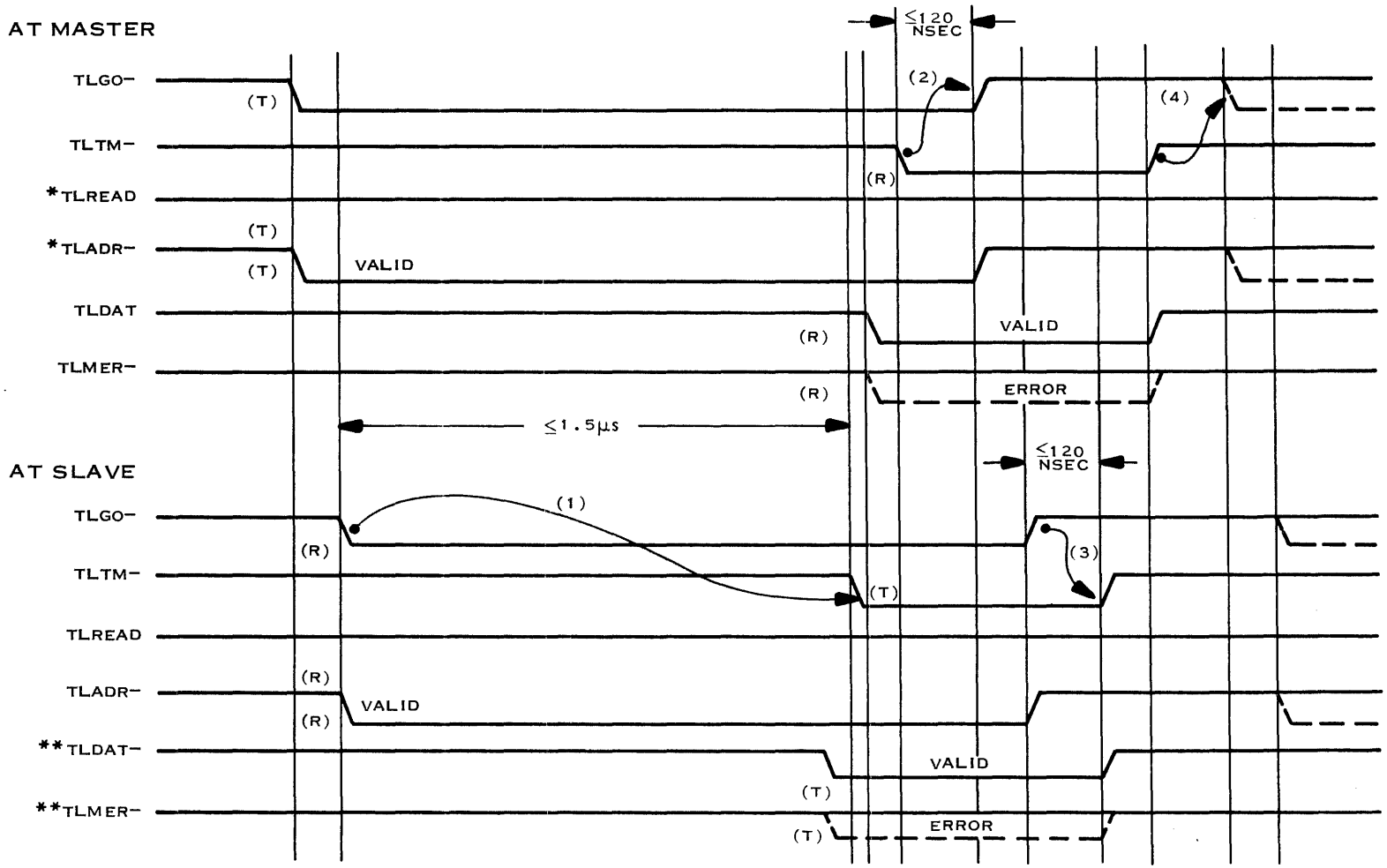
9. Set the following command in an available area of memory:

Memory Address	Data
8010	0000
8012	0200
8014	0100
8016	0000
8018	0060
801A	8200
801C	0400
801E	0000

This is a READ command and will be used to read the records previously written in step 6.

10. Loop on this command (with 0 answer at the CHECK ST? question) and check the TILINE interface signals as per figure 3-9. (Use the logic diagrams in order to localize the signal lines on the controller board.)

If the address TILINE control signals do not show any abnormality, then the MCU address lines must be verified. This can be done by using a logic analyzer or state board and setting the breakpoint to 027. Ensure that the controller sequences through the idle state in the proper sequence.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT. (TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED (R) = RECEIVED
*TLREAD AND TLADR– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED
**TLDAT– AND TLMER– MUST BE STABLE AT THE TIME (OR BEFORE) TLTM– IS ASSERTED

(A)133123

Figure 3-8. TILINE Master to Slave Read Cycle Timing Diagram

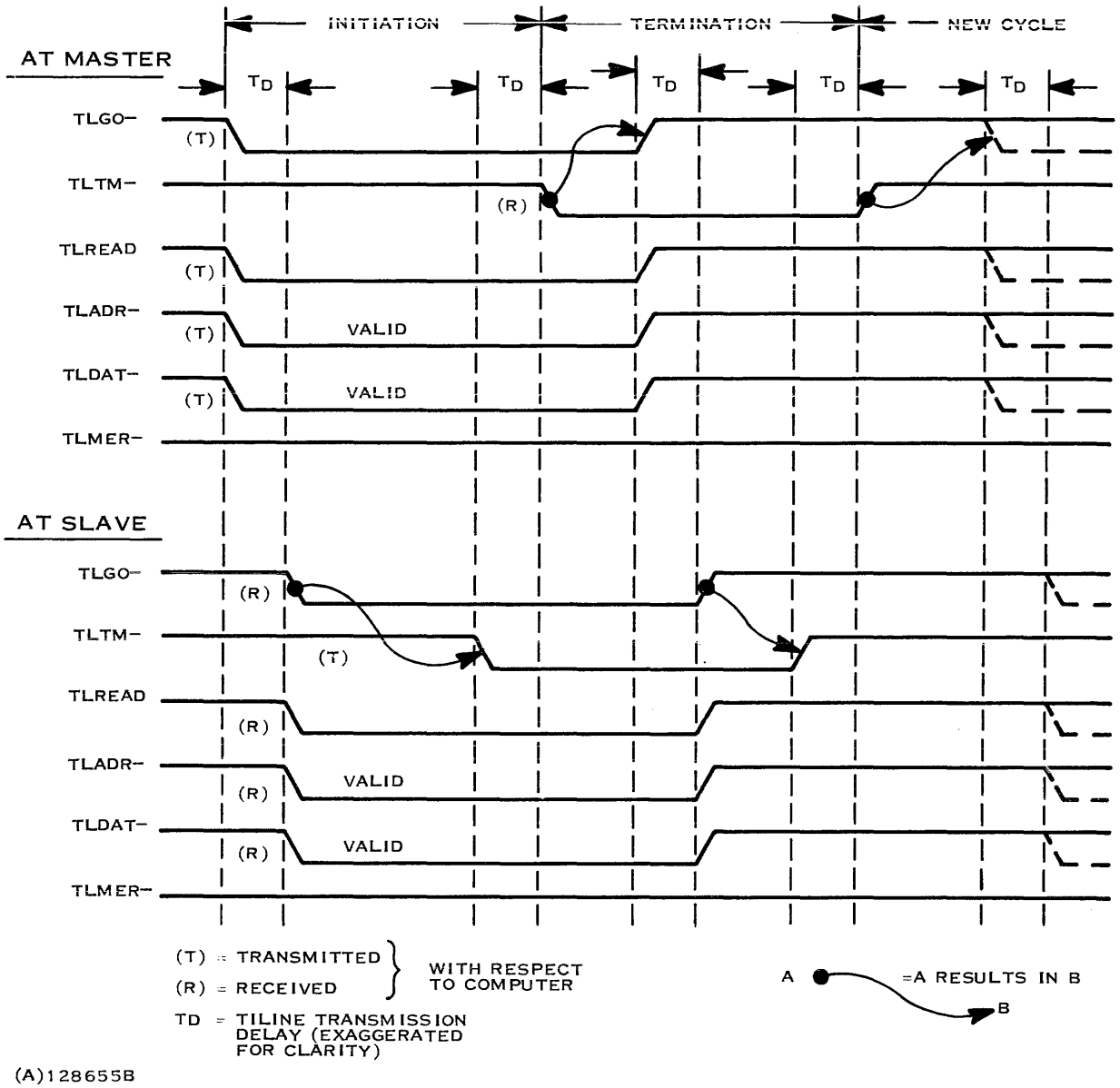


Figure 3-9. TILINE Write Cycle Timing

Address Points To One Of The Eight Controller Addresses. In this case, the failure is due to the slave part of the controller. First, be sure the DIP switches are correctly set for the proper TILINE address of the controller, as shown in Appendix A. After checking the DIP switch settings, isolate the fault, performing the following general steps:

1. Turn the computer off.
2. Turn the computer on again.
3. Try to read the eight slave registers of the controller from the front panel. These should be as shown in table 3-6.

After the last reading (location F80E), depress the MDD switch on the computer front panel again. (Read location F80E second time.) This time the content must be A900. If the readings do not correspond, perform the following steps:

a. Be sure the controller is looping on the idle loop by performing in step 10 in the paragraph titled *Address Points to a Nonavailable Memory Location.*

b. Check the PROCNT16 signal on M11 (PWB) pin 1 or UDK061 (fine line) pin 5.

c. Verify SLXFR signal on M11 (PWB) pin 2 or UDK061 (fine line) pin 4.

d. Enter the following short program (test loop 1) from the front panel switches:

Memory Address	Data	Comments
8000	C050	Move W0→W2
8002	10FE	Jump back one
8004	F80E	W0
8006	9000	W2

e. Then enter 8000 into PC, 8004 into WP.

f. Depress RUN. Loop 1 continually reads disk control and status register R7 from address F80E.

Table 3-6. Controller Slave Register Contents After Power Reset

Memory Address	Displayed Data
F800	0000
2	0000
4	FF00
6	XXXX
8	XXXX
A	XXXX
C	XXXX
E	A100

XXXX - irrelevant (can be any data)

g. Check the following signals:

- TLADR00- through TLADR19- on A05, C03, E03, C04, E04, C01, E02, E01, and C02 (PWB) or UAE039, UCC036, UBE036, UCC051, UBE051, UCC006, UBE021, UBE006, and UCC021 (fine line).
- T-type inputs on DM8136 (A02, A03, A04, PWB, or UAE050, UAE083, UAE028, fine line) to check the proper ground or VCC level.
- TLGO on M09 (PWB) or UBK072 (fine line), pin 1.
- SLGODLY on M09 (PWB) or UBK072 (fine line), pin 3.
- Check SLADOK on M09 (PWB) or UBK072 (fine line), pin 2.

- SLXFR on M11 (PWB) pin 2 or UDK072 (fine line) pin 4.
- SLVA- on G11 (PWB) or UDE072 (fine line), pin 9.
- SLVACT on J12 (PWB) or UDK039 (fine line), pin 8.
- TRAP- on H12 (PWB) or UDK072 (fine line), pin 8.
- ENSPEC- on J11 (PWB) or UEE050 (fine line), pin 15.
- TLDATEN on J08 (PWB) or UDK050 (fine line), pin 4.
- SLTM on B09 (PWB) or UBE116 (fine line), pin 4.
- TLTM- on P1 (connector) pin 20.

h. If the readings of the slaves match table 3-6, then write the word 8800 (from the front panel) in all eight locations. Check the written data. If one or more locations failed to properly load the word 8800, stop the program. Then, successively modify the location 1004 with one of the following values: F88C, F88A, F888, F886, F884, F882, F880. For each of the previous values, run the program and check the above signals.

3.7.5.2 Unexpected Interrupt Level Error Message. This error message might occur at the beginning of the PDT (while running part 0) or during the time when another program is running on the system with the disk controller. An example of this type of error message is shown in figure 3-10.

NOTE

The interrupt level (09 as shown in figure 3-10) must be that assigned to the disk controller slot.

```
VERB ? - PART 0
UNEXPECTED INT LEVEL= 09
990/10  10 MEG TEST     VERSION=XX/XX/XX
ENTER THE 733 INTERRUPT LEVEL DEFAULT-06
```

Figure 3-10. Unexpected Interrupt Level Error Message

This error message must not be confused with the UNEXPECTED INTERRUPT AT XXXX error message.

In order to isolate this type of fault, perform the following general steps:

1. Be sure the slave logic is working properly (can read from and write into controller slave registers). If necessary, perform the fault isolation procedure explained in the previous paragraph.
2. From the computer front panel, enter the following short program (test loop 2):

Memory Address	Data	Comments
8000	C401	Move W0→@W.
8002	10FE	Jump back one
8004	F80E	
8006	9000	

Then enter 8000 into PC, and 8004 into WP. Depress RUN.

Loop 2 continually loads register R7 with 9000_{16} at address F80E.

3. Check the following signals:

   - PBTLDAT- on B05 (PWB) or UAK083 (fine line), pin 1.
   - TLINT- on G05 (PWB) or UBE072 (fine line), pin 2.
   - TRAP- on J10 (PWB) or UFK017 (fine line), pin 1.
   - READ- on J10 (PWB) or UFK017 (fine line), pin 5.

If all above signals are correct, then determine if the interrupt wire is properly connected on the 990 motherboard.

3.7.5.3 Status Error Message Analysis. The controller status error messages will be analyzed in this paragraph. Figure 3-11 shows a typical status error message.

```
*STATUS ERROR
CONTROLLER STATUS COMP=X ERR=X IDLE=X
U.T.C. REG
DISK STAT COM SA S/R RA CYLA BYTEC MEMAD SEL CONT STAT
XXXX  XXXX XX  XX XX XXXX XXXX XXXXXX XX  XXXX
COMMAND ISSUED
DISK STAT COM SA S/R RA CYLA BYTEC MEMAD SEL CONT STAT
XXXX  XXXX XX  XX XX XXXX XXXX XXXXXX XX  XXXX
```

Figure 3-11. Typical Status Error Message

A status error does not necessarily indicate a controller malfunction. For example, detection of a write protect from the disk will cause the controller to set the write protect status bit. Refer to the formats of controls words W0 and W7 to determine the status conditions which will cause the controller to indicate a status error in R7, bit 2. The messages which are printed by the PDT as a result of a status error are useful in tracking down faults in the test system and in the controller.

Because this type of error message can occur as a result of malfunction of another system component (as for example a bad disk cartridge media), it is important to make a careful analysis of the error message in order to isolate the fault. In some situations, a message analysis must be combined with further action in order to isolate the fault.

There are eight fields in both Disk Registers and Command Issued rows. The data printed in each field is a hexadecimal representation of the device register contents after the operation has been completed (first row) and the data loaded into these registers at the time when the command was issued (second row).

These eight fields are:

DISK STAT	Device register 0
COM	Bytes 5-7 of device register 6; head select 10-15
SECT (SA, S/R, RA)	0-7 Sectors/record 8-15 Start sector address
CYLINDER ADRS (CYLA)	Device register 3
WORD COUNT (BYTEC)	Device register 4
MEM AD (MEMAD)	Device register 5 concatenated with bits 11-15 of device register 6 in the MSB position of the field.
UNIT (SEL)	Bits 4-7 of device register 6 (disk unit selected)
R7 STAT	Device register 7

For further analysis the meaning of each bit in the message is important. For reference see figure 1-12 (Control and Status Word Formats).

Status Register 7 Bit 15 Set. This error is reported when the controller detects the disk drive in an abnormal condition to be used. Once this status is reported, the disk status in Register 0 bits 0-7 should be checked to determine what was the cause of the unit error status. The disk status should be investigated according to the procedures listed in the following steps:

1. Check to see if R0 bit 0 is set. If this bit is set (1), then the drive has not been selected properly or the status from the disk is not being seen or reported properly by the controller. Check the following signals. If any are found to be faulty, signal trace through the logics until the fault is isolated. Check the following signals on the controller.

   - SELECTB- on R06-2 (PWB) or UJJ017-6 (fine line)
   - SELECTA- on R03-6 (PWB) or UJJ017-2 (fine line)
   - DISKSEL- on R06-4 (PWB) or UJJ061-12 (fine line)

   NOTE

   These lines are decoded at the disk drive and are used to select a particular drive and platter.

	Select B-	Select A-	Disksel
Drive 0	0	1	0 Fixed
	0	1	1 Removable
Drive 1	1	0	0 Fixed
	1	0	1 Removable

If these signals are not of proper value, be sure that the proper unit select bits have been entered into register 6 of the controller. If these signals are good, then the status lines from the disk should be checked. Probe the following signals:

- OFFLINE- on R08-12 (PWB) or UJD006-8 (fine line) or FILERDY- on R08-13 (PWB) or UJD006-9 (fine line)
  If FILERDY- is a logic low, then the disk drive is reporting proper status and the problem should then be signal traced through the logics until the fault is found. If FILERDY is a logic high at this point, then the drive is reporting improper status. Turn power off on the computer and disk drive and check resistances on this line between the drive and controller, insuring that no shorts or opens exist in the cable or between signals on the board.

  A good way to trace the OFFLINE status through the logics is to put the controller in the following loop:

Memory	Address
8000	C050
8002	10FE
8004	F800
8006	8000

  Then enter 8000 into PC, and 8004 into WP. Depress RUN.

  This continually reads register R0 and loads it into memory.

  Check: — PBDSKSTA- on R05 pin 1 (PWB) or UJD028 pin 19 (fine line)

  — TLDATA00- on A06 (PWB) or UAE061 (fine line) -6

2. Once R0 bit 0 is a logic 0 to show that the unit is selected, the other status bits can then be checked for problems. The next status bit from the drive that should be checked is R0 Bit 1, the ready status bit. Check the following:

   - RDYSRW- on R08 (PWB) or UJJ039 (fine line) -1

   When the drive is selected and the unit is idle, the RDYSRW- line should be at a low logic level. If this line is low but the status is still being reported bad, the same loop as given in step 1 should be run and this signal then traced through the logics and out onto the TILINE.

NOTE

If the state display is used to stop on breakpoints to check signal levels, the system will have TILINE timeouts because the controller will be stopped and not respond properly to the TILINE commands.

3. If R0 bit 2 (write protect on) is reported in the disk status register when the unit error status bit 15 in register 7 is reported, the drive write protect switches should be checked. These switches are active when depressed and the indicator is lighted. If this switch is ON, it should be deactivated provided a scratch cartridge has been installed or the fixed disk does not contain needed information. If the write protect status is being reported when it has not been selected at the drive, the input line from the drive should be checked. Check the following signals:

   - WP- on R05 (PWB) or UJJ050 (fine line) -8
   - PBDSKSTA- on R05 (PWB) or UJJ050 (fine line) -1

   Signal trace the write protect (WP-) status line through the controller and out to the TILINE until the problem is isolated. If a read command is being issued to the drive and the write protect has been selected, the controller should not be reporting unit error status in register 7. If this is happening, then check the write gate (WG-) at R02 pin 11 (PWB) or UJD050 pin 8 (fine line). This signal should not be going to a logic low level; if it is, trace the signal back through the logics until the fault is isolated.

4. If R0 bit three becomes set upon the issuing of a command, the controller will report a unit error status in R7. If this should occur, the fault should be cleared by either depressing the FAULT/RESET indicator/switch on the drive front panel or by issuing a RESTORE command to the drive. If the indicator should fail to become extinguished, the problem causing the fault is solid. The first thing that should be done is to unplug the controller to drive cable and depress the FAULT/RESET indicator/switch. If the light stays on, then the fault condition is in the drive, but if the light becomes extinguished, then the fault condition is caused by the controller. The controller should be reconnected to the drive and a disk command should be set up in memory and issued (looped on) such that the fault is obtained. An example of a command issued is shown below (use MM verb):

Address	Data	Comments
8000	0000	Disk status and interrupts
8002	0010	Disk command
8004	0100	Sectors per record/record address
8006	0060	Cylinder address
8008	0050	Byte count
800A	9000	Memory address (data source)
800C	0400	Unit select (removable)
800E	0000	Controller status
9000	F0F0	Data to be written

Once this has been entered in memory, enter an @ on the keyboard to get back to verb decoding. Then enter an LO command and answer with a "1" to the number of commands to be executed and a 0 for check status. The command should then be repeatedly executed by the controller. The FAULT/RESET indicator on the drive should now come on and stay on and should not stay off when depressed. Once the failure mode has been caused by the controller, the following signals on the controller should be checked:

- WG- on R02-11 (PWB) or UJD050 (fine line) -8
- EG- on R02-6 (PWB) or UJD050 (fine line) -3
- RESTORE- on R04-6 (PWB) or UJJ061 (fine line) -6

- HDSEL- on R03-10 (PWB) or UJJ028 (fine line) -10
- ADDSTB- on R02-3 (PWB) or UJD050 (fine line) -11
- FILERDY- on R08-13 (PWB) or UJD006 (fine line) -9

When checking these signals, ensure that the write and erase gate are turning on and off within approximately 10 microseconds of each other. The restore signal should not be active if commands other than a restore command are being executed. The head select line should be stable and should not be toggling unless multiple commands with different head selects are being executed. Sync the scope on ADDSTB- on channel one and look at signal FILERDY- on channel two. FILERDY- should always be a logic low when ADDSTB- goes to a logic low (on negative edge).

If any of these signals does not meet the above criteria or is not of proper voltage level or waveshape, then that signal should be traced through the controller until the fault is isolated.

5. If a unit error in register seven status was set and bit 5 in register 0 (R0) was set, then the fault was the result of a seek incomplete or illegal cylinder address (address interlock) being reported by the disk drive. To troubleshoot this type of failure, set up the same type of command as shown in Step 4. It may be necessary to try various cylinder addresses (address 8006) before a failure is reported. Once a command has been set up that will report the error, the error status reporting should not be selected and the interface signals to the drive should be checked. Check the following signals:

   - ADDSTB- on R02-3 (PWB) or UJD050 (fine line) -11
   - ADD001- on R06-12 (PWB) or UJJ028 (fine line) -8
   - ADD002- on R06-8 (PWB) or UJJ061 (fine line) -4
   - ADD004- on R03-4 (PWB) or UJJ017 (fine line) -10
   - ADD008- on R04-8 (PWB) or UJJ028 (fine line) -12
   - ADD016- on R06-6 (PWB) or UJJ061 (fine line) -2
   - ADD032- on R03-8 (PWB) or UJJ017 (fine line) -4
   - ADD064- on R04-12 (PWB) or UJJ017 (fine line) -8
   - ADD128- on R04-4 (PWB) or UJJ028 (fine line) -2
   - ADD256- on R04-10 (PWB) or UJJ028 (fine line) -4

   When probing these signals, sync the scope on ADDSTB- and look at the various address signals issued to the drive. These signals should be stable approximately 500 nanoseconds before address strobe goes active and should remain for approximately 500 nanoseconds after ADDSTB- is removed.

   By changing the address at 8006 and reissuing the command, each of the address lines can be made to toggle. Each bit location should be checked for proper level and to insure that the proper address (same as in Memory Location 8006) is being loaded into the D-Bus and is being presented to the drive.

With channel one connected and synced on ADDSTB-, look at address acknowledge (ADDACK-) and ensure that the trailing edge of strobe is not turned off until the address acknowledge signal (ADDACK-) is received at P07-11 (PWB) or UJJ039-9 (fine line).

Status Register 7 Bit 14 Set. When this status is reported, the controller has failed to detect the sync character within the sector that it started reading from. The controller is designed such that it will automatically attempt one retry when a search error is reported. This means that the controller has attempted to read that sector twice before reporting the error. The controller checks for this error by reading the sector address and when the desired sector is found, the controller clears the sector latch/flag and starts polling the READQ status and the sector status. If the controller finds that the sector status has become active (sector pulse occurred) before the READQ status line, then a sector frame was read without a sync character being detected, causing a search error to be reported.

This type of failure is best found by setting up a scoping loop and probing the associated control signals. The disk should be formatted first to ensure that all sectors have proper information. Once this has been done a write data command should be set up in memory as listed below:

Memory Address	Data	Comments
8000	0000	Disk status
8002	0300	Write data 0200 R0 data
8004	0100	1 sector/record
8006	0000	Cylinder address
8008	0060	Byte count
800A	8300	Write 8200 read
800C	0400	Unit select (fixed)
800E	0000	Controller status

Once this data has been entered in memory, initiate the command by issuing an IC command. Once this has been completed, change to a READ DATA command by changing the contents of memory location 8002 from 0200. The controller should execute the command, and the erroring status should be reported. To find the fault, put the controller in a looping command LO at address 8000 with status checking not selected (0). The following signals on the controller should then be checked:

- SECTORMRK- on P04-6 (PWB) or UHJ039-8 (fine line)
- SECTORMRKQ- on J05-12 (PWB) or UFK039-12

If these two signals are always active, probe CLRSECIDX- on P04-1 (PWB) or UHJ039-13 (fine line). This signal should pulse low during the cycle to clear the latch. If it does not pulse low, trace the signal until the fault is isolated. If the two signals listed above never went to the active (low) state, then P04-1 (PWB) or UHJ039-13 (fine line) should be checked to insure that this signal is not being held at a constant low level. If this signal is functional, P04-3 (PWB) or UHJ039-11 (fine line) (SECMRK) should be checked to insure the controller is receiving sector pulses from the disk drive (20 per revolution).

If the above signals were all correct, then the following signals should be probed.

Sync the scope (channel 1 at P04-3, PWB, or UHJ039-11, fine line) and observe the following signals.

RG- on R03-2 (PWB) or UJJ028-10 (fine line) (active ≈ 40 microseconds after sector pulse for sector zero)

- DSKSTRQ on R11-9 (PWB) or UJJ116-9 (fine line) (becomes active after sector pulse on sector address 0 for command given).
- DSTARTQ- on R11-6 (PWB) or UHJ094-6 (fine line)
- STRTREAD- on R10-6 (PWB) or UGE116-12 (fine line) (goes positive after DSTARTQ goes active).
- SYNC6E- on N02-8 (PWB) or UJD083-8 (fine line) (check to see that this signal goes low about 78 microseconds after the sector pulse for sector address 0).

If SYNC6E- is going negative (detecting the sync pattern from the disk) the following signals should be traced:

- SYNCQ on N12-9 (PWB) or UGE094-9 (fine line)
- READQ- on L12-8 (PWB) or UHD094-8 (fine line)
- READQQ- on J05-7 (PWB) or UFK039-7 (fine line)

If SYNC6E- did not go negative at the appropriate time, trace the data path back through the logics ensuring that data is being received from the drive properly. Check the following signals:

- PARDAT (9-15) on N02 pins 2-6, 11, and 12 (PWB) or UJD083 pins 1-4, 6, 11, and 12 (fine line)
- DISKDATIN- on N02-1 (PWB) or UJD083-5 (fine line)

If the parallel data is not passing data properly but DISKDATIN- seems to be toggling properly, trace the data through the serial/parallel register (M03, M04, L04 and L03, PWB, or UHJ083, UHD083, UFK061, and UFK083, fine line). If DISKDATIN is not toggling properly, check the following signals:

- RDATAQ on P03-5 (PWB) or UHD116-9 (fine line)
- RDATA on P09-6 (PWB) or UHJ116-8 (fine line)
- RDATA- on N11-8 (PWB) or UJD116-6 (fine line)
- RDB on N11-12 (PWB) or UJD116-2 (fine line)
- RDA- on N11-10 (PWB) or UJD116-4 (fine line)
- DCLK on L07-14 (PWB) or UFK116-14 (fine line)

Insure that the DCLK signal has a 400 nanosecond pulse width and an off time of approximately 100 nanoseconds.

If the read data path is deemed to be working properly, then the problem may be that write data path is faulty. Stop the command and by using an MM verb, change the command to a write format command. Change data at memory location 8002 from 0200 to 0100. Once this has been done, put the controller back in a looping command at address 8000 with status being ignored. Once this has been done, probe the following signals and trace any problems found through the logic until the fault is isolated.

- WG- on R02-11 (PWB) or UJD050-8 (fine line) turns on after leading edge of sector pulse and turns off after CRC has been written, which should occur before leading edge of the next sector pulse.
- EG- on R02-6 (PWB) or UJD050-3 (fine line) turns on and off within 10 microseconds of WG-
- WDNCLK- on R02-8 (PWB) or UJD050-6 (fine line)
- WCLK on R02-9 (PWB) or UJD050-4 (fine line)
- WDNCLKEN on N08-11 (PWB) or UJD105-3 (fine line)
- WRDATOUT- on N07-6 (PWB) or UHD116-6 (fine line)
- WRTDATD on N06-7 (PWB) or UHD105-7 (fine line)
- PARDAT00 on N06-5 (PWB) or UHD105-5 (fine line)

If PARDAT00 does not seem to be toggling properly, trace the data through serial/parallel register looking for a bad bit.

NOTE

The sync character for the ID field will be written on the disk approximately 78 microseconds after the leading edge of the sector pulse. All zeros will be output prior to this time.

If the data is not being passed properly in the serial/parallel register, check the controlling inputs. Check that DISKDATLD- on N09-6 (PWB) or UJD094-6 (fine line) is pulsing on every 16 disk clock pulses. If not, trace this signal until reason is found. If the input data to this register is not charging, probe the FIFO chips and assure that the input data lines are functioning properly and the input/output control signals are functioning properly.

Status Register 7 Bit 13 Set. When this status bit becomes set, the controller is reporting the fact that it had tried to execute a disk command but failed to complete the operation in the allotted time (200 milliseconds). The first thing to do is to issue various commands to the disk until this failure is reported. After this, a logic analyzer or state board should be used to find out where in the command the controller is hanging up. This is easily done by setting the breakpoint on the first address of the command timer interrupt routine (040) and then looking to see what the previous address was. Once this address is obtained, the function the controller was trying to execute at the time can be found by looking back at the previous address. By finding this address in the microcode flowcharts (Appendix D), the failing operation can be isolated and the circuitry of this operation can be investigated by putting the controller in a scoping loop with status errors deleted.

When the controller detects this type of error, it turns on the Red Fault LED on the top of the controller board. When the controller services this interrupt and goes through the terminate routine, the fault LED is turned off. After this status is reported, the operator should observe the fault LED. If the LED remains lighted, it indicates that the controller failed to sequence through the terminate routine properly or the command timer circuitry itself is bad. Check these signals:

- CMDTMRDLY- on J07-7 (PWB) or UFE105-7 (fine line)
- FAULTQ- on H11-11 (PWB) or UFK050-11 (fine line)

If CMDTMRDLY- is active then check to see if the controller is in the idle loop. When in the idle loop, the timer should be being cleared. Trace the signal back until the reason it is not being cleared is found. If it is not in the idle loop, then the MCU address generation logic should be probed.

If the command timer and fault latch are cleared, but the status bit in R7 has been set, then the controller sequencing is probably functioning properly but one of the test conditions the controller is waiting for (such as address acknowledge, FIFO available, sector address compare, etc.) did not occur. By breakpointing on entry point of the interrupt and looking back at the previous address, the problem circuitry should be identified and the fault isolation should just be a matter of tracing these signals through the logics.

Status Register 7 Bit 12 Set. This type of an error is caused by the FIFO not being ready to receive or give a word when required by the controlling signals. If the controller is writing data to the disk, it must keep data in the FIFO so the drive can continually pull words out and shift them serially to the disk. If the controller is taking words from the disk and putting them in memory, it must keep the FIFO from becoming full and unable to accept the words in as they are ready, thereby losing information. The rate error detection flip-flop is set (causing trap to rate error interrupt routine on controller) by having a shift pulse when the ERRORSET (INRDY-/OUTRDY-) signal is active. To find this type of pulse, put the controller in a read or write data loop and signal trace from the rate error detection flip-flop back until the problem is isolated. Check the following signals:

- TIMERRQ on N12-6 (PWB) or UGE094-6 (fine line)
- ERRORSET on N12-2 (PWB) or UGE072-12 (fine line)
- SHIFT on M05-9 (PWB) or UGE050-9 (fine line)

Check that a shift pulse is occurring every 15 DCLK pulses, once the disk operation is started. If ERRORSET is always positive, then the FIFO is never coming ready. Trace OUTRDY- back if doing write to disk and INRDY- if reading from the disk until the reason these signals are not going ready is determined.

Status Register 7 Bit 11 Set. This status indicates that the header information read from the disk failed to agree with the data for that command resident in the controller registers. Another possibility is that the CRC character for the three header words was wrong. The first thing is to do an UNFORMATTED READ data command at the location where the ID error occurred. Set up the following command in memory using the erroring sector address and cylinder address as entries to the command:

Address	Data	Comments
8000	0000	Disk status
8002	0400	Disk command (unformatted RD)
8004	01XX	Erroring starting sector address
8006	XXXX	Error cylinder address
8008	0060	Byte count
800A	8100	Memory address
800C	0X00	Unit select
800E	0000	Controller status

X — these values are entered from the values given in the error status reporting.

Once this data has been entered, this command should be executed by entering an IC command after verb and then depressing the space bar. The values of the header information read from the drive should be read from memory and compared with the command entered. To do this, enter an MM at address 8100 and depress the space bar three times. The CRT or ASR will then display the header words read from the disk. The first word displayed is the track address where the heads are to be positioned. This data should be the same as the information entered in register 3 of the controller word (same as memory location 8006). If these two registers do not compare, the most likely cause of the problem is a faulty cylinder address issued from the controller to the disk drive. If these values do not compare, the value loaded in the disk address should be probed and any discrepancies should be investigated.

NOTE

The header word containing the cylinder address will also have the head select added to the word. The head select bits are given in bit locations 0-4 and the cylinder address bits are given in bits 5-15.

If the cylinder bits compare, check that the proper head select was read. Compare the word read from the disk (bit 4) with the head select of the command issued. If they do not compare, probe the head select bit to the drive.

The second header word is the sector per record and sector starting address. The second word read from disk should compare with the value in register 2 of the command issued. If these words fail to compare, the sector address logic received from the disk and read by the controller may be faulty. Probe SECTORB(1-16)- on R07 pins 8, 6, 4, 2, and 17 (PWB) or UJD028 pins 8, 6, 4, and 2 and UJJ050 pin 17 (fine line) for proper pulses.

The third word contains the word count of the number of data words stored. This value is not compared with controller register values.

If the words compare properly but the status bit still is reporting the ID failure, the error would be reported from a CRC miscompare on the header words. This type of error should be checked by carefully observing the data path that feeds the CRC generator for both write format and read data operations.

Status Register 7 Bit 10 Set. This status error tells that the controller was attempting a TILINE master cycle but failed to complete the operation within the 10 microseconds allotted by the controller. Once the controller decides to do a master cycle it starts a 10 microsecond delay, during which time the controller must acquire access to the TILINE and complete the cycle before the delay value is reached. If the controller does not complete its operation in time, the time delay will cause an internal interrupt, stop the master cycle, report the erroring status, and go back to the idle loop to wait for another command. Either the TILINE handshake circuitry is failing or the TILINE address output by the controller is an illegal value.

One of the most effective methods of troubleshooting this type of failure is to disable the TILINE timer, causing the system to hang so that the signals can be probed. The fault causing the error should be isolated quite easily. The timer is disabled by connecting a ground wire to B09 pin 15 (PWB) or UBE116-15 (fine line). Once this has been done, the MASTER CYCLE command that had caused the error should be reissued. The controller should not be hung with the fault condition causing the problem. The first thing that should be checked is the TILINE address that the controller is gating to the TILINE [TLADR(00-19)-]. Ensure that a valid address is present on the TILINE and that all lines are within logic voltage specifications. Once the addresses have been verified to be good, the handshake interface signals should be probed. Check the following signals and verify that they are correct:

- TLGO- on A08-15 (PWB) or UAE094-15 (fine line)
- TLREAD on A08-2 (PWB) or UAE094-2 (fine line)
- TLTM- on B09-2 (PWB) or UBE116-2 (fine line)
- TLAV on B09-7 (PWB) or UBE116-7 (fine line)
- TLAK- on B09-9 (PWB) or UBE116-9 (fine line)

In addition to these signals, check the signals that can cause the TILINE circuitry to be disabled. Insure that none of these signals are active.

- TLIORES- on A08-7 (PWB) or UAE094-7 (fine line)
- TLWAIT- on A08-9 (PWB) or UAE094-9 (fine line)
- TLPRES- on L07-5 (PWB) or UFK116-4 (fine line)
- TLPFWP- on A10-1 (PWB) or UAK105-2 (fine line)

If all of these signals are of proper polarity and have good voltage levels, then the TLTM- signal should be traced to find out why the controller has not relinquished the use of the TILINE. If all signals are normal and the cycle completes normally, the ground should be taken off the delay circuit, a scoping loop should be set up, and the time delay of the TILINE timer should be checked. Probe B12-8 (PWB) or UBE094-8 (fine line) and see that it goes low approximately every 10 microseconds when looping on a MASTER CYCLE command with status reporting deleted.

Status Register Bit 9 Set. This bit is set whenever the controller reads information from the disk and the CRC generator has not gone to zero when the data and CRC character have been passed through the CRC generator chip. This essentially means that the information written to the disk is not the same as the data read back.

NOTE

Care must be taken when doing UNFORMATTED READ or UNFORMATTED WRITE commands. If the exact number of words for the UNFORMATTED READ are not the same as the number of UNFORMATTED WRITE, a data error will result. Also, if an UNFORMATTED READ is used to read data that has been written with formatted data, a data error will result if more than three words are specified (Header Data).

The first thing that should be done is to determine if the data paths are good or bad or if the CRC generator/checker logic is at fault. This is best done by running test 5 (E5) of the PDT or by use of WRITE/READ commands and looking at the data returned from the disk. If it is decided to check the data by using the WRITE/READ commands, enter and issue the following commands after the disk has been formatted:

Memory Address	Data	Comments
8000	0000	Disk status
8002	0500	Unformatted write (400 unformatted read)
8004	0100	1 Sector/record
8006	0000	Cylinder 0
8008	0240	Maximum byte count
800A	9000	Starting address for data
800C	0400	Removable disk
800E	0000	Controller status

After this command has been entered, the PDT should be put back to verb decoding mode by entering an @ on the keyboard. The data to be written should be entered by issuing an MI command at address 9000. When it asks for data, an easily recognized pattern should be entered, such as AAAA or 5555. Once this has been done, do an IC command at address 8000 to write this data out to the disk. After this has been completed, change the data at 8002 from 0500 to 0400 (Unformatted Read) and the data at 800A from 9000 to 9300. Clear the memory at location 9300 to all zeros, using an IM command. Now issue the command at 8000 and then check to see what the data transferred was. The data at 9300 should now read what was written to disk (AAAA or 5555). Carefully observe the data for any irregularities such as a bit stuck at one or zero. This type of failure seems to represent something wrong with the parallel data path and not the serial disk interface portion. To troubleshoot this, put the controller in the write mode and look at the data stream for the proper data pattern. If the data pattern is not correct, trace the problem back until the problem is located. If the write data path looks good, put the controller in a read cycle and trace the data coming from the disk until the fault is found. If the data received from the disk was the same as the data sent to the disk, but a data error was still reported, then the problem may be with the CRC generation logic. Check the following signals:

- CRCPRES- on M06-2 (PWB) or UGE105-2 (fine line)
- CRCENFLAG- on M06-10 (PWB) or UGE105-10 (fine line)
- CRCDATIN on M06-11 (PWB) or UGE105-11 (fine line)
- CRCDATOUT on M06-12 (PWB) or UGE105-12 (fine line)
- CRCERR on M06-13 (PWB) or UGE105-13 (fine line)

If irregularities are found, replace the CRC chip at M06 (PWB) or UGE105 (fine line).

Status Register 7 Bit 8 Set. This status indicates that the device sending data to the controller has detected bad parity on this data. When this condition is reported to the disk controller, the controller traps to an interrupt routine (command aborted) and reports this status in controller status register 7.

To troubleshoot this type of error the command being executed when this status is reported should be put in memory and put in a looping command such that the controller signals can be probed.

Once this has been done the signal TLMER- on A10 pin 5 (PWB) or UAK094 pin 3 (fine line) should be probed. If this signal never goes low but this status is reported, then the problem lies in the controller logic. This signal should be traced through the logic until the reason that this interrupt is being reported is found. Ensure that an interrupt trap is being generated (INTTRAP on M12-3 on the PWB or UFE006-6 on the fine line version of the disk controller). If this is being generated, it should be a matter of tracing the signals until the fault is isolated. If this signal is not being produced but this status is being reported, then the problem most likely is in the address sequencing logic. Probe these signals to see why the microcode is sequencing through the interrupt.

Status Register 7 Bit 7 Set. This status is caused by the controller receiving a TLIORES-, TLPFWP- or TLPRES- from the TILINE. Any of these signals will cause the controller to trap to interrupt 0 and set this status in register 7. All operations in progress are suspended at this time.

To troubleshoot this type of failure, the controller should be put in a scoping loop with status checking deleted. Once this has been done, probe F09-1 (PWB) or UEE094-1 (fine line) (TLPRES-) and F09-11 (PWB) or UEE094-11 (fine line) (TLABORTL-) to see which one is going to a logic low level causing the interrupt and error reporting status. It should now be just a matter of tracing the erroring signal back through the logics until the fault is isolated.

Status Register 7 Bits 7-15 Set. This condition tells that the controller experienced a self-test diagnostic failure while executing one of the commands. This type of failure is troubleshot by first reading the status count in register 2 of the controller (enter F804 on front panel, depress MA and then depress MD and record the value on front panel). After obtaining the status count, look at status error printout and see what type of command was being executed (R11) at the time of the failure. If it was anything other than a store registers command, the controller was executing the short diagnostic test when the error was encountered. Refer to table 3-3 (Status Error Decode) and find the status error count (if short test failure) that corresponds to the long test count. Once the corresponding long test count failure status count has been found, the troubleshooting procedure for that status count given in section 3.6.6 should be followed until the fault is isolated.

NOTE

Because the status is updated after the successful completion of a test, the procedure to follow in troubleshooting must be the next one from the status count given. If status count was FF07, then follow procedure for FF08 in section 3.6.6.

Special Diagnostic Error Messages. The PDT is composed of five major tests. The major tests are broken down into smaller subtests that comprise the larger test. How each test is broken down and what each test does is described in paragraph 3.7.2. Errors encountered during the executing of the PDT that result from the failure of a unique test will result in a specific printout telling what test failed. This will be accomplished by the following message being printed preceding the error message:

ERROR IN TEST XXXX

The leftmost two bits will identify the major test that the failure had occurred in (E1-E5). The rightmost two bits identify which of the subtests was being executed at the time of the error. By reading the error message following this printout and by reading the test description given in paragraph 3.7.2 for this failing test, a good idea of where the problem lies should have been obtained. If a step-by-step description is desired to troubleshoot this problem, the status error that closest resembles this problem should be followed. By reading the description of the failing test, a command sequence can many times be set up to duplicate the error. Once this has been done, a status error will be reported and the detailed procedure for troubleshooting this type of problem can be followed.

APPENDIX A

INSTALLATION DATA AND SWITCH SETTINGS

APPENDIX A

INSTALLATION DATA AND SWITCH SETTINGS

The following installation data has been reprinted from *Model DS10 Cartridge Disk System Installation and Operation,* P/N 946261-9701.

WARNING

This short-form tabulated data is not a substitute for the installation and operation procedures in the installation and operation manual. This information is supplied here solely for convenience in working on, or with, a properly installed disk controller and drive.

A.1 DISK CARTRIDGE INSTALLATION AND REMOVAL.

Before installing or removing a disk cartridge from the disk drive, be sure that the spindle of the disk drive is not rotating. Do not attempt to install or remove a cartridge unless the brush indicator on top of the disk drive is aligned with the black area as shown in figure A-1. A coin or screwdriver may be used to make the alignment.

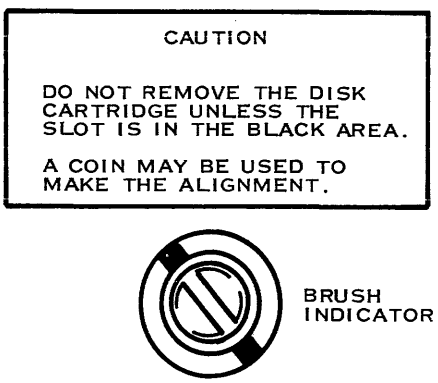


Figure A-1. Brush Indicator

A.1.1 Disk Cartridge Installation.

1. Raise cartridge access door (cabinet mount) or pull disk drive out of rack (rack mount).

NOTE

Power must be on and START/STOP lamp must be extinguished to release lock on hold-down arms.

Refer to figure A-2 for the remainder of this procedure.

2. Pull back hold-down arms.

3. Set disk cartridge upright on a firm supportive surface.

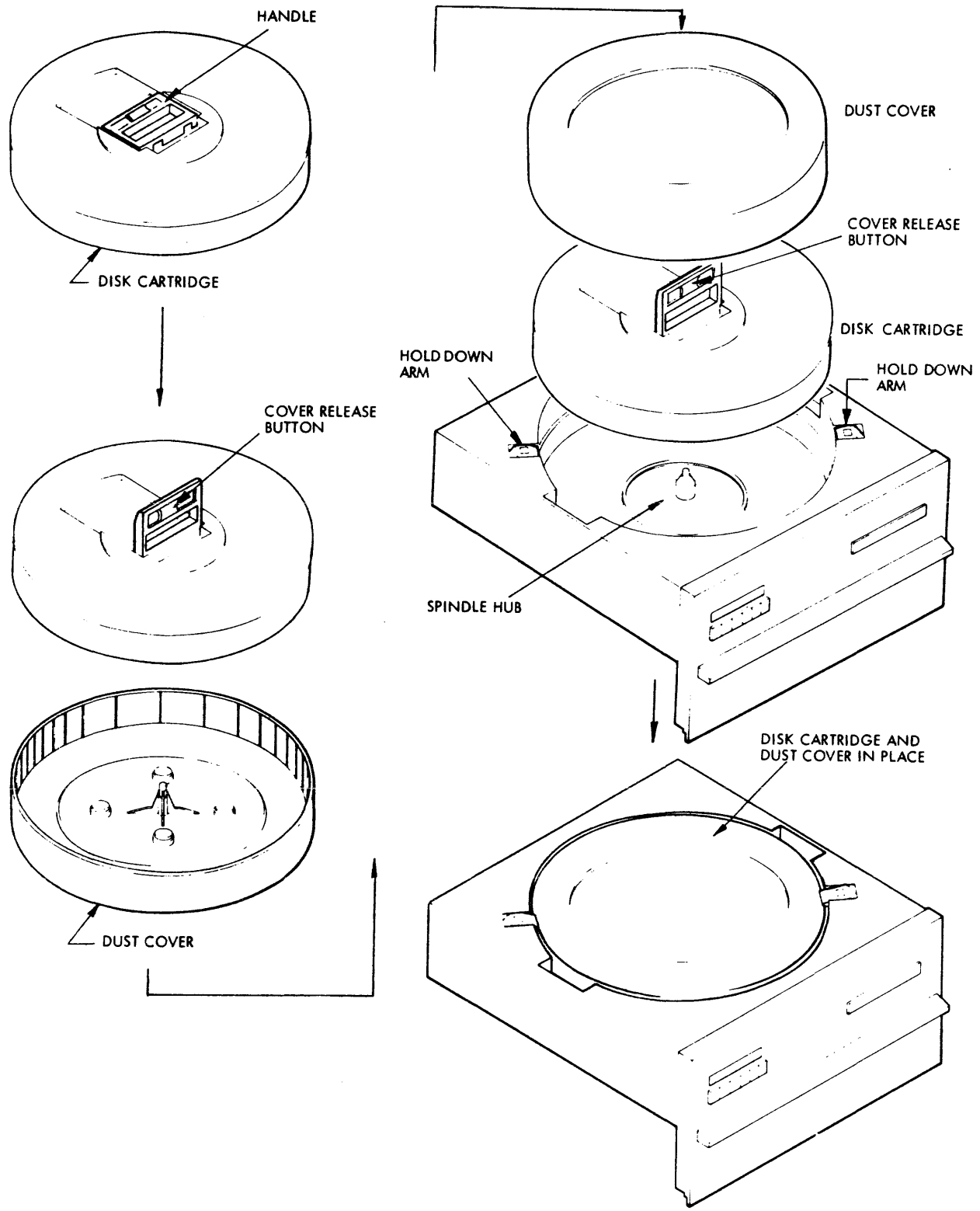


Figure A-2. Disk Cartridge Installation

NOTE

There are two types of disk cartridge available. One type has a dust cover lock that disengages when the slide button is moved to the left. The other type disengages the lock when the slide button is pushed towards center.

4. Push disk cartridge cover release button to left, or towards the center depending on the type cartridge, while lifting cartridge handle to separate dust cover and disk.

5. Disengage dust cover from disk. Set cover aside.

CAUTION

Do not make abusive contact between disk and spindle. Ensure that the read/write heads are fully retracted and the brushes are completely out of the disk area. Remove any dust from magnetic chuck.

6. Position head opening of disk toward rear of disk drive and place disk onto spindle hub.

7. Rotate cartridge slowly back and forth until cartridge seats over spindle.

8. Turn handle down to seat cartridge.

9. Place dust cover (removed in step 5) open end down over cartridge.

10. Position hold-down arms over cartridge and dust cover.

11. Close cartridge access door (cabinet mount) or push disk drive into rack (rack mount).

A.1.2 Disk Cartridge Removal. Refer to figure A-2 for the following procedure.

1. Press START/STOP switch and wait for START/STOP indicator to be extinguished.

CAUTION

If START/STOP indicator is still illuminated after 2-1/2 minutes and brushes are not fully retracted contact the customer service engineer.

2. Raise cartridge access door (cabinet mount) or pull disk drive out of rack (rack mount).

3. Pull back hold-down arms (arms will not move until cartridge rotation has stopped and START/STOP indicator is extinguished).

4. Remove cartridge dust cover.

5. Push cartridge release button to left, or towards the center, while lifting cartridge up and out of disk drive by handle.

6. Place cartridge inside dust cover and hold down handle until a snap is heard indicating that the cartridge and dust cover are locked together, or slide the release button away from the center.

7. Close cartridge access door (cabinet mount) or push disk drive back into rack (rack mount).

NOTE

If no cartridge is to be installed for any long period of time, install the dust cover received with the disk drive.

A.1.3 Removal of Disk Cartridge Following Power Failure or for Emergency. Removal of the disk cartridge following power failure or in an emergency situation, should be performed only by the customer service engineer.

1. Wait approximately three minutes for cartridge to stop spinning.
2. Raise cartridge access cover (cabinet mount) or pull disk drive out of rack (rack mount).
3. Release pack locks by inserting a flat head screwdriver (or similar object) into hole on top of pack lock (see figure A-3). Press solenoid plunger into solenoid and tilt pack lock.
4. Pull back hold-down arms.
5. Remove cartridge dust cover.
6. Lift cartridge handle, hold cover release button to left, or towards the center, and lift cartridge up and out of disk drive by handle.
7. Place cartridge inside dust cover and fold down handle until a snap is heard indicating that the cartridge and dust cover are locked together, or slide the release button away from center.
8. Close cartridge access door (cabinet mount) or push disk drive back into rack (rack mount).

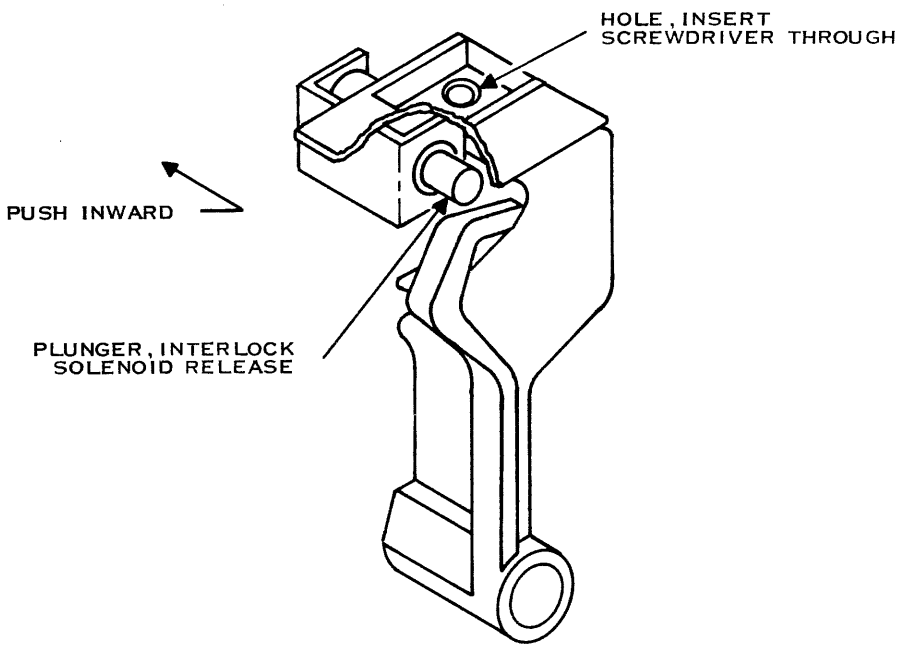


Figure A-3. Cartridge Locks

A.2 CHANGING DISK LOGICAL UNIT NUMBER ASSIGNMENTS.

The fixed disk in the primary (or only) disk drive is normally designated disk 0, and the cartridge is designated disk 1. The corresponding designations for the secondary disk drive are disks 2 and 3. A jumper on the cable adapter board permits reversing the designations for a given disk drive.

The jumper plug is normally stored as shown in figure A-4. To reverse designations for disks 0 and 1, remove the jumper plug and insert it to connect J1 and J3. To reverse designations for disks 2 and 3, remove the jumper plug and insert it to connect J1 and J4.

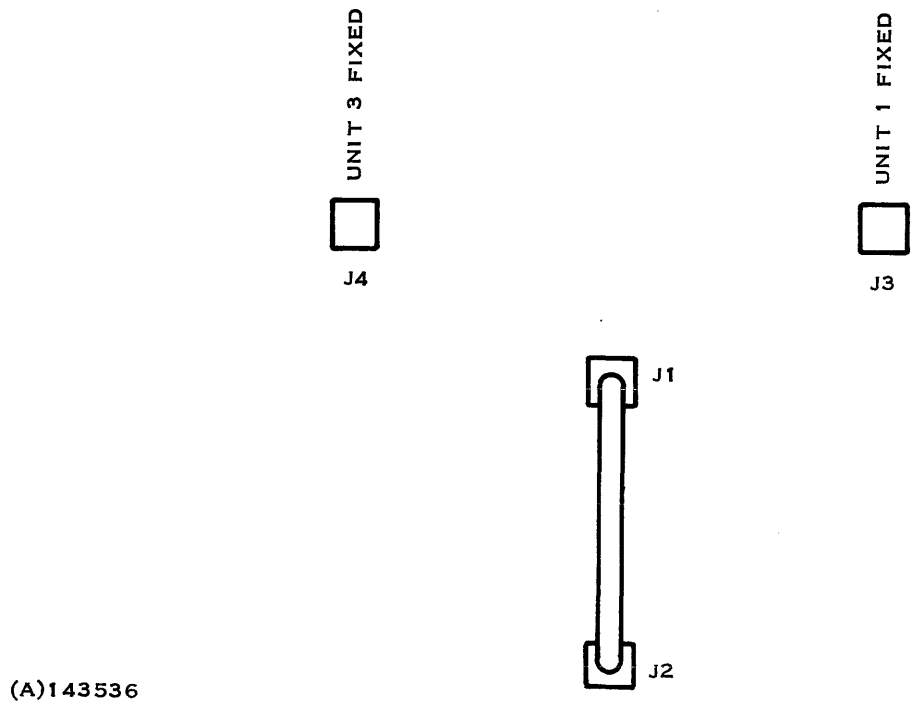


Figure A-4. Disk Designation Reversing Jumper on Cable Adapter

A.3 CHANGING TILINE SLAVE ADDRESS SWITCH SETTINGS.

The disk controller is assigned a block of eight TILINE word addresses, corresponding to command words W0-W7 (and to internal registers R0-R7). The base (lowest) address of this group is set by an on-board switch as shown in figure A-5 and table A-1.

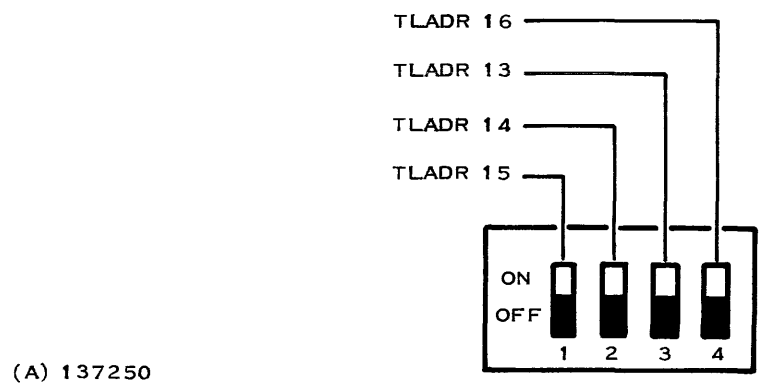


Figure A-5. TILINE Slave Address Switches

Table A-1. TILINE Slave Address Switch Settings and Addresses

TILINE Address (Hex)	CPU Address (Hex)	Switches 1	2	3	4
FFC00	F800	Off	Off	Off	Off
FFC08	F810	Off	Off	Off	On
FFC10	F820	On	Off	Off	Off
FFC18	F830	On	Off	Off	On
FFC20	F840	Off	On	Off	Off
FFC28	F850	Off	On	Off	On
FFC30	F860	On	On	Off	Off
FFC38	F870	On	On	Off	On
FFC40	F880	Off	Off	On	Off
FFC48	F890	Off	Off	On	On
FFC50	F8A0	On	Off	On	Off
FFC58	F8B0	On	Off	On	On
FFC60	F8C0	Off	On	On	Off
FFC68	F8D0	Off	On	On	On
FFC70	F8E0	On	On	On	On
FFC78	F8F0	On	On	On	On

A.4 DISK CONTROLLER JUMPERS.

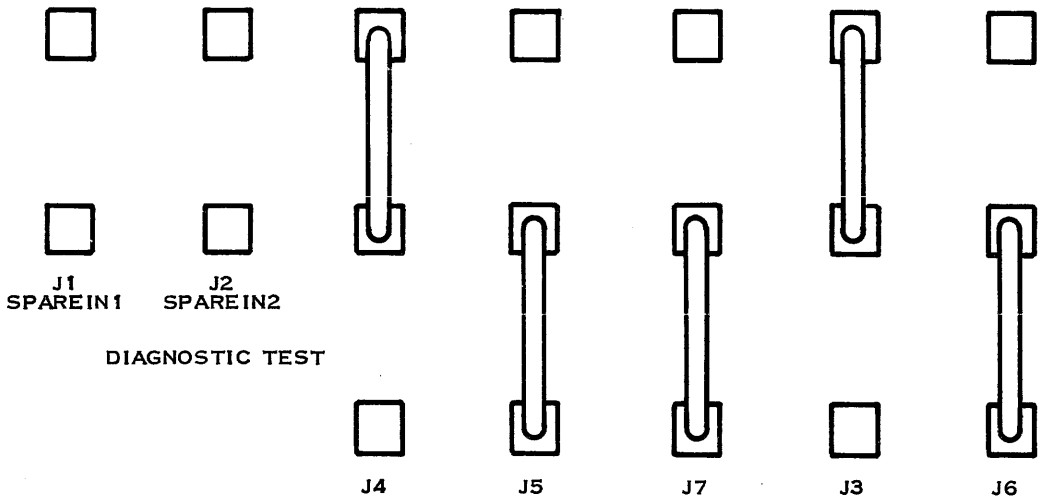
The standard setting of the disk controller on-board jumpers is shown in figure A-6. Note that the drawing does not correspond to the physical jumper locations on the board. Refer to figures 1-2 and 1-3, the board photographs, for assistance in locating the jumpers.

1. Jumper J1 has no current purpose. It grounds the unused SPAREIN1- line if installed (937502, sheet 11 or 2262102).

2. Jumper J2 may be installed during unit test, to force the controller to execute the long-form self-test on power up. It must be removed prior to normal operations. J2 grounds the SPAREIN2- line, if installed (937502, sheet 11 or 2262102). Jumper sensing is part of the controller microprogram.

3. Jumpers J3, J4, J6 and J7 change the read/write data format from double frequency (FM) to a higher density format. The jumpers must be in the positions shown for a 10 megabyte disk system (937502 or 2262102, sheet 19).

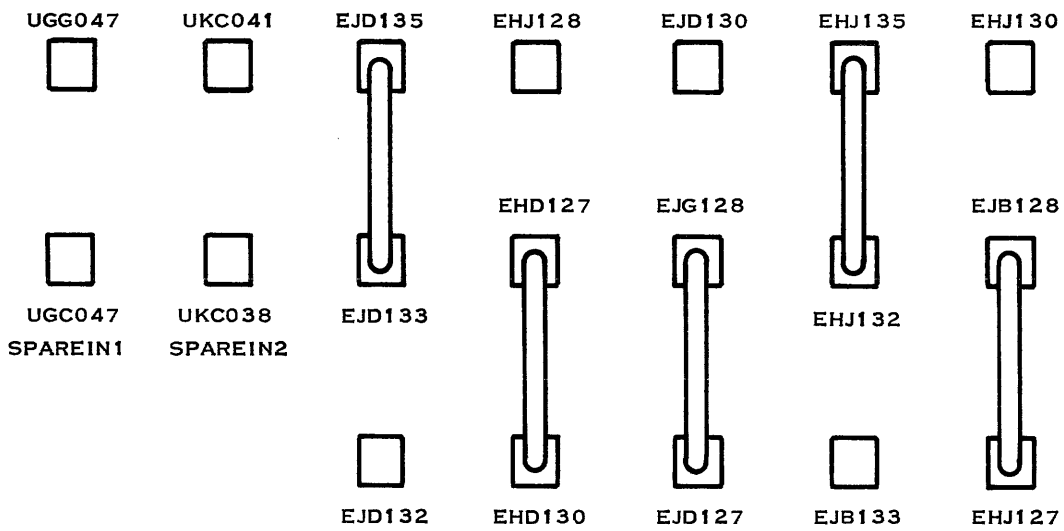
4. Jumper J5 provides the capability to alter the write clock phase by 180 degrees, as a skew compensation measure. No combination of cable lengths and cable capacity currently in use has required that correction capability.



NOTE:

THE LONG SELF-TEST JUMPER MAY BE INSTALLED BETWEEN THE SPAREIN2 LINE (J2) AND GROUND FOR TEST PURPOSES ONLY. IT MUST BE REMOVED TO RESUME NORMAL OPERATIONS.

PWB VERSION



FINE LINE PWB VERSION

(A)143534A

Figure A-6. Disk Controller Standard Jumpers

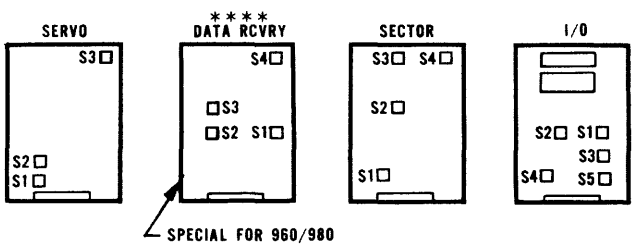
A.5 DISK DRIVE OPTION SWITCH SETTINGS

The disk drive has option switches on five of the logic boards in the electronics card cage. These switches must be set to a specific configuration to allow the disk drive to operate with the DS10 cartridge disk controller. A label on the power supply cover identifies the switch locations and mandatory settings. This label is reproduced in figure A-7.

The I/O board switches are accessible from the rear of a rack-mount drive if the cable adapter board is removed. On a pedestal-mount drive, it will be necessary to remove the sheet-metal dust cover by lifting it straight up. It may also be necessary to remove the cable clamp and to disconnect the flat 3M-type cables. Checking or changing the switch settings on the remaining boards will require removal of the solid electronics cover plate and the card cage clamp and lid. The individual boards must be removed from the cage to gain access to the switches.

SWITCH DESIGNATOR	CONTROL BOARD	SERVO BOARD			DATA **** RCVRY BOARD				SECTOR BOARD				I/O BOARD				
*** SWITCH POSITION	S1	S1	S2	S3	S1	S2	S3	S4	S1	S2	S3	S4	* S1	* S2	S3	S4	S5
1	0	1	0	** 0	0	0	1	0	1	1	0	0	UN1	INT1	0	0	0
2	1	1	0	** 1	1	0	0	0	1	0	0	0	UN2	INT2	1	1	0
3	1	1	0	1	0	1	0	1	0	0	0	0	UN3	INT3	0	** 1	0
4	0	1	0	1	0	** 0	1	1	1	0	1	0	UN4	INT4	0	1	0
5	0	1	0		** 0	** 1	1	0		0	1	0	0	1		0	0
6	0	1	0		** 0	** 0	0	0		0	0	1		0		0	0
7	1	1	0		1	** 1	1	1		1	0	1		1		0	0
8	0	1	0							0	1	0		0		1	0
9		1	0											0			
10		0	1											1			

* S1 AND S2 – UN AND INT SWITCHES MUST HAVE SAME UNIT SELECTED
** SWITCHES ARE REVERSED FOR 960/980 APPLICATIONS
*** 1=ON, 0=OFF
**** CDC PN 75886537 OR 75297105 FOR 990, CDC PN 75881050 FOR 960/980



DS10 SWITCH SETTINGS
THIS UNIT SET FOR 990 ☒ 960/980 ☐

Figure A-7. DS10 Disk Drive Option Switch Settings

APPENDIX B
PWB SIGNAL DICTIONARY

APPENDIX B

PWB SIGNAL DICTIONARY

Signature	937502 Sheet No.	Gate - Pin	Definitions
ACCDATEN	2	C11-10	Access data enable. Partially enables the TLDATEN gate when access logic is in the device access state (ACCESSOK- = 0) and TILINE terminate has not occurred.
ACCESSOK-	2	B11-3	TILINE access okay. During TILINE master cycle, enables TILINE address drivers, TLREAD, TLGO- drivers. For write operations, also partially enables TILINE data line drivers.
ADDACK-	16	Disk Drive	Address acknowledge, from selected disk unit. Acknowledges that the drive has accepted the cylinder address supplied by the controller.
ADDACKQ	16	J5-5	Latched version of address acknowledge (ADDACK), stored in I-bus input latch.
ADDSTB-	13	R2-3	Address strobe. Output which, when low, strobes the cylinder address (ADD001- thru ADD256-) into the selected disk drive.
ADD001-, 2-, 4-, 8-, 16-, 32-, 64-, 128-, 256-	14	R3, R4, R6	Cylinder address, to the selected disk unit. Addresses 0-407 are valid.
BUSYLED-	13	65-6	Open-collector output that lights the BUSY indicator when low. Controlled by BUSYQ-.
BUSYQ-	13	H11-10	Controller busy. Output of microinstruction decoder/register that indicates that the controller is busy performing a command. Lights BUSY indicator and enables busy indication for any TILINE master read operation.
CARRY (0-6)-	12	C7, D7	Carry signals from carry look-ahead units to microprocessors.
CIL-	12	D8-12	Carry input to left byte CPE array.
CLKEN	4	F11-1	Clock enable. Retriggers microprocessor clock cycle or in free-running mode when delay 3 expires.

Signature	937502 Sheet No.	Gate - Pin	Definitions
CLKINH	4	F11-4	Clock inhibit. Disables microprocessor clock generation during a TILINE master cycle.
CLKLED-	4	G5-8	Clock indicator. Open-collector version of CLKOFF that lights an LED indicator each time the clock on latch sets.
CLKOFF	4	M7-6	Clock off. This signal which has the same period as MPCK- is used in the development of microprocessor clock, MPCK-. It is also used as a synchronizing term in clearing interrupt latches. CLKOFF goes low coincident with the leading (falling) edge of MPCK-. CLKOFF remains low for 125 nanoseconds, then goes high for 175 nanoseconds (more if the clock waveform is extended by a TILINE master cycle).
CLKON	4	F8-6	Clock on. Latch output which activates the microprocessor clock generation cycle. The period is the same as the period of MPCK-, and the high level pulse width is 125 nanoseconds.
CLKRUN	4 18	R17-2 G6-11	Clock run. Pulled high except during single-step control by an external tester.
CLKSTP-	8	F11-13	CPE clock stop. Disables CPE left and right byte clocks when commanded by microinstruction bit 0 or when a trap occurs. Does not stop MPCK- clock generator.
CLKSTPMST-	13	M8-15	Clock stop, master cycle. Stops microprocessor clock during a TILINE master cycle to prevent waste of controller states during the data transfer. Decoded from special group 0 of microinstruction (ROM36-39 = 0001).
CLKSTRT-	4	J12-6	Clock start. Set input to clock on latch. Initiates the microprocessor clock generation cycle.
CLKT1-	4	H8-3	Output of delay 1 timer in microprocessor clock circuit. Sets pulse duration of MPCK-.
CLKT1	4	L8-12	Inverted form of CLKT1- used to trigger delay 2 and develop PBUSEN.
CLKT2-	4	H8-6	Output of delay 2 timer in microprocessor clock circuits.
CLKT3-	4	H8-8	Output of delay 3 timer in microprocessor clock circuits. Determines minimum retrigger time for clock circuit.

Signature	937502 Sheet No.	Gate - Pin	Definitions
CLK1RC	4	H7-2	RC term used in development of CLKT1-.
CLK2RC	4	H7-10	RC term used in development of CLKT2-.
CLK3RC	4	H7-8	RC term used in development of CLKT3-.
CLRCNTR-	14	M11-8	Clear shift counter.
CLRSECIDX-	13	N10-12	Clear sector latch and index latch.
CLRWRTQ-	5	F9-2	Clear Write. Latched and synchronized microcode interrupt condition that is generated if a FIFO timing error occurs during a disk write operation. Synchronized version of WRTTIMERR-.
CMDFRECLK-	5	R2-3	Command frequency clock. Approximate 320 Hz output of RC-controlled NE555 timer that is counted down to produce the 200 millisecond command timer delay.
CMDTMRCLK	5	J6-3	Command timer clock. Gated version of 320 Hz CMDFREQCLK-.
CMDTMRCLR	5	J6-8	Command timer clear generated as a result of a general reset or a trigger timer microinstruction.
CMDTMRDLY-	5	J7-7	Command timer delay. The command timer allows a 200 millisecond (approx) time frame for an operation to occur. Generates a microcode interrupt if the timer is allowed to expire.
CMDTMRQ-	5	F9-12	Command timer delay, latched. Latched and resynchronized (to microprocessor clock) version of the command timer delay. Enables command timer interrupt trap, if low.
CNTEQ15	14	P10-15	Count equals 15. Indicates that the disk clock bit counter has reached a count of 15. Used to keep track of 16-bit words as they are shifted through the serial/parallel shift register during disk read and write operations.
CPKONES	7	E11-10	Command CPE K-bus to all ones. Disables K-bus input multiplexers placing all low levels on CPE K-bus inputs. These low levels are interpreted as data ones by the active-low K-bus.
CPK (00-15)-	7	A7, B7, B6, B8	K-bus active low inputs 0-15.

Signature	937502 Sheet No.	Gate - Pin	Definitions
CPLCK-	8	E8-8	CPE left byte clock. Microprocessor clock (MPCK-) input to the left byte CPE array, gated by microinstruction word select field (ROM08, 09), CPE clock stop (ROM00) and the TRAP signal.
CPRCK-	10	E8-6	CPE right byte clock. Microprocessor clock (MPCK-) input to the right byte CPE array gated as described with CPLCK-, above.
CPSHIFT (2, 3, 6-8)-	8, 9, 10, 11	C3, E3, C4, E2, C1, E1	Right shift outputs of CPE devices to shift inputs (LI) of less-significant CPE stages.
CPUID	13	990 chassis	Central processor unit identifier. The input pin floats (and is pulled high) in a 990/9 chassis. The input is grounded (logic zero) for a 990/10 chassis. The distinction between processors is necessary due to minor differences in TILINE timing.
CPXL	12	C7-7	Carry propagation output from CPE left byte carry generator.
CPXLA	12	C9-4	Carry propagation output of CPE left byte carry multiplexer.
CPXR	12	D7-7	Carry propagate output from CPE right byte carry generator.
CPXRA	12	C8-9	Carry propagate output from CPE right byte carry multiplexer.
CPX (0-7)	8, 9, 10, 11	C3, E3, C4 E4, E2, C1 E1, C2	Carry propagate outputs from individual CPE devices to carry generators.
CPY (0-7)	8, 9, 10, 11	C3, E3, C4 E4, E2, C1 E1, C2	Carry propagate outputs from individual CPE devices to carry generators.
CPYL	12	C7-10	Carry propagate output from CPE left byte carry generator.
CPYLA	12	C9-12	Carry propagate output from CPE left byte carry multiplexer.
CPYR	12	D7-10	Carry propagate output from CPE right byte carry generator.
CPYRA	12	C8-12	Carry propagate output from CPE right byte carry multiplexer.

Signature	937502 Sheet No.	Gate - Pin	Definitions
CRCDATIN	19	N6-9	CRC data in. Serial read or write data into CRC generator/checker.
CRCDATOUT	19	M6-12	CRC data out. Serial CRC character out of CRC generator/checker at the end of a write operation (header or data) to disk.
CRCENFLAG	18	L5-14	CRC enable flag. Used to enable data input to (or CRC character out of) the CRC checker/generator.
CRCERR	19	M6-13	CRC error. Indicates that the CRC character calculated on read did not agree with the CRC character recorded at write time.
CRCPREFLAG	18	L5-13	CRC preset flag. An output of the disk write flag register which presets the CRC generator to all ones prior to writing data to the disk.
CRCPRES-	17	M5-7	CRC preset. Preset signal enabled by the sync character detector (read) or CRC preset flag (write). Presets CRC generator/checker to all ones.
DATCLK	19	N8-6 or L8-10 (Jumper Selected)	Disk data write clock input to write data out F/F. In phase with DCLK and DCLOCK unless phase inverting jumper J5 is installed.
DBUSHI	14	P4-9	Disk bus high. Most significant bit out of disk (cylinder) address register. Inverted to supply ADD256-.
DCLK	19	L7-14	Disk clock. Clock signal for disk interface circuits. Supplied by crystal oscillator and divider for write operations, disk for read operations, micro-instructions for self-test operations.
DCLOCK-	19	N9-8	Disk read or write clock.
DCLOCK	19	N8-6	Disk read, write or test clock.
DCLOCK1-	19	L8-10	Inverted form of DCLOCK. Not used unless excessive write skew requires installation of clock phase correcting jumper J5.
DCRCERRQ-	18	N4-6	CRC error, latched.

Signature	937502 Sheet No.	Gate - Pin	Definitions
DIAGFAULTQ-	13	H11-12	Diagnostic fault. Output of microinstruction special group 1 decoder/register which indicates that a fault was detected during controller self-test. Inhibits read, write, lights FAULT indicator.
DIRDATEN-	15	G12-11	Direct data enable. Enables 3-state outputs of direct read register onto the processor bus. Used during record leader verification when FIFO is bypassed.
DISKDATIN	19	P6-5	Disk data in. Serial read data from the read data buffers to the serial input of the serial/parallel shift register.
DISKDATLD	14	N9-6	Disk data load. A strobe issued during disk write operations which loads parallel data into the serial/parallel shift register. Data is shifted out of the register (serially) to the write data encoding circuits.
DISKSEL-	14	R6-4	Disk Select. When low, selects the fixed disk. When high, selects the removable cartridge. SELECTA- and SELECTB- are also required to complete the selection.
DSKBUSLD	12	M10-7	Disk bus load. Loads inverted processor bus outputs PBUS07- through PBUS15- into disk address register. Output of disk address register is cylinder address ADD001-through 256- to disk drive.
DSKCLR-	13	N10-14	Disk clear. Microinstruction-controlled clear to disk interface logic of controller.
DSKDIRECT-	13	F12-10	Disk direct. When low, disables FIFO input, and partially enables direct read register outputs to P-bus.
DSKDIRQ	13	H11-7	Disk direct mode. Microinstruction-controlled mode bit.
DSKOSC	19	P11-3	5MHz output of oscillator used to clock write data to the disk drive.
DSCOSC-	19	L10-8	Disk Oscillator. Gated version of 5MHz disk oscillator output. Used to clock disk interface logic during write operation.
DSKSHIN-	18	P9-8	Disk shift in. Shifts disk read data from the serial/parallel shift register into the FIFO buffer.

Signature	937502 Sheet No.	Gate - Pin	Definitions
DSKSHOUT-	18	18-8	Disk shift out. Unloads data from FIFO output stage during write operations.
DSKSTRQ	14	R11-9	Disk start transfer latch output. Set by a micro-instruction at the beginning of a disk read or write operations.
DSKSTRRST-	13	N10-13	Reset disk start transfer F/F. Clears disk interface logic as the result of a microinstruction command.
DSKSTRCK-	13	N10-11	Disk start transfer clock. This pulse is enabled by a microinstruction and strobed by MPCK- to form the initial event of any disk interface operation.
DSKSTRTR-	14	P12-6	Disk start transfer F/F summary reset. Clears disk I/F logic in case of general reset, interrupt reset, DSKSTRRST-, or DSCLR- micro-instruction-controlled reset.
DSTARTQ	14	R11-5	Disk start. Resynchronized (with disk clock) disk interface start signal.
EG-	13	R2-6	Erase gate to disk drive. Enables straddle erase in disk drive.
ENFLG-	17	M12-11	Enable flag. Enables FIFO flag multiplexer to gate H flag bits (FIFOIN16-19) into the FIFO. The flags accompany write data through the FIFO.
ENSPEC-	13	L10-6	Enable special field decoders. ROM32-39 of the controller microinstruction may be interpreted as an immediate operand to be loaded on the K-bus, or as special purpose fields. If ROM10=0 and there is no trap, the high level of CLKT1 enables ENSPEC-. ENSPEC- enables the TILINE operation decoder and the special function group select decoder.
ERRORSET	17	M2-12	Error set. Input to FIFO timing error F/F which sets it in case of a FIFO rate error.
FAULTLED-	13	G5-4, 10	Two-wire ORed open-collector outputs which light the controller FAULT indicator in case the command timer expires (CMDTMRDLY-) or a fault is detected during self-test (DIAGFAULTQ-). Note that DIAGFAULTQ and FAULTQ are microinstruction fields.

Signature	937502 Sheet No.	Gate - Pin	Definitions
FAULTQ-	13	H11-11	Microinstruction-controlled fault output from special group 1 decoder/register. Lights FAULT indicator via FAULTLED-.
FIFODATEN-	15	G12-3	FIFO output data enable. Enables three-state outputs of FIFO out/zero mix onto processor bus if direct mode is not specified and disk data to P-bus is specified by the appropriate microinstruction fields.
FIFOOUT (00-19)	17	K3, K7, K4, K5	FIFO output data from 16-word first-in/first-out buffer. Bits 16-19 are flag bits.
FIFOSEL	15	G12-6	FIFO select. Gates FIFO data through the FIFO out/zero multiplexer to the processor bus and on to the TILINE line drivers.
FILERDY-	16	Drive	Disk file ready. Output from the disk drive which indicates the drive is ready for operation; i.e., dc power ok, up to speed, heads loaded, no faults detected, terminator installed. Inverted in controller as OFFLINE-.
FLED-	13	L9-3	Fault LED. Lights FAULT indicator in case of microinstruction-specified fault during normal or self-test operations.
GO	2	F12-6	Inverted output of GO gate that is used during TILINE master cycle to supply the TILINE GO line driver.
GOINH	2	B11-8	Go inhibit. Prevents the setting of the GO gate if a TILINE GO or TILINE terminate is active when the master access logic reaches the device access state.
GROUP00-, 01-, 10-, 11-	13	J11	Microinstruction special group 0-2 decoder enabling signals. ROM34, 35 are decoded to enable the special group microinstruction decoders. Requires ENSPEC- low.
HDSEL-	13	R3-10	Head select. Output to the disk drive that selects the upper surface (HDSEL- low) or the lower surface (HDSEL- high) of the selected platter.
IDLE	19	M12-8	Idle. An input to the CRC multiplexers that forces CRCDATIN low when not checking read data or write data.

Signature	937502 Sheet No.	Gate - Pin	Definitions
INDEXMRK-	16	P6-8	Index mark, latched. The index mark is a reference pulse (supplied by the disk drive) which occurs once every disk revolution. The index mark is latched as INDEXMRK-.
INDEXMRKQ-	16	J5-10	Index mark latched for I-bus input and resynchronized to microprocessor clock.
INDMRK-	16	Disk Drive	Index mark. Generated by sensors in the disk drive once per revolution. Identifies the start of sector 0.
INRDY-	16	K2-6	FIFO summary input ready. Indicates FIFO buffer has space available for loading additional input data.
INTA-	5	F10-14	Interrupt A. Group select output of the interrupt address encoder that indicates, when low that at least one active, synchronized microcode interrupt condition is present. Used (in inverted form as INTA) to enable the TRAP- signal and to enable INTB, which disables TRAP- after one clock time.
INTAD (0-2)	5	F10-9, 7, 6	Interrupt address bits 0-2. Outputs of the interrupt address encoder that form part of a trap vector address for the highest priority active (and synchronized) interrupt condition.
INTB	5	F9-15	Interrupt B. Interrupt B goes high one clock time after INTA goes high. INTB (in inverted form as INTB-) disables TRAP- one clock time after INTA. INTB also prevents trap conditions from occurring too close together.
INTRST-	5	J12-11	Interrupt reset. Clears the unsynchronized interrupt latches after the synchronized interrupt trap operation starts. INTRST- = (CLKOFF.INTA)-.
INTTRAP	5	M12-3	Interrupt trap. This signal forces the NRA 06-09 multiplexer outputs to all zeros as part of a microcode interrupt trap operation. INTRAP is essentially an inverted form of TRAP-, but it is not enabled for TILINE slave trap operations.
IORES-	2	A10-4	I/O reset. TILINE I/O reset input to TILINE abort interrupt trap latch.

Signature	937502 Sheet No.	Gate - Pin	Definitions
IRDYA- IRDYD			Input ready. Outputs from individual five bit by 16-word FIFO devices which indicate that the FIFOs are ready to accept additional input data. Summarized as INRDY-.
LFBYT-	10	C12-6	Left byte only. Decoded from word select field (ROM08, ROM09) to disable clock to the right byte and disable the right byte carry multiplexer. See RTBYTE-.
LIR-	12	E7-7	Output of right shift multiplexer which supplies right shift input (LI) of right byte CPE array.
LMXSEL	7	B12-6	Left byte K-bus input multiplexer select. Steers eight-bit immediate operand field of micro-instruction through multiplexer to K-bus inputs.
M12V	19	990 chassis	Negative 12 volt dc power for TMS3129 TESTDATA shift register.
MCUADR (1-9)	6	69, 610, H9	Microcontrol unit address, bits 1-9. Outputs of the SN74S482 address generators which select the 40-bit microinstruction from ROM.
MCUCI (1-3)	6	J9-2, H9-3, G10-3	Microcontrol unit carries. MCUCI1 is generated by the branch decoder ROM and is used for address incrementation. The other carries are between the 'S482 address generators.
MCUS (1-6)	6	J9	Microcontrol unit select code. This code, developed by the branch decoder ROM, determines the operation(s) to be performed by the address generators.
MDAC	3	D12-9	(Master) device access. Output of device access F/F which identifies the device access state of the TILINE master cycle.
MDACCK	3	A11-9	(Master) device access F/F clock. This multiplexer-selected clock pulse clears the device access state at the end of a TILINE master cycle.
MDACRST	3	C11-4	(Master) device access reset (990/9 only). Source for MDACCK selected by the CPU ID multiplexer in a 990/9 chassis.
MDACSET-	3	B11-6	Device access F/F unconditional set. Advances the TILINE master cycle from the device acknowledge state to the device access state.

Signature	937502 Sheet No.	Gate - Pin	Definitions
MDACT	3	G11-5	(Master) device active F/F output. Indicates that the TILINE master access logic is performing a master cycle. Disables microprocessor clock, enables the 20-microsecond timeout delay, latches up the PBUS control register.
MDAK	3	D12-5	(Master) device acknowledge F/F output. This F/F when set indicates that the TILINE master cycle is in the device acknowledge state.
MDAKCK	3	E11-4	Device acknowledge F/F clock. Advances the TILINE master cycle from the device access request state to the device acknowledge state.
MDAKCLR-	3	C10-8	Device acknowledge F/F unconditional reset. Clears the device acknowledge F/F when the TILINE master cycle advances to the device access state.
MDAR	3	C11-13	(Master) device access request. Initiates the 100-nanosecond timer which determines the minimum time that the master cycle spent in the device access request state.
MDAR	3	C12-3	Device access request state. Disables TLAGOUT to lower priority masters during the period between the initiation of the master cycle and the start of the device access state.
MDAREN-	3	C12-11	(Master) device access request enable. Partially enables the MDAR gate if TILINE access granted is available and if the TILINE master cycle has not reached the device acknowledge state.
MDAROK-	3	F7-8	(Master) device access request ok. Output of delay timer that indicates that the access logic has been in the device access request state for the minimum required time.
MDARRC	3	H7-6	RC timing term used in the development of MDAROK-.
MDCMP-	3	B12-8	(Master) device complete. Indicates that the TILINE data transfer operation is complete. Used to restore master access logic to the initial state.

NOTE

The MDCMP- and MDTOL gate configuration resembles a latch, but is not a latch.

Signature	937502 Sheet No.	Gate - Pin	Definitions
MDGO	3	B10-5	(Master) device go. F/F output that initiates TILINE master cycle and remains active throughout the cycle.
MDTM	3	B12-12	(Master) device terminate. Identifies the end of the TILINE data transfer, and is used to reset master access logic to the idle state, on leading and trailing edges.
MDTMEN	3	A11-12	(Master) device terminate enable. An output of the CPU identification multiplexer used in the development of MDTM. Equal to hardwired 1 for 990/9, GO for 990/10.
MDTO-	3	F7-6	(Master) device timeout. Output of 20-microsecond (approximate) timer. The timer is initiated when device active F/F sets. If it expires before master device complete (MDCMP-), indicates a hung TILINE cycle.
MDTOEN-	2	B11-11	(Master) device timeout enable. Initiates 20-microsecond timer at start of TILINE master cycle, if no wait condition exists.
MDTOL	2	E12-7	Master device time-out, latched. Latched version of MDTO-.
MDTOQ-	5	F9-5	Latched and synchronized (with MPCK-) version of MDTO-.
MDTORC	2	B9-15	RC timing term used in the development of MDTO-. MDTO- is enabled when the MDTORC voltage reaches the input threshold of the MDTO- gate.
MPCK	4	L9-11	Microprocessor clock. Active high version of MPCK-.
MPCK-	4	F8-8	Microprocessor clock. Active-low main timing term for controller logic.
MPCKMNT	18	P7-4	Microprocessor clock maintenance. An isolated version of MPCK- which is available to an external tester at the test sockets.
MPCK482-	4	F8-11	Microprocessor clock (MPCK-) signal with fast rise time, dedicated to the SN74S482 address generator clock inputs.

Signature	937502 Sheet No.	Gate - Pin	Definitions
MSBADRINC	13	M8-13	Most significant address register increment. Output of microinstruction special group 0 decoder which increments the four-bit TILINE MSB address register when a TILINE master operation passes a 65K address boundary.
MSBADRLD-	13	M8-14	Most significant address register load. Loads a four-bit address from the processor bus into the TILINE MSB address register.
MSBADR (0-3)	8	H5	Four most significant TILINE address bits. Stored in an external TILINE MSB address register because there are only 16 address bits available from the CPE array at one time.
MSTRD-	13	J11-6	Master read. Output of microinstruction decoder which initiates a TILINE master read cycle.
MSTSTB	3	J12-3	Master cycle strobe. Clock input which triggers the master device go F/F to set and initiate a TILINE master read or master write cycle.
MSTWRT-	13	J11-7	Master write. Output of microinstruction decoder which initiates a TILINE master write cycle.
NOTRDY-	16	R8-2	Not ready to start read/write, Inverted form of RDYSRW- (ready to start read/write) from selected disk unit. NOTRDY- high indicates that the head carriage has reached the specified cylinder and the heads have had time to settle, in addition to the FILERDY- conditions.
NRA (01-09)	5	L9, H10, 510	Next ROM address bits 1-9. Outputs of the NRA multiplexers, which serve as A inputs to the address generators.
OFFLINE-	16	R8-12	Disk offline. Inverted form of FILERDY- from disk drive.
ORDYA, B, C, D	17	K3, K7, K4, K5	FIFO output ready signals from each of the five-bit by 16-word FIFO devices. Indicates that the FIFO has data available at the outputs. Summarized as OUTRDY-.
OUTRDY-	16	K2-8	Summary FIFO output ready.
PARDAT00	17	L3-12	Parallel data, bit 0. Most significant bit, and shift output, of serial/parallel shift register.

Signature	937502 Sheet No.	Gate - Pin	Definitions
PARDAT (00-15)	17	L3, L4, M4, M3	Parallel data outputs of serial/parallel shift register.
PBCPE-	12	E10-14	CPE to processor bus enable. An output of the PBUS source decode which enables the three-state CPE D-bus outputs onto the processor bus.
PBDSKDAT-	12	E10-11	Disk data to processor bus enable. An output of the PBUS source decoder which partially enables the FIFO and disk direct read register three-state outputs onto the P-bus. Selection between these sources is determined by direct/indirect mode F/F.
PBDSKSTA-	123	E10-9	Disk status to processor bus enable. An output of the PBUS source decoder which enables the three-state status line receiver outputs onto the processor bus.
PBTLDAT-	12	E10-12	Processor bus sourced by TILINE data. An output of the PBUS source decoder which enables data from the TILINE line receivers onto the processor bus. Controlled by bus source field (ROM13-15) of microinstruction.
PBUSEN	12	H8-11	Processor bus enable. A delayed version of CLKT1 which drives the PBUSENL latch in the PBUS source control register. PBUSENL follows PBUSEN except during TILINE master cycles.
PBUSENL	12	E9-2	Processor bus enable latched. Disables the processor bus source decoder during the time (immediately after MPCK- rising edge) that microinstruction outputs are unsettled. Signal is latched only if MDACT- goes active; otherwise, follows PBUSEN.
PBUS (00-15)	8-11	Multiple source bus	Processor bus.
PBZERO-	12	E10-15	Processor bus zero. Output of microinstruction bus source decoder that commands the processor bus to all zeros (high logic levels).
PFWP-	3	A11-4	Power failure warning pulse output of CPU selection multiplexer. See TILINE power failure warning pulse, TLPFWP-.

Signature	937502 Sheet No.	Gate - Pin	Definitions
RCLK-	19	Disk Drive	Read clock. One hundred nanosecond (nominal) active low clock pulses read from the selected disk track and separated from data by the clock/data separator in the disk drive.
RD-	19	Disk Drive	Read data. One hundred nanosecond (nominal) active low data pulses read from the selected disk track and separated from clock by the clock/data separator in the disk drive.
RDA-	19	L8-8	Read data into preset input of read 1 F/F.
RDATA-	19	N11-8	Read data output of read 1 F/F.
RDATAQ	19	P3-5	Read data output of read 2 F/F, converted from bit cell to NRZ format. Also used to store data in the test memory during closed-loop self-testing.
RDB	19		Grounded D-input of read 1 F/F.
RDYDIRRST-	13	N10-9	Ready direct reset. Strobed output of micro-instruction special group 0 decoder that resets the ready direct status F/F. Note that the F/F is in an upside down configuration, and RDYDIRRST- is wired to the preset input.
RDYDIRSTAT-	13	N4-9	Ready direct status. F/F which toggles on first FIFO/direct register SHIFTIN pulse after RDYDIRRST-. Indicates that valid data is available in the direct read register.
RDYDIRSTATQ-	16	J5-15	FIFO ready status. Latched and synchronized to microprocessor clock for I-bus input.
RDYSRW-	16	Disk Drive	Ready to start read/write. Active when all file ready conditions are met and head carriage is at specified cylinder and head selection transients have dissipated.
RDYSTATUS-	17	L2-4	FIFO ready status. FIFO ready to accept data (disk write) or supply data (disk read).
RDYSTATUSQ-	16	J5-15	FIFO ready status. Latched and resynchronized to microprocessor clock for CPE I-bus input.
READ-	2	B10-9	Slave read. TILINE slave logic read/write mode F/F output, controlled by TILINE read line receiver.
READQ-	14	L12-8	Disk interface read. Set during disk read operations after synchronization pulse is detected.

Signature	937502 Sheet No.	Gate - Pin	Definitions
READQQ-	16	J5-7	Disk interface read latched and resynchronized to microprocessor clock for CPE I-bus input.
RESTORE-	13	R4-6	Restore to track zero (also called return to zero seek). Output to disk drive which drives carriage to fully extended position and back to the home position, and clears drive fault latches and cylinder address register.
RG-	13	R3-2	Read gate. Enables disk drive read circuits.
ROL-	9	E4-8	Right shift output of left byte CPE array.
ROM (00-07)	6	F5	Controller microinstruction ROM output bits 0-7.
ROM (8-15)	6	F6	Controller microinstruction ROM output bits 8-15.
ROM (16-23)	6	K9	Controller microinstruction ROM output bits 16-23.
ROM (24-31)	6	K10	Controller microinstruction ROM output bits 24-31.
ROM (32-39)	6	K8	Controller microinstruction ROM output bits 32-39.
ROM 13L, 14L, 15L, 20L, 21L, 33L	12	E9	Latched versions of the bus source, bus destination fields and bit 33 of the controller microinstruction. These are latched in a transparent D latch. When the enable signal, (MDACT-) is high, the output follows the input. When MDACT- is low (during TILINE master access cycle) outputs are latched up.
ROR-	11	C2-8	Right shift output of least significant stage of right byte CPE array.
RST	2	L7-7	Reset. General controller interface reset enabled by TILINE I/O reset (TLIORES-) or power reset (TLPRES-).
RTBYT-	8	F7-11	Right byte (only). Decoded from the microinstruction word select field (ROM08,09) for right byte only instructions. Disables CPE left byte clock and left byte carry multiplexer.
RTSHFTRO	12	E7-9	Right shift output of least significant CPE stage from right shift multiplexer. Zero unless right shift (F-group 0, R-group 111) is performed.

Signature	937502 Sheet No.	Gate - Pin	Definitions
SECMRK-	16	Disk Drive	Sector Mark. A rotational position pulse which identifies the start of each sector.
SECTORB01-, 02-04-, 08-, 16-	16	Disk Drive	Sector address. Sampled by the disk controller after the sector mark is sensed.
SECTORMRK-	16	P4-6	Sector mark - latched. The sector mark latch sets on the first sector mark after a microinstruction-controlled clear sector and index (CLRSECIDX-) pulse. Stores sector mark for the I-bus input latch.
SECTORMRKQ-	16	J5-12	Sector Mark. Latched and resynchronized to microprocessor clock. Provides sector mark input to CPE I-bus.
SELECTA-	14	R3-6	Select disk drive A. When low, selects the dual disk drive designated A, usually the first drive. DISKSEL- also required for individual logical unit selection.
SELECTB-	14	R6-2	Select disk drive B. When low, selects the dual disk drive designated B, usually the second drive. DISKSEL- also required for individual logical unit selection.
SHFCMD	12	E11-1	Shift command. Active when CPEs perform a shift operation (F-group 0, R-group III). Disables left and right byte carry multiplexers when active.
SHFTPRE	12	E11-13	Partially decoded term used in development of SHFTPRE- and, consequently, SHFCMD.
SHFTPRE-	12	D11-8	Partially decoded term used in development of SHFCMD.
SHIFT	17	M5-9	Shift command used to clock the FIFO timing F/F. Supplied by SHIFTIN for read operations, SHIFTOUT for write operations.
SHIFTIN	18	P9-12	Shift command to FIFO input circuits. Loads a 20-bit data and flag word into the FIFO.
SHIFTOUT	18	L10-12	Shift command to FIFO output circuits. Unloads a 20-bit data and flag word from the FIFO, so that the next word in line may be shifted to the FIFO output.

Signature	937502 Sheet No.	Gate - Pin	Definitions
SIGNBIT-	7	J6-6	Sign bit. The immediate operand ($\overline{IM}$) field of a microinstruction contains only eight bits. Except for left byte only instructions, the immediate operand is supplied to the right byte CPE K-bus inputs, and SIGNBIT- extends the sign bit to all the left byte K-bus inputs.
SKIC-	16	Disk Drive	Seek incomplete, also called seek error. Disk output which indicates that the head carriage failed to seek to the specified cylinder address.
SLADOK	4	A4-9, A2-9 A3-9	TILINE slave address okay. Sets the slave transfer F/F if the received TILINE slave address equals the local board address as determined by switches and hardwired address bits.
SLBUSY-	4	D10-6	Slave busy. Strobe which returns a hardwired 1 on TILINE bit 0 output if a slave read is attempted on a busy controller.
SLGODLY	4	J8-10	Slave go delay. A protective delay (100 nsec) which assures that the incoming TILINE slave address has stabilized before it is decoded.
SLGORC	4	H7-4	RC term used in development of SLGODLY-.
SLSW (13-16)-	4	B2-3, 2, 1, 4	TILINE slave address switch outputs.
SLTM	4	C12-8	TILINE slave terminate. Output to the TILINE terminate line driver. Indicates that the slave logic has completed the specified operation. If a slave read is directed to a busy controller, an immediate slave terminate is issued, accompanied by a data 1 in the date word bit 0 position.
SLTMA-	4	K12-3	Slave terminate access. Enables a normal slave terminate at the completion of a slave cycle (controlled by SLVTRM- from microinstruction decoder).
SLTMB-	4	D10-8	Slave terminate B. Enables an immediate terminate and busy indication if a slave read is addressed to a busy controller.
SLVA-	4	G11-9	Output of one of the two FIFOs which control TILINE slave operation.
SLVACT	5	J12-8	Slave active. Disables interrupt priority encoder and serves as a slave trap address input.

Signature	937502 Sheet No.	Gate - Pin	Definitions
SLVAD-	4	M11-3	Slave cycle enable. Enables a TILINE slave cycle if the enable slave bit (ROM16) of the microinstruction is set and the slave transfer F/F is set.
SLVB-	4	L12-5	Output of one of the two F/F's which control TILINE slave cycles.
SLVTRM-	13	J11-5	Slave terminate. Output of microinstruction special field decoder, controlled by ROM32, 33. Causes TILINE slave logic to issue a TILINE terminate, ending the slave cycle.
SLXFR	4	M9-5	Slave transfer. Slave transfer F/F sets upon expiration of the 100 nanosecond slave go delay if the incoming TILINE address equals the board slave address.
SPAREIN1-	11	No Connection	Spare input from disk drive to CPE I-bus.
SPAREIN2-	11	Jumper J2 (test only)	Long test check jumper, if installed, grounds SPAREIN2-. This causes the microprogram to execute the long self-test on power-up for test only.
SPAREIN (3-6)-	16	No Connection	Spare inputs from disk drive to disk status word (processor bus) input.
SPAREOUT1-	13	R4-2	Status update strobe. During self-test the controller microprogram maintains a status count which is updated as various test segments are successfully completed. SPAREOUT1- is pulsed each time the status count is updated. Available as a strobe to synchronize logic analyzer or oscilloscope.
SPAREOUT2-	13	R6-10	Spare output.
SPAREOUTQ1-	14	P3-12	Latched spare output. A spare output of the disk select register.
STBCLR-	13	N10-7	Allows a deliberate clearing of the disk control functions in the special function 2 decoder/register.
STBRST-	13	P12-8	Strobe reset. Clears the special function 2 decoder/register in the event of a general reset (RST-), an interrupt reset (INTRST-), or a strobe clear from special function 0 (STBCLR-).

Signature	937502 Sheet No.	Gate - Pin	Definitions
STOPFLAG	18	L5-12	Write data (to disk) transfer stop flag. This flag accompanies the last TILINE-to-FIFO word through the FIFO. When it reaches the FIFO output, the transfer to disk should be stopped.
STRTREAD-	14	R10-6	Interface read logic clear.
SWAIN-	16	Adapter Board	Switch fixed/removable unit numbers on drive A, if low. Controlled by jumper J1-J3 of adapter board mounted on drive A. Normal designation (SWAIN- high) is: unit 0 - fixed disk unit 1 - removable disk cartridge.
SWBIN-	16	Adapter Board	Switch fixed/removable unit numbers on drive B, if low. Controlled by jumper J1-J4 of adapter board mounted on drive B. Normal designation (SWBIN- high) is: unit 2 - fixed disk unit 3 - removable disk cartridge.
SYNCQ-	14	N12-10	Synchronization character detected and latched. Enables read operations after the 6E synchronization character is detected.
SYNC6E	14	N2-8	Synchronization character present. Goes low for one disk clock time when the 6E synchonization character is detected.
TESTBIT-	12	D8-9	Input to test bit flip-flop from word look-ahead carry generator.
TESTBITQ	12	M9-8	Output of test bit F/F which steers execution of all conditional branch and conditional return microinstructions.
TESTCLK-	13	H11-5	Test clock. Microinstruction-controlled clock pulse which replaces disk read or write clock as the disk I/F timing source during controller self-test. Burst frequency is approximately 833.3 KHz.
TESTDATA	19	L11-3	Test data output of TMS 3129 serial shift register memory used for controller closed-loop self-tests.
TESTMODEQ	13	H11-4	Test mode output of microinstruction special group 1 decoder/register. Sets up data paths for controller closed-loop self-test.

Signature	937502 Sheet No.	Gate - Pin	Definitions
TESTOUTIN	19	L11-6	The TMS 3129 serial test memory consists of 2 sections, each with a 1-by-132 capacity. TESTOUTIN connects the output of one section to the input of the other, for a 1-by-264 net capacity.
TESTRDDAT-	19	M11-6	Test read data. Test data out of the serial test memory to the read data logic, as gated by TESTMODEQ. Self-test only.
TIMERRQ	14	N12-6	FIFO timing error - latched. Detects FIFO errors during read and write operations such as attempting to load a full FIFO or attempting to retrieve data from a FIFO without any data in it.
TLABORT-	2	C10-6	TILINE abort. Input to TILINE abort latch which sets the latch if a power failure warning (TLPFWP-) or a general I/O reset (IORES-) signal is received.
TLABORTL	2	E12-9	TILINE abort latch. Sets if controller operations are to be aborted by the power failure warning pulse (TLPFWP-), the power reset (TLPRES-) or a general I/O reset (TLIORES-).
TLABORTQ-	5	F9-10	Latched and synchronized (with MPCK-) version of TLABORTL. This microcode interrupt signal generated if a power failure warning, power reset, or I/O reset is issued to all the controllers in the 990 chassis.
TLADR (00-19)	8, 9, 10, 11	A5, CPE devices, TILINE	TILINE address. A 20-bit address which accompanies any word transferred on the TILINE.
TLAGIN	3	P2-6	TILINE access granted input from higher priority masters. TLAGIN must be high for the TILINE master cycle to initiate the 100 nanosecond device access request minimum timer.
TLAGOUT	3	C10-3	TILINE access granted output to lower priority masters. TLAGOUT is disabled during the device access request and device acknowledge states of the TILINE master cycle.
TLAK-	2	P1-71	TILINE acknowledge. As an input, must be inactive (high) for the TILINE master cycle to advance to the device acknowledge state. As an output, is asserted during the device acknowledge state.

Signature	937502 Sheet No.	Gate - Pin	Definitions
TLAV	2	P1-58	TILINE available. As an input, must be active for the TILINE master cycle to advance to the device access state. Disabled by the controller in device access sate.
TLDATA (00-15)-	8, 9, 10, 11	A6, B4, B3, B5. TILINE	TILINE data.
TLDATEN-	2	H12-6	TILINE data enable. Enables TILINE data line drivers during a master write or slave read cycle.
TLERR-	2	D11-6	TILINE error. Sets the TILINE error latch if a parity error (TLMER) is returned by TILINE memory during a master read cycle.
TLERRL-	2	E12-13	TILINE error latch output. See TLERR-.
TLERRQ-	5	F9-7	Latched and synchronized version of TLERRL-, used in interrupt trap circuits. Initiates a microcode interrupt trap if a memory parity error is detected while the controller is reading data from 990 memory for transmission to the disk.
TLGO-	2	P1-25	TILINE go. Control strobe asserted by a TILINE master throughout a data transfer. Used by slaves to enable slave address decoding, initiate slave response.
TLINT-	13	G5-2	TILINE interrupt. Disk controller interrupt to the 990 CPU. Enabled by a special group 1 microinstruction.
TLINTLED	13	G5-12	TILINE interrupt indicator. Light-emitting diode indicator that lights when the controller sends an interrupt (TLINT-) to the 990 CPU.
TLINTQ-	13	H11-9	TILINE interrupt. Output of microinstruction special group 1 decoder/register which enables an interrupt (TLINT-) to the 990 CPU.
TLIORES-	2	P1-14	TILINE I/O reset. Master clear signal from 990 CPU to all I/O controllers.
TLMER	2	P1-55	TILINE memory error. Asserted by TILINE memory if a parity error is detected as part of a memory read operation.

Signature	937502 Sheet No.	Gate - Pin	Definitions
TLPFWP-	3	P1-16	(TILINE) Power failure warning pulse. Advance notice from the 990 power supply that a power failure is imminent. Precedes power reset.
TLPRES-	2	P1-13	(TILINE) Power failure reset. Reset signal from 990 power supply that assures that I/O logic is cleared, and that it restarts in an orderly manner.
TLREAD-	2	P1-11	TILINE read. Identifies read/write TILINE operations.
TLSHIN-	18	D10-11	TILINE shift in. Generated during write data or write data unformattted operations to shift data from the TILINE line receivers into the FIFO.
TLSHOUT-	18	G12-8	TILINE shift out. Generated during read data or read data unformatted operations. Shifts a new word to the FIFO output after a word is transmitted to 990 memory via a master write cycle.
TLTM-	2	P1-20	TILINE terminate. Asserted by TILINE slave when read data is available or write data has been accepted.
TLWAIT-	2	P1-63	TILINE wait. Asserted only by TILINE bus couplers.
TRAP-	5	H12-8	Trap signal that steers the next ROM address multiplexers to gate a trap vector address to the address generators. Generated while servicing a TILINE slave trap, microcode interrupt trap, power or I/O reset trap.
TRIGTMR-	13	N10-10	Trigger command timer. Output of micro-instruction special group 0 decoder that retriggers command timer, preventing expiration of the 200 millisecond delay.
UNITA	14	P3-5	Select unit A. Disk select output which when high specifies the dual disk drive designated A (the first drive). Requires DISKSEL for complete selection of a logical unit.
UNITB	14	P3-2	Select unit B. Disk select output which specifies dual disk drive B. Requires DISKSEL for complete logical unit selection.
UNITLOAD-	12	M10-5	Unit load. Loads the disk selection signals from the processor bus into the disk select register.

Signature	937502 Sheet No.	Gate - Pin	Definitions
UTCSHIN-	12	M10-6	UTC shift in. Loads a word from the CPE outputs into the FIFO, such as when writing headers during a write format operations.
UTCSHOUT-	18	G12-8	UTC shift out. Unloads a word from the FIFO output when the CPE has accepted the word, such as during self-tests.
WCHK-	16	Disk Drive	Write check, also called fault. Indicates that the disk drive electronics has detected a fault condition and inhibited write and erase currents.
WCLK	19	M11-11	Write clock. A 5MHz square wave (200 nano-second pulse width) clock used to encode write data and clock.
WCLKAQQ-	19	N7-8	Write clock divider output. The 2.5 MHz output of clock divider. Serves as the source for DCLK (disk clock) during write operations. Also used in write data and clock encoding.
WDNCLK-	19	R2-8	Write data and clock. Double-frequency (FM) bit cell encoded data and clock to disk drive.
WDNCLKEN	19	N8-11	Write data and clock enable. A signal used in write data and clock encoding. Always high at clock time, high at data 1 time, low (to inhibit output pulse) at data 0 time.
WG-	13	R2-11	Write gate, to disk drive, enables write current.
WOSCSTOP-	19	TP1	Write oscillator stop, external test input.
WOSTST-	19	TP2	Write oscillator stop-external test input.
WP-	16	Disk Drive	Write protect. Indicates that data may not be written to the selected logical unit because the disk drive WRITE PROTECT switch for that fixed or removable disk is ON.
WRITEQ	14	N11-5	Write, latched. Output of write F/F in disk I/F start and read/write control logic.
WRITEQD	14	L9-8	Input to write F/F in disk I/F start and read/write control logic. Enabled when micro-instruction specifies a write operation (DSKWRTQ = 1) and the disk start F/F (DSTARTQ) sets.

Signature	937502 Sheet No.	Gate - Pin	Definitions
WRTDATD	19	N6-7	Serial output of write data/CRC multiplexer to write data and clock encoding circuits.
WRTDATOUT-	19	N7-6	Serial write data out, in NRZ form to write data and clock encoders. Also, self-test write data to serial test memory via read 2 (RDATAQ) F/F.
WRITTIMERR-	5	N8-3	Write timing error. Generated if a FIFO timing error is detected during a write to the disk. This signal is synchronized (as CLRWRTQ-) to initiate a microcode interrupt trap routine.
ZERODATEN-	15	C10-11	Zeros or data enable. Enables three-state outputs of FIFO data out/zero multiplexer onto processor bus.

APPENDIX C

FINE LINE SIGNAL DICTIONARY

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FINE LINE SIGNAL DICTIONARY

Signature	2262102 Sheet No.	Gate - Pin	Definitions
ACCDATEN	2	UCE072-1	Access data enable. Partially enables the TLDATEN gate when access logic is in the device access state (ACCESSOK- = 0) and TILINE terminate has not occurred.
ACCESSOK-	2	UBK094-6	TILINE access okay. During TILINE master cycle, enables TILINE address drivers, TLREAD, TLGO- drivers. For write operations, also partially enables TILINE data line drivers.
ADDACK-	16	UJJ039-9	Address acknowledge, from selected disk unit. Acknowledges that the drive has accepted the cylinder address supplied by the controller.
ADDACKQ	16	UFK039-5	Latched version of address acknowledge (ADDACK), stored in I-bus input latch.
ADDSTB-	13	UJD050-11	Address strobe. Output which, when low, strobes the cylinder address (ADD001- thru ADD256-) into the selected disk drive.
ADD001-, 2-, 4-, 8-, 16-, 32-, 64-, 128-, 256-	14	UJJ017, UJJ028, UJJ061	Cylinder address, to the selected disk unit. Addresses 0-407 are valid.
BUSYLED-	13	UBE072-10	Open-collector output that lights the BUSY indicator when low. Controlled by BUSYQ-.
BUSYQ-	13	UFK050-10	Controller busy. Output of microinstruction decoder/register that indicates that the controller is busy performing a command. Lights BUSY indicator and enables busy indication for any TILINE master read operation.
CARRY(0-6)-	12	UAK006, UAK050	Carry signals from carry look-ahead units to microprocessors.
CIL-	12	UAK072-12	Carry input to left byte CPE array.
CLKEN	4	UCE072-10	Clock enable. Retriggers microprocessor clock cycle or in free-running mode when delay 3 expires.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
CLKINH	4	UCE072-4	Clock inhibit. Disables microprocessor clock generation during a TILINE master cycle.
CLKLED-	4	UBE072-6	Clock indicator. Open-collector version of CLKOFF that lights an LED indicator each time the clock on latch sets.
CLKOFF	4	UAK094-12	Clock off. This signal which has the same period as MPCK- is used in the development of microprocessor clock, MPCK-. It is also used as a synchronizing term in clearing interrupt latches. CLKOFF goes low coincident with the leading (falling) edge of MPCK-. CLKOFF remains low for 125 nanoseconds, then goes high for 175 nanoseconds (more if the clock waveform is extended by a TILINE master cycle).
CLKON	4	UDE083-6	Clock on. Latch output which activates the microprocessor clock generation cycle. The period is the same as the period of MPCK-, and the high level pulse width is 125 nanoseconds.
CLKRUN	4 18	UEE105-3 XDK006-11	Clock run. Pulled high except during single-step control by an external tester.
CLKSTP-	8	UDE028-10	CPE clock stop. Disables CPE left and right byte clocks when commanded by microinstruction bit 0 or when a trap occurs. Does not stop MPCK- clock generator.
CLKSTPMST-	13	UHD050-15	Clock stop, master cycle. Stops microprocessor clock during a TILINE master cycle to prevent waste of controller states during the data transfer. Decoded from special group 0 of microinstruction (ROM36-39 = 0001).
CLKSTRT-	4	UCE083-11	Clock start. Set input to clock on latch. Initiates the microprocessor clock generation cycle.
CLKT1-	4	UDK105-3	Output of delay 1 timer in microprocessor clock circuit. Sets pulse duration of MPCK-. On fine line board, drives PBUSENL latch in the PBUS source control register. PBUSENL follows CLKT1- except during TILINE master cycles.
CLKT1	4	UDK094-8	Inverted form of CLKT1- used to trigger delay 2 and develop PBUSEN.
CLKT2-	4	UDK105-11	Output of delay 2 timer in microprocessor clock circuits.
CLKT3-	4	UCE083-3	Output of delay 3 timer in microprocessor clock circuits. Determines minimum retrigger time for clock circuit.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
CLK1RC	4	UEE105-2	RC term used in development of CLKT1-.
CLK2RC	4	UEE105-12	RC term used in development of CLKT2-.
CLK3RC	4	UBE072-8	RC term used in development of CLKT3-.
CLRCNTR-	14	UFK105-8	Clear shift counter.
CLRSECIDX-	13	UJJ072-12	Clear sector latch and index latch.
CLRWRTQ-	5	UEE094-2	Clear Write. Latched and synchronized microcode interrupt condition that is generated if a FIFO timing error occurs during a disk write operation. Synchronized version of WRTTIMERR-.
CMDFRECLK-	5	UDK115-3	Command frequency clock. Approximate 320 Hz output of RC-controlled NE555 timer that is counted down to produce the 200 millisecond command timer delay.
CMDTMRCLK	5	UDK105-6	Command timer clock. Gated version of 320 Hz CMDFREQCLK-.
CMDTMRCLR	5	UJD105-11	Command timer clear generated as a result of a general reset or a trigger timer microinstruction.
CMDTMRDLY-	5	UFE105-7	Command timer delay. The command timer allows a 200 millisecond (approx) time frame for an operation to occur. Generates a microcode interrupt if the timer is allowed to expire.
CMDTMRQ-	5	UEE094-12	Command timer delay, latched. Latched and resynchronized (to microprocessor clock) version of the command timer delay. Enables command timer interrupt trap, if low.
CNTEQ15	14	UFE116-15	Count equals 15. Indicates that the disk clock bit counter has reached a count of 15. Used to keep track of 16-bit words as they are shifted through the serial/parallel shift register during disk read and write operations.
CPKONES	7	UDE028-13	Command CPE K-bus to all ones. Disables K-bus input multiplexers placing all low levels on CPE K-bus inputs. These low levels are interpreted as data ones by the active-low K-bus.
CPK (00-15)-	7	UAK017, UDE017, UDE039, UAK039	K-bus active low inputs 0-15.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
CPLCK-	8	UDE061-8	CPE left byte clock. Microprocessor clock (MPCK-) input to the left byte CPE array, gated by microinstruction word select field (ROM08, 09), CPE clock stop (ROM00) and the TRAP signal.
CPRCK-	10	UBK083-8	CPE right byte clock. Microprocessor clock (MPCK-) input to the right byte CPE array gated as described with CPLCK-, above.
CPSHIFT (L,3,9,6-8)	8, 9, 10, 11	UBE036, UCC036, UCC051, UBE051, UCC006, UBE021, UCC021, UBE006	Right shift outputs of CPE devices to shift inputs (LI) of less-significant CPE stages.
CPUID	13	990 chassis (UAK105-1)	Central processor unit identifier. The input pin floats (and is pulled high) in a 990/9 chassis. The input is grounded (logic zero) for a 990/10 chassis. The distinction between processors is necessary due to minor differences in TILINE timing.
CPXL	12	UAK050-7	Carry propagation output from CPE left byte carry generator.
CPXLA	12	UAK061-4	Carry propagation output of CPE left byte carry multiplexer.
CPXR	12	UAK006-7	Carry propagate output from CPE right byte carry generator.
CPXRA	12	UAE072-9	Carry propagate output from CPE right byte carry multiplexer.
CPX (0-7)	8, 9, 10, 11	UBE036, UCC036, UCC051, UBE051, UBE021, UCC006, UBE006, UCC021	Carry propagate outputs from individual CPE devices to carry generators.
CPY (0-7)	8, 9, 10, 11	UBE036, UCC036, UCC051, UBE051, UBE021, UCC006, UBE006, UCC021	Carry propagate outputs from individual CPE devices to carry generators.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
CPYL	12	UAK050-10	Carry propagate output from CPE left byte carry generator.
CPYLA	12	UAK061-12	Carry propagate output from CPE left byte carry multiplexer.
CPYR	12	UAK006-10	Carry propagate output from CPE right byte carry generator.
CPYRA	12	UAE072-12	Carry propagate output from CPE right byte carry multiplexer.
CRCDATIN	19	UHD105-9	CRC data in. Serial read or write data into CRC generator/checker.
CRCDATOUT	19	UGE105-12	CRC data out. Serial CRC character out of CRC generator/checker at the end of a write operation (header or data) to disk.
CRCENFLAG	18	UHJ028-14	CRC enable flag. Used to enable data input to (or CRC character out of) the CRC checker/generator.
CRCERR	19	UGE105-13	CRC error. Indicates that the CRC character calculated on read did not agree with the CRC character recorded at write time.
CRCPREFLAG	18	UHJ028-13	CRC preset flag. An output of the disk write flag register which presets the CRC generator to all ones prior to writing data to the disk.
CRCPRES-	17	UGE050-7	CRC preset. Preset signal enabled by the sync character detector (read) or CRC preset flag (write). Presets CRC generator/checker to all ones.
DATCLK	19	UJD105-6 or UHJ105-8 (Jumper Selected)	Disk data write clock input to write data out F/F. In phase with DCLK and DCLOCK unless phase inverting jumper J5 is installed.
DBUSHI	14	UJD017-9	Disk bus high. Most significant bit out of disk (cylinder) address register. Inverted to supply ADD256-.
DCLK	19	UFK116-14	Disk clock. Clock signal for disk interface circuits. Supplied by crystal oscillator and divider for write operations, disk for read operations, micro-instructions for self-test operations.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
DCLOCK-	19	UJD094-8	Disk read or write clock.
DCLOCK	19	UJD105-6	Disk read, write or test clock.
DCLK1-	19	UFK116-9	Inverted form of DCLOCK. Not used unless excessive write skew requires installation of clock phase correcting jumper J5.
DCRCERRQ-	18	UFK028-8	CRC error, latched.
DIAGFAULTQ-	13	UFK050-12	Diagnostic fault. Output of microinstruction special group 1 decoder/register which indicates that a fault was detected during controller self-test. Inhibits read, write, lights FAULT indicator.
DIRDATEN-	15	UFE050-11	Direct data enable. Enables 3-state outputs of direct read register onto the processor bus. Used during record leader verification when FIFO is bypassed.
DISKDATIN	19	UHD094-9	Disk data in. Serial read data from the read data buffers to the serial input of the serial/parallel shift register.
DISKDATLD-	14	UJD094-6	Disk data load. A strobe issued during disk write operations which loads parallel data into the serial/parallel shift register. Data is shifted out of the register (serially) to the write data encoding circuits.
DISKSEL-	14	UJJ061-12	Disk Select. When low, selects the fixed disk. When high, selects the removable cartridge. SELECTA- and SELECTB- are also required to complete the selection.
DSKBUSLD	12	UFE028-9	Disk bus load. Loads inverted processor bus outputs PBUS07- through PBUS15- into disk address register. Output of disk address register is cylinder address ADD001- through 256- to disk drive.
DSKCLR-	13	UJJ072-14	Disk clear. Microinstruction-controlled clear to disk interface logic of controller.
DSKDIRECT-	13	UGE039-4	Disk direct. When low, disables FIFO input, and partially enables direct read register outputs to P-bus.
DSKDIRQ	13	UFK050-7	Disk direct mode. Microinstruction-controlled mode bit.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
DSKOSC	19	UJJ128-8	5MHz output of oscillator used to clock write data to the disk drive.
DSCOSC-	19	UHJ116-12	Disk Oscillator. Gated version of 5MHz disk oscillator output. Used to clock disk interface logic during write operation.
DSKSHIN-	18	UHJ116-6	Disk shift in. Shifts disk read data from the serial/parallel shift register into the FIFO buffer.
DSKSHOUT-	18	UFK105-11	Disk shift out. Unloads data from FIFO output stage during write operations.
DSKSTRQ	14	UJJ116-9	Disk start transfer latch output. Set by a micro-instruction at the beginning of a disk read or write operations.
DSKSTRRST-	13	UJJ072-13	Reset disk start transfer F/F. Clears disk interface logic as the result of a microinstruction command.
DSKSTRTCK-	13	UJJ072-11	Disk start transfer clock. This pulse is enabled by a microinstruction and strobed by MPCK- to form the initial event of any disk interface operation.
DSKSTRTR-	14	UJJ105-8	Disk start transfer F/F summary reset. Clears disk I/F logic in case of general reset, interrupt reset, DSKSTRRST-, or DSCLR- micro-instruction-controlled reset.
DSTARTQ	14	UHJ094-5	Disk start. Resynchronized (with disk clock) disk interface start signal.
EG-	13	UJD050-3	Erase gate to disk drive. Enables straddle erase in disk drive.
ENFLG-	17	UFE006-11	Enable flag. Enables FIFO flag multiplexer to gate H flag bits (FIFOIN16-19) into the FIFO. The flags accompany write data through the FIFO.
ENSPEC-	13	UEE083-12	Enable special field decoders. ROM32-39 of the controller microinstruction may be interpreted as an immediate operand to be loaded on the K-bus, or as special purpose fields. If ROM10=0 and there is no trap, the high level of CLKT1 enables ENSPEC-. ENSPEC- enables the TILINE operation decoder and the special function group select decoder.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
ERRORSET	17	UGE072-12	Error set. Input to FIFO timing error F/F which sets it in case of a FIFO rate error.
FAULTLED-	13	UEE105-8,10	Two-wire ORed open-collector outputs which light the controller FAULT indicator in case the command timer expires (CMDTMRDLY-) or a fault is detected during self-test (DIAGFAULTQ-). Note that DIAGFAULTQ and FAULTQ are microinstruction fields.
FAULTQ-	13	UFK050-11	Microinstruction-controlled fault output from special group 1 decoder/register. Lights FAULT indicator via FAULTLED-.
FIFODATEN-	15	UFE050-3	FIFO output data enable. Enables three-state outputs of FIFO out/zero mix onto processor bus if direct mode is not specified and disk data to P-bus is specified by the appropriate micro-instruction fields.
FIFOOUT (00-19)	17	UFE072, UGE061, UHD072, UHD028	FIFO output data from 16-word first-in/first-out buffer. Bits 16-19 are flag bits.
FIFOSEL	15	UFE050-6	FIFO select. Gates FIFO data through the FIFO out/zero multiplexer to the processor bus and on to the TILINE line drivers.
FILERDY-	16	Drive (UJD006-9)	Disk file ready. Output from the disk drive which indicates the drive is ready for operation; i.e., dc power ok, up to speed, heads loaded, no faults detected, terminator installed. Inverted in controller as OFFLINE-.
FLED-	13	UFK094-6	Fault LED. Lights FAULT indicator in case of microinstruction-specified fault during normal or self-test operations.
GO	2	UDK094-6	Inverted output of GO gate that is used during TILINE master cycle to supply the TILINE GO line driver.
GOINH	2	UBK094-8	Go inhibit. Prevents the setting of the GO gate if a TILINE GO or TILINE terminate is active when the master access logic reaches the device access state.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
GROUP00-, 01-, 10-, 11-	13	UEE050	Microinstruction special group 0-2 decoder enabling signals. ROM34, 35 are decoded to enable the special group microinstruction decoders. Requires ENSPEC- low.
HDSEL-	13	UJJ028-6	Head select. Output to the disk drive that selects the upper surface (HDSEL- low) or the lower surface (HDSEL- high) of the selected platter.
IDLE	19	UFK094-8	Idle. An input to the CRC multiplexers that forces CRCDATIN low when not checking read data or write data.
INDEXMRK-	16	UHJ039-6	Index mark, latched. The index mark is a reference pulse (supplied by the disk drive) which occurs once every disk revolution. The index mark is latched as INDEXMRK-.
INDEXMRKQ-	16	UFK039-10	Index mark latched for I-bus input and re-synchronized to microprocessor clock.
INDMRK-	16	Disk Drive (UJJ039-4)	Index mark. Generated by sensors in the disk drive once per revolution. Identifies the start of sector 0.
INRDY-	16	UFE061-6	FIFO summary input ready. Indicates FIFO buffer has space available for loading additional input data.
INTA-	5	UFE094-14	Interrupt A. Group select output of the interrupt address encoder that indicates, when low that at least one active, synchronized microcode interrupt condition is present. Used (in inverted form as INTA) to enable the TRAP- signal and to enable INTB, which disables TRAP- after one clock time.
INTAD(0-2)	5	UFE094-6, 7, 9	Interrupt address bits 0-2. Outputs of the interrupt address encoder that form part of a trap vector address for the highest priority active (and synchronized) interrupt condition.
INTB	5	UEE094-15	Interrupt B. Interrupt B goes high one clock time after INTA goes high. INTB (in inverted form as INTB-) disables TRAP- one clock time after INTA. INTB also prevents trap conditions from occurring too close together.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
INTRST-	5	UCE083-8	Interrupt reset. Clears the unsynchronized interrupt latches after the synchronized interrupt trap operation starts. INTRST- = (CLKOFF.INTA)-.
INTTRAP	5	UFE006-6	Interrupt trap. This signal forces the NRA 06-09 multiplexer outputs to all zeros as part of a microcode interrupt trap operation. INTRAP is essentially an inverted form of TRAP-, but it is not enabled for TILINE slave trap operations.
IORES-	2	UAK094-8	I/O reset. TILINE I/O reset input to TILINE abort interrupt trap latch.
IRDYA- IRDYD	17	UFE072-2, UGE061-2, UHD072-2, UHD028-2	Input ready. Outputs from individual five bit by 16-word FIFO devices which indicate that the FIFOs are ready to accept additional input data. Summarized as INRDY-.
LFBYT-	10	UCE083-6	Left byte only. Decoded from word select field (ROM08, ROM09) to disable clock to the right byte and disable the right byte carry multiplexer. See RTBYT-.
LIR-	12	UDE050-7	Output of right shift multiplexer which supplies right shift input (LI) of right byte CPE array.
LMXSEL	7	UBE094-12	Left byte K-bus input multiplexer select. Steers eight-bit immediate operand field of microinstruction through multiplexer to K-bus inputs.
M12V	19	990 chassis (P1-41)	Negative 12 volt dc power for TMS3129 TESTDATA shift register (UFK127-4).
MCUADR (1-9)	6	UHJ006, UHD006, UGE006	Microcontrol unit address, bits 1-9. Outputs of the SN74S482 address generators which select the 40-bit microinstruction from ROM.
MCUCI (1-3)	6	UFK006, UGE006, UHD006	Microcontrol unit carries. MCUCI1 is generated by the branch decoder ROM and is used for address incrementation. The other carries are between the 'S482 address generators.
MCUS (1-6)	6	UFK006	Microcontrol unit select code. This code, developed by the branch decoder ROM, determines the operation(s) to be performed by the address generators.
MDAC	3	UCE105-9	(Master) device access. Output of device access F/F which identifies the device access state of the TILINE master cycle.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
MDACCK	3	UAK105-9	(Master) device access F/F clock. This multiplexer-selected clock pulse clears the device access state at the end of a TILINE master cycle.
MDACRST	3	UBK105-1	(Master) device access reset (990/9 only). Source for MDACCK selected by the CPU ID multiplexer in a 990/9 chassis.
MDACSET-	3	UBK116-11	Device access F/F unconditional set. Advances the TILINE master cycle from the device acknowledge state to the device access state.
MDACT	3	UDE105-9	(Master) device active F/F output. Indicates that the TILINE master access logic is performing a master cycle. Disables microprocessor clock, enables the 20-microsecond timeout delay, latches up the PBUS control register.
MDAK	3	UCE105-5	(Master) device acknowledge F/F output. This F/F when set indicates that the TILINE master cycle is in the device acknowledge state.
MDAKCK	3	UBK105-10	Device acknowledge F/F clock. Advances the TILINE master cycle from the device access request state to the device acknowledge state.
MDAKCLR-	3	UCE094-6	Device acknowledge F/F unconditional reset. Clears the device acknowledge F/F when the TILINE master cycle advances to the device access state.
MDAR	3	UBK105-13	(Master) device access request. Initiates the 100-nanosecond timer which determines the minimum time that the master cycle spent in the device access request state.
MDAR-	3	UBE105-11	Device access request state. Disables TLAGOUT to lower priority masters during the period between the initiation of the master cycle and the start of the device access state.
MDAREN-	3	UBE105-6	(Master) device access request enable. Partially enables the MDAR gate if TILINE access granted is available and if the TILINE master cycle has not reached the device acknowledge state.
MDAROK-	3	UDK105-8	(Master) device access request okay. Output of delay timer that indicates that the access logic has been in the device access request state for the minimum required time.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
MDARRC	3	UEE105-6	RC timing term used in the development of MDAROK-.
MDCMP-	3	UBE094-8	(Master) device complete. Indicates that the TILINE data transfer operation is complete. Used to restore master access logic to the initial state. **NOTE** The MDCMP- and MDTO- gate configuration resembles a latch, but is not a latch.
MDGO	3	UDE105-5	(Master) device go. F/F output that initiates TILINE master cycle and remains active throughout the cycle.
MDTM	3	UBE094-6	(Master) device terminate. Identifies the end of the TILINE data transfer, and is used to reset master access logic to the idle state, on leading and trailing edges.
MDTMEN	3	UAK105-12	(Master) device terminate enable. An output of the CPU identification multiplexer used in the development of MDTM. Equal to hardwired 1 for 990/9, GO for 990/10.
MDTO-	3	UBE105-8	(Master) device timeout. Output of 20-microsecond (approximate) timer. The timer is initiated when device active F/F sets. If it expires before master device complete (MDCMP-), indicates a hung TILINE cycle.
MDTOL-	2	UDE094-13	Master device time-out, latched. Latched version of MDTO-.
MDTOQ-	5	UEE094-5	Latched and synchronized (with MPCK-) version of MDTO-.
MDTORC	2	UBE116-15	RC timing term (10μ second) used in the development of MDTO-. MDTO- is enabled when the MDTORC voltage reaches the input threshold of the MDTO- gate.
MPCK	4	UFK094-3	Microprocessor clock. Active high version of MPCK-.
MPCK-	4	UDE083-8	Microprocessor clock. Active-low main timing term for controller logic.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
MPCK482-	4	UDE083-11	Microprocessor clock (MPCK-) signal with fast rise time, dedicated to the SN74S482 address generator clock inputs.
MSBADRINC	13	UHD050-13	Most significant address register increment. Output of microinstruction special group 0 decoder which increments the four-bit TILINE MSB address register when a TILINE master operation passes a 65K address boundary.
MSBADRLD-	13	UHD050-14	Most significant address register load. Loads a four-bit address from the processor bus into the TILINE MSB address register.
MSBADR (0-3)	8	UHD039	Four most significant TILINE address bits. Stored in an external TILINE MSB address register because there are only 16 address bits available from the CPE array at one time.
MSTRD-	13	UEE050-6	Master read. Output of microinstruction decoder which initiates a TILINE master read cycle.
MSTSTB	3	UDK061-3	Master cycle strobe. Clock input which triggers the master device go F/F to set and initiate a TILINE master read or master write cycle.
MSTWRT-	13	UEE050-7	Master write. Output of microinstruction decoder which initiates a TILINE master write cycle.
NOTRDY-	16	UJJ039-2	Not ready to start read/write, Inverted form of RDYSRW- (ready to start read/write) from selected disk unit. NOTRDY- high indicates that the head carriage has reached the specified cylinder and the heads have had time to settle, in addition to the FILERDY- conditions.
NRA (01-09)	5	UFE006, UHD017, UFK017	Next ROM address bits 1-9. Outputs of the NRA multiplexers, which serve as A inputs to the address generators.
OFFLINE-	16	UJD006-8	Disk offline. Inverted form of FILERDY- from disk drive.
ORDYA, B, C, D	17	UFE072, UGE061, UHD072, UHD028	FIFO output ready signals from each of the five-bit by 16-word FIFO devices. Indicates that the FIFO has data available at the outputs. Summarized as OUTRDY-.
OUTRDY-	16	UFE061-8	Summary FIFO output ready.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
PARDAT00	17	UFK083-12	Parallel data, bit 0. Most significant bit, and shift output, of serial/parallel shift register.
PARDAT (00-15)	17	UHJ083, UHD083, UFK061, UFK083	Parallel data outputs of serial/parallel shift register.
PBCPE-	12	UEE039-14	CPE to processor bus enable. An output of the PBUS source decode which enables the three-state CPE D-bus outputs onto the processor bus.
PBDSKDAT-	12	UEE039-11	Disk data to processor bus enable. An output of the PBUS source decoder which partially enables the FIFO and disk direct read register three-state outputs onto the P-bus. Selection between these sources is determined by direct/indirect mode F/F.
PBDSKSTA-	12	UEE039-9	Disk status to processor bus enable. An output of the PBUS source decoder which enables the three-state status line receiver outputs onto the processor bus.
PBTLDAT-	12	UEE039-12	Processor bus sourced by TILINE data. An output of the PBUS source decoder which enables data from the TILINE line receivers onto the processor bus. Controlled by bus source field (ROM13-15) of microinstruction.
PBUSENL	12	UEE028-2	Processor bus enable latched. Disables the processor bus source decoder during the time (immediately after MPCK- rising edge) that microinstruction outputs are unsettled. Signal is latched only in MDACT- goes active; otherwise, follows CLKT1-.
PBUS (00-15)	8-11	Multiple source bus	Processor bus.
PBZERO-	12	UEE039-15	Processor bus zero. Output of microinstruction bus source decoder that commands the processor bus to all zeros (high logic levels).

Signature	2262102 Sheet No.	Gate - Pin	Definitions
PFWP-	3	UAK105-4	Power failure warning pulse output of CPU selection multiplexer. See TILINE power failure warning pulse, TLPFWP-.
RCLK-	19	Disk Drive (UJJ039-11)	Read clock. One hundred nanosecond (nominal) active low clock pulses read from the selected disk track and separated from data by the clock/data separator in the disk drive.
RD-	19	Disk Drive (UJD006-13)	Read data. One hundred nanosecond (nominal) active low data pulses read from the selected disk track and separated from clock by the clock/data separator in the disk drive.
RDA-	19	UJD116-4	Read data into preset input of read 1 F/F.
RDATA-	19	UJD116-6	Read data output of read 1 F/F.
RDATAQ	19	UHD116-9	Read data output of read 2 F/F, converted from bit cell to NRZ format. Also used to store data in the test memory during closed-loop self-testing.
RDB	19	UJD116-2	Grounded D-input of read 1 F/F.
RDYDIRRST-	13	UJJ072-9	Ready direct reset. Strobed output of micro-instruction special group 0 decoder that resets the ready direct status F/F. Note that the F/F is in an upside down configuration, and RDYDIRRST- is wired to the preset input.
RDYDIRSTAT-	13	UJD017-5	Ready direct status. F/F which toggles on first FIFO/direct register SHIFTIN pulse after RDYDIRRST-. Indicates that valid data is available in the direct read register.
RDYDIRSTATQ-	16	UFK039-2	FIFO ready status. Latched and synchronized to microprocessor clock for I-bus input.
RDYSRW-	16	Disk Drive (UJJ039-1)	Ready to start read/write. Active when all file ready conditions are met and head carriage is at specified cylinder and head selection transients have dissipated.
RDYSTATUS-	17	UFK072-4	FIFO ready status. FIFO ready to accept data (disk write) or supply data (disk read).
RDYSTATUSQ-	16	UFK039-15	FIFO ready status. Latched and resynchronized to microprocessor clock for CPE I-bus input.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
READ-	2	UDE072-5	Slave read. TILINE slave logic read/write mode F/F output, controlled by TILINE read line receiver.
READQ-	14	UHD094-6	Disk interface read. Set during disk read operations after synchronization pulse is detected.
READQQ-	16	UFK039-7	Disk interface read latched and resynchronized to microprocessor clock for CPE I-bus input.
RESTORE-	13	UJJ061-6	Restore to track zero (also called return to zero seek). Output to disk drive which drives carriage to fully extended position and back to the home position, and clears drive fault latches and cylinder address register.
RG-	13	UJJ028-10	Read gate. Enables disk drive read circuits.
ROL-	9	UBE051-8	Right shift output of left byte CPE array.
ROM (00-07)	6	UDE006	Controller microinstruction ROM output bits 0-7.
ROM (8-15)	6	UDK017	Controller microinstruction ROM output bits 8-15.
ROM (16-23)	6	UEE006	Controller microinstruction ROM output bits 16-23.
ROM (24-31)	6	UGE017	Controller microinstruction ROM output bits 24-31.
ROM (32-39)	6	UEE017	Controller microinstruction ROM output bits 32-39.
ROM 13L, 14L, 15L, 20L, 21L, 33L	12	UEE028	Latched versions of the bus source, bus destination fields and bit 33 of the controller microinstruction. These are latched in a transparent D latch. When the enable signal, (MDACT-) is high, the output follows the input. When MDACT- is low (during TILINE master access cycle) outputs are latched up.
ROR-	11	UCC021-8	Right shift output of least significant stage of right byte CPE array.
RST	2	UFK116-7	Reset. General controller interface reset enabled by TILINE I/O reset (TLIORES-) or power reset (TLPRES-).

Signature	2262102 Sheet No.	Gate - Pin	Definitions
RTBYT-	8	UDK061-11	Right byte (only). Decoded from the micro-instruction word select field (ROM08,09) for right byte only instructions. Disables CPE left byte clock and left byte carry multiplexer.
RTSHFTRO	12	UDE050-9	Right shift output of least significant CPE stage from right shift multiplexer. Zero unless right shift (F-group 0, R-group 111) is performed.
SECMRK-	16	Disk Drive (UJJ039-13)	Sector Mark. A rotational position pulse which identifies the start of each sector.
SECTORB01-, 02-04-, 08-	16	Disk Drive (UJD028)	Sector address. Sampled by the disk controller after the sector mark is sensed.
SECTORB16-	16	Disk Drive (UJJ050-17)	Sector address. Sampled by the disk controller after the sector mark is sensed.
SECTORMRK-	16	UHJ039-8	Sector mark - latched. The sector mark latch sets on the first sector mark after a microinstruction-controlled clear sector and index (CLRSECIDX-) pulse. Stores sector mark for the I-bus input latch.
SECTORMRKQ-	16	UFK039-12	Sector Mark. Latched and resynchronized to microprocessor clock. Provides sector mark input to CPE I-bus.
SELECTA-	14	UJJ017-2	Select disk drive A. When low, selects the dual disk drive designated A, usually the first drive. DISKSEL- also required for individual logical unit selection.
SELECTB-	14	UJJ017-6	Select disk drive B. When low, selects the dual disk drive designated B, usually the second drive. DISKSEL- also required for individual logical unit selection.
SHFCMD	12	UCE072-13	Shift command. Active when CPEs perform a shift operation (F-group 0, R-group III). Disables left and right byte carry multiplexers when active.
SHFTPRE	12	UDE028-4	Partially decoded term used in development of SHFTPRE- and, consequently, SHFCMD.
SHFTPRE-	12	UDE061-6	Partially decoded term used in development of SHFCMD.
SHIFT	17	UGE050-9	Shift command used to clock the FIFO timing F/F. Supplied by SHIFTIN for read operations, SHIFTOUT for write operations.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
SHIFTIN	18	UEE083-8	Shift command to FIFO input circuits. Loads a 20-bit data and flag word into the FIFO.
SHIFTOUT	18	UEE083-6	Shift command to FIFO output circuits. Unloads a 20-bit data and flag word from the FIFO, so that the next word in line may be shifted to the FIFO output.
SIGNBIT-	7	UDK039-3	Sign bit. The immediate operand ($I\overline{M}$) field of a microinstruction contains only eight bits. Except for left byte only instructions, the immediate operand is supplied to the right byte CPE K-bus inputs, and SIGNBIT- extends the sign bit to all the left byte K-bus inputs.
SKIC-	16	Disk Drive (UJJ050-2)	Seek incomplete, also called seek error. Disk output which indicates that the head carriage failed to seek to the specified cylinder address.
SLADOK	4	UAE028, UAE050, UAE083	TILINE slave address okay. Sets the slave transfer F/F if the received TILINE slave address equals the local board address as determined by switches and hardwired address bits.
SLBUSY-	4	UBE083-3	Slave busy. Strobe which returns a hardwired 1 on TILINE bit 0 output if a slave read is attempted on a busy controller.
SLGODLY	4	UDK050-6	Slave go delay. A protective delay (100 nsec) which assures that the incoming TILINE slave address has stabilized before it is decoded.
SLGORC	4	UBE072-12	RC term used in development of SLGODLY-.
SLSW (13-16)-	4	UAE083-4, 6, 10, 12	TILINE slave address switch outputs.
SLTM	4	UBE105-3	TILINE slave terminate. Output to the TILINE terminate line driver. Indicates that the slave logic has completed the specified operation. If a slave read is directed to a busy controller, an immediate slave terminate is issued, accompanied by a data 1 in the data word bit 0 position.
SLTMA-	4	UBE083-6	Slave terminate access. Enables a normal slave terminate at the completion of a slave cycle (controlled by SLVTRM- from microinstruction decoder).

Signature	2262102 Sheet No.	Gate - Pin	Definitions
SLTMB-	4	UBE083-11	Slave terminate B. Enables an immediate terminate and busy indication if a slave read is addressed to a busy controller.
SLVA-	4	UDE072-9	Output of one of the two FIFOs which control TILINE slave operation.
SLVACT	5	UDK039-8	Slave active. Disables interrupt priority encoder and serves as a slave trap address input.
SLVAD-	4	UDK061-6	Slave cycle_enable. Enables a TILINE slave cycle if the enable slave bit (ROM16) of the micro-instruction is set and the slave transfer F/F is set.
SLVB-	4	UFK028-5	Output of one of the two F/F's which control TILINE slave cycles.
SLVTRM-	13	UEE050-5	Slave terminate. Output of microinstruction special field decoder, controlled by ROM32, 33. Causes TILINE slave logic to issue a TILINE terminate, ending the slave cycle.
SLXFR	4	UBK072-5	Slave transfer. Slave transfer F/F sets upon expiration of the 100 nanosecond slave go delay if the incoming TILINE address equals the board slave address.
SPAREIN1-	11	Disk Drive (UGE039-1)	Spare input (J1) from disk drive to CPE I-bus.
SPAREIN2-	11	Disk Drive (UJJ039-5)	Long self-test check jumper (J2), if installed, grounds SPAREIN2-. This causes the micro-program to execute the long self-test on power-up for test only.
SPAREIN (3-6)-	16	UJD028, UJJ050	Spare inputs from disk drive to disk status word (processor bus) input.
SPAREOUT1	13	UJJ061-10	Status update strobe. During self-test the controller microprogram maintains a status count which is updated as various test segments are successfully completed. SPAREOUT1- is pulsed each time the status count is updated. Available as a strobe to synchronize logic analyzer or oscilloscope.
SPAREOUT2-	13	UJJ061-8	Spare output.
SPAREOUTQ1-	14	UJJ017-12	Latched spare output. A spare output of the disk select register.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
STBCLR-	13	UJJ072-7	Allows a deliberate clearing of the disk control functions in the special function 2 decoder/ register.
STBRST-	13	UJJ105-6	Strobe reset. Clears the special function 2 decoder/register in the event of a general reset (RST-), an interrupt reset (INTRST-), or a strobe clear from special function 0 (STBCLR-).
STOPFLAG	18	UHJ028-12	Write data (to disk) transfer stop flag. This flag accompanies the last TILINE-to-FIFO word through the FIFO. When it reaches the FIFO output, the transfer to disk should be stopped.
STRTREAD-	14	UGE116-12	Interface read logic clear.
SWAIN-	16	Disk Drive (UJJ050-13)	Switch fixed/removable unit numbers on drive A, if low. Controlled by jumper J1-J3 of adapter board mounted on drive A. Normal designation (SWAIN- high) is: unit 0 - fixed disk unit 1 - removable disk cartridge.
SWBIN-	16	Disk Drive (UJJ050-11)	Switch fixed/removable unit numbers on drive B, if low. Controlled by jumper J1-J4 of adapter board mounted on drive B. Normal designation (SWBIN- high) is: unit 2 - fixed disk unit 3 - removable disk cartridge.
SYNCQ-	14	UGE094-10	Synchronization character detected and latched. Enables read operations after the 6E synchronization character is detected.
SYNC6E	14	UJD083-8	Synchronization character present. Goes low for one disk clock time when the 6E synchonization character is detected.
TESTBIT-	12	UAK072-9	Input to test bit flip-flop from word look-ahead carry generator.
TESTBITQ	12	UBK072-8	Output of test bit F/F which steers execution of all conditional branch and conditional return microinstructions.
TESTCLK-	13	UFK050-5	Test clock. Microinstruction-controlled clock pulse which replaces disk read or write clock as the disk I/F timing source during controller self-test. Burst frequency is approximately 833.3 KHz.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
TESTDATA	19	UFK127-3	Test data output of TMS 3129 serial shift register memory used for controller closed-loop self-tests.
TESTMODEQ	13	UFK050-4	Test mode output of microinstruction special group 1 decoder/register. Sets up data paths for controller closed-loop self-test.
TESTOUTIN	19	UFK127-6	The TMS 3129 serial test memory consists of 2 sections, each with a 1-by-132 capacity. TESTOUTIN connects the output of one section to the input of the other, for a 1-by-264 net capacity.
TESTRDDAT-	19	UFK105-6	Test read data. Test data out of the serial test memory to the read data logic, as gated by TESTMODEQ. Self-test only.
TIMERRQ	14	UGE094-6	FIFO timing error - latched. Detects FIFO errors during read and write operations such as attempting to load a full FIFO or attempting to retrieve data from a FIFO without any data in it.
TLABORT-	2	UCE094-8	TILINE abort. Input to TILINE abort latch which sets the latch if a power failure warning (TLPFWP-) or a general I/O reset (IORES-) signal is received.
TLABORTL	2	UDE094-4	TILINE abort latch. Sets if controller operations are to be aborted by the power failure warning pulse (TLPFWP-), the power reset (TLPRES-) or a general I/O reset (TLIORES-).
TLABORTQ-	5	UEE094-10	Latched and synchronized (with MPCK-) version of TLABORTL. This microcode interrupt signal generated if a power failure warning, power reset, or I/O reset is issued to all the controllers in the 990 chassis.
TLADR (00-19)	8, 9, 10, 11	CPE devices, TILINE	TILINE address. A 20-bit address which accompanies any word transferred on the TILINE.
TLAGIN	3	TILINE (UCE094-2)	TILINE access granted input from higher priority masters. TLAGIN must be high for the TILINE master cycle to initiate the 100 nanosecond device access request minimum timer.
TLAGOUT	3	TILINE (UCE094-3)	TILINE access granted output to lower priority masters. TLAGOUT is disabled during the device access request and device acknowledge states of the TILINE master cycle.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
TLAK-	2	TILINE (UBE116-9)	TILINE acknowledge. As an input, must be inactive (high) for the TILINE master cycle to advance to the device acknowledge state. As an output, is asserted during the device acknowledge state.
TLAV	2	TILINE (UBE116-7)	TILINE available. As an input, must be active for the TILINE master cycle to advance to the device access state. Disabled by the controller in device access sate.
TLDATA (00-15)-	8, 9, 10, 11	UAK028, UAE061, UAE017, UAK083	TILINE data.
TLDATEN-	2	UDK072-6	TILINE data enable. Enables TILINE data line drivers during a master write or slave read cycle.
TLERR-	2	UBK083-6	LINE error. Sets the TILINE error latch if a rity error (TLMER) is returned by TILINE memory during a master read cycle.
TLERRL-	2	UDE094-7	TILINE error latch output. See TLERR-.
TLERRQ-	5	UEE094-7	Latched and synchronized version of TLERRL-, used in interrupt trap circuits. Initiates a microcode interrupt trap if a memory parity error is detected while the controller is reading data from 990 memory for transmission to the disk.
TLGO-	2	TILINE (UAE094-15)	TILINE go. Control strobe asserted by a TILINE master throughout a data transfer. Used by slaves to enable slave address decoding, initiate slave response.
TLINT-	13	UBE072-2	TILINE interrupt. Disk controller interrupt to the 990 CPU. Enabled by a special group 1 microinstruction.
TLINTLED-	13	UBE072-4	TILINE interrupt indicator. Light-emitting diode indicator that lights when the controller sends an interrupt (TLINT-) to the 990 CPU.
TLINTQ	13	UFK050-9	TILINE interrupt. Output of microinstruction special group 1 decoder/register which enables an interrupt (TLINT-) to the 990 CPU.
TLIORES-	2	TILINE (UAE094-7)	TILINE I/O reset. Master clear signal from 990 CPU to all I/O controllers.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
TLMER	2	TILINE (UAK094-4)	TILINE memory error. Asserted by TILINE memory if a parity error is detected as part of a memory read operation.
TLPFWP-	3	TILINE (UAK105-2)	(TILINE) Power failure warning pulse. Advance notice from the 990 power supply that a power failure is imminent. Precedes power reset.
TLPRES-	2	TILINE (UDE094-3)	(TILINE) Power failure reset. Reset signal from 990 power supply that assures that I/O logic is cleared, and that it restarts in an orderly manner.
TLREAD-	2	TILINE (UAE094-3)	TILINE read. Identifies read/write TILINE operations.
TLSHIN-	18	UBK094-11	TILINE shift in. Generated during write data or write data unformattted operations to shift data from the TILINE line receivers into the FIFO.
TLSHOUT-	18	UBK094-3	TILINE shift out. Generated during read data or read data unformatted operations. Shifts a new word to the FIFO output after a word is transmitted to 990 memory via a master write cycle.
TLTM-	2	TILINE (UBE116-2)	TILINE terminate. Asserted by TILINE slave when read data is available or write data has been accepted.
TLWAIT-	2	TILINE (UAE094-9)	TILINE wait. Asserted only by TILINE bus couplers.
TRAP-	5	UDK072-8	Trap signal that steers the next ROM address multiplexers to gate a trap vector address to the address generators. Generated while servicing a TILINE slave trap, microcode interrupt trap, power or I/O reset trap.
TRIGTMR-	13	UJJ072-10	Trigger command timer. Output of micro-instruction special group 0 decoder that retriggers command timer, preventing expiration of the 200 millisecond delay.
UNITA	14	UHJ017-5	Select unit A. Disk select output which when high specifies the dual disk drive designated A (the first drive). Requires DISKSEL for complete selection of a logical unit.
UNITB	14	UHJ017-2	Select unit B. Disk select output which specifies dual disk drive B. Requires DISKSEL for complete logical unit selection.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
UNITLOAD-	12	UFE028-11	Unit load. Loads the disk selection signals from the processor bus into the disk select register.
UTCSHIN-	12	UFE028-10	UTC shift in. Loads a word from the CPE outputs into the FIFO, such as when writing headers during a write format operations.
UTCSHOUT-	18	UFE050-8	UTC shift out. Unloads a word from the FIFO output when the CPE has accepted the word, such as during self-tests.
WCHK-	16	Disk Drive (UJJ050-6)	Write check, also called fault. Indicates that the disk drive electronics has detected a fault condition and inhibited write and erase currents.
WCLK	19	UJD105-8	Write clock. A 5MHz square wave (200 nano-second pulse width) clock used to encode write data and clock.
WCLKAQQ-	19	UJJ116-6	Write clock divider output. The 2.5 MHz output of clock divider. Serves as the source for DCLK (disk clock) during write operations. Also used in write data and clock encoding.
WDNCLK-	19	UJD050-6	Write data and clock. Double-frequency (FM) bit cell encoded data and clock to disk drive.
WDNCLKEN	19	UJD105-3	Write data and clock enable. A signal used in write data and clock encoding. Always high at clock time, high at data 1 time, low (to inhibit output pulse) at data 0 time.
WG-	13	UJD050-8	Write gate, to disk drive, enables write current.
WOSCSTOP-	19	HH124	Write oscillator stop. External test input.
WOSTST-	19	JJ124	Write oscillator stop external test input.
WP-	16	Disk Drive (UJJ050-8)	Write protect. Indicates that data may not be written to the selected logical unit because the disk drive WRITE PROTECT switch for that fixed or removable disk is ON.
WRITEQ	14	UHJ094-9	Write, latched. Output of write F/F in disk I/F start and read/write control logic.
WRITEQD	14	UFK094-11	Input to write F/F in disk I/F start and read/ write control logic. Enabled when micro-instruction specifies a write operation (DSKWRTQ = 1) and the disk start F/F (DSTARTQ) sets.

Signature	2262102 Sheet No.	Gate - Pin	Definitions
WRTDATD	19	UHD105-7	Serial output of write data CRC multiplexer to write data and clock encoding circuits.
WRTDATOUT-	19	UHD116-5	Serial write data out, in NRZ form to write data and clock encoders. Also, self-test write data to serial test memory via read 2 (RDATAQ) F/F.
WRITTIMERR-	5	UFK105-3	Write timing error. Generated if a FIFO timing error is detected during a write to the disk. This signal is synchronized (as CLRWRTQ-) to initiate a microcode interrupt trap routine.
ZERODATEN-	15	UCE094-11	Zeros or data enable. Enables three-state outputs of FIFO data out/zero multiplexer onto processor bus.

APPENDIX D

MICROCODE FLOWCHARTS

APPENDIX D

MICROCODE FLOWCHARTS

D.1 GENERAL

The disk controller operations are controlled by a microprogram which is permanently burned into a set of five ROM devices. The microprogram consists of 512 words of 40 bits each. This appendix contains a complete set of flowcharts for the microprogram. The flowcharts, together with the listings of Appendix E, form a powerful tool for troubleshooting and analysis at the most detailed level. The flowcharts also provide insights into controller operation that cannot be provided by any other means.

The principle flowchart in Section 2 (figure 2-10) shows the overall program organization and the relationship between the major routines.

D.2 USING THE FLOWCHARTS

Each process block in the flowcharts represents a single microinstruction, which may also be considered a controller state. Each block is identified by a three-letter mnemonic (IDL, INI, RDU) and a two-digit decimal number. The mnemonic identifies the routine or subroutine, and the number identifies the individual state (microinstruction). The three-digit hexadecimal address of the instruction is also shown adjacent to each process block. The identifiers and addresses also appear in the microprogram listings to simplify cross references between the two forms of documentation.

The information within each process block summarizes the 3002 CPE operation and identifies the most important of the other functions performed by the microinstruction. Table D-1 defines the symbols which are used in the process blocks. Registers R0-R9, T, and AC refer to registers internal to the 3002 CPE devices.

Conditional branches or returns are represented by a process block and a decision block. The decision is based on the carry or right shift output of the CPE operation. The process block associated with a conditional branch/return usually specifies CPE clock stop (CLKSTP). The CPE clock stop inhibits the clock input to the CPE, but does not affect microprocessor clock to other parts of the controller, such as the ROM address generator. The CPE clock stop allows the CPE to perform nondestructive bit testing and select the next microprogram address without changing the contents of any CPE registers. Refer to the 3002 CPE description and the test bit description for additional information.

Table D-2 is an index to all the flowcharts in this appendix. The flowcharts are arranged alphabetically by mnemonic. The sheet numbers refer to the sheets of figure D-1, rather than to page numbers in this appendix.

Figure D-2 contains a short microcode segment (SKS subroutine) that has been superseded by ECNs 428322 and 428323.

Table D-1. Symbols Used in Flowcharts

Symbol	Definition
I	Data on the I-bus
CI	Carry In
LI	Left In
CO	Carry Out
RO	Right Out
AC	Contents of the accumulator
T	Contents of T
MAR	Contents of the memory address register
+	Two's complement addition
-	Two's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
$\rightarrow$	Deposit into
L	(Subscript) Left byte operation
R	(Subscript) Right byte operation

Table D-2. Microcode Flowchart Index

Mnemonic	Title	Sheets
CCS	Check CRC and Stop	1
DST	Delay Start	3
DWS	**Disk Write Start**	4
HCU	Head/Cylinder Update Routine	5
INC, FAV	Increment AC and FIFO Available	7
IDL	**Idle**	8
INI	Initialize	9
INT	Interrupt	14
LTC	Long Test Check	17
RDD	Read Data	18
RDU	Read Unformat	24
RST	Restore	26
RUP	Record Update	28
SDS	Search, Delay Start	29
SKS	**Seek Subroutine**[1]	30
SRD	Slave Read	32
SWR	Slave Write	34
SRG	Store Registers	37
SRW	Store Registers Write	39
SSS	Start Sector Search	40
SSX	Secondary Start Transfer	41
STX	Start Transfer	42
TRM	Terminate Routine	47
VID	Verify ID Words	51
WCS	Write CRC and Stop	57
WFT	Write Format Track	59
WHD	Write Header	65
WRD	Write Data	67
WRU	Write Unformat	73
WST	Write Stop	76
ZAC	Z Abort Check	77
ZDR	Z Direct Register	78
ZDT	Z Diagnostic Test	79
ZER	Z Error Routine	93
ZRF	Z Register Fill	94
ZRH	Z Read Header	95
ZRT	Z Register Test	99
ZSU	Z Status Update	100
ZTC	Z Test Clock	101

Note: Offsheet references take the form "D-X" or "D-X, Y" and should be read "see Figure D-X, sheet Y."
Note: [1]Refer to figure D-2 for SKS subroutine prior to ECNs 428322, 428323.

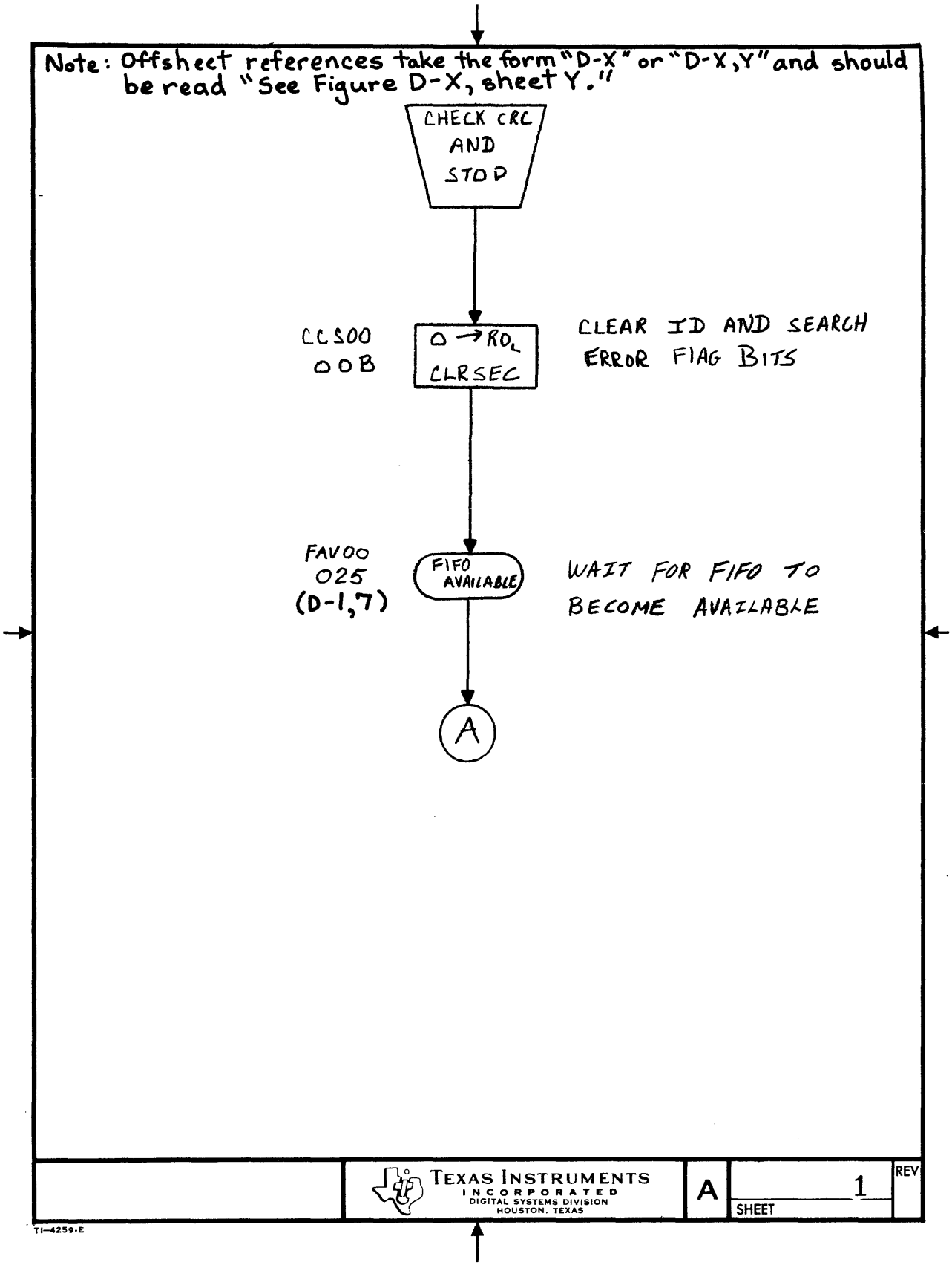


Figure D-1. Microcode Flowcharts (Sheet 1 of 101)

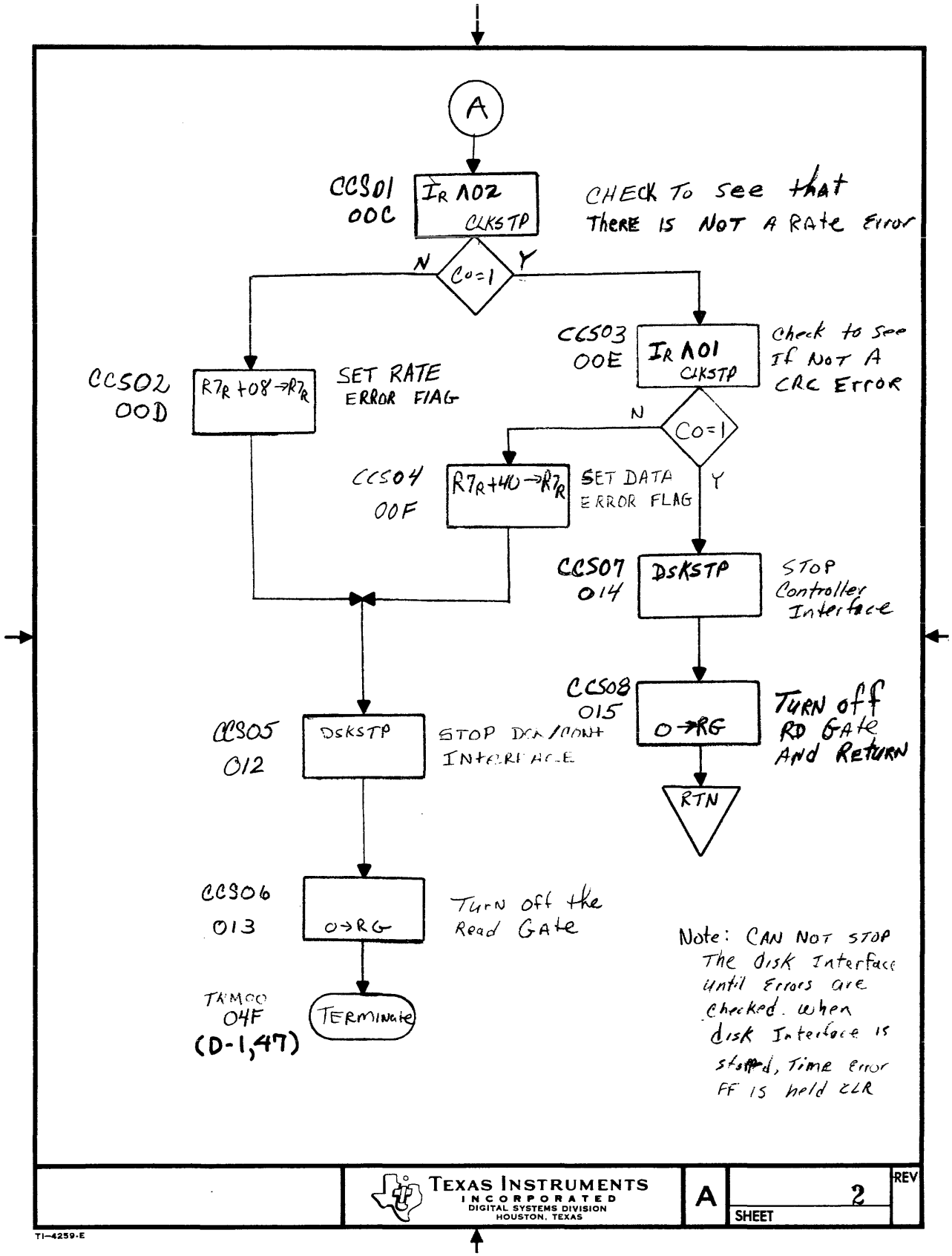


Figure D-1. Microcode Flowcharts (Sheet 2 of 101)

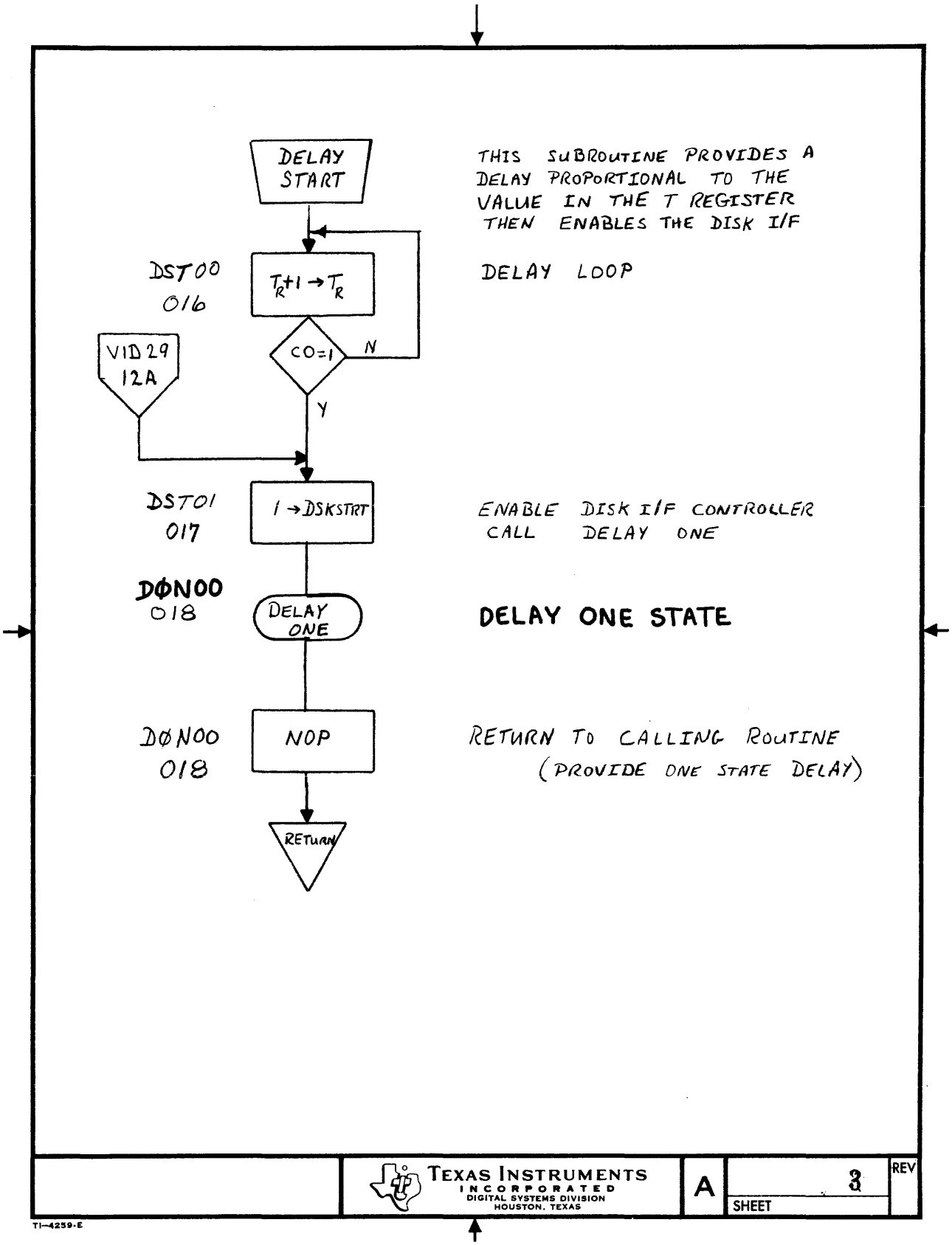


Figure D-1. Microcode Flowcharts (Sheet 3 of 101)

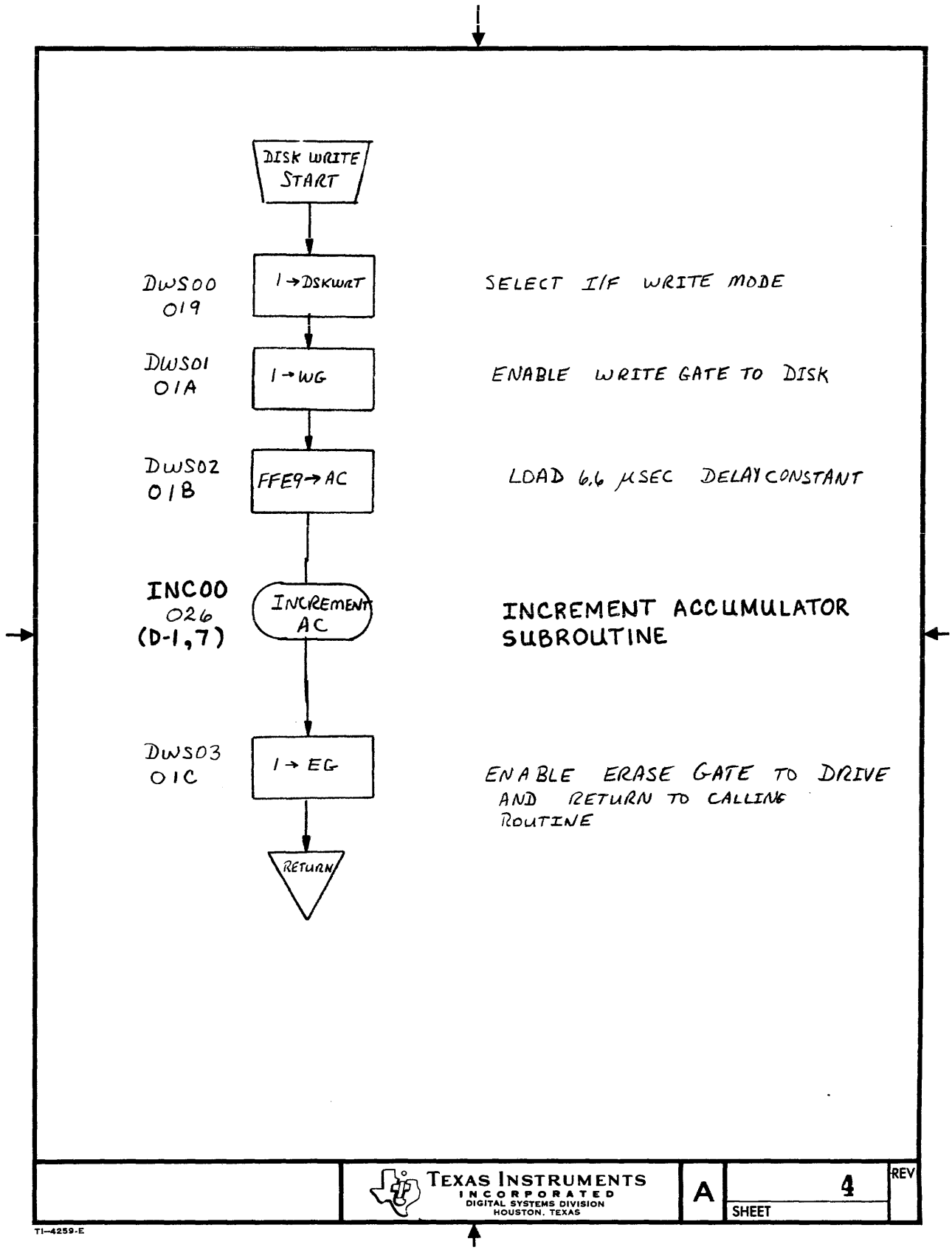


Figure D-1. Microcode Flowcharts (Sheet 4 of 101)

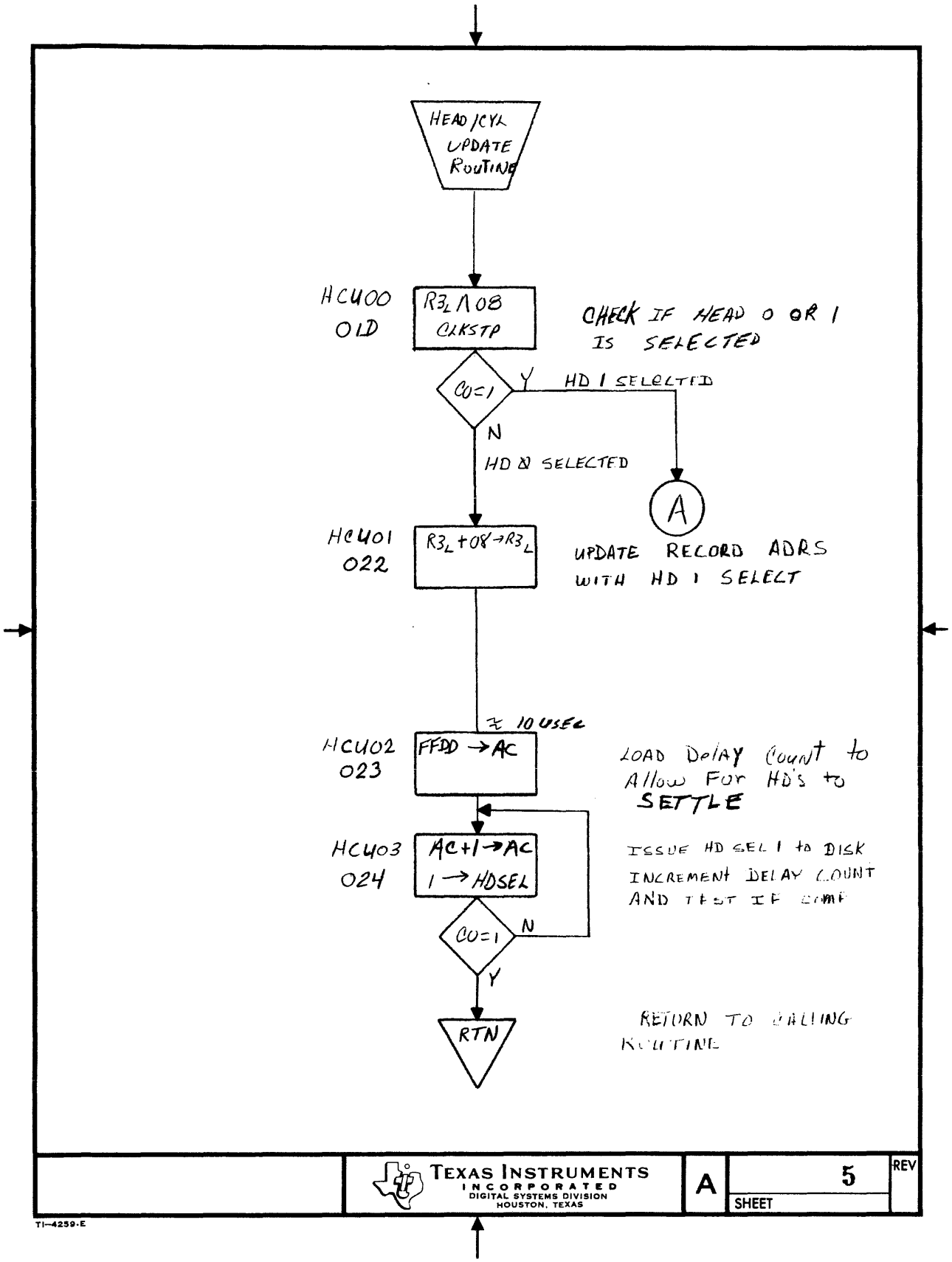


Figure D-1. Microcode Flowcharts (Sheet 5 of 101)

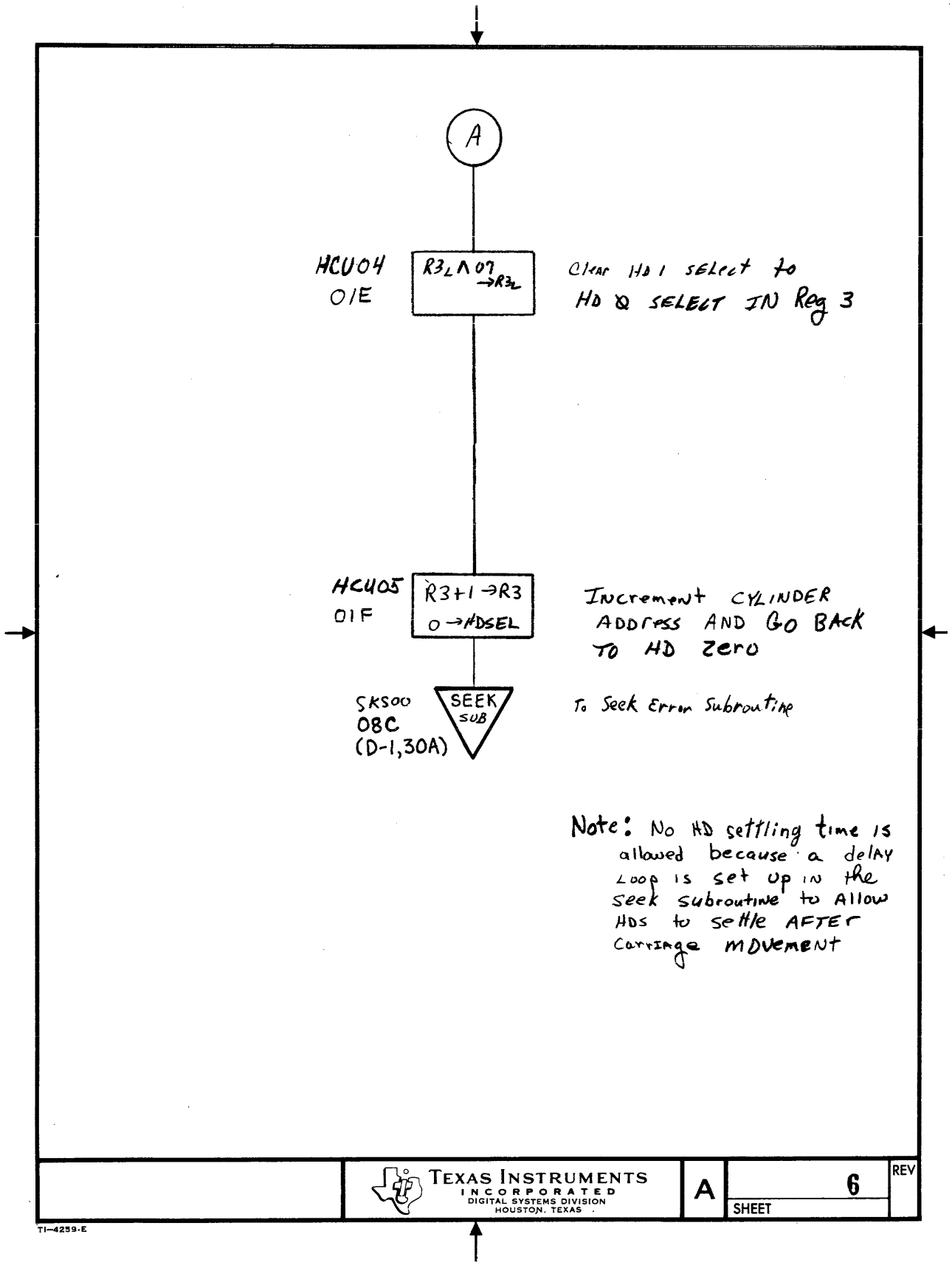


Figure D-1. Microcode Flowcharts (Sheet 6 of 101)

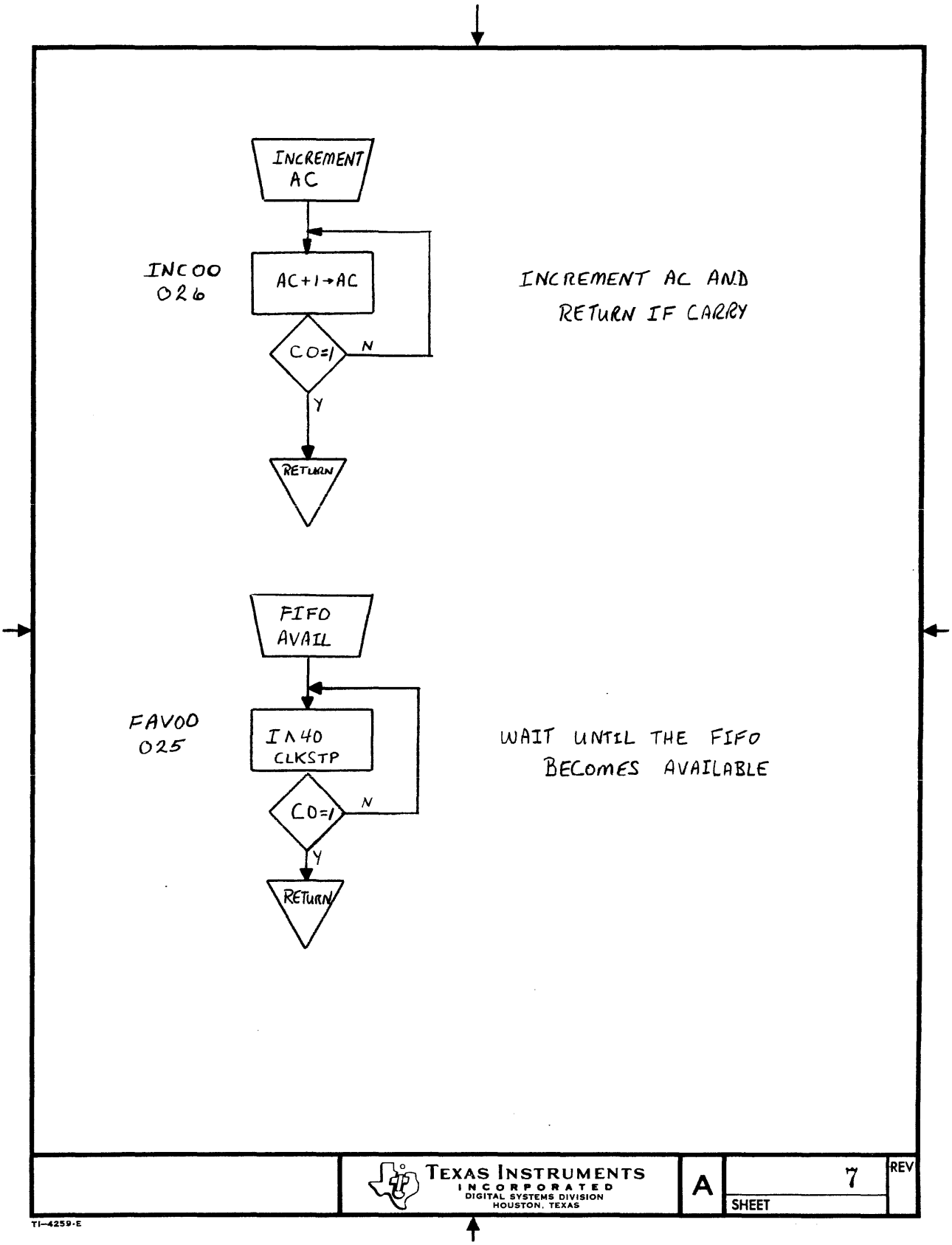


Figure D-1. Microcode Flowcharts (Sheet 7 of 101)

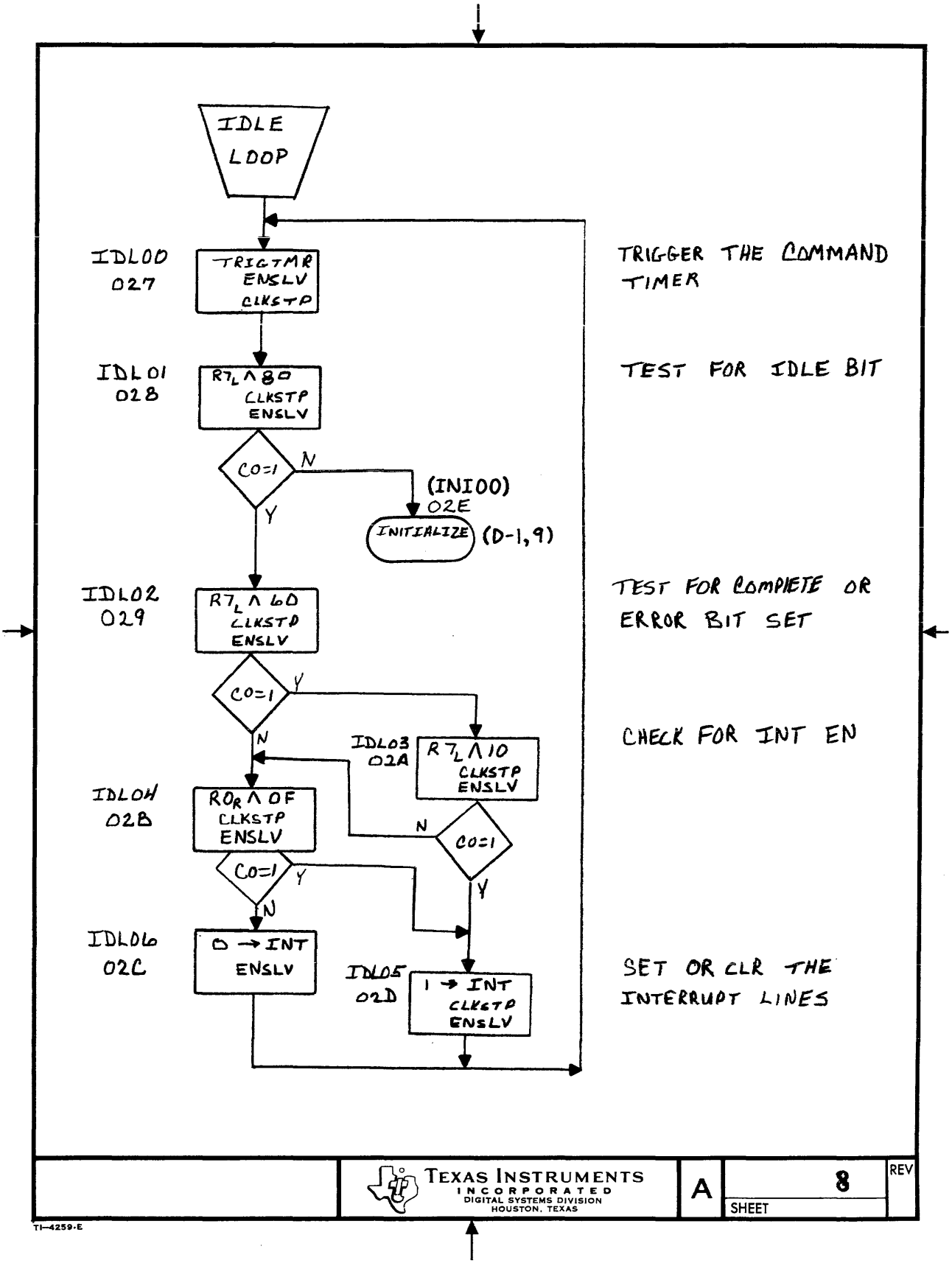


Figure D-1. Microcode Flowcharts (Sheet 8 of 101)

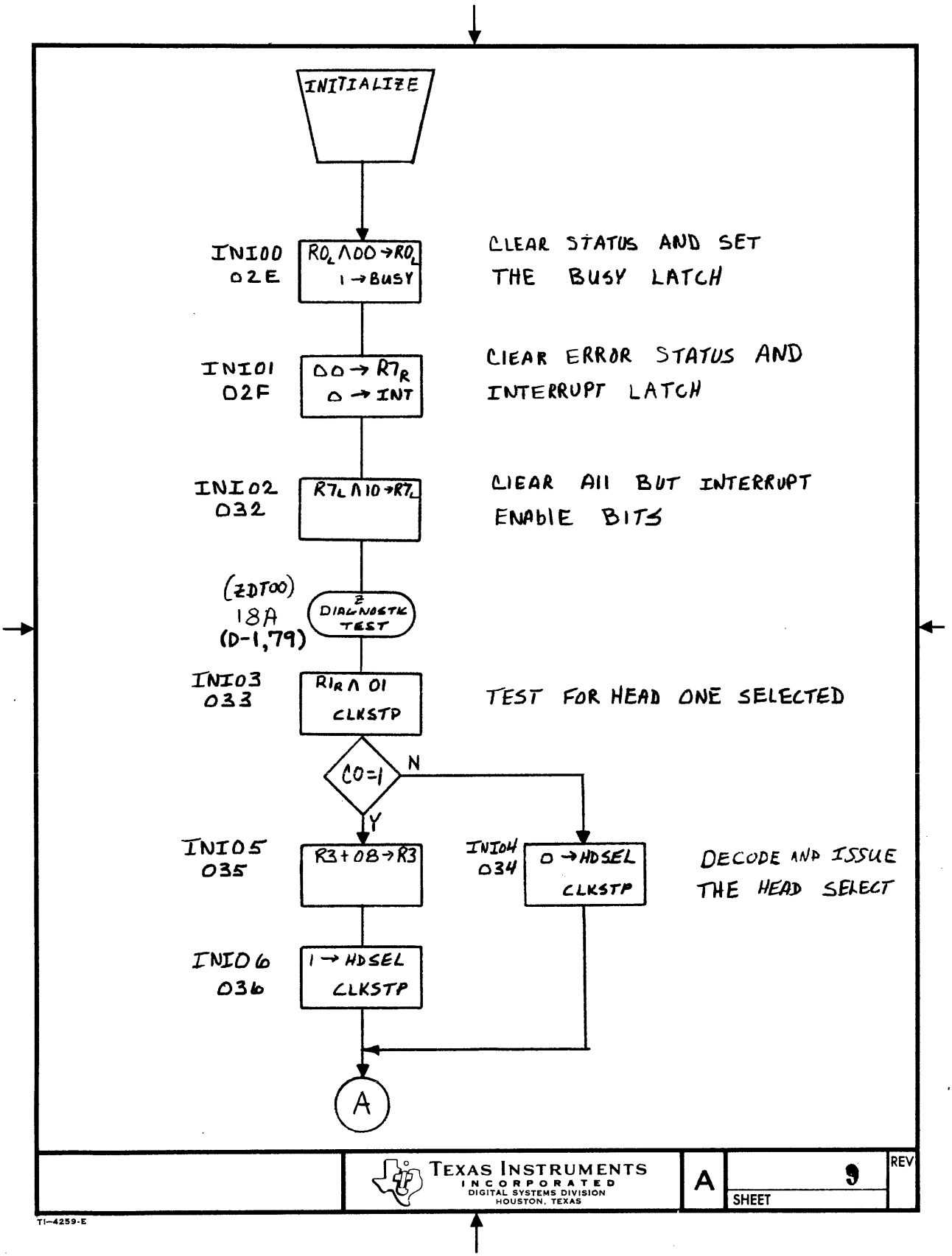


Figure D-1. Microcode Flowcharts (Sheet 9 of 101)

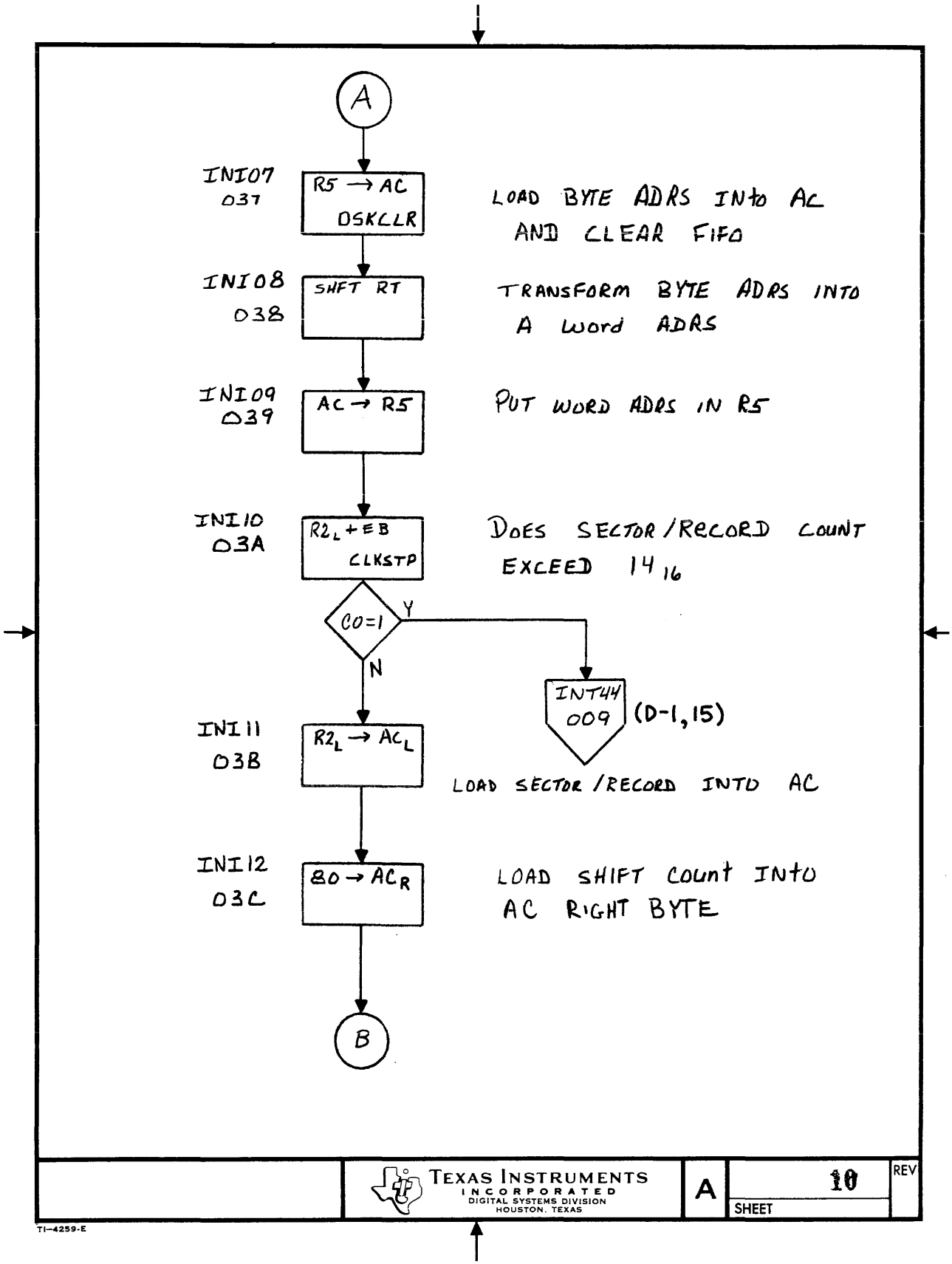


Figure D-1. Microcode Flowcharts (Sheet 10 of 101)

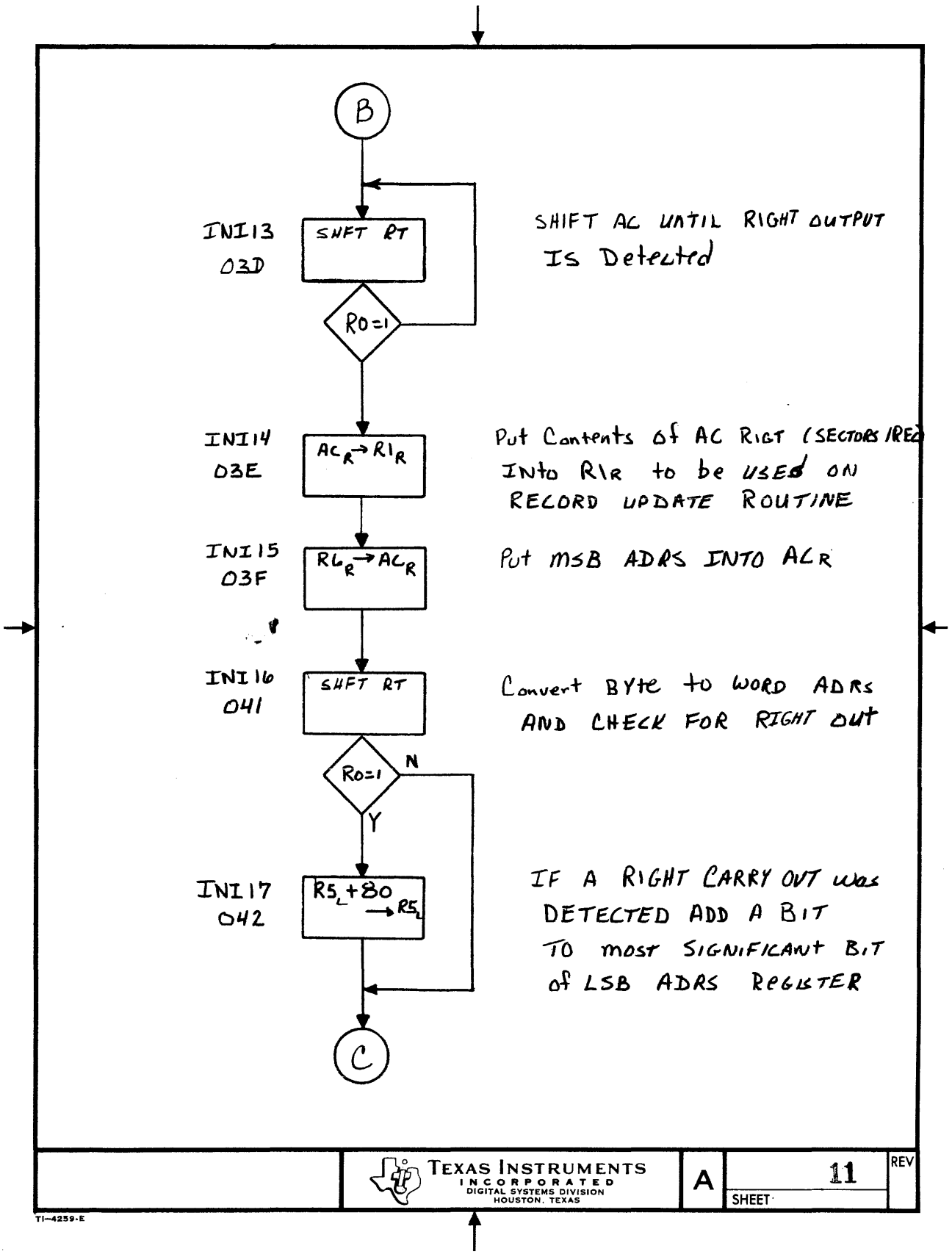


Figure D-1. Microcode Flowcharts (Sheet 11 of 101)

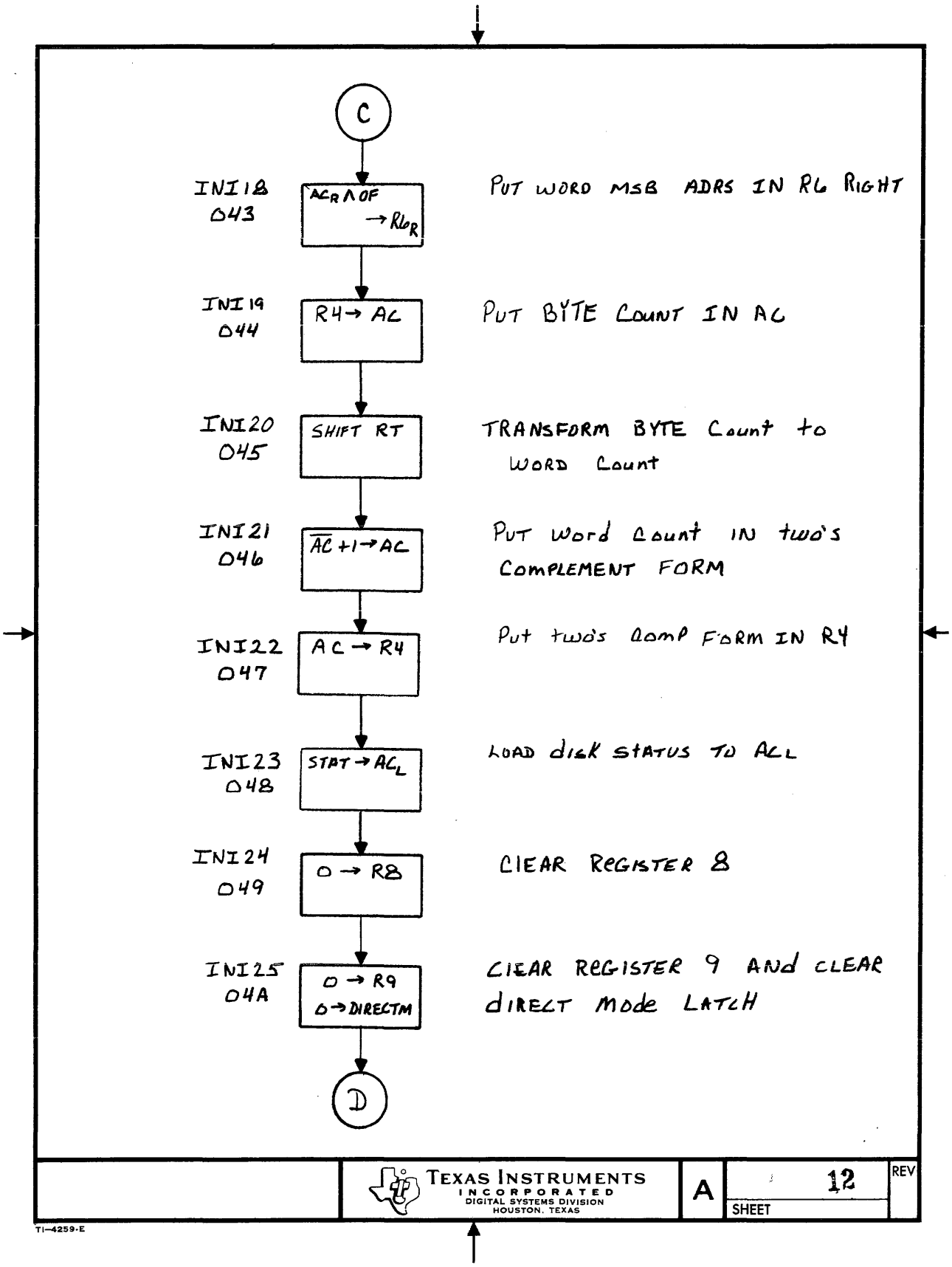


Figure D-1. Microcode Flowcharts (Sheet 12 of 101)

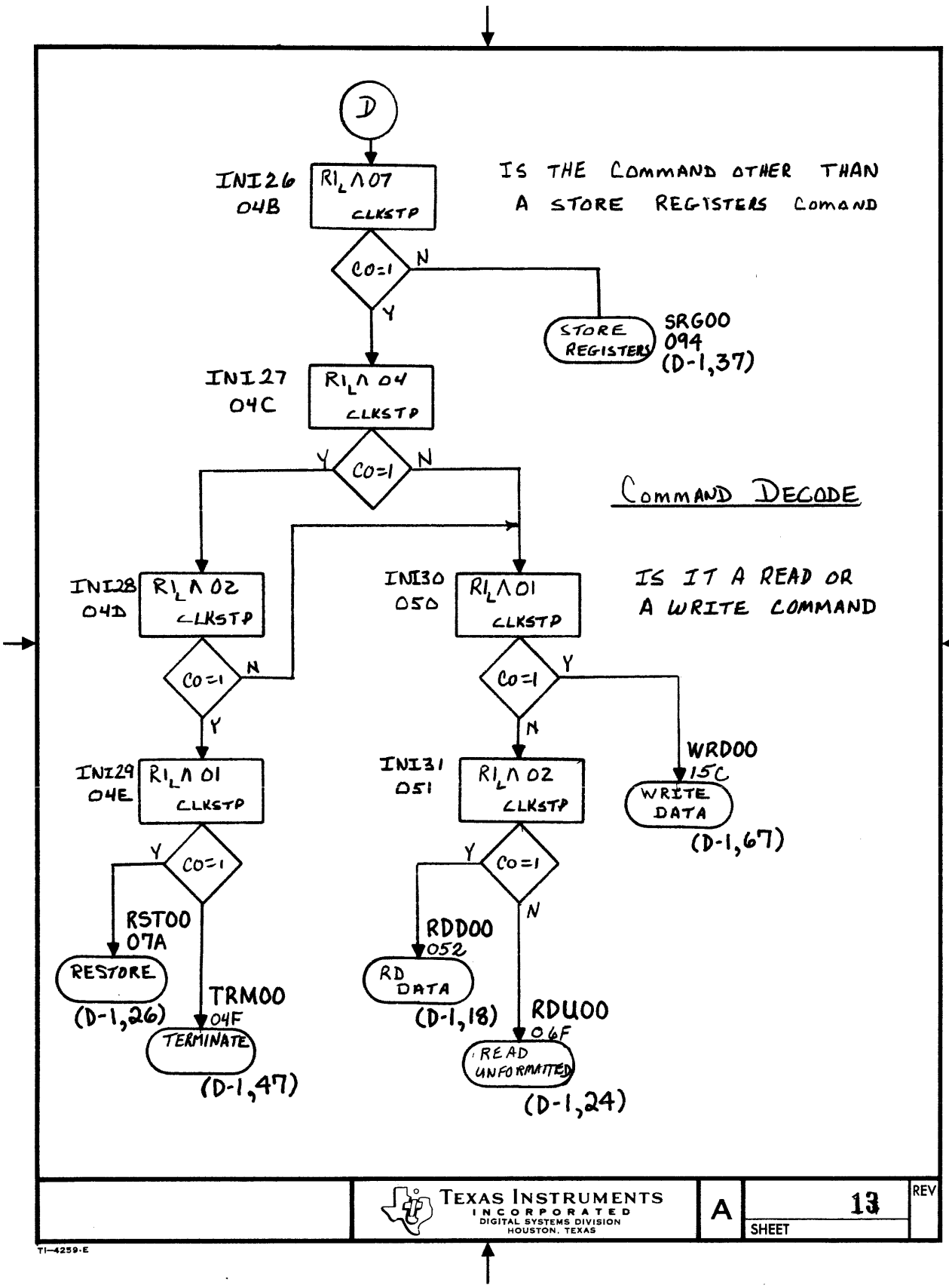


Figure D-1. Microcode Flowcharts (Sheet 13 of 101)

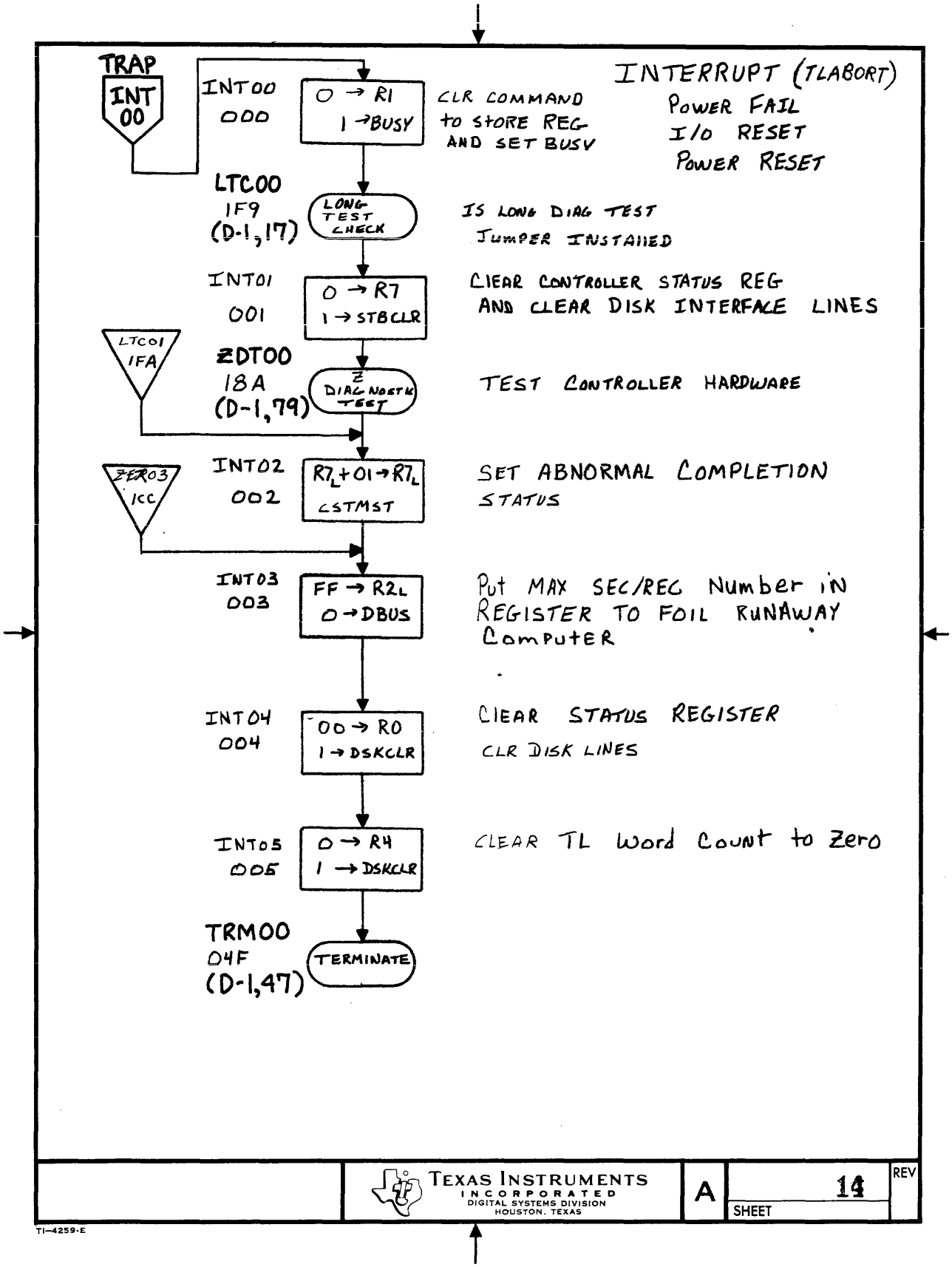


Figure D-1. Microcode Flowcharts (Sheet 14 of 101)

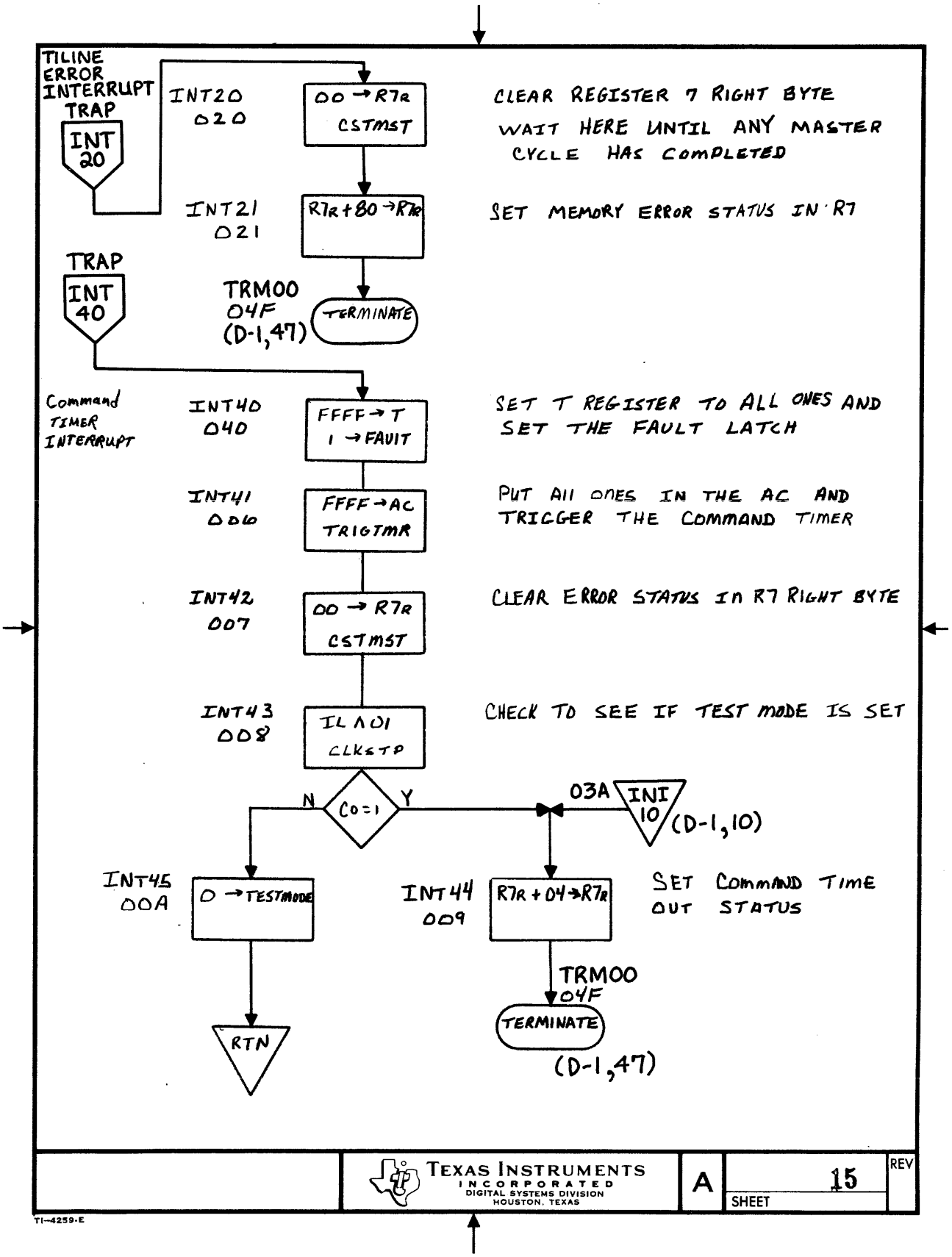


Figure D-1. Microcode Flowcharts (Sheet 15 of 101)

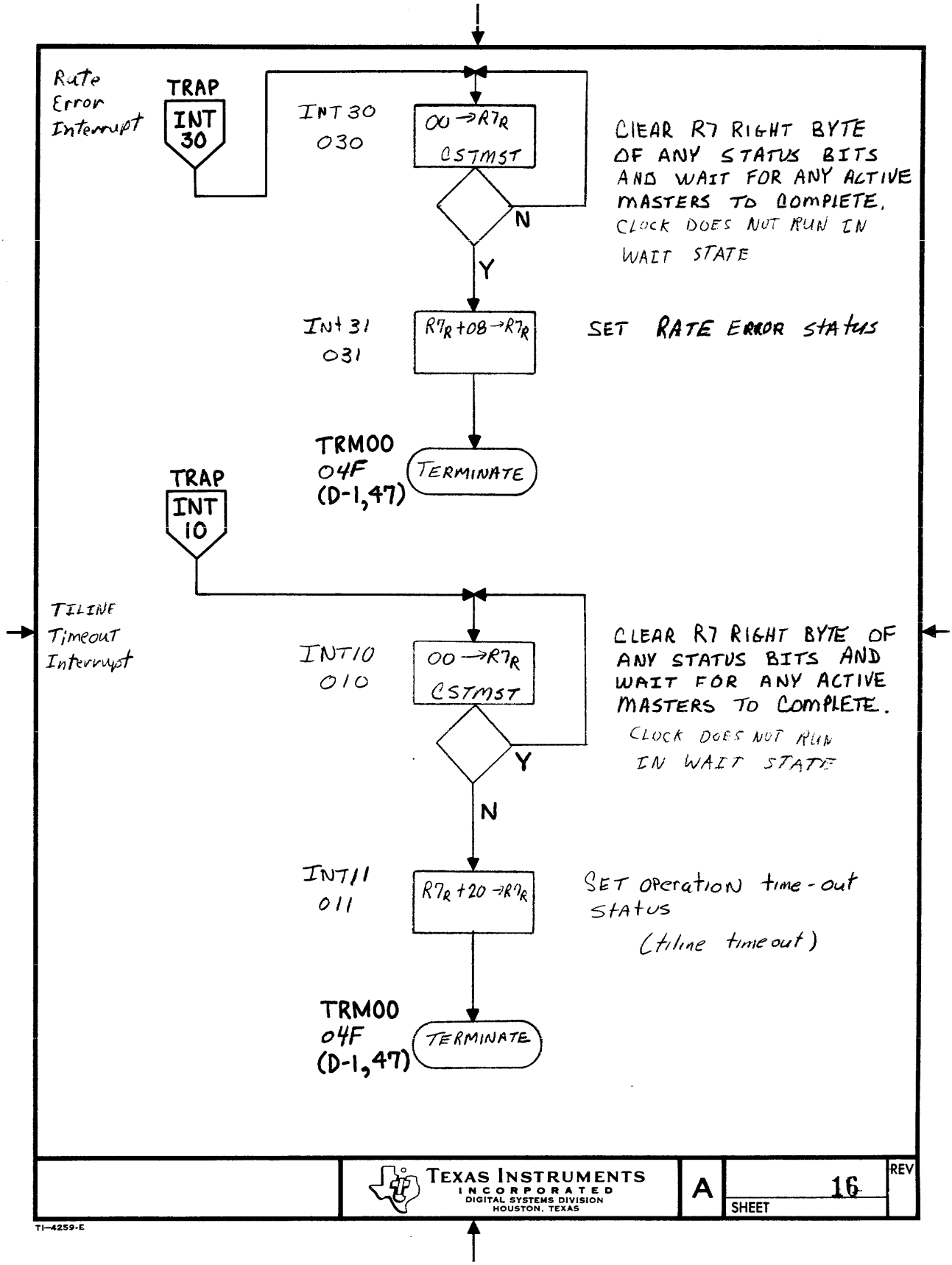


Figure D-1. Microcode Flowcharts (Sheet 16 of 101)

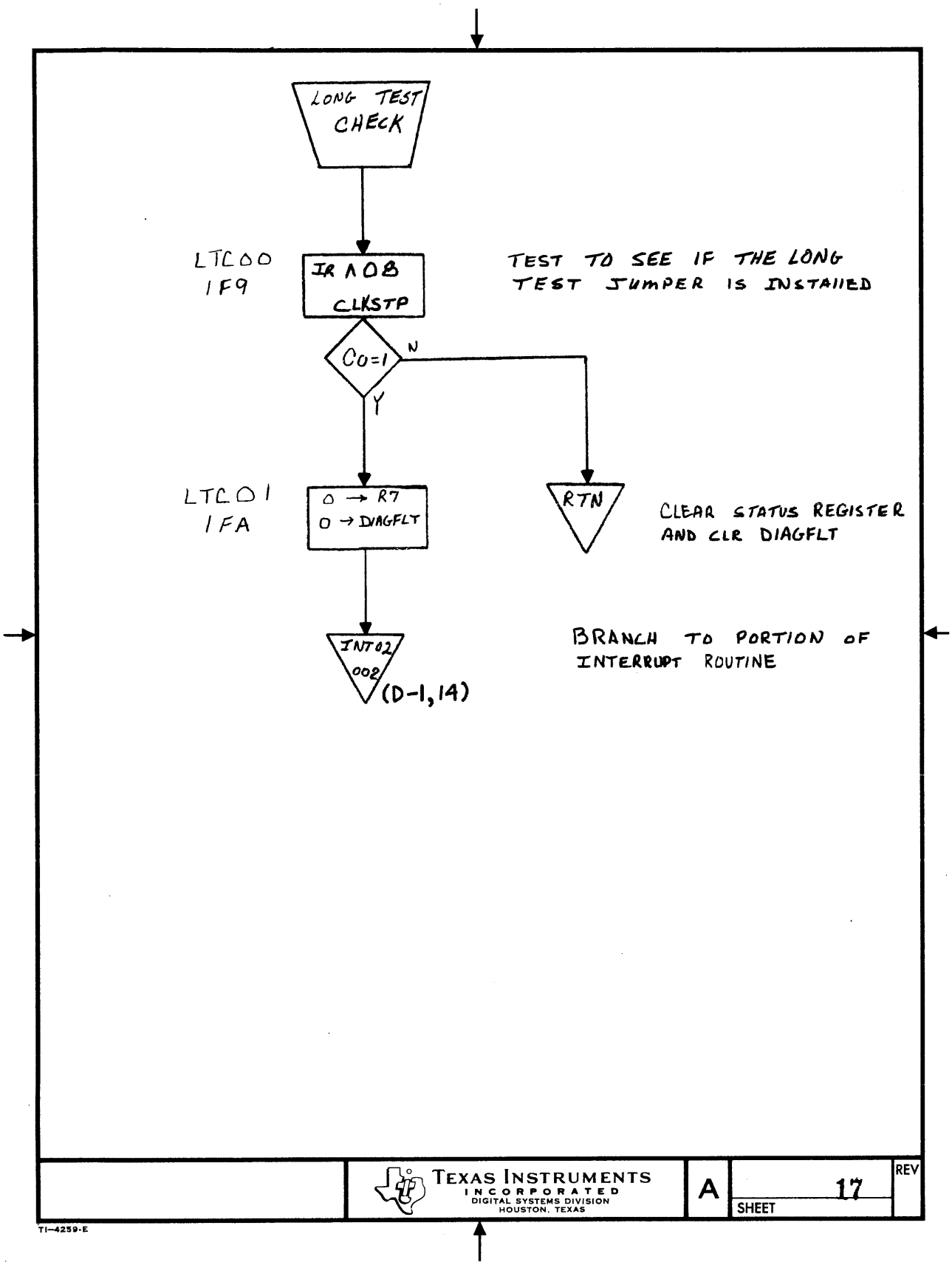


Figure D-1. Microcode Flowcharts (Sheet 17 of 101)

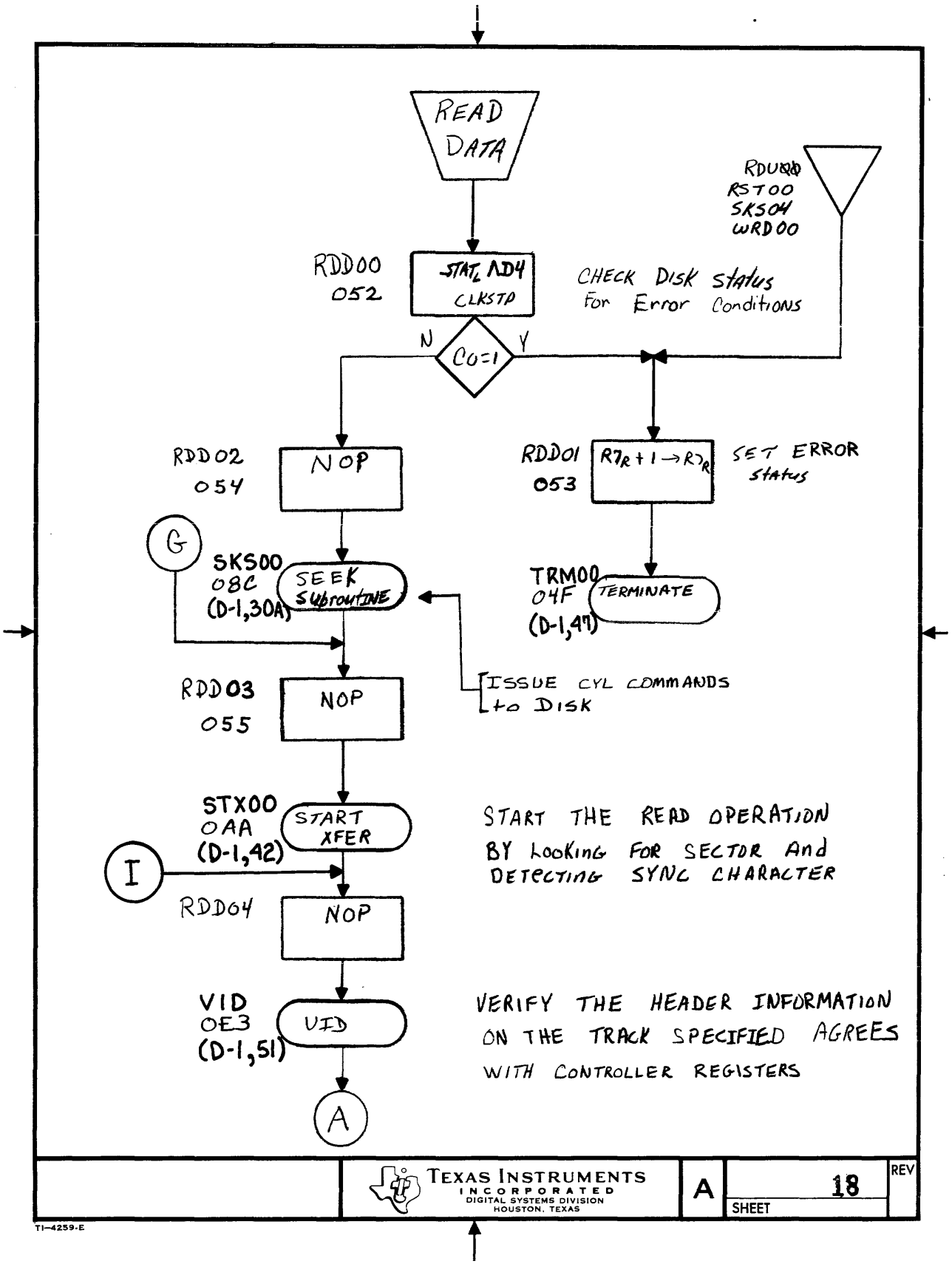


Figure D-1. Microcode Flowcharts (Sheet 18 of 101)

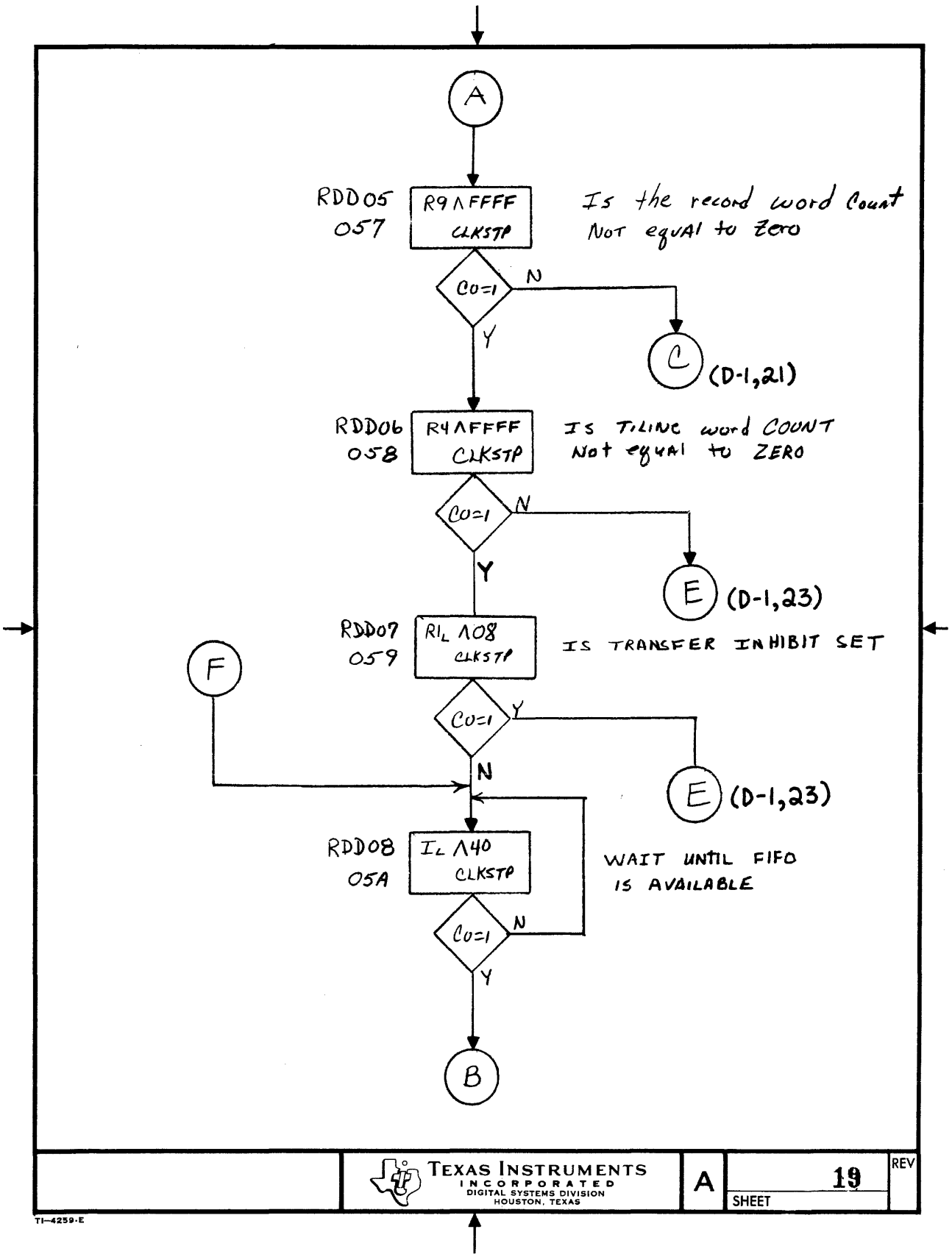


Figure D-1. Microcode Flowcharts (Sheet 19 of 101)

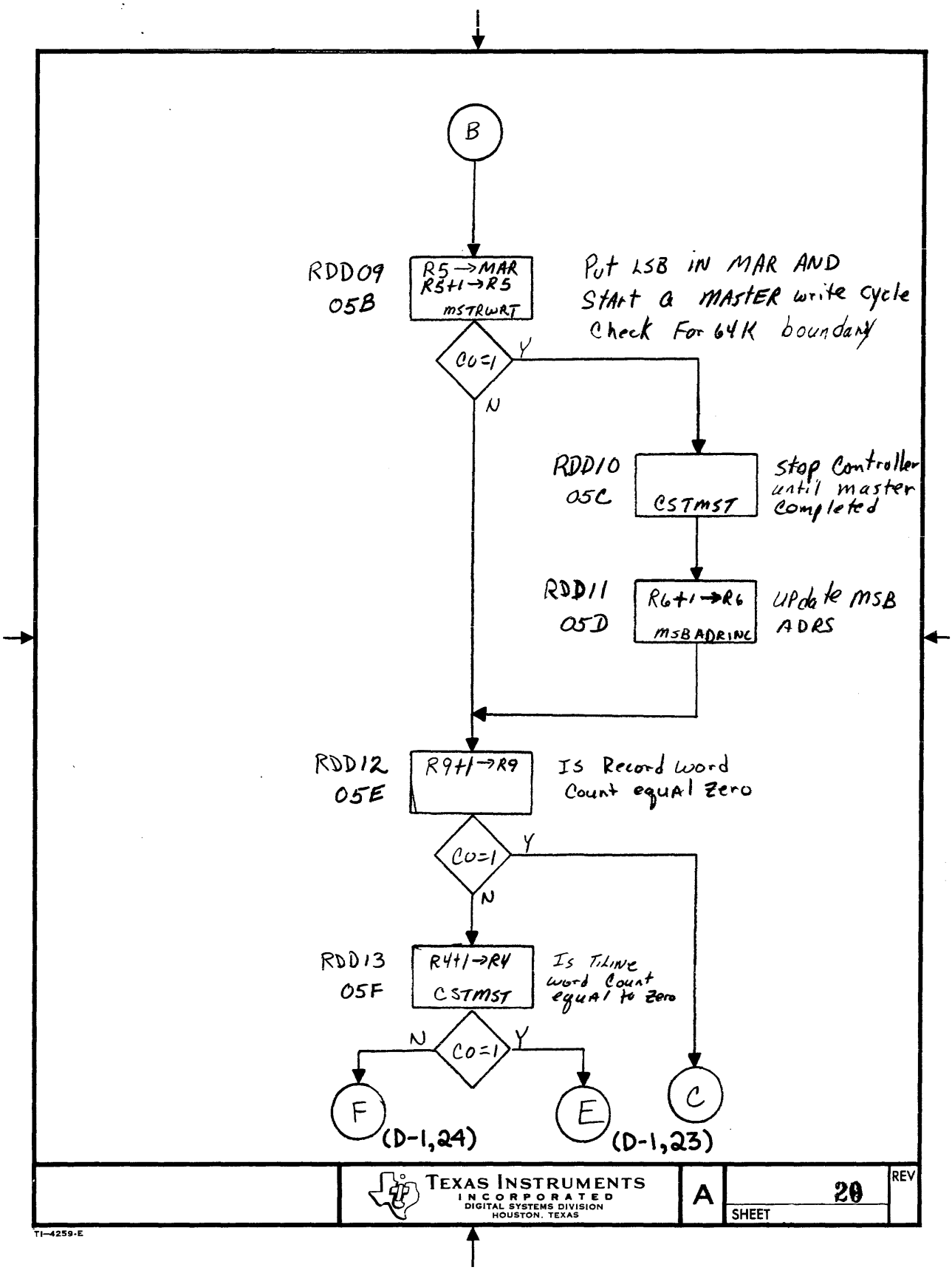


Figure D-1. Microcode Flowcharts (Sheet 20 of 101)

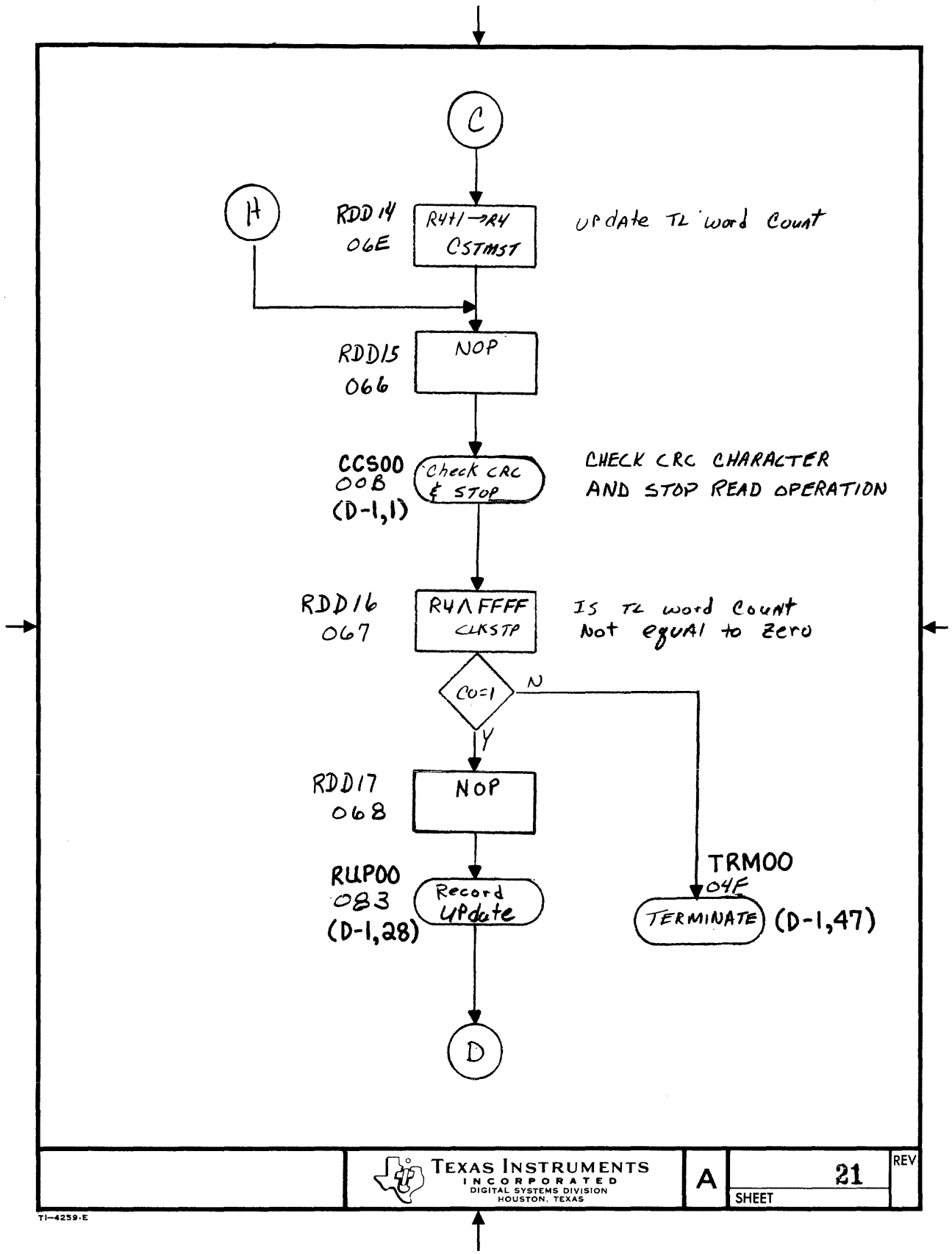


Figure D-1. Microcode Flowcharts (Sheet 21 of 101)

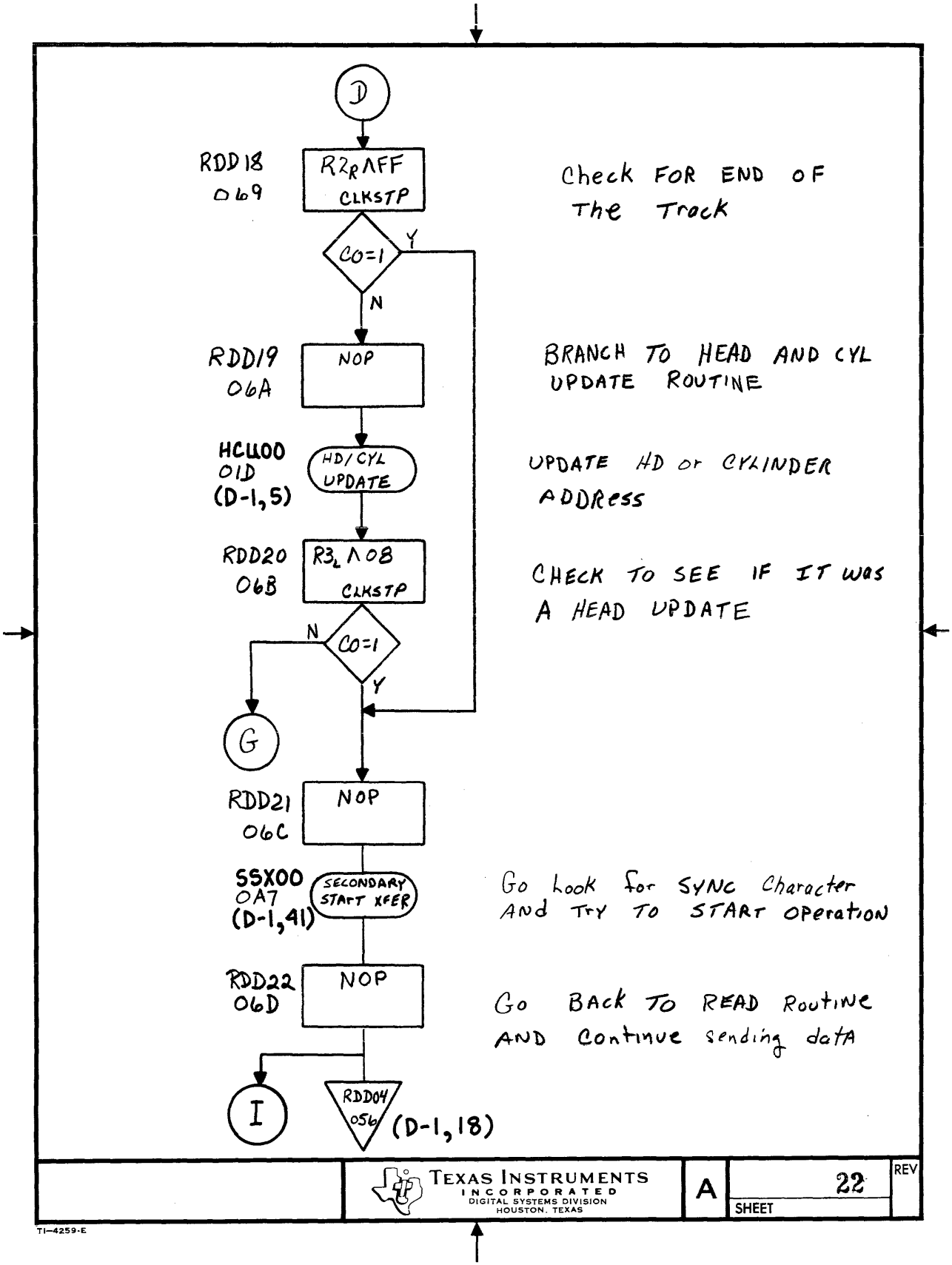


Figure D-1. Microcode Flowcharts (Sheet 22 of 101)

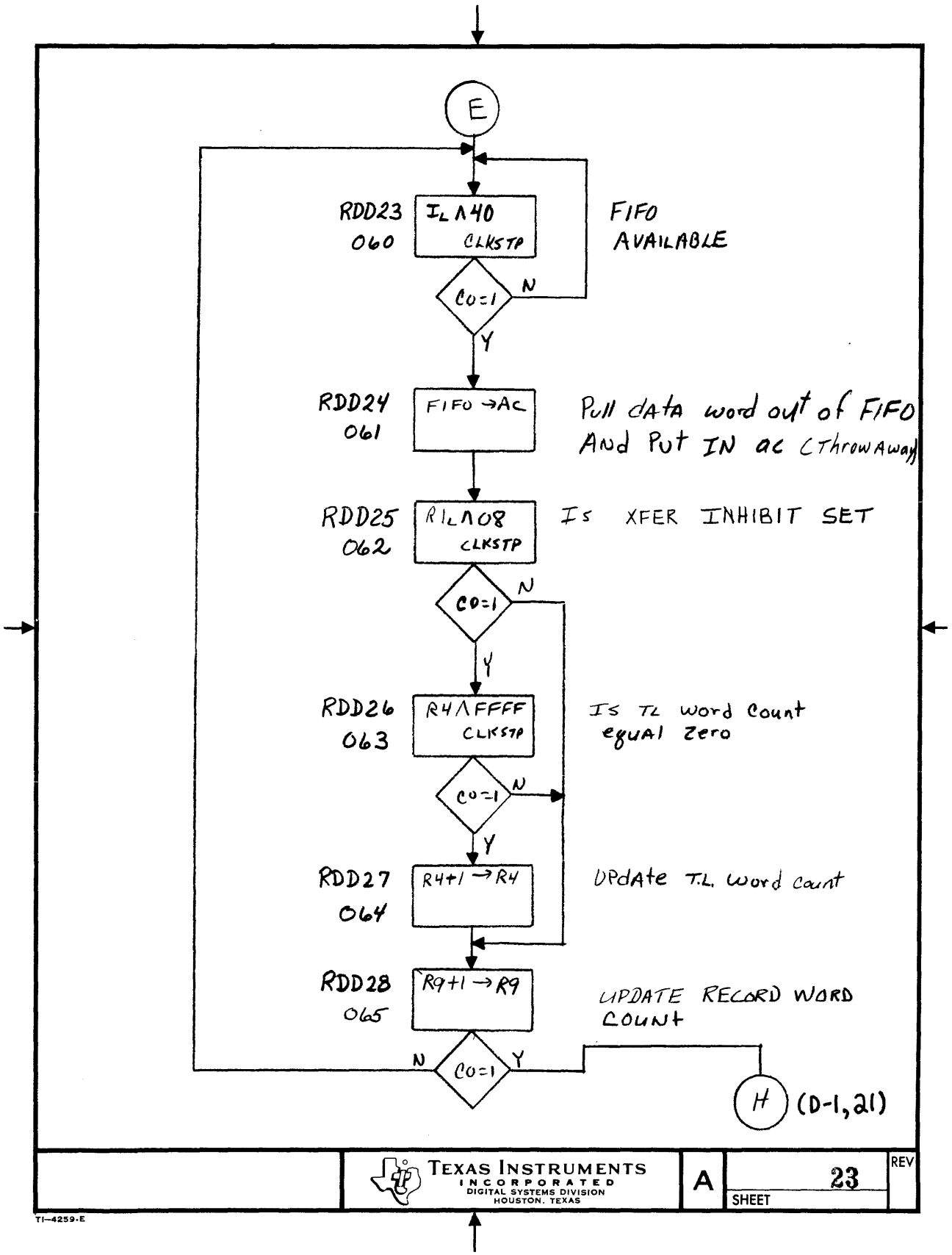


Figure D-1. Microcode Flowcharts (Sheet 23 of 101)

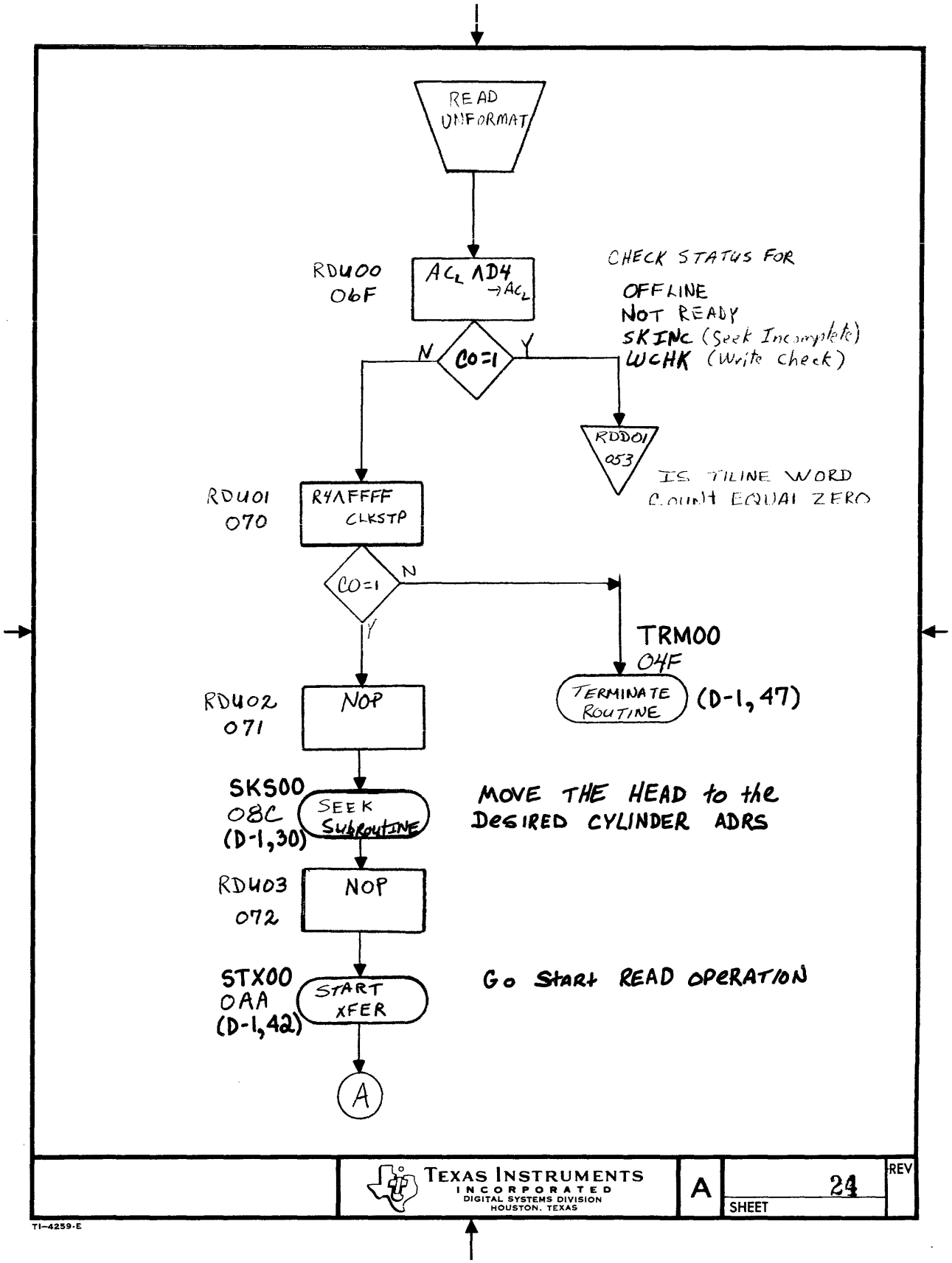


Figure D-1. Microcode Flowcharts (Sheet 24 of 101)

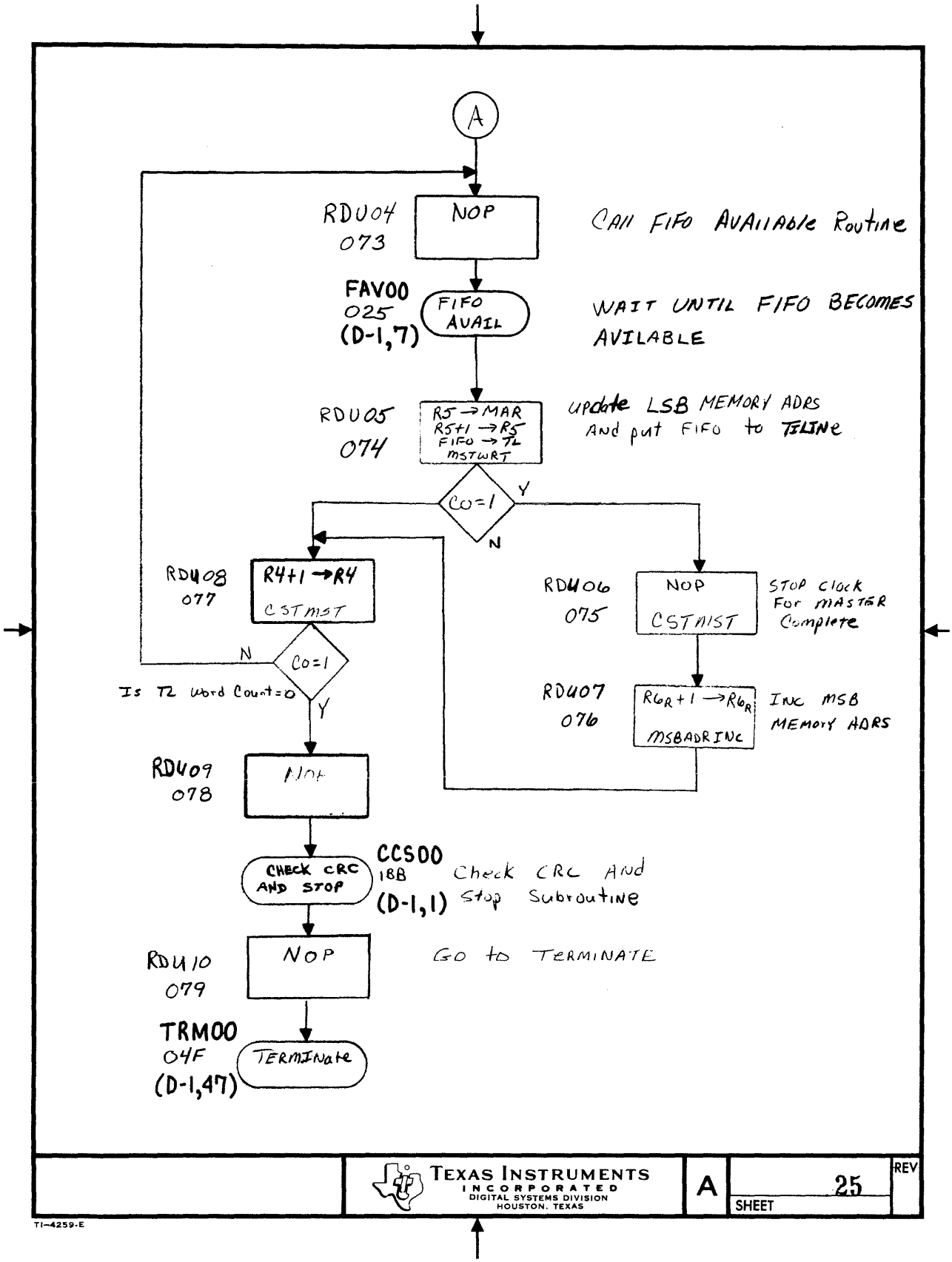


Figure D-1. Microcode Flowcharts (Sheet 25 of 101)

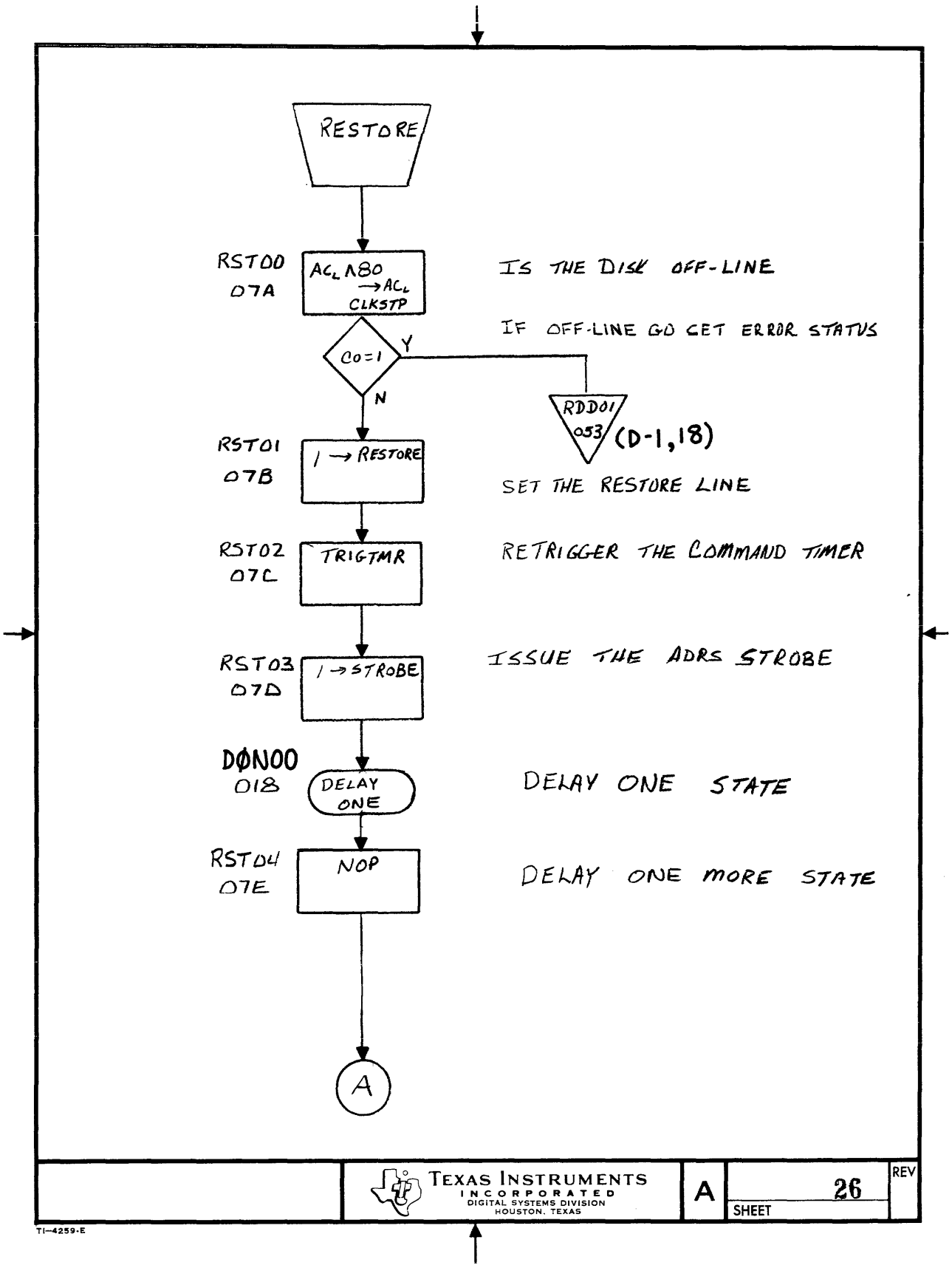


Figure D-1. Microcode Flowcharts (Sheet 26 of 101)

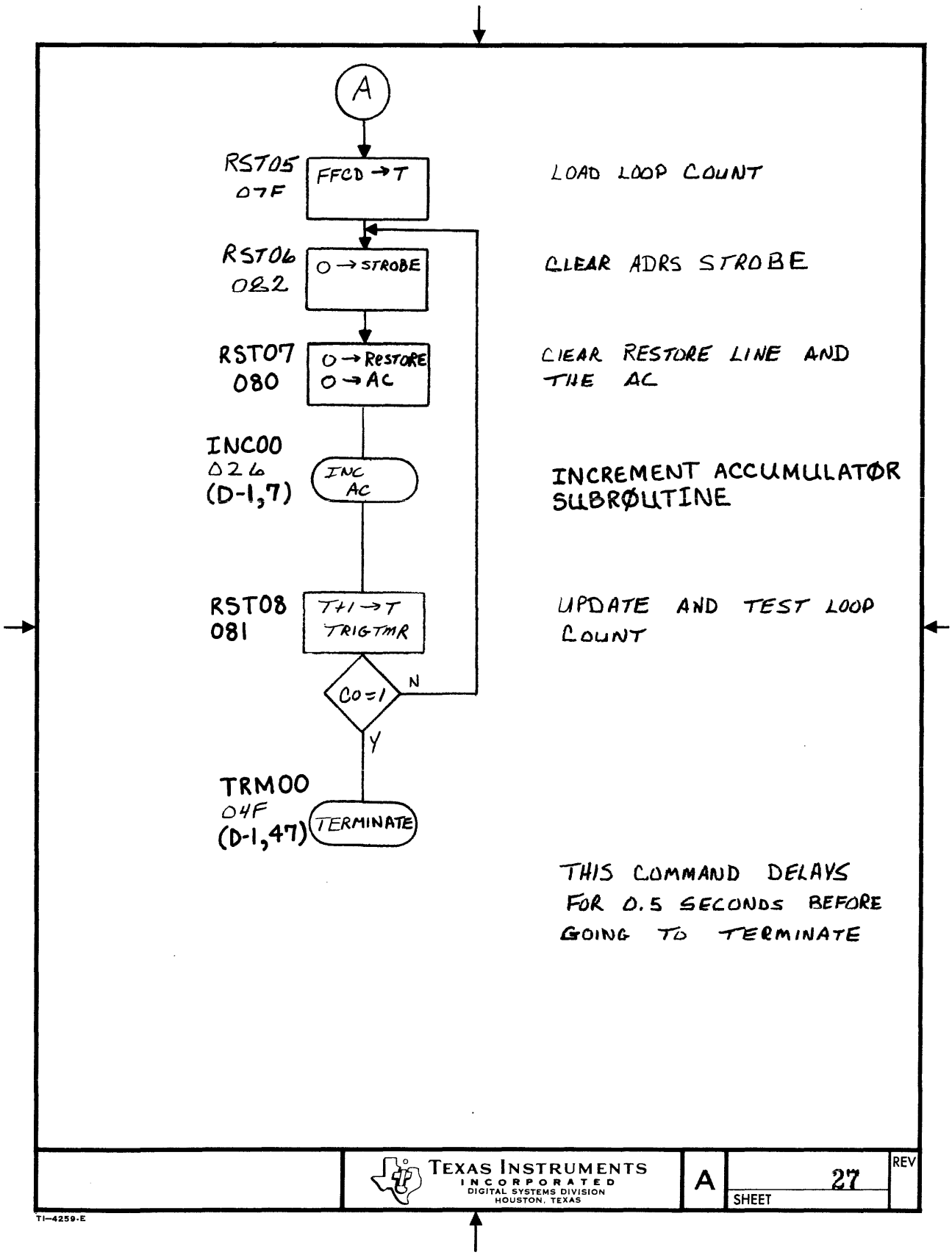


Figure D-1. Microcode Flowcharts (Sheet 27 of 101)

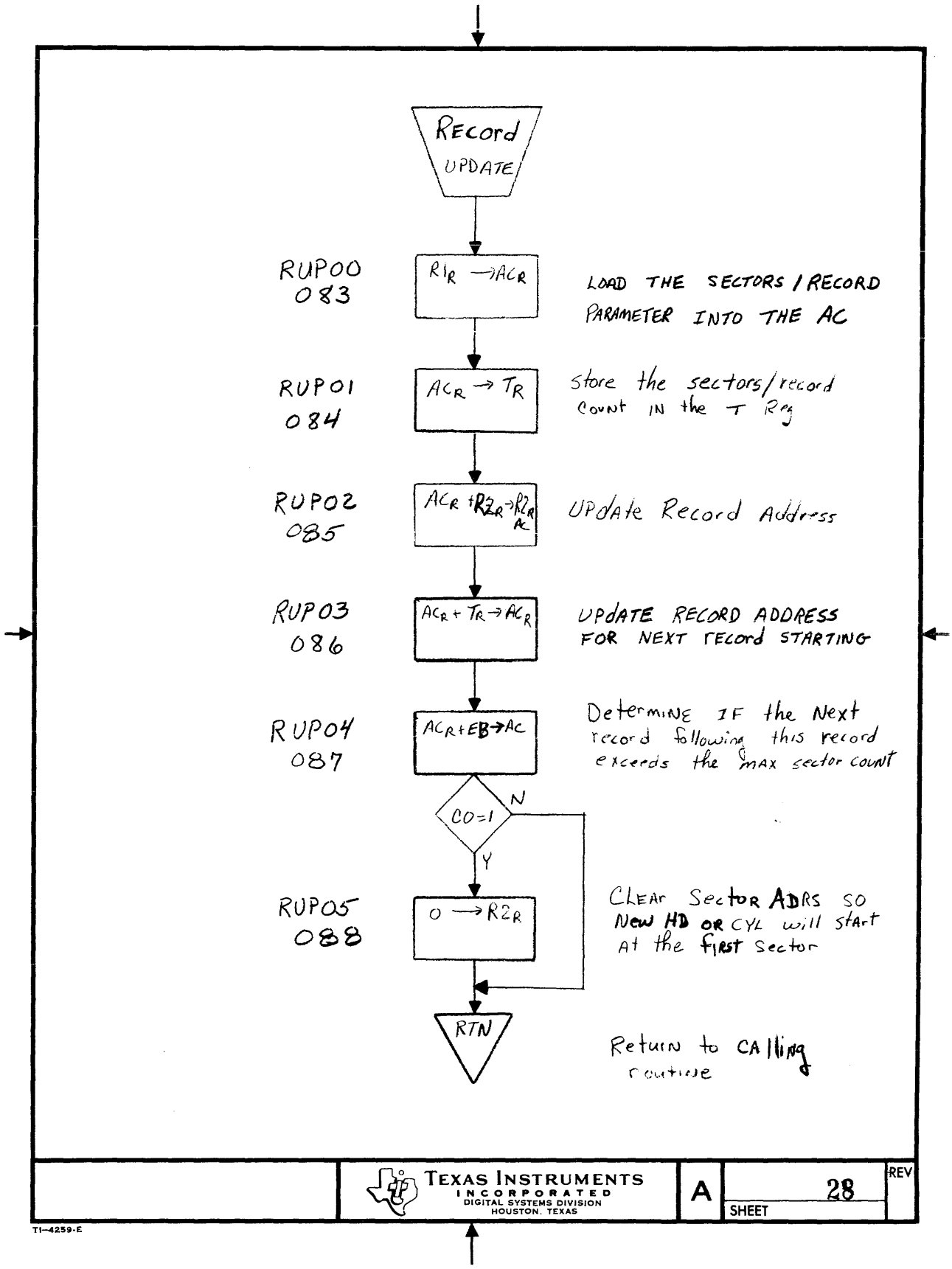


Figure D-1. Microcode Flowcharts (Sheet 28 of 101)

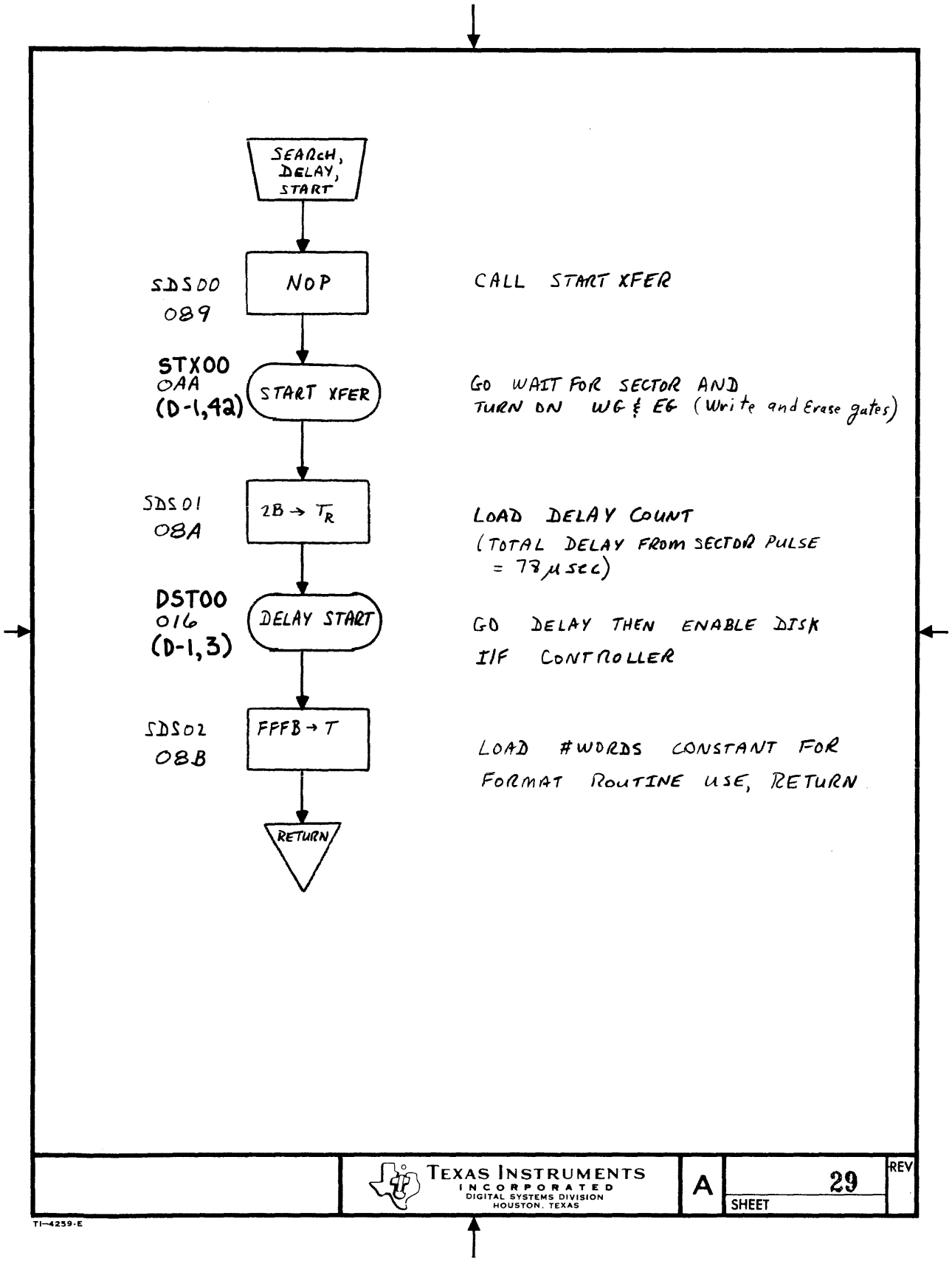


Figure D-1. Microcode Flowcharts (Sheet 29 of 101)

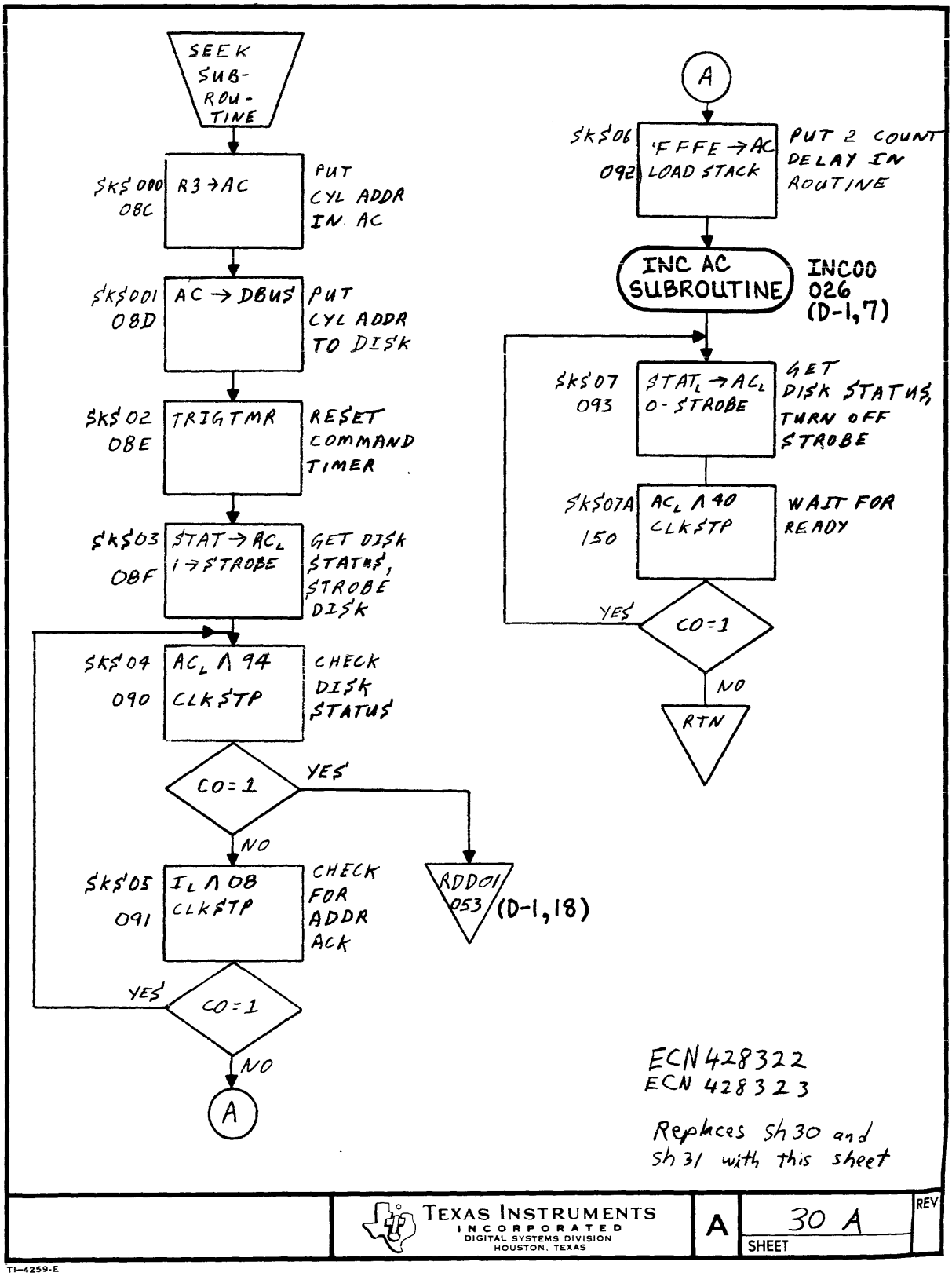


Figure D-1. Microcode Flowcharts (Sheet 30 of 101)

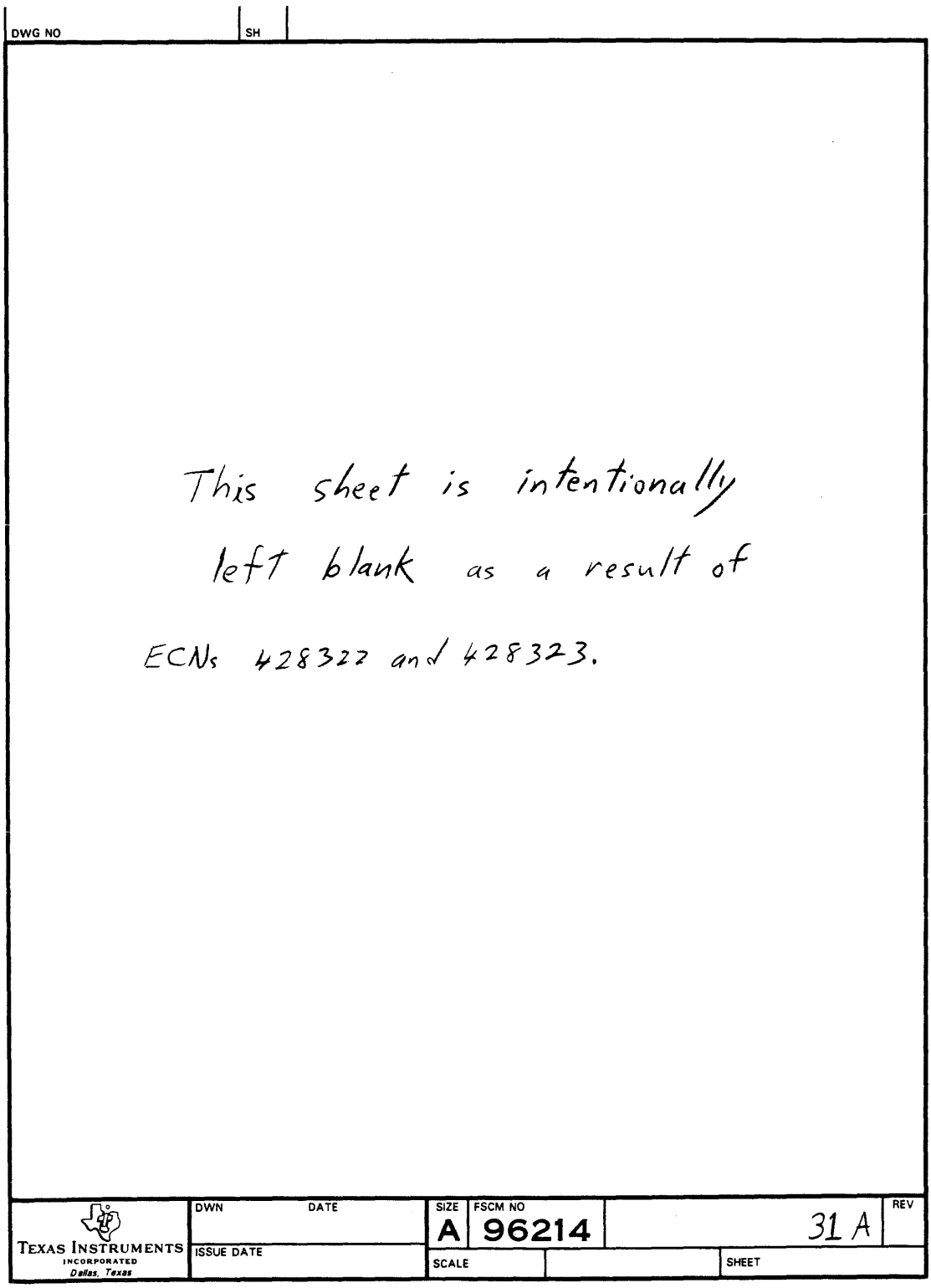


Figure D-1. Microcode Flowcharts (Sheet 31 of 101)

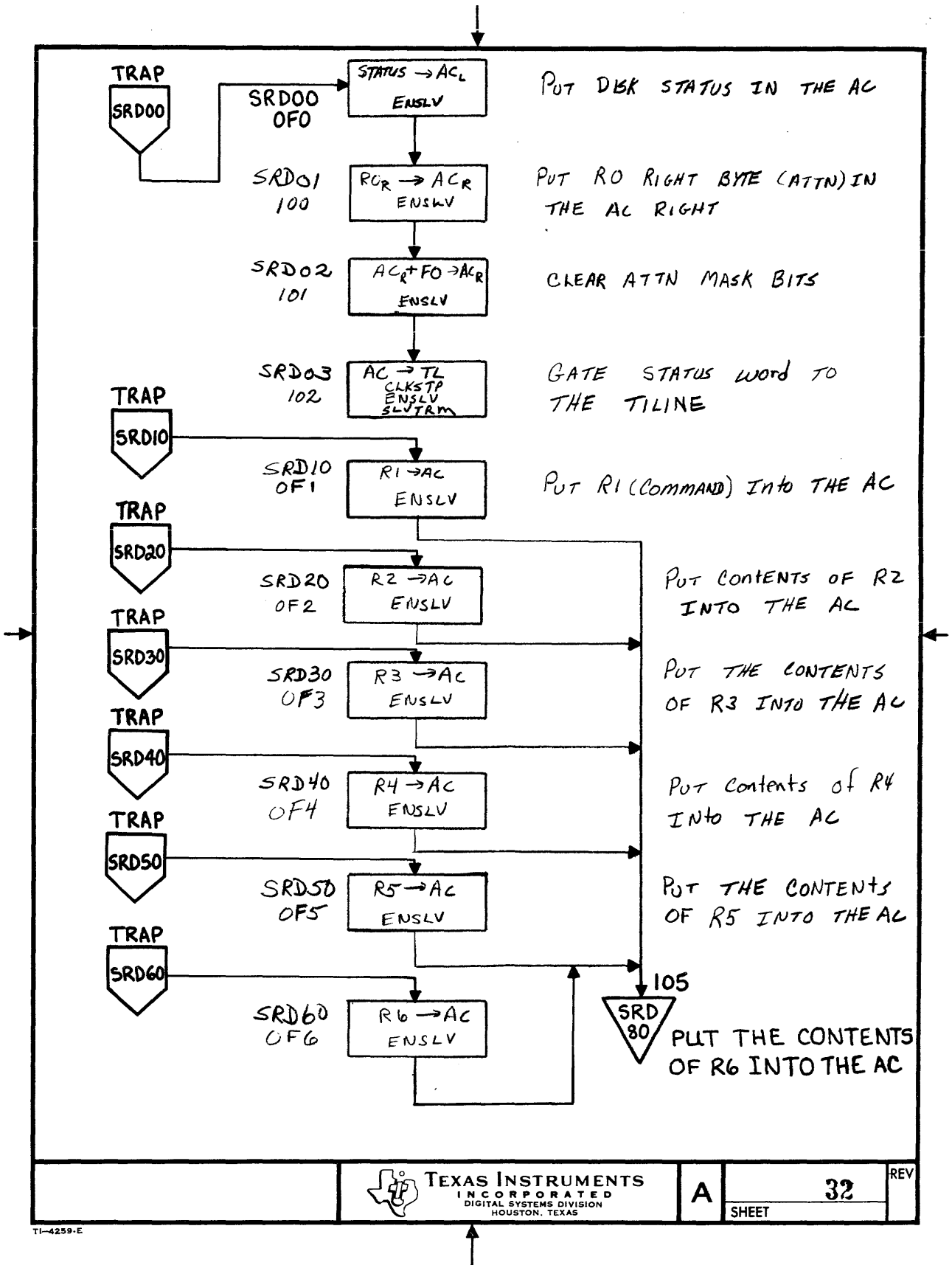


Figure D-1. Microcode Flowcharts (Sheet 32 of 101)

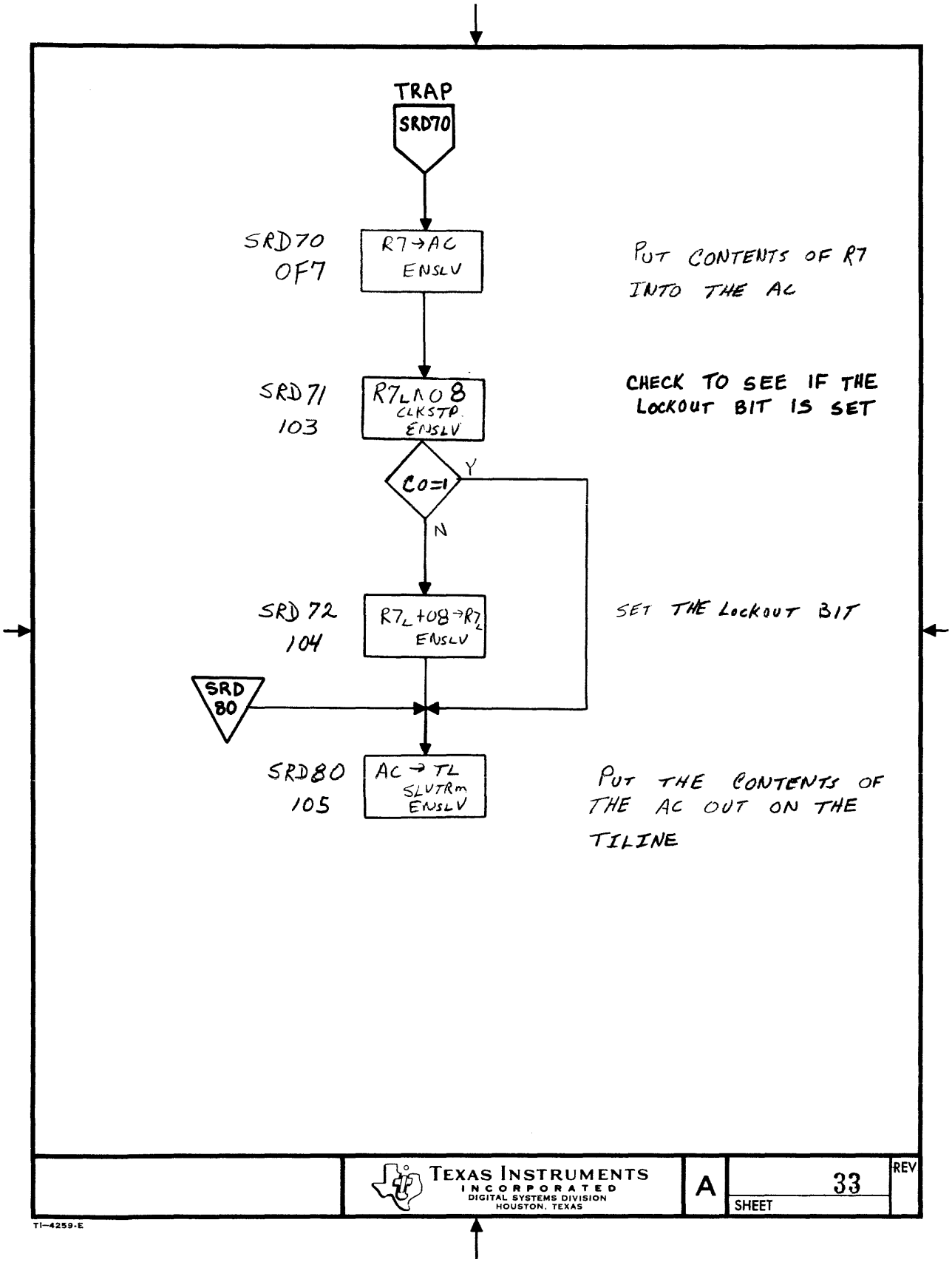


Figure D-1. Microcode Flowcharts (Sheet 33 of 101)

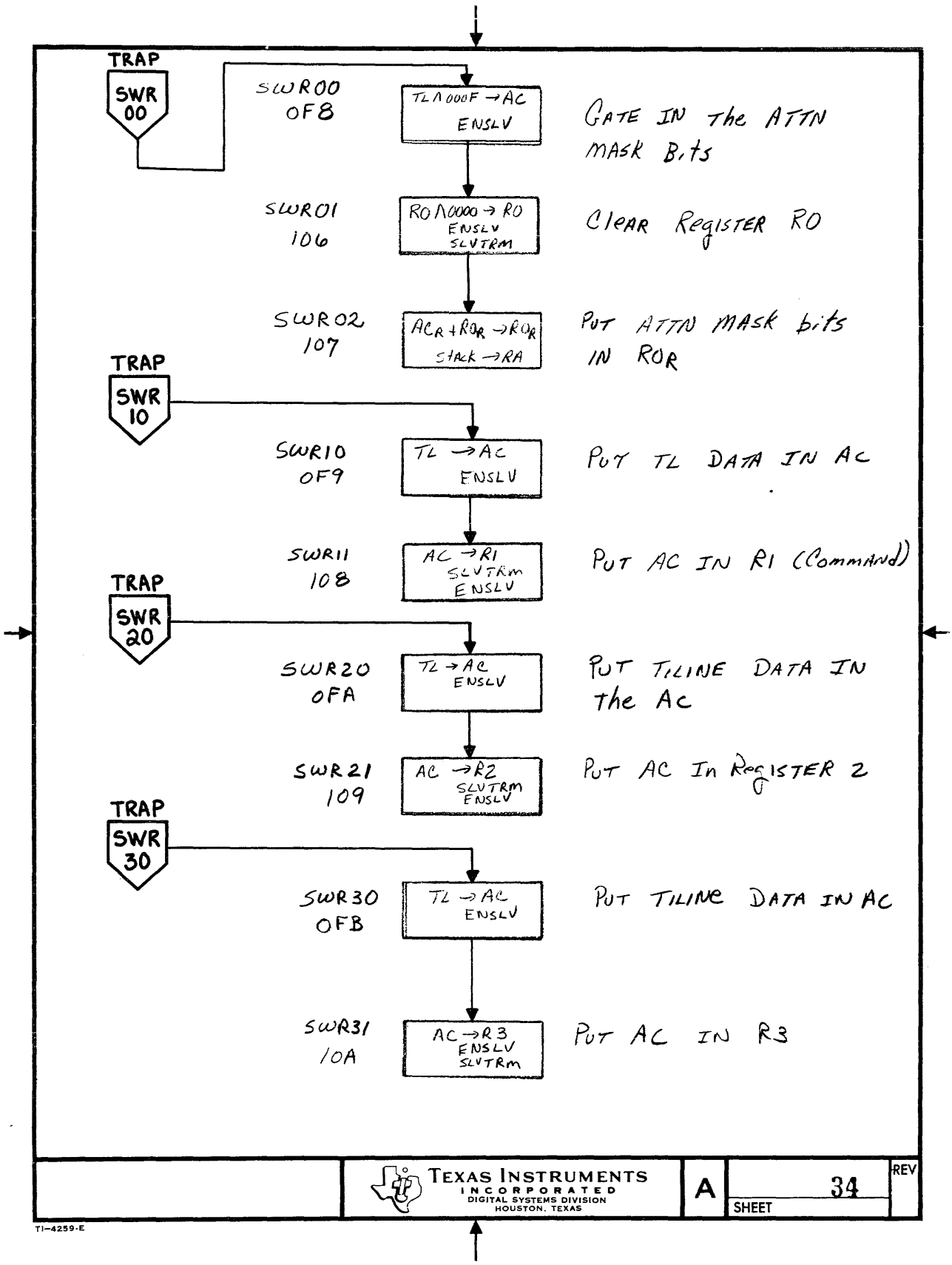


Figure D-1. Microcode Flowcharts (Sheet 34 of 101)

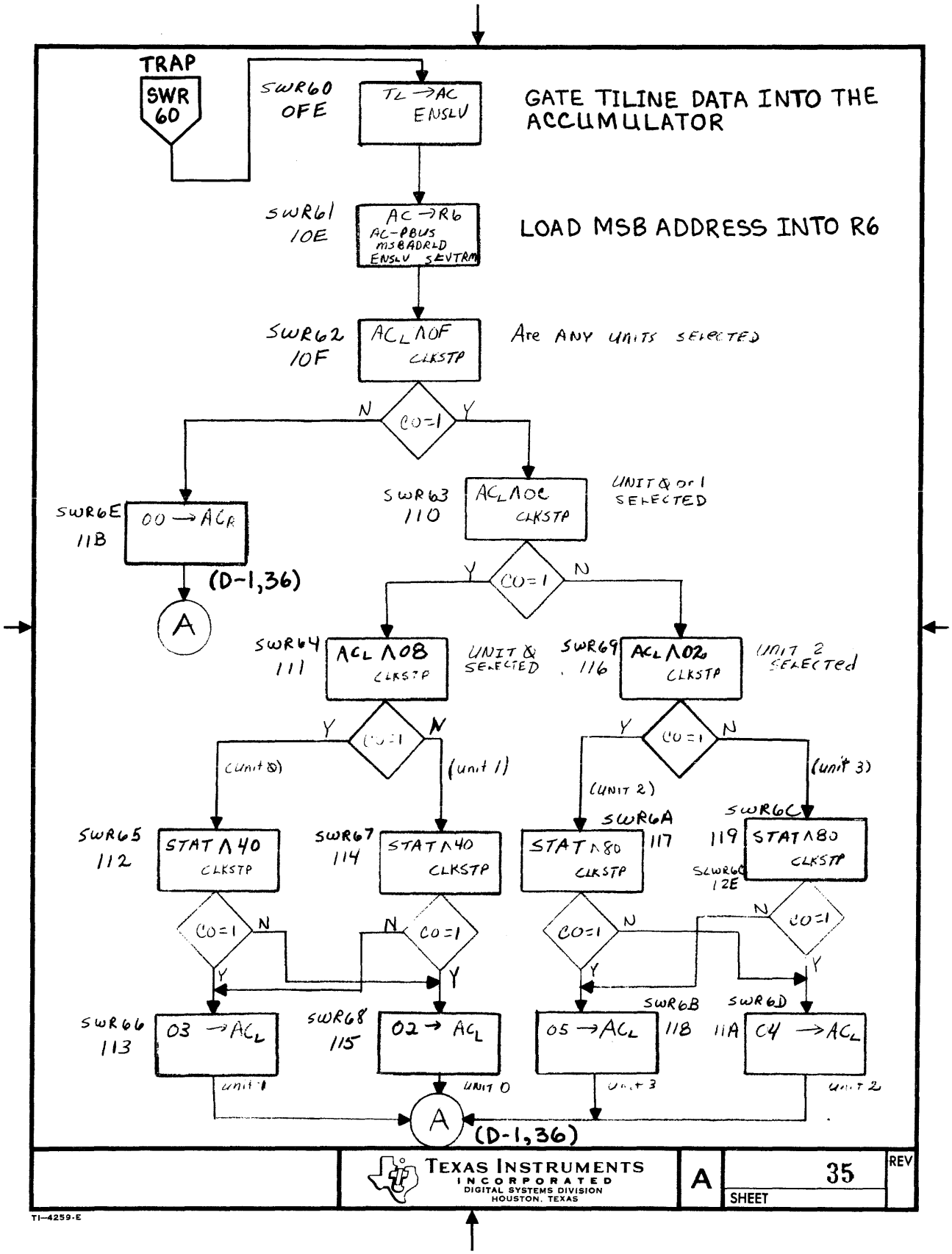


Figure D-1. Microcode Flowcharts (Sheet 35 of 101)

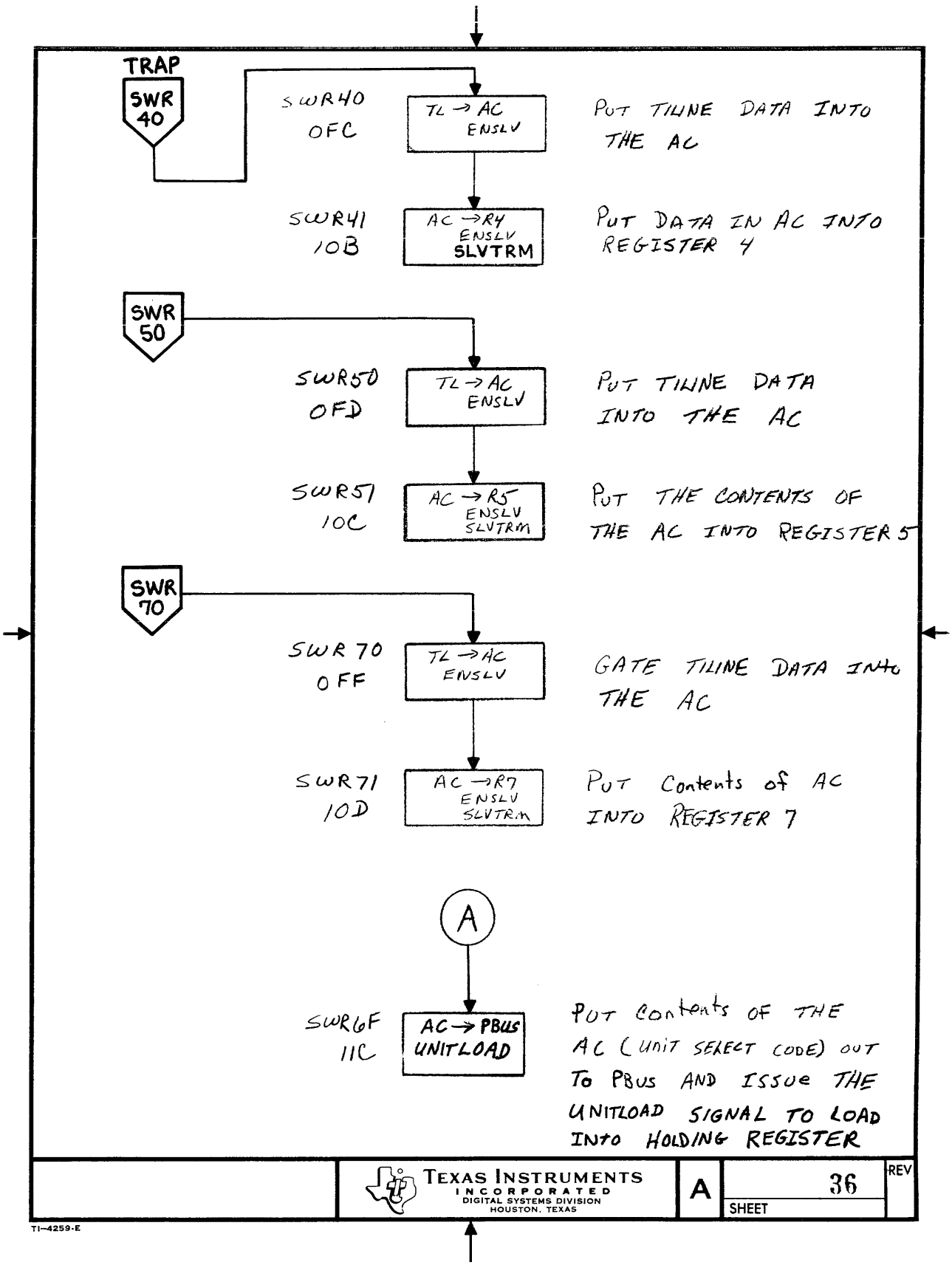


Figure D-1. Microcode Flowcharts (Sheet 36 of 101)

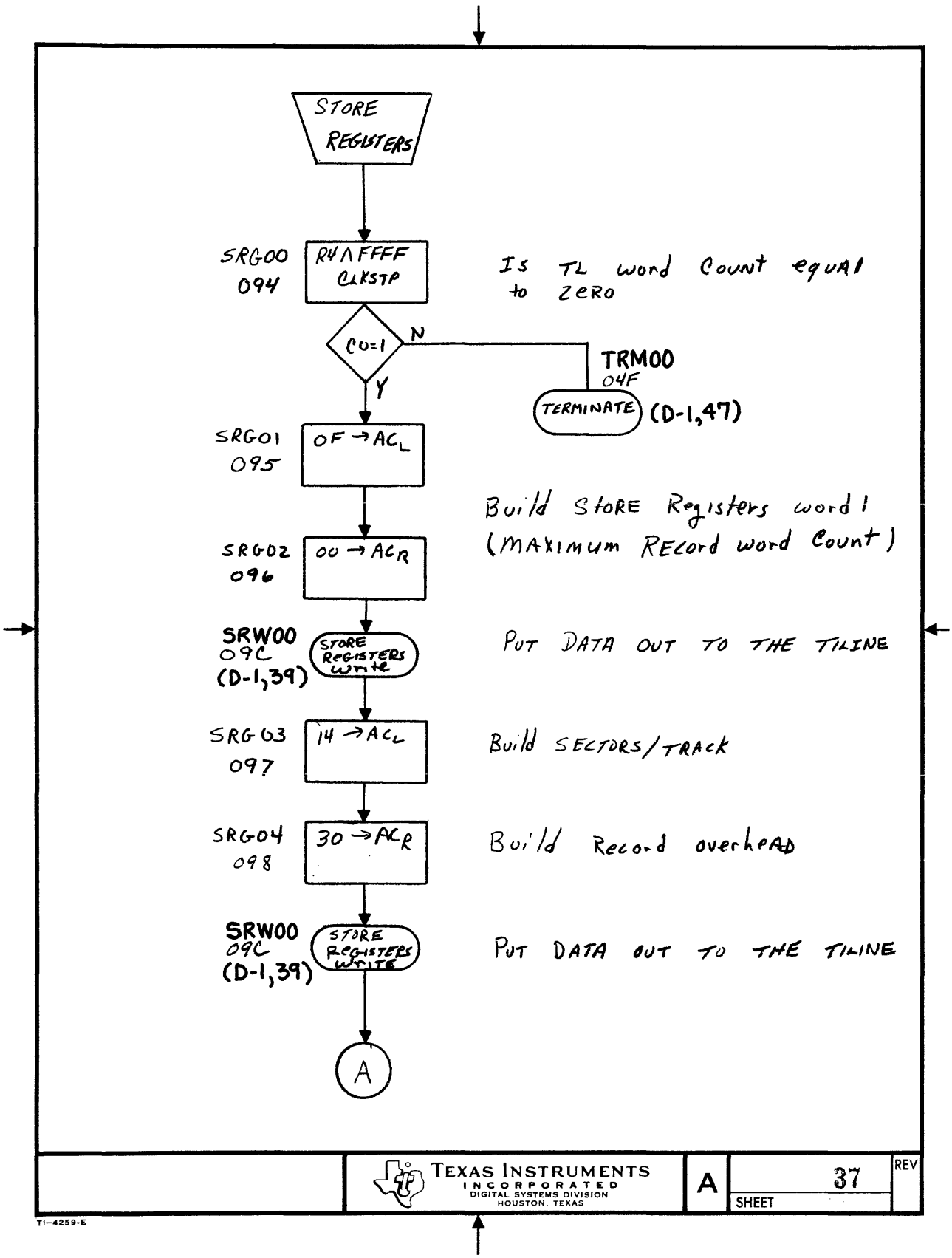


Figure D-1. Microcode Flowcharts (Sheet 37 of 101)

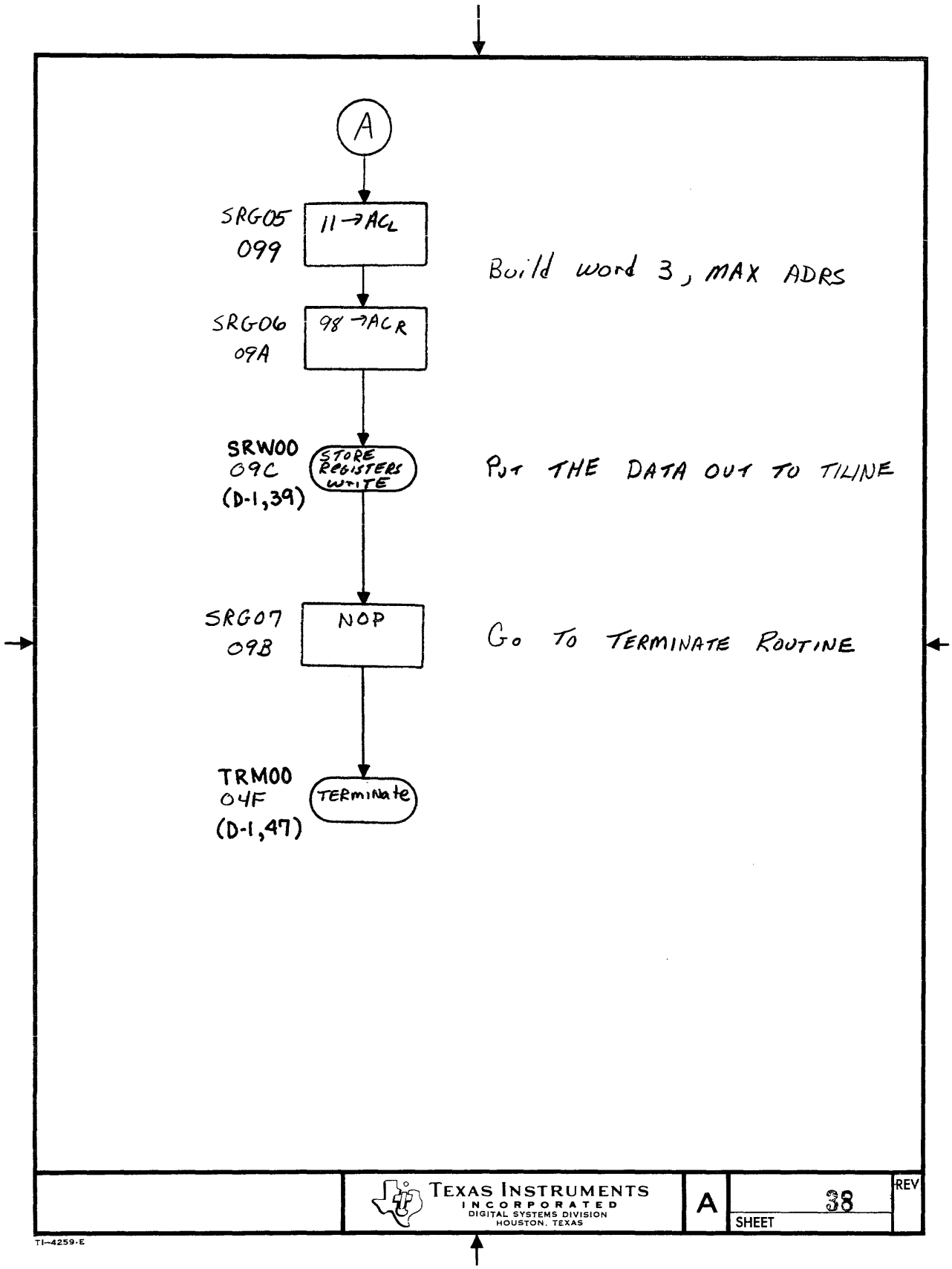


Figure D-1. Microcode Flowcharts (Sheet 38 of 101)

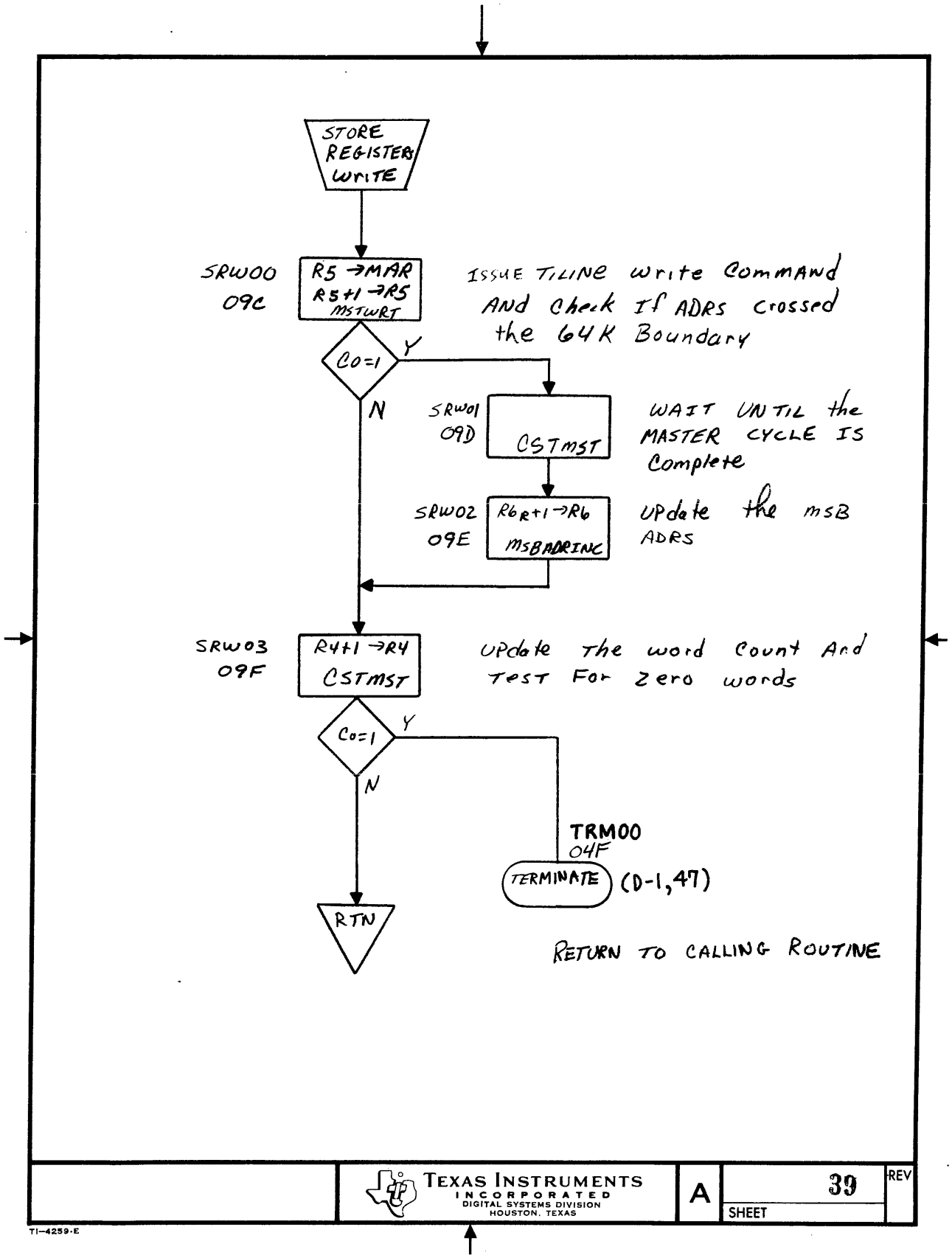


Figure D-1. Microcode Flowcharts (Sheet 39 of 101)

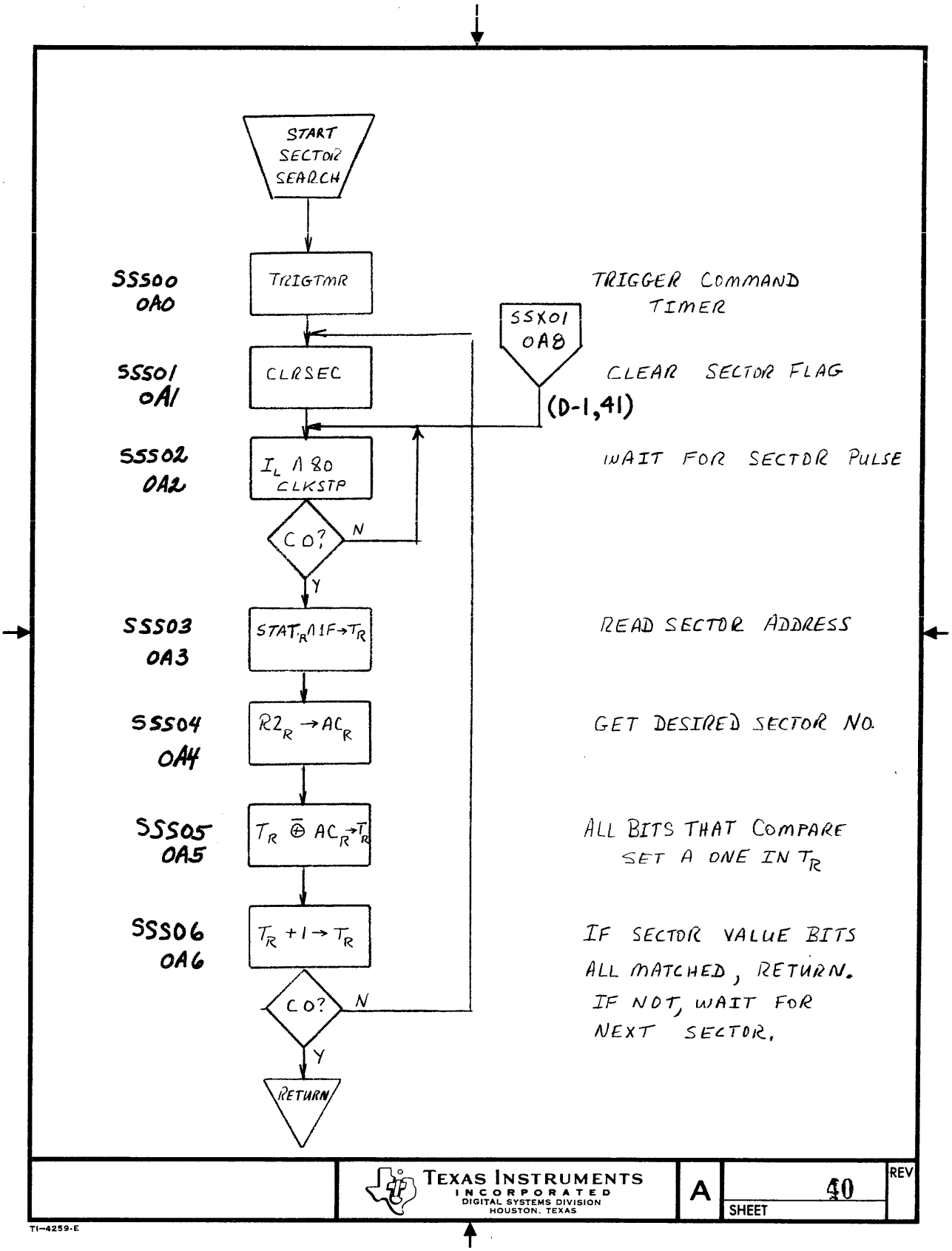


Figure D-1. Microcode Flowcharts (Sheet 40 of 101)

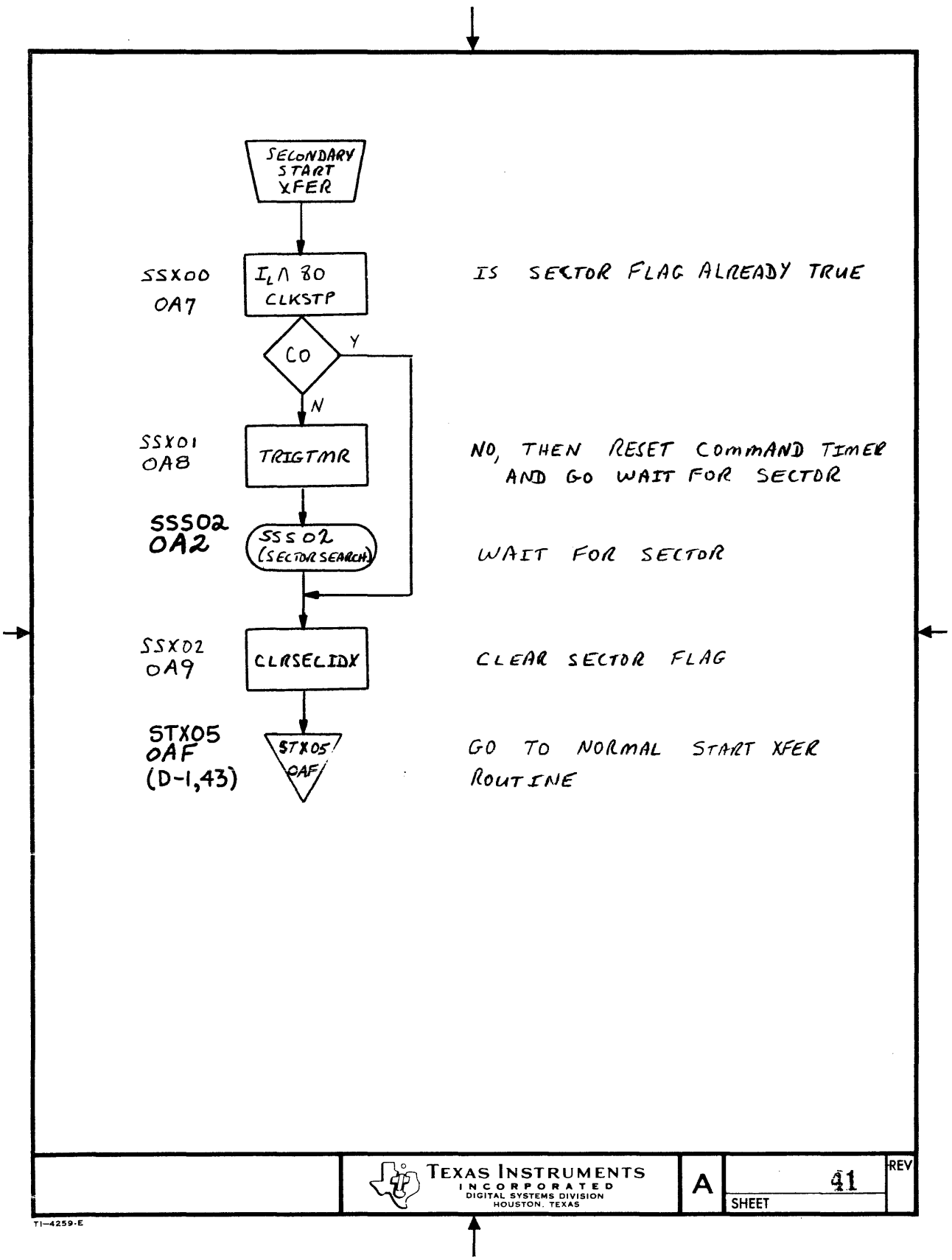


Figure D-1. Microcode Flowcharts (Sheet 41 of 101)

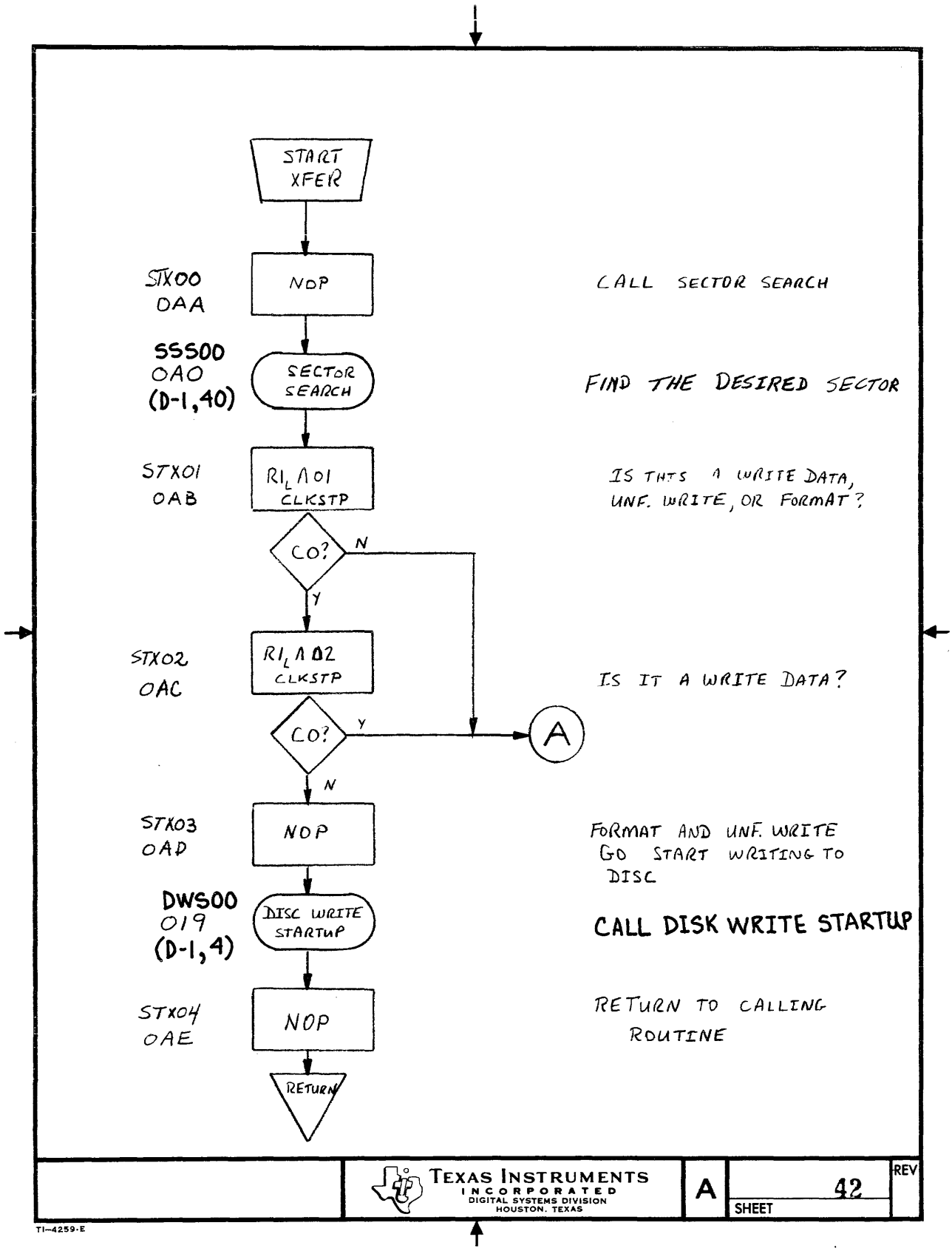


Figure D-1. Microcode Flowcharts (Sheet 42 of 101)

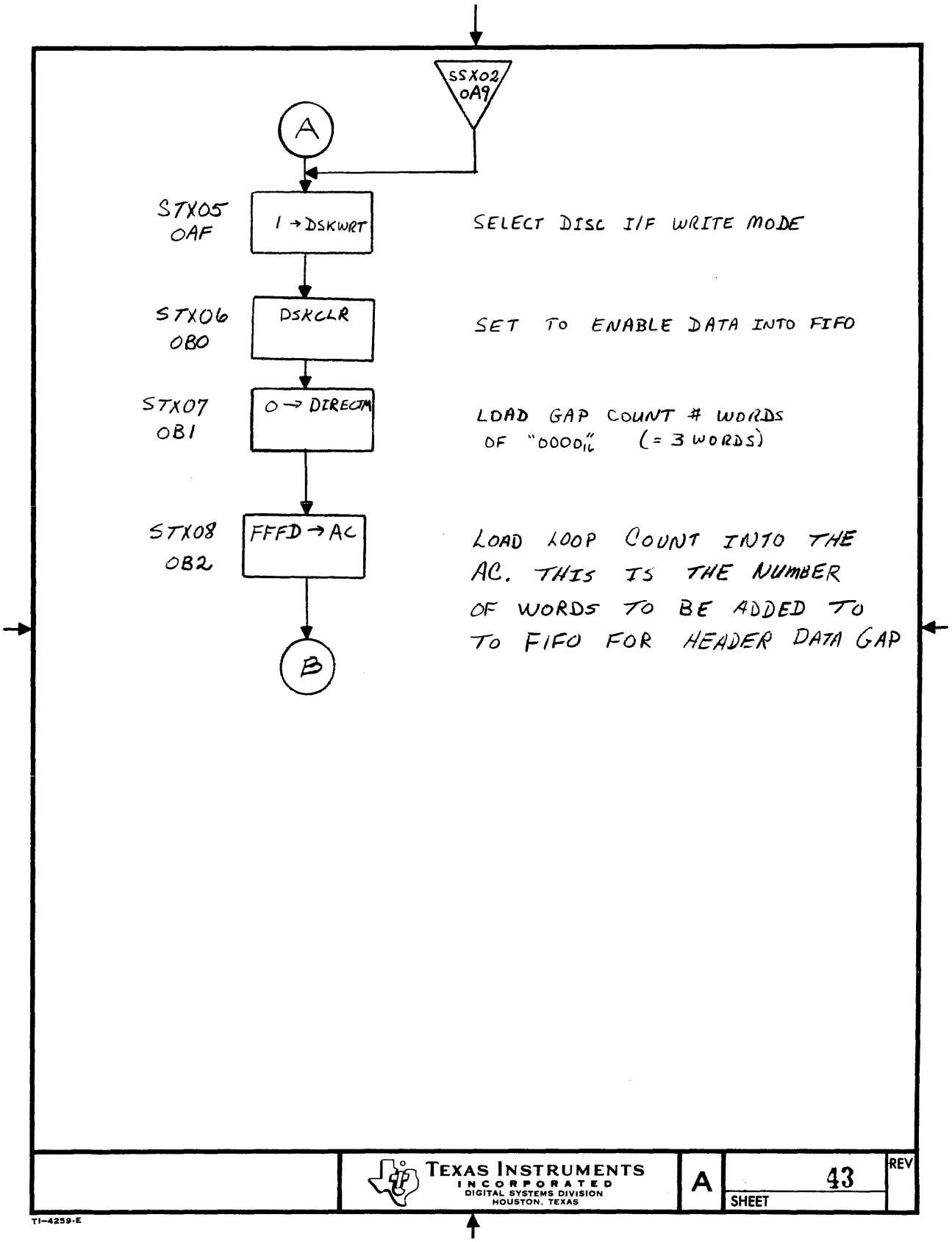


Figure D-1. Microcode Flowcharts (Sheet 43 of 101)

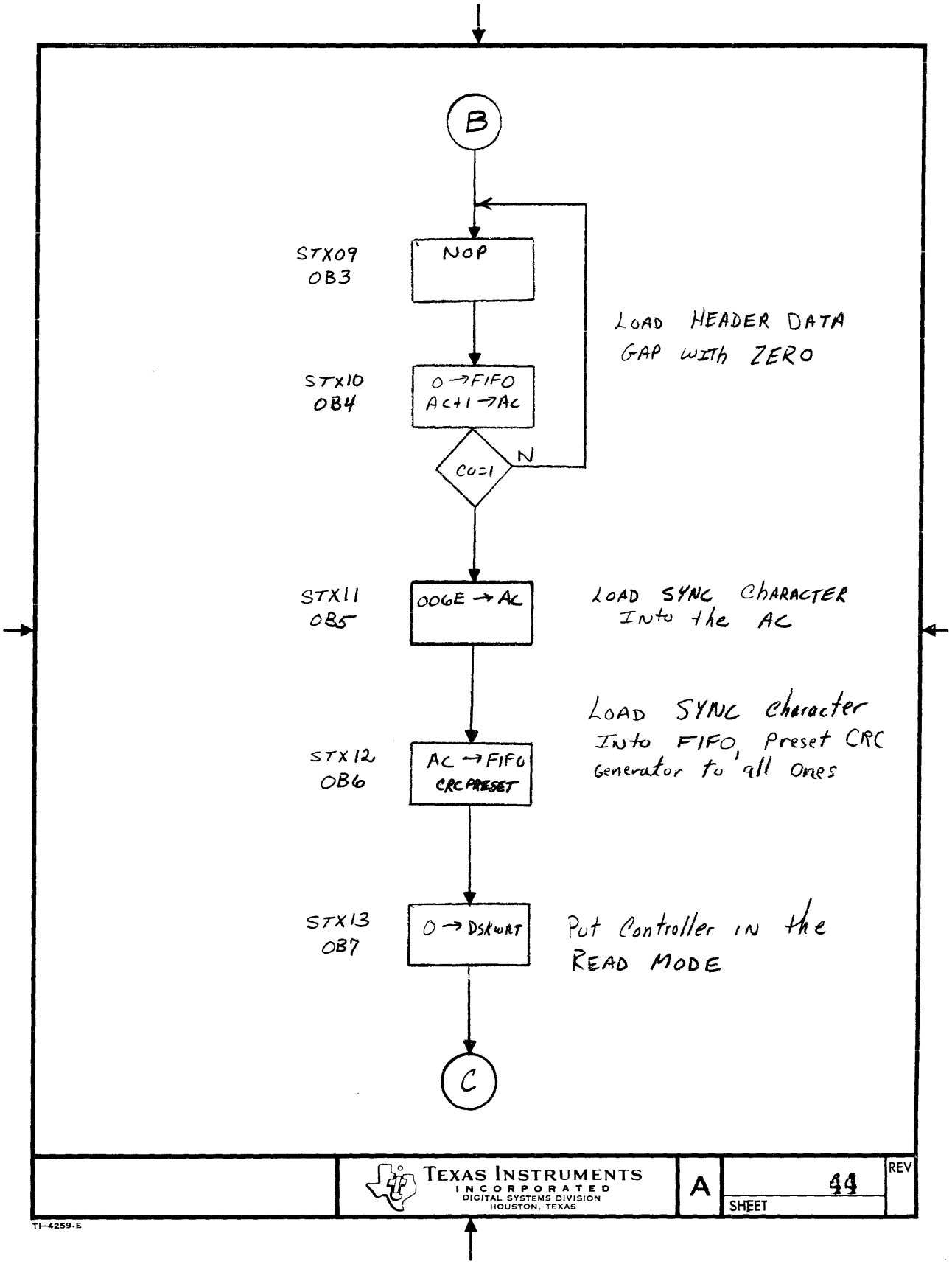


Figure D-1. Microcode Flowcharts (Sheet 44 of 101)

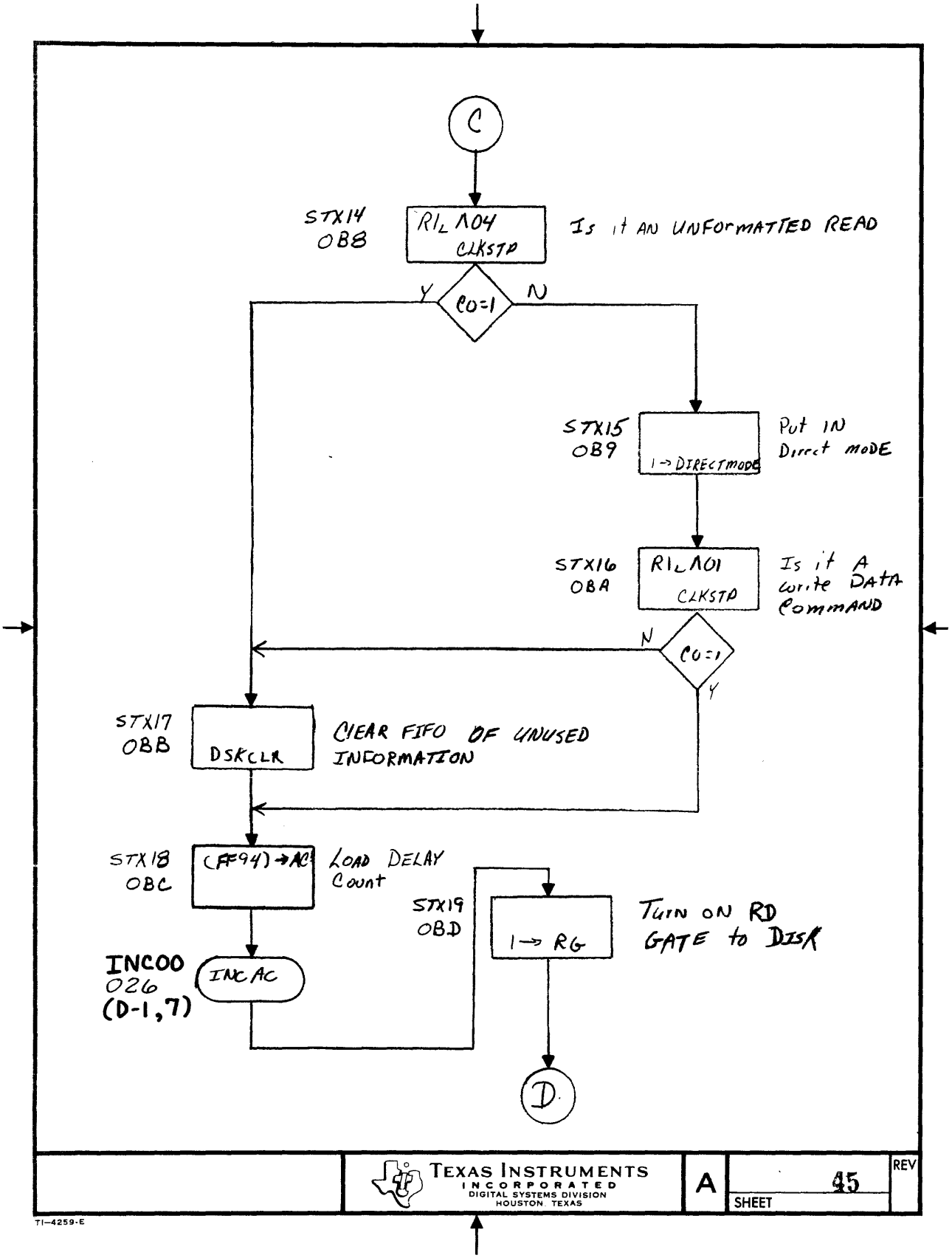


Figure D-1. Microcode Flowcharts (Sheet 45 of 101)

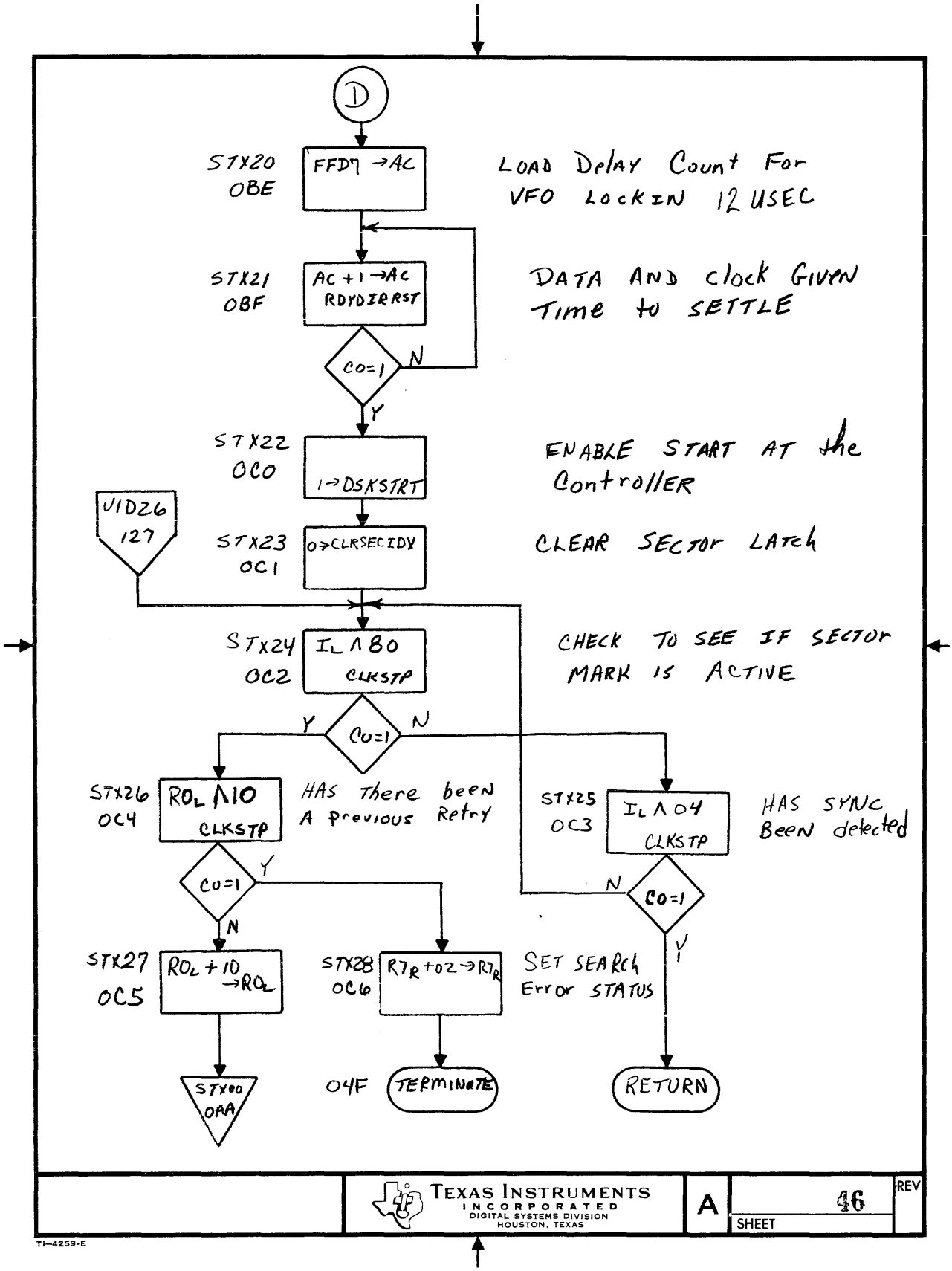


Figure D-1. Microcode Flowcharts (Sheet 46 of 101)

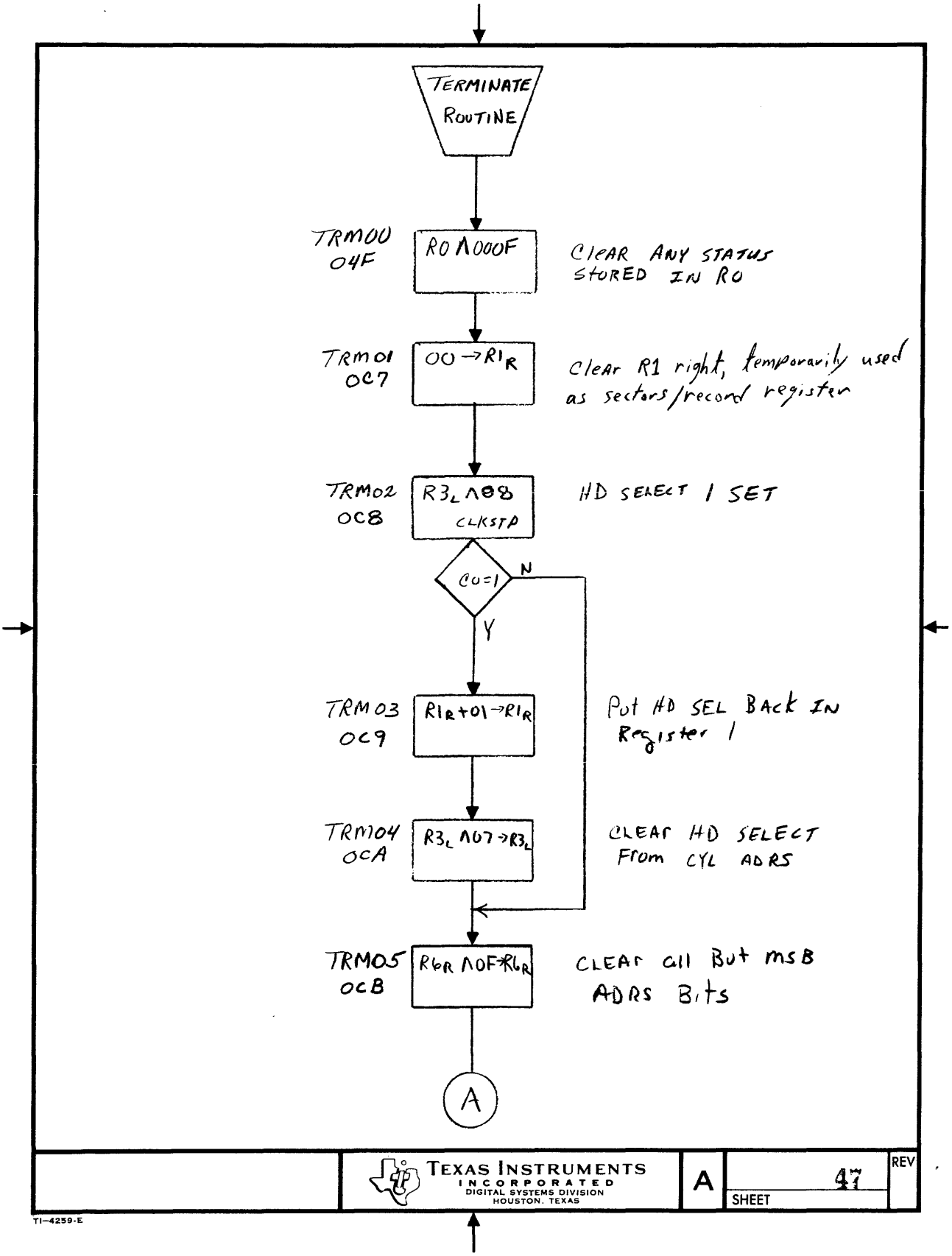


Figure D-1. Microcode Flowcharts (Sheet 47 of 101)

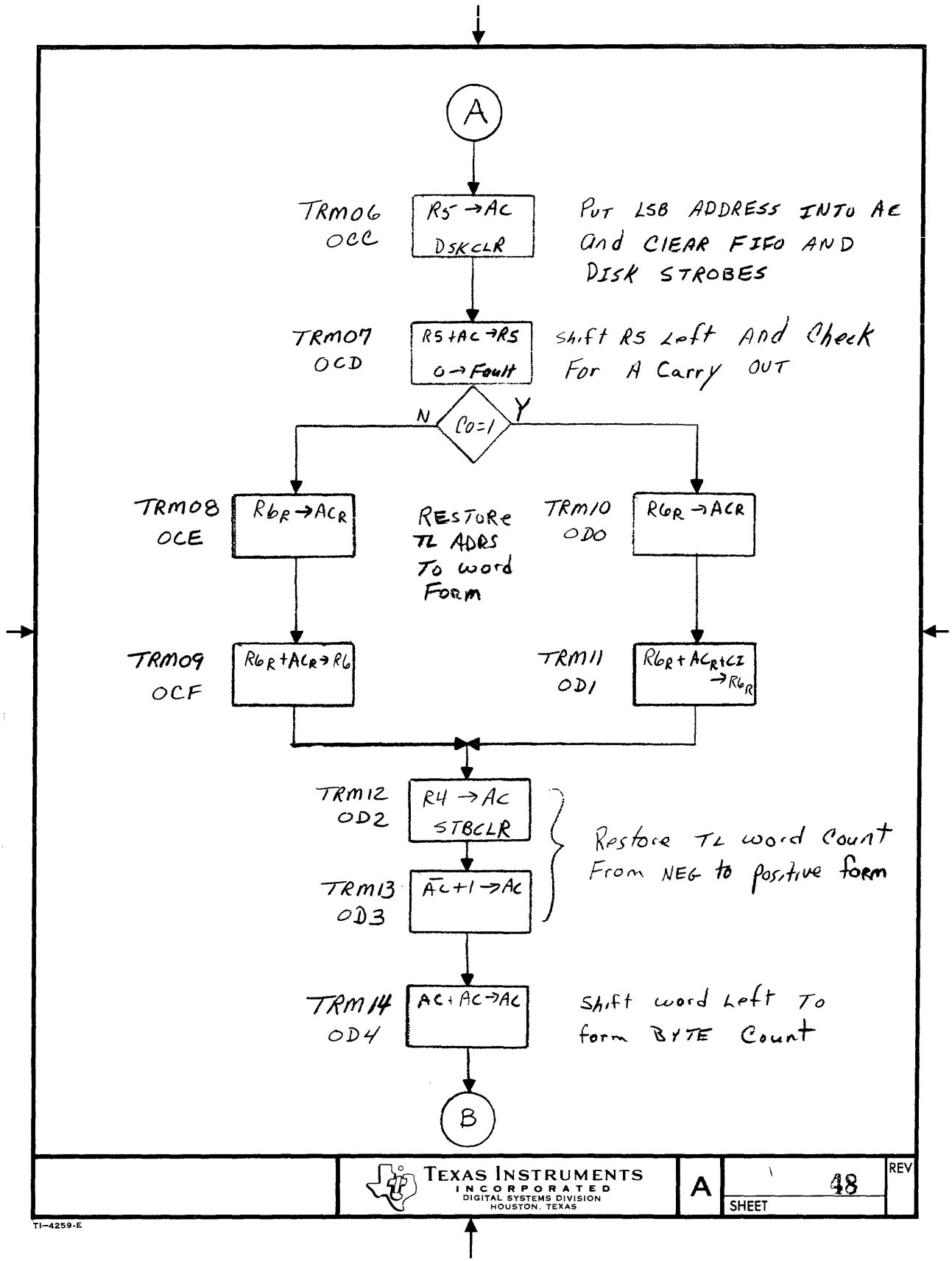


Figure D-1. Microcode Flowcharts (Sheet 48 of 101)

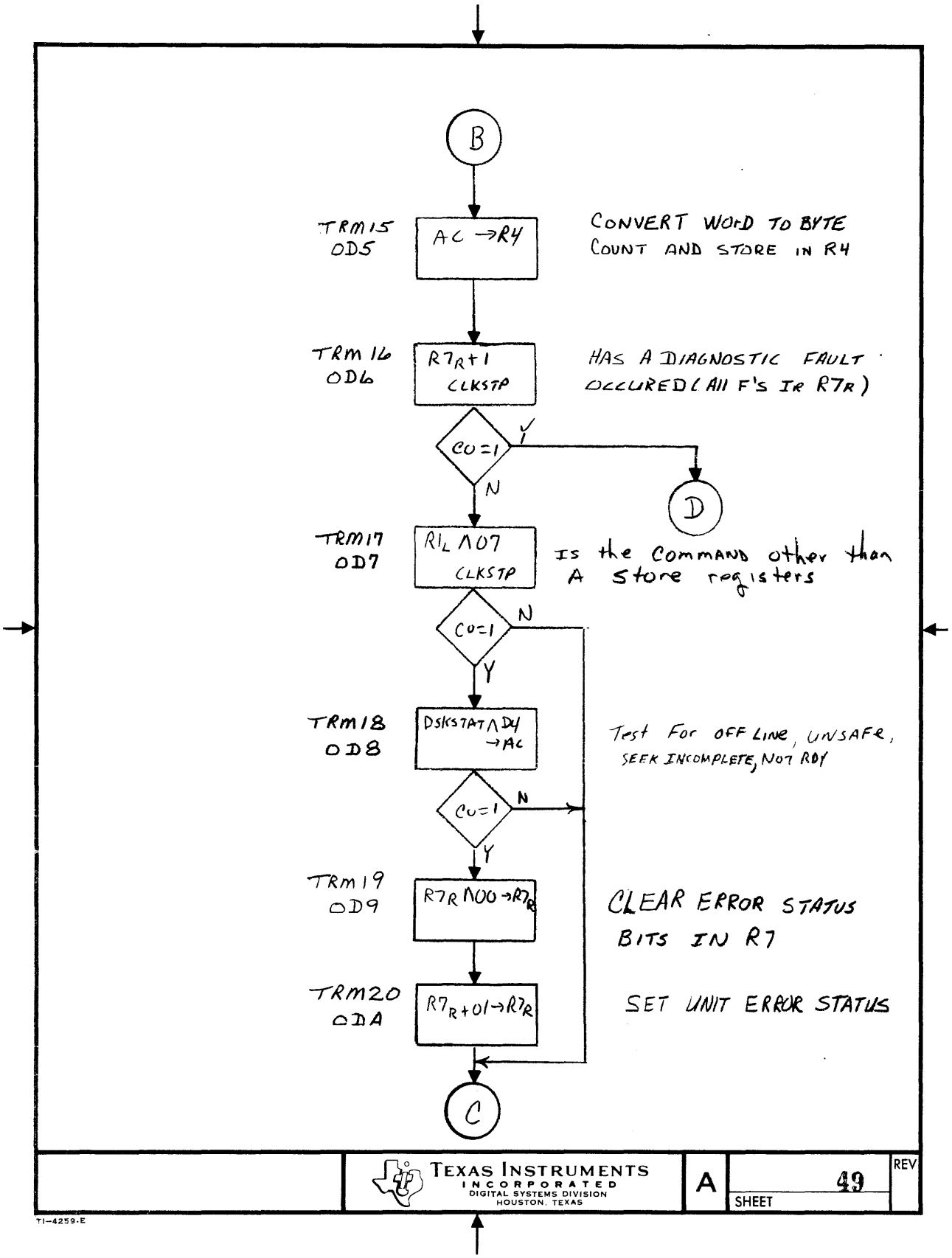


Figure D-1. Microcode Flowcharts (Sheet 49 of 101)

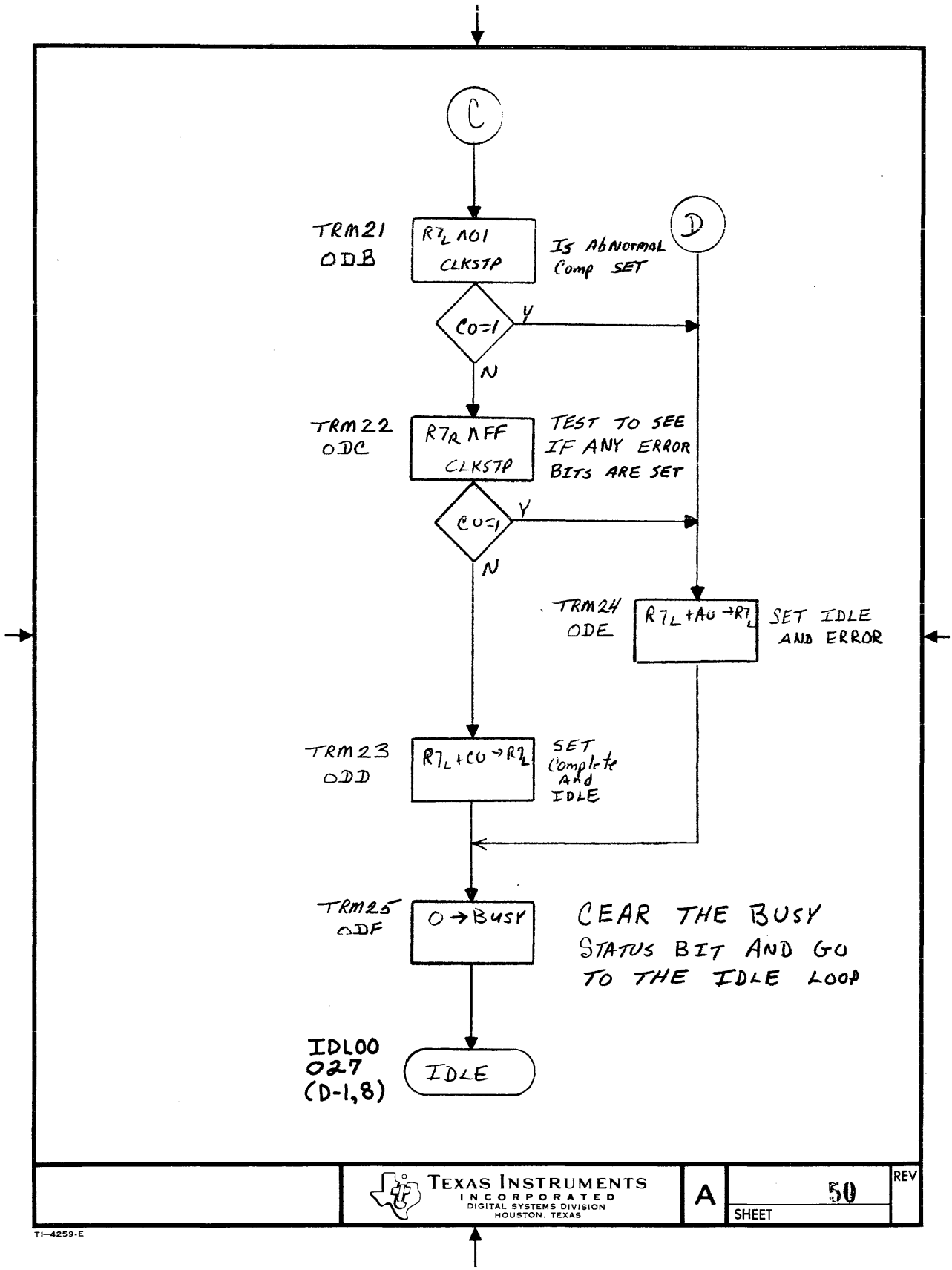


Figure D-1. Microcode Flowcharts (Sheet 50 of 101)

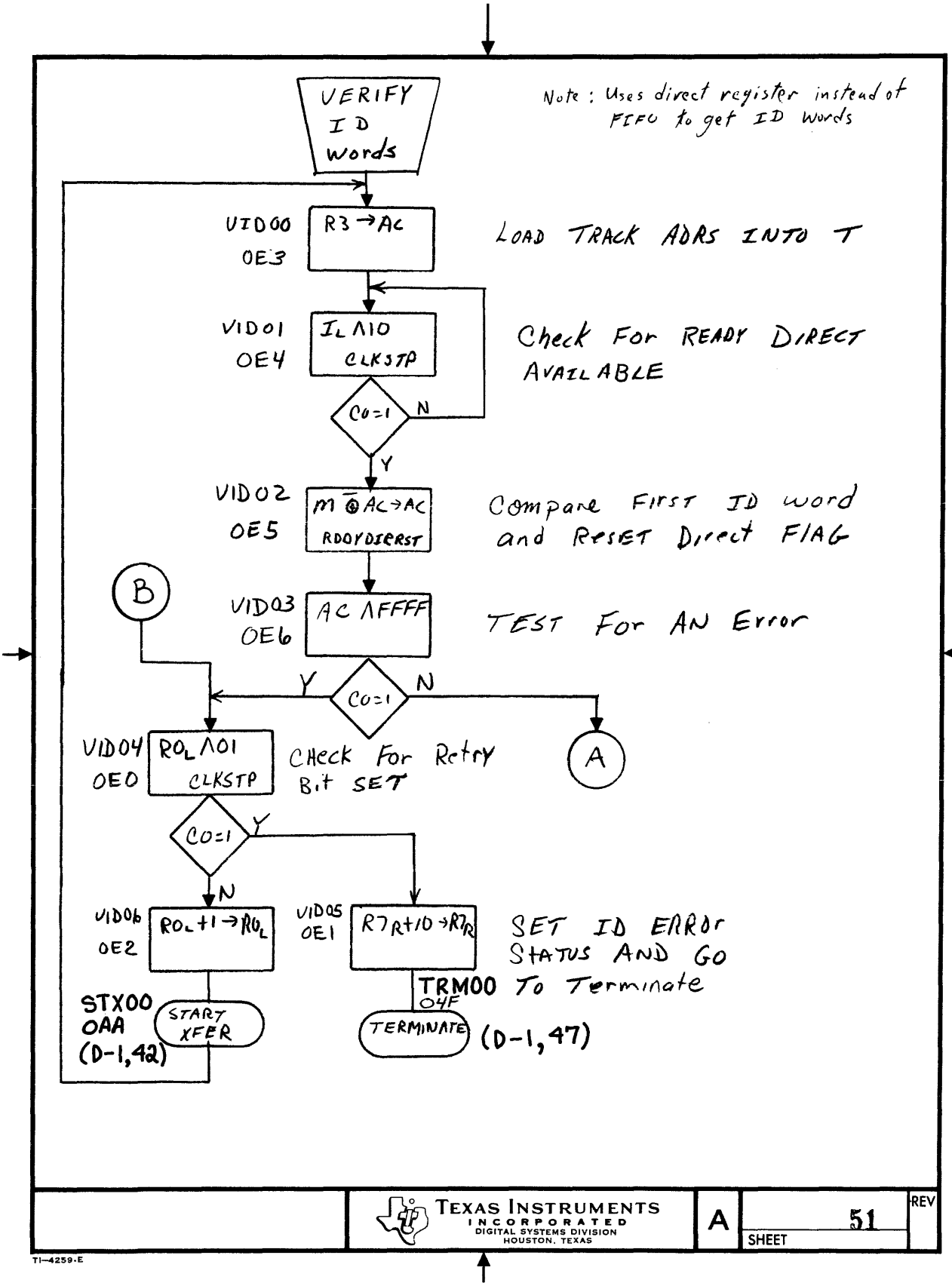


Figure D-1. Microcode Flowcharts (Sheet 51 of 101)

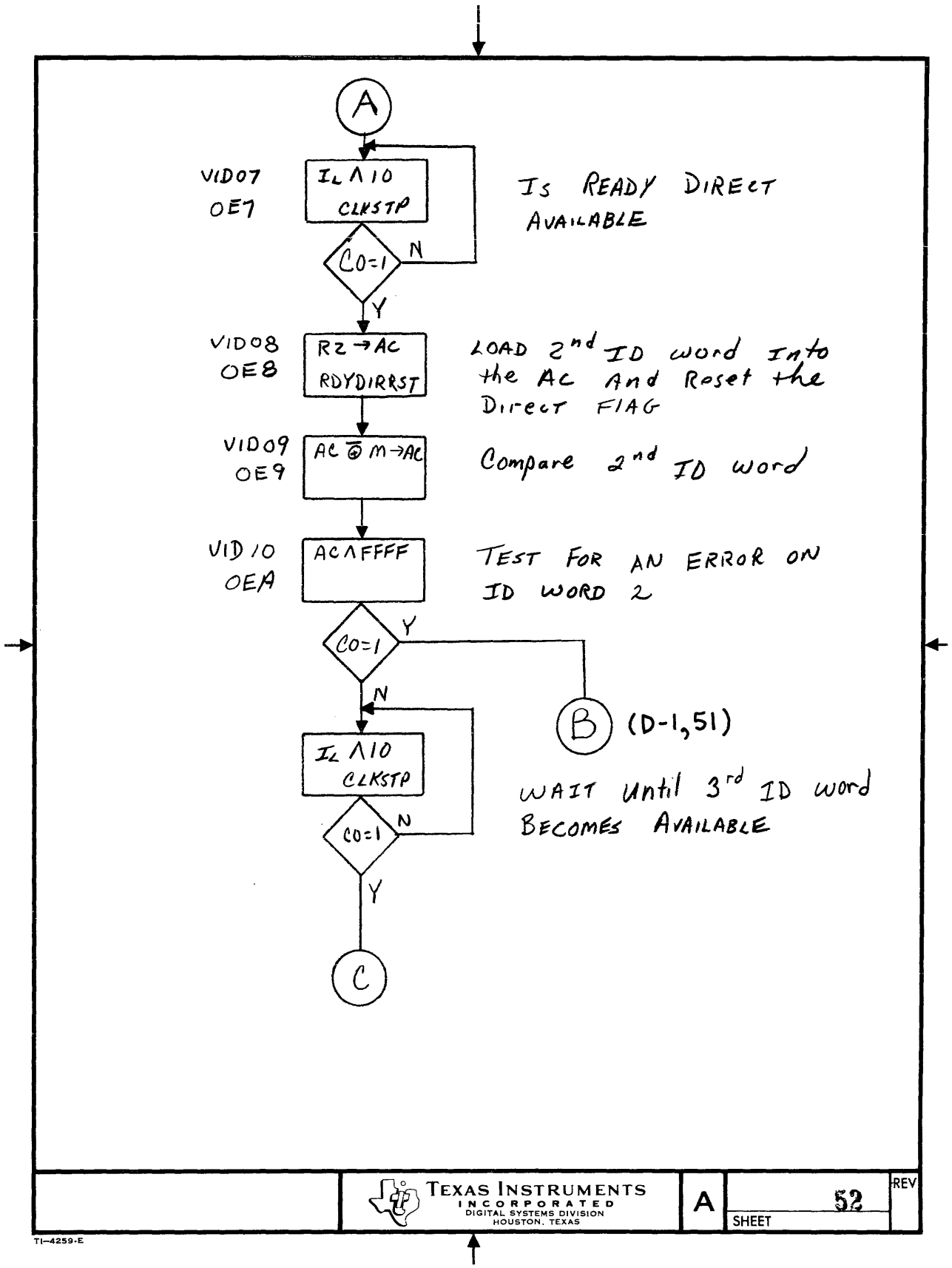


Figure D-1. Microcode Flowcharts (Sheet 52 of 101)

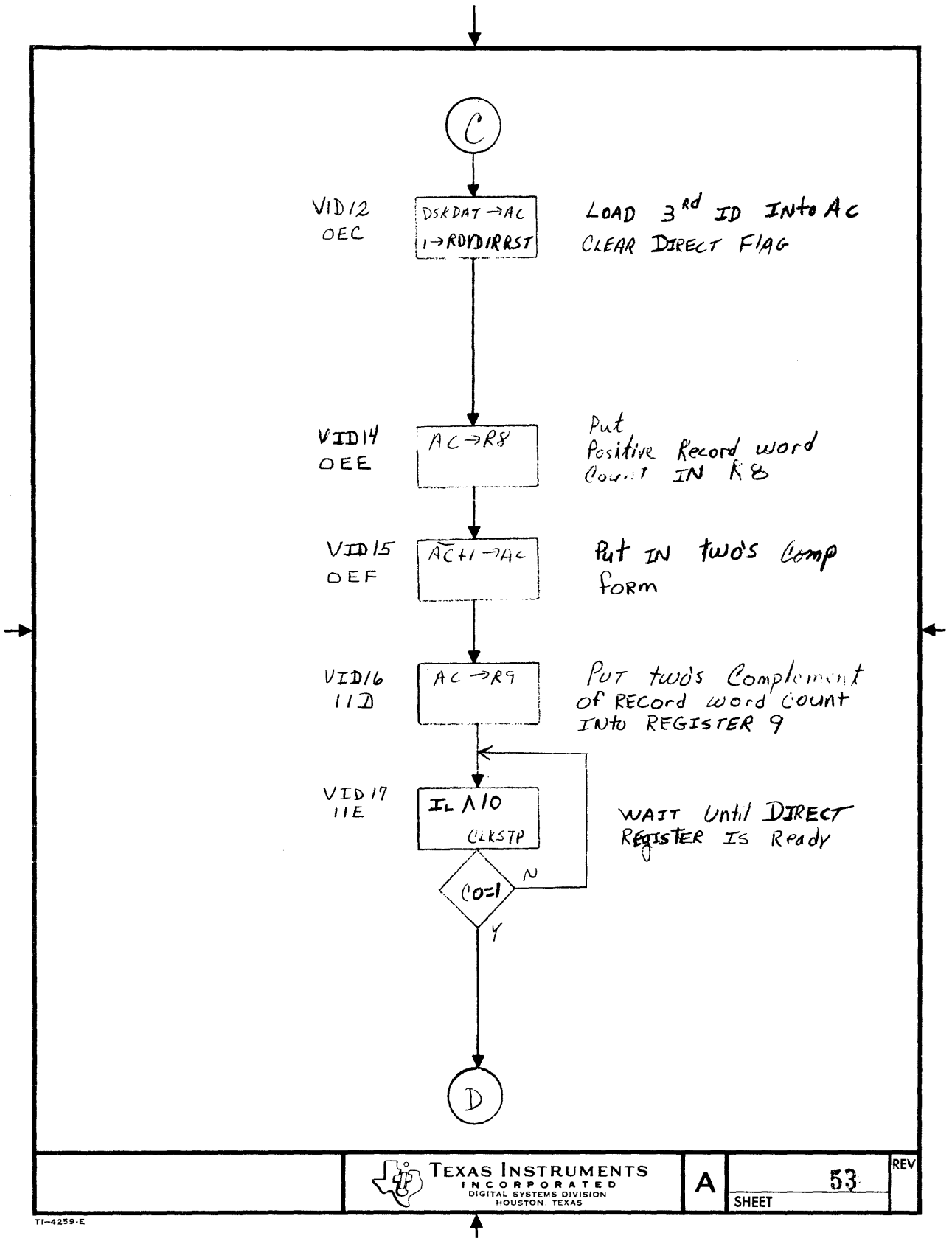


Figure D-1. Microcode Flowcharts (Sheet 53 of 101)

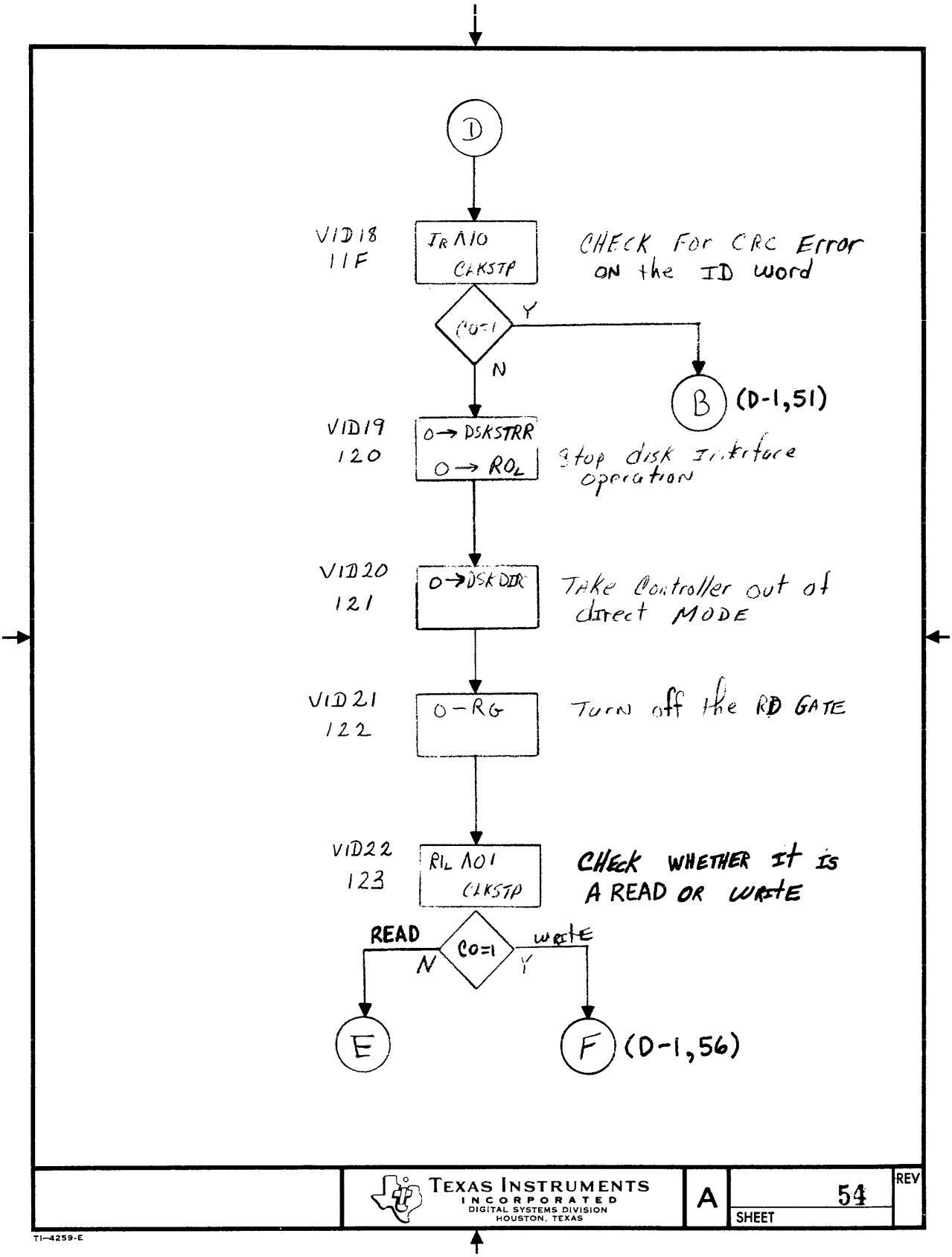


Figure D-1. Microcode Flowcharts (Sheet 54 of 101)

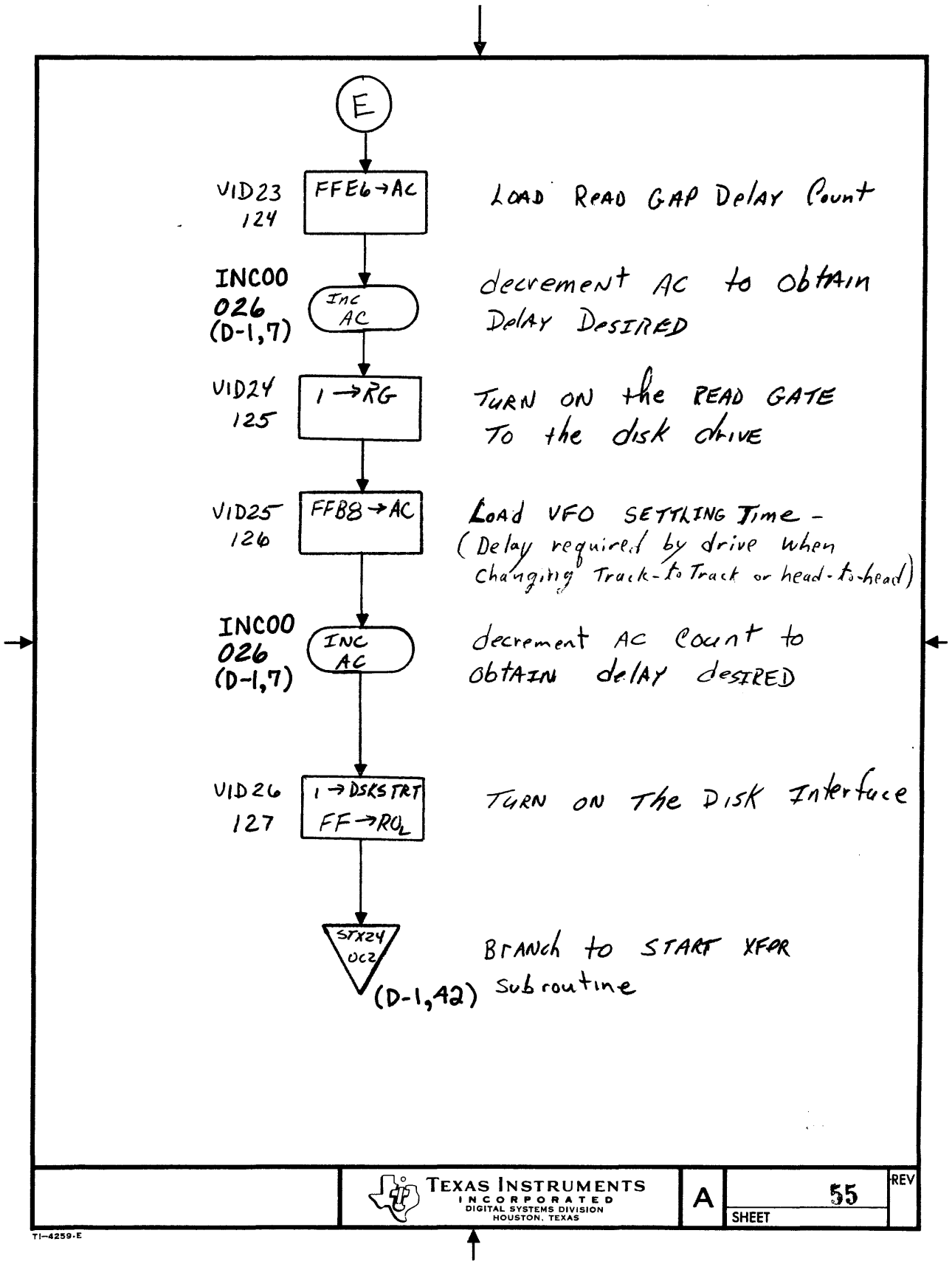


Figure D-1. Microcode Flowcharts (Sheet 55 of 101)

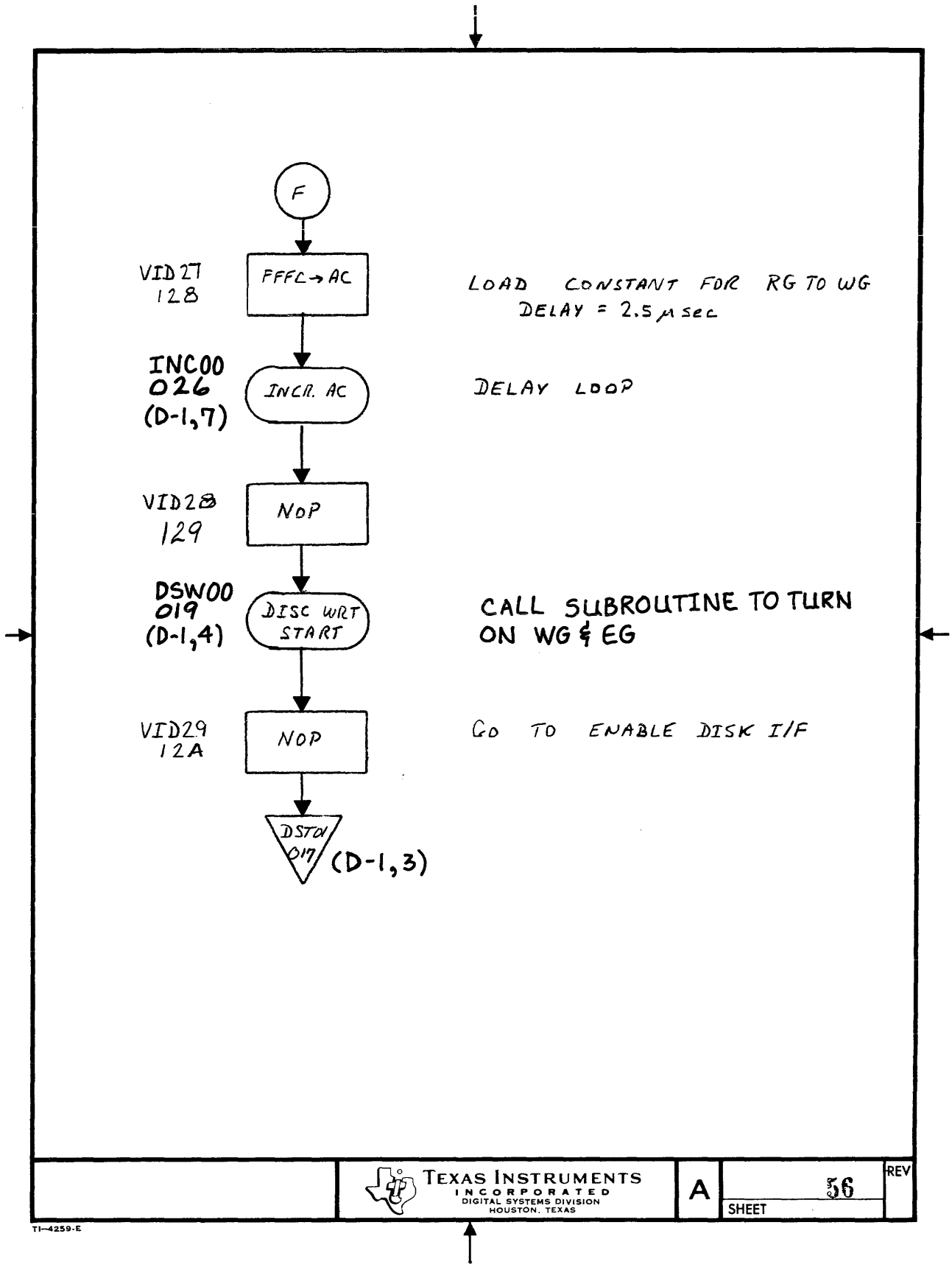


Figure D-1. Microcode Flowcharts (Sheet 56 of 101)

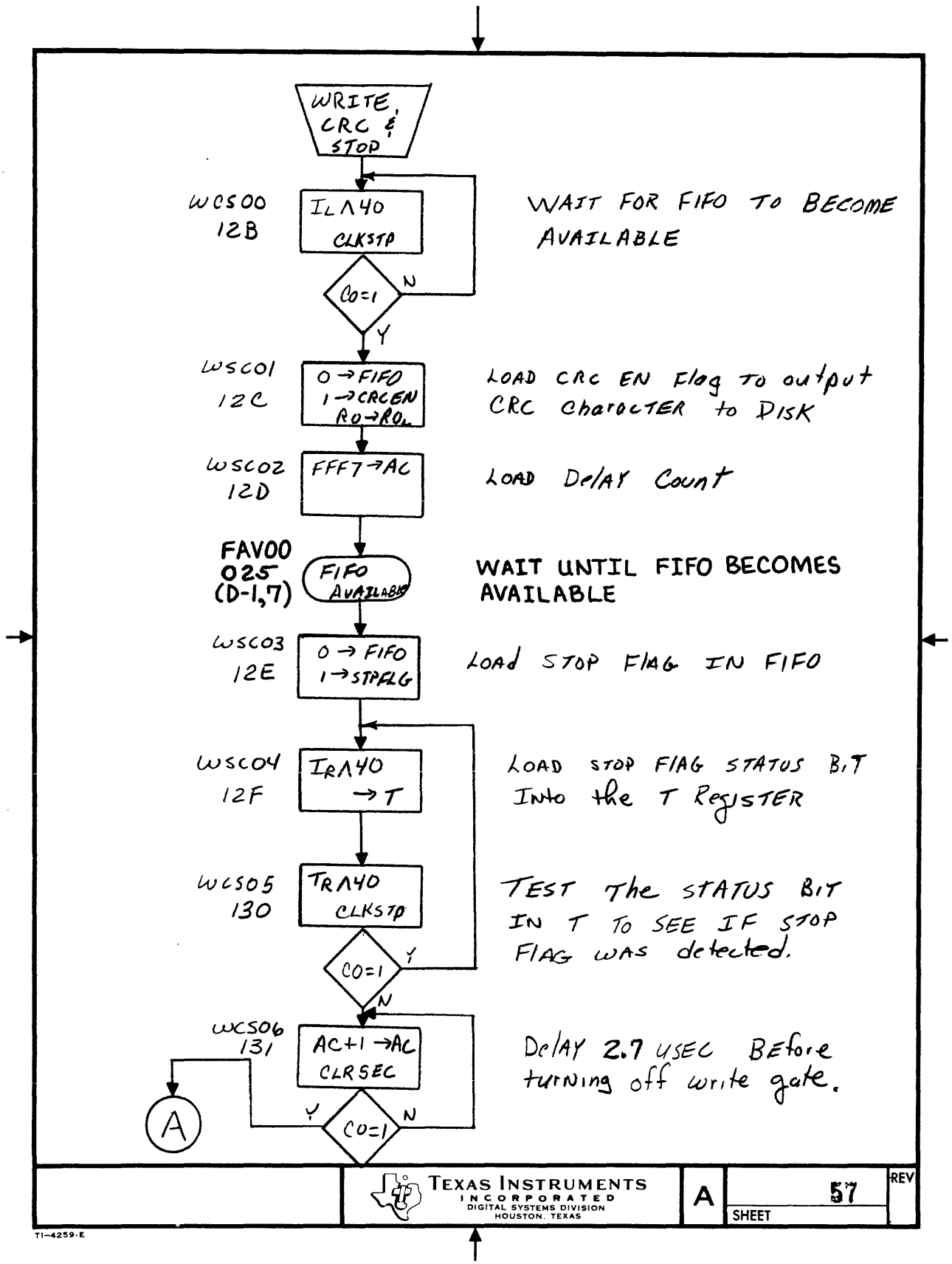


Figure D-1. Microcode Flowcharts (Sheet 57 of 101)

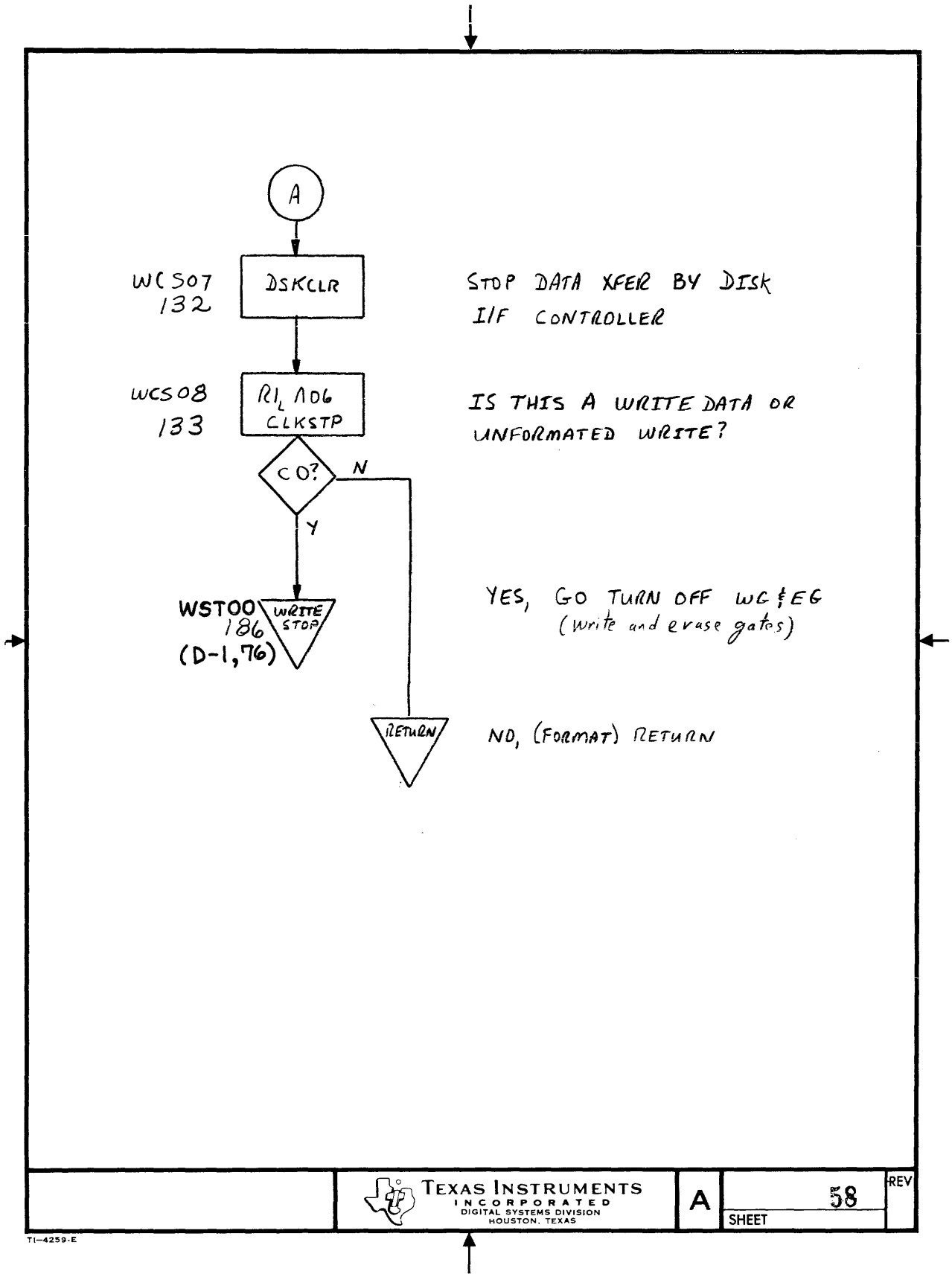


Figure D-1. Microcode Flowcharts (Sheet 58 of 101)

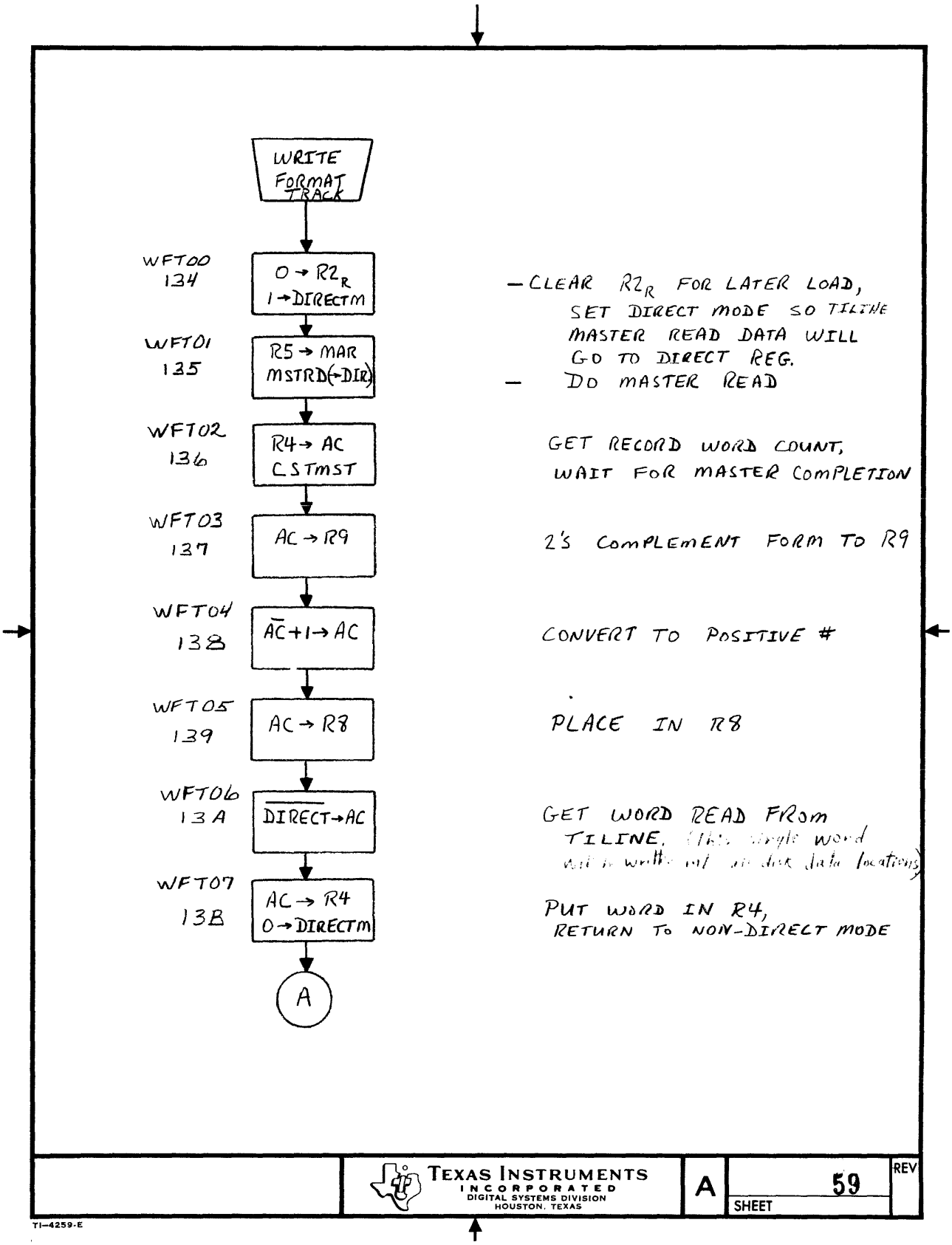


Figure D-1. Microcode Flowcharts (Sheet 59 of 101)

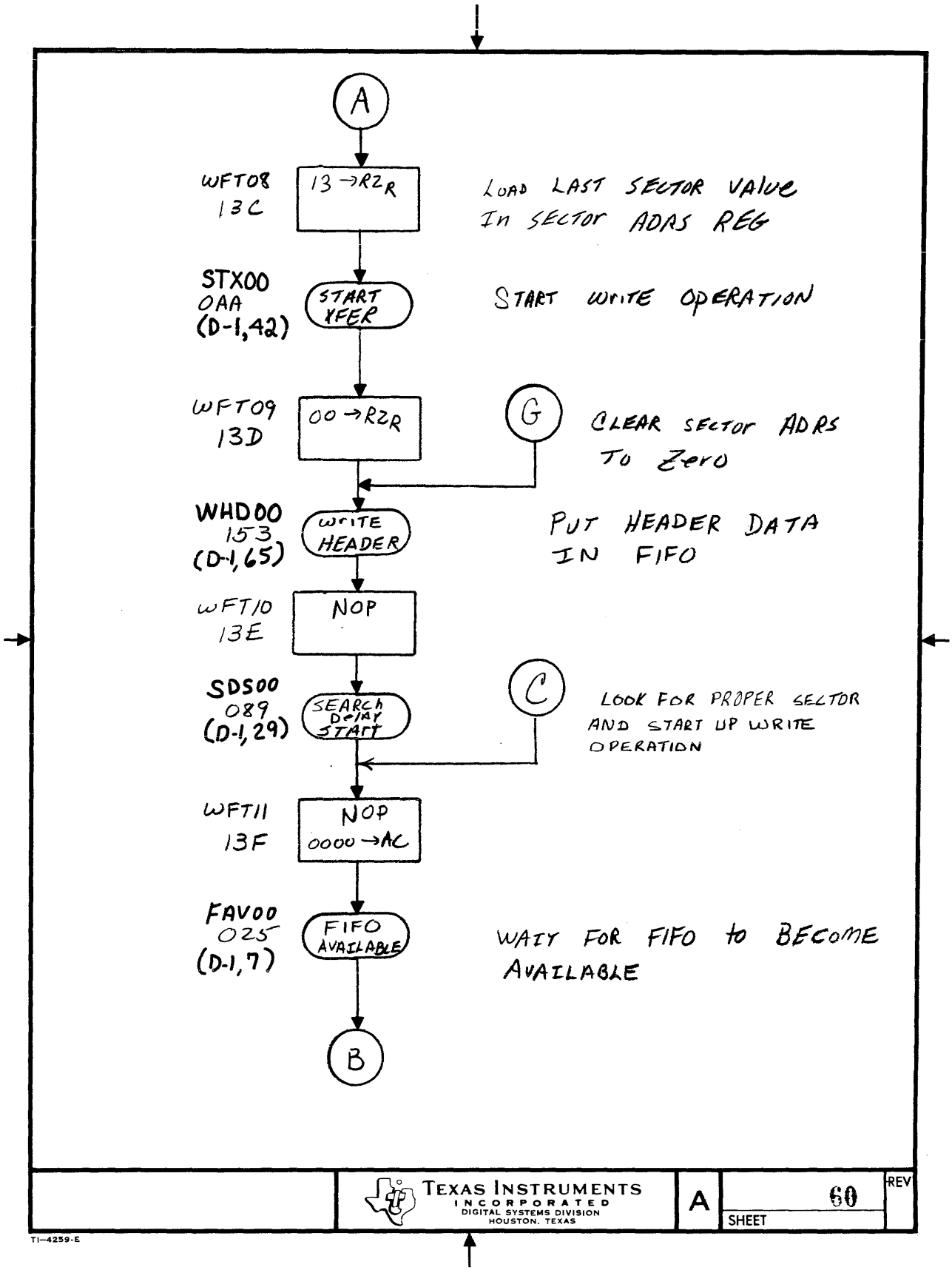


Figure D-1. Microcode Flowcharts (Sheet 60 of 101)

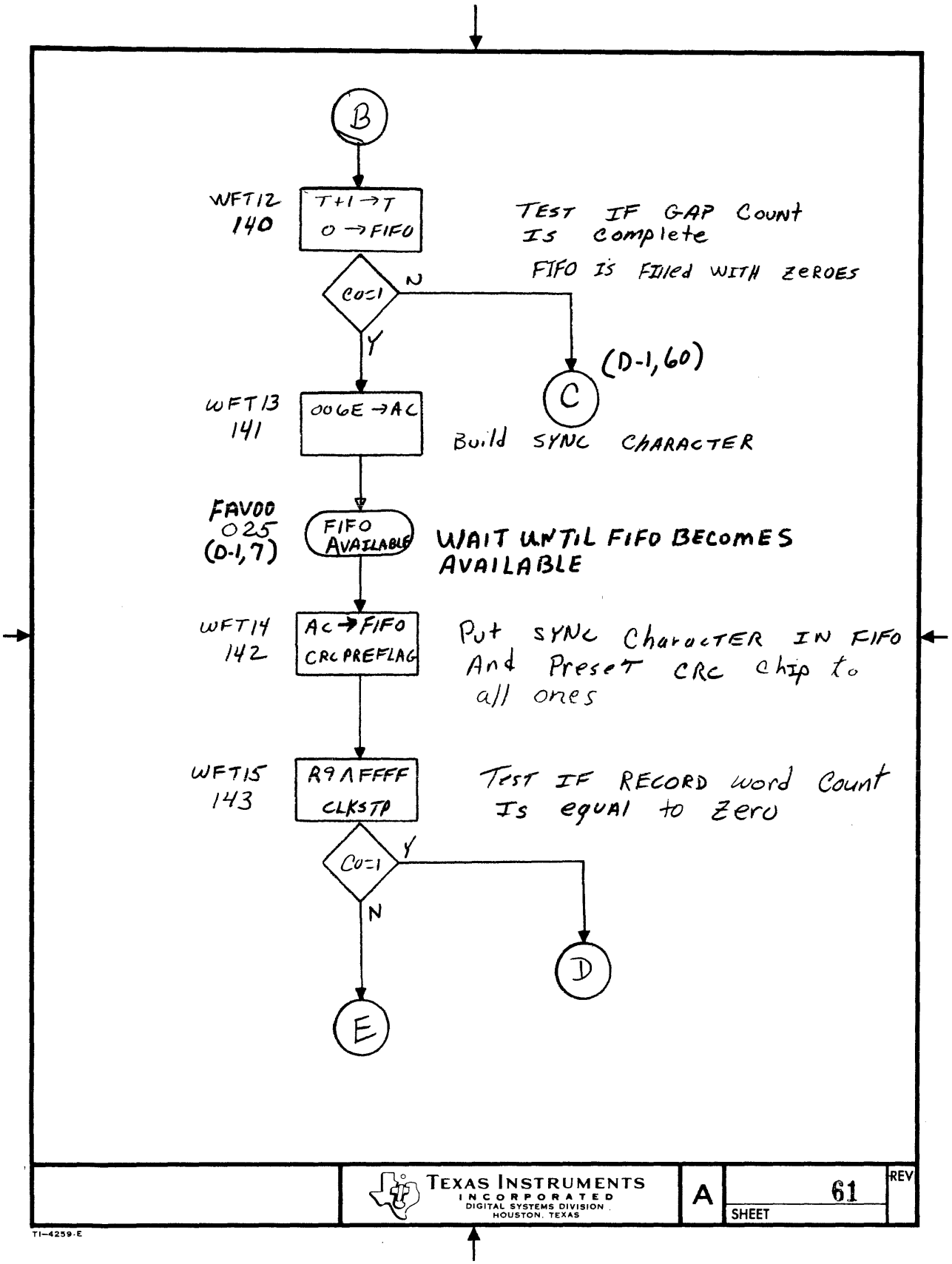


Figure D-1. Microcode Flowcharts (Sheet 61 of 101)

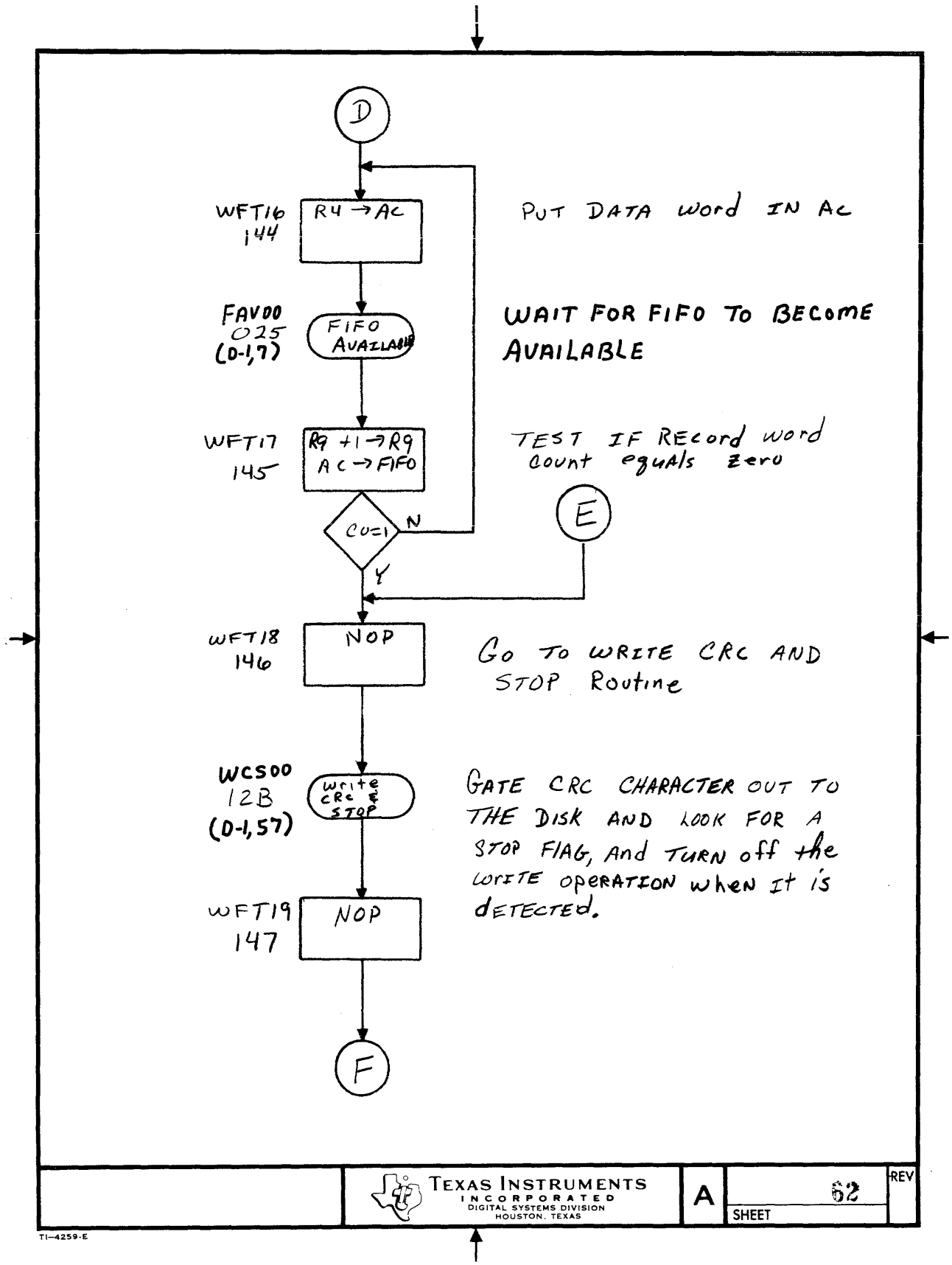


Figure D-1. Microcode Flowcharts (Sheet 62 of 101)

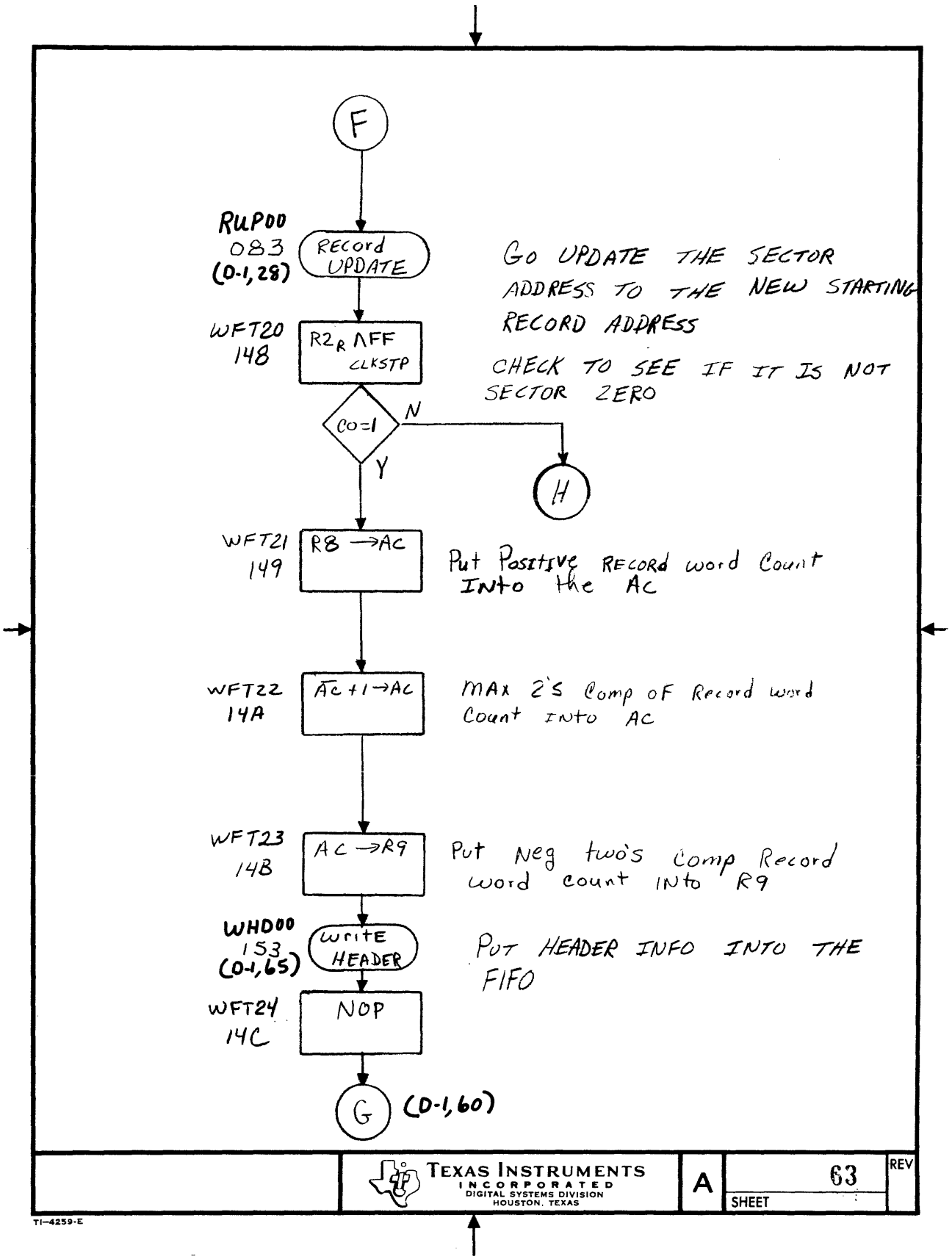


Figure D-1. Microcode Flowcharts (Sheet 63 of 101)

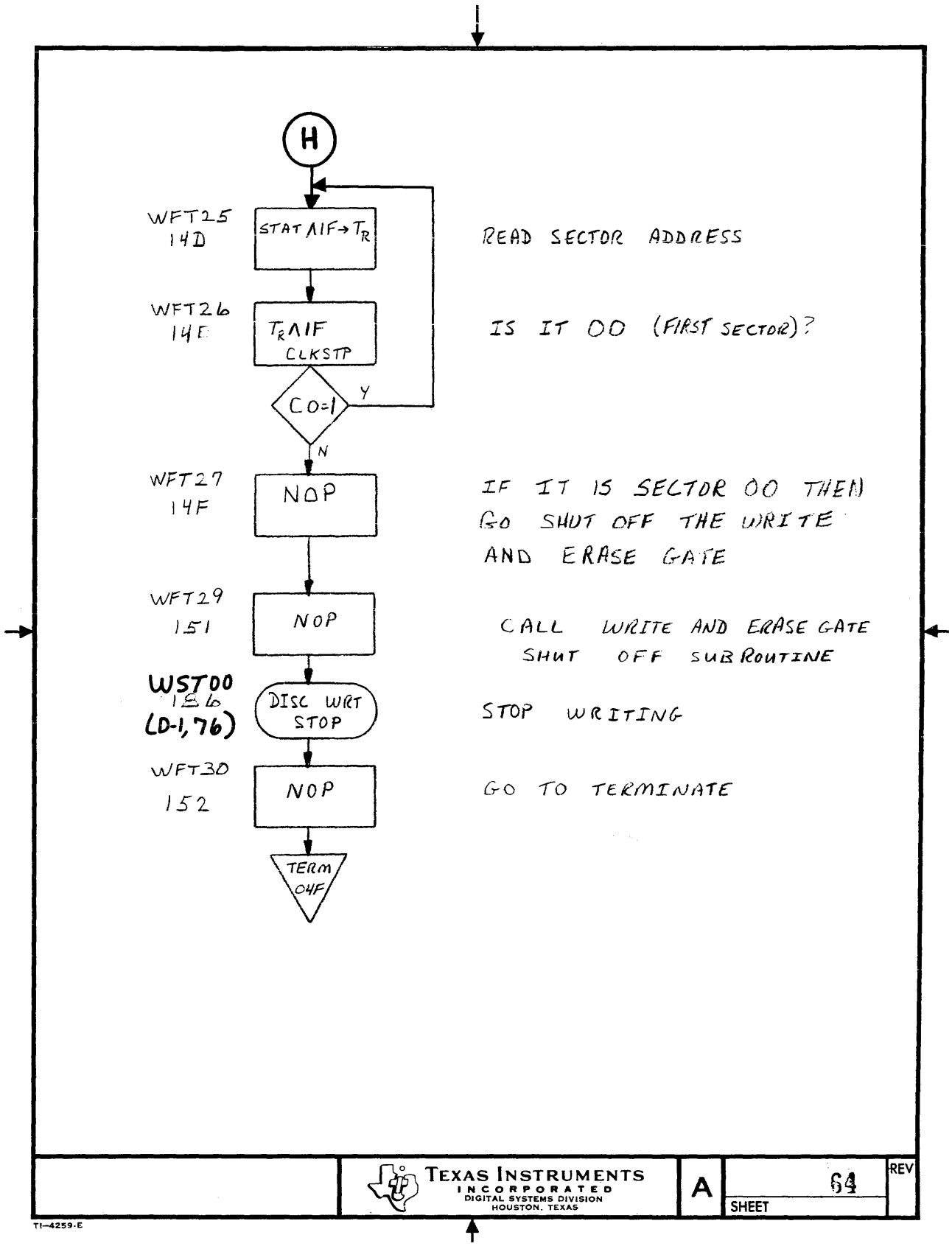


Figure D-1. Microcode Flowcharts (Sheet 64 of 101)

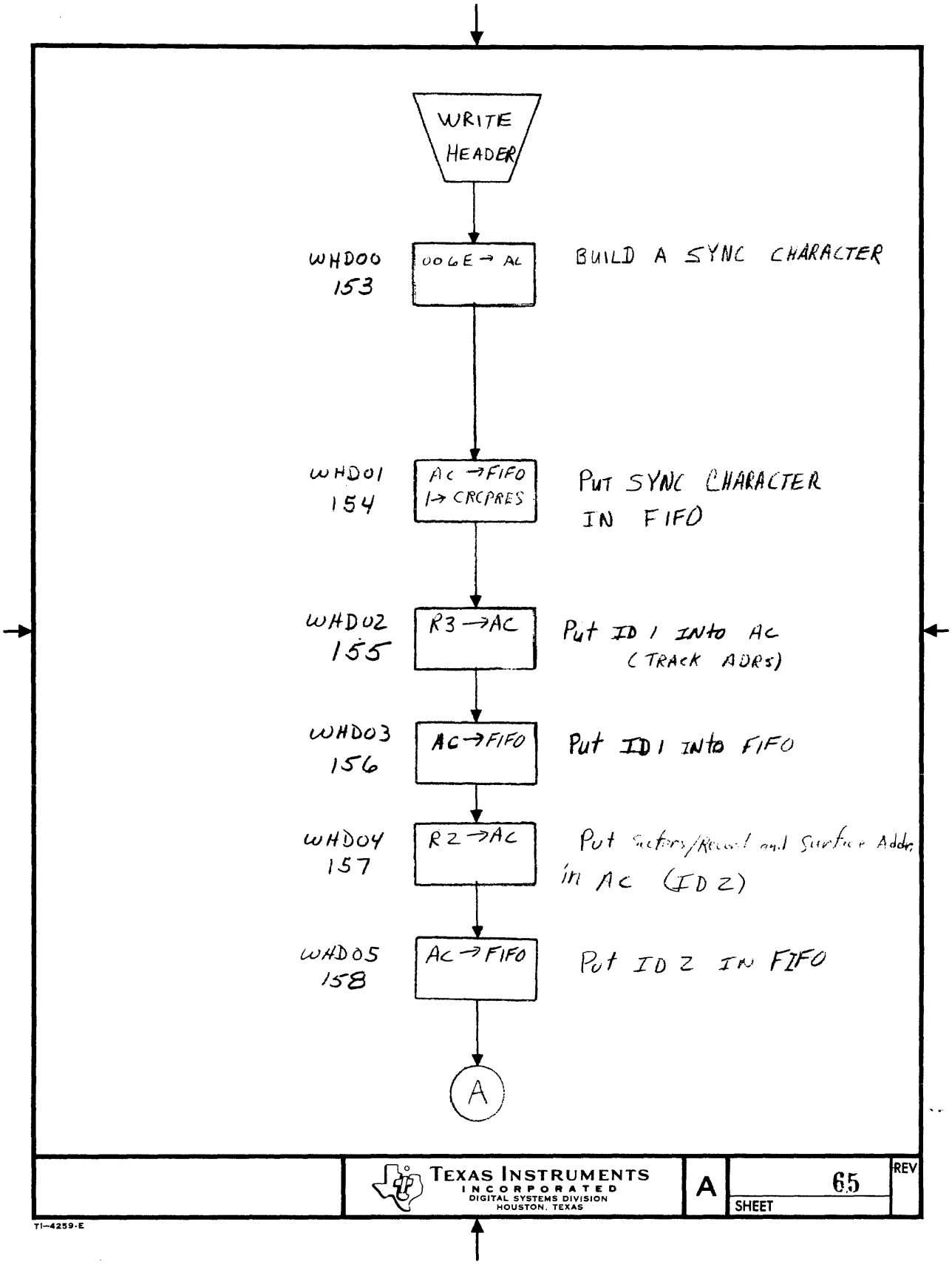


Figure D-1. Microcode Flowcharts (Sheet 65 of 101)

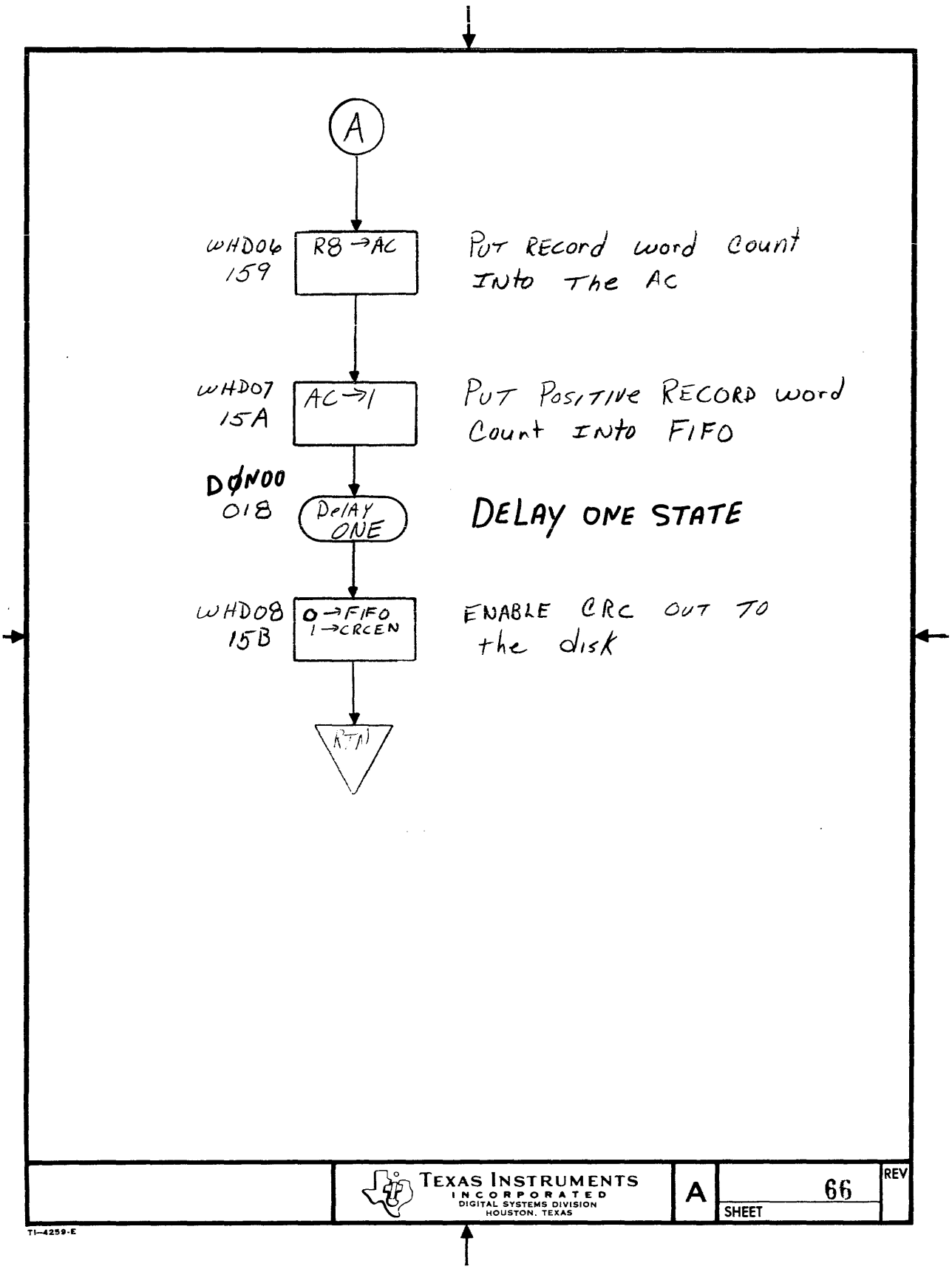


Figure D-1. Microcode Flowcharts (Sheet 66 of 101)

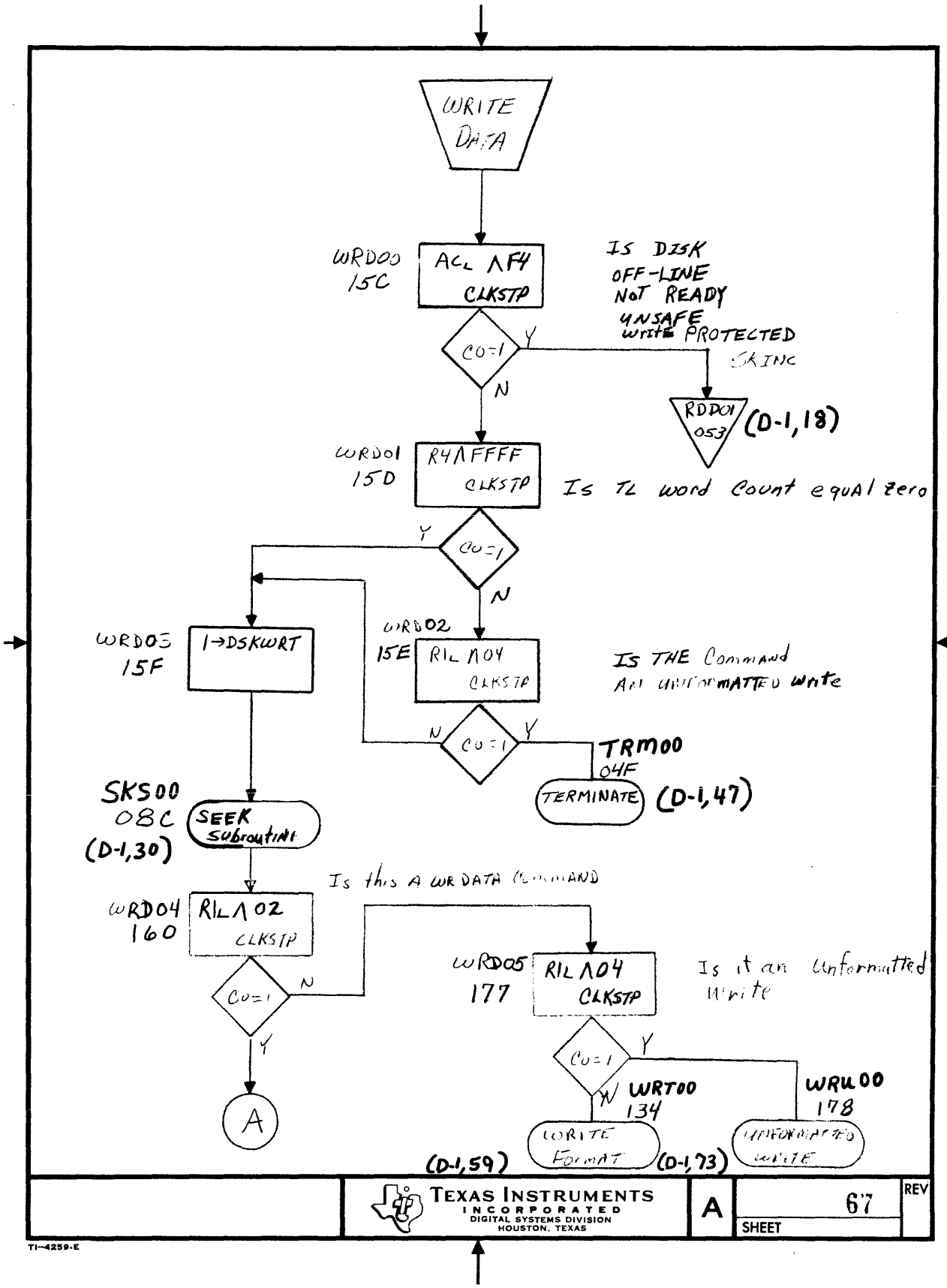


Figure D-1. Microcode Flowcharts (Sheet 67 of 101)

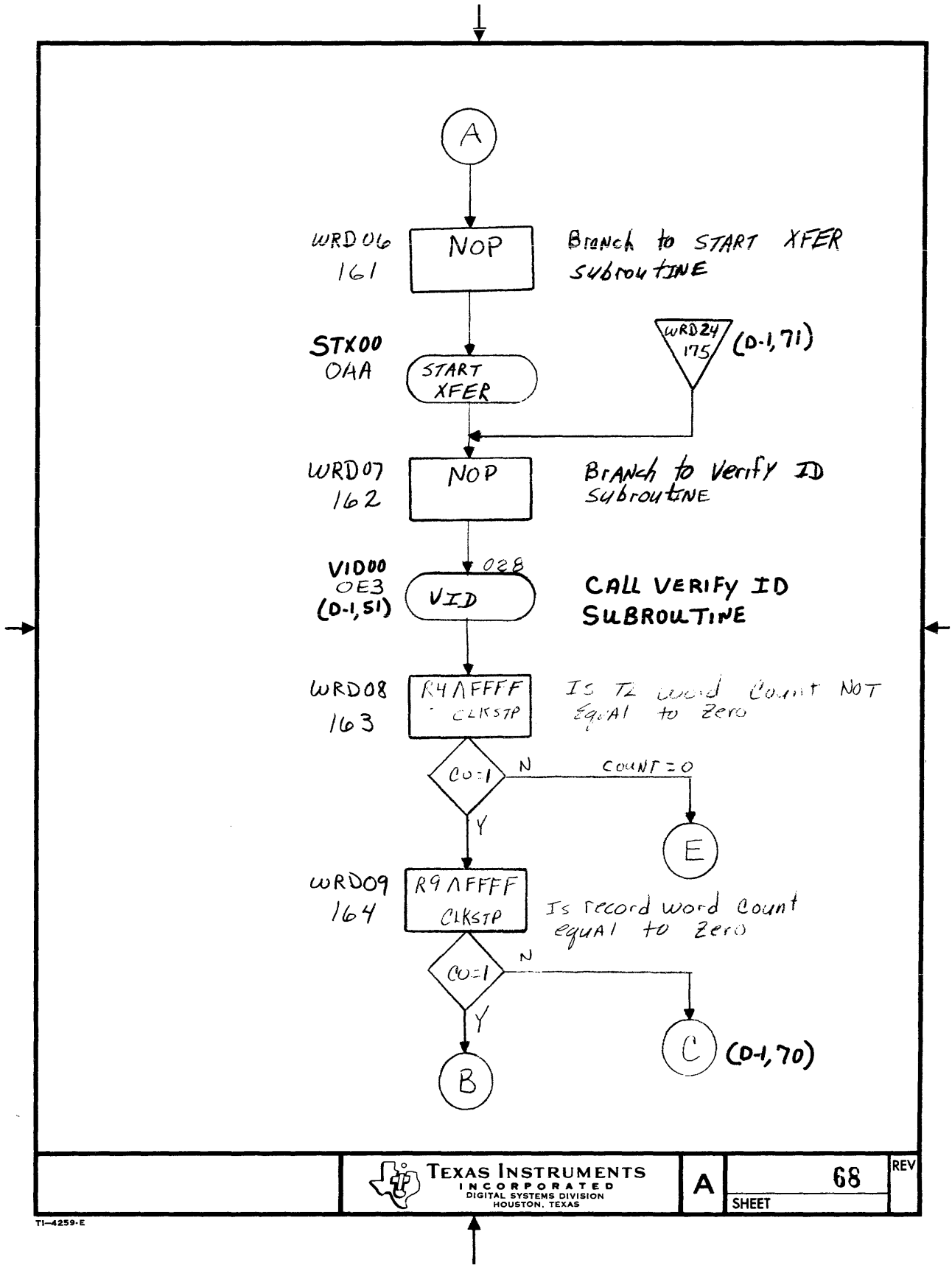


Figure D-1. Microcode Flowcharts (Sheet 68 of 101)

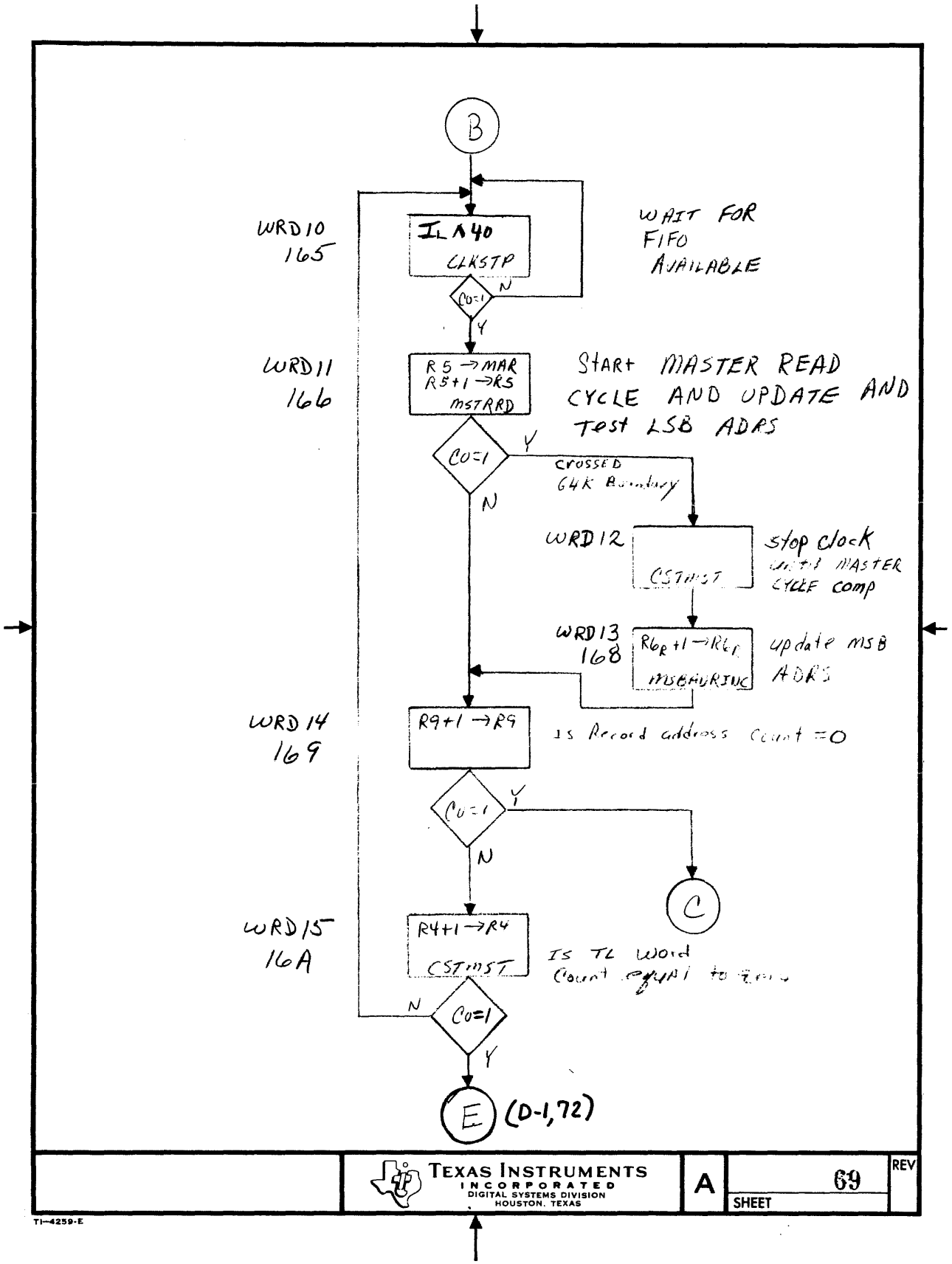


Figure D-1. Microcode Flowcharts (Sheet 69 of 101)

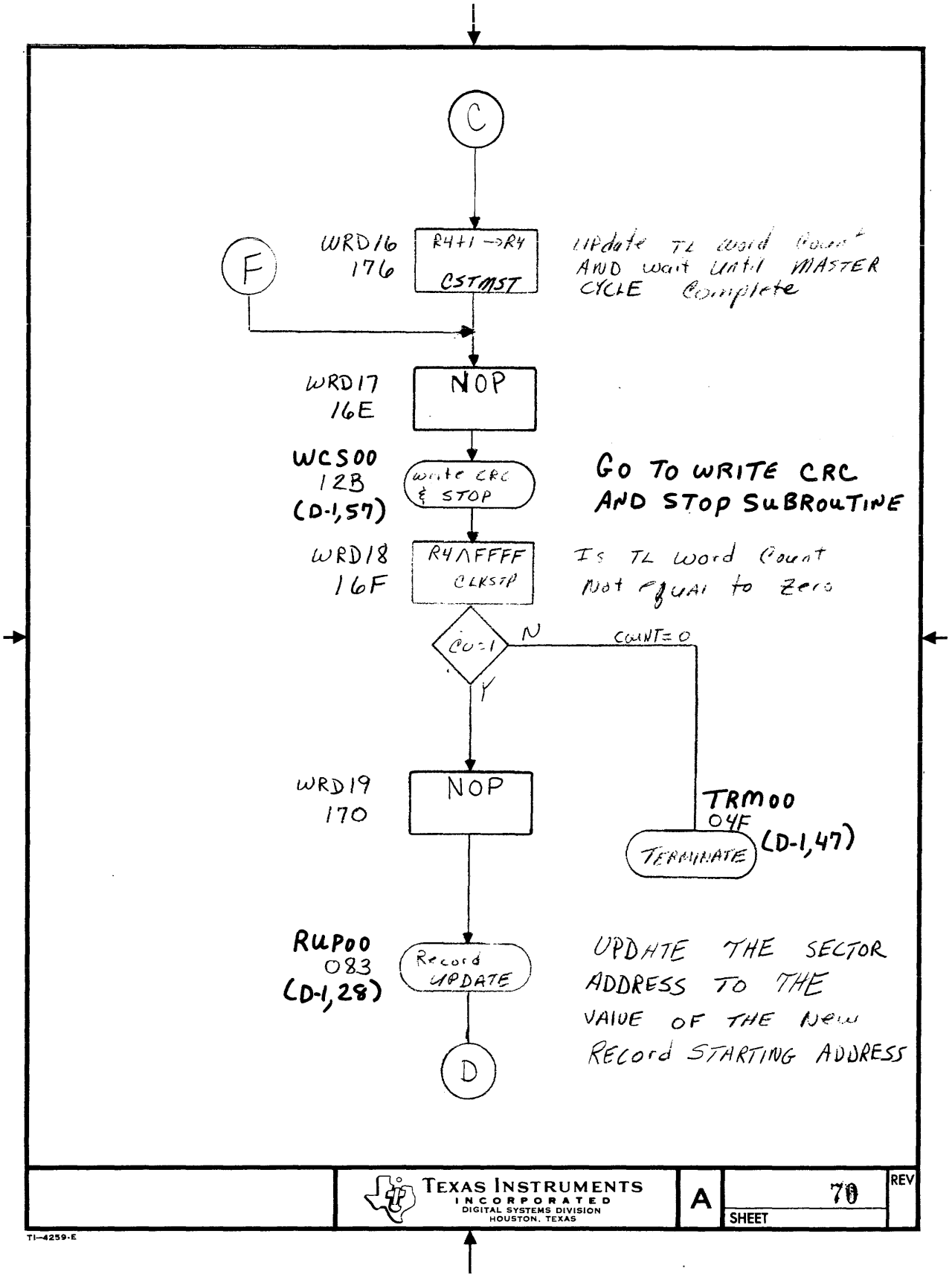


Figure D-1. Microcode Flowcharts (Sheet 70 of 101)

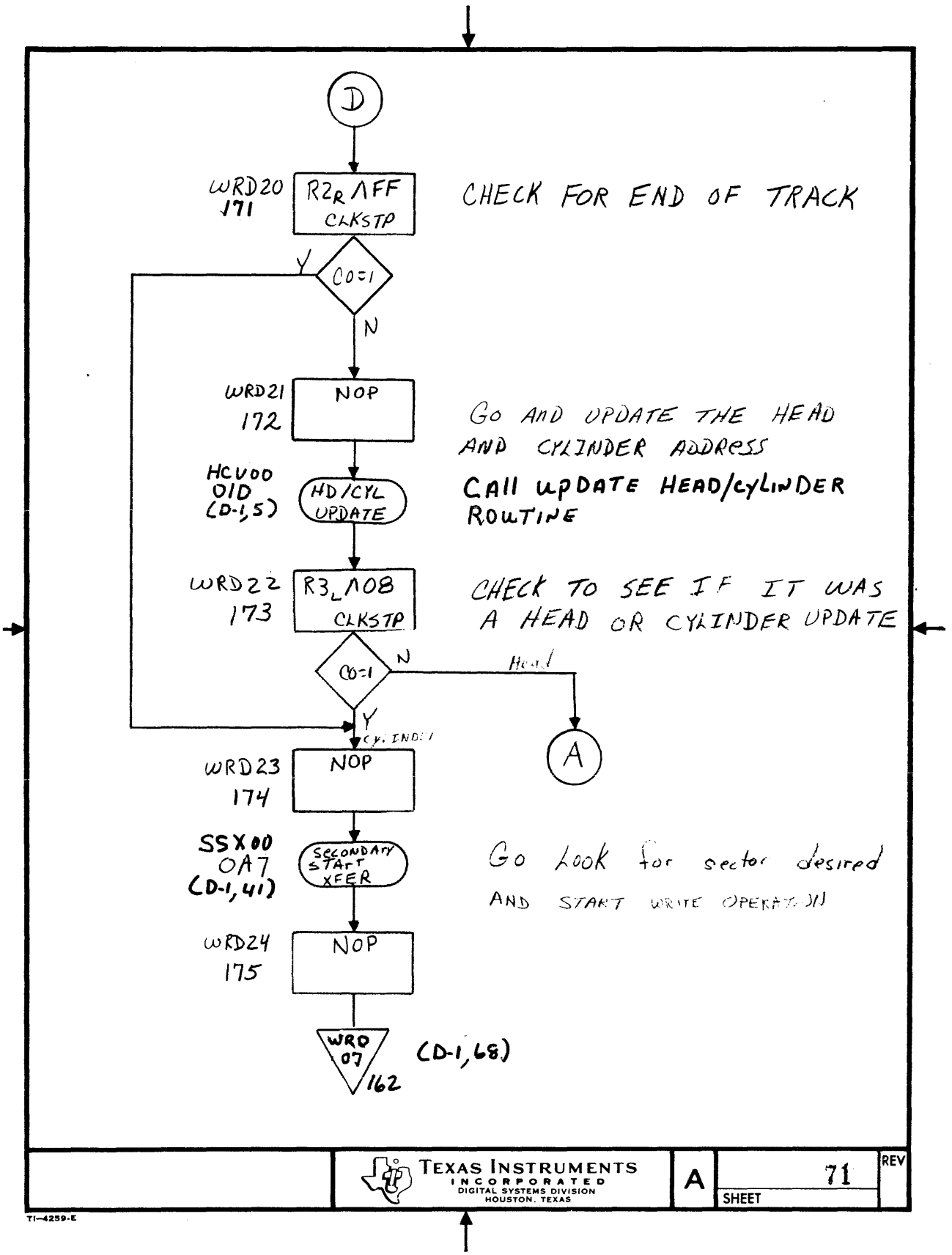


Figure D-1. Microcode Flowcharts (Sheet 71 of 101)

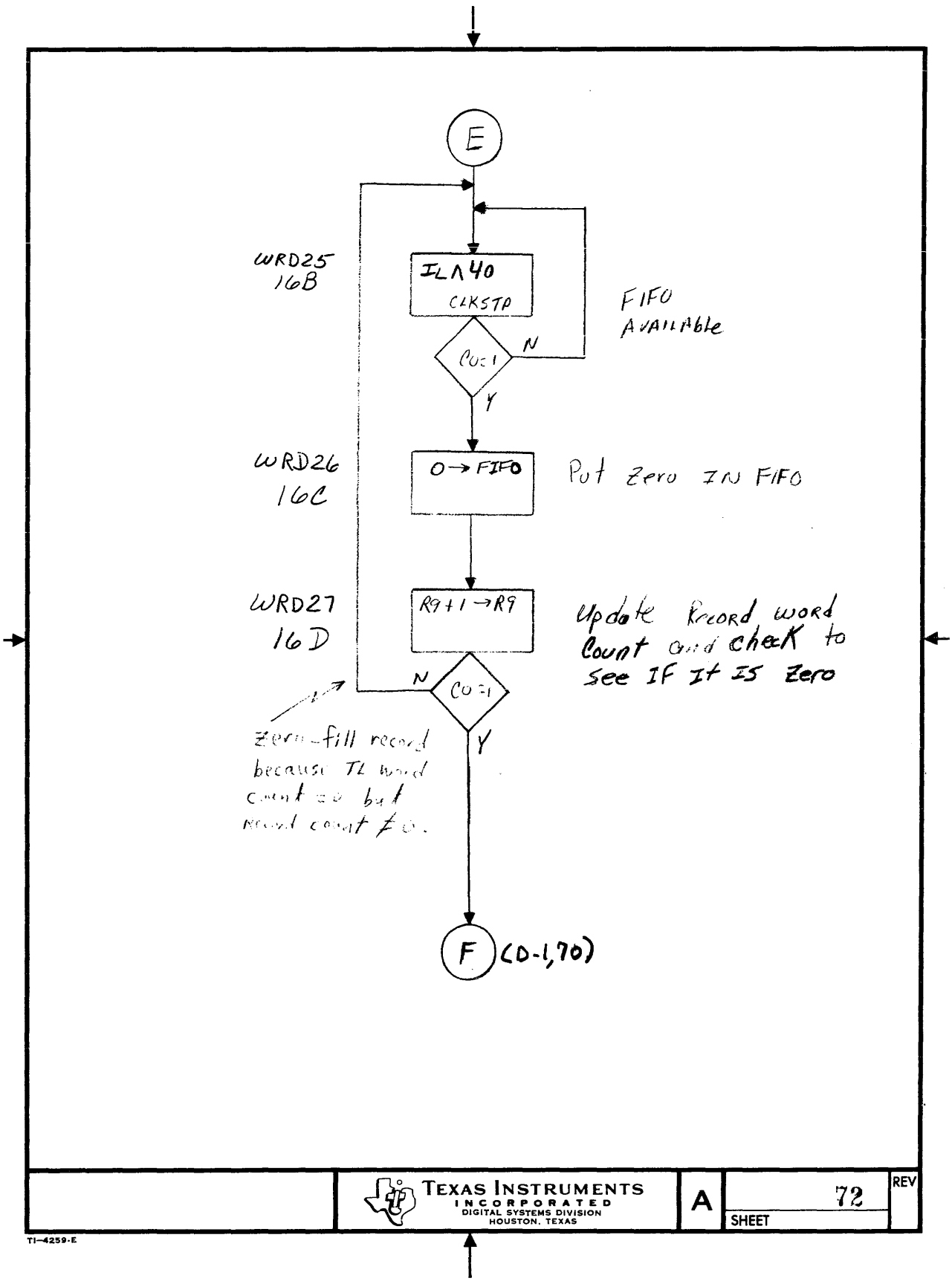


Figure D-1. Microcode Flowcharts (Sheet 72 of 101)

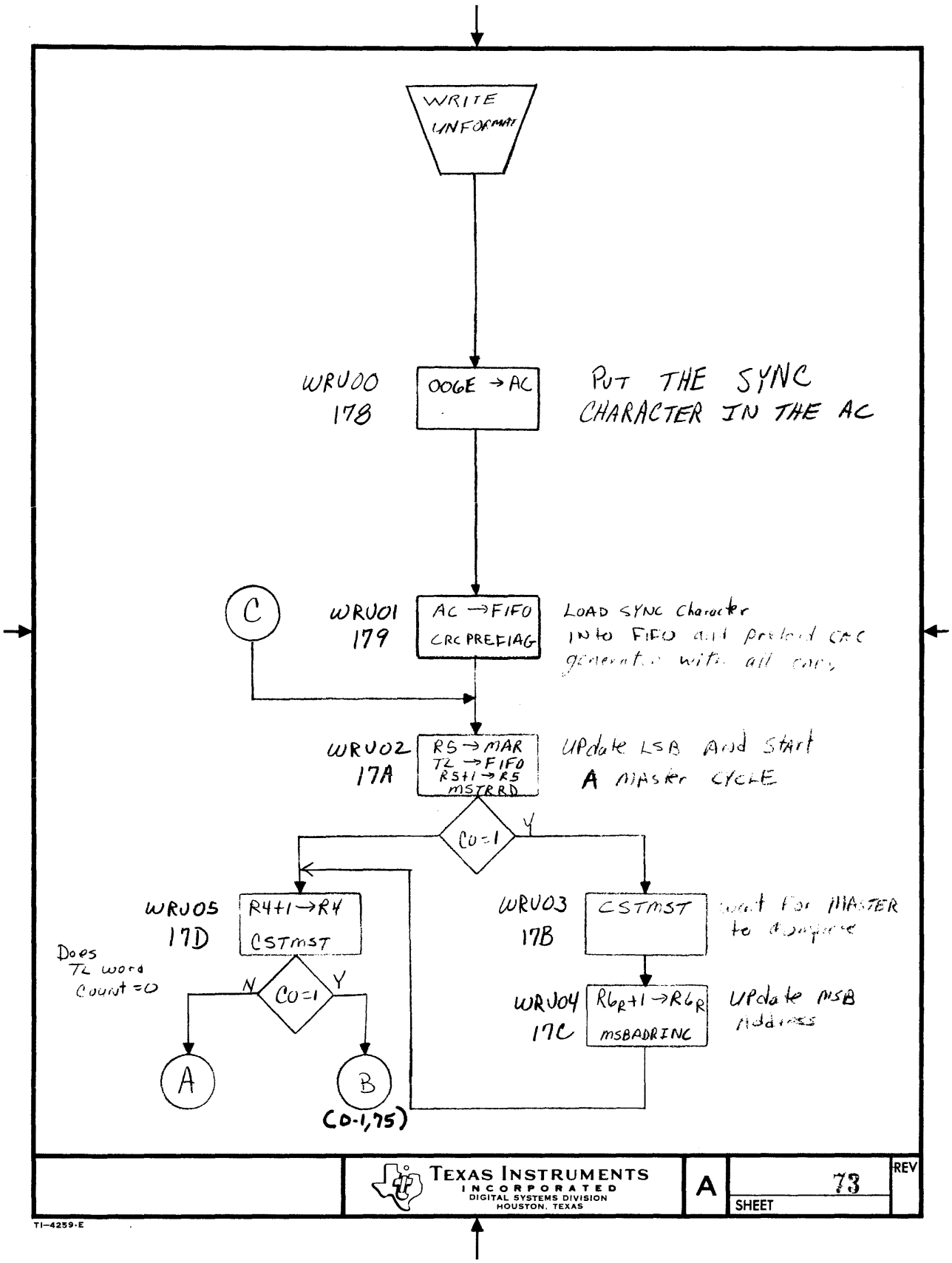


Figure D-1. Microcode Flowcharts (Sheet 73 of 101)

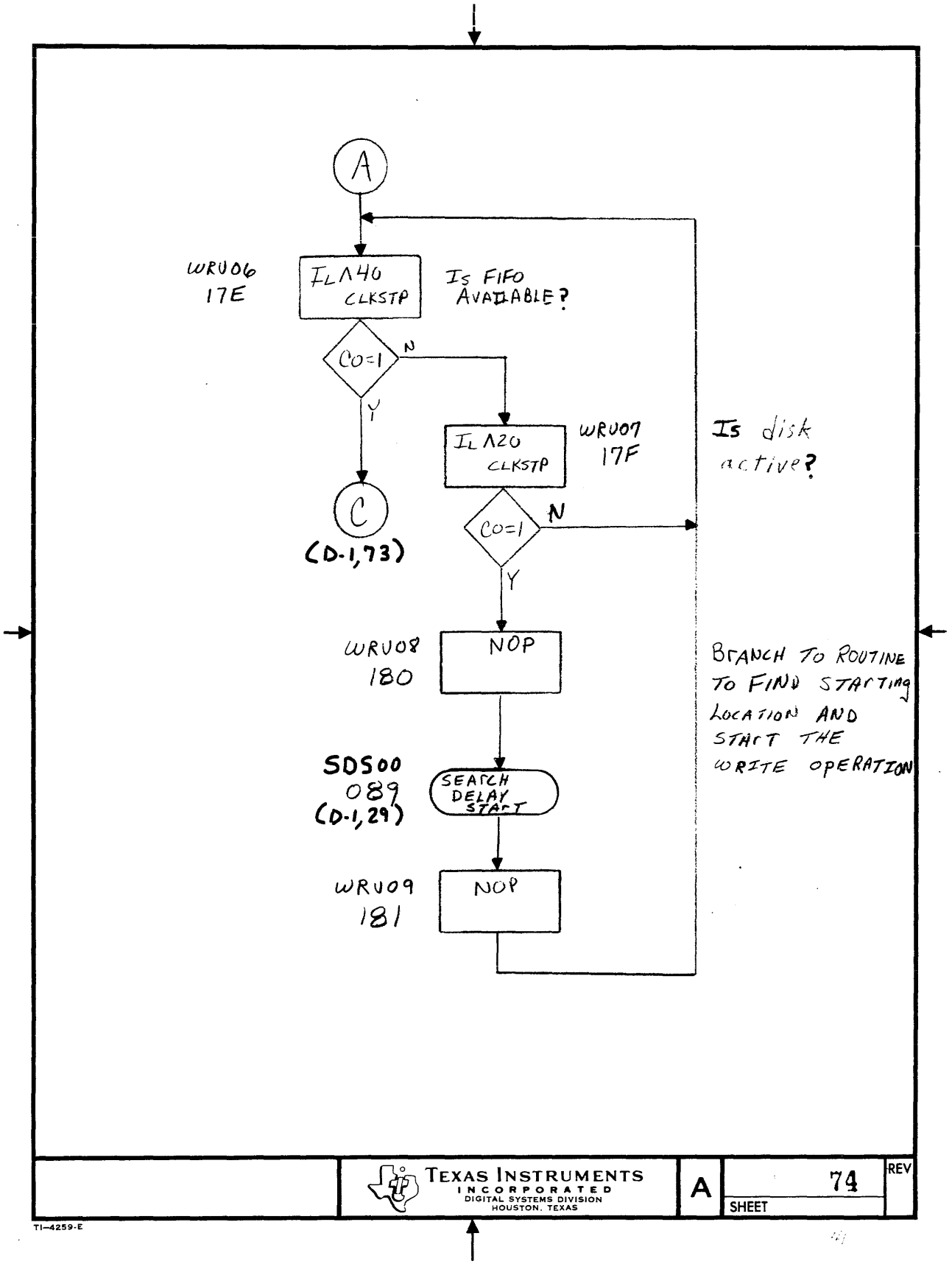


Figure D-1. Microcode Flowcharts (Sheet 74 of 101)

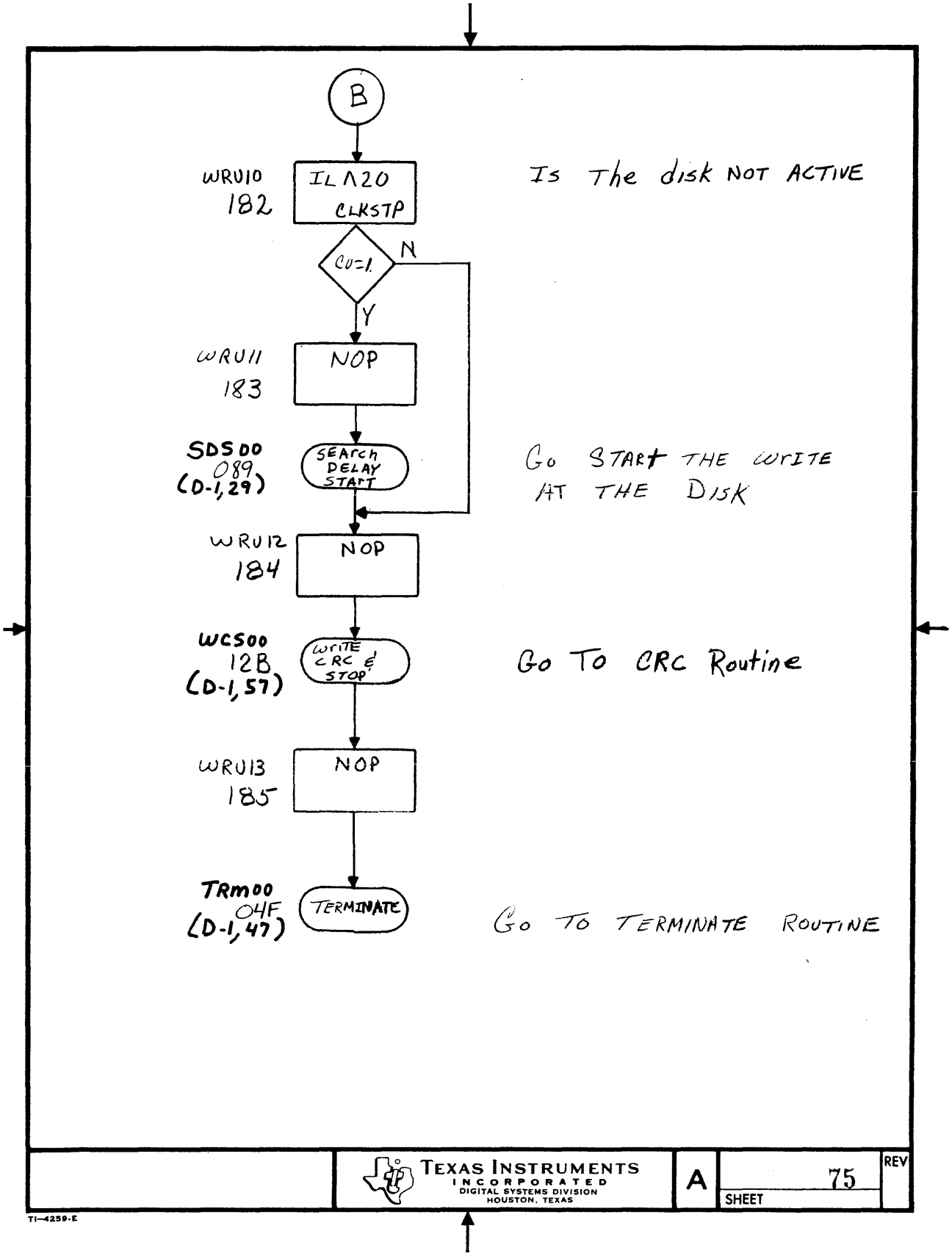


Figure D-1. Microcode Flowcharts (Sheet 75 of 101)

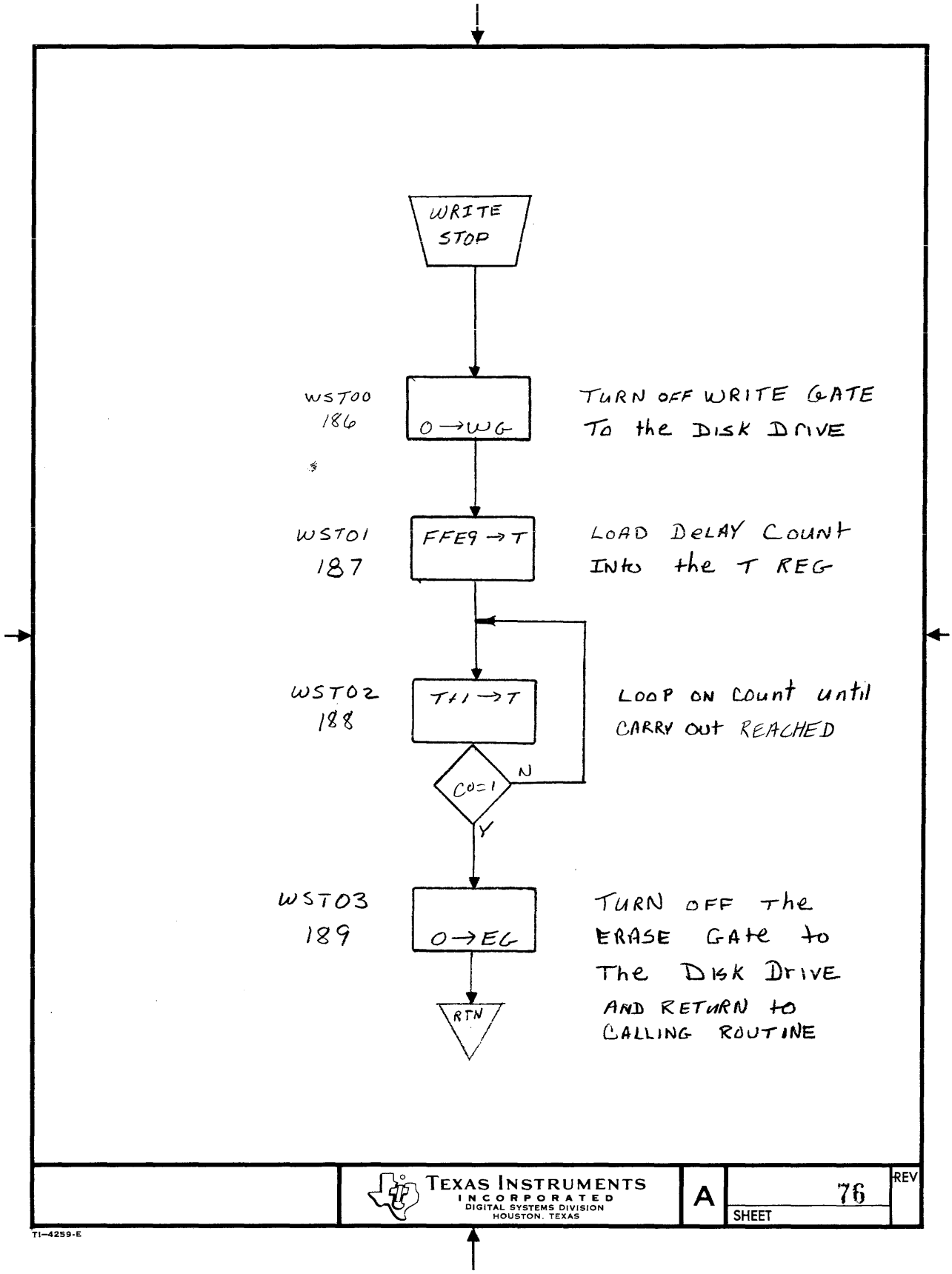


Figure D-1. Microcode Flowcharts (Sheet 76 of 101)

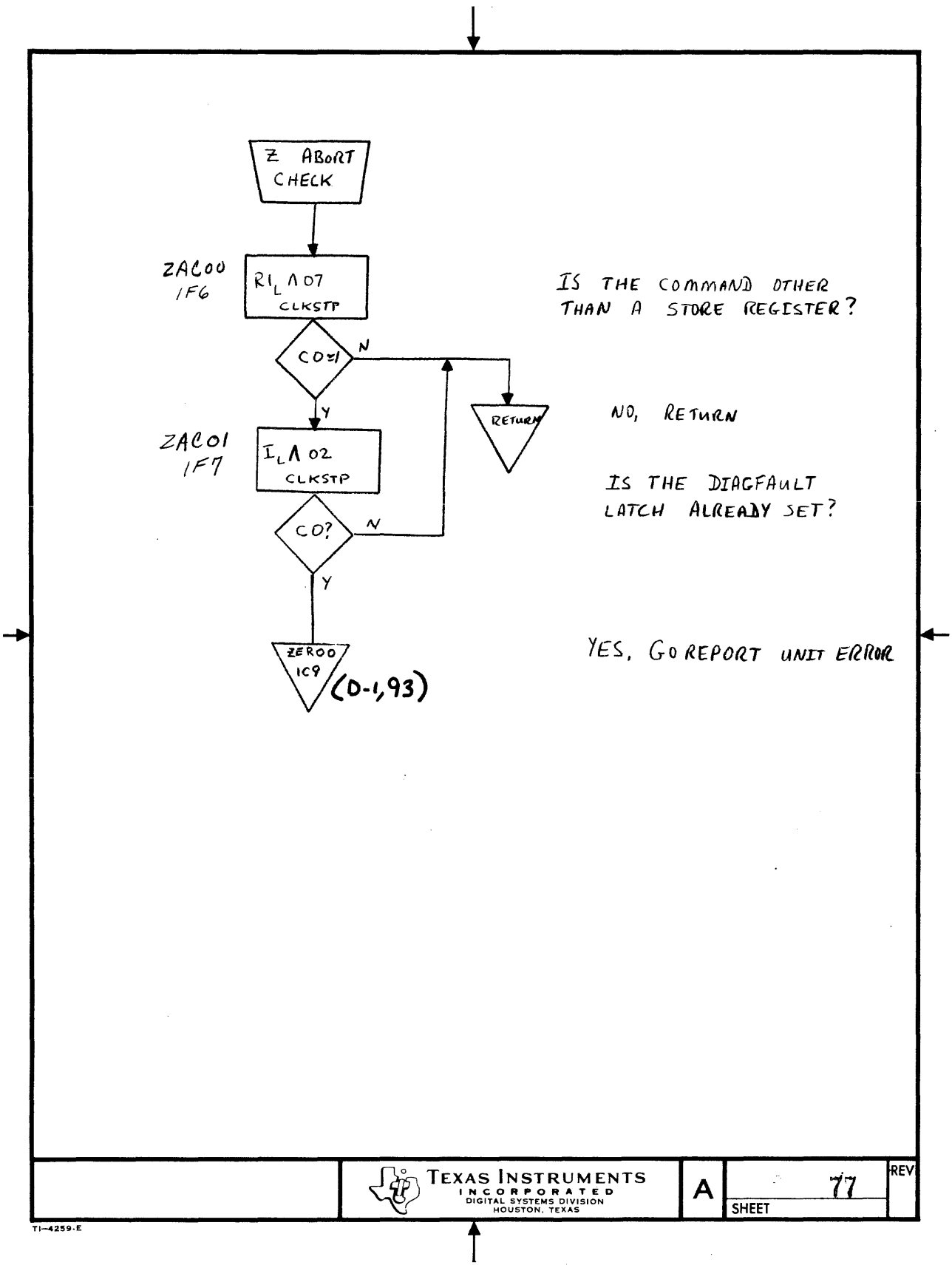


Figure D-1. Microcode Flowcharts (Sheet 77 of 101)

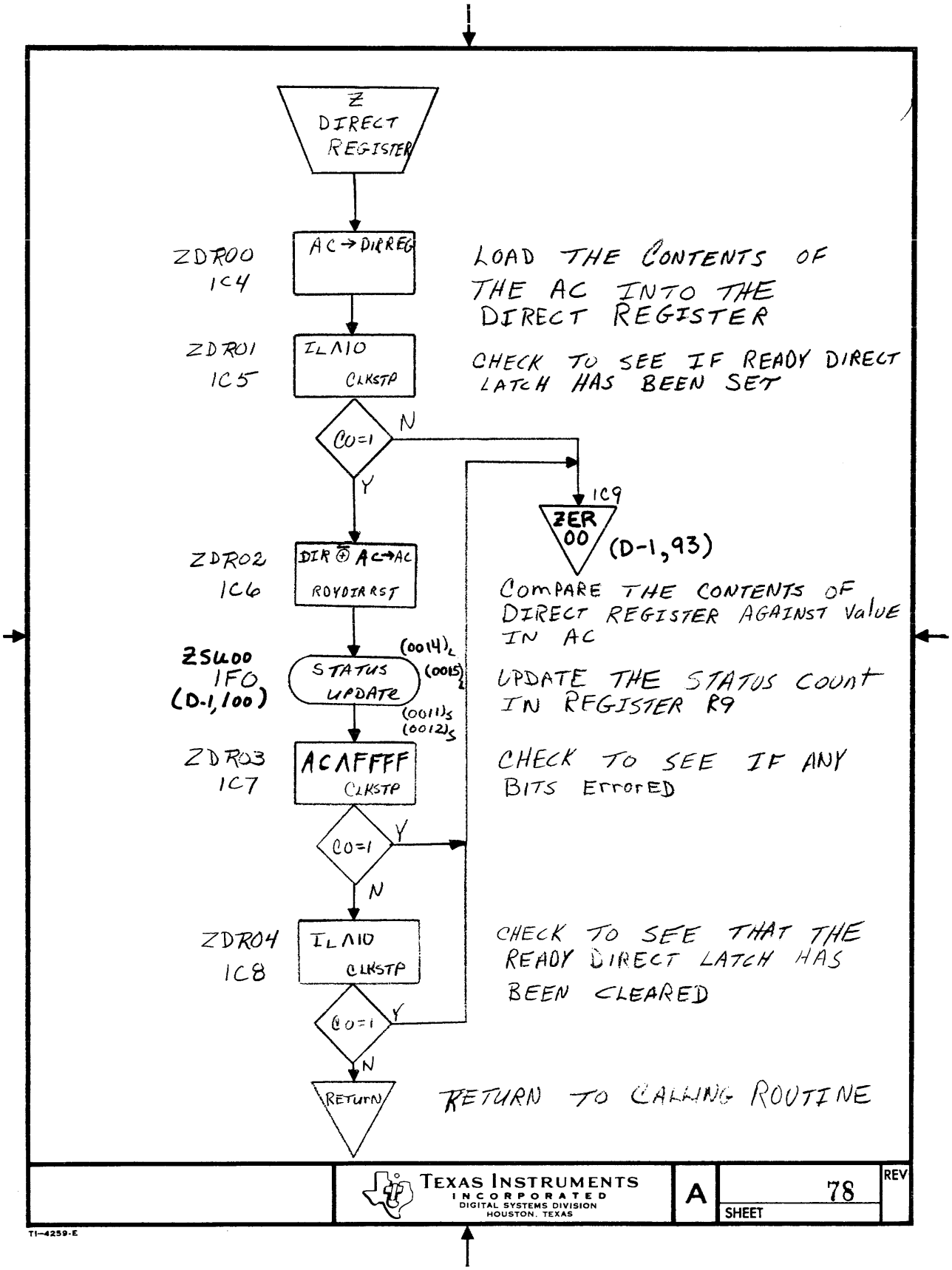


Figure D-1. Microcode Flowcharts (Sheet 78 of 101)

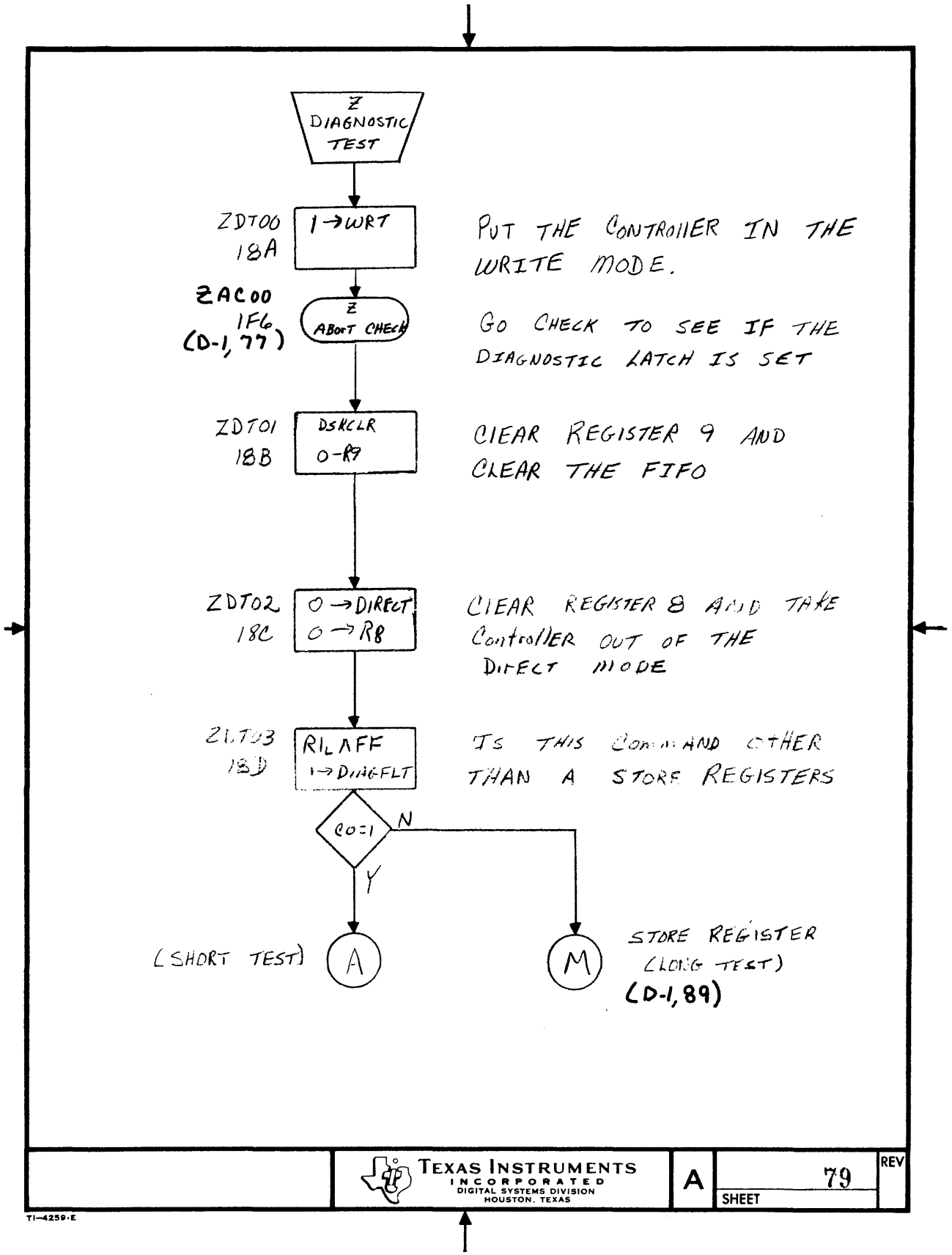


Figure D-1. Microcode Flowcharts (Sheet 79 of 101)

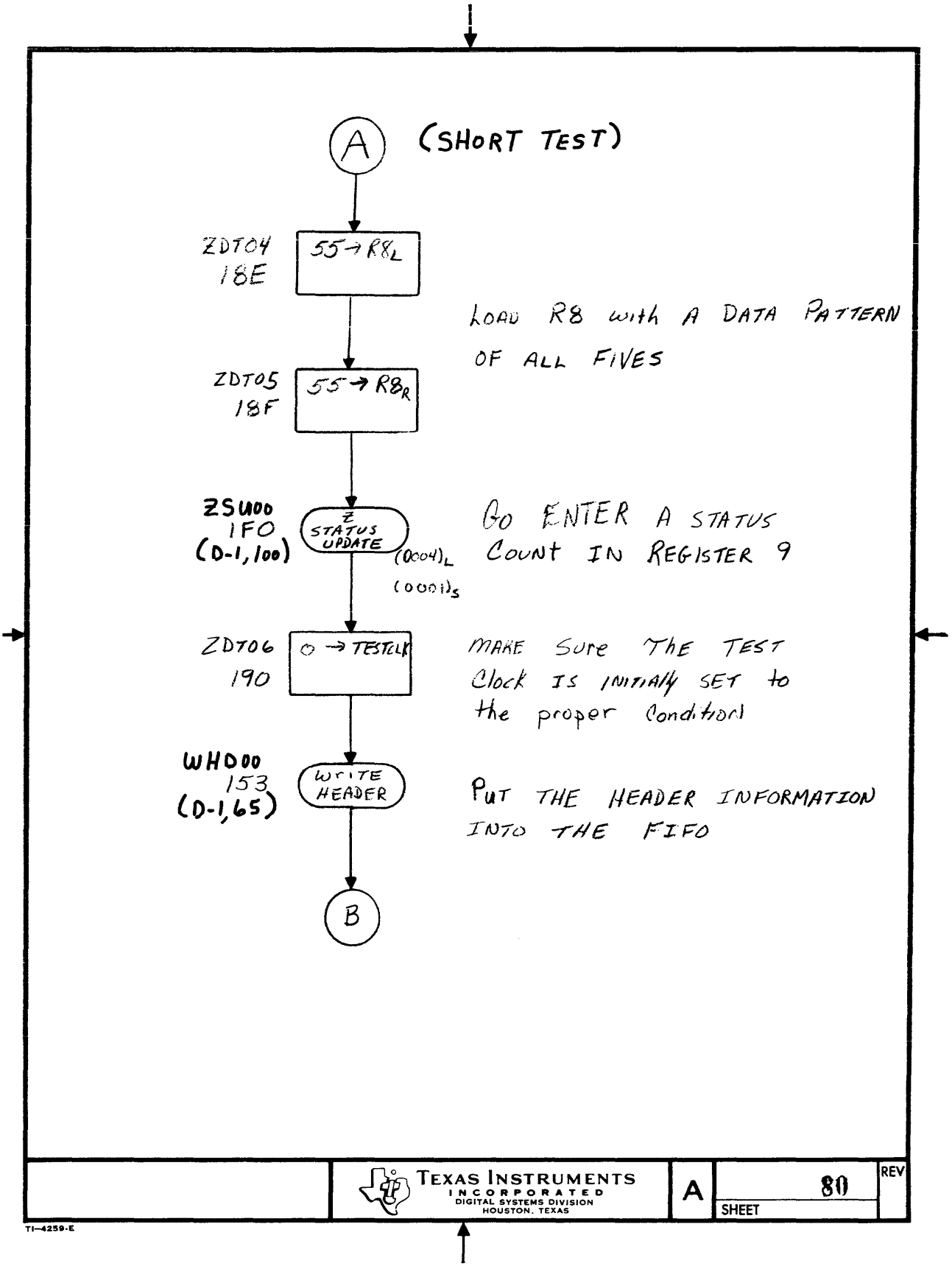


Figure D-1. Microcode Flowcharts (Sheet 80 of 101)

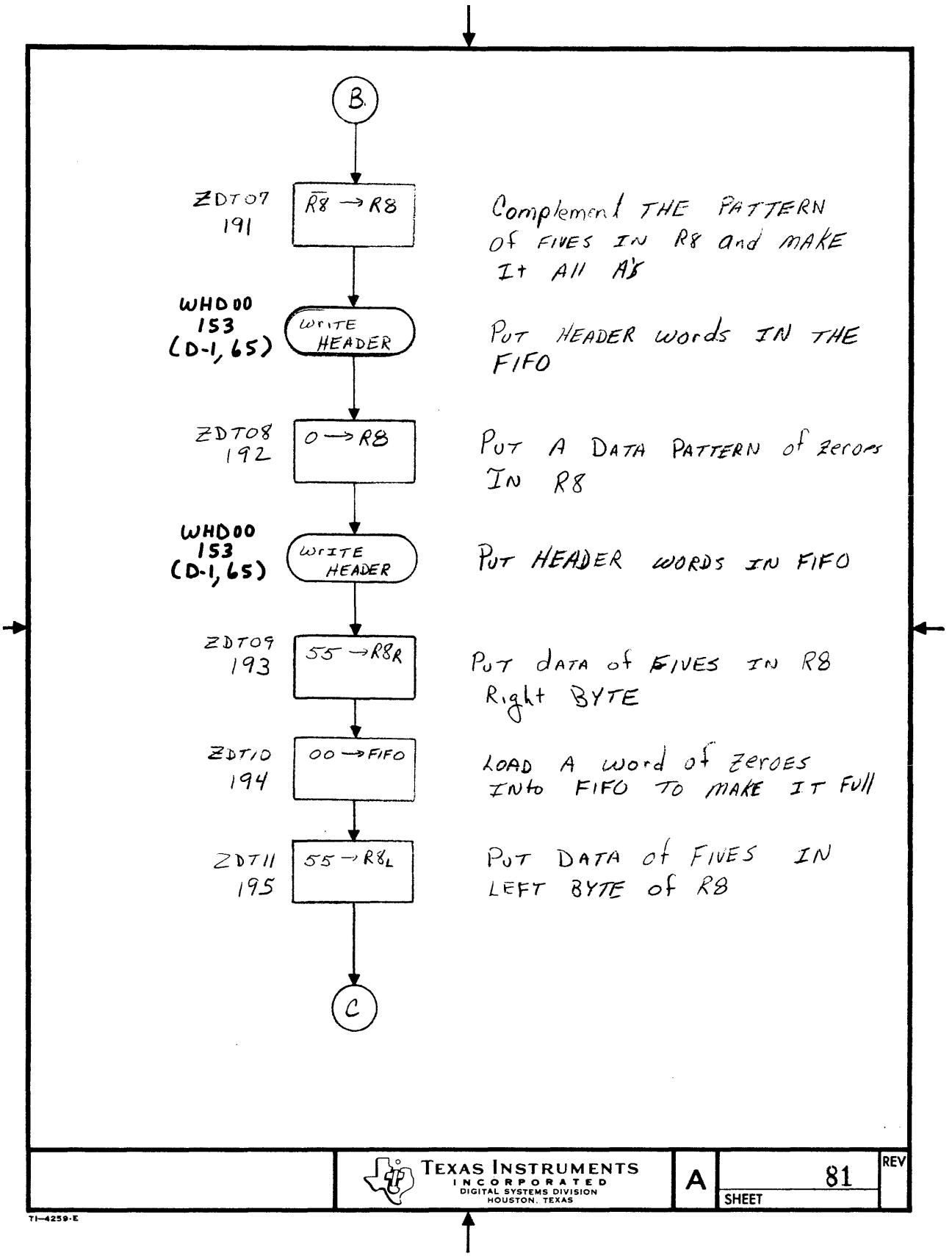


Figure D-1. Microcode Flowcharts (Sheet 81 of 101)

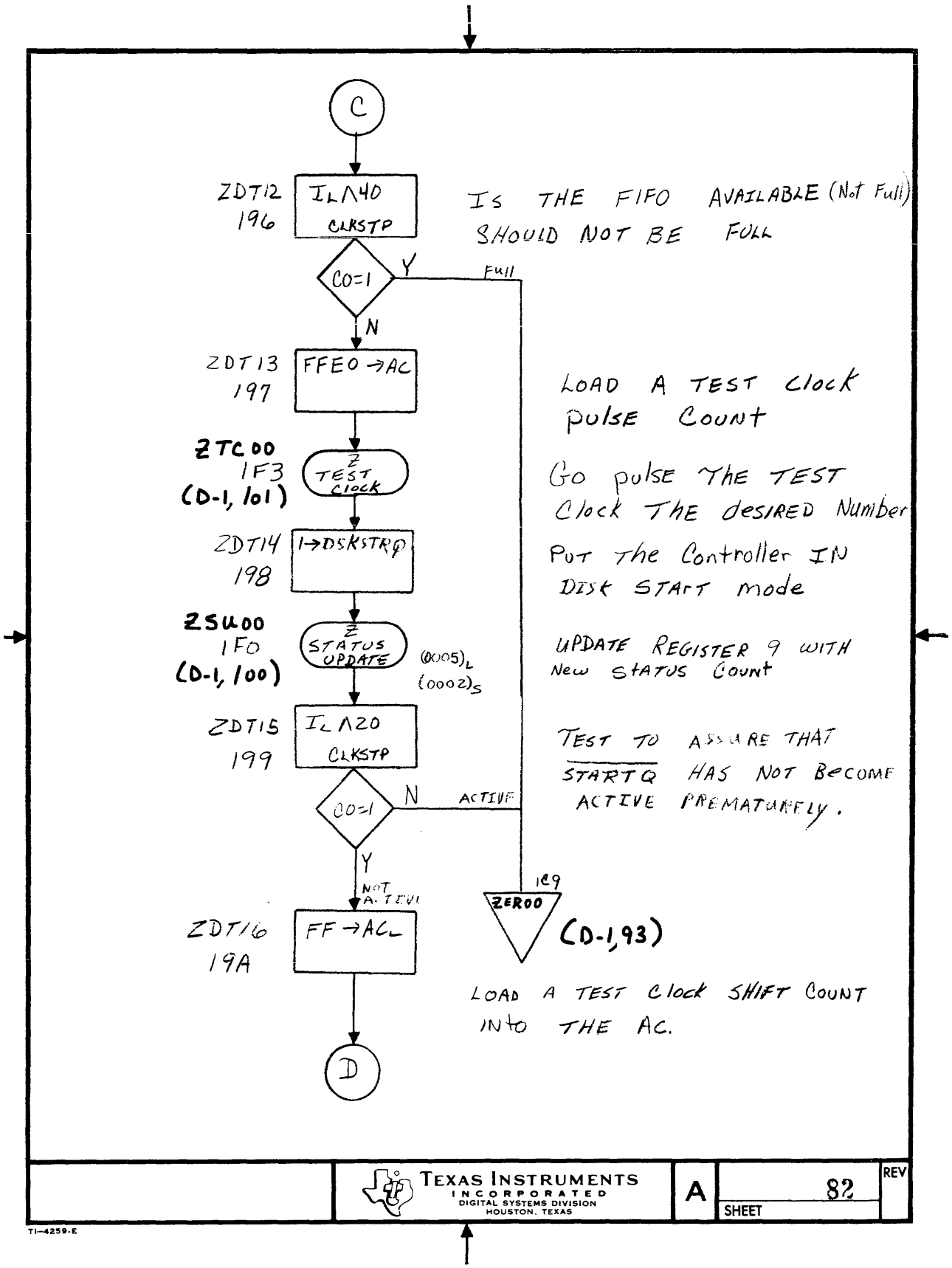


Figure D-1. Microcode Flowcharts (Sheet 82 of 101)

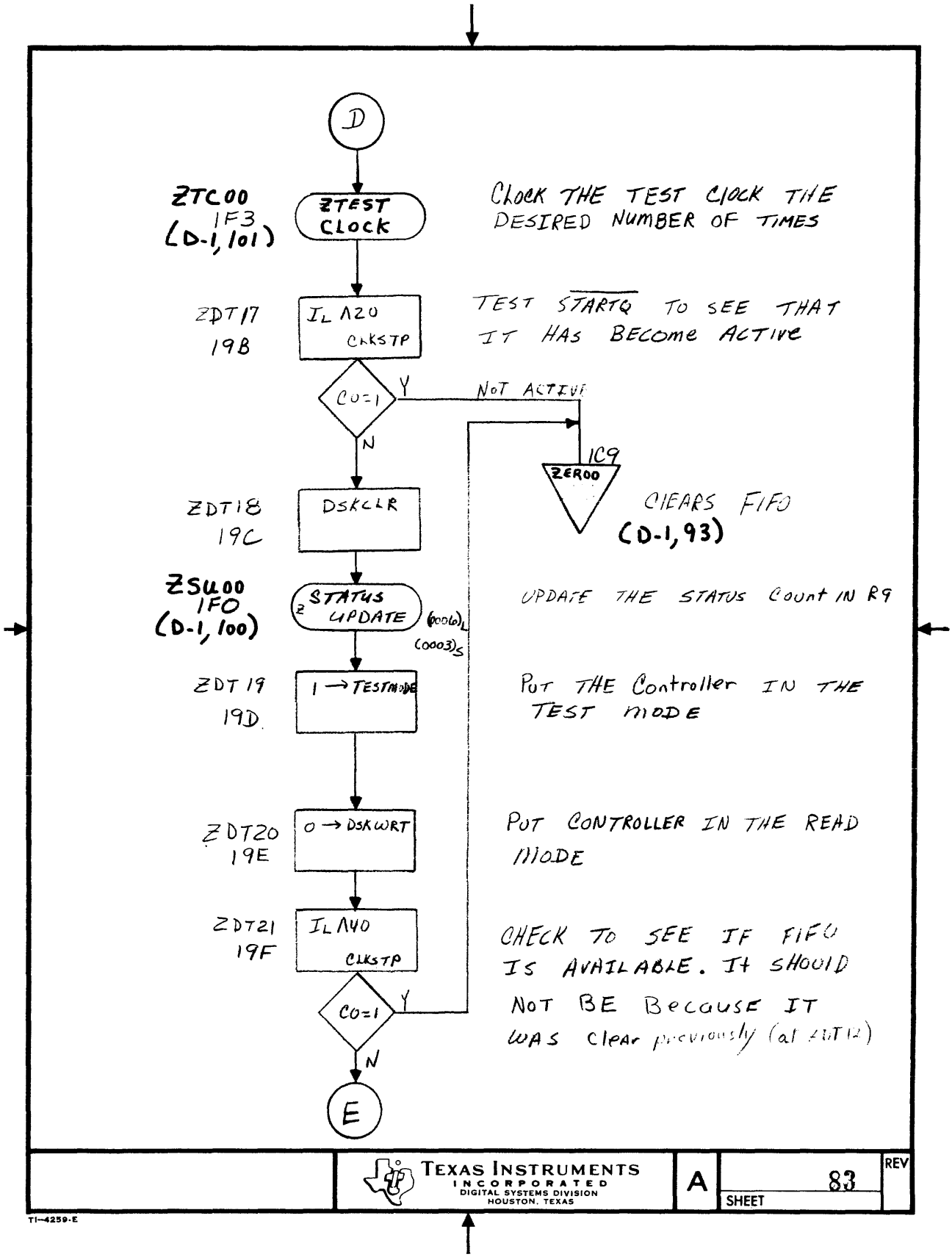


Figure D-1. Microcode Flowcharts (Sheet 83 of 101)

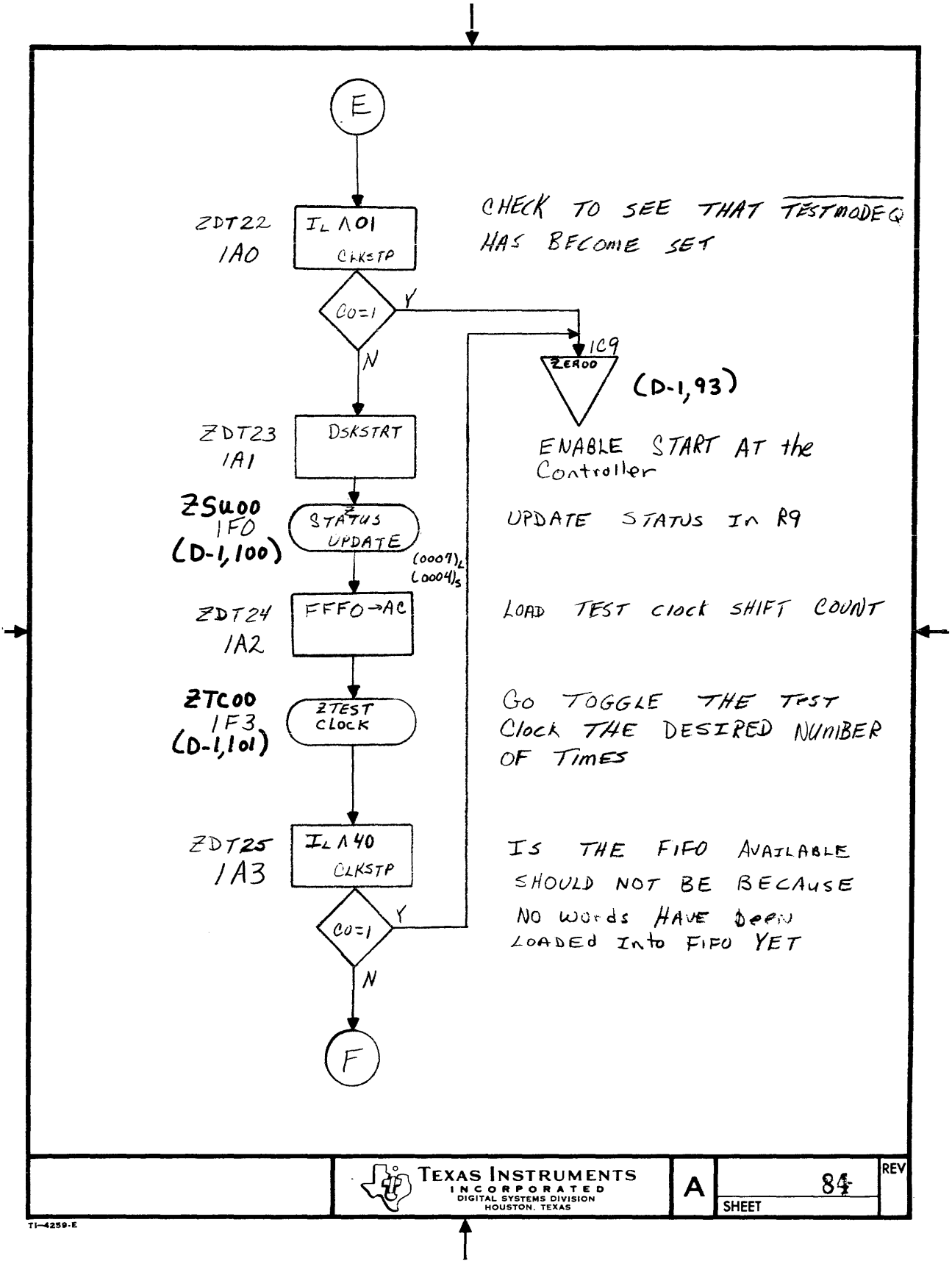


Figure D-1. Microcode Flowcharts (Sheet 84 of 101)

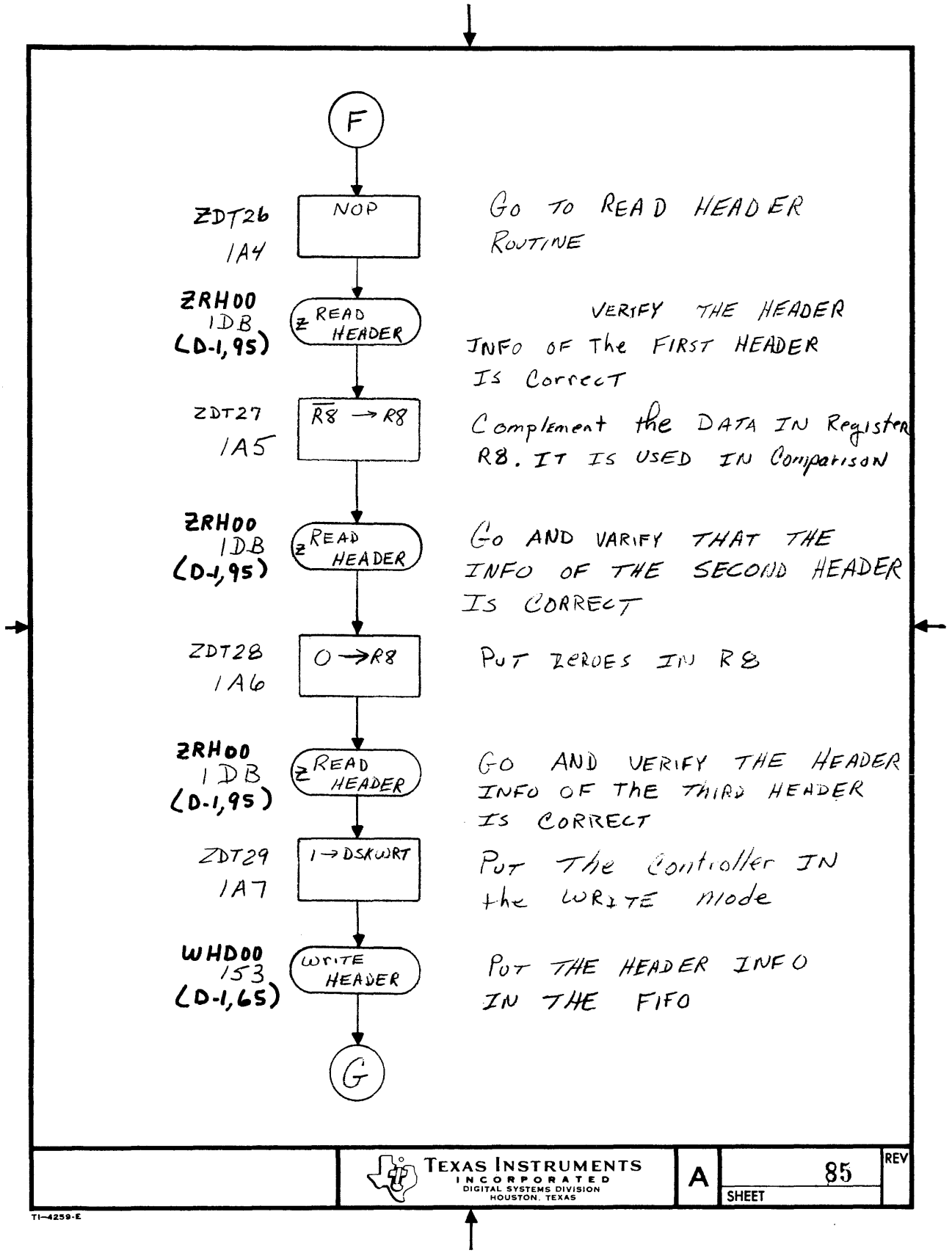


Figure D-1. Microcode Flowcharts (Sheet 85 of 101)

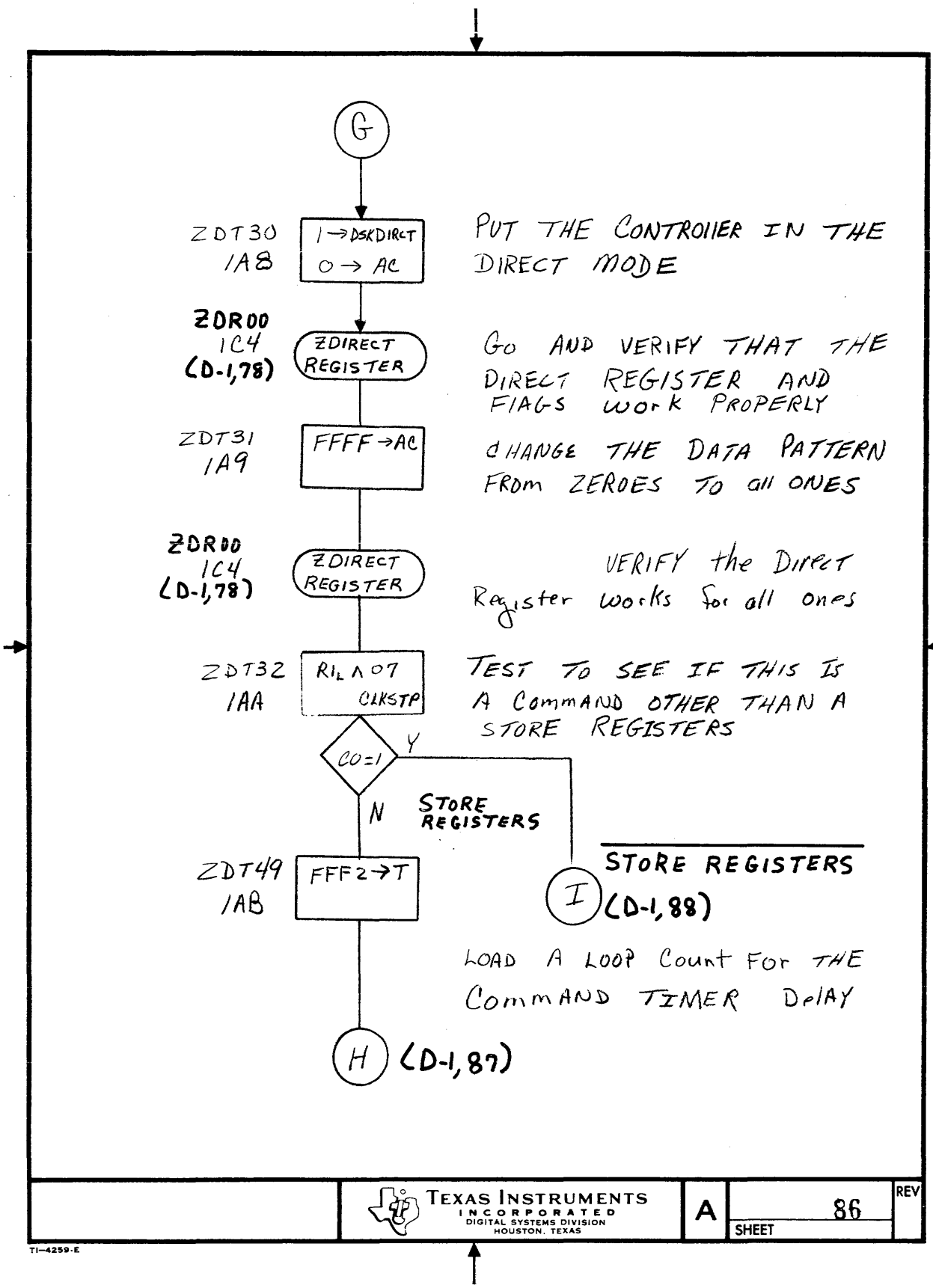


Figure D-1. Microcode Flowcharts (Sheet 86 of 101)

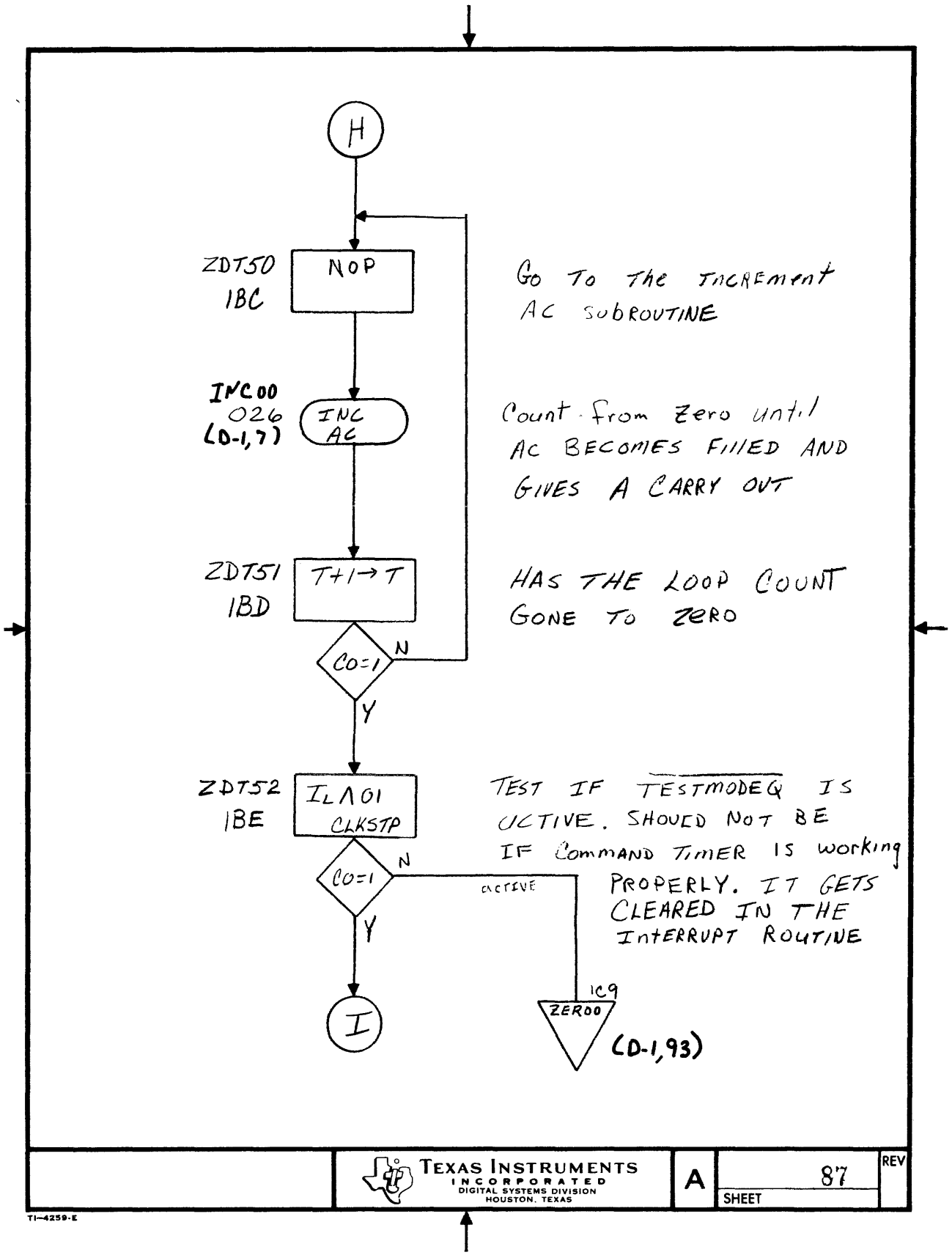


Figure D-1. Microcode Flowcharts (Sheet 87 of 101)

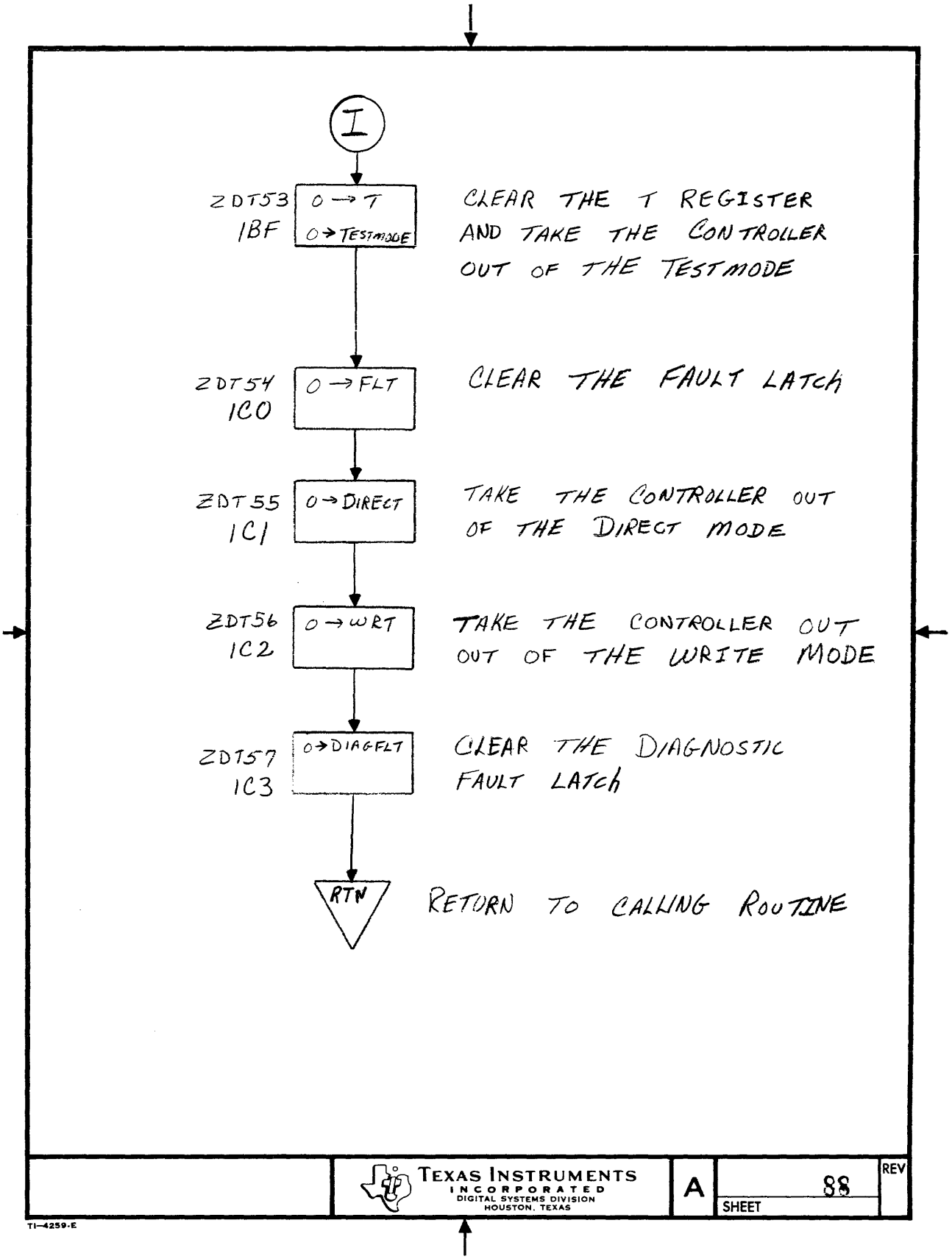


Figure D-1. Microcode Flowcharts (Sheet 88 of 101)

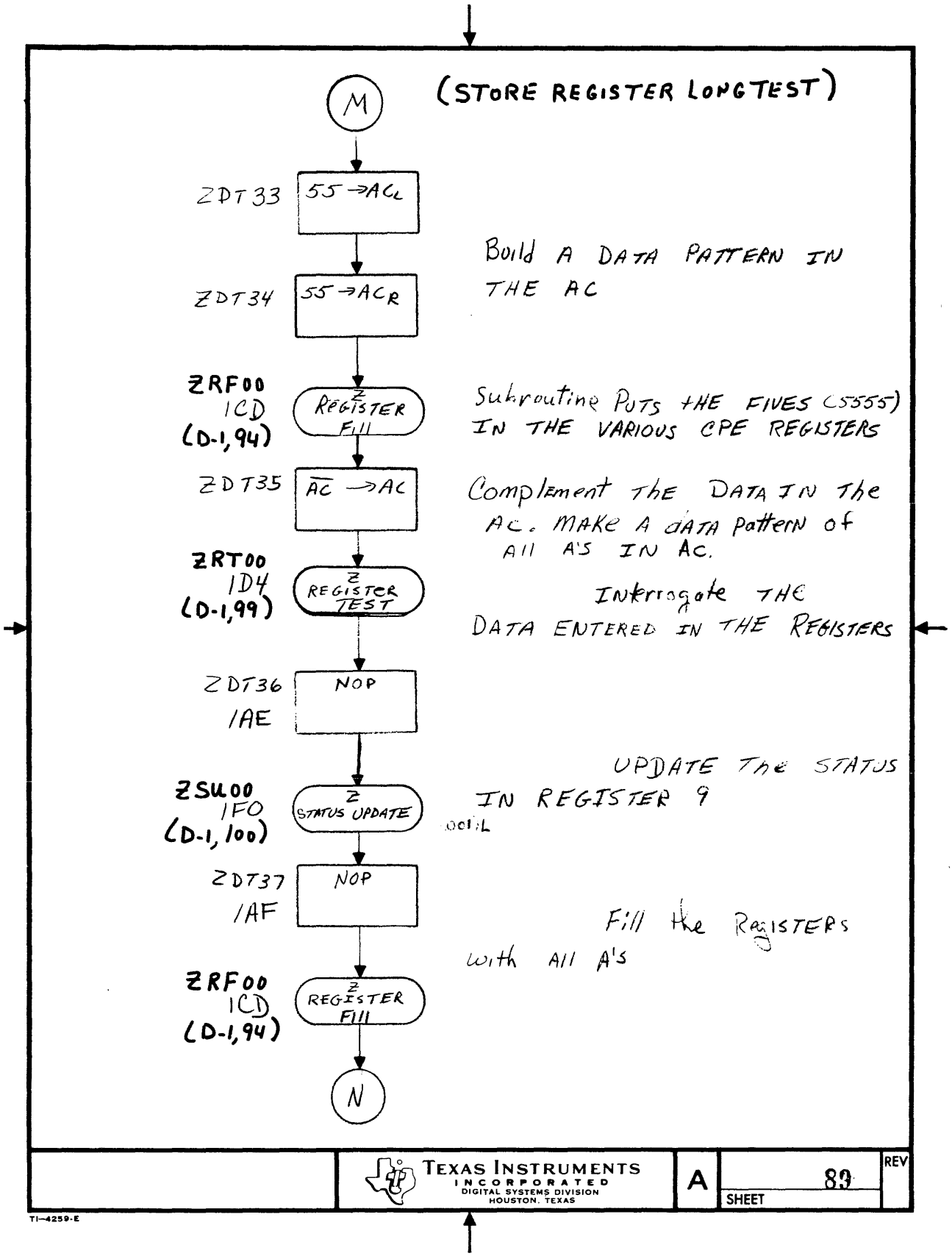


Figure D-1. Microcode Flowcharts (Sheet 89 of 101)

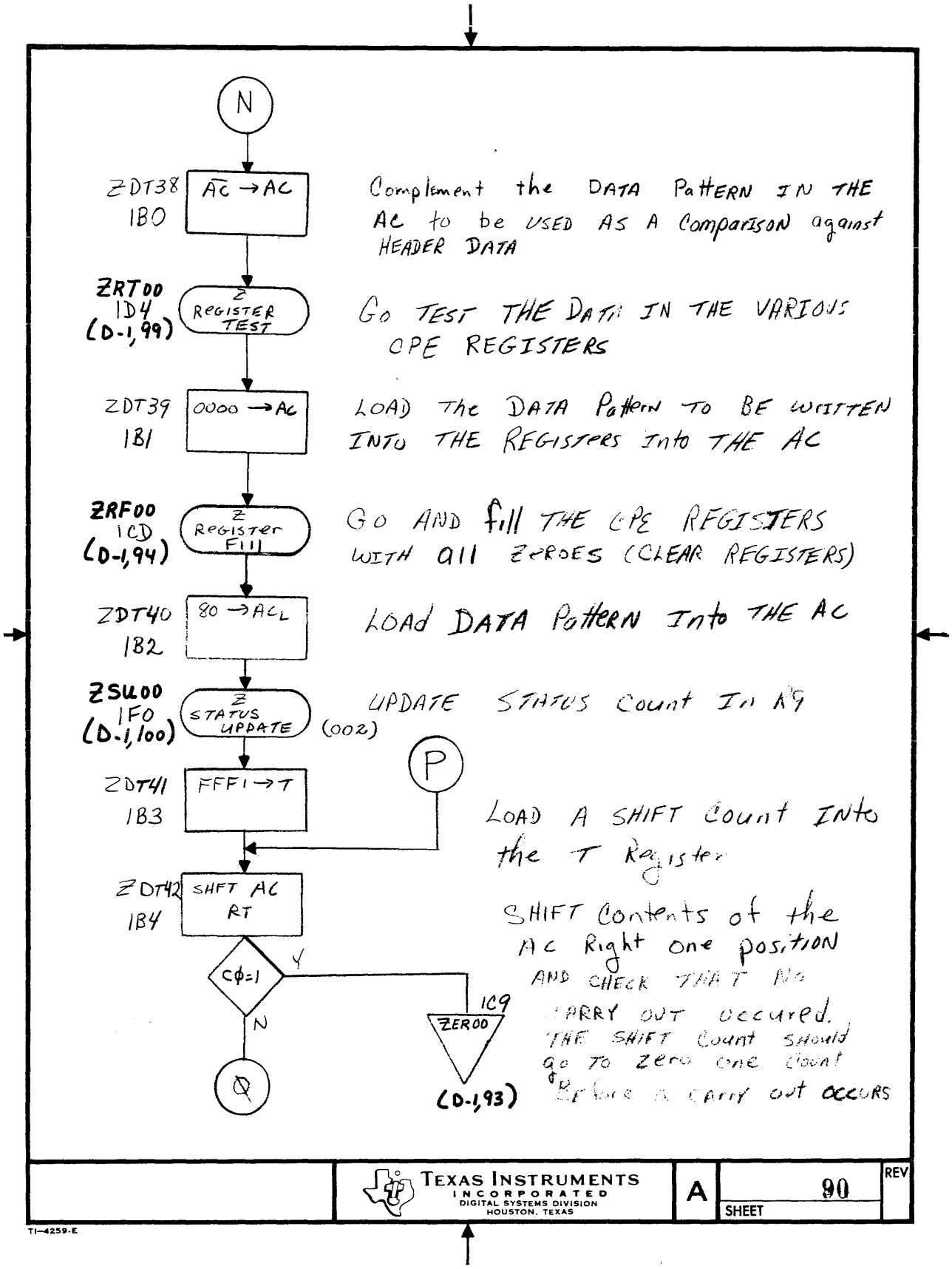


Figure D-1. Microcode Flowcharts (Sheet 90 of 101)

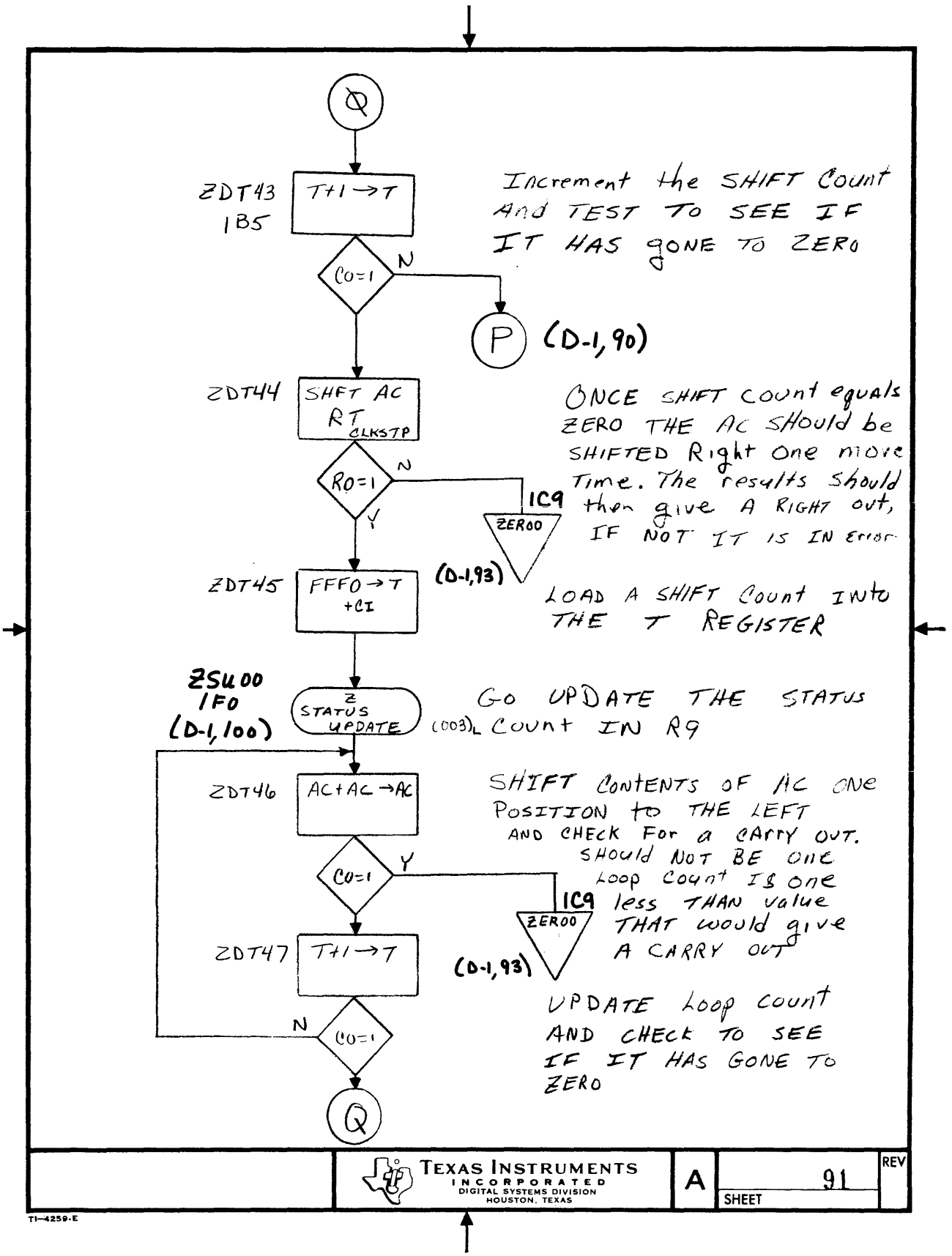


Figure D-1. Microcode Flowcharts (Sheet 91 of 101)

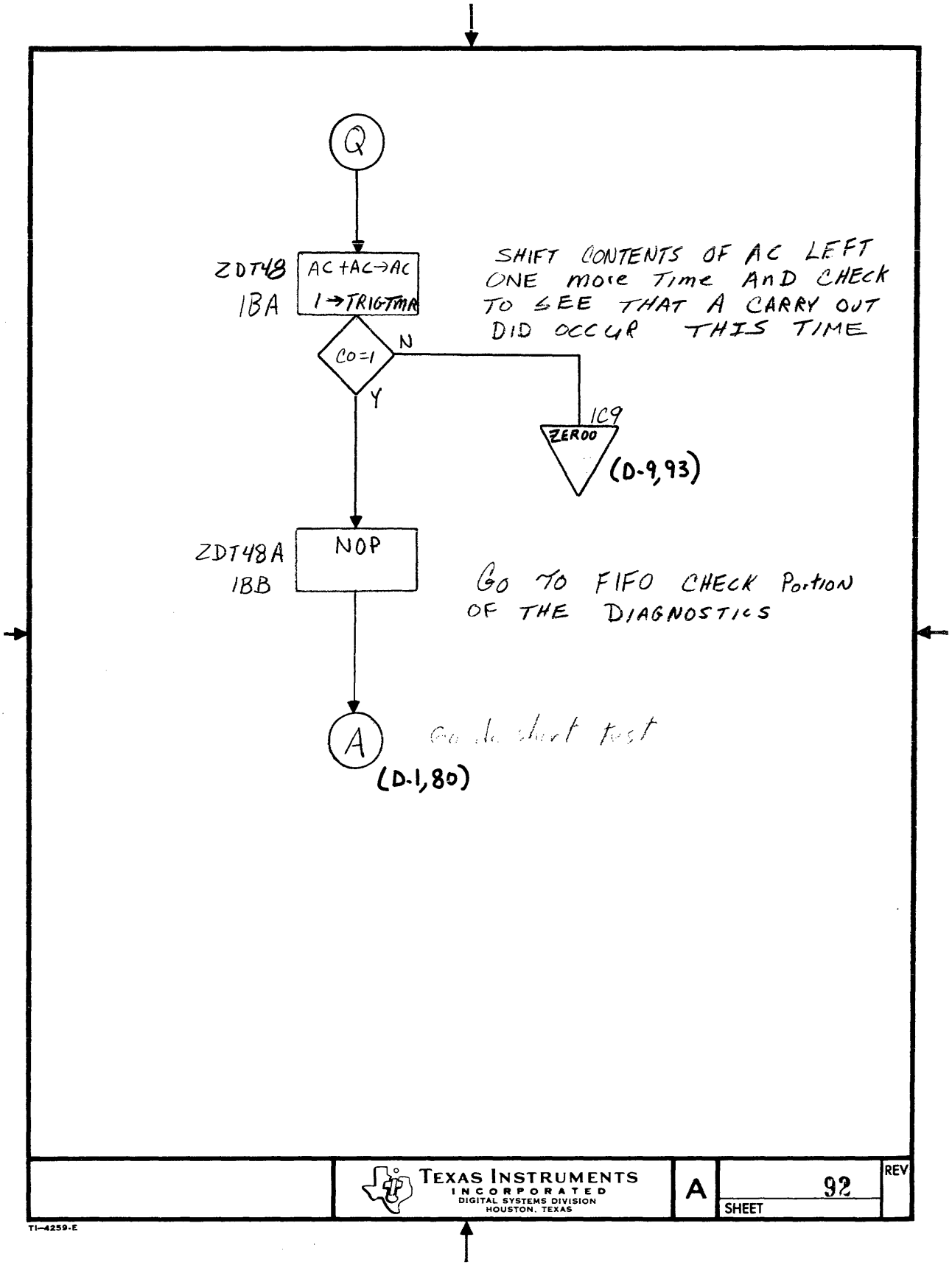


Figure D-1. Microcode Flowcharts (Sheet 92 of 101)

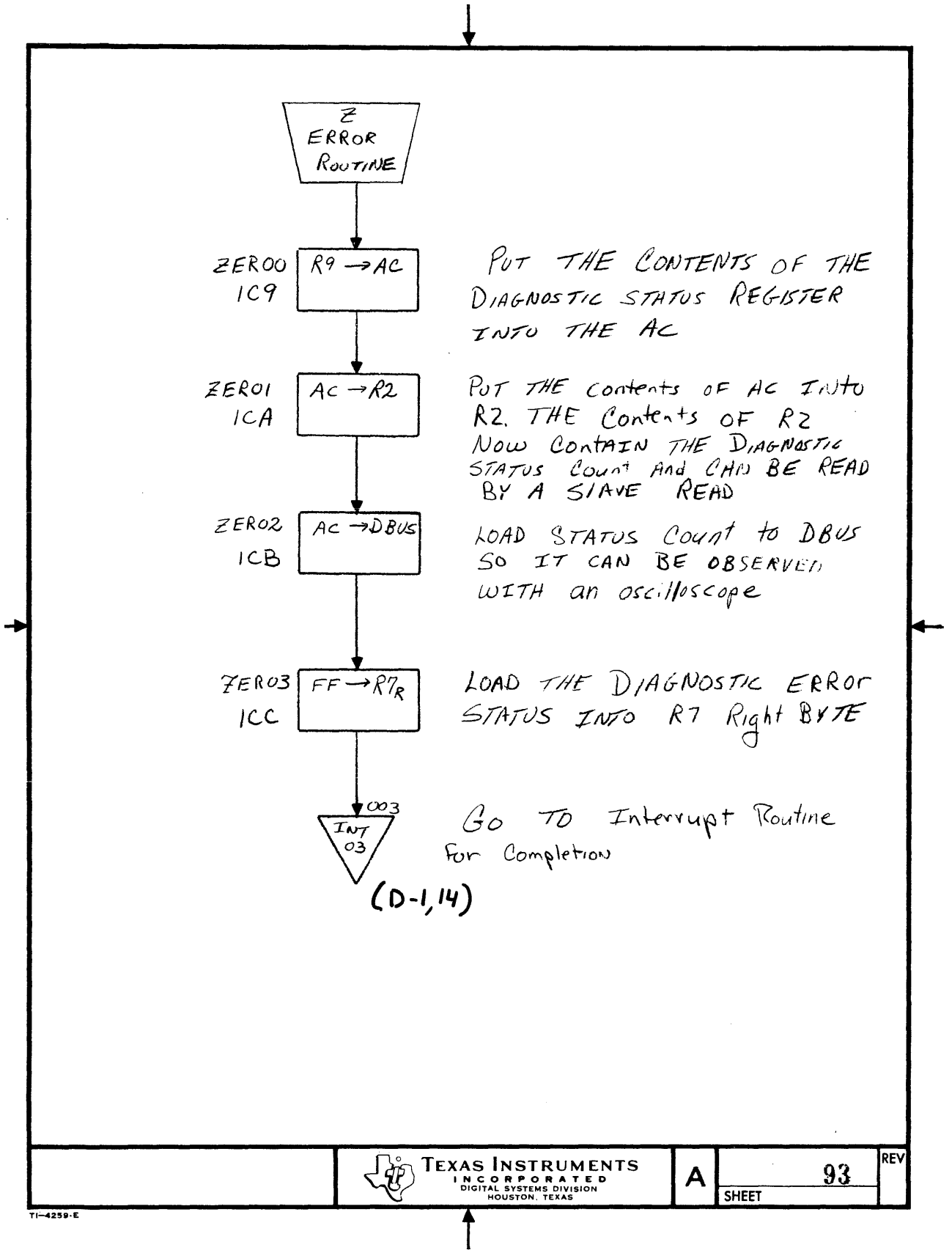


Figure D-1. Microcode Flowcharts (Sheet 93 of 101)

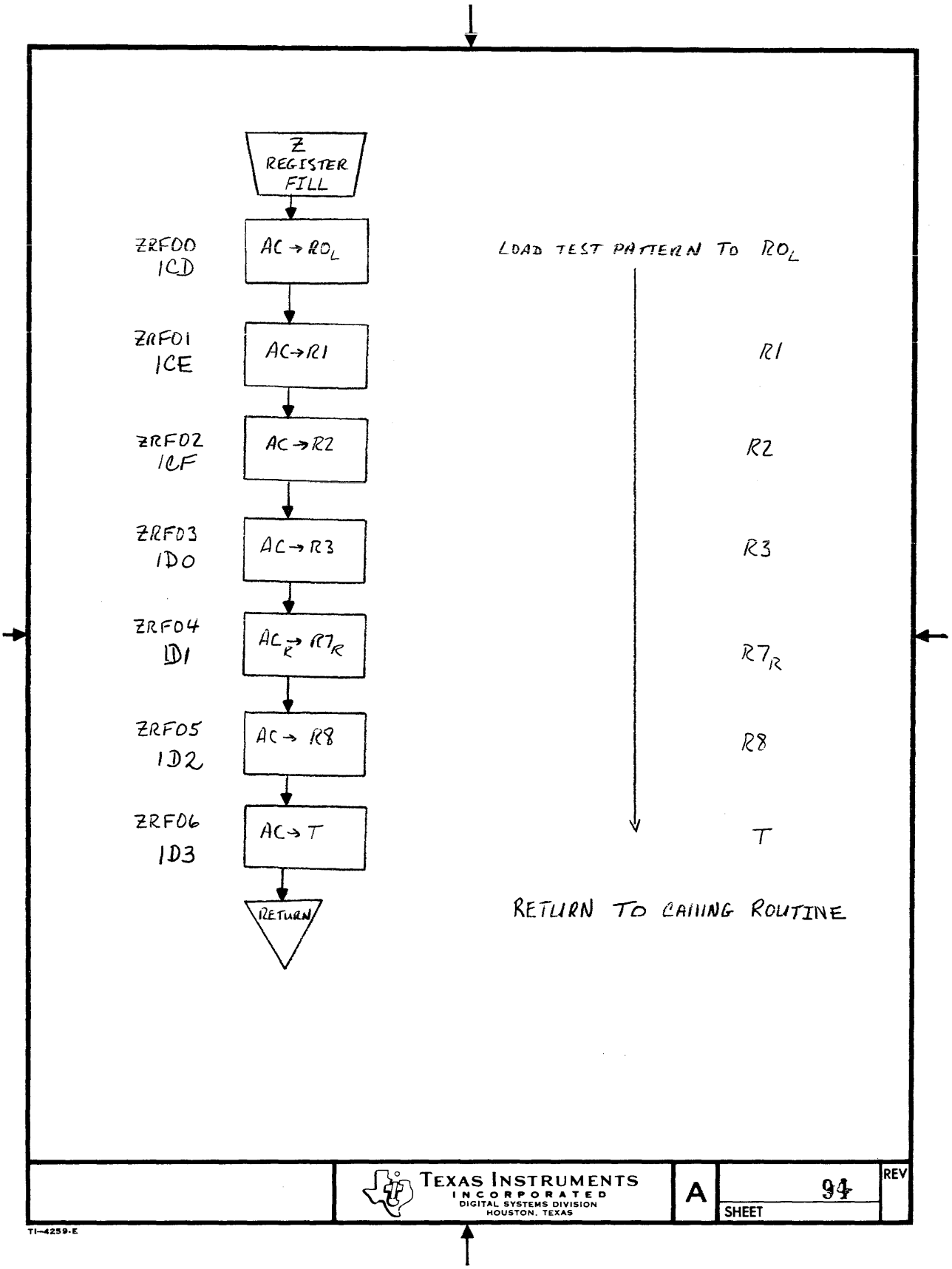


Figure D-1. Microcode Flowcharts (Sheet 94 of 101)

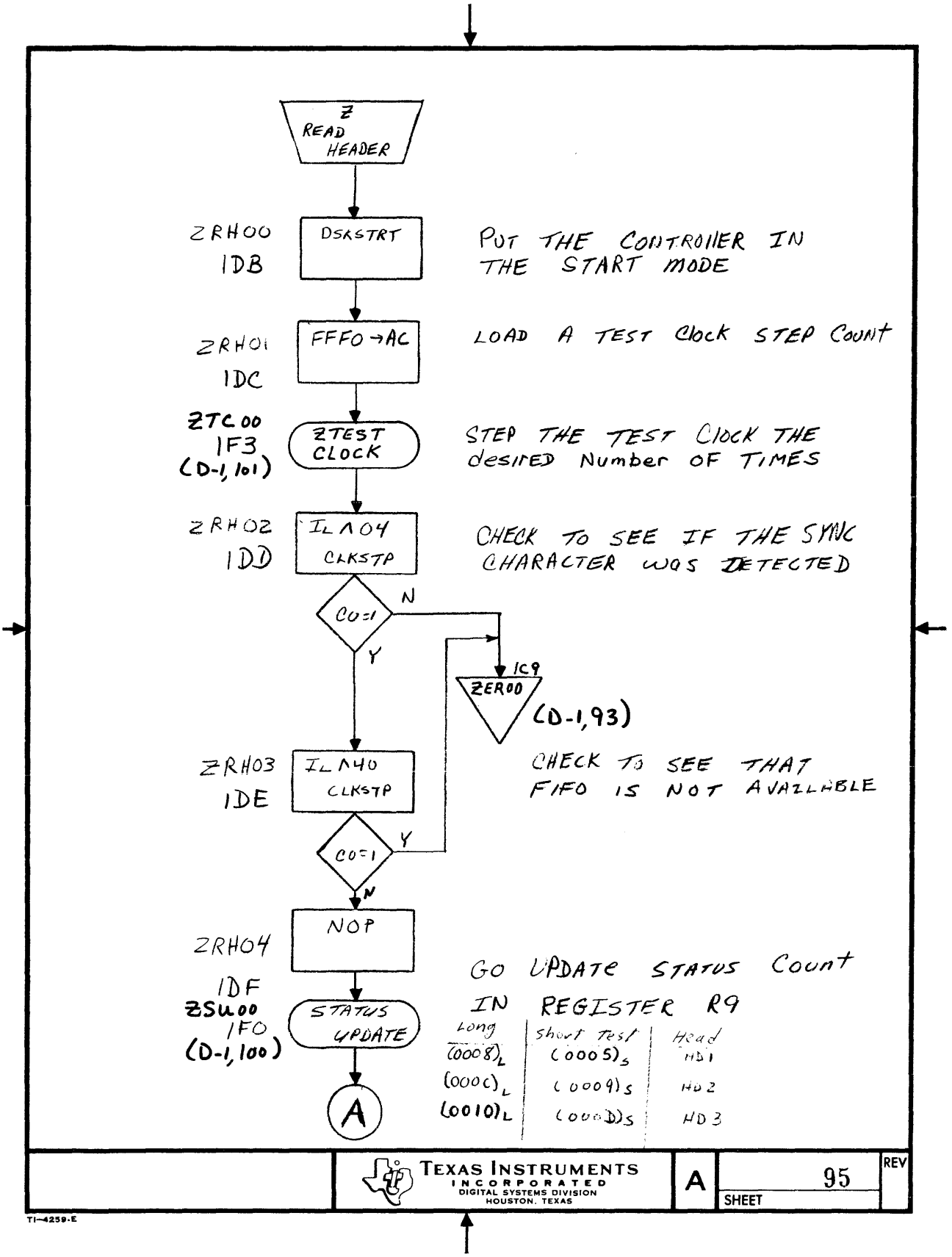


Figure D-1. Microcode Flowcharts (Sheet 95 of 101)

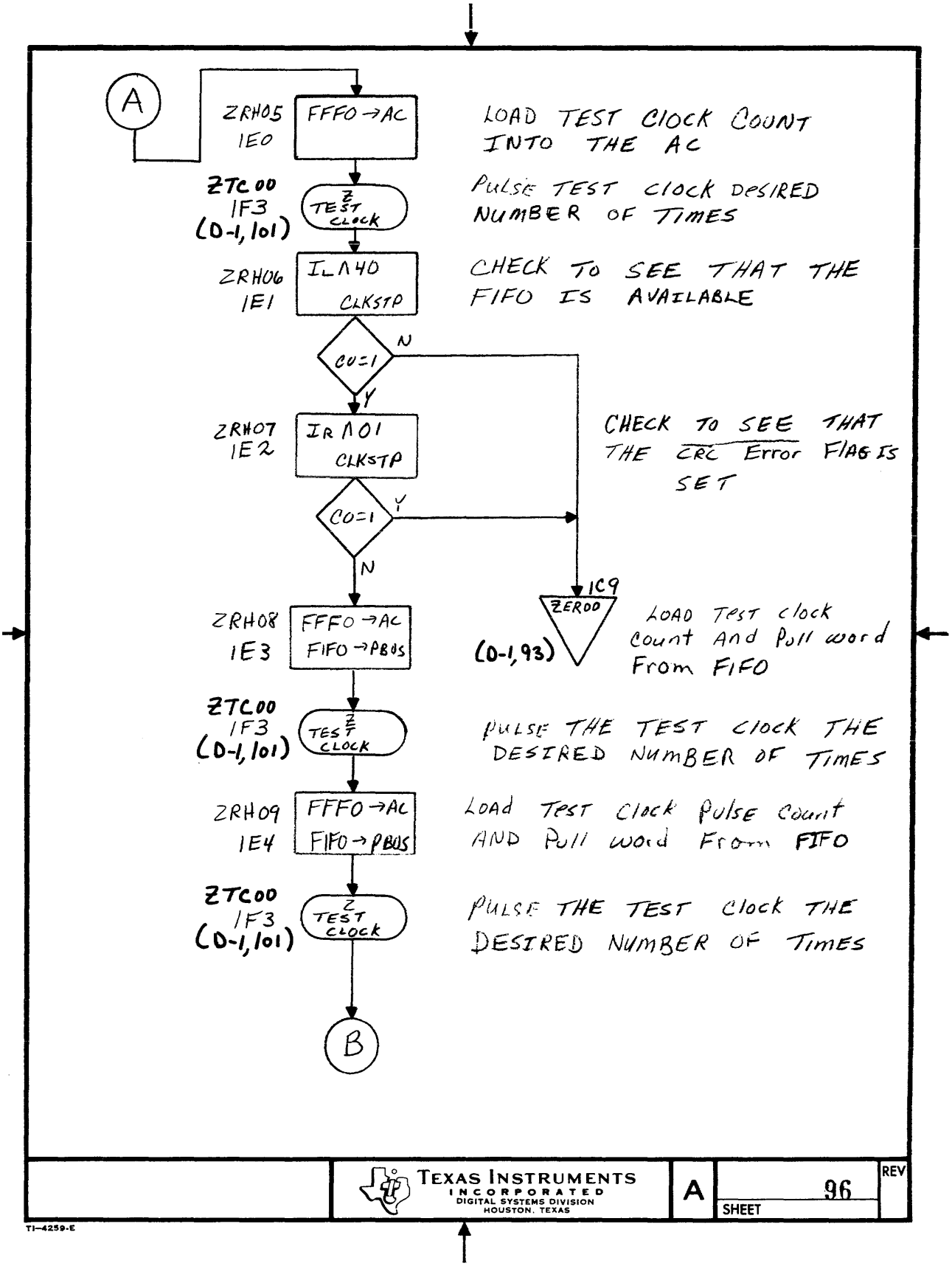


Figure D-1. Microcode Flowcharts (Sheet 96 of 101)

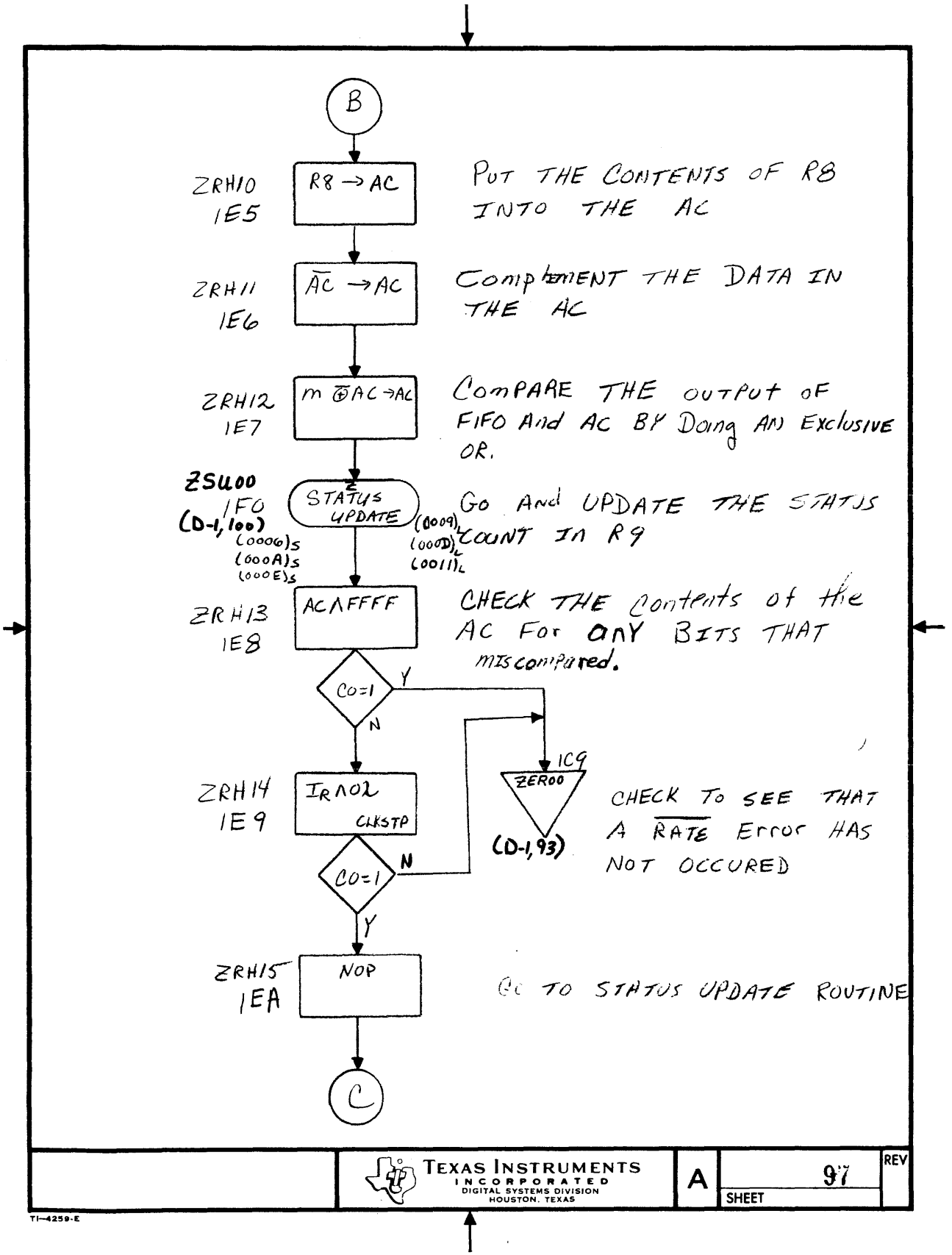


Figure D-1. Microcode Flowcharts (Sheet 97 of 101)

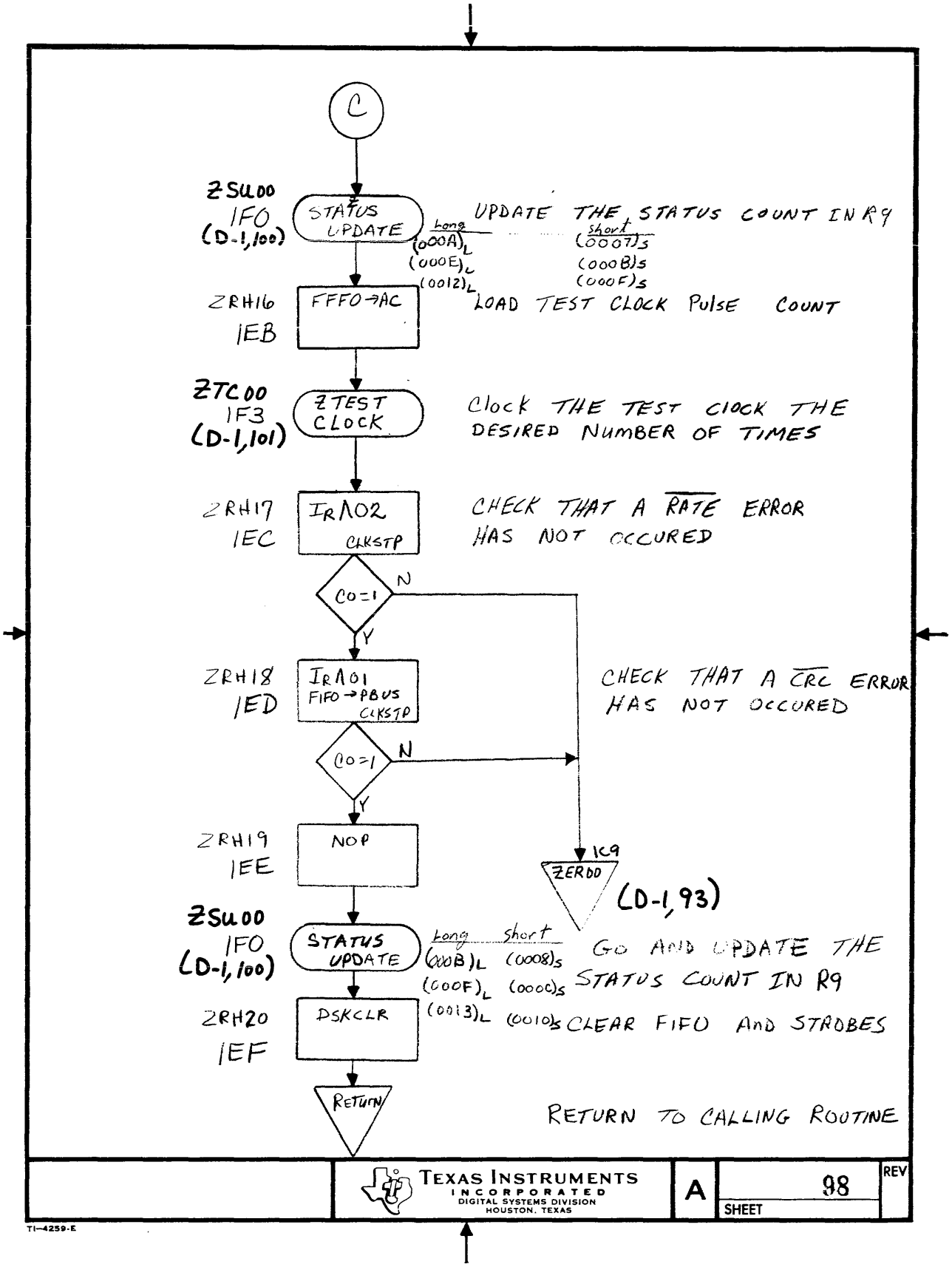


Figure D-1. Microcode Flowcharts (Sheet 98 of 101)

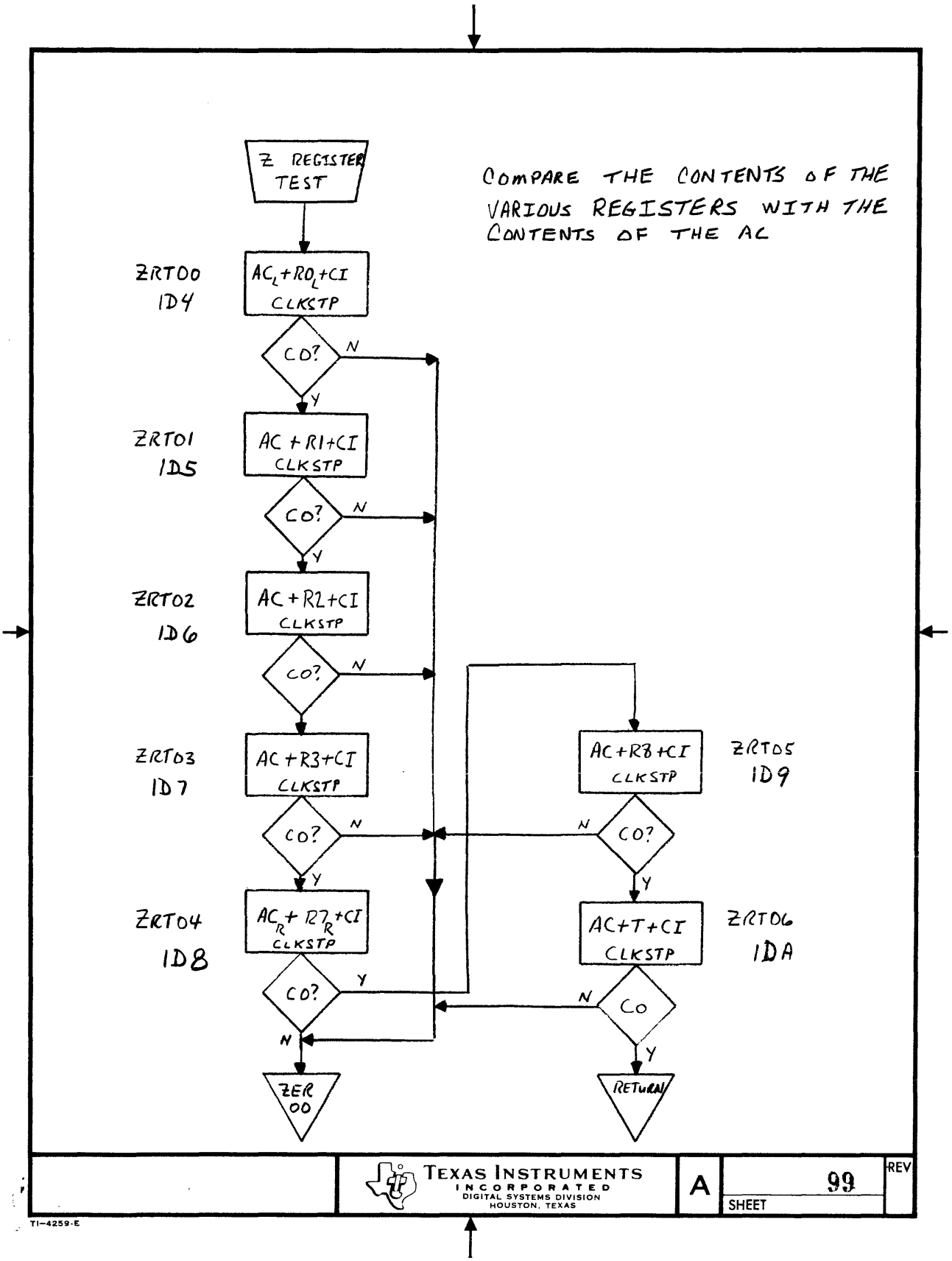


Figure D-1. Microcode Flowcharts (Sheet 99 of 101)

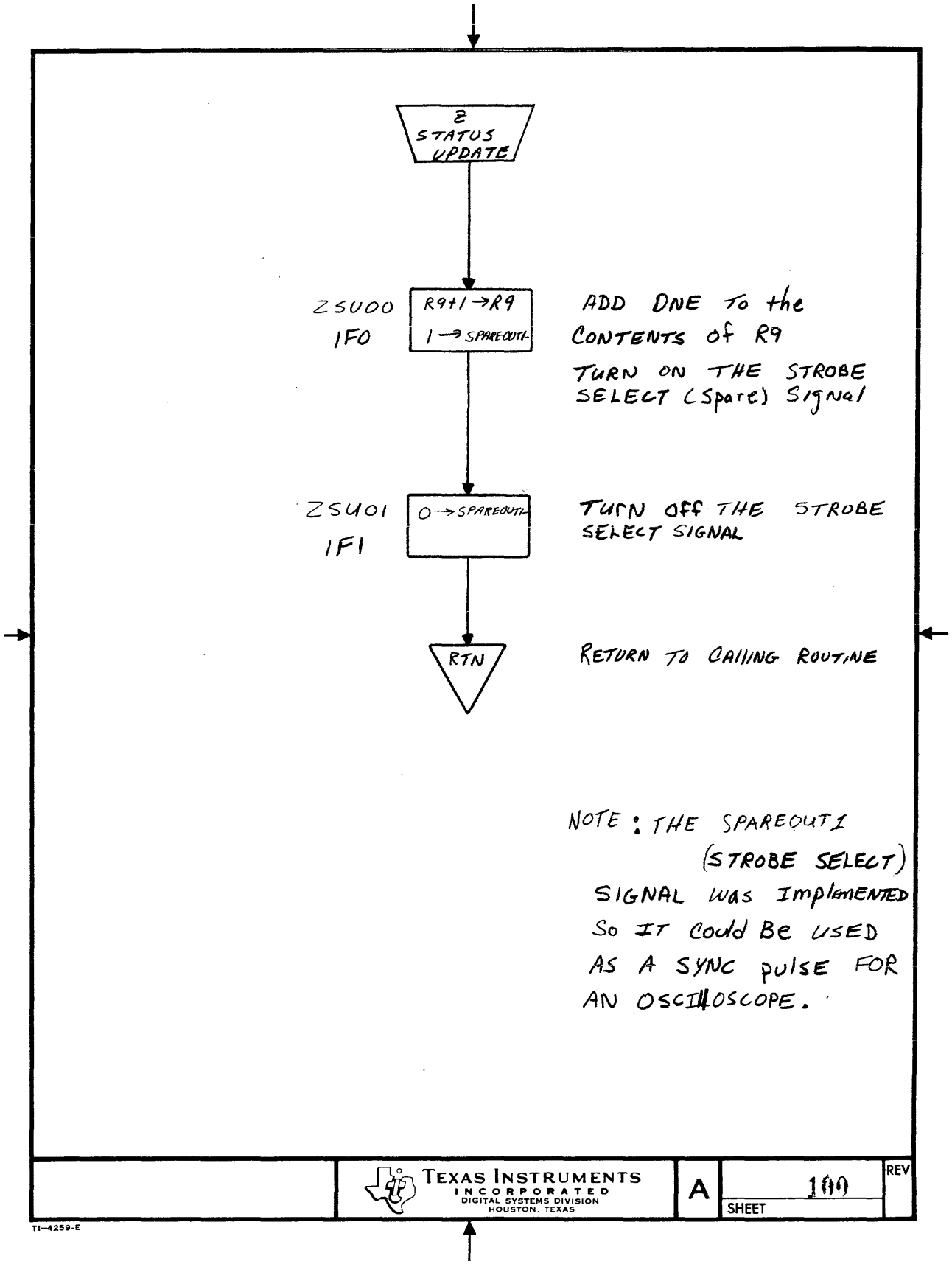


Figure D-1. Microcode Flowcharts (Sheet 100 of 101)

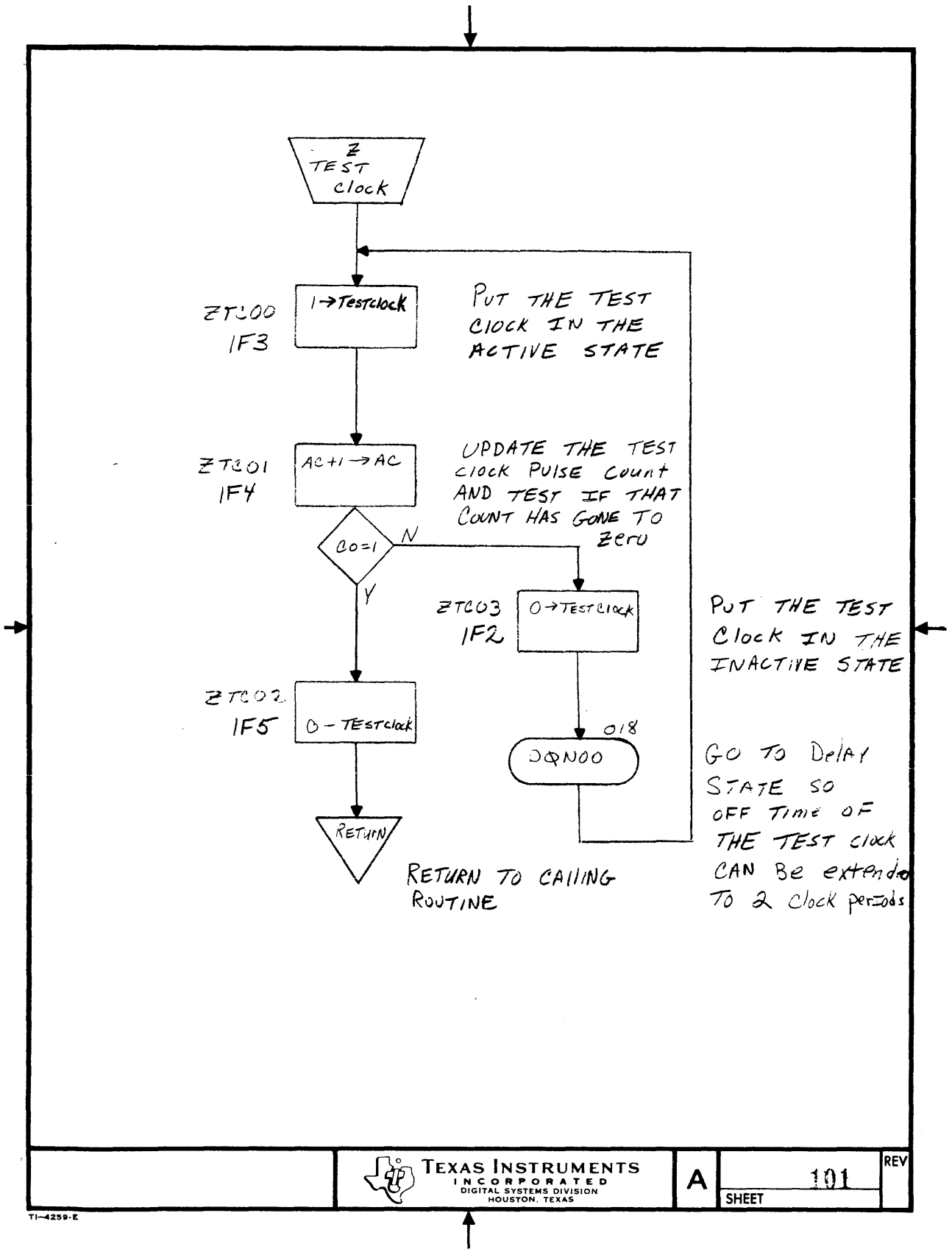


Figure D-1. Microcode Flowcharts (Sheet 101 of 101)

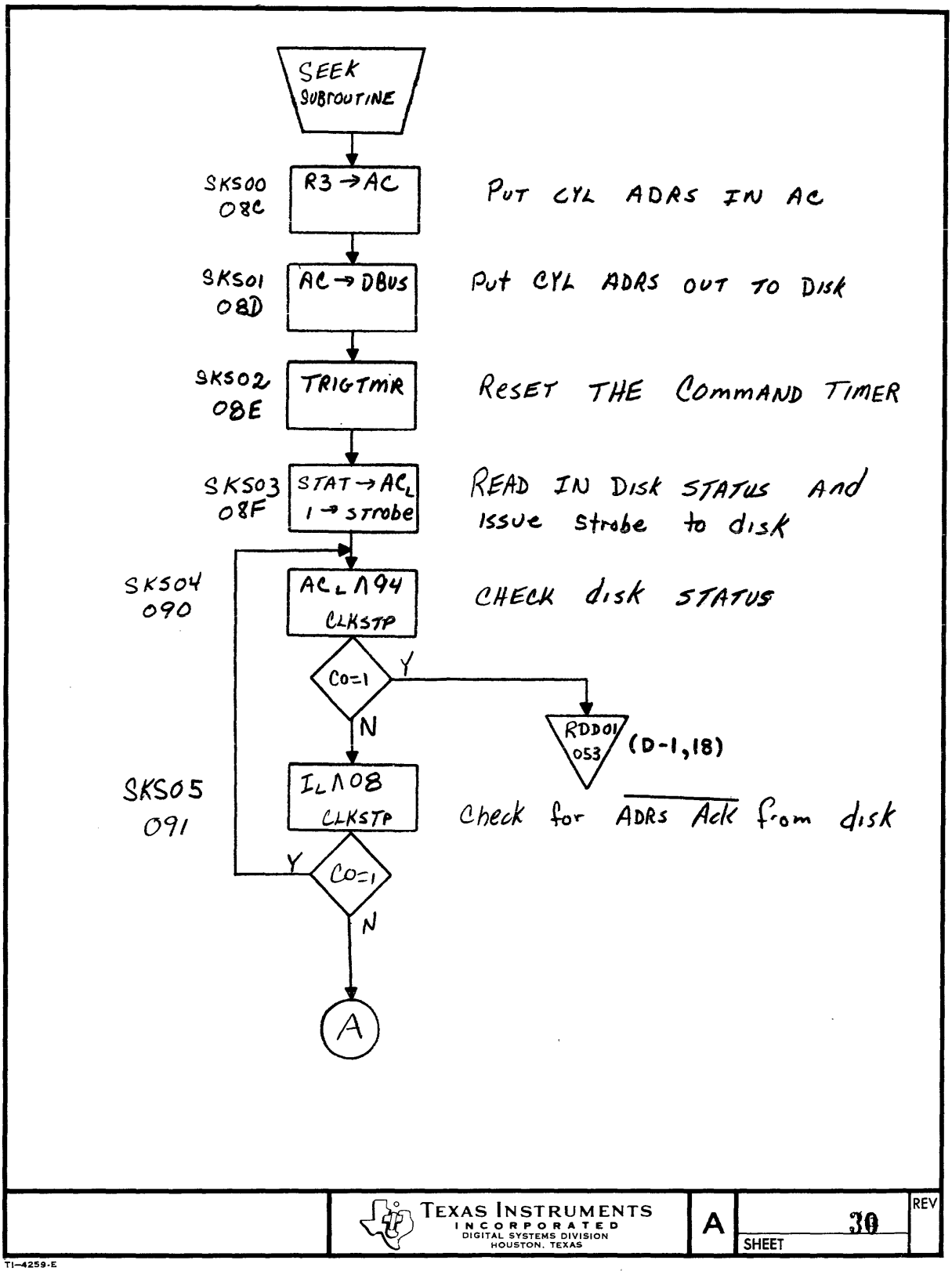


Figure D-2. Flowchart Segments Prior to ECN 428322 (Sheet 1 of 2)

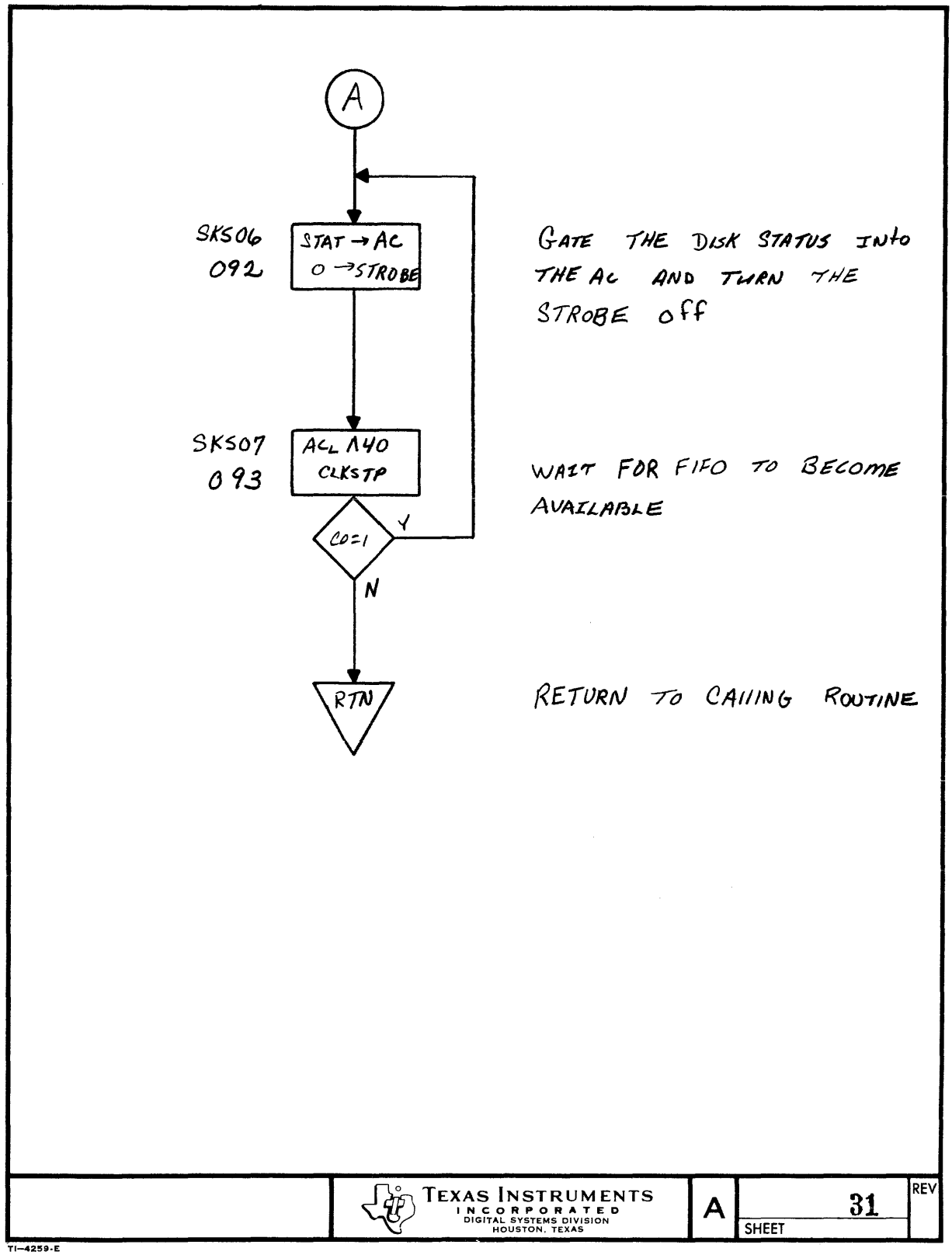


Figure D-2. Flowchart Segments Prior to ECN 428322 (Sheet 2 of 2)

APPENDIX E

ROM MICROCODE LISTING

Table E-1. DS10 Disk Controller ROM Microcode Index (In Order by Address)

Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic
000	INT00	020	INT20	040	INT40	060	RDD23
001	INT01	021	INT21	041	INI16	061	RDD24
002	INT02	022	HCU01	042	INI17	062	RDD25
003	INT03	023	HCU02	043	INI18	063	RDD26
004	INT04	024	HCU03	044	INI19	064	RDD27
005	INT05	025	FAV00	045	INI20	065	RDD28
006	INT41	026	INC00	046	INI21	066	RDD15
007	INT42	027	IDL00	047	INI22	067	RDD16
008	INT43	028	IDL01	048	INI23	068	RDD17
009	INT44	029	IDL02	049	INI24	069	RDD18
00A	INT45	02A	IDL03	04A	INI25	06A	RDD19
00B	CS00	02B	IDL04	04B	INI26	06B	RDD20
00C	CS01	02C	IDL06	04C	INI27	06C	RDD21
00D	CS02	02D	IDL05	04D	INI28	06D	RDD22
00E	CS03	02E	INI00	04E	INI29	06E	RDD14
00F	CS04	02F	INI01	04F	TRM00	06F	RDU00
010	INT10	030	INT30	050	INI30	070	RDU01
011	INT11	031	INT31	051	INI31	071	RDU02
012	CS05	032	INI02	052	RDD00	072	RDU03
013	CS06	033	INI03	053	RDD01	073	RDU04
014	CS07	034	INI04	054	RDD02	074	RDU05
015	CS08	035	INI05	055	RDD03	075	RDU06
016	DST00	036	INI06	056	RDD04	076	RDU07
017	DST01	037	INI07	057	RDD05	077	RDU08
018	DON00	038	INI08	058	RDD06	078	RDU09
019	DWS00	039	INI09	059	RDD07	079	RDU10
01A	DWS01	03A	INI10	05A	RDD08	07A	RST00
01B	DWS02	03B	INI11	05B	RDD09	07B	RST01
01C	DWS03	03C	INI12	05C	RDD10	07C	RST02
01D	HCU00	03D	INI13	05D	RDD11	07D	RST03
01E	HCU04	03E	INI14	05E	RDD12	07E	RST04
01F	HCU05	03F	INI15	05F	RDD13	07F	RST05

Table E-1. DS10 Disk Controller ROM Microcode Index (Continued)
(In Order by Address)

Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic
080	RST07	0A0	SSS00	0C0	STX22	0E0	VID04
081	RST08	0A1	SSS01	0C1	STX23	0E1	VID05
082	RST06	0A2	SSS02	0C2	STX24	0E2	VID06
083	RUP00	0A3	SSS03	0C3	STX25	0E3	VID00
084	RUP01	0A4	SSS04	0C4	STX26	0E4	VID01
085	RUP02	0A5	SSS05	0C5	STX27	0E5	VID02
086	RUP03	0A6	SSS06	0C6	STX28	0E6	VID03
087	RUP04	0A7	SSX00	0C7	TRM01	0E7	VID07
088	RUP05	0A8	SSX01	0C8	TRM02	0E8	VID08
089	SDS00	0A9	SSX02	0C9	TRM03	0E9	VID09
08A	SDS01	0AA	STX00	0CA	TRM04	0EA	VID10
08B	SDS02	0AB	STX01	0CB	TRM05	0EB	VID11
08C	SKS00	0AC	STX02	0CC	TRM06	0EC	VID12
08D	SKS01	0AD	STX03	0CD	TRM07	0ED	N/A
08E	SKS02	0AE	STX04	0CE	TRM08	0EE	VID14
08F	SKS03	0AF	STX05	0CF	TRM09	0EF	VID15
090	SKS04	0B0	STX06	0D0	TRM10	0F0	SRD00
091	SKS05	0B1	STX07	0D1	TRM11	0F1	SRD10
092	SKS06	0B2	STX08	0D2	TRM12	0F2	SRD20
093	SKS07	0B3	STX09	0D3	TRM13	0F3	SRD30
094	SRG00	0B4	STX10	0D4	TRM14	0F4	SRD40
095	SRG01	0B5	STX11	0D5	TRM15	0F5	SRD50
096	SRG02	0B6	STX12	0D6	TRM16	0F6	SRD60
097	SRG03	0B7	STX1B	0D7	TRM17	0F7	SRD70
098	SRG04	0B8	STX14	0D8	TRM18	0F8	SWR00
099	SRG05	0B9	STX15	0D9	TRM19	0F9	SWR10
09A	SRG06	0BA	STX16	0DA	TRM20	0FA	SWR20
09B	SRG07	0BB	STX10	0DB	TRM21	0FB	SWR30
09C	SRW00	0BC	STX18	0DC	TRM22	0FC	SWR40
09D	SRW01	0BD	STX19	0DD	TRM23	0FD	SWR50
09E	SRW02	0BE	STX20	0DE	TRM24	0FE	SWR60
09F	SRW03	0BF	STX21	0DF	TRM25	0FF	SWR70

Table E-1. DS10 Disk Controller ROM Microcode Index (Continued)
(In Order by Address)

Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic
100	SRD01	120	VID19	140	WFT12	160	WRD04
101	SRD02	121	VID20	141	WFT13	161	WRD06
102	SRD03	122	VID21	142	WFT14	162	WRD07
103	SRD71	123	VID22	143	WFT15	163	WRD08
104	SRD72	124	VID23	144	WFT16	164	WRD09
105	SRD80	125	VID24	145	WFT17	165	WRD10
106	SWR01	126	VID25	146	WFT18	166	WRD11
107	SWR02	127	VID26	147	WFT19	167	WRD12
108	SWR11	128	VID27	148	WFT20	168	WRD13
109	SWR21	129	VID28	149	WFT21	169	WRD14
10A	SWR31	12A	VID29	14A	WFT22	16A	WRD15
10B	SWR41	12B	WCS00	14B	WFT23	16B	WRD25
10C	SWR51	12C	WCS01	14C	WFT24	16C	WRD26
10D	SWR71	12D	WCS02	14D	WFT25	16D	WRD27
10E	SWR61	12E	WCS03	14E	WFT26	16E	WRD17
10F	SWR62	12F	WCS04	14F	WFT27	16F	WRD18
110	SWR63	13D	WCS05	150	SKS07A	170	WRD19
111	SWR64	131	WCS06	151	WFT29	171	WRD20
112	SWR65	132	WCS07	152	WFT30	172	WRD21
113	SWR66	133	WCS08	153	WHD00	173	WRD22
114	SWR67	134	WFT00	154	WHD01	174	WRD23
115	SWR68	135	WFT01	155	WHD02	175	WRD24
116	SWR69	136	WFT02	156	WHD03	176	WRD16
117	SWR6A	137	WFT03	157	WHD03	177	WRD05
118	SWR6B	138	WFT04	158	WHD05	178	WRU00
119	SWR6C	139	WFT05	159	WHD06	170	WRU01
11A	SWR6D	13A	WFT06	15A	WHD07	17A	WRU02
11B	SWR6E	13B	WFT07	15B	WHD08	17B	WRU03
11C	SWR6F	13C	WFT08	15C	WRD00	17C	WRU04
11D	VID16	13D	WFT09	15D	WRD01	17D	WRU05
11E	VID17	13E	WFT10	15E	WRD02	17E	WRU05
11F	VID18	13F	WFT11	15F	WRD03	17F	WRU07

Table E-1. DS10 Disk Controller ROM Microcode Index (Continued)
(In Order by Address)

Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic	Address	Instruction Mnemonic
180	WRU08	1A0	ZDT22	1C0	ZDT54	1E0	ZRH05
181	WRU09	1A1	ZDT23	1C1	ZDT55	1E1	ZRH06
182	WRU10	1A2	ZDT24	1C2	ZDT56	1E2	ZRH07
183	WRU11	1A3	ZDT25	1C3	ZDT57	1E3	ZRH08
184	WRU12	1A4	ZDT26	1C4	ZDR00	1E4	ZRH09
185	WRU13	1A5	ZDT27	1C5	ZDR01	1E5	ZRH10
186	WST00	1A6	ZDT28	1C6	ZDR02	1E6	ZRH11
187	WST01	1A7	ZDT29	1C7	ZDR03	1E7	ZRH12
188	WST02	1A8	ZDT30	1C8	ZDR04	1E8	ZRH13
189	WST03	1A9	ZDT31	1C9	ZER00	1E9	ZRH14
18A	ZDT00	1AA	ZDT32	1C2	ZER01	1EA	ZRH15
18B	ZDT01	1AB	ZDT49	1CB	ZER02	1EB	ZRH15
18C	ZDT02	1AC	ZDT34	1CC	ZER03	1EC	ZRH17
18D	ZDT03	1AD	ZDT35	1CD	ZRF00	1ED	ZRH18
18E	ZDT04	1AE	ZDT36	1CE	ZRF01	1EE	ZRH19
18F	ZDT05	1AF	ZDT37	1CF	ZRF02	1EF	ZRH20
190	ZDT06	1B0	ZDT38	1D0	ZRF03	1F0	ZSU00
191	ZDT07	1B1	ZDT39	1D1	ZRF04	1F1	ZSU01
192	ZDT08	1B2	ZDT40	1D2	ZRF05	1F2	ZTC03
193	ZDT09	1B3	ZDT41	1D3	ZRF06	1F3	ZTC00
194	ZDT10	1B4	ZDT42	1D4	ZRT00	1F4	ZTC01
195	ZDT11	1B5	ZDT43	1D5	ZRT01	1F5	ZTC02
196	ZDT12	1B6	ZDT44	1D6	ZRT02	1F6	ZAC00
197	ZDT13	1B7	ZDT45	1D7	ZRT03	1F7	ZAC01
198	ZDT14	1B8	ZDT46	1D8	ZRT04	1F8	ZDT33
199	ZDT15	1B9	ZDT47	1D9	ZRT05	1F9	LTC00
19A	ZDT16	1BA	ZDT48	1DA	ZRT06	1FA	LTC01
19B	ZDT17	1BB	ZDT48A	1DB	ZRH00	1FB	N/A
19C	ZDT18	1BC	ZDT50	1DC	ZRH01	1FC	N/A
19D	ZDT19	1BD	ZDT51	1DD	ZRH02	1FD	N/A
19E	ZDT20	1BE	ZDT52	1DE	ZRH03	1FE	N/A
19F	ZDT21	1BF	ZDT53	1DF	ZRH04	1FF	N/A

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	CI	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	
0B	0	1010000	10	0		000	0	100	00	0000100101	00000110	; CCS00
0C	1	0101111	11	11	0	000	0	010	00	0000001110	11111101	; CCS01
0D	0	0010111	11	11	1	000	0	001	00	0000010010	11110111	; CCS02
0E	1	1101111	11	11	1	000	0	010	00	0000010100	11111110	; CCS03
0F	0	0010111	11	11	1	000	0	001	00	0000010010	10111111	; CCS04
12	1	0000000	00	00	1	000	0	000	00	0000000000	00000100	; CCS05
13	1	0000000	00	00	1	000	0	001	00	0001001111	00101000	; CCS06
14	1	0000000	00	00	1	000	0	000	00	0000000000	00000100	; CCS07
15	1	0000000	00	00	1	000	0	111	00	0000000000	00101000	; CCS08
18	1	0000000	00	00	1	000	0	111	00	0000000000	00000000	; DON00
16	0	0111110	11	01	0	000	0	011	00	0000010110	00000000	; DST00
17	1	0000000	00	00	1	000	0	100	00	0000011000	00001000	; DST01
19	1	0000000	00	00	1	000	0	000	00	0000000000	00010101	; DWS00
1A	1	0000000	00	00	1	000	0	000	00	0000000000	00100111	; DWS01
1B	0	0011011	00	11	1	000	0	100	00	0000100110	00010110	; DWS02
1C	1	0000000	00	00	1	000	0	111	00	0000000000	00100101	; DWS03
25	1	1101111	10	10	1	000	0	101	00	0000100101	10111111	; FAV00
1D	1	1010011	10	10	1	000	0	011	00	0000100010	11110111	; HCU00
22	0	0010011	10	10	1	000	0	000	00	0000000000	11110111	; HCU01
23	0	0011011	00	11	1	000	0	000	00	0000000000	00100010	; HCU02
24	0	0111111	00	01	0	000	0	101	00	0000100100	00101101	; HCU03
1E	0	1010011	10	10	1	000	0	000	00	0000000000	11111000	; HCU04
1F	0	0110011	00	01	0	000	0	001	00	0010001100	00101100	; HCU05
27	1	0000000	00	01	1	000	1	000	00	0000000000	00001010	; IDL00
28	1	1010111	10	10	1	000	1	011	00	0000101110	01111111	; IDL01
29	1	1010111	10	10	1	000	1	011	00	0000101011	10011111	; IDL02
2A	1	1010111	10	10	1	000	1	010	00	0000101101	11101111	; IDL03
2B	1	1010000	11	10	1	000	1	010	00	0000101101	11110000	; IDL04
2D	1	0000000	00	00	1	000	1	001	00	0000100111	00011001	; IDL05
2C	1	0000000	00	00	1	000	1	001	00	0000100111	00011000	; IDL06
2E	0	1010000	10	01	1	000	0	000	00	0000000000	00011010	; INI00
2F	0	1010111	11	01	1	000	0	001	00	0000110010	00011000	; INI01
32	0	1010111	10	10	1	000	0	100	00	0110001010	11101111	; INI02
33	1	1010001	11	11	1	000	0	010	00	0000110101	11111110	; INI03
34	1	0000000	00	00	1	000	0	001	00	0000110111	00101100	; INI04
35	0	0010011	10	10	1	000	0	000	00	0000000000	11110111	; INI05
36	1	0000000	00	00	1	000	0	000	00	0000000000	00101101	; INI06
37	0	0000101	00	01	1	000	0	000	00	0000000000	00000010	; INI07
38	0	0001111	00	01	1	000	0	000	00	0000000000	00000000	; INI08
39	0	0100101	00	00	0	000	0	000	00	0000000000	00000000	; INI09
3A	1	0010010	10	10	1	000	0	010	00	0000001001	00010100	; INI10
3B	0	0000010	10	01	1	000	0	000	00	0000000000	00000000	; INI11
3C	0	0011011	11	11	1	000	0	000	00	0000000000	01111111	; INI12
3D	0	0001111	00	01	1	000	0	011	00	0000111101	00000000	; INI13
3E	0	0100001	11	00	0	000	0	000	00	0000000000	00000000	; INI14
3F	0	0000110	11	01	1	000	0	001	00	0001000001	00000000	; INI15
41	0	0001111	11	01	1	000	0	011	00	0001000011	00000000	; INI16
42	0	0010101	10	10	1	000	0	000	00	0000000000	01111111	; INI17
43	0	0100110	11	11	0	000	0	000	00	0000000000	11110000	; INI18
44	0	0000100	00	01	1	000	0	000	00	0000000000	00000000	; INI19
45	0	0001111	00	01	1	000	0	000	00	0000000000	00000000	; INI20
46	0	0011111	00	01	0	000	0	000	00	0000000000	00000000	; INI21
47	0	0100100	00	00	0	000	0	000	00	0000000000	00000000	; INI22
48	0	1011011	00	00	1	110	0	000	00	0000000000	00000000	; INI23
49	0	0101000	00	01	0	000	0	000	00	0000000000	00010000	; INI24
4A	0	0101001	00	01	0	000	0	000	00	0000000000	00010110	; INI25
4B	1	1010001	10	10	1	000	0	011	00	0010010100	11111000	; INI26
4C	1	1010001	10	10	1	000	0	011	00	0001010000	11111011	; INI27
4D	1	1010001	10	10	1	000	0	011	00	0001010000	11111101	; INI28
4E	1	1010001	10	10	1	000	0	010	00	0001111010	11111110	; INI29
50	1	1010001	10	10	1	000	0	010	00	0101011100	11111110	; INI30

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	$\overline{C}$	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	
51	1	1010001	10	10	1	000	0	011	00	0001101111	11111101	INI31
26	0	0111111	00	01	0	000	0	101	00	0000100110	00000000	INC00
00	0	1010001	00	01	1	000	0	100	00	0111111001	00011010	INT00
01	0	1010111	00	01	1	000	0	100	00	0110001010	00001110	INT01
02	0	0110111	10	01	0	000	0	000	00	0000000000	00000001	INT02
03	0	0100010	10	01	1	000	0	000	11	0000000000	00001111	INT03
04	0	1010000	00	01	1	000	0	000	00	0000000000	00000010	INT04
05	0	1000100	00	01	1	000	0	001	00	0001001111	00000010	INT05
10	0	1010111	11	01	1	000	0	000	00	0000000000	00000001	INT10
11	0	0010111	11	10	1	000	0	001	00	0001001111	11011111	INT11
20	0	1010111	11	01	1	000	0	000	00	0000000000	00000001	INT20
21	0	0010111	11	10	1	000	0	001	00	0001001111	01111111	INT21
30	0	1010111	11	01	1	000	0	000	00	0000000000	00000001	INT30
31	0	0010111	11	10	1	000	0	001	00	0001001111	11110111	INT31
40	0	0011010	00	00	1	000	0	001	00	0000000110	00011100	INT40
06	0	0011011	00	00	1	000	0	000	00	0000000000	00001010	INT41
07	0	1010111	11	01	1	000	0	000	00	0000000000	00000001	INT42
08	1	1101111	10	10	1	000	0	011	00	0000001010	11111110	INT43
09	0	0010111	11	10	1	000	0	001	00	0001001111	11111011	INT44
0A	1	0000000	00	00	1	000	0	111	00	0000000000	00010000	INT45
F9	1	1101111	11	11	1	000	0	110	00	0111111010	11110111	LTC00
FA	0	1010111	00	01	1	000	0	001	00	0000000010	00011111	LTC01
52	1	1011111	10	10	1	000	0	011	00	0001010100	00101011	RDD00
53	0	0010111	11	01	0	000	0	001	00	0001001111	00000000	RDD01
54	1	0000000	00	00	1	000	0	100	00	0010001100	00000000	RDD02
55	1	0000000	00	00	1	000	0	100	00	0010101010	00000000	RDD03
56	1	0000000	00	00	1	000	0	100	00	0011100011	00000000	RDD04
57	1	1011001	00	00	1	000	0	011	00	0001101110	00000000	RDD05
58	1	1010100	00	00	1	000	0	011	00	0001100000	00000000	RDD06
59	1	1010001	10	11	1	000	0	010	00	0001100000	11110111	RDD07
5A	1	1101111	10	10	1	000	0	011	00	0001011010	10111111	RDD08
5B	0	0010101	00	01	0	000	0	011	00	0001011110	11000000	RDD09
5C	1	0000000	00	00	1	000	0	000	00	0000000000	00000001	RDD10
5D	0	0010110	00	01	0	000	0	000	00	0000000000	00000101	RDD11
5E	0	0111001	00	01	0	000	0	010	00	0001101110	00000000	RDD12
5F	0	0110100	00	01	0	000	0	011	00	0001011010	00000001	RDD13
6E	0	0110100	00	01	0	000	0	001	00	0001100110	00000001	RDD14
66	1	0000000	00	00	1	000	0	100	00	0000001011	00000000	RDD15
67	1	1010100	00	00	1	000	0	011	00	0001001111	00000000	RDD16
68	1	0000000	00	00	1	000	0	100	00	0010000011	00000000	RDD17
69	1	1010010	11	00	1	000	0	010	00	0001101100	00000000	RDD18
6A	1	0000000	00	00	1	000	0	100	00	0000011101	00000000	RDD19
6B	1	1010011	10	10	1	000	0	011	00	0001010101	11110111	RDD20
6C	1	0000000	00	00	1	000	0	100	00	0010100111	00000000	RDD21
6D	1	0000000	00	00	1	000	0	001	00	0001010110	00000000	RDD22
60	1	1101111	10	10	1	000	0	011	00	0001100000	10111111	RDD23
61	0	1011011	00	00	1	100	0	000	00	0000000000	00000000	RDD24
62	1	1010001	10	10	1	000	0	011	00	0001100101	11110111	RDD25
63	1	1010100	00	00	1	000	0	011	00	0001100101	00000000	RDD26
64	0	0110100	00	01	0	000	0	000	00	0000000000	00000000	RDD27
65	0	0111001	00	01	0	000	0	011	00	0001100000	00000000	RDD28
6F	1	1011111	10	10	1	000	0	010	00	0001010011	00101011	RDU00
70	1	1010100	00	00	1	000	0	011	00	0001001111	00000000	RDU01
71	1	0000000	00	00	1	000	0	100	00	0010001100	00000000	RDU02
72	1	0000000	00	00	1	000	0	100	00	0010101010	00000000	RDU03
73	1	0000000	00	00	1	000	0	100	00	0000100101	00000000	RDU04
74	0	0010101	00	01	0	000	0	011	00	0001110111	11000000	RDU05
75	1	0000000	00	00	1	000	0	000	00	0000000000	00000001	RDU06
76	0	0010110	11	01	0	000	0	000	00	0000000000	00000101	RDU07
77	0	0000100	00	01	0	000	0	011	00	0001110011	00000001	RDU08
78	1	0000000	00	00	1	000	0	100	00	0000001011	00000000	RDU09
79	1	0000000	00	00	1	000	0	001	00	0001001111	00000000	RDU10

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)												STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39		
	CPE CK	F	WS	KC	$\overline{C}$	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC		
7A	1	1011111	10	10	1	000	0	010	00	0001010011	01111111		RST00
7B	1	0000000	00	00	1	000	0	000	00	0000000000	00100011		RST01
7C	1	0000000	00	00	1	000	0	000	00	0000000000	00001010		RST02
7D	1	0000000	00	00	1	000	0	100	00	0000011000	00101111		RST03
7E	1	0000000	00	00	1	000	0	000	00	0000000000	00000000		RST04
7F	0	0011010	00	11	1	000	0	001	00	0010000010	00110010		RST05
82	1	0000000	00	00	1	000	0	001	00	0010000000	00101110		RST06
80	0	1011111	00	01	1	000	0	100	00	0000100110	00100010		RST07
81	0	0111110	00	01	0	000	0	010	00	0001001111	00001010		RST08
83	0	0000001	11	01	1	000	0	000	00	0000000000	00000000		RUP00
84	0	0101010	11	00	0	000	0	000	00	0000000000	00000000		RUP01
85	0	0000010	11	00	1	000	0	000	00	0000000000	00000000		RUP02
86	0	0001100	11	00	1	000	0	000	00	0000000000	00000000		RUP03
87	0	0011101	11	11	1	000	0	110	00	0010001000	00010100		RUP04
88	0	1010010	11	01	1	000	0	111	00	0000000000	00000000		RUP05
89	1	0000000	00	00	1	000	0	100	00	0010101010	00000000		SDS00
8A	0	0011010	11	11	1	000	0	100	00	0000010110	11010100		SDS01
8B	0	0011010	00	10	1	000	0	111	00	0000000000	00000100		SDS02
8C	0	0000011	00	01	1	000	0	000	00	0000000000	00000000		SKS00
8D	1	0000000	00	00	1	001	0	000	11	0000000000	00000000		SKS01
8E	1	0000000	00	00	1	000	0	000	00	0000000000	00001010		SKS02
8F	0	1011011	10	00	1	110	0	000	00	0000000000	00101111		SKS03
90	1	1011111	10	10	1	000	0	010	00	0001010011	01101011		SKS04
91	1	1101111	10	10	1	000	0	010	00	0010001111	11110111		SKS05
92	0	0011011	00	10	1	000	0	100	00	0000100110	00000010		SKS06
93	0	1011011	10	00	1	110	0	001	00	0101010000	00101110		SKS07
150	1	1011111	10	10	1	000	0	110	00	0010010011	10111111		SKS07A
F0	0	1011011	10	00	1	110	1	001	00	0100000000	00000000		SRD00
100	0	0000000	11	01	1	000	1	000	00	0000000000	00000000		SRD01
101	0	0011101	11	10	1	000	1	000	00	0000000000	00001111		SRD02
102	1	0000000	00	00	1	001	1	111	00	0000000000	01000000		SRD03
F1	0	0000001	00	01	1	000	1	001	00	0100000101	00000000		SRD10
F2	0	0000010	00	01	1	000	1	001	00	0100000101	00000000		SRD20
F3	0	0000011	00	01	1	000	1	001	00	0100000101	00000000		SRD30
F4	0	0000100	00	01	1	000	1	001	00	0100000101	00000000		SRD40
F5	0	0000101	00	01	1	000	1	001	00	0100000101	00000000		SRD50
F6	0	0000110	00	01	1	000	1	001	00	0100000101	00000000		SRD60
F7	0	0000111	00	01	1	000	1	001	00	0100000011	00000000		SRD70
103	1	1010111	10	10	1	000	1	010	00	0100000101	11110111		SRD71
104	0	0010111	10	10	1	000	1	000	00	0000000000	11110111		SRD72
105	1	0000000	00	00	1	001	1	111	00	0000000000	01000000		SRD80
F8	0	1011011	00	11	1	011	1	001	00	0100000110	11110000		SWR00
106	0	1010000	00	01	1	000	1	000	00	0000000000	01000000		SWR01
107	0	0110000	11	00	1	000	0	111	00	0000000000	00000000		SWR02
F9	0	1011011	00	00	1	011	1	001	00	0100001000	00000000		SWR10
108	0	0100001	00	00	0	000	1	111	00	0000000000	01000000		SWR11
FA	0	1011011	00	00	1	011	1	001	00	0100001001	00000000		SWR20
109	0	0100010	00	00	0	000	1	111	00	0000000000	01000000		SWR21
FB	0	1011011	00	00	1	011	1	001	00	0100001010	00000000		SWR30
10A	0	0100011	00	00	0	000	1	111	00	0000000000	01000000		SWR31
FC	0	1011011	00	00	1	011	1	001	00	0100001011	00000000		SWR40
10B	0	0100100	00	00	0	000	1	111	00	0000000000	01000000		SWR41
FD	0	1011011	00	00	1	011	1	001	00	0100001100	00000000		SWR50
10C	0	0100101	00	00	0	000	1	111	00	0000000000	01000000		SWR51
FE	0	1011011	00	00	1	011	1	001	00	0100001110	00000000		SWR60
10E	0	0100110	00	00	0	001	1	000	00	0000000000	01000011		SWR61
10F	1	1011111	10	10	1	000	0	011	00	0100011011	11110000		SWR62
110	1	1011111	10	10	1	000	0	011	00	0100010110	11110011		SWR63
111	1	1011111	10	10	1	000	0	011	00	0100010100	11110111		SWR64
112	1	1011011	11	11	1	110	0	011	00	0100010101	10111111		SWR65
113	0	0011011	10	11	1	000	0	001	00	0100011100	11111100		SWR66
114	1	1011011	11	11	1	110	0	011	00	0100010011	10111111		SWR67

SEE NOTE 1

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	$\overline{CI}$	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	
115	0	0011011	10	11	1	000	0	001	00	0100011100	11111101	SWR68
116	1	1011111	10	10	1	000	0	011	00	0100011001	11111101	SWR69
117	1	1011011	11	11	1	110	0	011	00	0100011010	01111111	SWR6A
118	0	0011011	10	11	1	000	0	001	00	0100011100	11111010	SWR6B
119	1	1011011	11	11	1	110	0	011	00	0100011000	01111111	SWR6C
11A	0	0011011	10	11	1	000	0	001	00	0100011100	11111011	SWR6D
11B	0	0011011	11	01	1	000	0	001	00	0100011100	00000000	SWR6E
11C	1	0000000	00	01	1	001	0	111	01	0000000000	00000000	SWR6F
FF	0	1011011	00	00	1	011	1	001	00	0100001101	00000000	SWR70
10D	0	0100111	00	00	0	000	1	111	00	0000000000	01000000	SWR71
94	1	1010100	00	00	1	000	0	011	00	0001001111	00000000	SRG00
95	0	0011011	10	10	1	000	0	000	00	0000000000	11110000	SRG01
96	0	0011011	11	01	1	000	0	100	00	0010011100	00000000	SRG02
97	0	0011011	10	10	1	000	0	000	00	0000000000	11101011	SRG03
98	0	0011011	11	10	1	000	0	100	00	0010011100	11001111	SRG04
99	0	0011011	10	10	1	000	0	000	00	0000000000	11101110	SRG05
9A	0	0011011	11	11	1	000	0	100	00	0010011100	01100111	SRG06
9B	1	0000000	00	00	1	000	0	001	00	0001001111	00000000	SRG07
9C	0	0010101	00	01	0	001	0	011	00	0010011111	11000000	SRW00
9D	1	0000000	00	00	1	000	0	000	00	0000000000	00000001	SRW01
9E	0	0010110	00	01	0	000	0	000	00	0000000000	00000101	SRW02
9F	0	0110100	00	01	0	000	0	110	00	0001001111	00000001	SRW03
A0	1	0000000	00	00	1	000	0	000	00	0000000000	00001010	SSS00
A1	1	0000000	00	00	1	000	0	000	00	0000000000	00000110	SSS01
A2	1	1101111	10	10	1	000	0	011	00	0010100010	01111111	SSS02
A3	0	1011010	11	11	1	110	0	000	00	0000000000	11100000	SSS03
A4	0	0000010	11	01	1	000	0	000	00	0000000000	00000000	SSS04
A5	0	1111100	11	00	1	000	0	000	00	0000000000	00000000	SSS05
A6	0	0001100	11	01	0	000	0	101	00	0010100001	00000000	SSS06
A7	1	1101111	10	10	1	000	0	010	00	0010101001	01111111	SSX00
A8	1	0000000	00	00	1	000	0	100	00	0010100010	00001010	SSX01
A9	1	0000000	00	00	1	000	0	001	00	0010101111	00000110	SSX02
AA	1	0000000	00	00	1	000	0	100	00	0010100000	00000100	STX00
AB	1	1010001	10	10	1	000	0	011	00	0010101111	11111110	STX01
AC	1	1010001	10	10	1	000	0	010	00	0010101111	11111101	STX02
AD	1	0000000	00	00	1	000	0	100	00	0000011001	00000000	STX03
AE	1	0000000	00	00	1	000	0	111	00	0000000000	00000000	STX04
AF	1	0000000	00	00	1	000	0	000	00	0000000000	00010101	STX05
B0	1	0000000	00	00	1	000	0	000	00	0000000000	00000010	STX06
B1	1	0000000	00	00	1	000	0	000	00	0000000000	00010110	STX07
B2	0	0011011	00	10	1	000	0	000	00	0000000000	00000011	STX08
B3	1	0000000	00	00	1	000	0	000	00	0000000000	00000000	STX09
B4	0	0011101	00	01	0	000	0	011	10	0010110011	00000000	STX10
B5	0	0011011	00	11	1	000	0	000	00	0000000000	10010001	STX11
B6	1	0000000	00	00	1	001	0	000	10	0000000000	00110100	STX12
B7	1	0000000	00	00	1	000	0	000	00	0000000000	00010100	STX13
B8	1	1010001	10	10	1	000	0	010	00	0010111011	11111011	STX14
B9	1	0000000	00	00	1	000	0	000	00	0000000000	00010111	STX15
BA	1	1010001	10	10	1	000	0	010	00	0010111100	11111110	STX16
BB	1	0000000	00	00	1	000	0	000	00	0000000000	00000010	STX10
BC	0	0011011	00	10	1	000	0	100	00	0000100110	01101011	STX18
BD	1	0000000	00	00	1	000	0	000	00	0000000000	00101001	STX19
BE	0	0011011	00	11	1	000	0	000	00	0000000000	00101000	STX20
BF	0	0111111	00	01	0	000	0	011	00	0010111111	00001100	STX21
C0	1	0000000	00	00	1	000	0	000	00	0000000000	00001000	STX22
C1	1	0000000	00	00	1	000	0	000	00	0000000000	00000110	STX23
C2	1	1101111	10	10	1	000	0	010	00	0011000100	01111111	STX24
C3	1	1101111	10	10	1	000	0	101	00	0011000010	11111011	STX25
C4	1	1010000	10	10	1	000	0	010	00	0011000110	11101111	STX26
C5	0	0010000	10	10	1	000	0	001	00	0010101010	11101111	STX27
C6	0	0010111	11	11	1	000	0	001	00	0001001111	11111101	STX28
4F	0	1010000	00	10	1	000	0	001	00	0011000111	11110000	TRM00

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00-ROM39)												STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39		
	CPE CK	F	WS	KC	CI	P SRC	S	BC	P DST	NRA	IM OR SPEC		
C7	0	1010001	11	01	1	000	0	000	00	0000000000	00010011	;	TRM01
C8	1	1010011	10	10	1	000	0	011	00	0011001011	11110111	;	TRM02
C9	0	0010001	11	01	0	000	0	000	00	0000000000	00000000	;	TRM03
CA	0	1010011	10	10	1	000	0	000	00	0000000000	11111000	;	TRM04
CB	0	1010110	11	10	1	000	0	000	00	0000000000	11110000	;	TRM05
CC	0	0000101	00	01	1	000	0	000	00	0000000000	00000010	;	TRM06
CD	0	0000101	00	00	1	000	0	010	00	0011010000	00011101	;	TRM07
CE	0	0000110	11	01	1	000	0	000	00	0000000000	00000000	;	TRM08
CF	0	0000110	11	00	1	000	0	001	00	0011010010	00000000	;	TRM09
D0	0	0000110	11	01	1	000	0	000	00	0000000000	00000000	;	TRM10
D1	0	0000110	11	00	0	000	0	000	00	0000000000	00000000	;	TRM11
D2	0	0000100	00	01	1	000	0	000	00	0000000000	00001110	;	TRM12
D3	0	0011111	00	01	0	000	0	000	00	0000000000	00000000	;	TRM13
D4	0	0001101	00	00	1	000	0	000	00	0000000000	00000000	;	TRM14
D5	0	0100100	00	00	0	000	0	000	00	0000000000	00000000	;	TRM15
D6	1	0010111	11	01	0	000	0	010	00	0011011110	00000000	;	TRM16
D7	1	1010001	10	11	1	000	0	011	00	0011011011	11111000	;	TRM17
D8	1	1011011	10	10	1	110	0	011	00	0011011011	00101011	;	TRM18
D9	0	1010111	11	01	1	000	0	000	00	0000000000	00000000	;	TRM19
DA	0	0010111	11	01	0	000	0	000	00	0000000000	00000000	;	TRM20
DB	1	1010111	10	10	1	000	0	010	00	0011011110	11111110	;	TRM21
DC	1	1010111	11	00	1	000	0	010	00	0011011110	00000000	;	TRM22
DD	0	0010111	10	10	1	000	0	001	00	0011011111	00111111	;	TRM23
DE	0	0010111	10	10	1	000	0	000	00	0000000000	01011111	;	TRM24
DF	1	0000000	00	00	1	000	0	001	00	0000100111	00011011	;	TRM25
E3	0	0000011	00	01	1	000	0	000	00	0000000000	00000000	;	VID00
E4	1	1101111	10	10	1	000	0	011	00	0011100100	11101111	;	VID01
E5	0	1111011	00	00	1	100	0	000	00	0000000000	00001100	;	VID02
E6	1	1011111	00	00	1	000	0	010	00	0011100000	00000000	;	VID03
E0	1	1010000	10	10	1	000	0	011	00	0011100010	11111110	;	VID04
E1	0	0010111	11	11	1	000	0	001	00	0001001111	11101111	;	VID05
E2	0	0110000	10	01	0	000	0	100	00	0010101010	00000000	;	VID06
E7	1	1101111	10	10	1	000	0	011	00	0011100111	11101111	;	VID07
E8	0	0000010	00	01	1	000	0	000	00	0000000000	00001100	;	VID08
E9	0	1111011	00	00	1	100	0	000	00	0000000000	00000000	;	VID09
EA	1	1011111	00	00	1	000	0	010	00	0011100000	00000000	;	VID10
EB	1	1101111	10	10	1	000	0	011	00	0011101011	11101111	;	VID11
EC	0	1111011	00	01	1	100	0	001	00	0011101110	00001100	;	VID12
EE	0	0101000	00	00	0	000	0	000	00	0000000000	00000000	;	VID14
EF	0	0011111	00	01	0	000	0	001	00	0100011101	00000000	;	VID15
11D	0	0101001	00	00	0	000	0	000	00	0000000000	00000000	;	VID16
11E	1	1101111	10	10	1	000	0	011	00	0100011110	11101111	;	VID17
11F	1	1101111	11	11	1	000	0	010	00	0011100000	11101111	;	VID18
120	0	1010000	10	01	1	000	0	000	00	0000000000	00000100	;	VID19
121	1	0000000	00	00	1	000	0	000	00	0000000000	00010110	;	VID20
122	1	0000000	00	00	1	000	0	000	00	0000000000	00101000	;	VID21
123	1	1010001	10	10	1	000	0	010	00	0100101000	11111110	;	VID22
124	0	0011011	00	10	1	000	0	100	00	0000100110	00011001	;	VID23
125	1	0000000	00	00	1	000	0	000	00	0000000000	00101001	;	VID24
126	0	0011011	00	11	1	000	0	100	00	0000100110	01000111	;	VID25
127	0	0100000	10	01	1	000	0	001	00	0011000010	00001000	;	VID26
128	0	0011011	00	11	1	000	0	100	00	0000100110	00000011	;	VID27
129	1	0000000	00	00	1	000	0	100	00	0000011001	00000000	;	VID28
12A	1	0000000	00	00	1	000	0	001	00	0000010111	00000000	;	VID29
12B	1	1101111	10	10	1	000	0	011	00	0100101011	10111111	;	WCS00
12C	0	1010000	10	01	1	000	0	000	10	0000000000	00111000	;	WCS01
12D	0	0011011	00	11	1	000	0	100	00	0000100101	00001000	;	WCS02
12E	1	0000000	00	00	1	000	0	000	10	0000000000	00110010	;	WCS03
12F	0	0101110	11	11	0	000	0	000	00	0000000000	10111111	;	WCS04
130	1	1011100	11	10	1	000	0	010	00	0100101111	10111111	;	WCS05
131	0	0111111	00	01	0	000	0	011	00	0100110001	00000110	;	WCS06
132	1	0000000	00	00	1	000	0	000	00	0000000000	00000010	;	WCS07
133	1	1010001	10	10	1	000	0	110	00	0110000110	11111001	;	WCS08

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	CI	P SRC	S	BC	P DST	NRA	IM OR SPEC	
134	0	1010010	11	01	1	000	0	000	00	0000000000	00010111	WFT00
135	0	0010101	00	01	1	011	0	000	00	0000000000	10000000	WFT01
136	0	0000100	00	01	1	000	0	000	00	0000000000	00000001	WFT02
137	0	0101001	00	00	0	000	0	000	00	0000000000	00000000	WFT03
138	0	0011111	00	01	0	000	0	000	00	0000000000	00000000	WFT04
139	0	0101000	00	00	0	000	0	000	00	0000000000	00000000	WFT05
13A	0	1111011	00	01	1	100	0	000	00	0000000000	00000000	WFT06
13B	0	0100100	00	00	0	000	0	000	00	0000000000	00010110	WFT07
13C	0	0010010	11	11	1	000	0	100	00	0010101010	11101100	WFT08
13D	0	1010010	11	01	1	000	0	100	00	0101010011	00000000	WFT09
13E	1	0000000	00	00	1	000	0	100	00	0010001001	00000000	WFT10
13F	0	1011111	00	01	1	000	0	100	00	0000100101	00000000	WFT11
140	0	0111110	00	01	0	000	0	011	10	0100111111	00000000	WFT12
141	0	0011011	00	11	1	000	0	100	00	0000100101	10010001	WFT13
142	1	0000000	00	00	1	001	0	000	10	0000000000	00110100	WFT14
143	1	1011001	00	00	1	000	0	011	00	0101000110	00000000	WFT15
144	0	0000100	00	01	1	000	0	100	00	0000100101	00000000	WFT16
145	0	0011001	00	01	0	001	0	011	10	0101000100	00000000	WFT17
146	1	0000000	00	00	1	000	0	100	00	0100101011	00000000	WFT18
147	1	0000000	00	10	1	000	0	100	00	0010000011	00000010	WFT19
148	1	1010010	11	00	1	000	0	011	00	0101001101	00000000	WFT20
149	0	0001000	00	01	1	000	0	000	00	0000000000	00000000	WFT21
14A	0	0011111	00	01	0	000	0	000	00	0000000000	00000000	WFT22
14B	0	0101001	00	00	0	000	0	100	00	0101010011	00000000	WFT23
14C	1	0000000	00	00	1	000	0	001	00	0100111110	00000000	WFT24
14D	0	1011010	11	11	1	110	0	000	00	0000000000	11100000	WFT25
14E	1	1011110	11	11	1	000	0	010	00	0101001101	11100000	WFT26
14F	1	0000000	00	00	1	000	0	001	00	0101010001	00000000	WFT27
151	1	0000000	00	00	1	000	0	100	00	0110000110	00000000	WFT29
152	1	0000000	00	00	1	000	0	001	00	0001001111	00000000	WFT30
153	0	0011011	00	11	1	000	0	000	00	0000000000	10010001	WHD00
154	1	0000000	00	00	1	001	0	000	10	0000000000	00110100	WHD01
155	0	0000011	00	01	1	000	0	000	00	0000000000	00000000	WHD02
156	1	0000000	00	00	1	001	0	000	10	0000000000	00000000	WHD03
157	0	0000010	00	01	1	000	0	000	00	0000000000	00000000	WHD04
158	1	0000000	00	00	1	001	0	000	10	0000000000	00000000	WHD05
159	0	0001000	00	01	1	000	0	000	00	0000000000	00000000	WHD06
15A	1	0000000	00	00	1	001	0	100	10	0000011000	00000000	WHD07
15B	1	0000000	00	00	1	000	0	111	10	0000000000	00111000	WHD08
15C	1	1011111	10	10	1	000	0	010	00	0001010011	00001011	WRD00
15D	1	1010100	00	00	1	000	0	010	00	0101011111	00000000	WRD01
15E	1	1010001	10	10	1	000	0	010	00	0001001111	11111011	WRD02
15F	1	0000000	00	00	1	000	0	100	00	0010001100	00010101	WRD03
160	1	1010001	10	10	1	000	0	011	00	0101110111	11111101	WRD04
177	1	1010001	10	10	1	000	0	011	00	0100110100	11111011	WRD05
161	1	0000000	00	00	1	000	0	100	00	0010101010	00000000	WRD06
162	1	0000000	00	00	1	000	0	100	00	0011100011	00000000	WRD07
163	1	1010100	00	00	1	000	0	011	00	0101101011	00000000	WRD08
164	1	1011001	00	00	1	000	0	011	00	0101110110	00000000	WRD09
165	1	1101111	10	10	1	000	0	011	00	0101100101	10111111	WRD10
166	0	0010101	00	01	0	011	0	011	00	0101101001	10000000	WRD11
167	1	0000000	00	00	1	000	0	000	00	0000000000	00000001	WRD12
168	0	0010110	11	01	0	000	0	000	00	0000000000	00000101	WRD13
169	0	0111001	00	01	0	000	0	010	00	0101110110	00000000	WRD14
16A	0	0110100	00	01	0	000	0	011	00	0101100101	00000001	WRD15
176	0	0110100	00	01	0	000	0	001	00	0101101110	00000001	WRD16
16E	1	0000000	00	00	1	000	0	100	00	0100101011	00000000	WRD17
16F	1	1010100	00	00	1	000	0	011	00	0001001111	00000000	WRD18
170	1	0000000	00	00	1	000	0	100	00	0010000011	00000000	WRD19
171	1	1010010	11	00	1	000	0	010	00	0101110100	00000000	WRD20
172	1	0000000	00	00	1	000	0	100	00	0000011101	00000000	WRD21
173	1	1010011	10	10	1	000	0	011	00	0101100001	11110111	WRD22

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	$\overline{CI}$	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	
174	1	0000000	00	00	1	000	0	100	00	0010100111	00000000	WRD23
175	1	0000000	00	00	1	000	0	001	00	0101100010	00000000	WRD24
16B	1	1101111	10	10	1	000	0	011	00	0101101011	10111111	WRD25
16C	1	0000000	00	00	1	000	0	000	10	0000000000	00000000	WRD26
16D	0	0111001	00	01	0	000	0	011	00	0101101011	00000000	WRD27
178	0	0011011	00	10	1	000	0	000	00	0000000000	10010001	WRU00
179	1	0000000	00	01	1	001	0	000	10	0000000000	00110100	WRU01
17A	0	0010101	00	01	0	011	0	011	00	0101111101	10000000	WRU02
17B	1	0000000	00	00	1	000	0	000	00	0000000000	00000001	WRU03
17C	0	0010110	11	01	0	000	0	000	00	0000000000	00000101	WRU04
17D	0	0000100	00	01	0	000	0	010	00	0110000010	00000001	WRU05
17E	1	1101111	10	10	1	000	0	010	00	0101111010	10111111	WRU06
17F	1	1101111	10	10	1	000	0	011	00	0101111110	11011111	WRU07
180	1	0000000	00	00	1	000	0	100	00	0010001001	00000000	WRU08
181	1	0000000	00	00	1	000	0	001	00	0101111110	00000000	WRU09
182	1	1101111	10	10	1	000	0	011	00	0110000100	11011111	WRU10
183	1	0000000	00	00	1	000	0	100	00	0010001001	00000000	WRU11
184	1	0000000	00	00	1	000	0	100	00	0100101011	00000000	WRU12
185	1	0000000	00	00	1	000	0	001	00	0001001111	00000000	WRU13
186	1	0000000	00	00	1	000	0	000	00	0000000000	00100110	WST00
187	0	0011010	00	11	1	000	0	000	00	0000000000	00010110	WST01
188	0	0111110	00	01	0	000	0	011	00	0110001000	00000000	WST02
189	1	0000000	00	00	1	000	0	111	00	0000000000	00100100	WST03
1F6	1	1010001	10	10	1	000	0	110	00	0111110111	11111000	ZAC00
1F7	1	1101111	10	10	1	000	0	110	00	0111001001	11111101	ZAC01
18A	1	0000000	00	00	1	000	0	100	00	0111110110	00010101	ZDT00
18B	0	1011001	00	01	1	000	0	000	00	0000000000	00000010	ZDT01
18C	0	1011000	00	01	1	000	0	000	00	0000000000	00010110	ZDT02
18D	1	1010001	10	00	1	000	0	011	00	0111111000	00011110	ZDT03
18E	0	0011000	10	10	1	000	0	000	00	0000000000	10101010	ZDT04
18F	0	0011000	11	10	1	000	0	100	00	0111110000	10101010	ZDT05
190	1	0000000	00	00	1	000	0	100	00	0101010011	00010011	ZDT06
191	0	1111000	00	01	1	000	0	100	00	0101010011	00010000	ZDT07
192	0	1011000	00	01	1	000	0	100	00	0101010011	00000000	ZDT08
193	0	0011000	11	10	1	000	0	000	00	0000000000	10101010	ZDT09
194	1	0000000	00	00	1	000	0	000	10	0000000000	00000000	ZDT10
195	0	0011000	10	10	1	000	0	000	00	0000000000	10101010	ZDT11
196	1	1101111	10	10	1	000	0	010	00	0111001001	10111111	ZDT12
197	0	0011011	00	10	1	000	0	100	00	0111110011	00011111	ZDT13
198	1	0000000	00	00	1	000	0	100	00	0111110000	00001000	ZDT14
199	1	1101111	10	10	1	000	0	011	00	0111001001	11011111	ZDT15
19A	0	0011011	10	00	1	000	0	100	00	0111110011	00000000	ZDT16
19B	1	1101111	10	10	1	000	0	010	00	0111001001	11011111	ZDT17
19C	1	0000000	00	00	1	000	0	100	00	0111110000	00000010	ZDT18
19D	1	0000000	00	00	1	000	0	000	00	0000000000	00010001	ZDT19
19E	1	0000000	00	00	1	000	0	000	00	0000000000	00010100	ZDT20
19F	1	1101111	10	10	1	000	0	010	00	0111001001	10111111	ZDT21
1A0	1	1101111	10	10	1	000	0	010	00	0111001001	11111110	ZDT22
1A1	1	0000000	00	00	1	000	0	100	00	0111110000	00001000	ZDT23
1A2	0	0011011	00	10	1	000	0	100	00	0111110011	00001111	ZDT24
1A3	1	1101111	10	10	1	000	0	010	00	0111001001	10111111	ZDT25
1A4	1	0000000	00	00	1	000	0	100	00	0111011011	00000000	ZDT26
1A5	0	1111000	00	01	1	000	0	100	00	0111011011	00000000	ZDT27
1A6	0	1011000	00	01	1	000	0	100	00	0111011011	00000000	ZDT28
1A7	1	0000000	00	00	1	000	0	100	00	0101010011	00010101	ZDT29
1A8	0	1011111	00	01	1	000	0	100	00	0111000100	00010111	ZDT30
1A9	0	0101111	00	01	1	000	0	100	00	0111000100	00000000	ZDT31
1AA	1	1010001	10	10	1	000	0	010	00	0110111111	11111000	ZDT32
1F8	0	0011011	10	10	1	000	0	001	00	0110101100	10101010	ZDT33
1AC	0	0011011	11	10	1	000	0	100	00	0111001101	10101010	ZDT34
1AD	0	1111101	00	01	1	000	0	100	00	0111010100	00000000	ZDT35
1AE	1	0000000	00	00	1	000	0	100	00	0111110000	00000000	ZDT36

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	$\overline{C}$	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	
1AF	1	0000000	00	00	1	000	0	100	00	0111001101	00000000	ZDT37
1B0	0	1111101	00	01	1	000	0	100	00	0111010100	00000000	ZDT38
1B1	0	1011101	00	01	1	000	0	100	00	0111001101	00000000	ZDT39
1B2	0	0011011	10	10	1	000	0	100	00	0111110000	01111111	ZDT40
1B3	0	0011010	00	10	1	000	0	000	00	0000000000	00001110	ZDT41
1B4	0	0001111	00	01	1	000	0	010	00	0111001001	00000000	ZDT42
1B5	0	0111110	00	01	0	000	0	011	00	0110110100	00000000	ZDT43
1B6	1	0001111	00	01	1	000	0	011	00	0111001001	00000000	ZDT44
1B7	0	0011010	00	10	0	000	0	100	00	0111110000	00001111	ZDT45
1B8	0	0111101	00	00	1	000	0	010	00	0111001001	00000000	ZDT46
1B9	0	0111110	00	01	0	000	0	011	00	0110111000	00000000	ZDT47
1BA	0	0111101	00	00	1	000	0	011	00	0111001001	00001010	ZDT48
1BB	1	0000000	00	00	1	000	0	001	00	0110001110	00000000	ZDT48A
1AB	0	0011010	00	10	1	000	0	001	00	0110111100	00001101	ZDT49
1BC	1	0000000	00	00	1	000	0	100	00	0000100110	00000000	ZDT50
1BD	0	0111110	00	01	0	000	0	011	00	0110111100	00000000	ZDT51
1BE	1	1101111	10	10	1	000	0	011	00	0111001001	11111110	ZDT52
1BF	0	1011110	00	01	1	000	0	000	00	0000000000	00010000	ZDT53
1C0	1	0000000	00	00	1	000	0	000	00	0000000000	00011101	ZDT54
1C1	1	0000000	00	00	1	000	0	000	00	0000000000	00010110	ZDT55
1C2	1	0000000	00	00	1	000	0	000	00	0000000000	00010100	ZDT56
1C3	1	0000000	00	00	1	000	0	110	00	0000000000	00011111	ZDT57
1C4	1	0000000	00	00	1	001	0	000	10	0000000000	00000000	ZDR00
1C5	1	1101111	10	10	1	000	0	011	00	0111001001	11101111	ZDR01
1C6	0	1111011	00	00	1	100	0	100	00	0111110000	00001100	ZDR02
1C7	1	1011111	00	00	1	000	0	010	00	0111001001	00000000	ZDR03
1C8	1	1101111	10	10	1	000	0	110	00	0111001001	11101111	ZDR04
1C9	0	0001001	00	01	1	000	0	000	00	0000000000	00000000	ZER00
1CA	0	0100010	00	00	0	000	0	000	00	0000000000	00000000	ZER01
1CB	1	0000000	00	00	1	001	0	000	11	0000000000	00000000	ZER02
1CC	0	0100111	11	01	1	000	0	001	00	0000000011	00000000	ZER03
1CD	0	0100000	10	00	0	000	0	000	00	0000000000	00000000	ZRF00
1CE	0	0100001	00	00	0	000	0	000	00	0000000000	00000000	ZRF01
1CF	0	0100010	00	00	0	000	0	000	00	0000000000	00000000	ZRF02
1D0	0	0100011	00	00	0	000	0	000	00	0000000000	00000000	ZRF03
1D1	0	0100111	11	00	0	000	0	000	00	0000000000	00000000	ZRF04
1D2	0	0101000	00	00	0	000	0	000	00	0000000000	00000000	ZRF05
1D3	0	0101100	00	00	0	000	0	111	00	0000000000	00000000	ZRF06
1D4	1	0000000	10	00	0	000	0	011	00	0111001001	00000000	ZRT00
1D5	1	0000001	00	00	0	000	0	011	00	0111001001	00000000	ZRT01
1D6	1	0000010	00	00	0	000	0	011	00	0111001001	00000000	ZRT02
1D7	1	0000011	00	00	0	000	0	011	00	0111001001	00000000	ZRT03
1D8	1	0000111	11	00	0	000	0	011	00	0111001001	00000000	ZRT04
1D9	1	0001000	00	00	0	000	0	011	00	0111001001	00000000	ZRT05
1DA	1	0001100	00	00	0	000	0	101	00	0111001001	00000000	ZRT06
1DB	1	0000000	00	00	1	000	0	000	00	0000000000	00001000	ZRH00
1DC	0	0011011	00	11	1	000	0	100	00	0111110011	00001111	ZRH01
1DD	1	1101111	10	10	1	000	0	011	00	0111001001	11111011	ZRH02
1DE	1	1101111	10	10	1	000	0	010	00	0111001001	10111111	ZRH03
1DF	1	0000000	00	00	1	000	0	100	00	0111110000	00000000	ZRH04
1E0	0	0011011	00	11	1	000	0	100	00	0111110011	00001111	ZRH05
1E1	1	1101111	10	10	1	000	0	011	00	0111001001	10111111	ZRH06
1E2	1	1101111	11	11	1	000	0	010	00	0111001001	11111110	ZRH07
1E3	0	0011101	00	11	1	100	0	100	00	0111110011	00001111	ZRH08
1E4	0	0011101	00	11	1	100	0	100	00	0111110011	00001111	ZRH09
1E5	0	0001000	00	01	1	000	0	000	00	0000000000	00000000	ZRH10
1E6	0	0011111	00	01	1	000	0	000	00	0000000000	00000000	ZRH11
1E7	0	1111011	00	00	1	100	0	100	00	0111110000	00000000	ZRH12
1E8	0	1011111	00	00	1	000	0	010	00	0111001001	00000000	ZRH13
1E9	1	1101111	11	11	1	000	0	011	00	0111001001	11111101	ZRH14
1EA	1	0000000	00	00	1	000	0	100	00	0111110000	00000000	ZRH15
1EB	0	0011011	00	11	1	000	0	100	00	0111110011	00001111	ZRH16

ADDRESS (HEX)	MICROINSTRUCTION FIELDS (ROM00–ROM39)											STATE MNEMONIC
	00	01 07	08 09	10 11	12	13 15	16	17 19	20 21	22 31	32 39	
	CPE CK	F	WS	KC	CI	P SRC	S	BC	P DST	NRA	$\overline{IM}$ OR SPEC	

```
1EC     1 1101111 11 11 1 000 0 011 00 0111001001 11111101 ; ZRH17
1ED     1 1101111 11 11 1 100 0 011 00 0111001001 11111110 ; ZRH18
1EE     1 0000000 00 00 1 000 0 100 00 0111110000 00000000 ; ZRH19
1EF     1 0000000 00 00 1 000 0 111 00 0000000000 00000010 ; ZRH20
1F0     0 0111001 00 01 0 000 0 000 00 0000000000 00100001 ; ZSU00
1F1     1 0000000 00 00 1 000 0 111 00 0000000000 00100000 ; ZSU01
1F3     1 0000000 00 00 1 000 0 000 00 0000000000 00010010 ; ZTC00
1F4     0 0111111 00 01 0 000 0 011 00 0111110010 00000000 ; ZTC01
1F5     1 0000000 00 00 1 000 0 111 00 0000000000 00010011 ; ZTC02
1F2     1 0000000 00 00 1 000 0 100 00 0000011000 00010011 ; ZTC03
1FF     0 0000000 00 00 0 000 0 000 00 0000000000 00000000
```

NOTE 1: THE INSTRUCTIONS WITHIN THE OUTLINE INCLUDE THE CHANGES MADE BY ECNs 428322 AND 428323. THIS ALTERED SUBROUTINE APPEARS ON SHEET 30A OF THE FLOWCHARTS.

THE ORIGINAL INSTRUCTION SEQUENCE (FLOWCHART SHEETS 30, 31) PRIOR TO THE ECNs IS:

```
092     0 1011011 10 00 1 110 0 000 00 0000000000 00101110 ; SKS06
093     1 1011111 10 10 1 000 0 110 00 0010010010 10111111 ; SKS07
```

APPENDIX F

CONTROLLER I/O CONNECTOR P3 AND P4 PIN CONNECTIONS AND SIGNAL FLOW

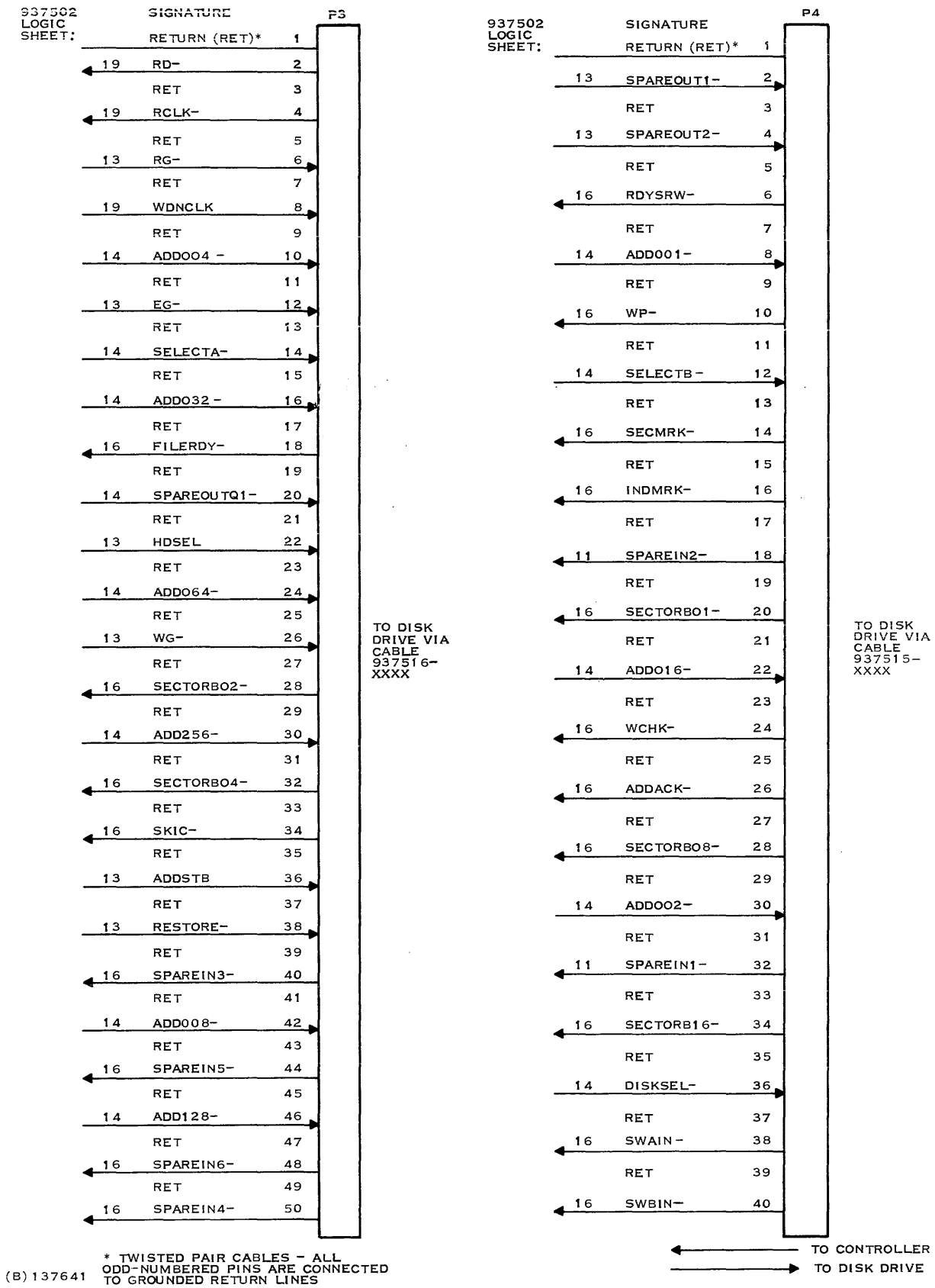


Figure F-1. Controller I/O Connector P3 and P4 Pin Connection and Signal Flow

APPENDIX G

DRAWINGS

APPENDIX G

DRAWINGS

Drawing	Part Number
Kit, 10M Byte Disk	937500 LM937500
Assy, Cable Adapter	937510 LM937510
Schematic, Cable Adapter	937512
Modification Procedure, Voltage & Frequency	940040
Disk Controller Assy, 10 Megabyte (PWB)	937505 LM937505
Disk Controller Assy, 10 Megabyte (fine line)	2262100 LM2262100
Diagram, Logic Detailed 10 Megabyte Disk Controller	937502
Diagram, Logic Detailed 10 Megabyte Disk Controller (fine line)	2262102
Assy, 40-Pin Cable	937515 LM937515
Assy, 50-Pin Cable	937516 LM937516

DWG NO 937500 SH 1

APPLICATION	
NEXT ASSY	USED ON
944900	7506

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN462321(C) R. [illegible]	1 11 79	[illegible]
B	CN429560(C) B. Bohl (1) ADDED SH 2A	2-7-79	[illegible]
C	CN440500(C) B. Bohl	2-7-79	[illegible]
D	CN437501(D) B. Bohl (1) ADDED SH 5	2-7-79	[illegible]
E	CN437765(E) B. Bohl	2-7-79	[illegible]
F	CN442772(C) B. Bohl	2-7-79	[illegible]
G	CN437522(E) R. [illegible]	2-7-79	[illegible]
H	CN448787(D) [illegible]	5-7-79	[illegible]
J	CN454645 (C) (1) ADDED SHT 6	[illegible]	[illegible]
K	CN451878 (C) [illegible]	[illegible]	[illegible]
L	CN435745(C) [illegible]	11-29-79	[illegible]
M	CN461344(B) [illegible]	11-29-79	[illegible]
N	CN461364 (C) [illegible]	3-25-80	[illegible]
P	CN462250 (C) [illegible]	3-25-80	[illegible]
R	CN464185(C) R. [illegible]	5-30-80	[illegible]
T	CN457884(D) J. Bowman	[illegible]	[illegible]
U	CN460373 (C) R. Wiatrek	4-24-81	[illegible]
V	CN484183 (B) R. Wiatrek ADDED SHT 7	4-24-81	[illegible]
W	CN478815 (D) J. Killgore	7-6-81	[illegible]

(REV CONT. SHT 8)

NOTES:

[1] 230 VOLT DRIVES FOR REPLACEMENT ONLY. USE WITH SYSTEMS REQUIRING AMERICAN STYLE NEMA 6-15 INTERFACE AND "220", "230" OR "240" VOLT DEFINITION.

NOTES CONT. ON SHEET 2

REV	AA																														
SHEET	2A																														
REV STATUS OF SHEETS	REV	AB	W	U	AA	AA	AA	AA	AB																						
	SHEET	1	2	3	4	5	6	7	8																						

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1° 3 PLACE DECIMALS ±.010 2 PLACE DECIMALS ±.02
- PARENTHETICAL INFO FOR REF ONLY

DWN C. Slimp DATE 7-22-77
CHK S. Dodson 8-2-77
ENGR Bob Norman 7-28-77
APVD [illegible] 7-28-77
QA [illegible] 7/28/77
CONTR
RLSE [illegible] 8/2/77
MFG [illegible] 7/28/77

TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas

KIT, 10 MEGA BYTE DISK

SIZE	FSCM NO	DRAWING NO
A	96214	937500

SCALE NONE SHEET 1 OF 9

TI-9923D

30 LM

NOTES CONT.

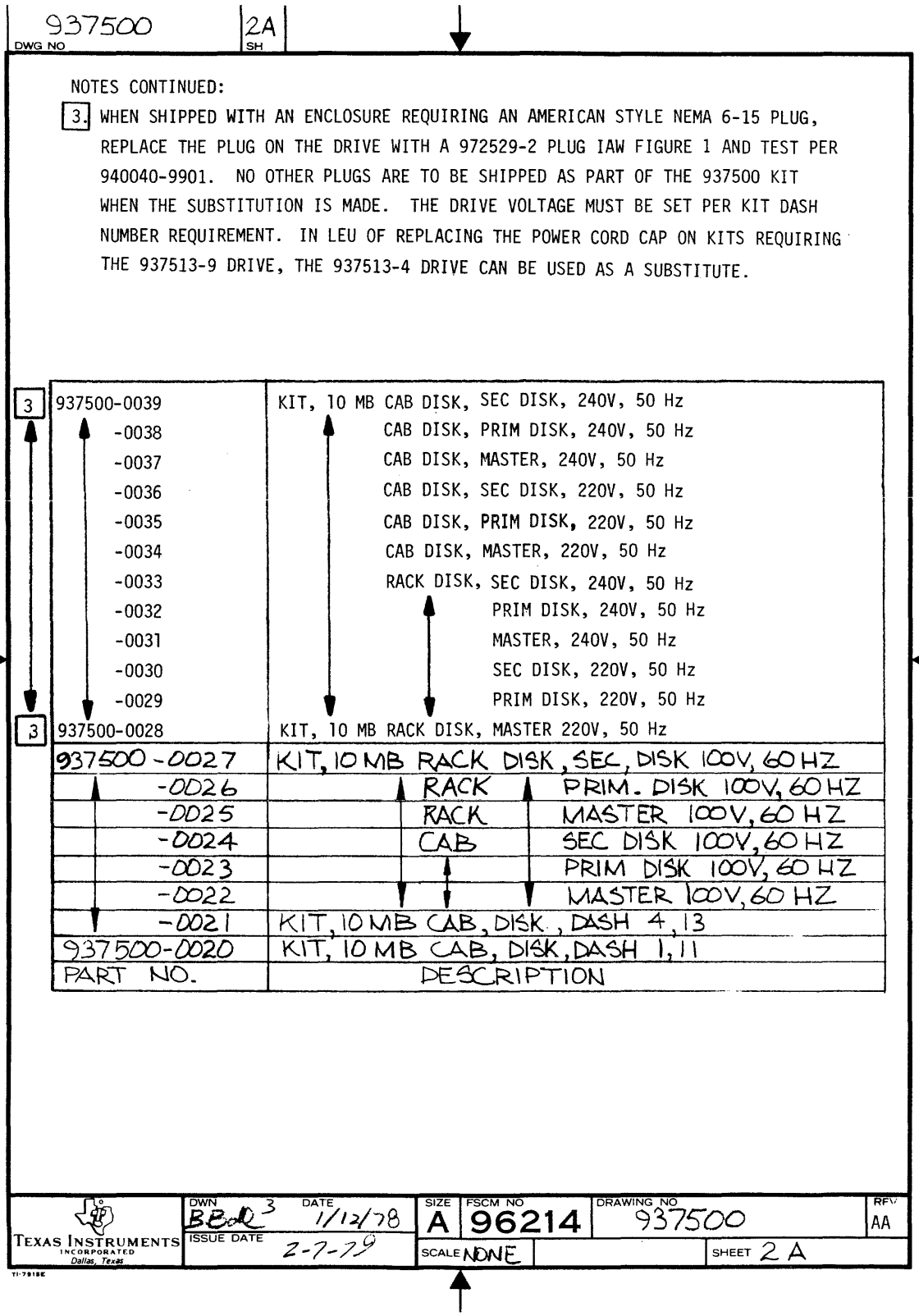
2. ON ALL SECONDARY DISK KITS CUT PINS 2,4,7,9,12 AND 16 OF ITEM 30. ITEM 30 WILL BE INSTALLED AT LOCATION XRM7 ON THE I/O BOARD OF THE PRIMARY DRIVE AT THE NEXT ASSEMBLY LEVEL.

(NOTES CONTINUED ON SHT 2A)

	PART NO.	DESCRIPTION
	937500-0019	KIT, 10MB CAB. DISK, SEC DISK, 100V, 50HZ
	-0018	PRIM DISK, 100V, 50HZ
	-0017	MASTER, 100V, 50 HZ
1	-0016	SEC DISK, 230V, 50HZ
1	-0015	PRIM DISK, 230V, 50HZ
1	-0014	MASTER, 230V, 50 HZ
	-0013	SEC DISK, 120V, 60 HZ
	-0012	PRIM DISK, 120V, 60HZ
	-0011	KIT, 10 MB CAB. DISK, MASTER, 120V, 60 HZ
	-0010	KIT, 10 MB RACK DISK, SEC DISK, 100V, 50 HZ
	-0009	PRIM DISK, 100V, 50 HZ
	-0008	MASTER, 100V, 50 HZ
1	-0007	SEC DISK, 230V, 50 HZ
1	-0006	PRIM DISK, 230V, 50 HZ
1	-0005	MASTER, 230V, 50 HZ
	-0004	SEC DISK, 120V, 60 HZ
	-0003	PRIM DISK, 120V, 60 HZ
	-0002	INTERFACE ONLY
	937500-0001	KIT, 10 MB RACK DISK, MASTER, 120V, 60 HZ

SIZE	CODE IDENT NO	DRAWING NO
A	96214	937500
SCALE	REV W	SHEET 2

TI-7915C



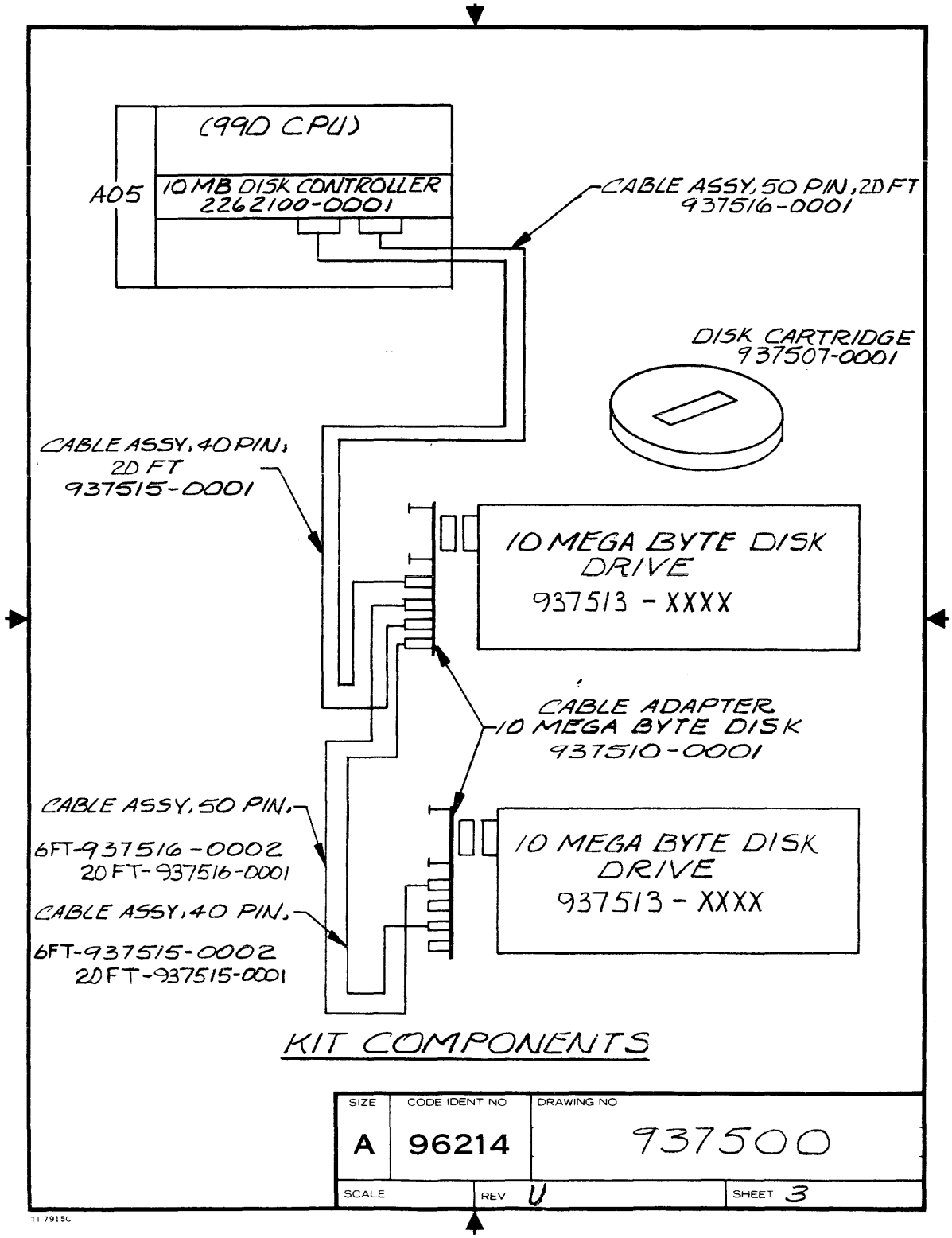
937500 DWG NO | 2A SH

NOTES CONTINUED:

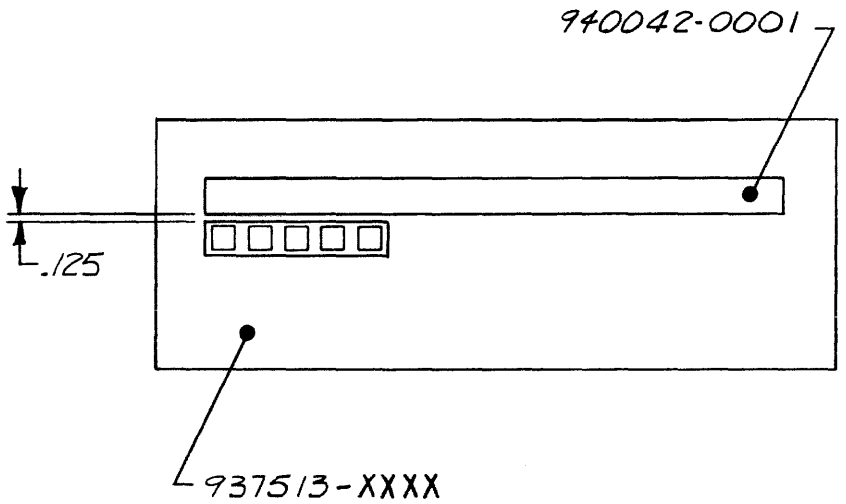
3. WHEN SHIPPED WITH AN ENCLOSURE REQUIRING AN AMERICAN STYLE NEMA 6-15 PLUG, REPLACE THE PLUG ON THE DRIVE WITH A 972529-2 PLUG IAW FIGURE 1 AND TEST PER 940040-9901. NO OTHER PLUGS ARE TO BE SHIPPED AS PART OF THE 937500 KIT WHEN THE SUBSTITUTION IS MADE. THE DRIVE VOLTAGE MUST BE SET PER KIT DASH NUMBER REQUIREMENT. IN LEU OF REPLACING THE POWER CORD CAP ON KITS REQUIRING THE 937513-9 DRIVE, THE 937513-4 DRIVE CAN BE USED AS A SUBSTITUTE.

PART NO.	DESCRIPTION
937500-0039	KIT, 10 MB CAB DISK, SEC DISK, 240V, 50 Hz
-0038	CAB DISK, PRIM DISK, 240V, 50 Hz
-0037	CAB DISK, MASTER, 240V, 50 Hz
-0036	CAB DISK, SEC DISK, 220V, 50 Hz
-0035	CAB DISK, PRIM DISK, 220V, 50 Hz
-0034	CAB DISK, MASTER, 220V, 50 Hz
-0033	RACK DISK, SEC DISK, 240V, 50 Hz
-0032	PRIM DISK, 240V, 50 Hz
-0031	MASTER, 240V, 50 Hz
-0030	SEC DISK, 220V, 50 Hz
-0029	PRIM DISK, 220V, 50 Hz
937500-0028	KIT, 10 MB RACK DISK, MASTER 220V, 50 Hz
937500-0027	KIT, 10 MB RACK DISK, SEC, DISK 100V, 60 HZ
-0026	RACK PRIM. DISK 100V, 60 HZ
-0025	RACK MASTER 100V, 60 HZ
-0024	CAB SEC DISK 100V, 60 HZ
-0023	PRIM DISK 100V, 60 HZ
-0022	MASTER 100V, 60 HZ
-0021	KIT, 10 MB CAB, DISK, DASH 4, 13
937500-0020	KIT, 10 MB CAB, DISK, DASH 1, 11

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas | DWN BEAR 3 | DATE 1/12/78 | ISSUE DATE 2-7-79 | SIZE A | FSCM NO 96214 | DRAWING NO 937500 | REV AA | SCALE NONE | SHEET 2A


(990 CPU)
A05
10 MB DISK CONTROLLER
2262100-0001
CABLE ASSY, 50 PIN, 20 FT
937516-0001
DISK CARTRIDGE
937507-0001
CABLE ASSY, 40 PIN,
20 FT
937515-0001
10 MEGA BYTE DISK
DRIVE
937513 - XXXX
CABLE ADAPTER,
10 MEGA BYTE DISK
937510-0001
CABLE ASSY, 50 PIN,
6FT-937516-0002
20 FT-937516-0001
CABLE ASSY, 40 PIN,
6FT-937515-0002
20 FT-937515-0001
10 MEGA BYTE DISK
DRIVE
937513 - XXXX
KIT COMPONENTS
SIZE
A
CODE IDENT NO
96214
DRAWING NO
937500
SCALE
REV U
SHEET 3
TI 7915C

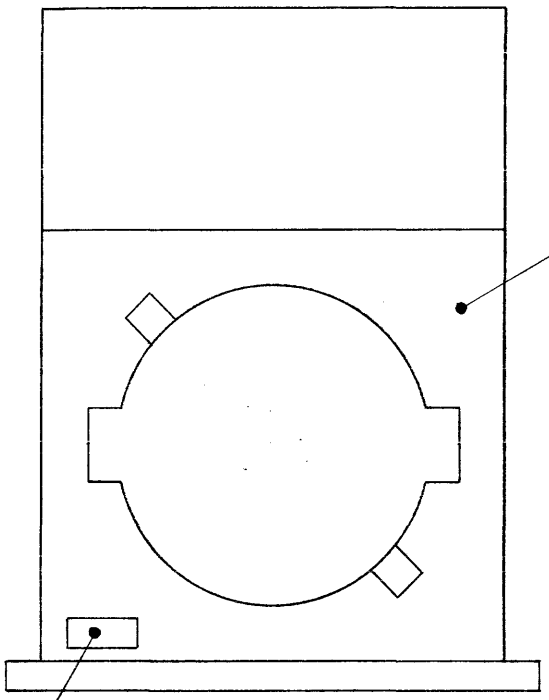
NOTES:
1. REMOVE ADHESIVE COVER FROM LABEL PN 940042.
2. INSTALL LABEL ON DISK DRIVE AS SHOWN BELOW. MAKE SURE OF CORRECT VERTICAL ALIGNMENT WITH BOTH ENDS. MAKE SURE OF CORRECT HORIZONTAL ALIGNMENT BY MATCHING MARKING ON LABEL TO SWITCHES.



SIZE	CODE IDENT NO	DRAWING NO
A	96214	937500
SCALE	REV AA	SHEET 4

TI-7915C

DWG NO 937500 | SH 5



TOP VIEW

NOTES:

1. REMOVE ADHESIVE BACK COVER FROM LABEL P/N 2262106.
2. INSTALL LABEL ON DISK DRIVE AS SHOWN. THE LABEL SHOULD BE PLACED SO THAT IT IS READABLE TO A PERSON STANDING IN FRONT OF THE DRIVE.
3. ~~ITEM 18 TO BE INSTALLED AT INCOMING TEST TIME.~~

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas	DWN B.Bolz 3 DATE 1/12/78	SIZE A	FSCM NO 96214	DRAWING NO 937500	REV AA
	ISSUE DATE 3-7-79	SCALE NONE		SHEET 5	

TI-7918E

DWG NO 937500 | 6 SH

TABLE I
KIT IDENTIFICATION UNDER 937500

	10 MB DISK KITS WITH DISK PACK					
	RACK MOUNTED			CABINET MOUNTED		
	MASTER	PRIM	SEC	MASTER	PRIM	SEC
KIT, DISK, 100V, 50 Hz	-0008	-0009	-0010	-0017	-0018	-0019
KIT, DISK, 100V, 60 Hz	-0025	-0026	-0027	-0022	-0023	-0024
KIT, DISK, 120V, 60 Hz	-0001	-0003	-0004	-0011	-0012	-0013
KIT, DISK, 220V, 50 Hz	-0028	-0029	-0030	-0034	-0035	-0036
KIT, DISK, 230V, 50 Hz	-0005	-0006	-0007	-0014	-0015	-0016
KIT, DISK, 240V, 50 Hz	-0031	-0032	-0033	-0037	-0038	-0039

	10 MB AUXILIARIES		
	INTERFACE ONLY	SPARE PARTS	
		DRIVE ONLY	WITH PWB
KIT, 50 OR 60 Hz	-0002	-0021	-0020

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas	DWN K. Doerfler 3 DATE 7/25/79	SIZE A	FSCM NO 96214	DRAWING NO 937500	REV AA
	ISSUE DATE	SCALE		SHEET 6	

TI-7915E

DWG NO 937500 | SH 7

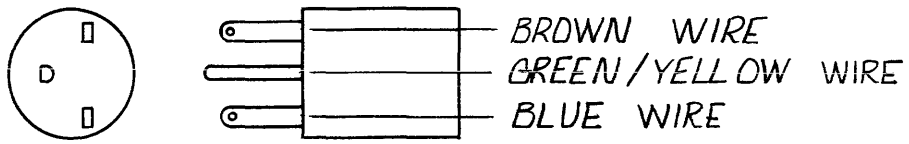


FIGURE 1
200 OR 230 VOLT / 50 HZ RECONFIG

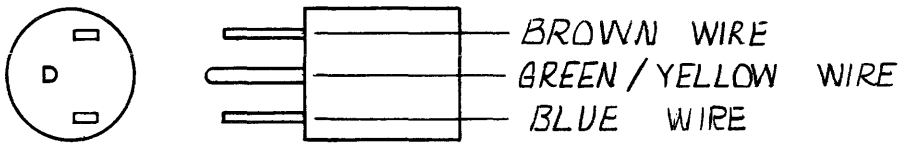


FIGURE 2
100 OR 120 VOLT 60/50 HZ RECONFIG

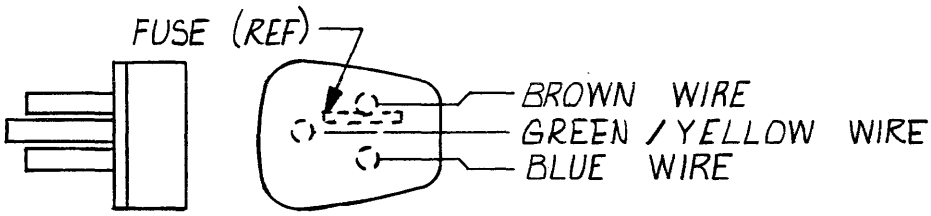
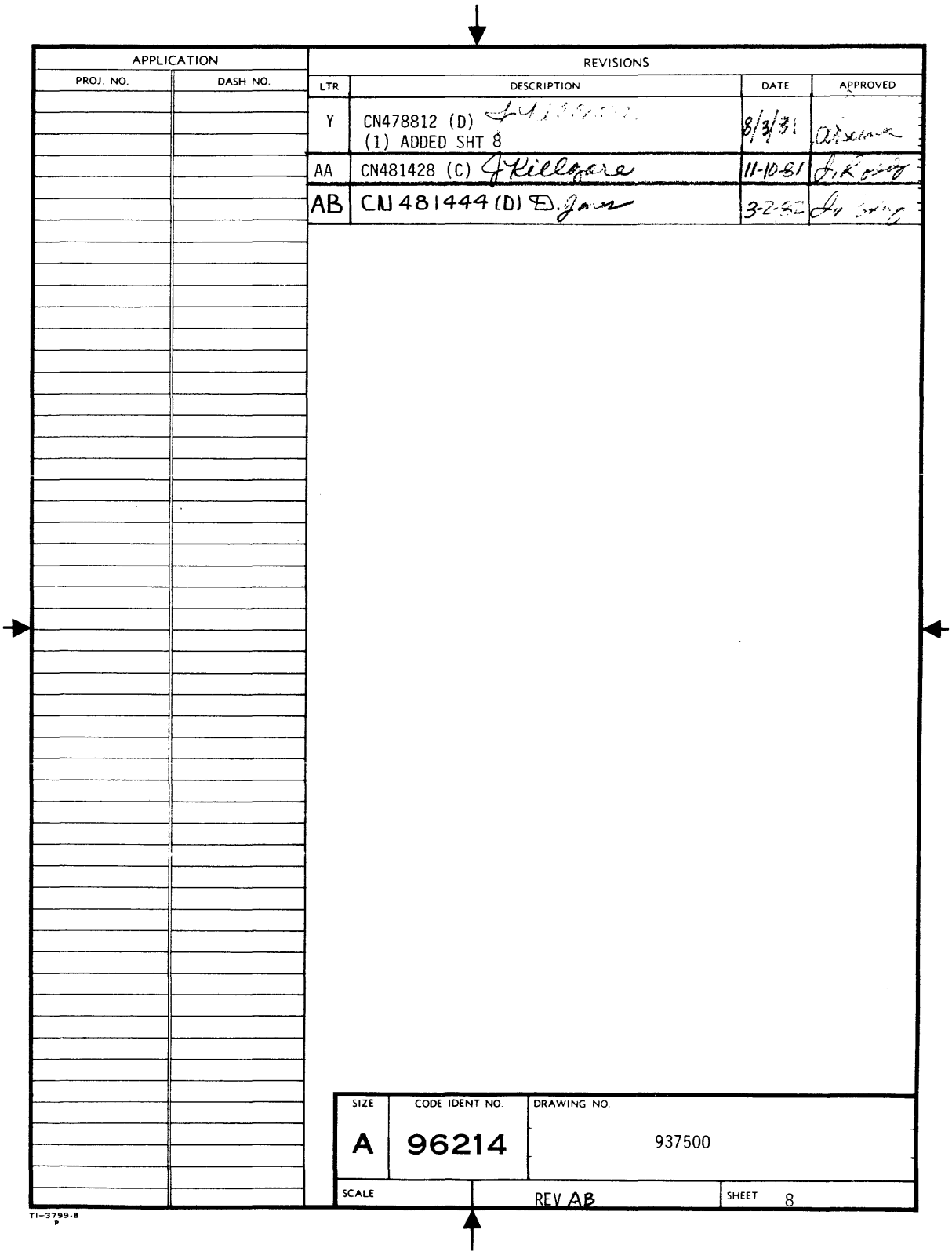


FIGURE 3
240 VOLT / 50 HZ RECONFIG
(TERMINALS SEEN FROM TOP)

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas	DWN R. Wistrak DATE 4-21-81	SIZE A	FSCM NO 96214	DRAWING NO 937500	REV AA
	ISSUE DATE 4-29-81	SCALE NONE		SHEET 7	

TI-7918E



APPLICATION		REVISIONS			
PROJ. NO.	DASH NO.	LTR	DESCRIPTION	DATE	APPROVED
		Y	CN478812 (D) J. Killgore (1) ADDED SHT 8	8/3/81	Dixon
		AA	CN481428 (C) J. Killgore	11-10-81	L. Kong
		AB	CN481444 (D) D. Jones	3-2-82	L. King

SIZE	CODE IDENT NO.	DRAWING NO.
A	96214	937500
SCALE	REV AB	SHEET 8

TI-3799-B

TEXAS INSTRUMENTS
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DATE 01/26/82

LIST OF MATERIAL

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PAGE 1 of

PART NUMBER LM0937500-0001 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	

DRAFTSMAN DATE | CKD. DRAFTSMAN J.R.Colby 1-27-82 DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB RACK DISK,MASTER,120V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. 7506 | PART NUMBER LM0937500-0001 REV AB

T.I. 25789

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INCORPORATED

DATE 01/26/82

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PAGE 2 of

PART NUMBER LM0937500-0001 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB RACK DISK,MASTER,120V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0001 REV AB

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TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/82

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PAGE 1 of

PART NUMBER LM0937500-0002 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0006	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0007	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0008	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0009	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB RACK DISK,INTERFACE ONLY
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0002 REV AB

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TEXAS INSTRUMENTS
INCORPORATED

DATE 01/26/82

LIST OF MATERIAL

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PAGE 1 of

PART NUMBER LM0937500-0003 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB RACK DISK,PRIM DISK,120V,60HZ
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0003 REV AB

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PART NUMBER LM0937500-0004 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE — CKD. DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: KIT,10 MB RACK DISK,SEC DISK,120V,60HZ

APPD.-MFG. DATE — APPD. PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO.

PART NUMBER LM0937500-0004 REV AB

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PART NUMBER LM0937500-0005 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 1 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE — CKD. DRAFTSMAN DATE — DESIGN ENGINEER DATE — TITLE: KIT,10 MB RACK DISK,MASTER,230V,50HZ

APPD.-MFG. DATE — APPD. PROJECT ENGINEER DATE — RELEASED DATE — PROJECT NO.

PART NUMBER LM0937500-0005 REV AB

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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0005 REV AB

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PART NUMBER LM0937500-0006 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 1 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946251-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0006 REV AB

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PART NUMBER LM0937500-0006 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0006 REV AB

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PART NUMBER LM0937500-0007 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 1 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0007 REV AB

T.I. 25789

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PART NUMBER LM0937500-0007 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0007 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0008 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 2 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0008 REV AB

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PART NUMBER LM0937500-0008 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0008 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0009 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 2 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,100V,50HZ

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0009 REV AB

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED

DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 2 of

PART NUMBER LM0937500-0009 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0009 REV AB

T.I. 26789

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0010 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 2 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0010 REV AB

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PART NUMBER LM0937500-0010 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0010 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0011 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,MASTER,120V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0011 REV AB

T.I. 26786

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0012 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: KIT,10 MB CAB. DISK,PRIM DISK,120V,60HZ

APPD-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937500-0012 REV AB

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0013 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: KIT,10 MB CAB. DISK,SEC DISK,120V,60HZ

APPD-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937500-0013 REV AB

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PART NUMBER LM0937500-0014 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 1 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,MASTER,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0014 REV AB

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PART NUMBER LM0937500-0014 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,MASTER,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0014 REV AB

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PART NUMBER LM0937500-0015 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 1 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,PRIM DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0015 REV AB

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PART NUMBER LM0937500-0016 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 1 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0002	CONNECTOR,PLUG-3 WIRE GRND-250 V 15A	HUL - 5666C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,SEC DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0016 REV AB

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PART NUMBER LM0937500-0016 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,SEC DISK,230V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0016 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0017 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 2 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,MASTER,100V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0017 REV AB

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PART NUMBER LM0937500-0017 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,MASTER,100V,50HZ

APPD MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0017 REV AB

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PART NUMBER LM0937500-0018 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 2 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB. DISK,PRIM DISK,100V,50HZ

APPD MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0018 REV AB

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DATE 01/26/82

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PART NUMBER LM0937500-0019 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 2 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		0972529-0001	CONNECTOR,PLUG-3 WIRE GRND-125V 15 AMP	HUL - 5266C

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB CAB. DISK,SEC DISK,100V,50HZ
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0019 REV AB

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PART NUMBER LM0937500-0019 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB CAB. DISK,SEC DISK,100V,50HZ
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0019 REV AB

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PART NUMBER LM0937500-0020 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937500-0021	KIT,10MB CAB,DISK DASH 4,13	
0002	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0002A					937505-1 IS AN ACCEPTABLE	
0002B					SUBSTITUTE FOR 2262100-1.	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10MB CAB,DISK DASH 1,11

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0020 REV AB

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PART NUMBER LM0937500-0021 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0943848-0003	CARD CONTROL	758916-58
0002	00001.000	EA		0943848-0004	CARD SERVO AGC	778312-00
0003	00001.000	EA		0943848-0005	CARD PWR PIGGYBACK	834751-05
0004	00001.000	EA		0943848-0006	RELAY	776126-60
0005	00001.000	EA		0943848-0007	DISK FIXED RECORDING	761906-40
0006	00001.000	EA		0943848-0008	CARD R/W/E	758911-00
0007	00001.000	EA		0943848-0009	CARD SERVO	758908-87
0008	00001.000	EA		0943848-0010	CARD SECTOR	758832-01
0009	00001.000	EA		0943848-0012	CARD I/O WINCH RACK	758577-06
0010	00001.000	EA		0943848-0013	CARD BRAKE	758662-06
0011	00001.000	EA		0943848-0014	HEAD ASM 200/SE/24	750375-04
0012	00001.000	EA		0943848-0015	HEAD ASM 200/SE/24	750375-05
0013	00001.000	EA		0943848-0016	CARD DATA RE	758865-37A
0014	00001.000	EA		0943848-0017	E.O.T. DETECTOR	834473-01
0015	00001.000	EA		0943848-0018	SWITCH SOLID STATE	776126-76
0016	00001.000	EA		0943848-0057	HEAD ALIGNMENT TOOL	757979-00
0017	00001.000	EA		0943848-0060	ARMATURE PLATE SIMULATOR	834555-00
0018	00001.000	EA		0943848-0019	RESISTOR MODULE	753002-00

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10MB CAB,DISK DASH 4,13

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM0937500-0021 REV AB

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PART NUMBER LM0937500-0021 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0019	00001.000	EA		0943848-0054	DRIVE BELT	757229-30
0020	00001.000	EA		0943848-0058	CARD EXTENDER	758615-04
0021	00001.000	EA		0943848-0050	FAULT BOARD	834578-01
0022	00002.000	EA		0943848-0049	AIR FILTER CAB	758048-00
0023	00003.000	EA		0943848-0034	FILTER AIR	834374-00
0024	00002.000	EA		0943848-0053	PRE-FILTER FILTER	776040-00
0025	00005.000	EA		0943848-0021	LAMP	122290-11

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10MB CAB,DISK DASH 4,13

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0021 REV AB

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PART NUMBER LM0937500-0022 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0008A					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB.DISK,MASTER 100V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0022 REV AB

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PART NUMBER LM0937500-0022 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB.DISK,MASTER 100V,60HZ

APPD-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0022 REV AB

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PART NUMBER LM0937500-0023 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0001A					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB.DISK,PRIM DISK 100V,60HZ

APPD-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0023 REV AB

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PART NUMBER LM0937500-0024 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0005	DISK DRIVE,60HZ,120V,CABINET	834484-70
0001A					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB CAB.DISK,SEC DISK 100V,60HZ
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0024 REV AB

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PART NUMBER LM0937500-0025 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0008A					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB RACK DISK,MASTER 100V,60HZ
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937500-0025 REV AB

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PART NUMBER LM0937500-0025 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER 100V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0025 REV AB

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PART NUMBER LM0937500-0026 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0001A					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM.DISK 100V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0026 REV AB

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PART NUMBER LM0937500-0027 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0001	DISK DRIVE,60HZ,120V,RACK MOUNT	834484-68
0001A					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC.DISK 100V,60HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0027 REV AB

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PART NUMBER LM0937500-0028 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0028 REV AB

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PART NUMBER LM0937500-0028 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0028 REV AB

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PART NUMBER LM0937500-0029 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0029 REV AB

T.I. 29788

TEXAS INSTRUMENTS INCORPORATED

DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0030 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0030 REV AB

T.I. 25788

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0031 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 3 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,MASTER,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0031 REV AB

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM0937500-0031 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0014	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0015	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: KIT,10 MB RACK DISK,MASTER,240V,50HZ

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937500-0031 REV AB

T.I. 26788

TEXAS INSTRUMENTS INCORPORATED — DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of — PART NUMBER LM0937500-0032 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 3 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0009	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0010	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: KIT,10 MB RACK DISK,PRIM DISK,240V,50HZ

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937500-0032 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of

PART NUMBER LM0937500-0032 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,PRIM DISK,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0032 REV AB

T.I. 26789

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0033 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0009	DISK DRIVE,50HZ,220V,RACK MOUNT	834484-69
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 3 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936534-9901	PACKING PROC,10 MB DISK DR,RACK MOUNTED	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0011	00001.000	EA		0996745-0001	CABLE CARRIER	016499-CC11
0012	00009.000	EA		0972632-0016	STRAP,TIEDOWN 14 1/2 LG,BUNDLE DIA 0-4	006383-SEE TI DWG
0017	00001.000	EA		2262107-0001	KIT,RETRACTOR BRACKET,DS10	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB RACK DISK,SEC DISK,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0033 REV AB

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PART NUMBER LM0937500-0033 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB RACK DISK,SEC DISK,240V,50HZ

APPD-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0033 REV AB

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PART NUMBER LM0937500-0034 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB CAB DISK ,MASTER,220V,50HZ

APPD-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0034 REV AB

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PART NUMBER LM0937500-0035 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB CAB DISK ,PRIM DISK,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0035 REV AB

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PART NUMBER LM0937500-0036 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE KIT,10 MB CAB DISK ,SEC DISK,220V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO.

PART NUMBER LM0937500-0036 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0037 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262100-0001	CDC DISK CONTROLLER	
0001A					937505-1 IS AN ACCEPTABLE	
0001B					SUBSTITUTE FOR 2262100-1.	
0002	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0003	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0004	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0005	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0006	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0008A					REPLACE POWER PLUG WITH	
0008B					ITEM 29 PER FIGURE 3 OF	
0008C					SHEET 7.	
0008D					SET VOLTAGE PER 940040.	
0009	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0010	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0011	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0012	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB DISK ,MASTER,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0037 REV AB

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DATE 01/26/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of

PART NUMBER LM0937500-0037 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0013	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB DISK ,MASTER,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0037 REV AB

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0038 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 3 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0004	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0005	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0006	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0007	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0008	00001.000	EA		0946261-9701	MNL,DS10 DISC SYS INSTALLATION/OPER-990	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0001	LABEL,DS10 LOGICAL UNIT,PRIMARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB DISK ,PRIM DISK,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0038 REV AB

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DATE 01/26/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937500-0039 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937513-0011	DISK DRIVE,50HZ,220V,CABINET	834484-71
0001A					REPLACE POWER PLUG WITH	
0001B					ITEM 29 PER FIGURE 3 OF	
0001C					SHEET 7.	
0001D					SET VOLTAGE PER 940040.	
0002	00001.000	EA		0937507-0001	DISC CARTRIDGE,TYPE 5440-HIGH DENSITY	
0003	00001.000	EA		0937515-0001	CABLE ASSY,40 PIN,20FT	
0004	00001.000	EA		0937516-0001	CABLE ASSY,50 PIN, 20FT	
0005	00001.000	EA		0937510-0001	CABLE ADAPTER,10 MEGA BYTE DISK	
0006	REF	EA		0936535-9901	PACKING PROC,10 MB DISK DR,BASE CABINET	
0007	REF	EA		0937509-9901	TEST PROC,SYS,10 MEGA BYTE DISK	
0008	00001.000	EA		0940042-0001	LABEL,10 MEGA BYTE DISK DRIVE	
0009	REF	EA		0940040-9901	PROCEDURE,VOLTAGE AND FREQ. CONVERSION	
0010	REF	EA		2261625-9901	DIA,FAMILY TREE,10 MEGA BYTE DISK	
0018	00001.000	EA		0945180-0001	LABEL,DS10 SWITCH SETTING	
0026	00001.000	EA		2262106-0002	LABEL,DS10 LOGICAL UNIT,SECONDARY	
0028	00001.000	EA		2268591-9901	MNL,REPACK INSTRC,DS10 DISK DRIVE	
0029	00001.000	EA		2211738-0001	PLUG, BRITISH ELECTRICAL,250VAC	SEE TI- DRAWING

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: KIT,10 MB CAB DISK ,SEC DISK,240V,50HZ

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937500-0039 REV AB

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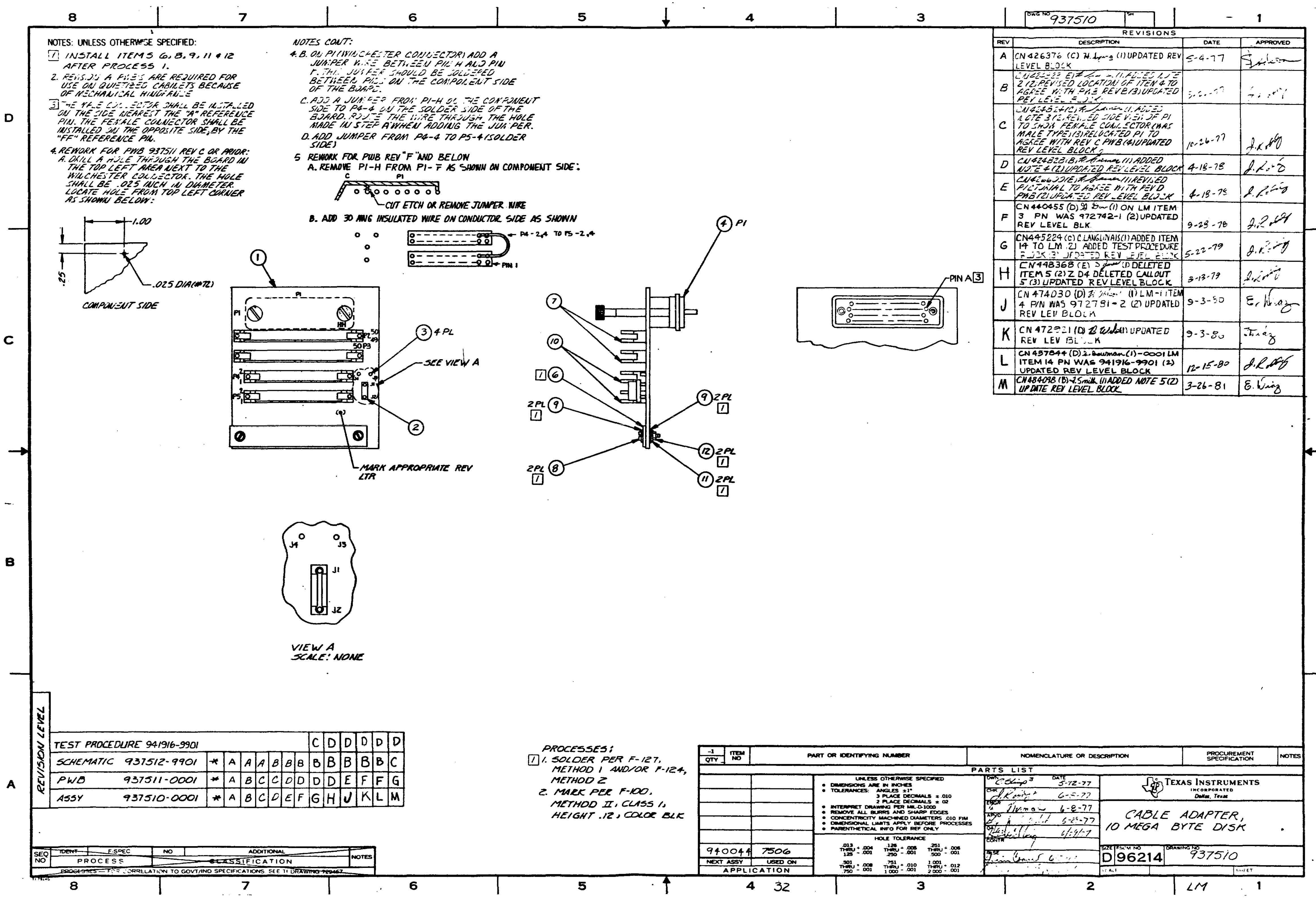
PART NUMBER LM0937500-0039 REV AB

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0030	00001.000	EA		0972037-2100	NETWORK,RES 100 OHM 2% 16PIN 8ELEMENT	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						KIT,10 MB CAB DISK ,SEC DISK,240V,50HZ

APPD.-MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	PART NUMBER	REV
							LM0937500-0039	AB

TI 25789


DWG NO 937510
REVISIONS
REV | DESCRIPTION | DATE | APPROVED
A | CN 426376 (C) (1) UPDATED REV LEVEL BLOCK | 5-4-77
B | 2 (2) REVISED LOCATION OF ITEM 4 TO AGREE WITH PWB REV B (3) UPDATED REV LEVEL BLOCK
C | NOTE 3 (2) REVISED SIDE VIEW OF P1 TO SHOW FEMALE CONNECTOR (WAS MALE TYPE) (3) RELOCATED P1 TO AGREE WITH REV C PWB (4) UPDATED REV LEVEL BLOCK | 10-26-77
D | (1) ADDED NOTE 4 (2) UPDATED REV LEVEL BLOCK | 4-18-78
E | (1) REVISED PICTORIAL TO AGREE WITH REV D PWB (2) UPDATED REV LEVEL BLOCK | 4-18-78
F | CN 440455 (D) (1) ON LM ITEM 3 PN WAS 972742-1 (2) UPDATED REV LEVEL BLK | 9-28-78
G | CN445224 (C) C.LANGLINAIS (1) ADDED ITEM 14 TO LM (2) ADDED TEST PROCEDURE BLOCK (3) UPDATED REV LEVEL BLOCK | 5-22-79
H | CN448368 (E) (1) DELETED ITEM 5 (2) Z D4 DELETED CALLOUT 5 (3) UPDATED REV LEVEL BLOCK | 3-13-79
J | CN 474030 (D) (1) LM-1 ITEM 4 P/N WAS 972781-2 (2) UPDATED REV LEV BLOCK | 9-3-80
K | (1) UPDATED REV LEV BLOCK | 9-3-80
L | CN 457844 (D) (1)-0001 LM ITEM 14 PN WAS 941916-9901 (2) UPDATED REV LEVEL BLOCK | 12-15-80
M | CN484098 (B) J.Smith (1) ADDED NOTE 5 (2) UPDATE REV LEVEL BLOCK | 3-26-81 | E. Vaig
NOTES: UNLESS OTHERWISE SPECIFIED:
1 INSTALL ITEMS 6, 8, 9, 11 & 12 AFTER PROCESS 1.
2. ARE REQUIRED FOR USE ON QUIETIZED CABINETS BECAUSE OF MECHANICAL HINDRANCE
3 THE MALE CONNECTOR SHALL BE INSTALLED ON THE SIDE NEAREST THE "A" REFERENCE PIN. THE FEMALE CONNECTOR SHALL BE INSTALLED ON THE OPPOSITE SIDE, BY THE "FF" REFERENCE PIN.
4. REWORK FOR PWB 937511 REV C OR PRIOR:
A. DRILL A HOLE THROUGH THE BOARD IN THE TOP LEFT AREA NEXT TO THE WINCHESTER CONNECTOR. THE HOLE SHALL BE .025 INCH IN DIAMETER. LOCATE HOLE FROM TOP LEFT CORNER AS SHOWN BELOW:
1.00
.25
.025 DIA(#72)
COMPONENT SIDE
NOTES CONT:
4. B. ON P1 (WINCHESTER CONNECTOR) ADD A JUMPER WIRE BETWEEN PIN H AND PIN F. THE JUMPER SHOULD BE SOLDERED BETWEEN PINS ON THE COMPONENT SIDE OF THE BOARD.
C. ADD A JUMPER FROM P1-H ON THE COMPONENT SIDE TO P4-4 ON THE SOLDER SIDE OF THE BOARD. ROUTE THE WIRE THROUGH THE HOLE MADE IN STEP A WHEN ADDING THE JUMPER.
D. ADD JUMPER FROM P4-4 TO P5-4 (SOLDER SIDE)
5 REWORK FOR PWB REV "F" AND BELOW
A. REMOVE P1-H FROM P1-F AS SHOWN ON COMPONENT SIDE:
C
P1
CUT ETCH OR REMOVE JUMPER WIRE
B. ADD 30 AWG INSULATED WIRE ON CONDUCTOR SIDE AS SHOWN
P4-2,4 TO P5-2,4
PIN 1
P1
4 PL
SEE VIEW A
MARK APPROPRIATE REV LTR
2 PL
PIN A 3
VIEW A
SCALE: NONE
J4
J3
J1
J2
REVISION LEVEL
TEST PROCEDURE 941916-9901 | C D D D D D
SCHEMATIC 937512-9901 | * A A A B B B B B B B B C
PWB 937511-0001 | * A B C C D D D D E F F G
ASSY 937510-0001 | * A B C D E F G H J K L M
PROCESSES:
1 1. SOLDER PER F-127, METHOD 1 AND/OR F-124, METHOD 2
2. MARK PER F-100, METHOD II, CLASS 1, HEIGHT .12, COLOR BLK
SEQ NO | PROCESS | CLASSIFICATION | NOTES
PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 729467
QTY | ITEM NO | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | PROCUREMENT SPECIFICATION | NOTES
PARTS LIST
940044 | 7506
NEXT ASSY | USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±1°
3 PLACE DECIMALS ±.010
2 PLACE DECIMALS ±.02
INTERPRET DRAWING PER MIL-D-1000
REMOVE ALL BURRS AND SHARP EDGES
CONCENTRICITY MACHINED DIAMETERS .010 FIM
DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
PARENTHETICAL INFO FOR REF ONLY
HOLE TOLERANCE
DWN 5-12-77
CHK 6-5-77
ENGR 6-8-77
APVD 5-25-77
TEXAS INSTRUMENTS INCORPORATED Dallas, Texas
CABLE ADAPTER, 10 MEGA BYTE DISK
SIZE D FSCM NO 96214 DRAWING NO 937510
LM

TEXAS INSTRUMENTS INCORPORATED

DATE 12/02/80 **LIST OF MATERIAL** PAGE 1 of

LM PART NUMBER 0937510-0001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937511-0001	PWB,CABLE ADAPTER	
0002	00001.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0003	00004.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-7506 OR 007
0003A					J1 J2 J3 J4	
0004	00001.000	EA		0972781-0004	CONNECTOR, MIN, RECT, PCB, RECEPTACLE	SEE TI- DRAWING
0004A					P1	
0004B					972781-0002 IS AN	
0004C					ACCEPTABLE SUBSTITUTE.	
0006	00001.000	EA		0975377-0001	STRAIN RELIEF,AMPEX SERIES 400	
0007	00002.000	EA		0996604-0005	HEADER STR PIN 50 CONTACTS .062 THK	076381-3433-2002
0007A					P2 P3	
0008	00002.000	EA		0972988-0030	SCREW 6-32 X .500 PAN HEAD CRES	
0009	00004.000	EA		0411027-0806	WASHER,#6 FLAT,CRES,.156 X .375 X .049	OPL - MS15795-806
0010	00002.000	EA		0996604-0004	HEADER STR PIN 40 CONTACTS .062 THK	076381-3433-2001
0010A					P4 P5	
0011	00002.000	EA		0411104-0136	WASHER, LOCK-SPRING, HELICAL, #6	OPL - MS35338-136
0012	00002.000	EA		0416453-0027	NUT,PLAIN 6-32 UNC-2B HEX CRES,SMALL	OPL - NAS671C6
0013	REF	EA		0937512-9701	SCHEM,CABLE ADAPTER,10 MEGA BYTE DISC	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CABLE ADAPTER,10 MEGA BYTE DISK
APPD MFG.	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO. 7506

LM PART NUMBER 0937510-0001 REV M

TI 12849

TEXAS INSTRUMENTS INCORPORATED

DATE 12/02/80 **LIST OF MATERIAL** PAGE 2 of

LM PART NUMBER 0937510-0001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0014	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						CABLE ADAPTER,10 MEGA BYTE DISK
APPD MFG.	DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

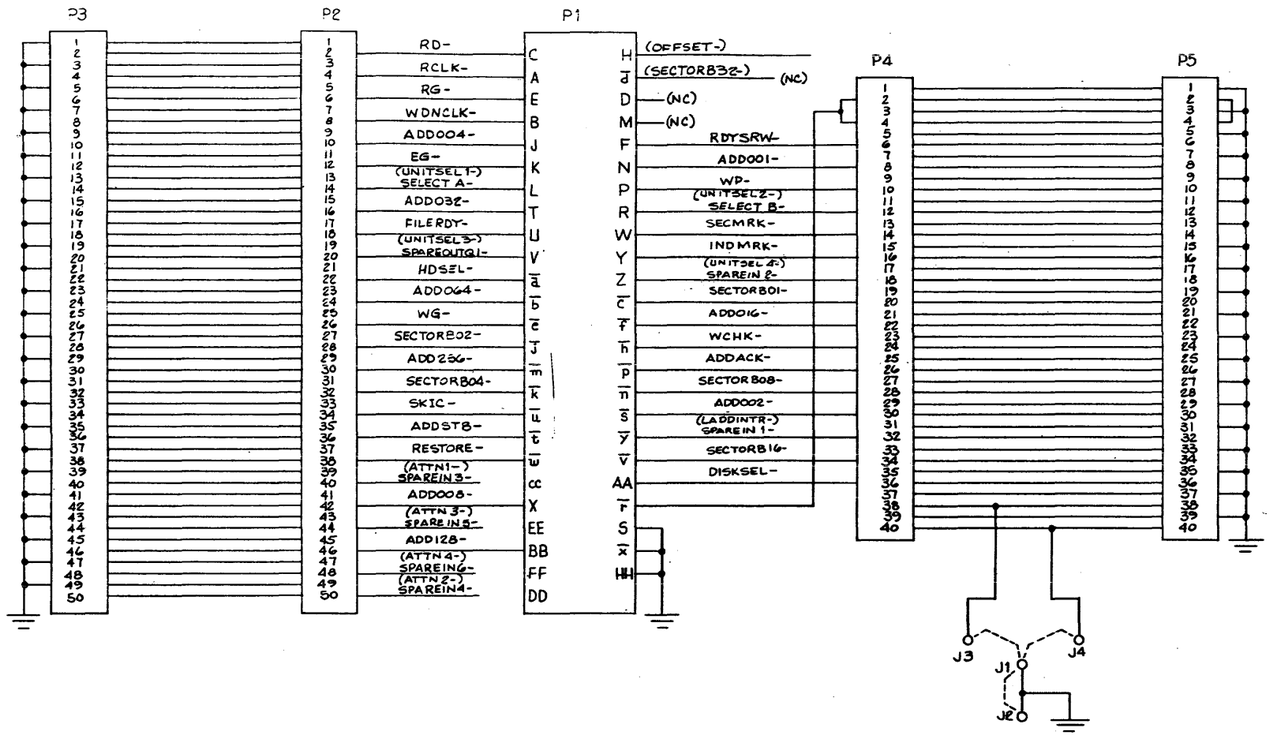
LM PART NUMBER 0937510-0001 REV M

TI 12849

NOTES: UNLESS OTHERWISE SPECIFIED:

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN#26375(E) C [illegible]	8-4-77	[illegible]
B	CN#[illegible](E) [illegible]	12-[illegible]-[illegible]	[illegible]
C	CN#34096(E) D. [illegible]	4-6-81	E. Wray

DWG NO 937512 SH



SEQ NO	IDENT	F SPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 729467

ITEM NO	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		PARTS LIST			

937510	7506
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-3000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .030 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .129 +.004 -.001	.130 THRU .250 +.005 -.005	.251 THRU .500 +.006 -.006
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.003	1.001 THRU 2.000 +.012 -.001

DWG	G.MALLETTE	DATE 4/29/77
CHK	[illegible]	5/9/77
ENGR	[illegible]	5/9/77
PROJ	[illegible]	5/10/77
QA	[illegible]	5/10/77
COMPT		
RLSE	[illegible]	
APVD	[illegible]	

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

SCHEMATIC, CABLE ADAPTER, 10 MEGA BYTE DISK

SIZE D | FSCM NO 96214 | DRAWING NO 937512 | SCALE | SHEET

A 940040

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
937500	7506	A	CN450287 (C)	6-29-79	
		B	CN453409 (C)	2-28-80	
		C	CN478879 (C) (1) ADDED SHTS 10 THRU 12	7-6-81	E. Hinz
		D	CN481399 (C)	1-6-82	
		E	CN491200 (D)	3-3-82	E. Hinz

MODIFICATION PROCEDURE FOR VOLTAGE AND FREQUENCY CONVERSION

REV STATUS OF SHEETS														
REV		E	B		A		E			E	C	C	C	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02

IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY

INTERPRET DWG IN ACCORDANCE WITH MIL-STD-100

DWN Gayle Metzler 3 DATE 7/7/77
CHK 7-19-77
ENGR Bob Norman 7/11/77
QA
APVD 7/19/77
CONTR NO
DESIGN ACTIVITY RELEASE Tony Bailey 7-19-77

TEXAS INSTRUMENTS
INCORPORATED
Equipment Group Dallas, Texas

MODIFICATION PROCEDURE, VOLTAGE AND FREQUENCY CONVERSION

SIZE	CODE IDENT NO	DRAWING NO
A	96214	940040

SCALE None SHEET 1 of 12

TI-9923-C 40

1.0 SCOPE

This procedure is written to allow Texas Instruments the option of changing the operating requirements of voltage and frequency on Control Data Corporation 10 Mega Byte Disc Drive.

2.0 REFERENCE DOCUMENTS

For further information refer to Control Data Incorporated Reference Manual 77614950 (formerly 77834675) that has been assigned TI PN 937517.

3.0 VOLTAGE ADJUSTMENT

3.1 Turn off DC power to the disk drive and wait until the READY indicator light goes off.

3.2 Turn off AC power (breaker at the rear of the unit) and remove the power cord from the wall outlet.

WARNING: Line voltages are present in the area of of the drive motor even when the main circuit breaker is off. Failure to disconnect or turn off main power source may result in injury to service personnel.

3.3 Remove the rear cover from the unit (remove holding screws).

3.4 Remove A1P12 plug from the drive. This plug is located at the lower rear portion, next to power cord, of the drive.

3.5 There will be two (2) plug locations to be changed when altering voltage requirement. Table I gives a list of the voltage ranges along with the plug jumper position required for each of these voltage settings. For each voltage there are two jumper plugs, one end of each plug goes to a fixed pin location. These ends should never be removed or changed on the plug (pins 14 and 15). The location of each pin in connector P12 is shown in Figure 1 and should be studied closely to insure the proper numbering sequence is understood before proceeding to change the jumpers.

3.6 Example

If it is desired to change a unit from a 110 volt unit to a 230 volt unit the jumpers shall be changed as listed below:

Jumper #1 - No Change Required

Jumper #2 - Remove wire and pin at location Number 7 on Plug P12 and move it to location Number 9 on Plug 12

	JUMPER #1		JUMPER #2	
VOLTAGE	FIXED PIN	MOVEABLE PIN	FIXED PIN	MOVEABLE PIN
100	14	4	15	7
110	14	3	15	7
120	14	2	15	7
130	14	1	15	7
140	14	6	15	8
150	14	5	15	8
160	14	4	15	8
170	14	3	15	8
180	14	2	15	8
190	14	1	15	8
200	14	6	15	9
210	14	5	15	9
220	14	4	15	9
230	14	3	15	9
240	14	2	15	9
250	14	1	15	9

TABLE I
VOLTAGE JUMPER CONNECTIONS

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON, TEXAS

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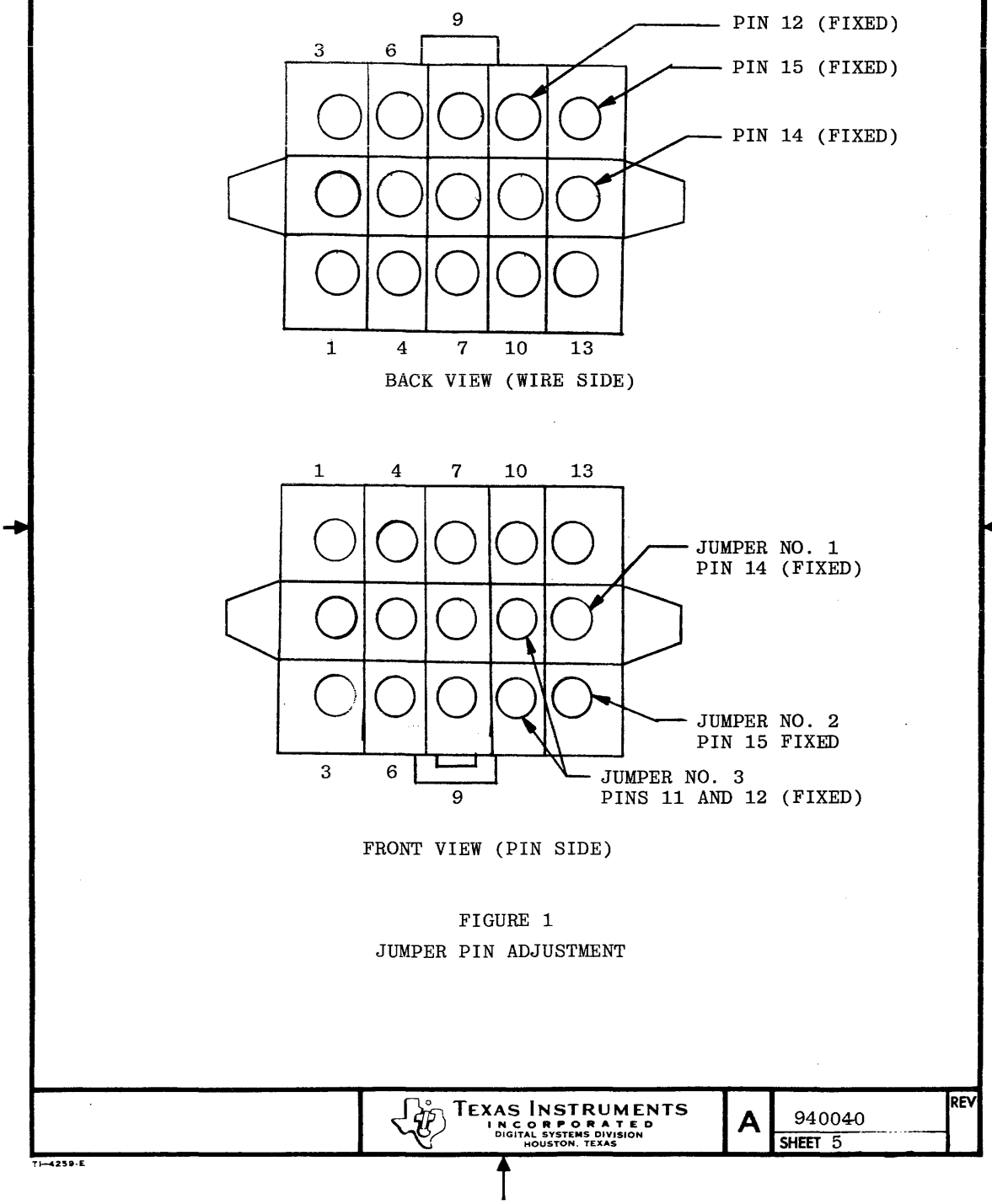

FIGURE 1
JUMPER PIN ADJUSTMENT

3.7 Once the desired changes have been made the plug P12 should be inserted back into its connector at the rear of the drive.

3.8 If the voltage changes such that a new type of cord connector is required, the cord should be changed or the old connector should be taken off and the appropriate connector installed. If the cord or connector is changed, the Hipot Test must be executed. See Appendix A for Hipot instructions.

3.9 Document the voltage change in the space provided on the power supply identification plate at the rear of the unit with a black permanent ink.

3.10 If only the voltage operating range is to be changed and not the line frequency, the rear cover can be replaced and fastened down with the retaining screws. The drive can now be connected to the appropriate new power source and brought up to speed. If the frequency of operation is not to be changed, Paragraph 4.0 can be skipped.

4.0 FREQUENCY ADJUSTMENT

NOTE:
Frequency conversions to 60HZ for delivery within UL-CSA jurisdictions are forbidden. Frequency conversions to 50HZ require that the FCC "Non-Compliant" label be removed.

4.1 Depress START/STOP switch to remove DC voltage from the unit. Wait until the spindle stops rotating (START/STOP lamp extinguished) and then turn the AC power off by tripping the two breakers at the left rear area of the drive. Disconnect the unit from the main power source by unplugging the cord from the power outlet.

CAUTION: Line voltages are present in the area of of the drive motor, even when the main circuit breaker is off. Failure to disconnect or turn off main power source may result in injury to service personnel.

4.2 Hardware Removal

4.2.1 Remove the front panel by removing six screws.

4.2.2 Remove the control panel by disconnecting A5P1 connector from switchboard assembly by removing four screws.

4.2.3 Remove the bottom cover by removing three screws.

4.2.4 Disconnect the IDLER clutch spring by removing the 6-32 screw from the IDLER arm.

4.2.5 Remove the drive belt from the motor and spindle pulleys.

4.2.6 Remove the drive pulley from the motor by loosening the pulley clamp screw.

4.3 Hardware Installation

The parts required for modification (50 or 60 HZ) are listed in TI Drawing 937506.

4.3.1 Fit the new pulley onto the motor shaft so the collar is away from the motor.

4.3.2 Install the new collar and screw over the four pronged hub of the new pulley just installed. Tighten the screw in the collar to 5 $\pm$ 0.5 inch-pounds,

4.3.3 Install the new drive belt such that the smooth side of the belt is against the drive motor and spindle pulley faces.

4.3.4 Rotate the IDLER clutch spring (in free direction) to align with the tapped hole in the IDLER ARM and replace the screw that was removed in Paragraph 4.2.4.

4.3.5 Install the bottom cover by installing the 3 screws removed in Paragraph 4.2.3.

4.3.6 Install the control panel and connect plug A5P1.

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4.3.7 The AC power cord should be removed and replaced with the appropriate cord and connector for the new frequency and voltage.

4.4 The new operating frequency should be recorded in the space provided on the power supply identification plate at the rear of the unit with a black permanent ink.

4.5 The rear cover can now be put back on and anchored with the screws removed earlier. The drive can now be plugged in to the appropriate A.C. outlet and normal operation started.

APPENDIX A
HIPOT PROCEDURE

1.0 SCOPE

1.1 The tests called for in this appendix are to ensure that the ground terminal on the device's power cord is attached to and making good electrical contact with the device's frame. The test also insures that there is sufficient electrical isolation between the frame and the live electrical parts of the device.

2.0 TEST EQUIPMENT

2.1 Slaughter Co. Model A116/213 Dielectric Breakdown Tester.

WARNING
HIGH VOLTAGE IS PRESENT
APPROPRIATED PRECAUTIONS
SHOULD BE OBSERVED

3.0 TEST SET-UP

3.1 Verify that the power cord is connected to the plug as shown in Figure 2, 3, or 4, depending on plug used.

3.2 The switches on the Hipot tester should be set in the following positions:

CONTROL	POSITION
Grd. Lead Bypass	Down
Run Test Disable	Up
AC/DC	DC
124/240V.	120V. (All Devices)
On/Off	On
Test voltage	Adjust for a reading of 1.7 kilovolts on meter
Continuity Disable (If option avail.)	Up (On)

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3.3 The front panel light indicators should be as follows;
The Pilot and 120V lights should be on.
The Grd. Lead Bypass, HV. on and 240V. lights should be off.

3.4 Ensure that the device's main power switch is turned on.

3.5 Attach the ground returen lead (red lead with alligator clip) to the exposed portion of the units frame, Care should be taken to prevent scratching the metal with the clip.

3.6 Insert the device's power plug into the appropriate socket extension on the front panel of the test set. If the plug does not fit in the extension socket, select the appropriate adapter plug and then insert the power cord in the corresponding socket.

4.0 DETAILED TESTS

ENSURE THAT NO ONE IS IN CONTACT
WITH THE CHASSIS UNDER TEST BEFORE
PROCEDING WITH THIS TEST

4.1 Momentarily depress the test switch on the front panel of the test set until the fault buzzer sounds or the test complete light comes on.

4.2 Observe the test set lights on the front of the test set and take the appropriate action as indicated below if they come on:

TEST SET LIGHT	ACTION
Breakdown	Unit has failed dielectric test.
Grd. Open	Unit has failed ground continuity test.
Line/Line Short	Primary lines shorted together. (Should not occur if Continuity Disable is on.)
Continuity Fail	Primary lines exeeced input resistance limits. (Should not occur if Continuity Disable is on.)
Test Complete	Test is complete and voltage is no longer being applied.

4.3 Unplug the device under test's power cord from the test set and then disconnect the test set's ground clip.

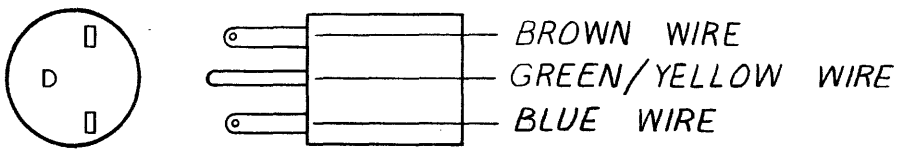


FIGURE 2
200 OR 230 VOLT / 50 HZ RECONFIG

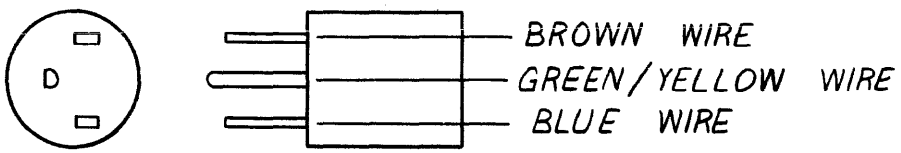


FIGURE 3
100 OR 115 VOLT RECONFIG

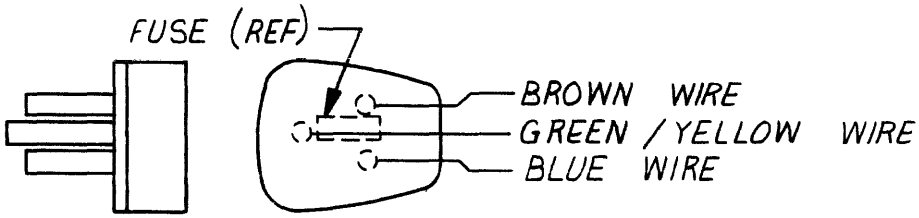


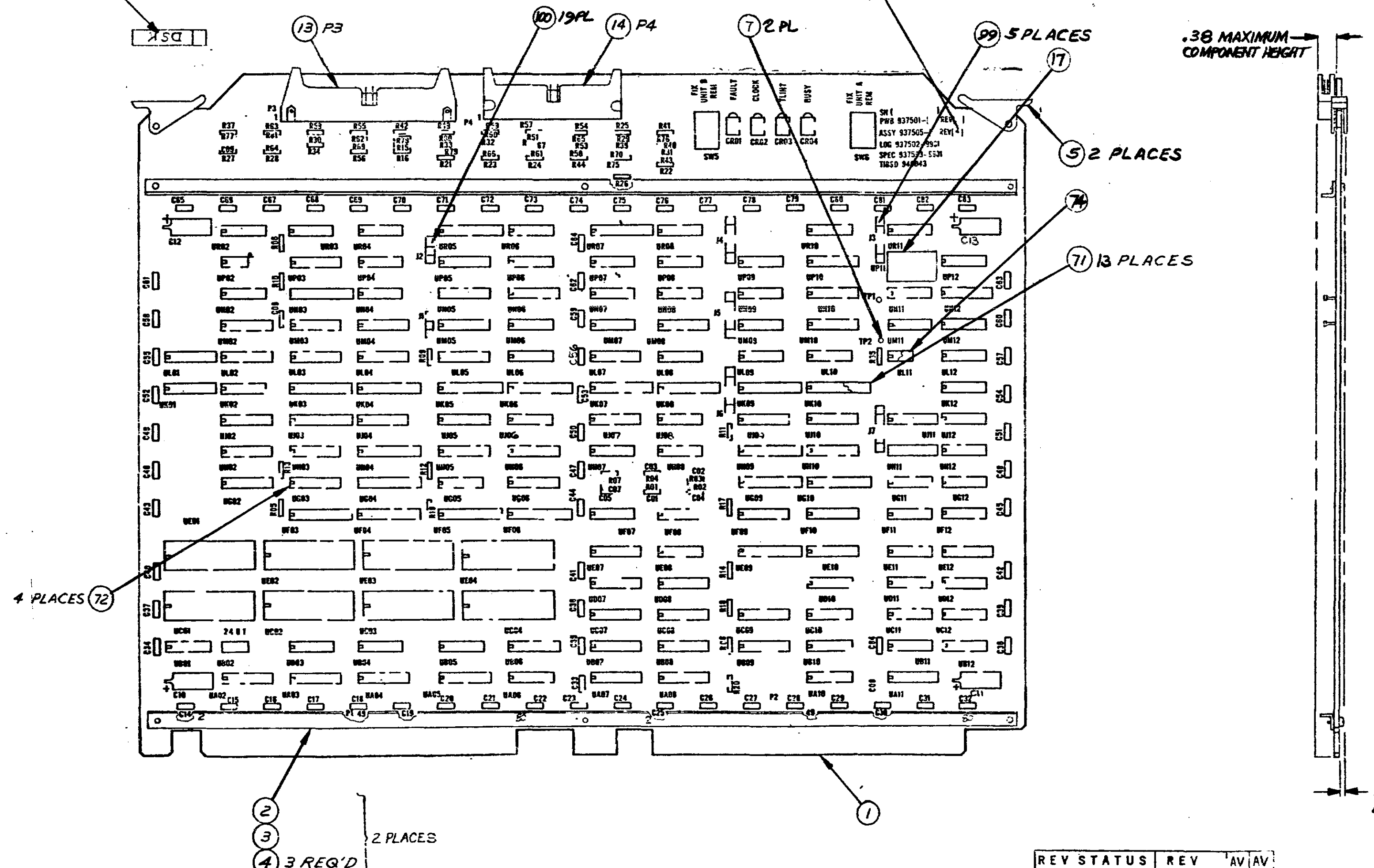
FIGURE 4
240 VOLT / 50 HZ RECONFIG
(TERMINALS SEEN FROM TOP)

	TEXAS INSTRUMENTS INCORPORATED DIGITAL SYSTEMS DIVISION HOUSTON, TEXAS	A	940040 SHEET 12	REV C

TI-4259-E

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

NOTES: UNLESS OTHERWISE SPECIFIED:
1. PIN 1 OF ALL IC PACKAGES IS AT LOWER LEFT CORNER AS VIEWED
~~2. SEAL ITEM 4 PER PROCESS 4~~
3. UG03 UG04 UH06 AND UG06 ARE TEST SOCKETS
4. SW5 AND SW6 ARE NOT USED
5. UG02 AND UF03 ARE SPARES
6. ~~NO CAPACITOR AT C02 WILL BE ADDED AT BOARD ASSEMBLY BUT MAY BE ADDED DURING TEST, DEPENDS ON DELAY REQUIREMENTS FOR EACH BOARD~~
7. REVISION * ASSY CAN BE CHANGED TO REV D ASSY BY INCORPORATING THIS ECN #426598 AND ECN #418078 (REV A). REVISIONS B AND C ARE SKIPPED BECAUSE THEY DEAL WITH A NEW PWB LAYOUT AND SILK SCREEN WHICH MAY NOT BE AVAILABLE FOR EARLY PRODUCTION RUNS
8. REWORK FOR PWB 937501 REV A THRU C ONLY, ADD THE FOLLOWING JUMPERS ON THE COMPONENT SIDE OF THE PWB WITH 30 GAUGE WIRE
   - JUMPER J1 UPPER PIN → UN04-7
   - GND: JUMPER J2 → UR04-7; JUMPER J3 → UR10-7; JUMPER J7 → UJ10-8
   - VCC — JUMPER J6 UPPER PIN → UL09-14 (NOTES CON'T SH2)



DWG NO 937505	SH 1		
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN418778(C) (1) INITIAL RELEASE LEVEL [illegible]	[illegible]	[illegible]
B	CN418078 (C) (1) QTY [illegible] 71 [illegible] (3) [illegible]	[illegible]	[illegible]
C	CN4[illegible] (1) UPDATED ASSY DWG FOR NEW [illegible] UPDATED REV LEV BLOCK	8/11/77	[illegible]
D	CN426598 (2) [illegible] (1) ON LM ITEM 82 QTY WAS 7 (2) ON LM D [illegible] ITEM 82 & 82A (3) ITEM 45 PN WAS 996460-0002 (4) ADDED ITEM 105 (5) ADDED NOTES 6 AND 7 (6) UPDATED REV LEV BLK	8.10/77	[illegible]
E	CN424827(C) [illegible] ADDED TOP BRACKET TO FRONT VIEW (2) REV PICTORIAL TO AGREE WITH REV C PWB (3) ITEM 84 WAS 939370-0325 (4) ITEMS 71 & 83 QTY WAS 6 & 3 RESP (5) ADDED ITEMS 106 & 107 (6) DELETED TOOLING MARKS (7) UPDATED REV LEVEL BLOCK	3-21-78	[illegible]
F	CN426374(C) [illegible] ADDED NOTE 8 (2) UPDATED REV LEVEL BLOCK	3-21-78	[illegible]
G	CN428235(B) [illegible] ADDED SH2 (2) ADDED NOTE 9 (3) UPDATED REV LEVEL BLOCK	3-21-78	[illegible]
H	CN428312(B) [illegible] ADDED NOTE #10 (2) UPDATED REV LEVEL BLOCK	6-8-78	[illegible]
J	CN428322(E) [illegible] (1) LM: PN OF ITEM 94 WAS 937504-001; ITEM 95 WAS 937504-002; ITEM 96 WAS 937504-003; ITEM 97 WAS 937504-004; ITEM 98 WAS 937504-005; (2) UPDATED REV LEVEL BLOCK	6-9-78	[illegible]
K	CN422417(C) [illegible] (1) P1 & P2 PIN NOS 2 & 30 WERE 79 & 1 RESP. (2) UPDATED REV LEVEL BLOCK.	7-24-78	[illegible]
L	CN 442301 (D) [illegible] (1) ON LM ITEM 100 PN WAS 972742-1 (2) UPDATED REV LEVEL BLOCK	9-25-78	[illegible]
M	CN446473 (D) [illegible] (1) LM AND F/D DELETED ITEM 106 (2) UPDATED REV LEVEL BLOCK	[illegible]	[illegible]
N	CN446667 (C) [illegible] (1) UPDATED REV LEVEL BLOCK (2) SH2; ADDED NOTE 11	[illegible]	[illegible]
P	CN441743 (C) E. Molina (1) CREATED LM FOR -5001 (2) ON LM -0001 ADDED ITEM 108 (3) UPDATED REV LEVEL BLOCK	3-22-79	[illegible]
R	CN448751 (B) E. Molina (1) ON LM -0001 ITEM 94 WAS -6, ITEM 95 WAS -7, ITEM 96 WAS -8 ITEM 97 WAS -9 ITEM 98 WAS -10 (2) NOTE 10 WAS ...PERFORM REWORK AFTER ATS TEST... (3) ADDED NOTE 12 (4) UPDATED REV LEVEL BLOCK	3-22-79	[illegible]
T	CN451937 (D) J. [illegible] (1) -0001 LM ITEM 3 WAS 9[illegible]456-0001 (2) UPDATED REV STATUS BLOCK	5-2-79	E. [illegible]
U	CN441765 (C) J. [illegible] (1) ON -5001 LM ITEM 43 WAS 972900-7279, ITEM 56 WAS 972900-7195 (2) UPDATED REV LEVEL BLOCK	5-2-79	E. [illegible]
V	CN448774 (C) [illegible] (1) ON -0001 LM, ITEM 84 WAS -0327 (2) UPDATED REV LEVEL BLOCK	5-24-79	[illegible]

(REV CONT SH 2)

	PART NO	DESCRIPTION
13	937505-5001	AUTO-INSERTED PARTS LIST FOR 937505-0001
	937505-0001	DISK CONTROLLER, 10 MEGA BYTE

REV STATUS	REV	AV	AV
OF SHEETS	SHEET	1	2

REVISION LEVEL																							
TEST PROC 937508	*	*	*	*	*	A	A	A	A	A	C	C	C	C	C	C	D	E					
LOGIC 937502	G	G	G	H	H	H	J	J	K	K	L	L	L	L	L	M	N	N	N				
PWB 937501	J	J	J	J	K	K	K	K	L	L	M	N	N	N	N	N	N	N					
ASSEMBLY	✓	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV				
TEST PROC 937508	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
LOGIC 937502	*	A	A	A	B	C	C	C	E	E	E	F	F	F	G	G	G	G	G				
PWB 937501	*	*	A	B	B	D	D	E	F	F	G	G	G	H	H	H	H	H	H				
ASSEMBLY 937505	*	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V				

SEQ NO	IDENT / F SPEC	NO	ADDITIONAL	NOTES
	PROCESS		CLASSIFICATION	

PROCESSES:
1. SOLDER PER F-127, METHOD I AND/OR F-124, METHOD 2
2. MARK PER F-100, METHOD II, CLASS I, HEIGHT .12, COLOR BLACK, TYPE 6
3. MARK PER F-100, METHOD III, CLASS 12, COLOR BLACK
~~4. SEAL PER F-650 USING ITEMS 92 AND 93~~

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

NEXT ASSY	USED ON
945214	7506
937500	7506
APPLICATION	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE: .013 THRU .125 +.004 −.001; .126 THRU .250 +.005 −.001; .251 THRU .500 +.006 −.001; .501 THRU .750 +.008 −.001; .751 THRU 1.000 +.010 −.001; 1.001 THRU 2.000 +.012 −.001

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

DISK CONTROLLER, 10 MEGA BYTE

SIZE D | CODE IDENT NO 96214 | DRAWING NO 937505 | SCALE 1/1 | SHEET 1 OF 2

4 32 | LM

(NOTES CONT)

9. REWORK FOR PWB 937501 REV A THRU D ONLY
   A) LIFT PIN 12 ON CHIP E10.
   B) LIFT PIN 4 ON CHIP J08
   C) ADD A WIRE FROM E10 PIN 12 (CHIP-NOT CONNECTED TO BOARD) TO THE PAD AT J08 PIN 4 (WHERE THE PIN HAD BEEN REMOVED).
   D) ADD A WIRE FROM J08 PIN 4 (CHIP-NOT CONNECTED TO BOARD) TO THE PAD AT E10 PIN 12 (WHERE THE PIN HAD BEEN REMOVED).
10. REWORK FOR PWB 937501 REV * THRU J ONLY: (USE 30AWG WIRE)
   A) LIFT UC12 PIN 9. ADD WIRE FROM UC12 PIN 9 (RAISED PIN) TO UK12 PIN 6.
   B) ADD WIRE FROM UK12 PIN 3 TO UK12 PIN 4. ADD WIRE FROM UH08 PIN 8 TO UK12 PIN 5.
   C) PERFORM REWORK BEFORE A.T.S.
11. REWORK FOR PWB 937501 REV * THRU J ONLY:
   A) CUT PINS 3 AND 4 ON CHIP UP07
   B) ON COMPONENT SIDE OF PWB, ADD WIRE FROM UH05 PIN 2 TO UP07 PIN 4 (ETCH PAD)
12. REWORK PROCEDURE FOR ASSY 937505 REV P AND EARLIER:
   A) ROM PART NUMBERS 937504-8 -9 AND -10 ARE SUBSTITUTABLE FOR 937504-15 -16 AND -17 RESPECTIVELY. 937504-6 AND -7 MUST BE REPLACED WITH 937504 -13 AND -14 TO DETECT RATE ERRORS ON A READ COMMAND.

[3] ITEM 108 IN -0001 LM CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5001 LM

14. JUMPER PLUG CONFIGURATION TO BE DETERMINED AT U.T. PER OPERATORS MANUAL.
15. REWORK FOR ASSY REV. AA AND EARLIER. REMOVE C05 AT LOCATION G07 AND INSTALL A 1200 PF CAP (ITEM 109) P.N. 972753-0021 AT THIS LOCATION.
16. REWORK FOR PWB REV K AND EARLIER:
   A. INSTALL A SN74S32, ITEM 111, IN UB11
   B. CUT PIN 11 ON UB11 AND CUT PIN 13 ON UB09
   C ADD 30 AWG WIRE FROM UB11 PIN 3 TO UB09 PIN 13 (PKG.)
   D. INSTALL A 3.0 K OHM RESISTOR, ITEM 87, IN LOCATION R2
17. REWORK FOR REV L PWB AND LOWER:
   A CUT PIN 3 AT UP08
   B ADD 30 AWG WIRE FROM UP08-3 (PKG) TO UN08-6
18. REWORK PROCEDURE FOR ASSY REV AE AND BELOW
   A. REPLACE 74LS10 AT UP09 WITH 74S10 ITEM 110 P/N 219402-7410
19. REWORK FOR PWB 937501 REV * AND HIGHER
   A. CUT PIN 2 ON UR04
   B. CUT PIN 10 ON UR06
20. REWORK FOR PWB 937501 REV * AND ABOVE:
   A. CUT PIN 11 AT UH08
   B. ADD 30 AWG WIRE FROM UE08-12 TO UE09-3
   C. INSTALL A 220 pF CAPACITOR AT C02, ITEM 81, P/N 972927-0035
   D. INSTALL A 510FF CAPACITOR AT C03, ITEM 78, P/N 972927-0044
   E. INSTALL A 383 OHM RESISTOR AT R03, ITEM 85, P/N 539370-0345
   F. INSTALL A 402 OHM RESISTOR AT R04, ITEM 83, P/N 539370-0347

DWG NO. 937505 SH 2

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	W	ZN 64 WAS [illegible] ITEM 96 [illegible] UPDATED REV LEVEL BLOCK.	8-1-79	[illegible]
	Y	CN 462587 (C) [illegible] (1) ON SH 1 ADDED REV LEVEL BLOCK	3-5-79	[illegible]
	AA	CN 433599 (D) [illegible] (1) ADDED NOTE 14 (2) UPDATED REVISION LEVEL BLOCK.	[illegible]	[illegible]
	AB	CN 433814 (E) [illegible] (1) ADDED NOTE 15 (2) UPDATED REVISION LEVEL BLOCK	11-5-79	[illegible]
	AC	CN 437960 (D) [illegible] (1) ON LM -0001 LM PN ITEM 103 WAS 972946-0043. (2) CHANGED NOTE 10 (3) UPDATED REV LEVEL BLOCK	2-12-80	[illegible]
	AD	CN 437966 (D) [illegible] (1) CHANGED REWORK NOTES 10 & 11 TO REFLECT REV * THRU J ONLY (2) REWORK NOTE 12 WAS REWORK ... PWB 937501 REV H ... COMMAND (3) UPDATED REV LEVEL BLOCK (4) CORRECTED REV LEVEL BLOCK FOR LOGIC TO REV G FOR ASSY AT REV AB (5) ON SHT 1 ZN D-4 REMOVED FARSIDE FROM MARKING NOTE	2-12-80	[illegible]
	AE	CN 437987 (E) [illegible] (1) UPDATED REV LEVEL BLOCK	[illegible]	[illegible]
	AF	CN 437990 (B) [illegible] (1) ON LM -5001 QTY ITEM 25 WAS 2, AND DELETED UP09 FROM ITEM 25A, AND ADDED ITEM 110 (2) UPDATED REV LEVEL BLOCK	5-20-80	[illegible]
	AG	CN 445174 (C) [illegible] (1) ON SH 1 ADDED VIEW OF ITEM 17 TO F/D (2) DELETED NOTE 2 (3) DELETED PROCESS 4 (4) DELETED BALOONS 92 & 93 (5) ON -0001 LM ITEM 4 PN WAS 972988-0003 (6) UPDATED REV LEVEL BLOCK	5-30-80	[illegible]
	AH	CN 472749 (B) [illegible] (1) ON -1 LM ITEM 87 PN WAS 539370-453 (2) ON -5001 LM QTY ITEM 31 WAS 3 & DELETED UB11 FROM ITEM 31A & ADDED ITEMS 111 & 111A (3) ON SH 2 ADDED NOTE 16 (4) UPDATED REV LEVEL BLOCK	8/5/80	[illegible]
	AJ	CN 461235 (D) [illegible] (1) DELETED THE FOLLOWING ITEM NOS FROM -1 LM & ADDED TO -5001 LM: 83 THRU 89, 103, 104, 107 & 109 (2) ON -1 LM ITEM 75 QTY WAS 72 (3) ON -5001 ADDED ITEMS 75 & 75A (4) UPDATED REV LEVEL BLOCK	9/15/80	[illegible]
	AK	CN 472790 (B) [illegible] (1) ON SH 2 ADDED NOTE 17 (2) UPDATED REV LEVEL BLOCK	9/15/80	[illegible]
	AL	CN 472918 (C) [illegible] (1) UPDATED REV LEVEL BLOCK	10-25-80	[illegible]
	AM	CN 453158 (B) [illegible] (1) REV AC ECN CLASS OF CHANGE WAS C (1) UPDATED REV LEVEL BLOCK	10-9-80	[illegible]
	AN	CN 472940 (C) [illegible] (1) CHANGED REWORK NOTE 16 WAS FOR ASSY AND EARLIER (2) UPDATED REV LEVEL BLOCK	2-18-81	[illegible]
	AP	CN 484067 (B) [illegible] (1) ADDED NOTE 18 (2) ON ECN 472749 REV AH CLASS OF CHANGE WAS C (3) UPDATE REV LEVEL BLOCK	4-3-81	[illegible]
	AR	CN 484059 (B) [illegible] (1) ADDED NOTE 19 (2) UPDATE REV LEVEL BLOCK	4-3-81	[illegible]
	AT	CN 476187 (B) [illegible] (1) DELETED FLAG NOTE 6 (2) ON -5001 ITEM 43 WAS -333 AND ITEM 85 WAS -337 (3) ON -1 ITEM 78 WAS C01, C07 & -78 QTY WAS 2, AND ITEM 81 WAS -48 (4) ADDED NOTE 20 (5) CHANGE NOTE 19 & 3 REV WAS 937505 (6) UPDATED REV LEVEL BLOCK	6-5-81	[illegible]
	AU	CN 471898 (D) [illegible] (1) UPDATED REV LEVEL BLOCK.	10-18-81	[illegible]
	AV	CN 485712 (D) [illegible] (1) UPDATED REV LEVEL BLOCK	2-[illegible]	[illegible]

TEXAS INSTRUMENTS

DATE [illegible]
ISSUE DATE [illegible]

D 96214 937505 V

SHEET 2

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

DATE 01/05/82 — PART NUMBER LM0937505-0001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0003	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0004	00006.000	EA		0972634-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0005	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0007	00002.000	EA		0235794-0050	TERMINAL 1280B	SEE TI- DRAWING
0007A					TP1 TP2	
0008	REF	EA		0937502-9901	LOGIC DIAGRAM,DISK CONT,10 MEGA BYTE	
0009	REF	EA		0937503-9901	SPECIFICATION,DISK CONT,10 MEGA BYTE	
0010	REF	EA		0937508-9901	T.P.,UNIT,DISK CONT,10 MEGA BYTE	
0013	00001.000	EA		0972137-0010	CONNECTOR,P.C.HEADER 50 CONTACTS	BEI - 65483-020
0013A					P3	
0014	00001.000	EA		0972706-0005	HEADER, CONN, RIGHT ANGLE, 40 CONTACTS	075037-3495-1002
0014A					P4	
0015	00001.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0015A					CR01	
0016	00003.000	EA		0972537-0002	DIODE,LED GREEN RT ANGLE	072619-550-0206
0016A					CR02 CR03 CR04	
0017	00001.000	EA		0996059-0013	OSCILLATOR,RF,CRYSTAL 5.000MHZ 0.01%	001537-K-1100 A

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: DISK CONTROLLER,10 MEGA BYTE

APPD MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. 7506 — PART NUMBER LM0937505-0001 — REV AV

TI 25789

TEXAS INSTRUMENTS INCORPORATED — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of

DATE 01/05/82 — PART NUMBER LM0937505-0001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0017A					UP11	
0040	00002.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	001295-SN74LS240N
0040A					UH04 UN03	
0042	00002.000	EA		0996089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0042A					UR05 UR07	
0044	00001.000	EA		0996307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0044A					UE09	
0045	00003.000	EA		0996201-0001	IC,SN74S374N,EDGE-TRIGGERED FLIP-FLOPS	TI -SN74S374N
0045A					UF04 UJ03 UK06	
0046	00001.000	EA		0222222-7497	NETWORK SN7497N	
0046A					UJ07	
0057	00004.000	EA		0996564-0001	IC,SN74S225N 16 X 5-BIT FIFO MEMORY	001295-SN74S225N
0057A					UK03 UK04 UK05 UK07	
0064	00003.000	EA		0996102-0001	IC,SN74S482N MICRO-ADDRESS GENERATOR	TI -SN74S482N
0064A					UG09 UG10 UH09	
0066	00008.000	EA		0974859-0001	NETWORK, BI-POLAR 2BIT PROCESSOR -3002	
0066A					UC01 UC02 UC03 UC04 UE01	
0066B					UE02 UE03 UE04	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: DISK CONTROLLER,10 MEGA BYTE

APPD MFG — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-0001 — REV AV

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM0937505-0001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0070	00001.000	EA		0972899-0004	NETWORK, DUAL STATIC SHIFT REGISTER 1328	001295-TMS3129NC
0070A					UL11	
0071	00013.000	EA		2210188-0014	SOCKET,DIP,20-PIN,LOW PROFILE	SEE T -I DRAWING
0071A					XUF05 XUF06 XUK09 XUK10	
0071B					XUK08 XUG04 XUG09 XUG10	
0071C					XUH09 XUK03 XUK04 XUK05	
0071D					XUK07	
0072	00004.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING
0072A					XUG03 XUG06 XUH06 XUJ07	
0074	00001.000	EA		2210188-0010	DIP SOCKET,8-PIN,LOW PROFILE	SEE TI- DRAWING
0074A					XUL11	
0075	00001.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0075A					C14	
0076	00001.000	EA		0972927-0041	CAP FIX MICA 500V 390 PF 5 %	SEE TI- DRAWING
0076A					C09	
0078	00003.000	EA		0972927-0044	CAP FIX MICA 300V 510 PF 5 %	QPL -CM05F511J0C
0078A					C01,C03,C07	
0079	00001.000	EA		0972929-0433	CAP FIX CERAMIC .100 UF 10 % 50 V	QPL -M39014/01-1433

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: DISK CONTROLLER,10 MEGA BYTE

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-0001 — REV AV

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TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 4 of — PART NUMBER LM0937505-0001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0079A					C06	
0080	00001.000	EA		0972929-0415	CAP FIX CERAMIC .010 UF 10 % 100 V	QPL -M39014/01-1415
0080A					C04	
0081	00001.000	EA		0972927-0035	CAP FIX MICA 500V 220 PF 5 %	SEE TI- DRAWING
0081A					C02	
0090	00001.000	EA		0772923-0001	SWITCH DUAL IN LINE, 4 POSITION	AMP -435166-2
0090A					U802	
0094	00001.000	EA		0937504-0013	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 1	
0094A					UF05	
0095	00001.000	EA		0937504-0014	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 2	
0095A					UF06	
0096	00001.000	EA		0937504-0015	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 3	
0096A					UK09	
0097	00001.000	EA		0937504-0016	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 4	
0097A					UK10	
0098	00001.000	EA		0937504-0017	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 5	
0098A					UK08	
0099	00005.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: DISK CONTROLLER,10 MEGA BYTE

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-0001 — REV AV

TEXAS INSTRUMENTS INCORPORATED

DATE 01/05/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 5 of

PART NUMBER LM0937505-0001 REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0099A					J3 J4 J5 J6 J7	
0100	00019.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0101	00004.000	EA		0972924-0011	CAP FIX TANT SOLID 68 MFD 10 % 15 VOLT	QPL -M39003/1-2274
0101A					C10 C11 C12 C13	
0108	00001.000	EA		0937505-5001	AUTO-INSERTED PARTS LIST FOR 937505-0001	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: DISK CONTROLLER,10 MEGA BYTE

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937505-0001 REV AV

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED

DATE 01/05/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of

PART NUMBER LM0937505-5001 REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		0937501-0001	PWB,DISK CONTROLLER,10 MEGA BYTE	
0018	00001.000	EA		0240000-7400	NETWORK-SN74H00N	
0018A					UF08	
0019	00003.000	EA		0972900-7402	NETWORK,SN74LS02N	
0019A					UC11 UE11 UF11	
0020	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0020A					UJ08	
0021	00003.000	EA		0222222-7406	NETWORK SN7406N	
0021A					UR03 UR04 UR06	
0022	00002.000	EA		0222222-7407	NETWORK-SN7407N	TI- -SN7407N
0022A					UG05 UH07	
0023	00002.000	EA		0972749-0001	NETWORK, SN74LS08N	
0023A					UL09 UM12	
0024	00001.000	EA		0219402-7403	NETWORK SN74S08N	TI- -SN74S08N
0024A					UC10	
0025	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0025A					UL10	
0026	00001.000	EA		0240000-7411	NETWORK-SN74H11N	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937505-5001 REV AV

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0026A					UB12	
0027	00008.000	EA		0972784-0002	NETWORK SN74LS14N	
0027A					UA10 UF12 UL06 UL08 UM07	
0027B					UP07 UR08 UB01	
0028	00001.000	EA		0972813-0001	NETWORK-SN74LS21N	
0028A					UP12	
0029	00001.000	EA		0972814-0001	NETWORK-SN74LS27N	
0029A					UR10	
0030	00001.000	EA		0972900-7430	NETWORK SN74LS30N	TI -SN74LS30N
0030A					UN02	
0031	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0031A					UD10 UK12	
0032	00001.000	EA		0222222-7438	NETWORK SN7438N	
0032A					UR02	
0033	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0033A					UN09	
0034	00001.000	EA		0240000-7451	NETWORK-SN74H51N	
0034A					UH12	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-5001 — REV AV

TI 25788

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0035	00010.000	EA		0972900-7474	NETWORK SN74LS74N	
0035A					UB10 UG11 UL12 UN04 UN07	
0035B					UN11 UP04 UP06 UP08 UR11	
0036	00001.000	EA		0219402-7474	NETWORK SN74S74N	
0036A					UM09	
0037	00001.000	EA		0972900-7109	NETWORK SN74LS109N	TI -SN74LS109N
0037A					UN12	
0038	00006.000	EA		0972732-0001	NETWORK SN74LS132N	TI -SN74LS132N
0038A					UC12 UF07 UJ06 UJ12 UM11	
0038B					UN08	
0039	00003.000	EA		0972900-7174	NETWORK SN74LS174N	
0039A					UF09 UJ05 UP03	
0041	00004.000	EA		0996588-0002	IC,QUADRUPLE BUS TRANSCEIVER SN74LS243N	02195S-N74LS243N
0041A					UA06 UB03 UB04 UR05	
0043	00001.000	EA		0972667-0001	NETWORK,SN74LS279N	
0043A					UE12	
0047	00002.000	EA		0972900-7138	NETWORK SN74LS138N	TI -SN74LS138N
0047A					UM08 UN10	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-5001 — REV AV

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 4 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0048	00001.000	EA		0219402-7138	NETWORK SN74S138N	
0048A					UE10	
0049	00002.000	EA		0219402-7139	NETWORK SN74S139N	
0049A					UJ11 UM10	
0050	00001.000	EA		0222222-7148	NETWORK SN74148N	
0050A					UF10	
0051	00001.000	EA		0972900-7153	NETWORK SN74LS153N	TI -SN74LS153N
0051A					UN06	
0052	00001.000	EA		0219402-7153	NETWORK SN74S153N	TI -SN74S153N
0052A					UE07	
0053	00013.000	EA		0972686-0001	NETWORK-QUAD MULTIPLEXER, SN74LS157N	
0053A					UA07 UA11 UB06 UB07 UB08	
0053B					UH03 UH10 UJ04 UJ10 UL02	
0053C					UM02 UM05 UN05	
0054	00003.000	EA		0972669-0001	NETWORK,SN74LS163N	
0054A					UH05 UL05 UP10	
0055	00003.000	EA		0219402-7182	NETWORK SN74S182N	TI -SN74S182N
0055A					UC07 UD07 UD09	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937505-5001 — REV AV

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 5 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0056	00004.000	EA		0996427-0001	IC,SN74LS195AN 4-BIT PARALLEL-ACCESS	001295-SN74LS195AN
0056A					UL03 UL04 UM03 UM04	
0058	00004.000	EA		0996136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N
0058A					UH02 UJ02 UK01 UL01	
0059	00002.000	EA		0996023-0001	IC,LOW POWER SCHOTTKY 8 BIT SN74LS259N	TI -SN74LS259N
0059A					UH11 UP05	
0060	00001.000	EA		0972159-7265	NETWORK, SN74265N	
0060A					UL07	
0061	00001.000	EA		0947573-0001	PROM,32X8,BOOLEAN,MTC NO.1	
0061A					UJ09	
0062	00001.000	EA		0972787-0004	NETWORK SN74LS368N	
0062A					UA05	
0063	00002.000	EA		0219402-7157	NETWORK SN74S157N	
0063A					UC08 UC09	
0065	00002.000	EA		0974674-0001	NETWORK SN75138N	
0065A					UA08 UB09	
0067	00001.000	EA		0974866-0001	NETWORK,CRC GENERATOR	FCD --9401
0067A					UM06	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937505-5001 — REV AV

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 6 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0068	00001.000	EA		0972188-0001	NETWORK,NE555V,MONOLITHIC TIMING,LINEAR	ST -NE555V
0068A					UP02	
0069	00003.000	EA		0974849-0001	NETWORK, DM8136	
0069A					UA02 UA03 UA04	
0073	00001.000	EA		0240000-7474	NETWORK-SN74H74N	
0073A					UD12	
0075	00071.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0075A					C03,C15 THRU C84	
0077	00003.000	EA		0972900-7420	NETWORK SN74LS20N	
0077A					UD11 UE08 UK02	
0083	00001.000	EA		0539370-0347	RES FIX FILM 402 OHM 1% .25 WATT	COR - NA55
0083A					R04	
0084	00001.000	EA		0539370-0334	RES FIX FILM 294 OHM 1% .25 WATT	COR - NA55
0084A					R01	
0085	00001.000	EA		0539370-0345	RES FIX FILM 383 OHM 1% .25 WATT	COR - NA55
0085A					R03	
0086	00002.000	EA		0539370-0498	RES FIX FILM 15.0K OHM 1% .25 WATT	COR - NA55
0086A					R06 R10	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-5001 — REV AV

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/05/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 7 of — PART NUMBER LM0937505-5001 — REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0087	00001.000	EA		0972976-0098	RES,FIX,3.0K OHM, 5%,0.25 W,CARBON COMP.	
0087A					R02	
0088	00012.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0088A					R05 R08 R09 R11 R12 R13 R14	
0088B					R17 R18 R19 R20 R35	
0089	00004.000	EA		0539370-0332	RESISTOR, 280 OHMS .25W 1% FX MEDAL FILM	016299-NA55 100PPM/C
0089A					R21 R22 R23 R24	
0102	00001.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N
0102A					UG12	
0103	00023.000	EA		0972946-0047	RES FIX 180 OHM 5 % .25 W CARBON FILM	ROH - R-25
0103A					R15 R16 R25 THRU R27 R29	
0103B					THRU R34 R37 R39 THRU R44	
0103C					R49 R64 R77 R79 R81	
0104	00023.000	EA		0972946-0052	RES FIX 300 OHM 5 % .25 W CARBON FILM	ROH - R-25
0104A					R28 R50 R51 R53 THRU R63	
0104B					R65 THRU R67 R69 R70 R75	
0104C					R76 R78 R80	
0105	00001.000	EA		0222222-7132	NETWORK SN74132N	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO-INSERTED PARTS LIST FOR 937505-0001

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM0937505-5001 — REV AV

TI 25789

TEXAS INSTRUMENTS INCORPORATED

DATE 01/05/82

LIST OF MATERIAL

ORIGINAL COPY

PAGE 8 of

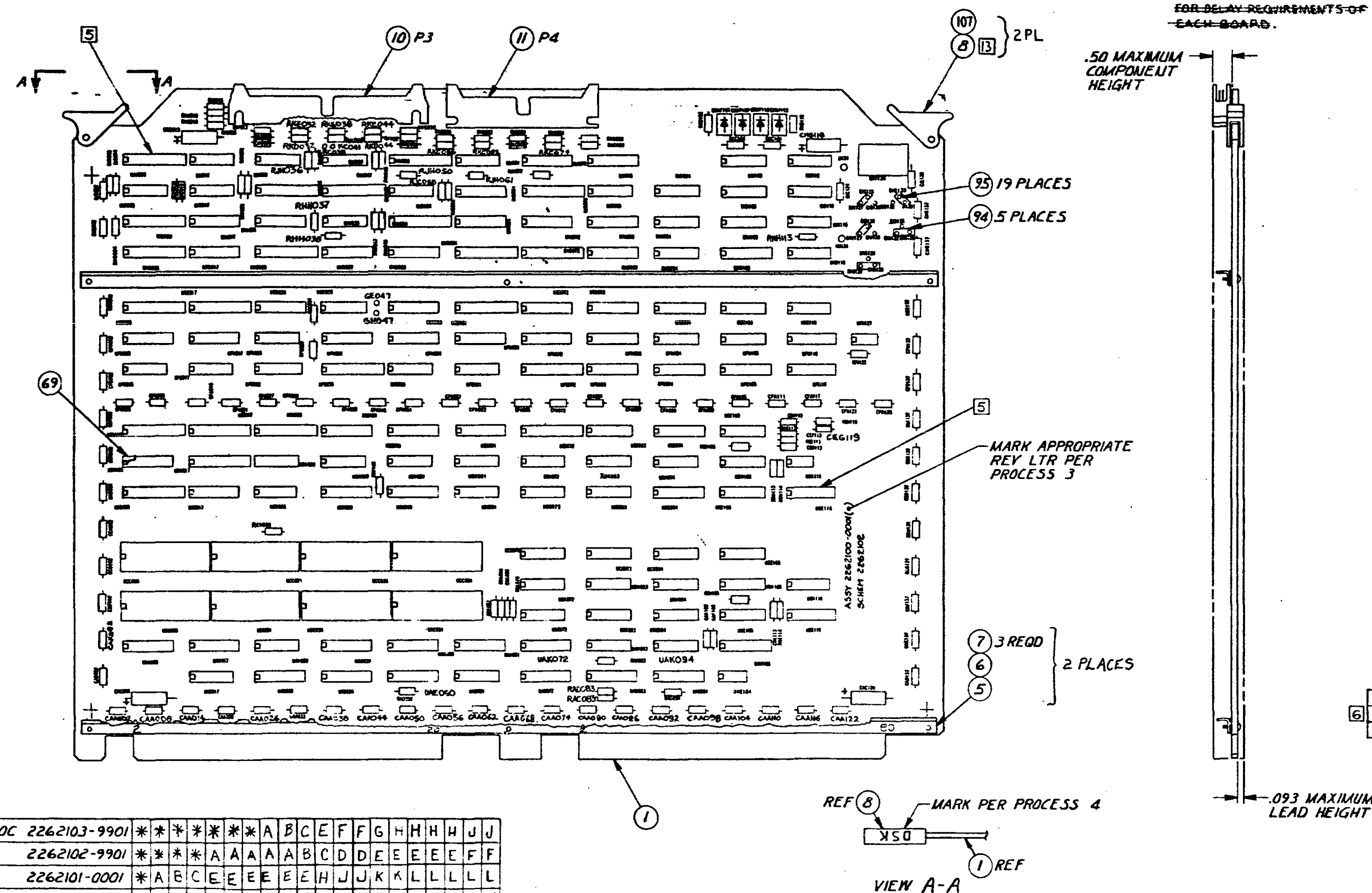
PART NUMBER LM0937505-5001 REV AV

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0105A					UH08	
0107	00002.000	EA		0533370-0349	RES FIX FILM 422 OHM 1% .25 WATT	COR - NA55
0107A					R07 R38	
0109	00001.000	EA		0972753-0021	CAP.,1200PF, 2%, 25V, CERAMIC, AX.LEAD	
0109A					C05	
0110	00001.000	EA		0219402-7410	IC, SN74S10N	
0110A					UP09	
0111	00001.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N
0111A					UB11	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						AUTO-INSERTED PARTS LIST FOR 937505-0001
APPD MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0937505-5001 REV AV

TI 25789

NOTES: UNLESS OTHERWISE SPECIFIED:
1. PIN 1 OF ALL IC PACKAGES IS AT LOWER LEFT CORNER AS VIEWED
~~2 SEAL ITEM 7 PER PROCESS 5~~
3. XDK006 IS TEST SOCKET
~~4 S1 AND S2 ARE NOT USED~~
5 UJJ006 AND UDE116 ARE SPARE LOCATIONS
6 ITEM 103 IN THE -0001 LM CONSISTS OF COMPONENTS WHICH ARE AUTO-INSERTED AND CONTAINED IN THE -5001 LM
7 REWORK FOR ASSY REV C AND LOWER
 A) REPLACE CAPACITOR CEH113 WITH 1200pF, ITEM 104
 B) REPLACE RESISTOR RBE114 WITH 3K OHMS, ITEM 83
 C) REPLACE IC UBK094 WITH 74S32, ITEM 105
 D) REPLACE IC VEE083 WITH 74S10, ITEM 106
8 REWORK FOR PWB 2262101 REV C & LOWER (USE 30 AWG WIRE)
 A) CUT PIN UBK116-3, ADD WIRE VBK094-6 TO UBE116-13
 B) CUT PINS UDK094-3 & 4, ADD WIRE UDK094-4 (ETCH PAD) UDE083-8
 C) CUT PIN UBE105-1, ADD WIRE UBE105-1 (PKG) TO VBE083-8
 D) ADD WIRE UCE083-3 TO UBE083-10
 E) ADD WIRE UBE083-6 TO UBE083-9
 F) CUT UHD116-11 ADD UJD105-6 TO UHD116-11 (PKG)
~~9 NO CAPACITOR AT CEG119 INSTALLED AT BOARD ASSY. IT MAY BE ADDED AT UNIT TEST FOR DELAY REQUIREMENTS OF EACH BOARD.~~



DWG NO 2262100 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN435780 (D) (1) FOLLOWING ITEMS DELETED FROM -0001 LM AND ADDED TO -5001 LM; 1, 15 THRU 36, 38 40, 44 THRU 53, 55 THRU 60, 62, 65, 66, 70, 74 & 97 (2) ON -0001 LM QTY ITEM 24 WAS 7 (3) ADDED NOTE 6 (4) UPDATED REV LEVEL BLOCK	5-15-80	J.R.
B	CN 456122 (D) C. (1) UPDATED PICTORIAL AS PER REV B PWB (2) UPDATED REV LEVEL BLOCK	5-15-80	J.R.
C	CN472721 (D) C. (1) ON -0001 L/M ITEM 80 WAS 539370-0327 (2) UPDATED REV LEVEL BLOCK	5-15-80	J.R.
D	CN472787 (B) (1) REVISED PER EXTENSIVE ENGINEERING CHANGES	7/11/80	
E	CN 472710 (D) (1) ON -0001 LM ADDED ITEM 107 (2) DELETED PROCESS 5 (3) UPDATED REV LEVEL BLOCK	8-26-80	J.R.
F	CN 459029 (D) (1) ON -0001 LM QTY ITEM 72 & 85 WAS 72 & 4 RESP (2) DELETED THE FOLLOWING FROM -0001 LM & ADDED TO -5001 LM: ITEMS 79 THRU 84, 96, 98, 99 101 & 102 (3) ON -5001 ADDED ITEMS 72 & 85 (4) UPDATED REV LEVEL BLOCK	8-26-80	J.R.
G	CN472799 (E) (1) UPDATED REV LEVEL BLOCK	8-26-80	J.R.
H	CN461253 (D) J. Smith (1) DELETED ITEMS 96 & 96A FROM -5001 LM (2) ADDED ITEMS 96 & 96A TO -0001 LM (3) UPDATED REV LEVEL BLOCK	11-11-80	J.R.
J	CN472917 (E) J. Smith (1) UPDATED REV LEVEL BLOCK	11-11-80	J.R.
K	CN461294 (D) R. (1) DELETED ITEMS 37, 39, 41, 42, 63, 64, 100, 105, AND 106 FROM -0001 LM AND ADDED TO -5001 LM (2) UPDATED REV LEVEL BLOCK	1-30-81	J.R.
L	CN 484091 (B) D. (1) ADDED NOTE 10 (2) UPDATED REV LEVEL BLOCK (3) SH1 ZB7 WAS CCK028 (4) ADDED SH.2	4-27-81	E.
M	CN476132 (D) D. (1) REVISED PER EXTENSIVE ENGR LM CHANGE	4-27-81	E.
N	CN476186 (B) D. (1) ON LM-5001 ITEM 81 DASH NO. WAS -337 & ITEM 79 DASH NO. WAS -339 (2) ON LM-1 ITEM 75A QTY WAS 2 & ITEM 78 DASH NO. WAS -48 & REF DES WAS CBE068 (3) DELETED NOTE 9 & 4 (4) ADDED NOTE 11 (5) UPDATED REV LEVEL BLOCK	7-16-81	J.R.

(REVISIONS CON'T ON SH 2)

	PART NUMBER	DESCRIPTION
	2262100-5001	AUTO INSERTION TAPE FOR -0001
6	2262100-0001	CDC DISK CONTROLLER

REV LEVEL																					
TEST PROC	2262103-9901	*	*	*	*	*	*	*	A	B	C	E	F	F	G	H	H	H	H	J	J
LOGIC	2262102-9901	*	*	*	*	A	A	A	A	A	B	C	D	D	E	E	E	E	E	F	F
PWB	2262101-0001	*	A	B	C	E	E	E	E	E	E	H	J	J	K	K	L	L	L	L	L
ASSEMBLY	2262100-0001	*	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

SEQ NO	PROCESS IDENT	PROCESS F-SPEC	CLASSIFICATION NO	CLASSIFICATION ADDITIONAL	NOTES
~~5~~	~~SEAL~~	~~630-01~~	~~14~~	~~USING ITEMS 87 AND 88~~	
4	MARK	100-07	712	CLR BLACK, TYPE 6	
3	MARK	100-02	21	HGT .12, CLR BLACK	
2	SLDR	127-01	00		
1	SLDR	124-02	00		

PROCESSES — FOR CORRELATION TO GOV'T IND SPECIFICATIONS SEE TI DRAWING 729467

REV STATUS OF SHEETS			
REV	W	W	
SHEET	1	2	

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

NEXT ASSY	USED ON
937500	7506

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE: .013 THRU .125 +.004 −.001; .126 THRU .250 +.005 −.001; .251 THRU .500 +.006 −.001; .501 THRU .750 +.008 −.001; .751 THRU 1.000 +.010 −.001; 1.001 THRU 2.000 +.012 −.001

DWN C. Molina 3-21-79
ENGR 5-14-79
RLSE 5-23-79

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

CDC DISK CONTROLLER

SIZE D FSCM NO 96214 DWG NO 2262100

SCALE NONE SHEET 1 OF 2

32 LM

DWG NO 2262100 REV W

NOTES CONT:

10. REWORK FOR PWB 2262101 REV "H" AND BELOW:
   A. CUT UJJ061 PIN 8 (SN 7406)
   B. CUT UJJ061 PIN 10 (SN 7406)

11. REWORK FOR PWB 2262101 REV "J" AND BELOW:
   A. CUT PIN 11 AT UDK039
   B. ADD 30 AWG WIRE FROM UDE061-9 TO UEE028-3
   C. INSTALL A 220 pF CAPACITOR AT CEG119, ITEM 78, P/N 972927-0035
   D. INSTALL A 510 pF CAPACITOR AT CBE068, ITEM 75, P/N 972927-0044
   E. INSTALL A 383 OHM RESISTOR AT REH119, ITEM 81, P/N 539370-0345
   F. INSTALL A 402 OHM RESISTOR AT RBE067, ITEM 79, P/N 539370-0347

12. ITEM 79 (RBE067), ITEM 80 (REE113), AND ITEM 81 (REH119) VALUES WILL BE SELECTED PER THE UNIT TEST PROCEDURE AND INSTALLED AT UNIT TEST.

13. DISCARD STEEL ROLL PIN IF SUPPLIED WITH ITEM 8

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
		CONT FROM SH 1		
	P	CN 454055 (D) (1) 1 LM; ITEM 95 PN WAS 0972742-0001	7-16-81	
		DELETED ITEMS 54, 54A, 61, 61A & 95; ADDED ITEMS 79, 79A, 80, 80A, 81 & 81A (2) -5001 LM; ADDED ITEMS 54, 54A, 61 & 61A, DELETED ITEMS 79, 79A, 80, 81, AND 81A (3) ADDED NOTE 12 (4) UPDATED REVISION LEVEL BLOCK		
	R	CN 476200 (D) (1) UPDATED REV LEVEL BLOCK	10-6-81	
	T	CN 484920 (D) (1) -0001 LM; ITEM 86 PN WAS 772925-0001 ADDED B6B, C8 D (2) UPDATED REV LEVEL BLK	10-21-81	
	U	CN 487756 (D) (1) LM-0001 ADDED ITEM 107 (2) SH 1 Z D-4 ADDED BALLOON ITEM 107 (3) SH 2 ADDED NOTE 13 (4) UPDATED REV LEVEL BLOCK	3-4-82	
	V	CN 485701 (C) (1) LM-0001 ITEM 8 PN WAS 539370-0345 (2) UPDATED REV LEVEL BLOCK (3) SH 1, Z B-8 C4 E D-4 DELETED BALLOONS FOR ITEM 9, 71 AND 107 AND CUT-AWAY LINES	3-4-82	
	W	CN 465477 (D) (1) SH 1, Z C-8, ITEM 69 WAS "4 PL" (2) SI, Z D-8, REVISED NOTE 3 (3) UPDATED REV LEVEL BLOCK	3-16-82	

TEXAS INSTRUMENTS | DSN | DATE 7/10/81 | SIZE D | FSCM NO 96214 | DRAWING NO 2262100 | REV W | SCALE NONE | SHEET 2

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of — PART NUMBER LM2262100-0001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	REF	EA		2262102-9901	LOGIC DIAGRAM,CDC DISK CONTROLLER	
0003	REF	EA		2262103-9901	TEST PROCEDURE,CDC DISK CONTROLLER	
0004	REF	EA		2262104-9901	SPECIFICATION,CDC DISK CONTROLLER	
0005	00002.000	EA		0945239-0001	BRACKET-STIFFENER, PWB, 14IN	
0006	00002.000	EA		0944954-0001	INSULATOR, PWB, 14IN	
0007	00006.000	EA		0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	
0008	00002.000	EA		0533844-0001	EJECTOR, NYLON, NON-LOCKING, PWB	
0010	00001.000	EA		0972137-0010	CONNECTOR,P.C.HEADER 50 CONTACTS	BEI - 65483-020
0010A					P3	
0011	00001.000	EA		0972706-0005	HEADER, CONN, RIGHT ANGLE, 40 CONTACTS	075037-3495-1002
0011A					P4	
0012	00001.000	EA		0972537-0001	DIODE,LED 550-0103 50 MA 3 V	DIA --550-0103
0012A					CRKF113	
0013	00003.000	EA		0972537-0002	DIODE,LED GREEN RT ANGLE	072619-550-0206
0013A					CRKF104 CRKF107 CRKF110	
0014	00001.000	EA		0995059-0013	OSCILLATOR,RF,CRYSTAL 5.000MHZ 0.01%	001537-K-1100 A
0014A					UJJ128	
0069	00001.000	EA		2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	SEE T -I DRAWING

DRAFTSMAN — DATE — CKD DRAFTSMAN H. Rowell 1-7-82 — DATE — DESIGN ENGINEER — DATE — TITLE: CDC DISK CONTROLLER

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. 7506 — PART NUMBER LM2262100-0001 — REV W

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM2262100-0001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0069A					XDK006	
0072	00003.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0072A					CAD002 CAD137 CAA002	
0073	00001.000	EA		0972927-0041	CAP FIX MICA 500V 390 PF 5 %	SEE TI- DRAWING
0073A					CKC026	
0075	00003.000	EA		0972927-0044	CAP FIX MICA 300V 510 PF 5 %	QPL -CM05F511J3C
0075A					CEF113 CBE069 CBE068	
0078	00001.000	EA		0972927-0035	CAP FIX MICA 500V 220 PF 5 %	SEE TI- DRAWING
0078A					CEG119	
0079	00001.000	EA		0539370-0347	RES FIX FILM 402 OHM 1% .25 WATT	COR - NA55
0079A					RBE067	
0080	00001.000	EA		0539370-0332	RESISTOR, 280 OHMS .25W 1% FX MEDAL FILM	016299-NA55 100PPM/C
0080A					REE113	
0081	00001.000	EA		0539370-0334	RES FIX FILM 294 OHM 1% .25 WATT	COR - NA55
0081A					REH119	
0086	00001.000	EA		2220184-0003	SWITCH,ROCKER,4-POS,,.48" LONG,SEALED	SEE TI- DRAWING
0086A					UAE104	
0086B					PN 772923-0001 MAY BE USED	

DRAFTSMAN — DATE — CKD DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CDC DISK CONTROLLER

APPD MFG — DATE — APPD PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2262100-0001 — REV W

TI 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM2262100-0001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0086C					AS AN ALTERNATE PART FOR	
0086D					ITEM 86	
0094	00005.000	EA		0972713-0001	PLUG, JUMPER, I.C., 0.300 INCH	
0095	00019.000	EA		0996864-0001	CONNECTOR,SOCKET PCB	022526-75060-007
0095A					KC038 KC041 EJG128 EJG133	
0095B					EJD127 EJD130 EJD132 EJD135	
0095C					EJB128 EJB133 EHJ127 EHJ130	
0095D					EHJ132 EHJ135 EHG128 EHD127	
0095E					EHD130 GE047 GH047	
0096	00004.000	EA		0972924-0001	CAP FIX TANT SOLID 6.8 MFD 10 % 6 VOLT	QPL -M39003/1-2242
0096A					CKD013 CKC116 CAC124 CAC005	
0103	00001.000	EA		2262100-5001	AUTO INSERTION TAPE FOR 2262100-0001	
0104	00001.000	EA		0972753-0021	CAP.,1200PF, 2%, 25V, CERAMIC, AX.LEAD	
0104A					CEH113	
0107	00002.000	EA		0085936-0065	EYELET,ROLLED FLANGE,.089 D.D. X .312 LG	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CDC DISK CONTROLLER

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2262100-0001 — REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 1 of — PART NUMBER LM2262100-5001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		2262101-0001	PWB,CDC DISK CONTROLLER	
0015	00001.000	EA		0240000-7400	NETWORK-SN74H00N	
0015A					UDE083	
0016	00003.000	EA		0972900-7402	NETWORK,SN74LS02N	
0016A					UBK105 UDE028 UCE072	
0017	00001.000	EA		0219402-7404	NETWORK SN74S04N	
0017A					UDK050	
0018	00003.000	EA		0222222-7406	NETWORK SN7406N	
0018A					JJJ017 UJJ028 UJJ061	
0019	00002.000	EA		0222222-7407	NETWORK-SN7407N	TI- -SN7407N
0019A					UBE072 UEE105	
0020	00002.000	EA		0972749-0001	NETWORK, SN74LS08N	
0020A					UFK094 UFE006	
0021	00001.000	EA		0219402-7408	NETWORK SN74S08N	TI- -SN74S08N
0021A					UCE094	
0022	00001.000	EA		0972900-7410	NETWORK SN74LS10N	
0022A					UHJ116	
0023	00001.000	EA		0240000-7411	NETWORK-SN74H11N	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO — PART NUMBER LM2262100-5001 — REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 2 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0023A					UBE094	
0024	00007.000	EA		0972784-0002	NETWORK SN74LS14N	
0024A					UAK094 UDK094 UGE039	
0024B					UHJ105 UJD006 UJJ039	
0024C					UDK028	
0025	00001.000	EA		0972813-0001	NETWORK-SN74LS21N	
0025A					UJJ105	
0026	00001.000	EA		0972814-0001	NETWORK-SN74LS27N	
0026A					UGE116	
0027	00001.000	EA		0972900-7430	NETWORK SN74LS30N	TI -SN74LS30N
0027A					UJD083	
0028	00002.000	EA		0972900-7432	NETWORK SN74LS32N	TI -SN74LS32N
0028A					UBK116 UBE083	
0029	00001.000	EA		0222222-7438	NETWORK SN7438N	
0029A					UJD050	
0030	00001.000	EA		0972900-7451	NETWORK SN74LS51N	TI -SN74LS51N
0030A					UJD094	
0031	00001.000	EA		0240000-7451	NETWORK-SN74H51N	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 3 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0031A					UDK072	
0032	00010.000	EA		0972900-7474	NETWORK SN74LS74N	
0032A					UDE105 UDE072 UFK028 UHD094	
0032B					UJD017 UHD116 JJJ116 UHJ094	
0032C					UJD116 UHJ039	
0033	00001.000	EA		0219402-7474	NETWORK SN74S74N	
0033A					UBK072	
0034	00001.000	EA		0972900-7109	NETWORK SN74LS109N	TI -SN74LS109N
0034A					UGE094	
0035	00006.000	EA		0972782-0001	NETWORK SN74LS132N	TI -SN74LS132N
0035A					UBE105 UCE083 UDK061 UDK039	
0035B					UJD105 UFK105	
0036	00003.000	EA		0972900-7174	NETWORK SN74LS174N	
0036A					UEE094 UFK039 UHJ017	
0037	00002.000	EA		0996089-0001	IC,SN74LS240N,LINE DRIVERS	01295-SN74LS240N
0037A					UJD072 UHJ050	
0038	00004.000	EA		0996588-0002	IC,QUADRUPLE BUS TRANSCEIVER SN74LS243N	02195S-N74LS243N
0038A					UAE061 UAE017 UAK028 UAK083	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — **LIST OF MATERIAL** — ORIGINAL COPY PAGE 4 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0039	00002.000	EA		0995089-0004	IC,SN74LS244N LINE DRIVER	-SN74LS244N
0039A					UJD028 UJJ050	
0040	00001.000	EA		0972667-0001	NETWORK,SN74LS279N	
0040A					UDE094	
0041	00001.000	EA		0995307-0001	IC,SN74S373,OCTAL D, FLIPFLOP	TI -SN74S373
0041A					UEE028	
0042	00003.000	EA		0995201-0001	IC,SN74S374N,EDGE-TRIGGERED FLIP-FLOPS	TI -SN74S374N
0042A					UJD039 UEE072 UHD061	
0043	00001.000	EA		0222222-7497	NETWORK SN7497N	
0043A					UFE105	
0044	00002.000	EA		0972900-7138	NETWORK SN74LS138N	TI -SN74LS138N
0044A					UHD050 UJJ072	
0045	00001.000	EA		0219402-7138	NETWORK SN74S138N	
0045A					UEE039	
0046	00002.000	EA		0219402-7139	NETWORK SN74S139N	
0046A					UEE050 UFE028	
0047	00001.000	EA		0222222-7148	NETWORK SN74148N	
0047A					UFE094	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2262100-5001 REV W

T.I. 25788

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — **LIST OF MATERIAL** — ORIGINAL COPY PAGE 5 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0048	00001.000	EA		0972900-7153	NETWORK SN74LS153N	TI -SN74LS153N
0048A					UHD105	
0049	00001.000	EA		0219402-7153	NETWORK SN74S153N	TI -SN74S153N
0049A					UDE050	
0050	00013.000	EA		0972686-0001	NETWORK-QUAD MULTIPLEXER, SN74LS157N	
0050A					UAK039 UAK105 UAK017 UDE039	
0050B					UDE017 UHJ061 UHD017 UHJ072	
0050C					UFK017 UFK072 UGE072 UGE050	
0050D					UGE028	
0051	00003.000	EA		0972669-0001	NETWORK,SN74LS163N	
0051A					UHD039 UHJ028 UFE116	
0052	00003.000	EA		0219402-7182	NETWORK SN74S182N	TI -SN74S182N
0052A					UAK050 UAK006 UAK072	
0053	00004.000	EA		0996427-0001	IC,SN74LS195AN 4-BIT PARALLEL-ACCESS	001295-SN74LS195AN
0053A					UFK083 UFK061 UHJ083 UHD083	
0054	00004.000	EA		0995564-0001	IC,SN74S225N 16 X 5-BIT FIFO MEMORY	001295-SN74S225N
0054A					UFE072 UHD072 UHD028 UGE061	
0055	00004.000	EA		0995136-0002	IC,SN74LS258N,DATA SELECTORS/MULTIPLEXER	TI -SN74LS258N

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY PAGE 6 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0055A					UEE061 UFE083 UGE083 UJJ083	
0056	00002.000	EA		0995023-0001	IC,LOW POWER SCHOTTKY 8 BIT SN74LS259N	TI -SN74LS259N
0056A					UFK050 UJD061	
0057	00001.000	EA		0972159-7265	NETWORK, SN74265N	
0057A					UFK116	
0058	00001.000	EA		0947573-0001	PROM,32X8,BOOLEAN,MTC NO.1	
0058A					UFK006	
0059	00001.000	EA		0972787-0004	NETWORK SN74LS368N	
0059A					UAE039	
0060	00002.000	EA		0219402-7157	NETWORK SN74S157N	
0060A					UAE072 UAK061	
0061	00003.000	EA		0995102-0001	IC,SN74S482N MICRO-ADDRESS GENERATOR	TI -SN74S482N
0061A					UHJ006 UHD006 UGE006	
0062	00002.000	EA		0974674-0001	NETWORK SN75138N	
0062A					UAE094 UBE116	
0063	00008.000	EA		0974859-0001	NETWORK, BI-POLAR 2BIT PROCESSOR -3002	
0063A					UCC006 UCC021 UCC036 UCC051	
0063B					JBE006 UBE021 UBE036 UBE051	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD. MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY PAGE 7 of — PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0064	00001.000	EA		0974866-0001	NETWORK,CRC GENERATOR	FCD --9401
0064A					UGE105	
0065	00001.000	EA		0972188-0001	NETWORK,NE555V,MONOLITHIC TIMING,LINEAR	ST -NE555V
0065A					UDK115	
0066	00003.000	EA		0974849-0001	NETWORK, DM8136	
0066A					UAE050 UAE083 UAE028	
0067	00001.000	EA		0972899-0004	NETWORK, DUAL STATIC SHIFT REGISTER 1328	001295-TMS3129NC
0067A					UFK127	
0070	00001.000	EA		0240000-7474	NETWORK-SN74H74N	
0070A					UCE105	
0072	00069.000	EA		0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	
0072A					CAK102 CFJ125 CJC002 CHG002	
0072B					CGD002 CFH002 CFB002 CEF002	
0072C					CDK002 CDD002 CCH002 CCB002	
0072D					CBF002 CAK002 CJE136 CHK137	
0072E					CHD137 CGD137 CFH137 CFB137	
0072F					CEF137 CDK137 CDD137 CCH137	
0072G					CCB137 CBF137 CAK137 CFA003	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD. MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 8 of — PART NUMBER LM2262100-5001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0072H					CFA009 CFA015 CFA021 CFA027	
0072J					CFA033 CFA039 CFA045 CFA051	
0072K					CFA057 CFA063 CFA059 CFA075	
0072L					CFA081 CFA087 CFA093 CFA099	
0072M					CFA105 CFA111 CFA117 CFA123	
0072N					CFA129 CAA008 CAA014 CAA020	
0072P					CAA026 CAA032 CAA038 CAA044	
0072R					CAA050 CAA056 CAA062 CAA068	
0072T					CAA074 CAA080 CAA086 CAA092	
0072U					CAA098 CAA104 CAA110 CAA116	
0072V					CAA122	
0074	00003.000	EA		0972900-7420	NETWORK SN74LS20N	
0074A					UDE061 UBK083 UFE061	
0076	00001.000	EA		0972757-0037	CAP FIX CER 0.1MF 10% 50V	
0076A					CED113	
0077	00001.000	EA		0972757-0025	CAP FIX CER .01MF 10% 50V	
0077A					CBE113	
0082	00002.000	EA		0539370-0498	RES FIX FILM 15.0K OHM 1% .25 WATT	COR - NA55

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2262100-5001 — REV W

T.I. 26709

TEXAS INSTRUMENTS INCORPORATED — DATE 01/06/82 — LIST OF MATERIAL — ORIGINAL COPY — PAGE 9 of — PART NUMBER LM2262100-5001 — REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0082A					RDH113 RDH114	
0083	00001.000	EA		0972976-0098	RES,FIX,3.0K OHM, 5%,0.25 W,CARBON COMP,	
0083A					RBE114	
0084	00012.000	EA		0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	COR - NA55
0084A					RBJ105 RAK103 RAD050 RHH116	
0084B					RAD094 RDE048 RED105 RCK028	
0084C					RAJ083 RAD083 RJC124 RAC083	
0085	00004.000	EA		0539370-0332	RESISTOR, 280 OHMS .25W 1% FX MEDAL FILM	016299-NA55 100PPM/C
0085A					RKC109 RKC104 RKD116 RKD102	
0089	00001.000	EA		0937504-0013	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 1	
0089A					UDE006	
0090	00001.000	EA		0937504-0014	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 2	
0090A					UDK017	
0091	00001.000	EA		0937504-0015	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 3	
0091A					UEE006	
0092	00001.000	EA		0937504-0015	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 4	
0092A					UGE017	
0093	00001.000	EA		0937504-0017	PROM,CONTROL,10 MEGA BYTE CONT,NUMBER 5	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: AUTO INSERTION TAPE FOR 2262100-0001

APPD.-MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM2262100-5001 — REV W

T.I. 26709

TEXAS INSTRUMENTS INCORPORATED

DATE 01/06/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 10 of

PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0093A					UEE017	
0097	00001.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N
0097A					UFE050	
0098	00023.000	EA		0972946-0047	RES FIX 180 OHM 5 % .25 W CARBON FILM	ROH - R-25
0098A					RFG037 RKE038 RHH047 RKE044	
0098B					RKD062 RJH047 RJC059 RKE050	
0098C					RJH061 RKE032 RHH038 RJD004	
0098D					RKC068 RKD074 RKC050 RKD056	
0098E					RKF013 RJH037 RKJ018 RJD025	
0098F					RKE026 RJC015 RKC080	
0099	00023.000	EA		0972946-0052	RES FIX 300 OHM 5 % .25 W CARBON FILM	ROH - R-25
0099A					RJC014 RGC037 RKD038 RKC062	
0099B					RKD068 RKC074 RKD050 RKC056	
0099C					RKG018 RJH036 RKD080 RKD044	
0099D					RHH048 RJH050 RKD032 RHH037	
0099E					RJD003 RKH018 RJD026 RKD026	
0099F					RJC058 RJH048 RJH072	
0100	00001.000	EA		0222222-7132	NETWORK SN74132N	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2262100-3001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2262100-5001 REV W

T.I. 25789

TEXAS INSTRUMENTS INCORPORATED

DATE 01/06/82 — **LIST OF MATERIAL** — ORIGINAL COPY — PAGE 11 of

PART NUMBER LM2262100-5001 REV W

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0100A					UDK105	
0101	00002.000	EA		0539370-0349	RES FIX FILM 422 OHM 1% .25 WATT	CDR - MA55
0101A					REG113 RBE070	
0102	00001.000	EA		0972946-0035	RES FIX 56.0 OHM 5 % .25 W.CARBON FILM	ROH - R-25
0102A					RHG004	
0105	00001.000	EA		0219402-7432	NETWORK SN74S32N	TI- -SN74S32N
0105A					UBK094	
0106	00001.000	EA		0219402-7410	IC, SN74S10N	
0106A					UEE083	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: AUTO INSERTION TAPE FOR 2252100-3001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM2262100-5001 REV W

T.I. 25789

NOTES: CONTINUED

6. JUMPER INSTALLED TO ALLOW THE CONTROLLER TO RUN LONG SELF DIAGNOSTIC TEST ON POWER UP. TO BE USED BY UNIT TEST ONLY.
7. SWITCH 5 AND 6 ARE NORMALLY NOT INSTALLED ON BOARD BUT MAY BE ADDED AS OPTION LATER.
8. THIS JUMPER (J5) IS USED TO INVERT THE PHASE OF THE WRITE CLOCK IF NEED BE.
9. J3, J4, J6, AND J7 ARE INSTALLED AS SHOWN AND ARE USED TO CHANGE THE DATA INTERFACE FROM A 10 MEGA BYTE DRIVE TO A 20 MEGA BYTE DRIVE.
10. ~~THIS CAPACITOR IS OMITTED AT ASSEMBLEY AND MAY BE ADDED AT UNIT TEST ON TIMING REQUIREMENTS.~~
11. RESISTOR VALUES 180 OHMS
12. RESISTOR VALUES 300 OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DEVICE TYPES PREFIXED WITH SN74
2. GROUND IS APPLIED TO PIN 7 OF ALL 14 PIN IC'S, PIN 8 OF ALL 16-PIN IC'S, PIN 10 OF ALL 20-PIN IC'S, AND PIN 14 OF ALL 28-PIN IC'S.
3. VCC IS APPLIED TO PIN 14 OF ALL 14-PIN IC'S; PIN 16 OF ALL 16-PIN IC'S, PIN 20 OF ALL 20-PIN IC'S, AND PIN 28 OF ALL 28-PIN IC'S.
4. DEVICE TYPE, PIN NUMBERS, AND LOCATION OF IC IS SHOWN AS FOLLOWS:

30 AND 04 = DEVICE TYPE
4 5 AND 6 = PIN NUMBERS
B06 AND C10 = LOCATION; FIRST LETTER DENOTES ROW, SECOND AND THIRD DIGITS DENOTE COLUMN. IC IS LOCATED AT THE INTERSECTION OF ROW AND COLUMN. (ALL LOCATIONS ARE PREFIXED ON THE ASSEMBLY SILKSCREEN BY THE LETTER "U".)

5. ALL RESISTORS ARE 1/4 WATT.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SDadson (1) REVISED W/CHG'D		
	B	SDadson (1) REVISED W/CHANGE		
		FORMAL RELEASE		
	C	CN424830(E) [illegible]	11/9/[illegible]	[illegible]
	D	CN428509(C) [illegible]	4-4-[illegible]	[illegible]
	E	CN428311(E) [illegible]	[illegible]	[illegible]
	F	CN[illegible]	[illegible]	[illegible]
	G	CN440[illegible](C) D Bark	12-4-[illegible]	[illegible]
	H	CN437962(E) [illegible]	3-18-[illegible]	[illegible]
	J	CN437992(E) C Patrick	4-1-[illegible]	[illegible]
	K	CN472751(E) [illegible]	5-3-[illegible]	[illegible]
	L	CN472792(E) [illegible]	5/[illegible]	[illegible]
	M	CN484095(E) D. [illegible]	4-27-81	[illegible]
	N	CN476189(D) D. [illegible]	6-5-81	[illegible]

REVISION STATUS	REV	N	K	K	N	H	H	C	C	H	C	H	N	M	D	B	H	C	J	L	B	C	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

UNLESS OTHERWISE SPECIFIED
• REMOVE ALL BURRS AND SHARP EDGES
• CONCENTRICITY MACHINED DIAMETERS .010 FIR
• DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
• IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
• INTERPRET DRAWING IN ACCORDANCE WITH MIL STD-100

HOLE TOLERANCE		
.013 THRU .125 +.004 -.001	.126 THRU .250 +.005 -.001	.251 THRU .500 +.006 -.001
.501 THRU .750 +.008 -.001	.751 THRU 1.000 +.010 -.001	1.001 THRU 2.000 +.012 -.001

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
• DIMENSIONS ARE IN INCHES
• TOLERANCES
ANGLES ±1°
3 PLACE DECIMALS ±.010
2 PLACE DECIMALS ±.02

MATERIAL

-2 QTY REQD	-1 QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST

DWN	DATE
CHK	
ENGR	
QA	
APVD	
CONTR NO	
DESIGN ACTIVITY RELEASE	
NO	

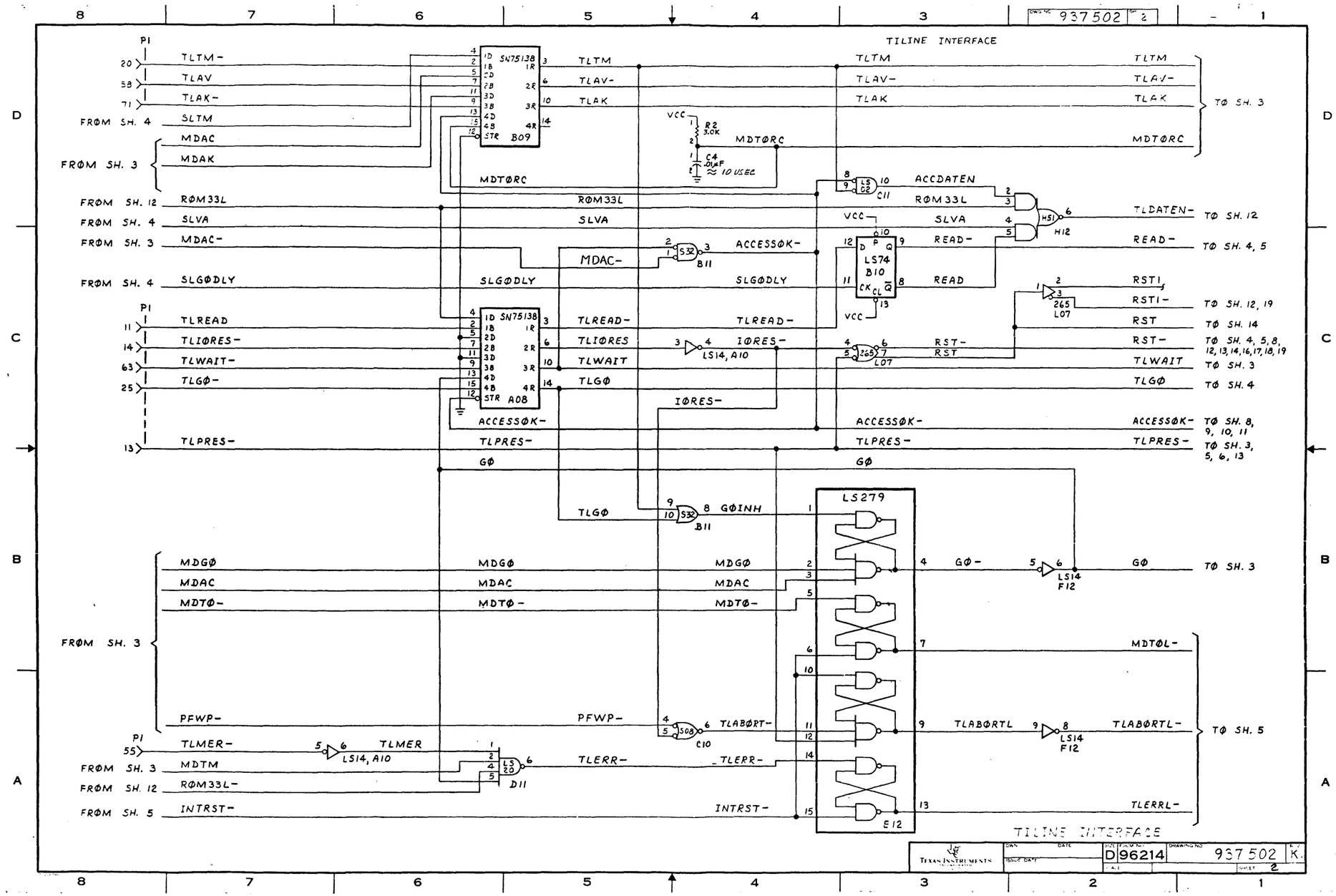
TEXAS INSTRUMENTS INCORPORATED
Equipment Group Dallas, Texas

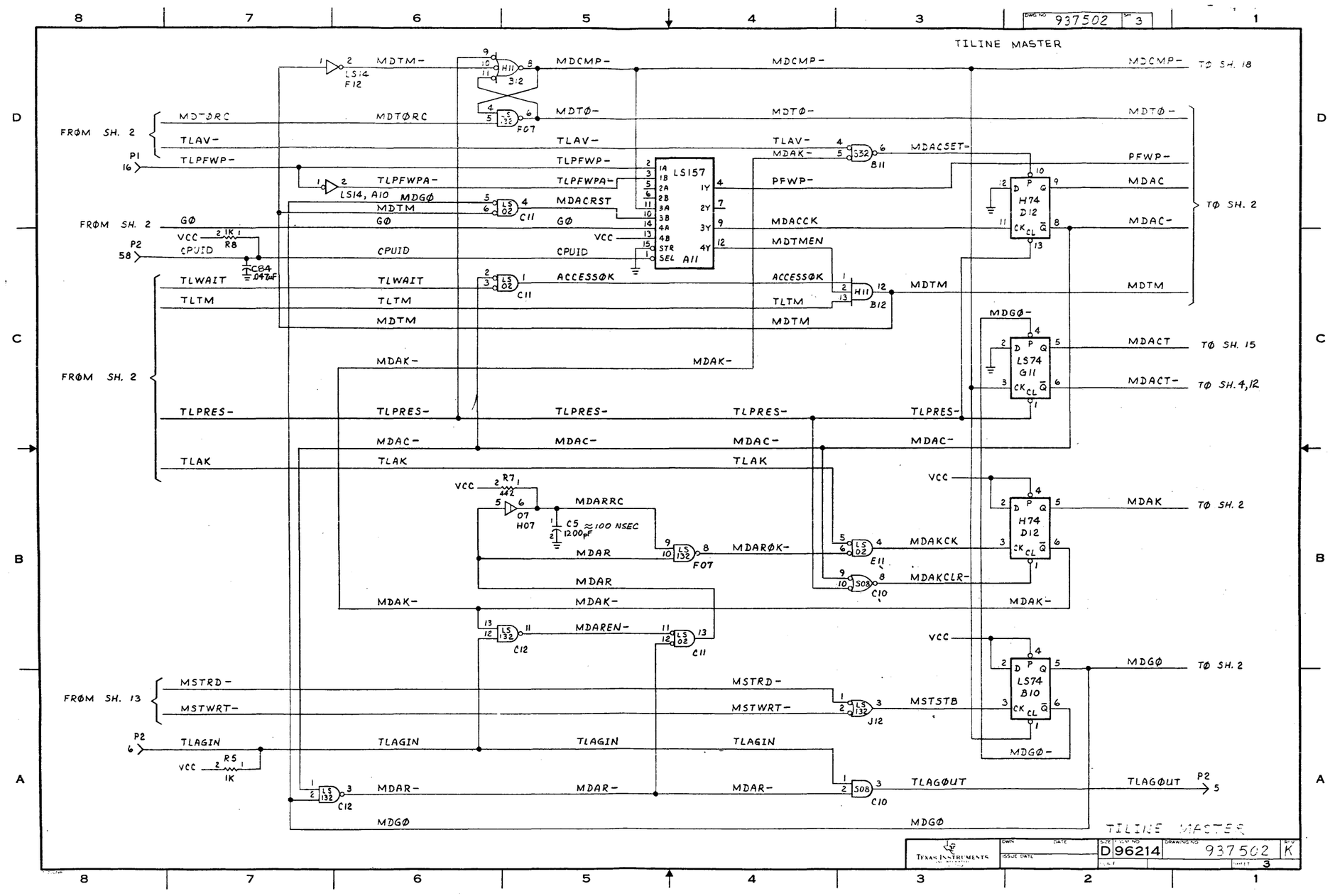
DIAGRAM, LOGIC, DETAILED, [illegible]

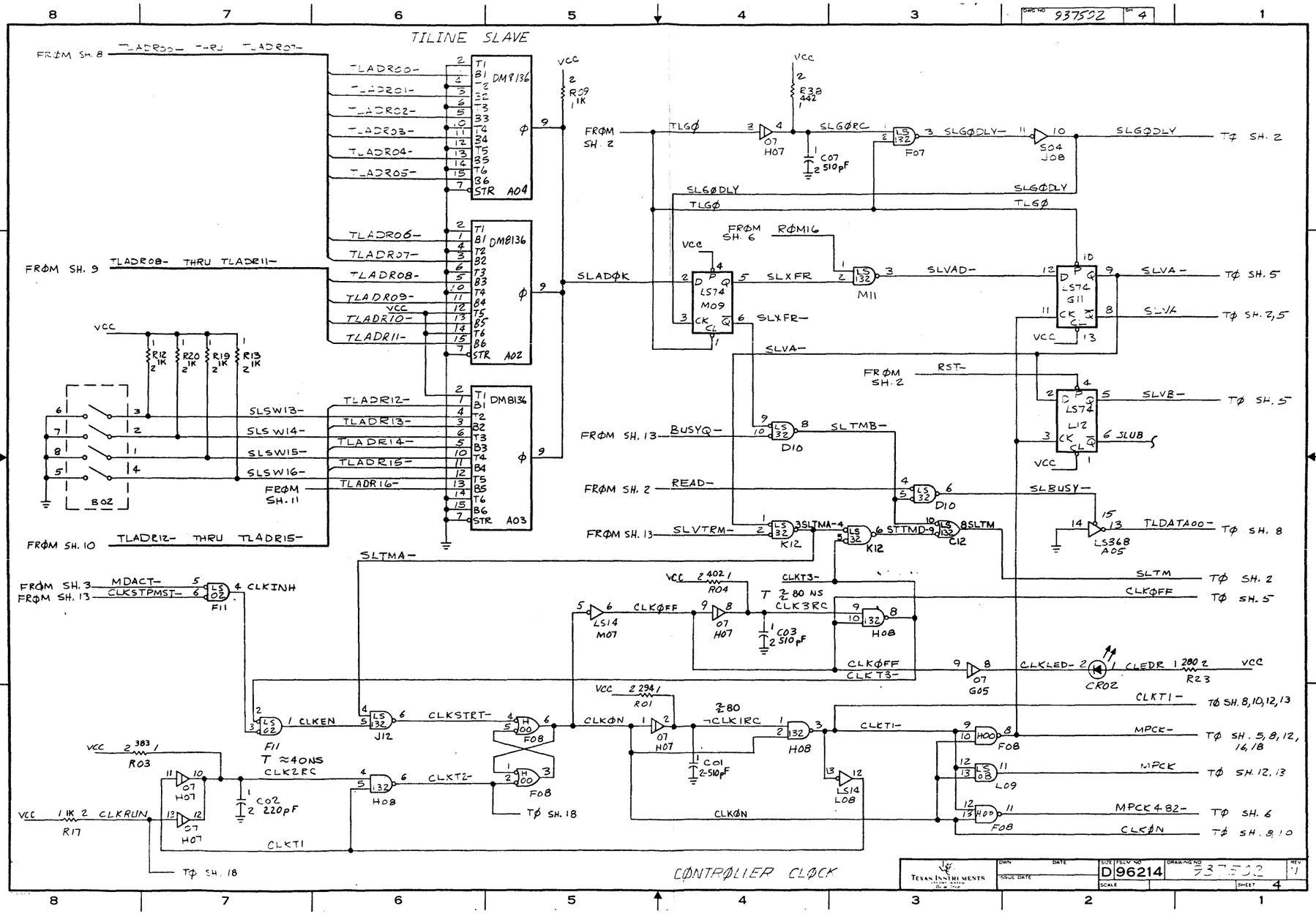
SIZE	CODE IDENT NO	DRAWING NO
D	96214	937502

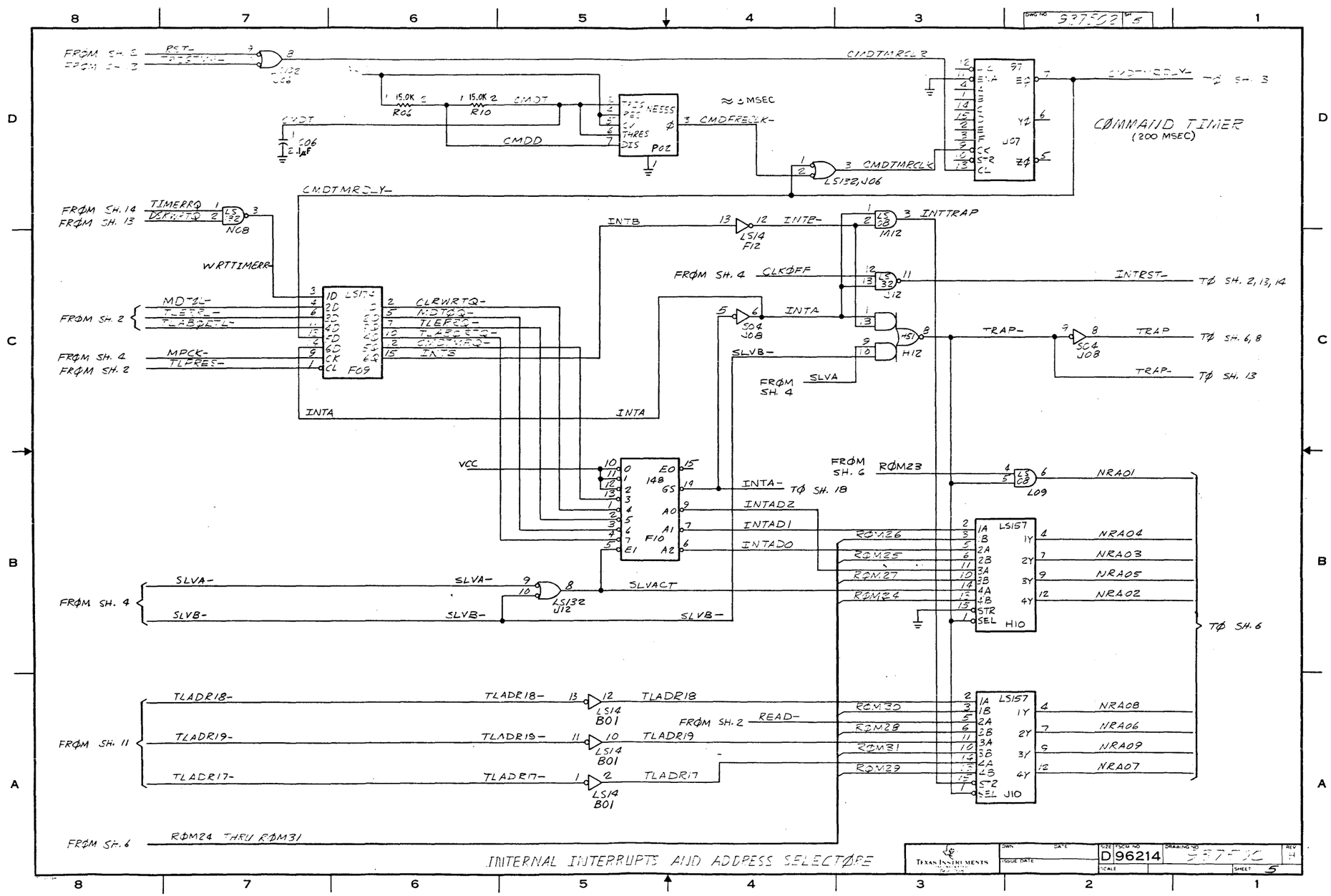
SCALE | SHEET 1 OF 22

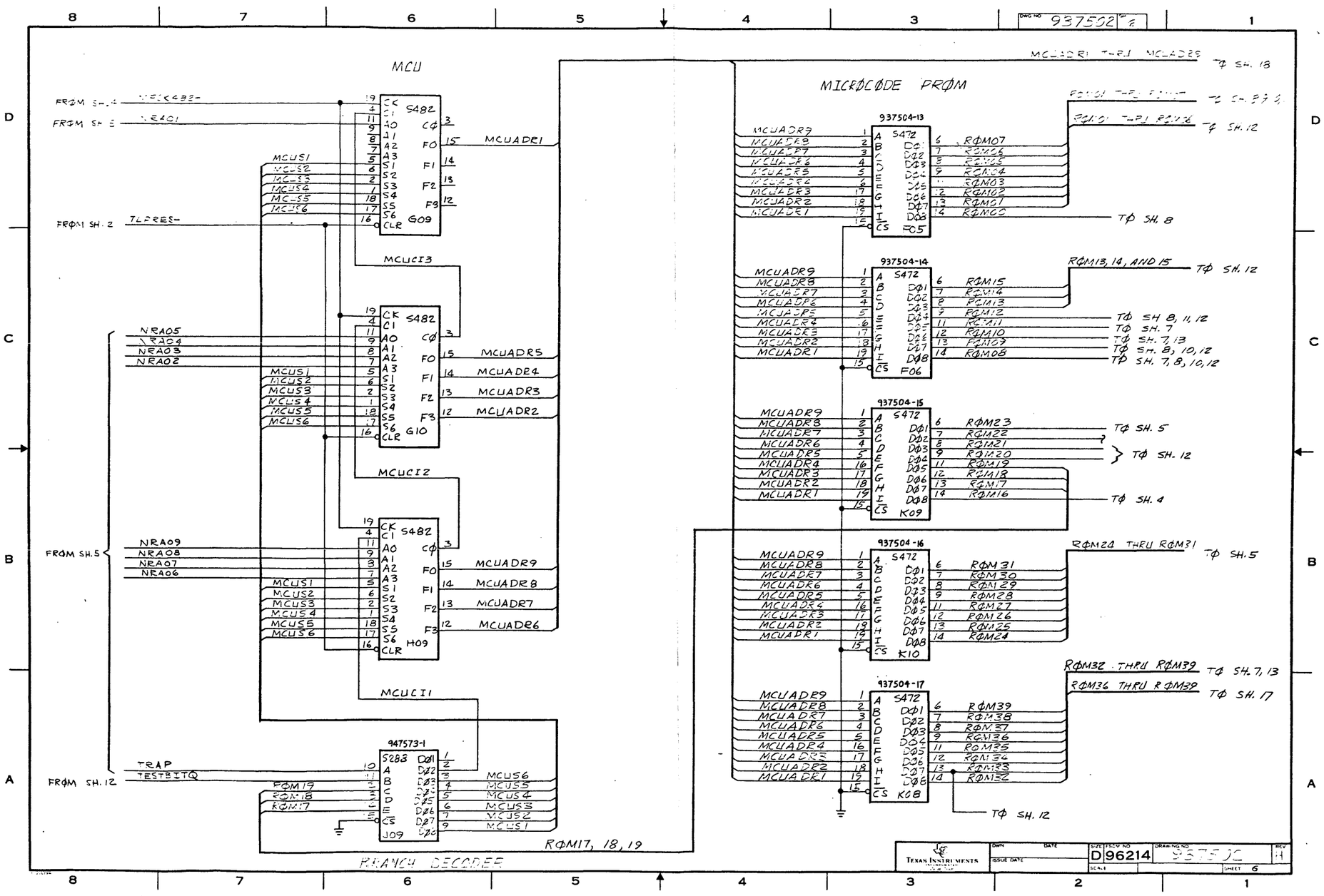
TI-7914 D

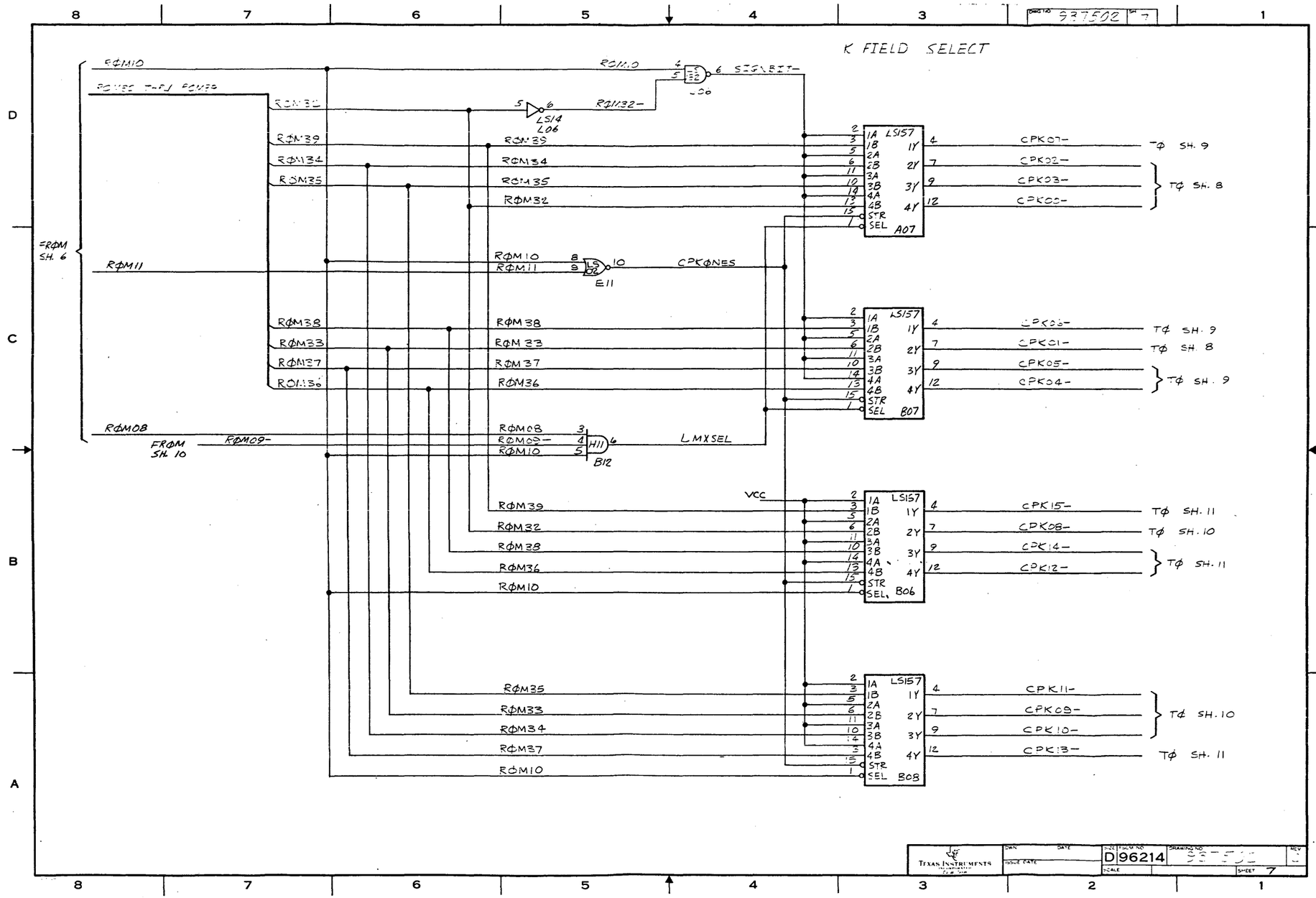

937502 2
TILINE INTERFACE
P1
TLTM-
TLAV
TLAK-
FROM SH. 4
SLTM
MDAC
FROM SH. 3
MDAK
FROM SH. 12
R0M33L
FROM SH. 4
SLVA
FROM SH. 3
MDAC-
FROM SH. 4
SLG0DLY
TLREAD
TLI0RES-
TLWAIT-
TLG0-
TLPRES-
SN75138
B09
A08
TLTM
TLAV-
TLAK
MDT0RC
R2 3.0K
C4 .01μF ≈ 10 USEC
VCC
R0M33L
SLVA
MDAC-
ACCESS0K-
SLG0DLY
TLREAD-
TLI0RES
TLWAIT
TLG0
I0RES-
LS14, A10
S32 B11
LS08 C11
H51 H12
LS74 B10
LS265 L07
ACCDATEN
READ-
READ
RST1
RST1-
RST
RST-
TLDATEN-
TO SH. 12
TO SH. 4, 5
TO SH. 12, 19
TO SH. 14
TO SH. 4, 5, 8, 12, 13, 14, 16, 17, 18, 19
TO SH. 3
TO SH. 4
TO SH. 8, 9, 10, 11
TO SH. 3, 5, 6, 13
ACCESS0K-
TLPRES-
G0
TLG0
G0INH
S32 B11
LS279
E12
MDG0
MDAC
MDT0-
FROM SH. 3
G0-
G0
TO SH. 3
MDT0L-
PFWP-
TLAB0RT-
S08 C10
TLAB0RTL
TLAB0RTL-
TO SH. 5
P1
TLMER-
TLMER
LS14, A10
MDTM
R0M33L-
INTRST-
TLERR-
LS32 D11
TLERL-
TEXAS INSTRUMENTS
D96214
937502
K
SHEET 2

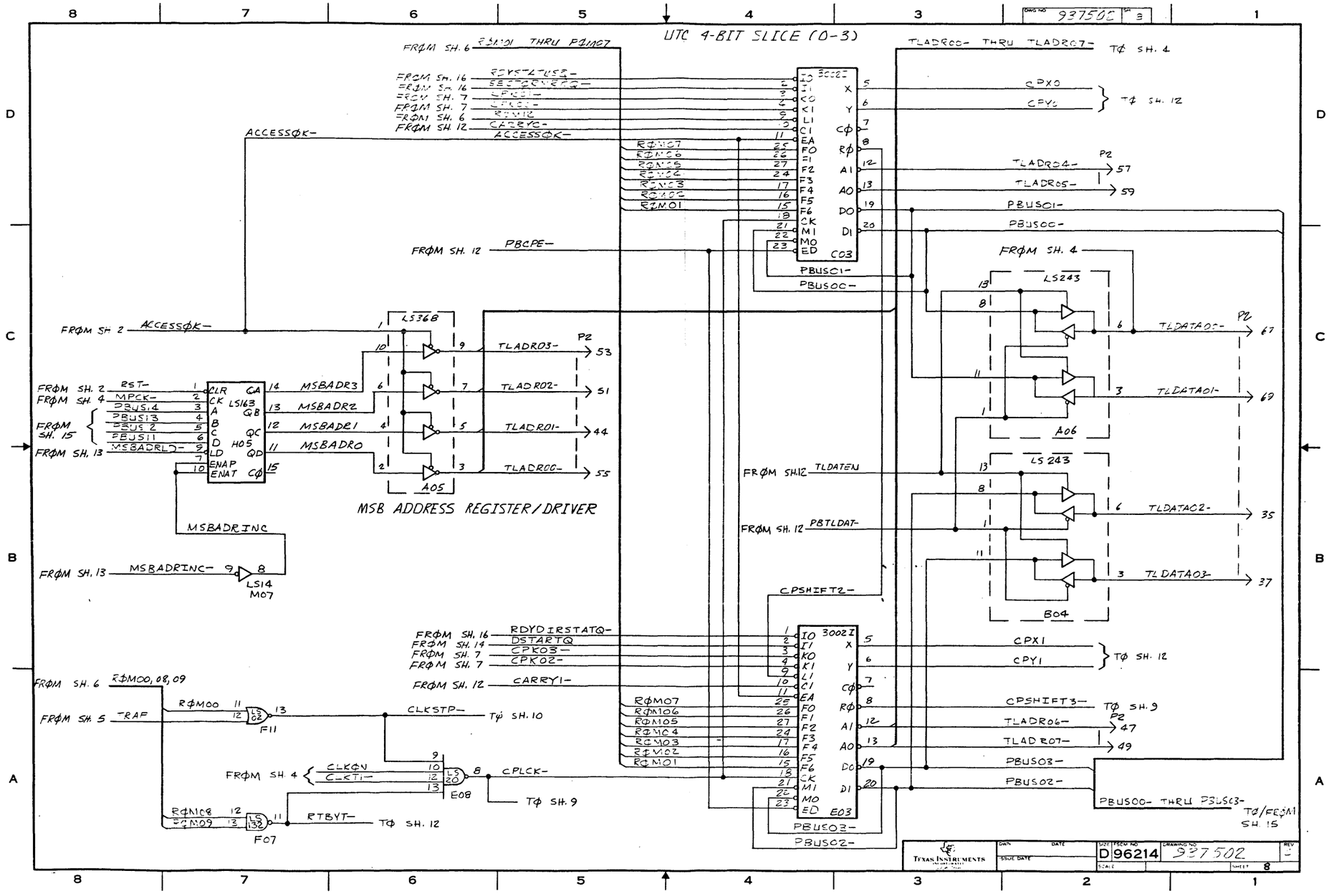

937502 3
TILINE MASTER
MDTM-
MDCMP-
MDTØRC
MDTØ-
TLAV-
TLPFWP-
TLPFWPA-
MDACRST
GØ
CPUID
TLWAIT
ACCESSØK
TLTM
MDTM
MDAK-
TLPRES-
MDAC-
TLAK
MDARRC
MDAR
MDAREN-
MDARØK-
MDAKCK
MDAKCLR-
MDACSET-
PFWP-
MDAC
MDACCK
MDTMEN
MSTRD-
MSTWRT-
MSTSTB
TLAGIN
TLAGØUT
MDGØ-
MDGØ
FROM SH. 2
FROM SH. 13
TØ SH. 18
TØ SH. 2
TØ SH. 15
TØ SH. 4,12
P1
P2
LS14 F12
H11 B12
LS157 A11
H74 D12
LS74 G11
LS74 B10
TILINE MASTER
D96214
937502
K

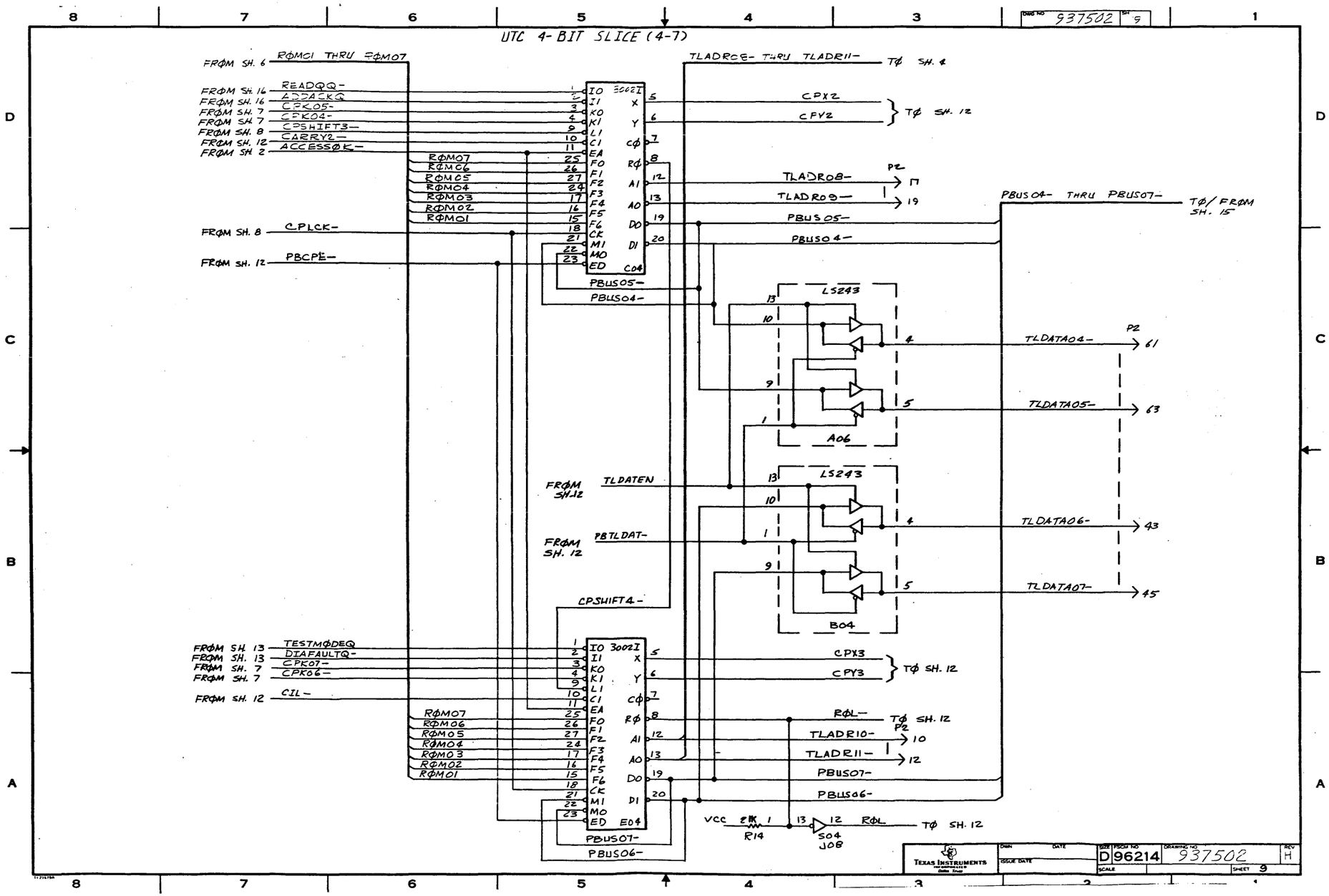

TILINE SLAVE
FROM SH. 8 TLADR00- THRU TLADR07-
FROM SH. 9 TLADR08- THRU TLADR11-
FROM SH. 10 TLADR12- THRU TLADR15-
TLADR00-
TLADR01-
TLADR02-
TLADR03-
TLADR04-
TLADR05-
TLADR06-
TLADR07-
TLADR08-
TLADR09-
TLADR10-
TLADR11-
TLADR12-
TLADR13-
TLADR14-
TLADR15-
TLADR16-
DM8136
A04
A02
A03
B02
SLSW13-
SLSW14-
SLSW15-
SLSW16-
FROM SH. 11
SLADØK
VCC
R59 1K
R12 1K
R20 1K
R19 1K
R13 1K
FROM SH. 2
TLGØ
SLGØRC
SLGØDLY-
SLGØDLY
TØ SH. 2
C07 510pF
E38 442
F07
S04 J08
FROM SH. 6
RØM16
LS74 M09
SLXFR
SLXFR-
M11
SLVAD-
SLVA-
TØ SH. 5
SLVA
TØ SH. 2,5
LS74 G11
FROM SH. 2
RST-
SLVB-
TØ SH. 5
LS74 L12
SLUB
FROM SH. 13
BUSYQ-
SLTMB-
D10
FROM SH. 2
READ-
SLBUSY-
FROM SH. 13
SLVTRM-
3SLTMA-4
K12
STTMD-9
8SLTM
C12
TLDATA00-
TØ SH. 8
LS368 A05
SLTMA-
SLTM
TØ SH. 2
CLKØFF
TØ SH. 5
FROM SH. 3
FROM SH. 13
MDACT-
CLKSTPMST-
CLKINH
F11
CLKEN
CLKSTRT-
J12
F08
CLKØN
CLKTI-
CLKTI
TØ SH. 8,10,12,13
MPCK-
TØ SH. 5, 8, 12, 16, 18
MPCK
TØ SH. 12, 13
MPCK482-
TØ SH. 6
CLKØN
TØ SH. 8, 10
VCC 2402 1 R04
CLKT3-
T ≈80 NS
CLK3RC
CLKØFF
CLKT3-
CLKLED-
CLEDR 1280 2 R23
CR02
VCC 2294 1 R01
CLKØN
≈80
¬CLKIRC
C01 2-510pF
VCC 2383 1 R03
CLK2RC
C02 220pF
CLKRUN
VCC 1.1K 2 R17
CLKT2-
TØ SH. 18
CONTROLLER CLOCK
TEXAS INSTRUMENTS
D96214
937502
SHEET 4

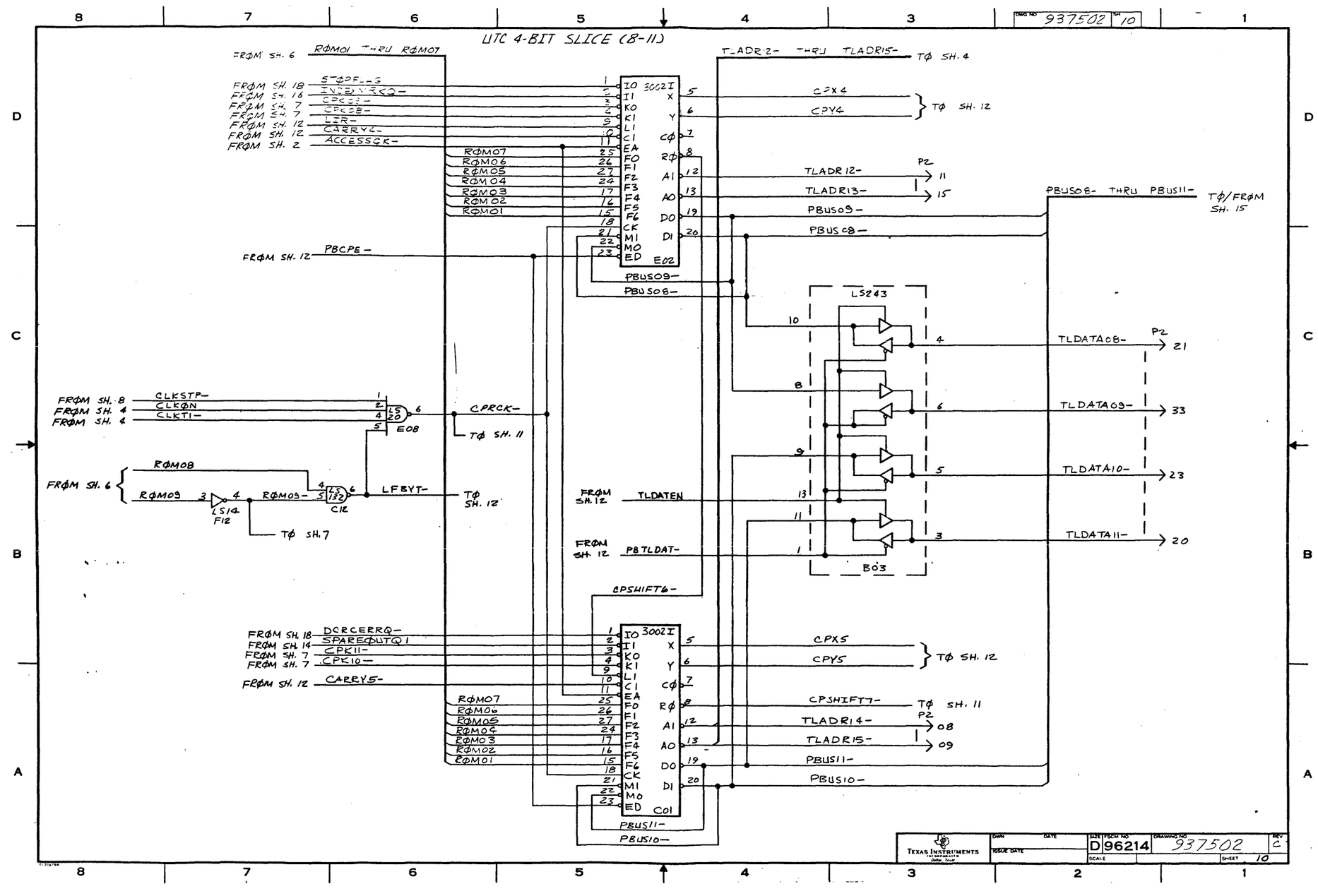

8
7
6
5
4
3
2
1
D
C
B
A
DWG NO 937502 SH 5
FROM SH. 5
FROM SH. 3
RST-
CMDTMRCLR
15.0K 1%
R06
15.0K 1%
R10
CMDT
CMDD
C06
.1µF
≈ 5 MSEC
CMDTMRCLK-
CMDTMRCLK
LS132, J06
J07
CMDTMRD_Y-
CMDTMRD_Y-
TO SH. 3
COMMAND TIMER
(200 MSEC)
FROM SH. 14
FROM SH. 13
TIMERRQ
DSRVCRTQ
LS32
N08
WRTTIMERR-
INTB
INTB-
LS14
F12
INTTRAP
M12
FROM SH. 4
CLKOFF
LS32
J12
INTRST-
TO SH. 2, 13, 14
FROM SH. 2
MDTQ-
TLEFRQ-
TLABRTQ-
CLRWRTQ-
MDTRQ-
TLEFRQ-
TLABRTQ-
CLRWRTQ-
IR-3
FROM SH. 4
FROM SH. 2
MPCK-
TLPRES-
LS174
F09
INTA
INTA
INTA
LS04
J08
SLVB-
FROM SH. 4
SLVA
LS51
H12
TRAP-
LS04
J08
TRAP
TO SH. 6, 8
TRAP-
TO SH. 13
VCC
LS148
F10
EO
GS
A0
A1
A2
INTA-
TO SH. 18
INTADZ
INTADI
INTADO
FROM SH. 6
ROM23
LS08
L09
NRA01
ROM26
ROM25
ROM27
ROM24
LS157
H10
NRA04
NRA03
NRA05
NRA02
TO SH. 6
FROM SH. 4
SLVA-
SLVB-
LS132
J12
SLVACT
SLVA-
SLVB-
SLVB-
TLADR18-
TLADR19-
TLADR17-
FROM SH. 11
LS14
B01
TLADR18
TLADR19
TLADR17
FROM SH. 2
READ-
ROM30
ROM28
ROM31
ROM29
LS157
J10
NRA08
NRA06
NRA09
NRA07
FROM SH. 6
ROM24 THRU ROM31
INTERNAL INTERRUPTS AND ADDRESS SELECTORE
TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
SCALE
SIZE D
FSCM NO 96214
DRAWING NO 937502
SHEET 5
REV H

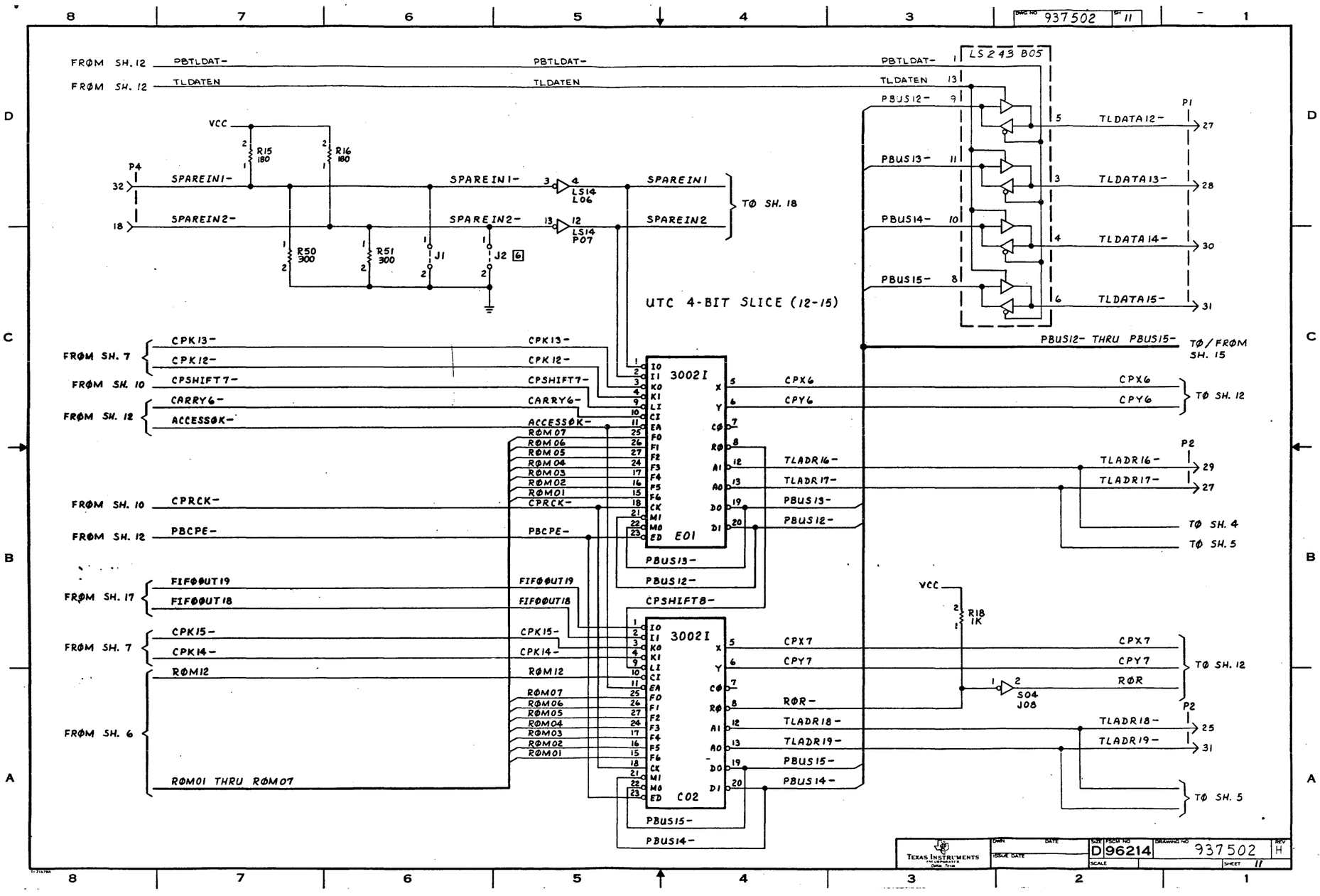

MCU
MICRØCØDE PRØM
BRANCH DECODER
FROM SH. 4
FROM SH. 5
FROM SH. 2
FROM SH. 12
MCUCI3
MCUCI2
MCUCI1
MCUCI0
MCUADR9
MCUADR8
MCUADR7
MCUADR6
MCUADR5
MCUADR4
MCUADR3
MCUADR2
MCUADR1
MCUS1
MCUS2
MCUS3
MCUS4
MCUS5
MCUS6
NRA05
NRA04
NRA03
NRA02
NRA09
NRA08
NRA07
NRA06
TRAP
TESTBITQ
RØM19
RØM18
RØM17
RØM17, 18, 19
TØ SH. 18
TØ SH. 8
TØ SH. 12
TØ SH. 7
TØ SH. 7, 13
TØ SH. 8, 10, 12
TØ SH. 7, 8, 10, 12
TØ SH. 5
TØ SH. 4
TØ SH. 17
RØM13, 14, AND 15
RØM28 THRU RØM31
RØM32 THRU RØM39
RØM36 THRU RØM39
937504-13
937504-14
937504-15
937504-16
937504-17
947573-1
TEXAS INSTRUMENTS
D 96214

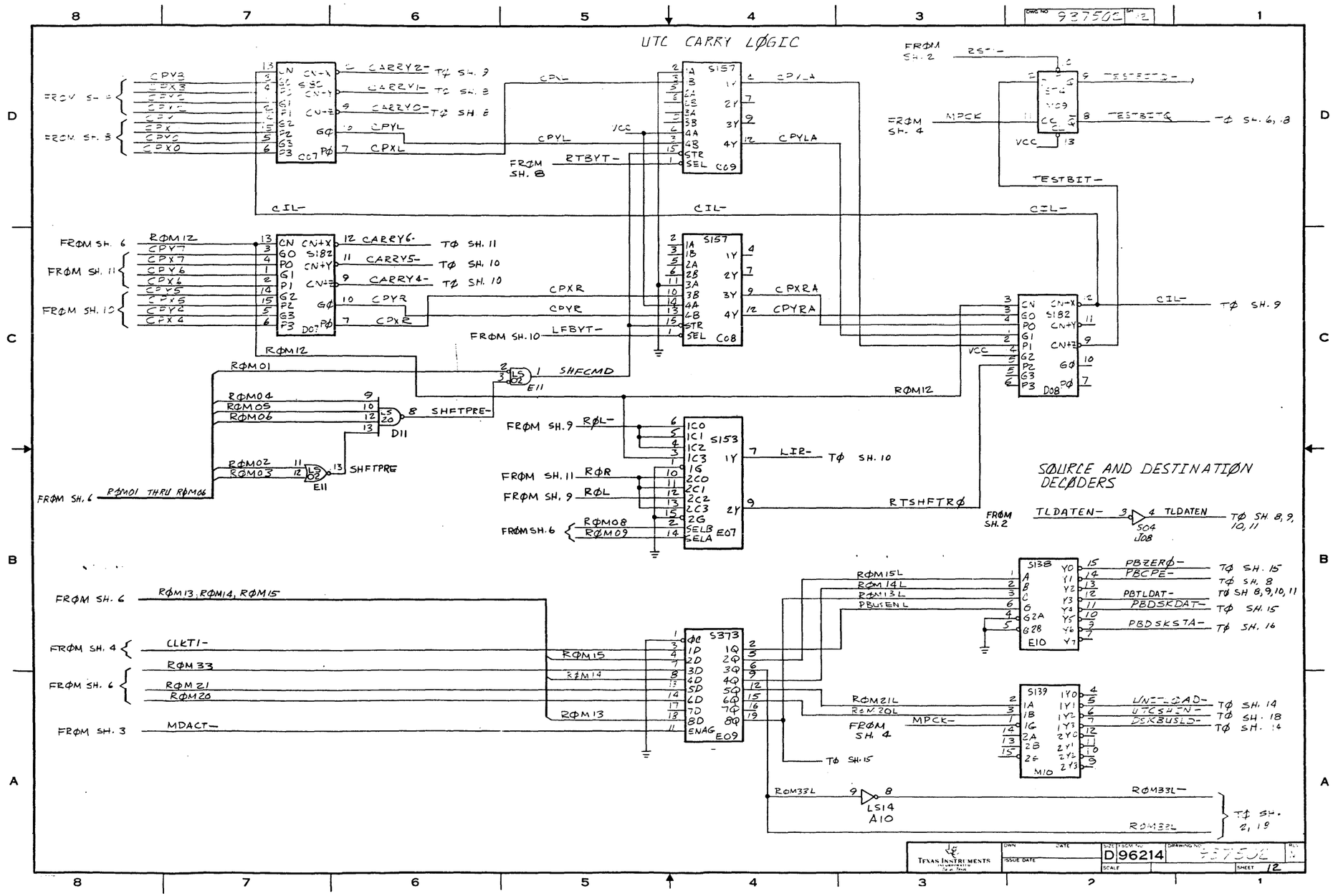

K FIELD SELECT
DWG NO 937502 SH 7
RØM10
RØM11.0
SIG\BIT-
POWER T-FJ POWER
RØM32
LS14 L06
RØM11.32-
RØM39
RØM34
RØM35
RØM32
FROM SH. 6
RØM11
RØM10
RØM11
CPKØNES
E11
RØM38
RØM33
RØM37
RØM36
RØM08
FROM SH. 10
RØM09-
RØM08
RØM09-
RØM10
H11
LMXSEL
B12
VCC
RØM39
RØM32
RØM38
RØM36
RØM10
RØM35
RØM33
RØM34
RØM37
RØM10
LS157
A07
B07
B06
B08
CPK07-
CPK02-
CPK03-
CPK00-
CPK06-
CPK01-
CPK05-
CPK04-
CPK15-
CPK08-
CPK14-
CPK12-
CPK11-
CPK09-
CPK10-
CPK13-
TØ SH. 9
TØ SH. 8
TØ SH. 11
TØ SH. 10
TEXAS INSTRUMENTS
D96214
SHEET 7

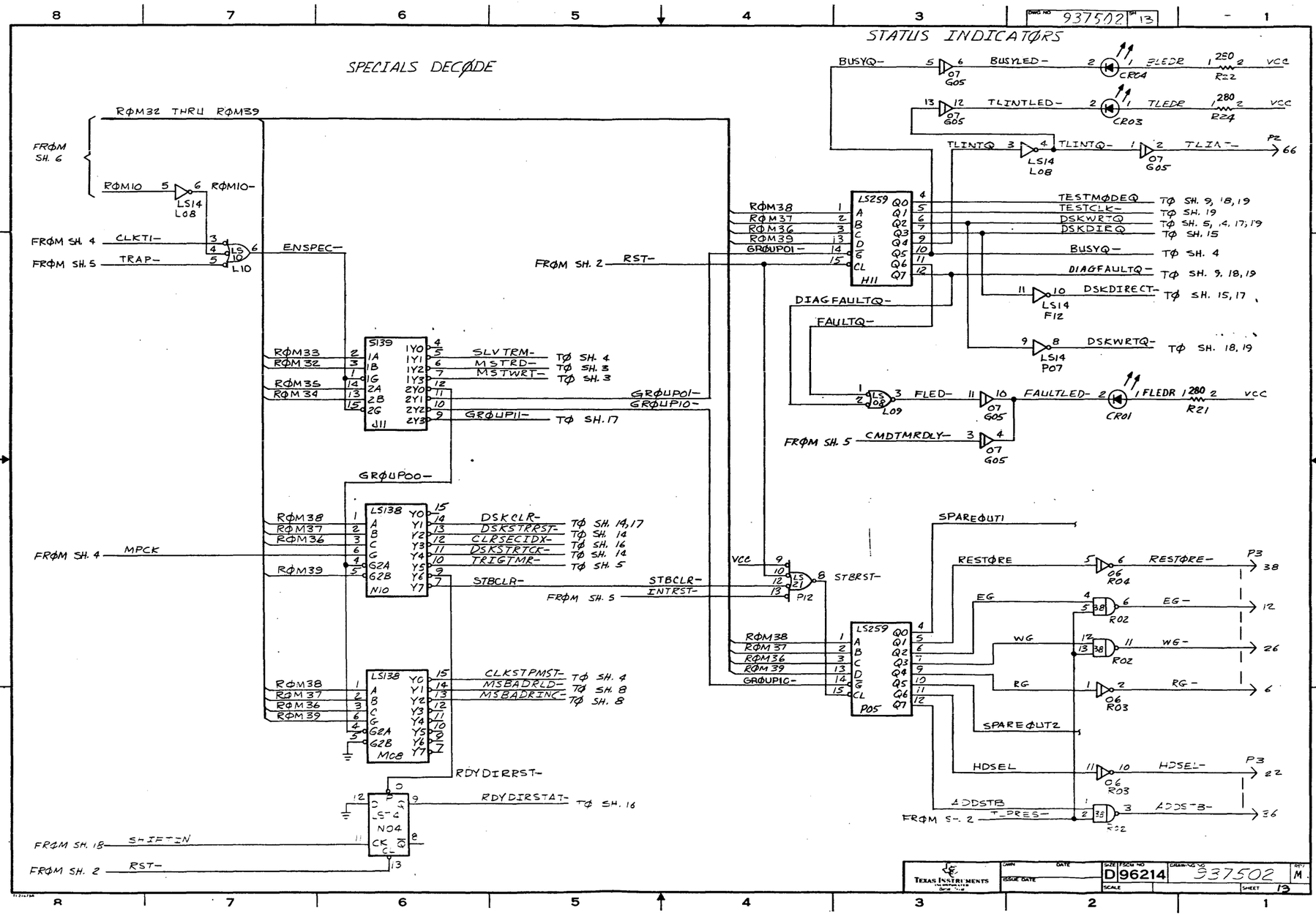

UTC 4-BIT SLICE (0-3)
MSB ADDRESS REGISTER/DRIVER
TLADR00- THRU TLADR07-
TLDATA00-
TLDATA01-
TLDATA02-
TLDATA03-
PBUS00- THRU PBUS03-
MSBADRINC
ACCESSØK-
PBCPE-
CLKSTP-
RTBYT-
CPSHIFT2-
CPSHIFT3-
TLDATEN
PBTLDAT-
CARRY1-
LS368
LS163
LS243
LS14
LS02
LS32
3002
A05
A06
B04
E08
F11
F07
E03
TLADR00- 55
TLADR01- 44
TLADR02- 51
TLADR03- 53
TLADR04- 57
TLADR05- 59
TLADR06- 47
TLADR07- 49
TLDATA00- 67
TLDATA01- 69
TLDATA02- 35
TLDATA03- 37
TØ SH. 12
TØ SH. 9
TØ SH. 10
TØ/FROM SH. 15
D96214
937502

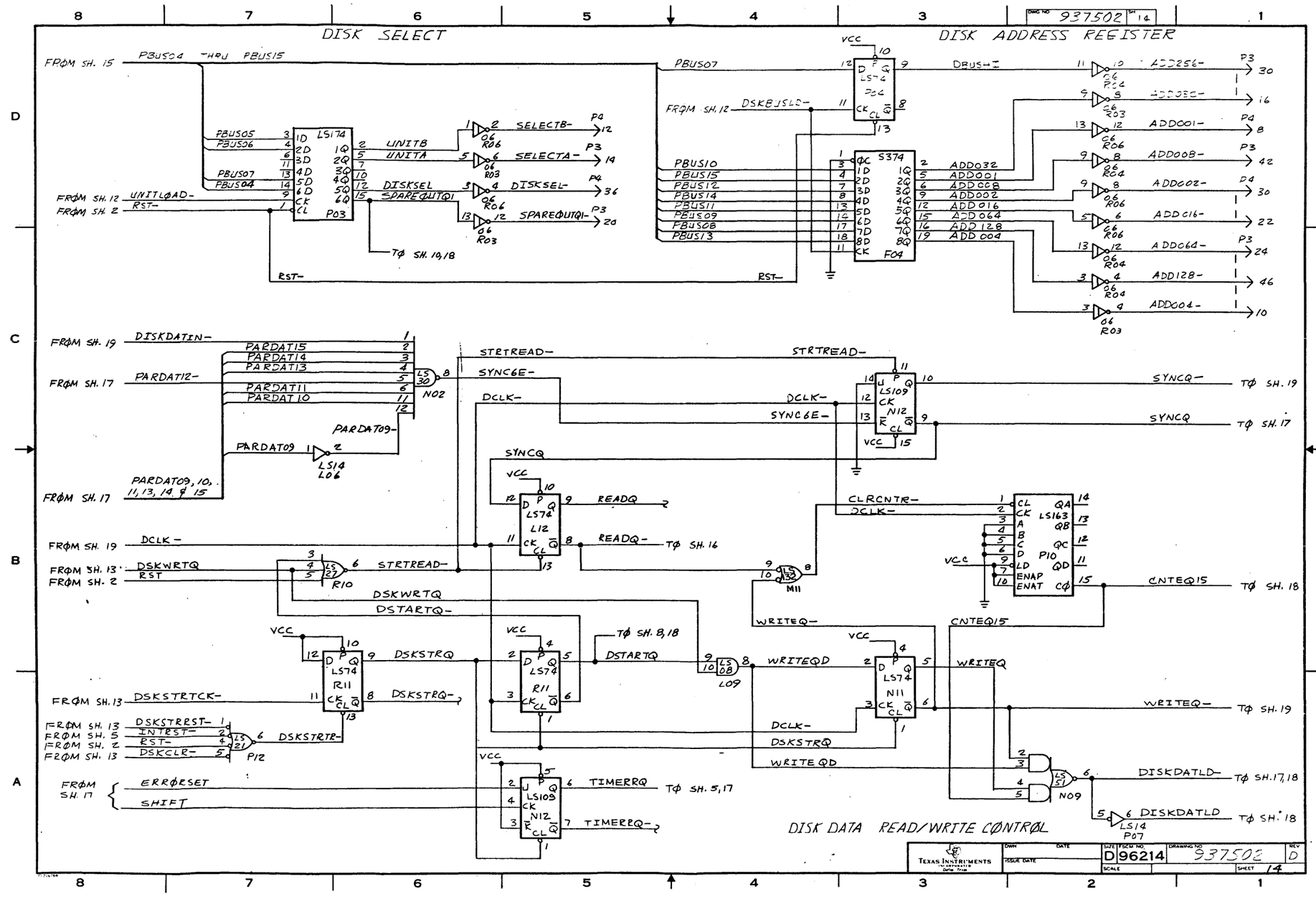

UTC 4-BIT SLICE (4-7)
Dwg NO 937502 SH 9
FRØM SH. 6 RØM01 THRU RØM07
FRØM SH. 16 READQQ-
FRØM SH. 16 ADDACKQ
FRØM SH. 7 CPK05-
FRØM SH. 7 CPK04-
FRØM SH. 8 CPSHIFT3-
FRØM SH. 12 CARRY2-
FRØM SH. 2 ACCESSØK-
FRØM SH. 8 CPLCK-
FRØM SH. 12 PBCPE-
RØM07
RØM06
RØM05
RØM04
RØM03
RØM02
RØM01
3002I
IO I1 KO K1 L1 C1 EA F0 F1 F2 F3 F4 F5 F6 CK M1 MO ED
X Y CØ RØ A1 A0 DO DI C04
TLADR08- THRU TLADR11- TØ SH. 8
CPX2
CPY2
TØ SH. 12
TLADR08- P2 17
TLADR09- 19
PBUS04- THRU PBUS07- TØ/FRØM SH. 15
PBUS05-
PBUS04-
LS243
A06
B04
TLDATA04- P2 61
TLDATA05- 63
TLDATA06- 43
TLDATA07- 45
FRØM SH.12 TLDATEN
FRØM SH. 12 PBTLDAT-
CPSHIFT4-
FRØM SH. 13 TESTMØDEQ
FRØM SH. 13 DIAFAULTQ-
FRØM SH. 7 CPK07-
FRØM SH. 7 CPK06-
FRØM SH. 12 CIL-
CPX3
CPY3
TØ SH. 12
RØL- TØ SH. 12
TLADR10- P2 10
TLADR11- 12
PBUS07-
PBUS06-
VCC 8K R14
S04 J08
RØL TØ SH. 12
PBUS07-
PBUS06-
TEXAS INSTRUMENTS
DWN DATE
ISSUE DATE
SIZE D FSCM NO 96214
DRAWING NO 937502
REV H
SCALE
SHEET 9

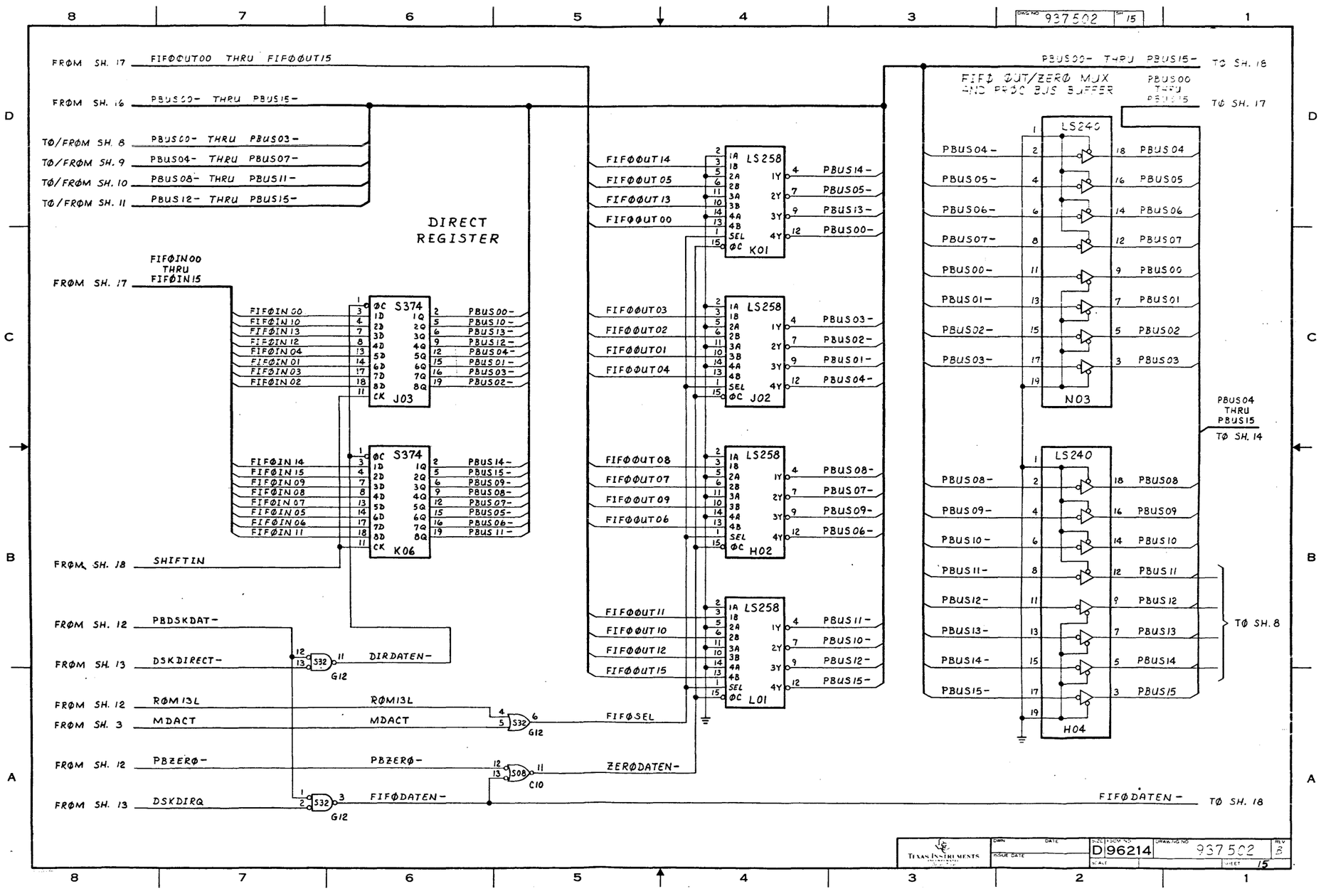

UTC 4-BIT SLICE (8-11)
DWG NO 937502 SH 10
FRØM SH. 6 RØM01 THRU RØM07
TLADR12- THRU TLADR15-
TØ SH. 4
FRØM SH. 18 STØPENB
FRØM SH. 18 ENDWRSQ-
FRØM SH. 7 CPCEB-
FRØM SH. 7 CPCEB-
FRØM SH. 12 LIR-
FRØM SH. 12 CARRY2-
FRØM SH. 2 ACCESSQR-
3002I
CPX4
CPY4
TØ SH. 12
TLADR12-
TLADR13-
P2
11
15
PBUS08- THRU PBUS11-
TØ/FRØM SH. 15
PBUS09-
PBUS08-
PBCPE-
FRØM SH. 12
E02
LS243
TLDATA08-
TLDATA09-
TLDATA10-
TLDATA11-
21
33
23
20
B03
FRØM SH. 8 CLKSTP-
FRØM SH. 4 CLKØN
FRØM SH. 4 CLKTI-
E08
CPRCK-
TØ SH. 11
RØM08
FRØM SH. 6
RØM09
LS14 F12
RØM09-
LS132 C12
LFBYT-
TØ SH. 12
TØ SH. 7
FRØM SH. 12 TLDATEN
FRØM SH. 12 PBTLDAT-
CPSHIFT6-
FRØM SH. 18 DCRCERRQ-
FRØM SH. 14 SPAREOUTQ1
FRØM SH. 7 CPK11-
FRØM SH. 7 CPK10-
FRØM SH. 12 CARRY5-
CPX5
CPY5
TØ SH. 12
CPSHIFT7-
TØ SH. 11
TLADR14-
TLADR15-
08
09
PBUS11-
PBUS10-
Co1
TEXAS INSTRUMENTS
DWN DATE
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 937502
REV C
SCALE
SHEET 10


DWG NO 937502 SH 11
FROM SH. 12 PBTLDAT-
PBTLDAT-
PBTLDAT-
FROM SH. 12 TLDATEN
TLDATEN
TLDATEN
LS243 B05
PBUS12-
PBUS13-
PBUS14-
PBUS15-
P1
TLDATA12-
TLDATA13-
TLDATA14-
TLDATA15-
VCC
R15 180
R16 180
P4
SPAREIN1-
SPAREIN2-
LS14 L06
LS14 P07
SPAREIN1
SPAREIN2
TØ SH. 18
R50 300
R51 300
J1
J2 6
UTC 4-BIT SLICE (12-15)
PBUS12- THRU PBUS15-
TØ/FRØM SH. 15
FROM SH. 7 CPK13-
CPK12-
FROM SH. 10 CPSHIFT7-
FROM SH. 12 CARRY6-
ACCESSØK-
3002I
E01
CPX6
CPY6
TØ SH. 12
P2
TLADR16-
TLADR17-
TØ SH. 4
TØ SH. 5
FROM SH. 10 CPRCK-
FROM SH. 12 PBCPE-
RØM07
RØM06
RØM05
RØM04
RØM03
RØM02
RØM01
FROM SH. 17 FIFØØUT19
FIFØØUT18
CPSHIFT8-
FROM SH. 7 CPK15-
CPK14-
FROM SH. 6 RØM12
RØM01 THRU RØM07
C02
CPX7
CPY7
RØR
RØR-
TLADR18-
TLADR19-
R18 1K
S04 J08
TEXAS INSTRUMENTS
DRWN DATE
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 937502
REV H
SCALE
SHEET 11


UTC CARRY LØGIC
SOURCE AND DESTINATION DECØDERS
TESTBIT-
CIL-
VCC
RØM12
SHFCMD
SHFTPRE-
SHFTPRE
LIR-
RTSHFTRØ
TLDATEN-
TLDATEN
PBZERØ-
PBCPE-
PBTLDAT-
PBDSKDAT-
PBDSKSTA-
UNLOAD-
UTCSYN-
DSKBUSLD-
RØM33L-
RØM33L
TEXAS INSTRUMENTS
D96214


SPECIALS DECODE
STATUS INDICATORS
937502
13
RØM32 THRU RØM39
FRØM SH. 6
RØM10
RØM10-
LS14 L08
FRØM SH. 4
CLKT1-
FRØM SH. 5
TRAP-
LS10 L10
ENSPEC-
FRØM SH. 2
RST-
RØM33
RØM32
RØM35
RØM34
S139
SLVTRM-
MSTRD-
MSTWRT-
TØ SH. 4
TØ SH. 3
TØ SH. 3
GRØUP01-
GRØUP10-
GRØUP11-
TØ SH. 17
GRØUP00-
RØM38
RØM37
RØM36
RØM39
LS138
DSKCLR-
DSKSTRRST-
CLRSECIDX-
DSKSTRTCK-
TRIGTMR-
TØ SH. 14,17
TØ SH. 14
TØ SH. 16
TØ SH. 14
TØ SH. 5
FRØM SH. 4
MPCK
STBCLR-
FRØM SH. 5
CLKSTPMST-
MSBADRLD-
MSBADRINC-
TØ SH. 4
TØ SH. 8
TØ SH. 8
M08
RDYDIRRST-
RDYDIRSTAT-
TØ SH. 16
N04
FRØM SH. 18
SHIFTIN
FRØM SH. 2
RST-
BUSYQ-
BUSYLED-
CR04
SLEDR
R22
TLINTLED-
CR03
TLEDR
R24
VCC
TLINTQ
TLINTQ-
TLIA-
P2
66
LS14 L08
LS14 G05
RØM38
RØM37
RØM36
RØM39
GRØUP01-
LS259
H11
TESTMØDEQ
TESTCLK-
DSKWRTQ
DSKDIRQ
BUSYQ-
DIAGFAULTQ-
DSKDIRECT-
DSKWRTQ-
TØ SH. 9, 18, 19
TØ SH. 19
TØ SH. 5, 14, 17, 19
TØ SH. 15
TØ SH. 4
TØ SH. 9, 18, 19
TØ SH. 15, 17
TØ SH. 18, 19
LS14 F12
LS14 P07
DIAGFAULTQ-
FAULTQ-
FLED-
FAULTLED-
FLEDR
CR01
R21
LS08 L09
FRØM SH. 5
CMDTMRDLY-
SPAREØUT1
RESTØRE
RESTØRE-
EG
EG-
WG
WG-
RG
RG-
SPAREØUT2
HDSEL
HDSEL-
ADDSTB
ADDS-B-
T_PRES-
FRØM SH. 2
R04
R02
R03
P05
P12
STBRST-
INTRST-
TEXAS INSTRUMENTS
D
96214
937502
M
SHEET 13


DISK SELECT
DISK ADDRESS REGISTER
DWG NO 937502 SH 14
FROM SH. 15 PBUS04 THRU PBUS15
PBUS05
PBUS06
PBUS07
PBUS04
FROM SH. 12 UNITLOAD-
FROM SH. 2 RST-
LS174
P03
UNITB
UNITA
DISKSEL
SPAREOUTQ1
SELECTB-
SELECTA-
DISKSEL-
SPAREOUTQ1-
TO SH. 10,18
RST-
PBUS07
FROM SH. 12 DSKBUSLD-
PBUS10
PBUS15
PBUS12
PBUS14
PBUS11
PBUS09
PBUS08
PBUS13
S374
F04
DBUS-I
ADD256-
ADD128-
ADD064-
ADD032
ADD001
ADD008
ADD002
ADD016
ADD064
ADD128
ADD004
ADD256-
ADD032-
ADD001-
ADD008-
ADD002-
ADD016-
ADD064-
ADD128-
ADD004-
FROM SH. 19 DISKDATIN-
FROM SH. 17 PARDAT12-
PARDAT15
PARDAT14
PARDAT13
PARDAT11
PARDAT10
LS30
N02
PARDAT09-
PARDAT09
LS14
L06
FROM SH. 17 PARDAT09, 10, 11, 13, 14 & 15
STRTREAD-
SYNC6E-
DCLK-
SYNCQ
VCC
L12
LS74
READQ
READQ-
TO SH. 16
FROM SH. 19 DCLK-
FROM SH. 13 DSKWRTQ
FROM SH. 2 RST
R10
STRTREAD-
DSKWRTQ
DSTARTQ-
VCC
R11
DSKSTRQ
DSKSTRQ-
FROM SH. 13 DSKSTRTCK-
FROM SH. 13 DSKSTRREST-
FROM SH. 5 INTRST-
FROM SH. 2 RST-
FROM SH. 13 DSKCLR-
P12
DSKSTRTR-
FROM SH. FROM SH. 17 ERRORESET SHIFT
LS109
N12
TIMERRQ
TIMERRQ-
TO SH. 5,17
TO SH. 8,18
DSTARTQ
LS08
L09
WRITEQD
M11
CLRCNTR-
DCLK-
LS163
P10
CNTEQ15
TO SH. 18
WRITEQ
N11
WRITEQ-
TO SH. 19
DISKDATLD-
TO SH. 17,18
DISKDATLD
TO SH. 18
P07
DISK DATA READ/WRITE CONTROL
TEXAS INSTRUMENTS
SIZE D
FSCM NO. 96214
DRAWING NO. 937502
REV D
SHEET 14


DWG NO 937502 SH 15
FROM SH. 17 FIFØOUT00 THRU FIFØOUT15
FROM SH. 16 PBUS00- THRU PBUS15-
TØ/FROM SH. 8 PBUS00- THRU PBUS03-
TØ/FROM SH. 9 PBUS04- THRU PBUS07-
TØ/FROM SH. 10 PBUS08- THRU PBUS11-
TØ/FROM SH. 11 PBUS12- THRU PBUS15-
DIRECT REGISTER
FIFØIN00 THRU FIFØIN15
FROM SH. 17
FIFØIN00 FIFØIN10 FIFØIN13 FIFØIN12 FIFØIN04 FIFØIN01 FIFØIN03 FIFØIN02
ØC S374 1D 2D 3D 4D 5D 6D 7D 8D CK 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
PBUS00- PBUS10- PBUS13- PBUS12- PBUS04- PBUS01- PBUS03- PBUS02-
J03
FIFØIN14 FIFØIN15 FIFØIN09 FIFØIN08 FIFØIN07 FIFØIN05 FIFØIN06 FIFØIN11
PBUS14- PBUS15- PBUS09- PBUS08- PBUS07- PBUS05- PBUS06- PBUS11-
K06
FROM SH. 18 SHIFTIN
FROM SH. 12 PBDSKDAT-
FROM SH. 13 DSKDIRECT-
S32 G12
DIRDATEN-
FROM SH. 12 RØM13L
FROM SH. 3 MDACT
FIFØSEL
FROM SH. 12 PBZERØ-
S08 C10
ZERØDATEN-
FROM SH. 13 DSKDIRQ
FIFØDATEN-
FIFØOUT14 FIFØOUT05 FIFØOUT13 FIFØOUT00
LS258 1A 1B 2A 2B 3A 3B 4A 4B SEL ØC
1Y 2Y 3Y 4Y
PBUS14- PBUS05- PBUS13- PBUS00-
K01
FIFØOUT03 FIFØOUT02 FIFØOUT01 FIFØOUT04
PBUS03- PBUS02- PBUS01- PBUS04-
J02
FIFØOUT08 FIFØOUT07 FIFØOUT09 FIFØOUT06
PBUS08- PBUS07- PBUS09- PBUS06-
H02
FIFØOUT11 FIFØOUT10 FIFØOUT12 FIFØOUT15
PBUS11- PBUS10- PBUS12- PBUS15-
L01
PBUS00- THRU PBUS15- TØ SH. 18
FIFØ OUT/ZERØ MUX AND PROC BUS BUFFER
PBUS00 THRU PBUS15
TØ SH. 17
LS240
PBUS04- PBUS05- PBUS06- PBUS07- PBUS00- PBUS01- PBUS02- PBUS03-
PBUS04 PBUS05 PBUS06 PBUS07 PBUS00 PBUS01 PBUS02 PBUS03
N03
PBUS04 THRU PBUS15
TØ SH. 14
PBUS08- PBUS09- PBUS10- PBUS11- PBUS12- PBUS13- PBUS14- PBUS15-
PBUS08 PBUS09 PBUS10 PBUS11 PBUS12 PBUS13 PBUS14 PBUS15
H04
TØ SH. 8
FIFØDATEN- TØ SH. 18
TEXAS INSTRUMENTS
DWN DATE ISSUE DATE
SIZE D 96214 DRAWING NO 937502 REV B
SCALE SHEET 15

DISK INTERFACE RECEIVERS

DWG NO 937502 SH 16

PBUS00- THRU PBUS15- TØ SH. 15, 18

FRØM SH. 12 PBDSKSTA-

FILERDY- SPAREIN3- RDYSRW- SPAREIN5- WP- WCHK- SPAREIN6- SKIC-

ØFFLINE- NØTRDY-

PBUS00- PBUS06- PBUS01- PBUS07- PBUS02- PBUS03- PBUS04- PBUS05-

PBDSKSTA- SECTØRB03- SECTØRB04- SECTØRB02- SECTØRB01- SWBIN- SWAIN- SPAREIN4- SECTØRB16-

PBUS12- PBUS13- PBUS14- PBUS15- PBUS08- PBUS09- PBUS10- PBUS11-

I-BUS LATCH

FRØM SH. 13 RDYDIRSTAT-
FRØM SH. 14 READQ-
FRØM SH. 17 RDYSTATUS-
FRØM SH. 4 MPCK-
FRØM SH. 2 RST-

RDYDIRSTATQ- ADDACKQ READQQ- INDEXMRKQ- SECTØRMRKQ- RDYSTATUSQ-

TØ SH. 8,18 TØ SH. 9,18 TØ SH. 9,18 TØ SH. 10,18 TØ SH. 8,10 TØ SH. 8,10

INDMRK- ADDACK- SECMRK-

INDMRK ADDACK SECMRK

INDEXMRK- ADDACK SECTØRMRK-

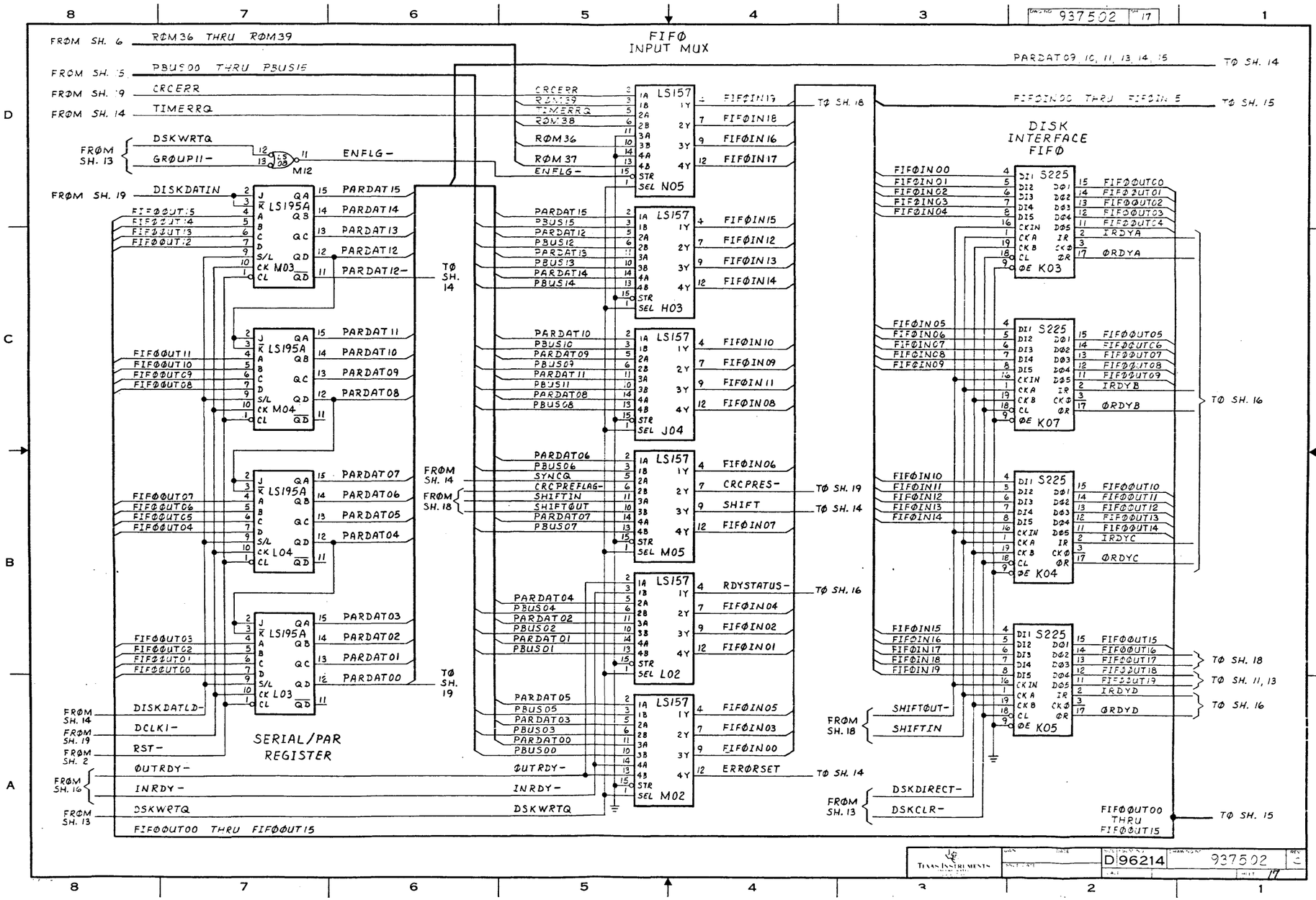
FRØM SH. 13 CLRSECIDX-

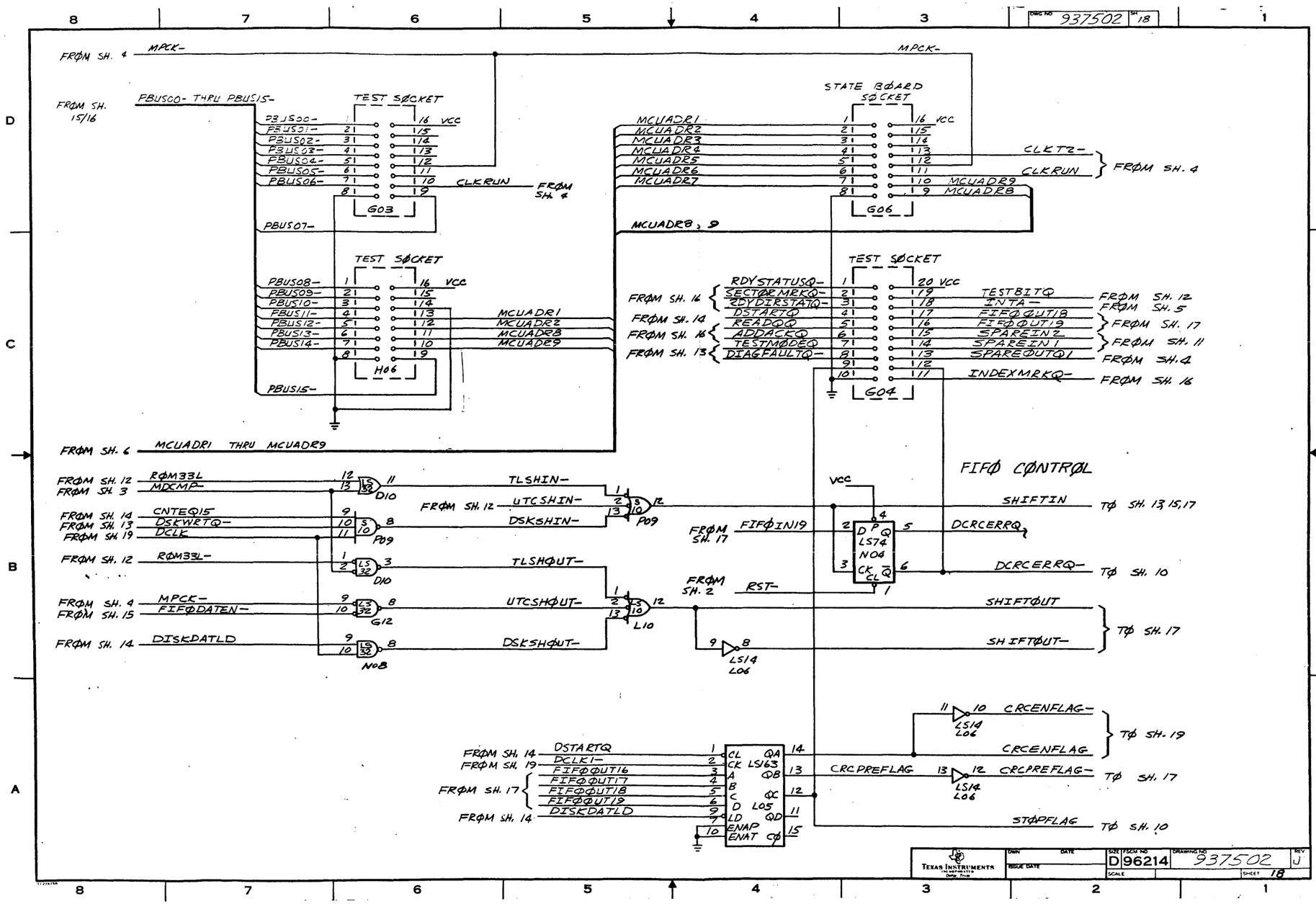
IRDYA IRDYB IRDYC IRDYD ØRDYA ØRDYB ØRDYC ØRDYD

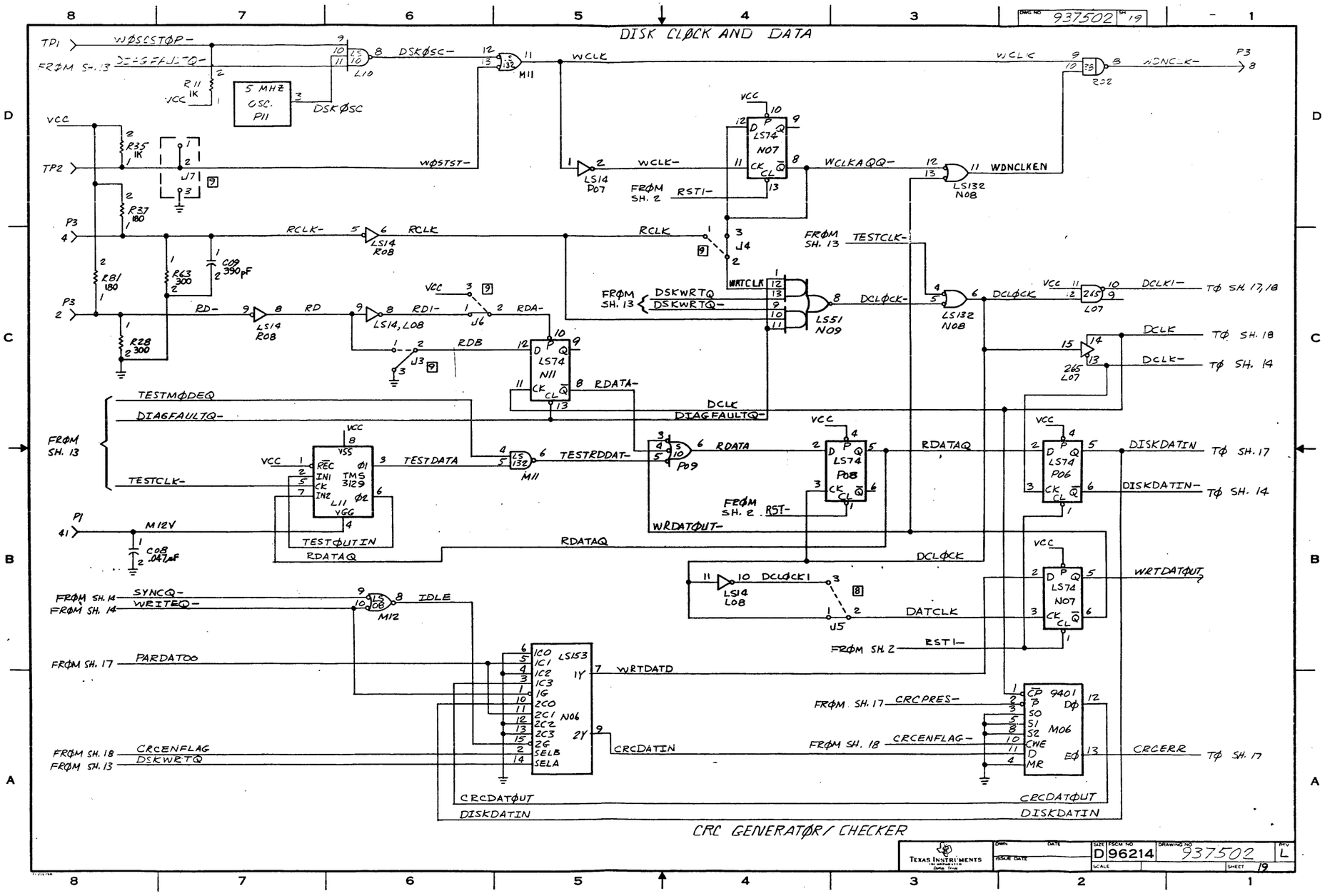
INRDY- ØUTRDY-

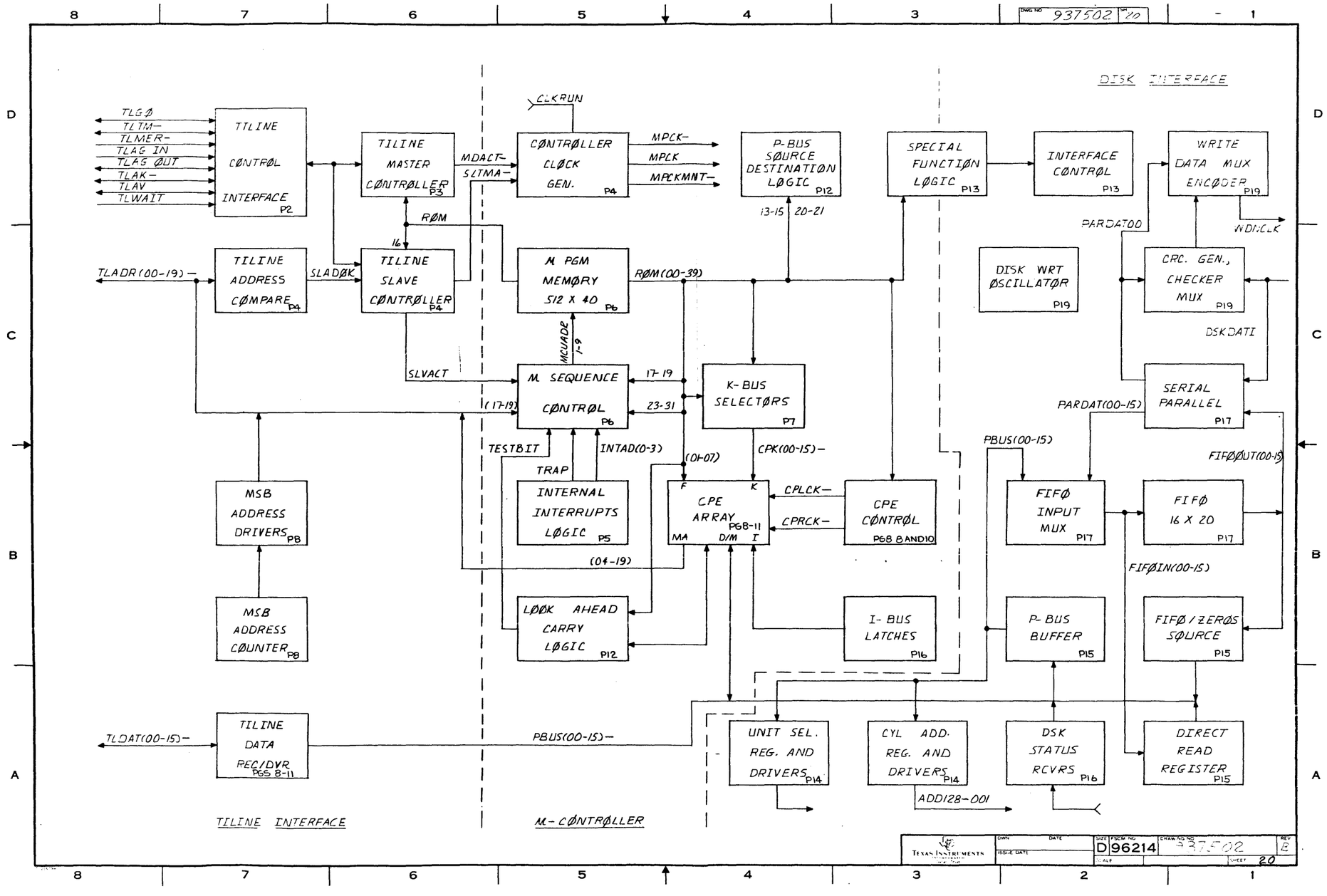
TØ SH. 17

TEXAS INSTRUMENTS	DWN / DATE	CAGE / FSCM NO D96214	DRAWING NO 937502 REV H
	ISSUE DATE	SCALE	SHEET 16


FIFØ INPUT MUX
DISK INTERFACE FIFØ
SERIAL/PAR REGISTER
FROM SH. 6 RØM36 THRU RØM39
FROM SH. 5 PBUS00 THRU PBUS15
FROM SH. 9 CRCERR
FROM SH. 14 TIMERRQ
FROM SH. 13 DSKWRTQ GROUP11-
ENFLG-
FROM SH. 19 DISKDATIN
PARDAT15 PARDAT14 PARDAT13 PARDAT12 PARDAT12-
PARDAT11 PARDAT10 PARDAT09 PARDAT08
PARDAT07 PARDAT06 PARDAT05 PARDAT04
PARDAT03 PARDAT02 PARDAT01 PARDAT00
TØ SH. 14
TØ SH. 19
FIFØOUT:5 FIFØOUT:4 FIFØOUT:3 FIFØOUT:2
FIFØOUT11 FIFØOUT10 FIFØOUT09 FIFØOUT08
FIFØOUT07 FIFØOUT06 FIFØOUT05 FIFØOUT04
FIFØOUT03 FIFØOUT02 FIFØOUT01 FIFØOUT00
M03 M04 L04 L03
FROM SH. 14 DISKDATLD-
FROM SH. 19 DCLKI-
FROM SH. 2 RST-
FROM SH. 16 ØUTRDY- INRDY-
FROM SH. 13 DSKWRTQ
FIFØOUT00 THRU FIFØOUT15
CRCERR RØM39 TIMERRQ RØM38 RØM36 RØM37 ENFLG-
PARDAT15 PBUS15 PARDAT12 PBUS12 PARDAT13 PBUS13 PARDAT14 PBUS14
PARDAT10 PBUS10 PARDAT09 PBUS09 PARDAT11 PBUS11 PARDAT08 PBUS08
PARDAT06 PBUS06 SYNCQ CRCPREFLAG- SHIFTIN SHIFTØUT PARDAT07 PBUS07
PARDAT04 PBUS04 PARDAT02 PBUS02 PARDAT01 PBUS01
PARDAT05 PBUS05 PARDAT03 PBUS03 PARDAT00 PBUS00
ØUTRDY- INRDY- DSKWRTQ
N05 H03 J04 M05 L02 M02
FIFØIN17 FIFØIN18 FIFØIN16 FIFØIN17
FIFØIN15 FIFØIN12 FIFØIN13 FIFØIN14
FIFØIN10 FIFØIN09 FIFØIN11 FIFØIN08
FIFØIN06 CRCPRES- SHIFT FIFØIN07
RDYSTATUS- FIFØIN04 FIFØIN02 FIFØIN01
FIFØIN05 FIFØIN03 FIFØIN00 ERRØRSET
TØ SH. 18
TØ SH. 19
TØ SH. 14
TØ SH. 16
PARDAT09 10 11 13 14 15 TØ SH. 14
FIFØIN00 THRU FIFØIN 5 TØ SH. 15
FIFØIN00 FIFØIN01 FIFØIN02 FIFØIN03 FIFØIN04
FIFØIN05 FIFØIN06 FIFØIN07 FIFØIN08 FIFØIN09
FIFØIN10 FIFØIN11 FIFØIN12 FIFØIN13 FIFØIN14
FIFØIN15 FIFØIN16 FIFØIN17 FIFØIN18 FIFØIN19
K03 K07 K04 K05
ØRDYA IRDYA ØRDYB IRDYB ØRDYC IRDYC ØRDYD IRDYD
TØ SH. 16
TØ SH. 18
TØ SH. 11, 13
TØ SH. 16
SHIFTØUT- SHIFTIN
DSKDIRECT- DSKCLR-
FIFØOUT00 THRU FIFØOUT15 TØ SH. 15
937502
D96214


DWG NO 937502 SH 18
FROM SH. 4 MPCK-
MPCK-
FROM SH. 15/16 PBUS00- THRU PBUS15-
TEST SOCKET
PBUS00- PBUS01- PBUS02- PBUS03- PBUS04- PBUS05- PBUS06- PBUS07-
VCC
CLKRUN
FROM SH. 4
G03
TEST SOCKET
PBUS08- PBUS09- PBUS10- PBUS11- PBUS12- PBUS13- PBUS14- PBUS15-
MCUADR1 MCUADR2 MCUADR8 MCUADR9
H06
STATE BOARD SOCKET
MCUADR1 MCUADR2 MCUADR3 MCUADR4 MCUADR5 MCUADR6 MCUADR7
CLKT2-
CLKRUN
FROM SH. 4
MCUADR9 MCUADR8
G06
MCUADR8, 9
TEST SOCKET
RDYSTATUSQ-
FROM SH. 16 SECTORMRKQ- RDYDIRSTATQ-
FROM SH. 14 DSTARTQ READQQ
FROM SH. 16 ADDACKQ
FROM SH. 13 TESTMODEQ DIAGFAULTQ-
20 VCC
TESTBITQ FROM SH. 12
INTA- FROM SH. 5
FIFOQUT18 FIFOQUT19 FROM SH. 17
SPAREIN2 SPAREIN1 FROM SH. 11
SPAREOUTQ1 FROM SH. 4
INDEXMRKQ- FROM SH. 16
G04
FROM SH. 6 MCUADR1 THRU MCUADR9
FIFO CONTROL
FROM SH. 12 RQM33L
FROM SH. 3 MDCMP-
FROM SH. 14 CNTEQ15
FROM SH. 13 DSKWRTQ-
FROM SH. 19 DCLK
FROM SH. 12 RQM33L-
FROM SH. 4 MPCK-
FROM SH. 15 FIFODATEN-
FROM SH. 14 DISKDATLD
LS32 D10 P09 D10 G12 N08
TLSHIN-
FROM SH. 12 UTCSHIN-
DSKSHIN-
TLSHOUT-
UTCSHOUT-
DSKSHOUT-
LS32 LS10 P09 LS10 L10
VCC
FROM SH. 17 FIFOIN19
FROM SH. 2 RST-
LS74 NO4
DCRCERRQ
DCRCERRQ-
SHIFTIN
SHIFTOUT
SHIFTOUT-
LS14 L06
TO SH. 13, 15, 17
TO SH. 10
TO SH. 17
FROM SH. 14 DSTARTQ DCLK1- FIFOQUT16 FIFOQUT17 FIFOQUT18 FIFOQUT19 DISKDATLD
FROM SH. 19
FROM SH. 17
FROM SH. 14
LS163 LS05
CL CK A B C D LD ENAP ENAT QA QB QC QD CO
CRCENFLAG-
CRCENFLAG
CRCPREFLAG
CRCPREFLAG-
LS14 L06
TO SH. 19
TO SH. 17
STOPFLAG
TO SH. 10
TEXAS INSTRUMENTS
DWN DATE
ISSUE DATE
SIZE D FSCM NO 96214
DRAWING NO 937502
REV J
SCALE
SHEET 18


DISK CLØCK AND DATA
DWG NO 937502 SH 19
TP1
WØSCSTØP-
FRØM SH. 13
DIAGFAULTQ-
DSKØSC-
DSKØSC
5 MHZ OSC. P11
R11 1K
VCC
WCLK
WCLK
WDNCLK-
P3
LS132 L10
LS132 M11
LS132 Z12
TP2
R35 1K
J7
WØSTST-
LS14 P07
WCLK-
LS74 N07
WCLKAQQ-
LS132 N08
WDNCLKEN
FRØM SH. 2
RST1-
RCLK-
LS14 R08
RCLK
J4
FRØM SH. 13
TESTCLK-
R81 180
R63 300
C09 390pF
R28 300
RD-
RD
RD1-
RDA-
J6
RDB
J3
LS14, L08
LS14 R08
LS74 N11
RDATA-
WRTCLK
DSKWRTQ
DSKWRTQ-
LS51 N09
DCLØCK-
LS132 N08
DCLØCK
DCLK1-
TØ SH. 17, 18
LS74 L07
DCLK
TØ SH. 18
DCLK-
TØ SH. 14
TESTMØDEQ
DIAGFAULTQ-
DCLK
DIAGFAULTQ-
FRØM SH. 13
VCC
VSS
REC
INI
CK
IN2
Ø1
Ø2
TMS 3129
L11 YGG
TESTDATA
TESTRDDAT-
LS132 M11
TESTCLK-
TESTØUTIN
RDATAQ
RDATA
LS74 P09
LS74 P08
FRØM SH. 2 RST-
WRDATØUT-
RDATAQ
DISKDATIN
DISKDATIN-
TØ SH. 17
TØ SH. 14
P1
4
M12V
C08 .047μF
DCLOCK1
LS14 L08
DCLOCK
DATCLK
U5
WRTDATØUT
FRØM SH. 2
RST1-
FRØM SH. 14
SYNCQ-
WRITEQ-
LS08 M12
IDLE
FRØM SH. 17
PARDATOO
LS153
1C0
1C1
1C2
1C3
1G
2C0
2C1
2C2
2C3
2G
SELB
SELA
1Y
2Y
WRTDATD
CRCDATIN
N06
FRØM SH. 18
CRCENFLAG
DSKWRTQ
FRØM SH. 17
CRCPRES-
FRØM SH. 18
CRCENFLAG-
9401 M06
CP
P
CWE
CRCERR
TØ SH. 17
CRCDATØUT
DISKDATIN
CRC GENERATØR/CHECKER
TEXAS INSTRUMENTS
DWN
DATE
ISSUE DATE
SIZE D
FSCM NO 96214
DRAWING NO 937502
REV L
SCALE
SHEET 19


DISK INTERFACE
TLG Ø
TLTM–
TLMER–
TLAG IN
TLAG ØUT
TLAK–
TLAV
TLWAIT
TILINE CØNTRØL INTERFACE P2
TILINE MASTER CØNTRØLLER P3
CLKRUN
CØNTRØLLER CLØCK GEN. P4
MPCK–
MPCK
MPCKMNT–
P-BUS SØURCE DESTINATIØN LØGIC P12
SPECIAL FUNCTIØN LØGIC P13
INTERFACE CØNTRØL P13
WRITE DATA MUX ENCØDER P19
WDICLK
PARDAT00
RØM
16
TLADR(00-19)–
TILINE ADDRESS CØMPARE P4
SLADØK
TILINE SLAVE CØNTRØLLER P4
M PGM MEMØRY 512 X 40 P6
RØM(00-39)
13-15
20-21
DISK WRT ØSCILLATØR P19
CRC. GEN., CHECKER MUX P19
DSKDATI
MCUADR 1-9
SLVACT
M SEQUENCE CØNTRØL P6
17-19
23-31
K-BUS SELECTØRS P7
SERIAL PARALLEL P17
PARDAT(00-15)
(17-19)
TESTBIT
TRAP
INTAD(0-3)
(01-07)
CPK(00-15)–
PBUS(00-15)
FIFØØUT(00-15)
MSB ADDRESS DRIVERS P8
INTERNAL INTERRUPTS LØGIC P5
CPE ARRAY PGS 8-11
F
K
MA
D/M
I
CPLCK–
CPRCK–
CPE CØNTRØL PGS 8 AND 10
FIFØ INPUT MUX P17
FIFØ 16 X 20 P17
(04-19)
FIFØIN(00-15)
MSB ADDRESS CØUNTER P8
LØØK AHEAD CARRY LØGIC P12
I-BUS LATCHES P16
P-BUS BUFFER P15
FIFØ/ZERØS SØURCE P15
TLDAT(00-15)–
TILINE DATA REC/DVR PGS 8-11
PBUS(00-15)–
UNIT SEL. REG. AND DRIVERS P14
CYL ADD. REG. AND DRIVERS P14
DSK STATUS RCVRS P16
DIRECT READ REGISTER P15
ADD128-001
TILINE INTERFACE
M-CØNTRØLLER
TEXAS INSTRUMENTS
SIZE D
96214
SHEET 20
REV B

DWG NO 937502 SH 21

0	1 7	8 9	10 11	12	13 15	16	17 19	20 21	22 31	32 33	34 35	36 39
CLKSTP	FUNCTIØN	WS	KC	CI	SØURCE	ENSLV	BRANCH	DEST	NRA	IMMEDIATE		
							CO=0 / CO=1			TILINE DP	SPECIAL GRØUP	SPECIAL FUNCTIØN
000	NØP	WØRD	F'S→K ENSP	1→CI	ODDO	NØP	RA+1→RA	NØP		NOP		
001	CLKSTP	RT SHFD WD	0'S→K ENSP	0→CI	CPE	ENSLV	NRA →RA	UNITLØAD		SLVTRM		
010		LEFT BYTE	IM →K		EXTERNAL		RA+1 →RA/NRA→RA	FIFØ		MSTRD		
011		RIGHT BYTE	IM →K		TILINE		NRA→RA, RA+1→RA	CYL ADDR		MSTWRT		
100					DSKDATA		NRA→RA/RA+1→STACK					
101							NRA→RA/STACK→RA					
110					DSKSTATUS		STACK→RA/NRA→RA					
111							STACK→RA					

(A)

RØM 36 37 38 39	RØM 34, 35 00	01	10
0 0 0 0	NØP	RST TESTMØDE	RST SPAREØUT1
0 0 0 1	CLK STØP MAST	SET TESTMØDE	SET SPAREØUT1
0 0 1 0	CLR DSK I/F	SET TESTCLK	RST RESTØRE
0 0 1 1	MSB ADR LD	RST TESTCLK	SET RESTØRE
0 1 0 0	STØP I/F CØNT.	RST I/F WRT	RST ERASE
0 1 0 1	MSB ADR INC	SET I/F READ	SET ERASE
0 1 1 0	CLR SECT/INDX	RST DIRECT MØDE	RST W.G.
0 1 1 1	NØP	SET DIRECT MØDE	SET W.G.
1 0 0 0	START I/F CØNT.	RST TL. INT	RST READ
1 0 0 1	NØP	SET TL. INT	SET READ
1 0 1 0	TRIGER TIMER	SET BUSY	RST SPAREØUT2
1 0 1 1	NØP	RST BUSY	SET SPAREØUT2
1 1 0 0	RST DIR. READY	SET FAULT	RST HEADSEL
1 1 0 1	NØP	RST FAULT	SET HEADSEL
1 1 1 0	CLR DISK CØNT.	SET DIAGFAULT	RST ADDSTB
1 1 1 1	NØP	RST DIAGFAULT	SET ADDSTB

(A)

RØM 34 35	RØM 36– 39
11	BIT 36 SET(ØNE) CAUSES CRC TØ BE ENABLED ØUT TØ DISK
11	BIT 37 SET(ØNE) CAUSES THE CRC CHARACTER GENERATØR TØ BE SET TØ A STATE ØF ALL ØNES
11	BIT 38 SET(ØNE) ENABLES A SPECIAL FLAG BIT TØ BE LØADED INTØ FIFØ TØ ALLØW THE CØNTRØLLER TØ DETECT WHEN A STØP CØNDITIØN IS PRESENT
11	BIT 39 IS AN UNUSED SPARE FLAG BIT

MICRØCØDE FIELD DEFINITIØNS

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
R0	SE SE I. ATTN MSK 0 1 2 3
R1	T.I. COMMAND SECTØRS/RECØRD
R2	SECTØRS/RECØRD DIAG. ERRØR # / SECTØR ADDRESS
R3	HD. CYLINDER
R4	FØRMAT WØRD
R5	TILINE WØRD CØUNT(2'S CØMPL)
R6	TILINE ADDRESS(04-19)
R7	UNIT SEL. 0 1 2 3 ; TILINE ADR. 00-03
R8	TDL COM ERR INT L.D. ØØ A.C. M.E. D.E. T.T. I.E. R.E. C.T. S.E. U.E.
R9	RECØRD WØRD CØUNT
T	TEST CØMPLETIØN CØUNT
AC	RECØRD WØRD CØUNT (2'S CØMPL.)
H	GENERAL UTILITY
	GENERAL UTILITY
	SECTØR-RDYSTATUS-STARTQ-RDYDIRSTAT-ADDRACK-READQ-DIAGFAULTQ-TESTMØDEQ-INDEX-STØPFLAG-SPAREØUTI-DCRCERRQ-SPAREIN2-SPAREINI-FIFØØUTI8-FIFØØUTI9-

		BIT PØSITIØN 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
PBUS SOURCE	ZERØ'S	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø
	CPE	CPE ARRAY ØUTPUT (AC)
	EXTERNAL	FLØAT
	TILINE	TILINE DATA 00-15
	DISK DATA	(DIRECT DATA) DISK DATA (FIFØ ØUTPUT)
	DISK STATUS	ØFFLINE, NØT READY, WRTPRØT, UNSAFE, SPAREIN6, SEEKINC, SPAREIN3, SPAREIN5, SWB, SWA, SPAREIN4, SECTØRB16, SECTØRB8, SECTØRB4, SECTØRB2, SECTØRB1
PBUS DESTINATIØN	NØNE	NØP
	UNIT	SPARE1, SELB, SELA, DSKSEL
	FIFO	FIFØ INPUT 00-15
	CYL. ADD.	ADD256, ADD128, ADD064, ADD032, ADD016, ADD008, ADD004, ADD002, ADD001

	DAN	DATE	SIZE	FSCM NO	DRAWING NO	REV
TEXAS INSTRUMENTS	TITLE		D	96214	937502	C
			SCALE		SHEET 21	

DWG NO 937502 SH 22

MICRØ-FUNCTIØN SUMMARY

STEP	F-GRØUP	R-GRØUP	MICRO-FUNCTIØNS	
1		I	$R_N+(AC\wedge K)+CI\rightarrow R_N \cdot AC$	
2	0	II	$M+(AC\wedge K)+CI\rightarrow AT$	
3		III	$AT_L\wedge(\overline{I_L\wedge K_L})\rightarrow RO$ $LI\vee[(I_H\wedge K_H)\wedge AT_H]\rightarrow AT_H$ $[AT_L\wedge(I_L\wedge K_L)]\vee[AT_H\vee(I_H\wedge K_H)]\rightarrow AT_L$	
4		I	$K\vee R_N\rightarrow MAR$	$R_N+K+CI\rightarrow R_N$
5	1	II	$K\vee M\rightarrow MAR$	$M+K+CI\rightarrow AT$
6		III	$(\overline{AT}\vee K)+(AT\wedge K)+CI\rightarrow AT$	
7		I	$(AC\wedge K)\cdot 1+CI\rightarrow R_N$	
8	2	II	$(AC\wedge K)\cdot 1+CI\rightarrow AT$	SEE NØTE (1)
9		III	$(I\wedge K)\cdot 1+CI\rightarrow AT$	
10		I	$R_N+(AC\wedge K)+CI\rightarrow R_N$	
11	3	II	$M+(AC\wedge K)+CI\rightarrow AT$	
12		III	$AT+(I\wedge K)+CI\rightarrow AT$	
13		I	$CI\vee(R_N\wedge AC\wedge K)\rightarrow CO$	$R_N\wedge(AC\wedge K)\rightarrow R_N$
14	4	II	$CI\vee(M\wedge AC\wedge K)\rightarrow CO$	$M\wedge(AC\wedge K)\rightarrow AT$
15		III	$CI\vee(AT\wedge I\wedge K)\rightarrow CO$	$AT\wedge(I\wedge K)\rightarrow AT$
16		I	$CI\vee(R_N\wedge K)\rightarrow CO$	$K\wedge R_N\rightarrow R_N$
17	5	II	$CI\vee(M\wedge K)\rightarrow CO$	$K\wedge M\rightarrow AT$
18		III	$CI\vee(AT\wedge K)\rightarrow CO$	$K\wedge AT\rightarrow AT$
19		I	$CI\vee(AC\wedge K)\rightarrow CO$	$R_N\vee(AC\wedge K)\rightarrow R_N$
20	6	II	$CI\vee(AC\wedge K)\rightarrow CO$	$M\vee(AC\wedge K)\rightarrow AT$
21		III	$CI\vee(I\wedge K)\rightarrow CO$	$AT\vee(I\wedge K)\rightarrow AT$
22		I	$CI\vee(R_N\wedge AC\wedge K)\rightarrow CO$	$R_N\ \overline{\oplus}\ (AC\wedge K)\rightarrow R_N$
23	7	II	$CI\vee(M\wedge AC\wedge K)\rightarrow CO$	$M\ \overline{\oplus}\ (AC\wedge K)\rightarrow AT$
24		III	$CI\vee(AT\wedge I\wedge K)\rightarrow CO$	$AT\ \overline{\oplus}\ (I\wedge K)\rightarrow AT$

NØTES:
1. 2'S COMPLEMENT ARITHMETIC ANDS 111...11 TØ PERFØRM SUBTRACTIØN ØF 000...01.
2. R_N INCLUDES T AND AC AS SØURCE AND DESTINATIØN REGISTERS IN F-GRØUP 1 MICRO-FUNCTIØNS.
3. STANDARD ARITHMETIC ARRY ØUTPUT VALUES ARE GENERATED IN F-GRØUP 0, 1, 2 AND 3 INSTRUCTIØNS.

LEGEND

SYMBØL	MEANING
I, K, M	DATA ØN THE I, K, AND M BUSES, RESPECTIVELY
CI, LI	DATA ØN THE CARRY INPUT AND LEFT INPUT, RESPECTIVELY
CO, RO	DATA ØN THE CARRY ØUTPUT AND RIGHT ØUTPUT, RESPECTIVELY
R_N	CØNTENTS ØF REGISTER N INCLUDING T AND AC (R-GRØUP 1)
AC	CØNTENTS ØF THE ACCUMULATØR
AT	CØNTENTS ØF AC ØR T, AS SPECIFIED
MAR	CØNTENTS ØF THE MEMØRY ADDRESS REGISTER
+	2'S CØMPLEMENT ADDITIØN
$\wedge$	LØGICAL AND
$\vee$	LØGICAL ØR
$\overline{\oplus}$	EXCLUSIVE NØR
$\rightarrow$	DEPØSIT INTØ

FUNCTIØN GRØUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GRØUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SLAVES

	READ ADRS.	WRITE ADRS
SLAVE Ø	ØFØ	ØF8
SLAVE 1	ØF1	ØF9
SLAVE 2	ØF2	ØFA
SLAVE 3	ØF3	ØFB
SLAVE 4	ØF4	ØFC
SLAVE 5	ØF5	ØFD
SLAVE 6	ØF6	ØFE
SLAVE 7	ØF7	ØFF

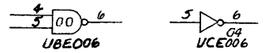
TRAPS

TRAP ADRS.	DESCRIPTIØN
ØØØ	TLABØRTQ- (I/Ø RESET, PFWP, TLPRES)
010	MDTØQ- (TILINE TIMEØUT)
020	TLERRQ-(MEMØRY PARITY ERRØR)
030	CLRWRTQ- (RATE ERRØR)
040	CMDTMRQ-(CØMMAND TIMER)

TEXAS INSTRUMENTS | DWN | DATE | ISSUE DATE | SIZE D | FSCM NO 96214 | DRAWING NO 937502 | REV B | SCALE | SHEET 22

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL DEVICE TYPES PREFIXED WITH 3N74.
2. GROUND IS APPLIED TO PIN 7 OF ALL 14 PIN IC'S. PIN 8 OF ALL 16-PIN IC'S, PIN 10 OF ALL 20 PIN IC'S. AND PIN 14 OF ALL 28-PIN IC'S.
3. VCC IS APPLIED TO PIN 14 OF ALL 14-PIN IC'S. PIN 16 OF ALL 16 PIN IC'S. PIN 20 OF ALL 20-PIN IC'S. AND PIN 28 OF ALL 28-PIN IC'S.
4. DEVICE TYPE. PIN NUMBERS. AND LOCATION OF IC IS SHOWN AS FOLLOWS:



00 AND 04 = DEVICE TYPE
4, 5 AND 6 = PIN NUMBERS
UBE006 AND UCE006 = LOCATION: FIRST THREE LETTERS DENOTE ROW WITH EACH LETTER INCREMENTED EVERY .100 INCH. THE NEXT THREE NUMERALS DENOTE COLUMN WITH EACH DIGIT INCREMENTED EVERY .108 INCH. IC(PIN 1) IS LOCATED AT INTERSECTION OF ROW AND COLUMN. (ALL LOCATIONS ARE PREFIXED ON THE ASSEMBLY SILKSCREEN BY THE LETTER "U").

5. ALL RESISTORS ARE 1/4 WATT.

NOTES: CONTINUED

6. JUMPER INSTALLED TO ALLOW THE CONTROLLER TO RUN LONG SELF DIAGNOSTIC TEST ON POWER UP TO BE USED BY UNIT TEST ONLY.
7. SWITCH 5 AND 6 ARE NORMALLY NOT INSTALLED ON BOARD BUT MAY BE ADDED AS OPTION LATER.
8. THIS JUMPER (J5) IS USED TO INVERT THE PHASE OF THE WRITE CLOCK IF NEED BE.
9. J3, J4, J6 AND J7 ARE INSTALLED AS SHOWN AND ARE USED TO CHANGE THE DATA INTERFACE FROM A 10 MEGA BYTE DRIVE TO A 20 MEGA BYTE DRIVE.

~~10. THIS CAPACITOR IS OMITTED AT ASSEMBLY AND MAY BE ADDED AT UNIT TEST ON TIMING REQUIREMENTS~~

11. RESISTOR VALUES ARE 180 OHM.
12. RESISTOR VALUES ARE 300 OHM.
13. RESISTOR VALUES MAY BE CHANGED TO MEET TIMING SPECIFICATIONS PER TEST PROCEDURE.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	CN 47Z729(E)	7/1/	
B	CN 47213(C)	11-17-80	
C	CN 47213(D)	1/	
D	CN 47213(E)	3-26-81	
E	CN 47615(D)	5-22-81	
F	CN 48571(D)	2-16-82	

REVISION STATUS	REV	F	C	C	F	C	A	A	A	A	C	E	D	C	C	C	C	A	C			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

SEC NO	CONT	FSPEC	NO	ADDITIONAL	NOTES
	PROCESS			CLASSIFICATION	

ADDITIONAL CLASSIFICATION TO GOVT MD SPECIFICATIONS SEE TI DRAWING 729367

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
			PARTS LIST		
		2262100	7506		
		NEXT ASSY	USED ON		
		APPLICATION			

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER M.I.D.1002
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .104 ± .001	.126 THRU .250 ± .001	.251 THRU .500 ± .001
.501 THRU .750 ± .001	.751 THRU 1.000 ± .001	1.001 THRU 2.000 ± .001

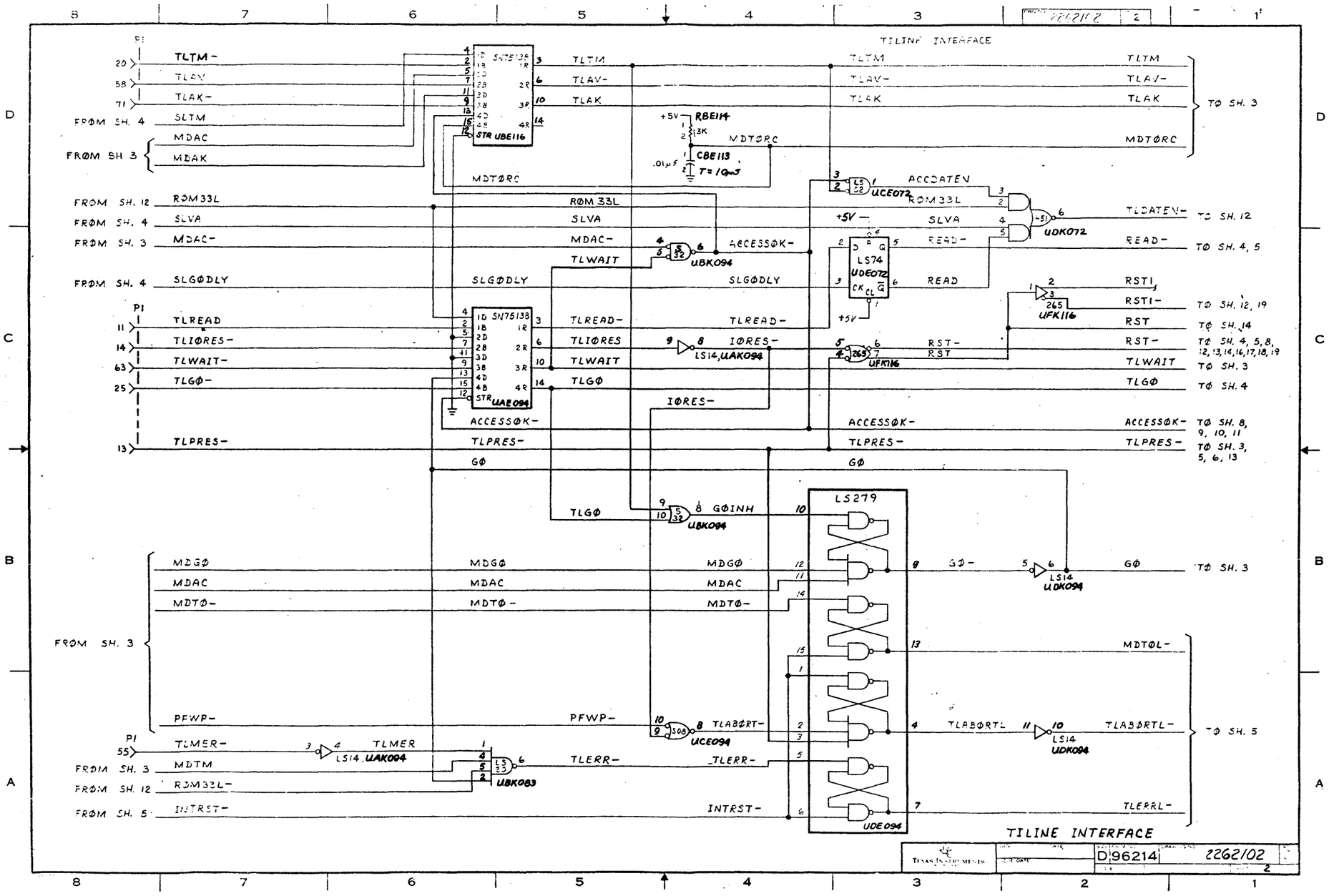
DRAWN [illegible] DATE 7-6-72
CHK Ryder 11-30-79
ENGR [illegible] 2-25-81
MFG [illegible] 2-16-82
QUAL
R/E [illegible] 3-5-82

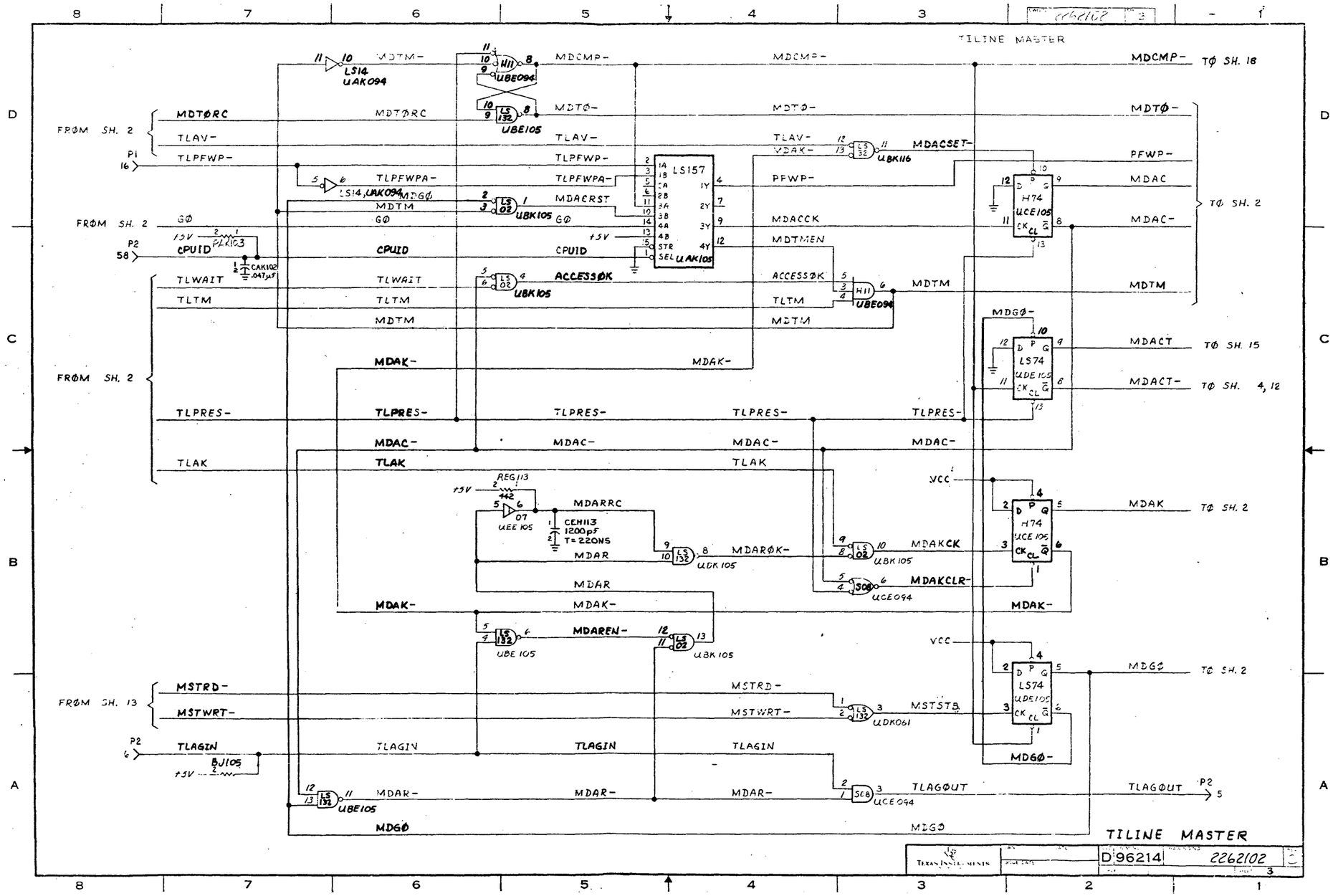
TEXAS INSTRUMENTS INCORPORATED Dallas Texas

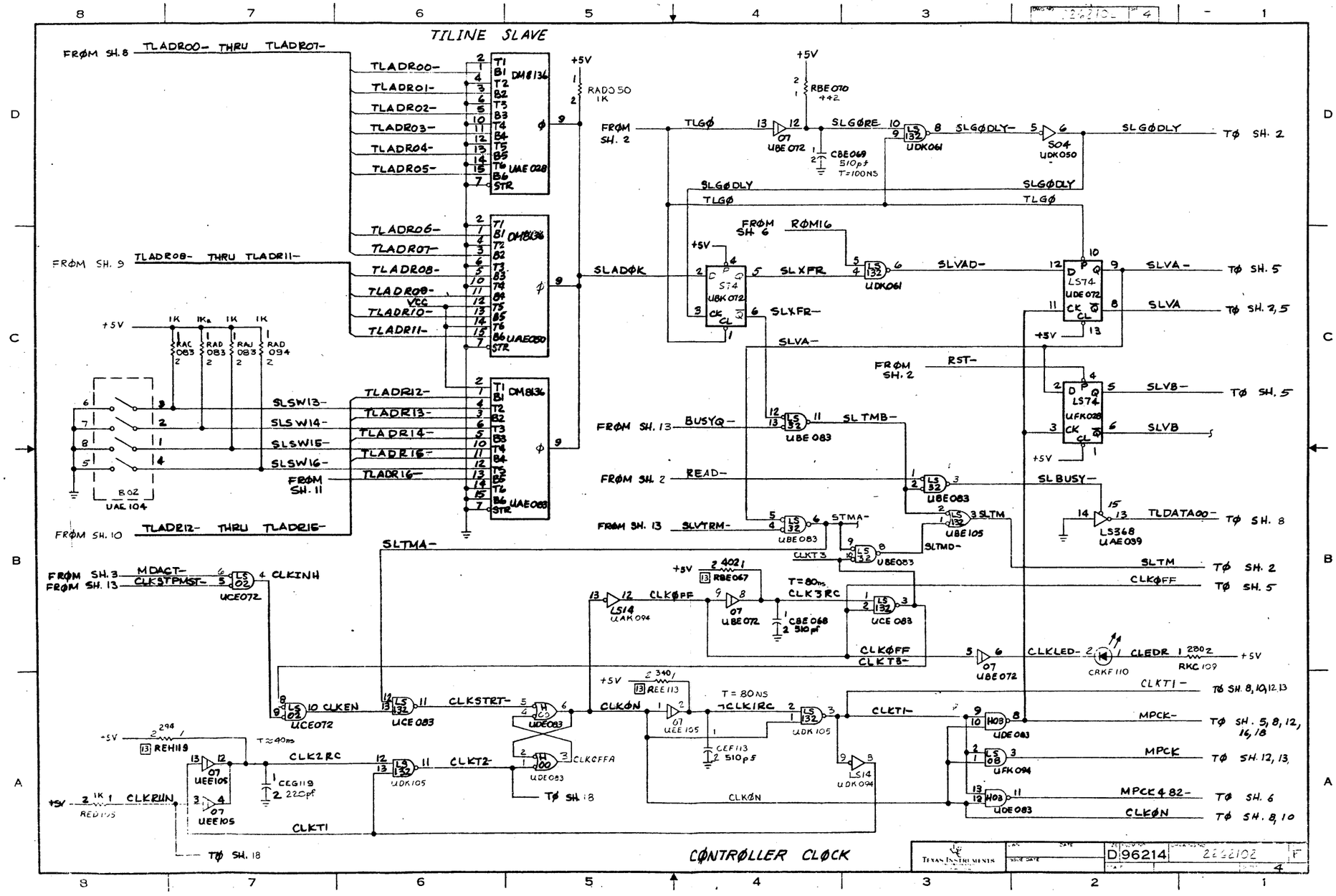
DIAGRAM, LOGIC, DETAILED, 10 MEGA BYTE DISK CONTROLLER (FINE LINE)

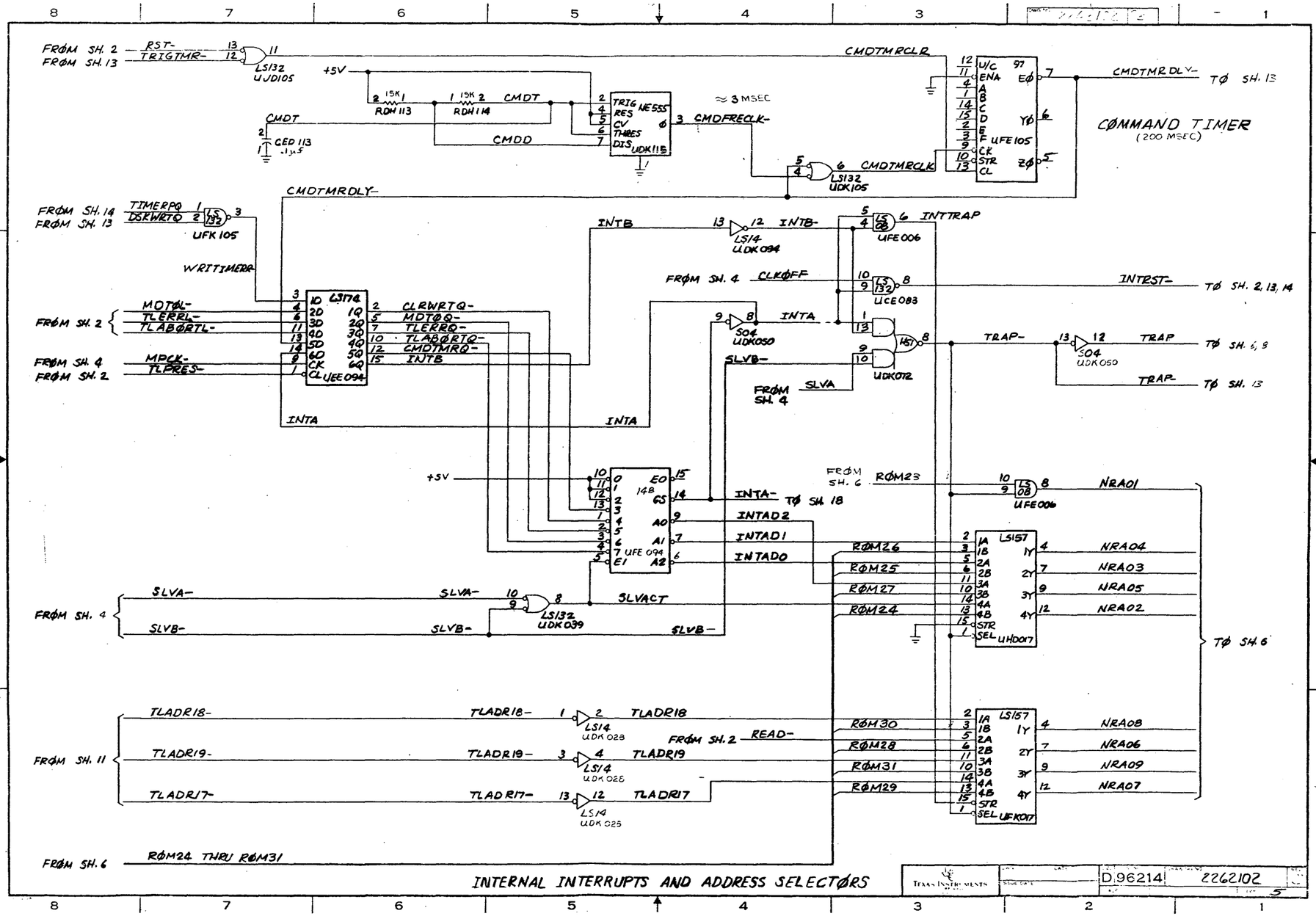
SIZE	CODE IDENT NO	DRAWING NO
D	96214	2262102

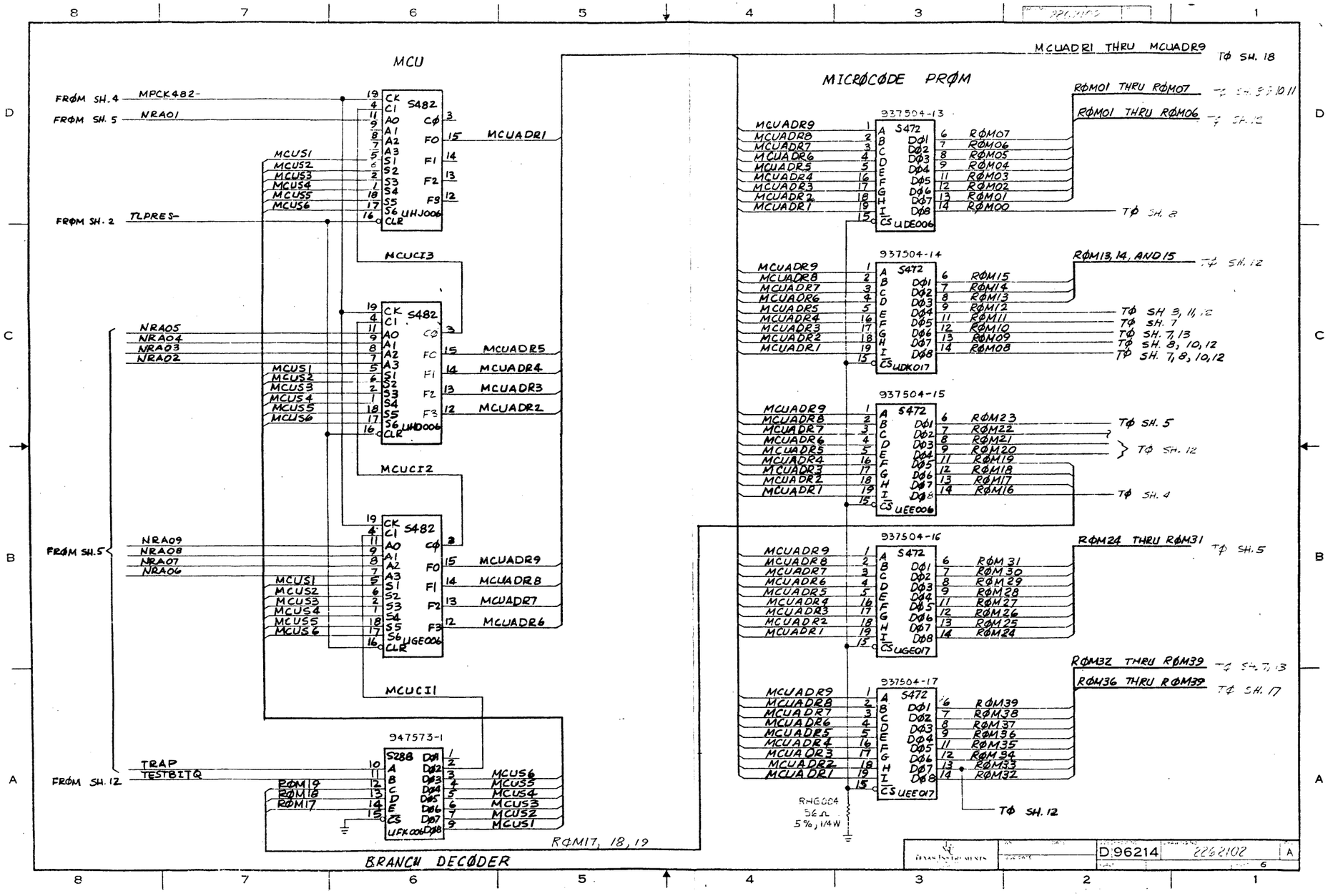
1 OF 22

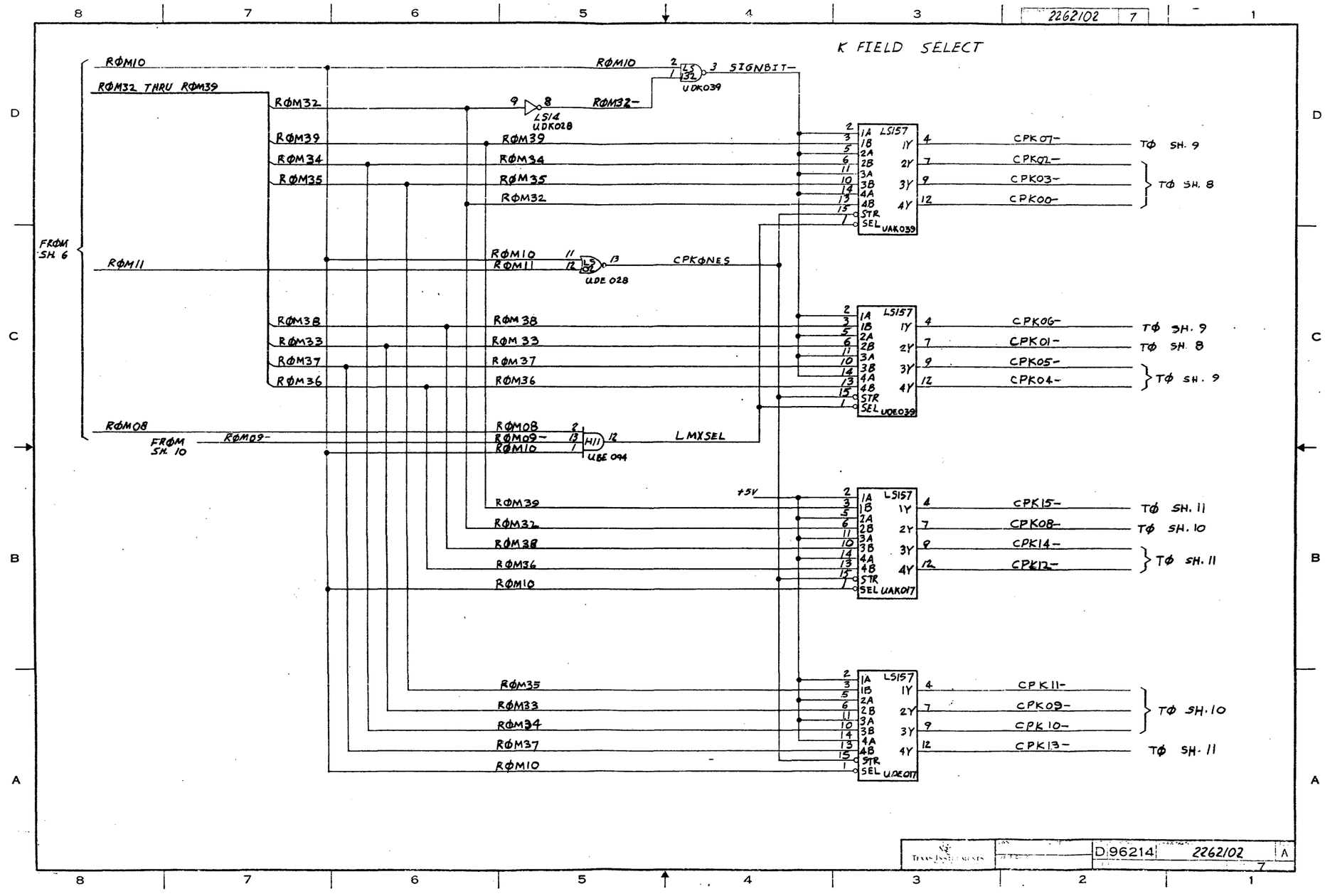

TILINE INTERFACE
TLTM-
TLAV
TLAK-
SLTM
MDAC
MDAK
FROM SH. 4
FROM SH 3
FROM SH. 12
FROM SH. 4
FROM SH. 3
FROM SH. 4
RØM33L
SLVA
MDAC-
SLGØDLY
P1
TLREAD
TLIØRES-
TLWAIT-
TLGØ-
TLPRES-
13
SN75138
STR UBE116
STR UAE094
RBE114
3K
CBE113
.01µF
T=10nS
MDTØRC
ACCESSØK-
TLPRES-
GØ
TLREAD-
TLIØRES
TLWAIT
TLGØ
IØRES-
TLGØ
GØINH
UBK094
LS14, UAK094
ACCDATEN
UCE072
ROM33L
SLVA
+5V
LS74
UDE072
READ-
READ
RST
UFK116
LS279
UDE094
TLTM
TLAV-
TLAK
MDTØRC
TØ SH. 3
TLDATEN-
TØ SH. 12
READ-
TØ SH. 4, 5
RSTI
RSTI-
TØ SH. 12, 19
RST
TØ SH. 14
RST-
TØ SH. 4, 5, 8, 12, 13, 14, 16, 17, 18, 19
TLWAIT
TØ SH. 3
TLGØ
TØ SH. 4
ACCESSØK-
TØ SH. 8, 9, 10, 11
TLPRES-
TØ SH. 3, 5, 6, 13
GØ-
MDTØL-
TLABØRTL
TLABØRTL-
TØ SH. 5
TLERRL-
MDGØ
MDAC
MDTØ-
PFWP-
TLABØRT-
UCE094
TLMER-
TLMER
MDTM
ROM33L-
INTRST-
TLERR-
UBK083
D 96214
2262102

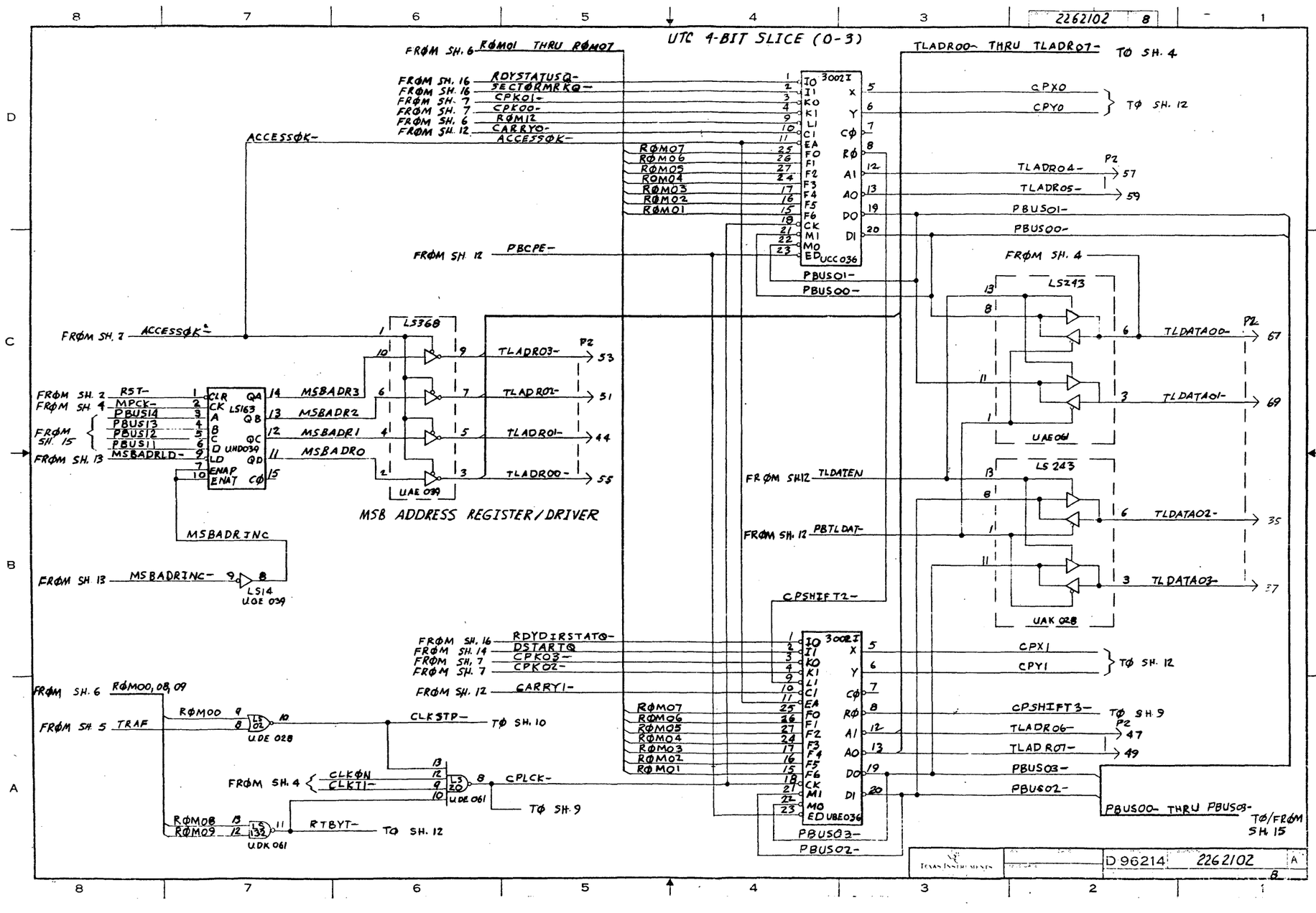

TILINE MASTER
FROM SH. 2
MDTØRC
TLAV-
TLPFWP-
P1 16
MDTM-
LS14, UAK094
LS11 UBE094
MDCMP-
LS132 UBE105
MDTØ-
TLPFWPA-
MDGØ
MDTM
MDARST
LS02 UBK105
GØ
CPUID
P2 58
+5V
PLR103
CAK102 .047µF
TLWAIT
TLTM
ACCESSØK
LS157 UAK105
MDTMEN
LS32 UBK116
MDACSET-
PFWP-
MDAC
MDAC-
H74 UCE105
TØ SH. 2
MDTM
MDGØ-
MDACT
MDACT-
TØ SH. 15
TØ SH. 4, 12
MDAK-
TLPRES-
MDAC-
TLAK
REG113
+42
UEE105 07
CEH113 1200pF T=220NS
MDARRC
MDAR
MDARØK-
UDK105
MDAKCK
UBK105
MDAKCLR-
UCE094
VCC
MDAK
TØ SH. 2
MDAREN-
UBE105
UBK105
FROM SH. 13
MSTRD-
MSTWRT-
MSTSTB
UDK061
MDGØ
P2
TLAGIN
BJ105
MDAR-
UBE105
TLAGØUT
TØ SH. 18
TILINE MASTER
TEXAS INSTRUMENTS
D 96214
2262102
3

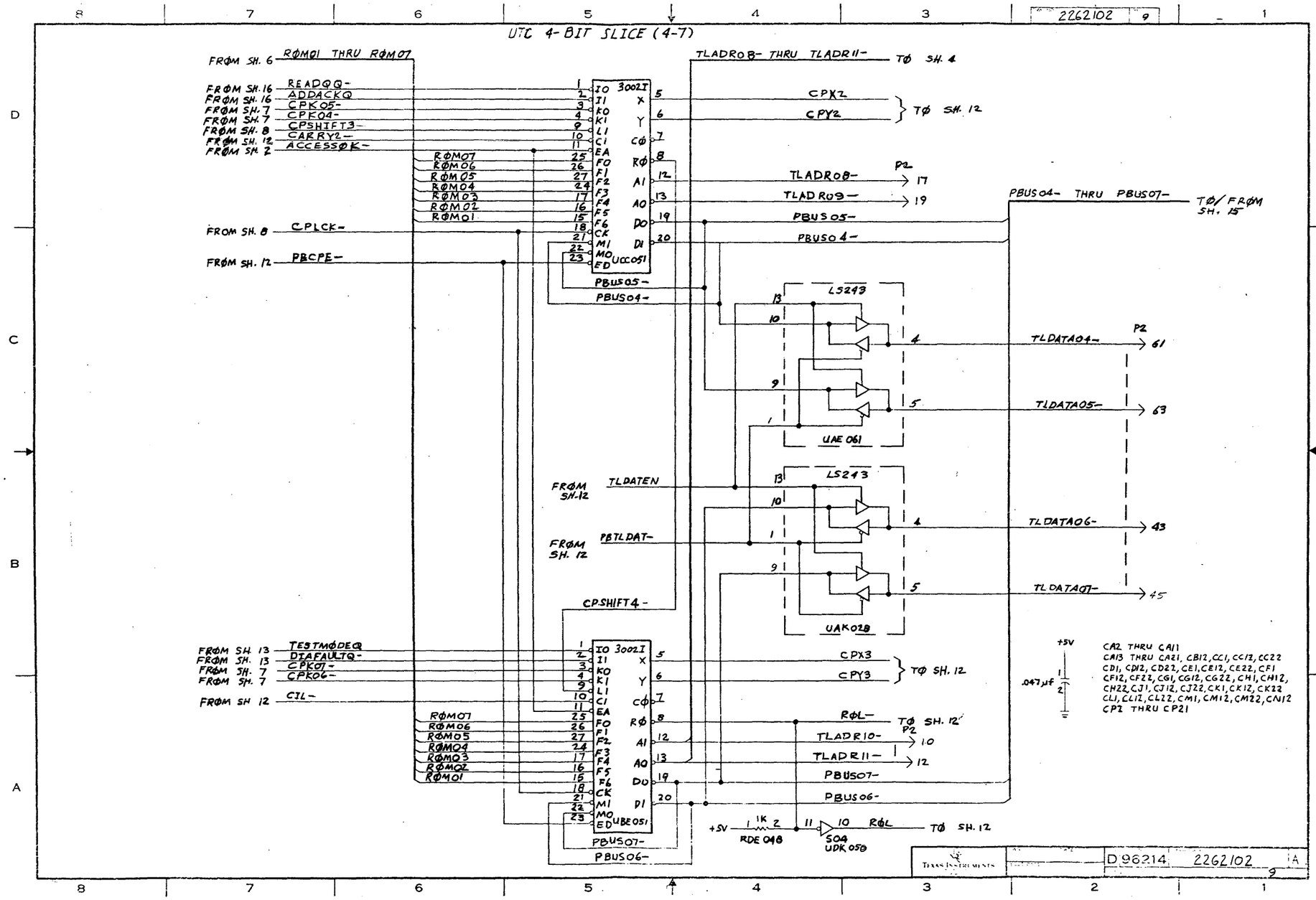

TILINE SLAVE
FROM SH. 8 TLADR00- THRU TLADR07-
FROM SH. 9 TLADR08- THRU TLADR11-
FROM SH. 10 TLADR12- THRU TLADR15-
TLADR00-
TLADR01-
TLADR02-
TLADR03-
TLADR04-
TLADR05-
TLADR06-
TLADR07-
TLADR08-
TLADR09-
TLADR10-
TLADR11-
TLADR12-
TLADR13-
TLADR14-
TLADR15-
TLADR16-
DM8136
UAE028
UAE050
UAE083
+5V
RAD050 1K
SLADØK
FROM SH. 11
SLSW13-
SLSW14-
SLSW15-
SLSW16-
B02
UAE104
FROM SH. 2 TLGØ
TLGØ
SLGØRE
SLGØDLY-
SLGØDLY
TØ SH. 2
RBE070 442
CBE069 510pf T=100NS
UBE072
UDK061
UDK050
FROM SH. 6 RØM16
SLXFR
SLXFR-
SLVAD-
SLVA-
SLVA
TØ SH. 5
TØ SH. 2,5
LS74 UBK072
LS74 UDE072
SLVA-
FROM SH. 2 RST-
SLVB-
SLVB
TØ SH. 5
LS74 UFK028
FROM SH. 13 BUSYQ-
SL TMB-
UBE083
FROM SH. 2 READ-
SL BUSY-
FROM SH. 13 SLVTRM-
STMA-
SLTMA-
SLTM
SLTMD-
UBE105
CLKT3
TLDATA00-
TØ SH. 8
LS368 UAE039
SLTM
TØ SH. 2
CLKØFF
TØ SH. 5
FROM SH. 3 MDACT-
FROM SH. 13 CLKSTPMST-
UCE072
CLKINH
CLKØFF
CLKT3-
CLKLED-
CLEDR 1 280Ω
RKC109
CRKF110
+5V
T=80ns CLK3RC
CBE068 510pf
UCE083
LS14 UAK094
CLKT1-
TØ SH. 8,10,12,13
MPCK-
TØ SH. 5,8,12, 16,18
MPCK
TØ SH. 12, 13
MPCK4 82-
TØ SH. 6
CLKØN
TØ SH. 8,10
UDE083
CLKSTRT-
CLKØN
T=80NS ¬CLK1RC
CLKT1-
UEE105
UDK105
UDK094
CLK2RC
CLK2T-
CLKCFFA
CEG119 220pf
CEF113 510pf
T≈40ns
REH119 298Ω
REE113 340Ω
RBE067 402Ω
REE105 1K
CLKRUN
CLKT1
TØ SH. 18
CONTRØLLER CLØCK
TEXAS INSTRUMENTS
D96214
2266102
F

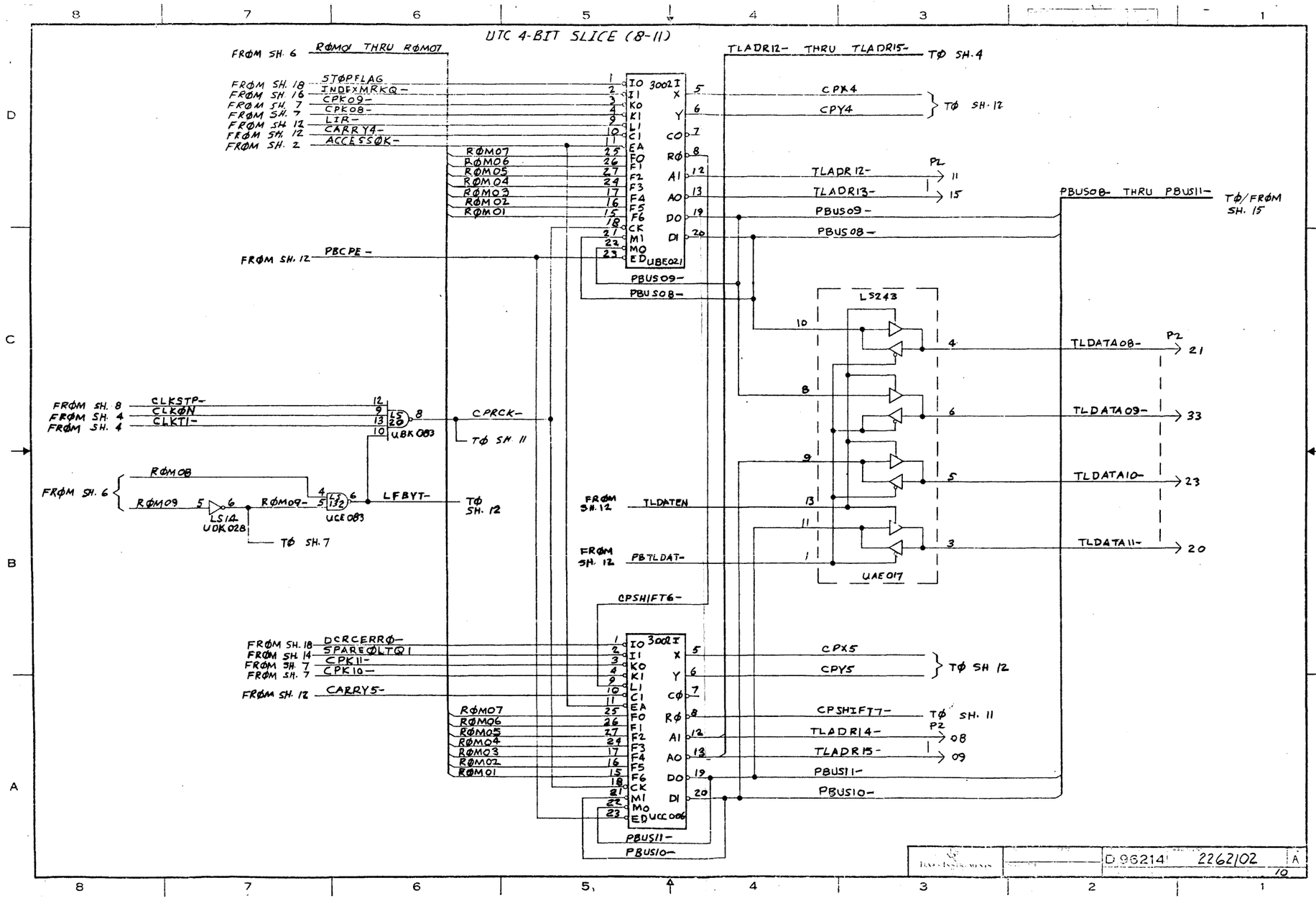

FRØM SH. 2
FRØM SH. 13
RST-
TRIGTMR-
LS132
UUDI05
+5V
15K
RØM113
RØM114
CMDT
CED 113
.1µF
CMDD
TRIG NE555
RES
CV
THRES
DIS UDK115
≈ 3 MSEC
CMDFRCLK-
CMDTMRCLR
U/C
ENA
A
B
C
D
F ULFE105
CK
STR
CL
EØ
YØ
ZØ
CMDTMRDLY-
TØ SH. 13
COMMAND TIMER
(200 MSEC)
CMDTMRCLK
LS132
UDK105
FRØM SH. 14
FRØM SH. 13
TIMERPØ
DSKWRTØ
LS132
UFK105
WRITIMERR
INTB
LS14
UDK094
INTB-
LS08
UFE006
INTTRAP
FRØM SH. 4
CLKØFF
INTREST-
TØ SH. 2, 13, 14
UCE083
INTA
S04
UDK050
SLVB-
FRØM SH. 4
SLVA
UDK012
TRAP-
TØ SH. 6, 8
TØ SH. 13
FRØM SH. 2
MDTØL-
TLERRL-
TLABØRTL-
FRØM SH. 4
FRØM SH. 2
MPCK-
TLPRES-
LS174
UEE094
CLRWRTQ-
MDTØQ-
TLERRQ-
TLABØRTQ-
CMDTMRQ-
INJTB
INTA
+5V
148
UFE094
EO
GS
A0
A1
A2
E1
INTA-
TØ SH. 18
INTAD2
INTAD1
INTAD0
FRØM SH. 6
RØM23
NRA01
RØM26
RØM25
RØM27
RØM24
LS157
UHD017
NRA04
NRA03
NRA05
NRA02
TØ SH. 6
FRØM SH. 4
SLVA-
SLVB-
LS132
UDK039
SLVACT
FRØM SH. 11
TLADR18-
TLADR19-
TLADR17-
LS14
UDK028
UDK026
UDK025
TLADR18
TLADR19
TLADR17
FRØM SH. 2
READ-
RØM30
RØM28
RØM31
RØM29
NRA08
NRA06
NRA09
NRA07
UFK017
FRØM SH. 6
RØM24 THRU RØM31
INTERNAL INTERRUPTS AND ADDRESS SELECTØRS
TEXAS INSTRUMENTS
D.96214
2262102

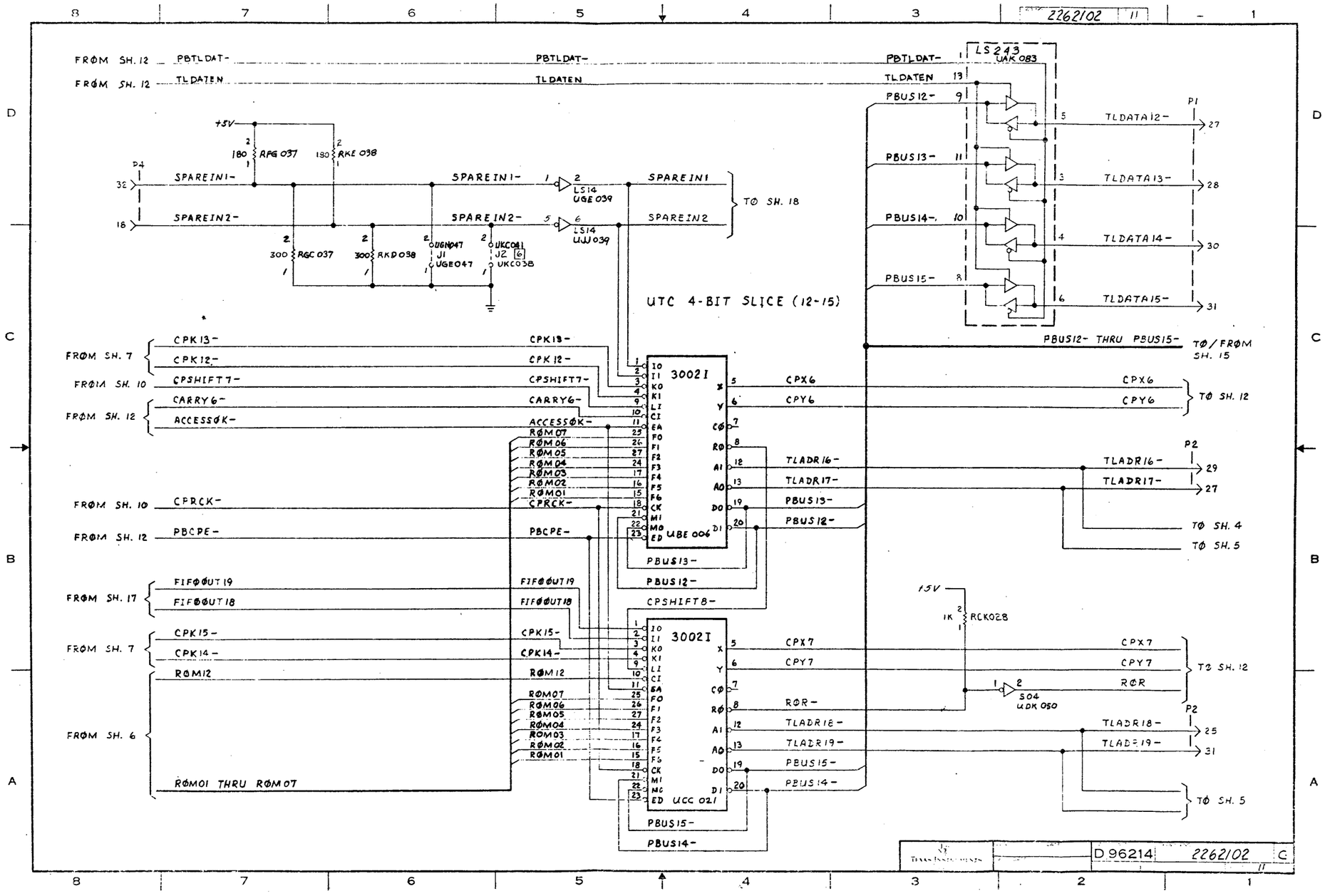

MCU
MICROCODE PROM
BRANCH DECODER
FROM SH. 4
MPCK482-
FROM SH. 5
NRAO1
MCUS1
MCUS2
MCUS3
MCUS4
MCUS5
MCUS6
FROM SH. 2
TLPRES-
S482
MCUCI3
MCUCI2
MCUCI1
MCUADR1
MCUADR5
MCUADR4
MCUADR3
MCUADR2
MCUADR9
MCUADR8
MCUADR7
MCUADR6
NRAO5
NRAO4
NRAO3
NRAO2
NRAO9
NRAO8
NRAO7
NRAO6
FROM SH. 5
TRAP
TESTBITQ
FROM SH. 12
947573-1
S288
ROM 19
ROM 18
ROM 17
UFK006
MCUADR1 THRU MCUADR9
TO SH. 18
937504-13
S472
UDE006
ROMO1 THRU ROMO7
TO SH. 9, 10, 11
ROMO1 THRU ROMO6
TO SH. 12
ROMO7
ROMO6
ROMO5
ROMO4
ROMO3
ROMO2
ROMO1
ROMOO
TO SH. 2
937504-14
UDK017
ROM13, 14, AND 15
TO SH. 12
ROM15
ROM14
ROM13
ROM12
ROM11
ROM10
ROM09
ROM08
TO SH 3, 11, 12
TO SH. 7
TO SH. 7, 13
TO SH. 8, 10, 12
TO SH. 7, 8, 10, 12
937504-15
UEE006
ROM23
ROM22
ROM21
ROM20
ROM19
ROM18
ROM17
ROM16
TO SH. 5
TO SH. 12
TO SH. 4
937504-16
UGE017
ROM24 THRU ROM31
TO SH. 5
ROM31
ROM30
ROM29
ROM28
ROM27
ROM26
ROM25
ROM24
937504-17
UEE017
ROM32 THRU ROM39
TO SH. 7, 13
ROM36 THRU ROM39
TO SH. 17
ROM39
ROM38
ROM37
ROM36
ROM35
ROM34
ROM33
ROM32
TO SH. 12
RNC60A
56Ω
5%, 1/4W
RCM17, 18, 19
D 96214
2262102
A

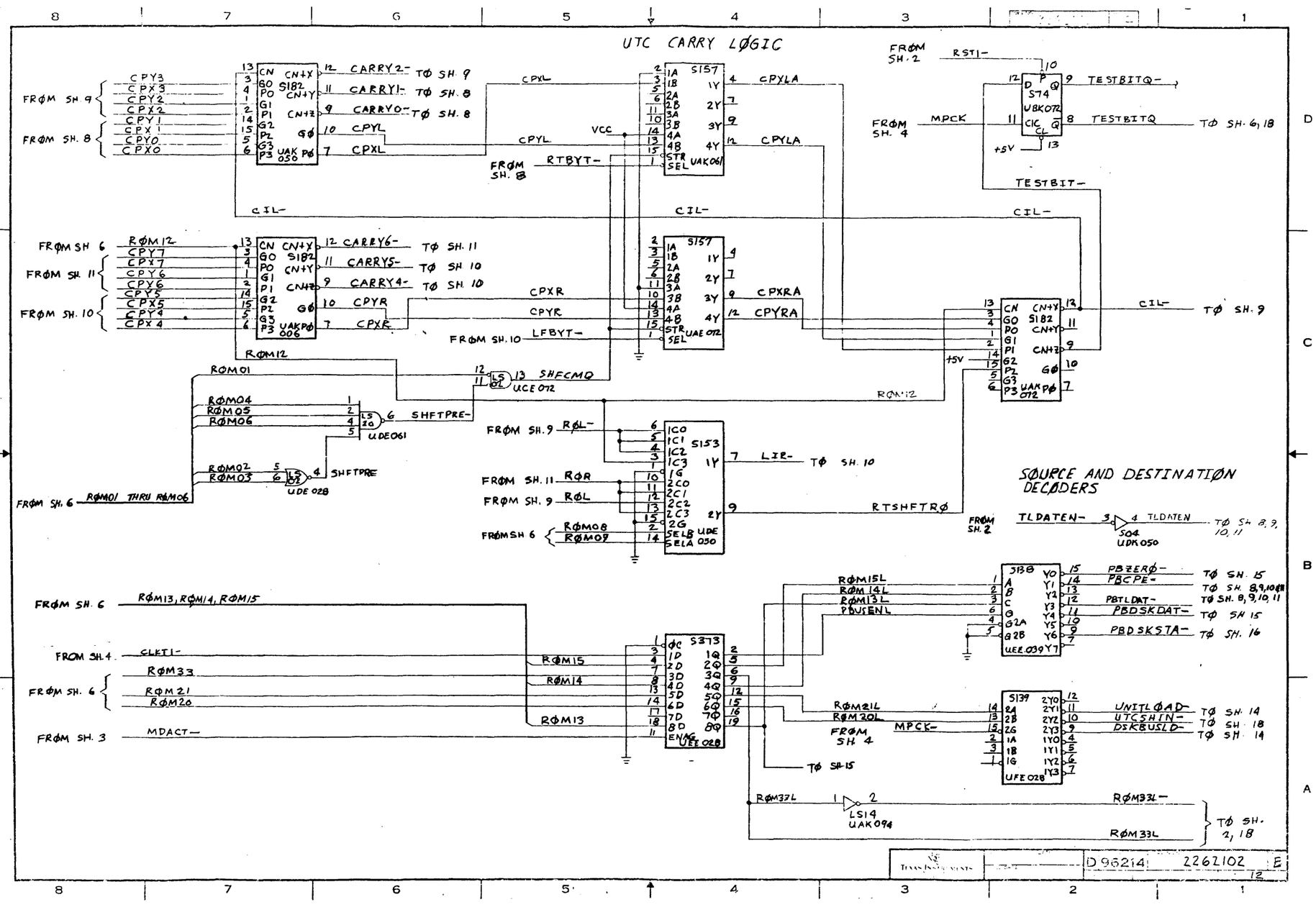

2262102 7
K FIELD SELECT
RØM10
RØM32 THRU RØM39
RØM11
RØM08
FROM SH. 6
FROM SH. 10
RØM09-
SIGNBIT-
UDK039
LS14
UDK028
RØM32-
RØM39
RØM34
RØM35
RØM32
RØM38
RØM33
RØM37
RØM36
CPKØNES
UDE028
LMXSEL
UBE094
+5V
LS157
UAK039
UDE039
UAK017
UDE017
CPK07-
CPK02-
CPK03-
CPK00-
CPK06-
CPK01-
CPK05-
CPK04-
CPK15-
CPK08-
CPK14-
CPK12-
CPK11-
CPK09-
CPK10-
CPK13-
TØ SH. 9
TØ SH. 8
TØ SH. 11
TØ SH. 10
D 96214 2262/02 A

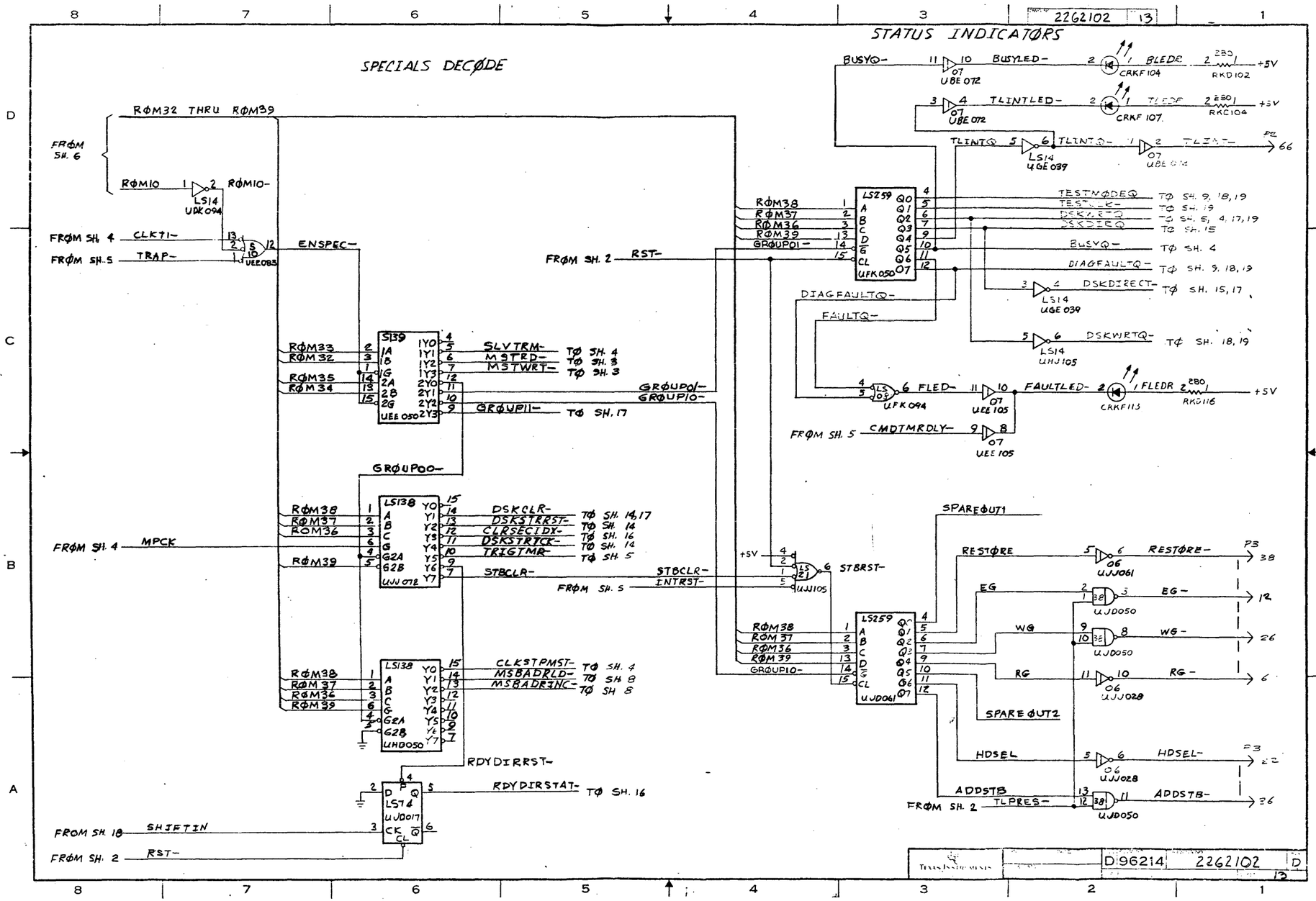

UTC 4-BIT SLICE (0-3)
MSB ADDRESS REGISTER/DRIVER
TLADR00- THRU TLADR07- TO SH. 4
FROM SH. 6 RØM01 THRU RØM07
ACCESSØK-
PBCPE-
MSBADRINC
CPSHIFT2-
CPSHIFT3-
PBUS00- THRU PBUS03-
TØ/FROM SH. 15
D 96214 2262102

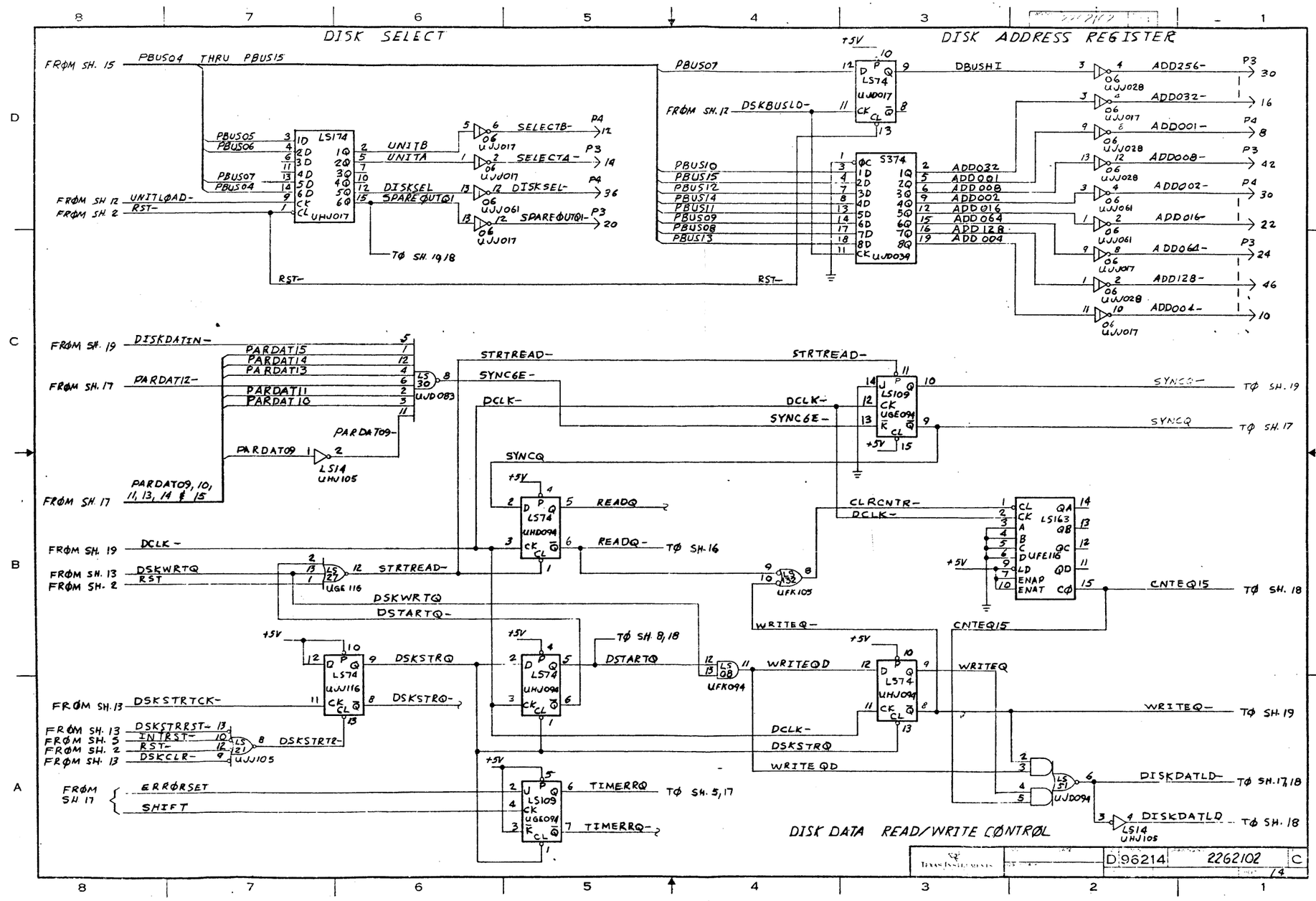

UTC 4-BIT SLICE (4-7)
2262102
FROM SH. 6 R0M01 THRU R0M07
TLADR08- THRU TLADR11-
TØ SH. 4
FROM SH. 16 READQQ-
FROM SH. 16 ADDACKQ
FROM SH. 7 CPK05-
FROM SH. 7 CPK04-
FROM SH. 8 CPSHIFT3-
FROM SH. 12 CARRY2-
FROM SH. 7 ACCESSØK-
R0M07
R0M06
R0M05
R0M04
R0M03
R0M02
R0M01
3002I
UCC051
CPX2
CPY2
TØ SH. 12
TLADR08-
TLADR09-
P2
17
19
PBUS04- THRU PBUS07-
TØ/FROM SH. 15
PBUS05-
PBUS04-
FROM SH. 8 CPLCK-
FROM SH. 12 PBCPE-
LS243
UAE061
TLDATA04-
TLDATA05-
61
63
FROM SH. 12 TLDATEN
FROM SH. 12 PBTLDAT-
TLDATA06-
TLDATA07-
43
45
CPSHIFT4-
UAK028
FROM SH. 13 TESTMØDEQ
FROM SH. 13 DIAFAULTQ-
FROM SH. 7 CPK07-
FROM SH. 7 CPK06-
FROM SH 12 CIL-
UBE051
CPX3
CPY3
TØ SH. 12
RØL-
TØ P2 SH. 12
TLADR10-
TLADR11-
10
12
PBUS07-
PBUS06-
+5V
1K
RDE048
SØA
UDK050
RØL
TØ SH. 12
+5V
.047µf
CA2 THRU CA11
CA13 THRU CA21, CB12, CC1, CC12, CC22
CD1, CD12, CD22, CE1, CE12, CE22, CF1
CF12, CF22, CG1, CG12, CG22, CH1, CH12,
CH22, CJ1, CJ12, CJ22, CK1, CK12, CK22
CL1, CL12, CL22, CM1, CM12, CM22, CN12
CP2 THRU CP21
TEXAS INSTRUMENTS
D 96214 2262102 A
9

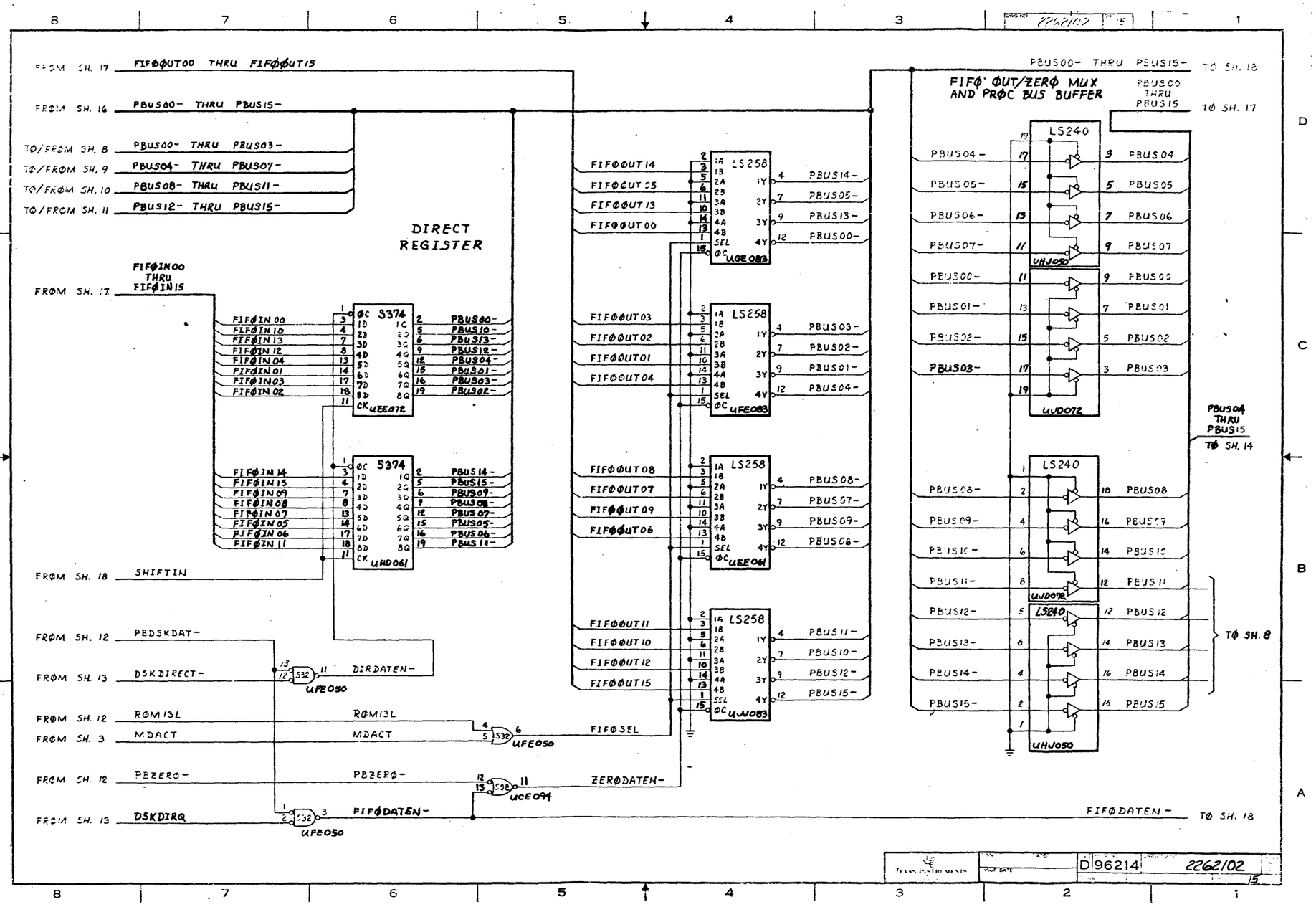

UTC 4-BIT SLICE (8-11)
FROM SH. 6 RØM00 THRU RØM07
FROM SH. 18 STØPFLAG
FROM SH. 16 INDEXMRKQ-
FROM SH. 7 CPK09-
FROM SH. 7 CPK08-
FROM SH. 12 LIR-
FROM SH. 12 CARRY4-
FROM SH. 2 ACCESSØK-
RØM07
RØM06
RØM05
RØM04
RØM03
RØM02
RØM01
FROM SH. 12 PBCPE-
3002
UBE021
PBUS09-
PBUS08-
TLADR12- THRU TLADR15-
TØ SH. 4
CPX4
CPY4
TØ SH. 17
TLADR12-
TLADR13-
P2
PBUS08- THRU PBUS11-
TØ/FROM SH. 15
PBUS09-
PBUS08-
LS243
TLDATA08-
TLDATA09-
TLDATA10-
TLDATA11-
UAE017
FROM SH. 8 CLKSTP-
FROM SH. 4 CLKØN
FROM SH. 4 CLKTI-
LS 20
UBK083
CPRCK-
TØ SH. 11
RØM08
FROM SH. 6 RØM09
LS12 UDK028
RØM09-
LS 132
UCE083
LFBYT-
TØ SH. 12
TØ SH. 7
FROM SH. 12 TLDATEN
FROM SH. 12 PBTLDAT-
CPSHIFT6-
FROM SH. 18 DCRCERRØ-
FROM SH. 14 SPAREØLTQ1
FROM SH. 7 CPK11-
FROM SH. 7 CPK10-
FROM SH. 12 CARRY5-
3002
UCC006
CPX5
CPY5
TØ SH 12
CPSHIFT7-
TØ SH. 11
TLADR14-
TLADR15-
PBUS11-
PBUS10-
D 96214 2262102 A
10

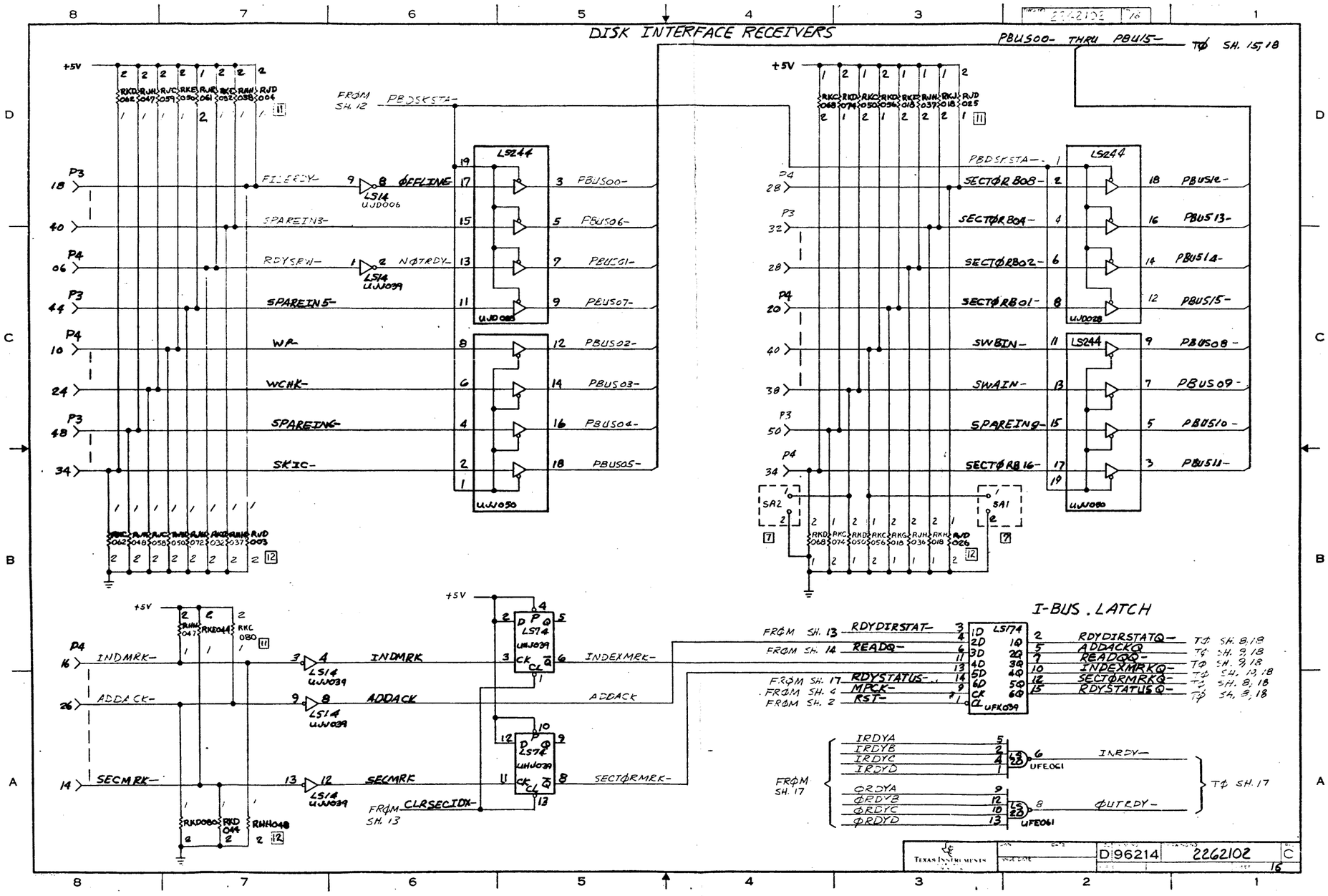

2262102 11
FROM SH. 12 PBTLDAT-
FROM SH. 12 TLDATEN
PBTLDAT-
TLDATEN
LS243 UAK083
PBUS12-
PBUS13-
PBUS14-
PBUS15-
P1
TLDATA12-
TLDATA13-
TLDATA14-
TLDATA15-
+5V
180 RPG037
180 RKE038
P4
SPAREIN1-
SPAREIN2-
LS14 UGE039
LS14 UJJ039
SPAREIN1
SPAREIN2
TO SH. 18
300 RGC037
300 RKD038
UGN047 J1 UGE047
UKC041 J2 UKC038
UTC 4-BIT SLICE (12-15)
PBUS12- THRU PBUS15-
TO/FROM SH. 15
FROM SH. 7 CPK13-
CPK12-
FROM SH. 10 CPSHIFT7-
FROM SH. 12 CARRY6-
ACCESSOK-
FROM SH. 10 CPRCK-
FROM SH. 12 PBCPE-
FROM SH. 17 FIFOOUT19
FIFOOUT18
FROM SH. 7 CPK15-
CPK14-
FROM SH. 6 ROM12
ROM07
ROM06
ROM05
ROM04
ROM03
ROM02
ROM01
ROM01 THRU ROM07
3002I
UBE006
UCC021
CPX6
CPY6
TLADR16-
TLADR17-
PBUS13-
PBUS12-
PBUS15-
PBUS14-
CPSHIFT8-
CPX7
CPY7
ROR-
TLADR18-
TLADR19-
15V
1K RCK028
S04 UDK050
ROR
TO SH. 12
TO SH. 4
TO SH. 5
P2
D 96214 2262/02 C

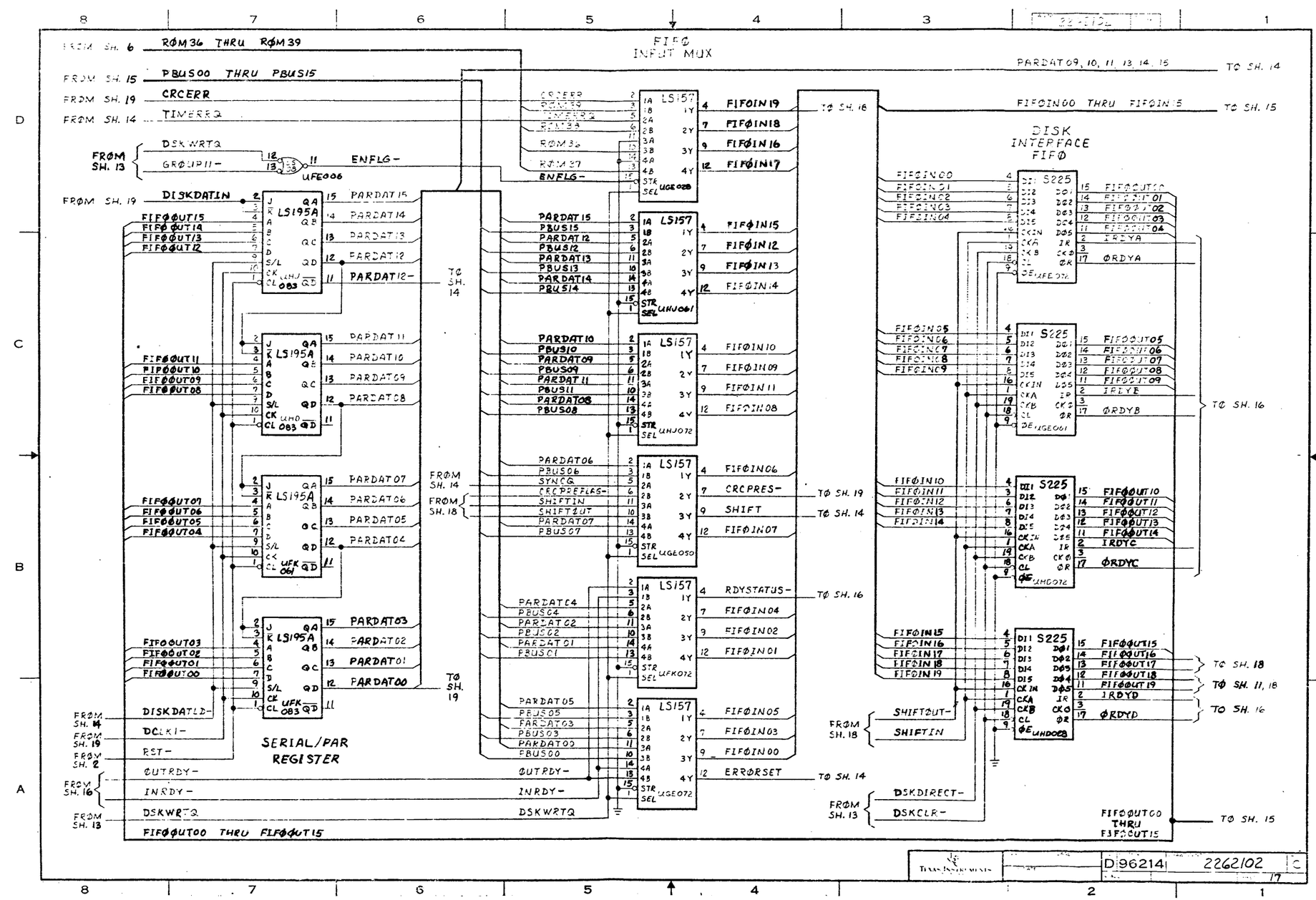

UTC CARRY LØGIC
FRØM SH. 9
FRØM SH. 8
CPY3
CPX3
CPY2
CPX2
CPY1
CPX1
CPY0
CPX0
S182
UAK PØ 050
CARRY2- TØ SH. 9
CARRY1- TØ SH. 8
CARRYØ- TØ SH. 8
CPXL
CPYL
VCC
RTBYT-
S157
UAK061
CPYLA
FRØM SH. 2
RST1-
S74
UBK072
TESTBITQ-
TESTBITQ
TØ SH. 6, 18
MPCK
+5V
TESTBIT-
CIL-
FRØM SH 6
RØM12
FRØM SH. 11
FRØM SH. 10
CPY7
CPX7
CPY6
CPX6
CPY5
CPX5
CPY4
CPX4
UAKPØ 006
CARRY6- TØ SH. 11
CARRY5- TØ SH. 10
CARRY4- TØ SH. 10
CPXR
CPYR
UAE 072
CPXRA
CPYRA
LFBYT-
UAE 072
UAKPØ 072
RØM01
RØM04
RØM05
RØM06
RØM02
RØM03
LS 20
UDE061
UDE 028
SHFTPRE-
SHFCMQ
UCE 072
FRØM SH. 6
RØM01 THRU RØM06
FRØM SH. 9
RØL-
FRØM SH. 11
RØR
RØL
FRØMSH 6
RØM08
RØM09
S153
UDE 050
LIR- TØ SH. 10
RTSHFTRØ
SØURCE AND DESTINATIØN DECØDERS
TLDATEN-
S04
UDK050
TLDATEN
TØ SH. 8, 9, 10, 11
FRØM SH. 6
RØM13, RØM14, RØM15
FRØM SH. 4
CLET1-
FRØM SH. 6
RØM33
RØM21
RØM20
FRØM SH. 3
MDACT-
S373
UFE 028
RØM15
RØM14
RØM13
PØUSENL
RØM15L
RØM14L
RØM13L
S138
UEE 039
PBZERØ- TØ SH. 15
PBCPE- TØ SH. 8, 9, 10, 11
PBTLDAT- TØ SH. 8, 9, 10, 11
PBDSKDAT- TØ SH 15
PBDSKSTA- TØ SH. 16
RØM21L
RØM20L
MPCK-
S139
UNITLØAD- TØ SH. 14
UTCSHIN- TØ SH 18
DSKBUSLD- TØ SH 14
TØ SH. 15
RØM33L
LS14
UAK094
RØM33L-
TØ SH. 2, 18
D 96214 2262102 E
12

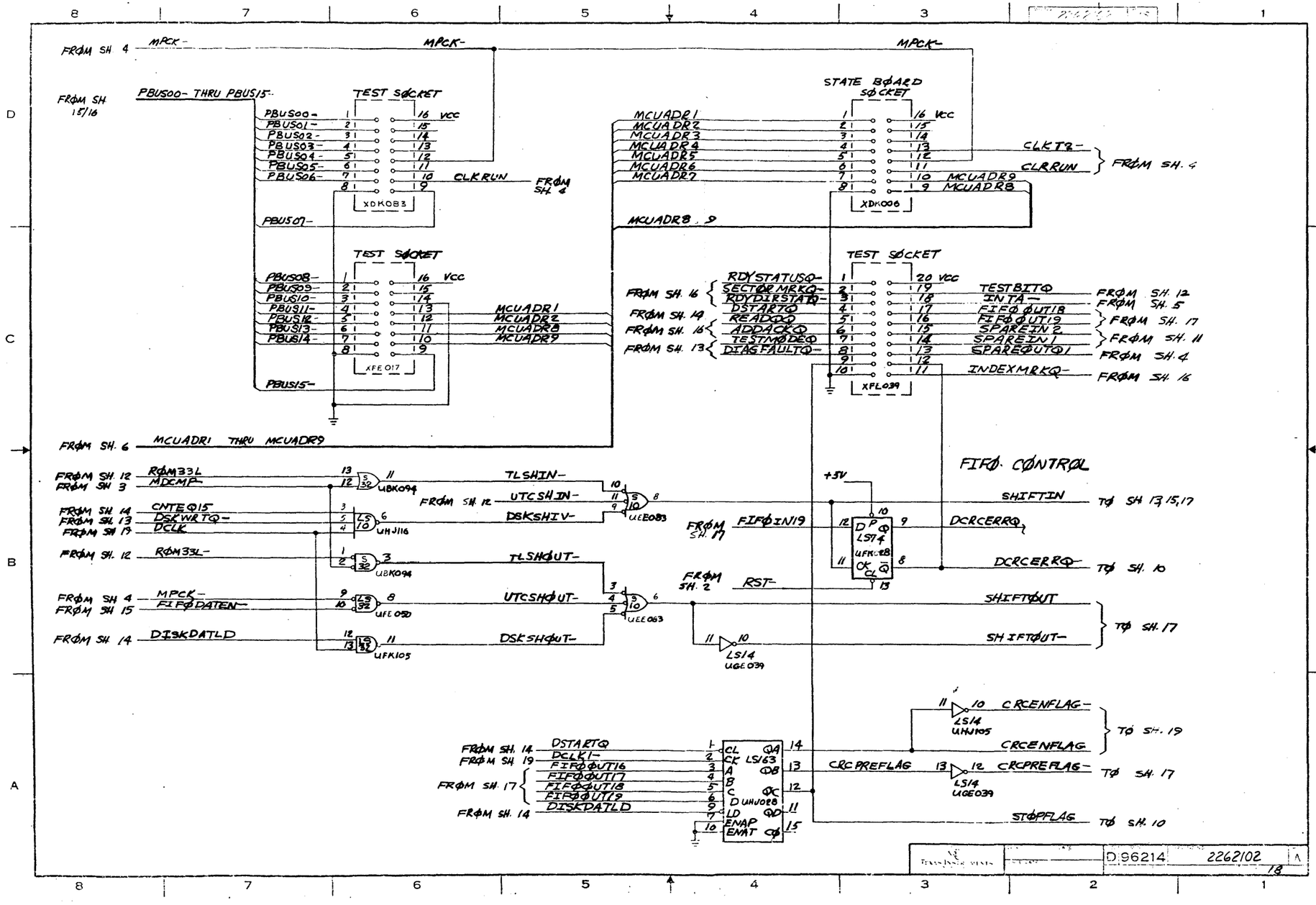

2262102 13
STATUS INDICATORS
SPECIALS DECØDE
RØM32 THRU RØM39
FRØM SH. 6
RØM10
RØM10-
LS14 UDK094
FRØM SH. 4 CLK1I-
FRØM SH. 5 TRAP-
UEE083
ENSPEC-
FRØM SH. 2 RST-
RØM33
RØM32
RØM35
RØM34
S139
UEE050
SLVTRM-
MSTRD-
MSTWRT-
TØ SH. 4
TØ SH. 3
TØ SH. 3
GRØUPØ1-
GRØUPØ-
GRØUP11-
TØ SH. 17
GRØUPØØ-
RØM38
RØM37
RØM36
RØM39
LS138
UJJ072
FRØM SH. 4 MPCK
G2A
G2B
DSKCLR-
DSKSTRRST-
CLRSECIDX-
DSKSTRTCK-
TRIGTMR-
STBCLR-
TØ SH. 14,17
TØ SH. 14
TØ SH. 16
TØ SH. 14
TØ SH. 5
CLKSTPMST-
MSBADRLD-
MSBADRINC-
TØ SH. 4
TØ SH 8
TØ SH 8
UHD050
RDYDIRRST-
LS74
UJD017
RDYDIRSTAT-
TØ SH. 16
FROM SH. 18 SHIFTIN
FRØM SH. 2 RST-
BUSYØ-
BUSYLED-
CRKF104
RKD102
TLINTLED-
CRKF107
RKD104
TLINTØ
TLINTØ-
LS14 UGE039
TLINT-
P2
66
LS259
UFK050
TESTMODEØ
TESTMODE-
DSKDIRØ
BUSYØ-
DIAGFAULTØ-
DSKDIRECT-
DSKWRTØ-
TØ SH. 9, 18, 19
TØ SH. 19
TØ SH. 5, 4, 17, 19
TØ SH. 15
TØ SH. 4
TØ SH. 9, 18, 19
TØ SH. 15, 17
TØ SH. 18, 19
LS14 UGE039
LS14 UHJ105
DIAGFAULTØ-
FAULTØ-
FLED-
FAULTLED-
FLEDR
CRKF113
RKD116
UFK094
UEE105
FRØM SH. 5 CMDTMRDLY-
SPAREØUT1
SPAREØUT2
RESTØRE
RESTØRE-
EG
EG-
WG
WG-
RG
RG-
HDSEL
HDSEL-
ADDSTB
ADDSTB-
TLPRES-
FRØM SH. 2
UJJ061
UJD050
UJJ028
P3
38
12
26
6
22
36
+5V
STBRST-
STBCLR-
INTRST-
FRØM SH. 5
UJJ105
D96214 2262102 D
12

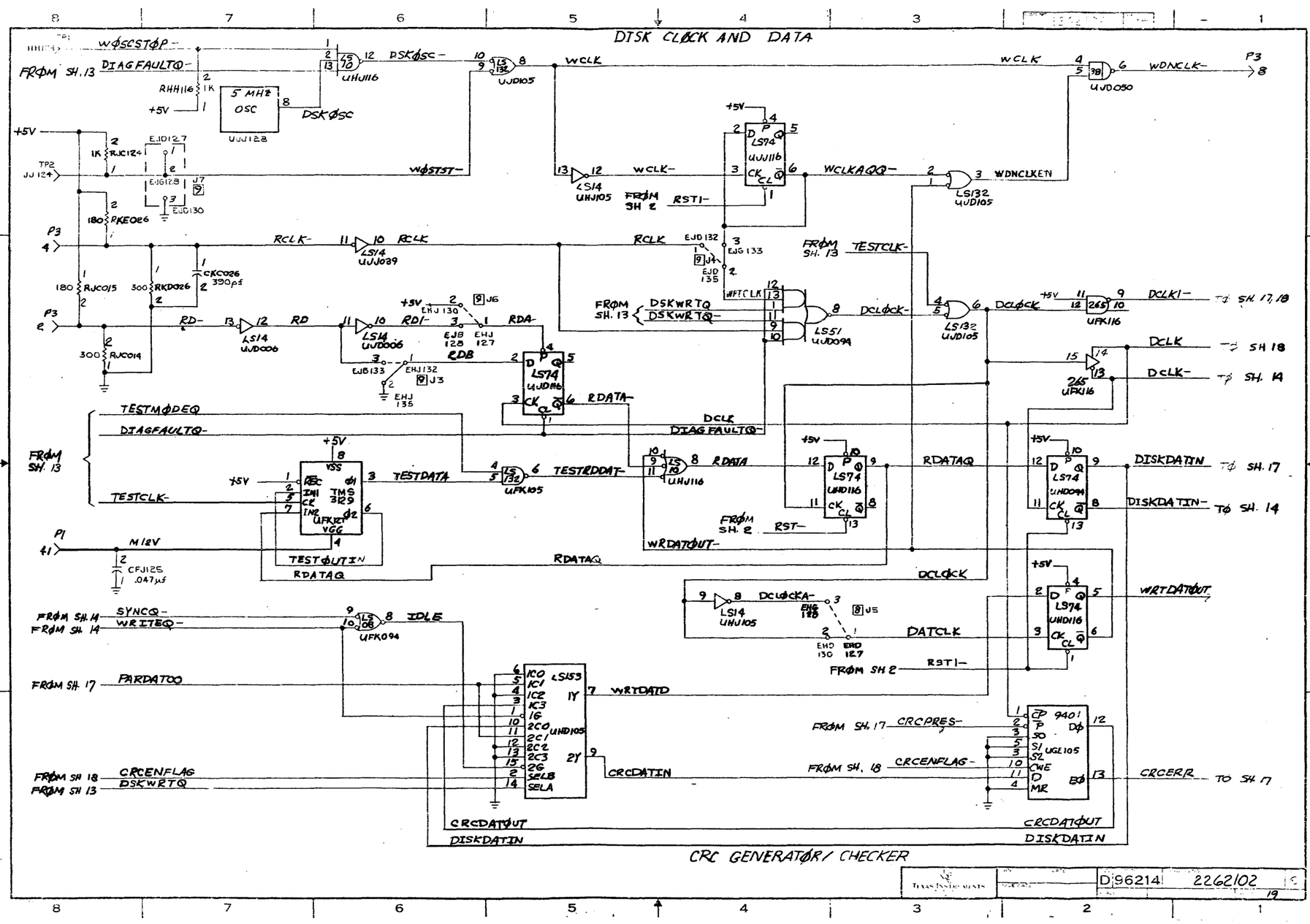

DISK SELECT
DISK ADDRESS REGISTER
FROM SH. 15
PBUS04 THRU PBUS15
PBUS07
FROM SH. 12
DSKBUSLO-
+5V
DBUSHI
ADD256-
ADD032-
ADD001-
ADD008-
ADD002-
ADD016-
ADD064-
ADD128-
ADD004-
PBUS05
PBUS06
PBUS07
PBUS04
UNITLOAD-
RST-
UNITB
UNITA
DISKSEL
SPAREOUT01
SELECTB-
SELECTA-
DISKSEL-
SPAREOUT01-
TO SH. 19/18
PBUS10
PBUS15
PBUS12
PBUS14
PBUS11
PBUS09
PBUS08
PBUS13
ADD032
ADD001
ADD008
ADD002
ADD016
ADD064
ADD128
ADD004
RST-
FROM SH. 19
DISKDATIN-
FROM SH. 17
PARDATIZ-
PARDAT15
PARDAT14
PARDAT13
PARDAT11
PARDAT10
PARDAT09-
PARDAT09
PARDAT09, 10, 11, 13, 14 & 15
STRTREAD-
SYNC6E-
DCLK-
SYNCQ
READQ
READQ-
TO SH. 16
SYNCQ-
TO SH. 19
SYNCQ
TO SH. 17
FROM SH. 19
DCLK-
FROM SH. 13
DSKWRTQ
RST
FROM SH. 2
DSKWRTQ
DSTARTQ-
CLRCNTR-
CNTEQ15
CNTEQ15
TO SH. 18
TO SH. 8, 18
DSKSTRQ
DSKSTRQ-
FROM SH. 13
DSKSTRTCK-
DSKSTRRST-
INTRST-
RST-
DSKCLR-
DSKSTRTZ-
WRITEQ-
WRITEQD
WRITEQ
WRITEQ-
TO SH. 19
DISKDATLD-
TO SH. 17, 18
DISKDATLD
TO SH. 18
FROM SH. 17
ERRORSET
SHIFT
TIMERRQ
TO SH. 5, 17
TIMERRQ-
DISK DATA READ/WRITE CONTROL
D 96214 2262102 C
14


FROM SH. 17 FIFØOUT00 THRU FIFØOUT15
FROM SH. 16 PBUS00- THRU PBUS15-
TØ/FROM SH. 8 PBUS00- THRU PBUS03-
TØ/FROM SH. 9 PBUS04- THRU PBUS07-
TØ/FROM SH. 10 PBUS08- THRU PBUS11-
TØ/FROM SH. 11 PBUS12- THRU PBUS15-
DIRECT REGISTER
FIFØIN00 THRU FIFØIN15
FROM SH. 17
FIFØIN 00
FIFØIN 10
FIFØIN 13
FIFØIN 12
FIFØIN 04
FIFØIN 01
FIFØIN 03
FIFØIN 02
S374
UEE072
PBUS00-
PBUS10-
PBUS13-
PBUS12-
PBUS04-
PBUS01-
PBUS03-
PBUS02-
FIFØIN 14
FIFØIN 15
FIFØIN 09
FIFØIN 08
FIFØIN 07
FIFØIN 05
FIFØIN 06
FIFØIN 11
UHD061
PBUS14-
PBUS15-
PBUS09-
PBUS08-
PBUS07-
PBUS05-
PBUS06-
PBUS13-
FROM SH. 18 SHIFTIN
FROM SH. 12 PBDSKDAT-
FROM SH. 13 DSKDIRECT-
532
UFE050
DIRDATEN-
FROM SH. 12 RØMI3L
FROM SH. 3 MDACT
RØMI3L
MDACT
FIFØSEL
FROM SH. 12 PBZERØ-
PBZERØ-
UCE094
ZERØDATEN-
FROM SH. 13 DSKDIRQ
FIFØDATEN-
FIFØOUT14
FIFØOUT05
FIFØOUT13
FIFØOUT00
FIFØOUT03
FIFØOUT02
FIFØOUT01
FIFØOUT04
FIFØOUT08
FIFØOUT07
FIFØOUT09
FIFØOUT06
FIFØOUT11
FIFØOUT10
FIFØOUT12
FIFØOUT15
LS258
UGE083
UFE083
UHD061
UWJ083
PBUS14-
PBUS05-
PBUS13-
PBUS00-
PBUS03-
PBUS02-
PBUS01-
PBUS04-
PBUS08-
PBUS07-
PBUS09-
PBUS06-
PBUS11-
PBUS10-
PBUS12-
PBUS15-
PBUS00- THRU PBUS15- TØ SH. 18
FIFØ OUT/ZERØ MUX AND PRØC BUS BUFFER
PBUS00 THRU PBUS15 TØ SH. 17
LS240
UHJ050
UVD072
PBUS04 THRU PBUS15 TØ SH. 14
TØ SH. 8
FIFØDATEN- TØ SH. 18
TEXAS INSTRUMENTS
D 96214
2262102
SHEET 5


DISK INTERFACE RECEIVERS
PBUS00- THRU PBUS15-
TO SH. 15, 18
FROM SH. 12 PBDSKSTA-
+5V
FILERDY-
SPAREIN3-
RDYSRW-
SPAREIN5-
WR-
WCHK-
SPAREIN6-
SKIC-
OFFLINE
NOTRDY-
INDMRK-
ADDACK-
SECMRK-
INDMRK
ADDACK
SECMRK
INDEXMRK-
SECTORMRK-
FROM SH. 13 CLRSECIDX-
SECTOR B08-
SECTOR B04-
SECTOR B02-
SECTOR B01-
SWBIN-
SWAIN-
SPAREIN9-
SECTOR B16-
I-BUS . LATCH
FROM SH. 13 RDYDIRSTAT-
FROM SH. 14 READDQ-
FROM SH. 17 RDYSTATUS-
FROM SH. 6 MPCK-
FROM SH. 2 RST-
RDYDIRSTATQ-
ADDACKQ
READDQ0-
INDEXMRKQ-
SECTORMRKQ-
RDYSTATUSQ-
IRDYA
IRDYB
IRDYC
IRDYD
QRDYA
QRDYB
QRDYC
QRDYD
INRDY-
QUTRDY-
FROM SH. 17
TO SH. 17
LS244
LS14
LS74
LS174
UJJ039
UJJ050
UJJ080
UJJ088
UFK039
UFE061
SA1
SA2
D96214
2262102


FIFO INPUT MUX
DISK INTERFACE FIFO
SERIAL/PAR REGISTER
FROM SH. 6 ROM36 THRU ROM39
FROM SH. 15 PBUS00 THRU PBUS15
FROM SH. 19 CRCERR
FROM SH. 14 TIMERRQ
FROM SH. 13 DSKWRTQ, GROUP11-
UFE006
FROM SH. 19 DISKDATIN
FIFOOUT15
FIFOOUT14
FIFOOUT13
FIFOOUT12
FIFOOUT11
FIFOOUT10
FIFOOUT09
FIFOOUT08
FIFOOUT07
FIFOOUT06
FIFOOUT05
FIFOOUT04
FIFOOUT03
FIFOOUT02
FIFOOUT01
FIFOOUT00
LS195A
UFK 083
UHJ 083
PARDAT15
PARDAT14
PARDAT13
PARDAT12
PARDAT11
PARDAT10
PARDAT09
PARDAT08
PARDAT07
PARDAT06
PARDAT05
PARDAT04
PARDAT03
PARDAT02
PARDAT01
PARDAT00
TO SH. 14
TO SH. 19
FROM SH. 14 DISKDATLD-
FROM SH. 19 DCLK1-
FROM SH. 2 RST-
FROM SH. 16 OUTRDY-, INRDY-
FROM SH. 13 DSKWRTQ
FIFOOUT00 THRU FIFOOUT15
LS157
UGE028
UHJ061
UHJ072
UFK072
UGE050
UGE072
FIFOIN19
FIFOIN18
FIFOIN16
FIFOIN17
FIFOIN15
FIFOIN12
FIFOIN13
FIFOIN14
FIFOIN10
FIFOIN11
FIFOIN09
FIFOIN08
FIFOIN06
FIFOIN07
FIFOIN04
FIFOIN02
FIFOIN01
FIFOIN05
FIFOIN00
CRCPRES-
SHIFT
RDYSTATUS-
ERRORSET
TO SH. 19
TO SH. 14
TO SH. 16
PARDAT09, 10, 11, 13, 14, 15 TO SH. 14
FIFOIN00 THRU FIFOIN15 TO SH. 15
S225
UHD028
UHD072
IRDYA
ORDYA
IRDYB
ORDYB
IRDYC
ORDYC
IRDYD
ORDYD
TO SH. 16
FROM SH. 18 SHIFTOUT-, SHIFTIN
FROM SH. 13 DSKDIRECT-, DSKCLR-
TO SH. 18
TO SH. 11, 18
TO SH. 16
FIFOOUT00 THRU FIFOOUT15 TO SH. 15
TEXAS INSTRUMENTS
D 96214 2262102 C
17


FROM SH 4 MPCK-
MPCK-
MPCK-
FROM SH 15/16
PBUS00- THRU PBUS15-
TEST SOCKET
PBUS00-
PBUS01-
PBUS02-
PBUS03-
PBUS04-
PBUS05-
PBUS06-
CLKRUN
FROM SH 4
XDK083
PBUS07-
TEST SOCKET
PBUS08-
PBUS09-
PBUS10-
PBUS11-
PBUS12-
PBUS13-
PBUS14-
XFE017
PBUS15-
MCUADR1
MCUADR2
MCUADR3
MCUADR9
FROM SH 6 MCUADR1 THRU MCUADR9
STATE BOARD SOCKET
MCUADR1
MCUADR2
MCUADR3
MCUADR4
MCUADR5
MCUADR6
MCUADR7
CLKT2-
CLRRUN
FROM SH. 4
MCUADR9
MCUADR8
XDK006
MCUADR8 . 9
TEST SOCKET
RDYSTATUSQ-
SECTORMRKQ-
RDYDIRSTATQ-
DSTARTQ
READQQ
ADDACKQ
TESTMODEQ
DIAGFAULTQ-
FROM SH. 16
FROM SH. 14
FROM SH. 16
FROM SH. 13
XFL039
TESTBITQ
INTA-
FIFOOUTI8
FIFOOUTI9
SPAREIN2
SPAREIN1
SPAREQUTQ1
INDEXMRKQ-
FROM SH. 12
FROM SH. 5
FROM SH. 17
FROM SH. 11
FROM SH. 4
FROM SH. 16
FIFO CONTROL
+5V
SHIFTIN
TO SH 13,15,17
FROM SH. 17 FIFOIN19
DCRCERRQ
DCRCERRQ-
TO SH. 10
FROM SH. 2 RST-
SHIFTOUT
SHIFTOUT-
TO SH. 17
LS14 UGE039
CRCENFLAG-
LS14 UHJ105
CRCENFLAG
TO SH. 19
CRCPREFLAG
CRCPREFLAG-
TO SH. 17
LS14 UGE039
STOPFLAG
TO SH. 10
FROM SH. 12 RQM33L
FROM SH 3 MDCMP-
FROM SH. 14 CNTEQ15
FROM SH. 13 DSKWRTQ-
FROM SH 19 DCLK
FROM SH. 12 RQM33L-
FROM SH 4 MPCK-
FROM SH 15 FIFODATEN-
FROM SH. 14 DISKDATLD
UBK094
UHJ116
UBK094
UFE050
UFK105
TLSHIN-
UTCSHIN-
DSKSHIV-
TLSHOUT-
UTCSHOUT-
DSKSHOUT-
UEE083
UEE063
FROM SH. 14 DSTARTQ
FROM SH 19 DCLK1-
FROM SH. 17 FIFOOUTI6
FIFOOUTI7
FIFOOUTI8
FIFOOUTI9
FROM SH. 14 DISKDATLD
LS163
UHJ088
ENAP
ENAT
D 96214
2262102
A
18


DISK CLOCK AND DATA
WØSCSTØP-
FROM SH. 13 DIAGFAULTØ-
RHH116 1K
5 MHz OSC
UJJ128
DSKØSC
UHJ116
DSKØSC-
UJD105
WCLK
WCLK
UJD050
WDNCLK-
P3 8
+5V
1K RJC124
EJD127
TP2 JJ124
EJD128
J7
EJD130
WØSTST-
180 RKE026
LS14 UHJ105
WCLK-
LS74 UJJ116
WCLKAQQ-
LS32 UJD105
WDNCLKEN
FROM SH 2 RSTI-
P3 4
RCLK-
LS14 UJJ039
RCLK
EJD132
EJG133
J4
EJD135
FROM SH. 13 TESTCLK-
180 RJC015
300 RKD026
CKC026 330pf
P3 2
RD-
LS14 UJD006
RD
RDI-
RDA
+5V EHJ130 J6
EJB128 EHJ127
EDB
EJB133
EHJ132
J3
EHJ135
#FTCLK
FROM SH. 13 DSKWRTQ
DSKWRTQ-
LS51 UJD094
DCLØCK-
LS32 UJD105
DCLØCK
+5V
265 UFK116
DCLK1-
TO SH. 17, 19
DCLK
TO SH 18
DCLK-
TO SH. 14
300 RJC014
TESTMØDEQ
DIAGFAULTQ-
DCLK
DIAGFAULTQ-
FROM SH. 13
+5V
TESTDATA
TESTCLK-
TMS 3129
UFK127
VGG
TESTDDAT-
LS 132
UFK105
RDATA
UHJ116
RDATAQ
LS74 UHD116
DISKDATIN
TO SH. 17
DISKDATIN-
TO SH. 14
FROM SH. 2 RST-
WRDATØUT-
P1 41
M12V
CFJ125 .047µf
TESTØUTIN
RDATAQ
DCLOCK
WRTDATØUT
DCLOCKA-
LS14 UHJ105
EHD130 EHD127
J5
DATCLK
FROM SH 2 RSTI-
FROM SH 14 SYNCQ-
FROM SH 14 WRITEQ-
LS08 UFK094
IDLE
FROM SH 17 PARDATOO
LS153 UHD105
WRTDATD
FROM SH 17 CRCPRES-
9401 UGL105
FROM SH. 18 CRCENFLAG-
CRCDATIN
FROM SH 18 CRCENFLAG
FROM SH 13 DSKWRTQ
CRCDATØUT
DISKDATIN
CRCERR
TO SH 17
CRC GENERATØR/ CHECKER
TEXAS INSTRUMENTS
D96214 2262102
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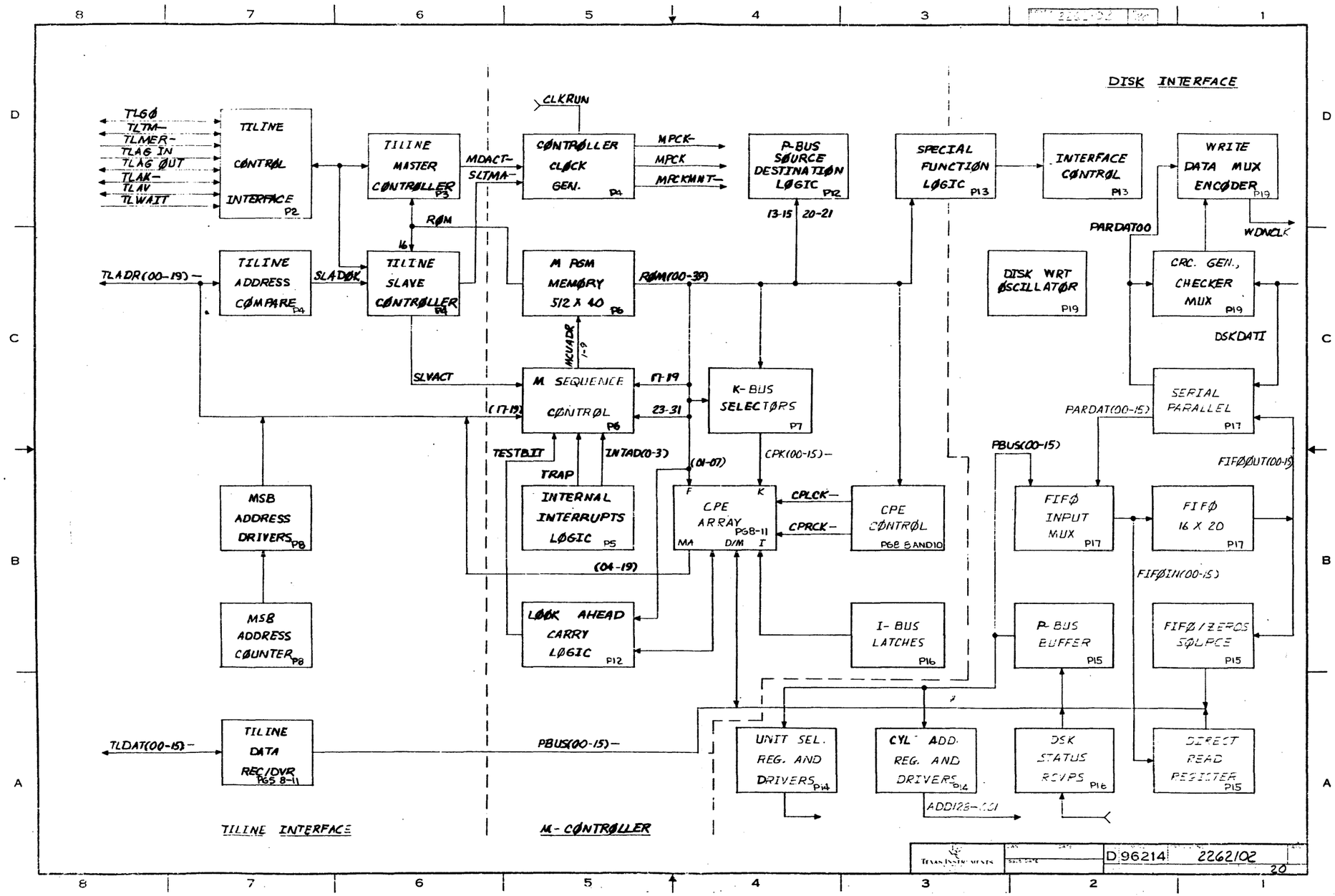
DISK INTERFACE
TLGØ
TLTM-
TLMER-
TLAG IN
TLAG ØUT
TLAK-
TLAV
TLWAIT
TILINE CONTRØL INTERFACE P2
TILINE MASTER CONTRØLLER P3
CLKRUN
CONTRØLLER CLØCK GEN. P4
MPCK-
MPCK
MRCKMNT-
P-BUS SØURCE DESTINATIØN LØGIC P12
13-15
20-21
SPECIAL FUNCTIØN LØGIC P13
INTERFACE CØNTRØL P13
WRITE DATA MUX ENCØDER P19
WDWCLK
PARDAT00
MDACT-
SLTMA-
RØM
16
TLADR(00-19)-
TILINE ADDRESS CØMPARE P4
SLADØK
TILINE SLAVE CØNTRØLLER P4
M PSM MEMØRY 512 X 40 P6
RØM(00-39)
DISK WRT ØSCILLATØR P19
CRC. GEN., CHECKER MUX P19
DSKDATI
INCVADR 1-9
SLVACT
M SEQUENCE CØNTRØL P6
(17-19)
23-31
K-BUS SELECTØRS P7
SERIAL PARALLEL P17
PARDAT(00-15)
(17-19)
TESTBIT
TRAP
INTAD(0-3)
(01-07)
CPK(00-15)-
PBUS(00-15)
FIFØØUT(00-15)
MSB ADDRESS DRIVERS P8
INTERNAL INTERRUPTS LØGIC P5
F
K
CPE ARRAY P68-11
MA
D/M
I
CPLCK-
CPRCK-
CPE CØNTRØL P68 & AND10
FIFØ INPUT MUX P17
FIFØ 16 X 20 P17
FIFØIN(00-15)
(04-19)
MSB ADDRESS CØUNTER P8
LØØK AHEAD CARRY LØGIC P12
I-BUS LATCHES P16
P-BUS BUFFER P15
FIFØ/ZEROS SØURCE P15
TLDAT(00-15)-
TILINE DATA REC/DVR P65 8-11
PBUS(00-15)-
UNIT SEL. REG. AND DRIVERS P14
CYL ADD. REG. AND DRIVERS P14
ADD128-(01
DSK STATUS RGVPS P16
DIRECT READ REGISTER P15
TILINE INTERFACE
M-CØNTRØLLER
D96214
2262102
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0	1 7	8 9	10 11	12	13 15	16	17 19	20 21	22 31	32 33	34 35	36 39
CLKSTP	FUNCTIØN	WS	KC	CI	SØURCE	ENSLV	BRANCH	DEST	NRA	IMMEDIATE		
							CO=0/CO=1			TILINE DP	SPECIAL GRØUP	SPECIAL FUNCTIØN
000	NØP	WØRD	F'S→K ENSP	1→CI	ØDDØ	NØP	RA+1→RA	NØP	NCP			
001	CLKSTP	RT SHFD WD	Ø'S→K ENSP	Ø→CI	CPE	ENSLV	NRA →RA	UNITLØAD	SLVTRM			
010		LEFT BYTE	IM →K		EXTERNAL		RA+1→RA/NRA→RA	FIFØ	MSTRD			
011		RIGHT BYTE	IM →K		TILINE		NRA→RA, RA+1→RA	CYL ADDR	MSTWRT			
100					DSKDATA		NRA→RA/RA+1→STACK					
101							NRA→RA/STACK→RA					
110					DSKSTATUS		STACK→RA/NRA→RA					
111							STACK→RA					

RØM 36 37 38 39	RØM 34, 35 00	01	10
0000	NØP	RST TESTMØDE	RST SPAREØUT1
0001	CLK STØP MAST	SET TESTMØDE	SET SPAREØUT1
0010	CLR DSK I/F	SET TESTCLK	RST RESTØRE
0011	MSB ADR LD	RST TESTCLK	SET RESTØRE
0100	STØP I/F CØNT.	RST I/F WRT	RST ERASE
0101	MSB ADR INC	SET I/F READ	SET ERASE
0110	CLR SECT/INDX	RST DIRECT MØDE	RST W.G.
0111	NØP	SET DIRECT MØDE	SET W.G.
1000	START I/F CØNT.	RST TL. INT	RST READ
1001	NØP	SET TL. INT	SET READ
1010	TRIGER TIMER	SET BUSY	RST SPAREØUT2
1011	NØP	RST BUSY	SET SPAREØUT2
1100	RST DIR. READY	SET FAULT	RST HEADSEL
1101	NØP	RST FAULT	SET HEADSEL
1110	CLR DISK CØNT.	SET DIAG FAULT	RST ADDSTB
1111	NØP	RST DIAG FAULT	SET ADDSTB

RØM 34 35	RØM 36–39
11	BIT 36 SET(ØNE) CAUSES CRC TØ BE ENABLED ØUT TØ DISK
11	BIT 37 SET(ØNE) CAUSES THE CRC CHARACTER GENERATØR TØ BE SET TØ A STATE ØF ALL ØNES
11	BIT 38 SET(ØNE) ENABLES A SPECIAL FLAG BIT TØ BE LØADED INTØ FIFØ TØ ALLØW THE LØNTRØLLER TØ DETECT WHEN A STØP CØNDITIØN IS PRESENT
11	BIT 39 IS AN UNUSED SPARE FLAG BIT

MICRØCØDE FIELD DEFINITIØNS

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
R0	SE I. ATN MSK 0 1 2 3
R1	T.I. COMMAND SECTØRS/RECØRD
R2	SECTØRS/RECØRD DIAG. ERRØR # / SECTØR ADDRESS
R3	HD. CYLINDER / FØRMAT WØRD
R4	TILINE WØRD CØUNT(2'S CØMPL.)
R5	TILINE ADDRESS(04-19)
R6	UNIT SEL. 0 1 2 3 / TILINE ADR. 00-03
R7	IDL COM FER INT LØ Ø Ø AC ME DE TT IE RE CT SE UE
R8	RECØRD WØRD CØUNT
R9	TEST CØMPLETIØN CØUNT / RECØRD WØRD CØUNT(2'S CØMPL.)
T	GENERAL UTILITY
AC	GENERAL UTILITY

H: SECTØR- · RDYSTATUS · STARTØ- · RDYDIRSTAT · ADDRACK- · READØ · DIAGFAULTQ · TESTMØDEQ- · INDEX · STØPFLAG- · SPAREØUTI- · DCRCERRQ · SPARE IN2- · SPARE INI- · FIFØØUTM- · FIFØØUT19-

BIT PØSITIØN	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
ZERØS	Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø
CPE	CPE ARRAY ØUTPUT (ACØ)
EXTERNAL	FLØAT
TILINE	TILINE DATA 00-15
DISK DATA	(DIRECT DATA) DISK DATA (FIFØ ØUTPUT)

PBUS SØURCE — DISK STATUS: ØFFLINE · NØT READY · WRTPRØT · UNSAFE · SPARE IN6 · SEEKINC · SPARE IN3 · SPARE IN5 · SWB · SWA · SPARE IN4 · SECTØR 16 · SECTØR 8 · SECTØR 4 · SECTØR 2 · SECTØR 1

PBUS DESTINATIØN — NØNE · NØP · UNIT · SPARE SELB · SELA · DSKSEL · FIFØ · FIFØ INPUT 00-15 · CYL. ADD. · ADD256 · ADD128 · ADD064 · ADD032 · ADD016 · ADD008 · ADD004 · ADD002 · ADD001

TEXAS INSTRUMENTS — D 96214 2262102 — 21

MICRO-FUNCTION SUMMARY

STEP	F-GROUP	R-GROUP	MICRO-FUNCTIONS
1		I	$R_N+(AC\wedge K)+CI \rightarrow R_N \cdot AC$
2	0	II	$M+(AC\wedge K)+CI \rightarrow AT$
3		III	$AT_L\wedge(\overline{I_L\wedge K_L})\rightarrow RO \quad LI\vee[(I_H\wedge K_H)\wedge AT_H]\rightarrow AT_H$ $[AT_L\wedge(I_L\wedge K_L)]\vee[AT_H\vee(I_H\wedge K_H)]\rightarrow AT_L$
4		I	$K\vee R_N \rightarrow MAR \quad R_N+K+CI\rightarrow R_N$
5	1	II	$K\vee M \rightarrow MAR \quad M+K+CI\rightarrow AT$
6		III	$(\overline{AT}\vee K)+(AT\wedge K)+CI \rightarrow AT$
7		I	$(AC\wedge K)\cdot 1+CI\rightarrow R_N$
8	2	II	$(AC\wedge K)\cdot 1+CI\rightarrow AT$ } SEE NOTE (1)
9		III	$(I\wedge K)\cdot 1+CI\rightarrow AT$
10		I	$R_N+(AC\wedge K)+CI\rightarrow R_N$
11	3	II	$M+(AC\wedge K)+CI\rightarrow AT$
12		III	$AT+(I\wedge K)+CI\rightarrow AT$
13		I	$CI\vee(R_N\wedge AC\wedge K)\rightarrow CO \quad R_N\wedge(AC\wedge K)\rightarrow R_N$
14	4	II	$CI\vee(M\wedge AC\wedge K)\rightarrow CO \quad M\wedge(AC\wedge K)\rightarrow AT$
15		III	$CI\vee(AT\wedge I\wedge K)\rightarrow CO \quad AT\wedge(I\wedge K)\rightarrow AT$
16		I	$CI\vee(R_N\wedge K)\rightarrow CO \quad K\wedge R_N\rightarrow R_N$
17	5	II	$CI\vee(M\wedge K)\rightarrow CO \quad K\wedge M\rightarrow AT$
18		III	$CI\vee(AT\wedge K)\rightarrow CO \quad K\wedge AT\rightarrow AT$
19		I	$CI\vee(AC\wedge K)\rightarrow CO \quad R_N\vee(AC\wedge K)\rightarrow R_N$
20	6	II	$CI\vee(AC\wedge K)\rightarrow CO \quad M\vee(AC\wedge K)\rightarrow AT$
21		III	$CI\vee(I\wedge K)\rightarrow CO \quad AT\vee(I\wedge K)\rightarrow AT$
22		I	$CI\vee(R_N\wedge AC\wedge K)\rightarrow CO \quad R_N\,\bar{\oplus}\,(AC\wedge K)\rightarrow R_N$
23	7	II	$CI\vee(M\wedge AC\wedge K)\rightarrow CO \quad M\,\bar{\oplus}\,(AC\wedge K)\rightarrow AT$
24		III	$CI\vee(AT\wedge I\wedge K)\rightarrow CO \quad AT\,\bar{\oplus}\,(I\wedge K)\rightarrow AT$

NOTES:
1. 2'S COMPLEMENT ARITHMETIC ANDS III...II TO PERFORM SUBTRACTION OF 000...01.
2. R_N INCLUDES T AND AC AS SOURCE AND DESTINATION REGISTERS IN F-GROUP 1 MICRO-FUNCTIONS.
3. STANDARD ARITHMETIC ARRY OUTPUT VALUES ARE GENERATED IN F-GROUP 0, 1, 2 AND 3 INSTRUCTIONS.

LEGEND

SYMBOL	MEANING
I, K, M	DATA ON THE I, K, AND M BUSES, RESPECTIVELY
CI, LI	DATA ON THE CARRY INPUT AND LEFT INPUT, RESPECTIVELY
CO, RO	DATA ON THE CARRY OUTPUT AND RIGHT OUTPUT, RESPECTIVELY
R_N	CONTENTS OF REGISTER N INCLUDING T AND AC (R-GROUP 1)
AC	CONTENTS OF THE ACCUMULATOR
AT	CONTENTS OF AC OR T, AS SPECIFIED
MAR	CONTENTS OF THE MEMORY ADDRESS REGISTER
+	2'S COMPLEMENT ADDITION
$\wedge$	LOGICAL AND
$\vee$	LOGICAL OR
$\bar{\oplus}$	EXCLUSIVE NOR
$\rightarrow$	DEPOSIT INTO

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SLAVES

	READ ADRS.	WRITE ADRS
SLAVE Ø	ØFØ	ØF8
SLAVE 1	ØF1	ØF9
SLAVE 2	ØF2	ØFA
SLAVE 3	ØF3	ØFB
SLAVE 4	ØF4	ØFC
SLAVE 5	ØF5	ØFD
SLAVE 6	ØF6	ØFE
SLAVE 7	ØF7	ØFF

TRAPS

TRAP ADRS.	DESCRIPTION
ØØØ	TLABØRTG- (I/Ø RESET, PFWP, TLPRES)
010	MDTØG- (TILINE TIMEØUT)
020	TLERRQ- (MEMORY PARITY ERROR)
030	CLRWRTQ- (RATE ERROR)
040	CMDTMRQ- (COMMAND TIMER)

D 96214 2262102

DWG NO 937515 SH 1

NOTES: UNLESS OTHERWISE SPECIFIED:

1. P1 AND P2 MUST BE CRIMPED TO THE FLAT UNTWISTED AREAS OF THE CABLE (ITEM 2)
2. MATERIAL (ITEM 2) INITIAL CUT TO BE AT CENTER OF 2 INCH FLAT SECTION, OVERALL LENGTH TO BE AS SHOWN IN DIMENSIONAL TABLE. DIMENSION "A" IS NOMINAL AND IS FOR REFERENCE ONLY
3. ITEM 101 IN -0001, -0002 & -0003 LMS CONSISTS OF BULK CABLE ASSEMBLY MATERIAL.

REVISIONS

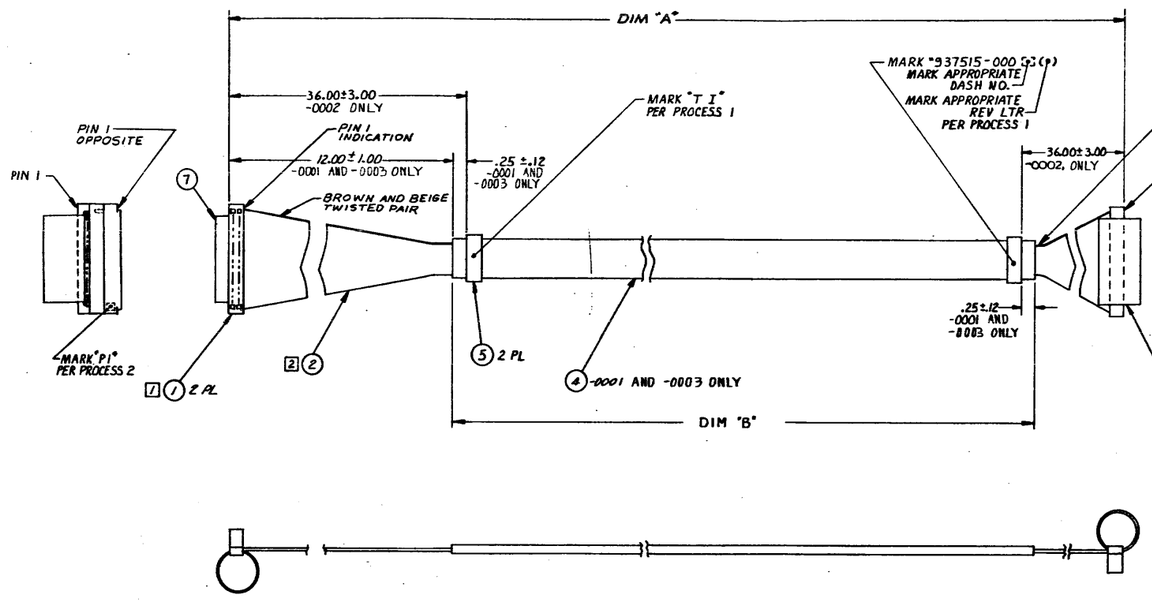
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	K	CN464121 (D) ~~[illegible]~~ (1) CREATED -0003 -5003 LMS & ADDED RESP COLUMNS TO PN BLOCK (2) ADDED NHA 226802 5 - PROJ 7068 (3) ADDED -0003 TO NOTE 3 & DIM 36.00±6 DC IN ZC-4,7 (4) ADDED 3 TO -3003 IN PN BLOCK	2-28-78	

REV CONT SH 2 ZD1-2

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	CN 424809 (C) [illegible] REVISED PER EXTENSIVE ENGR CHANGES	1.9.78	
B	CN424814.C [illegible] ITEMS 2&4 QTY WAS 5.5 & 11.5 RESP2: TITLE DESCRIPTION WAS "5 FT CA LM(3) DIM AB & C CN-0001 WAS 180.00±6.00 80.00±6.00 & 240.00±12.00 RESP	3-15-78	
C	CN 440480 (C) [illegible] (1) CHANGED PRESENTATION OF P1 & P2 TO SHOW SLOT (2) REVERSED TRIANGLE ON P1, REMOVED TRIANGLE ON P2 (3) ADDED PROJECTION OF P1 & P2.	7-26-78	
D	CN430778 (C) [illegible] (1)-0001 LM, ITEM 3 PN NAS417177-2	11-13-78	
E	CN446556 (E) [illegible] (1) REVISED PER EXTENSIVE ENGR CHANGES	4-6-79	E. Wray
F	CN448358 (C) [illegible] (1) REVISED PICT @ B-7, C-1, C-8 ROTATED CONNECTOR	5-10-79	E. Wray
G	CN 437441 (C) D. Edwards (1) CREATED -5001 & -5002 LMS (2) ADDED ITEM 101 TO -5001, -5002 (3) ADDED NOTE 3, (4) ADDED PART NUMBER TO BLOCK	10-3-79	E. Wray
H	CN 448377 (E) D. Edwards (1) DELEATED ITEMS 3 AND 6, LM-5001 (2) LM-5001 ITEM 4 WAS 972435-0003	10-3-79	E. Wray 6
J	CN 447468 (C) D. Edwards (1) ADDED DIMENSION 192.00±6.00 -0001 ONLY IN ZONE B5 (2) ADDED -0002 ONLY TO DIMENSION 36.00±3.00 IN ZONE C4.	10-3-79	E. Wray

(REV CONT ZD-4)



937515-5003	BULK CABLE ASSY MAT'L FOR -0003	——	——
937515-5002	BULK CABLE ASSY MAT'L FOR -0002	——	——
937515-5001	BULK CABLE ASSY MATERIAL FOR -0001	——	——
3 937515-0003	CABLE ASSY, 40 PIN, 10 FT	120.00±6.00	72.00 ± 6.00
3 937515-0002	CABLE ASSY, 40 PIN, 6 FT	80.00±6.00	——
3 937515-0001	CABLE ASSY, 40 PIN, 20 FT	240.00±12.00	192.00 ± 6.00
PART NUMBER	DESCRIPTION	DIM "A" 2	DIM "B"

REV STATUS	REV	M	M
OF SHEETS	SHEET	1	2

SEQ NO	IDENT	PROCESS	NO	ADDITIONAL SPECIFICATION	NOTES
2	MARK	100-02	21	HGT 12 CLR WHT	
1	MARK	100-07	712	CLR BLACK TYPE 6	

PROCESSED — FOR CORRELATION TO GOVT/IND SPECIFICATIONS, SEE TI DRAWING 1C9467

PARTS LIST

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
2268025	7068				
937500	7506				
NEXT ASSY	USED ON				
APPLICATION					

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125 + .004 - .001	.126 THRU .250 + .005 - .001	.251 THRU .500 + .006 - .001	
.501 THRU .750 + .008 - .001	.751 THRU 1.000 + .010 - .001	1.001 THRU 2.000 + .012 - .001	

Dwn GMALCETTE 3/16/77
Ck [illegible] 5-11-77
Engr [illegible] 5-19-77
Mech [illegible] 5-17-77
Qa [illegible]
Contr [illegible]
Rlse Tony Bailey 3/19/77

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

CABLE ASST, 40 PIN

SIZE D | FSCM NO 96214 | DRAWING NO 937515

SCALE 1/1 | SHEET 1 OF 2

DWG NO	SH
937515	2

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	L	CN43E775 (D) SH1 Z-27 WAS 36.[illegible]3.00 -5002, -0002 ONLY: 18.03 ± 1.003 -0001 ONLY: 12.5 ±.12 -0001 ONLY (2) SH1 ZC-6 ITEM 4 WAS -[illegible] ONLY (3) SH Z B-[illegible] WAS [illegible] ± 6.00 -[illegible] 4 -[illegible] Z-12 WAS 36.90 ± 3.00 -[illegible] ONLY (3) SH Z B-[illegible] WAS [illegible] -0001 ONLY ADDED DIM B COLUMN TO PN BLOCK (7) -5003 LM ADDED ITEM 4	6-3-80	
	M	CN4 4G425(D)2 ~~was~~ (1) ADDED ITEM 8 TO -1,-2,-3 LM'S	10-21-80	

TEXAS INSTRUMENTS	DWN [illegible] DATE 5-22-6	SIZE D	FSCM NO 96214	DRAWING NO 937515 REV M
	ISSUE DATE	SCALE		SHEET 2

TEXAS INSTRUMENTS INCORPORATED

DATE 10/14/80 — **LIST OF MATERIAL** — PAGE 1 of

PART NUMBER LM0937515-0001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0007	CONN,RECEPTACLE, 40 POSITION	000779-88379-7
0001A					P1 P2	
0007	00002.000	EA		2210259-0008	TAB,PULL,PLASTIC LOOP,40 POS, 2.000 L	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937515-5001	BULK CABLE ASSEMBLY MATERIAL FOR -0001	

DRAFTSMAN — DATE — CKD. DRAFTSMAN J.K. 10-16-80 — DATE — DESIGN ENGINEER — DATE — TITLE: CABLE ASSY,40 PIN,20FT

APPD. MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. 7506/7068 — PART NUMBER LM0937515-0001 REV M

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TEXAS INSTRUMENTS INCORPORATED

DATE 10/14/80 — **LIST OF MATERIAL** — PAGE 1 of

PART NUMBER LM0937515-0002 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0007	CONN,RECEPTACLE, 40 POSITION	000779-88379-7
0001A					P1 P2	
0007	00002.000	EA		2210259-0008	TAB,PULL,PLASTIC LOOP,40 POS, 2.000 L	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937515-5002	BULK CABLE ASSEMBLY MATERIAL FOR -0002	

DRAFTSMAN — DATE — CKD. DRAFTSMAN — DATE — DESIGN ENGINEER — DATE — TITLE: CABLE ASSY,40 PIN, 6FT

APPD. MFG. — DATE — APPD. PROJECT ENGINEER — DATE — RELEASED — DATE — PROJECT NO. — PART NUMBER LM0937515-0002 REV M

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DATE 10/14/80 **LIST OF MATERIAL** PAGE 1 of

PART NUMBER LM0937515-0003 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0007	CONN,RECEPTACLE, 40 POSITION	000779-88379-7
0001A					P1 P2	
0007	00002.000	EA		2210259-0008	TAB,PULL,PLASTIC LOOP,40 POS, 2.000 L	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937515-5003	BULK CABLE ASSEMBLY MATERIAL FOR -0003	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: CABLE ASSY,40 PIN,10FT

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937515-0003 REV M

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PART NUMBER LM0937515-5001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00020.000	FT		0996128-0007	CABLE,FLAT,20 TWISTED PR,1.950 WIDE	SSW -455-248-40
0004	00016.000	FT		0972435-0104	INSUL SLEEVING, 5/8" ID ZIP TUBE,PVC	007240-ZTZ06250320B0L
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	GPL-MS-3368-1-96

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BULK CABLE ASSEMBLY MATERIAL FOR -0001

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937515-5001 REV M

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

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PART NUMBER LM0937515-5002 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00006.667	FT		0996128-0007	CABLE,FLAT,20 TWISTED PR,1.950 WIDE	SSW -455-248-40
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL-MS-3368-1-9B

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BULK CABLE ASSEMBLY MATERIAL FOR -0002

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM0937515-5002 REV M

T.I. 13849

TEXAS INSTRUMENTS INCORPORATED

DATE 10/14/80 **LIST OF MATERIAL** PAGE 1 of

PART NUMBER LM0937515-5003 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00010.500	FT		0996128-0007	CABLE,FLAT,20 TWISTED PR,1.950 WIDE	SSW -455-248-40
0004	00006.000	FT		0972435-0104	INSUL SLEEVING, 5/8" ID ZIP TUBE,PVC	007240-ZTZ062563208OL
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL-MS-3368-1-9B

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BULK CABLE ASSEMBLY MATERIAL FOR -0003

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM0937515-5003 REV M

T.I. 13849

NOTES: UNLESS OTHERWISE SPECIFIED:

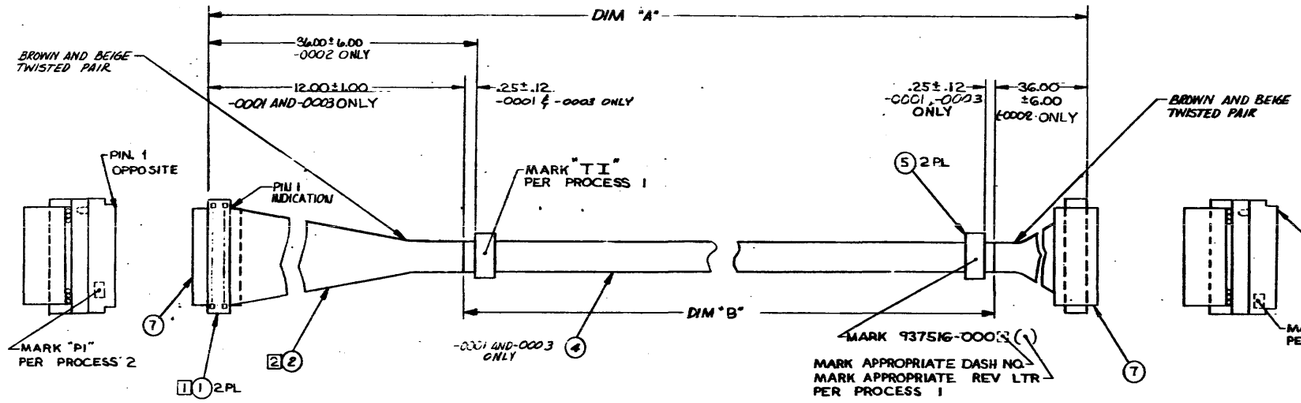
1. P1 AND P2 MUST BE CRIMPED TO THE FLAT UNTWISTED AREAS OF THE CABLE (ITEM 2)
2. MATERIAL (ITEM 2) INITIAL CUT BE AT CENTER OF 2 INCH FLAT SECTION, OVERALL LENGTH TO BE AS SHOWN IN DIMENSIONAL TABLE. DIMENSION A IS NOMINAL AND IS FOR REFERENCE ONLY
3. ~~CUT CABLE IN FLAT UNTWISTED AREAS OF THE WIRE.~~
3. ITEM 101 (A) -0001, -0002 & -0003 LMS CONSISTS OF BULK CABLE ASSY MATL

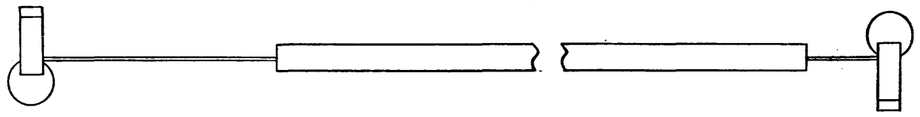
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
M	CN 44G425 (C) B. Lin (1) ADDED PN 948424-9901 (ITEM 8) TO LMS -0001 THRU -0003	9-27-80	J. Reed

937516

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN 424810 (C) H. Rubio (1) DELETED ITEMS 3, 4 & 6 FROM -0002 LM (2) CN-0002 LM QTY OF ITEM 2 WAS 6.50 AND QTY OF ITEM 4 WAS 5.00 (3) DIMS FOR "A" "B" & "C" ON -0002 WAS 72.00±5.00, 40.00±6.00 & 15.00±3.00 RESPECTIVELY (4) DIMS FOR "B & C" ON -0001 WAS 97.00±6.00 & 25.00±3.00 RESPECTIVELY (5) ADDED (-0001 ONLY) TO BALLOONS 3, 4 & 6 AND DIMS 10.00±1.00, 4.00±1.00, 3.00±.50, 2.00±1.00 (6) DELETED 2 PL FROM 10.00±1.00 DIM & BALLOON 3 (7) ADDED BALLOON 3 (-0001 ONLY) ON P2 END OF CABLE (8) ADDED 40.00±6.00 (-0001 ONLY) ON P2 END OF CABLE	1-18-78	J. Reed
B	CN 424815 (C) D. Tinsley (1) PN BLOCK, -1, DIM A WAS 185±5, DIM B WAS 90±6, DIM C WAS 90±6 (2) ON -1 LM, QTY'S ITEM 2 & 4 WERE 15.5 & 11.5 (3) PN BLOCK -1 TITLE DESCRIP WAS CABLE ASSY, 50 PIN, 15 FT	3-14-78	J. Reed
C	CN 440479 (C) Rod Gill (1) CHANGED PRESENTATION OF P1 & P2 TO SHOW SLOT (2) ADDED PROJECTIONS OF P1 P2 (3) REMOVED TRIANGLE OF P2	8-16-78	J. Reed
D	CN 430777 (C) B. Rubio (1) ITEM 3 P/N WAS 417177-B	11-15-78	E. Wing
E	CN 446555 (E) B. Rubio (1) REVISED FOR EXTENSIVE ENGINEERING CHANGES	4-10-79	E. Wing
F	CN 448360 (C) Reed Gill (1) CHGD PICTORIAL OF P1 ZN C-7 (2) CHGD PICTORIAL OF P1 ZN B-7	4-30-79	J. Reed
G	CN 451439 (C) J. Hill (1) CREATED -5001 & -5002 LMS (2) ADDED ITEM 101 TO -0001 & -0002 LMS (3) ADDED NOTE 3 (4) ADDED -5001 -5002 TO P.L. BLOCK	9-6-79	E. Wing
H	CN 448378 (E) J. Hill (1) DELETED ITEMS 5 & 6 FROM -5001 LM (2) ITEM 4 P.L. WAS -0003 ON -5001 LM	9-6-79	E. Wing
J	CN 435004 (C) J. Hill (1) ADDED DIM. 36.00±6.00 (REF) (2) ADDED (-0001 ONLY) TO 12.00±1.00 DIM. (REF) (3) ADDED DIM. 192.00±6.00 (-0001 ONLY) (REF) (4) ADDED (-0002 ONLY) TO 36.00±6.00 DIM (REF)	9-6-79	E. Wing
K	CN 464122 (D) Rod Gill (1) CREATED -0003 & -5003 LMS & RESP COLUMNS IN PN BLOCK (2) ADDED -0003 TO NOTE 3 & DIM. 36.00 ±6.00 IN ZONE C-4 (3) ADDED 3 TO -0003 IN PN BLOCK	3-5-80	J. Reed
L	CN 433776 (D) B. Rubio REV. PER EXTENSIVE ENGR CHANGE	5-30-80	E. Wing

(REV CONTINUED IN ZONE D4)





937516-5003	BULK CABLE ASSY MATL FOR -0003	—	—
937516-5002	BULK CABLE ASSY MATL FOR -0002	—	—
937516-5001	BULK CABLE ASSY MATL FOR -0003	—	—
3 937516-0003	CABLE ASSY, 50 PIN, 10 FT.	120.00±6.00	72 ± 6.00
3 937516-0002	CABLE ASSY, 50 PIN, 6 FT	80.00±6.00	—
3 937516-0001	CABLE ASSY, 50 PIN, 20 FT.	240.00±12.00	192 ± 6.00
PART NUMBER	DESCRIPTION	DIM "A"	DIM "B"

SEQ NO	IDENT	FSPEC	NO	ADDITIONAL	NOTES
	PROCESS		CLASSIFICATION		
2	MARK	100-02	21	HGT .12 CLR WHT	
1	MARK	100-07	712	CLR BLK TYPE 6	

PROCESSES ARE FOR CORRELATION TO ROUTING AND SPECIFICATIONS SEE MFG DRAWING 729067

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES
		PARTS LIST			
			UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN INCHES • TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02 • INTERPRET DRAWING PER MIL-D-1000 • REMOVE ALL BURRS AND SHARP EDGES • CONCENTRICITY MACHINED DIAMETERS .010 T.I.R. • DIMENSIONAL LIMITS APPLY BEFORE PROCESSES • PARENTHETICAL INFO FOR REF ONLY		
		2268025	7068		
		937500	750G		
		NEXT ASSY	USED ON		
		APPLICATION			

HOLE TOLERANCE

.013 THRU .125 — .004 .001	.126 THRU .250 — .005 .001	.251 THRU .500 — .006 .001
.501 THRU .750 — .008 .001	.751 THRU 1.000 — .010 .001	1.001 THRU 2.000 — .012 .001

DRAWN	H. Rubio	5/16/77	TEXAS INSTRUMENTS INCORPORATED Dallas, Texas
CHECKED	D. Tinsley	5/17/77	CABLE ASSY, 50 PIN
ENGINEER	J. Reed	5/17/77	
PROJECT ENGR	E. Wing	5/17/77	
MFG ENGR	J. Tinsley	5/17/77	

SPECIFICATION NO	DRAWING NO
D 96214	937516
SCALE 1/1	SHEET

TEXAS INSTRUMENTS INCORPORATED

DATE 09/26/80

LIST OF MATERIAL

PAGE 1 of

PART NUMBER LM 0937516-0001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0008	CONNECTOR,RECEPT,50POS W/O STRAIN RELIEF	000779-88379-8
0001A					P1 P2	
0007	00002.000	EA		2210259-0009	TAB,PULL,PLASTIC LOOP, 2.500 L, 50 POS	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937516-5001	BULK CABLE ASSEMBLY MATERIAL FOR -0001	

DRAFTSMAN DATE | CKD DRAFTSMAN 9-29-80 DATE | DESIGN ENGINEER DATE | TITLE CABLE ASSY,50 PIN, 20FT

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO 7506 | PART NUMBER LM 0937516-0001 REV M

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PAGE 1 of

PART NUMBER LM 0937516-0002 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0008	CONNECTOR,RECEPT,50POS W/O STRAIN RELIEF	000779-88379-8
0001A					P1 P2	
0007	00002.000	EA		2210259-0009	TAB,PULL,PLASTIC LOOP, 2.500 L, 50 POS	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937516-5002	BULK CABLE ASSEMBLY MATERIAL FOR -0002	

DRAFTSMAN DATE | CKD DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE CABLE ASSY,50 PIN, 6FT

APPD MFG. DATE | APPD PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO | PART NUMBER LM 0937516-0002 REV M

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PART NUMBER LM 0937516-0003 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00002.000	EA		0996261-0008	CONNECTOR,RECEPT,50POS W/O STRAIN RELIEF	000779-88379-8
0001A					P1 P2	
0007	00002.000	EA		2210259-0009	TAB,PULL,PLASTIC LOOP, 2.500 L, 50 POS	000779-88450-9
0008	REF	EA		0948424-9901	OMNI OPERATION PROC AND TEST FLOW	
0101	00001.000	EA		0937516-5003	BULK CABLE ASSEMBLY MATERIAL FOR -0003	

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE CABLE ASSY,50 PIN, 10FT

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 0937516-0003 REV M

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DATE 09/26/80 **LIST OF MATERIAL** PAGE 1 of

PART NUMBER LM 0937516-5001 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00020.000	FT		0996128-0008	CABLE #28 AWG 7-STRAND TWISTED PAIRS FL	SSW - 455-248-50
0004	00016.500	FT		0972435-0104	INSUL SLEEVING, 5/8" ID ZIP TUBE,PVC	007240-ZIZ06256320B0L
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL-MS-3368-1-9B

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE BULK CABLE ASSEMBLY MATERIAL FOR -0001

APPD.-MFG DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 0937516-5001 REV M

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PART NUMBER LM 0937516-5002 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00007.500	FT		0996128-0008	CABLE #28 AWG 7-STRAND TWISTED PAIRS FL	SSW - 455-248-50
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL-MS-3368-1-98

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BULK CABLE ASSEMBLY MATERIAL FOR -0002

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 0937516-5002 REV M

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PART NUMBER LM 0937516-5003 REV M

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0002	00010.500	FT		0996128-0008	CABLE #28 AWG 7-STRAND TWISTED PAIRS FL	SSW - 455-248-50
0004	00006.000	FT		0972435-0104	INSUL SLEEVING, 5/8" ID ZIP TUBE,PVC	007240-ZIZ062563200L
0005	00002.000	EA		0418201-0060	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL-MS-3368-1-98

DRAFTSMAN DATE | CKD. DRAFTSMAN DATE | DESIGN ENGINEER DATE | TITLE: BULK CABLE ASSEMBLY MATERIAL FOR -0003

APPD.-MFG. DATE | APPD. PROJECT ENGINEER DATE | RELEASED DATE | PROJECT NO. | PART NUMBER LM 0937516-5003 REV M

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ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

HOW TO USE THE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables. The table of contents does not contain four-level paragraph entries. Therefore, for four-level paragraph numbers such as 2.3.1.2, use the three-level number and the corresponding page number. In this case, the three-level number is 2.3.1.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.

- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.

- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.

- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See"followed by the referenced entry.

The index is divided into sections for the letters of the alphabet. Acronyms and mnemonics (words made up entirely of capital letters) are listed first within each section. Words that begin with a capital letter follow the acronyms and mnemonics.

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USER'S RESPONSE SHEET

Manual Title: Model 990 Computer DS10 Cartridge Disk Controller Depot Maintenance Manual (946262-9701)

Manual Date: 1 May 1982 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

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Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual	Comment/Suggestion

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