

TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 960/980 Computer Model DS44 Disc Controller Maintenance Manual

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PREFACE

This manual provides maintenance instructions for the Texas Instruments Model DS44 Moving Head Disc Controller. The manual also provides the theory of operation for the controller. The information in the manual is divided into the following sections:

- I Introduction – Provides a general introduction to the Model DS44 Moving Head Disc Controller.
- II Moving Head Disc Controller – Provides a description of the organization and functions of the controller.
- III Theory of Operation – Provides the detailed theory of operation for the Moving Head Disc Controller.
- IV Maintenance – Provides the information necessary to troubleshoot the controller.
- V Documentation – Describes the computer-generated documentation, including the Pin List and Load List for the controller.
- VI Drawings – Contains the drawings pertinent to the maintenance of the controller.

Additional information concerning the Model DS44 Moving Head Disc Controller may be found in the following:

Title	Part Number
<i>960/980 DMAP Expander Manual</i>	216759-9701
<i>Maintenance Manual for Model DS44 Disc Drive</i>	973792-9701
<i>Model 980A Maintenance Manual System Description</i>	960699-9701
<i>Model 980B Maintenance Manual System Description</i>	943012-9701
<i>Model 960A Maintenance Manual System Description</i>	226750-9701
<i>Model 960B Maintenance Manual System Description</i>	942773-9701
<i>Block Transfer Controller Maintenance Manual</i>	240802-9701



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SECTION I

INTRODUCTION

1.1 SCOPE

This manual contains the maintenance documentation and theory of operation for the Model DS44 Moving Head Disc Controller, which interfaces the Direct Memory Access Channel of the Model 960 or Model 980 Computer. This document discusses only the controller and its interface to the moving head disc unit.

1.2 DISC CHARACTERISTICS

The controller is designed for the Model DS44 Moving Head Disc Drive. Each Disc Drive contains one fixed and one removable disc with one read/write head per surface. Each disc surface has 408 tracks, 88 data sectors/track (an 89th sector is used for head switching), 32 data words/sector, for a total of 1,148,928 words/surface. The maximum data transfer rate is 156.25K words/second.

The controller accommodates up to four Model DS44 disc units. Additional information on the disc drives may be obtained from the maintenance manuals or specifications.

1.3 INSTALLATION

The Moving Head Disc Controller can be included in several combinations of peripheral controllers. The connector plate wiring for all combinations is documented in the DMAC Expander Maintenance Manual. Refer to the appropriate section to determine the correct board locations of the controller.



SECTION II

MOVING HEAD DISC CONTROLLER

2.1 GENERAL

The controller for the Model DS44 disc drive, combined with a Block Transfer Controller (BTC), provides an interface to the Direct Memory Access Port of the Model 960 or 980 computers through the Direct Memory Access Channel (DMAC) Expander. Refer to figure 2-1 for a block diagram relationship of the disc controller and disc drive to the 960 or 980 computer.

2.2 DISC CONTROLLER ORGANIZATION

The Moving Head Disc Controller consists of two major logic sections: the Block Transfer Controller (BTC), and the Disc Control Logic (DCL). The BTC provides the interface for the DMAC Expander and the DCL provides the interface for the disc drive. The BTC and DCL are discussed in detail in Section III - Theory of Operation. Figure 2-2 illustrates the disc controller organization.

2.3 DISC SECTOR ORGANIZATION

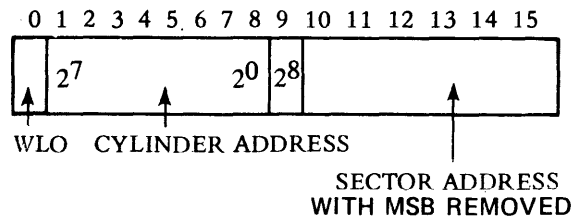
The minimum addressable block of data on the disc is a sector. Each sector consists of a 16-bit preamble word, an identification (I.D.) word, 32 data words, and a data check word.



SECTOR FORMAT

The controller generates the preamble, I.D., and check words. The preamble word is used to activate the disc drive read/write logic. The I.D. word identifies the associated sector. The check word is used to determine if the data was read from the disc correctly.

2.4 IDENTIFICATION WORD



Bit 0	Write Lockout Bit. A logic ZERO indicates that the data in the associated sector is not protected and can be written over. A logic ONE indicates that the data in the associated sector is protected and can be written over only with a Write I.D. command or a Write Data command with Lockout Override. This bit is specified by the Write I.D. Command.
Bits 1 through 9	Cylinder Address Field. These bits indicate the cylinder address on which the associated sector may be found.
Bits 10 through 15	Sector Address Field with MSB Removed. These bits indicate the address of the next sector which will come under the read/write head.

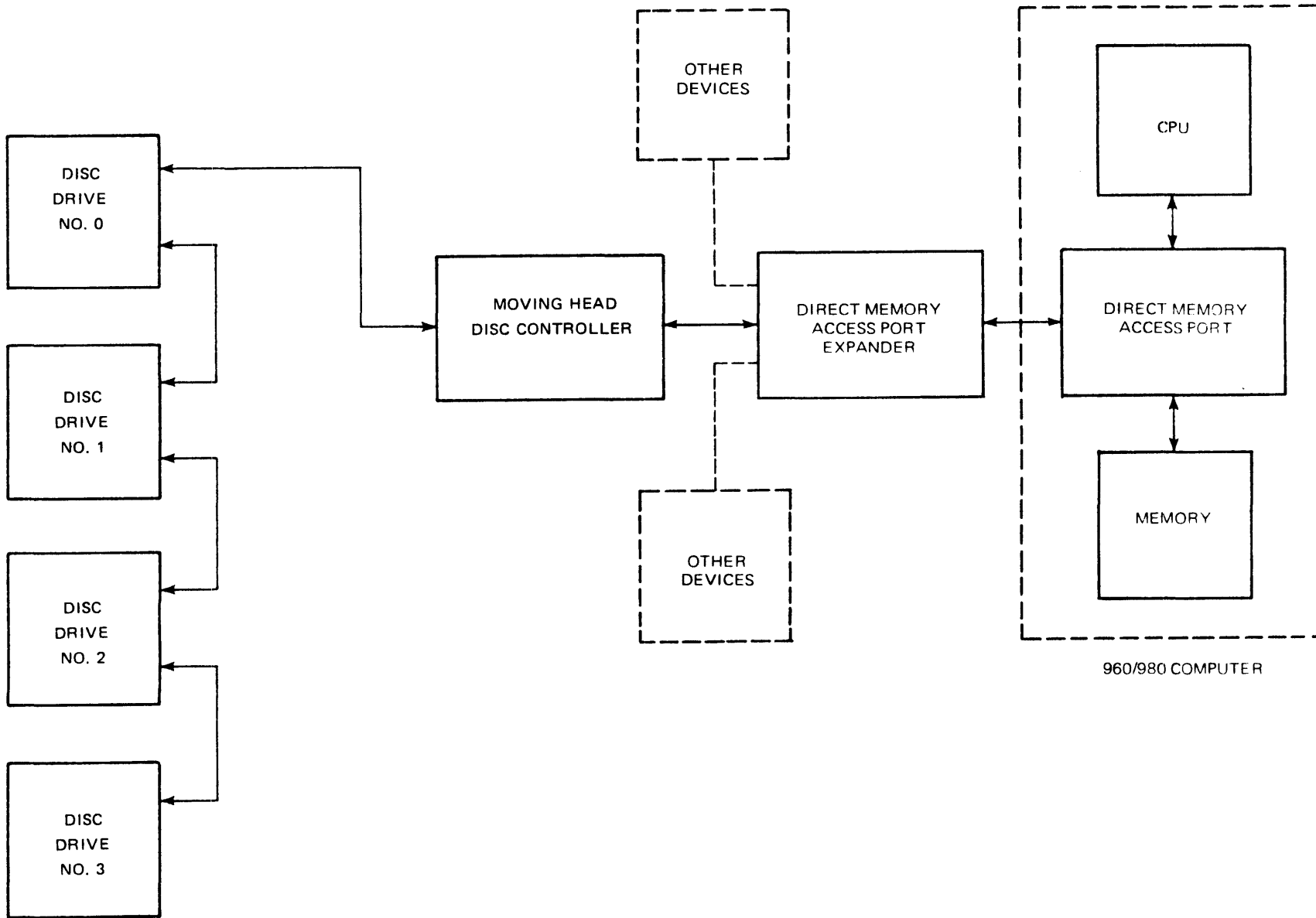


Figure 2-1. Disc Drive, Disc Controller and Computer Block Diagram Relationship

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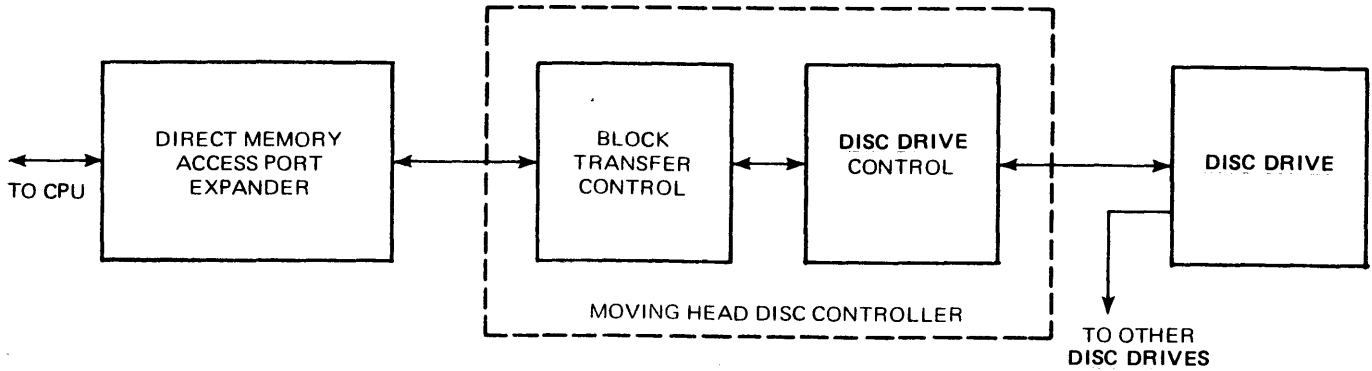


Figure 2-2. Disc Controller Organization Block Diagram

2.5 DISC CONTROLLER FUNCTIONS

The controller is capable of performing several types and combinations of read, write, and seek operations. While executing certain read/write commands, the controller performs several automatic functions such as data checking, head switching, and data address verification. The automatic functions are explained in the following paragraphs, and should be remembered when using this controller.

2.5.1 AUTOMATIC SEEKING. Upon receipt of a Read, Write, or Compare command, the controller always causes the disc to seek to the cylinder address given in List Word 3. Therefore, it is not mandatory that a Data Transfer command be preceded by an Independent Seek command.

2.5.2 AUTOMATIC TRACK INCREMENT. If the end of a track is encountered during a data transfer operation and all the data has not yet been transferred, the controller will seek to the next cylinder and/or switch heads (refer to figure 2-3). If only the head was switched, data transfer will be interrupted for only one sector time (about 280 microseconds). If the cylinder was incremented, thereby causing an automatic seek, data transfer will be interrupted for about 12.5 milliseconds.

		OUTER EDGE OF DISC	DS31/DS32 END OF DISC (INNER MOST CYLINDER)	DS44 END OF DISC (INNER MOST CYLINDER)
	CYLINDER ADDRESS	0 1 2 3 4 5 6 . . . 200 201 202	203 . . . 405 406 407	
TOP SURFACE HEAD ADDRESS 0	TRACK NUMBER	0 2 4 6 8 10 12 . . . 400 402 404	406 . . . 810 812 814	
BOTTOM SURFACE HEAD ADDRESS 1	TRACK NUMBER	1 3 5 7 9 11 13 . . . 401 403 405	407 . . . 811 813 815	

THE COMBINATION OF HEAD ADDRESS AND CYLINDER ADDRESS DEFINE A TRACK ADDRESS.

IF AN OPERATION IS BEING PERFORMED ON AN EVEN NUMBERED TRACK, i.e., 0, 2, 4, 6 ... 404, UPON REACHING THE END OF THE TRACK, IF THE SECTOR COUNT IS NOT ZERO, THE HEAD WILL BE SWITCHED TO THE BOTTOM SURFACE AND PROCESSING WILL RESUME WITH SECTOR ZERO, SAME CYLINDER, BOTTOM SURFACE.

IF AN OPERATION IS BEING PERFORMED ON AN ODD NUMBERED TRACK, i.e., 1, 3, 5, 7 ... 405, UPON REACHING THE END OF THE TRACK IF THE SECTOR COUNT IS NOT ZERO, THE HEAD WILL BE SWITCHED TO THE TOP SURFACE AND THE CYLINDER WILL BE INCREMENTED. AFTER THE DISC HAS BEEN SEEKED TO THE NEXT CYLINDER, THE I.D. WILL BE VERIFIED, AND PROCESSING WILL RESUME WITH SECTOR ZERO.

(A)133414

Figure 2-3. Automatic Track Incrementing



2.5.3 AUTOMATIC I.D. VERIFICATION. The controller automatically checks the I.D. word for proper cylinder address during a read data, write data, or compare data operation under the following conditions:

NOTE

A track address is defined by a head address and a cylinder address. Refer to figure 2-3.

1. After acquiring an initialization list, the controller checks the I.D. word on the starting track address before executing the list.
2. After an automatic cylinder increment and after the disc reaches the new cylinder, the controller checks the I.D. word on the new cylinder before continuing with the list. The I.D. word is not checked if only the head is switched (refer to figure 2-3). Therefore, a Write I.D. with Lockout Enabled should be performed on a cylinder basis.

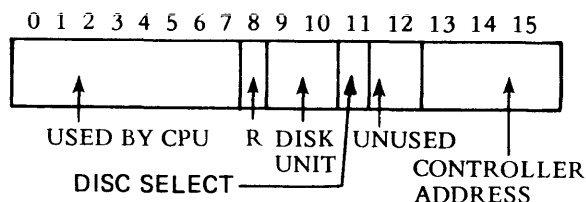
2.5.4 WRITE PROTECTED DATA. Since automatic I.D. verification is performed on a first sector encountered basis, the minimum amount of data that can be write-protected is 88 sectors (one track). Any track on the top surface of the disc (Head Address = 0) which is write protected can only be changed by a Write I.D. command or a Write Data with Lockout Override command. If data is to be write-protected on a track on the bottom surface, the whole cylinder (top track and bottom track) should be protected.

2.5.5 STATUS STORAGE. Every time status is stored, the Status Register in the controller is cleared. Any time the controller is addressed by an Automatic Transfer Instruction (ATI) while it is executing a previous list, a Busy status will be stored. Therefore, any nonabortive status that had accumulated to that point is stored with the Busy status and is not reported again when the current list is completed. Note that Operation Complete status may be accompanied by Busy, Parity Error, I.D. Compare Error status, and/or Seek Complete Unit XX status.

2.6 INSTRUCTION FORMAT

The Automatic Transfer Instruction (ATI) in the 980 computer and the Activate Direct Access Channel (ADAC) command in the 960 computer are each two-word instructions by which a device on the Direct Memory Access Channel is activated. Execution of an ATI or ADAC command causes a strobe to be generated with each of the two words. Each strobe indicates that the corresponding word is stable on the memory read data lines and may be accepted by the controller. The format for each of the two words is given in the following paragraphs.

2.6.1 FIRST ACTIVATE WORD





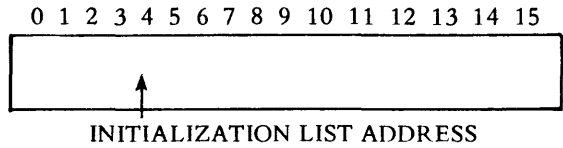
When the first word from the CPU is stable on the read data lines (indicated by the first strobe), the BTC decodes the address bits (12 through 15) to determine if it is being addressed. If addressed, the BRC presents bits 8 through 11 to the DCL.

- Bit 8 Reset/Acquire List Bit. A logic ZERO indicates the controller is is to acquire an initialization list. A logic ONE resets the BTC and DCL (equivalent to depressing the Master Reset button on the front panel of the computer).

- Bits 9 These bits determine the disc unit on which reading/writing and 10 will occur.
 00 selects Disc Drive No. 0
 01 selects Disc Drive No. 1
 10 selects Disc Drive No. 2
 11 selects Disc Drive No. 3

- Bit 11 Disc Select
 0 selects Fixed Disc
 1 selects Removable Disc
 (can be reversed with plug-in jumper)

2.6.2 SECOND ACTIVATE WORD

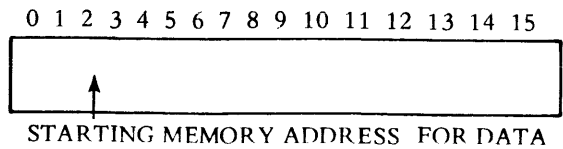


The second word of the ATI or ADAC command is the memory address from which the BTC fetches the initialization list. The controller does not need any further commands from the CPU until the specified list operation is completed or aborted. The second word is accepted by the BTC only if it was addressed by the first word and the controller was not still processing a previous list.

2.7 INITIALIZATION LIST

The initialization list is stored in memory prior to the issuance of an ATI or ADAC command. The list consists of four words located in consecutive memory locations, with the address of the first list word being defined in the second word of the ATI or ADAC command. The format for the list words is given in the following paragraphs.

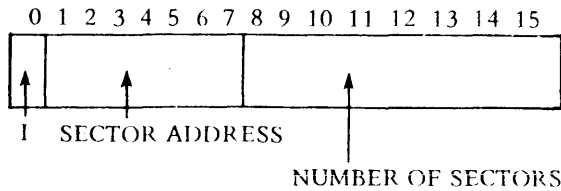
2.7.1 LIST WORD 1



List Word 1 specifies the starting memory address where the first data word will be fetched/stored. Successive data words will be fetched/stored at consecutively higher memory locations.



2.7.2 LIST WORD 2

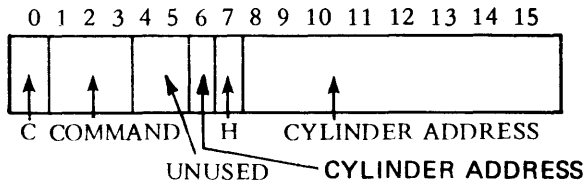


- Bit 0 Interrupt Bit. A logic ZERO enables the controller to store status without issuing an interrupt. A logic ONE causes the controller to issue an interrupt and wait for interrupt recognition before storing status.

- Bits 1 through 7 Sector Address Bits. These bits determine the sector at which the controller begins data transfer. The minimum allowable number in this field is 00_{16} . The maximum allowable number is 57_{16} . A number greater than 57_{16} results in a Program Error status.

- Bits 8 through 15 Sector Count Field. This field determines the number of sectors to be transferred. When performing ANY operation on the disc, this field must be nonzero. If not, a Program Error status will result. The maximum allowable value in this field is FF_{16} .

2.7.3 LIST WORD 3



- Bit 0 Chain Bit. A logic ZERO indicates the controller is to terminate processing after completing the operation specified in the current list. A logic ONE indicates the controller is to acquire another initialization list (from the memory address specified by List Word 4) after completing the operation specified in the current list.

- Bits 1 through 3 Command Field. This field determines the type of operation the controller is to perform.
 - 000 Read data
 - 001 Read Identification word
 - 010 Compare data
 - 011 Independent seek
 - 100 Write data
 - 101 Write I.D., Lockout disabled
 - 110 Write I.D., Lockout enabled
 - 111 Write data, Override lockout

- Bits 4 and 5 Not used.



Bit 6 and Bits
8 through 15

Cylinder Address. This field specifies the cylinder address at which the data transfer will begin. Bit 6 is the most significant bit, and bits 8 through 15 must be between 0 and 197_{16} .

Bit 7

Head Select. This bit selects the head which is to be used in the transfer operation. Together with the cylinder address, this bit specifies a unique track on the disc. The head selection is:

- 0 - Upper head (top surface)
- 1 - Lower head (bottom surface)

2.7.3.1 Read Data. The controller reads data from the disc and stores it in CPU memory until the number of sectors specified in List Word 2 have been transferred. Automatic track incrementing applies. See figure 2-3.

2.7.3.2 Read I.D. The next identification word that comes under the read head will be transferred to the memory location specified in List Word 1.

2.7.3.3 Compare Data. The controller compares the data in memory (starting at the address specified in List Word 1) to the data on the disc (starting at the sector and cylinder specified in List Words 2 and 3, respectively).

2.7.3.4 Independent Seek. This operation causes the controller to move the head to the cylinder address specified in List Word 3. After the disc accepts the Seek command, the controller stores Operation Complete status (this occurs 20 microseconds to 50 microseconds after receipt of List Word 4). The controller is then ready to accept a command to perform an operation on another unit. When the disc completes the seek, the controller stores Seek Complete status for that unit whether or not the controller is busy processing a list on another unit.

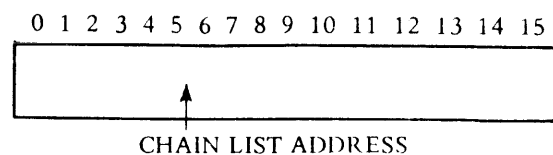
2.7.3.5 Write Data. The controller writes data on the disc until the number of sectors specified in List Word 2 have been written. If the lockout bit (Bit 0 of the I.D. word) is set, no data is written and the controller stores Write Lockout status and terminate.

2.7.3.6 Write I.D., Lockout Disabled. The I.D. word is written on the number of sectors specified in List Word 2. The data portion of each sector consists of the data word in the specified memory address of List Word 1.

2.7.3.7 Write I.D., Lockout Enabled. This operation is the same as write I.D., lockout disabled, except that the write lockout bit (bit 0 of I.D. word) is written as a logic ONE. Therefore, a Write Data Override Lockout command is required to write data on these sectors.

2.7.3.8 Write Data, Override Lockout. The number of sectors specified in List Word 2 is written on the disc, whether or not the write lockout bits (bit 0 of the I.D. word) is on. The write lockout bit condition of the I.D. word is not altered by this operation.

2.7.4 LIST WORD 4





List Word 4 specifies the starting memory address of the next Initialization List to be acquired if chaining is indicated by bit 0 of List Word 3. If chaining is not indicated, this list word is ignored. Chaining allows the controller to read/write from different areas of memory and/or execute more than FF_{16} sectors with the CPU issuing only one ATI or ADAC command.

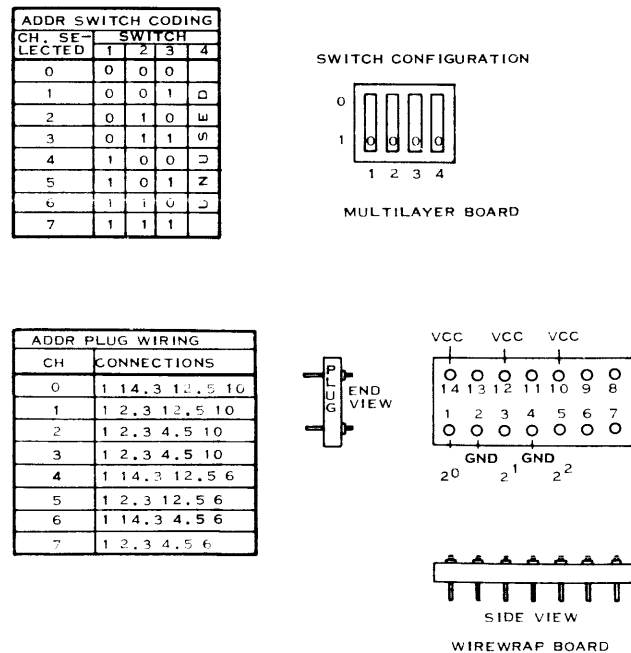
2.8 CHANNEL ADDRESSING

The controller may be assigned any channel (DMAP) address from channel 0 through channel 7. Circuitry within the BTC section of the disc controller uses the assigned (hardwired) address to determine when to respond to an ATI or ADAC command. This circuitry also determines which request lines to drive and which acknowledge lines to monitor as explained in the following paragraphs. Refer to the BTC manual for detailed information.

2.8.1 ADDRESS SELECTION. The channel addressing scheme utilized permits assignment of any channel address and enables the address to be changed if required. The assigned channel address is wired on an address select plug as shown in figure 2-4. The decoding and comparison of the assigned address to the address in ATI1 or ADAC1 is shown functionally in figure 2-5.

2.8.2 ADDRESS MODIFICATION. In order that the channel address may be changed without altering the controller logic or connector plate wiring, the BTC section of the Disc controller picks up seven sets of channel control lines. However, only one line from each group, the one corresponding to the assigned channel, is utilized.

The circuitry for driving the appropriate memory access line and interrupt request line is shown in figure 2-6. The circuitry for monitoring the memory access grant line and interrupt acknowledge line is shown in figure 2-7. Using this channel addressing scheme makes address modification a simple matter of altering the address select plug wiring.



(A)134196

Figure 2-4. Channel Address Decoding

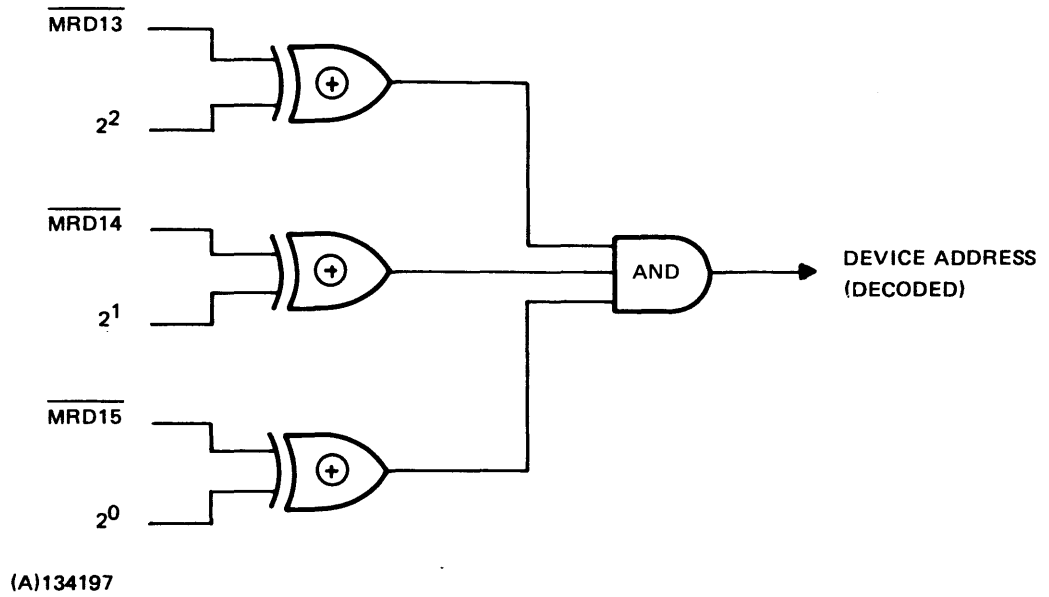


Figure 2-5. Channel Address Decoding Logic

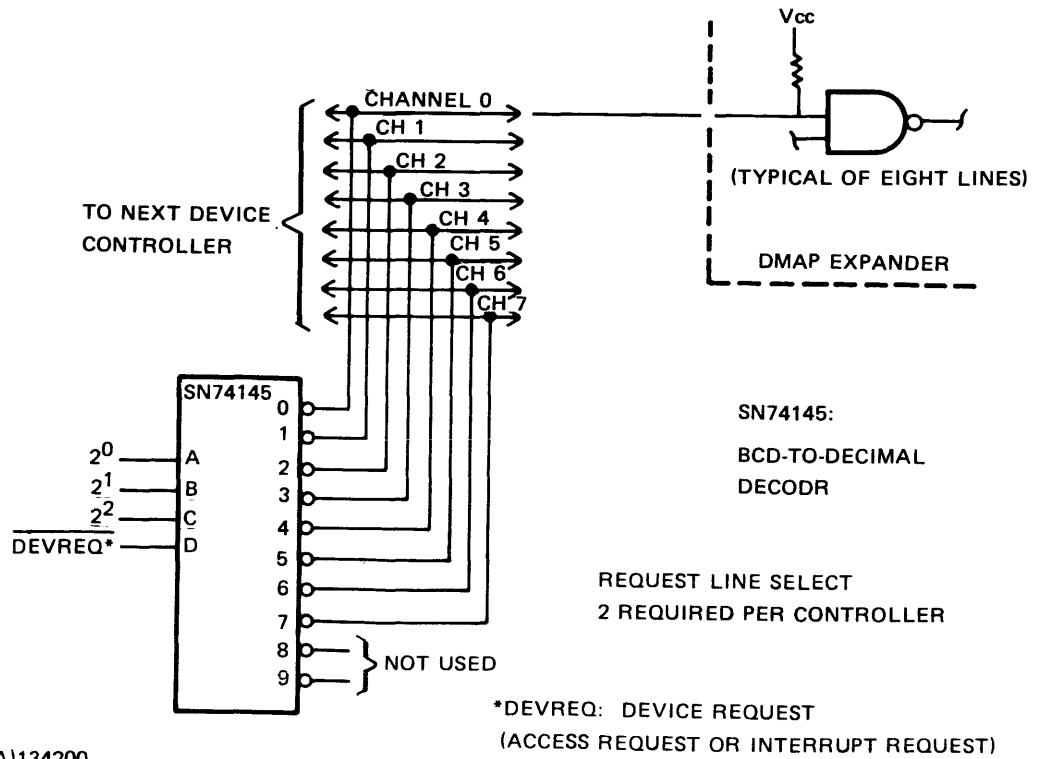


Figure 2-6. Request Line Select

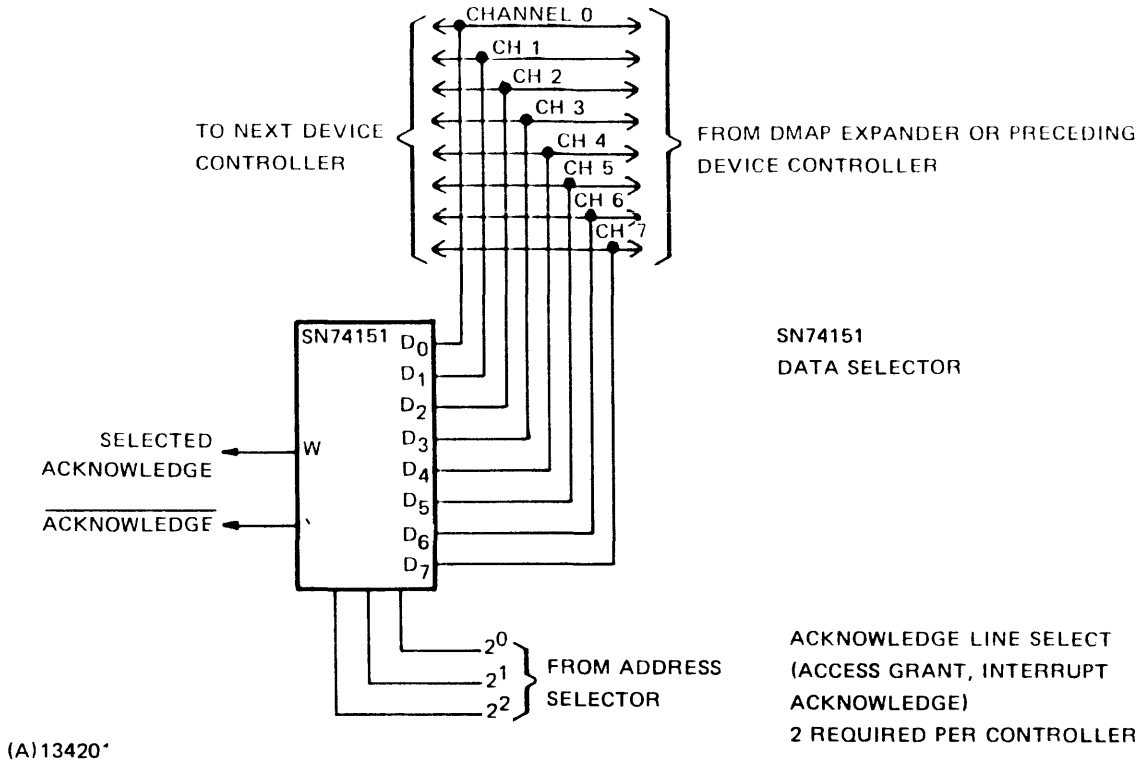


Figure 2-7. Acknowledge Line Select

2.9 MEMORY ACCESS

In executing a memory cycle, the controller issues a request for memory access and then waits until a memory access grant is received before proceeding. The time elapsing between a request and receiving access is dependent on CPU activity, the Expander, other device controllers, and the channel address assigned to this controller (priority). The BTC section of the disc controller contains the circuitry for executing memory cycles. For detailed information refer to the BTC manual. The generalized timing chart of figure 2-8 gives the relationship between signals at the controller/expander interface.

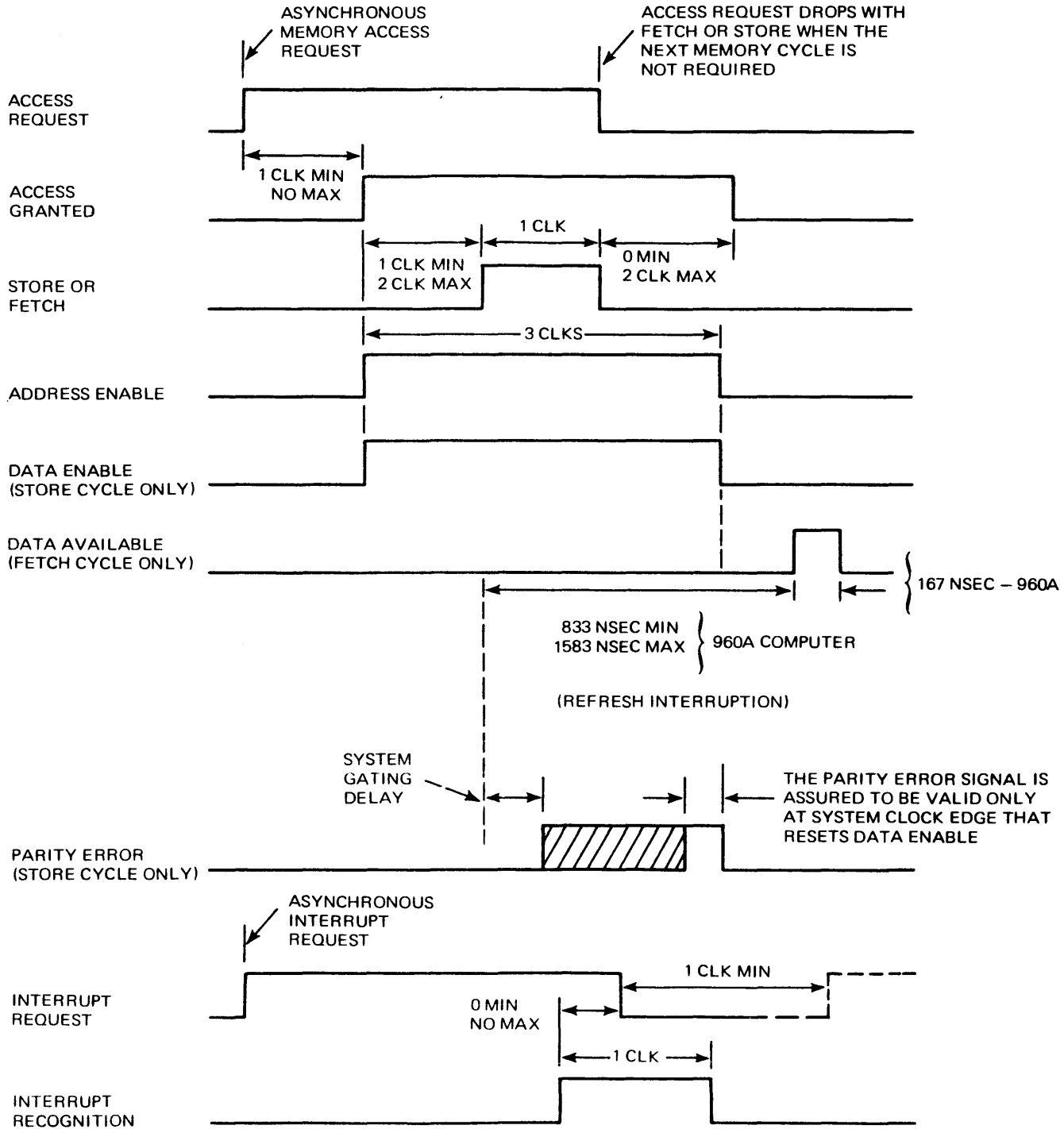
2.10 INTERRUPTS/STATUS

The controller may interrupt the program being executed by the CPU and cause the controller status to be processed.

When the specified operation is completed, the controller issues an interrupt request (if interrupts were enabled by bit 0 of the last List Word 2 that was received) indicating that status is ready to be stored in memory and processed by the CPU. The controller must then wait until an interrupt recognition is received before taking further action (to receive an interrupt recognition, the DMAC interrupt bit in the CPU Status Register must be set).

When an interrupt recognition is received, the controller proceeds with status storage through the memory access request sequence.

2.10.1 STATUS STORAGE LOCATIONS. The controller stores two status words each time it stores status. The locations in memory where status is stored are a function of the channel that the controller is "on". Refer to figure 2-4.



NOTES:

1. SIGNALS ARE SHOWN IN THE TRUE SENSE.
2. DEVICE CONTROLLER INTERFACE IS ASYNCHRONOUS TO THE COMPUTER.
3. SYSTEM CLOCK IS 3 MHz (333 NSEC) FOR THE 960 COMPUTER AND 4 MHz (250 NSEC) FOR THE 980 COMPUTER

(A)134202

Figure 2-8. Controller Interface Signal Relationship



2.10.2 STATUS WORD 1.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
O.C.	W.P.E.	O.L.E.	D.T.O.	E.F.D.	P.O.F.	C.E.	P.A.R.	I.D.R.	B.S.Y.	CH.L.TKN.	W.L.ON	S.C. ₁₁₂	S.C. ₁₀₂	S.C. ₀₁₂	S.C. ₀₀₂

- Bit 0 Operation Complete. Status is stored upon successful completion of a nonchained list, where the operation called for is a read, compare, read I.D., write I.D., or the disc unit accepts an Independent Seek command.
- Bit 1 Write Protect Enabled. Status is stored if an attempt is made to write on a disc while its write protect switch is "on". The controller is reset to its idle state when the status is stored.
- Bit 2 Offline. Status is stored if an attempt is made to perform an operation on the disc and it is not ready, i.e., power is not "on", disc is not at proper speed, disc cartridge is not in position, unit does not exist, and after a restore operation following a disc malfunction during a seek. The controller then returns to its idle state.
- Bit 3 Data Transfer Error. Status is stored if a data word was not available from the CPU at the time required (write operation) or if the controller could not store a data word in the CPU in the time required (read operation). The word transfer rate between the controller and the CPU is approximately 156.25 KHz, (one word every 6.4 microseconds). Upon detection of a data transfer error, reading or writing is discontinued and the controller resets to its idle condition after storing status. This status will also occur if an attempt is made to transfer data to/from a disc cartridge that has never been initialized by a write I.D. operation (i.e., a new cartridge or a cartridge with a bad surface on it).
- Bit 4 End of Disc. If an attempt is made to read or write beyond cylinder address 407, the controller restores the disc to cylinder 00₁₆. After the disc is restored, an End of Disc status will be stored. The controller then resets to its idle condition.
- Bit 5 Program Error. Status will ALWAYS be stored if List Word 2 has an invalid starting sector address or List Word 2 contains a sector count of zero. The controller then resets to its idle state.
- Bit 6 Compare Error. Status is set during a compare operation if the data read from the disc does not match the data pulled from the specified CPU memory buffer. Status is stored after the current sector has been compared. The controller then returns to its idle state. Chaining is ignored.



- Bit 7 Parity Error. Status is set during a read operation or a compare operation if the parity read from the disc does not match the parity generated by the controller. Status is stored after all sectors in the list have been read. If the list is chained, the controller acquires the new list and continues.
- Bit 8 I.D. Compare Error. Before executing a data transfer to or from the disc for a read, compare or write operation, the I.D. word is checked against the cylinder, head, and sector address registers of the controller.
- For a write data operation, the I.D. word of the first sector encountered of the selected track is checked. If a match does not occur with controller registers, the I.D. Compare Error status is set and the write operation terminates before writing begins on the disc. The controller returns to its idle state after the status has been stored. For a read or compare operation, an I.D. Compare Error status does not terminate the operation.
- Bit 9 Device Busy. Status is set when the controller receives an ATI command while it is processing another list. Status is stored immediately. The controller then continues processing its list and the status register is reset.
- Bit 10 Chain List Taken. Upon successful completion of a list whose chain bit is "on" (List Word 3, bit 0), the controller does not store status, but acquires the new list. The controller then stores the Chain List Taken status and continues by processing the new list. If a list whose chain bit is "on" is not successfully completed, the new list is not acquired and processing will be discontinued.

NOTE

On a parity error, processing and chaining will continue.

- Bit 11 Write Lockout On. Status is stored if an attempt is made to write on a track whose write lockout bit (bit 0 of the I.D. word) is "on". Refer to the Write Protected Data paragraph for exceptions.
- Bit 12 Seek Complete Unit 11_2 . Status is stored when the unit indicates it has reached the proper cylinder address. The sequence of events for a seek operation is as follows (assuming the controller is idle, not busy):
1. The controller becomes busy upon receipt of a Seek command.
 2. The disc unit accepts the Seek command.



3. The controller stores Operation Complete status and returns to its idle condition (ready for another ATI command).
4. From 8 to 70 milliseconds later, depending on how far the disc had to seek, the disc completes its seek and the controller stores Seek Complete status for that unit. This status is stored as soon as it is encountered whether or not the controller is in the process of executing another list on a different disc unit. An interrupt precedes this status only if interrupts were enabled by the last List Word 2 received by the controller.

- Bit 13 Seek Complete Unit 10_2 . See description for bit 12.
- Bit 14 Seek Complete Unit 01_2 . See description for bit 12.
- Bit 15 Seek Complete Unit 00_2 . See description for bit 12.

2.10.3 STATUS WORD 2. The second status word is not utilized.

2.11 DATA TRANSFER RATE

Data transfer between the controller and the CPU is in 16-bit parallel form. Data transfer between the controller and the disc is in bit serial form with the least significant bit being transferred first and the most significant bit being transferred last. The bit transfer rate between the controller and the disc is 2.5 MHz. The maximum word transfer rate between the controller and the CPU memory is 156.25 KHz. The actual rate is governed by the activity of other DMAC controllers.

2.12 CONTROLLER INTERFACE SIGNALS

Signal levels are compatible with Texas Instruments Series 74 TTL (transistor-transistor logic) integrated circuits and are defined as follow:

- | | |
|------------|--|
| Logic ONE: | +5 volts (maximum)
+2.4 volts (minimum) |
| Logic ZERO | +0.8 volt (maximum)
+0.0 volt (minimum) |

Three interfaces will be described: CPU/Block Transfer Controller Logic (BTCL), BTCL/Disc Controller Logic (DCL), and DCL/Disc.

2.12.1 SIGNALS FROM THE CPU. Signals from the CPU that are buffered and/or processed by the Expander and routed to the BTC are listed in table 2-1. Data lines are provided in the logically true sense and all other lines are provided in the logically false sense.

2.12.2 SIGNALS TO THE CPU. Signals from the BTC that are buffered and/or processed by the Expander and routed to the CPU are listed in table 2-2. Data and address lines are provided in the logically true sense and all other lines are provided in the logically false sense.

**Table 2-1. Signals from CPU to BTC**

Signal	Remarks
DEVMRD(N)	Memory Read Data. N = 00-16. Bit 0 is MSB. Bit 15 is LSB.
AG,(N)–	Memory Access Granted. N = 0-7. Indicates that channel (N) has the next memory cycle
DEVATI1–	Channel Activate Strobe. Accompanies first ATI or ADAC word
DEVATI2–	Channel Activate Strobe. Accompanies first ATI or ADAC word
IRECOG(N)–	Interrupt Acknowledge. N = 0-7. Indicates that channel (N) may proceed with a status (store) cycle
DATAV–	Data Available. Indicates that the memory read data lines are stable on a fetch cycle
CLOCK–	System Clock. 3MHz for 960 computer and 4MHz for 980 computer
RESET–	Master Reset. For initialization when required.

Table 2-2. Signals to CPU from BTC

Signal	Remarks
DEVMWD,(N)	Memory Write Data. N = 00-16. Bit 0 is MSB. Bit 15 is LSB.
DEVADD,(N)	Memory Address. N = 00-15. Bit 0 is MSB. Bit 15 is LSB.
ARDEV,(N)–	Memory Access Request. N = 0-7. Channel (N) request for memory access
INTDEV,(N)–	Interrupt Request. N = 0-7. Channel (N) request for an interrupt cycle (status store cycle)
DEVSTORE–	Store cycle initiate
DEVFETCH	Fetch cycle initiate



2.12.3 DISC CONTROLLER TO BTC INTERFACE. The controller/BTC interface is designed so that the controller and the BTC must be located in the same motherboard and mounted within one standard enclosure.

Signal levels are determined by the signature of the signal. The signals suffixed with a bar(-) are referred to as false or inverted logic (at the low-voltage level, the logical function of the signal is true; at the high-voltage level, the logical function of the signal is false.)

All signals at the BTC/controller interface are synchronized with the trailing edge of the CPU system clock (SCLOCK).

The signal definitions in this section apply only when the BTC is used with the disc controller. For a more detailed description, refer to the BTC specification.

2.12.3.1 BTC to Controller Signals. The signals from the BTC to the controller are given in table 2-3.

2.12.3.2 Controller to BTC Signals. The signals from the controller to the BTC are given in table 2-4. These signals are generated by cut-collector IC devices with enables.

2.12.4 CONTROLLER/DISC INTERFACE. The logic levels for the controller/disc interface signals are TTL compatible.

Logic ONE +2.4 to +5.0 Vdc

Logic ZERO 0 to 0.8 Vdc

All interface connections are made with one cable to disc unit 0. This cable connects to a top edge connector of one disc controller board.

Tables 2-5 and 2-6 define the signals between the controller and the disc.

For a more detailed description, refer to the applicable disc specification.



Table 2-3. BTC to Controller Signals

Signal	Remarks
ATI1	This one clock time signal occurs every time the CPU addresses the disc controller with an ATI or ADAC command.
ATI2	This one clock time signal indicates that the second word of the ATI or ADAC command is available. This signal will not occur if the ATI1 was received while the disc controller was busy (processing a previous initialization list).
MRD(N)	N = 08 to 11. These lines are monitored only during the ATI1 pulse. At this time they indicate the contents of bits 8, 9, 10 and 11 of the first ATI word.
LIST(N)	N = 1, 2, 3, or 4. These one clock time signals indicate that List Word N is available during this clock time only.
RFOUT(N)-	N = 00 to 15. These signals represent a bidirectional data bus. All data transfers between the controller and the BTC are made through these 16 lines.
READY	This signal indicates the BTC is ready to transfer a word from/to the controller.
STATBUSY	This signal indicates the BTC is ready to begin a status store operation.
ZERO8	This signal indicates that all the sector(s) in the initialization list have been read or written.
MREST	This signal indicates that the CPU Master Reset switch or the power clear has been actuated. A high on this line causes the controller to be immediately reset to its idle condition.
SCLOCK	This is the CPU system clock.



Table 2-4. Controller to BTC Signals

Signal	Remarks
LISTEN-	This one clock time signal causes the BTC to fetch four list words.
RF4EN	This signal indicates which Register File Register in the BTC contains the address of the first list word.
MEMEN-	This one clock time signal activates the BTC data transfer controllers. Upon activation, these controllers begin transferring data to/from CPU memory.
DEVREAD	This signal indicates whether data is being transferred to or from CPU memory.
ACK-	This signal indicates that the disc controller is ready to transfer a word to the BTC (if reading from the disc) or that the disc controller has taken a data word from the BTC (if writing on the disc).
COUNT	This signal will be disabled so that the second status word stored will be the list address.
DECOUNT-	This one clock time signal decrements the sector counter in the BTC.
STATEN-	This signal activates the BTC status controller.
INTEN-	This signal indicates that status will be stored via interrupts.
TWOSC	This signal indicates that two status words will be stored.
BUSY-	This signal indicates the disc controller is busy.
BTCLR-	This signal resets all active controllers and flip-flops in the BTC and resets the disc controller.



Table 2-5. Controller to Disc Signals

Signal	Description
ADDS(N)–	Cylinder Address. N = 0-7, and 0, A. Nine lines which establish the 9-bit parallel address that defines a track on each disc surface by defining the position of the heads. Logic ZERO for true
RESTORE–	Restore. One line which signals the disc to retract the heads to the home position, cylinder address (000) ₈ . In response to this signal, the Address Register in the disc is also set to (000) ₈ and an address acknowledge (ADSACK–) is issued by the disc. Logic ZERO for true
ADDSST–	Cylinder Address Strobe. This signal is used by the disc for sampling the cylinder address lines and the restore line. This signal is held until either the address acknowledge signal or the attention signal is issued by the disc. Logic ZERO for true
HS–	Head Select. This signal selects one of the two heads for the purpose of reading or writing. Logic ZERO selects upper head. Logic ONE selects lower head.
WG–	Write Gate. This signal controls the current for the write coil. Logic ZERO for current on. Logic ONE for current off.
EG–	Erase Gate. This signal controls the current for the erase coil. Logic ZERO for current on. Logic ONE for current off.
DS–	This signal selects either the fixed or the removable disc. A logic “0” selects the removable disc and a logic 1 selects the fixed disc.
WDNCLK–	Write Data and Clock. This line carries the multiplexed data and clock pulses for double frequency type recording on the disc, one complete pulse for each recorded flux reversal. The pulses should have a minimum width of 100 nanoseconds and the leading edge transition time at the disc should be less than 50 nanoseconds, negative going leading edge.
SELU(N)	Select Lines. N - 0-3. These lines select and control the input/output lines of an individual disc unit in a daisy-chain system configuration. Up to four direct select lines are provided. Logic ZERO on a line selects the disc unit associated with that line.



Table 2-6. Disc to Controller Signals

Signal	Description
FRY $\bar{}$	<p>File Ready.</p> <p>A signal on this line indicates the disc drive is in the following condition.</p> <ul style="list-style-type: none">Proper power is supplied.Disc cartridge is loaded.Door is closed.Disc is rotating at operating speed and heads are in flying position.It is not in the write check condition. <p>Logic ZERO for true</p>
RTS/R/W $\bar{}$	<p>Ready to Seek/Read/Write.</p> <p>A signal on this line indicates the disc is in the file ready condition and it is not in the process of executing a seek operation.</p> <p>Logic ZERO for true</p>
ADSACK $\bar{}$	<p>Address Acknowledge.</p> <p>A signal on this line notifies the controller that a command to move the heads to a specified address has been accepted, and execution of the command has begun. Pulswidth is 1 μsec.</p> <p>Logic ZERO for true</p>
SKIC $\bar{}$	<p>Seek Incomplete.</p> <p>This signal indicates that, due to some malfunction, a seek operation was not completed by the disc. This signal, once it becomes true, is held until a Restore command is received by the disc.</p> <p>Logic ZERO for true</p>
RCLK $\bar{}$	<p>Read Clock.</p> <p>This line carries pulses representing clock signals that have been separated from data signals during read operation of the disc. Pulswidth is 50 nanoseconds to 150 nanoseconds (100 nanoseconds nominal). The leading edge should be used as reference.</p> <p>Logic ZERO for true</p>
RD $\bar{}$	<p>Read Data.</p> <p>This line carries pulses representing data signals which have been separated from clock signals during read operation of the disc. Pulswidth is 50 nanoseconds to 150 nanoseconds (100 nanoseconds nominal). The leading edge should be used as reference.</p> <p>Logic ZERO for true</p>



Table 2-6. Controller to Disc Signals (Continued)

Signal	Description
SECTORM—	<p>Sector Marks.</p> <p>This line supplies one pulse for each of the sector slots as they pass by the sector transducer of the disc drive. The leading edge of these pulses should be used as reference. There will be 24 sector marks per revolution of the disc pack.</p> <p>Logic ZERO for true</p>
INDEXM—	<p>Index Marks.</p> <p>This line supplies one pulse per disc revolution to ensure proper sector identification. It signifies that the next sector mark following this pulse is the sector mark of the first disc sector on the track. The leading edge of these pulses should be used as reference.</p> <p>Logic ZERO for true</p>
WCHK—	<p>Write Check.</p> <p>This signal notifies the controller of the following:</p> <ul style="list-style-type: none">Due to some malfunction, the disc may not be able to perform adequate write function.Temporary voltage fluctuation has occurred without interrupting operation. <p>The controller generates an offline status if writing is attempted during this condition.</p> <p>Logic ZERO for true.</p>
WPS—	<p>Write Protect Status.</p> <p>When true, this signal indicates to the controller that the disc is under write protect condition. The controller generates a Write Protect status if writing is attempted when this signal is true.</p> <p>Logic ZERO for true</p>
ATTNX—	<p>Attention Line Unit X. X = 0-3.</p> <p>There is one attention line for each disc unit on the controller. The attention line of each unit is active even though that unit may not have been selected by the last ATI Word 1. Refer to Figure 3-11 for use of attention lines.</p>



SECTION III

THEORY OF OPERATION

3.1 GENERAL

The Moving Head Disc Controller may be assigned any channel address on the Direct Memory Access Port. The controller decodes the two-word ATI or ADAC command and, if properly addressed and in a ready condition, acquires the list words from the specified location (if required).

The controller transfers data to or from CPU memory as 16-bit words with a maximum rate of 156.2K words/second. Data transfer between the controller and the disc is in bit-serial form at a rate of 2.5M bits/second.

List operations may be chained so that the controller performs many operations with only one ATI or ADAC command issued from the CPU. The interrupt capability may be enabled or disabled in any or all of the lists. When the operation is completed (or aborted) the appropriate status of the controller and/or disc unit is stored in the memory location assigned to the channel address of the controller.

Figure 3-1 is a generalized flowchart of the controller. This flowchart shows the major logic paths followed by the control logic when executing a disc operation.

3.2 LOGIC ORGANIZATION

The Moving Head Disc Controller is divided into two major logic sections: the Block Transfer Control (BTC), and the Disc Control Logic (DCL). The reason for this division is that the BTC provides the basic interface circuitry for interfacing to the Direct Memory Access Port Expander and is available as an aid to controller design. The BTC is fully documented in the Block Transfer Controller Maintenance Manual. Therefore, only the basic operation is mentioned here.

The DCL provides the necessary read/write and seek control necessary for completing the interface of the disc to the DMAP Expander. Figure 3-2 is a block diagram of the DCL logic areas, the BTC registers, and gating pertinent to the disc controller.

3.3 BLOCK TRANSFER CONTROL

The Block Transfer Control logic section provides the circuitry required to interface to the DMAP Expander. This logic includes capabilities to perform the following functions:

1. Decode the device (channel) address bits of an ATI or ADAC Word 1 and determine whether the disc controller is being addressed.
2. Accept the Activate Word 2 if addressed by Word 1 (and the controller is not busy), and store this word in the register file.
3. Acquire the initialization list from the address specified by Activate Word 2 and save the four list words as appropriate.



4. Execute memory cycles to either fetch or store data as required by the Disc Control Logic.
5. Decrement the sector counter as indicated by the DCL, and notify the DCL when counter reaches zero.

The Block Transfer Control executes the above functions as described in the following paragraphs. Refer to the BTC Maintenance Manual for detailed information.

3.3.1 ACTIVATE WORD MONITORING. The first activate word is accepted by the BTC if the address bits (13 through 15) indicate that the disc controller is being addressed and if the DCL is not busy. If both of these conditions are true, the word is stored in Register File 1 (RF1) and bits 8, 9, 10 and 11 are presented to the DCL along with a strobe indicating the presence of a (buffered) ATI or ADAC word. If the DCL is busy, the BTC presents the first word as above, but it is not stored in the register file. In either case, the DCL decodes bits 8, 9, 10 and 11 to take the appropriate action as described in later sections.

If properly addressed by Activate Word 1, and the DCL is not busy, Activate Word 2 is accepted and stored in Register File 3 (RF3). This word is presented to the DCL along with a strobe indicating its presence. The DCL does not use this word, though the strobe is utilized by the DCL Activation Control logic. This word will be stored in RF3 until required for list acquisition.

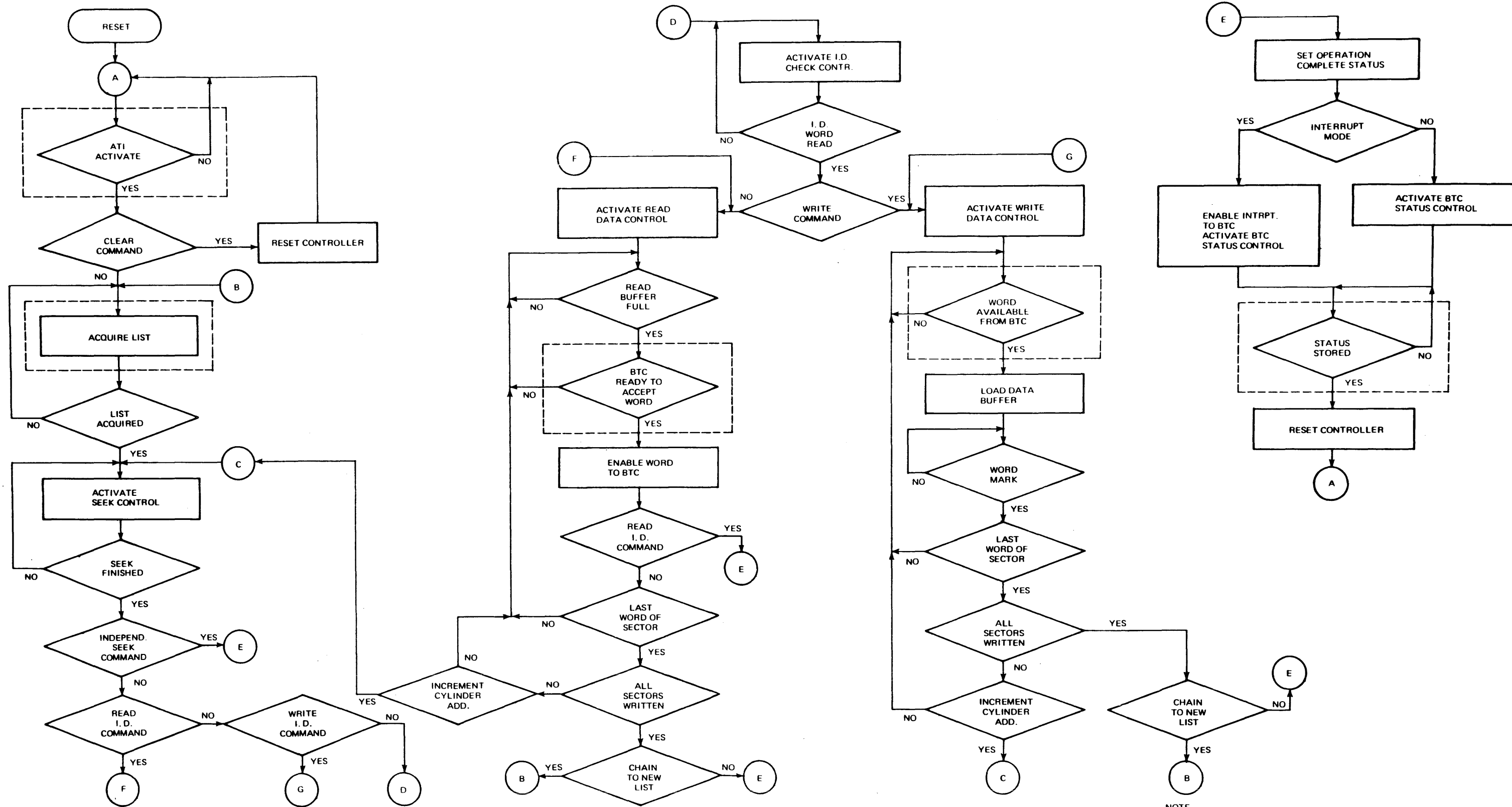
3.3.2 LIST ACQUISITION. The disc controller acquires the initialization list through activation of the BTC by the DCL. When the DCL issues a list enable (LISTEN), the BTC checks the RF4EN signal to determine where the list address is stored. RF4EN equal to a logic ZERO indicates that the list address is stored in Register File 3 (RF3). RF4EN equal to a logic ONE indicates that Register File 4 (RF4) contains the list address. RF4EN is reset to logic ZERO each time a list acquisition is initiated following an Activate 2 strobe. Thereafter, RF4EN is toggled after each list acquisition when chaining. The contents of the various registers in the BTC are outlined in table 3-1.

3.3.3 MEMORY CYCLE EXECUTION. The Disc Control Logic (DCL) indicates to the BTC whether a Read or Write command is to be executed, and whether data is to be acquired from memory or stored in memory. The appropriate memory cycle execution begins when the DCL issues a memory enable (MEMEN) to the BTC.

For a disc write operation, the BTC begins acquiring data from the starting data address (indicated by List Word 1). The BTC presents the data to the DCL as required. Register Files RF1 and RF2 are utilized as buffer storage until the DCL requests a new data word, so the BTC is normally two words ahead of the DCL. This means that two extra words are acquired by the BTC during a write operation, but this is of no consequence since they are not requested by the DCL.

For a disc read operation, the BTC begins storing data when the DCL indicates that a data word is ready to be transferred. The BTC has the capability of buffering two words from the DCL while the DCL is acquiring a third word, but normally the BTC will have stored a data word before the next word is acquired by the DCL.

3.3.4 STATUS STORAGE. A status cycle is initiated by the BTC when the DCL issues a status enable (STATEN). The status storage is preceded by an interrupt if the interrupt enable signal (INTEN) from the DCL so indicates. The DCL also indicates that two status words are to be stored (TWOSC). The first status word is supplied by the DCL, which is requested to do so by the BTC after a status cycle has been initiated. The second word, the address of the initialization list, is supplied by the BTC. Status storage memory cycles and data transfer memory cycles may be executed (interleaved) as required.



NOTE
AREAS WITHIN DASHED LINES ARE BTC
FUNCTIONS. OTHER AREAS ARE DCL FUNCTIONS.

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Figure 3-1. Disc Controller General Flowchart

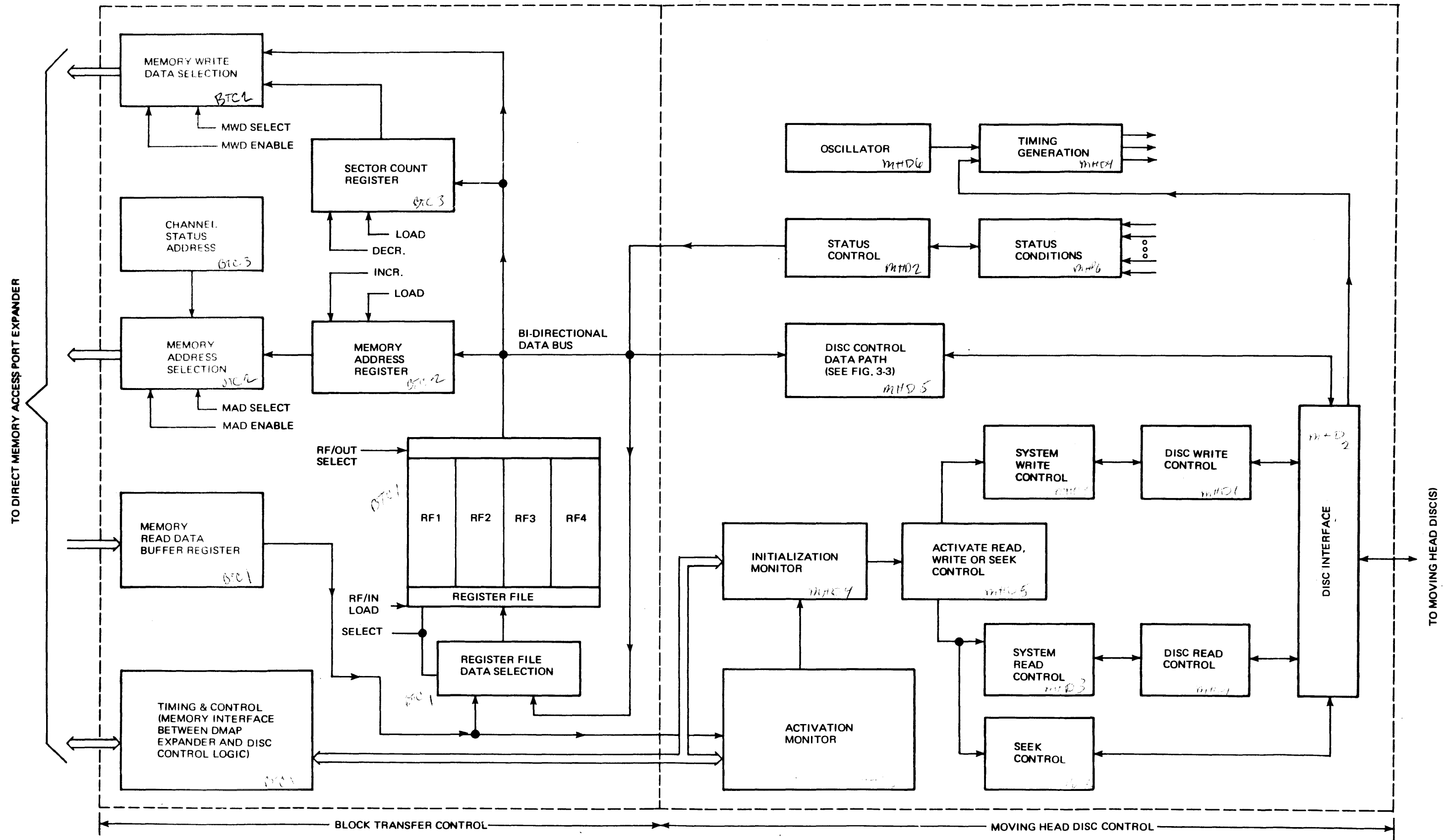


Figure 3-2. Disc Controller Block Diagram



Table 3-1. BTC Register Content

STROBE OR ENABLE (SEE NOTE 1)	RF4EN (SEE NOTE 2)	BTC REGISTER CONTENT									
		REGISTER FILE 1 (RF1)	REGISTER FILE 2 (RF2)	REGISTER FILE 3 (RF3)	REGISTER FILE 4 (RF4)	MEMORY ADDRESS REGISTER	SECTOR COUNT REGISTER				
ACTIVATE 1	_____	ACTIVATE WORD 1	_____	_____	_____	_____	_____	_____			
ACTIVATE 2	_____	ACTIVATE WORD 1	_____	ACTIVATE WORD 2 (LIST ADDRESS)	_____	_____	_____	_____			
INITIAL LIST ACQUISITION	0	ACTIVATE WORD 1	_____	LIST ADDRESS	_____	LIST ADDRESS	_____	_____			
	0	ACTIVATE WORD 1	STARTING DATA ADDRESS	LIST ADDRESS	_____	LIST ADDRESS + 1	_____	_____			
	0	SECTOR COUNT	STARTING DATA ADDRESS	LIST ADDRESS	_____	LIST ADDRESS + 2	_____	_____			
	0	DCL COMMAND WORD	STARTING DATA ADDRESS	LIST ADDRESS	_____	LIST ADDRESS + 3	SECTOR COUNT	_____			
LW4	0	DCL COMMAND WORD	STARTING DATA ADDRESS	LIST ADDRESS (CURRENT)	CHAIN (LIST) ADDRESS	STARTING DATA ADDRESS	SECTOR COUNT	_____			
MEMEN	1	_____	_____	LIST ADDRESS (CURRENT)	CHAIN (LIST) ADDRESS	STARTING DATA ADDRESS	SECTOR COUNT	_____			
CHAIN LIST ACQUISITION	1	_____	_____	LIST ADDRESS (PREVIOUS)	CHAIN (LIST) ADDRESS	(CHAIN) LIST ADDRESS	_____	_____			
	1	_____	(NEW) STARTING DATA ADDRESS	LIST ADDRESS (PREVIOUS)	LIST ADDRESS (CURRENT)	LIST ADDRESS + 1	_____	_____			
	1	SECTOR COUNT (NEW)	STARTING DATA ADDRESS	LIST ADDRESS (PREVIOUS)	LIST ADDRESS (CURRENT)	LIST ADDRESS + 2	_____	_____			
	1	DCL COMMAND WORD (NEW)	STARTING DATA ADDRESS	LIST ADDRESS (PREVIOUS)	LIST ADDRESS (CURRENT)	LIST ADDRESS + 3	SECTOR COUNT (NEW)	_____			
	LW4	1	DCL COMMAND WORD	STARTING DATA ADDRESS	CHAIN (LIST) ADDRESS	LIST ADDRESS (CURRENT)	(NEW) STARTING DATA ADDRESS	SECTOR COUNT	_____		
	MEMEN	0	_____	_____	CHAIN (LIST) ADDRESS	LIST ADDRESS (CURRENT)	(NEW) STARTING DATA ADDRESS	SECTOR COUNT	_____		

NOTES:

1. REGISTER CONTENT TRUE AT STROBE TIME OR AS A RESULT OF AN ENABLE FROM THE DCL.
2. RF4EN (REGISTER FILE 4 ENABLE) TO THE BTC IS TOGGLED UPON COMPLETION OF EACH LIST ACQUISITION; INITIALLY RESET TO LOGIC ZERO WITH EACH ACTIVATE 2 STROBE.



3.4 DISC CONTROL LOGIC (DCL)

The Disc Control Logic (DCL) provides the necessary circuitry to control the disc and execute the commands previously described. The flowchart and block diagram shown in figures 3-1 and 3-2, respectively, illustrate the general operation and organization of the DCL and the BTC. The following paragraphs describe the DCL in detail.

The DCL is comprised of eleven major subsections as follows:

- Registers
- Timing Generation
- Activation Monitor
- Initialization List Monitor
- Seek Control
- Identification Control
- System Write Control
- Disc Write Control
- System Read Control
- Disc Read Control
- Status Control

3.5 DCL REGISTERS

The DCL Registers are used to assemble/disassemble data, contain command information, and contain addressing information. Table 3-2 lists and describes the DCL Registers. Figure 3-3 shows the registers in the DCL path and figure 3-4 shows the registers associated with command and addressing.

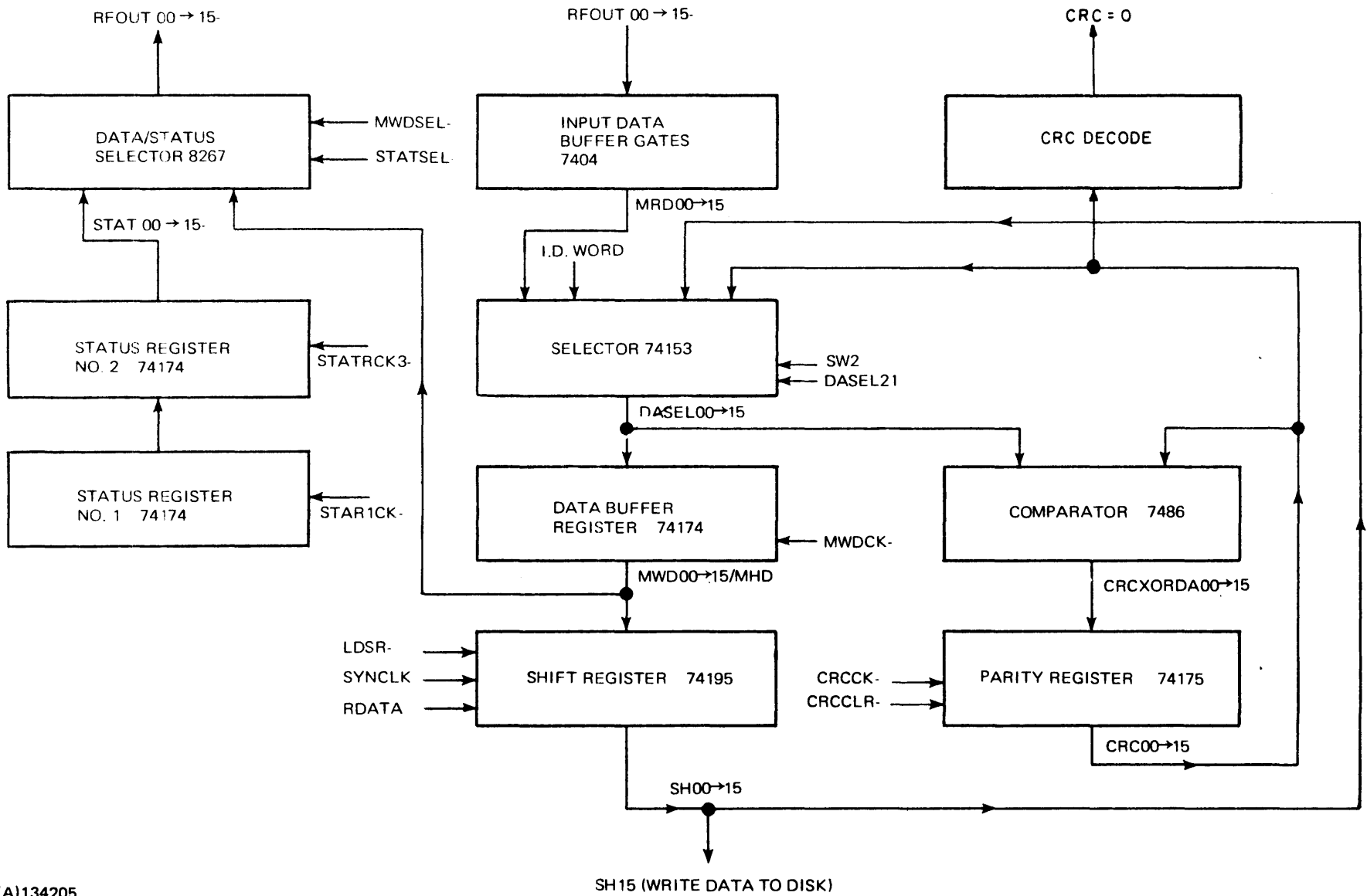
Table 3-2. DCL Registers

Register	Function
Input Data Buffer Register (MRDXX/MHD XX=00-15)	Accepts data from the BTC and provides sufficient drive for all controller register inputs to which data may be routed. Data is loaded into the appropriate register by selective clocking.
Data Buffer Register (MWDXX/MHD XX=00-15)	Provides a one-word buffer which allows the BTC to have two-word times in which to perform a data transfer between the DCL and the BTC.
Shift Register (SHXX XX=00-15)	Provides the parallel to serial conversion when writing on the disc. Provides the serial to parallel conversion when reading from the disc.
Parity Register (CRCXX XX=00-15)	Generates the parity on information being transferred to/from the disc.
Status Register (STATXX XX=00-15)	Contains the status of the controller and/or disc. The content of this register is the first status word stored.



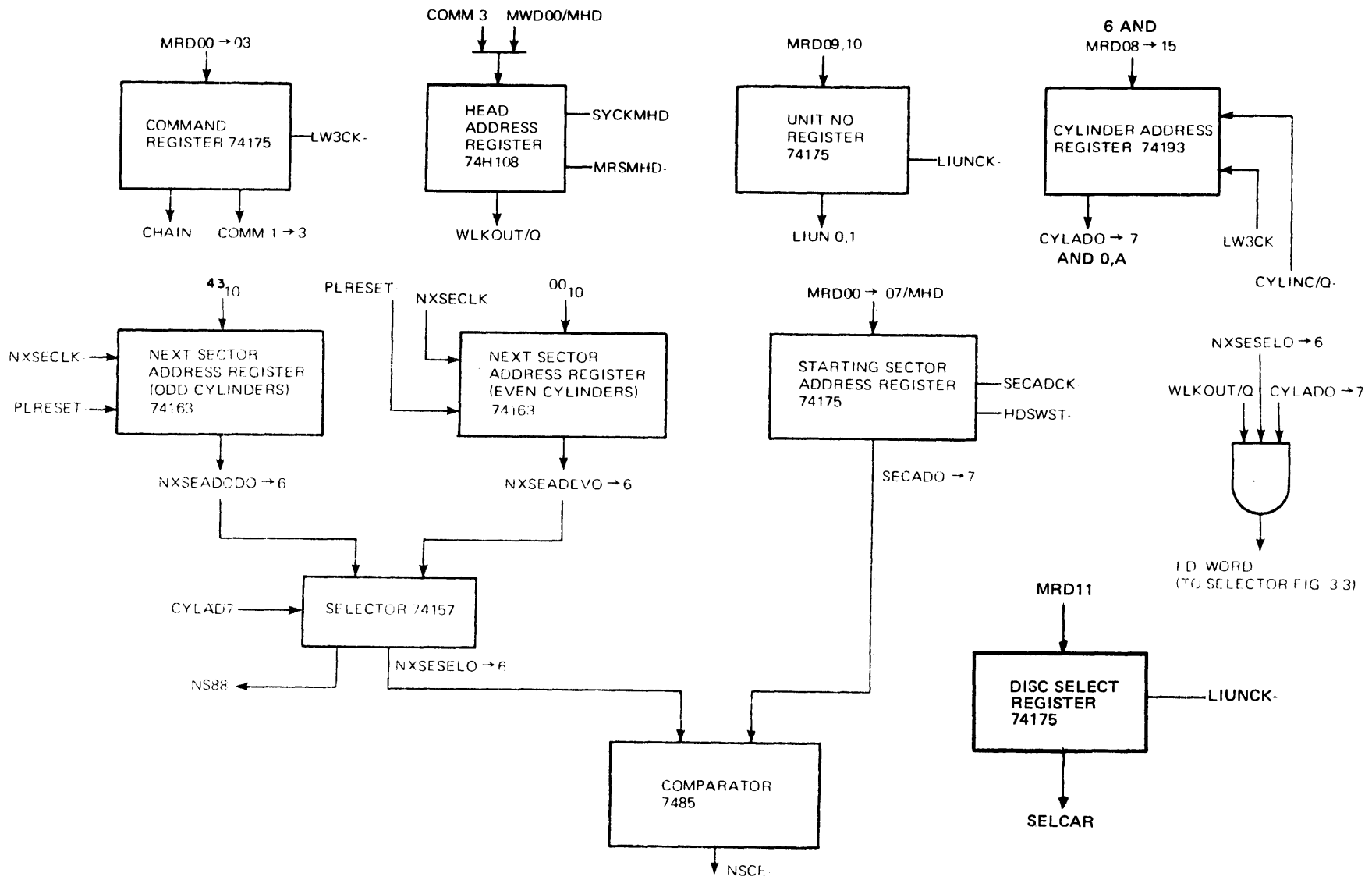
Table 3-2. DCL Registers (Continued)

Register	Function
Command Register (chain, commx X=1-3)	Loaded with bits 0 through 3 of List Word 3. This register determines what type of operation the controller will perform. (Read, Write, Seek, etc.)
Head Address Register (UPHD/Q)	Loaded with bit 7 of List Word 3. This register determines which surface of the disc the controller will read/write.
Cylinder Address Register (CYLADX X=0-7 and 0, A)	Loaded with bits 6, and 8 through 15 of List Word 3. This register determines which cylinder of this disc the controller will read/write/seek. This register is incremented at the occurrence of an automatic cylinder increment. (See figure 2-3.)
Unit Number Register (LIUNX X=0-1)	Loaded with bits 9 and 10 of ATI or ADAC Word 1. Selects the disc unit which will be read/written/seeked.
Disc Select Register (SELCAR)	Loaded with bit 11 of ATI or ADAC Word 1. Selects the disc (fixed or removable) which will be read/written/seeked.
Sector Address Register (SECADX X=0-6)	Loaded initially with bits 1 through 7 of List Word 2. Contains the sector address at which reading/writing will begin. This register is reset to zero during an automatic track increment. (See figure 2-3.)
Write Lockout Register (WLKOUT/Q)	Loaded with bit 3 of List Word 3 for a Write I.D. command. Loaded with bit 0 of the I.D. word for a Read or Write Data command. Determines whether or not data is write protected.
Next Sector Address Register (even cylinders) (NXSEADDEVX X=0-6)	Contains the address of the next sector which will come under the read/write head on the disc. Used for even numbered cylinders. (See figure 2-3.)
Next Sector Address Register (odd cylinders) (NXSEADODX X=0-6)	Contains the address of the next sector which will come under the read/write head on the disc. Used for odd numbered cylinders. (See Figure 2-3.) This register runs 180° out of phase with the N.S.A. Register for even cylinders. When the N.S.A. Register for even cylinders contains 00 ₁₀ , this register contains 44 ₁₀ .
Independent Seek in Progress Register (SKNGX/Q X=0-3)	This 4-bit register (1-bit for each disc unit) indicates which disc unit(s) are performing an independent seek.



(A)134205

Figure 3-3. DCL Registers, Data Path



(A)134206

Figure 3-4. Command and Sector Addressing Registers Block Diagram



3.6 TIMING GENERATION

The sector pulses which segment the disc surface into 89 sectors are provided by the Sector Pulse Generator (SPG). The SPG consists of a phase-locked loop (PLL) which generates a high-frequency signal of approximately 1.5 MHz synchronized to the disc speed and a counter which divides the high frequency down to the sector pulse frequency. Figure 3-5 is a block diagram of the SPG.

3.6.1 PHASE-LOCKED LOOP. The phase-locked loop (PLL) is a frequency feedback system comprised of a phase comparator, a filter, and voltage-controlled oscillator (VCO). In addition, a frequency divider may be inserted in the feedback path for frequency multiplication application such as is required in the SPG.

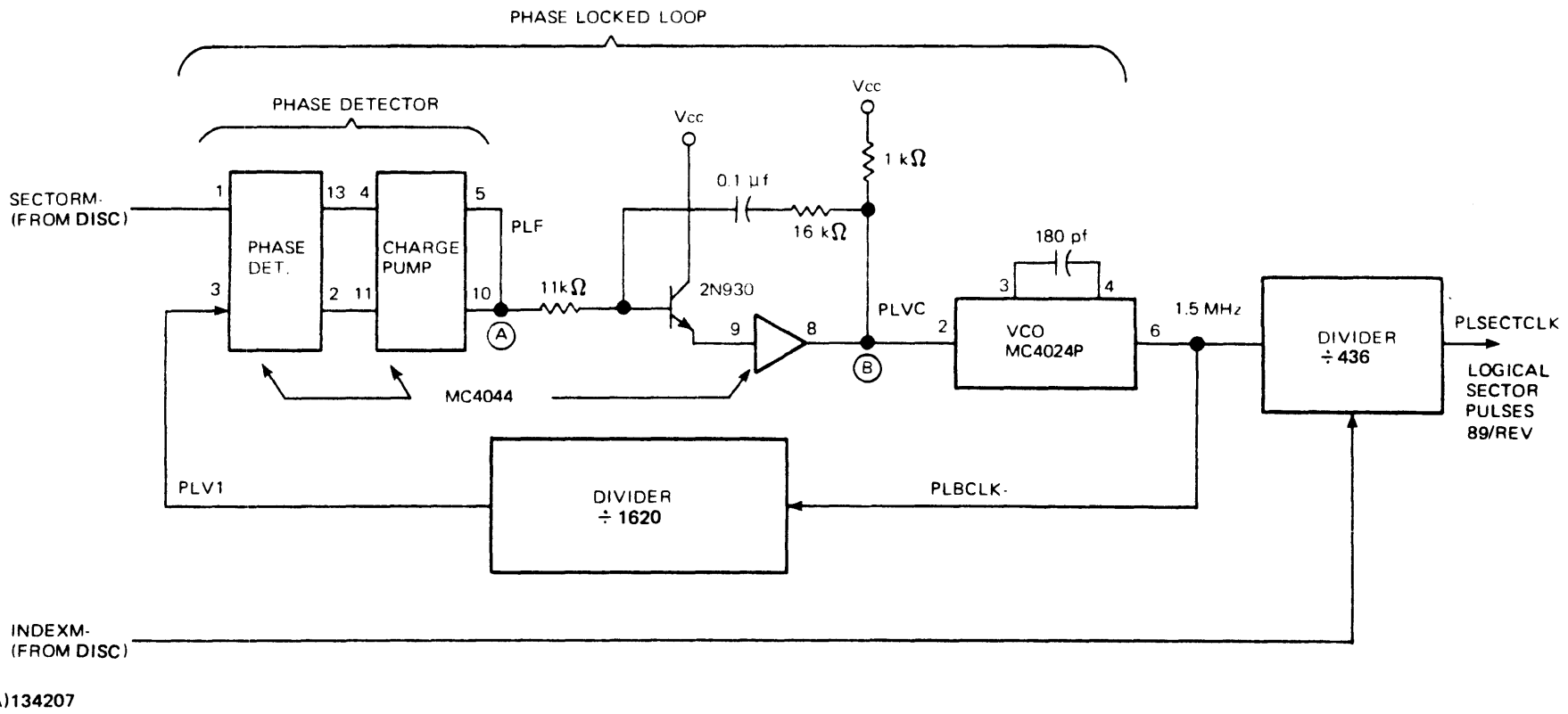
The PLL basic principle of operation is briefly explained as follows. With no signal input applied to the system, the error voltage at the input of the VCO (PLVC) is essentially zero and the VCO operates at its free-running frequency. If an input is applied to the system, the phase detector compares the phase and frequency of the input (SECTORM-) with the frequency (PLV1) of the feedback path (the VCO frequency divided by the feedback counter). It then generates an error voltage which is related to the phase and frequency difference between the two signals.

This error voltage (PLF) is then filtered, amplified, and applied to the control input of the VCO. The phase detector is designed so that the error voltage causes the VCO to move in a direction which decreases the phase and frequency difference at the phase detector. When the input frequency is sufficiently close to the feedback frequency, the PLL locks or synchronizes to the input frequency and continues to track the input for small frequency or phase deviations. The lock-on and transient characteristics of the PLL are determined by the phase detector, filter, and VCO characteristics.

3.6.2 SECTOR PULSE GENERATOR DETAILS. The moving head disc drive, TI Part Number 973780-0008, provides 24 sector pulses and 1 index pulse per revolution from the disc hub. The speed of the disc is 2400 rpm $\pm 2\%$. Additionally, there is a ± 29 microsecond variation in the sector pulses from the disc due to manufacturing tolerances. The purpose of the SPG is to utilize the sector and index pulses from the disc to derive 89 sector pulses per disc revolution with less than a ± 10 microsecond variation from actual physical disc locations.

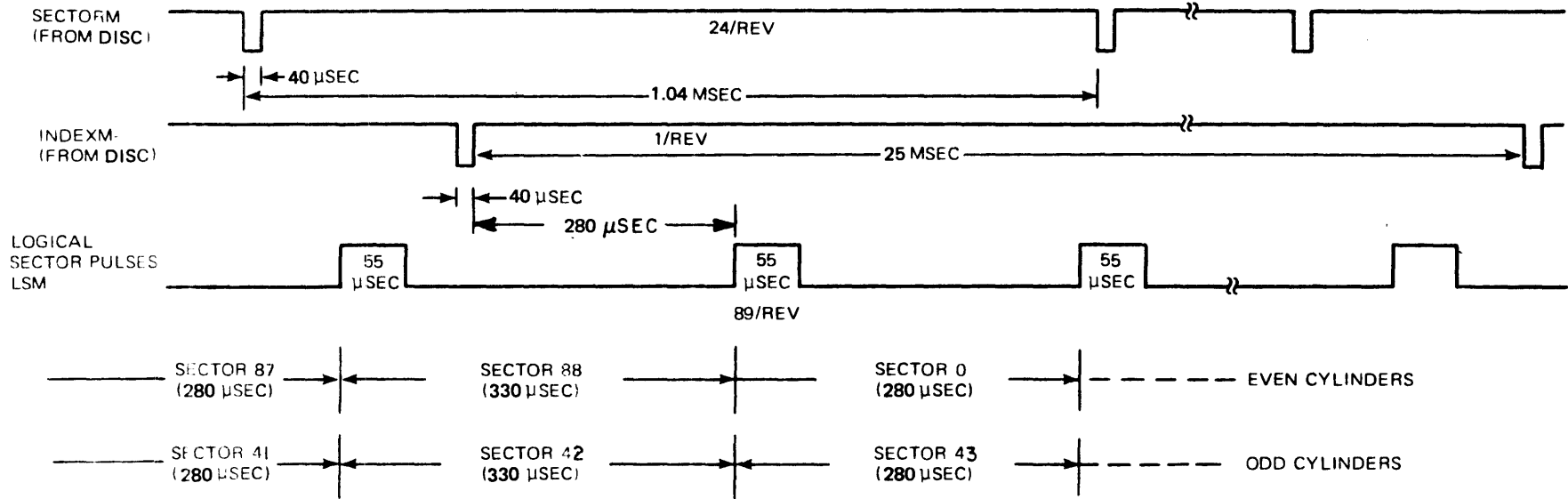
The PLL components of the SPG consist of an MC4044P phase detector and amplifier integrated circuit, and an MC4024P VCO integrated circuit. The PLL circuit and counters are shown in figure 3-5. The blocks labeled 'Phase Det.' and 'Charge Pump' form the complete PLL phase detector. The output of this section, A, is a signal (PLF) that is normally between 2 and 3 volts with 0.7 volt (0 to 10 microseconds wide) positive and negative pulses superimposed. These pulses are the error-correction pulses produced by the phase detector due to a phase or frequency error at its inputs. The active filter formed by R1, C1, R2, T1, and the amplifier in the MC4044 amplify and filter this signal to provide a nominal 4.0-volt control voltage, B, for the VCO (MC4024). This control voltage also has superimposed error pulses. When viewed on an oscilloscope, these pulses occur immediately before or after the negative transition of the input signal at the phase detector. The component values in the active filter are chosen to allow the PLL to lock and settle to less than 5 percent in approximately 8 milliseconds with less than 15 percent overshoot. The loop bandwidth in this configuration is 1 KHz.

Figure 3-6 shows the typical timing relationship of the SPG signals. The SPG logic is designed to ensure synchronization and validity of logical sector pulses and sector addresses during startup and disc drive unit switching.



(A)134207

Figure 3-5. Sector Pulse Generator Block Diagram



NOTES:

- 1. SECTOR 88 CONTAINS NO DATA AND IS USED FOR HEAD SWITCHING
- 2. ALL OTHER SECTORS CONTAIN 32 DATA WORDS, 1 PREAMBLE WORD, AND 1 PARITY WORD.
- 3. ABOVE TIMING IS NORMAL CASE; HOWEVER, DURING FIRST REVOLUTION AFTER ADDRESSING A DIFFERENT DISC UNIT (INDEXM-) MAY OCCUR RANDOMLY.
- 4. ALL SECTORS ARE NOMINALLY 280μSEC EXCEPT SECTOR 88 ON EVEN CYLINDERS AND SECTOR 43 ON ODD CYLINDERS WHICH ARE 320μSEC
- 5. ABOVE TIMING IS NOT TO SCALE AND IS FOR REFERENCE ONLY. INDICATED DELAYS MAY VARY DUE TO DISC SPEED AND COMPONENT VARIATIONS.

(A)134208

Figure 3-6. Sector Pulse Generator Timing Diagram



3.7 ACTIVATION MONITOR

Refer to figure 3-7. The function of the Activation Monitor is to take appropriate action when an activate strobe is received from the BTC. When an Activate Word (AT11) strobe is received, the DCL decodes bits 8, 9, 10 and 11 of the word. If the activate word is not a Clear command, and the controller is not busy, bits 9, 10 and 11 are loaded into the Unit Number Register (LIUNO&1) and the Disc Select Register (SELCAR).

The BTC will not send an Activate Word 2 (AT12) strobe if the DCL is busy processing another list. When an Activate Word 2 strobe is received by the DCL, it activates the list acquisition control logic in the BTC (LISTEN-) and selects Register File 3 for the list address by setting RF4EN to a logic ZERO.

3.8 INITIALIZATION LIST MONITOR

Refer to figures 3-8 and 3-9. List word strobes will not be sent by the BTC if the DCL is already processing another list.

List Word 1 (List 1) strobe is not monitored by the DCL since it is the starting data address and is saved in a BTC register.

Only the first 8 bits of List Word 2 are saved by the DCL (the interrupt bit and the starting sector address field). The least significant 8 bits (sector count) are saved in a register in the BTC. That register is decremented by the DCL, and the BTC notifies the DCL when it has decremented to zero.

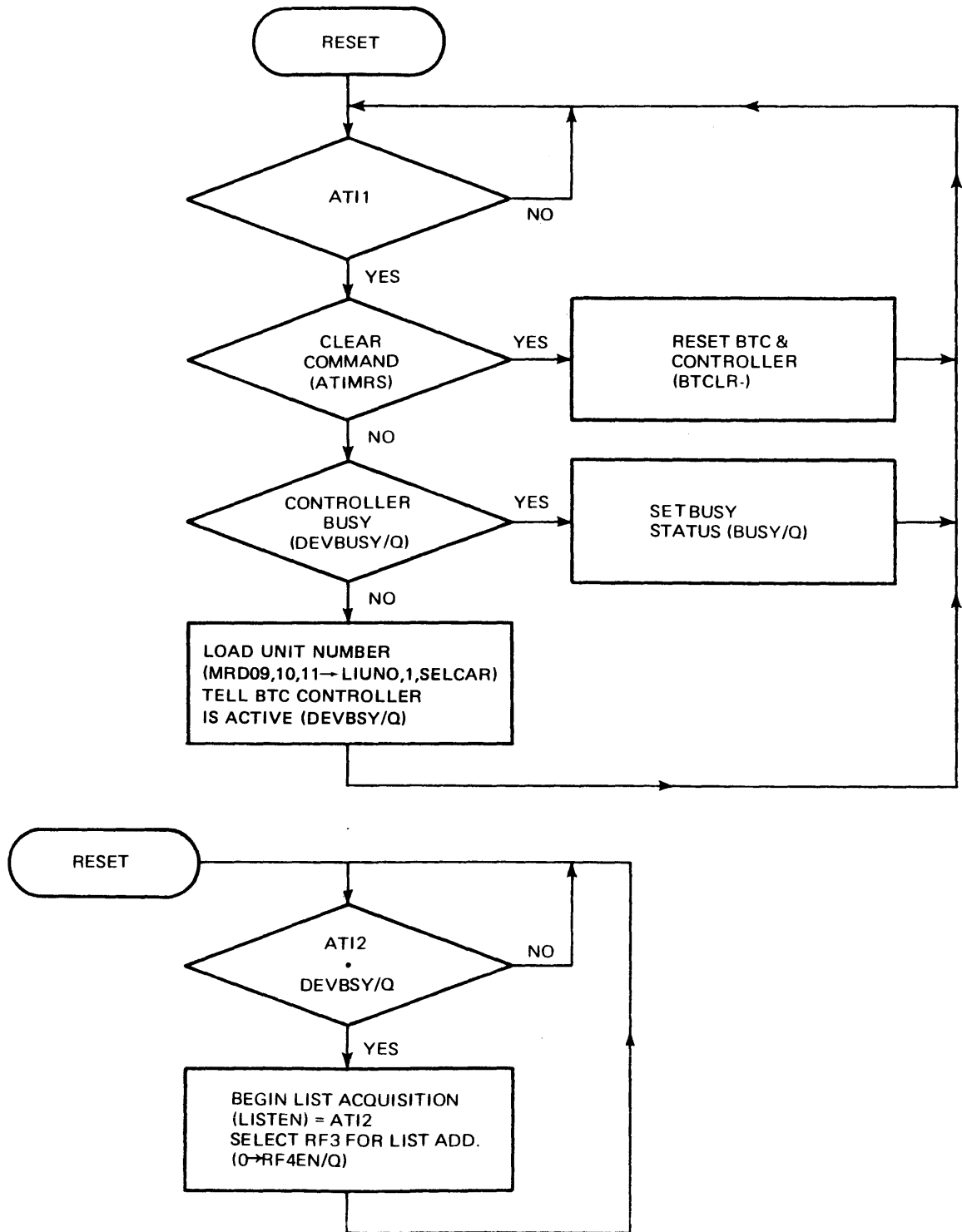
When List Word 3 (LIST 3) strobe occurs, the DCL loads bits 0 through 3 into the Command Register, bit 7 into the Head Address Register, and bits 8 through 15 into the Cylinder Address Register.

Assuming there is no program error in List Word 2, List Word 4 (LIST 4) strobe activates the BTC data control logic (MEMEN). Also, at this time the Chain List Taken status is set (if applicable) and the Command Register activates the DCL Read, Write, and/or Seek Control Logic.

3.9 SEEK CONTROL

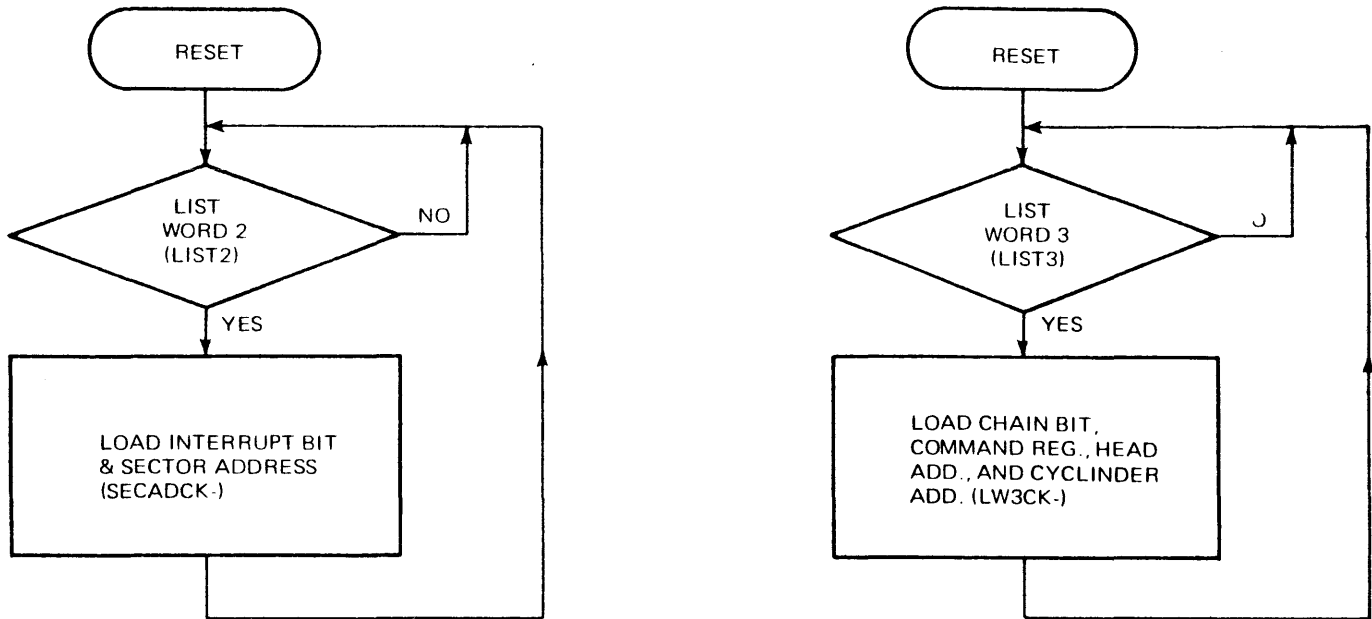
Refer to figure 3-10. The purpose of the Seek Control Logic is to initiate and complete seek operations on the disc (i.e., move the head to the desired cylinder). If there is no error in List Word 2, List Word 4 strobe activates the Seek Control Logic.

3.9.1 SEEK STATE 0 (SK0). SK0 determines whether to initiate a seek on the disc by monitoring several control signals from the disc. If the seek cannot be performed, appropriate status bits are set, status is stored, and the controller resets to its idle condition. If the seek can be performed, SK0 determines if it is to be an ordinary seek or a restore (return the head to cylinder zero). A restore is caused by an invalid cylinder address or a malfunction during a seek.



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Figure 3-7. Activation Monitor



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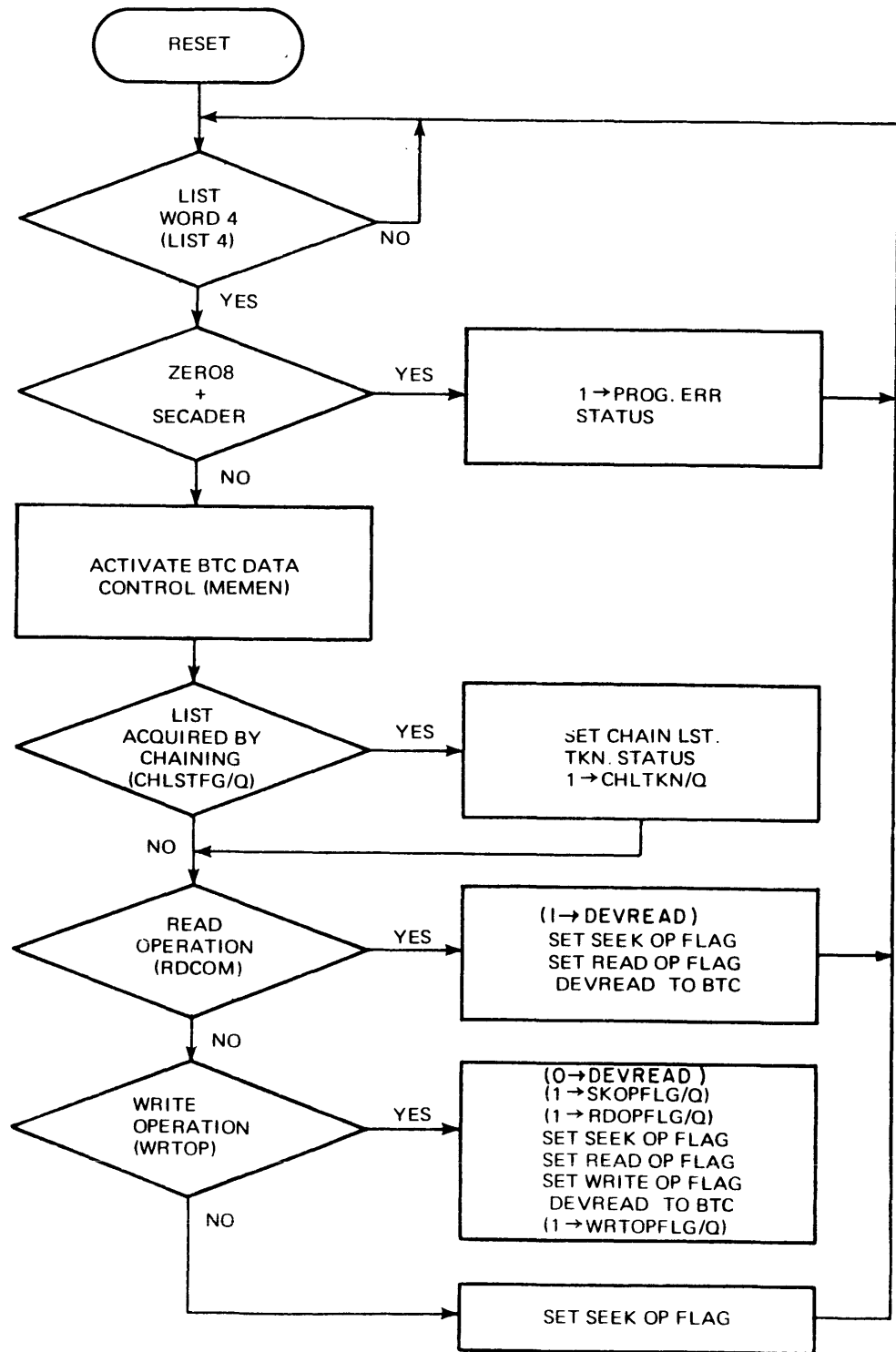
Figure 3-8. Initialization List Monitor (List Word 2, List Word 3)

3.9.2 **SEEK STATE 1 (SK1/Q)**. During SK1, an address strobe (ADSST) is sent to the disc telling it to take the cylinder address which is on the lines. One of the following occurs while in SK1 (refer to figure 3-11):

1. The disc accepts the cylinder address and returns an address acknowledge (ADSACK/Q).
2. The disc does not accept the cylinder address (invalid address) and issues a pulse on the attention line (ATTN) causing a logical address interlock (LAIL).
3. The head is at the desired cylinder and the disc issues a pulse on both the address acknowledge line and the attention line.

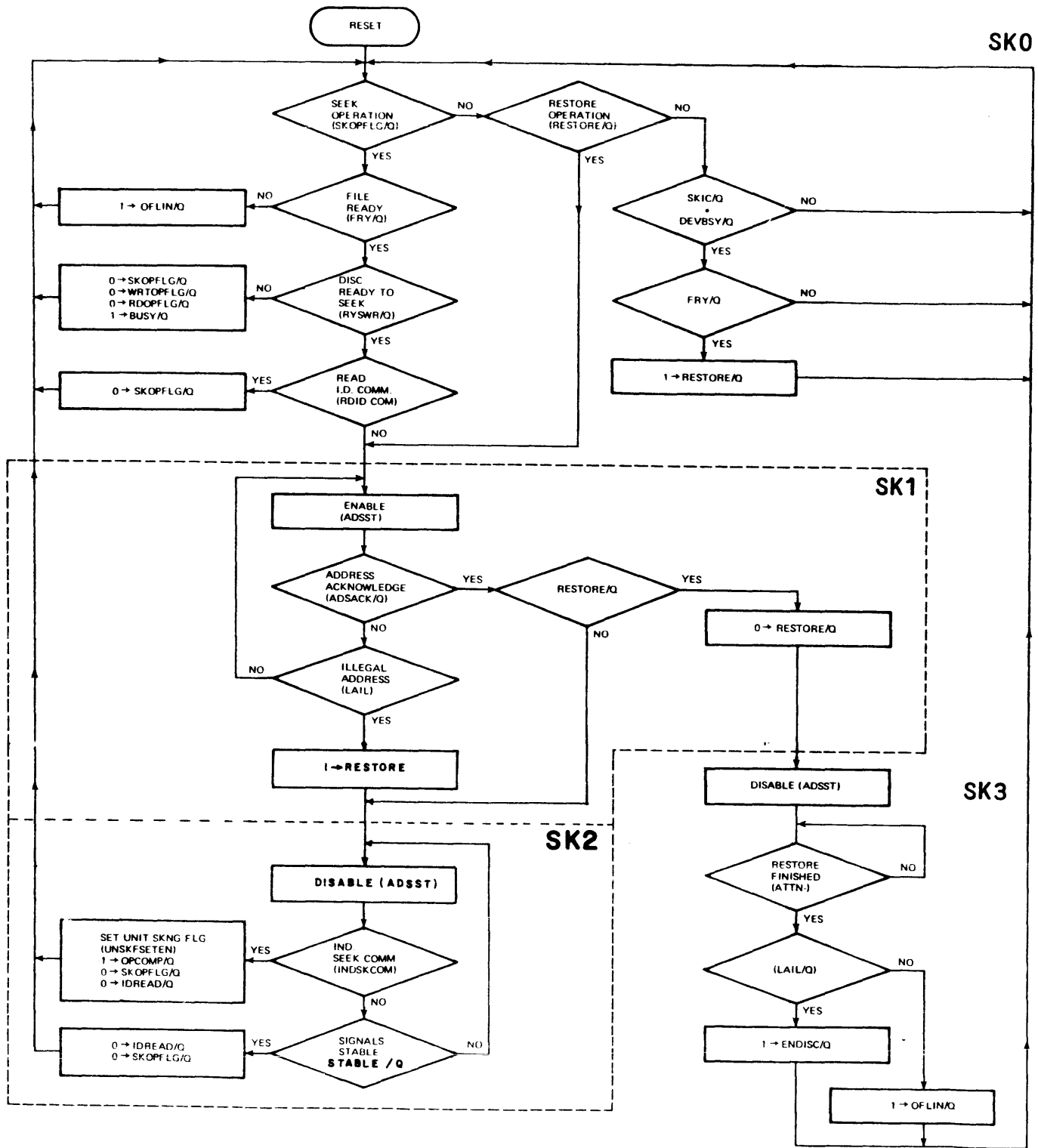
3.9.3 **SEEK STATE 2 (SK2/Q)**. The function of SK2 is to initiate a restore operation if a LAIL occurred in SK1, activate the independent seek monitor if the command was an Independent Seek, or synchronize the Disc Read Control Logic to the disc by waiting for the trailing edge of a logical sector mark before turning off the Seek Control Logic.

3.9.4 **SEEK STATE 3 (SK3/Q)**. The function of SK3/Q is to determine when a restore operation has been completed by the disc. If the restore operation was due to a LAIL, the End of Disc status is set. Otherwise, the restore was initiated due to a malfunction by the disc during a previous seek and the OFF Line status is set.



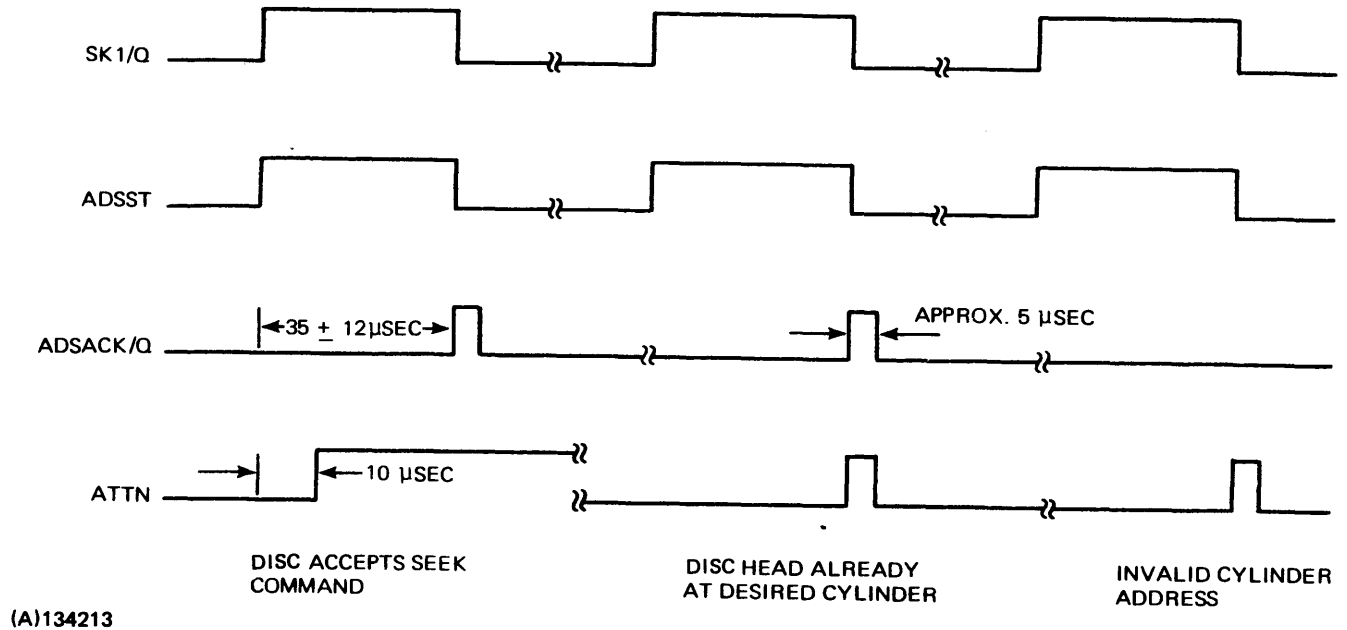
(A)134211

Figure 3-9. Initialization List Monitor (List Word 4)



(A)134212

Figure 3-10. Seek Control



(A)134213

Figure 3-11. Disc Response to Seek Command

3.9.5 INDEPENDENT SEEK MONITOR (ISM). Refer to figure 3-12. If a valid Independent seek is initiated in SK1, SK2 sets the independent seek in progress bit (SKNGX/Q, X=0→3) of that unit. When a disc completes an Independent Seek, the ISM sets the Independent Seek Finished status for that unit (SKFINX/Q, X=0→3). The occurrence of an Independent Seek Finished status causes an immediate status storage cycle whether or not the controller is active. An Interrupt precedes the status storage only if interrupts were enabled by the last List Word 2 that was received by the controller. It is possible for more than one disc unit to be seeking while a data transfer is occurring on another unit.

3.10 IDENTIFICATION WORD VERIFICATION

The I.D. word verifies that the disc has seeked to the correct cylinder. The controller performs an I.D. check prior to every read or write operation and if an automatic cylinder increment occurs while reading or writing. The I.D. check logic is included in the System Read and Disc Read Control Logic.

3.10.1 SYSTEM READ STATE 0 (SR0). List Word 4 (LIST 4) strobe activates the System Read Controller if a read or write operation is going to be performed. Once activated, SR0 monitors the Seek Controller. When the Seek Controller has finished and the Command Register indicates a read data or write data operation and the I.D. word has not been checked, SR0 initiates an I.D. check cycle by sending a start signal (DRSRTF/Q) to the Disc Read Control Logic. When the Disc Read Controller reaches State 2 (DR2), the desired I.D. word (Cylinder Address Register, Head Address Register, next Sector Address Register) is loaded into the Parity (CRC) Register. (Refer to figure 3-22.)

3.10.2 SYSTEM READ STATE 1 (SR1/Q). SR1 waits for the I.D. word to be read and loaded into the Data Buffer Register and the Parity Register. (Refer to figure 3-13.) When the buffer contains a word, indicated by BUFFUL/Q, the next system clock turns off SR1/Q.

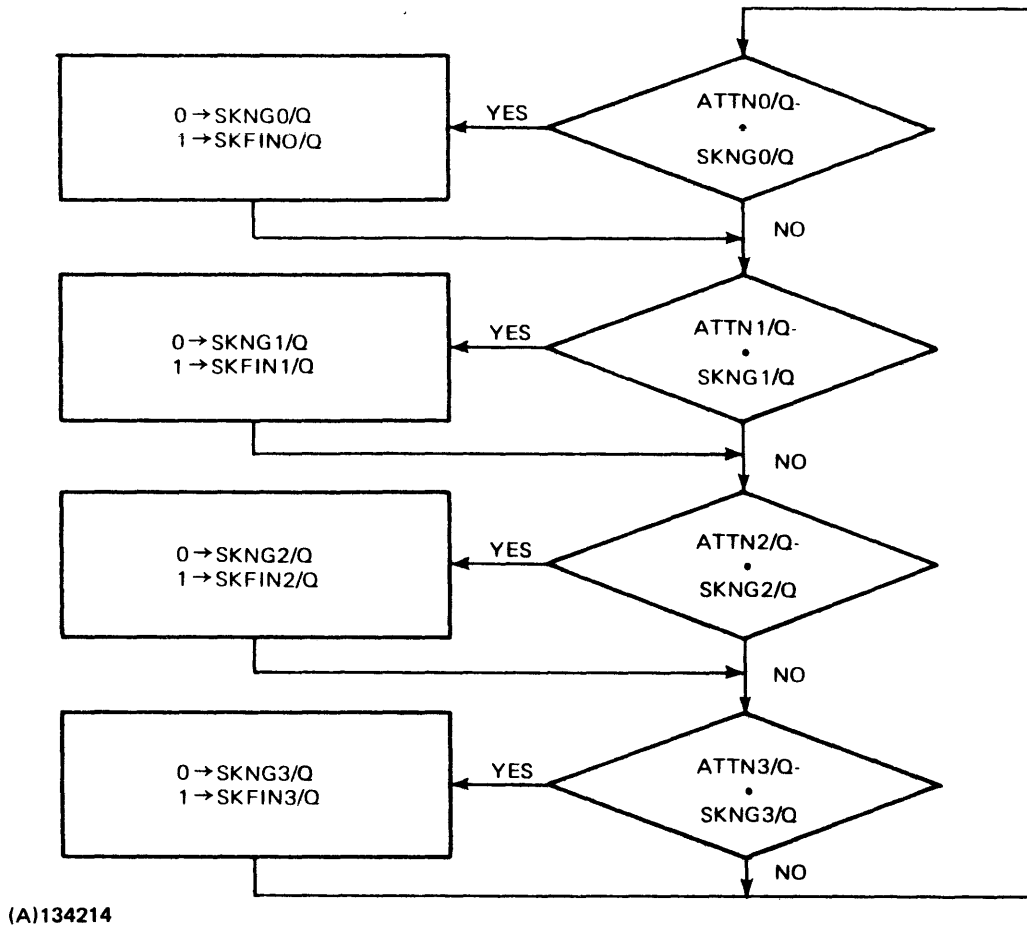
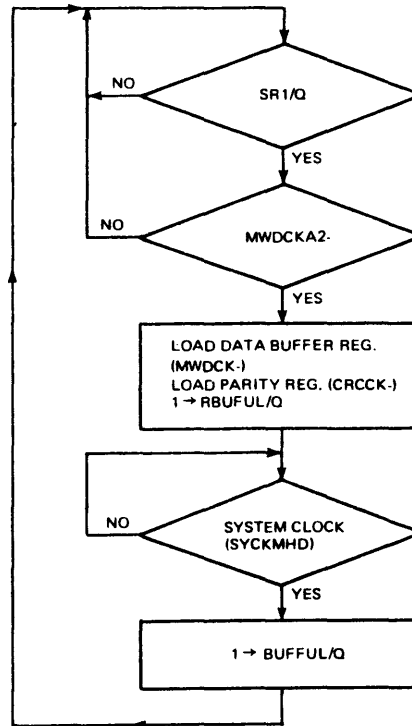


Figure 3-12. Independent Seek Status Monitor

3.10.3 SYSTEM READ STATE 2 (SR2/Q). SR2 waits for the word mark to go away before continuing. This is to ensure that the system control stays in synchronization with the disc control. The content of the Parity Register is then examined. If it is zero, the I.D. word read from the disc was correct. However, if the Parity Register is nonzero, the I.D. Compare Error status is set. An I.D. Compare Error status only terminates a write data operation. Otherwise, processing continues. (Refer to figure 3-24, sheets 1 and 3.)

3.11 SYSTEM WRITE CONTROL

The System Write Control Logic is activated during List Word 4 strobe if the command is a Write or Compare command. Once activated, System Write State 0 (SW0) monitors the System Write Control to determine when to start the write operation. The Read Controller remains active until the disc has completed a seek operation and the I.D. has been verified. The I.D. will be checked if the command is a Write Data or Compare Data but not if it is a Write I.D.



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Figure 3-13. General Flowchart, Data Buffer Register and Parity Register Loading When Reading

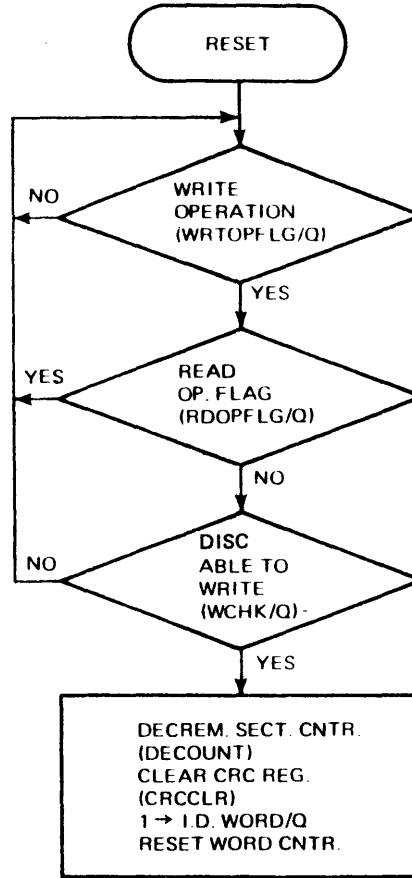
3.11.1 **SYSTEM WRITE STATE 0 (SW0)**. Refer to figure 3-14. When the Read Controller turns off and if the disc is ready, the sector counter in the BTC is decremented. The Parity Register and the word counter are cleared. The I.D. word/Q flip-flop inhibits incrementing the word counter when the I.D. word is written. Refer to the timing chart in figure 3-15.

3.11.2 **SYSTEM WRITE STATE 1 (SW1/Q)**. During SW1, a start signal is sent to the Disc Write Controller (if writing on the disc) or to the Disc Read Controller (if reading from the disc). The I.D. word to be written (or compared) is loaded into the Data Buffer Register. The word mark received indicates that the Disc Write Controller (DRC if comparing) has taken the I.D. word from the Data Buffer Register and loaded it in the Shift Register. (Refer to figure 3-14.)

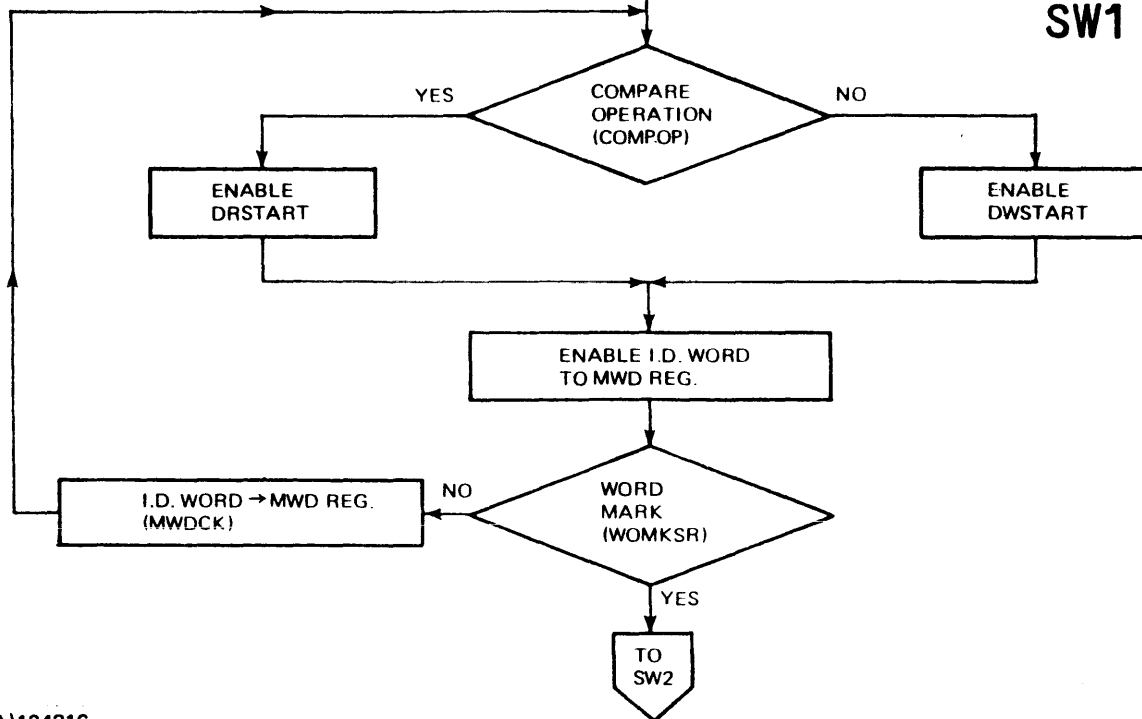
3.11.3 **SYSTEM WRITE STATE 2 (SW2/Q)**. Refer to figure 3-16. The System Write Controller remains in SW2 until all the data words and the parity word for that sector have been written. WS2 obtains the data words from the BTC and holds them in the Data Buffer Register until the disc controller loads the word into its Shift Register. Each time a word mark (WOMKSR/Q) is received from the disc controller, a word has been taken from the Data Buffer Register and loaded into the Shift Register. The next data word is then fetched from the BTC. This process continues until the parity word has been loaded into the Shift Register. At this point, the System Write Controller steps to System Write State 3 (SW3/Q). If a word is not available from the BTC by the time the disc controller is ready for it, a Data Transfer Error status will be set.



SW0



SW1

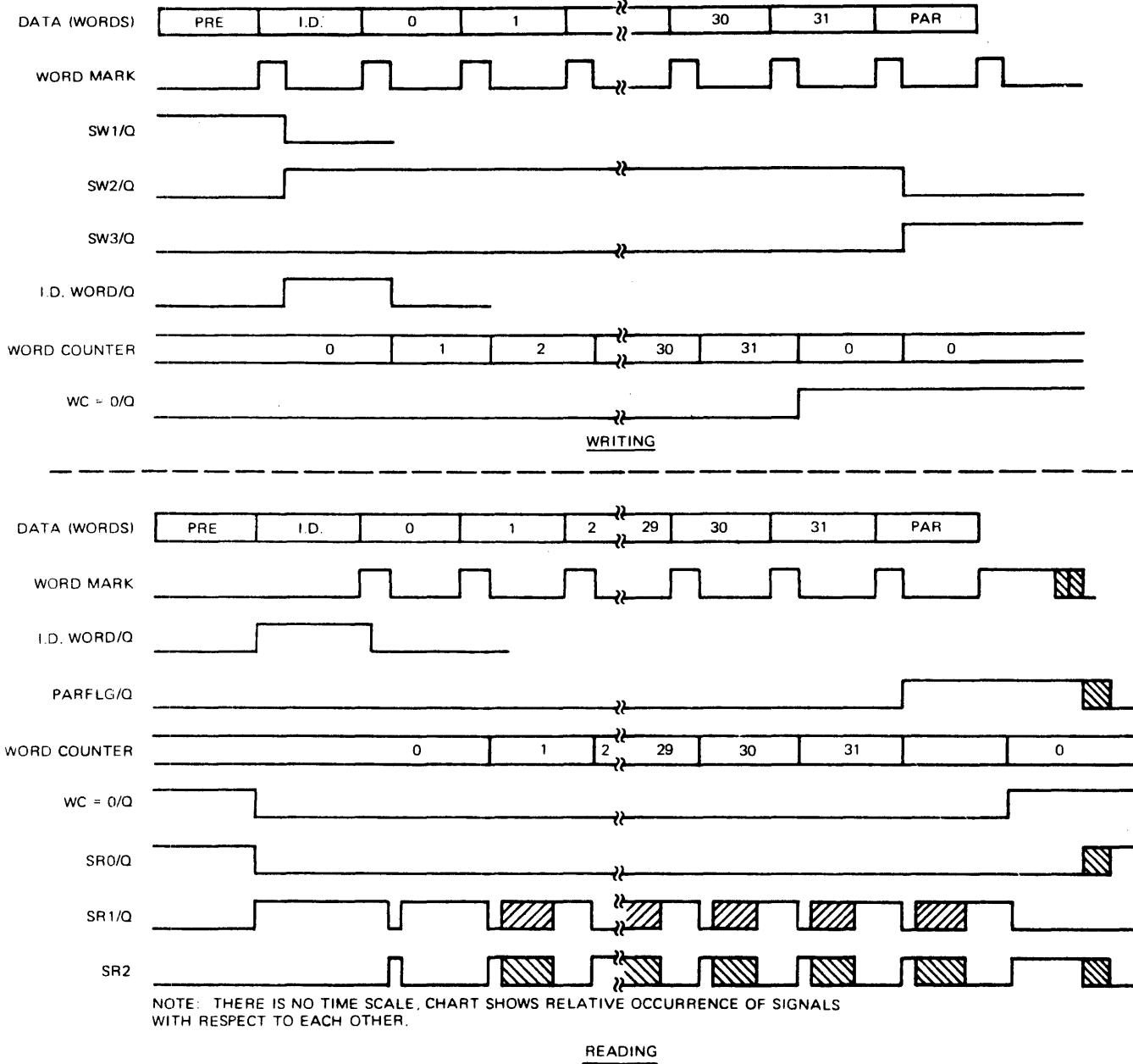


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Figure 3-14. System Write Control, States 0 and 1



944824-9701

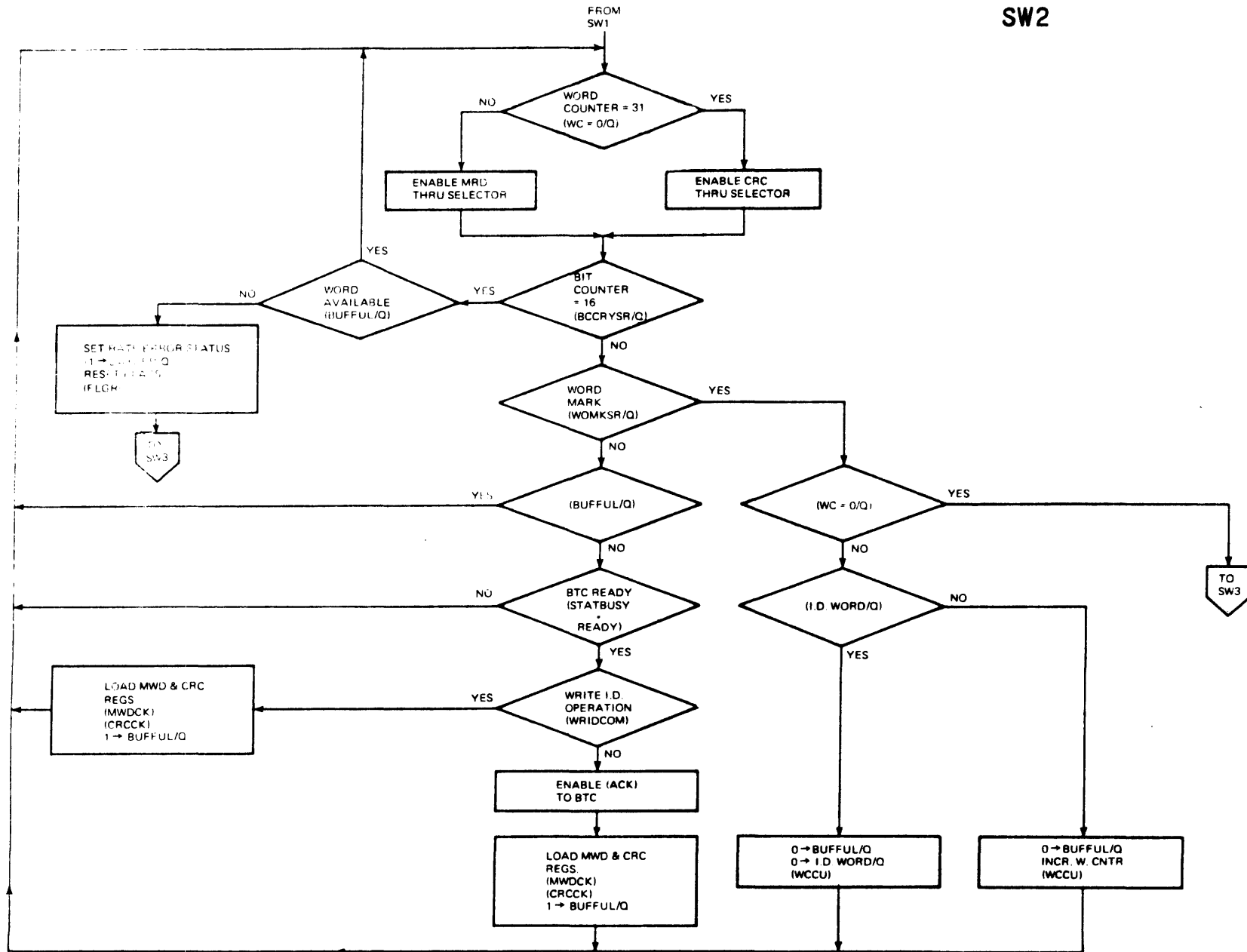


(A)134217

Figure 3-15. Timing Chart, System Read and Write Controller



SW2



(A)134218

Figure 3-16. System Write Control, State 2



3.11.4 SYSTEM WRITE STATE 3 (SW3/Q). Refer to figure 3-17. SW3 determines if the operation is to be aborted (due to data transfer error or compare error), continued (ZERO8 or CHAIN), or is complete (ZERO8 and CHAIN). If the operation is to be continued (or is finished), SW3 waits for the disc controller to return to its initial state (DR0 and SW0) before continuing. This is to ensure that the system controller stays in synchronization with the disc controller. If all the sectors have not been written (or compared), the system returns to SW0 and the process is repeated. Once all the sectors have been written (compared), the controller chains to a new list (if required) or sets Operation Complete status.

3.12 DISC WRITE CONTROL

The Disc Write Controller provides the necessary circuitry to control the disc when writing. It depends on the System Write Control to furnish data at the proper time and to activate and stop it. Whereas all System Control Logic is synchronized to the CPU (system) clock, all Disc Read and Write Control Logic is synchronized to a clock generated by a crystal oscillator in the controller. The oscillator clock is a square wave signal with a 400-nanosecond period (BITCK).

3.12.1 DISC WRITE STATE 0 (DW0/Q). Refer to figure 3-18. Once a start signal (DWSRTF/Q) is received from the system controller, DW0 waits for a logical sector mark. After the LSMF/Q is seen, DW0 must determine if it should write that sector. EQUAL/Q means that at least one sector has been written, but the BTC sector counter is not zero. NSCE means that the next sector is the starting sector at which writing begins. EQUAL/Q, the Write Gate and the Erase Gate Delay are turned on when exiting DW0. The Erase Gate Delay ensures that the Erase Gate and Write Gate are turned on at the same physical point on the disc. Refer to the Diablo Maintenance Manual for details.

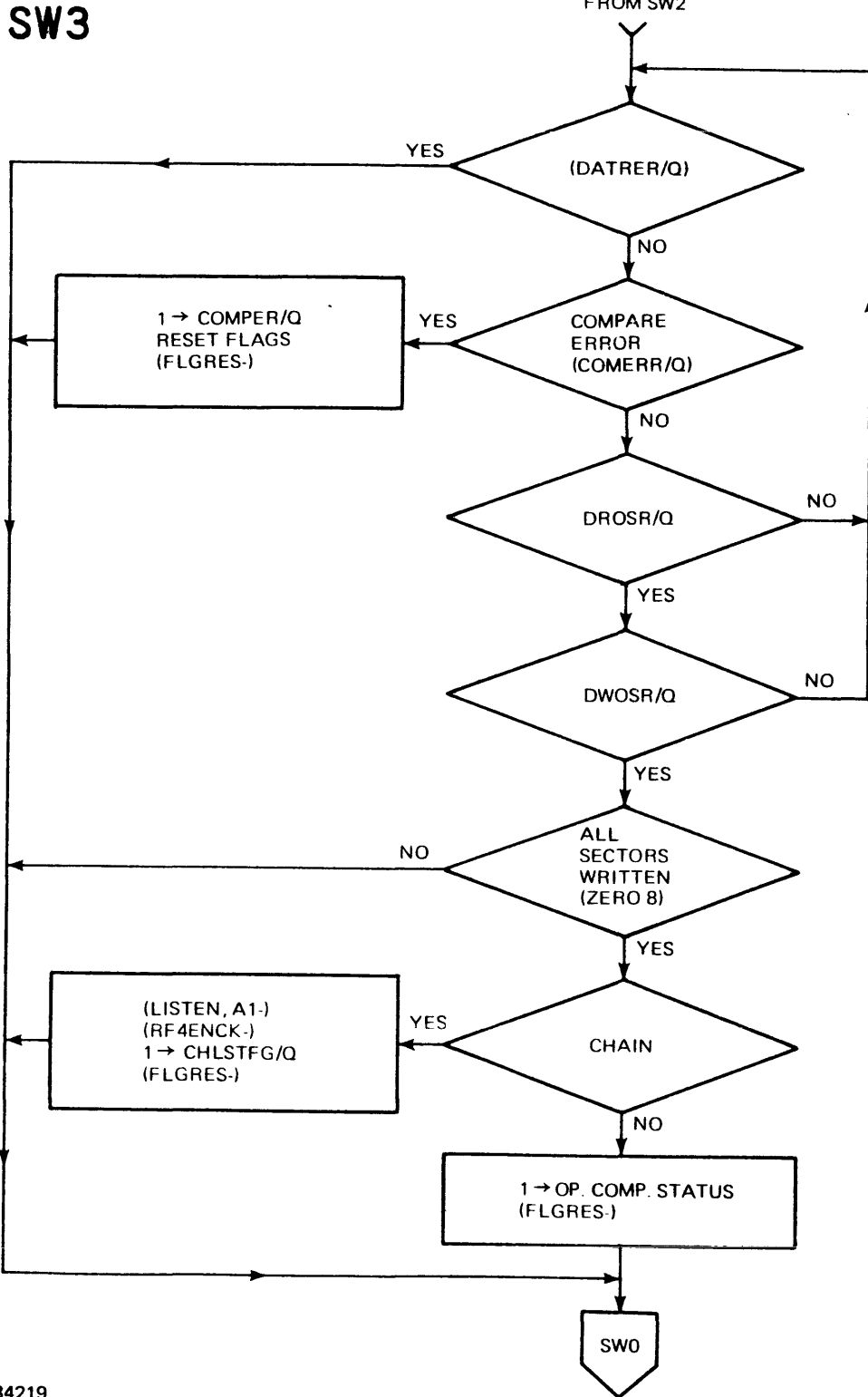
3.12.2 DISC WRITE STATE 1 (DW1/Q). Refer to figure 3-19. When the Erase Gate Delay times out (20 ± 5 milliseconds), the Erase Gate turns on the disc until the logical sector mark signal disappears (LSMF/Q will be 55 milliseconds). When LSMF/Q drops, the Disc Write Control steps to DW2/Q.

3.12.3 DISC WRITE STATE 2 (DW2/Q). Refer to figure 3-20. All the words in the sector (preamble, I.D., data, and parity) are written while in DW2. The preamble word is 15 zeros followed by a 1. When writing the I.D., data, and parity words, the least significant bit is written first. The controller multiplexes the data and the data clock (both data and clock are written on the disc). See figure 3-20. After each word is written, DW2 checks if the System Write Control is still in SW2. If the System Write Control has gone to SW3, the sector has been written. DW2 then writes one more clock pulse (this is required when reading) and steps to DW3.

3.12.4 DISC WRITE STATE 3 (DW3/Q). Refer to figure 3-21. If all sectors have not been written and the end of the track is not imminent, the Disc Write Controller returns to DW0 and continues. If the end of the track is encountered or all the sectors have been written, DW3 waits for the next sector mark. When the sector mark occurs, the Disc Write Controller steps to DW4 and stops writing on the disc.

The time between the parity word and the next sector mark is about 50 microseconds.

3.12.5 DISC WRITE STATE 4 (DW4/Q). When the sector mark (LSMF/Q) turns off (the Erase Gate turns off during the sector mark), DW4 determines if processing is to continue. If all the sectors have been written (ZERO8), the Disc Write Controller returns to DW0 and waits for another start signal from the system controller. If processing is to continue, the disc read/write head is switched and the cylinder address is incremented (if applicable). Refer to figure 2-3, Automatic Track Incrementing.

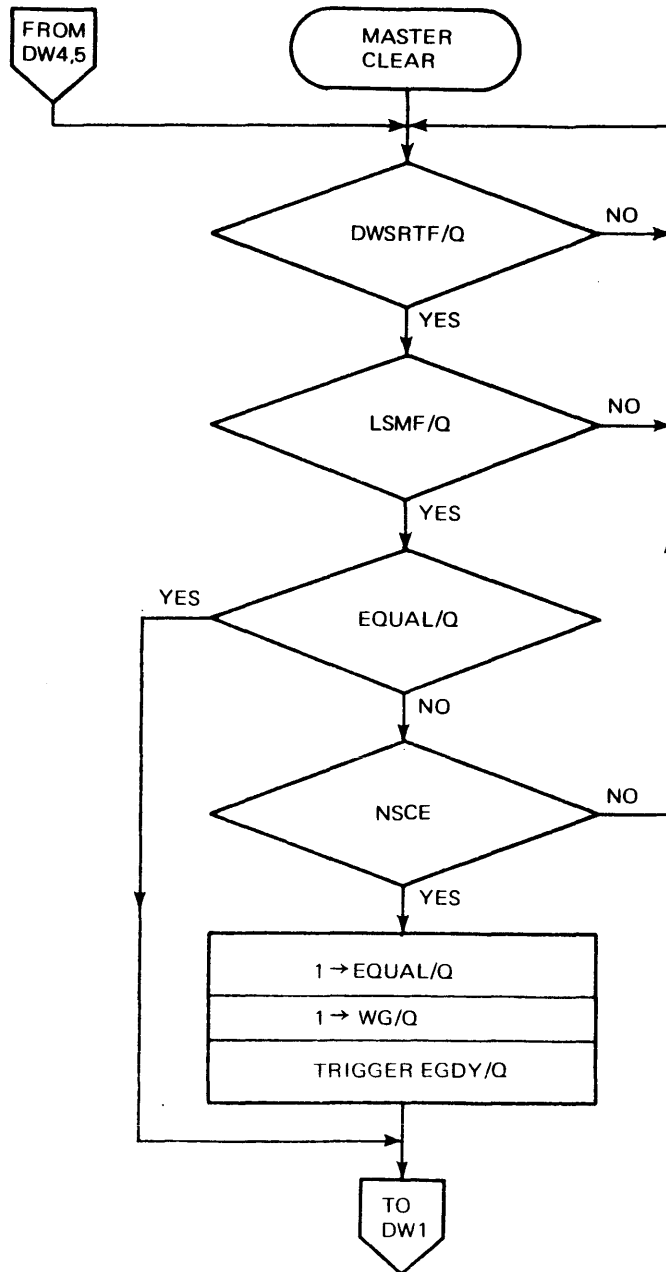


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Figure 3-17. System Write Control, State 3

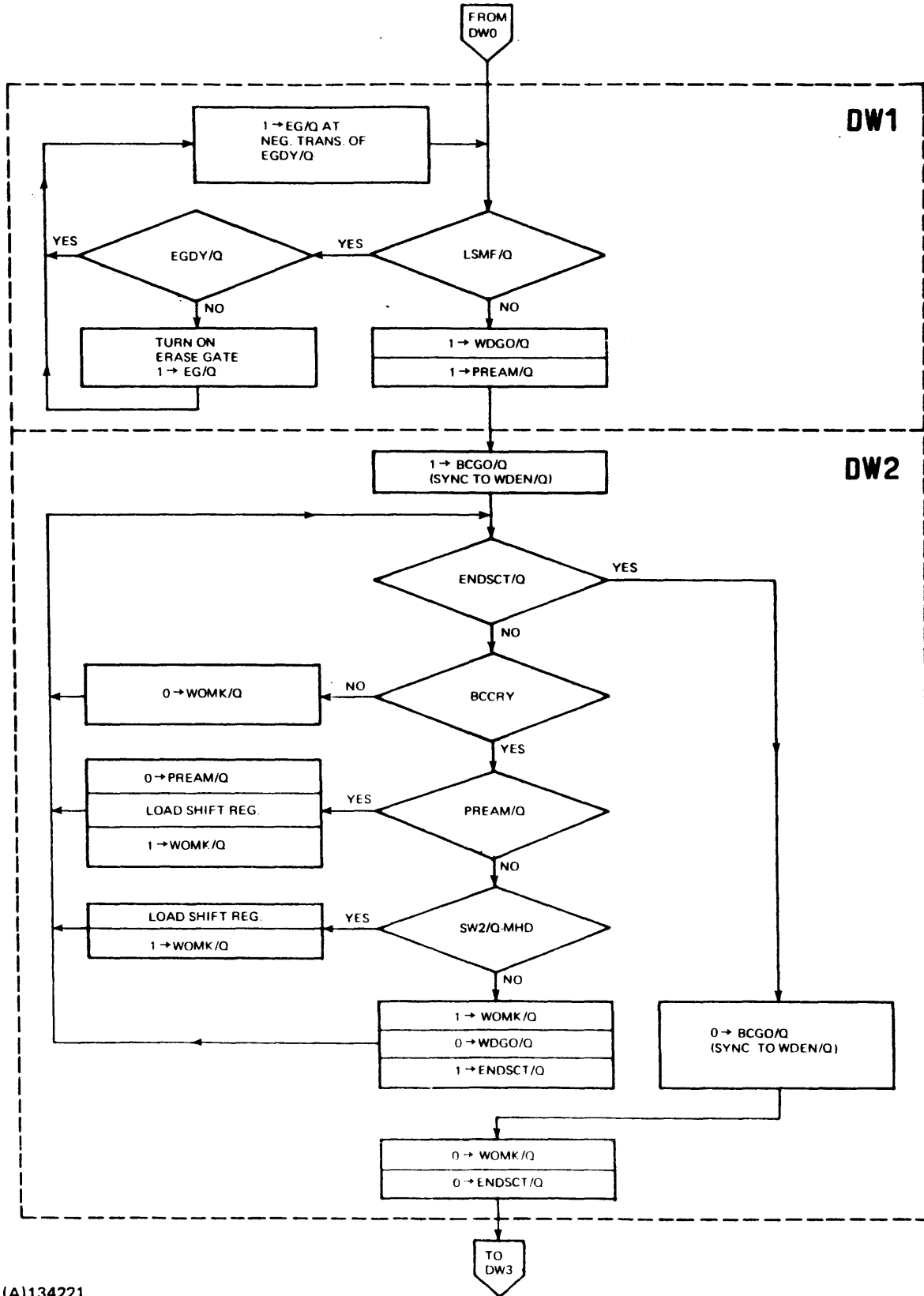


DWO



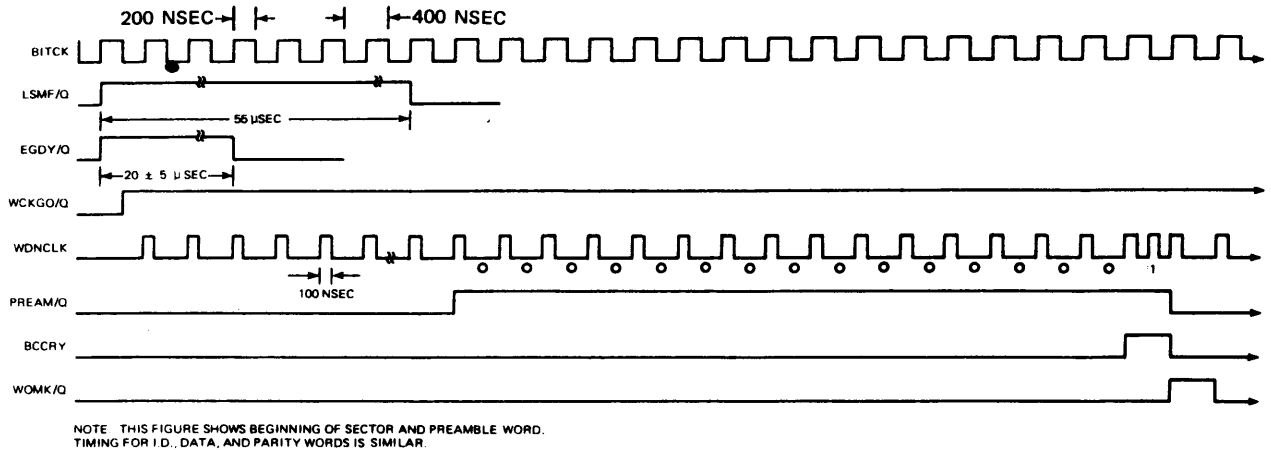
(A)134220

Figure 3-18. Disc Write Control, State 0



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Figure 3-19. Disc Write Control, States 1 and 2



(A)134222

Figure 3-20. Timing Chart, Disc Write Control

3.13 SYSTEM READ CONTROL

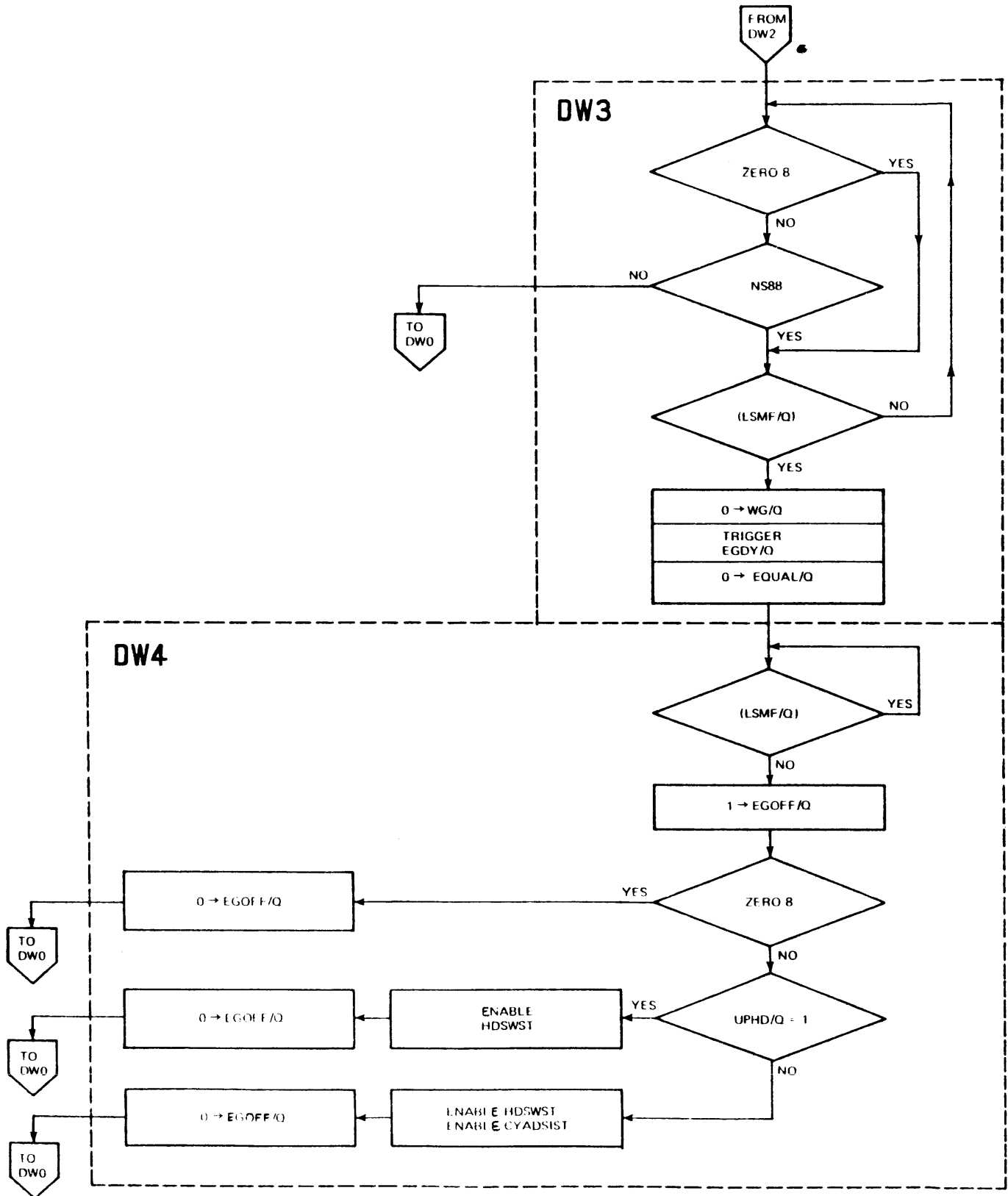
The System Read Controller is activated by the List Word 4 strobe for all Read and Write commands. The System Read Control performs I.D. verification prior to data transfer (not applicable for a Read I.D. or Write I.D. command) and prevents writing on the disc if an I.D. error is encountered. Other functions of the System Read Controller are to accept data from the Disc Read Controller and transfer it to CPU memory via the BTC, and to monitor the BTC and Disc Read Controller in order to set status bits and abort or terminate the list operation. The System Read Controller is synchronized to the CPU (system) clock.

3.13.1 SYSTEM READ STATE 0 (SR0/Q). Refer to figure 3-22. The I.D. check operation is detailed in the Identification Word Verification paragraph and will not be discussed in this section. The primary function of SR0 is to determine when to initiate a read or write operation on the disc. It does this by monitoring the Seek Controller to see when the disc has finished seeking. For a Read I.D. command, a start signal is given to the Disc Read Controller. When the DRC reaches its State 2 (DR2/Q), the System Read Controller steps to State 1 (SR1/Q). For a Read Data command and if the I.D. word has been read (whether or not it was correct), a start signal is issued to the Disc Read Controller. When the DRC reaches State 2 (DR2/Q), the Parity Register, Word Counter, and word count equal 0 flip-flops are reset. The sector counter in the BTC is decremented, and the IDWORD/Q flip-flop (used to inhibit the Word Counter) is set.

3.13.2 SYSTEM READ STATE 1 (SR1/Q). Refer to figure 3-23. SR1 determines when a word has been read from the disc (refer to figure 3-13) and when to increment the Word Counter. When a word has been loaded into the Data Buffer Register, the System Read Controller steps to SR2/Q.

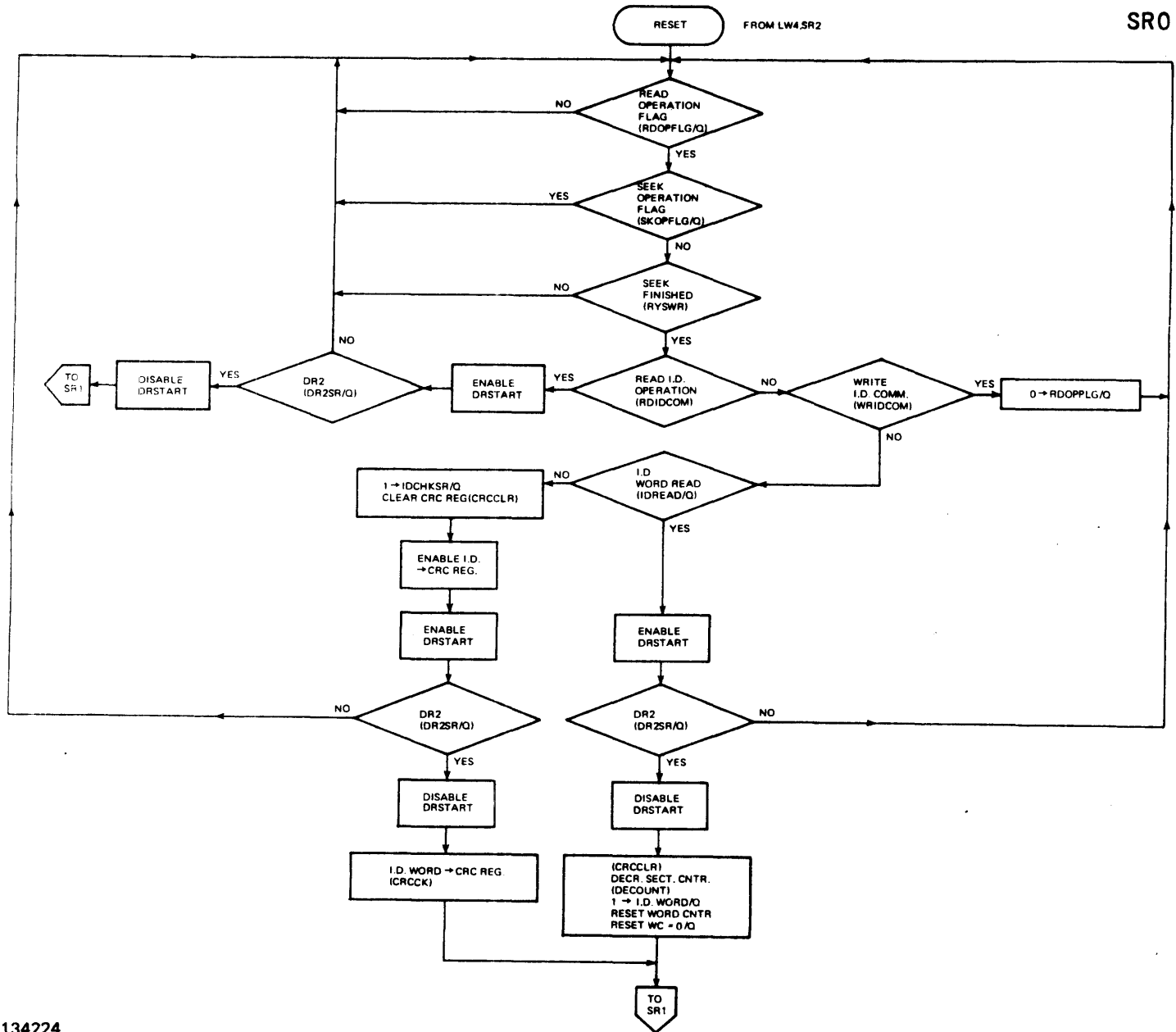
3.13.3 SYSTEM READ STATE 2 (SR2/Q). Refer to figure 3-24 (sheets 1 through 3). To keep the System Read Controller in synchronization with the Disc Read Controller, SR2 waits for the word mark to fall before proceeding. If the I.D. word/Q flip-flop is "on", System Read steps back to SR1 to wait for the first data word. If the WC=0/Q flip-flop is "on", the word just read was the parity word. Once the parity word is read (refer to figure 3-24, sheet 2), SR2 must decide whether to continue with the next sector, terminate, or chain to a new list, and it must check the parity word.

If it is not an I.D. check operation, the data word is transferred to the BTC. Operation Complete status will be set if the command was a Read I.D., otherwise, the System Read Controller Steps back to SR1 and waits for the next word.



(A)13223

Figure 3-21. Disc Write Control, States 3 and 4

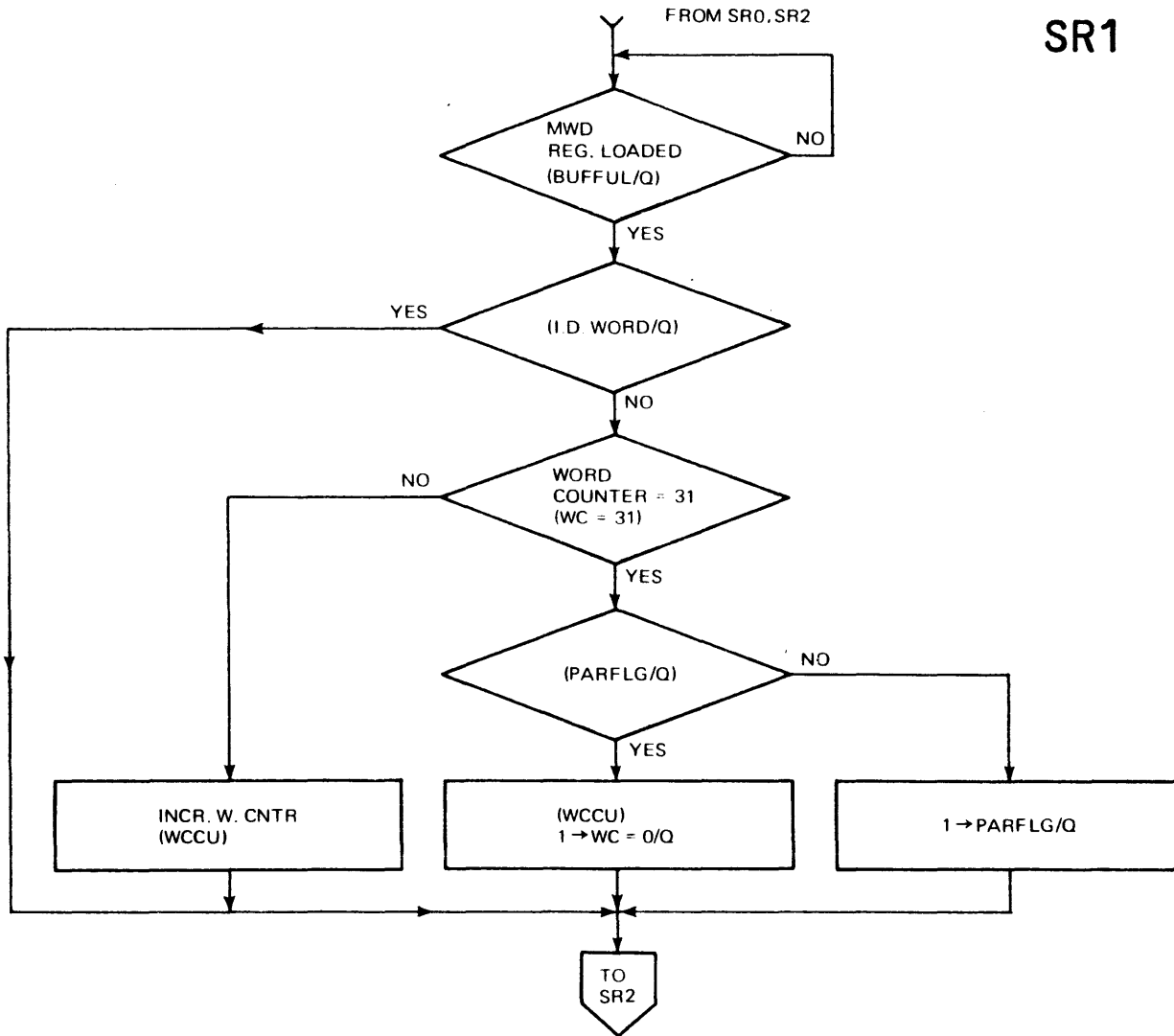


(A)134224

Figure 3-22. System Read Control, State 0



SR1



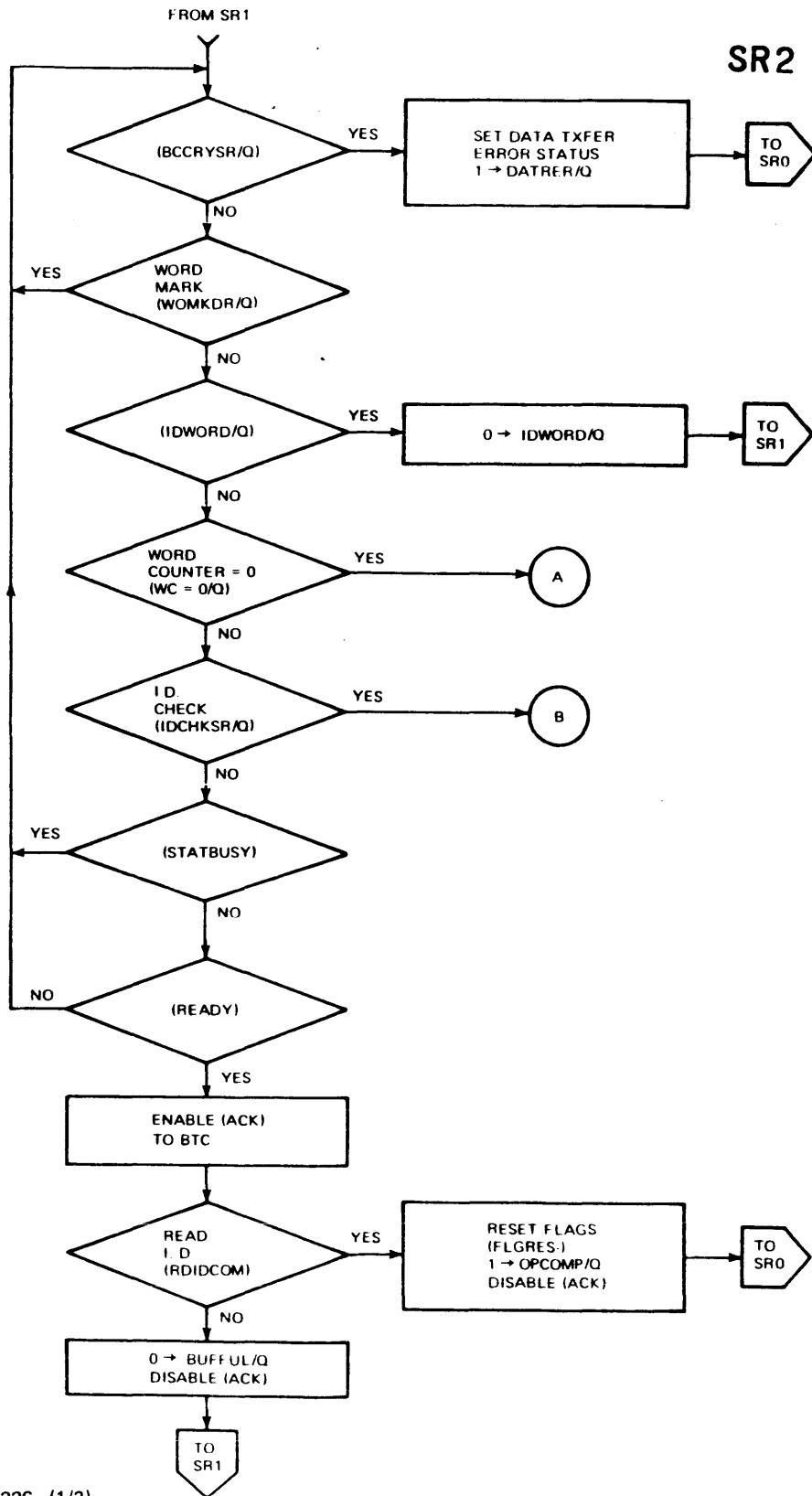
(A)134225

Figure 3-23. System Read Control, State 1

3.14 DISC READ CONTROL

The primary function of the Disc Read Controller (DRC) is to provide the necessary circuitry to retrieve data from the disc and present the information to the system controller. The system control is synchronized to the CPU (system) clock. The DRC is synchronized to the disc via the crystal/and generated clock (BITCK).

3.14.1 DISC READ STATE 0 (DR0). Refer to figure 3-25. The DR0 initiates the read operation on the proper sector. The system controller sends a start signal (DRSFTF/Q) when it is ready. Reading commences with the next sector encountered if that sector is not the 89th (switching) sector and if the operation is an I.D. check or Read I.D. command. The EQUAL/Q flag means that at least one sector has been read, the BTC sector counter is not zero (ZERO8) and to continue reading. NSCE (next sector compare equal) means that the next sector is the starting sector at which reading begins.

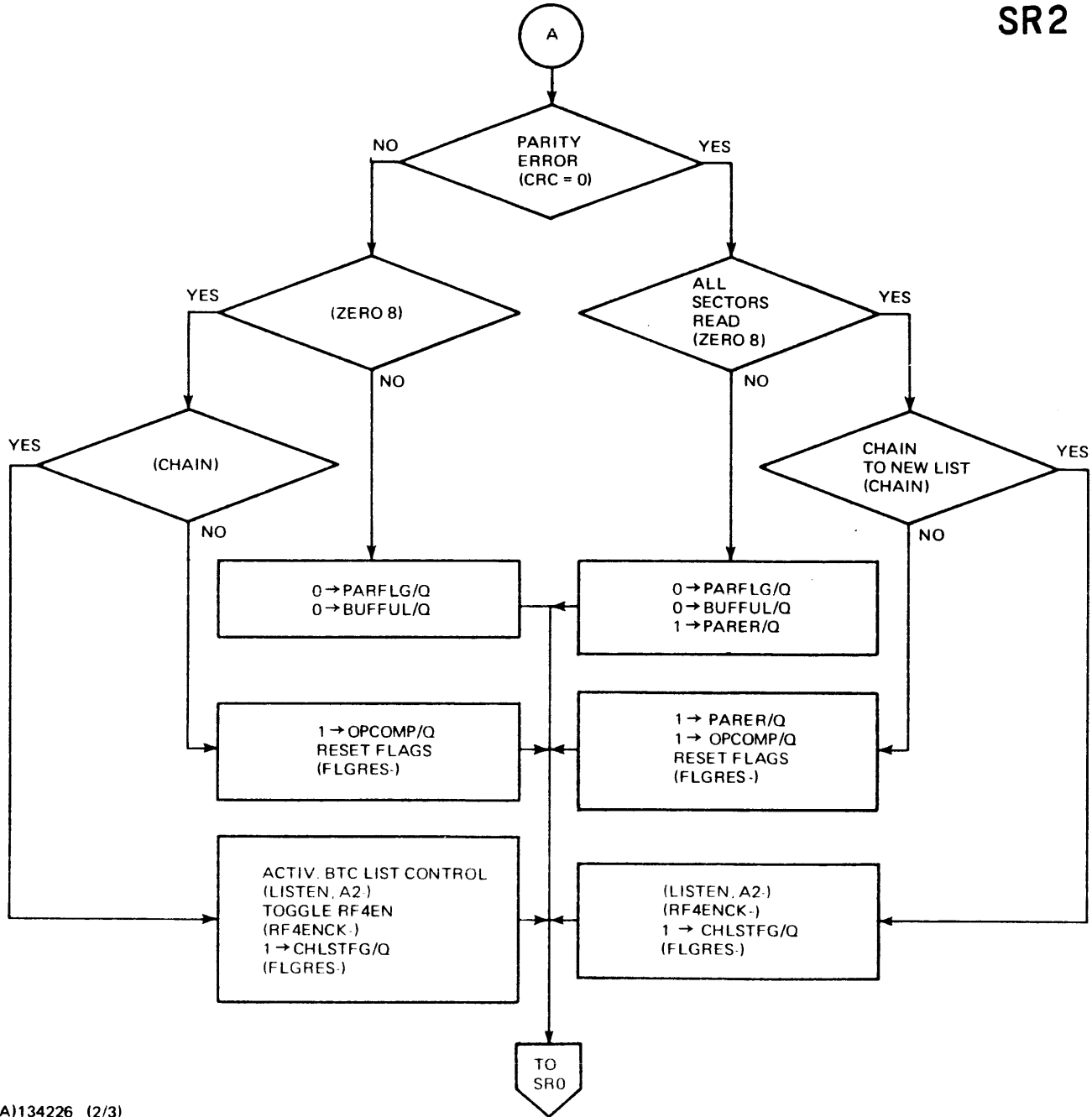


(A)134226 (1/3)

Figure 3-24. System Read Control, State 2 (Sheet 1 of 3)



SR2



(A)134226 (2/3)

Figure 3-24. System Read Control, State 2 (Sheet 2 of 3)



SR2

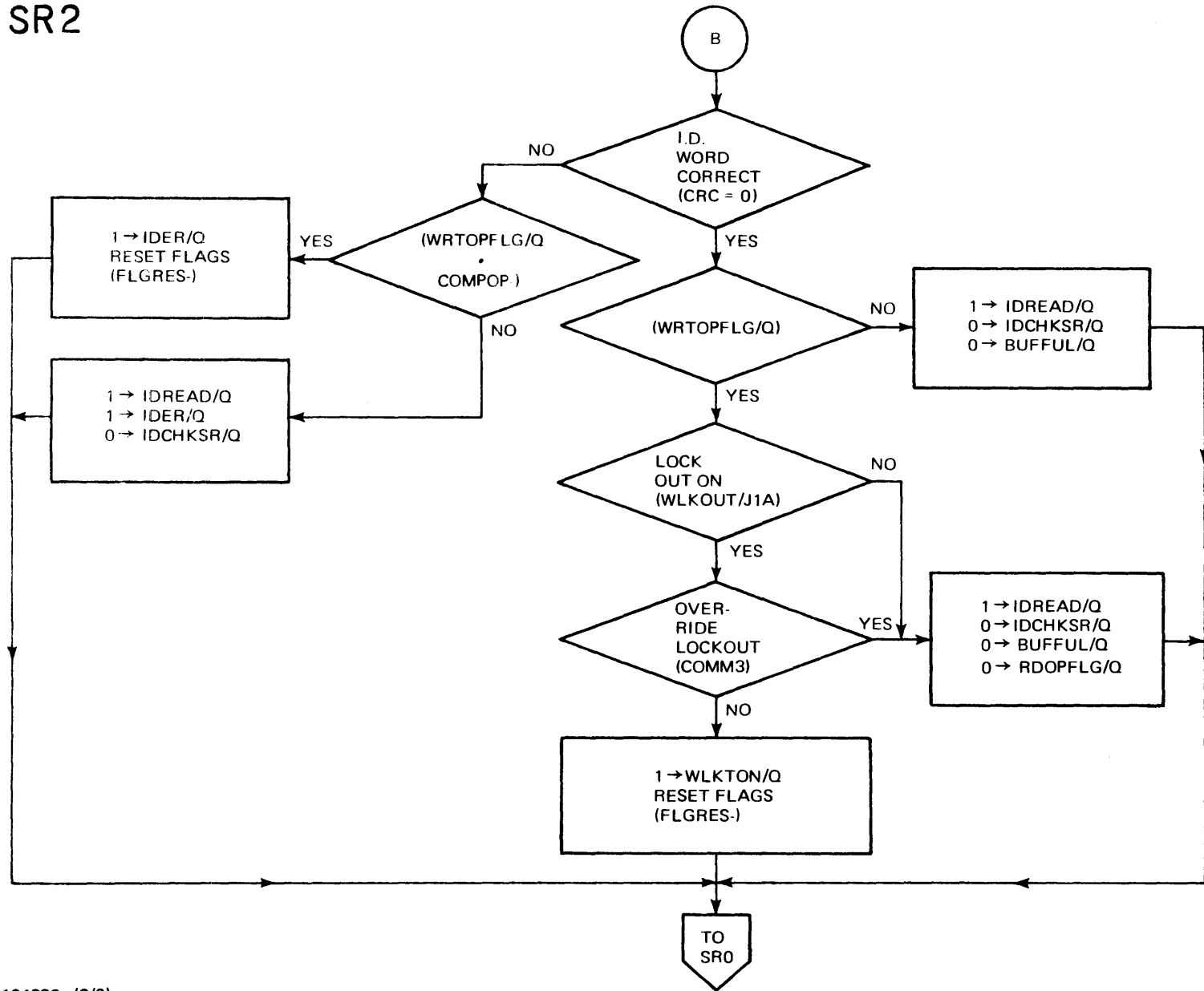
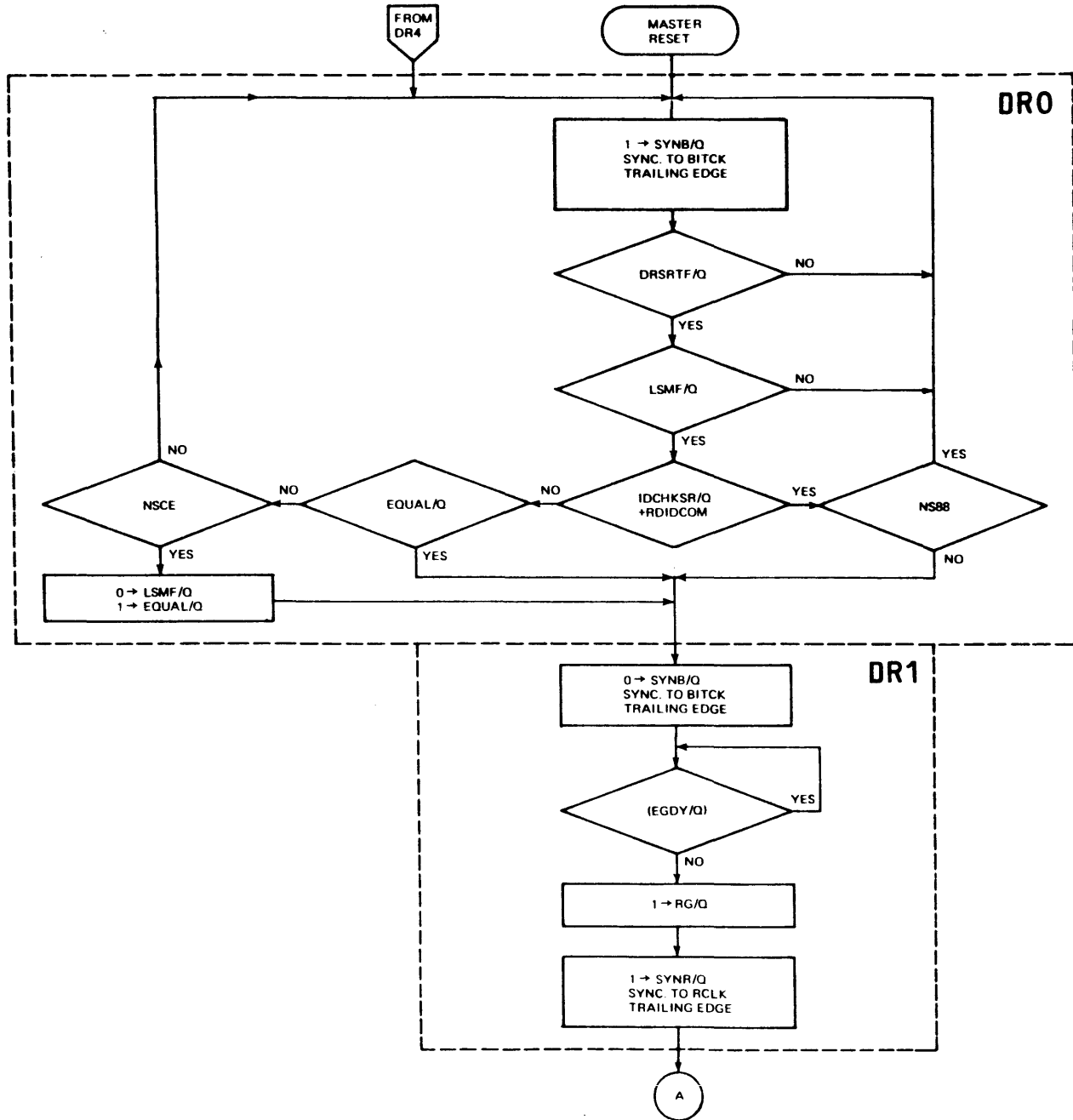


Figure 3-24. System Read Control, State 2 (Sheet 3 of 3)



(A)134227

Figure 3-25. Disc Read Control, States 0 and 1



3.14.2 DISC READ STATE 1 (DR1). Refer to figure 3-25. The first portion of DR1 switches the DRC from the crystal oscillator clock (BITCK) to the clock being read from the disc (RCLK). After clock switching has been effected, DR1 reads the preamble word (15 zeros followed by a one). A word mark is generated before existing DR1 if this is a compare operation and the I.D. has been checked. For a compare operation the Disc Read Controller and the System Write Controller are active.

3.14.3 DISC READ STATE 2 (DR2). Refer to figure 3-26. The I.D. word, data words, and parity word are read during DR2. When the System Write Controller leaves SW2 (if a compare operation) or the System Read Controller sets PARFLG/Q or IDCHSR/Q, the DRC steps to Disc Read State 3.

3.14.4 DISC READ STATE 3 (DR3). Refer to figure 3-26. During DR3, the parity word is loaded into the Data Buffer Register and the Parity Register (CRCK-). (Refer to figure 3-23.) The clock to which the DRC is synchronized is switched back from the clock being read from the disc (RDCLK) to the crystal oscillator clock (BITCK).

3.14.5 DISC READ STATE 4 (DR4). Refer to figure 3-27. DR4 determines if the read operation has been completed (ZERO8), or if reading is to continue. If reading is to continue, DR4 performs a head switch and/or cylinder increment, if necessary.

3.15 STATUS CONTROL

The Status Controller determines when status should be stored. It stores status and determines whether processing is to continue after status has been stored. The Status Controller is a system controller, and is synchronized to the CPU (system) clock.

3.15.1 STATUS CONTROL STATE 0 (ST0). Refer to figure 3-28. ST0 determines when status should be stored (ST1/JA1). If the status to be stored is a terminal type status, meaning that processing is to be stopped, a reset signal (FLGRES) is generated which resets the System Read, Write, and Seek Controllers to their idle state. The BTC Status Controller is then activated by a signal from ST0 (STATEN) and the status word to be stored is transferred from Status Register 1 to Status Register 2.

3.15.2 STATUS CONTROL STATE 1 (ST1). Refer to figure 3-29. ST1 waits for the BTC Status Controller to obtain memory access granted from the CPU and take the status word. When the BTC takes the status word, the Status Controller steps to State 2.

3.15.3 STATUS CONTROL STATE 2 (ST2). Refer to figure 3-29. ST2 is primarily a wait state for waiting until the BTC has stored both status words. If the status stored was a terminal type status, indicated by STRESEN/Q, a reset signal is generated (STATMRS) which resets the entire Moving Head Disc Controller (the BTC logic and the DCL). The Moving Head Disc Controller is now ready for another Activate command from the CPU.

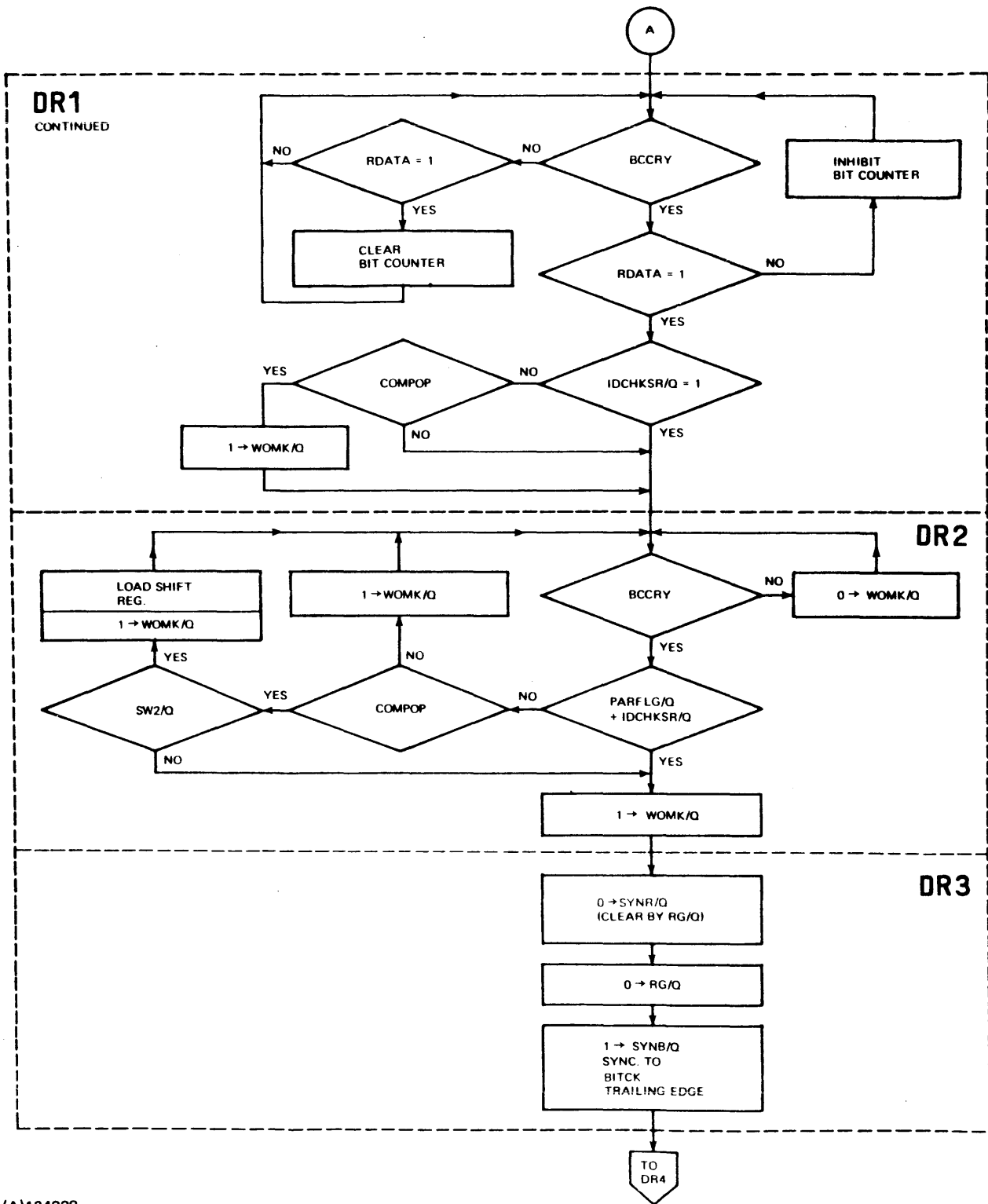
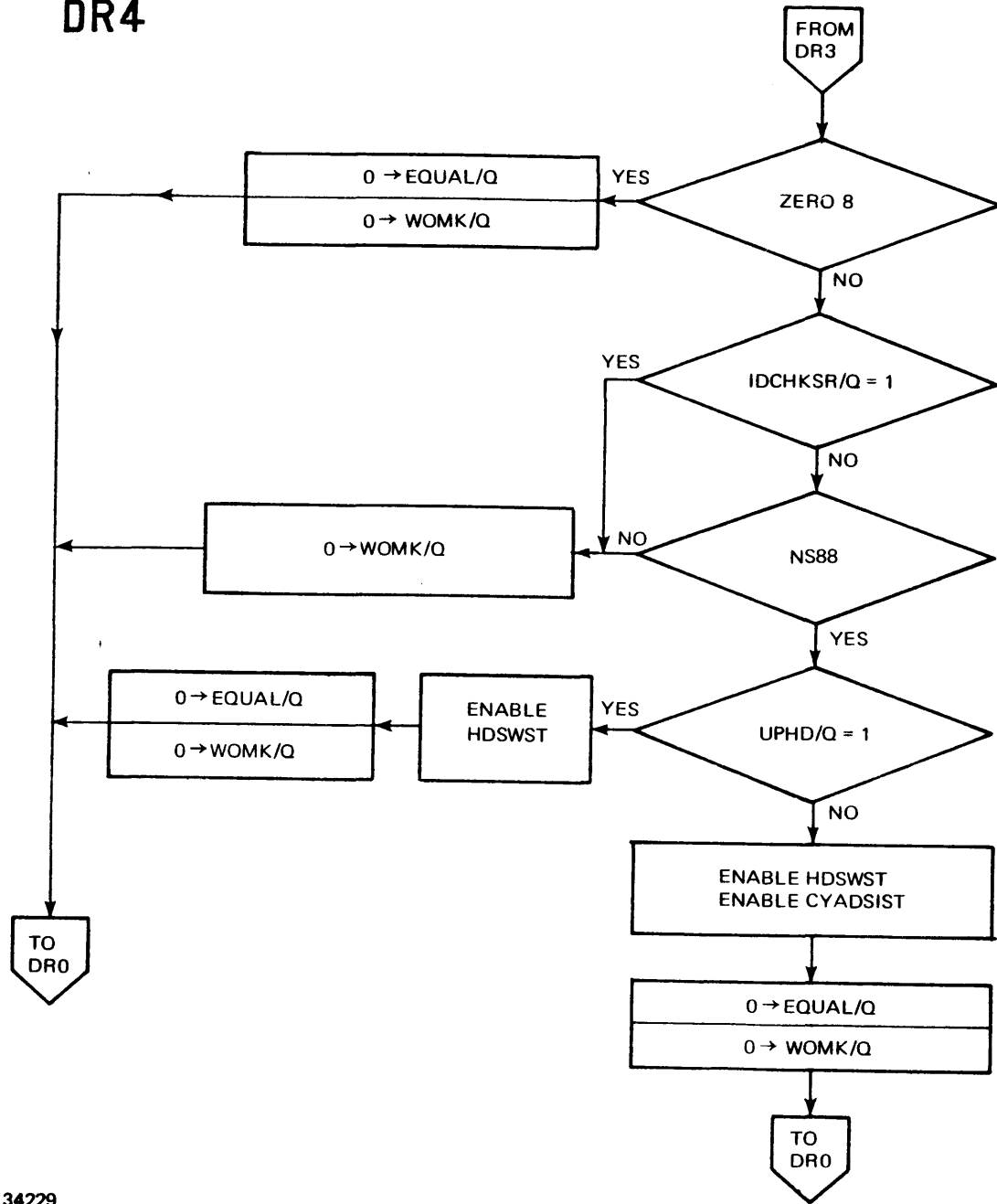


Figure 3-26. Disc Read Control, States 1, 2, and 3



DR4

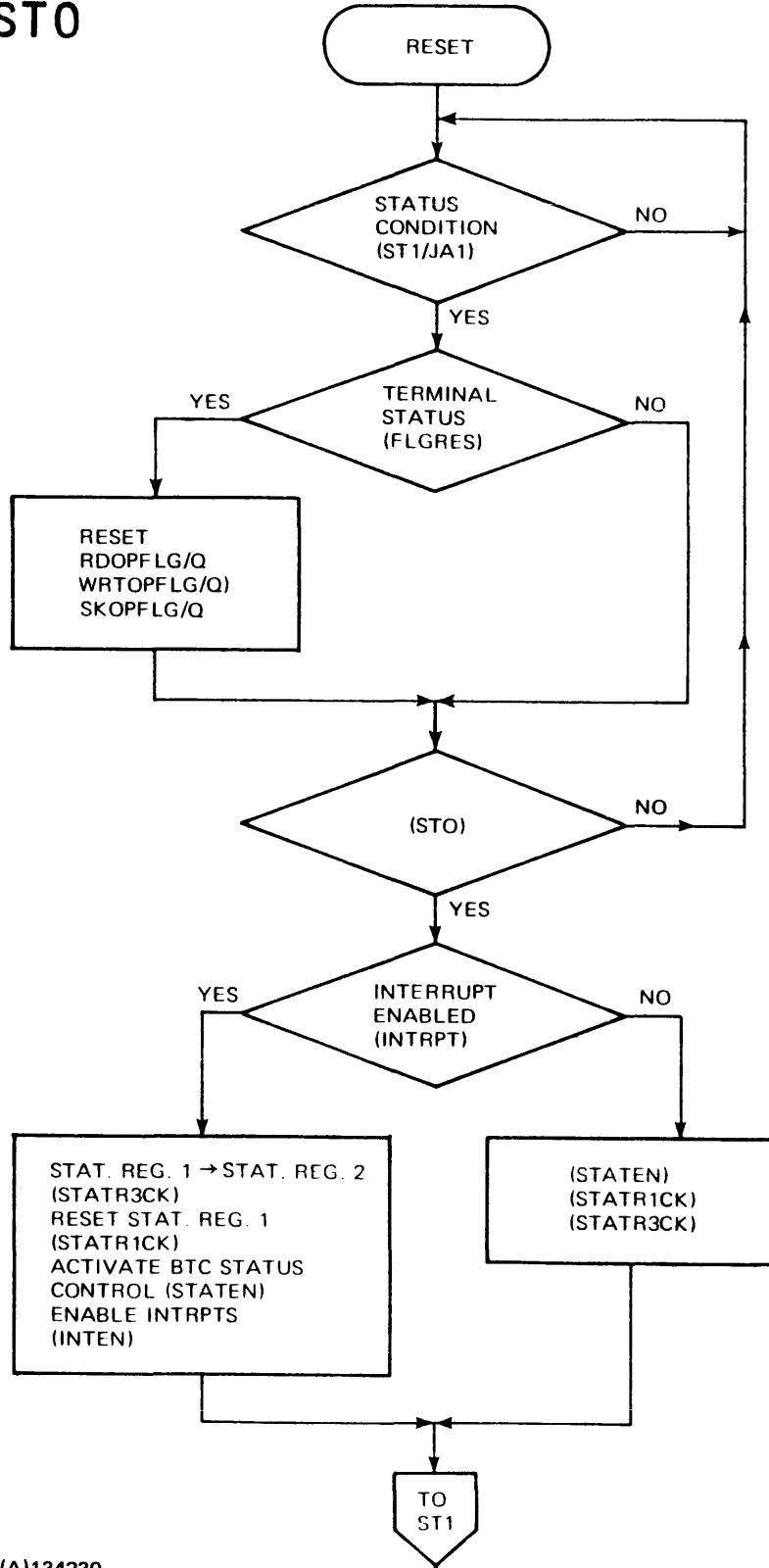


(A)134229

Figure 3-27. Disc Read Control, State 4

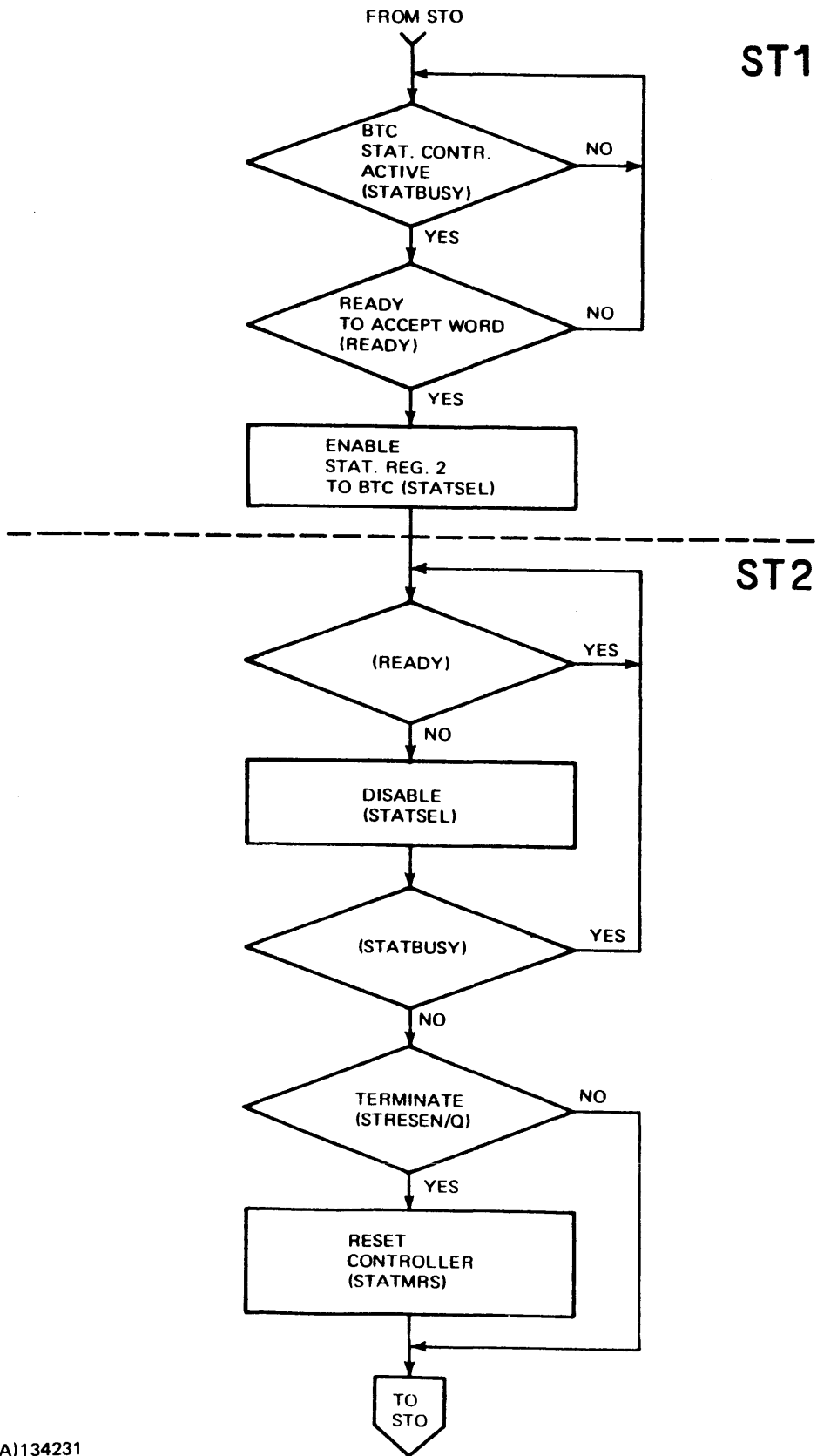


STO



(A)134230

Figure 3-28. Status Control, State 0



(A)134231

Figure 3-29. Status Control, States 1 and 2



SECTION IV

MAINTENANCE

4.1 GENERAL

This section, combined with Sections V and VI, provides the information required to troubleshoot the controller circuitry. These sections include the connector pin numbering, circuit board network location designations, listing of the signals within the controller and those signals interconnecting the circuit boards, and logic diagrams.

4.2 PREVENTIVE MAINTENANCE

Maintenance is not required for the controller. However, proper preventive maintenance of the disc unit is essential and reference should be made to the maintenance manual for the appropriate maintenance.

4.3 CIRCUIT BOARDS

The circuit boards used are provided with individual network pin sockets which are designed for wire-wrap interconnections. The network location designations are those utilized in the circuit documentation. The single connector board is illustrated in figure 4-1 and the double connector circuit board is illustrated in figure 4-2. The circuit boards are always installed with the component side toward the front of the I/O Expansion Unit.

The bottom edge connector is designated as location M, and the top edge connector is designated as location N. Figure 4-3 shows the top edge pin assignment which corresponds to the cable connector used.

4.4 CONTROLLER/DISC CABLING

The controller and disc(s) are connected via cabling consisting of twisted pair lines. Figure 4-4 illustrates the controller/disc connections.

4.5 DIAGNOSTICS

The following diagnostics are pertinent to the 980A and 980B computers.

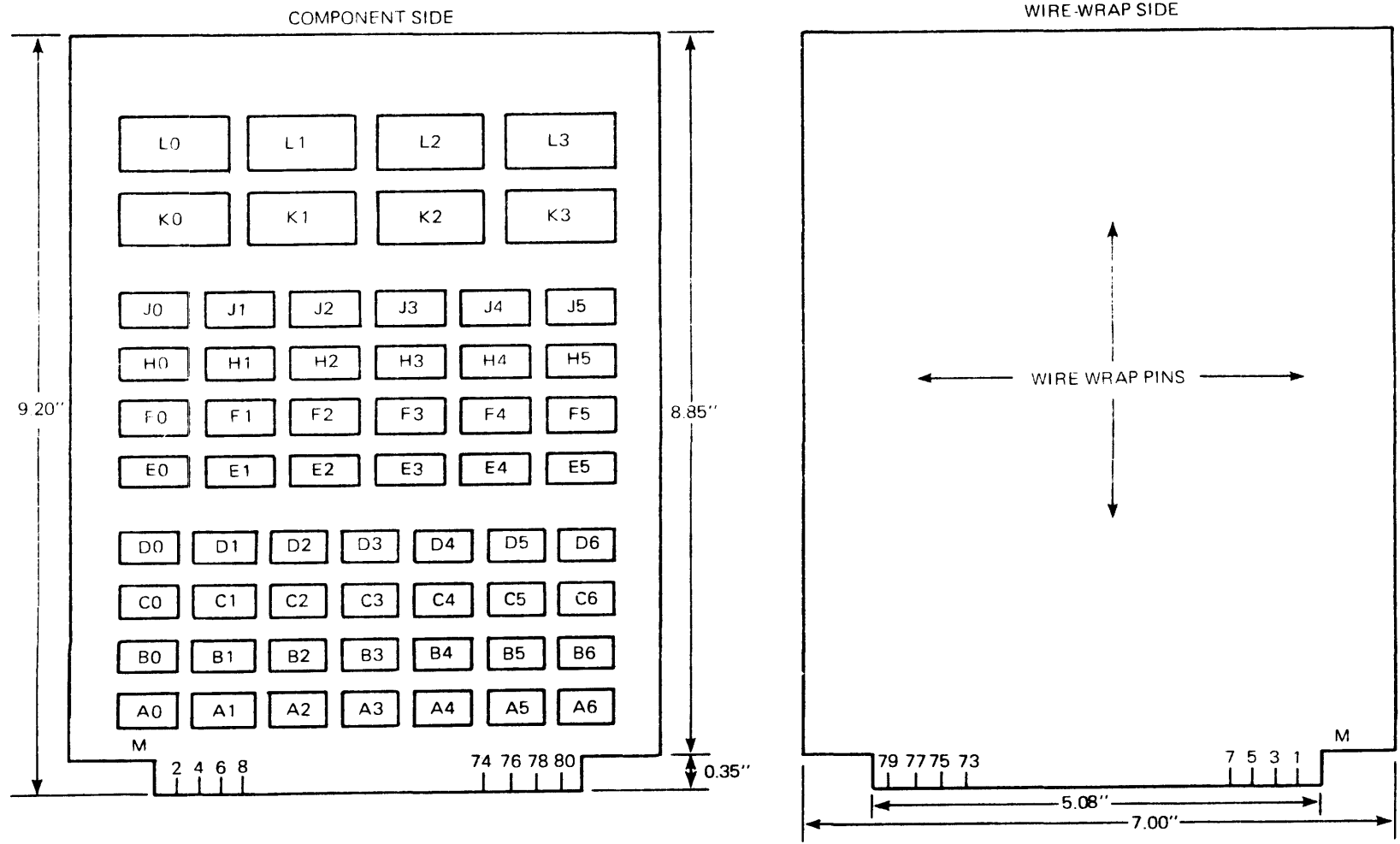
Program Description	985137-9901
Assembly Listing	985137-9902
Paper Tape Object	985137-1101

The following diagnostics are pertinent to the 960A and 960B computers.

Program Description	985136-9901
Assembly Listing	985136-9902
Paper Tape Object	985136-1101



944824-9701



(A)134232

Figure 4-1. Single Connector Circuit Board, Outline Dimensions and Circuit Location Designations

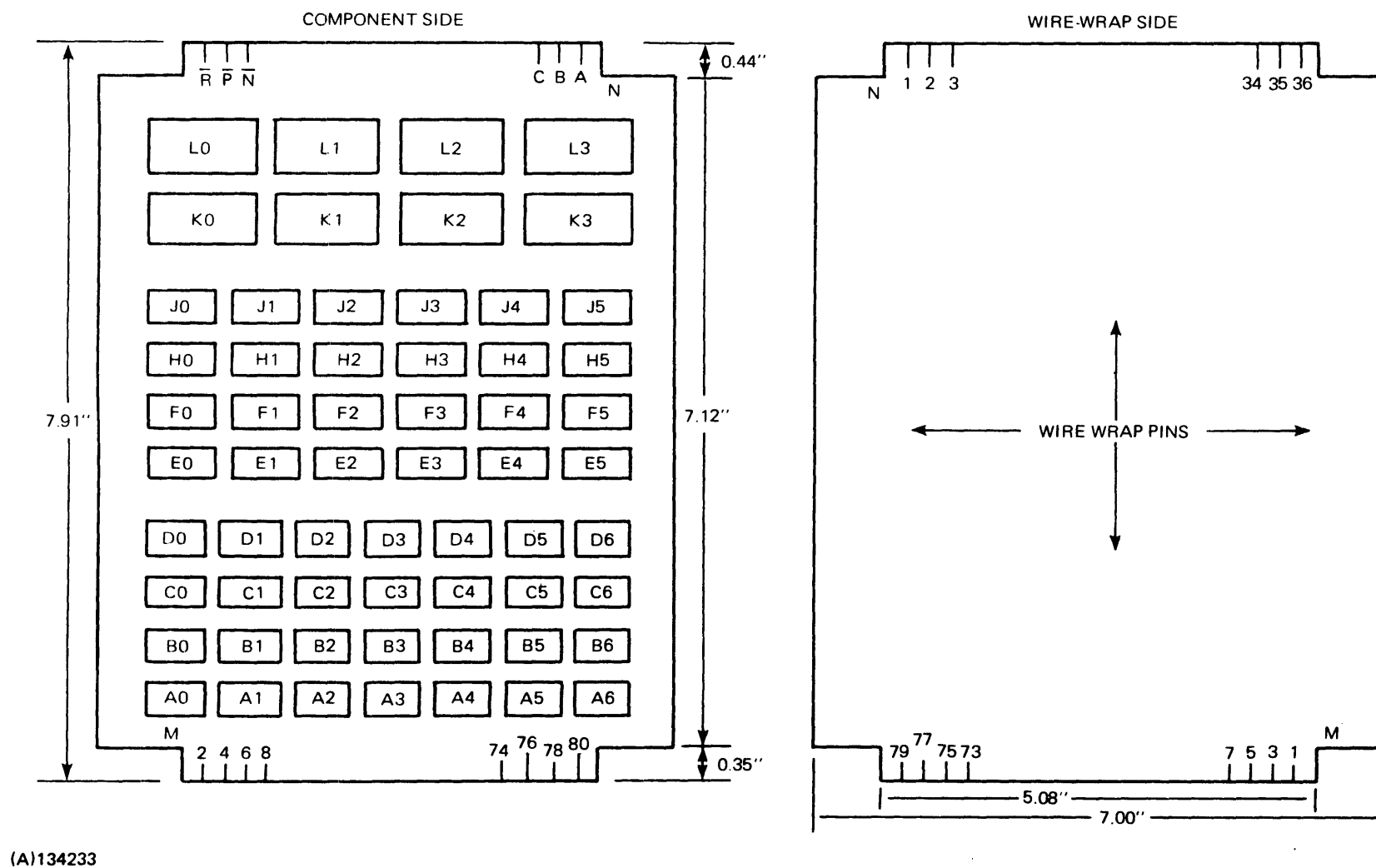
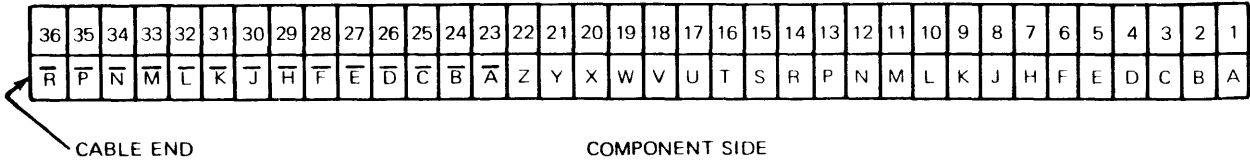
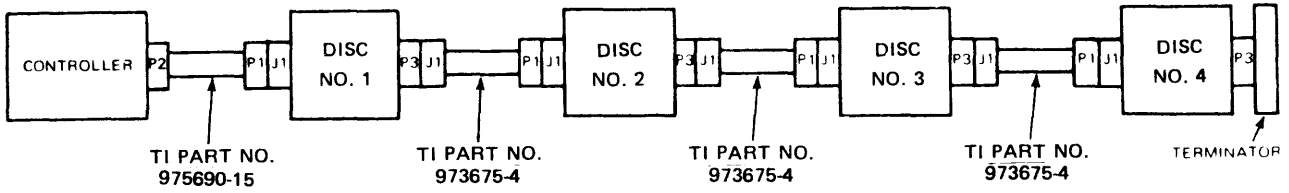


Figure 4-2. Double Connector Circuit Board, Outline Dimensions and Circuit Location Designations



(A)134234

Figure 4-3. Top Edge Connector Pin Assignment



(A)134235

Figure 4-4. Controller/Disc Cabling



SECTION V

DOCUMENTATION

5.1 GENERAL

This section describes the optional, computer-generated documentation including the signature load list, and the location pin list.

5.2 CONTROLLER LOAD LIST, PART NUMBER 961711-9920

The signature load list is an alphanumerical listing of all signal names utilized in the controller circuitry. Each listing indicates every point to which a signal connects. The load list reference information is given in table 5-1. The load list is as follows.

5.3 CONTROLLER PIN LIST, PART NUMBER 961771-9921

The location pin list is a listing of the signal on each pin every network, component, and connector of the controller circuit boards. The pin listing for each location includes the information defined in table 5-2. The pin list is as follows.

5.4 CONNECTOR PLATE WIRING

The connector plate wiring for any configuration which includes the Moving Head Disc Controller is documented in the appropriate appendix of the DMAP Expander Maintenance Manual, Part Number 216759-9701.

If connector plate wiring information is required concerning the BTC and/or the DMAP Expander and/or other controllers of a given configuration, refer to the manual listed above.



944824-9701

LOAD LIST

Drawing No. 967711-9920



Table 5-1. Load List Reference Information

Item	Description
Signature	Signal name
Circuit type	Type of circuit providing a load or source
Location name	Indicates the location of the load or source Network or component locations are listed as X YOZ, where: X indicates the (module) board no., i.e., 1 indicates Circuit Board N. 1, etc. YOZ indicates the row/column location as indicated in figures 4-1 and 4-2, i.e., row Y column OZ. Connector locations are indicated as either X MOX (bottom connector) or X NOX (top connector). Again, X indicates the (module) board no.
Pin name	Indicates the pin number associated with corresponding location name.
Pin function	An asterisk (*) indicates a signal source. If no signal source is indicated, the source enters through a connector pin from an external point.
Block number	} Not used in maintenance/troubleshooting
Device name	
Sequence no.	
N + Load	
Branch vector	
Wiring comment	

LOAD LISTING FOR: PRODUCT CODE							MODULE	DATE 10/01/76	PAGE	1	
PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
ACK-	X CB	BTCCB3X	3		CN		0	1	/910 3	CONN	.00
ACK-	X CB	CB003MHD	7		CN		0	1	/902 7	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
AG	X CB	BTCCB3X	4		CN		0	1	/910 4	CONN	.00
AG	X CB	BTCCB2X	3		CN		0	1	/908 3	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
AGDEV-	CB	BTCCB0X	21		CN		0	1	/912 21	CONN	.00
AGDEV-	CB	BTCCB3X	5		CN		0	1	/910 5	CONN	.00
AGDEV-	CB	BTCCB3X	6		CN		0	1	/910 6	CONN	.00
AGDEV-	CB	BTCCB3X	7		CN		0	1	/910 7	CONN	.00
AGDEV-	CB	BTCCB3X	8		CN		0	1	/910 8	CONN	.00
AGDEV-	CB	BTCCB3X	9		CN		0	1	/910 9	CONN	.00
AGDEV-	CB	BTCCB3X	10		CN		0	1	/910 10	CONN	.00
AGDEV-	CB	BTCCB3X	11		CN		0	1	/910 11	CONN	.00
AGDEV-	CB	BTCCB3X	12		CN		0	1	/910 12	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ARDEV-	CB	BTCCB0X	67		CN		0	1	/912 67	CONN	.00
ARDEV-	CB	BTCCB3X	14		CN		0	1	/910 14	CONN	.00
ARDEV-	CB	BTCCB3X	15		CN		0	1	/910 15	CONN	.00
ARDEV-	CB	BTCCB3X	16		CN		0	1	/910 16	CONN	.00
ARDEV-	CB	BTCCB3X	17		CN		0	1	/910 17	CONN	.00
ARDEV-	CB	BTCCB3X	18		CN		0	1	/910 18	CONN	.00
ARDEV-	CB	BTCCB3X	19		CN		0	1	/910 19	CONN	.00
ARDEV-	CB	BTCCB3X	20		CN		0	1	/910 20	CONN	.00
ARDEV-	CB	BTCCB3X	21		CN		0	1	/910 21	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ATT1	X CB	BTCCB1X	4		CN		0	1	/907 4	CONN	.00
ATT1	X CB	CB002MHD	8		CN		0	1	/901 8	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ATT2	X CB	BTCCB3X	74		CN		0	1	/910 74	CONN	.00
ATT2	X CB	BTCCB1X	5		CN		0	1	/907 5	CONN	.00
ATT2	X CB	CB003MHD	9		CN		0	1	/902 9	CONN	.00
ATT2	X CB	CB002MHD	76		CN		0	1	/901 76	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BCCRY	XA CB	CB001MHD	36		CN		0	1	/903 36	CONN	.00
BCCRY	XA CB	CB003MHD	44		CN		0	1	/902 44	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BCCRY-	XA CB	CB001MHD	46		CN		0	1	/903 46	CONN	.00
BCCRY-	XA CB	CB003MHD	58		CN		0	1	/902 58	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BITOSC	XA CB	CB006MHD	21		CN		0	1	/904 21	CONN	.00
BITOSC	XA CB	CB001MHD	66		CN		0	1	/903 66	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BTCLR	XA CB	CB001MHD	17		CN		0	1	/903 17	CONN	.00
BTCLR	XA CB	CB002MHD	17		CN		0	1	/901 17	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BTCLR-	X CB	BTCCB1X	6		CN		0	1	/907 6	CONN	.00
BTCLR-	X CB	CB004MHD	9		CN		0	1	/906 9	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
BUFFUL/Q	XA CB	CB001MHD	52		CN		0	1	/903 52	CONN	.00
BUFFUL/Q	XA CB	CB003MHD	64		CN		0	1	/902 64	CONN	.00
BUFFUL/Q	XA CB	CB002MHD	62		CN		0	1	/901 62	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RUSY-	X CB	BTCCB1X	7		CN		0	1	/907 7	CONN	.00
RUSY-	X CB	CB002MHD	5		CN		0	1	/901 5	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RUSY/D-	XA CB	CB006MHD	36		CN		0	1	/904 36	CONN	.00
RUSY/D-	XA CB	CB002MHD	57		CN		0	1	/901 57	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RUSY/DR2-	XA CB	CB003MHD	11		CN		0	1	/902 11	CONN	.00
RUSY/DR2-	XA CB	CB002MHD	15		CN		0	1	/901 15	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RUSY/Q-	XA CB	CB005MHD	75		CN		0	1	/905 75	CONN	.00
RUSY/Q-	XA CB	CB006MHD	29		CN		0	1	/904 29	CONN	.00
RUSY/Q-	XA CB	CB002MHD	35		CN		0	1	/901 35	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CHAIN	XA CB	CB004MHD	29		CN		0	1	/906 29	CONN	.00
CHAIN	XA CB	CB003MHD	12		CN		0	1	/902 12	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CHAIN-	XA CB	CB004MHD	30		CN		0	1	/906 30	CONN	.00
CHAIN-	XA CB	CB003MHD	13		CN		0	1	/902 13	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CHLTKN/D-	XA CB	CB006MHD	39		CN		0	1	/904 39	CONN	.00
CHLTKN/D-	XA CB	CB003MHD	62		CN		0	1	/902 62	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CHLTKN/Q-	XA CB	CB006MHD	28		CN		0	1	/904 28	CONN	.00
CHLTKN/Q-	XA CB	CB002MHD	34		CN		0	1	/901 34	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CLOCK-	CB	BTCCB0X	33		CN		0	1	/912 33	CONN	.00
CLOCK-	CB	BTCCB1X	8		CN		0	1	/907 8	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
CNTUP-	X CB	BTCCB3X	22		CN		0	1	/910 22	CONN	.00
CNTUP-	X CB	BTCCB2X	4		CN		0	1	/908 4	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
COMERR/Q	XA CB	CB001MHD	43		CN		0	1	/903 43	CONN	.00
COMERR/Q	XA CB	CB003MHD	54		CN		0	1	/902 54	CONN	.00

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DRAWING NUMBER 961711-9920 REVISION LTR N

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
0 NET LOADS *EXTERNAL SOURCE*											
COMM1- COMM1- COMM1-	XA XA XA	CB CB CB	CB004MHD CB001MHD CB003MHD	31 11 14	CN CN CN		0 0 0	1 1 1	/906 31 /903 11 /902 14	CONN CONN CONN	.00 .00 .00
0 NET LOADS *EXTERNAL SOURCE*											
COMM2 COMM2	XA XA	CB CB	CB004MHD CB001MHD	32 12	CN CN		0 0	1 1	/906 32 /903 12	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
COMM3- COMM3-	XA XA	CB CB	CB004MHD CB001MHD	33 13	CN CN		0 0	1 1	/906 33 /903 13	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
COMPFR/D- COMPFR/D-	XA XA	CB CB	CB006MHD CB003MHD	44 72	CN CN		0 0	1 1	/904 44 /902 72	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
COMPDP- COMPDP- COMPDP- COMPDP-	XA XA XA XA	CB CB CB CB	CB004MHD CB006MHD CB001MHD CB003MHD	76 32 33 35	CN CN CN CN		0 0 0 0	1 1 1 1	/906 76 /904 32 /903 33 /902 35	CONN CONN CONN CONN	.00 .00 .00 .00
0 NET LOADS *EXTERNAL SOURCE*											
COUNT COUNT	X X	CB CB	BTCCB2X CB001MHD	5 4	CN CN		0 0	1 1	/908 5 /903 4	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CRC=0 CRC=0	XA XA	CB CB	CB004MHD CB005MHD	69 72	CN CN		0 0	1 1	/906 69 /905 72	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CRC=0- CRC=0-	XA XA	CB CB	CB004MHD CB006MHD	72 43	CN CN		0 0	1 1	/906 72 /904 43	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CRCK- CRCK-	XA XA	CB CB	CB005MHD CB003MHD	27 16	CN CN		0 0	1 1	/905 27 /902 16	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CRCLP- CRCLP-	XA XA	CB CB	CB005MHD CB003MHD	26 15	CN CN		0 0	1 1	/905 26 /902 15	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLADCRY CYLADCRY		CB CB	CB004MHD CB005MHD	75 76	CN CN		0 0	1 1	/906 75 /905 76	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD0 CYLAD0	XA XA	CB CB	CB005MHD CB002MHD	44 24	CN CN		0 0	1 1	/905 44 /901 24	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD1 CYLAD1	XA XA	CB CB	CB005MHD CB002MHD	43 23	CN CN		0 0	1 1	/905 43 /901 23	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD2 CYLAD2	XA XA	CB CB	CB005MHD CB002MHD	42 22	CN CN		0 0	1 1	/905 42 /901 22	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD3 CYLAD3	XA XA	CB CB	CB005MHD CB002MHD	41 21	CN CN		0 0	1 1	/905 41 /901 21	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD4 CYLAD4	XA XA	CB CB	CB005MHD CB002MHD	48 27	CN CN		0 0	1 1	/905 48 /901 27	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD5 CYLAD5	XA XA	CB CB	CB005MHD CB002MHD	47 26	CN CN		0 0	1 1	/905 47 /901 26	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD6 CYLAD6	XA XA	CB CB	CB005MHD CB002MHD	46 25	CN CN		0 0	1 1	/905 46 /901 25	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLAD7 CYLAD7 CYLAD7	XA XA XA	CB CB CB	CB004MHD CB005MHD CB002MHD	36 33 16	CN CN CN		0 0 0	1 1 1	/906 36 /905 33 /901 16	CONN CONN CONN	.00 .00 .00
0 NET LOADS *EXTERNAL SOURCE*											
CYLINC/Q- CYLINC/Q- CYLINC/Q-	XA XA XA	CB CB CB	CB004MHD CB005MHD CB001MHD	48 45 20	CN CN CN		0 0 0	1 1 1	/906 48 /905 45 /903 20	CONN CONN CONN	.00 .00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DATAV- DATAV-		CB CB	BTCCB0X BTCCB1X	27 9	CN CN		0 0	1 1	/912 27 /907 9	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DATAVL DATAVL	X X	CB CB	BTCCB3X BTCCB1X	23 10	CN CN		0 0	1 1	/910 23 /907 10	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DATEN- DATEN-	X X	CB CB	BTCCB3X BTCCB2X	69 70	CN CN		0 0	1 1	/910 69 /908 70	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DATREFR/D- DATREFR/D-	XA XA	CB CB	CB006MHD CB003MHD	47 73	CN CN		0 0	1 1	/904 47 /902 73	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DATREFR/Q- DATREFR/Q-	XA XA	CB CB	CB006MHD CB003MHD	27 23	CN CN		0 0	1 1	/904 27 /902 23	CONN CONN	.00 .00
0 NET LOADS *EXTERNAL SOURCE*											
DD2/Q- DD2/Q-	X X	CB CB	BTCCB3X	25	CN		0	1	/910 25	CONN	.00

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME	PIN	WIRING COMMENT	WIRE LENGTH
DD2/Q-	X CB	BTCCB1X	11		CN		0	1	/907	11	CONN	.00
DECOUNT-	X CB	BTCCR3X	26		CN		0	1	/910	26	CONN	.00
DECOUNT-	X CB	CB003MHD	4		CN		0	1	/902	4	CONN	.00
DEVADD,00	CB	BTCCB0X	34		CN		0	1	/912	34	CONN	.00
DEVADD,00	CB	BTCCB2X	7		CN		0	1	/908	7	CONN	.00
DEVADD,01	CB	BTCCB0X	35		CN		0	1	/912	35	CONN	.00
DEVADD,01	CB	BTCCB2X	8		CN		0	1	/908	8	CONN	.00
DEVADD,02	CB	BTCCB0X	36		CN		0	1	/912	36	CONN	.00
DEVADD,02	CB	BTCCB2X	9		CN		0	1	/908	9	CONN	.00
DEVADD,03	CB	BTCCB0X	37		CN		0	1	/912	37	CONN	.00
DEVADD,03	CB	BTCCB2X	10		CN		0	1	/908	10	CONN	.00
DEVADD,04	CB	BTCCB0X	38		CN		0	1	/912	38	CONN	.00
DEVADD,04	CB	BTCCB2X	11		CN		0	1	/908	11	CONN	.00
DEVADD,05	CB	BTCCB0X	39		CN		0	1	/912	39	CONN	.00
DEVADD,05	CB	BTCCB2X	12		CN		0	1	/908	12	CONN	.00
DEVADD,06	CB	BTCCB0X	40		CN		0	1	/912	40	CONN	.00
DEVADD,06	CB	BTCCB2X	13		CN		0	1	/908	13	CONN	.00
DEVADD,07	CB	BTCCB0X	41		CN		0	1	/912	41	CONN	.00
DEVADD,07	CB	BTCCB2X	14		CN		0	1	/908	14	CONN	.00
DEVADD,08	CB	BTCCB0X	42		CN		0	1	/912	42	CONN	.00
DEVADD,08	CB	BTCCB2X	15		CN		0	1	/908	15	CONN	.00
DEVADD,09	CB	BTCCB0X	43		CN		0	1	/912	43	CONN	.00
DEVADD,09	CB	BTCCB2X	16		CN		0	1	/908	16	CONN	.00
DEVADD,10	CB	BTCCB0X	45		CN		0	1	/912	45	CONN	.00
DEVADD,10	CB	BTCCB2X	17		CN		0	1	/908	17	CONN	.00
DEVADD,11	CB	BTCCB0X	44		CN		0	1	/912	44	CONN	.00
DEVADD,11	CB	BTCCB2X	18		CN		0	1	/908	18	CONN	.00
DEVADD,12	CB	BTCCB0X	46		CN		0	1	/912	46	CONN	.00
DEVADD,12	CB	BTCCB2X	19		CN		0	1	/908	19	CONN	.00
DEVADD,13	CB	BTCCB0X	47		CN		0	1	/912	47	CONN	.00
DEVADD,13	CB	BTCCB2X	20		CN		0	1	/908	20	CONN	.00
DEVADD,14	CB	BTCCB0X	48		CN		0	1	/912	48	CONN	.00
DEVADD,14	CB	BTCCB2X	21		CN		0	1	/908	21	CONN	.00
DEVADD,15	CB	BTCCB0X	49		CN		0	1	/912	49	CONN	.00
DEVADD,15	CB	BTCCB2X	22		CN		0	1	/908	22	CONN	.00
DEVADSFLO	X CB	BTCCR3X	27		CN		0	1	/910	27	CONN	.00
DEVADSFLO	X CB	BTCCB1X	12		CN		0	1	/907	12	CONN	.00
DEVADSEL1	X CB	BTCCR3X	28		CN		0	1	/910	28	CONN	.00
DEVADSEL1	X CB	BTCCB2X	23		CN		0	1	/908	23	CONN	.00
DEVADSEL1	X CB	BTCCB1X	13		CN		0	1	/907	13	CONN	.00
DEVADSEL2	X CB	BTCCB3X	29		CN		0	1	/910	29	CONN	.00
DEVADSEL2	X CB	BTCCB2X	24		CN		0	1	/908	24	CONN	.00
DEVADSEL2	X CB	BTCCB1X	14		CN		0	1	/907	14	CONN	.00
DEVAT11-	CB	BTCCB0X	25		CN		0	1	/912	25	CONN	.00
DEVAT11-	CB	BTCCB1X	15		CN		0	1	/907	15	CONN	.00
DEVAT12-	CB	BTCCB0X	23		CN		0	1	/912	23	CONN	.00
DEVAT12-	CB	BTCCB1X	16		CN		0	1	/907	16	CONN	.00
DEVRSY/Q	XA CB	CB003MHD	75		CN		0	1	/902	75	CONN	.00
DEVRSY/Q	XA CB	CB002MHD	10		CN		0	1	/901	10	CONN	.00
DEVFL1CH-	CB	BTCCB0X	73		CN		0	1	/912	73	CONN	.00
DEVFL1CH-	CB	BTCCB2X	25		CN		0	1	/908	25	CONN	.00
DEVMP00	CB	BTCCB0X	4		CN		0	1	/912	4	CONN	.00
DEVMP00	CB	BTCCB1X	17		CN		0	1	/907	17	CONN	.00
DEVMP01	CB	BTCCB0X	3		CN		0	1	/912	3	CONN	.00
DEVMP01	CB	BTCCB1X	18		CN		0	1	/907	18	CONN	.00

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DRAWING NUMBER 961711-9920 REVISION LTR N

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
DEVMPD02 DEVMPD02	CA CB	BTCCBOX BTCCB1X	6 19		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 6	CONN CONN	.00 .00
DEVMPD03 DEVMPD03	CB CB	BTCCBOX BTCCB1X	5 20		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 20	CONN CONN	.00 .00
DEVMPD04 DEVMPD04	CA CB	BTCCBOX BTCCB1X	8 21		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 21	CONN CONN	.00 .00
DEVMPD05 DEVMPD05	CA CB	BTCCBOX BTCCB1X	7 22		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 22	CONN CONN	.00 .00
DEVMPD06 DEVMPD06	CA CB	BTCCBOX BTCCB1X	10 23		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 23	CONN CONN	.00 .00
DEVMPD07 DEVMPD07	CB CB	BTCCBOX BTCCB1X	9 24		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 24	CONN CONN	.00 .00
DEVMPD08 DEVMPD08	CA CB	BTCCBOX BTCCB1X	12 25		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 25	CONN CONN	.00 .00
DEVMPD09 DEVMPD09	CA CB	BTCCBOX BTCCB1X	11 26		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 26	CONN CONN	.00 .00
DEVMPD10 DEVMPD10	CA CB	BTCCBOX BTCCB1X	14 27		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 27	CONN CONN	.00 .00
DEVMPD11 DEVMPD11	CB CB	BTCCBOX BTCCB1X	13 28		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 28	CONN CONN	.00 .00
DEVMPD12 DEVMPD12	CB CA	BTCCBOX BTCCB1X	16 29		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 29	CONN CONN	.00 .00
DEVMPD13 DEVMPD13	CB CB	BTCCBOX BTCCB1X	15 30		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 30	CONN CONN	.00 .00
DEVMPD14 DEVMPD14	CB CB	BTCCBOX BTCCB1X	18 31		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 31	CONN CONN	.00 .00
DEVMPD15 DEVMPD15	CB CB	BTCCBOX BTCCB1X	17 32		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 32	CONN CONN	.00 .00
DEVMPD16 DEVMPD16	CB CB	BTCCBOX BTCCB1X	19 33		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /907 33	CONN CONN	.00 .00
DEVMPD,00 DEVMPD,00	CA CB	BTCCBOX BTCCB2X	50 26		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 26	CONN CONN	.00 .00
DEVMPD,01 DEVMPD,01	CB CB	BTCCBOX BTCCB2X	51 27		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 27	CONN CONN	.00 .00
DEVMPD,02 DEVMPD,02	CB CA	BTCCBOX BTCCB2X	52 28		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 28	CONN CONN	.00 .00
DEVMPD,03 DEVMPD,03	CA CB	BTCCBOX BTCCB2X	53 29		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 29	CONN CONN	.00 .00
DEVMPD,04 DEVMPD,04	CA CA	BTCCBOX BTCCB2X	54 30		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 30	CONN CONN	.00 .00
DEVMPD,05 DEVMPD,05	CA CB	BTCCBOX BTCCB2X	55 31		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 31	CONN CONN	.00 .00
DEVMPD,06 DEVMPD,06	CA CB	BTCCBOX BTCCB2X	56 32		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 32	CONN CONN	.00 .00
DEVMPD,07 DEVMPD,07	CB CB	BTCCBOX BTCCB2X	57 33		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 33	CONN CONN	.00 .00
DEVMPD,08 DEVMPD,08	CA CA	BTCCBOX BTCCB2X	58 34		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 34	CONN CONN	.00 .00
DEVMPD,09 DEVMPD,09	CB CA	BTCCBOX BTCCB2X	59 35		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 35	CONN CONN	.00 .00
DEVMPD,10 DEVMPD,10	CA CB	BTCCBOX BTCCB2X	60 36		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 36	CONN CONN	.00 .00
DEVMPD,11 DEVMPD,11	CA CB	BTCCBOX BTCCB2X	61 37		CN CN		0 0 0 NET LOADS *EXTERNAL SOURCE*	1 1	/912 /908 37	CONN CONN	.00 .00

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
DEVWMD,12	CB	BTCCBOX	62		CN		0	1	/912 62	CONN	.00
DEVWMD,12	CB	BTCCB2X	38		CN		0	1	/908 38	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVWMD,13	CB	BTCCBOX	63		CN		0	1	/912 63	CONN	.00
DEVWMD,13	CB	BTCCB2X	39		CN		0	1	/908 39	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVWMD,14	CB	BTCCBOX	64		CN		0	1	/912 64	CONN	.00
DEVWMD,14	CB	BTCCB2X	40		CN		0	1	/908 40	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVWMD,15	CB	BTCCBOX	65		CN		0	1	/912 65	CONN	.00
DEVWMD,15	CB	BTCCB2X	41		CN		0	1	/908 41	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVWMD,16	CB	BTCCBOX	66		CN		0	1	/912 66	CONN	.00
DEVWMD,16	CB	BTCCB2X	42		CN		0	1	/908 42	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVREAD	X CB	BTCCB3X	30		CN		0	1	/910 30	CONN	.00
DEVREAD	X CB	CB004MHD	13		CN		0	1	/906 13	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVSELO-	X CB	BTCCB2X	43		CN		0	1	/938 43	CONN	.00
DEVSELO-	X CB	BTCCB1X	34		CN		0	1	/907 34	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DEVSTORE-	CB	BTCCBOX	69		CN		0	1	/912 69	CONN	.00
DEVSTORE-	CB	BTCCB2X	44		CN		0	1	/908 44	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DRSTARTB1	XA CB	CB001MHD	29		CN		0	1	/903 29	CONN	.00
DRSTARTB1	XA CB	CB003MHD	31		CN		0	1	/902 31	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DR0MHD/Q	XA CB	CB004MHD	58		CN		0	1	/906 58	CONN	.00
DR0MHD/Q	XA CB	CB001MHD	44		CN		0	1	/903 44	CONN	.00
DR0MHD/Q	XA CB	CB003MHD	55		CN		0	1	/902 55	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
DMO	XA CB	CB001MHD	47		CN		0	1	/903 47	CONN	.00
DMO	XA CB	CB003MHD	59		CN		0	1	/902 59	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
EGDY/Q-	XA CB	CB001MHD	62		CN		0	1	/903 62	CONN	.00
EGDY/Q-	XA CB	CB002MHD	71		CN		0	1	/901 71	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
ENDISC/D-	XA CB	CB006MHD	46		CN		0	1	/904 46	CONN	.00
ENDISC/D-	XA CB	CB002MHD	75		CN		0	1	/901 75	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
ENDISC/O-	XA CB	CB006MHD	26		CN		0	1	/904 26	CONN	.00
ENDISC/O-	XA CB	CB002MHD	33		CN		0	1	/901 33	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
ENRFWB-	X CB	BTCCB3X	31		CN		0	1	/910 31	CONN	.00
ENRFWB-	X CB	BTCCB1X	35		CN		0	1	/907 35	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
HDSWST-	XA CB	CB004MHD	34		CN		0	1	/906 34	CONN	.00
HDSWST-	XA CB	CB001MHD	14		CN		0	1	/903 14	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IDCHKSR/Q	XA CB	CB001MHD	35		CN		0	1	/903 35	CONN	.00
IDCHKSR/Q	XA CB	CB003MHD	39		CN		0	1	/902 39	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IDCHKSR/Q-XA	CB	CB005MHD	68		CN		0	1	/905 68	CONN	.00
IDCHKSR/Q-XA	CB	CB001MHD	34		CN		0	1	/903 34	CONN	.00
IDCHKSR/Q-XA	CB	CB003MHD	38		CN		0	1	/902 38	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IDREAD/J	XA CB	CB004MHD	71		CN		0	1	/906 71	CONN	.00
IDREAD/J	XA CB	CB006MHD	42		CN		0	1	/904 42	CONN	.00
IDREAD/J	XA CB	CB003MHD	71		CN		0	1	/902 71	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IDREAD/Q-	XA CB	CB001MHD	28		CN		0	1	/903 28	CONN	.00
IDREAD/Q-	XA CB	CB003MHD	30		CN		0	1	/902 30	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IDWOPC/Q	XA CB	CB001MHD	41		CN		0	1	/903 41	CONN	.00
IDWOPC/Q	XA CB	CB003MHD	49		CN		0	1	/902 49	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
INDEXM	XA CB	CB004MHD	20		CN		0	1	/906 20	CONN	.00
INDEXM	XA CB	CB003MHD	76		CN		0	1	/902 76	CONN	.00
INDEXM	XA CB	CB002MHD	14		CN		0	1	/901 14	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
INTDFV-	CB	BTCCB0X	71		CN		0	1	/912 71	CONN	.00
INTDFV-	CB	BTCCB3X	32		CN		0	1	/910 32	CONN	.00
INTDFV-	CB	BTCCB3X	33		CN		0	1	/910 33	CONN	.00
INTDFV-	CB	BTCCB3X	34		CN		0	1	/910 34	CONN	.00
INTDFV-	CB	BTCCB3X	35		CN		0	1	/910 35	CONN	.00
INTDFV-	CB	BTCCB3X	36		CN		0	1	/910 36	CONN	.00
INTDFV-	CB	BTCCB3X	37		CN		0	1	/910 37	CONN	.00
INTDFV-	CB	BTCCB3X	38		CN		0	1	/910 38	CONN	.00
INTDFV-	CB	BTCCB3X	39		CN		0	1	/910 39	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
INTEN-	X CB	BTCCB3X	40		CN		0	1	/910 40	CONN	.00
INTEN-	X CB	CB004MHD	3		CN		0	1	/906 3	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
IRFCOGEV-	CB	BTCCBOX	29		CN		0	1	/912 29	CONN	.00

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
IREC0GDEV-	CB	BTCCB3X	41		CN		0	1	/910 41	CONN	.00
IREC0GDEV-	CB	BTCCB3X	42		CN		0	1	/910 42	CONN	.00
IREC0GDEV-	CB	BTCCB3X	43		CN		0	1	/910 43	CONN	.00
IREC0GDEV-	CB	BTCCB3X	44		CN		0	1	/910 44	CONN	.00
IREC0GDEV-	CB	BTCCB3X	45		CN		0	1	/910 45	CONN	.00
IREC0GDEV-	CB	BTCCB3X	46		CN		0	1	/910 46	CONN	.00
IREC0GDEV-	CB	BTCCB3X	47		CN		0	1	/910 47	CONN	.00
IREC0GDEV-	CB	BTCCB3X	48		CN		0	1	/910 48	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
LATL	XA	CB	CB004MHD	55			0	1	/906 55	CONN	.00
LAIL	XA	CB	CB005MHD	58			0	1	/905 58	CONN	.00
LAIL	XA	CB	CB002MHD	55			0	1	/901 55	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
LC2/Q-	X	CB	BTCCB3X	49			0	1	/910 49	CONN	.00
LC2/Q-	X	CB	BTCCB2X	45			0	1	/908 45	CONN	.00
LC2/Q-	X	CB	BTCCB1X	36			0	1	/907 36	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
LC3+LCNT4	X	CB	BTCCB3X	50			0	1	/910 50	CONN	.00
LC3+LCNT4	X	CB	BTCCB2X	75			0	1	/908 75	CONN	.00
LC3+LCNT4	X	CB	BTCCB1X	37			0	1	/907 37	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
LDSP-	XA	CB	CB005MHD	73			0	1	/905 73	CONN	.00
LDSP-	XA	CB	CB001MHD	64			0	1	/903 64	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L1STEN-	X	CB	BTCCB3X	51			0	1	/910 51	CONN	.00
L1STEN-	X	CB	CB003MHD	8			0	1	/902 8	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L1ST1	X	CB	BTCCB3X	52			0	1	/910 52	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L1ST2	X	CB	BTCCB3X	53			0	1	/910 53	CONN	.00
L1ST2	X	CB	BTCCB2X	46			0	1	/908 46	CONN	.00
L1ST2	X	CB	CB004MHD	12			0	1	/906 12	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L1ST3	X	CB	BTCCB3X	54			0	1	/910 54	CONN	.00
L1ST3	X	CB	CB001MHD	7			0	1	/903 7	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L1ST4	X	CB	BTCCB3X	55			0	1	/910 55	CONN	.00
L1ST4	X	CB	BTCCB1X	38			0	1	/907 38	CONN	.00
L1ST4	X	CB	CB004MHD	6			0	1	/906 6	CONN	.00
L1ST4	X	CB	CB003MHD	5			0	1	/902 5	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L5MF/Q	XA	CB	CB004MHD	65			0	1	/906 65	CONN	.00
L5MF/Q	XA	CB	CB001MHD	50			0	1	/903 50	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
L5MF/Q-	XA	CB	CB004MHD	64			0	1	/906 64	CONN	.00
L5MF/Q-	XA	CB	CB001MHD	49			0	1	/903 49	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
LW3CK-	XA	CB	CB004MHD	17			0	1	/906 17	CONN	.00
LW3CK-	XA	CB	CB005MHD	17			0	1	/905 17	CONN	.00
LW3CK-	XA	CB	CB001MHD	8			0	1	/903 8	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MC-	XA	CB	CB001MHD	63			0	1	/903 63	CONN	.00
MC-	XA	CB	CB002MHD	72			0	1	/901 72	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MC0MP	X	CB	BTCCB3X	56			0	1	/910 56	CONN	.00
MC0MP	X	CB	BTCCB2X	47			0	1	/908 47	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MC0-	X	CB	BTCCB3X	57			0	1	/910 57	CONN	.00
MC0-	X	CB	BTCCB2X	48			0	1	/908 48	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MC2/Q	X	CB	BTCCB2X	76			0	1	/908 76	CONN	.00
MC2/Q	X	CB	BTCCB1X	74			0	1	/907 74	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MC5+MC7-	X	CB	BTCCB2X	49			0	1	/908 49	CONN	.00
MC5+MC7-	X	CB	BTCCB1X	40			0	1	/907 40	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MEMEN-	X	CB	BTCCB3X	58			0	1	/910 58	CONN	.00
MEMEN-	X	CB	CB004MHD	15			0	1	/906 15	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MEMPD-	X	CB	BTCCB3X	75			0	1	/910 75	CONN	.00
MEMPD-	X	CB	BTCCB2X	6			0	1	/908 6	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MEMPAD	X	CB	BTCCB3X	59			0	1	/910 59	CONN	.00
MEMPAD	X	CB	BTCCB2X	50			0	1	/908 50	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MPESET-	CB	BTCCB3X	68		CN		0	1	/912 68	CONN	.00
MPESET-	CB	CB002MHD	3		CN		0	1	/901 3	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MR000/MHD	XA	CB	CB004MHD	21			0	1	/906 21	CONN	.00
MR000/MHD	XA	CB	CB005MHD	18			0	1	/905 18	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
MR001/MHD	XA	CB	CB004MHD	22			0	1	/906 22	CONN	.00
MR001/MHD	XA	CB	CB005MHD	19			0	1	/905 19	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
MRD02/MHD MRD02/MHD	XA XA	CB CB	C8004MHD C8005MHD	23 20	CN CN		0 0	1 1	/906 23 /905 20	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD03/MHD MRD03/MHD	XA XA	CB CB	C8004MHD C8005MHD	24 21	CN CN		0 0	1 1	/906 24 /905 21	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD04/MHD MRD04/MHD	XA XA	CB CB	C8004MHD C8005MHD	25 22	CN CN		0 0	1 1	/906 25 /905 22	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD05/MHD MRD05/MHD	XA XA	CB CB	C8004MHD C8005MHD	26 23	CN CN		0 0	1 1	/906 26 /905 23	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD06/MHD MRD06/MHD	XA XA	CB CB	C8004MHD C8005MHD	27 24	CN CN		0 0	1 1	/906 27 /905 24	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD07/MHD MRD07/MHD MRD07/MHD	XA XA XA	CB CB CB	C8004MHD C8005MHD C8001MHD	28 25 10	CN CN CN		0 0 0	1 1 1	/906 28 /905 25 /903 10	CONN CONN CONN	.00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD08 MRD08	X X	CB CB	BTCCB1X C8002MHD	41 4	CN CN		0 0	1 1	/907 41 /901 4	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD09 MRD09	X X	CB CB	BTCCB1X C8002MHD	42 7	CN CN		0 0	1 1	/907 42 /901 7	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD10 MRD10	X X	CB CB	BTCCB1X C8002MHD	43 9	CN CN		0 0	1 1	/907 43 /901 9	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD11 MRD11	X X	CB CB	BTCCB1X C8001MHD	44 67	CN CN		0 0	1 1	/907 44 /903 67	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRD12	X	CB	BTCCB1X	45	CN		0	1	/937 45	CONN	.00
MREST MREST	X X	CB CB	BTCCB1X C8006MHD	76 8	CN CN		0 0	1 1	/907 76 /904 8	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MREST- MRFST- MRFST-	XA XA XA	CB CB CB	C8006MHD C8003MHD C8002MHD	40 70 67	CN CN CN		0 0 0	1 1 1	/904 40 /902 70 /901 67	CONN CONN CONN	.00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRSMHD MRSMHD MRSMHD	XA XA XA	CB CB CB	C8004MHD C8005MHD C8001MHD	67 74 54	CN CN CN		0 0 0	1 1 1	/906 67 /935 74 /903 54	CONN CONN CONN	.00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MRSMHD- MRSMHD- MRSMHD- MRSMHD- MRSMHD-	XA XA XA XA XA	CB CB CB CB CB	C8004MHD C8006MHD C8001MHD C8003MHD C8002MHD	46 13 18 18 18	CN CN CN CN CN		0 0 0 0 0	1 1 1 1 1	/906 46 /904 13 /903 18 /902 18 /901 18	CONN CONN CONN CONN CONN	.00 .00 .00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWDCK- MWDCK-	XA XA	CB CB	C8005MHD C8003MHD	28 17	CN CN		0 0	1 1	/905 28 /902 17	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWDCKA2- MWDCKA2-	XA XA	CB CB	C8001MHD C8003MHD	39 47	CN CN		0 0	1 1	/903 39 /922 47	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWDSEL- MWDSEL- MWDSEL-	XA XA XA	CB CB CB	C8005MHD C8006MHD C8003MHD	53 16 22	CN CN CN		0 0 0	1 1 1	/905 53 /904 16 /902 22	CONN CONN CONN	.00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWD00/MHD MWD00/MHD MWD00/MHD	XA XA XA	CB CB CB	C8004MHD C8005MHD C8006MHD	35 31 11	CN CN CN		0 0 0	1 1 1	/906 35 /905 31 /904 11	CONN CONN CONN	.00 .00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWD01/MHD MWD01/MHD	XA XA	CB CB	C8005MHD C8006MHD	30 10	CN CN		0 0	1 1	/905 30 /904 10	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWD02/MHD MWD02/MHD	XA XA	CB CB	C8005MHD C8006MHD	29 9	CN CN		0 0	1 1	/905 29 /904 9	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
MWD03/MHD MWD03/MHD	XA XA	CB CB	C8005MHD C8006MHD	32 12	CN CN		0 0	1 1	/905 32 /904 12	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
NSCF NSCF	XA XA	CB CB	C8004MHD C8001MHD	45 16	CN CN		0 0	1 1	/906 45 /903 16	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
NSRB- NSRB-	XA XA	CB CB	C8004MHD C8001MHD	43 15	CN CN		0 0	1 1	/906 43 /933 15	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
NXSFSFL1 NXSFSFL1	XA XA	CB CB	C8004MHD C8005MHD	38 35	CN CN		0 0	1 1	/906 38 /905 35	CONN CONN	.00 .00
							NET LOADS *EXTERNAL SOURCE*				
NXSFSFL2	XA	CB	C8004MHD	40	CN		0	1	/906 40	CONN	.00

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LOAD LISTING FOR: PRODUCT CODE				MODULE	DATE 10/01/76	PAGE	8				
PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
NXSESEL2	XA CB	CB005MHD	37		CN		0	1	/905 37	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
NXSESEL3	XA CB	CB004MHD	37		CN		0	1	/906 37	CONN	.00
NXSESEL3	XA CB	CB005MHD	34		CN		0	1	/905 34	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
NXSESEL4	XA CB	CB004MHD	42		CN		0	1	/906 42	CONN	.00
NXSESEL4	XA CB	CB005MHD	39		CN		0	1	/905 39	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
NXSESEL5	XA CB	CB004MHD	44		CN		0	1	/906 44	CONN	.00
NXSESEL5	XA CB	CB005MHD	40		CN		0	1	/905 40	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
NXSESEL6	XA CB	CB004MHD	41		CN		0	1	/906 41	CONN	.00
NXSESEL6	XA CB	CB005MHD	38		CN		0	1	/905 38	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
DFLIN/D-	XA CB	CB006MHD	48		CN		0	1	/904 48	CONN	.00
DFLIN/D-	XA CB	CB002MHD	73		CN		0	1	/901 73	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
OPCOMP/D-	XA CB	CB006MHD	50		CN		0	1	/904 50	CONN	.00
OPCOMP/D-	XA CB	CB003MHD	74		CN		0	1	/902 74	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PAPER	X CB	BTCCB1X	46		CN		0	1	/907 46	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PARERR-	CB	BTCCBOX	75		CN		0	1	/912 75	CONN	.00
PARERR-	CB	BTCCB1X	47		CN		0	1	/907 47	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PARFLG/Q	XA CB	CB001MHD	58		CN		0	1	/903 58	CONN	.00
PARFLG/Q	XA CB	CB003MHD	69		CN		0	1	/902 69	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PARFLG/Q-	XA CB	CB001MHD	57		CN		0	1	/903 57	CONN	.00
PARFLG/Q-	XA CB	CB003MHD	68		CN		0	1	/902 68	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PLR1	XA CB	CB004MHD	19		CN		0	1	/906 19	CONN	.00
PLR1	XA CB	CB002MHD	13		CN		0	1	/901 13	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PROGER/D-	XA CB	CB004MHD	73		CN		0	1	/906 73	CONN	.00
PROGER/D-	XA CB	CB006MHD	45		CN		0	1	/904 45	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
PROGER/DA-XA	CB	CB004MHD	59		CN		0	1	/906 59	CONN	.00
PROGER/DA-XA	CB	CB003MHD	56		CN		0	1	/902 56	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RBUFUL/Q-	XA CB	CB001MHD	38		CN		0	1	/903 38	CONN	.00
RBUFUL/Q-	XA CB	CB003MHD	46		CN		0	1	/902 46	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RDATA	XA CB	CB005MHD	71		CN		0	1	/905 71	CONN	.00
RDATA	XA CB	CB001MHD	53		CN		0	1	/903 53	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RDATAP	XA CB	CB001MHD	60		CN		0	1	/903 60	CONN	.00
RDATAP	XA CB	CB002MHD	69		CN		0	1	/901 69	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ROCK-	XA CB	CB001MHD	24		CN		0	1	/903 24	CONN	.00
ROCK-	XA CB	CB002MHD	36		CN		0	1	/901 36	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
R0IDCOM	XA CB	CB004MHD	66		CN		0	1	/906 66	CONN	.00
R0IDCOM	XA CB	CB001MHD	51		CN		0	1	/903 51	CONN	.00
R0IDCOM	XA CB	CB003MHD	61		CN		0	1	/902 61	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
R0IDCOM-	XA CB	CB001MHD	27		CN		0	1	/903 27	CONN	.00
R0IDCOM-	XA CB	CB003MHD	29		CN		0	1	/902 29	CONN	.00
R0IDCOM-	XA CB	CB002MHD	42		CN		0	1	/901 42	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
R0OPFLG/J	XA CB	CB004MHD	53		CN		0	1	/906 53	CONN	.00
R0OPFLG/J	XA CB	CB003MHD	36		CN		0	1	/902 36	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
READY	X CB	BTCCB3X	60		CN		0	1	/910 60	CONN	.00
READY	X CB	CB005MHD	10		CN		0	1	/905 10	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
READYMHD	XA CB	CB005MHD	69		CN		0	1	/905 69	CONN	.00
READYMHD	XA CB	CB003MHD	41		CN		0	1	/902 41	CONN	.00
READYMHD	XA CB	CB002MHD	46		CN		0	1	/901 46	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RESET-	CB	BTCCBOX	31		CN		0	1	/912 31	CONN	.00
RESET-	CB	BTCCB1X	48		CN		0	1	/907 48	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RESETA-	X CB	BTCCB3X	61		CN		0	1	/910 61	CONN	.00
RESETA-	X CB	BTCCB2X	51		CN		0	1	/908 51	CONN	.00
RESETA-	X CB	BTCCB1X	49		CN		0	1	/907 49	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
RFOU00-	X CB	BTCCB2X	52		CN		0	1	/908 52	CONN	.00
RFOU00-	X CB	BTCCB1X	50		CN		0	1	/907 50	CONN	.00
RFOU00-	X CB	CB004MHD	8		CN		0	1	/906 8	CONN	.00
RFOU00-	X CB	CB006MHD	3		CN		0	1	/904 3	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				

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PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME	PIN	WIRING COMMENT	WIRE LENGTH
RFOUT01-	X CB	BTCC82X	53		CN		0	1	/938	53	CONN	.00
RFOUT01-	X CB	BTCC81X	51		CN		0	1	/907	51	CONN	.00
RFOUT01-	X CB	C8004MHD	11		CN		0	1	/906	11	CONN	.00
RFOUT01-	X CB	C8006MHD	4		CN		0	1	/904	4	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT02-	X CB	BTCC82X	54		CN		0	1	/908	54	CONN	.00
RFOUT02-	X CB	BTCC81X	52		CN		0	1	/907	52	CONN	.00
RFOUT02-	X CB	C8004MHD	16		CN		0	1	/906	16	CONN	.00
RFOUT02-	X CB	C8006MHD	7		CN		0	1	/904	7	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT03-	X CB	BTCC82X	55		CN		0	1	/908	55	CONN	.00
RFOUT03-	X CB	BTCC81X	53		CN		0	1	/907	53	CONN	.00
RFOUT03-	X CB	C8004MHD	14		CN		0	1	/906	14	CONN	.00
RFOUT03-	X CB	C8006MHD	5		CN		0	1	/904	5	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT04-	X CB	BTCC82X	56		CN		0	1	/908	56	CONN	.00
RFOUT04-	X CB	BTCC81X	54		CN		0	1	/907	54	CONN	.00
RFOUT04-	X CB	C8004MHD	5		CN		0	1	/906	5	CONN	.00
RFOUT04-	X CB	C8005MHD	6		CN		0	1	/905	6	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT05-	X CB	BTCC82X	57		CN		0	1	/908	57	CONN	.00
RFOUT05-	X CB	BTCC81X	55		CN		0	1	/907	55	CONN	.00
RFOUT05-	X CB	C8004MHD	10		CN		0	1	/906	10	CONN	.00
RFOUT05-	X CB	C8005MHD	9		CN		0	1	/905	9	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT06-	X CB	BTCC82X	58		CN		0	1	/908	58	CONN	.00
RFOUT06-	X CB	BTCC81X	56		CN		0	1	/907	56	CONN	.00
RFOUT06-	X CB	C8004MHD	4		CN		0	1	/906	4	CONN	.00
RFOUT06-	X CB	C8005MHD	5		CN		0	1	/905	5	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT07-	X CB	BTCC82X	59		CN		0	1	/908	59	CONN	.00
RFOUT07-	X CB	BTCC81X	57		CN		0	1	/907	57	CONN	.00
RFOUT07-	X CB	C8005MHD	13		CN		0	1	/905	13	CONN	.00
RFOUT07-	X CB	C8001MHD	6		CN		0	1	/903	6	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT08-	X CB	BTCC82X	60		CN		0	1	/908	60	CONN	.00
RFOUT08-	X CB	BTCC81X	58		CN		0	1	/907	58	CONN	.00
RFOUT08-	X CB	C8005MHD	14		CN		0	1	/905	14	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT09-	X CB	BTCC82X	61		CN		0	1	/908	61	CONN	.00
RFOUT09-	X CB	BTCC81X	59		CN		0	1	/907	59	CONN	.00
RFOUT09-	X CB	C8005MHD	4		CN		0	1	/905	4	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT10-	X CB	BTCC82X	62		CN		0	1	/908	62	CONN	.00
RFOUT10-	X CB	BTCC81X	60		CN		0	1	/907	60	CONN	.00
RFOUT10-	X CB	C8005MHD	15		CN		0	1	/905	15	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT11-	X CB	BTCC82X	63		CN		0	1	/908	63	CONN	.00
RFOUT11-	X CB	BTCC81X	61		CN		0	1	/907	61	CONN	.00
RFOUT11-	X CB	C8005MHD	8		CN		0	1	/905	8	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT12-	X CB	BTCC82X	64		CN		0	1	/908	64	CONN	.00
RFOUT12-	X CB	BTCC81X	62		CN		0	1	/907	62	CONN	.00
RFOUT12-	X CB	C8005MHD	12		CN		0	1	/905	12	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT13-	X CB	BTCC82X	65		CN		0	1	/908	65	CONN	.00
RFOUT13-	X CB	BTCC81X	63		CN		0	1	/907	63	CONN	.00
RFOUT13-	X CB	C8005MHD	7		CN		0	1	/905	7	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT14-	X CB	BTCC82X	66		CN		0	1	/908	66	CONN	.00
RFOUT14-	X CB	BTCC81X	64		CN		0	1	/907	64	CONN	.00
RFOUT14-	X CB	C8005MHD	3		CN		0	1	/905	3	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFOUT15-	X CB	BTCC82X	67		CN		0	1	/908	67	CONN	.00
RFOUT15-	X CB	BTCC81X	65		CN		0	1	/907	65	CONN	.00
RFOUT15-	X CB	C8005MHD	16		CN		0	1	/905	16	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFADD1	X CB	BTCC83X	62		CN		0	1	/910	62	CONN	.00
RFADD1	X CB	BTCC81X	66		CN		0	1	/907	66	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RFWADD1	X CB	BTCC83X	64		CN		0	1	/910	64	CONN	.00
RFWADD1	X CB	BTCC81X	68		CN		0	1	/907	68	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RF4EN	X CB	BTCC83X	65		CN		0	1	/910	65	CONN	.00
RF4EN	X CB	C8003MHD	3		CN		0	1	/902	3	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RG/Q	XA CB	C8001MHD	56		CN		0	1	/903	56	CONN	.00
RG/Q	XA CB	C8002MHD	64		CN		0	1	/901	64	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RG/Q-	XA CB	C8001MHD	55		CN		0	1	/903	55	CONN	.00
RG/Q-	XA CB	C8002MHD	63		CN		0	1	/901	63	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RTS/R/W	XA CB	C8003MHD	48		CN		0	1	/902	48	CONN	.00
RTS/R/W	XA CB	C8002MHD	51		CN		0	1	/901	51	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*			
RYSWP/Q	XA CB	C8003MHD	37		CN		0	1	/902	37	CONN	.00
RYSWP/Q	XA CB	C8002MHD	45		CN		0	1	/901	45	CONN	.00

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PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
0 NET LOADS *EXTERNAL SOURCE*											
RYSWR/Q-	XA CB	C8003MHD	65		CN		0	1	/902 65	CONN	.00
RYSWR/Q-	XA CB	C8002MHD	65		CN		0	1	/901 65	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SCLOCK	X CB	BTCCB1X	69		CN		0	1	/907 69	CONN	.00
SCLOCK	X CB	C8002MHD	11		CN		0	1	/901 11	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SC4/Q-	X CB	BTCCB3X	66		CN		0	1	/910 66	CONN	.00
SC4/Q-	X CB	BTCCB1X	70		CN		0	1	/907 70	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SC4,5-	X CB	BTCCB3X	67		CN		0	1	/910 67	CONN	.00
SC4,5-	X CB	BTCCB2X	68		CN		0	1	/908 68	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SC5/Q	X CB	BTCCB3X	68		CN		0	1	/910 68	CONN	.00
SC5/Q	X CB	BTCCB2X	69		CN		0	1	/908 69	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SC5/Q-	X CB	BTCCB3X	63		CN		0	1	/910 63	CONN	.00
SC5/Q-	X CB	BTCCB1X	67		CN		0	1	/907 67	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SH15	XA CB	C8005MHD	51		CN		0	1	/905 51	CONN	.00
SH15	XA CB	C8001MHD	21		CN		0	1	/903 21	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SIGSTA/Q-	XA CB	C8004MHD	52		CN		0	1	/906 52	CONN	.00
SIGSTA/Q-	XA CB	C8001MHD	30		CN		0	1	/903 30	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SIGSTAR/Q	XA CB	C8004MHD	60		CN		0	1	/906 60	CONN	.00
SIGSTAR/Q	XA CB	C8001MHD	45		CN		0	1	/903 45	CONN	.00
SIGSTAR/Q	XA CB	C8003MHD	57		CN		0	1	/902 57	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SIGSTA1/Q	XA CB	C8004MHD	61		CN		0	1	/906 61	CONN	.00
SIGSTA1/Q	XA CB	C8002MHD	59		CN		0	1	/901 59	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SKOPFLG/J	XA CB	C8004MHD	68		CN		0	1	/906 68	CONN	.00
SKOPFLG/J	XA CB	C8003MHD	66		CN		0	1	/902 66	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SKOPFLG/K	XA CB	C8003MHD	67		CN		0	1	/902 67	CONN	.00
SKOPFLG/K	XA CB	C8002MHD	66		CN		0	1	/901 66	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SKOPFLG/Q	XA CB	C8003MHD	51		CN		0	1	/902 51	CONN	.00
SKOPFLG/Q	XA CB	C8002MHD	54		CN		0	1	/901 54	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SKOPFLG/Q-XA	CB	C8003MHD	43		CN		0	1	/902 43	CONN	.00
SKOPFLG/Q-XA	CB	C8002MHD	48		CN		0	1	/901 48	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SK1/Q-	XA CB	C8001MHD	25		CN		0	1	/903 25	CONN	.00
SK1/Q-	XA CB	C8002MHD	38		CN		0	1	/901 38	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SK2/J	XA CB	C8004MHD	56		CN		0	1	/906 56	CONN	.00
SK2/J	XA CB	C8002MHD	56		CN		0	1	/901 56	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SK2/K	XA CB	C8004MHD	51		CN		0	1	/906 51	CONN	.00
SK2/K	XA CB	C8003MHD	27		CN		0	1	/902 27	CONN	.00
SK2/K	XA CB	C8002MHD	40		CN		0	1	/901 40	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SK2/Q-	XA CB	C8004MHD	50		CN		0	1	/906 50	CONN	.00
SK2/Q-	XA CB	C8001MHD	26		CN		0	1	/903 26	CONN	.00
SK2/Q-	XA CB	C8002MHD	39		CN		0	1	/901 39	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SRO/J	XA CB	C8006MHD	33		CN		0	1	/904 33	CONN	.00
SRO/J	XA CB	C8003MHD	40		CN		0	1	/902 40	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SRO/K	XA CB	C8001MHD	32		CN		0	1	/903 32	CONN	.00
SRO/K	XA CB	C8003MHD	34		CN		0	1	/902 34	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SRI/J	XA CB	C8003MHD	32		CN		0	1	/902 32	CONN	.00
SRI/J	XA CB	C8002MHD	44		CN		0	1	/901 44	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SRI/Q	XA CB	C8001MHD	65		CN		0	1	/903 65	CONN	.00
SRI/Q	XA CB	C8003MHD	63		CN		0	1	/902 63	CONN	.00
SRI/Q	XA CB	C8002MHD	61		CN		0	1	/901 61	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
SRI/Q-	XA CB	C8005MHD	67		CN		0	1	/905 67	CONN	.00
SRI/Q-	XA CB	C8002MHD	43		CN		0	1	/901 43	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
STATRUSY	X CB	BTCCB3X	70		CN		0	1	/910 70	CONN	.00
STATRUSY	X CB	BTCCB2X	71		CN		0	1	/908 71	CONN	.00
STATRUSY	X CB	C8005MHD	11		CN		0	1	/905 11	CONN	.00
STATRUSY	X CB	C8002MHD	6		CN		0	1	/901 6	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											
STATRUSY-	XA CB	C8003MHD	28		CN		0	1	/902 28	CONN	.00
STATRUSY-	XA CB	C8002MHD	41		CN		0	1	/901 41	CONN	.00
0 NET LOADS *EXTERNAL SOURCE*											

PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	WIRE LENGTH
STATEN-	X CB	BTCCB3X	71		CN		0	1	/910 71	CONN	.00
STATEN-	X CB	BTCCB1X	71		CN		0	1	/937 71	CONN	.00
STATEN-	X CB	CB006MHD	6		CN		0	1	/904 6	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STATR1CK-	XA CB	CB006MHD	49		CN		0	1	/904 49	CONN	.00
STATR1CK-	XA CB	CB002MHD	74		CN		0	1	/901 74	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STATR3CK-	XA CB	CB006MHD	25		CN		0	1	/904 25	CONN	.00
STATR3CK-	XA CB	CB002MHD	32		CN		0	1	/901 32	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STATSEL-	XA CB	CB005MHD	52		CN		0	1	/905 52	CONN	.00
STATSEL-	XA CB	CB006MHD	15		CN		0	1	/904 15	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT04-	XA CB	CB005MHD	55		CN		0	1	/905 55	CONN	.00
STAT04-	XA CB	CB006MHD	18		CN		0	1	/904 18	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT05-	XA CB	CB005MHD	54		CN		0	1	/905 54	CONN	.00
STAT05-	XA CB	CB006MHD	17		CN		0	1	/904 17	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT06-	XA CB	CB005MHD	57		CN		0	1	/905 57	CONN	.00
STAT06-	XA CB	CB006MHD	20		CN		0	1	/904 20	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT07-	XA CB	CB005MHD	56		CN		0	1	/905 56	CONN	.00
STAT07-	XA CB	CB006MHD	19		CN		0	1	/904 19	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT08-	XA CB	CB005MHD	59		CN		0	1	/905 59	CONN	.00
STAT08-	XA CB	CB006MHD	22		CN		0	1	/904 22	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT10-	XA CB	CB005MHD	61		CN		0	1	/905 61	CONN	.00
STAT10-	XA CB	CB006MHD	24		CN		0	1	/904 24	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT11-	XA CB	CB005MHD	60		CN		0	1	/905 60	CONN	.00
STAT11-	XA CB	CB006MHD	23		CN		0	1	/904 23	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT12-	XA CB	CB005MHD	63		CN		0	1	/905 63	CONN	.00
STAT12-	XA CB	CB002MHD	29		CN		0	1	/901 29	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT13-	XA CB	CB005MHD	62		CN		0	1	/905 62	CONN	.00
STAT13-	XA CB	CB002MHD	28		CN		0	1	/901 28	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT14-	XA CB	CB005MHD	65		CN		0	1	/905 65	CONN	.00
STAT14-	XA CB	CB002MHD	31		CN		0	1	/901 31	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
STAT15-	XA CB	CB005MHD	64		CN		0	1	/905 64	CONN	.00
STAT15-	XA CB	CB002MHD	30		CN		0	1	/901 30	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
ST1/J	XA CB	CB006MHD	37		CN		0	1	/904 37	CONN	.00
ST1/J	XA CB	CB002MHD	58		CN		0	1	/901 58	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
ST1/J-	XA CB	CB006MHD	30		CN		0	1	/904 30	CONN	.00
ST1/J-	XA CB	CB002MHD	37		CN		0	1	/901 37	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SW1/O	XA CB	CB001MHD	42		CN		0	1	/903 42	CONN	.00
SW1/O	XA CB	CB003MHD	52		CN		0	1	/902 52	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SW2	XA CB	CB005MHD	50		CN		0	1	/905 50	CONN	.00
SW2	XA CB	CB003MHD	21		CN		0	1	/902 21	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SW2/O-	XA CB	CB001MHD	31		CN		0	1	/903 31	CONN	.00
SW2/O-	XA CB	CB003MHD	33		CN		0	1	/902 33	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SYCKMHD	XA CB	CB004MHD	18		CN		0	1	/906 18	CONN	.00
SYCKMHD	XA CB	CB001MHD	9		CN		0	1	/903 9	CONN	.00
SYCKMHD	XA CB	CB003MHD	10		CN		0	1	/902 10	CONN	.00
SYCKMHD	XA CB	CB002MHD	12		CN		0	1	/901 12	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SYCKMHD-	XA CB	CB004MHD	74		CN		0	1	/906 74	CONN	.00
SYCKMHD-	XA CB	CB006MHD	14		CN		0	1	/904 14	CONN	.00
SYCKMHD-	XA CB	CB001MHD	19		CN		0	1	/903 19	CONN	.00
SYCKMHD-	XA CB	CB003MHD	19		CN		0	1	/902 19	CONN	.00
SYCKMHD-	XA CB	CB002MHD	19		CN		0	1	/901 19	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SYCKMHQJ	XA CB	CB004MHD	47		CN		0	1	/906 47	CONN	.00
SYCKMHQJ	XA CB	CB003MHD	20		CN		0	1	/902 20	CONN	.00
SYCKMHQJ	XA CB	CB002MHD	20		CN		0	1	/901 20	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SYCL-	X CB	BTCCB3X	72		CN		0	1	/910 72	CONN	.00
SYCL-	X CB	BTCCB2X	72		CN		0	1	/908 72	CONN	.00
SYCL-	X CB	BTCCB1X	73		CN		0	1	/907 73	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		
SYNCLK	XA CB	CB004MHD	63		CN		0	1	/906 63	CONN	.00
SYNCLK	XA CB	CB005MHD	70		CN		0	1	/905 70	CONN	.00
SYNCLK	XA CB	CB001MHD	48		CN		0	1	/903 48	CONN	.00
							0 NET LOADS		*EXTERNAL SOURCE*		

LOAD LISTING FOR: PRODUCT CODE						MODULE	DATE 10/01/76	PAGE	12		
PIN SIGNATURE	CIRCUIT TYPE	DEVICE NAME	PIN NAME	WIRE CODE	PIN FUNC	CKT FREQ.	N+ LOAD	BLOCK NUMBER	LOCATION NAME PIN	WIRING COMMENT	# WIRE LENGTH
SYNR/Q-	XA CB	C8001MHD	40		CN		0	1	/903 40	CONN	.00
SYNR/Q-	XA CB	C8002MHD	52		CN		0	1	/901 52	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
TERM-	XA CB	C8006MHD	34		CN		0	1	/904 34	CONN	.00
TERM-	XA CB	C8003MHD	42		CN		0	1	/902 42	CONN	.00
TERM-	XA CB	C8002MHD	47		CN		0	1	/901 47	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
TWOSC	X CB	BTCCB3X	73		CN		0	1	/910 73	CONN	.00
TWOSC	X CB	C8001MHD	3		CN		0	1	/903 3	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
UNSKFSETENXA	CB	C8004MHD	54		CN		0	1	/906 54	CONN	.00
UNSKFSETENXA	CB	C8003MHD	50		CN		0	1	/902 50	CONN	.00
UNSKFSETENXA	CB	C8002MHD	53		CN		0	1	/901 53	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
UPHD/Q	XA CB	C8001MHD	37		CN		0	1	/903 37	CONN	.00
UPHD/Q	XA CB	C8002MHD	50		CN		0	1	/901 50	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WC=O/Q	XA CB	C8005MHD	66		CN		0	1	/905 66	CONN	.00
WC=O/Q	XA CB	C8006MHD	31		CN		0	1	/904 31	CONN	.00
WC=O/Q	XA CB	C8003MHD	26		CN		0	1	/902 26	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WCHK/Q-	XA CB	C8003MHD	45		CN		0	1	/902 45	CONN	.00
WCHK/Q-	XA CB	C8002MHD	49		CN		0	1	/901 49	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WDNCK	XA CB	C8001MHD	59		CN		0	1	/903 59	CONN	.00
WDNCK	XA CB	C8002MHD	68		CN		0	1	/901 68	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WG/Q	XA CB	C8001MHD	61		CN		0	1	/903 61	CONN	.00
WG/Q	XA CB	C8002MHD	70		CN		0	1	/901 70	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WLKOUT/Q	XA CB	C8004MHD	49		CN		0	1	/906 49	CONN	.00
WLKOUT/Q	XA CB	C8005MHD	49		CN		0	1	/905 49	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WLKTON/Q-	XA CB	C8004MHD	70		CN		0	1	/906 70	CONN	.00
WLKTON/Q-	XA CB	C8006MHD	41		CN		0	1	/904 41	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WOMKDP/Q-	XA CB	C8001MHD	23		CN		0	1	/903 23	CONN	.00
WOMKDR/Q-	XA CB	C8003MHD	25		CN		0	1	/902 25	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WOMKSP	XA CB	C8001MHD	22		CN		0	1	/903 22	CONN	.00
WOMKSP	XA CB	C8003MHD	24		CN		0	1	/902 24	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WPS	XA CB	C8006MHD	38		CN		0	1	/904 38	CONN	.00
WPS	XA CB	C8002MHD	60		CN		0	1	/901 60	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WRIDCOM	XA CB	C8004MHD	62		CN		0	1	/906 62	CONN	.00
WRIDCOM	XA CB	C8003MHD	60		CN		0	1	/902 60	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
WRTOPFLG/QXA	CB	C8004MHD	57		CN		0	1	/906 57	CONN	.00
WRTOPFLG/QXA	CB	C8006MHD	35		CN		0	1	/904 35	CONN	.00
WRTOPFLG/QXA	CB	C8003MHD	53		CN		0	1	/902 53	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ZER016	X CB	BTCCB2X	73		CN		0	1	/908 73	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
ZER08	X CB	BTCCB2X	74		CN		0	1	/908 74	CONN	.00
ZER08	X CB	C8004MHD	7		CN		0	1	/906 7	CONN	.00
ZER08	X CB	C8001MHD	5		CN		0	1	/903 5	CONN	.00
ZER08	X CB	C8003MHD	6		CN		0	1	/902 6	CONN	.00
							0 NET LOADS *EXTERNAL SOURCE*				
31/445IGNAL	CB	C8004MHD	39		CN		0	1	/906 39	CONN	.00
31/445IGNAL	CB	C8005MHD	36		CN		0	1	/905 36	CONN	.00
31/445IGNAL	CB	C8001MHD	68		CN		0	1	/903 68	CONN	.00



944824-9701

PIN LIST

Drawing No. 961711-9921

LOCATION /901				CIRCUIT TYPE CB				BLOCK	1	GATE				
1			CONN	2			CONN	3						
4	MPD08	X	C8002MHD	CONN	5	BUSY-	X	C8002MHD	CONN	6	MPRESET-	C8002MHD	CONN	
7	MPD09	X	C8002MHD	CONN	8	AT11	X	C8002MHD	CONN	9	STATBUSY	X	C8002MHD	CONN
10	DEVBSY/Q	X	C8002MHD	CONN	11	SCLOCK	X	C8002MHD	CONN	12	MRD10	X	C8002MHD	CONN
13	PLR1	XA	C8002MHD	CONN	14	INDEXM	XA	C8002MHD	CONN	15	SYCKMHD	XA	C8002MHD	CONN
16	CYLAD7	XA	C8002MHD	CONN	17	BTCLR	XA	C8002MHD	CONN	18	BUSY/DB2-	XA	C8002MHD	CONN
19	SYCKMHD-	XA	C8002MHD	CONN	20	SYCKMHDJ	XA	C8002MHD	CONN	21	MRSMHD-	XA	C8002MHD	CONN
22	CYLAD2	XA	C8002MHD	CONN	23	CYLAD1	XA	C8002MHD	CONN	24	CYLAD3	XA	C8002MHD	CONN
25	CYLAD6	XA	C8002MHD	CONN	26	CYLAD5	XA	C8002MHD	CONN	27	CYLAD4	XA	C8002MHD	CONN
28	STAT13-	XA	C8002MHD	CONN	29	STAT12-	XA	C8002MHD	CONN	30	STAT15-	XA	C8002MHD	CONN
31	STAT14-	XA	C8002MHD	CONN	32	STATR3CK-	XA	C8002MHD	CONN	33	ENDISC/Q-	XA	C8002MHD	CONN
34	CHLTKN/Q-	XA	C8002MHD	CONN	35	BUSY/Q-	XA	C8002MHD	CONN	36	RDCK-	XA	C8002MHD	CONN
37	ST1/J-	XA	C8002MHD	CONN	38	SK1/Q-	XA	C8002MHD	CONN	39	SK2/Q-	XA	C8002MHD	CONN
40	SK2/K	XA	C8002MHD	CONN	41	STATBUSY-	XA	C8002MHD	CONN	42	RDIIDCOM-	XA	C8002MHD	CONN
43	SR1/Q-	XA	C8002MHD	CONN	44	SR1/J	XA	C8002MHD	CONN	45	RYSMR/Q	XA	C8002MHD	CONN
46	READYMHD	XA	C8002MHD	CONN	47	TERM-	XA	C8002MHD	CONN	48	SKOPFLG/Q-	XA	C8002MHD	CONN
49	WCHK/Q-	XA	C8002MHD	CONN	50	UPHD/Q	XA	C8002MHD	CONN	51	RTS/R/W	XA	C8002MHD	CONN
52	SYNR/Q-	XA	C8002MHD	CONN	53	UNSKFSETENXA	C8002MHD	CONN	54	SKOPFLG/Q	XA	C8002MHD	CONN	
55	LAIL	XA	C8002MHD	CONN	56	SK2/J	XA	C8002MHD	CONN	57	BUSY/D-	XA	C8002MHD	CONN
58	ST1/J	XA	C8002MHD	CONN	59	SIGSTA1/Q	XA	C8002MHD	CONN	60	WPS	XA	C8002MHD	CONN
61	SR1/Q	XA	C8002MHD	CONN	62	BUFFUL/Q	XA	C8002MHD	CONN	63	RG/Q-	XA	C8002MHD	CONN
64	RG/Q	XA	C8002MHD	CONN	65	RYSMR/Q-	XA	C8002MHD	CONN	66	SKOPFLG/K	XA	C8002MHD	CONN
67	MPEST-	XA	C8002MHD	CONN	68	WONCK	XA	C8002MHD	CONN	69	RDATAP	XA	C8002MHD	CONN
70	WG/Q	XA	C8002MHD	CONN	71	EGDY/Q-	XA	C8002MHD	CONN	72	MC-	XA	C8002MHD	CONN
73	OFLIN/D-	XA	C8002MHD	CONN	74	STATP1CK-	XA	C8002MHD	CONN	75	ENDISC/D-	XA	C8002MHD	CONN
76	AT12	X	C8002MHD	CONN	77			CONN	78					
79			CONN	80			CONN							

LOCATION /902				CIRCUIT TYPE CB				BLOCK	1	GATE				
1			CONN	2			CONN	3						
4	DECOUNT-	X	C8003MHD	CONN	5	LIST4	X	C8003MHD	CONN	6	RF4EN	X	C8003MHD	CONN
7	ACK-	X	C8003MHD	CONN	8	LISTEN-	X	C8003MHD	CONN	9	ZERO8	X	C8003MHD	CONN
10	SYCKMHD	XA	C8003MHD	CONN	11	BUSY/DB2-	XA	C8003MHD	CONN	12	AT12	X	C8003MHD	CONN
13	CHAIN-	XA	C8003MHD	CONN	14	COMM1-	XA	C8003MHD	CONN	15	CHAIN	XA	C8003MHD	CONN
16	CPCK-	XA	C8003MHD	CONN	17	WMOCK-	XA	C8003MHD	CONN	18	CRCLR-	XA	C8003MHD	CONN
19	SYCKMHD-	XA	C8003MHD	CONN	20	SYCKMHDJ	XA	C8003MHD	CONN	21	MRSMHD-	XA	C8003MHD	CONN
22	WMOSEL-	XA	C8003MHD	CONN	23	DATRETR/Q-	XA	C8003MHD	CONN	24	SM2	XA	C8003MHD	CONN
25	WCHKDR/Q-	XA	C8003MHD	CONN	26	MC=0/Q	XA	C8003MHD	CONN	27	WOMKSR	XA	C8003MHD	CONN
28	STATBUSY-	XA	C8003MHD	CONN	29	RDIIDCOM-	XA	C8003MHD	CONN	30	SK2/K	XA	C8003MHD	CONN
31	DPSTARTRB1	XA	C8003MHD	CONN	32	RDIIDCOM-	XA	C8003MHD	CONN	33	IDREAD/Q-	XA	C8003MHD	CONN
34	SRO/K	XA	C8003MHD	CONN	35	SR1/J	XA	C8003MHD	CONN	36	SM2/Q-	XA	C8003MHD	CONN
37	RYSMR/Q	XA	C8003MHD	CONN	38	COMPOP-	XA	C8003MHD	CONN	39	RDOPFLG/J	XA	C8003MHD	CONN
40	SRO/J	XA	C8003MHD	CONN	41	IDCHKSR/Q-	XA	C8003MHD	CONN	42	IDCHKSR/Q	XA	C8003MHD	CONN
43	SKOPFLG/Q-	XA	C8003MHD	CONN	44	READYMHD	XA	C8003MHD	CONN	43	TERM-	XA	C8003MHD	CONN
46	RUFUL/Q-	XA	C8003MHD	CONN	47	BCCRY	XA	C8003MHD	CONN	45	WCHK/Q-	XA	C8003MHD	CONN
49	IDWORD/Q	XA	C8003MHD	CONN	48	WMOCKA2-	XA	C8003MHD	CONN	48	RTS/R/W	XA	C8003MHD	CONN
52	SM1/Q	XA	C8003MHD	CONN	50	UNSKFSETENXA	C8003MHD	CONN	51	SKOPFLG/Q	XA	C8003MHD	CONN	
55	DRMHD/Q	XA	C8003MHD	CONN	53	WRTOPFLG/QXA	C8003MHD	CONN	54	COMERR/Q	XA	C8003MHD	CONN	
58	BCCRY-	XA	C8003MHD	CONN	56	PROGER/DA-	XA	C8003MHD	CONN	57	SIGSTAB/O	XA	C8003MHD	CONN
61	RDIIDCOM	XA	C8003MHD	CONN	59	DWO	XA	C8003MHD	CONN	60	WRIDCOM	XA	C8003MHD	CONN
64	RUFFUL/Q	XA	C8003MHD	CONN	62	CHLTKN/D-	XA	C8003MHD	CONN	63	SR1/Q	XA	C8003MHD	CONN
67	SKOPFLG/K	XA	C8003MHD	CONN	65	RYSMR/Q-	XA	C8003MHD	CONN	66	SKOPFLG/J	XA	C8003MHD	CONN
70	MPEST-	XA	C8003MHD	CONN	68	PARFLG/Q-	XA	C8003MHD	CONN	69	PARFLG/Q	XA	C8003MHD	CONN
73	DATRETR/D-	XA	C8003MHD	CONN	71	IDREAD/J	XA	C8003MHD	CONN	72	COMPER/D-	XA	C8003MHD	CONN
76	INDEXM	XA	C8003MHD	CONN	74	OPCOMP/D-	XA	C8003MHD	CONN	75	DEVBSY/Q	XA	C8003MHD	CONN
79			CONN	80			CONN	78						

LOCATION /903				CIRCUIT TYPE CB				BLOCK	1	GATE				
1			CONN	2			CONN	3						
4	COJNT	X	C8001MHD	CONN	5	ZERO8	X	C8001MHD	CONN	6	TWOSC	X	C8001MHD	CONN
7	LIST3	XA	C8001MHD	CONN	8	LW3CK-	XA	C8001MHD	CONN	9	RFOUT07-	X	C8001MHD	CONN
10	MRD07/MHD	XA	C8001MHD	CONN	11	COMM1-	XA	C8001MHD	CONN	12	SYCKMHD	XA	C8001MHD	CONN
13	COMM3-	XA	C8001MHD	CONN	14	HDSWST-	XA	C8001MHD	CONN	15	COMM2	XA	C8001MHD	CONN
16	NSCE	XA	C8001MHD	CONN	17	BTCLR	XA	C8001MHD	CONN	18	NS00-	XA	C8001MHD	CONN
19	SYCKMHD-	XA	C8001MHD	CONN	20	CYL INC/Q-	XA	C8001MHD	CONN	21	MRSMHD-	XA	C8001MHD	CONN
22	WOMKSR	XA	C8001MHD	CONN	23	CYLAD1	XA	C8001MHD	CONN	24	SH15	XA	C8001MHD	CONN
25	SK1/Q-	XA	C8001MHD	CONN	26	WOMKDR/Q-	XA	C8001MHD	CONN	27	RDCK-	XA	C8001MHD	CONN
28	IDREAD/Q-	XA	C8001MHD	CONN	29	SK2/Q-	XA	C8001MHD	CONN	30	RDIIDCOM-	XA	C8001MHD	CONN
31	SW2/Q-	XA	C8001MHD	CONN	32	DRSTARTB1	XA	C8001MHD	CONN	31	SIGSTA/Q-	XA	C8001MHD	CONN
34	IDCHKSR/Q-	XA	C8001MHD	CONN	35	SRO/K	XA	C8001MHD	CONN	33	COMPOP-	XA	C8001MHD	CONN
37	UPHD/Q	XA	C8001MHD	CONN	38	IDCHKSR/Q	XA	C8001MHD	CONN	36	BCCRY	XA	C8001MHD	CONN
40	SYNR/Q-	XA	C8001MHD	CONN	39	RUFFUL/Q-	XA	C8001MHD	CONN	39	WMOCKA2-	XA	C8001MHD	CONN
43	COMERR/Q	XA	C8001MHD	CONN	41	IDWORD/Q	XA	C8001MHD	CONN	42	SM1/Q	XA	C8001MHD	CONN
46	BCCRY-	XA	C8001MHD	CONN	44	DRMHD/Q	XA	C8001MHD	CONN	45	SIGSTAB/O	XA	C8001MHD	CONN
49	LSMF/Q-	XA	C8001MHD	CONN	47	DWO	XA	C8001MHD	CONN	48	SYNCK	XA	C8001MHD	CONN
52	RUFFUL/Q	XA	C8001MHD	CONN	50	LSMF/Q	XA	C8001MHD	CONN	51	RDIIDCOM	XA	C8001MHD	CONN
55	RG/Q-	XA	C8001MHD	CONN	53	RDATA	XA	C8001MHD	CONN	54	MRSMHD	XA	C8001MHD	CONN
58	PARFLG/Q	XA	C8001MHD	CONN	56	RG/Q	XA	C8001MHD	CONN	57	PARFLG/Q-	XA	C8001MHD	CONN
61	WG/Q	XA	C8001MHD	CONN	59	WONCK	XA	C8001MHD	CONN	60	RDATAP	XA	C8001MHD	CONN
64	LSR-	XA	C8001MHD	CONN	62	EGDY/Q-	XA	C8001MHD	CONN	63	MC-	XA	C8001MHD	CONN
67	MRD11	X	C8001MHD	CONN	65	SR1/Q	XA	C8001MHD	CONN	66	BITOSC	XA	C8001MHD	CONN
70			CONN	68	31/44SIGNAL	C8001MHD	CONN	69						
73			CONN	71			CONN	72						
76			CONN	74			CONN	75						
79			CONN	77			CONN	78						

LOCATION /904				CIRCUIT TYPE CB				BLOCK	1	GATE				
1			CONN	2			CONN	3						
4	RFOUT01-	X	C8006MHD	CONN	5	RFOUT03-	X	C8006MHD	CONN	6	RFOUT00-	X	C8006MHD	CONN
7	RFOUT02-	X	C8006MHD	CONN	8	MPREST	X	C8006MHD	CONN	9	STATEN-	X	C8006MHD	CONN
10	MRD01/MHD	XA	C8006MHD	CONN	11	MRD00/MHD	XA	C8006MHD	CONN	12	MRD02/MHD	XA	C8006MHD	CONN
13	MFSMHD-	XA	C8006MHD	CONN	14	SYCKMHD-	XA	C8006MHD	CONN	15	MRD03/MHD	XA	C8006MHD	CONN
16	MWDSSEL-	XA	C8006MHD	CONN	17	STAT05-	XA	C8006MHD	CONN	18	STATSEL-	XA	C8006MHD	CONN
19	STAT07-	XA	C8006MHD	CONN	20	STAT06-	XA	C8006MHD	CONN	21	STAT04-	XA	C8006MHD	CONN
22	STAT08-	XA	C8006MHD	CONN	23	STAT11-	XA	C8006MHD	CONN	22	BITOSC	XA	C8006MHD	CONN
25	STATR3CK-	XA	C8006MHD	CONN	26	ENDISC/Q-	XA	C8006MHD	CONN	24	STAT10-	XA	C8006MHD	CONN
								27	DATRETR/Q-	XA	C8006MHD	CONN		

28	CHLTKN/Q-	XA	C8006MHD	CONN	29	BUSY/Q-	XA	C8006MHD	CONN	30	ST1/J-	XA	C8006MHD	CONN
31	WC=O/Q	XA	C8006MHD	CONN	32	COMPOP-	XA	C8006MHD	CONN	33	SRO/J	XA	C8006MHD	CONN
34	TERM-	XA	C8006MHD	CONN	35	WPTOPFLG/QXA	XA	C8006MHD	CONN	36	BUSY/D-	XA	C8006MHD	CONN
37	ST1/J	XA	C8006MHD	CONN	38	WPS	XA	C8006MHD	CONN	39	CHLTKN/D-	XA	C8006MHD	CONN
40	MREST-	XA	C8006MHD	CONN	41	WLKTON/D-	XA	C8006MHD	CONN	42	IDREAD/J	XA	C8006MHD	CONN
43	CRC=O-	XA	C8006MHD	CONN	44	COMPER/D-	XA	C8006MHD	CONN	45	PROGER/D-	XA	C8006MHD	CONN
46	ENDISC/D-	XA	C8006MHD	CONN	47	DATFR/D-	XA	C8006MHD	CONN	48	OFLIN/D-	XA	C8006MHD	CONN
49	STATRICK-	XA	C8006MHD	CONN	50	OPCOMP/D-	XA	C8006MHD	CONN	51				CONN
52				CONN	53				CONN	54				CONN
55				CONN	56				CONN	57				CONN
58				CONN	59				CONN	60				CONN
61				CONN	62				CONN	63				CONN
64				CONN	65				CONN	66				CONN
67				CONN	68				CONN	69				CONN
70				CONN	71				CONN	72				CONN
73				CONN	74				CONN	75				CONN
76				CONN	77				CONN	78				CONN
79				CONN	80				CONN					CONN

LOCATION /905

CIRCUIT TYPE CB

BLOCK

1

GATE

1				CONN	2				CONN	3	RFOUT14-	X	C8005MHD	CONN
4	RFOUT09-	X	C8005MHD	CONN	5	RFOUT06-	X	C8005MHD	CONN	6	RFOUT04-	X	C8005MHD	CONN
7	RFOUT13-	X	C8005MHD	CONN	8	RFOUT11-	X	C8005MHD	CONN	9	RFOUT05-	X	C8005MHD	CONN
10	READY	X	C8005MHD	CONN	11	STATBUSY	X	C8005MHD	CONN	12	RFOUT12-	X	C8005MHD	CONN
13	RFOUT07-	X	C8005MHD	CONN	14	RFOUT08-	X	C8005MHD	CONN	15	RFOUT10-	X	C8005MHD	CONN
16	RFOUT15-	X	C8005MHD	CONN	17	LW3CK-	XA	C8005MHD	CONN	18	MRD00/MHD	XA	C8005MHD	CONN
19	MRD01/MHD	XA	C8005MHD	CONN	20	MRD02/MHD	XA	C8005MHD	CONN	21	MRD03/MHD	XA	C8005MHD	CONN
22	MRD04/MHD	XA	C8005MHD	CONN	23	MRD05/MHD	XA	C8005MHD	CONN	24	MRD06/MHD	XA	C8005MHD	CONN
25	MRD07/MHD	XA	C8005MHD	CONN	26	CRCLLR-	XA	C8005MHD	CONN	27	CRCK-	XA	C8005MHD	CONN
28	MWDCK-	XA	C8005MHD	CONN	29	MWD02/MHD	XA	C8005MHD	CONN	30	MWD01/MHD	XA	C8005MHD	CONN
31	MWD00/MHD	XA	C8005MHD	CONN	32	MWD03/MHD	XA	C8005MHD	CONN	33	CYLAD7	XA	C8005MHD	CONN
34	NXSESEL3	XA	C8005MHD	CONN	35	NXSESEL1	XA	C8005MHD	CONN	36	31/44SIGNAL			CONN
37	NXSESEL2	XA	C8005MHD	CONN	38	NXSESEL6	XA	C8005MHD	CONN	39	NXSESEL4	XA	C8005MHD	CONN
40	NXSESEL5	XA	C8005MHD	CONN	41	CYLAD3	XA	C8005MHD	CONN	42	CYLAD2	XA	C8005MHD	CONN
43	CYLAD1	XA	C8005MHD	CONN	44	CYLAD0	XA	C8005MHD	CONN	45	CYLINC/Q-X	XA	C8005MHD	CONN
46	CYLAD6	XA	C8005MHD	CONN	47	CYLAD5	XA	C8005MHD	CONN	48	CYLAD4	XA	C8005MHD	CONN
49	WLKOUT/Q	XA	C8005MHD	CONN	50	SW2	XA	C8005MHD	CONN	51	SH15	XA	C8005MHD	CONN
52	STATSEL-	XA	C8005MHD	CONN	53	MWSEL-	XA	C8005MHD	CONN	54	STAT05-	XA	C8005MHD	CONN
55	STAT04-	XA	C8005MHD	CONN	56	STAT07-	XA	C8005MHD	CONN	57	STAT06-	XA	C8005MHD	CONN
58	LAIL	XA	C8005MHD	CONN	59	STAT08-	XA	C8005MHD	CONN	60	STAT11-	XA	C8005MHD	CONN
61	STAT10-	XA	C8005MHD	CONN	62	STAT13-	XA	C8005MHD	CONN	63	STAT12-	XA	C8005MHD	CONN
64	STAT15-	XA	C8005MHD	CONN	65	STAT14-	XA	C8005MHD	CONN	66	WC=O/Q	XA	C8005MHD	CONN
67	SP1/Q-	XA	C8005MHD	CONN	68	TDCMSP/Q-X	XA	C8005MHD	CONN	69	READYMHD	XA	C8005MHD	CONN
70	SYNCLK	XA	C8005MHD	CONN	71	RDATA	XA	C8005MHD	CONN	72	CRC=O	XA	C8005MHD	CONN
73	LDSR-	XA	C8005MHD	CONN	74	MRSMD	XA	C8005MHD	CONN	75	BUSY/Q-	XA	C8005MHD	CONN
76	CYLADCRY		C8005MHD	CONN	77				CONN	78				CONN
79				CONN	80				CONN					CONN

LOCATION /906

CIRCUIT TYPE CB

BLOCK

1

GATE

1				CONN	2				CONN	3	INTEN-	X	C8004MHD	CONN
4	RFOUT06-	X	C8004MHD	CONN	5	RFOUT04-	X	C8004MHD	CONN	6	LIST4	X	C8004MHD	CONN
7	ZEROB	X	C8004MHD	CONN	8	RFOUT00-	X	C8004MHD	CONN	9	BTCLR-	X	C8004MHD	CONN
10	RFOUT05-	X	C8004MHD	CONN	11	RFOUT01-	X	C8004MHD	CONN	12	LIST2	X	C8004MHD	CONN
13	DEVREAD	X	C8004MHD	CONN	14	RFOUT03-	X	C8004MHD	CONN	15	MEMEN-	X	C8004MHD	CONN
16	RFOUT02-	X	C8004MHD	CONN	17	LW3CK-	XA	C8004MHD	CONN	18	SYCKMHD	XA	C8004MHD	CONN
19	PLR1	XA	C8004MHD	CONN	20	INDEXM	XA	C8004MHD	CONN	21	MRD00/MHD	XA	C8004MHD	CONN
22	MRD01/MHD	XA	C8004MHD	CONN	23	MRD02/MHD	XA	C8004MHD	CONN	24	MRD03/MHD	XA	C8004MHD	CONN
25	MRD04/MHD	XA	C8004MHD	CONN	26	MRD05/MHD	XA	C8004MHD	CONN	27	MRD06/MHD	XA	C8004MHD	CONN
28	MRD07/MHD	XA	C8004MHD	CONN	29	CHAIN	XA	C8004MHD	CONN	30	CHAIN-	XA	C8004MHD	CONN
31	COMM1-	XA	C8004MHD	CONN	32	COMM2	XA	C8004MHD	CONN	33	COMM3-	XA	C8004MHD	CONN
34	HDSWST-	XA	C8004MHD	CONN	35	MWD00/MHD	XA	C8004MHD	CONN	36	CYLAD7	XA	C8004MHD	CONN
37	NXSESEL3	XA	C8004MHD	CONN	38	NXSESEL1	XA	C8004MHD	CONN	39	31/44SIGNAL			CONN
40	NXSESEL2	XA	C8004MHD	CONN	41	NXSESEL6	XA	C8004MHD	CONN	42	NXSESEL4	XA	C8004MHD	CONN
43	NSBB-	XA	C8004MHD	CONN	44	NXSESEL5	XA	C8004MHD	CONN	45	NSCE	XA	C8004MHD	CONN
46	MPSMHD-	XA	C8004MHD	CONN	47	SYCKMHDJ	XA	C8004MHD	CONN	48	CYLINC/Q-X	XA	C8004MHD	CONN
49	WLKOUT/Q	XA	C8004MHD	CONN	50	SK2/Q-	XA	C8004MHD	CONN	51	SK2/K	XA	C8004MHD	CONN
52	SIGSTA/Q-	XA	C8004MHD	CONN	53	RDPFLG/J	XA	C8004MHD	CONN	54	UNSKFSFTFNXA			CONN
55	LAIL	XA	C8004MHD	CONN	56	SK2/J	XA	C8004MHD	CONN	57	WPTOPFLG/QXA			CONN
58	DPOMHD/Q	XA	C8004MHD	CONN	59	PROGER/DA-XA		C8004MHD	CONN	60	SIGSTAE/Q	XA	C8004MHD	CONN
61	SIGSTA1/Q	XA	C8004MHD	CONN	62	WRIDCOM	XA	C8004MHD	CONN	63	SYNCLK	XA	C8004MHD	CONN
64	LSMF/Q-	XA	C8004MHD	CONN	65	LSMF/Q	XA	C8004MHD	CONN	66	RIDCOM	XA	C8004MHD	CONN
67	MPSMHD	XA	C8004MHD	CONN	68	SKDPFLG/J	XA	C8004MHD	CONN	69	CRC=O	XA	C8004MHD	CONN
70	WLKTON/D-	XA	C8004MHD	CONN	71	IDREAD/J	XA	C8004MHD	CONN	72	CRC=O	XA	C8004MHD	CONN
73	PROGER/D-	XA	C8004MHD	CONN	74	SYCKMHD-	XA	C8004MHD	CONN	75	CYLADCRY		C8004MHD	CONN
76	COMPOP-	XA	C8004MHD	CONN	77				CONN	78				CONN
79				CONN	80				CONN					CONN

LOCATION /907

CIRCUIT TYPE CB

BLOCK

1

GATE

1				CONN	2				CONN	3				CONN
4	AT11	X	BTCCB1X	CONN	5	AT12	X	BTCCB1X	CONN	6	BTCLR-	X	BTCCB1X	CONN
7	BUSY-	X	BTCCB1X	CONN	8	CLOCK-		BTCCB1X	CONN	9	DATAV-		BTCCB1X	CONN
10	DATAVL	X	BTCCB1X	CONN	11	DD2/Q-	X	BTCCB1X	CONN	12	DEVADSFL0	X	BTCCB1X	CONN
13	DEVADSEL1	X	BTCCB1X	CONN	14	DEVADSEL2	X	BTCCB1X	CONN	15	DEVAT11-		BTCCB1X	CONN
16	DEVAT12-	X	BTCCB1X	CONN	17	DEVMRD00		BTCCB1X	CONN	18	DEVMRD01		BTCCB1X	CONN
19	DEVMRD02		BTCCB1X	CONN	20	DEVMRD03		BTCCB1X	CONN	21	DEVMRD04		BTCCB1X	CONN
22	DEVMRD05		BTCCB1X	CONN	23	DEVMRD06		BTCCB1X	CONN	24	DEVMRD07		BTCCB1X	CONN
25	DEVMRD08		BTCCB1X	CONN	26	DEVMRD09		BTCCB1X	CONN	27	DEVMRD10		BTCCB1X	CONN
28	DEVMRD11		BTCCB1X	CONN	29	DEVMRD12		BTCCB1X	CONN	30	DEVMRD13		BTCCB1X	CONN
31	DEVMRD14		BTCCB1X	CONN	32	DEVMRD15		BTCCB1X	CONN	33	DEVMRD16		BTCCB1X	CONN
34	DEVSELO-X		BTCCB1X	CONN	35	ENRFMR-	X	BTCCB1X	CONN	36	LC2/Q-	X	BTCCB1X	CONN
37	LC3+LCNT4	X	BTCCB1X	CONN	38	LIST4	X	BTCCB1X	CONN	39				CONN
40	MC5+MC7-	X	BTCCB1X	CONN	41	MRD08	X	BTCCB1X	CONN	42	MRD09	X	BTCCB1X	CONN
43	MRD10	X	BTCCB1X	CONN	44	MRD11	X	BTCCB1X	CONN	45	MRD12	X	BTCCB1X	CONN
46	PAPER	X	BTCCB1X	CONN	47	PARERR-		BTCCB1X	CONN	48	RESFT-		BTCCB1X	CONN
49	RESETA-	X	BTCCB1X	CONN	50	RFOUT00-	X	BTCCB1X	CONN	51	RFOUT01-	X	BTCCB1X	CONN
52	RFOUT02-	X	BTCCB1X	CONN	53	RFOUT03-	X	BTCCB1X	CONN	54	RFOUT04-	X	BTCCB1X	CONN
55	RFOUT05-	X	BTCCB1X	CONN	56	RFOUT06-	X	BTCCB1X	CONN	57	RFOUT07-	X	BTCCB1X	CONN
58	RFOUT08-	X	BTCCB1X	CONN	59	RFOUT09-	X	BTCCB1X	CONN	60	RFOUT10-	X	BTCCB1X	CONN
61	RFOUT11-	X	BTCCB1X	CONN	62	RFOUT12-	X	BTCCB1X	CONN	63	RFOUT13-	X	BTCCB1X	CONN
64	RFOUT14-	X	BTCCB1X	CONN	65	RFOUT15-	X	BTCCB1X	CONN	66	RFPACD1	X	BTCCB1X	CONN
67	SC5/Q-	X	BTCCB1X	CONN	68	RFWADD1	X	BTCCB1X	CONN	69	SCLOCK	X	BTCCB1X	CONN

70	SC4/Q-	X	BTCCB1X	CONN	71	STATEN-	X	BTCCB1X	CONN	72	CONN
73	SYCL-	X	BTCCB1X	CONN	74	MC2/Q	X	BTCCB1X	CONN	75	CONN
76	MREST	X	BTCCB1X	CONN	77				CONN	78	CONN
79				CONN	80				CONN		CONN

LOCATION /908				CIRCUIT TYPE CB				BLOCK	I	GATE				
1				CONN	2			3	AG	X	BTCCB2X	CONN		
4	CNTUP-	X	BTCCB2X	CONN	5	COUNT	X	BTCCB2X	CONN	6	MEMRD-	X	BTCCB2X	CONN
7	DEVADD,00		BTCCB2X	CONN	8	DEVADD,01		BTCCB2X	CONN	9	DEVADD,02		BTCCB2X	CONN
10	DEVADD,03		BTCCB2X	CONN	11	DEVADD,04		BTCCB2X	CONN	12	DEVADD,05		BTCCB2X	CONN
13	DEVADD,06		BTCCB2X	CONN	14	DEVADD,07		BTCCB2X	CONN	15	DEVADD,08		BTCCB2X	CONN
16	DEVADD,09		BTCCB2X	CONN	17	DEVADD,10		BTCCB2X	CONN	18	DEVADD,11		BTCCB2X	CONN
19	DEVADD,12		BTCCB2X	CONN	20	DEVADD,13		BTCCB2X	CONN	21	DEVADD,14		BTCCB2X	CONN
22	DEVADD,15		BTCCB2X	CONN	23	DEVADEL1	X	BTCCB2X	CONN	24	DEVADEL2	X	BTCCB2X	CONN
25	DEVFETCH-		BTCCB2X	CONN	26	DEVWMD,00		BTCCB2X	CONN	27	DEVWMD,01		BTCCB2X	CONN
28	DEVWMD,02		BTCCB2X	CONN	29	DEVWMD,03		BTCCB2X	CONN	30	DEVWMD,04		BTCCB2X	CONN
31	DEVWMD,05		BTCCB2X	CONN	32	DEVWMD,06		BTCCB2X	CONN	33	DEVWMD,07		BTCCB2X	CONN
34	DEVWMD,08		BTCCB2X	CONN	35	DEVWMD,09		BTCCB2X	CONN	36	DEVWMD,10		BTCCB2X	CONN
37	DEVWMD,11		BTCCB2X	CONN	38	DEVWMD,12		BTCCB2X	CONN	39	DEVWMD,13		BTCCB2X	CONN
40	DEVWMD,14		BTCCB2X	CONN	41	DEVWMD,15		BTCCB2X	CONN	42	DEVWMD,16		BTCCB2X	CONN
43	DEVSELO-	X	BTCCB2X	CONN	44	DEVSTORE-		BTCCB2X	CONN	45	LC2/Q-	X	BTCCB2X	CONN
46	LIST2	X	BTCCB2X	CONN	47	MCMP	X	BTCCB2X	CONN	48	MCQ-	X	BTCCB2X	CONN
49	MC5+MC7-	X	BTCCB2X	CONN	50	MEMREAD	X	BTCCB2X	CONN	51	RESETA-	X	BTCCB2X	CONN
52	RFOU00-	X	BTCCB2X	CONN	53	RFOU01-	X	BTCCB2X	CONN	54	RFOU02-	X	BTCCB2X	CONN
55	RFOU03-	X	BTCCB2X	CONN	56	RFOU04-	X	BTCCB2X	CONN	57	RFOU05-	X	BTCCB2X	CONN
58	RFOU06-	X	BTCCB2X	CONN	59	RFOU07-	X	BTCCB2X	CONN	60	RFOU08-	X	BTCCB2X	CONN
61	RFOU09-	X	BTCCB2X	CONN	62	RFOU10-	X	BTCCB2X	CONN	63	RFOU11-	X	BTCCB2X	CONN
64	RFOU12-	X	BTCCB2X	CONN	65	RFOU13-	X	BTCCB2X	CONN	66	RFOU14-	X	BTCCB2X	CONN
67	RFOU15-	X	BTCCB2X	CONN	68	SC4,5-	X	BTCCB2X	CONN	69	SC5/Q	X	BTCCB2X	CONN
70	DATEN-	X	BTCCB2X	CONN	71	STATRUSY	X	BTCCB2X	CONN	72	SYCL-	X	BTCCB2X	CONN
73	ZERO16	X	BTCCB2X	CONN	74	ZERO8	X	BTCCB2X	CONN	75	LC3+LCNT4	X	BTCCB2X	CONN
76	MC2/Q	X	BTCCB2X	CONN	77				CONN	78			CONN	
79				CONN	80				CONN			CONN		

LOCATION /910				CIRCUIT TYPE CB				BLOCK	I	GATE				
1				CONN	2			3	ACK-	X	BTCCB3X	CONN		
4	AG	X	BTCCB3X	CONN	5	AGDEV-		BTCCB3X	CONN	6	AGDEV-		BTCCB3X	CONN
7	AGDEV-		BTCCB3X	CONN	8	AGDEV-		BTCCB3X	CONN	9	AGDEV-		BTCCB3X	CONN
10	AGDEV-		BTCCB3X	CONN	11	AGDEV-		BTCCB3X	CONN	12	AGDEV-		BTCCB3X	CONN
13				CONN	14	ARDEV-		BTCCB3X	CONN	15	ARDEV-		BTCCB3X	CONN
16	ARDEV-		BTCCB3X	CONN	17	ARDEV-		BTCCB3X	CONN	18	ARDEV-		BTCCB3X	CONN
19	ARDEV-		BTCCB3X	CONN	20	ARDEV-		BTCCB3X	CONN	21	ARDEV-		BTCCB3X	CONN
22	CNTUP-	X	BTCCB3X	CONN	23	DATAVL	X	BTCCB3X	CONN	24				CONN
25	MC2/Q-	X	BTCCB3X	CONN	26	DECOUNT	X	BTCCB3X	CONN	27	DEVADEL0	X	BTCCB3X	CONN
28	DEVADEL1	X	BTCCB3X	CONN	29	DEVADEL2	X	BTCCB3X	CONN	30	DEVREAD	X	BTCCB3X	CONN
31	ENRFMR-	X	BTCCB3X	CONN	32	INTDEV-		BTCCB3X	CONN	33	INTDEV-		BTCCB3X	CONN
34	INTDEV-		BTCCB3X	CONN	35	INTDEV-		BTCCB3X	CONN	36	INTDEV-		BTCCB3X	CONN
37	INTDEV-		BTCCB3X	CONN	38	INTDEV-		BTCCB3X	CONN	39	INTDEV-		BTCCB3X	CONN
40	INTEN-	X	BTCCB3X	CONN	41	IREFCGDEV-		BTCCB3X	CONN	42	IREFCGDEV-		BTCCB3X	CONN
43	IREFCGDEV-		BTCCB3X	CONN	44	IREFCGDEV-		BTCCB3X	CONN	45	IREFCGDEV-		BTCCB3X	CONN
46	IREFCGDEV-		BTCCB3X	CONN	47	IREFCGDEV-		BTCCB3X	CONN	48	IREFCGDEV-		BTCCB3X	CONN
49	LC2/Q-	X	BTCCB3X	CONN	50	LC3+LCNT4	X	BTCCB3X	CONN	51	LISTEN-	X	BTCCB3X	CONN
52	LIST1	X	BTCCB3X	CONN	53	LIST2	X	BTCCB3X	CONN	54	LIST3	X	BTCCB3X	CONN
55	LIST4	X	BTCCB3X	CONN	56	MCMP	X	BTCCB3X	CONN	57	MCQ-	X	BTCCB3X	CONN
58	MEMEN-	X	BTCCB3X	CONN	59	MEMREAD	X	BTCCB3X	CONN	60	READY	X	BTCCB3X	CONN
61	RESETA-	X	BTCCB3X	CONN	62	RFRADD1	X	BTCCB3X	CONN	63	SC5/Q-	X	BTCCB3X	CONN
64	RFRADD1	X	BTCCB3X	CONN	65	RFR4EN	X	BTCCB3X	CONN	66	SC4/Q-	X	BTCCB3X	CONN
67	SC4,5-	X	BTCCB3X	CONN	68	SC5/Q	X	BTCCB3X	CONN	69	DATEN-	X	BTCCB3X	CONN
70	STATRUSY	X	BTCCB3X	CONN	71	STATEN-	X	BTCCB3X	CONN	72	SYCL-	X	BTCCB3X	CONN
73	TWOSC	X	BTCCB3X	CONN	74	AT12	X	BTCCB3X	CONN	75	MEMRD-	X	BTCCB3X	CONN
76				CONN	77				CONN	78			CONN	
79				CONN	80				CONN			CONN		

LOCATION /912				CIRCUIT TYPE CB				BLOCK	I	GATE				
1				CONN	2			3	DEVMPD01		BTCCB0X	CONN		
4	DEVMPD00		BTCCB0X	CONN	5	DEVMPD03		BTCCB0X	CONN	6	DEVMPD02		BTCCB0X	CONN
7	DEVMPD05		BTCCB0X	CONN	8	DEVMPD04		BTCCB0X	CONN	9	DEVMPD07		BTCCB0X	CONN
10	DEVMPD06		BTCCB0X	CONN	11	DEVMPD09		BTCCB0X	CONN	12	DEVMPD08		BTCCB0X	CONN
13	DEVMPD11		BTCCB0X	CONN	14	DEVMPD10		BTCCB0X	CONN	15	DEVMPD13		BTCCB0X	CONN
16	DEVMPD12		BTCCB0X	CONN	17	DEVMPD15		BTCCB0X	CONN	18	DEVMPD14		BTCCB0X	CONN
19	DEVMPD16		BTCCB0X	CONN	20				CONN	21	AGDEV-		BTCCB0X	CONN
22				CONN	23	DEVAT12-		BTCCB0X	CONN	24				CONN
25	DEVAT11-		BTCCB0X	CONN	26				CONN	27	DATAV-		BTCCB0X	CONN
28				CONN	29	IREFCGDEV-		BTCCB0X	CONN	30				CONN
31	RESETA-		BTCCB0X	CONN	32				CONN	33	CLCK-		BTCCB0X	CONN
34	DEVADD,00		BTCCB0X	CONN	35	DEVADD,01		BTCCB0X	CONN	36	DEVADD,02		BTCCB0X	CONN
37	DEVADD,03		BTCCB0X	CONN	38	DEVADD,04		BTCCB0X	CONN	39	DEVADD,05		BTCCB0X	CONN
40	DEVADD,06		BTCCB0X	CONN	41	DEVADD,07		BTCCB0X	CONN	42	DEVADD,08		BTCCB0X	CONN
43	DEVADD,09		BTCCB0X	CONN	44	DEVADD,11		BTCCB0X	CONN	45	DEVADD,10		BTCCB0X	CONN
46	DEVADD,12		BTCCB0X	CONN	47	DEVADD,13		BTCCB0X	CONN	48	DEVADD,14		BTCCB0X	CONN
49	DEVADD,15		BTCCB0X	CONN	50	DEVWMD,00		BTCCB0X	CONN	51	DEVWMD,01		BTCCB0X	CONN
52	DEVWMD,02		BTCCB0X	CONN	53	DEVWMD,03		BTCCB0X	CONN	54	DEVWMD,04		BTCCB0X	CONN
55	DEVWMD,05		BTCCB0X	CONN	56	DEVWMD,06		BTCCB0X	CONN	57	DEVWMD,07		BTCCB0X	CONN
58	DEVWMD,08		BTCCB0X	CONN	59	DEVWMD,09		BTCCB0X	CONN	60	DEVWMD,10		BTCCB0X	CONN
61	DEVWMD,11		BTCCB0X	CONN	62	DEVWMD,12		BTCCB0X	CONN	63	DEVWMD,13		BTCCB0X	CONN
64	DEVWMD,14		BTCCB0X	CONN	65	DEVWMD,15		BTCCB0X	CONN	66	DEVWMD,16		BTCCB0X	CONN
67	ARDEV-		BTCCB0X	CONN	68	MREST		BTCCB0X	CONN	69	DEVSTORE-		BTCCB0X	CONN
70				CONN	71	INTDEV-		BTCCB0X	CONN	72				CONN
73	DEVFETCH-		BTCCB0X	CONN	74				CONN	75	PARFR-		BTCCB0X	CONN
76				CONN	77				CONN	78				CONN
79				CONN	80				CONN				CONN	

**SECTION VI****DRAWINGS**

This section includes drawings that are pertinent to maintenance of the Moving Head Disc Controller (Disc Control Logic) as follows:

Title	Drawing Number	Page Number
MHD No. 1 Assembly	973721	6-3
MHD No. 1 Logic	973722	6-9
MHD No. 2 Assembly	973678	6-21
MHD No. 2 Logic	973679	6-27
MHD No. 3 Assembly	961630	6-37
MHD No. 3 Logic	973755	6-41
MHD No. 4 Assembly	973683	6-55
MHD No. 4 Logic	973684	6-61
MHD No. 5 Assembly	973788	6-69
MHD No. 5 Logic	973786	6-73
MHD No. 6 Assembly	973784	6-81
MHD No. 6 Logic	973782	6-85
Cable Assembly, Disc Controller	973690	6-89
Wire List	973691	6-92
Cable Assembly, Daisy Chain	973675	6-95
Wire List	973787	6-99



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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	0001.000	EA		0217862-0002	LOGIC BOARD-SINGLE ENDED WIRE WRAP		
0002	REF	CA		0973695-9911	WIRE DECK, MHD MODEL 44		
0003	0003.000	EA		022222-7400	NETWORK SN7400N	-SN7400N	
0003A					C0 C1 C2 C3 C4 C5 C6 B6		
0004	0004.000	EA		022222-7402	NETWORK SN7402N	TI- -SN7402N	
0004A					D0 D1		
0005	0005.000	EA		022222-7404	NETWORK SN7404N		
0005A					D2 D3 D4		
0006	0006.000	EA		022222-7408	NETWORK-SN7408N		
0006A					E0 E1 D5 D6		
0007	0007.000	EA		022222-7410	NETWORK SN7410N	-SN7410N	
0007A					F0 E2 F3 E4 F5		
0008	0008.000	EA		022222-7420	NETWORK SN7420N	-SN7420N	
0008A					F1 E2 F3		
0009	0009.000	EA		022222-7437	NETWORK SN7437N		
0009A					F4		
0010	0010.000	EA		022222-7451	NETWORK SN7451N	-SN7451N	
0010A					F5		
0011	0011.000	EA		022222-7474	NETWORK SN7474N	-SN7474N	
0011A					H0 H1 H2 H3		
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
			<i>J. Ross</i>	5-11-77			MHD, NO. 1, MODEL 44
APPD.-MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
							8100
						PART NUMBER	REV
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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF MEASURE	DMO. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0012	00002.000	EA		0222222-7123	NETWORK SN74123N		
0012A					J2 J3		
0013	00001.000	EA		0222222-7161	NETWORK SN74161N	-SN74161N	
0013A					J4		
0014	00002.000	EA		0222222-7175	NETWORK SN74175N		
0014A					J5 H4		
0015	00001.000	EA		0240000-7106	NETWORK SN74H106N		
0015A					J1		
0016	00009.000	EA		0240000-7108	NETWORK SN74H108N		
0016A					R0 R1 R2 A1 A2 A3 A4 A5 A6		
0017	00002.000	EA		0240000-7411	NETWORK-SN74H11N		
0017A					R3 R4 R5		
0018	00001.000	EA		0222222-7496	NETWORK-SN7486N		
0018A					A0		
0019	00002.000	EA		0972975-0065	RES FIX COMP 4.7 K OHMS 5% 1/8 WATT	QPL - RC05G472JS	
0019A					R1 R2		
0020	00001.000	EA		0539370-0473	RES FIX FILM 8.25K OHM 1% .25 WATT	QOR - NA55	
0020A					R3		
0021	00012.000	EA		0230590-9000	CAP .05 MF 12 V 20% CER TRANSCAP	ERI -5635-000-Y5FC5	
0021A					C6 THRU C17		
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MHD, N.O. 1, MODEL 44
APPD-MFG		DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
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PART NUMBER REV
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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0022	0002.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 15 * 15 VOL	QPL -M3903/1-2271	
0023	0002.000	EA		0972926-0016	CAP FIX MICA 500V 36.0 PF 5 *	QPL -CM045260JJD	
0024	0001.000	EA		0058023-0008	CAP FIX .010 MFD 5 * 100V MYLAR FOIL	TRW - 663UW	
0025	0001.000	EA		0972932-0001	DIODE, 1N914P SWITCHING 75V PIV 75MA 4NS	TI - IN914B	
0026	AP	FT		0535978-0058	WIRE ELEC., SOLID, "KYNAR" INSUL #30 AWG		
0027	REF	EA		0973722-9901	LOGIC DIAGRAM, MHD, NO. 1, MODEL 44		
0028	REF	EA		0973722-9901	TEST PROCEDURE, MHD, NO. 1, MODEL 44		
0029	AP	FT		0410499-0006	INSULATION SLEEVING, TEFLON #22 NATURAL	QPL -81349	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MHD, NO. 1, MODEL 44
APPD. MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM0973721-0001	H

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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0013	00001.000	EA		0222222-7161	J2 J3 NETWORK SN74161N	-SN74161N	
0014	00002.000	EA		0222222-7175	J4 NETWORK SN74175N		
0015	00001.000	EA		0240000-7106	J5 H4 NETWORK SN74H106N		
0016	00009.000	EA		0240000-7108	J1 NETWORK SN74H108N		
0017	00002.000	EA		0240000-7411	R0 R1 R2 A1 A2 A3 A4 A5 A6 NETWORK-SN74H11N		
0018	00001.000	EA		0222222-7486	R3 R4 R5 NETWORK-SN7486N		
0019	00002.000	EA		0972975-0065	A0 RES FIX COMP 4.7 K OHMS 5% 1/8 WATT	QPL - RC05C472JS	
0020	00001.000	EA		0539370-0473	F1 R2 RES FIX FILM 0.25K OHM 1% .25 WATT	QPL - MA55	
0021	00012.000	EA		0230590-0000	F3 CAP .05 MF 12 V 20% 3 CER TRANSCAP	ERI -5635-000-Y5FC5	
0022	00002.000	EA		0972924-0010	C6 THRU C17 CAP FIX TANT SOLID 22 MFD 10% 15 VOLT	QPL -M39003/1-2271	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MHD, NO.1, MODEL 44
APPD.-MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
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PART ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF MEAS	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0023					C4 C5		
0023	00002.000	FA		0972926-0016	CAP FIX MICA 500V 36.0 PF 5 %	QPL -CM04E360J00	
0023A					C1 C2		
0024	00001.000	FA		005P023-0008	CAP FIX .010 MFD 5 % 100V MYLAR FOIL	TRW - 6630W	
0024A					C3		
0025	00001.000	FA		0972932-0001	DIODE,IN914P SWITCHING 75V PIV 75MA 4NS	TI - IN914B	
0026	AF	FT		0535278-0058	WIRE ELEC.,SOLID,"KYNAR" INSUL #30 AWG		
0027	REF	FA		0973722-9901	LOGIC DIAGRAM,MHD,NO.1,MODEL 44		
0028	REF	FA		0973723-9901	TEST PROCEDURE,MHD,NO.1,MODEL 44		
0029	AF	FT		0410499-0006	INSULATION SLEEVING,TEFLON #22 NATURAL	QPL -81349	
0030	00001.000	FA		0539544-0002	SOCKET,16PIN IC LOW PROFILE SOLDER TAIL	TI -C93-16-02	
0030A					XJ3		
DRAFTSMAN		DATE	CDR DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MHD, NO.1, MODEL 44
APPRO. MFG.		DATE	APPRO. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						PART NUMBER	REV
						LM0973721-0002	H

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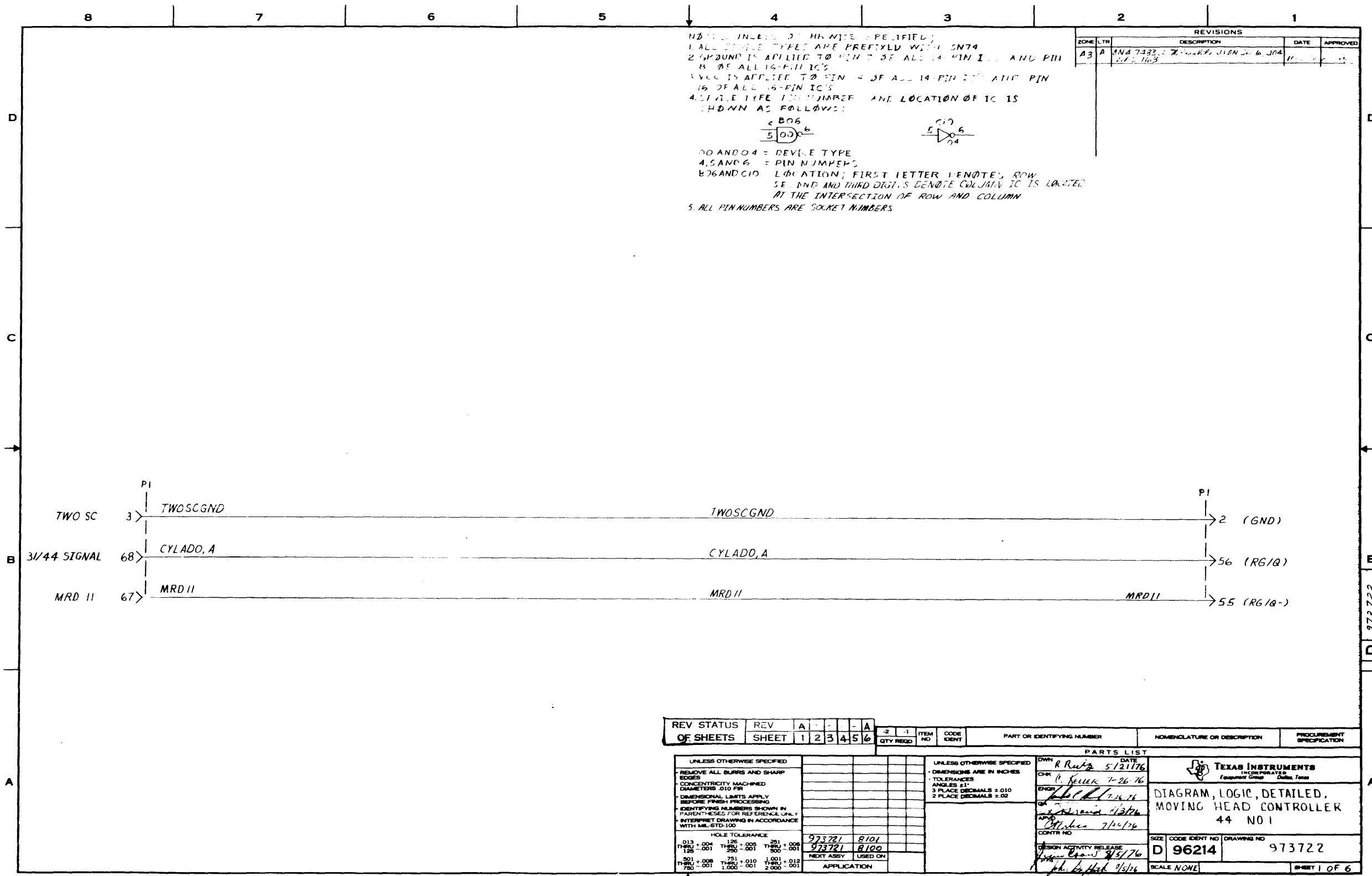
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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	00001.000	EA		0944040-0001	MWB, MOVING HEAD DISC 44 CONTROLLER NO 1		
0002	00008.000	FA		0222222-7400	NETWORK SN7400N	-SN7400N	
0003A					C0 C1 C2 C3 C4 C5 C6 R6		
0004	00002.000	FA		0222222-7402	NETWORK SN7402N	TI- -SN7402N	
0004A					D0 D1		
0005	00003.000	FA		0222222-7404	NETWORK SN7404N		
0005A					D2 D3 D4		
0006	00004.000	EA		0222222-7408	NETWORK-SN7408N		
0006A					F0 F1 D5 D6		
0007	00005.000	FA		0222222-7410	NETWORK SN7410N	-SN7410N	
0007A					F0 F2 F3 F4 F5		
0008	00007.000	FA		0222222-7420	NETWORK SN7420N	-SN7420N	
0008A					F1 F2 F3		
0009	00001.000	FA		0222222-7437	NETWORK SN7437N		
0009A					F4		
0010	00001.000	FA		0222222-7451	NETWORK SN7451N	-SN7451N	
0010A					F5		
0011	00004.000	FA		0222222-7474	NETWORK SN7474N	-SN7474N	
0011A					H0 H1 H2 H3		
0012	00002.000	FA		0222222-7123	NETWORK SN74123N		
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MHD, NO.1, MODEL 44
APPD-MFG		DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0973721-0002	REV H





REV STATUS		REV	A	-	-	-	A	-2		-1	ITEM	CODE	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
OF SHEETS		SHEET	1	2	3	4	5	6	QTY	REQD	NO	IDENT			

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

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REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
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				APPLICATION		

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

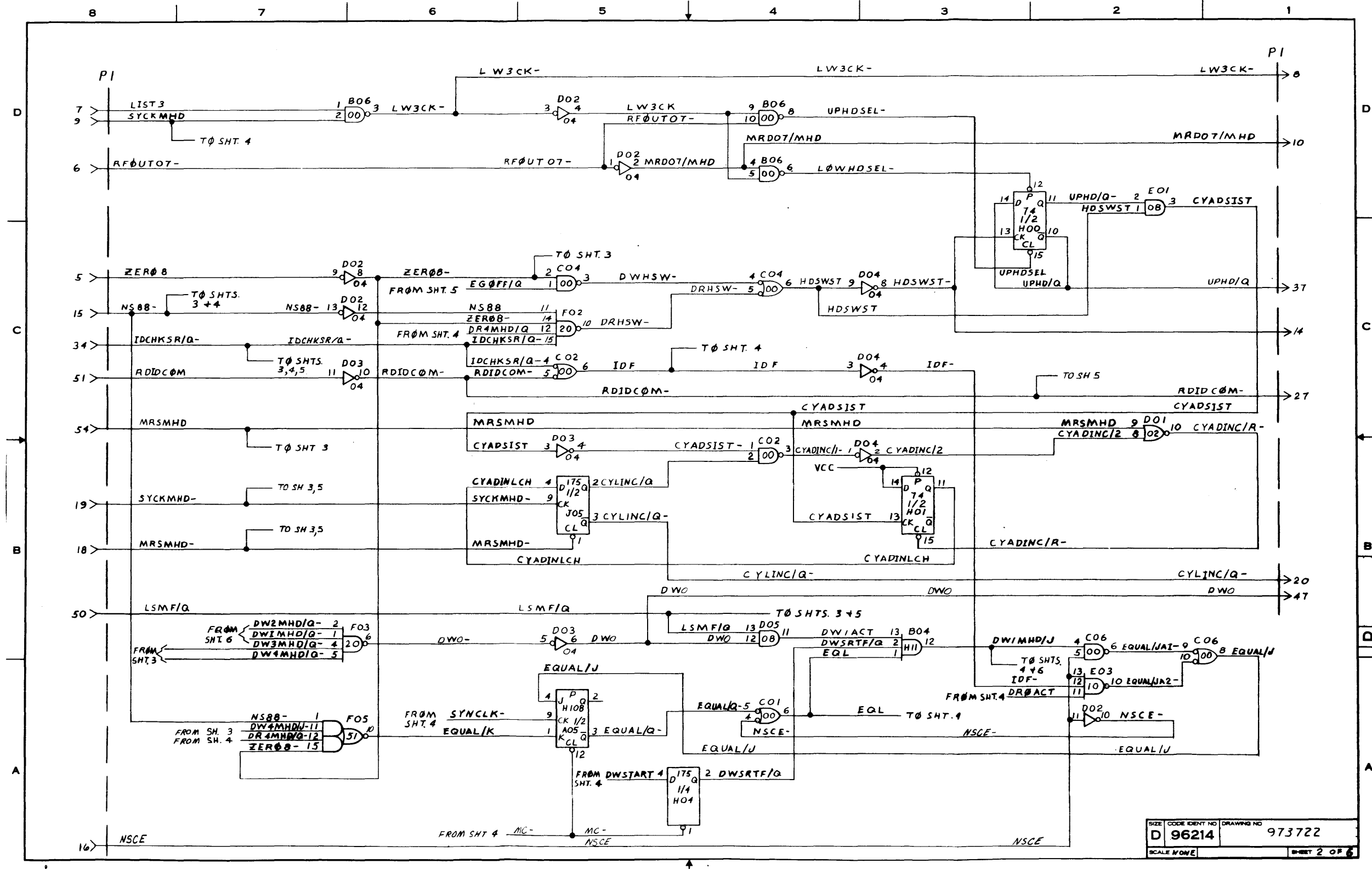
UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
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001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

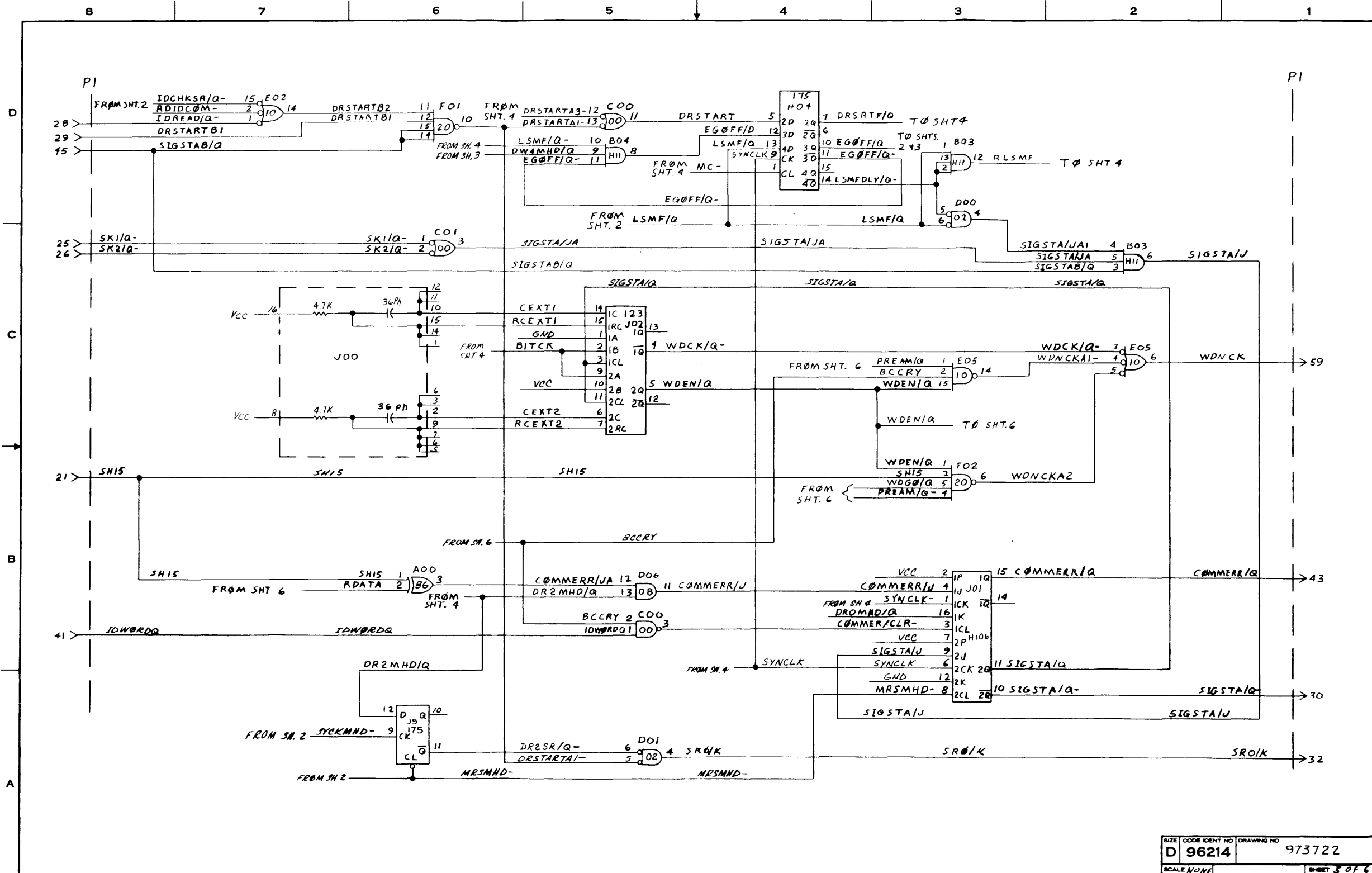
UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

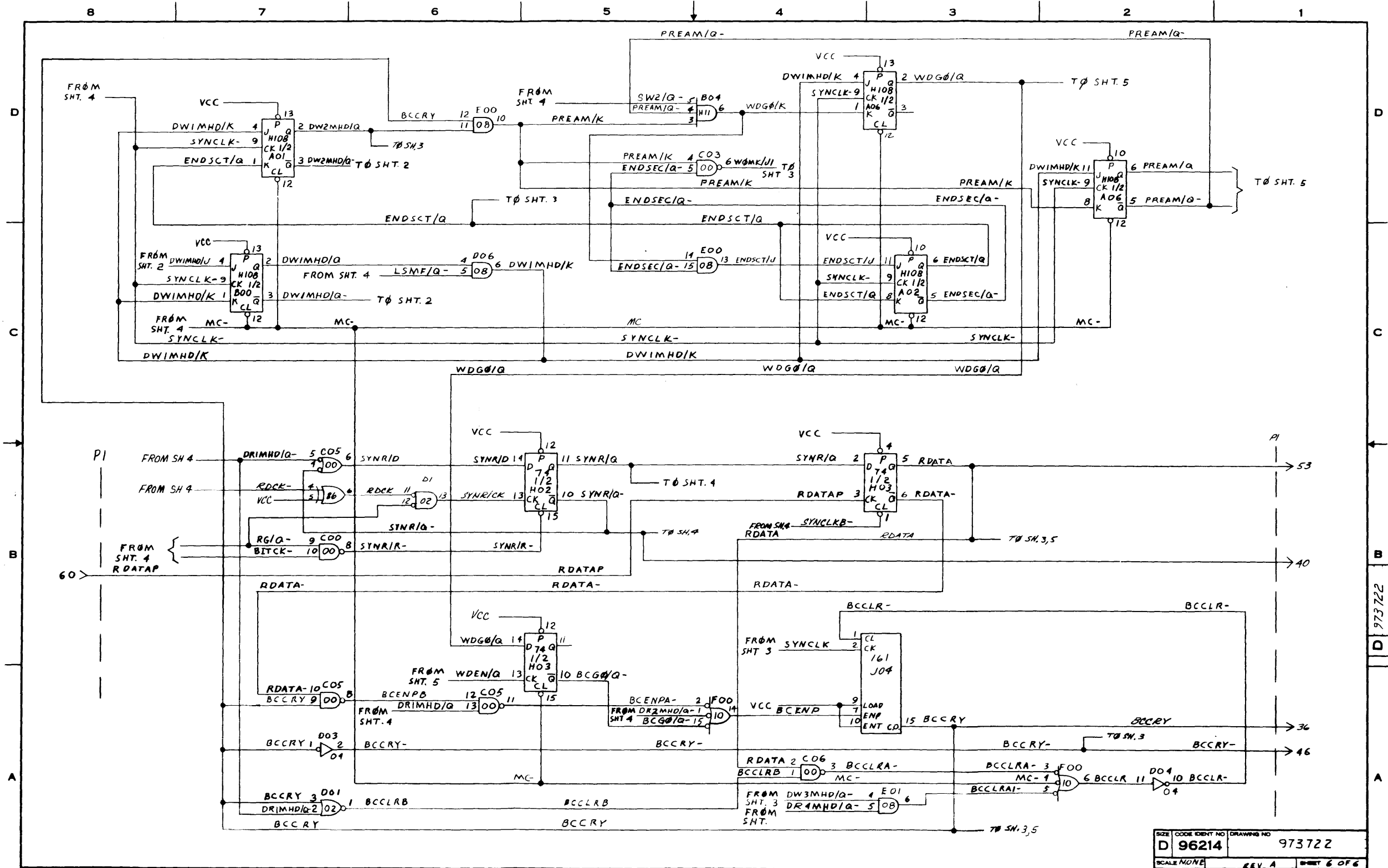
UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
REMOVE ALL BURRS AND SHARP EDGES	CONCENTRICITY MACHINED DIAMETERS .010 FIR	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	HOLE TOLERANCE	973721 8101
013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
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UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED		PARTS LIST		
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013 +.004	126 +.005	251 +.008	THRU -.001	THRU -.001	THRU -.001	973721 8100
001	751	1.001	THRU +.008	THRU +.010	THRU +.012	
THRU -.001	1.000	-.001	THRU -.001	THRU -.001	2.000	
				APPLICATION		

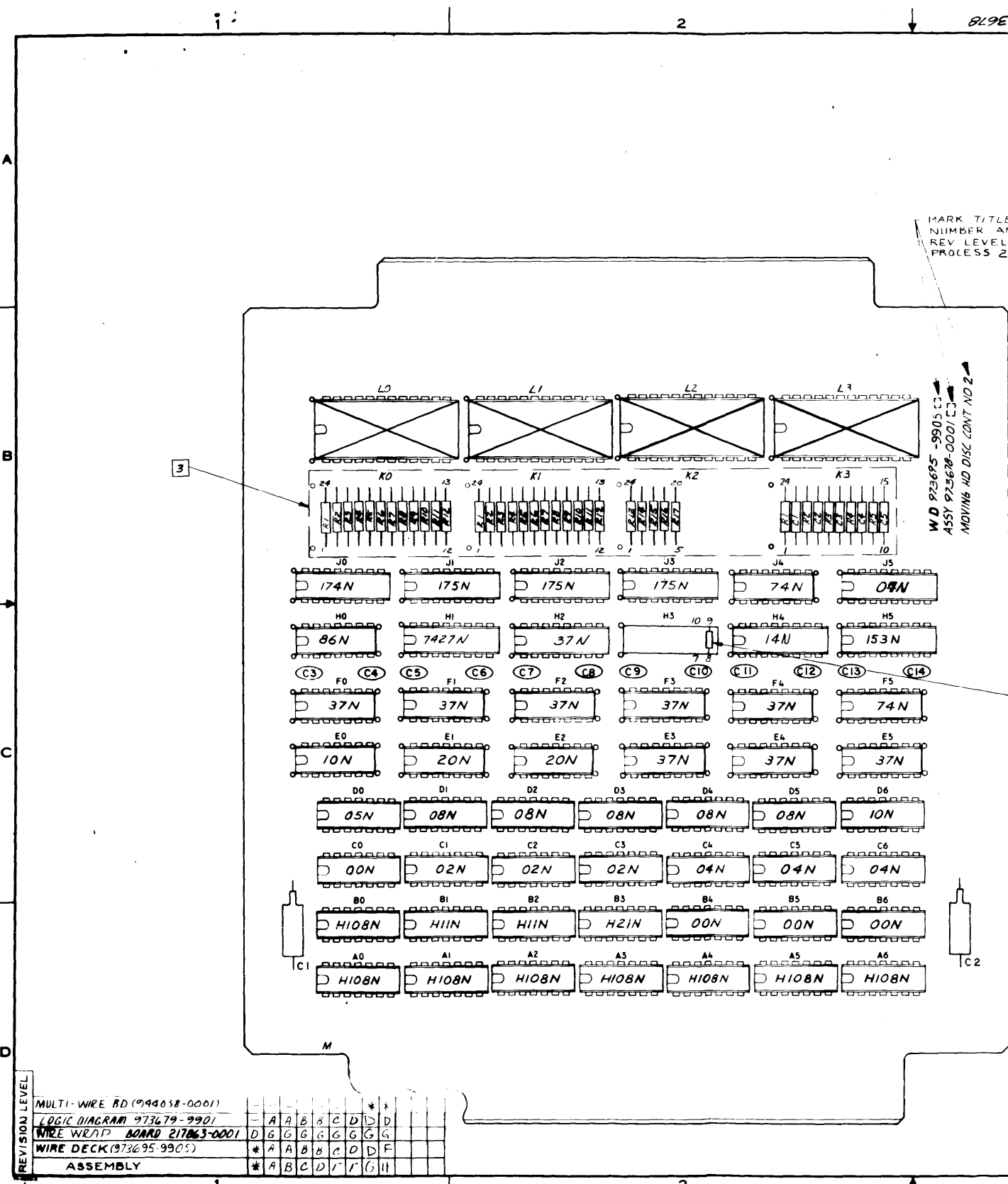


SIZE	CODE IDENT NO	DRAWING NO
D	96214	973722
SCALE	NOV E	SHEET 2 OF 6





SIZE	CODE IDENT NO	DRAWING NO
D	96214	973722
SCALE NONE	REV A	SHEET 6 OF 6



NOTES: UNLESS OTHERWISE SPECIFIED
 1. NETWORKS ARE SN74 SERIES
 2. CLAMP LEADS OF CAPACITORS TO WIRE DECK PRIOR TO WIRE WRAP AND PROCESS 1
 3. HAND SOLDER COMPONENTS PER PROCESS 1
 4. INSTALL JUMPER PLUG (ITEM 31) BETWEEN PINS 8 AND 9 OF H3 WITH THE JUMPER INSTALLED IN THIS POSITION. MRD11=0 SELECTS THE FIXED DISC. FOR MRD10 TO SELECT THE REMOVABLE DISC. INSTALL THE JUMPER BETWEEN PINS 7 AND 10 OF H3

REV	DESCRIPTION	DATE	BY
A	CN41152 (1) R. Bann (1) ADDED LARG DIAG TO REV LEVEL BLOCK, WIRE DECK WAS -9906 IN REV LEVEL BLOCK & ON FD (2) ON LM PAU OF ITEM 2 WMS -9906 (3) UPDATED REV LEVEL BLOCK	11/3/75	R. Bann
B	CN409331 (1) S. Damm (1) UPDATED REV LEVEL (2) DELETED NOTE 2	11/10/75	R. Bann
C	CN407266 (1) R. Bann (1) REVISED PER EXTENSIVE ENGR CHANGES (2) UPDATED REV LEVEL BLOCK	7/23/76	R. Bann
D	CN407237 (1) R. Bann (1) ADDED ITEM 31 TO LM & FID (2) ADDED NOTE 4 (3) UPDATED REV LEVEL BLOCK	9/4/76	R. Bann
E	CN406765 (1) D. L. (1) ADDED ITEM 32 (2) QTY OF ITEM 27 WAS 64 DELETED REF TO K3 R1 THRU K3 R5 (3) RELOCATED RESISTOR AT LOCATION H3 WAS AT PIN 7 TO 10 (4) REVISED NOTE 4 (5) UPDATED REV LEVEL BLOCK	5/19/76	R. Bann
F	CN406890 (1) D. L. (1) UPDATED REV LEVEL BLOCK	9/11/76	R. Bann
G	CN412182 (1) D. L. (1) ADDED -2 LM AND REVISED REV STATUS BLOCK	8/26/76	R. Bann
H	CN414996 (1) R. Bann (1) UPDATED REV LEVEL BLOCK	8/26/76	R. Bann

QTY	PART NO	DESCRIPTION
1	973678-0002	MOVING HEAD DISC 44 CONTROLLER NO 2 M/W
1	973678-0001	MOVING HEAD DISC 44 CONTROLLER NO 2 W/W

REVISION LEVEL	DESCRIPTION	A	B	C	D	E	F	G	H	I	J	K	L	M
1	MULTI-WIRE BD (994038-0001)													
2	LOGIC DIAGRAM 973679-9901	*	A	B	C	D								
3	WIRE WRAP BOARD 217063-0001	D	G	G	G	G	G	G						
4	WIRE DECK (973695-9905)	*	A	B	B	C	D							
5	ASSEMBLY	*	A	B	C	D	F	G	H					

UNLESS OTHERWISE SPECIFIED	PROCESS	QTY	PART NO	DESCRIPTION	REV	DATE	BY
DECIMAL ANGLES 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0, 15.0, 30.0, 45.0, 60.0, 75.0, 90.0, 120.0, 150.0, 180.0, 225.0, 270.0, 315.0, 360.0 FRACTIONS 1/16, 1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8, 1, 1 1/8, 1 1/4, 1 3/8, 1 1/2, 1 5/8, 1 3/4, 1 7/8, 2, 2 1/8, 2 1/4, 2 3/8, 2 1/2, 2 5/8, 2 3/4, 2 7/8, 3, 3 1/8, 3 1/4, 3 3/8, 3 1/2, 3 5/8, 3 3/4, 3 7/8, 4, 4 1/8, 4 1/4, 4 3/8, 4 1/2, 4 5/8, 4 3/4, 4 7/8, 5, 5 1/8, 5 1/4, 5 3/8, 5 1/2, 5 5/8, 5 3/4, 5 7/8, 6, 6 1/8, 6 1/4, 6 3/8, 6 1/2, 6 5/8, 6 3/4, 6 7/8, 7, 7 1/8, 7 1/4, 7 3/8, 7 1/2, 7 5/8, 7 3/4, 7 7/8, 8, 8 1/8, 8 1/4, 8 3/8, 8 1/2, 8 5/8, 8 3/4, 8 7/8, 9, 9 1/8, 9 1/4, 9 3/8, 9 1/2, 9 5/8, 9 3/4, 9 7/8, 10, 10 1/8, 10 1/4, 10 3/8, 10 1/2, 10 5/8, 10 3/4, 10 7/8, 11, 11 1/8, 11 1/4, 11 3/8, 11 1/2, 11 5/8, 11 3/4, 11 7/8, 12, 12 1/8, 12 1/4, 12 3/8, 12 1/2, 12 5/8, 12 3/4, 12 7/8, 13, 13 1/8, 13 1/4, 13 3/8, 13 1/2, 13 5/8, 13 3/4, 13 7/8, 14, 14 1/8, 14 1/4, 14 3/8, 14 1/2, 14 5/8, 14 3/4, 14 7/8, 15, 15 1/8, 15 1/4, 15 3/8, 15 1/2, 15 5/8, 15 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1/4, 143 3/8, 143 1/2, 143 5/8, 143 3/4, 143 7/8, 144, 144 1/8, 144 1/4, 144 3/8, 144 1/2, 144 5/8, 144 3/4, 144 7/8, 145, 145 1/8, 145 1/4, 145 3/8, 145 1/2, 145 5/8, 145 3/4, 145 7/8, 146, 146 1/8, 146 1/4, 146 3/8, 146 1/2, 146 5/8, 146 3/4, 146 7/8, 147, 147 1/8, 147 1/4, 147 3/8, 147 1/2, 147 5/8, 147 3/4, 147 7/8, 148, 148 1/8, 148 1/4, 148 3/8, 148 1/2, 148 5/8, 148 3/4, 148 7/8, 149, 149 1/8, 149 1/4, 149 3/8, 149 1/2, 149 5/8, 149 3/4, 149 7/8, 150, 150 1/8, 150 1/4, 150 3/8, 150 1/2, 150 5/8, 150 3/4, 150 7/8, 151, 151 1/8, 151 1/4, 151 3/8, 151 1/2, 151 5/8, 151 3/4, 151 7/8, 152, 152 1/8, 152 1/4, 152 3/8, 152 1/2, 152 5/8, 152 3/4, 152 7/8, 153, 153 1/8, 153 1/4, 153 3/8, 153 1/2, 153 5/8, 153 3/4, 153 7/8, 154, 154 1/8, 154 1/4, 154 3/8, 154 1/2, 154 5/8, 154 3/4, 154 7/8, 155, 155 1/8, 155 1/4, 155 3/8, 155 1/2, 155 5/8, 155 3/4, 155 7/8, 156, 156 1/8, 156 1/4, 156 3/8, 156 1/2, 156 5/8, 156 3/4, 156 7/8, 157, 157 1/8, 157 1/4, 157 3/8, 157 1/2, 157 5/8, 157 3/4, 157 7/8, 158, 158 1/8, 158 1/4, 158 3/8, 158 1/2, 158 5/8, 158 3/4, 158 7/8, 159, 159 1/8, 159 1/4, 159 3/8, 159 1/2, 159 5/8, 159 3/4, 159 7/8, 160, 160 1/8, 160 1/4, 160 3/8, 160 1/2,							



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INCORPORATED

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PART NUMBER
LM 973678-0001 REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	FA		217863-0001	LOGIC BCARC-CBL ENDED WIRE WRAP	
0002	RFF	FA		973655-5905	WIRE DFCR, MHD MODEL 44	
0003	00004.000	FA		222222-7400	NETWRK SN7400N	-SN7400N
0003A					CO B4 B5 E6	
0004	00003.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N
0004A					C1 C2 C3	
0005	00003.000	EA		222222-7404	NETWORK SN7404N	
0005A					C4 C5 C6	
0006	00001.000	FA		222222-7405	NETWRK SN7405N	
0006A					D0	
0007	00005.000	EA		222222-7408	NETWORK-SN7408N	
0007A					C1 C2 D3 C4 D5	
0008	00002.000	FA		222222-7410	NETWRK SN7410N	-SN7410N
0008A					E0 C6	
0009	00002.000	EA		222222-7420	NETWORK SN7420N	-SN7420N
0009A					E1 E2	
0010	00009.000	EA		222222-7437	NETWRK SN7437N	
0010A					F0 F1 F2 F3 F4 E3 F4 E5	
0010B					H2	
0011	00002.000	EA		222222-7474	NETWORK SN7474N	-SN7474N

DRAFTSMAN DATE *CD* DRAFTSMAN DATE *8/25/76* DESIGN ENGINEER DATE TITLE MOVING HEAD DISC 44 CONTROLLER NO.2
 APPD MFG DATE APPD PROJECT ENGINEER DATE RELEASED DATE PROJECT NO PART NUMBER LM 973678-0001 REV H

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PART NUMBER
LM 973678-0001 REV H

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011A					J4 F5	
0012	00001.000	FA		222222-7486	NETWRK-SN7486N	
0012A					H0	
0013	00001.000	EA		222222-7153	NETWRK SN74153N	-SN74153N
0013A					H5	
0014	00001.000	EA		222222-7174	NETWRK SN74174N	
0014A					J0	
0015	00003.000	FA		222222-7175	NETWRK SN74175N	
0015A					J1 J2 J3	
0016	00002.000	FA		240000-7411	NETWRK-SN7411N	
0016A					B1 P2	
0017	00001.000	FA		240000-7421	NETWRK-SN7421N	
0017A					B3	
0018	00008.000	EA		240000-7108	NETWRK SN74108N	
0018A					B0 A0 A1 A2 A3 A4 A5 A6	
0019	00012.000	FA		230590-9000	CAP .05 MF 12 V 20. X CEP TRANSCAP	FRI-5635-000-Y5F0503M
0019A					C3 THRU C14	
0020	00002.000	FA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 X 15 VOLT	OPL-M39003/1-2271
0020A					C1 C2	
0021	AR	FT		535578-0058	WIRE FLFC., SOLID, "KYNAR" INSUL #30 AWG	

DRAFTSMAN DATE *CD* DRAFTSMAN DATE *8/25/76* DESIGN ENGINEER DATE TITLE MOVING HEAD DISC 44 CONTROLLER N1.2
 APPD MFG DATE APPD PROJECT ENGINEER DATE RELEASED DATE PROJECT NO PART NUMBER LM 973678-0001 REV H

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TEXAS INSTRUMENTS INCORPORATED		DATE 08/24/76		LIST OF MATERIAL		PAGE 3 of		LM 973678-0001		REV. H	
PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER					
0023	500	EA		973678-5901	DIAGRAM, MIP 44 N7.2						
0024	32001.000	EA		222222-7427	NETWORK SN7427A	TI--SN7427A					
0024A					H1						
0025	00014.000	EA		972946-0043	RES FIX 120 OHM 5 % .25 W CARBON FILM	R0H- P-25					
0025A					K0P2 K0F4 K0F6 K0R9 K2R10						
0025B					K0P12 K1P2 K1P4 K1R6 K1P8						
0025C					K1R10 K1P12 K2P14 K2R15						
0026	33311.000	EA		972946-0052	RES FIX 300 OHM 5 % .25 W CARBON FILM	R0H- P-25					
0026A					K0P1 K0P3 K0P5 K0R7 K0R9						
0026B					K0R11 K1P1 K1P3 K1R5 K1P7						
0026C					K1R5 K1P11 K2P13 K2P15						
0027	33301.000	EA		972946-0065	RES FIX 1.0K OHM 5 % .25 W CARBON FILM	R0H- P-25					
0027A					K2P17						
0028	00001.000	EA		972909-0397	CAP FIX CERAMIC .001 JF 10% 200V	OPL-M39014/01-1397					
0028A					K3C1 THRU K3C5						
0029	30001.000	EA		222222-7414	NETWORK SN7414N						
0029A					H4						
0030	30001.000	EA		222222-74C7	NETWORK-SA74C7N	TI--SN74C7N					
0030A					J5						
DRAFTSMAN		DATE	CED DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE				
APPC MFG		DATE	APPC PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO				
							LM 973678-0001				
							REV. H				

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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER					
0031	00001.000	EA		972713-C001	PLUG, JUMPER, I.C., 0.300 INCH						
0031A					H3						
0032	00005.000	EA		972946-C062	RES FIX 5.1K OHM 5 % .25 W CARBON FILM	R0H- P-25					
0032A					K3R1 THRU K3R5						
DRAFTSMAN		DATE	CED DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE				
APPC MFG		DATE	APPC PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO				
							LM 973678-0001				
							REV. H				



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LM PART NUMBER 973678-0002 REV H

ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER			
0001	03001.000	EA		944038-0001	MWR, MOVING HEAD DISC 44 CONTROLLER NO 2				
0003	33004.330	EA		222222-7400	NETWORK SN7400N	-SN7400N			
0003A					C0 B4 B5 B6				
0004	00003.000	EA		222222-7402	NETWORK SA7402N	T1--SN7402N			
0004A					C1 C2 C3				
0005	33003.000	EA		222222-7404	NETWORK SA7404N				
0005A					C4 C5 C6				
0006	33001.330	EA		222222-7405	NETWORK SA7405N				
0006A					D0				
0007	33005.000	EA		222222-7408	NETWORK-SN7408N				
0007A					D1 D2 D3 D4 D5				
0008	33002.000	EA		222222-7410	NETWORK SA7410N	-SN7410N			
0008A					E0 E6				
0009	33002.000	EA		222222-7420	NETWORK SN7420N	-SN7420N			
0009A					E1 F2				
0010	00009.000	EA		222222-7437	NETWORK SN7437N				
0010A					F0 F1 F2 F3 F4 E3 E4 E5 H2				
0011	00002.000	EA		222222-7474	NETWORK SN7474N	-SN7474N			
0011A					J4 F5				
0012	00001.000	EA		222222-7486	NETWORK-SN7486N				
DRAFTSMAN		DATE	CEO DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	MOVING HEAD DISC 44 CONTROLLER NO.2	
APPRO. MFG		DATE	APPRO. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO	LM	PART NUMBER 973678-0002 REV H

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LM PART NUMBER 973678-0002 REV H

ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER			
0012A					H0				
0013	00001.000	EA		222222-7153	NETWORK SN74153N	-SN74153N			
0013A					H5				
0014	00001.000	EA		222222-7174	NETWORK SN74174N				
0014A					J0				
0015	00003.000	EA		222222-7175	NETWORK SA74175N				
0015A					J1 J2 J3				
0016	00002.000	EA		240000-7411	NETWORK-SN74H11N				
0016A					B1 B2				
0017	30001.000	EA		240000-7421	NETWORK-SN74H21N				
0017A					B3				
0018	00008.000	EA		240000-7108	NETWORK SA74H108N				
0018A					B0 A0 A1 A2 A3 A4 A5 A6				
0019	03012.000	EA		230590-9000	CAP .05 MF 12 V 20. % CEP TRANSCAP	E21-5635-000-Y5F0503M			
0019A					C3 THRU C14				
0020	33002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	OPL-M39003/1-2271			
0020A					C1 C2				
0021	AR	FT		535578-0058	WIRE ELEC., SOLID, "KYNAR" INSUL #30 AWG				
0022	RFF	EA		973679-9901	DIACRAM, MFD 44 NO 2				
0022A	RFF	EA		973680-9901	UNIT TEST PROC, MFD 44 NO 2				
DRAFTSMAN		DATE	CEO DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	MOVING HEAD DISC 44 CONTROLLER NO.2	
APPRO. MFG		DATE	APPRO. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO	LM	PART NUMBER 973678-0002 REV H

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LM PART NUMBER: 973673-0003

REV	DATE	BY	DESCRIPTION	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
00001	01/24/77					
00002				97294-0003	RES. FIX 100 1/4" X 1/2" W CERAMIC FILM	974-5425
00003					*K12 *K04 *K06 *K08 *K010	
00004					*K117 *K192 *K194 *K196 *K198	
00005					*K1910 *K1912 *K2914 *K2916	
00006	01/24/77			97294-0003	RES. FIX 300 1/4" X 1/2" W CERAMIC FILM	974-5425
00007					*K12 *K04 *K06 *K08 *K010	
00008					*K117 *K191 *K193 *K195 *K197	
00009					*K199 *K1911 *K2912 *K2914	
00010	01/24/77			97294-0003	RES. FIX 1.0" 1/4" X 1/2" W CERAMIC FILM	974-5425
00011					*K117	
00012	01/24/77			97292-0007	CAP. FIX CERAMIC 1001 1/2" 10% 200V	974-33014/01-1307
00013					*K01 *K06 *K08	
00014	01/24/77			97292-0007	RES. FIX 5.1" 1/4" X 1/2" W CERAMIC FILM	
00015					*K117	
00016	01/24/77			97292-0007	NETWORK-5A74074	974-6874074
00017					JS	
00018	01/24/77			97291-0001	PERM. JUMPER, 1.7" X 0.300" INCH	
00019					H3	

DESIGNER: DATE: 01/24/77 PROJECT: ENGINEER: DATE: RELEASE: DATE: PROJECT NO: **LM** PART NUMBER: 973673-0003 REV: H



TEXAS INSTRUMENTS
CORPORATED

DATE: 01/24/77

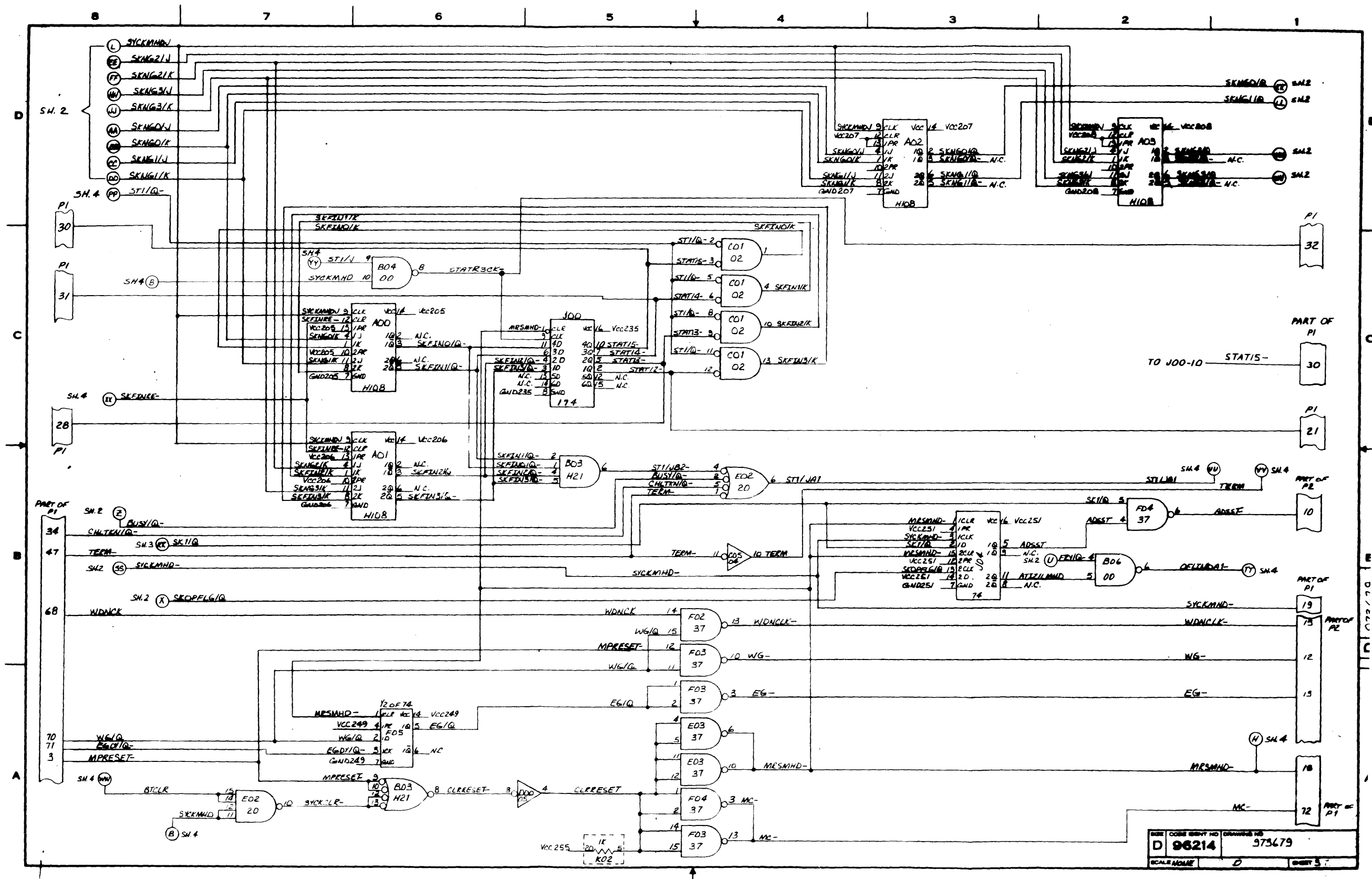
LIST OF MATERIAL

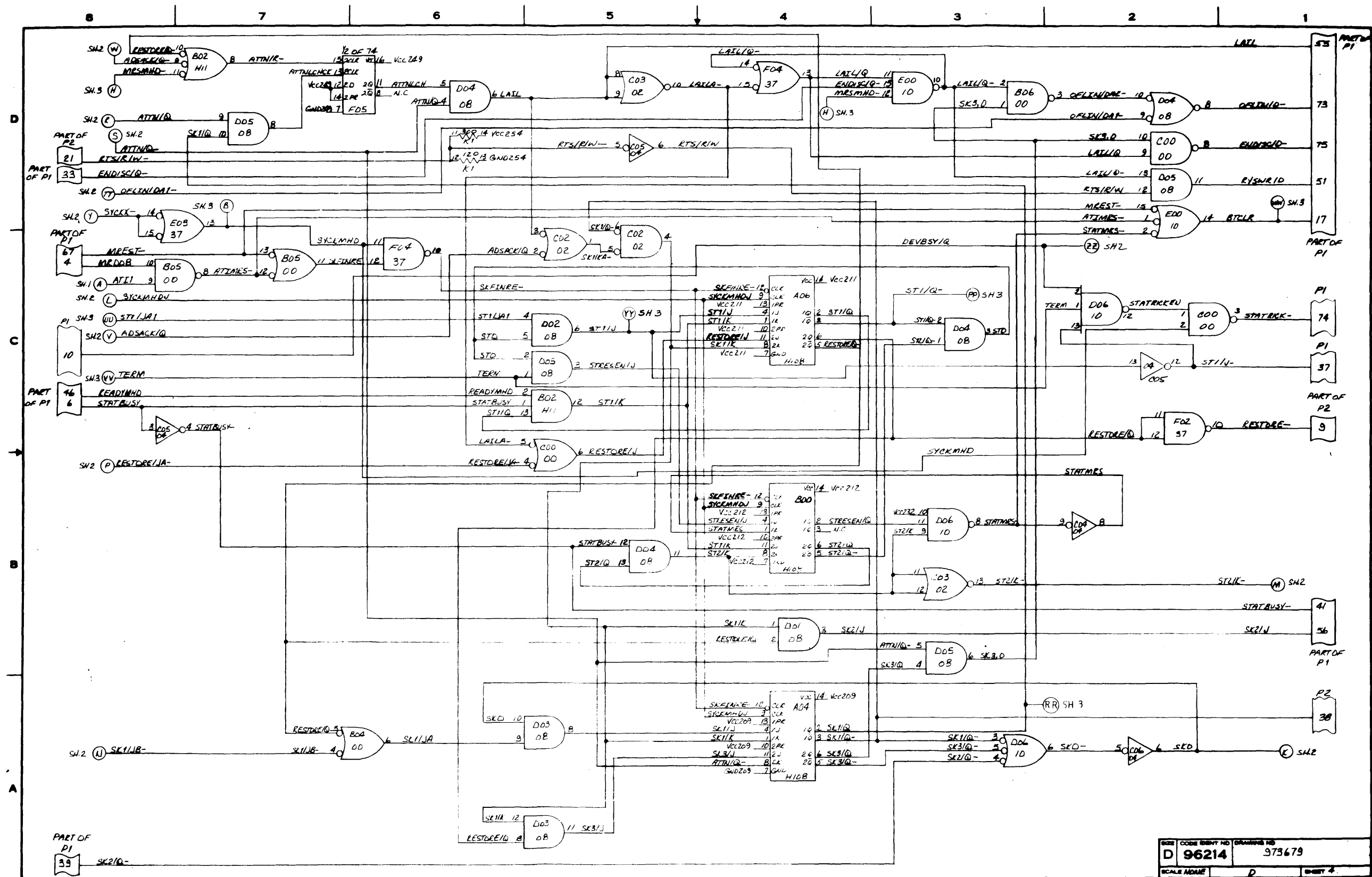
PAGE: 4 of 4

LM PART NUMBER: 973673-0003

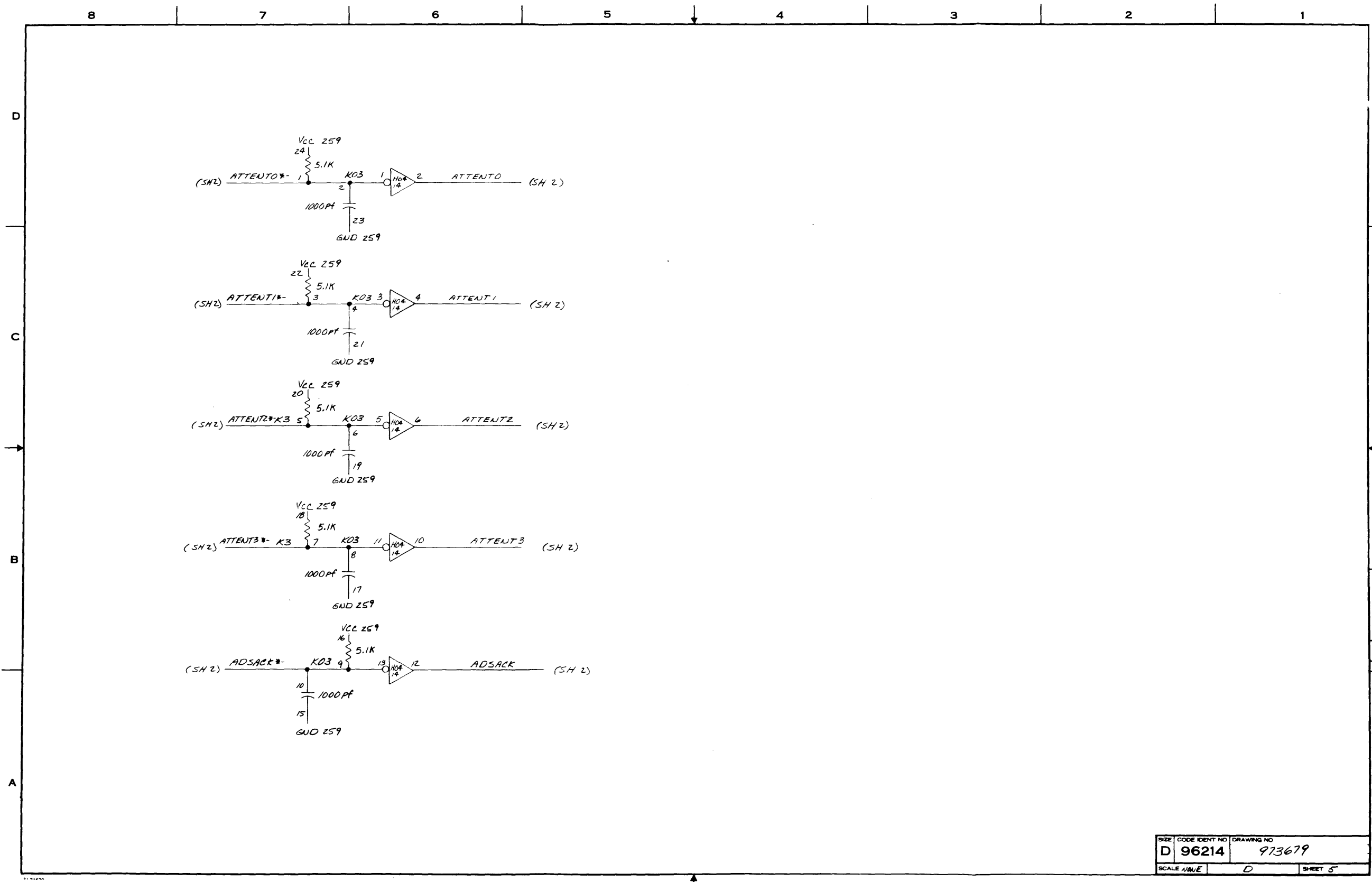
REV	DATE	BY	DESCRIPTION	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
00020	01/24/77			97346-0002	RES. FIX 5.1" 1/4" X 1/2" W CERAMIC FILM	974-5425
00021					*K01 *K06 *K08	

DESIGNER: DATE: 01/24/77 PROJECT: ENGINEER: DATE: RELEASE: DATE: PROJECT NO: **LM** PART NUMBER: 973673-0003 REV: H





SIZE	CODE IDENT NO	DRAWING NO
D	96214	973679
SCALE	NAME	SHEET
	D	4



SIZE	CODE IDENT NO	DRAWING NO
D	96214	973679
SCALE	NAME	SHEET
	D	5



OE9196

NOTES: UNLESS OTHERWISE SPECIFIED
 1. NETWORKS ARE SN74 SERIES
 2. CAPACITORS C1 THRU C14 TO BE INSTALLED PRIOR TO WIRE WRAP

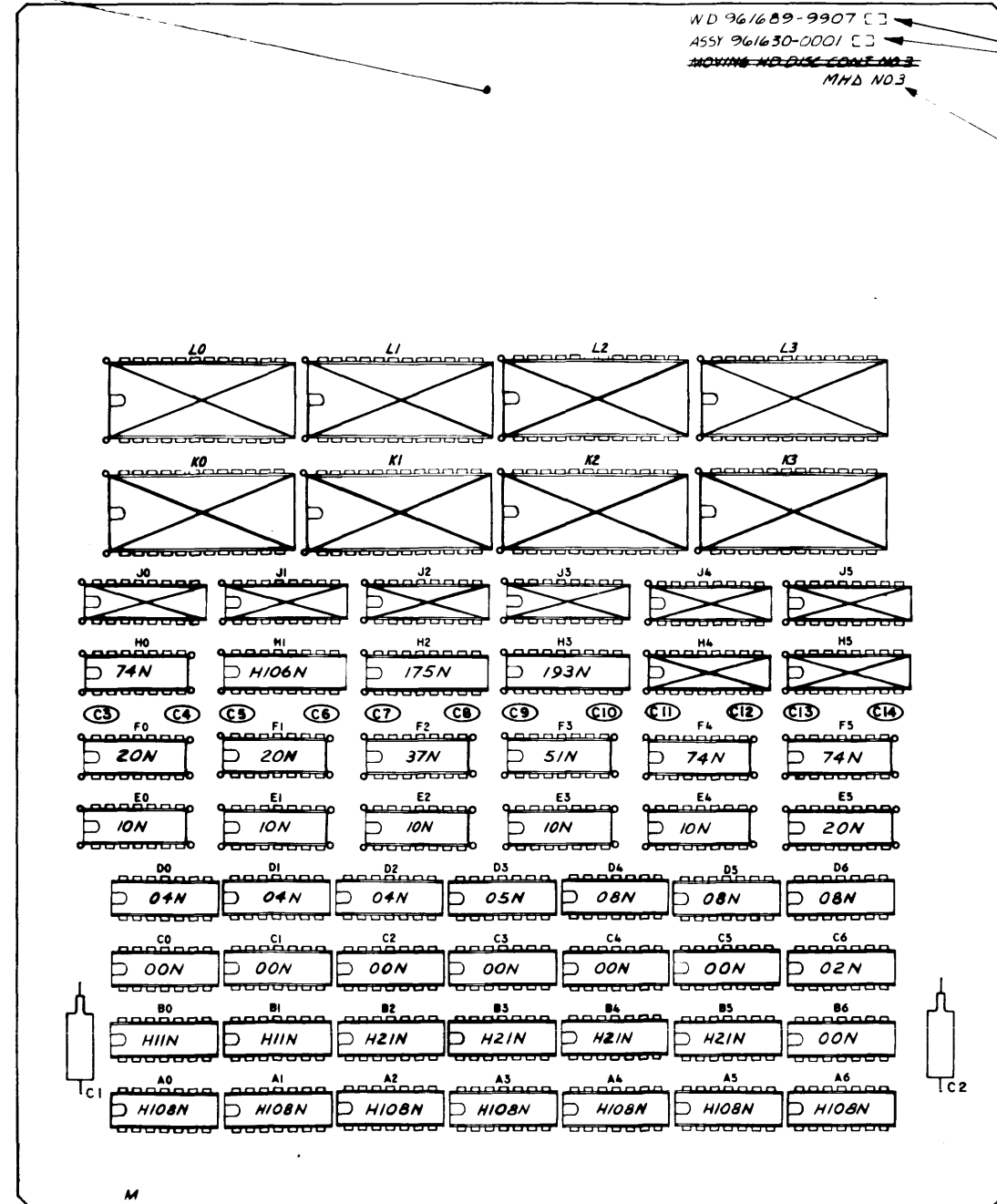
MARK ASSY. REV LETTER
 (-2 ONLY)

WD 961689-9907
 ASSY 961630-0001
~~MOVING HEAD DISC CONT NO.3~~
 MHD NO.3

MARK TITLE, ASSY PART NUMBER,
 WIRE DECK NUMBER AND APPROPRIATE
 REV LETTERS PER REV LEVEL BLOCK
 APPROX WHERE SHOWN PER PROCESS 1
 (-1 ONLY)

MARK TITLE

REV	DESCRIPTION	DATE	BY
A	381070 (D) J. P. ... 1-12-73	1/12/73	...
CHG: 1) LM IT. 1 WAS P/N 961629-0001			
2) LM IT. 2 WAS QTY OF 2 (P/N 539748-0001)			
3) PROCESS 1 WAS METAL STAMP/F-100 HEIGHT JR			
COLOR BLACK (4) MARK WAS METAL STAMPED			
ON REPLACED ITEM 2			
ADDED: 1) REV LEVEL BLOCK (2) NOTE 2 (3) ITEMS			
24 THRU 26			
B	394003 (C) ... 1/21/74	1/21/74	...
WAS NO TRM N3 (2) K0 THRU K3 WAS L0 THRU L3			
(3) ADDED ITEMS 27 & 28 TO P/L (4) UPDATED REV			
LEVEL BLOCK (4) ADDED "N" TO CONNECTOR TRS			
C	383789 (D) ... 1/15/75	1/15/75	...
LOGIC DIAG, PWB & UPDATED REV			
LEVEL BLOCK			
D	CN 412179 (D) ... 1/25/76	1/25/76	...
ADDED -0002 C/M (5) ADDED MULTI-			
WIRE BOARD TO REV LEVEL BLOCK			
E	CAUTION (C) ... 1-1-76	1-1-76	...
TEST PROCEDURE & UPDATED REV LEVEL			
BLOCK			
F	CN 420797 (C) ... 12/9/76	12/9/76	...
(1) UPDATE REV. BLK. (2) BOARD A-3, IN PROGRAM NAME			
DELETE "TITLE" AND ADD (-1 ONLY) (3) BOARD A-4,			
CHANGE "MOVING ... NO.3" TO "MHD NO.3" (4) BOARD A-4,			
ADD "MARK ASSY REV LETTER (-2 ONLY)			
G	CN 421977 (E) ... 5-9-77	5-9-77	...
(1) UPDATED REV LEVEL BLOCK			



961630-0002	MOVING HEAD DISC CONTROLLER NO 3000
961630-0001	MOVING HEAD DISC CONTROLLER NO 3000
PART NO	DESCRIPTION

REVISION LEVEL	TEST PROCEDURE (973776-9901)	X	R	F
	MULTI-WIRE BOARD (994035-0001)	*	*	A
	LOGIC DIAGRAM (973755-9901)	*	R	A
	PWB (217862-0002) (W/W)	G	G	H
	WIRE DECK (961689-9907)	B	B	B
	ASSEMBLY	A	B	C

UNLESS OTHERWISE SPECIFIED	PROCESS	QTY REQD	DESCRIPTION	VENOR PART NUMBER
DECIMAL XX ± 02 XXX ± 010	1. MARK PER F-100			
FRACTIONAL 2/64 ANGULAR 1/16	TYPE I THRU X OPT.	8980	A	953157
CONCENTRICITY MACHINED DIAMETERS 0.04 TR	HGT. .03 ± .03, COLOR OPT.	8980	A	953158
REMOVE ALL BURRS AND SHARP EDGES		6980	A	961792
DO NOT SCALE THIS DRAWING		7502		
ALL DIMENSIONS IN INCHES		7503		941870
SURFACES MARKED ✓ TO HAVE				
DIMENSIONED TO HOLE				
0.13 TO 1.34 ± .005				
1.34 TO 2.50 ± .008				
2.50 AND ABOVE ± .010				

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LM PART NUMBER 961630-0001 REV G 8

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		217862-0002	LOGIC BOARD-SINGLE ENDED WIRE WRAP	
0002	REF	EA		961689-9907	WIRE DECK,MHD 3, BLOCK 3	
0003	00007.000	EA		222222-7400	NETWORK SN7400N	-SN7400N
0004	00001.000	EA		222222-7402	NETWORK SA7402N	TI--SN7402N
0005	00003.000	EA		222222-7404	NETWORK SN7404N	
0006	00001.000	EA		222222-7405	NETWORK SA7405N	
0007	00003.000	EA		222222-7408	NETWORK-SN7408N	
0008	00005.000	EA		222222-7410	NETWORK SN7410N	-SN7410N
0009	00001.000	EA		222222-7437	NETWORK SN7437N	
0010	00001.000	EA		222222-7451	NETWORK SN7451N	-SN7451N
0011	00003.000	EA		222222-7474	NETWORK SN7474N	-SN7474N
0012	00001.000	EA		222222-7175	NETWORK SN74175N	
0013	00001.000	EA		222222-7193	NETWORK SN74193N	-SN74193N
0014	00002.000	EA		240000-7411	NETWORK-SA74H11N	
0015	00004.000	EA		240000-7421	NETWORK-SN74H21N	
0016	00001.000	EA		240000-7106	NETWORK SN74H106N	
0017	00007.000	EA		240000-7108	NETWORK SN74H108N	
0018	00003.000	EA		222222-7420	NETWORK SN7420N	-SN7420N
0024	00012.000	EA		230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503N
0024A					C3 THRU C14	

DRAFTSMAN	DATE	CHKD. DRAFTSMAN	DATE	DESIGN NUMBER	DATE	TITLE
		<i>[Signature]</i>	8/24/76			MOVING HEAD DISC CONTROLLER NO 3
APPD. -MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						8100/8101
						LM PART NUMBER 961630-0001 REV G 8



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LM	PART NUMBER 961630-0002	REV G
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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	0001.000	EA		944035-0001	MWB, MOVING HEAD DISC CONTROLLER NO 3	
0003	0007.000	EA		22222-7400	NETWCRK SN7400N	-SN7400N
0004	0001.000	EA		22222-7402	NETWCRK SN7402N	TI--SN7402N
0005	0003.000	EA		22222-7404	NETWCRK SN7404N	
0006	0001.000	EA		22222-7405	NETWCRK SN7405N	
0007	0003.000	EA		22222-7408	NETWORK-SN7408N	
0008	0005.000	EA		22222-7410	NETWORK SN7410N	-SN7410N
0009	0001.000	EA		22222-7437	NETWCRK SN7437N	
0010	0001.000	EA		22222-7451	NETWCRK SN7451N	-SN7451N
0011	0003.000	EA		22222-7474	NETWCRK SN7474N	-SN7474N
0012	0001.000	EA		22222-7175	NETWCRK SN74175N	
0013	0001.000	EA		22222-7153	NETWCRK SA74193N	-SN74193N
0014	0002.000	EA		240000-7411	NETWCRK-SA74H11N	
0015	0004.000	EA		240000-7421	NETWCRK-SA74H21N	
0016	0001.000	EA		240000-7106	NETWORK SA74H106N	
0017	0007.000	EA		240000-7108	NETWCRK SN74H108N	
0018	0003.000	EA		22222-7420	NETWCRK SN7420N	-SN7420N
0024	00012.000	EA		230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503A
0024A					C3 THRU C14	
0025	0002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT QPL-M39003/1-2271	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	MOVING HEAD DISC CONTROLLER NO 3	
APPD-MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	LM	PART NUMBER 961630-0002

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LM	PART NUMBER 961630-0002	REV G D
-----------	----------------------------	------------

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0025A					C1 C2	
0026	AR	FT		535978-0058	WIRE ELEC., SOLID, "KYNAR" INSUL #30 AWG	
0027	REF	EA		973755-9901	LOGIC DIAGRAM, MHD #3	
0028	REF	EA		973776-9901	TEST PROCEDURE, MHD #3	

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	MOVING HEAD DISC CONTROLLER NO 3	
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	LM	PART NUMBER 961630-0002
								REV G D

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LM PART NUMBER 961630-0001 REV G D

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0025	00002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL-M39003/1-2271
0025A					C1 C2	
0026	AR	FT		535978-0058	WIRE ELEC., SOLID, "KYNAR" INSUL #30 AWG	
0027	REF	EA		973755-9901	LOGIC DIAGRAM, MHD #3	
0028	REF	EA		973776-9901	TEST PRCCEDURE, MHD #3	

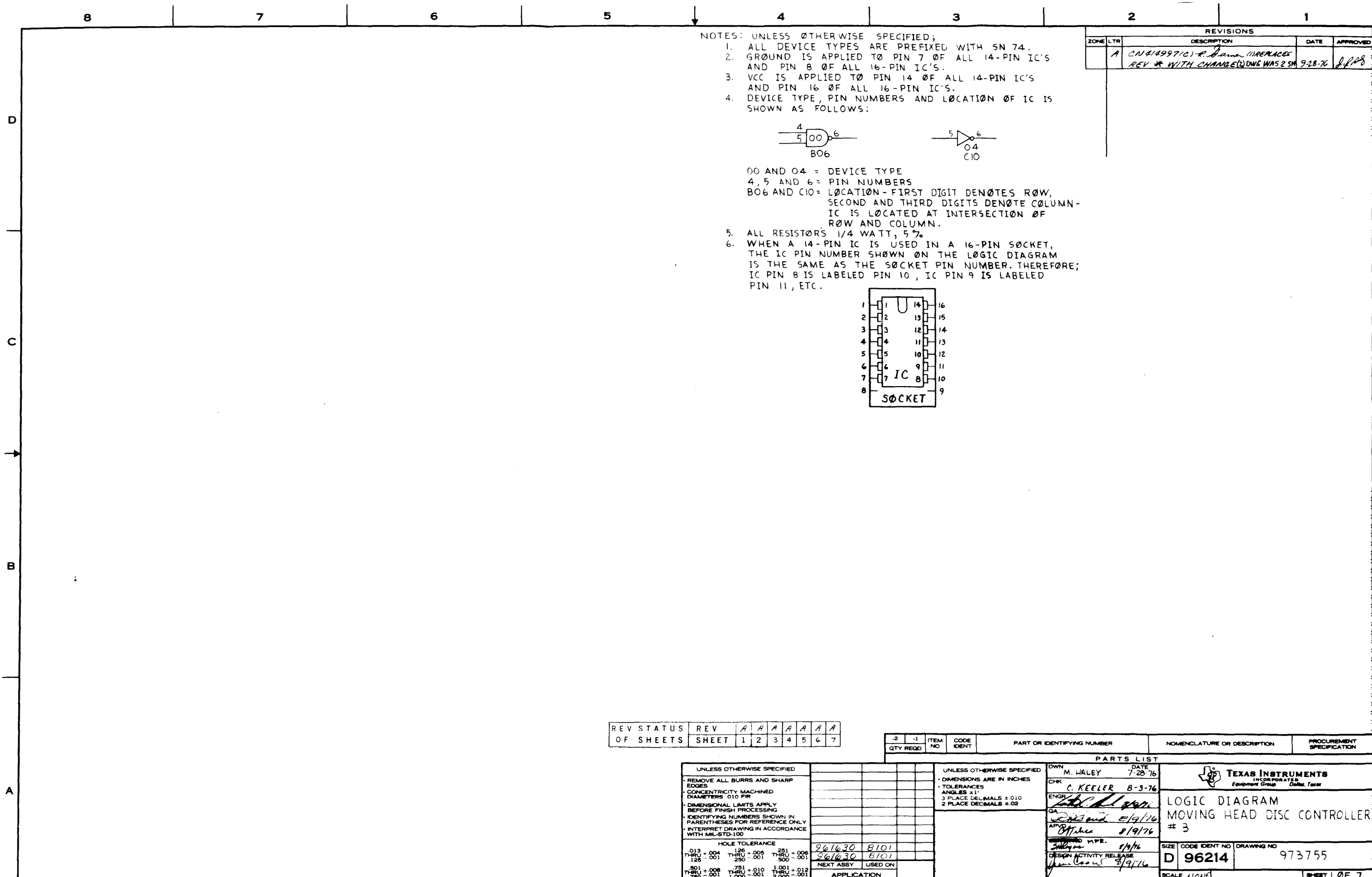
DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	MOVING HEAD DISC CONTROLLER NO 3	
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	LM	PART NUMBER 961630-0001 REV G D

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	21418997(C) R. Hanna (REPLACES REV # WITH CHANGE) DMS WAS 2 SW	9-28-76	J.P.P.

REV STATUS	REV	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7

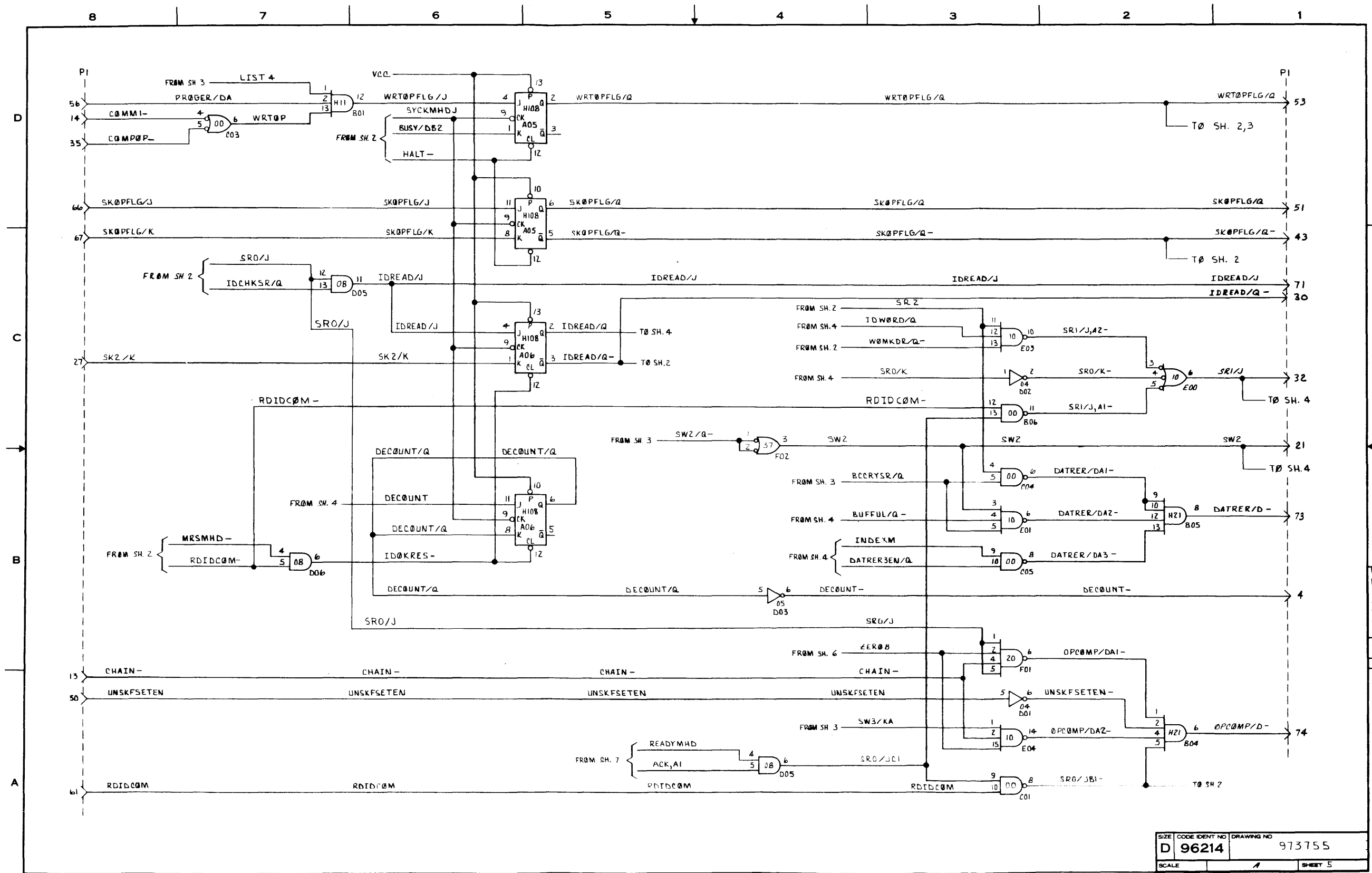
-2	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
PARTS LIST						
				OWN M. WALEY	DATE 7-28-76	<p>TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas</p>
				CHK C. KEELER	8-3-76	
				ENGR [Signature]	8/9/76	
				APP [Signature]	8/9/76	
				DESIGNED BY [Signature]	1/1/76	<p>LOGIC DIAGRAM MOVING HEAD DISC CONTROLLER # 3</p>
				DESIGN ACTIVITY RELEASE [Signature]	8/9/76	
				SIZE D	CODE IDENT NO 96214	DRAWING NO 973755
				SCALE NONE	SHEET 1 OF 7	

UNLESS OTHERWISE SPECIFIED		
REMOVE ALL BURRS AND SHARP EDGES		
CONCENTRICITY MACHINED DIAMETERS 0.10 P/R		
DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING		
IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY		
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100		
HOLE TOLERANCE		
0.13 THRU +.001	1.26 THRU +.005	251 THRU +.008
1.25 THRU -.001	250 THRU -.001	500 THRU -.001
501 THRU +.008	751 THRU +.010	1.001 THRU +.012
750 THRU +.001	1.000 THRU -.001	2.000 THRU -.001
NEXT ASSY USED ON		
APPLICATION		

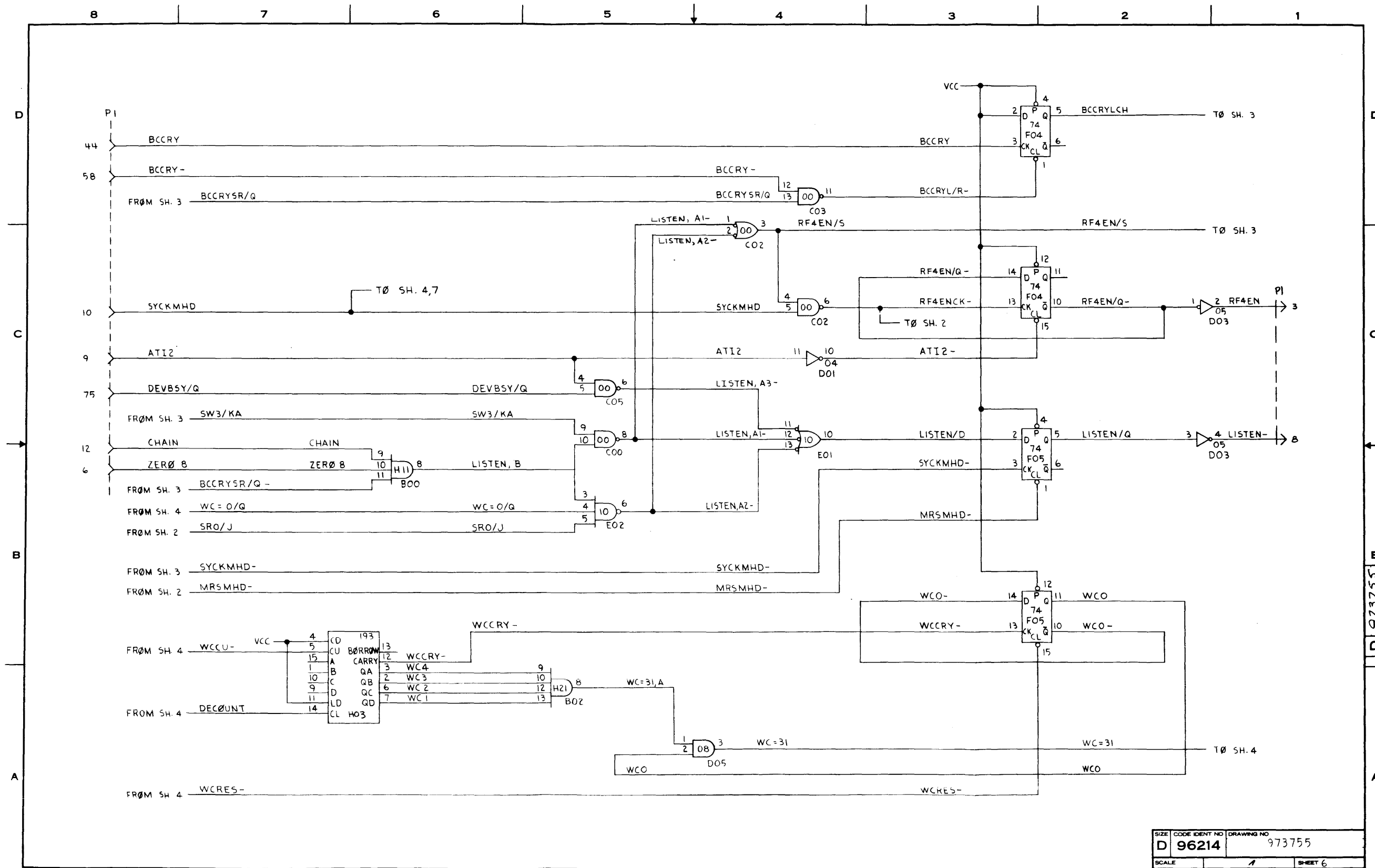
UNLESS OTHERWISE SPECIFIED	
DIMENSIONS ARE IN INCHES	
TOLERANCES ARE ±	
ANGLES ±1°	
3 PLACE DECIMALS ±0.10	
2 PLACE DECIMALS ±0.2	

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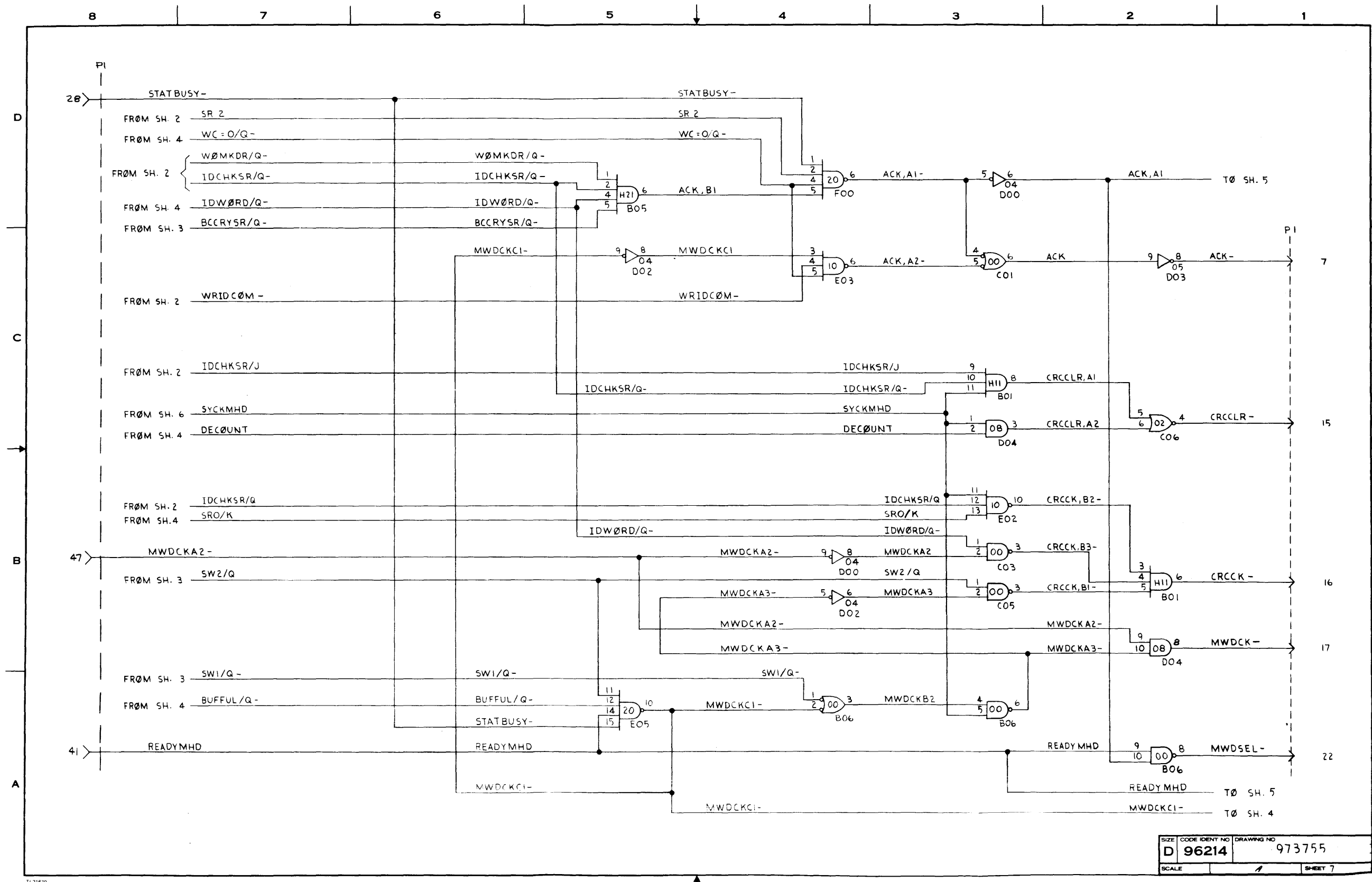
D 973755



SIZE	CODE IDENT NO	DRAWING NO
D	96214	973755
SCALE	A	SHEET 5



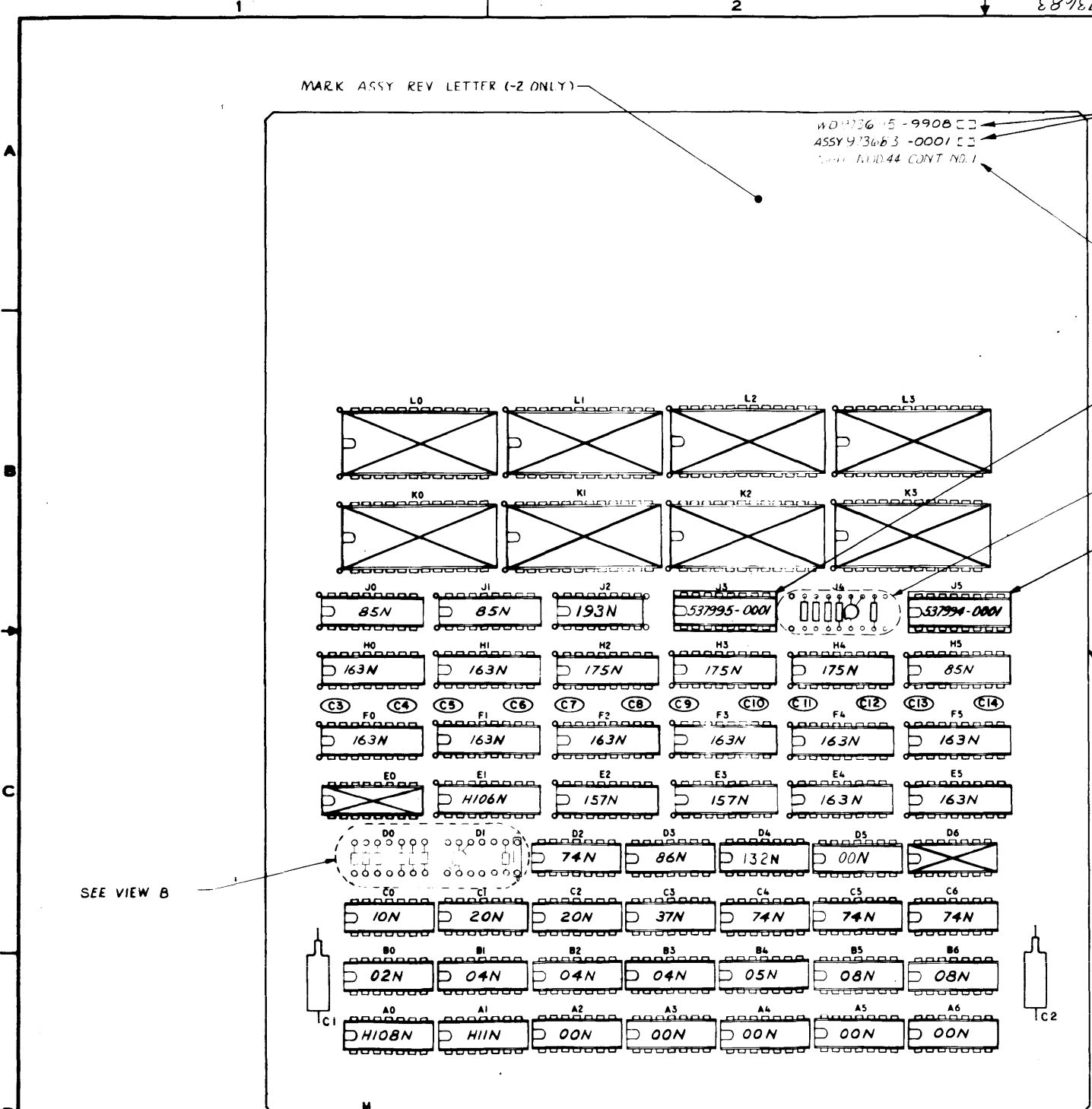
SIZE	CODE IDENT NO	DRAWING NO
D	96214	973755
SCALE	1	SHEET 6



SIZE	CODE IDENT NO	DRAWING NO
D	96214	973755
SCALE		SHEET 7



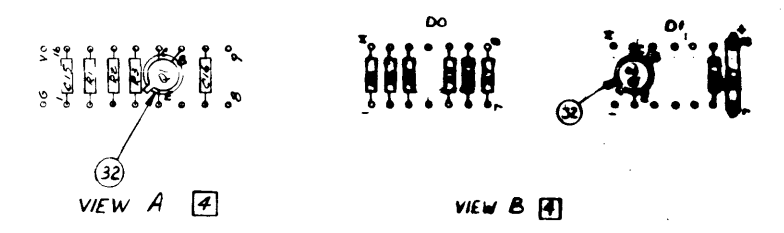
973683



NOTES: UNLESS OTHERWISE SPECIFIED
 1. NETWORKS ARE SN74 SERIES
 2. LEADS OF CAPACITORS (1) TRIM TO PROPER WIRE WRAP AND PROCESS 1
 3. MAXIMUM COMPONENT HEIGHT FROM BOARD IS .35 INCHES.

4. HAND SOLDER COMPONENTS PER PROCESS 1

REV	DESCRIPTION	DATE	BY
A	(1) 41118 (1) 7.0mm (1) ADDED LOGIC DIAG TO REV LEVEL BLOCK (2) ADDED DS WALS 0241 (3) DUAL IN LINE 4 QTY WALS 0241 DELETED DS IN ITEM 4A, ITEM 7 QTY 5, ADDED DS TO ITEM 3A (4) SUPPORTED REV LEVEL BLOCK	11/75	W. J. G.
B	CN 409332 (C) 4.0mm (1) DELETED NOTE 2 (2) UPDATED REV LVL BLK	11/75	W. J. G.
C	CN 412115 (D) 2.0mm (1) ADDED -2 LM AND UPDATED REV LEVEL BLOCK	9/75	W. J. G.
D	CN 421268 (A) 4.0mm (1) ZNC-1 ADDED DISCRETE COMPONENT LOCATIONS D0 & D1 (2) LCM D4 CHANGED (3) WALS 0241 L/M REVISED (4) UPDATED REV LVL BLK	11-2-76	W. J. G.
E	CN 422641 (D) 4.0mm (1) ON -14-2 LCM: ITEM 40 WAS 418767-0117 (2) UPDATED REV LEVEL BLK	11/76	W. J. G.
F	CN 420793 (C) 4.0mm (1) UPDATED REV LVL BLK (2) ADDED TEST PROC TO REV LVL BLK (3) REV. MARKING CALL-OUTS	11/76	W. J. G.
G	CN 421977 (E) 4.0mm (1) UPDATED REV LEVEL BLOCK	5-9-77	W. J. G.
H	CN 420298 (B) 2.0mm (1) UPDATED REVISION LEVEL BLOCK	4-6-77	W. J. G.
J	CN 392214 (C) 4.0mm (1) ADDED TO LM -0002 IT 4.4 (2) UPDATED REVISION LEVEL BLOCK	5-10-77	W. J. G.



973683-0002	MOVING HEAD DISC 44 CONTROLLER NO 4 M/W
973683-0001	MOVING HEAD DISC 44 CONTROLLER NO 4 W/W
PART NO	DESCRIPTION

REVISION LEVEL	TEST PROC 973685-9901	A	A	A	A
	MULTI-WIRE NO 944039-0001	*	A	A	A
	LOGIC DIAGRAM 973684-9901	-	A	A	A
	WIRE WRAP 80000 973682-0002	G	G	H	H
	WIRE DECK (973695-9900)	A	A	A	A
	ASSEMBLY	*	A	B	C

UNLESS OTHERWISE SPECIFIED
 DECIMAL: .002 .010 .015 .020
 FRACTIONAL: 1/64 ANGULAR: 2:1
 CONCENTRICITY: MACHINED DIAMETERS: 0.004 TIR
 ALL DIMENSIONS TO BE MET BEFORE PLATING
 REMOVE ALL BURRS AND SHARP EDGES
 DO NOT SCALE THIS DRAWING
 ALL DIMENSIONS IN INCHES
 SURFACES MARKED ✓ TO HAVE
 DRILLED HOLE TOLERANCES
 0.125 TO 1.250 ± .005
 1.250 TO 2.500 ± .010
 2.500 AND ABOVE ± .015

QTY	REQD	PART NUMBER	DESCRIPTION
8980	A	973674	MOVING HEAD DISC 44 CONTROLLER NO 4
8980	A		
8980	A		
7502		973674	
7503		973674	

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PART NUMBER	REV
LM 0973683-0001	J



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	00001.000	EA		0217862-0002	LOGIC BOARD-SINGLE ENDED WIPE WRAP		
0002	REF	EA		0273695-0008	MASTER FILE TAPE MODEL 44 MHD CONTR NO4		
0003	00006.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N	
0003A					A2 A3 A4 A5 A6 D5		
0004	00001.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N	
0004A					R0		
0005	00002.000	EA		0222222-7404	NETWORK SN7404N		
0005A					R1 R2 R3		
0006	00001.000	EA		0222222-7405	NETWORK SN7405N		
0006A					R4		
0007	00002.000	EA		0222222-7408	NETWORK-SN7408N		
0007A					R5 R6		
0008	00001.000	EA		0222222-7410	NETWORK SN7410N	-SN7410N	
0008A					C0		
0009	00002.000	EA		0222222-7420	NETWORK SN7420N	-SN7420N	
0009A					C1 C2		
0010	00001.000	EA		0222222-7437	NETWORK SN7437N		
0010A					C3		
0011	00004.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N	
0011A					D2 C4 C5 C6		
DRAFTSMAN		DATE	CRD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
			<i>J. R. ...</i>	5-11-77			MOVING HEAD DISC 44 CONTROLLER NC.4
APPD.-MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
							8980
						PART NUMBER	REV
						LM 0973683-0001	J



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PART NUMBER	REV
LM0973683-0001	J



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF MEAS	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0012	00003.000	EA		0222222-7485	NETWORK, SN7485N		
0012A					J0 J1 H5		
0013	00001.000	EA		0222222-7486	NETWORK-SN7486N		
0013A					D3		
0014	00002.000	EA		0222222-7157	NETWORK SN74157N		
0014A					E2 F3		
0015	00010.000	EA		0222222-7163	NETWORK SN74163N		
0015A					H0 H1 F0 F1 F2 F3 F4 F5		
0015B					E4 F5		
0016	00003.000	EA		0222222-7175	NETWORK SN74175N		
0016A					H2 H3 H4		
0017	00001.000	EA		0222222-7193	NETWORK SN74193N	-SN74193N	
0017A					J2		
0018	00001.000	EA		0240000-7411	NETWORK-SN74H11N		
0018A					A1		
0019	00001.000	EA		0240000-7106	NETWORK SN74H106N		
0019A					E1		
0020	00001.000	EA		0240000-7108	NETWORK SN74H108N		
0020A					A0		
0021	00001.000	EA		0537995-0001	NETWORK MC4044P	MOT -MC4044P	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DTSC 44 CONTROLLER NO.4
APPD. MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						PART NUMBER	REV
						LM0973683-0001	J

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LM 0973683-0001 J



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PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0022	00001.000	EA		0537994-0001	J3 NETWORK MC4024P	MJT -MC4024P	
0023	00012.000	EA		0230590-9000	J5 CAP .05 MF 12 V 20. % CER TRANSCAP C3 THRU C14	ERI -5635-000-Y5F09	
0024	00002.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MF 10 % 15 VOLT C1 C2	QPL -M39007/1-2271	
0025	AF	FT		0535978-0058	WIRE ELEC., SOLID, "KYNAR" INSUL #30 AWG		
0026	00001.000	EA		0972957-0001	TRANSISTOR, 2N930A NPN LOW CUR AMP, TO-5	MJT - 2N930A	
0027	00001.000	EA		0972927-0033	Q1 CAP FIX MICA 500V 180 PF 5%	QPL -CM05F181J00	
0028	00001.000	EA		0230618-0008	C16 CAP .10000 MF 100V 10. %	ERI -R131-M100-W5F1	
0029	00001.000	EA		0972975-0049	C15 RES FIX COMP 1.0 K OHMS 5% 1/8 WATT	QPL - RC050102J5	
0030	00001.000	EA		0530466-0074	R3 RESISTOR, FIXED, COMPOSITION-STYLE RC05		
0031	00001.000	EA		0530466-0078	P1 RESISTOR, FIXED, COMPOSITION-STYLE RC05		
0031A					P2		
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC 44 CONTROLLER NO.4
APPD. MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973683-0001	J

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PART NUMBER
LM0973683-0001 REV
J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0043A					C17		
DRAFTSMAN		DATE	CRD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
APPD.-MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER LM0973683-0001	REV J

MOVING HEAD DISC 44 CONTROLLER NO.4



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PART NUMBER	REV
LM 0573083-0002	J



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	0001.000	EA		0944039-0001	MWB, MOVING HEAD DISC 44 CONTROLLER NO 4		
0003	00006.000	EA		0222222-7400	NETWORK SN7400N	-SN7400N	
0003A					A2 A3 A4 A5 A6 D5		
0004	00001.000	EA		0222222-7402	NETWORK SN7402N	TI- -SN7402N	
0004A					B0		
0005	00003.000	EA		0222222-7404	NETWORK SN7404N		
0005A					B1 B2 B3		
0006	00001.000	EA		0222222-7405	NETWORK SN7405N		
0006A					B4		
0007	00002.000	EA		0222222-7408	NETWORK-SN7408N		
0007A					B5 B6		
0008	00001.000	EA		0222222-7410	NETWORK SN7410N	-SN7410N	
0008A					C0		
0009	00002.000	EA		0222222-7420	NETWORK SN7420N	-SN7420N	
0009A					C1 C2		
0010	00001.000	EA		0222222-7437	NETWORK SN7437N		
0010A					C3		
0011	00004.000	EA		0222222-7474	NETWORK SN7474N	-SN7474N	
0011A					D2 C4 C5 C6		
0012	00003.000	EA		0222222-7485	NETWORK, SN7485N		
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC 44 CONTROLLER NO. 4
APPD MFG		DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						PART NUMBER	REV
						LM 0573083-0002	J

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PART NUMBER	REV
LM 0973083-0002	J



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0012A					J0 J1 M5		
J013	00001.000	EA		J222222-7486	NETWORK-SN7486N		
0013A					D3		
0014	00002.000	EA		J222222-7157	NETWORK SN74157N		
0014A					E2 E3		
0015	00010.000	EA		J222222-7163	NETWORK SN74163N		
J015A					H0 H1 F0 F1 F2 F3 F4 F5		
0015B					E4 E5		
0016	00003.000	EA		J222222-7175	NETWORK SN74175N		
0016A					H2 H3 H4		
0017	00001.000	EA		0222222-7193	NETWORK SN74193N	-SN74193N	
0017A					J2		
0018	00001.000	EA		0240000-7411	NETWORK-SN74H11N		
0018A					A1		
0019	00001.000	EA		0240000-7106	NETWORK SN74H106N		
0019A					E1		
0020	00001.000	EA		J240000-7108	NETWORK SN74H108N		
0020A					A0		
0021	00001.000	EA		0537995-0001	NETWORK MC4044P	MOT -MC4044P	
0021A					J3		
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC 44 CONTROLLER NO. 4
APPD.-MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973083-0002	J



TEXAS INSTRUMENTS
INCORPORATED

DATE **05/18/77**

LIST OF MATERIAL

PAGE 3 of

PART NUMBER	REV
LM 0973683-0002	J



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0022	00001.000	EA		0537994-0001	NETWORK MC4024P	MOT -MC4024P	
0022A					J5		
0023	00012.000	EA		0230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI -5635-000-Y5F05	
0023A					C3 THRU C14		
0024	00002.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	WPL -M39003/1-2271	
0024A					C1 C2		
0025	AR	FT		0535978-0058	WIRE ELEC.,SOLID,"KYNAR" INSUL #30 AWG		
0026	00001.000	EA		0972957-0001	TRANSISTOR,2N930A NPN LOW CUR AMP,TO-5	MOT - 2N930A	
0026A					Q1		
0027	00001.000	EA		0972927-0033	CAP FIX MICA 500V 180 PF 5%	WPL -CM05E181J00	
0027A					C16		
0028	00001.000	EA		0230618-0008	CAP .10000 MF 100V 10. %	ERI -8131-M100-W5R1	
0028A					C15		
0029	00001.000	EA		0972975-0049	RES FIX COMP 1.0 K OHMS 5% 1/8 WATT	WPL - KC05G102J5	
0029A					R3		
0030	00001.000	EA		0530466-0074	RESISTOR,FIXED,COMPOSITION-STYLE RC05		
0030A					R1		
0031	00001.000	EA		0530466-0078	RESISTOR,FIXED,COMPOSITION-STYLE RC05		
0031A					R2		
0032	00002.000	EA		0185113-0001	X SPACER XST TU-18 CASE	* -	
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC 44 CONTROLLER NO. 4
APPD -MFG		DATE	APPD PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973683-0002	J

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LIST OF MATERIAL

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PART NUMBER	REV
LM 0973683-0002	J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0033	REF	EA		0973684-9901	DIAG, LOGIC, MHD 44 CONTROLLER NO.4		
0034	REF	EA		0973685-9901	UNIT TEST PROC, MHD 44 CONTROLLER NO.4		
0035	00001.000	EA		0222222-7132	NETWORK SN74132N		
0035A					U4		
0036	00002.000	EA		0538130-0019	RESISTOR, 56.00 OHM 1/8W 5%		
0036A					R4,R6		
0037	00001.000	EA		0972975-0025	RES FIX COMP 100 OHMS 5% 1/8 WATT	QPL - RC05G101J5	
0037A					R5		
0038	00001.000	EA		0972975-0033	RES FIX COMP 220 OHMS 5% 1/8 WATT	QPL - RC05G221J5	
0038A					R7		
0039	00001.000	EA		0972958-0002	TRANSISTOR, 2N2907A PNP GEN PURP SW TG-18 T1	- 2N2907A	
0039A					Q2		
0040	00001.000	EA		0972975-0079	RES FIX COMP 18K 5% 1/8 WATT	81349 -	
0040A					R8		
0041	00001.000	EA		0972934-0001	DIODE, 1N746A 3.3 V 5% SIL VOLT REG	QPL - 1N746A	
0041A					CR2		
0042	00001.000	EA		0153733-0001	DIODE GTD-132 / CGD-949		
0042A					CR1		
0043	00001.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 10% 15 VOLT	QPL -M39003/1-2271	
0043A					C17		
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MUOVING HEAD DISC 44 CONTROLLER NO. 4
APPD. MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973683-0002	J





TEXAS INSTRUMENTS
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DATE 05/18/77

LIST OF MATERIAL

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PART NUMBER	REV
LM 0973683-0002	J

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0044	00002.000	EA		0539544-0002	SOCKET, 16PIN IC LOW PROFILE SOLDER TAIL	TI -C93-16-02
0044A					XJ3 XJ5	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
						MOVING HEAD DISC 44 CONTROLER NL. 4
APPD. MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.

PART NUMBER	REV
LM 0973683-0002	J

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Digital Systems Division



TEXAS INSTRUMENTS
INCORPORATED

DATE 05/09/77

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PAGE 4 of

PART NUMBER	REV
LM 0973683-0001	J



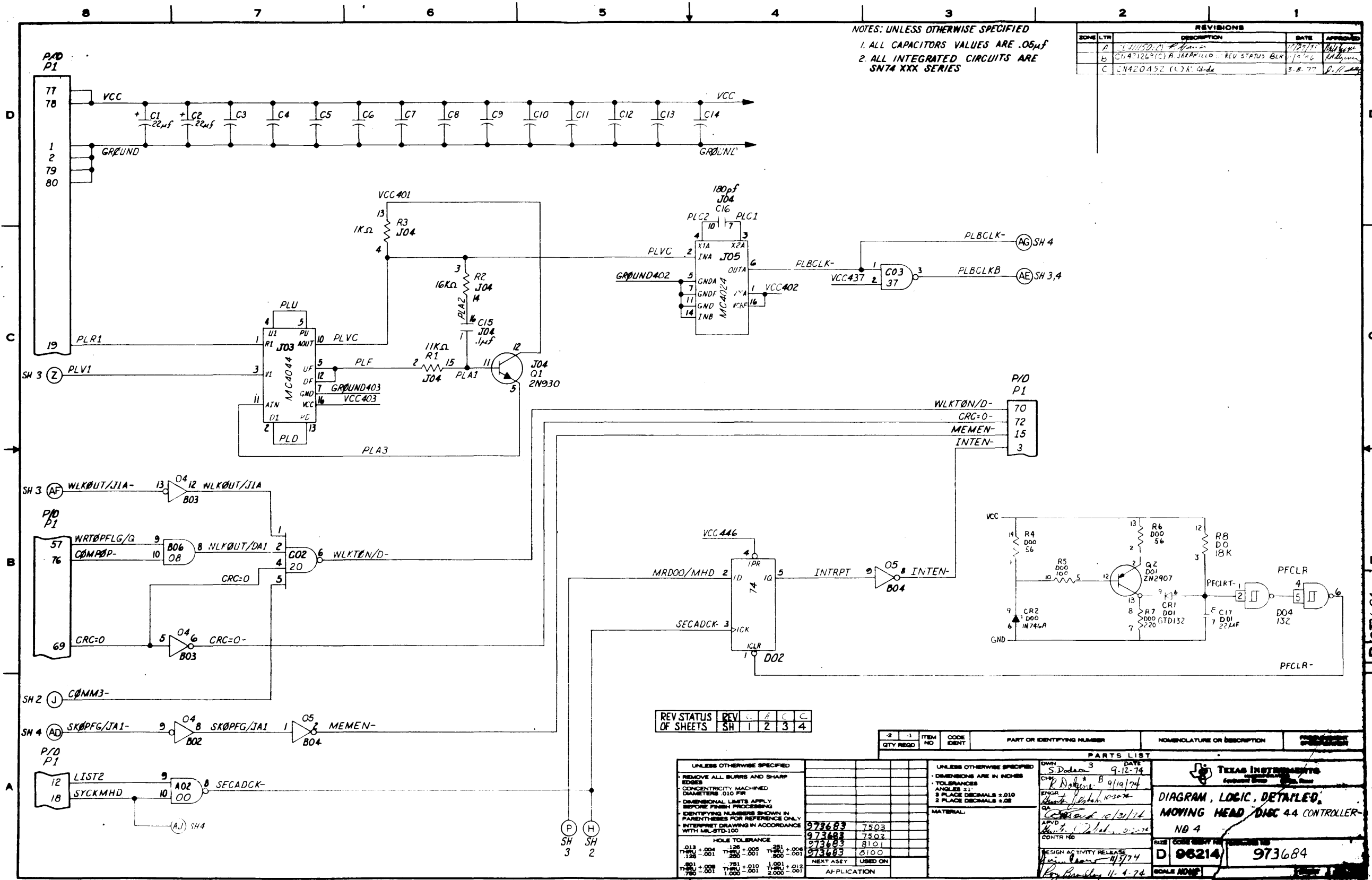
PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF MEAS	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0033	00002.000	EA		0185113-0001	X SPACER XSY TO-18 CASE	* -	
0033	REF	FA		0973684-9901	DIAG, LOGIC, MHD 44 CONTROLLER NO.4		
0034	FFF	EA		0973685-9901	UNIT TEST PROC, MHD 44 CONTROLLER NO.4		
0035	00001.000	FA		0222222-7132	NETWORK SN74132N		
0035A					D4		
0036	00002.000	FA		0538130-0019	RESISTOR, 56.00 OHM 1/8W 5%		
0036A					R4, R6		
0037	00001.000	EA		0972975-0025	RES FIX COMP 100 OHMS 5% 1/8 WATT	QPL - RC05C101JS	
0037A					R5		
0038	00001.000	EA		0972975-0033	RES FIX COMP 220 OHMS 5% 1/8 WATT	QPL - RC05C221JS	
0038A					R7		
0039	00001.000	EA		0972958-0002	TRANSISTOR, 2N2907A PNP GEN PURP SW TO-18	TI - 2N2907A	
0039A					Q2		
0040	00001.000	FA		0972975-0079	RES FIX COMP 18K 5% 1/8 WATT	81349 -	
0040A					R8		
0041	00001.000	FA		0972934-0001	DIODE, 1N746A 3.3 V 5% SIL VOLT REG	QPL - 1N746A	
0041A					CR2		
0042	00001.000	FA		0153733-0001	DIODE GTD-132 / CGD-949		
0042A					CR1		
0043	00001.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 10% 15 VOLT	QPL -M39007/1-2271	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC 44 CONTROLLER NO.4
APPD. MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973683-0001	J

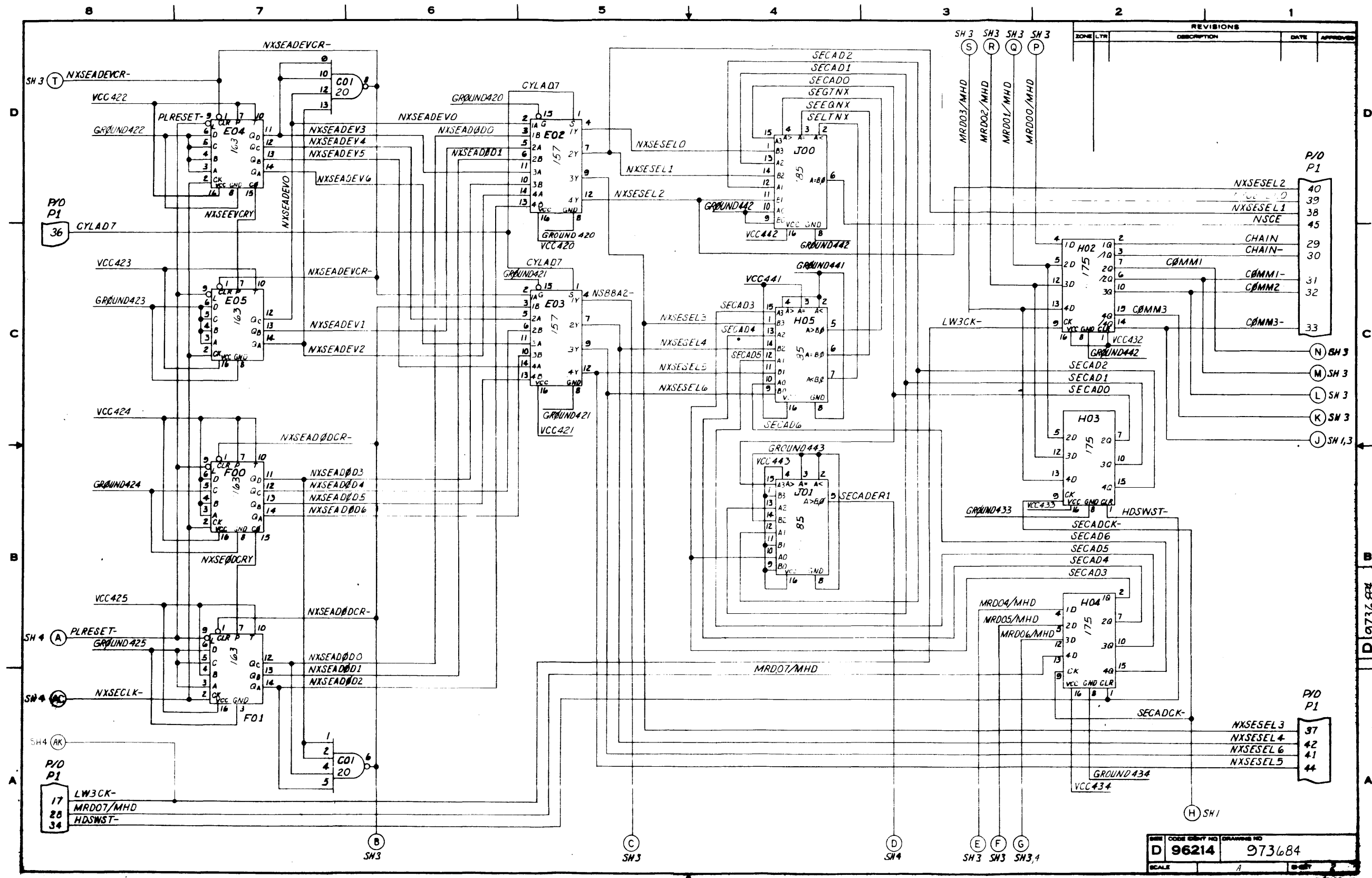
TI 13849

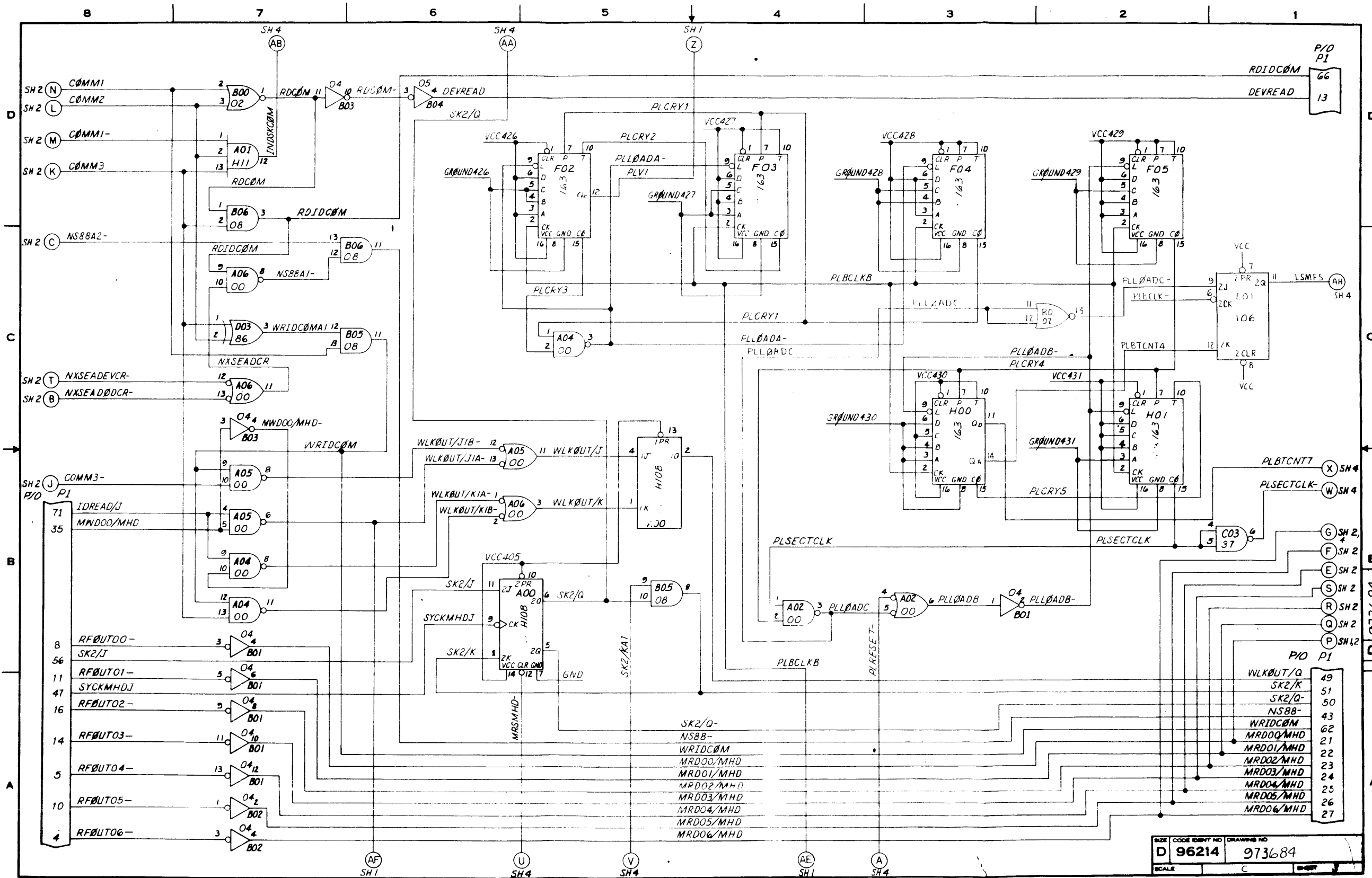
Change 1

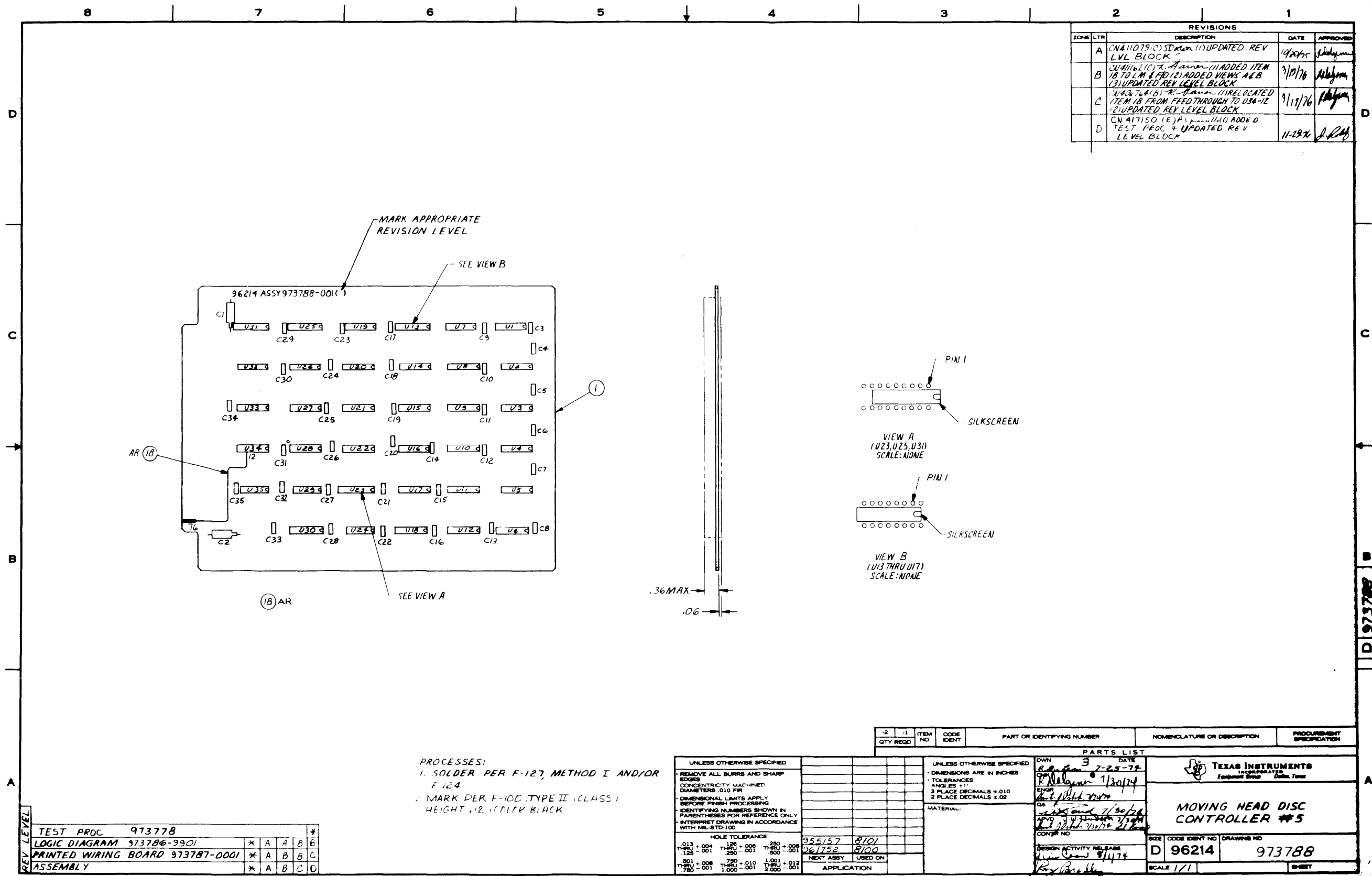
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Digital Systems Division









REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		CN 11079 (C) SD (1) UPDATED REV LVL BLOCK	1/20/76	[Signature]
B		U4 (1) U2 (C) F. A. (1) ADDED ITEM 18 TO L.M. & F.D. (2) ADDED VIEWS A & B (3) UPDATED REV LEVEL BLOCK	7/17/76	[Signature]
C		U4 (2) U4 (B) F. A. (1) RELOCATED ITEM 18 FROM FEED THROUGH TO U3A-12 (2) UPDATED REV LEVEL BLOCK	7/17/76	[Signature]
D		CN 417150 (E) F. A. (1) ADDED TEST PROC. & UPDATED REV LEVEL BLOCK	11-29-76	[Signature]

PROCESSES:
 1. SOLDER PER F-127, METHOD I AND/OR F 124
 2. MARK PER F-100, TYPE II, CLASS I HEIGHT .12, COLOR BLACK

REV. LEVEL	TEST PROC.	973778	*	A	B	C	D	*
	LOGIC DIAGRAM	973786-9901	*	A	A	B	B	E
	PRINTED WIRING BOARD	973787-0001	*	A	B	B	C	C
	ASSEMBLY		*	A	B	C	D	D

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED			UNLESS OTHERWISE SPECIFIED		
REMOVE ALL BURRS AND SHARP EDGES CONCENTRICITY MACHINED DIAMETERS .010 FIR DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100			DIMENSIONS ARE IN INCHES TOLERANCES ANGLES 1:1 3 PLACE DECIMALS ±.010 2 PLACE DECIMALS ±.02		
HOLE TOLERANCE .013 - .004 THRU +.008 .125 - .001 THRU +.008 .501 - .008 THRU +.010 .750 - .001 THRU +.012			MATERIAL: 955157 8101 061752 8100 NEXT ASSY USED ON APPLICATION		
OWN DATE [Signature] 7-25-74 [Signature] 1/20/74 [Signature] 1/30/76 [Signature] 7/17/76 [Signature] 11/29/76			TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas MOVING HEAD DISC CONTROLLER #5		
DESIGN ACTIVITY RELEASE			SCALE 1/1		
[Signature] 7/17/74			SIZE CODE IDENT NO DRAWING NO D 96214 973788		



TEXAS INSTRUMENTS
INCORPORATED

DATE 03/09/76

LIST OF MATERIAL

PAGE 1 of

PART NUMBER
LM 973788-0001 REV **D 00**

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	00001.000	EA		973787-0001	PWB, MHC, CCNTROLLER #5		
0002	00001.000	EA		222222-7400	NETWORK SN7400N	-SN7400N	
0002A					U1		
0003	00001.000	EA		222222-7402	NETWORK SN7402N	TI--SN7402N	
C003A					U35		
0004	00002.000	EA		222222-7404	NETWORK SN7404N		
C004A					U7,U24		
0005	00001.000	EA		222222-7408	NETWORK-SN7408N		
C005A					U25		
0006	00002.000	EA		222222-7430	NETWORK SN7430N	-SN7430N	
C006A					U19,U29		
0007	00004.000	EA		222222-7486	NETWORK-SN7486N		
C007A					U14,U15,U16,U17		
0008	00008.000	EA		222222-7153	NETWORK SN74153N	-SN74153N	
C008A					U2,U3,U4,U5,U8,U9,U10,U11		
0009	00003.000	EA		222222-7174	NETWORK SN74174N		
C009A					U6,U26,U27		
0010	00004.000	EA		222222-7175	NETWORK SN74175N		
0010A					U20,U21,U22,U23		
0011	00002.000	EA		222222-7193	NETWORK SN74193N	-SN74193N	
DRAFTSMAN		DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
			<i>R. Delaney</i>	3/10/76			MOVING HEAD DISC CONTROLLER #5
APPD.-MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
							8980
						PART NUMBER	REV
						LM 973788-0001	D 00

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DATE **03/09/76**

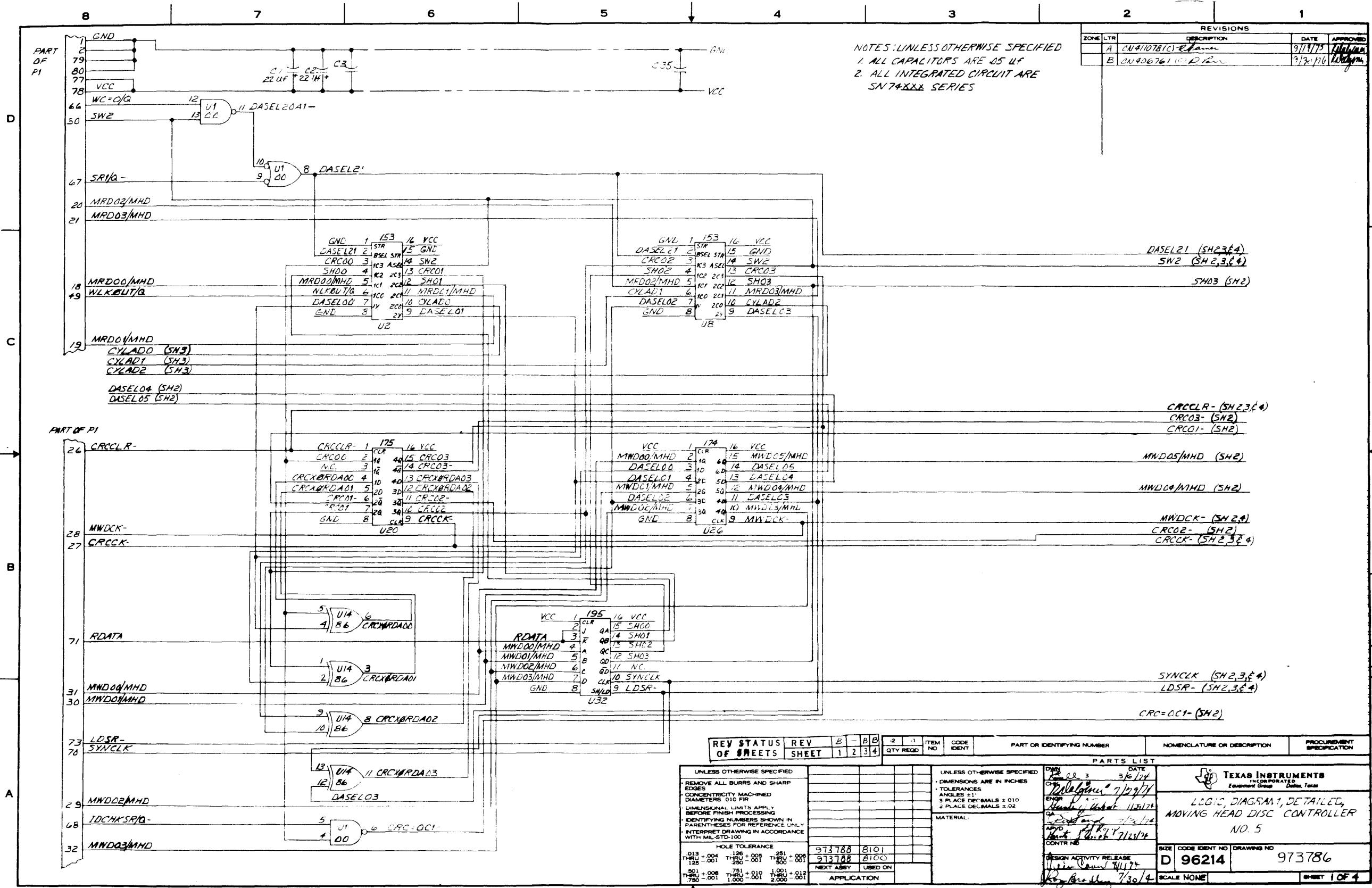
LIST OF MATERIAL

PAGE 2 of

PART NUMBER	REV
LM 973788-0001	D 02



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0011A					U30,U34		
0012	00004.000	EA		222222-7195	NETWORK SN74195N		
0012A					U12,U20,U32,U33		
0013	00003.000	EA		244712-8267	NETWORK,OM8267B		
0013A					U13,U18,U31		
0014	00033.000	EA		230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI-5635-000-Y5F0503M	
0014A					C3 THRU C35		
0015	00002.000	EA		972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL-M39003/1-2271	
0015A					C1,C2		
0016	REF	EA		973786-9901	DIAGRAM, LOGIC, MHD CONTROLLER #5		
0017	REF	EA		973778-9901	TEST PROCEDURE, MHD #5		
0018	AR	FT		538347-1999	WIRE TACK UP B-26 AWG 19 STR WHITE	JUD- HM0109	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							MOVING HEAD DISC CONTROLLER #5
APPD. MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO
						PART NUMBER	REV
						LM 973788-0001	D 02



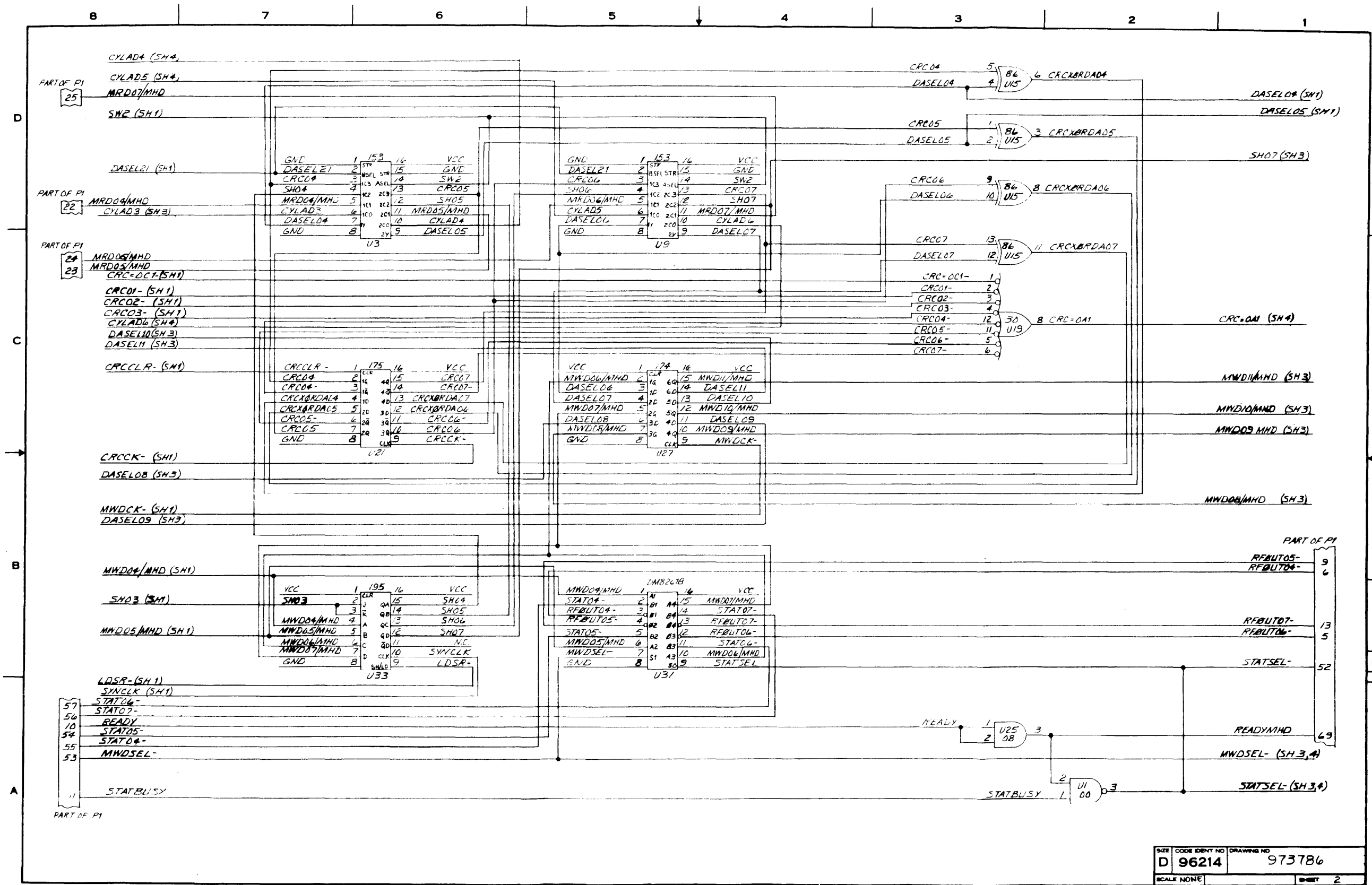
NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL CAPACITORS ARE .05 UF
 2. ALL INTEGRATED CIRCUITS ARE SN 74XXX SERIES

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
A		CU410781C	9/19/75
B		CU406761	9/23/76

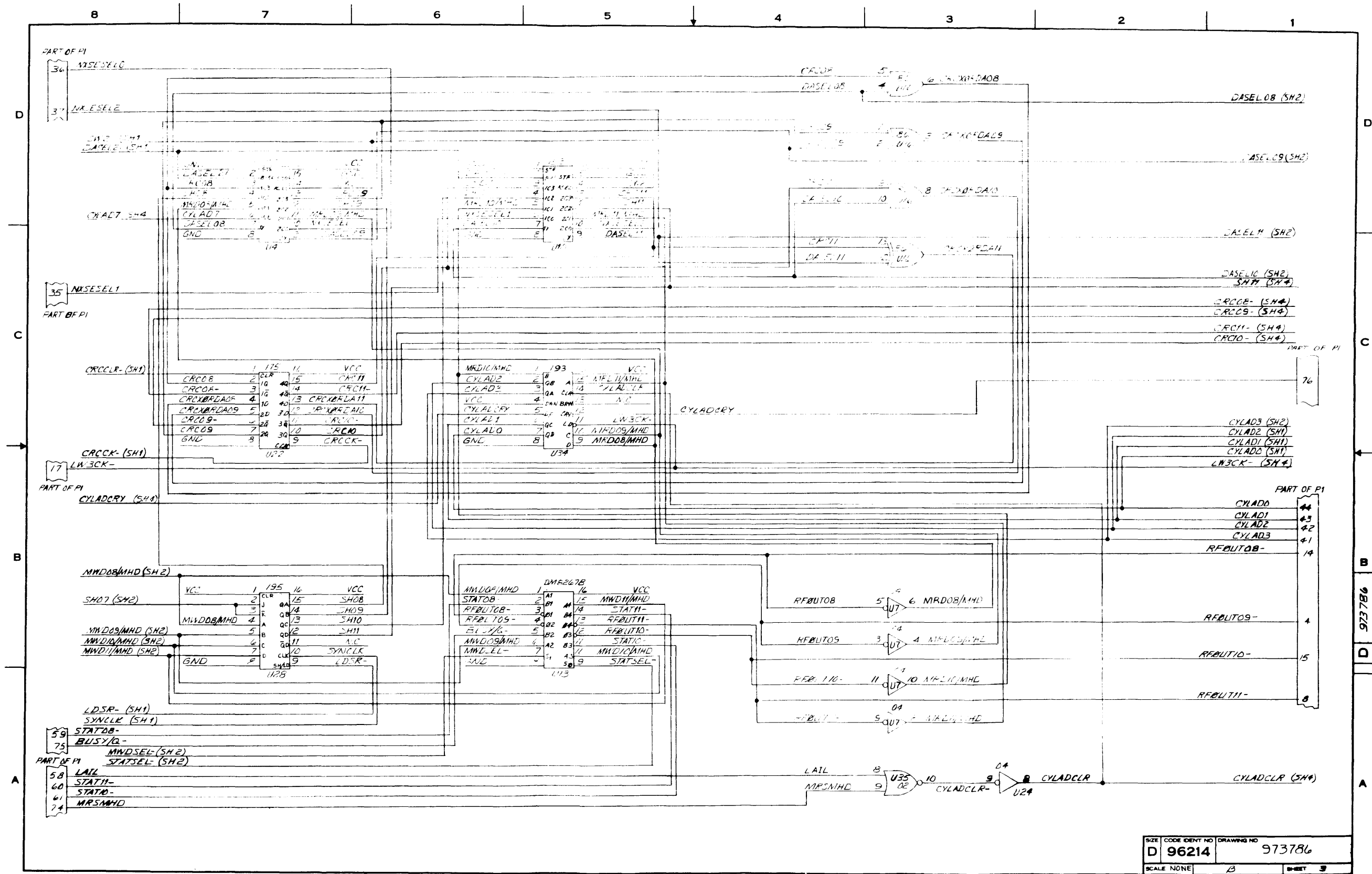
- DASEL21 (SH2,3,4)
- SWZ (SH2,3,4)
- SH03 (SH2)
- CRCCLR- (SH2,3,4)
- CRC03- (SH2)
- CRC01- (SH2)
- MWD05/MHD (SH2)
- MWD04/MHD (SH2)
- MWD03/MHD (SH2)
- MWD02/MHD (SH2)
- MWD01/MHD (SH2)
- MWD00/MHD (SH2)
- CRC02- (SH2)
- CRC00- (SH2,3,4)
- SYNCLK (SH2,3,4)
- LDR- (SH2,3,4)
- CRC=DCI- (SH2)

REV STATUS OF SHEETS	REV SHEET	B	B	2	1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
	1	2	3	4						

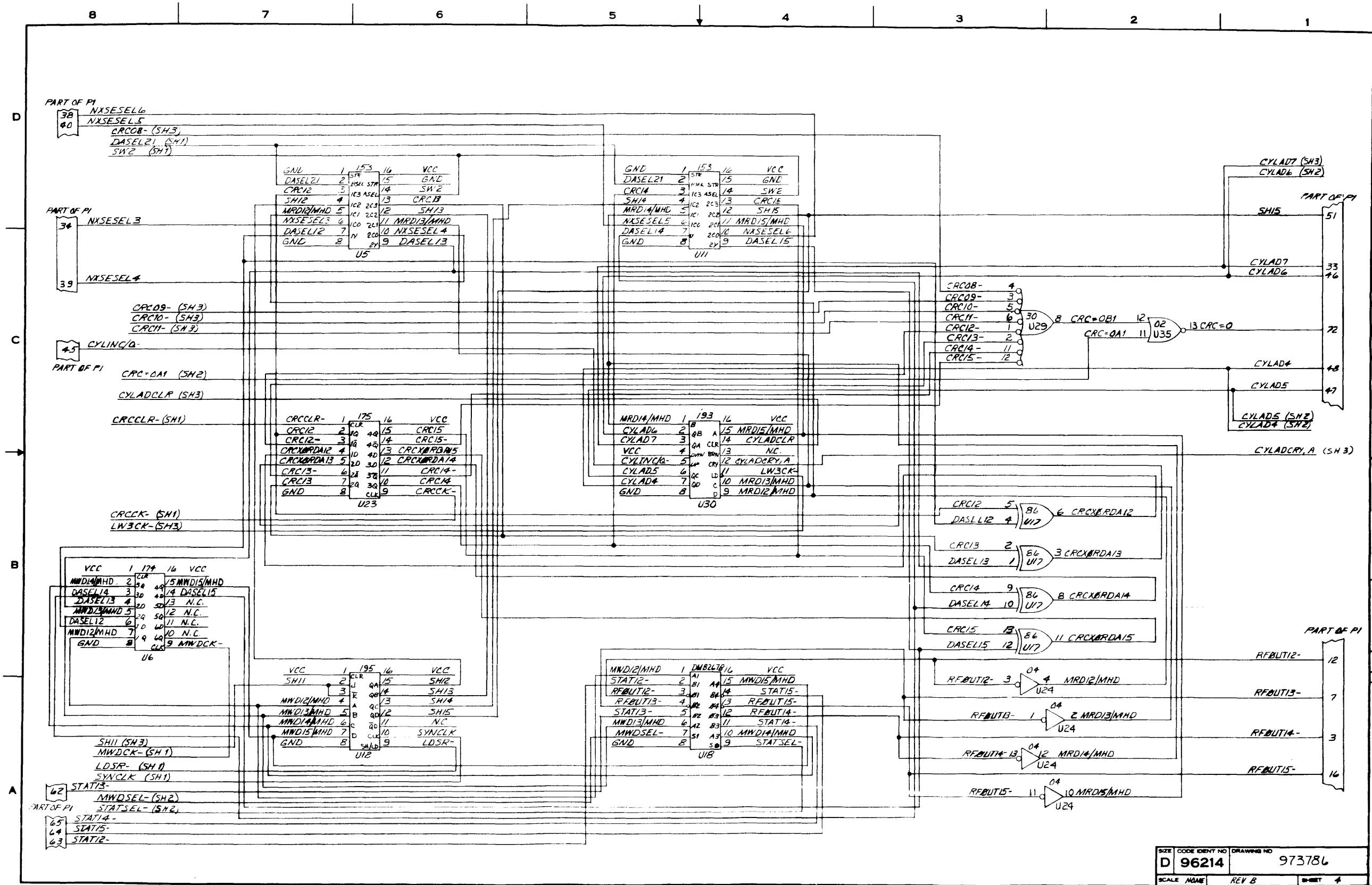
PARTS LIST	
QTY	DESCRIPTION
	UNLESS OTHERWISE SPECIFIED
	REMOVE ALL BURRS AND SHARP EDGES
	CONCENTRICITY MACHINED
	DIAMETERS .010 FIR
	DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING
	IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY
	INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100
	HOLE TOLERANCE
.013 + .004	.126 + .008
THRU .125 - .001	THRU .250 - .001
.501 + .008	.751 + .010
THRU .750 - .001	THRU 1.000 - .001
	2.000 - .001
	UNLESS OTHERWISE SPECIFIED
	DIMENSIONS ARE IN INCHES
	TOLERANCES
	ANGLES ±1°
	3 PLACE DECIMALS ±0.10
	2 PLACE DECIMALS ±0.2
	MATERIAL
	DATE
	3/10/74
	DESIGNED BY
	W. J. G. 7/19/74
	HECKED BY
	H. J. G. 11/21/74
	DATE
	7/23/74
	APPROVED BY
	W. J. G. 7/15/74
	CONTR NO
	DESIGN ACTIVITY RELEASE
	W. J. G. 7/11/74
	DATE
	7/30/74
	SCALE NONE



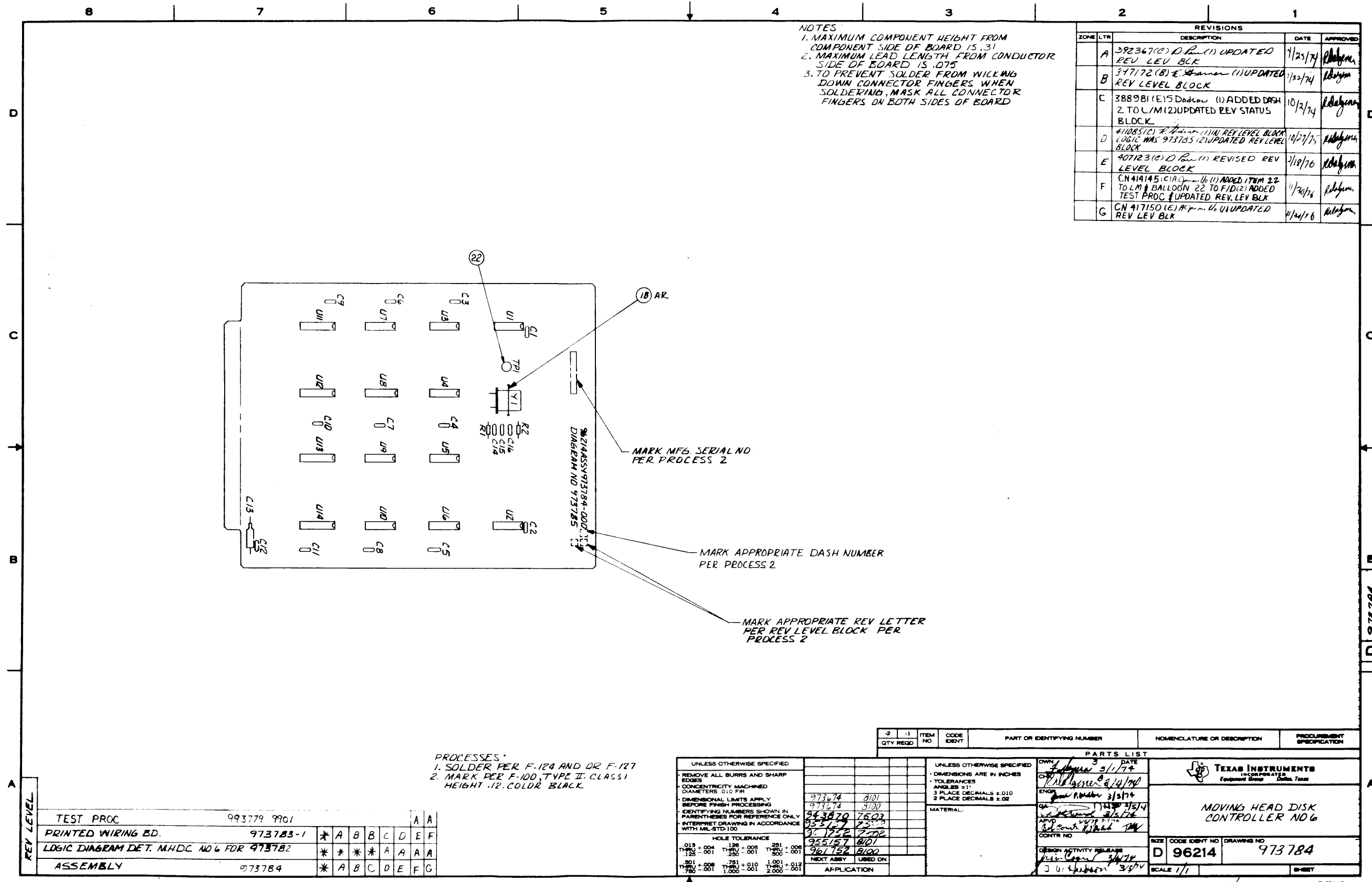
SIZE	CODE IDENT NO	DRAWING NO
D	96214	973786
SCALE NONE		SHEET 2



SIZE	CODE IDENT NO	DRAWING NO
D	96214	973786
SCALE NONE	B	SHEET 3



SIZE	CODE	IDENT NO	DRAWING NO
D	96214		973786
SCALE	NAME	REV	SHEET
		B	4



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LIST OF MATERIAL

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PAGE 1 of

PART NUMBER
LM 0973784-0001 REV
G F

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		022222-7400	NETWORK SN7400N	-SN7400N
0001A					U5	
0002	00001.000	EA		022222-7402	NETWORK SN7402N	TI- -SN7402N
0002A					U10	
0003	00001.000	EA		022222-7404	NETWORK SN7404N	
0003A					U6	
0004	00001.000	EA		022222-7405	NETWORK SN7405N	
0004A					U1	
0005	00001.000	EA		022222-7408	NETWORK-SN7408N	
0005A					U2	
0006	00001.000	EA		022222-7410	NETWORK SA7410N	-SN7410N
0006A					U9	
0007	00001.000	EA		022222-7430	NETWORK SN7430N	-SN7430N
0007A					U4	
0008	00001.000	EA		022222-7437	NETWORK SN7437N	
0008A					U3	
0009	00001.000	EA		022222-7474	NETWORK SN7474N	-SN7474N
0009A					U7	
0010	00004.000	EA		022222-7174	NETWORK SA74174N	
0010A					U8 U13 U14 U12	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	
		<i>J.R. [Signature]</i>	11-11-76			PW3 ASSY, MOVING HEAD DISK CONT NO.6	
APPD. -MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	
						7502	
						PART NUMBER	REV
						LM 0973784-0001	G F

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PAGE 1 of

PART NUMBER	REV
LM 0973784-0002	G #

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		022222-7400	NETWORK SN7400N	-SN7400N
0001A					U5	
0002	00001.000	EA		022222-7402	NETWORK SN7402N	TI- -SN7402N
0002A					U10	
0003	00001.000	EA		022222-7404	NETWORK SN7404N	
0003A					U6	
0004	00001.000	EA		022222-7405	NETWORK SN7405N	
0004A					U1	
0005	00001.000	EA		022222-7408	NETWORK-SN7408N	
0005A					U2	
0006	00001.000	EA		022222-7410	NETWORK SN7410N	-SN7410N
0006A					U9	
0007	00001.000	EA		022222-7430	NETWORK SN7430N	-SN7430N
0007A					U4	
0008	00001.000	EA		022222-7437	NETWORK SN7437N	
0008A					U3	
0009	00001.000	EA		022222-7474	NETWORK SN7474N	-SN7474N
0009A					U7	
0010	00004.000	EA		022222-7174	NETWORK SN74174N	
0010A					U8 U13 U14 U12	

DRAFTSMAN	DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	
						PW3 ASSY, MHD CONTROLLER NO. 6	
APPD.-MFG.	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	
						PART NUMBER	REV
						LM 0973784-0002	G #





TEXAS INSTRUMENTS
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DATE 11/10/76

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PART NUMBER	REV
LM 0973784-0002	G #



PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0011	00001.000	EA		0244712-0267	NETWORK, DM0267B	
0011A					U11	
0012	00001.000	EA		0418801-0007	CRYSTAL, QUARTZ 5.000 MHZ HC-18/U	QPL - CR-64/U
0012A					Y1	
0013	00002.000	EA		0972975-0041	RES FIX COMP 470 OHMS 5 % 1/8 WATT	QPL - RC05G471JS
0013A					R1 R2	
0014	00012.000	EA		0230590-9000	CAP .05 MF 12 V 2J. % CER TRANSCAP	EPI -5635-000-Y5F05
0014A					C1 THRU C12	
0015	00001.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL -M39003/1-2271
0015A					C13	
0016	00002.000	EA		0972926-0020	CAP FIX MICA 500V 51.0 PF 5 %	QPL -CM04E510J7D
0016A					C14 C16	
0017	00001.000	EA		0972929-0391	CAP FIX CERAMIC 470 PF 10 % 200 V	QPL -M39014/01-1391
0017A					C15	
0018	AR	FT		0538347-1999	WIRE SOCK UP 8-26 AWG 19 STR WHITE	JUD - HH0109
0019	00001.000	EA		0973783-0001	PWB, MOVING HEAD DISC CONTROLLER NO. 6	
0020	REF	EA		0973782-9901	LOGIC DIAGRAM, DETAILED MHD CONT. NO. 6	
0021	REF	EA		0973779-9901	TEST PROCEDURE, MHD NO. 6	
0022	00001.000	EA		0083654-0003	TERMINAL TURRET TYPE	USF - 2010B

DRAFTSMAN	DATE	CKD DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE	
						PWB ASSY, MHD CONTROLLER NO. 6	
APPD -MFG	DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.	
						PART NUMBER	REV
						LM 0973784-0002	G #

Change 1

6-84B

Digital Systems Division

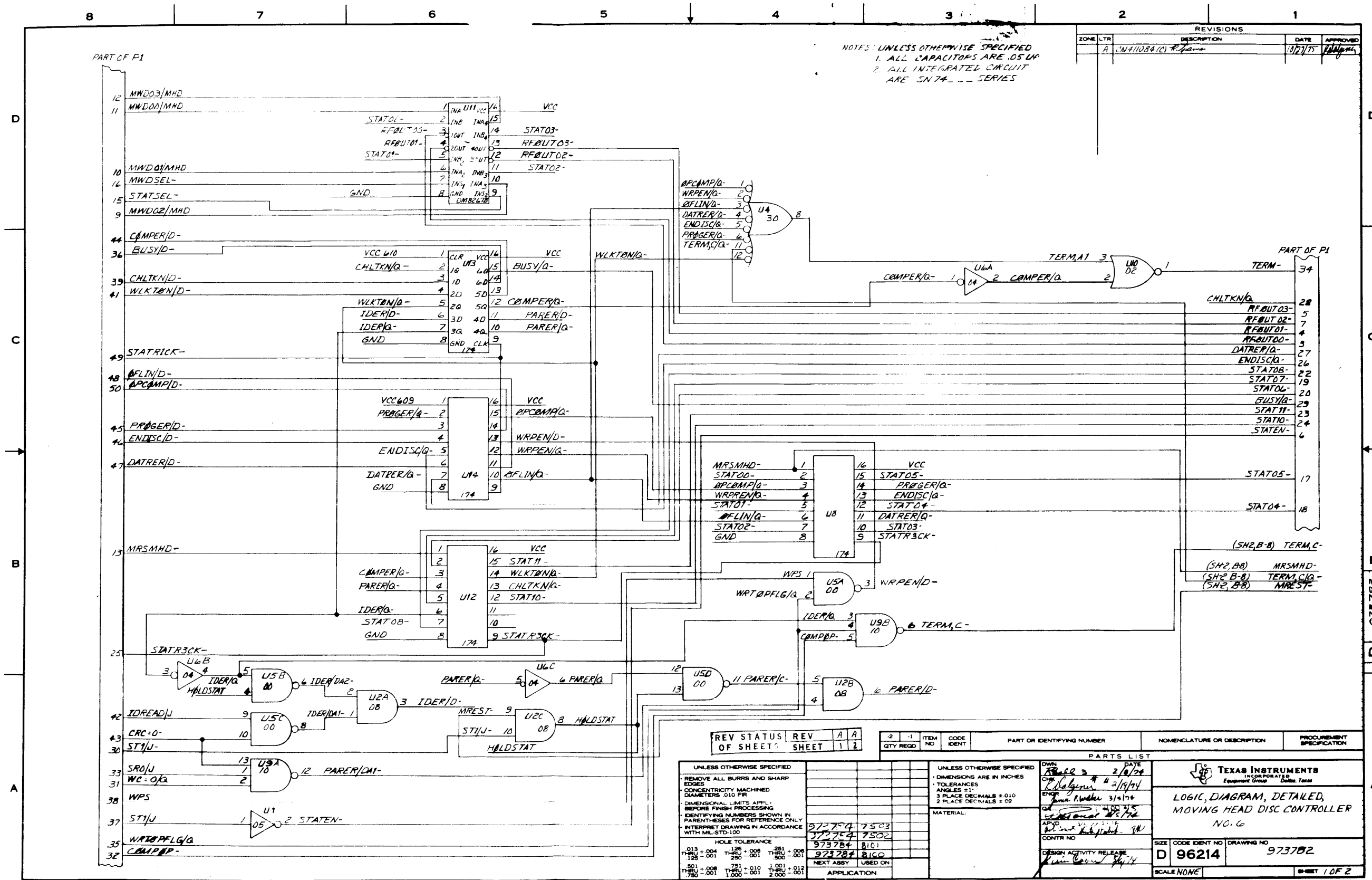


PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0011	00001.000	EA		0244712-8267	NETWORK, CM8267B		
0011A					U11		
0012	00001.000	EA		0418801-0005	CRYSTAL, QUARTZ 3.124 MHZ HC-18/U	QPL - CR-64/U	
0012A					Y1		
0013	00002.000	EA		0972975-0041	RES FIX COMP 470 CHMS 5 % 1/8 WATT	QPL - RC05G471JS	
0013A					R1 R2		
0014	00012.000	EA		0230590-9000	CAP .05 MF 12 V 20. % CER TRANSCAP	ERI -5635-000-Y5F05	
0014A					C1 C2 C3 C4 C5 C6 C7 C8 C9		
0014B					C10 C11 C12		
0015	00001.000	EA		0972924-0010	CAP FIX TANT SOLID 22 MFD 10 % 15 VOLT	QPL -M39003/1-2271	
0015A					C13		
0016	00002.000	EA		0972926-0020	CAP FIX MICA 500V 51.0 PF 5 %	QPL -CM04E510J00	
0016A					C14 C16		
0017	00001.000	EA		0972929-0391	CAP FIX CERAMIC 470 PF 10 % 200 V	QPL -M39014/01-1301	
0017A					C15		
0018	AR	FT		0538347-1999	WIRE HOOK UP 3-26 AWG 19 STR WHITE	JUD - HH0109	
0019	00001.000	EA		0973783-0001	PWB, MOVING HEAD DISC CONTROLLER NO. 6		
0020	REF	EA		0973782-9901	LOGIC DIAGRAM, DETAILED MHD CONT. NO. 6		
0021	REF	EA		0973779-9901	TEST PROCEDURE, MDH NO. 6		
0022	00001.000	EA		0083694-0003	TERMINAL TURRET TYPE	USE - 2010B	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
							PWB ASSY, MOVING HEAD DISK CONT NO. 6
APPD. -MFG		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
						PART NUMBER	REV
						LM 0973784-0001	G 5

Change 1

6-84

Digital Systems Division



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL CAPACITORS ARE .05 UF
 2. ALL INTEGRATED CIRCUIT ARE SN 74-__ SERIES

ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		CU#11084(1) R. James	1/27/75	[Signature]

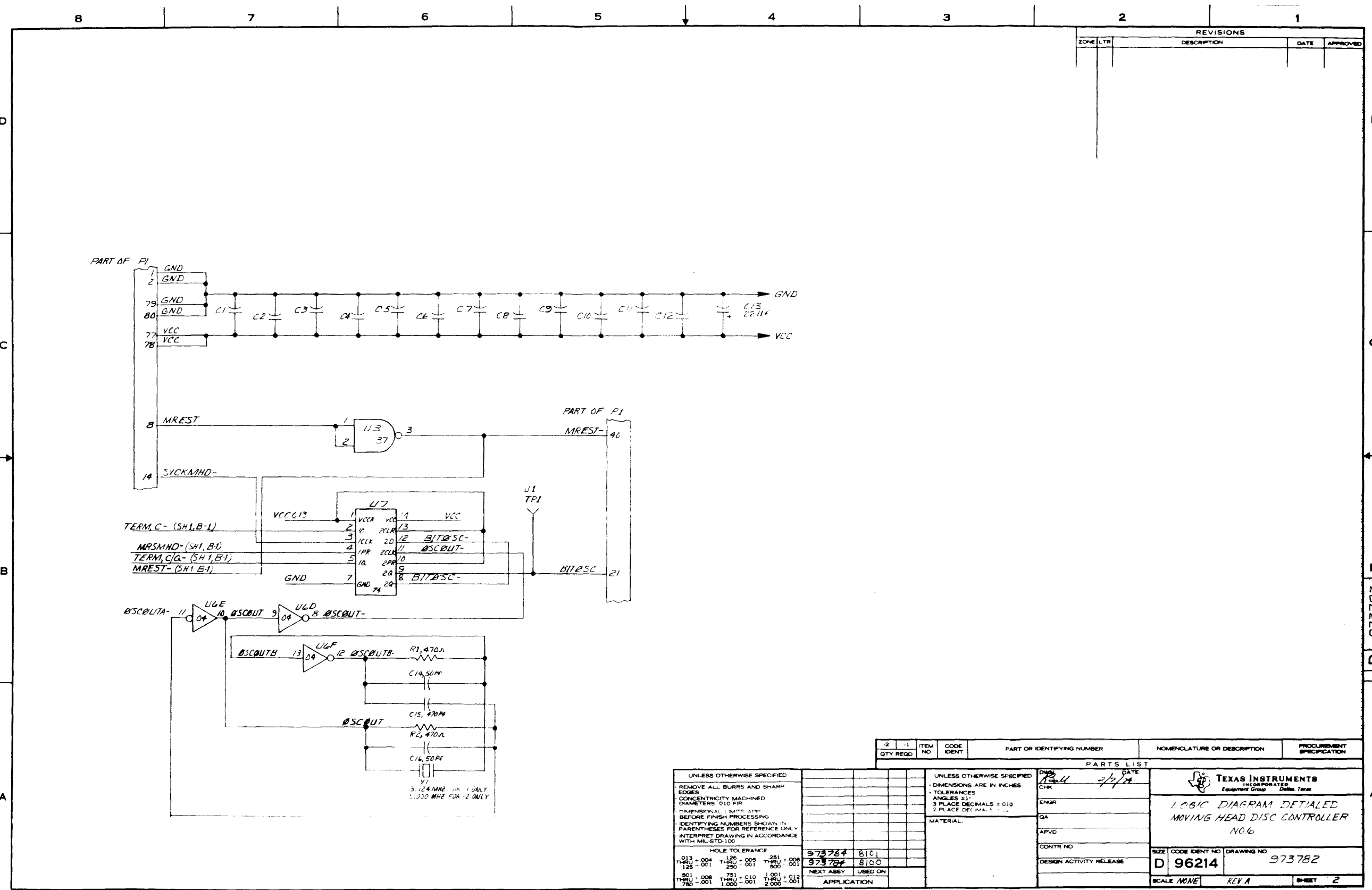
REV	STATUS	REV	DATE	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
2	-	1						
1								
A								
A								

HOLE TOLERANCE	
.013 +.004	.126 +.008
.125 - .001	.251 +.008
	.250 - .001
.501 +.008	.751 +.010
.750 - .001	1.000 - .001
	1.001 +.012
	2.000 - .001

UNLESS OTHERWISE SPECIFIED	UNLESS OTHERWISE SPECIFIED
REMOVE ALL BURRS AND SHARP EDGES	DIMENSIONS ARE IN INCHES
CONCENTRICITY MACHINED DIAMETERS .010 FIR	TOLERANCES ANGLES ±1°
DIMENSIONAL LIMITS APPL. BEFORE FINISH PROCESSING	3 PLACE DECIMALS ±.010
IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY	2 PLACE DECIMALS ±.02
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100	

DATE	BY	CHKD	APP'D	CONTR NO
2/10/74	[Signature]	[Signature]	[Signature]	
3/19/74	[Signature]	[Signature]	[Signature]	
3/20/74	[Signature]	[Signature]	[Signature]	
3/21/74	[Signature]	[Signature]	[Signature]	

SIZE	CODE IDENT NO	DRAWING NO
D	96214	973782



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE

QTY	REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

UNLESS OTHERWISE SPECIFIED		UNLESS OTHERWISE SPECIFIED	
REMOVE ALL BURRS AND SHARP EDGES	DIMENSIONS ARE IN INCHES	TOLERANCES	APPROVED
CONCENTRICITY MACHINED DIAMETERS .010 MIN	ANGLES ±1°	3 PLACE DECIMALS ±.010	DATE
PHIENSPRAL 3 WAY 5000 BEFORE FINISH PROCESSING	2 PLACE DECIMALS ±.005		9/1/78
IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY			
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100			

SIZE	CODE IDENT NO	DRAWING NO
D	96214	973782

SCALE	REV	SHEET
NONE	REV A	2



TEXAS INSTRUMENTS
INCORPORATED

DATE 07/02/76 LIST OF MATERIAL PAGE 1 of

LM PART NUMBER 973690-0015 REV A

PRINT ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF ISSUE	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER
0001	00001.000	EA		216136-C001	MOOD,CONNECTOR	
0002	00001.000	EA		231447-0800	CONNECTOR PC 36 PIN	VIK-2VH-36/1CN-5
C002A					P2	
0003	00004.000	EA		4182C1-0001	STRAP,MARKER,ADJUSTABLE,PLASTIC	QPL- MS3368-1-9
0004	00015.000	FT		972435-0007	INSUL SLEEVING,1.0" ID ZIPPER TUBE PVC	ZIP- ZTR-1000-63-20
0005	00002.000	EA		972988-0016	SCREW 4-40 X .438 PAN HEAD CRES	
0006	00001.000	EA		216138-C001	COVER,CONNECTOR	
0007	00001.000	FT		411400-0016	WIRE, 16AWG, SOLID, UNINSULATED	
0008	00108.000	FT		772570-0005	CABLE, ELEC, FLAT (ST-1426-19B-XL)	
C009	REF	EA		973691-9901	WIRE LIST, MHD44 TO CONTROLLER	
0010	00001.000	EA		973657-0003	CONNECTOR,RECTANGULAR,ELECTRICAL	
0010A					P1	
0011	00043.000	EA		411378-0004	CONTACT ELECTRICAL FEMALE	WIN-100-10265
0012	00003.000	EA		231554-0085	CONTACT SOCKET 100-10165	WIN-100-10165
0013	00002.000	EA		418212-0040	STRAP,TIECCMN,ADJUSTABLE,PLASTIC	QPL- MS3367-4-9
0014	AR	FT		411634-0710	SLEEVE,PVC, .066 DIA. CLEAR	QPL- MIL-1-631

DRAFTSMAN DATE 07/02/76 DESIGNED BY DATE 07/02/76 DESIGN ENGINEER DATE 07/02/76 TITLE CABLE ASSY, MHD44 TO CONTROLLER
 APP'D. MFG DATE 07/02/76 PROJECT ENGINEER DATE 07/02/76 RELEASED DATE 07/02/76 PROJECT NO 8100 PART NUMBER LM 973690-0015 REV A

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1/1



APPLICATION		REVISED		DATE		APPROVED	
A 973691		LTM					
NEXT ASSY	ISSUE ON	DESCRIPTION		DATE		APPROVED	
973690	8/00						
973690	8/01						
REV. STATUS		REV. SHEET		REV. SHEET		REV. SHEET	
1		2		3		4	
2		3		4		5	
3		4		5		6	
4		5		6		7	
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94		95		96		97	
95		96		97		98	
96		97		98		99	
97		98		99		100	

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
1	EXIST. CABLE RED TEFLON	AR	ADD50-	P2-36	P1-M		8
2	WHT		GND	P2-GND BUS	P1-GND BUS		
3	RED		ADD51-	P2-1	P1-BB		
4	WHT		GND	P2-GND BUS	P1-GND BUS		
5	RED		ADD52-	P2-34	P1-B		
6	WHT		GND	P2-GND BUS	P1-GND BUS		
7	RED		ADD53-	P2-3	P1-T		
8	WHT		GND	P2-GND BUS	P1-GND BUS		
9	RED		ADD54-	P2-4	P1-F		
10	WHT		GND	P2-GND BUS	P1-GND BUS		
11	RED		ADD55-	P2-5	P1-X		
12	WHT		GND	P2-GND BUS	P1-GND BUS		
13	RED		ADD56-	P2-6	P1-J		
14	WHT		GND	P2-GND BUS	P1-GND BUS		
15	RED		ADD57-	P2-7	P1-S		
16	WHT		GND	P2-GND BUS	P1-GND BUS		
17	RED		ADD58-	P2-8	P1-N		
18	WHT		GND	P2-GND BUS	P1-GND BUS		
19	RED		RESTORE-	P2-9	P1-W		
20	WHT		GND	P2-GND BUS	P1-GND BUS		
21	RED		ADD59-	P2-10	P1-T		
22	WHT		GND	P2-GND BUS	P1-GND BUS		
23	RED		HS-	P2-11	P1-A		
24	EXIST. CABLE WHT TEFLON	AR	GND	P2-GND BUS	P1-GND BUS		8



WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LN ITEM NO.
25	EXST CABLE RED TEFLON	AR	WG-	P2-12	P1-E	T P	8
26	WHT		GND	P2 GND BUS	P1 GND BUS	T P	
27	RED		EG-	P2-13	P1-K		
28	WHT		GND	P2 GND BUS	P1 GND BUS		
29	RED		PG-	P2-14	P1-E		
30	WHT		GND	P2 GND BUS	P1 GND BUS		
31	RED		WDNCLK-	P2-15	P1-B		
32	WHT		GND	P2 GND BUS	P1 GND BUS		
33	RED		SELUD-	P2-16	P1-L		
34	WHT		GND	P2 GND BUS	P1 GND BUS		
35	RED		SELUI-	P2-17	P1-R		
36	WHT		GND	P2 GND BUS	P1 GND BUS		
37	RED		SELUJ-	P2-18	P1-V		
38	WHT		GND	P2 GND BUS	P1 GND BUS		
39	RED		SELU3-	P2-19	P1-Z		
40	WHT		GND	P2 GND BUS	P1 GND BUS		
41	RED		FRY-	P2-20	P1-U		
42	WHT		GND	P2 GND BUS	P1 GND BUS		
43	RED		RTS/RW-	P2-21	P1-F		
44	WHT		GND	P2 GND BUS	P1 GND BUS		
45	RED		ADSACK-	P2-22	P1-P		
46	WHT		GND	P2 GND BUS	P1 GND BUS		
47	RED		SELIC-	P2-23	P1-U	T P	
48	EXST CABLE WHT TEFLON	AR	GND	P2 GND BUS	P1 GND BUS	T P	8

WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LN ITEM NO.
49	EXST CABLE RED TEFLON	AR	RCLK	P2-24	P1-A	T P	8
50	WHT		GND	P2 GND BUS	P1 GND BUS	T P	
51	RED		RD	P2-25	P1-C		
52	WHT		GND	P2 GND BUS	P1 GND BUS		
53	RED		SECTOR M-	P2-26	P1-W		
54	WHT		GND	P2 GND BUS	P1 GND BUS		
55	RED		INDEX M-	P2-27	P1-Y		
56	WHT		GND	P2 GND BUS	P1 GND BUS		
57	RED		WCHK-	P2-28	P1-W		
58	WHT		GND	P2 GND BUS	P1 GND BUS		
59	RED		WPS	P2-29	P1-P		
60	WHT		GND	P2 GND BUS	P1 GND BUS		
61	RED		ATTENT0-	P2-30	P1-CC		
62	WHT		GND	P2 GND BUS	P1 GND BUS		
63	RED		ATTENT1-	P2-31	P1-DD		
64	WHT		GND	P2 GND BUS	P1 GND BUS		
65	RED		ATTENT2-	P2-32	P1-EE		
66	WHT		GND	P2 GND BUS	P1 GND BUS		
67	RED		ATTENT3-	P2-33	P1-FF		
68	WHT		GND	P2 GND BUS	P1 GND BUS		
69	RED		WPI	P2-B	P1-H		
70	WHT		GND	P2 GND BUS	P1 GND BUS		
71	RED		LOGADINTL	P2-C	P1-Y	T P	
72	EXST CABLE WHT TEFLON	AR	GND	P2 GND BUS	P1 GND BUS	T P	8



WIRE NO.	DESCRIPTION	TOTAL LENGTH	SIGNATURE	COMPONENT CONNECTION FOR START STATION	COMPONENT CONNECTION FOR FINISH STATION	REMARKS	N/A LM ITEM NO.
73	EXST /ABLE RED TEFLON AR		SECTION BIT 1	P2-D	P1-C		8
74	WHT		GND	P2GND BUS	P1GND BUS		
75	RED		SECTION BIT 2	P2-E	P1-J		
76	WHT		GND	P2GND BUS	P1GND BUS		
77	RED		SECTION BIT 4	P2-F	P1-K		
78	WHT		GND	P2GND BUS	P1GND BUS		
79	RED		SECTION BIT 8	P2-H	P1-N		
80	WHT		GND	P2GND BUS	P1GND BUS		
81	RED		SECTION BIT 16	P2-K	P1-V		
82	WHT		GND	P2GND BUS	P1GND BUS		
83	RED		RESTRI LINE -	P2-M	P1-Z		
84	WHT		GND	P2GND BUS	P1GND BUS		
85	RED		DS-	P2-35	P1-AA		
86	EXST /ABLE WHT TEFLON AR		GND	P2GND BUS	P1GND BUS		8

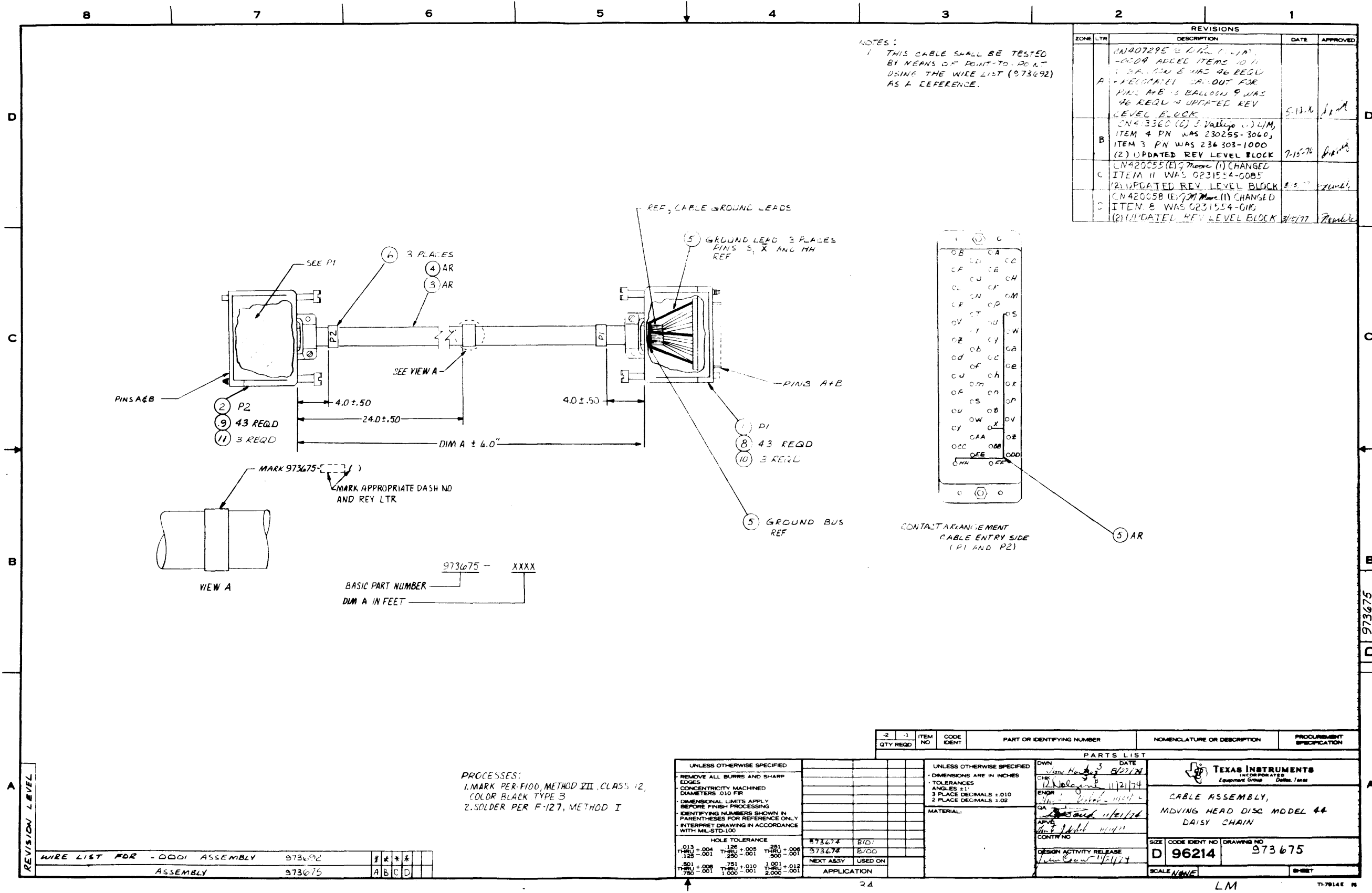
VBI/ELIA

TEXAS INSTRUMENTS
 12000 GREENLEAF DRIVE
 DALLAS, TEXAS 75243-9720

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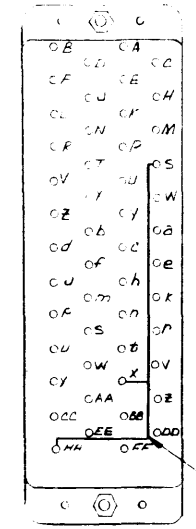
SHEET 5
 973691

REV



NOTES:
 1. THIS CABLE SHALL BE TESTED BY MEANS OF POINT-TO-POINT USING THE WIRE LIST (973692) AS A REFERENCE.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		UN407295 (1) LJM, -0004 ADDED ITEMS 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100	5-13-76	JLM
B		UN43360 (1) J. Vallejo (1) LJM, ITEM 4 PN WAS 230255-3060, ITEM 3 PN WAS 236303-1000 (2) UPDATED REV LEVEL BLOCK	7-15-76	JLM
C		UN420055 (1) J. Vallejo (1) CHANGED ITEM 11 WAS 0231554-0085 (2) UPDATED REV LEVEL BLOCK	8-5-77	JLM
D		UN420058 (1) J. Vallejo (1) CHANGED ITEM 8 WAS 0231554-0101 (2) UPDATED REV LEVEL BLOCK	8/15/77	JLM



REVISION LEVEL			
WIRE LIST FOR	ASSEMBLY	973692	973675

PROCESSES:
 1. MARK PER F100, METHOD VII, CLASS 12, COLOR BLACK TYPE 3
 2. SOLDER PER F-127, METHOD I

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

Change 1

6-97/6-98

Digital Systems Division



TEXAS INSTRUMENTS
INCORPORATED

DATE 03/10/77

LIST OF MATERIAL

PAGE 1 of

PART NUMBER	REV
LM 0973675-0004	D



ITEM NUMBER	QUANTITY PER ASSEMBLY	UNIT OF MEAS	DWG. SIZE	PART NUMBER	DESCRIPTION	VENDOR PART NUMBER	
0001	00001.000	EA		0973697-0002	CONNECTOR, PLUG, 50 PIN		
0001A					P1		
0002	00001.000	EA		0973697-0001	CONNECTOR, SOCKET, 50 PIN		
0002A					P2		
0003	00004.000	FT		0972435-0007	INSUL SLEEVING, 1.0" ID ZIPPER TUBE PVC	ZIP - ZTR-1000-63-2	
0004	00030.000	FT		0772970-0005	CABLE, ELEC, FLAT (ST-1426-19B-XL)		
0005	00001.000	FT		0411400-0016	WIRE, 16AWG, SOLID, UNINSULATED		
0006	00003.000	EA		0418201-0060	STRAP, MARKER, ADJUSTABLE, PLASTIC	QPL-MS-3368-1-98	
0007	REF	EA		0973652-9901	WIRE LIST, MHD44 DAISY CHAIN CABLE ASSY		
0008	00043.000	EA		0411377-0006	CONTACT #24-28 ELECTRICAL MALE	1-00-1024P	
0009	00043.000	EA		0411378-0004	CONTACT ELECT FEMALE	GE -11637	
0010	00003.000	EA		0418722-0002	CONTACT PIN, CRIMP, REMOVABLE SIZE 16 & 20 MIL	-MS17803-16-16	
0011	00003.000	EA		0972739-0002	CONTACT #16 13 AMP SOCKET, CONNECTOR	006779-100-1016S	
DRAFTSMAN		DATE	CKD. DRAFTSMAN	DATE	DESIGN ENGINEER	DATE	TITLE
			<i>[Signature]</i>	3-11-77			CABLE ASSY, DAISY CHAIN, MHD44
APPD.-MFG.		DATE	APPD. PROJECT ENGINEER	DATE	RELEASED	DATE	PROJECT NO.
							5101
							PART NUMBER
							LM 0973675-0004
							REV
							D



ALPHABETICAL INDEX



ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as “Section x” with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as “Appendix y” with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word “See” followed by the referenced entry.



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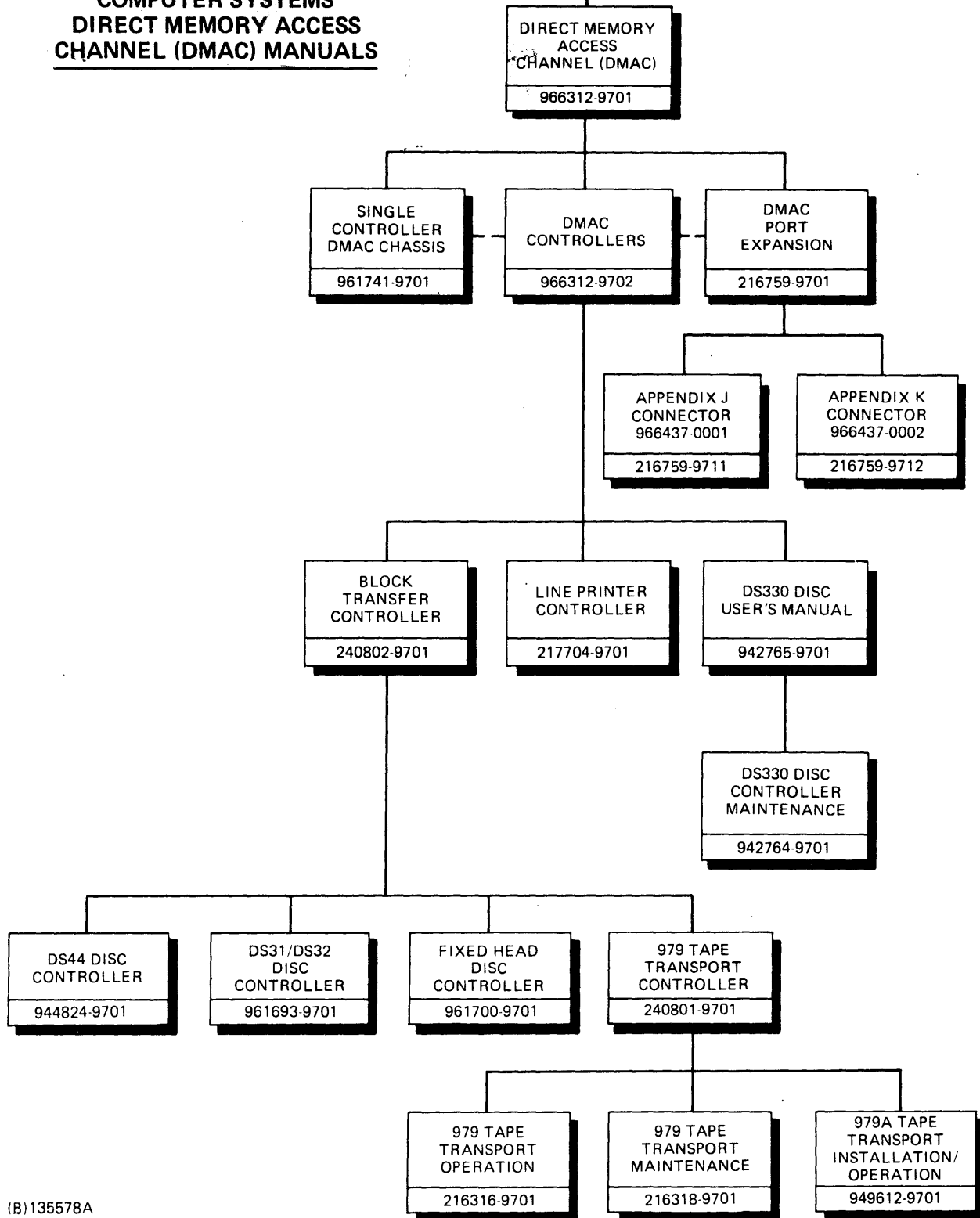
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