TeleVideo®
TS 806, TS 806C, TS 806H, TS 806/20 and TS 806H/20 Maintenance Manual

TeleVideo Systems, Inc.

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TS 806, TS 806C, TS 806H, TS 806/20 and TS 806H/20 Maintenance Manual

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PREFACE

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TS-806 THEORY OF OPERATION

This theory of operation describes the hardware layout, functions and operations.

TABLE OF CONTENTS

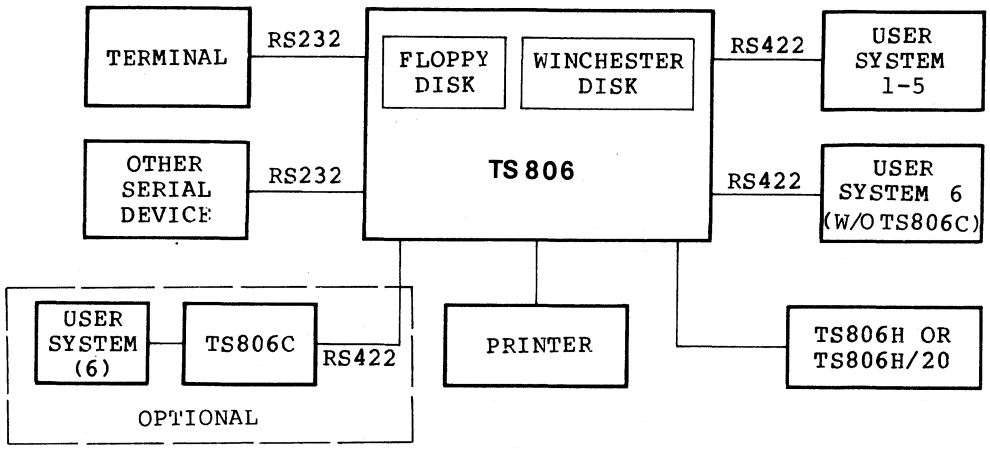
1. INTRODUCTION

The TS-806 is a multi-user system that supports up to 6 user stations. The user stations may be configured from TS-800, TS-801, or TS802-series systems.

The TS-806 is a single board microcomputer based on the Z80A family of microprocessor components. The system functions a central resource manager in a multi-user environment through RS-422 SDLC control. The terminal used with the TS-806 is a standard TeleVideo terminal used as a service terminal.

The TS806 contains a 10-megabyte Winchester technology hard disk drive. The TS806/20 uses a 20-megabyte Winchester drive in the same style cabinet as the TS806. Both systems use the WD-1000 disk interface board. The TS806 can be expanded with the TS-806H, and the TS806/20 is expanded with the TS806H/20.

The TS806C is a magnetic cartridge option to the TS806-series systems. The TS806C is interfaced to the TS806-series system through one of the RS-422 high speed serial data links used for a user station. A user station can be connected to the TS806C as shown in the block diagram to allow the full compliment of 6 stations.



2. GENERAL DESCRIPTION

a. Z80A-CPU

The main processing unit in the system (4.0 MHz operation).

b. Z80A-CTC

Counter/timer chip, generating the baud rate for RS232C serial channel.

c. Z80A-PIO

Parallel I/O chip, provides centronics-type printer interface.

d. Z80A-SIO

Serial I/O chips, providing RS232C interface (data rate to 19.2 KB) and/or RS422 high-speed serial interface with data rate of 800K bit/sec.

e. Z80A-DMA

Direct memory access controller chip is used for direct transfer of data between memory and peripheral I/O like floppy disk, Winchester hard disk, etc.

f. Memory

Main memory available to user is 64K bytes, using 64K X 1 DRAM 4K bytes of ROM and 1K byte of SRAM are used for system firmware (used on power up or reset only).

g. Floppy disk controller

Western Digital's FD 1793 chip along with its support chips WD 2143-01 and WD1691 provides control and interface to the 5 ¼" floppy drive.

h. Winchester hard disk interface

Interface is provided to the disk controller board for the 5 ¼" hard disk.

3. FUNCTION

The facilities available to the users are 64K bytes of main memory, floppy disk controller which can drive potentially up to 4 drives (0.5M byte each), interface to communicate with the hard disk controller which can also drive potentially up to 4 hard disk drives 5 ¼" Winchester, and parallel port for high-speed centronics-type printer interface.

2 channels of RS232C type interface (from 1 SIO), and 6 channels of RS422 interface (from the other 3 SIO's) to communicate with the user systems (TS-800, TS-801) are provided.

4K bytes of ROM and 1K bytes of SRAM are used for system initialization, diagnostics, boot, and floppy/hard disk control during the power-up or reset, and are not accessible by the users. After the initial program in the ROM is run upon power-up or reset, the dynamic memory area (address 00-16 K hex.) is switched on so that the whole 64K byte of main memory can be used by the user.

TS-806 uses a DMA controller to transfer data between memory and I/O devices, memory to memory, and also I/O device to I/O device.

A CTC chip (A40) is reserved to provide vectored interrupt capability. Another CTC chip (A39) generates (switch-selectable) baud rates for RS232C interface. 2 Channels of this CTC are reserved for time-of-day generation as a user implemented option.

4 LED indicators are used for diagnostic purposes to indicate faults in the hardware.

The system block diagram is shown in Figure 2, I/O port assignment is shown in Table 1 and the baud rate switch configuration is shown in Table 2.

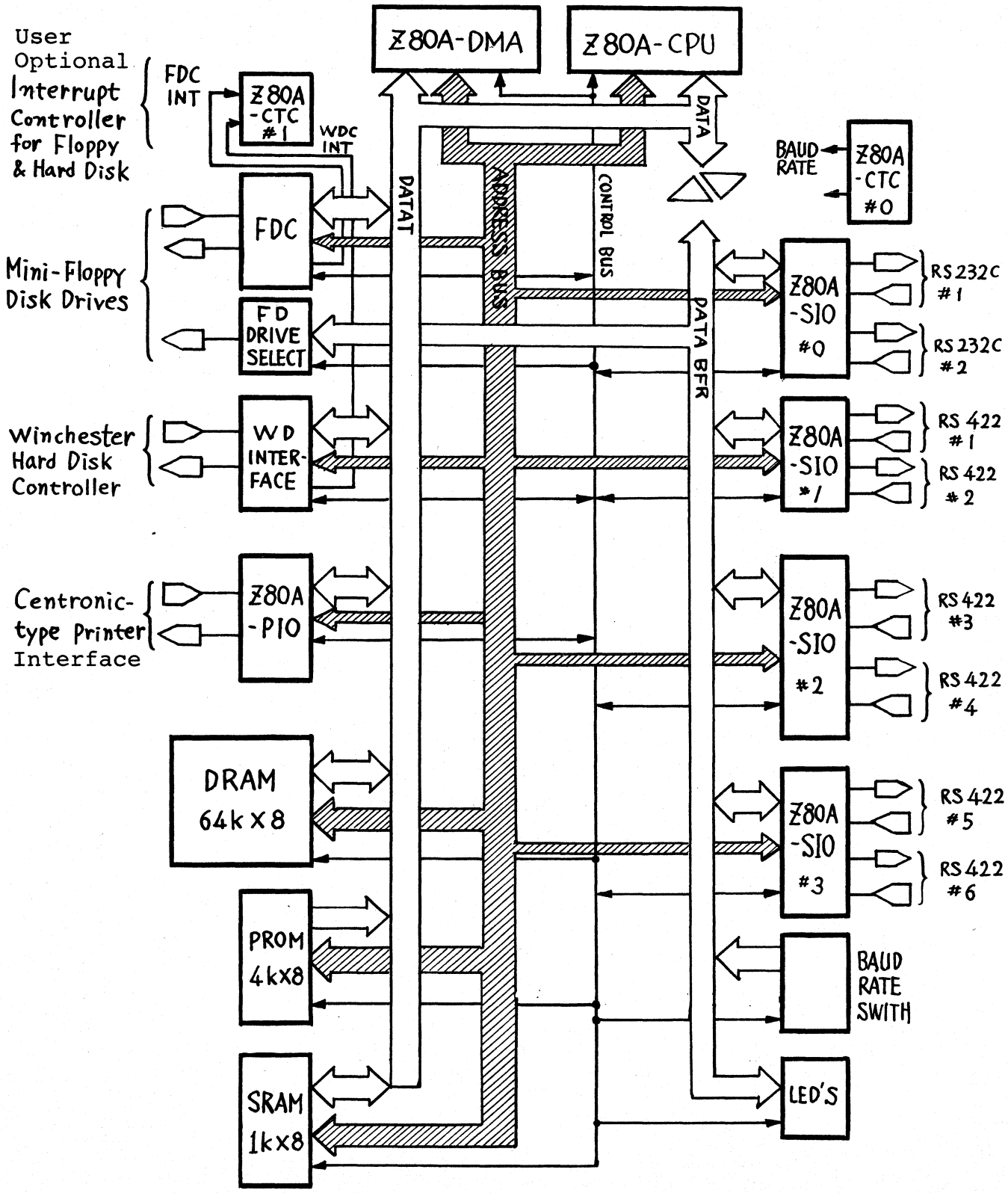


DIAGRAM 2 - BLOCK DESIGN OF TS-806

ABUS BIT #								I/O PORT	
7	6	5	4	3	2	1	0	HEX.	
0	0	0	0	0	X	X	X	00	Indicator Load (LED Ref.)
0	0	0	1	0	X	0	0	10	SIO 1, Ch A Data Reg.
						1	0	12	Com/Stat Reg
						0	1	11	Ch B Data Reg.
						1	1	13	Com/Stat Reg
0	0	1	0	0	X	0	0	20	SIO 2, Ch A Data Reg.
						1	0	22	Com/Stat Reg
						0	1	21	Ch B Data Reg.
						1	1	23	Com/Stat Reg
0	0	1	1	0	X	0	0	30	SIO 3, Ch A Data Reg.
						1	0	32	Com/Stat Reg
						0	1	31	Ch B Data Reg.
						1	1	33	Com/Stat Reg
0	1	0	0	0	X	X	X	40	WDC Reset (Winchester Disk Soft Reset)
0	1	0	1	0	X	0	0	50	SIO 0, Ch A Data Reg.
						1	0	52	Com/Stat Reg
						0	1	51	Ch B Data Reg.
						1	1	53	Com/Stat Reg
0	1	1	0	0	X	X	X	60	Baud Rate Load
0	1	1	1	0	X	X	X	70	FDD Select
1	0	0	0	0	X	0	0	80	CTC Ch 0
						0	1	81	Ch 1
						1	0	82	Ch 2
						1	1	83	Ch 3
1	0	0	1	0	X	X	X	90	DMA
1	0	1	0	0	0	0	0	A0	WDC Reg. 0 Data Reg.
					0	0	1	A1	Reg. 1 Error/Write Precompensation Reg.
					0	1	0	A2	Reg. 2 Sector Count Reg.
					0	1	1	A3	Reg. 3 Sector Number Reg.
					1	0	0	A4	Reg. 4 Cylinder Low Reg.
					1	0	1	A5	Reg. 5 Cylinder High Reg.
					1	1	0	A6	Reg. 6 Size/Drive/Head Reg.
					1	1	1	A7	Reg. 7 Status/Command Reg.

ABUS BIT #									I/O PORT
7	6	5	4	3	2	1		HEX.	
1	0	1	1	0	X	0	0	B0	FDC Com/Stat Reg.
						0	1	B1	Track Reg.
						1	0	B2	Sector Reg.
						1	1	B3	Data Reg.
1	1	0	0	0	X	0	0	C0	PIC Ch 0 (CTC) User Option
						0	1	C1	Ch 1
						1	0	C2	Ch 2
						1	1	C3	Ch 3
1	1	0	1	0	X	0	0	D0	PIO Ch A Data Reg.
						1	0	D2	Com/Stat Reg
						0	1	D1	Ch B Data Reg.
						1	1	D3	Com/Stat Reg
1	1	1	0	0	X	X	X	E0	Enable Dram
1	1	1	1	0	X	X	X	F0	Disable Dram

Table 1. I/O Port Assignment

Baud Rate Generation for SIO:

Switches for baud rates are upper 4 dip switches which can be set up as following table.

Baud Rate	Switch Pos. 4	3	2	1
19.2 KBaud	0	0	0	0
9.6 KBaud	0	0	0	1
4.8 KBaud	0	0	1	0
2.4 KBaud	0	0	1	1
1.2 KBaud	0	1	0	0
600 Baud	0	1	0	1
300 Baud	0	1	1	0
150 Baud	0	1	1	1
75 Baud	1	0	0	0

Table 2. Baud Rate Switch

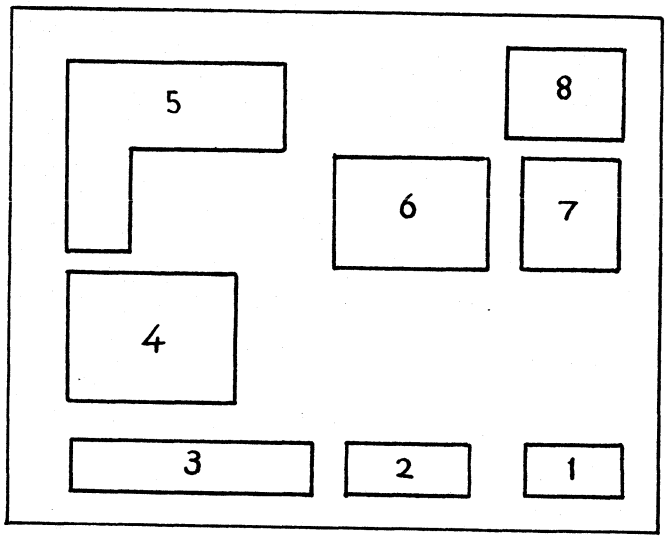
Dip Switch Description:

0 (Close) / 1 (Open)

SW 1: Baud Rate
2: "
3: "
4: "
5: Unused
6: Unused
7: Unused
8: Reserved for Diagnostic

4. Circuit Description

Generally TS-806 circuitry can be divided into 8 sections as shown in Figure 3.



1. Reset
2. Clock
3. Memory
4. CPU & DMA
5. Serial I/O
6. Floppy Disk Control
7. Hard Disk Controller
8. Printer Interface

Figure 3 System Board Description

4.1 Reset

The chip associated with the reset circuit is a 74LS00 (A2), which debounces the reset signal when the reset switch is pressed.

A2-13 is normally low and Pin 1 is normally high. -Reset must be active for at least three clock cycles to properly reset the CPU. As long as -Reset remains active, the address and data bus float, and the control signal outputs are inactive.

The CPU returns to normal operation after two internal "T" cycles. -Reset clears the PC register so the register now contains a value of 0000.

4.2 Clock Generation

16 MHz signal from the oscillator (OSC) is divided down to a 4 MHz signal using a 93S16 (A7) and TR 2N2907 is used to drive the proper system clock level and again buffered for enough driving current.

The 1 MHz clock from the 93S16 is supplied to the floppy disk controller chip (FD 1793). To generate the baud rate, the 8 MHz signal from the 93S16 is fed into a 74LS163 (A8), to generate the frequency of 1/6.5 times the system clock for the CTC. Transmit clock for the SIO (RS422) is generated through another 74LS163 (A38) and 74S04 (A23) using system clock.

4.3 Memory

ROM and Static RAM:

A single 4K X 8 ROM and two 1K X 4 SRAM are used. ROM and SRAM are enabled upon power-up or reset. The enabling circuitry is composed of two 74LS138 (A21, A22) and other necessary chips of flip-flop and gates. By issuing an I/O instruction, we can either enable or disable the ROM and SRAM. When the ROM and SRAM are enabled, -CAS signal for dynamic RAM column address goes inactive disabling dynamic RAM (00H-16KH), so only ROM and SRAM are active. During read/write operations involving ROM and SRAM the 74LS74 (A36) generates one wait state to allow sufficient time for the read/write operation.

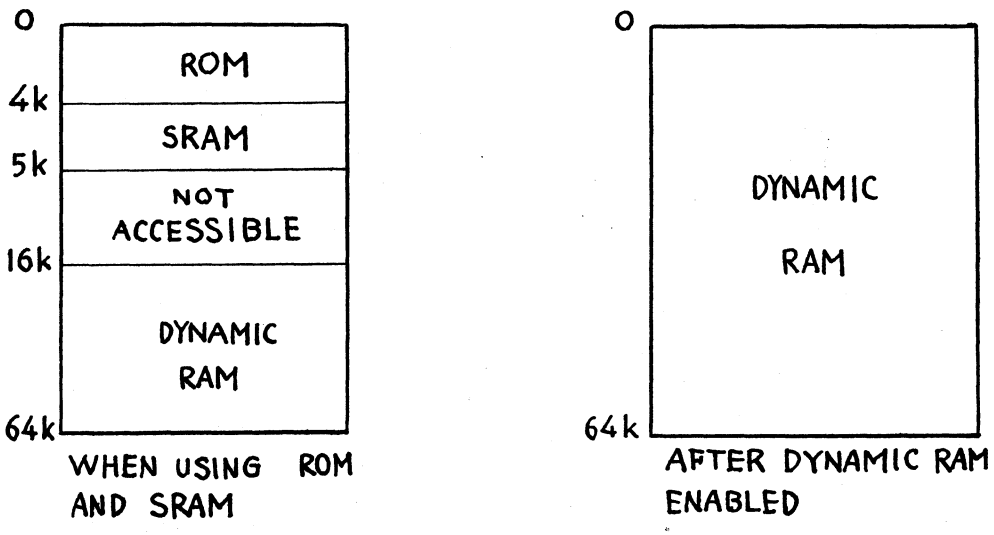


Figure 4 Memory Space Description

4.3 Eight DRAM chips (64Kb each) are used for main memory. Two 74S74 (A35,A37) and other related chips (A18, A19) are used to generate -CAS and -RAS signals using -M1 and -MREQ signals. Select column signal chooses either A0-A7 or A8-A15 as row and column address. As explained previously, when dynamic RAM is enabled it activiates -CAS signal so that all DRAM locations can be accessed by the user. During refresh, only -RAS signal is activated and one whole row is refreshed at one time.

The following diagrams show the timing of those signals.

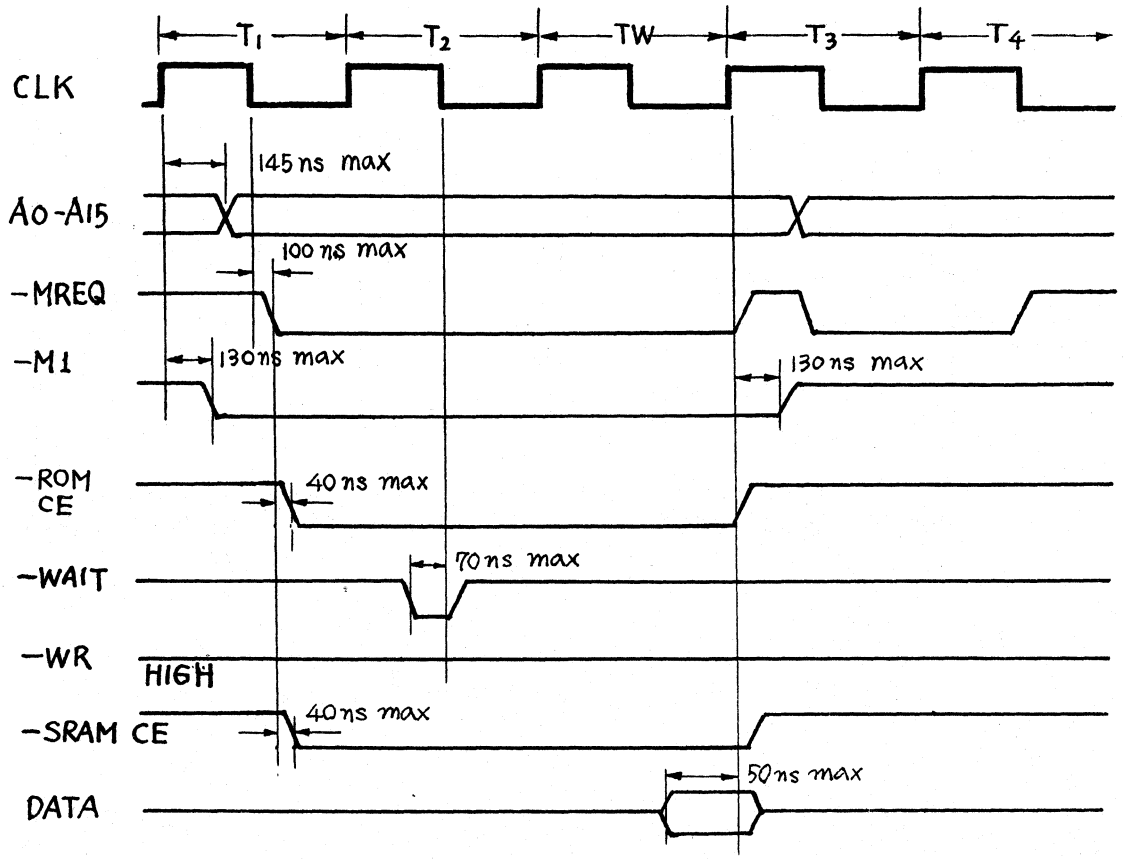


Figure 5 Instruction Fetch from ROM/SRAM

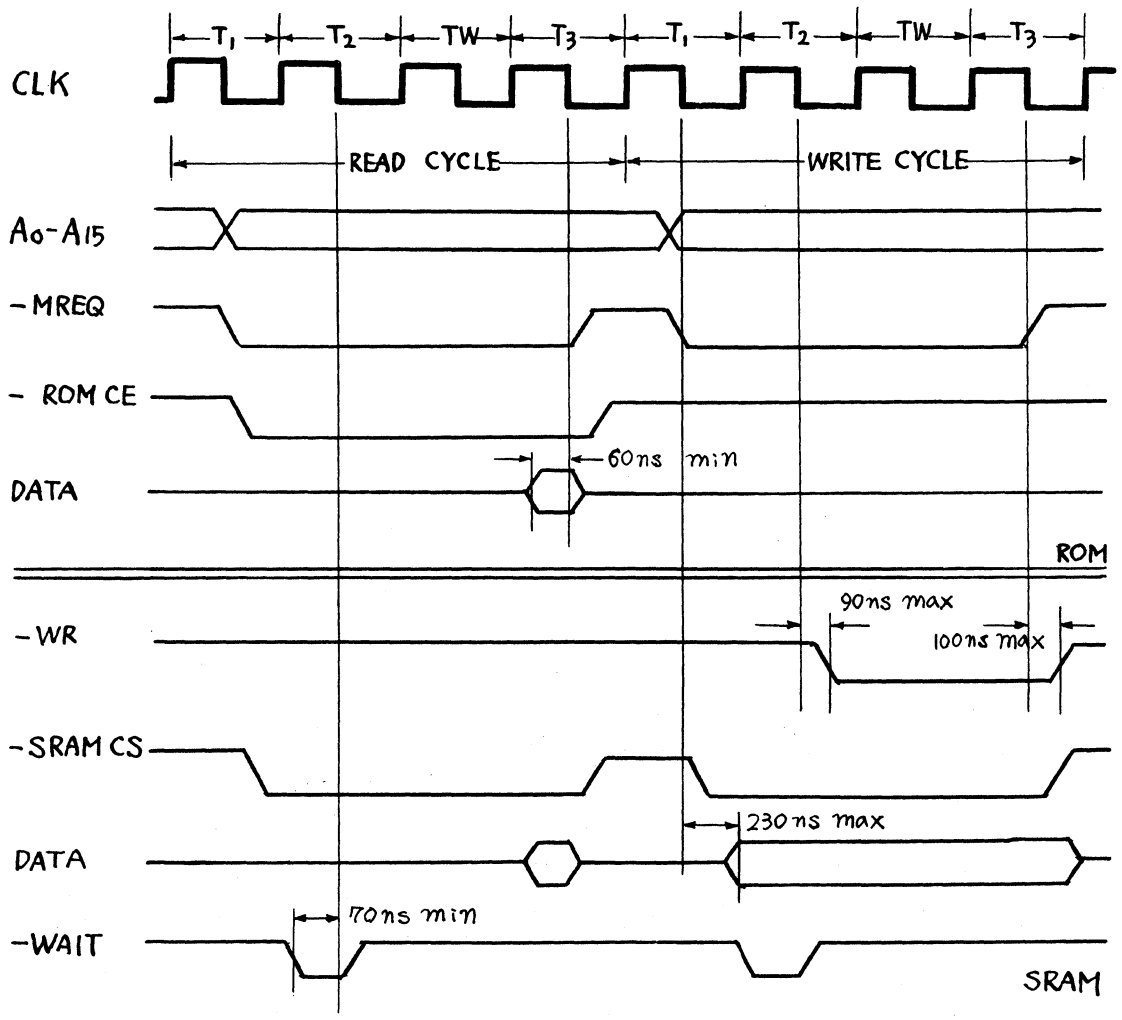


Figure 6 Read/Write on ROM and SRAM

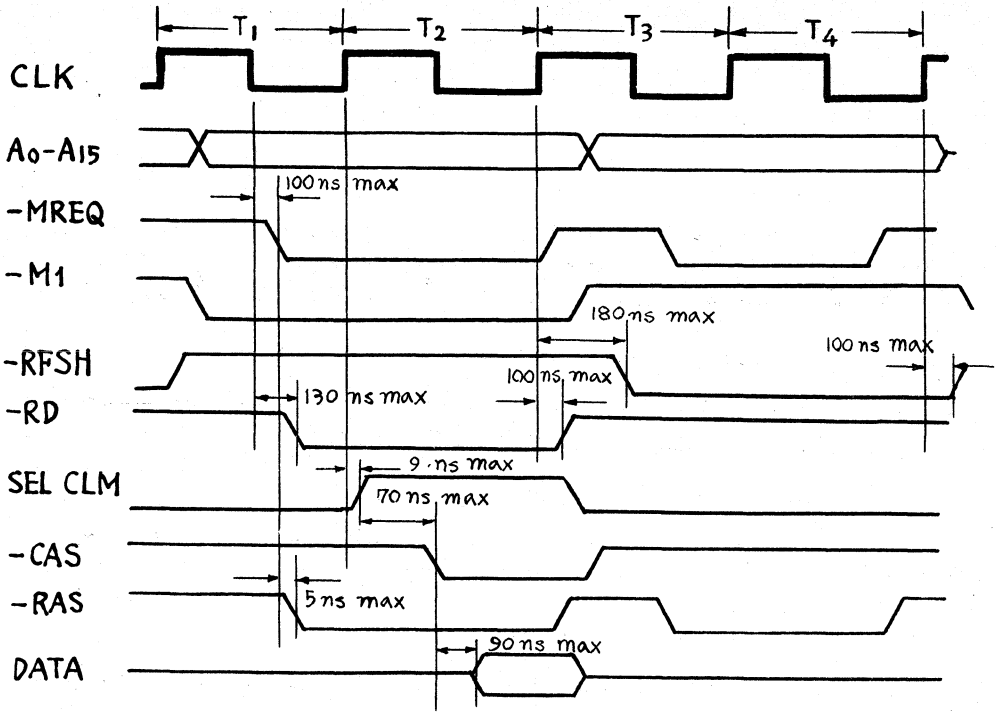


Figure 7 Instruction Fetch from DRAM

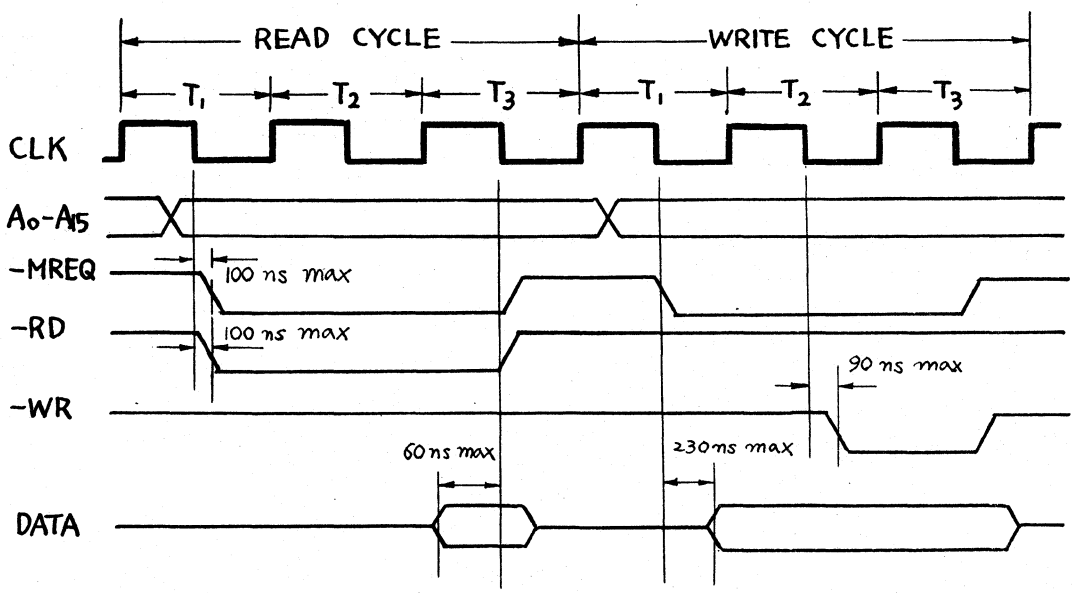


Figure 8 Read/Write from DRAM without Wait States

4.4 DMA Operation

The RDY line is monitored by the DMA to determine when a peripheral device is ready for read or write operation. When the DMA is enabled the RDY line indirectly controls DMA activity. -BUSREQ is used as output from the DMA chip to request for control of the address, data and control bus from the CPU. If CPU receives active -BUSREQ, the CPU will set these buses to high impedance state as soon as the current CPU machine cycle is terminated, and then sends out -BUSAK signal to indicate that DMA can control these signals.

Figure 9 illustrates the -BUSREQ and -BUSAK (BAI) timing. The RDY line is sampled on every rising edge of CLK as a level, not an edge. When the DMA detects a low on -BAI line for two consecutive rising edges of CLK, the DMA begins transferring data on the next rising edge of CLK.

Figure 10 and Figure 11 explain the timing diagram of RDY line in burst mode and in continuous mode of the DMA.

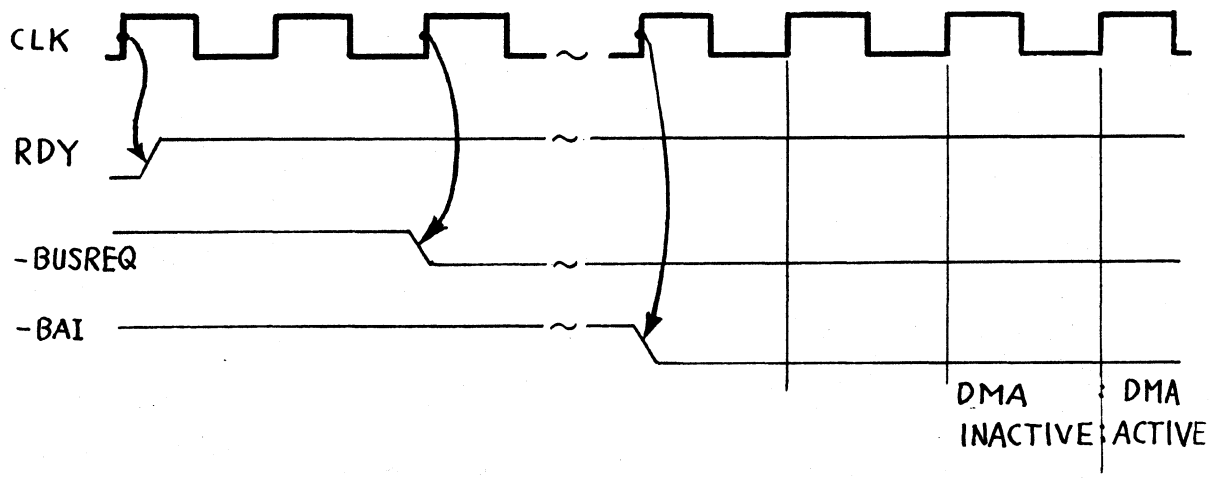


Figure 9 Bus Request and Acceptance Timing

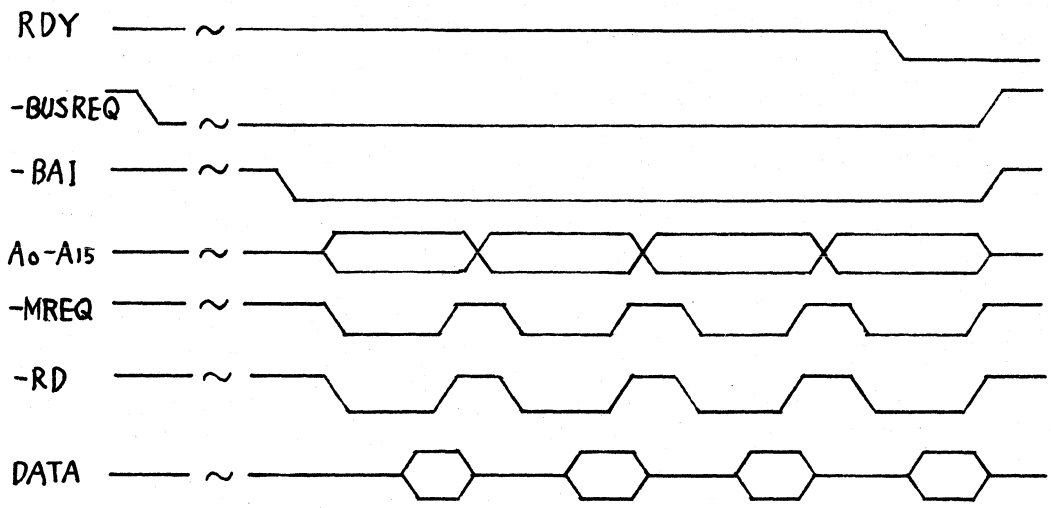


Figure 10 RDY Line in Burst Mode

(Refer to I/O Operation for precise timing.)

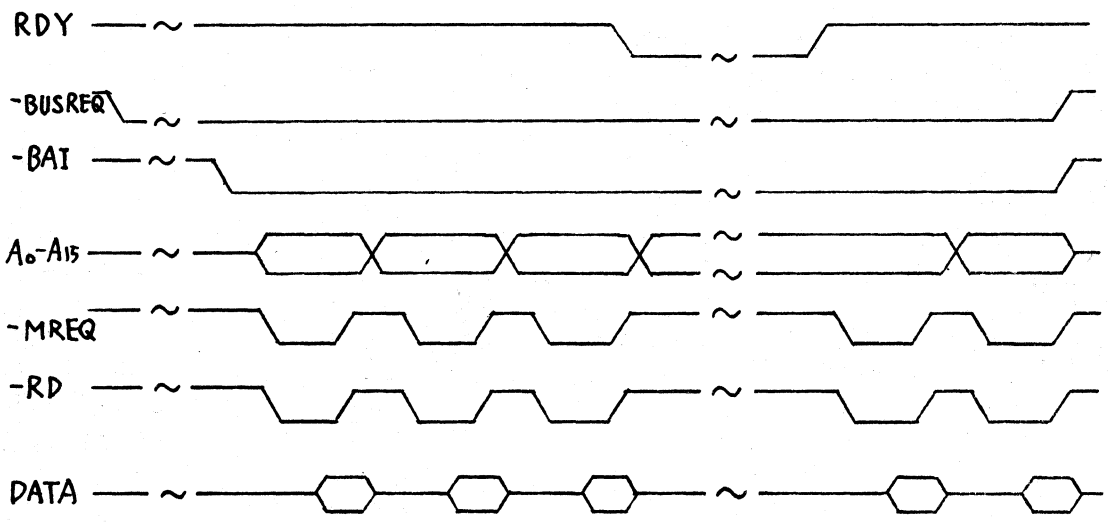


Figure 11 RDY Line in Continuous Mode

(Refer to I/O Operation for precise timing)

4.5 I/O Operation

The Z80A CPU can address up to 256 I/O ports. The CPU uses only the lower 8 address lines for I/O addressing. The address lines A3 to A7 are decoded through two 74LS138 (A58,59). For I/O read/write, the -IORQ signal "NANDED" with RD/WR is used to provide -IORD/-IOWR signal. During the I/O operation, the CPU automatically inserts a single wait state (TW). This extra wait state allows sufficient time for an I/O port to complete a read/write operation.

One SIO (A82) is for RS232 interfaces and its related chips are 75188 (for output) and 75189 (for input). The other 3 SIO's (A61, A83, A84) are for RS422 interfaces with the user system; the related chips are 26LS31 (for output) and 26LS32 (for input). The timing of the signals generated by the CPU input instruction (to read data or the status byte) and output instruction (to write data or control bytes) are illustrated in Figure 12.

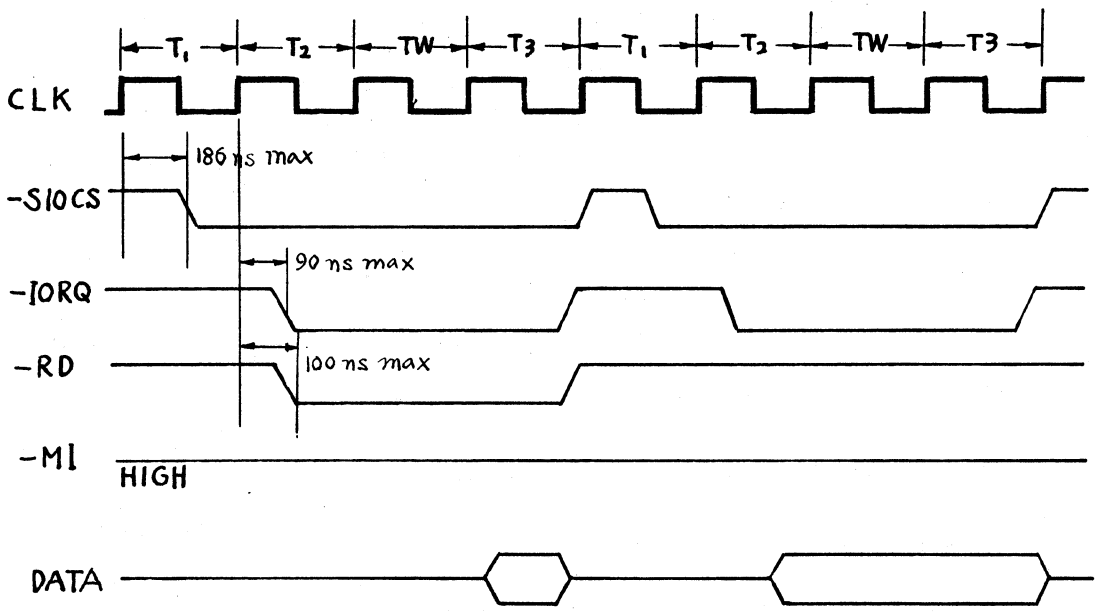


Figure 12 Timing Diagram for Read/Write Through SIO

4.5 I/O Operation

FD 1793, WD1691, WD2143-01 and other related chips are used for floppy disk control. FD 1793 has two modes of operation according to the state of -DDEN (Pin 37). When -DDEN=1, single density is selected. The CLK input (Pin 24) is set at 1 MHz for mini floppy. DRQ line indicates that the data register contains assembled data in the read operation, or the data register is empty in the write operation. This signal is reset when serviced by the system through reading or loading the data register.

Figure 13 and 14 show timing diagram of those related signals.

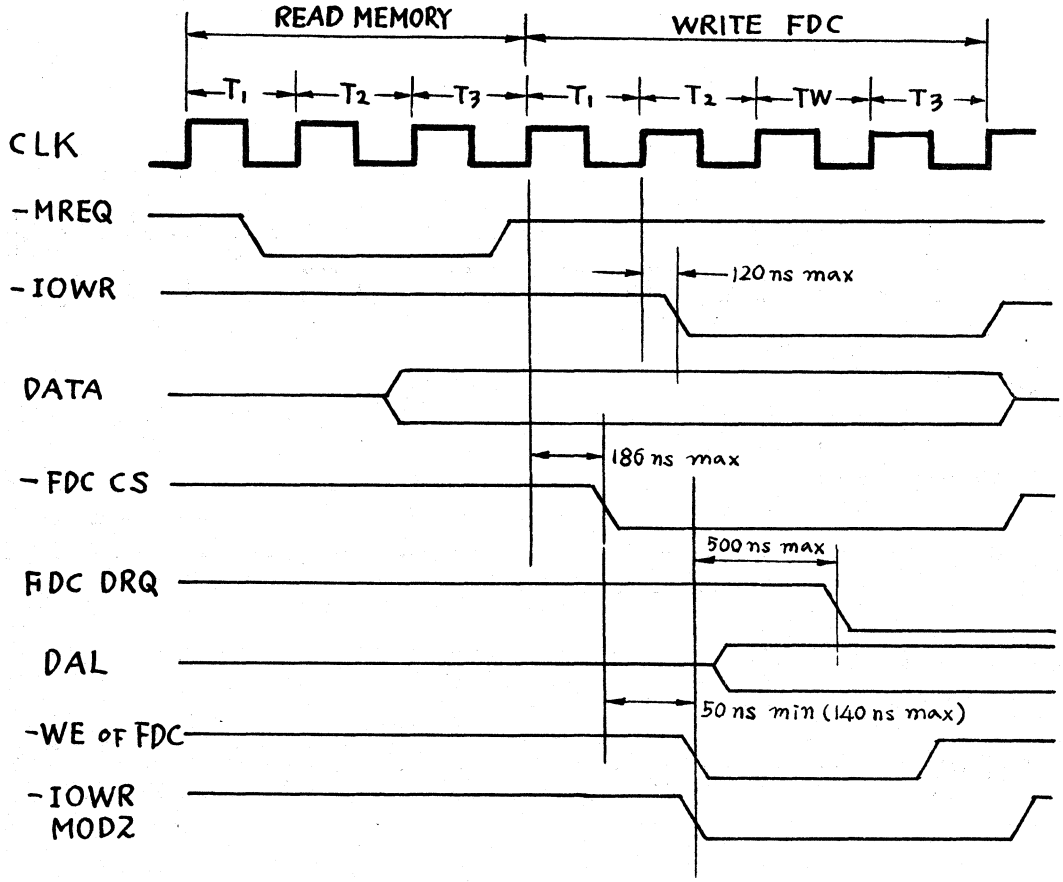


Figure 13 Timing Diagram of Memory to FDC Transfer (DMA Write Operation)

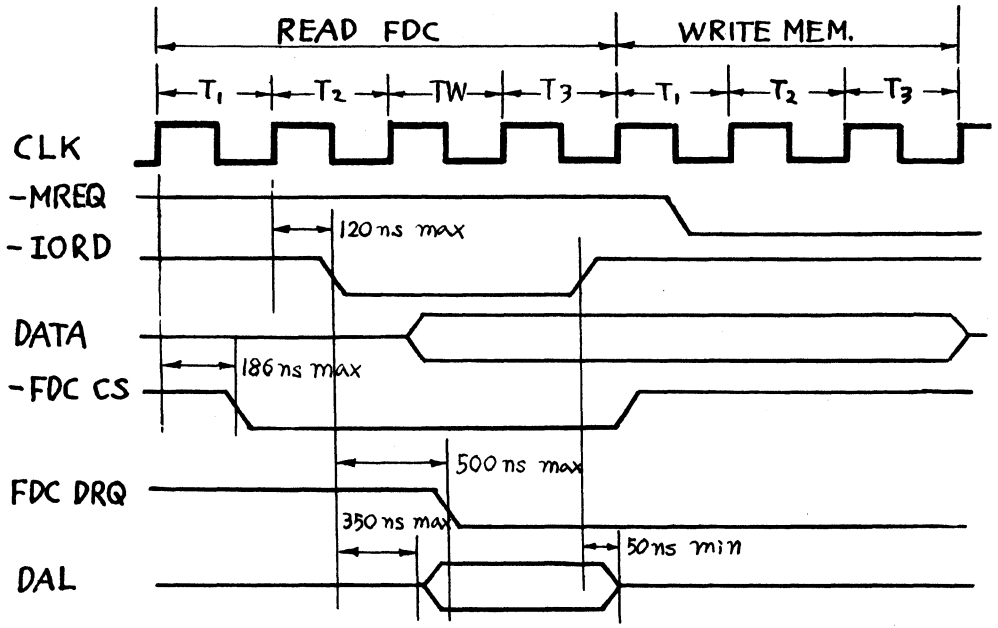


Figure 14 Timing Diagram of FDC to Memory Transfer (DMA read operation)

WD 1000 controller board is used for 5¼" Winchester disk interface. As with the floppy disk controller, -WDC DRQ signal is used to control the RDY line of DMA by being "NANDED" with other I/O RDY signals through 74S133 (A71). -IORD signal decides the direction of data on 74LS245 (A91) between the system and controller. Figure 15 and 16 shows the timing diagram in WDC read/write operation using DMA.

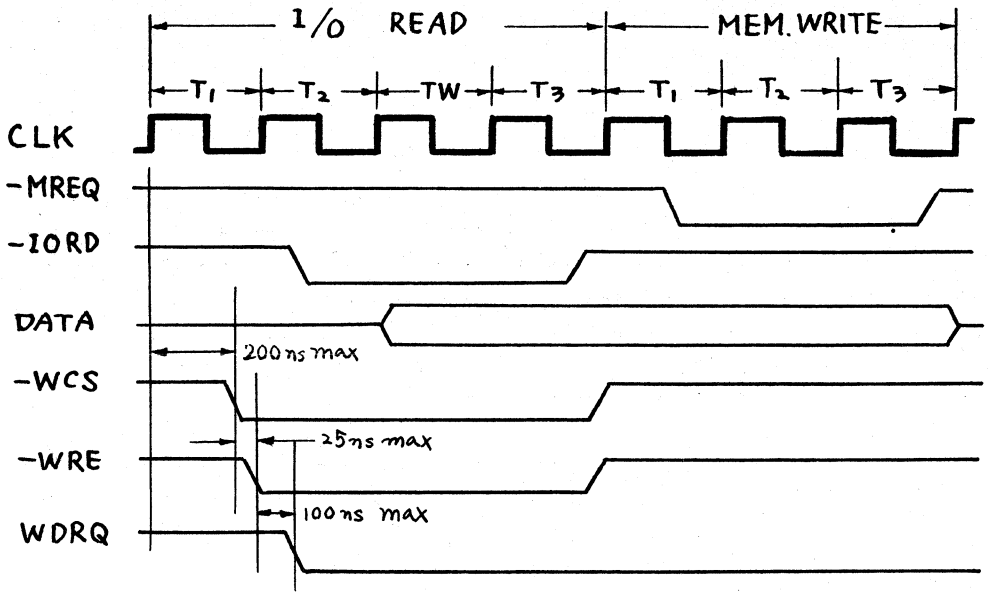


Figure 15 WDC To Memory Transfer
(DMA Read Operation)

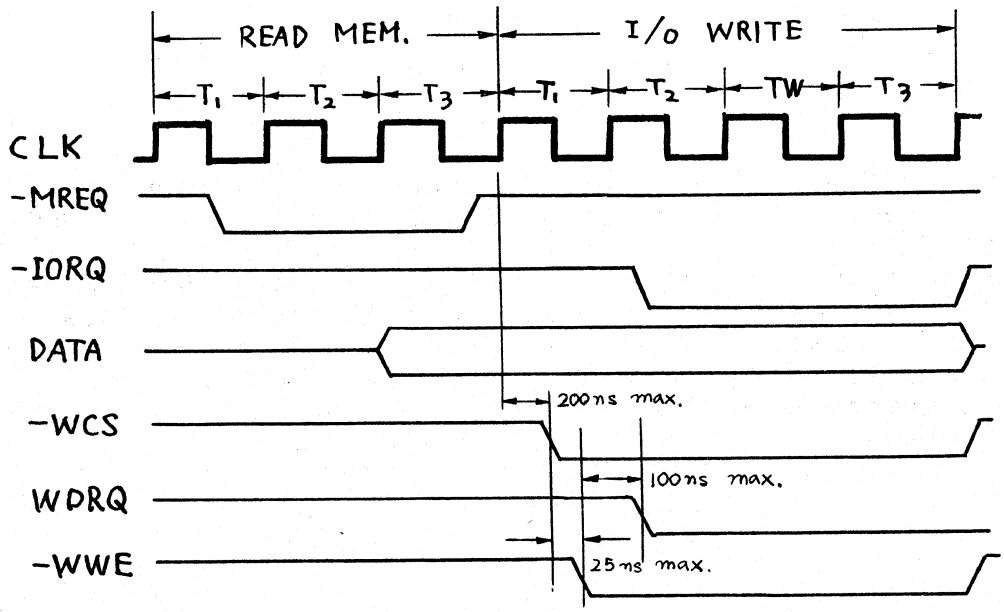


Figure 16 Memory to WDC Transfer
(DMA Write Operation)

5. Connector Description

All the connector position is shown in Figure 17 and Table 3.

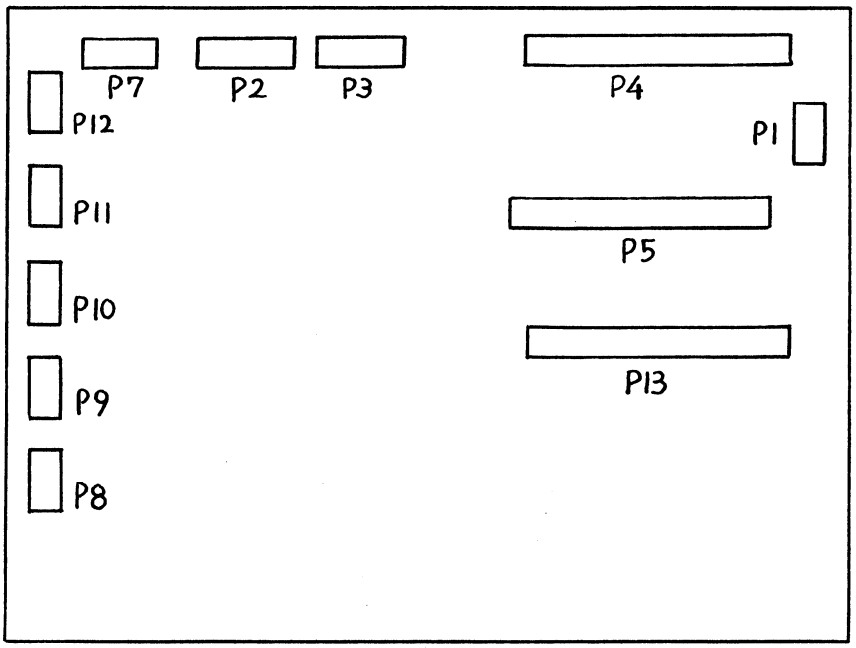


Figure 17 Connectors on the board

Connector #	Description
P1	Power
P2	RS232C Service Terminal Interface
P3	RS232C Serial Interface
P4	Centronics-type Printer Interface
P5	Winchester Disk Controller Interface
P6	Reset, Power On Light
P7	RS422 User Channel 1
P8	RS422 User Channel 2
P9	RS422 User Channel 3
P10	RS422 User Channel 4
P11	RS422 User Channel 5
P12	RS422 User Channel 6
P13	Floppy Disk Drive Interface

Table 3. Connector Assignment

5.1 Power Connector (P1: 5 Pin)

Pin No.	Description
1	-12 V
2	Unused
3	GND
4	+5 V
5	+12 V

Table 4 Power Connector Configuration

5.2 RS232C Connector (P2,3: 25 Pin)

Pin No.	Description (DCE P3)
1	Frame Ground
2	Transmit Data (Receive Data P3)
3	Receive Data (Transmit Data P3)
4	Request to Send
5	Clear to Send
7	Signal Ground
8	Data Carrier Detect
20	Data Terminal Ready (Printer Busy P3)

Polarity of Data Signals: - True
Polarity of Control Signals: + True

Table 5 RS232C Connector Configuration

5.3 Floppy Disk Controller Connector

Pin No.	Description
6	-Drive Select 3
8	-Index/Sector
10	-Drive Select 0
12	-Drive Select 1
14	-Drive Select 2
16	-Motor On
18	-Direction Select: - Toward Center + Off Center
20	-Step
22	-Composite Write Data
24	-Write Enable
26	-Track 00
28	-Write Protected
30	-Composite Read Data
32	-Side 1 Select (Ignored by one side floppy disk drive)

Pin 1, 2, 3, 4, and 34 are not used.
All other odd number pins are grounded.

Table 6. FDC Connector Configuration

5.4 Winchester Hard Disk Controller Interface Connector (P5: 40 Pin)

Pin No.	Description
1	WDAL 0
3	WDAL 1
5	WDAL 2
7	WDAL 3
9	WDAL 4
11	WDAL 5
13	WDAL 6
15	WDAL 7
17	WA 0
19	WA 1
21	WA 2
23	-WCS (Winchester Chip Select)
25	-WWE (Winchester Read Enable)
27	-WWAIT
29	WINTRQ (Interrupt Request)
35	WDRQ (Data Request)
37	-WMR (Master Reset)
39	

Pin 31, 33 are not used.
All even number pins are grounded.

Table 7. WDC Connector Configuration

5.5 Centronics-type Printer Interface Connector (P4: 40 Pin)

40 pin right angle header is used on the board, so the pin configuration on the board is different from the 36 pin connector on the rear panel but it will be matched when they are connected together.

Refer to Figure 18 for comparison of two connector pin assignment between 40 pin connector on the board and 36 pin connector on the rear panel which will be hooked up to the printer.

Table 8 describes the pin configuration of the connector on the board.

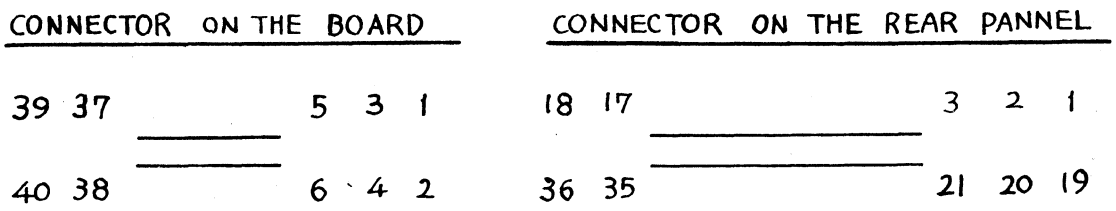


Figure 18. Comparison of Two Connectors for Printer

Pin No.					Description	
Rear Panel Connector	Board	Port/Data Bit				
1, 19*	1, 2*	DØ/Ø			-Data strobe	Output
2, 20	3, 4*	D1/Ø			Data 0	Output
3, 21*	5, 6*	D1/1			Data 1	Output
4, 22*	7, 8*	D1/2			Data 2	Output
5, 23*	9, 10*	D1/3			Data 3	Output
6, 24*	11, 12*	D1/4			Data 4	Output
7, 25*	13, 14*	D1/5			Data 5	Output
8, 26*	15, 16*	D1/6			Data 6	Output
9, 27*	17, 18*	D1/7			Data 7	Output
10, 28*	19, 20*	BSTB/P10			-Acknlg	Input
11, 29*	21, 22*	DØ/5			Busy	Input
12	23	DØ/4	(W5)	**	PE (paper empty)	Input
13	25	DØ/6	(W4)	***	Select	Input
31, 30*	26, 24* (W6)	DØ/1	(W8)		-Input Prime	Output
14	27		(W7)		Gnd	
32	28	DØ/3	(W3)	***	-Fault	Input
15	29				Unused	
33	30	DØ/2	(W2)	**	Light Detect	Input
16	31				GND	
34	32	DØ/7	(W9)		LC Pulse	Output
17	33				Gnd	
35	34				Unused	
18	35				Unused	
36	36				Unused	

* Second pin number indicates return ground.

Pin 37, 38, 39, and 40 are not connected.

**Ground if no connection
***Tie high if no connection

Table 8: Configuration of parallel Printer Interface

5.6 User system connector: RS422 (P7: 15 pin, P8-P12: 16 pin)

There are two types of connectors for RS422 on the system board. User 1 connector is D type 15 pin (P7) but from user 2 to user 6 (P8 to P12) connectors are 16 pin header type but these are connected to the D type on the rear panel eventually. The difference is only due to the different numbering order between those two types. Refer to Figure 19 for comparison.

D Type

```
8  7  6  5  4  3  2  1
 15 14 13 12 11 10  9
```

Header Type

```
15  13  11  9  7  5  3  1
16  14  12  10 8  6  4  2
```

Figure 19 Two Different Type Connector Pin Order for RS422

a. P7 (D type: 15 Pin)

Pin No.	Description	Pin No.	Description
1	Shield	9	-TXD
2	TXD	10	-RXD
3	RXD	11	-RTS
4	RTS	12	-CTS
5	CTS	13	TXC
6	-TXC	14	RXC
7	-RXC	15	Reserved for Manufacturer
8	Signal GND		

Table 9. D Type Configuration for RS422

b. P8 to P12 (header type: 16 pin)

Pin No.		Description			Description
"D" Conn.	Board		"D" Conn.	Board	
1	1	Shield	9	2	-TXD
2	3	TXD	10	4	-RXD
3	5	RXD	11	6	-RTS
4	7	RTS	12	8	-CTS
5	9	CTS	13	10	TXC
6	11	-TXC	14	12	RXC
7	13	-RXC	15	14	Unused
8	15	Signal GND	N/C	16	Unused

Table 10. Header Type Configuration for RS422

5.7 Reset Power On Light Connector (P6: 3 Pin)

Pin No.	Description
1	GND
2	Reset SW (normally high)
3	Reset SW (normally low)

Table 11. Reset, Power On Light Connector Configuration

5.8 LED Description

4 LED's are used for diagnostic purposes. They are lit when the data line goes low. The corresponding port address is 00 the data byte assigned to each LED is as follows.

LED No.	Data Byte
1	F0
2	F1
3	F2
4	F3

The LED sequence for each test is as follows:

Lit LED	Test In Process
o o o ● 1	MEM Test
o o ● o 2	DMA
o ● o o 3	WDC
● o o o 4	SIO
o o ● ● 1, 2	PIO
● ● o o 3, 4	FDC
● ● ● ● 1, 2, 3, 4	After finishing all tests

6.0 Description for Jumpers

W1: 1) Connect B and C when used with service terminal.
2) Connect A and B when used without service terminal.

W2-W9: Use as follows depending on the type of printer.

Jumper	Related Signal and Pin No. (Centronics-type) on rear panel	Description
W2	Light detect (pin 33)	Connect when the printer interface does not need this signal.
W3	-Fault (pin 32)	Connect when the printer interface does not need this signal.
W4	Select (pin 13)	Connect when the printer interface does not need this signal.
W5	Paper empty (pin 12)	Connect when the printer interface does not need this signal.
W6	-Input prime return (pin 30)	Connect if GND is needed.
W7	GND (pin 14)	Connect if GND is needed.
W8	-Input prime (pin 31)	Connect when the printer interface needs this signal.
W9	LC pulse (pin 34)	Connect when the printer interface needs this signal.

7.0 POWER REQUIREMENTS

	Sys. Bd	WDC	Hard Disk	Floppy Disk
+5V	5.5 A Max.	2.5 A Max.	1.0 A Max	0.5 A Max.
	2.5 A Typ.	2.1 A Typ.	.75 A Typ.	0.45A Typ.
+12V	80 mA Max.		5.0 A Max.	2.2 A Max.
	50 mA Typ.		1.5 A Typ.	0.8 A Typ.
-12V	50 mA Max.	50 mA Max.		
	30 mA Typ.	25 mA Typ.		

8.0 WINCHESTER DISK CONTROLLER

8.1 Overview

The WD1000 hard disk controller is a discrete implementation of all the functions required to control SA1000/ST506-compatible Winchester (hard) disk drives via a standard data and control BUS. The controller is fabricated using a mix of high-speed bipolar and NMOS devices contained on a single, two-sided PC board.

The design of the circuitry makes use of a high-speed Microcontroller called the 8X300, newly developed NMOS support devices, Schottky devices, and low power Schottky devices. Together they work to achieve low component count and cost while maintaining high performance and reliability.

All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors are provided to permit direct pin-for-pin connection to ST506 compatible 5" drives.

All power for the board can be supplied from a single 5-volt power supply on a separate connector.

All host-to-disk data transfers are buffered by onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around five basic sections:

1. Processor functions
2. Serial data separation
3. Data conversion and checking
4. Serial data generation
5. Host interface functions

8.2 Processor Functions

All functions of the WD1000 controller are ultimately controlled by the onboard processor. Due to the high data rates associated with hard disk drives, processing of data and control of machine functions within the circuitry requires a processor capable of extremely fast execution speed. The processor used is the 8X300, a bipolar microcontroller particularily well suited for handling data efficiently at high rates.

The 8X300 operates at a basic clock rate of 8 MHz and performs all operations within 2 clock cycles giving it a speed of 4 MIPS (Million Instructions Per Second) or one instruction executed

every 250 nS. The architecture of the processor is different from most other microprocessors in that no common data or address BUS is provided to be shared by RAM, ROM or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data BUS. The instruction address BUS (IAO-IA13) is capable of directly accessing 8K words of program storage. However, the WD1000 uses only the first 10 address lines, limiting onboard program storage to 1K words.

Program data is input to the 8X300 (U50) on the Instruction Data Operation. All BUS designations utilized by the 8X300 are reversed from the traditional LSB to MSB weighting. These bus lines have all been renamed on the schematic of the WD1000 to provide a more conventional designation system for the board.

8.2.1 Fast I/O Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast I/O Select" byte is not processed by the 8X300. It is decoded by auxiliary hardware to provide eight read strobes and eight write strobes which route data to the various devices distributed along the interface vector BUS.

The Fast I/O byte is latched into a 6-bit latch (U27) on the trailing edge of MCLK to ensure the data remains stable during the entire instruction. This data selects a read strobe and write strobe through two 1-of-8 decoders (U20 and U26) which are alternately enabled by the -WC control strobe produced by the 8X300. To provide edges on read strobes during sequential read operations from various ports, the red strobe decoder (U20) is always disqualified at the end of instruction by +MCLK' which is a delayed copy of +MCLK. This delay compensates for timing races through the Fast I/O latch (U27) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit BUS called the "I/O" BUS. This BUS is active low. It must be noted that this BUS is in no way related to the instruction data BUS and can be thought of as simply an 8-bit bidirectional I/O BUS of the 8X300. In fact it has been renamed as I/O0-I/O7 to reflect this distinction.

8.2.2 Internal BUS Control

Several BUS control signals are produced by the 8X300 to identify and strobe the data in the I/O BUS. WC (write control) is a signal which determines the direction of the data to and from peripherals. When WC is false (during the first half cycle), data is being input to the 8X300 from the I/O BUS. When WC is true (during the second half cycle), data is being output from the 8X300 onto the I/O BUS. SC (select control) is a signal which

becomes active during the second half cycle instead of WC if the I/O BUS contains an 8-bit I/O address. In the WD1000, both WC and SC are combined by a NOR gate (U24) to indicate all accesses to any port. This arrangement allows 8-bit immediate-data moves from the 8X300 to any output port within one instruction, instead of the normal 5-bit immediate moves provided for by the instructions set.

All instruction fetches occur late in the second cycle of the preceding instruction. This time is marked by the generation of a 65 nS (nominal) active high pulse called MCLK which occurs every instruction. MCLK is used to latch data prior to being input on the I/O BUS to insure stability during reads. It is also used to disqualify any read strobes that would otherwise remain true during the second clock cycle of any instruction which does not write to a port.

Two additional BUS control signals are produced by the 8X300. They are RIGHT BANK SELECT (-RB) and LEFT BANK SELECT (-LB). These are not used, however, in the WD1000 due to the implementation of the Fast I/O Select logic.

8.2.3 Reset Circuit

The 8X300 is held in reset for approximately 40 mS after initial power on. This is accomplished by an RC network (R42, C68 and CR3) which drives a Schmitt trigger (U31) to provide a proper rise/fall time on the -RESET line of the 8X300. Alternate reset of the processor can be accomplished by dropping -MR (J5 pin 39) whenever the host wishes to reset the controller. A Schmitt trigger (U31) is provided with a 4.7K pull-up (R43) to buffer the -MR input from the host. -RESET also propagates to the drive control latches (U52 and U48) and their associated line drivers (U54-56) and host interface WAIT (U320, DRQ and INTRQ latches (U30), ensuring proper initialization of these functions during power-up and subsequent resets from the host.

8.2.4 Processor Power Supply

Power is supplied to the 8X300 from the +5 Volt (Vcc) power BUS. Due to the internal operation of the 8X300, an on-chip voltage reference is provided to produce bias to an external pass transistor (Q4). This drops Vcc to the 8X300 to approximately +3.0 Volts. All signals into and out of the 8X300 are internally level shifted to be TTL compatible.

8.2.5 Read and Write Ports

Throughout the circuit, output ports are formed by D type latches using write strobes (WRO-7) to latch data into the ports. Reading of ports is universally accomplished by using read strobes (RDO, RD2, RD4-6) that enable selected tri-state output devices on the I/O BUS. Additionally, two read strobes are used to clock the host DRQ and INTRQ latches (U30) and one read strobe is left unused as a "dummy" port for instructions not requiring data

from a port. This insures troublefree operation of the Fast I/O port decoders.

8.2.6 Read/Write Memory

Since the 8X300 does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the I/O BUS. RAM must, therefore, be accessed via the I/O BUS by I/O instructions like all other port accesses. To provide for addressing the RAM, three latch counters (U40, 45 and 46) are connected to the I/O BUS to receive and store addresses required to access the RAM (U33 and U39).

8.2.6.1 RAM Addressing

The RAM address BUS (RAO-RA9) uniquely addresses 1 of 1024 memory locations. As each counter chip reaches a count of 0, it sets a borrow condition to the next higher counter which is decremented at the end of the next access to RAM. When all bits of the address have been reset, the -ROVF bit on the last counter (U40) is reset providing an overflow status which can be read by the processor on U43. By setting various beginning address values, -ROVF can be used to mark the end of any RAM access loop from 1 to 1024 bytes in length. In the WD1000, this function is used for setting sector buffer lengths of 128, 256, or 512 bytes.

8.2.6.2 Sector Buffering

All data read from the disk or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented which means that effective addresses are stable to the RAM by at least the instruction prior to the actual access. This preselection feature effectively reduces RAM access time to the output enable and propagation time of the RAM for read operations and the width of the minimum -WR strobe pulse for write operations.

8.2.6.3 RAM Accessing

RAM access is initiated by -RCS which is the logical OR (by U25) of -RDO and -WRO generated by the Fast I/O decoders (U20 and U26). Data to be read from RAM will be placed on the I/O BUS whenever -RCS is low and -WC is high. Data is written into a selected RAM cell on the trailing edge of -WC if -RCS is low. During writes, both -WC and -RCS will be low for at least 120 nS so that data setup time requirements are met.

8.2.6.4 Scratchpad Operations

Because the RAM address counters can be preset, direct reads and writes to a specific address are possible. This function is used for scratchpad storage during program execution. This mode of RAM access requires 2 or 3 instruction cycles for each random access to the RAM as opposed to 1 for sequential access using the

post-decrement feature.

8.2.7 MAC Control Port

Basic control of the various functional sections of the WD1000 is accomplished by a dedicated 6-bit control port called MAC CNTRL (U34). MAC CNTRL enables the functions of the WAIT control circuitry (-WAEN), CRC generation (-CRCIZ), gating of read data into data separation circuitry (RGATE), selection of read or write functions (-WRITE), control of CRC check word output (-1BLA) and AM detection (SRCH). MAC CNTRL output states are latched into the port by a write strobe (WR7). Additionally, any time MAC CNTRL is loaded with a new byte, the lower two data bits (I/O0-1) are strobed into the upper two address counter/latch bits (RA8,9).

All remaining ports are distributed among the basic functional sections of the WD1000 and are described in detail within the discussion of those functions.

8.3 Serial Data Separation

The WD1000 controller contains on-board circuitry to process incoming MFM data from the drive by a process called data separation. Here, some background information may be helpful:

In order to provide maximum data-recording density for maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of data capacity, hence the term "double density".

The fact that clock bits are not recorded with every data bit cell requires circuitry that can remain in sync with data during the absence of clock bits. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bit timing when clocks are missing and synchronize to clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship to the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

8.3.1 Incoming Data Selection

In the WD1000, serial data is input from up to four radially-connected drives via a quad RS 422 differential receiver (U15). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to the data separation circuitry by a four-section

AND/OR/INVERT gate (U23). At this point data and clocks are still combined and appear as 50 nS (nominal) active high pulses spaced at intervals of 1, 1.5, or 2 times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U18) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

8.3.2 Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q3, U17 and associated circuitry). This oscillator uses a fundamental crystal cut to oscillate at 4 times the RCLK frequency. The 4X output is then divided by U17 to produce both a 2X clock (2XDR) which is used as a reference and a 1X clock (WCLK) which is used to produce MFM write data for the disk. The crystal (Y1) frequency is 20.000 MHz for ST506 compatible drives or 17.360 MHz for SA1000 compatible drives.

8.3.3 Clock Gating

The gating of the reference and MFM data into the data separator is dependent on the condition of the read gate (RGATE) signal and the spacing of the data on the serial stream after RGATE is brought true. The techniques used to separate data from clocks make it necessary to run the VCO at a rate twice the data clock (RCLK) rate. The VCO is therefore set to an open loop frequency of 2X RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VCO. Instantaneous shifts in data due to the effects of adjacent bit cells on the disk and minor noise must be ignored. Also, the response of the VCO must be adjusted to effectively override missing clock bits which occur as a result of the MFM recording technique.

The resultant compromise between response and reject requirements of the VCO causes the VCO to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at 1.5 or 2 times the actual RCLK time intervals.

To prevent this from occurring, the VCO is always held locked onto a stable clock running at 2 X RCLK frequency whenever the controller is not actually reading data. Read data is switched to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

8.3.4 High Frequency Detector

The switching function is initiated immediately after the RGATE goes true. It will only switch read data into the VCO after 16 consecutive ones or zeros (high frequency) are detected by a one-shot (U10) and counter (U12) connected directly to the raw MFM data.

The one-shot is adjusted for a pulse width of 1.25 times the RCLK period. This is a 250 +/-10 nS for ST506 compatible drives and 287 +/-10 nS for SA1000 compatible drives. These adjustments of the DRUN one-shot (U10) provide tolerance of up to 1/4 RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.

Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constant, the one-shot remains retriggered.

As the one-shot is triggered by data stream bits, so is the up/down counter (U12), whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered, the counter counts up.

When any data bit fails to reach the one-shot before its time constant is over, the one-shot resets and in turn clears the counter. Only when 16 successive retriggers occur can the counter reach its terminal count. At this time, the counter overflow goes true and sets up the -DRUN latch output (U13 pin 8) low which switches read data in and reference clock out. An AND/OR/INVERT gate (U18) performs the switching. -DRUN is read through U42 by the 8X300 to determine the condition of the MFM data stream.

The data and clocks are now connected to the first stage of the data separator. The heart of the data separator is the VCO (U2 and associated circuitry) and the error amplifier and filter (U1). As previously stated, the VCO runs at a frequency twice that of the RCLK rate.

8.3.5 VCO

RCLK is produced by the VCO through a divide-by-two counter (U8). The VCO is a discrete LC oscillator with a shunt capacitor formed by a hyper-abrupt tuning diode (CR1). The diode varies its capacitance in accordance with the amount of reverse DC bias applied to its PN junction. As the bias decreases, the capacitance increases, pulling the oscillator down in frequency. Conversely, as the bias increases, the oscillator frequency rises.

The VCO performs conventionally with one exception. To help the VCO lock onto the incoming signals more quickly, an external timing signal freezes the output of the VCO in the high state. This is done by disqualifying U2 in the VCO feedback circuit and by removing bias from the transistor (Q2) which provides loop gain in the oscillator. -PHASEUP performs this function and is present just after the switch over from reference clock to MFM data is made.

The width of -PHASEUP is directly related to the difference in timing between the positive going transition of the VCO output and the positive transition of the second data/clock bit of the

MFM data stream. -PHASEUP causes the output of the VCO to rise in phase with the MFM data from the drive. This allows the VCO to adjust its phase slightly to center data/clocks within the RCLK rather than performing a frequency acquisition to lock onto the data stream. The phase acquisition is much faster and easier to achieve and results in vastly improved performance.

8.3.6 Error Amplifier

The error amplifier and filter control the VCO. The error amplifier is a balanced differential amplifier whose output either sources or sinks current to the filter stage. The error amplifier output is pulse-width modulated by the phase detector (U6, 7).

Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these pulses producing an average increase in the voltage to the cathode of the hyper-abrupt tuning diode (CR1). This effectively increases the reverse bias on the diode which reduces its capacitance and therefore increases the VCO frequency slightly to match the phase of the incoming data.

Whenever the VCO is running too fast, the error amplifier produces pump-down pulses to the filter. The diode then receives decreased reverse bias, more capacitance, and lower VCO frequency.

The operating point of the tuning diode (CR1) is initially set for an open loop VCO frequency of two times RCLK by setting -OSC ADJUST and monitoring the VCO output. This adjustment places the initial bias through the bias divider (R18-20, R22 and C8-9) at approximately -2.8 V to -3.2 V. At this setting the most responsive region of the diode is being used giving higher gain in the VCO. To keep the initial bias voltage close to three volts with varying disk data rates, the VCO inductor (L1) is 3.3 UH for 5 MHz drives and 3.9 UH for 4.34 MHz drives.

The VCO is forced to match the phase of the incoming data. Once the VCO is close to the phase of the incoming data, the pump pulses become very small or are missing completely. It must be noted, however, that a slight error is always be present because, without pumps, the filter floats and the VCO drifts. The overall gain of the error amplifier and the VCO maintains this very small error, resulting in very close tracking between the VCO ouput phase and the incoming data phase.

As previously stated, great care is taken to insure that the VCO starts on the same phase as the incoming data. If this were not the case, the error amplifier would produce very large pumps in an attempt to pull the VCO onto frequency and phase. Due to the gain of the error amplifier and the required characteristics of the filter, the integrated pump pulses would over-compensate, causing the VCO to overshoot in its attempt to lock-on. This

action would continue in a diminishing fashion until lock-on occurred. Unfortunately, the data sync fields it was trying to acquire would be over by the time the VCO finally acquired lock-on. -PHASEUP is, therefore, extremely important to the overall ability of the data separator to function reliably.

8.3.7 Sample on Phase Detector

The circuitry which feeds the error amplifier is called the Sample on Phase Detector. This circuit consists of several D latches (U7) and a delay line (DL1). The function of the circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 50 nS in length. The windows are initiated by a leading edge of any data bit as it enters the detector. They are terminated by that same data bit, edge-delayed by a net 50 nS (60 nS in the delay line minus approximately 10 nS in propagation delays).

When both the delayed data bit and the nearest VCO edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce a pump-up condition at the error amplifier. The VCO clock edge sets its half of the detector to produce a pump-down condition. When the circuit is balanced, either both pumps are on or both pumps are off, producing no net pump-up or down.

8.3.8 Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. This is done by using a technique called window extention. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles and then to be latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data off the sample on-phase detector delay line at the 60 nS tap and inverting the VCO clock to the RCLK divider (U8). The delayed data clocks a pair of latches (U9). The 'data' latch has its D input and CLEAR connected to +RCLK and the 'clock' latch has its D input and CLEAR connected to -RCLK.

If an MFM data bit enters the latches while -RCLK is high, it will be extended as a data bit. If -RCLK is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately 1/4 the RCLK period without being lost. The output of each latch is then further extended by feeding directly into another stage of latches (U3) and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals, one consisting solely of NRZ data, and the other NRZ clocks. NRZ data and clocks are finally in a form suitable for processing by subsequent circuitry within the WD1000.

8.3.9 Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on -RCLK are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U8) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the AM detector (U14) by raising the SEARCH signal. This signal releases a latch (U13) which removes -DHOLD from the RCLK divider (U8) on the next rising edge of a MFM data bit so that CLOCKS will be on the -RCLK phase and DATA will be on the +RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which are detected by the one-shot (U10) in the DRUN circuit. Once released, the phase of RCLK vs data and clocks remains stable throughout the read of an ID field or data field. Whenever SEARCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

8.4 Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X300. This processing consists of 3 functional circuits.

1) AM detection (U14)

2) Serial to parallel conversion (U29)

3) CRC checking circuit (U19)

Each function is discussed separately but many interdependencies exist.

8.4.1 AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. It is also impossible to determine byte boundaries. This problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'A1' with a missing clock pattern of HEX 'OA'. Normally, a data byte of HEX 'A1' requires a clocking pattern of HEX 'OE'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (Data or ID field) within each sector. Preceding each AM on the disk there is always a long run of "zero" data.

Zeros have a clock bit for every RCLK. When attempting to read information from the disk, the WD1000 first acquires phase lock over a field of zeros. After this acquisition is achieved, the processor releases the AM detector (U14) by raising the SEARCH control line (SRCH) on the MAC CNTRL port (U34). Because of the circuitry associated with the VCO to RCLK divider, the -RDAT output of the data separator (U3 pin 8) will be high and the -CLKS output (U3 pin 6) will be low. -RCLK will be the shifting clock for -RDAT and +RCLK will be the shifting clock for -CLKS. These 4 signals are routed into the AM detector.

Inside the AM detector, the -RDAT is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of -RCLK. -CLKS are shifted into a similar shift register on the falling edge of +RCLK. The output stage of the -RDAT register is dumped into an 'A1' comparator and the output stage of the -CLKS register is dumped into an 'OA' comparator. AM detection occurs when both detectors are true, thereby making the relationship between data and clocks known. It is also known that data is being clocked by -RCLK so -CLKS can actually be discarded; their only purpose was in detecting AM. The -AMDET signal is used as a synchronization signal to start subsequent conversion circuitry. The -AMDET signal remains true until the processor again de-asserts the SEARCH control line.

8.4.2 Serial to Parallel Conversion

After an AM has been detected, the Serial to Parallel converter (U29) takes over. NRZ data and -RCLK are used to shift data bits into an 8-bit serial to parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is incremented. After every eight bit of data is shifted, the counter produces an overflow pulse, marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the I/O BUS using read strobe 4 (RD4) in conjunction with a tri-state buffer (U36). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial to parallel device also include -SHFTCLK and -DOUT. -SHFTCLK is actually -RCLK propagated through the device. -DOUT and -SHFTCLK are tri-stated along with BDONE, and are active only when -WRITE is high, indicating a read mode of operation. -DOUT and -SHFTCLK are routed to the CRC generator checker device.

8.4.3 CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. On the WD1000, a Cyclic Redundancy Check (CRC) is performed on all data transfers from the disk. The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16-bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator re-computes the original CRC bits. After the last two bytes (containing the original recorded CRC) are read, the value in the CRC generator must always be zero. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after it has checked all bytes of the recorded data, then the controller will flag the data as erroneous and enter into a retry condition. If after attempting to correctly read the data 16 times, the controller still cannot get correct data, the read is aborted and the host is informed that the data in the buffer is questionable.

The WS1000 uses the same device to generate and check CRCs for data being written and read on the disk. The polynomial used is:

X16+X12+X5+1 (commonly called the CRC-CCITT polynomial)

During read operations, the processor polls the condition of the DRUN circuitry. When DRUN is true, it begins to search for an address mark. Once the AM is located, the processor starts to read parallel data which has been converted from NRZ data by the serial-to-parallel device. The processor terminates this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting -CRCIZ low for at least 250 nS during the search for the AM. -CRCIZ is originated on the MAC CNTRL port (U34). Upon receiving the -CRCIZ signal, the CRC generator/checker presets all 16 of its internal polynomial division shift registers to logic ones. It also arms an internal latch which enables the checking function on the leading edge of the first non-zero data to enter the device.

Prior to an AM there is a field of zeros (all data bits low), so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

Once enabled by the first non-zero data bit, the CRC device shifts succeeding data bits into a feedback shift register string with exclusive OR gates tied to the feedback nodes on the first, fifth, twelvth and sixteenth registers. As each RCLK occurs, the registers divide the incoming data and a unique pattern of ones

and zeros appear across the registers.

When the last bit of an ID or DATA field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the exclusive OR gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16-bit wide comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U43 to see if a CRC error occurred.

After the CRC bits are processed, the data stream contains at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers, then none are flipped if a constant input of zeros is shifted into the registers. This provides a convenient latching function for the CRCOK flag which remains true for at least 1 byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock and BDONE are supplied to the CRC device on a 3-bit minibus. During read operations, the Serial-to-Parallel device (U29) sources these lines because the WRITE control line from MAC CNTRL (U34) is low. This enables the tri-state drivers on these lines. The Parallel-to-Serial device (U37) has its tri-state drivers disabled.

8.5 Serial Data Generation

The WD1000 records data on the disk in MFM format. To produce the proper data format, the WD1000 uses several specialized devices. These devices process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data generation section are listed below:

1) Parallel to Serial conversion (U37)

2) CRC generation (U19)

3) MFM and precompensation (U30)

8.5.1 Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the Parallel-to-Serial device (U37). The processor enables this conversion by lowering the -WRITE signal on MAC CNTRL (U34). -WRITE causes the tri-state buffers present on the parallel-to-serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the I/O bus along with the -WR4 write strobe which latches the data into the parallel port on the trailing edge of the strobe. The write strobe also resets any pending BDONE. Inside the parallel-to-serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transistion. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U43 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate 1/8 that of the bit rate of the NRZ data stream. For ST506 compatible drives the byte timing is 1.6 us and for SA1000 drives it is 1.84 us.

The output of the last register in the shift string is brought out of the device as an NRZ serial data stream. The shifting clock is also brought out as SHFCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

8.5.2 CRC Generation

The CRC generator/checker (U19) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing -CRCIZ for approximately 250 nS while the parallel-to-serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero data bit enters the device. The first non-zero bit is the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it stores a HEX A1 in the parallel-to-serial device. At the proper time (in sync with BDONE) the

parallel-to-serial device begins to send the MSB of the AM to the CRC device. This starts the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel-to-serial device, it drops the -1BLA (1 Byte Look-ahead) signal on MAC CNTRL port (U34). This signal causes the CRC generator to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last date (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. -1BLA is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving -1BLA low for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device.

8.5.3 MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precomp device. This device accepts NRZ data and a complimentary WCLK. It also produces MFM data and clocks by sending the data through circuitry which decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1) If the current data cell contains a data bit, then no clock bit is generated.

2) If the previous data cell contained a data bit, then no clock bit is generated.

3) If the previous data cell and the present data cell are vacant, then a clock bit in the current clock cell is produced.

The terms "data cell" and "clock cell" are defined by the state of the WCLK. While WCLK is low, it is a data cell. While WCLK is high, it is a clock cell. Therefore, both clock and the data cells are 1/2 the period of WCLK or 100 nS for ST506 compatible drives and 115 nS for SA1000 drives. Also, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be 1, 1.5, or 2 times the WCLK period only.

These rules are implemented within the device by shift registers that hold the next two last and present data bits and combinatorial logic. The state of WCLK is considered and the appropriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so

it is run through a re-timing latch (U21) to clean it up.

8.5.3.1 Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as 'dynamic bit shift'.

Dynamic bit shift comes about as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. "Write precompensation" is a method which can be applied to reduce the effect of this shift on the data.

Precompensation is a way of predicting which direction a particular bit will be shifted and then intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last and the present bits to be written, and producing three signals depending on what these bits are. The three signals are EARLY, LATE and NOMINAL. They are used in conjunction with a delay line to cause the leading edge of a data/clock bit to be written early, late, or on time. As with MFMW, these signals are subject to decoding slivers and must be retimed by U21.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from the MAC CNTRL port (U34). When RWC is high, precomp is in effect. When RWC is low, no precomp is generated and the NOM output of the device is held true.

The delay line actually performs the precomp with the help of an AND/OR/INVERT gate (U22). MFMW pulses are applied to the input of the delay line and, depending on which of the three precomp signals is present, the AND/OR/INVERT gate selects a different tap on the delay line. Nominal data is tapped from the second tap, early data from the first tap, and late data from the third tap. From the AND/OR/INVERT gate, the MFMW data is sent to the input of an RS 422 driver (U16) where it is converted to a differential form and then is sent to the drive.

The AND/OR/INVERT gate has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal is low. This is inverted by U38 and applied to the AND/OR/INVERT gate's fourth section. This resulting high input effectively inhibits the gate from accepting MFMW data.

8.6 Host Interface

All data transfers between the host and the WD1000 take place over an eight-bit bi-directional bus (J5) consisting of eight Data Access Lines (DALO-7). The source or destination register inside the WD1000 is selected by the three address lines (A0-2). All accesses to the WD1000 are controlled by Card Select (CS-), Read enable (RE-), or Write Enable (WE-). Since the access time for any particular read or write operation varies, the WD1000 provides a not-ready signal (WAIT-). For systems using interrupts and/or DMA, the WD1000 provides INTerrupt reQuest (INTRQ) and Data ReQuest (DRQ).

Accessing the WD1000 is like accessing variable speed RAM. The host must provide a valid address in A0-2 along with a CS-. Immediately or after a short set-up time, the host may assert RE- or WE-. If access time on the WD1000 is over 100 nS, then WAIT- is asserted. The host must keep all address lines and strobes stable while WAIT- is true. When the WD1000 de-asserts WAIT-, the data has been accepted on a write or the data is on the DAL bus on a read.

8.6.1 Wait Enable

Since most of the registers in the WD1000 are not implemented in hardware, it takes the 8X300 a finite amount of time to fetch the requested data on a read or to store data on a write. This time varies depending on the amount of processing the 8X300 must do to access the desired register. After the data has been written or read, the WD1000 de-asserts the WAIT- line, allowing the host to terminate the current bus cycle.

The generation of the WAIT- signal is controlled by a bit in the MAC latch (U34) called WAit ENable (WAEN- will be asserted). On each bus access, the host must drop the Card Select (CS-) line on J5. The leading edge of CS- clocks the wait control latch (U32), transferring the WAEN- state through the latch, qualifying the wait drivers (U44, 54). This clocking action is required to ensure that WAIT- will not be asserted in the middle of any bus access already in progress. After the wait latch has been clocked, CS- (BIC or BOC in some installations) causes WAIT- to be asserted to the host.

The WAIT- line is released on the trailing edge of any read or write strobe to the communications latch (U49). This release is caused by the logical OR of RD6- and WR6- on U25 which presets the wait latch (U32) to a non-wait request condition. The WAIT- signal is stretched to the trailing edge of the RD6- or WR6- by U2.

If WAEN- is de-asserted, the WD1000 generates no waits at all. In this case, the host reads the dummy status written to the communications latch by the 8X300. This feature is used by the microcode to simulate a busy condition when the host reads the

status register in non-interrupt driven systems. When the WD1000 becomes un-busy, the WAEN- line is asserted and operations on the host interface bus are monitored once again.

8.6.2 Bus Gating

During all accesses by the host, one of two signals are produced to gate the bus. During read operations, CS- and RE- are ANDed, producing Bus Output Control (BOC-). This signal gates the contents of the communication latch (U49) onto the DAL bus. During write operations, CS- and WE- produce Bus Input Control (BIC). This signal latches the state of the DAL lines into an internal R/S latch.

8.6.3 Register Selection

The combination of a host read or write operation along with the WREQ- signal being asserted, generates a signal called the Card Select ACcess (CSAC). The 8X300 samples this signal at U43 every 250 nS, and, if asserted, reads the status of A0-2 and WE- (U43). The state of A0-2 and WE- determines which register is to be accessed (A0-2) and in what direction that access will take place.

8.6.4 Interrupts and DRQs

The WD1000 produces INTerrupt ReQuests (INTRQ) to signal the end of all disk operations and Data ReQuests (DRQ) to signal data ready to DMA controllers. INTRQ and DRQ originate on the MFM generator (U30) as an auxillary function of the chip. The WD1000 sets INTRQ using INTCLK- and sets DRQ using DRQCLK-, both of which are produced by U20.

Interrupts are cleared by HSAC- (Host Select ACcess) and AO, when the host reads the Status register, issues a command, or accesses the Sector Number register. DRQs are cleared when the host accesses the Data or cylinder Low registers. DRQs are re-issued for each byte to be transferred. HSAC- is a 200 nS version of the CSAC- signal. During Power-On Reset of Master Reset (MR-), INTRQ is set and DRQ is reset.

8.7 Maintenance and Adjustments

The WD1000 requires no scheduled preventive maintenance. There are a few adjustments associated with the data separation circuitry that may need to be adjusted if a drive with a different data rate is installed. Remember, the inductor L1 must be the proper value for the data rate being used and Y1 must be selected for a fundamental frequency of four times the data rate.

8.7.1 VCO Adjustments

Data separation circuitry on the WD1000 uses a voltage-controlled oscillator (VCO) which phaselocks onto incoming data and provides a clock suitable for separating data and clock bits on an MFM

encoded data stream. The VCO must be adjusted using the following procedures.

1. Ground the cathode of the tuning diode (CR1) to the closest accessible ground using a low inductance-shorting cable. This cable should consist of the shortest piece of wire possible to make the connection.

2. Connect a frequency counter to the VCO buffered output on TP9.

3. Apply power to the board. Ensure a logic "1" exists at TP17. A logic "0" on TP17 inhibits the VCO and makes adjustments impossible. If a logic "1" is not present, verify that the DRUN circuitry (U10-U13) is functioning and adjusted properly. Refer to Section 8.7.4 for adjustments to DRUN.

4. Vary the OSC ADJ pot (R22) to verify that the range of adjustment values listed in the following table are obtainable. After the range has been verified, adjust R22 to the final setting listed in the table.

Y1 Frequency	Identity	Range	Final Setting
20.000 MHz	L1 = 3.3 uh	9.0-11.0 MHz	10.0 MHz +/-1 KHz
17.360 MHz	L1 = 3.9 uh	7.5-9.5 MHz	8.68 MHz +/-1 KHz

5. Turn off power to the board. Disconnect all test jumpers and test equipment.

8.7.2 Error Amplifier Adjustments (Static)

The phase detection technique used to correct the frequency and phase of the VCO employs a balanced sample and hold error amplifier. To ensure reliable operation of the data separator, the error amplifier must be properly balanced. The balance adjustment must be made using the following procedures.

1. Apply power to the board. Ground TP20 or U7 pin 4 to turn off the right half of the error amplifier (U1). In this state current only flows in the left half of the amplifier.

2. Connect a 100-ohm resistor between U1 pin 8 and ground.

3. Adjust the BAL pot (R1) until a reading of 0 V +/- 20 mV is observed on TP5.

4. Remove the ground from TP20. Install a ground to the PUP1 signal line accessible on U7 pin 1. Connect Vcc to U7, pin 4 to turn off the left half of the error amplifier (the right half of the error amplifier will be on).

5. Verify a reading of 0 V +/- 50 mV on TP6. This indicates that the side-to-side balance of the error amplifier is within tolerance.

6. Re-adjust R1 until the reading at TP5 is 0 V +/- 20 mV.

7. Turn off the power to the board. Disconnect all jumpers and test equipment.

8.7.3 Error Amplifier Adjustments (Dynamic)

After the static balance adjustments are performed, the error amplifier should be adjusted for balanced dynamic operation.

This adjustment requires that the controller be constantly reading data on the innermost cylinder of a formatted drive.

1. While reading data, monitor TP9 (-OSC) with a frequency counter.

2. Adjust the error amplifier balance pot (R1) until the most stable display reading is obtained. This indicates that the VCO is being locked on every attempt to read data.

3. Turn off power to the board.

4. Disconnect all test equipment.

8.7.4 DRUN Adjustments

To facilitate the process of acquiring phase-lock on data being read from a disk, a hardware detector is utilized to indicate when the read/write head of the drive is over a recorded field of all ones or all zeros. The detector depends on the timing of a one-shot (U10) which is adjustable by the DRUN pot (R26). R26 must be adjusted according to the following procedures:

The DRUN adjustment is made with the WD1000 in an operating test configuration with a host, drive and power source.

1. Once the proper setup is made, apply power to the WD1000 and all test equipment.

2. Monitor TP14 (-DRUN) with a 10X oscilloscope probe while attempting to read a sector of data from the drive. The scope should be set to trigger on a high to low transition.

3. While observing TP14, adjust R26. The period of the DRUN single shot should be adjusted to 1.25 times the period of RCLK.

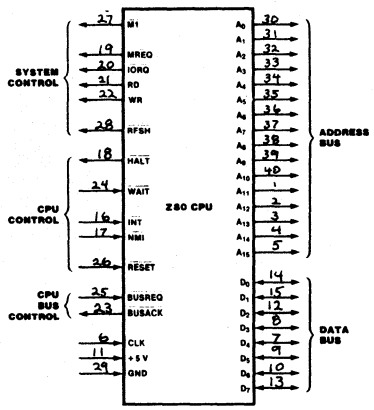
4. Turn off power to the WD1000.

5. Disconnect all test equipment.

Zilog

Z8400
Z80® CPU Central Processing Unit

Features



Pin Descriptions

A_0-A_{15}. *Address Bus* (output, active High, 3-state). A_0-A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

BUSACK. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR have entered their high-impedance states. The external circuitry can now control these lines.

BUSREQ. *Bus Request* (input, active Low). Bus Request has a higher priority than NMI and is always recognized at the end of the current machine cycle. BUSREQ forces the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR to go to a high-impedance state so that other devices can control these lines. BUSREQ is normally wire-ORed and requires an external pullup for these applications. Extended BUSREQ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0-D_7. *Data Bus* (input/output, active High, 3-state). D_0-D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

HALT. *Halt State* (output, active Low). HALT indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

INT. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. INT is normally wire-ORed and requires an external pullup for these applications.

IORQ. *Input/Output Request* (output, active Low, 3-state). IORQ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. IORQ is also generated concurrently with M1 during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

M1. *Machine Cycle One* (output, active Low). M1, together with MREQ, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. M1, together with IORQ, indicates an interrupt acknowledge cycle.

MREQ. *Memory Request* (output, active Low, 3-state). MREQ indicates that the address bus holds a valid address for a memory read or memory write operation.

NMI. *Non-Maskable Interrupt* (input, active Low). NMI has a higher priority than INT. NMI is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

RD. *Memory Read* (output, active Low, 3-state). RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

RESET. *Reset* (input, active Low). RESET initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that RESET must be active for a minimum of three full clock cycles before the reset operation is complete.

RFSH. *Refresh* (output, active Low). RFSH, together with MREQ, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

WAIT. *Wait* (input, active Low). WAIT indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended WAIT periods can prevent the CPU from refreshing dynamic memory properly.

WR. *Memory Write* (output, active Low, 3-state). WR indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchanges, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts
- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	Flags H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	•	X	•	•	•	01 r r'		1	1	4	r, r' Reg.
LD r, n	r ← n	•	•	X	•	X	•	•	•	00 r 110 – n –		2	2	7	000 B 001 C
LD r, (HL)	r ← (HL)	•	•	X	•	X	•	•	•	01 r 110		1	2	7	010 D
LD r, (IX+d)	r ← (IX+d)	•	•	X	•	X	•	•	•	11 011 101 01 r 101 – d –	DD	3	5	19	011 E 100 H 101 L
LD r, (IY+d)	r ← (IY+d)	•	•	X	•	X	•	•	•	11 111 101 01 r 110 – d –	FD	3	5	19	111 A
LD (HL), r	(HL) ← r	•	•	X	•	X	•	•	•	01 110 r		1	2	7	
LD (IX+d), r	(IX+d) ← r	•	•	X	•	X	•	•	•	11 011 101 01 110 r – d –	DD	3	5	19	
LD (IY+d), r	(IY+d) ← r	•	•	X	•	X	•	•	•	11 111 101 01 110 r – d –	FD	3	5	19	
LD (HL), n	(HL) ← n	•	•	X	•	X	•	•	•	00 110 110 – n –	36	2	3	10	
LD (IX+d), n	(IX+d) ← n	•	•	X	•	X	•	•	•	11 011 101 00 110 110 – d – – n –	DD 36	4	5	19	
LD (IY+d), n	(IY+d) ← n	•	•	X	•	X	•	•	•	11 111 101 00 110 110 – d – – n –	FD 36	4	5	19	
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00 111 010 – n – – n –	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00 110 010 – n – – n –	32	3	4	13	
LD A, I	A ← I	↕	↕	X	0	X	IFF	0	•	11 101 101 01 010 111	ED 57	2	2	9	
LD A, R	A ← R	↕	↕	X	0	X	IFF	0	•	11 101 101 01 011 111	ED 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	•	11 101 101 01 000 111	ED 47	2	2	9	
LD R, A	R ← A	•	•	X	•	X	•	•	•	11 101 101 01 001 111	ED 4F	2	2	9	

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	•	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	X	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	X	•	•	11 101 101 ED 01 dd1 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	X	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	X	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	X	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	X	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	•	X	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	•	X	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	•	X	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	X	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	•	X	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H SP ← SP − 2	•	•	X	•	X	•	•	11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H SP ← SP − 2	•	•	X	•	X	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H SP ← SP − 2	•	•	X	•	X	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qq_H ← (SP + 1) qq_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively,
e.g., BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	00 001 000 08	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	11 011 001 D9	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•		1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	•	•	X	① 0	X	↕	0 •	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0 •	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	① ↕	0 •	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0 •	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	↕	② ↕	X	↕	X	① ↕	1 •	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1 •	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	↕	② ↕	X	↕	X	① ↕	1 •	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X	↕	X	① ↕	1 •	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.
② Z flag is 1 if A = (HL), otherwise Z = 0.

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	↕	↕	X	↕	X	V	0 ↕	10 000 r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	↕	↕	X	↕	X	V	0 ↕	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	X	↕	X	V	0 ↕	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	X	↕	X	V	0 ↕	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	X	↕	X	V	0 ↕	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	↕	↕	X	↕	X	V	0 ↕	001				s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.
SUB s	A ← A − s	↕	↕	X	↕	X	V	1 ↕	010				
SBC A, s	A ← A − s − CY	↕	↕	X	↕	X	V	1 ↕	011				
AND s	A ← A ∧ s	↕	↕	X	1	X	P	0 0	100				
OR s	A ← A ∨ s	↕	↕	X	0	X	P	0 0	110				
XOR s	A ← A ⊕ s	↕	↕	X	0	X	P	0 0	101				
CP s	A − s	↕	↕	X	↕	X	V	1 ↕	111				
INC r	r ← r + 1	↕	↕	X	↕	X	V	0 •	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	↕	↕	X	↕	X	V	0 •	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	X	↕	X	V	0 •	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	X	↕	X	V	0 •	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	↕	↕	X	↕	X	V	1 •	101				m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	P	•	↕	00 100 111	27	1	1	4	Decimal adjust accumulator.
CPL	$A \leftarrow \overline{A}$	•	•	X	1	X	•	1	•	00 101 111	2F	1	1	4	Complement accumulator (one's complement).
NEG	$A \leftarrow 0 - A$	↕	↕	X	↕	X	V	1	↕	11 101 101 01 000 100	ED 44	2	2	8	Negate acc. (two's complement).
CCF	$CY \leftarrow \overline{CY}$	•	•	X	X	X	•	0	↕	00 111 111	3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	0	X	•	0	1	00 110 111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	•	•	00 000 000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01 110 110	76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	•	•	11 110 011	F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	•	•	11 111 011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 101 101 01 000 110	ED 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 101 101 01 010 110	ED 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 101 101 01 011 110	ED 5E	2	2	8	

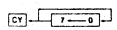
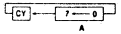
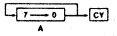
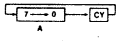
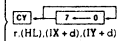
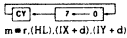
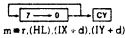
NOTES: IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip-flop.
* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

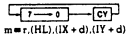
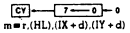
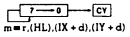
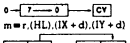
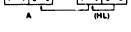
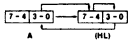
Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	↕	00 ss1 001		1	3	11	ss Reg. 00 BC 01 DE 10 HL 11 SP
ADC HL, ss	HL ← HL + ss + CY	↕	↕	X	X	X	V	0	↕	11 101 101 01 ss1 010	ED	2	4	15	
SBC HL, ss	HL ← HL − ss − CY	↕	↕	X	X	X	V	1	↕	11 101 101 01 ss0 010	ED	2	4	15	
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	↕	11 011 101 01 pp1 001	DD	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	↕	11 111 101 00 rr1 001	FD	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00 ss0 011		1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11 011 101 00 100 011	DD 23	2	2	10	
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11 111 101 00 100 011	FD 23	2	2	10	
DEC ss	ss ← ss − 1	•	•	X	•	X	•	•	•	00 ss1 011		1	1	6	
DEC IX	IX ← IX − 1	•	•	X	•	X	•	•	•	11 011 101 00 101 011	DD 2B	2	2	10	
DEC IY	IY ← IY − 1	•	•	X	•	X	•	•	•	11 111 101 00 101 011	FD 2B	2	2	10	

NOTES: ss is any of the register pairs BC, DE, HL, SP.
pp is any of the register pairs BC, DE, IX, SP.
rr is any of the register pairs BC, DE, IY, SP.

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00 000 111	07	1	1	4	Rotate left circular accumulator.
RLA		•	•	X	0	X	•	0	↕	00 010 111	17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0	↕	00 001 111	0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0	↕	00 011 111	1F	1	1	4	Rotate right accumulator.
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 r	CB	2	2	8	Rotate left circular register r.
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 110	CB	2	4	15	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)	 r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	11 011 101 11 001 011 ← d → 00 000 110	DD CB	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 11 001 011 ← d → 00 000 110	FD CB	4	6	23	
RL m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	010					Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	001					

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	011					
SLA m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	100					
SRA m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	101					
SRL m	 m ≡ r,(HL),(IX + d),(IY + d)	↕	↕	X	0	X	P	0	↕	111					
RLD		↕	↕	X	0	X	P	0	•	11 101 101 01 101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL).
RRD		↕	↕	X	0	X	P	0	•	11 101 101 01 100 111	ED 67	2	5	18	The content of the upper half of the accumulator is unaffected.

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b, r	$Z \leftarrow \overline{r_b}$	X	↕	X	1	X	X	0	•	11 001 011 01 b r	CB	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A b Bit Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	X	↕	X	1	X	X	0	•	11 001 011 01 b 110	CB	2	3	12	
BIT b, (IX + d)$_b$	$Z \leftarrow \overline{(IX+d)_b}$	X	↕	X	1	X	X	0	•	11 011 101 11 001 011 ← d → 01 b 110	DD CB	4	5	20	
BIT b, (IY + d)$_b$	$Z \leftarrow \overline{(IY+d)_b}$	X	↕	X	1	X	X	0	•	11 111 101 11 001 011 ← d → 01 b 110	FD CB	4	5	20	
SET b, r	$r_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011 11 b r	CB	2	2	8	
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 001 011 11 b 110	CB	2	4	15	
SET b, (IX + d)	$(IX + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 011 101 11 001 011 ← d → 11 b 110	DD CB	4	6	23	
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 111 101 11 001 011 ← d → 11 b 110	FD CB	4	6	23	
RES b, m	$m_b \leftarrow 0$ m ≡ r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	10					To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) of location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011 ← n → ← n →	C3	3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 ← n → ← n →		3	3	10	cc Condition 000 NZ non-zero 001 Z zero 010 NC non-carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign positive 111 M sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 ← e − 2 →	18	2	3	12	
JR C, e	If C = 0, continue	•	•	X	•	X	•	•	•	00 111 000 ← e − 2 →	38	2	2	7	If condition not met.
	If C = 1, PC ← PC + e											2	3	12	If condition is met.
JR NC, e	If C = 1, continue	•	•	X	•	X	•	•	•	00 110 000 ← e − 2 →	30	2	2	7	If condition not met.
	If C = 0, PC ← PC + e											2	3	12	If condition is met.
JP Z, e	If Z = 0 continue	•	•	X	•	X	•	•	•	00 101 000 ← e − 2 →	28	2	2	7	If condition not met.
	If Z = 1, PC ← PC + e											2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue	•	•	X	•	X	•	•	•	00 100 000 ← e − 2 →	20	2	2	7	If condition not met.
	If Z = 0, PC ← PC + e											2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101 11 101 001	DD E9	2	2	8	

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ, e	B ← B - 1 If B = 0, continue If B ≠ 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 010 000 10 ← e - 2 →	2	2	8	If B = 0.
											2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < -126, 129 >.
e - 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e.

Call and Return Group

			S	Z	H	P/V	N	C				
CALL nn	(SP - 1) ← PC_H (SP - 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD ← n → ← n →	3	5	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 ← n → ← n →	3	3	10	If cc is false.
											3	5	17	If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1	1	5	If cc is false.
											1	3	11	If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP - 1) ← PC_H (SP - 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: [1]RETN loads IFF_2 → IFF_1

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB ← n →	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	↕	↕	X	↕	X	P	0	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B - 1 HL ← HL + 1	X	①	X	X	X	X	1	•	11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B - 1 HL ← HL + 1 Repeat until B = 0	X	①	X	X	X	X	1	•	11 101 101 ED 10 110 010 B2	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B=0)	16	
IND	(HL) ← (C) B ← B - 1 HL ← HL - 1	X	①	X	X	X	X	1	•	11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B - 1 HL ← HL - 1 Repeat until B = 0	X	①	X	X	X	X	1	•	11 101 101 ED 10 111 010 BA	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B=0)	16	
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 ← n →	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B - 1 HL ← HL + 1	X	①	X	X	X	X	1	•	11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B - 1 HL ← HL + 1 Repeat until B = 0	X	①	X	X	X	X	1	•	11 101 101 ED 10 110 011 B3	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
											2	4 (If B=0)	16	
OUTD	(C) ← (HL) B ← B - 1 HL ← HL - 1	X	①	X	X	X	X	1	•	11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: ① If the result of B - 1 is zero the Z flag is set, otherwise it is reset.

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B - 1 HL ← HL - 1 Repeat until B = 0	X	↕	X	X	X	↕	•	11 101 101 ED 10 111 011	2	5 (If B≠0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
										2	4 (If B=0)	16	

Summary of Flag Operation

Instruction	D_7 S	Z	H	P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	P	0	0	Logical operations.
OR s, XOR s	↕	↕	X	0	P	0	0	
INC s	↕	↕	X	↕	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA, RLCA, RRA; RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD; RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r (C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI; OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 0.
INIR; INDR; OTIR, OTDR	X	1	X	X	X	X	1	•	
LDI; LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I, LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

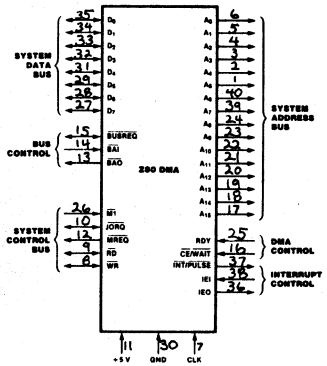
Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Z8410
Z80® DMA Direct Memory Access Controller

Features



Pin Description

A_0-A_{15}. *System Address Bus* (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. *Bus Acknowledge In* (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. *Bus Acknowledge Out* (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system buses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSREQ}$. *Bus Request* (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input, when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a buffer between it and the CPU because it is unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. *Chip Enable and Wait* (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. *System Clock* (input). Standard Z-80 single-phase clock at 2.5 MHz (Z-80 DMA) or 4.0 MHz (Z-80A DMA). For slower system clocks, a TTL gate with a pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements. In all cases there should be a resistive pullup to the power supply of 10K ohms (max) to ensure proper power when the DMA is reset.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. *Interrupt Enable In* (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$/PULSE. *Interrupt Request* (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system. This pin can also be used to generate periodic pulses to an external device. It can be used this way only when the DMA is bus master (i.e., the CPU's $\overline{BUSREQ}$ and $\overline{BUSACK}$ lines are both Low and the CPU cannot see interrupts).

$\overline{IORQ}$. *Input/Output Request* (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates that the 8-bit or 16-bit address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. *Machine Cycle One* (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. After the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. *Read* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

RDY. *Ready* (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (Byte, Burst or Continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSREQ}$ line to go Low or High.

$\overline{WR}$. *Write* (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled write to a memory or I/O port address.

Programming

The Z-80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests nor data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enable command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z-80 CPU).

Writing. Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

This is illustrated in Figure 8b. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)," then the next two bytes written to the DMA will be stored in these two registers, in that order.

Reading. The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z-80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming. A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.

Programming (Continued)

4. Load Port A address in WR6.
5. Enable DMA in WR6.

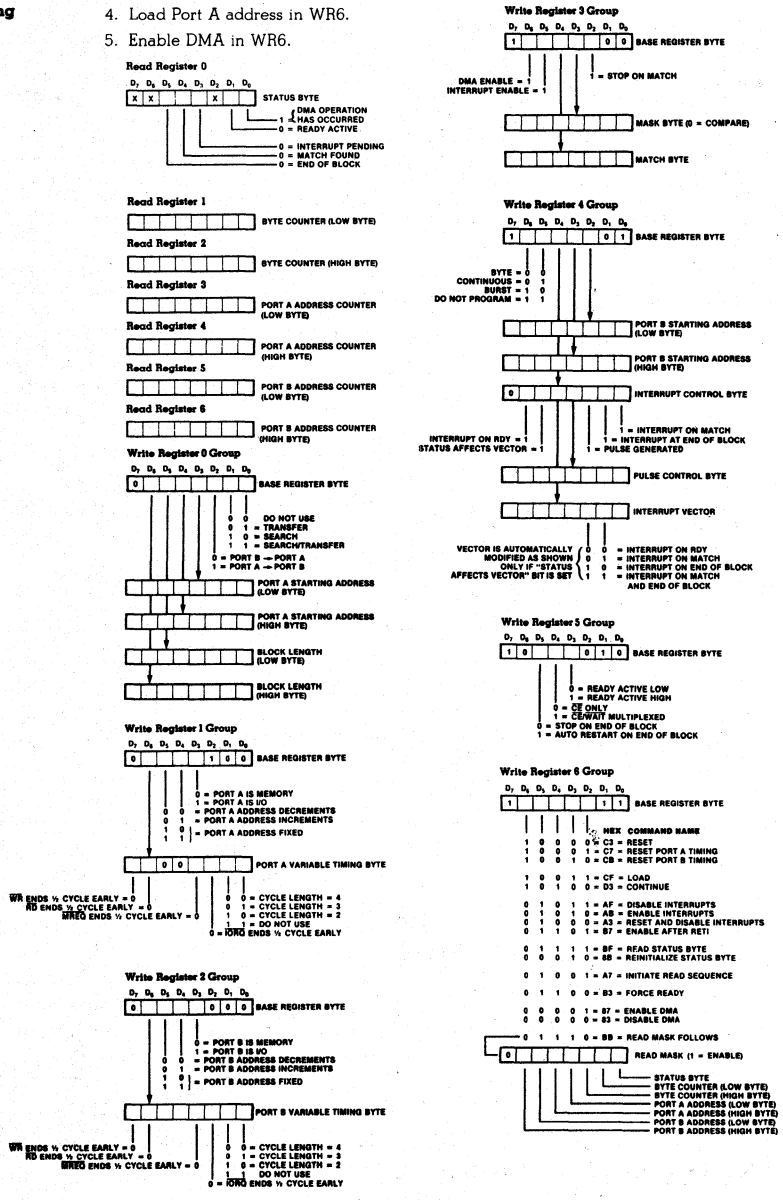
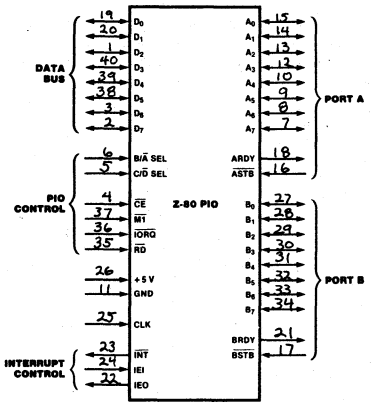


Figure 8b. Write Registers

Zilog

Z8420
Z80® PIO Parallel Input/Output Controller

Features



Pin Description

A_0-A_7. *Port A Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port A of the PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

ARDY. *Register A Ready* (output, active High). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

Input Mode. This signal is active when the Port A input register is empty and ready to accept data from the peripheral device.

Bidirectional Mode. This signal is active when data is available in the Port A output register for transfer to the peripheral device. In this mode, data is not placed on the Port A data bus, unless $\overline{ASTB}$ is active.

Control Mode. This signal is disabled and forced to a Low state.

$\overline{ASTB}$. *Port A Strobe Pulse From Peripheral Device* (input, active Low). The meaning of this signal depends on the mode of operation selected for Port A as follows:

Output Mode. The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

Input Mode. The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

Bidirectional Mode. When this signal is active, data from the Port A output register is gated onto the Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

Control Mode. The strobe is inhibited internally.

B_0-B_7. *Port B Bus* (bidirectional, 3-state). This 8-bit bus transfers data, status, or control information between Port B and a peripheral device. The Port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

B/$\overline{A}$. *Port B Or A Select* (input, High = B). This pin defines which port is accessed during a data transfer between the CPU and the PIO. A Low on this pin selects Port A; a High selects Port B. Often address bit A_0 from the CPU is used for this selection function.

BRDY. *Register B Ready* (output, active High). This signal is similar to ARDY, except that in the Port A bidirectional mode this signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

$\overline{BSTB}$. *Port B Strobe Pulse From Peripheral Device* (input, active Low). This signal is similar to $\overline{ASTB}$, except that in the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

C/$\overline{D}$. *Control Or Data Select* (input, High = C). This pin defines the type of data transfer to be performed between the CPU and the PIO. A High on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a *command* for the port selected by the B/$\overline{A}$ Select line. A Low on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often address bit A_1 from the CPU is used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally decoded from four I/O port numbers for Ports A and B, data, and control.

CLK. *System Clock* (input). The Z-80 PIO uses the standard single-phase Z-80 system clock.

D_0-D_7. *Z-80 CPU Data Bus* (bidirectional, 3-state). This bus is used to transfer all data and commands between the Z-80 CPU and the Z-80 PIO. D_0 is the least significant bit.

IEI. *Interrupt Enable In* (input, active High). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A High level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

Pin Description (Continued)

IEO. *Interrupt Enable Out* (output, active High). The IEO signal is the other signal required to form a daisy chain priority scheme. It is High only if IEI is High and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When $\overline{INT}$ is active the Z-80 PIO is requesting an interrupt from the Z-80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from Z-80 CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the Z-80 CPU and the Z-80 PIO. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt; the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. *Machine Cycle* (input from CPU, active Low). This signal is used as a sync pulse to control several internal PIO operations. When both the $\overline{M1}$ and $\overline{RD}$ signals are active, the Z-80 CPU is fetching an instruction from memory. Conversely, when both $\overline{M1}$ and $\overline{IORQ}$ are active, the CPU is acknowledging an interrupt. In addition, $\overline{M1}$ has two other functions within the Z-80 PIO: it synchronizes the PIO interrupt logic; when $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO is reset.

$\overline{RD}$. *Read Cycle Status* (input from Z-80 CPU, active Low). If $\overline{RD}$ is active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the Z-80 PIO to the Z-80 CPU.

Programming **Mode 0, 1, or 2.** *(Byte Input, Output, or Bidirectional).* Programming a port for Mode 0, 1, or 2 requires two words per port. These words are:

A Mode Control Word. Selects the port operating mode (Figure 6). This word may be written any time.

An Interrupt Vector. The Z-80 PIO is designed for use with the Z-80 CPU in interrupt Mode 2 (Figure 7). When interrupts are enabled, the PIO must provide an interrupt vector.

Mode 3. *(Bit Input/Output).* Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled), and three additional words, described as follows:

I/O Register Control. When Mode 3 is selected, the mode control word must be followed by another control word that sets the I/O control register, which in turn defines which port lines are inputs and which are outputs (Figure 8).

Interrupt Control Word. In Mode 3, handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits changes to the active level, an interrupt is triggered). Bit D_6 sets the logic function, as shown in Figure 9. The active level of the input bits can be set either High or Low. The active level is controlled by Bit D_5.

Mask Control Word. This word sets the mask control register, allowing any unused bits to be masked off. If any bits are to be masked, then D_4 must be set. When D_4 is set, the next word written to the port must be a mask control word (Figure 10).

Interrupt Disable. There is one other control word which can be used to enable or disable a port interrupt. It can be used without changing the rest of the interrupt control word (Figure 11).

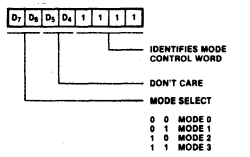


Figure 6. Mode Control Word

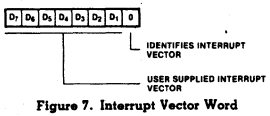


Figure 7. Interrupt Vector Word

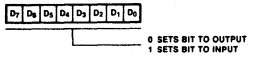


Figure 8. I/O Register Control Word

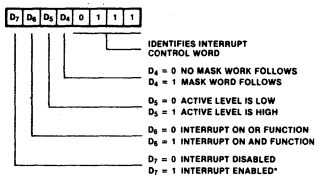


Figure 9. Interrupt Control Word

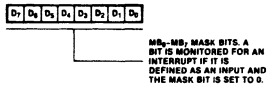


Figure 10. Mask Control Word

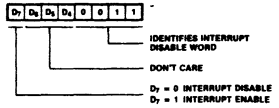
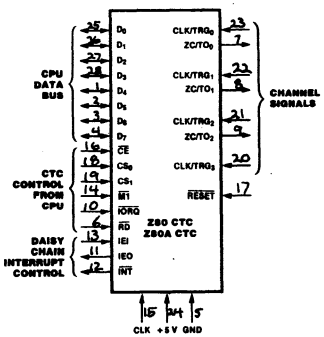


Figure 11. Interrupt Disable Word

Zilog

Z8430
Z80® CTC Counter/ Timer Circuit

Features



Pin Description

$\overline{CE}$. *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the down-counter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

CLK. *System Clock* (input). Standard single-phase Z-80 system clock.

CLK/TRG_0-CLK/TRG_3. *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z-80 CTC channels. In counter mode, every active edge on this pin decrements the down-counter. In timer mode, an active edge starts the timer.

CS_0-CS_1. *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A_0 and A_1).

D_0-D_7. *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z-80 CPU and the Z-80 CTC.

IEI. *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z-80 CPU.

IEO. *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z-80 CPU is not servicing an interrupt from any Z-80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). Low when any Z-80 CTC channel that has been programmed to enable interrupts has a zero-count condition in its down-counter.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z-80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ are active; the contents of the down-counter are read by the Z-80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z-80 data bus.

$\overline{M1}$. *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z-80 CPU is acknowledging an interrupt. The Z-80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

$\overline{RD}$. *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC.

$\overline{RESET}$. *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the Interrupt outputs go inactive; IEO reflects IEI; D_0-D_7 go to the high-impedance state.

ZC/TO_0-ZC/TO_2. *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z-80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the down-counter decrements to zero.

Programming

Each Z-80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z-80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 0 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed to Channel 0, and identified by a 0 in bit 0.

Addressing. During programming, channels are addressed with the channel select pins CS_1 and CS_2. A 2-bit binary code selects the appropriate channel as shown in the following table.

Channel	CS_1	CS_0
0	0	0
1	0	1
2	1	0
3	1	1

Reset. The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and D_0–D_7 go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits D_1 and D_2 set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if $D_3 = 0$, operation is triggered automatically when the time constant word is loaded.

Channel Control Word Programming. The channel control word is shown in Figure 5. It sets the modes and parameters described below.

Interrupt Enable. D_7 enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

Operating Mode. D_6 selects either timer or counter mode.

Prescaler Factor. (Timer Mode Only). D_5 selects factor—either 16 or 256.

Trigger Slope. D_4 selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

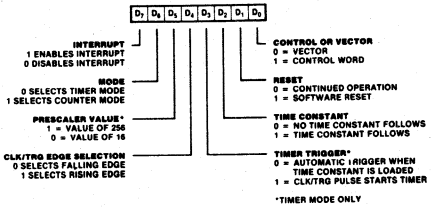


Figure 5. Channel Control Word

Programming (Continued)

Trigger Mode (Timer Mode Only). D_3 selects the trigger mode for timer operation. When D_3 is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse (T_2) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When D_3 is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse (T_2) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede T_2 by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle (T_3).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

Time Constant to Follow. A 1 in D_2 indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in D_2 indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with D_2 set.

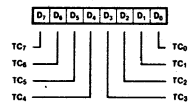


Figure 6. Time Constant Word

Software Reset. Setting D_1 to 1 causes a software reset, which is described in the Reset section.

Control Word. Setting D_0 to 1 identifies the word as a control word.

Time Constant Programming. Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that 00_{16} is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (ϕ)
- The prescaler factor (P), which multiplies the interval by either 16 or 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of $\phi \times P \times T$. The minimum timer resolution is $16 \times \phi$ (4 μs with a 4 MHz clock). The maximum timer interval is $256 \times \phi \times 256$ (16.4 ms with a 4 MHz clock). For longer intervals timers may be cascaded.

Interrupt Vector Programming. If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

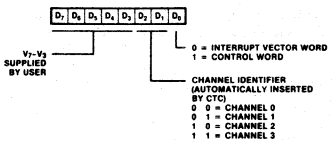
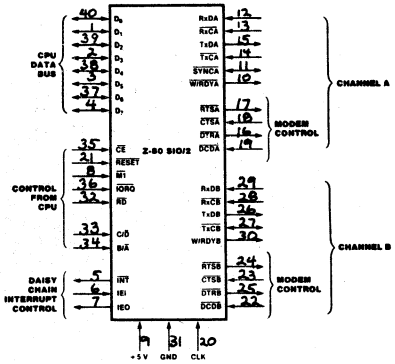


Figure 7. Interrupt Vector Word

Zilog

Z8440
Z80® SIO Serial Input/Output Controller

Features



Pin Description

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- Z-80 SIO/2 lacks $\overline{SYNCB}$
- Z-80 SIO/1 lacks $\overline{DTRB}$
- Z-90 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

B/$\overline{A}$. *Channel A Or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. *Control Or Data Select* (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The SIO uses the standard Z-80 System Clock to synchronize internal signals. This is a single-phase clock.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z-80 SIO. D_0 is the least significant bit.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into Z-80 SIO. They can also be programmed as general-purpose outputs.

In the Z-80 SIO/1 bonding option, $\overline{DTRB}$ is omitted.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. If $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

Pin Description (Continued)

$\overline{M1}$. *Machine Cycle* (input from Z-80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z-80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z-80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the Z-80 SIO/0 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. *Receive Data* (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. *Reset* (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{RTS}$ output goes Low. When the RTS bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z-80 SIO/2 bonding option, $\overline{SYNCB}$ is omitted.

$\overline{TxCA}$, $\overline{TxCB}$. *Transmitter Clocks* (inputs). In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z-80 CTC Counter Timer Circuit for programmable baud rate generation.

In the Z-80 SIO/0 bonding option, $\overline{TxCB}$ is bonded together with $\overline{RxCB}$.

TxDA, TxDB. *Transmit Data* (outputs, active High). Serial data at TTL levels. TxD changes from the falling edge of $\overline{TxC}$.

$\overline{W/RDYA}$, $\overline{W/RDYB}$. *Wait/Ready A, Wait/Ready B* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally-modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must not be combined with the pointing to any register.

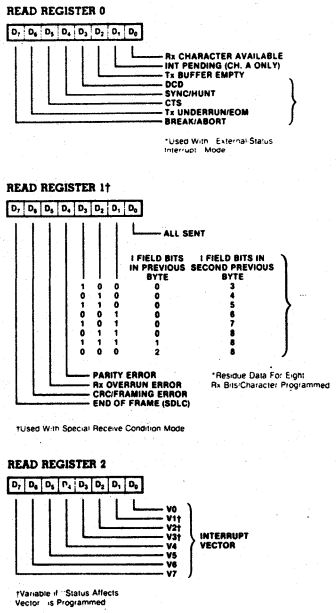


Figure 13. Read Register Bit Functions

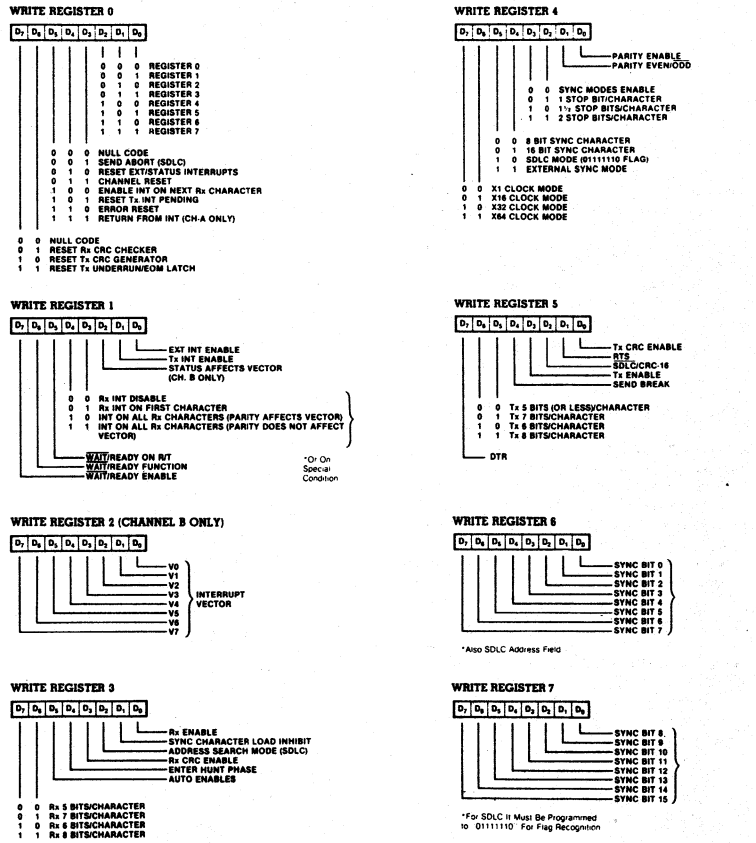


Figure 14. Write Register Bit Functions

TS 806C THEORY OF OPERATION

1.0 INTRODUCTION

The TS 806C is an intelligent tape-cartridge unit with its own controller designed to be used with the TS 806 service processor. The TS 806C has three ports: one of the ports (50 pin internal connector) is used to interface to the tape drive; one RS 422 port is used to communicate with the service processor; one RS 422 is used to pass the normal communications through to the work station. The service processor controls the communication links between the tape controller and the work station. The TS 806C receives commands from the TS 806 to perform tape read, write or erase functions; all other data is passed through to the work station.

The system block diagram is shown in Figure 1.

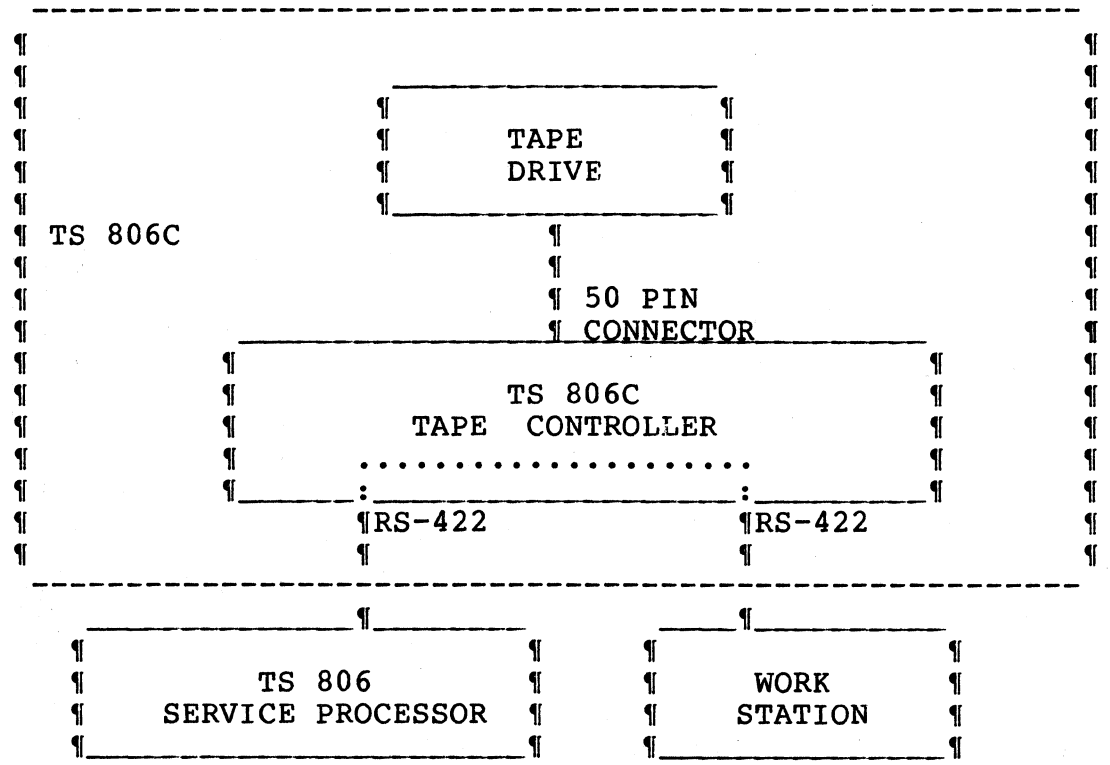


Figure 1 System Block Diagram

2.0 TS 806C TAPE CONTROLLER BOARD DESCRIPTION

The TS 806C controller board contains

Three Z80A family ICs

CPU, CTC and SIO

64 Kbytes of dynamic RAM

4 Kbytes of EPROM

Two 8-bit output latches

Associated control logic

See Figure 2.

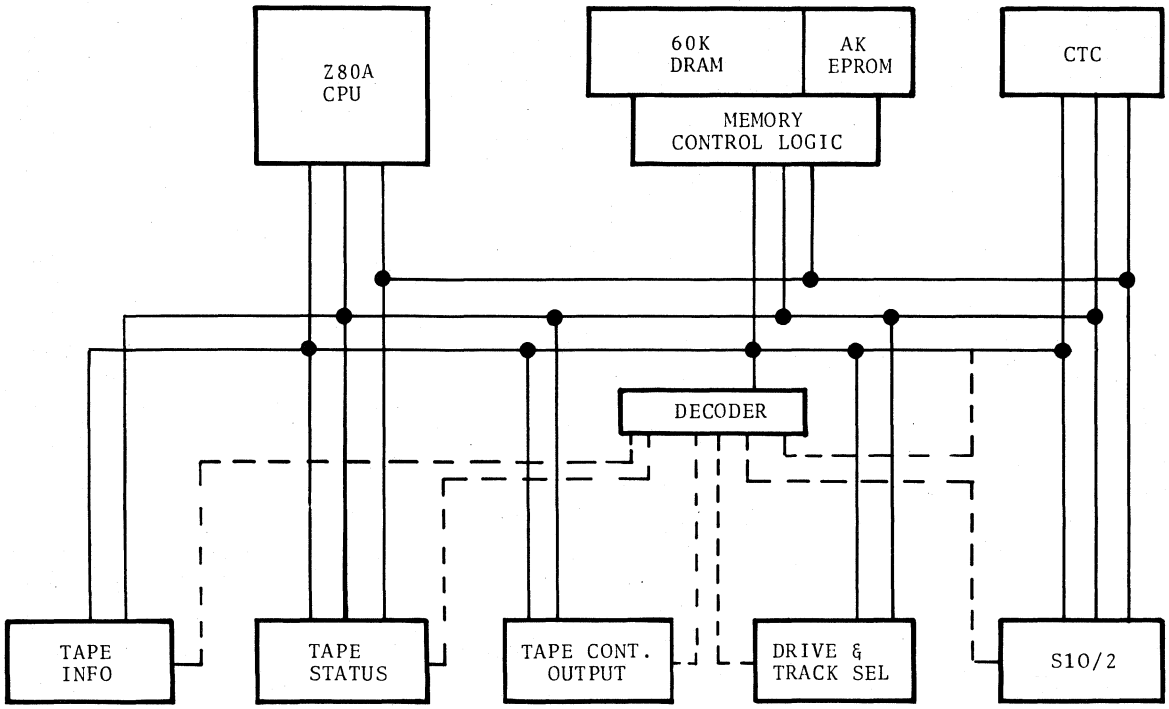


Figure 2 Block Diagram of TS 806C Controller Board

The Z80A ICs are driven by a 4 MHz system or tape clock. This clock is also used to generate the necessary timing for the memory control logic.

The Z80A CPU has a 16-bit address bus which can address up to 64 Kbytes for memory. The lower eight address lines are also used to address up 256 Input/Output devices. During instruction fetch cycles, the CPU sends out refresh addresses. The refresh enable address signals to the memory control which then refreshes 64 Kbytes of dynamic RAM.

A second bus is an eight-bit bidirectional data bus. The third bus is the control bus which includes the following signals:

-M1, -MREQ, -IORQ, -RD, -WR, -RFSH, -WAIT, -INT and -RESET. The TS 806C has eight I/O devices: the SIO, CTC, LEDs, a four-bit dipswitch, two tri-state input latches, and two 8-bit output latches.

The Z80A CTC is a four-channel programmable clocking device which can be programmed as a timer or as a counter. The main function of this CTC is to provide transmit clocks for the RS 422 communication interface. The CTC is programmed to reset the Z80 SIO which effects both channels of the SIO.

The Z80A SIO is a dual-channel serial I/O controller. It is programmed in the SDLC mode and clocked at a data rate of 800 Kbits/sec.

The main memory in the TS 806C controller contains eight 64K x 1 dynamic memory devices (only 60 Kbytes are accessible). There are four kilobytes of EPROM.

3.0 FUNCTION OF THE SYSTEM

The TS 806C generates an 8-MHz clock and a 4-MHz clock. These are supplied to the CPU, SIO, CTC, DMA and memory control logic. After power is first turned on, the system is reset to the idle state and all devices are then programmed for operation.

There are two different types of memory devices in the TS 806C, dynamic RAM and EPROM. See Figure 3.

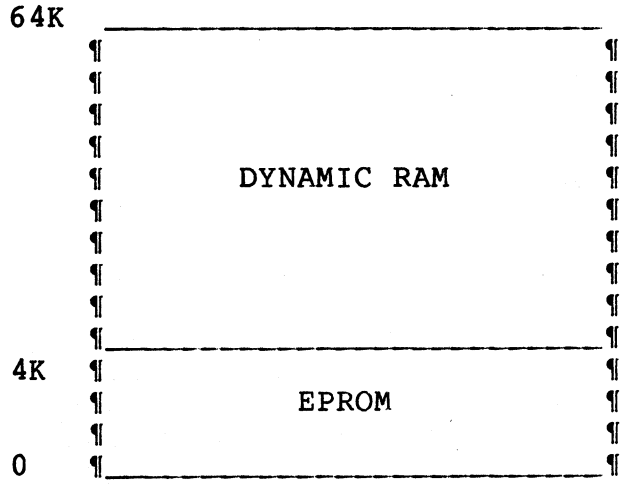


Figure 3 Memory Devices

The EPROM contains software for initialization of the controller, power-on diagnostics, and the download program.

The memory control logic supplies the necessary read/write signals, address latching signals, and refresh signal to the

dynamic RAM. Because of the speed difference between the access of the two types of memory, a one cycle "wait state" is inserted during read/write operations to the EPROM.

The daisy-chain style of communication makes it possible to reset the controller without effecting the link from the service processor to the work station.

4.0 OPERATION OF THE SYSTEM

The 16 MHz clock from the oscillator is counted down to 4 MHz by counter A14 (74LS 161A) and becomes the system clock frequency. This 4 MHz signal is sent to all the Z80A family devices and the memory control logic. The level of the clock signal is critical to the Z80A devices. The high level of the clock must be between 4.4 V and 5.3 V and the low level must be between -0.3 V and 0.45 V (see Figure 4). A transistor (2N2907) is used to pull the clock's output high level to about five volts.

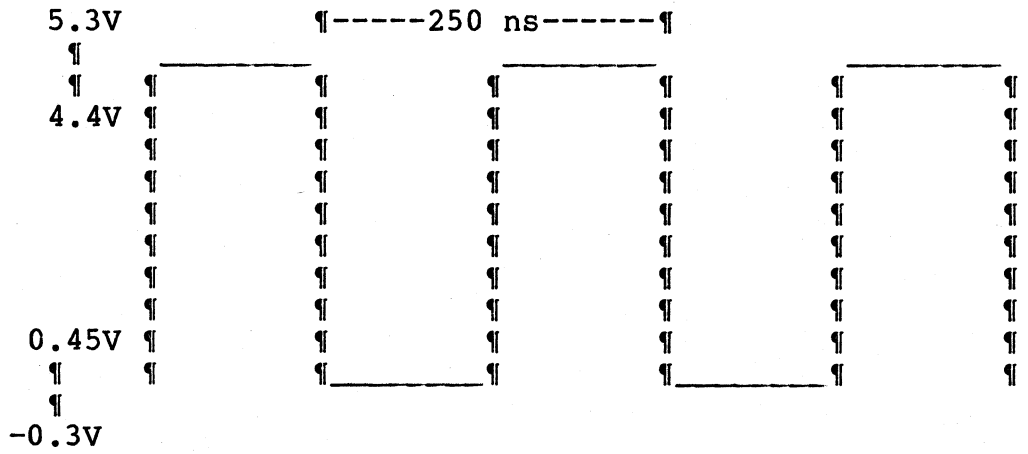


Figure 4 System Clock

Each dynamic RAM used in the TS 806C is organized as 65536 x 1 bits; eight dynamic RAMs are used on the controller board. Multiplexed addressing and periodic refreshing are required in the operation of this type of memory. The memory and refresh cycle diagram is shown in Figure 5.

The -MREQ and -RFSH signals from the CPU are sent to the memory control logic. The memory control logic is comprised of the following devices:

Three "D" flip-flops 74S74 (A41, A46)

Two nand gates 74S00 (A37)

Three nor gates 74LS02 (A38)

Two inverter gates 74LS04

Two three-input nor gates 74LS27 (A31)

Two multiplexers, A11 and A12 (74S157), are used to multiplex the 16-bit address lines from the CPU into the 8-bit address lines of the dynamic memory. The row address and column address are latched internally by the falling edge of the -RAS and -CAS signals. Each memory cell in the memory device must be refreshed at least every two milliseconds. A serial resistor (33 ohm) is connected to the address line signal, the write signal, the -RAS signal, and the -CAS signal on the input to the dynamic memory. The purpose of these resistors is to reduce the signal under-shoot caused from the capacitance of the devices.

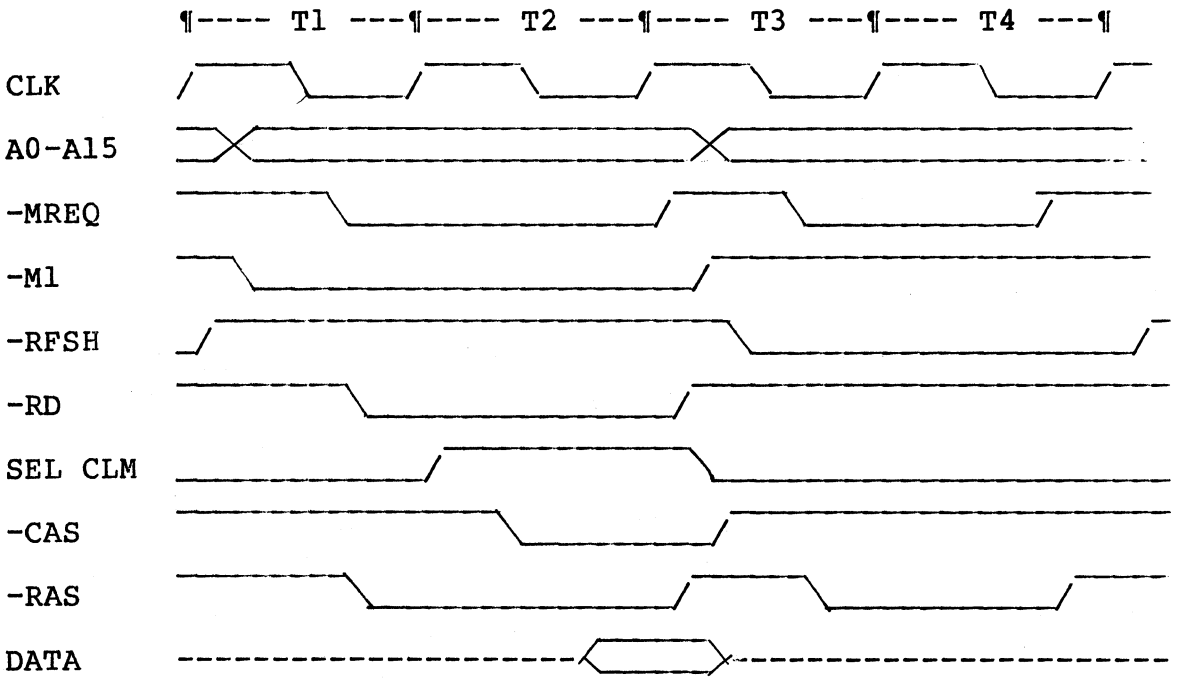


Figure 5 Memory and Refresh Cycle

The other type of memory used in this system is the EPROM. Since the EPROM has a slower access time compared to the Z80A memory access cycle, one "wait state" is automatically inserted by the "wait control circuit" when the EPROM is accessed. The memory latch timing diagram is shown in Figure 7. The "wait control circuit" is implemented with two "D" flip-flops (74LS74 A34), one three-input nor gate (74LS27 A31), and one inverter gate (74LS04 A30).

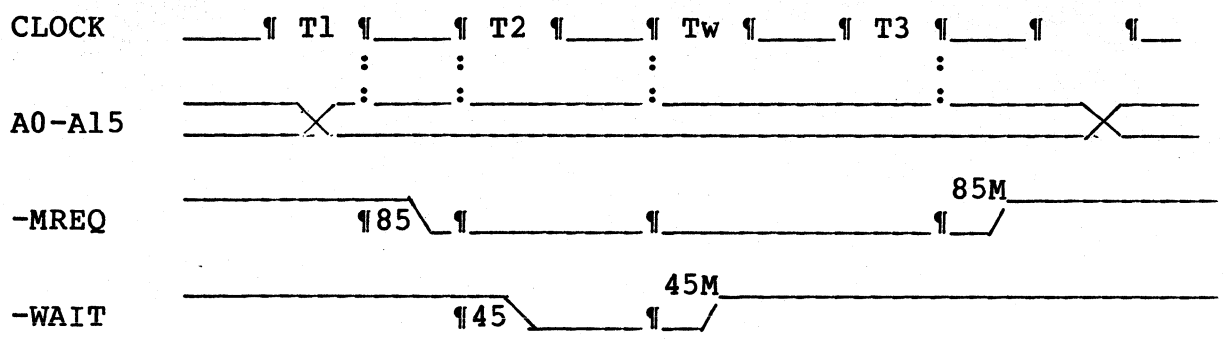


Figure 6 Wait Cycle Inserted Timing

The TS 806C controller board has eight logical I/O devices. They are the LED, CTC, SIO, four-bit dipswitch, two tri-state input buffers, and two output latches. During CPU I/O operations, the address bus is decoded by A26 (74LS138 IC) to select one of the I/O devices. The LED and tape select have the same port address but different times of use.

4.1 TAPE OPERATION

The data latches (A23 and A28) are used to latch the data word that controls the tape drive operation.

4.1.1 Output Latches (from the computer)

The control signals to the tape drive are programmed by two data latches. These latches are write-only ports.

4.1.1.1 Tape Output Latch 2

Tape Output Latch 2 controls the track select and, if in a multiple drive system, the drive select.

Data word for "Tape output latch 2"

D07	D06	D05	D04	D03	D02	D01	D00
-TR2	-TR1	-SL4	-SL2	-SL1	X	X	X

Track select is controlled via D07 and D06 according to the following chart with low being true. All heads for a given track (read, write, and erase) are selected simultaneously through the use of these control bits. The last track selection is stored in the tape drive even after deselection by the controller.

Track No.	Track Select Signals	
	TR2	TR1
1	H	L

2	L	H
3	L	L
4	H	H

Tape drive select is controlled via D05, D04, AND D03. Together these bits determine the tape drive address (low true). The address function processes and remains active during any other drive I/O. The following chart shows the address selection.

Drive No.	Drive Select Signals		
	SL4	SL2	SL1
1	H	H	L
2	H	L	H
3	H	L	L
4	L	H	H
5	L	H	L
6	L	L	H
7	L	L	L
8	H	H	H

Data bits D02, D01, and D00 are not used and do not effect the system.

4.1.1.2 Tape Output Latch 1

The Tape Output latch 1 is called the **Tape Command/Control Output Latch (14H).**

Data Word for Output Latch 1

¶ SLG ¶	X ¶	-RWD ¶	FB ¶	-WEN ¶	-HSP ¶	-FWD ¶	-REV ¶
---D7----	D6-----	D5-----	D4-----	D3-----	D2-----	D1-----	D0---

Reverse direction (-REV) is D00. Active low causes the tape to move in the reverse direction.

Forward direction (-FWD) is D01. Active low causes the tape to move in the forward direction.

High speed (-HSP) causes the tape to move at high speed in the direction selected.

Tape motion continues until command signals go false. This can be triggered by the end of the tape (when going forward) or the beginning of the tape (when in reverse). The tape will also stop if both directions are given at the same time, if the ready signal goes inactive, and if a higher priority rewind command is given.

When in high speed motion, the speed will drop to low speed if the upper loading point hole is sensed in the reverse direction or if

the upper early warning hole is sensed in the forward direction.

Write enable (-WEN) enables writing and erasing functions for the selected track. The writing or erasing operations is only allowed if the tape cartridge is in the unprotected state. Write enable should be set prior to the tape going in motion and should not be reset until the drive has stopped. At least two milliseconds are needed between the reset of write enable and the selection of a new track. The write enable signal is reset by either reverse or high speed commands.

Feedback (FB) is for general use and can also be read through port 0CH at D04.

Rewind (-RWD) causes the tape to be positioned at the beginning at high speed. The drive must be selected to start a rewind but may be deselected after the sequence has started.

Data bit D06 is not used.

Select gate (SLG) allows selection per the select and address codes. It is used to prevent unwanted selection during the change of a select operation.

4.1.2 Input Latches (to the controller)

The status of the tape controller is read through two input ports. These ports are read-only status line which are latched by the tape drive.

4.1.2.1 Tape Status Input Latch 1

Input Latch 1 is called the **Tape Status Input Latch (08H).**

Data word for the Tape Status Input Latch

¶ RDY	¶ LPS	¶ EWS	¶ FLG	¶ FUP	¶ WEN	¶ BSY	¶ SLD ¶
--D07	---D06	---D05	---D04	---D03	---D02	---D01	---D00--

Ready (RDY) is true when the tape cartridge is installed, the sensor lamp is drawing current and five volts is applied to the tape drive.

Load point sensed (LPS) is set and latched when the upper load point hole (the warning for the start of the tape) is passed in the reverse direction. The signal is reset when the load point is passed with the tape going in the forward direction. When this signal is true, the high speed signal is disabled in the reverse direction. At this time, reverse tape motion is allowed to proceed until the beginning of tape hole is encountered. When this happens, the drive stops and only accepts forward commands.

Early warning sensed (EWS) is set and latched when the upper early warning hole (warning for end of the tape) is passed in the

forward direction. This signal is reset when the hole is passed in the reverse direction. When this signal is true, the high speed signal is disabled and forward motion is allowed to proceed until the end of tape hole. When this happens, the tape stops and only accepts reverse direction commands.

Flag (FLG) is set when the automatic sequence to position the tape at the beginning has been executed or a rewind command has been completed. This signal is reset by a subsequent receipt of a forward command.

File unprotected (FUP) is true when a tape cartridge is installed and it is in the unprotected state (meaning the tape can be written on).

Write enable (WEN) is true when a write enable is latched within the tape drive.

Busy (BSY) is true when the drive is performing an automatic rewind sequence (a cartridge is initially installed), normal rewind, forward or reverse command. This signal goes true when the command is received and remain true until tape motion has stopped. The time for slow speed commands is 30 milliseconds and for high speed commands is 80 milliseconds.

Selected (SLD) is true when the tape drive has received its proper address.

4.1.2.2 Tape Information Latch 2

Input latch 2 is called the **Tape Information Input Latch (OCH).**

Data word for Tape Information Input Latch 2

¶ SIO-A	¶ DIAG	¶ DAD	¶ FB	¶ X	¶ X	¶ X	¶ X	¶
D07	D06	D05	D04	D03	D02	D01	D00	

The SIO ready signal for channel A is represented here.

Diagnostic (DIAG) is reserved for starting the diagnostic routines. These routines can be initiated by power-up or reset.

Data Detected (DAD) is true when the data has been detected during a read from the tape cartridge at either low or high speed.

Feedback (FB) is the same as bit four in "Tape output status 2".

4.2 DATA COMMUNICATION WITH THE TAPE DRIVE

The preamble for tape data is 39 zeros (0) followed by a one (1) at the beginning of each data block. The postamble is the

reverse of this with a one (1) followed by 39 zeros (0) at the end of each data block. The preamble is stripped from the read data when data is being read in the forward direction. The postamble is stripped from the read data when the data is read in the reverse direction.

Example of a data block on the tape cartridge:

39 'ZEROS'¶ 1 'ONE'¶ ADDRESS ¶ DATA ¶ 1 'ONE'¶ 39 'ZEROS'¶

To create preambles and postambles, -DTR must be low on the SIO for the equivalent of a five-byte transmission time before and after the data is transmitted. During data transfer, -DTR is at a high level.

5.0 Input/Output Port Assignments and Timing

5.1 Input/Output Port Addresses

- General Purpose Switch ---------- 00H --> 03H
- CTC Channel 0 ---------- 04H
- CTC Channel 1 ---------- 05H
- CTC Channel 2 ---------- 06H
- CTC Channel 3 ---------- 07H
- Tape Input-Status ---------- 08H --> 0BH
- Tape Input-Info. ---------- 0CH --> 0FH
- LED ---------- 10H --> 13H
- Tape Select (Drive and Track) ------- 10H --> 13H
- Tape Command/Control ---------- 14H --> 17H
- SIO Channel A (Data) ---------- 18H
- SIO Channel A (Command/Status) ------ 19H
- SIO Channel B (Data) ---------- 1AH
- SIO Channel B (Command/Status) ------ 1BH
- Party Line Priority Controller ------ 1CH --> 1FH

5.2 Memory Latch Timing

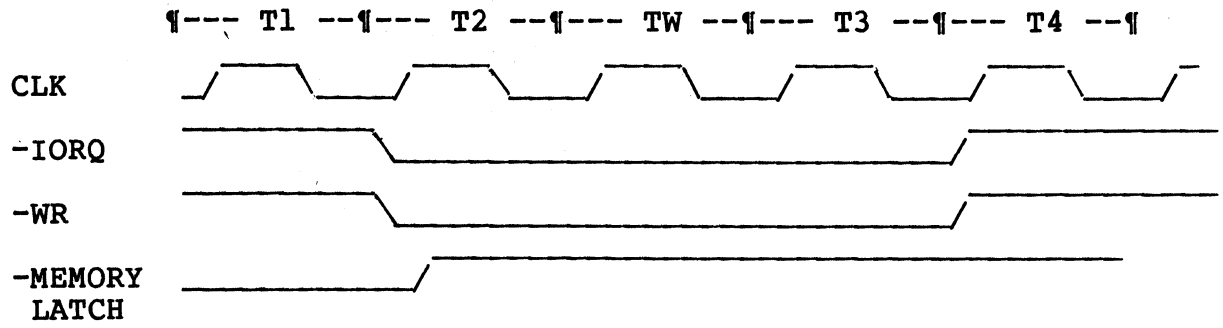


Figure 7 Memory Latch Timing

5.3 SI/O Read/Write Cycle

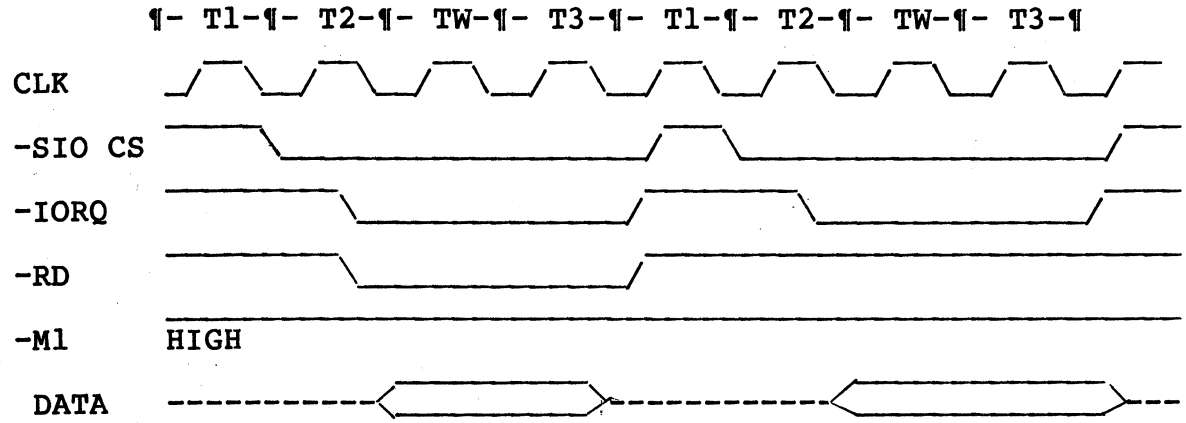


Figure 8 SI/O Read/Write Cycle

6.0 Connector Description

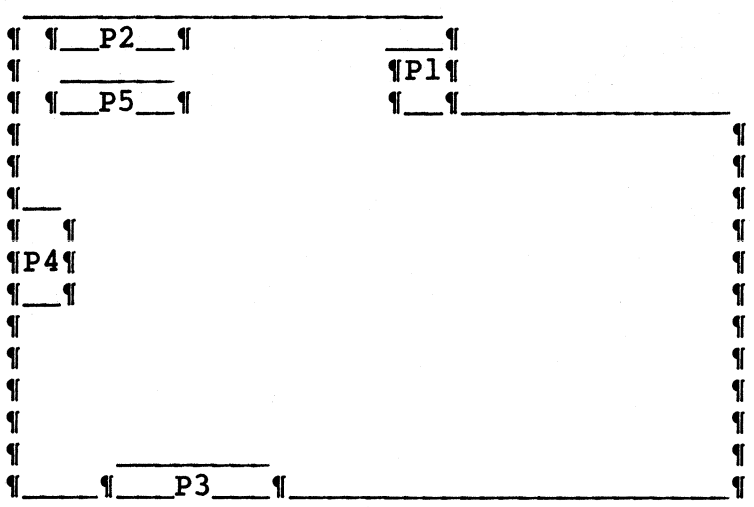


Figure 9 Connector Positions

Legend

Connector No.	Description
P1	POWER CONNECTOR
P2	RS422 CONNECTOR (TS806)
P5	RS422 CONNECTOR (TS800)
P3	TAPE INTERFACE CONNECTOR
P4	RESET SWITCH CONNECTOR (OPTION)

6.1 P1 Power Connector (5-Pin Wafer)

Pin No.	Description
1	- 12 V
2	UNUSED
3	GROUND
4	+ 5 V
5	+ 12 V

6.2 P2, P5 Communication Ports RS 422

(16 pin header on the PCB), (Rear panel 15 pin D-type conn.)

D-conn.	Header	Description
1	1	GND
9	2	-TxD
2	3	+TxD
10	4	-RxD
3	5	+RxD
11	6	+RTS
4	7	-RTS
12	8	+CTS
5	9	-CTS
13	10	-TxC
6	11	+TxC
14	12	-RxC
7	13	+RxC
15	14	Test
8	15	GND
-	16	NC

6.3 P3 Tape Connector (50 Pin St. Header)

Pin No.	Signal	I/O
2	-SLD	I
4	-RDY	I
6	-WND	I
8	-FLG	I
10	-LPS	I
12	-FUP	I

14	-BSY	I
16	-EWS	I
18	-RWD	O
20	-REV	O
22	-FWD	O
24	-HSP	O
26	-WEN	O
28	-SL1	O
30	-SL2	O
32	-SL4	O
34	-SLG	O
36	-RNZ	I
38	-RDS	I
40	-DAD	I
42	-WDE	O
44	-WNZ	O
46	-TR2	O
48	-WDS	I
50	-TR1	O

NOTE

All odd numbered pins are ground.

6.4 P4 Reset Connector (5-Pin Wafer) (Option)

PIN	DESCRIPTION
1	NC (Option for lighted switch)
2	Void (No pin)
3	Reset Signal
4	Ground
5	NC (Not used)

7.0 SPECIFICATIONS

- Power Requirement --------- 1.08 Amp @ +5 V
- Power Consumption --------- TYPICAL 5.4 Watts
- System Clock -------------- 4 MHZ
- Memory
  - 60 Kbytes of dynamic RAM
  - 4 Kbytes of EPROM
- Tape Communication
  - SDLC Mode
  - 192 Kbits/sec (supplied by tape drive)
- TS 806 Communication (RS 422)
  - SDLC / Asynchronous mode
  - Fix Rate of 800 Kbits/sec

. Interrupt Priority
    . 1st Priority ------ SIO
    . 2nd Priority ------ CTC

SYSTEM REPAIR PRICE AND SPARE PARTS PRICE LISTS

This section contains the Repair Price List for Computers and the Systems Spare Parts Price List in effect at the printing date of this manual. Use these lists for estimating repairs: prices are subject to change without prior notice.

Repairs Price List for Computers

March 1, 1983

DESCRIPTION	PRICE
Logic Board TS 800 (Obsolete)	$ 135.00
Logic Board TS 800A, 802, 802H	150.00
Logic Board TS 801 (Obsolete)	175.00
Logic Board TS 806, 806/20	250.00
Logic Board TS 816, 816/40	350.00
Logic Board TS 1602G, 1602GH	400.00
Graphics Board TS 1602G, 1602GH	175.00
Floppy Controller (Daughter Board) TS 802, 802H	50.00
Winchester Disk Controller (5" Drive & 40MB 8" Drive)	175.00
Tape Controller TS 806C	95.00
Interface Board TS 816U	50.00
Keyboard TS 800, 800A, 802, 802H	50.00
Keyboard TS 1602G, 1602GH	50.00
Power Supply Module TS 800, 800A	50.00
Power Supply TS 802, 802H, 806, 806H, 816, 1602G	110.00
Video Module TS 800, 800A, 802, 802H, 1602G, 1602GH	50.00
Floppy Disk Drive 5"	160.00
Winchester Disk Drive 5"	160.00
Winchester Disk Drive 8"	450.00
Tape Drive	300.00
Picture Tube Broken P31	214.00
Picture Tube Broken P39	230.00
Top Case Broken TS 802, 800A, 1602G	80.00
Bottom Case Broken TS 802, 800A, 1602G	100.00
Top or Bottom Case Broken Computer Boxes TS 806, 816	80.00
Front or Rear Panel Broken	60.00
Basic Repair charge (This additional amount charged when an entire system is returned for repair)	70.00

TeleVideo will bill per above price schedule when no trouble is found in the module returned for repair.

Out of Warranty

Customer to return defective replaceable module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send replacement repaired module, billing per above price schedule plus return freight.

Prices subject to change without notice.

TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

Eastern Region—(212) 308-0705 • Northeast Region—(617) 369-9370 • Midwest Region—(312) 969-0112
South Central Region—(214) 258-6776 • Southwest Region—(714) 752-9488 • Northwest Region—(408) 745-7760
Southeast Region—(404) 447-1231 • European Sales—(31) 075-28-7461 TLX:844-19122
U.K./Scandinavian Sales—(44) 0908-668778 TLX:851-825151

Systems Spare Parts Price List

TeleVideo Systems, Inc.

TELEVIDEO COMPUTER SYSTEMS
SPARE PARTS PRICE LIST

05-10-83

PART NUMBER	PRICE	DESCRIPTION
		MANUALS [class A]
2004200	20.00	Guide, Installation & User's TS 800A
2003700	20.00	Guide, Installation & User's TS 802
2003900	20.00	Guide, Installation & User's TS 802H
2248100	20.00	Guide, Installation & User's TS 803
2133700	20.00	Guide, Installation & User's TS 1602G
2133800	20.00	Guide, Installation & User's TS 1602GH
2248600	20.00	Guide, Installation & User's TS 1603
2003000	10.00	Guide, Installation & User's TS 806
2226500	20.00	Guide, Installation & User's TS 806/20
2004700	10.00	Guide, Installation & User's TS 806C
2002300	10.00	Guide, Installation & User's TS 806H
2232000	20.00	Guide, Installation & User's TS 806H/20
2004100	10.00	Guide, Installation & User's TS 816
2226400	20.00	Guide, Installation & User's TS 816/40
2150300	50.00	Guide, User's TELEPLAN
2200200	20.00	Manual, Operator's Tele3780
2219700	40.00	Manual, TeleDBMS
2003200	25.00	Manual, Mmmost
2003400	50.00	Manual, CP/M
2162400	50.00	Manual, CPM/86
2150400	40.00	Manual, TeleVideo - COBOL
2133900	50.00	Manual, Maintenance TS 800A, 802, 802H
2230700	50.00	Manual, Maintenance TS 806/20, 806, 806C & H
2131400	50.00	Manual, Maintenance TS 816
2259000	50.00	Manual, Maintenance TS 1602G/GH
2291000	50.00	Manual, Maintenance TS 803
		KITS [class B]
2000700	300.12	Kit, Spare Parts, Logic Board 8 Bit Systems *
2252100	703.50	Kit, Spare Parts, Logic Board 16 Bit Systems *
2202900	244.80	Kit, Spare Parts, Logic Board WDC *
2203000	199.59	Kit, Spare Parts, Logic Board FDC *
2252000	401.40	Kit, Spare Parts, Graphics Board TS 1602G *
2280700	153.28	Kit, Spare Parts, Video Mod ts 800A *
2202800	90.88	Kit, Spare Parts, Mechanical TS 802/800A*
2228400	235.72	Kit, Spare Parts, Data Cables TS 816's*
2270800	223.08	Kit, Spare Parts, Data Cbls TS 806 & User Stat *

* Contents of Kits at end of List

05-10-83

PART NUMBER	PRICE	DESCRIPTION
		MAJOR ASSEMBLIES/PRINTED CIRCUIT BOARDS [class B]
2198900	1,474.14	PCB Asy Mod 8" Flpy TS 801
2018000	1,199.67	PCB Asy Logic Board TS 800A,802
2018001	1,199.67	PCB Asy Logic Board TS 802H
2226000	1,047.78	PCB Asy Logic Board TS 803,800
2020400	2,157.93	PCB Asy Logic Board TS 1602G
2022000	1,529.10	PCB Asy Logic Board TS 1603
2012000	1,251.12	PCB Asy Logic Board TS 806 TS 806/20
2017501	658.32	PCB Asy Logic Board TS 806C
2012500	1,765.83	PCB Asy Logic Board TS 816
2012501	1,403.05	PCB Asy Logic Board TS 816/40
2013000	360.00	PCB Asy Logic Board TS 816U
2195800	93.00	Video Module TS 800A,802
2226900	72.00	Video Module TS 803,1603
2013500	866.19	PCB Asy 5" Winchester Disk Controller (806, 806/20)
2013501	866.19	PCB Asy 8" Winchester Disk Controller (816/40)
2017000	210.75	PCB Asy Floppy Disk Cont TS 802 (Daughter Bd)
2019000	656.87	PCB Asy Graphics TS 1602G
2109200	654.00	Power Supply Switching 100W TS 806,806/20
2109201	827.34	Power Supply Switching 150W TS 802,802H,1602G
2129202	954.00	Power Suppy Switching 200W TS 816,806C
2191500	103.00	Power Supply 3A/5V TS 800A (TS 800 OBS)
2227500	275.04	Power Supply 120W TS 803,1603
2227400	63.84	Power Supply Transformer TS 1603,803
2304000	288.00	Power Supply (OPC) TS 1602/SGH,802S
2304800	288.00	Power Supply (OPC) TS 803H,1603H
2294000	288.00	Power Supply (OPC) TS 806S/20
2299100	324.84	Power Supply (OPC) TS 816/40
		STORAGE DEVICES [class C]
2099200	591.00	Floppy Drive 48 TPI D/S 5 1/4" .5 MB Full Height
2221300	399.00	Floppy Drive 48 TPI D/S 5 1/4" .5 MB Half Height
2252300	489.00	Floppy Drive 96 TPI D/S 5 1/4" 1.0 MB Half Height
2198800	1,800.00	Disk Drive Winchester 5 1/4" 20 MB
2099400	4,140.00	Disk Drive Winchester 8" 23 MB
2220300	4,575.00	Disk Drive Winchester 115V 8" 40 MB
2220100	4,575.00	Disk Drive Winchester 230V 8" 40 MB
2099500	2,100.00	Tape Drive W/Codec Bd 14 MB

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PART NUMBER	PRICE	DESCRIPTION
		MISC. MAJOR PARTS [class D]
2049300	179.00	Picture Tube Black/Green 12" P31
2173800	192.00	Picture Tube Black/Green 12" P39 Graphics (1602G)
2218700	192.00	Picture Tube Black/Green 14" P31P
2090200	175.00	Detachable Keyboard TS 800A/802 *
2183701	210.00	Detachable Keyboard TS 1602G *
2183700	210.00	Detachable Keyboard TS 803/1603 *
2099800	70.20	Case Bottom TS 806/806-20/RWP
2099900	70.20	Case Top TS 806/806-20/RWP
2100600	110.00	Case Top TS 802/1602G
2100700	85.00	Case Bottom TS 802/1602G
2100800	40.00	Bezel TS 802/1602G
2141700	70.20	Case Bottom TS 800A
2141800	97.80	Case Top TS 800A
2141900	20.00	Bezel TS 800A
2103100	70.00	Case Top TS 816/816-40
2103200	180.00	Case Bottom TS 816/816-40
2188300	16.32	Case Back Cover Crt TS 803/1603
2188500	71.16	Case Main Elect. TS 803/1603
2188600	66.00	Case CRT TS 803/1603
2188800	15.48	Bezel TS 803/1603
2189100	10.68	Case Arm Top TS 803/1603
2189200	.12	Case Arm Bottom TS 803/1603
2218800	1.44	Thumb Wheel Adj TS 803/1603
2291100	26.10	Power Cord TS 803/1603

* ORDER APPROPRIATE LABELS FROM LABELS/LOGO'S (PAGE 7)

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PART NUMBER	PRICE	DESCRIPTION
		FIRMWARE
8000002	16.92	IC 2332 Char Gen Upper Character Cell
8000003	16.92	IC 2332 Char Gen Lower Character Cell
8000009	23.28	IC 8048 With Program ROM for Keyboard TS 800A/802
8000016	15.0	IC charicter Gen. for Graphics Systems
8000018	34.50	IC 2716 System Program EPROM Kybd TS 800A/802
8000045	37.50	IC System Program EPROM Z80 Portion TS 800A/802
8000046	37.50	IC System Program EPROM Lower Terminal Firmware
8000047	37.50	IC System Program EPROM Higher Terminal Firmware
8000050	37.50	IC System Program EPROM Z80 Portion TS 802H
8000024	55.80	IC System Program EPROM 450ns TS 806
8000053	30.90	IC System Program EPROM 450ns TS 816
8000106	30.90	IC System Program EPROM 450ns TS 816/40
8000054	30.90	IC System Program EPROM 450ns TS 806C
8000093	24.00	IC System Program EPROM 450ns TS 1602G/GH
8000080	5.40	IC Memory Decode TS 1602G
8000079	5.40	IC I/O Decode TS 1602G
8000027	55.80	IC Diagnostic EPROM TS 806
8000052	55.80	IC Diagnostic EPROM TS 806C
8000096	55.80	IC Diagnostic EPROM TS 816
8000107	55.80	IC Diagnostic EPROM TS 816/40
8000035	23.70	IC L2-7 System Program ROM WDC (74S472 512 X 8)
8000036	23.70	IC MX-7 System Program ROM WDC (74S472 512 X 8)
8000037	23.70	IC FX-7 System Program ROM WDC (74S472 512 X 8)
8100024	100.00	Listing System Program TS 806 *
8100045	100.00	Listing 800A, 802, [Z80 Portion] *
8100046	500.00	Listing 800A, 802, 802H [6502 Portion] *
8100050	100.00	Listing TS 802H [Z80 Portion] *
8100053	100.00	Listing System Program EPROM TS 816 W/Code *
8100054	100.00	Listing System Program EPROM TS 806C *
8100093	100.00	Listing System Program EPROM TS 1602G/GH *

* Require non-disclosure agreements and letter of intended use.

		CABLES/CONNECTORS/WIRE ASSEMBLIES
2005700	25.44	Cbl Asy, Keyboard TS 800A/802
2006800	14.22	Cbl Asy, 20 Pin 12" TS 802H WDC To Winchester
2006900	18.60	Cbl Asy, 34 Pin 15" TS 802H Daughter Bd/Floppy WDC/Winch
2007001	32.28	Cbl Asy, 40 Pin 16" TS 802H Daughter Bd To WDC
2007300	29.16	Cbl Asy, 34 Pin 14" TS 802 Daughter Bd To Floppy
2006100	11.88	Cbl Asy, 40 Pin 2" TS 802/H Logic to Daughter Bd
2006901	18.96	Cbl Asy, 34 Pin TS 806 Logic To Floppy/WDC To Winch
2007000	20.28	Cbl Asy, 40 Pin 13" TS 806 Logic To WDC
2006801	14.52	Cbl Asy, 20 Pin 15" TS 806-816/40 WDC To Winchester
2006501	11.34	Cbl Asy, 16 Pin 8" TS 806 RS 422 To Logic
2006600	36.00	Cbl Asy, 34 Pin 7" TS 806 Parallel Printer
2006400	24.12	Cbl Asy, 50 Pin 16" TS 816 WDC To Winchester

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PART NUMBER	PRICE	DESCRIPTION
2006201	20.10	Cbl Asy, 14" TS 816U To Logic, Logic To Tape
2006601	30.54	Cbl Asy, 34 Pin 8" TS 816 Parallel Printer
2006500	32.70	Cbl Asy, 16 Pin 3" TS 806C RS 422 Internal
2007100	51.00	Cbl Asy, 50 Pin 3" TS 806C Logic Board To Tape Drive
2007101	42.00	Cbl Asy, 20 Pin 12" TS 806 Internal For TS 806H
2007800	73.08	Cbl Asy, 34 Pin 16" TS 806 Internal For TS 806H
2128500	19.32	Cbl Asy, 20 Pin 10" TS 806H External to TS 806
2006300	23.40	Cbl Asy, 34 Pin 10" TS 806H External to TS 806
2007600	42.60	Cbl Asy, 20 Pin 12" TS 806H Internal for Winchester
2007700	54.00	Cbl Asy, 34 Pin 10" TS 806H Internal for Winchester
2135700	15.84	Cbl Asy, 50 Pin TS 1602G Logic to Graphics
2007002	38.22	Cbl Asy, 40 Pin 21" TS 816/40 Logic to WDC
2006204	27.42	Cbl Asy, 50 Pin 10" TS 816/40 Logic to Tape/Logic to 816U
2006200	21.30	Cbl Asy, 50 Pin 8" TS 816/40 Logic to WDC
2006404	31.50	Cbl Asy, 50 Pin 22" TS 816/40 WDC to Winchester
2224300	28.00	Cbl Asy, 34 Pin 4" TS 816/40 Parallel Printer
2235400	81.60	Cbl Asy, 25 Pin TS 816/40H External to TS 816/40
2160700	158.46	Cbl Asy, 50 Pin TS 816/40H External to TS 816/40
2235500	39.72	Cbl Asy, 25/20 Pin TS 816/40 Internal for TS 816/40H
2160800	150.06	Cbl Asy, 50/57 Pin TS 816/40 Internal for TS 816/40H
2161000	57.66	Cbl Asy, 50/57 Pin TS 816/40H Internal for Winchester
2235600	42.36	Cbl Asy, 25/20 Pin TS 816/40H Internal for Winchester
2008600	28.00	Harness Asy, Power TS 802H
2007900	28.00	Harness Asy, Power Cable 16" TS 806
2136500	28.00	Harness Asy, Power Cable 12" TS 806
2008000	12.84	Harness Asy, Power Cable 24" TS 816
2008101	69.60	Harness Asy, Tape Cassette Power-1
2008201	28.08	Harness Asy, Tape Cassette Power-2
2176200	50.00	Harness Asy, Power TS 816
2008800	28.00	Harness Asy, Winchester Serv. Board TS 816
2008900	28.00	Harness Asy, Tape Cassette Power 1 & 2
2136702	41.88	Harness Asy, TS 816/40
2192901	40.44	Harness Asy, TS 816/40
2008400	10.20	Harness Asy, 1.00 Reset Switch 3 Pin 14"
2008401	20.40	Harness Asy, 1.00 Reset Switch 3 Pin 15"
2008700	30.36	Harness Asy, Power Floppy General 14"
2097900	2.22	RJ11 Connector Female PCB Mount (AMP)
2141200	3.89	RJ12 Connector Female PCB Mount 6 Pin
2208400	2.82	RJ12 Modular Jack
2098000	9.60	Connector 15 Pin D-Sub Female PCB Mount RS422
2163100	24.24	Connector 15 Pin S-Sub Metal Female PCB Mount RS422
2097800	10.62	Connector 25 Pin D-Sub Female PCB Mount RS232
2165300	29.04	Connector 25 Pin D-Sub Metal Female PCB Mount RS232
2098100	.72	Connector 3 Pin Header - Straight
2216400	1.92	Connector 10 Pin Header - Straight
2098103	3.06	Connector 16 Pin Header - Straight
2098104	2.76	Connector 20 Pin Header - Straight
2098106	4.56	Connector 34 Pin Header - Straight
2098107	4.68	Connector 40 Pin Header - Straight
2098108	7.56	Connector 50 Pin Header - Straight

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PART NUMBER	PRICE	DESCRIPTION	
2174401	8.10	Connector 50 Pin Header - Angle	
2098300	1.80	Connector 2 Position Jumper	
2098703	1.74	Connector 2 Pin Right Angle Molex	
2098800	.72	Connector 2 Pin Straight Wafer	
2098801	3.72	Connector 3 Pin Straight Wafer	
2098802	.72	Connector 5 Pin Straight Wafer	
2098700	1.02	Plug 5 Pin Molex Right Angle Wafer	
2001200	11.34	Jack Socket Connector Kit	
2109000	19.87	Power Cord 3 Conductor 3 Prong 6 FT	
		CRYSTALS	
2098602	6.60	Crystal 1.8432 MHz	
2216500	18.00	Crystal 4 MHz	
2098603	4.80	Crystal 8.0000 MHz	
2098605	3.54	Crystal 13.6080 MHz	
2048800	18.00	Crystal 15 MHz	
2042800	27.00	Crystal 16 MHz	(MOT, CTS, HYT)
2098604	4.50	Crystal 20.000 MHz	
2035200	37.08	Crystal 23.814 MHz K1114A	(MOT, CTS)
2099700	1.02	Insulator Mounting Pad For Crystal	
		FANS	
2099000	35.28	Fan 115V/230V AC 36-47 CFM (AIR OVER)	
2141500	52.50	Fan Box 230V AC TS 802/802H	
2245800	56.28	Fan Box 115V AC TS 1602G/GH	
2245700	67.20	Fan Box 230V AC TS 1602G/GH	
		BEZEL'S/CASE ASSEMBLIES	
2142000	40.00	Panel Front	TS 806
2142100	40.00	Panel Front	TS 806C
2142200	40.00	Panel Front	TS 806H
2105401	40.00	Panel Back	TS 806
2105500	40.00	Panel Back	TS 816
2105600	40.00	Panel Front	TS 816
2100102	10.00	Shroud Connector	TS 800A
2100500	10.00	Shroud Connector	TS 802/1602G
2219800	5.00	Card Guide	TS 802
2100300	15.00	Cover Fan	TS 816
2105700	28.80	Panel Floppy Cover	TS 802H (Plastic)

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PART NUMBER	PRICE	DESCRIPTION
MISCELLANEOUS SPARES		
2101600	64.80	Chassis Mounting TS 806/806H
2101900	5.88	Panel Cover Hard Disk TS 806
2103500	19.98	Cover Top Power Supply TS 802
2152800	6.72	Speaker (8 ohm) With Connector
2150100	41.70	Filter A.C. Line SAE HP2-2
2001300	2.88	Bail Mount Enclosure
2101900	5.88	Panel Shield Winchester Disk TS 806
2204900	2.89	Shield Board TS 816
2225200	31.80	Bracket TS 816/40 WDC
LABELS/LOGO'S		
2105000	1.50	Label Logo Plastic "TeleVideo" Systems
2191300	2.40	Label Logo Plastic "TeleVideo" Printer
2105104	.72	Label Keyboard TS 800A
2105105	.72	Label Keyboard TS 802
2105106	.72	Label Keyboard TS 802H
2208500	.72	Label Keyboard TS 1602G
2208600	.72	Label Keyboard TS 1602GH
2105300	.96	Label Back Panel "RS 232" TS 806-806/20
2105301	.96	Label Back Panel "Terminal" TS 806-806/20
2154402	1.50	Label Back of Unit TS 800A
2142900	.90	Label S1 TS 800A
2142901	.90	Label S2 TS 800A
BOXES/PACKING MATERIAL		
2208800	25.00	Carton Inner Shipping TS 802/TS 1602G
2143600	16.86	Carton Outer Shipping TS 802/TS 1602G
2143700	20.52	Carton Inner Shipping TS 806
2208900	31.98	Carton Outer Shipping TS 806
2143800	26.22	Carton Inner Shipping TS 816
2209000	31.98	Carton Outer Shipping TS 816
2185700	3.18	Corner Blocks Shipping Carton
2208200	16.00	Carton Shipping Hard Disk
2214401	12.00	Formed Foam TS 806
2237300	10.00	Formed Foam TS 800A

ALL PRICES SUBJECT TO CHANGE WITHOUT NOTICE

MINIMUM ORDER $500.00

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	SPARE PARTS KITS	PRICE
2280700	Kit, Spare Parts, Power - Video Module TS 800A	$ 153.28
2042200	2N3906 Vertical Amplifier	
2046500	2N3904 Vertical Drive	
2200000	2N4401 Horizontal Drive	
2047100	2N5551 Reference Amplifier	
2046700	KTC1627A 75Volt Regulator	
2201400	DS135D/IN391	
2047500	IN914	
2200800	Yoke Deflection With Connector	
2201200	Transformer Horizontal Drive	
2200900	Linearity Coil 5.40uh	
2201300	Transformer Flyback (High Voltage)	
2201000	Inductor 27uh	
2126900	Voltage Regulator LAS 16CB 2A/13.8Volts	
2186200	Resistor CF 390 Ohms 1/2Watt 5%	
2201600	IN759A Zener Diode	
2199300	Capacitor 220uf 16Volt Electrolytic	
2197300	Capacitor .1uf 600Volt Mylar	
2047300	2SC2233 MJE13006	
2280800	Diode 30S2 I.R. 3 Amp	
2126600	Voltage Regulator LAS L1405 3 Amp 5 Volt	
2000700	Kit, Spare Parts, Logic Bd 8 Bit Systems	$ 300.12
2042600	26LS32 RS422 interface	
2042400	26LS31 RS422 interface	
2050600	SIO/2 serial communications chip	
2050800	CTC counter timer chip	
2051000	CPU Z80A central processor unit	
2051200	DMA direct memory access chip	
2051600	64K dynamic RAM (4 each)	
2029200	75188N	
2029400	75189N	
2228400	Kit Data Cables TS 816's	$ 235.72
2006201	Logic to Tape/Logic to 816U	
2006400	Logic to Winchester 816	
2006801	816/40 WDC To Winchester	
2006601	816 Parallel Printer to Logic	
2007002	816/40 logic to WDC	
2006204	816/40 Logic to Tape/Logic to 816U	
2006200	816/40 Logic to WDC	
2006404	816/40 WDC to Winchester	
2224300	816/40 Parallel Printer	
2203000	Kit, Spare Parts Logic bd FDC	$ 199.59
2040200	WD2143-01 four phase clock logic	
2040400	WD1691 floppy support logic	
2040600	FD1793-02 (93816 fair amd) floppy controller	

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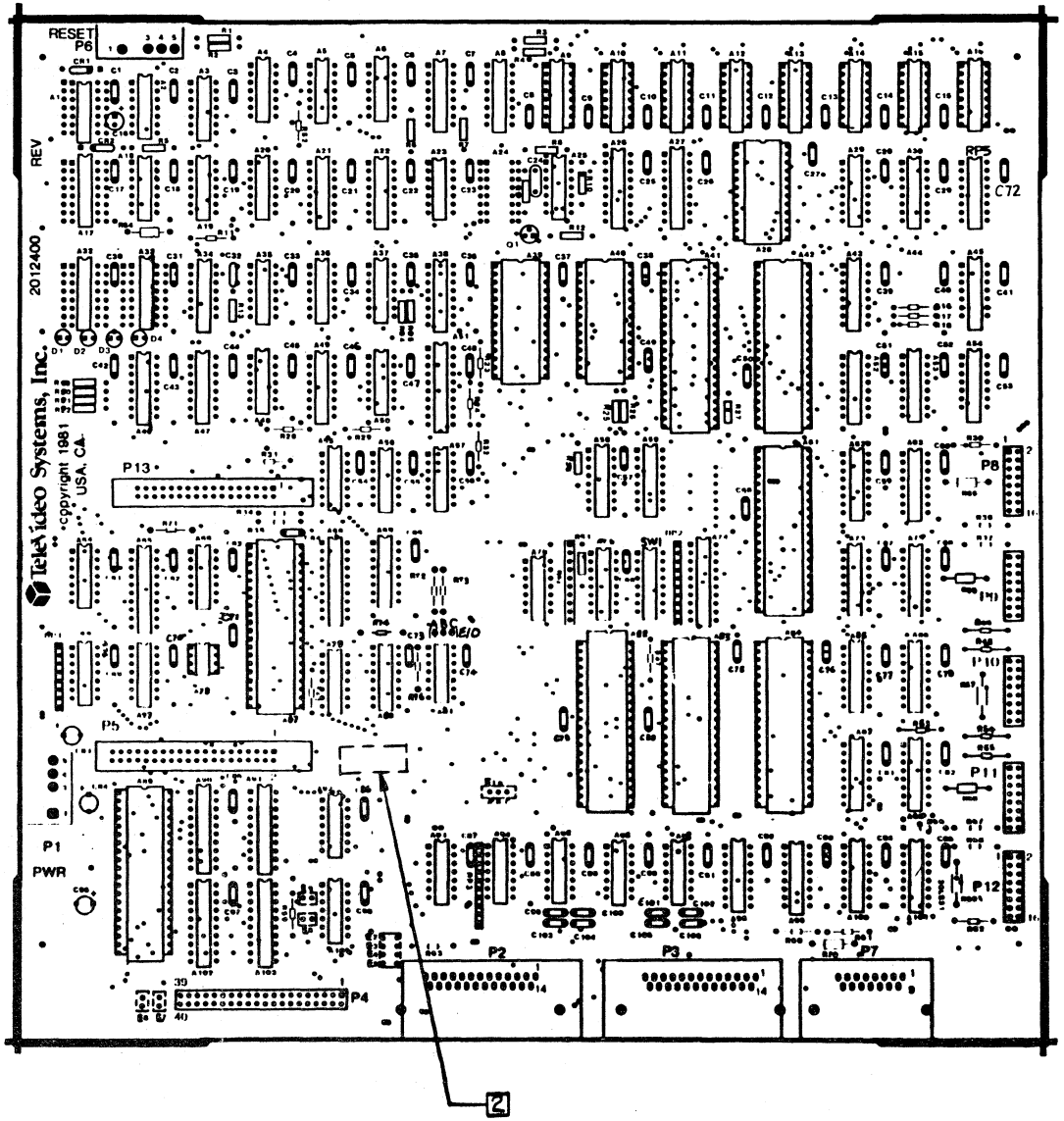
	SPARE PARTS KITS	PRICE
2270800	Kit Data Cables User Stations and TS 806's	$ 223.08
2006800	802H WDC To Winchester	
2007001	802H Daughter Board To WDC	
2007300	802 Daughter Board To Floppy	
2006100	802 Logic to Daughter Board	
2135700	1602G Logic to Graphics Board	
2006900	802H Daughter Board To Floppy/ WDC To Winchester	
2006501	806 RS422 to Logic	
2006901	806 Logic To Floppy/ WDC To Winchester	
2007000	806 Logic To WDC	
2006801	806 WDC To Winchester	
2006600	806 Parallel Printer	
2202800	Kit, Spare Parts, Mechanical TS802/800A	$ 90.88
2005700	cord for keyboard	
2223700	3 amp 125V fuse (25 each)	
2199400	keyswitch	
2096800	10 position side dip switch	
2223300	1 amp 250V fuse (25 each)	
2182100	RS232 connector	
2097900	RJ-11 connector	
2098000	RS422 connector	
2100500	connector shroud	
2202900	Kit, Spare Parts Logic bd WDC	$ 244.80
2056200	parallel converter	
2056400	MFM converter	
2056600	AM detector	
2056800	CRC generator/checker	
2057000	parallel to serial converter	
2057200	delay line	
2252000	Kit, Graphics Board	$ 401.40
2057400	IC Gate Array Graphics/1603	
2139800	IC 7220 Graphic Display Controller	
2139200	IC Dynamic RAM 4116 16K x 1 (120ns) [4 each]	
2252100	Kit, Spare Parts, Logic Board 16 Bit Systems	$ 703.50
2051600	64K dynamic RAM (4 each)	
2029200	75188N	
2029400	75189N	
2042600	26LS32 RS422 interface	
2042400	26LS31 RS422 interface	
2054000	IC 8284A Clock Generator	
2054200	IC 8288 Bus Controller	
2054400	IC P8088 CPU IAPX 88/10	
2054600	IC 8274 USART	
2054800	IC 8254 Program Interval Timer	
2055000	IC 8259A Priorty Interrupt Controller	
2055200	IC 8089 IOP	

DRAWINGS

This section contains the latest board assembly drawings and logic diagrams. When ordering parts, use the component type or value shown in the diagrams to refer to the TeleVideo part number listed in the Spare Parts Price List. These prices are for estimating only.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	PROD REL PER ECO 0429		

NOTE: UNLESS OTHERWISE SPECIFIED

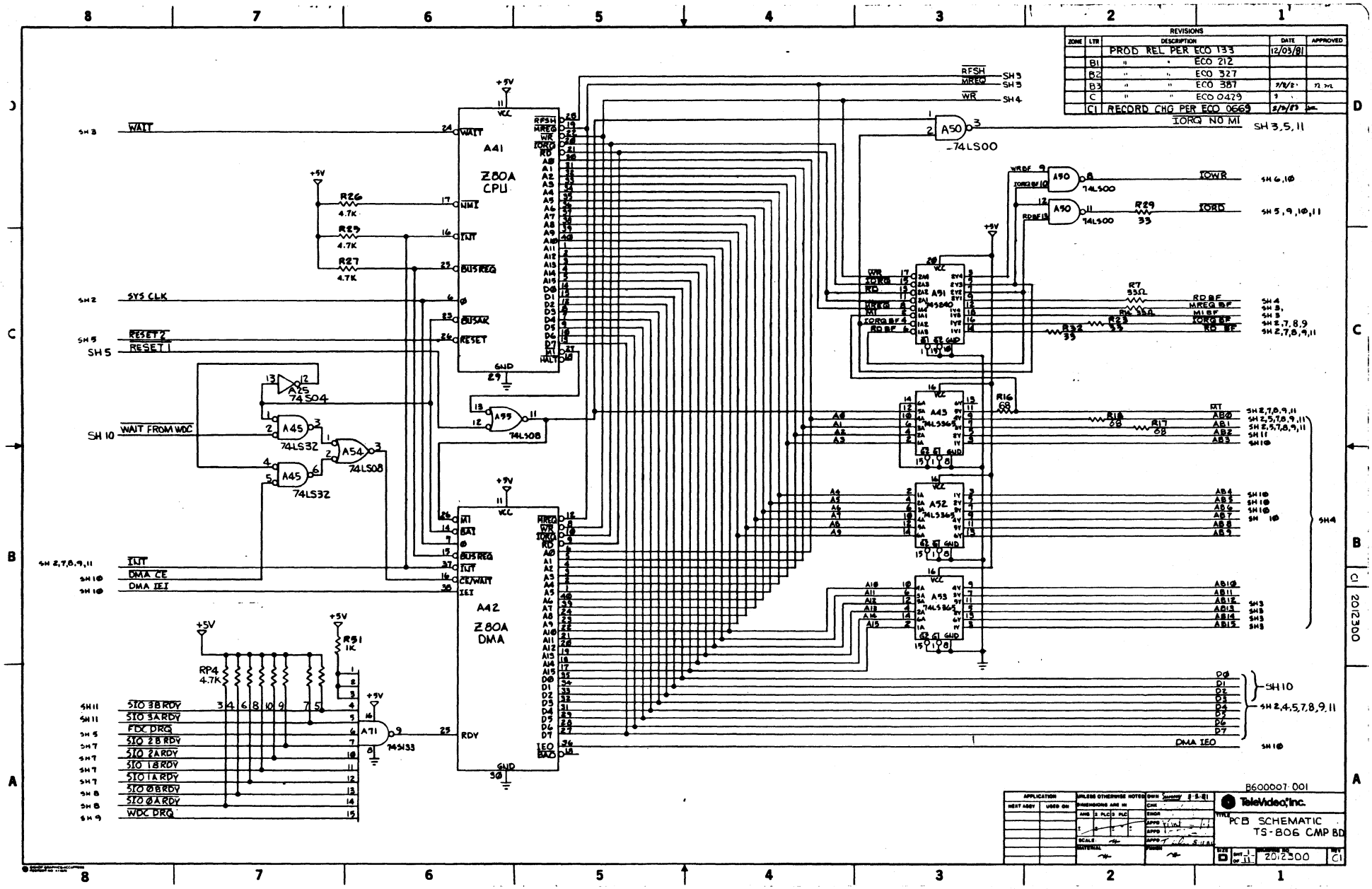
1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK .50-.100R APPROXIMATELY WHERE SHOWN.
3. MADE FROM 2012.100 FAB REV C.

B930007-001

TeleVideo, Inc.

TITLE: PCB ASY DWG TS-80C CMP BD

SIZE D | DRAWING NO. 2012400 | REV C


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
PROD REL PER ECO 133 12/03/81
B1 " " ECO 212
B2 " " ECO 327
B3 " " ECO 387
C " " ECO 0479
C1 RECORD CHG PER ECO 0669 2/5/83
IORQ NO MI
A41 Z80A CPU
A42 Z80A DMA
A50 74LS00
A90 74LS00
A91 74LS640
A43 74LS365
A52 74LS365
A53 74LS365
A25 74S04
A45 74LS32
A54 74LS08
A99 74LS08
A71 74S133
RP4 4.7K
R26 4.7K
R28 4.7K
R27 4.7K
R51 1K
R7 33Ω
R29 33
R32 33
R23 33
R16 68
R18 68
R17 68
WAIT
SYS CLK
RESET2
RESET1
WAIT FROM WDC
INT
DMA CE
DMA IEI
DMA IEO
RFSH
MREQ
WR
IORQ
RD
M1
IOWR
IORD
RD BF
MREQ BF
M1 BF
IORQ BF
STO 3B RDY
STO 3A RDY
FDC DRQ
STO 2B RDY
STO 2A RDY
STO 1B RDY
STO 1A RDY
STO ØB RDY
STO ØA RDY
WDC DRQ
SH 3,5,11
SH 6,10
SH 5,9,10,11
SH 4
SH 3,
SH 5
SH 2,7,8,9
SH 2,7,8,9,11
SH 10
SH 2,4,5,7,8,9,11
B600007-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
2012300
C1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
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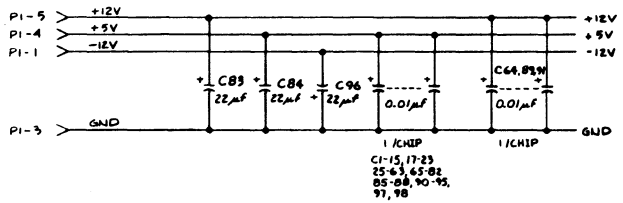
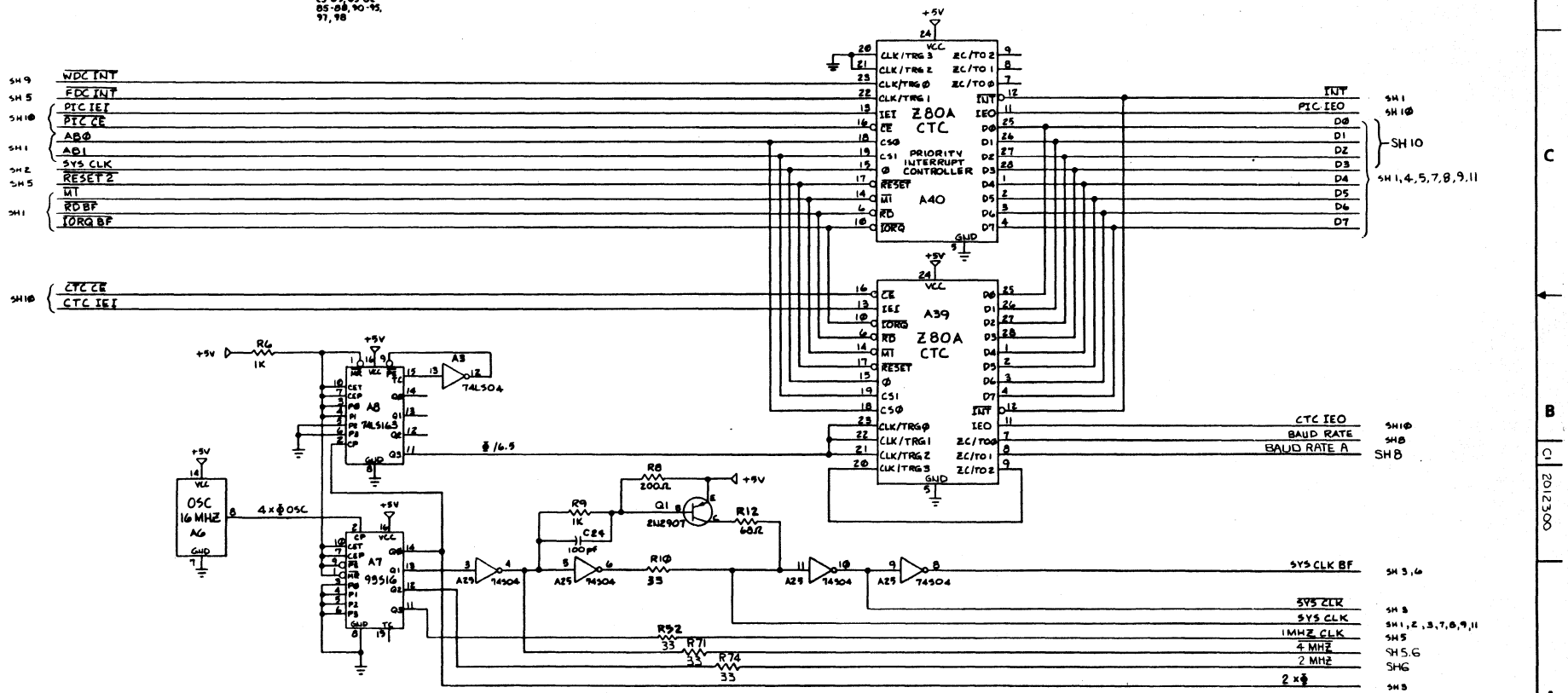
	C1	SEE SHT1	2/3/83	

POWER CABLE





B600007-001

TeleVideo, Inc.	
TITLE	PCB SCHEMATIC TS-806 CMP BD
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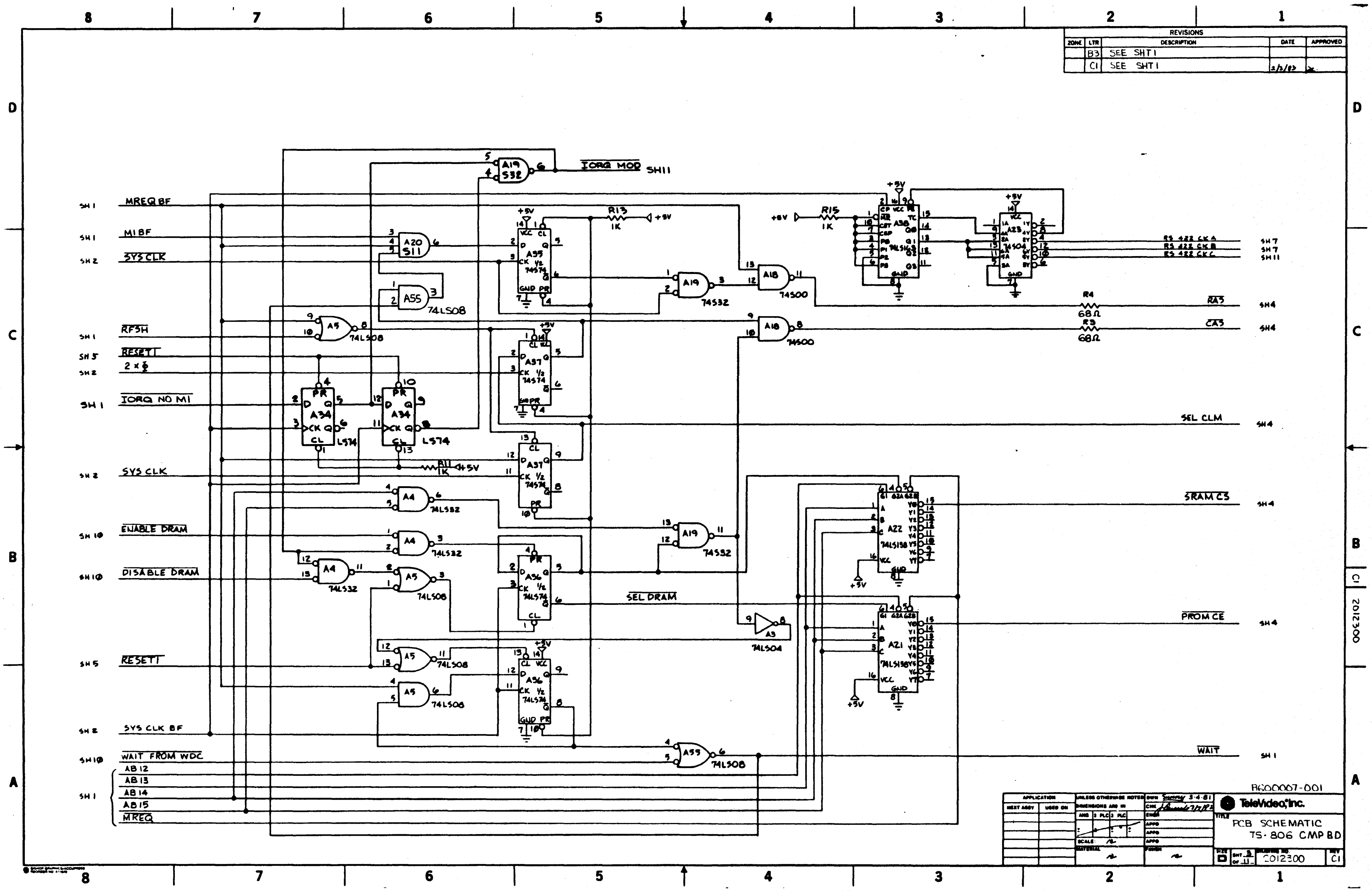
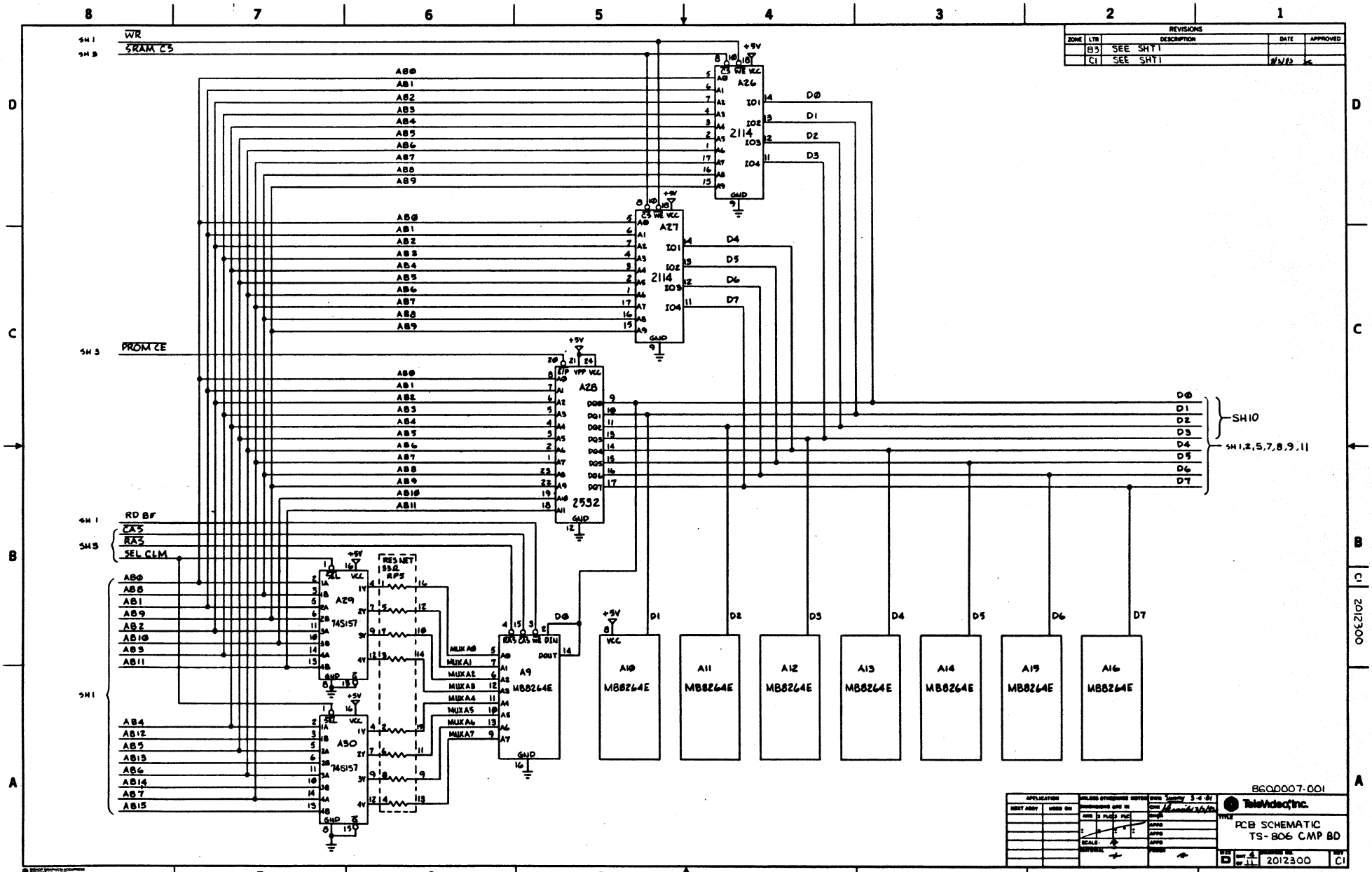
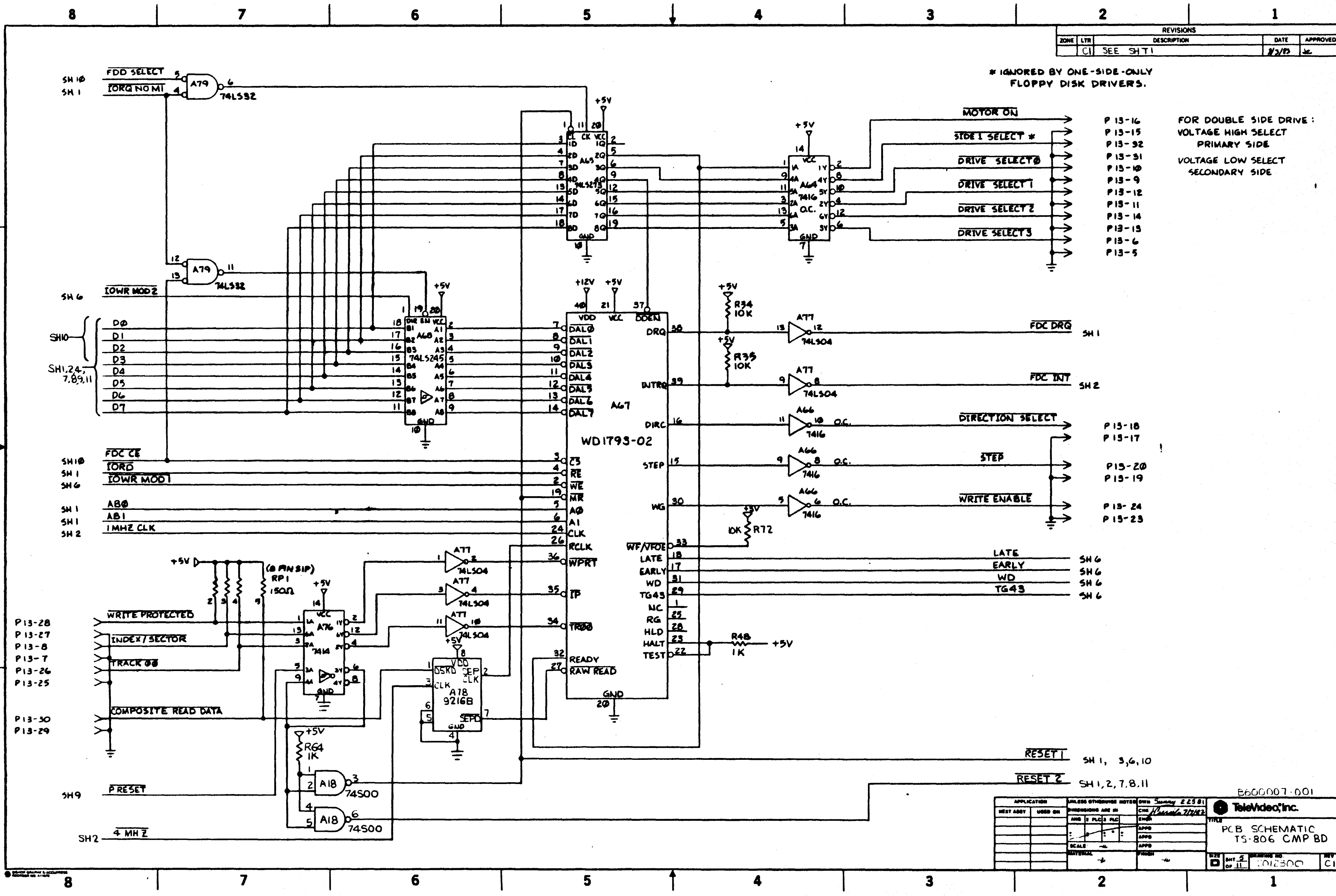
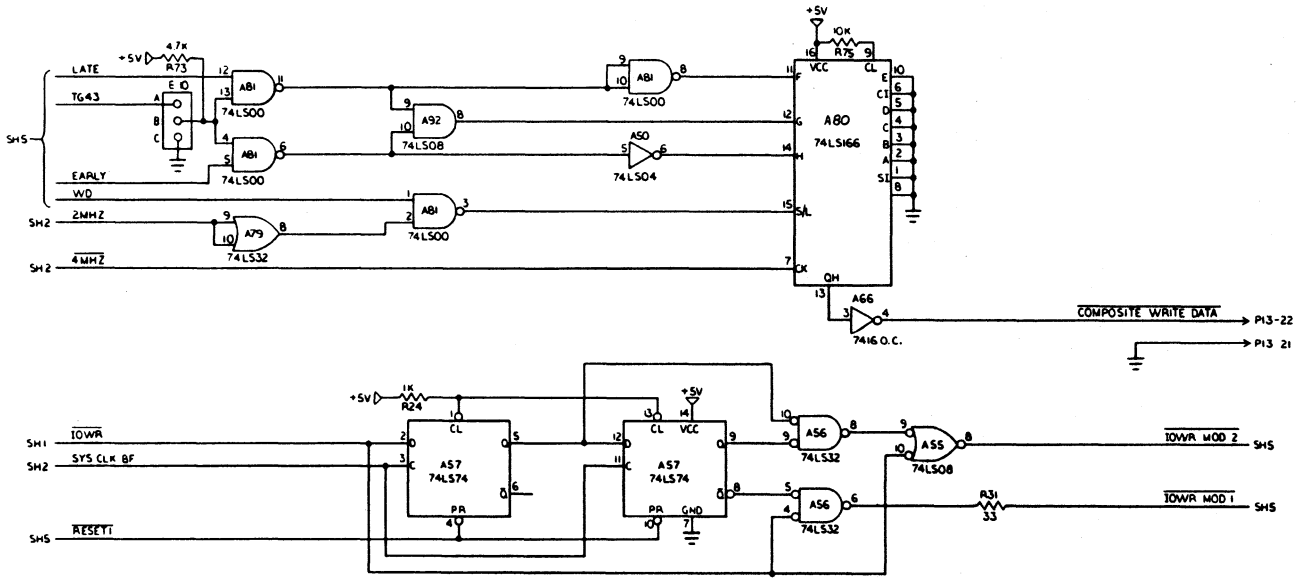
DWG NO	2012300
REV	C1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B3 SEE SHT 1
C1 SEE SHT 1
IORQ MOD SH11
MREQ BF
M1 BF
SYS CLK
RFSH
RESET1
2 × Φ
IORQ NO M1
SYS CLK
ENABLE DRAM
DISABLE DRAM
RESET1
SYS CLK BF
WAIT FROM WDC
AB 12
AB 13
AB 14
AB 15
MREQ
R13 1K
R15 1K
R11 1K
R4 68Ω
R3 68Ω
RS 422 CK A SH7
RS 422 CK B SH7
RS 422 CK C SH11
RAS SH4
CAS SH4
SEL CLM SH4
SRAM CS SH4
SEL DRAM
PROM CE SH4
WAIT SH1
74LS08
74LS32
74S00
74S32
74LS04
74S74
LS74
74LS138
B600007-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
D
SHT 3 OF 11
2012300
C1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B3 SEE SHT1
C1 SEE SHT1
WR
SRAM CS
PROM CE
RD BF
CAS
RAS
SEL CLM
A26
A27
A28
A29
A30
2114
2532
74S157
MB8264E
A9
A10
A11
A12
A13
A14
A15
A16
RES NET
330 RPS
+5V
GND
D0
D1
D2
D3
D4
D5
D6
D7
SH10
SH1,2,5,7,8,9,11
MUX A0
MUX A1
MUX A2
MUX A3
MUX A4
MUX A5
MUX A6
MUX A7
B6Q0007-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
2012300
C1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
C1 SEE SHT 1
* IGNORED BY ONE-SIDE-ONLY FLOPPY DISK DRIVERS.
FOR DOUBLE SIDE DRIVE:
VOLTAGE HIGH SELECT PRIMARY SIDE
VOLTAGE LOW SELECT SECONDARY SIDE
FDD SELECT
IORQ NO M1
A79 74LS32
74LS273
A64 7416 O.C.
MOTOR ON
SIDE 1 SELECT *
DRIVE SELECT 0
DRIVE SELECT 1
DRIVE SELECT 2
DRIVE SELECT 3
IOWR MOD 2
A68 74LS245
A67
WD1793-02
R34 10K
R35 10K
A77 74LS04
FDC DRQ
FDC INT
A66 7416
DIRECTION SELECT
STEP
WRITE ENABLE
R72 10K
FDC CE
IORD
IOWR MOD 1
AB0
AB1
1MHZ CLK
LATE
EARLY
WD
TG43
RESET 1
RESET 2
(8 PIN SIP)
RP1 150Ω
WRITE PROTECTED
INDEX/SECTOR
TRACK 00
COMPOSITE READ DATA
A76 7414
A78 9216B
R48 1K
R64 1K
A18 74S00
PRESET
4 MHZ
E600007-001
TeleVideo Inc.
PCB SCHEMATIC TS-806 CMP BD
2012300 C1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C1	SEE SHT 1 -	5/2/83	



B600007.001

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± 2 PLCS FLC
SCALE
MATERIAL

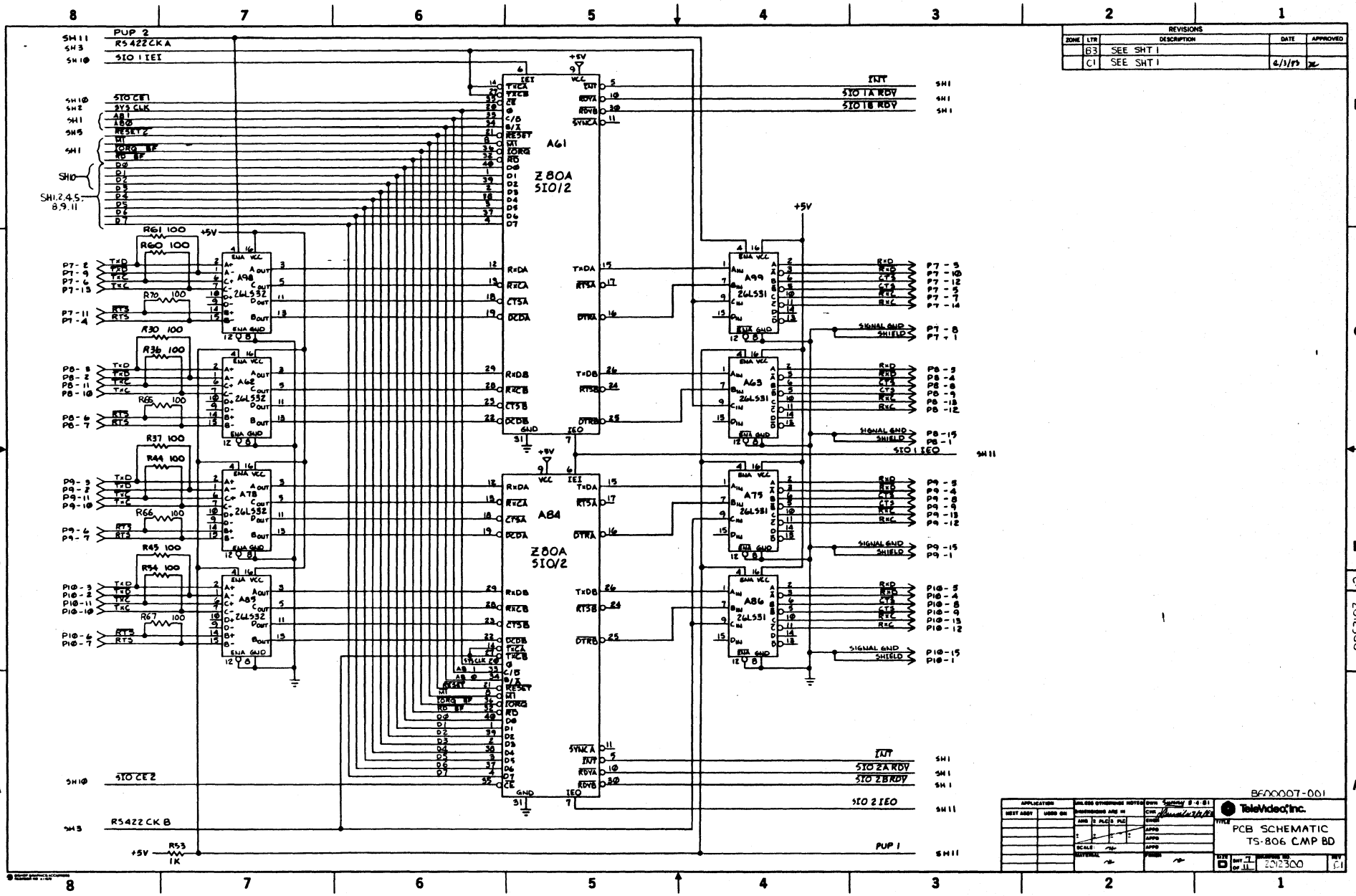
DWN H.H.JR 7/27/82
CHK
ENGR
APPD
APPD
APPD
FINISH

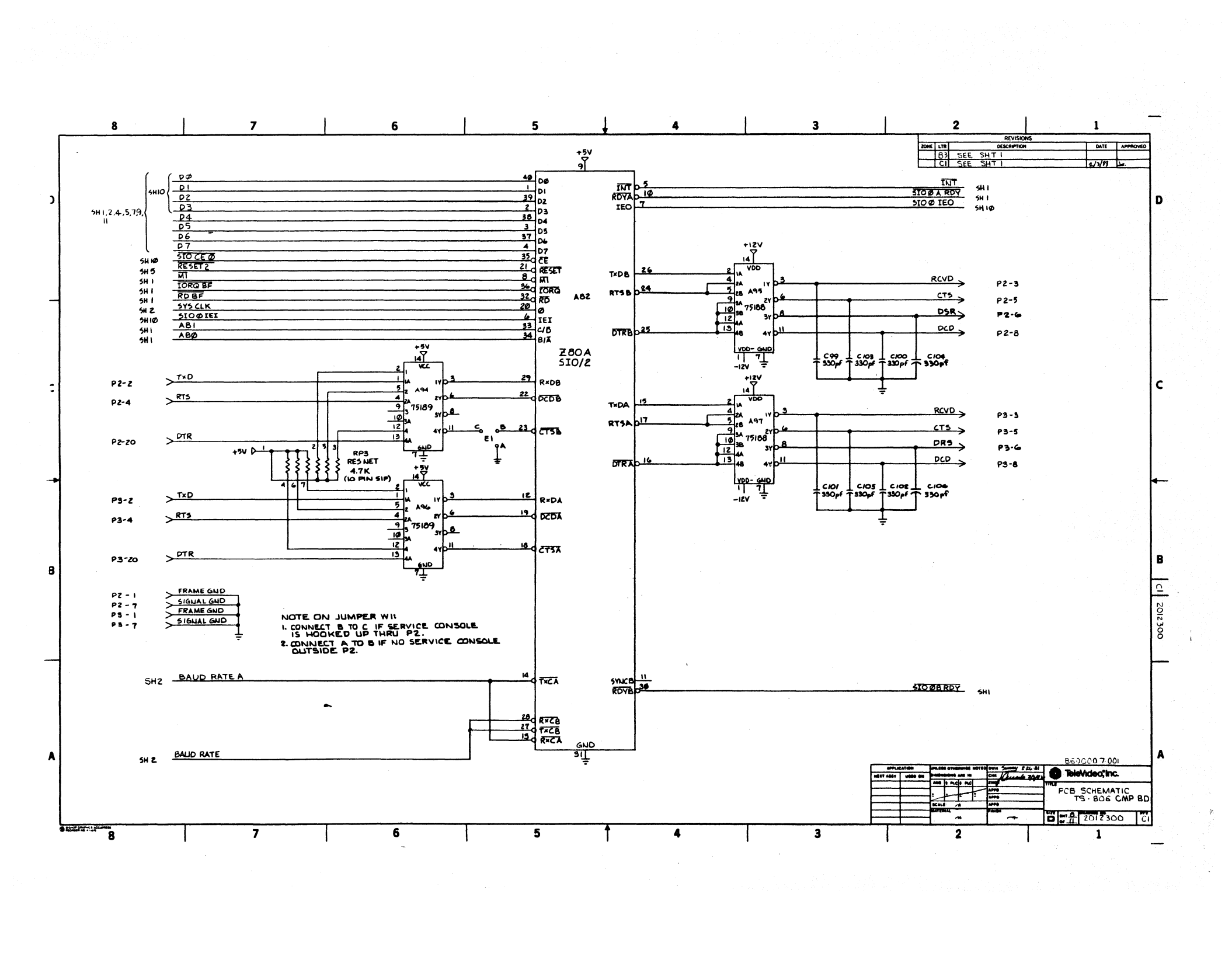
TeleVideo, Inc.

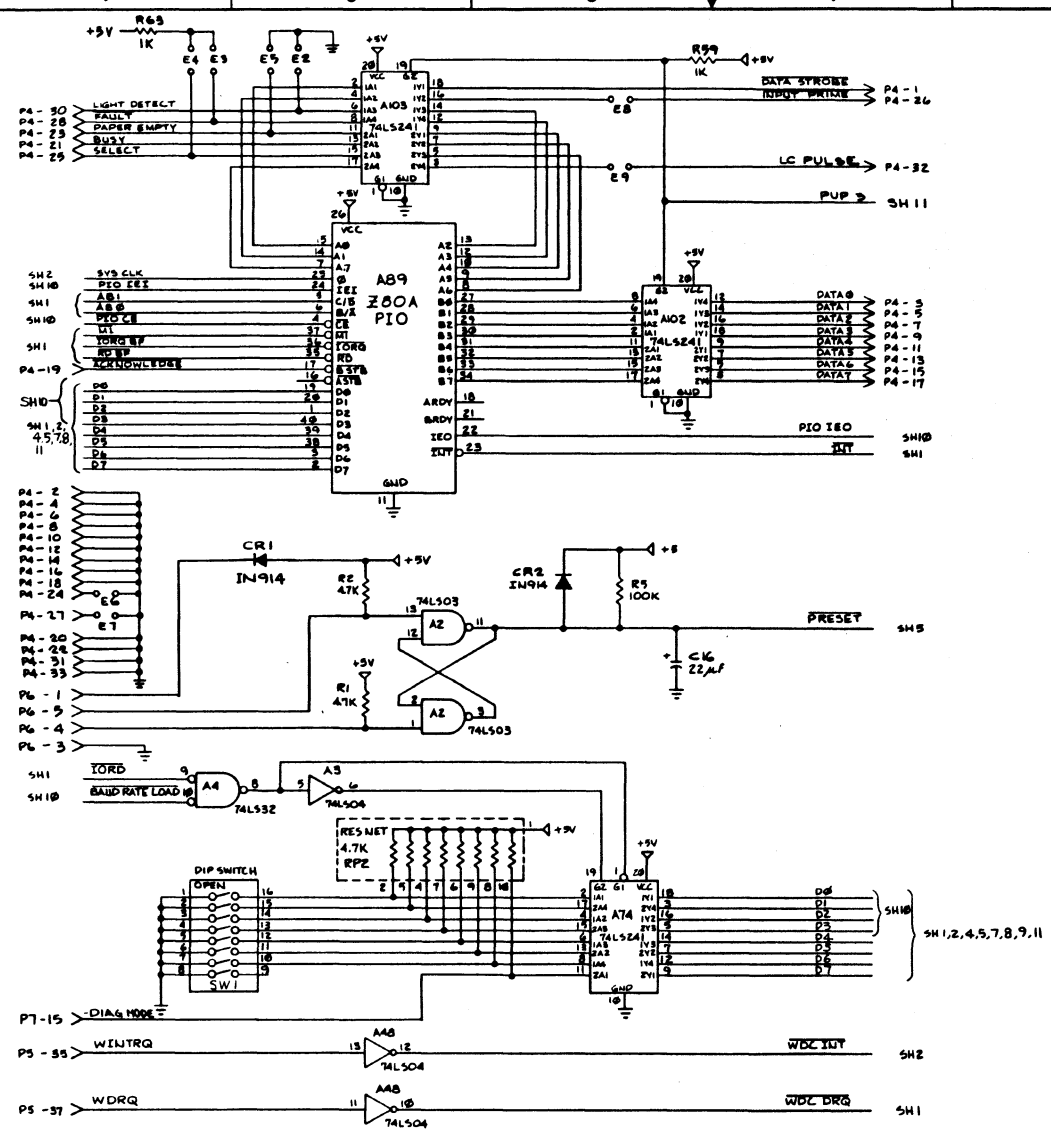
TITLE
PCB SCHEMATIC
TS 806 CMP BD

SIZE D | SHT 6 OF 11 | DRAWING NO 2012300 | REV C1

2012300 | 12 | 9


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B3 | SEE SHT 1
C1 | SEE SHT 1 | 4/3/83
PUP 2
RS422CKA
SIO 1 IEI
SIO CE1
SYS CLK
RESET 2
Z80A SIO/2
A61
A84
R61 100
R60 100
R70 100
R30 100
R36 100
R65 100
R37 100
R44 100
R66 100
R45 100
R54 100
R67 100
R53 1K
+5V
SIO CE2
RS422CK B
PUP 1
INT
SIO 1A RDY
SIO 1B RDY
SIO 1 IEO
SIO 2A RDY
SIO 2B RDY
SIO 2 IEO
SIGNAL GND
SHIELD
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
BF00007-001
2012300
C1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B3 SEE SHT 1
C1 SEE SHT 1 4/3/89
Z80A SIO/2
RP3 RES NET 4.7K (10 PIN SIP)
NOTE ON JUMPER W11
1. CONNECT B TO C IF SERVICE CONSOLE IS HOOKED UP THRU P2.
2. CONNECT A TO B IF NO SERVICE CONSOLE OUTSIDE P2.
75189
75188
TxDB
RTSB
DTRB
TxDA
RTSA
DTRA
RCVD
CTS
DSR
DCD
C99 330pf
C103 330pf
C100 330pf
C104 330pf
C101 330pf
C105 330pf
C102 330pf
C106 330pf
BAUD RATE A
BAUD RATE
FRAME GND
SIGNAL GND
B60000 7.001
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
2012300
C1



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B3	SEE SHT 1		
	C1	SEE SHT 1	6/3/83	

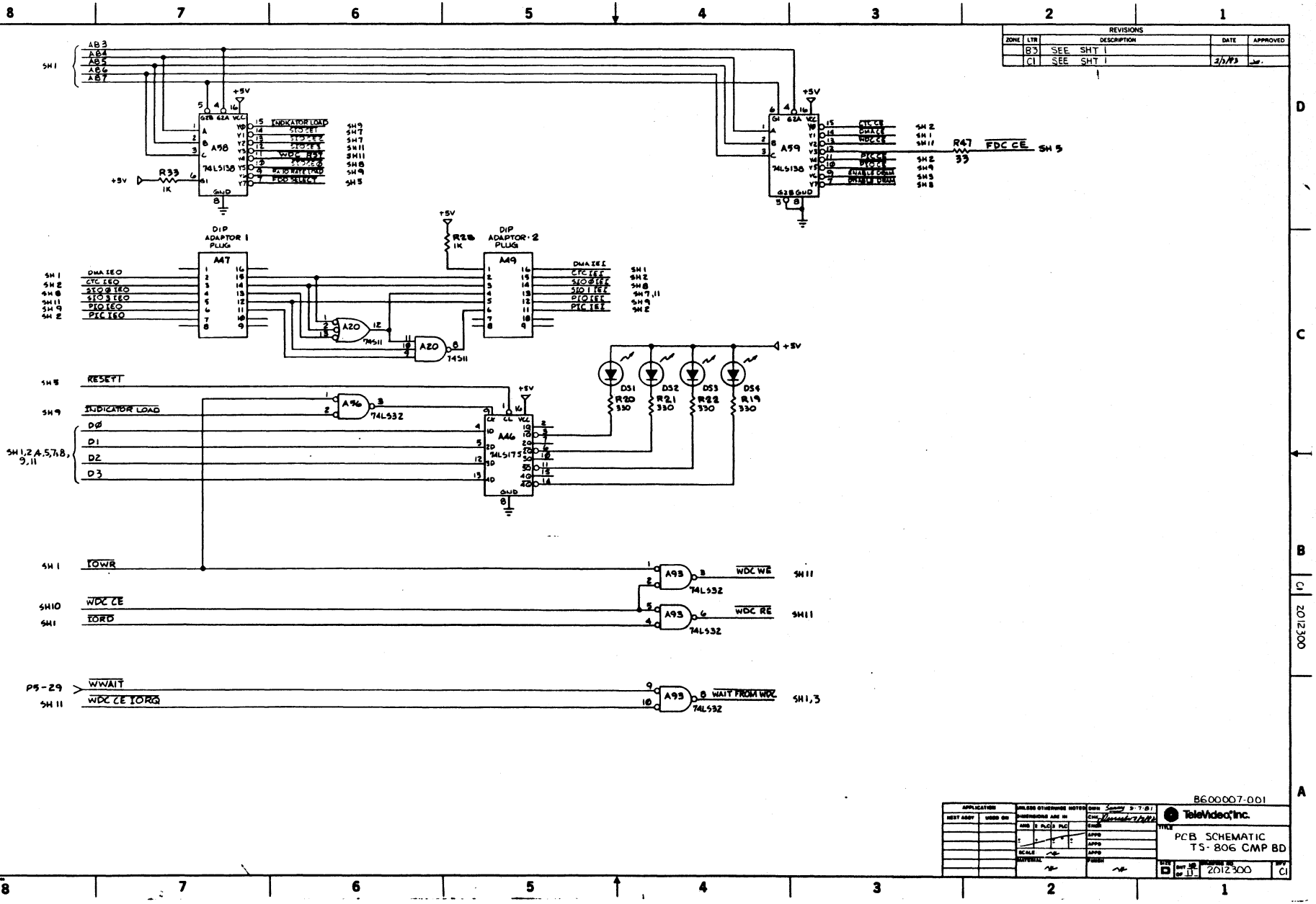
B600007-001

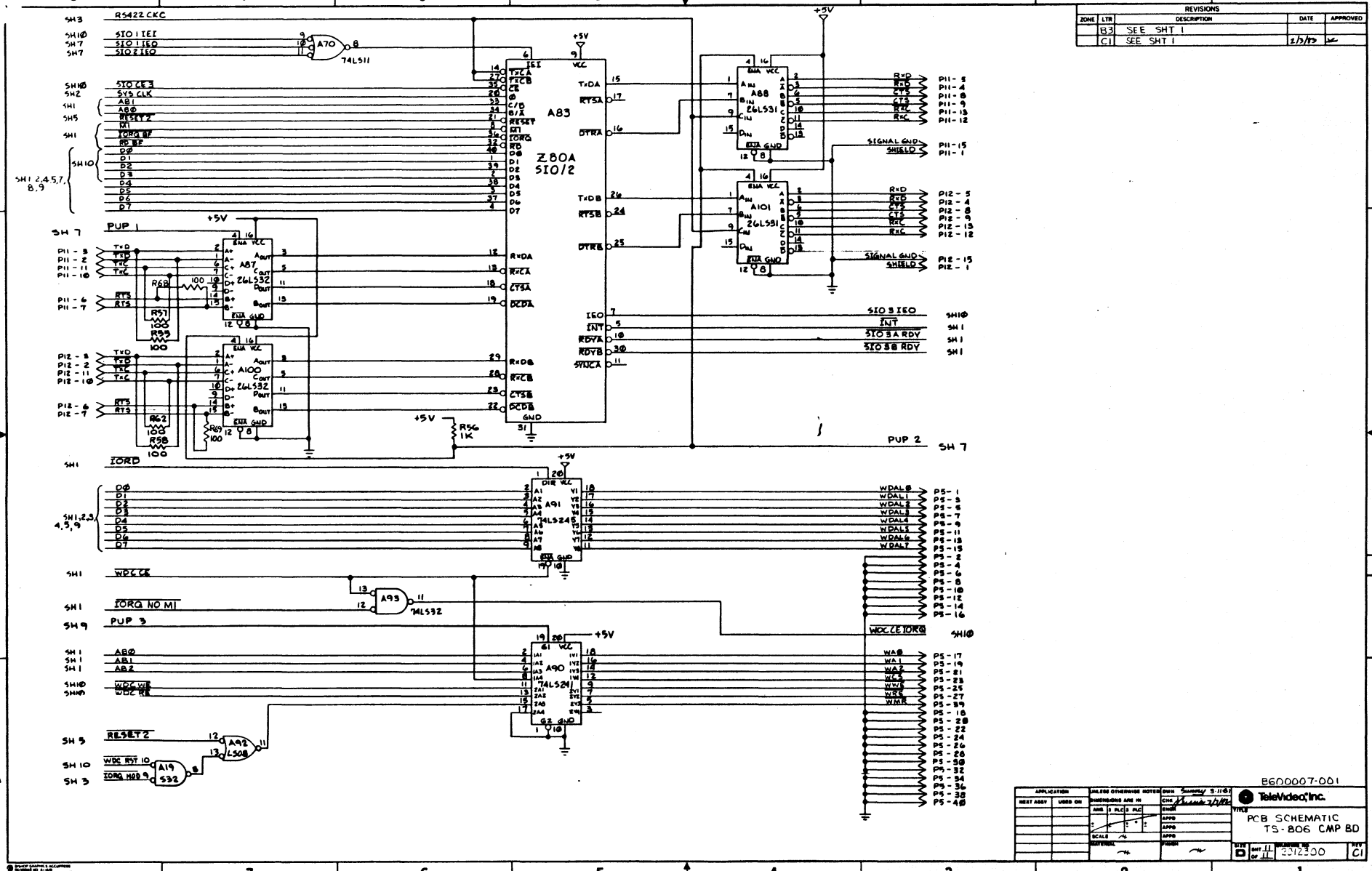
TeleVideo, Inc.

TITLE: PCB SCHEMATIC TS-806 CMP BD

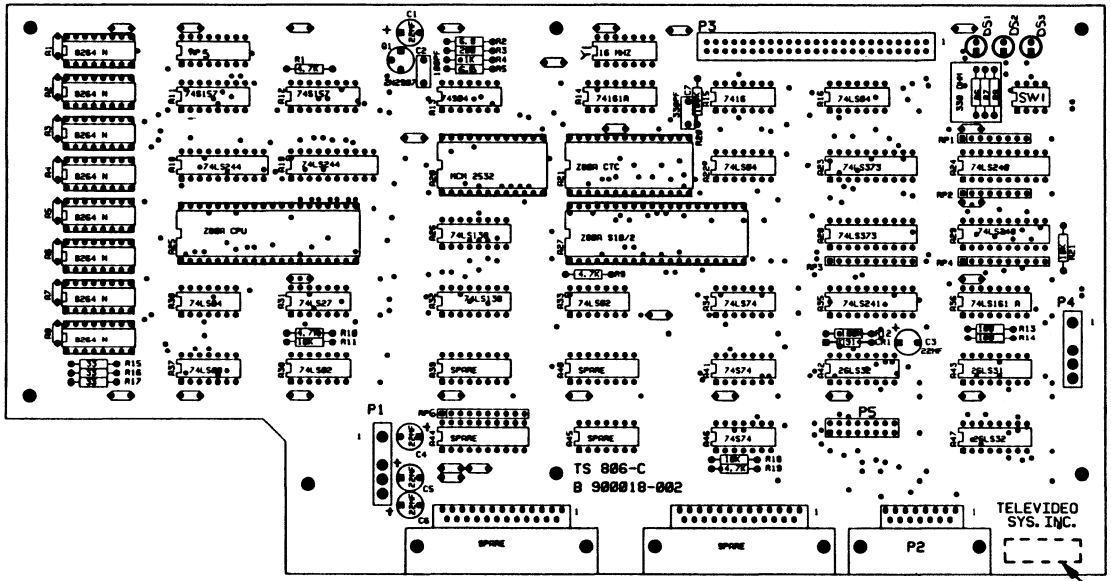
SIZE D | SHT 9 OF 11 | DRAWING NO. 2012300 | REV C1

C1 2012300


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B3 SEE SHT 1
C1 SEE SHT 1
A98
A99
74LS138
R33 1K
R47 33
FDC CE
DIP ADAPTOR 1 PLUG
DIP ADAPTOR 2 PLUG
A47
A49
A20
74S11
R28 1K
A46
74LS175
A96
74LS32
DS1 DS2 DS3 DS4
R20 R21 R22 R19 330
RESET
INDICATOR LOAD
D0
D1
D2
D3
IOWR
WDC CE
IORD
WDC WE
WDC RE
WWAIT
WDC CE IORQ
WAIT FROM WDC
B600007-001
TeleVideo Inc.
PCB SCHEMATIC
TS-806 CMP BD
2012300
C1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B3 | SEE SHT 1
C1 | SEE SHT 1 | 2/3/83
Z80A SIO/2
A83
A70
74LS11
A87
A100
A88
A101
Z6L532
Z6L531
A91
74LS245
A93
74LS32
A90
74LS241
A92
LS08
A19
S32
PUP 1
PUP 2
PUP 3
R56 1K
R57 100
R58 100
R62 100
R69 100
R68 100
R93 100
SIO 3 IEO
INT
SIO 3A RDY
SIO 3B RDY
IORD
IORQ NO MI
WDC CE
WDC CE IORQ
RESET 2
SIGNAL GND
SHIELD
B600007-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-806 CMP BD
SIZE D
SHT 11 OF 11
2012300
REV C1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 172		
	B	PROD REL PER ECO 266		



NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK (50-100R), APPROXIMATELY WHERE SHOWN.
3. MADE FROM B800018-002 FAB REV B.

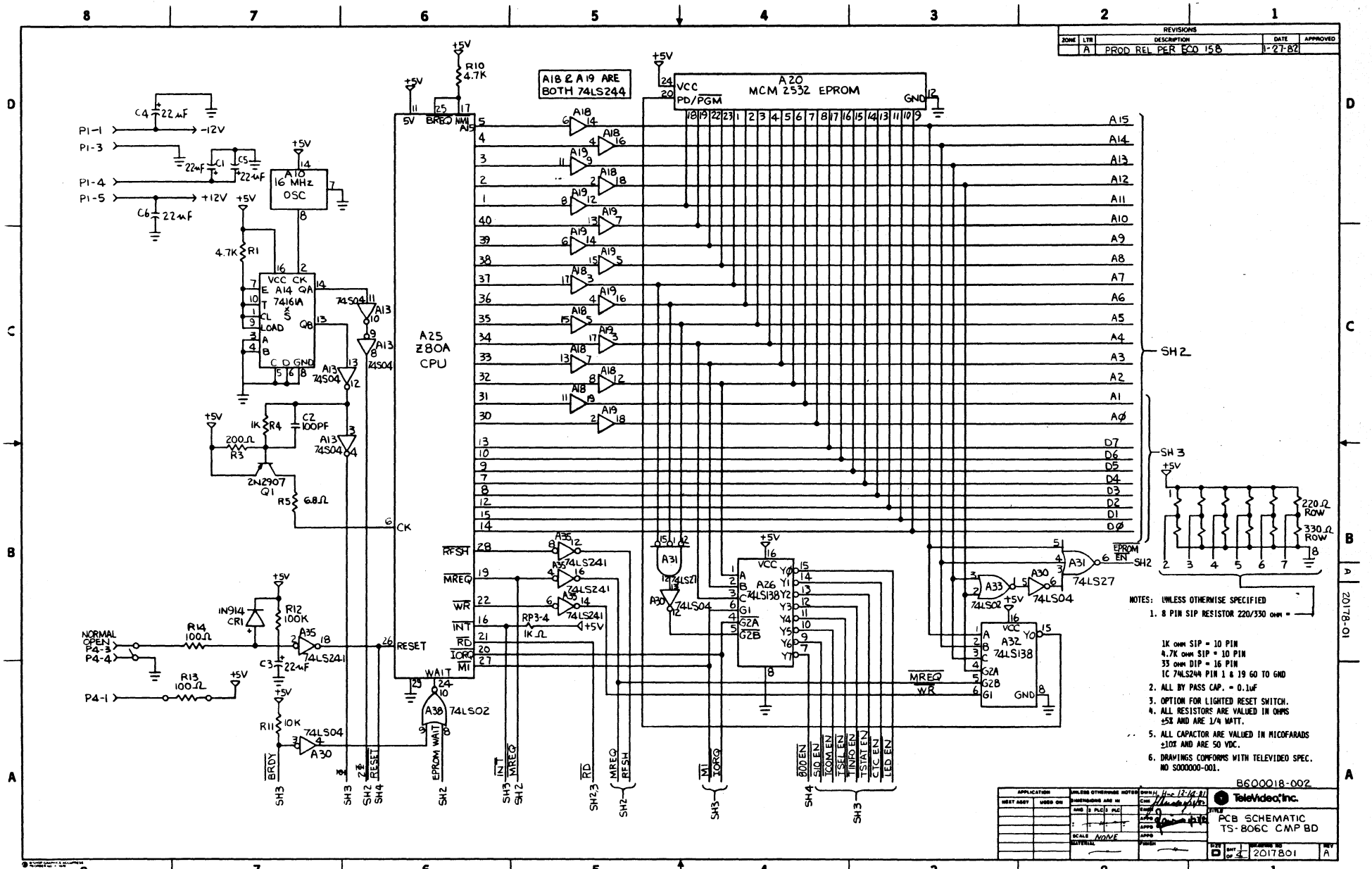
B930018-002

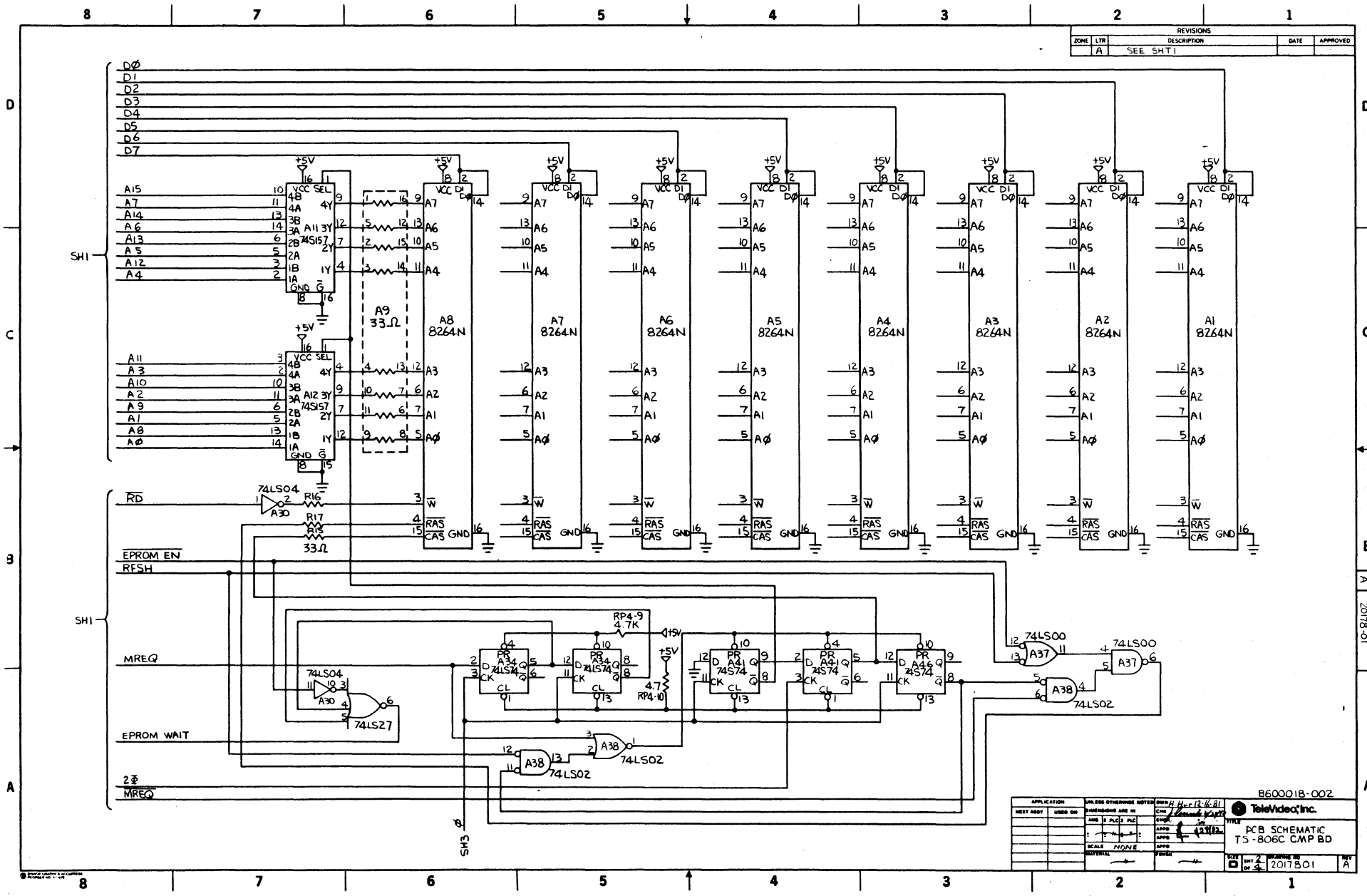
TeleVideo Inc.

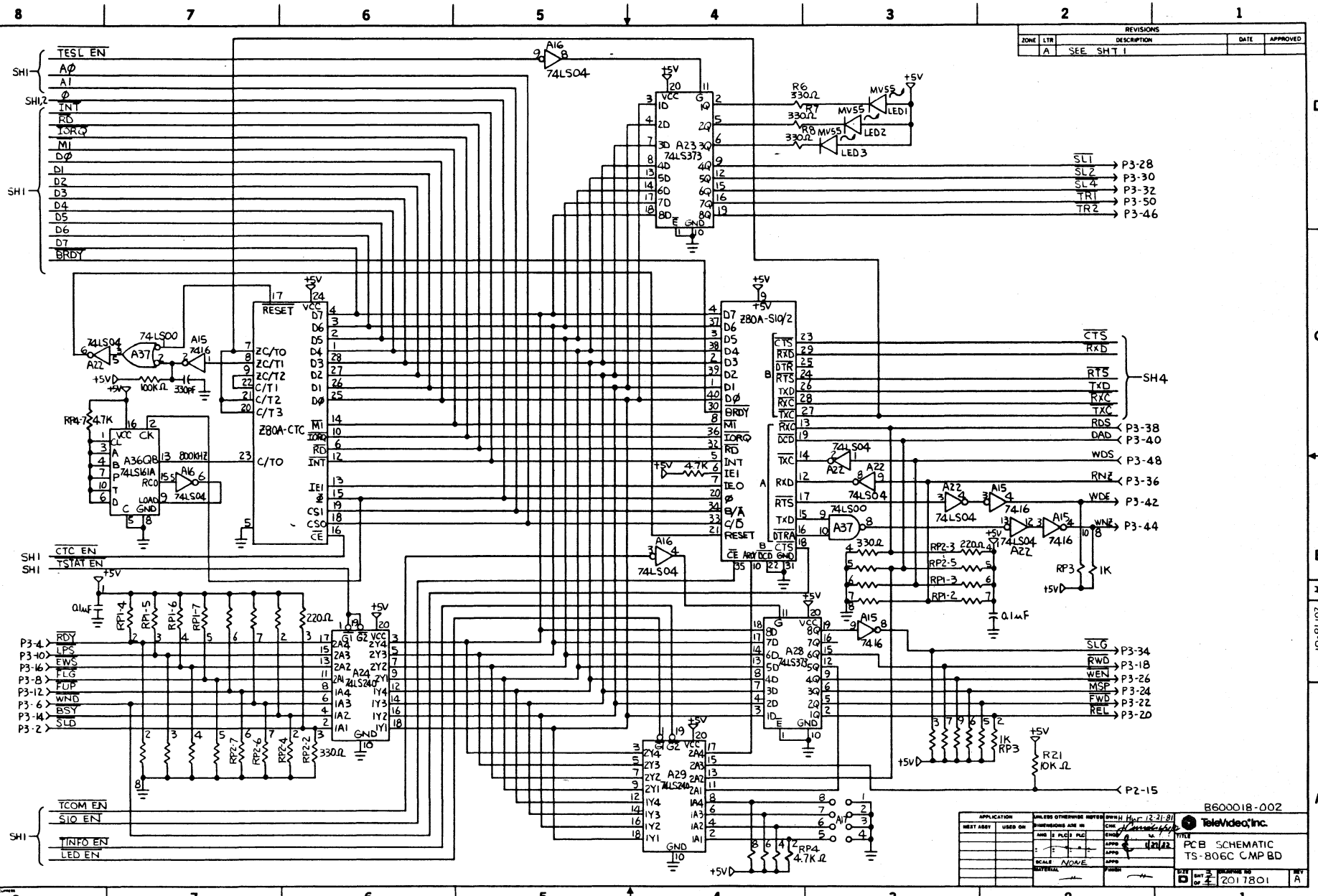
TITLE: PCB ASSY DWG TS-806C CMP BD

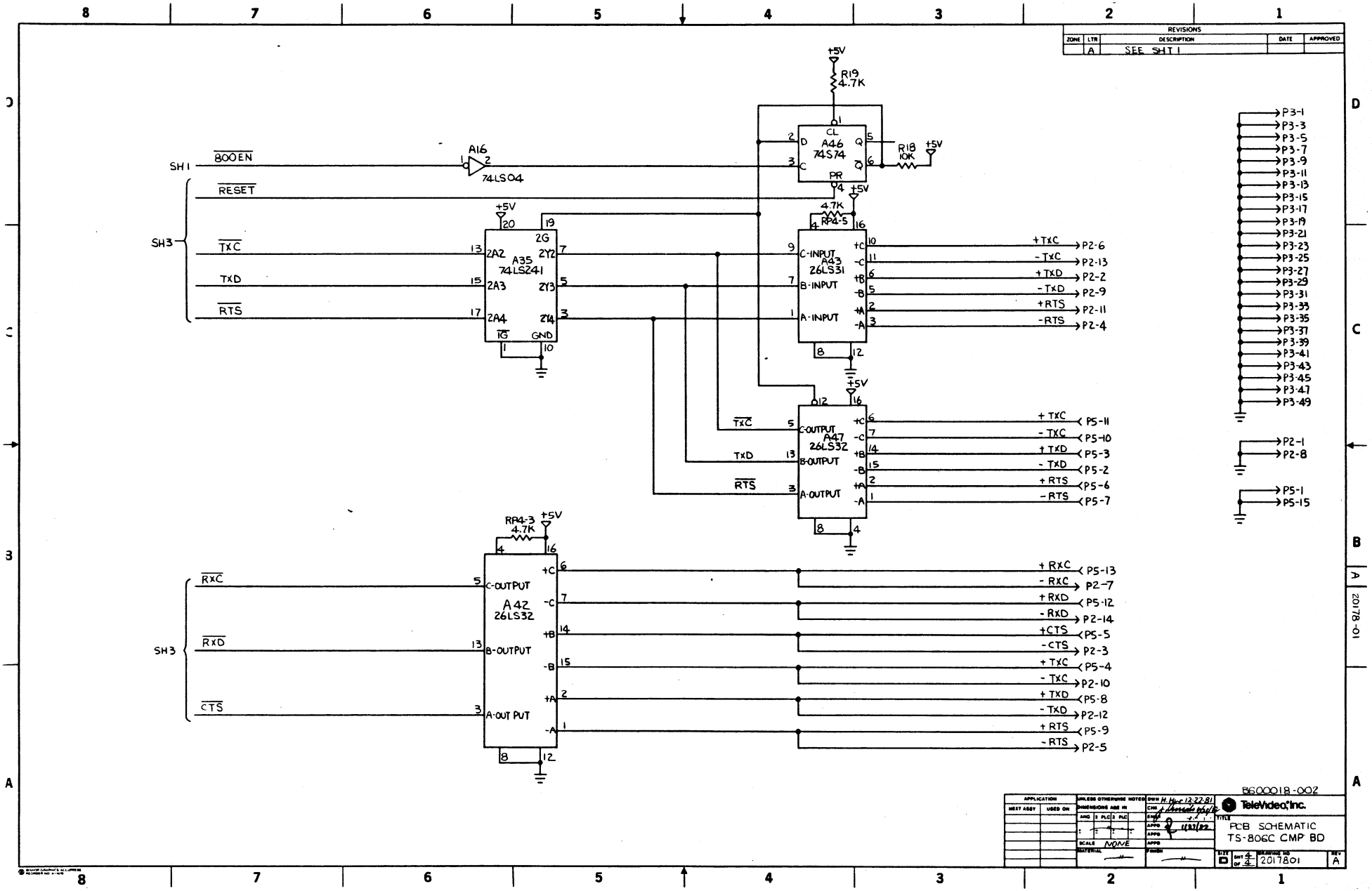
SIZE D | DWG NO 2017901 | REV B

2017901

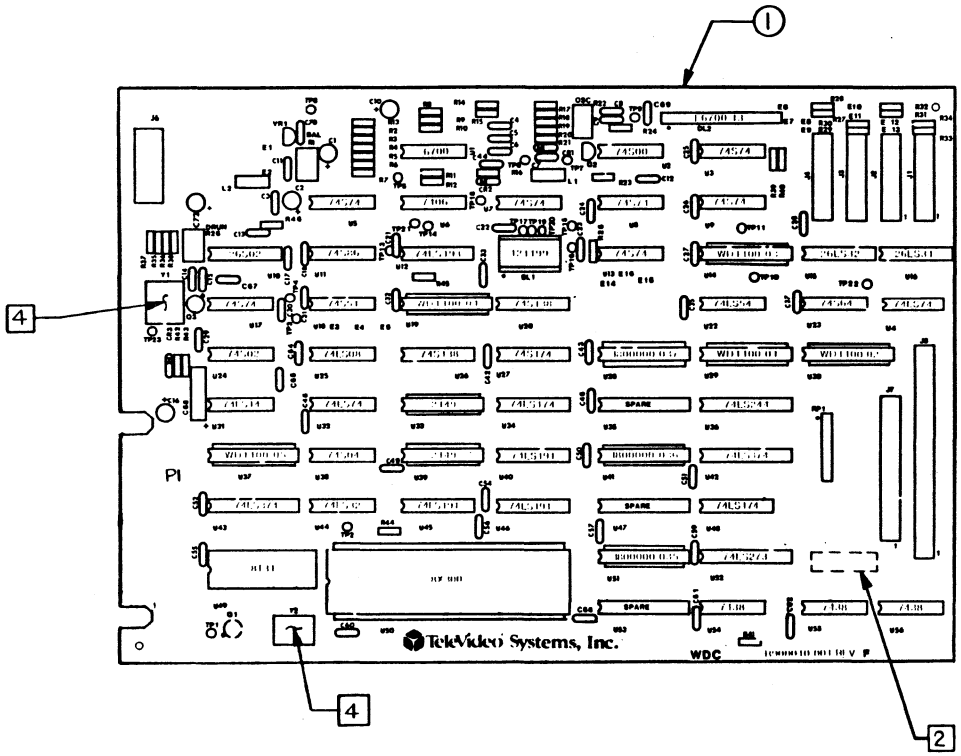

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | PROD REL PER ECO 158 | 1-27-82
A18 & A19 ARE BOTH 74LS244
A20 MCM 2532 EPROM
A25 Z80A CPU
A10 16 MHz OSC
A30 74LS04
A31 74LS27
A32 74LS138
A33 74LS02
A35 74LS241
A36 74LS241
A38 74LS02
A26 74LS138
A31 74LS21
R10 4.7K
R1 4.7K
R3 200Ω
R4 1K
R5 6.8Ω
R11 10K
R12 100K
R13 100Ω
R14 100Ω
RP3-4 1K Ω
C1 22uF
C2 100PF
C3 22uF
C4 22uF
C5 22uF
C6 22uF
CR1 IN914
Q1 2N2907
P1-1 -12V
P1-3
P1-4
P1-5 +12V
P4-1
P4-3
P4-4
NORMAL OPEN
SH2
SH3
SH4
220Ω ROW
330Ω ROW
NOTES: UNLESS OTHERWISE SPECIFIED
1. 8 PIN SIP RESISTOR 220/330 OHM =
1K OHM SIP = 10 PIN
4.7K OHM SIP = 10 PIN
33 OHM DIP = 16 PIN
IC 74LS244 PIN 1 & 19 GO TO GND
2. ALL BY PASS CAP. = 0.1uF
3. OPTION FOR LIGHTED RESET SWITCH.
4. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
5. ALL CAPACTOR ARE VALUED IN MICOFARADS ±10% AND ARE 50 VDC.
6. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. NO S000000-001.
B600018-002
TeleVideo, Inc.
PCB SCHEMATIC
TS-806C CMP BD
2017801
A
20178-01


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A SEE SHT1
D0
D1
D2
D3
D4
D5
D6
D7
SH1
A15
A7
A14
A6
A13
A5
A12
A4
A11
A3
A10
A2
A9
A1
A8
A0
74LS157
A11 3Y
A12 3Y
A9
33Ω
A8 8264N
A7 8264N
A6 8264N
A5 8264N
A4 8264N
A3 8264N
A2 8264N
A1 8264N
+5V
VCC SEL
4B 4A 4Y 3B 3A 3Y 2B 2A 2Y 1B 1A 1Y GND G
VCC DI DØ
A7 A6 A5 A4 A3 A2 A1 A0
W RAS CAS GND
RD
74LS04
A30
R16
R17
R18
33Ω
EPROM EN
RFSH
MREQ
EPROM WAIT
2Ø
MREQ
SH3
RP4-9
4.7K
4.7
RP4-10
74LS74
PR D CK CL Q
74LS27
74LS02
74LS00
A37
A38
B600018-002
TeleVideo Inc.
PCB SCHEMATIC
TS-806C CMP BD
SIZE D
SHT 2 OF 4
DRAWING NO 2017801
REV A
2017801-01


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | SEE SHT 1
TESL EN
AØ
A1
Ø
INT
RD
IORQ
M1
DØ
D1
D2
D3
D4
D5
D6
D7
BRDY
SH1
SH2
A16 74LS04
A23 74LS373
R6 330Ω
R7 330Ω
R8 330Ω
MV55 LED1
MV55 LED2
MV55 LED3
SL1 P3-28
SL2 P3-30
SL4 P3-32
TR1 P3-50
TR2 P3-46
Z80A-CTC
Z80A-SIO/2
RESET
ZC/TO
ZC/T1
ZC/T2
C/T1
C/T2
C/T3
C/TO
800KHZ
A36QB 74LS161A
A37 74LS00
A15 74LS16
A22 74LS04
100KΩ
330pF
4.7K
CTC EN
TSTAT EN
SIO EN
TCOM EN
TINFO EN
LED EN
0.1mF
220Ω
330Ω
1K RP3
10K Ω R21
A24 74LS240
A29 74LS240
A28 74LS373
RDY P3-4
LPS P3-10
EWS P3-16
FLG P3-8
FUP P3-12
WND P3-6
BSY P3-14
SLD P3-2
CTS
RXD
DTR
RTS
TXD
RXC
TXC
DCD
RDS P3-38
DAD P3-40
WDS P3-48
RNZ P3-36
WDE P3-42
WNZ P3-44
SH4
SLG P3-34
RWD P3-18
WEN P3-26
MSP P3-24
FWD P3-22
REL P3-20
P2-15
B600018-002
TeleVideo, Inc.
TITLE PCB SCHEMATIC TS-806C CMP BD
SIZE D
DRAWING NO 2017801
REV A
SHT 3 OF 4
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
SCALE NONE
MATERIAL
FINISH
DRWN H Hor 12-21-81
CHK
ENGR
APPD
APPD
APPD
APPD
1/21/82
2017801-01

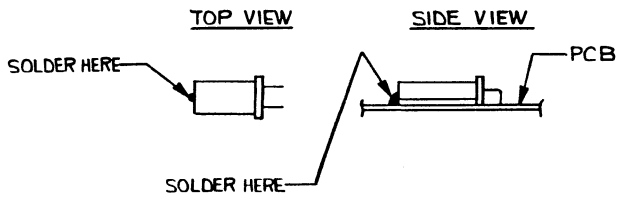

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A SEE SHT 1
+5V
R19 4.7K
A46 74S74
R18 10K
A16 74LS04
800EN
RESET
SH1
SH3
A35 74LS241
TXC
TXD
RTS
RP4-5 4.7K
A43 26LS31
+TXC
-TXC
+TXD
-TXD
+RTS
-RTS
P3-1
P3-3
P3-5
P3-7
P3-9
P3-11
P3-13
P3-15
P3-17
P3-19
P3-21
P3-23
P3-25
P3-27
P3-29
P3-31
P3-33
P3-35
P3-37
P3-39
P3-41
P3-43
P3-45
P3-47
P3-49
P2-6
P2-13
P2-2
P2-9
P2-11
P2-4
A47 26LS32
P5-11
P5-10
P5-3
P5-2
P5-6
P5-7
P2-1
P2-8
P5-1
P5-15
RP4-3 4.7K
RXC
RXD
CTS
A42 26LS32
+RXC
-RXC
+RXD
-RXD
+CTS
-CTS
P5-13
P2-7
P5-12
P2-14
P5-5
P2-3
P5-4
P2-10
P5-8
P2-12
P5-9
P2-5
B600018-002
TeleVideo, Inc.
PCB SCHEMATIC
TS-806C CMP BD
2017801
A
20178-01

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	PROD REL PER ECO 0138		
	E	" " ECO 0146		
	E1	" " ECO 0219		
	E2	" " ECO 0278, 0280		
	E3	" " ECO 0332		
	F	" " ECO 0475	11/11/87	



NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50 - 100R APPROXIMATELY WHERE SHOWN.
3. MADE FROM 2013600 FAB REV F.
4. SOLDER TIE DOWN Y1 AND Y2 IN LOCATION AS SHOWN.



TeleVideo Inc.

PCB ASSY DWG
WIN DISC CONTL

SIZE D | SHT 1 OF 1 | DRAWING NO. 2013900 | REV F

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO	4/20/82	
	B	" " ECO 0125		
	C	" " ECO 0131		
	D	" " ECO 0138		
	E	" " ECO 0146		
	E1	" " ECO 0322		
	F	" " ECO 0415	10/20/82	
	G	" " ECO 0594	11-17-82	WMC

MNEMONIC	MEANING
$\overline{\text{AMDET}}$	ADDRESS MARK DETECT
A2-AØ	TASK FILE ADDRESS SELECT BITS 2-Ø
$\overline{\text{BIC}}$	BUS INPUT CONTROL
$\overline{\text{BOC}}$	BUS OUTPUT CONTROL
$\overline{\text{CLKS}}$	CLOCK DATA
$\overline{\text{CRCIZ}}$	CYCLIC REDUNDANCY CHECK WORD INITIALIZE
CRCOK	CRC OKAY
$\overline{\text{CS}}$	CARD SELECT
CSAC	CARD SELECT ACCESS CONTROL
DAL7-DALØ	DATA ACCESS LINE
-DIRECTION IN	DIRECTION CONTROL
DHOLD	DATA HOLD
DLYDAT	DELAYED DATA
DRQ	DATA REQUEST
$\overline{\text{DRQCLK}}$	DATA REQUEST CLOCK
$\overline{\text{DRSEL}}$	DRIVE SELECT
DRS4-DRS1	DRIVE SELECT BITS 4-1
$\overline{\text{DRUN}}$	DATA RUN
$\overline{\text{HFRQ}}$	HIGH FREQUENCY
$\overline{\text{HSAC}}$	HOST SELECT ACCESS CONTROL
HS2-HSØ	HEAD SELECT BITS 2-Ø
IA9-IAØ	INSTRUCTION ADDRESS LINES BITS 9-Ø
ID15-IDØ	INSTRUCTION DATA BITS 15-Ø
-INDEX	INDEX PULSE FROM DRIVE
$\overline{\text{INTCLK}}$	INTERRUPT CLOCK
INTRQ	INTERRUPT REQUEST
IO7-IOØ	I/O LINES 7-Ø
$\overline{\text{IVBØ}}$-$\overline{\text{IVB7}}$	INPUT VECTOR BUS BITS Ø-7
MCLK	MASTER CLOCK
$\overline{\text{MFMW}}$	MODIFIED FREQUENCY MODULATION WRITE STREAM
$\overline{\text{MR}}$	MASTER RESET
$\overline{\text{OSC}}$	OSCILLATOR OUTPUT
RA9-RAØ	RAM ADDRESS BITS 9-Ø
RCLK	READ CLOCK
$\overline{\text{RCS}}$	RAM CHIP SELECT
$\overline{\text{RDAT}}$	READ DATA
RD6-RD4 RD2 RDØ	READ CONTROL LINES
$\overline{\text{RE}}$	READ ENABLE
-$\overline{\text{READY}}$	READY STATUS FROM DRIVE
$\overline{\text{RESET}}$	RESET SIGNAL
RGATE	READ GATE
$\overline{\text{ROVF}}$	RAM OVERFLOW
RWC	REDUCE WRITE CURRENT

MNEMONIC	MEANING
-SEEK COMPLETE	SEEK COMPLETE STATUS FROM DRIVE
SRCH	SEARCH
-STEP PULSE	STEP PULSE TO DRIVE
TIMCLK	TIMING CLOCK FOR SA1000
TRACK ØØØ	TRACK ØØØ STATUS FROM DRIVE
$\overline{\text{WAEN}}$	WAIT ENABLE
$\overline{\text{WAIT}}$	MEMORY NOT READY SIGNAL
WCLK	WRITE CLOCK
$\overline{\text{WE}}$	WRITE ENABLE
WGI	WRITE GATE INTERNAL
-WRITE FAULT	WRITE FAULT STATUS FROM DRIVE
WR7-WRØ	WRITE CONTROL LINES
$\overline{\text{1BLA}}$	1 BYTE LOOK AHEAD
$\overline{\text{2XDR}}$	2 x DATA REFERENCE CLOCK

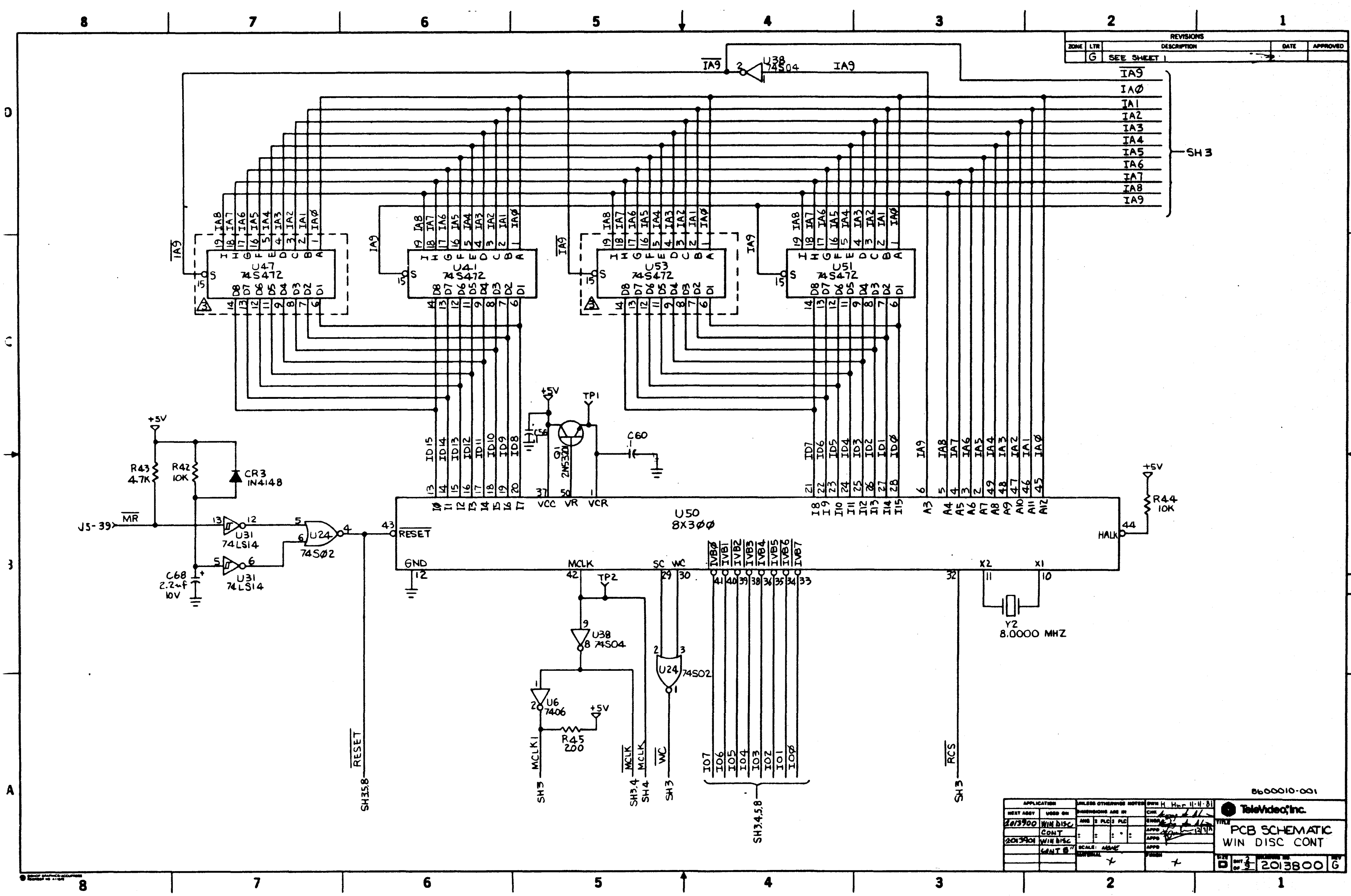
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS ±5%, ¼ W.
2. JUMPER E5 TO E4 TO QUALIFY $\overline{\text{WAIT}}$ BY $\overline{\text{CS}}$
   JUMPER E3 TO E4 IF $\overline{\text{BIC}}$-$\overline{\text{BOC}}$ TO QUALIFY $\overline{\text{WAIT}}$
3. NOT USED, USED ONLY WHEN FOR EXPANDING MEMORY TO 1K.
4. ALL CAPACITOR ARE VALUED IN μf 50V AND ARE 10%.
5. NOT USED FOR 5 1/4" DRIVE.
6. J7 IS FOR 5 1/4" DRIVE, J8 IS FOR 8" DRIVE.

SCG80010-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H. Hsu 11-19-81	TeleVideo, Inc.
NEXT ASSY	USED ON		CHK	
2013900	WIN DISC CONT		ENGR	PCB SCHEMATIC WIN DISC CONT
2013901	WIN DISC CONT 8"	SCALE: None	APVD	
		MATERIAL	APVD	
			FINISH	SIZE D · SHT 1 OF 1 · DRAWING NO. 2013800 · REV G

2013800


U47 74S472
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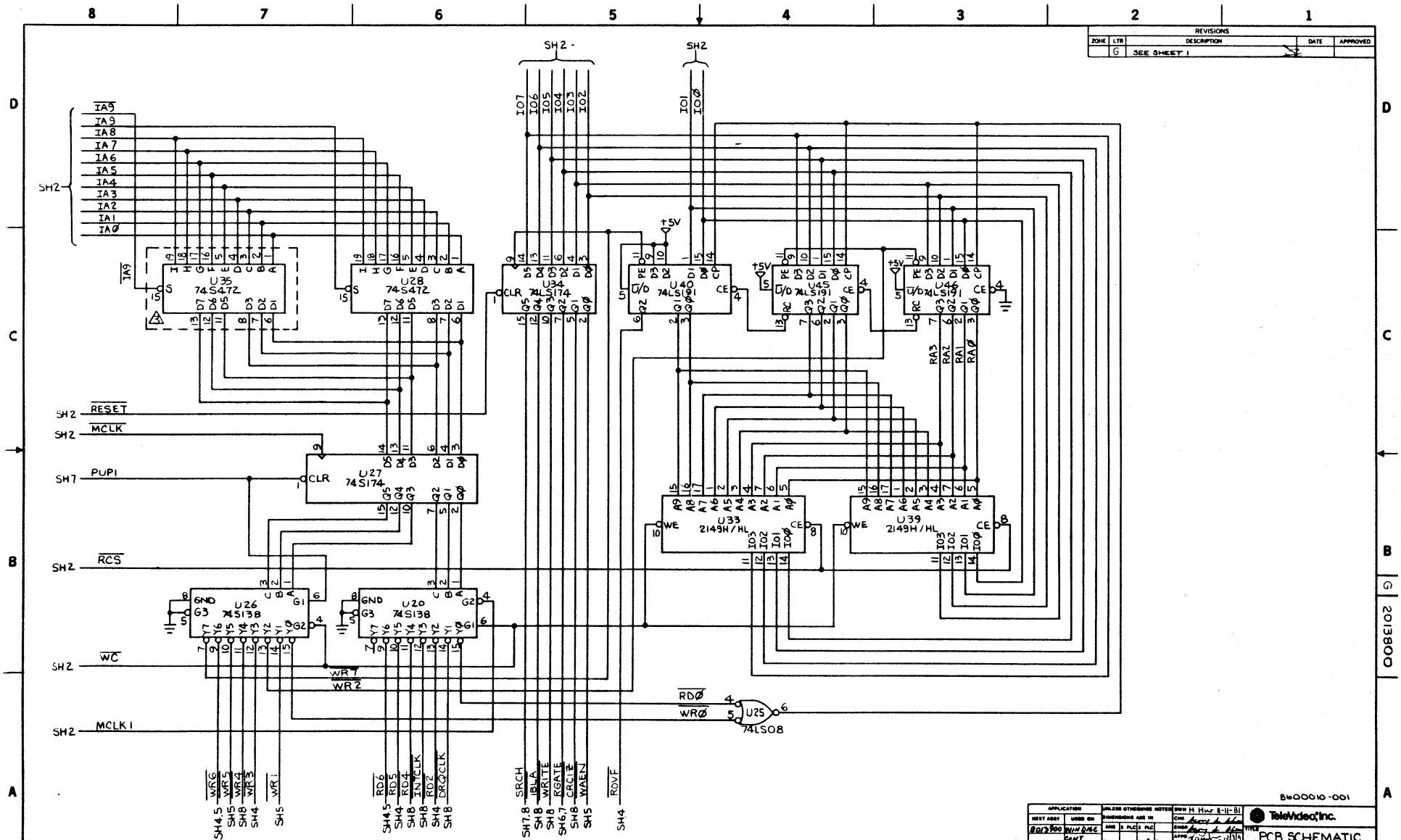
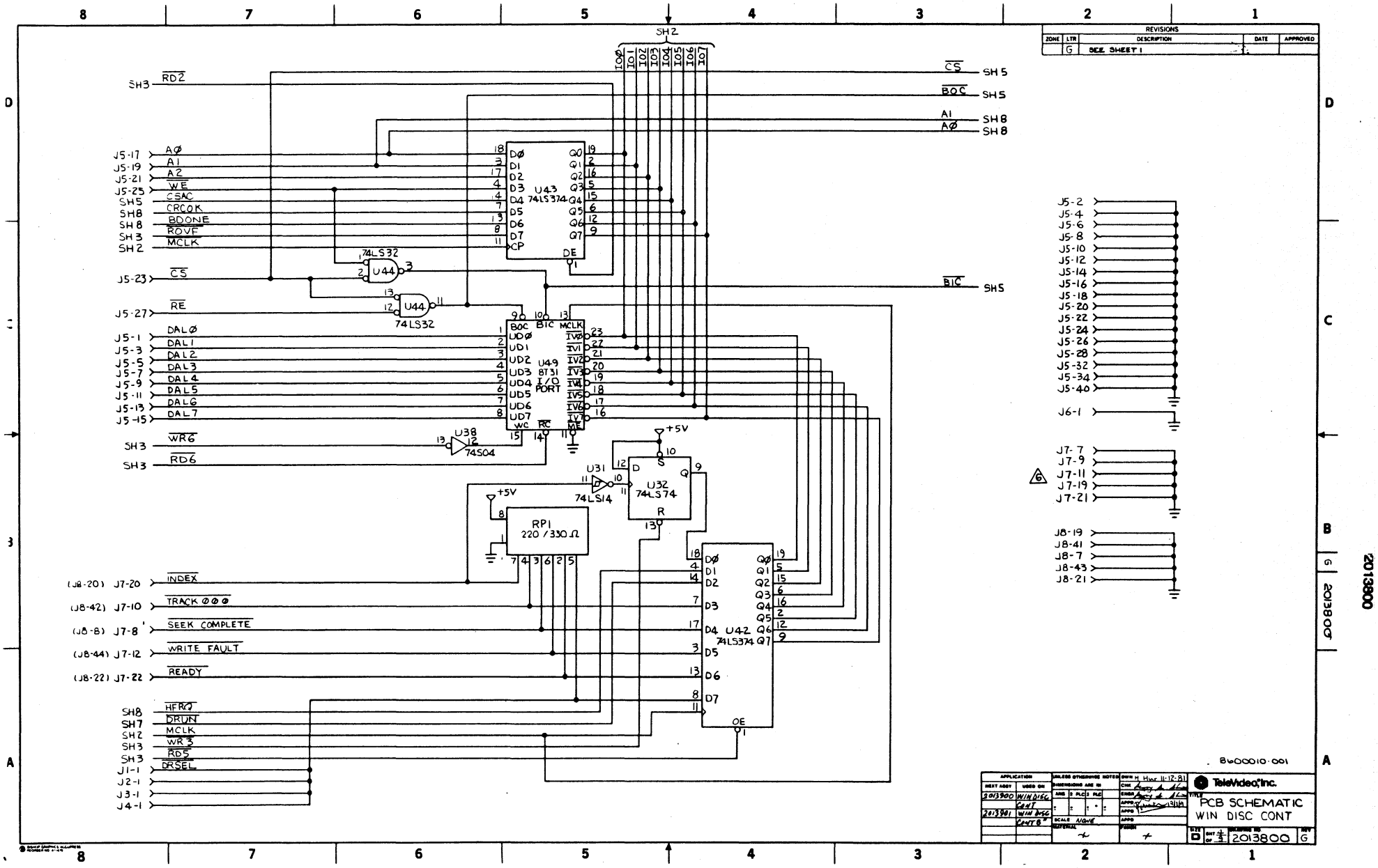
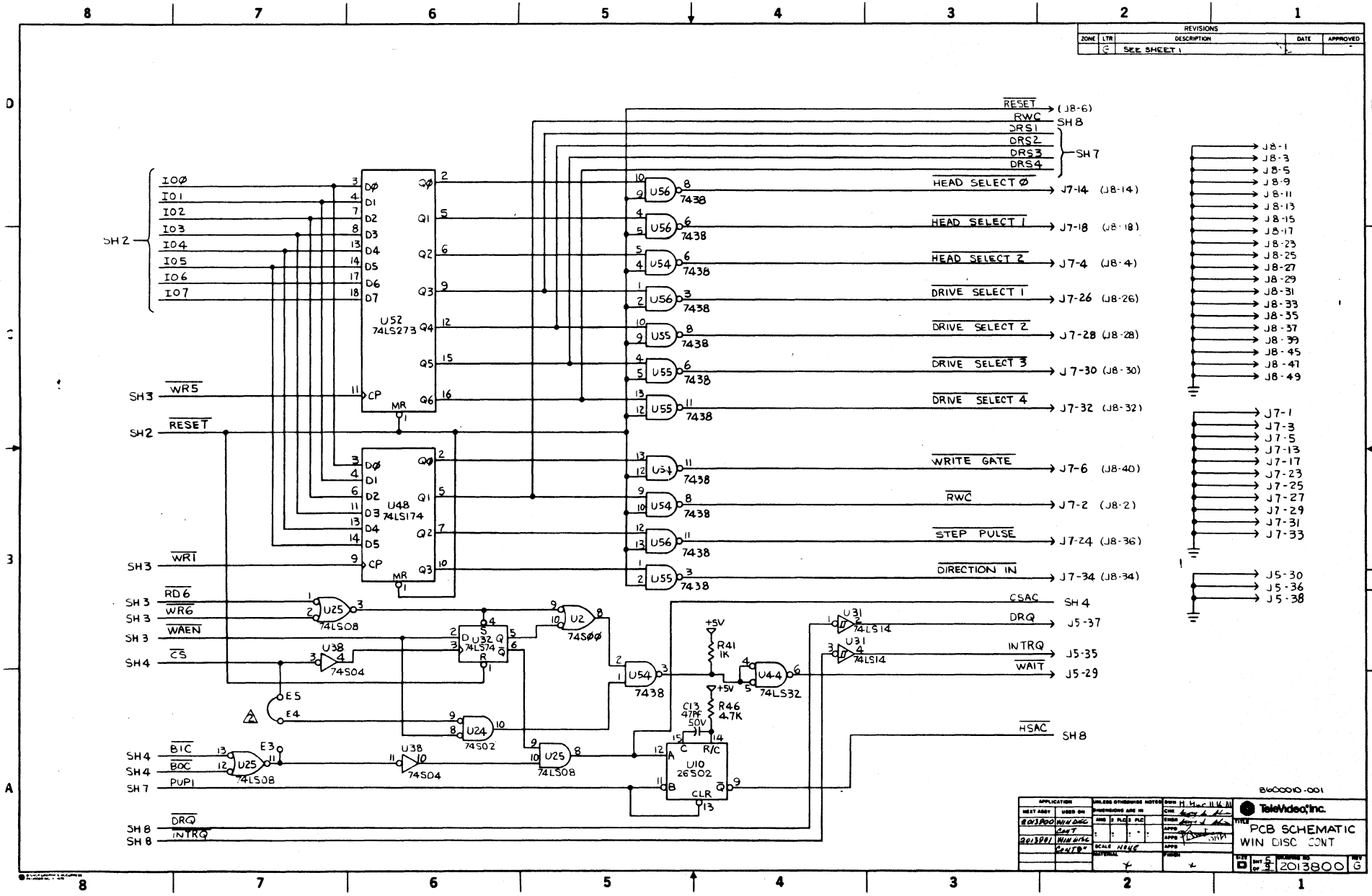
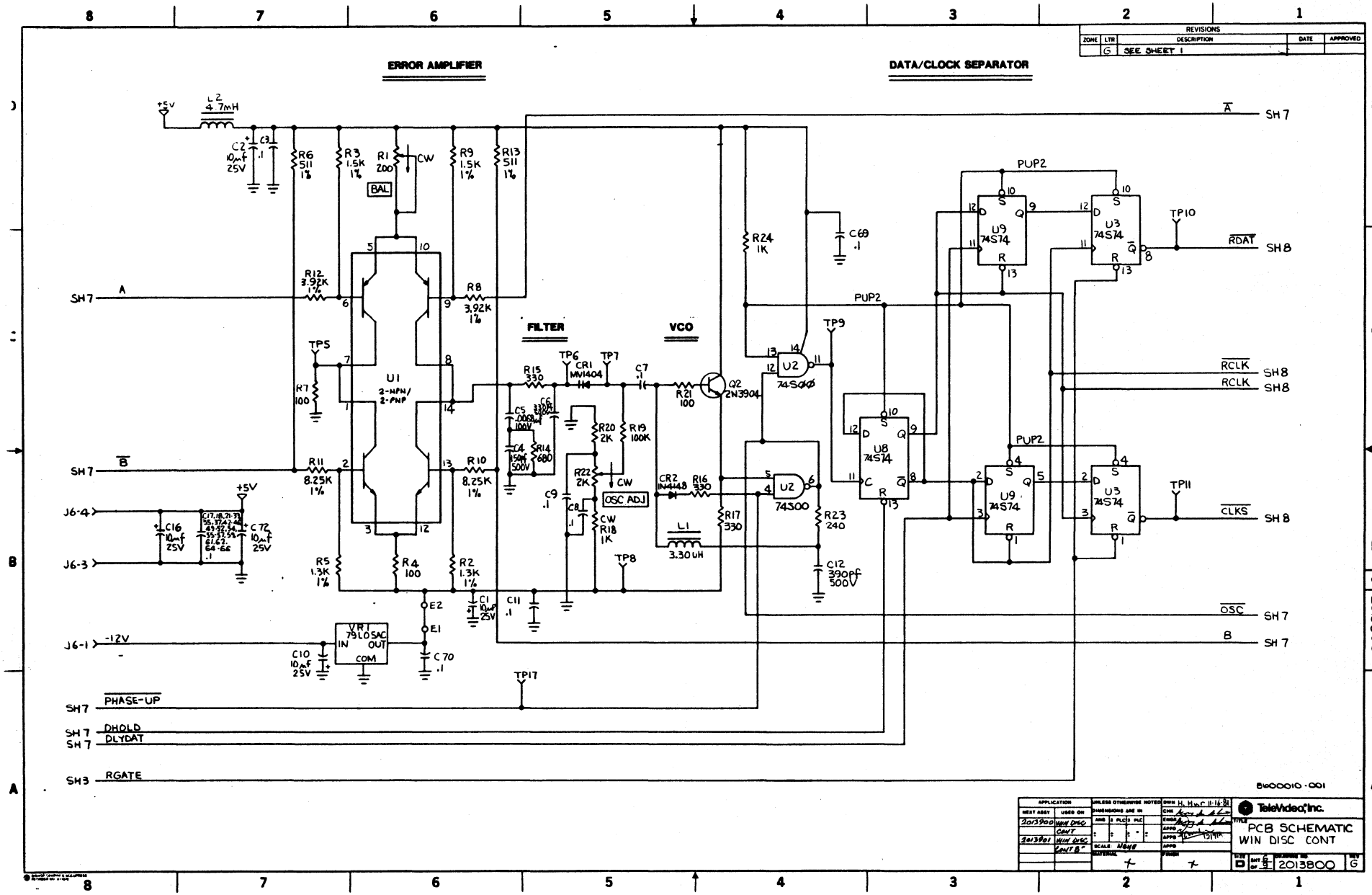
U53 74S472
U51 74S472
U50 8X300
U38 74S04
U31 74LS14
U24 74S02
U6 7406
Q1 2N5320
CR3 1N4148
R43 4.7K
R42 10K
R44 10K
R45 200
C68 2.2uf 10V
C56
C60
Y2 8.0000 MHZ
J5-39
MR
RESET
SH3,5,8
MCLK1
MCLK
WC
RCS
SH3
SH3,4
SH4
SH3,4,5,8
TP1
TP2
+5V
IA0 IA1 IA2 IA3 IA4 IA5 IA6 IA7 IA8 IA9
ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7 ID8 ID9 ID10 ID11 ID12 ID13 ID14 ID15
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
IVB0 IVB1 IVB2 IVB3 IVB4 IVB5 IVB6 IVB7
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
G SEE SHEET 1
8600010-001
TeleVideo, Inc.
PCB SCHEMATIC
WIN DISC CONT
D 2 of 5 2013800 G


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
G | SEE SHEET 1
SH2
IA9
IA8
IA7
IA6
IA5
IA4
IA3
IA2
IA1
IAØ
U35 74S472
U28 74S472
U34 74LS174
U40 74LS191
U45 74LS191
U46 74LS191
+5V
SH2 RESET
SH2 MCLK
SH7 PUPI
U27 74S174
SH2 RCS
U26 74S138
U20 74S138
SH2 WC
WR7
WR2
SH2 MCLK1
RDØ
WRØ
U25 74LS08
U33 2149H/HL
U39 2149H/HL
RA3
RA2
RA1
RAØ
WR6
WR5
WR4
WR3
WR1
RD6
RD5
RD4
INTCLK
RD2
DRQCLK
SRCH
IBLK
WRITE
RGATE
CRCLE
WAEN
ROVF
B400010-001
TeleVideo, Inc.
PCB SCHEMATIC
WIN DISC CONT
2013800 G
2013800


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
G | SEE SHEET 1
SH2
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
SH3 RD2
CS SH5
BOC SH5
A1 SH8
A0 SH8
BIC SH5
J5-17 A0
J5-19 A1
J5-21 A2
J5-25 WE
SH5 CSAC
SH8 CRCOK
SH8 BDONE
SH3 ROVF
SH2 MCLK
J5-23 CS
J5-27 RE
U43 74LS374
74LS32
U44
U49 8731 I/O PORT
J5-1 DAL0
J5-3 DAL1
J5-5 DAL2
J5-7 DAL3
J5-9 DAL4
J5-11 DAL5
J5-13 DAL6
J5-15 DAL7
SH3 WR6
SH3 RD6
U38 74S04
U31 74LS14
U32 74LS74
+5V
RP1 220/330Ω
(J8-20) J7-20 INDEX
(J8-42) J7-10 TRACK 000
(J8-8) J7-8 SEEK COMPLETE
(J8-44) J7-12 WRITE FAULT
(J8-22) J7-22 READY
U42 74LS374
SH8 HFRQ
SH7 DRUN
SH2 MCLK
SH3 WR3
SH3 RD5
SH3 DRSEL
J1-1
J2-1
J3-1
J4-1
J5-2 J5-4 J5-6 J5-8 J5-10 J5-12 J5-14 J5-16 J5-18 J5-20 J5-22 J5-24 J5-26 J5-28 J5-32 J5-34 J5-40
J6-1
J7-7 J7-9 J7-11 J7-19 J7-21
J8-19 J8-41 J8-7 J8-43 J8-21
6
B000010-001
TeleVideo, Inc.
TITLE PCB SCHEMATIC WIN DISC CONT
SIZE D SHT 1 OF 1 DRAWING NO 2013800 REV G
2013800


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
G SEE SHEET 1
RESET (J8-6)
RWC SH8
DRS1
DRS2
DRS3
DRS4
SH7
HEAD SELECT Ø J7-14 (J8-14)
HEAD SELECT 1 J7-18 (J8-18)
HEAD SELECT 2 J7-4 (J8-4)
DRIVE SELECT 1 J7-26 (J8-26)
DRIVE SELECT 2 J7-28 (J8-28)
DRIVE SELECT 3 J7-30 (J8-30)
DRIVE SELECT 4 J7-32 (J8-32)
WRITE GATE J7-6 (J8-40)
RWC J7-2 (J8-2)
STEP PULSE J7-24 (J8-36)
DIRECTION IN J7-34 (J8-34)
CSAC SH4
DRQ J5-37
INTRQ J5-35
WAIT J5-29
HSAC SH8
IOØ
IO1
IO2
IO3
IO4
IO5
IO6
IO7
SH2
U52 74LS273
U48 74LS174
SH3 WR5
SH2 RESET
SH3 WR1
SH3 RD6
SH3 WR6
SH3 WAEN
SH4 CS
SH4 BIC
SH4 BOC
SH7 PUPI
SH8 DRQ
SH8 INTRQ
U56 7438
U55 7438
U54 7438
U53 7438
U25 74LS08
U38 74S04
U32 74LS74
U2 74SØØ
U24 74S02
U10 26S02
U44 74LS32
U31 74LS14
R41 1K
R46 4.7K
C13 47PF 50V
+5V
E3
E4
E5
J8-1
J8-3
J8-5
J8-9
J8-11
J8-13
J8-15
J8-17
J8-23
J8-25
J8-27
J8-29
J8-31
J8-33
J8-35
J8-37
J8-39
J8-45
J8-47
J8-49
J7-1
J7-3
J7-5
J7-13
J7-17
J7-23
J7-25
J7-27
J7-29
J7-31
J7-33
J5-30
J5-36
J5-38
81600010-001
TeleVideo, Inc.
TITLE PCB SCHEMATIC WIN DISC CONT
SIZE D SHT 5 OF 5 DRAWING NO 2013800 REV G
2013800 G

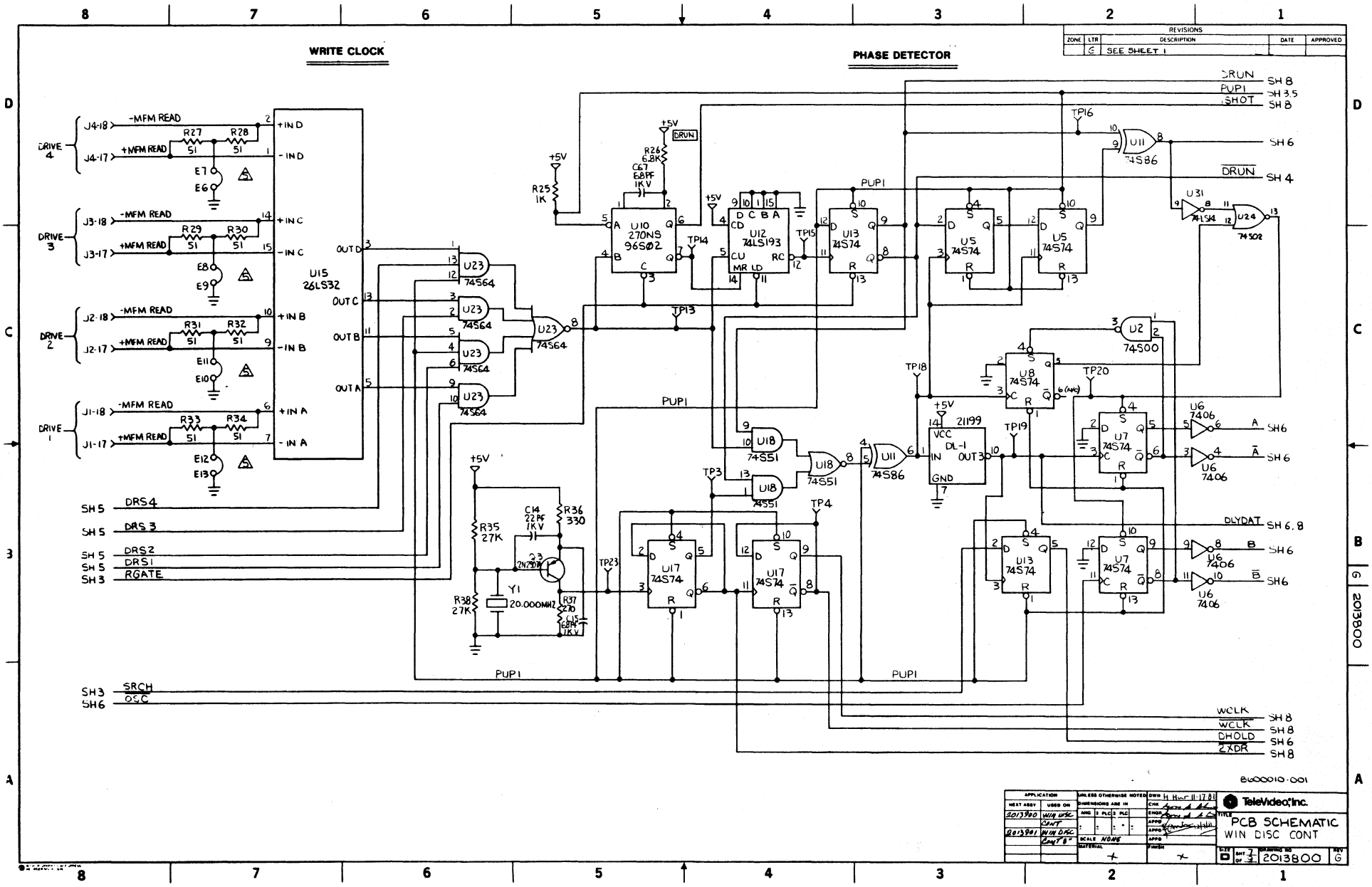


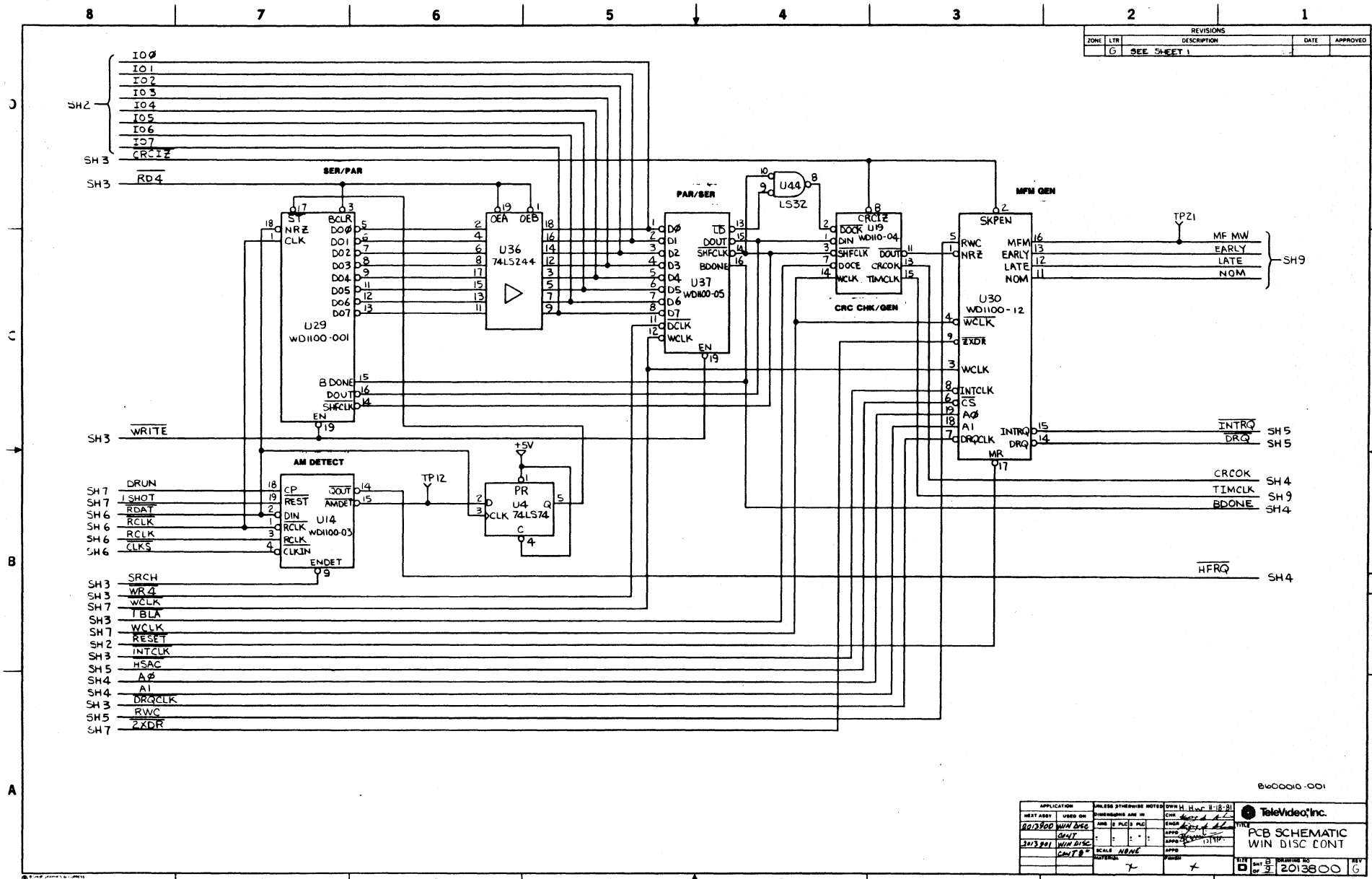
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	G	SEE SHEET 1		

B600010-001

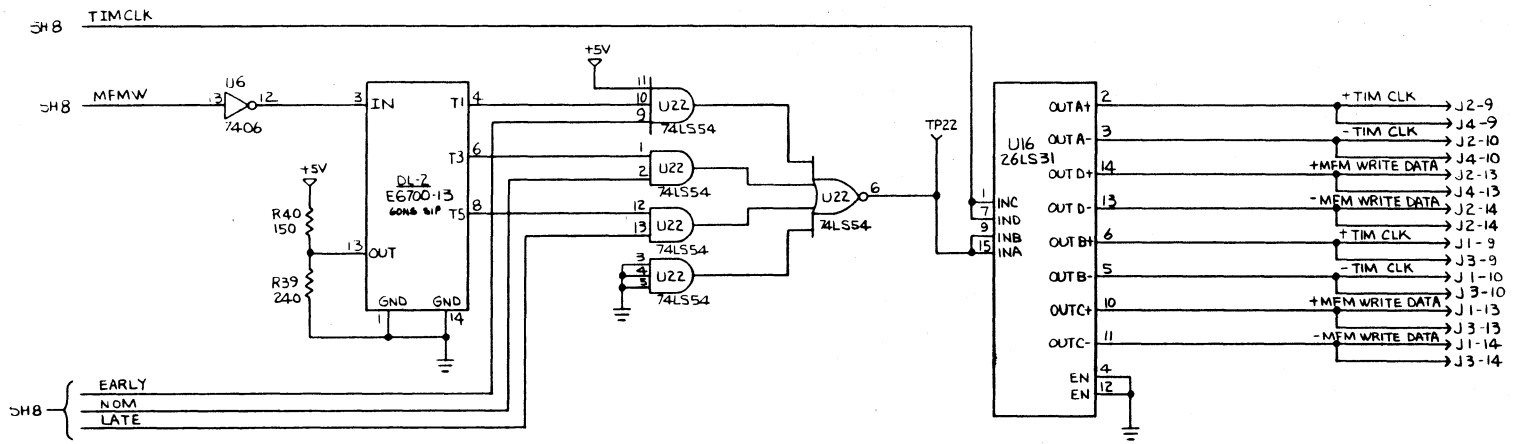
APPLICATION		UNLESS OTHERWISE NOTED	DRN H. Hwc 11-16-81	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2013900	WIN DISC CONT	ANG ±	ENGR	TITLE PCB SCHEMATIC WIN DISC CONT
2013901	WIN DISC CONT'B'	SCALE NONE	APPD	
		MATERIAL —	FINISH —	SIZE D SHT 2 OF 3 DRAWING NO 2013800 REV G

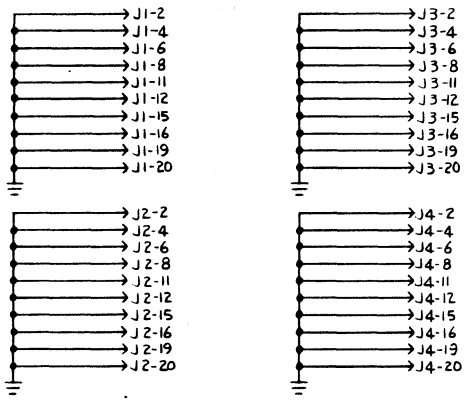
2013800 G


WRITE CLOCK
PHASE DETECTOR
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
G | SEE SHEET 1
DRIVE 4
DRIVE 3
DRIVE 2
DRIVE 1
-MFM READ
+MFM READ
R27 51
R28 51
R29 51
R30 51
R31 51
R32 51
R33 51
R34 51
U15 26LS32
+IN D
-IN D
+IN C
-IN C
+IN B
-IN B
+IN A
-IN A
OUT D
OUT C
OUT B
OUT A
U23 74S64
U10 270NS 96S02
U12 74LS193
U13 74S74
U5 74S74
U11 74S86
U31 74LS14
U24 74S02
U2 74S00
U8 74S74
U7 74S74
U6 7406
U18 74S51
U17 74S74
21199 DL-1
R25 1K
R26 6.8K
C67 68PF 1KV
R35 27K
R36 330
C14 22PF 1KV
R37 270
C15 68PF 1KV
R38 27K
Y1 20.000MHZ
2N2907A
TP3
TP4
TP13
TP14
TP15
TP16
TP18
TP19
TP20
TP23
+5V
DRUN
PUP1
DRS4
DRS 3
DRS2
DRS1
RGATE
SRCH
OSC
SH 8
SH 3.5
SH 6
SH 4
SH 6.8
A
Ā
B
B̄
WCLK
WCLK
DHOLD
2XDR
2013800
8600010-001
TeleVideo, Inc.
PCB SCHEMATIC
WIN DISC CONT
DRAWING NO 2013800
REV G


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
G SEE SHEET 1
SH2 IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7
SH3 CRCIZ
SH3 RD4
SER/PAR
U29 WD1100-001
ST NRZ CLK BCLR DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7
B DONE DOUT SHFCLK EN
U36 74LS244 OEA OEB
PAR/SER
U37 WD1100-05
D0 D1 D2 D3 D4 D5 D6 D7 DCLK WCLK TB DOUT SHFCLK BDONE EN
U44 LS32
CRCIZ
U19 WD110-04
DCCK DIN SHFCLK DOCE WCLK DOUT CRCOK TIMCLK
CRC CHK/GEN
MFM GEN
SKPEN
U30 WD1100-12
RWC NRZ WCLK ZXDR WCLK INTCLK CS A0 A1 DRQCLK MR
MFM EARLY LATE NOM INTRQ DRQ
TP21
MF MW
EARLY
LATE
NOM
SH9
INTRQ SH5
DRQ SH5
CRCOK SH4
TIMCLK SH9
BDONE SH4
HFRQ SH4
SH3 WRITE
AM DETECT
U14 WD1100-03
CP REST DIN RCLK RCLK CLKIN DOUT AMDET ENDET
SH7 DRUN
SH7 1 SHOT
SH6 RDAT
SH6 RCLK
SH6 RCLK
SH6 CLKS
TP12
+5V
PR
U4 74LS74 D CLK Q C
SH3 SRCH
SH3 WR4
SH7 WCLK
SH3 TBLA
SH7 WCLK
SH2 RESET
SH3 INTCLK
SH5 HSAC
SH4 A0
SH4 A1
SH3 DRQCLK
SH5 RWC
SH7 ZXDR
B600010-001
TeleVideo, Inc.
PCB SCHEMATIC
WIN DISC CONT
2013800 WIN DISC CONT B
DRAWING NO 2013800 REV G
SHT 8 OF 9
SIZE D
8 7 6 5 4 3 2 1
A B C D
G
2013800

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	G	SEE SHEET 1		





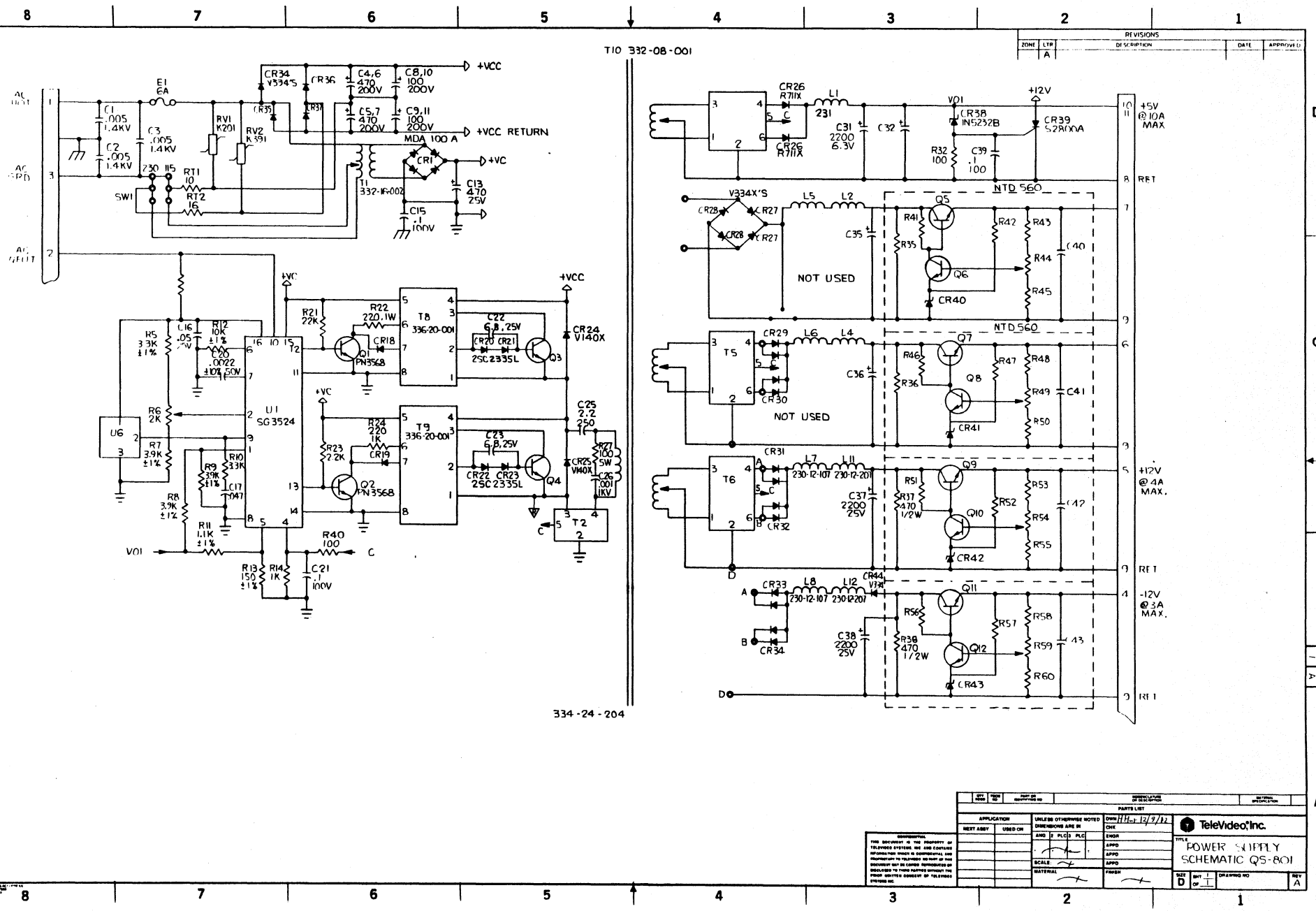
B600010-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		DWN H. Hsu 11-18-81	TeleVideo, Inc.
NEXT ASSY	USED ON			CHK	
2013800	WIN DISC	ANG	2 PLC	3 PLC	ENGR
	Conf	.	:	: . :	APPD
2013801	WIN DISC CONF'G	SCALE NONE			APPD
		MATERIAL X		FINISH	APPD

TITLE: PCB SCHEMATIC WIN DISC CONT

SIZE D | SHT OF SHTS | DRAWING NO. 2013800 | REV G

2013800 G


T10 332-08-001
334-24-204
+VCC
+VCC RETURN
+VC
MDA 100 A
T1 332-16-002
U1 SG3524
T8 336-20-001
T9 336-20-001
T5
T6
T2
Q1 PN3568
Q2 PN3568
Q3 2SC2335L
Q4 2SC2335L
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
NTD 560
NOT USED
+5V @10A MAX
+12V @4A MAX.
-12V @3A MAX.
RET
TeleVideo, Inc.
POWER SUPPLY SCHEMATIC QS-801