Model 950 Maintenance Manual

TeleVideo Systems, Inc.

TELEVIDEO®
950 VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

Document 120021-00-A
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Disclaimer

TeleVideo Systems, Inc. makes no representations or warranties with respect to this manual. Further, TeleVideo Systems, Inc. reserves the right to make changes in the specifications of the product described within this manual at any time without notice and without obligation of TeleVideo Systems, Inc. to notify any person of such revision or changes.

TeleVideo Systems, Inc., 550 East Brokaw Road, San Jose, California 95112 408/971-0255

TABLE OF CONTENTS

LIST OF FIGURES

Section 4

Section 6

STATEMENT OF LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to its distributors, systems houses, end users, and OEMs ("Buyer") that products manufactured by TeleVideo are free from defects in materials and workmanship. TeleVideo's obligations under this warranty are limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship within one year after shipment by TeleVideo.

Products may be returned to Buyer only after a Return Material Authorization number ("RMA") has been obtained from TeleVideo by telephone or in writing. Buyer will prepay all freight charges to return any products to the repair facility designated by TeleVideo and include the RMA number on the shipping container. TeleVideo will, at its option, either repair the defective products or parts or deliver replacements for defective products or parts on an exchange basis to Buyer, freight prepaid to the Buyer. Products returned to TeleVideo under this warranty will become the property of TeleVideo. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof, applies.

Exclusions

This limited warranty does not cover losses or damage which occur in shipment to or from Buyer, or are due to, (1) improper installation or maintenance, misuse, neglect, or any cause other than ordinary commercial or industrial application, or (2) adjustment, repair, or modifications by other than TeleVideo-authorized personnel, or (3) improper environment, excessive or inadequate heating or air conditioning and electrical power failures, surges, or other irregularities, or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors or agents, unless confirmed in writing by a TeleVideo officer.

If the firmware or hardware is altered or modified by the Buyer, this firmware and hardware is not covered within this limited warranty and the Buyer bears sole responsibility and liability for that firmware and hardware.

THE FOREGOING TELEVIDEO LIMITED WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER ORAL, WRITTEN, EXPRESSED, IMPLIED, OR STATUTORY. IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE DO NOT APPLY. TELEVIDEO'S WARRANTY OBLIGATIONS AND DISTRIBUTOR'S REMEDIES HEREUNDER ARE SOLELY AND EXCLUSIVELY AS STATED HEREIN.

TELEVIDEO'S LIABILITY, WHETHER BASED ON CONTRACT, TORT, WARRANTY, STRICT LIABILITY, OR ANY OTHER THEORY, SHALL NOT EXCEED THE PRICE OF THE INDIVIDUAL UNIT WHOSE DEFECT OR DAMAGE IS THE BASIS OF THE CLAIM. IN NO EVENT SHALL TELEVIDEO BE LIABLE FOR ANY LOSS OF PROFITS, LOSS OF USE OF FACILITIES OR EQUIPMENT, OR OTHER INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Service Out of Warranty

If your terminal is out of warranty when it needs service, follow the same procedure to receive an RMA. You will be responsible for all shipping costs.

If your company requires a purchase order for out-of-warranty repairs, let us know the purchase order number when you call in. One purchase order may cover several repairs, but we will give each unit its own individual RMA number. This allows us to return each unit quickly without holding up the entire purchase order for one unit.

Extended Warranty

TeleVideo offers an Extended Warranty Agreement, which extends the terms of the above-stated Limited Warranty for an additional year. To take advantage of this Extended Warranty, you must sign the Extended Warranty Agreement and return it, together with full payment, to TeleVideo before the Limited Warranty expires. Shipping charges are not included in the Extended Warranty. This is normally the only expense you incur. Please contact the Customer Service department or your sales representative for details. To renew the Extended Warranty for another year, follow the same procedure.

ORDERING SPARE PARTS

Order parts directly from the Spare Parts Order Entry Department in San Jose, California. The toll free numbers are 800/821-3774 (inside California) or 800/521-4897 (outside California). Please have the purchase order number and TeleVideo part number ready when you call. International customers can telex 910-339-9621, attention Spares Order Entry.

Contract customers and institutions can order parts on a purchase order and be invoiced. All other customers must order parts on a C.O.D. or cash-in-advance basis.

All orders have a $50 minimum. Add 6.5 percent sales tax to orders placed in California. Since we do not make any drop shipments, please include the shipping and billing addresses with your order. Shipments are Best Way, which is UPS. Although special shipping requests will be accommodated, any extra costs incurred will be added to the invoice.

REGIONAL SALES OFFICES

East
6900 Jericho Turnpike
Suite 100 LL
Syosset, NY 11791
(516) 496-4777

Northeast
1601 Trapelo Road
Reservoir Place
Waltham, MA 02154
(617) 890-3282

West
18662 MacArthur Blvd.
Suite #107
Irvine, CA 92715
(714) 476-0244

Northwest
550 East Brokaw Road
P.O. Box 6602
San Jose, CA 95150-6602
(408) 971-0255

South
5525 High Point Drive
Suite #101
Irving, TX 75062
(214) 258-6776

Midwest
1002 E. Algonquin
Suite #112
Schaumburg, IL 60195
(312) 397-5400

Southeast
6075 The Corners Parkway
Suite #208
Norcross, GA 30092
(404) 447-1231

Central Europe
Saturnusstraat 25
2132 HB Hoofddorp
The Netherlands
Phone: 011-31-2503-35444
Telex: 74615 TLVDO NL

Northern Europe
Dorna House,
Guildford Rd., West End
Surrey GU249PW
England
Phone: 011-44-9-905-6464
Telex: 858922

Southern Europe
3 rue leCorbusier
bat. Berne Silic 244
94568 Rungis Cedex,
France
Phone: 011-33-686-4412
Telex: 205191F

TeleVideo Systems, Inc.

January 7, 1985
TERMINAL DIVISION SPARE PART PRICE LIST

DESCRIPTION	NEW P/N	LIST PRICE
OPERATORS MANUALS		
INSTAL & USERS GUIDE PERSONAL TERMINAL	130624-00	10.00
INSTAL & USERS GUIDE 914	130316-00	10.00
INSTAL & USERS GUIDE 924	130903-00	10.00
INSTAL & USERS GUIDE 910	120025-00	10.00
INSTAL & USERS GUIDE 910PLUS	120046-00	10.00
INSTAL & USERS GUIDE 912/920	120018-00	10.00
INSTAL & USERS GUIDE 925	120035-00	10.00
INSTAL & USERS GUIDE 950	120020-00	10.00
INSTAL & USERS GUIDE 921	131961-00	10.00
INSTAL & USERS GUIDE 925E	131960-00	10.00
INSTAL & USERS GUIDE 970	122446-00	10.00
INSTAL & USERS GUIDE 970/50	130902-00	25.00
INSTAL & USERS GUIDE 922	130906-00	10.00
MAINTENANCE MANUALS		
MAINTENANCE MANUAL 910/910PLUS	120026-00	50.00
MAINTENANCE MANUAL 912/920	120019-00	50.00
MAINTENANCE MANUAL 925	120036-00	50.00
MAINTENANCE MANUAL 950	120021-00	50.00
MAINTENANCE MANUAL 970	130021-00	50.00
MAINTENANCE MANUAL 914	130623-00	50.00
MAINTENANCE MANUAL 924	130622-00	50.00
MAINTENANCE MANUAL 921	131967-00	50.00
MAINTENANCE MANUAL 925E	131966-00	50.00
MAINTENANCE MANUAL PERSONAL TERMINAL	130825-00	50.00
MAINTENANCE MANUAL 922	130621-00	50.00

MODULES

POWER SUPPLY MODULE	121957-00	100.00
POWER SUPPLY MODULE 970	122257-00	150.00
VIDEO MODULE	121958-00	100.00
VIDEO MODULE 970	122269-00	110.00
VIDEO MODULE PERSONAL TERMINAL	130830-00	100.00
VIDEO MODULE/POWER SUPPLY 914/924	130851-00	220.00
LOGIC BOARD 910 TTL	120140-00	395.00
LOGIC BOARD 910 G/A	120140-01	395.00
LOGIC BOARD 910PLUS TTL	120140-02	395.00
LOGIC BOARD 910PLUS G/A	122469-00	395.00
LOGIC BOARD 912/920B TTL	120090-00	458.00
LOGIC BOARD 912/920C TTL	120090-02	458.00
LOGIC BOARD/POWER SUPPLY PERSONAL TERM.	130898-00	250.00
LOGIC BOARD 925 TTL	120155-00	514.00
LOGIC BOARD 925 G/A	120155-01	514.00
LOGIC BOARD 950 TTL	120095-00	539.00
LOGIC BOARD 950 G/A	120095-01	539.00
LOGIC BOARD 970 G/A (TTL Not Available)	120210-02	750.00
LOGIC BOARD 914	130320-00	325.00
LOGIC BOARD 924	130050-00	465.00
LOGIC BOARD 921	131260-00	385.10
LOGIC BOARD 925E	130990-00	365.00
KEYBOARD ASSEMBLY 910/910PLUS	120900-01	126.00
KEYBOARD ASSEMBLY 912B	122065-00	126.00
KEYBOARD ASSEMBLY 912C	120900-00	126.00
KEYBOARD ASSEMBLY 920B	120899-00	126.00
KEYBOARD ASSEMBLY 920C	120901-00	126.00
KEYBOARD ASSEMBLY 914	130119-00	180.00
KEYBOARD ASSEMBLY 924/925E/921	130057-00	210.00
KYBD ASSEMBLY W/HOUSING 925/950	120902-00	210.00
KYBD ASSEMBLY W/HOUSING 970	121837-00	210.00
KEYBOARD ASSEMBLY PERSONAL TERMINAL	130093-00	150.00
TUBE B/W P4 12"	120491-00	179.00
TUBE GREEN P31 12"	120493-00	179.00
TUBE GREEN P31 14"	122187-00	192.00
TUBE 9" CRT (AMBER)	123550-00	100.00
TUBE 12" CRT (AMBER)	130462-00	179.00

OPTIONS*

PATTERN GENERATOR (912/950 INSTALLED)	121223-00	200.00
DEMO PROGRAM EPROM 910	180000-94	16.00
DEMO PROGRAM EPROM 910PLUS	180000-73	16.00
DEMO PROGRAM EPROM 925	180000-72	16.00
DEMO PROGRAM EPROM 950	180000-74	16.00
DEMO PROGRAM EPROM 970	180001-19	16.00
DEMO PROGRAM EPROM 914	180001-91	16.00
DEMO PROGRAM EPROM 924	180001-66	16.00
DEMO PROGRAM EPROM PT	180002-18	16.00
CONVERSION KIT 910	121697-00	25.00
CONVERSION KIT 910PLUS	121691-00	25.00
CONVERSION KIT 970/50 TTL	130073-00	100.00
CONVERSION KIT 970/50 GATE ARRAY	130649-00	100.00
CONVERSION KIT CP/M WORDSTAR 925	122509-00	100.00
CONVERSION KIT CP/M WORDSTAR 950	121874-00	100.00
CURRENT LOOP KIT 910/910PLUS	121310-00	50.00
CURRENT LOOP KIT 925/924/914	121311-00	60.00
MEMORY KIT 2ND PAGE 912/920	120014-00	35.00
MEMORY KIT 2ND PAGE 925/950	120015-00	46.00
MEMORY KIT 3RD 4TH PAGE 950	120016-00	80.00
MEMORY KIT 2ND 3RD 4TH PAGE 950	122317-00	120.00
MEMORY KIT 924	132093-00	160.00
EMULATION KIT 925 (ADDS REGENT)	122499-00	100.00
300/1200 BAUD MODEM PERSONAL TERMINAL	130615-00	549.00
300 BAUD MODEM PERSONAL TERMINAL	130617-00	150.00
HANDSET PERSONAL TERMINAL	130616-00	79.95
CARRYING CASE PERSONAL TERMINAL	130810-00	69.00
925E 2ND PAGE OPTION BOARD KIT	132098-00	125.00
970 RS-422 INTERFACE	120870-00	100.00
970 GRAPHICS MOUSE	130892-00	149.00

ELECTRICAL COMPONENTS CAPACITORS

CAP CERAMIC .02uF 50V	130186-00	.83
CAP CERMAIC 150pF 50V 100%	130138-00	.83
CAP CERAMIC 1.0pF 1KV SPARK GAP	120309-00	2.35
CAP CERAMIC 220pF 50V	121959-00	.83
CAP CERAMIC .01uF 50V	130178-00	.83
CAP CERAMIC .01uF 16V 20%	120287-00	.83
CAP CERAMIC 330PF 50V 20%	120291-00	.83
CAP CERAMIC 3300uF 10V	130276-00	.83
CAP CERAMIC .1uF 50V 10%	120301-00	.83
CAP ELECTROLYTIC 1uF 10V	122614-00	.83
CAP ELECTROLYTIC (NON-P) 16uF 25V	122800-00	5.32
CAP ELECTROLYTIC 22uF 16V 20%	120257-00	.83
CAP ELECTROLYTIC 10uF 16V +80%	130176-00	.83
CAP ELECTROLYTIC 2.2uF 25V 10%	120265-00	.83
CAP ELECTROLYTIC 22uF 16V 20%	130189-00	.83
CAP ELECTROLYTIC 22uF 35V	120261-00	.83
CAP ELECTROLYTIC 4.7uF 35V 10%	120269-00	2.39
CAP ELECTROLYTIC 10uF 16V 20%	120273-00	.83

*ALL GRAPHICS EMULATIONS MUST NOW BE PURCHASED AS TOP ASSY'S.
*SPARE PARTS WILL NO LONGER CARRY THE GRAPHICS EMULATIONS.

CAP ELECTROLYTIC 1uF 16V 10%	120279-00	1.24
CAP ELECTROLYTIC 100uF 10V	121960-00	.83
CAP ELECTROLYTIC 22uF 100V	121961-00	.83
CAP ELECTROLYTIC 2.2KuF 10V	121962-00	2.62
CAP ELECTROLYTIC 2.2KuF 16V	130164-00	7.59
CAP ELECTROLYTIC 100uF 160V	121963-00	7.59
CAP ELECTROLYTIC 22uF 160V	121964-00	1.46
CAP ELECTROLYTIC 22uF 16V +20%	130175-00	.83
CAP ELECTROLYTIC 220uF 16V	121993-00	.83
CAP ELECTROLYTIC 220uF 25V	130127-00	.83
CAP ELECTROLYTIC 1000uF 16V	130185-00	.83
CAP ELECTROLYTIC 3.3KuF 35V	121965-00	7.45
CAP ELECTROLYTIC 3300uF 50V	130281-00	6.83
CAP ELECTROLYTIC 2000uF 35V	130275-00	3.73
CAP ELECTROLYTIC 4.7KuF 16V	121966-00	7.54
CAP ELECTROLYTIC 4.7uF 16V	121967-00	.83
CAP ELECTROLYTIC 47 uF 35V	130648-00	1.15
CAP ELECTROLYTIC 470uF 35V	121982-00	1.93
CAP ELECTROLYTIC 470uF 35V A/L+-20%	130211-00	1.40
CAP ELECTROLYTIC 3300uF 16V	130618-00	7.83
CAP ELECTROLYTIC 680 uF 16V	130584-00	.83
CAP ELECTROLYTIC 100uF 100V	130827-00	1.17
CAP DIP MICA 10pF 50V 5%	120241-00	.83
CAP MICA 20pF 50V 5%	120243-00	.83
CAP MICA 100pF 50V 5%	120247-00	.83
CAP MICA 47pF 50V 5%	120249-00	.83
CAP MICA 150pF 500V 1%	120251-00	.83
CAP MICA 330pF 500V 5%	120253-00	1.09
CAP MICA 390pF 500V 5%	120255-00	1.23
CAP MONOLYTHIC .01uF 50V 10%	120289-00	.83
CAP MONOLYTHIC 330pF 100V 20%	120293-00	.83
CAP MONOLYTHIC 22pF 50V +-10% A/L	130196-00	.83
CAP MONOLYTHIC 47pF 100V 5%	120295-00	1.24
CAP MONOLYTHIC 68pF 1KV 20%	120299-00	.83
CAP MONOLYTHIC .039uF 50V 10%	120303-00	.83
CAP MONOLYTHIC .039uF 50V 5%	120305-00	1.24
CAP MONOLYTHIC 100pF 100V 5%	120307-00	1.24
CAP MONOLYTHIC .1uF 50V +-5%	121868-00	.83
CAP MYLAR .1pF 100V	130169-00	.83
CAP MYLAR .047uF 50V	130168-00	.83
CAP MYLAR .0068uF 100V 5%	120281-00	.83
CAP MYLAR .0068uF 200V	121968-00	.83
CAP MYLAR .001uF 50V	121969-00	.83
CAP MYLAR .01uF 50V	121970-00	.83
CAP MYLAR .015uF 50V 5%	130139-00	.83
CAP MYLAR .033uF 400V	130126-00	.83
CAP MYLAR .039uF 50V	130145-00	.83
CAP MYLAR .47uF 50V	121971-00	.83
CAP MYLAR .47uF 50V	121972-00	1.66
CAP MYLAR .47uF 100V	130188-00	3.24
CAP MYLAR .1uF 600V	121973-00	1.55
CAP MYLAR .1uF 800V 10%	130184-00	1.10
CAP MYLAR .47uF 400V	121975-00	2.14
CAP TANTALUM .22uF 35V	120285-00	.83
CAP TANTALUM .68uF 50V	120259-00	2.00

CAP TANTALUM 2.2uF 35V	130274-00	.83
CAP TANTALUM 3.3uF 50V 10%	120263-00	2.76
CAP TANTALUM 4.7uF 16V +-20%	130177-00	1.52
CAP TANTALUM 10uF 25V 10%	120271-00	2.28
CAP TANTALUM 4.7uF 16V 10%	120275-00	1.10
CAP TANTALUM 4.7uF 25V	130284-00	.83
CAP TANTALUM .33uF 35V	121981-00	1.38
CAP GL PK 10pF 25V +-20%	130171-00	.83
CAP GL PK .1uF 25V +80%	130172-00	.83
CAP GL PK 330pF 25V +80%	130173-00	.83
CAP GL PK .01uF 25V +80%	130174-00	.83
CAP GL PK 47 pF 50V	130179-00	.83
CAP GL PK 100pF 50V +-10%	130183-00	.83
CAP GL PK .001uF 25V +80/-20%	130190-00	.83
CAP GL PK 150pF 50V +-20%	130202-00	.83
CAP A/L 3300uF 25V +-20%	130212-00	4.12

DIODES - REGULATORS - TRANSISTORS

DIODE ZENER IN759A/RD12EB	122016-00	2.09
DIODE ZENER IN747	122070-00	.83
DIODE IN914	120475-00	.83
DIODE IN920/KDS8513A	122018-00	4.97
DIODE IN4001	120477-00	1.05
DIODE IN4004/DS-130TB	122022-00	1.15
DIODE IN5391/DS135D	122006-00	.83
DIODE DSA17C/MR500	122015-00	2.23
DIODE DS18/IDS135D	122014-00	.83
DIODE DS113A/MRI-1000	122017-00	7.23
DIODE LED MV55A RED	120481-00	3.45
DIODE P6KE	120479-00	4.83
DIODE PLR 817	130147-00	.83
DIODE PFR 852	130251-00	.83
DIODE BY251 3A 200V	130098-00	.83
DIODE SWITCH IN4148	120485-00	.83
DIODE ZENER 8.2V	122445-00	.83
DIODE 2AMP 100V BRIDGE	130213-01	1.36
DIODE FAST RECOV RCTFIR 1AMP 800V	130147-00	.83
REGULATOR 79M12	121265-00	2.00
REGULATOR LAS1512	122025-00	40.25
REGULATOR LAS16CB	121269-00	21.39
REGULATOR SI-3122V	123540-00	6.90
REGULATOR LM 317T 1.5A	130496-00	4.14
REGULATOR LAS1605	121268-00	27.26
REGULATOR LAS1812	122024-00	40.25
REGULATOR 78MO5	121261-00	4.55
REGULATOR 79LO5AC	121262-00	2.77
REGULATOR 7912	130018-00	3.66
REGULATOR SI-80506Z	122464-00	36.64
REGULATOR SI-3052P/STR9005 924/914 IC101	130643-00	17.94
TRANSISTOR 2N5320 PWR	120463-00	3.28
TRANSISTOR HORIZ 60V KTC2233 TO220	130118-00	2.69
TRANSISTOR 2N2219A	120453-00	4.14
TRANSISTOR 2N2222A NPN/SILICON	120469-00	14.84
TRANSISTOR 2N2907A	120459-00	1.12

TRANSISTOR 2N3019	120457-00	3.04
TRANSISTOR 2N3906/2SA495	120422-00	1.05
TRANSISTOR 2N4401/2SC1166	120455-00	2.32
TRANSISTOR 2SC983	120471-00	3.00
TRANSISTOR 2N6121/2SC1173	121997-00	4.60
TRANSISTOR 2N6124/2SA473	122021-00	4.92
TRANSISTOR 2SC2373	120473-00	5.32
TRANSISTOR KTC 1627A	120467-00	2.38
TRANSISTOR 2N3904/KTC1815	120465-00	5.18
TRANSISTOR KTC 2229Y	130116-00	.83
TRANSISTOR KTC 1815Y	130146-00	3.11
TRANSISTOR KTA 1015Y	130167-00	.83
TRANSISTOR KTC 200Y	130117-00	.83

FIRMWARE

SYSTEM PROG EPROM PT 300 (U1)	180001-90	43.13
SYSTEM PROG EPROM PT 1200 (U1)	180002-00	43.13
SYSTEM PROG EPROM 910	180000-20	43.13
SYSTEM PROG EPROM 910PLUS	180000-40	28.75
SYSTEM PROG ROM 910	180000-15	21.74
SYSTEM PROG ROM 912/920B (A49B1)	120338-00	29.67
SYSTEM PROG ROM 912/920C (A49C1)	120340-00	29.67
SYSTEM PROG EPROM 925 A	180000-33	43.13
SYSTEM PROG EPROM 925 B	180000-31	43.13
SYSTEM PROG ROM 950 (-001A)	180000-01	21.74
SYSTEM PROG ROM 950 (-007A)	180000-07	21.74
SYSTEM PROG EPROM 950 (043X)	180000-43	43.13
SYSTEM PROG EPROM 950 (044X)	180000-44	43.13
SYSTEM EPROM 970 G/A (U70)	180001-61	43.13
SYSTEM EPROM 970 G/A (U71)	180001-62	43.13
SYSTEM EPROM 970 G/A (U72)	180001-63	43.13
SYSTEM EPROM 970 G/A (U73)	180001-64	43.13
SYSTEM EPROM 924 AOOO (U14)	180001-53	28.57
SYSTEM EPROM 924 EOOO (U21)	180001-54	28.57
SYSTEM EPROM 970 TTL (A82)	180001-00	43.13
SYSTEM EPROM 970 TTL (A87)	180001-01	43.13
SYSTEM EPROM 970 TTL (A99)	180001-02	43.13
SYSTEM EPROM 970/950 (A82)	180001-70	43.13
SYSTEM EPROM 970/950 (A87)	180001-71	43.13
SYSTEM EPROM 970/950 (A99)	180001-72	43.13
SYSTEM EPROM 914 (U7)	180001-73	43.13
33333M EPROM 921 (U7)	180002-33	43.13
SYSTEM EPROM 925E (U7)	180002-28	43.13
PROG MICROCOMPTR 8749	180000-68	43.13
CHAR GEN EPROM 910/910PLUS	180000-21	43.13
CHAR GEN ROM 910/910PLUS	180000-16	21.74
CHAR GEN ROM 912/920 (A3-2)	120346-00	17.18
CHAR GEN ROM 924 (U10)	180001-42	43.13
CHAR GEN EPROM 925	180000-21	43.13
CHAR GEN ROM 925	180000-16	21.74
CHAR GEN ROM 950 (003A)	180000-03	21.74
CHAR GEN ROM 950 (002A)	180000-02	21.74
CHAR GEN EPROM US/UK 970	180001-39	43.13
CHAR GEN ROM 914 (U19)	180001-74	43.13

KYBD ENCDR 910/910PLUS (W/INTERNAL EPROM)	120518-00	25.86
KYBD CPU 925/950 8048 (U6)	180000-09	43.13
KYBD CPU 914/924/970 (A6) 8049	121390-00	43.13
* KYBD EPROM PRO 910/910PLUS (A2)	180000-19	24.15
* KYBD ENCDR PRO 910/910PLUS (A1)	120532-00	25.86

* These two parts are used together in a two chip set

INTEGRATED CIRCUITS

IC 74S00	120240-00	2.53
IC 74LS00	120242-00	1.98
IC 74LS03	120244-00	1.98
IC 74S04	120246-00	2.77
IC 74LS04	120248-00	2.07
IC 74LS05	120250-00	2.07
IC 74LS08	120252-00	2.07
IC 74LS10	120254-00	2.07
IC 74SL20	120256-00	2.00
IC 74LS32	120258-00	2.14
IC 74LS42	120260-00	2.93
IC 74LS51	120262-00	2.07
IC 74S74	120264-00	4.12
IC 74H74	130232-00	3.45
IC 74LS86	120268-00	2.38
IC 74LS109	120270-00	2.30
IC 74LS139	120272-00	3.66
IC 74LS145	121700-00	3.54
IC 74LS157	120274-00	3.17
IC 74LS163	120276-00	5.24
IC 74LS166	120278-00	5.80
IC 74LS173	120280-00	4.76
IC 74LS174	120282-00	3.66
IC 74LS253	120284-00	3.73
IC 74LS367	120286-00	3.17
IC 74LS373	120288-00	4.00
IC 74LS374	120290-00	4.00
IC 75188N/1488	120292-00	4.76
IC 75189AN/1489	120294-00	4.76
IC TIL117	120298-00	5.15
IC NE555	120302-00	2.97
IC DP8304	120304-00	20.23
IC AMD2111-4A	120306-00	15.32
IC 2502HP	120308-00	17.85
IC TMS9927/5027	120310-00	94.02
IC P8035	120312-00	47.21
IC H11G3	120342-00	3.97
IC 7406	120348-00	2.36
IC 4N38	120350-00	4.97
IC 7414	120354-00	2.21
IC 2114	120358-00	11.21
IC 74LS245/N8T245N	120362-00	6.62
IC 74LS191	120366-00	3.11
IC 74LS273	120376-00	4.00
IC 74S240	120378-00	10.14

IC 74LS175	120380-00	2.00
IC 74S32/629	120388-00	2.07
IC 74LS11	120400-00	1.31
IC 93S16PC	120408-00	7.59
IC 74LS138	120410-00	1.93
IC 74LS02	120416-00	1.31
IC 74LS241	120420-00	4.07
IC AM26LS31	120424-00	9.11
IC AM26LS32	120426-00	9.11
IC 74LS240	120440-00	4.07
IC 74LS244	120442-00	6.35
IC 74S174	120446-00	4.55
IC 74LS14	120458-00	1.66
IC 74LS164	120482-00	3.45
IC 14040B	122450-00	2.24
IC 6116 STATIC RAM 2Kx8 150ns	120492-00	46.00
IC 6502A	120496-00	33.28
IC 6545 1MHz	120498-00	76.18
IC 6551 1MHz	121557-00	33.12
IC 6522A	120502-00	31.29
IC Z80A SIO/2	120506-00	66.70
IC Z80A CTC	120508-00	19.32
IC Z80A CPU	120510-00	24.36
IC Z80A DMA	120512-00	65.27
IC 68B045 2 MHz	120526-00	36.23
IC SY6551A-1 2MHz	120530-00	27.60
IC SY6545A-1 2MHz	120528-00	57.62
IC910/910 PLUS GATE ARRAY (IMI)	120574-00	48.99
IC 924 GATE ARRAY A	130170-00	27.26
IC 924 GATE ARRAY B	130180-00	19.32
IC 925 GATE ARRAY (IMI)	120574-00	48.99
IC 950 GATE ARRAY A (A34)	130237-00	31.74
IC 950 GATE ARRAY B (A37)	120578-00	27.46
IC 74LS112	121385-00	2.14
IC 74S251	121386-00	2.62
IC 2K BY 8 CMOS STATIC RAM	121387-00	32.43
IC 4116 16K DRAM	121392-00	8.28
IC 9007 CRTC	121399-00	124.20
IC 9006-135 BUFFER	121400-00	37.95
IC 2681 DUAL UART	130222-00	48.30
IC 2673 ATT CONT	130223-00	55.55
IC 2672 CRT CONT	130227-00	38.64
IC 9212 BUFFER	121708-00	70.04
IC 970 G/A A (KIT)	132099-00	28.75
IC G/A 970 B	122098-00	28.75
IC G/A 970 C	122099-00	28.75
IC G/A PERSONAL TERMINAL	130182-00	31.63
IC G/A 914/925/910 (AMI)	130181-00	48.99
IC 74166 8BIT S.R.	130231-00	3.38
IC 74LS74 2XD TYPE EDG-TRIG F/F	120266-00	2.07
IC 6845R CRT CNTRL 910/914/925	123443-00	34.50
IC NS455 VIDEO CPV TMP	130264-00	124.20

RESISTORS & POTENTIOMETERS

RES CF 4.7 OHM 1/4W 5%	120381-00	.83
RES CF 68 OHM 1/4W 5%	120511-00	.83
RES CF 270 OHM 1/4W 5%	120513-00	.83
RES CF 330 OHM 1/4W 5%	120515-00	.83
RES CF 470 OHM 1/4W 5%	120517-00	.83
RES CF 510 OHM 1/4W 5%	120519-00	.83
RES CF 560 OHM 1/4W 5%	120375-00	.83
RES CF 1K OHM 1/4W 5%	120521-00	.83
RES CF 10K OHM 1/2W 5%	121768-00	.83
RES CF 1.8K OHM 1/4W 5%	120523-00	.83
RES CF 3.3K OHM 1/4W 5%	120527-00	.83
RES CF 3.9K OHM 1/4W 5%	120339-00	.83
RES CF 4.7K OHM 1/4W 5%	120531-00	.83
RES CF 5.6K OHM 1/4W 5%	130136-00	.83
RES CF 12K OHM 1/4W 5%	130137-00	.83
RES CF 180 OHM 1/4W 5%	120533-00	.83
RES CF 1M OHM 1/4W 5%	120315-00	.83
RES CF 820 OHM 1/2W 5%	121770-00	.83
RES CF 390 OHM 1/2W 5%	121861-00	.83
RES CF 750 OHM 1/4W 5%	120317-00	.83
RES CF 1.2K OHM 1/4W 5%	120319-00	.83
RES CF 100K OHM 1/4W 5%	120321-00	.83
RES CF 51K OHM 1/4W 5%	120323-00	.83
RES CF 22 OHM 1/4W 5%	120335-00	.83
RES CF 47K OHM 1/4W 5%	120337-00	.83
RES CF 150 OHM 1/4W 5%	120339-00	.83
RES CF 10K OHM 1/4W 5%	120341-00	.83
RES CF 200 OHM 1/4W 5%	120343-00	.83
RES CF 220 OHM 1/4W 5%	120403-00	.83
RES CF 33 OHM 1/4W 5%	120345-00	.83
RES CF 100 OHM 1/4W 1%	120349-00	.83
RES CF 51 OHM 1/4W 5%	120361-00	.83
RES CF 22K OHM 1/4W 5%	120363-00	.83
RES CF 27K OHM 1/4W 5%	120373-00	.83
RES CF 47 OHM 1/4W 5%	120377-00	.83
RES CF 2.7K OHM 1/4W 5%	120383-00	.83
RES CF 90 OHM 1/4W 5%	121776-00	.83
RES CF 91 OHM 1/4W 5%	120385-00	.83
RES CF 2.2K OHM 1/4W 5%	120387-00	.83
RES CF 3.9K OHM 1/4W 5%	121774-00	.83
RES CF 6.8K OHM 1.4W 5%	120391-00	.83
RES CF 30K OHM 1/4W 5%	120393-00	.83
RES CF 56K OHM 1/4W 5%	120395-00	.83
RES CF 82 OHM 1/4W 5%	121440-00	.83
RES CF 220 OHM 1/4W 5%	120403-00	.83
RES CF 680 OHM 1/4W 5%	120371-00	.83
RES CF 2K OHM 1/4W 5%	120369-00	.83
RES CF 22 OHM 1/2W 5%	130194-00	.83
RES PACK 1K OHM SIP 10%	120405-00	1.82
RES PACK 6.2K OHM SIP 10%	120407-00	1.99
RES PACK 10K OHM SIP 5%	120411-00	2.35
RES PACK 4.7K OHM SIP 10%	120413-00	1.38
RES PACK 4.7K OHM 8 PIN SIP	120429-00	.83
RES PACK 1K OHM SIP 5%	120427-00	3.45

RES PACK 2.2K OHM SIP	122300-00	3.04
RES PACK 33 OHM DIP	120417-00	3.04
RES CF 56K OHM 1/2W 5%	130165-00	.83
RES CF 510 OHM 1/2W 5%	120451-00	.83
RES CF 220 OHM 1/2W 5%	121860-00	.83
RES CF 390 OHM 1/2W 5%	121766-00	.83
RES CF 820 OHM 1/2W 5%	121862-00	.83
RES CF 1.5K OHM 1/2W 5%	121863-00	.83
RES CF 10K OHM 1/2W 5%	121864-00	.83
RES CF 2.2M OHM 1/2W 5%	121865-00	.83
RES WW 0.4 OHM 2W 10%	130195-00	.83
RES WW 0.6 OHM 2W	121771-00	.83
RES WW 0.4 OHM 2W 5%	130197-00	.83
RES WW 37.40 OHM 1/2W 1%	130192-00	.83
RES CF 3.9K OHM, 1/4W, 5%	120389-00	.83
RES CF 13K OHM, 1/4W, 5%	130193-00	.83
POT BRIGHTNESS & VERTICAL HEIGHT	121777-00	1.22
POT VERTICAL LINEARITY	121778-00	1.22
POT VIDEO B+	121779-00	1.22
POT FOCUS	121801-00	4.44
POT CONTRAST	121802-00	3.19
POT CONTRAST	121551-00	4.00
POT TRIM 100K OHM TOP-ADJ PCMT	120441-00	6.66
POT TRIM 2K OHM TOP-ADJ PCMT	120445-00	6.66

TRANSFORMERS/COILS

YOKE ASSY. PERSONAL TERMINAL	130836-00	57.50
TRANSFORMER FLYBACK KFS-00093	122013-00	63.80
TRANSFORMER FLYBACK 970/914/924	122690-00	67.72
TRANSFORMER HORIZ DR HDT19	122012-00	4.70
TRANSFORMER POWER W/CON CRT858	122011-00	148.63
TRANSFORMER POWER 970	122256-00	146.83
TRANSFORMER BALUN	121866-00	9.04
TRANSFORMER 924	130059-00	86.25
TRANSFORMER PERSONAL TERMINAL	130225-00	115.00
TRANSFORMER FLYBACK PERSONAL TERMINAL	130226-00	57.50
COIL 1.4uH 5%	122689-00	2.30
COIL 200uF 5%	122688-00	18.49
COIL INDUCTOR 27uH .3PIE	122010-00	1.38
COIL LINEARITY ADJUSTABLE	122136-00	8.28
COIL LINEARITY NON ADJUSTABLE	122009-00	6.03
COIL DEFLECTION YOKE W/CONN	122008-00	36.37
COIL WIDTH 9 MHz	130135-00	1.30
UPGRADE YOKE 970	132094-00	57.50
YOKE DEFLECTION	123551-00	34.09
YOKE DEFLECTION KYS 00060	130794-00	12.77
COIL LINEAR 52mh	130134-00	4.70
COIL WIDTH 10 UH +40%	130838-00	2.30

CRYSTALS/FUSES/BATTERIES

CRYSTAL 12.00 MHZ	130271-00	2.83
CRYSTAL 16 MHZ OSC	120428-00	31.05

CRYSTAL 23.814 MHZ (912/920)	120986-00	12.78
CRYSTAL 5.7143 MHZ	120986-01	9.03
CRYSTAL 1.8432 MHZ	120986-02	9.38
CRYSTAL 8.0000 MHZ	120986-03	5.52
CRYSTAL 13.6080 MHZ	120986-05	10.01
CRYSTAL 13.7931 MHZ	130214-00	3.59
CRYSTAL 23.814	130217-00	42.64
CRYSTAL 21.2544 MHz OSC	121389-00	23.46
CRYSTAL 13.4784 MHz	121414-00	3.73
CRYSTAL 22.2912 MHZ	122149-00	16.11
CRYSTAL 23.8140 MHZ	120352-00	42.64
CRYSTAL 3.6864 MHZ	122168-00	12.81
FUSE 4A 125V	130253-00	1.56
FUSE 3A 125V	121931-00	1.56
FUSE 1A 250V	120970-00	.83
FUSE 4A 3AG 250V SLO.BL0	130580-00	1.56
FUSE 3A 3AG 250V SLO.BLO	130581-00	1.56
POWER ADAPTER PATTERN GEN	121763-00	47.61
SPEAKER W/CONNECTOR	121528-00	8.89
THERMISTER SDT-100	121803-00	1.66
FILTER AC LINE, 3 AMP, PT	122664-00	21.32
FILTER AC LINE, 3 AMP, 910,912,950	121956-00	20.36
TRANSDUCER AUDIO KYBD 970,924,914	122151-00	6.35
BATTERY 970	120500-01	4.83
BATTERY 924	130501-00	10.35
BATTERY 970 COIN TYPE	130089-00	6.56
ANGLE ADJUST(SCREEN TILT MECHANISM)	121086-00	2.30
SHIELD FLY TRANSFRMR SCREW TYPE 925	130450-00	2.76

MECHANICAL COMPONENTS CASES

TOP CASE 910/912	121516-00	112.47
TOP CASE 920	121538-00	112.47
TOP CASE 925/950	121418-00	112.47
TOP CASE KEYBOARD 925/950	122042-00	28.75
BOTTOM CASE 910/912/920	121517-00	80.73
BOTTOM CASE 925/950	121417-00	80.73
BOTTOM CASE KEYBOARD 925/950	121991-00	40.25
BEZEL TOP CASE 925/950	121419-00	23.00
BEZEL KEYBOARD 925/950	121980-00	11.50
HOUSING ARM ASSEMBLY 970	121834-00	69.83
HOUSING CRT 970	121886-00	75.90
HOUSING MAIN ELECTRONIC 970	121885-00	81.83
HOUSING KYBD TOP W/PALM REST 970	121889-00	19.73
HOUSING KYBD BOTTOM W/PALM REST 970	121890-00	40.43
COVER BACK HOUSING CRT 970	121883-00	18.77
COVER SIDE HOUSING LOGIC BOARD 970	121884-00	45.40
BEZEL CRT 970	121888-00	17.80
HOUSING BOTTOM 914/924	130041-00	57.50
HOUSING TOP 914/924	130042-00	57.50
BEZEL FRONT 914/924	130043-00	23.00
PEDESTAL 914/924	130044-00	86.25
BEZEL PERSONAL TERMINAL	130479-00	17.25

BRACKET CRT MTG PERSONAL TERMINAL	130480-00	17.25
HOUSING TOP PERSONAL TERMINAL	130478-00	69.00
HOUSING BOTTOM PERSONAL TERMINAL	130477-00	46.00
CONNECTOR SHROUD PERSONAL TERMINAL	130484-00	11.50
KEYCAPS*		
KEYCAP DG 1X1 BLANK	120658-00	1.15
KEYCAP DG 1X1 SCULP BLANK 0	121616-01	1.15
KEYCAP DG 1X1 SCULP BLANK -7	121619-00	1.15
KEYCAP DG 1X1 SCULP BLANK +7	121618-00	1.15
KEYCAP DG 1X1 SCULP BLANK +14	121617-00	1.15
KEYCAP DG 1X1-1/2 BLANK	120724-00	1.75
KEYCAP DG 1X1-1/2 SCULP BLANK +7	121618-01	2.94
KEYCAP DG 1X2 SCULP BLANK 0	122514-00	3.45
KEYCAP DG 1X8	120774-00	2.28
KEYCAP DG 1X8 SCULP	120897-00	3.45
KEYCAP LG 1X1 BLANK	120730-00	1.15
KEYCAP LG 1X1 SCULP BLANK 0	121616-00	1.15
KEYCAP LG 1X1 SCULP BLANK -7	121619-01	1.15
KEYCAP LG 1X1 LOW PRO BLANK	120765-00	1.15
KEYCAP LG 1X1 LOW PRO SCULP BLANK	121621-01	1.15
KEYCAP LG 1X1-1/4 BLANK	120772-00	1.75
KEYCAP LG 1X1-1/4 SCULP BLANK +7	121618-02	2.81
KEYCAP LG 1X1-1/2 BLANK	120727-00	1.75
KEYCAP LG 1X1-1/2 SCULP BLANK -7	121619-02	2.94
KEYCAP LG 2X1 SCULP BLANK 0	122513-00	3.45
KEYCAP LG "L" RETURN	120771-00	2.14
KEYCAP LG "L" BLANK (RETURN)	120771-01	4.49
KEYCAP LG "L" SCULP RETURN	120894-00	3.17
KEYCAP LG "L" SCULP BLANK (RETURN)	121616-02	4.49
KEYCAP BLACK 1X1 BLANK	120537-00	1.15
KEYCAP BLACK 1X1-1/2 BLANK	120633-00	2.07
KEYCAP BLACK 1X8	120775-00	3.11
KEYCAP TAN 1X1 BLANK	120638-00	1.15
KEYCAP TAN 1X1-1/2 BLANK	120636-00	1.73
KEYCAP WHITE BLANK 1X1 1.5 DEGREE	130680-00	.83
KEYCAP GRAY BROWN BLANK 1X1 1.5 DEGREE	130680-01	.83
KEYCAP WHITE BLANK 1X1 2 DEGREE	130681-00	.83
KEYCAP WHITE BLANK 1X1 2.5 DEGREE	130682-00	.83
KEYCAP WHITE BLANK 1X1 9 DEGREE	130683-00	.83
KEYCAP GRAY BROWN BLANK 1X1 9 DEGREE	130683-01	.83
KEYCAP WHITE BLANK 1X1 10 DEGREE	130684-00	.83
KEYCAP GRAY BROWN BLANK 1X1 10 DEGREE	130684-01	.83
KEYCAP WHITE BLANK 1X2 10 DEGREE	130685-00	1.15
KEYCAP GRAY BROWN 1.25X1 2.5 DEGREE	130686-00	1.15
KEYCAP GRAY BROWN BLANK 1X1 2 DEGREE	130681-01	.83
KEYCAP GRAY BROWN BLANK 1X1 2.5 DEGREE	130682-01	.83
KEYCAP GRAY BROWN BLANK 1.25X1 9 DEGREE	130687-00	1.15
KEYCAP WHITE BLANK 2X1 10 DEGREE	130688-00	1.15
KEYCAP GRAY BROWN BLANK 2X1 2 DEGREE	130689-00	1.15
KEYCAP GRAY BROWN BLANK 1X2X2 2 DEGREE	130690-00	1.73
KEYCAP WHITE BLANK 1X9 10 DEGREE	130413-00	2.30
KEYCAP LG. BLOCK/CONV L.P. 912C	120766-00	1.15
KEYCAP LG. PRINT LP 912C	120770-00	1.15

*PART NUMBERS FOR PRINTED KEYCAPS CAN BE OBTAINED IN YOUR MAINTENANCE MANUAL OR THROUGH SPARES ORDER ENTRY, TELEVIDEO.

SWITCHES

KEYSWITCH	121994-00	4.14
KEYSWITCH - ALPHA LOCK	121995-00	7.15
SWITCH TOP ADJ 7 POS DIP	121742-00	4.42
SWITCH TOP ADJ 10 POS DIP	121810-00	4.49
SWITCH SIDE ADJ 10 POS DIP	120968-00	6.56
SWITCH PUSHBUTTON	120969-00	20.56
SWITCH POWER ON/OFF SPST	120973-00	9.07
SWITCH POWER SELECT DPDT	120974-00	7.96
SWITCH ROCKER 5A 125V 3A 250V	130808-00	8.05
SWITCH KYBRD LOCKING 910/912	121533-00	8.63
SWITCH KYBRD MMNTRY 910/912	121534-00	5.75
SWITCH KYBRD MMNTRY 914/924 FUTABA	130446-00	5.75
SWITCH KYBRD ALPHA LOCK 914/924	130447-00	8.63

SHIPPING CARTONS

CARTON SHIP W/FOAM 910/912/920	122372-00	30.00
CARTON SHIP W/FOAM 925/950	122373-00	30.00
CARTON SHIP W/FOAM 970	122497-00	30.00
CARTON SHIP W/FOAM 914/924/921/925E	130114-00	30.00
CARTON SHIP W/FOAM PERSONAL TERMINAL	130811-00	30.00

MECHANICAL/CONNECTORS/CABLES/SOCKETS

BATTERY HOLDER	121955-00	5.31
CABLE ASY KEYBOARD 912/920	120059-00	28.84
CABLE ASY KEYBOARD 910	120059-01	28.84
CABLE ASY KEYBOARD 925/950	120057-00	24.15
CABLE ASY KEYBOARD 970	122161-00	35.88
CABLE ASY MODEM RJ11	121359-00	19.94
CABLE ASSY CURRENT LOOP 925	120058-02	12.63
CONNECTOR 2 PIN RT ANGLE	120987-03	.83
CONNECTOR 2 PIN STR WAF	120988-00	.83
CONNECTOR 5 PIN STR WAF	120988-02	.83
CONNECTOR 10 PIN WIRE WRAP	121893-00	3.80
CONNECTOR 40 PIN HDR STRAIGHT	120981-07	8.63
CONNECTOR KEYBOARD PCB 26PIN	120987-01	4.84
CONNECTOR KEYBOARD RJ11 925/950	120979-00	2.55
CONNECTOR KEYBOARD RJ12 PCB 970	121412-00	4.49
CONNECTOR KEYBOARD RJ12 KYBD 970	121411-00	4.49
CONNECTOR RIGHT ANGLE RS232	120978-00	12.21
CONNECTOR RIGHT ANGLE METAL RS232	121653-00	33.40
CONNECTOR STRAIGHT RS232	121743-00	23.00
CONNECTOR BLUE MOLEX MALE	122173-01	4.14
CONNECTOR BLUE MOLEX FEMALE	122173-00	4.14
CONNECTOR RED MOLEX MALE	122172-01	4.14
CONNECTOR RED MOLEX FEMALE	122172-00	4.14
CONNECTOR WHITE MOLEX MALE	122174-01	4.14
CONNECTOR WHITE MOLEX FEMALE	122174-00	4.14
CONNECTOR 4P HDR RED (5P W/#2P OUT)	122639-00	1.00
CORD POWER 6' 3 PRONG CONN	121090-00	22.85
CORD POWER 3PIN W/PLUG & CONN	122911-00	23.00

E-RING	121979-00	.83
EQL ASY SPACE BAR DAMPER	120963-00	.83
EQL ASY SPACE BAR GUIDE STEM	120962-00	1.04
EQL ASY SPACE BAR KEY GUIDE	120912-00	2.07
EQL ASY SPACE BAR KEYGUIDE ARM	120964-00	3.14
FOOT KEYBOARD 925/950	121906-00	.83
FOOT KEYBOARD 970	122127-00	.83
FUSE HOLDER CLIP	121804-00	.83
FUSE HOLDER PANEL MOUNT	120972-00	2.30
INSULATION PAD TRANSISTOR	121808-00	.83
INSULATOR PAD CRYSTAL	120997-00	1.17
KNOB CONTRAST	121530-00	.83
KEYSTOPPERS 100ea	122238-00	13.80
PIVOTSHAFT MINIMUM 25	121978-00	5.38
PLUG JUMPER 910/910PLUS	120983-00	2.07
RETAINER BALUN	121645-00	.83
SHIELD PLATE LOGIC BOARD 970	130005-00	69.00
SHROUD CONN 910/912/920	121002-00	25.88
SHROUD CONN MODEM 910/912/920	121002-01	25.88
SHROUD CONN 925/950	121001-00	25.88
SHROUD CONN MODEM 925/950	121001-03	25.88
SPACER NYLON, PCB SNAP MTG	121644-00	1.04
SOCKET IC 14 PIN	120984-03	.90
SOCKET IC 16 PIN	120984-05	.83
SOCKET IC 18 PIN	120984-00	.95
SOCKET IC 24 PIN	120984-01	1.27
SOCKET IC 28 PIN	120984-04	1.52
SOCKET IC 40 PIN	120984-02	2.07
SOCKET IC 16 PIN LOW PROFILE	121746-01	6.40
SPRING CRT GROUNDING	122105-00	.83
THUMB WHEEL 970	122188-00	1.66
FOOT RUBBER PERSONAL TERMINAL	130208-00	.83
CONN 7P MALE MOLEX	130288-00	1.38
CONN 11P MALE MOLEX	130290-00	1.73
CONN 5P MOLEX	130820-00	1.38
CONN 3P MOLEX	130820-01	1.38

CABLE HARNESSES WITH CONNECTORS

POWER HRN ASSY 970	122185-00	22.49
VIDEO HRN ASSY 970	122191-00	6.21
POWER HRN ASSY 924	130066-00	13.80
VID & P/S ASSY	130535-00	2.82
HRN ASSY W/230-115 SWITCH 912	130493-00	1.16
P/S HRN ASSY 910/912/920	130551-00	7.73
VID HRN ASSY 910/912/920	130552-00	16.48
VID & LGC HRN ASSY 925/950	130547-00	15.18
P/S & VID HRN ASSY 925/950	130539-00	8.00
VID & CTRL BRD HRN ASSY PT	130845-00	8.83

PRICES SUBJECT TO CHANGE WITHOUT NOTICE
Spare parts has a $50.00 minimum requirement on all part orders.

950 Detachable Keycaps

Description	Stepped Keycaps Printed	Stepped Keycaps Blank	Sculptured/Matted Keycaps Printed	Sculptured/Matted Keycaps Blank	Degrees/Notes	
1X1 LIGHT GREY BLANK	---------	120730-00	---------	121616-00	0	(1)
1X1 LG NO SCROLL/SETUP	120755-00	120730-00	120887-00	121616-00	0	
1X1 LIGHT GREY F1	120731-00	120730-00	120850-00	121616-00	0	
1X1 LIGHT GREY F2	120732-00	120730-00	120851-00	121616-00	0	
1X1 LIGHT GREY F3	120733-00	120730-00	120852-00	121616-00	0	
1X1 LIGHT GREY F4	120734-00	120730-00	120853-00	121616-00	0	
1X1 LIGHT GREY F5	120735-00	120730-00	120854-00	121616-00	0	
1X1 LIGHT GREY F6	120736-00	120730-00	120855-00	121616-00	0	
1X1 LIGHT GREY F7	120737-00	120730-00	120856-00	121616-00	0	
1X1 LIGHT GREY F8	120738-00	120730-00	120857-00	121616-00	0	
1X1 LIGHT GREY F9	120739-00	120730-00	120858-00	121616-00	0	
1X1 LIGHT GREY F10	120740-00	120730-00	120859-00	121616-00	0	
1X1 LIGHT GREY F11	120741-00	120730-00	120860-00	121616-00	0	
1X1 LG CHAR INSERT	120742-00	120730-00	120861-00	121616-00	0	
1X1 LG CHAR DELETE	120743-00	120730-00	120862-00	121616-00	0	
1X1 LG LINE INSERT	120744-00	120730-00	120863-00	121616-00	0	
1X1 LG LINE DELETE	120745-00	120730-00	120864-00	121616-00	0	
1X1 DARK GREY BLANK	---------	120658-00	---------	121617-00	+14	
1X1 DG ESC/LOC ESC	120723-00	120658-00	120842-00	121617-00	+14	
1X1 DARK GREY 1/!	120659-00	120658-00	120778-00	121617-00	+14	(2)
1X1 DARK GREY 2/@	120660-00	120658-00	120779-00	121617-00	+14	
1X1 DARK GREY 3/#	120661-00	120658-00	120780-00	121617-00	+14	
1X1 DARK GREY 4/$	120662-00	120658-00	120781-00	121617-00	+14	
1X1 DARK GREY 5/%	120663-00	120658-00	120782-00	121617-00	+14	
1X1 DARK GREY 6/^	120664-00	120658-00	120783-00	121617-00	+14	
1X1 DARK GREY 7/&	120665-00	120658-00	120784-00	121617-00	+14	
1X1 DARK GREY 8/*	120666-00	120658-00	120785-00	121617-00	+14	
1X1 DARK GREY 9/(	120667-00	120658-00	120786-00	121617-00	+14	
1X1 DARK GREY 0/)	120668-00	120658-00	120787-00	121617-00	+14	
1X1 DARK GREY -/_	120669-00	120658-00	120788-00	121617-00	+14	
1X1 DARK GREY =/+	120670-00	120658-00	120789-00	121617-00	+14	
1X1 DARK GREY `/~	120671-00	120658-00	120790-00	121617-00	+14	
1X1 DARK GREY \/|	120672-00	120658-00	120791-00	121617-00	+14	
1X1 DG BACK SPACE	120673-00	120658-00	120792-00	121617-00	+14	
1X1-1/2 DARK GREY TAB	120726-00	120724-00	120845-00	121618-01	+7	
1X1 DARK GREY Q	120687-00	120658-00	120806-00	121618-00	+7	
1X1 DARK GREY W	120688-00	120658-00	120807-00	121618-00	+7	

950 Detachable Keycaps
Continued

Description	Stepped Keycaps Printed	Stepped Keycaps Blank	Sculptured/Matted Keycaps Printed	Sculptured/Matted Keycaps Blank	Degrees/Notes
1X1 DARK GREY E	120689-00	120658-00	120808-00	121618-00	+7
1X1 DARK GREY R	120690-00	120658-00	120809-00	121618-00	+7
1X1 DARK GREY T	120691-00	120658-00	120810-00	121618-00	+7
1X1 DARK GREY Y	120692-00	120658-00	120811-00	121618-00	+7
1X1 DARK GREY U	120693-00	120658-00	120812-00	121618-00	+7
1X1 DARK GREY I	120694-00	120658-00	120813-00	121618-00	+7
1X1 DARK GREY O	120695-00	120658-00	120814-00	121618-00	+7
1X1 DARK GREY P	120696-00	120658-00	120815-00	121618-00	+7
1X1 DARK GREY [/]	120697-00	120658-00	120816-00	121618-00	+7
1X1-1/2 DG LINE FEED	120725-00	120724-00	120844-00	121618-01	+7
1X1-1/4 LG CLEAR SPACE	120773-00	120772-00	120896-00	121618-02	+7
1X1 LIGHT GREY CTRL	120750-00	120730-00	120869-00	121618-00	0
1X1 DARK GREY ALPHA LOCK	120699-00	120658-00	120818-00	121616-01	0
1X1 DARK GREY A	120700-00	120658-00	120819-00	121616-01	0
1X1 DARK GREY S	120701-00	120658-00	120820-00	121616-01	0
1X1 DARK GREY D	120702-00	120658-00	120821-00	121616-01	0
1X1 DARK GREY F	120703-00	120658-00	120822-00	121616-01	0
1X1 DARK GREY G	120704-00	120658-00	120823-00	121616-01	0
1X1 DARK GREY H	120705-00	120658-00	120824-00	121616-01	0
1X1 DARK GREY J	120706-00	120658-00	120825-00	121616-01	0
1X1 DARK GREY K	120707-00	120658-00	120826-00	121616-01	0
1X1 DARK GREY L	120708-00	120658-00	120827-00	121616-01	0
1X1 DARK GREY ;/:	120709-00	120658-00	120828-00	121616-01	0
1X1 DARK GREY '/"	120710-00	120658-00	120829-00	121616-01	0
LIGHT GREY "L" RETURN	120771-00	120771-01	120894-00	121616-02	0
1X1 LIGHT GREY BREAK	120751-00	120730-00	120870-00	121616-00	0
1X1 DARK GREY BACK TAB	120698-00	120658-00	120817-00	121619-00	-7
1X1-1/2 LG SHIFT	120728-00	120727-00	120847-00	121619-02	-7
1X1 DARK GREY Z	120711-00	120658-00	120830-00	121619-00	-7
1X1 DARK GREY X	120712-00	120658-00	120831-00	121619-00	-7
1X1 DARK GREY C	120713-00	120658-00	120832-00	121619-00	-7
1X1 DARK GREY V	120714-00	120658-00	120833-00	121619-00	-7
1X1 DARK GREY B	120715-00	120658-00	120834-00	121619-00	-7
1X1 DARK GREY N	120716-00	120658-00	120835-00	121619-00	-7
1X1 DARK GREY M	120717-00	120658-00	120836-00	121619-00	-7
1X1 DARK GREY ,/<	120718-00	120658-00	120837-00	121619-00	-7
1X1 DARK GREY ./>	120719-00	120658-00	120838-00	121619-00	-7

950 Detachable Keycaps
Continued

Description	Stepped Keycaps Printed	Stepped Keycaps Blank	Sculptured/Matted Keycaps Printed	Sculptured/Matted Keycaps Blank	Degrees/Notes
1X1 DARK GREY //?	120720-00	120658-00	120839-00	121619-00	-7
1X1 DARK GREY {/}	120721-00	120658-00	120840-00	121619-00	-7
1X1 LIGHT GREY DEL	120752-00	120730-00	120871-00	121619-01	-7
1X1 LG PRINT (LP)	120770-00	120765-00	120893-00	121621-01	0 (3)
1X1 LG FUNCT (LP)	120767-00	120765-00	120890-00	121621-01	0 (3)
1X8 DARK GREY SPACE BAR	120774-00	---------	120897-00	---------	0
1X1 LG HOME (LP)	120768-00	120765-00	120891-00	121621-01	0 (3)
1X1 LG CURSOR (LP)	120769-00	120765-00	121405-00	121621-01	0 (3) (4)
1X1 LG LINE ERASE	120746-00	120730-00	120865-00	121616-00	0
1X1 LG PAGE ERASE	120747-00	120730-00	120866-00	121616-00	0
1X1 LIGHT GREY SEND	120753-00	120730-00	120885-00	121616-00	0
1X1 DARK GREY 7	120680-00	120658-00	120799-00	121616-01	0
1X1 DARK GREY 8	120681-00	120658-00	120800-00	121616-01	0
1X1 DARK GREY 9	120682-00	120658-00	120801-00	121616-01	0
1X1 DARK GREY 4	120677-00	120658-00	120796-00	121616-01	0
1X1 DARK GREY 5	120678-00	120658-00	120797-00	121616-01	0
1X1 DARK GREY 6	120679-00	120658-00	120798-00	121616-01	0
1X1 DARK GREY 1	120674-00	120658-00	120793-00	121616-01	0
1X1 DARK GREY 2	120675-00	120658-00	120794-00	121616-01	0
1X1 DARK GREY 3	120676-00	120658-00	120795-00	121616-01	0
1X1 DARK GREY ,	120685-00	120658-00	120804-00	121616-01	0
1X1 DARK GREY 0	120683-00	120658-00	120802-00	121616-01	0
1X1 DARK GREY .	120686-00	120658-00	120805-00	121616-01	0
1X1-1/2 LG ENTER	120729-00	120727-00	120848-00	121621-03	0
1X1 DARK GREY -	120684-00	120658-00	120803-00	121616-01	0

NOTES:

(1) DEGREES REFER TO SCULPTURED/MATTED KEYCAPS ONLY

(2) SLASH BETWEEN TWO CHARACTERS (FOR EXAMPLE: 1/!) IS FOR CLARITY AND IS NOT PRINTED ON THE KEYCAP

(3) LOW PROFILE KEYCAPS

(4) SAME KEYCAP CAN BE USED FOR ALL FOUR CURSOR POSITIONS

TeleVideo® Model 950 CRT Terminal Installation and User's Guide

TeleVideo Systems, Inc.

TeleVideo® Model 950 CRT Terminal Installation and User's Guide

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REVISION B
APRIL 1982

This manual is written for the latest Model 950 firmware. Earlier firmware (i.e., 1.0) functions may not correspond to this manual.

Disclaimer

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TELEVIDEO SYSTEMS, INC., 1170 Morse Avenue, Sunnyvale, California 94086 408/745-7760

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

This manual explains how to install, operate, program, and troubleshoot the Model 950 terminal. The manual has been designed to help you use the terminal easily regardless of your previous experience with terminals.

1.1 TERMINAL OVERVIEW

The Model 950 is a compact state-of-the-art "smart" terminal that provides high level performance at low cost. Compatible with most computer systems, the Model 950 fits a wide variety of applications in the end-user environment.

The following features are standard:

Monitor mode
Protected fields
Addressable/readable cursor
Line and character insert/delete
Local and duplex edit
Upper and lower case characters
Tabbing
X-On/X-Off and Data Terminal Ready control
Split screen with line lock
Programmable function keys (11 keys with 22 functions)
15 special graphics characters
On-screen status (25th) line
Programmable user line
Buffered auxiliary printer port
Dedicated editing keys
Smooth scrolling
Etched CRT face to reduce glare
14 x 10 character resolution
20 mA current loop communications
Detached keyboard
Typewriter-styled keyboard with numeric keypad
Self testing

1.1.1 Options

The terminal may be ordered with several options that enhance its already-comprehensive list of features. These options, available at additional cost, are:

- An additional 24 lines of memory, allowing total memory to be divided into either one 48-line page or two 24-line pages.
- An additional 48 lines of memory which can be added provided the optional 24 lines of memory (described above) have been installed. The total memory can be divided into one 96-line page, two 48-line pages, or four 24-line pages.
- An integral modem/dialer

1.2 HOW TO USE THIS MANUAL

1.2.1 Contents

The manual contains the following chapters:

2. **INSTALLATION**

   How to install the terminal and make field modifications.

3. **OPERATION**

   How to set up the terminal and use the basic operator controls.

4. **PROGRAMMING**

   Describes the controls which enable you to include the terminal features in application programs.

5. **TROUBLESHOOTING AND SERVICE**

   What to do if you have a problem with the terminal.

APPENDICES

Specifications, limited warranty, and ASCII code chart.

INDEX

OPERATOR'S QUICK REFERENCE GUIDE

Listing of all control and escape commands.

SWITCH SETTING SUMMARY

1.2.2 Symbols

Throughout the manual, special symbols are used to call your attention to information of special importance. The symbols used are as follows:

Information for every operator.

Warning concerning the safety of the operator or possible loss of data. *When you see this note, STOP and read the note before proceeding!*

1.2.3 Commands

Escape Sequences—Escape sequences are shown here with a space before alphanumeric character(s). For example, the sequence shown as

ESC c

involves pressing only the ESCAPE key and a lower case character "c." This space is *not* to be entered as part of the sequence; it is included only for the sake of clarity.

The ESCAPE key is used in conjunction with one alphanumeric character and is always pressed and released before the second key is pressed.

Control Commands—The symbol used in this manual to represent the CONTROL (CTRL) key is ^.

The CONTROL (CTRL) key is always used simutaneously with the other character in the command; i.e., the CTRL key is pressed first and held down while the other key is pressed. (It is similar in action to the SHIFT key.)

Entering Commands—In order for commands to work as expected, the command must be entered exactly as shown. Notice whether the command requires upper or lower case, a number one or a lower case "L," a zero or an upper case "oh."

1.2.4 Terminology—The optional lines of memory allow you to create pages which are longer than the 24-line screen display. In the following chapters, the following terms will be used:

Page	An amount of memory, defined by the memory chips installed. May be 24, 48, or 96 lines. The memory which constitutes one page may not all be visible at one time, since the screen displays only 24 lines at a time.
Screen or display	The 24-line terminal viewing area.

2. INSTALLATION

This manual is written for the latest Model 950 firmware. Earlier firmware (i.e., 1.0) functions may not correspond to this manual.

2.1 UNPACKING

To unpack the terminal, turn the opened packing carton on its side and slide the terminal out. It is not important to keep the terminal upright.

After you unpack the terminal, inspect it thoroughly for hidden damage and loose components or fittings, using the following checklist:

1. Remove the terminal cover by removing the four Phillips screws underneath the terminal—two in the front and two in the back. Lift up the cover carefully. (Figure 2-1 shows the location of the screws.)

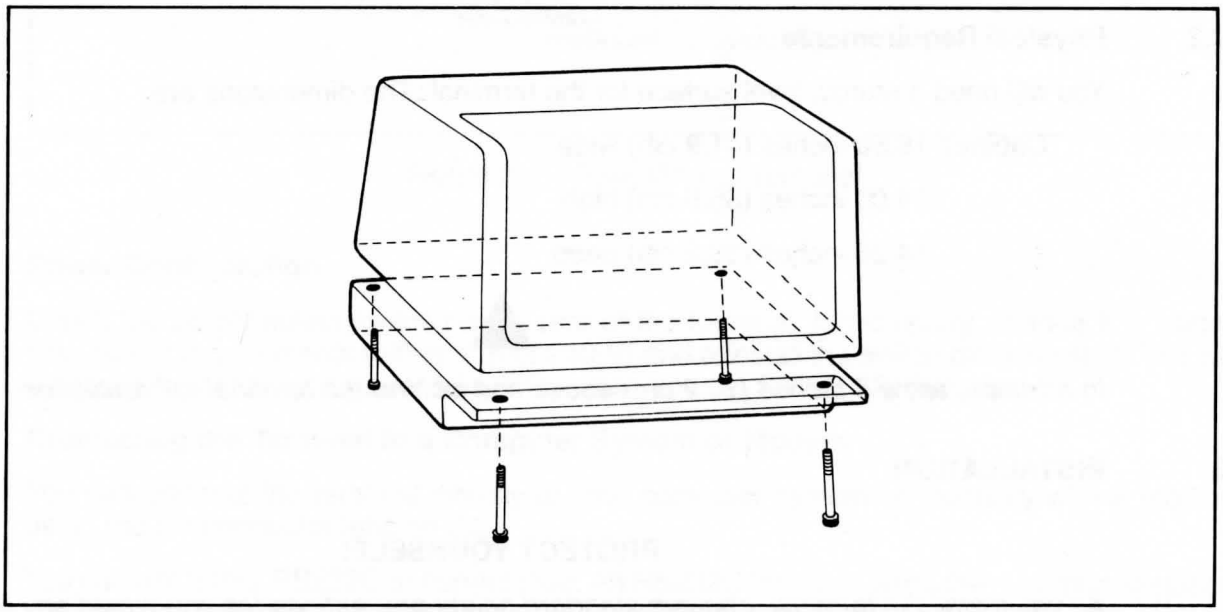


Figure 2-1 Location of Screws in Cabinet

2. Inspect the keyboard and display cabinet interior for shipping damage.

If the CRT tube is broken, always wear heavy rubber gloves or use tongs to pick up the broken CRT fragments since the coating on the inside of the tube is poisonous.

EVEN AFTER THE POWER IS TURNED OFF, CHARGES ARE RETAINED BY THE CRT AND CAPACITORS. ALWAYS DISCHARGE THEM TO GROUND BEFORE TOUCHING THEM. NEVER REACH INTO THE TERMINAL ENCLOSURE UNLESS SOMEONE CAPABLE OF GIVING AID IS PRESENT.

3. Examine cable harnesses for stress, loose or broken wires, or broken cable ties.
4. Examine all internally-mounted components for loose or missing hardware.

5. Tighten any loose hardware.
6. Clean any loose debris from the cabinet interior.
7. Replace the cover. Do not overtighten the screws.

2.2 PREPARING THE SITE

Make sure you are ready with the proper power and a sufficiently-large table.

2.2.1 Power Requirements

115 VAC 60 Hertz at 0.5 amp

OR

230 VAC 50 Hertz at 0.25 amp

NEMA standard 5-15R, 3-prong receptacle (US only)

2.2.2 Physical Requirements

You will need a sturdy, level surface for the terminal. The dimensions are:

Cabinet 16.50 inches (41.9 cm) wide
14.00 inches (35.6 cm) high
14.25 inches (36.2 cm) deep

In addition, allow 4 inches (10.2 cm) above and behind the terminal for ventilation.

2.3 INSTALLATION

PROTECT YOURSELF!

As you install the terminal, observe standard safety precautions (as you would any electrical or electronic equipment).

The actual installation consists of only five steps:

1. Connect the keyboard to the terminal (2.3.1).
2. Configure the terminal for either 115 or 230 VAC operation (2.3.2).
3. Connect the terminal to the computer or a modem (and to a printer, if used) (2.3.3 and 2.3.4)
4. Configure the terminal by setting exterior switches (2.3.5).
5. Plug the terminal into the wall outlet (2.3.6).

2.3.1 Connecting the Keyboard

Connect the end of the keyboard cable to the connector labeled *P6* on the rear of the terminal (Fig. 2-2).

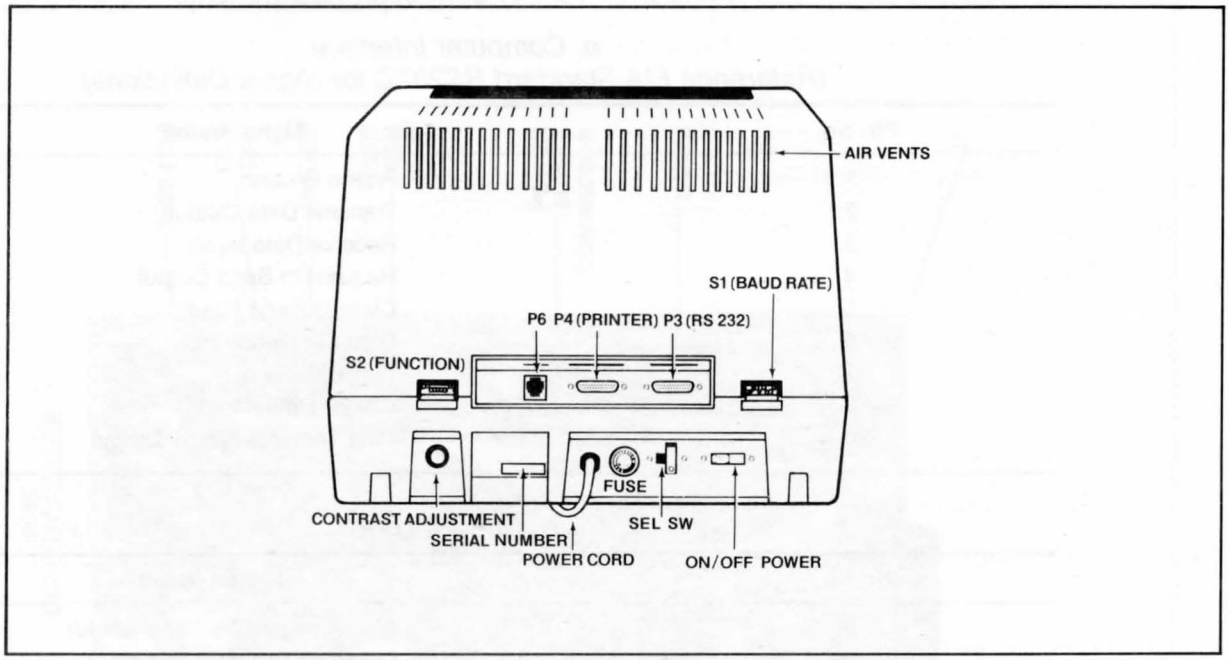


Figure 2-2 Rear View of Terminal

2.3.2 Power Configuration

Check the power select switch on the rear of the terminal. If necessary, change it to match your power requirements (either 115 or 230 V) and reinstall the switch blocking strip. You will set Hertz to match your power frequency when you set Switch S2, dipswitch 9.

2.3.3 Connecting the Terminal to a Computer System or Modem

You can connect the terminal directly to your computer system or indirectly with a modem using the pin connector labeled P3.

You can use either RS232C or current loop. An RS232C interface limits the maximum distance between the terminal and computer or modem to 50 feet (if shielded, twisted-pair cable is used). A current loop interface allows the terminal to be located up to 1,000 feet from the computer.

For an RS232C installation, use a shielded, twisted-pair cable with a connector which has been configured to match the pin connector assignments listed in Table 2-1a.

Table 2-1b lists the pin assignments of the P3 connector for current loop. For a current loop installation, configure the cable connector as described in Table 2-2. The current loop configuration can be any *one* of the following:

1. Full duplex, active transmit, active receive
2. Full duplex, active transmit, passive receive
3. Full duplex, passive transmit, active receive
4. Full duplex, passive transmit, passive receive
5. Half duplex, either active or passive transmit/receive

Table 2-1 P3 Pin Connector Assignments

a. Computer Interface
(Reference EIA Standard RS232C for Signal Definitions)

Pin No.	Signal Name
1	Frame Ground
2	Transmit Data Output
3	Receive Data Input
4	Request to Send Output
5	Clear to Send Input
6	Data Set Ready Input
7	Signal Ground
8	Carrier Detect Input
20	Data Terminal Ready Output

b. Current Loop

Pin No.	Signal Name
9	20 mA source (+12V, no load)
10	Detected current loop data
12	Current Loop +, Receive
13	Current Loop −, Transmit
14	20 mA source (+12V, no load)
24	Current Loop −, Receive
25	Current Loop +, Transmit

Table 2-2 Configuration of Computer Interface Connector for Current Loop

Transmission	Current Source*	Cable Connector Jumpers	Pin Connection
1. Full duplex transmit	Active	9 to 25	7 −
			13 +
	Passive	—	13 −
			25 +
2. Full duplex receive	Active	14 to 12	7 −
		3 to 10	24 +
	Passive	3 to 10	12 +
			24 −
3. Half duplex	Active	3 to 10	7 −
		9 to 25	24 +
		12 to 13	
	Passive	3 to 10	24 −
		12 to 13	25 +

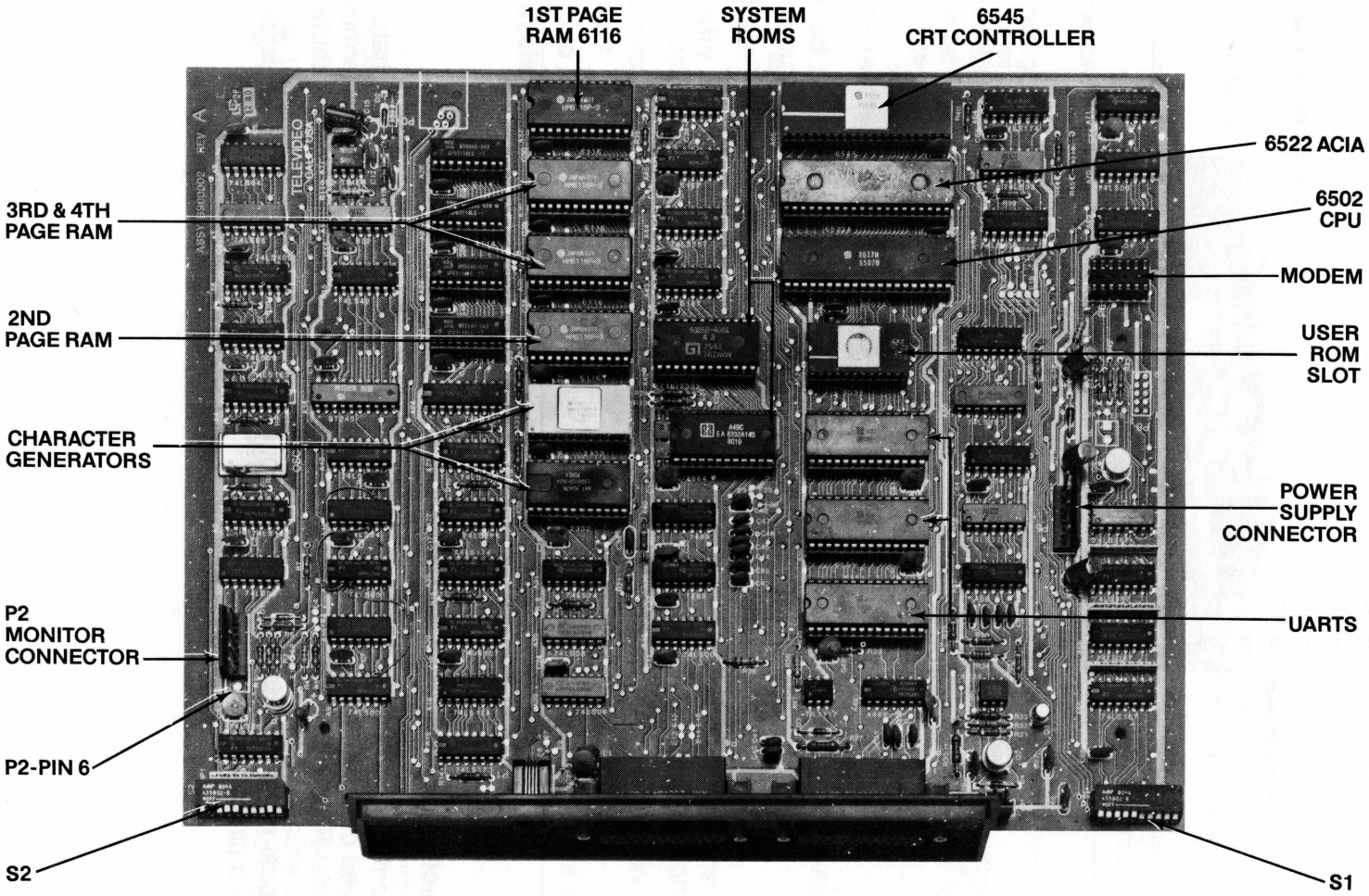


Figure 2-3 Logic Board

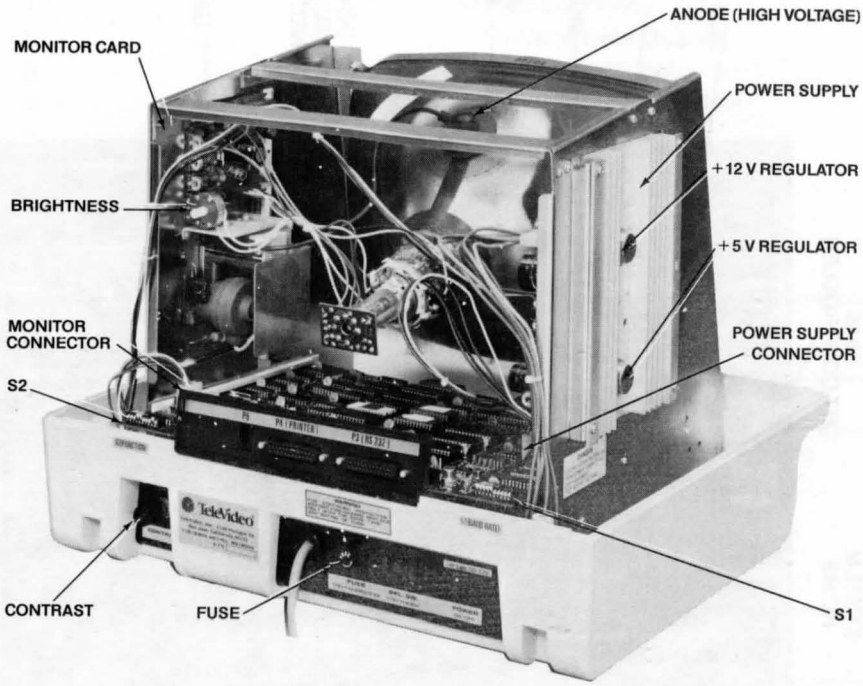


Figure 2-4 Terminal Interior

2.3.4 Connecting the Terminal to a Printer

Your terminal can be connected to an auxiliary serial printer to make a hard copy of data displayed on the screen. The terminal's serial printer interface allows the terminal to be used with most RS232-compatible serial printers currently available on the market.

The serial printer interface is a 25-pin connector labeled *P4*. Table 2-3 defines the printer interface pin connections.

Table 2-3 P4 (Serial Printer Interface) Pin Connector Assignments (Reference EIA Standard RS232C for Signal Definitions)

Pin No.	Signal Name
1	Protect Ground
2	Receive Data (input)
3	Transmit Data (output)
4	Request to Send (input)
5	Clear to Send (output)
6	Data Set Ready (output)
7	Signal Ground
8	Data Carrier Detect (output)
20	Data Terminal Ready (input)

2.3.5 Configuring the Terminal for the Computer and Printer

Two switches (located on the rear of the terminal as shown in Fig. 2-2) allow you to configure the terminal to operate according to the requirements of your computer system and printer and change the operation of the terminal.

The switchable features are:

Baud Rates—You can select any of 15 baud rates according to the requirements of your computer system and printer.

Hertz—You can set the Hertz switch to match your powerline frequency.

Parity, Stop Bits, and Word Structure—You can set the parity, number of stop bits, and number of bits in the word structure to match the requirements of your computer system.

Communications—You can select half or full duplex (conversational mode), local, or block mode.

Video Display—You can cause the display to be green on black or black on green.

Keyclick—You can select keyclick or silent key action.

▲

These parameters can also be changed by codes entered from the keyboard or sent from the computer.

Switch Settings—Two external switches (S1 and S2) on the rear of the terminal can be set to control many of the possible parameters described above. The possible switch settings are listed in Tables 2-4a through 2-4d. Figure 2-5 shows a typical switch setting.

Table 2-4 External Switch Settings

a. S1 and S2

Switch	Dipswitch	Position: Open (Up)	Position: Closed (Down)	Function
S1	1,2,3,4			Computer baud rate; see Table 2-4b
	5	x		Seven-bit word structure
			x	Eight-bit word structure
	6	x		Two stop bits
			x	One stop bit
	7,8,9,10			Printer baud rate; see Table 2-4b
S2	1	x		Duplex edit
			x	Local edit
	2	x		Blinking cursor
			x	Steady cursor
	3,4,5			Parity; see Table 2-4c
	6	x		Green on black display
			x	Black on green display
	7,8			Communication mode; see Table 2-4d
	9	x		60 Hertz[1]
			x	50 Hertz[1]
	10	x		Keyclick off
			x	Keyclick on

Note

1. Set to match powerline frequency to avoid screen flicker.

Table 2-4b Switch S1 Settings for Baud Rates

Terminal / Printer	Dipswitches 1 / 7	2 / 8	3 / 9	4 / 10	Baud Rates
	D	D	D	D	9600
	U	D	D	D	50
	D	U	D	D	75
	U	U	D	D	110
	D	D	U	D	135
	U	D	U	D	150
	D	U	U	D	300
	U	U	U	D	600
	D	D	D	U	1200
	U	D	D	U	1800
	D	U	D	U	2400
	U	U	D	U	3600
	D	D	U	U	4800
	U	D	U	U	7200
	D	U	U	U	9600
	U	U	U	U	19200

Legend
D = Down/closed/0
U = Up/open/1

Table 2-4c Switch S2 Settings for Parity

Dipswitch 3	4	5	Parity Setting
X	X	D	No parity
D	D	U	Odd parity (receive/transmit)
D	U	U	Even parity (receive/transmit)
U	D	U	Mark (transmit parity disabled)
U	U	U	Space (transmit parity disabled)

Legend
X = Either up or down
D = Down/closed/0
U = Up/open/1

▲

If word structure, parity, or stop bits are set incorrectly, the terminal will only display "@" signs when data is received (if any data is received).

Table 2-4d Switch S2 Settings for Communication Mode

Dipswitch 7	8	Communication
D	D	Half duplex
D	U	Full duplex
U	D	Block
U	U	Local

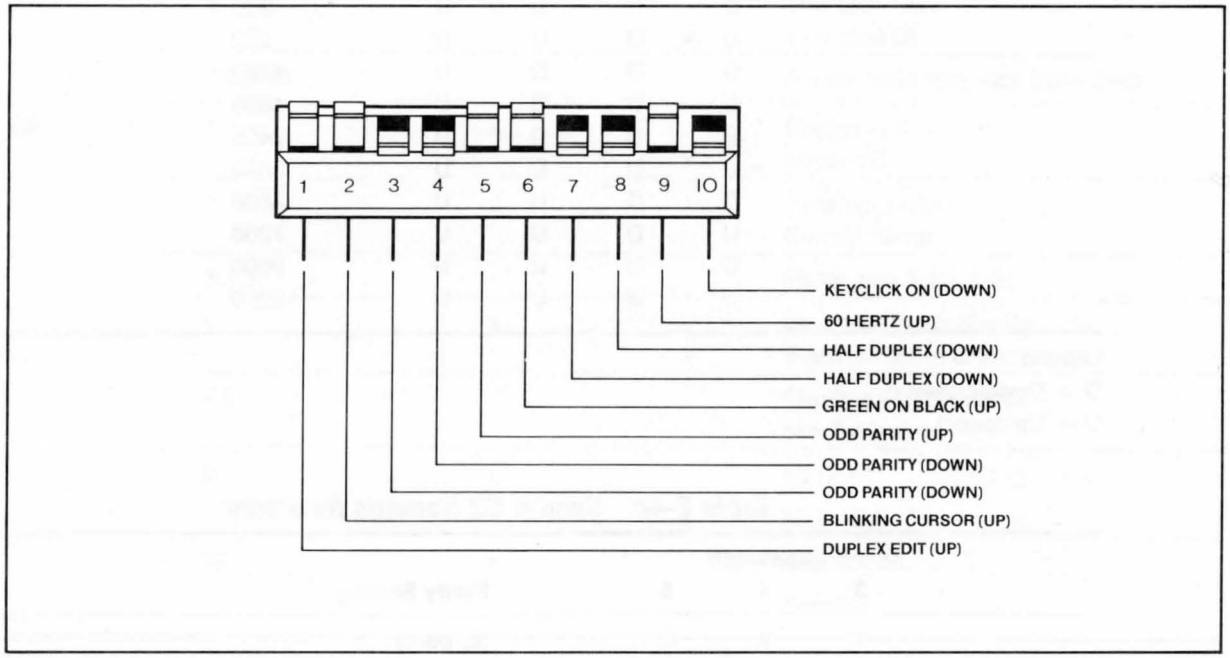


Figure 2-5 A Typical S2 Switch Setting

▲

Whenever you change any switches, turn the terminal power off and back on. This allows the software to scan all new switch positions.

Set the dipswitches prior to turning on power to the terminal and record the switch settings on the form in 5.4.1.

2.3.6 Plugging the Terminal In

After all cables have been connected and switches set, plug the terminal into the wall outlet.

2.4 INSTALLATION CHECKLIST

Before you turn on the terminal, answer the following questions:

1. Does your power plug match the wall socket?
2. Did you set the power selector switch to match your power requirements?
3. Is the interface cable to the computer system properly wired and attached to both the terminal and the computer?
4. If you are using a printer, did you plug in the printer interface connector?
5. Did you set the switches for the correct

   Baud rate (both for terminal and printer)?
   Stop bits?
   Word structure?
   Parity?
6. Did you set switches for the desired communication mode?
7. Did you plug the terminal into the wall outlet?
8. Did you plug the keyboard into the terminal?

2.5 FIELD MODIFICATIONS

2.5.1 Composite Video Option

If you wish to drive a monitor in addition to or other than the terminal monitor, modify the logic board (Fig. 2-3). Add an Amphenol BNC connector (Part 227169-5) to the rear of the terminal case. (See Fig. 2-4 for recommended placement of the connector.)

Connect the center lead of the BNC connector to P2 pin 6 and the BNC ground lead to P2 pin 3. Cut the trace between E1 and E2. Install a jumper between E3 and E4.

▲

The monitor should not be more than 10 feet from the terminal.

2.5.2 Additional Pages of Screen Memory

The terminal can be modified to provide additional pages of screen memory. If you ordered the terminal with this additional memory, this modification will have been made at the factory before the terminal was shipped. You can perform this modification in the field later by following these directions.

To add 24 lines (one page) of screen memory to the terminal, you will need to add one chip. This will provide a total of 48 lines of memory. You can increase this total to 96 lines by adding two more chips to the second chip. (You can not add only two chips; you must add a total of either one or three chips.)

You will need 2 K by 8 bit static RAM chips with a maximum rise time of 150 nanoseconds. (These may be purchased from your dealer or distributor.) Approved manufacturers include the following:

Brand	Part No.
Hitachi	HN 6116-150nt
Toshiba	TMM 2016-150ns
Mostek	MK 4802N-150ns

To install the chip(s), follow these steps:

1. Remove the terminal cover by removing the four Phillips screws underneath the terminal—two in the front and two in the back. Lift up the cover carefully. (Figure 2-1 shows the location of the screws.)

Even after the power is turned off, charges are retained by the CRT and capacitors. Always discharge them to ground before touching them. Never reach into the terminal enclosure unless someone capable of giving aid is present.

2. Add chip(s) to the logic board as described in Table 2-5.

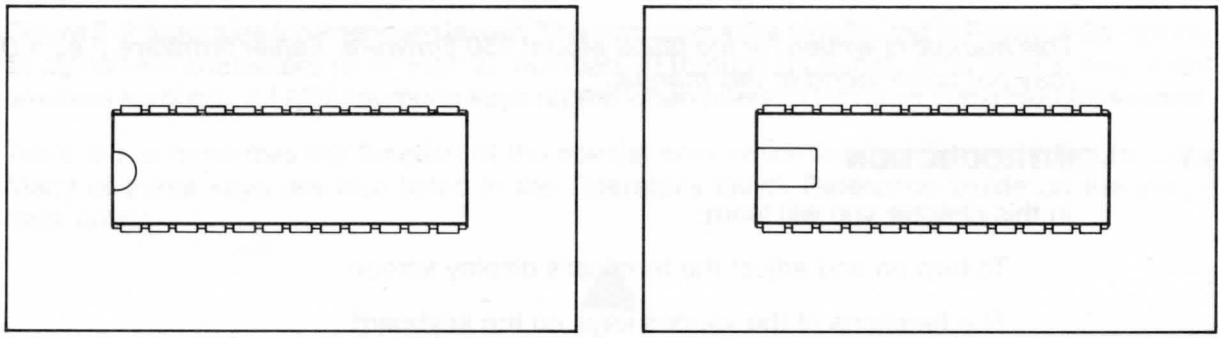
Install the chips carefully to avoid bending the pins. Each chip has a half-moon notch on the side or a depression on the top. This notch or depression must be oriented to match the orientation of the other chips on the logic board (Fig. 2-6).

3. Replace the cover, being careful not to overtighten the screws.

Table 2-5 Adding Screen Memory Chips to the Logic Board

Lines of Memory Being Added	No. of Chips Added	Location on Logic Board of New Chips
24	One	Position A34
48*	Two	Positions A35 and A36

Note
*You must add a chip into Position A34 before you add chips into Positions A35 and A36.



a. Notch in Chip

b. Depression in Chip

Figure 2-6 Notches and Depressions in Chips

3. OPERATION

This manual is written for the latest Model 950 firmware. Earlier firmware (i.e., 1.0) functions may not correspond to this manual.

3.1 INTRODUCTION

In this chapter you will learn:

To turn on and adjust the terminal's display screen

The functions of the various keys on the keyboard

To direct data to the computer system and the printer through send commands

To change the default set-up values

To communicate with your computer system

3.2 TURNING ON THE TERMINAL

1. Make sure the AC power plug is plugged into a grounded outlet.
2. Locate the ON/OFF rocker switch on the rear of the terminal (Figure 3-1). Push the end of the switch which is marked with a white dot.
3. Listen for a beep within one second (indicating that power is on and the terminal has scanned the switch settings).
4. Watch for the cursor to appear in the upper lefthand corner of the screen within 10 to 15 seconds.
5. Adjust the contrast control on the rear of the terminal for the desired screen intensity.
6. Adjust the tilt of the screen by unscrewing the knob which is between the two front legs of the terminal.
7. Refer to Chapter 5 if the installation does not proceed as indicated.

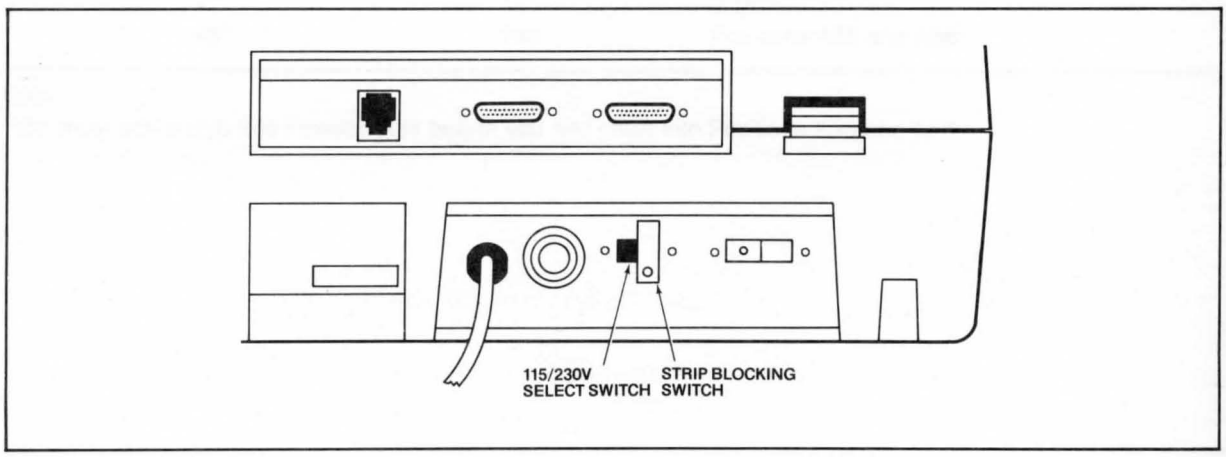


Figure 3-1 Rear Panel

3. OPERATION

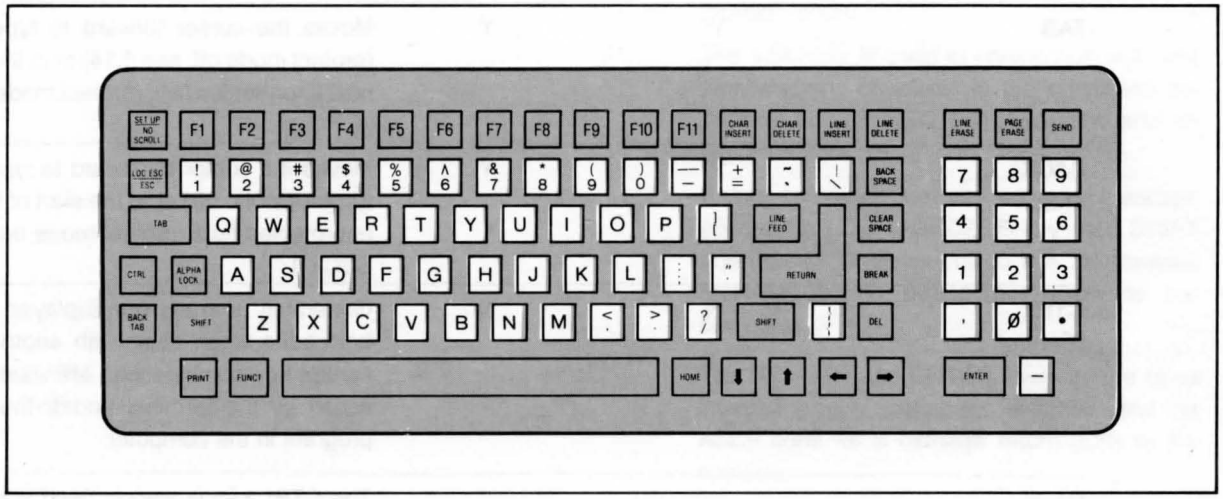
3.3 KEYBOARD CONTROLS

Figure 3-2 illustrates the keyboard layout. The character keys highlighted in Figure 3-2a include all alphabetic characters (a through z), numbers (0 through 9), punctuation marks, and mathematical symbols. All alphanumeric keys repeat when pressed for more than one-half second.

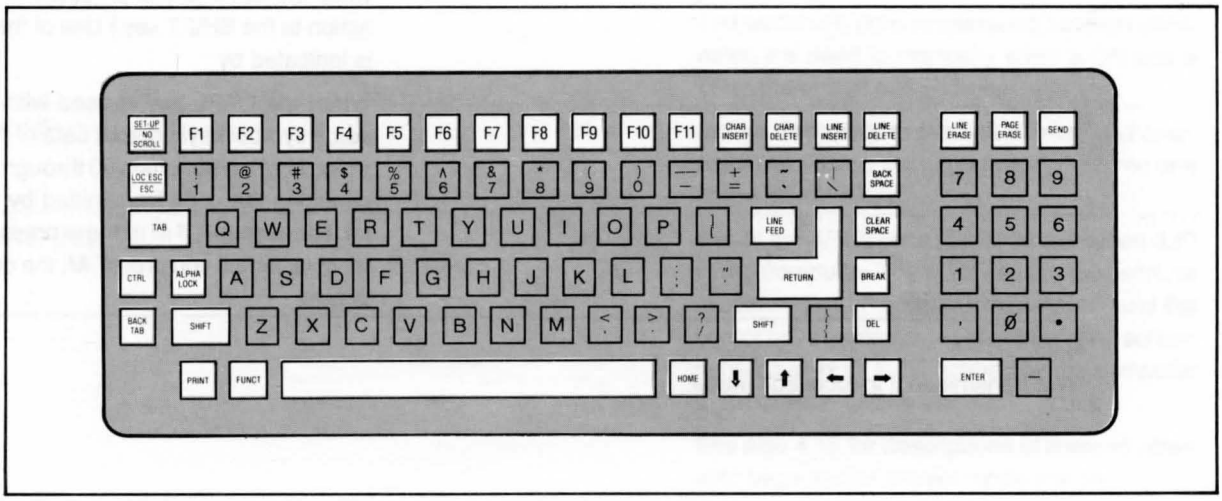
Table 3-1 summarizes the function of the special keys which are highlighted in Figure 3-2b. Many of these keys are also listed in the Operator's Quick Reference Guide on the inside back cover.

▲

Protect mode, which is frequently referred to in Table 3-1, is explained fully in 4.14.



a. Character Keys



b. Special Keys

Figure 3-2 Keyboard Layout

Table 3-1 Function of Keys

Key Name	Transmitted? (Y/N)*	Repeat Action? (Y/N)	Description
Space Bar	Y*	Y	Causes a blank space to appear on the display and transmits an ASCII space code (20 Hex).
SHIFT	N	N	Selects upper character inscribed on a key, changes operation of most special keys, and capitalizes alpha characters.
ALPHA LOCK	N	N	Locks the SHIFT keys so that all alpha keys transmit codes for upper-case characters. The key is pressed to lock and pressed again to release.
TAB	Y*	Y	Moves the cursor forward to typewriter tabs (protect mode off; see 4.14) or to the start of the next unprotected field (protect mode on). (Same as ^I.)
BACK TAB	Y*	Y	Moves the cursor backward to typewriter tabs (protect mode off) or to the start of the previous unprotected field (protect mode on). (Same as ESC I.)
CTRL (Control)	N	N	Generates normally-nondisplayed ASCII control codes when used with another key. The control key combinations are used for special action by the terminal and/or the application program in the computer.
CTRL			The CTRL key is always used *simultaneously* with the other character in the command; i.e., the CTRL key is pressed first and held down while the other key is pressed. (It is similar in action to the SHIFT key.) Use of the control key is indicated by ^. When the CTRL key is used with an alpha or some symbol keys, output data of the character which is typed becomes 00 through IF Hex, thus changing the code transmitted by that character. For example, if *M* alone is pressed, the code for M is sent. If you press ^*M*, the code for a CR is sent.

Note
*Not transmitted if in local edit mode.

Table 3-1 continued

Key Name	Transmitted? (Y/N)*	Repeat Action? (Y/N)	Description
ESC (Escape)	Y*	N	The ESC key sends an ASCII code for escape to the display processor. The key is generally used to momentarily leave (escape) an application program in order to use a special feature or function. Another function of the ESC key is to cause the next control character entered to be displayed on the screen. This facilitates putting control characters on the screen without going into monitor mode. The ESC key is used in conjunction with one alphanumeric character in the command sequence; i.e., *the ESC key is pressed and released before the second key is pressed.* If your computer does not echo back escape codes, the LOCAL ESCAPE key (i.e., SHIFT and ESCAPE) allows you to use the terminal features without transmitting them to the computer.
RETURN/ ENTER	Y*	N	The RETURN and ENTER keys can be used interchangeably. (Same as ^M.)They send the ASCII code for a carriage return (CR) to the computer. If the entire current line is protected, the code moves the cursor to the next unprotected position on the page. The terminal's auto wraparound function eliminates the need to manually enter a CR and a LF at the end of each 80-character line.
HOME	Y*	N	Moves the cursor to the first unprotected character position on the page (usually column one of row one). (Same as ^^.)
LINEFEED	Y*	Y	Sends the ASCII code (OAH) for a linefeed (LF) to the computer. The code causes the terminal to transmit an LF code to the computer and the cursor to be moved down one line on the screen in half duplex or to be echoed by the computer in full duplex. (Same as ^J.) See also 4.15 for descriptions of linefeed when auto page and/or protect mode are on.

Note
*Not transmitted if in local edit mode.

Table 3-1 continued

Key Name	Transmitted? (Y/N)*	Repeat Action? (Y/N)	Description
BACKSPACE ←	Y*	Y	Moves the cursor one character to the left. (Same as ^H.)
↑	Y*	Y	Moves the cursor up one line. (Same as ^K.)
↓	Y*	Y	Moves the cursor down one line. If the cursor is on the bottom line of the screen, the display will roll up one line. If additional memory has been installed, a page may be longer than the visual screen. In that case, if the cursor is on the bottom line of the page, the code has no effect (except in block mode). (Same as ^V.)
→	Y*	Y	Moves the cursor one character to the right. (Same as ^L.)
DEL (Delete)	Y*	Y	The DEL key sends an ASCII DEL character to the computer. The computer echoes the code back to the terminal to be performed. This is usually interpreted by the computer as a character erase code.
CLEAR SPACE	Y*	Y	Replaces all unprotected characters on the page with spaces. Shifted CLEAR SPACE (same as ESC *) clears the entire page to nulls and turns off protect and half intensity modes.
BREAK	Y*	N	Transmits a 250-millisecond break pulse to the computer.
PRINT	Y*	N	PRINT causes all data on a page from the home position to the cursor position to be output through the printer port. Data is output with a CR, LF, and null (or CR and null) automatically inserted at the end of each 80-character line. (Same as ESC P.) Shifted PRINT prints all data from the home position to the cursor position (not necessarily 80-character lines). (Same as ESC L.)
FUNCT			The FUNCT key transmits a user-selected character bracketed by ^A (SOH) and a carriage return (CR).

Note
*Not transmitted if in local edit mode.

Table 3-1 continued

Key Name	Transmitted? (Y/N)*	Repeat Action (Y/N)	Description
F1 through F11 (Function)	Y*	N	Transmit a three-code sequence to the computer (default) or may be user-programmed. When received, may initiate a special form or subroutine in the program that causes the terminal to display or perform a special function.
SET UP/ NO SCROLL	Y*	N	Stops screen updating during normal operation. Manually sets the operating characteristics of the terminal through the status line. During normal operation, the no scroll function is active. When NO SCROLL is pressed once, the terminal stops screen updating; when pressed again, screen updating resumes. If the receive buffer fills up while update is disabled, the terminal will send X-Off to the computer, causing it to stop sending data. When update is reenabled, the buffer will empty, X-On will be sent, and data will be transmitted to the computer. Shifted SET-UP/NO SCROLL displays the terminal operating characteristics and permits manual changes to these values on the status line.
CHARACTER INSERT	Y*	Y	Enters a space at the cursor position, causing all succeeding characters to shift one position to the right. All characters shifted past the 80th character will be lost (unless page edit is on). Shifted CHAR INSERT changes edit mode from edit to insert. (Table 4-11.)
CHARACTER DELETE	Y*	Y	Deletes the character at the cursor position and causes all succeeding characters to shift one position to the left. Shifted CHAR DELETE changes edit mode from insert to edit.
LINE INSERT	Y*	Y	LINE INSERT creates an entire line of space characters on the cursor line. The data on the cursor line and all following lines will shift down one line (the last line on the page will be lost). Shifted LINE INSERT changes the edit mode from line to page.

Note
*Not transmitted if in local edit mode.

Table 3-1 continued

Key Name	Transmitted? (Y/N)*	Repeat Action? (Y/N)	Description
LINE DELETE	Y*	Y	LINE DELETE causes the entire line at the cursor position to be deleted. All following lines will shift up one line. Shifted LINE DELETE changes the edit mode from page to line.
LINE ERASE and PAGE ERASE	Y*	Y	LINE ERASE and PAGE ERASE replace the unprotected data (from the cursor to the end of the line or page) with a space of the proper intensity. Shifted LINE ERASE and shifted PAGE ERASE cause a line erase to null or a page erase to null.
SEND	Y*	N	Sends all unprotected data on the page from home through the cursor position to the computer. Shifted SEND sends all data from the first column through the cursor position.

Note
*Not transmitted if in local edit mode.

3.3.1 Cursor

The lighted rectangular block on the screen is the entry spot for the following character to be typed. It is called a *cursor.* As you reach the end of a line, the cursor automatically *wraps around* to the beginning of the next line; you do not need to enter a carriage return at the end of each line.

You can change the appearance of the cursor itself. To do this, either change the dipswitches on the rear (described in Table 2-4a) or follow the instructions in 4.6.

The cursor can be moved around the screen by pressing one of the cursor control keys (marked with an arrow) if you are in the local edit mode, by entering an escape sequence (described in Chapter 4), or pressing LINEFEED (to move it down one line). To return the cursor quickly to the top left position on the screen (referred to as *home*), press the HOME key.

Cursor movement is affected by the use of auto page and/or protect mode. Refer to 4.13 and 4.14.

3.4 SETTING UP THE TERMINAL

The bottom line on the screen is a status line which displays the following information:

Currently-selected cursor position
Edit mode
Communication mode
Terminal baud rate

Additional information such as terminal or printer busy and some error messages will appear automatically when appropriate. The terminal default values (those selected by switch settings) will be displayed until they are changed using the procedure described here. You can also change these values either locally or from the computer using the escape and control sequences for each value.

The possible values for the status line are summarized in Table 3-2 and described in greater detail in the following sections.

The left block on the status line displays the cursor position. This value automatically changes as the cursor is moved and cannot be changed by entering the status line.

To change the other values on the status line, follow these steps:

1. Press SHIFT and SET-UP at the same time.
2. Look for the cursor to appear in the block which displays either DUPE or LOCE.
3. Press T to change the values of a block. Figure 3-3 lists the values which may appear in the status line blocks.
4. Press → to move the cursor to the next status line block to be changed.
5. Press T to select a new value.
6. Press SHIFT and SET-UP at the same time to leave the status line and return to normal operation.

At the next power on, the status line will return to default values.

3.5 EDITING

While entering or changing text on the screen in the local edit mode, you can delete or insert a character, a line (either partially or completely) or the data on the screen (either partially or completely) using the editing keys described in Table 3-1.

Deletions will start with the column position of the cursor.

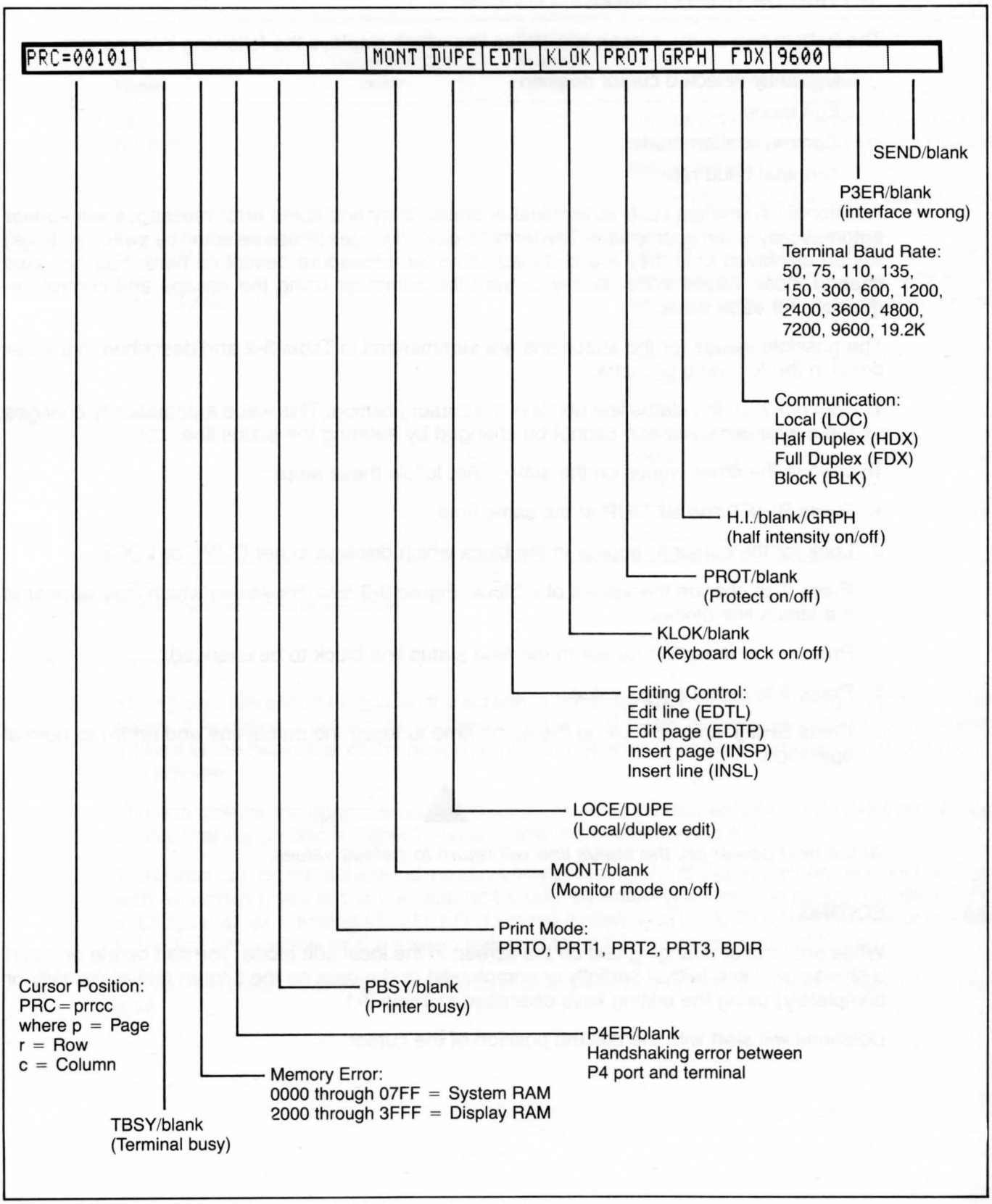


Figure 3-3 Status Line Fields

3.6 COMMUNICATING WITH THE COMPUTER

The terminal can communicate with the computer in any of four communication modes:

Local
Block
Half duplex (conversational)
Full duplex (conversational)

The selection can be made using one of three methods:

Changing switch settings (2.3.5)
Changing the status line (3.4)
Using escape sequences (4.22)

The communications flow caused by these modes is illustrated in Figure 3-4.

3.6.1 Local Mode

In local mode, you can enter or change text and the results are sent only to the screen. The port leading to the computer is turned off.

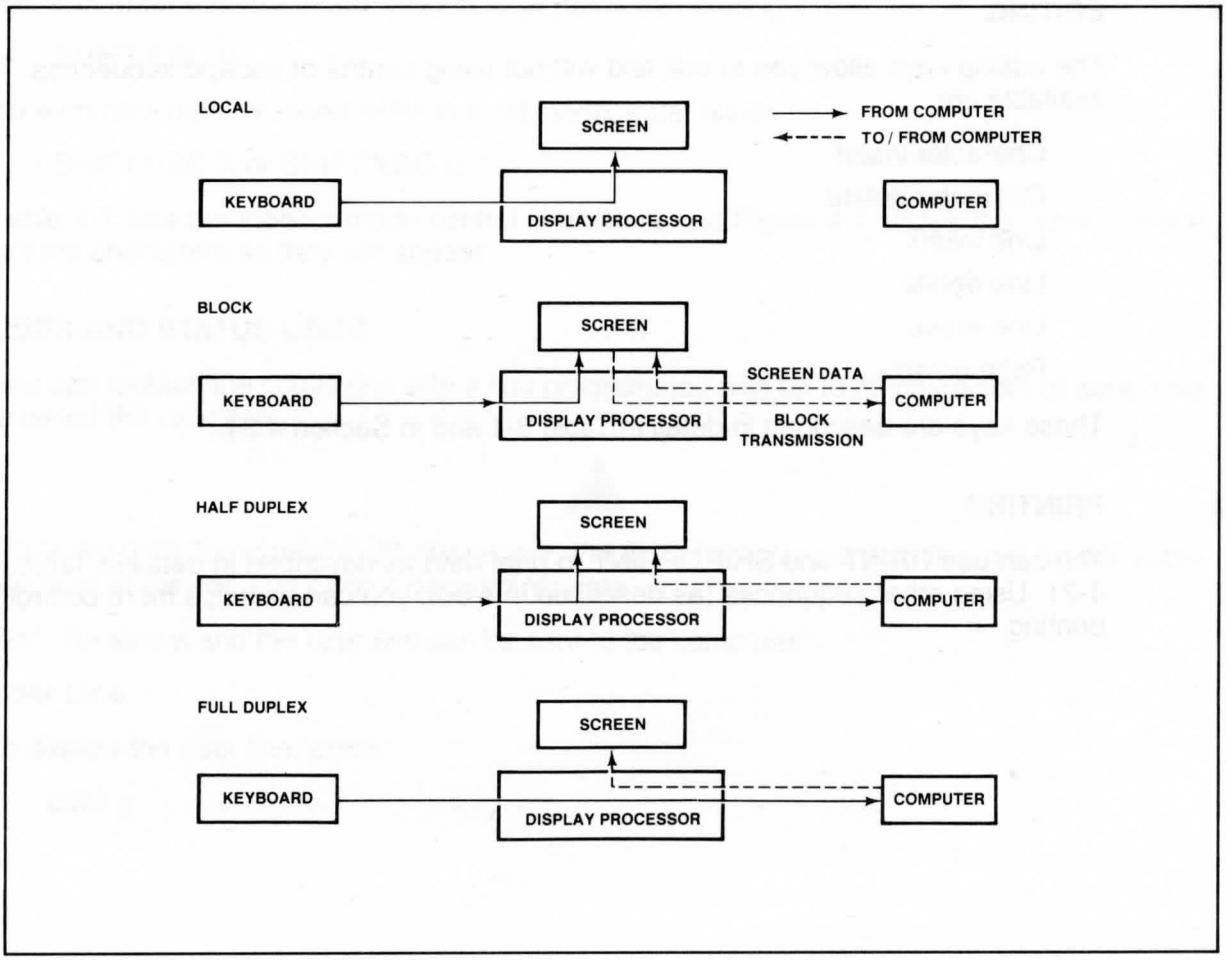


Figure 3-4 Communications Flow

3.6.2 Block Mode

In block mode, the terminal sends the results to the screen. When you are satisfied with the results of the data entry or changes made in the local mode, you can send the data to the computer in a block. Block mode allows you to make all corrections before transmission.

3.6.3 Half Duplex

The half duplex mode sends keyboard entries to the screen and to the computer at the same time.

3.6.4 Full Duplex

The full duplex mode sends keyboard entries to the computer only. If the computer is programmed to act upon a code received from a keyboard entry, it may echo the result back to the terminal. (The time needed to echo back the information is so short it will seem to happen simultaneously.) For example, if *A* is pressed on the keyboard, the computer will probably send the *A* back to the terminal screen.

3.6.5 Conversational Modes

In conversational modes, communication with the computer occurs on a continuous basis. The terminal is conversational in either half or full duplex modes.

3.7 EDITING

The editing keys allow you to edit text without using control or escape sequences. The keys available are:

Character insert
Character delete
Line insert
Line delete
Line erase
Page erase

These keys are described in detail in Table 3-1 and in Section 4.24.

3.8 PRINTING

You can use PRINT and SHIFT/PRINT to print data as described in detail in Tables 3-1 and 4-21. Using other sequences (as described in 4.30), you can exercise more control over the printing.

4. PROGRAMMING

This manual is written for the latest Model 950 firmware. Earlier firmware (i.e., 1.0) functions may not correspond to this manual.

4.1 INTRODUCTION

Your computer programs can control the terminal by transferring to it the appropriate ASCII codes. This chapter describes the features which can be utilized in your programs.

4.2 MONITOR MODE

You can display control commands to make program debugging easier. This is called *monitor mode* and it can be used in local mode or through the computer.

To enable monitor mode via the computer, enter

ESC U

To terminate the display of the control commands, enter either

ESC u or ESC X

You can enter monitor mode while in local mode by entering

SHIFT/ESC U

To terminate monitor mode while in local mode, enter either

SHIFT/ESC X or SHIFT/ESC u

Table 4-1 lists the monitor mode control characters and Figure 4-1 shows the monitor mode control characters as they will appear.

4.3 USER AND STATUS LINES

You can replace the status line with a line programmed with up to 79 characters of data. This is called the *user line.*

While the 25th line contains 80 characters, the first character position is used for the video attribute of the line and cannot be used for data.

Both the status and the user line can be sent to the computer.

4.3.1 User Line

To display the user line, press

ESC g

To load the user line with data:

1. Display the user line (if desired) by entering ESC g.
2. Press

   ESC f
3. The first character position is used for the video attribute for the user line. (Default is reverse video.) You can also add another attribute at any position in the line. To enter a video attribute for all or part of the user line, enter

   ESC G n

   where n is the position at which the attribute will begin and is a value from Table 4-2.
4. Enter up to 79 characters of text. (The message will appear on the user line as it is entered.)
5. You can move the cursor to any position by sending TAB plus the position (using a value from Table 4-2).
6. Press

   RETURN

   to end the programming mode.

To send the user line to the computer, press (in sequence)

ESC Z 0

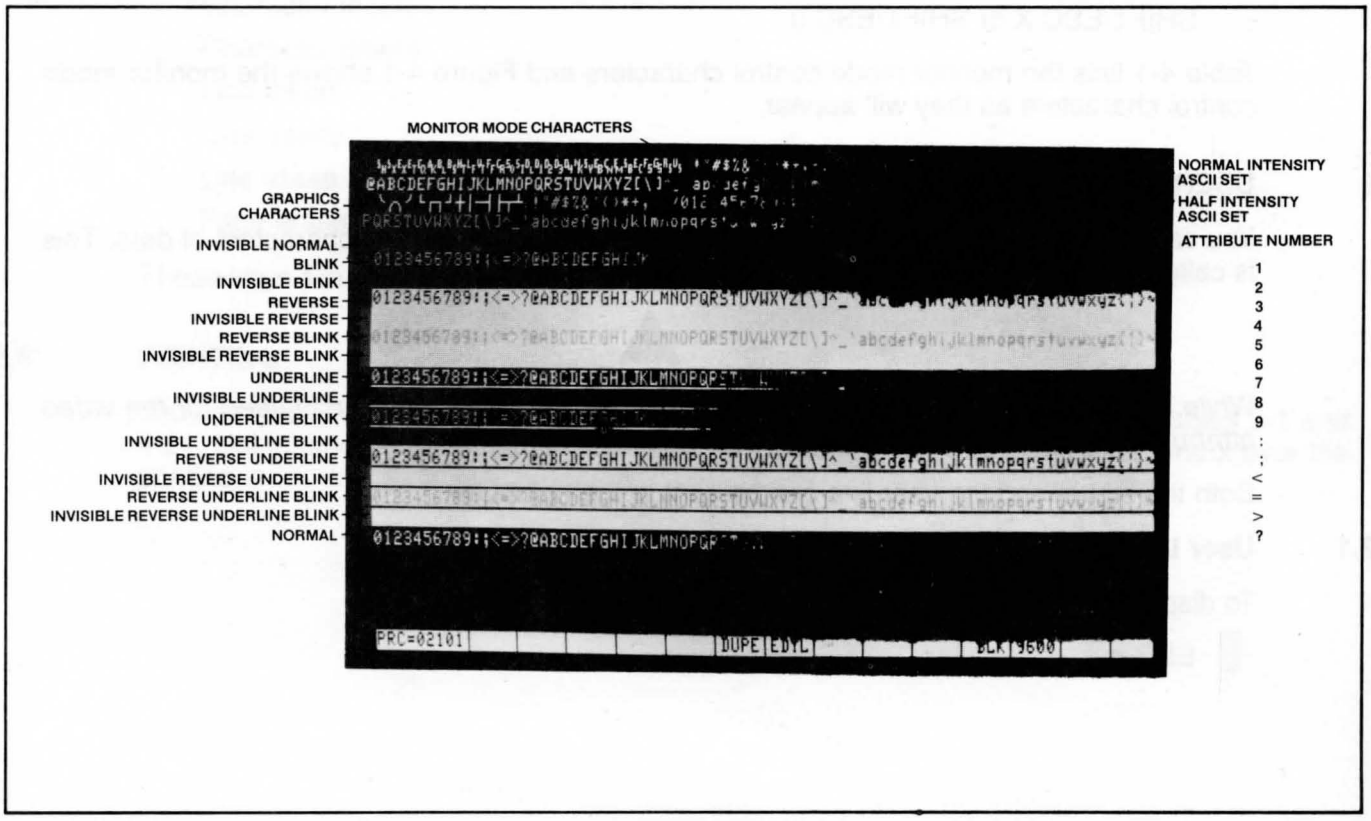


Figure 4-1 Video Attributes and Monitor Mode

To redisplay the status line after displaying the user line, press

ESC h

Table 4-1 Monitor Mode Control Characters

Code	ASCII	Hex	Character Displayed
^@	NULL	00	none
^A	SOH	01	S_H
^B	STX	02	S_X
^C	ETX	03	E_X
^D	EOT	04	E_T
^E	ENQ	05	E_Q
^F	ACK	06	A_K
^G	BEL	07	B_L
^H	BS	08	B_S
^I	HT	09	H_T
^J	LF	OA	L_F
^K	VT	OB	V_T
^L	FF	OC	F_F
^M	CR	OD	C_R
^N	SO	OE	S_O
^O	SI	OF	S_I
^P	DLE	10	D_L
^Q	DC1	11	D_1
^R	DC2	12	D_2
^S	DC3	13	D_3
^T	DC4	14	D_4
^U	NAK	15	N_K
^V	SYN	16	S_Y
^W	ETB	17	E_B
^X	CAN	18	C_N
^Y	EM	19	E_M
^Z	SUB	1A	S_B
^[	ESC	1B	E_C
^\	FS	1C	F_S
^]	GS	1D	G_S
^^	RS	1E	R_S
^_	US	1F	U_S
DEL	DEL	7F	▒

Table 4-2 Cursor Coordinates

Row/ Column	ASCII Code Transmitted	Row/ Column	ASCII Code Transmitted	Row/ Column	ASCII Code Transmitted
1	Space	33	@	65	`
2	!	34	A	66	a
3	"	35	B	67	b
4	#	36	C	68	c
5	$	37	D	69	d
6	%	38	E	70	e
7	&	39	F	71	f
8	'	40	G	72	g
9	(	41	H	73	h
10	)	42	I	74	i
11	*	43	J	75	j
12	+	44	K	76	k
13	,	45	L	77	l
14	–	46	M	78	m
15	.	47	N	79	n
16	/	48	O	80	o
17	0	49	P	81	p
18	1	50	Q	82	q
19	2	51	R	83	r
20	3	52	S	84	s
21	4	53	T	85	t
22	5	54	U	86	u
23	6	55	V	87	v
24	7	56	W	88	w
25	8	57	X	89	x
26	9	58	Y	90	y
27	:	59	Z	91	z
28	;	60	[	92	{
29	<	61	\	93	|
30	=	62	]	94	}
31	>	63	^	95	~
32	?	64	_	96	DEL/RUB

4.3.2 Status Line

To send the status line to the computer, press (in sequence)

ESC Z 1

4.4 LINE LOCK

The line lock feature allows you to lock the 80-character line on which the cursor is positioned into screen memory until the lock is released. The line will remain fixed in position on the screen regardless of the action of the remainder of the screen data (i.e., scrolling). The line lock function may be used to set up a stationary 80-character line or group of lines while other screen data scrolls past. Once line lock is cleared, all lines on the page can scroll normally.

You may lock multiple lines in any sequence; however, no more than 23 of the 24 lines on each page may be locked.

To enable line lock, enter

ESC ! 1

To disable line lock, enter

ESC ! 2

▲

This command will unlock the entire screen.

4.5 DISABLING/ENABLING THE KEYBOARD

You can disable (lock) all keys except FUNCT, PRINT, BREAK, SET-UP, NO SCROLL, and the function keys using a command sent from the computer.

Once the keyboard is disabled, it can only be enabled by another command.

▲

If your applications program echoes all codes, the keyboard may be accidentally disabled.

To disable the keyboard, enter

ESC #

The keyboard will remain disabled until one of the following occurs:

The terminal receives an ESC " sequence

You press BREAK twice while holding down the SHIFT key

You change the status line

4.6 CURSOR DISPLAY

The cursor may appear in any of five ways. To change the appearance of the cursor without changing the rear switch settings, enter one of the following escape sequences:

Appearance	Command
Cursor not displayed	ESC .0
Blinking block cursor	ESC .1
Steady block cursor	ESC .2
Blinking underline cursor	ESC .3
Steady underline cursor	ESC .4

4.7 KEYCLICK AND BELL

You can control keyclick (the noise made as each key is activated) and sound the terminal's bell with the following code sequences:

Function	Command
Keyclick on	ESC >
Keyclick off	ESC <
Ring bell	^G

4.8 SMOOTH SCROLL

The smooth scroll feature prevents display jitter as text lines scroll up or down and the slower rate of scrolling allows you to more easily read the scrolling text.

When smooth scroll is on, the screen scrolls smoothly at a rate of six data rows per second. Without smooth scroll, screen data scrolls as fast as it is received.

To activate smooth scroll, enter

ESC 8

To turn off smooth scroll, enter

ESC 9

The computer must respond to X-On/X-Off commands or DTR control in order for this feature to work correctly.

4.9 VIDEO DISPLAY

The video display feature turns the screen on (default) or off. You could use this to blank the screen while the computer is building a form or writing a long data list. The following commands control video display:

Screen Display	Command
On	ESC n
Off	ESC o

4.10 VISUAL ATTRIBUTES

The visual attributes of each character as well as the spaces on the screen may be controlled to define the appearance of the screen (either wholly or partially).

Two methods may be used to set visual attributes. The method used determines whether the attribute will occupy a space and how much of the display will be affected. The two methods are summarized in Table 4-3.

Table 4-3 Visual Attributes

Method	Uses	Affects	Attribute Occupies Space?
1	Escape sequence	Partial/whole line/screen	Yes
2	Switch setting or escape sequence	Whole screen	No

The following attributes are available:

Normal Video Restores the background of the screen to that selected by rear terminal switch settings.

Reverse Video Changes the background of the screen to the reverse of that which appears at power on (default). If the screen is normally black with green characters, it will now be green with black characters. If method one is used, this attribute starts with the cursor position and continues until another attribute is encountered.

Half Intensity Changes the intensity to half of normal on a character-by-character basis.

▲

Half intensity differs from other visual attributes in two ways:

1. *Once it is set, it affects all characters entered (regardless of cursor position) until it is turned off.*
2. *This attribute character never occupies a character space.*

Underline Creates a solid line below all characters on the line (including the line created by the underscore key). This attribute starts with the cursor position and continues until another attribute is encountered. (Changed only by method one.)

Blink Causes all characters to blink. This attribute starts with the cursor position and continues until another attribute is encountered. (Changed only by method one.)

Blank Causes all data entered on the line to be invisible to you although the cursor will move and be transmitted to the computer. (A typical application might be payroll information.) This attribute starts with the cursor position and continues until another attribute is encountered. (Changed only by method one.)

Setting Visual Attributes

Method One

To set a visual attribute which can affect part or all of the screen, follow these steps:

1. Place the cursor one position *before* you want the attribute to start.

Remember that each attribute occupies a character position. If you type over the attribute, it will be lost unless you have protected it using protect mode.

2. Enter the appropriate escape sequence as listed in Table 4-4.

Table 4-4 Escape Sequences for Visual Attributes

Attribute	Escape Sequence
Normal (default) video	ESC G 0
Invisible normal video	ESC G 1
Blink	ESC G 2
Invisible blink	ESC G 3
Reverse video (reverse of default)	ESC G 4
Invisible reverse	ESC G 5
Reverse and blink	ESC G 6
Invisible reverse and blink	ESC G 7
Underline	ESC G 8
Invisible underline	ESC G 9
Underline and blink	ESC G :
Invisible underline and blink	ESC G ;
Reverse and underline	ESC G <
Invisible reverse and underline	ESC G =
Reverse and underline and blink	ESC G >
Invisible reverse and underline and blink	ESC G ?

Method Two

This method changes the entire screen display using switches on the rear of the terminal or an escape sequence. Changing the display with those switches or with the escape sequence described in this section differs from the video attributes described above in two ways:

The attribute occupies no space on the screen

The entire screen is affected

Table 4-5 summarizes the effect of these escape sequences in combination with the rear switch settings.

Table 4-5 Screen Attributes

Rear Switch Setting	Escape Sequence	Function	Effect
Normal (green on black)	ESC b	Set reverse background	Changes screen to reverse video (black on green)
Reverse (black on green)	ESC b	Set reverse background	No effect since screen is already reversed with switch setting
Normal	ESC d	Set normal background	No effect since screen is already normal
Reverse	ESC d	Set normal background	Changes screen to normal video (green on black)

4.11 SPECIAL GRAPHICS

The special graphics feature converts all alphanumeric characters received while this feature is active to one of 15 special graphic characters.

When this feature is being used, the SHIFT key has no effect and the status line displays GRPH. When special graphics is inactive, the status line displays either a space (or H.I. if half intensity was previously set).

To control the special graphics mode, use the following commands:

Status	Code Sequence
Special graphics on	ESC $
Special graphics off	ESC %

The graphics characters which will be displayed are shown in Figure 4-2 with the corresponding alphanumeric characters.

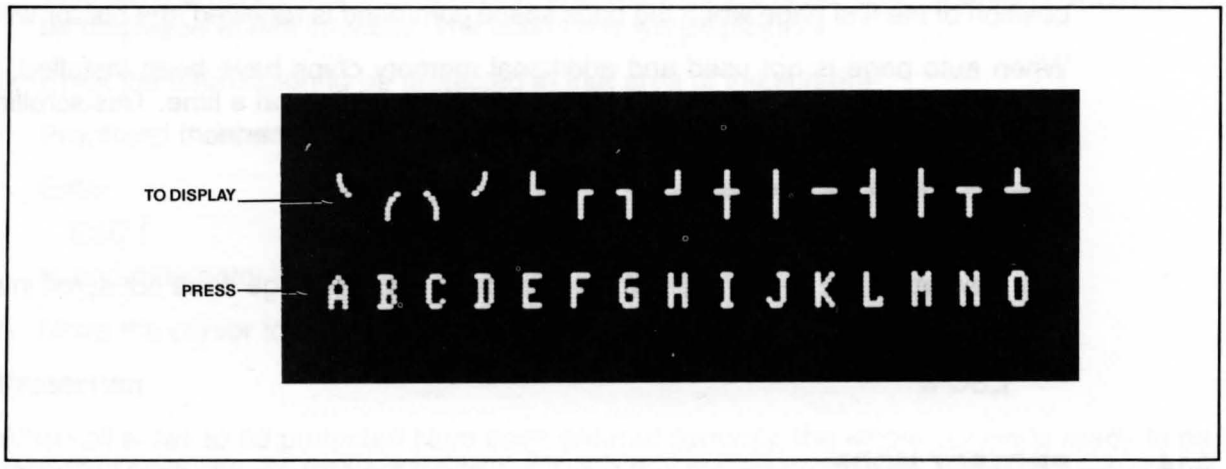


Figure 4-2 Special Graphics Characters

4.12 ADDITIONAL SCREEN MEMORY

You can add additional screen memory to the terminal by installing one or three chips in addition to the standard chip (which provides 24 lines or one page of memory).

If your terminal contains the second chip (providing an additional 24 lines), you can divide the total 48 lines into either two 24-line pages or one 48-line page. If your terminal contains the four chips (adding 48 lines to the 48 provided by the first two chips), you can divide these 96 lines into four 24-line pages (standard), two 48-line pages, or a single 96-line page. You can scroll back and forth within the pages, one screen (page) at a time.

To set the number of lines per page, enter

ESC \ n

where n = 1 for 24 lines per page
2 for 48 lines per page
3 for 96 lines per page

To look at the next page of memory, enter

ESC K

To print the current page and look at the next page, enter

ESC P or ESC L

To look at the previous page of memory, enter

ESC J

If you move forward (or backward) to the next page, the cursor will be located in the same position on the new page as it was on the previous page.

4.13 AUTO PAGE

Auto page requires the installation of the additional screen memory chips (4.12). With the auto page feature on, when the cursor reaches the end of the screen, the screen flips to a new page and the cursor moves to the first unprotected position on the new page. (The flipping action of auto page is similar to viewing photographic slides.) If the cursor is at the home position and it receives the back space command, the screen flips to the previous screen and moves the cursor to the last unprotected position on the new page. If the cursor is in the home position of the first page when the back space command is received, the cursor will not move.

When auto page is not used and additional memory chips have been installed, the screen scrolls through the total pages, allowing you to view 24 lines at a time. This scrolling action is similar to the action of a movie camera which is panning a scene.

To turn on auto page, enter

ESC v

This new page will appear as a whole new page (i.e., the page does not scroll into view).

To turn auto page off, enter

ESC w

4.14 PROTECT MODE

4.14.1 Introduction

Using protect mode during the creation of a page allows you to:

Protect designated areas of the page from future change by the operator
Control transmission of those areas

Using protect mode involves two procedures:

Creating the areas to be protected using protected writing

Protecting all of those areas with protect mode

4.14.2 Application

A typical application would be the creation of a form, leaving blank spaces for later entry of variable information. Were the form headings not protected by protect mode, they would be vulnerable to change or accidental deletion as the form was being filled in.

4.14.3 Effect

Fields input under protected writing appear on the screen at one half the regular intensity. When protect mode is in effect, the cursor is not able to enter those fields, but will instead advance across those fields to the first unprotected field when you use → or ←. ↑, ↓, or linefeed will, however, move the cursor to the protected field. The screen does not scroll up in protect mode. If the whole screen is protected, the cursor will go to the home position and will not move. At no time, however, can any data be entered in the protected field.

4.14.4 Input

Individual areas (fields) which will be given blanket protection from later change are created using protected writing mode.

Information must be input using this procedure if it is to be protected later.

1. Position the cursor where the first protected character is to be located.
2. Enter
   ESC)
   This turns on protected writing mode. Until the mode is reset, each character entered will be displayed at *half intensity.* The status line will display *H.I.*
3. Enter the information to be protected in that area of the screen.
4. Proofread the entry and correct it if necessary.
5. Enter
   ESC (
   to end data entry in that area and turn off protected writing mode.
6. Move the cursor to the next area to be protected and repeat.

4.14.5 Protection

When all areas to be protected have been entered correctly, the *whole screen* is ready to be protected from change (protect mode on). Once this protection is given, the cursor will not be able to enter those areas unless the protection is removed.

1. To turn on protect mode, enter
   ESC &

The position of the cursor during this escape sequence is irrelevant.

2. Look for *PROT* on the status line, indicating that protect mode is on.

With protect mode on, all half-intensity, graphics, and attribute characters are protected from overwriting or erasure. All data and visual attributes within the protected areas are protected.

To disable protect mode (remove the protection), enter

ESC '

The absence of *PROT* on the status line indicates that protect mode is off.

4.15 NORMAL AND REVERSE LINEFEED

You can cause a normal linefeed with the sequence

^J

To move the cursor up one line (reverse linefeed), send

ESC j

Using auto page and/or protect mode can affect where the cursor will move when a linefeed or reverse linefeed is received.

Tables 4-6 and 4-7 summarize the effect of auto page and protect mode when linefeed and reverse linefeed are used.

Linefeeds received by the terminal under certain conditions may result in the loss of data. Read the following control code explanations carefully.

Table 4-6 Effects of Auto Page and Protect Mode on Linefeed Actions

Auto Page	Protect Mode	Description
Off	Off	With auto page (4.13) on and protect mode (4.14) off, a linefeed advances the cursor to the next line on the page. If the cursor is at the bottom of the screen, linefeeds cause the display to roll up one line for each linefeed. If the cursor is also at the bottom of the page, a linefeed causes a new line of data to appear at the bottom of the screen and results in the loss of the top line of data on the page. The new line contains the insert character (4.20), which is normally spaces, but may be programmed to be any other character.
On	Off or On	Linefeed advances the cursor to the next line on the page. When the cursor reaches the bottom of the page, it will advance to the first line of the next page. When it reaches the last line of the last page, it advances to the first line of the first page (page zero).
Off	On	A linefeed causes the cursor to return to the top of the current page when it reaches the last line of the page.

Table 4-7 Effects of Auto Page and Protect Mode on Reverse Linefeed Actions

Auto Page	Protect Mode	Description
On	Off or On	The cursor will move to the last line of the previous page when it reaches the first line of the current page. When the cursor reaches line one of page zero, it will not move further.
Off	On	The cursor does not move when on the first line.
Off	Off	The screen will scroll down one line when the cursor is on the first line.

4.16 CURSOR CONTROL CODES

All cursor controls may be performed using escape and control sequences sent from the computer.

The cursor control codes are summarized in Table 4-8.

Table 4-8 Cursor Control Commands

Cursor Control	Control Code	Auto Page	Protect Mode	Effect
Up	^K	Off/On	Off/On	Moves the cursor up one line until it encounters the top of the screen. If the cursor is not on the first line of the page, the display will roll down one line with each ^K until the cursor reaches the top of the page. Once it reaches the top of the page, receipt of further ^K codes has no effect.
Down	^V	Off/On	Off/On	Moves cursor down one line.
		Off	Off/On	If the cursor is on the bottom line of the page, the code has no effect.
Left	^H	Off/On	Off/On	Functions the same as BACKSPACE. Moves the cursor left to the next unprotected position on the page. If the cursor is currently in the first column of the line, it will move to the last column of the preceding line.
HOME	^^	Off	On	Moves cursor to the first unprotected space on the screen. If the cursor is currently at the home position or the first unprotected position on the page, the code has no effect.
		On	Off/On	If the cursor is at the home position or the first unprotected position on the page, the cursor will move to the end of the preceding page or to the last position of the last unprotected field of the preceding page. If the current page is page zero, the code has no effect.

Table 4-8 continued

Cursor Control	Control Code	Auto Page	Protect Mode	Effect
Right	^L	Off/On	Off/On	Moves the cursor right one column. If the cursor is at column 80, it moves the cursor to the first column of the next line.
		Off	Off	Causes the screen to scroll one line if the cursor is at column 80 of the last line.
		On	Off/On	If the cursor is at the last unprotected position on the page, the cursor will move to the first unprotected position of the next page. If that page is the last page, the cursor will advance to the first unprotected position of the first page.
		Off	On	If the cursor is at the last unprotected position on the page, the cursor will move to the first unprotected position of the current page.
Carriage Return	^M	Off/On	Off	Moves the cursor left to column one of the current line.
		Off/On	On	Moves the cursor to the first unprotected position of the current cursor line.
New Line	^_ (underline)	Off/On	Off/On	Causes the terminal to perform a LF and a CR.

4.17 THE FUNCTION KEYS

The function keys (F1 through F11) send a user-defined or default code to the screen, to the computer, or to both, depending on whether the keys are set up for local or duplex communication mode. (For example, the user-defined code may be a frequently-used escape or control code sequence in a text editing application.)

4.17.1 Description

There are eleven function keys; using them in combination with SHIFT allows up to 22 sets of codes to be transmitted.

4.17.2 Default Messages

When the terminal is first turned on, the function keys are already programmed with default messages set to full duplex mode. If you do not program the function keys, the default values shown in Table 4-9 will be transmitted by each function key.

Table 4-9 Default Function Key Values

Key	Unshifted Code	Shifted Code
F1	´A @ CR	´A \ CR
F2	´A A CR	´A a CR
F3	´A B CR	´A b CR
F4	´A C CR	´A c CR
F5	´A D CR	´A d CR
F6	´A E CR	´A e CR
F7	´A F CR	´A f CR
F8	´A G CR	´A g CR
F9	´A H CR	´A h CR
F10	´A I CR	´A i CR
F11	´A J CR	´A j CR

4.17.3 Programming the Function Keys

You may program the function keys (i.e., not use the default values listed in Table 4-9) following the procedure described in this section.

Enter the following code in the exact sequence shown:

ESC ¦ p1 p2 message ^Y

where

p1 is the number of the function key. The values of p1 are as follows:

Key	Unshifted	Shifted
F1	1	<
F2	2	=
F3	3	>
F4	4	?
F5	5	@
F6	6	A
F7	7	B
F8	8	C
F9	9	D
F10	:	E
F11	;	F

The message can contain up to 63 bytes per key. (The total memory available for the function keys is 256 bytes total or 64 characters per key; however, one byte is added by the terminal processor for control purposes.)

p2 is one of the following values:

1 = Send to the computer (full duplex)
2 = Send to screen (local)
3 = Send to computer and to screen (half duplex)

^Y is the termination character

Because control, escape, cursor position, and similar function keys are not normally stored, a ^P embedded in the text of the function key message may be used to store the next character entered.

For example, assume that the message desired for key F1 in local mode is:

TURN ON THE PRINTER

Precede this message with the following:

ESC ¦

The key number (1 for key F1)

The transmission mode (2 for local mode)

The entry will be:

ESC ¦ 1 2 TURN ON THE PRINTER CR ^Y

Program the computer's input/output string routine to catch the entire string and then process it (unless you are using an interrupt-driven computer, in which case you should not need to worry about data being lost). If your computer cannot receive the message fast enough, enter a ^@ (null) sign between each character of the message.

4.17.4 Using Function Keys

To use one of the function keys in normal operation, press the function key for the first message, or press SHIFT and the key at the same time for the second message.

4.18 THE FUNCT KEY

Not to be confused with the function keys described in 4.17, the FUNCT key transmits a user-selected character (the ASCII code of the depressed key) bracketed by ^A (SOH) and a carriage return (CR). For example, if a ^A C CR sequence is required for a special operation in a text editing program, press FUNCT and C at the same time to transmit ^A C CR to the computer.

Program your computer's input/output string routine to catch the entire string and then process it (unless you are using an interrupt-driven computer, in which case you do not need to worry about data being lost).

4.19 ADDRESSING AND READING THE CURSOR POSITION

The computer can position the cursor (called *addressing* or *loading* the cursor) and determine the position of the cursor (*reading* the cursor).

To address the cursor, enter

ESC = r c

or

ESC - p r c

where

r is the desired row (line). Refer to Table 4-2 to find the ASCII code representing the desired row.

c is the desired column. Refer to Table 4-2 to find the ASCII code representing the desired column.

p is the page number if the chip for additional pages of memory has been installed. Possible values are:

0 for page one
1 for page two
2 for page three
3 for page four

▲

If your applications program inserts nulls between characters, loading the cursor will not function as described. Instead, the cursor will go to an unpredictable position.

For example, if you want the cursor to go to Row 9 of Column 50, enter

ESC = (Q

To read the cursor's row and column position (listed in Table 4-2), enter

ESC ?

To read the cursor's current page, row, and column, enter

ESC /

The page value will be

0 for page one
1 for page two
2 for page three
3 for page four

The row and column values sent (specified in Table 4-2) are followed by a carriage return.

4.20 LOADING AN INSERT CHARACTER

Several editing, erase, and clear functions (in addition to scroll and reverse scroll) cause certain areas of the page to be replaced with a predefined character. When the terminal is turned on, this insert character is defined as a space (ASCII 20 HEX).

During normal operation, the insert character may be redefined to be any ASCII character (e.g., a null or an underline) with the following escape sequence:

ESC e n

where n is the insert character.

4.21 TAB PROGRAMMING

Two types of tabs are available:

Typewriter-style tabs
Field tabs (used when protect mode is on)

Table 4-10 summarizes all tab controls.

Table 4-10 Tab Controls

Action	Control Code	Auto Page	Protect Mode	Effect
Set tab[1]	ESC 1	Off/On	Off	Sets a typewriter-style column tab.
		Off/On	On	Generates a vertical column of half-intensity spaces from the cursor position down to the first write-protected character or to the end of the page, whichever is first.
Typewriter (Column) Tab	\I	Off/On	Off	Causes the cursor to advance to the next typewriter-style tab set. If no tabs are set, the code has no effect and the cursor will not move.
		Off	On	If there are no following unprotected fields, the cursor moves to the first character of the first unprotected field at the top of the page. If there are no characters on the page, the cursor will move to the home position.
		On	On	If no unprotected field follows, the cursor will advance to the first unprotected character on the next page. If no unprotected field exists on the next page, the cursor moves to home position on that page.
Field Tab	ESC i		Off	No effect.
			On	If there are no following unprotected fields, the cursor moves to the first character of the first unprotected field at the top of the page. If there are no unprotected characters on the page, the cursor will move to the home position.
Back Tab	ESC I	Off/On	Off	Causes the cursor to go back to the previous tab position set. If no tabs are set or if the cursor is on the first tab position on the page, this code moves the cursor to the first column on the line.
		Off	On	Moves the cursor back to the start of the first preceding unprotected field. If no preceding positions exist, the cursor will not move.

Table 4-10 continued

Action	Control Code	Auto Page	Protect Mode	Effect
		On	On	If the cursor is at the first unprotected position on the page, it will move the cursor to the first unprotected character of the last unprotected field of the previous page. If no protected fields exist, home position is considered the start of an unprotected field. If the cursor is on the first unprotected position of the first page, this code has no effect.
Clear Typewriter Tab[2]	ESC 2	Off/On	Off	Clears the typewriter tab where the cursor is located when this code is entered.
		Off/On	On	No effect.
Clear All Tabs[3]	ESC 3	Off/On	Off/On	Clears all typewriter tabs regardless of the position of the cursor when the code is entered.

Notes

1. To set a tab, move the cursor to the column position where you want a tab. Be sure you enter a *numeral* one, not a lower case *L*.
2. Position the cursor at the tab to be cleared before entering the sequence.
3. The position of the cursor when this code is entered is not important.

4.22 COMMUNICATION MODES

Communication between the terminal and the computer can be controlled by escape sequences, switch settings, or the status line. Four modes are possible:

Local
Block
Half duplex (conversational)
Full duplex (conversational)

These are described in detail in 3.6.

4.22.1 Local

To operate in the local mode, enter

ESC c

4.22.2 Block

To operate in block mode, enter

ESC B

4.22.3 Half Duplex

To operate in half duplex mode, enter

ESC DH

4.22.4 Full Duplex

To operate in full duplex mode, enter

ESC DF

4.22.5 Conversation

Half duplex and full duplex are both conversational modes. You can return to the previous conversational mode by entering

ESC C

For example, you were using full duplex before you changed to local mode. Now you want to return to full duplex. You can do so by entering either ESC C (conversational) or the command for full duplex (ESC FD).

4.23 EDIT KEYS

The edit modes which are described in this section can be selected either with the switches on the rear of the terminal or with control codes.

Two communication editing modes are available: local edit and duplex edit.

4.23.1 Local Edit

Using local edit enables you to change the text without transmitting the editing commands to the computer (i.e., all editing is in local mode).

In local edit mode, SEND, PRINT, and the edit keys (CLEARSPACE, BACKSPACE, ↑, ↓, →, ←, TAB, HOME, BACK TAB, LINE INSERT, LINE DELETE, CHARACTER INSERT, CHARACTER DELETE, LINE ERASE, and PAGE ERASE) and the changes caused by these keys are not transmitted to the computer.

To enter local edit mode, either change the status line or enter

ESC k

While local edit is on, all other keys will operate normally.

4.23.2 Duplex Edit

When duplex edit is selected, all editing commands are transmitted to the computer. To make editing changes which will be sent to the computer in the same manner as the alphanumeric keys (i.e., either half or full duplex), either change the status line or enter

ESC l (lower case "L")

For example, if the terminal is set for half-duplex operation, both the alphanumeric and edit keys will operate in half duplex mode.

4.24 EDITING TEXT

Changing text can involve the following three actions:

Replacing (i.e., typing over) existing text; referred to here as *editing*

Inserting new text which pushes existing text to the right from the cursor position

Deleting existing text (by either character, line, or page) by moving that text backward toward the cursor

Editing, inserting, and deleting can occur within either the line on which the cursor is positioned or within the entire page of memory. Text which reaches the beginning or the end of a line or the page by these actions will, if moved *further*, be lost (i.e., "fall off") that boundary (either line or page).

The four modes of operation available are:

Edit Page

Edit Line

Insert Page

Insert Line

These modes can be selected by any of the following methods:

Changing the status line (3.4)

Pressing some of the edit keys along with the SHIFT key (see Table 4-11)

Sending escape commands (see Table 4-11)

Table 4-11 summarizes the changes possible and the commands and keys which will cause those changes.

Table 4-11 Edit and Insert Modes

Change From	Change To	Command	Press	Status Line Displays
Edit (replace)	Insert	ESC q	Shifted Char Insert	INS
Insert	Edit (replace)	ESC r	Shifted Char Delete	EDT
Line	Page	ESC N	Shifted Line Insert	P
Page	Line	ESC O	Shifted Line Delete	L

The following sections describe in detail the effect of these modes.

Page Edit—When page edit is selected and characters are inserted, the remaining text moves forward to the next line as necessary. The *page* length is determined by the number of lines of memory for that page. For example, if you have the extra memory chips installed and have configured the memory to have one 96-line page, the text, of which you can see 24 lines at a time, would be able to flow forward within that 96-line area. When the end of the page is reached, however, text being pushed forward by the inserted text will be lost as it moves beyond column 80 of the last line of memory.

When characters are deleted while page edit is in effect, the character in column one of each line will move to column 80 of the previous line (i.e., backward wraparound).

Page edit will be indicated by the presence of *EDTP* on the status line.

Line Edit—This is the default mode (i.e., the mode in effect when the terminal is turned on). Line edit allows you to insert or delete text only on the line on which the cursor presently rests. Characters will move forward or backward until column one or column 80 is reached. Text can be lost (i.e., "fall off") either end of the line being edited.

Line edit will be indicated by the abbreviation *EDTL* on the status line.

Insert Line—Insert line allows you to insert or delete text only within the line on which the cursor presently rests.

Insert line will be indicated by the presence of *INSL* on the status line.

Insert Page—Insert page allows you to insert or delete text in the page of memory on which the cursor is resting. Characters will move forward or backward until column one of page one or column 80 of the last line is reached. Text can be lost (i.e., "fall off") either end of the page of memory being edited.

Insert page will be indicated by the presence of *INSP* on the status line.

Table 4-12 summarizes the effects of the available editing commands in conjunction with page edit, line edit, and protect mode.

Table 4-12 Editing Commands

Edit Command	Escape Sequence	Edit Mode	Protect On/Off	Effect
Character Insert	ESC Q	–	–	Causes character at the cursor to move right one column position and enters an insert character at the cursor position.
		EDTP	–	The character at column 80 wraps to column one of the next line.
		EDTP	On	This control will turn off edit page. A character insert will insert from the cursor position to the end of the line or to the first protected field.
		EDTL	–	As characters are inserted, characters reaching column 80 are lost.
		EDTL	Off	Causes the character at the cursor to move right one column and enters an insert character at the cursor position. The character at column 80 is lost.
			On	Inserts from the cursor position to the end of the line or to the first protected field.

Table 4-12 continued

Edit Command	Escape Sequence	Edit Mode	Protect On/Off	Effect
Character Delete	ESC W	EDTL	Off	Deletes the character at the cursor position and moves all following characters left one position. At the end of the delete function, an insert character is written into the last position on the line.
		EDTP	Off	Deletes the character at the cursor position and moves all following characters left one position. At the end of the delete function, an insert character is written into the last position on the page.
		EDTL	On	Operates only from the cursor position to the end of the unprotected field or line.
Line Insert	ESC E	–	Off	Inserts a line consisting of insert characters at the cursor position. This causes the cursor to move to the start of the new line and all following lines to move down one line, resulting in the loss of the last line on the page.
		–	On	No effect.
Line Delete	ESC R	–	Off	Deletes the line at the cursor position and all following lines move up one line. The cursor will move to column one of the line and insert characters will be loaded into the last line of the page.
		–	On	No effect.
Erase to End of Line	ESC T	–	Off	Erases all characters from the cursor to the end of the line and replaces them with insert characters. If half intensity is on, half-intensity insert characters will replace the erased characters.
		–	On	Erases all unprotected characters from the cursor to the end of the field and replaces them with insert characters. If half intensity is on, half-intensity insert characters will replace the erased characters.
Erase to End of Line with Nulls	ESC t	–	Off	Erases all characters from the cursor position to the end of the line and replaces them with null characters.
		–	On	Erases all characters from the cursor position to the end of an unprotected field and replaces them with null characters.

Table 4-12 continued

Edit Command	Escape Sequence	Edit Mode	Protect On/Off	Effect
Erase to End of Page	ESC Y	–	On	Replaces unprotected characters from the cursor position to the end of the screen with insert characters. If half intensity is on, erased characters will be replaced with half-intensity insert characters.
Erase to End of Page with Nulls	ESC y	–	On	Erases all unprotected characters from the cursor position to the end of the page and replaces them with null characters.

4.25 CLEAR FUNCTION

The clear function is used in one of four ways to clear data from screen memory. Clear commands are summarized in Table 4-13.

Table 4-13 Clear Commands

Clear Command	Escape Sequence	Half Intensity	Protect	Effect
Clear Unprotected to Nulls	ESC :	Off/On	Off/On	Clears all unprotected data on the page to the null character or to the half intensity character if half intensity is on.
Clear Unprotected to Insert Characters	ESC ; ESC + ^Z	Off/On	Off/On	Clears all unprotected data on the page to insert characters. The default insert character is a space, but may be programmed to be another character. If half intensity is on, the screen will be cleared to half-intensity insert characters.
		On	Off	Clears screen to half-intensity spaces.
Clear Page to Half-Intensity Insert Characters	ESC ,	On	Off/On	Clears all unprotected data on the page to half-intensity insert characters.
Clear All Data to Nulls	ESC *	On/Off	On/Off	Clears all data on the page to nulls. Resets half intensity and protect modes.

4.26 X-ON/X-OFF CONTROL

When the terminal's receive buffer is almost full (less than 32 characters), the terminal automatically transmits X-Off to the computer, requesting it to stop sending data. When the data in the buffer has been sent to the screen or the printer's buffer, the terminal transmits X-On to the computer, indicating that the computer may resume sending data to the terminal.

This X-On/X-Off feature may be enabled or disabled with the following control sequences:

Enable X-ON/X-Off	^O
Disable X-On/X-Off	^N

At power on, X-on/X-off is enabled. If X-On/X-Off is disabled, DTR control (4.27) is enabled.

4.27 DATA TERMINAL READY CONTROL

If you have disabled the X-on/X-off feature described above, the Data Terminal Ready feature is enabled (i.e., the DTR line is high). In that case, the DTR line will go low when the 256-byte receive buffer in the terminal has received 224 bytes from the computer—until the buffer is 20 percent empty again.

4.28 USER ROM

If you have installed your own programs in the ROM (as described in the Model 950 Customizing Manual), you can command the terminal to execute one of the programs with the command:

ESC z p

where

p is the optional parameter as defined in the ROM

If the user ROM has not been installed, the command will have no effect.

4.29 COMPUTER PORT PROGRAMMING

The default operating parameters of the RS232C computer port (terminal/computer interface) can be set using switch S1 on the terminal's rear panel. The terminal processor reads these parameters once when the terminal is turned on. These may, however, be changed with escape sequences after power up.

To change the parameters, enter

ESC { p1 p2 p3 p4

where

p1 is the baud rate (with values as shown in Table 4-14)

p2 is the number of stop bits (with values as shown in Table 4-15)

p3 is parity (with values as shown in Table 4-16)

p4 is the word length (with values as shown in Table 4-17)

Table 4-14 Baud Rate Values

Value	Baud Rate
0	9600
1	50
2	75
3	110
4	135
5	150
6	300
7	600
8	1200
9	1800
:	2400
;	3600
<	4800
=	7200
>	9600
?	19200

Table 4-15 Stop Bit Values

Value	Stop Bits
0	1
1	2

Table 4-16 Parity Values

Value	Parity
0	Disabled/ignored
1	Odd (receive/transmit)
3	Even (receive/transmit)
5	Mark (transmit parity check disabled)
7	Space (transmit parity check disabled)

Table 4-17 Word Length Values

Value	Word Length
0	8 bits
1	7 bits

You would select parameters of

baud rate of 4800
one stop bit
even parity
7-bit word length

if you entered the following command sequence:

ESC { < 0 3 1

4.30 PRINTER PORT PROGRAMMING

Like the computer port, printer port default operating parameters are set with switch S1 on the rear of the terminal. The terminal processor reads these parameters once when the terminal is turned on. The parameters may, however, be changed after power up using escape sequences.

To change the parameters, use the following command sequence:

ESC } p1 p2 p3 p4

where the values for p1, p2, p3, and p4 are the same as those listed for programming the main port.

4.31 SEND FUNCTION

Once you have entered and edited data or text, you can transmit it to the computer by one of two methods:

1. Press the preprogrammed SEND key to transmit line or page data.
2. Enter a control sequence to send specific data.

4.31.1 Programming the SEND Key

To program the SEND key, enter the following code:

ESC 0 x y

where

x is 1 to program the SEND key
2 to program the shifted SEND key
y is 4 to program ESC 4
5 to program ESC 5
6 to program ESC 6
7 to program ESC 7
S to program ESC S
s to program ESC s

The SEND key operates both unshifted and shifted for transmittal of two-character escape sequences. Transmission of text by the SEND key may include embedded delimiters which define fields, end of line, and end of text.

4.31.2 Delimiter Programming

To set the send delimiters, enter the following code in the exact sequence shown below:

ESC x n p1 p2

where

n = 0 for delimit field code to p1 p2
1 for delimit line code to p1 p2
2 for delimit start protect field to p1 p2
3 for delimit end protect field to p1 p2
4 for delimit end of text to p1 p2

p1 = A standard ASCII or control character

p2 = A standard ASCII or control character

If no delimiter is desired, program p1 and p2 as nulls. For example, to eliminate the field delimiter during transmission, enter

ESC x O null null

The default delimiter values are shown in Table 4-18.

Table 4-18 Default Delimiter Values

Delimiter	Values p1	p2
Field	FS	null
Line	US	null
Start protected field	ESC	)
End protected field	ESC	(
End of text	Carriage return	null

To send specific data to the computer, use the commands shown in Table 4-19.

Table 4-19 Data Transmission Commands

Data Sent	Code	Effect
Unprotected line from start of line to cursor	ESC 4	Sends all unprotected data on the line from column one through the cursor position. Also sends an FS code (1C Hex) as field delimiters in place of each protected field and end-of-text characters at the end of the send transmission.
Unprotected page from home to cursor	ESC 5	Sends all unprotected data on the page from home through the cursor position. Sends an FS code (1C Hex) as field delimiters in place of each protected field. Sends line delimiters at the end of a line and an end-of-text at the end of the send transmission.

Table 4-19 continued

Data	Code	Effect
Whole line from start of line to cursor	ESC 6	Sends all data from the first column through the cursor position. Also sends ESC) at the beginning of each protected field and ESC (at the end of each protected field. If the character at the cursor position is protected, the terminal sends ESC ((end-protected field) to the computer. Sends the end-of-text characters at the end of the send transmission. If the data to be sent includes attribute characters, these will be sent also [the terminal will automatically include the suitable escape sequences (ESC Gn)].
Send whole page	ESC 7	Sends all data on the page from home through the cursor position. It also sends ESC) at the start of each protected field and ESC (at the end of each protected field. If the character at the cursor position is protected, the terminal sends an ESC (to the computer. This code also sends line delimiters at the end of each line and the end-of-text characters at the end of the send transmission. If the data to be sent includes attribute characters, these will be sent also [the terminal will automatically include the suitable escape sequences (ESC Gn)].
Send unprotected message (STX to ETX)	ESC S	Sends all unprotected data bracketed by the start of text (STX) and end of text (ETX) codes displayed on a page. After the data is sent, the terminal positions the cursor at the ETX code. If the page contains no STX codes, transmission begins from the home position. If the page contains no ETX code, the terminal sends to the end of the page and positions the cursor at home after the data is sent. If the page contains neither an STX nor an ETX code, the entire page will be sent. The code sends an FS code (1C Hex) as field delimiters in place of protected fields. It also sends line delimiters at the end of each line and an end-of-text delimiter at the end of the send transmission.
Send whole message (STX to ETX)	ESC s	Same as ESC S above except protected fields delimited by start-protected field ESC (and end-protected field ESC) are also transmitted.

Data other than text may also be sent to the computer using control sequences. Pressing SEND will not send that data. The commands to transmit other-than-text data are shown in Table 4-20.

Table 4-20 Transmit Commands

Data Transmitted	Code
Terminal identification[1]	ESC M
User line[2]	ESC Z 0
Status line[2]	ESC Z 1

Notes

1. The identification will include the software level and the number of lines in its memory, followed by a carriage return. The lines of memory will be indicated by the following values:

   1 for a 24-line memory
   2 for a 48-line memory
   3 for a 96-line memory

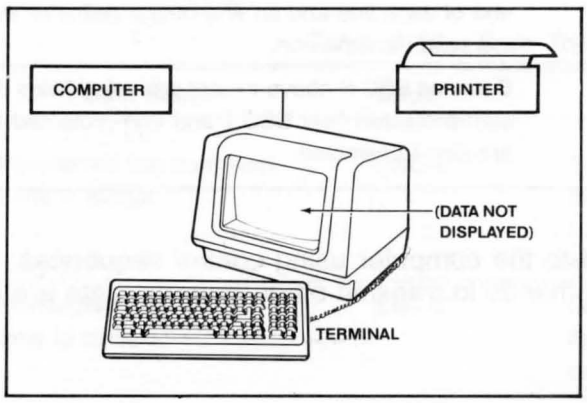
   For example, 2.0,2 CR would be sent for Level 2.0 firmware and 48 lines of memory.
2. Transmission is followed by a carriage return.

4.32 PRINT FUNCTION PROGRAMMING

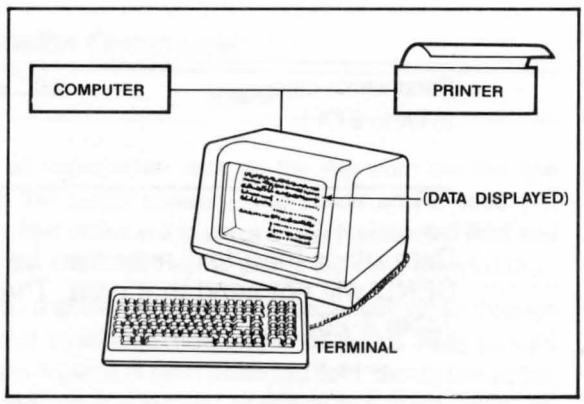
The terminal's printer port may be set for one of five types of communication:

1. Extension (copy all): All data received by the terminal is displayed and sent to the printer. (See Figure 4-3.)
2. Transparent: All data transmitted from the computer to the terminal is printed without being displayed on the screen. (See Figure 4-3.)
3. Bidirectional: Two-way communication occurs between a KSR (keyboard send/receive) printer with a keyboard and the computer.
4. Formatted page print: All data between the home position and the cursor position is sent to the printer. Each line will be terminated with a CR, LF, and null.
5. Unformatted page print: All data between home position and the cursor position is sent to the printer. No line delimiters are sent.

Table 4-21 summarizes the print controls available.



a. Transparent Mode



b. Extension Mode

Figure 4-3 Print Modes

Table 4-21 Print Controls

Name	Activated by	Prints	Status Line Shows	Buffer Action	Sends
Extension (copy all) print on	ESC @	All subsequent data received by the terminal goes to screen and continues on to the printer.	PRT 2	1	3
Extension print off	ESC A	Screen updating continues normally; any data remaining in the receive buffer continues to go to the printer until the buffer is empty.			
Buffered transparent on	ESC '	All data goes through the terminal to the printer without going to the screen.	PRT 3	2	3
Buffered transparent off	ESC a	Printing continues only until receive and print buffers are empty. Data received goes to the screen.			
Formatted page print on	ESC P or PRINT key	Data from home to cursor (not limited by the screen display if optional lines of memory have been added). Nothing typed or received from the computer goes to printer until ESC P is entered or PRINT key is pressed. Advances screen to the next page.	PRT 0	6	4, 5
Unformatted page print on	ESC L or shifted PRINT key	Data from home to cursor (not limited by the screen display if optional lines of memory have been added). Advances screen to next page.	PRT 1	6	3, 4

Notes

1. When the terminal's receive buffer contains 224 characters, the terminal sends X-Off to the computer (or if X-Off has been disabled, toggles DTR low). When the receive buffer is 20 percent empty, the terminal sends X-On to the computer (or toggles DTR high if X-Off has been disabled).
2. Data goes first to the terminal's receive buffer and then to the terminal's print buffer. When the receive buffer contains 224 characters, the terminal transmits X-Off to the computer. If X-Off has been disabled, the terminal toggles DTR low instead. The terminal will send X-On when the receive buffer is 20 percent empty.
3. All control and escape characters are transmitted. Control characters are sent with the data.
4. An ACK will be sent to the computer, indicating that all print data has been output to the printer port.
5. Each 80-character line is followed by a CR, LF, and null.
6. If the printer sends X-Off to the terminal (or toggles the DTR line), the terminal will stop sending data to the printer until the printer sends X-On or toggles the DTR line. The status line will display PBSY, indicating that the printer is busy.

Table 4-21 continued

Name	Activated by	Prints	Status Line Shows	Buffer Action	Sends
Enable bidirectional port	^R	Data from computer to printer passes through and is acted on by the terminal (i.e., keyboard lock enabled). Data can be sent from a KSR printer to the computer (passing through the terminal) but does not affect terminal (i.e., can't unlock the keyboard if it has been locked). PRINTER AND COMPUTER BAUD RATES MUST BE THE SAME.	BDIR		
Disable bidirectional port	^T	Data from computer to the terminal is not passed automatically to printer and no direct communication is possible between the computer and the device connected to the printer port.			

5. TROUBLESHOOTING AND SERVICE

This manual is written for the latest Model 950 firmware. Earlier firmware (i.e., 1.0) functions may not correspond to this manual.

5.1 CARE

Periodic cleaning and inspection will prolong the useful life of your terminal.

To clean the case:

1. Vacuum the keyboard with a soft brush or use a small soft brush.
2. Clean the housing with a soft, lint-free cloth and a commercial cleaner.

Do NOT use solvent-based or abrasive cleaners.

3. If you spill liquids on the keyboard, disassemble the keyboard and clean it with a soft cloth and water. Dry it thoroughly before re-using.

Inspect the cabinet and keyboard for damage or excessive wear periodically.

1. Inspect the cabinet for cracks or breaks. On customized units, check the bezel for paint damage (peeling, cracking, or severe scratches).
2. Check each key for free movement.
3. Inspect the cables and pin connectors twice a year for damage. Inspect the interface cable connectors for kinks or other signs of excessive stress (such as stretching).

Refer any damage to a qualified service technician.

5.2 TROUBLESHOOTING

The information provided in this section may enable you to resolve many operating problems without placing a service call.

You can run two self tests. If both tests run satisfactorily and you still have problems, consult Table 5-1.

Table 5-1 Troubleshooting Terminal Problems

Symptom	Possible Cause	Solution
Terminal dead (no beep; no cursor)	No AC power	Unplug power cord and plug in.
		Turn on power switch.
		Check power select switch.
	Fuse(s) blown	Check line and power supply fuses.
Terminal dead; cursor may appear	Loose or defective line/power supply fuses	Turn power off and change fuses.

Table 5-1 continued

Symptom	Possible Cause	Solution
Terminal will not go on line	System is not "up"	Check system status.
	Loose, unconnected, or damaged cables	Re-attach all cables; check for damage.
		Check main port (P3) interface cables:
		Pins 5, 6, and 8 must be driven by +12 VDC or not connected
		Pins 1 and 7 must be grounded
		Pin 3 must be connected to the computer transmitter; Pin 2 must be connected to the computer receiver.
	Incorrect switch settings.	Check settings.
	Modem not turned on, or defective, or phone handset upside down.	Turn on modem. Switch modems. Check handset.
Cursor will not appear.	Defective contrast pot.	Place service call.
	Contrast set too light.	Adjust contrast.
System does not respond while on line	Incorrect parity, word structure, stop bits	Set parity to match system
Terminal does not respond to switch settings	Terminal not powered down after being reconfigured; software has not scanned new settings	Turn terminal off and back on
No keyboard response	Terminal set for on line and full duplex	Set to half duplex
	Keyboard unplugged	Check keyboard connector
Terminal locked up	Keyboard disabled	Enter ESC "
	Switches set incorrectly	Review all switch settings
Terminal prints correct data only part of the time	Incorrect parity settings	Check system parity needs
	Stop bits or word structure wrong	Change switch settings
Display is wavy	Hertz setting wrong	Change power switch to match local power frequency
Printer does not print what is typed	Incorrect print mode	Check print function
	Cable connector pins connected incorrectly	Refer to Table 2-3. Pins 4 and 20 must be driven by +12 VDC or not connected; 3 must be connected to printer data input; 2 must be connected to printer data output for operation with X-On/X-Off control.
	Printer set up incorrectly	Check printer switch settings
		Check other printer port device requirements.

Table 5-1 continued

Symptom	Possible Cause	Solution
Escape and control codes do not function as expected	Incorrect escape and control codes used	Make sure upper and lower case codes are used as required. Is a numeral one being used instead of lower case "L"?
	Keyboard locked in SHIFT (AUTO LOCK on) position	Put in lower case.
		Connect P3-2 to P3-3 and try in full duplex. Disconnect computer system.

5.2.1 Testing the Terminal (Self-Test 1)

You can test the terminal yourself to verify proper operation of the video display circuitry, the transmit and receive portions of the RS232C circuitry, the character generator, and the control processor. The test will display all displayable characters and all 16 video attributes (in both half and full duplex).

To activate the self-test, follow these steps:

1. Press SHIFT and SET-UP/NO SCROLL at the same time.
2. Press 1.
3. Verify that the screen appears as shown in Figure 5-1. It should contain twenty lines with all the characters and attributes displayed. All characters should appear, and all video attributes and half-intensity characters should appear as shown. Each character should be formed properly; you should not see any extra dots and no dots should be missing.
4. If any of the video attributes or display functions are inoperative, call a qualified service technician.
5. To stop the test, press SHIFT and SET-UP/NO SCROLL again at the same time.

5.2.2 Testing the Computer and Printer Port Communications (Self Test 2)

This self test checks communications of the computer and printer ports by running four test patterns. The test patterns are:

1. 55 (16) from P3 to P4
2. AA (16) from P3 to P4
3. 55 (16) from P4 to P3
4. 2A (16) from P4 to P3

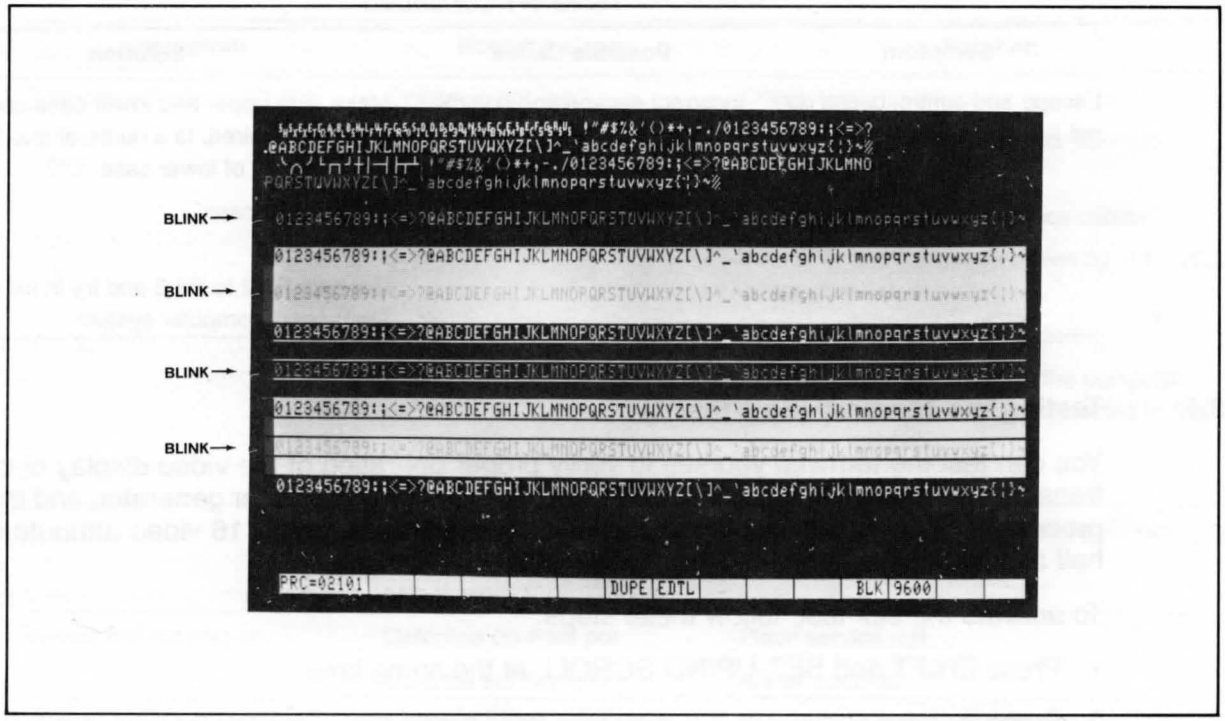


Figure 5-1 Normal Screen During Self Test 1

▲

The terminal must be set for an 8-bit data word and full or half duplex or this self test will fail.

To run this self test, follow these steps:

1. Connect P3-2 to P4-2 and P3-3 to P4-3 on the rear panel. (If necessary, use a prefabricated test cable with RS232C 25-pin male connectors at either end.)
2. Set both ports to the same baud rate (see Table 2-4b).
3. Press SHIFT and SET-UP/NO SCROLL at the same time.
4. Press 2.
5. Wait while the test runs.
6. Look for a pass or fail indicator to appear in line one on the screen. The failure indicator is FAIL n where n is the number of test(s).
7. If any of the tests fail, recheck the cable connection and the baud rates, then run the test once again.
8. If the problem persists, call a qualified service technician.
9. To stop the test, press SHIFT/SET-UP once more.

5.3 REPAIR

Operator repair is limited to changing the line fuse and the two internal power supply fuses.

5.3.1 Changing the Line Fuse

To avoid electrical shock, disconnect the terminal power cord before changing the line fuse.

1. Remove the fuse holder (see Figure 2-3) by unscrewing it counterclockwise.
2. Remove the blown fuse and replace it with a 3AB, 1 amp "slow blow" 125 VAC or 0.5 amp, 250 VAC instantaneous "fast blow" fuse for 220 VAC applications.
3. Install the fuse in the reverse order of Steps 1 and 2.
4. Plug the power cord in again.

5.3.2 Changing the Power Supply Fuses

The two terminal power supply fuses are installed in fuse clips on the power supply assembly inside the terminal (see Fig. 2-6). To replace either of these fuses, follow these steps:

Hazardous voltages are exposed in the cabinet. Turn off the power switch and disconnect power BEFORE opening the terminal cabinet.

1. Disconnect the terminal power cord from primary power.
2. Remove the four Phillips screws that hold the cabinet cover on the base and remove the cover.
3. Remove the blown fuse from its fuse clip.
4. Replace the blown fuse with a 3AG, 3 amp, 125 VAC fuse.
5. Reinstall the terminal cover and screws. (Do not overtighten the screws.)

5.4 TECHNICAL ASSISTANCE

The Service Department is open from 7:00 a.m. until 5:00 p.m., Pacific Time, Monday through Friday, except holidays. Be specific when describing the problem and failure history. Have the terminal in question by the phone before calling. If the line is busy and your problem can wait, leave a message with the TeleVideo operator and your call will be returned at our first opportunity.

5.4.1 Vital Statistics

Enter here the serial number, date received, and switch settings. This will expedite any technical conversations about your terminal.

Serial Number_____ Date Received_____

Switch Settings Used:

	Up/Down		Up/Down
S1	1____	S2	1____
	2____		2____
	3____		3____
	4____		4____
	5____		5____
	6____		6____
	7____		7____
	8____		8____
	9____		9____
	10____		10____

5.5 RESHIPPING THE TERMINAL

Should you need to reship the terminal, follow these procedures:

1. Remove the four screws on the bottom of the terminal (Figure 2-1) and lift off the top portion of the cover.
2. Check the integrity of the cabling and security of internal mounting hardware.
3. Replace the cover, being careful not to overtighten the screws.
4. Repack the terminal in the original TeleVideo shipping container or other suitable materials.

APPENDIX A MODEL 950 SPECIFICATIONS

MONITOR	
Size	12 inches measured diagonally
Phosphor	P31 green nonglare read out
CHARACTER FONT	14 × 10 dot resolution with lower case descenders
DISPLAYED CHARACTER SET	128 displayable characters: 96 character ASCII upper/lower case alphabet 32 control characters 15 special graphics characters
	24 lines (80 characters per line; 1920 characters per screen)
	Dual intensity with Protected fields Reverse video Underlined fields Blink Blank Half intensity (alone or in combination)
CURSOR ATTRIBUTES	Reverse block Blinking reverse block Undisplayed Underline Blinking underline
EDITING	Insert/delete character Insert/delete line Line/page edit Local/duplex edit
SPECIAL FEATURES	Smooth scroll/no scroll Line lock
CURSOR CONTROL	↑ , ↓ , ← , →, home, tab, back tab, return, line feed, backspace
REPEAT	20 cps auto repeat
PARITY	Even, odd, send, mark, space, or no
WORD STRUCTURE	7 or 8 data bits 10 or 11 bit word
BAUD RATES	15 switch-selectable: 50, 75, 110, 135, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19,200
TRANSMISSION	Local Block Conversation: full or half duplex (keyboard selectable)
COMMUNICATION PROTOCOL	X-On/X-Off DTR
INTERFACES	Standard RS232C point-to-point (50 ft. maximum)
PRINTER PORT	RS232C bidirectional page print buffered transparent buffered with screen copy

APPENDIX A MODEL 950 SPECIFICATIONS

POWER	
Requirements	115 VAC (60 Hertz) at 0.54 amps 230 VAC (50 Hertz) at 0.27 amps 65 watts
DIMENSIONS	
Cabinet	16.50 inches (41.9 cm) wide 14.00 inches (35.6 cm) 14.25 inches (36.2 cm)
Keyboard	16.50 inches (41.9 cm) 7.50 inches (29.0 cm) 3.00 inches (7.6 cm)
WEIGHT	
Net	Cabinet 30 lbs. (13.6 kg) Keyboard 4.5 lbs. (2.3 kg)
Shipping	44 lbs.
ENVIRONMENT	
Ventilation Requirements	4 inches minimum
Temperature	Ambient operating 32°F (0°C) to 122°F (50°C) Storage -40°F (-40°C) to 149°F (65°C)
Relative humidity	Operating 5 to 95 percent noncondensing Nonoperating no restrictions

APPENDIX B STATEMENT OF LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to Buyer that products, except software, manufactured by TeleVideo will be free from defects in material and workmanship. TeleVideo's obligations under this warranty will be limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship within 90 days after shipment by Televideo, provided that Buyer gives TeleVideo prompt notice of any defect and satisfactory proof thereof. Products may be returned by Buyer only after a Return Material Authorization number ("RMA") has been obtained from TeleVideo by telephone or in writing. Buyer will prepay all freight charges to return any products to the repair facility designated by TeleVideo and include the RMA number on the shipping container. TeleVideo will deliver replacements for defective products or parts on an exchange basis to Buyer, freight prepair to the Buyer. Products returned to TeleVideo under this warranty will become the property of TeleVideo. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof, will apply.

Exclusions

This limited warranty does *not* cover losses or damage which occurs in shipment to or from Buyer, or is due to (1) improper installation or maintenance, misuse, neglect, or any cause other than ordinary commercial or industrial application or (2) adjustment, repair or modifications by other than TeleVideo-authorized personnel or (3) improper environment, excessive or inadequate heating or air conditioning, and electrical power failures, surges or other irregularities or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors or agents, unless confirmed in writing by a TeleVideo officer.

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APPENDIX C ASCII CODE CHART

Bits 4	3	2	1	Row ↓ / Column →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
					0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN↓	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS←	CAN	(	8	H	X	h	x
1	0	0	1	9	SKIP HT	EM	)	9	I	Y	i	y
1	0	1	0	10 (a)	LF	SUB	★	:	J	Z	j	z
1	0	1	1	11 (b)	VT↑	ESC	+	;	K	[	k	{
1	1	0	0	(c)	FF→	FS	,	<	L	\	l	¦
1	1	0	1	13 (d)	CR	GS	−	=	M	]	m	}
1	1	1	0	14 (e)	SO	HOME RS	.	>	N	Λ	n	~
1	1	1	1	15 (f)	SI	NEW LINE US	/	?	O	_	o	DEL RUB

ASCII Code Table
Abbreviations For Control Characters

NUL	null	FF	form feed	CAN	cancel
SOH	start of heading	CR	carriage return	EM	end of medium
STX	start of text	SO	shift out	SUB	substitute
ETX	end of text	SI	shift in	ESC	escape
EOT	end of transmission	DLE	data link escape	FS	file separator
ENQ	enquiry	DC1	device control 1	GS	group separator
ACK	acknowledge	DC2	device control 2	RS	record separator
BEL	bell	DC3	device control 3	US	unit separator
BS	backspace	DC4	device control 4	SP	space
HT	horizontal tabulation	NAK	negative acknowledge	DEL	delete
LF	linefeed	SYN	synchronous idle		
VT	vertical tabulation	ETB	end of transmission block		

INDEX

OPERATOR'S QUICK REFERENCE GUIDE

Function	Command
MONITOR (4.2)	
Monitor mode on (transmitted)	ESC U
Monitor mode off (transmitted)	ESC X
	ESC u
USER AND STATUS LINE (4.3)	
Display user line	ESC s
Load user line	ESC f (text) CR
Display status line	ESC h
LINE LOCK (4.4)	
Enable linelock	ESC ! 1
Disable linelock	ESC ! 2
DISABLE/ENABLE KEYBOARD (4.5)	
Disable keyboard	ESC #
Enable keyboard	ESC "
CURSOR (4.6, 4.15, 4.16)	
Home	^^
New line (LF and CR)	^_
Carriage return	^M
Linefeed/cursor down	^J or ^V
Cursor up	^K or ESC j
Backspace/cursor left	^H
Cursor right	^L
Cursor off	ESC . 0
Blinking block cursor	ESC . 1
Steady block cursor	ESC . 2
Blinking underline	ESC . 3
Steady underline	ESC . 4
KEYCLICK AND BELL (4.7)	
Keyclick on	ESC >
Keyclick off	ESC <
Ring bell	^G
SMOOTH SCROLL (4.8)	
Enable smooth scroll	ESC 8
Disable smooth scroll	ESC 9
VIDEO DISPLAY (4.9)	
Screen display on	ESC n
Screen display off	ESC o

Function	Command
VISUAL ATTRIBUTES (4.10)	
Normal video (green on black)	ESC G 0
Invisible normal	ESC G 1
Blink	ESC G 2
Invisible blink	ESC G 3
Reverse video (black on green)	ESC G 4
Invisible reverse	ESC G 5
Reverse blink	ESC G 6
Invisible reverse blink	ESC G 7
Underline	ESC G 8
Invisible underline	ESC G 9
Underline blink	ESC G :
Invisible underline blink	ESC G ;
Reverse blink underline	ESC G <
Invisible reverse underline	ESC G =
Reverse blink underline	ESC G >
Invisible reverse blink underline	ESC G ?
Reverse screen background	ESC b
Normal screen background	ESC d
SPECIAL GRAPHICS (4.11)	
Special graphics on	ESC $
Special graphics off	ESC %
SCREEN MEMORY (4.12)	
Set lines per page	ESC \ n
Advance page of memory	ESC K
Print current page and view next page	ESC P ESC L
View previous page	ESC J
AUTO PAGE (4.13)	
Auto page on	ESC v
Auto page off	ESC w
PROTECT MODE (4.14)	
Half intensity (protected writing) on	ESC)
Half intensity (protected writing) off	ESC (
Protect on	ESC &
Protect off	ESC '

OPERATOR'S QUICK REFERENCE GUIDE

Function	Command
FUNCTION KEYS (4.17)	
Program function key	ESC ¦ p1 p2 (text) ^Y
ADDRESS/READ CURSOR (4.19)	
Address cursor (column, row)	ESC = r c
Address cursor (page, column, row)	ESC – p r c
Read cursor (row, column)	ESC ?
Read cursor (page, row, column)	ESC /
INSERT CHARACTER (4.20)	
Program insert character	ESC e n
TAB (4.21)	
Set typewriter (column) tab	ESC 1
Typewriter tab	^I
Field tab	ESC i
Back tab	ESC I
Clear typewriter tab	ESC 2
Clear all tabs	ESC 3
COMMUNICATION (4.22)	
Local on	ESC c
Block on	ESC B
Half duplex on	ESC D H
Full duplex on	ESC D F
Return to previous conversational mode	ESC C
EDIT KEYS (4.23)	
Local edit keys	ESC k
Duplex edit keys	ESC l
EDITING TEXT (4.24)	
Character insert	ESC Q
Character delete	ESC W
Line insert	ESC E
Line delete	ESC R
Erase line to spaces	ESC T
Erase line to nulls	ESC t
Erase screen to spaces	ESC Y
Erase screen to nulls	ESC y
Insert on	ESC q
Edit on	ESC r
Page on	ESC N
Line on	ESC O

Function	Command
CLEAR (4.25)	
Clear unprotected to insert characters	ESC + ^Z ESC ;
Clear all data to nulls	ESC *
Clear unprotected to nulls	ESC :
Clear page to half-intensity insert characters	ESC ,
X-ON/X-OFF	
Enable X-On/X-Off	^O
Disable X-On/X-Off	^N
DATA TERMINAL READY (4.27)	
Enable DTR	^N
Disable DTR	^O
USER ROM (4.28)	
Execute ROM program	ESC z p
COMPUTER AND PRINTER PORTS (4.29, 4.30)	
Configure computer port	ESC { p1 p2 p3 p4
Configure printer port	ESC } p1 p2 p3 p4
SEND KEY (4.31)	
Load SEND key	ESC 0 x y
Set send delimiters	ESC x n p1 p2
Send unprotected line to cursor	ESC 4
Send unprotected page to cursor	ESC 5
Send line to cursor	ESC 6
Send page to cursor	ESC 7
Send unprotected message	ESC S
Send entire message	ESC s
Send terminal identification	ESC M
Send status line	ESC Z 1
Send user line	ESC Z 0
PRINT KEY (4.32)	
Extension print on	ESC @
Extension off	ESC A
Buffered transparent print on	ESC '
Buffered transparent print off	ESC a
Formatted page print on	ESC P
Unformatted page print on	ESC L
Bidirectional printer port on	^R
Bidirectional printer port off	^T

TeleVideo® Model 950

OPERATOR'S QUICK REFERENCE GUIDE

Function	Command
FUNCTION KEYS (4.17)	
Program function key	ESC ¦ p1 p2 (text) ^Y
ADDRESS/READ CURSOR (4.19)	
Address cursor (column, row)	ESC = r c
Address cursor (page, column, row)	ESC - p r c
Read cursor (row, column)	ESC ?
Read cursor (page, row, column)	ESC
INSERT CHARACTER (4.20)	
Program insert character	ESC e n
TAB (4.21)	
Set typewriter (column) tab	ESC 1
Typewriter tab	^I
Field tab	ESC i
Back tab	ESC I
Clear typewriter tab	ESC 2
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Local on	ESC c
Block on	ESC B
Half duplex on	ESC D H
Full duplex on	ESC D F
Return to previous conversational mode	ESC C
EDIT KEYS (4.23)	
Local edit keys	ESC k
Duplex edit keys	ESC l
EDITING TEXT (4.24)	
Character insert	ESC Q
Character delete	ESC W
Line insert	ESC E
Line delete	ESC R
Erase line to spaces	ESC T
Erase line to nulls	ESC t
Erase screen to spaces	ESC Y
Erase screen to nulls	ESC y
Insert on	ESC q
Edit on	ESC r
Page on	ESC N
Line on	ESC O

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Clear unprotected to nulls	ESC :
Clear page to half-intensity insert characters	ESC .
X-ON/X-OFF	
Enable X-On X-Off	^O
Disable X-On X-Off	^N
DATA TERMINAL READY (4.27)	
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Send unprotected page to cursor	ESC 5
Send line to cursor	ESC 6
Send page to cursor	ESC 7
Send unprotected message	ESC S
Send entire message	ESC s
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Send user line	ESC Z 0
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Bidirectional printer port off	^T

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Disable linelock	ESC ! 2
DISABLE ENABLE KEYBOARD (4.5)	
Disable keyboard	ESC #
Enable keyboard	ESC "
CURSOR (4.6. 4.15. 4.16)	
Home	^^
New line (LF and CR)	^_
Carriage return	^M
Linefeed cursor down	^J or ^V
Cursor up	^K or ESC j
Backspace cursor left	^H
Cursor right	^L
Cursor off	ESC . 0
Blinking block cursor	ESC . 1
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Steady underline	ESC . 4
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Keyclick on	ESC @
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Ring bell	^G
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Reverse blink	ESC G 6
Invisible reverse blink	ESC G 7
Underline	ESC G 8
Invisible underline	ESC G 9
Underline blink	ESC G :
Invisible underline blink	ESC G ;
Reverse blink underline	ESC G <
Invisible reverse underline	ESC G =
Reverse blink underline	ESC G >
Invisible reverse blink underline	ESC G ?
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Advance page of memory	ESC K
Print current page and view next page	ESC P ESC L
View previous page	ESC J
AUTO PAGE (4.13)	
Auto page on	ESC v
Auto page off	ESC w
PROTECT MODE (4.14)	
Half intensity (protected writing) on	ESC)
Half intensity (protected writing) off	ESC (
Protect on	ESC &
Protect off	ESC '

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No. 300002-001 Revision B JKH

950 THEORY OF OPERATION

TTL

SECTION

MAIN LOGIC BOARD

KEYBOARD

MAIN LOGIC BOARD

4.1

Overview

Please refer to figures 1, 2, 3, and 4 of the block diagrams as you read the text that follows.

Figure 1 shows the power-on reset, which is controlled by A17. During power-up, this chip sends the signals necessary to reset the CPU and to perform the initial diagnostic routine. This routine reads the switches in the back of the terminal and configures it for the proper handshaking protocol.

The 950's CPU is a 6502, located at A53.

The Shift clock (OSC1) generates the timing for the 950's logic system. The Stretch clock functions as the main clock for the CPU. Other clock circuits include the Crystal clock to the UARTs, the Shift clock, the DC Carry clock, the C clock, and the QC clock.

The CPU's address bus (6502 bus) addresses the ROM chips (A41 and A42).

The ROMs contain the operating instructions, the power-up diagnostics, and the other intructions necessary to operate the terminal. Most systems only use two ROMs, but the 950 contains an additional, optional ROM (A52).

The decoding gates (A58 and A63) select one of the three ROMs. The other decoder (A62) selects either the DISP.MEM (display memory) or the IOP.SEL (input/output select) signal.

The auxiliary chip in this figure (6522) reads switches (S1 and S2), and generates the control signals for the video attributes and the bell, as well as several auxiliary control signals used to address the display RAM.

In figure 2 of the block diagram, note the continuation of the 6502 and the 6522.

The CRT controller chip (CRTC 6545) generates the signals necessary to control the monitor portion of the terminal. It outputs three primary signals: horizontal synch, vertical synch, and cursor. These signals go to the video module.

The display RAMs are addressed by the 14 address bits coming from the CPU bus, as well as the memory address bits from the CRTC.

The multiplexers in the center of the figure (A43 through A46) alternately select whether the CPU or the CRTC is permitted to address the system and the display RAMs (A25 through A28, A34 through A37).

The Phase clock controls this process. During one phase of the clock the CPU can address RAM. During the other phase, this multiplexer allows the CRTC to address RAM.

When the CPU addresses the system display RAMs, the bidirectional latch at A14 is enabled to either input or output data from the system RAMs. When the CRT controller addresses the RAMs, the latch at A24 holds the display data.

Normally, the outputs of the CRTC would be used for scrolling. However, since the 950 has a smooth scroll option, the output of the counter latches at the bottom of figure 2 (A60 and A61) are used to scroll. The CPU controls these latches through the decoder at A62.

In figure 3 of the block diagrams, the row address signals coming from these counter latches (A60 and A61) and the display data from the latch above it (A24) are used to address the character-generator ROMs (A32 and A33). The character-generator ROMs then output 14 bits to a parallel-to-serial shift register.

The DC.Carry signal loads these 14 bits at the shift register (A22 and A23), and the shift clock shifts the data into the video logic and the drivers as a serial data stream.

The eight bits of display data from latch A24, as well as one bit from the character generator ROMs, address the attribute registers.

The attribute registers' output also addresses the video logic and drivers, as do the video attribute signals sent by 6522. These signals (dark on light, cursor, force blank, blink rate, and maximum intensity) control the video attributes through the video logic and drivers. Note that, in the 950, the maximum intensity signal (MI) is standard. To highlight, the 950 uses half intensity. The output is routed to the video module.

The XTAL1 clock (clock source) controls the three UARTs on figure 4 of the block diagrams.

A49 receives data from the keyboard.
A50 receives and transmits data for the main port (P3).
A51 receives and transmits data for the printer port (P4).

4.2

CPU Timing and Control

A 23.814 MHz. oscillator (OSC 1, sheet 6) generates the timing for the 950's entire internal logic system. Known as the Shift (or dot) clock, it drives the two shift registers (A22 and A23). These registers bring in parallel data and shift it out as serial dot data.

The active low* shift clock is gated with the terminal count output of the C.clock (Character clock) counter. Together they drive a latch (A24, sheet 4) that holds data from character addresses 0 through 7, as well as the flip-flop (A31, sheet 4) that controls the DEL CURSOR signal.

A 4-bit binary counter (A3, sheet 6) divides the shift clock's rate by 14, creating eight 1.701 mHz clocks.

The C.clock, which is the time base for character generation, drives the CRT chip (6545, sheet 2). The active low C.clock has two purposes. It drives the Hex D flip-flops (A64 and A71) that time the CRTC RESET. It also controls the Stretch clock, which generates clock periods twice the normal length (1175ns vs. 588ns) upon command from the CPU.

This circuit (sheet 6) accesses slower memory or peripheral devices. The final output (called "00" or "Phase Zero clock") goes to the 6502 and all the peripheral chips. The Phase Zero clock controls the CPU bus timing, and it triggers all data transfers between the CPU and the other internal processors.

The DC.carry signals function as two clocks. The active high DC.Carry clock drives a flip-flop (A19, sheet 4) that is part of the video attribute circuitry. The active low DC.Carry clock is connected to the LD or Shift/Load enable lines (A22 and A23, pin 15, sheet 4) of two parallel-to-serial shift registers (A22 and A23). These registers are part of the characacter generation circuitry.

The XTAL1 clock drives UARTs A49, A50, and A51, which interface data to and from the terminal.

The QC clock combines with three RAM address lines (A15, sheet 3) to form a 1-of-10 decoder. The decoder's output goes to the chip select lines of each system RAM and each page of memory. The QC clock also deselects the RAM chips while the address lines are settling.

Line lock and smooth scroll are two 950 features not normally attainable with the 6545 CRT controller. To use them, additional circuity is required.

*The active low state is indicated by a bar above the signal name.

To achieve line lock, the top of the 6545's display register must be reloaded at the beginning of each character row. A general description of this circuitry follows.

To achieve smooth scroll, a CPU-loadable count-up counter (A60, sheet 4) must replace the 6545's internal scan line counter.

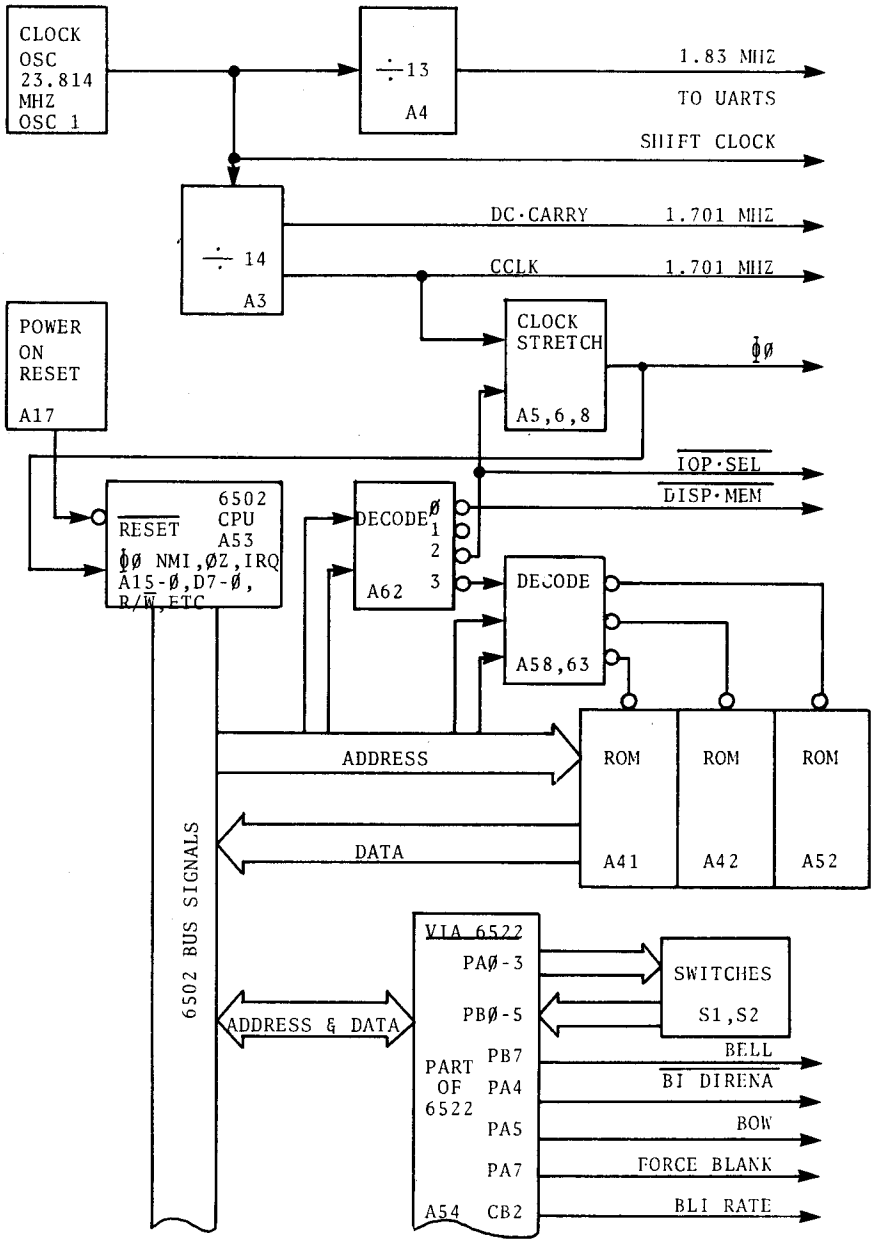


Figure 1 CPU, Timing, and Control

4.3

Display Controller

The 6545 (A55) generates each character's memory address in the display RAMS (A25 through A28) as it is to be displayed. It also generates the horizontal and vertical synchronization (synch) pulses necessary to control the deflection circuits of the monitor (CRT).

Note! In the text that follows, the term "scan line" refers to one of ten scan lines created by the electron beam, which makes up one data row.

The 6522's timer (T2) counts horizontal scan lines. When a specified number of scans have been executed, it interrupts the CPU (6502) with the NMI-interrupt. The CPU then loads the memory address of the next data row into the CRT controller (6545).

At the same time the NMI-interrupt is issued to the CPU, the CRTC reset timer (A64 and A71, sheet 7) is cleared, causing it to reset. The reset is released after seven C.CLK periods, and the CRTC starts timing the next character row. This operation allows the CPU to determine the order of the display lines so that some lines can be locked while others scroll.

To achieve a smooth scrolling effect, the number of scan lines in the character row and the starting scan line of each row must be specified.

The 6522's timer, which counts horizontal synch pulses, specifies the number of scan lines in the present character row. Normally, ten lines are used when smooth scroll is disabled. During a smooth scroll, this number ranges between 1 and 10 on the top and bottom rows.

To do this, the processor loads a 4-bit value into a latch (A61, sheet 4). When the CRTC is reset, this value is transferred to the counter (A60, sheet 4) and becomes the first scan line of the next data line. Each horizontal synch pulse then increases this value until the start of the next data line. At that point, it is preset again to a value determined by the CPU.

The CPU and the display controller share access to the system and display RAM during the alternate phase of the 6502's Phase 2 clock.

During the positive portion of the Phase 2 clock, the CPU address can be gated onto the RAM address bus through multiplexers (A43 through A46, sheet 2). A bidirectional transceiver (A14, sheet 3) passes data between the CPU data bus and the RAM data bus.

During the negative portion of the Phase 2 clock, the 6545 address bus (A55) is gated onto the RAM address bus, allowing the video data to be loaded into a latch (A24, sheet 4). This address becomes the input for the character generators and the attribute generation circuitry.

This alternating ("interleaved") access allows the processor to operate at normal speed without interruption or degradation of the display quality (which could be caused by accidental appropriation of the display bus by the processor as it accesses data).

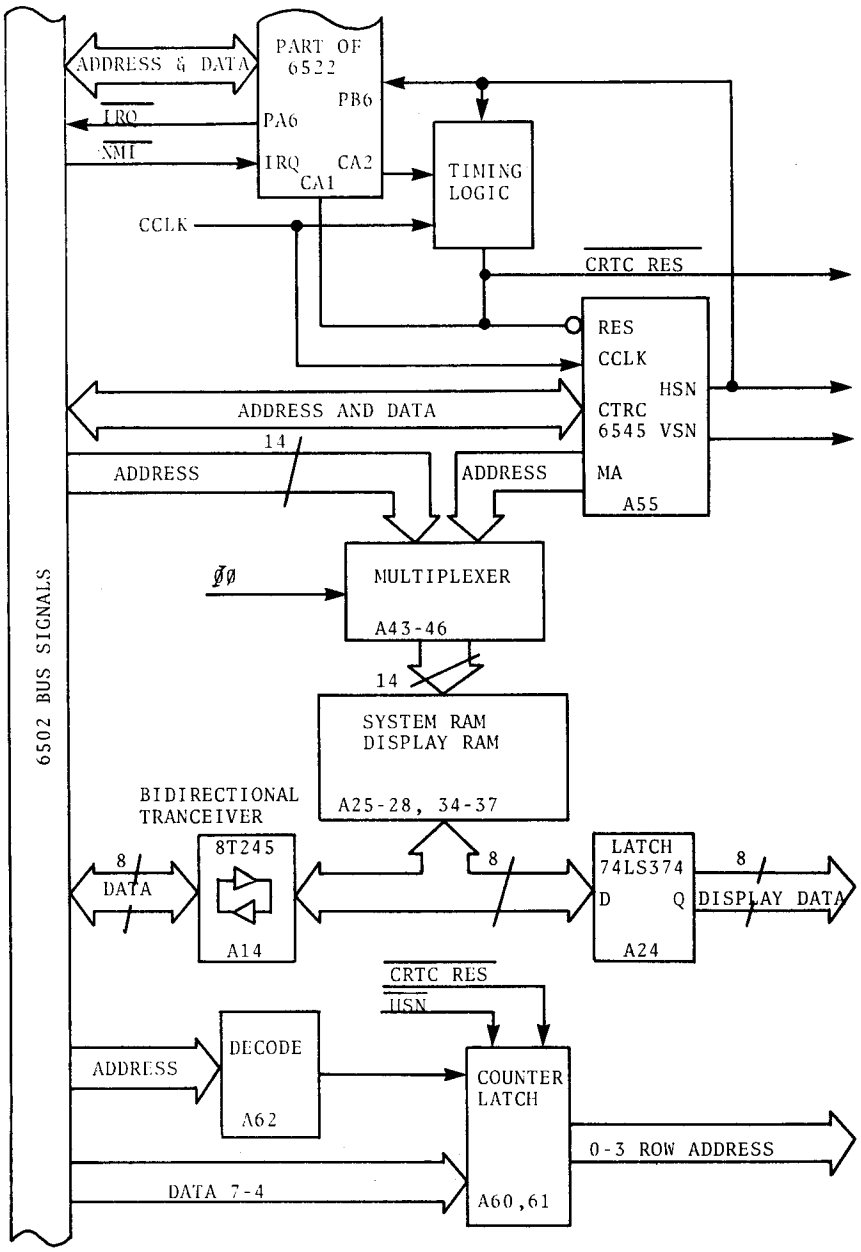


Figure 2 Display Controller

4.4

Video and Character Generation

To create the 950's display, the CRT scans horizontally from left to right, and vertically from top to bottom. Depending on the terminal's Hertz setting, the scan consists of 250 horizontal scan lines, each repeated 50 or 60 times per second. Each scan line displays 80 sections of 14-dot pixels. Each character line contains ten horizontal scan lines. This makes each character cell 14 pixels wide by 10 pixels high.

Characters are formed when the electron beam turns on individual pixels. The CRTC "MA" lines access the display memory once each character time (14 dot clocks). Once each cycle, the data from the display memory is then latched by the character address latch (A24, sheet 4). The output from this latch drives the eight most significant address lines of the character generator ROMs (A32 and A33, sheet 4).

The scan-line counter controls the four least significant address lines of the character generators. The scan-line counter's output changes only at the end of the scan line, when horizontal synch goes high.

The character generator's output is a 14-bit word that represents the pixel pattern to be displayed. The Shift clock loads this word into a 14-bit parallel-in/serial-out shift register (A22 and A23, sheet 4), and shifts it out, one bit at a time.

Thus, as the present pixel pattern of one character is loaded, the character address of the next character is latched. The bits shifted out of the shift register are mixed with display enable and the cursor and attribute data, creating the video output to the monitor. This signal turns the CRT's electron beam on and off as the beam sweeps the raster.

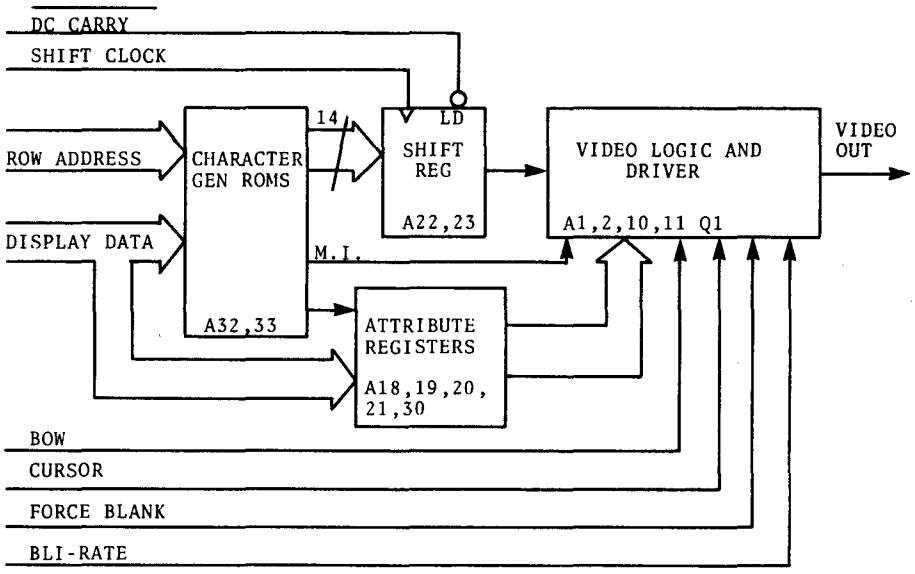


Figure 3 Video and Character Generation

4.5

Visual Attributes

The 950 has five visual attributes: half intensity, blink, blank, underline, and reverse video.

The only attribute created on a character-by-character basis is half intensity. All other attributes are "field" attributes; i.e. they have a specified starting and ending point. All characters between these points are affected by the attribute selected.

In the 950, attributes are stored in the display RAM just like displayed characters. An attribute character occupies a character space on the screen and is displayed as a half intensity space. The attribute becomes active immediately to the right of that space and remains in effect until the end of the screen.

Since an attribute is stored as a character in the display RAM, the character generation logic processes it as though it were a displayed character. However, the byte stored in RAM for an attribute character differs from that for a display character in that bits 4 and 7 are always set, while bits 5 and 6 are always reset.

Bits 0 through 3 define the active attribute. When the low-order character generator ROM (A33, sheet 4) is accessed by these codes (90 through 9F), the resulting data bit (A33, pin 17) is output as a high.

A21's data input comes from the output of a four-channel, two-to-one multiplexer (A20). While nonattribute characters are displayed, the multiplexer is driven by the output of A19. During an attribute character time, the output of Nand gate A11 is low, and it selects the A input to the multiplexer. This input connects with the output of the And gates that compare the previous attributes (output of A21) to the new attributes (output of A24).

If the previous attribute bit and the corresponding bit of the new attribute are both high, the output of the And gate is high. If one or both are low, the ouptut of the And gate is low and the attribute is turned off.

Thus, if an attribute is true for both the previous attribute and the new attribute, it is true while the new attribute is displayed on the screen. Otherwise, it turns off when the new attribute character starts.

The 950's attributes continue from character line to character line. Since any attribute on the previous line must be displayed on the current line until a new attribute is found, the logic must remember the last attribute of the previous line.

To summarize, A21's output is used by the video logic to turn visual attributes on or off. Its input can come from two sources: the output of the AND gates and the output of A19.

The output of the And gates defines the attribute(s) to be displayed during the attribute character, while A19's output determines the attribute(s) to be displayed during a nonattribute character.

A19's output is set to equal the previous character line's attribute until a new attribute is encountered. At that time, the output changes to the new attribute. A18 is used to remember the last attribute of a character in any character line.

Since each character line contains ten scan lines, the attribute data changes ten times. At the end of the displayed portion of each scan line, the Display Enable signal changes from high to low. This signal is then inverted and fed into a two-input Nand gate with the Delayed Display Enable signal, which changes one character time after Display Enable. Both signals are high only during the 81st character time of each scan line, creating a low pulse on the output of the Nand gate (A13 and A11). This pulse enables the output of a tri-state latch (A18).

A18's input comes from A20 and is latched only during the last scan line of the character row (pin 9, clock enable). This "remembers" the last attribute data of any character line. A18's output is latched into A19 at the end of the displayed portion of each scan line. A19's output then defines the attribute to be displayed during the current nonattribute character time.

The signals for Delayed Display Enable, Delayed Cursor, Dot Serial, Bow, Force Blank, and Visual Attribute Data are combined on sheet 6. They are gated together through A1, A9, A10, and A11, and are amplified to proper voltage and current levels by an NPN transistor Q1 (sheet 6). This transistor drives the video signal to the video module and/or external monitor (i.e. composite video).

4.6

Input/Output Circuits

Each of the three peripheral ports is controlled by a seperate 6551 UART.

UART A50 receives and transmits data for the main port (P3)
UART A51 receives and transmits data for the printer port (P4)
UART A49 receives data from the keyboard

The UARTs receive serial data, convert it to parallel data, and tie it directly to the CPU's data bus with input drivers, receivers, and switching circuits (A39, 40, 47, 48, 56, 57, 58, 50, sheet 5).

The use of seperate UARTs for the P3 and P4 ports allows the setting of different baud rates for each port.

The 1489 quadruple input line receivers (A57 and A40) convert RS232C voltage levels to TTL voltage levels. The 1488 quadruple output line drivers (A48 and A39) convert TTL voltage levels to RS232C voltage levels.

The output of A59, a quadruple 2-to-1 multiplexer, selects the output line drivers. A59 can select between two inputs (A or B), and route it to its respective outputs.

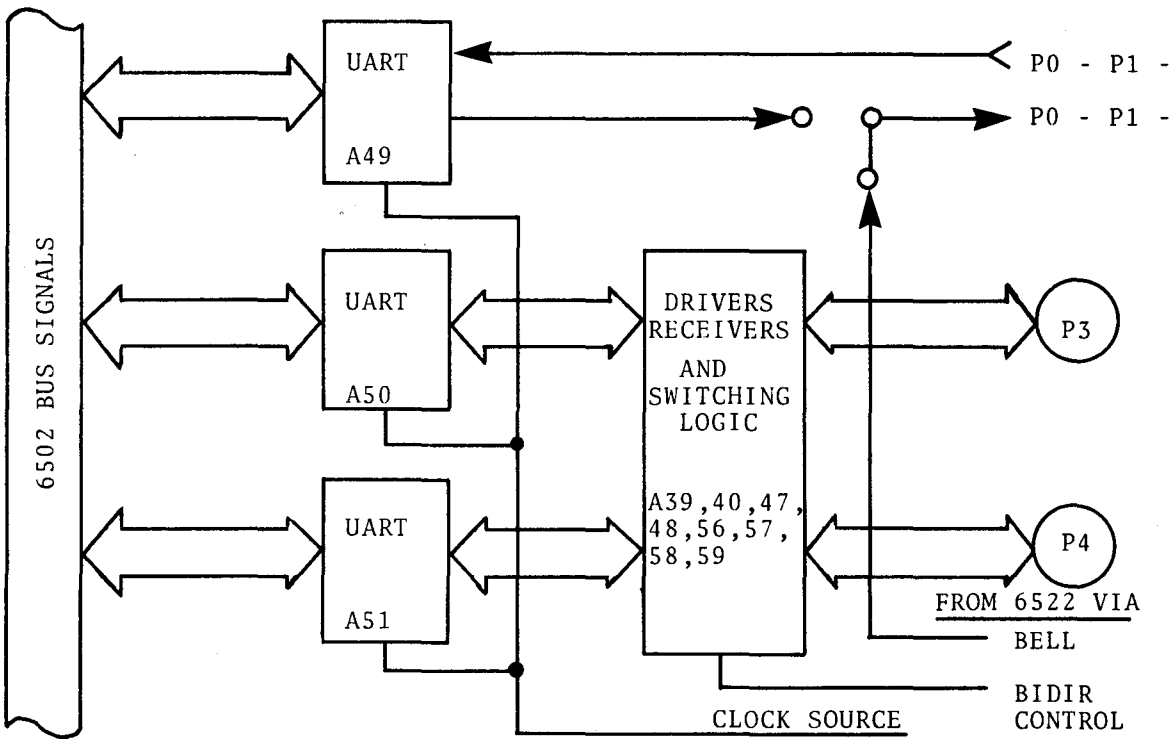


Figure 4 I/O Circuits

KEYBOARD

4.7

Overview

The 950 contains a microprocessor-based keyboard. The firmware monitors keyboard scanning, return-line testing, and communication with the control board.

In addition to the standard keyboard, additional parts let you create a keyboard that allows new key codes to be programmed into the keyboard PROM (2716).

Standard Keyboard (Version 1)

- Requires 5 volts (typical input current = 80 milliamps)
- 8048 microprocessor
- 1k byte ROM capacity (internal to the 8048)
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

Version 2 Keyboard with EPROM

- Requires 5 volts (typical input current = 150 milliamps) .
- 8035 microprocessor
- 2K x 8 byte EPROM 2716 (external to 8035)
- Status display - 8 LED display
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

The Version 2 keyboard with the 2716 EPROM requires a larger memory map and storage capability in the microprocessor. Therefore, you must also change the standard 1K x 8B 8048 microprocessor to a 2K x 8B 8035.

To install it, cut jumpers A through M on the circuit side of the logic board and install the following components in the appropriate locations.

Components

U2,U3	74LS367
U4	75L5373
U5	EPROM (2716)
U7	74LS05
C2,C3	{.01uf cap}
C4,C5	{10% 50V}
R2	1K 5% 1/4 watt

4.8

Keyboard Layout

The keyboard contains 101 keys on a PC board, as shown in Figures 5-A and 5-B.

The key switches are arranged in an X-Y matrix (Figure 6). Only four special keys (CTRL, SHIFT, FUNCT, and ALPHA LOCK) are not included in the X-Y matrix.

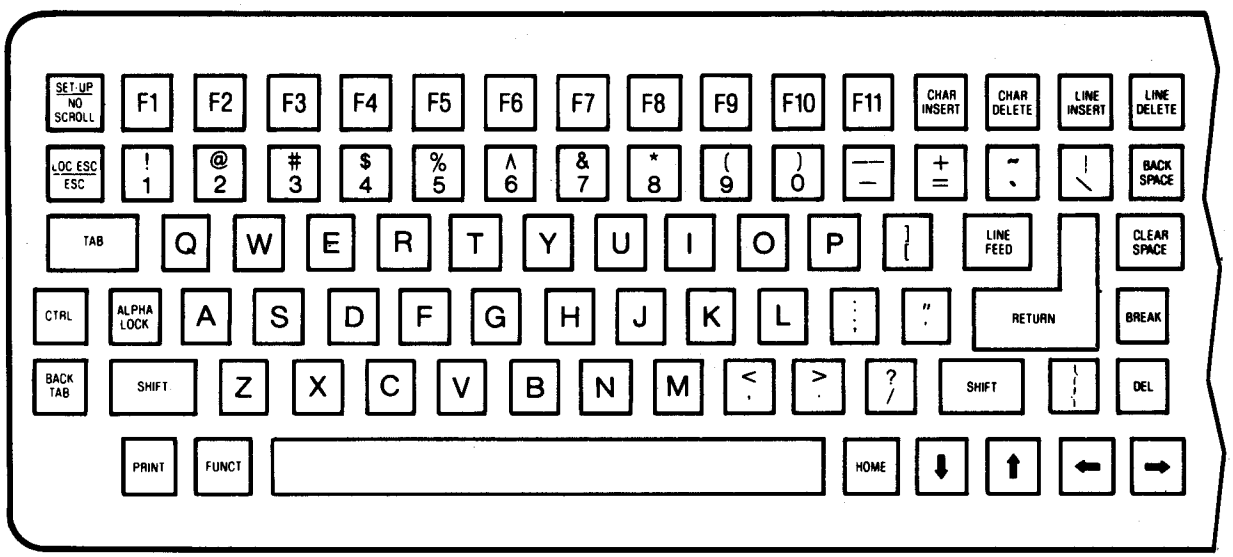


Figure 5-A Keyboard Layout

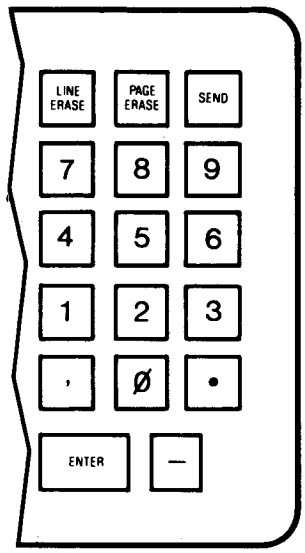


Figure 5-B
Keypad Layout

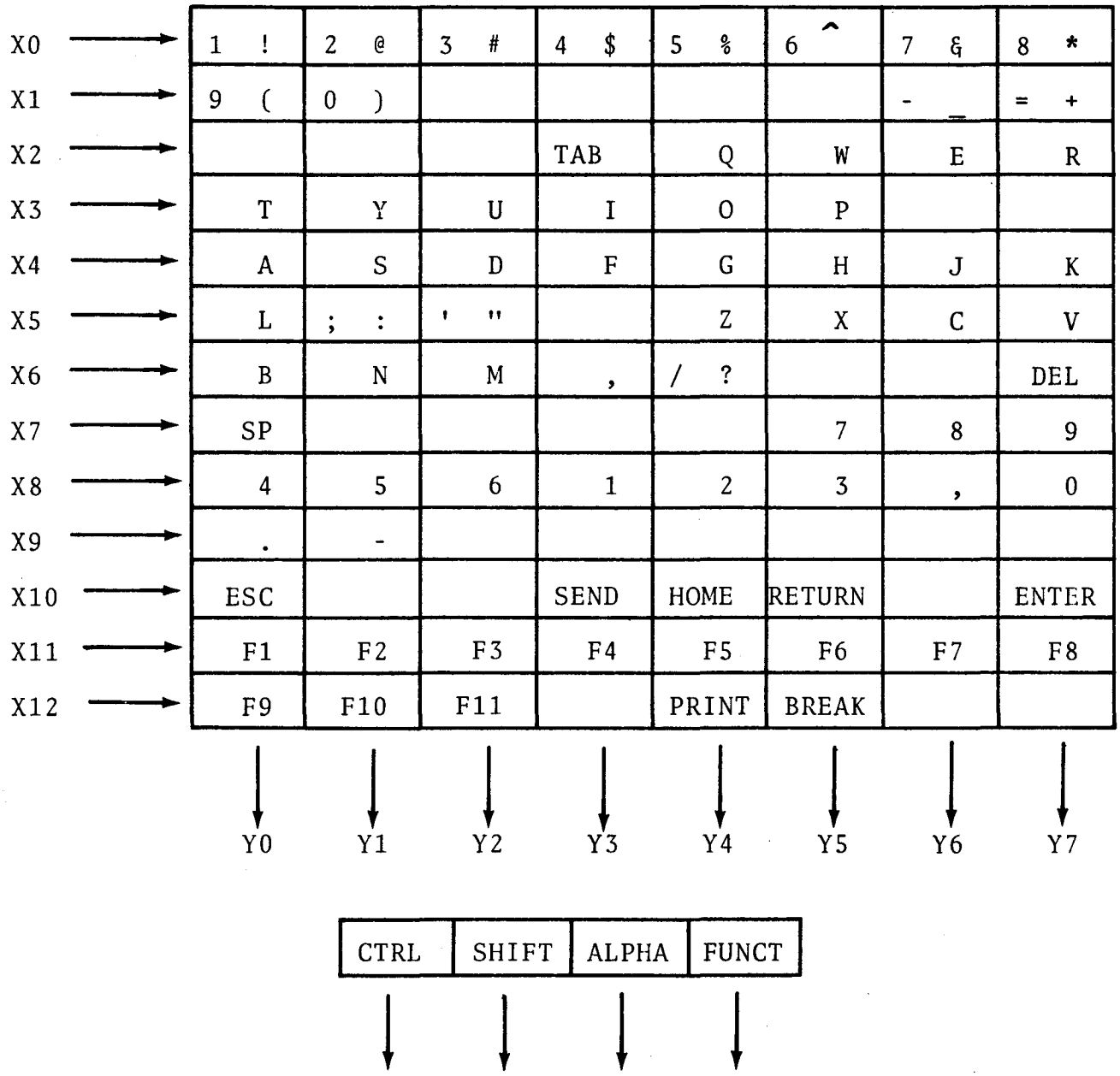


Figure 6 Keyboard X-Y Matrix Arrangement

4.9

Keyboard Interface

Communication between the main control board and the keyboard controller is asynchronous. The standard asynchronous format used by the 950 (Figure 9) consists of one start bit, eight data bits, and one stop bit. The baud rate is set to 1200 bits/sec.

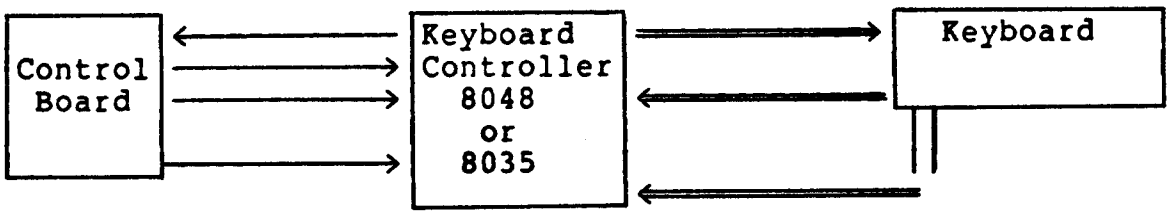


Figure 7 Keyboard Interface

4.10

Keyboard Scanning Method

The keyboard microprocessor (8048 or 8035) drives the scan lines (X lines), one at a time, to a low voltage. The return lines (Y lines) are tested by the microprocessor.

The keyboard matrix output ports (10 through 14, 20 through 27) latch the X0 through X12 lines to the keyboard. The connections are shown in Figure 7.

Whenever a low voltage is detected on a Y input line, it means that a key has been depressed. That key is at the intersection of the driven line (X) and the detected line (Y).

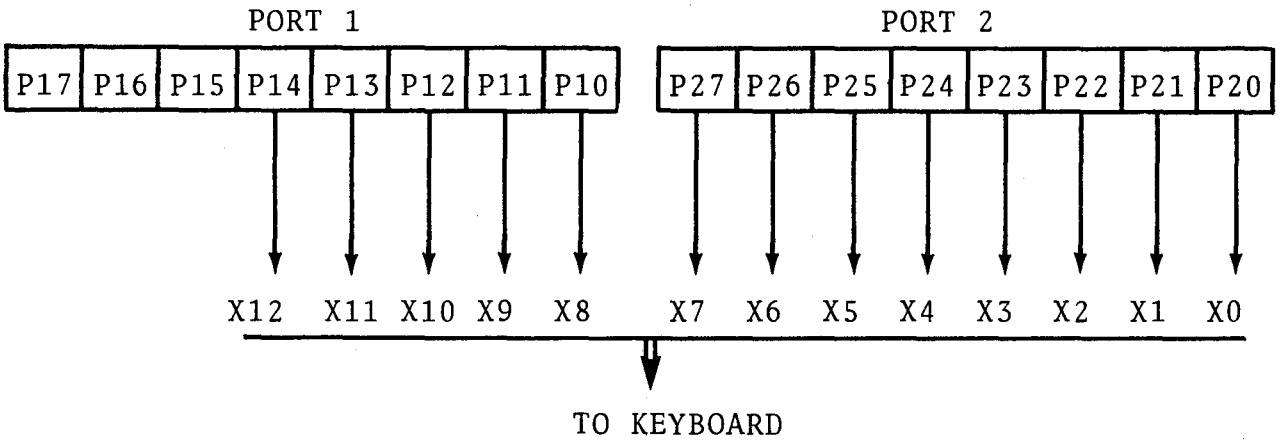


Figure 8 8048 Ports

The return matrix lines (Y lines) from the keyboard are read by the microprocessor's data bus (D0 through D7). The connections are shown in Figure 8.

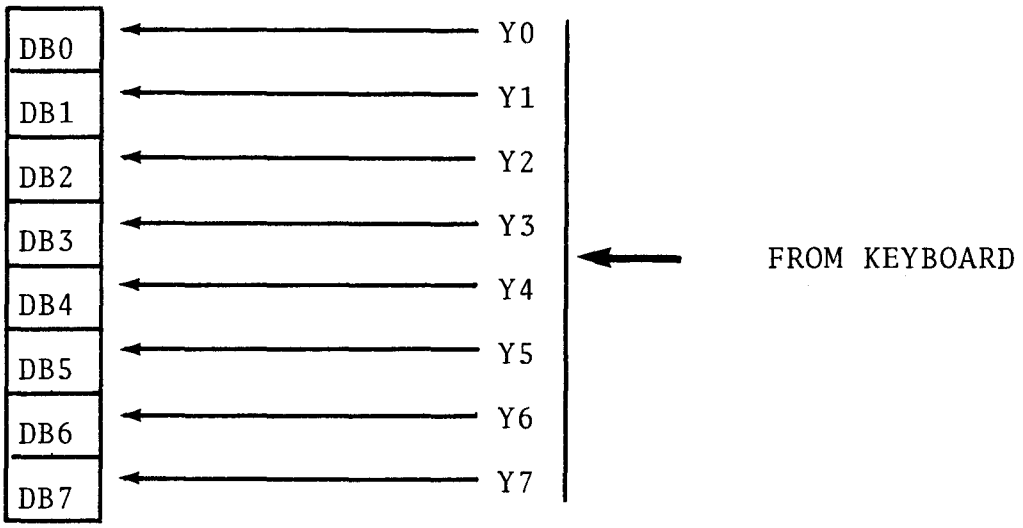


Figure 9 8048 Data Bus

Basic Scan Routine

Starting the scan routine resets the transmit flag and enables the external interrupt for receiving status from the control board.

The keyboard matrix is scanned from the top row to the bottom row. As soon as a key is pressed, the row is tested bit by bit, from left to right. The matrix key codes are immediately encoded and stored in two registers (NEWKY 1 and NEWKY 2).

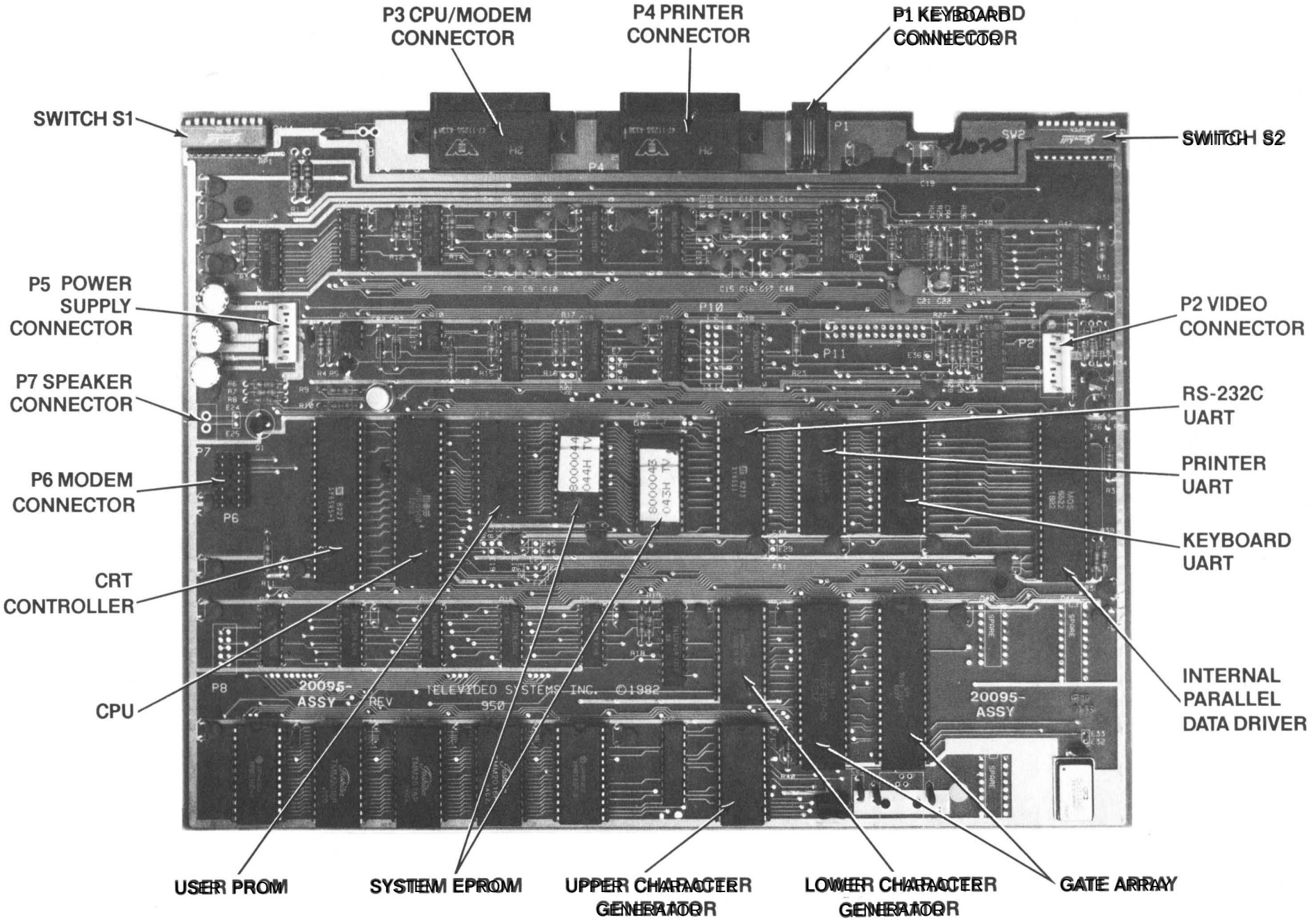
If the results of a matrix scan indicate that more than two keys are depressed, the program enters a delay loop for 11 ms. Meanwhile, the whole matrix is read once again to verify that the key is still depressed. After the key is proven to be valid, the microprocessor sends the proper code to the terminal.

If the depressed key is a repeat key, the last portion of the scan routine controls the length of the repeat delay (0.5 sec.) and the autorepeat rate (16 char/sec.). The program then branches back to the beginning of the scan routine.

950 GATE ARRAY LOGIC BOARD

Newer model 950 terminals have a green gate array logic board instead of the blue TTL logic board found in older versions. The logic and control signals are the same on both boards. However, on the gate array board, the logic gates have been incorporated into one integral semi-custom IC, referred to as the gate array chip. This substantially reduces the number of chips on the logic board and makes it simpler to troubleshoot to the component and signal level.

The corresponding logic schematic in this manual for the 950 gate array board is labeled **950 G/A**.



Gate Array Board

DOCUMENT NO. 29000 D39
REV. 3, FEBRUARY 1979

PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX _ _ _

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concerning availability.

R6500 MICROPROCESSORS (CPU's)

Specifications subject to change without notice

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

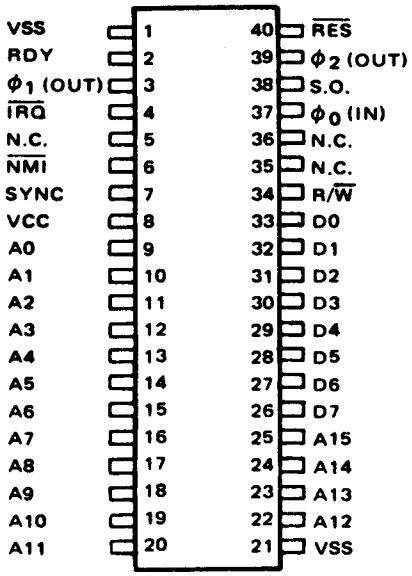
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z PAGE. X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V - B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V . . . . Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N . . . . . Z .	AND
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N . . . . . Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							. . . . .	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							. . . . .	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							. . . . .	BEQ
BIT	A∧M				2C	4	3	24	3	2																															M, M_6 . . . . Z .	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							. . . . .	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							. . . . .	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							. . . . .	BPL
BRK	BREAK													00	7	1																									. . . 1 . 1 . .	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							. . . . .	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							. . . . .	BVS
CLC	0 → C													18	2	1																									 0	CLC
CLD	0 → D													D8	2	1																									. . . . 0 . .	CLD
CLI	0 → I													58	2	1																									. . . . . 0 . .	CLI
CLV	0 → V													B8	2	1																									. 0	CLV
CMP	A - M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N . . . . . Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																															N . . . . . Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																															N . . . . . Z C	CPY
DEC	M - 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N . . . . . Z .	DEC
DEX	X - 1 → X													CA	2	1																									N . . . . . Z .	DEX
DEY	Y - 1 → Y													88	2	1																									N . . . . . Z .	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N . . . . . Z .	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N . . . . . Z .	INC
INX	X + 1 → X													E8	2	1																									N . . . . . Z .	INX
INY	Y + 1 → Y													C8	2	1																									N . . . . . Z .	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				. . . . .	JMP
JSR	JUMP SUB				20	6	3																																		. . . . .	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N . . . . . Z .	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N . . . . . Z .	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N . . . . . Z .	LDY
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 . . . . . Z C	LSR
NOP	NO OPERATION													EA	2	1																									. . . . .	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N . . . . . Z .	ORA
PHA	A → Ms S - 1 → S													48	3	1																									. . . . .	PHA
PHP	P → Ms S - 1 → S													08	3	1																									. . . . .	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N . . . . . Z .	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[C] ← [7 6 5 4 3 2 1 0]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N . . . . . Z C	ROL
ROR	[C] → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N . . . . . Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									. . . . .	RTS
SBC	A - M - $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V . . . . Z (3)	SBC
SEC	1 → C													38	2	1																									 1	SEC
SED	1 → D													F8	2	1																									. . . . 1 . .	SED
SEI	1 → I													78	2	1																									. . . . 1 . .	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										. . . . .	STA
STX	X → M				8E	4	3	86	3	2																													96	4	2	. . . . .	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	. . . . .	STY
TAX	A → X													AA	2	1																									N . . . . . Z .	TAX
TAY	A → Y													A8	2	1																									N . . . . . Z .	TAY
TSX	S → X													BA	2	1																									N . . . . . Z .	TSX
TXA	X → A													8A	2	1																									N . . . . . Z .	TXA
TXS	X → S													9A	2	1																									. . . . .	TXS
TYA	Y → A													98	2	1																									N . . . . . Z .	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

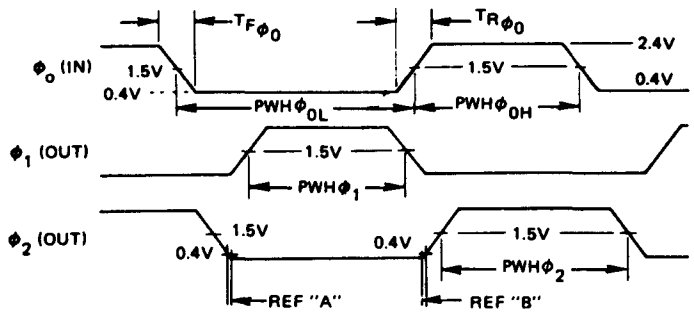
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

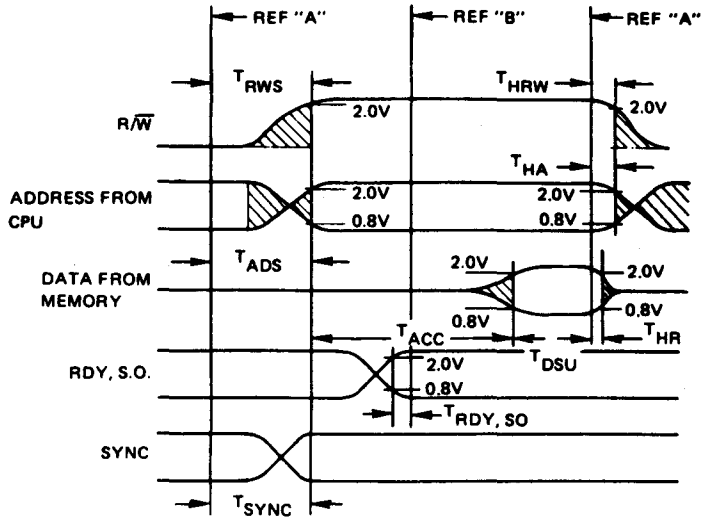
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M7	MEMORY BIT 7
Y	INDEX Y	-	SUBTRACT	M6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR		

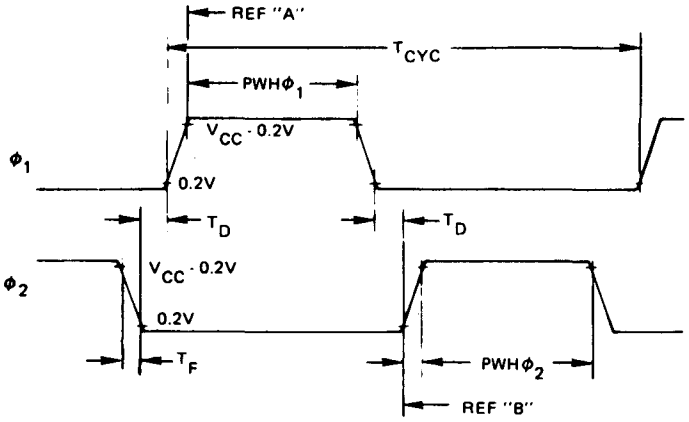
Clock Timing – R6502, 03, 04, 05, 06, 07



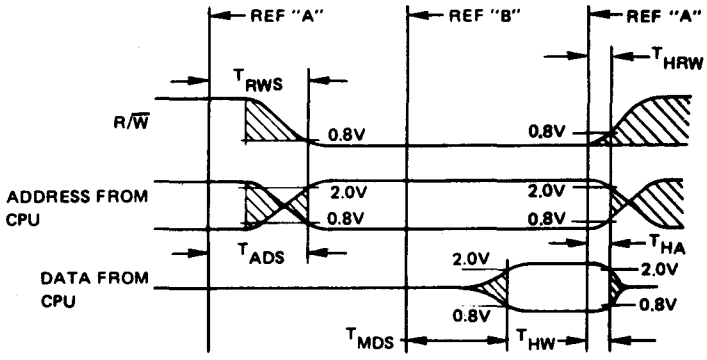
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

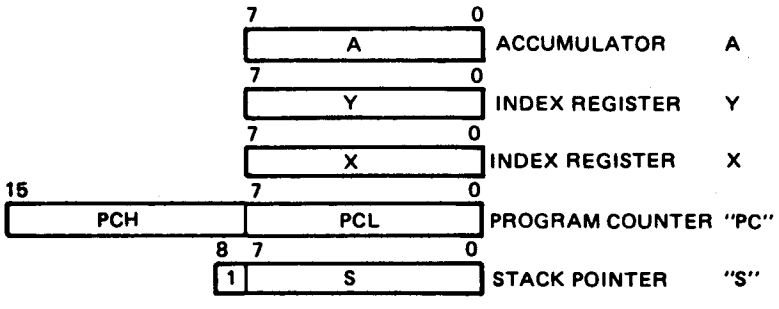


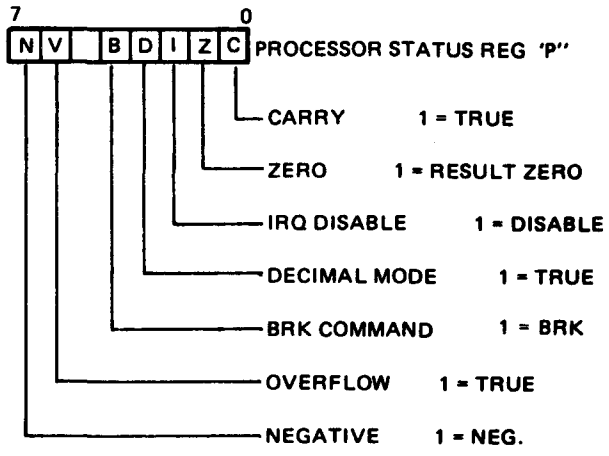
Timing for Writing Data to Memory or Peripherals

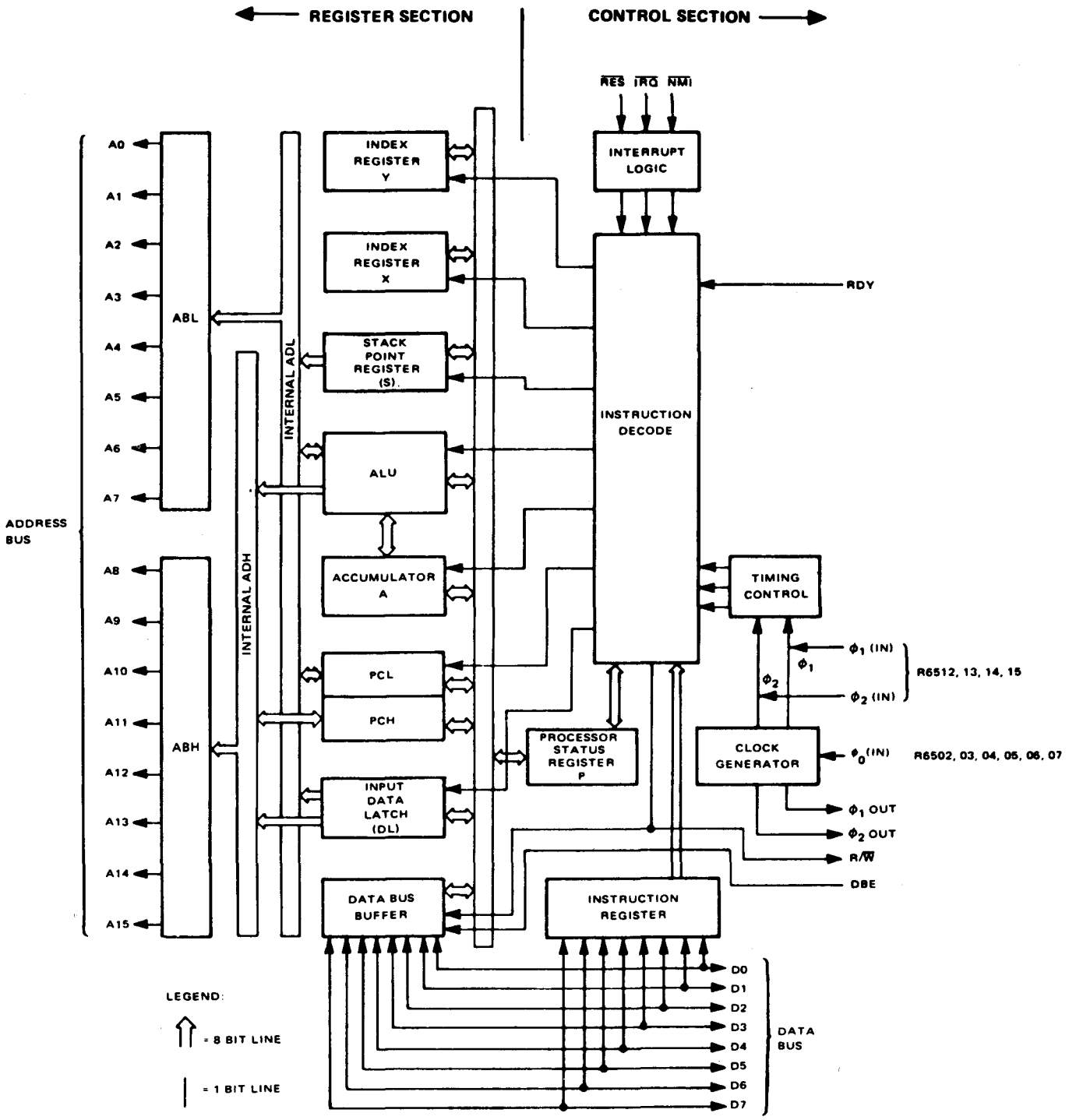


Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL







Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

Rockwell

R6500 Microcomputer System DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

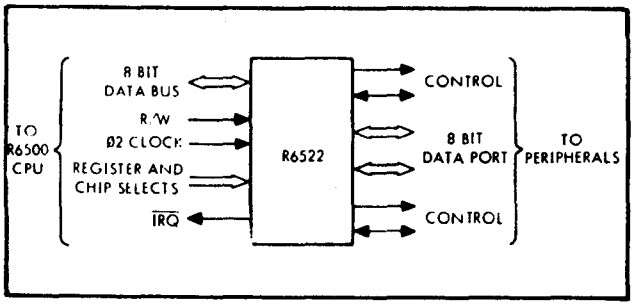
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

FEATURES

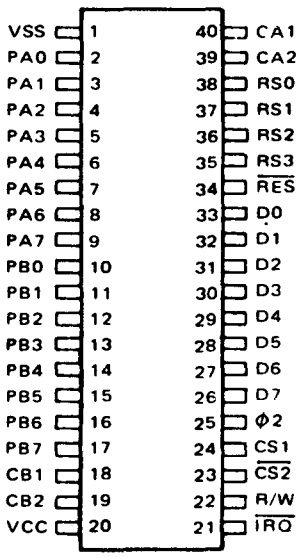
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0°C to +70°C
R6522AP	Plastic	2 MHz	0°C to +70°C
R6522C	Ceramic	1 MHz	0°C to +70°C
R6522AC	Ceramic	2 MHz	0°C to +70°C
R6522PE	Plastic	1 MHz	-40°C to +85°C
R6522APE	Plastic	2 MHz	-40°C to +85°C
R6522CE	Ceramic	1 MHz	-40°C to +85°C
R6522ACE	Ceramic	2 MHz	-40°C to +85°C
R6522CMT	Ceramic	1 MHz	-55°C to +125°C



Basic R6522 Interface Diagram



Pin Configuration

R6522 VERSATILE INTERFACE ADAPTER (VIA)

Specifications subject to change without notice

OPERATION SUMMARY

Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks	RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB	Controls Handshake	H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
L	L	L	H	ORA							
L	L	H	L	DDRB		H	L	L	H	T2C-H	Triggers T2L-L/T2C-L Transfer
L	L	H	H	DDRA							
						H	L	H		SR	
L	H	L	L	T1L-L T1C-L	Write Latch Read Counter	H	L	H	H	ACR	
						H	H	L	L	PCR	
L	H	L	H	T1C-H	Trigger T1L-L/T1C-L Transfer	H	H	L	H	IFR	
						H	H	H	L	IER	
L	H	H	L	T1L-L		H	H	H	H	ORA	No Effect on Handshake
L	H	H	H	T1L-H							

Note: L = 0.4V DC, H = 2.4V DC.

Timer 2 Control

RS3	RS2	RS1	RS0	R/W = L	R/W = H
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch
L	H	L	H	Write into high order latch Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag
L	H	H	L	Write low order latch
X	H	H	H	Write high order latch Reset T1 interrupt flag

Reading the Timer 1 Registers

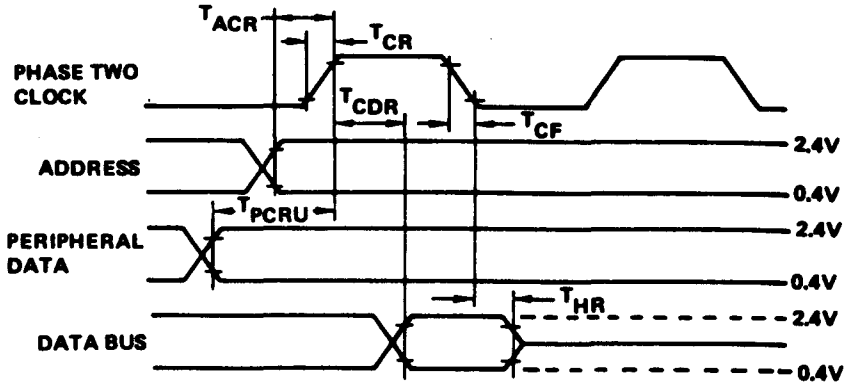
For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter Reset T1 interrupt flag
L	H	L	H	Read T1 high order counter
L	H	H	L	Read T1 low order latch
L	H	H	H	Read T1 high order latch

TIMING CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

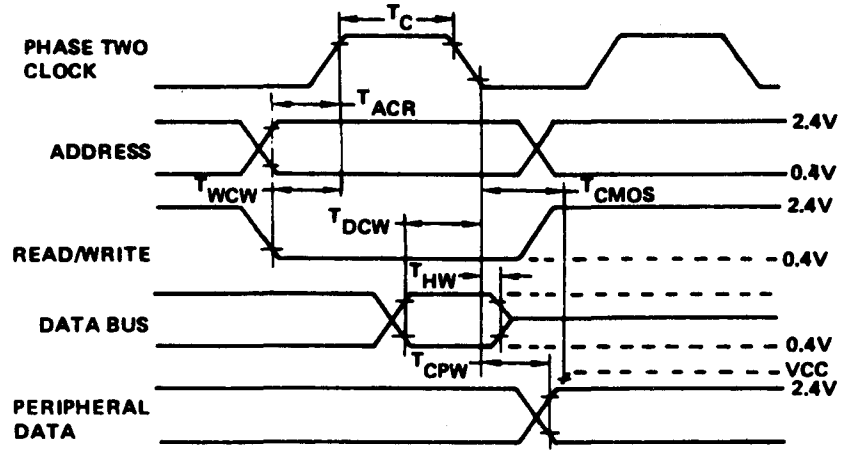
Parameter	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{RC} T_{RF}	–	–	25	nS



Read Timing Characteristics

Write Timing Characteristics

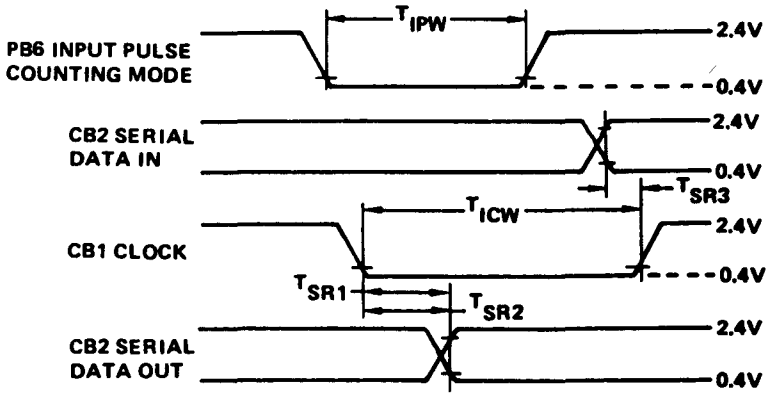
Parameter	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%)	T_{CMOS}	–	–	2.0	μS



Write Timing Characteristics

I/O Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals	T_{RF}	–	–	1.0	μs
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode)	T_{CA2}	–	–	1.0	μs
Delay time, clock negative transition to CA2 positive transition (pulse mode)	T_{RS1}	–	–	1.0	μs
Delay time, CA1 active transition to CA2 positive transition (handshake mode)	T_{RS2}	–	–	2.0	μs
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake)	T_{WHS}	–	–	1.0	μs
Delay time, peripheral data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode)	T_{RS3}	–	–	1.0	μs
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode)	T_{RS4}	–	–	2.0	μs
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching)	T_{IL}	300	–	–	ns
Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out)	T_{SR1}	–	–	300	ns
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out)	T_{SR2}	–	–	300	ns
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	ns
Pulse Width – PB6 Input Pulse	T_{IPW}	2	–	–	μs
Pulse Width – CB1 Input Clock	T_{ICW}	2	–	–	μs
Pulse Spacing – PB6 Input Pulse	I_{IPS}	2	–	–	μs
Pulse Spacing – CB1 Input Pulse	I_{ICS}	2	–	–	μs



I/O Timing Characteristics

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded
0	1	Generate continuous interrupts
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation
1	1	Generate continuous interrupts and a square wave output on PB7

FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Typical functions are shown below:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode – Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode – Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode – Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode – Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode – Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse output mode – CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode – The CA2 output is held low in this mode.
1	1	1	Manual output mode – The CA2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

Rockwell

R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

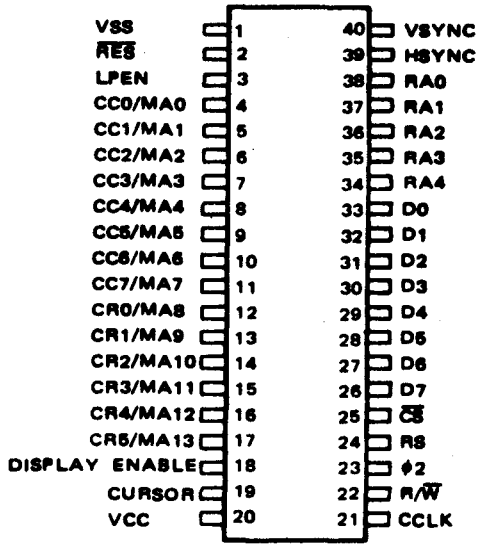
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

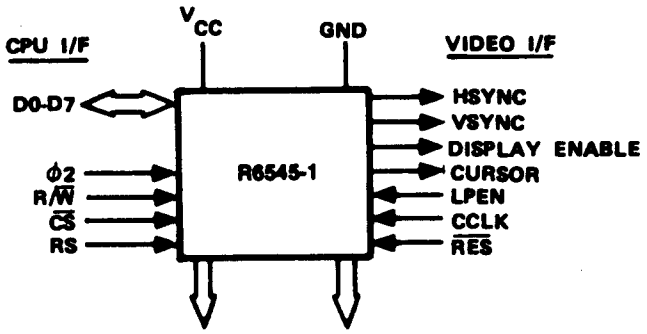
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read ($R/\overline{W}$ = High)	Write ($R/\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register		✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	–		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	–	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	–	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	–	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	–	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

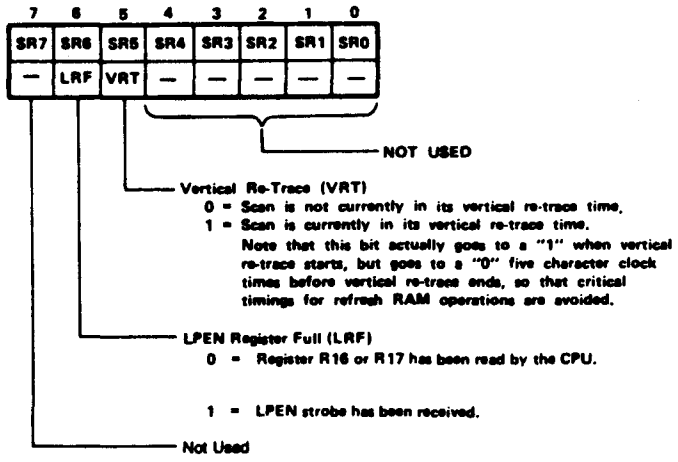
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, [–][0][1][–][–][–][–][–] immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

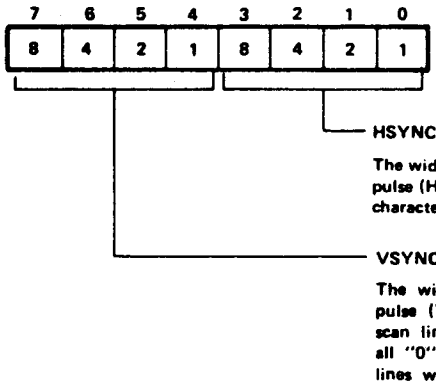
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

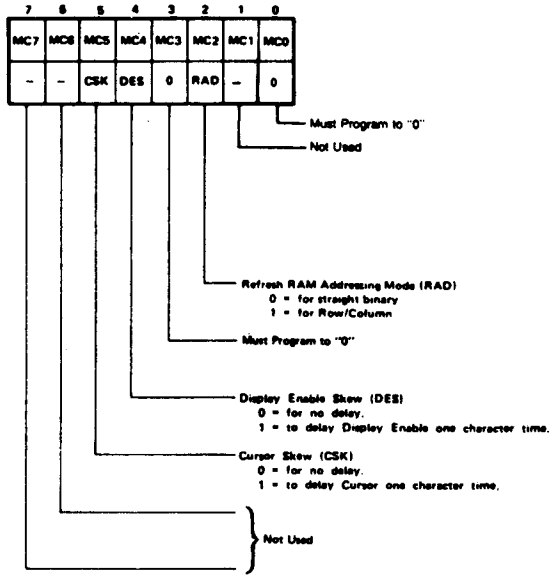
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

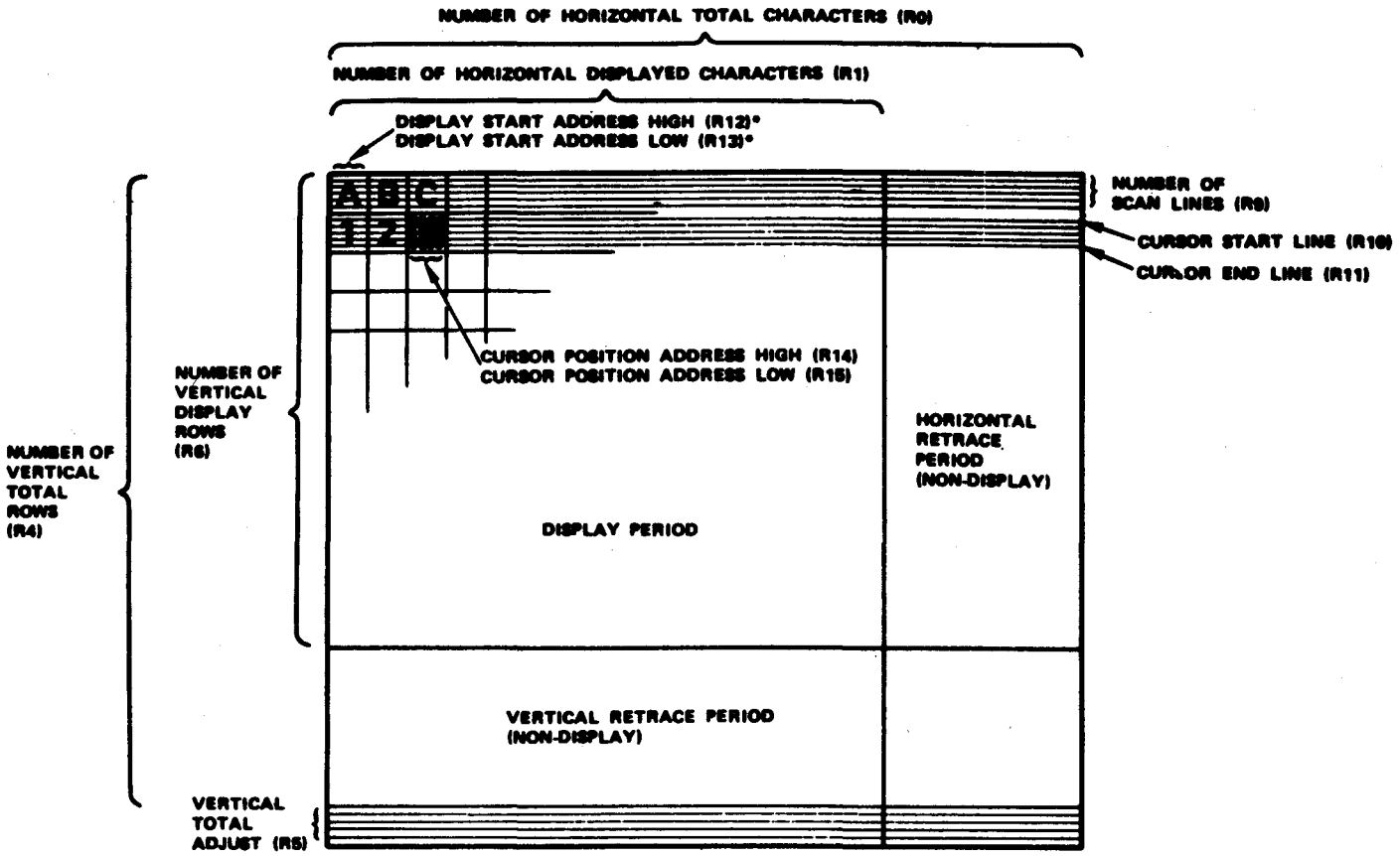


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81		89
80	81	82	83		156	157	158	159	160	161		169
160	161	162				237	238	239	240			249
240	241	242				317	318	319	320			329
1680	1681	1682				1757	1758	1759	1760			1769
1760	1761	1762				1837	1838	1839	1840			1849
1840	1841	1842				1917	1918	1919	1920			1929
1920	1921	1922				1997	1998	1999	2000			2009
2000	2001	2002				2077	2078	2079	2080			2089
2640	2641	2642				2717	2718	2720				2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

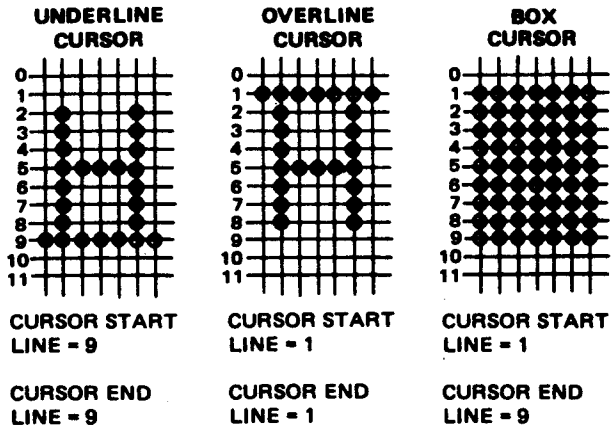


Figure 3. Cursor Display Scan Line Control Examples

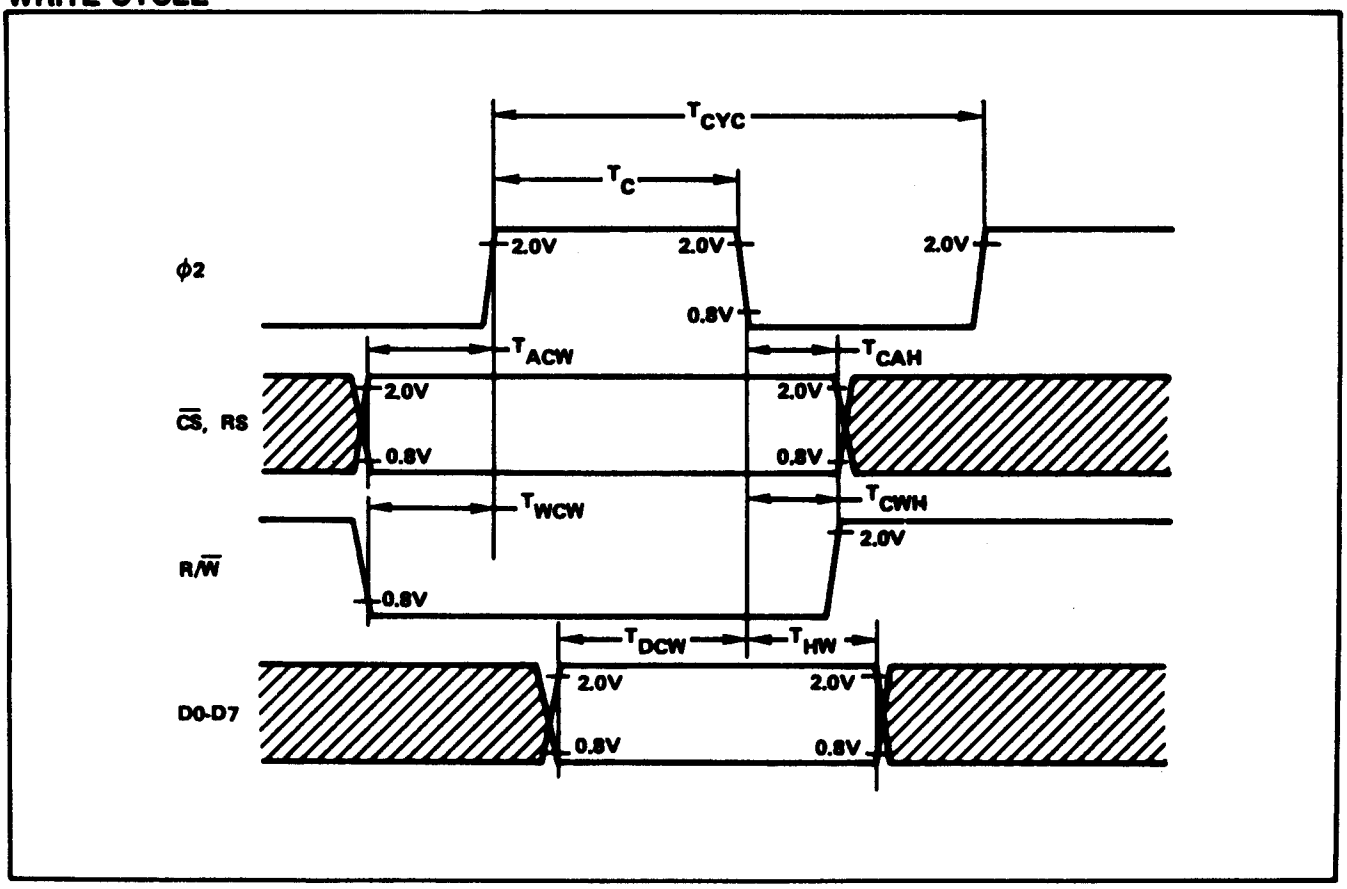
MPU WRITE TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	µs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACW}	180	–	90	–	ns
Address Hold Time	T_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	T_{DCW}	265	–	100	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE CYCLE



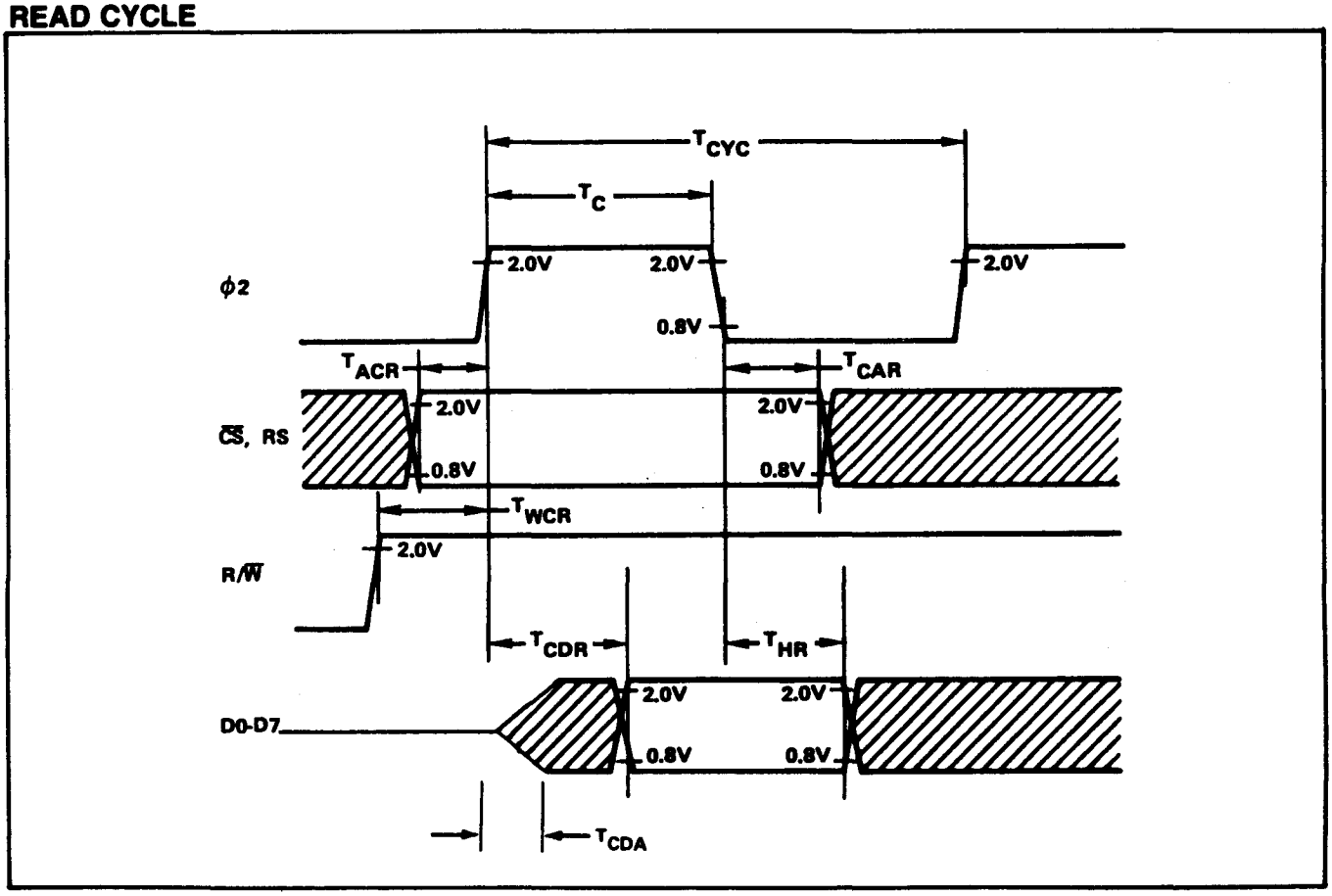
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



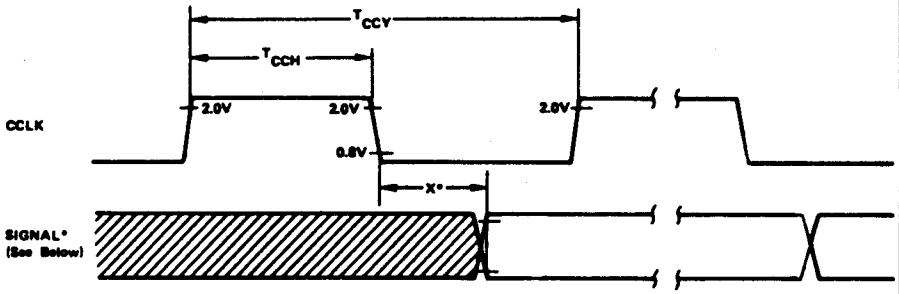
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCV}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	–	200	–	ns
MA0-MA13 Propagation Delay	T_{MAD}	–	300	–	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	–	300	–	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	–	450	–	450	ns
HVSNC Propagation Delay	T_{HSD}	–	450	–	450	ns
VSYNC Propagation	T_{VSD}	–	450	–	450	ns
Cursor Propagation Delay	T_{CDD}	–	450	–	450	ns
LPEN Strobe Width	T_{LPH}	150	–	150	–	ns
LPEN to CCLK Delay	T_{LP1}	20	–	20	–	ns
CCLK to LPEN Delay	T_{LP2}	0	–	0	–	ns

t_r, t_f = 20 ns (max)

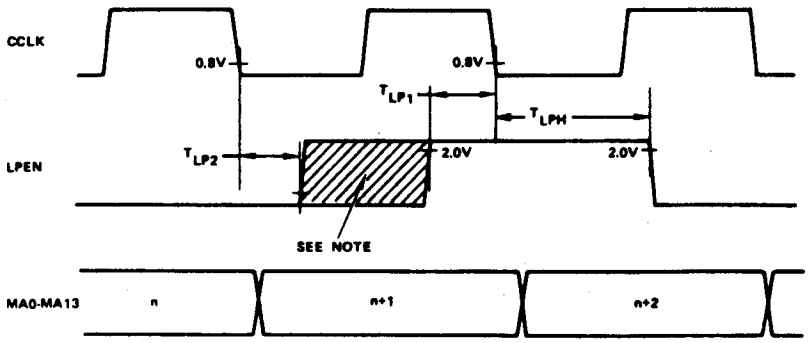
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

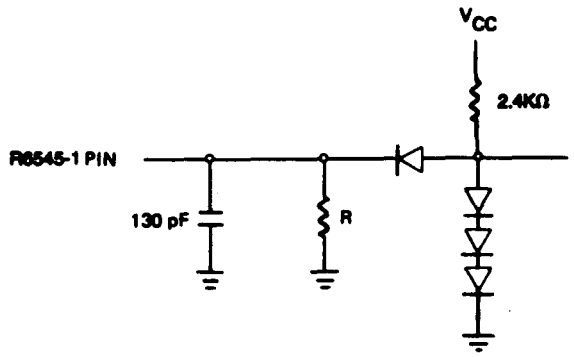
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	µAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	µAdc
Output High Voltage I_{LOAD} = 205 µAdc (D0-D7) I_{LOAD} = 100 µAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

Rockwell

R6500 Microcomputer System
DATA SHEET

Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component – eliminating the multiple-component support that is typically needed.

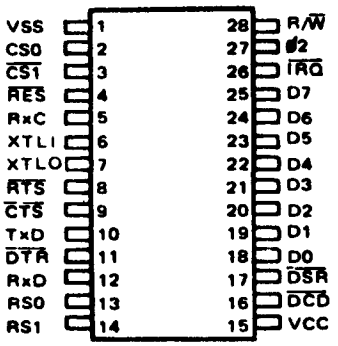
In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

FEATURES

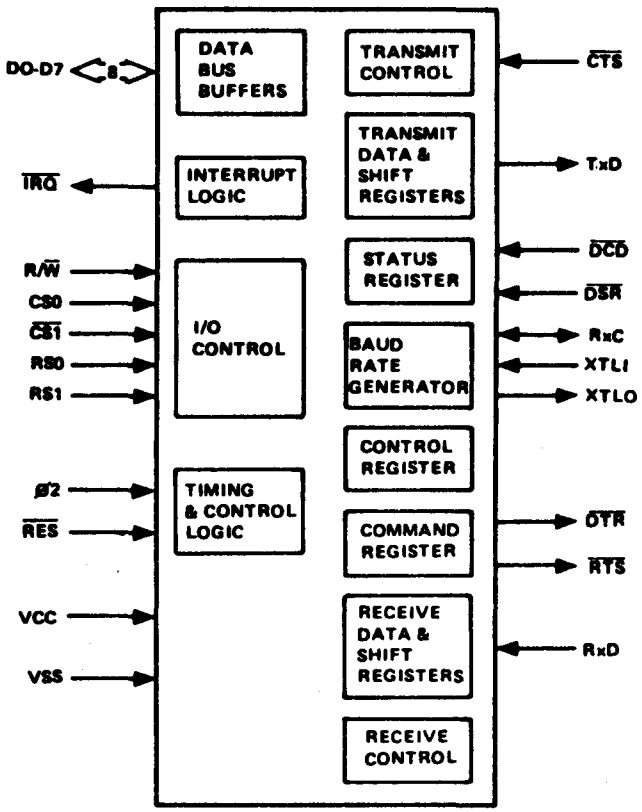
- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6551P	Plastic	1 MHz	0°C to +70°C
R6551AP	Plastic	2 MHz	0°C to +70°C
R6551C	Ceramic	1 MHz	0°C to +70°C
R6551AC	Ceramic	2 MHz	0°C to +70°C



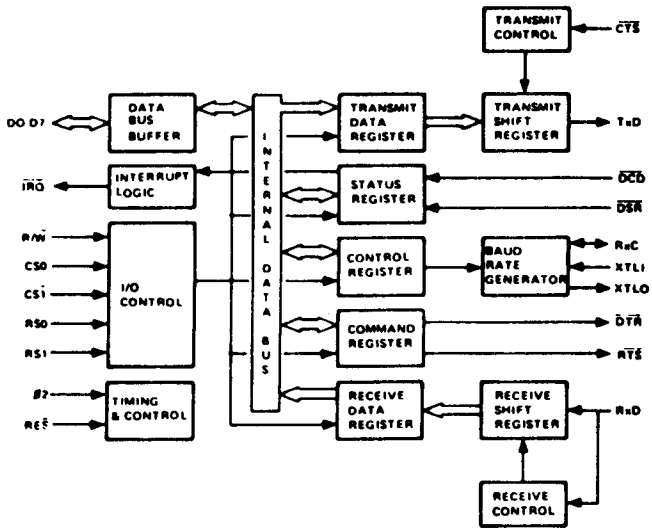
R6551 Pin Configuration



R6551 Interface Diagram

Specifications subject to change without notice
Document No. 29000 D53
Rev. 1, January 1981

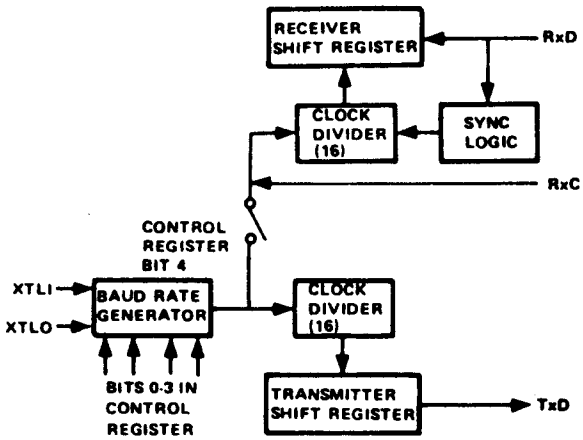
INTERNAL ORGANIZATION



R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

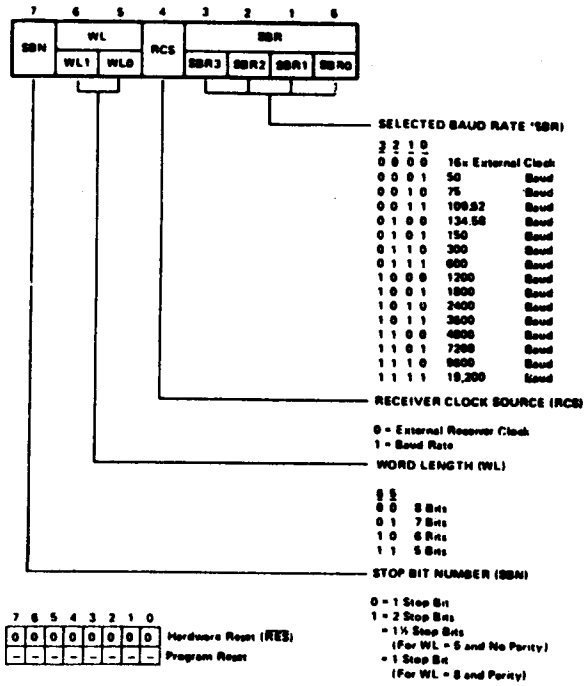
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

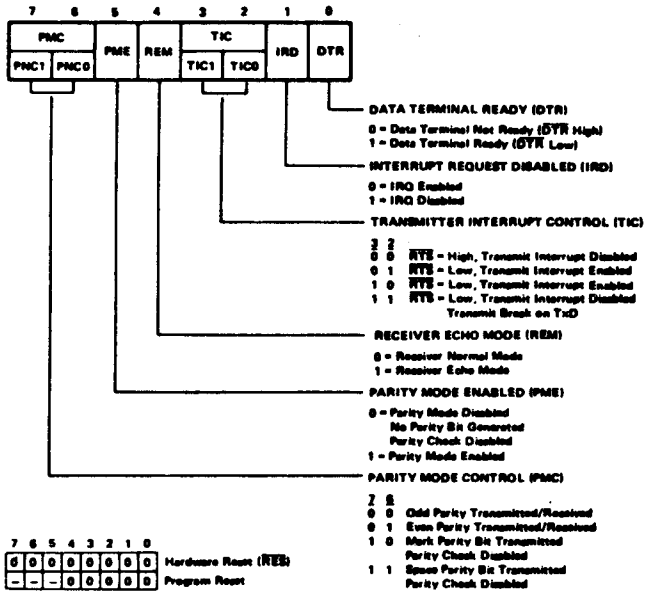
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



R6551 Control Register

Command Register

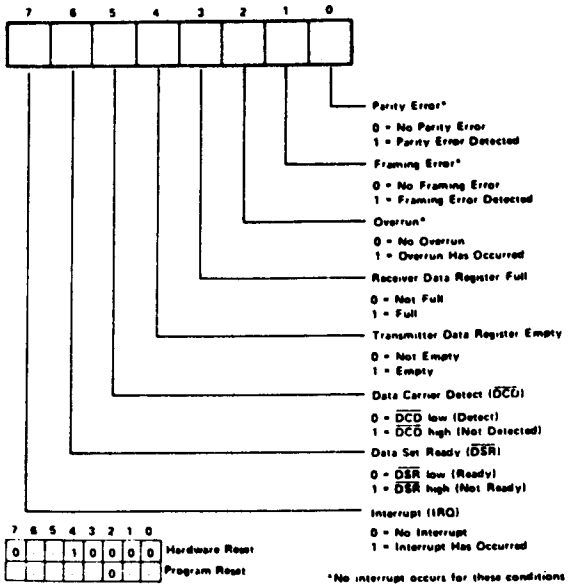
The Command Register controls specific modes and functions.



R6551 Command Register

Status Register

The Status Register reports the status of various R6551 functions



R6551 Status Register

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{W}$ pin allows a write to the R6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

D0-D7 (Data Bus)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

CS0, $\overline{CS1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{CS1}$ is low.

RS0, RS1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTLI, XTLO (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input, and must be connected. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect)

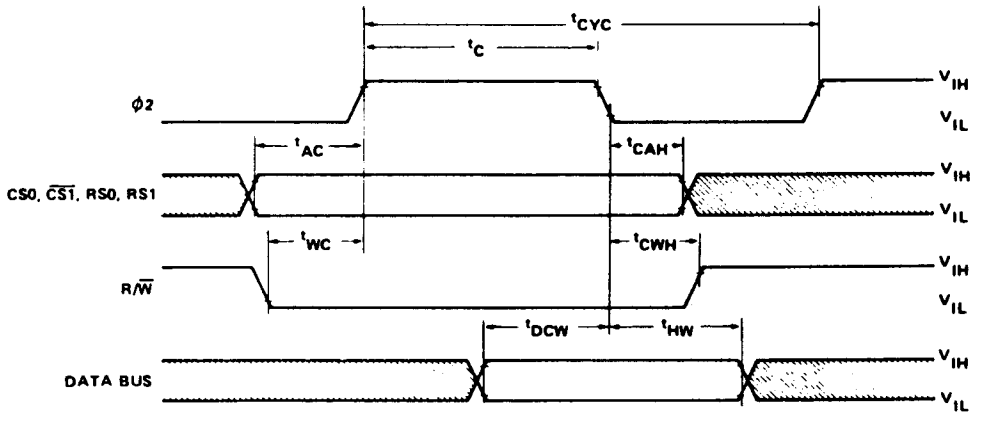
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like $\overline{DSR}$, $\overline{DCD}$ is a high-impedance input, and must be connected.

READ/WRITE CYCLE CHARACTERISTICS

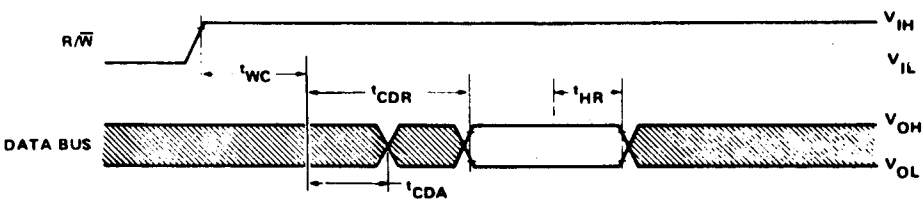
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



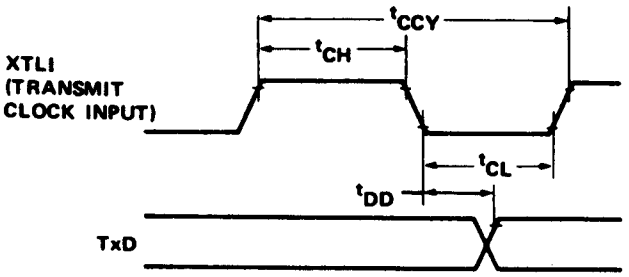
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

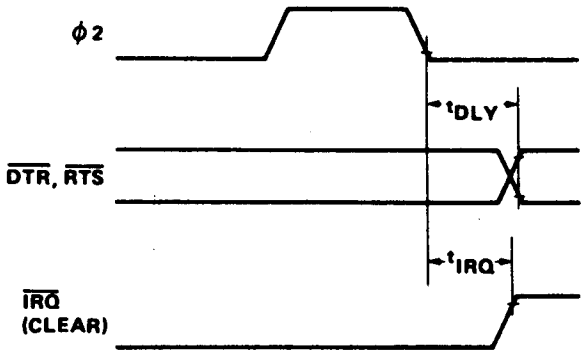
(t_r, t_f = 10 to 30 ns)

The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

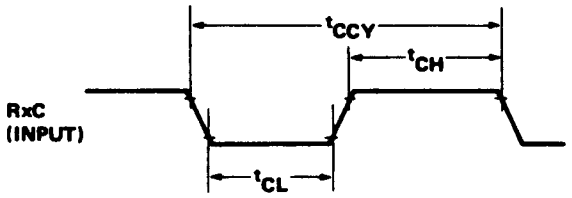


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

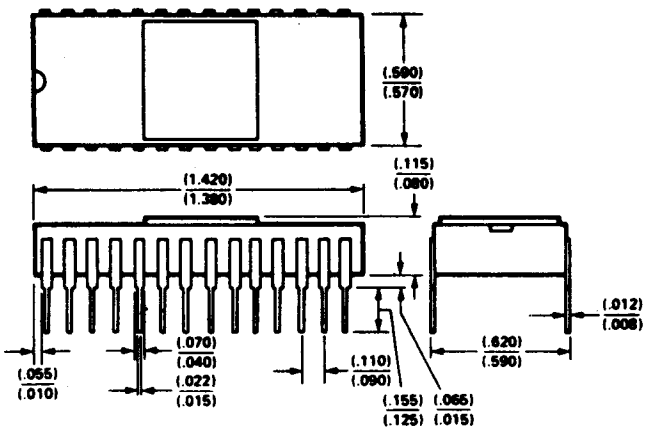


NOTE: RxD rate is 1/16 RxC rate

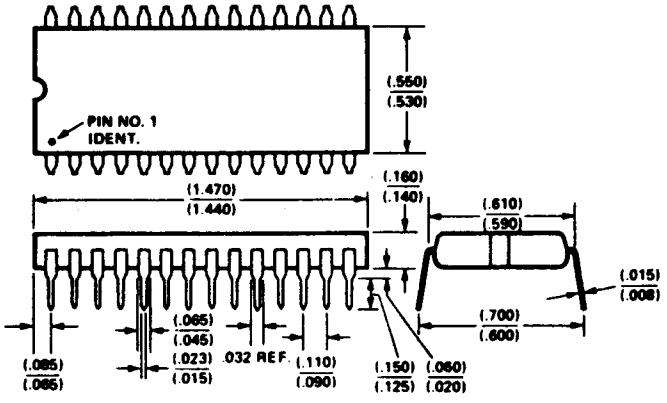
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



PRELIMINARY

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

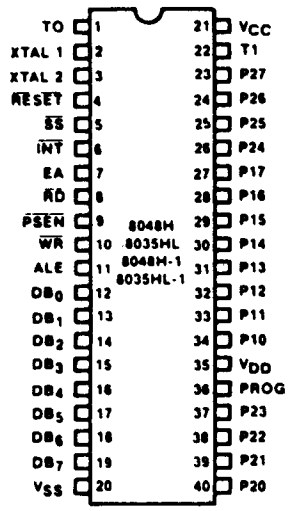
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

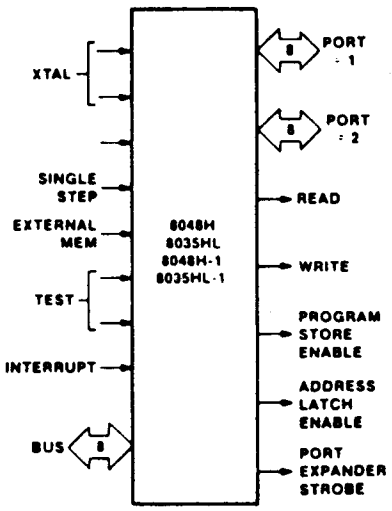
To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.

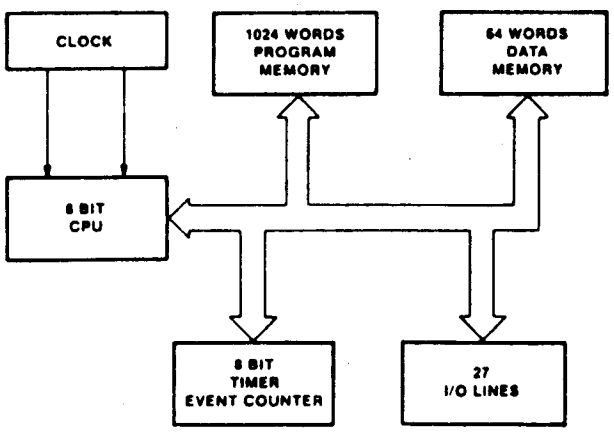
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

PIN CONFIGURATION **LOGIC SYMBOL** **BLOCK DIAGRAM**







PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R*	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNT1	Enable timer/counter interrupt	1	1
DIS TCNT1	Disable timer/counter interrupt	1	1

Control

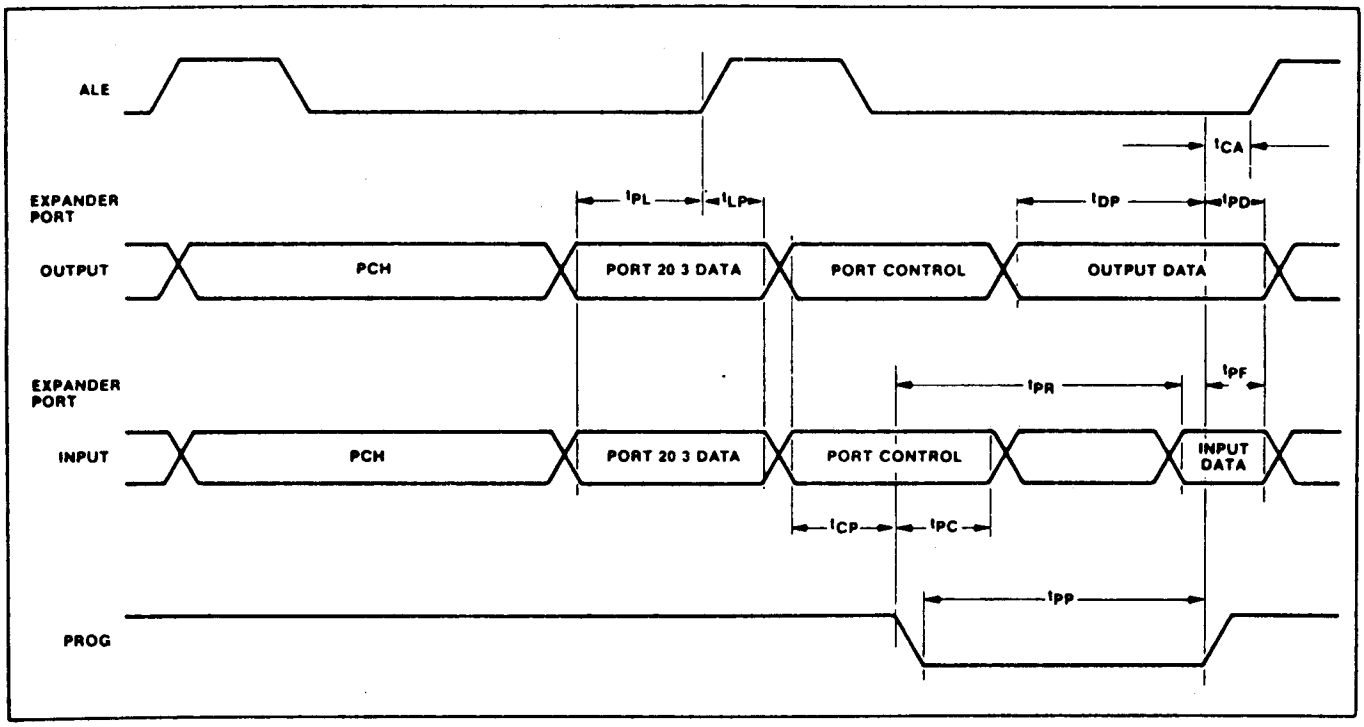
Mnemonic	Description	Bytes	Cycles
EN 1	Enable external interrupt	1	1
DIS 1	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING



BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY		
T_{LL}	7/30	T_{CY}	MIN
T_{AL}	1/10	T_{CY}	MIN
T_{LA}	1/15	T_{CY}	MIN
T_{CC} (1)	1/2	T_{CY}	MIN
T_{CC} (2)	2/5	T_{CY}	MIN
T_{DW}	2/15	T_{CY}	MIN
T_{WD}	1/15	T_{CY}	MIN
T_{DR}	0		MIN

T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2) : $\overline{PSEN}$

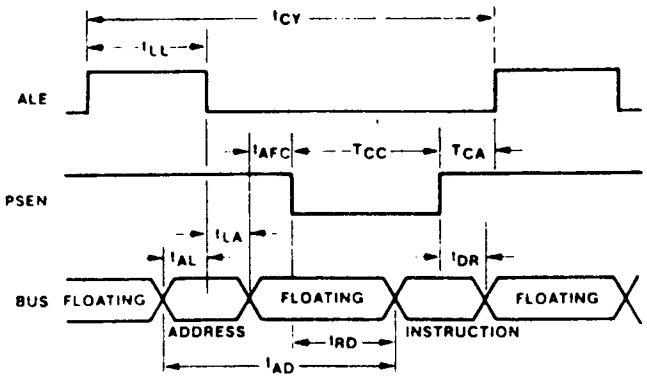
SYMBOL	FUNCTION OF TCY		
T_{RD} (1)	11/30	T_{CY}	MAX
T_{RD} (2)	3/10	T_{CY}	MAX
T_{AW}	3/10	T_{CY}	MIN
T_{AD} (1)	1/2	T_{CY}	MAX
T_{AD} (2)	1/3	T_{CY}	MAX
T_{AFC}	1/30	T_{CY}	MIN
T_{CA}	1/15	T_{CY}	MIN

T_{RD} (1) : $\overline{RD}$
T_{RD} (2) : $\overline{PSEN}$

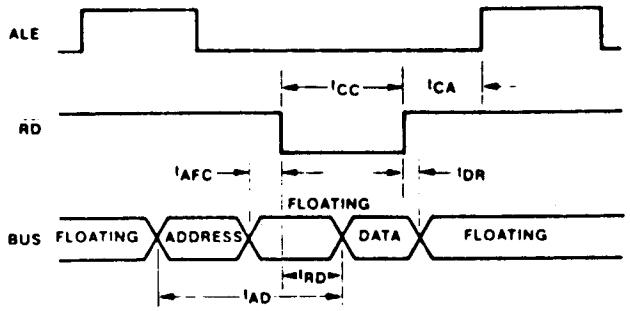
T_{AD} (1) : $\overline{RD}$
T_{AD} (2) : $\overline{PSEN}$

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

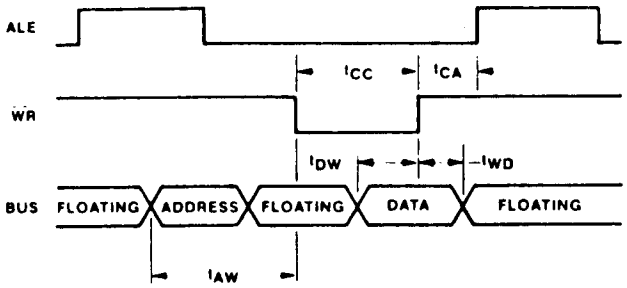
WAVEFORMS



Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory

Input and Output for A.C.Tests.

A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit	Conditions (Note 1)
		6 MHz		8 MHz		11 MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		490		300		ns	
t_{DW}	Data Setup before $\overline{WR}$	370		370		280		ns	
t_{WD}	Data Hold after $\overline{WR}$	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		340		200	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

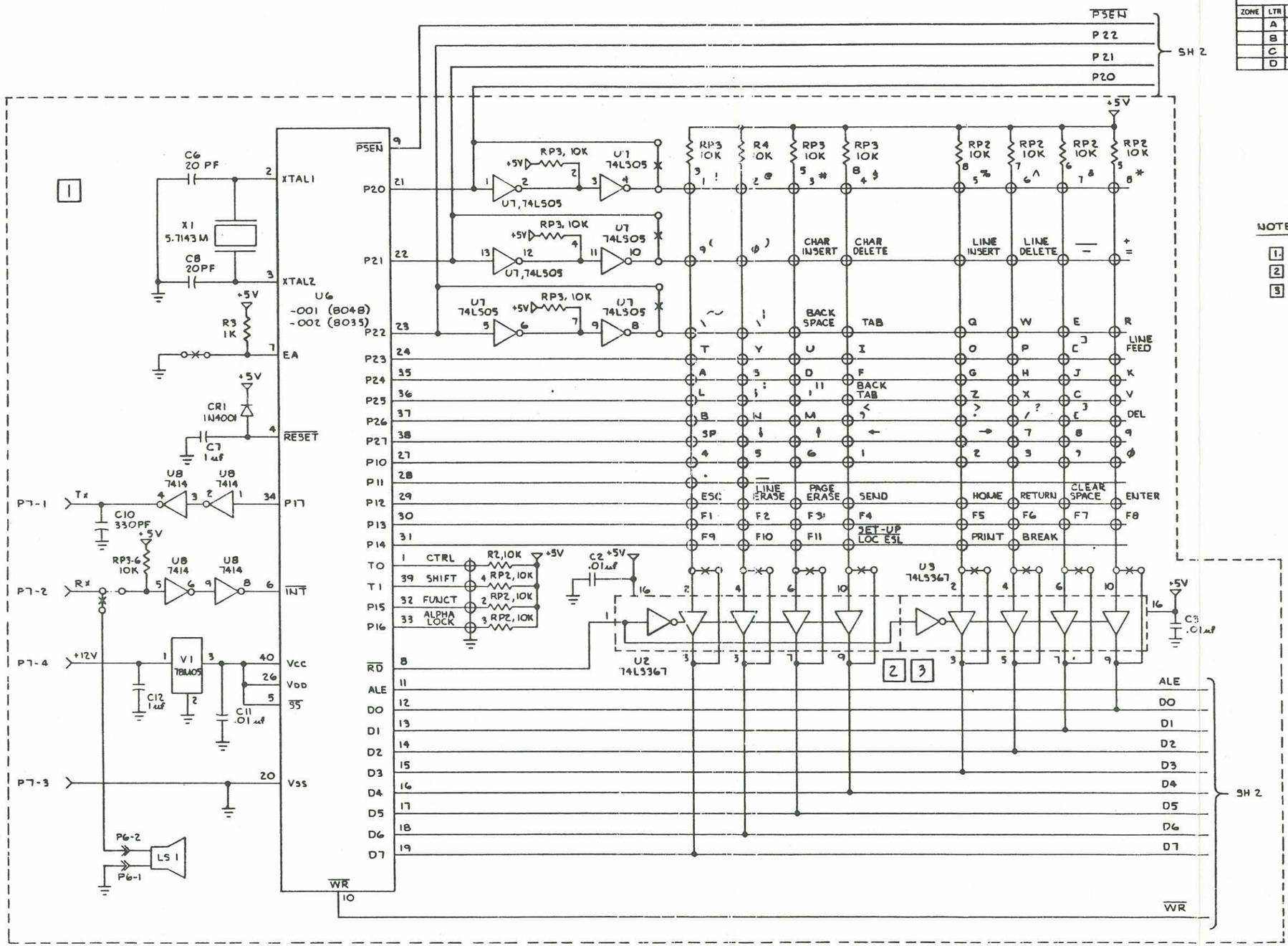
NOTE 1: Control outputs CL = 80 pF
BUS outputs CL = 150 pF

NOTE 2: BUS High Impedance Load: 20 pF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		

NOTES:-UNLESS OTHERWISE SPECIFIED

1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL

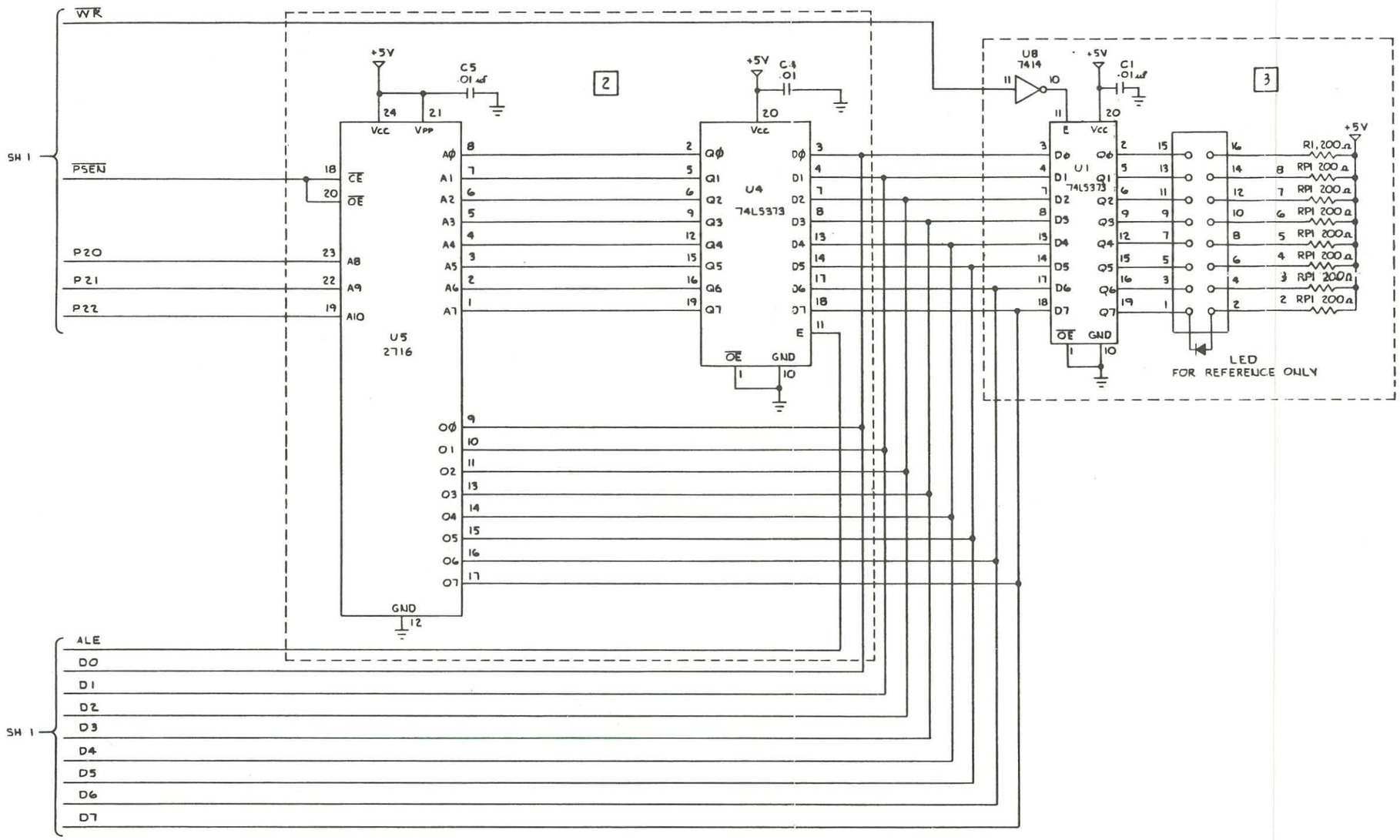


8600003-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
		ANG ± PLC ± PLC	ENGR	TITLE PCB SCHEMATICS 950 KEYBOARD
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 1 OF 2 DRAWING NO 2010300 REV D

20103-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED	DWN Caballero 10-2-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK Caballero 10-2-80	TITLE PCB SCHEMATIC 950 KEYBOARD
		ANG 2 PLC 3 PLC	ENGR	
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 2 OF 2 DRAWING NO 2010300 REV

D 2010300-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 40		
	A1	" " ECO 45		
	B	" " ECO 41,47		
	B1	" " ECO 54		
	B2	" " ECO 70,82	9/21/81	
	B3	" " ECO 01380442	9/15/82	

A69 74LS04 — A70 74LS00 — A69 74LS04 — A63 74LS32 — A63 74LS32 — A58 74LS32

E20 E18 E17 E15 E19 E16 E14 E22 E23 E26 E21

A62 74LS139

A52 2332

A42 2716/2332

A41 2332/2564

R24 1K R23 1K R39 3.3K R45 9.3K R46 3.3K

A53 6502A

A62 74LS139

SH 5,7 IRQ

SH 7 NMI

SH 6 ϕ0

SH 6 RESET

DISP. MEM. SH 2,6

TOP. SEL SH 2,5,6,7

SCREG SEL SH 4

P8-1 P8-2 P8-3 P8-8 P8-7

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 — SH 2,5,7 / SH 2,7 / SH 2,7 / SH 2 / SH 2,5 / SH 2,5 / SH 2 / SH 2,6,7

R/W DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 — SH 2,3,5,7

B5	PROD REL PER ECO 0483			
B4	PROD REL PER ECO 0473			

APPLICATION — NEXT ASSY | USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG ± PLC .3 PLC

DWN O. Cavallero 9-25-80 — CHK O. Cavallero 9-25-80 — ENGR S. Tilly 9/15/82 — APPD — APPD — APPD

SCALE NONE — MATERIAL — FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD

SIZE — SHT 1 OF 7 — DRAWING NO 7009800 — REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 7 CRTC. RESET
SH 6 CCLK
SH 1 ABØ
SH 1 R/W
SH 1 DBØ DB1 DB2 DB3 DB4 DB5 DB6 DB7
SH 1 IO.P.SEL
SH 1 ØO
SH 1 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 DISP.MEM
SH 6 SEL.CPU.ADDR.

+5V
20 Vcc
2 RES
21 CCLK
24 RS
22 R/W
33 DBØ
32 DB1
31 DB2
30 DB3
29 DB4
28 DB5
27 DB6
26 DB7
25 CS
23 Ø2
1 Vss

A55 6545

HSYNC 39 → HSN → SH 7
VSYNC 40 → VSN → SH 4,6
ENABLE 18 → DISPL.ENA → SH 4
CURSOR 19 → CURSOR → SH 4
RAØ 38
RA1 37
RA2 36
RA3 35
RA4/STB 34
MAØ 4
MA1 5
MA2 6
MA3 7
MA4 8
MA5 9
MA6 10
MA7 11
MA8 12
MA9 13
MA10 14
MA11 15
MA12 16
MA13 17

A63 74LS32 (13, 12 → 11)
A63 74LS32 (10, 9 → 8)

R25 1K

A46 74LS157
A45 74LS157
A44 74LS157
A43 74LS157

(1A 2A 3A 4A 1B 2B 3B 4B; EN 15; SEL 1; 1Y 2Y 3Y 4Y 4 7 9 12)

A46: DMEM.EN, AD.RAM.13, AD.RAM.12
A45: DM.R/W, AD.RAM.11, AD.RAM.10, AD.RAM.9, AD.RAM.8
A44: AD.RAM.7, AD.RAM.6, AD.RAM.5, AD.RAM.4
A43: AD.RAM.3, AD.RAM.2, AD.RAM.1, AD.RAM.Ø

SH 3 SH 3 SH 3 SH 3

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O Carrillo 9-24-80	TeleVideo, Inc.
HEX ASSY	USED ON	ANG 2 PLC 3 PLC	CHK O Carrillo	TITLE PCB SCHEMATIC 950 CONT. BD.
			ENGR	
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE SHT 2 OF 7 DRAWING NO. 2009800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

A15 74LS42

2 ADRAM 13
SH 2 AD·RAM·11
SH 2 AD·RAM·12
SH 6 QC·CLK

A8 74LS04

A16 74LS32

SH 2 AD·RAM·10, AD·RAM·9, AD·RAM·8, AD·RAM·7, AD·RAM·6, AD·RAM·5, AD·RAM·4, AD·RAM·3, AD·RAM·2, AD·RAM·1, AD·RAM·Ø

A25 2114 · A26 2114 · A27 2114 · A28 2114 · A34 6116 · A35 6116 · A36 6116 · A37 6116

SH 2 DM·R/$\overline{W}$

SH 1 DB·7, DB·6, DB·5, DB·4, DB·3, DB·2, DB·1, DB·Ø

A14 BTL45

SH 2 $\overline{DMEN}$·EN
SH 1 R/$\overline{W}$

CH·AD·7, CH·AD·6, CH·AD·5, CH·AD·4, CH·AD·3, CH·AD·2, CH·AD·1, CH·AD·Ø → SH 4

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN: O Cavallaro 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O Cavallaro 9-25-80	
		ANG 2 PLC 3 PLC	ENGR	TITLE: PCB SCHEMATIC 950 CONT. BD.
		± . ± . ±	APPD	
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE · SHT 3 OF 7 · DRAWING NO 2009800 · REV B5

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
	B5	SEE SHT 1	

SH 3 { CH·AD·7, CH·AD·6, CH·AD·5, CH·AD·4, CH·AD·3, CH·AD·2, CH·AD·1, CH·AD·Ø }

A24 74LS374 (1D–8D, CLK, OE, 1Q–8Q)

SH 7 { CRTC·RES, HSN }

SH 1 { SCREG SEL., DB4, DB5, DB6, DB7 }

A61 74LS174 (CP, D5, D2, D1, DØ, MR, Q5, Q2, Q1, QØ)

A60 74LS191 (PL, CP, DØ, D1, D2, D3, TC, RC, Q0, Q1, Q2, Q3, U/D, CE)

R38 1K +5V

SH 6 SHIFT.CLK
SH 6 DC CARRY
A13 74LS00

SH 2 VSN

A18 74LS173 (CLK, SIR, ID, 2D, 3D, 4D, M, N, 1Oz, 1Oı, 1Q–4Q)

R14 1K +5V

E5 E6

DEL·DISPL·ENA
DISPL·EN
A13 74LS00

A2 74LS04

SH 6 SHIFT·CLK
SH 6 ROW 9
A12 74LS04

SH 6 DISPL.ENA
A12 74LS04

A9 74LS00 (×2)

A29 74LS08

SH 6 VSYNC (VSN)

A19 74LS174 (1D–4D, CK, CLR, 1Q–4Q)

A30 74LS08 (×4)

A20 74LS157 (SEL, 1A–4A, 1B–4B, STRB, 1Y–4Y)

A32 2332 (A11, A10, A9, A8, A7, A6, A5, A4, 2Ø, C5, A0–A3, O1–O8)

A33 2332 (A11, A10, A9, A8, A7, A6, A5, A4, C5, VPP, A0–A3, O1–O8)

R20 1K +5V

74LS00 (A11)

SH 6 DC CARRY

R19 1K +5V

A22 74LS166 (C, D, E, F, G, H, CK, S.IN, CK INH, LD, QH)

R16 1K +5V

SH 2 CURSOR

SH 6 RAØ
SH 6 RA3

R17 1K +5V

A23 74LS166 (A, B, C, D, E, F, G, H, CK, CK.INH, LD, CLR, S.IN, QH)

SH 6 DOT SERIAL

A13 74LS00

C75 100 pf

A12 74LS04

R18 1K +5V

A31 74LS74 (PR, D, Q, CK, CLR)

SH 6 DEL CURSOR

A21 74S174 (1D–6D, CK, CLR, 1Q–6Q)

R15 1K +5V

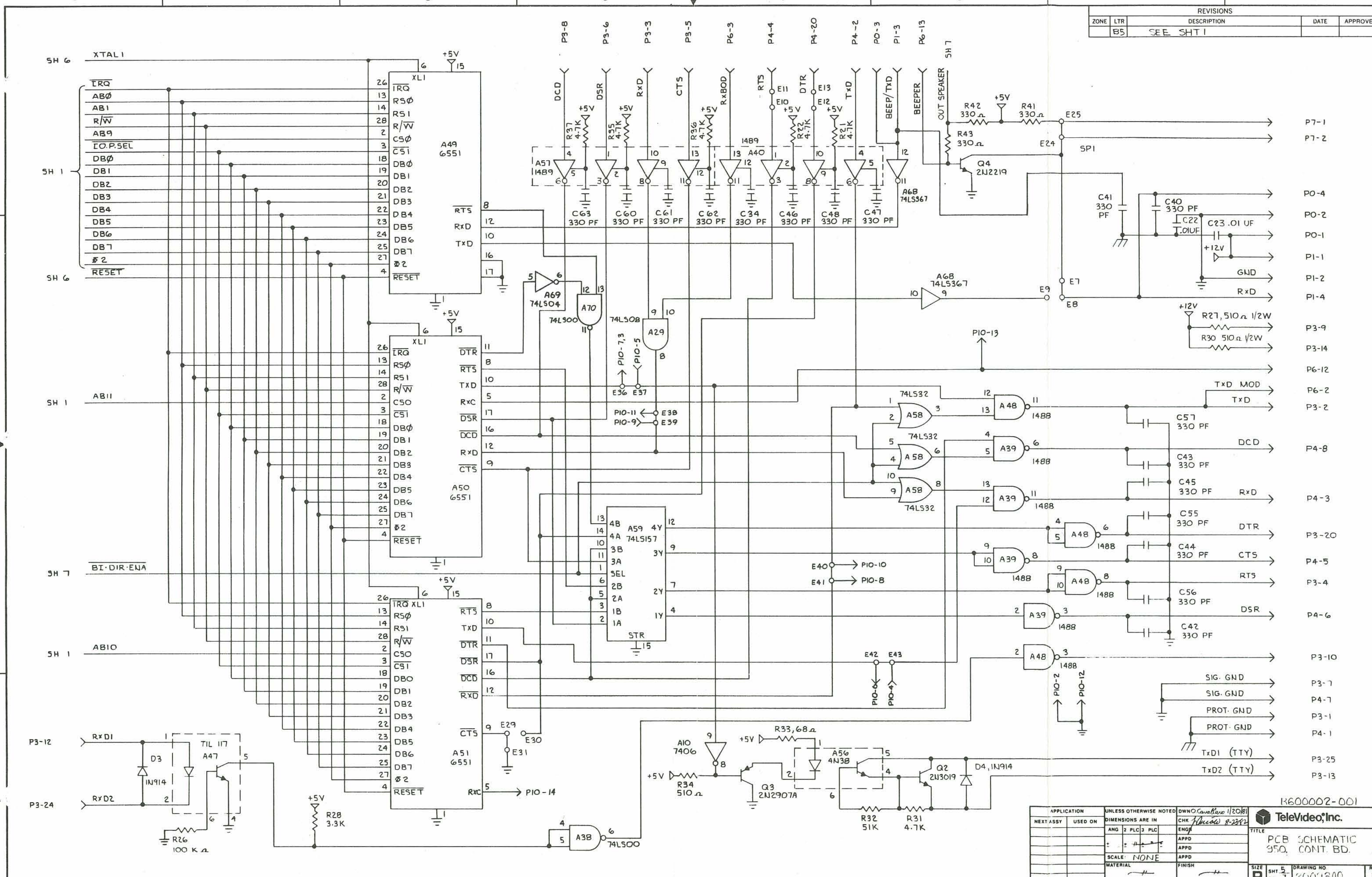
SH 6 { UNDERLINE, REVERSE·VIDEO, BLINK, BLANK, DEL·DISPL·EN–, HALF·INTENSITY }

P10-1

SH 6 ROW·9
SH 4 DISPL·EN–

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Carrillo 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Carrillo 9-	TITLE: PCB SCHEMATIC 950 CONT. BD.
		ANG 2 PLC 3 PLC	ENGR	
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE — SHT 4 OF 7 — DRAWING NO. 2009800 — REV B5


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B5 SEE SHT 1
SH 6 XTAL1
SH 1
IRQ
ABØ
AB1
R/W
AB9
I.O.P.SEL
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Ø2
SH 6 RESET
A49 6551
A50 6551
A51 6551
SH 1 AB11
SH 7 BI·DIR·ENA
SH 1 AB10
P3-12 RxD1
P3-24 RxD2
TIL 117 A47
D3 1N914
R26 100 K Ω
R28 3.3K
A38 74LS00
A69 74LS04
A70 74LS00
A29 74LS08
A59 74LS157
A57 1489
A40 1489
A68 74LS367
A58 74LS32
A39 1488
A48 1488
A10 7406
A56 4N38
Q2 2N3019
Q3 2N2907A
Q4 2N2219
D4, 1N914
R33, 68 Ω
R34 510 Ω
R32 51K
R31 4.7K
R42 330 Ω
R41 330 Ω
R43 330 Ω
R27, 510 Ω 1/2W
R30 510 Ω 1/2W
C41 330 PF
C40 330 PF
C22 .01UF
C23 .01 UF
DCD DSR RxD CTS RxBOD RTS DTR TxD BEEP/TxD BEEPER OUT SPEAKER
P3-8 P3-6 P3-3 P3-5 P6-3 P4-4 P4-20 P4-2 P0-3 P1-3 P6-13 SH 7
P7-1
P7-2
SP1
P0-4
P0-2
P0-1
P1-1
P1-2 GND
P1-4 RxD
P3-9
P3-14
P6-12
P6-2 TxD MOD
P3-2 TxD
P4-8 DCD
P4-3 RxD
P3-20 DTR
P4-5 CTS
P3-4 RTS
P4-6 DSR
P3-10
P3-7 SIG. GND
P4-7 SIG. GND
P3-1 PROT. GND
P4-1 PROT. GND
P3-25 TxD1 (TTY)
P3-13 TxD2 (TTY)
P10-14
P10-13
P10-10
P10-8
P10-11
P10-9
P10-6
P10-4
P10-2
P10-12
B600002-001
TeleVideo, Inc.
TITLE PCB SCHEMATIC 950, CONT. BD.
SCALE: NONE
SIZE D SHT 5 OF 11
DRAWING NO 2002800
REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 2 RAØ
SH 2 RA3
SH 7 BLACK·ON·WHITE (B·O·W)
SH 4 BLINK
SH 7 BLI·RATE
74LS00 A11, A11, A2 74LS04, A11 74LS00, A2 74LS04, A11 74LS00, A9 74LS00, A1 74LS86
SH 4 BLANK
DOTS·SERIAL
ROW·9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
A9 74LS00, A1 74LS86
DEL DISPL·EN –
HALF·INTENSITY
A1 74LS86, A10 7406, R5 1K
SH 7 FORCE·BLANK
A10 7406
SH 2 VSN
SH 7 HSN
SH 1 DISP·MEN
A2 74LS04, A1 74LS86
A12 74LS04, C9 0.01 uf, A12 74LS04, A13 74LS00
ROW 9 SH 4
A10 7406, R6 750Ω, R3 1K, R7 22Ω, +5V
E1 E2, R4 270Ω, D1 1N914, E3, E4, R1 1K, Q1 2N2219, + C6 4.7 uf, R2 68Ω
+12V P8-5 P8-6 P6-1 P6-14
+5V P6-6 P6-9
-12V P6-5 P6-10
GND P6-7 P6-8 P8-9 P8-10
P2-4
P2-3
SH 4 COMP.V+TTL VIDEO P2-6
+VSYNC (VSN) P2-5
+HSYNC. P2-1
A2 74LS04, A16 74LS32
SEL·CPU·ADDR SH 2
DC.CARRY SH 4
C.CLK SH 2
DC.CARRY SH 4
C.CLK SH 7
R8 1K, +5V, EN EN CLR, A3 74LS163, TC QD QC LD CLK, A12 74LS04, E33 E32, OSC.1 K1114A 23.814 MHZ
A2 74LS04, A5 74LS00, A8 74LS04, R10 1K, +5V, PR J AG Q CLK K CLR, 74LS109
SH 1 IO.P.SEL
SH 1 AB13
74LS32 A16, A8 74LS04
R9 1K, +5V, EN EN CLR, A4 74LS163, QD QC QB QA LD CLK
A7 A5 74LS08, 74LS00
A8 74LS04
A5 74LS00
R11 3.3K, R12 1M, R13 47K, 1N914 D2, A17 555 TIMER, C13 .01uf, C12 .01uf, C15 10uf, +5V, R29 4.7K, C49 .01uf
RESET SH 1,5,7
Ø 0 SH 1
SHIFT·CLK. SH 4
SHIFT·CLK SH 4
XTAL1 SH 5
QC CLOCK SH 3

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Carvalho 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± PLC .3 PLC	CHK O. Carvalho 9-25-80	TITLE PCB SCHEMATIC 950 CONT. BD.
		SCALE NONE	ENGR	
		MATERIAL	APPD	SIZE SHT 6 OF 7 DRAWING NO. 2009800 REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 1 { DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ }
SH 1 { ABØ AB1 AB2 AB3 }
SH 1 R/W
SH 1 Ø0
SH 6 RESET
SH 1 IO.P.SEL
SH 1 AB13
SH 1 NMI
SH 5 IRQ

A54 G522A: DB7 26, DB6 27, DB5 28, DB4 29, DB3 30, DB2 31, DB1 32, DBØ 33, RSØ 38, RS1 37, RS2 36, RS3 35, R/W 22, Ø2 25, RES 34, CS1 23, CS2 24, IRQ 21, PA6 8, PB6 16, Vcc 20 (+5V), GND 1, CB2 19, PA7 9, PB7 17, PBØ 10, PB1 11, FA3 5, PA5 7, PA2 4, PB2 12, PB3 13, PB4 14, PB5 15, PA4 6, PA1 3, PAØ 2, CA1 40, CA2 39

BLI.RATE — SH 6
FORCE BLANK — SH 6
OUT SPEAKER — SH 5
BLACK-ON-WHITE (BOW) — SH 6
BI.DIR.ENA — SH 5

A66 74LS367 (GND, +5V)
A65 74LS367 (GND, +5V)
A67 74LS367 (GND)
A68 74LS367 (GND)
RP4 RES. 1K (+5V)
RP1 RES 1K (+5V)
RP3 RES. 1K (+5V)
RP2 RES 1K (+5V)
S2
S1

SH 2 HSN
SH 6 C.CLK
SH 6 HSN

A69 74LS04
74LS00 A70
A64 74LS174
A71 74LS574
R40 1K
R44, 1K

CRTC RESET — SH 2,4

P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND

D5 1N4001
C72 22 uf
C71 22 uf
C2-5,9-14,16,17 31-33,37-39, .01 uf 49-54,58,59 69-6A,73,74
C1,7,8, 30,36 0.1 uf
C69 22 uf
C59 .01 uf
C58 .01 uf
C66 .01 uf
C67 .01 uf

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Cavallaro 9-27-84
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Cavallaro 9-29-84
		ANG. 2 PLC 3 PLC	ENGR
			APPD
		SCALE NONE	APPD
		MATERIAL	FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD.

SIZE | SHT 7 OF 7 | DRAWING NO. 2009800 | REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 40		
	A1	" " ECO 45		
	B	" " ECO 41,47		
	B1	" " ECO 54		
	B2	" " ECO 70,82	9/21/81	
	B3	" " ECO 0438,0442	9/15/82	
	C	ADD C76 ECO 2696	3/30/85	
	B5	PROD REL PER ECO 0483	12/20/84	
	B4	PROD REL PER ECO 0473	12/3/84	

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± 2 PLC ± .3 PLC ± .1
SCALE NONE
MATERIAL
FINISH

DWN O. Caballero 9-25-80
CHK O. Caballero 9-25-80
ENGR T. Scully 9/15/82
APPD
APPD
APPD

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD.

SIZE D | SHT 1 OF 7 | DRAWING NO. 120098-00 | REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 7 CRTC. RESET
SH 6 CCLK
SH 1 ABØ
SH 1 R/W
SH 1 DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
SH 1 IO.P.SEL
SH 1 Ø0
SH 1 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 DISP.MEM
SH 6 SEL.CPU.ADDR.

+5V
20 Vcc
2 RES
21 CCLK
24 RS
22 R/W
33 DBØ
32 DB1
31 DB2
30 DB3
29 DB4
28 DB5
27 DB6
26 DB7
25 CS
23 Ø2
1 Vss

A55 6545

39 HSYNC → HSN → SH 7
40 VSYNC → VSN → SH 4,6
18 DISPL.ENA → DISPL.ENA → SH 4
19 CURSOR → CURSOR → SH 4
38 RAØ
37 RA1
36 RA2
35 RA3
34 RA4/STB
4 MAØ
5 MA1
6 MA2
7 MA3
8 MA4
9 MA5
10 MA6
11 MA7
12 MA8
13 MA9
14 MA10
15 MA11
16 MA12
17 MA13

A63 74LS32 (13, 12 → 11)
A63 74LS32 (10, 9 → 8)

R25 1K → +5V

A46 74LS157 (SEL ← SEL.CPU.ADDR.)
- 1Y → DMEM.EN
- 2Y → AD.RAM.13
- 3Y → AD.RAM.12
- 4Y → SH 3

A45 74LS157 (SEL ← DM.R/W)
- 1Y → AD.RAM.11
- 2Y → AD.RAM.10
- 3Y → AD.RAM.9
- 4Y → AD.RAM.8 → SH 3

A44 74LS157 (SEL ← DM.R/W)
- 1Y → AD.RAM.7
- 2Y → AD.RAM.6
- 3Y → AD.RAM.5
- 4Y → AD.RAM.4 → SH 3

A43 74LS157 (SEL ← DM.R/W)
- 1Y → AD.RAM.3
- 2Y → AD.RAM.2
- 3Y → AD.RAM.1
- 4Y → AD.RAM.Ø → SH 3

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Ø Carrillo 9-24-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK Ø Carrillo	TITLE: PCB SCHEMATIC 950 CONT. BD.
			ENGR	
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE B SHT 2 OF 7 DRAWING NO 1200278-01 REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

A15 74LS42

SH 2 AQRAM 13 → 13 C
SH 2 AD·RAM·11 → 15 A
SH 2 AD·RAM·12 → 14 B
SH 6 QC·CLK → 12 D

4 1 9 7 6 5 4

A8 74LS04 (5 → 6)

A16 74LS32 (10, 9 → 8)

A16 74LS32 (5, 4 → 6)

SH 2 {
AD·RAM·10
AD·RAM·9
AD·RAM·8
AD·RAM·7
AD·RAM·6
AD·RAM·5
AD·RAM·4
AD·RAM·3
AD·RAM·2
AD·RAM·1
AD·RAM·Ø
}

A25 2114 — A26 2114 — A27 2114 — A28 2114

A34 6116 — A35 6116 — A36 6116 — A37 6116

SH 2 DM·R/W

SH 1 {
DB·7 → 11 B7
DB·6 → 12 B6
DB·5 → 13 B5
DB·4 → 14 B4
DB·3 → 15 B3
DB·2 → 16 B2
DB·1 → 17 B1
DB·Ø → 18 BØ
}

A14 8T245 (OE, DIR)

A7 → 9 CH·AD·7
A6 → 8 CH·AD·6
A5 → 7 CH·AD·5
A4 → 6 CH·AD·4
A3 → 5 CH·AD·3
A2 → 4 CH·AD·2
A1 → 3 CH·AD·1
AØ → 2 CH·AD·Ø

→ SH 4

SH 2 DMEN·EN → 19 OE
SH 1 R/W → 1 DIR

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Caballero 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON		CHK O. Caballero 9-25-80	
		ANG 2 PLC 3 PLC	ENGR	TITLE PCB SCHEMATIC 950 CONT. BD.
		SCALE NONE	APPD	
		MATERIAL	APPD	
			FINISH	SIZE SHT 3 OF 7 DRAWING NO 1000098-00 REV C

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
	B5	SEE SHT 1	

SH 3 CH·AD·7 CH·AD·6 CH·AD·5 CH·AD·4 CH·AD·3 CH·AD·2 CH·AD·1 CH·AD·Ø

A24 74LS374 — 1D 2D 3D 4D 5D 6D 7D 8D CLK OE; 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q

SH 7 CRTC·RES HSN

A60 74LS191 — PL CP D0 D1 D2 D3; TC RC Q0 Q1 Q2 Q3 U/D CE

SH 1 SCREG SEL. DB4 DB5 DB6 DB7

A61 74LS174 — CP MR D5 D2 D1 DØ; Q5 Q2 Q1 QØ; R38 1K +5V

SH 6 SHIFT.CLK
SH 6 DC CARRY
A13 74LS00

SH 2 VSN

A18 74LS173 — CLK SIR ID 2D 3D 4D M N; 1Q 2Q 3Q 4Q; +5V R14 1K; E5 E6

DEL·DISPL·ENA
DISPL·EN
A13 74LS00

A2 74LS04

SH 6 SHIFT·CLK
SH 6 ROW 9
A12 74LS04

SH 6 DISPL.ENA
A12 74LS04

A9 74LS00

A9 74LS00 — A29 74LS08

SH 6 VSYNC (VSN)

A19 74LS174 — 1D 2D 3D 4D CK CLR; 1Q 2Q 3Q 4Q

A30 74LS08

A30 74LS08

A30 74LS08

A20 74LS157 — SEL 1A 2A 3A 4A 1B 2B 3B 4B STRB; 1Y 2Y 3Y 4Y

A32 2332 — A11 A10 A9 A8 A7 A6 A5 A4 CS AØ A1 A2 A3; O1 O2 O3 O4 O5 O6 O7 O8

A33 2332 — A11 A10 A9 A8 A7 A6 A5 A4 CS AØ A1 A2 A3; O1 O2 O3 O4 O5 O6 O7 O8 VPP

+5V R19 1K
+5V R20 1K

74LS00 A11

SH 6 DC CARRY

A22 74LS166 — C D E F G H CK CK INH. LD CLR S.IN QH

+5V R16 1K

SH 2 CURSOR

RAØ SH 6
RA3 SH 6

+5V R17 1K

A23 74LS166 — A B C D E F G H CK CK.INH LD CLR S.IN QH

DOT SERIAL SH 6

A13 74LS00

C75 47pf

A12 74LS04

+5V R18 1K

A31 74LS74 — D CK PR CLR; Q

DEL CURSOR SH 6

A21 74S174 — 1D 2D 3D 4D 5D 6D CK CLR; Q1 Q2 Q3 Q4 Q5 Q6

+5V R15 1K

UNDERLINE
REVERSE·VIDEO
BLINK
BLANK
DEL.DISPL·EN–
HALF·INTENSITY
SH 6

P10-1

ROW·9 SH6
DISPL·EN– SH4

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN O. Cavallero 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK O. Cavallero 9-	TITLE: PCB SCHEMATIC 950 CONT. BD.
		ANG ± 2 PLC ± 3 PLC ±	ENGR	
		SCALE: NONE	APPD	
		MATERIAL	FINISH	SIZE C; SHT 4 OF 7; DRAWING NO. 120098-0C; REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 6 XTAL1

SH 1 IRQ, AB0, AB1, R/W, AB9, I.O.P.SEL, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, Φ2

SH 6 RESET

A49 6551 XL1 (+5V, 15; 1)

SH 1 AB11

A50 6551 XL1 (+5V, 15; 1)

SH 7 BI-DIR-ENA

SH 1 AB10

A51 6551 XL1 (+5V, 15; 1)

P3-8 DCD — R37 4.7K — A57 1489 — C63 330 PF

P3-6 DSR — R35 4.7K — C60 330 PF

P3-3 RxD — C61 330 PF

P3-5 CTS — R36 4.7K — C62 330 PF

P6-3 RxBOD — C34 330 PF

P4-4 RTS — E11 — E10 — R22 4.7K — C46 330 PF

P4-20 DTR — E13 — E12 — C48 330 PF

P4-2 TxD — R21 4.7K — C47 330 PF

P0-3 BEEP/TxD — P1-3 BEEPER — P6-13 SH 7 OUT SPEAKER

1489 A40

A68 74LS367

R42 330Ω — R41 750Ω — R43 330Ω — Q4 2N2219 — E25 — E24 — SP1

C41 330 PF — C40 330 PF — C22 .01UF — C23 .01 UF — +12V — GND — RxD

P7-1, P7-2, P0-4, P0-2, P0-1, P1-1, P1-2, P1-4

A68 74LS367 — E9 — E7 — E8

R27, 510Ω 1/2W — R30 510Ω 1/2W

P3-9, P3-14

A69 74LS04 — A70 74LS00 — 74LS08 A29

PIO-7,3 — PIO-5 — E36 — E37

PIO-11 — E38 — PIO-9 — E39

PIO-13 — P6-12

74LS32 A58 — A48 1488 — TxD MOD — TxD — P6-2, P3-2

C57 330 PF

74LS32 A58 — A39 1488 — DCD — P4-8

C43 330 PF

A58 — 74LS32 — C45 330 PF — RxD — P4-3

A39 1488 — C55 330 PF — DTR — P3-20

A48 1488 — C44 330 PF — CTS — P4-5

A39 1488 — A48 1488 — RTS — P3-4

C56 330 PF

A39 1488 — DSR — P4-6

C42 330 PF

A59 74LS157 STR

E40 → PIO-10

E41 → PIO-8

A48 1488 — E42 — E43 — PIO-6 — PIO-4 — PIO-2 — PIO-12 — P3-10

SIG. GND — P3-7

SIG. GND — P4-7

PROT. GND — P3-1

PROT. GND — P4-1

TxD1 (TTY) — P3-25

TxD2 (TTY) — P3-13

P3-12 RxD1 — P3-24 RxD2 — TIL 117 A47 — D3 IN914 — R26 100 KΩ — +5V R28 3.3K

A10 7406 — +5V R34 510Ω — Q3 2N2907A — R33, 68Ω — A56 4N38 — Q2 2N3019 — D4, IN914 — R32 511K — R31 4.7K

A38 74LS00

E29 — E30 — E31

RxC → PIO-14

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED	DWN: Carrillero 1/20/81
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK: Nuñez 8-23-82
		ANG ± 2 PLC 3 PLC	ENG:
		SCALE: NONE	APPD
		MATERIAL	FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT. BD.

SIZE D — SHT 5 OF 7 — DRAWING NO. 120098-00 — REV C

BUSHNELL GRAPHICS ACCUPRESS REORDER NO. A1-1-1/2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 2 RA Ø
SH 2 RA 3
SH 7 BLACK·ON·WHITE (B·O·W)
SH 4 BLINK
SH 7 BLI·RATE
BLANK
DOTS·SERIAL
ROW·9
UNDERLINE
SH 4 DEL CURSOR
REVERSE VIDEO
DEL DISPL·EN –
HALF·INTENSITY
SH 7 FORCE·BLANK
SH 2 VSN
SH 7 $\overline{HSN}$
SH 1 DISP·MEN
SH 1 IO·P·SEL
SH 1 AB13

74LS00 A11 · 74LS00 A11 · A2 74LS04 · 74LS00 A11 · 74LS00 A9 · 74LS00 A1 · 74LS86 A1 · 74LS86 A1 · A10 7406
A2 74LS04 · 74LS00 A9 · 74LS86 A1
A2 74LS04 · A1 74LS86
A10 7406 · A10 7406 · A10 7406 · A10 7406
A2 74LS04 · A1 74LS86
A2 74LS04
A12 74LS04 · A12 74LS04 · C9 0.01 µf · C76 68 pf · A13 74LS00 → $\overline{ROW\,9}$ SH 4
A16 74LS32
A2 74LS04
A2 74LS04
A8 74LS04 · A8 74LS04 · A8 74LS04
A5 74LS00 · A5 74LS00 · A5 74LS00 · A5 74LS00 · A7 74LS08

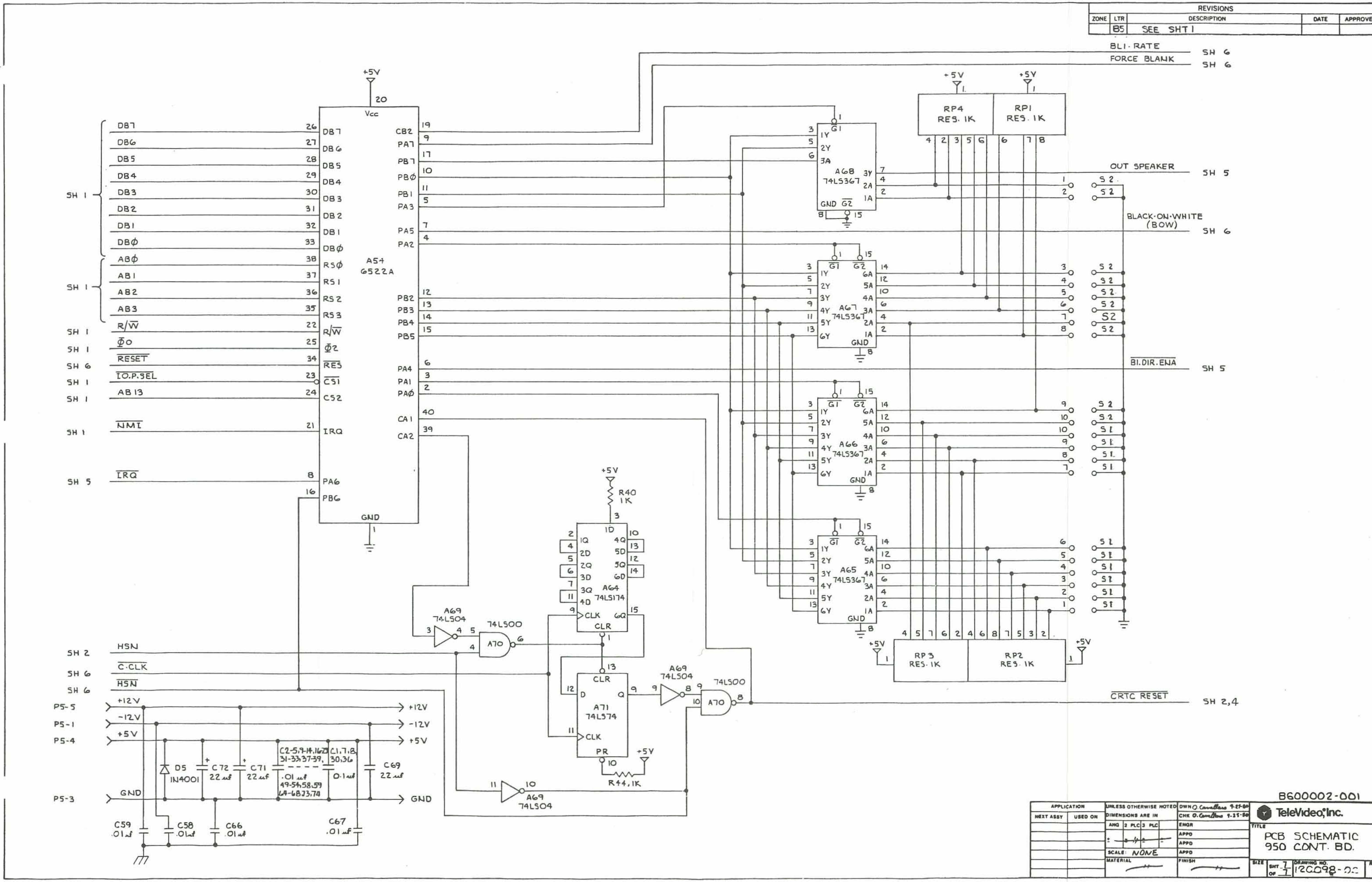
+5V R7 22Ω · R6 750Ω · R3 1K · R1 1K · R4 270Ω · R5 1K · R2 68Ω · C6 4.7 µf · D1 1N914 · Q1 2N2219 · E1 E2 E3 E4

+12V → P8-5, P8-6, P6-1, P6-14
+5V → P6-6, P6-9
-12V → P6-5, P6-10
GND → P6-7, P8-8, P8-9, P8-10
P2-4
P2-3
SH 4 COMP.V + TTL VIDEO → P2-6
+VSYNC ($\overline{VSN}$) → P2-5
+HSYNC. → P2-1
SEL·CPU·ADDR SH 2
DC.CARRY SH 4
C·CLK SH 2
$\overline{DC.CARRY}$ SH 4
$\overline{C.CLK}$ SH 7

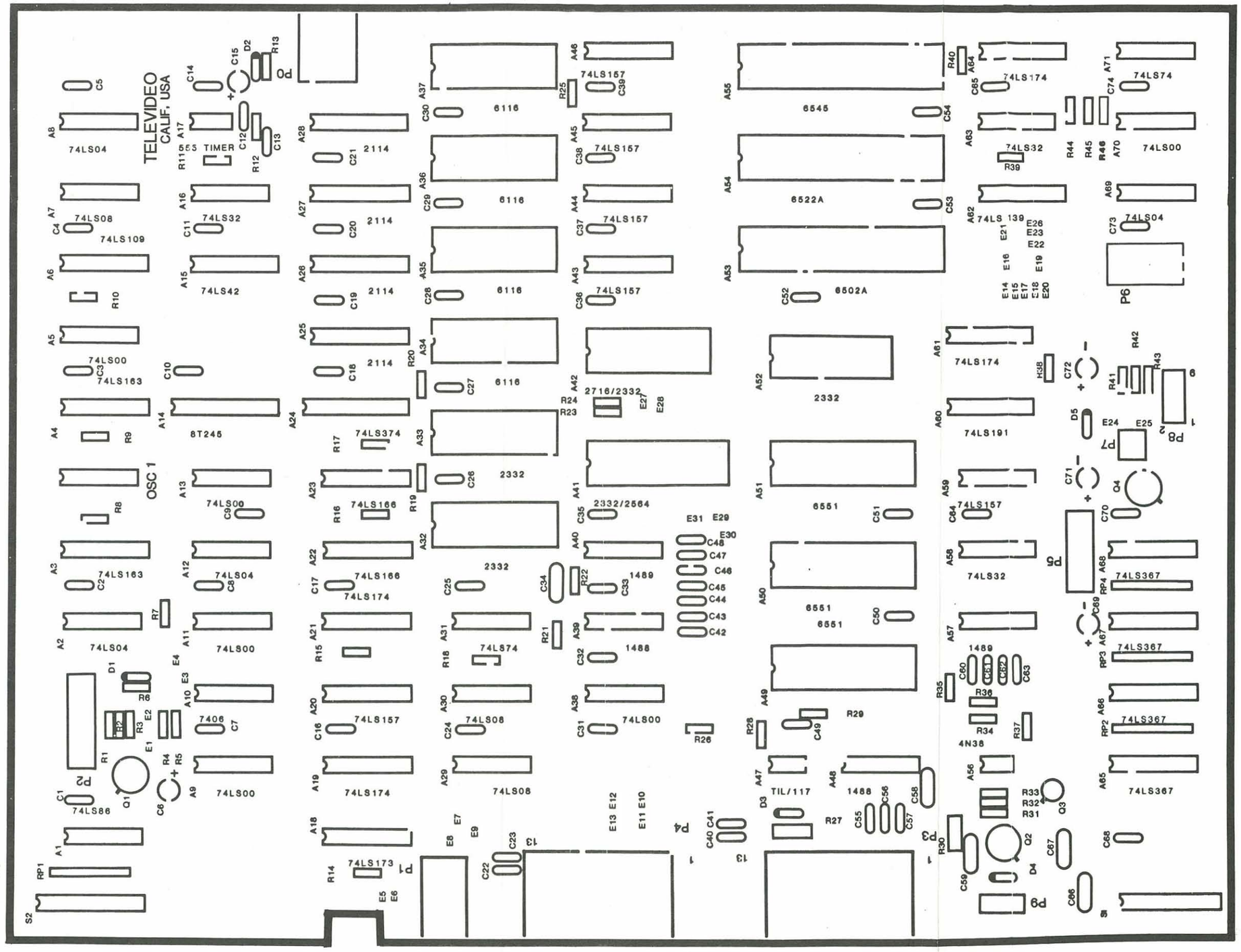
R8 1K · R9, 1K · R10, 1K
74LS163 A3 · 74LS163 A4
OSC. 1 K1114A 23.814 MHZ · E32 · E33
74LS109 A6 PR J Q CLK K CLR
R11 3.3K · R12 1M · R13 47K · 1N914 D2 · A17 555 TIMER · C13 .01µf · C12 .01µf · C15 10µf · R29 4.7K · C49 .01µf
$\overline{RESET}$ SH 1,5,7
Φ0 SH 1
SHIFT·CLK. SH 4
SHIFT·CLK SH 4
XTAL1 SH 3
$\overline{QC\ CLOCK}$ SH 3

B600002-001

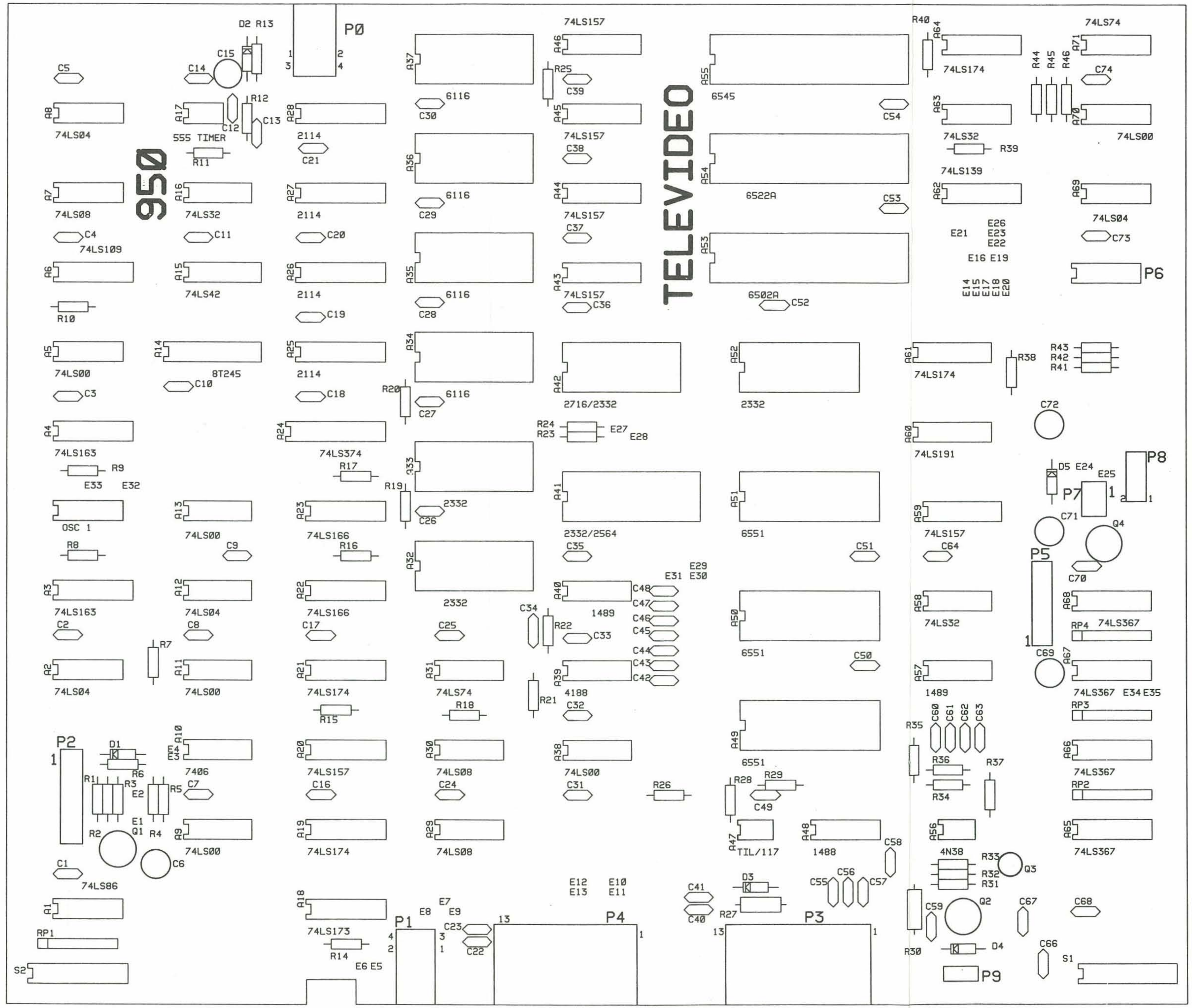
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Carvalho 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK O. Carvalho 9-25-80	TITLE: PCB SCHEMATIC 950 CONT. BD.
		SCALE: NONE	ENGR / APPD / APPD / APPD	
		MATERIAL	FINISH	SIZE · SHT 6 OF 7 · DRAWING NO. 120038-00 · REV C



REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B5 SEE SHT I
BLI. RATE SH 6
FORCE BLANK SH 6
OUT SPEAKER SH 5
BLACK-ON-WHITE (BOW) SH 6
BI.DIR.ENA SH 5
CRTC RESET SH 2,4
A54 6522A
A68 74LS367
A67 74LS367
A66 74LS367
A65 74LS367
A64 74LS174
A71 74LS74
A69 74LS04
A70 74LS00
RP4 RES. 1K
RP1 RES. 1K
RP3 RES. 1K
RP2 RES. 1K
R40 1K
R44, 1K
D5 1N4001
C72 22 uf
C71 22 uf
C69 22 uf
C2-5,9-14,16,23 31-33,37-39, .01 uf 49-54,58,59 61-68,73,74
C1,7,8, 30,36 0.1 uf
C59 .01 uf
C58 .01 uf
C66 .01 uf
C67 .01 uf
SH 1 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ
SH 1 ABØ AB1 AB2 AB3
SH 1 R/W
SH 1 Φ0
SH 6 RESET
SH 1 IO.P.SEL
SH 1 AB 13
SH 1 NMI
SH 5 IRQ
SH 2 HSN
SH 6 C.CLK
SH 6 HSN
P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND
B600002-001
TeleVideo, Inc.
PCB SCHEMATIC 950 CONT. BD.
SCALE: NONE
SHT 7 OF 7
120098-02
REV C



950
CONTROLBOARD
REV B


TELEVIDEO
950
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
S1
S2
RP1
RP2
RP3
RP4
74LS04
74LS08
74LS109
74LS00
74LS163
OSC 1
74LS86
555 TIMER
74LS32
74LS42
8T245
7406
2114
74LS374
74LS166
74LS174
74LS157
74LS173
6116
2332
74LS74
74LS08
2716/2332
2332/2564
1489
4188
6545
6522A
6502A
6551
1488
TIL/117
4N38
74LS174
74LS32
74LS139
74LS191
74LS367
74LS04
74LS00

PCB ASSEMBLY CONTROL BOARD

Part Number	Description	Location
120287-00	CAP CER .01uF 16V 20%	C2-5, 9-14, 16-29 31-33, 37-39, 49-54, 58, 59, 64-68, 73, 74
120257-00	CAP ELEC 22uF 16V +20%	C69, 71, 72
120291-00	CAP CER 330pF 50V 20%	C34, 40-48, 55-57, 60-63
120275-00	CAP TANT 4.7uF 16V 10%	C6
120273-00	CAP ELEC 10uF 16V 20%	C15
121868-00	CAP MONO .1uF 50V 20%	C1, 7, 8, 30, 36
120249-00	CAP MICA 47pF 500V +/-5%	C75
123013-00	CAP MICA 68pF 500V +/-5%	C76
120366-00	IC 74LS191	A60
120446-00	IC 74S174	A21
120270-00	IC 74LS109	A6
120242-00	IC 74LS00	A5, 9, 11, 13, 38, 70
120248-00	IC 74LS04	A2, 8, 12, 69
120348-00	IC 7406	A10
120252-00	IC 74LS08	A7, 29, 30
120258-00	IC 74LS32	A16, 58, 63
120266-00	IC 74LS74	A31, 71
120268-00	IC 74LS86	A1
120272-00	IC 74LS139	A62
120274-00	IC 74LS157	A20, 43-46, 59
120276-00	IC 74LS163	A3, 4
120278-00	IC 74LS166	A22, 23
120280-00	IC 74LS173	A18
120282-00	IC 74LS174	A19, 61, 64
120286-00	IC 74LS367	A65-68
120290-00	IC 74LS374	A24
120292-00	IC 75188	A39, 48
120294-00	IC 75189A	A40, 57
120298-00	IC TIL117 OPTP CPLR	A47
120350-00	IC 4N38 OPTO CPLR	A56
120358-00	IC 2114-1CB RAM 150ns	A25-28
120492-00	IC 6116 STAT RAM 2Kx8 150ns	A34-37
120496-00	IC 6502A CPU	A53
120528-00	IC 6545A-1 CRT CONTR	A55
121557-00	IC 6551 1MHZ UART	A49-51
120502-00	IC 6522A	A54
120362-00	IC 74LS245	A14
120352-00	CRY 23.8140 MHZ CLOCK OSC	OSC-1
180000-43	IC EPROM SYS 950 F000	A41
180000-02	IC ROM CHAR GEN UP	A33
180000-03	IC ROM CHAR GEN LOWER	A32
180000-44	IC EPROM SYS 950 E000	A42
120260-00	IC 74LS42	A15

PCB ASSEMBLY CONTROL BOARD
Continued

Part Number	Description	Location
120302-00	IC NE555 TIMER	A17
120317-00	RES CF 750 OHM 1/4W 5%	R6, 41
120323-00	RES CF 51K OHM 1/4W 5%	R32
120511-00	RES CF 68 OHM 1/4W 5%	R2, 33
120531-00	RES CF 4700 OHM 1/4W 5%	R21, 22, 29, 31, 35-
120513-00	RES CF 270 OHM 1/4W 5%	R4
120515-00	RES CF 330 OHM 1/4W 5%	R42, 43
120519-00	RES CF 510 OHM 1/4W 5%	R34
120521-00	RES CF 1000 OHM 1/4W 5%	R1, 3, 5, 8-10, 14-20, 23-25, 38, 40, 44
120527-00	RES CF 3300 OHM 1/4W 5%	R11, 28, 45, 46
120321-00	RES CF 100K 1/4W 5%	R26
120315-00	RES CF 1M OHM 1/4W 5%	R12
120427-00	RES PK 1K OHM 8 PIN SIP	RP1-4
120451-00	RES CF 510 OHM 1/2W 5%	R27-30
120335-00	RES CF 22 OHM 1/4W 5%	R7
120453-00	TRAN 2N2219A NPN SI	Q1, 4
120457-00	TRAN 2N3019 NPN	Q2
120459-00	TRAN 2N2907A PNP SI	Q3
120475-00	DIODE 1N914	D5
120477-00	DIODE 1N4001	D1-4
120968-00	SWITCH 10 POS DIP/20P SIDE ADJ	S1, 2
120337-00	RES CF 47K OHM 1/4W 5%	R13
120984-01	SOCKET 24P IC DIP	XA32-37, 41, 42, 52
120984-04	SOCKET 28P IC DIP	XA49-51
120984-02	SOCKET 40P IC DIP	XA 53-55
120988-02	CONN 4P HDR WT (5P/#2P OUT)	P2, 5
120979-00	CONN 4P MODULAR JK RJ11	P1
120988-00	CONN 2P STR WAF	P9
121808-00	INSUL PAD TRAN 3005-A LARGE	Q1, 2, 4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 0333		
	A2	PROD REL PER ECO 0395		
	B	REVISED PER ECO 0456		
	B1	" " ECO 0554		
	B2	" " " 0544		

ZONE	LTR	DESCRIPTION	DATE	APPD
B3		RECORD CHANGES PER ECO # 2010	3-1-83	

SH 6 — E19, E16, EX

E20 E18 E17 E15 E14 E19 E16

E44 E45

+5V R16 1K → CS/A11 (A20 2532, OE/CS, VCC, GND)

+5V R17 1K → E27 E28 → A12 (A25 2532, PD/PGM, VCC, VPP, GND, CS1, CS2)

A15 2332: CS, A11, AØ–A10, I/O1–I/O8

+5V R39 3.3K → SH 7 IRQ → 4 IRQ

+5V R38 3.3K → SH 7 NMI → 6 NMI

A11 6502A: ABØ–AB15, R/W, Φ2, DBØ–DB7, ΦØ, RESET

SH 4 ΦØ → 37 ΦØ

SH 7 RESET → 40 RESET

R23 3.3K → +5V

E21 E22 E23 E26

E23 → SH6

P11-8, P11-7, P11-5, P11-3

AB Ø, AB 1 — SH 2,5,7

AB 2, AB 3 — SH2,7

AB 4, AB 5, AB 6, AB 7 — SH2

AB8 — SH2,6

AB9, ABI0, ABI1 — SH2,5

ABI2 — SH2,6

ABI3 — SH2,6,7

ABI4, ABI5 — SH 6

R/W — SH2,3,5,6,7

P11-20

DBØ, DB 1, DB 2, DB 3 — SH 2,3,5,7

DB 4, DB 5, DB 6, DB 7 — SH 2,3,5,6,7

P8-1, P8-2, P8-3, P8-8, P8-7

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACITORS ARE VALUED IN µF, 16VDC, ±20%
3. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. 212730

B600002-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H HUR 3-8-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK	TITLE: PCB SCHEMATIC CONT. BD 950 G/A
2009501	—	SCALE:	ENGR	
		MATERIAL	APPD / APPD / APPD	SIZE D · SHT 1 OF 7 · DRAWING NO. 2009801 · REV B3
		FINISH		

2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	.	SEE SHT 1		

SH6 CRTC.RESET
SH4 CCLK
SH1 AB0, R/W
SH1 DB0–DB7
SH6 SEL CRTC
SH4 Ø0
SH1 AB1–AB7
SH1 AB8–AB11
SH1 AB12, AB13
SH6 DISP.MEM
SH6 SEL.CPU.ADDR

+5V → 20 VCC

A6 6545
2 RES, 21 CCLK, 24 RS, 22 R/W, 1 VSS, 3 LPEN, 33–26 DB0–DB7, 25 CS, 23 Ø2

HSYNC 39 → HSN → SH6
VSYNC 40 → VSN → SH4,6
ENABLE 18, CURSOR 19 → DISPL_ENA, CURSOR → SH4
RA0 38, RA1 37, RA2 36, RA3 35, RA4/STB 34 → P11-22, P11-23
MA0–MA13 4–17

A7 74LS157, A12 74LS157, A16 74LS157, A21 74LS157
1A 2A 3A 4A 1B 2B 3B 4B; EN 15; SEL B 1; 1Y 2Y 3Y 4Y 4 7 9 12

+5V → R11 4.7K

SH6 SEL.CPU.ADDR

DMEM.EN, AD.RAM.13, AD.RAM.12 → SH3
AD.RAM.11, AD.RAM.10, AD.RAM.9, AD.RAM.8 → SH3
AD.RAM.7, AD.RAM.6, AD.RAM.5, AD.RAM.4 → SH3
AD.RAM.3, AD.RAM.2, AD.RAM.1, AD.RAM.0 → SH3

APPLICATION		UNLESS OTHERWISE NOTED	DWN H HUR 3-8-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE: PCB SCHEMATIC CONT. BD 950 G/A
			APPD	
		SCALE:	APPD	
		MATERIAL	FINISH	SIZE D, SHT 2 OF 7, DRAWING NO 2009801, REV B3

B600002-002

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH2 AD.RAM.13
AD.RAM.11
AD.RAM.12
SH4 QC CLK

A2 74LS42 — C, A, B, D; Ø, 1, 2, 3, 4, 5, 6, 7, 8, 9

SH2 AD.RAM.10
AD.RAM.9
AD.RAM.8
AD.RAM.7
AD.RAM.6
AD.RAM.5
AD.RAM.4
AD.RAM.3
AD.RAM.2
AD.RAM.1
AD.RAM.Ø

A3, A8, A13, A17, A22 — 6116 (+5V, VCC, GND, WE, OE, CS, A0–A10, I/O1–I/O8)

SH6 DM.R/$\overline{W}$

SH1 DB.7
DB.6
DB.5
DB.4
DB.3
DB.2
DB.1
DB.Ø

A26 8T245 — B7–B0, A7–A0, $\overline{OE}$, DIR

SH2 $\overline{DMEN.EN}$
SH1 R/$\overline{W}$

CH.AD.7
CH.AD.6
CH.AD.5
CH.AD.4
CH.AD.3
CH.AD.2
CH.AD.1
CH.AD.Ø
→ SH4

DB.7 → P11-24
DB.6 → P11-18
DB.5 → P11-15
DB.4 → P11-16
DB.3 → P11-13
DB.2 → P11-12
DB.1 → P11-11
DB.Ø → P11-10

P5-5 +12V → +12V
P5-1 -12V → -12V
P5-4 +5V → +5V
P5-3 GND → GND

CR1 IN4001
C2 22 50V
C3 22 50V
C27~55 C57~68 .01
0.1
C1 22 50V
C69 .01
C70 .01
C71 .01
C72 .01

BE00002-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN HHUR 3-9-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK	TITLE: PC,B SCHEMATIC CONT. BD 950 G/A
2009501	—	SCALE:	ENGR	
		MATERIAL	APPD	
		FINISH	APPD	
			APPD	SIZE D · SHT 3 of 7 · DRAWING NO 2009801 · REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH3: CH.AD.7, CH.AD.6, CH.AD.5, CH.AD.4, CH.AD.3, CH.AD.2, CH.AD.1, CH.AD.Ø

A27 74LS374 (6D 3D 4D 5D 1D 8D 2D 7D; CLK; OE; 6Q 3Q 4Q 5Q 1Q 8Q 2Q 7Q)

SH6: RAØ, RA1, RA2, RA3

R18 4.7K +5V

A30 2332 (VPP VDD; A11 A10 A9 A8 A7 A6 A5 A4 CS; A0 A1 A2 A3; 01 02 03 04 05 06 07 08)

R19 4.7K +5V

A31 2332 (A0 A1 A2 A3 VPP; A11 A10 A9 A8 A7 A6 A5 A4 CS; VDD; 01 02 03 04 05 06 07 08)

OSC1 K1114A 23.814 MHZ A45 (+5V, pin 14, pin 7, pin 8)

E32, E33

C24 47PF 50V

R41 33

C23 20PF 50V

LCHADØ LCHAD1 LCHAD2 LCHAD3

CG15 CG14 CG13 CG12 CG11 CG10 CG9 CG8 CG7 CG6 CG5 CG4 CG3 CG2 CG1 CGØ

A34 GATE ARRAY I740012-008

CHAR LATCH OUT EN	33
LATCH CHAR	22
B.O.W.	36
CLOCK EXTEND	2
SHIFT CLOCK	17
ROW 9	23
VERT SYNC	24
HORIZ SYNC	25
DISP. EN	34
CURSOR	38
BLINK RATE	39

SH7 B.O.W.
SH6 CLOCK EXTEND
SH6 ROW 9
SH2 VERT SYNC
SH6 HORIZ SYNC
SH2 DISPLAY ENABLE
SH2 CURSOR
SH7 BLINK RATE

ØØ	1	ØØ → SH 1,2,5,6,7
XTAL I	18	XTAL I → SH5
CHAR CLOCK	19	CHAR CLOCK → SH2,6
QC CLOCK	21	QC CLOCK → SH3
COMPOSITE VIDEO	26	COMPOSITE VIDEO → SH6
HALF INTENSITY	28	HALF INTENSITY → SH6
VIDEO	37	VIDEO → SH6
VSS	20	

+5V → P6-6, P6-9, P11-1, P11-2

+12V → P6-1, P6-14, P8-5, P8-6, P11-6

-12V → P6-5, P6-10, P8-9, P8-10, P11-14

E36 → P11-25

P6-7, P6-8, P10-2, P10-12, P11-9, P11-19

SHIFT CLOCK → P11-21

P3-12 RXDI
P3-24 RX D2

CR3 IN914; TIL 117 A10; R40 100K

R15 3.3K +5V

A14 74LS00; A18 1488

R4 68 +5V

R5 510

4N38 A5

Q2 2N2907A

Q3 2N3019

CR2 IN914

R10 51K; R9 4.7K

SH5 TXD

SIG.GND → P3-10, P3-7, P4-7

PROT.GND → P3-1, P4-1

TXDI (TTY) → P3-25

TXD2 (TTY) → P3-13

+12V R1 510 → P3-9

R2 510 → P3-14

B600002-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN				OWN H HUR3-10-82	TeleVideo, Inc.
NEXT ASSY	USED ON		ANG	2 PLC	3 PLC	CHK Edward Hopper	
2009501	—		±	.x ±	.xx ±	ENGR	TITLE PCB SCHEMATIC CONT. BD 950 G/A
						APPD	
		SCALE				APPD	
		MATERIAL				FINISH	SIZE D SHT 4 OF 7 DRAWING NO 2009801 REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH4 XTAL 1
SH7 IRQ
SH1 AB0 AB1 R/W AB9
SH6 IO.P.SEL
SH1 DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
SH4 Ø
SH7 RESET
SH6 RXD
SH1 AB11
SH6 DTR
SH7 BI.DIR.ENA
SH1 AB10

A36 6551 (XL1): IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; RTS, RXD, TXD
A29 6551 (XL1): IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; DTR, RTS, TXD, RXC, DSR, DCD, RXD, CTS
A33 6551 (XL1): IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; RTS, TXD, DTR, DSR, DCD, RXD, CTS, RXC
A28 74LS157: 4B, 4A, 3B, 3A, SEL, 2B, 2A, 1B, 1A, STR; 4Y, 3Y, 2Y, 1Y
A9 1489 (A32): DCD (P3-8), DSR (P3-6), RXD (P3-3), CTS (P3-5), RXD MOD (P6-3), RTS (P4-4), DTR (P4-20), TXD (P4-2)
R12–R14, R20 4.7K; C8, C4, C9, C7, C13, C14, C18, C17 330PF 100V
A19 74LS32: BEEP/TXD (P0-3, P1-3), BEEPER (P6-13)
A19 74LS37
OUT SPEAKER (SH 7); R7 330, R6 330, R8 330; Q1 2N2219A
E25, E24, E7, E8, E9, E11, E10, E13, E12
C19 330PF 100V; C25 330 PF 100V; C74 .01; C73 .01
+12V, GND
P7-1, P7-2, P0-4, P0-2, P0-1, P1-1, P1-2, P9-1, P9-2, P1-4
RXD (MODEM), RXD (HOST) } SH6
P10-11, P10-9, P10-3,7, P10-5
P10-10, P10-8, P10-6, P10-4
A19, A24, A18, A23 1488
TXD, TXD MOD, DCD, RXD, DTR, CTS, RTS, DSR
C10, C15, C16, C6, C11, C5, C12 330 PF 100V
P10-13, P6-12, SH4, P3-2, P6-2, P4-8, P4-3, P3-20, P4-5, P3-4, P4-6
E29, E30, E31
P10-14

APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-12-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE: PCB SCHEMATIC CONT. BD 950 G/A
		SCALE:	APPD	
		MATERIAL	APPD	
		FINISH	APPD	SIZE D, SHT 5 OF 7, DRAWING NO. 2009801, REV B3

B600002-002

2009801 B3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH 4 CHAR CLOCK
SH 5 RXD (HOST)
RXD (MODEM)
SH 1 DB4
DB5
DB6
DB7
SH 2 HORIZ SYNC
SH 4 Ø0
SH 1 ABØ
SH 5 RTS
DTR
SH 7 CA2
SH 1 AB14
AB15
E23
R/W
AB12
AB13

+5V
40 VDD
VSS 20

A37 GATE ARRAY I740012-009

CHAR CLOCK	1	RXD	5
RXD (HOST)	3	I/O P SEL	29
RXD (MODEM)	4	SEL CPU ADD	2
DB4	8	HORIZ SYNC	23
DB5	10	ROW 9	6
DB6	12	RA Ø	9
DB7	14	RA 1	11
HORIZ SYNC	22	RA2	13
Ø0	16	RA3	15
ABØ	17	CLOCK EXT	37
RTS	19	DTR	18
DTR	21	CRTC RESET	25
CA2	24	DISP MEM	26
AB14	27	E19	31
AB15	28	E16	32
E23	30	DISP MEM R/W	34
R/W	33	SEL CRTC	36
AB12	35	EX	39
AB13	38		

RXD SH 5
I/O P SEL SH 5,7
SEL CPU ADDR SH 2
HORIZ SYNC SH 4,7
ROW 9
RA Ø
RA 1
RA2
RA3
CLOCK EXTEND
} SH 4
DTR SH 5
CRTC RESET SH 2,7
DISP MEM SH 2
E19
E16
} SH 1
DISP MEM R/W SH 3
SEL CRTC SH 2
EX SH 1

A39 9 8 7406 +5V R30 1K → +HSYNC → P2-1

A14 9 8 12 13 10 11 74LS00 → AXXX → P11-4

SH 7 FORCE BLANK
SH 4 HALF INTENSITY
SH 4 VIDEO
SH 4 COMPOSITE VIDEO
SH 2 VERT SYNC

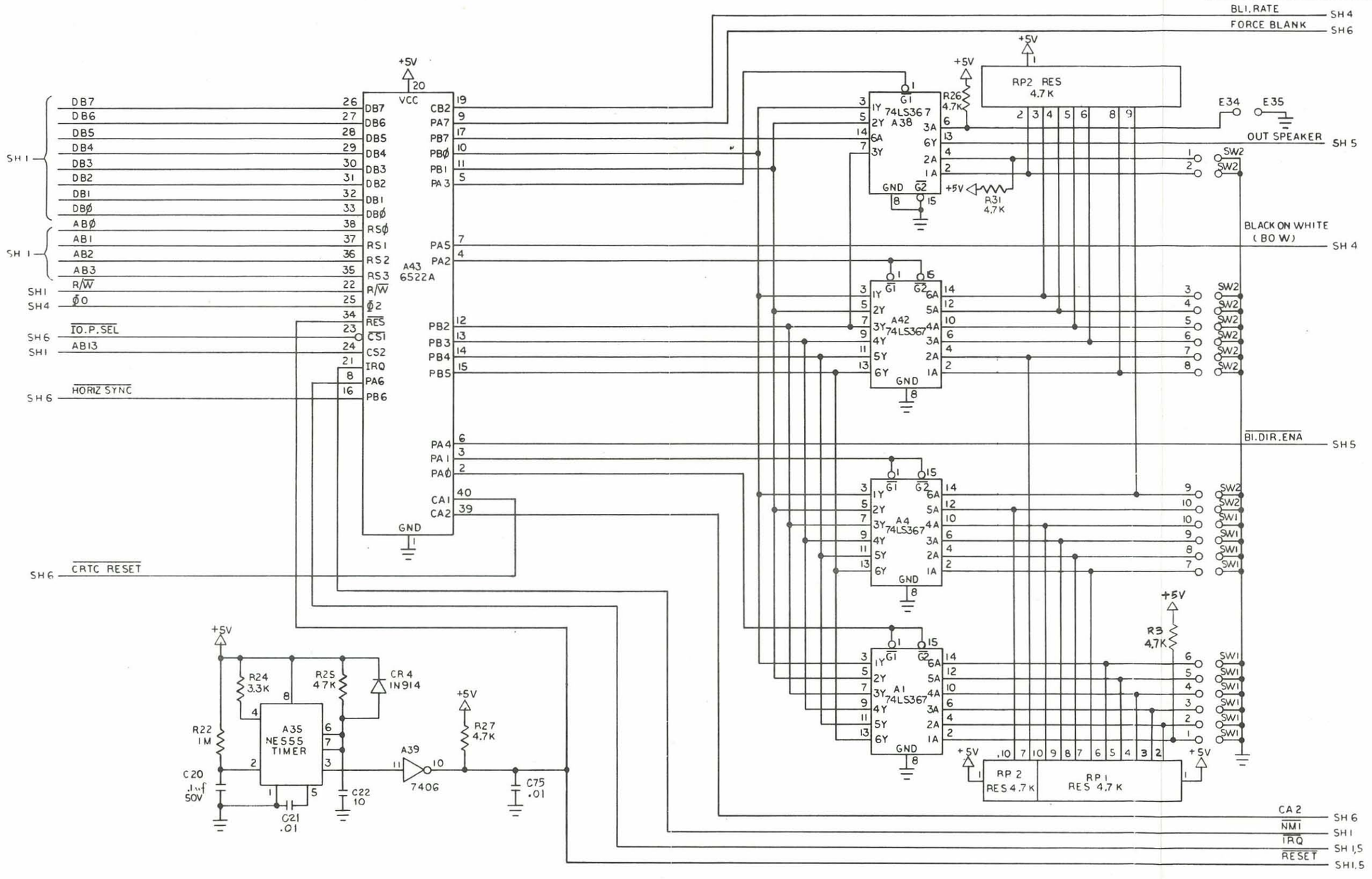
A39 5 6 7406 → P11-17
A39 3 4 7406 R28 1K → P11-26
+5V R36 22
R33 750
R34 1K
E1 E2
CR5 IN914
Q4 2N2219A
C26 4,7µF
R32 270
E3
E4
R35 68
R37 1K
→ P2-4
→ P2-3
A39 1 2 7406 → COMP. V + TTL VIDEO → P2-6
A39 13 12 7406 R29 1K → +VSYNC (VSN) → P2-5

B600002-00

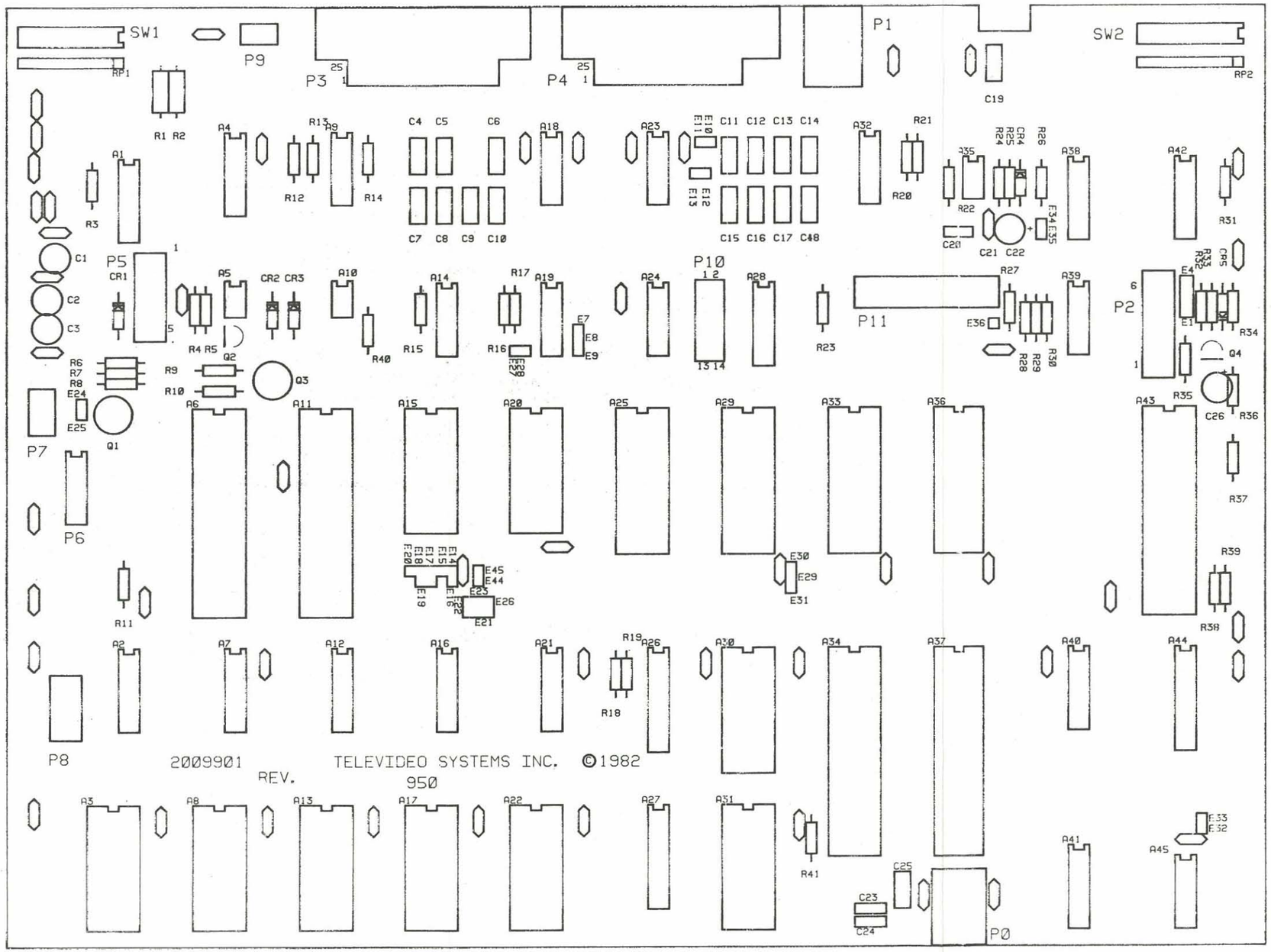
APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-17-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE
		± ± ± ±	APPD	PCB SCHEMATIC
		SCALE	APPD	CONT. BD 950 G/A
		MATERIAL	APPD	
			FINISH	SIZE D SHT 6 OF 7 DRAWING NO 2009801 REV B3

B3 2009801

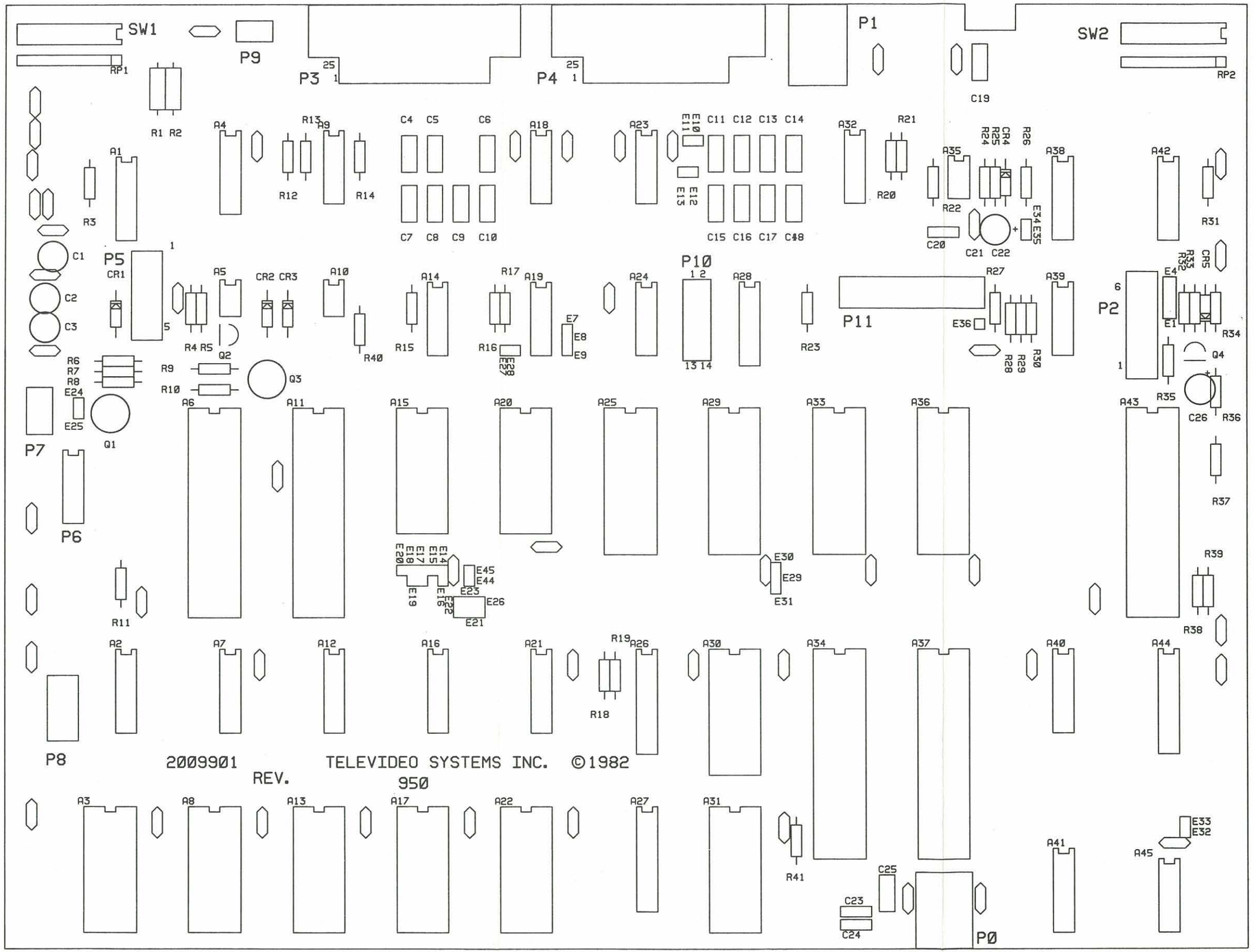
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H HUR 3-15-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC	CHK	
2009501	—		ENG	TITLE
			APPD	PCB SCHEMATIC
		SCALE	APPD	CONT. BD 950 G/A
		MATERIAL	FINISH	SIZE D SHT 7 of 7 DRAWING NO 2009801 REV B3



950 GATE ARRAY
CONTROL BOARD
REV B



TELEVIDEO 950-G SILKSCREEN

PCB ASSEMBLY CONTROL BOARD GATE ARRAY

Part Number	Description	Location
120275-00	CAP TANT 4.7uF 16V 10%	C26
120301-00	CAP CER .1uF 50V 10%	C20
120287-00	CAP CER .01uF 16V 20%	C27-55, 57-75
120273-00	CAP ELEC 10uF 16V 20%	C22
120293-00	CAP MONO 330pF 100V 20%	C4-19, 25
120261-00	CAP ELEC 22uF 35V 20%	C1, 2, 3
120289-00	CAP MONO .01uF 50V 10%	C21
120249-00	CAP MICA 47pF 500V +/-5%	C76
120286-00	IC 74LS367	A1, 4, 38, 42
120260-00	IC 74LS42	A2
120492-00	IC 6116 STAT RAM 2Kx8 150ns.	A3, 22
120350-00	IC 4N38 OPTO CPLR	A5
120528-00	IC 6545A-1 CRT CONTR	A6
120274-00	IC 74LS157	A7, 12, 16, 21, 28
120294-00	IC 75189A	A9, 32
120298-00	IC TIL117 OPTP CPLR	A10
120496-00	IC 6502A CPU	A11
120242-00	IC 74LS00	A14
180000-43	IC EPROM F000 SYS	A25
120292-00	IC 75188	A18, 23
120258-00	IC 74LS32	A19, 24
120362-00	IC 74LS245	A26
120290-00	IC 74LS374	A27
120530-00	IC SY6551A/1 2MHZ	A29, 33, 36
130237-00	IC G/A	A34
120578-00	IC G/A (B)	A37
120302-00	IC NE555 TIMER	A35
120348-00	IC 7406	A39
120502-00	IC 6522A	A43
130217-00	CRY CLK OSC 23.814 MHZ	A45
180000-44	IC E000 EPROM SYS	A20
180000-02	IC ROM CHAR GEN UP	A31
180000-03	IC ROM CHAR GEN LOWER	A30
120984-02	SOCKET 40P IC DIP	XA6, 11, 34, 37, 43
120984-04	SOCKET 28P IC DIP	XA29, 33, 36
120984-01	SOCKET 24P IC DIP	XA3, 8, 13, 15, 17, 20, 22, 25, 30, 31
120984-03	SOCKET 14P IC DIP	P6
120968-00	SWITCH 10 POS DIP/20P SIDE ADJ	SW1, 2
121653-00	CONN 25P PCB D-SUB MTL	P3, 4
120979-00	CONN 4P MODULAR JK RJ11	P1
120988-02	CONN 4P HDR WT (5PW/#2P OUT)	P2, 5
121808-00	INSUL PAD TRAN 3005-A LARGE	Q3
120521-00	RES CF 1000 OHM 1/4W 5%	R16, 17, 28-30, 34, 37
120513-00	RES CF 270 OHM 1/4W 5%	R32
120317-00	RES CF 750 OHM 1/4W 5%	R33

PCB ASSEMBLY CONTROL BOARD GATE ARRAY
Continued

Part Number	Description	Location
120335-00	RES CF 22 OHM 1/4W 5%	R36
120511-00	RES CF 68 OHM 1/4W 5%	R4, 35
120527-00	RES CF 3300 OHM 1/4W 5%	R15, 23, 24, 38, 39
120531-00	RES CF 4700 OHM 1/4W 5%	R3, 9, 11-14, 18-21, 26, 27, 31
120315-00	RES CF 1M OHM 1/4W 5%	R22
120321-00	RES CF 100K OHM 1/4W 5%	R40
120451-00	RES CF 510 OHM 1/2W 5%	R1, 2
120323-00	RES CF 51K OHM 1/4W 5%	R10
120515-00	RES CF 330 OHM 1/4W 5%	R6-8
120413-00	RES PK 4.7K OHM 10P SIP	RP1, 2
120337-00	RES CF 47K OHM 1/4W 5%	R25
120519-00	RES CF 510 OHM 1/4W 5%	R5
120477-00	DIODE 1N4001	CR1
120475-00	DIODE 1N914	CR2-5
120453-00	TRANS 2N2219A NPN SI	Q1, 4
120457-00	TRANS 2N3019 NPN	Q3
120459-00	TRANS 2N2907A PNP/SI	Q2

VIDEO MONITOR/POWER SUPPLY SCHEMATICS AND PARTS LIST

VIDEO MONITOR

The video monitor contains two sections: the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam, which is generated by the CRT electron gun, sweeps across and down the screen to create scan lines (see section on character generation). The beam's movement is driven by vertical and horizontal sweep rates, which are determined by the display circuitry on the logic board. The horizontal sweep is approximately 16 KHz, the vertical sweep 60 Hz for domestic and 50 Hz for European applications.

The horizontal synch pulses coming into the video monitor are inverted and amplified by transistor Q301. This signal is then coupled across the drive transformer T301 and applied to the base of the ouptut transistor Q302. Q302's output drives both horizontal yoke windings, as well as the step-up transformer that produces the anode voltage and the grid voltage for the CRT grid in the neck of the CRT. Since high-frequency magnetic fields are produced and then broken, the flyback transformer is necessary to provide high voltages for the horizontal scans.

These horizontal scans start in the upper left corner and scan across to the upper right corner. Once the scan reaches the end of the line, a blank appears where the video beam is turned off and retraced to the beginning of the next scan line.

The vertical synch pulses coming into the video monitor are converted to a sawtooth waveform. Initially, this pulse goes from a negative leading edge to a positive falling edge and passes through transistor Q202, which inverts it to its usable form.

At that point, the pulse goes from a +2-volt leading edge to a -2.5-volt falling edge. Timing is critical since 250 horizontal scan lines (which comprise the total number of horizontal scan lines on the CRT) occur within one sawtooth pulse. Therefore, the sawtooth pulse has to be proportional to all previous pulses or the timing will be off for the vertical as well as the horizontal sweep.

When the vertical sweep is negative, Q201 conducts and C202 discharges. During the positive portion, Q201 cuts off and allows C202 to charge. While C202 is charging, the electron beam scans.

The vertical sweep scans from top to bottom. Once it reaches the bottom of the page, a blank occurs when the video beam is turned off and is retraced to the top of the screen. At that point, C202 discharges. After the retrace, the beam turns off again and begins its scan routine.

Adjusting SFR1 (vertical height) and SFR2 (vertical linearity) changes the rate of C202's charge, and therefore the slope of the sawtooth pulse.

POWER SUPPLY

Voltages are created and regulated as follows: A 9.8 AC voltage is rectified by diodes D105 and D108, resulting in a 9-volt output. These 9 volts are then filtered through C117 and applied at the 5-volt regulator IC2.

The raw AC voltages for the positive and negative 12 DC voltage are derived from the center top of the secondary winding of D101. The diodes D101 and D102 form a full-wave rectifier that converts the 37-volt AC waveform to a 20-volt DC level. This DC voltage is then filtered by C116 and stabilized to -12 volts by a zener-regulated circuit that consists of a resistor (R102) and the zener diode (D112).

Diodes D103 and D104 also form a full-wave rectifier that converts the 37-volt AC waveform to a +20-volt DC level.

This DC voltage is filtered by C113 and applied to the 13.8-volt regulator IC1. The 13.8 output, in turn, is dropped 1.6 volts across diodes D113 and D114 to achieve the desired +12 volts DC.

A 79-volt AC waveform is applied to the half-wave rectifier D109, which is filtered by C119. The resulting 95-volt DC level is then regulated by a series voltage regulator. The reference element is the positive 12-volt zener diode D111. The sensing and control elements are transistors Q103 and Q102.

The high voltages needed to drive the CRT tube V501 are derived from the flyback transformer T302 on the video module.

TUBE SPECIFICATION

12 INCH 90 DEGREE, HIGH RESOLUTION

DISPLAY TUBE

310KGB 31

The 310KGB31 is a 12 inch 90 degree high resolution, rectangular display tube primarily intended for use as a alpha-numerical and graphic display tube for computer peripheral devices. The tube is provided with banded type integral implosion protection (with mounting lugs). The tube features a low reflectance high contrast screen.

ELECTRICAL DATA

Heating	
Indirect by AC or DC:	
Heater voltage	12.0 volts
Heater current	75 nA
Focusing Method	Electrostatic
Deflection Method	Magnetic
Deflection Angles (Approx.)	
Diagonal	90 degrees
Horizontal	78 degrees
Vertical	61 degrees
Anode voltage	15,000 max. volts 8,000 min. volts

Using high voltage with this tube internal flash-overs may occur, which may cause damage to the cathode of the tube and to various circuit components on the video monitor board. Therefore it is necessary to provide protective circuits using spark-gaps etc. These should be connected as illustrated in figure #1 below.

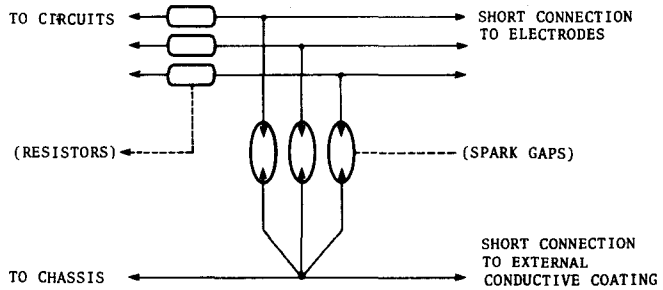


Figure 1.

No other connections between external conductive coating and chassis are permissible.

OPTICAL DATA

Faceplate	Filterglass
Anti-reflection treatment	No
Screen	Aluminized
Appearance	Low Reflective

A:
The dark-colored screen, in combination with the filterglass, produces the low reflectivity (equivalent to a 20% light transmission filterglass) for easy-to-see display.

MECHANICAL DATA

Tube Dimensions:

Overall length	278.8 max. mm
Greatest dimensions of tube (excluding lugs)	
Diagonal	318.5 +/- 2.7 mm
Width	279.6 +/- 2.7 mm
Heigth	218.7 +/- 2.7 mm
Useful screen dimensions (projected)	
Diagonal	295.0 min. mm
Width	257.0 min. mm
Heigth	195.0 min. mm

Pin Position Alignment	Pin No 5 aligns approx. with anode contact.
Operating Position	Any
Weight (approx.)	3.2 kg
Implosion Protection	Tension band (with mounting lugs)

GENERAL CONSIDERATIONS:

1. Tube handling. Care should be taken not to scratch the tube.

2. Impact. The tubes should never be exposed to impacts of more than 30G during handling or transportation.

3. Grounding. The external conductive coating of the tube should be grounded with multiple contacts (e.g. a contact plate having many fingers.) Poor contact might cause local heating resulting in tube leakage.

WARNING

SHOCK HAZARD:

The high voltage at which the tube is operated may be very dangerous. Design of the equipment should include safeguards to prevent the user from coming in contact with the high voltage. Extreme care should be taken in the servicing or adjustment of any high voltage circuit.

Caution must be exercised during the replacement or servicing of the tube since a residual electrical charge is stored within the tube. Before handling the tube remove any undersible residual high voltage charge from the tube, by shorting the anode contact button to the frame of the terminal as illustrated in figure #2. Discharging the high voltage to isolated metal parts sucha as cabinets and control brackets may produce a shock hazard.

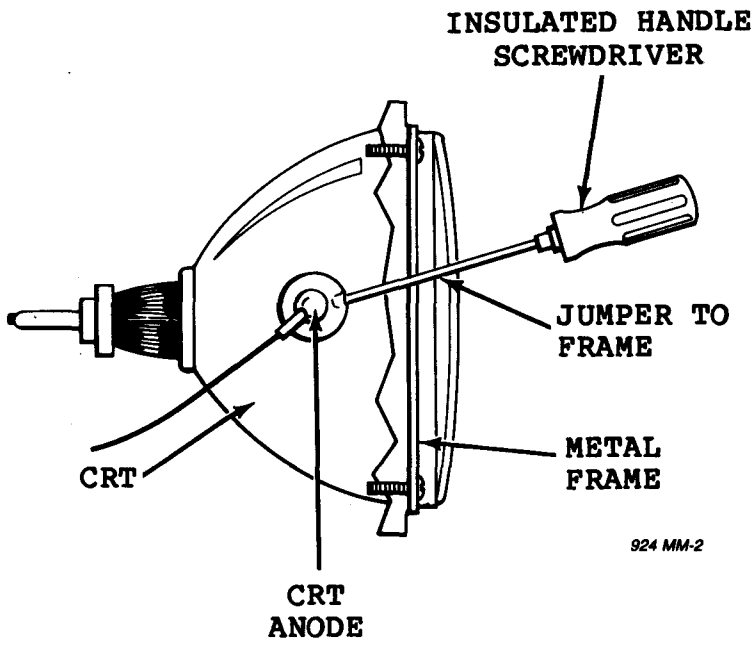
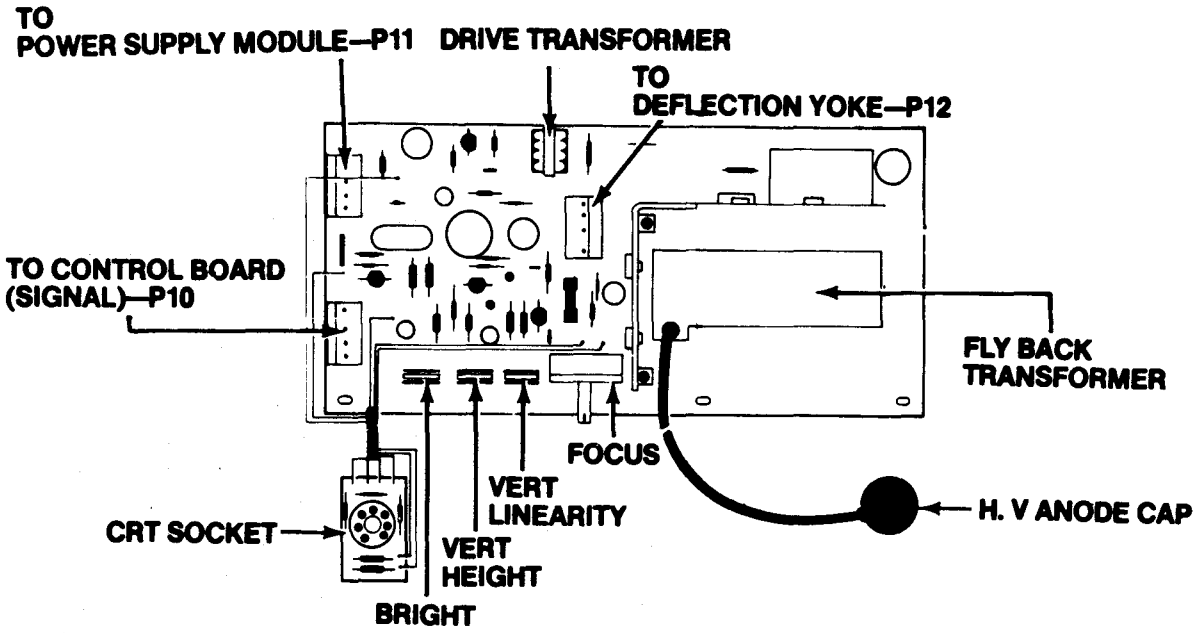
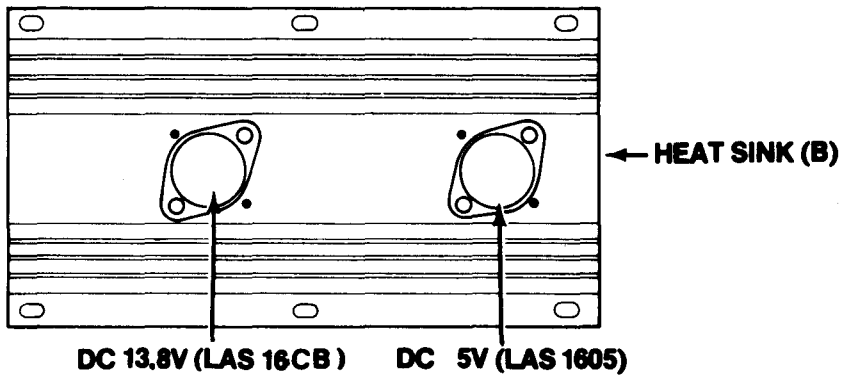
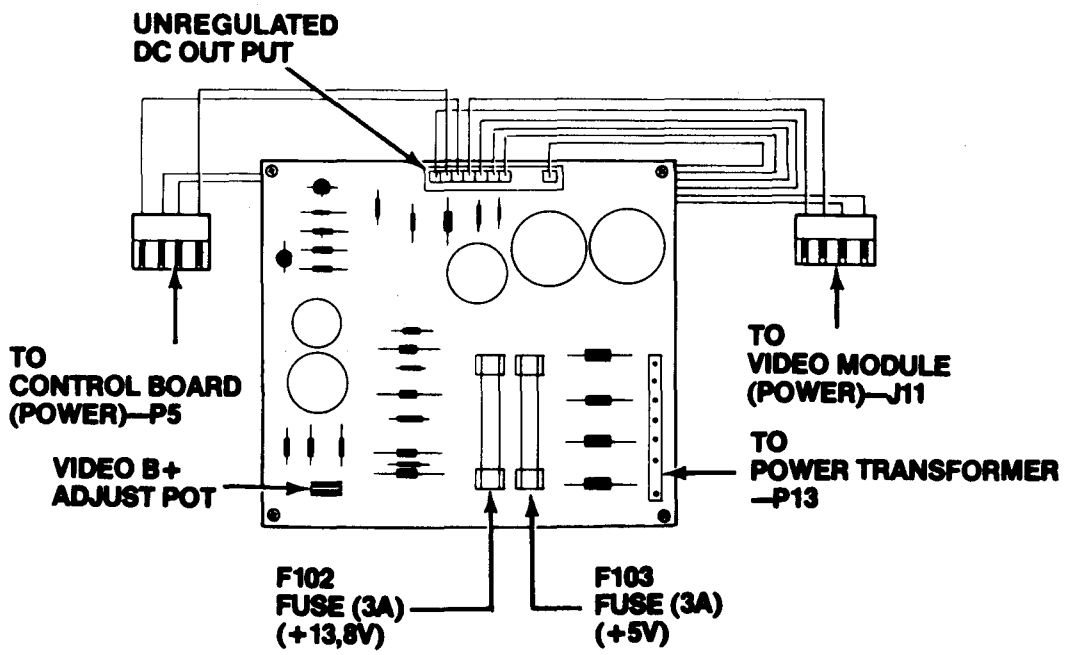


Figure 2.



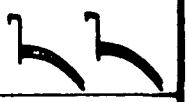
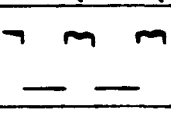
VIDEO MONITOR MODULE





POWER SUPPLY MODULE

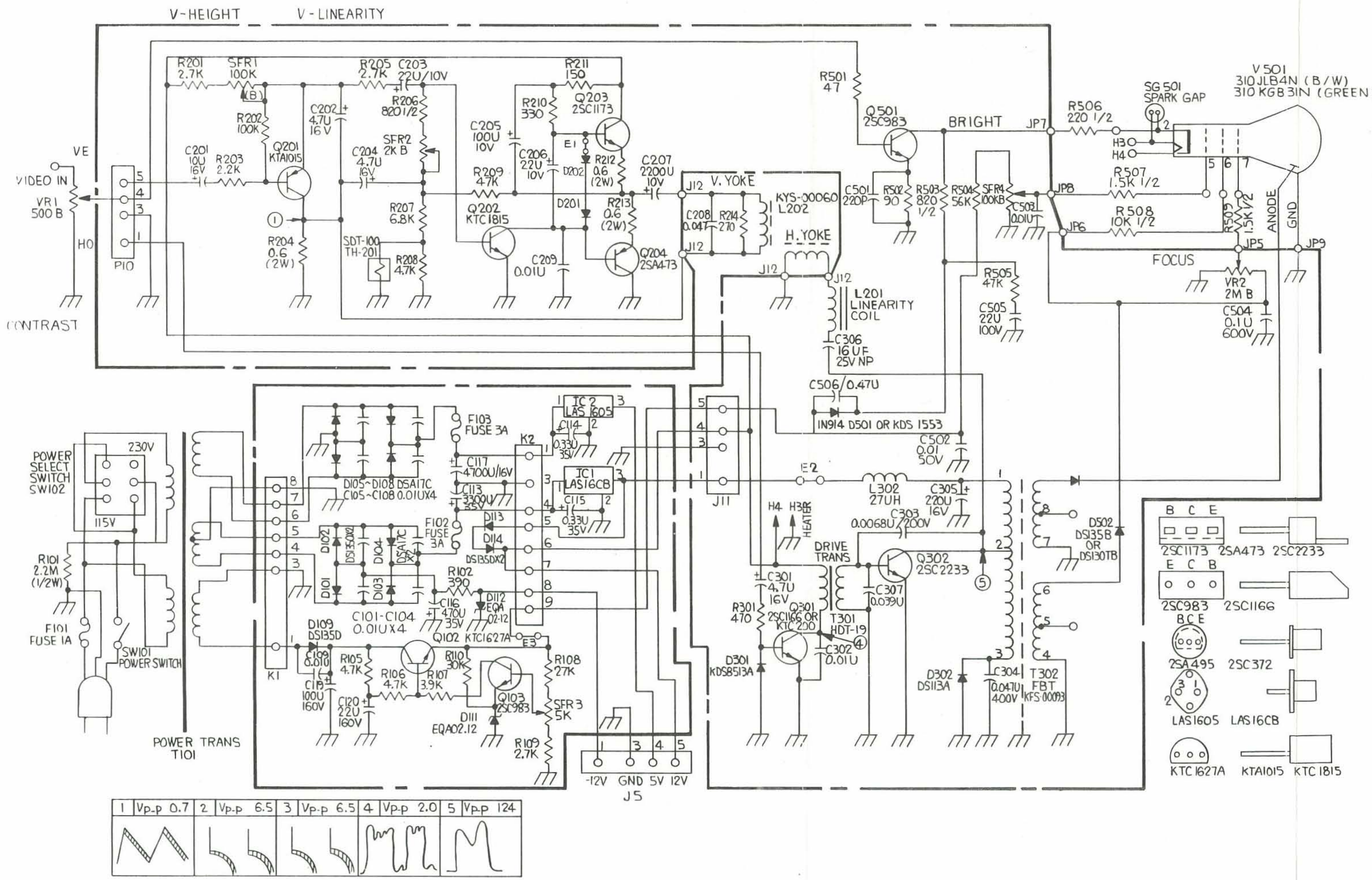
TR WAVEFORM and VOLTAGE

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC)	LAS1512	Regulation	12	2.5		12	0.0		0.0	0.0	
(IC)	LAS1605	〃		1.6		5	0.0		0.0	0.0	
(IC)	LAS1812	〃		0.1		-12	0.0		0.0	0.0	
(IC)	LAS16CB	〃		1.4		13.8	0.0		0.0	0.0	
Q102	2SC509	〃	78.7	0.0		86.4	1.5		98.0	0.0	
Q103	2SC983	〃	12.0	0.0		75.7	0.0		11.9	0.0	
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0		8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0		8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	
Q501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

ZONE	LTR	DESCRIPTION	DATE	APPROVED
REVISIONS				



1. ALL RESISTANCE VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD $U=10^{-6}$ $P=10^{-12}$
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENT OR PARTIAL SCHEMATIC DIFFERENCE BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

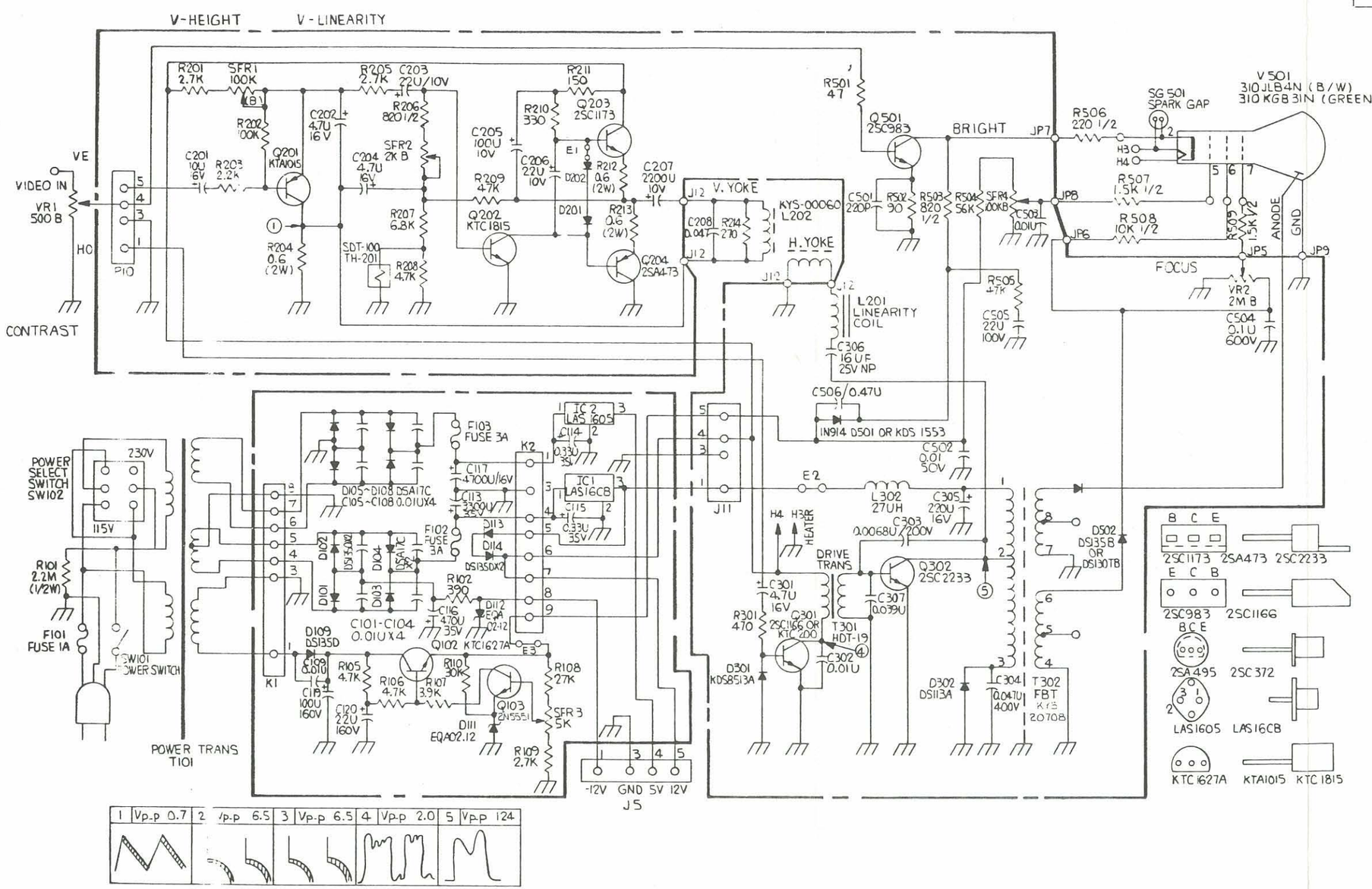
DWG NO. 2281900 SH 1 REV

PARTS LIST

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN 2/8/83	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK	TITLE PCB SCHEMATIC DIARAM POWER SUPPLY VIDEO MONITOR
			ENGR S.M. Kim	
		SCALE:	APPD	
		MATERIAL	FINISH	SIZE D SHT 1 OF 1 DRAWING NO. 2281900 REV

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REMOVED C207 PER ECC 2243	[illegible]	[illegible]
	A1	T302 WAS KSF0CC93 ECO 2557	[illegible]	[illegible]



1	2	3	4	5
Vp-p 0.7	Vp-p 6.5	Vp-p 6.5	Vp-p 2.0	Vp-p 124

1. ALL RESISTANCE VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD U=10^{-6} P=10^{-12}
3. UMLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENT OR PARTIAL SCHEMATIC DIFFERENCE BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

PARTS LIST

QTY PER UNIT	ITEM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± PLC ± PLC
SCALE
MATERIAL
FINISH

DWN HHW 2/8/83
CHK
ENGR S.H.K.in 4/21/83
APPD
APPD
APPD

TeleVideo, Inc.

TITLE
PCB SCHEMATIC DIAGRAM
POWER SUPPLY VIDEO
MONITOR 910-950/300

SIZE	DWT OF	DRAWING NO	REV
D	1	122813-00	A

PCB ASSEMBLY VIDEO MONITOR

Part Number	Description	Location
120383-00	RES CF 2.7K OHM 1/4W +/- 5%	R201, 205
120321-00	RES CF 100K OHM 1/4W 5%	R202
120387-00	RES CF 2.2K OHM 1/4W 5%	R203
121771-00	RES WW .6 OHM 2W	R204, 212, 213
121862-00	RES CF 820 OHM 1/2W 5%	R206, 503
120391-00	RES CF 6.8K OHM 1/4W 5%	R207
120531-00	RES CF 4700 OHM 1/4W 5%	R208
120337-00	RES CF 47K OHM 1/4W 5%	R209, 505
120515-00	RES CF 330 OHM 1/4W 5%	R210
120339-00	RES CF 150 OHM 1/4W 5%	R211
120513-00	RES CF 270 OHM 1/4W 5%	R214
120517-00	RES CF 470 OHM 1/4W 5%	R301
120377-00	RES CF 47 OHM 1/4W +-5%	R501
121776-00	RES CF 90 OHM 1/4W	R502
120395-00	RES CF 56K OHM 1/4W 5%	R504
121860-00	RES CF 220 OHM 1/2W 5%	R506
121863-00	RES CF 1.5K OHM 1/2W 5%	R507, 509
121864-00	RES CF 10K OHM 1/2W 5%	R508
121777-00	POT TRIM 100K SIDE ADJ	SFR1, 4
121778-00	POT TRIM VERTICAL LINEARITY	SFR2
121779-00	POT TRIM 5K OHM SIDE ADJ	SFR3
121802-00	POT CONTRAST	VR1
121801-00	POT FOCUS 2M OHM	VR2
121803-00	THERMISTOR 1K OHM	TH201
120273-00	CAP ELEC 10uF 16V 20%	C201
120275-00	CAP TANT 4.7uF 16V 10%	C202, 204
120257-00	CAP ELEC 22uF 16V +20%	C203
121960-00	CAP ELEC 100uF 10V +/- 20%	C205
121961-00	CAP ELEC 22uF 100V	C206, 505
121962-00	CAP ELEC 2200uF 10V	C207
121971-00	CAP MYLAR .47uF 50V	C208
121967-00	CAP ELEC 4.7uF 16V	C301
121970-00	CAP MYLAR .01uF 50V	C302
121968-00	CAP MYLAR .0068uF 200V	C303
121975-00	CAP MYLAR .47uF 400V	C304
121993-00	CAP ELEC 220uF 16V	C305
122800-00	CAP ELEC 16uF 25V (NON-P)	C306
120305-00	CAP MONO .039uF 50V 5%	C307
121959-00	CAP CER 220pF 50V	C501
120289-00	CAP MONO .01uF 50V 10%	C503
121973-00	CAP MYLAR .1uF 600V	C504
121972-00	CAP MYLAR .47uF 50V	C506
120309-00	CAP CER 1.0pF 1KV SPARK GAP	SG501
122022-00	DIODE 1N4004 MOT	D502
122018-00	DIODE 1N920/KD8513A	D201, 202, 301

PCB ASSEMBLY VIDEO MONITOR
Continued

Part Number	Description	Location
122008-00	YOKE DEFLECT W/CONN KYS-00060	L202
122009-00	COIL LINEARITY NON ADJ LC-36	L201
122010-00	COIL INDCTR 27uH .3PIE	L302
122012-00	TNFR HORIZ DR HDT-19	T301
130745-00	TNFR FLYBACK KYS-20708	T302

PCB ASSEMBLY POWER SUPPLY

Part Number	Description	Location
120287-00	CAP CER .01uF 16V 20%	C101-109
120383-00	RES CF 2.7K OHM 1/4W +/-5%	R109
120393-00	RES CF 30K OHM 1/4W 5%	R110
120467-00	TRAN KTC1627/MPSA06 NPN	Q102
120471-00	TRAN 2N5551 NPN HIGH VOLTAGE	Q103
120531-00	RES CF 4700 OHM 1/4W 5%	R105, 106
121268-00	VOLT REG LAS 1605 2A/5V	IC2
121269-00	VOLT REG LAS 16CB 2A/13.8V	IC1
121373-00	RES CF 27K OHM 1/4W +/-5%	R108
121766-00	RES CF 390 OHM 1/2W 5%	R102
121774-00	RES CF 3.9K OHM 1/4W	R107
121779-00	POT TRIM 5K OHM SIDE ADJ	SFR3
121931-00	FUSE 3 AMP 125V 3AG	F102, 103
121963-00	CAP ELEC 100uF 160V	C119
121964-00	CAP ELEC 22uF 160V	C120
121965-00	CAP ELEC 3300uF 35V	C113
121966-00	CAP ELEC 4700uF 16V	C117
121981-00	CAP TANT .33uF 35V	C114, 115
121982-00	CAP 470uF 35V	C116
122006-00	DIODE 1N5391/DS135D	D101-108, 113, 114
122014-00	DIODE DS18/1DS135D	D109
122016-00	DIODE 1N759A/RD12EB ZENER	D111, 112

TERMINAL TROUBLESHOOTING GUIDE

1. INTRODUCTION

This is a general troubleshooting guide to be used with the Operator's Manual, Maintenance Manual, and Service Bulletins as required. By following the procedures described here, you should be able to quickly isolate and repair most field failures.

The following sections are included:

2. OVERVIEW OF TERMINAL MODULES

The design of TeleVideo® terminals permits fast fault isolation since the terminal hardware is divided into four main modules:

1. Video monitor
2. Power supply
3. Main logic board
4. Keyboard

The video monitor and power supply are common to all TeleVideo terminals and may be freely interchanged. Terminal keyboards are interchangeable, as outlined in the section on the keyboard. The main logic board is the only module that provides each terminal with its unique characteristics.

The quickest and easiest way to isolate the malfunctioning module is to exchange (swap) each module with a known good module. Once the faulty module is identified, refer to the appropriate troubleshooting table.

WARNING!

High voltages are retained by the CRT tube and capacitors even after power has been turned off. As soon as you open the case, clip one end of a wire to the chassis. Attach the other end of the wire to an insulated screwdriver. Being careful not to touch the metal part of the screwdriver, gently slip the metal end of the screwdriver under the cap of the anode, as shown in Figure 2-1.

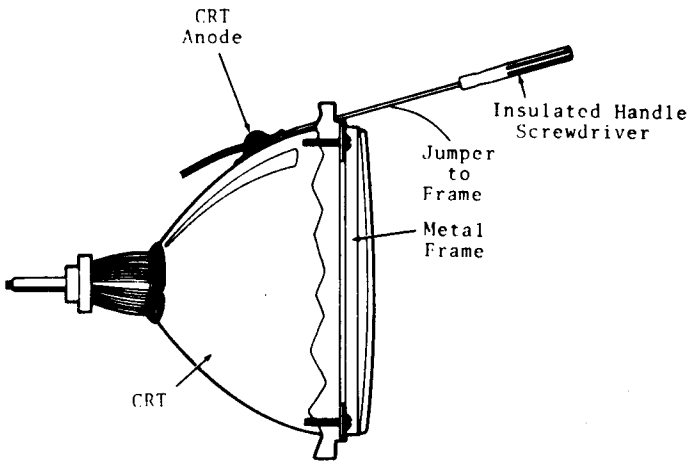


Figure 2-1 Discharging Voltages

3. FUNCTIONAL DESCRIPTION OF MODULES

Logic Board

The logic board processes and controls all data received and transmitted, and generates the video and sync signals required to display data.

The logic board consists of the following five functional areas:

1. Display processor
2. Display generator
3. Keyboard interface
4. Main port interface
5. Printer port interface

Power Supply

The power supply provides DC operating voltages to all circuits in the terminal. The power supply contains two user-replaceable 3 AG-type fuses.

Video Monitor

The video monitor contains horizontal, vertical, and intensity modulation circuits which produce a television-type conventional noninterlaced raster display on the screen. Character signals received from the display generator cause intensified dots to appear at precise intervals on a raster line. These dots, when combined with other dots on other raster lines above and/or below a given line, produce characters.

Keyboard

910/910 PLUS/912C/920C--This keyboard sends matrixed data via a ribbon cable to the logic board, where the ASCII code is generated.

This data is encoded in the 910/910 PLUS by the keyboard encoder (position A1) and in the 912C/920C by the CPU (position A54) and the multiplexers (positions A68 and A69).

The keyboards for these models are all functionally interchangeable. The 910/910 PLUS keyboard has a PRINT keycap where 912C/920C models have a BLOCK/CONV keycap. The 920C keyboard is also fitted with an additional top row of function and editing keys.

925/950--On this keyboard, data is encoded by a microprocessor on the keyboard (position U6) and sent in an ASCII serial data stream to the logic board via the coiled cable. On the logic board, the keyboard interface circuits convert the keyboard data from serial to parallel data for input to the display processor circuitry. All detachable keyboards are identical and interchangeable.

4. TROUBLESHOOTING THE LOGIC BOARD

Visual Inspection

With the Logic Board Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Internal and external switch settings: are they all correct?

* Socketed chips: are they all plugged tightly into their sockets?

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated or burned?

With the Logic Board Removed--Make these inspections with the logic board removed. The procedure for removing the logic board varies slightly according to the model. Follow the appropriate directions for your model.

910/910 PLUS/912C/920C

To remove the logic board:

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P2 (video signals)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P5 (voltage connector)
   P6 (modem connector) if connected
   P7 (speaker connector)

3. Remove the four (910/910 PLUS) or six (912C/920C) securing screws on the logic board.

4. Carefully remove the logic board.

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P6 (modem connector) if connected

3. Carefully slide the logic board half way out of the terminal and disconnect:

   P2 (video signals)
   P5 (voltage connector)

4. Carefully slide the logic board entirely out of the terminal.

With the logic board removed, inspect the logic board for:

* Overheated or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

STOP!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the logic board before proceeding with the procedures in the next section, Large Scale Integration Failures.

Large Scale Integration Failures

Since most failures involve Large Scale Integration (LSI) chips, this step will quickly repair most failures encountered. Exchange all socketed chips, one at a time, with known good chips. If the logic board malfunctions after the chips are swapped, confirm the operation of the data lines described in the next section, Data Line Operation.

NOTE!

The remainder of this guide involves troubleshooting to the component level and requires schematics, an oscilloscope, a working knowledge of transistor-transistor logic (TTL), and basic debugging skills.

Data Line Operation

Confirm that the data lines are operating properly before proceeding further.

NOTE!

It is beyond the scope of this bulletin to list all possible data line problems.

The best place to check the data lines is directly from the CPU (see page 1 of the schematics). There should be activity on all data lines and the signals should range from 0 (ground) to +4.5 to +5.0 volts. If the malfunction persists after you have confirmed proper operation of the data lines, follow the procedures in the next section, Debugging Tables.

Debugging Tables

NOTE!

The items listed in the tables in this section are only suspect areas; they should not be automatically replaced when the symptoms listed are present.

Table 4-1 910/910 PLUS Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6502	A39	1 of 5
	6545	A26	2 of 5
	2114	A30, A31, A36, A37	2 of 5
	or		
	6116	A24	2 of 5
	Crystal	Y2	3 of 5
	74LS163	A15	3 of 5
	2332	A45	1 of 5
	2N2219	Q2	4 of 5
Distorted video	6502	A39	1 of 5
	6545	A26	2 of 5
	6116	A24	2 of 5
	or		
	2114	A30, A31, A36, A37	2 of 5
	2332	A48	3 of 5
	74LS166	A49	3 of 5
Horizontal bar across screen	6545	A26	2 of 5
	74S04	A22	4 of 5
Loss of underline, reverse video, blinking, or blanking	74LS174	A42	3 of 5
	6545	A26	2 of 5
Loss of half intensity	74LS175	A41	3 of 5
	6545	A26	2 of 5
Loss of all attributes	6545	A26	2 of 5
	74S74	A40*	3 of 5
Unable to transmit data	75188	A10	4 of 5
	6551A	A19	4 of 5
Unable to receive data	75189	A5	4 of 5
	6551A	A19	4 of 5
Poor/no printing	75189	A5	4 of 5
	75188	A10	4 of 5
	6551A	A19	4 of 5
Incorrect/no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2**	5 of 5

Notes
*Must be a Texas Instruments part.
**If used.

Table 4-1 Continued

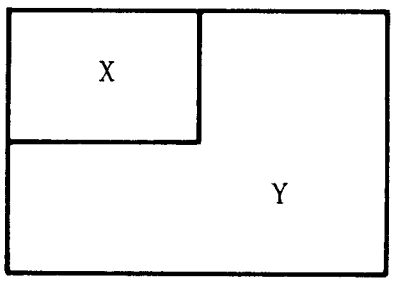
Symptom	Suspect Areas Part No.	Position	Schematic Page
SHIFT or CTRL keys do not function	A6-5-3600	A1	5 of 5
	7406	A12	5 of 5
	RP4		5 of 5
ALPHA LOCK or FUNCT keys do not function	AY-5-3600	A1	5 of 5
	74LS364	A8	5 of 5
	RP4		5 of 5
Keys repeat	AY-5-3600	A1	5 of 5

*Must be a Texas Instruments part.
**If used.

Table 4-2 912/920 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	8035	A54	1 of 6
	5027	A23	4 of 6
	23.814-MHz Crystal	X1	4 of 6
	74LS109	A56	4 of 6
	74LS163	A57	4 of 6
	System ROMs	A49	2 of 6
	System ROMs	A50*	2 of 6
	2332	A3	5 of 6
No video, constant beep	5027	A23	4 of 6
	2114 RAM, page 1	A6, A8, A10, A12	3 of 6
	2114 RAM, page 2	A5, A7, A9, A11	3 of 6
Horizontal bar across screen	5027	A23	4 of 6
	74LS08	A32	5 of 6
	74LS05	A14	5 of 6
Bad video or incorrect character displayed in:			
Area X of screen**	2114 RAMs	A8	3 of 6
	2114 RAMs	A12	3 of 6
Area Y of screen**	2114 RAMs	A6	3 of 6
	2114 RAMs	A10	3 of 6
Bad video on entire screen	74LS157	A24, A25, A26	3 of 6
	74LS00	A40	3 of 6
	8035	A54	1 of 6
	5027	A23	4 of 6

Notes
* If installed
**



Areas X and Y of Screen

Table 4-2 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Distorted characters	2316	A3	5 of 6
	8035	A54	1 of 6
	2114 RAMs	A5 through A12	3 of 6
Unable to transmit	75188	A59	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Unable to receive	75189	A60	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Loss of blinking or blanking	74LS74	A35	4 of 6
	5027	A23	4 of 6
Loss of half intensity	74LS74	A16	5 of 6
	74LS03	A15	5 of 6
	5027	A23	4 of 6
Loss or underlining/reverse video	74LS74	A28	5 of 6
	74LS74	A29	5 of 6
	5027	A23	4 of 6
Incorrect or no keyboard input	8035	A54	1 of 6
	74LS253	A68	1 of 6
	74LS253	A69	1 of 6
ALPHA LOCK, SHIFT, CTRL, or Function keys do not function	74LS364	A76	1 of 6
	74LS42	A58	1 of 6
Unable to select one or more baud rates	74LS163 Counter	A70 through A73	6 of 6
	Baud rate switch	S1	6 of 6
	74LS00 Nand Gate	A74	6 of 6

Table 4-3 925 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No beep, no video	13.6080-MHz Crystal	Y2	7 of 7
	74LS00	A55	4 of 7
	74LS139	A37	4 of 7
	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
Constant beep, no video	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
	74LS223	A44	7 of 7
Horizontal bar	74504	A16	7 of 7
	6545A-1	A59	2 of 7
Bad video	10uf cap	C41	1 of 7
	74LS74	A6	4 of 7
	6545A-1	A59	2 of 7
Distorted characters	74LS166	A30	2 of 7
	2332	A31	2 of 7
Unable to transmit to computer	75188	A34	5 of 7
	6551	A32	5 of 7
	74LS32	A26	5 of 7
Unable to receive from computer	75189	A9, A17	5 of 7
	6551	A32	5 of 7
Unable to transmit to printer	75188	A34, A25	5 of 7
	74LS32	A26	5 of 7
	6551	A32	5 of 7
Unable to receive from printer	75189	A9, A19	5 of 7
	74LS32	A26	5 of 7
	75188	A25	5 of 7
Loss of any video attribute	74LS173	A19, A20, A21	3 of 7
	74LS245	A40	2 of 7
	74LS374	A39	2 of o7
	2332	A50, A49	1 of 7
No keyboard communication*	1.8432-MHz Crystal	Y1	5 of 7
	6551	A33	5 of 7
	6502A	A60	1 of 7

*Refer also to Service Bulletin 2, Eliminating Keyboard Lockup

Table 4-3 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select switch bank S1	Switch	S1	6 of 7
	74LS244	A53, A52	6 of 7
	Resistor pack	RP5	6 of 7
Unable to select switch bank S2	Switch	S2	6 of 7
	74LS244	A51, A52, A53	6 of 7
	Resistor pack	RP1	6 of 7
Unable to select switch bank S3	Switch	S3	6 of 7
	74LS244	A43, A51,	6 of 7
	Resistor pack	RP4	6 of 7

Table 4-4 950 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	6502	A53	1 of 7
	6551	A49, A50 A51	5 of 7
	6545	A56	2 of 7
	Program ROMs	A41, A42	1 of 7
	User ROMs	A52	1 of 7
	Character Generator ROMs	A32, A33	4 of 7
	23.824-MHz Crystal	OSC1	6 of 7
	74LS163	A3	6 of 7
	74LS109	A6	6 of 7
No video, constant beep	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Horizontal bar across screen	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Bad video, one section of screen	2114	A25	3 of 7
	2114	A26	3 of 7
	2114	A27	3 of 7
	2114	A28	3 of 7
Bad video on only one page			
Page 1	6116	A37	3 of 7
Page 2	6116	A34	3 of 7
Page 3	6116	A35	3 of 7
Page 4	6116	A36	3 of 7
Bad video on entire screen	74LS157	A43 through A46	2 of 7
	6545	A55	2 of 7
	6502	A53	1 of 7
Distorted characters	2332	A32, A33	4 of 7
	74LS166	A22, A23	4 of 7
	6502	A53	1 of 7
	All 2114's	A25 through A28	3 of 7

Table 4-4 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to transmit to system	1488	A48	5 of 7
	74LS32	A58	5 of 7
	6551	A50	5 of 7
	74LS157	A59	5 of 7
Unable to receive from system	1489	A57	5 of 7
	74LS08	A29	5 of 7
	6551	A51	5 of 7
Unable to transmit to printer	1488	A39	5 of 7
	74LS32	A58	5 of 7
	6551	A51	5 of 7
	74LS157	A59	5 of 7
Unable to receive from printer	1489	A40	5 of 7
	6551	A51	5 of 7
Loss of any video attribute	74LS174	A19	4 of 7
	74LS157	A20	4 of 7
	74LS174	A21	4 of 7
Incorrect or no keyboard input	6502	A53	1 of 7
	6551	A49	3 of 7
Unable to select one or more baud rates	6502	A53	1 of 7
	6552	A54	7 of 7
	74LS367	A65, A66	7 of 7
	RP 2		7 of 7
	RP 3		7 of 7
	Switch 1		7 of 7

"Gate Array" Logic board, Supplement Debugging Guide

Although the components are laid out differently, "Gate Array" boards are completely interchangable with TTL boards. When troubleshooting the "Gate Array" Logic boards care should be taken when handling the CMOS devices. The "Gate Array" chip positions are listed below. When exchanging these custom CMOS chips one must be grounded to earth ground to avoid damage to the chip from static discharge.

Model No.	Televideo Part Number	Location
910, 910Plus	2057400	A22
925	2057400	A39
950, Chip A	2057600	A34
Chip B	2057800	A37

Follow the procedure in the begining of this section for a visual inspection of the logic board.

Table 4-5 910/910 PLUS GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6545A-1	A20	2 of 5
	6502	A27	1 of 5
	6116	A13	2 of 5
	Crystal	Y2	3 of 5
	2532	A38	1 of 5
	74LS163	A25	3 of 5
	74LS166	A18	3 of 5
	2N2219	Q2	4 of 5
	70200-11B	A22	3 of 5
Distorted video	6545A-1	A20	2 of 5
	6116	A13	2 of 5
	70200-11B	A22	3 of 5
	74LS166	A18	3 of 5
	2532	A38	1 of 5
Horizontal Bar across screen	6545A-1	A20	2 of 5
	74LS08	A37	2 of 5
Loss of Attribute	70200-11B	A22	3 of 5
	6545A-1	A20	2 of 5
Unable to Transmit to Computer or printer	75188	A9	4 of 5
	6551A-1	A15	4 of 5
Unable to Receive from Computer or printer	75189	A10	4 of 5
	6551A-1	A15	4 of 5
Inncorect/ no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2	5 of 5
	74LS367	A3,A8	5 of 5
Shift or CTRL keys inoperative	AY-5-3600	A1	5 of 5
	7406	A7	5 of 5
	resistor pack	RP2	5 of 5
Alpha Lock or Funct keys inoperative	AY-5-3600	A1	5 of 5
	74LS367	A8	5 of 5
	resistor pack	RP2	5 of 5
Repeating keys	AY-5-3600	A1	5 of 5

Table 4-6 925 GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic page
No video/ no beep	Crystal	Y2	6 of 6
	70200-11A	A39	3 of 6
	74LS139	A38	3 of 6
	6502	A11	1 of 6
	6545A-1	A28	2 of 6
Constant beep/ no video	6545A-1	A28	2 of 6
	74LS273	A26	6 of 6
	6502	A11	1 of 6
Horizontal bar across screen	6545A-1	A28	2 of 6
	74S04	A40	3 of 6
Bad video	10uF cap	C28	1 of 6
	6545A-1	A28	2 of 6
	70200-11a	A39	3 of 6
Distorted characters	2332	A17	2 of 6
	74LS166	A12	2 of 6
Loss of Attribute	70200-11A	A39	3 of 6
	2333	A14,A15	1 of 6
No transmit to computer or printer	75188	A23	4 of 6
	6551A-1	A4	4 of 6
	74LS32	A24	4 of 6
No receive from computer or printer	75189	A2	4 of 6
	6551A-1	A4	4 of 6
No keyboard response	Crystal	Y3	4 of 6
	6551A-1	A5	4 of 6
	6502	A11	1 of 6
Unable to select S1	Switch	S1	5 of 6
	74LS244	A3,A41	5 of 6
	resistor pack	RP1	5 of 6
Unable to select S2	Switch	S2	5 of 6
	74LS244	A3,A41, A34	5 of 6
	resistor pack	RP2	5 of 6
Unable to select S3	Switch	S3	5 of 6
	74LS244	A34,A29	5 of 6
	resistor pack	RP4	5 of 6

Table 4-7 950 GA Logic Board Debugging Guide

Symptom	Suspect Areas		Schematic
	Part No.	Position	Page
No video/ no beep	6502	A11	1 of 7
	6551	A29,A33	5 of 7
		A36	
	6545	A6	2 of 7
	740012	A34	4 of 7
	2532	A20,A25	1 of 7
	2332	A30,A31	4 of 7
	Crystal	OSC 1	4 of 7
No video/ constant beep	6545	A6	2 0f 7
	6116	A3	3 of 7
Horizontal bar across screen	6545	A6	2 of 7
	7406	A39	6 of 7
Bad video	6116	A8,A13	3 of 7
		A17,A22	3 of 7
	74LS157	A7,A12	2 of 7
		A16,A21	2 of 7
	6545	A6	2 of 7
	6502	A11	1 of 7
	740012	A34	4 of 7
Distorted characters	2332	A30,A31	4 of 7
	740012	A34	4 of 7
	740012	A37	6 of 7
Loss of Attributes	740012	A34	4 of 7
Unable to transmit to computer	75188	A18	5 of 7
	74LS32	A19	5 of 7
	6551	A29	5 of 7
	74LS157	A28	5 of 7
Unable to receive from computer	75189	A9	5 of 7
	740012	A37	6 of 7
	6551	A29	5 of 7
Unable to transmit to printer	75188	A23	5 of 7
	74LS32	A24	5 of 7
	6551	A33	5 of 7
	74LS157	A28	5 of 7
Unable to receive from printer	75189	A32	5 of 7
	6551	A33	5 of 7
Inncorect/ no keyboard response	6551	A36	5 of 7
	6502	A11	1 of 7
	74LS32	A19	5 of 7

Table 4-7 continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select S1	Switch	S1	7 of 7
	resistor pack	RP1,RP2	7 of 7
	74LS367	A1,A4	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7
Unable to select S2	Switch	S2	7 of 7
	resistor pack	RP2	7 of 7
	74LS367	A4,A38 A42	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7

5. TROUBLESHOOTING THE KEYBOARD

Visual Inspection

With the Keyboard Installed--Turn off power to the terminal. Check keyboard alignment; are any keys binding on the cover?

Open the top case.

910/910 PLUS/912/920

Remove the two screws from the bottom front corners of the terminal. Carefully tip the top case back until it rests on a firm surface.

NOTE!

The terminal will now be top heavy and may tip over if there is not sufficient table space to support the top.

925/950

Remove the four screws from the bottom of the keyboard case. Carefully life off the top of the keyboard case and set it aside.

Check the following areas:

* Key switches:

  Foreign objects (e.g., paperclips, staples, matches)

  Liquid residue (e.g., coffee, soft drinks)

  Broken keyswitches

  Missing or incorrectly placed keycaps

* Cables:

  Broken wires

  Loose wires at connectors

  Creased, kinked, or cut cables

* Connectors:

  Loose or damaged connectors

  Bent pins

  Dirty contacts

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

With the Keyboard Removed--Make the following inspections with the keyboard removed from its case. The procedure for removing the keyboard varies slightly according to the model.

910/910 PLUS/912/920

To remove the keyboard:

1. Unplug the ribbon cable from the logic board.
2. Remove the two securing screws and washers from the inner bottom corners of the keyboard.
3. Carefully remove the keyboard from the surrounding case.

925/950

To remove the keyboard:

1. Disconnect on the keyboard:

   P6 (speaker connector)
   P7 (keyboard cable)

2. Remove the four screws from the bottom corners of the keyboard case.
3. Carefully remove the keyboard from the bottom case.

Inspect the keyboard for:

* Overheated, damaged, or burned components
* Cracked, shorted, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Broken, loose, or frayed wires

NOTE!

If any defects are found, correct them and recheck before continuing.

Table 5-1 Keyboard Debugging Guide

Symptom	Suspect Areas	Models
One key inoperative/ intermittent	Respective keyswitch	A
	Open trace/bad solder joint	A
	8048 keyboard CPU, position U6	B
Several keys inoperative/intermittent	Open/shorted trace	A
	Broken/loose jumper	A
	Defective ribbon cable	C, D
	Bent pin at ribbon cable connectors	C, D
	8048 keyboard CPU, position U6	B
	10K ohm resistor packs, positions RP2, RP3	B
	10K ohm resistor, position R3	B
All keys inoperative	Open/shorted trace	A
	Defective ribbon or keyboard cable	A
	8048 keyboard CPU, position U6	B
	7805 +5V regulator, position V1	B
	5.7143-MHz crystal, position X1	B
SHIFT, FUNCT, or ALPHA LOCK keys	10K ohm resistor pack, position RP2	
	8048 keyboard CPU, position U6	B
CTRL key inoperative	10K ohm resistor pack, position R2	
	8048 keyboard CPU, position U6	B
Incorrect characters	Shorted trace	A
	Shorted/improperly plugged ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Table 5-1 Continued

Symptom	Suspect Areas	Models
Keys repeat	Respective keyswitch*	B, D
	Shorted trace	A
	Shorted ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Note
*On the 910/910 PLUS terminals, a key which is shorted will not repeat on power up. Instead, any key pressed will repeat until another key is pressed.

6. TROUBLESHOOTING THE VIDEO MONITOR

Visual Inspection

With the Video Monitor Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

If any defects are found, correct them and recheck the terminal before continuing.

With the Video Monitor Removed--The following inspections should be made with the video monitor removed.

To remove the video monitor:

1. With the power off and the cover removed, disconnect the following connections on the video monitor:

   J10 (signal input)
   J11 (DC power)
   J12 (yoke)

2. Disconnect the following parts on the CRT tube:

   CRT socket (small printed circuit board at rear of tube)

   Anode lead (SEE WARNING ON PAGE 2-1)

   Ground wire

3. Remove the three securing screws on the video monitor.

4. Carefully remove the video monitor.

With the video monitor removed, inspect it for:

* Overheated, leaking, or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the video monitor.

Apply power.

WARNING!

High voltages are present on the video logic board. USE EXTREME CARE during troubleshooting.

The four adjustments which can be made to the video board are listed in Table 6-1. The controls are shown in Figure 6-1.

Table 6-1 Video Board Adjustments

Problem	Control
Characters are too bright or too dim	Brightness
Whole screen is too tall or too short	Height
Characters are not even in height from the top to the bottom of the screen	Linearity
Characters are not sharp	Focus

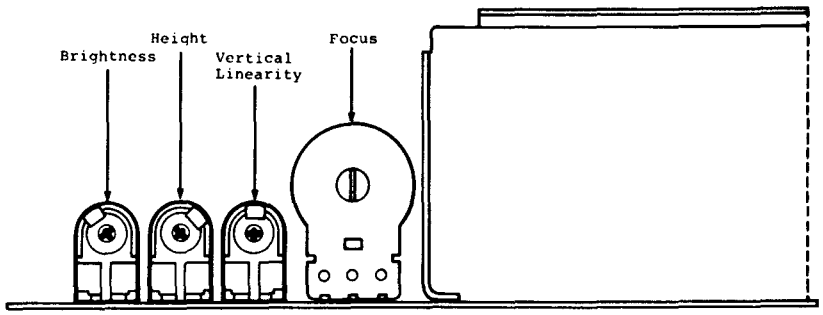


Figure 6-1 Location of Controls on Video Board

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and wave forms.

SYMPTOM: No Vertical Deflection

1. Check Q201 collector for vertical deflection.

   a. If it is present, proceed to Step 2.

   b. If it is not present, check the base of Q201.

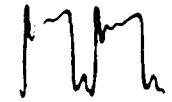
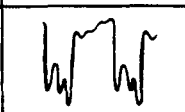
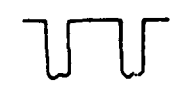
   c. If vertical deflection is present at the base, isolate the Q201 collector to see if signal is being pulled down. If there is still no output at Q201, suspect Q201.

   d. If vertical deflection is not present at the base, troubleshoot between the base of Q201 and P10 pin 5 (vertical sync signal from the logic board).

2. Check Q202 collector for vertical deflection.

   a. If it is present, proceed to Step 3.

   b. If it is not present, check the base of Q202.

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC 1)	LAS1512	Regulation	12	2.5		12	0.0		0.0	0.0	
(IC 2)	LAS1605	〃		1.6		5	0.0		0.0	0.0	
(IC 3)	LAS1812	〃		0.1		12	0.0		0.0	0.0	
(IC 4)	LAS15CB	〃		1.4		13.8	0.0		0.0	0.0	
Q102	2SC509	〃	78.7	0.0		86.4	1.5		08.0	0.0	
Q103	2SC983	〃	12.0	0.0		75.7	0.0		11..	0.0	
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0		8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0		8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	
Q501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

Table 6-2 Voltage Levels and Waveforms

c. If vertical deflection is present at the base, isolate the Q202 collector to see if signal is being pulled down. If there is still no output at Q202, suspect Q202.

d. If vertical deflection is not present at the base, troubleshoot back from the base of Q202.

3. Check the negative side of C207 for vertical deflection.

a. If vertical deflection is present, the vertical drive section of the video monitor is good. If a vertical problem still exists, check the following areas:

Connections
CRT socket
Related components (small pcb at neck of CRT)

b. If vertical deflection is not present at C207, check the Q203 emitter.

c. If vertical deflection is not present at the Q203 emitter, check the base of Q203.

d. If vertical deflection is present at the base, suspect Q203.

e. If not present at the base of Q203, troubleshoot back.

f. If Q203 emitter is good, check Q204 emitter.

g. If vertical deflection is not present at Q204 emitter, check the base of A204.

h. If present at base, suspect A204.

i. If not present at base, troubleshoot back from Q204.

NOTE!

Since Q203 and Q204 are a matched set of push/pull amplifiers, replace both if one require replacement.

SYMPTOM: No Horizontal Deflections

1. Check the Q301 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 2.

b. If not present, check the base of Q301.

c. If horizontal deflections are present at the base, isolate the Q301 collector to see if signal is being pulled down.

d. If there is no output at the Q301 collector, suspect Q301.

e. If horizontal deflections are not present at the base of Q301, troubleshoot between the base of Q301 and P10 pin 1 (horizontal sync signal from the logic board).

2. Check the Q302 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 3.

b. If not present, check the base of Q302.

c. If horizontal deflections are present at the base, isolate the Q302 collector to see if signal is being pulled down.

d. If there is no output at the Q302 collector, suspect A302.

e. If horizontal deflections are not present at the base of Q301, suspect T301 (drive transformer) or Q302.

f. If the proper signal is present at Q302 collector, suspect the following areas:

C306
L201

SYMPTOM: No Video

1. Suspect the following areas:

L302
Q302
Q301
T302 (FBT)
C305
Q501

2. Check for cracked, broken, or lifted traces.

SYMPTOM: Jittery Screen

1. Make sure that yoke connector J12 is not dirty.

2. Suspect C504.

3. Check for

   * Bad crimps

   * Poor solder joints (loose solder balls, cold solder joints, or solder bridges)

SYMPTOM: Poor Linearity

1. If horizontal linearity is the problem, check L201.

2. If vertical linearity is the problem, check the following:

   a. Adjust SFT 2 (linearity potentiometer)

   b. Q203 and Q204

SYMPTOM: Fuses Blow and/or Voltage is Low

1. Check T302 (FBT)

2. Check for cracked, broken, or lifted traces.

7. TROUBLESHOOTING THE POWER SUPPLY

Visual Inspection

With the Power Supply Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

  Depressed pins in connectors

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

* Bad fuse

  NOTE!

  Check the fuse with an ohm meter. Do not rely on a visual check.

* Loose fuse holder

If defects are found, correct them and recheck the terminal before continuing.

With the Power Supply Removed--The following inspections should be made with the power supply removed.

To remove the power supply:

1. Turn the power off and remove the cover.
2. Unplug the power cord from the wall outlet.
3. Disconnect K1 (AC input) on the power supply.
4. Disconnect J11 on the video monitor.
5. Disconnect J5 on the logic board.
6. Remove the securing screws on the power supply (four on the 925/950; three on 910/910 PLUS/912/920).
7. Carefully remove the power supply.

With the Power Supply Removed--Inspect the power supply for:

* Overheated, leaking, or burned components
* Bad crimps
* Bad connectors/connections

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

Disassemble the power supply by removing the four securing screws and spacers which hold the small pcb on the heat sink.

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and waveforms.

SYMPTOM: No +5V DC

1. Remove F103 and check for approximately +13V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C105 through C108

      D105 through D108

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

   b. If correct voltage is present, suspect the following areas:

      F103 (fuse)

      LAS1605

      C114

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +5V DC is Low

1. Check the following areas:

   LAS1605

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +12V DC or 13.8V DC

1. Remove F102 and check for +24V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C101 through C104
      D101 through D104
      Bad crimps
      Bad connectors/connections
      Broken or loose clips

   b. If correct voltage is present, suspect the following areas:

      LAS15CB/LAS16CB

      C115

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +12V DC or +13.8V DC is Low

1. Check the following areas:

   LAS15CB

   C113

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No -12V DC

1. Check the following areas:

   C101 and C102

   D101 and D102

   D112

   C116

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +75V DC

1. Check the following areas:

   C109 (can be removed; do not need to be replaced)
   C120
   C119
   Q102
   Q103

SYMPTOM: +75V DC is Low

1. Adjust SFR3.

2. If +75V DC cannot be adjusted, check the following areas:

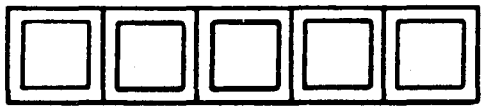
   Q103
   C109

If no defects are found, reinstall the video monitor. Make sure the securing screws are locked tight before proceeding.

Apply power.

ELIMINATING LOSS OF VIDEO BY UPGRADING THE POWER SUPPLY

If you suspect that the power supply is causing loss of video, upgrading the power supply may correct the problem. To determine whether the power supply is the cause, measure the voltage on pin 5 of plug P5 on the logic board when the terminal is in the fail mode. (Refer to Figure 4-1).



Pins	1	2	3	4	5
	-12v	Not Used	Grd	+5V	+12V

Figure 4-1 Top View of P5

The reading should be between 11.4V and 12.6V. If the P5-5 reading is below 11.4V, modify the power supply using this procedure.

TOOLS REQUIRED

1. Volt meter
2. 25-watt soldering iron
3. Solder
4. Needle nose pliers
5. Medium Phillips-head screwdriver

PARTS REQUIRED

1. One 0.22uf/35V Tantalum capacitor

PROCEDURE

1. Make sure the power has been turned off.

2. Remove the power supply from the terminal.

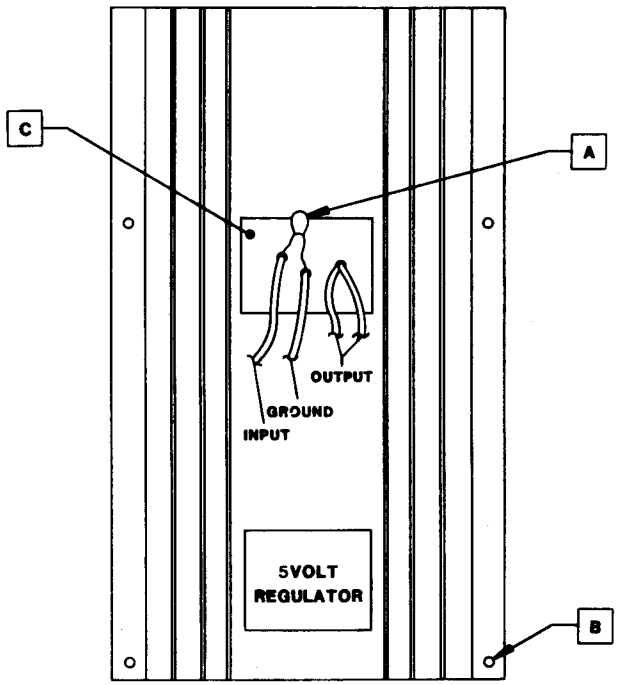
3. Separate the printed circuit board from the heat sink by removing plug K2 and the four screws and spacers from the corners of the board. Set the printed circuit board aside.

4. Inspect the capacitors which are mounted on the socket used for the 13.8V regulator (either LAS15CB or LAS16CB). If two 0.22uf capacitors are in place, remove the one on the output and proceed to Step 6. Remove all other capacitors which you find. Refer to Figure 4-2.

ALL

NOTE!

Do not perform any modifications to the other regulator, as it is the 5 volt supply and does not need to be changed.



A - .22μF Capacitor
B - PC Board Mounting Screws
C - LAS16CB Socket

Figure 4-2 Power Supply Heat Sink with PCB Removed

5. Install the 0.22uf capacitor on the input side of the regulator, observing polarity requirements. (Refer to Figure 4-2.)

6. Reassemble the power supply board and mount it in the terminal.

7. Reconnect all cables.

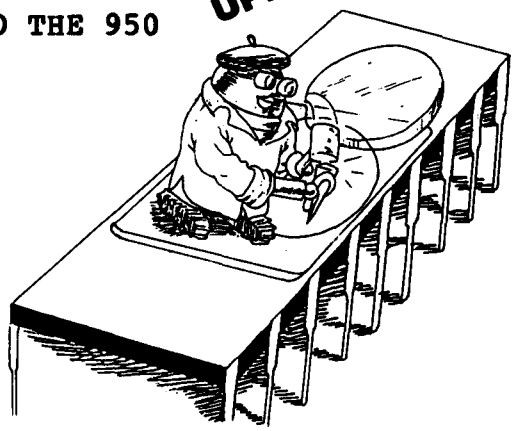
The modification is now complete.

Service Bulletin

UPDATED

Issue No. 6

ADDING ADDITIONAL PAGES OF MEMORY TO THE 950



The 950 is normally shipped with one page of memory.

However, you can add one or three (but not two) additional 24-line pages of memory by adding memory chips.

PARTS REQUIRED

To add memory to the 950, install 2K x 8 Static RAM, 150 ns. memory chips.

Page of Memory	TeleVideo Part No.
Second (one chip)	2001500
Third and fourth (two chips)	2001600

950

PROCEDURE

Install the appropriate memory chips on the logic board, in the locations listed. Make sure that the notch in the top of the chip points in the same direction as that in the other ICs.

For your convenience, we recommend that you install sockets (if they are not already installed on the board).

A. TTL Logic Boards (blue boards)

Page Number	Location
One (factory installed)	A37
Two	A34
Three*	A35
Four	A36

B. Gate Array Logic Boards (green boards)

Page Number	Location
One (factory installed)	A22
Two	A8
Three*	A13
Four	A17

* Page three cannot be accessed unless page four has been installed.

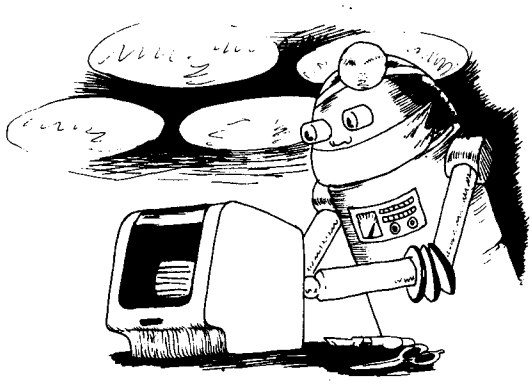
121482 SB6 950

Service Bulletin

Issue No. 12

ELIMINATING 950 DISPLAY VIBRATION AFTER EPROMS ARE INSTALLED

The display on some 950 terminals may vibrate after EPROMs are installed in place of the program ROMs. Changing six capacitors should eliminate this problem.



TOOLS REQUIRED

1. 25-watt soldering iron
2. Solder
3. Solder sucker
4. Wire clippers
5. Needlenose pliers

PARTS REQUIRED

1. Five 0.1uF 50 volt monolithic capacitors
2. One 10.0uF 25 volt tantalum capacitor

PROCEDURE

1. Remove the six capacitors which are located at the following positions on the logic board:

   C1 C7 C8 C30 C35 C36

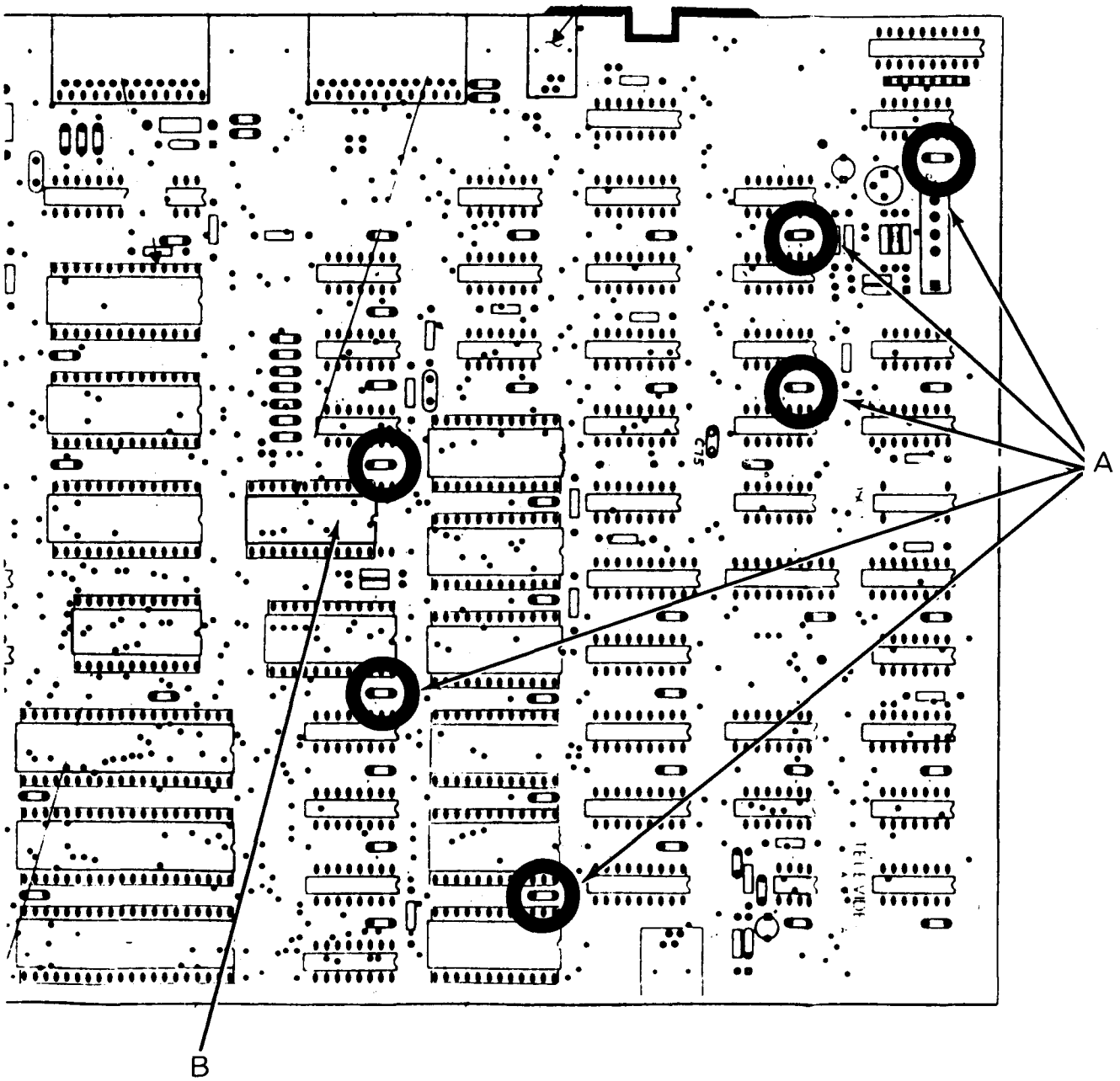
2. Install the five 0.1uF capacitors in the following locations on the logic board:

   C1 C7 C8 C30 C36

3. Install the 10.0uF capacitor in position C35 on the logic board, observing the polarity requirements shown in Figure 12-1.

4. Remove any solder splash to avoid causing a short.

950



Legend:

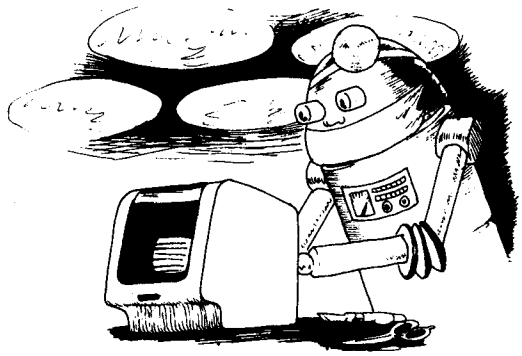
A. Replace these capacitors with 0.1uF 50 volt monolithic capacitors.
B. Replace this capacitor with a 10.0 uF 25 volt tantalum capacitor.

Figure 12-1 Capacitor Locations on the Logic Board

Service Bulletin

Issue No. 13

ELIMINATING MISSING CHARACTER DOTS ON 950 TERMINALS



Some 950 terminals may contain a chip which causes a timing problem with the parallel-in/ serial-out shift registers which convert character data into serial dot data for display on the screen. The result can be missing character dots.

The chip which can cause this problem is chip 74LS166AN (in locations A22 and A23 on the logic board). If the older chip 74LS166N has been installed instead, no modification is needed.

By cutting one trace and installing four jumpers and one capacitor, the clock input will be delayed and the input set-up time delayed.

950

TOOLS REQUIRED

1. 25-watt soldering iron or equivalent
1. Solder
3. Solder sucker
4. Needlenose pliers
5. X-ACTO knife or razor blade

PARTS REQUIRED

1. 0.031-gauge jumper wire
2. One 100pF 500 volt 5% ceramic disk capacitor

PROCEDURE

1. Cut the trace which connects A-23 pin 7 to crystal oscillator 1, as shown in Figure 13-1.

2. Install jumpers between the following locations, as shown in Figures 13-1 and 13-2:

   A12 pin 9 to A13 pin 6
   A12 pin 8 to A23 pin 7
   A13 pin 4 to A13 pin 5
   A13 pin 5 to OSC 1 pin 8

3. Install the 100pF capacitor between A12 pin 9 and the feedthrough as shown in Figure 13-3.

4. Figure 13-4 shows the revised schematic.

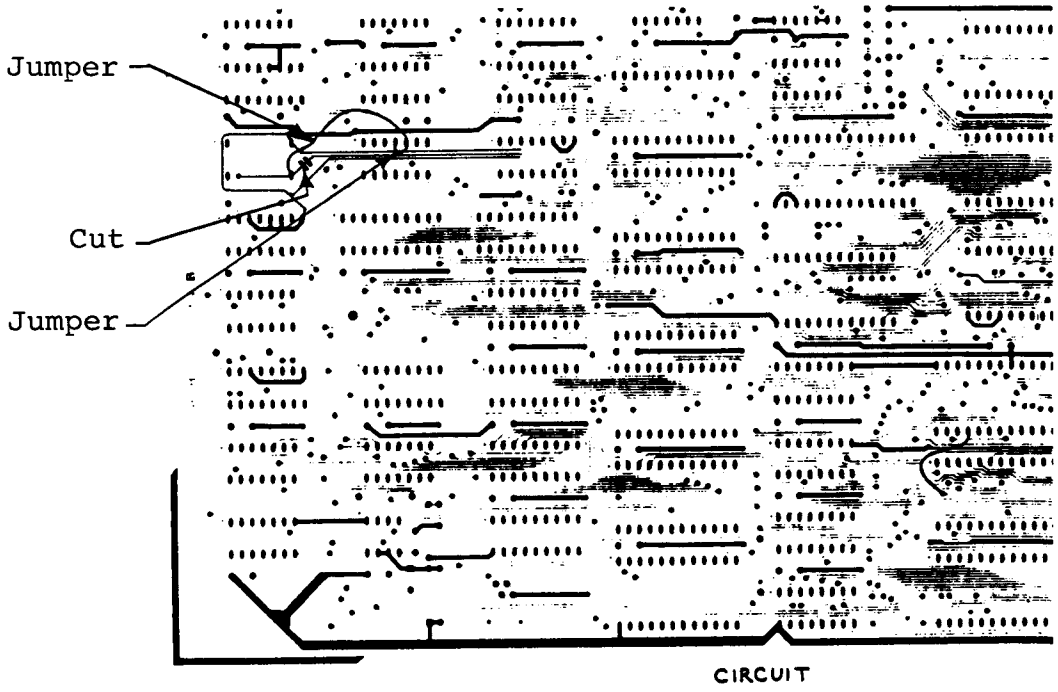


Figure 13-1 Cuts and Jumpers on Logic Board

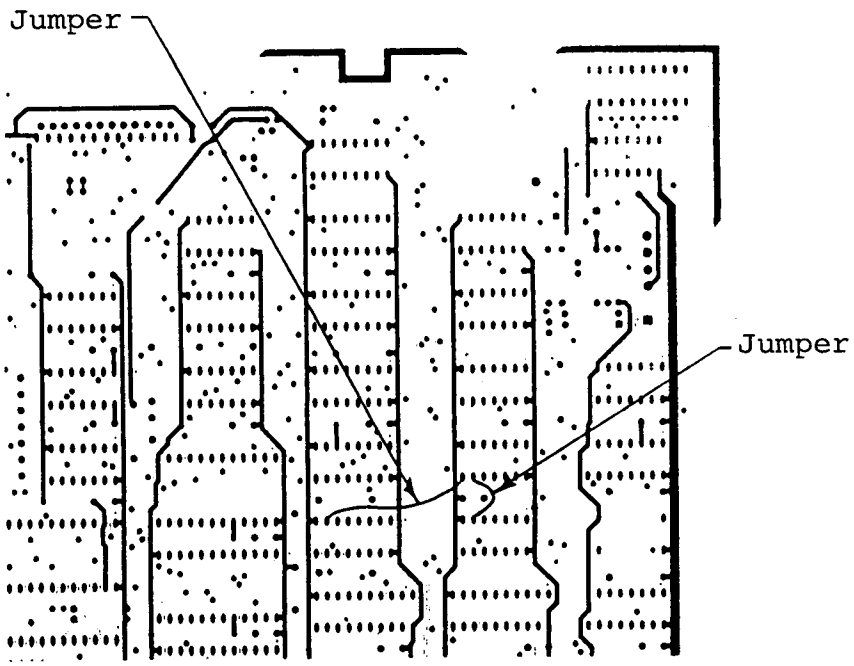


Figure 13-2 Location of Jumpers to be Installed on Logic Board

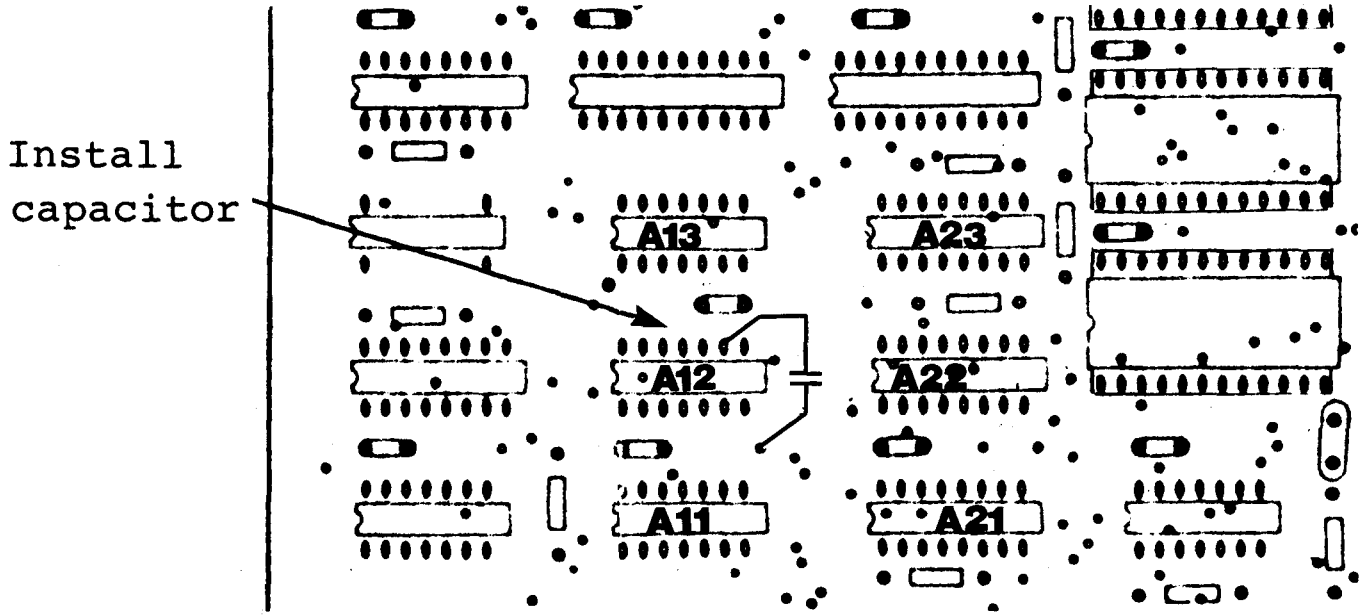


Figure 13-3 Location of Additional Capacitor

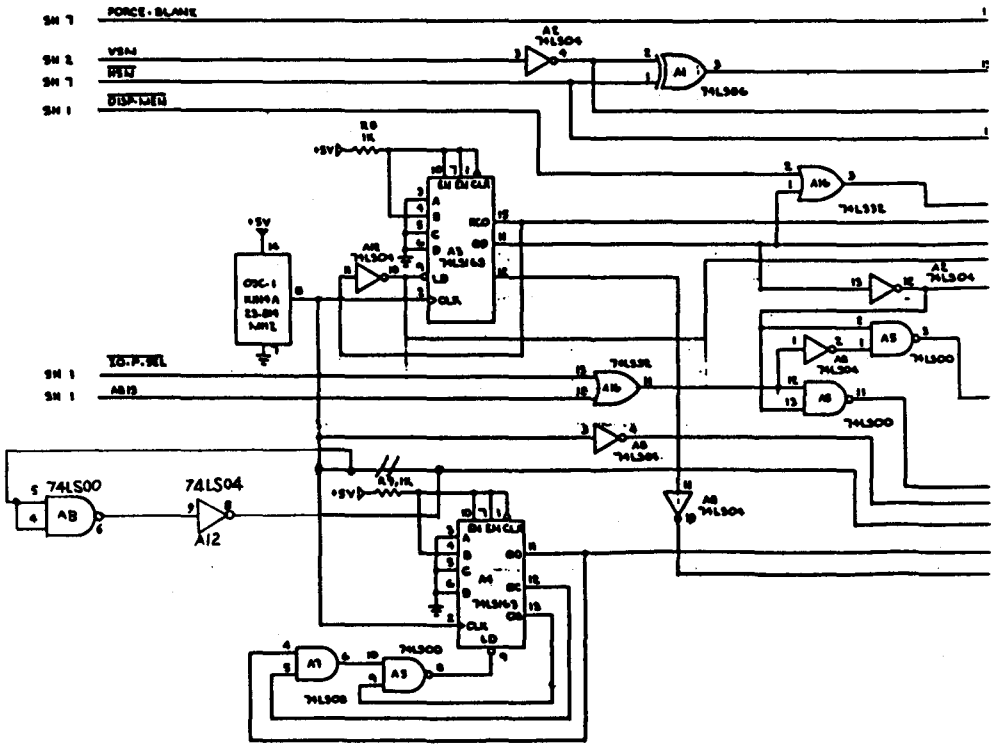


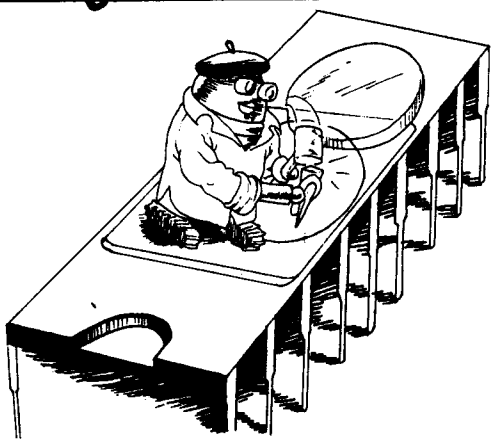
Figure 13-4 Revised Schematic, Sheet 6 of 7

Service Bulletin

UPDATED

Issue No. 15

INSTALLING THE CURRENT LOOP FEATURE



This bulletin tells you how to install or activate the current loop feature in each of the terminals. It also includes a section on testing and troubleshooting.

Install or activate the current loop when the terminal is located more than 50 feet and less than 1000 feet from the computer, or when the device connected to the RS232 port (P3) requires current loop.

Configuration

The current loop feature must be configured for either half or full duplex mode, and for an active or passive terminal state.

Either the terminal or the computer must provide a 20mA current source to drive a current loop signal. If the terminal provides the current source, configure the current loop board for an active state. If the computer provides the current source, configure for a passive state.

The full duplex mode requires two current sources, one for the transmit and one for the receive loop. The half duplex mode requires only one current source for the single transmit and receive loop.

910, 910 PLUS, and 925 Current Loop Installation

Tools Required

1. 25-watt soldering iron
2. Solder sucker
3. Solder
4. Medium Phillips screwdriver
5. Needlenose pliers

Parts Required

For the 910, 910 PLUS terminals:

Current loop installation kit (Part No. 2131000)
20-gauge jumper wire

For 925 terminals:

Current loop installation kit (Part No. 2131100)
20-gauge jumper wire

ALL

Procedure

1. Inspect the current loop board for damage caused by shipping.

2. Configure the current loop board to match the requirements of the system you want to interface with. See Figure 15-1 for jumper locations and Table 15-1 for configuration combinations. Note that the half duplex mode requires jumpers in the connector pins of the cable, as well as on the current loop board.

3. Remove the the screws beneath the terminal that hold the terminal cover in place. Remove the cover.

4. **910, 910 PLUS (TTL and gate array logic boards):** Insert the current loop board connector pins into the 16-pin socket* at P6 on the logic board, as shown in Figure 2. Secure with mounting hardware.

   925, TTL Logic Board*: Mount the current loop board on the logic board, as shown in Figure 3. Connect it to the 16-pin socket at P6** with a 16-pin ribbon. Secure with mounting hardware.

   925, Gate Array Logic Board: Insert the current loop board connector pins into the 16-pin socket at P6 on the logic board, as shown in Figure 4. Secure with mounting hardware.

6. Replace the terminal cover and the screws that hold it in place. Be careful not to overtighten the screws.

7. Connect the computer to the terminal at the RS232 port (P3), using a RS232 cable. See Table 15-1 for the necessary pin connector assignments.

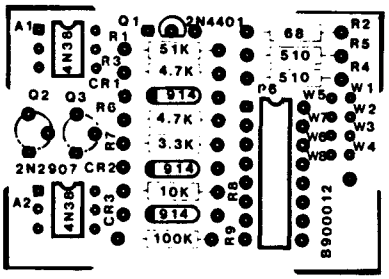
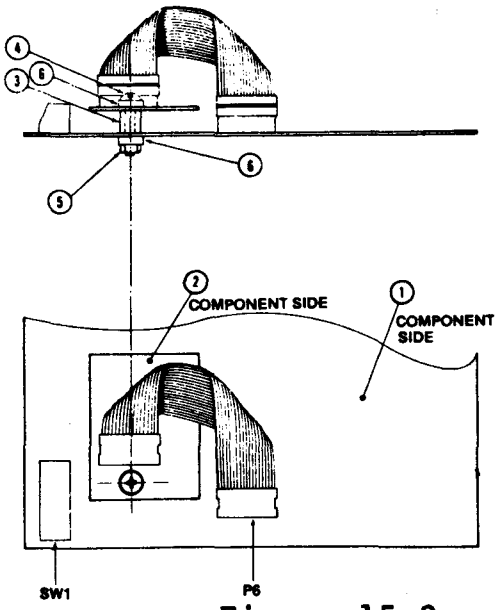


Figure 15-1 Location of Jumpers on Current Loop Board

* For the fastest way to distinguish between TTL and Gate Array boards, consult Service Bulletin 23.

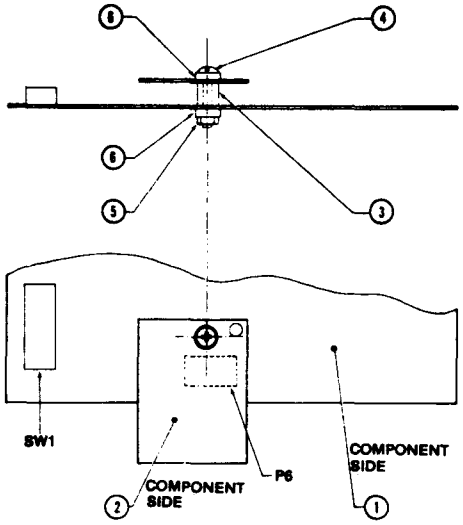
**Some early models were shipped without a 16-pin IC socket in location P6. If your terminal doesn't have a socket at P6, install a standard 16-pin IC socket. These sockets are available from most computer vendors or from TeleVideo (Part No. 2098405)



1. 925 TTL BOARD
2. CURRENT LOOP BOARD
3. NYLON SPACER
4. SCREW
5. HEX NUT
6. NYLON WASHER

Figure 15-2

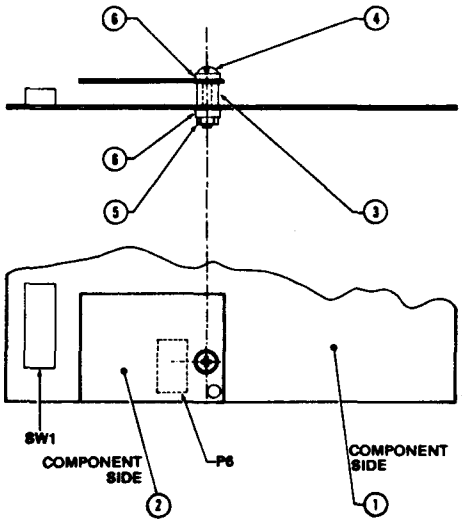
Current Loop Board in Socket
on 910, 910 PLUS TTL or Gate Array Logic Board



1. 910, 910 PLUS BOARD
2. CURRENT LOOP BOARD
3. NYLON SPACER
4. SCREW
5. HEX NUT
6. NYLON WASHER

Figure 15-3

Current Loop Board Installed with Cable on 925 TTL Logic Board



1. 925 GATE ARRAY BOARD
2. CURRENT LOOP BOARD
3. NYLON SPACER
4. SCREW
5. HEX NUT
6. NYLON WASHER

Figure 15-4

Current Loop Board in Socket on 925 Gate Array Logic Board

Table 15-1 lists the possible current loop configurations and the correct pin connector assignments for the RS232 cable.

In full duplex mode, you must select a transmit and a receive state. That means that four pins will be connected. The terminal can supply the voltage (i.e. active state) for either or both loops. If the computer supplies it, the terminal is in the passive state.

In half duplex mode, there is a single transmit and receive loop. Therefore, only two pins need to be connected. The terminal can supply the voltage (i.e. active state) for this loop. If the computer provides it, the terminal is in the passive state.

Table 15-1

Cuts, Jumpers, and P3 Configuration for 910, 910 PLUS, and 925

Mode	State	Cuts	Jumpers	P3 Assignments
Full Duplex	Active Transmit	W2 to W3	W1 to W2 W3 to W4	13+ 25-
	Active Receive	W6 to W7	W5 to W6 W7 to W8	24+ 12-
	Passive Transmit	None	None	25+ 13-
	Passive Receive	None	None	12+ 24-
Half Duplex	Active Transmit/ Receive	None	W1 to W2 P3-12 to P3-13	24+ 07-
	Passive Transmit/ Receive	None	P3-12 to P3-13	25+ 24-

Service Bulletin

Issue No. 20

950 JUMPER OPTIONS AND PORT CONNECTORS

The 950 logic board contains many jumpers and several ports. This bulletin gives you information about them in tabular form. For more information, refer to the User's Guide and Maintenance Manual.

Table	Description
20-1	Lists the jumpers which are called out on the logic board, the schematic page where they can be found, and a description of the purpose of the jumper
20-2	Lists the ports on the logic board, their use, and the pin assignments

Table 20-1a Logic Board Jumpers

Jumper No.*	Schematic Page No.	Description
E1, E2	6 of 7	Cut to enable composite video
E3, E4	6 of 7	Jumper to enable composite video
E5, E6	4 of 7	Not used
E7, E8, E9	5 of 7	Not used
E10, E11	5 of 7	Enables P4 pin 4 (Request to Send)
E12, E13	5 of 7	Enables P4 pin 4 (Data Terminal Ready)
E14 through E20	1 of 7	Allows 8K ROM to be used in Position A41
E21, E22, E23	1 of 7	Allows 8K ROM to be used in Position A50
E24, E25	5 of 7	Disables optional speaker port P7
E26	1 of 7	Allows 8K ROM to be used in Position A50

Note
*See Table 20-1b for jumpers normally traced or not traced.

950

Table 20-1a Continued

Jumper No.*	Schematic Page No.	Description
E27, E28	1 of 7	Allows 8K ROM to be used in Position A50.
E29, E30, E31	5 of 7	Not used

Note
*See Table 20-1b for jumpers normally traced or not traced.

Table 20-1b Jumpers Normally Traced/Not Traced

Traced	Not Traced
E1 to E2	E3 to E4
E5 to E6	E7 to E8
E10 to E11	E8 to E9
E12 to E13	E14 to E15
E14 to E16	E16 to E17
E15 to E17	E19 to E20
E18 to E19	E21 to E22
E21 to E22	E22 to E23
E24 to E25	E29 to E30
E27 to E28	
E29 to E31	

Table 20-2 Ports and Associated Pin Assignments

Port No.	Description	Pin No.	Function
P0	Optional keyboard input		
		1	+12 volt supply
		2	Ground
		3	Data input from keyboard
		4	Speaker output

Table 20-2 Continued

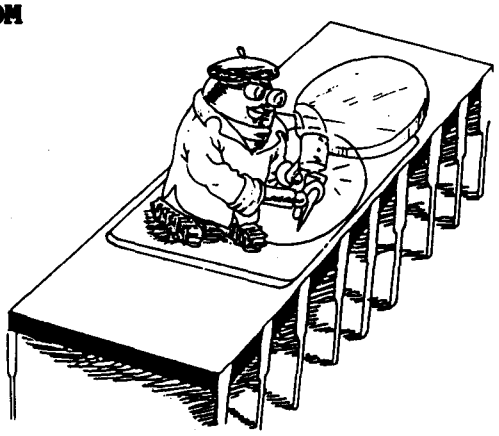
Port No.	Description	Pin No.	Function
P1*	Keyboard input		
		1	+12 volt supply
		2	Ground
		3	Data input from keyboard
		4	Speaker output
P2	Video output		
		1	Horizontal sync
		2	Index pin (not installed)
		3	Ground
		4	Video output
		5	Vertical sync
		6	Composite video output (not installed)
P3	RS232C		
		1	Frame ground
		2	Transmit data output
		3	Receive data input
		4	Request to Send output
		5	Clear to Send input
		6	Data Set Ready input
		7	Signal ground
		8	Data Carrier Detect input
		9	20mA source (+12 volt, no load)
		10	Detected current loop data
		12	Current loop, + receive
		13	Current loop, - transmit
		14	20mA source (+12 volt, no load)
		20	Data Terminal Ready output
		24	Current loop, - receive
		25	Current loop, + transmit

*May be labeled P6 on rear of terminal.

Table 20-2 Continued

Port No.	Description	Pin No.	Function
P4	Printer		
		1	Protect ground
		2	Receive data input
		3	Transmit data output
		4	Request to Send input
		5	Clear to Send output
		6	Data Set Ready output
		7	Signal ground
		8	Data Carrier Detect output
		20	Data Terminal Ready input
P5	Power supply input		
		1	-12 volt supply
		2	Index pin (not installed)
		3	Ground
		4	+5 volt supply
		5	+12 volt supply
P6	Optional modem		
		1	+12 volt supply
		2	Transmit data to modem
		3	Receive data from modem
		4	Not used
		5	-12 volt supply
		6	+5 volt supply
		7	Ground
		8	Ground
		9	+5 volt supply
		10	-12 volt supply
		12	Data clock input to modem
		13	Speaker ouput from modem
		14	+12 volt supply
P7	Optional speaker output		
		1	+5 volt supply
		2	Speaker output
P8	Optional connector (not used)		
P9	Frame ground		
		1	Ground
		2	Ground

INCREASING THE SIZE OF THE 950 SYSTEM ROM



You can increase the size of the 950 system ROM from 4K to 8K by performing the modification described here.

TOOLS REQUIRED

1. 25-watt soldering iron
2. Solder
3. Solder sucker
4. X-ACTO knife or razor blade

PARTS REQUIRED

1. 0.31-guage jumper wire
2. One 28-pin IC socket
3. One 8K ROM (Part No. 2564) or one 8K EPROM (Texas Instruments Part No. 2564)

PROCEDURE

1. Cut the following traces which are located on the solder side of the logic board (as shown in Figure 21-1):

   E23 to E21
   E27 to E28

2. Install the following jumpers (as shown in Figure 21-1):

   E23 to E26
   E21 to E28

3. Remove the ROM which is located in position A41 (Figure 21-1).

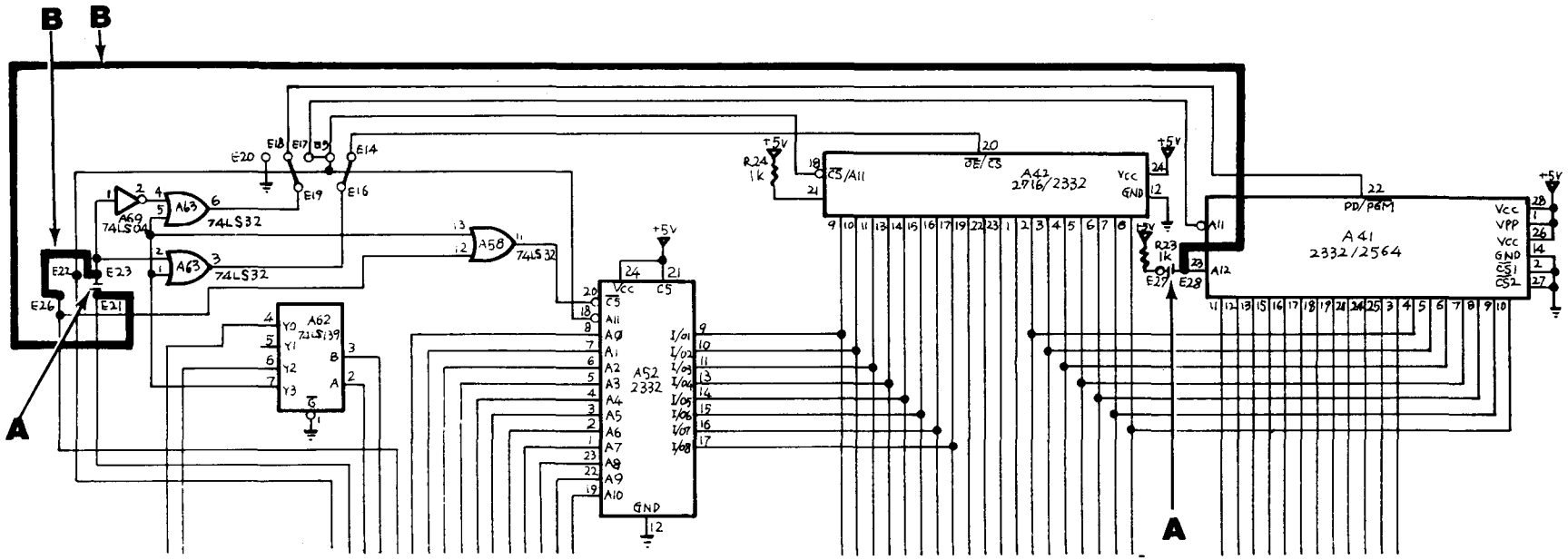
4. Remove the 24-pin IC socket from position A41, taking care not to lift any traces from the board.

5. Install the 28-pin IC socket in position A41.

6. Install the 8K ROM/EPROM in position A41.

7. The starting address for the new EPROM/ROM will be E000 hex.

950



A. Cut Trace
B. Add Jumper

Figure 21-1 Revised Logic Board Schematic, Page 1 of 7

Service Bulletin

Issue No. 23

HOW TO TELL A TTL LOGIC BOARD FROM A GATE ARRAY LOGIC BOARD

TeleVideo® now uses new gate array logic boards in the 910, 910 PLUS, 925, and 950 terminals. Since these boards have fewer components, they are more reliable. Troubleshooting is also simplified.

Although the components are laid out differently, gate array boards are completely interchangable with TTL boards.

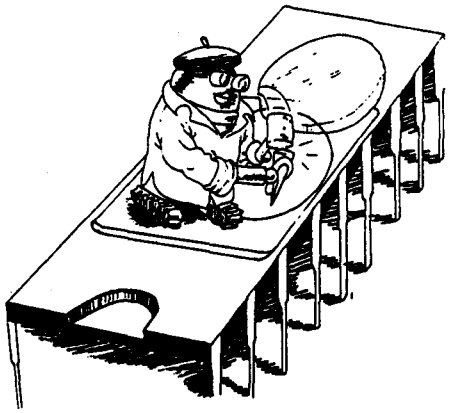


Table 23-1 gives the part number and the location of the gate array chips for each of the models.

Table 23-1 Location of Gate Array Chip(s)

Model No.	Part Number	Location
910, 910 PLUS	2057400	A22
925	2057400	A39
950, Chip A	2057600	A34
Chip B	2057800	A37

Table 23-2 shows the quickest way to determine which type of board is installed in your terminal.

Table 23-2 Determining Type of Logic Board

Model No.	Type of Board	Look for
910, 910 PLUS	TTL	Chip in A22 (14-pin package)
	Gate Array	Chip in A22 (40-pin package)
925	TTL	Size (10"x 12")
	Gate Array	Size (7" x 12")
950	TTL	Color (Blue)
	Gate Array	Color (Green)

You can also determine the type of board you have by comparing it to the illustrations that follow.

ALL

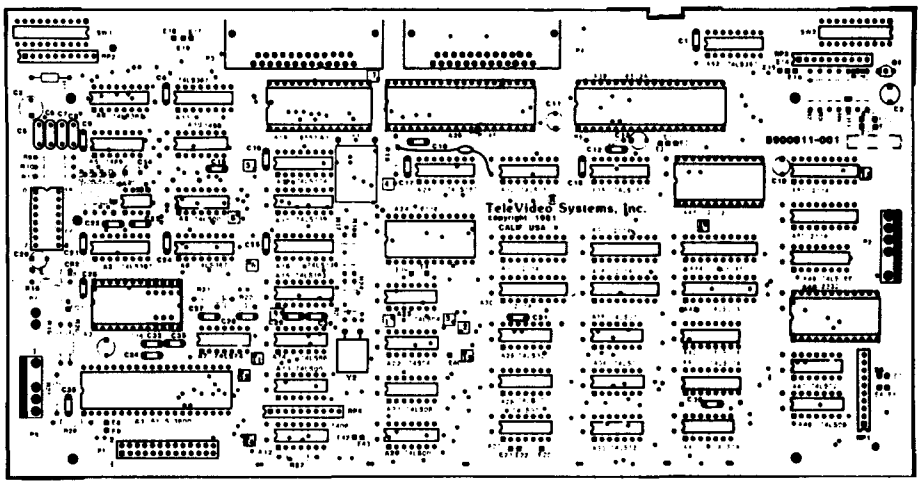


Figure 23-1A 910 or 910 PLUS TTL Logic Board

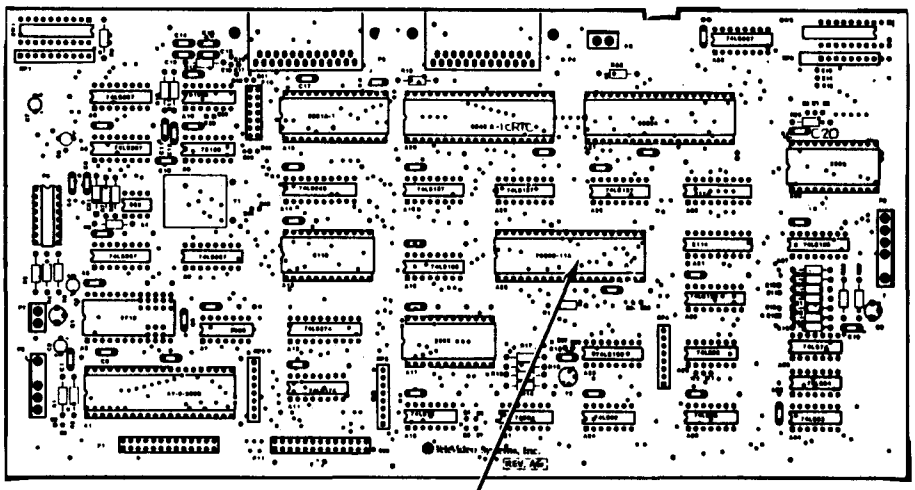


Figure 23-1B 910 or 910 PLUS Gate Array Logic Board

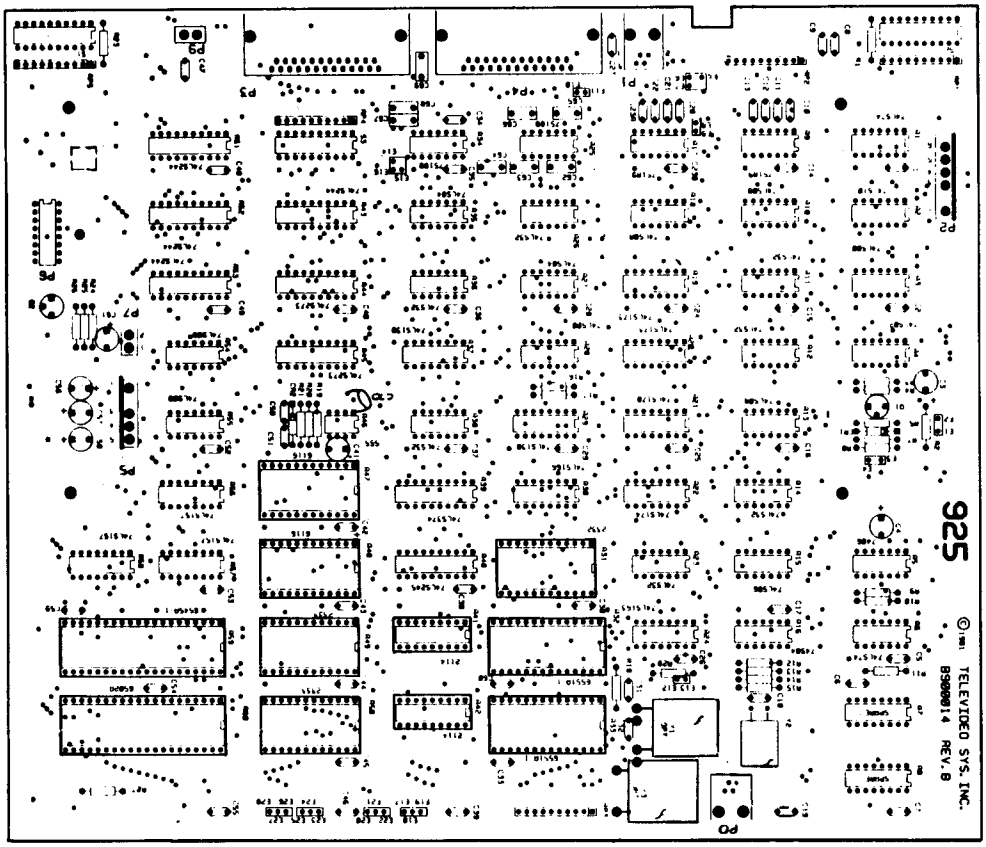


Figure 23-2A 925 TTL Logic Board

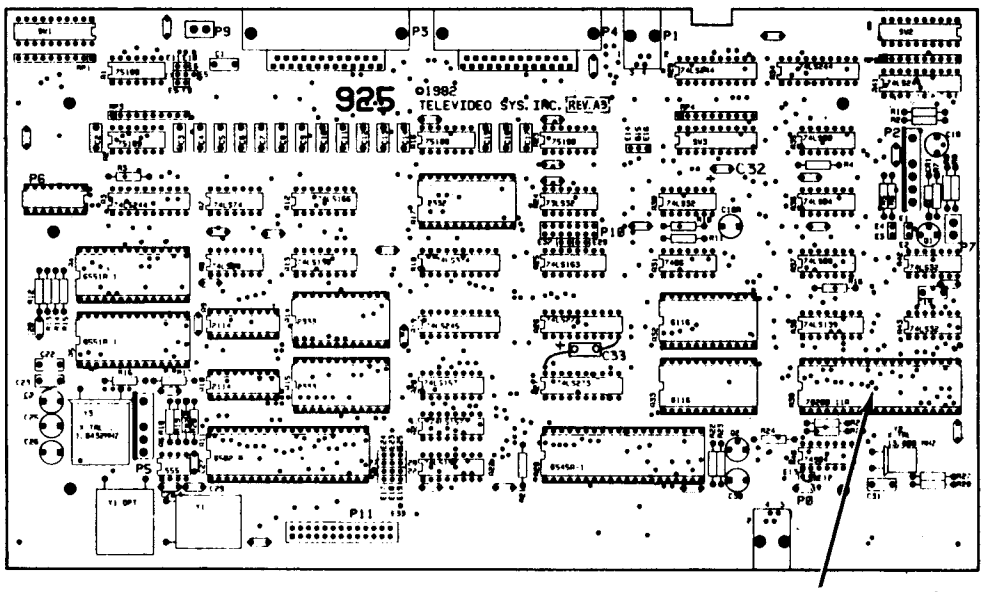


Figure 23-2B 925 Gate Array Logic Board

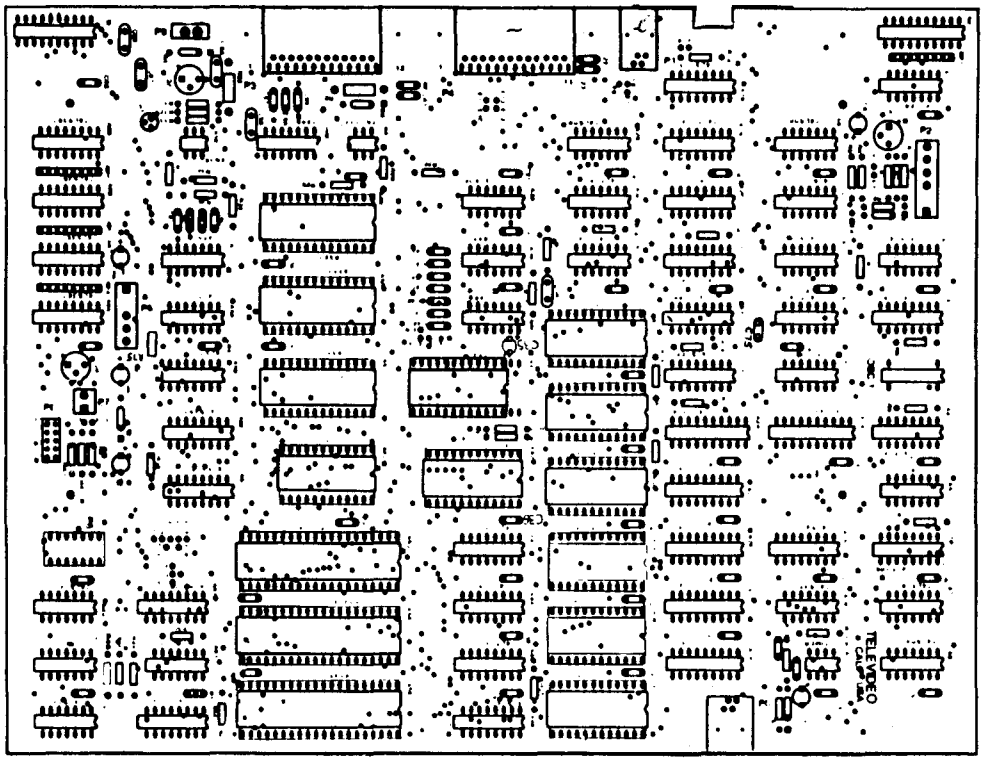
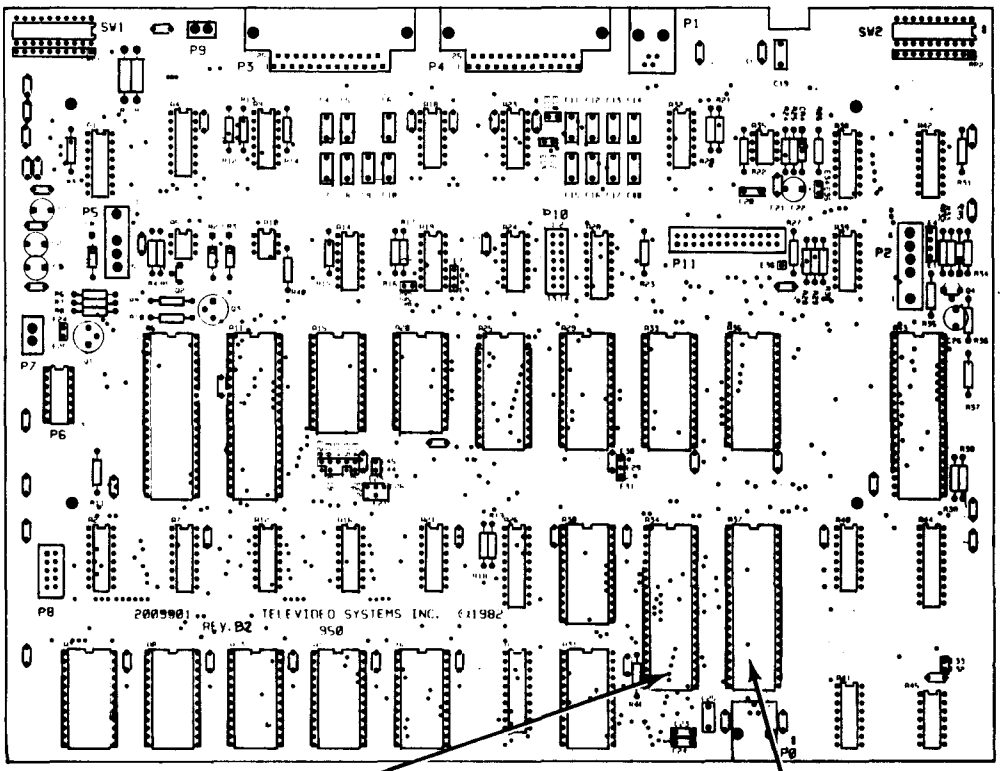


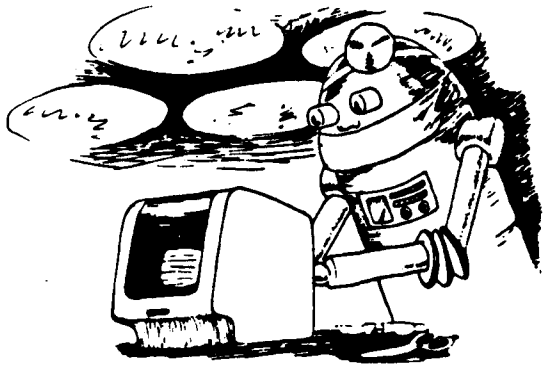
Figure 23-3A 950 TTL Logic Board



Gate Array Chip A Gate Array Chip B

Figure 23-3B 950 Gate Array Logic Board

TESTING THE 6502 ADDRESS LINE



With a 6502 address line tester, you can test all address lines on any logic board that uses a 6502 chip.

When the 6502 receives instruction hex EA (a NOP), it does nothing except increment the program counter and read the next instruction. If the next instruction is also a NOP, the microprocessor is forced to count through all 65,536 possible addresses on its 16-bit address bus.

If you then monitor the address bus lines with an oscilloscope, each address line will display a square wave, with a period twice that of the next lower address line. This gives you a predictable set of signals to trace.

TOOLS REQUIRED

1. Wire cutters
2. Soldering iron
3. Solder

PARTS REQUIRED

1. 40-pin wire wrap socket (not available from TeleVideo)
2. 6502 microprocessor (Part No. 2049600)
3. Jumper wire

PROCEDURE

Construction of test assembly:

1. Cut pins 26 through 33 on the bottom of the wire wrap socket by about 1/4 inch. This will prevent them from making contact with the pins in the socket of the pcb (see Figure 24-1).

2. Wire pins 29, 31, and 33 to pin 1 (ground), and pins 26, 27, 28, 30, and 32 to pin 8 (+5V) to force the hex EA instruction on the data bus (see Figure 24-1).

3. Plug the 6502 into the wire wrap socket. Make sure that its notch faces in the same direction as the notch on the wire wrap socket (see Figure 24-1).

ALL

Operation of test assembly:

1. Remove the 6502 CPU from the board to be tested and set it aside.

2. Install the test assembly (with a known good 6502) in the wire wrap socket. Make sure that the notch faces in the same direction as that on the other chips.

3. Apply power to the logic board.

4. Inspect the address lines for the wave forms listed in Table 1.

5. If you do not detect any pulses on the address lines, check for the following signals:

   Pin 2 Ready (should be high)
   8 +5V
   37 Phase 0 clock
   38 Set overflow (should be high)
   40 Reset (should be high)

   If any of these inputs are held in an incorrect state, the microprocessor will not work. Before continuing, correct any problems with these lines.

Figure 24-1 shows a top and a bottom view of the wire wrap socket.

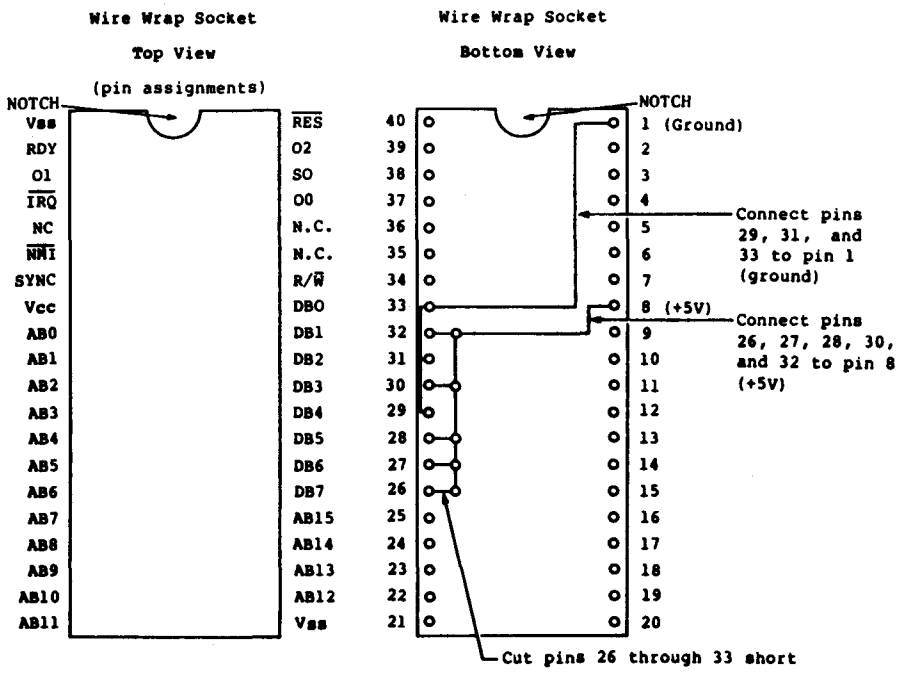


Figure 24-1 Wire Wrap Socket

Table 1

Expected Wave Forms

Pin No	Name	Wave form
1	Vss	Ground
2	RDY	+5V
3	O1 (out)	.6u second period square wave
4	IRQ	+5V noisy
5	N.C.	Ground
6	NMI	+5V noisy
7	SYNC	1.2u second period square wave
8	Vcc	+5V
9	AB0	2.4u second period square wave
10	AB1	4.8u second period square wave
11	AB2	9.6u second period square wave
12	AB3	19.2u second period square wave
13	AB4	38.4u second period square wave
14	AB5	76.8u second period square wave
15	AB6	150u second period square wave
16	AB7	.3m second period square wave
17	AB8	.6m second period square wave
18	AB9	1.2m second period square wave
19	AB10	2.4m second period square wave
20	AB11	4.8m second period square wave
21	Vss	Ground
22	AB12	9.6m second period square wave
23	AB13	19.2 second period square wave
24	AB14	38.4m second period square wave
25	AB15	76.8m second period square wave
26	DB7	Tied high
27	DB6	Tied high
28	DB5	Tied high
29	DB4	Tied low
30	DB3	Tied low
31	DB2	Tied low
32	DB1	Tied high
33	DB0	Tied low
34	R/W	4V to 4.5V noisy
35	N.C.	Ground noisy
36	N.C.	Ground noisy
37	O0 (in)	.6u second period square wave with ringing
38	S.O.	+5V noisy
39	O2 (out)	.6u second period square wave
40	RES	+5V noisy

ENABLING THE DTR LINE ON 950 TERMINALS

To enable the DTR line of the main port of 950 terminals shipped before November 1, 1982, install revision C (or above) firmware. The revision is identified by a letter on the label of the system EPROMs located at positions A41 and A42 on the logic board. (See Figure 25-1.)

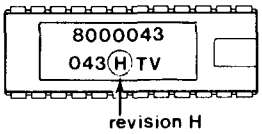


Figure 25-1

You must also perform the hardware modifications described below.

TOOLS REQUIRED:

1. Soldering iron
2. Solder
3. X-ACTO knife or razor blade

PARTS REQUIRED

31-gauge jumper wire

NOTE!

Use care when modifying or repairing any high-density logic board. ANY DAMAGE INCURRED WHILE PERFORMING THIS MODIFICATION MAY RESULT IN INCREASED COST FOR FACTORY REPAIR.

PROCEDURE:

1. Cut the trace that runs between A50 pin 11 and A59 pin 13. (See Figure 25-2)

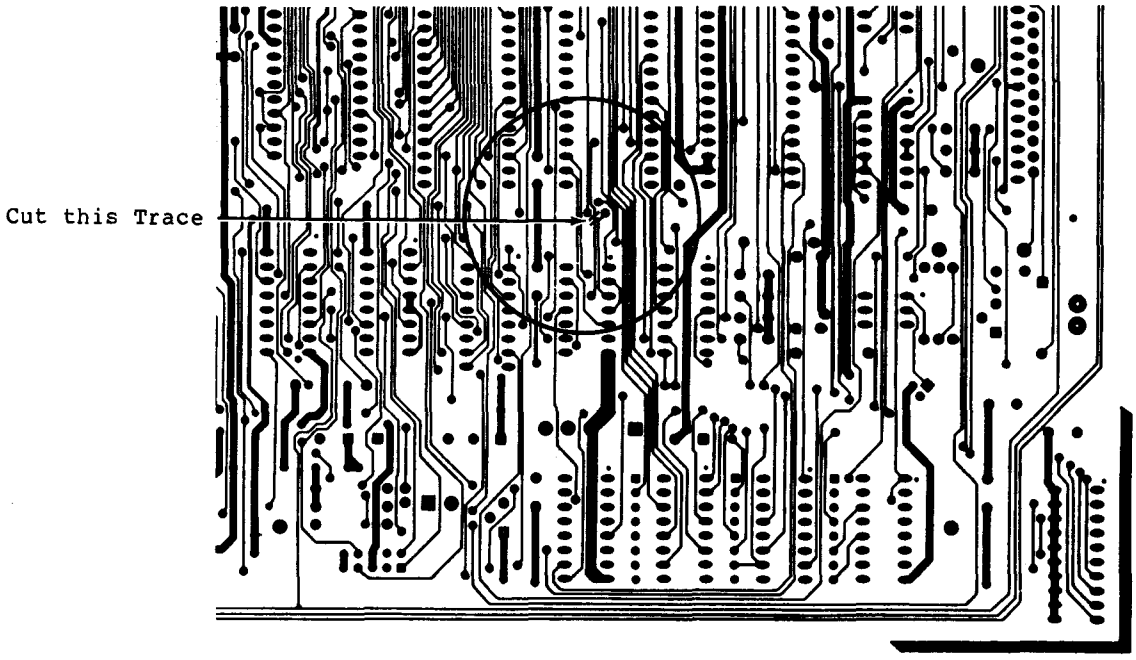


Figure 25-2 Location of Trace to be Cut on Logic Board

950

2. Connect the following jumpers:

   A50 pin 11 to A69 pin 5
   A69 pin 6 to A70 pin 12
   A49 pin 8 to A70 pin 13
   A70 pin 11 to A59 pin 13

3. When this modification is completed, change the schematic as shown in Figure 25-3.

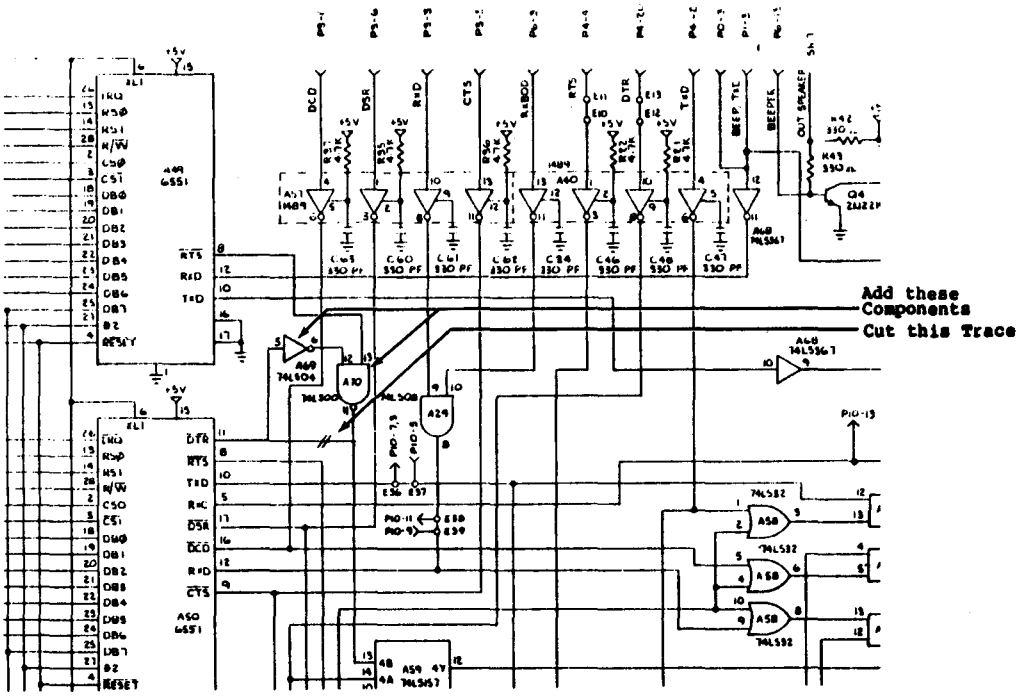


Figure 25-3 Revised Schematic, Page 5 of 7

4. You can now enable or disable DTR handshaking control from the keyboard or system. It is disabled when power is turned on.

   To enable DTR: Enter ^N (this disables X/ON, X/OFF)
   To disable DTR: Enter ^O (this enables X/ON, X/OFF)

Service Bulletin

Issue No. 26.

C306 RELATED FAILURES

Some TeleVideo® terminals shipped during the latter months of 1982 may experience a problem with capacitor C306 on the video module. The symptoms include, but are not limited to:

No video
Bad video
No horizontal deflection
Blowing fuse F102 on the power supply

The suspect capacitor is blue in color and is rated at 20uF, 50V. This capacitor must be replaced with TSI Part No. 2280000 (16uF, 25V nonpolarized capacitor).

If your terminal has experienced one of these symptoms and the suspect capacitor is installed, contact Customer Service, Terminal Division (800/438-8725 x 439 outside California, or 408/745-7760 x 439 in California).

We will have a replacement capacitor sent to you at no charge, or arrange for the module or terminal to be returned to TeleVideo for warranty repair.

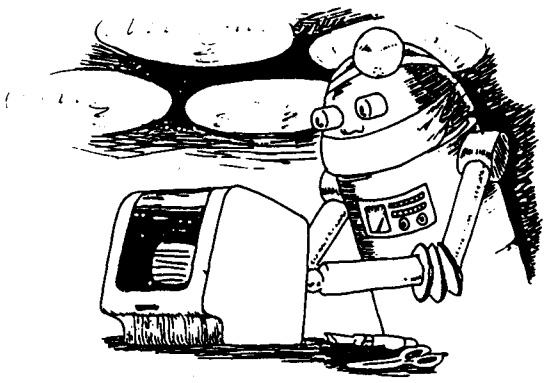
ALL

TeleVideo® Systems Inc.

Service Bulletin

Issue No. 27

925/910/910 PLUS GATE ARRAY CHIP

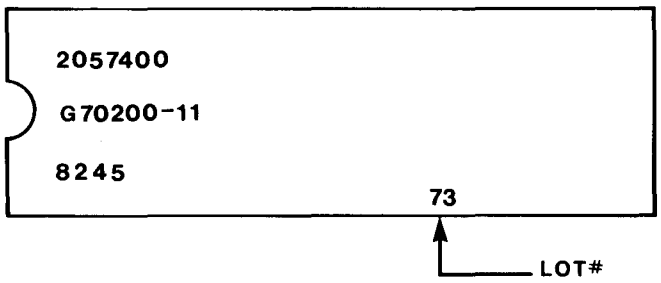


A few TeleVideo® 925, 910, and 910 PLUS terminals shipped in the latter months of 1982 and early months of 1983 may experience difficulties caused by the gate array (G/A) chip on the logic board.

If you have a problem with one of those models, first follow the suggestions in the Troubleshooting section of the operator's manual. Should the problem persist, consult the Terminal Troubleshooting and Repair Guide in the TeleVideo maintenance manual.

If you troubleshoot the terminal according to those sources and the terminal still malfunctions, it is possible that the G/A chip is defective. In that case, open the case and find the chip on the logic board. (The 910 and 910 PLUS G/A chip is in position A22; the 925 G/A chip is in position A39.) Then look at the lot number printed on top of the chip, as shown in Figure 27-1.

Figure 27-1 Location of Lot Number on Gate Array Chip



If the lot number is 72 or less, call the Customer Service Department for the Terminal Division.* We will send you a replacement G/A chip at no charge or arrange for you to return the logic board or terminal to TeleVideo for warranty repair.

Please keep in mind that not all G/A chips from those lots are defective. If your terminal is functioning satisfactorily, the G/A chip does not need to be replaced.

*800/438-8725, extension 439 from outside California; 408/745-7760, extension 439 within California.

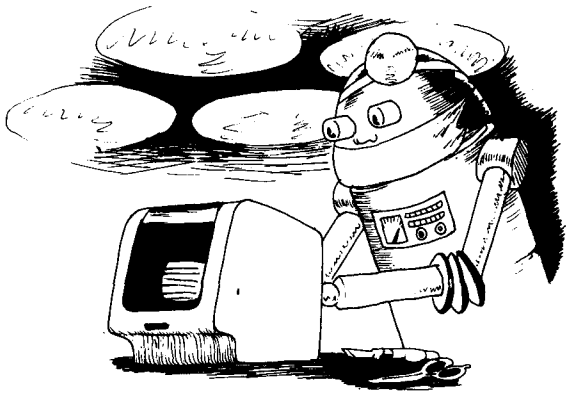
ALL

Service Bulletin

Issue No. 32

WAS THAT CHIP DEFECTIVE, OR JUST A VICTIM OF ESD?

Is your normally reliable terminal suddenly suffering from mysterious glitches and component failures? If so, electrostatic discharge (ESD) could be the culprit.



ESD is by far the most common cause of component failure. The released static charge can damage or destroy circuitry both before and after you install a component. And while some electronic components are less susceptible to ESD than others, most can be affected. ESD can even damage input-protected devices such as EPROMs.

ESD does not always cause instant failure. Because it often causes miniscule degradations of a circuit, a component may function for some time before it mysteriously fails or causes glitches.

Even small amounts of voltage can affect components. A 100-volt charge is enough to damage EPROMs, but you probably would not realize ESD was causing any damage. Most people can not hear or feel ESD unless it's above 3,000 volts. You can generate and hold a charge ten times that amount just by walking across a synthetic carpet.

Avoid ESD damage by setting up your workstation to minimize static build-up. We recommend the following precautions:

1. Wear a wrist grounding strap, grounded through a 1-megohm resistor, when handling components. Be sure it's attached to a metal conduit, pipe, or building frame.

2. Hold boards by their edges to avoid touching pins, traces, connectors, etc. Never slide or throw boards or components.

3. Wear antistatic smocks and cotton gloves. Keep clothing (especially synthetic clothing) away from static-sensitive devices.

4. Use equipment that helps prevent static charge build-up--conductive table mats, for example. Use only static-protective bags and containers.

5. Avoid using parts you know have been mishandled or improperly stored.

SB032 032784

ALL

Repairs Price List for Video Display Terminals

October 1, 1983

REPAIR	Price
Terminal Repair Charge (plus individual charges below)	$ 35.00

INDIVIDUAL REPAIR CHARGES	Price
Logic Board (910/910 PLUS)	$ 50.00
Logic Board (912/920)	$ 65.00
Logic Board (914/924/925/950)	$100.00
Logic Board (970)	$120.00
Keyboard (910/912/920)	$ 30.00
Keyboard (914/924/925/950/970)	$ 50.00
Power Supply (all models)	$ 50.00
Video Board (all models)	$ 50.00
Current Loop Board (910/925)	$ 25.00
Integral Modem	$ 60.00

Service

Nationwide Field Service is available from General Electric Co. Instrumentation and Computer Service Centers. In Canada, service is available from Canadian General Electric Service Centers.

Out of Warranty

Customer to return defective module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send repaired module, billing per above price schedule plus return freight.

Prices subject to change without notice.

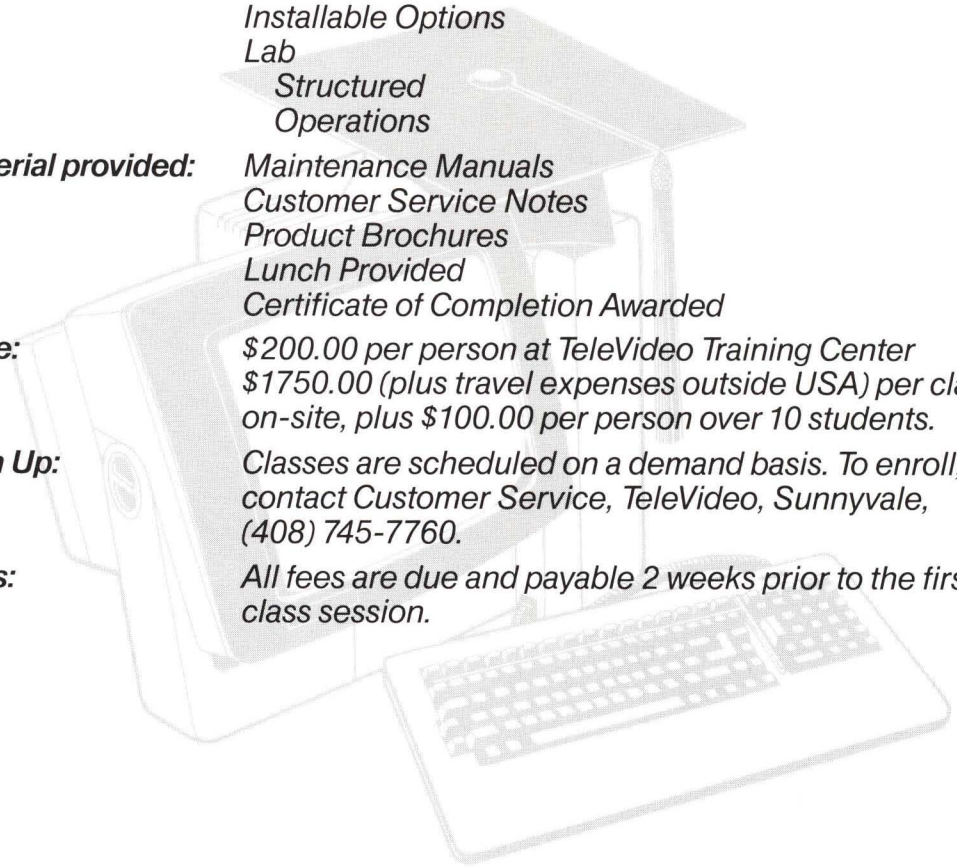
TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

California: Santa Ana (714) 557-6095; Sunnyvale (408) 745-7760 • Georgia: Atlanta (404) 399-6464
Texas: Dallas (214) 980-9978 • Illinois: Bloomingdale (312) 351-9350 • Massachusetts: Boston (617) 668-6891
New York/New Jersey: (201) 267-8805 • London 44-9905-6464 • Paris 33 (1) 687-3440

Terminal Maintenance Training Class

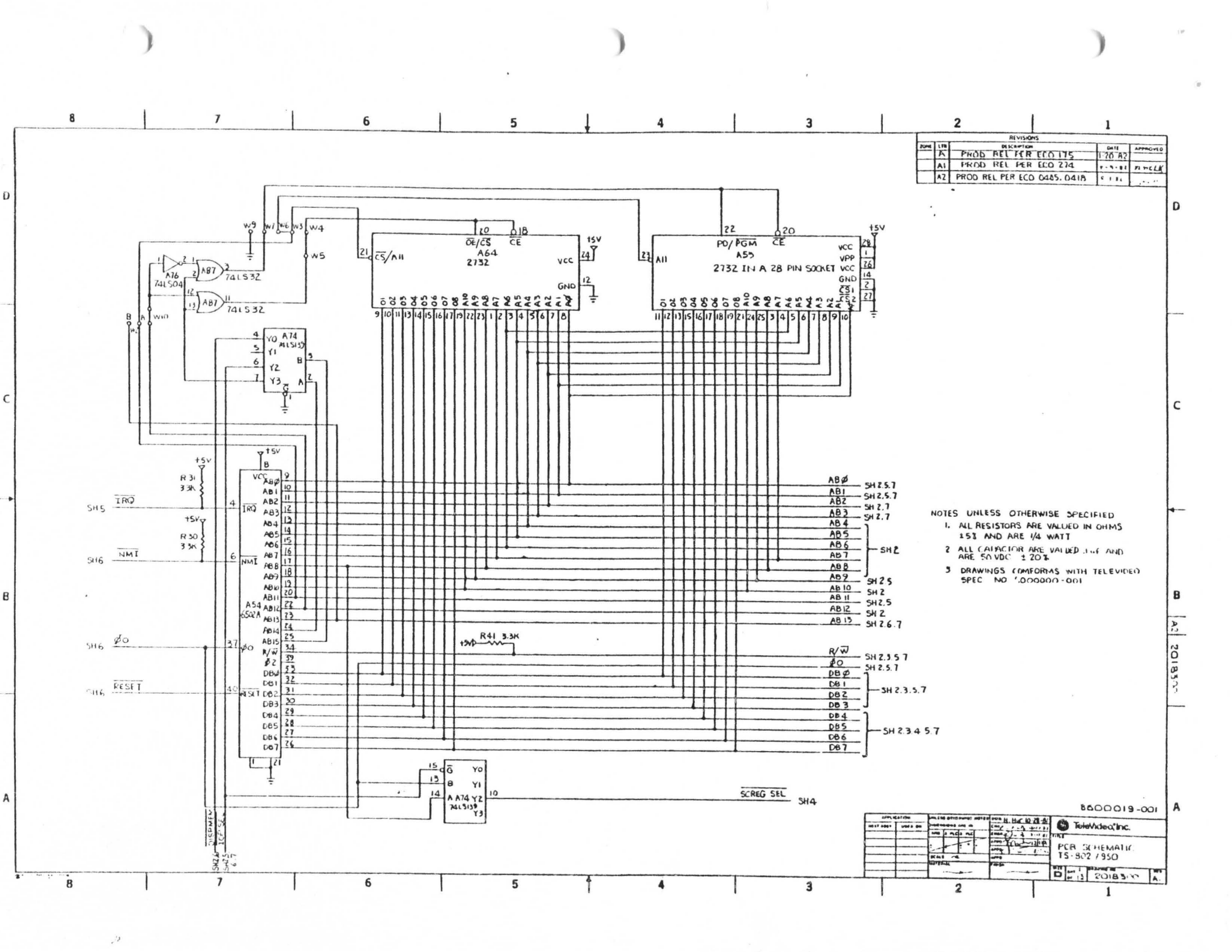
Subjects covered:	*Basic Operation* *Theory of Operation* *Overview of Schematics* *Debug to Component Level* *Interface Considerations* *Installable Options* *Lab* *Structured* *Operations*
Material provided:	*Maintenance Manuals* *Customer Service Notes* *Product Brochures* *Lunch Provided* *Certificate of Completion Awarded*
Price:	*$200.00 per person at TeleVideo Training Center* *$1750.00 (plus travel expenses outside USA) per class on-site, plus $100.00 per person over 10 students.*
Sign Up:	*Classes are scheduled on a demand basis. To enroll, contact Customer Service, TeleVideo, Sunnyvale, (408) 745-7760.*
Fees:	*All fees are due and payable 2 weeks prior to the first class session.*



TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

California: Santa Ana (714) 557-6095; Sunnyvale (408) 745-7760 • Georgia: Atlanta (404) 399-6464
Texas: Dallas (214) 980-9978 • Illinois: Bloomingdale (312) 351-9350 • Massachusetts: Boston (617) 668-6891
New York/New Jersey: (201) 267-8805 • London 44-9905-6464 • Paris 33 (1) 687-3440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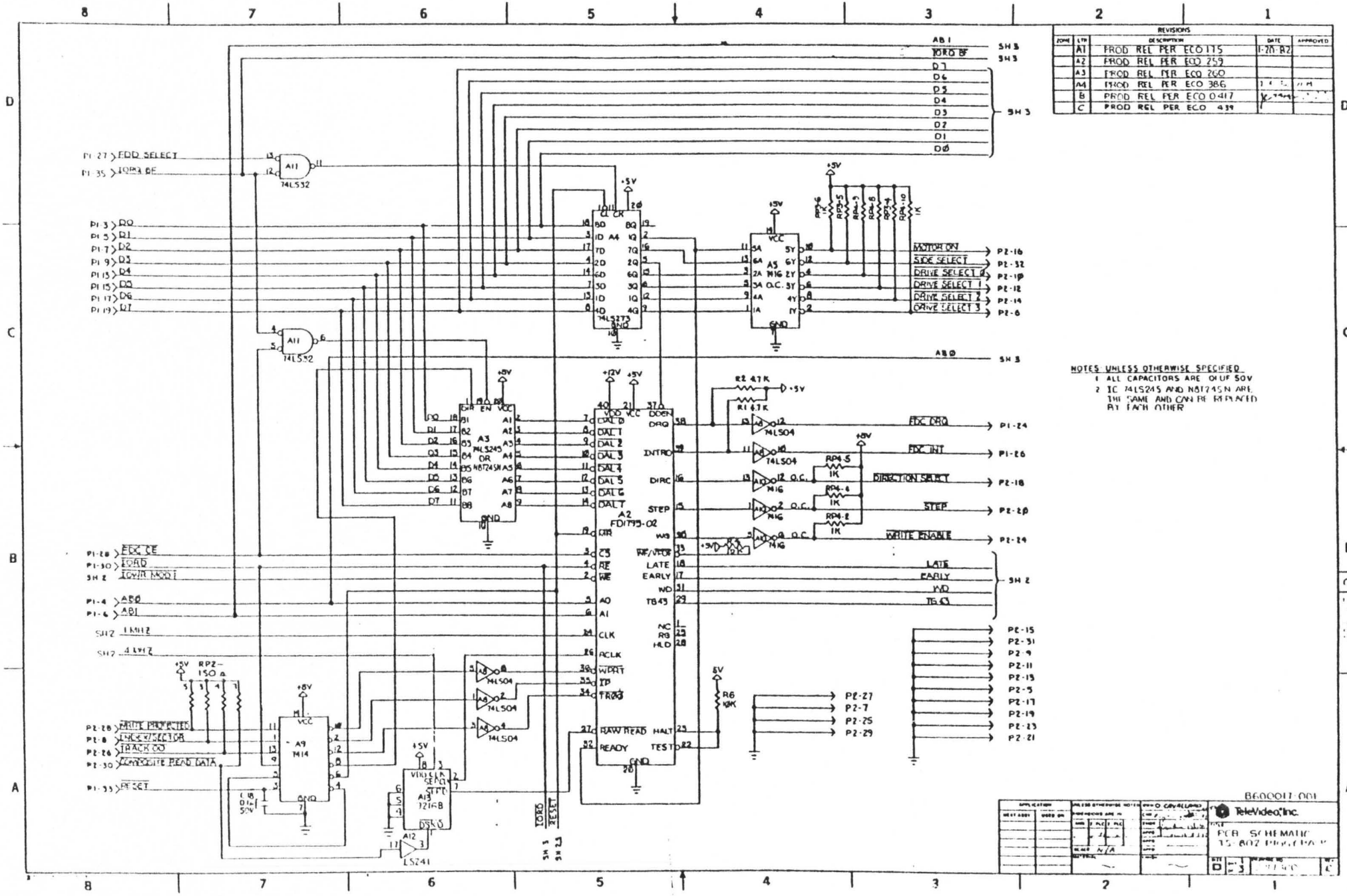
A PROD REL PER ECO 175 1-20-82
A1 PROD REL PER ECO 224 9-9-82 RICHELK
A2 PROD REL PER ECO 0485, 0418 9-1-83
A64 2732
A55 2732 IN A 28 PIN SOCKET
A74 74LS139
A54 6502A
A76 74LS04
A87 74LS32
A81 74LS32
R31 3.3K
R30 3.3K
R41 3.3K
SH5 IRQ
SH6 NMI
SH6 ØO
SH6 RESET
SCREG SEL SH4
NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT
2 ALL CAPACITOR ARE VALUED .1uF AND ARE 50 VDC ± 20%
3 DRAWINGS CONFORMAS WITH TELEVIDEO SPEC NO '.000000-001
B000019-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802/950
D
2018300
A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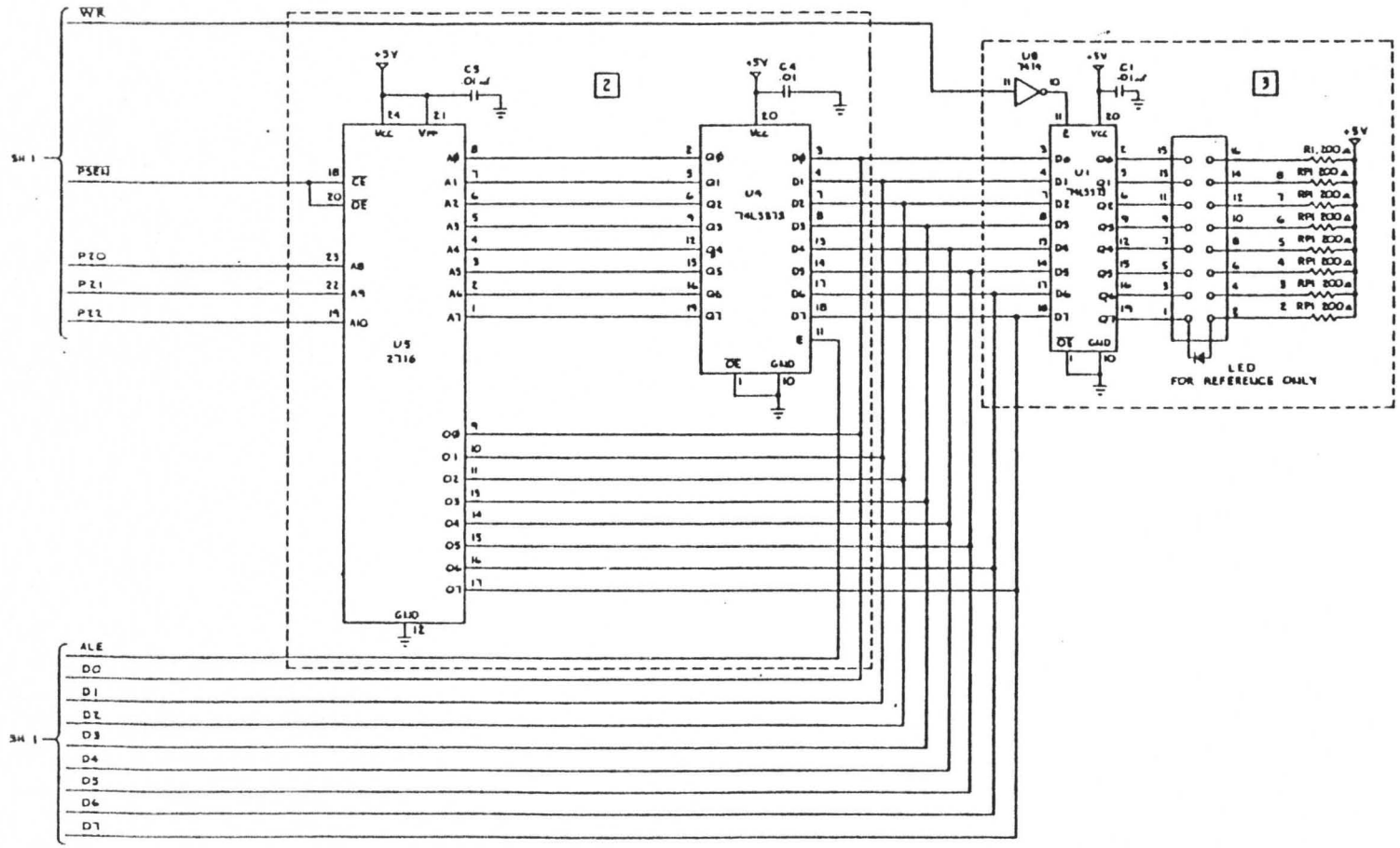
A2 PROD REL PER ECO 259
A3 PROD REL PER ECO 260
A4 PROD REL PER ECO 386
B PROD REL PER ECO 0417
C PROD REL PER ECO 439
NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL CAPACITORS ARE 0.1UF 50V
2 IC 74LS245 AND N8T245N ARE THE SAME AND CAN BE REPLACED BY EACH OTHER
B600011-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802 PROCESSOR



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TeleVideo Inc.

KEYBOARD 950

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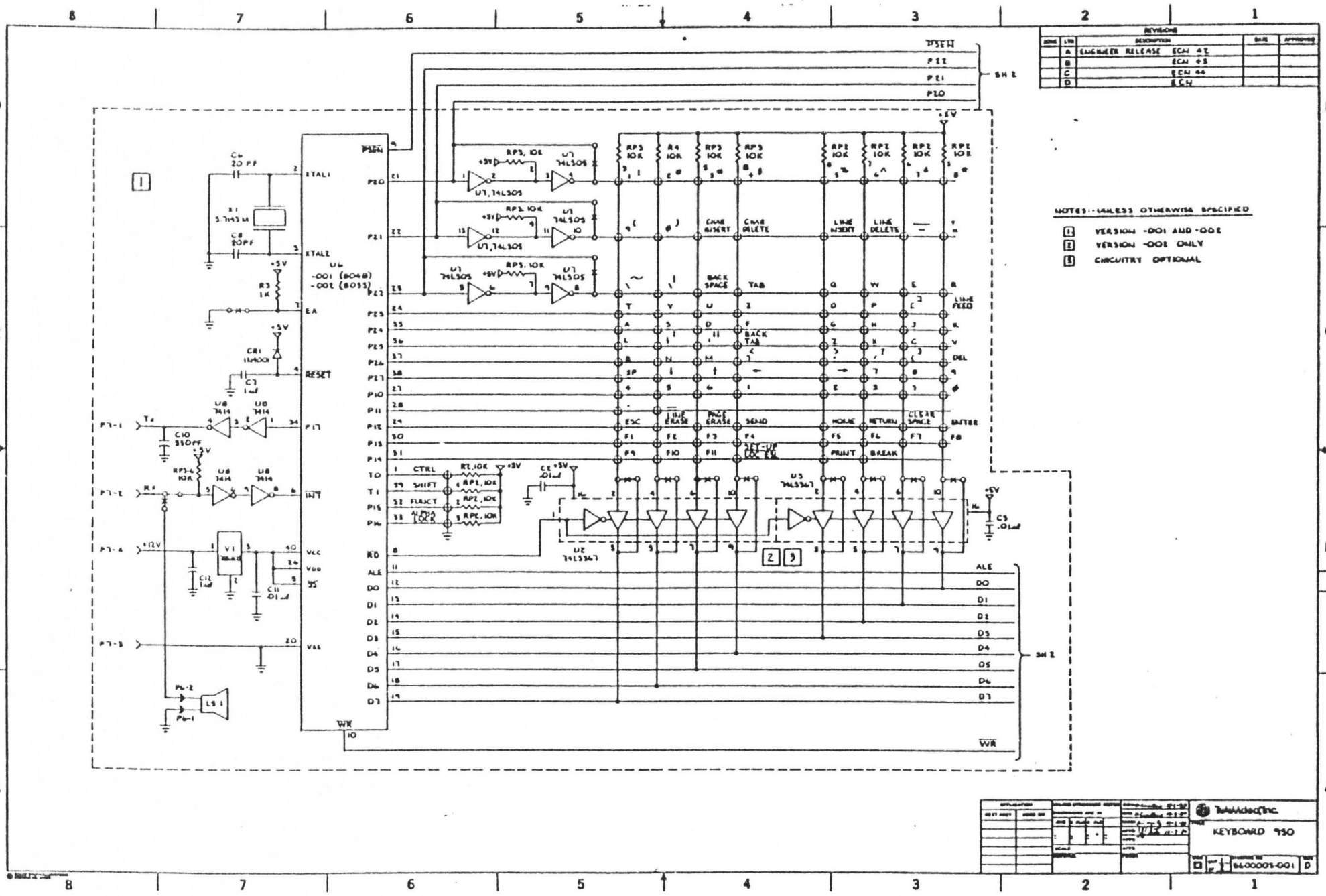
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LTR
DESCRIPTION
DATE
APPROVED
A
ENGINEER RELEASE ECN 43
B
ECN 43
C
ECN 44
D
ECN
NOTES: UNLESS OTHERWISE SPECIFIED
1 VERSION -001 AND -002
2 VERSION -002 ONLY
3 CIRCUITRY OPTIONAL
U6 -001 (8048) -002 (8035)
U7 74LS05
U5 74LS367
U8 7414
RP3 10K
RP2 10K
RP1 10K
RESET
XTAL1
XTAL2
VCC
VDD
VSS
WR
ALE
PSEN
SHIFT
CTRL
ALPHA LOCK
SET-UP LOCK ESC
LINE ERASE
PAGE ERASE
SEND
BACK SPACE
TAB
BACK TAB
LINE FEED
CHAR INSERT
CHAR DELETE
LINE INSERT
LINE DELETE
HOME
RETURN
CLEAR SPACE
ENTER
PRINT
BREAK
KEYBOARD 950
84000015-001
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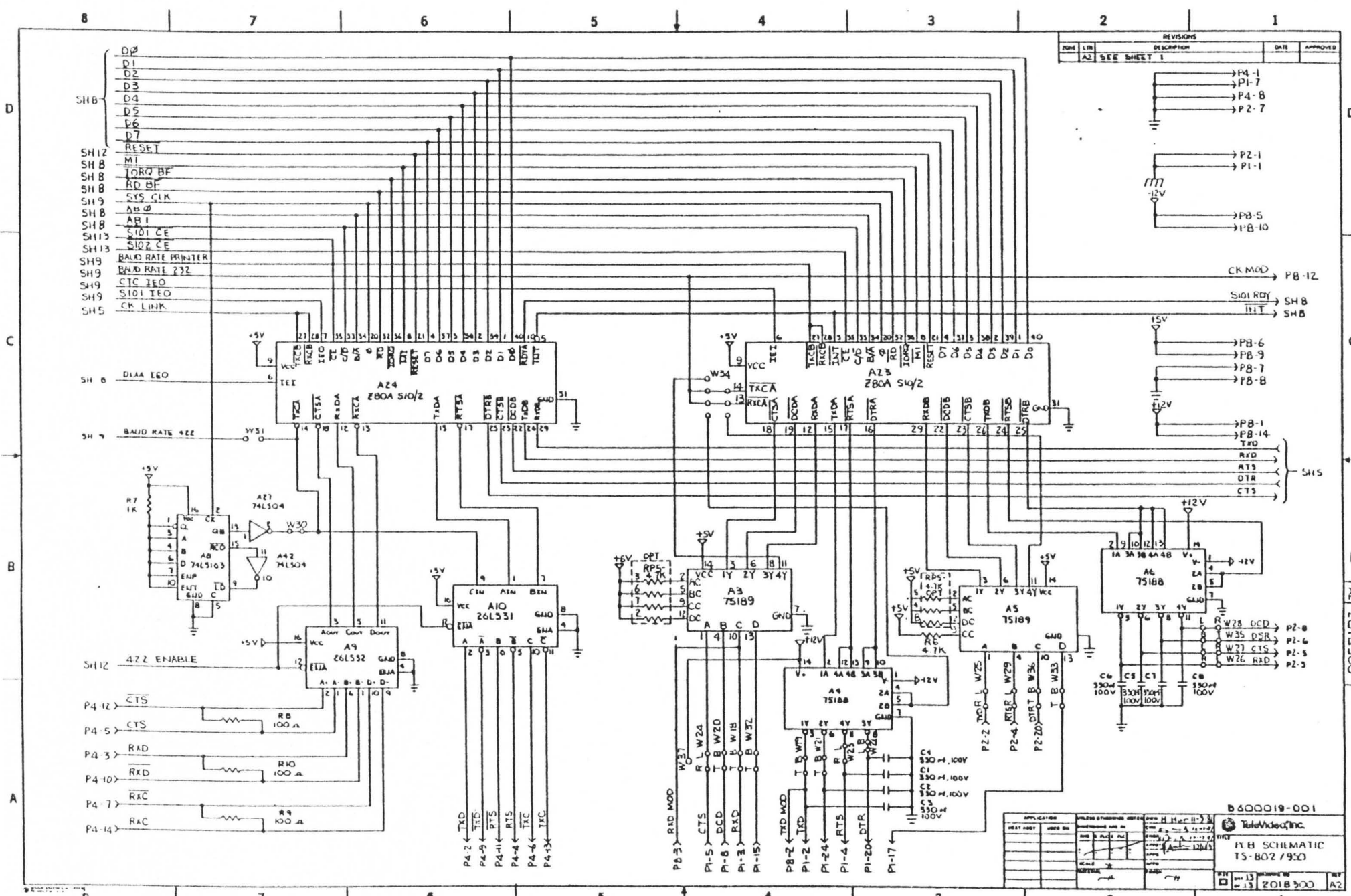
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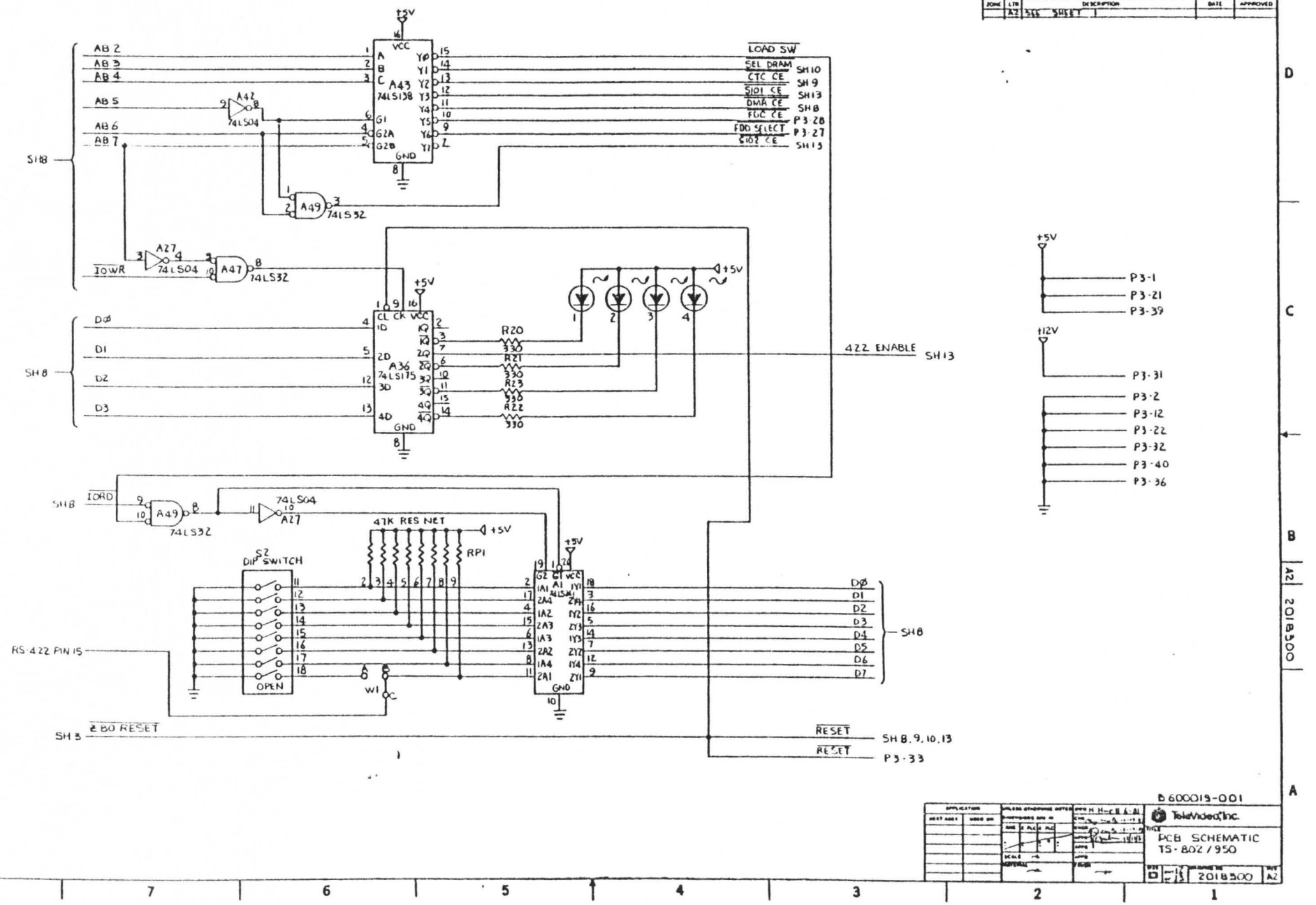
SHB D0 D1 D2 D3 D4 D5 D6 D7
SH12 RESET
SH8 M1
SH8 IORQ BF
SH8 RD BF
SH9 SYS CLK
SH8 AB Ø
SH8 AB 1
SH13 S101 CE
SH13 S102 CE
SH9 BAUD RATE PRINTER
SH9 BAUD RATE 232
SH9 CTC IEO
SH9 S101 IEO
SH5 CK LINK
SH 8 DMA IEO
SH 9 BAUD RATE SEL
SH12 422 ENABLE
P4-12 CTS
P4-5 CTS
P4-3 RXD
P4-10 RXD
P4-7 RXC
P4-14 RXC
AZ4 Z80A SIO/2
AZ3 Z80A SIO/2
AZ7 74LS04
A42 74LS04
A8 74LS163
A10 26LS31
A9 26LS32
A3 75189
A5 75189
A6 75188
A9 75188
R7 1K
RB 100Ω
R9 100Ω
RPS 4.7K
W30
W31
W34
CK MOD P8-12
S101 RDY SHB
INT SHB
P4-1 P1-7 P4-8 P2-7
P2-1 P1-1
P8-5 P8-10
P8-6 P8-9 P8-7 P8-8
P8-1 P8-14
TXD RXD RTS DTR CTS SH15
W28 DCD P2-8
W35 DSR P2-6
W27 CTS P2-5
W26 RXD P2-3
P2-2 P2-4 P2-20
C4 C5 C6 C7 C8 C9 C1 C2 C3
330pf 100V
B600018-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-802/950
2018300 A2



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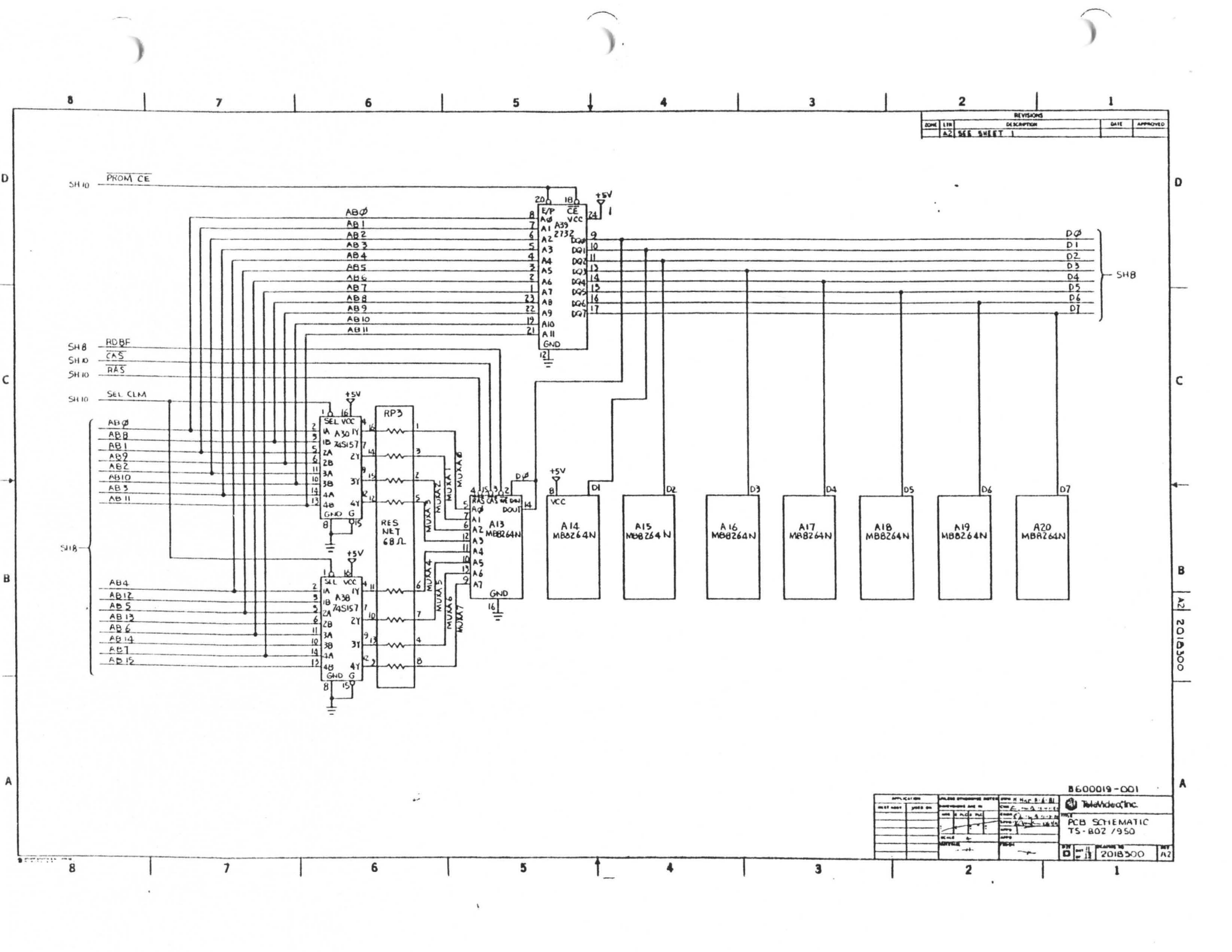
TeleVideo Inc.

PCB SCHEMATIC
TS-802/950

D 2018500 A2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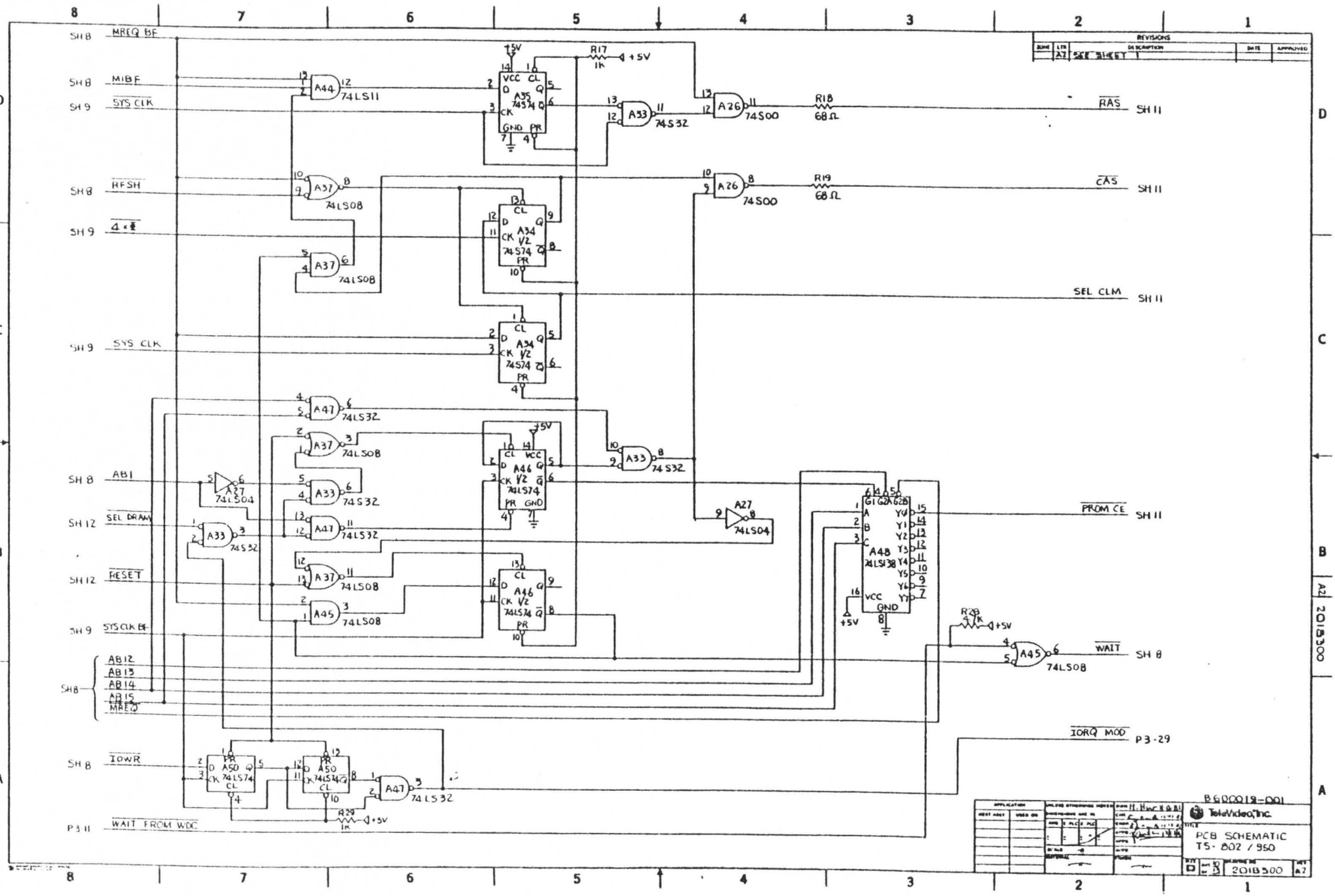
A2 SEE SHEET 1
PROM CE
SH10
ABØ
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
SH8 RDBF
SH10 CAS
SH10 RAS
SH10 SEL CLM
SH8
AB12
AB13
AB14
AB15
A39 2732
E/P CE VCC GND
DQØ DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
DØ D1 D2 D3 D4 D5 D6 D7
SH8
+5V
A30 74S157
A38 74S157
SEL VCC GND G
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
RP3
RES NET 68Ω
MUXA Ø MUXA 1 MUXA 2 MUXA 3 MUXA 4 MUXA 5 MUXA 6 MUXA 7
A13 MB8264N
RAS CAS WE DIN DOUT
A0 A1 A2 A3 A4 A5 A6 A7
A14 MB8264N
A15 MB8264N
A16 MB8264N
A17 MB8264N
A18 MB8264N
A19 MB8264N
A20 MB8264N
VCC
GND
B600019-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802/950
2018300
A2
2018300


SH 8 MREQ BF
SH 8 MIBF
SH 9 SYS CLK
SH 8 RFSH
SH 9 4 x 8
SH 9 SYS CLK
SH 8 AB1
SH 12 SEL DRAM
SH 12 RESET
SH 9 SYSCLK BF
SH 8 AB12
AB13
AB14
AB15
MREQ
SH 8 IOWR
P3 11 WAIT FROM WDC
A44 74LS11
A35 74S74
A33 74S32
A26 74S00
R17 1K
R18 68Ω
R19 68Ω
RAS SH 11
CAS SH 11
SEL CLM SH 11
A37 74LS08
A34 V2 74S74
A47 74LS32
A46 V2 74LS74
A27 74LS04
A48 74LS138
PROM CE SH 11
R20 1K
A45 74LS08
WAIT SH 8
IORQ MOD P3-29
A50 74LS74
R21 1K
+5V
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SEE SHEET
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TeleVideo, Inc.
PCB SCHEMATIC
TS-802 / 950
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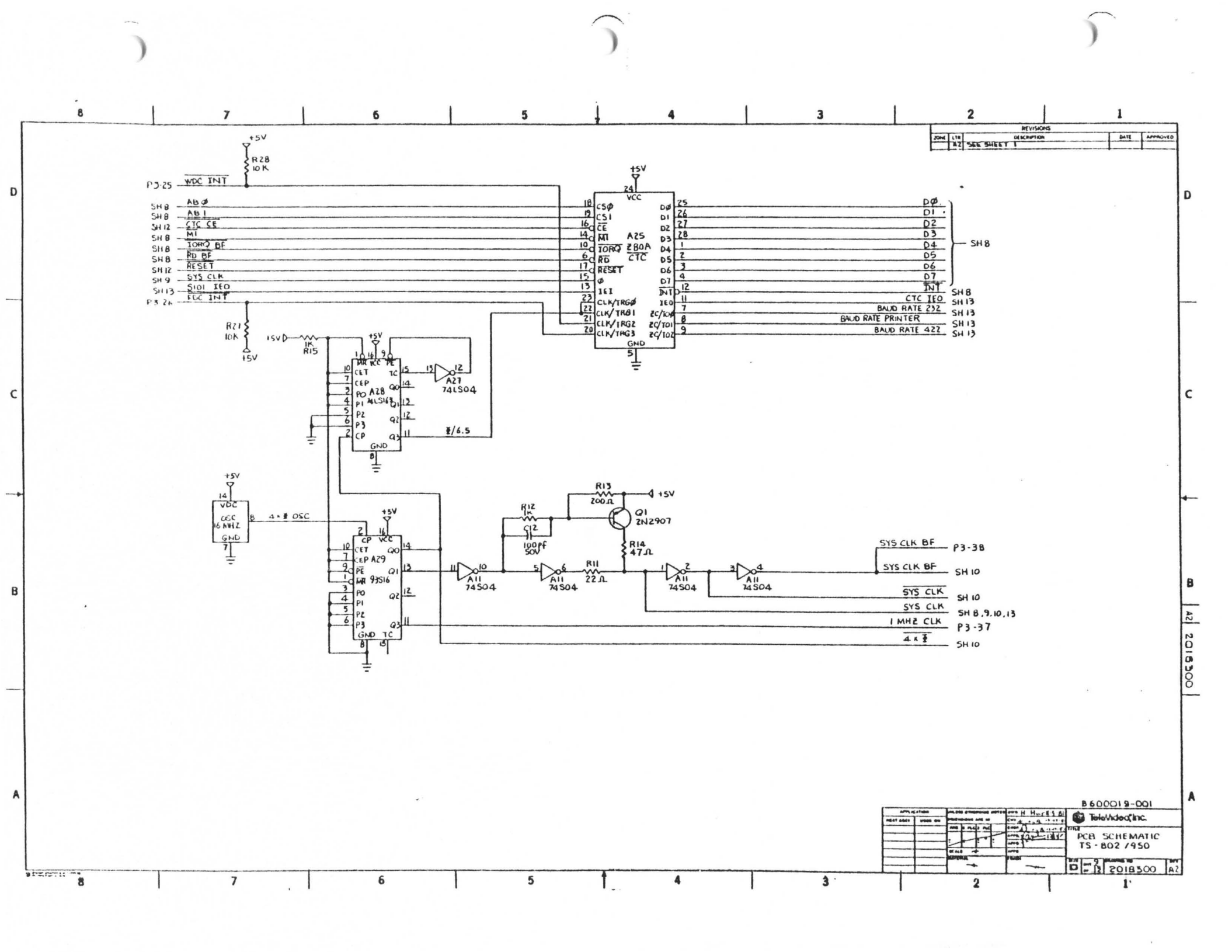
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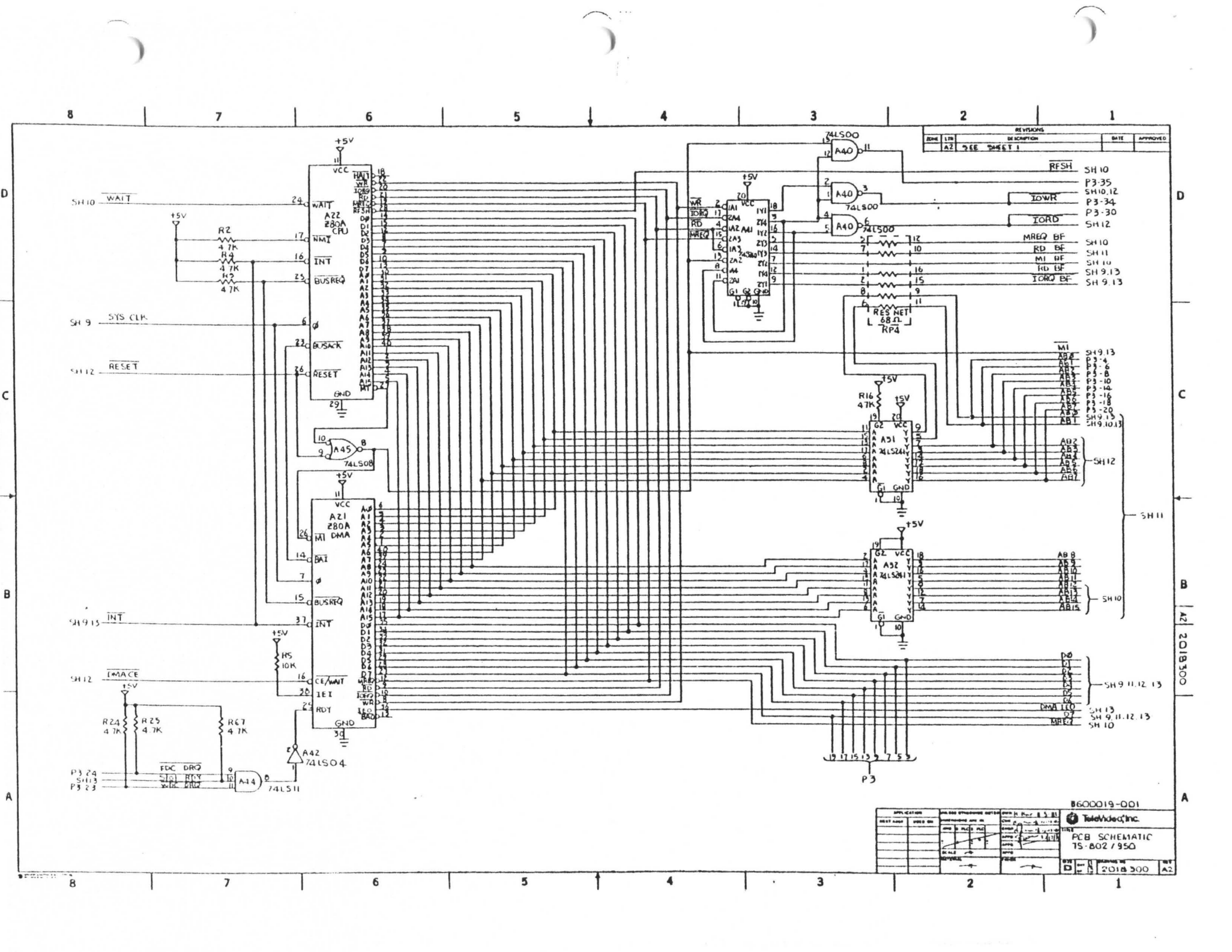
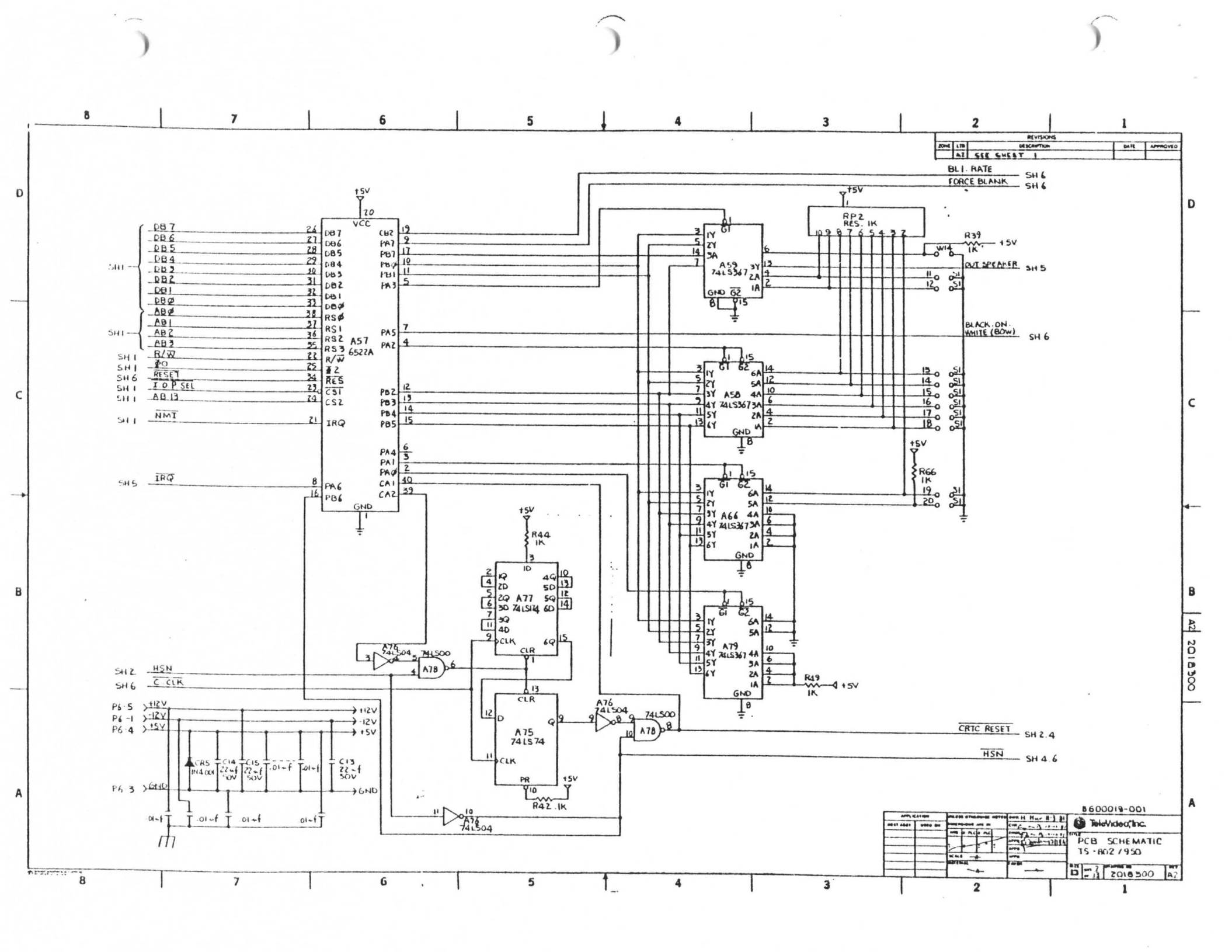
A2 SEE SHEET 1
+5V
R28 10K
P3-25 WDC INT
SH 8 AB Ø
SH 8 AB 1
SH 12 CTC CE
SH 8 M1
SH 8 IORQ BF
SH 8 RD BF
SH 12 RESET
SH 9 SYS CLK
SH 13 SIOI IEO
P3-26 FDC INT
R27 10K
+5V
+5V
1K R15
A25 Z80A CTC
VCC
GND
CS Ø
CS 1
CE
M1
IORQ
RD
RESET
Ø
IEI
CLK/TRG Ø
CLK/TRG 1
CLK/TRG 2
CLK/TRG 3
D Ø
D1
D2
D3
D4
D5
D6
D7
INT
IEO
ZC/TO Ø
ZC/TO 1
ZC/TO 2
D Ø
D1
D2
D3
D4
D5
D6
D7
INT SH 8
CTC IEO SH 13
BAUD RATE 232 SH 13
BAUD RATE PRINTER SH 13
BAUD RATE 422 SH 13
SH 8
A28 74LS163
A27 74LS04
Ø/6.5
+5V
VDC
OSC 16 MHZ
GND
4 x Ø OSC
A29 93S16
R13 200Ω
Q1 2N2907
R12 1K
C12 100pf 50V
R14 47Ω
R11 22Ω
A11 74S04
SYS CLK BF P3-38
SYS CLK BF SH 10
SYS CLK SH 10
SYS CLK SH 8,9,10,13
1 MHZ CLK P3-37
4 x Ø SH 10
B600019-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802/950
D
2018500
A2


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A2 SEE SHEET 1
A22 Z80A CPU
A21 Z80A DMA
A45 74LS08
A42 74LS04
A44 74LS11
A40 74LS00
A31 74LS241
A32 74LS241
A30 74LS30
RES NET 68Ω RP4
R2 4.7K
R3 4.7K
R4 4.7K
R16 4.7K
R24 4.7K
R25 4.7K
R67 4.7K
R5 10K
WAIT
SYS CLK
RESET
INT
DMACE
BUSREQ
BUSACK
NMI
P3 24
P3 23
FDC DRQ
RFSH
IOWR
IORD
MREQ BF
RD BF
M1 BF
IORQ BF
P3
B600019-001
TeleVideo, Inc.
PCB SCHEMATIC
TS-802/950
2018300
A2


REVISIONS
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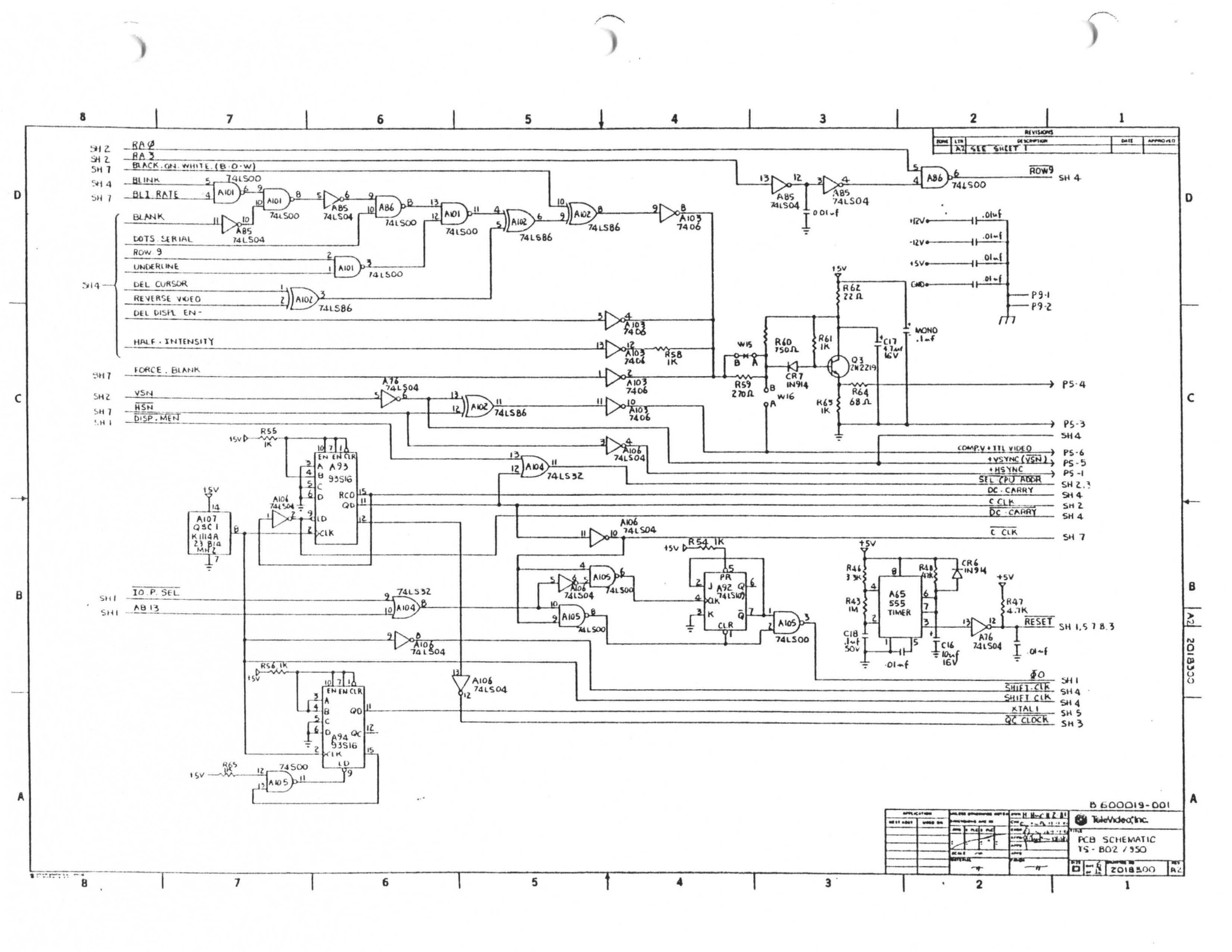
A2 SEE SHEET 1
BLI. RATE
SH 6
FORCE BLANK
SH 6
+5V
VCC
A57 6522A
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
RS0 RS1 RS2 RS3 R/W Ø2 RES CS1 CS2 IRQ
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0
CA1 CA2
GND
SH1 SH1 SH1 SH1 SH6 SH1 SH1 SH1
R/W Ø2 RESET I O P SEL A0 13 NMI
SH5 IRQ
SH2 HSN
SH6 C CLR
RP2 RES. 1K
R39 1K +5V
W14
OUT SPEAKER
SH 5
BLACK ON WHITE (BOW)
SH 6
A59 74LS367
A58 74LS367
A66 74LS367
A79 74LS367
R66 1K
R49 1K +5V
R44 1K
A77 74LS174
A75 74LS74
R42 1K
A76 74LS04
74LS00 A78
CRTC RESET
SH 2.4
HSN
SH 4.6
P6-5 +12V
P6-1 -12V
P6-4 +5V
P6-3 GND
CR5 IN4004
C14 22-f 50V
C15 22-f 50V
.01-f
C13 22-f 50V
8600018-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802/950
2018300
A2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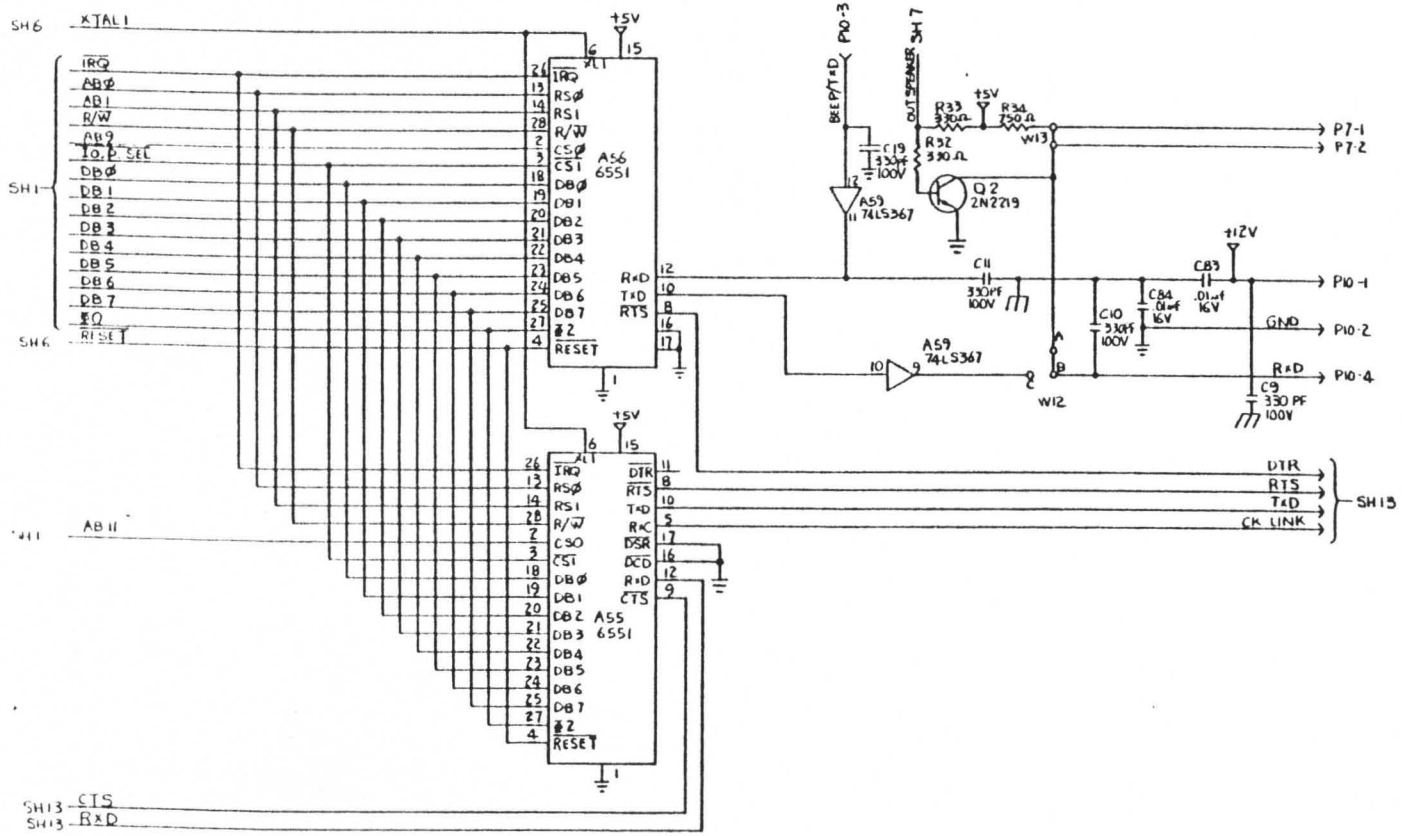
RA Ø
RA 3
BLACK.GN.WHITE.(B.O.W)
BLINK
BLI.RATE
BLANK
DOTS SERIAL
ROW 9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
DEL DISPL EN-
HALF-INTENSITY
FORCE.BLANK
VSN
HSN
DISP.MEN
IO.P.SEL
AB 13
ROW9
SH 4
+12V
-12V
+5V
GND
.01uf
P9-1
P9-2
MONO .1uf
C17 4.7uf 16V
R62 22Ω
R60 750Ω
R61 1K
R64 68Ω
R63 1K
R59 270Ω
R58 1K
W15
W16
Q3 2N2219
CR7 IN914
PS-4
PS-3
PS-6
PS-5
PS-1
COMP.V+TTL VIDEO
+VSYNC (VSN)
+HSYNC
SEL CPU ADDR
DC-CARRY
C CLK
SH 2,3
SH 4
SH 2
SH 4
SH 7
SH 1,5 7 8.3
RESET
ØO
SHIFT.CLK
SHIFT CLK
XTAL1
QC CLOCK
SH 1
SH 4
SH 4
SH 5
SH 3
A65 555 TIMER
R46 3.3K
R43 1M
R48 47K
R47 4.7K
C18 .1uf 50V
C16 10uf 16V
CR6 IN914
A107 QSC1 K1114A 23.814 MHZ
A93 93S16
A94 93S16
A92 74LS107
R55 1K
R54 1K
R56 1K
R65 1K
74LS00
74LS04
74LS86
74LS32
74LS107
B 600019-001
TeleVideo Inc.
PCB SCHEMATIC
TS-802/950
2018300
A2



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
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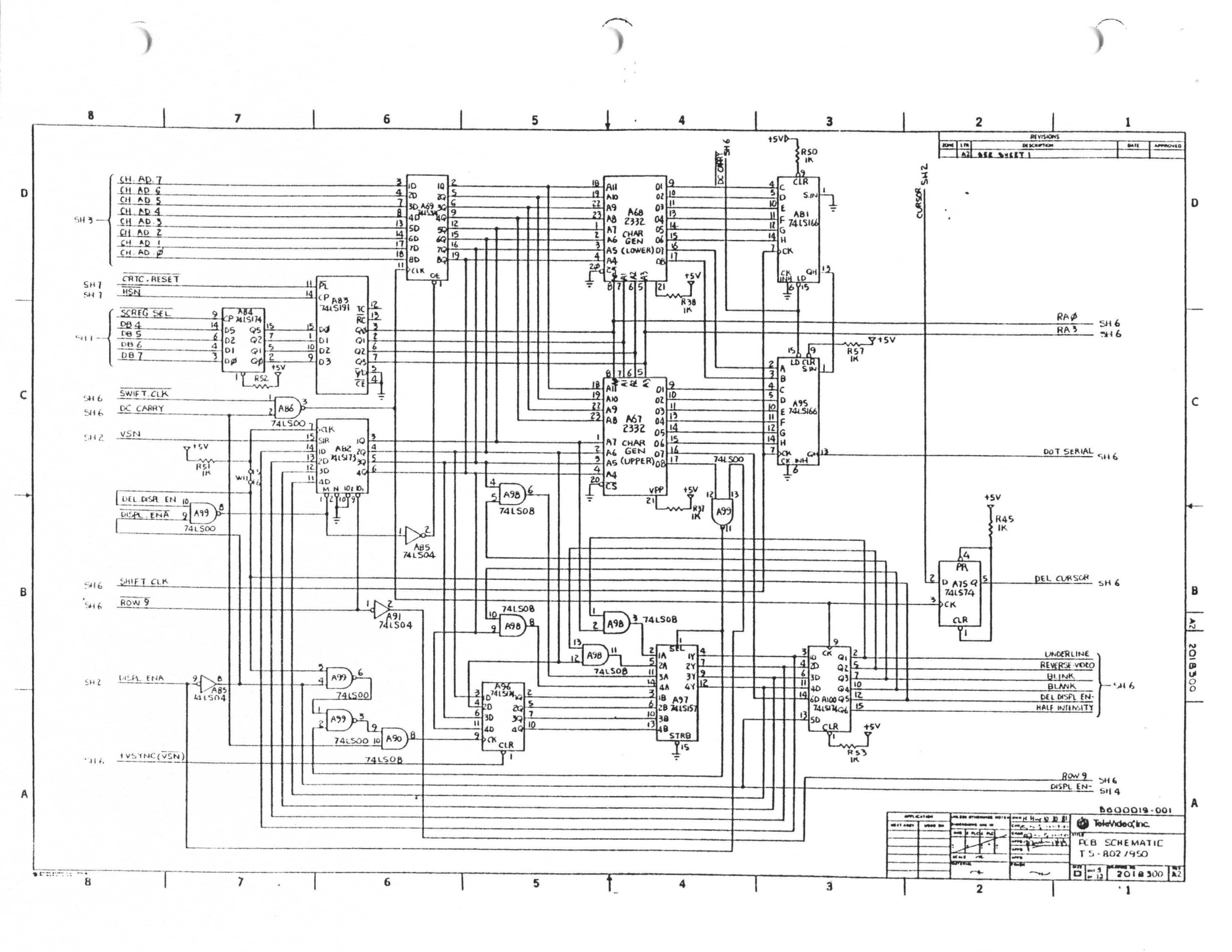
TeleVideo, Inc.

PCB SCHEMATIC
TS-802 / 950

2018300 A2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ZONE | LTR | DESCRIPTION | DATE | APPROVED
A2 | SEE SHEET 1
CH. AD 7
CH AD 6
CH AD 5
CH AD 4
CH AD 3
CH AD 2
CH AD 1
CH. AD Ø
SH 3
CRTC. RESET
HSN
SH 7
SCREG SEL
DB 4
DB 5
DB 6
DB 7
SH 1
SWIFT. CLK
DC CARRY
SH 6
VSN
SH 2
DEL DISP EN
DISPL ENA
SHIFT CLK
ROW 9
DISPL ENA
+VSYNC (VSN)
A68 2332 CHAR GEN (LOWER)
A67 2332 CHAR GEN (UPPER)
A95 74LS166
A81 74LS166
A83 74LS191
A84 74LS174
A82 74LS173
A96 74LS174
A97 74LS157
A75 74LS74
A100 74LS174
R50 1K
R57 1K
R38 1K
R37 1K
R52
R51 1K
R45 1K
R53 1K
+5V
74LS00
74LS08
74LS04
RA Ø
RA 3
DOT SERIAL
DEL CURSOR
UNDERLINE
REVERSE VIDEO
BLINK
BLANK
DEL DISPL EN-
HALF INTENSITY
ROW 9
DISPL EN-
B000019-001
TeleVideo Inc.
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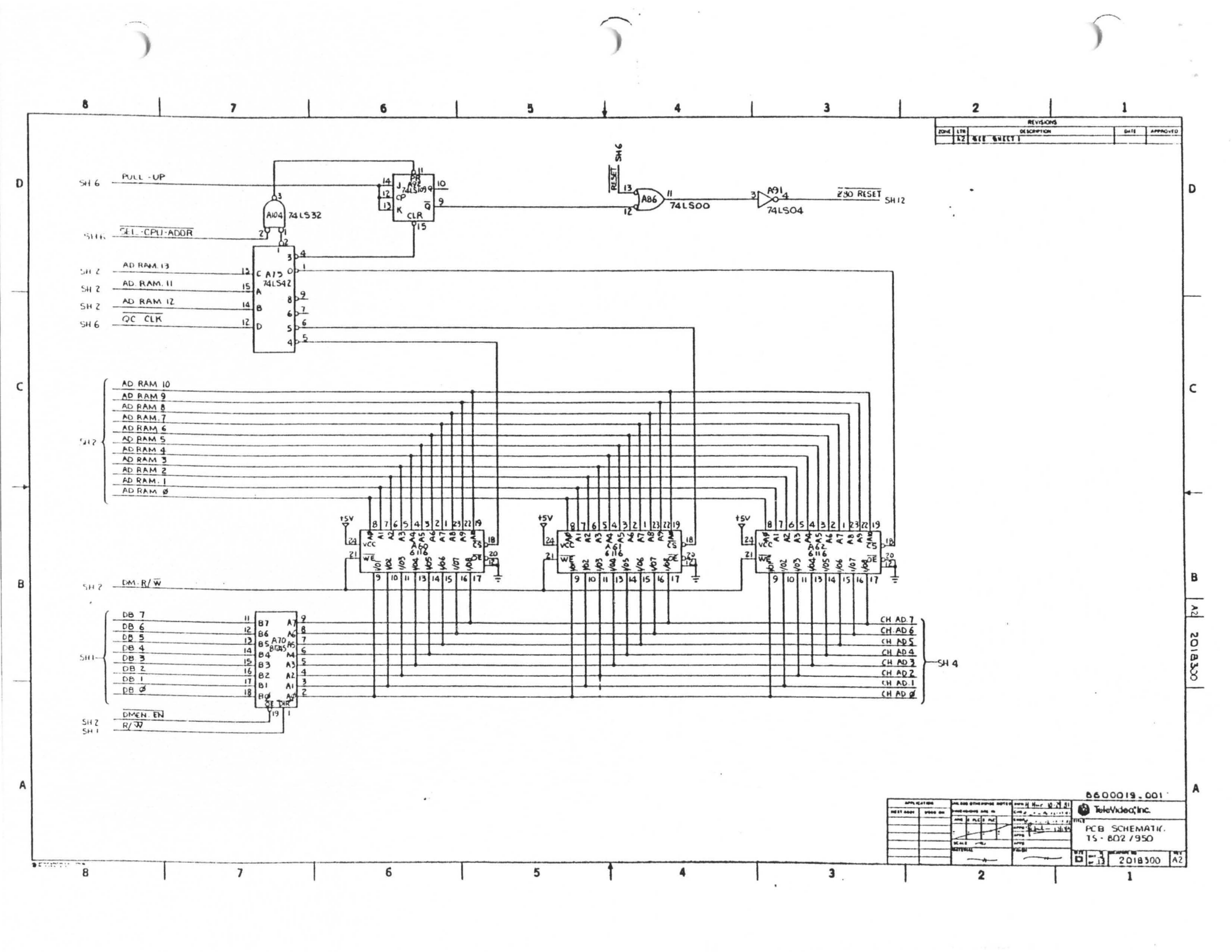
TS-802/950
201@300
A2


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
12 REF SHEET 1
PULL-UP
SEL-CPU-ADDR
AD RAM 13
AD RAM 11
AD RAM 12
QC CLK
A104 74LS32
A73 74LS42
A74 74LS109
RESET
A86 74LS00
A91 74LS04
Z80 RESET
AD RAM 10
AD RAM 9
AD RAM 8
AD RAM 7
AD RAM 6
AD RAM 5
AD RAM 4
AD RAM 3
AD RAM 2
AD RAM 1
AD RAM Ø
DM R/W
DB 7
DB 6
DB 5
DB 4
DB 3
DB 2
DB 1
DB Ø
A70 8T245
DMEN EN
R/W
+5V
CH AD 7
CH AD 6
CH AD 5
CH AD 4
CH AD 3
CH AD 2
CH AD 1
CH AD Ø
SH 4
8600019-001
TeleVideo, Inc.
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TS-802/950
2018300
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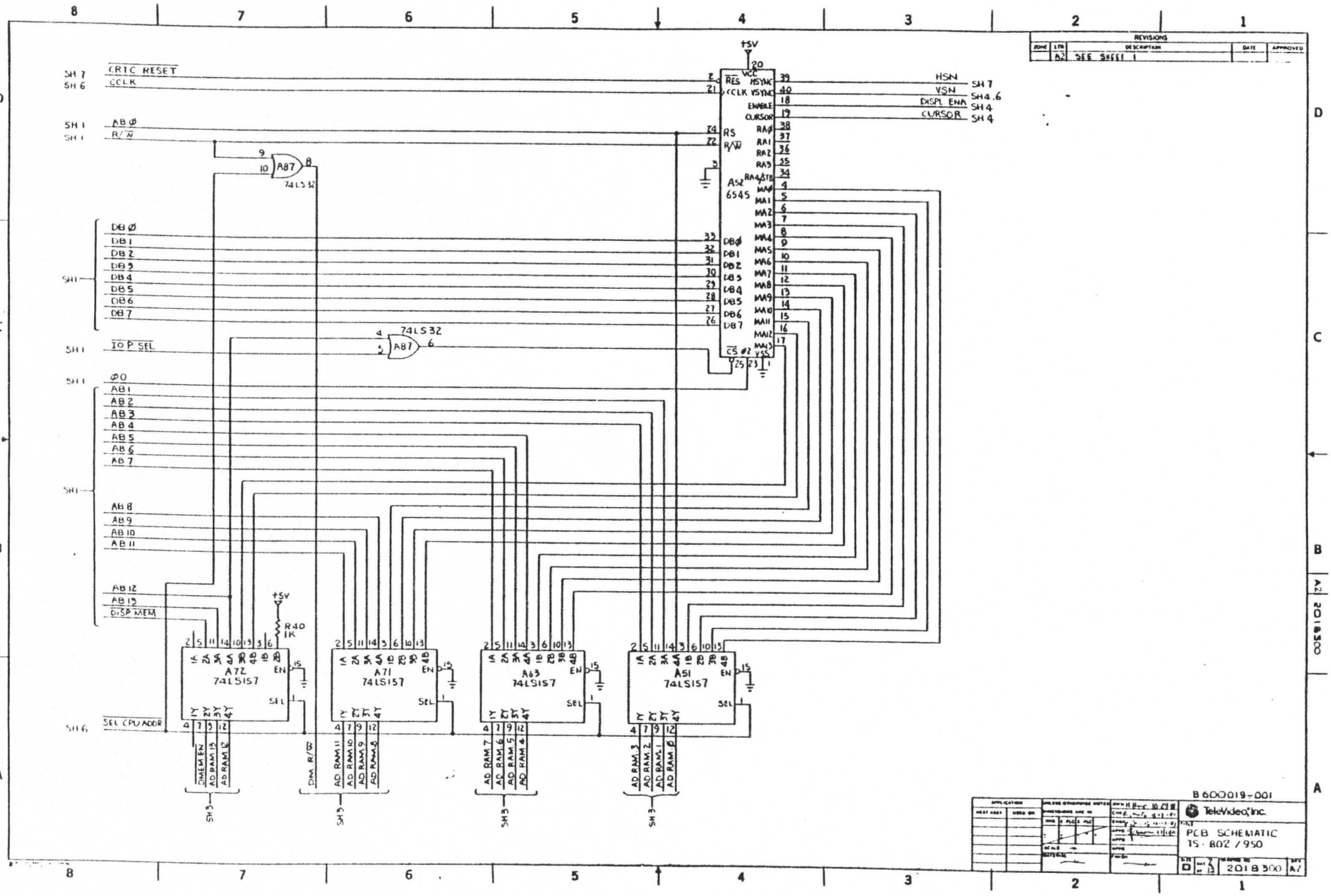
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A2 SEE SHEET 1
+5V
CRTC RESET
CCLK
AB Ø
R/W
DB Ø
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7
IO P SEL
Ø0
AB 1
AB 2
AB 3
AB 4
AB 5
AB 6
AB 7
AB 8
AB 9
AB 10
AB 11
AB 12
AB 13
DISP MEM
SEL CPU ADDR
A87
74LS32
A52
6545
A72
A71
A63
A51
74LS157
R40
1K
HSN
VSN
DISPL ENA
CURSOR
SH 7
SH 4,6
SH 4
DMEM EN
AD RAM 13
AD RAM 12
DMA R/W
AD RAM 11
AD RAM 10
AD RAM 9
AD RAM 8
AD RAM 7
AD RAM 6
AD RAM 5
AD RAM 4
AD RAM 3
AD RAM 2
AD RAM 1
AD RAM Ø
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