TEK SERVICE MANUAL

Part No. 070-4759-00
Product Group 61

8560/8561/8562 Multi-User Software Development Unit

Service Manual

Tektronix
COMMITTED TO EXCELLENCE

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Please check for change information at the rear of this manual

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Tektronix®
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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Printed in U.S.A.

PREFACE

INTRODUCTION

This manual supports the service, installation, and verification of the TEKTRONIX 8560 Series Multi-User Software Development Units (MUSDUs). Since this manual is a Service Manual and not a User's Manual, it contains only those operating instructions necessary to perform system verification procedures. The manual is sufficiently detailed to permit service technicians to perform on-site board-level repairs.

Relationship to Other Equipment

The 8560 MUSDU is used primarily in conjunction with the 8540 Integration Unit. These two units constitute a complete microcomputer development lab. Uses of this lab are described in separate user manuals.

Products Supported

This manual supports the 8560 (SN B100000 and above), the 8561 (SN B100000 and above), and the 8562 Multi-User Software Development Units. The following table summarizes the basic differences between these products.

System Components	8561 SN B100000 and up	8560 SN B100000 and up	8562
Microprocessor	LSI-11/23 (LSI-11/73 optional upgrade)	LSI-11/23 (LSI-11/73 optional upgrade)	LSI-11/73
Internal disk mass storage capacity	15M bytes (55M bytes with optional upgrade 40M-byte disk)	40M bytes (80M bytes with optional upgrade 40M-byte disk)	40M bytes (80M bytes with optional upgrade 40M-byte disk)
External disk(s) mass storage capacity	Up to 2 external disks	Up to 2 external disks	Up to 2 external disks
System memory	256K bytes (up to 1M bytes optional upgrade)	256K bytes (up to 1M bytes optional upgrade)	1M bytes
Disk Controller	MSC	MSC	MSC
Number of users supported	2 (4 or 8 optional)	4 (8 optional)	8

Definition of Terms

In this manual, any references to the 8560 apply equally to the 8561 and the 8562, with the following exceptions:

- The standard 8561 has a hard disk storage capacity of 15M bytes, while the standard 8560 and 8562 have a hard disk storage capacity of 40M bytes.
- The standard version of the 8561 supports two users. The standard version of the 8560 supports four users, while the standard version of the 8562 supports eight users.
- Any reference to a second IOP Board applies to the 8562, and to all 8560 and 8561 units that include the Eight-User Upgrade Option.

ABOUT THIS MANUAL

This manual introduces you to the 8560 Series MUSDUs and describes their hardware operation at a block diagram level. This manual is divided into 22 sections providing the following information:

Section 1 An introduction to the 8560 Series MUSDU and information of general interest.

Section 2 The electrical specifications, physical characteristics and environmental characteristics.

Section 3 A brief description of front and rear panel controls, connectors and indicators. This section also provides locations and functions of all 8560 Series MUSDU straps and jumpers and their default positions.

Section 4 A description of the LSI-11 Processor.

Section 5 A description of the Utility Board.

Section 6 A description of the system memory boards.

Section 7 A description of the I/O Processor Board.

Section 8 A description of the I/O Adapter Board and I/O Connector Board.

Section 9 A description of the MSC Board.

Section 10 A description of the Xebec S1410 Disk Controller.

Section 11 A general description of the hard disk and flexible disk drive units.

Section 12 A description of the power supply. This section also contains procedures for bringing up and adjusting the supply.

Section 13 Descriptions of power-up diagnostic test routines.

Section 14 Adjustment procedures.

Section 15 General preventive maintenance procedures to improve equipment reliability.

Section 16 Descriptions of disk-based diagnostic test routines and their use in isolating problems.

Section 17 A list of 8560 Series MUSDU accessories.

Section 18 Instructions for installing the 8560 Series MUSDUs.

Section 19 Reference material, including bus signal mnemonic descriptions, and Main Interconnect Board connector-pin assignments.

Section 20 Electrical Parts list.

Section 21 Diagrams.

Section 22 Mechanical Parts list.

Notational Conventions

Nomenclature

Throughout this manual, the following terminology is used:

- All references to an 8560, 8560 Series MUSDU or MUSDU include the 8560 (SN B100000 and above), the 8561 (SN B100000 and above) and the 8562 Multi-User Software Development Unit(s).
- All references to an 8540 refer to the 8540 Integration Unit.
- All references to a terminal or system terminal refer to any terminal used for command entry which is connected to the 8540 Integration Unit or to the 8560 Series MUSDU.

The term LSI-11, as used in this manual, includes the LSI-11/23 and the LSI-11/73, unless otherwise specified. The terms LSI-11/23, LSI-11/73 and DEC are registered trademarks of the Digital Equipment Corporation, Maynard, Massachusetts.

Signal Line Conventions

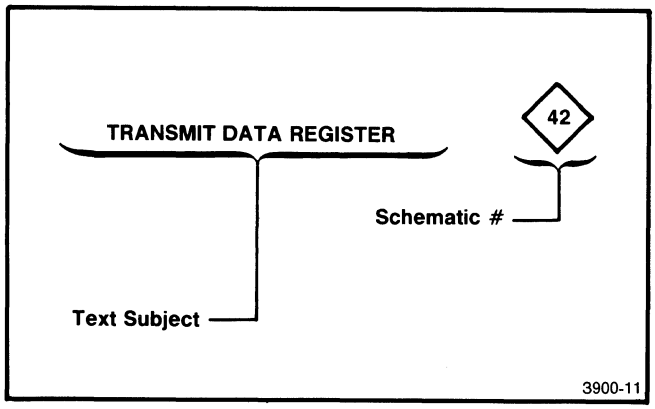
The schematic drawings in this manual use a high/low convention to describe the asserted state of all signal lines. The asserted (true) state of each signal line is shown as (L) for

low or (H) for high, immediately following the signal line name, as follows:

- SLVOPREQ(L)
- CMEM(H)
- M(L)/IO(H)

Schematics

Schematics in this manual have been drawn with grey overlays to highlight functional blocks of circuitry. The text is coordinated with these block overlays. Text headings indicate the schematics that depict the circuit under discussion. The following example illustrates a text heading:



The example shows that:

- The subject of the text is the Transmit Data Register.
- The register appears on schematic 42.

CHANGE INFORMATION

Change notices are issued by Tektronix, Inc., to document changes to the manual after it has been published. Change information is located at the back of this manual, following the yellow tab marked, "CHANGE INFORMATION". When you receive the manual, you should enter any change information into the body of the manual, according to instructions on the change notice.

Revision History

As this manual is revised and reprinted, revision history information is included on the text and diagram pages. Revised pages of manuals are indicated by REV and the date (REV OCT l984) at the bottom inside corner of the page. New pages added to an existing section, whether they contain old, new or revised information, contain the word "ADD" and the revision date (ADD OCT 1984).

DOCUMENTATION OVERVIEW

Support documentation for TEKTRONIX microcomputer development systems consists of service manuals, installation manuals, and users manuals.

Service Manuals

Service manuals provide the information necessary to perform system testing, to isolate hardware problems, and to repair system components. Service manuals may be purchased from Tektronix, Inc. as optional accessories. The following manuals provide service information for the 8560 Series Multi-User Software Development Units:

- 8560/8561/8562 Multi-User Software Development Unit Service Manual
- QumeTrak 242 Maintenance Manual
- Micropolis 1300 Series Rigid Disk Drive Maintenance Manual
- Seagate ST406/412/419 Microwinchester Service Manual

Installation Manuals

Installation manuals explain how to unpack and install the equipment and how to verify that it operates properly. Installation manuals are provided as standard accessories.

Users Manuals

Users manuals describe how to operate the development system and its peripheral devices. They are provided as standard accessories in the system package.

The following manuals provide an overview of your development system, including information about system software and the TNIX operating system.

- 8560 Series Multi-User Software Development Unit System Users Manual TNIX Version 2.1
- 8560 Series Multi-User Software Development Unit System Reference Manual
- 8560 Series Multi-User Software Development Unit Instruction Sheet

Options

8560 Series MUSDU options are documented by individual manuals. See the Tektronix Products Catalog or contact your local Tektronix field office or representative for a list of available options.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as you read the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS

As Marked on Equipment


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION - Refer to manual.

SAFETY PRECAUTIONS

Grounding the Product

This product is grounded through the grounding conductor in the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the equipment's power input terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Use the Proper Power Cord

- Use only the power cord and connector specified for your product.
- Use only a power cord that is in good condition.
- Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product. Be sure the fuse is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

(Refer also to the preceding Operators Safety Summary)

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

The product is designed to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

856x Multi-User Software Development Unit

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Section 1

GENERAL INFORMATION

INTRODUCTION

This section provides general information about the 8560 Series MUSDU, introducing individual hardware system building blocks, separately and in relation to each other. It also provides a general overview of the system's operating software and the diagnostic firmware/software.

The 8560 MUSDU is a 16-bit bus-oriented computer with mass storage. The 8560 MUSDU's main purpose is to serve as a program development tool and system file management system for 8540 Integration Units. (The 8540 Integration Unit is described in a separate service manual.)

Data storage is provided on two disk drives. Winchester-technology hard disk drive units store up to 80M bytes of data. A second disk drive unit provides 1M bytes of storage on double-sided, double-density flexible disks. The 8560 MUSDU consists of the following major components:

- System hardware
- Mechanical package
- Operating firmware
- Diagnostic firmware
- Diagnostic software
- Operating software

8560 system software, the TNIX operating system and its components are described in a separate 8560 Users Manual.

SYSTEM HARDWARE

The 8560 MUSDU is a single-enclosure mainframe. It contains power supplies, disk drives, and all control circuits in a bus-oriented system architecture.

The 8560 main controller is a Digital Equipment Corporation LSI-11 processor. Additional processor-controlled boards (IOP Board(s) and the MSC Controller) work in conjunction with the LSI-11. Figure 1-1 shows a simplified 8560 block diagram.

The 8560 MUSDU employs the back-plane concept, in which major system boards plug into a horizontally located Main Interconnect Board. It provides the vehicle for the 100-line-wide 8560 bus. The Main Interconnect Board provides direct system bus access for the following boards:

- The LSI-11 Processor
- The MSC Controller
- System memory boards
- I/O Processor Boards
- The Utility Board

The 8560 Bus

The 8560 bus is the main system bus. The 100-line-wide bus is based on the DEC Qbus but with increased flexibility. The DEC interrupt structure is retained, as is most of the DEC signal protocol. Each 8560 circuit board interfaces directly with the 8560 bus. The 8560 bus provides 22 data lines. For additional 8560 bus information, refer to Section 19 of this manual.

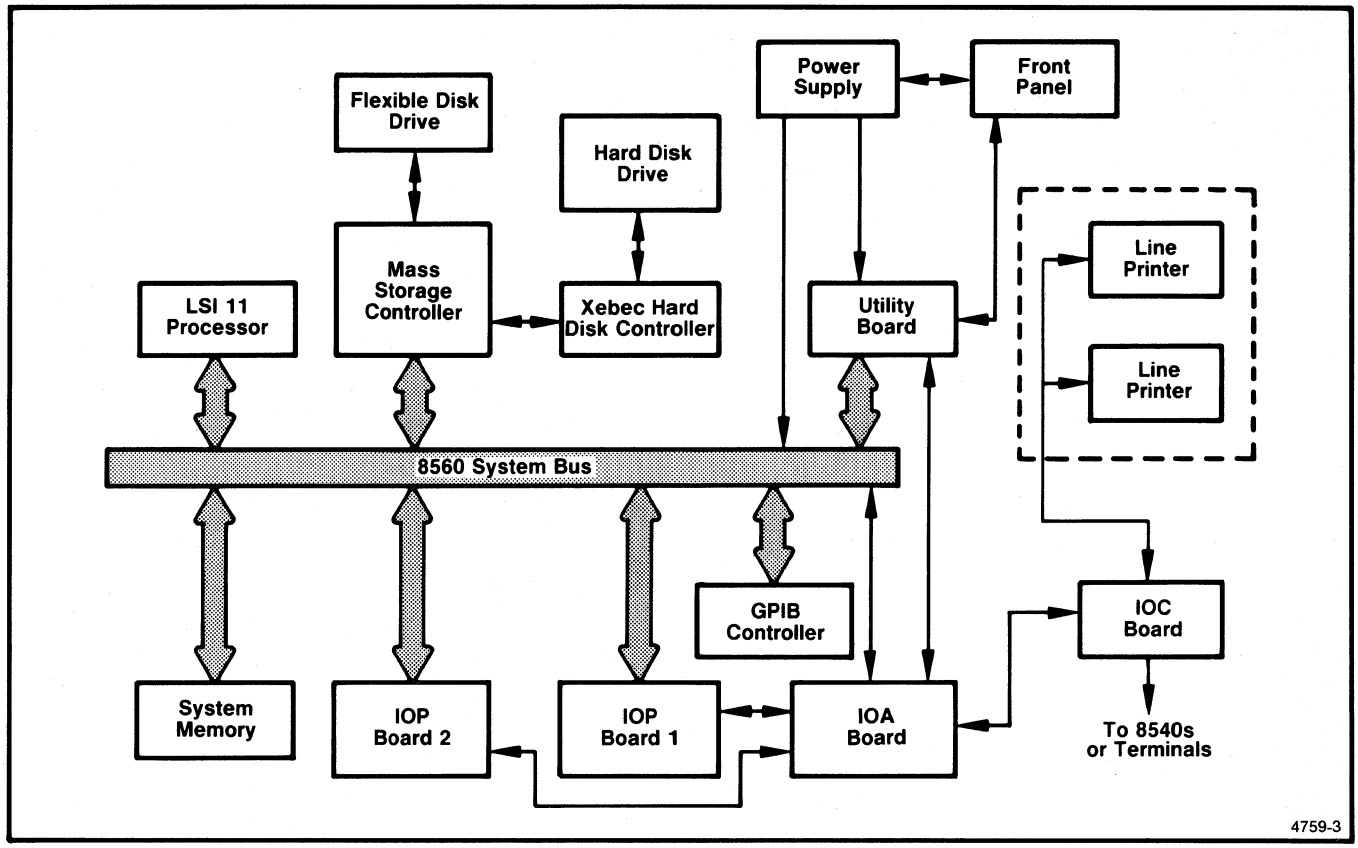

Fig. 1-1. The 8560 system block diagram.

The Main Interconnect Board

The Main Interconnect Board is a horizontally mounted circuit board located near the cabinet bottom, adjacent to the drive units. It provides a vehicle for the 100-line-wide 8560 system bus. Seventy-two of those lines serve the LSI-11. The remaining 28 lines provide specific functions for the system boards shown in Fig. 1-2.

The Main Interconnect Board contains one 72-pin connector and eight 100-pin connectors. The 72-pin connector services the LSI-11. All other 8560 system boards, except the power supply and two I/O Boards, plug into the Main Interconnect Board's 100-pin connectors. Because of the 8560 bus structure, each circuit board is assigned a specific connector. Figure 1-2 shows the system bus and a typical system configuration.

The Main Interconnect Board also contains seven bus grant jumpers that pass the system bus grant to the next installed board when a connector is empty. Section 19 of this manual provides connector wiring charts, and Section 3 identifies the bus grant jumpers.

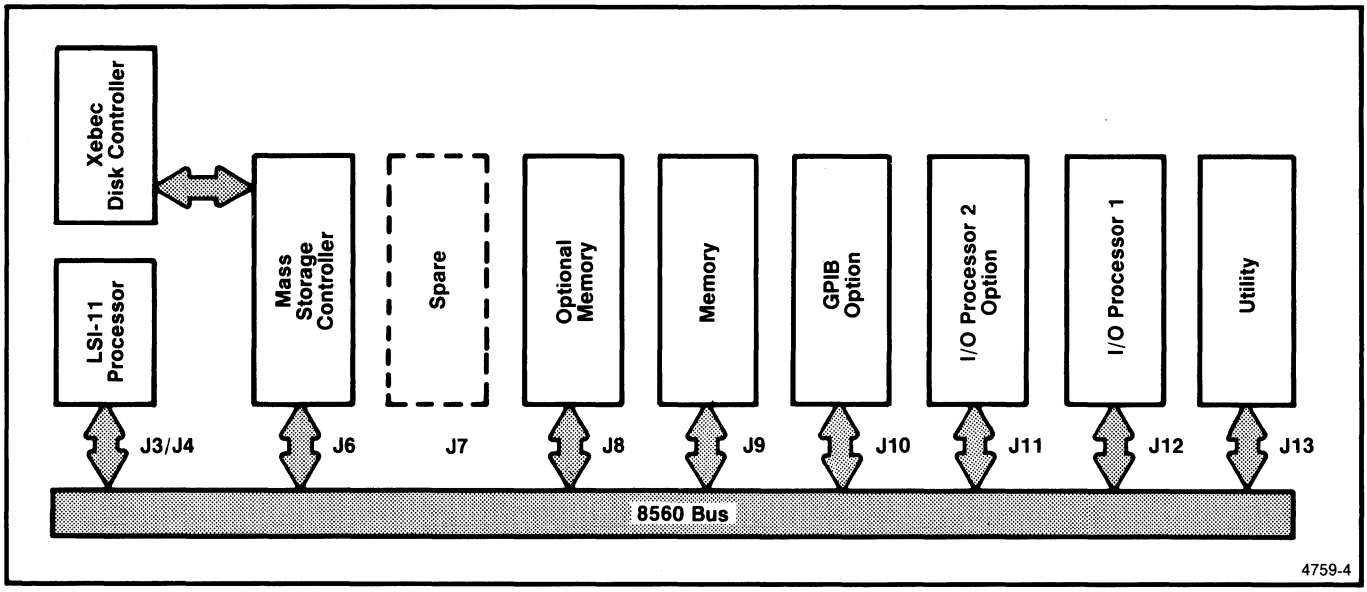

Fig. 1-2. A typical 8560 configuration.

The LSI-11/23 Processor

The Digital Equipment Corporation LSI-11/23 is a 16-bit microcomputer which contains the LSI-11/23 chip set, consisting of a data control unit, a memory management unit, and an optional floating point arithmetic unit.

The LSI-11/73 Processor

The Digital Equipment Corporation LSI-11/73 is a 16-bit microcomputer which contains the LSI-11/73 chip set, consisting of of a data control unit, a memory management unit, and a floating point arithmetic unit.

The Utility Board

The Utility Board contains miscellaneous logic that provides the following features:

- Two RS-232-C interfaces
- A Line-Time Clock control circuit (LTC)
- System bootstrap firmware
- RAM Board service routine firmware
- Power-up diagnostic firmware

The Utility Board plugs into connector J13 on the Main Interconnect Board.

The System Memory Board

The 8560 Series system memory consists of up to 1M bytes of RAM on a total of two circuit boards which plug into connnectors J8 and J9 on the Main Interconnect Board.

The I/O Processor (IOP) Board

The I/O Processor (IOP) Board is a communications board controlled by an 8088 microprocessor. The IOP controls data flow to and from external 8560 peripherals. The IOP relieves the LSI-11 of most I/O processing chores associated with external 8560 peripheral communications.

IOP Boards plug into connectors J11 and J12 of the Main Interconnect Board and process data for up to eight High Speed Interface (HSI) channels.

The I/O Adapter (IOA) Board

The I/O Adapter (IOA) Board is a small circuit board mounted to the side rail toward the rear of the 8560 cabinet. The IOA Board services up to eight HSI ports and two RS-232-C compatible printer ports.

HSI Ports 0 through 7 operate under either High Speed Interface protocol (electrically compatible with RS-422) or RS-232-C protocol. HSI Port 0 is factory-jumpered for RS-232-C protocol for use with a system terminal. Printer Ports LP1 and LP2 operate only under RS-232-C protocol.

The I/O Connector (IOC) Board

The I/O Connector (IOC) Board is a small circuit board without active devices that contains up to ten 25-pin D-type connectors. The board is mounted on the rear panel with the connectors protruding through the rear panel. These connectors are accessible from outside the cabinet and serve Printer Ports LP1 and LP2, and HSI Ports 0 through 7. The standard 8561 contains connectors for HSI Ports 0 and 1. The standard 8560 contains connectors for HSI Ports 0 through 3. The 8562 standard configuration includes HSI Ports 0 through 7. HSI Ports 4 through 7 require the addition of a second IOP Board and four additional HSI connectors on the IOA Board.

The Mass Storage Controller (MSC) Board

The MSC Board provides control and interface functions for the flexible disk and control functions for the hard disk drive. The MSC Board is 80186-based and can assume 8560 bus mastership whenever required. It controls all interfacing between the flexible hard disk drives and the 8560 system. The MSC Board plugs into connector J6 on the Main Interconnect Board.

The Xebec S1410 Disk Controller

The Xebec S1410 Disk Controller provides interfacing logic for the Winchester-type hard disk drive(s). It provides interlocked data transfer through the Shugart Associates System Interface (SASI).

The Power Supply

The 8560 power supply is located in an enclosed assembly occupying the left rear corner of the 8560 MUSDU cabinet. It provides four DC voltages.

The Flexible Disk Drive

The 8560 flexible disk drive is a QumeTrak 242. The flexible disk drive stores data on standard, removable double-sided, single-density disks (0.5M bytes of storage), or on double-sided, double-density disks (1M bytes of storage).

The Winchester-Technology Hard Disk Drive

The 8560 Series hard disk drives are Winchester-technology type drive units. The disks are in a sealed chamber in the drive unit. To service the disks, the entire drive unit must be completely removed and returned to your Tektronix service center. For more service information and instructions for removing the hard disk drive, refer to Section 15 of this manual.

The Front Control Panel

The front control panel contains the Front Panel Board, the DC ON, RUN/HALT, and RESTART switches, and three LED status indicators.

The Front Panel Board is located to the right of the two disk drives, directly behind the front panel. The RESTART, DC, and RUN/HALT switches are mounted on the Front Panel Board and extend through the front control panel. The DC ON power switch, however, is mounted directly on the front control panel.

The Rear Panel

The 8560 rear panel contains up to eight HSI ports, two auxiliary RS-232-C compatible ports, a primary power switch, a line fuse, a primary line-voltage indicator, a power-supply fan assembly, and an optional Mass Storage Interface Bus Port. Attached to the rear of the 8560 is a fan enclosure. The fan provides cooling for the disk drives, power supply assembly and circuit boards.

OPERATING FIRMWARE

The 8560 operating firmware provides instructions for the microprocessor-controlled system boards. Operating firmware is located in the Utility Board, the MSC Board, the I/O Processor Board and Xebec S1410 Disk Controller Board. 8560 operating firmware falls into two categories:

- System boot-up firmware
- Firmware containing instructions for the Mass Storage Controller and the I/O Processor

Boot-up Firmware

The boot-up firmware initializes the system and turns control over to the power-up diagnostics. The 8560 boot-up firmware, located on the Utility Board, is the initial firmware executed when the 8560 is turned on or restarted. The boot-up firmware is located on the Utility Board. Once the power-up diagnostics have checked system operation, control returns to the boot-up firmware, moving the 8560 operating system from disk into memory. At that point, system control is turned over to the operating system. The boot-up and power-up diagnostics are executed by the LSI-11 processor.

Controller Firmware

The MSC and I/O Processor (IOP) are both microprocessor-based boards, with controlling firmware contained in PROMS.

DIAGNOSTIC FIRMWARE

The 8560 diagnostic firmware informs you of overall system conditions and provides you with specific system status information. It also provides power-up tests for the user and service routines for the service technician.

The 8560 diagnostic firmware consists of power-up diagnostic tests, including disk drive service routines for the system memory boards.

The power-up tests and the system memory board firmware are located on the Utility Board. They share ROM with the boot-up routines. Power-up tests are described in Section 13 of this manual.

The Octal Debugging Technique (ODT) package is also part of the diagnostic firmware. ODT is located in unchangeable microcode and is part of the LSI-11 chip set. Section 13 describes ODT usage. The ODT firmware allows you to look at memory and I/O port locations and check the status of the LSI-11.

Power-up Diagnostics Firmware

The 8560 power-up diagnostics perform a general system check, verifying that all standard circuit boards are installed and are in working condition. If a failure occurs, the power-up diagnostics display a message on the system terminal. Power-up diagnostics are further described in Section 13 of this manual.

DIAGNOSTIC SOFTWARE

The 8560 also offers you disk-based diagnostics providing individual board test programs that you can invoke from a terminal. These programs locate problem areas to the block diagram level. The disk-based diagnostics are stored on a separate flexible disk. Section 16 provides detailed descriptions of the tests and their functions.

OPERATING SOFTWARE

The 8560 TNIX[1] operating system is an enhanced version of the popular UNIX[2] operating system. The TNIX operating system is stored on a Winchester-technology hard disk and is described in the **8560 Series System Users Manual**.

[1] TNIX is a registered trademark of Tektronix, Inc.

[2] UNIX is a registered trademark of Bell Laboratories.

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SPECIFICATIONS

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Section 2

SPECIFICATIONS

INTRODUCTION

This section contains the 8560 system specifications. Table 2-1 lists the electrical specifications, Table 2-2 lists the environmental specifications, and Table 2-3 lists the physical specifications. Power supply internal specifications are given with the supply description in Section 12.

Table 2-1
Electrical Characteristics

Characteristic	Performance Requirement	Supplemental Information
Primary Power		
Input Voltages	90 to 132 Vac 180 to 250 Vac	
Frequency	48 to 66 Hz	
Line Fuses		
115 Vac		3AG, 8 Amps, 250 Volt, fast-blow
230 Vac		3AG, 4 Amps, 250 Volt, fast-blow
Power Consumption (maximum)		410 Watts
Power Supply	+5.0 Vdc +/-3% +12.0 Vdc +/-5% -12.0 Vdc +/-5% +15.0 Vdc +/-10% +24.0 Vdc +/-10%	33A 6.5A 260mA 20mA l.0A
Static Discharge		
Operating		12.5 kV and below with no effect on operation of unit

Table 2-2
Environmental Characteristics

Characteristic	Description
Temperature	
Operating	+10°C to +35°C (+50°F to +95°F)
Storage	-10°C to +45°C (+14°F to 113°F)
Humidity	
Operating	20% to 80% noncondensing 26°C (79°F) maximum wet bulb
Altitude	
Operating	To 2 500 m (8,000 feet)
Storage	To 9 140 m (30,000 feet)

Table 2-3
Physical Characteristics

Characteristic	Description
Net Weight	22.4 kg (49.2 lb.)
Overall Dimensions	
Height	267 mm (10.5 in.)
Width	432 mm (17 in.)
Length	646 mm (25.4 in.)

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Section 3

OPERATING INFORMATION

INTRODUCTION

This section briefly describes all 8560 controls, connectors, and indicators. It also describes all circuit board straps and jumpers and shows how the 8560 communicates with other peripherals.

Detailed 8560 operating information can be found in the *8560 System Users Manual.* Refer to that manual for explanations about software.

CONTROLS, CONNECTORS, AND INDICATORS

The following paragraphs discuss the 8560 controls, connectors, and indicators. The pin configurations for all rear panel connectors are also included. Figure 3-1 shows the 8560 front panel layout, and Fig. 3-2 shows the 8560 rear panel.

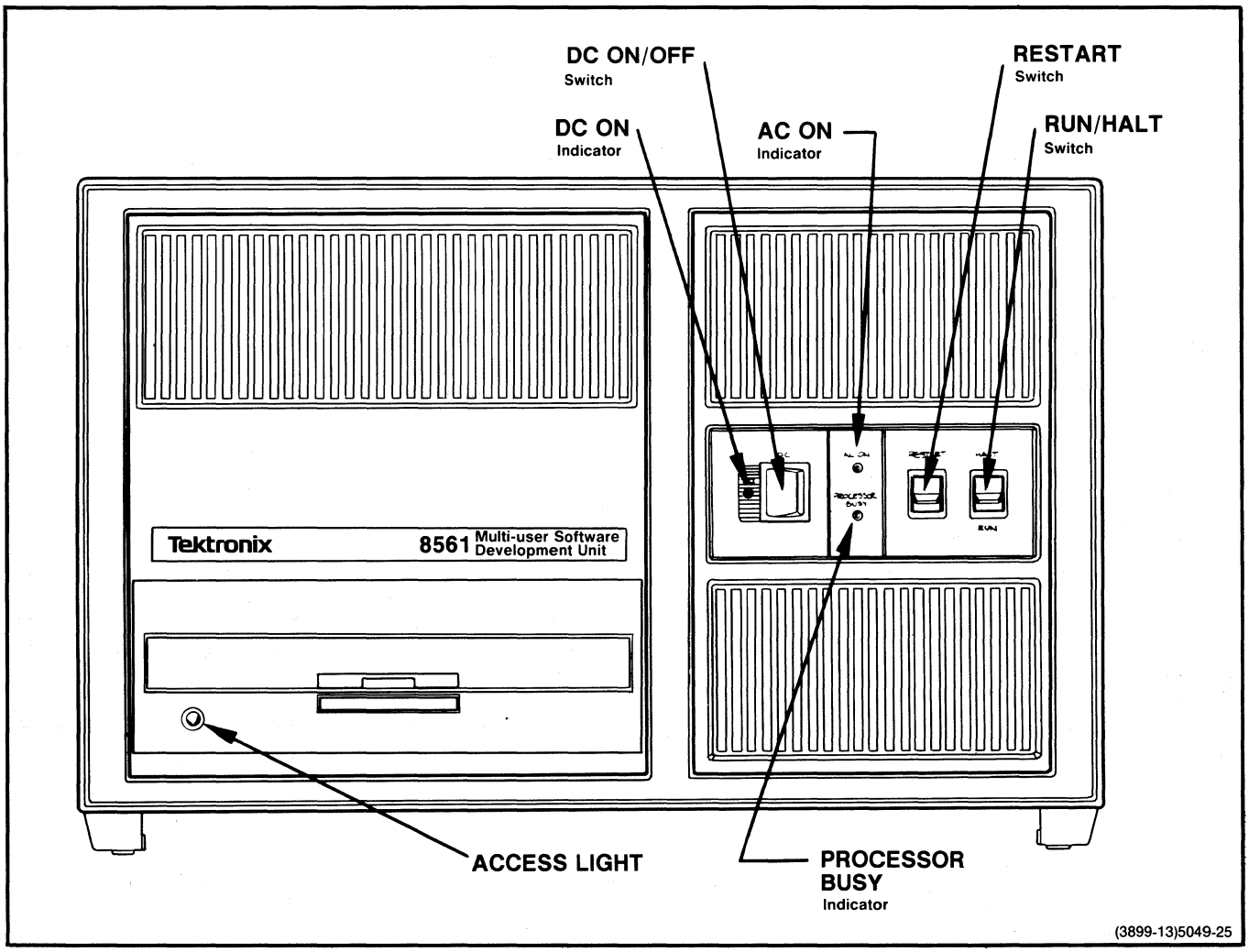


Fig. 3-1. The 8560 front panel controls and connectors.

Front Panel Switches

The 8560 front panel has three switches: DC ON/OFF, RESTART, and RUN/HALT. They are described as follows:

DC ON/OFF

The DC ON/OFF switch supplies DC voltage to the system. When this switch is in the OFF position, the system is in the standby mode. In this mode, the DC voltages are available on the power supply, but are not supplied to the individual circuits.

RESTART

Toggling this momentary-contact switch resets the entire system to its initial state and executes the power-up tests.

RUN/HALT

Toggling the RUN/HALT switch halts the processor, regardless of what task it is performing at the time.

Front Panel Indicators

The front panel has three indicator lights: DC ON, PROCESSOR BUSY, and AC ON.

DC ON

The DC ON indicator is lit when the DC ON/OFF switch is in the ON position and DC power is applied to the system.

AC ON

The AC ON indicator is lit whenever the rear panel POWER ON/OFF switch is in the ON position.

PROCESSOR BUSY

The PROCESSOR BUSY indicator is lit when the LSI-11 is performing a task.

Rear Panel Controls

The following paragraphs describe the 8560 rear panel controls.

POWER ON/OFF

The POWER ON/OFF switch is the main system power switch, providing line voltage to the power supply. When this switch is on, the front panel AC ON indicator is lit. Figure 3-2 shows the 8560 rear panel layout.

LINE FUSE

This is the line fuse for the 8560. If the system is configured for 115 Vac, use a 3AG, 8 Amp, 250 Volt, fast-blow fuse. If the 8560 is configured for 230 Vac, use a 3AG, 4 Amp, 250 Volt, fast-blow fuse.

PRIMARY POWER PLUG

This is the primary power supply plug for the 8560. Only the line voltage indicated by the source voltage cover plate should be connected.

PRIMARY VOLTAGE SOURCE

The primary voltage source for an 8560 is selected at the factory. A cover plate on the rear panel of the instrument indicates two possible voltage source selections. To change the voltage source, remove this cover plate, change the two-position switch to the new setting, and replace the cover plate.

If you change the voltage source, be certain that your 8560 has the proper fuse for the new configuration.

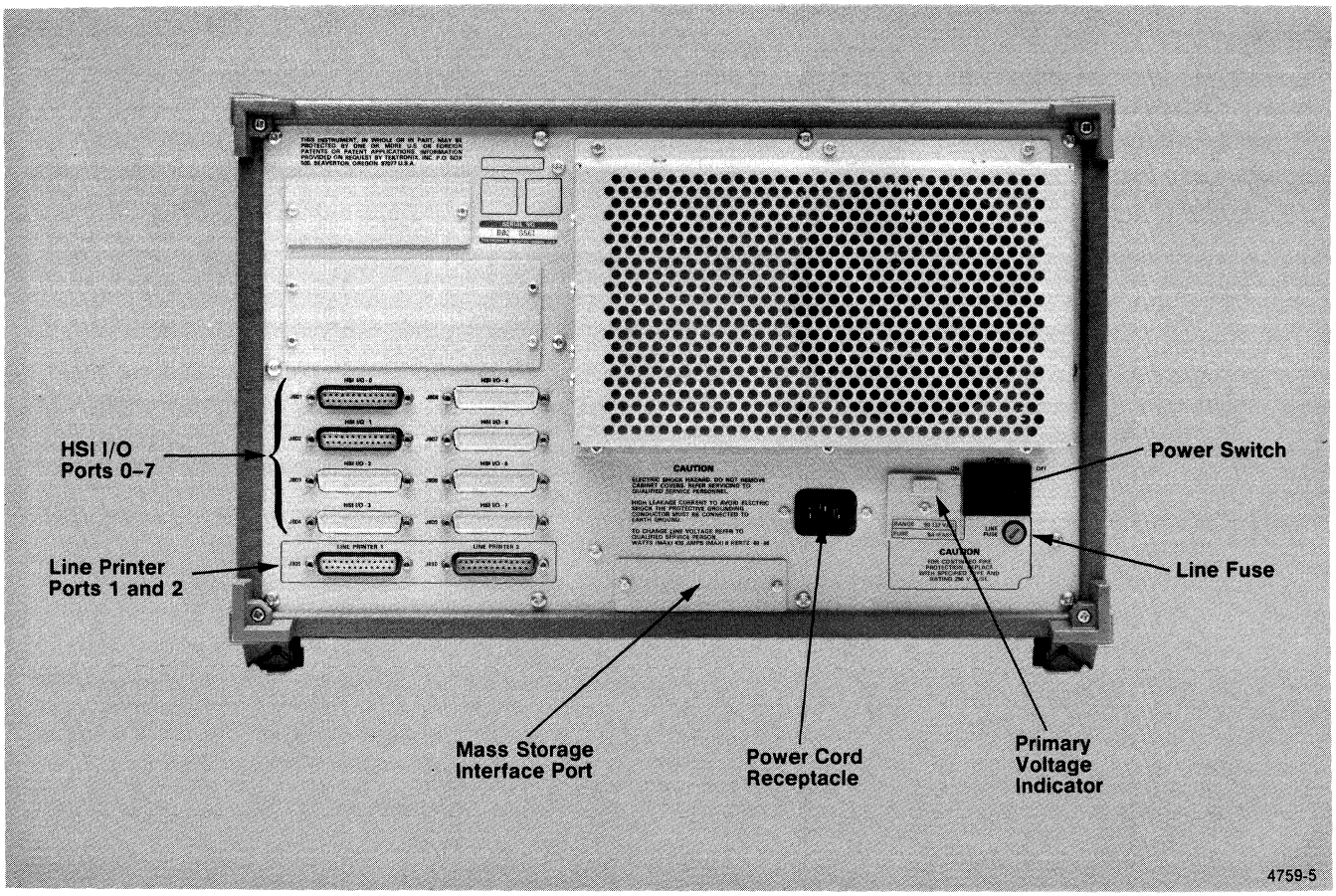


Fig. 3-2. The 8560 rear panel control and connectors.

Rear Panel Connectors

The following paragraphs describe the 8560 rear panel connectors.

HSI Ports O through 7

J801 through J804 and J806 through J809 are the HSI ports. HSI Port 0 is factory-jumpered for RS-232-C protocol for use with a system terminal. HSI Ports 1 through 7 are factory-jumpered for RS-422 protocol to communicate with a workstation such as the TEKTRONIX 8540 Integration Unit.

The HSI ports transmit and receive at 153.6K baud. Any HSI port, however, may be reconfigured to operate under RS-232-C protocol by moving the appropriate jumper block on the IOA Board. You can then connect a terminal directly to the 8560. Instructions to configure an HSI port and an RS-232-C port are provided in Section 8 of this manual. Table 3-1 shows HSI port pin assignments.

Table 3-1
HSI Port Configurations

Pin	Name	Function
1		Shield
7	GRD	Signal Ground
2	R DATA	Receive Data
11	R DATA'	Receive Data
3	T DATA	Transmit Data
12	T DATA'	Transmit Data
20	DTR	Data Terminal Ready
13	DTR'	Data Terminal Ready
5	CTS	Clear To Send
25	CTS'	Clear To Send
6	DSR	Data Set Ready
18	DSR'	Data Set Ready
8	CAR DET	Carrier Detect
9	CAR DET'	Carrier Detect

Printer Ports LP1 and LP2

Ports J8051 and J8101 provide communications with auxiliary equipment, such as line printers and terminals. These ports are RS-232-C compatible and have selectable baud rates. Table 3-2 shows the pin configurations for the printer ports.

Table 3-2
Line Printer Port Configuration

Pin	Name	Function
1		Shield
7	GRD	Ground
2	R DATA	Receive Data
3	T DATA	Transmitted Data
20	DTR	Data Terminal Ready
5	CTS	Clear to Send
6	DSR	Data Set Ready
8	CAR DET	Carrier Detect
15	T CLK	Internal Clock (These two pins are tied together internally to R CLK)
17	R CLK	External Clock (These two pins are tied together internally to R CLK)
4	RTS	Request to Send

COMMUNICATIONS

The following paragraphs describe how to connect various peripherals to the 8560. In its standard configuration, the 8560 Series MUSDU supports up to eight HSI ports and two printer ports.

Each I/O Processor (IOP) Board controls up to four HSI ports. Refer to Section 7 of this manual for a detailed description of the I/O Processor Board. Refer to Section 8 for information on the I/O Adapter Board and I/O Connector Board.

HSI Ports 1 through 7 typically operate under modified RS-422 protocol and communicate with the Tektronix 8540 Integration Unit. You can, however, reconfigure the I/O ports for use as terminal ports, operating under RS-232-C protocol.

Refer to Fig. 3-3 for I/O port connections to the I/O processor.

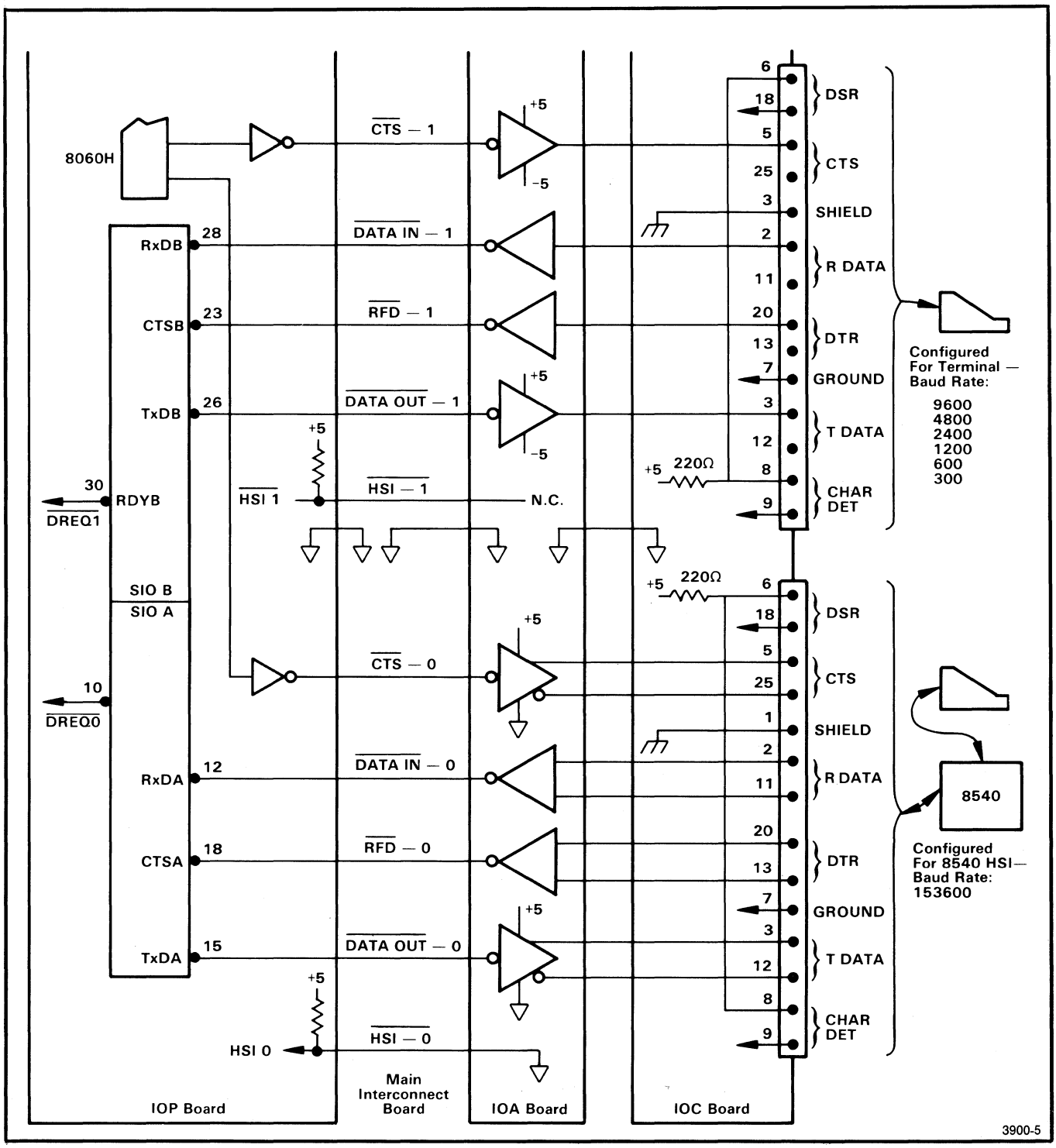


Fig. 3-3. I/O port connections to the I/O processor.

Interfacing to an 8540

The 8560 and the 8540 communicate through interconnecting cables. Figure 3-4 identifies the interconnecting signal lines for an HSI interface between the 8560 and the 8540. For additional interfacing information, refer to the *8560 Series Installation Guide*. Baud rate selection is also described later in this section.

Interfacing to a Terminal via an HSI Port

If a terminal is connected directly to an 8560 HSI port, the appropriate IOA Board jumper block must be repositioned to provide the RS-232-C interface protocol. Figure 3-5 shows the interconnecting signal lines between a typical system terminal and the 8560.

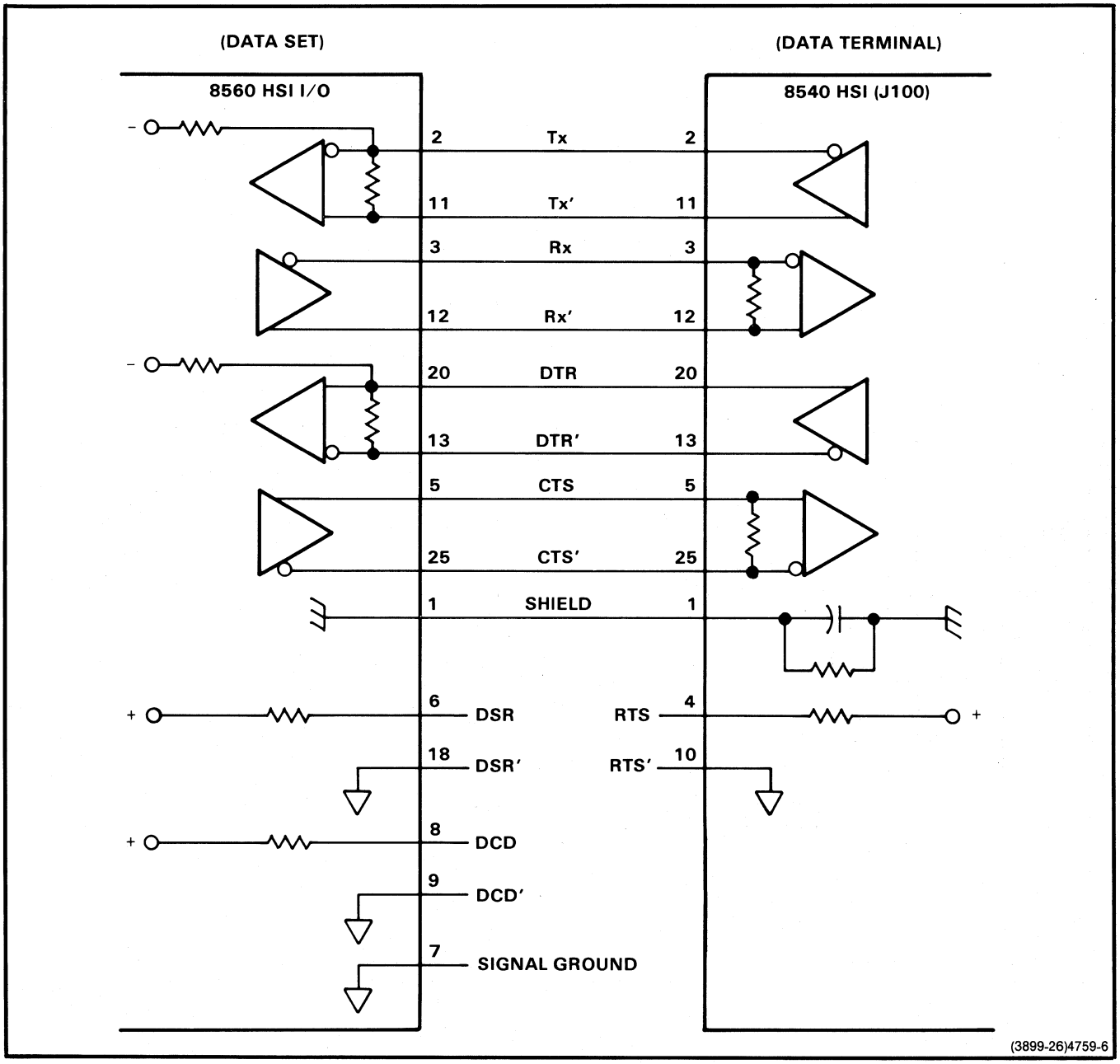


Fig. 3-4. High-Speed Interface (HSI) lines.

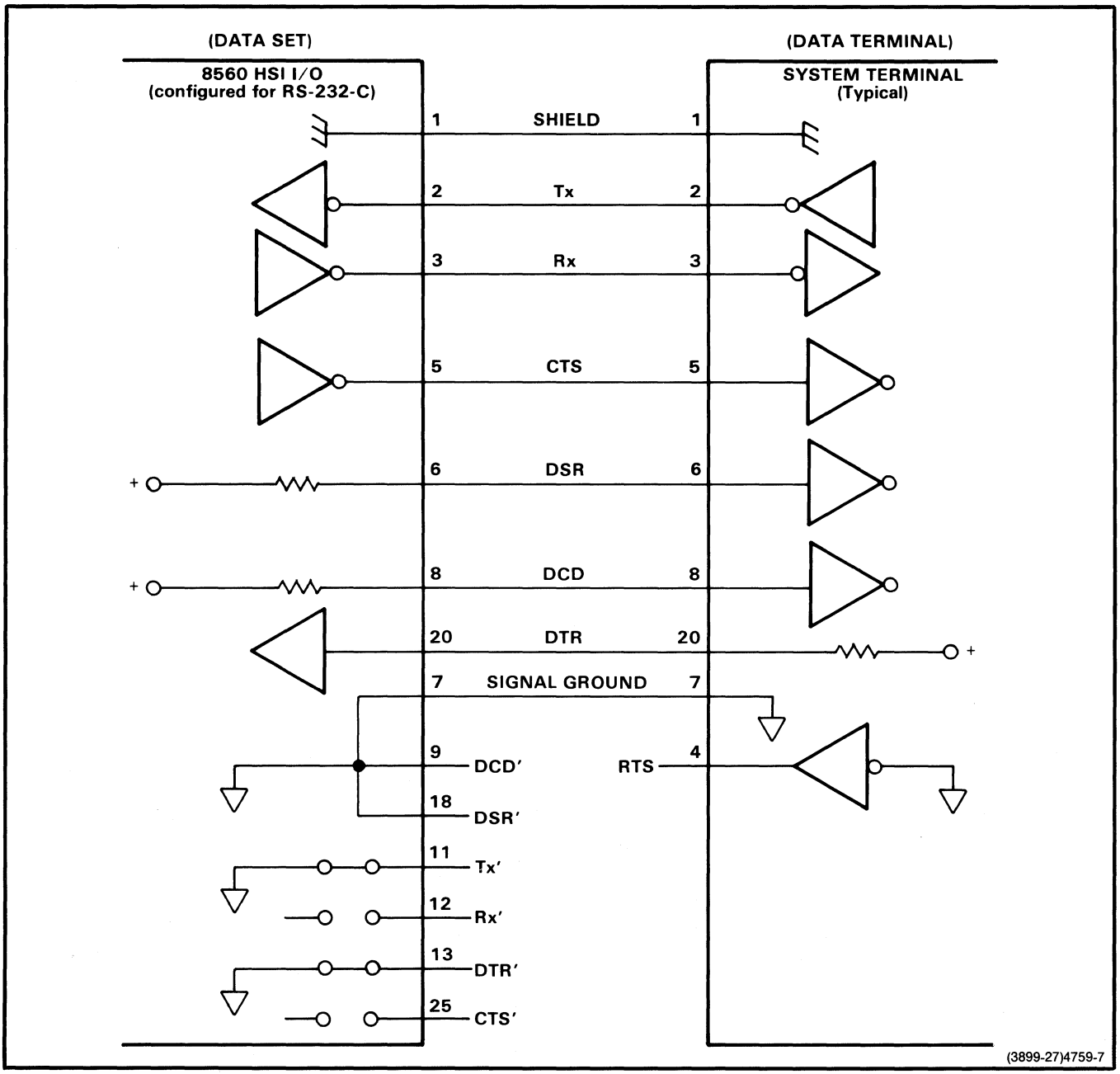


Fig. 3-5. A typical RS-232-C system terminal interface.

Interfacing to a Line Printer

Line printers may be connected directly to the 8560 line printer connectors J805 or J810. Figure 3-6 shows the interconnecting signal lines between an 8560 and a typical line printer.

8540 Remote Interfacing

The 8560 can also communicate with an 8540 via the 8540 remote port J101 (an RS-232-C compatible interface with a maximum baud rate of 9600 baud.) Interconnecting signal lines for this interface configuration are shown in Fig. 3-7.

Communications over this interface are established and maintained by the COMM commands as described in the *8540 Integration Unit System Users Manual.*

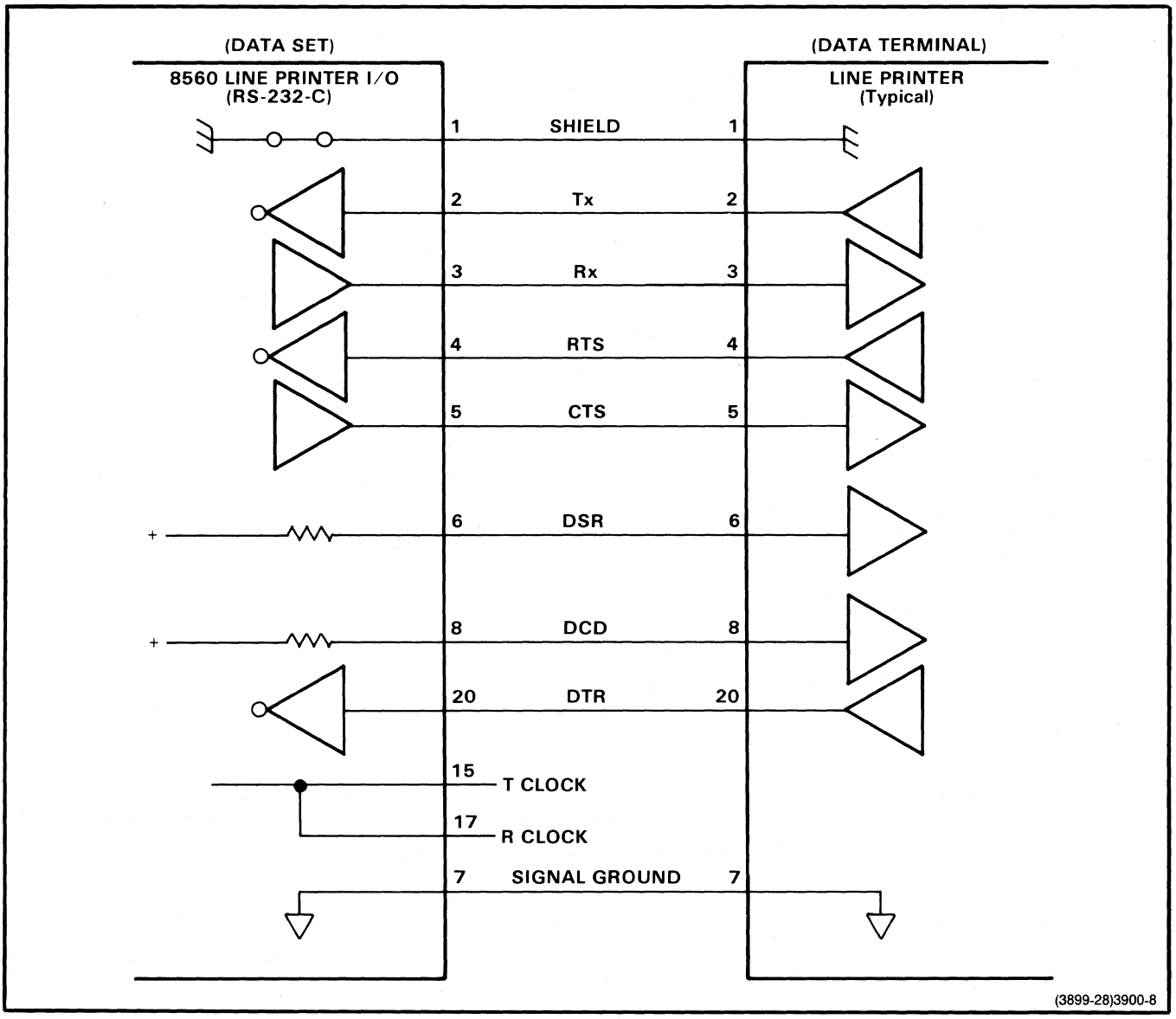


Fig. 3-6. A typical line printer interface with the 8560.

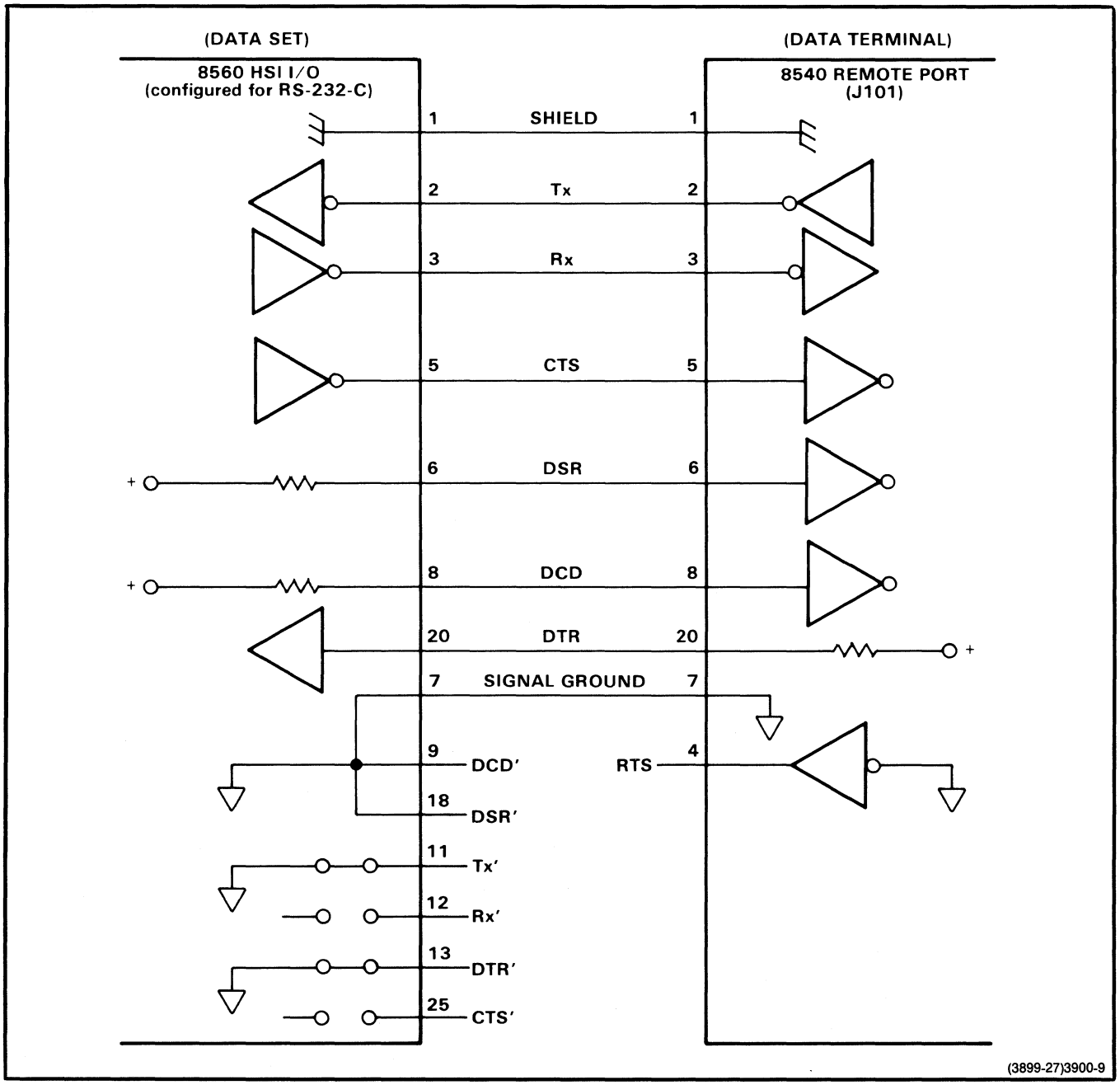


Fig. 3-7. RS-232-C interface lines between the 8560 and the 8540.

Port Characteristics

Introduction

This section summarizes the RS-232-C and RS-422 protocols used with the 8560. The 8560 provides up to 10 ports to communicate with external peripherals. Eight ports are defined as HSI ports and the remaining two are printer ports.

I/O Processor boards serve up to eight ports. Typically, these ports are defined as High Speed Interface (HSI) ports because they transmit and receive at a rate of 153.6K baud, with the exception of HSI Port 0, which is factory-jumpered for RS-232-C protocol for use with a system terminal. You can, however, configure any HSI port to operate under the RS-232-C protocol and set its baud rate to any value permitted by this protocol. HSI ports are accessible at the rear panel.

Two additional ports are defined as Printer Ports LP1 and LP2. These ports always operate under RS-232-C protocol. Their baud rates, however, are variable and can be set to any speed allowed under the RS-232-C protocol. Printer ports are usually dedicated for line printer or terminal operations.

Note that a printer port vector-interrupt can be selected from the Utility Board. (See "Circuit Board Configurations," later in this section.) Printer Port LP 1 uses a default address of 17777510 and an interrupt vector address of 200. Printer Port LP2 uses default address 17777560 and an interrupt vector address of 60. Both printer ports are identical in their wiring and communication methods.

RS-232-C Protocol

In RS-232-C protocol, data is sent from the 8560 on the TDATA line and received by the peripheral on the RDATA line. All data byte communications are preceded by one start bit and terminated by one or more stop bits. The firmware checks if the start/stop bits are present. If they are not, a framing error is generated. Parity is also checked by the 8560 unless the Utility Board is strapped for the NO PARITY option. See "Circuit Board Configurations," later in this section, for Utility Board strapping/jumpering options.

The Clear-to-Send (CTS) signal is asserted by the 8560 when the 8560 is free to receive data. The Request-to-Send (RTS) signal is asserted when the peripheral wants to receive data, placing the 8560 in transmit mode. The Data-Terminal-Ready (DTR) signal is activated by the peripheral when it is ready to transmit or receive data. All signals, including data signals, are active low.

The Transmit/Receive (T/R) Clock line is an optional facility for setting communication rates by means of an external clock. This must be an even baud rate, including stop bits and is determined by dividing the bit rate frequency by 16.

The 8560 conforms to the Electronic Industries Association (EIA) standard. For time durations of all signals mentioned, refer to the relevant EIA documents.

HSI/RS-422 Protocol

The RS-422 communication standard is similar to RS-232-C in terms of signals but differs in the method of transmission. All four principal communication lines (RDATA, TDATA, RTS and CTS) use two lines to communicate instead of one. For example, TDATA uses pins 3 and 12 instead of just pin 3 as is used in RS-232-C protocol. In the case of RS-422, each pair is a set of balanced lines.

Baud Rate Selection

The following paragraphs describe baud rate selection for the 8560 line printer ports and HSI ports.

Printer Ports LP1 and LP2

Printer Ports LP1 and LP2 are factory-jumpered to transmit and receive at 2400 baud. You can change this baud rate by moving the appropriate jumper on the Utility Board. Table 3-8, later in this section, identifies these jumpers and provides information for selecting other available baud rates.

HSI Ports

When an HSI port is configured for RS-422 protocol, the baud rate is fixed at 153.6K baud. When an HSI port is configured (with jumpers on the IOA Board) as a RS-232-C port, the baud rate defaults on power-up to 2400 baud. Firmware on the IOP Board permits selection from the terminal for the baud rate that matches the attached terminal by depressing the BREAK key. An intelligible message appears on the terminal screen when you have obtained the correct baud rate.

JUMPERS AND STRAPS

The 8560 provides circuit board jumpers and straps that change a board's operating configuration. Most 8560 circuit boards contain straps that are used to tailor the board for a specific function or are used for troubleshooting. Configuration tables are provided in this section for the default strapping and jumpering of all boards. A strap or jumper is either in, out or connected to a specific position.

Jumpers

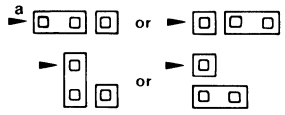
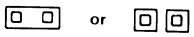
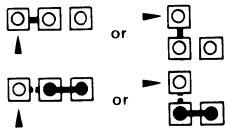
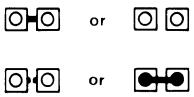
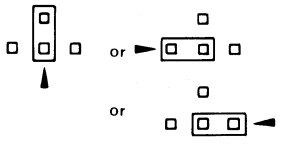
In this manual, the term "jumper" refers to a small connector designed to fit across a jumper position, consisting of two square pins that can accommodate the placement of the jumper. Jumper positions are arranged on the circuit boards as one-position or two-position jumpers. One-position jumpers have only two square pins, and the jumper is either installed or removed. Two-position jumpers have three square pins arranged in a straight line or in an "L" pattern. The jumpers may be installed on pins 1 and 2, or 2 and 3, or removed. Table 3-3 shows the symbols used for jumpers on the circuit board configuration drawings that appear later in this section. Jumper numbers are designated with a "Pxxxx" or a "Jxxxx", unless otherwise noted.

Jumpers are also used in clusters, in which case all jumpers in the cluster are changed at once with a jumper block. A jumper block consists of two or more jumpers in one physical unit. These blocks are usually used where a number of jumpers change the same function on different signal lines.

Straps

In this manual, the term "strap" refers to an ECB through-hole that may be bridged with a soldered wire to select an alternate function. A strap may also be a cuttable run, which is an ECB run between two through-holes. The run must be cut before one of the through-holes can be strapped to a third through-hole. If there is a cuttable run at the location, it must be cut before the strap is bridged to prevent system errors. Table 3-3 shows the symbols used for straps on the circuit board configuration drawings that appear later in this section. Straps are designated with a "Wxxxx."

Table 3-3
Symbols for Jumpers and Straps

Jumper/Strap Symbols	Usage
	These two-position jumpers show the jumper across pins 1 and 2 or across pins 2 and 3.
	This single-position jumper shows the jumper across the single jumper position or the jumper removed.
	These two-position straps show the cuttable runs between pins 1 and 2. The runs may be cut and the straps bridged across pins 2 and 3.
	These single-position straps show the through-holes with or without a cuttable run. The cuttable run may be cut or the through-holes may be bridged with a strap.
	The 3-position jumpers show the jumper across pins 1 and 3, or across pins 2 and 3 or across pins 3 and 4

[a] **Arrow = pin 1**

CIRCUIT BOARD CONFIGURATIONS

This section describes the default configurations of jumpers and straps for all 8560 system circuit boards.

Main Interconnect Board Configuration

The Main Interconnect Board provides seven pairs of bus grant jumpers (J19 through J32). Each board that plugs into the Main Interconnect Board, except the LSI-11 Board and the Utility Board, has an associated pair of bus grant jumpers.

Jumper pairs are either set to the PASS or the NO PASS position. In the PASS position, the bus grant is passed to the next inline board. In the NO PASS position, the grant is passed or intercepted by the board. For example, if the jumper pair J23/30 is strapped to PASS, the bus grant is passed or intercepted by IOP Board 2.

Figure 3-8 shows the location of the bus grant jumpers. All empty slots and the system memory boards are strapped to PASS. All other slots are strapped to the NO PASS condition. When changing the jumpers, remove the adjacent board, and use needle-nose pliers to reposition the jumper.

Table 3-4 shows the default strapping of the bus grant jumpers. These jumpers pass the bus grant to the next card if the next inline slot is empty.

Table 3-4
Bus Grant Jumpers

Jumper	Default
J19/26	NO PASS
J20/27	PASS
J21/28	PASS
J22/29	PASS
J23/30	PASS
J24/31	PASS
J25/32	NO PASS

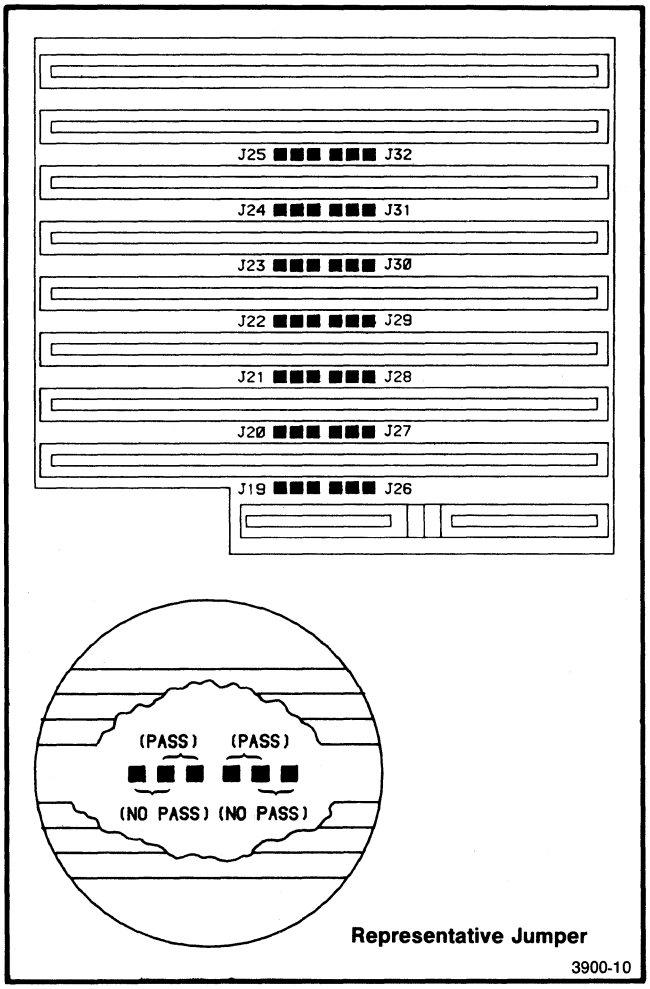


Fig. 3-8. Main Interconnect Board jumper locations.

LSI-11 Configuration

Table 3-5A shows the default jumper configuration for the LSI-11/23. Figure 3-9a shows the jumper locations on the board.

Table 3-5B shows the default jumper configuration for the LSI-11/73. Figure 3-9b shows the jumper locations on the board.

Table 3-5A
Default LSI-11/23 Jumper Configuration

Jumper	Default	Jumper	Default
W1[a]	In	W10	In
W2	In	W11	In
W3	In	W12	In
W4	Out	W13	In
W5	Out	W14	In
W6	In	W15	In
W7	Out	W16	In
W8	In	W17	In
W9	In	W18	In

[a] Jumper numbers are referred to in this instance with "W" references consistent with DEC nomenclature.

Table 3-5B
Default LSI-11/73 Jumper Configuration

Jumper	Default
W1[a]	In
W2	In
W3	Out
W4	In
W5	In
W6	In
W7	In
W8	In
W9	Out

[a] Jumper numbers are referred to in this instance with "W" references consistent with DEC nomenclature.

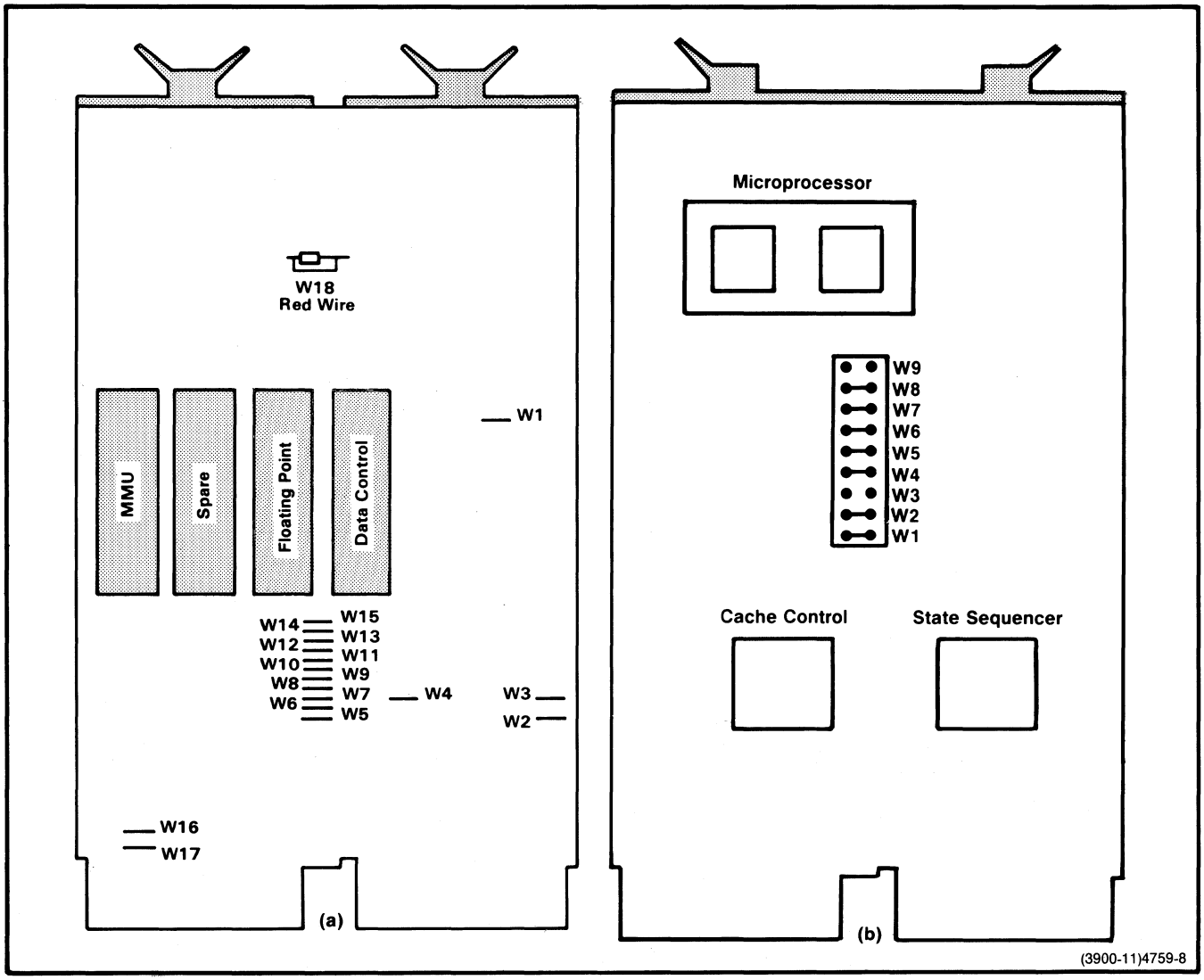


Fig. 3-9. LSI-11 jumper locations.

Utility Board Configuration

This section provides default configuration information for miscellaneous jumpers and straps that control the following functions:

- Diagnostics control
- Parity and bits/character
- RS-232-C port baud rates
- LAV-11 mode selection

Figure 3-10 illustrates the Utility Board. Table 3-6 shows the jumpers and straps in their default positions.

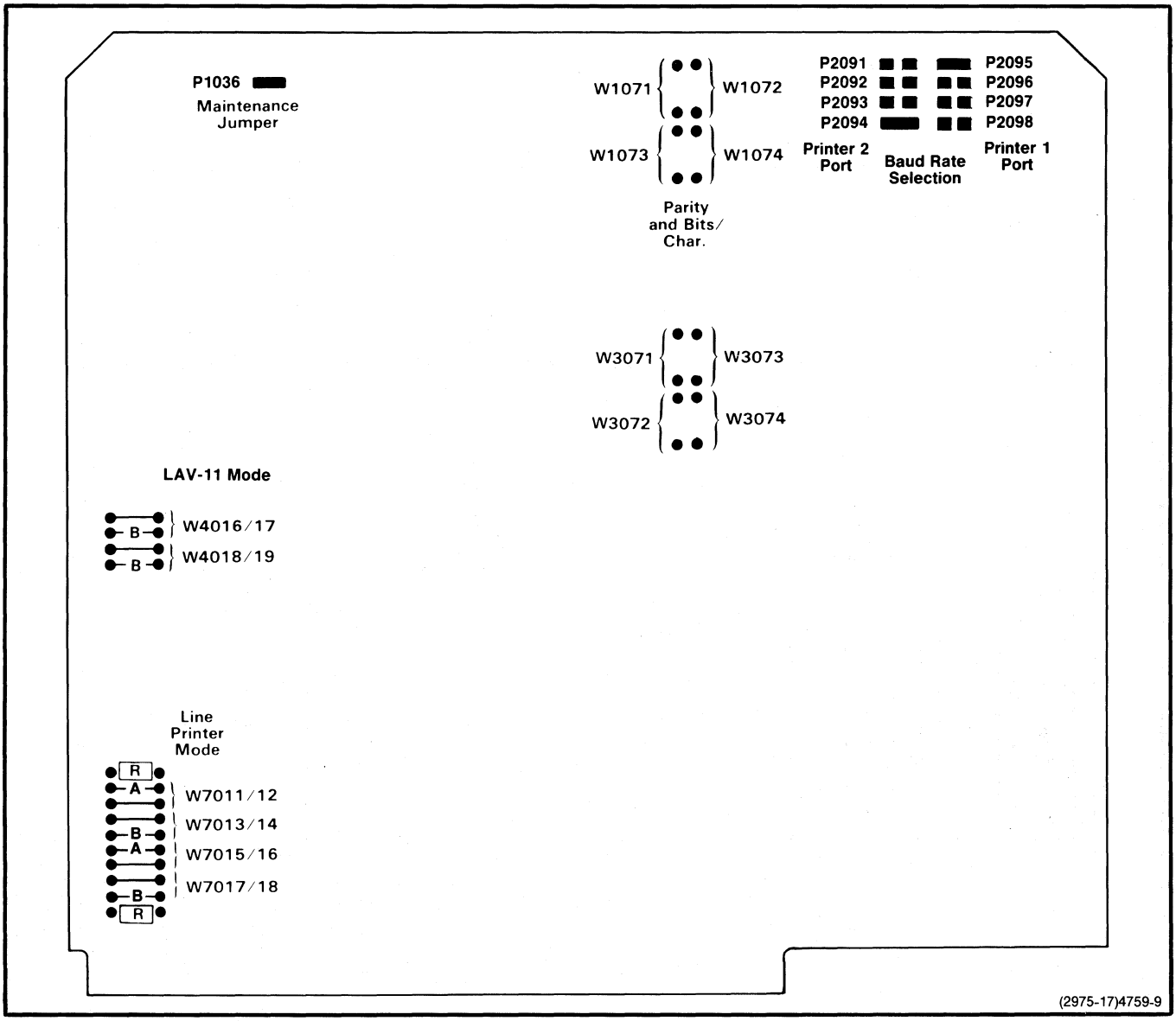


Fig. 3-10. Utility Board strap and jumper locations.

Table 3-6
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
W3071	Printer Port 1 8 Bits/Char.	OUT
W3072	Printer Port 1 No Parity	OUT
W3073	Printer Port 1 No Parity	OUT
W3074	Printer Port 1 8 Bits/Char.	OUT
W1071	Printer Port 2 8 Bits/Char.	OUT
W1072	Printer Port 2 No Parity	OUT
W1073	Printer Port 2 No Parity	OUT
W1074	Printer Port 2 8 Bits/Char.	OUT
P2095	Printer Port 1 2400 Baud	IN
P2096	Printer Port 1 2400 Baud	OUT
P2097	Printer Port 1 2400 Baud	OUT
P2098	Printer Port 1 2400 Baud	OUT
P2091	Printer Port 2 2400 Baud	OUT
P2092	Printer Port 2 2400 Baud	OUT
P2093	Printer Port 2 2400 Baud	OUT
P2094	Printer Port 2 2400 Baud	IN
W7011/12	Printer Port 1 Non-LAV-11	B
W7013/14	Printer Port 1 Non-LAV-11	A
W4016/17	Printer Port 1 Non-LAV-11	A

Table 3-6 (Cont.)
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
W7015/16	Printer Port 1 Non-LAV-11	B
W7017/18	Printer Port 1 Non-LAV-11	A
W4018/19	Printer Port 2 LAV-11	A

The Maintenance Jumper

When jumper P1036 is installed, the 8560 runs through its normal power-up sequence. When P1036 is removed, the 8560 enters the ROM-based debugging mode, and all communication with the 8560 occurs through a printer port. In normal operation, the jumper is always installed.

Parity and Bits/Character

Wire straps allow you to configure the parity and bits/character feature of each printer port. The Utility Board default strapping is set to 8 bits/character and NO PARITY. Table 3-7 shows available port combinations.

Table 3-7
Parity and Bits/Character Straps

Printer 1	W3071	W3072	W3073	W3074
Printer 2	**W1071**	**W1072**	**W1073**	**W1074**
8 Bits/Character	OUT	X[a]	X	OUT
7 Bits/Character	IN	X	X	OUT
6 Bits/Character	OUT	X	X	IN
5 Bits/Character	IN	X	X	IN
Even Parity	X	OUT	IN	X
Odd Parity	X	IN	IN	X
No Parity	X	X	OUT	X

[a] **X = don't care**

Baud Rate Selection

Printer port baud rates are factory set to 2400 baud. However, you can change these baud rates using the jumpers on the Utility Board. Table 3-8 lists the settings for each port.

Table 3-8
Baud Rate Selection Jumpers

Printer Port 1	P2095	P2096	P2097	P2098
Printer Port 2	**P2094**	**P2093**	**P2092**	**P2091**
External Clock	IN	IN	IN	IN
External Clock	IN	IN	IN	OUT
50 Baud	IN	IN	OUT	IN
75 Baud	IN	IN	OUT	OUT
110 Baud	OUT	OUT	OUT	OUT
134.5 Baud	IN	OUT	IN	IN
200 Baud	IN	OUT	IN	OUT
300 Baud	OUT	OUT	IN	OUT
600 Baud	IN	OUT	OUT	IN
1200 Baud	OUT	IN	OUT	OUT
1800 Baud	OUT	IN	OUT	IN
2400 Baud	IN	OUT	OUT	OUT
4800 Baud	OUT	IN	IN	OUT
9600 Baud	OUT	IN	IN	IN

Port Mode Selection

Both printer ports can operate in Digital Equipment Corporation's four LAV-11 modes. (LAV-11 modes force bit 2 of the interrupt vector to a zero.) You can also set the ports to a non-LAV-11 mode. Table 3-9 lists the modes and straps for each port.

Table 3-9
Port Mode Straps

Printer Port 1	W4016/ 4017	W7011/ 7012	W7013/ 7014
Printer Port 2	**W4018/ 4019**	**W7015/ 7016**	**W7017 7018**
LAV-11 Mode: no hold-off	A	A	A
LAV-11 Mode: hold-off while RTS is false	A	B	A
Default Strapping LAV-11 Mode: hold-off while DTSR is false	A	A	B
Non-LAV-11 Mode	B	X[a]	X

[a] **X = don't care**

The System Memory Board Configuration

The memory board jumper straps fall into three basic categories:

- Miscellaneous straps
- Bank interchange straps
- Data/parity interchange test straps

Figure 3-11 shows the jumper/strap locations of the 256K Memory Board. Figure 3-12 shows the jumper/strap locations of the 512K Memory Board.

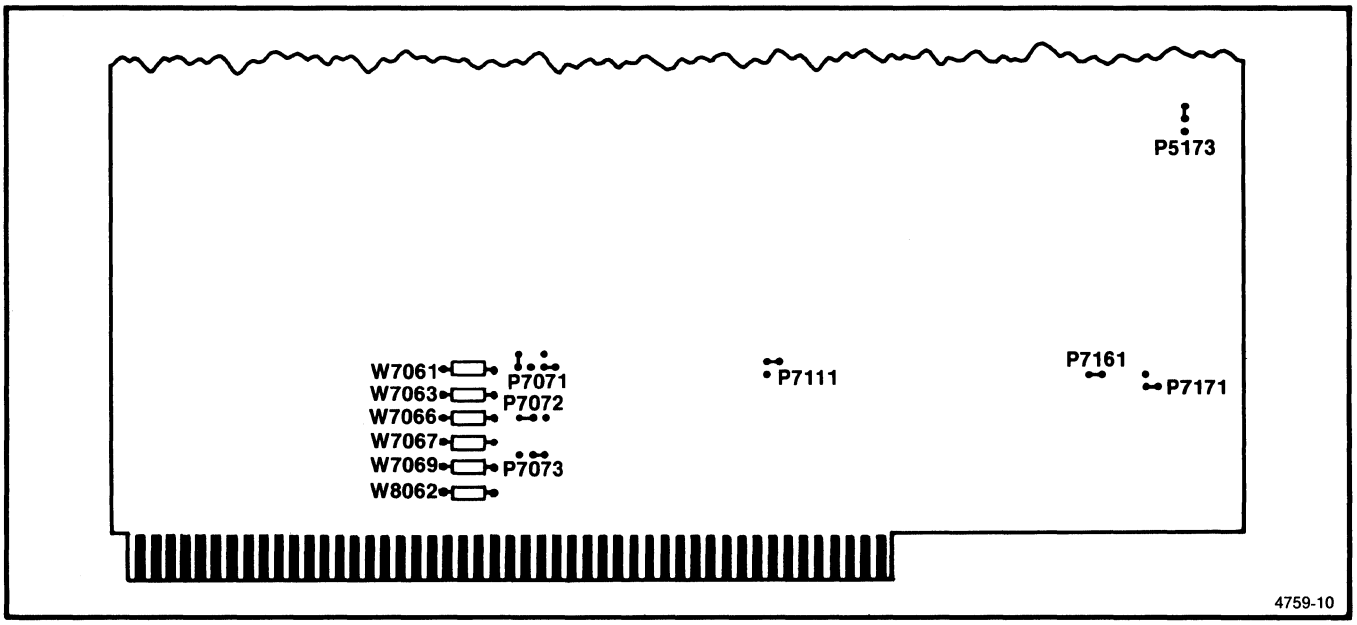


Fig. 3-11. 256K Memory Board jumper/strap locations.

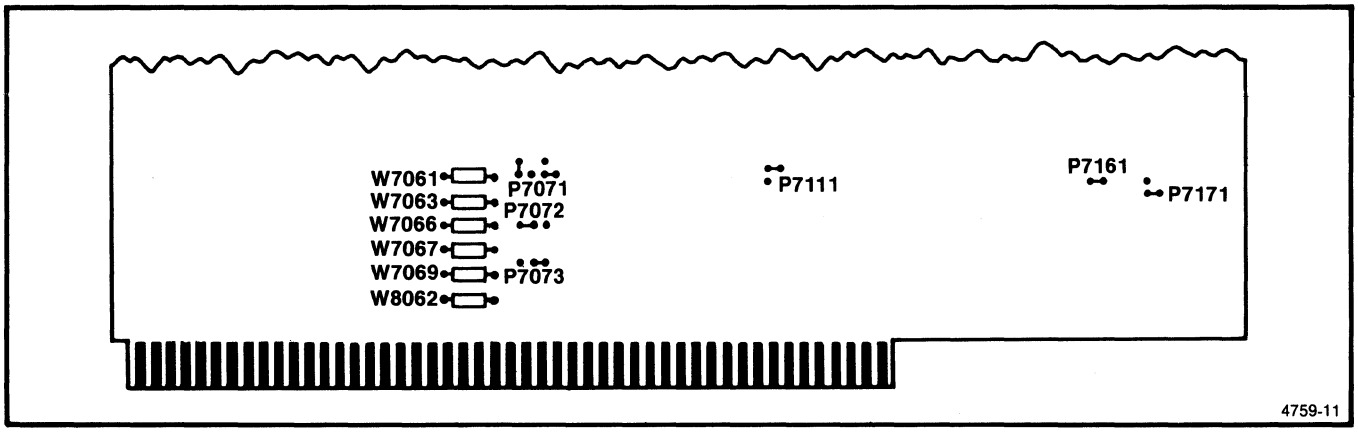


Fig. 3-12. 512K Memory Board jumper/strap locations.

Miscellaneous Straps

Table 3-10 lists the memory board miscellaneous jumpers. P7072 selects the size of the I/O space, and P5173 configures the board either as the upper or the lower memory bank. All other memory board jumpers are used for troubleshooting, to disable signals such as the input data, clock, refresh and others.

Table 3-10
Memory Board Miscellaneous Jumpers

Number	Function
P7072	Sets I/O space
P5173	Configures the board as either the upper or lower 256K-word bank
P7111	Parity enable
P7073	Read enable
P7171	Disables clock signal
P7161	Refresh enable
P5081, P5091, P5101, P5111	Parity/RAM exchange

Address Decoding for Memory Select Upgrades

Table 3-11 shows the positions of the various jumpers and straps involved in address decoding (address lines A19, A20 and A21) for the possible memory-select optional upgrades.

Table 3-11
Memory Address Selection Jumpers/Straps

Straps								Address Lines		
P7071(1)	P7071(2)	W7065	W7063	W7061	W7067	W7069	W8062	A21	A20	A19
1[a]	0[b]	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

[a] a "1" denotes a strap in the lower position.

[b] a "0" denotes a strap in the upper position.

Data and Parity Swapping

Table 3-12 lists the straps by which the low-byte parity-bit memory may be swapped with bit 0 memory, and the high-byte parity-bit memory may be swapped with bit 8 memory. Parity may therefore be read as data, allowing all memory chips on the board to be tested.

Table 3-12
Data and Parity Interchange Test Jumpers

Jumper No.	Name	Signal	Function	Default
P5081	AM-AI AO-AK AN-AJ AP-AL	DN0(H) DNLP(H) DN0(H) DNLP(H)	Swaps DT0H and DNLPH signals J6078	IN OUT OUT IN
P5091	AE-AA AG-AC AF-AB AH-AD	DT0(H) DTLP(H) DT0(H) DTLP(H)	Swaps DT0H and DTLPH signals J5077	IN OUT OUT IN
P5101	AU-AQ AW-AS AV-AR AX-AT	DN8(H) DNHP(H) DN8(H) DNHP(H)	Swaps DN8H and DNHPH signals J5091	IN OUT OUT IN
P5111	BE-BA BG-BC BF-BB BH-BD	DT8(H) DTHP(H) DT8(H) DTHP(H)	Swaps DT8H and DTHPH signals J5108	IN OUT OUT OUT

The system memory in the 8560 MUSDU consists of one or two dynamic RAM boards. Any one, or combination of any two, of the 256K-byte and 512K-byte Memory Board(s) may be used.

Memory Bank Selection

If only one memory board is installed, the board must be assigned to control the low bank of memory addresses. Jumper P7071(1) must be in the A-B position, jumper P7071(2) must be in the D-F position, and jumper P5073 (256K memory board only) must be in the W-X position. Refer to Fig. 3-13 for low-bank configuration of the 256K Memory Board. Refer to Fig. 3-14 for low-bank configuration of the 512K Memory Board (one or two 512K Memory Boards installed). Refer to Fig. 3-15 for low-bank configuration of the 512K Memory Board (256K Memory Board and 512K Memory Board installed.)

If two memory boards are used, one board must be configured as the low bank board. The second board must be configured as the high bank board. Refer to Fig. 3-13 for

high-bank configuration of the 256K Memory Board (two 256K Memory Boards installed). Refer to Fig. 3-15 for high-bank configuration of the 256K Memory Board (256K Memory Board and 512K Memory Board installed). Refer to Fig. 3-14 for high-bank configuration of the 512K Memory Board (two 512K Memory Boards installed).

NOTE

When the 256K and 512K Memory Boards are used together for a 768K-byte memory system, the 512K Memory Board must be configured as the low bank and the 256K Memory Board must be configured as the high bank. Refer to Fig. 3-15 for jumper locations.

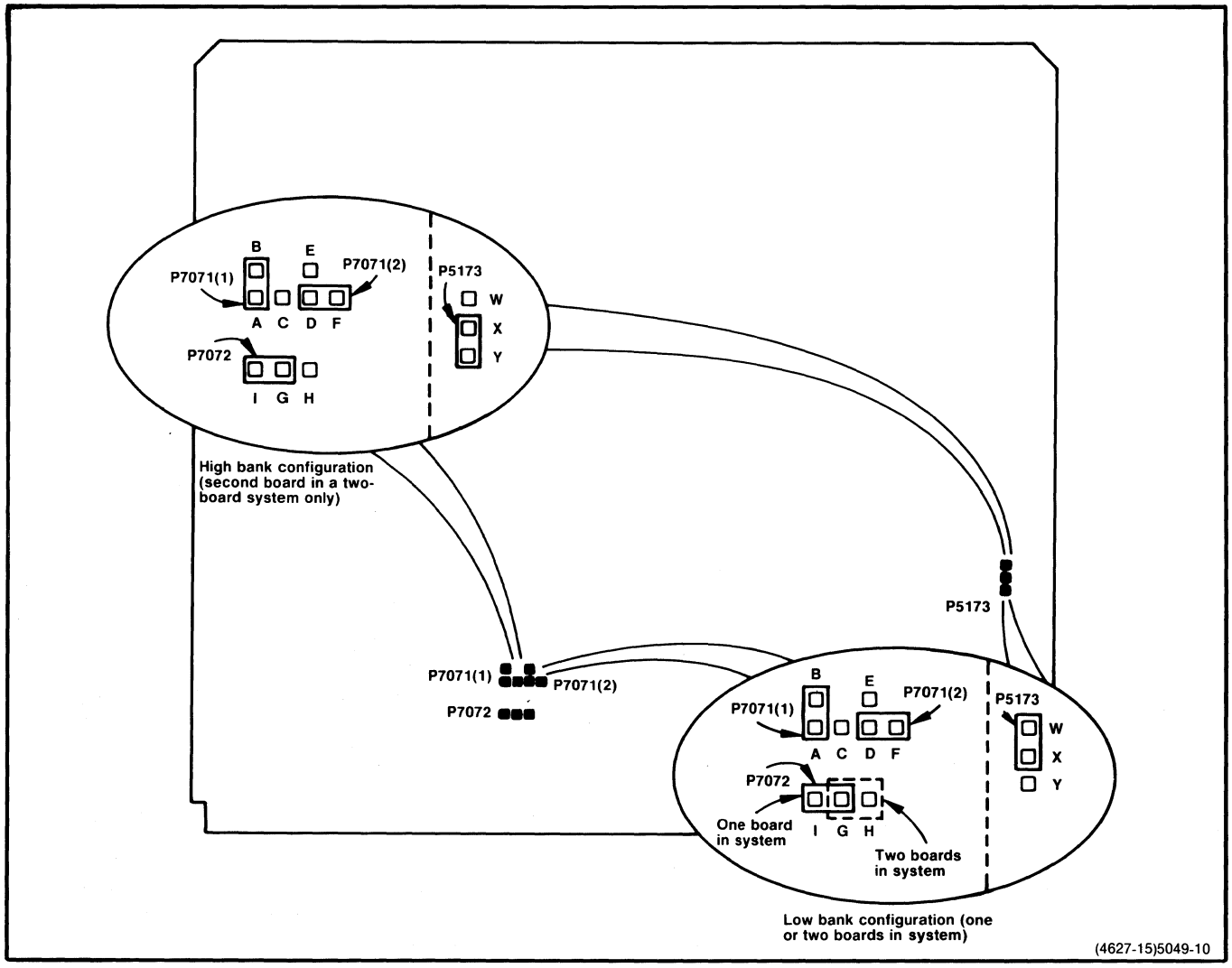


Fig. 3-13. Jumper locations for one or two 256K Memory Boards installed.

I/O Memory Selection

If only one memory board is installed (low-bank operation), jumper P7072 must be in the I-G position. This enables the lower half of the highest 8K of memory for I/O operations. Refer to Fig. 3-13 and Fig. 3-14 for low-bank configurations.

If two memory boards are installed, I/O memory must be enabled on the high-bank board and disabled on the low-bank board. On the low-bank board, jumper P7072 must be in the position G-H; on the high-bank board, jumper P7072 must be in position I-G. Refer to Fig. 3-13, Fig. 3-14 and Fig. 3-15 for jumper configurations.

CAUTION

For the 8560's TNIX operating system to function properly, jumper P7072 must be properly installed.

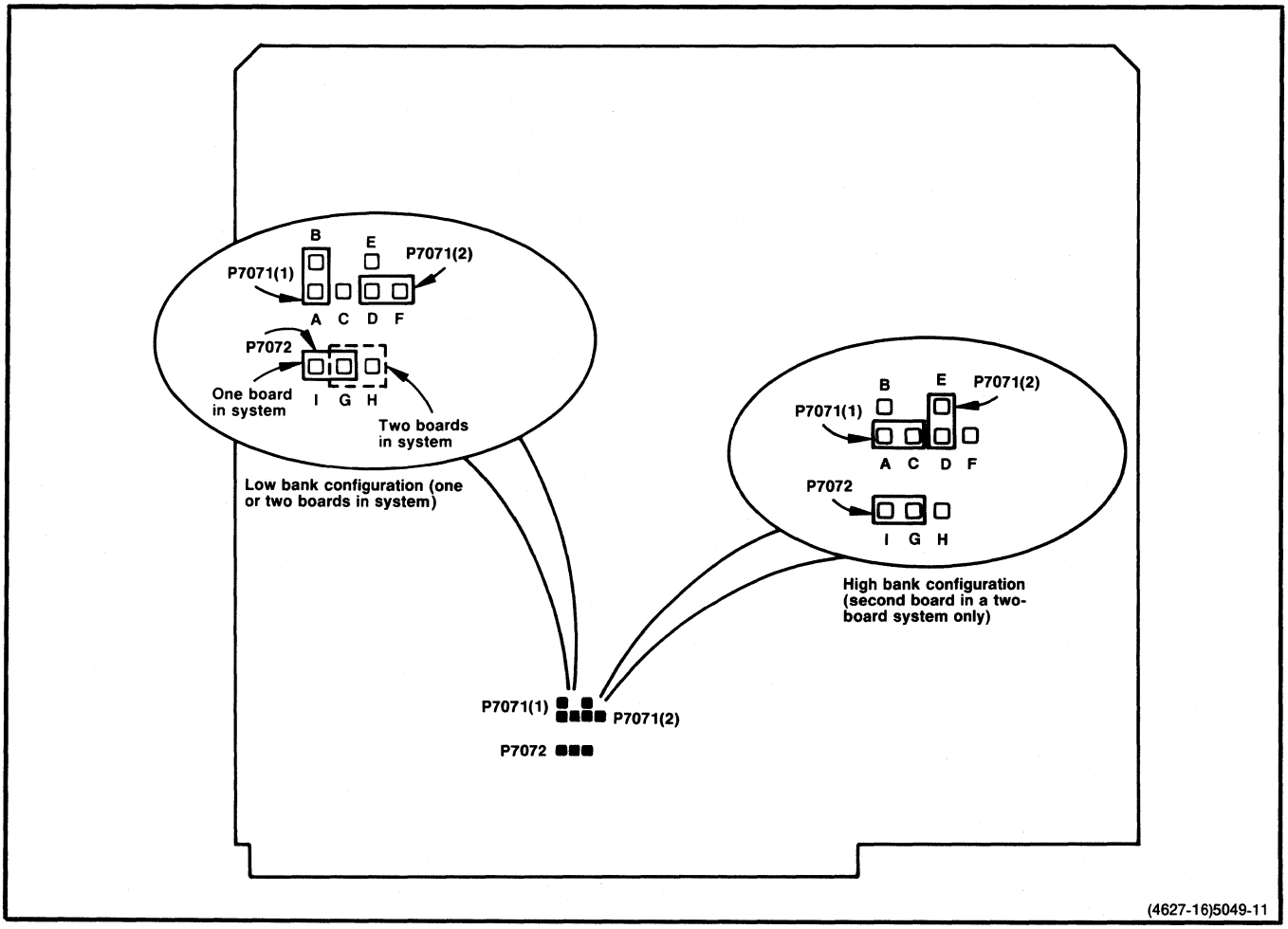


Fig. 3-14. Jumper locations for one or two 512K Memory Boards installed.

RAM Test Jumpers

With the exception of P7071(1), P7071(2), P7072, and P5173 (256K Memory Board only), all jumpers on the memory boards are preset at the factory for normal operation and should not be changed. These jumpers are for test purposes only. Figures 3-13, 3-14, and 3-15 may be used to verify proper placement of the test jumpers.

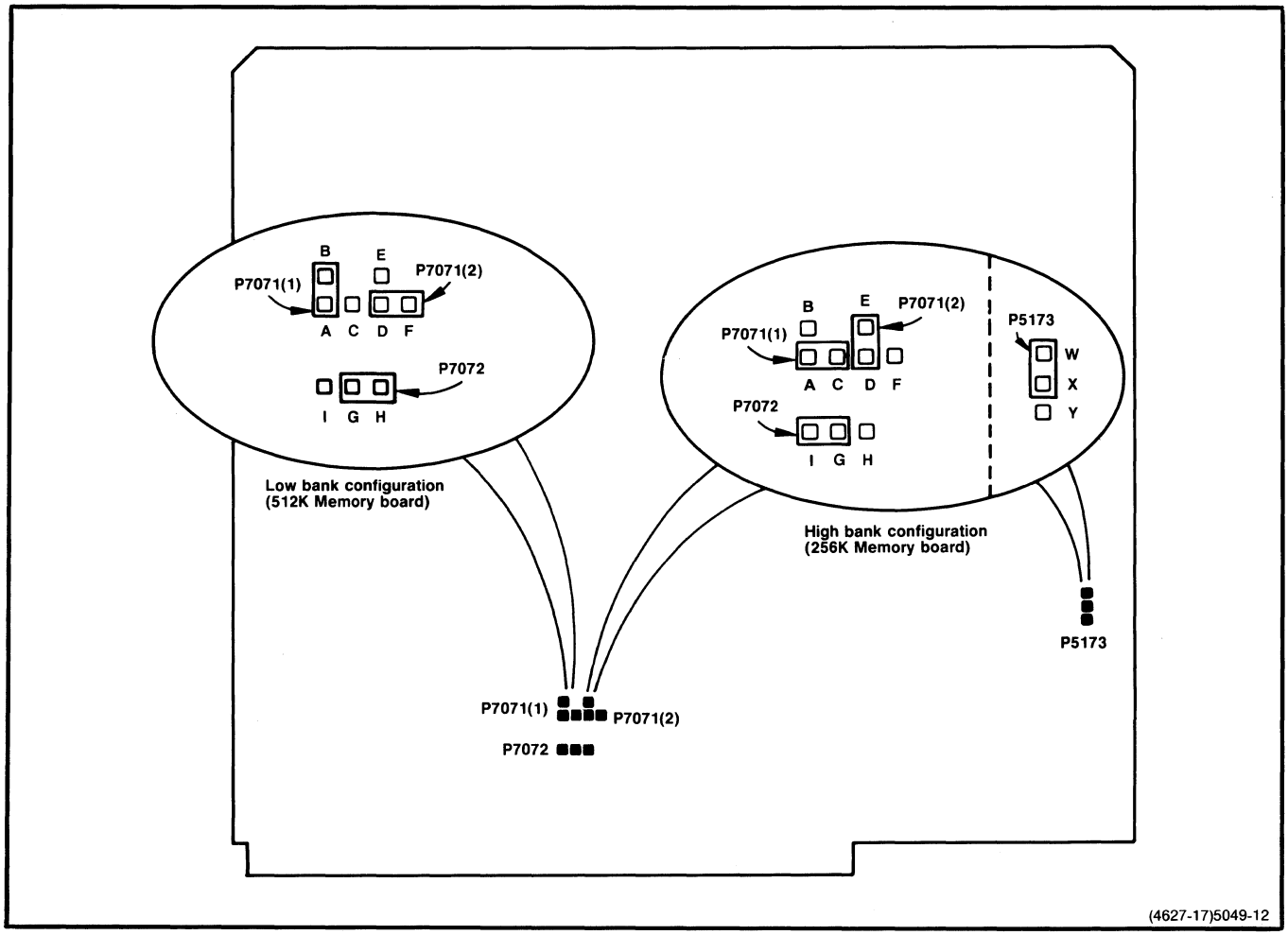


Fig. 3-15. Jumper locations for a 256K and a 512K Memory Board installed.

IOP Board Configuration

The IOP Board provides jumpers and straps for the following functions:

- Priority levels
- Vector strap functions
- Miscellaneous functions
- Board selection

See Fig. 3-19 for proper placement of test jumpers on the IOP Board.

Interrupt Vectors

Each IOP Board generates an interrupt vector to the LSI-11 Processor Board. The two interrupt vector circuits can be independently jumpered to select a level of interrupt priority. One set of jumpers determines which interrupt lines are asserted. The other set of jumpers selects which lines are monitored when intercepting a grant from the LSI-11 processor. Table 3-13 describes the priority levels. Figure 3-16 shows the jumpers for Vectors 0 and 1. Figure 3-17 illustrates jumper configurations for both vectors at priority levels 4, 5, and 6.

Priority level 7 is assigned for LSI-11 use only and is not user-selectable.

Table 3-13
Interrupt Priority Assignments

Priority Level	Interrupt Lines Asserted	Interrupt Lines Monitored
4	BIRQ 4	BIRQ 5, 6
5	BIRQ 4, 5	BIRQ 6
6	BIRQ 4, 6	BIRQ 7
7	BIRQ 4, 6, 7	—

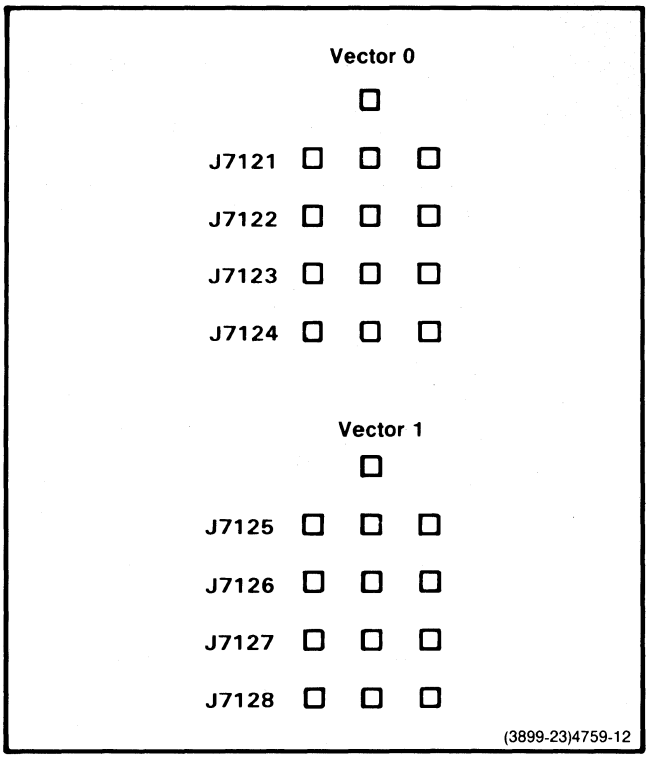


Fig. 3-16. Interrupt priority jumpers.

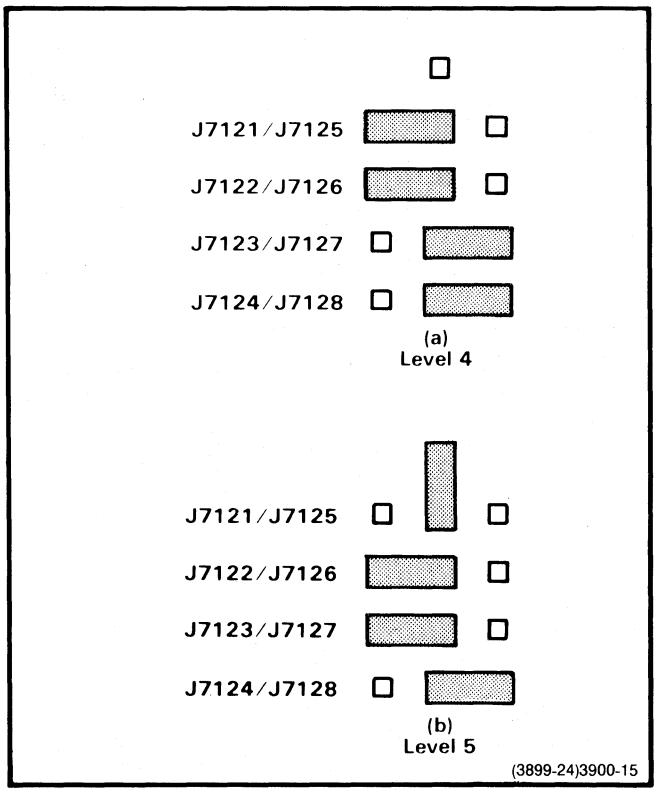


Fig. 3-17. Jumper configurations for interrupt priority levels.

Miscellaneous Diagnostic Jumpers

Table 3-14 shows miscellaneous diagnostic jumpers used by the Tektronix service center for diagnostic purposes.

Table 3-14
Miscellaneous Diagnostic Jumpers

Jumper	Function	Default
J2171	Forced NOP	o o-o
J2172	Processor testing	o o-o
J2173	Testing system bus	o o-o
J2174	Testing SIO DMA	o o-o
J7011	Disable bus driver	IN
J3162	Clock normal/slow	o o-o
J2061	Disable HRQ between 8088 and 8237	o o-o
J2041	I/O read 00 or NOP	OUT
J5161	Normal or forced OP codes	o o-o
J6171	Slow clock	o o-o
J6091	Disable DC010	o o-o

Board Selection Jumpers

Device Register jumper configurations define IOP Boards as either IOP 1 or IOP 2. If your system uses only one IOP Board, it must be configured as IOP 1 and installed in the IOP 1 slot in the 8560 Main Interconnect Board. Figure 3-18a illustrates the jumper configuration for IOP 1.

If your 8560 utilizes two IOP Boards, one of these boards must be configured as IOP 1 and installed in the IOP 1 slot. The second board must be configured as IOP 2 and installed in the IOP 2 slot in the card cage. See Fig. 3-18b.

Memory Jumpering

Table 3-15 shows the memory jumpers. These jumpers are preset at the factory and are not normally moved. They are used by Tektronix to define the board configuration.

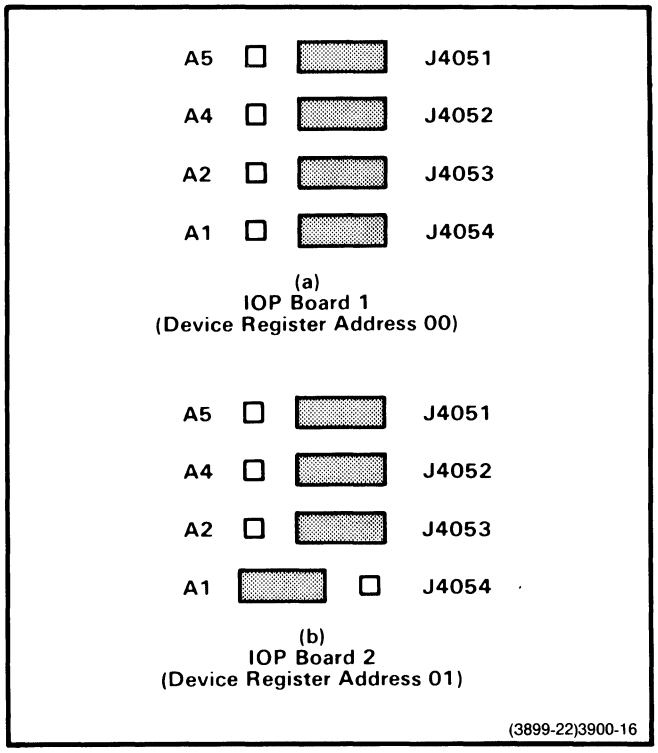


Fig. 3-18. Device Register jumper positions.

Table 3-15
Memory Jumpers

Jumper	Function	Default
J1081 J1082	Changes U1080 from RAM to ROM	ROM
J1091 J1092	Changes U1090 from RAM to ROM	RAM
J1101 J1102	Changes U1100 from RAM to ROM	RAM
J1121 J1122	Changes U1120 from RAM to ROM	RAM
J1131 J1132	Changes U1130 from RAM to ROM	RAM

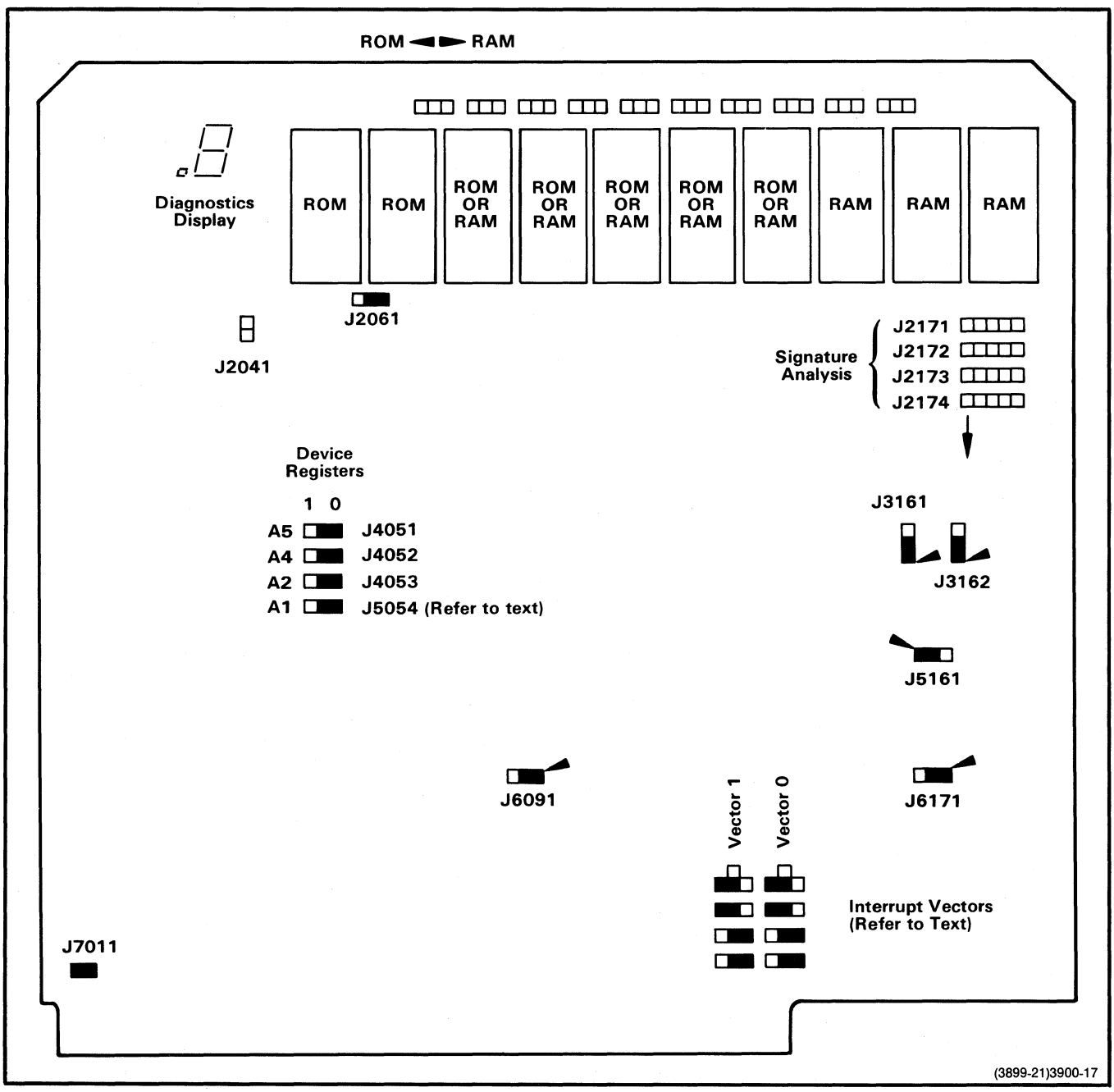


Fig. 3-19. IOP Board jumper/strap locations.

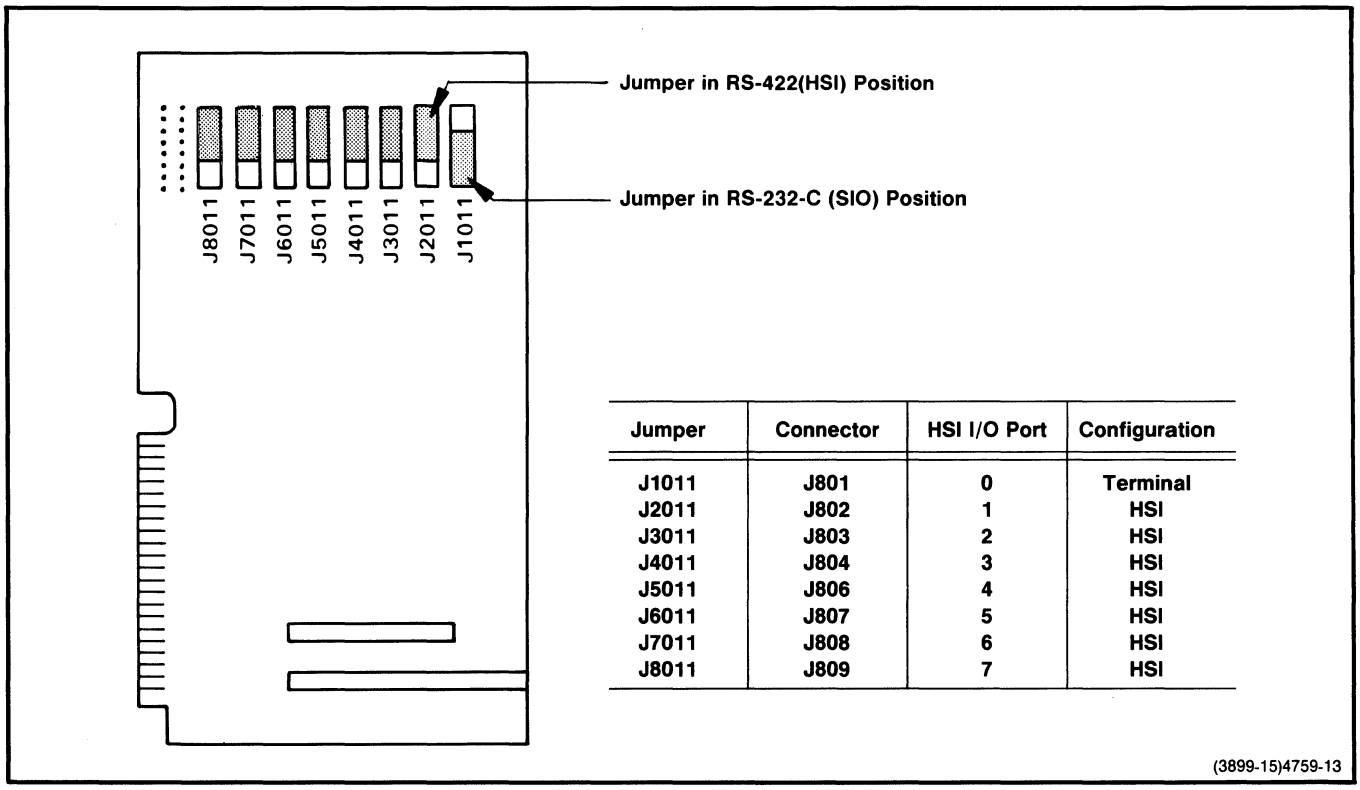
I/O Adapter (IOA) Board Configuration

The IOA Board contains eight jumpers for configuring up to eight HSI ports. J1011 through J4011 service Ports 0 through 3, and J5011 through J8011 service Ports 4 through 7. By moving the jumper either up or down one set of pins, you can change the port configuration from HSI protocol to RS-232-C protocol.

NOTE

HSI Port 0 is factory-jumpered for RS-232-C protocol for use with a system terminal.

Figure 3-20 shows the jumper locations and how to configure them for RS-232-C or RS-422 protocol.



Jumper	Connector	HSI I/O Port	Configuration
J1011	J801	0	Terminal
J2011	J802	1	HSI
J3011	J803	2	HSI
J4011	J804	3	HSI
J5011	J806	4	HSI
J6011	J807	5	HSI
J7011	J808	6	HSI
J8011	J809	7	HSI

Fig. 3-20. IOA Board jumper locations.

I/O Connector Board Configuration

Figure 3-21 shows the IOC Board strap locations, and Table 3-16 relates the straps to the port connectors. Straps W802 through W811 are associated with the communications ports. There is one strap for every port connector. You can install a resistor or capacitor between the shield (of the transmission line) and ground by first removing the strap. All straps on this board are installed when the board is shipped from the factory .

Table 3-16
IOC Board Straps

Port	Strap	Port	Strap
J801	W8011	J805	W8051
J802	W8021	J807	W8071
J803	W8031	J808	W8081
J804	W8041	J809	W8091
J805	W8051	J810	W8101

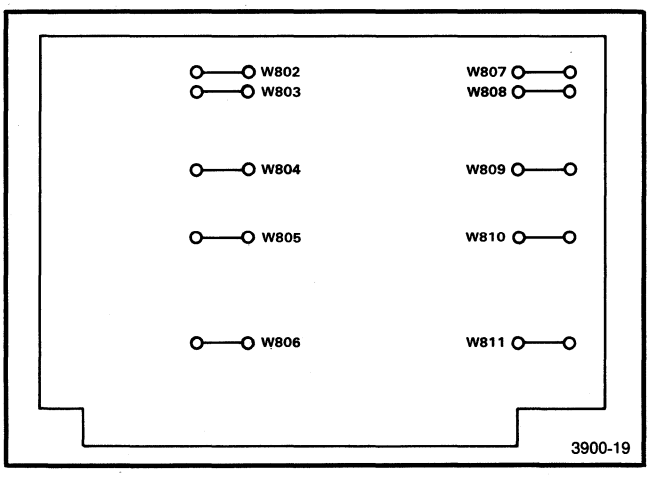


Fig. 3-21. IOC Board strap locations.

MSC Board Configuration

Figure 3-22 shows the MSC Board jumper locations. Table 3-17 lists the jumper functions and their default positions. Schematics show all jumpers in the default position.

Table 3-17
MSC Board Configuration

Jumper	Default Strapping	Function
P3021	o-o o	Device address = 777150
P3111 P2063	IN o o-o	P3111 and P2063 are used for NOP testing when both are not in their normal positions
P2061	OUT	Used for diagnostic pushbutton
P2163	o-o o	MSC SCSI ID = 7
P2161	o-o o	Unused
P614	o | o o	Used for phase locked loop calibration

Xebec S1410 Disk Controller Board Configuration

The Xebec S1410 Disk Controller Board provides jumpers and straps which are preset at the factory. Jumper W3, together with the connection of various feed-throughs, determines the sector size and number of sectors per track. These feed-throughs are located on the board above the 50-pin connector and to the right of the termination resistor pack. Figure 3-23 shows the location of Jumper W3 and the feed-throughs.

Flexible Disk Drive QumeTrak 242

There are several jumpers and straps on the QumeTrak 242 Flexible Disk Drive. Default jumpering and strapping consists of cutting trace B and Z of the programmable shunt and adding optional jumpers C, DC, 2S and Y.

NOTE

*Refer to the **QumeTrak 242 Maintenance Manual** for a detailed description of programmable shunt options.*

Figure 3-24 shows default strapping and jumpering of the QumeTrak 242 main PCB Board.

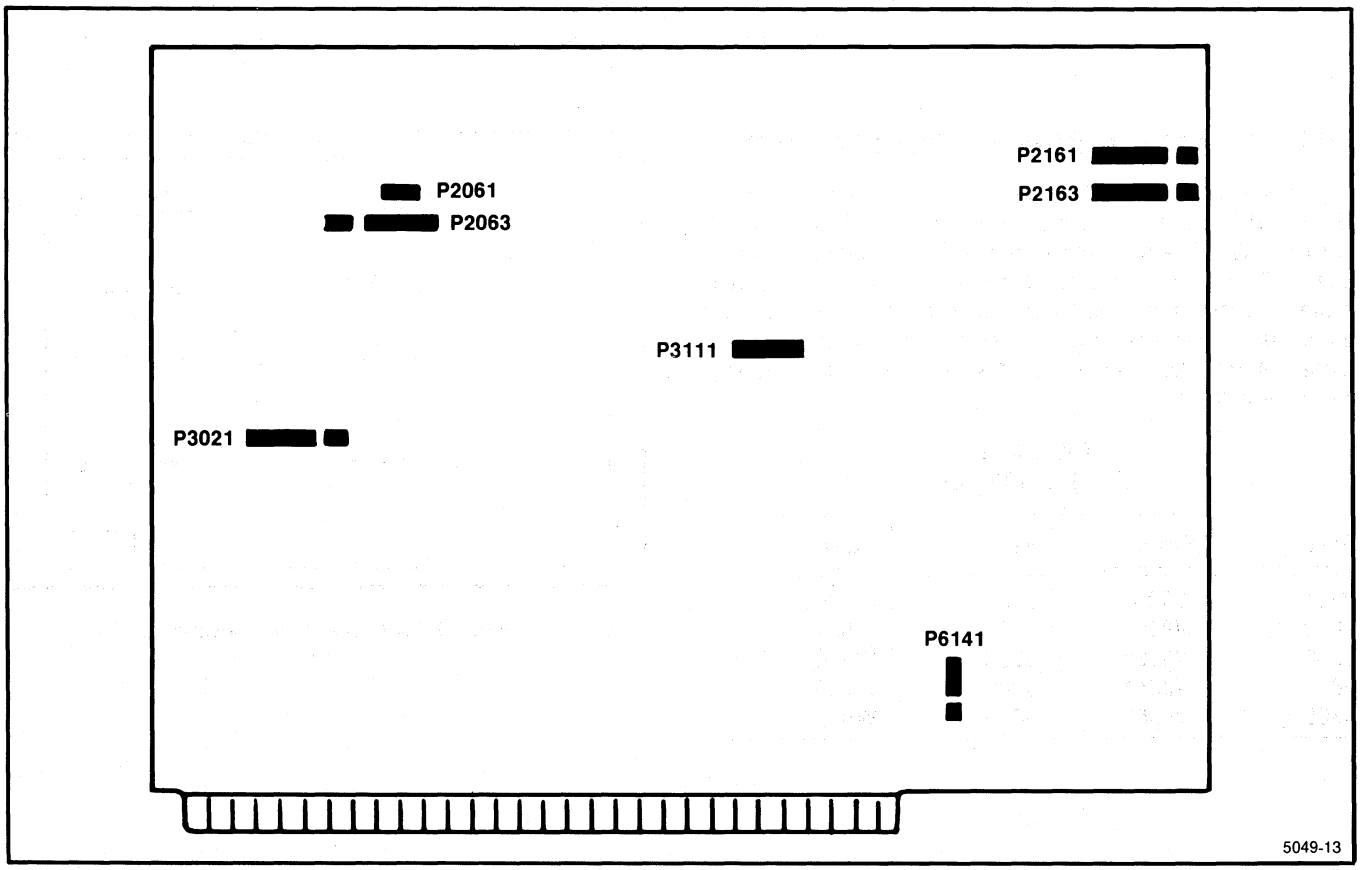


Fig. 3-22. MSC Board jumper locations.

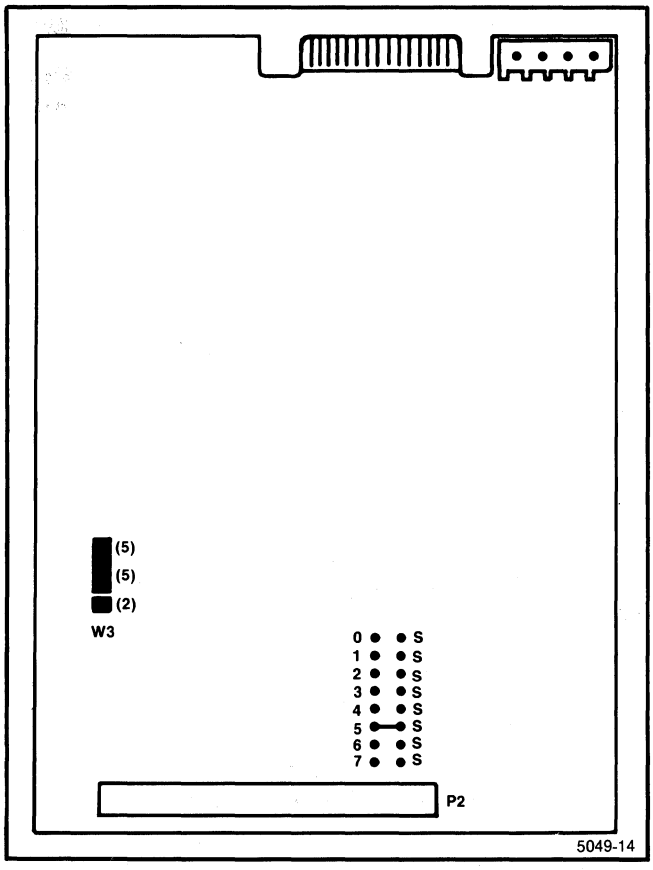


Fig. 3-23. Jumper location on the Xebec Disk Controller.

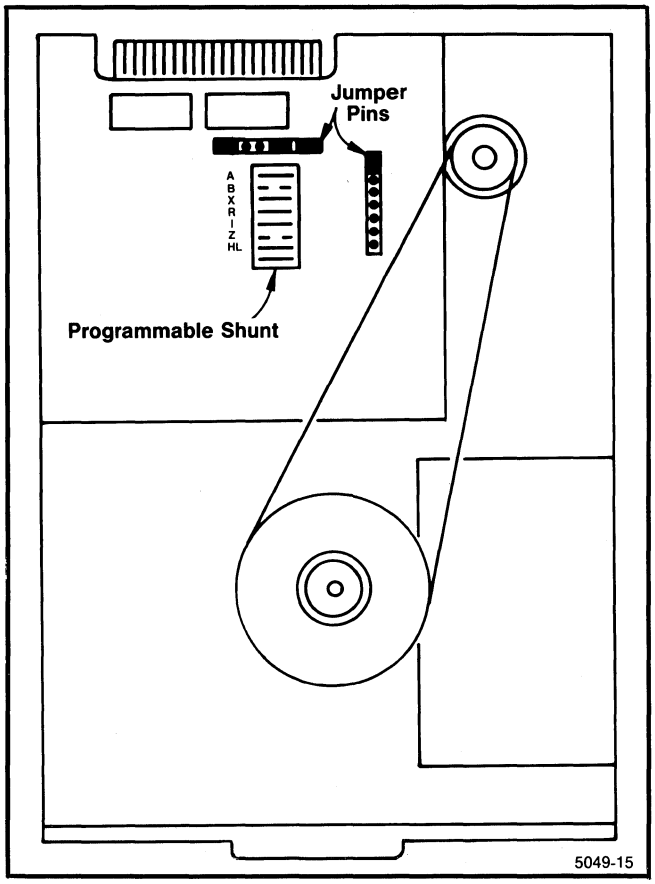


Fig. 3-24. Jumper/strap locations on the QumeTrak 242 Flexible Disk Drive.

Seagate ST419 HARD DISK DRIVE

The programming shunt for the Seagate ST419 Hard Disk Drive is a 14-pin shunt in a 16-pin socket located on Main Control PCB 20096 of the Seagate ST419 Hard Disk Drive. Pins 1 and 16 of the socket are not used; the shunts are cut between pins 7 and 10, 6 and 11, and 5 and 12. Refer to the *Seagate ST406/412/419 Microwinchester Service Manual* for a detailed description of the programmable shunt options. The shunt is factory-installed to select the drive as Drive 1. Figure 3-25 shows the programmable shunt for the Seagate ST419 Hard Disk Drive.

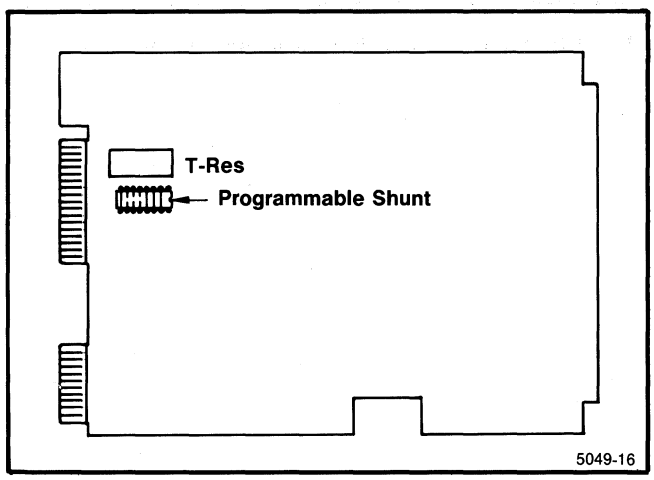


Fig. 3-25. Seagate Hard Disk Drive programmable shunt.

Micropolis 1304 Hard Disk Drive

The drive select for the Micropolis 1304 Hard Disk Drive is a movable jumper on the drive's Device Electronics Board. The jumper is factory-installed to select the drive as Drive 1 or Drive 2. Refer to the *Micropolis 1300 Series Rigid Disk Drive Maintenance Manual* for more information about the selection of drives. Figure 3-26 shows the default jumpering of the Micropolis 1304 Hard Disk Drive.

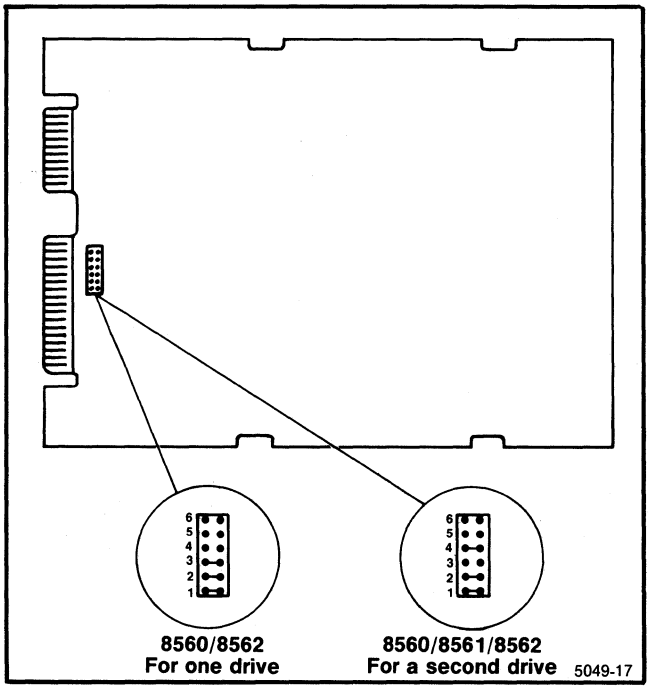


Fig. 3-26. Micropolis 1304 Hard Disk Drive jumper locations.

Power Supply Board Configurations

The Secondary Board and the Regulator Board are the only power supply boards which have jumpers. Tables 3-18 and 3-19 show the jumpers and their functions. Figures 3-27 and 3-28 show the jumper locations.

Most power supply jumpers are used for troubleshooting. Except for P7017 and P7075, all jumpers are normally installed.

Table 3-18
Secondary Board Jumpers

Jumper	Function	Default
P4114	overvoltage protection	IN
P4102	overcurrent protection for -12 V output	IN
P4112	overcurrent protection for +24 V output	IN
P4097	overcurrent protection for +5 V output	IN
P4116	overcurrent protection for +12 V output	IN

Table 3-19
Regulator Board Jumpers

Jumper	Function	Default
P7017	Fan connection	No jumper
P7047	Low line voltage shutdown	IN
P7048	Thermal shutdown	IN
P7075	External power supply connection	No jumper

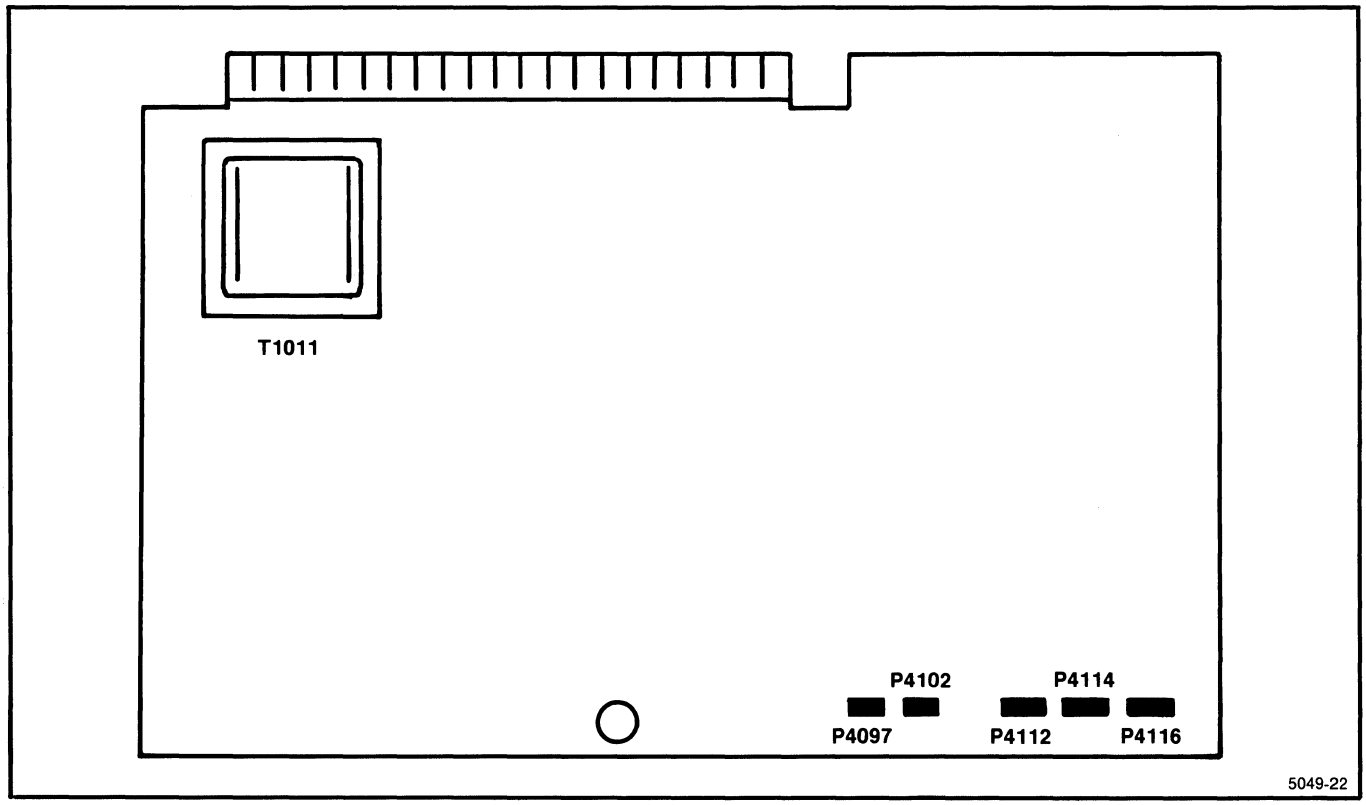


Fig. 3-27. Secondary Board jumper locations.

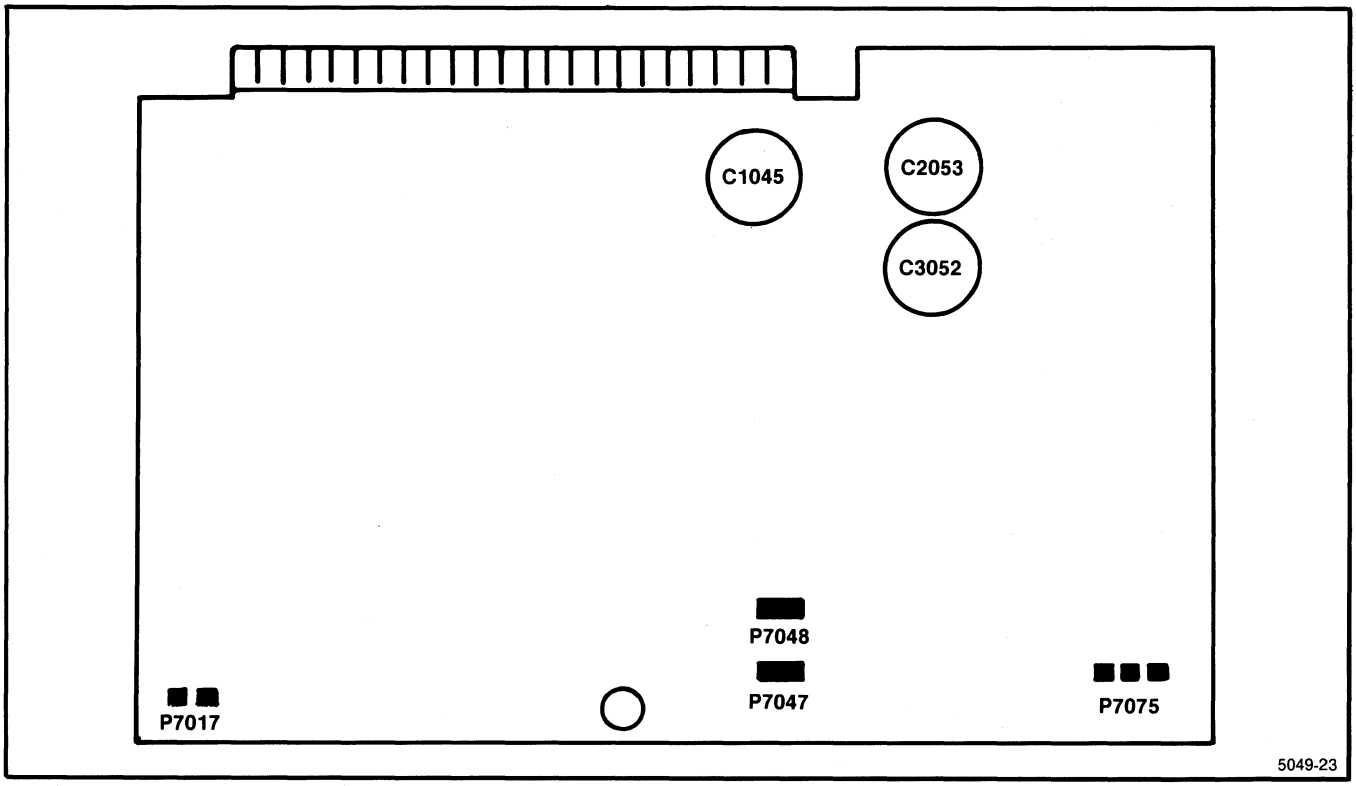


Fig. 3-28. Regulator Board jumper locations.

Section 4
LSI-11 PROCESSOR

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The ODT Terminal 4-1
Entering ODT 4-1

Jumpers 4-1

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Section 4

LSI-11 PROCESSOR

INTRODUCTION

The 8560 uses the Digital Equipment Corporation (DEC) LSI-11 16-bit microcomputer as its main control unit. The LSI-11 is a standard DEC dual height circuit board that is compatible with the DEC LSI-11 bus. The heart of the LSI-11 microcomputer is the LSI-11 chip set. The LSI-11 has the following features and capabilities:

- 128K word address space
- Four levels of vectored interrupts
- DMA
- Memory management
- Octal Debugging Technique (ODT)
- Floating-point arithmetic processor (standard on 8562 MUSDU)

The LSI-11/23 chip set consists of three LSI devices: a data/control unit, a memory management unit, and a floating point unit.

The LSI-11/73 chip set consists of three LSI devices: a data/control unit, an 8K-byte cache memory, and a state sequencer.

The data/control device contains a separate data chip and control chip. The data chip contains the ALU, registers, and interface circuits for the data and address lines. The control chip contains the instruction decoder and instruction ROM.

OCTAL DEBUGGING TECHNIQUE

The Octal Debugging Technique (ODT) is a built-in feature of the LSI-11 which allows you to examine and change register contents and memory locations. ODT also permits single-stepping and restarting of a user program. ODT works through the ODT terminal and responds to single character commands and octal numbers. Table 4-1 contains a summary of ODT commands.

The ODT Terminal

The 8560 treats any device connected to Printer Port LP2 as the ODT terminal. If a line printer is connected to this port when the processor enters ODT, it will print the address of the next instruction to be executed.

Entering ODT

ODT instructions execute only when the processor is in the HALT mode. The HALT mode is entered in any of the following ways:

- The processor executes a HALT instruction
- The 8560 front panel HALT switch is toggled, asserting the BHALT(L) bus signal
- A double bus error occurs because the stack pointer points to a non-existent memory location when the stack is used after an error condition
- A bus error occurs when the processor is attempting to input a vector from an interrupting device.

Table 4-1
ODT Command Summary

Command	ASCII	Function
x/ (Slash)	057	Prints contents of location specified by x, and leaves that location open.
<CR> (Return)	015	Closes an open location and accepts next command.
<LF> (Line Feed)	021	Closes current location and opens the next sequential location.
Rx/ (Register) or $x/	122 044	Opens a specific processor register x.
S (Processor Status)	123	Opens the Processor Status Register (PS). This command must follow a "$" or "R" command.
xG (Go)	107	Goes to location x and starts program execution.
P (Proceed)	120	Resumes execution of a program.

JUMPERS

Refer to Section 3 of this manual for the default jumper configurations of the LSI-11.

Section 5
UTILITY BOARD

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Section 5

UTILITY BOARD

INTRODUCTION

The Utility Board is a system board that plugs into the Main Interconnect Board. It provides several unrelated system functions. Figure 5-1 is a block diagram of the Utility Board hardware.

The Utility Board contains the following logic circuits:

- A two-port RS-232-C compatible communications interface
- 8560 bus driver/receiver logic
- Data Selection logic
- A Line-Time Clock (LTC)
- Power control logic
- Front panel control logic
- Bootstrap and diagnostic ROMs

The **communications interface** provides two RS-232-C ports for communications between the two line printer ports and the 8560 bus.

The **bus driver/receiver logic** interfaces the Utility Board with the 8560 bus. The bus driver/receiver consists of data/address transceiver logic and a control line transceiver.

The **data selection logic** makes Utility Board register data and status information available to the 8560 bus.

The **Line-Time Clock (LTC)** generates LSI-11 event interrupts. LTC logic consists of a clock circuit, LTC Status Register address logic and supporting logic that controls the bootstrap/diagnostic ROM access.

The **power control** circuit provides a power supply voltage level check and controls the system power-up/power-down sequence.

The **front panel control logic** directs the 8560 HALT and RESTART operations.

The **Diagnostic/Bootstrap ROM** provides storage for boot-up instructions and 8560 power-up diagnostics. The two ROM devices together contain two 4K words of diagnostic and bootstrap memory.

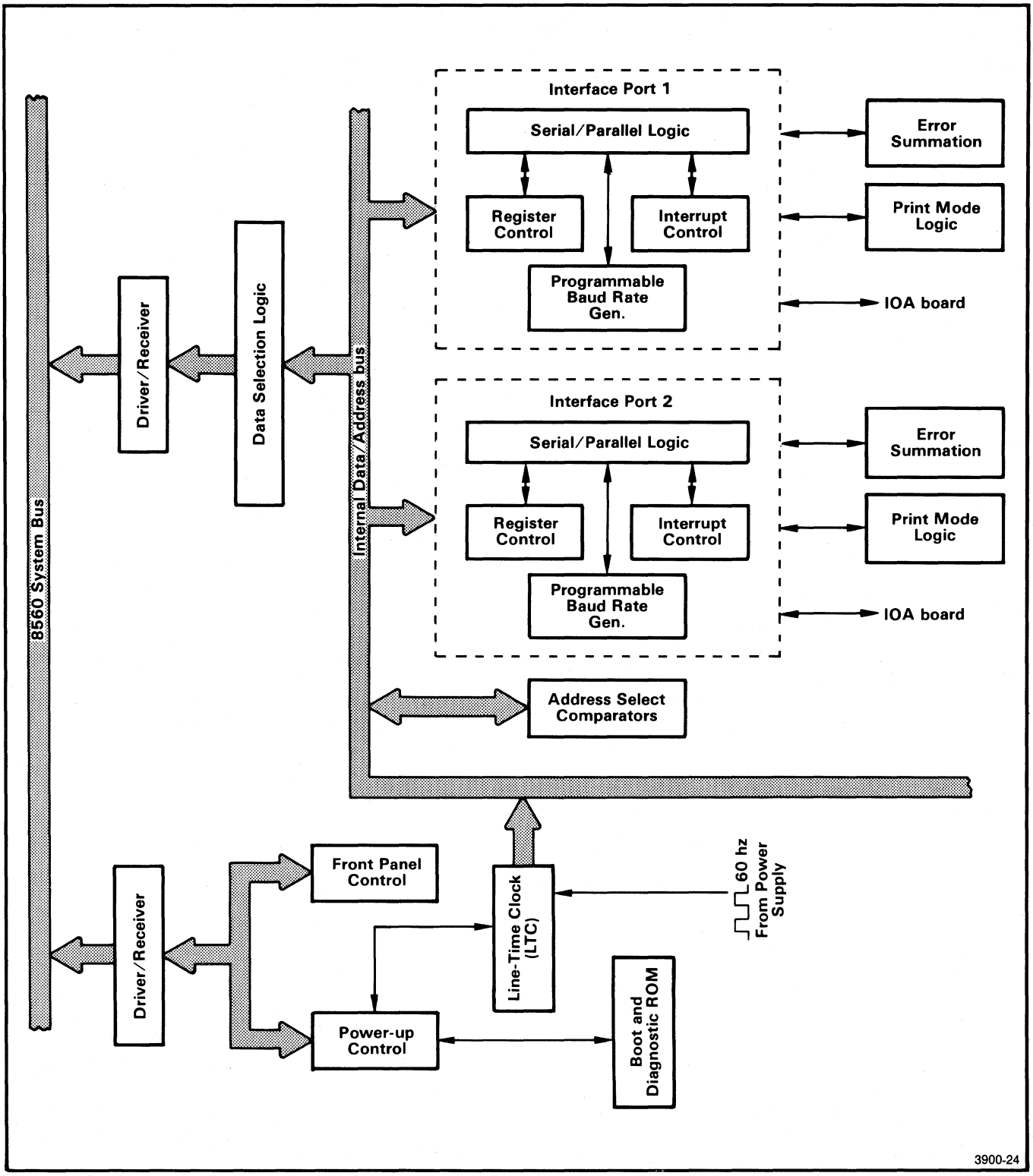


Fig. 5-1. The Utility Board hardware block diagram.

THE COMMUNICATIONS INTERFACE

The communications interface serves two line printer ports compatible with RS-232-C protocol located on the rear panel of the 8560. This interface controls communications between two external line printers and the 8560 bus. Figure 5-2 is a block diagram of the communications interface. The communications interface consists of the following major parts:

- Serial/parallel I/O logic
- Register control logic
- Interrupt control logic
- Error summation logic
- Printer mode control logic
- Data selection logic
- Address select comparators
- Programmable baud rate generator
- Internal data bus
- Bus termination resistors

Serial/Parallel I/O Logic 3 4

The serial/parallel I/O logic consists of two identical circuits, one for each line printer port. Each circuit contains a Universal Asynchronous Receiver/Transmitter (UART) device and the Ready-To-Send (RTS) logic. The UART performs the serial/parallel conversions required to interface line printer ports with the 8560 bus. Since both circuits are identical, only the logic serving Printer Port LP1 is described here.

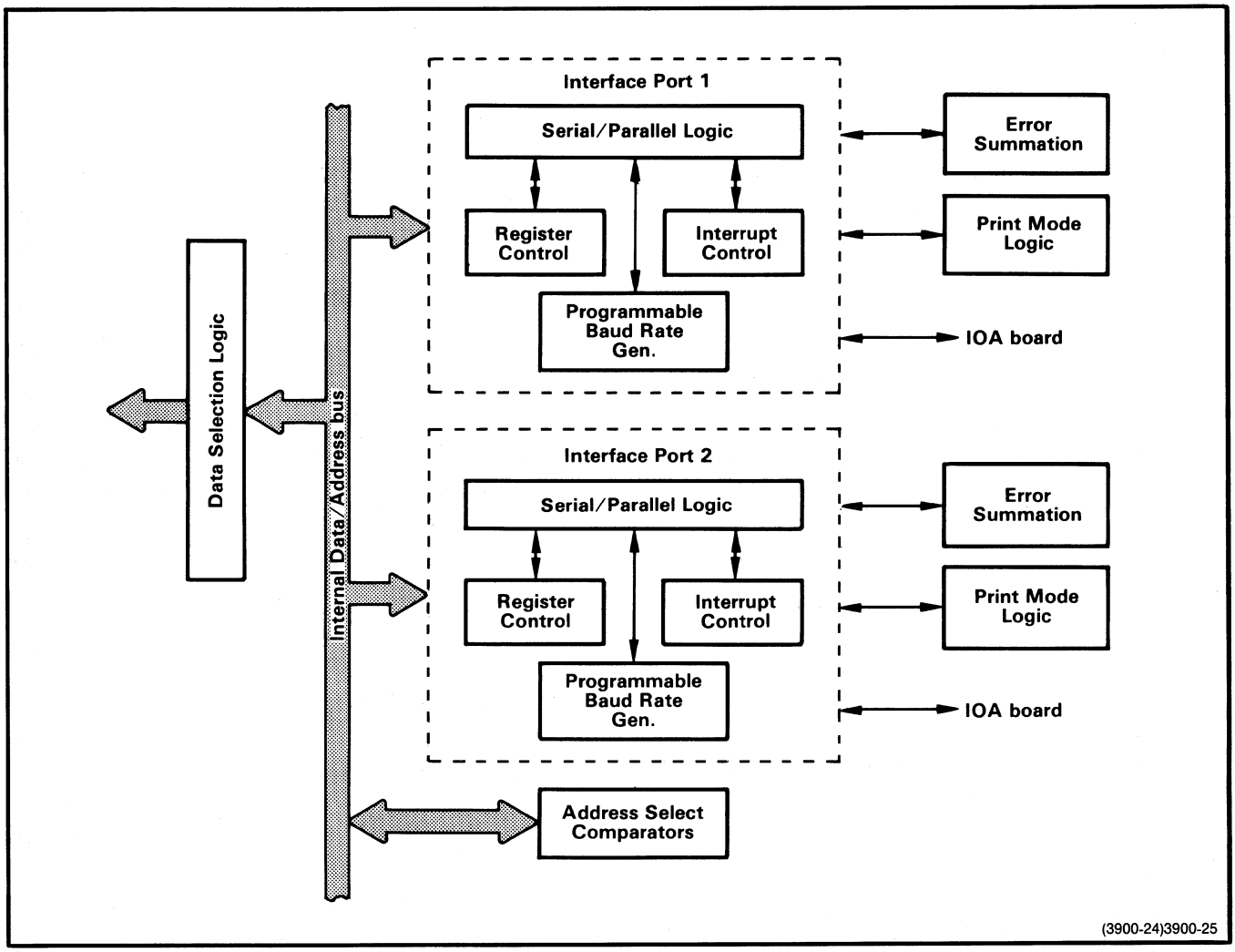


Fig. 5-2. Communications interface block diagram.

The UART accepts serial data into its port and converts it into 8-bit parallel data for the 8560 bus. When the LSI-11 returns data to the connected peripherals, the UART accepts parallel data from the 8560 bus and outputs it to the I/O Adapter Board.

The serial/parallel logic provides two line printer port inputs/outputs that connect to the I/O Adapter Board. The I/O Adapter Board provides the translation between Utility Board TTL levels and standard RS-232-C voltage levels.

Ready-To-Send (RTS) Logic 3 4

The RTS logic receives RTS(L) and RDY1(L) signals and generates the RTS(H) or RDY1(H) signal from them. RTS logic consists of gates U4010C, U6010, and U6020. When RTS(H) is asserted, transmit-enable interrupts are enabled and UART pin 22 goes high. These interrupts inform the LSI-11 that the UART is ready to send more data.

Register Control Logic 3 4 5

Figure 5-3 shows the four principal registers used by each port when data is transferred to and from the LSI-11 processor. Each UART contains a transmit buffer (XBUF) and a receive buffer (RBUF). These buffers control the parallel data transmitted to and from the 8560 bus via the data selector multiplexers. In addition, the Receive Control/Status Register (RCSR) and the Transmit Control/Status Register (XCSR) are used in the serial/parallel data transfer. These two registers are located outside the UART. Table 5-1 lists the serial/parallel interface registers and their addresses. The following paragraphs describe the register control logic and register formats.

Register addresses for the four serial/parallel I/O logic registers (XBUF, RBUF, XCS, and RCS) are located in the 8560 I/O space. The register control logic described here controls the RCS and XCS Registers described later in this section.

Table 5-1
Serial/Parallel Interface Register Addresses

Register	Function	Address (octal)
RCS-1	read/write	17777560
RBUF-1	read-only	17777562
XCS-1	read/write	17777564
XBUF-1	write-only	17777566
RCS-2	read/write	17777510
RBUF-2	read-only	17777512
XCS-2	read/write	17777514
XBUF-2	write-only	17777516

Because the register control logic circuits are identical for both ports, only the logic for Printer Port LP1 is described here. Except for different signal names and device identifiers, this description applies to both ports.

For Printer Port LP1, the register control logic consists of decoder/multiplexer U3120, flip-flops U4020A and U5020A, and part of U1080.

The main register control signals and their basic operations are as follows: Pins 3 and 13 of U3120 (a dual one-of-four decoder) receive signals LA1(H) and LA2(H), respectively. These signals are address bits 1 and 2 of the register address. U3120 generates four signals that select one of four registers for a particular port. The four signals are RD-RBUF-1(L), LD-XBUF-1(L), LD-XCSR-1(L), and LD-RCSR-1(L).

When LD-RCSR-1(L) is asserted, the data on lines DAL0(L) and DAL7(L) is clocked into flip-flops U4020A and U5020A. This asserts flip-flop outputs RDAVI1-EN, CTS-1(H) and NCTS-1(H). RDAVI1-EN informs the LSI-11 that eight bits of read data are available on the 8560 bus. CTS-1(H) informs the peripheral that it can send data. When NCTS-1(H) is asserted, the peripheral stops sending data.

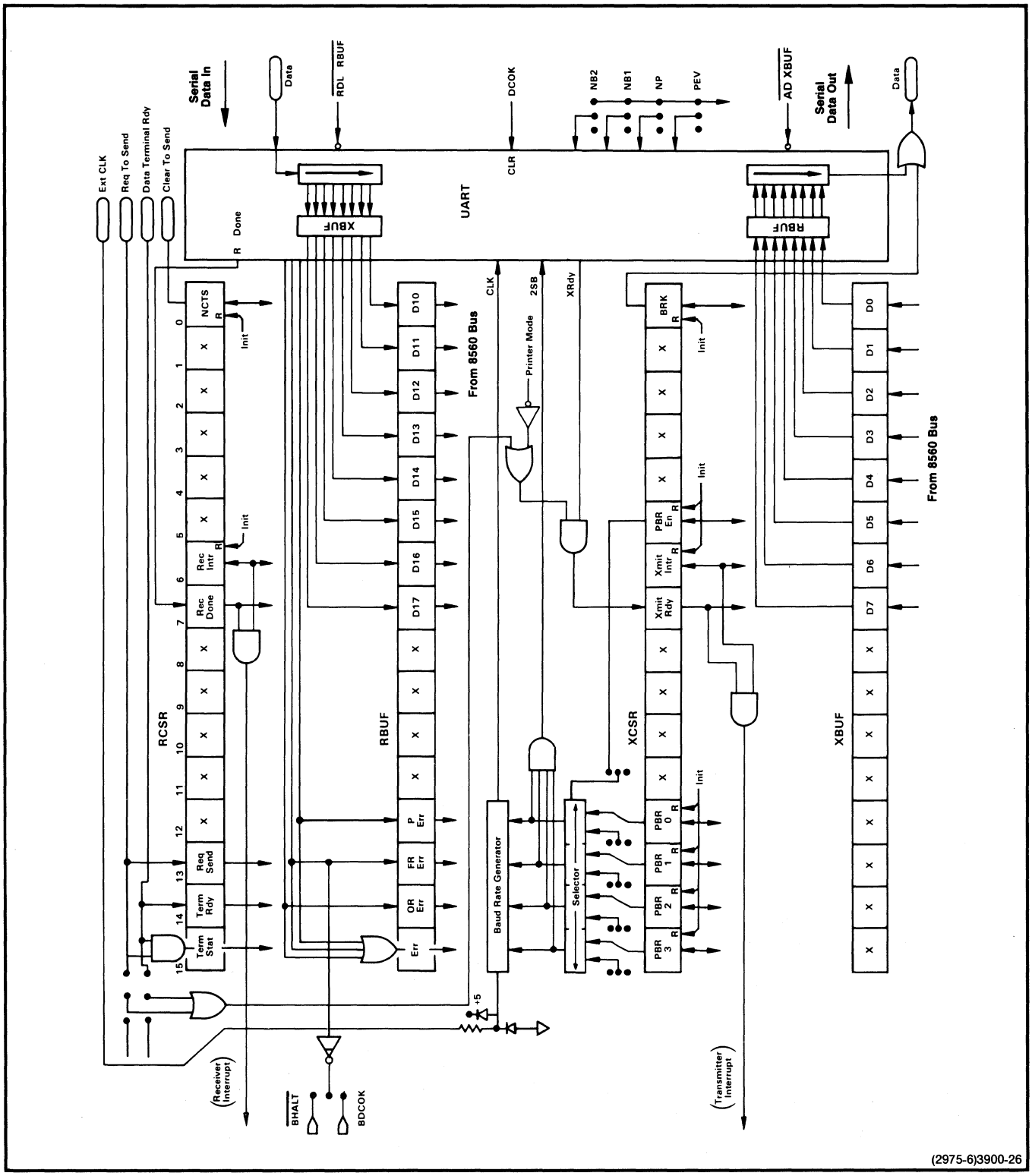


Fig. 5-3. Serial/parallel interface registers.

Register Control Signals

Table 5-2 identifies the most important signals that control the serial/parallel I/O registers for each line printer port.

Table 5-2
Register Control Signals

Signal	Description
TCP	The transmit clock input which controls the transmit baud rate.
RCP	The receive clock input which controls the receive baud rate. Since transmit and receive baud rates are identical, TCP and RCP pins are connected.
DIN(L)	Controls the movement of data from the register addressed by LA1(H) and LA2(H).
SER1(L)	Enables U3120. With either DIN(L) or DOUT(L) asserted, SER1(L) enables the address decoder.
LD-XBUF-1(L)	Connects to flip-flops U4020A and U5020A to generate CTS-1(H) (Clear-to-Send) and NCTS-1(H) (Not-Clear-to-Send) for port 1. When LD-XBUF-1(L) is asserted, data on address lines DAL0 through DAL7 is read by the UART and strobed into its transmit buffer (XBUF).
LD-RCSR-1(L)	Connects to flip-flops U4020A and U5020A to generate the CTS-1(H) (Clear-to-Send) and NCTS-1(H) (Not-Clear-to-Send) for port 1. The output of flip-flop U4020A connects to gate U4060C to be ANDed with the DAV signal from the UART (U3070). The output of gate U4060C generates RDAVI-INT(H) (Read-Data-Available Interrupt). The RD-BUF-1(L) signal strobes the RDAV input (Read-Data-Available) on pin 18. When RD-BUF-1(L) is asserted, the UART makes data available to the 8560 bus.

Table 5-2 (Cont.)
Register Control Signals

Signal	Description
LD-XCSR-1(L)	Is inverted and connected to the clock input of U3080. Output pins 5 and 9 of U3080 then provide two additional register control signals: TBMTI-EN(H) (Transmit Interrupt Enable), and XBREAK(H) (Transmit Break).
TBMT1-EN(H)	Enables the Utility Board to send an interrupt to the LSI-11, informing it that the transmit buffer (XBUF) is ready to accept new data.
XBREAK1(H)	Is asserted when a break in data transmission occurs. XBREAK1(H) is latched into Transmit Control/Status Register bit 0. XBREAK1(H) is cleared by INIT(L) or when the software writes a zero to bit 0 of the XCS Register.

Register Data Flow

The following paragraphs show the data flow for the four previously mentioned serial/parallel interface registers during read and write operations. In this discussion, the terms "read" and "write" refer to reading from and writing to a register, respectively. The terms "transmit" and "receive" are used with respect to the LSI-11.

In a **receive/write operation** data arrives from the IOA Board serially and is transferred to the internal UART RBUF Register. The LSI-11 then writes receive control/status information into the RCS Register. Figure 5-4 illustrates the receive/write operation.

In a **receive/read operation** the LSI-11 reads the RCS Register to determine when to put the data on the 8560 bus. Receive control/status information was written into the RCS Register during the previously explained receive/write operation. Figure 5-5 illustrates the receive/read operation.

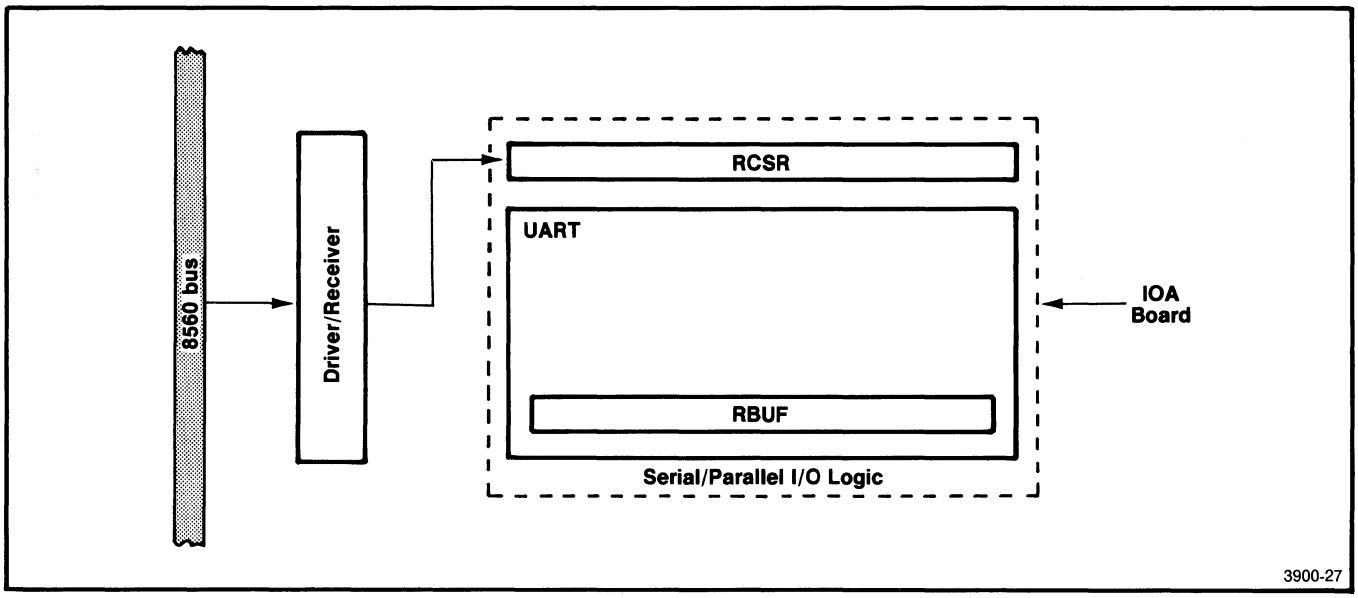


Fig. 5-4. A receive/write operation.

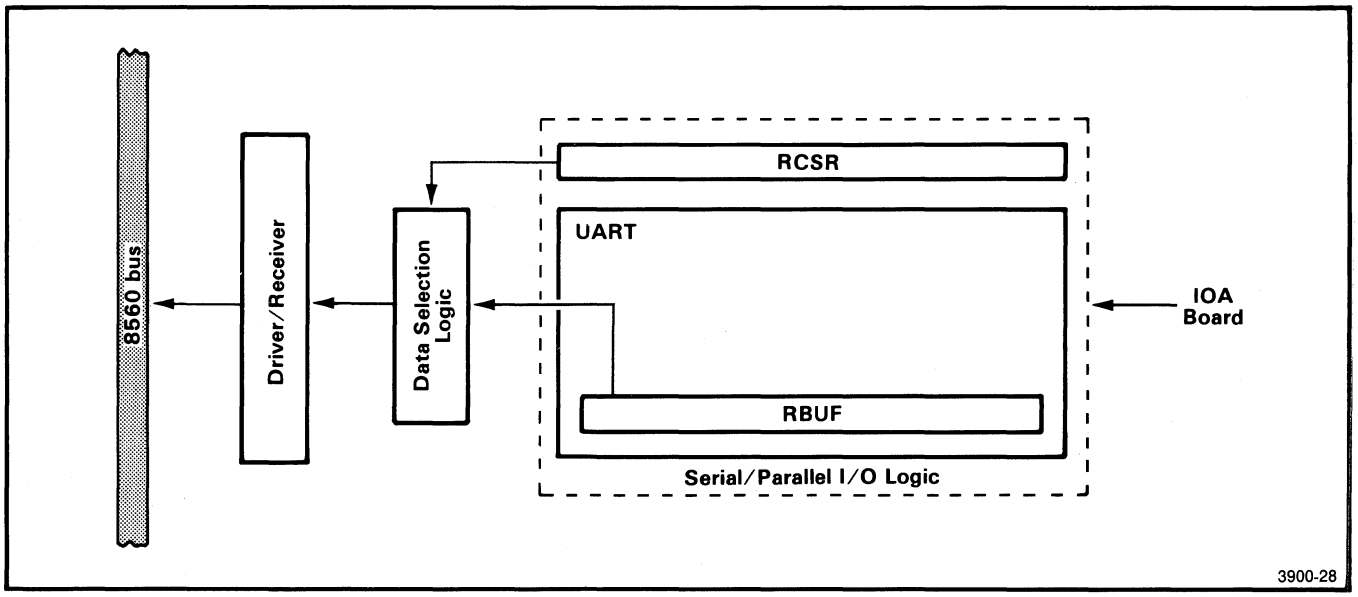


Fig. 5-5. A receive/read operation.

In a **transmit/write operation** data arrives from the 8560 bus in parallel format at the internal UART XBUF Register. The LSI-11 then writes transmit control/status information into the XCS Register. Figure 5-6 illustrates the transmit/write operation.

In a **transmit/read operation** the LSI-11 reads the XCS Register contents (which were written into the XCS Register in the transmit/write operation). If the LSI-11 finds the proper status information in the XCS Register, data in the transmit buffer is then output serially to the IOA Board. Figure 5-7 illustrates the transmit/read operation.

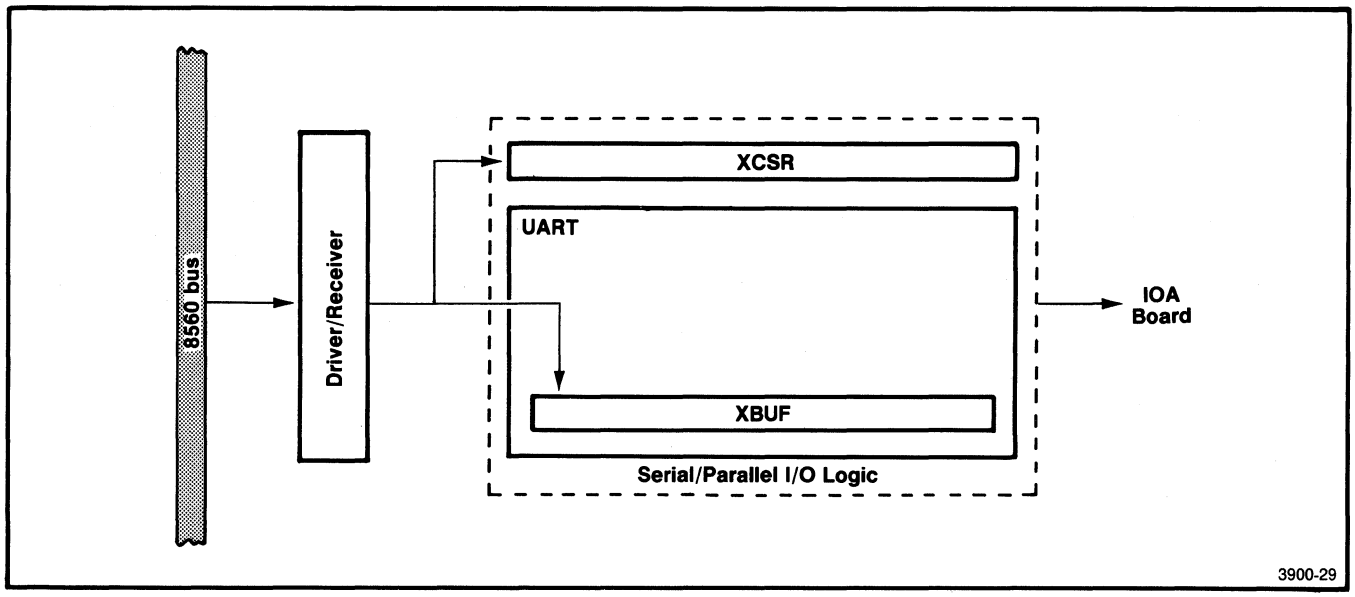


Fig. 5-6. A transmit/write operation.

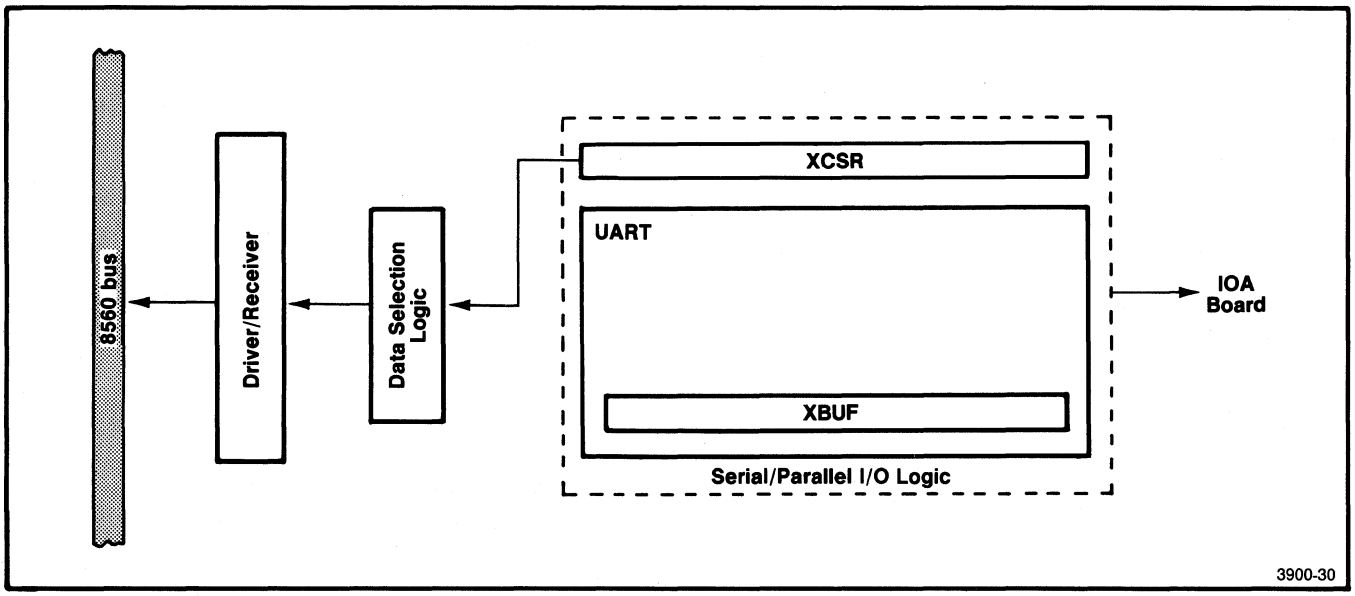


Fig. 5-7. A transmit/read operation.

Register Formats

Following are the four serial/parallel I/O registers:

- Receive Control/Status Register 1 (RCSR1)
- Receive Data Buffer 1 (RBUF1)
- Transmit Control/Status Register 1 (XCSR1)
- Transmit Data Buffer 1 (XBUF1)

Since register formats are identical for both ports, only register formats for port 1 are given here.

Receive Control/Status Register (RCSR) 4

The Receive Control/Status Register (RCSR) acknowledges receipt of characters from the serial input (RS-232-C) lines, and informs the transmitting peripheral to begin sending new data over the serial lines. As shown in Fig. 5-8, the RCS Register uses only six of its bits. Table 5-3 shows individual register bits and their functions.

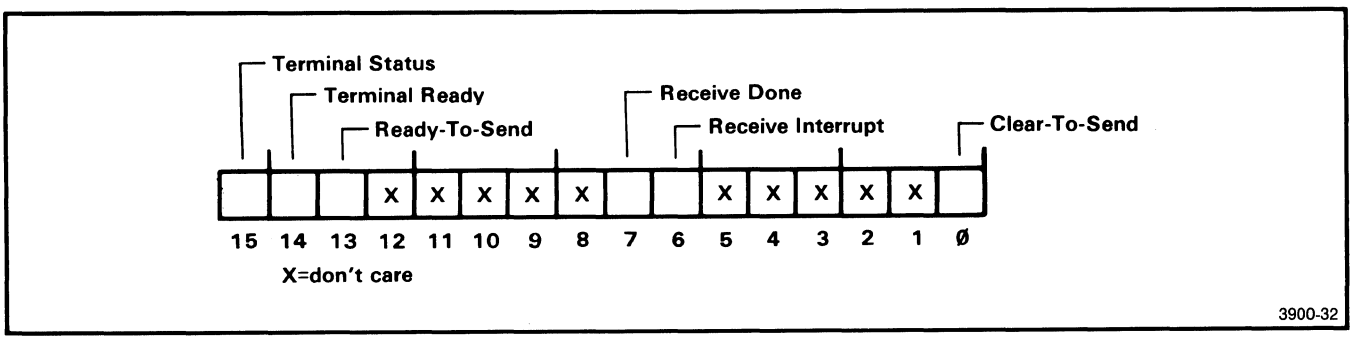


Fig. 5-8. The Receive Control/Status Register (RCSR).

Table 5-3
The Receive Control/Status Register (RCSR)

Bit No.	Function	Description
0	read/write	Bit 0 drives the Clear-To-Send (CTS(H)) signal. If bit 0 is set, CTS(H) is not asserted. If bit 0 is cleared, CTS(H) goes high, and data is sent to the line printer. (This is a read/write bit that is cleared by INIT(H) during initialization).
1-5		These bits are not used.
6	read/write	Bit 6 is set to generate an interrupt request when a character is ready for input to the LSI-11.
7	read-only	Bit 7 is set when a character has been received and is ready to be read from RBUF. This bit is cleared automatically every time the contents of RBUF are read or when DCOK(L) goes high. A receiver interrupt is sent when this bit is set and the receiver is enabled (bit 6 is also set). Bit 7 is cleared either under program control or when INIT(H) is asserted.
8-12	read-only	These bits are read as zero.
13	read-only	This bit is set when RTS is asserted.
14	read-only	This bit is set when DTR is asserted.
15	read-only	This bit is set when DTR and RTS are asserted.

Receive Data Buffer (RBUF) ◇4◇

The receive data buffer (Fig. 5-9) is an internal UART buffer. RBUF receives data from the IOA Board in serial format. Table 5-4 describes individual buffer bits and their functions.

Table 5-4
The Receive Data Buffer (RBUF)

Bit No.	Function	Description
0-7	read-only	Bits 0-7 hold the data received from the IOA Board before it is transferred from the UART to the 8560 bus and the LSI-11. Data is right justified and the UART is strapped to 8 bits.
8-11		These bits are not used.
12	read-only	Bit 12 is set when the parity of the received character does not match the expected parity. If parity was not selected, this bit is always 0. Bit 12 is cleared when DCOK(L) is high or a new valid character is received.
13	read-only	Bit 13 is set when the incoming data is transmitted at the incorrect baud rate. Bit 13 is cleared when DCOK(L) is high or a new valid character is received.
14	read-only	Bit 14 indicates that the previously received character was not read prior to receiving a new character. Bit 14 is cleared when DCOK(L) is high or after receipt of a valid character that overruns the buffer.
15	read-only	Bit 15 is set when either a parity or an overrun error occurs.

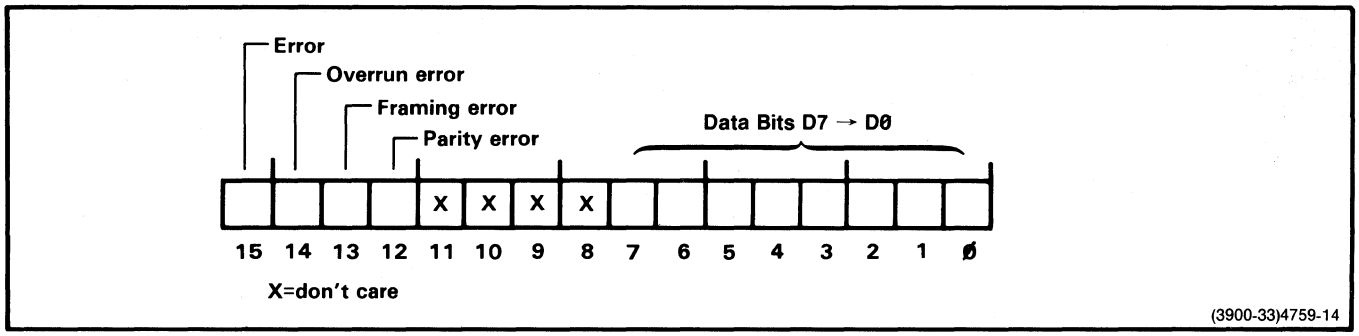


Fig. 5-9. The Receive Data Buffer (RBUF).

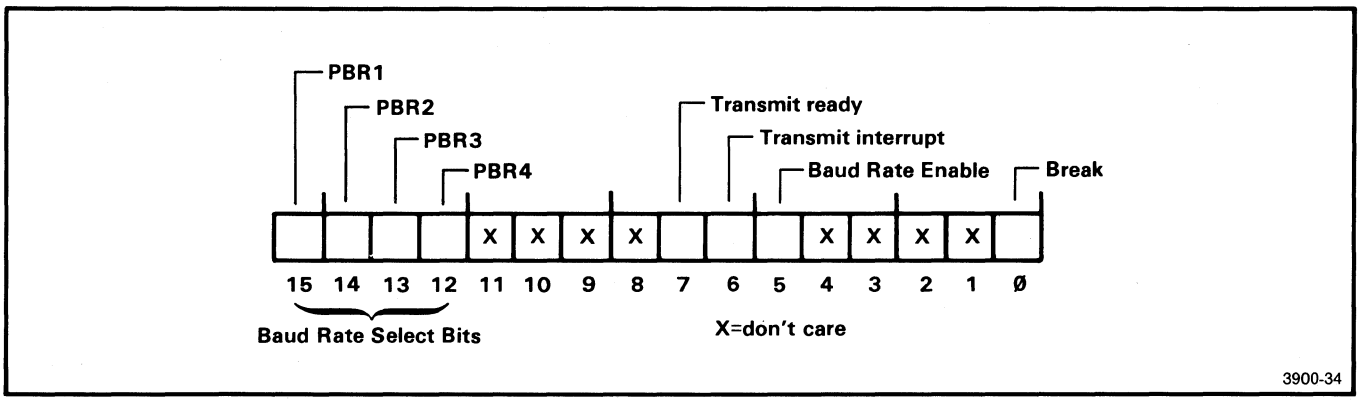


Fig. 5-10. The Transmit Control/Status Register (XCSR).

Transmit Control/Status Register (XCSR) ◇4◇

The Transmit Control/Status Register (XCSR) controls data transmit rate and time. This register is directly accessible by the LSI-11 processor. The Transmit Control/Status Register format is similar to the Receive Control/Status Register. Figure 5-10 shows the Transmit Control/Status Register format, and Table 5-5 describes individual bit functions.

Table 5-5
The Transmit Control/Status Register (XCSR)

Bit No.	Function	Description
0	read/write	When bit 0 is set, a continuous space is transmitted across the RS-232-C interface, giving the receiver a framing error. Bit 0 is cleared by the INIT(H) signal.
1-4		These bits are not used (set to zero).

Table 5-5 (Cont.)
The Transmit Control/Status Register (XCSR)

Bit No.	Function	Description
5	read/write	Bit 5 allows bits 12 through 15 to select the baud rate. Bit 5 must be set before bits 12 through 15 are enabled. Bit 5 is cleared by INIT(H).
6	read/write	Bits 6 and 7 control the start of an interrupt sequence.
7	read-only	Bit 7 is set when the transmit buffer (XBUF) can accept another character. When both bit 7 and bit 6 are set, an interrupt sequence is initiated. The INIT(H) signal clears bit 7.
8-11		These bits are not used (set to zero).
12-15	read-write	Bits 12 through 15 program the baud rate generator for baud rates between 50 and 9600 baud or external clock input. Before bits 12 through 15 can be enabled, XCS Register bit 5 must be set.

Transmit Data Buffer (XBUF) ◇4

The Transmit Data Buffer is an internal UART buffer that stores the data as it is received from the 8560 bus through the bus driver/receiver. (The bus driver/receiver logic is described later in this section). The data is transferred from the buffer to an internal UART shift register and serially output to the I/O Adapter Board. Figure 5-11 shows the Transmit Data Buffer, and Table 5-6 describes the individual bits.

Table 5-6
The Transmit Data Buffer (XBUF)

Bit No.	Function	Description
0-7	write-only	Bits 0 through 7 hold the data before it is transferred to the internal UART shift register and serially output to the IOA Board.
8-15	read-only	These bits are not used (set to zero).

Interrupt Control Logic ◇9

The Utility Board interrupt control logic allows the serial/parallel logic to interrupt the LSI-11 processor. The Utility Board interrupts the LSI-11 when either one of the receiver buffers is full or when either one of the transmit buffers is empty.

The interrupt control logic consists of flip-flops U2020 and U2030, decoder U3020, various gates and interrupt vector strapping jumpers. There is a set of interrupt logic input circuits for each port. Flip-flops U2030A and U2030B provide interrupts for receive and transmit operations on port 1, respectively. Similarly, flip-flops U2020A and U2020B provide receive and transmit interrupts for port 2.

For port 1, U2030 Q(L) outputs are ANDed with RDAVI-INT(H) and TBMT-EN(H). Port 1 interrupt signals are ORed with port 2 interrupt signals through U3040, generating the interrupt request signal IRQ(H). IRQ(H) is asserted any time a UART has data available for the 8560 bus or is ready to read data from the bus.

The outputs of the four gates (U2040) also connect to U3030 and U3020, generating a set of interrupt vectors for each port. Output pins 14 and 15 of U3020 are ANDed with the IAKI(H) signal to generate VECTOR(L) and the bus grant acknowledge signal, BIAKO(L).

Interrupt Vector Addresses

The interrupt vector address logic references two starting locations in memory for each interface port:

- Port 1 vector address 1 200
- Port 1 vector address 2 204
- Port 2 vector address 1 60
- Port 2 vector address 2 64

Error Summation Logic ◇3 ◇4

The error summation logic consists of a 4-input OR gate (U4050B) and an inverter (U3050C). This logic ORs three UART error detection lines: OR (Over-run Error), FE (Framing Error), and PE (Parity Error).

An **Overrun Error** occurs when data arrives too fast to be read by the LSI-11. This data is lost.

A **Framing Error** is generated by the UART logic when the first stop bit in an RS-232-C character transmission was either not received or was invalid. (Refer to EIA RS-232-C standards for details and parameters of stop bits).

A **Parity Error** occurs when the parity detected does not match the parity programmed by the UART parity straps. These strapping options are described in Section 3.

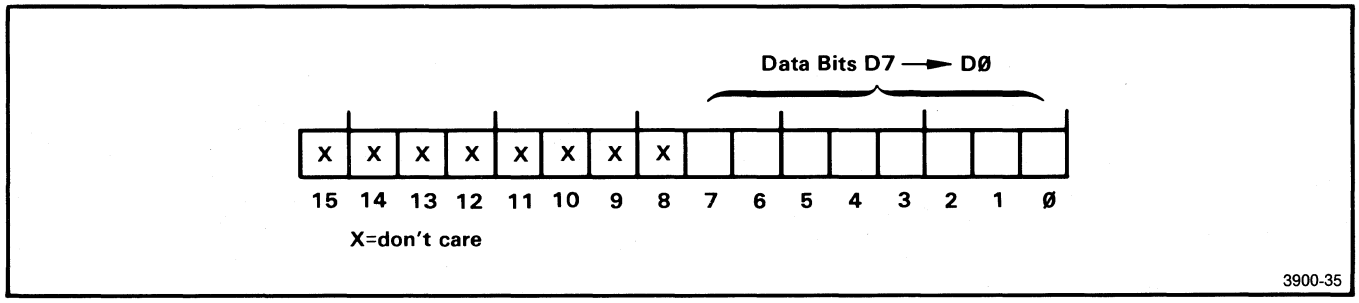


Fig. 5-11. The Transmit Data Buffer (XBUF).

Printer Mode Control Logic ◇3◇4

The printer mode control logic for Printer Port LP1 consists of gates U6010C, U6020E, U4010C, inverter U6020F, and straps W7012/W7011 and W4017/W4016. For Printer Port LP2, the corresponding components are gates U6010B, U6020A, U4010B, inverter U6020B, and straps W7015/W7016 and W4019/W4018.

Printer mode control logic responds to the printer by asserting the RDY1(L) and RTS1(L) signals. Asserting RDY1(H) sets bit 14 of the RCS Register. Asserting RTS1 sets bit 13 in the RCS Register.

The printer type affects the time the transmit buffer XBUF is empty. For additional information on line printer mode strapping, refer to Section 3 of this manual.

Address Select Comparators ◇6

The 8560 address comparator logic consists of four 8136 comparator devices. The address comparator for Printer Port LP1 consists of U6110 and U7110. The address comparator for Printer Port LP2 consists of U6130 and U7130. Since both address comparators are functionally identical, only the address comparator for Printer Port LP1 is described here.

When SYNC(H) is asserted, the data present on data lines DAL3(H)-DAL12(H) is latched into the address comparator (U6110, U7110). If the latched address is valid, pin 9, an open collector output, goes high. U5110D inverts this signal and asserts SER-1(L). SER-1(L) selects the appropriate register and puts its data on the 8560 bus.

Programmable Baud Rate Generation Logic ◇3◇4

The Utility Board provides a crystal-controlled baud rate generator that permits independent baud rate programming for each port (Fig. 5-12). Baud rates are programmable from 50 to 9600 baud and are selected for both RS-232-C ports with Utility Board jumpers. For additional information on baud rate selection, refer to Section 3 of this manual.

Baud rate generation for both RS-232-C ports is identical, except that Printer Port LP2 receives the 2.4576 MHz frequency on pin 5 of U1100. The following description covers only the logic for Printer Port LP1.

The programmable baud rate generation logic consists of U3090, U3100 and part of U3080. Data lines DAL12(H) through DAL15(H) provide programmable baud rate control. These four signals are latched into register U3080. DAL5(H) selects the register output. If pin 6 of U3090 is not asserted, U3090 selects its inputs from jumpers P2095 through P2098 and assumes the baud rate specified.

U3100 is a programmable generator device that produces a master oscillator frequency of 2.4576 MHz. Four data lines from the multiplexer U3090 arrive on inputs S0 through S3 of U3100. These inputs are BCD decoded and determine the baud rate output on pin 10.

The four outputs of multiplexer U3090 are ANDed by U2100B. The output of U2100B drives the TSB input to U3070. When TSB is asserted, it informs the UART that two stop bits are needed.

Pin 8 of U3080 is driven by the DAL0(H) signal, and asserts the XBREAK1(H) signal and the SEROUT1(H) signal. XBREAK1(H) sets bit 0 of the Transmit Control/Status Register (XCSR). SEROUT1(H) is the serial data output line to the IOA Board.

Pin 4 of U3080, driven by DAL6(H), asserts TBMIT-EN(H).

Internal Data/Address Bus

The Utility Board uses a 16-bit data bus to transfer data onto the 8560 bus through the data selection logic. The Utility Board's internal data/address bus is accessed by the data selection logic, the two RS-232-C compatible interfaces, and the address select comparators.

Data Selection Logic ◇5

The data selection multiplexer reads data and status information from the Utility Board registers and makes it available to the 8560 bus through the bus driver/receiver. The data selection logic consists of the data selection multiplexer and the data selection line encoder.

The Data Selection Multiplexer

The Utility Board data selection multiplexer consists of eight 8:4 multiplex devices (U1050, U1060, U1110, U2050, U2080, U2110, U4080, U4090), and two 4:1 multiplex devices (U2060 and U3060). Data select lines SELA(L), SELB(L), and SELC(L) are encoded to control the multiplexing logic.

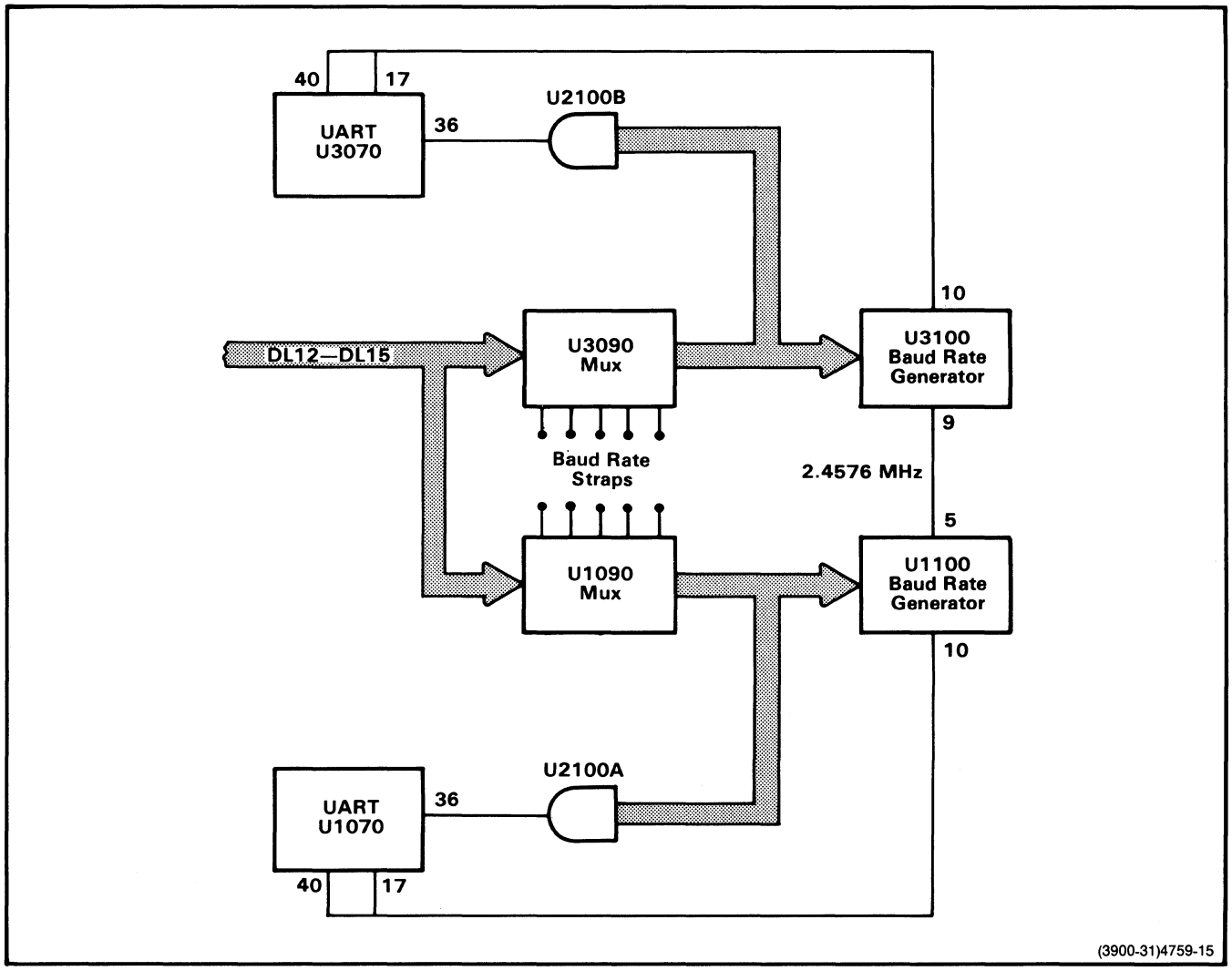


Fig. 5-12. Baud rate generation logic.

The data selection multiplexer design combines the output of the eight 8:4 multiplexer devices to form one register word. To select a Utility Board register, the address of the register appears on the multiplexer output and is asserted on the 8560 bus through the bus drivers/receivers. Register "don't-care" bits are not multiplexed and arrive on the bus as zero.

U2060 and U3060 are two 4:1 multiplexers that multiplex Line-Time Clock Register data.

Data Selection Line Encoder ◇5◇

Line encoder U2120 generates three data select signals that select the output of the data selection multiplexer. The three signals, SELA(L), SELB(L), and SELC(L), appear at multiplexer inputs pins 11, 10, and 9, respectively. At the appropriate time, the bus driver/receiver logic asserts the multiplexer output data onto the 8560 bus.

BUS DRIVER/RECEIVER LOGIC ◇7◇ ◇8◇

The bus driver/receiver logic interfaces the Utility Board with the 8560 bus. For this discussion, the bus driver/receiver is divided into the data/address transceiver and the control line transceiver.

Data/Address Transceiver ◇7◇

The data/address transceiver consists of four 8838 quad bus transceiver devices (U6080, U6090, U7070, and U7090). These devices are bidirectional. Data and address information can be written to or read from the 8560 data bus providing transmit and receive capability for four signal lines.

Control Line Transceiver 7 8

The control line transceiver logic provides correct load impedance and drive levels to signals coming from or going to the 8560 bus. The control transceiver is similar in operation to the data address transceiver logic. However, it operates on control signals rather than on data and address signals. The control line transceiver consists of three 8838 quad bus transceiver devices (U6070, U7040, and U7050).

Bus Termination Resistors 7 8

Since the Utility Board is the last board on the 8560 bus, all bus signals are terminated here with a resistive divider network. This consists of 180 ohms to +5 Vdc and 390 ohms to ground. DMA grant (DMGI(L)) and interrupt acknowledge (IAKI(H)) signals are terminated with a resistive divider network consisting of 330 ohms to +5 Vdc and 680 ohms to ground.

LINE-TIME CLOCK (LTC) LOGIC 6

The Line-Time Clock logic consists of the clock circuit, LTC Status Register address logic and supporting logic.

Line-Time Clock (LTC) Circuit

The Line-Time clock (LTC) is used by the LSI-11 for real-time functions. The LTC is also used by the power-up test that checks if the unit is connected to the correct line voltage frequency and by the 8560 disk-based diagnostics. The LTC circuit consists of flip-flops U1030B and gates U1010D and U4010D. The line-time clock circuit is driven by FR(H), a 5 V p-p 60 Hz or 50 Hz square wave originating at the 8560 power supply.

LTC Status Register Address Logic

U7100 and U5110 form the LTC Status Register address. Data address lines DAL3(H) and DAL6(H) through DAL12(H) are ANDed with BS7(H). BS7(H), an LSI-11 signal, is asserted any time the top 8K bytes of addressable memory space are accessed. When the 8560 bus contains an address, pin 9 of U7100 goes low and is ANDed with pins 9 and 10 of U7121. The output of NAND gate U5100 is then latched into U5070 by an asserted SYNC(H) signal. LTC(H) generates LTC read and write signals, RD-LTCR(L) and LD-LTCR(L), which enable the LTC Status Register during the read and write cycle, respectively. An LTC handshake signal (LTC(L)) is asserted after any read or write cycle.

Figure 5-13 shows the LTC Status Register, and Table 5-7 describes individual register bits and their functions. The LTC address is 17777546 or 17777520.

Table 5-7
The LTC Status Register

Bit No.	Function	Description
0	read/write	Bit 0 identifies a strap-selected logic level for diagnostic steering. The condition of this bit depends on the Maintenance Jumper (P1036).
1-4	read-only	These bits are not used (set to zero).
6	read/write	When bit 6 is a 1, the line frequency clock signal asserts the EVENT(H) signal. Bit 6 is cleared by INIT(H).
5, 7	read/write	Bits 5 and 7 are set by INIT(H) and determine which bank of the diagnostic/bootstrap ROMs is accessed.
8-10	read-only	These bits are not used (set to zero).
11	read/write	This bit performs two functions. Bit 11 is the LSB of the diagnostic LEDs and also determines which bank of the diagnostic/bootstrap ROMs is accessed.
11-15	write-only	Bits 11-15 are used by the power-up test to indicate error conditions. Writing a 0 to a bit turns on its associated LED. Writing a 1 turns the LED off. The initialize condition sets all LEDs.

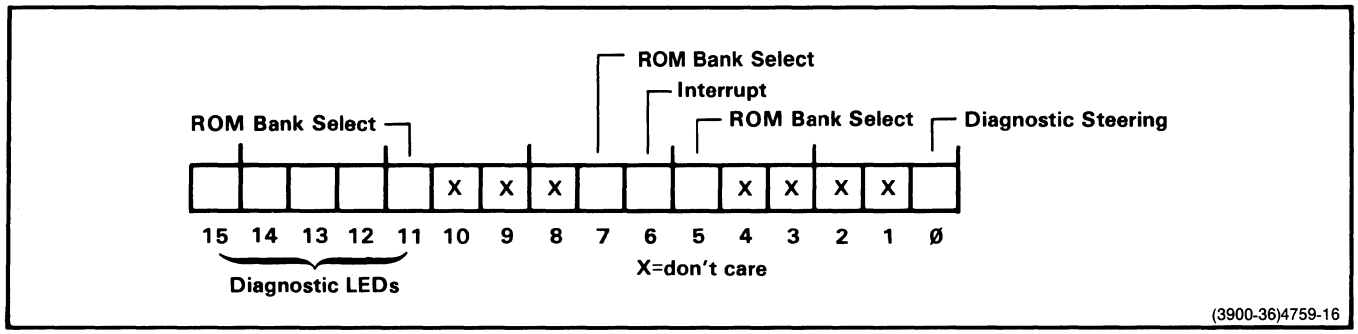


Fig. 5-13. The LTC Status Register.

Supporting Logic

Latch U1020, a hex flip-flop device, is the supporting logic for bank selection and diagnostic LEDs. U1020 uses five of its outputs to drive LEDs DS1021 through DS1032. The remaining output, 6Q, selects the proper bank of the diagnostic ROM. Latch U1020 is loaded any time the LTC Status Register is addressed.

POWER CONTROL CIRCUIT 8

The Power Control Circuit consists of voltage level comparator logic, and power-up/power-down logic. The following paragraphs explain these circuits and describe the 8560 power-up sequence.

Voltage Level Comparator Logic 8

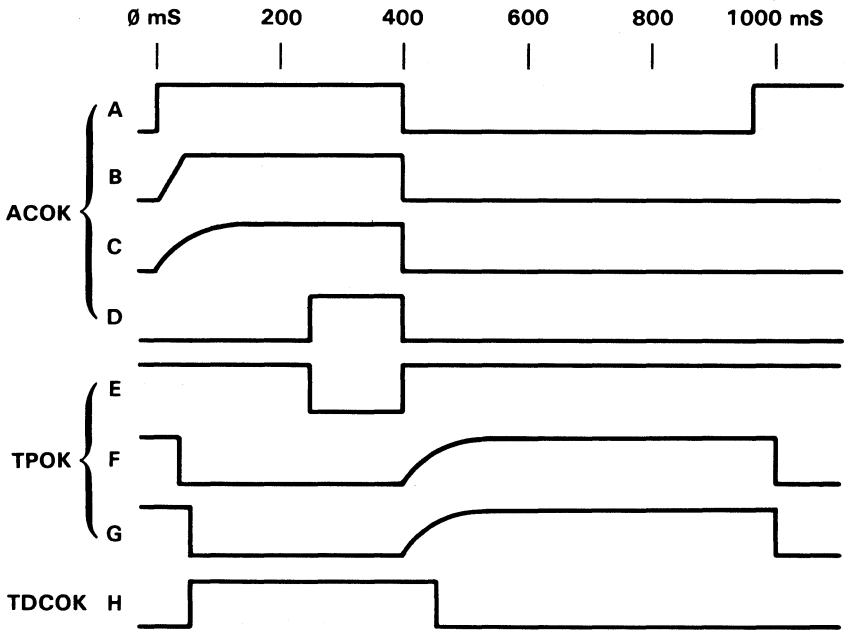
Voltage comparator U5030 consists of three comparators in one package. These comparators monitor the +12 V, -12 V, and +5 V voltages, ensuring that they maintain their proper level.

When the power supply asserts ACOK(H) and the three voltages are within operating range, pin 11 of U6040E goes high. This permits DCOK(L) and TPOK(L) to be asserted, and the LSI-11 starts to run.

Power-Up/Power-Down Circuit 8

The power-up/power-down circuit consists of U4030 and U5030 and associated logic. The power-down sequence ensures that proper shut-down procedures are followed during a power failure.

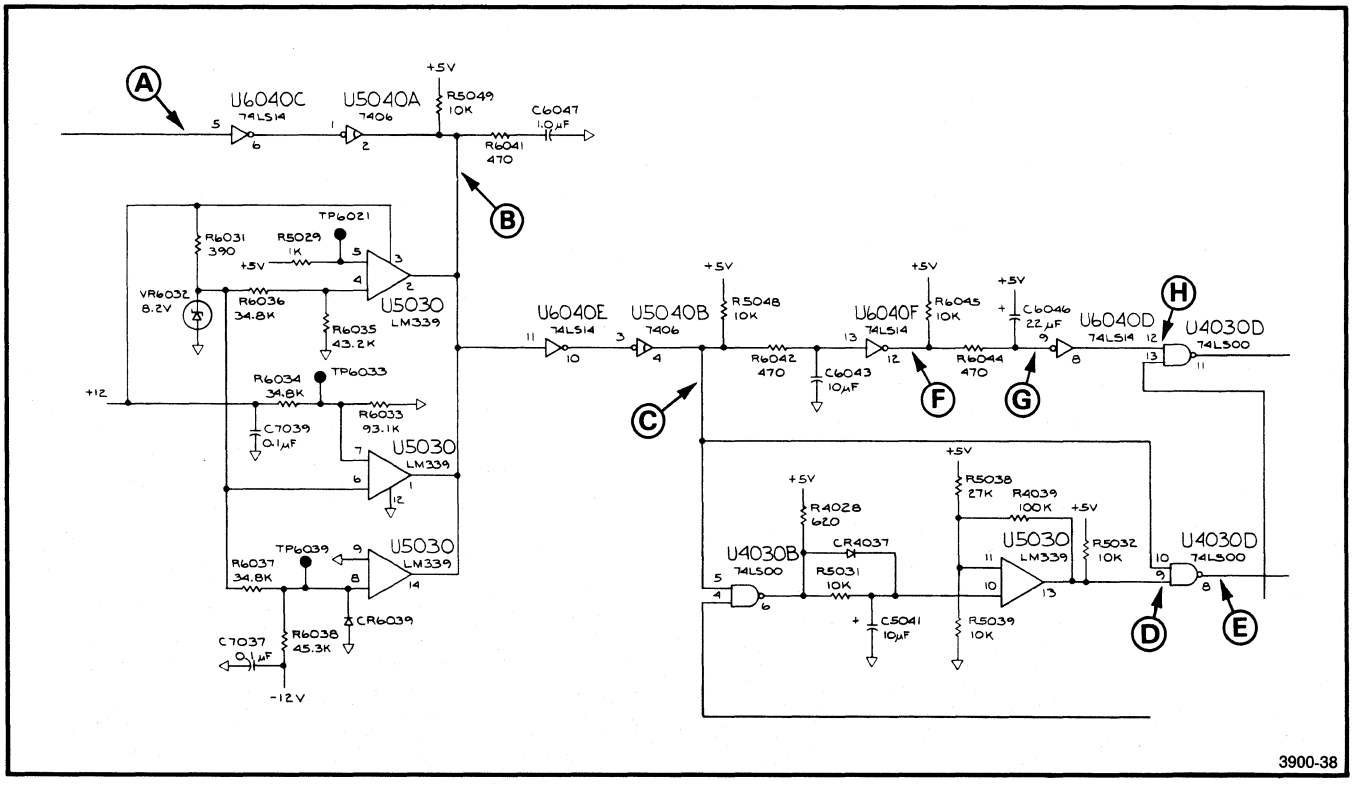
Figure 5-14 shows a timing diagram of the power-up timing sequence. Figure 5-15 identifies the test point locations used in Figure 5-14. Figure 5-16 provides minimum 8560 bus execution times.



Note: Voltages are typical TTL levels.

3900-37

Fig. 5-14. Power-up timing diagram.



3900-38

Fig. 5-15. Power-up/power-down logic.

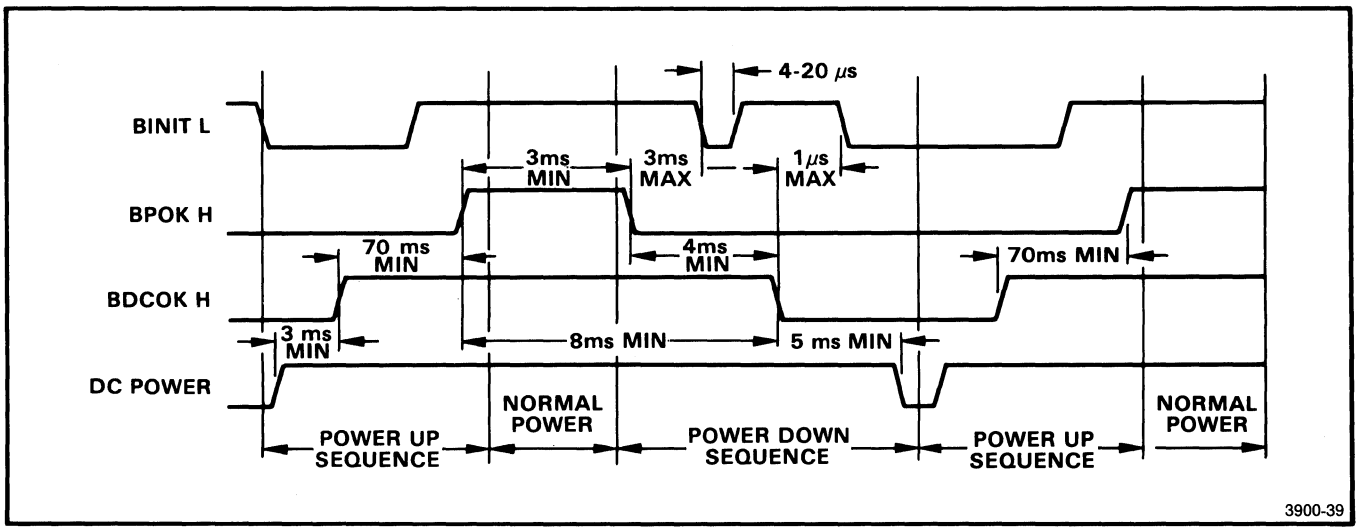


Fig. 5-16. 8560 bus timing limits.

Power-Up Sequence

When the front panel DC ON/OFF switch is turned on, the following power-up sequence occurs:

1. Initially, both the DCOK(L) (dc voltage OK) and ACOC(L) (Power OK) signals are high.
2. When the LSI-11 processor dc voltages are normal, the LSI-11 initializes the bus by asserting INIT(H). This also clears every device in the system.
3. Approximately 40 ms after the +5 V reference voltage, the +12 V and -12 V supplies have been received by the Utility Board and are stable. The Utility Board then asserts DCOK(L).
4. The processor responds by negating INIT(H).
5. Approximately 220 ms after asserting DCOK(L), the Utility Board asserts ACOK(L).
6. The processor responds by executing the user-selected power-up diagnostics, followed by the bootstrap routine.

FRONT PANEL CONTROL ◇8

The Utility Board front panel control logic provides the 8560 with HALT and RESTART capability. The front panel control logic consists of flip-flops U5050 and U5060 and associated logic.

The Utility Board controls the 8560 system restart operation. When the front panel RESTART switch is toggled, the BDCOK(H) signal goes low and the processor starts execution at octal address 17777300.

When the front panel RUN/HALT switch is in the HALT position, pin 10 of U3040B goes high, asserting the bus HALT(L) signal. The LSI-11 halts after the current instruction is executed.

Front panel controls and indicators connect to the Utility Board. The Utility Board generates a DMA request on receipt of a restart signal. On receipt of a bus grant, or after 150 ms have elapsed, DCOK(L) is asserted. The Utility Board also generates a processor-busy (PROC-BUSY(L)) signal from the RUN line and connects the BRUN(L) signal to front panel LEDs.

DIAGNOSTIC/BOOTSTRAP ROM ◇6

U5080 and U5090 provide read-only memory storage for boot instructions and power-up diagnostics. These devices contain 4K words of diagnostic and bootstrap memory at octal addresses 17773000 through 17774776. The ROM is divided into four banks. Figure 5-17 shows the memory bank division. Bits 5 and 11 of the LTC Status Register determine which bank is addressed. ROM is addressed using address lines A0(H) and A8(H).

When the 8560 is powered-up or reset, the power-up tests in bank zero are executed, followed by the bootstrap routines in bank three. The 8560 initially tries to boot from the flexible disk drive. If it cannot do so, it tries to boot from a hard disk. If the 8560 cannot boot, it repeats the power-up test sequence. Power-up tests are described in Section 13 of this manual.

ROM Bank 0 contains power-up tests for RAM, ROM, and MMU.

ROM Bank 1 contains flexible disk drive alignment service routines, RAM tests, and IOP Board drivers.

ROM Bank 2 contains a command interpreter. This interpreter is executed after the power-up tests if jumper P1036 is open or an error is encountered.

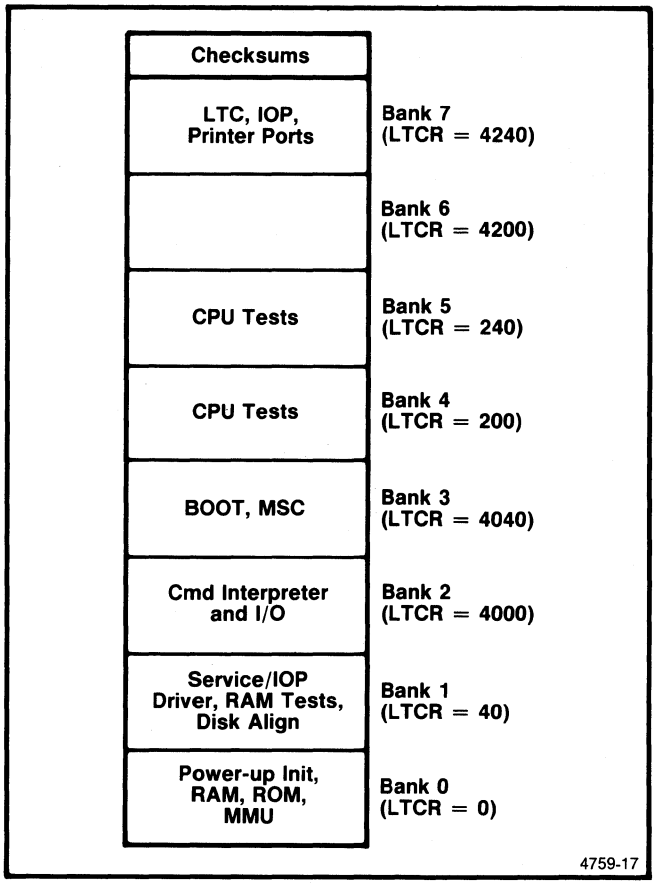


Fig. 5-17. Diagnostic and Bootstrap ROM functions.

ROM Bank 3 contains the bootstrap routine and power-up tests for the MSC.

ROM Bank 4 and ROM Bank 5 contain power-up tests for the CPU.

ROM Bank 6 is not used.

ROM Bank 7 contains power-up tests for the LTC, IOP Boards and printer boards.

Addressing

Bootstrap and diagnostic ROM addresses occupy approximately 512 words of memory between octal locations 17773000 and 17774776.

LTC Status Register bits 5, 7, and 11 enable one 512-word bank and disable all others, thus allocating the specified address space to only one bank at a time.

Each bank requires a total address space of 512 words. Therefore, individual banks share the same address space. Banks are selected by LTC Status Register bits 5, 7, and 11, which control address lines A9, A10, and A11, respectively. These bits are cleared automatically at power-up or restart. Execution of the 8560 power-up tests begins in Bank 0.

Diagnostic Error Indicators (LEDs)

Table 5-8 shows the diagnostic error indicator sequence. The LEDs are visible (from the side opposite the drives) when the 8560 top cover is removed. The LED closest to the front is the most significant bit.

If the 8560 is powered up, the sequence is completed in approximately 30 seconds. If the 8560 is reset, the sequence is completed in less than 20 seconds.

Table 5-8
LED Error Codes

LEDs	Octal Value	Definition
*****[a]	37	Unable to execute firmware
-----	00	LTC error
----*	01	Initialization error
---*-	02	Printer Port 2 error
---**	03	LSI-11 MMU error
--*--	04	Printer Port 1 error
--*-*	05	ROM error (low byte)
--**-	06	MSC error
--***	07	ROM error (high byte)
-*---	10	Page 0 RAM error
-*--*	11	Page 0 RAM error
-*-*-	12	Page 1 RAM error
-*-**	13	Page 1 RAM error
-**--	14	Page 2 RAM error
-**-*	15	Page 2 RAM error
-***-	16	Page 3 RAM error
-****	17	Page 3 RAM error
*----	20	Page 0 RAM parity fault
---	21	Page 0 RAM parity fault
---	22	Page 1 RAM parity fault
*--**	23	Page 1 RAM parity fault
---	24	Page 2 RAM parity fault
--*	25	Page 2 RAM parity fault
*-**-	26	Page 3 RAM parity fault
*-***	27	Page 3 RAM parity fault
**---	30	IOP error
**--*	31	LSI-11 CPU error
**-*-	32	Trying to boot from a flexible disk
-	33	Not used
***--	34	Debugging mode
***-*	35	Debugging mode
****-	36	Executing secondary boot from disk
*****	37	TNIX running

[a] **The dash represents an unlit LED. The asterisk represents a lit LED.**

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SYSTEM MEMORY

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Section 6

SYSTEM MEMORY

INTRODUCTION

This section describes the system memory board(s) used in the 8560 Series MUSDUs.

A 256K Memory Board is the standard memory circuit board for both the 8560 and 8561. Two 512K Memory Boards provide the standard 1M byte of system memory for the 8562. Both the 8560 and 8561 can be upgraded from their standard 256K-byte configuration to 512K bytes, 768K bytes or 1M bytes of system memory.

Figure 6-1 provides a block diagram of the system memory boards. Refer to this diagram as you read the following paragraphs.

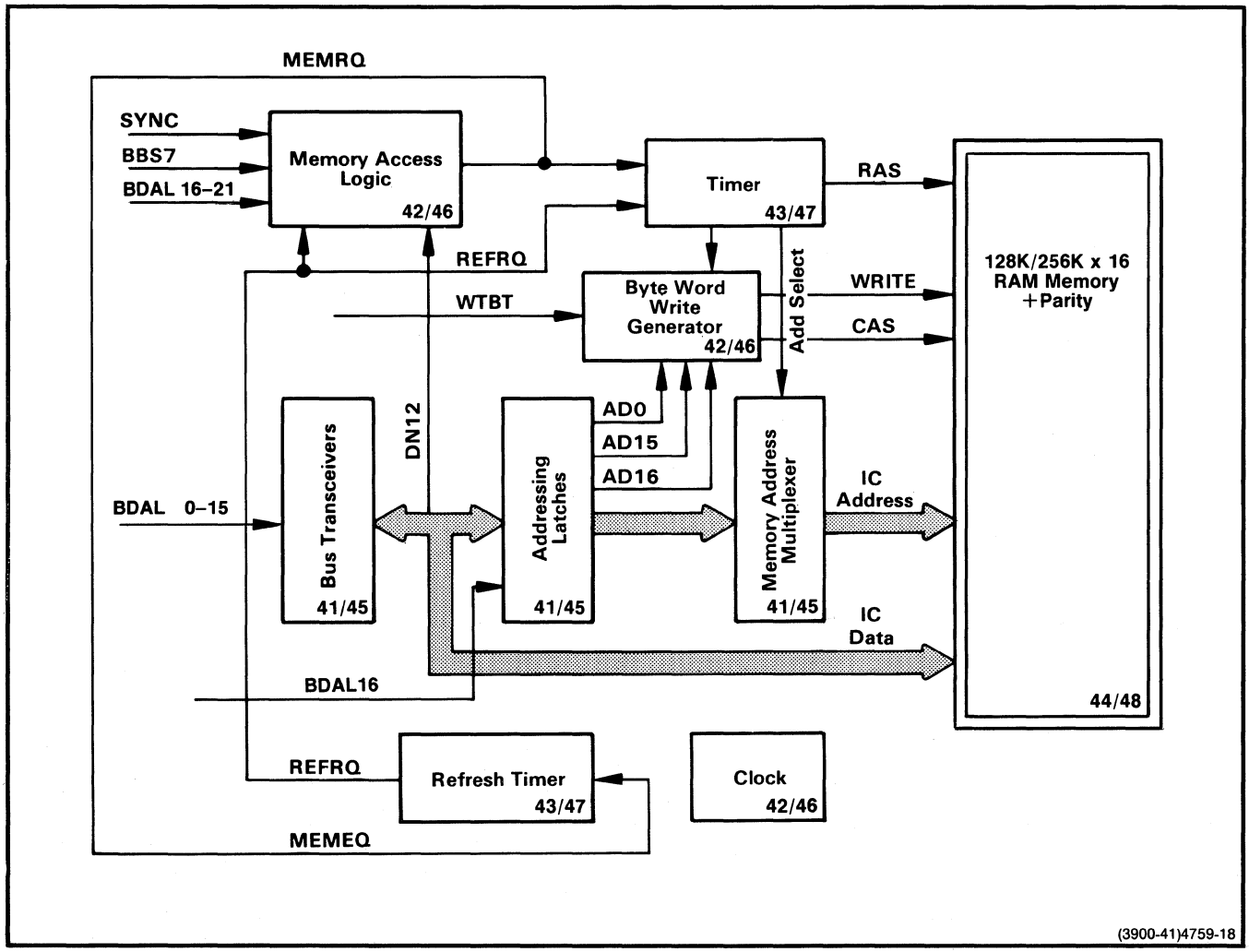

Fig. 6-1. 256K/512K Memory Board block diagram.

256K MEMORY BOARD

The 256K Memory Board provides the standard memory configuration for the 8560 and 8561 MUSDUs. The following paragraphs describe some of the features of this board.

Bus Protocol 

The entire 256K Memory Board is logically structured in two banks of 64K, 16-bit words, plus byte parity. The two banks of memory on a board are differentiated by address bit 17. This bit is used to gate CAS to one of the two banks through a decoder chip (74F139) in the timing circuitry. RAS is transmitted to the two banks with every access, and the write enable signal is sent to all chips if a word-write is in progress.

The interface between memory and the LSI-11 bus is achieved through four AM2908 quad bus transceivers. These chips also generate 4-bit parity. The entire parity generator check for two bytes of data is accomplished by the four transceivers and one 74LS266 exclusive-NOR chip.

The received data lines at BSYNC time contain the lower-order 16 bits of the word address. These lines, as well as address lines BDAL 16 and 17 and BDAL 19 through 21 are sampled at the falling edge of BSYNC. Lines BDAL 1 through 16 are latched in the dynamic-RAM controller chip to form the RAS/CAS address for the memory chips. BVDAL 0 and 17 are latched in a holding register. BDAL 19 through 21 determine which board is to be accessed during the current memory cycle.

The BDAL 18 input to the holding register is grounded, and the BDAL 18 true input inhibits the board address recognition circuitry. The 256K Memory Board responds to addresses from 0 to 256K if it is configured for low-address space and, correspondingly, responds to 512K to 768K addresses if it is configured for high-address space.

Memory Timing 

A 25.00 MHz clock (with a period of 40 nsec) is located on the memory board and provides memory timing. A shift register generates the RAS, Address Select, and CAS signals to the memory.

Bus signal BDOUT generates the WRITE ENABLE, and both BDOUT and BDIN generate BRPLY to the processor. BDIN also configures the bus transceiver chips to allow data from the memory (read) to be placed on the bus by signal ENOUT. The shift register halts at State 6, T5(H) through T6(L), until the fall of BDOUT or BDIN from the processor. T6 is set by this event, and the timing returns to a quiescent state (after a sufficient length of time for RAS to recharge) before another cycle can be initiated.

I/O Space 

Each board is a complete stand-alone memory and can be configured to occupy the lower 256K-byte bank or to occupy memory space of 512K bytes, 768K bytes or 1M bytes of the LSI-11 processor memory.

A read, write, or read-modify-write memory cycle is initiated at BSYNC time unless BBS7 is set to access peripheral units, or bits BDAL 19 through 21 are jumpered to access the optional 512K Memory Board. The board containing the highest addressable portion of memory will be jumpered to respond to the bottom 4K bytes of I/O space. This I/O space will overlay the lower half of the highest 8K bytes of addressable space available.

Only the upper 4K bytes of I/O space will be used to address peripheral units. The response to the bottom 4K-byte space of the system I/O must always be enabled on this board whether it occupies the memory space from 0 to 256K or from 512K to 768K. This board must always occupy the top addressable memory position in the system when it is installed in the 8560 or the 8561.

Address Selection 

The RAS/CAS address select is performed by an AM2964B dynamic memory controller chip. This chip also contains a refresh address counter and logic to gate this counter on the memory address lines during refresh.

Bus lines BWTBT and BDAL0 determine a high/low byte-write sequence at BSYNC time. There is no byte-read from main memory. The read sequence always addresses a full 16-bit word from memory, placing it on the bus. The processor must arbitrate a read-byte access. Byte parity allows the write of one byte per access in memory.

The read-modify-write sequence consists of two full memory cycles. The first cycle is a normal read, but the write cycle is triggered by bus signal BDOUT. BWTBT is low at BSYNC time and MERQ remains high.

Refresh 43

The 128 RAS-only refresh cycles are generated by the countdown of the 25.00 MHz clock generating 128 refresh cycles every 1.6 ms. A memory access is prohibited during a refresh cycle and is delayed until the completion of that refresh. A refresh is prohibited during a memory access and will be delayed until the completion of that memory access. The refresh cycle/memory access cycle requests are sampled by different edges of the memory clock and will not enter a race condition for grant. The time between counter resets is always 13 μs, because within this time, a refresh cycle is always allowed by the falling edge of MERQ. A counter in the address mux chip provides the refresh address count and multiplexing every 13 μs (the refresh cycle).

Jumpers and Straps

The 256K Memory Board provides various jumpers. The low-byte parity-bit memory may be completely swapped with bit-0 memory, and the high-byte parity-bit memory may be completely swapped with bit-8 memory. This memory swapping allows you to test all memory chips (including parity) on the board. Jumpers are provided which disable clock, parity, and refresh operations during diagnostic execution. See Section 3 for default jumpering of the 256K Memory Board.

512K MEMORY BOARD

The 512K Memory Board provides the standard 1M bytes of system memory for the 8562, as well as an optional upgrade for the 8560 and 8561. The following paragraphs provide some of the features of the board.

Bus Protocol 46

The entire 512K Memory Board is logically structured in four banks of 64K, 16-bit words, plus byte parity. The four banks of memory on a board are differentiated by address bits 17 and 18. These address bits are used to gate CAS to one of the four banks through a decoder chip (74F139) in the timing circuitry. RAS is transmitted to the four banks with every access, and the write enable signal is sent to all chips if a word-write cycle is in progress.

The memory interfaces to the LSI-11 bus through four AM2908 quad bus transceivers. These chips also generate 4-bit parity. The entire parity generator check for two bytes of data is accomplished by the four transceivers and one 74LS266 exclusive-NOR chip.

The received data lines at BSYNC time contain the lower order 16 bits of the word address. These lines, as well as address lines BDAL 16 through 21, are sampled at the falling edge of BSYNC. Lines BDAL 1 through 16 are latched in the dynamic RAM controller chip to form the RAS/CAS address for the memory chips. BDAL lines 0, 17 and 18, are latched in a holding register. BDAL, lines 19 through 21, determine which board is to be accessed during the current memory cycle.

Memory Timing 47

A 25.00 MHz clock (with a period of 40 nsec), located on the memory board, provides memory timing. A shift register generates the RAS, Address Select, and CAS signals to the memory.

Bus signal BDOUT generates the WRITE ENABLE, and both BDOUT and BDIN generate BRPLY to the processor. BDIN also configures the AM2908 bus transceiver chips to allow data from the memory (read) to be placed on the bus by signal ENOUT. The shift register halts at State 6, T5(H) through T6(L), until the fall of BDOUT or BDIN from the processor. T6 is set by this event. The timing returns to a quiescent state (after a sufficient length of time for RAS to recharge) before another cycle can be initiated.

I/O Space 46

Each board is a complete stand-alone memory. Each board contains the requisite jumper option to configure it as either the upper or lower 512K-byte bank of the LSI-11 processor memory in the 8560 Series system.

A read, write, or read-modify-write memory cycle is initiated at BSYNC time unless BBS7 is set to access peripheral units, or bits BDAL 19 through 21 are jumpered to access the 512K Memory Board. The board containing the highest addressable portion of memory is jumpered to respond to the bottom 4K bytes of I/O space. This I/O space overlays the lower half of the highest 8K bytes of addressable space available. Only the upper 4K bytes of I/O space is used to address peripheral units.

Address Selection (45)

The RAS/CAS address select is performed by an AM2964B dynamic memory controller chip. This chip also contains a refresh address counter and logic to gate this counter on the memory address lines during refresh.

Bus lines BWTBT and BDAL0 determine a high/low byte-write sequence at BSYNC time. There is no byte-read from main memory. The read sequence always addresses a full 16-bit word from memory, placing it on the bus. The processor must arbitrate a byte-read access. Byte parity allows the write of one byte per access in memory.

The read-modify-write sequence consists of two full memory cycles. The first cycle is a normal read. However, the write cycle is triggered by bus signal BDOUT, BWTBT having been low at BSYNC time and MERQ remaining high.

Refresh (47)

The 128 RAS-only refresh cycles are generated by the countdown of the 25.00 MHz clock generating 128 refresh cycles every 1.6 ms. A memory access is prohibited during a refresh cycle and is delayed until the completion of that refresh. A refresh is prohibited during a memory access and will be delayed until the completion of that memory access. The refresh cycle/memory access cycle requests are sampled by different edges of the memory clock and will not enter a race condition for grant. The time between counter resets is always 13 μs because within this time, a refresh cycle will always be allowed by the falling edge of MERQ. A counter in the address mux chip provides the refresh address count and multiplexing every 13 μs (the refresh cycle).

Jumpers and Straps

The 512K Memory Board provides various jumpers. The low-byte parity-bit memory may be completely swapped with bit-0 memory and the high-byte parity-bit memory may be swapped with bit-8 memory. This allows the testing of all memory chips (including parity) on the board. Jumpers are provided which disable clock, parity, and refresh operations during diagnostic execution.

The state diagrams in Table 6-1 define the system RAS/CAS generation for 256K and 512K Memory Boards.

See Section 3 of this manual for default jumpering of the 512K Memory Board.

Table 6-1
State Diagrams for 256K and 512K Memory Boards

STATE	T 0	T 1	T 2	T 3	T 4	T 5	T 6	EVENT	SIGNAL
0	0	0	0	0	0	0	0	MERQ(H). GO(L)	RAS Address Enabled
1	1	0	0	0	0	0	0	T0(H)	RAS(L)
2	1	1	0	0	0	0	0	T1(H)	—
3	1	1	1	0	0	0	0	T2(H)	CAS Address Enabled
4	1	1	1	1	0	0	0	T3(H)	CAS(L)
5	1	1	1	1	1	0	0	T4(H)	ENOUT(L) if RDIN(H)
6	1	1	1	1	1	1	0	T5(H)	(Wait state)
7	1	1	1	1	1	1	1	TRPLY(L)	(End of cycle), T6(H)
8	0	1	1	1	1	1	1	T0(L)	—
9	0	0	1	1	1	1	0	T1(L)	T6(L)
10	0	0	0	1	1	1	0	T2(L)	RAS(H)
11	0	0	0	0	1	1	0	T3(L)	CAS(H) . ENOUT(H)
12	0	0	0	0	0	1	0	T4(L)	GO(L) . MERQ(L)
0	0	0	0	0	0	0	0	T5(L)	—

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THE I/O PROCESSOR

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Section 7

THE I/O PROCESSOR

INTRODUCTION

This section describes the I/O Processor (IOP) Board hardware and its functions. Section 3 of this manual provides information for the default jumpering/strapping of the IOP Board. IOP diagnostics are described in Sections 13 and 16.

The IOP Board is a microprocessor-controlled communications board that controls the information flow to and from 8560 external peripherals. The IOP Board relieves the LSI-11 of most I/O processing chores associated with external 8560 peripheral communications. Figure 7-1 is a block diagram of the IOP Board.

IOP Board logic is composed of the following parts:

- The kernel
- System memory access logic
- I/O logic
- Interrupt vector logic
- Diagnostic registers

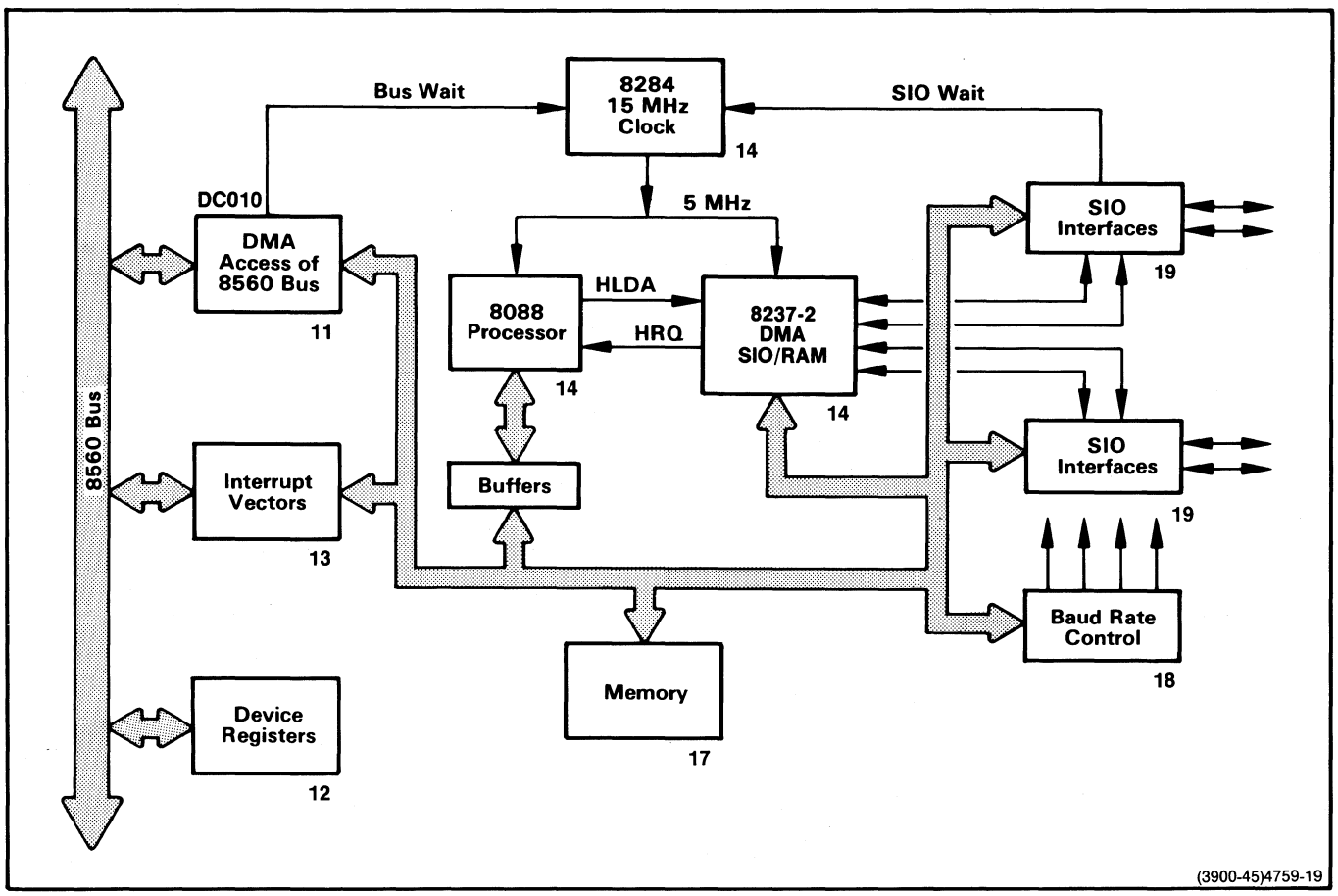

Fig. 7-1. I/O Processor block diagram.

The IOP **kernel** consists of an 8088 microprocessor (U3050), a clock circuit, 10K bytes of RAM and 20K bytes of ROM.

The **system memory access logic** provides memory mapping and direct memory access functions. The 8088 accesses the 8560 bus by treating it as a subset of its address bus.

The **I/O logic** provides up to eight full-duplex serial data channels, I/O registers, SIO wait logic and a baud rate generator, contained on up to two IOP Boards.

Interrupt vector logic provides two vector ports that interface with the LSI-11 through interrupt vector registers. The 8088 sets 8560 bus interrupts under firmware control.

The IOP provides two **diagnostic registers**: a write-only register, and a read-only register. The output of the write-only register drives a seven-segment LED display.

THE KERNEL

The kernel is defined as the part of the IOP Board that must be operational before any firmware or software diagnostics can be executed. The kernel includes the 8088 processor (U3050), the clock, and the ROM and RAM memories.

The Processor 

The heart of the IOP Board is an Intel 8088 microprocessor strapped for min mode and capable of addressing one megabytes of memory.

The 8088 has an 8-bit external data path to memory and I/O space and a 16-bit wide internal data bus. The 8088 contains an Execution Unit (EU) and a Bus Interface Unit (BIU). The EU executes instructions, and the BIU fetches instructions, reads operands and writes results. The EU and BIU operate independently, and generally, instruction-fetch operations can overlap with instruction executions. Because the processor does not need to stop while an instruction is fetched, the overall fetch-execution time is reduced. Instructions for the 8088 processor are stored in on-board RAMs.

The Clock Circuit 

An 8284A clock generator/driver device (U3160) supplies the master clock signal for the 8088. In addition to supplying the primary CPU clock signal, the 8284A provides a hardware reset function and a mechanism to insert bus cycle wait states.

The 8284A Clock Generator device uses an external crystal oscillating at 15 MHz. From this frequency, U3160 generates a 15 MHz, 5 MHz and 2.5 MHz output. The 2.5 MHz output is not used. The 7.5 MHz clock drives the DEC DC010 8560 bus DMA device (U6080). The 3.75 MHz clock output drives the SIO devices.

The clock logic also has an internal Schmitt trigger circuit that provides a hardware reset function. This circuit is asserted from the 8284A's RESET input. When the RESET input is high, the RESET output is asserted synchronously with the CLK signal for four clock cycles. This causes the CPU to fetch and execute the instruction at location FFFF.

IOP Memory Allocation and Assignments

The IOP Board provides 10K bytes of RAM. In addition, the 8088 can access the 8560 system memory. The 20K bytes of ROM on the IOP Board contain the 8088 operating firmware and various IOP service routines. Figure 7-2 shows the 8088 address space, which is divided into four quarters.

The bottom quarter (address 00000 to 3FFFF) is reserved for on-board RAM and control/status registers.

The next quarter (addresses 40000 to 7FFFF) maps the 8560 bus I/O space for direct use by the 8088.

The next highest quarter (addresses 80000 to BFFFF) is used to map the 8560 system memory into the 8088 memory space.

The top quarter (addresses C0000 to FFFFF) is designated for on-board PROM and ROM memory.

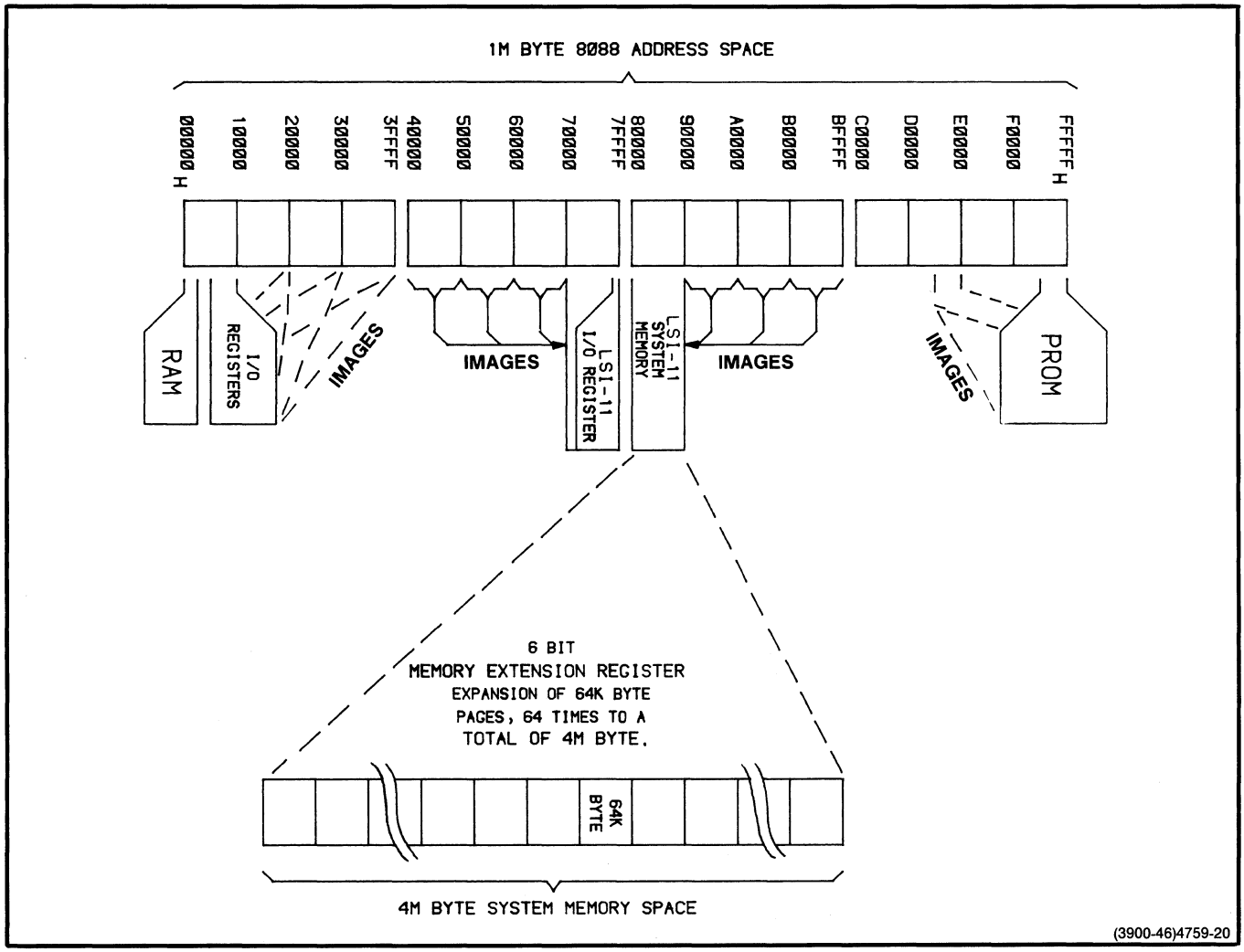

Fig. 7-2. 8088 memory map.

Figure 7-3 shows the 8088 memory space hardware decoding. All I/O registers are located in the 8088 memory space. The diagnostic registers, however, reside in I/O space. Except for the DMA controller (U3060), all least significant bits are "don't-care" bits.

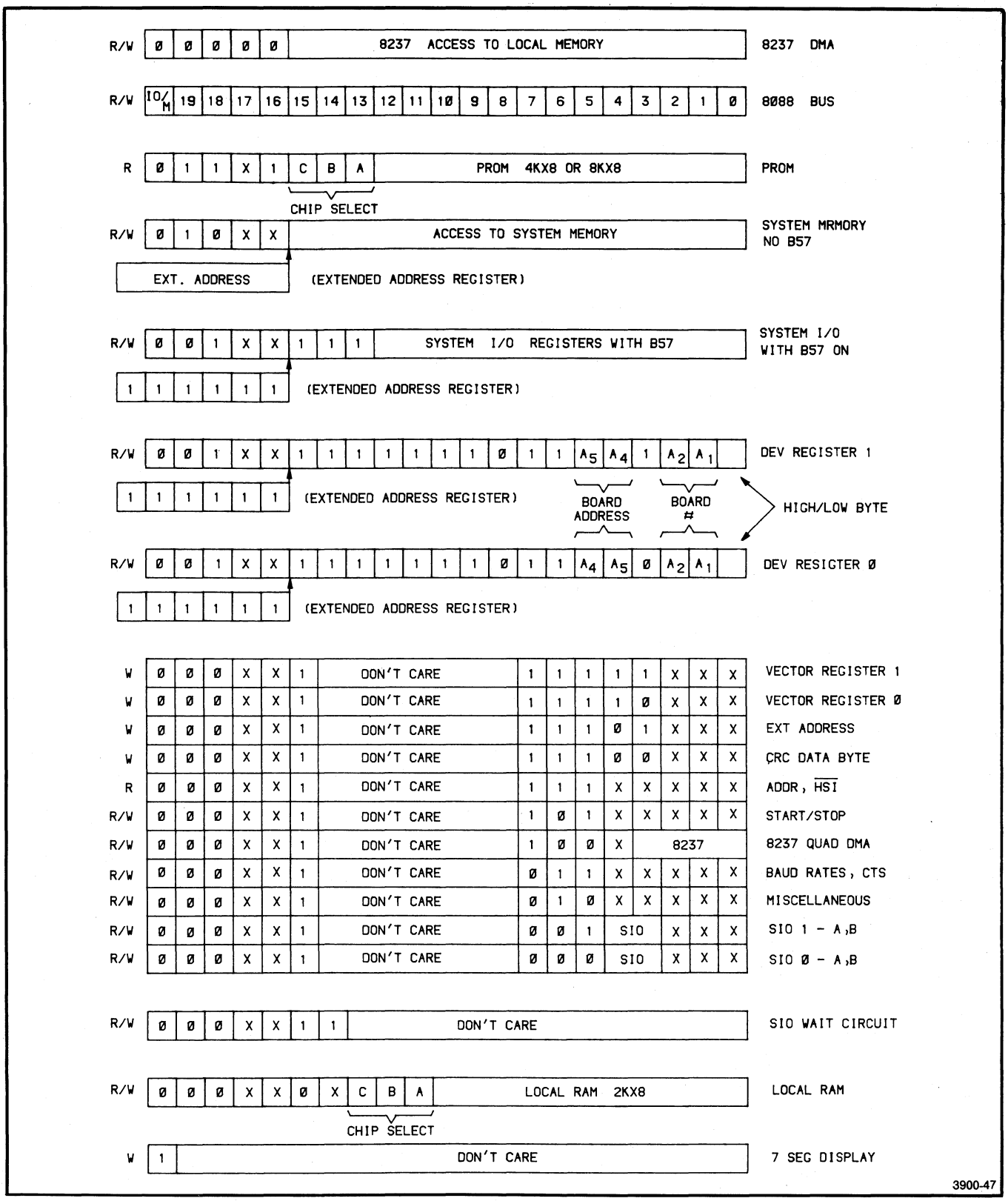

Fig. 7-3. 8088 memory hardware decoding.

SYSTEM MEMORY ACCESS LOGIC

The system memory access logic consists of DMA control circuits and various registers and buffers.

Memory Mapping

Memory mapping is a technique by which a processor can access memory space with a given number of address lines. The 8088 has 20 address lines which allow direct addressing of 1M bytes of RAM.

The 8560 bus, however, provides 22 address lines. Because the 8088 has only 20 address lines, the 8088 can only map a subset of the 8560 system memory. However, a 6-bit address extension register allows the 8088 to address up to 4M bytes of system memory. A memory extension register acts as a bank switch for a 64K-byte memory partition. This register is called the Extended Memory Address Register.

DMA Control Circuit 

The 8560 bus DMA logic allows the 8088 to access address locations that are normally accessed by the LSI-11. The 8560 bus DMA logic consists of a DEC DCO1O device (U6080) and its associated logic. The 8560 bus DMA controller is managed by the 8088 and provides direct access to the system memory.

Bit 7 of the Miscellaneous Register determines whether a system memory data transfer is in word mode or in byte mode. With bit 7 set, all data transfers through the 8560 bus are in byte mode. If bit 7 is cleared, all data transfers through the 8560 bus are in word mode.

Figure 7-4 shows the timing relationship between the 8560 bus and the 8088. When the 8088 accesses the 8560 bus, the DMA circuit signals the 8284 baud rate generator to extend the 8088's read or write cycle. The 8088 clock logic receives a signal instructing it to wait, and the 8560 bus receives a request for bus mastership. When the request is granted, the timing progresses until either the DIN(L) or DOUT(L) signal goes low. The DMA logic then waits for the accessed device to return a reply. When the reply is received, the DMA logic completes its timing and negates the WAIT signal allowing the 8088 to complete its read or write cycle. If a reply is not detected before the one-shot U6170 times out, bit 6 in the Miscellaneous Register is set to indicate an error condition, and U6080 is allowed to terminate the DIN or DOUT cycle.

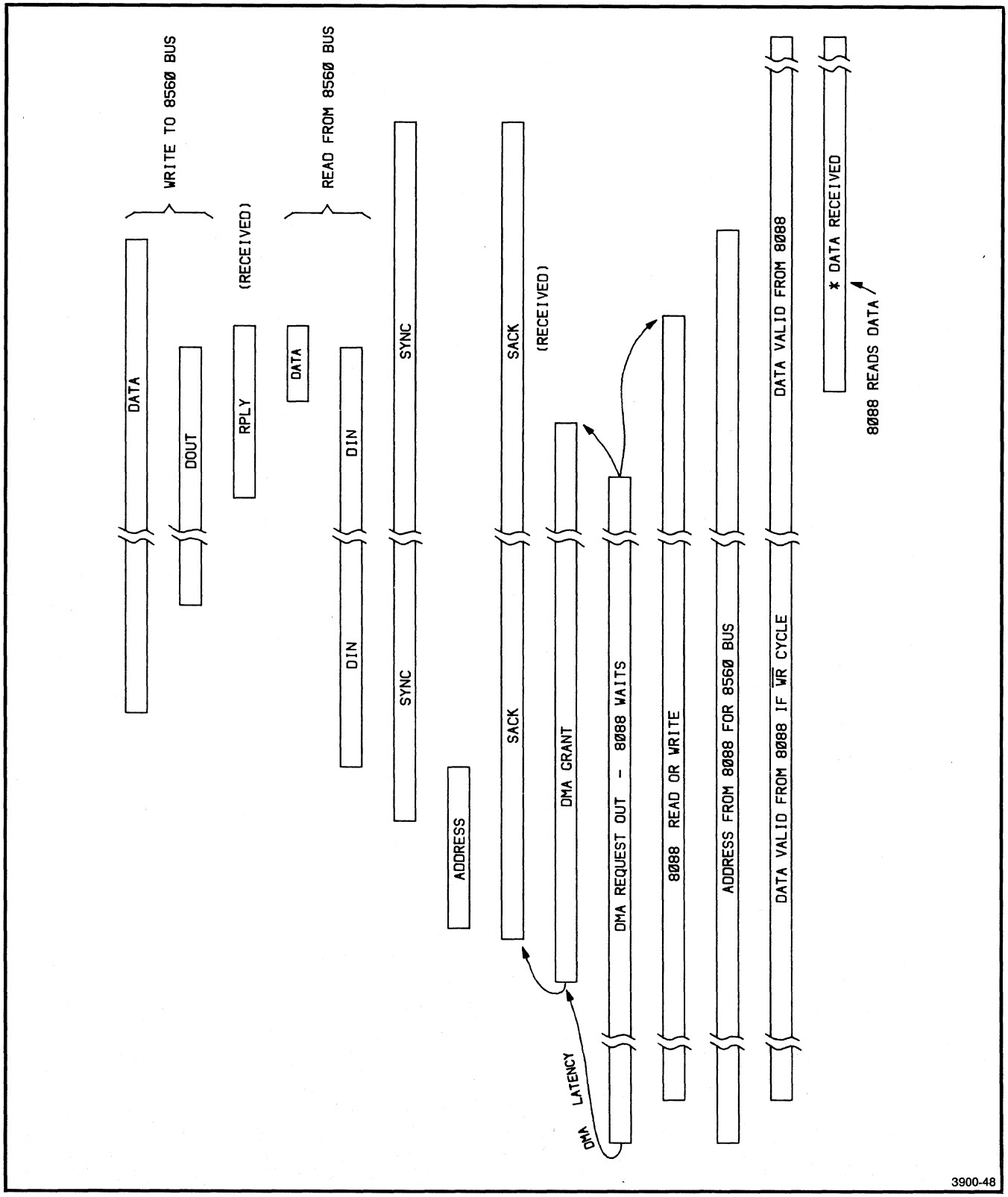

Fig. 7-4. System bus access timing.

Registers

The system memory access registers include the Extended Memory Addressing Register, device registers for HSI terminal functions, 8560 bus registers and buffers, and a register that performs miscellaneous functions.

Extended Memory Address Register 12

The Extended Memory Address Register is a 6-bit register that is used to extend the 16-bit portion of the 8088 bus to address the 22-bit 8560 bus. The contents of this register determine which 64K-byte bank the 8088 can access. Fig. 7-5 shows the Extended Memory Address Register format.

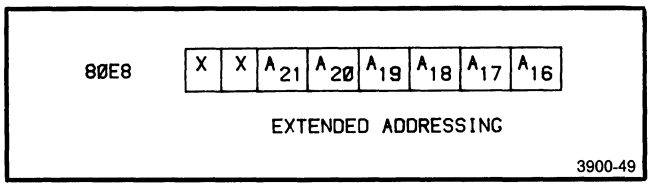

Fig. 7-5. Extended Memory Address Register format.

Any device on the 8560 bus, such as the LSI-11 or the IOP, can access (read and write) these registers. Data is normally written into the registers by the LSI-11, and read back by the 8088 on the IOP Board using its memory-mapped 8560 bus access. Figure 7-6 shows the format of the device registers.

Device Registers 12

The IOP has two 16-bit device registers. Device Register 1 (U6020 and U6040) is designated for HSI functions. Device Register 0 (U6010 and U6030) is designated for terminal functions.

System Bus Registers and Buffers 10 11

Four groups of hardware registers and buffers are used to transfer data to and from the 8560 bus. These registers are described in the following paragraphs:

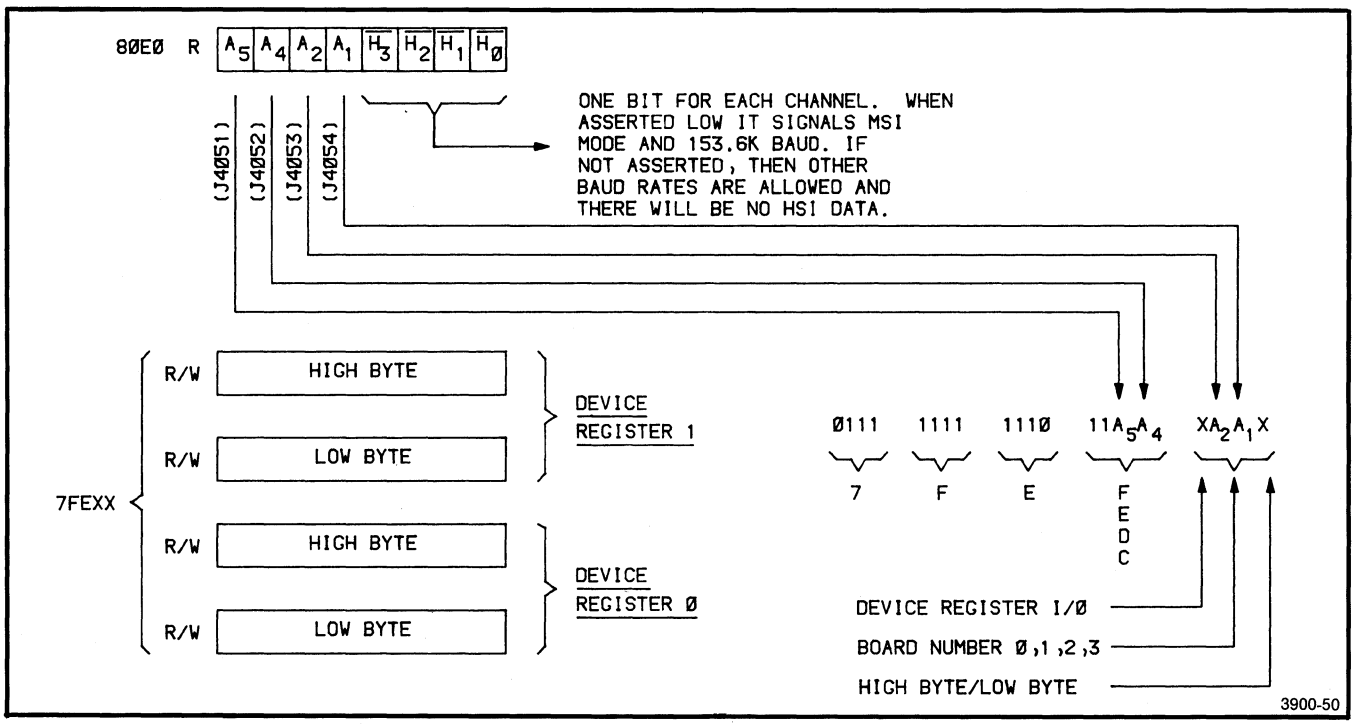

Fig. 7-6. Device Register format.

Registers U7080 and U7090 are the 8560 bus protocol buffers. These two registers work in conjunction with the DEC DC010 8560 bus DMA controller.

The 8560 bus address/data I/O buffers consist of U7010, U7020, U7030, and U7040. These devices are open-collector driven to assert data on the system bus. They also contain a Schmitt bus receiver to receive data from the 8560 bus.

Registers U4020 and U4040 provide addresses for the 8560 bus.

Registers U5010, U5020, U5030, and U5040 are SIO registers that provide data-in and data-out functions. Registers U5020 and U5040 latch the data from the 8088 bus and transfer it to the 8560 bus through buffers U7010, U7020, U7030, and U7040. Registers U5010 and U5030 receive the data from the 8560 bus buffers and latch it before it is transmitted onto the 8088 bus.

Miscellaneous Register 16

The Miscellaneous Register (U6060) located at address 8040H provides various control and status functions. Figure 7-7 shows the register format.

The following paragraphs describe the functions of each bit.

Bit 0—Device Register 0 Loaded. When an 8560 bus master, such as the LSI-11, writes to Device Register 0, this bit is set. When the 8088 finds this bit set, it takes appropriate action and then clears the bit.

Bit 1—Device Register 1 Loaded. This bit is set when an 8560 bus master writes to Device Register 1. When the 8088 finds this bit set, the processor takes the appropriate action and then clears the bit.

Bit 2—Vector 0 Busy. This bit is set when the 8088 writes to the 8560 bus Vector 0 Register. When the LSI-11 responds with the proper interrupt grant, and the IOP intercepts the grant, bit 2 is cleared. As long as the interrupt is pending, bit D2 is read as a 1.

Bit 3—Vector 1 Busy. This bit is set when the 8088 writes to the 8560 bus Vector 1 Register. When the LSI-11 responds with the proper interrupt grant, and the IOP intercepts the interrupt, this bit is cleared. As long as the interrupt is pending, the D3 bit is read as a 1.

Bit 4—Line Frequency. The information in this bit is a square wave of the ac line frequency and has a TTL-level amplitude. A firmware timing loop samples this bit to determine whether the 8560 is connected to a 50 Hz or 60 Hz power line.

Bit 5—This bit is not used.

Bit 6—8560 Bus Timeout Error R/W. Normally this bit is cleared. However, when the 8088 accesses the 8560 bus at an invalid address, a timeout occurs, this error bit is set and the 8560 bus cycle is completed. The 8088 then polls this bit, takes appropriate action, and clears the bit.

Bit 7—8560 Bus Word/Byte Mode. If bit D7 is set, a byte mode bus cycle is generated and the 8560 bus is accessed. A write cycle exercises the 8560 bus BWTBT signal.

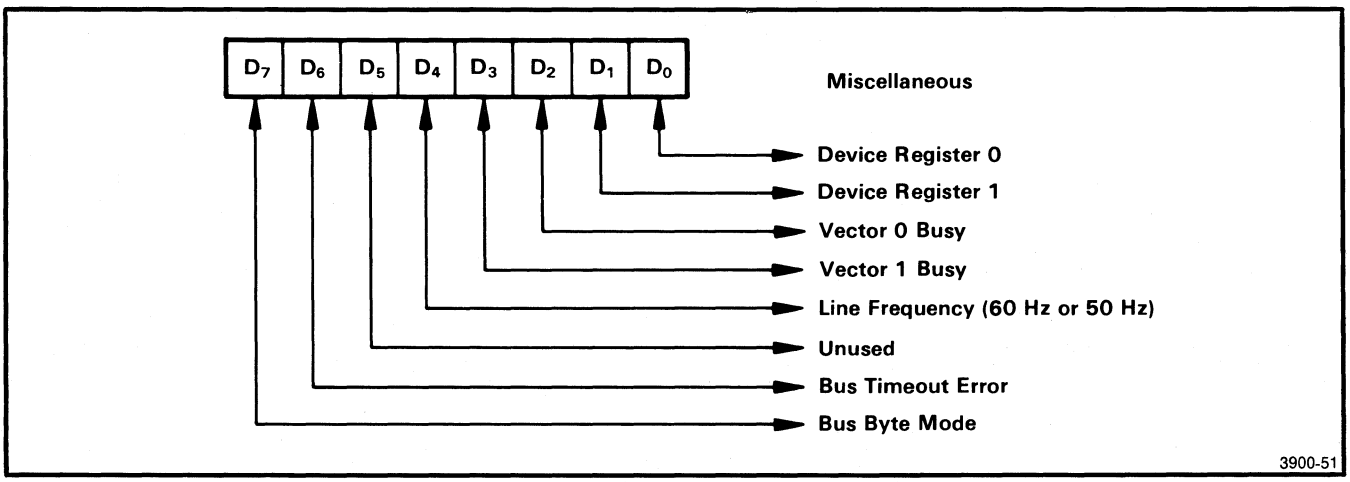

Fig. 7-7. Miscellaneous Register.

If bit D7 is cleared, the 8088 assumes word mode. The information contained in the even-numbered address (low byte) is temporarily stored in a latch. No bus cycle is generated. Writing an odd-numbered address (high byte) then causes both high and low bytes to be transmitted to the 8560 bus as a 16-bit word.

Word mode requires an even 8560 bus address. Therefore, it takes two steps to read a 16-bit word in word mode from the 8560 bus. The first step reads the addressed word from 8560 memory and stores it in a 16-bit latch. The 8088 immediately reads the low byte of the stored word. The next 8560 bus address is odd. This time the LSI-11 does not generate a bus cycle, there is no read operation from 8560 memory, and the temporary latch remains unchanged. The 8088 then reads the high byte stored in the latch from the previous memory read operation.

I/O LOGIC

The I/O logic consists of the SIO-DMA controller with its associated registers, SIO interfacing logic, SIO registers, SIO wait logic, and a baud rate generator.

SIO-DMA Controller 

The SIO-DMA Controller consists of the 8237 four-channel DMA controller device (U3060), latches (U3010) and associated logic. The 8237 performs queuing tasks between the data coming from the SIO device and from IOP RAM. The DMA controller is programmed by the 8088 and provides direct memory access between the IOP memory and the SIO channels.

For each SIO channel, the 8237 automatically stores incoming data in IOP memory. The 8237 reads the data from the SIO device and sends a write pulse to the memory.

The 8088 monitors the status of each channel queue. If the peripheral sending data is an 8540, the queue stops the 8540 from sending data until the queue can accept it. If, however, the peripheral sending data is a terminal, the CTS signal cannot stop the incoming data flow. If the limit of the 8237 queue size is reached, incoming data overruns the queue until the terminal stops transmitting data.

SIO-DMA Control/Status Registers

The 8237 uses seven DMA control/status registers. These software registers are accessed at memory locations 8088H through 808FH. Figure 7-8 shows the registers and their bit assignment.

SIO Interfacing Logic 

The SIO interfacing logic controls serial data interfacing between the IOP and the 8560 on one hand, and the external workstations, such as the 8540, on the other. The SIO interfacing logic consists of U4080, U4100 and associated logic. Each SIO device provides two I/O channels, giving each IOP four-channel capability. Both SIO devices are configured for asynchronous operation.

When interfacing the 8560 to an 8540, the I/O Adapter Board is configured for RS-422 protocol and asserts the HSI mode for the specified channel. When the HSI mode is asserted, the baud rate generator and the SIO channel assume a baud rate of 153.6K baud. Refer to Section 8 for information on the I/O Adapter Board.

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT Ø
W	808F DMAMSK	Ø	Ø	Ø	Ø	MASK 3	MASK 2	MASK 1	MASK Ø
W	808D DMAMC	MASTER CLEAR FOR 8237-2							
W	808C DMACBF	SET FOR LOW BYTE							
W	808B DMAMOD	Ø	1	Ø	AUTO REPEAT	Ø	1	ØØ = SELECT CHØ Ø1 = SELECT CH1 1Ø = SELECT CH2 11 = SELECT CH3	
W	808A DMASMB	Ø	Ø	Ø	Ø	Ø	Ø = CLR MASK 1 = SET MASK	ØØ = SELECT CHØ Ø1 = SELECT CH1 1Ø = SELECT CH2 11 = SELECT CH3	
W	8089 DMAREQ	Ø	Ø	Ø	Ø	Ø	Ø = CLR REQUEST 1 = SET REQUEST	ØØ = SELECT CHØ Ø1 = SELECT CH1 1Ø = SELECT CH2 11 = SELECT CH3	
W	8088 DMACMD	1	1	1	1	Ø	MASTER MASK	Ø	Ø

3900-52

Fig. 7-8. SIO-DMA control/status registers.

Figure 7-9 shows how the IOP Board connects to the I/O Connector (IOC) Board. An SIO treats the data paths as data terminal devices. The IOP channels, however, are configured as data sets. Therefore, signal names must change before they will match the names in the SIO literature.

The upper channel in Fig. 7-9 is configured for a terminal, and all signal levels are compatible with RS-232-C protocol. In Fig.7-9, the lower channel illustrates HSI operation. The HSI signal is asserted low, and the RS-422 differential signals (CTS, RDATA, DTR, TDATA) are used for data transfer.

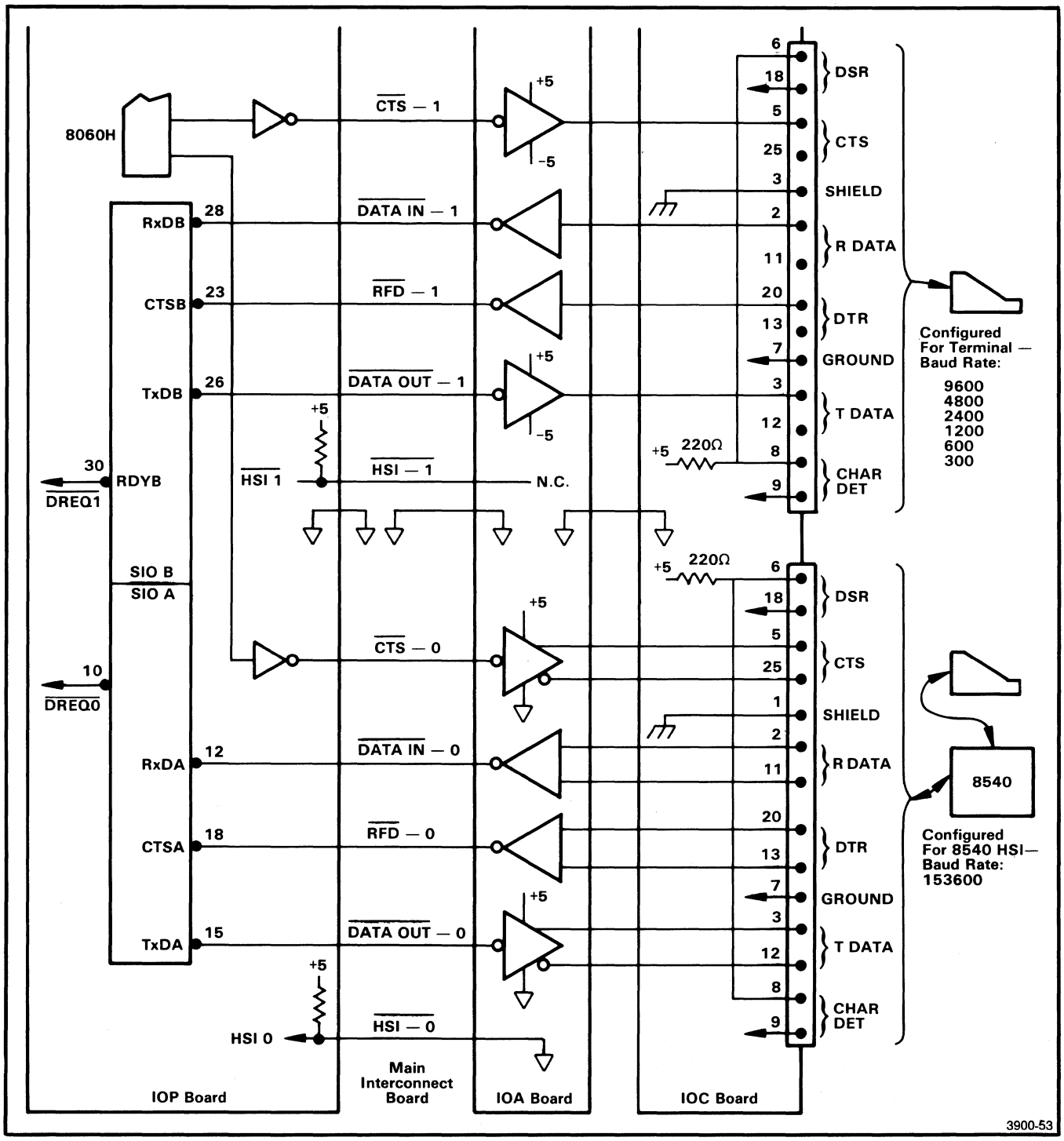

Fig. 7-9. Serial interfacing connections.

SIO Registers

The IOP uses two SIO devices, each providing two duplex channels. Each channel has one data input/output register and one control register. The SIO multiplexes the control registers internally. As a result, the SIO provides eight write registers and three read registers used by the 8088 for status information.

The Control Register is a single read/write address that multiplexes eleven registers: write registers W0 through W7 and read registers R0 through R2. Figure 7-10 defines these write and read registers.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
W 0	0	0	000 = NULL CODE 001 = NOT USED 010 = UPDATE STATUS INPUTS 011 = CHANNEL RESET 100 = NOT USED 101 = NOT USED 110 = ERROR RESET 111 = NOT USED			000 = REGISTER 0 001 = REGISTER 1 010 = REGISTER 2 011 = REGISTER 3 100 = REGISTER 4 101 = REGISTER 5 110 = REGISTER 6 111 = REGISTER 7		
W 1	0=NORMAL 1=DMA	1	1	0	0	0	0	0
W 2	0	0	0	0	0	0	0	0
W 3	00 = R_X 5 BITS 01 = R_X 7 BITS 10 = R_X 6 BITS 11 = R_X 8 BITS		1	0	0	0	0	1
W 4	00 = NOT USED 01 = X16 CLK 10 = X32 CLK 11 = X64 CLK		0	0	00 = NOT USED 01 = 1 STOP BIT 10 = 1½ STOP BITS 11 = 2 STOP BITS		00 = NO PARITY 00 = ODD PARITY 10 = NO PARITY 11 = EVEN PARITY	
W 5	0	00 = T_X 5 BITS 01 = T_X 7 BITS 10 = T_X 6 BITS 11 = T_X 8 BITS	BREAK		TRANSMIT ENABLE	0	0	0
W 6	0	0	0	0	0	0	0	0
W 7	0	0	0	0	0	0	0	0
R 0	BREAK (LATCHED)	X	DTR (CTS)	X	X	T_X BUFF AVAILABLE	X	R_X CHAR AVAILABLE
R 1	X	FRAME ERROR (NOT LATCHED)	OVERRUN ERROR	PARITY ERROR	X	X	X	ALL SENT
R 2	X	X	X	X	X	X	X	X

12807-01

Fig. 7-10. SIO Data/Control Register definitions.

When an output register is ready to accept data, the 8088 simply writes the data into the register. When input data becomes available, it is read from the same address as the output register.

Write Register 0 contains a three-bit pointer that indicates the register to be accessed next. After the register has been accessed, the pointer returns to zero and is ready to be set for another register.

SIO Wait Logic 16

The SIO wait logic consists of binary counter U5160 and associated logic. Because the 8088 clock rate is 5 MHz and the SIO clock is 3.75 MHz, the 8088 must wait for the SIO devices. The SIO wait logic generates the wait states for the 8088. The SIO wait logic provides a wait time of approximately 600 ns. This increases the read or write cycle and allows the SIO to catch up.

The SIO wait logic responds when an address space is accessed. If the address is in the form CXXX, the wait circuit is inhibited. For example, if SIO channel 0 is accessed at location 8000H, the wait logic does not respond. If, however, the same channel is accessed at address C000H, the wait logic is initialized and the 8088's read or write cycle is extended for the required time interval.

Wait logic is also asserted during an 8237 DMA cycle, which moves data between the SIOs and the on-board RAM. The SIO wait logic checks bus address bits 14 and 15 to determine whether or not the SIO wait logic is turned on. The wait logic is asserted when signal lines A14 and A15 are asserted.

Baud Rate Generator 18

The IOP baud rate generator consists of clock generator U2100, latch U2090, and multiplexers U5080, U5090, U5100, and U5110. U2100 generates a crystal-controlled clock frequency of 2.4576 MHz and divides it into several frequencies. Of these, only the 153.6 KHz and 19.2 KHz frequencies are used.

For HSI operation, the SIO receives the 2.4576 MHz frequency. The IOP operating firmware then programs the SIO for a X16 clock, effectively dividing the 2.4576 MHz frequency by 16 and generating a baud rate of 153.6K baud.

For RS-232-C operation, the SIO receives either the 153.6 KHz or the 19.2 KHz frequency as shown in Fig. 7-11. The IOP operating firmware then programs the SIO for a X16, X32, or X64 clock, generating baud rates ranging from 300 to 9600.

Jumpers on the IOA Board determine whether a port communicates as an HSI port or an RS-232-C port. When

HS1	B_n	SIØ	GENERATOR FREQUENCY	BAUD RATE
YES	DON'T CARE	X16	2.4587 MHz	153600
NO	1	X16	153.6 KHz	9600
NO	1	X32	153.6 KHz	4800
NO	1	X64	153.6 KHz	2400
NO	Ø	X16	19.2 KHz	1200
NO	Ø	X32	19.2 KHz	600
NO	Ø	X64	19.2 KHz	300

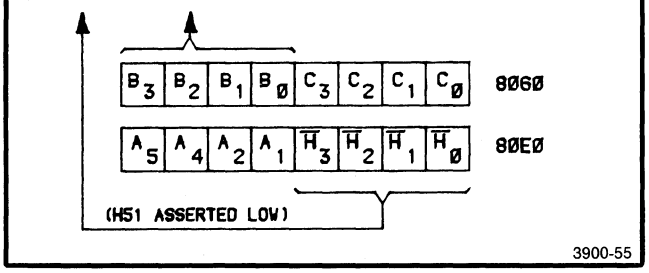

Fig. 7-11. Baud rate control.

strapped for RS-232-C protocol, the port can transmit and receive data at rates varying from 300 baud through 9600 baud. When strapped as an HSI port, the data transmit and receive rate is 153.6K baud.

You can change baud rates on HSI ports by pressing the BREAK key on the terminal keyboard after a port is strapped for RS-232-C. The IOP operating firmware then steps through the available baud rates. At power-up, the default baud rate is 2400.

INTERRUPT VECTOR LOGIC

The vector generator logic provides vector ports for Vector 0 and Vector 1. There are two independent vector circuits that interface with the LSI-11 through vector registers. Vector 1 is loaded at location 808F, and Vector 0 is loaded at location 80F0.

Vector 0 13

The logic for Vector 0 consists of flip-flop U6110A, jumpers, a write-only vector register (U4010), and other associated logic. The priority of Vector Port 0 is selected by jumpers J7121, J7122, J7123, and J7124. Jumpers J7123 and J7124 determine the transmit priority, and J7121 and J7122 determine the receive priority. In addition, bit 2 of the Miscellaneous Register controls when the vector register can be rewritten. If bit 2 is a 1, Vector 0 is still pending. If bit 2 is a 0, the data from the register has been transmitted, and the register is ready to accept new data.

Vector 1 ◇13◇

The logic for Vector 1 consists of flip-flop U6110B, jumpers, a write-only vector register (U4030), and other associated logic. Vector 1 priority is selected by jumpers J7125, J7126, J7127, and J7128. Jumpers J7127 and J7128 determine the transmit priority, and J7125 and J7126 determine the receive priority. In addition, bit 3 of the Miscellaneous Register controls when the vector register can be rewritten. If bit 3 is a 1 , Vector 1 is still pending. If bit 3 is a 0, the data from the register has been transmitted, and the register is ready to accept new data.

Vector Register Content Transmission

When the contents of the 8-bit vector register are transmitted to the LSI-11, two zeros are added to the LSB to produce a 10-bit vector. This vector points to the system memory location from which the LSI-11 fetches a processor status word. The next memory location contains the starting address of the LSI-11 interrupt routine.

Interrupt Priority Levels

Each vector circuit can be independently jumpered for a selected priority level. Priority levels are shown in Table 7-1.

Table 7-1
Priority Levels

Level	Lines Asserted	Lines Monitored
4	BIRQ 4	BIRQ 5, 6
5	BIRQ 4, 5	BIRQ 6
6	BIRQ 4, 6	BIRQ 7
7	BIRQ 4, 6, 7	

Table 7-2
Vector Jumper Functions

Vector 0 Jumper	Vector 1 Jumper	Function
J7121	J7125	IN-IRQ5, NULL, IRQ7
J7122	J7126	IN-NULL, IRQ6
J7123	J7127	OUT-NULL, IRQ5
J7124	J7128	OUT-NULL, IRQ6

Each vector has two sets of jumpers. One set selects the signal lines to be asserted, and the other selects the lines to be monitored on request from the LSI-11. Jumpers and their functions are shown in Table 7-2. For additional information on board configuration and default jumpering, refer to Section 3 of this manual.

DIAGNOSTIC REGISTERS

The IOP Board contains hardware diagnostic registers U2020 (write-only) and U3030 (read-only). The 8088 accesses both registers with I/O instructions.

Write-Only Register ◇15◇

The contents of the write-only register are visually displayed on a seven-segment readout (DS1031) plus decimal point. For each register bit, a zero turns the segment on and a 1 turns it off. Figure 7-12 shows the element selection.

Read-only Register ◇15◇

The positions of jumpers J2041 and J5161 control the contents of the read-only register. If J2041 is open and J5161 is in the default position, a read cycle moves the register contents into the 8088. The read-only register drives the 8088 with NOP instructions. The register is filled with NOP instructions when the pins of J2041 are shorted.

Typically, the read-only register is read at I/O location 0. The read-only register can be strapped to address 90 or 00. If you install a switch on J2041, you can use the read-only register for single stepping through diagnostics. Refer to Section 3 of this manual for the default strap positions.

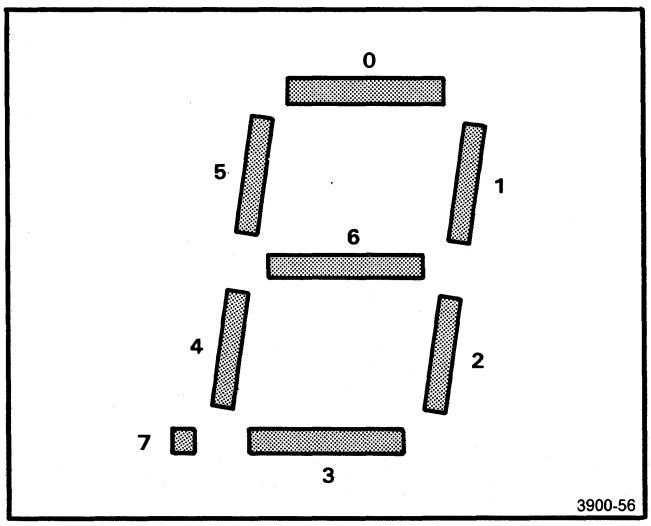

Fig. 7-12. Seven-segment decimal diagnostic display.

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Section 8

I/O ADAPTER AND I/O CONNECTOR BOARDS

INTRODUCTION

This section describes the I/O Adapter (IOA) Board and I/O Connector (IOC) Board. The IOA Board, in conjunction with the I/O Processor and the Utility Board, services the IOC Board's rear panel connectors. These four boards operate together to provide up to ten 8560 serial I/O ports. Figure 8-1 is a block diagram that illustrates the 8560's serial interfacing.

Two ports are line printer ports and operate only under RS-232-C protocol. They are designated LP1 and LP2. The remaining eight ports are typically defined as High Speed Interface (HSI) ports and are designated HSI 0 through HSI 7. HSI ports operate under either RS-422 protocol or RS-232-C protocol.

The IOA Board is a signal conversion board mounted on the 8560 side rail toward the rear of the cabinet. The IOA Board converts signals from TTL levels to RS-232-C or RS-422 levels.

The IOC Board is a small circuit board that contains up to ten 25-pin D-type connectors, depending on your system configuration. The IOC Board contains no active devices. It is mounted on the rear panel with the connectors protruding through the rear panel, making them accessible from outside the cabinet. The connectors serve Printer Ports LP1 and LP2, and up to eight HSI ports.

THE IOA BOARD

The IOA Board contains two identical line printer port circuits, and eight identical circuits that serve the HSI ports.

Line Printer Ports ◇24◇

The following text describes the driver/receiver circuits for Printer Port LP1.

Line receivers U6060C, U6060B, and U8060C operate in the unbalanced mode. They receive the RDATA 1(L), RTS 1(L) and DTR 1(L) lines, respectively. Line drivers U7060D and U7060C operate as single-ended drivers. They drive the TDATA 1(L) and CTS 1(L) signals, respectively.

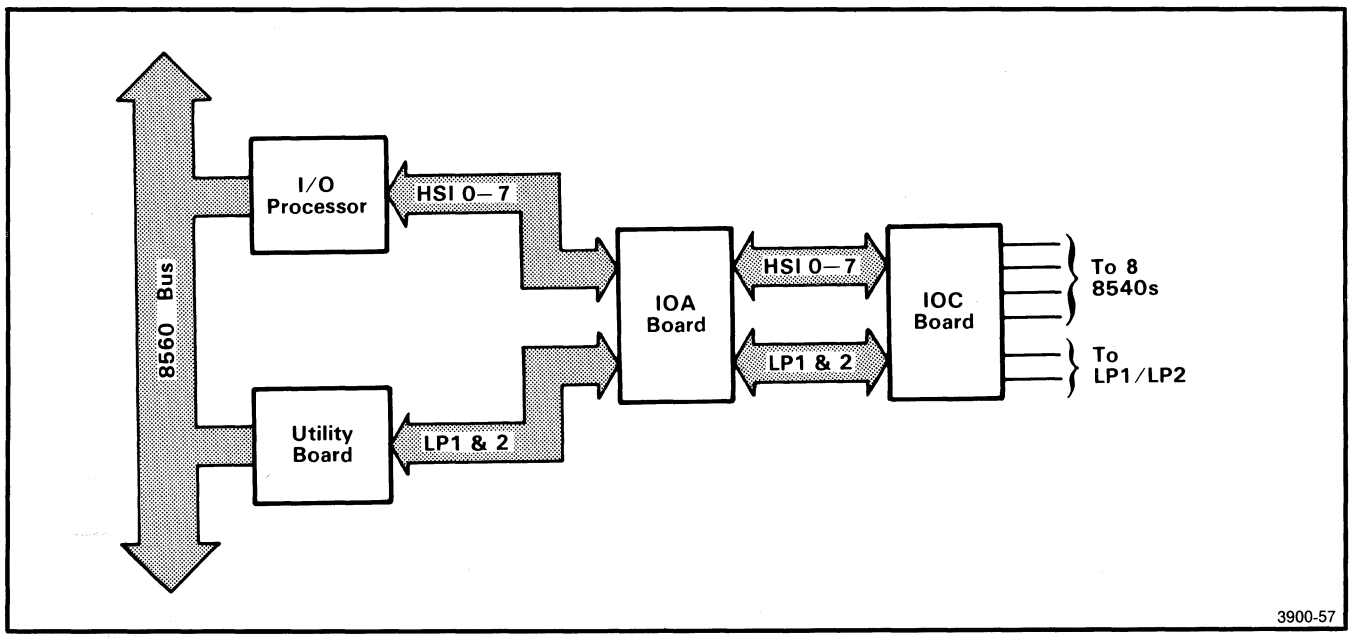


Fig. 8-1. 8560 serial interfacing.

The HSI Ports 20 21

Although the following discussion pertains specifically to HSI Port 0, it applies equally to HSI ports 1 through 7.

The position of jumper J1011 determines whether the port is configured for HSI operation or for RS-232-C operation. The upper position selects RS-422 and the lower position selects RS-232-C. Figure 8-2 shows all jumper locations. Refer to Section 3 for the default jumper positions.

NOTE

HSI Port 0 is factory-jumpered for RS-232-C protocol for use with a system terminal.

When a port operates as a High Speed Interface, U1040D and U1040C are differential input receivers for the DTR 0(L) and RDATA 0(L) lines, respectively. During RS-232-C operation, U1040D and U1040C are connected as unbalanced line receivers for these lines. Positive inputs are grounded, and the signals are applied to the negative inputs.

The TDATA 0(L) and CTS 0(L) lines are driven by U1030, which is configured as a dual differential driver. During High Speed Interface operation, both lines are balanced. During RS-232-C operation, only the inverting outputs of U1030 are used, and outputs are unbalanced.

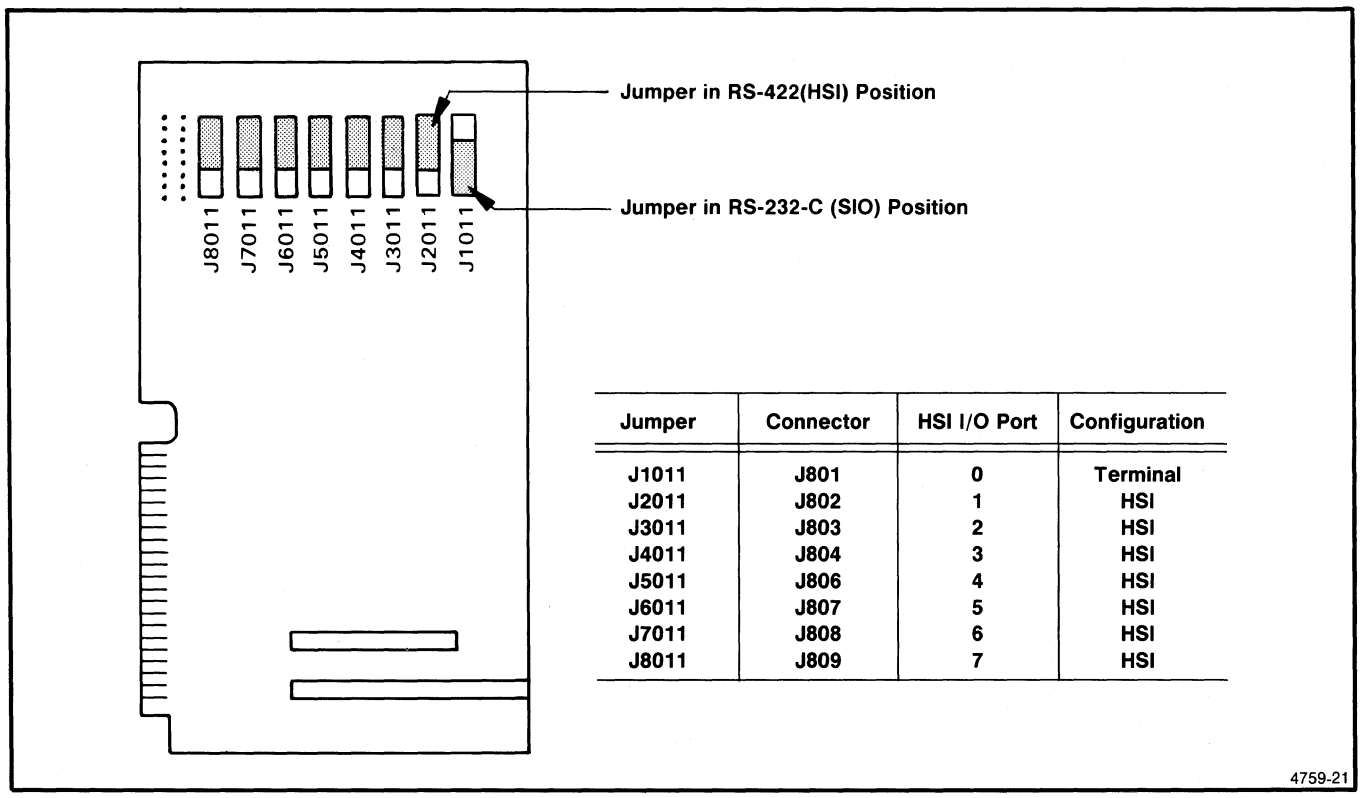
The HSI0 signal connects J1011 to the I/O Processor. When the jumper is in the High Speed Interface position, HSI0 is grounded, indicating to the I/O Processor that High Speed Interface operation has been selected. When the jumper is in the RS-232-C position, HSI0 is not grounded and the I/O Processor selects one of six baud rates compatible with RS-232-C protocol.

Power Supply

The IOA Board receives +5 V, -12 V, and +12 V supplies from the 8560 backplane. A -5 V supply is derived from the -12 V supply by U1050.

THE IOC BOARD 25

The IOC Board contains up to ten 25-pin D-connectors for Printer Ports LP1, LP2, and up to eight HSI ports. The connector assignment for each port is shown in Table 8-1. The connector pin assignments are shown in Tables 8-2 and 8-3.



Jumper	Connector	HSI I/O Port	Configuration
J1011	J801	0	Terminal
J2011	J802	1	HSI
J3011	J803	2	HSI
J4011	J804	3	HSI
J5011	J806	4	HSI
J6011	J807	5	HSI
J7011	J808	6	HSI
J8011	J809	7	HSI

Fig. 8-2. IOA Board jumper locations.

If your system has one IOP Board, the installed IOC Board contains four connectors, serving two to four ports (HSI ports 0 through 3). If, however, your system contains two IOP Boards, the IOC Board contains eight connectors, serving HSI ports 0 through 7.

The IOC Board connects to the IOA Board with 20-pin connector J8102 and 72-pin connector P2.

Table 8-1
Port Connector Assignments

Port	Connector
LP 1	J8051
LP 2	J8101
HSI 0	J8011
HSI 1	J8021
HSI 2	J8031
HSI 3	J8041
HSI 4	J8061
HSI 5	J8071
HSI 6	J8081
HSI 7	J8091

Table 8-2
HSI Port Connector Pin Assignments

Pin	Name	Function
1	Shield	
7		Signal Ground
2	R DATA	Receive Data
11	R DATA'	
3	T DATA	Transmit Data
12	T DATA'	
20	DTR	Data Terminal Ready
13	DTR'	
5	CTS	Clear To Send
25	CTS'	
6	DSR	Data Set Ready
18	DSR'	
8	CAR DET	Carrier Detect
9	CAR DET'	

1. The DSR and CAR DET signals are always transmitted ON.
2. During RS-232-C operation, only the positive (+) side of the balanced signals is used.

Table 8-3
Line Printer Ports 1 and 2 Pin Assignments

Pin	Name	Function
1	Shield	
7		Signal Ground
2	R DATA	Receive Data
3	T DATA	Transmitted Data
20	DTR	Data Terminal Ready
5	CTS	Clear to Send
6	DSR	Data Set Ready
8	CAR DET	Carrier Detect
15	T CLK	External Clock
17	R CLK	External Clock
4	RTS	Request to Send

1. The DSR and CAR DET signals are always asserted.
2. The external clock input (T CLK and R CLK) is routed directly to the Utility Board.

Shield Straps

All output connector shields are grounded through a strap. To deal with unusual static discharge problems, you can cut these straps and bridge the gaps with passive components.

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MASS STORAGE CONTROLLER BOARD

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Section 9

MASS STORAGE CONTROLLER BOARD

INTRODUCTION

This section describes the Mass Storage Cntroller (MSC) Board's hardware and firmware and provides information about how the MSC hardware interacts under firmware control with the TNIX Operating System. In addition, this section describes internal command buffers that control the MSC Board hardware.

The MSC Board, together with the Xebec S1410 Disk Controller Board, interfaces the 8560 to the flexible and hard disk drives. The MSC Board provides control and interface functions for the flexible disk, and control functions for the Xebec Disk Controller Board. The Xebec Disk Controller Board handles interface functions for the hard disk drive and is described in Section 10 of this manual. The disk drives are described in Section 11.

MSC HARDWARE

For the purpose of this discussion, the MSC Board hardware consists of the following:

- The kernel
- The LSI-11 8560 bus interface
- I/O Logic
- The flexible disk controller
- The SCSI bus interface
- Diagnostic jumpers and test points

Fig. 9-1 shows a block diagram of the MSC Board.

The MSC kernel consists of an Intel 80186 processor, 8K x 16 bits of RAM, and 16K x 16 bits of EPROM.

The 8560 bus interfacing circuits consist of DMA circuits that transfer data to and from the system memory under control of the MSC Board's 80186 processor. Furthermore, DMA disables the LSI-11's control of the 8560 bus and allows the 80186 to obtain control.

The I/O logic provides 8560 bus control and status to the 8560 flexible disk drive and the SCSI bus. It also affords diagnostic capability.

The Flexible Disk Controller (FDC) circuitry controls the flexible disk drive. The precompensation logic and the phase-locked loop reside within the FDC chip.

The SCSI bus interface consists of two 8-bit registers/buffers, a state machine to coordinate handshaking during data transfers, and a state machine to handle arbitration and selection.

The MSC Board contains a number of jumpers used for troubleshooting. Section 3 contains the jumper default positions.

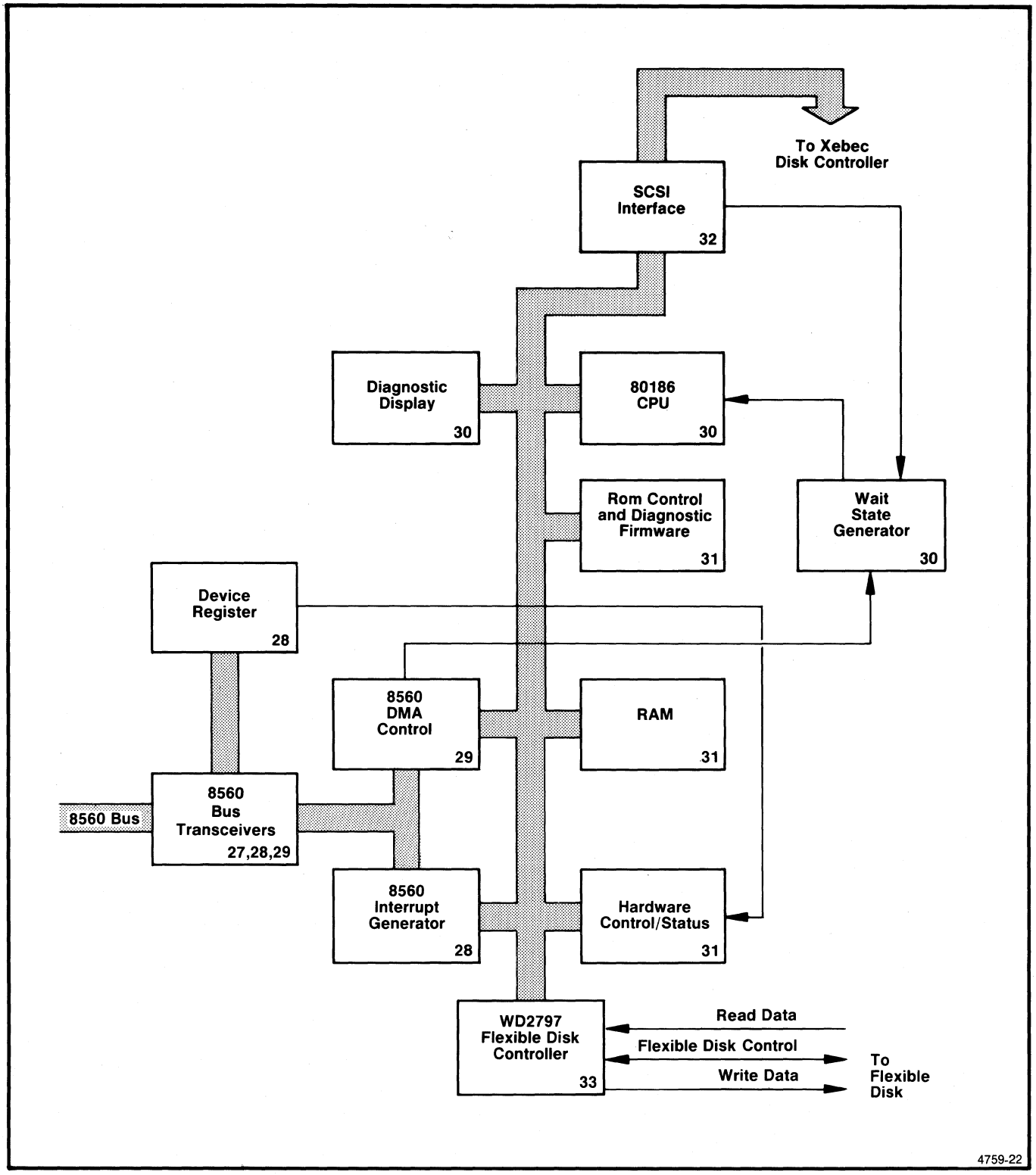


Fig. 9-1. The MSC Board block diagram.

The Kernel

The MSC kernel consists of the 80186 microprocessor, 8K x 16 bits of RAM, and 16K x 16 bits of EPROM.

The 80186 Processor 

The 80186 microprocessor (U3070) controls the MSC. It fetches instructions from ROM and performs the specified operations. The 80186 CPU instructions are contained in 16K words of on-board ROM, and 8K words of RAM serve as working memory.

The 80186 is a leadless chip with 68 connections. It contains an 8 MHz microprocessor that can be regarded as an 8086 in min mode with an extended instruction set. The chip also contains a clock generator, two channels of DMA, three programmable counter/timers, thirteen programmable chip select lines and an interrupt controller.

Address Decoding 

Address decoding for the MSC Board is performed by the 80186. Table 9-1 describes the 80186 chip select lines and their functions.

Table 9-1
80186 Chip Select Lines/Functions

80186 Chip Select Line	Function
UCS(L)	Selects EPROM
MCS1(L)	Selects FDC
PCS6(L)	Selects SCSI Data Register
PCS5(L)	Selects Diagnostics Register
PCS4(L)	Selects Disk Status Register
PCS3(L)	Qbus Vector Register
PCS2(L)	Qbus Status Register
PCS1(L)	Qbus High Address
PCS0(L)	Diagnostics Display
LCS(L)	Selects RAM

The MSC Memory 

The EPROMs extend from F8000H to FFFFFH (U4060, U4090) and contain command and diagnostics firmware for the board. The RAM (U4040, U4080) extends from 00000H to 03FFFH and holds stack for the CPU, queued commands from the LSI-11 and data transferred to or from the flexible and hard disks. Figure 9-2 shows a memory map of the 80186 I/O space.

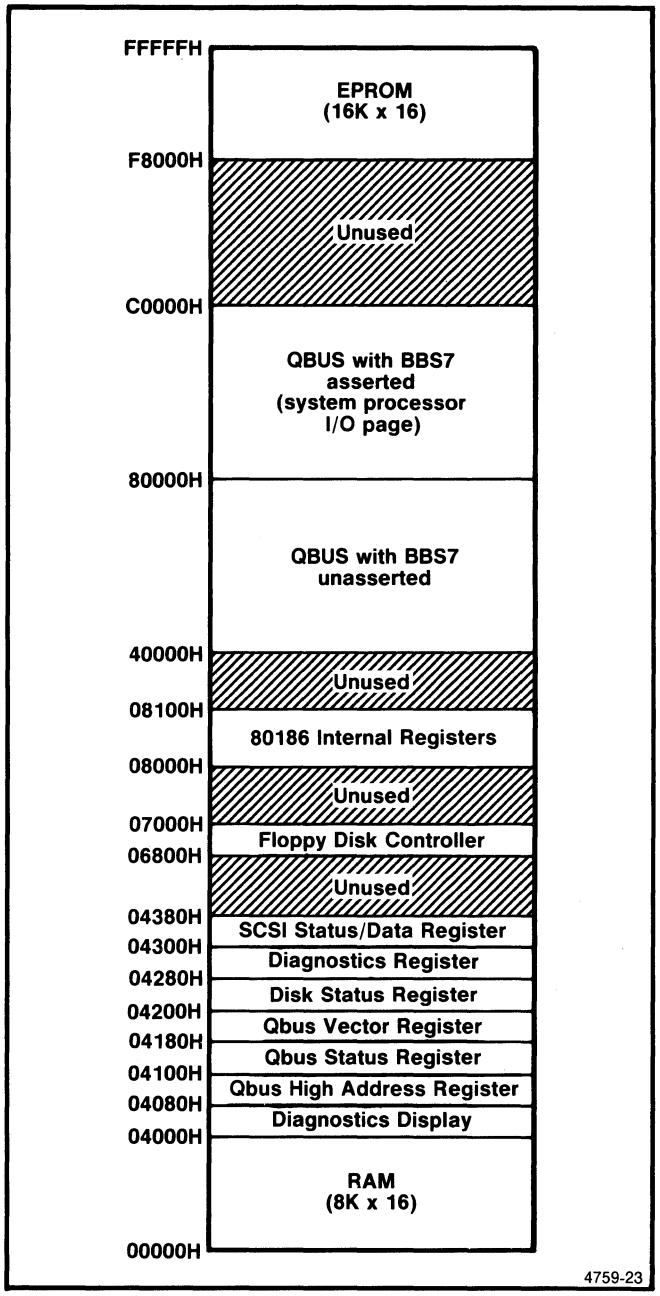


Fig. 9-2. The MSC memory map.

LSI-11 Interfacing

This section covers the DMA control logic, DMA data address registers, interrupt logic, and 8560 bus transceivers.

DMA Control 29

The MSC contains a DMA control circuit which transfers data to and from the system memory under control of the 80186 processor. A DMA disables the LSI-11 and allows the 80186 to take control of the 8560 bus. The 80186 initiates a DMA operation and accesses data in the two middle 64K-byte memory banks in the 80186 memory space.

Qbus DMA State Machine 29

A Finite State Machine (FSM) was designed to handle the DMA cycles on the Qbus and incorporated into PLA (Programmable Logic Array) U4130 and several external gates. The inputs, outputs and the timing of the state machine are shown in Fig. 9-3. Several of the inputs pass through U4160 before being input to the FSM. They are multiplexed with firmware-controllable signals which are output by the Diagnostics Register. For the following discussion, assume that the A inputs of U4160 are the inputs to the FSM.

Inputs. The REQ(H) input informs the FSM that a Qbus transfer is ready to occur. The CONT(H) input is cleared if a single transfer is to occur and set for multiple transfers. The state machine checks the CONT(H) input before the end of each transfer. If it is cleared, the state machine relinquishes the Qbus. If CONT(H) is set, the state machine waits until REQ(H) goes high, indicating that everything is in place for the next transfer to begin.

The REQ(H) input goes high whenever an 80186 address that maps out to the Qbus is accessed and cleared when one state after RPLY is asserted by the memory board. This ensures that the 80186 data is held on the D0-15(H) bus long enough. The CONT(H) input is the output of the Diagnostics Register. Before executing a DMA cycle with multiple transfers, the firmware must set CONT(H). After the Qbus transfer has completed, CONT(H) must be cleared in order to free the Qbus.

The input DIAGCONT is set or cleared by writing to the Diagnostics Register. When set, DIAGCONT does not allow the state machine to advance past state T4 (see Fig. 9-2). This holds the Qbus address on the DIN bus so that it can be read back during the execution of diagnostic firmware. During normal operation, DIAGCONT(L) will be cleared.

An LS393 counter (U5170-B) output is ORed with Qbus RPLY(H) to timeout the Qbus. If the FSM does not receive RPLY(H) from the Qbus within 32 μsec, an on-board RPLY(H) is generated by the counter to finish the transfer cycle. QBUSTIMEOUT(L) is asserted when a timeout occurs. DMGGI(H) and RSYNC(H) are received directly from the Qbus.

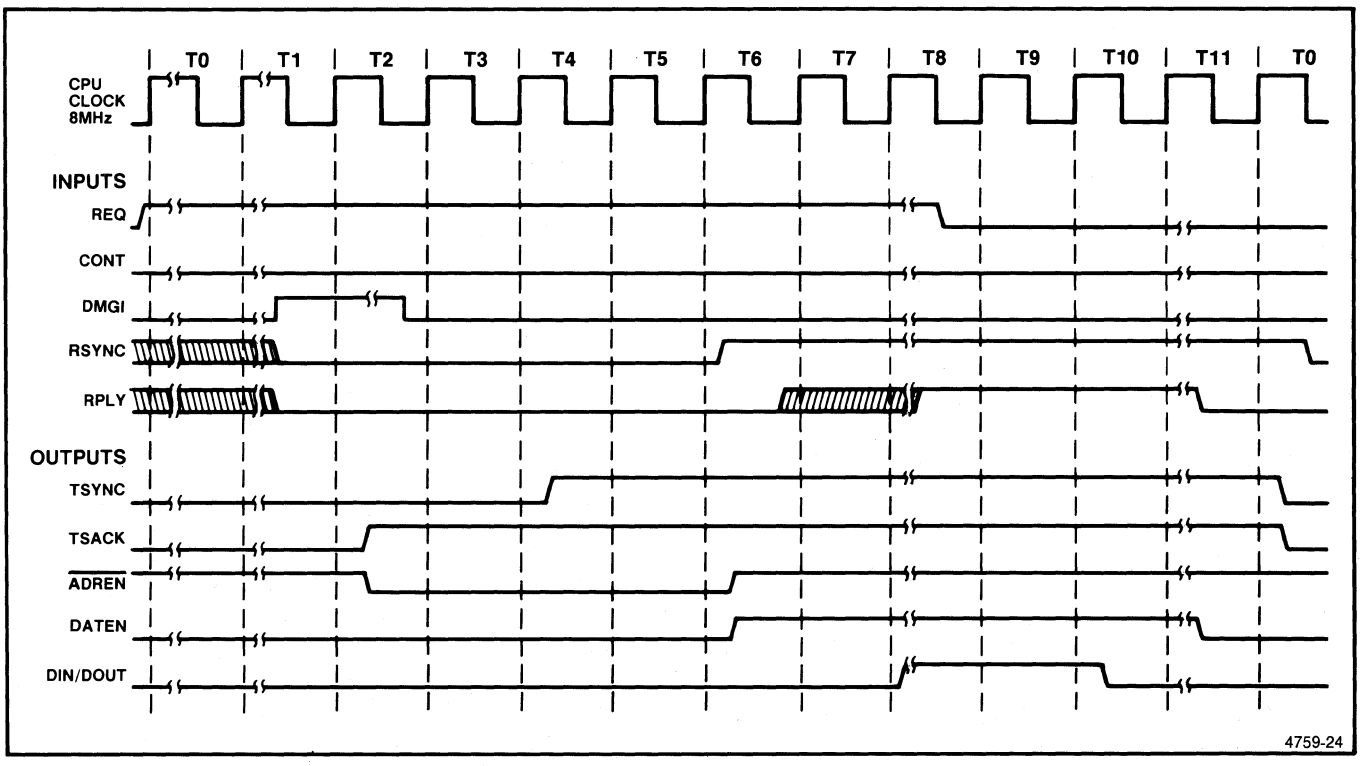


Fig. 9-3. Inputs, outputs and timing of the DMA state machine.

Outputs. The signal ADREN(L) enables the address buffers. This signal ensures that the address appears on the Qbus at the right time during DATI and DATO cycles. The DATEN(H) signal performs the same function for the data out registers during DATO cycles.

TSACK(H) and TSYNC(H) are output directly to the Qbus and meet the Qbus specifications. TDIN/DOUT(H) is output to the Qbus DIN line during a DATI transfer. TDOUT(H) is output to the Qbus DOUT(H) line during a DATO transfer.

DMA Data and Address Registers ◇27◇ ◇28◇

The following paragraphs describe DMA address comparator logic and four DMA data and address registers. The registers are used by the DMA control logic, and are as follows:

- Device Register
- Data-In Register
- Data-Out Register
- High Address Register

Device Register. The Device Register (U4010, U4020) is located in the I/O page of the Qbus memory at address 777150.

During each Qbus cycle, RSYNC(H) latches the state of the Qbus address data lines into U3020. If there is a match between the Qbus address data lines and the Device Register address, the output of U3010 goes low and the output of U3010 is asserted. If the Qbus cycle is a DATO cycle, the DOUT signal is used to latch the Qbus data into the Device Register and generate a TRPLY(H) signal. If the cycle is a DATI cycle, the DIN signal puts the data on the Qbus by enabling the Device Register outputs. DIN is also used to generate TRPLY(H).

The Device Register cannot be directly accessed by the 80186 CPU. The 80186 must go through the Qbus to read or write the Device Register.

Data-In Register. The 16-bit Data-In Register (U5010 and U5030) latches data received from the 8560 system memory during a DMA access.

Data-Out Register. The Data-Out Register (U5020 and U5040) receives and latches data to be transmitted to the 8560 bus from the 80186.

High Address Register. The Qbus High Address Register outputs the six most significant address lines on the Qbus (AD16 through AD21). This register consists of one LS373 transparent latch (U5070). Before accessing Qbus memory, this register is loaded under firmware control.

8560 Interrupt and Vector Circuitry ◇28◇

When the 80186 CPU writes to the Vector Register (U4030), the Disk Controller Board interrupts the LSI-11. The Vector Register write signal (U4175, pin 8) clocks U4115A that latches out an interrupt request to the Qbus on the IRQ(L) lines. The priority of the Disk Controller Board interrupt is Level 5. When the DIN signal is received from the Qbus, U4115B is clocked. If any other interrupts are pending on the Qbus and are of higher priority, the flip-flop will clock a low on its Q output, causing the IAKI(L) input signal to be duplicated on the IAKO(L) output signal. If no interrupts of higher priority are pending on the Qbus, the flip-flop will clock a high on its Q output and use the IAKI(L) input signal to generate the Qbus RPLY signal. INTDATEN(L) is used to enable U4030 to put the vector on the address data lines of the Qbus. INTDATEN(L) also clears the interrupt request.

8560 Bus Transceivers ◇27◇

U6010, U6020, U6030, U6040, U6050 and U6080 buffer data and addresses from the 8560 bus. Pins 7 and 9 are the enable inputs. When they are low, the MSC transmits data and addresses to the system memory.

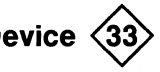
When an interrupt occurs on the bus, QBUSVECTEN(L) is asserted. That enables U6020 and U6030, address bits 2 through 9. The other address bits remain disabled and float to a logical zero.

U6060, U6080, U6090 and U6100 serve the DMA control lines, memory access control lines, and interrupt control lines.

Flexible Disk Controller

This section covers the part of the MSC Board that controls access to the QumeTrak 242 disk drive. For this discussion, the controller circuits are divided into the following parts:

- The flexible disk controller device
- The head load circuitry
- The write precompensation circuit
- The phase-locked loop circuit
- The flexible disk driver/receiver circuits

The Flexible Disk Controller Device 

The flexible disk interface is simplified considerably due to the use of the Western Digital 2797 Flexible Disk Controller Chip (U5130). This chip generates most of the signals necessary for the flexible disk interface. It also contains a phase-locked loop. Therefore, the chip can read the data directly from the disk and lock on the data without the aid of external circuitry. In addition, U5130 performs data separation of incoming data and write data precompensation on chip. However, the MSC Board has the capability to control one 8-inch drive only.

U5130 contains four registers: a Command/Status Register, a Disk Data Register, and two Command Parameter Registers.

The Head Load Circuitry 

The head load circuitry is composed of flip-flop U6160B and timer 0 of the 80186. When a command is issued to U5130 which requires reading or writing the disk, U5130 asserts its HLD(H) output. This asserts the drive's HEADLOAD(L) signal and enables a 500 KHz signal to clock timer 0 of the 80186. The HLD signal also clocks the flip-flop whose output sets the U5130 HLT(H) input low. U5130 will not access the disk until its HLT input is high. This allows for the head to settle on the disk. The timer 0 output of the 80186 (TIMER0) is set under firmware control to generate a negative-going pulse after the head settling time has elapsed. This pulse presets U6160B, thus setting HLT(H). If there is no disk activity for 15 disk revolutions (2.5 sec), the HLD(H) signal is deasserted.

The Write Precompensation Circuit 

Due to the physical disk limitations, data patterns on inner disk tracks 43 through 76 are located much closer to each other than on the outer tracks. This causes the timing of bits to shift when they are read back. To overcome this problem, data is written a little sooner or later than normal. This is called write precompensation.

A 10K pot (R5158) on the WPW input of U5130 is used to set the amount of write precompensation. A setting of 100 ns to 300 ns from normal is possible. The write compensation is set during the phase-locked loop calibration procedure.

The Phase Locked Loop Circuit 

The phase-locked loop compensates for data rate shifts that occur as the data is read from the flexible disk. Data rate shifts can occur when the disk speed changes.

U5130 has an internal phase-locked loop circuit. However, the addition of a 10K pot (R6153), a variable capacitor (C6151), and a first-order, lag-lead filter are needed to complete the circuit. The filter is connected to the PUMP output of U5030 and consists of C5155, R5153, and CR5151. This filter controls the instantaneous response of the VCO to bit-shifted data (jitter), as well as the response to normal frequency shift (the lock-up time).

The 10K pot tied to the RPW input of U5130 sets the internal Read Data pulse for proper phasing. The variable capacitor adjusts the free-running frequency of the phase-locked loop.

Phase-Locked Loop Calibration. The phase-locked loop is calibrated using the following procedure:

1. Situate the 8560 so that you have access to the top of the unit. Make sure the power on the 8560 is off. Remove the top cover, following the instructions in Section 15, "Removing the Cover Panels."
2. Remove the MSC Board from the card cage. Install an extender card in the MSC slot, and insert the MSC Board in the extender card.
3. Make sure jumper P6141 is in its normal position, connecting the upper pin (indicated by an arrow) and the middle pin.
4. Power up the 8560.
5. Attach an oscilloscope probe to TP5131.
6. Move jumper P6141 so that it connects the middle and lower pins.
7. Adjust variable resistor R6153 until the oscilloscope reflects a 500 KHz signal and the positive-going pulses are 250 ns wide.
8. Move the probe to TP5153.
9. Adjust variable capacitor C6151 for a 500 KHz square wave.
10. Move the probe to TP6111.
11. Adjust variable resistor R5158 until the positive-going pulses on the oscilloscope are 200 ns wide.

Flexible Disk Driver/Receiver Circuits 33

U6170 and U6129 are used to drive signals that the MSC outputs to the flexible disk drive. U6110, U5120 and U3110 receive incoming signals from the flexible disk drive. Table 9-2 describes the flexible disk's input signals, and Table 9-3 describes the flexible disk's output signals.

Table 9-2
Flexible Disk Input Signals

Signal	Description
TRACK00(L)	This signal indicates when the R/W head is positioned at track 0 (the outermost track). A logical 1 indicates that the head is positioned at track 0.
WRITE PROTECT(L)	This signal informs the WD2797 when a write-protected disk is installed. A logical 1 indicates that the disk is write-protected. The drive inhibits writing to a write-protected disk.
TWO SIDED(L)	This interface signal indicates whether a two-sided or a single-sided disk is installed. A logical 1 indicates that a two-sided disk is installed. A logical 0 indicates a single-sided disk.
INDEX(L)	This signal arrives from the flexible disk drive once for every disk revolution (approximately every 167 ms). INDEX(L) indicates the beginning of the track (sector 1). INDEX(L) is asserted for a period of 1.8 ms once every revolution.
READ DATA(L)	This signal carries the incoming data stream when the heads are loaded.
READY(L)	READY(L) confirms that the drive contains a disk, the door is closed, and the disk is at operating speed.
DKCHG(L)	This signal informs the 80186 that the disk drive door has been opened, indicating a possible change of disks.

Table 9-3
Flexible Disk Output Signals

Signal	Description
STEP(L)	This pulse causes the R/W heads to move one track in the direction defined by the DIRECTION line.
LOW CURRENT(L)	This interface line switches to the low write current mode for tracks 43 and higher.
DIRECTION(L)	This signal defines the direction of the R/W heads when the STEP signal is asserted. A logical 1 defines the direction as "in". As a result, the R/W head moves toward the center of the disk (high-numbered track). A logical 0 defines the "out" direction and the R/W head moves toward the outer disk edge.
DRV SEL(L)	This output line enables the flexible disk drive.
WRITE DATA(L)	This interface line sees a 250 ns pulse whenever a data bit is written on the disk.
HEAD LOAD(L)	This signal loads the R/W head against the disk. The HEAD LOAD signal also locks the drive door. The HEAD LOAD signal remains true for 2.5 seconds after the last disk operation. In addition, the HEAD LOAD signal lights the LED indicator on the flexible disk drive door.
WRITE GATE(L)	This signal informs the flexible disk drive that a write operation is in progress. This signal is ANDed with WRITE PROTECT to supply the write current.
SIDE SELECT(L)	This signal selects the proper disk side for reading or writing. A logical 0 selects side 0, a logical 1 selects side 1.

SCSI Interface Circuitry

The SCSI interface circuitry allows the MSC Board to talk to SCSI compatible devices. It supports arbitration and reselection. The MSC Board cannot talk to other initiators but only talks to targets. Initially the SCSI interface on the MSC Board will be used to communicate with one or two hard disk controllers. Tape controllers or other SCSI-compatible devices may be attached to the SCSI bus at a later date.

Data and Status Lines 

Four AMD2908s (U2110, U2120, U2140, U2150) are used to interface to the data lines and all but one of the status lines on the SCSI bus. Each 2908 contains a four-bit transceiver register and a four-bit receiver register. The transceiver register is a latch similar to an LS374. The receiver register is a transparent latch similar to an LS373. The bus lines are open collector. Each 2908 also has a built-in parity check.

Two of the 2908s (U2140, U2150) are combined into a SCSI data register that the CPU can read and write at address 4300H. The other two 2908s (U2110, U2120) make up the SCSI Status Register at 4200H. A copy of the last word written to this register by the MSC firmware must be kept in RAM. When a SCSI status line is set by the firmware, a read-modify-write operation cannot be performed because a read of the SCSI Status Register is an inverted read of the SCSI bus lines. A copy of the last word written serves as a record of which bits were set by MSC firmware as opposed to other devices on the bus.

The SELECT line on the SCSI bus is set and cleared through writing a bit in the Disk Status Register. This allows the arbitration state machine to determine when the SEL(L) line is asserted by a device other than the MSC Board.

SCSI Arbitration and Selection 

Arbitration on the SCSI bus is done through a combination of firmware and a state machine contained in part of the PAL16R4 (U2130). The firmware writes the MSC Board's ID to the data buffers and then sets the state machine input, ARBEN(H). When ARBEN(H) is set, the state machine (see Fig. 9-4) waits for both the SEL(H) and BSY(H) lines on the SCSI bus to be deasserted. When this condition is detected, the state machine waits one state (approximately 125 ns) before asserting BSY(H) and enabling the MSC Board's ID from the data buffers onto the SCSI bus. The assertion of BSY(H) (read back through the signal ONBUS(H)) signals

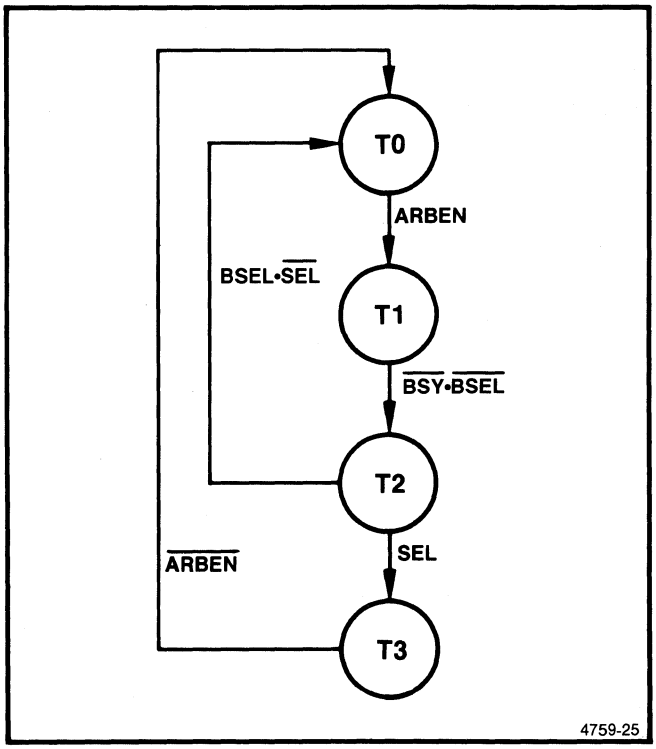


Fig. 9-4. SCSI arbitration diagram.

the firmware to check to see if the MSC Board is the highest priority device on the bus. If not, the firmware does nothing because the higher priority device on the bus will eventually assert SEL(H), forcing the state machine to its initial state. If the MSC Board is the highest priority device on the bus, it then goes through the selection process in firmware, by asserting SEL(H) and BSY(H). The assertion of SEL(H) by the MSC firmware advances the state machine to T3. The firmware then asserts the target's ID on the bus, deasserts BSY(H) and waits for BSY(H) to be asserted by the selected target. When the target asserts BSY, the selection process is complete. When ARBEN(H) is cleared, the state machine returns to state T0.

Data Transfers on the SCSI Bus 

Data transfers to the SCSI bus are done through 80186 DMA transfers and a DMA state machine. The 80186 DMA transfers are not synchronized. This means that the DMA cycle (read the source, write the destination) will occur at full processor speed regardless of the validity of the data on the bus. The purpose of the state machine is to insert wait states in the read cycle of the DMA cycle until the SCSI bus REQ(H) line is asserted, indicating that the target is ready to send or receive another byte. Figure 9-5 shows a SCSI data transfer.

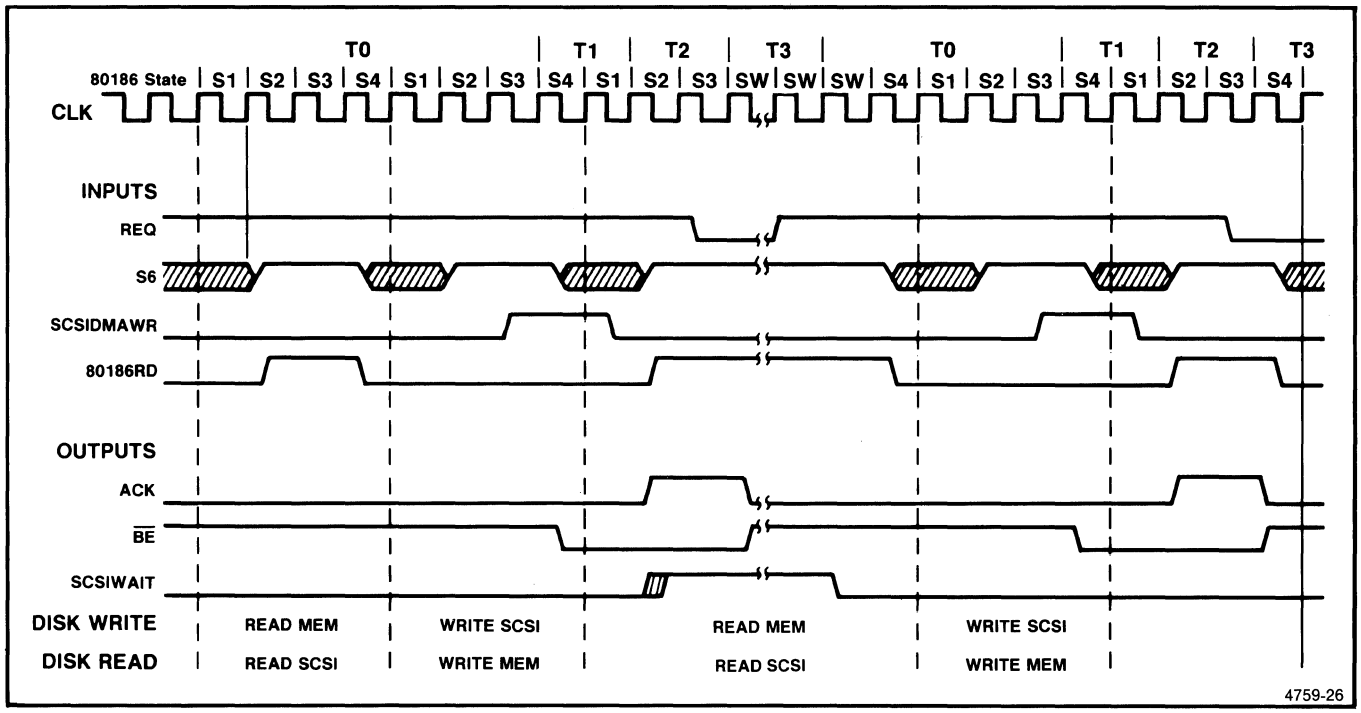


Fig. 9-5. SCSI data transfer.

Inputs. The state machine timing diagram is shown in Figure 9-4. The input S6 comes directly from the 80186. This input is valid in CPU states S2, S3, SW and S4 of a CPU read or write cycle and indicates that a DMA cycle is in process when asserted.

The REQ(H) input is a logical OR of three signals: the SCSI bus REQ(H), a firmware programmable request used to reset the state machine after a transfer takes place, and a timeout signal. The REQ(H) input is synchronized to the state machine clock.

Outputs. The outputs of the state machine are BE(L), ACK(H) and SCSIWAIT(L).

The ACK(H) signal is asserted in the read cycle of the DMA transfer and dropped one state after the REQ(H) input has been deasserted.

The BE(L) signal enables the transceiver register outputs in the 2908s onto the SCSI bus. BE(L) will be active during both SCSI reads and writes. Therefore, before a SCSI read takes place, the firmware must write 00H to the SCSI data lines.

Hardware Registers <29> <31>

The following paragraphs describe the various MSC Board hardware registers.

Disk Status Register. The Disk Status Register can be acccessed through address 4200H. It is composed of U3130 for writing and U1060 for readback. It is 8 bits wide. Although it is called the Disk Status Register, some diagnostic testing signals are output by this register. Its bits have the following definitions:

D0 This bit is read only. It is readback of the ONBUS(H) output of the SCSI arbitration state machine. When set, the MSC Board has won mastership of the SCSI bus.

D1 This bit provides readback of the flexible interface signal, DKCHG(H). When set, it indicates that the door of the flexible drive has been opened, resulting in a possible change of disks.

D2 This bit is the diagnostics signal DIAGS(H). Its purpose is described in the discussion on diagnostics.

D3 This bit is the diagnostics signal QBUSEN. Its purpose is described in the discussion on diagnostics.

D4 This bit, when cleared, resets both the SCSI arbitration state machine and the SCSI DMA state machine.

D5 This bit sets or resets the SCSI bus SEL(H) line.

D6 Unused.

D7 When set, this bit tells the SCSI arbitration state machine to arbitrate for the SCSI bus.

Qbus Status Register. The Qbus Status Register can be accessed through address 4180H. It is composed of flip-flops U1080, U1040 and U4110B for writing and U1090 for readback. It is 8 bits wide. Although it is called the Qbus status Register, some bits are not concerned with the Qbus. Its bits have the following definition:

D0 This bit, when set, indicates that the Device Register has been written. D0 can be set or cleared by writing to the register.

D1 This bit, when set, indicates that the Qbus timed out during a Qbus DMA transfer. D1 can be set or cleared by writing the register.

D2 This bit, when set, configures the Flexible Disk Controller Chip to read and write single-density disks. When cleared, the Flexible Disk Controller Chip assumes a double-density disk is in the drive.

D3 This bit is read only. When set, D3 indicates that an interrupt to the Qbus is pending.

D4 This bit is read only. When set, D4 indicates that a parity error occurred when reading or writing LSI-11 memory.

D5 This bit is read only. When D5 is set, a double-sided disk is in the flexible disk drive unit. When cleared, a single-sided disk is in the drive.

D6 This bit can be read or written. When set, D6 selects flexible disk drive number 1.

D7 This bit provides readback for the INTRQ output of the WD2797.

Diagnostics Register. The Diagnostics Register is used by the diagnostics firmware to test the Qbus interface. A full description of how to use the register for diagnostic purposes is given in the section on board test hardware.

The Diagnostics Register can be accessed through address 4300H. It is composed of U3160 for writing and U2160 for readback. Its bits have the following definitions:

D0 When written, this bit is the diagnostics signal, DCONT. When read, D0 is the TSACK output of the Qbus DMA state machine.

D1 When written, this bit is the diagnostics signal, DREQ. When read, D1 is the TDIN/DOUT output of the Qbus DMA state machine.

D2 When written, this bit is the diagnostics signal DRPLY. When read, D2 is the TSYNC output of the Qbus DMA state machine.

D3 When written, this bit is the diagnostics signal, DDMGI. When read, D3 is the DATEN output of the Qbus DMA state machine.

D4 When written, this bit is the diagnostics signal, SYNC. When read, D4 is the ADREN(bar) output of the Qbus DMA state machine.

D5 When written, this bit is the diagnostics signal, DQBUS.

D6 When written, this bit is the diagnostics signal, IAKI. When read, D6 specifies the SCSI ID for the MSC Board. This bit can be configured to be a logic low or high through a jumper. D6 is interpreted as follows:

D6	SCSI ID
0	40H
1	80H

D7 When written, this bit is the diagnostics signal, DDATA. When read, D7 is the diagnostics signal, DRDY.

FIRMWARE/HARDWARE INTERACTIONS

This section describes interactions between the MSC hardware, the MSC operating firmware, and the TNIX Operating System.

Simplified Disk Access Operation

When you enter a command from the terminal requiring the TNIX operating system to access a file (either to read or to write), a sequence of steps occurs. During that sequence, TNIX generates a command buffer in the 8560 memory and stores the starting address of that buffer in a hardware register on the MSC . TNIX then informs the MSC that it can access the command buffer and execute the command it contains. Here is a simplified description of this sequence:

NOTE

Except where noted, this description is valid for both read and write operations. Only the direction of transfer differs.

1. TNIX searches the disk directories during a read operation until it finds the specified file and identifies its corresponding disk blocks. In a write operation, TNIX searches the free queue for an empty disk block into which to write. Free queues are described later in this section.
2. TNIX requests that the MSC transfer the specified blocks it has identified. TNIX provides the MSC with a block number, byte count, and the memory location at which the MSC must deposit the block of data. These parameters are stored in a command buffer in 8560 memory. If the file is larger than one block, TNIX still requests one block at a time.
3. TNIX stores the command buffer address in the Device Register located on the MSC Board. (This register is described earlier in this section.)
4. The 80186 on the MSC Board performs a DMA operation and reads the buffer contents. (Since the Device Register is not on the 80186 bus, the 80186 cannot access this register directly).
5. The MSC firmware stores the command buffer instructions in the command queue for the accessed disk drive and informs TNIX that the instructions have been received.
6. The command queue may already contain other previously entered commands. To minimize seek time, the MSC firmware changes the order in which commands are executed. (Seek time is the time needed by the disk drive to move the heads over the specified disk block.)

When the command is executed, the MSC firmware calculates the physical disk address of the requested block (file). The MSC then moves the disk heads over the specified block. If the command is a read, the data is read from the disk into RAM on the MSC and then transferred to the appropriate place in the 8560 memory. If the command is a write, the data is transferred from the appropriate place in the 8560 memory into RAM on the MSC Board and written to the disk.

When the data transfer is completed, the 80186 sends an interrupt to the LSI-11 informing TNIX that the block of data is now stored at the appropriate place.

Hardware Devices

The following text describes hardware devices accessed by the MSC operating firmware. The four hardware devices are: the Xebec S1410 Disk Controller, the Device Register, the WD2797 Flexible Disk Controller Device, and the Seven-Segment Display device. A short description of each hardware device follows.

The Xebec S1410 Disk Controller

The Xebec S1410 Disk Controller Board interfaces the MSC Board to the hard disk drive unit. The 80186 sends commands to the Xebec Disk Controller and receives data and status information. Section 10 of this manual provides a more detailed description of the Xebec S1410 Disk Controller Board.

Device Register

The Device Register is the hardware communications link between the 8560's LSI-11 and the MSC's 80186 processor. The Device Register is located on the MSC Board.

To read the Device Register contents, the 80186 performs a DMA operation on the 8560 bus. This is required because the 80186 cannot read the Device Register directly.

Any time TNIX generates a command buffer, TNIX stores the address of the first command buffer word in the Device Register located at address 777150 (octal).

The WD2797 Flexible Disk Controller Device

The WD2797 Flexible Disk Controller Device sends the 80186 data and status information to the 80186. The WD2797 (U5130) is described earlier in this section.

Seven-Segment Display

This is a write-only device and the information must be interpreted by the user. The seven-segment display is used mostly for diagnostic purposes. During normal operation, this display contains the number 5.

Software Data Structures

The MSC firmware also accesses four 8560 memory software data structures: 8560 data transfer buffers, 8560 termination buffer pointers, an Interrupt Vector Register, and the 8560 command buffers.

8560 command buffers are located in 8560 memory space. A slightly different formatted version called a device command buffer is stored in RAM on the MSC Board. The function of both command buffers is identical.

8560 Data Transfer Buffers

The 8560 data transfer buffers are located in the 8560 memory space. These transfer buffers store data before it is transferred to the MSC. Data transfer buffers also store data that has been read from a disk.

8560 Termination Buffer Pointers

Two 8560 buffer pointers store the addresses of terminated commands. When a command has been executed, the MSC informs TNIX with an interrupt that the command has been completed and terminated. The device driver (a software program) reads the buffer pointer for the address of the terminated command buffer.

Buffer Pointer 1 and Buffer Pointer 2 are located at 8560 memory locations 224 and 226, respectively. Both locations are used in alternating fashion to store addresses of terminated command buffers.

The Interrupt Vector Register

The Interrupt Vector Register is located at a fixed address in the MSC memory. This register identifies the vector to be asserted on the bus when the LSI-11 answers an interrupt from the 80186.

Interrupt Vectors

To communicate with the TNIX device driver routine, the MSC uses four interrupt vectors:

- TNIX disk access command acknowledge vector (location 234)
- Command termination vector 1 (location 270)
- Command termination vector 2 (location 274)
- Utility command termination vector (location 260)

The **command acknowledge vector** informs the device driver that the last command buffer address issued to the Device Register (location 777150) has been accepted and another command may be initiated.

The **command termination vector 1** also informs the device driver that Buffer Pointer 1 contains the address of a terminated command.

The **command termination vector 2** informs the device driver that Buffer Pointer 2 contains the address of a terminated command.

The **utility command termination vector** terminates all utility commands.

8560 Command Buffers

The MSC communicates with the 8560's LSI-11 through command buffers in the 8560 memory. A command buffer is a designated memory location that contains instructions for the 80186 to execute when the MSC accesses a disk. Command buffers are located in the lower 64K bank of 8560 memory.

TNIX generates eight 8560 command buffers in 8560 memory space. One buffer contains commands to access disks for normal read and write operations. The remaining seven command buffers provide utility functions for troubleshooting.

Error Codes

The MSC returns error status bytes to ODT (Octal Debugging Technique) or the console port after each command is executed successfully. The most significant bit (MSB) of each status byte indicates a fatal error. If the MSB is not set, the command was executed successfully although possibly only after several tries. If two codes are shown, they correspond to fatal and nonfatal errors of the same type.

Table 9-4 lists software interface error codes and their corresponding ODT and TNIX codes. Tables 9-5 and 9-6 list error codes for flexible disk errors and hard disk errors, respectively.

The "Error Code" column lists the hexadecimal error codes. The "ODT" column lists error codes in the octal format displayed when the DEC supplied ODT is used.

The TNIX column shows the octal error code that is returned to the 8560 console port. Note, however, that the console port displays only fatal errors.

Diagnostic Jumpers

The MSC Board has one diagnostic jumper. Refer to Section 3 of this manual for the default position of this jumper.

Table 9-4
Software Interface Error Codes

Error Code	ODT Code	TNIX Code	Explanation
84	1020XX	04	Parity error
85	1021XX	05	Invalid device number
88	1040XX	10	Invalid command code
9D	1164XX	35	Qbus timeout error

Table 9-5
Flexible Disk Errors

Error Code	ODT Code	TNIX Code	Explanation
91	1104XX	21	Drive not ready
92	1110XX	22	No track-zero signal detected
13,93	0114XX, 1114XX	23	Data overrun error
14,94	0120XX, 1120XX	24	CRC Error
19,99	0144XX, 1144XX	31	Missing ID field address mark
9B	1154XX	33	Attempting sector access beyond limits
9C	1160XX	34	Invalid flexible disk cylinder address
9E	1170XX	36	Write-protected disk
D4	1520XX	124	Disk block number too large

Table 9-6
Hard Disk Errors

Error Code	ODT Code	TNIX Code	Explanation
A1	1204XX	41	Invalid hard disk command
A3	1214XX	43	Disk drive not ready
A5	1224XX	45	Illegal head or cylinder address
26,A6	0230XX, 1230XX	46	Sector not found
27,A7	0234XX, 1234XX	47	Data error
AB	1254XX	53	Write fault
2D,AD	0264XX, 1264XX	55	DMA timeout during read operation
2F,AF	0274XX, 1274XX	57	DMA timeout during write operation
E1	1604XX	141	No spare sector on specified track
E3	1614XX	143	Disk access timeout
E4	1620XX	144	Disk block number too large
E5	1624XX	145	Bad format

MSC DIAGNOSTICS FIRMWARE

This section describes the diagnostic firmware used on the MSC Board. This firmware shares ROM space with the operating firmware. The power-up portion of the firmware is invoked each time a Qbus INIT signal is received. A set of "extended" tests is available for more comprehensive board evaluation.

Introduction

On BUSINIT (RESET), the diagnostic firmware performs a kernel test of the basic hardware, which evaluates the ROM, RAM and the CPU on the board. The LEDs display the status of each element of this test.

After completion of the kernel test, the user may invoke a set of extended tests by installing a normally-open pushbutton switch on P2061. Detection of a switch closure upon completion of the power-up tests selects the extended test mode. Control passes to the normal operating firmware if the extended test mode is not selected.

If the extended test mode is selected, a set of menus is displayed from which the user may select either a specific test or a group of related tests.

A terminal or printer may be connected to Printer Port LP2 to receive and display error and status messages.

Program Overview

This section describes the test groups in the diagnostic firmware package. Each test group is described with the selection menu for that level in the diagnostics. All test groups, except the kernel mode tests which are run by default at power-up, are selectable from the Test Selection Menu. The Test Selection Menu is displayed when a switch closure is detected after completion of the kernel tests.

Power-Up Sequence

At power-up, or assertion of the Qbus BUSINIT signal, the kernel tests are performed. These tests determine the integrity of the Processor, ROM, RAM, and the LED display. The kernel tests complete within two seconds after INIT and are explained later in this section.

Upon successful completion of the kernel test, the pushbutton switch connection is sampled. If no switch closure is detected, the LED displays a "5" and control passes to the normal mode firmware. If a switch closure is detected, the diagnostics Test Selection Menu is displayed.

Error Displays

LED Error Displays. Errors are generally designated by alternately displaying an identifier for the test detecting the error and an identifier for the test mode. Some tests display their identifier alternately with an error indication. This display occurs primarily during the kernel tests when a line printer/terminal connection is not assumed. Tests that do not detect errors display only the test identifier.

Printer Port 2 Error Displays. A line printer or terminal connected to Printer Port LP2 displays error information for a test after the test terminates. These messages are valid for the most recent failing pass of the test. The printer only displays error messages after test F5 (floppy mode line printer test) runs successfully.

Standard Form for Error Messages. The general form for an error message is:

Identifier for type of error information

```
xxxx xxxx xxxx xxxx  - expected
xxxx xxxx xxxx xxxx  - actual
xxxx xxxx xxxx xxxx  - mask
```

The first line of text typically contains a register identifier which specifies the location of the data values. In some cases, this indicates the type or location of the error, such as the SCSI data bus or the Qbus finite state machine.

The *expected* field contains the bit pattern anticipated from the specified location.

The *mask* field specifies which bit positions are significant in evaluating the *actual* field.

The *actual* field contains the 16-bit value read from the specified location.

For some displays, not all bits in the *actual* field will display meaningful information. (Refer to the board schematics to determine which bit values are significant.)

In determining the success or failure of a test, the *mask* field specifies the bits tested in the *actual* field. In general, the *actual* field is ANDed with the *mask* value and compared to the expected field value to determine test results; for example, only bits with a "1" in the *mask* field are tested.

For some tests, the identifier line contains the only meaningful information. The actual bit values are of little significance. The *mask*, *actual* and *expected* fields are all zeros for these displays.

The following exceptions exist in the interpretation of the data contained in the *mask*, *actual* and *expected* fields, as follows:

- The hard disk drive-ready tests identify the drive that failed the test but do not provide specific failure information.
- When a drive failure is detected, the controller returns an extended status block. When this occurs, the *expected*, *actual* and *mask* fields contain the first, second and third bytes, respectively, of the extended status block.

  The error summaries at the end of this section contain a list of possible error messages and causes. Refer to Tables 9-4, 9-5, and 9-6 for software error codes, flexible disk error codes, and hard disk error codes, respectively.

Test Selection Menu

The Test Selection Menu is entered when a switch closure is detected upon completion of the kernel tests. The LED successively displays a set of characters indicating the next lower level of possible selections, as reflected in Table 9-7.

Table 9-7
Test Selection Menu

Display Char	Test Group Selected
F	Floppy disk tests
H	Hard disk tests
E	Extended tests
L	Perform all tests (except extended)
‼	Return to next higher level (in this case, the normal mode firmware)

Each character is displayed for one second. If a switch closure is detected while a character is displayed, the decimal point on the LED lights, acknowledging the selection. The decimal point flashes on and off for a two-second period. If a switch closure is detected while the decimal point is lit, the Test Group Menu is selected for the indicated test group. The Test Selection Menu display is resumed if the decimal point is not lit during a switch closure.

Test Group Menus

The Test Group Menus are chosen from the Test Selection Menu. Either a single test or all tests in a group may be run.

The Test Group Menus operate in a manner similar to the Test Selection Menu. A set of characters indicates the selections available. Detection of a switch closure stops the scan at the current display. A second switch closure either restarts the menu scan or initiates the selected test, depending on whether or not the decimal point is lit.

Selection of the display of vertical bars ("‼") returns the user to the next higher level of menu.

Each test in a group is identified by a unique character. The RUN ALL TESTS mode is indicated by an "L" (Loop) on the LED display.

If a single test is selected, it repeats until another switch closure is detected, regardless of success or failure. This is the LOOP UNTIL RESET mode. Failure is indicated by the alternate display of the test group identifier and the test identifier with the decimal point lit. If a test runs with no errors, only its test identifier is displayed with the decimal point unlit.

All tests in a group are run when "L" is selected. If an error is detected, the identification character of the failing test is alternately displayed on the LED with the identifier for the test group. This error display method is also used by the LOOP UNTIL RESET mode. When all the tests in a group have completed without error, the display returns to the test selection mode. The RUN ALL TESTS mode may be terminated by a switch depression, returning to the subtest select menu for the current test group.

A failing test may be terminated by a switch depression. If floppy test F5 has run successfully, Printer Port 2 displays fault information after a switch depression terminates a looping test. This text is valid for the most recent test failure.

Test Descriptions

This section describes the kernel tests, the floppy mode tests, the SCSI interface tests, and the extended tests. It also details the individual tests in each major test group.

Kernel Tests

A BUSINIT (RESET) signal from the Qbus initiates the kernel tests. These tests, performed at every power-up or reset, verify such basic board functions as RAM, ROM, and the CPU, as well as the condition of the on-board, seven-segment LED display. The ROM and RAM tests determine if the system address and data buses are functioning properly and verify the chip-selects required for basic kernel functions. Both the ROM and RAM tests identify the device failing the checksum or data/addressing test, using a low-byte or high-byte indicator. (A low byte specifies the even-addressed bytes while a high byte refers to odd-addressed bytes.)

Table 9-8
Kernel Tests

Error Display	Name of Test	Key ICs	Function
None	LED segment		Verifies each segment of LED display lights
".1", alternately with "H" or "L"	ROM checksum	U4090 (High byte) U4060 (Low byte)	Verifies integrity of ROM contents
".2", alternately with "d" (data) or "A" (address) (display of "d"or "A" inverted inciates high byte failure)	RAM	U4040, (low byte RAM), U4080, U3090, U3100 (high byte RAM)	Verifies two 4K x 8-bit RAMs on Disk Controller
".3", alternately with identifier for failing test	CPU	80186	Verifies integrity of 80186 including timers, DMA controller and interrupt controller

The CPU test establishes whether the processor can successfully complete a sequence of operations, exercising its instruction set and integrated peripheral functions. If any section of the CPU test fails, the LED displays the identifying code for the CPU test and an indicator for that section such as arithmetic, logic, or stack operations.

If test faults are detected by the kernel tests, (with the exception of the LED display test), the decimal point lights in conjunction with the test identification number. If a failure is detected during the CPU, ROM or RAM tests, the test halts.

The LED test has no error indication since it cannot determine whether the segments actually did light.

The MSC Board will halt with an error display and will not begin normal operation if an error is detected during the kernel tests. If the tests complete without an error, the normal control firmware takes control and the display is blanked.

The kernel tests do not provide for the display of error information through Printer Port LP2.

The kernel tests and their error indicators are shown in Table 9-8.

Floppy Mode Tests

This group of tests checks the Qbus interface logic, interrupt logic, Qbus protocol state machine, and Qbus addressing capability. It also tests some basic characteristics of the LSI floppy disk controller and the disk drive. The Qbus tests require the MSC Board to access the Qbus to loop signals through, providing readback of on-board buses.

These tests are manually selected after the kernel mode tests are complete, using a normally-open pushbutton switch. Detection of a switch closure displays the Test Selection Menu. The menu display for the floppy mode tests is an "F". A switch closure while the "F" is displayed halts the menu scan and the decimal point flashes on and off for a two-second period. Depression of the switch again while the decimal point is lit invokes the menu display for the floppy mode tests. If a switch depression is detected while the decimal point is not lit, the Test Selection Menu scan resumes.

A list of the floppy mode tests and their respective display codes is reflected in Table 9-9.

Table 9-9
Floppy Mode Test Selection Menu

Display Code	Test Selected
0	Qbus finite state machine test
1	Qbus interface Din/Dout bus readback
2	Qbus interface address test
3	Qbus interrupt 4 logic
4	Qbus timeout logic
5	Terminal test (write to LP2 Port)
6	FDC Registers write/read
7	Status Register readback
8	FDD restore (seek track 0)
L	RUN ALL TESTS
‼	Return to next higher menu level

Any test selected from 0 to 8 runs repeatedly. The first error encountered alternately displays the test mode identifier (an "F" for Floppy tests) and the test number. If a test fails, the decimal point lights simultaneously with the test identifier. The success/failure indication is updated after each test pass.

A second switch depression halts the test currently running after the present test pass completes.

If option "L" is selected, all tests in the floppy menu run in succession. The test currently running is identified on the LED display. When the last test completes, the menu is again displayed.

If a failure occurs during this sequence, the failing test runs repeatedly, alternately displaying its identification character with the test mode identifier. The decimal point will indicate pass/fail status for successive passes.

Selection of the "::" display returns the user to the Test Selection Menu.

Floppy mode tests and their error indicators are shown in Table 9-10.

Table 9-10
Kernel Tests

Error Display (Printer Port Disply)	Name of Test	Key ICs	Function
".0", alternately with "F" (Standard error message for Qbus Status Register)	State machine	U4160, U4130, U3160, U2160, U4170, U4125	Verifies state transfer table for Qbus machine
".1", alternately with "F" (Standard error message for Qbus Status Register)	Din/Dout register readback	U5010, U5030, U5120, U5040, U4145	Verifies integrity of Qbus Din/Dout bus interface circuitry
".2", alternately with "F" (Standard error message for Qaddrs Register)	Qbus address bus	U5050, U5060	Verifies MSC Board can assert Qbus addresses
".3", alternately with "F" (Standard error message for Qbus Status Register or Vector Register)	Interrupt 4 logic	U4115, U5090, U4175	Verifies assertion of Interrupt 4
".4", alternately with "F" (Standard error message for Qbus Status Register)	Qbus timeout logic	U1080, U5170, U4170	Verifies integrity of Qbus timeout logic
".5", alternately with "F"	Terminal	Miscellaneous Qbus circuitry	Verifies actual data transfer on Qbus
".6", alternately with "F" (Standard error message for Qbus Status Register; data fields all zeros)	Device Register readback	U4010, U4120, U3010, U3020, U1080	Verifies the integrity of the MSC Device Register and Device written flag
"7", alternately with "F" (Standard error message for FDC Track Register, FDC Sector Register or FDC Data Register)	FDC register	U5130	Verifies that processor can access internal registers of FDC IC
".8", alternately with "F" (Standard error message for Qbus Status Register or Disk Status Register)	Status ports readback	Latches, buffers	Verifies integrity of Qbus and disk status latches
".9", alternately with "F" (Standard error message for Qbus Status Register or Disk Status Register)	Floppy drive restor	U5130, U6120, U6110, U5120	Verifies flexible disk drive seeks track 00

SCSI Interface Tests

The SCSI interface tests determine the integrity of the controller interface for the hard disk drive. One or all of the tests in this group may be selected from the SCSI Test Selection Menu as reflected in Table 9-11.

Table 9-11
SCSI Test Selection Menu

Display Code	Test Selected
0	SCSI Bus RESET logic
1	SCSI Bus control signals
2	SCSI bus poll
3	Disk controller internal diagnostics
L	RUN ALL TESTS
!!	Return to next higher menu level

SCSI interface tests and their error indicators are shown in Table 9-12.

Extended Tests

These tests provide a means of troubleshooting for both manufacturing and service support. Extended tests may only be run individually. The RUN ALL TESTS mode is not available.

These tests provide debugging capability. They also provide for tests that are not included in the test groups because they require either an extended length of time to run (the hard disk diagnostics), or they require additional hardware (the floppy exercise tests). These tests are intended to provide a little broader board stimulus than the dedicated tests in the other test groups.

Table 9-13 reflects a list of tests available.

Table 9-13
Extended Test Selection Menu

Display Char	Subtest Selected
0	RAM write/read scan
1	Qbus memory size
2	Read track 0 (floppy)
3	Read track 76 (floppy)
4	Hard disk diagnostic (can take up to 25 seconds)
5	Read Qbus (location 0177777)
6	Write Qbus (location 0177777)
!!	Return to next higher menu level

Extended tests and their error indicators are shown in Table 9-14.

Table 9-12
SCSI Interface Tests

Error Display (Printer Port Display)	Name of Test	Key ICs	Function
".0", alternately with "H" (Standard error message where all bit fields equal zeros)	SCSI bus RST	U2110, U4165B	Verifies that the 80186 can detect SCSI bus Reset assertion
".1", alternately with "H"(Standard error message for SCSI data bus or Disk Status Register)	SCSI bus control	U2110, U2120, U2150, U2160	Verifies the SCSI bus signals
".2", alternately with "H" (Standard error message for SCSI Status Register, data bus or controller)	Hard disk controller Diags	Hard disk controller	Verifies operation of internal diagnostic routines in hard disk controller
".3", alternately with "E" (Standard error message for SCSI bus or drv0 not ready when bits equal 00)	SCSI bus poll		Verifies access to a system disk drive

Table 9-14
Extended Tests

Error Display (Printer Port Display)	Name of Test	Key ICs	Function
None	RAM read/write scan	Data buffers	Low level RAM write/read (no verification)
"1", alternately with "E" (Standard error message for Ext Addr Register)	Qbus memory bank selection	U5070, U6050, U5110	Verifies each bank of Qbus memory and reports size (xxxxK bytes)
"2", alternately with "E" (Standard error message for FDC Status Register)	Floppy read track 00	U5120 and interface circuitry	Verifies floppy drive and interface circuitry
".3", alternately with "E" (Standard error message for FDC Status Register or data read error)	Floppy drive track 76	U5120	Verifies write/read function flexible drive
".4", alternately with "E" (Standard error message for drive n not ready (field equals 00) or drv n (n is the drive tested)	Fixed disk diagnostics	Controller-drive interface	Verifies access to and formatting of fixed disk drive(s)
None	Read Qbus 0177777	Many	Verifies read operation of Qbus interface circuitry
None	Write Qbus 0177777	Many	Verifies write operation of Qbus interface circuitry

Printer Port Error Display Summary

A list of possible error messages, together with a description of each, follows. These messages appear upon termination of a failing test.

Qbus status reg. The bit fields for *actual* and *expected* refer to the Qbus Status Register composed of U1080, U1040, U4110, U1090.

Vector reg. The bit fields for *actual* and *expected* refer to the Qbus Vector Register U4030.

Disk status reg. The bit fields for *actual* and *expected* refer to the Disk Status Register U3130 and U1060. This message also refers to the SCSI status control bus since it is mapped into upper 8 bits of the Disk Status Register. The Mask Register allows differentiating.

FDC track reg. The bit fields for *actual* and *expected* refer to the Track Register internal to floppy controller U5130.

FDC sector reg. The bit fields for *actual* and *expected* refer to the Sector Register internal to floppy controller U5130.

FDC status reg. The bit fields for *actual* and *expected* refer to the Status Register internal to floppy controller U5130. The bit field actual represents the state of the floppy disk system known by the controller. The bit position definitions are as follows:

bit 0: 1 => controller BUSY status

bit 1: 1 => INDEX hole under detector or DATA REQUEST depending on command in process

bit 2: 1 => TRACK 0 or LOST DATA depending on command in process

bit 3: 1 => CRC ERROR

bit 4: 1 => SEEK ERROR or RECORD NOT FOUND depending on command in process

bit 5: 1 => HEAD LOADED or RECORD TYPE in read operation

bit 6: 1 => disk WRITE PROTECTed

bit 7: 1 => drive NOT READY

FDC data reg. The bit fields for *actual* and *expected* refer to floppy controller Data Register U5130 which is accessed with address lines 0 and 1 at logic 1.

Din/Dout bus. This message appears when errors occur during readback of the Din/Dout bus. This is accomplished by logically connecting the Din/Dout bus through the Qbus drivers (U6010, U6020, U6030, U6040) and reading from the Din Registers (U5010, U5030) the data pattern written to the Dout Registers (U5020, U5040).

Qaddrs reg. This message implies that an error was detected while testing the Qbus Address Register (U5050, U5060). The Address Register is read back by logically connecting it to the Din Registers (U5010, U5030) through the Qbus transceivers.

Qbus FSM. This message suggests an error in the Qbus control FSM. The *actual* field contains the pattern read back from the Diagnostic Register, U2160. The *mask* field describes the set of bits actually compared.

Dev Reg. This message suggests a problem with the Qbus Device Register (U4010, U4020). This register is tested by writing through the Qbus and reading it back.

SCSI data bus. This test suggests an error while testing the SCSI data bus. This bus is tested by writing it a walking one pattern, followed by a walking zero pattern. The pattern written is recorded in the *expected* field. The pattern read back is recorded in the *actual* field. This bus is 8 bits wide and is right justified in the record fields.

xxxxK bytes memory detected. This message reflects the number of contiguous 64K memory banks found to be unique. A bus timeout indicates the end of available memory. This number should be compared with the amount of memory known to exist in the system. A mismatch between this value and the system memory size might occur as the result of a problem with the Extended Address Register (U5070) or the Qbus driver associated with the address lines from the Extended Address Register (U6050, U6080).

Bus timeout. This message is printed by the Device Register test indicating that a Qbus timeout occured while running patterns on the Device Register.

MSC diagnostics. This message, printed by the terminal test routine, is used to determine if any other messages should be printed.

print error. This message indicates that the transmitter on Printer Port LP2 took longer than 10 ms to return 'transmitter empty' status. This happens if there is no printer connected. This message may also appear if a printer is connected whose buffer becomes full and therefore unable to accept additional characters until some are printed out.

drv0 not ready. This message implies that hard disk drive 0 did not indicate 'ready' status when polled. This may be due to cable connections from the disk controller to the drive, drive not powered-up, or drive not up to speed (can take up to 25 seconds after power-up).

SCSI BSY timeout. This message indicates that a timeout occurred while communicating with the hard disk controller. The timeout limits the length of time for the complete communication process, (sending command, returning data and status). The timeout does not begin until the MSC Board has control of the bus and the target selection process is completed. This may indicate a problem with the controller.

target select timeout. The target did not respond within the 300 ms time limit. Verify that a hard disk controller exists at bus address "5".

SCSI reset interrupt fault. No interrupt was detected after asserting the SCSI reset line. The 80186 INT0 is used to detect the interrupt. This is generally caused by the SCSI RESET line sticking or inverter U4165B not working.

SCSI arbitration timeout. A timeout occured while waiting for the SCSI state machine (U2130 and related logic) to gain control of the SCSI bus.

lost arbitration. A higher priority device took control of the SCSI bus during the arbitration process. If there are no other masters on the bus, and the SCSI CONTROL test passed (E1), a problem may exist in the SCSI control logic (U2130 and related logic).

Ext Addrs Reg bank interdependence. One of the Qbus memory banks appeared to overwrite another while testing the Extended Address Register (U5070). This may be due to a stuck or shorted address line.

data read err. This message is generated by the floppy write/read test. It indicates that the information read back from track 76 sector 26 is different from what was written. A different data pattern is written each time this test runs. This may indicate a write gate assertion or write data problem (U6120).

disk controller fault. This message indicates that the hard disk controller failed its internal diagnostics. These diagnostics test its processor, data buffers, error correction circuitry, and internal RAM. The controller was healthy enough, however, to communicate successfully on the SCSI bus.

drive 0. This message indicates that hard disk drive 0 failed the drive diagnostic tests. This may be due to the disk's not being formatted, having crashed, read data separation problems in the controller, or cabling problems.

drive 1. This message indicates that hard disk drive 1 failed the drive diagnostic tests. This may be due to the disk's not being formatted, having crashed, read data separation problems in the controller, or cabling problems.

drv 1 not ready. Hard disk drive 1 did not return 'ready' status when polled. This may be due to cabling problems, the drive not powered up, the drive not up to speed or only having one drive (drive 0) in the system.

LED displays

The seven-segment LED displays provide a rough indication of possible problems. These displays are used whether or not a display device is connected to Printer Port LP2. In order to remove some of the ambiguity from the test displays, the test group identifier is alternately displayed with the test identifier for the user selected tests. The kernel mode power-up tests display an error type identifier alternately with the test identifier. In all cases the decimal point is used to indicate that an error was encountered on the most recent pass of the test. For the user selected tests, it is possible to have the decimal point light, then go out, indicating that the test now passes. The kernel tests do not repeat a test, and the error displays will always have the decimal point lit while displaying the test identifier.

The following displays are shown with the alternately displayed characters on either side of a "/". Decimal points are shown where they appear if appropriate. The character to the left of the "/" is the display while the test is running.

.0/F: the floppy group state machine test

.0/H: the hard disk group SCSI reset test

.0/E: the extended test group RAM scan

1/.x: the kernel group ROM test

"x" may be:

.d indicating failed data test low byte RAM (U4040)

.A indicating failed address test low byte RAM (U4040)

.p indicating failed data test high byte RAM (U4080)

.U indicating failed address test high byte RAM (U4080)

.2/F: floppy group Qbus interface address bus

.2/H: hard disk group hard disk controller internal diagnostics

.2/E: extended test group raw read track 00 (requires formatted floppy in drive)

3/.x: kernel group CPU test

"x" may be:

.L indicating failed low byte ROM checksum (U4060)

.H indicating failed high byte ROM checksum (U4090)

.1/F: the floppy group Dout/Din bus test

.1/H: the hard disk group SCSI bus lines test

.1/E: the extended test group Qbus memory sizing test

2/.x: the kernel group RAM test

"x" may be:

.a indicating byte wide register tests

.b indicating word wide register tests

.c indicating byte wide memory operations

.d indicating word wide memory operations

.g indicating stack operations

.h indicating interrupt operations

.n indicating flag operations

.o indicating string operations

.r indicating timer operation

.u indicating interrupt controller operation

.y indicating DMA operations

.3/F: floppy group interrupt 4 test

.3/H: hard disk group SCSI bus drive 0 ready test

.3/E: extended test group write/read track 76 (floppy)

.4/F: floppy group Qbus timeout test

.4/E: extended test group hard disk diagnostic test

.5/F: floppy group Printer Port LP2 communication test

.5/E: extended test group Qbus read stimulus

.6/F: floppy group Device Register test

.6/E: extended test group Qbus write stimulus

.7/F: floppy group Floppy Controller Register test

.8/F: floppy group Status Register test

.9/F: floppy group floppy drive track 0 test

.L: F/H test groups, top menu—loop on tests

.!!: Return to next higher menu

.u: could come from anywhere—unexpected interrupt received.

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THE XEBEC S1410 DISK CONTROLLER

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Section 10

THE XEBEC S1410 DISK CONTROLLER

INTRODUCTION

The Xebec S1410 Disk Controller controls the operation of up to two 5 1/4-inch Winchester-type disk drive units. The S1410 Disk Controller uses the Shugart Associates System Interface (SASI).

Functional Organization

Figure 10-1 is a simplified block diagram of the functional organization of the controller. The major functional blocks are as follows:

1. The host interface connects the internal data bus to the host adapter.
2. The processor monitors and controls operation.
3. The state machine controls and synchronizes operations.
4. The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected disk drive. SERDES converts serial data from the selected disk drive to parallel data and places it on the internal data bus.
5. The data separator makes required conversions of NRZ data to MFM data and vice versa.
6. The selector buffer handles data transfers between the disk and the host computer to prevent data overruns.

Diagnostic Jumpers

The Xebec S1410 Disk Controller contains jumpers and straps. Refer to Section 3 of this manual for the function and default positions of the jumpers and straps for the Xebec S1410 Disk Controller Board.

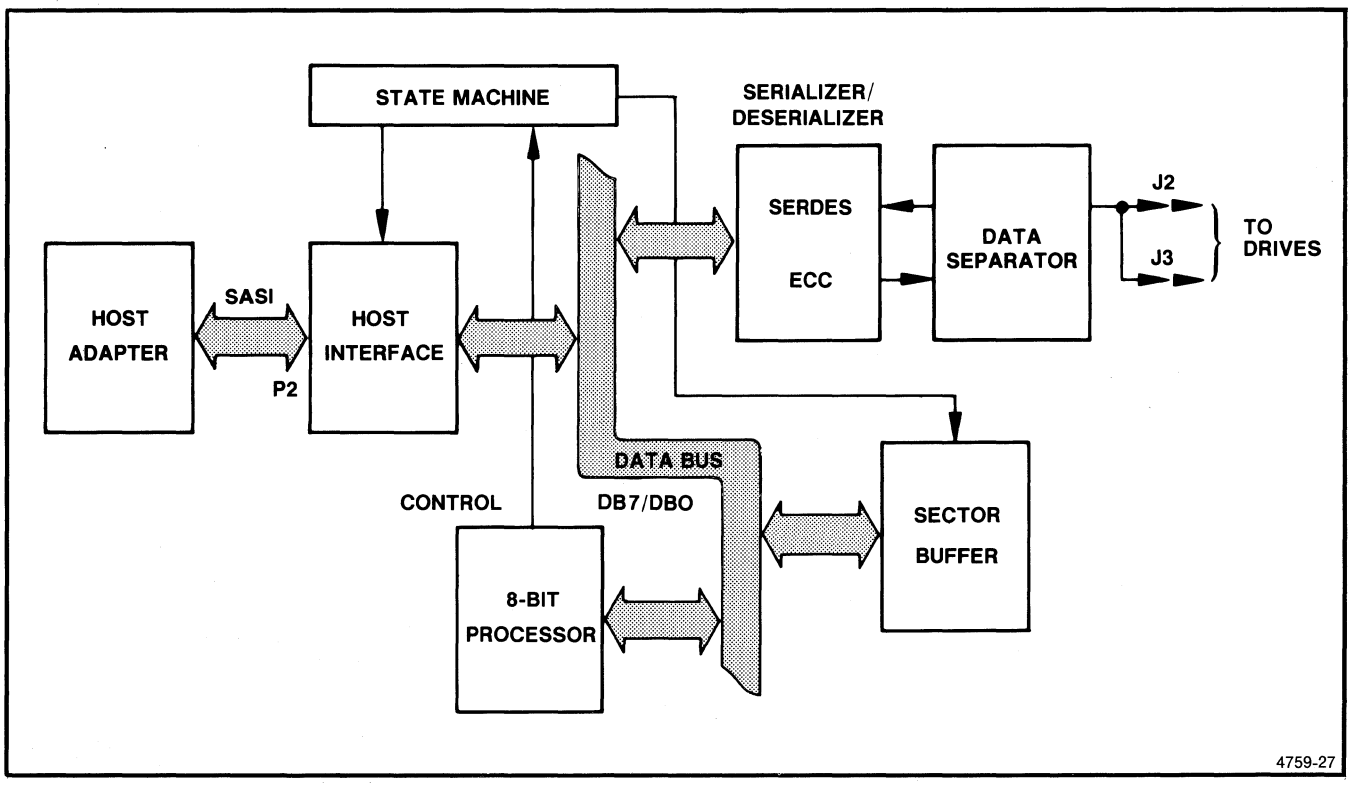

Fig. 10-1. Xebec S1410 Disk Controller block diagram.

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THE DISK DRIVES

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Section 11

THE DISK DRIVES

INTRODUCTION

The 8560 Series MUSDU provides up to approximately 80M bytes of nonvolatile memory. The vehicles for this storage are a double-sided, double-density flexible disk drive and Winchester-type hard disk drives.

THE FLEXIBLE DISK DRIVE

The 8560 flexible disk drive is a Qume Corporation QumeTrak 242. This unit uses standard removable 8-inch flexible disks.

This drive provides storage under these standards:

- 0.5M bytes of storage capacity on a double-sided, single-density disk
- 1M bytes of storage capacity on a double-sided, double-density disk

The QumeTrak 242 drive has a two-sided head/carriage assembly with two ceramic read/write heads that provide a track-to-track access time of 3 ms.

For additional information, see the *QumeTrak 242 Maintenance Manual*, available from Tektronix, Inc.

THE WINCHESTER-TECHNOLOGY HARD DISK DRIVE(S)

The 8560 Series MUSDU is equipped with one or two hard disk drive units. The type of hard disk drive installed depends on the particular development system selected.

The Seagate ST419 Disk Drive

The Seagate ST419 is a 15M-byte hard disk drive. The ST419's formatted capacity is 15M bytes. The heads, actuator and disks are protected by an aluminum enclosure. Air is circulated through the clean area by a spindle pump. The air flow is directed through a 0.3 micron absolute filter. Thermal isolation of the motor assemblies from the disk enclosure results in a very low temperature increase within the disk enclosure. This low temperature increase provides read and write operations to be performed immediately after power-up without a thermal stabilization delay.

The Seagate ST419 utilizes 5 l/4-inch nonremovable disks as storage media.

The Seagate ST419 interfaces with an intelligent Xebec S1410 Disk Controller which can control the operation of up to two 5 l/4-inch Winchester-type disk drives. The S1410 Disk Controller uses the Shugart Associates System Interface (SASI) to communicate with the 8560 bus.

Servicing the disks inside the clean area of the Seagate ST419 is performed only by the manufacturer. If your disk drive needs servicing, you will have to remove it from the 8560 MUSDU. Service information and instructions for removing the Seagate ST419 disk drive are given in Section 15 of this manual. Detailed information on the Seagate ST419 is provided in the *ST406/412/419 Microwinchester Service Manual*, which is available from Tektronix, Inc.

Additional information regarding the Xebec S1410 Disk Controller is provided in Section 10 of this manual.

The Micropolis Model 1304 Disk Drive

The Micropolis Model 1304 is a 40M-byte hard disk drive. The 1304's formatted capacity is 40M bytes. The disk drive unit consists of an inner and outer die casting separated by shock isolators. The inner casting contains the read/write heads, disks, and voice coil rotary motor. Air is circulated through the clean area by the rotation of the disks. The air flow is directed through a 0.3 micron absolute filter. The shock isolators protect the inner casting from mechanical shock.

The Micropolis Model 1304 has a direct drive, brushless dc motor that rotates up to four sealed disks.

The Micropolis Model 1304 is interfaced with an intelligent Xebec S1410 Disk Controller, which can control the operation of up to two 5 1/4-inch Winchester-type disk drives. The S1410 Disk Controller uses the Shugart Associates System Interface (SASI) to communicate with the 8560 bus.

Servicing the disks inside the clean area requires that you remove the drive unit completely from the 8560 enclosure. The disk drive is serviced by the manufacturer only.

Service information and instructions for removing the Micropolis Model 1304 disk drive are given in Section 15 of this manual. Detailed information on the Micropolis Model 1304 is provided in the *Micropolis 1300 Series Rigid Disk Drive Maintenance Manual*, available from Tektronix, Inc.

Section 12
POWER SUPPLY

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Section 12

POWER SUPPLY

INTRODUCTION

This section describes the 8560 Series power supply and provides procedures for troubleshooting the supply. The material in this section consists of:

- A functional description of the 8560 power supply.
- A troubleshooting guide for the 8560 power supply.
- A bring-up procedure to return a repaired power supply to operation.

NOTE

All references to the 8560 power supply include the 8560 and 8561 (SN B100000 and above) and the 8562.

FUNCTIONAL DESCRIPTION

This subsection describes the circuitry of the 8560 power supply and is divided into two parts:

- A general description of an inverter-type supply.
- A description of the dc output circuitry in the 8560 power supply.

Inverter-Type Supply Description

The 8560 power supply is an inverter-type supply. The power supply provides four dc voltages (+5 V, +12 V, -12 V, and +24 V) generated in four steps:

1. The incoming ac line voltage is rectified and filtered into high voltage dc.
2. The high voltage dc powers an ultrasonic oscillator called an inverter.
3. The output of the inverter is fed to an isolation transformer.
4. The waveform at each transformer secondary is rectified and filtered into low voltage dc.

The four steps are illustrated in the block diagram in Fig. 12-1.

DC Output Circuitry

The output voltages are regulated by control circuitry that feeds information from the output rectifiers and filters back to the inverter. Three of the four output voltages (+12 V, -12 V, and +24 V) must have additional regulation; only the +5 V output can be adequately regulated by controlling just the inverter. This additional regulation is performed by the secondary regulators. The +12 V and +24 V secondary regulators are controlled by the same reference voltage that controls the +5 V output. The -12 V secondary regulator's reference is internal to the regulator. All of the control circuitry is powered by a ±15 V supply, which is separately derived from the incoming ac line.

Protection circuitry monitors the voltage outputs and the inverter and shuts the supply down when fault conditions occur. Three types of faults external to the supply can shut the supply down:

- Line voltage below about 85 V will shut down the supply until the line voltage rises above 90 V.
- Overcurrent or overvoltage on any of the power outputs shuts down all of the outputs for about 1 second. The supply then tries to restart every 1 to 1.5 seconds until the fault is corrected or until the supply is turned off.

Figure 12-2 is a block diagram of the 8560 power supply.

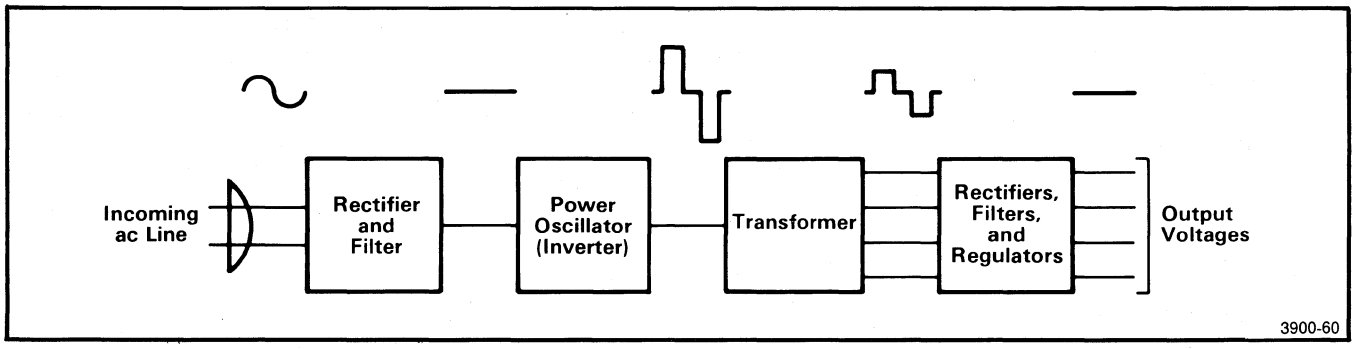

Fig. 12–1. Inverter-type supply block diagram.

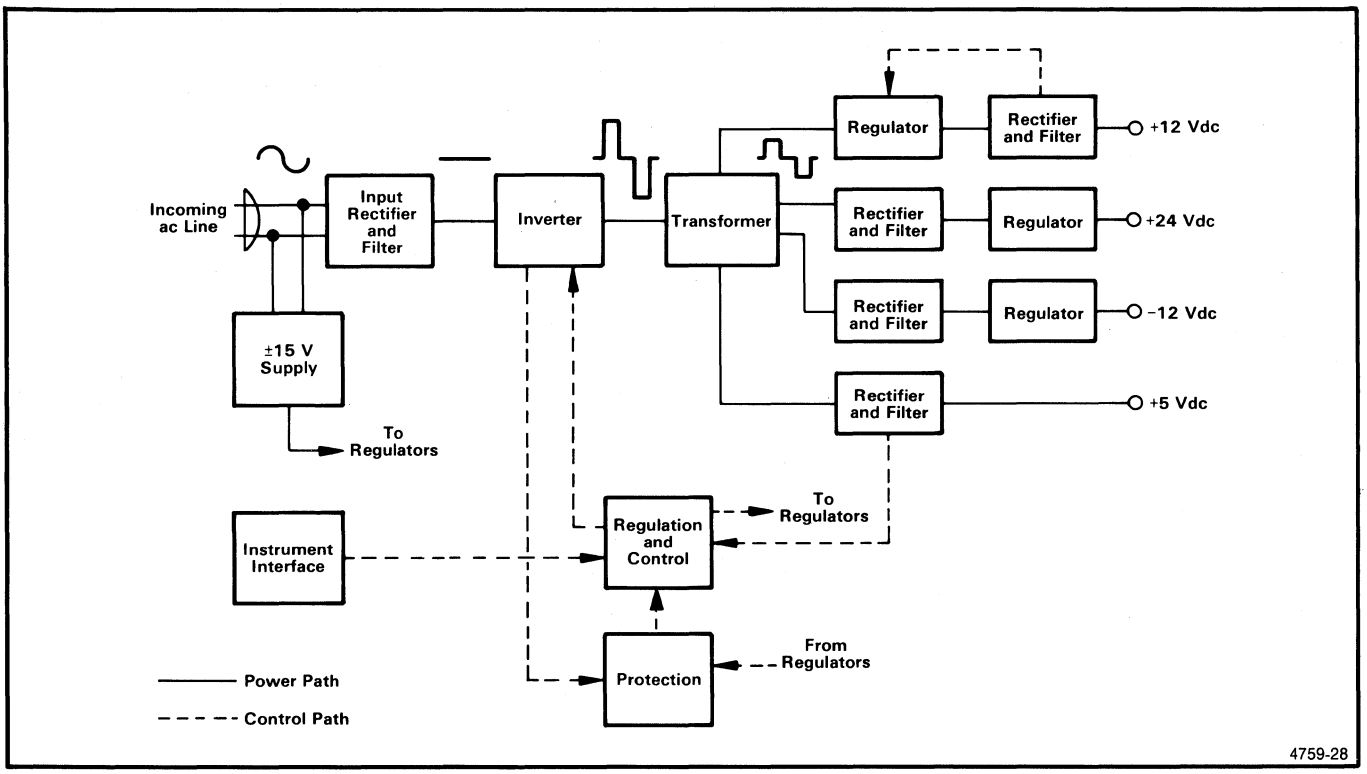

Fig. 12-2. 8560 power supply block diagram.

TROUBLESHOOTING GUIDE

This troubleshooting guide enables you to locate and repair most failures that occur in the 8560 power supply. The guide is divided into two main parts:

1. Catastrophic failures
2. Non-catastrophic failures
   - Determining why the supply won't turn on
   - Troubleshooting the +12 V secondary regulator
   - Troubleshooting the +24 V and -12 V secondary regulators
   - EMI test procedure

To troubleshoot the supply, follow the appropriate procedure in this troubleshooting guide. If you are troubleshooting a catastrophic failure, proceed to the bring-up procedure, later in this section, after you have repaired the problem.

Equipment Required

The following equipment is required to perform the tasks described in this troubleshooting guide:

Equipment	Recommended Type
Soldering iron/solder	800° F tip temperature/ 63% tin, 37% lead, rosin core
Needle-nose pliers	Sturdy, with plastic grips
Screwdriver	Phillips for #6 and #2 screws
Voltmeter/diode meter	Fluke Model 8030A or equivalent
Oscilloscope	TEKTRONIX 465 or equivalent

Jumpers

Refer to Section 3 of this manual for detailed information on all power supply jumpers.

Catastrophic Failures

Catastrophic failures generally occur while the instrument is up and running. Failures of this type cause the instrument lights to go out and the line fuse to blow. These symptoms are sometimes accompanied by a burning odor or popping noises.

Catastrophic failures most often originate in the high-voltage switching circuit of the main inverter. This circuit is located on the Inverter Board, which is one of three plug-in circuit boards in the 8560 power supply.

In the following inspection and repair procedure, the most likely causes of failure are investigated first.

1. Make sure the 8560 is disconnected from the primary power source.

WARNING

Use insulated tools and probes at all times and observe the supplementary cautions contained in the text. Stored charge in the large capacitors of the power supply can cause severe burns and/or electric shock even when the supply is turned off.

2. To gain access to the Inverter Board, remove the fan housing at the rear of the 8560. Remove the two screws closest to the rear panel on the housing's left side, and the six screws that secure the housing to the rear panel. Disconnect the two wires connected to the fan and set the fan housing aside.
3. Three plug-in circuit boards are now visible through the opening that the fan housing normally covers. The Inverter Board is the lowest of these three boards. To remove the Inverter Board, grasp the left side of the board firmly with a pair of insulated needle-nose pliers (see Fig. 12-3), and pull the board out.

WARNING

Do not touch the metal on the pliers; high voltage may be present on the board while it is installed. Keep away from grounded objects while pulling the board out. After removing the board, allow five seconds for the capacitors on the board to discharge before handling the board.

WARNING

Whenever the 8560 is connected to a power source and the unit's power switch is on, use caution in the area of the Inverter Board. A 200 Vdc potential exists on the screw in the left-hand corner of the board. Refer to Fig. 12-4 for the location of this screw. The same 200 Vdc potential may exist on the shield below the board if the insulating coating on the shield is damaged. Damaged shields should be replaced immediately.

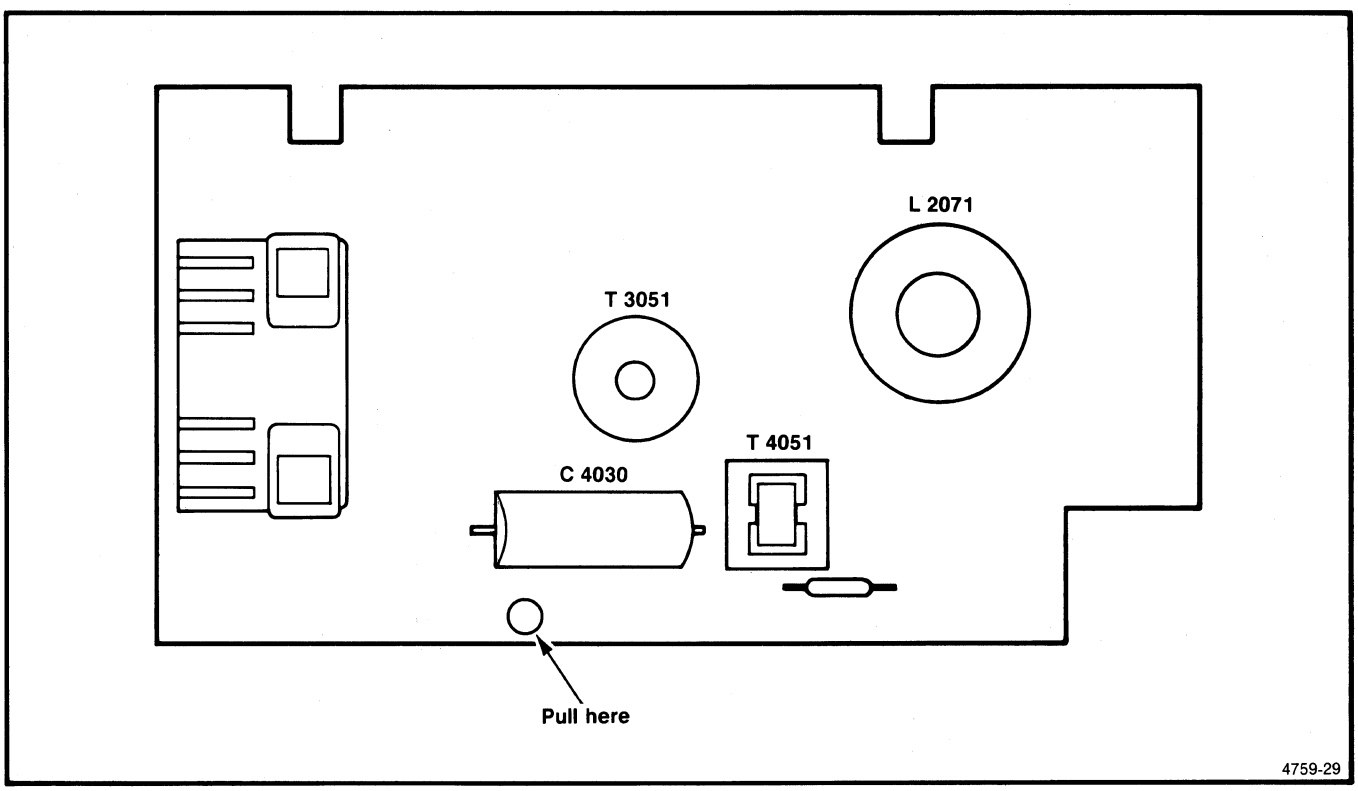

Fig. 12-3. The Inverter Board.

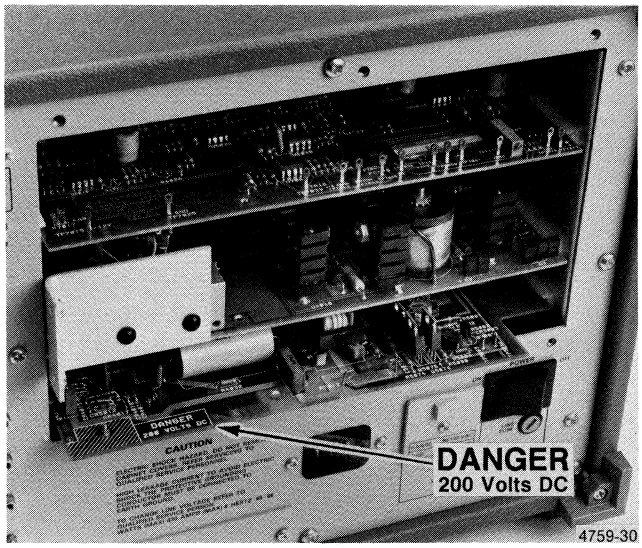

Fig. 12-4. The Inverter Board—200 Vdc.

4. Notice the finned heatsink on the left side of the Inverter Board. The two transistors (Q3010 and Q2010) on the finned heatsink are the main inverter's high-voltage switching components. Look for obvious signs of failure, such as cracked transistor cases or charred circuit board.

NOTE

While performing the rest of the procedure, refer to the power supply Inverter Board schematics at the rear of this manual.

5. If the failure appears to be in the main inverter, the following components (listed in descending order of probability) may have failed:
   - High-voltage switching transistors, Q3010 and Q2010
   - Turn-off capacitors, C4019 and C1019
   - Turn-off transistors, Q4011 and Q1010
   - Drive transistors, Q5074 and Q5075
   - Bleeder resistors, R4014 and R1016

   If either Q3010 or Q2010 is obviously damaged, remove the bad transistor(s). Be careful when removing these transistors. The two screws holding down the collector tabs of these transistors are the only secure mechanical connection between the heatsink assembly and the circuit board.

   Even if Q3010 or Q2010 appear undamaged, check the components in-circuit with any diode meter having a 1 mA measuring current. Forward base-collector and base-emitter voltages for good transistors are between 400 mV and 600 mV. See Fig. 12-5 for pinouts. Remove any transistor that shows a bad junction voltage.

After Q3010 and Q2010 have been removed, all of the other components listed at the beginning of step 5 can be checked with the diode meter. The capacitors should read between 1300 mV and 1600 mV in either direction, although a resistor failure or turn-off transistor failure could affect these readings. The turn-off transistors should show forward junction voltages between 400 mV and 600 mV. The bleeder resistors should read between 900 mV and 1100 mV in either direction. The drive transistors should eventually read between 400 mV and 600 mV when the positive lead of the meter is connected to the source and the negative lead is connected to the drain. With the leads reversed, the reading should eventually rise to more than 1999 mV. ("Eventually" means that the meter may take a few seconds to charge up the capacitors in parallel with the component being measured.)

Replace any of the components that seem to be faulty. Rebuild the heatsink assembly. (Make sure all parts are present, including the plastic inserts and rectangular aluminum washers.) Make sure there is heatsink compound under the transistors.

6. Proceed to the bring-up procedure, later in this section.

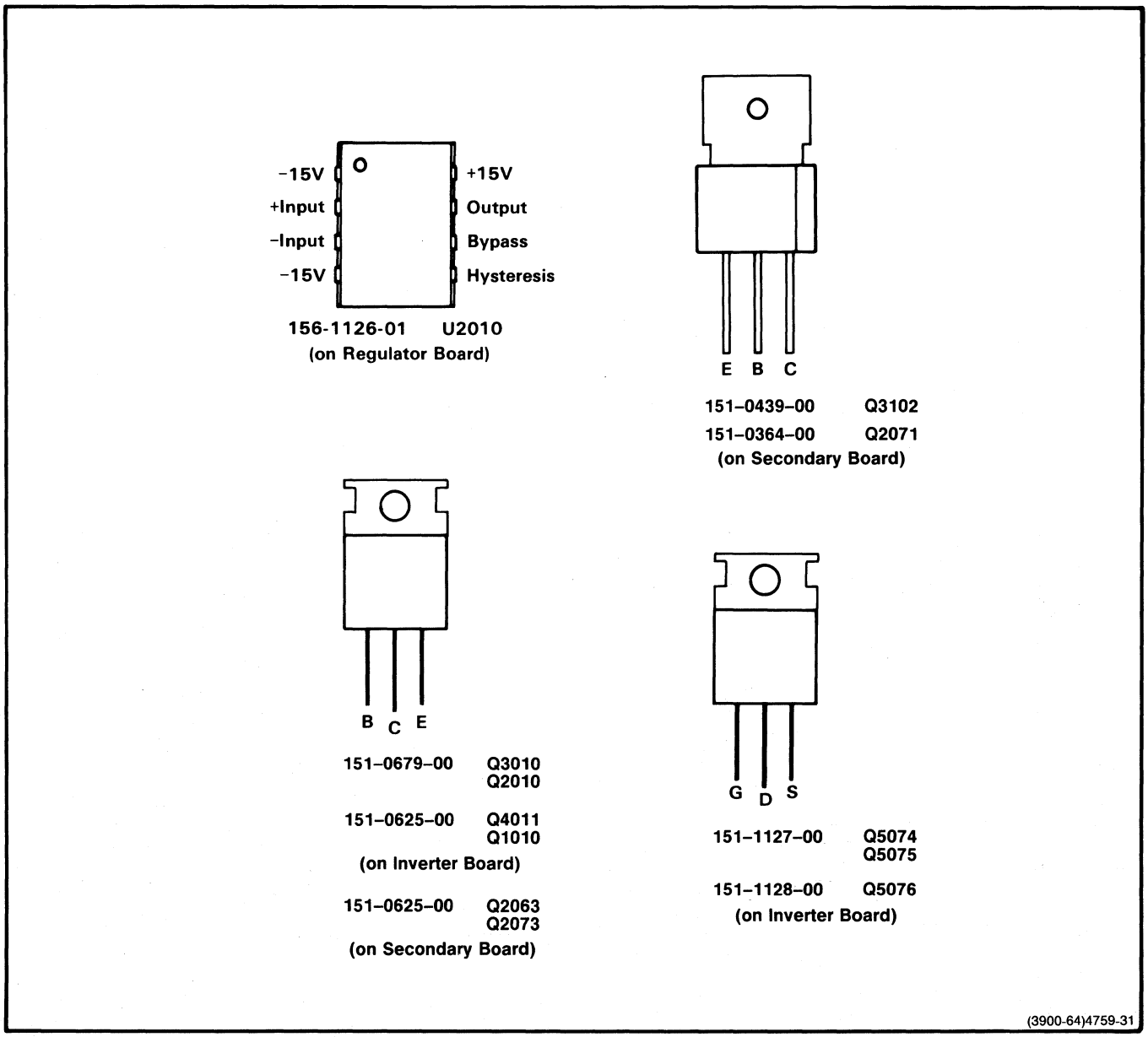

Fig. 12-5. Semiconductor component pinouts.

Non-Catastrophic Failures

The two most common non-catastrophic failures are failure of the supply to turn on and failure of a secondary regulator to produce the correct output voltage. This part of the troubleshooting guide is organized as follows:

- Determing why the supply won't turn on
- Troubleshooting the +12 V secondary regulator
- Troubleshooting the +24 V and -12 V secondary regulators

Follow the appropriate procedure until you've discovered and repaired the problem. Then, power up the system to verify that you have completely repaired the supply.

The Supply Won't Turn On

The 8560 power supply has many different kinds of fault sensing and protection features. As a result, any of a number of things can prevent the supply from coming up when both front and rear panel power switches are turned on.

If the AC ON light on the front panel remains off, the line fuse is probably open, indicating one of the following possibilities:

- A catastrophic failure has occurred in the supply. See "Catastrophic Failures," earlier in this section.
- Your 8560 is configured for a 115 V line, but is connected to a 230 V line. See "Selecting the Proper Primary Voltage" in Section 19 of this manual.

If the AC ON light is illuminated but the 8560 doesn't power up when you turn on the front panel DC switch, the following procedure should reveal the source of the problem.

NOTE

If the front panel switch is on when the rear panel switch is turned on, the AC ON light will illuminate immediately but the instrument won't power up for about a second. This delay is entirely normal.

Procedure.

1. Remove the two top cover retainers at the rear of the mainframe and slide off the top cover. Locate the power supply top shield, which is behind the hard disk drive(s).

WARNING

Use extreme caution once you have removed the power supply top shield. Dangerous voltages are present underneath the top shield.

WARNING

Be careful to keep fingers and other objects out of the power supply fan blades. The fan housing has no protective covering from the inside of the supply.

Remove the four screws that secure the shield and lift the shield off.

2. If you can hear a faint chirping sound coming from the supply about once every second, proceed to step 3.

   If you cannot hear any chirping, measure the voltage at the PONPS testpoint (TP7048) and at PON on the Interconnect Board (the second pin from the left on the upper row of J1010). Both of these voltages should be between 12 V and 15 V if the front and rear switches are both on.

   a. If both voltages are near ground, either the front panel or the wiring to it from the Interconnect Board is probably defective. (It is also possible that the +15 V supply circuit has failed. Check the +15 V testpoint (TP7076). The voltage should be correct within +/- 5 percent.)

   b. If only PONPS is incorrect, check the shutdown testpoint (TP7046). If the testpoint voltage is above 11 V, check the yellow LED on the Regulator Board, which is visible through the fan. If the LED is lit, the overtemperature protection has tripped. To reset it, turn off the rear power switch and allow the instrument to cool down. Then apply power again. When the supply comes on, check the fan for proper operation. If the LED is not lit, proceed to step 3. The supply is probably chirping as previously described. You may not be able to hear this sound if you are in a noisy work area.

3. Turn off the 8560 at the rear panel power switch.

WARNING

Use insulated tools and probes at all times and observe the supplementary cautions contained in the text. Stored charge in the large capacitors of the power supply can cause severe burns and/or electric shock even when the supply is turned off.

4. Locate the fan housing at the rear of the instrument. Remove the two screws (closest to the rear panel) on the fan housing's left side and the six screws that secure it to the rear panel. Disconnect the two wires connected to the fan and set the fan housing aside.
5. Notice the three plug-in circuit boards in the rear opening. From top to bottom these boards are: the Regulator Board, the Secondary Board, and the Inverter Board.

WARNING

Dangerous voltages are present on the Secondary Board even when the front panel power switch is turned off. Line voltage is connected to the side of the large transformer (T1011) that faces the Interconnect Board.

6. Remove the Regulator Board and Secondary Board from their slots. Insert the Secondary Board in the top slot, and the Regulator Board in the second slot.
7. Connect the external trigger of an oscilloscope to the shutdown testpoint on the Regulator Board (TP7046). The scope's sweep rate should be set to 10 ms/div initially. The triggering should be set to normal mode, dc coupling, external source, positive level, and negative slope.
8. Turn on the 8560 with the rear panel power switch. If the front panel switch is also on, the supply should chirp faintly as before. A single trace should be displayed on the scope with every chirp.

   If you determine that the shutdown testpoint is not providing a trigger signal but is staying above 11 V at all times, three possible causes exist:

   - The undervoltage shutdown circuitry (U5040, U3040A) is faulty.
   - The 8560 is configured for a 230 V line but is connected to a 115 V line. See "Selecting the Proper Primary Voltage" in Section 19 of this manual.
   - If the 8560 was running for some time prior to failure, the supply's overtemperature protection may have tripped. See step 2(b) in this procedure.
9. Set the scope's vertical sensitivity to 5 V/cm. Connect a probe from the vertical input of the scope to TP7046. The two traces shown in Fig. 12-6 illustrate the range of expected waveforms. If the waveform matches Fig. 12-6b, reduce the sweep speed until event Y (shown in Fig. 12-6a) is visible. Note the position of event Y on the screen. Event Y occurs when the supply shuts down.

WARNING

Use extreme caution when servicing the Inverter Board. Dangerous voltages exist on the Inverter Board when the 8560 is turned on.

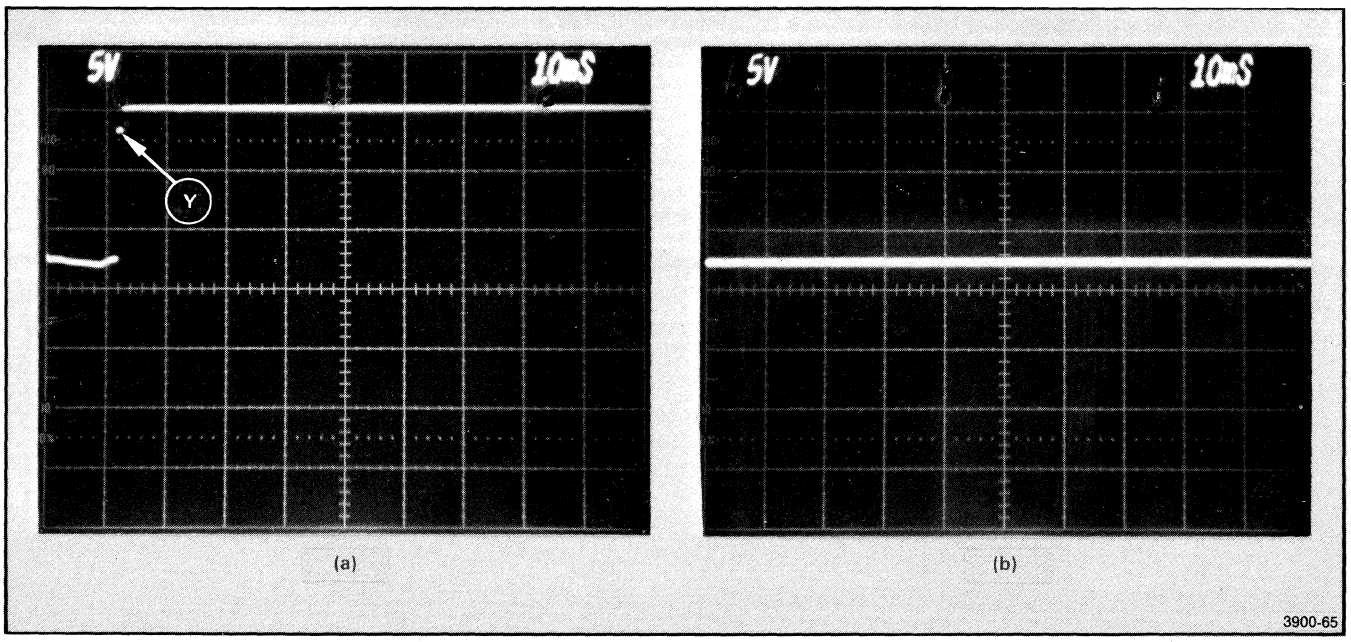

Fig. 12-6. Waveforms at shutdown testpoint.

10. Connect the scope probe to the 15K resistor R5084 on the Inverter Board on the opposite side of the resistor from the connection to TP5085. You should see a 10 V negative-going spike from +15 V at the same position as event Y in Fig. 12-6a. You may have to increase the intensity of the display for the spike to become readily visible.
11. Connect the probe to TP5085.
    - If the spike amplitude is the same as in step 10, proceed to step 11.
    - If the spike amplitude is greater than in step 10, the primary current limit is being activated. A fault may exist in the main inverter control circuitry, or a secondary winding of power transformer T1011 on the Secondary Board may be shorted.
12. Test for an overvoltage problem on the supply outputs by connecting the scope probe to each of the following testpoints on the Regulator Board: +5 V Sense (TP7061), +12 V Sense (TP7043), -12 V (TP7015), +15 V (TP7076), and +24 V (TP7057).
    a. If the voltage during event Y at any of these testpoints is greater than 105 percent of the designated testpoint voltage, the supply is probably being shut down by the overvoltage protection circuit (U2110A on the Secondary Board).
    b. If the overvoltage is on the 5 V line, the reference voltage Vref (TP7066) may be set too high. Check Vref by measuring the voltage between TP7066 and Ground Sense (TP7056). The reading should be within 1 percent of 5 V.
    c. If the overvoltage is confined to the +12 V line, see "Troubleshooting the +12 V Secondary Regulator."
    d. If the overvoltage is confined to the +24 V or -12 V line, see "Troubleshooting the +24 V and -12 V Secondary Regulators." If the overvoltage is on the +15 V line, U1060 on the Regulator Board is probably faulty.
13. Check for a short or an overload on one of the supply's dc outputs if an overvoltage does not appear to be the problem. You can accomplish this by connecting the scope's vertical input differentially across the capacitors listed in Table 12-1. The setup for this connection is accomplished as follows:

    In order to differentially connect across the +5 V and +12 V capacitors, connect a separate scope channel to each end of the capacitor you want to look at. Then, set the scope's controls so that the difference between the two channels is displayed. To connect across the +12 V and -12 V capacitors, the same method can be used if your scope has a linear range of 130 cm at a vertical sensitivity of 100 mV/cm. Otherwise, you must use a differential probe, such as the TEKTRONIX P6046. In any case, set the vertical sensitivity of the scope to 100 mV/cm for both channels, but do not change the triggering and sweep from their previous settings.

    Each of the capacitors listed in Table 12-1 is the input capacitor of one of the overcurrent comparators. The listed capacitors are all located on the Secondary Board. If the voltage across a given capacitor approaches within +10 mV of ground at event Y of Fig. 12-6a, the corresponding output is being overloaded.

Table 12-1
Overcurrent Checkpoints

DC Output	Overcurrent Comparator Input Capacitor
+5 V	C2106
+12 V	C2098
-12 V	C3111
+24 V	C2113

Troubleshooting the +12 V Secondary Regulator

The output of the +12 V secondary regulator is determined by a switching regulator that is slaved to the +5 V regulator. The regulating elements are the two paralleled switching transistors (Q2063 and Q2073). These are driven by a comparator (U2010) through a complementary emitter follower (Q1057, Q2071). The comparator generates a switching signal through comparison of Vref with the actual output voltage. All of these components are on the Secondary Board, except for U2010 on the Regulator Board.

The two most common symptoms of failure in this circuit are overvoltage on the output (which causes the supply to shut down), and insufficient voltage (usually less than half the proper value, even with light loads).

Output overvoltage is usually due to a collector-emitter short in one of the switching transistors. This short effectively removes the regulator from the circuit. Insufficient voltage on the output is usually due to an open PNP driver transistor or a comparator that has failed. Refer to Fig. 12-5.

Procedure.

1. Make sure the 8560 is disconnected from the primary power source.

WARNING

Use insulated tools and probes at all times and observe the supplementary cautions contained in the text. Stored charge in the large capacitors of the power supply can cause severe burns and/or electric shock even when the supply is turned off.

2. Remove the fan housing at the rear of the 8560 to gain access to the Secondary Board. Remove the two screws closest to the rear panel on the housing's left side and the six screws securing the housing to the rear panel. Disconnect the two wires connected to the fan and set the fan housing aside.
3. Notice the three plug-in circuit boards in the fan housing opening. The Secondary Board is the middle board. To remove the board, grasp firmly with a pair of pliers and pull the board out.
4. Check the forward base-collector and base-emitter voltages of Q2063 and Q2073 with a diode meter. These voltages should be between 400 mV and 600 mV. (Since the transistors are paralleled, only two measurements need be made.)
5. Check for a collector-emitter short by connecting the positive lead of the diode meter to an emitter and the negative lead to the collectors. The reading should be more than 1999 mV for a good transistor.
6. If the switching transistor is good, check the two driver transistors in the same way. Reverse the meter leads when checking for a collector-emitter short in the NPN driver transistor.
7. If the driver transistors are good, check the comparator while the supply is running. A failure of this component usually shows up in one of two ways:
   - The output may be incompatible with the inputs (for example, the positive input is above the negative input, but the output is low).
   - The input may be more than a few hundred millivolts above Vref.

Troubleshooting the +24 V and -12 V Secondary Regulators

If the supply won't turn on because of overvoltage on the +24 V or -12 V outputs, or if one or both of these output lines is the wrong voltage, use Table 12-2 to find the problem. For each faulty circuit condition, the most likely bad components are listed in descending order of probability. All listed components are located on the Secondary Board.

Table 12-2
-12 V and +24 V Secondary Regulator Faults

Circuit Fault	Component Fault	Suspect Components	
		+24 V	-12 V
Output voltage is close to ground	1. Open secondary fuse	F3071	—
	2. Failed op amp/ regulator IC	U3110B	U4060
	3. Open pass transistor	Q4109	—
Undervoltage on output	1. Failed op amp/ regulator IC	U3110B	U4060
	2. Failed pass transistor	Q4109	—
Overvoltage on output	1. Shorted pass transistor/ regulator IC	Q4109	U4060
	2. Failed op amp	U3110B	—
	3. Shorted drive transistor	Q3102	—

EMI Test Procedure

The Inverter Board contains an EMI filter amplifier for the purpose of reducing conducted EMI. The following procedure is used to test the EMI filter amplifier.

To test the EMI filter, you need the following equipment:
Oscilloscope (465 or equivalent)
Power supply (PS 503 or equivalent)
Generator (FG 502 or equivalent)

Procedure

With the Inverter Board out of the instrument, check the EMI filter amplifier as follows:

1. Set the PS 503 to 33 Vdc (+/- 5 percent). Connect the negative lead of the supply to pins 31 and 32 of the Inverter Board. Connect the positive lead to pin 36.
2. Set the FG 502 for a 50 mV 10 KHz sinewave and connect it to pin 35 of the inverter edge connector.
3. Check for a 1.5 V (+/-200 mV) signal at the cathode of CR1058 on the Inverter Board. Increase the frequency of the generator to 500 KHz. Check that there are no major peaks or valleys in the waveform (.25 V). The 3 db point of the EMI filter is 500 KHz (-50 KHz, +300 KHz).

BRING-UP PROCEDURE

The following bring-up procedure is intended to be used after you have completed the troubleshooting procedure for catastrophic failure. This procedure enables you to fully check out the power supply and restore it to working order.

Preconditions

Before you perform the bring-up procedure, make sure that you have completed the following steps:

- The fan housing on the rear panel of the 8560 and the power supply top shield have been removed.
- The Inverter Board has been investigated for failures according to procedures outlined under "Catastrophic Failures", and has been repaired as needed.
- The rear panel power switch is off, and the input capacitors (the large cans below the Inverter Board) have discharged to a safe voltage. Discharging occurs within 5 minutes after line power is removed.
- The 8560's line voltage selector switch is properly set.

After verifying that all preconditions are met, refer to Fig. 12-7 and prepare the test set-up. Table 12-3 reflects the equipment required to perform the bring-up procedure.

Table 12-3
Equipment Required for Bring-Up Procedure

Equipment	Recommended Type
Soldering iron/solder	800° F tip temperature/63% tin, 37% lead, rosin core
Needle-nose pliers	Sturdy, with plastic grips
Screwdriver	Phillips for #6 and #2 screws
Voltmeter/diode meter	Fluke Model 8030A or equivalent
Oscilloscpe	TEKTRONIX 465 or equivalent
Isolation transformer	Must have at least 8 A output capability
Variable autotransformer	Variac[a] with at least 8 A output capability
External power supply	Must be able to supply +/-17 V at 400 mA
Extender board kit	Part No. 067-1058-01

[a] **Variac is a registered trademark of the GenRad Corporation**

After installing the test equipment, check that all instrument fuses are good.

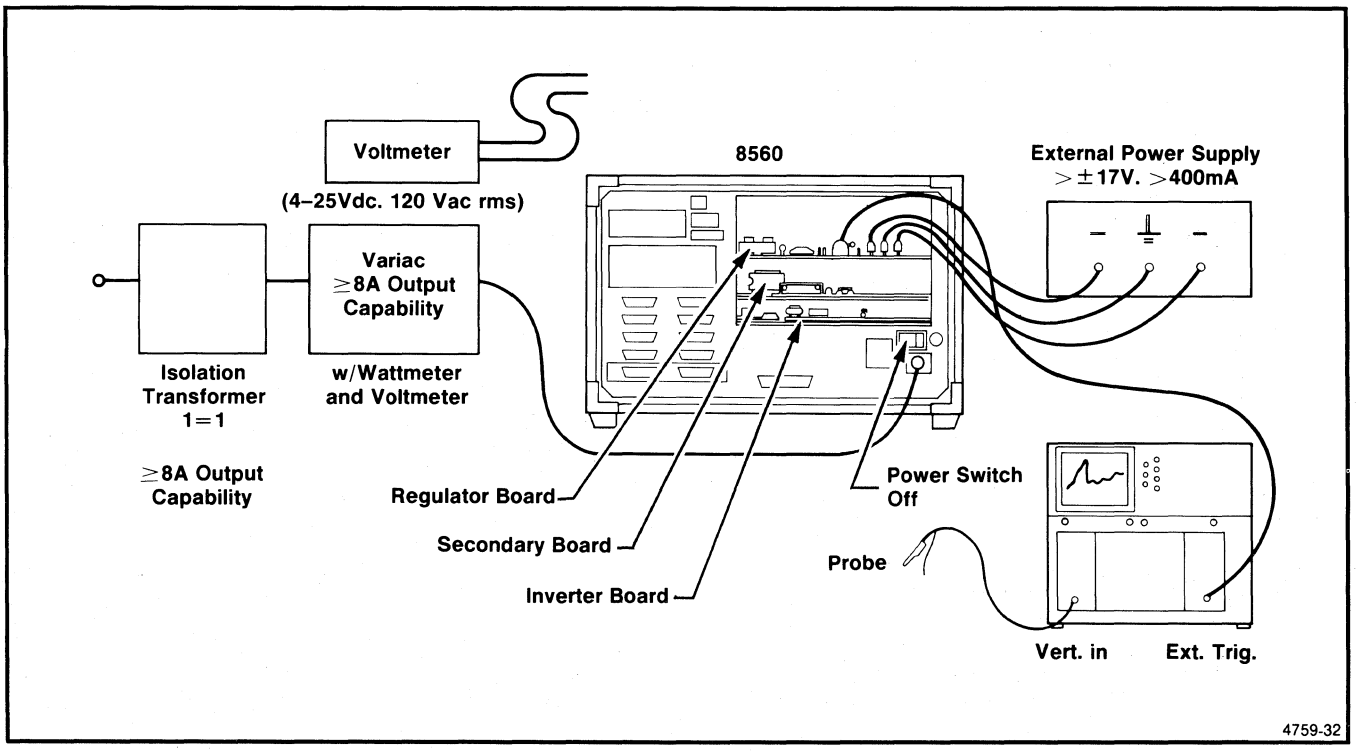

Fig. 12-7. Test equipment set-up.

Procedure

This procedure contains enough detail to allow you to check out every primary supply characteristic except output ripple, input line frequency range, and overvoltage shutdown.

WARNING

Use insulated tools and probes at all times and observe the supplementary cautions contained in the text. Stored charge in the large capacitors of the power supply can cause severe burns and/or electric shock even when the supply is turned off.

1. Remove the Inverter Board from its slot and insert the Inverter Extender Board into the same slot. Then insert the Inverter Board into the extender.
2. Make sure the external power supply is off. Connect leads from the external supply through a 3-pin harmonica connector to the three square pins on the Regulator Board (J7075). The connections should be to +Voltage, Ground, and -Voltage, from left to right (viewed from the rear of the 8560). The supply should be set between +17 V and +40 V (nominally +20 V).
3. Make sure that the rear panel power switch and the Variac power switch are off. Turn on the external power supply. Measure the voltage from the +15 V test point (TP7076) to ground (TP7025), and from the -15 V test point (TP7077) to ground on the Regulator Board. If any measured voltages are not within 5 percent of a test point's assigned voltage, you must repair the standby regulators (U1060, U1070) on the Regulator Board before further testing. Make sure that the external supplies are not operating in a current-limited mode. The external supply current limits should be at least 400 mA each.
4. Measure the voltage from Vref (TP7066) to Ground Sense (TP7056). Adjust the trimmer on the Regulator Board (R7067) until Vref is within 1 percent of +5 V.
5. Remove the undervoltage shutdown jumper (J7047) from the Regulator Board.
6. Connect the external trigger input of the scope to the trigger testpoint (TP7039) on the Regulator Board. Set the scope's sweep rate to 10 μs/cm. Be sure that the external trigger is selected.
7. Connect the vertical input of the scope through a probe to the base of Q3010 on the Inverter Board. Connect the ground clip of the probe to the emitter of the selected transistor. Set the vertical sensitivity to 2 V/cm.
8. Turn on the 8560 dc power switch. The scope should display the waveform shown in Fig. 12-8 or a waveform shifted from this by 180 degrees. If the waveform is correct, proceed to step 10.

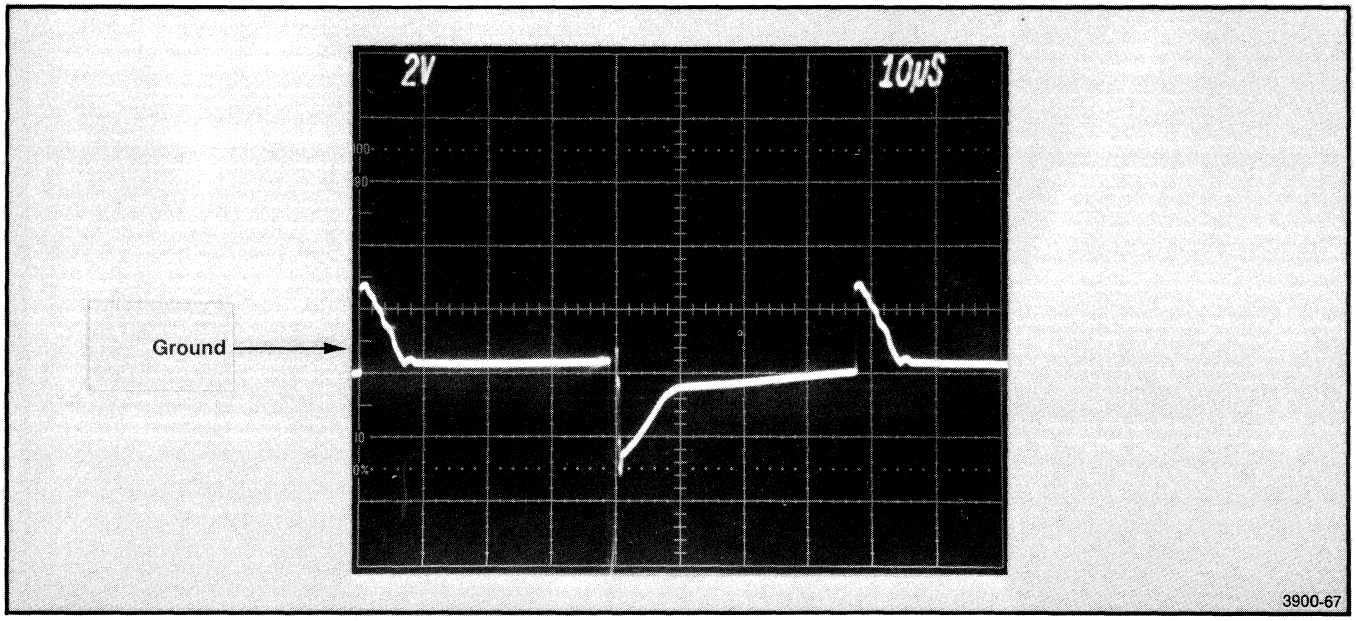

Fig. 12-8. Q3010/Q2010 base-emitter voltage waveform.

9. If the voltage does not drop from 0.7 V to -2 V, but remains near ground or 0.7 V until the negative pulse, one of the driver transistors (Q5074 or Q5075) is probably bad. If the negative pulse is less than about 3 V from base to peak, and the transition time of the falling edge of the positive pulse is less than 1 μs, the other driver transistor is probably bad.

   To check these transistors, change the scope's vertical sensitivity to 1 V/cm, and connect the probe to each of the drain tabs in turn while connecting the ground clip to TP6069. The scope should display the waveform shown in Fig. 12-9, or a waveform shifted from this by 180 degrees. If the large positive pulse has a flat top or is severely attenuated, the transistor is defective. Replace any bad transistors with good ones. If, after you have checked these transistors, the circuit still does not seem to be working properly, proceed to step 11.

10. Check the base-emitter voltage waveform on Q2010. The waveform should have the same shape as that of Q3010 but shifted 180 degrees in phase. If the waveform does not meet this description, check for failures, as in step 9.

11. If the supply is being brought up after a catastrophic main inverter failure, check the waveforms at the gates of Q5074, Q5075, and Q5076. The waveforms at Q5074 and Q5075 should be square waves with a period between 50 μs and 70 μs, a high level at +15 V, and a low level at ground. These two waveforms should also be 180 degrees out of phase. The waveform at Q5076 should be a 1 μs negative-going pulse from +15 V to ground every 25 μs to 35 μs.

    If any voltage is more than a few volts away from the proper level, the transistor you are checking is probably defective even if its drain voltage is correct. However, if the transistor under investigation checks out good, U2030 on the Regulator Board is bad. If no voltage is observed on the bases of Q3010 and Q2010, and the gate waveform of Q5076 is approximately correct, Q5076 is bad.

    If you skipped step 10, go back and do it now. Then proceed to step 12.

12. Make sure at least a minimum load exists on the 5 V supply in the 8560. (A minimum load consists of the flexible disk drive plus the the standard circuit board configuration in the 8560 card cage.) One hard disk should also be plugged in to provide a minimum load on the +12 V supply. However, do not bring up the supply with maximum load on the 5 V output.

13. Connect the vertical input probe to the emitter of Q3010 and the ground clip to the end of C2030 closest to the rear of the instrument. (C2030 is the large, white plastic film capacitor parallel to the long side of the finned heatsink.) Set the vertical sensitivity to 50 V/cm.

14. Turn the Variac output voltage control to zero. Turn on both the Variac and the 8560 rear panel power switch.

WARNING

Use extreme caution when servicing circuitry on the Inverter Board. Dangerous voltages exist on the Inverter Board when the 8560 is connected to line voltage.

15. Increase the Variac output voltage slowly to about 20 V. The scope should display the waveform shown in Fig. 12-10a. The wattmeter should read near zero. If so, slowly turn the Variac output voltage towards 90 V. If the waveform seems to be unstable, slowly increase the Variac voltage while watching its wattmeter. The waveform should stabilize, eventually increasing in frequency. The wattmeter should not read much over 140 W if there is a minimum load in the instrument (see step 12). If anything indicates failure, turn the Variac down immediately. The supply may shut off at some line voltage below 90 Vrms, but if nothing else suspicious occurs, keep turning the Variac up until its output is 90 V. If the supply is operating correctly, when the Variac output is 90 V, the scope will display the waveform shown in Fig. 12-10b.

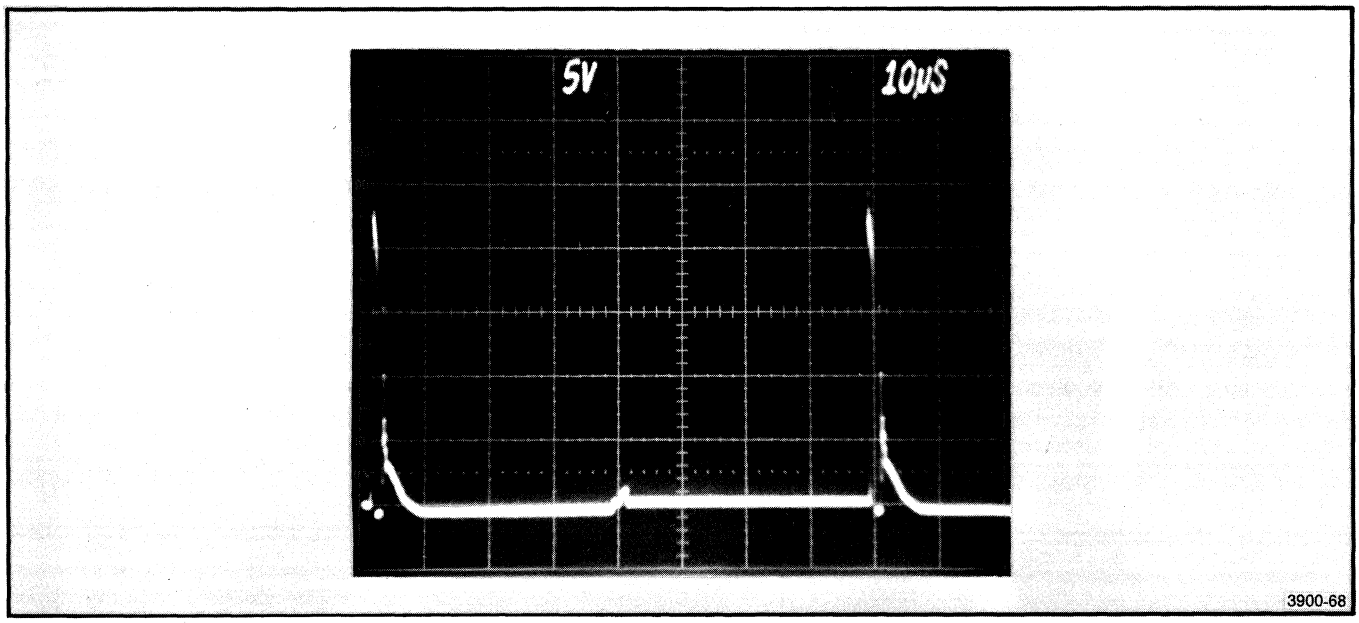

Fig. 12-9. Q5074/Q5075 drain voltage waveform.

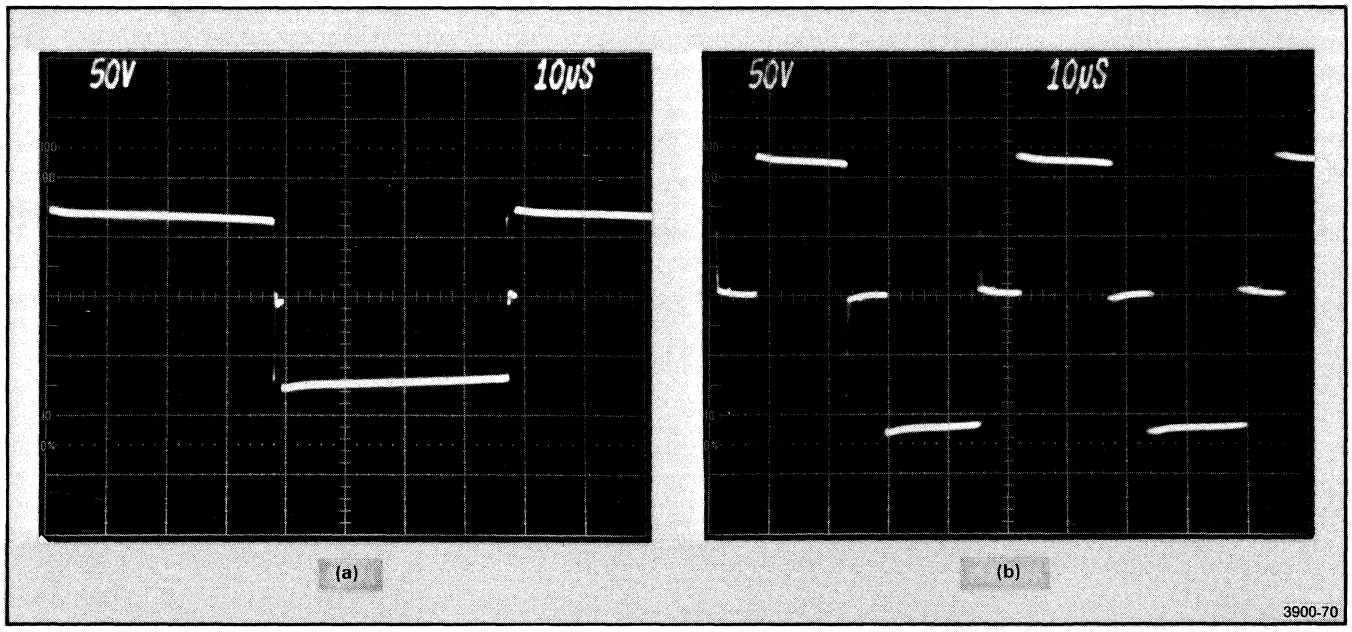

Fig. 12-10. T1011 primary winding waveforms.

16. If the waveform doesn't stabilize or rise in frequency, a fault probably exists in the main inverter control circuitry on the Regulator Board (U3030, U5030D, U5060B, U6010, U2040, U2030, and U3040B). If the wattmeter indicates excessive power consumption, a shorted diode probably exists on the secondary side of power transformer T1011. (See the Secondary Board schematics.) If the supply won't come on when the Variac output is 90 V, turn to "The Supply Won't Turn On" (ignore step 2 of that procedure).

17. Connect the negative lead of your voltmeter to Ground Sense (TP7065), and the positive lead to each of the testpoints listed in Table 12-4.

Table 12-4
Regulator Board Testpoints

Testpoint Name	Testpoint Number	Expected Voltage
+5 V Sense	TP7061	+4.85 V to +5.15 V
+24 V	TP7057	+21.8 V to +23.2 V
+12 V Sense	TP7043	+11.4 V to +12.6 V
-12 V	TP7015	-11.4 V to -12.6 V

18. If the +12 V output is incorrect, see "Troubleshooting the +12 V Secondary Regulator" in the Troubleshooting Guide, earlier in this section. If either the +24 V or the -12 V output is incorrect, see "Troubleshooting the +24 V and -12 V Secondary Regulators", also in the Troubleshooting Guide.

19. Replace the undervoltage shutdown jumper (J7047) on the Regulator Board. Place the voltmeter leads on the +5 V Sense testpoint (TP7061) and Ground Sense testpoint (TP7056). Vary the Variac voltage between 132 Vrms and 90 Vrms. The waveform on the scope should remain stable, and neither the positive or negative peak should go over 200 V. The voltmeter reading should remain within 1 percent of 5 V.

20. If the supply is being brought up after a catastrophic failure in the main inverter, and the supply fails to stay on over an input voltage range of 90 to 132 Vrms, the +12 V secondary regulator may be regulating improperly. To check the +12 V secondary regulator, set the scope's vertical sensitivity to 50 mV/cm and change the coupling to ac. With the supply running, observe the waveform at pin 3 of U2010 on the Regulator Board. If this waveform does not match the waveform in Fig. 12-11 (especially if the sawtooth is smaller or nonexistent), U5030 on the Regulator Board is probably faulty and should be replaced.

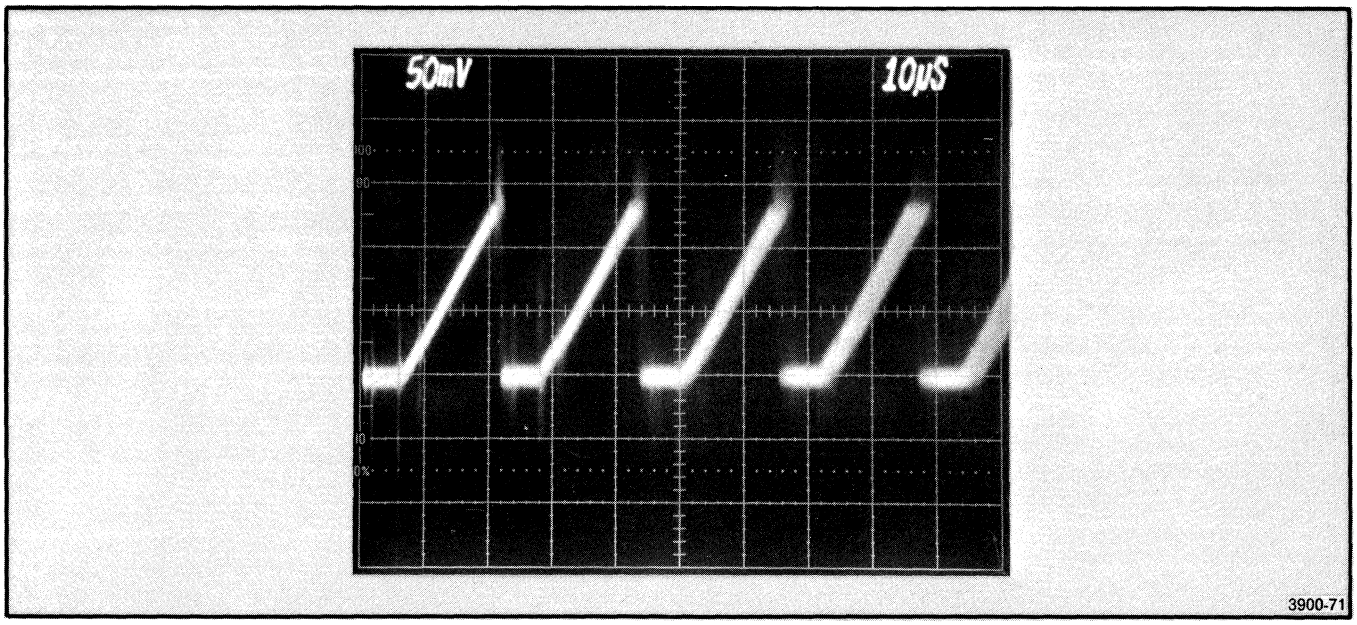

Fig. 12-11. +12 V regulator reference waveform.

21. Turn off the external power supply. The 8560 supply should stay on without change. Turn the Variac voltage below 90 Vrms until the supply shuts off. It should shut off at approximately 80 to 85 Vrms. Turn the Variac voltage back up until the supply turns back on. This should occur below 90 Vrms. The supply should turn on cleanly, with only one chirp and no sputtering.

22. Check the overcurrent shutdown circuitry (U6040 on the Regulator Board, U3110A and U2110 on the Secondary Board). Connect a 20-ohm resistor from the -12 V test point (TP7015) to ground (TP7025). The supply should shut down immediately and chirp faintly every second or so until the resistor is removed. If the supply does not shut down, don't do any further overcurrent shutdown testing until the problem in the -12 V shutdown circuitry is repaired.

    If the supply does shut down, connect a 0.75-ohm resistor from +12 V sense (TP7043) to ground. Then, connect a 16-ohm resistor from +24 V (TP7057) to ground. In both cases, the supply should shut down and chirp until the resistor is removed. Finally, connect a 0.1-ohm resistor from the +5 V power bus to ground near the edge connector on the Regulator Board. The supply should again shut down and chirp until the resistor is removed.

23. Turn off the 8560 from the rear panel. Unplug the 8560 and wait 5 minutes for the input capacitors to discharge to a safe voltage. Then remove all probes from the supply boards.

24. Remove the Inverter Board and its extender, then insert the Inverter Board into its edge connector. Be certain that the Secondary and Regulator Boards are in the correct slots. Replace the top shield over the supply with its four screws. If the fan was disconnected, plug its connector into J7017, being careful to observe the correct polarity. Replace the fan housing with its eight screws. Reconnect all hard disk power connector(s) and replace any circuit boards removed during this bring-up procedure. Replace any outside covers and feet that were removed from the instrument. The supply should now be in satisfactory working order.

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FUNCTIONAL CHECK PROCEDURES

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Section 13

FUNCTIONAL CHECK PROCEDURES

INTRODUCTION

This section describes the self-testing diagnostics that are executed within the 8560 MUSDU every time you power-up the system or toggle the front panel RESTART switch. The diagnostics consist of seven power-up tests and three service routines.

The power-up tests check the RAM, ROM, CPU, Line-Time Clock (LTC), line printer ports, the I/O Processor (IOP) Board(s), and the MSC Board. The service routines help align the flexible disk drive heads and exercise the memory board(s) for examination by oscilloscope.

NOTE

Throughout this section, all addresses are shown in octal notation unless otherwise noted.

This section is organized into five parts:

- An introduction to the 8560 ROM-based diagnostics and some general background information. This part of the section includes the power-up test summary
- A detailed description of the power-up tests and the five LEDs on the Utility Board that display error codes
- A description of the debugging mode, including service routines
- A description of the Octal Debugging Technique (ODT) and a summary of ODT commands
- A summary of error codes

The Firmware

The 8560 power-up diagnostics and service routines and the debugging monitor are contained in two 2K x 8-bit ROMs. The ROMs are located in the system address space as shown in Fig. 13-1.

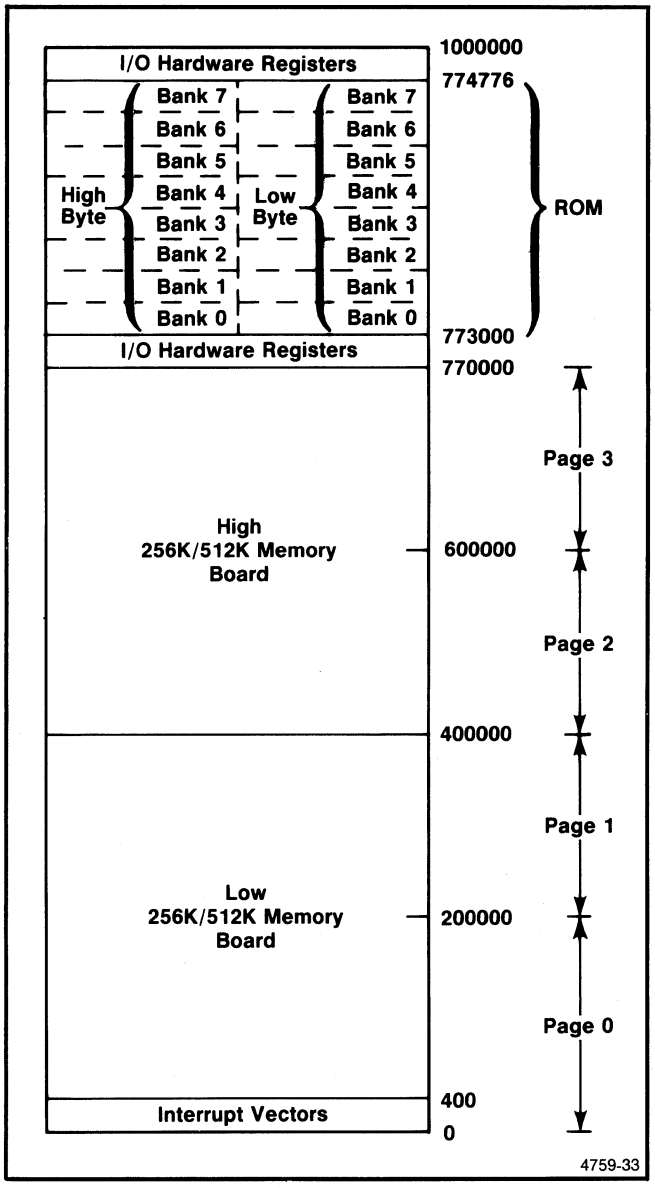


Fig. 13-1. 8560 system memory map.

The ROM firmware is organized in eight selectable banks. Each bank consists of 512 16-bit words:

- Bank 0 tests processor-related functions, such as RAM, ROM and MMU.
- Bank 1 contains flexible disk drive alignment service routines, RAM tests and IOP Board drivers.
- Bank 2 contains a command interpreter. This interpreter is executed after the power-up tests if jumper P1036 is open or an error is encountered.
- Bank 3 contains the bootstrap routine and power-up tests for the MSC.
- Bank 4 and Bank 5 contain power-up tests for the CPU.
- Bank 6 is not used.
- Bank 7 contains power-up tests for the LTC, IOP Boards and printer boards.

Hardware Restrictions

For the power-up tests to execute properly, certain parts of the 8560 must be functioning correctly. The diagnostic firmware assumes that the LSI-11 processor and support circuits (power supplies, clock, and reset circuits) are operational.

Utility Board LEDs

The Utility Board contains five LEDs that represent an octal code. You can view the five LEDs when the 8560 top cover is removed. (For more information on removing the top cover, refer to the *8560 Series Hardware Installation Guide*.) The LEDs are mounted along the Utility Board's top edge with the least significant bit closest to the rear panel. Figure 13-2 illustrates the Utility Board LEDs.

During the power-up sequence, each test function sets the individual LEDs on or off, corresponding to the octal number representing that function. This allows you to identify the last executed test or function before the sequence was halted.

The LED error codes for the functional checks are listed in Table 13-1.

These codes are described in detail in the error summary at the end of this section.

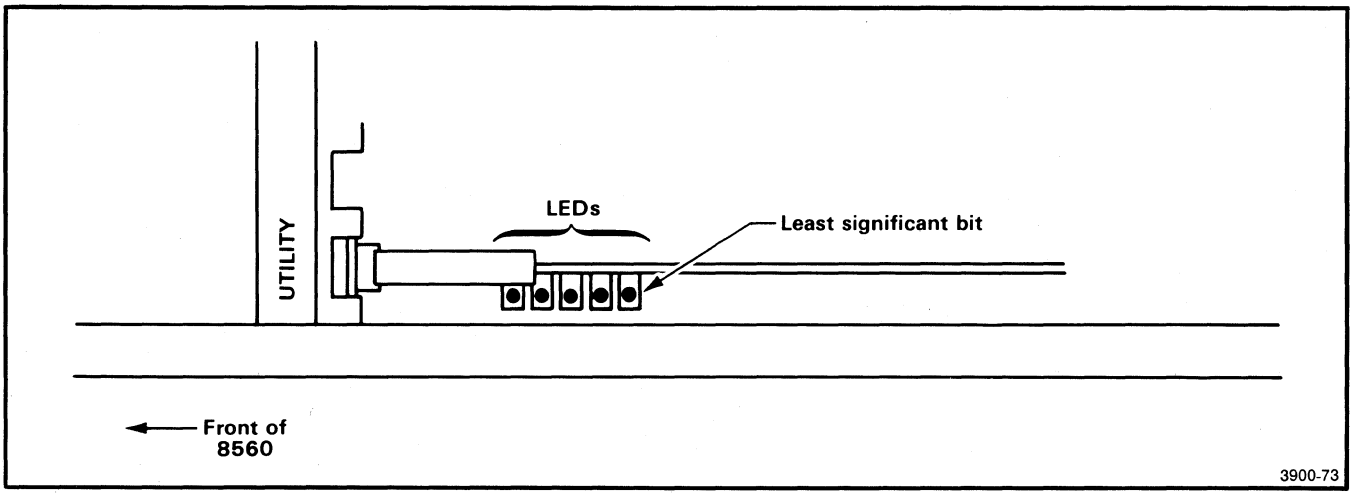


Fig. 13-2. The Utility Board LEDs.

Table 13-1
LED Error Codes

LEDs[a]	Octal Value	Definition
*****	37	Unable to execute firmware
-----	00	LTC error
----*	01	Initialization error
---*-	02	Printer Port 2 error
---**	03	LSI-11 MMU error
--*--	04	Printer Port 1 error
--*-*	05	ROM error (low byte)
--**-	06	MSC error
--***	07	ROM error (high byte)
-*---	10	Page 0 RAM error
-*--*	11	Page 0 RAM error
-*-*-	12	Page 1 RAM error
-*-**	13	Page 1 RAM error
-**--	14	Page 2 RAM error
-**-*	15	Page 2 RAM error
-***-	16	Page 3 RAM error
-****	17	Page 3 RAM error
*----	20	Page 0 RAM parity fault
---	21	Page 0 RAM parity fault
---	22	Page 1 RAM parity fault
*--**	23	Page 1 RAM parity fault
---	24	Page 2 RAM parity fault
--*	25	Page 2 RAM parity fault
*-**-	26	Page 3 RAM parity fault
*-***	27	Page 3 RAM parity fault
**---	30	IOP error
**--*	31	LSI-11 CPU error
**-*-	32	Trying to boot from a disk
-	33	Not used
***--	34	Debugging mode
***-*	35	Debugging mode
****-	36	Executing secondary boot from disk
*****	37	TNIX running

[a] **The dash represents an unlit LED. The asterisk represents a lit LED.**

POWER-UP TESTS

The seven power-up tests execute automatically every time you power up the system or toggle the front panel RESTART switch. You can also start the power-up sequence at any test by entering the appropriate debugging mode "t" command from a terminal. The "t" commands are described in the debugging mode discussion later in this section.

Operation

The power-up tests execute sequentially under control of the LSI-11 processor. The power-up sequence executes in about 15 seconds for a system restart or 40 seconds for a power-up and gives reasonable assurance that the system is operational. Once all power-up tests have passed, the system boots automatically.

If any power-up test fails, the LED readout identifies the test. If a terminal is installed, the diagnostics pass control to the debugging monitor. To troubleshoot the problem, you can loop on the failed test and display the affected registers. In addition, a set of disk-based diagnostic programs, described in Section 16 of this manual, permits further investigation of the failure.

Table 13-2 summarizes the power-up tests and lists the corresponding restart **t** commands for each test.

Table 13-2
Power-Up Tests

Name	Command	Description
Initialization and RAM Test	0t	This test initializes critical interrupt vectors, sets up the LSI-11's Memory Management Unit (MMU), and checks the system memory by writing various patterns to all RAM locations and then reading them back.
ROM Test	1t	This test performs a checksum test on the diagnostic ROMs located on the Utility Board.
CPU Test	2t	This test verifies that the LSI-11 processor is functioning correctly.
LTC Test	3t	This test uses instruction timing to verify that LTC interrupts occur at either a 50 Hz or 60 Hz rate.
Printer Ports Test	4t	This test verifies that the line printer ports on the Utility Board can be written to and read from.
IOP Test	5t	This test verifies that at least one IOP Board is installed in the 8560 and is working properly. If two boards are installed, both are verified.
MSC Test	6t	This test verifies that the MSC is working properly and able to access its disks.

Power-Up Test Descriptions

The 8560 executes the seven power-up tests in the sequence shown in Table 13-2. Once the sequence is started, it continues until it is completed or halted by an error. Figure 13-3 is a flowchart of the power-up diagnostics sequence.

Figure 13-4 is a block diagram of the 8560. Refer to this figure as you read the power-up test descriptions. The power-up diagnostics execute as follows:

1. The LSI-11 initializes the system and attempts to read from RAM location 4. If this is not possible, the PROCESSOR BUSY light dims noticeably.
2. The LSI-11 starts the power-up sequence at ROM location 17773000. The seven power-up tests are then executed in sequence. Each test sets the LEDs to an error code during the course of the test. If a test does not pass, the LEDs remain set, identifying the failed test. If a line printer is connected to LP1 or LP2, or if a terminal is connected to LP2, the diagnostics write an error message. If a line printer or terminal is not connected, the failing test halts the system.
3. If all tests in the power-up sequence pass, the 8560 bootstrap routine tries to boot from the flexible disk. If the routine cannot boot from the flexible disk, the routine tries to boot from the hard disk. In the event that no bootable disk is found, the routine restarts the 8560, and the power-up sequence repeats. This cycle continues until either a bootable disk is found or the 8560 is turned off.

Initialization and RAM Test

Command: 0t

Function: To check the addressing and data storage capability of the system memory.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED Errors 01, 03, 10 through 27

Description. The initialization routine is started every time you power the system or toggle the front panel RESTART switch. This routine initializes critical interrupt vectors and sets up the LSI-11's Memory Management Unit (MMU) by:

1. Setting the LEDs to 01 to show that the firmware is initializing.
2. Initializing the stack pointer.
3. Initializing the Processor Status Word (PSW).
4. Setting all interrupt vectors (0 through 374) to halt at the location following the vector. (For example, a trap to 0 halts at 2.)
5. Setting the LEDs to 11.
6. Checking the parity error locations (114 and 116) for the correct data. Since this is the first time that RAM is read, the program halts at 116 if a RAM problem exists.
7. Writing the address of the parity error handler into the parity error vector, and verifying that the address was written.
8. Checking all of the interrupt vectors for the correct contents and writing the address of the appropriate error handler into each vector location.
9. Setting the LEDs to 03, making sure that the MMU is disabled and then setting up each MMU register.
10. Enabling the MMU.
11. Initializing the RAM test.

The RAM test verifies system memory by writing patterns into each byte of memory and then reading each location to see if the expected data is there. To be more precise, the test starts at the beginning of free memory (location 400) and writes a counter into each location within a 128-word block. The test does a parity check on that block of memory and then complements the contents of the block. After another parity check, the test moves on to the next block of memory and repeats the process.

When the RAM test reaches the top of memory, a bus error occurs. The bus error handler then determines the size of system memory. After that, the test starts at the top of memory and reads each location to check for the expected data. If the data is correct, the location is cleared.

The RAM test can detect parity errors and "wrong data" errors. If a parity error occurs, the parity interrupt handler sets the "parity error" LED code and finds the address of the error. If a "wrong data" error occurs, the test branches to an error handler that determines the address of the error.

This test takes approximately 4 seconds per memory board to execute. If the test passes, the next test is automatically initialized.

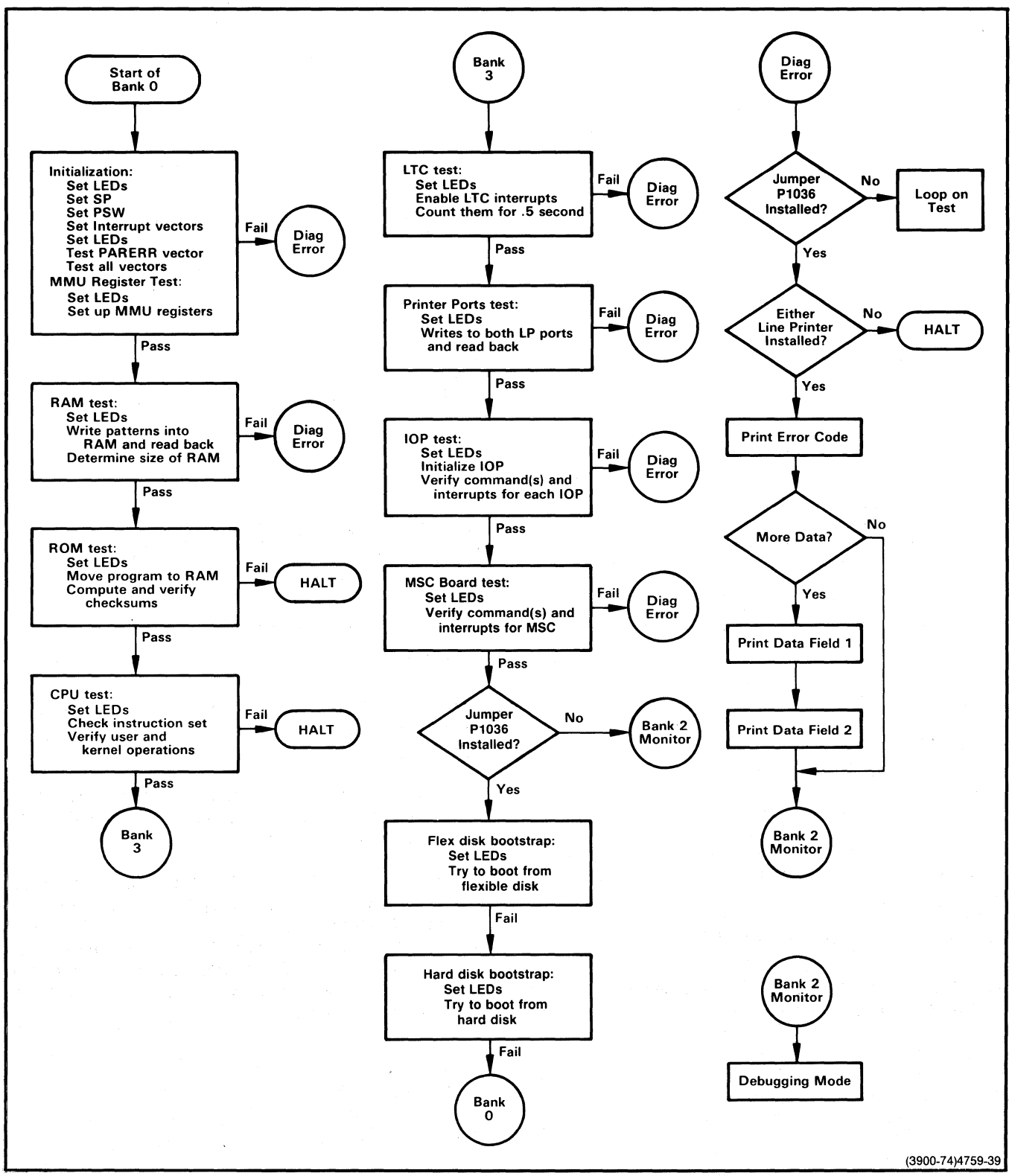


Fig. 13-3. Power-up sequence flowchart.

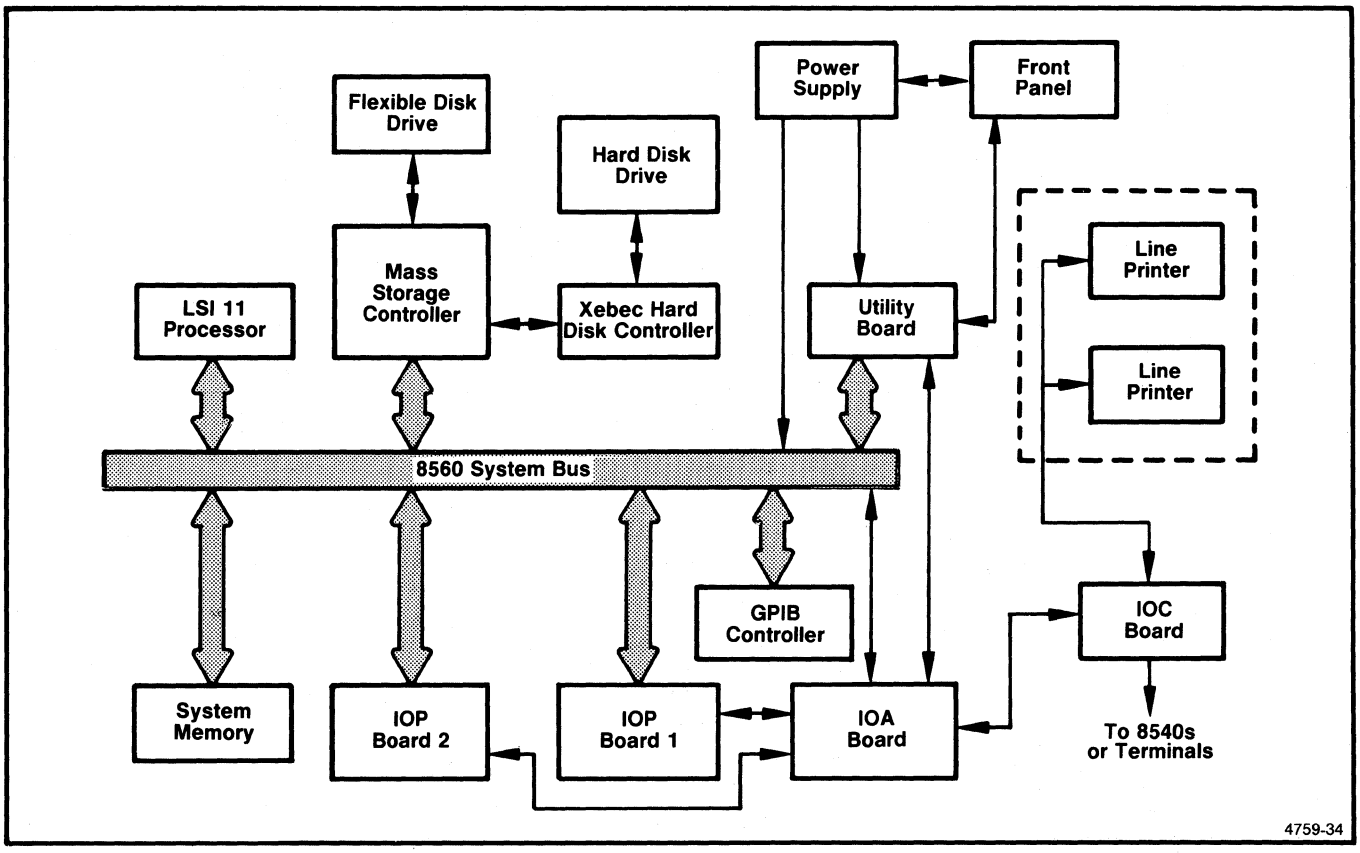


Fig. 13-4. 8560 block diagram.

ROM Test

Command: 1t

Function: To perform a checksum test on the two Utility Board ROM devices.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED errors 05 and 07

Description. The ROM test performs a checksum test on the two ROM devices located on the Utility Board. The 8560 contains two 4K-byte ROMs, one for the low byte and one for the high byte. This test takes only a few milliseconds to execute.

Figure 13-5 shows how the program is organized within the two ROMs. As shown, bank 0 and bank 3 of each ROM contain the power-up tests.

This test sets the LEDs to 05 and then moves all of the firmware banks from ROM into system memory. After the contents of ROM have been transferred, the ROM test performs a checksum test on the low-byte ROM. The ROM test then sets the LEDs to 07 and performs a checksum test on the high-byte ROM. If a ROM error occurs, the program halts with the LEDs set.

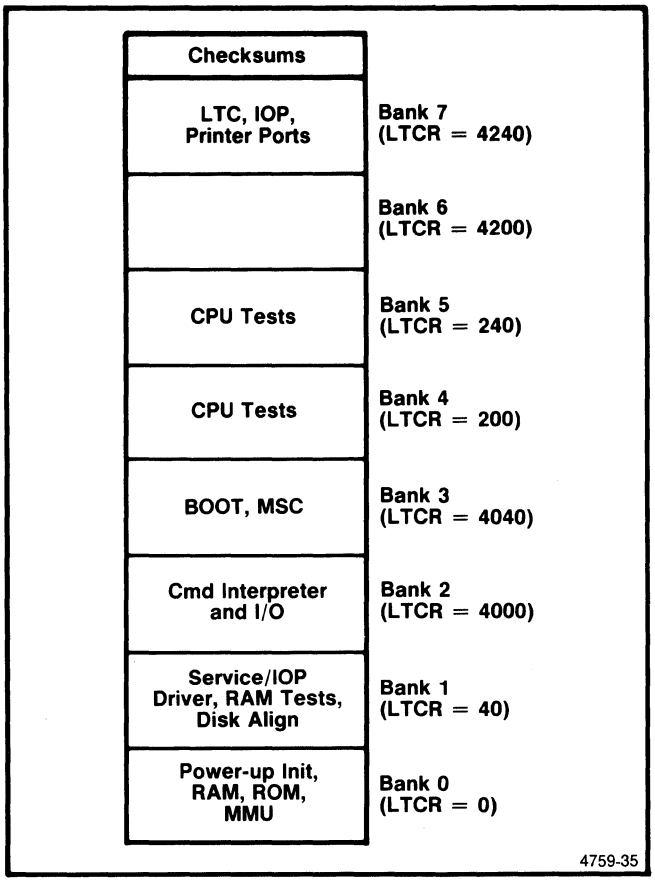


Fig. 13-5. Firmware memory map.

CPU Test

Command: 2t

Function: To execute a representative LSI-11 instruction set, which indicates whether the CPU is operational.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED Error 31

Description. The CPU test checks a representative sample of LSI-11 instructions to determine whether the CPU is operating properly. This test takes only a few milliseconds to execute.

The test sets the LEDs to 31 and then fetches and executes instructions from ROM. The test executes the simpler instructions first and then proceeds to more complex instructions. The CPU test performs the following steps:

1. Checks a representative set of single-operand instructions with destination mode 0.
2. Checks a representative set of single-operand instructions with destination mode 0 using byte mode.
3. Checks a representative set of double-operand word instructions using most source modes and using destination mode 0.
4. Checks a representative set of double-operand byte instructions using various source modes and using destination mode 0.
5. Checks a representative set of word instructions using various source modes and most destination modes.
6. Checks a representative set of byte instructions using various source modes and various destination modes.
7. Checks the JSR, RTS, and MARK instructions using various modes.
8. Checks the MUL, DIV, and ASHC instructions by solving an equation and checking the result.
9. Checks that instructions operating in user and kernel mode work properly when the MMU is activated.

The CPU test checks the results of the executed instructions and halts the LSI-11 if any result is not correct.

Line-Time Clock Test

Command: 3t

Function: To verify that the Line-Time Clock interrupts the LSI-11 at the correct rate.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED Error 00

Description. The LTC test checks that the Line-Time Clock interrupts occur at the proper intervals. This test takes 0.5 seconds to execute.

The LTC test starts by setting the LEDs to 00, setting up the LTC vector, and enabling the LTC interrupts. The test then detects the first interrupt and waits in a loop for 0.5 seconds while the LTC handler counts the number of interrupts that occur. The program then disables interrupts and checks the interrupt counter. If the frequency of the LTC is between 46 and 54 Hz, the frequency is stored as 50 Hz. If the frequency of the LTC is between 56 and 64 Hz, the frequency is stored as 60 Hz. All other frequencies are considered invalid and are reported without rounding. If an invalid frequency is reported, the test fails.

Printer Ports Test

Command: 4t

Function: To verify that the line printer ports on the Utility Board can be written to and read from.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED Errors 02 and 04

Description. This test sets the LEDs to 02, writes to the LP2 Control/Status Register, reads the register, and verifies that the same data is written and read. The test then sets the LEDs to 04 and repeats the same procedure for the LP1 Control/Status Register. If either register doesn't respond correctly, or if a bus error occurs when either register is accessed, the program will report the error. This test takes only a few milliseconds to execute. The main purpose of the printer ports test is to verify the addresses on the Utility Board.

I/O Processor Test

Command: 5t

Function: To verify that at least one IOP Board is installed in the 8560 and is operating correctly. If two IOP Boards are installed, both boards are verified.

Blocks Involved: LSI-11 Processor, IOP Board, Utility Board, System Memory (See Fig. 13-4.)

Error Codes: LED Error 30

Description. This test sets the LEDs to 30, sends a command to the IOP Board(s), and verifies the interrupt and status indication sent back. If Device Register 1 on an IOP Board does not respond correctly, or if a bus error occurs during a register access, the test will also report the error. The test then initializes the IOP Board(s) as necessary for use by the operating system. This test takes only a few milliseconds to execute under normal conditions. However, if the IOP Board is malfunctioning, this test may take 2 or 3 seconds to execute.

MSC Test

Command: 6t

Function: To verify that the MSC is operating properly and is able to access its disk drives.

Blocks Involved: LSI-11 Processor, MSC Board, Utility Board, System Memory, Xebec Disk Controller, Hard Disk Drive, Flexible Disk Drive (See Fig. 13-4.)

Error Codes: LED Error 06

Description. This test sets the LEDs to 06, sends a self-test command to the MSC, and then verifies the interrupt and status indication sent back. The test also reports an error if the Control Register on the MSC is performed by the boot routine, which issues a read command for the flexible disk and/or the hard disk. During an automatic boot, errors such as "drive not ready" and "no boot record on disk" do not cause the diagnostics to report an error. However, these errors are reported during a manual boot attempt.

Bootstrap Routine

Once all of the power-up tests have passed, the bootstrap routine is automatically started. In the normal power-up sequence, the firmware first attempts to boot from the flexible disk. If no flexible disk is present, or if the disk doesn't have a correct boot record, the firmware tries to boot from the hard disk. If a bootable hard disk cannot be found, the firmware repeats the power-up sequence.

THE DEBUGGING MODE

The debugging mode is a firmware program that aids in troubleshooting minor system failures prior to system boot-up. The debugging mode requires that a terminal be connected to either LP2 or one of the IOP terminal ports (directly or through an 8540). The debugging mode allows you:

- To write or read any location in the 8560
- To restart the power-up routine at any test
- To boot the system manually rather than automatically
- To type in a program and execute it
- To execute any service routine

Entering the Debugging Mode

You can enter the debugging mode under the following conditions:

- If all power-up tests pass and maintenance jumper P1036 on the Utility Board is not installed, the firmware automatically selects the debugging mode.
- If any test fails (other than ROM or CPU) and maintenance jumper P1036 is installed, the firmware automatically selects the debugging mode. However, if error codes are to be printed out, a line printer must be connected to LP1 or LP2, or a terminal must be connected to LP2.
- You can also enter the debugging mode manually by the following method:

  1. Set the RUN/HALT switch to HALT
  2. Toggle the RESTART switch
  3. Set the RUN/HALT switch to RUN
  4. Enter the following underlined characters on a terminal connected to LP2:

```
777546/ xxxxxx  4000 <CR>
P
```

Baud Rate Selection

The debugging mode normally communicates with your terminal at 2400 baud, but this baud rate may be changed if necessary. The following text explains how to use a terminal set for a baud rate other than 2400.

If you are using the debugging mode from a terminal connected to LP2 or to an 8540, the debugging mode baud rate is determined by hardware settings. (See the *8560 Series Hardware Installation Guide* or the *8540 Installation Guide*, depending on your set-up.)

If you are using a terminal connected directly to an IOP channel, the debugging mode baud rate will be 2400 by default. However, you can change the baud rate of any IOP channel to which your terminal is connected. First set the baud rate of your terminal to the desired setting. Then press the BREAK key until the "=" prompt appears on the screen. You have now programmed the channel's baud rate to match the baud rate of your terminal.

Debugging Mode Commands

The debugging mode follows a predetermined operating sequence unless interrupted by a valid debugging mode command. Valid commands are listed in Table 13-3. Figure 13-6 shows the debugging mode program flow.

Table 13-3
Debugging Mode Commands

Command	Function
xt	Starts a power-up test or service routine specified by x [a]
f	Causes the 8560 to boot from the flexible disk
h	Causes the 8560 to boot from the hard disk
x/	Prints contents of a location x
RETURN	Closes an open location and accepts next command
LINEFEED	Closes current location and opens the next sequential location
xg	Goes to location x and starts program execution

[a] **In this table, "x" is an octal number of up to six digits.**

Commands may be entered in either uppercase or lowercase. If you enter an illegal command, the firmware will print a "help" message.

The debugging mode commands are similar to the Octal Debugging Technique (ODT) commands discussed later in this section. Debugging mode commands can be used in most situations where ODT commands are used. Differences between the two types of commands include:

- The debugging mode **Go** command accepts a 16-bit address only, and no memory mapping is allowed (as in ODT).
- In debugging mode, LSI-11 internal registers cannot be written to or read from (as in ODT).
- In debugging mode, the terminal does not need to be connected to LP2 (as required by ODT); the terminal can also be connected to any IOP port, or the terminal port of a connected 8540.
- The ODT **Proceed** command is not used in the debugging mode.

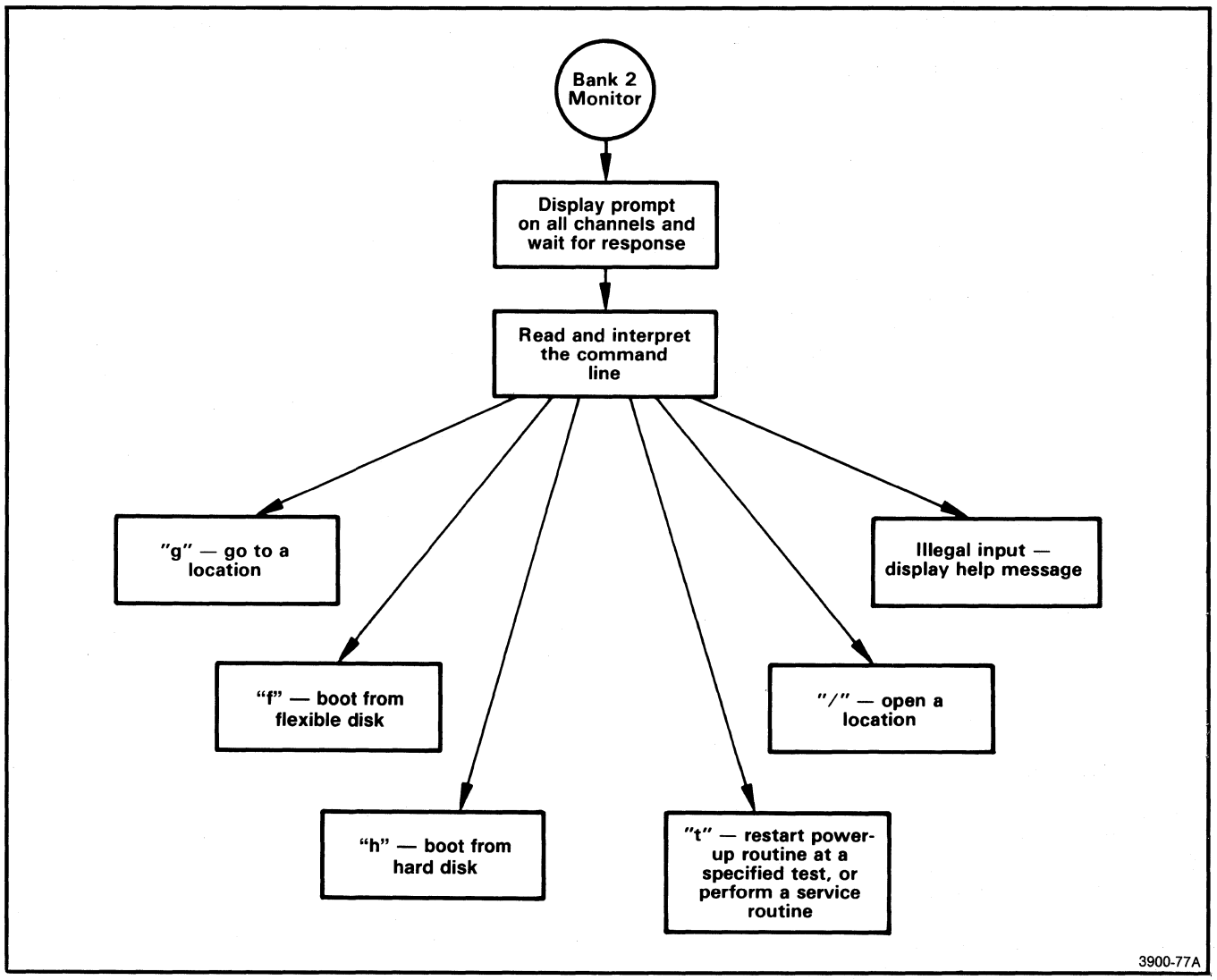


Fig. 13-6. Debugging mode flowchart.

The Restart (t) Commands

The debugging mode allows you to restart the power-up sequence at any test. When the "=" prompt appears on the terminal, you can issue a command that determines where to restart the power-up sequence. Following is a list of the restart commands and their respective functions:

0t Initializes the power-up tests and restarts the RAM test

1t Restarts the ROM test

2t Restarts the CPU test

3t Restarts the LTC test

4t Restarts the Printer Ports test

5t Restarts the IOP test

6t Restarts the MSC test

Maintenance Jumper

If a power-up test failed, you may want to use an oscilloscope or other test equipment for further troubleshooting. Troubleshooting can be done by removing the maintenance jumper (P1036 on the Utility Board) and restarting the 8560. The system loops on any hardware failure that it finds, thus exercising the failed circuits. However, this method of troubleshooting is effective only for solid errors. In the case of intermittent errors, the test drops out of the loop the first time the test passes.

As previously mentioned, the maintenance jumper can also be used to control access to the debugging mode. Table 13-4 lists the functions of jumper P1036. These functions depend the position of P1036 and on whether the power-up tests pass or fail.

Table 13-4
Maintenance Jumper Functions

Tests pass?	P1036 position	Result
no	ON	Enter debugging mode (if terminal connected)
no	OFF	Loop on error
yes	ON	Boot from disk
yes	OFF	Enter debugging mode

Service Routines

The debugging mode allows you to perform flexible disk drive head alignment, an azimuth check and perform additional memory verification. Table 13-5 summarizes the service routines.

Table 13-5
Service Routines

Name	Command	Description
Alignment Aid	7t	This service routine assists in aligning the flexible disk heads and checking the azimuth. An oscilloscope and alignment disk are required. This routine can also be used with a head-cleaning disk to clean the heads.
Low Memory Board Signal Exerciser	10t	This service routine exercises the signal paths on the low memory board, which permits troubleshooting the board with an oscilloscope.
High Memory Board Signal Exerciser	11t	This service routine exercises the signal paths on the high memory board, which permits troubleshooting the board with an oscilloscope.

Alignment Aid

Command: 7t

Function: To assist in aligning the flexible disk drive heads.

Blocks Involved: LSI-11 Processor, MSC , Flexible Disk Drive, System Memory, Utility Board (See Fig. 13-4.)

Description. The following service routine is divided into three parts:

- A supplementary procedure for flexible disk drive head alignment
- A supplementary procedure for a flexible disk drive azimuth check
- A procedure for cleaning the flexible disk drive heads

Head Alignment. The alignment aid service routine allows you to perform a track-38 head alignment of the flexible disk drive. Refer to the *QumeTrak 242 Maintenance Manual* for the basic procedure. Use the following service routine to supplement the procedure.

A message is displayed advising you to type "0" to align side 0 of the disk or "1" to align side 1. After you select the desired side of the disk, the disk drive produces a whirring noise as the heads are loaded onto the alignment disk and moved to track 38. Once the heads move to track 38, the same message prints on the screen again.

Each time you select a side of the disk, the program alternately does a seek to either track 0 or 76 and then returns to track 38. The program then causes the disk drive to do a perpetual read to track 38, thereby reading continuously from the alignment track.

Press the front panel RESTART switch to stop this routine.

Head Azimuth Check. The alignment aid service routine is used to check head azimuth as well as to adjust head alignment. Refer to the *QumeTrak 242 Maintenance Manual* for the basic azimuth check procedure. Use the following information to supplement the procedure.

Before performing the azimuth check, you must temporarily alter the alignment aid service routine so it will do a perpetual read to track 76. Changing the routine is accomplished by completing the following procedure:

1. Enter the debugging mode by removing jumper P1036 on the Utility Board and RESTARTing the 8560.
2. When you see the "=" prompt, enter "124/". In response, you will see 000046 printed (the octal equivalent of 38).
3. Enter 114 (the octal equivalent of 76), followed by a RETURN.
4. In response to the "=" prompt, enter "7t", just as you would for head alignment.

After completing this procedure, the firmware will move the heads to track 76, as required in the azimuth check procedure. You select the disk side and move the heads, as outlined in the preceding head alignment description.

To stop this routine, press the front panel RESTART switch.

Head Cleaning Procedure. The Alignment Aid service routine can also be used to clean the flexible disk drive heads. To clean the heads, insert a head-cleaning disk in the drive, and type "7t". In response to the "side of disk" prompt, type "0". After waiting the time specified in your head-cleaning kit (usually about 30 seconds), press RESTART and remove the disk.

Memory Board Signal Exerciser

Command: 10t (low memory board) or 11t (high memory board)

Function: To exercise the signal paths on one of the memory boards, permitting an oscilloscope to be used to troubleshoot the board.

Blocks Involved: LSI-11 Processor, MSC , Flexible Disk Drive, System Memory, Utility Board (See Fig. 13-4.)

Description. This service routine is used with an oscilloscope to troubleshoot the memory board(s) by allowing you to examine activity on all of the signal lines. This routine is a loop that writes to and reads from sequential memory locations, thus stimulating all signal paths on the memory board.

To use this routine, first disable parity and refresh on the memory board you want to troubleshoot. You can disable parity by moving jumper P7111 to position 2. Disable refresh by removing jumper P7161 on the memory board. Enter "10t" or "11t" (while in the debugging mode). After the routine has started, all signal paths on the memory board will be toggling. Refer to the memory boards schematics at the back of this manual.

TROUBLESHOOTING IN THE ODT MODE

The Octal Debugging Technique (ODT) is a built-in feature of the LSI-11 which allows you to examine and change register contents and memory locations. ODT permits you to single-step and restart a user program. The ODT commands and octal addresses must be entered on a terminal connected to LP2.

Table 13-6 summarizes the ODT commands and lists the ASCII code for each command. The commands may be uppercase or lowercase characters.

Entering ODT

ODT is invoked automatically when the RUN/HALT switch is set to HALT or the LSI-11 executes a HALT instruction.

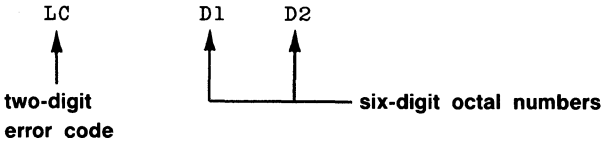
Table 13-6
ODT Commands

Command	ASCII	Function
x/	057	Prints contents of location x[a] and leaves that location open.
RETURN	015	Closes an open location and accepts next command.
LINEFEED	021	Closes current location and opens the next sequential location.
rx/ or $x/	122 044	Opens a specific processor cessor register x.
s	123	Opens the Processor Status Register (PS). This command must follow a "$" or "r" command.
xg	107	Goes to location x and starts program execution.
p	120	Resumes execution of a program.

[a] **In this table, "x" is an octal number of up to six digits.**

ERROR SUMMARY

The following text summarizes the power-up test error codes displayed on the Utility Board LEDs, a line printer connected to LP1 or LP2, or on a terminal connected to LP2. If a line printer or terminal (connected to LP2) is installed on the 8560 before the power-up sequence, error messages are printed in the following format:



LC is an octal representation of the LED error code reflecting what the LEDs would have displayed if a line printer or terminal were not installed. D1 and D2 are optional data fields containing information about the error. If the error codes were not printed, you can still find them stored in 8560 memory as follows:

```
LC      location 52
D1      location 54
D2      location 56
```

When reading an LED error code, remember that the LED representing the least significant bit is located closest to the rear panel.

Error Codes

00 Error during the LTC test. If this message is printed, the data fields provide the following information:

- If no data fields are printed after the 00, a bus error or unexpected interrupt occurred during the test.
- If D1 is 0, no LTC interrupts occurred. This might be due to a broken signal path on the Utility Board, a missing signal on the bus, or an incorrectly placed jumper on the CPU Board.
- If D1 is greater than 0 but less than 27, the line frequency is less than 46 Hz.
- If D1 is greater than 40, the line frequency is greater than 64 Hz. It is also possible that the CPU is slowing down due to DMA operations on part of the system.

01 Normally this code is never printed. If the LEDs display this code, the CPU was unable to complete initialization. Failure to initialize may be due to a hung bus, a faulty CPU Board, or a faulty memory board.

02 LP2 is faulty. This means that the CPU is unable to write to or read from the registers jumpered for 17777560 on the Utility Board. Either the Utility Board is at fault or an address conflict exists between the Utility Board and another board.

03 The CPU Board's Memory Management Unit is not working properly. To find out which of the MMU's registers is faulty, divide D1 by 2; the result is the number of the bad register.

04 LP1 is faulty. This means that the CPU is unable to write to or read from the registers jumpered for 17777510 on the Utility Board. Either the Utility Board is at fault, or there is an address conflict between the Utility Board and another board.

05 Normally this code is never printed. If the LEDs display this code, U5080 on the Utility Board does not verify. Either the ROM or its associated circuitry might be bad. Check related jumpers.

06 Error during MSC test. If this message is printed, the data fields provide the following information:

- If no data fields are printed, a bus error or invalid interrupt occurred during the test. This could mean that the MSC Board is not installed.
- If D1 is 0, the program was unable to correctly write or read the Device Register on the MSC Board.
- If D1 is 1, the MSC did not send a valid interrupt to the CPU. Make sure the jumpers on the MSC are correctly installed.
- If D1 is 2, the MSC sent a valid interrupt to the CPU but did not set its "done" bit. This could indicate DMA problems.
- If D1 is 3, the MSC reported a self-test error. D2 displays the MSC error code. These codes are described at the end of Section 16 of this manual.

07 Normally this code is never printed. If the LEDs display this code, U5090 on the Utility Board does not verify. Either the ROM or its associated circuitry might be bad. Check related jumpers.

10-11 This code indicates a RAM error (other than a parity error) in page 0 (0 to 177777). The error could be due to addressing or data paths, or to RAM size, which must be at least 256K bytes. D1 displays the address (without the two most significant bits) where the error occurred, but this address could be off by ±2. D2 displays the expected data at the location specified by D1. With this information you can open the specified location and determine which bits are incorrect. The error is probably on the low memory board.

12-13 This code indicates a RAM error (other than a parity error) in page 1 (200000 to 377777). The error might be due to addressing or data paths, or to RAM size, which must be at least 256K bytes. D1 displays the address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays the expected data at the location specified by D1. With this information you can open the specified location and determine which bits are not correct. The error is probably on the low memory board.

14-15 This code indicates a RAM error (other than a parity error) in page 2 (400000 to 577777). The error might be due to addressing or data paths, or to RAM size, which must be at least 256K bytes. D1 displays the address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays the expected data at the location specified by D1. With this information you can open the specified location and determine which bits are not correct. The error is probably on the high memory board.

16-17 This code indicates a RAM error (other than a parity error) in page 3 (600000 to 777777). The error might be due to addressing or data paths, or to RAM size, which must be at least 256K bytes. D1 displays the address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays the expected data at the location specified by D1. With this information you can open the specified location and determine which bits are not correct. The error is probably on the high memory board.

20-21 This code indicates a RAM parity error in page 0 (0 to 177777). D1 displays the address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays where the program was when the error occurred. Therefore, D2 is not intended for general use. To determine which of the 16 bits is at fault, disable parity and execute the RAM test again, allowing the last part of the test to run. To disable parity, move jumper P7111 on the memory board(s) to position 2. (Position 1 is indicated by the arrow on the circuit board.) The error is probably on the low memory board.

22-23 This code indicates a RAM parity error in page 1 (200000 to 377777). D1 displays the 16-bit address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays where the program was when the error occurred. Therefore, D2 is not intended for general use. To determine which of the 16 bits is at fault, disable parity and execute the RAM test again, allowing the last part of the test to run. To disable parity, move jumper P7111 on the memory board(s) to position 2. (Position 1 is indicated by the arrow on the circuit board.) The error is probably on the low memory board.

24-25 This code indicates a RAM parity error in page 2 (400000 to 577777). D1 displays the 16-bit address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays where the program was when the error occurred. Therefore, D2 is not intended for general use. To determine which of the 16 bits is at fault, disable parity and execute the RAM test again, allowing the last part of the test to run. To disable parity, move jumper P7111 on the memory board(s) to position 2. (Position 1 is indicated by the arrow on the circuit board.) The error is probably on the high memory board.

26-27 This code indicates a RAM parity error in page 3 (600000 to 777777). D1 displays the 16-bit address (without the two most significant bits) where the error occurred, but this address might be off by ±2. D2 displays where the program was when the error occurred. Therefore, D2 is not intended for general use. To determine which of the 16 bits is at fault, disable parity and execute the RAM test again, allowing the last part of the test to run. To disable parity, move jumper P7111 on the memory board(s) to position 2. (Position 1 is indicated by the arrow on the circuit board.) The error is probably on the high memory board.

30 Error during IOP test. The data fields provide the following information:

- If no fields are printed, an IOP bus error occurred. Verify that there is at least one IOP Board in the 8560.

NOTE

For the following cases, D2 displays the error code returned by the IOP Board.

- If D1 is 0, the firmware could not correctly write to or read from Device Register 0 on IOP Board 1.
- If D1 is 1, IOP Board 1 timed out without returning an interrupt. Make sure that the jumpers on the IOP Board are correctly installed.

- If D1 is 2, IOP Board 1 returned an interrupt, but the buffer was not changed. This might be due to DMA-related problems.
- If D1 is 3, IOP Board 1 detected a fatal error.
- If D1 is 4, the firmware could not correctly write to or read from Device Register 0 on IOP Board 2.
- If D1 is 5, IOP Board 2 timed out without returning an interrupt. Make sure that the jumpers on the IOP Board are correctly installed.
- If D1 is 6, IOP Board 2 returned an interrupt but the buffer was not changed. This might be a DMA-related problem.
- If D1 is 7, IOP Board 2 detected a fatal error.

31 Error during CPU test, indicating that the LSI-11 processor is not operational. Normally this code only appears on the LEDs.

32 Normally this code appears on the LEDs as a status indication that the 8560 is trying to find a bootable disk. However, if you used the **f** or **h** command and a message is printed, the data fields provide the following information:

- If no data fields are printed, a bus error or unexpected interrupt occurred. Check that an MSC Board is installed.
- If D1 is 0, the MSC ignored the command to boot.
- If D1 is 1, the MSC returned a fatal error code, which appears in D2. These codes are described at the end of Section 16 of this manual.
- If D1 is 2, the boot block on the disk was invalid because it did not have correct data.
- If D1 is 3, the boot block was loaded and executed, but the file system on the disk was incorrect.

33 This code is not used.

34-35 This code normally appears only on the LEDs as a status indication that the firmware is in the debugging mode.

36 This code normally appears only on the LEDs, signifying that a boot block was loaded from the disk and is being executed.

37 This code normally appears only on the LEDs. If this code appears when power is first turned on and does not change, the firmware cannot execute. This condition may occur if the RUN/HALT switch is in the HALT position or as the result of missing memory boards, a missing CPU board, or a hung bus.

If this code appears after the LEDs flash through their normal sequence, the TNIX operating system is in control of the 8560.

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Section 14

ADJUSTMENT PROCEDURES

+5 V REFERENCE ADJUSTMENT

The +5 V reference adjustment in the power supply sets the level of the +12 V, -12 V, and +24 V dc outputs. This adjustment should never be changed during normal operation.

Procedure

1. Make sure the 8560 is disconnected from the primary power source.

WARNING

Use insulated tools and probes at all times. Stored charge in the large capacitors of the power supply can cause severe burns and/or electric shock even when the supply is turned off.

2. To gain access to the +5 V reference adjustment (which is located on the Regulator Board of the power supply), remove the fan housing at the rear of the 8560. Remove the fan housing by taking out the two screws closest to the rear panel on the housing's left side, and the six screws that secure the housing to the rear panel. Disconnect the fan plug from the Regulator Board (the uppermost board) and set the fan housing aside. Three plug-in circuit boards are now visible through the opening that the fan housing normally covers.
3. Connect the 8560 to the primary power source. Turn on the rear panel ac power switch, but leave the front panel dc power switch off.
4. Measure the voltage between Vref (TP7066) and Ground Sense (TP7056) on the Regulator Board. The voltage should be within 4.95 to 5.05 V. If the measured voltage is out of that range, adjust trimmer resistor R7067 (located near the right-hand edge of the board).
5. Remove the voltmeter and replace the fan housing at the rear of the 8560. The adjustment is now complete.

MSC BOARD PHASE LOCKED LOOP CALIBRATION

The following procedure is used to calibrate the phase-locked loop circuit on the MSC Board:

1. Locate the 8560 so that you have access to the top of the unit. Make sure the power on the 8560 is off. Remove the top cover, following instructions in Section 15, "Removing the Cover Panels."
2. Remove the MSC Board from the card cage. Install an extender card in the MSC slot and insert the MSC Board in the extender card.
3. Make sure jumper P6141 is in its normal position, connecting the upper pin (indicated by an arrow) and the middle pin.
4. Power up the 8560 MUSDU.
5. Attach an oscilloscope probe to TP5131.
6. Move jumper P6141 so that it connects the middle and lower pins.
7. Adjust variable resistor R6153 until the oscilloscope reflects a 500 KHz signal and positive-going pulses are 250 ns wide.
8. Move the probe to TP5153.
9. Adjust variable capacitor C6151 for a 500 KHz square wave.
10. Move the probe to TP6111.
11. Adjust variable resistor R5158 until the positive-going pulses are 200 ns wide.

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MAINTENANCE

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Section 15

MAINTENANCE

INTRODUCTION

This section describes preventive maintenance procedures to improve equipment reliability. It contains techniques and aids for troubleshooting, including diagnostic testing routines. If the equipment fails to operate properly, corrective measures should be taken immediately to prevent additional problems from developing.

STATIC-SENSITIVE DEVICES

Some of the transistor and integrated circuit devices in this equipment are sensitive to static discharge and can be damaged by improper handling. Observe the following suggestions to minimize the possibility of such damage:

- Minimize the handling of static-sensitive parts.
- Transport and store static-sensitive parts in their original containers, on a metal rail or on conductive foam. Label any container that has a static-sensitive assembly or device.
- Discharge the static charge on yourself by using a wrist strap before you handle these devices. Servicing of static-sensitive assemblies or devices should be performed only at a static-free workstation by qualified personnel.
- Do not allow anything capable of generating or holding a static charge onto the workstation surface.
- Pick up a part by the body, never by its leads, and keep the leads shorted together whenever possible.
- Do not subject the part to sliding movements over any surface.
- Avoid handling static-sensitive parts in areas where the floor or work surface covering contributes to the generation of a static charge.
- Use a soldering iron that has a connection to earth ground.
- Use a special anti-static suction-type desoldering tool, such as the Silverstat Soldapullt.

REDUCING SUSCEPTIBILITY TO STATIC DISCHARGE

The 8560 incorporates a number of safeguards to reduce the chance of static discharge damage.

CAUTION

Violation or modification of the following safeguards can result in ground loops and/or static discharge problems.

1. The ground (earth) wire of the primary power cable is connected to the chassis where the cable enters the unit.
2. Shields of interconnecting cables are grounded to the chassis at the point of connection to each unit.
3. Ground loops have been avoided by installing a common ground between all units.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, and performance checks. The preventive maintenance schedule established for the equipment should be based on the amount of use and on the environment in which the equipment is operated.

Cleaning

Clean the equipment often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulator and prevents efficient heat dissipation. It also provides high-resistance electrical leakage paths between conductors or components in a humid environment.

CAUTION

Do not allow water to get inside any enclosed assembly or components, such as switch assemblies and potentiometers. Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone, or similar compounds. Such solvents may damage the plastic.

Exterior

Remove dust from the outside of the equipment by cleaning the surface with a soft cloth or brush. Hardened dirt may be removed with a cloth dampened in water containing a mild detergent. Do not use abrasive cleaners.

Interior

Clean the interior by loosening accumulated dust with a dry, soft brush. Blow the loosened dirt away with low-pressure air. To clean a circuit board, remove the circuit board and clean it with a dry, soft brush. Hardened dirt or grease may be removed with a cotton-tipped applicator dampened with a solution of mild detergent and water. Abrasive cleaners should not be used.

After cleaning, allow the interior to dry thoroughly before applying power to the equipment.

Visual Inspection

After cleaning, carefully check the equipment for defective connections and damaged parts. The remedy for most visible defects is obvious. If you discover heat-damaged parts, try to determine the cause of overheating before replacing the damaged part. Otherwise, the damage may reoccur.

TROUBLESHOOTING

Check your warranty or service agreement before performing any troubleshooting yourself. For your warranty to remain in effect, all service must be performed by Tektronix, Inc. for the first 90 days following delivery.

Your Tektronix service support center is best suited to perform repairs on Tektronix equipment. However, the following servicing aids and troubleshooting procedures may aid you in tracing a problem to its source.

Servicing Aids

Diagrams

Circuit diagrams appear on foldout pages in the Diagrams section of this manual. The circuit number and electrical value of each component are shown on the diagram. (See the first page of the Diagrams section for an explanation of the symbols used to identify components in this equipment.)

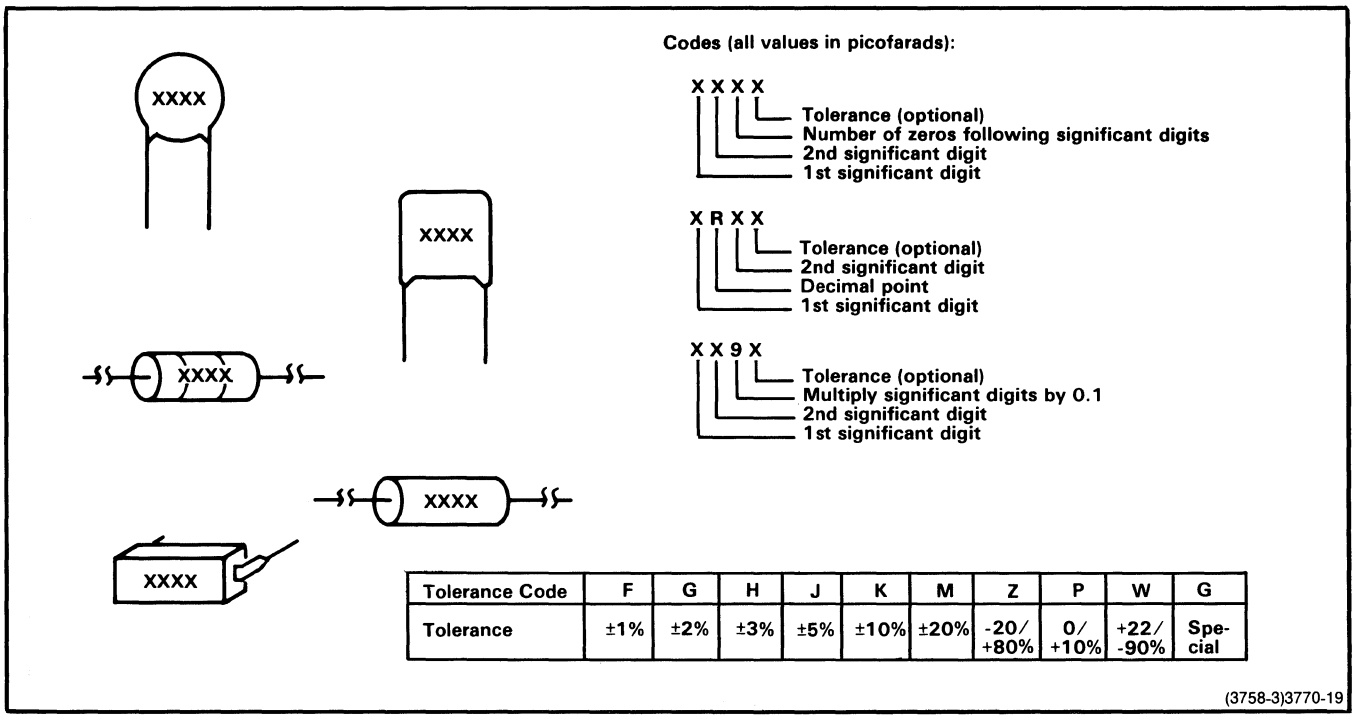
Components on circuit boards are assigned vertical and horizontal grid numbers which correspond to the location of the component on the circuit board. Refer to Section 20 of this manual for a complete description of each component and assembly.

NOTE

Corrections and modifications to the manual and equipment are described on inserts bound into the rear of the manual. Check this Change Information section for manual or instrument changes and corrections.

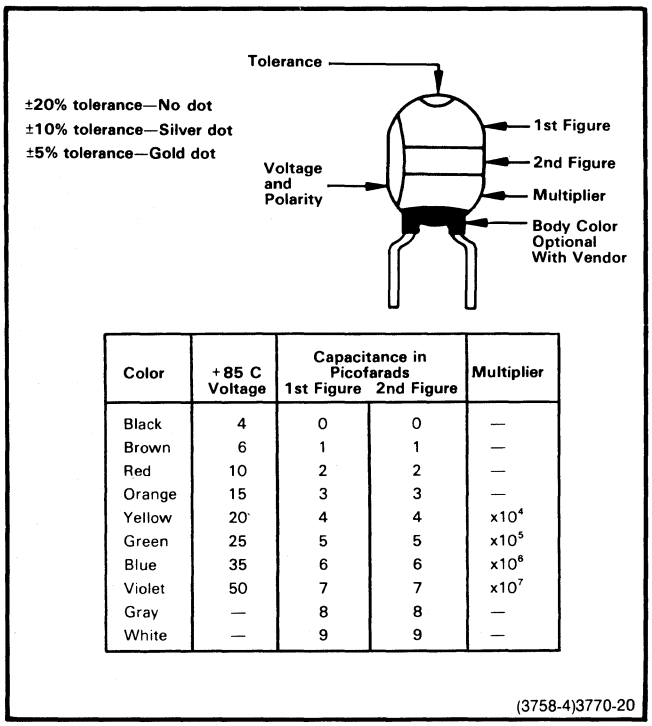
Circuit Board Illustrations

Electrical components, connectors, and test points are identified on circuit board illustrations located on the inside fold of the corresponding circuit diagram or on the back of the preceding diagram. This allows cross-referencing between the diagram and the circuit board and shows the physical location of components.



Tolerance Code	F	G	H	J	K	M	Z	P	W	G
Tolerance	±1%	±2%	±3%	±5%	±10%	±20%	-20/ +80%	0/ +10%	+22/ -90%	Special

Fig. 15-1. Ceramic and film capacitor coding.



Color	+85 C Voltage	Capacitance in Picofarads 1st Figure	2nd Figure	Multiplier
Black	4	0	0	—
Brown	6	1	1	—
Red	10	2	2	—
Orange	15	3	3	—
Yellow	20	4	4	$x10^4$
Green	25	5	5	$x10^5$
Blue	35	6	6	$x10^6$
Violet	50	7	7	$x10^7$
Gray	—	8	8	—
White	—	9	9	—

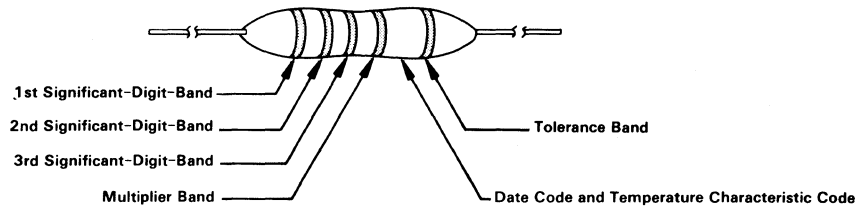
Fig. 15-2. Tantalum capacitor color code.

Capacitor Marking

The capacitance (in microfarads or picofarads) and voltage rating of any ceramic, mica, plastic film, and electrolytic capacitors are marked on the side of the component body. The values of other ceramic disk and plastic film capacitors, as well as monolithic ceramic capacitors (such as DIP and glass-encapsulated types), are marked according to the code shown in Fig. 15-1. Tantalum capacitors are marked in microfarads or according to the color code shown in Fig. 15-2.

Resistor Marking

Carbon resistors are marked according to the standard four-band resistor color code. A fifth band, if present, defines the failure rate. Metal film resistors are marked according to either the standard four-band resistor color code or the five-band color code illustrated in Fig. 15-3.



DATE CODE INFORMATION

YYWW
- WW — Week of the year (may be from 01-52)
- YY — Last two digits of the year

COLOR BAND INFORMATION

Color	1st Sig. Digit	2nd Sig. Digit	3rd Sig. Digit	Multiplier	Tolerance ± %	
Black	0	0	0	1	—	
Brown	1	1	1	10	1.	F
Red	2	2	2	100	2.	G
Orange	3	3	3	1,000	3.	H
Yellow	4	4	4	10,000	—	
Green	5	5	5	100,000	.5	D
Blue	6	6	6	1,000,000	.25	C
Violet	7	7	7	10,000,000	.1	B
Grey	8	8	8	100,000,000	.05	A
White	9	9	9	1,000,000,000	—	
Gold				.1	5.	J
Silver				.01	10.	K
No Color					15.	L
No Color					20.	M

TEMPERATURE CHARACTERISTIC INFORMATION

Temperature Characteristic Code	Temperature Coefficient (PPM/°C)	Temperature Range (°C)
T-0 D (C-0)	0 to ±150	-55 to +175
T-00	0 to ±200	-55 to +175
T-1 D (C-1)	0 to ±100	-55 to +175
T-2 C (C-2)	0 to ± 50	-55 to +175
T-9 E (C-3)	0 to ± 25	-55 to +175
T-10	0 to ± 15	-20 to + 85
T-13	0 to ± 10	-20 to + 85
T-14	0 to ± 20	-20 to + 85
T-15	0 to ± 25	-20 to + 85
T-16	0 to ± 5	-20 to + 85
T-18	0 to ± 2	0 to + 60
T-18	0 to ± 5	-55 to +125
T-B	0 to ± 10	25 to +125
T-E	0 to +100 -500	-55 to +175
T-R	0 to +100 -250	-55 to +175

(3758-5)3770-21

Fig. 15-3. Metal film resistor color code.

Diode Code. Diode cathodes are indicated by a stripe, a series of stripes, or a dot on the diode body. Some diodes have a diode symbol printed on one side. Figure 15-4 illustrates diode types and polarity markings.

Coil and Transformer Identification

Coils and transformers are identified by Tektronix part numbers. If the part number appearing on the part consists of only four numbers, a prefix number must be added to obtain the complete part number, as follows:

Classification	Part No. Prefix
Fixed Coils	108-XXXX-XX
Variable Coils	114-XXXX-XX
Transformers	120-XXXX-XX

Transistor and Integrated Circuit Pin Configuration

Lead identification drawings for transistors and three-lead integrated circuits are included with the schematic diagrams. Pin 1 identification for typical DIP integrated circuits is shown in Fig. 15-5.

Obtaining Replacement Parts

Most electrical and mechanical parts are available through your local Tektronix field office or representative. The Replaceable Electrical and Mechanical Parts List sections contain information on how to order these replacement parts. You can obtain many standard electronic components locally in less time than if you ordered them from Tektronix, Inc. If you do so, try to duplicate the original component as closely as possible. Parts orientation and lead dress should be duplicated, since orientation may affect circuit interaction.

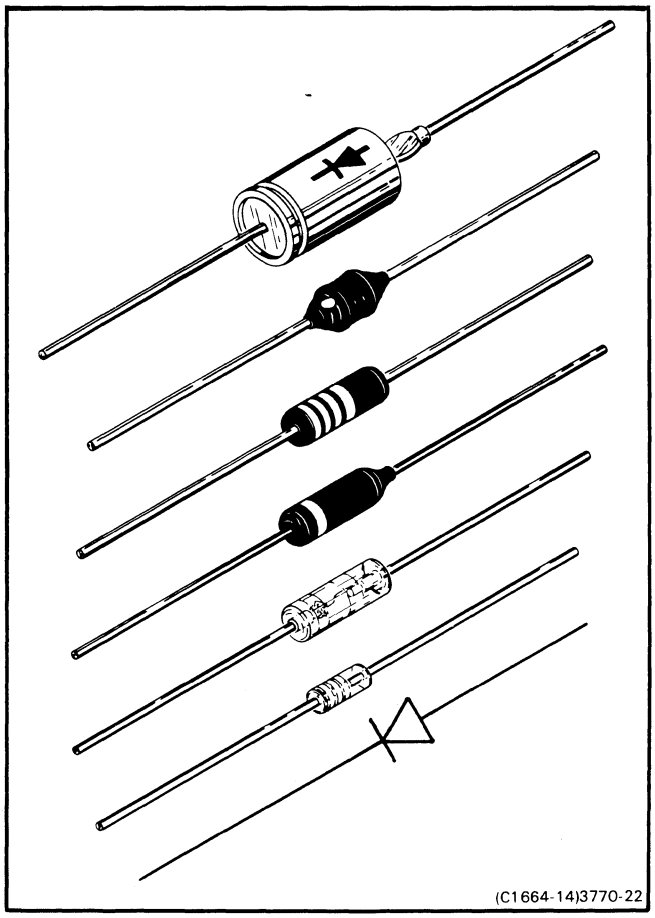


Fig. 15-4. Diode polarity markings.

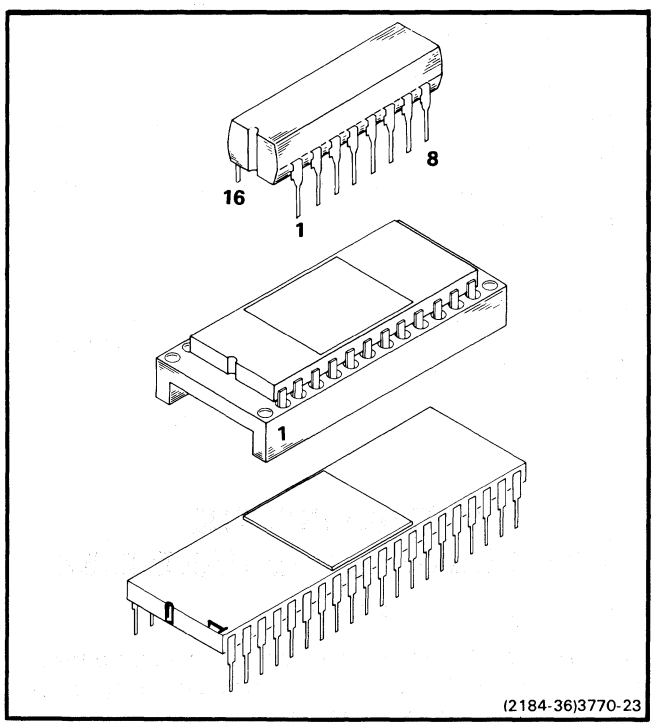


Fig. 15-5. Integrated circuits pin 1 identification.

If a component you have ordered has been replaced with a new or improved part, your local Tektronix field office or service representative will contact you concerning the change in the part number.

Assembly Repair and Exchange Program

Tektronix service centers provide replacement or repair of major equipment assemblies in addition to complete equipment units. Contact your local service center for this service.

Initial Equipment Checks

Before you start any detailed troubleshooting of the equipment, perform the following basic equipment checks:

- Check that all cabling is installed properly
- Verify that all supporting equipment is operating correctly
- Check power supply levels
- Remove appropriate circuit boards, clean the edge connectors on the boards, and replace the boards in their correct positions in the equipment

PREPARING THE 8560 FOR SERVICING POWER SUPPLY

To inspect, replace or calibrate the power supply, the 8560 must be powered down, and the top cover-panel and rear panel fan housing must be removed.

Section 12 in this manual describes the power supply and provides troubleshooting information. Section 14 contains procedures to adjust the power supply +5 V reference voltage.

Removing The Cover Panels

The 8560 has four cover panels: two side panels, one top panel, and one bottom panel. These panels are flat metal sheets with a small flange at their rear edge. Each cover, except the top one, fits into two grooves along the side or bottom of the chassis. Four plastic retainers at the rear of the cabinet hold them in place. The retainers are fastened to the rear casting with screws. A T-20 Torx tip screwdriver is required to remove any of the cover retainer screws.

CAUTION

Before removing any of the cover panels, make sure the power to the 8560 is off.

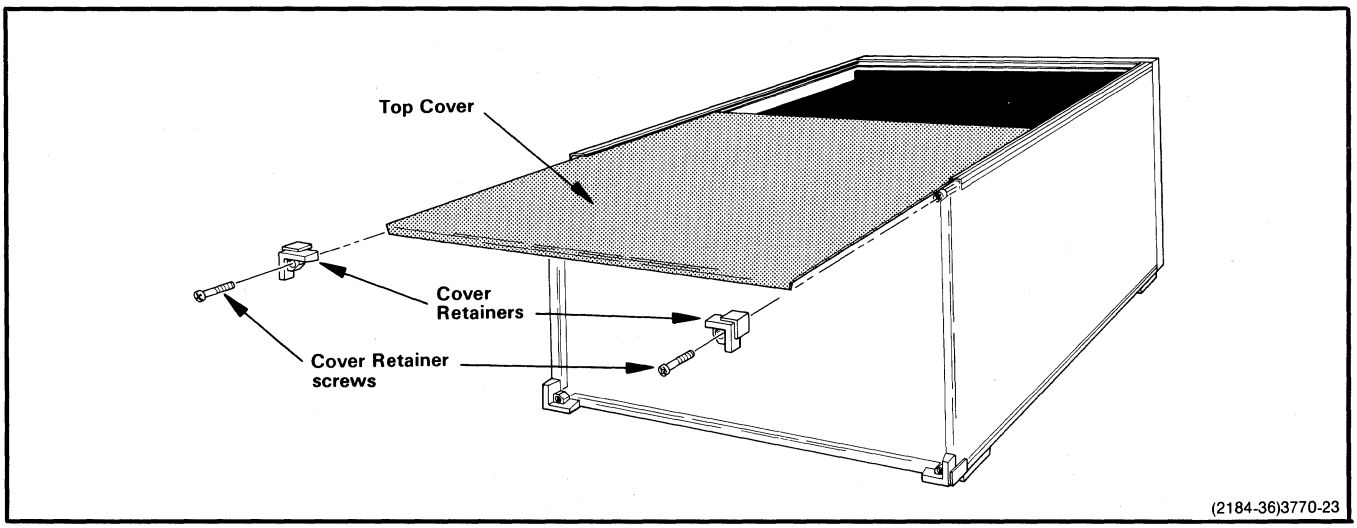


Fig. 15-6. Removing the 8560 top cover.

To remove the top cover, remove the screws and retainers as shown in Fig. 15-6. Slide the top cover an inch or so towards the cabinet rear and lift it away.

To remove any other cover, remove the appropriate retainers and slide the cover all the way toward the cabinet rear. Make sure that there is sufficient clearance to do so.

Removing The Rear Panel Fan Housing

To access the power supply area, remove the fan housing at the 8560 cabinet rear panel. Facing the cabinet rear, remove the housing as follows:

1. Remove the two horizontally mounted screws in the housing's left side.
2. Remove six additional screws (three on top and three on the bottom) that mount the housing to the rear panel.
3. Remove the fan power cable which is located at the rear-left corner of the Regulator Board. Notice the color coding of the cable when removing it so that the cable will be reinstalled in the appropriate direction.

REMOVING THE WINCHESTER-TYPE DISK DRIVE UNIT(S)

Remove the Winchester-type hard disk drive(s) in the following sequence:

1. Remove the two top rear cover retainers and the bottom cover retainer on the drive side. (See "Removing the Cover Panels," earlier in this section.) Slide the top cover an inch or so to the rear and lift it off the unit. Remove the drive unit side cover by sliding it out.
2. Disconnect the power cable and the two Xebec S1410 Disk Controller interface cables at the disk drive(s).
3. Remove 2 screws from the top left rail, 2 screws from the top of each drive, and 2 top bulkhead screws to loosen the drive retainer plate. Figure 15-7 shows the screw locations.
4. Lift the MSC Board, together with the 50-pin flat cable attached to it, out of the instrument and adjust the board and cable so that they are not in the way of the drive retainer plate.
5. Slide the retainer plate toward the rear of the 8560.
6. Grasp the drive unit(s) at the back and front and carefully lift out.
7. Place the unit(s) in a safe location where they will not be damaged.

NOTE

Prior to installing a new hard disk drive unit, see the default strapping configuration information contained in Section 3 of this manual.

INSTALLING THE WINCHESTER-TYPE HARD DISK DRIVE

To install a Winchester-type hard disk drive, reverse the removal process. Make sure the holes provided on the bottom side of the drive drop onto the locating pins.

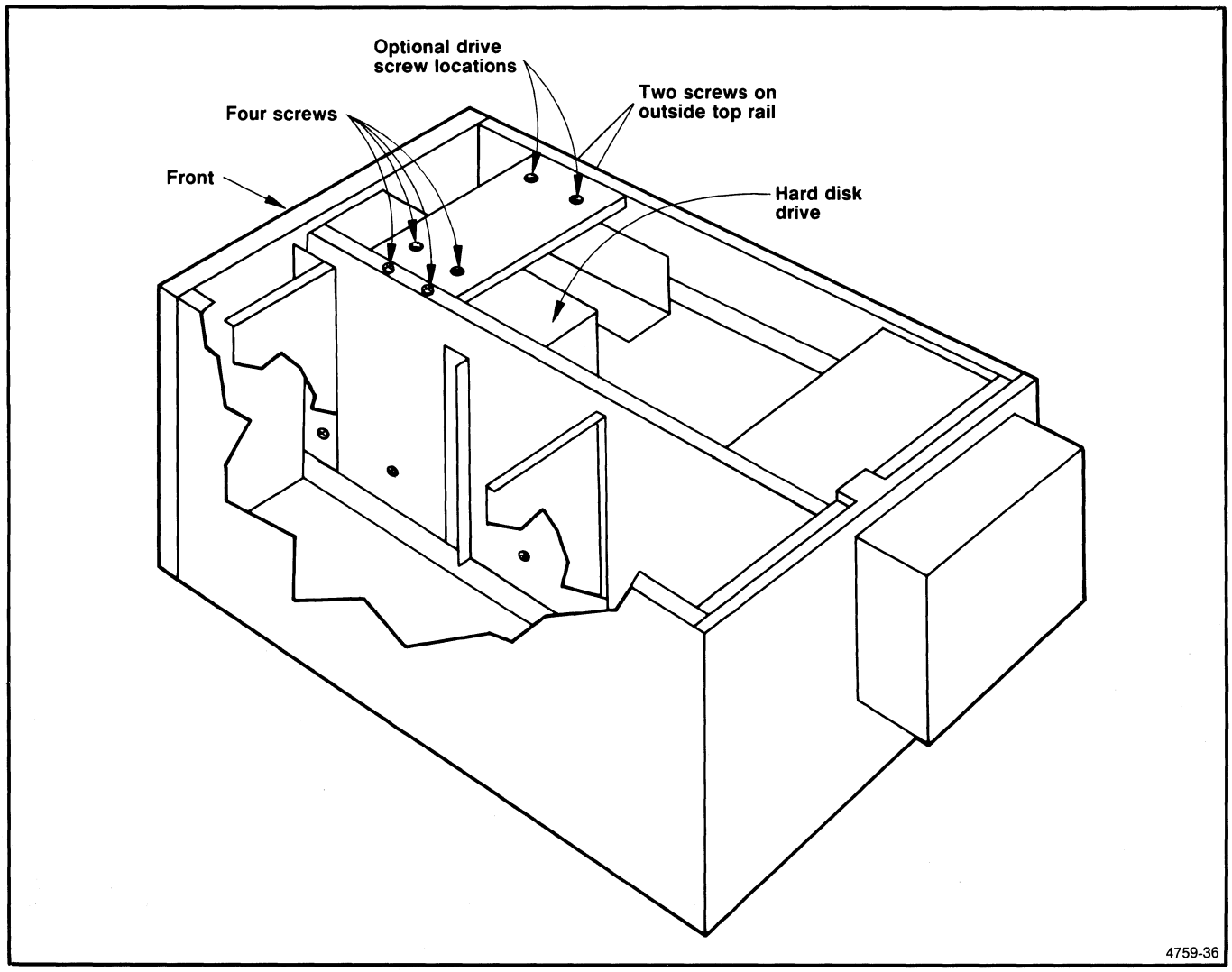


Fig. 15-7. Hard disk drive screw locations.

REMOVING THE FLEXIBLE DISK DRIVE

The QumeTrak 242 flexible disk drive unit is removed through the front of the 8560 cabinet. Figure 15-8 shows the Qume disk drive screw locations. (Note that the screws used in this drive are metric.) Refer to this illustration as you perform the following procedure:

1. Disconnect the 50-pin ribbon cable located at the rear center of the drive. Disconnect the power cable.
2. Remove both of the side covers and the top cover. (See "Removing the Cover Panels" earlier in this section.)
3. Remove all boards from the main card cage.
4. Remove the three screws on the left side.
5. Turn the 8560 on its left (drive unit) side.
6. Remove the three inside screws.
7. Slide the flexible disk drive unit out through the front of the 8560 unit.

NOTE

Prior to installing a new flexible disk drive unit, see the default strapping configuration information provided in Section 3 of this manual.

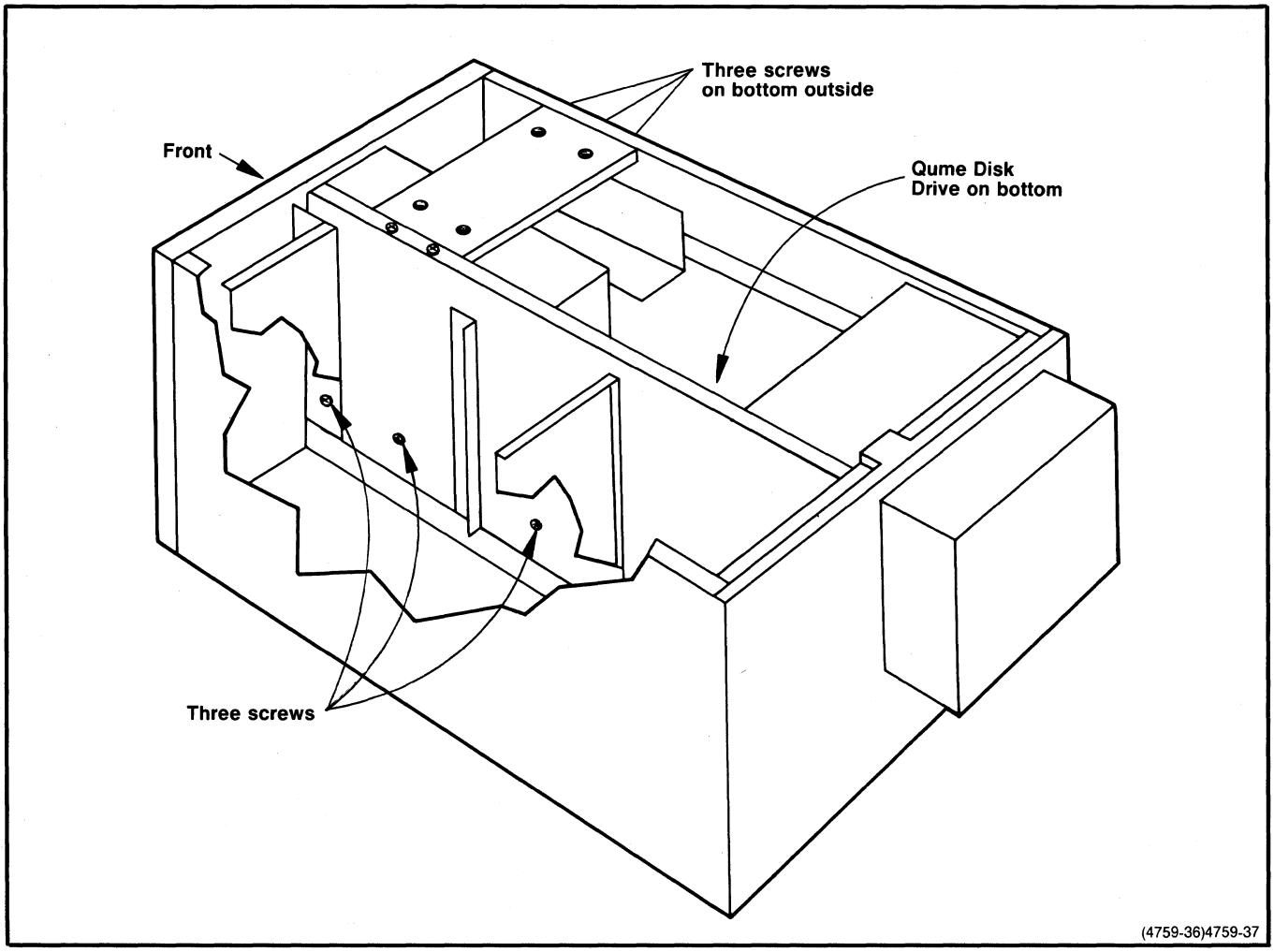


Fig. 15-8. Qume disk drive screw locations.

INSTALLING THE FLEXIBLE DISK DRIVE UNIT

To install a flexible disk drive unit, reverse the removal process. Then reinstall all previously removed circuit boards in the main card cage. Install top and side covers and secure the covers with the corner plastic retainers.

ACCESSING THE FLEXIBLE DISK DRIVE FOR HEAD ALIGNMENT

To align the flexible disk drive head, or to perform an azimuth check using 8560 firmware, you do not need to remove the drive unit from the 8560. You can access the drive unit from the 8560 cabinet bottom using the following procedure:

1. Remove the four cover retainers at the rear of the 8560.
2. Remove the hard disk drive(s) as described in "Removing the Winchester-Type Disk Drive," earlier in this section.
3. Slide the bottom cover toward the rear and remove it completely. Turning the 8560 on either side will facilitate this step.

You now have access to all adjustments and testpoints needed to perform a firmware-aided head alignment or azimuth check. Service routines to perform those operations are described in Section 13 of this manual. The actual procedures are described in the **QumeTrak 242 Flexible Disk Drive Service Manual.**

REMOVING THE XEBEC S1410 DISK CONTROLLER

The Xebec S1410 Disk Controller Board is removed through the top of the instrument. Figure 15-9 shows the Xebec Board with cable and screw locations. Refer to this illustration as you perform this procedure.

1. Remove the top and left side cover panels, as explained earlier in this section.
2. Remove the hard disk drive(s) as described in "Removing the Winchester-Type Disk Drive," earlier in this section.
3. Unplug the center 50-pin ribbon cable from the Xebec Board. Remove the power connector at the top rear of the unit.
4. Turn the 8560 on its right side with the Xebec Board facing up, and remove the four nylon screws (one in each corner of the board).
5. Lift the board out of the unit.
6. Remove the two flat cables from the old board and attach them to the new board.

NOTE

Prior to installing a new disk controller, see the default strapping configuration information in Section 3 of this manual.

INSTALLING THE XEBEC S1410 DISK CONTROLLER

To install the Xebec S1410 Disk Controller Board, reverse the removal process. Be careful not to overtighten the nylon screws.

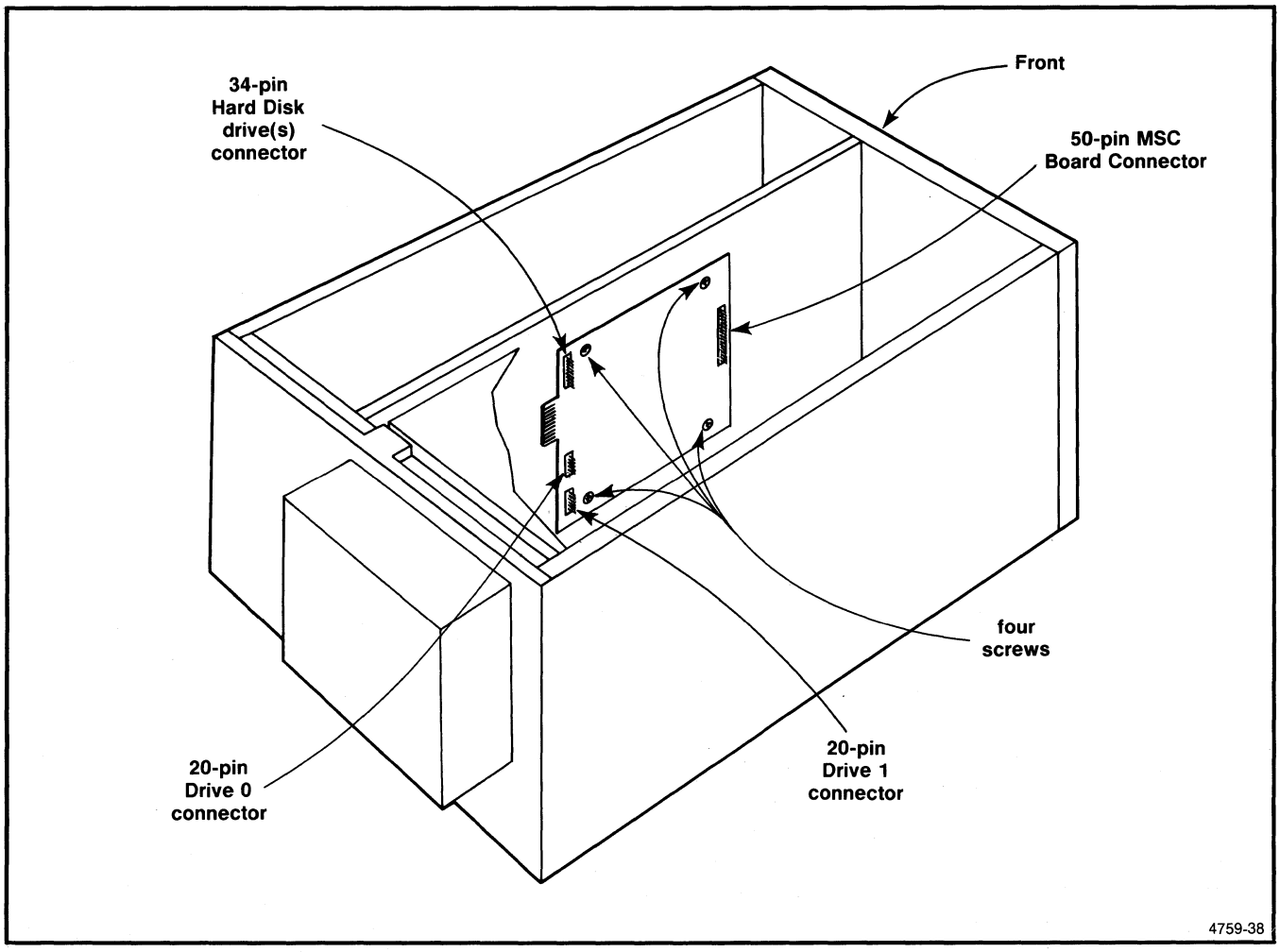


Fig. 15-9. Xebec Disk Controller Board cable and screw locations.

Section 16
DISK-BASED DIAGNOSTICS

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Section 16

DISK-BASED DIAGNOSTICS

INTRODUCTION

This section describes the 8560 disk-based diagnostics. The diagnostics consist of eight individual tests:

1. RAM test—checks the 8560 system memory
2. ROM test—checks the 8560 boot and diagnostic memory
3. CPU test—checks the LSI-11 processor
4. LTC test—checks the Line-Time Clock
5. Printer ports test—checks the printer ports
6. IOP test—checks the IOP channels
7. Disks test—checks the read/write capability of the disks
8. GPIB test—checks GPIB hardware

These tests check the same hardware as the ROM-based diagnostics discussed in Section 13 of this manual but check it more thoroughly. In addition, a separate system interaction test checks how well the different elements of the tested 8560 system hardware work together. The system interaction test executes automatically every time all the diagnostic tests are executed in a series.

NOTE

Throughout this section, all addresses are shown in octal notation unless otherwise noted.

This section is organized into four major parts:

1. General information introducing the disk-based diagnostics, giving a summary of tests and their functions and providing other information of general interest
2. Instructions for executing the 8560 disk-based diagnostics
3. Detailed descriptions of individual test routines
4. A summary of all terminal-displayed error messages

The disk-based diagnostics outlined in this section are distinct from the ROM-based power-up tests described in Section 13. The disk-based diagnostics are contained on a flexible disk and can be accessed from a terminal connected to LP2 or to one of the I/O Processor (IOP) terminal ports.

The 8560 disk-based diagnostics can execute within an 8560 system or a combined 8560/8540 system.

HARDWARE RESTRICTIONS

The 8560 diagnostics work only if the 8560 kernel is operational. The kernel consists of:

- Power supplies
- LSI-11 processor
- The lower memory board
- The portion of the Utility Board containing the boot ROM
- Either an IOP Board or that portion of the Utility Board that controls a serial I/O channel (LP2)
- The I/O Adapter (IOA) Board and I/O Connector (IOC) Board
- The MSC Board
- The flexible disk drive

8560 DIAGNOSTICS OVERVIEW

The following basic procedure is used for running the diagnostics:

1. Insert the diagnostic disk into the 8560 flexible disk drive.
2. If the 8560 is already on, toggle the front panel RESTART switch. Otherwise, turn on the 8560.
3. Answer the questions that appear on your terminal.

The "Typical Operating Procedure," later in this section, provides a more detailed explanation.

Figure 16-1 is a flowchart of the 8560 diagnostics procedure.

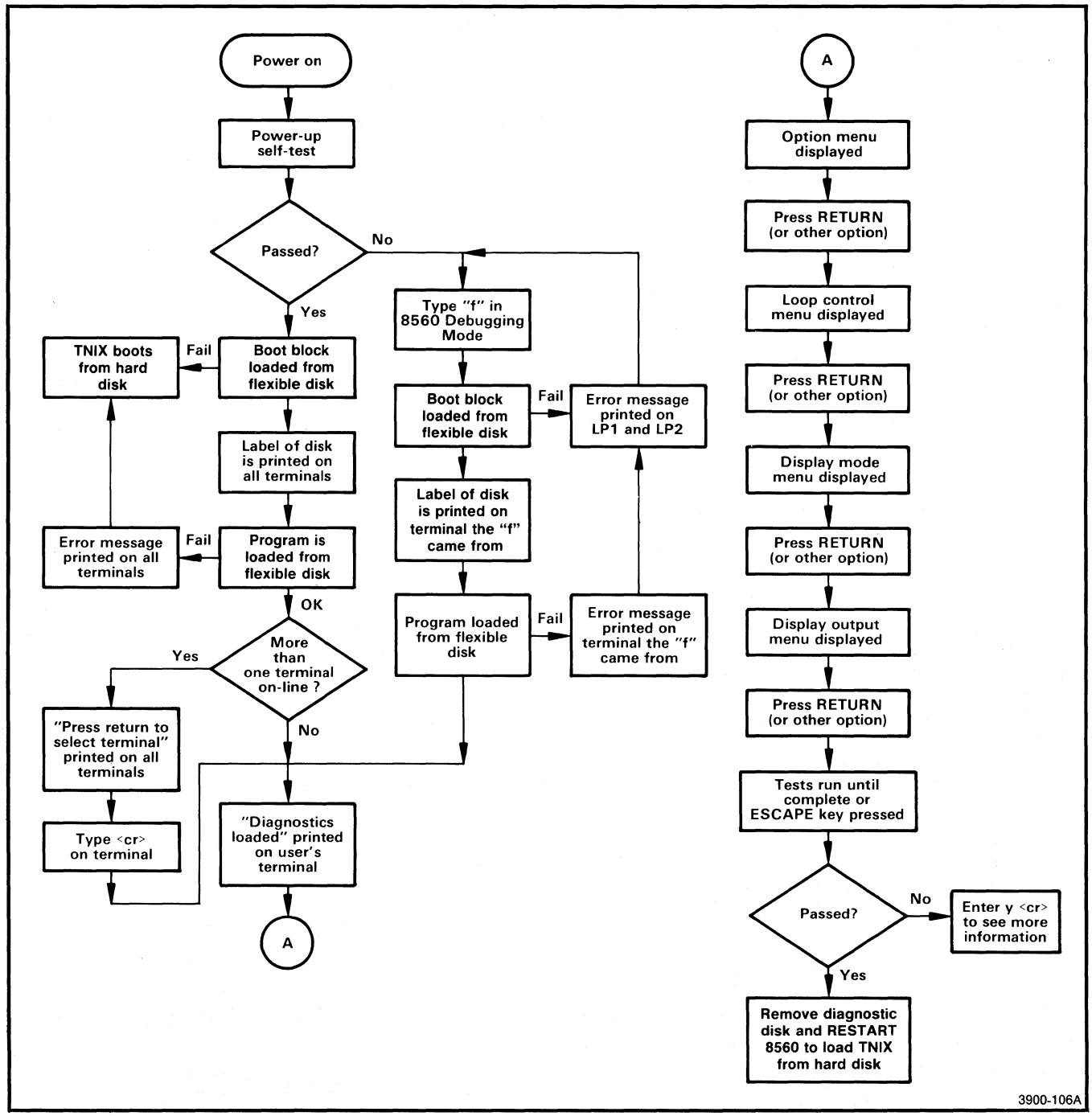

Fig. 16-1. 8560 diagnostics flowchart.

The 8560 diagnostic program, which consists of a single file called "diag60.sav", resides on one flexible disk written in the TNIX file structure. The disk is self-loading and does not require either the TNIX operating system or the hard disk for loading. Once this file is loaded, it remains in system memory until the 8560 is restarted.

The diagnostics are nondestructive in that they will not corrupt any directories or files on the disks in the 8560. A terminal connected to any serial I/O port in the system (except LP1) may be used to communicate with the program.

8560 Menu Descriptions

To perform all 8560 diagnostics functions, four menus are provided: the Option, Loop Control, Display Mode, and Display Output menus. If you want to select a test or function listed in one of the menus, enter the number that precedes that test or function, and then press RETURN. If you want to select the default option, simply press RETURN.

The Option Menu

The Option Menu is the first 8560 menu displayed on the system terminal after the 8560 has passed its power-up tests. Display 16-1 shows the Option Menu as it appears on the terminal screen.

Run all tests. This item executes the test series once. When the 8560 has passed all eight tests, the diagnostic program executes the system interaction test which determines whether all checked system components interact properly with each other. If you do not specify an individual test, this option is selected by default.

Run specified tests. Items 1 through 8 are run codes that each specify an individual test routine to be executed.

Help. This item displays information that explains all of the options in the display.

The Loop Control Menu

After you choose one of the Option Menu tests, the diagnostic program displays the Loop Control Menu. This menu allows you to select a looping option. Display 16-2 shows the format of the Loop Control Menu as it appears on the terminal screen.

```
856x Diagnostic Disk V1.x

Press RETURN to select terminal

******** 856x Diagnostics - Version 1.x - Loaded ********

Option Menu

0 - Run all tests    [default]
1 - Test 856x RAM
2 - Test 856x ROM
3 - Test 856x Processor
4 - Test 856x Line-Time Clock
5 - Test 856x Printer Ports
6 - Test 856x IOP Channels
7 - Test 856x Disk Drives
8 - Test 856x GPIB controller
h - Help

Type in option {<CR>} or {0 - 8 or h and <CR>}
?
```

Display 16-1

```
Loop Control Menu

1 - Do not loop on test   [default]
2 - Loop on test
3 - Loop until error
h - Help

Type in loop control {<CR>} or {1 - 3 or h and <CR>}

?
```

Display 16-2

```
Display Mode Menu

1 - Display run-time status   [default]
2 - No run-time display
h - Help

Type in mode {<CR>} or {1 - 2 or h and <CR>}
?
```

Display 16-3

Do not loop on test. This item executes the selected test option only once. Select the "no looping" option either with a RETURN or with a "1" followed by a RETURN.

Loop on test. This item continuously repeats the selected test option until you press the ESC key.

Loop until error. This item continuously repeats the selected test option until an error is encountered, or until you press the ESC key.

Help. This item displays information that explains all of the options in the display.

Display Mode Menu

This menu is displayed after you select either item 1, 2, or 3 from the Loop Control Menu. Display 16-3 shows the Display Mode Menu as it appears on the terminal. The display mode option allows you to turn the run-time status displays either on or off. (For an example of the run-time status display, see Display 16-5.) You can select either item 1, 2 or Help.

Display run-time status. This option displays messages during the tests to describe what is going on. Select this option by entering a RETURN or a "1" followed by a RETURN.

No run-time display. This option disables the run-time display (but input prompt messages are still displayed).

Help. This item displays information that explains both of the options in the display.

Display Output Menu

This menu selects the peripheral device on which the test data is displayed. Display 16-4 shows the Display Output Menu as it appears on the terminal. This menu is the last 8560 menu displayed. Press RETURN to display the test data on the terminal. You may alternatively display the error information on a line printer connected to either LP1 or LP2.

Help. This item displays information that explains all of the options in the display.

```
Display Output Menu

  1 - Display on terminal     [default]
  2 - Display on printer 1
  3 - Display on printer 2
  h - Help

  Type in display output (<CR>) or (1 - 3 or h and <CR>)
  ?
```

Display 16-4

```
Beginning of pass 1        Elapsed time:   0 : 0 : 0
Testing RAM.................
Testing ROM...
Testing Processor...
Testing Line Time Clock...
Testing Printer Ports...
Lpr1
Nothing connected to Lpr1 - press RETURN to continue?
Lpr2
Testing IOP channels...
IOP1....
Nothing connected to channel 3 - press RETURN to continue?
Testing disk drives...
Flex disk drive
Writing to unused blocks between 137 and 1994
Hard disk drive(s)
Writing to unused block 69599 on hard disk 0
Testing GPIB controller
```

Display 16-5

The Diagnostics Test Series

Instead of executing tests individually, you can execute all diagnostic tests sequentially. When you press RETURN (or "0" followed by a RETURN), the diagnostic program executes all tests in the sequence shown. When the tests are executed in a series, all error information is displayed at the end of the series.

While the diagnostic program is executing the test series, the program keeps you informed about test status on the terminal. As each test is executed, the terminal displays the name of each test. Each time the test series executes, the terminal displays the time that has elapsed since the test series was started.

When you execute the 8560 test series, a display similar to Display 16-5 is shown on the terminal.

The System Interaction Test

When you execute all tests in a series, the diagnostic program automatically proceeds to the system interaction test after the last test is executed.

The system interaction test checks that all individual system components work together as designed. This test cannot be selected individually; it is always part of the test series. The system interaction test requires about a minute to execute and displays the contents of the error registers on the terminal, as shown in Display 16-6. The error registers' contents change continuously, as this test exercises the system. If the system passes the system interaction test, you can be reasonably sure that your 8560 is operating properly.

If you respond with a "y" and RETURN, statistical data similar to Display 16-7 appears on the terminal. Information only appears for the tests you run.

If you respond with an "n" and RETURN, the Option Menu is displayed again.

```
Beginning device interaction test (error counters in octal)...
  ROM    RAM    CPU    INT    BUS    LTC   IOP1   IOP2   LPR1   LPR2   DISCS
000000 000000 000000 000000 000000 000000 000000 000000 000000 000000 000000

Results of 856x Diagnostics V1.x  Copyright 1981, Tektronix, Inc.
856x verification passed. Do you want to see more information?
Type y or n
?
```

Display 16-6

```
Note: addresses and register values are listed in octal
Number of test cycles: 1       Elapsed time:   0 : 1 : 26
RAM -
  memory installed: 256 K bytes
ROM -
  utility board PROM part number(s): 160 2634 01, 160 2633 01
CPU -
  standard processor installed
LTC -
  frequency = 60 hz, status: 000340
Lpr1 -
  line printer connected
  baud   rcsr   rbuf   xcsr   xbuf
  2400  040000 000000 070200 000000
Lpr2 -
  test plug connected
  baud   rcsr   rbuf   xcsr   xbuf
  2400  160000 000000 070200 000000
IOPs -
  IOP1 PROM part number(s): 160 1408 01, 160 1407 01, 160 1406 01
  HSI I/O 0 - terminal connected,  current baud rate = 2400
  HSI I/O 1 - terminal connected,  current baud rate = 2400
  HSI I/O 2 - test plug connected,  IOA set for HSI
  HSI I/O 3 - nothing connected,  IOA set for terminal

Disks -

 PMS/MSC controller board Prom part number(s): 160 2219 00, 160 2218 00

 flexible disk: double-sided, double-density

 hard disk 0 capacity = 69599 blocks (35 M bytes)

GPIB -
 GPIB controller board PROM part number(s): 160 1820 00
 local RAM size: 32 K bytes
 status of device at 0, 4 = 16 (decimal)

 856x verification passed
 Ready for next menu (press RETURN)?
```

Display 16-7

Diagnostics Failure

If some 8560 boards do not pass a particular test, the diagnostic program displays warning messages while that test executes. After the system interaction test is completed, you may request that the diagnostic program display statistical information as shown in Display 16-7.

Display 16-7 shows statistical data from an error-free run. If any errors occur during diagnostic testing, they will be reported along with the statistical data in this display. The error messages that can be displayed by the diagnostic program are explained later in this section in the "Error Displays" discussion. These error messages enable you to determine whether the failures are serious enough to warrant further investigation and/or repair.

TYPICAL OPERATING PROCEDURE

The following procedure may be used to run the entire 8560 diagnostic test series once. (The same procedure can be used to run individual diagnostic tests by selecting a different option.)

Fixtures Required

The serial ports can be partially tested without any additional hardware. However, to fully exercise the 8560 ports, one or more wrap-back connectors are required. Wrap-back connectors are RS-232-C-type connectors wired so that output signals from the port are fed back into the same port. (A wrap-back connector is referred to as a "test plug" in displays produced by the diagnostic program.) Thus, data transmitted by a port is received by the same port. Wrap-backs connectors can be ordered from Tektronix, Inc.

NOTE

When performing this procedure on a terminal connected directly to an IOP channel jumpered for RS-232-C operation, set the terminal for 2400 baud if it can be done from the keyboard. If the terminal is not set for 2400 baud, the first message from the diagnostic program will be garbled.

Procedure

The following paragraphs describe the procedure for running the 8560 diagnostic test series.

Verify that your terminal is properly connected to the system. Turn the terminal on. If the terminal is connected to the 8560 through an 8540 Integration Unit, turn the 8540 on and make sure it is in its transparent mode. Refer to the *8540 System Users Manual* for information about the 8540.

Turn on the 8560's ac power switch (located on the rear panel of the unit) and the dc power switch (located on the front panel of the unit). Both the DC ON and AC ON indicators on the front panel will light. The whining noise you hear is caused by the spinning of the hard disk and the fan. The PROCESSOR BUSY indicator will light and remain on.

Insert the 8560 diagnostic disk into the flexible disk drive. Within approximately 30 seconds, the access light indicator on the front panel will light as the 8560 reads the boot block off the disk. (If the system is unable to boot from the disk, refer to the "System Won't Boot" discussion, following this procedure.)

The following message will appear on the screen:

```
856x Diagnostic Disk V1.x
```

If the message appears garbled, check that your terminal's baud rate is set at 2400.

If more than one terminal (and/or a line printer connected to LP2) is online, the following message appears:

```
Press RETURN to select terminal
```

After you have pressed RETURN, if the display appears garbled, press the BREAK key to select a new baud rate. Continue pressing the BREAK key until you see the message "new baud rate selected". Now press RETURN.

The following message will be displayed:

```
******** 856x Diagnostics - version 1.x -
loaded ********
```

This message is followed by the Option Menu. If the display appears garbled, press the BREAK key until the message "new baud rate selected" appears. Then press the ESC key to cause the Option Menu to be printed.

Press RETURN to select the "Run all tests" option. The Loop Control Menu will be displayed. Press RETURN to disable the looping options.

At this point, the Display Mode Menu will be displayed. Press RETURN to enable the run-time display.

The Display Output Menu will now be displayed. Press RETURN to direct the output to your terminal.

The tests will begin running. A run-time display similar to that shown in Display 16-5 will be displayed.

When the program tests a serial I/O port and discovers nothing is connected to the port, the following message is displayed:

```
nothing connected to port x - press RETURN
to continue?
```

If the foregoing message is displayed, you can connect a terminal or wrap-back connector to the port and then press RETURN. You can rearrange connectors whenever the program is paused. This enables you to use one wrap-back connector to test all of the ports.

After the test series is completed, the following message will appear:

```
Verification passed.  Do you want to see
more information?
Type y or n
```

If you type a "y" and press RETURN, the program displays information about how your 8560 is configured. If you don't want to perform any more tests, remove your diagnostic disk and toggle the RESTART switch to boot the TNIX operating system.

System Won't Boot

If the system won't boot from the diagnostic disk, read through the following four situations. Find the situation that describes the condition of your system, and follow the directions provided.

Situation 1

The light on the flexible disk drive flashes briefly, then the 8560 loads the operating system off the hard disk.

The 8560 firmware decided that booting the flexible disk was impossible. Perform the following steps:

1. Remove jumper P1036 from the Utility Board.
2. Connect a line printer to LP1 or LP2, or connect a terminal to LP2. (These two ports are used by the firmware to report errors.)
3. RESTART the 8560.
4. When you see the "=" prompt on your terminal, press "f". Three error codes should print out. For an explanation of these codes, refer to "Error Summary" at the end of Section 13 in this manual.

Situation 2

The light on the flexible disk drive stays on for a period ranging from several seconds to over a minute. After the light goes out, an error message is displayed on one or more terminals (at 2400 baud). TNIX is then loaded. This means that the boot block was loaded from the disk, but the file could not be loaded.

If this situation occurs, perform the following steps:

1. If the message displayed was not legible, set the baud rate of your terminal to 2400 baud and RESTART the 8560.
2. If the message concerns an invalid file system, the directory and/or diagnostic file on your flexible disk may have been altered. If you suspect a problem with your disk, substitute another disk.
3. If the message refers to disk read errors, a problem may exist with your flexible disk, or with your flexible disk drive. Substituting another disk or cleaning the heads may solve this problem. (A head cleaning procedure is described under the "Alignment Aid" description in Section 13 of this manual.)

   If this does not solve the problem, refer to the MSC error code summary at the end of this section. The error code displayed may indicate why the read error occurred.

Situation 3

Neither TNIX nor the diagnostic disk can be loaded and executed.

This generally means that a power-up self-test failed. To locate the problem, complete the following steps:

1. Connect a line printer to LP1 or LP2, or connect a terminal to LP2. (These two ports are used by the firmware to report errors.)
2. RESTART the 8560. One of the following events will occur:
   - Within a minute, an error code is displayed.
   - The PROCESSOR BUSY light on the front panel goes out. If this occurs, remove the 8560 top cover, and look at the error code displayed on the Utility Board LEDs. Refer to Utility Board LEDs in Section 13 in this manual.)
3. If the "=" prompt is displayed on your terminal, you may be able to override the error by typing an "f", depending on the type of error detected.

Situation 4

TNIX and the diagnostic disk won't load and the 8560 firmware won't run.

This may be due to bad firmware on the Utility Board. Try the following procedure to manually load the disk diagnostic tests:

1. Insert the diagnostic disk in the flexible disk drive.
2. Connect a terminal to LP2.
3. Set the front panel RUN/HALT switch to the HALT position.
4. Toggle the RESET switch on the front panel.
5. Set the front panel RUN/HALT switch to the RUN position.
6. You are now in ODT mode. Enter the following underlined characters on the keyboard:

```
11000/  xxxxxx    2013  <LF>
011002/ xxxxxx       0  <LF>
011004/ xxxxxx    1000  <LF>
011006/ xxxxxx       0  <LF>
011010/ xxxxxx       0  <LF>
011012/ xxxxxx       0  <LF>
011014/ xxxxxx       0  <CR>
777150/ xxxxxx  11001  <CR>
```

7. You will hear the flexible disk drive activate. When the drive noise subsides (after about a second) enter:

```
R7/  xxxxxx  0          <CR>
P
```

8. The system should now boot from the flexible disk.

Program Stops Running

If the diagnostic program hangs up while executing, and pressing the ESC key does not produce any results, complete the following procedure:

1. Connect your terminal to LP2. The baud rate of your terminal must match the LP2 baud rate (which is set for 2400 at the factory).
2. Raise the front panel RUN/HALT switch, and then lower it again.
3. Enter "3000g" on your terminal. If the diagnostic program is still intact in system memory, the program will display the results from the tests that were previously run.

TEST PROGRAM DESCRIPTIONS

The following discussion provides a summary of the 8560 tests and detailed descriptions of each individual test routine.

Test Summary

Table 16-1 summarizes the disk-based diagnostic routines. For each routine, the table gives the test name, the run code, and a short test description. Figure 16-2 is a block diagram of the 8560. Refer to Fig. 16-2 while reading the test descriptions.

Table 16-1
Diagnostic Test Summary

Name	Run Code	Description
RAM test	1	This test checks the system RAM.
ROM test	2	This test performs a checksum test on bootstrap/diagnostic ROMs, and checks for a valid ROM part number. The test consists of two parts with each part testing one ROM.
CPU test	3	This test checks selected LSI-11 instructions and registers. The CPU test performs a more thorough check of the instruction set than the ROM-based CPU test.
LTC test	4	This test checks the 8560 Line-Time Clock interrupts.
Printer ports test	5	This test checks the two RS-232-C line printer ports.
IOP test	6	This test checks the operation of the IOP ports and the associated DMA circuitry.
Disks test	7	This test verifies the operation of the MSC and the disk drives. The test checks the read/write capability of the disks.
GPIB	8	This test checks for the presence of a GPIB Controller, requests a self-test operation, then allows a serial bus poll of a selected device.

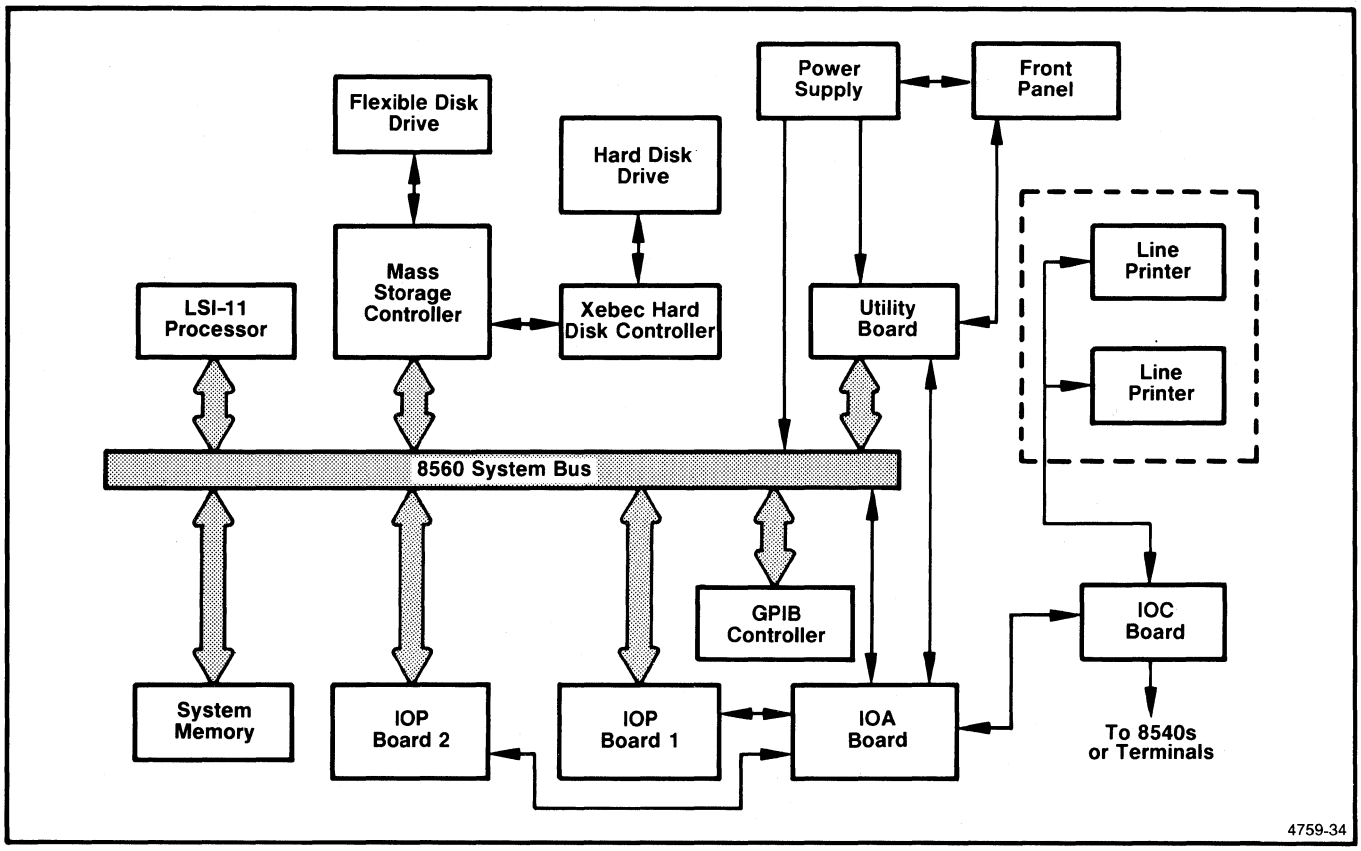

Fig. 16-2. 8560 block diagram.

RAM Test

Run Code: 1

Function: Checks the data storage capability of the system RAM

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: Up to 30 seconds

Description

The RAM test verifies system memory by determining the size of memory, writing patterns into each location, and then reading the patterns back. If you have selected the "Run-time display" option from the Display Mode Menu, the test will print out a series of period characters while executing. Each period that is printed represents a test module that is executed within the RAM test. The test performs the following steps:

1. The first period character of the display is printed if you selected the run-time display.
2. The test first determines how much RAM is installed by writing to memory locations above the program until a bus timeout is detected. An error occurs if less than 64K words of memory is installed or if the memory banks are not unique.
3. The test now verifies that part of RAM occupied by diagnostics by:
   - Saving the contents of each program location
   - Writing complementary test patterns into the location
   - Verifying that the patterns were written
   - Restoring the original contents of each location

   If an error is detected, it is stored in RAM for later display.

4. The test verifies the remaining RAM in the 8560 by:
   - Printing the second period, putting the CPU in user mode, and writing 125252 into every location above the program
   - Printing the third period, then waiting 2.5 seconds (this step is used to verify the refresh circuit)
   - Printing the fourth period, then waiting 2.5 seconds
   - Printing the fifth period, then complementing each word of the test pattern (starting at the bottom of the test area)
   - Printing the sixth period, then verifying each location
   - Printing the seventh period, then complementing each word of test pattern (starting at the bottom of the test area)
   - Printing the eighth period, then reading and verifying each location
   - Printing the ninth period, then complementing each byte of the test pattern (starting at the top of the test area)
   - Printing the tenth period, then reading and verifying each location
   - Printing the eleventh period, then complementing each byte of the test pattern (starting at the top of the test area)
   - Printing the twelfth period, then reading and verifying each location
   - Printing the thirteenth period, then complementing each word twice and adding 1 to each byte (starting at the bottom of the test area)
   - Printing the fourteenth period, then reading and verifying each location
   - Printing the fifteenth period, then complementing each word (starting at the top of the test area)
   - Printing the sixteenth period, reading and verifying each location, and then putting the CPU in kernel mode

If an error occurs, the error information is stored for future display. Note that the interval between printing two successive periods varies (depending on how much memory is installed) but should never be more than about 3 seconds between any two successive periods.

If a parity error interrupt occurs during this test, the location of the error is stored, but the bit fault mask is not. The fault mask is a six-digit octal number, in which each non-zero bit represents a mismatch between the data written and the data read inside the given address range. To determine which bit is at fault, you must disable parity error reporting by moving P7111 on the memory board(s) to position 2 and run the test again. Parity should be enabled again before you reboot TNIX.

It is possible to narrow down the source of a reported error, because the error message prints out both an address range and a mask of the bits that failed. For example, if a single bit failed within a narrow range of addresses, a RAM chip probably failed. The address range in the error message will allow you to identify the failed chip. On the other hand, if more than one bit is set in the fault mask, it is more likely that the support circuitry for the RAMs has failed.

ROM Test

Run Code: 2

Function: Checks the data recorded in the diagnostic/bootstrap ROMs.

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: 1 second

Description

1. Test Low-Byte ROM. The test calculates the checksum and compares it with the checksum stored in the low-byte ROM. The ROM test also reads the ROM-stored part number and determines whether that number is valid.

2. Test High-Byte ROM. The test calculates the checksum and compares it against the checksum stored in the high-byte ROM. The ROM test also reads the ROM-stored part number and determines whether the number is valid.

3. Recall Error Information. If the test is executed alone, and both ROMs have been checked, the program recalls the error information from the system memory and displays it on the terminal. If the test is executed as part of the test series, the diagnostics program displays the error at the completion of the test series.

CPU Test

Run Code: 3

Function: Checks the operation of the CPU by executing a representative instruction set

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: Less than 1 second

Description

The CPU test checks a representative sample of LSI-11 instructions to determine whether the CPU is operating properly. The disk-based CPU test checks more instructions than the ROM-based test. The test executes the simpler instructions first and then proceeds to more complex instructions. The CPU test verifies most LSI-11 operations by checking:

1. A representative set of single-operand instructions with destination mode 0
2. A representative set of single-operand instructions with destination mode 0, using byte mode
3. A representative set of double-operand word instructions using most source modes and using destination mode 0
4. A representative set of double-operand byte instructions using various source modes and using destination mode 0
5. A representative set of word instructions using various source modes and most destination modes
6. A representative set of byte instructions using various source modes and various destination modes
7. The JSR, RTS, and MARK instructions using various modes
8. Trap instructions
9. The MUL, DIV, and ASHC instructions by solving an equation and checking the result
10. The instructions operating in user and kernel mode assuring they work properly when the MMU (Memory Management Unit) is on
11. The floating point function

The CPU test checks the results of the executed instructions. If any result is not correct, the test records the error for later display.

LTC Test

Run Code: 4

Function: Checks the frequency of interrupts from the ac power source

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: 1 second

Description

This test verifies that the processor is correctly receiving line frequency interrupts. The test uses the Line-Time Clock to count the interrupts caused by the line frequency.

1. Initialize Interrupts. The LTC test starts by setting up the LTC vector and enabling the LTC interrupts. The test detects the first interrupt, then waits in a loop for 1 second while the LTC handler counts the number of interrupts that occur. The program then disables interrupts and checks the interrupt counter. If the frequency of the LTC is between 48 and 52 Hz, the frequency is stored as 50 Hz. If the frequency is between 58 and 62 Hz, the frequency is stored as 60 Hz. All other frequencies are considered invalid and are reported without rounding. If an invalid frequency is reported, the program logs the error and stores the frequency.

2. Display Errors. If the test is executed alone, the program recalls the error information from the memory and displays it on the terminal. If the test is executed as part of the test series, the error data is displayed at the completion of the test series.

Printer Ports Test

Run Code: 5

Function: Check the two line printer (RS-232-C) ports

Blocks Involved: LS1-11 Processor, Utility Board, System Memory, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: Up to 20 seconds

Description

The printer ports test consists of two identical parts. The first part checks LP1, and the second checks LP2. Each part is divided into individual routines, depending on the system configuration. The printer ports test can check the two ports under the various conditions determined by the external port connections. This test checks port operation with the port connected to one of the following devices:

- A wrap-back connector
- A line printer
- The terminal from which the test is exercised
- An open circuit

The following test sequence is used for each printer port:

1. The test displays the name of the port under test on your terminal if the "run-time display" option was selected from the Display Mode Menu.
2. The test determines whether the printer control registers can be accessed. If not, the test logs the error and discontinues testing this printer interface.
3. The test exercises the CTS line to determine whether any device is connected to the port. If the DTR signal is not detected, the test assumes that nothing is connected and notifies you. After you acknowledge this notification by pressing RETURN, the test again checks the port to see if any device is connected.
4. The test verifies that the bits in the interface registers can be turned on and off. If any bit fails, the test logs an error.
5. The test determines the vector address of the transmit interrupt if any device is connected to the port (DTR has been detected). The vector address determines whether the port is strapped for terminal or printer operation. If the port is not strapped for printer operation, an error is logged.
6. The test exercises the transmit and receive circuits by transmitting a series of characters through the wrap-back connector if a wrap-back connector is installed. The test transmits characters at various baud rates by reprogramming the interface, and checks these baud rates against the line frequency. Since this process takes about 10 seconds, the test prints out three period characters during this step.
7. The test verifies overrun error checking by transmitting several characters without emptying the receive buffer if a wrap-back connector is installed.
8. The test transmits the following test pattern if a line printer is connected:

```
!"#$%&'()*+,-./0123456789:;<=>?@AB
CDEFGHIJKLMNOPQRSTUVWXYZ[]^
_`abcdefghijklmnopqrstuvwxyz{|}~
```

9. The test retrieves the error information from the system memory and displays it on the terminal if the printer ports test is executed alone. The error information is displayed at the end of the series if the test is executed as part of the test series.

IOP Channel Test

Run Code: 6

Function: Check the I/O channel operation

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, IOA, IOC Board and IOP Board (See Fig. 16-2.)

Duration: Up to 30 seconds

Description

The IOP Channel test consists of two identical parts. The first part checks IOP Board 1 (channels 0 through 3), and the second checks IOP Board 2 (channels 4 through 7). At least one IOP Board must be installed for the test to pass. If two boards are installed, both are tested.

Each test part consists of individual test routines that are assembled to match the system configuration. If the jumper plug on the IOA Board for a particular channel is in the RS-232-C position, the test will automatically execute a set of routines for any of the following configurations (depending on what is connected to the IOP channel):

- A wrap-back connector
- A terminal
- An open circuit

If the jumper plug on the IOA Board for a particular channel is in the HSI position, the test will automatically execute a set of routines for any of the following configurations (depending on what is connected to the IOP channel):

- A wrap-back connector
- An 8540
- An open circuit

The following test sequence is used for each IOP Board:

1. The test attempts to read the Device Register on the IOP Board. If a bus time-out occurs, the test assumes the board is not installed and stops testing the board.
2. The test prints the name of the board under test if the "run-time display" option was selected from the Display Mode Menu.

3. The test issues a self-test command to the board under test. This causes the IOP Board to verify its ROM, RAM, and DMA and to verify that certain control circuits respond. On completion, the IOP writes its PROM part numbers and status into 8560 RAM and issues an interrupt to the LSI-11 processor. If the test program times out without receiving the interrupt, the program logs the fact that no interrupt was received. If the status is invalid, the program logs an appropriate error code. (Note that in this part of the test, the program may ignore keyboard interrupts.)
4. The routine tests each of the four IOP channels individually after the self-test is completed, using the following steps:
   a. If the "Run-time display" option was selected from the Display Mode menu, the routine prints a period character.
   b. The routine requests HSI status for the IOP channel. The routine uses the response to determine whether the jumper block on the IOA Board is in the RS-232-C or HSI position.
   c. If the channel is jumpered for a terminal, the routine tells the IOP to assert CTS and then check for DTR. If DTR is not present, the output of the channel is assumed to be an open circuit, and the routine skips to step h.
   d. The routine "characterizes" the channel. This characterization involves telling the IOP what baud rate to use for the channel, how characters are to be echoed, and what to return if a framing error is detected. The routine tells the IOP to return a <null> any time a framing error is detected. You may get confusing results if you type a <null> on the keyboard while the diagnostics are running.
   e. The routine tells the IOP to return a character if the IOP receives a character on this channel.
   f. The routine tells the IOP to transmit a RETURN on this channel. If after 0.07 seconds the character has still not been transmitted, the routine assumes the channel is an open circuit and skips to step h.
   g. If the routine receives a RETURN from this channel, the routine assumes that a wrap-back connector is attached. If nothing is received from the channel, the routine assumes that either a terminal or an 8540 is connected depending on the position of the IOA jumper block.
   h. The routine recharacterizes the channel using parameters that are appropriate for the device connected to the channel. The routine now branches to one of the following steps (i, ii, or iii), depending on which device is connected to the channel.
      i. If the test has determined that the connector is an open circuit, and if this is the first pass of the test, the routine reminds you that the circuit is open. At this point you have the option of connecting a device to the port. When you press RETURN, the routine repeats steps b through h to see if the connector is still an open circuit. If the circuit is still open, the routine goes back to the beginning of step 4 or goes on to step 5, depending on whether this is the last IOP channel to be tested.
      ii. If a wrap-back connector is installed, the test exercises the transmit and receive functions of the channel by transmitting a series of characters through the wrap-back connector. The test exercises these functions at various baud rates by reprogramming the interface. The test also checks the throughput rate against the line frequency to determine whether the baud rate circuitry is being programmed correctly. Note that baud rate verification is performed only on channels that are jumpered for terminals; the HSI baud rate of 153.6K is not verified by this test.
      iii. If a terminal or 8540 is connected to this channel, but this is not the channel that you are using (as determined by the diagnostics after boot-up), the routine transmits the message:

```
Diagnostics in progress.
No logins.
```

      The routine does not automatically perform character input testing in part iii, but you can still verify that this channel works by typing characters on the terminal connected to this channel (or to an 8540 connected to this channel), and noting that the characters are echoed.

      If the IOA is set up for HSI mode, this verification also checks the baud rate of 153.6K. If a terminal is connected, you can use the BREAK key to select different baud rates as outlined in the "Typical Operating Procedure", earlier in this section. This type of verification can be performed at any time, not just during the IOP channels test.

5. When all four channels of the IOP Board have been tested, the program displays an error count if any errors have occurred. (If the "run-time display" option was selected from the Display Mode Menu, the error count is not displayed.)

6. After both boards have been checked, and if the IOP test was executed alone, the program retrieves the error information from memory and displays it on the output device. If the test was executed as part of the test series, the error information is displayed at the end of the series.

Disks Test

Run Code: 7

Function: Checks the operation of the MSC Board and the disk drives

Blocks Involved: LSI-11 Processor, Utility Board, System Memory, MSC Board, Xebec Disk Controller, Flexible Disk Drive, Hard Disk Drive, IOA, IOC, and IOP Boards (See Fig. 16-2.)

Duration: Less than 1 minute

Description

1. The test attempts to read the Device Register on the MSC Board. If a bus time-out occurs, the test stores an error code in system memory and makes an exit.
2. The test issues a self-test command to the MSC. This command causes the MSC to verify its own RAM and ROM, the DMA interface, the interrupt circuitry, the interface to the disk drives, and the ability of the controller to move the heads. The test does not, however, check the read/write capability of the drives. The MSC also reports the part numbers of its PROMs.

   The program logs one or more error codes if the self-test command doesn't issue an interrupt to the LSI-11 or if the command returns invalid status bytes.
3. The test informs you that it is checking the flexible disk drive. The test then asks the MSC what type of disk is in the flexible disk drive. If an invalid response is returned, the test logs an error code.
4. The test searches the directory to locate the free (unused) blocks if a disk is in the flexible disk drive. The test skips to step 5 if free blocks can be located. If not, the test gives you the option of choosing a read/write test (which will erase the disk) or a read-only test on the entire disk. If the test cannot locate free blocks, one of the following conditions exists:
   - All blocks on the disk are used
   - The directory is unreadable
   - The directory is not a TNIX fbr-type directory
   - The directory is corrupted

CAUTION

If the test is looping, do not change flexible disks after the first test pass; the test may write over used blocks on the new disk. The disks test searches for free blocks only during the first test pass. If you substitute another disk after the free block search, the test will not perform another search.

5. The test writes to five randomly-selected blocks within the permitted range if there are free blocks on the flexible disk, or if you have decided to let the program write on the disk anyway (and the disk is not write-protected). The test then reads back the information to verify the write operation. If a read-only test is being run, the test simply verifies the CRCs (cyclic redundancy checks) on five randomly selected blocks.
6. The test reads the first four blocks of track 0 into a high-address memory area if there is a disk in the flexible disk drive. This is simply to verify that the boot block area on the disk is readable and that the MSC can access upper RAM addresses in the 8560.
7. The number of recoverable errors is displayed if any recoverable errors were detected during the test (for example, the MSC was able to read data after several tries). Recoverable errors are usually due to worn flexible disks or dirty heads. Unless these errors occur consistently (for example, once per test pass), they may be ignored.
8. The test informs you that it is testing the hard disk drive. The test then asks the MSC what the disk capacity is. If the controller returns an invalid response, the test logs an error code.
9. The test writes and reads a special reserved service block on the disk, which is not accessible by TNIX. The test compares the data to make certain the data was written correctly.
10. The test reads from 10 randomly selected blocks on the disk and verifies their CRCs.
11. The test reads the first four blocks of the hard disk into a high-address memory area. This verifies that the boot block area on the disk is readable, and that the MSC can access upper RAM addresses in the 8560.
12. The number of recoverable errors is displayed if any recoverable errors were detected during the test. Recoverable errors may result from reading blocks that were in TNIX's bad block list (and therefore not used by TNIX). Running the TNIX syschk program ensures that TNIX never accesses the bad blocks but does not prevent diagnostics from reading the bad blocks.
13. If the disks test is executed alone, the error data is retrieved from system memory and displayed on the terminal. If the test is executed as part of a test series, the error information is displayed at the end of the series.

GPIB Test

Run Code: 8

Function: This test checks for the presence of a GPIB Controller and, if found, requests a self-test operation. Upon successful completion, this test allows the user to perform a serial poll of an external device.

Blocks Involved: LSI-11 Processor, System Memory, MSC, GPIB Controller (See Fig. 16-2.)

Description

1. The test attempts to read the Device Register on the GPIB Controller Board. If a bus timeout occurs, it then tries to read the alternate Device Register address. If the alternate address also fails, the test assumes no GPIB Controller is installed, reports "not installed," and exits.
2. This test issues a no-op command to the board to verify its DMA addressing if the Device Register responds at the correct address. Possible errors are "board does not process commands," "missing interrupts," and "DMA error."
3. A self-test command is sent to the GPIB Controller firmware if the no-op command completes without errors. This command causes the GPIB Controller to sequentially test its RAM, ROM, CPU, GPIB chip, and DMA interface to the CPU. This test does not, however, check the GPIB path beyond the GPIB Controller itself. The program will log an error code if the self-test does not complete with correct status, does not return an interrupt and does not alter the scratch buffer allocated to it for DMA interface testing. There is a failsafe timeout just in case the GPIB command does not complete. The error code returned by the board (if any), as well as the PROM part number(s) and on-board RAM size, are also logged for later display.
4. If the GPIB Controller Board self-test completes with no fatal errors, (i.e., no error occurred which would prohibit GPIB traffic), then, as a final check, the user may elect to verify the external GPIB interface by conducting a serial poll of a selected device. During the initial pass of the GPIB Controller test, the user is asked if a serial poll of an external device should be performed ("Poll external device?"). If this option is selected, the user is prompted to supply the primary (and secondary, if used) GPIB address of the device (default is 0 and 4 is for the Dylon tape controllers).

   Since no serial poll routine resides in the GPIB firmware, a serial poll test file residing on the diagnostic disk is loaded into system memory, down-loaded into the GPIB Board and executed. If there is no response to the serial poll within the allotted time, the test reports the error ("device at address PP [,SS] does not respond"). Otherwise, the most recent status is logged for later display. As in the self-test, any error codes returned by the serial poll routine are logged for later display.

Device Interaction Test

Run Code: Only executes after all the other tests have been run

Function: Checks that all 8560 devices interact with each other properly

Blocks Involved: All (See Fig. 16-2.)

Duration: Less than 1 minute

Description

This test consists of a foreground task (the RAM test described previously), and a number of background tasks that are interrupt-controlled and DMA-controlled. These background tasks consist of parts of the LTC test, the printer ports test, the IOP test, and the disks test. The ROM test and CPU test are not rerun, but the CPU is tested implicitly. If the "run-time display" option was selected from the Display Mode Menu, a set of error counters will be continuously reprinted in octal during the device interaction test. These error counters are also displayed on any other terminals that are online. If any of these error counters is not zero, the test will display a more detailed error message explaining the counter after the test is stopped.

ERROR DISPLAYS

At the end of a set of tests, you will see a display similar to Display 16-8.

The following is an explanation of the messages in Display 16-8:

- "NNNNN" is the number of errors detected
- "Function A" is the name of the function that caused errors
- "Device X" is the name of the module or board that is the likely culprit
- "Device Y" or "device Z" are less likely culprits

When you type "y" and RETURN, you will see a display or printout similar to that in Display 16-9. Information appears only for those tests run.

```
***Warning***  NNNNN function A error(s)
   Probable source: device X
   Other possibilities: device Y, device Z
   Verification [failed or passed]. Do you want to see more information?
   Type y or n
   ?
```

Display 16-8

```
Note: addresses and register values are listed in octal
Number of test cycles: 1        Elapsed time:   0 : 1 : 26
RAM -
  memory installed: 256K bytes
ROM -
  utility board PROM part number(s): 160 2634 01, 160 2633 01
CPU -
  standard processor installed
LTC -
  frequency = 60 hz, status: 000340
Lpr1 -
  line printer connected
  baud   rcsr   rbuf   xcsr   xbuf
  2400  040000 000000 070200 000000
Lpr2 -
  test plug connected
  baud   rcsr   rbuf   xcsr   xbuf
  2400  160000 000000 070200 000000
IOPs -
  IOP1 PROM part number(s): 160 1408 01, 160 1407 01, 160 1406 01
  HSI I/O 0 - terminal connected,  current baud rate = 2400
  HSI I/O 1 - terminal connected,  current baud rate = 2400
  HSI I/O 2 - test plug connected,  IOA set for HSI
  HSI I/O 3 - nothing connected,  IOA set for terminal

Disks -
  PMS/MSC controller board PROM part number(s): 160 2219 00, 160 2218 00

  flexible disk: double-sided, double-density

  hard disk 0 capacity = 69599 blocks (35M bytes)

GPIB -
  GPIB controller board PROM part number(s): 160 1820 00
  local RAM size: 32K bytes
  status of device at 0 , 4 = 16 (decimal)

856x verification passed
Ready for next menu (press RETURN)?
```

Display 16-9

Display 16-9 shows statistical data from an error-free run. If any errors occurred during diagnostic testing, they will be reported along with the statistical data in this display. The error messages displayed by the diagnostic program are explained in the following paragraphs.

General Messages

The following messages, if they are used, appear near the top of the display. These messages do not relate specifically to any of the eight diagnostic tests.

Number of test cycles. The number of test cycles that were run or started. If you did not specify looping, there will be only one test cycle.

Elapsed time. The amount of time the test took to run. For a pass of the entire 8560 diagnostic series, this number ranges between 1 to 2 minutes, depending how the 8560 is configured for the test.

Unexpected interrupt vectored at NNNNNN. An interrupt occurred that was not anticipated by the diagnostics. The number represents the interrupt vector address. Standard 8560 interrupts include:

```
000004 - bus timeout or stack overflow
000010 - invalid instruction executed
000014 - BPT instruction
000020 - IOT instruction
000024 - power fluctuation
000030 - EMT instruction
000034 - TRAP instruction
000060 - LP2 I/O
000064 - LP2 (normally unused)
000100 - Line Time Clock
000114 - RAM parity error
000200 - LP1 I/O
000204 - LP1 (normally unused)
000234 - Mass Storage Controller
000244 - floating point
000250 - memory management
000260 - Mass Storage Controller
000270 - Mass Storage Controller
000274 - Mass Storage Controller
000300 - IOP 1
000304 - IOP 2
000310 - IOP 1
000314 - IOP 2
```

If the vector displayed is not on this list, the vector strapping on one of the boards may be incorrect. Run the diagnostic tests individually to determine which board is producing the interrupt.

Stack overflow—possible interrupt problem. The processor detected that its stack pointer was outside the legal range. This problem could occur if the CPU has to process more interrupts than it can handle. This problem could also be caused by a series of unexpected interrupts.

Run the tests individually to determine which board is causing the problem. Also look at other error messages, such as RAM errors or unexpected interrupt errors. It may be necessary to reload the program and start over.

Invalid instruction trap. Possible program error. Restart or press <ESC>. The processor detected an invalid instruction. The presence of an invalid instruction probably means that part of the program has been accidentally altered. The program could have been altered by a number of problems: a CPU error, RAM error, unauthorized DMA operation by another device on the bus, or unexpected interrupts.

Press the ESC key to see if any error messages are printed. Then reload the diagnostic program and run individual tests to isolate the problem.

Memory mapping error. Possible program error. Restart or press <ESC>. The processor reported a memory management exception indicating program corruption. Memory management exceptions are generally caused either by writing to write-protected RAM, or by an unauthorized action of a diagnostic task running in user mode. Also, the program may have been corrupted by a RAM error, CPU error, Memory Management Unit (MMU) error, unauthorized DMA operation on the bus, or an unexpected interrupt. First press ESC to see if any error messages are printed. Then reload the program and run individual tests to isolate the source of the problem.

Power failure detected. Restart or press <ESC>. This message is displayed if a power-fail interrupt is detected by the CPU Board. A power-fail interrupt generally indicates that the dc outputs of the power supply are fluctuating.

NNNNN bus errors. This indicates that intermittent bus reply timeouts were detected at an unknown address. You can isolate the problem by running individual tests.

NNNNN interrupt errors. This indicates that unanticipated interrupts occurred. Look for a subsequent message indicating the vector at which the interrupts occurred.

RAM-Related Messages

The following messages display information gathered by the RAM test.

RAM error in program space. Restart or press <ESC>. An error occurred in the memory that the diagnostic program occupies. If the diagnostic program is loaded into bad memory, the program may not run properly. Note that since the program itself requires less than 32K words, it is possible to reconfigure memory by changing jumpers. See "Bank Interchange Straps" in Section 3 of this manual.

NNNNN RAM error(s). Some type of RAM error was detected. Error types include configuration errors, parity errors, and data or addressing errors. The following messages should help you isolate the problem.

Memory installed—NNN K words. NNN is the amount of memory (in K words) tested by the program. This can range upward from 64K words to 128K words, depending on the number and type of memory board(s) installed. If less than 64K words of memory is installed, an error will be reported. The program determines how much memory is installed by writing to memory locations above the program until a bus reply timeout is detected. If the diagnostics report less memory than you have installed, recheck the jumpers on the memory board(s) before you suspect a malfunctioning board.

RAM error(s) in range xxxxx to xxxxx, fault mask = NNNNNN. This indicates the address range where RAM errors were detected. The fault mask is a 6-digit octal number in which each non-zero bit represents a mismatch between the data written and the data read inside the given address range.

If only parity errors were detected, the fault mask will be 0 because the program is unable to determine bit faults when a parity interrupt occurs. If necessary, you can disable parity error reporting by moving P7111 on the memory board(s) to position 2, and then rerun the test to isolate the bits at fault. (Restore P7111 before reloading TNIX.) If the errors are in a single bit of the mask, and within a single 16K-word address range (for example, 100000 to 177777), the error is likely to be in or near the corresponding 16K RAM chip. If the range is larger than 16K words (100000 octal) or errors are detected in more than one bit, the problem may be in the support circuitry on the memory board.

If you disable parity and run through the above test and no errors occur, the problem may be in the parity error RAM chips.

Relocate jumpers P5081, P5092, P5101 and P5111 to the positions shown in Fig. 16-3. Rerun the above test with parity disabled to see if the error occurs. If it does, replace the appropriate chips. After testing, make sure you restore all jumpers to their original positions.

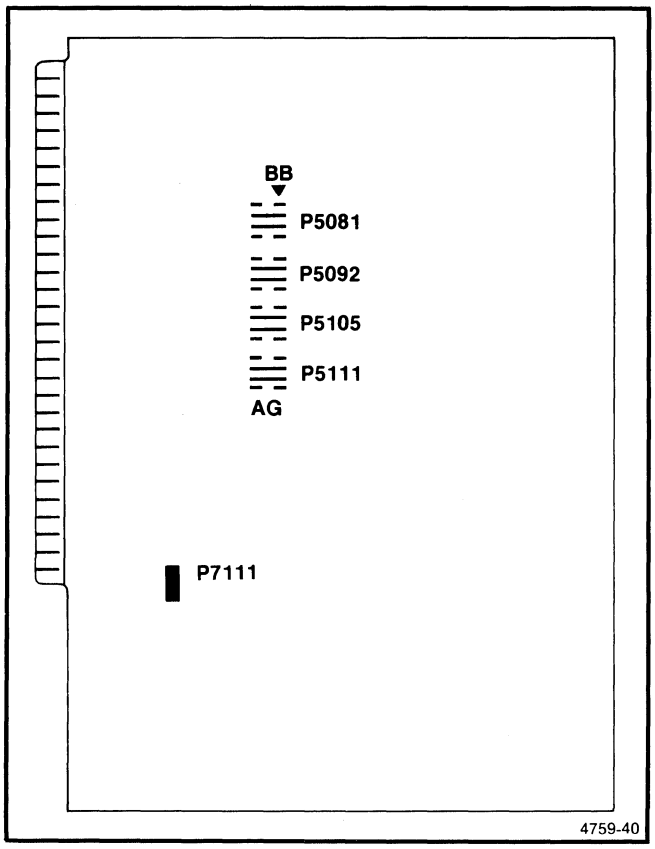

Fig. 16-3. Jumper locations for chip swap.

Patterns in the address range or fault mask may help isolate the problem. For example, errors that only occur within a 16K-word range may indicate a problem with the corresponding 16K-word bank of memory. A fault mask of 177400 or 000377 may indicate a problem in the byte accessing circuits.

NNNNN parity error(s) were detected. This indicates the number of parity interrupts that occurred during testing. If the jumpers on the memory board are set up for normal operation (for running TNIX), almost all memory errors should produce a parity error interrupt. For troubleshooting the memory board, however, you should move the parity enable jumper (P7111 on the memory board) to position 2. This disables hardware error checking and allows the diagnostics to more easily isolate the error.

ROM-Related Messages

The following messages display information gathered by the ROM test.

NNNNN ROM error(s): U50xx. The contents of the Utility Board ROMs, which contain the 8560 bootstrap and power-up diagnostics, don't match their checksums. U50xx indicates which ROM (U5080 or U5090) failed to verify. If replacing the ROMs does not help, check for activity on the ROMs' data and address lines during the ROM test.

Utility Board PROM part numbers: 160-2634-xx, 160-2633-xx. This message indicates which version of bootstrap/diagnostic firmware is installed in your 8560. The first number is the part number of U5080, the second is the part number of U5090. The last two digits of each part number are the version number. If the parts are reversed or identical, your 8560 will not be able to boot automatically.

CPU-related Messages

The following messages display information gathered by the CPU test.

NNNNN processor error(s). The 8560's LSI-11 processor did not pass its instruction set test. The CPU Board is probably at fault. However, this error message may be printed if part of the program memory has been corrupted by a RAM failure or an unauthorized DMA access.

standard processor installed. The LSI-11/23 processor in your 8560 has no options installed. If the diagnostic program displays this message, but your processor has the floating point option, check to be certain the floating point device is properly inserted in the correct socket before rerunning the CPU test.

enhanced processor installed. An LSI-11/73 processor is installed in your 8560.

floating point option installed. The LSI-11/23 processor in your 8560 has the floating point option installed.

bad floating point function. Processor failed floating point instruction set test. Make certain the floating point device is properly inserted in the correct socket. If the floating point device is properly installed, the device itself is probably bad.

LTC-Related Messages

The following messages display information gathered by the LTC test.

NNNNN line-time clock error(s). The Line-Time Clock did not provide interrupts at the correct frequency, as measured by the processor. See the following message for information about the frequency observed by the 8560's processor. Ranges accepted by the test are 48-52 Hz, and 58-62 Hz. Note that if power supply noise (glitches) occurs during the LTC test, you may see a figure of 51 Hz or 61 Hz.

frequency = NN Hz, status: NNNNNN. The frequency provided in this message should be the line frequency of the 8560 power source. If a frequency error occurs at any time during the test, the incorrect frequency will be reported in this message. If the reported frequency is too high, it may be due to power line noise or to a device performing excessive DMA accesses. Either of these conditions effectively slows down the processor speed, which is used as a frequency reference.

NNNNNN represents the contents of the LTC Status Register on the Utility Board. This Status Register normally contains either 000340 (if jumper P1036 on the Utility Board is installed) or 000341 (if P1036 is removed).

missing interrupt. The expected line frequency interrupts did not occur. This may be due to a broken signal path somewhere between the power supply and the Processor Board, or to an unauthorized jumper on the Processor Board.

Line Printer Port-Related Messages

The following messages display information gathered by the LPR test.

lpr n errors. Some type of error was detected on the specified line printer port. The following messages indicate the type of error:

incorrect address strapping. A bus reply timeout was detected when the processor attempted to access the printer port's registers. This is probably due to incorrect jumper configurations on the Utility Board.

xxxxx connected. This message indicates whether a line printer or wrap-back connector (or nothing at all) was connected to the printer port. If the device was later moved to another channel, "later removed" will also be printed. The test uses the CTS and DTR signals to determine which device is connected. The message "nothing connected" means no DTR signal was detected, and "test plug connected" means the DTR and CTS lines were tied together.

```
baud   rcsr   rbuf   xcsr   xbuf
```

xxxxxx xxxxxx xxxxxx xxxxxx xxxxxx. The numbers displayed in this message indicate the status of the printer interface on the Utility Board.

The baud rate that the previously specified printer port is strapped for is "baud". If no error message is printed, the other four status fields can be ignored.

For a detailed explanation of the following registers' contents, refer to "Serial Interface Register Definitions" in Section 5 of this manual.

- "rcsr" displays the contents of the Receiver Control/Status Register. Bits 0, 13, 14, and 15 represent various interface signals. Bit 6 is the interrupt enable bit, and bit 7 is the character received bit.
- "rbuf" displays the contents of the Receiver Data Buffer, which is the logical OR of the characters that caused errors. Bits 13, 14, and 15 are error bits.
- "xcsr" displays the contents of the Transmit Control/Status Register, which indicates the transmitter's control status. Bits 12, 13, 14, and 15 represent the baud rate in use by the interface. Bits 0, 5, and 6 are various control signals. Bit 7 is the transmitter ready bit.
- "xbuf" displays the contents of the Transmit Data Buffer, which is the transmitter's output buffer. The XBUF Register always contains zero unless there is a stuck bit on the data bus.

The RCSR and RBUF Registers are for diagnostic use. The XCSR and XBUF Registers are used by TNIX as well as by the diagnostics.

baud rate not as shipped. This message is intended primarily for factory use. When shipped, line printer ports on the Utility Board are jumpered for 2400 baud. If you have intentionally changed the baud rate jumpering, you may ignore this message.

baud rate errors. One or more baud rates for this printer port did not seem to be correct. Baud rate verification is performed only if a wrap-back connector is connected to the port. Verification is performed by measuring the throughput rate against the line frequency. Anything that interferes with throughput or with the Line-Time Clock may also cause this test to fail. The baud rate at which the test failed is reported in the xcsr display. Note that the baud rate that failed may not be the baud rate that the port is now jumpered for because the test reprograms the baud rate.

output not present—port not fully tested. No output device was detected for this printer port so only minimal testing was performed. In other words, the DTR and/or Transmit Ready (TRDY) signals were not present. DTR is received through the connector on the back panel. TRDY is generated by the UART on the Utility Board.

output interrupt not present—port not fully tested. Although a device was connected to the printer port, the port was unable to correctly generate a transmit interrupt. This may be due either to an incorrectly set jumper on the Utility Board or to a problem with the interrupt request circuit.

LP mode not as shipped. The line printer mode straps on the Utility Board are set incorrectly. TNIX requires that the line printer ports be strapped for line printers.

input not present—port not fully tested. This message is meaningful only if a wrap-back connector is installed. No data was received due to a problem with the receive or transmit lines on the IOA, IOC, or Utility Boards. Make sure the wrap-back connector is installed properly and is wrapping the signals back. This message may also appear if the line printer ports strapping is incorrect.

NNNNN data errors. Receiver errors have probably occurred. If bit 13 in rbuf is set (in a preceding message), a framing error was detected. If bit 14 in the rbuf is set, an overrun occurred (characters were received faster than the program could process them). If neither of these error bits is set, an out-of-sequence character was received.

Other errors in the 8560 may also produce this error message, such as excessive DMA requests or interrupt requests. If receiver errors seem to be the cause of this message, check the UART on the Utility Board.

input interrupt not present—port not fully tested. Although the rcsr indicated that characters were received by the port through the wrap-back connector, no input interrupt occurred. This may be due to a problem with the interrupt request circuit.

IOP-Related Messages

NNNNN IOPx errors. Errors were detected during the IOP test in IOP Board x. The following messages provide more details.

IOPn PROM part numbers: 160-xxxx-xx, 160-xxxx-xx, 160-xxxx-xx. This message indicates which firmware is installed on IOP Board number n. The last two digits of each part number indicate the version number.

HSI I/O n—description. This message describes what the diagnostics have decided is connected to channel n (where n is a number between 0 and 7). If a terminal is connected, the current baud rate will also be shown. If a wrap-back connector is in use, the IOA jumper configuration will be shown. A "nothing connected" message indicates that the IOP test detected no DTR signal for this channel.

If you do not see the description you expect, there are several different steps you can take to find and correct the problem:

- Reseat the IOP Board in its socket.
- Connect your terminal to the channel specified in this message and then run the IOP test to see if characters can be transmitted and received.
- Check to see if the ROM-resident debugging monitor will communicate with this channel. (Refer to Section 13 for information on the debugging mode.)

For further details on how the IOP test determines what device is connected to an HSI I/O channel, refer to the IOP test description earlier in this section.

baud rate did not verify. One of the programmable terminal baud rates did not verify when throughput was checked against the Line-Time Clock. Baud rate verification is performed only if the IOA jumper block is in the terminal position and a wrap-back connector is installed. Anything that interferes with either the IOP throughput or the LTC may also cause this test to fail.

To verify that a baud rate is failing, connect a terminal to the specified channel and restart the IOP test to see if a message is displayed. If a message is displayed but the message is garbled, program the channel for different baud rates by pressing the BREAK key.

missing interrupts. The anticipated interrupts from the IOP Board did not occur within the expected time. This might be due to a throughput problem that prevents the IOP from sending or receiving characters or to a problem with the interrupt logic on the IOP Board.

board does not process commands. The IOP firmware does not respond to commands issued by the system processor, although the Device Register on the IOP Board can be accessed. There are many possible causes for this problem.

To determine if the IOP Board is operational, check to see if the LED on the IOP Board matches any of the displays shown in Fig. 16-4.

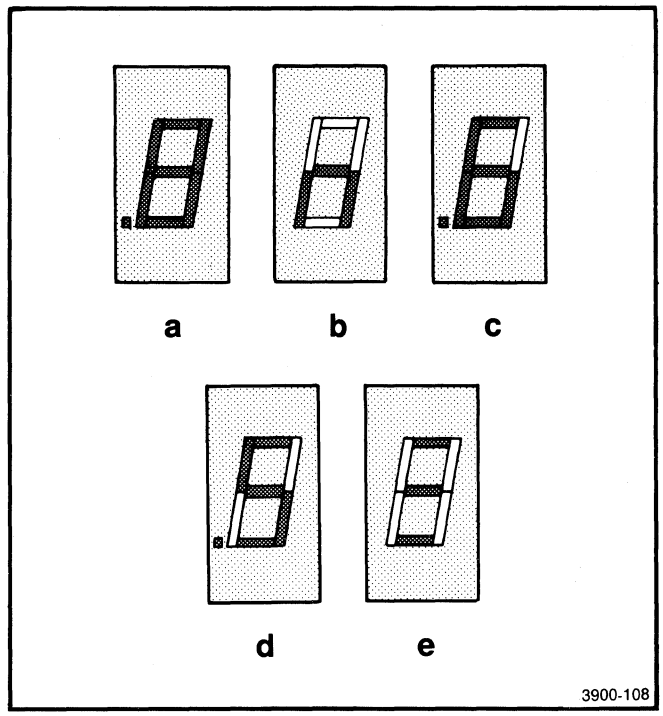

Fig. 16-4. IOP Board seven-segment LED.

The displays shown in Fig. 16-4 indicate the following:

a. The 8088 microprocessor is probably not running at all.

b. The self-test PROM activated normally but could not transfer control to the other two PROMs correctly.

c. The self-test PROM correctly transferred control but the IOP Board is unable to properly communicate with the 8560 bus. This display is used only if the input power line frequency to the 8560 is 60 Hz.

d. The self-test PROM correctly transferred control, but the IOP Board is unable to properly communicate with the 8560 bus. This display is used only if the input power-line frequency to the 8560 is 50 Hz.

e. If the IOP self-test is in progress, the seven-segment LED display shows three horizontal bars.

If the LED displays characters other than those shown in Fig. 16-3, an HSI communication problem may exist with the 8088 operation.

no IOP Boards installed. Bus reply timeouts occurred when the system processor tried to access IOP1 and IOP2. If you have an IOP Board installed, make sure that the jumpers on the board are set properly and the board is firmly seated in the 8560.

IOP aborted command. The IOP Board unexpectedly aborted a command that was sent to the board. Make sure that all of the connectors are firmly attached. Do not change any jumpers while the test is running.

missing DMA write or unexpected interrupt. More interrupts were received than could be accounted for by DMA transfers. (The software expects the number of interrupts and the number of DMA transfers to match.) A DMA write problem may exist with the IOP Board.

transmit timeout. The program tried to transmit something from this channel but was unable to transmit within the expected time period. This may occur if a connector is disconnected. It may also be caused by an intermittent DTR signal.

timeout. The program sent a command to the IOP Board expecting a quick reply, but the response did not occur as expected. This problem may occur if a connector or jumper is changed during the test, or if the IOP Board spends excessive time on some previous command.

invalid character(s) received. The program thought that a wrap-back connector was connected to this channel, but the program received a character that was different than the character it sent. The problem may be on the IOA Board or IOP Board. An IOP addressing error may also be responsible for this message. For example, the IOP Board may have read from or written to the wrong location in system memory.

self-test error, code = NNNNNN. The self-test command issued to the IOP Board did not produce the expected response.

The self-test error code is initially set to 177777 by the diagnostic program. The IOP Board changes this error code to 0 if the self-test reveals no problems and writes a test pattern into memory. If these events do not occur as expected, one of three codes is displayed. IOP error codes and their meanings are as follows:

- 000017—SIO device U4100 failed
- 000360—SIO device U4080 failed
- 000377—both SIO devices failed

Make sure that all IOP Board jumpers are correctly set and the three IOP PROMs are properly installed.

Disk-Related Messages

The following messages display information gathered by the disks test.

Timeout waiting for interrupt. This message appears during the disks test if the MSC did not complete an operation in the expected time period. For additional information, check the messages printed after the tests are complete.

PMS/MSC RAM addressing error. This message appears during the disks test if the MSC does not seem to be using the 8560 RAM buffers set aside for its use. This may be due to a problem with the MSC bus interface.

PMS/MSC overran buffer. Attempting restart. This message appears during the disks test if the MSC exceeded the boundaries of its data buffer in 8560 memory. Since the diagnostic program may have lost control, the program attempts to reinitialize itself after printing this message. The problem may be due to the DMA sequencer on the MSC Board that communicates with the 8560 bus, or to some other problem on the MSC Board.

Writing to unused block(s).... This message is displayed during the first pass of the disks test to reassure the user that the only blocks written to by the test are those not used by TNIX.

When responding to the following error message, typing a "y" and RETURN will erase the inserted flexible disk.

Cannot locate TNIX (fbr) free blocks. OK to erase flex disk? This message is displayed during the disks test if the diagnostics are unable to determine where to write on the flexible disk. Either the disk inserted does not have an fbr directory, the directory is corrupted, or parts of the directory are unreadable. Since the 8560 diagnostic disk has a valid fbr directory on it, this message should not appear unless you have changed disks. If you press RETURN, or "n" and RETURN, the diagnostics program will perform a read-only test on the drive. If you press "y" and RETURN, the diagnostics will assume this is a formatted "scratch" disk, and will write and read to random blocks all over the flexible disk. If you press the ESC key, the test will be aborted, and the program will tell you whether any read errors were detected while reading the directory. The program will also specify the type of read errors.

Disk just became ready. This message will be printed during the the disks test if the corresponding disk drive has changed its "ready" status to ready. For example, if you insert a disk into the flexible disk drive while diagnostics are running, this message will be displayed. After you have started a test pass, don't do anything that might change the ready status.

Disk just became not ready. This message will be printed during the disks test if the corresponding disk drive has changed its "ready" status to not ready. For example, if you open the door of the flexible disk drive while diagnostics are running, this message will be displayed. After you have started a test pass, don't do anything that might change the ready status.

NNNNN recoverable errors. Errors were detected during operations on the previously specified drive, but the MSC Controller automatically retried the operation and the errors were no longer present. Unless the number of recoverable errors is excessive (one or more per test pass), the errors may be ignored. Usually, these errors are due to disk media-related problems. If these errors occurred on a flexible disk, the disk is probably worn from use or the heads are dirty. If these errors occurred on a hard disk, you can use the syschk program under TNIX to make sure that TNIX never accesses the bad blocks. (Unlike TNIX, the diagnostics have access to the bad blocks).

NNNNN disk error(s). Nonrecoverable errors were detected during the disks test. The following messages provide more details:

Controller does not respond at address. A bus reply timeout occurred when the program tried to access the Device Register of the MSC. This may be due to incorrectly placed jumpers on the MSC Board, an incorrectly installed board, or a problem with the bus interface circuit on the MSC Board.

PMS/MSC Board PROM part numbers: 160-2218-xx, 160-2219-xx. This message indicates which version of firmware is installed. The first part number is the low byte of the MSC PROM set; the second part number is the high byte. If the two PROMs are reversed, or if both PROMs are the same, the system will not boot.

NNNNN controller error(s). The MSC does not seem to be functioning properly. Generally, there will be an error code listed several lines below this message indicating the specific symptom. Check the error code before assuming the MSC is faulty.

missing interrupts. The expected interrupts from the MSC Board did not occur. Possible causes include:

- The MSC may be waiting indefinitely for a particular signal to occur.
- The MSC Board may have its jumpers set for stand-alone diagnostics. (Remember that in normal operation, the MSC will usually have a "5" in its LED display while 8560 diagnostics are running.)
- If everything else seems to be normal, the interrupt logic on the MSC Board may be at fault.

flexible disk: description. This message describes which type of disk (if any) is inserted in the drive. This message also reports the density, whether the disk is double-sided, and whether the write-protect notch is covered.

hard disk n not ready. The specified drive did not return a ready status. Make sure all the cables are connected. If the disk has power applied, you will hear a steadily increasing whining noise as the disk comes up to speed after power-on. The problem is more likely caused by the hard disk and its associated circuitry than by the MSC.

hard disk n capacity = NNNNNN blocks. This indicates the capacity of the hard disk. Each block holds 512 bytes of user data.

bad blocks include: NNNNNN NNNNNN. This message indicates which blocks the MSC had trouble reading. The program can report up to 52 different bad blocks. If this message follows the flexible disk message, the errors may be due to worn media or to an unformatted flexible disk. On the hard disk, the blocks may be blocks that TNIX has already recorded in its bad block list. Since the diagnostics do not look at the bad block list, they may be reporting irrelevant information. To make certain TNIX does not use the bad blocks, you may want to run the syschk program supplied with TNIX.

(These should be in TNIX's bad block list. If you're not sure, run syschk). Bad blocks were detected on the hard disk. Since the diagnostics do not use the bad block list, it is possible that the bad blocks reported by the diagnostics are ones that TNIX already knows about. To be safe, you should run syschk.

(Try using a new disk and/or cleaning the heads). Errors that occurred while reading the flexible disk could be due to a worn disk or dirty heads. A head-cleaning procedure is described under "Alignment Aid" in Section 13 of this manual.

error codes include NNNNNN NNNNNN. This message displays up to five octal error codes for each disk drive. Most of these error codes are reported by the MSC Board; however, some special codes are generated by the diagnostic program. In general, if the high bit (bit 15) of the code is a 1, the error was nonrecoverable. If bit 15 is a 0, the error may generally be ignored unless it is frequent (one or more recoverable errors per test pass).

The following error codes are generated by the diagnostic program:

```
177400 - invalid disk size for this drive
177401 - timeout and/or missing interrupt
177402 - MSC is not addressing 8560 RAM
         correctly
177403 - the value written to the MSC
         Board's Device Register is not
         the value being used by the MSC.
177404 - the MSC completed a read operation,
         but did not put anything in the
         8560's data buffer.
177405 - the data read from the disk is not
         the same as the data written to it.
```

The following error codes are returned by the MSC Board firmware during self-test operations:

```
100010 - timeout waiting for response from
         Xebec
100011 - Xebec Board ROM checksum error
100012 - Xebec Board RAM error
100013 - timeout waiting for hard disk to
         become ready
```

In addition to the previous error codes, there are approximately 40 error codes that can be returned by the MSC during normal operation. These error codes are listed under three categories: software interface errors, flexible disk errors, and hard disk errors.

Software interface errors

The following errors should never occur under normal circumstances. If any of these error codes is returned, reload the diagnostic software.

```
102400 - invalid device number
104000 - invalid command code
116400 - QBus timeout error
```

Flexible disk errors

```
010400 - drive not ready
011000 - no track 0 signal
011400 - data overrun error
012000 - CRC error
014400 - missing ID field address mark
015400 - attempt to access sector beyond end
         of track
016000 - invalid cylinder address
017000 - write-protected disk
052000 - block number is too large
```

Hard disk errors

```
020400 - invalid hard disk command
021400 - drive not ready
022400 - illegal head or cylinder address
023000 - sector not found
023400 - data error
025400 - drive fault during write
026400 - DMA timeout during disk read
027400 - DMA timeout during disk write
060400 - no spare sector on track
061400 - hard disk access timeout
062000 - block number is too large
062400 - bad hard disk format
```

GPIB Controller Error Messages

The following messages display information gathered by the GPIB controller test.

NNNNN GPIB Controller errors. Errors were detected during the GPIB Controller test. The following messages provide more details.

Not installed. There is no bus reply when an attempt is made to communicate with the board. The board does not appear to be in the system.

incorrect address strapping. The board is jumpered for its alternate test address, not for normal operation.

primary address out of range: [0-30]. A primary address outside of the valid range was entered. (Primary address 31 is illegal because it is used to send the **UNT** (untalk) command.)

secondary address out of range: [0-31]. A secondary address outside of the valid range was entered.

GPIB Controller PROM part number(s): 160-xxxx-xx. This message indicates what level of firmware is installed on the GPIB Controller Board. The last two digits of the part number indicate the version number.

local RAM size: NN K bytes. This tells how much RAM is accessible on the GPIB Controller Board.

[last] status of device at address PP [, SS]= DD (decimal). The external GPIB device at primary address PP, optional secondary address SS, returned a status byte of DD (decimal) in response to the last serial poll. "last status..." indicates that the selected device replied to a serial poll on at least one pass, but currently the device does not respond.

device at address PP [, SS]does not respond. The external GPIB device at primary address PP, optional secondary address SS, did not respond to the serial poll within the allotted time. Either an invalid address was specified, or a fault condition exists in the external device, the system interconnections, the 8560 rear panel assembly, or the GPIB Controller bus drivers.

board does not process commands. The GPIB Controller firmware does not respond to commands issued by the system processor although the Device Register on the board can be accessed. This can be due to a whole range of problems, including a bad 8088 chip, bad PROMs, and faulty DMA and interrupt logic. Look at the seven-segment LED on the board for clues.

controller error(s). Errors were detected in the GPIB Controller.

DMA error. The GPIB Controller does not seem to be accessing the correct locations in system memory.

interface error(s). No listeners were on the external GPIB during a serial poll. Either the line drivers, the rear panel connector board, the GPIB cable, or the external device is faulty.

possible address error. No device responded to the serial poll. However, one or more devices did complete the transfer of the serial poll command string. This may be caused by an incorrect address or by the absence of the selected device from the bus.

cannot open file: <filename>. The GPIB test file, <filename>, was not found in the directory of the diagnostic disk and could not be opened for read operations.

cannot read file: <filename>. The GPIB test file, <filename>, was located on the disk, but an error occurred during the read operation of the file. The file is probably corrupted.

missing interrupts. The anticipated interrupt from the GPIB controller did not occur as expected. A problem may exist with the interrupt logic, or the GPIB controller's program.

error codes include. The following error codes are returned during the GPIB tests. This list is in approximate reverse order of occurrence and contains the last 10 unique error codes.

NOTE

Several of the following error types use the low byte of the error code to return specific bit errors. In these instances, multi-bit errors are represented by logically ORing the individual bit error codes. For example, error code 101103 indicates system DMA errors of bits 0, 1 and 6. Error code 103300 suggests GPIB control lines DAV and ATN are faulty.

The error codes listed in Table 16-2 are returned by the GPIB Controller firmware during self-test operations.

Table 16-2
GPIB Controller Errors

Error Code	Type of Error	Explanation
101xxx	DMA	Data bit error (xxx = bits in error) 001 = bit 0 002 = bit 1 . . . 200 = bit 7
101401	DMA	Argument error (byte count too large)
101402	DMA	DMA timeout
002007	LTC	Line time clock not running
002010	LTC	Slow clock (freq. < 44 Hz)
002011	LTC	Fast clock (freq. > 66 Hz)
103xxx	GPIB control line	Where xxx = lines in error 001 = REN error 002 = IFC error 004 = SRQ error 010 = EOI error 020 = NRFD error 040 = NDAC error 100 = DAV error 200 = ATN error
104xxx	GPIB data line	Where xxx = bits in error 001 = DIO 1 002 = DIO 2 . . . 200 = DIO 8
104402	GPIB data line	Transfer timeout
104420	GPIB data line line	DAV error
104440	GPIB data line	BO (Byte Out) error
104460	GPIB data line	DAV & BO errors
104500	GPIB data line	Handshake error

Table 16-2 (Cont.)
GPIB Controller Errors

Error Code	Type of Error	Explanation
005xxx	8088 maskable interrupt	Vector bit error (xxx = bits in error) 001 = bit 0 002 = bit 1 . . . 200 = bit 7
005402	8088 maskable interrupt	Interrupt timeout (no interrupt within 100 μs)
005412	8088 maskable interrupt	Early interrupt
005500	8088 maskable interrupt	Handshake error (9914A did not sense error condition)
006001	Local DMA error	Argument error (byte count too large)
006002	Local DMA error	DMA timeout
006003	Local DMA error	Data comparison error
006004	Local DMA error	Terminal count error
000003	RAM size warning	Less than standard RAM available
000002	NOP/Serial poll	Invalid command
177002	NOP/Serial poll	Timeout during transfer of serial poll command string
177005	NOP/Serial poll	No response from selected device
177040	NOP/Serial poll	"Byte Out" error (9914A did not take control)
177100	NOP/Serial poll	Handshake error (no listener on the bus)
177200	NOP/Serial poll	Listen mode error (9914A did not become a listener)

LED Error Message Summary

The disk-based diagnostics also use the five Utility Board LEDs to display error information. (The LED error displays are discussed fully in Section 13 of this manual.) A summary of the error codes is shown in Table 16-3.

Table 16-3
Diagnostic Disk LED Error Codes

LEDs[a]	Octal Value	Definition
_	33	Booting in file from disk
***_*	35	Printing label from disk
*****	37	Program started and issued a reset
-----	00	Program cleared LEDs after starting
----*	01	Initializing RAM variables and interrupt vectors, enabling LTC interrupts and verifying LTC frequency
---*-	02	Program checking which IOP channels have terminals
---**	03	Program checking which line printer ports have terminals
--*--	04	Printing "Press RETURN to select terminal" on all terminals
--*-*	05	Waiting for a terminal to send a return
--**-	06	Reinitializing terminal interfaces and variables
-*-*-	12	Illegal instruction trap; program not executing properly (could not recover)
-*-**	13	Memory management trap; program not executing properly (could not recover)
*----	20	Using terminal connected to HSI I/O 0
---	21	Using terminal connected to HSI I/O 1
---	22	Using terminal connected to HSI I/O 2
*--**	23	Using terminal connected to HSI I/O 3
---	24	Using terminal connected to HSI I/O 4
--*	25	Using terminal connected to HSI I/O 5
*-**-	26	Using terminal connected to HSI I/O 6
*-***	27	Using terminal connected to HSI I/O 7
**---	30	Using terminal connected to LP2

[a] **The dash represents an unlit LED. The asterisk represents a lit LED.**

Section 17
ACCESSORIES

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Standard Accessories 17-1

Optional Accessories 17-1

Section 17

ACCESSORIES

STANDARD ACCESSORIES

The 8560 has the following standard accessories:

- TNIX Operating System 062-5882-xx
- Diagnostic Software 062-5840-xx
- *System Users Manual* 070-3940-xx
- *System Reference Booklet* 070-3942-xx
- Two blank flexible disks
- One power cord (Options A1-A5)
- Shipping restrainer 360-1073-xx
- Shipping restrainer 360-1074-xx
- *8560 Series Hardware Installation Guide* 070-5049-xx
- *8560 Series System Manager's Operation Guide* 070-5050-xx

OPTIONAL ACCESSORIES

The 8560 has the following optional accessories:

- *8560/8561/8562 Service Manual* 070-4759-xx
- *System Reference Manual* 070-3941-xx
- *QumeTrak 242 Maintenance Manual* 070-5080-xx
- *Micropolis 1300 Series Rigid Disk Drive Maintenance Manual* 070-5090-xx
- *Seagate ST406/412/419 Microwinchester Service Manual* 070-5081-xx

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INSTALLATION

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Section 18

INSTALLATION

INTRODUCTION

This section contains information on how to install the 8560 Multi-User Software Development Unit (MUSDU). This section does not describe optional components. Installation procedures for options are given in each option's Installation Manual.

This section contains only minimum operating information. For more information on how to operate the 8560, refer to your System Users Manual.

This section explains the steps involved in unpacking, installing, and preparing the 8560 for operation. The following subjects are covered:

- Site selection and preparation, including space and power requirements
- Unpacking the 8560
- Preparing the 8560 for operation
- Storage and reshipping

SITE SELECTION AND PREPARATION

Figure 18-1 illustrates the 8560 dimensions. The three main considerations for selecting an appropriate work site for an 8560 are space, power requirements and environmental conditions. These considerations are explained further in the following paragraphs.

Space Requirements

Consider the following points when choosing an appropriate work site for your 8560 unit:

1. Adequate ventilation.
2. Room at the rear of the unit for proper cable dress.

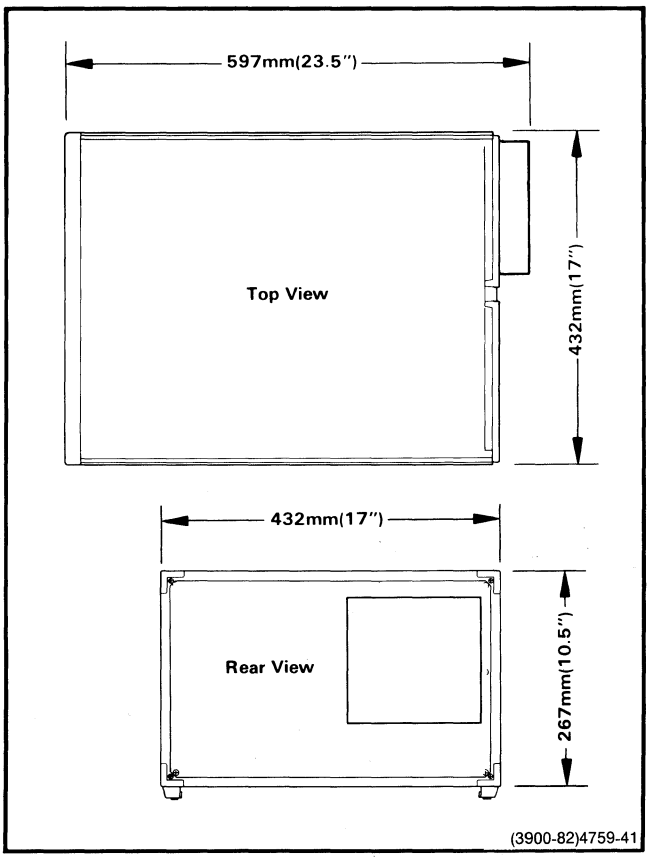

Fig. 18-1. 8560 dimensions.

3. Storage space for manuals and other documents.
4. Space for ongoing hardware development projects.
5. Space for a system terminal and perhaps a line printer.
6. Sufficient space behind and to the sides of the unit to permit removal of the cover and access to the inside of the unit. (Refer to Fig. 18-2 for the required circuit board clearances.)

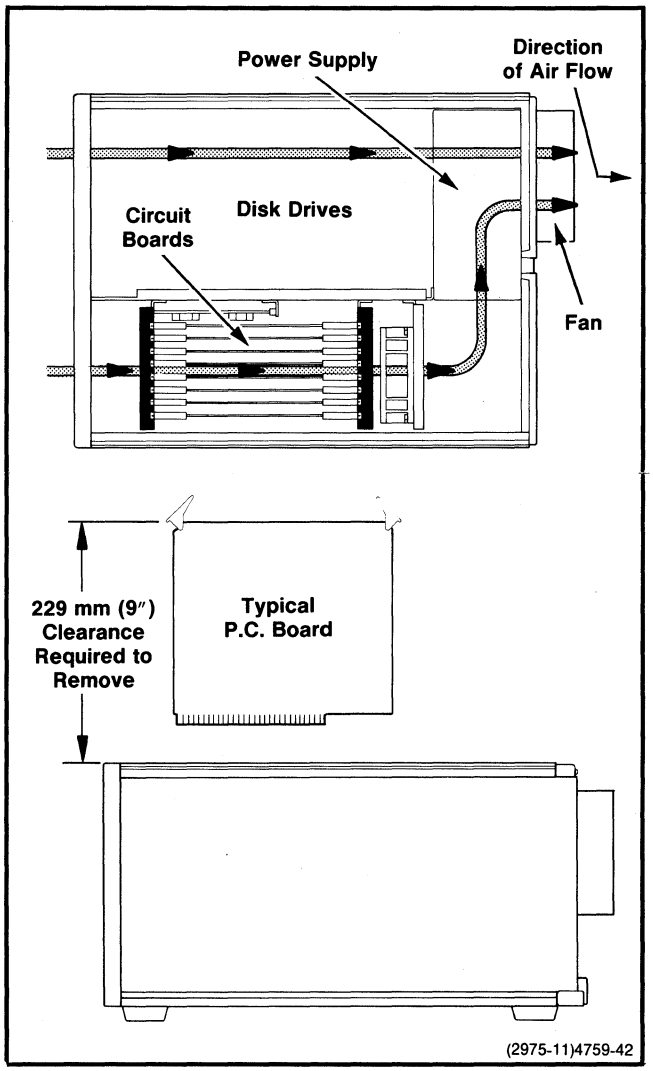

Fig. 18-2. Circuit board clearance requirements.

Power Requirements

The primary power requirements for the 8560 are as follows:

Line Voltages:	115 Vac Nominal (90-132 Vac) or 230 Vac Nominal (180-250 Vac)
Line Frequency	48-66 Hz
Line Current	7.3 Amps (maximum) @115V 3.8 Amps (maximum) @220V
Power Consumption	410 Watts

When preparing a work site for the 8560, observe the following electrical guidelines :

1. All peripheral components at the work station must share common ground and neutral lines to avoid noisy grounds and ground loops.
2. All units must be properly grounded.
3. The work station should be on a separate power breaker switch.

Environmental Considerations

The following considerations should be taken into account when preparing the work site:

- The area selected for the work station should be adequately lit, air-conditioned and dust-free.

CAUTION

Static electricity may damage components of the 8560. Use standard anti-static procedures when setting up the work site.

- The work area should be as static-free as possible. If carpet is used, the carpet must be static-free and treated with anti-static chemicals as often as required.
- The 8560 should be placed on a static-free work surface.
- Allowances must be made for adequate air exhaust at the rear of the unit (6 inches minimum).

UNPACKING THE 8560

Before you unpack the 8560, examine the carton for external damage. If you find any damage:

- Immediately notify the carrier who made delivery and request inspection.
- Contact your nearest Tektronix field engineering office or sales representative.
- Do not throw away the boxes.
- DO NOT TRY TO REPAIR THE INSTRUMENT.

Removing the 8560 From the Carton

The 8560 unit is packed in a heavy-duty cardboard container surrounded by foam packing material. A piece of cardboard covers the top of the unit. The power cord and options rest on the cardboard.

When you open the carton, remove the power cord and any other material that may rest on the cardboard and set them aside. Remove the cardboard and set it aside.

WARNING

Use caution when lifting the 8560 out of the box. The 8560 weighs 22 kg (49 lb). Don't hurt yourself—get some help.

Remove the 8560 and surrounding foam. Set the packing material aside. (Don't lose the packing material—you'll need it again if you ever want to ship or store the instrument).

Removing The Circuit Board Restrainer

Before you can remove any circuit board from the Main Interconnect Board, the circuit board restrainer must be removed. (The restrainer prevents boards from being damaged during shipment.) Note that the aluminum circuit board restrainer covers the circuit boards. Using a Phillips screwdriver, remove the restrainer as shown in Fig. 18-4.

CAUTION

This step involves removing two machine screws from the 8560. Be careful not to drop the screws into the 8560. Severe electrical damage can occur if they are left inside the unit.

Set the screws and nuts aside, and lift out the restrainer. Store the restrainer with the packing material for possible later use. Carefully replace the two screws and two nuts.

Examine the inside of the 8560 for any loose circuit boards, cables or connectors. If you see any damage, follow the procedure given earlier for reporting damage.

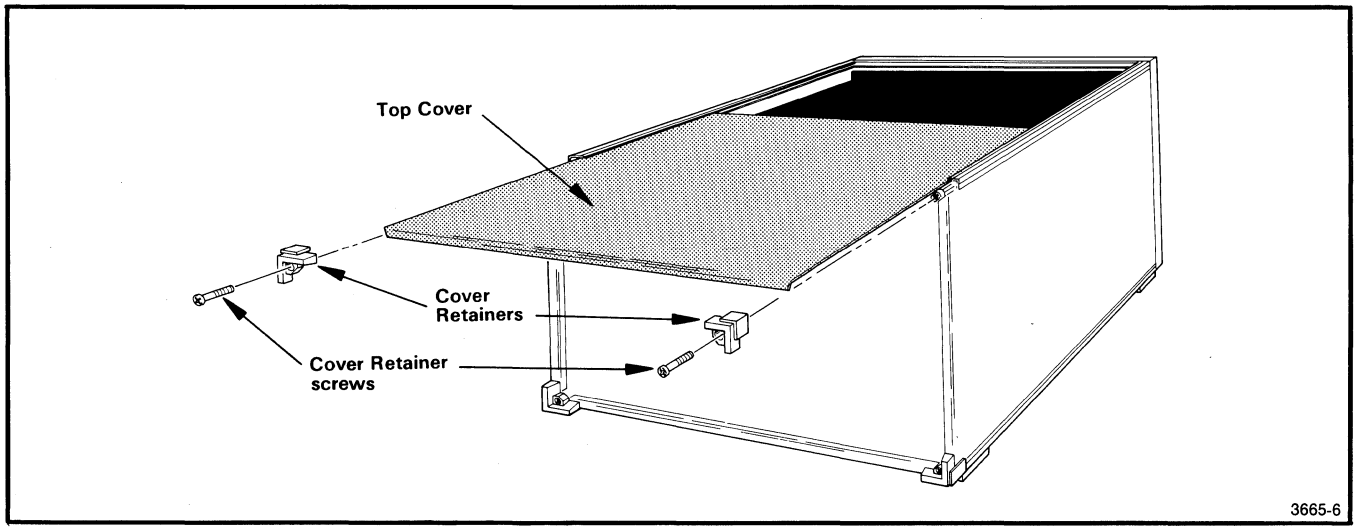

Fig. 18-3. Removing the 8560 top cover.

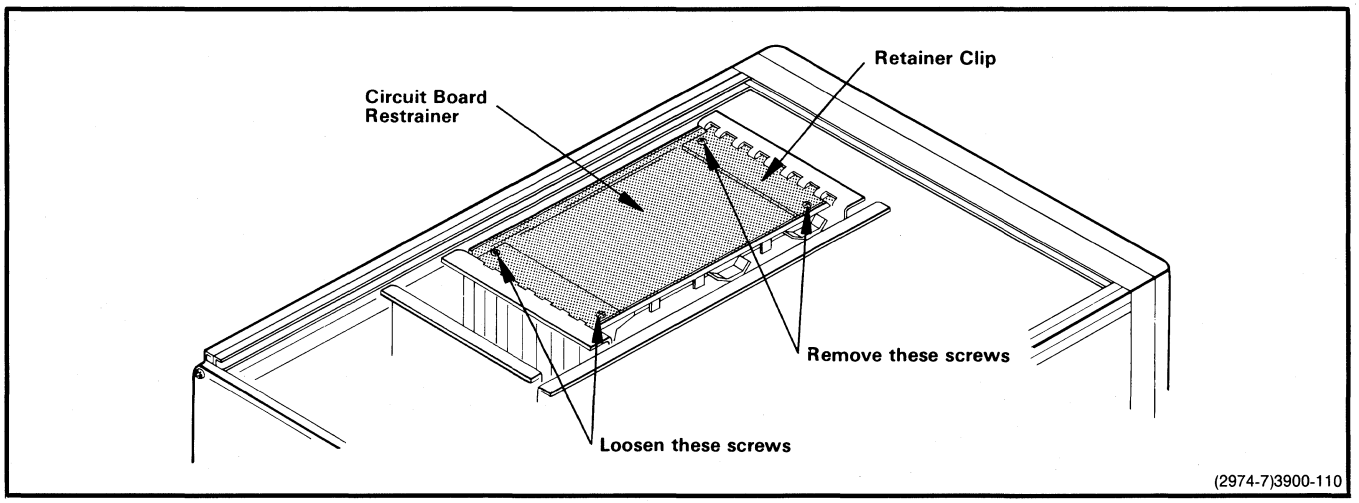

Fig. 18-4. Removing the 8560 circuit board restrainer.

Removing the Flexible Disk Head Restraint

To prevent damage to the read/write heads in the flexible-disk drive assembly, a cardboard head restraint is installed in the disk slot during shipment or storage. Before you operate the 8560, remove this restraint by pulling outward on the cardboard tab that protrudes through the front panel of the flexible-disk drive unit. Store the cardboard head restraint with the other packing materials to use if you store or ship the unit.

Internal Cables

The 8560 has a number of signal and power supply cables. Check that all cables are connected tightly.

Replacing the Covers

Replace the 8560 covers in the following manner:

1. Slide the cover(s) from the rear into the appropriate two grooves located along the instrument's edges.
2. Insert the cover into the grooves until the right-angle flange at its rear edge is flush with the rear panel of the 8560 chassis.
3. Place a cover retainer at each upper rear corner of the 8560, covering the right-angle flange of the top cover.
4. Thread the screws through the cover retainers and tighten them.

PREPARING THE 8560 FOR OPERATION

The 8560 is configured to plug into the primary power source available at your work site. If, for some reason, you need to change power sources, use the following procedure:

1. Refer to Fig. 18-5. Notice the small plate at the lower part of the rear panel. Using a Phillips screw driver, remove the screws holding the plate.
2. The power range selector switch is located under the plate. It selects either 115 or 230 volts.
3. Set the switch to the correct primary power range.

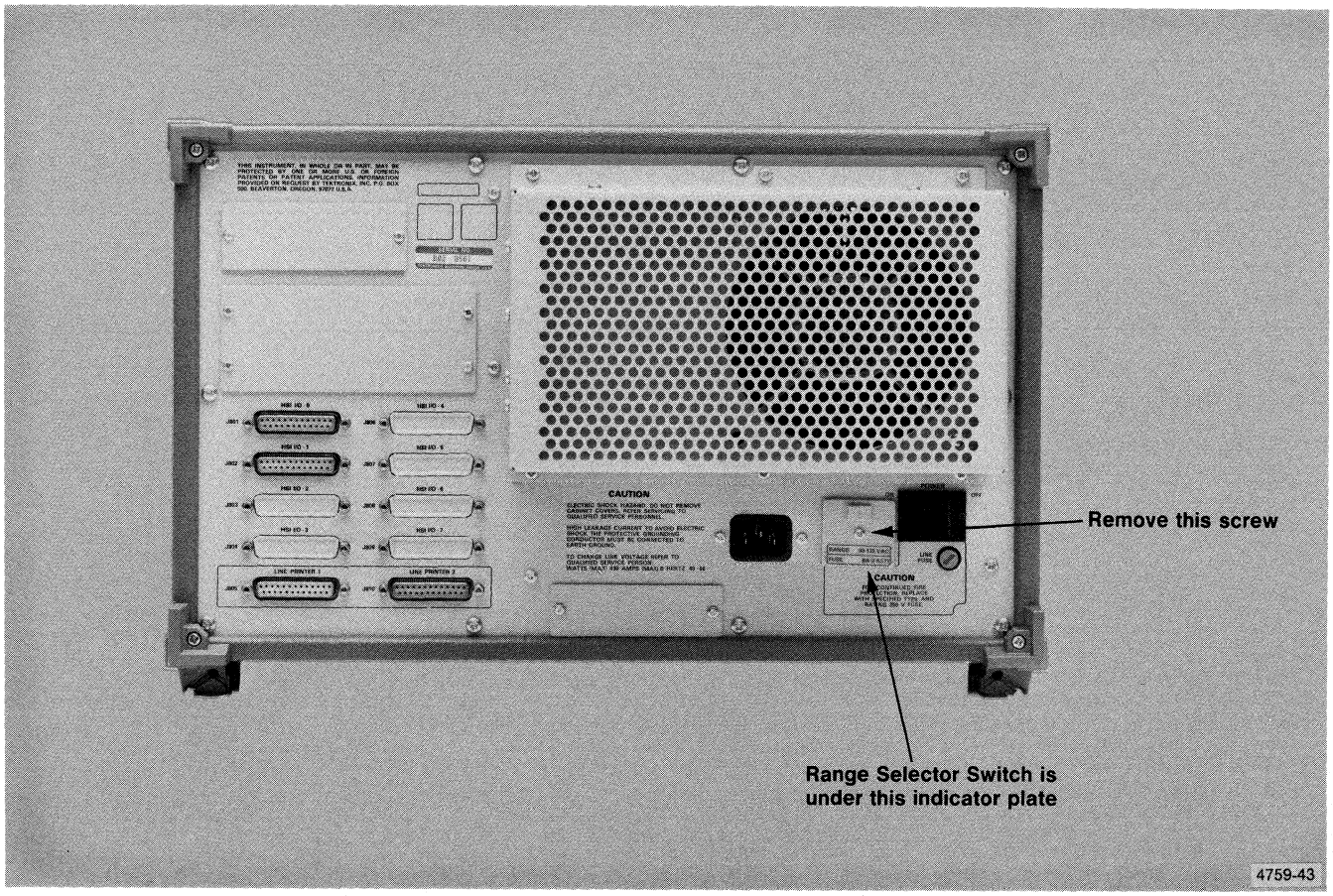

Fig. 18-5. Selecting the primary power voltage.

CAUTION

The fuse rating depends on the voltage selected. For 115 volt operation, use a 3AG, 8 amp, 250 volt, fast-blow (5 sec.) fuse. For 230 volt operation, use a 3AG, 4 Amp, 250 volt, fast-blow (5 sec.) fuse.

4. Install a fuse with the proper rating into the line fuse holder.
5. Replace the switch cover plate.

RACK MOUNT PROCEDURE

If your 8560 includes the rack-mount option, you'll find rack-mount hardware in the bottom of the 8560 shipping carton. The rack-mount slides are already mounted to the sides of the 8560. You must install the slide guides in the equipment rack frame.

Figure 18-6 illustrates the guide orientation. Mount the guides in the rack with the hardware provided. Tighten all screws securely. When the guides are mounted, slide the 8560 into the rack, keeping cable dress in mind.

STORAGE AND RESHIPPING

To repack the 8560, simply follow the unpacking instructions in reverse order. In addition, consider the following information when storing or reshipping the 8560.

Storage

Observe the following considerations whenever you place the 8560 in storage:

- Provide adequate protection from dust.
- Do not exceed the humidity or temperature limitations of the instrument outlined in Section 2 of this manual.
- Store the carton upright. Do not compress the carton or stack heavy objects upon it.

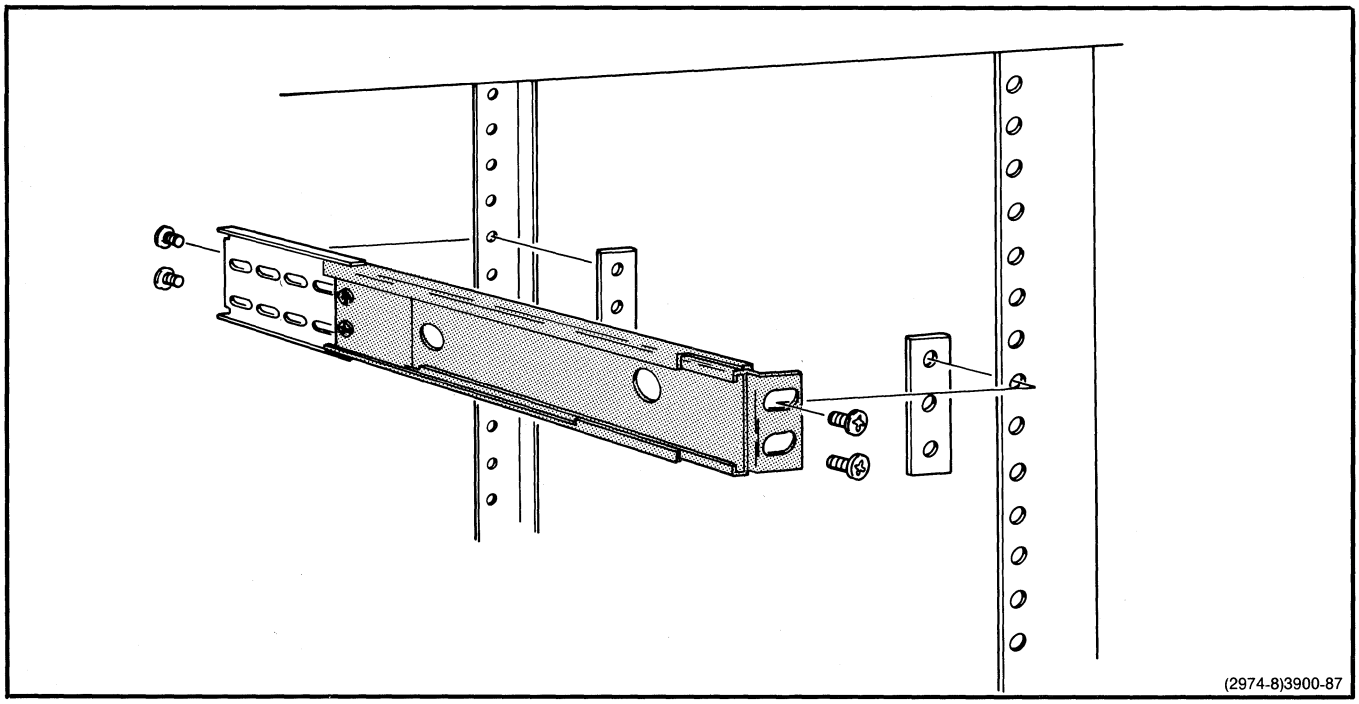

Fig. 18-6. Rack-mount guide orientation.

Reshipping

If the unit must be shipped to the factory or service center, the following steps should be taken:

1. Note the serial number on the back panel of the unit and any other relevant numbers or symbols required for identification. Include these numbers when you correspond with Tektronix about any possible problems concerning your 8560 unit.
2. Replace the cardboard head restraint in the flexible disk drive slot.
3. Wrap the unit in durable waterproof material, such as heavy polyethylene, and tape securely. This step should be carried out only in a dry atmosphere, and with the unit cool to the touch.
4. Pack the unit in a sturdy box (heavy cardboard is acceptable for land shipments) lined with 76 mm (3 inches) of medium-density foam or expanded polystyrene.
5. Wrap cables, adapters, and other accessories separately and tape them to the inner liner at a break in the foam or to a separate platform mounted above the foam or polystyrene. In the latter case, a sheet of 25 mm (1 inch) minimum thick foam should be taped above the cable package.
6. Seal the carton with reinforced packaging tape and identify the sender, the unit number, and the serial number on the outside of the carton.
7. Notify the factory or your sales representative of your intent to ship the unit and await their acknowledgement before shipping.

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REFERENCE MATERIAL

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Section 19

REFERENCE MATERIAL

INTRODUCTION

This section describes Main Interconnect Board connector wiring so you may easily relate pins and signal names for each system board. In addition, this section describes the 8560 bus signals and their functions.

BACK PLANE CONNECTOR CONFIGURATIONS

Figures 19-1 through 19-6 show eight Main Interconnect Board connector configurations. As shown, each figure repeats all LSI-11 lines, thus relating the 100-line 8560 bus to the 72-line DEC Q-bus.

Since a connector configuration depends on the type of board the connector serves, each connector configuration is different. Connectors for board pairs, however, are identical. Connectors for Memory Boards 1 and 2 are wired identically, as are the connectors for IOP Boards 1 and 2.

The following pages show the Main Interconnect Board connector configurations for these connectors:

- J3/J4—LSI-11 Processor (Fig. 19-1)
- J6—MSC Board (Fig. 19-2)
- J8—System Memory Board 2 (Fig. 19-3)
- J9—System Memory Board 1 (Fig. 19-3)
- J10—GPIB Option (Fig. 19-4)
- J11—I/O Processor Board 2 (Fig. 19-5)
- J12—I/O Processor Board 1 (Fig. 19-5)
- J13—Utility Board (Fig. 19-6)

J3/J4 LSI-11 Processor

COMPONENT SIDE			BACK SIDE		
	2			1	
	4			3	
	6			5	
	8			7	
	10			9	
	12			11	
	14			13	
8560 Bus	16		8560 Bus	15	
	18			17	
	20			19	
BIRQ5 L	22		+5V	21	
BIRQ6 L	24		-12V	23	
BDAL 16 L	26		GND	25	
BDAL 17 L	28		+12V	27	
SSPARE 1	30		BDOUT L	29	
SSPARE 2	32		BRPLY L	31	
SSPARE 3	34		BDIN L	33	
GND	36		BSYNC L	35	
MSPARE A	38		BWTBT L	37	
MSPARE A	40		BIRQ L	39	
GND	42		BIAKI L	41	
BDMR L	44		BIAKO L	43	
BHALT L	46		BB57 L	45	
BREF L	48		BDM61 L	47	
+12 B	50		BDM60 L	49	
GND	52		BINIT L	51	
PSPARE 1	54		BDAL0 L	53	
+5 B	56		BDAL1 L	55	
	58			57	
	60			59	
	62			61	
	64			63	
BDCOK H	66		+5V	65	
BPOK H	68		-12V	67	
BDAL 18 L	70		GND	69	
BDAL 19 L	72		+12V	71	
BDAL 20 L	74		BDAL2 L	73	
BDAL 21 L	76		BDAL3 L	75	
SSPARE 8	78		BDAL4 L	77	
GND	80		BDAL5 L	79	
MSPARE B	82		BDAL6 L	81	
MSPARE B	84		BDAL7 L	83	
GND	86		BDAL8 L	85	
BSACK L	88		BDAL9 L	87	
BIRQ7 L	90		BDAL10 L	89	
BEVNT L	92		BDAL11 L	91	
+12 B	94		BDAL12 L	93	
GND	96		BDAL13 L	95	
PSPARE 2	98		BDAL14 L	97	
+5V	100		BDAL15 L	99	

3900-88

Fig. 19-1. J3/J4 LSI-11 Processor.

J6 MSC Board

8560 Bus		COMPONENT SIDE		BACK SIDE	8560 Bus
		2	DRIVE SELECT4 L	1	DRIVE SELECT3 L
		4	DIRECTION L	3	DRIVE SELECT2 L
		6	STEP L	5	DRIVE SELECT1 L
		8	WRITE DATA L	7	*
		10	WRITE DATA L	9	READY L
		12	TRACK 00 L	11	MUDEX L
		14	WRITE PROTECT L	13	HEROLOAD L
		16	REA DATA L	15	*
		18	*	17	SIDE SELECT L
		20	*	19	DISK CHANGE L
BIRQ5 L	22			+5V	21
BIRQ6 L	24			-12V	23
BDAL 16 L	26			GND	25
BDAL 17 L	28			+12V	27
SSPARE 1	30			BDOUT L	29
SSPARE 2	32			BRPLY L	31
SSPARE 3	34			BDIN L	33
GND	36			BSYNC L	35
MSPARE A	38			BWTBT L	37
MSPARE A	40			BIRQ L	39
GND	42			BIAKI L	41
BDMR L	44			BIAKO L	43
BHALT L	46			BB57 L	45
BREF L	48			BDM6I L	47
+12 B	50			BDM60 L	49
GND	52			BINIT L	51
PSPARE 1	54			BDAL0 L	53
+5 B	56			BDAL1 L	55
	58	NOT USED		57	TWO SIDED L
	60	NOT USED		59	*
	62	W/WRWRL		61	*
	64	RD FLTRSW/WRWR L		63	NOT USED
BDCOK H	66			+5V	65
BPOK H	68			-12V	67
BDAL 18 L	70			GND	69
BDAL 19 L	72			+12V	71
BDAL 20 L	74			BDAL2 L	73
BDAL 21 L	76			BDAL3 L	75
SSPARE 8	78			BDAL4 L	77
GND	80			BDAL5 L	79
MSPARE B	82			BDAL6 L	81
MSPARE B	84			BDAL7 L	83
GND	86			BDAL8 L	85
BSACK L	88			BDAL9 L	87
BIRQ7 L	90			BDAL10 L	89
BEVNT L	92			BDAL11 L	91
+12 B	94			BDAL12 L	93
GND	96			BDAL13 L	95
PSPARE 2	98			BDAL14 L	97
+5V	100			BDAL15 L	99

* CONNECTED BUT NOT USED

3900-89

Fig. 19-2. J6 MSC Board.

J8 and J9 System Memory Boards 2 and 1

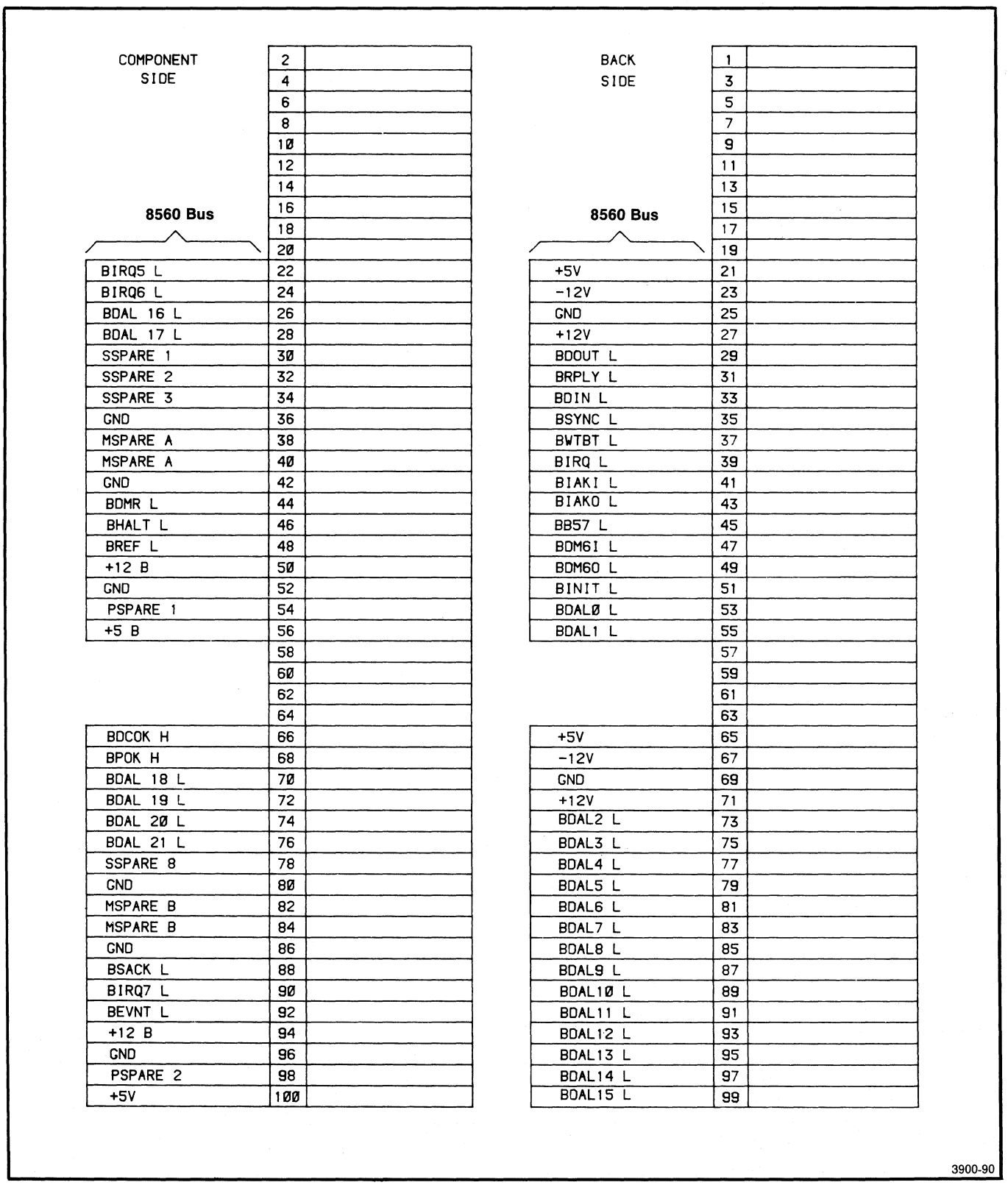

Fig. 19-3. J8 and J9 System Memory Boards 2 and 1.

J10 GPIB Option

COMPONENT SIDE			BACK SIDE		
	2	*		1	*
	4	*		3	*
	6	*		5	*
	8	*		7	*
	10	*		9	*
	12	*		11	*
	14	*		13	*
	16	*		15	*
	18	*		17	*
	20	*		19	*
BIRQ5 L	22		+5V	21	
BIRQ6 L	24		-12V	23	
BDAL 16 L	26		GND	25	
BDAL 17 L	28		+12V	27	
SSPARE 1	30		BDOUT L	29	
SSPARE 2	32		BRPLY L	31	
SSPARE 3	34		BDIN L	33	
GND	36		BSYNC L	35	
MSPARE A	38		BWTBT L	37	
MSPARE A	40		BIRQ L	39	
GND	42		BIAKI L	41	
BDMR L	44		BIAKO L	43	
BHALT L	46		BB57 L	45	
BREF L	48		BDM6I L	47	
+12 B	50		BDM6O L	49	
GND	52		BINIT L	51	
PSPARE 1	54		BDAL0 L	53	
+5 B	56		BDAL1 L	55	
	58	*		57	*
	60	*		59	*
	62	*		61	*
	64	*		63	*
BDCOK H	66		+5V	65	
BPOK H	68		-12V	67	
BDAL 18 L	70		GND	69	
BDAL 19 L	72		+12V	71	
BDAL 20 L	74		BDAL2 L	73	
BDAL 21 L	76		BDAL3 L	75	
SSPARE 8	78		BDAL4 L	77	
GND	80		BDAL5 L	79	
MSPARE B	82		BDAL6 L	81	
MSPARE B	84		BDAL7 L	83	
GND	86		BDAL8 L	85	
BSACK L	88		BDAL9 L	87	
BIRQ7 L	90		BDAL10 L	89	
BEVNT L	92		BDAL11 L	91	
+12 B	94		BDAL12 L	93	
GND	96		BDAL13 L	95	
PSPARE 2	98		BDAL14 L	97	
+5V	100		BDAL15 L	99	

8560 Bus

8560 Bus

* CONNECTED, BUT NOT USED

3900-91

Fig. 19-4. J10 GPIB option.

J11 and J12 I/P Processor Boards 2 and 1

COMPONENT SIDE				BACK SIDE	
	2	CLK		1	CTS-Ø L
	4	DTR-0 L		3	SEROUT-Ø L
	6	SERIN-Ø L		5	HSI-Ø L
	8	2SA-Ø H		7	CTS-1 L
	10	CTS-3 L		9	SEROUT-1 L
	12	SEROUT L		11	DTR-1 L
	14	DTR-3 L		13	HSI-1 L
	16	HSI-3 L		15	SERIN-1 L
	18	SERIN-3 L		17	CTS-2 L
8560 Bus	20	LINE PR	8560 Bus	19	SEROUT-2 L
BIRQ5 L	22		+5V	21	
BIRQ6 L	24		-12V	23	
BDAL 16 L	26		GND	25	
BDAL 17 L	28		+12V	27	
SSPARE 1	30		BDOUT L	29	
SSPARE 2	32		BRPLY L	31	
SSPARE 3	34		BDIN L	33	
GND	36		BSYNC L	35	
MSPARE A	38		BWTBT L	37	
MSPARE A	40		BIRQ L	39	
GND	42		BIAKI L	41	
BDMR L	44		BIAKO L	43	
BHALT L	46		BB57 L	45	
BREF L	48		BDM6I L	47	
+12 B	50		BDM60 L	49	
GND	52		BINIT L	51	
PSPARE 1	54		BDALØ L	53	
+5 B	56		BDAL1 L	55	
	58	NOT USED		57	NOT USED
	60	NOT USED		59	DTR-2 L
	62	NOT USED		61	HSI-2 L
	64	NOT USED		63	SERIN-2 L
BDCOK H	66		+5V	65	
BPOK H	68		-12V	67	
BDAL 18 L	70		GND	69	
BDAL 19 L	72		+12V	71	
BDAL 20 L	74		BDAL2 L	73	
BDAL 21 L	76		BDAL3 L	75	
SSPARE 8	78		BDAL4 L	77	
GND	80		BDAL5 L	79	
MSPARE B	82		BDAL6 L	81	
MSPARE B	84		BDAL7 L	83	
GND	86		BDAL8 L	85	
BSACK L	88		BDAL9 L	87	
BIRQ7 L	90		BDAL10 L	89	
BEVNT L	92		BDAL11 L	91	
+12 B	94		BDAL12 L	93	
GND	96		BDAL13 L	95	
PSPARE 2	98		BDAL14 L	97	
+5V	100		BDAL15 L	99	

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Fig. 19-5. J11 and J12 I/O Processor 2 and 1.

J13 Utility Board

	COMPONENT SIDE	2	POWER	L	BACK SIDE	1	OCON	L
		4	DTR2	L		3	DTRI	L
		6	EXTCLKQ	L		5	EXTCLK	
		8	SEROUT2	L		7	SERIN	
		10	SERIN2	L		9	SEROUT	
		12	RTS 2	L		11	RST1	L
		14	CTS 2	L		13	CTS1	L
	8560 Bus	16	NOT USED		8560 Bus	15	NOT USED	
		18	NOT USED			17	NOT USED	
		20	ACOK	H		19		
BIRQ5 L		22			+5V	21		
BIRQ6 L		24			-12V	23		
BDAL 16 L		26			GND	25		
BDAL 17 L		28			+12V	27		
SSPARE 1		30			BDOUT L	29		
SSPARE 2		32			BRPLY L	31		
SSPARE 3		34			BDIN L	33		
GND		36			BSYNC L	35		
MSPARE A		38			BWTBT L	37		
MSPARE A		40			BIRQ L	39		
GND		42			BIAKI L	41		
BDMR L		44			BIAKO L	43		
BHALT L		46			BB57 L	45		
BREF L		48			BDM6I L	47		
+12 B		50			BDM6O L	49		
GND		52			BINIT L	51		
PSPARE 1		54			BDAL0 L	53		
+5 B		56			BDAL1 L	55		
		58	RUN/HALT	L		57	HSFE	L
		60	RESTART	L		59	NOT USED	
		62	PROCBUSY	L		61	NOT USED	
		64	NOT USED			63	NOT USED	
BDCOK H		66			+5V	65		
BPOK H		68			-12V	67		
BDAL 18 L		70			GND	69		
BDAL 19 L		72			+12V	71		
BDAL 20 L		74			BDAL2 L	73		
BDAL 21 L		76			BDAL3 L	75		
SSPARE 8		78			BDAL4 L	77		
GND		80			BDAL5 L	79		
MSPARE B		82			BDAL6 L	81		
MSPARE B		84			BDAL7 L	83		
GND		86			BDAL8 L	85		
BSACK L		88			BDAL9 L	87		
BIRQ7 L		90			BDAL10 L	89		
BEVNT L		92			BDAL11 L	91		
+12 B		94			BDAL12 L	93		
GND		96			BDAL13 L	95		
PSPARE 2		98			BDAL14 L	97		
+5V		100			BDAL15 L	99		

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Fig. 19-6. J13 Utility Board.

8560 BUS SIGNALS

Table 19-1 describes the 8560 bus signals.

Table 19-1
8560 Bus Signal Descriptions

Mnemonic	Description
BSPARE1 BSPARE2	Bus Spare—(Not assigned. Reserved for DEC use.)
BADL16 BADL17	Extended address bits
GND	Ground—System signal ground and dc return.
BDMR(L)	Direct Memory Access (DMA) Request—A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC(L) is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO(L). The device responds by negating BDMR(L) and asserting BSACK(L).
BHALT(L)	Processor Halt—When BHALT(L) is asserted, the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the processor module is removed) and DMA request/grant sequences are enabled. When in the HALT state, the processor executes the ODT microcode and the console device operation is invoked.
BREF(L)	Memory Refresh—Asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC(L)/BDIN(L) bus transaction.
BDCOK(H)	DC Power OK—Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BPOK(H)	Power OK—Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BSACK(L)	This signal is asserted by a DMA device in response to the processor's BDMGO(L) signal, indicating that the DMA device is bus master.
BSPARE6	Bus Spare—(Not assigned. Reserved for DEC use.)
BEVNT(L)	External Event Interrupt Request—When the processor is asserted, the processor responds (if PS bit 7 is 00) by entering a service routine through vector address 100 (octal). A typical use of this is a line time clock interrupt.
PSPARE4	Spare—Not assigned.
PSPARE2	Spare—Not assigned.
+5 +5 -12	+5 V Power—Normal +5 Vdc system power. +5 V Power—Normal +5 Vdc system power. -12 V Power—-12 Vdc power for devices requiring this voltage.
+12	+12 V Power—+12 Vdc system power.
BDOUT(L)	Data Output—BDOUT, when asserted, implies that valid data is available on BDALO-15(L) and that an output transfer, with respect to the bus master device, is taking place. The BDOUT(L) signal must assert BRPLY(L) to complete the transfer.

Table 19-1 (Cont.)
8560 Bus Signal Descriptions

Mnemonic	Description
BRPLY(L)	Reply—BRPLY is asserted in response to BDIN(L) or BDOUT(L) and during an IAK transaction. BRPLY(L) is generated by a slave device to indicate that its data is on the BDAL bus or that it has accepted output data from the bus.
BDIN(L)	Data Input—BDIN(L) is used for two types of bus operation: 1. When asserted during BSYNC(L) time, BDIN(L) implies an input transfer with respect to the current bus master, and requires a response (BRPLY(L)). BDIN(L) is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC, BDIN(L) indicates that an interrupt operation is occurring.
BSYNC(L)	Synchronize—BSYNC(L) is asserted by the bus master to indicate that it has placed an address on BDAL0-15. The transfer is in process until BSYNC(L) is negated.
BWTBT(L)	Write/BWTBT(L) is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC(L) to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT(L), in a DATOB bus cycle, for byte addressing.
BIRQ(L)	Interrupt Request—A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the processor's PS word bit 7 is 0, the processor acknowledges the request by asserting BDIN(L) and BIAKO(L).
BIAKI(L), BIAKO(L)	Interrupt Acknowledge Input and Interrupt Acknowledge Output—This is an interrupt acknowledge signal generated by the processor in response to an interrupt request (BIRQ(L)). The processor asserts BIAKO(L), which is routed to the BIAKI(L) pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO(L). If it is not asserting BIRQ(L), the device will pass BIAKI(L) to the next (lower priority) device through its BIAKO(L) pin and the lower priority device's BIAKI(L) pin.
BBS7(L)	Bank 7 Select—The bus master asserts BBS7(L) when an address in the upper 4K bank (address in the 28-32K range) is placed on the bus. BSYNC(L) is then asserted and BBS7(L) remains active for the duration of the addressing portion of the bus cycle.
BDMGI(L), BDMGO(L)	DMA Grant input and DMA Grant Output—This is the processor-generated, daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO(L), which is routed to the BDMGI(L) pin of the first device on the bus. If the processor requests the bus, it will inhibit passing BDMGO(L). If it is not requesting the bus, it will pass the BDMGI(L) signal to the next (lower priority) device via its BDMGO(L) pin. The device asserting BDMR(L) is the device requesting the bus, and it responds to the BDMGI(L) signal by negating BDMR, asserting BSACK(L), assuming bus mastership, and executing the required bus cycle.
BINIT(L)	Initialize—BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK(H)).
BDALO(L) BDALI(L)	Data/Address Lines—These two lines are part of the 16-line data/address bus over which address and data information are placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to, the addressed lines.
+5 -12 +12	+5 V Power—Normal +5 Vdc system power. -12 V Power— -12 Vdc power for devices requiring this voltage. +12 V Power— +12 Vdc system power.

Table 19-1 (Cont.)
8560 Bus Signal Descriptions

Mnemonic	Description
BDAL2(L) BDAL3(L) BDAL4(L) BDAL5(L) BDAL6(L) BDAL7(L) BDAL8(L) BDAL9(L) BDAL10(L) BDAL11(L) BDAL12(L) BDAL13(L) BDAL14(L) BDAL15(L)	Data Address Lines.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

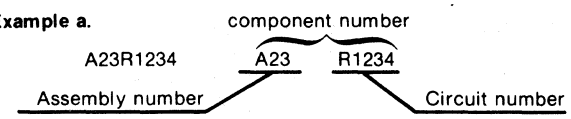
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

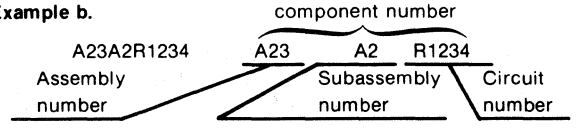
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000FG	RIFA WORLD PRODUCTS INC.	7625 BUSH LAKE RD P.O. BOX 35263	MINNEAPOLIS, MN 55435
000FJ	MARCOM SWITCHES INC.	67 ALBANY STREET	CAZENOVIA, N.Y. 13035
000GU	SUPERTEX INC.	1225 BORDEAUX DRIVE	SUNNYVALE, CA 94086
000JR	MUSASHA WORKS OF HITACHI LTD	1450 JOSUIHON-CHO	KODAIRA-SHI, TOKYO, JAPAN
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P.O. BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01281	TRW ELECTRONIC COMPONENTS, SEMICONDUCTOR OPERATIONS	14520 AVIATION BLVD.	LAWNDALE, CA 90260
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
01807	PETERSEN RADIO COMPANY, INC.	2800 WEST BROADWAY	COUNCIL BLUFFS, IN 51501
02111	SPECTROL ELECTRONICS CORPORATION	17070 EAST GALE AVENUE	CITY OF INDUSTRY, CA 91745
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
05828	GENERAL INSTRUMENT CORP ELECTRONIC SYSTEMS DIV.	600 W JOHN ST.	HICKSVILLE LI, NY 11802
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
12954	SIEMENS CORPORATION, COMPONENTS GROUP	8700 E THOMAS RD, P O BOX 1390	SCOTTSDALE, AZ 85252
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
15476	DIGITAL EQUIPMENT CORP.	146 MAIN ST.	MAYNARD, MA 01754
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50157	MIDWEST COMPONENTS INC.	P. O. BOX 787 1981 PORT CITY BLVD.	MUSKEGON, MI 49443
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
54563	SANIVOID CO.	881 S GRAND AVE.	PASADENA, CA 91105
55112	PLESSEY CAPACITORS, DIV. OF PLESSEY INC.	5334 STERLING CENTER DR.	WEST LAKE VILLAGE, CA 91361
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
56708	ZILOG INC.	14060 BUBB RD.	CUPERTINO, CA 95014
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
57924	BOURNS INC NETWORKS DIV 12155	MAGNOLIA AVE	RIVERSIDE, CA 92503
58361	GENERAL INSTRUMENT CORP. OPTO ELECTRONICS DIV.	3400 HILLVIEW AVE	PALO ALTO, CA 94304
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
63743	WARD LEONARD ELECTRIC CO., INC.	31 SOUTH ST.	MOUNT VERNON, NY 10550
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
72619	DIALIGHT, DIV. AMPEREX ELECTRONIC	203 HARRISON PLACE	BROOKLYN, NY 11237
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
74276	SIGNALITE DIV., GENERAL INSTRUMENT CORP.	1933 HECK AVE.	NEPTUNE, NJ 07753
75037	MINNESOTA MINING & MFG CO. ELECTRO PRODUCTS DIV.	3M CENTER	ST. PAUL, MN 55101

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80031	ELECTRA-MIDLAND CORP., MEPCO DIV.	22 COLUMBIA ROAD	MORRISTOWN, NJ 07960
81483	INTERNATIONAL RECTIFIER CORP.	9220 SUNSET BLVD.	LOS ANGELES, CA 90069
82389	SWITCHCRAFT, INC.	5555 N. ELSTON AVE.	CHICAGO, IL 60630
84411	TRW ELECTRONIC COMPONENTS, TRW CAPACITORS	112 W. FIRST ST.	OGALLALA, NE 69153
87034	ILLUMINATED PRODUCTS INC., A SUB OF OAK INDUSTRIES, INC.	2620 SUSAN ST, PO BOX 11930	SANTA ANA, CA 92711
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
95121	QUALITY COMPONENTS, INC.	P O BOX 113	ST. MARYS, PA 15857
95238	CONTINENTAL CONNECTOR CORP.	34-63 56TH ST.	WOODSIDE, NY 11377
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
D5243	ROEDERSTEIN E SPEZIALFABRIK FUER KONDENSTATOREN GMBN	LUDMILLA STRASSE 23-25	8300 LANDSHUT, GERMANY
T0510	PANASONIC COMPANY DIVISION OF MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY	SECAUCUS, NJ 07094
T0946	SAN-O INDUSTRIAL CORP.	170 WILBUR PL	BAHEMIA, LONG ISLAND,NY 1171

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-7208-00			CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-7208-00
A15	119-1447-00			MODULE:PROCESSOR LSI 11/23	54563	5013326-00
A15	----- -----			(8560 & 8561 ONLY)		
A15	119-1793-00			CKT BOARD ASSY:KDJ11-A PROCESSOR	15476	KDJ11-A
A15	----- -----			(8560 OPT 10/F10 & 8561 OPT 10 & 8562 ONLY		
A15	----- -----			REPLACEABLE AS A UNIT ONLY)		
A20	670-8495-00			CKT BOARD ASSY:UTILITY	80009	670-8495-00
A30	670-7330-02			CKT BOARD ASSY:I/O PROCESSOR	80009	670-7330-00
A30	----- -----			(8560 & 8561 QTY 1,8562 QTY 2)		
A35	670-7308-00			CKT BOARD ASSY:I.O ADAPTER	80009	670-7308-00
A40	670-7306-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-7306-00
A40	----- -----			(8560 & 8561 OPT 08 ONLY)		
A40	670-8162-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-8162-00
A40	----- -----			(8561 & 8561 OPT 08 ONLY)		
A40	670-7307-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-7307-00
A40	----- -----			(8562 ONLY)		
A45	670-1277-00			CKT BOARD ASSY:MASS STORAGE CONTROLLER	80009	670-1277-00
A60	670-8245-00			CKT BOARD ASSY:PS INTERCONNECT	80009	670-8245-00
A62	670-3184-00			CKT BOARD ASSY:INVERTER	80009	670-3184-00
A64	670-3163-00			CKT BOARD ASSY:REGULATOR	80009	670-3163-00
A66	670-3057-00			CKT BOARD ASSY:SECONDARY	80009	670-3057-00
A68	670-8244-00			CKT BOARD ASSY:PS LINE	80009	670-8244-00
A70	670-7474-00			CKT BOARD ASSY:FRONT PANEL	80009	670-7474-00
A75	670-7951-01			CKT BOARD ASSY:256K BYTE MEMORY	80009	670-7951-00
A75	----- -----			(8560/8561 ONLY)		
A80	119-1617-01			CONTROLLER DISK:	80009	119-1617-01
A80	----- -----			(REPLACEABLE AS A UNIT ONLY)		
A85	670-7952-01			CKT BOARD ASSY:512K BYTE MEMORY	80009	670-7952-00
A85	----- -----			(8562 ONLY)		
A10	670-7208-00			CKT BOARD ASSY:MAIN INTERCONNECT	80009	670-7208-00
A10J2	131-1425-00			TERM SET,PIN:(36) 0.025 SQ RTANG,0.15L	22526	65521-136
A10J3	131-1973-00			CONN,RCPT,ELEC:CKT BD,36 CONT W/O MTG TABS	15476	H807
A10J4	131-1973-00			CONN,RCPT,ELEC:CKT BD,36 CONT W/O MTG TABS	15476	H807
A10J5	131-2409-00			CONN,RCPT,ELEC:CKT BD,2 X 25,MALE	75037	3496-2003
A10J6	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J7	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J8	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J9	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J10	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J11	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J12	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J13	131-2240-00			CONN,RCPT,ELEC:CKT BD,50/100 CONT	05574	000201-5256
A10J14	131-1939-00			TERM. SET,PIN:1 X 14,0.15 SPACING	22526	65561-114
A10J15	131-2406-00			CONN,RCPT,ELEC:CKT BD,2 X 17,MALE	22526	65692-020
A10J16	131-2727-00			CONN,RCPT,ELEC:HEADER,2 X 20,0.100 CTR	22526	65692-026
A10J17	131-2410-00			CONN,RCPT,ELEC:CKT BD,2 X 25,MALE	22526	65496-035
A10J19	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J20	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J21	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J22	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J23	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J24	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J25	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J26	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J27	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J28	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J29	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J30	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J31	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
A10J32	131-1343-00			TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15	119-1447-00			MODULE:PROCESSOR LSI 11/23	54563	5013326-00
A15	----- -----			(8560 & 8561 ONLY)		
A15	119-1793-00			CKT BOARD ASSY:KDJ11-A PROCESSOR	15476	KDJ11-A
A15	----- -----			(8560 OPT 10/F10 & 8561 OPT 10 & 8562 ONLY		
A15	----- -----			REPLACEABLE AS A UNIT ONLY)		
A15C1	283-0786-00			CAP.,FXD,MICA D:745PF,1%,500V	09023	CD19FD(745)F03
A15C2	283-0786-00			CAP.,FXD,MICA D:745PF,1%,500V	09023	CD19FD(745)F03
A15C3	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A15C4	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C5	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C6	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C7	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C8	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C9	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C10	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C11	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C12	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C13	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C14	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C15	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C16	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C17	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C18	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A15C19	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A15C20	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A15C21	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A15C22	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A15C23	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A15C24	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A15C25	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A15C26	283-0198-00			CAP.,FXD,CER DI:0.22UF,20%,50V	56289	1C10Z5U223M050B
A15C27	290-0135-00			CAP.,FXD,ELCTLT:15UF,20%,20V	56289	150D156X0020B2
A15C28	290-0135-00			CAP.,FXD,ELCTLT:15UF,20%,20V	56289	150D156X0020B2
A15C29	290-0261-00			CAP.,FXD,ELCTLT:6.8UF,10%,35V	12954	D6R8B35K1
A15C30	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C31	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C32	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C33	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A15C34	283-0796-00			CAP.,FXD,MICA D:100PF,5%,500V	09023	CD10FD101J03
A15D1	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A15E1	156-0948-02			MICROCIRCUIT,DI:QUAD D F-F,BURN-IN	01295	SN74S175J4
A15E2	156-0180-04			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A15E3	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN	01295	SN74S174(JP4)
A15E4	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TRIGGER BFR	01295	SN74S240J
A15E5	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A15E6	156-1600-00			MICROCIRCUIT,DI:DUAL RETRIG MONO MULTIVIB	01295	SN74LS123NP3
A15E7	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM,0.1W	01121	316E331681
A15E8	118-0998-00			MICROCIRCUIT,DI:8881 NAND GATE QUAD	54563	OBD
A15E9	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A15E10	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A15E11	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A15E12	118-0646-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	27014	DS8641N
A15E13	156-1179-01			MICROCIRCUIT,DI:OCTAL BFR,W/3 STATE OUT	01295	SN74S241 JP4
A15E14	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15E15	118-1108-00			OSCILLATOR:13.824 MHZ,0.05%	54563	1812131-00
A15E16	118-1000-00			MICROCIRCUIT,INTFC:TTL,DUAL TTL TO MOS	54563	OBD
A15E17	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A15E18	156-0304-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74S20
A15E19	156-1055-00			MICROCIRCUIT,DI:QUAD NOR UNIFIED BUS RCVR	27014	DS8640N
A15E20	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A15E21	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A15E22	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A15E23	118-1003-00			MICROCIRCUIT,DI:32 X 8 TS PROM	54563	23266A1-00
A15E24	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A15E25	156-1055-00			MICROCIRCUIT,DI:QUAD NOR UNIFIED BUS RCVR	27014	DS8640N
A15E26	307-0406-00			RES.,FXD,FILM:NETWORK,4.3 AND 7.5K OHM,2%	91637	MPP16-00-5XX
A15E27	156-0735-02			MICROCIRCUIT,DI:4 BIT BISTABLE LCH,BURN-IN	01295	SN74LS75
A15E28	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A15E29	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A15E30	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A15E31	118-1106-00			MICROCIRCUIT,DI:DATA CONTROL HYBRID	54563	5700000-01
A15E32	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A15E33	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A15E34	118-0646-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	27014	DS8641N
A15E35	118-1389-00			MICROCIRCUIT,DI:QUAD J-K FLIP-FLOP	54563	1915367-00
A15E36	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A15E37	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E38	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A15E40	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A15E41	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A15E42	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM,0.1W	01121	316E331681
A15E43	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E44	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	01295	SN74S112JP3
A15E45	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A15E46	156-1058-00			MICROCIRCUIT,DI:OCTAL SCHMITT TRIGGER BFR	01295	SN74S240J
A15E47	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E49	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POS EDGE TRIG	80009	156-0331-03
A15E50	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	07263	74S64
A15E51	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM,0.1W	01121	316E331681
A15E52	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E53	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A15E54	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A15E55	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E56	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A15E58	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A15E59	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A15Q1	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A15R1	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A15R2	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A15R3	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A15R4	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R5	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R6	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A15R7	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A15R8	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A15R9	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A15R10	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A15R11	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15R12	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A15R13	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A15R14	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R15	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A15R16	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A15R17	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A15R18	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A15R19	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A15R20	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A15R21	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A15R22	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A15R23	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A15R24	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R25	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R26	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R27	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R28	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A15R29	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A15R30	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15R31	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A15W3	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20	670-8495-00			CKT BOARD ASSY:UTILITY	80009	670-8495-00
A20C1022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1033	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1054	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1057	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1063	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1108	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C1119	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C2079	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20C2082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C2121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C3031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C3069	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C3093	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C3096	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	59660	855-536-COGO560K
A20C3117	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	59660	855-536-COGO560K
A20C3131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4057	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A20C4058	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20C4079	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C4109	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C5041	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20C5056	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	96733	R3247
A20C5063	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A20C5119	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C6011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C6022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C6043	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20C6046	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A20C6047	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A20C6053	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C6054	283-0078-00			CAP.,FXD,CER DI:0.001UF,20%,500V	59660	0801 547X5F0102M
A20C6139	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7037	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7038	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20C7039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7059	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7067	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7078	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A20C7091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20C7117	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A20CR4037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR5031	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR6039	152-0075-00			SEMICOND DEVICE:SW,GE,22V,40MA	14433	G866
A20CR7098	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR7099	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR7105	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR7106	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20DS1021	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20DS1022	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1023	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1031	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20DS1032	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A20R1035	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R2051	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R3107	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065
A20R4028	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A20R4039	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A20R4047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R4059	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A20R5028	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R5029	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R5031	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R5032	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R5038	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A20R5039	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R5048	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R5049	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R5052	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R5053	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R5064	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A20R5111	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R5121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R5122	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R5131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6031	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A20R6033	321-0382-00			RES.,FXD,FILM:93.1K OHM,1%,0.125W	91637	MFF1816G93101F
A20R6034	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A20R6035	321-0350-00			RES.,FXD,FILM:43.2K OHM,1%,0.125W	91637	MFF1816G43201F
A20R6036	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A20R6037	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A20R6038	321-0352-00			RES.,FXD,FILM:45.3K OHM,1%,0.125W	91637	MFF1816G45301F
A20R6041	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R6042	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R6044	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A20R6045	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R6052	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R6055	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6059	321-0290-00			RES.,FXD,FILM:10.2K OHM,1%,0.125W	91637	MFF1816G10201F
A20R6111	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R6131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R7008	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R7019	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R7023	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R7024	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A20R7045	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A20R7047	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A20R7055	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A20R7056	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R7065	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R7066	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A20R7096	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015

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A20R7097	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R7121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20RP1092	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A20RP3092	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A20RP7030	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A20RP7060	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A20RP7080	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A20TP1058	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A20TP1059	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A20U1010	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A20U1020	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A20U1030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A20U1040	156-0535-02			MICROCIRCUIT,DI:3-STATE HEX BUFFER,SCRN	27014	DM8097NA+
A20U1050	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U1060	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U1070	156-0361-00			MICROCIRCUIT,DI:UNIV A SYN RCVR XMTR	80009	156-0361-00
A20U1080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U1090	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A20U1100	156-0850-02			MICROCIRCUIT,DI:PRGM BIT RATE GEN SCRN	07263	4702BDCQR
A20U1110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U2010	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A20U2020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A20U2030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A20U2040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U2050	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U2060	156-0471-02			MICROCIRCUIT,DI:DUAL 4/1 LINE DATA SEL	01295	SN74LS253NP3
A20U2080	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U2100	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A20U2110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U2120	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
A20U3010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U3020	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
A20U3030	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A20U3040	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A20U3050	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U3060	156-0471-02			MICROCIRCUIT,DI:DUAL 4/1 LINE DATA SEL	01295	SN74LS253NP3
A20U3070	156-0361-00			MICROCIRCUIT,DI:UNIV A SYN RCVR XMTR	80009	156-0361-00
A20U3080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A20U3090	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A20U3100	156-0850-02			MICROCIRCUIT,DI:PRGM BIT RATE GEN SCRN	07263	4702BDCQR
A20U3120	156-0390-02			MICROCIRCUIT,DI:DUAL 4/2 LINE DCDR/DEMUX	01295	SN74LS155
A20U3130	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U4010	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A20U4020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A20U4030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U4040	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A20U4050	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A20U4060	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A20U4080	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U4090	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	01295	SN74LS251
A20U4100	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A20U4110	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U4120	156-0390-02			MICROCIRCUIT,DI:DUAL 4/2 LINE DCDR/DEMUX	01295	SN74LS155
A20U4130	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A

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A20U5010	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A20U5020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A20U5030	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A20U5040	156-0153-02			MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A20U5050	156-0405-03			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602
A20U5060	156-0405-03			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602
A20U5070	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A20U5080	160-2634-00			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-2634-00
A20U5090	160-2633-00			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-2633-00
A20U5100	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U5110	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U5120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A20U5130	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U6010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A20U6020	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A20U6040	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A20U6050	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A20U6070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U6080	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U6090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U6100	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A20U6110	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A20U6130	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A20U7020	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U7040	156-0455-02			MICROCIRCUIT,DI:HEX BUS RECEIVER	80009	156-0455-02
A20U7050	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U7070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A20U7100	156-0866-02			MICROCIRCUIT,DI:13 INP NAND GATES,SCRN	80009	156-0866-02
A20U7110	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A20U7120	156-0111-02			MICROCIRCUIT,DI:BCD TO DEC DC DR/DRVR	01295	SN74145
A20U7130	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A20VR6032	152-0437-00			SEMICOND DEVICE:ZENER,SI,8.2V,2%,0.4W	14552	TD332679
A20Y3111	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05% PARALLEL	75378	MP-024

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A30	670-7330-02			CKT BOARD ASSY:I/O PROCESSOR	80009	670-7330-02
A30	----- -----			(8560 & 8561 QTY 1,8562 QTY 2)		
A30C1011	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A30C1041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C1161	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A30C1171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2101	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	59660	855-536-COGO560K
A30C2102	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	59660	855-536-COGO560K
A30C2131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C2171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C3171	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	96733	TDR43BY100DP
A30C4011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C4171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C5151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C6172	283-0144-00			CAP.,FXD,CER DI:33PF,1%,500V	59660	801-547P2G330G
A30C7011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7011	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A30C7021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30C7071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7102	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A30C7111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30C7171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A30DS1031	150-1037-00			LAMP,LED,RDOUT:7 SEGMENT,LH DECIMAL,ORANGE	58361	03409/MAN36202
A30Q6171	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A30R2041	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R2091	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A30R2111	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065
A30R2161	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A30R2171	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A30R5171	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A30R5172	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A30R5173	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A30R7061	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A30R7071	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R7072	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R7073	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A30R7101	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30R7102	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A30R7141	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A30R7151	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A30RP1021	307-0636-00			RES NTWK,FXD,FI:8,330 OHM,2%,0.125W	01121	316B331
A30RP5111	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A30U1040	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A30U1050	160-1408-02			MICROCIRCUIT,DI:4096 X 8 EPROM	80009	160-1408-02
A30U1060	160-1407-02			MICROCIRCUIT,DI:8192 X 8 EPROM	80009	160-1407-02
A30U1080	160-1406-02			MICROCIRCUIT,DI:8192 X 8 EPROM	80009	160-1406-01
A30U1090	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1100	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1120	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1130	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1150	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1160	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U1170	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A30U2010	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A30U2020	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A30U2030	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U2040	156-0694-02			MICROCIRCUIT,DI:DCDR/3 LINE TO 8 LINE,SCRN	07263	74S138DCQR
A30U2080	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U2090	156-0874-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	04713	SN74LS259
A30U2100	156-0850-02			MICROCIRCUIT,DI:PRGM BIT RATE GEN SCRN	07263	4702BDCQR
A30U2130	156-0396-02			MICROCIRCUIT,DI:QUAD 2-INP 3-STATE BFR	27014	DM8094N/A+
A30U2140	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U2150	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U2160	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U3010	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30U3020	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U3030	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U3040	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U3050	156-1609-00			MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	34649	D8088
A30U3060	156-1606-00			MICROCIRCUIT,DI:DMA CONTROLLER	34649	(C OR D)8237A-5
A30U3110	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U3120	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A30U3130	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U3140	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A30U3150	156-0693-02			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	27014	DM74S139
A30U3160	156-1428-02			MICROCIRCUIT,DI:CLOCK GENERATOR & DRIVER	34649	QD8284A
A30U4010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U4020	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U4030	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U4040	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U4060	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH,SCRN	01295	SN74LS279NP3
A30U4070	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U4080	156-1424-01			MICROCIRCUIT,DI:SERIAL INPUT/OUTPUT	56708	Z80A-SIO/1CS-01
A30U4100	156-1424-01			MICROCIRCUIT,DI:SERIAL INPUT/OUTPUT	56708	Z80A-SIO/1CS-01
A30U4110	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A30U4120	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U4130	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A30U4140	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A30U4150	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U4160	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U4170	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U5010	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U5020	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U5030	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U5040	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A30U5050	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U5060	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U5070	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A30U5080	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A30U5090	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A30U5100	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A30U5110	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A30U5120	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A30U5130	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U5140	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A30U5150	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A30U5160	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A30U5170	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A30U6010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U6020	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U6030	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U6040	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A30U6050	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A30U6060	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A30U6070	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A30U6080	156-1605-00			MICROCIRCUIT,DI:DIRECT MEMORY ACCESS	15476	DC01019.14038
A30U6090	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A30U6100	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A30U6110	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A

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A30U6120	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A30U6130	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A30U6140	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A30U6150	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U6160	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A30U6170	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A30U7010	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7020	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7030	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7040	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7050	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A30U7070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7080	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7100	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A30U7110	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A30U7130	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A30U7140	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A30U7150	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A30U7160	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A30U7170	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A30Y2121	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05% PARALLEL	75378	MP-024
A30Y3170	158-0135-00			XTAL UNIT,QTZ:14.7456 MHZ,0.01%,SERIES	01807	OBD

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A35	670-7308-00			CKT BOARD ASSY:I/O ADAPTER	80009	670-7308-00
A35C1011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C1012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C1013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C1031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C1041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C2011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C2012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C2031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C2051	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A35C2052	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A35C3011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C3012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C3013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C3031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C3041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C3061	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A35C4011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C4012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C4013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C4031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C5011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C5012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C5013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C5031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C5041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C6011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C6012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C6013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C6031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C6061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C7011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C7031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C7041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C7061	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7062	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7063	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7064	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C7065	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35C8011	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C8012	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	51642	200-100-NP0-511G
A35C8013	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A35R2041	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R2042	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R2043	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R2044	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R2045	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R2046	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R2047	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R2048	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R4041	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R4042	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015

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A35R4043	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R4044	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R4045	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R4046	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R4047	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R4048	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6041	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6042	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R6043	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6044	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R6045	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R6046	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6047	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R6048	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6061	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6062	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R6063	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R7059	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A35R7061	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R7062	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R8041	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R8042	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R8043	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R8044	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R8045	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R8046	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R8047	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A35R8048	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35R8049	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A35R8061	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A35U1030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U1040	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A35U2030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U2050	156-0846-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC7905CT
A35U3030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U3040	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A35U4030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U5030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U5040	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A35U6030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U6060	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A35U7030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U7040	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32
A35U7060	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U8030	156-1316-00			MICROCKT,INTFC:QUAD 3 STATE SINGLE ENDED	80009	156-1316-00
A35U8060	156-1315-00			MICROCKT,INTFC:QUAD DIFFERENTIAL RECEIVER	34335	AM26LS32

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40	670-7306-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-7306-00
A40	----- -----			(8560 & 8561 OPT 08 ONLY)		
A40	670-8162-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-8162-00
A40	----- -----			(8561 & 8561 OPT 08 ONLY)		
A40	670-7307-00			CKT BOARD ASSY:I/O CONNECTOR	80009	670-7307-00
A40	----- -----			(8562 ONLY)		
A40J8001	131-1178-03			CONN,RCPT,ELEC:CKT BD,36/72 CONT	80009	131-1178-03
A40J8011	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8021	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8031	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8031	----- -----			(8560/8562 ONLY)		
A40J8041	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8041	----- -----			(8560/8562 ONLY)		
A40J8051	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8061	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8061	----- -----			(8562 ONLY)		
A40J8071	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8071	----- -----			(8562 ONLY)		
A40J8081	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40J8081	----- -----			(8562 ONLY)		
A40J8101	131-1437-00			CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
A40RP1011	307-0594-00			RES NTWK,FXD FI:7,220 OHM,2%,1.0W	91637	CSC08A01101221G
A40RP2011	307-0594-00			RES NTWK,FXD FI:7,220 OHM,2%,1.0W	91637	CSC08A01101221G
A40RP3011	307-0594-00			RES NTWK,FXD FI:7,220 OHM,2%,1.0W	91637	CSC08A01101221G

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A45	670-1277-00			CKT BOARD ASSY:MASS STOARGE CONTROLLER	80009	670-1277-00
A45C1021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C1071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C1081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2083	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A45C2085	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A45C2091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C2164	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A45C3011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C3161	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4023	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4133	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C4171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5132	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5155	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A45C5171	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C5173	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6123	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A45C6151	281-0205-00			CAP.,VAR,PLSTC:5.5-65PF,100V	80031	2810C5R565QJ02F0
A45C6173	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A45CR5151	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A45DS2011	150-1037-00			LAMP,LED,RDOUT:7 SEGMENT,LH DECIMAL,ORANGE	58361	03409/MAN36202
A45J2	131-2221-00			CONN,RCPT,ELEC:CKT BD,50 CONT,MALE	00779	2-86479-9
A45R1031	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R1041	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R2041	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A45R2071	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A45R3023	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A45R3061	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A45R3091	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45R3093	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45R3095	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A45R3112	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R3131	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R3151	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R4021	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R4126	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A45R4131	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R5153	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A45R5156	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45R5157	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45R5158	311-1228-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	32997	3386F-T04-103
A45R5161	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A45R5163	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A45R6071	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A45R6072	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A45R6073	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A45R6074	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A45R6075	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A45R6076	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A45R6077	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A45R6078	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A45R6124	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45R6153	311-1228-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	32997	3386F-T04-103
A45R6155	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A45RP1110	307-0847-00			RES NTWK,FXD,FI:12X220 OHM,12X330 OHM,5%	01121	314E221331
A45RP1160	307-0847-00			RES NTWK,FXD,FI:12X220 OHM,12X330 OHM,5%	01121	314E221331
A45RP2021	307-0636-00			RES NTWK,FXD,FI:8,330 OHM,2%,0.125W	01121	316B331
A45RP6121	307-0611-00			RES NTWK,FXD FI:7,150 OHM,5%,1.125W	32997	4308R101-151J
A45TP5151	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A45TP6111	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A45TP6133	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A45U1010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A45U1020	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A45U1030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A45U1040	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U1060	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U1070	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A45U1080	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U1090	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U1100	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A45U2015	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U2030	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A45U2040	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U2060	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A45U2070	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U2090	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A45U2100	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U2110	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A45U2120	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A45U2130	160-2414-00			MICROCIRCUIT,DI:REGISTERED AND/OR GATE	80009	160-2414-00
A45U2140	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A45U2150	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A45U2160	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U3010	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A45U3020	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR	80009	156-0539-01
A45U3030	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A45U3040	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A45U3060	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A45U3070	156-1841-00			MICROCIRCUIT,DI:16 BIT MICROPROCESSOR,68 P	34649	80186
A45U3090	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U3100	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A45U3110	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A45U3120	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A45U3130	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A45U3140	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A45U3150	156-1393-01			MICROCIRCUIT,DI:QUAD 2 INPUT NAND BFR,SCRN	01295	SN74S38
A45U3160	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A45U4010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A45U4020	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A45U4030	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A45U4040	156-1842-00			MICROCIRCUIT,DI:CMOS,1892 X 8 SRAM	T1126	HM6264P-15
A45U4060	160-2218-00			MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-2218-00
A45U4080	156-1842-00			MICROCIRCUIT,DI:CMOS,1892 X 8 SRAM	T1126	HM6264P-15
A45U4090	160-2219-00			MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-2219-00
A45U4110	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U4115	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U4120	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A45U4125	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U4130	160-2217-00			MICROCIRCUIT,DI:LOGIC ARRAY,PRGM	80009	160-2217-00
A45U4140	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A45U4145	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A45U4150	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A45U4155	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A45U4160	156-1388-00			MICROCIRCUIT,DI:QUAD 2-INP MUX W/STOR,SCRN	04713	SN74LS399
A45U4165	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A45U4170	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A45U4175	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A45U5010	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U5020	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U5030	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U5040	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U5050	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U5060	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A45U5070	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A45U5080	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A45U5090	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A45U5100	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A45U5110	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A45U5120	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A45U5130	156-1983-00			MICROCIRCUIT,DI:FLOPPY DISK CONTROLLER		
A45U5160	156-0389-02			MICROCIRCUIT,DI:4-BIT RT SHF,LFT SHF SR,SCR	01295	SN74LS95(NP3 OR
A45U5170	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A45U6010	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6020	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6030	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6040	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6050	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6060	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6080	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6100	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XVER INV	27014	D58838
A45U6110	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A45U6120	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	01295	SN74LS00 (NP3)
A45U6160	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A45U6170	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	01295	SN74LS00 (NP3)
A45Y2081	158-0115-00			XTAL UNIT,QTZ:16MHZ,0.01%,SERIES	01807	7-13P

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A60	670-8245-00			CKT BOARD ASSY:PS INTERCONNECT	80009	670-8245-00
A60CR4061	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A60CR4063	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A60J1010	131-2194-01			CONN,RCPT,ELEC:CKT BD,12/24 MALE,R ANGLE	00779	1-87229-2
A60J2010	131-1078-00			CONNECTOR,RCPT,:28/56 CONTACT	95238	600-1156Y25GDF30
A60J4010	131-1078-00			CONNECTOR,RCPT,:28/56 CONTACT	95238	600-1156Y25GDF30
A60J5010	131-1078-00			CONNECTOR,RCPT,:28/56 CONTACT	95238	600-1156Y25GDF30
A60J6051	131-2588-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.25 SPACING	00779	1-350948-D
A60R4041	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A60W1061	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62	670-3184-00			CKT BOARD ASSY:INVERTER	80009	670-3184-00
A62C1018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C1019	283-0194-00			CAP.,FXD,CER DI:4.7UF,20%,50V	56289	5C37Z5U475M050B
A62C1030	285-0932-00			CAP.,FXD,PLSTC:1UF,10%,400V	14752	230B1E105K
A62C1051	281-0815-00			CAP.,FXD,CER DI:0.027UF,20%,50V	72982	8005D9AABW5R273M
A62C1054	281-0815-00			CAP.,FXD,CER DI:0.027UF,20%,50V	72982	8005D9AABW5R273M
A62C1056	281-0815-00			CAP.,FXD,CER DI:0.027UF,20%,50V	72982	8005D9AABW5R273M
A62C1059	285-1196-00			CAP.,FXD,PAPER:0.01UF,20%,250V	80009	285-1196-00
A62C2030	285-1226-00			CAP.,FXD,PLSTC:2.6UF,10%,200V	84411	TRW-35
A62C4010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A62C4019	283-0194-00			CAP.,FXD,CER DI:4.7UF,20%,50V	56289	5C37Z5U475M050B
A62C4023	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	51642	400-050-Z5U205M
A62C4030	285-1226-00			CAP.,FXD,PLSTC:2.6UF,10%,200V	84411	TRW-35
A62C4031	283-0078-00			CAP.,FXD,CER DI:0.001UF,20%,500V	59660	0801 547X5F0102M
A62C5052	285-1196-00			CAP.,FXD,PAPER:0.01UF,20%,250V	80009	285-1196-00
A62C5064	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A62C5078	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A62C5079	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	51642	400-050-Z5U205M
A62CR1011	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A62CR1012	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR1013	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR1014	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A62CR1015	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR1016	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A62CR1018	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A62CR1052	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A62CR1053	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A62CR1056	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR1058	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR1062	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR1063	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A62CR4011	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A62CR4015	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR4016	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A62CR4017	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR4018	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A62CR4019	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A62CR4021	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A62CR5012	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A62CR5083	152-0779-00			SEMICOND DEVICE:RECT,SI,200V,0.75A	05828	RW02M
A62L2033	108-0691-00			COIL,RF:1.8MH	76493	02279
A62L2071	108-0909-00			COIL,RF:FIXED,1.6MH	80009	108-0909-00
A62Q1010	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
A62Q1053	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A62Q2010	151-0679-00			TRANSISTOR:SILICON,NPN	04713	SJE362
A62Q3010	151-0679-00			TRANSISTOR:SILICON,NPN	04713	SJE362
A62Q5010	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
A62Q5074	151-1127-00			TRANSISTOR:SILICON,N-CHANNEL	000GU	VN0204T5
A62Q5075	151-1127-00			TRANSISTOR:SILICON,N-CHANNEL	000GU	VN0204T5
A62Q5076	151-1128-00			TRANSISTOR:SILICON,P-CHANNEL	81483	IRF9523
A62Q5085	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A62R1016	315-0102-03			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R1017	307-0115-00			RES.,FXD,CMPSN:7.5 OHM,5%,0.25W	01121	CB75G5
A62R1032	301-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.50W	01121	EB8205

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A62R1051	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A62R1052	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R1054	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A62R1055	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R1057	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R1058	301-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.50W	01121	EB2025
A62R1059	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A62R1060	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A62R1061	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A62R1064	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A62R2032	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A62R2035	301-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.50W	01121	EB2715
A62R3032	308-0387-00			RES.,FXD,WW:178 OHM,1%,3W	91637	RS2B-B178R0F
A62R4012	307-0115-00			RES.,FXD,CMPSN:7.5 OHM,5%,0.25W	01121	CB75G5
A62R4014	315-0102-03			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R4022	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A62R4032	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A62R5062	308-0779-00			RES.,FXD,WW:2 OHM,1%,3W	91637	NS2B-2R000F-T/R
A62R5063	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A62R5072	308-0779-00			RES.,FXD,WW:2 OHM,1%,3W	91637	NS2B-2R000F-T/R
A62R5073	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R5074	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R5080	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A62R5081	301-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.50W	01121	EB2015
A62R5082	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A62R5084	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A62T3051	120-1511-00			TRANSFORMER,RF:TOROID,COMMON MODE		
A62T4051	120-1528-00			TRANSFORMER,RF:DRIVER	80009	120-1528-00
A62T4071	120-1432-00			TRANSFORMER,RF:CURRENT	80009	120-1432-00
A62TP5085	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A62TP5086	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A62U1050	156-1381-00			MICROCIRCUIT,LI:XSTR ARRAY	02735	CA3096AE-17
A62VR5082	152-0647-00			SEMICOND DEVICE:ZENER,0.4W,6.8V,5%	04713	SZG35014K3RL

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A64	670-3163-00			CKT BOARD ASSY:REGULATOR	80009	670-3163-00
A64C1015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C1016	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C1021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C1032	281-0861-00			CAP.,FXD,CER DI:270 PF,5%,50V	04222	GC105A271J
A64C1036	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A64C1041	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A64C1045	290-0916-00			CAP.,FXD,ELCTLT:2200UF,+50-10%,35V	55680	ULB1V222TFAANA
A64C2037	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A64C2048	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A64C2051	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A64C2053	290-0922-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,50V	55680	ULB1E102TFAANA
A64C2064	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C2068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C2071	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A64C3011	281-0707-00			CAP.,FXD,CER DI:15000PF,20%,100V	20932	402EM200AD153K
A64C3013	281-0707-00			CAP.,FXD,CER DI:15000PF,20%,100V	20932	402EM200AD153K
A64C3015	283-0341-00			CAP.,FXD,CER DI:0.047UF,10%,100V	72982	8121N153X7R0473K
A64C3016	281-0865-00			CAP.,FXD,CER DI:1000PF,5%,100V	04222	MA201A102JAA
A64C3017	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C3021	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A64C3026	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C3031	285-1049-00			CAP.,FXD,PLSTC:0.01UF,1%,200V	14752	230B1C103F
A64C3052	290-0922-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,50V	55680	ULB1E102TFAANA
A64C3072	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A64C4013	285-0905-00			CAP.,FXD,PLSTC:0.33UF,5%,50V	56289	LP66A1A334J002
A64C4028	283-0341-00			CAP.,FXD,CER DI:0.047UF,10%,100V	72982	8121N153X7R0473K
A64C4029	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C4031	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A64C4038	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A64C4058	281-0865-00			CAP.,FXD,CER DI:1000PF,5%,100V	04222	MA201A102JAA
A64C4061	283-0100-00			CAP.,FXD,CER DI:0.0047UF,10%,200V	56289	273C3
A64C4062	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A64C4063	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A64C4065	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C4066	281-0865-00			CAP.,FXD,CER DI:1000PF,5%,100V	04222	MA201A102JAA
A64C5012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C5014	281-0865-00			CAP.,FXD,CER DI:1000PF,5%,100V	04222	MA201A102JAA
A64C5019	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A64C5021	281-0537-00			CAP.,FXD,CER DI:0.68PF,20%,600V	95121	OC-.68MM 20%
A64C5022	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A64C5037	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A64C5073	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A64C5074	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A64C6018	281-0865-00			CAP.,FXD,CER DI:1000PF,5%,100V	04222	MA201A102JAA
A64C6037	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C6038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64C6041	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	51642	400-050-Z5U205M
A64C6046	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A64C6066	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A64CR1019	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR1032	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR1057	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,200V,1A	80009	152-0585-00
A64CR2024	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

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A64CR2025	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR2061	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A64CR2062	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A64CR2063	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A64CR2073	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A64CR3021	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3026	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3031	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3032	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3033	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3034	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3041	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3043	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3048	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR3051	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4014	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4023	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4024	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4032	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4039	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4041	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4042	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4045	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR4064	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR5026	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR5036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6013	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6014	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6025	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6043	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6055	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR6061	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR7035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64CR7046	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A64DS7052	150-1063-00			LT EMITTING DIO:YELLOW,585 NM,40 MA	72619	550-0305-804
A64Q1034	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q1035	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q2022	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q3029	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q3037	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A64Q3038	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A64Q3043	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A64Q4016	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q4038	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q4046	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q4047	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q6019	151-1005-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	27014	F55037
A64Q6021	151-1066-00			TRANSISTOR:SILICON,FE,P-CHANNEL	27014	SF88025
A64Q6025	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A64Q6026	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A64Q6047	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677

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A64Q7045	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A64R1011	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A64R1012	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A64R1018	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A64R1023	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A64R1031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A64R1032	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A64R1033	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A64R1034	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A64R2012	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R2021	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R2023	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A64R2025	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A64R2026	303-0221-00			RES.,FXD,CMPSN:220 OHM,5%,1W	01121	GB2215
A64R2033	301-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.50W	01121	EB1525
A64R2034	321-0264-00			RES.,FXD,FILM:5.49K OHM,1%,0.125W	91637	MFF1816G54900F
A64R2036	321-0243-00			RES.,FXD,FILM:3.32K OHM,1%,0.125W	91637	MFF1816G33200F
A64R2037	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A64R2038	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A64R2047	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A64R2065	321-0234-00			RES.,FXD,FILM:2.67K OHM,1%,0.125W	91637	MFF1816G26700F
A64R2066	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A64R2067	321-0234-00			RES.,FXD,FILM:2.67K OHM,1%,0.125W	91637	MFF1816G26700F
A64R2074	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A64R3012	321-0342-00			RES.,FXD,FILM:35.7K OHM,1%,0.125W	91637	MFF1816G35701F
A64R3013	321-0358-00			RES.,FXD,FILM:52.3K OHM,1%,0.125W	91637	MFF1816G52301F
A64R3014	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A64R3015	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A64R3017	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A64R3018	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A64R3019	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A64R3025	301-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.50W	01121	EB1525
A64R3027	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A64R3028	321-0188-00			RES.,FXD,FILM:887 OHM,1%,0.125W	91637	MFF1816G887R0F
A64R3029	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A64R3042	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R3044	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R3045	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R3046	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A64R3047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A64R3051	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A64R3052	321-0358-00			RES.,FXD,FILM:52.3K OHM,1%,0.125W	91637	MFF1816G52301F
A64R3062	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R3063	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A64R4015	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A64R4032	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	01121	CB1345
A64R4033	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A64R4034	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R4035	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A64R4036	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R4037	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A64R4041	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A64R4043	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A64R4044	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535

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A64R4045	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A64R4047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A64R4048	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A64R4049	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A64R4051	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A64R4067	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A64R5014	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R5015	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A64R5016	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A64R5017	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A64R5018	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A64R5019	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R5027	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R5028	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R5029	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A64R5031	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A64R5038	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A64R5039	321-0280-00			RES.,FXD,FILM:8.06K OHM,1%,0.125W	91637	MFF1816G80600F
A64R5041	321-0322-00			RES.,FXD,FILM:22.1K OHM,1%,0.125W	91637	MFF1816G22101F
A64R5045	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A64R5046	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A64R5047	321-0188-00			RES.,FXD,FILM:887 OHM,1%,0.125W	91637	MFF1816G887R0F
A64R5048	321-0246-00			RES.,FXD,FILM:3.57K OHM,1%,0.125W	91637	MFF1816G35700F
A64R5051	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A64R5065	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A64R5066	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A64R5071	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A64R6011	315-0226-00			RES.,FXD,CMPSN:22M OHM,5%,0.25W	01121	CB2265
A64R6012	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R6022	315-0184-00			RES.,FXD,CMPSN:180K OHM,5%,0.25W	01121	CB1845
A64R6023	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A64R6025	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R6026	301-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.50W	01121	EB1525
A64R6027	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R6028	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A64R6039	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A64R6044	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A64R6045	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R6056	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R6071	321-0279-00			RES.,FXD,FILM:7.87K OHM,1%,0.125W	91637	MFF1816G78700F
A64R6072	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A64R7031	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A64R7033	321-0241-00			RES.,FXD,FILM:3.16K OHM,1%,0.125W	91637	MFF1816G31600F
A64R7036	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R7037	321-0302-00			RES.,FXD,FILM:13.7K OHM,1%,0.125W	91637	MFF1816G13701F
A64R7041	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A64R7042	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R7043	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A64R7044	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A64R7051	301-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.50W	57668	NTR501E620E
A64R7055	307-0972-00			RES.,THERMAL:1K OHM,5%,0.25W	50157	2K-102-J
A64R7067	311-1340-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	02111	43P102T672
A64TP7015	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7025	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00

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A64TP7039	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7043	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7046	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7048	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7056	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7057	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7058	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7061	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7066	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7076	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64TP7077	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A64U1060	156-1161-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM317T
A64U1070	156-1451-00			MICROCIRCUIT,DI:3-TERM NEG VOLTAGE RGLTR	27014	LM337T
A64U2010	156-1126-01			MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A64U2030	156-0524-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATES	80009	156-0524-02
A64U2040	156-0350-05			MICROCIRCUIT,DI:QUAD 2 INPUT NAND GATE,CHK	80009	156-0350-05
A64U3030	156-1126-01			MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A64U3040	156-0366-02			MICROCIRCUIT,DI:DUAL D FLIP-FLOP,CHK	80009	156-0366-02
A64U5030	156-1225-01			MICROCIRCUIT,LI:DUAL COMPARATOR,SCREENED	27014	LM393N/AT
A64U5040	156-1225-01			MICROCIRCUIT,LI:DUAL COMPARATOR,SCREENED	27014	LM393N/AT
A64U5060	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A64U6010	156-1191-00			MICROCIRCUIT,LI:BI-FET OPNL AMPL	01295	TL072ACP
A64U6040	156-0402-03			MICROCIRCUIT,LI:TIMER,TESTED	80009	156-0402-03
A64U7040	156-1225-01			MICROCIRCUIT,LI:DUAL COMPARATOR,SCREENED	27014	LM393N/AT
A64VR2035	152-0662-00			SEMICOND DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
A64VR4025	152-0760-00			SEMICOND DEVICE:ZEN,SI,6.2V,2%,400MW	04713	SZ630205
A64VR4026	152-0760-00			SEMICOND DEVICE:ZEN,SI,6.2V,2%,400MW	04713	SZ630205
A64VR4027	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A64VR4039	152-0667-00			SEMICOND DEVICE:ZENER,0.4W,3.0V,2%	04713	SZG30025RL
A64VR4051	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A64VR5013	152-0281-00			SEMICOND DEVICE:ZENER,0.4W,22V,5%	12954	1N969B
A64VR5047	152-0662-00			SEMICOND DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
A64VR5072	152-0317-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	04713	SZG20012
A64VR6024	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL

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A66	670-3057-00			CKT BOARD ASSY:SECONDARY	80009	670-3057-00
A66C1045	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	04222	MA101C102MAA
A66C1051	290-0964-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,12V	90201	VPR122N012E1L1J
A66C1053	290-0964-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,12V	90201	VPR122N012E1L1J
A66C1091	290-0916-00			CAP.,FXD,ELCTLT:2200UF,+50-10%,35V	55680	ULB1V222TFAANA
A66C1102	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A66C2061	290-0946-00			CAP.,FXD,ELCTLT:270UF,10+100%,40V	90201	VPR271N040E1E1C
A66C2096	290-0974-00			CAP.,FXD,ELCTLT:10UF,20%,50VDC	55680	ULB1H100MEA
A66C2098	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	04222	MA101C102MAA
A66C2101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C2102	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C2106	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A66C2113	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A66C3031	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A66C3037	281-0815-00			CAP.,FXD,CER DI:0.027UF,20%,50V	72982	8005D9AABW5R273M
A66C3039	281-0815-00			CAP.,FXD,CER DI:0.027UF,20%,50V	72982	8005D9AABW5R273M
A66C3062	290-0950-00			CAP.,FXD,ELCTLT:100UF,+50-10%,50V	55680	ULB1H101TJAANA
A66C3072	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A66C3074	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A66C3094	290-0918-00			CAP.,FXD,ELCTLT:220UF,+50-10%,63V	55680	TLB1J221TCAANA
A66C3111	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A66C3114	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C3115	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C3116	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C3117	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A66C4095	283-0059-00			CAP.,FXD,CER DI:1UF,+80-20%,50V	51642	400050Z5U105Z
A66C4115	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	51642	G1710100NP0151K
A66CR1041	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A66CR1043	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A66CR1061	152-0582-00			SEMICOND DEVICE:SILICON,20V,3A	04713	1N5820
A66CR2031	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A66CR2033	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A66CR3032	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A66CR3033	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A66CR3036	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A66CR3038	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A66CR3112	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A66CR4011	152-0810-00			SEMICOND DVC,DI:RECT,SI,150V,7A FAST	12969	UES1430
A66CR4012	152-0810-00			SEMICOND DVC,DI:RECT,SI,150V,7A FAST	12969	UES1430
A66CR4015	152-0714-00			SEMICOND DEVICE:RECT,SI,SCHOTTKY,40V,50A	01281	1N6098
A66CR4035	152-0714-00			SEMICOND DEVICE:RECT,SI,SCHOTTKY,40V,50A	01281	1N6098
A66CR4082	152-0720-00			SEMICOND DEVICE:SILICON,100V,7A	80009	152-0720-00
A66F3071	159-0015-01			FUSE,CARTRIDGE:3AG,3A,250V,FAST-BLOW	71400	GJV3
A66F3092	159-0193-00			FUSE,WIRE LEAD:10A,125V,5 SEC	T0946	SP-5 10A
A66L1055	108-1125-00			COIL,RF:FIXED,2.3UH	80009	108-1125-00
A66L2041	108-1126-00			COIL,RF:FIXED,10.5UH	80009	108-1126-00
A66L3023	108-0981-00			COIL,RF:FIXED,270UH	80009	108-0981-00
A66L3061	108-1107-00			COIL,RF:FIXED,4MH	80009	108-1107-00
A66L3083	108-0923-00			COIL,RF:FIXED,1.3MH	80009	108-0923-00
A66L4091	108-1207-00			COIL,RF:87MH,10%	80009	108-1207-00
A66Q1031	151-1120-00			TRANSISTOR:FE,P CHANNEL,SI,VP-3	000GU	VP0106N3
A66Q1049	151-1120-00			TRANSISTOR:FE,P CHANNEL,SI,VP-3	000GU	VP0106N3
A66Q1057	151-0710-00			TRANSISTOR:SILICON,NPN	27014	2N6715/92 PU01A
A66Q2063	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11

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A66Q2071	151-0364-00			TRANSISTOR:SILICON,PNP	80009	151-0364-00
A66Q2073	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
A66Q3101	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A66Q3102	151-0439-00			TRANSISTOR:SILICON,NPN	80009	151-0439-00
A66Q4109	151-0660-00			TRANSISTOR:SILICON,NPN	01295	EP2785
A66R1047	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1048	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1063	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R1101	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1103	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1111	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1112	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R1113	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1114	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R1119	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A66R2081	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A66R2082	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A66R2084	308-0695-00			RES.,FXD,WW:0.05 OHM,10%,5W	91637	RLS-5 .05OHM,10%
A66R2091	308-0695-00			RES.,FXD,WW:0.05 OHM,10%,5W	91637	RLS-5 .05OHM,10%
A66R2097	308-0179-00			RES.,FXD,WW:5 OHM,5%,5W	91637	CW5-5RD00J
A66R2103	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R2104	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A66R2105	321-0374-00			RES.,FXD,FILM:76.8K OHM,1%,0.125W	91637	MFF1816G76801F
A66R2107	321-0362-00			RES.,FXD,FILM:57.6K OHM,1%,0.125W	91637	MFF1816G57601F
A66R2111	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A66R2112	321-0351-00			RES.,FXD,FILM:44.2K OHM,1%,0.125W	91637	MFF1816G44201F
A66R2114	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A66R2115	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R2116	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A66R3021	303-0151-00			RES.,FXD,CMPSN:150 OHM,5%,1W	01121	GB1515
A66R3025	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A66R3027	307-0007-00			RES.,FXD,CMPSN:2.7 OHM,10%,2W	01121	GB27G1
A66R3029	307-0007-00			RES.,FXD,CMPSN:2.7 OHM,10%,2W	01121	GB27G1
A66R3034	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A66R3035	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A66R3063	321-0223-00			RES.,FXD,FILM:2.05K OHM,1%,0.125W	91637	MFF1816G20500F
A66R3091	308-0070-00			RES.,FXD,WW:	63743	7404
A66R3101	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A66R3102	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R3103	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A66R3104	321-0411-00			RES.,FXD,FILM:187K OHM,1%,0.125W	91637	MFF1816G18702F
A66R3105	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R3106	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A66R3107	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A66R3108	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R3109	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A66R3112	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A66R3113	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A66R3118	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A66R3119	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A66R4037	308-0818-00			RES.,FXD,WW:0.005 OHM,3%,10W	91637	RH10-89/.005 3%
A66R4067	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A66R4073	308-0702-00			RES.,FXD,WW:0.33 OHM,5%,2W	75042	BWH-R3300J
A66R4075	303-0360-00			RES.,FXD,CMPSN:36 OHM,5%,1W	01121	GB3605

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A66R4083	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A66R4099	308-0843-00			RES.,FXD WW:0.2 OHM,5%,1.0W	91637	RS1AR2000JT/R
A66R4101	308-0843-00			RES.,FXD WW:0.2 OHM,5%,1.0W	91637	RS1AR2000JT/R
A66R4111	315-0685-00			RES.,FXD CMPSN:6.8M OHM,5%,0.25W	01121	CB6855
A66R4113	321-0370-00			RES.,FXD,FILM:69.8K OHM,1%,0.125W	91637	MFF1816G69801F
A66R4117	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A66T1011	120-1527-00			XFMR,PWR,STDN:HIGH FREQUENCY	80009	120-1527-00
A66TP1	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A66TP2	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A66TP3	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A66TP4	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A66TP5	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A66U2110	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A66U3110	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A66U4060	156-1451-00			MICROCIRCUIT,DI:3-TERM NEG VOLTAGE RGLTR	27014	LM337T
A66VR1104	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	TD3810983
A66VR1115	152-0147-00			SEMICOND DEVICE:ZENER,0.4W,27V,5%	04713	SZ50622KRL
A66VR1116	152-0571-00			SEMICOND DEVICE:ZENER,0.4W,16V,5%	04713	SZ35014K1
A66VR1117	152-0702-00			SEMICOND DEVICE:ZENER,500MW,13V,2%	04713	SZG30214RL
A66VR1118	152-0175-01			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG5021RL
A66W3035	175-4700-00			CABLE ASSY,SP,ELEC:4,26 AWG,3.0L,RIBBON	80009	175-4700-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A68	670-8244-00			CKT BOARD ASSY:PS LINE	80009	670-8244-00
A68C1017	290-1015-00			CAP.,FXD,ELCTLT:1000UF,+100-10%,200V	00853	DCM102M200AA2P
A68C1019	290-1015-00			CAP.,FXD,ELCTLT:1000UF,+100-10%,200V	00853	DCM102M200AA2P
A68C2011	290-1015-00			CAP.,FXD,ELCTLT:1000UF,+100-10%,200V	00853	DCM102M200AA2P
A68C2013	290-1015-00			CAP.,FXD,ELCTLT:1000UF,+100-10%,200V	00853	DCM102M200AA2P
A68C2024	285-1192-00			CAP.,FXD,PPR DI:0.0022UF,20%,250VAC	000FG	PME271Y422
A68C2025	285-1222-00			CAP.,FXD,PLSTC:0.068UF,20%,250V	55112	158/.068/M/250/H
A68C2026	285-1192-00			CAP.,FXD,PPR DI:0.0022UF,20%,250VAC	000FG	PME271Y422
A68C2031	285-1250-00			CAP.,FXD,PPR DI:0.1UF,20%,250VAC	D5243	F1772-410-2000
A68CR2027	152-0838-00			SEMICOND,DI:BRIDGE RECT,SI,400V,8A		
A68E1025	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L
A68E2023	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L
A68F2023	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
A68F2037	159-0174-00			FUSE,CARTRIDGE:3AG,8A,250V,5 SEC	71400	ABC-8
A68P1	131-2803-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.25	00779	350430-1
A68P2	131-2663-00			CONN.,RCPT,ELEC:PWR,3 MALE,250VAC,6A	82389	EAC 303
A68P3	131-2802-00			CONN,RCPT,ELEC: HEADER,1 X 3,0.25 CENTERS	00779	350429-1
A68R1011	303-0114-00			RES.,FXD,CMPSN:110K OHM,5%,1W	01121	GB1145
A68R1013	305-0393-00			RES.,FXD,CMPSN:39K OHM,5%,2W	01121	HB3935
A68R1023	303-0513-00			RES.,FXD,CMPSN:51K OHM,5%,1W	01121	GB5135
A68R2021	307-0746-00			RES.,THERMAL:5 OHM,10%,7A/DEG C	15454	SG-6
A68R2022	307-0746-00			RES.,THERMAL:5 OHM,10%,7A/DEG C	15454	SG-6
A68SW2035	260-2042-00			SWITCH,SLIDE:DPDT,5A,250VAC	T0935	4021.4220
A68T1015	120-1511-00			TRANSFORMER,RF:TOROID,COMMON MODE		
A68VR1021	152-0241-00			SEMICOND DEVICE:ZENER,0.4W,33V,5%	04713	SZG35009K5

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A70	670-7474-00			CKT BOARD ASSY:FRONT PANEL	80009	670-7474-00
A70C1027	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A70R1012	303-0751-00			RES.,FXD,CMPSN:750 OHM,5%,1W	01121	GB7515
A70R1022	301-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.50W	01121	EB1315
A70R1024	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A70R1025	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A70R1026	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A70R1027	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A70R1028	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A70U1010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A75	670-7951-01			CKT BOARD ASSY:256K BYTE MEMORY	80009	670-7951-00
A75	----- -----			(8560/8561 ONLY)		
A75C1032	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A75C1162	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A75C3011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C3181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C4181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C5141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C5151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C5161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C5172	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6122	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6132	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A75C6141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C6181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7092	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7102	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7112	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7152	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C7162	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A75C8010	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A75R5152	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A75R7101	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A75R7141	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A75R7142	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A75R7151	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A75RP7091	307-1096-00			RES NTWK,FXD,FI:7,2 OHM,2%,1W	57924	4308R-101-202
A75TP5171	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A75TP6171	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A75TP7143	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A75TP7144	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A75U3010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U3180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A75U4110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U4180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A75U5020	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A75U5030	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A75U5040	156-1749-00			MICROCIRCUIT,DI:DYUNAMIC MEMORY CONTROLLER	34335	AM2964BDCB
A75U5060	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A75U5130	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A75U5140	156-1726-00			MICROCIRCUIT,DI:DUAL 1 OF 4 DCDR,SCRN	07263	74F139
A75U5150	156-1743-00			MICROCIRCUIT,DI:QUAD 2 INPUT NOR GATE	07263	74F02(PCQR OR DC
A75U5160	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A75U5170	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A75U6020	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A75U6030	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A75U6080	156-0652-02			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL NOR GATE	01295	SN74LS266
A75U6090	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A75U6100	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN	01295	SN74S174(JP4)
A75U6110	156-1752-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	07263	74F10NDS/JDS
A75U6120	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A75U6130	156-1752-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	07263	74F10NDS/JDS
A75U6140	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	01295	SN74LS221N3
A75U6150	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A75U6160	156-0966-01			MICROCIRCUIT,DI:DUAL 5 INP NOR GATES	80009	156-0966-01
A75U6170	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A75U7040	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838
A75U7050	156-1746-00			MICROCIRCUIT,DI: 8 INP DATA SEL,SCRN	01295	SN74S151
A75U7080	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A75U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838
A75U7100	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838
A75U7110	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A75U7120	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN	01295	SN74S174(JP4)
A75U7140	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A75U7150	156-1723-00			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE	07263	74F08
A75U7160	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A75W7061	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75W7063	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75W7065	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75W7067	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75W7069	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75W8062	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A75Y7170	119-1599-00			OSC,XTAL CLOCK:25MHZ,0.05%	04713	K1114A
A80	119-1617-01			CONTROLLER DISK:	80009	119-1617-01
A80	----- -----			(REPLACEABLE AS A UNIT ONLY)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A85	670-7952-01			CKT BOARD ASSY:512K BYTE MEMORY	80009	670-7952-00
A85	----- -----			(8562 ONLY)		
A85C1011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1032	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A85C1041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1162	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A85C1171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C1181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C2181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A85C3151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C3181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4011	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4111	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C4181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C5141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C5151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C5161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C5172	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6061	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6071	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6091	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6101	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6122	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6132	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6141	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6151	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C6181	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7021	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7031	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7041	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7051	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7081	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7092	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7102	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7112	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7121	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7152	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C7162	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A85C8010	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A85R5152	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A85R7101	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A85R7141	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A85R7142	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A85R7151	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A85RP7091	307-1096-00			RES NTWK,FXD,FI:7,2 OHM,2%,1W	57924	4308R-101-202
A85TP5171	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A85TP6171	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A85TP7143	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A85TP7144	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A85U1010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U1180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U2180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A85U3110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U3180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4010	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4020	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4030	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4040	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4050	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4060	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4070	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4080	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4090	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4100	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4110	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4120	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4130	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4140	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4150	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4160	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4170	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U4180	156-1626-00			MICROCIRCUIT,DI:NMOS,65536 X1 DRAM	04713	MCM6665AL-20
A85U5020	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A85U5030	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A85U5040	156-1749-00			MICROCIRCUIT,DI:DYNAMIC MEMORY CONTROLLER	34335	AM2964BDCB
A85U5060	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A85U5070	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A85U5120	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A85U5130	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2966DCB
A85U5140	156-1726-00			MICROCIRCUIT,DI:DUALL 1 OF 4 DCDR,SCRN	07263	74F139
A85U5150	156-1743-00			MICROCIRCUIT,DI:QUAD 2 INPUT NOR GATE	07263	74F02(PCQR OR DC
A85U5160	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A85U5170	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A85U6020	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A85U6030	156-1618-00			MICROCIRCUIT,DI:QUAD BUS TRANSCEIVER	34335	AM2908DCB
A85U6080	156-0652-02			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL NOR GATE	01295	SN74LS266
A85U6090	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A85U6100	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN	01295	SN74S174(JP4)
A85U6110	156-1752-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATES	07263	74F10NDS/JDS
A85U6120	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A85U6130	156-1752-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATES	07263	74F10NDS/JDS
A85U6140	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	01295	SN74LS221N3
A85U6150	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A85U6160	156-0966-01			MICROCIRCUIT,DI:DUAL 5 INP NOR GATES	80009	156-0966-01
A85U6170	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A85U7040	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838
A85U7050	156-1746-00			MICROCIRCUIT,DI: 8 INP DATA SEL,SCRN	01295	SN74S151
A85U7080	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A85U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838
A85U7100	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS	27014	DS8838

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A85U7110	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A85U7120	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN	01295	SN74S174(JP4)
A85U7140	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A85U7150	156-1723-00			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE	07263	74F08
A85U7160	156-1707-00			MICROCIRCUIT,DI: QUAD 2-INPUT NAND GATE	07263	74F00PCQR
A85W7061	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85W7063	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85W7065	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85W7067	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85W7069	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85W8062	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A85Y7170	119-1599-00			OSC,XTAL CLOCK:25MHZ,0.05%	04713	K1114A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B610	119-1751-00			FAN,TUBEAXIAL:80CFM,12VDC,1A	T0510	FB12C12L
DS1032	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
DS1038	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
DS1052	150-0093-01			LAMP,INCAND:5V,0.06A,0.05 MSCP,SEL	87034	9AS15
F100	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
F615	159-0174-00			FUSE,CARTRIDGE:3AG,8A,250V,5 SEC	71400	ABC-8
F615	----- -----			(STANDARD ONLY)		
F615	159-0017-00			FUSE,CARTRIDGE:3AG,4A,250V,FAST BLOW	71400	MTH4
F615	----- -----			(OPTIONS A1,A2,A3,A4 & A5)		
S615	260-1967-00			SWITCH,SLIDE:DPDT,5A/250V	000FJ	4021.0512
S650	260-1989-00			SWITCH,ROCKER:DPST,16A,250VAC	000FJ	1602-0120
S1014	260-1867-00			SWITCH,TOGGLE:SPDT,0.4A,20V	09353	7108-J61-CB8
S1024	260-1868-00			SWITCH,TOGGLE:SPDT,0.4A,20V	09353	7101-J61-CB8
S1045	260-2028-00			SWITCH,ROCKER:DPDT,0.4A,20VAC	000FJ	OBD
T660	120-1529-00			XFMR,PWR,STPDN:LOW FREQUENCY	80009	120-1529-00

Section 21
DIAGRAMS

Standards

The following American National Standard Institute standards are used in the preparation of Tektronix, Inc. diagrams.

Graphic Symbols	ANSI Y32.2–1975
Logic Symbols	ANSI Y32.14–1973 (Positive logic. Logic symbols depict the logical function performed and may differ from the manufacturer's data.)
Abbreviations	ANSI Y1.1–1972
Drafting Practices	ANSI Y14.15–1966
Line Conventions And Lettering	ANSI Y14.2–1973
Letter Symbols	ANSI Y10.5–1968

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

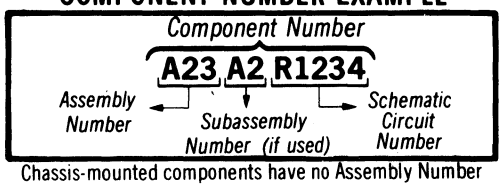
Resistors = Ohms (Ω)

The following special symbols may appear on the diagrams:

Assembly Numbers and Grid Coordinates

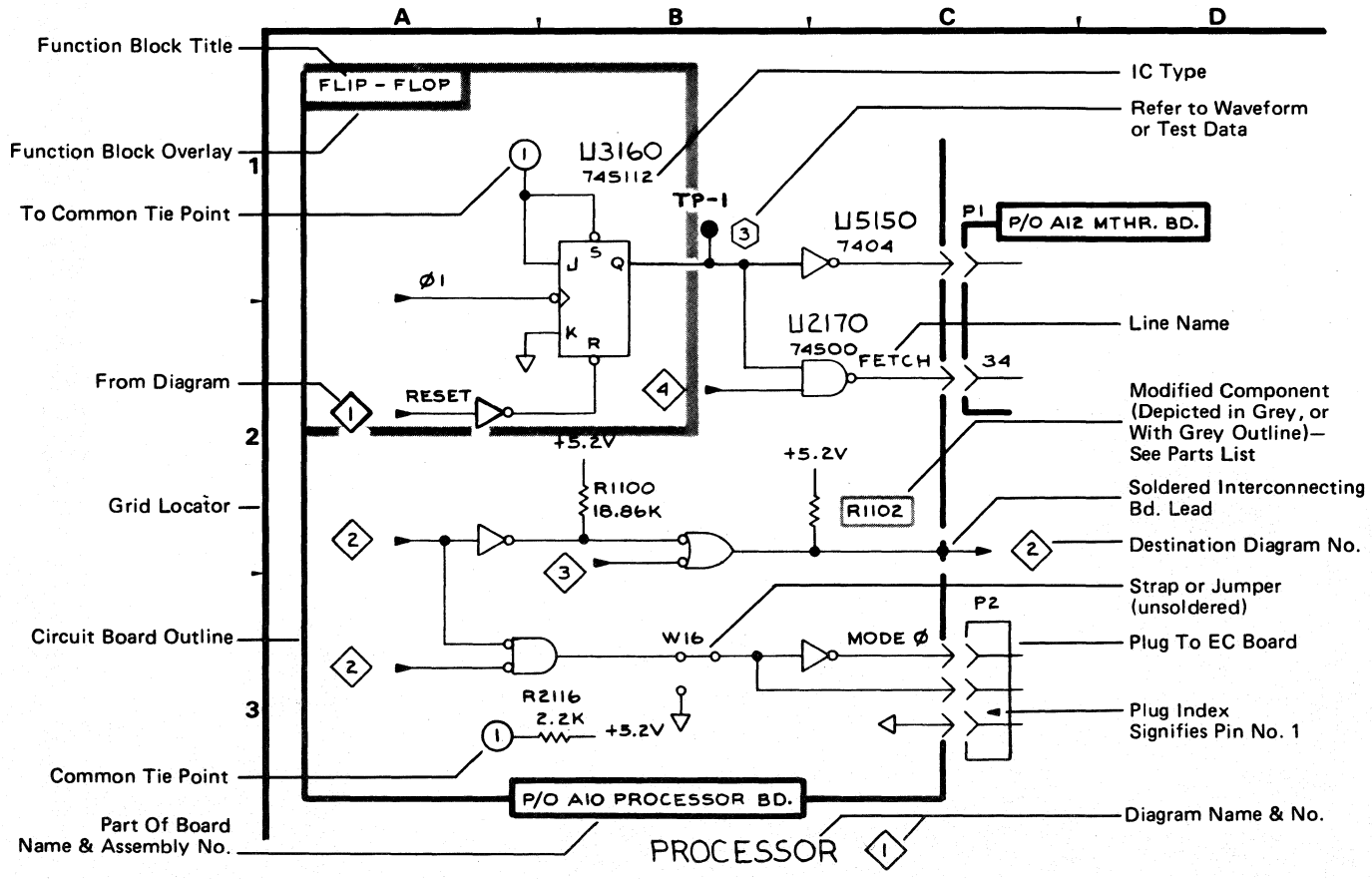
Each circuit board in the instrument is assigned an assembly number (e.g. A20). This number appears on the component location illustration, the schematics, and the component lookup table. The Replaceable Electrical Parts list also uses the number to list components by assembly. The following illustration shows an example of a component number in the Electrical Parts list.

COMPONENT NUMBER EXAMPLE

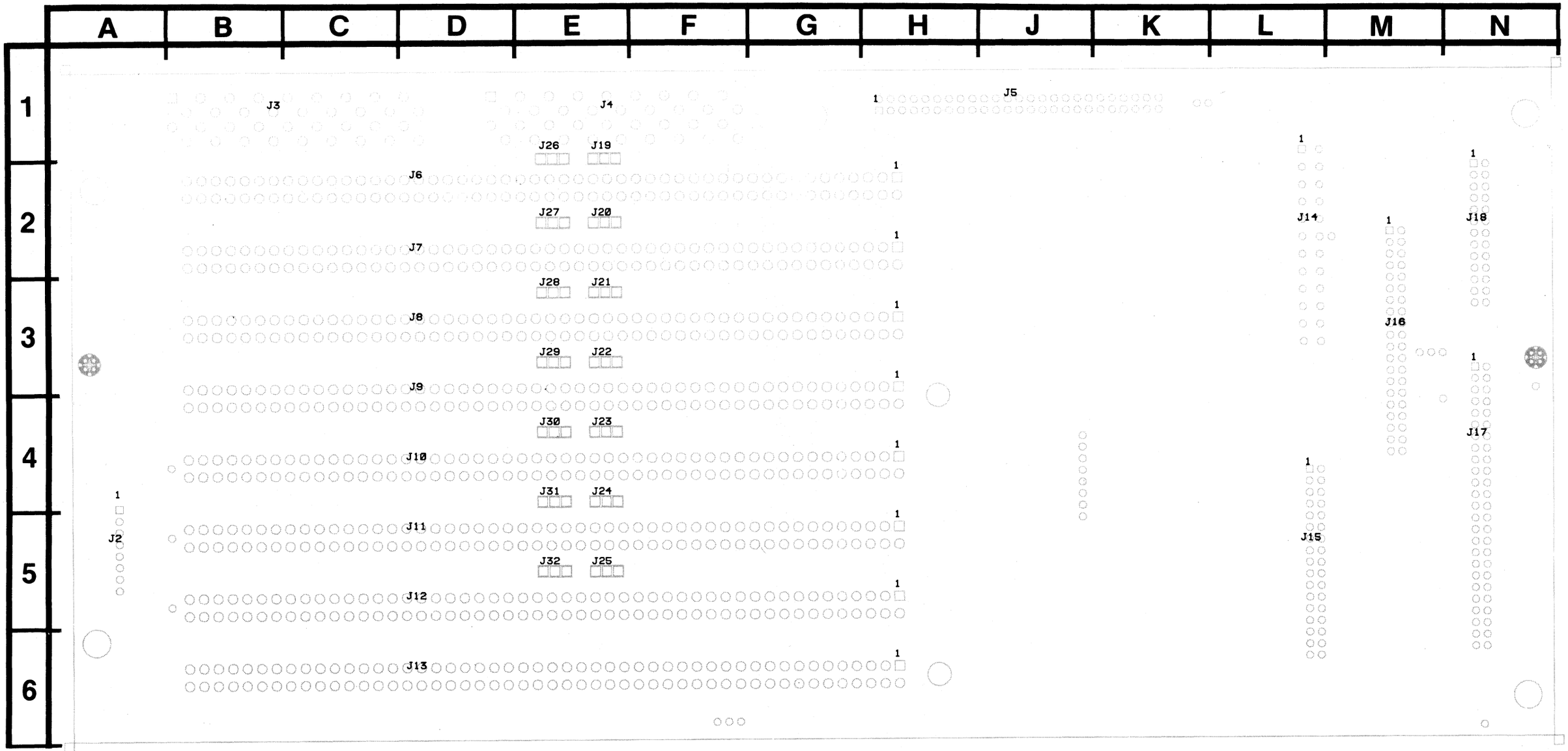


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

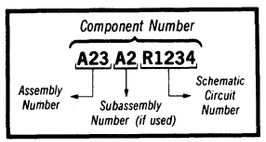
Both the schematics and the component locator illustration have locating grids. A lookup table is assigned to each schematic. The lookup table gives the component location in both the associated schematic, and on the component locator illustration.



MAIN INTERCONNECT
COMPONENT LOCATIONS



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Figure 21-1. A10 Main Interconnect Board.

Static Sensitive Devices
See Maintenance Section

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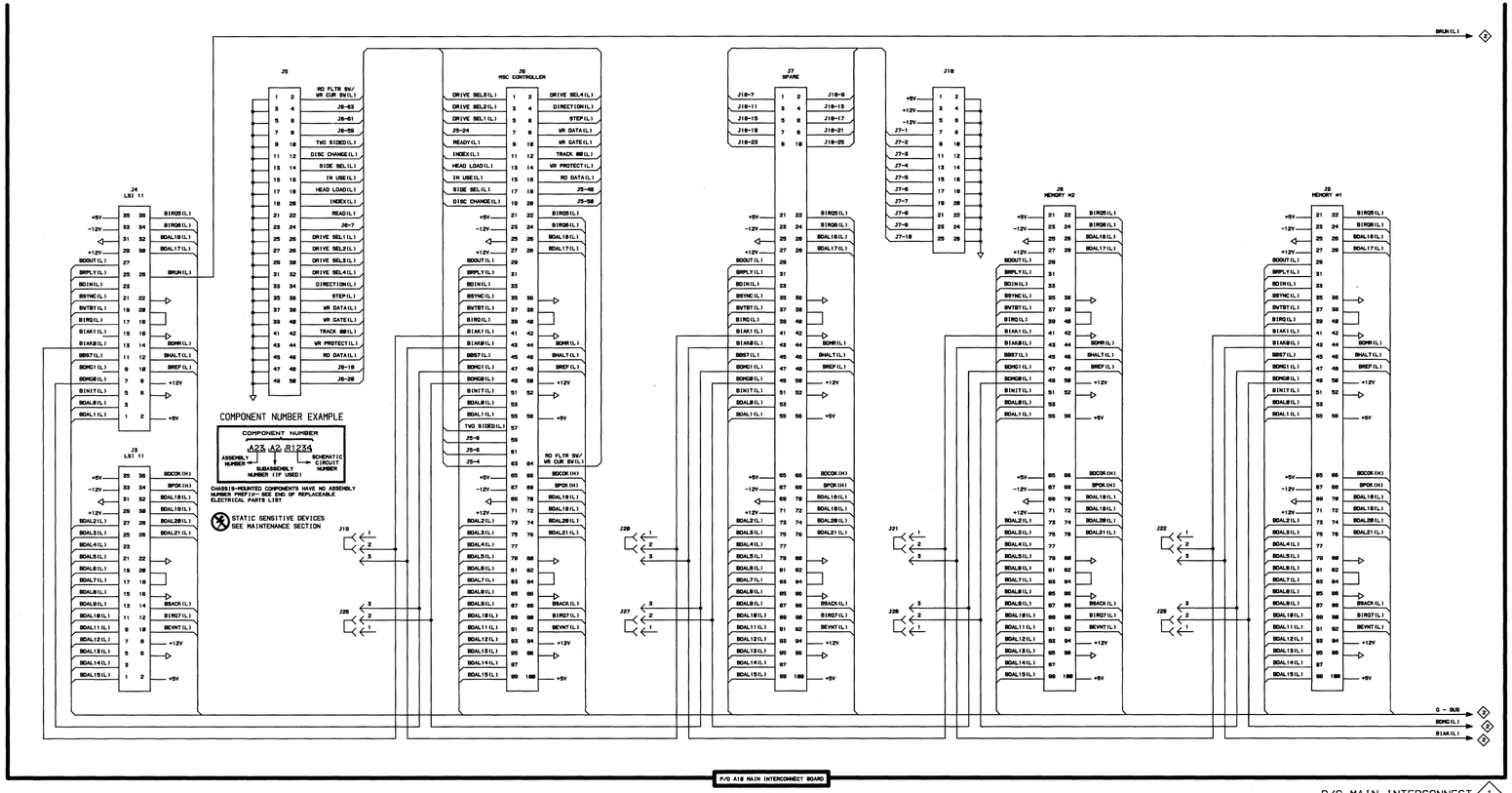
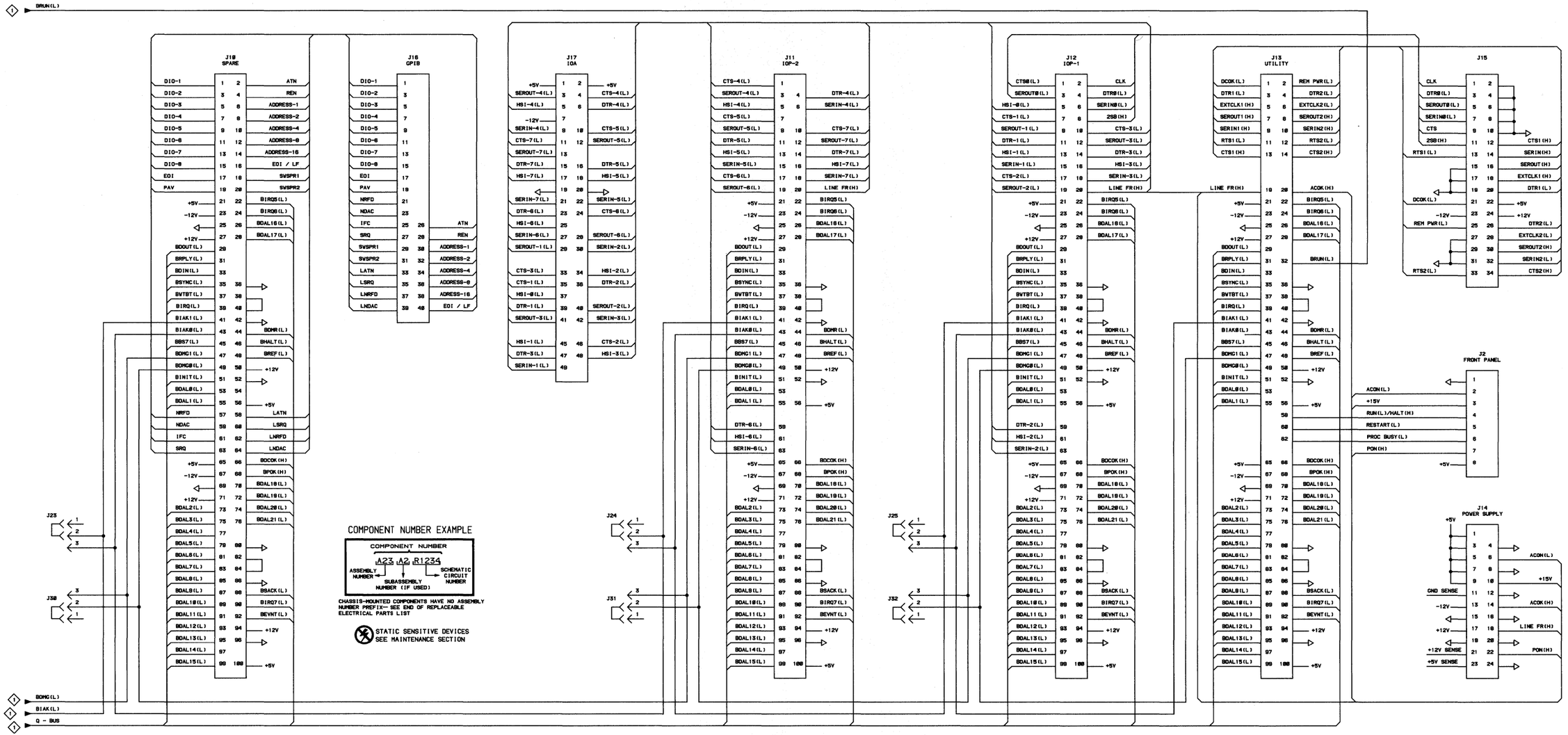
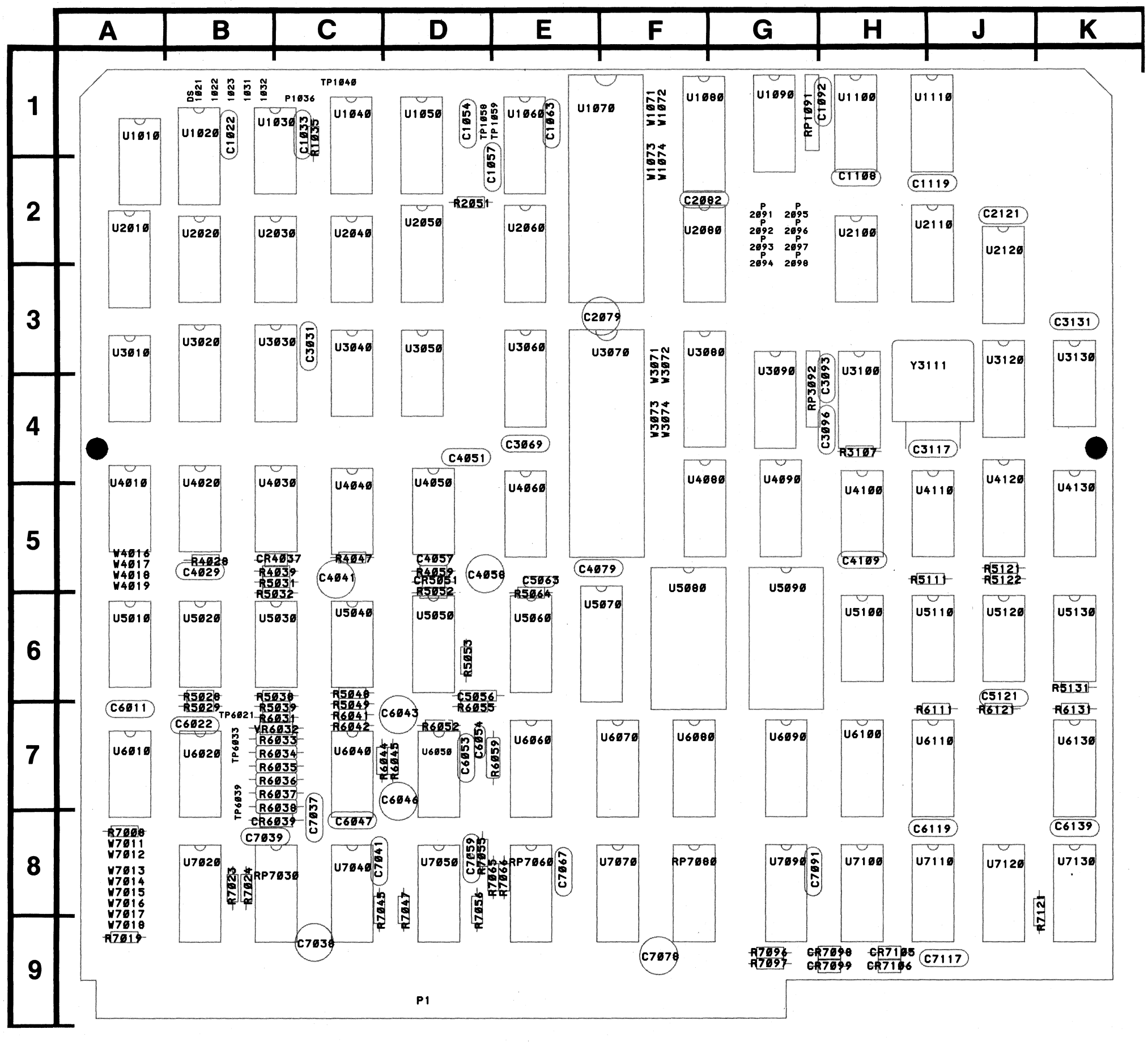
Table 21-1
IC Pin Information

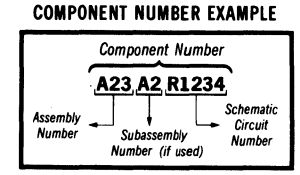
Device	VCC	GND	Device	VCC	GND	Device	VCC	GND
26LS30	1	8	74LS86	14	7	74LS273	20	10
26LS32	16	8	74LS11	14	7	74LS275	20	10
4024	14	7	74LS123	16	8	74LS279	16	8
4044	14	7	74LS130	16	8	74LS367	16	8
4116	9	16	74LS138	16	8	74LS373	20	10
4118	24	12	74S139(LS)	16	8	74LS374	20	10
4702	16	8	74148	16	8	74LS393	14	7
74S00(LS)	14	7	74LS151	16	8	8094	14	7
74S02(LS)	14	7	74LS153	16	8	8136	16	8
74S04(LS)	14	7	74LS155	16	8	8237-2	31	20
7406	14	7	74LS157	16	8	8272	40	20
74S08(LS)	14	7	74LS163	16	8	8837	16	8
74LS10	14	7	74LS174	16	8	8838	16	8
74S11(LS)	14	7	74LS175	16	8	9602	16	8
74LS14	14	7	74LS191	16	8	AM2908	20	5,16
7416	14	7	74LS221	16	8	AY5-1031A	1	3
74LS20	14	7	74S241	20	10	D8284A	18	9
74S21(LS)	14	7	74LS244	20	10	HM6116	24	12
74LS27	14	7	74LS245	20	10	MC1458	8	4
74LS30	14	7	74LS251	16	8	MK3881	26	11
74S32(LS)	14	7	74LS253	16	8	MK4118-4	24	12
7438	14	7	74LS255	14	7	MLM339	3	12
74S64	14	7	74LS260	14	7	MM5369	8	2
74LS74	14	7	74LS266	14	7			




BRUN(L)
J18 SPARE
J16 GPIB
J17 IOA
J11 IOP-2
J12 IOP-1
J13 UTILITY
J15
J2 FRONT PANEL
J14 POWER SUPPLY
J23
J24
J25
J38
J31
J32
COMPONENT NUMBER EXAMPLE
COMPONENT NUMBER
A23 A2 R1234
ASSEMBLY NUMBER
SUBASSEMBLY NUMBER (IF USED)
SCHEMATIC CIRCUIT NUMBER
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX— SEE END OF REPLACEABLE ELECTRICAL PARTS LIST
STATIC SENSITIVE DEVICES SEE MAINTENANCE SECTION
BOMG(L)
BIAK(L)
Q - BUS



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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Figure 21-2. A20 Utility Board.

P/O P1
11 RTS1(L)
3 RDY1(L)
9 SER-IN-1(L)
5 EXT CLK1(H)
P/O MAIN INT. BD.

W4017 W4016
U6020E 74LS04
U4010C 74LS32
U6020F 74LS04
U6010D 74LS02
U6010C 74LS02
W7012 W7011 W7014 W7013
R7008 100

RTS1(H) 5
LINE-PTR-1(H) 9
RDY1(H)
TERMSTAT1(H)
RDAV1-EN(H)
NCTS-1(H)
P/O P1
CTS-1(H) 13

U4020A 74LS74
U5020A 74LS74
U3050A 74LS04
5 LD-RCSR-1(L)

Static Sensitive Devices
See Maintenance Section

U3130D 74LS04
U5100A 74LS02
U5130E 74LS04
U5010D 74LS08
U5010C 74LS08
U4060C 74LS08
U4050C 74LS27
U3050E 74LS04

SER OUT1(H) 7
P/O MAIN INT. BD.
XRDY1(H) 5
XRDY1-INT(H) 9
RDAV1-INT(H)
RDAV1(H)
PERR1(H) 5
FERR1(H) 5 6
ORERR1(H)
ERR1(H) 5
RDAT1-Ø – RDAT1-7(H)

U3070 AY5-1013A
+5V
W3073 35 NP
W3074 37 NB2
W3071 38 NB1
W3072 39 EPS
TCP RCP TSB 25
TBMT 22
DAV 19
18 RDAV
23 D5
OR 15
FE 14
PE 13
33 DE8
32 DP7
31 DP6
30 DB5
29 DB4
28 DB3
27 DB2
26 DB1
21 XR
20 S1
16 SWE
4 RDE
RD8 5 RDAT1-7
RD7 6 RDAT1-6
RD6 7 RDAT1-5
RD5 8 RDAT1-4
RD4 9 RDAT1-3
RD3 10 RDAT1-2
RD2 11 RDAT1-1
RD1 12 RDAT1-Ø
-12V

8 RD-RBUF-1(L)
5 LD-XBUF-1(L)
DAL7(H)
DAL6(H)
DAL5(H)
4 DAL4(H)
6 DAL3(H)
7 DAL2(H)
DAL1(H)
DALØ(H)
8 DCOK(L)

RP3092 10K
+5V

U2100B 74LS21
TBMT1-EN(H) 9 5
XBREAK1(H)
PBR1-EN(H)
PBRSEL1-3(H)
PBRSEL1-2(H)
PBRSEL1-1(H)
PBRSEL1-Ø(H)

U3080 74LS273
4 2D 2Q 5
8 4D 4Q 9
7 3D 3Q 6
13 5D 5Q 12
14 6D 6Q 15
17 7D 7Q 16
18 8D 8Q 19
CL 1 11

U3090 74LS157
SEL 1
P2095
P2096
P2097
P2098
11 3A
5 2A
14 4A
2 1A
10 3B
6 2B
13 4B
3 1B
9 3Y
7 2Y
12 4Y
4 1Y
STB 15

U3100 4702
11 S3
12 S2
13 S1
14 SØ
5 CP
15 1M
2 Ox
6
Ix 7
10
C3096 56pF
R3107 10M
Y3111
C3117 56pF
9 2.4576MHz 4

7 DAL15(H)
DAL14(H)
DAL13(H)
DAL12(H)

8 INIT(L)

R7096 100
+5V
CR7098
CR7099

R5028 1K +5V

5 LD-XCSR-1(L)
U3130B 74LS04

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

COMPONENT NUMBER EXAMPLE

Component Number
A23, A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O P1 — 12 — RTS2(L)

4 — RDY2(L)

W4019 W4018

U6020A 74LS04 — RTS2(H) → 5

U4010B 74LS32 — LINE-PTR-2(L) → 9

U6020B 74LS04 — RDY2(H)

U6010A 74LS02 — TERMSTAT2(H), RDAV2-EN(H), NCTS-2(H)

P/O P1 — CTS-2(H) → 14

U6010B 74LS02 — R7019 100; W7015, W7016, W7018, W7017

U4020B 74LS74

U3050B 74LS04 — 5 LD-RCSR-2(L)

U5020B 74LS74

U3130E 74LS04

U5100D 74LS02

U3130F 74LS04 — SER OUT2(L) → 8; XRDY2(H) → 5

U5010A 74LS08

U5010B 74LS08 — XRDY2-INT(H) → 9; RDAV2-INT(H), RDAV(H) → 5; PERR2(H), FERR2(H) → 8; ORERR2(H), ERR2(H) → 5

U4060D 74LS08

U4050B 74LS27

U3050C 74LS04 — RDAT2-Ø–RDAT2-7(H)

P/O MAIN INT. BD. — SER OUT2(L) → 8

Static Sensitive Devices *See Maintenance Section*

U1070 AY5-1013A — +5V; W1073, W1074, W1071, W1072; TCP, RCP, TSB, NP, NB2, NB1, EPS, TBMT, DAV, RDAV, DS, OR, FE, PE, DE8, DP7, DP6, DB5, DB4, DB3, DB2, DB1, XR, SI, RD8–RD1, SWE, RDE; -12V

RD-RBUF-2(L) → 5

LD-XBUF-2(L) → 5

DAL7(H), DAL6(H), DAL5(H), DAL4(H), DAL3(H), DAL2(H), DAL1(H), DALØ(H) → 7

DCOK(L) → 8

SER-IN-2(L) → 10

RDAT2-7 … RDAT2-Ø

RP1091,2 10K — +5V

U2100A 74LS21 — TBMT2-EN(H) → 5 9; XBREAK2(H), PBR2-EN(H), PBRSEL2-3(H), PBRSEL2-2(H), PBRSEL2-1(H), PBRSEL2-Ø(H) → 5

U1080 74LS273 — 2D 2Q, 4D 4Q, 3D 3Q, 5D 5Q, 6D 6Q, 7D 7Q, 8D 8Q, CL

U1090 74LS157 — SEL; P2094, P2093, P2092, P2091; 3A, 2A, 4A, 1A, 3B, 2B, 4B, 1B STB; 3Y, 2Y, 4Y, 1Y

U1100 4702 — S3, S2, S1, SØ, ECP, CP, 1M

DAL15(H), DAL14(H), DAL13(H), DAL12(H) → 7

2.4576MHz → 3

INIT(L) → 8

EXT CLK2(H) → 6

R7097 100 — +5V — CR7105, CR7106

U3130C 74LS04 — LD-XCSR-2(L) → 5

R5028 1K — +5V

P/O MAIN INT. BD.

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234 — Assembly Number; Subassembly Number (if used); Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

SELECTED OUTPUT DATA

READ/WRITE STROBE

RDY2(H) ORERR2(H) RDY1(H) ORERR1(H) RTS2(H) FERR2(H) RTS1(H) FERR1(H) PERR2(H) PERR1(H) DIN(H) LTC(H)

TDØ(H)-TD7(H), TD12(H)-TD15(H)

PBRSEL2,0-3(H)
PBRSEL1,0-3(H)

U1110 74LS251 — PBRSEL 2-3(H) — PBRSEL1-3 — ERR1(H) TERMSTAT1(H) ERR2(H) TERMSTAT2(H) — TD15(H)
U2110 74LS251 — PBRSEL 2-2(H) — PBRSEL1-2 — TD14(H)
U4090 74LS251 — PBRSEL 2-1(H) — PBRSEL1-1 — TD13(H)
U4080 74LS251 — PBRSEL2-Ø — PBRSEL1-Ø — TD12(H)

PBR2-EN(H)
PBR1-EN(H)
TBMT1-EN(H)
RDAV1-EN(H)
TBMT2-EN(H)
RDAV2-EN(H)

U5120D 74LSØØ — TP1040 — RD-LTCR(L)
U5130B 74LSØ4
U5120A 74LSØØ — LD-LTCR(L)

U2050 74LS251 — XRDY1(H) RDAV1(H) XRDY2(H) RDAV2(H) — RDAT2-7(H) RDAT1-7(H) — TD7(H)
U1060 74LS251 — RDAT2-6(H) RDAT1-6(H) — TD6(H)
U1050 74LS251 — RDAT2-5(H) RDAT1-5(H) — TD5(H)

U1040D 8097
U1040E 8097
U1040F 8097

U3120 74LS155 — RD-RBUF-1(L) LD-XBUF-1(L) LD-XCSR-1(L) LD-RCSR-1(L)

LTC-EN(H)
HI-ROM(H)

1V2(H)
2V2(H)
RDAT2-Ø-RDAT2-7(H)
RDAT1-Ø-RDAT1-7(H)

P1036 +5V — R1035 10K — U1040C 8097 — TDØ(H)

U2120 74148 — SEL C(L) SEL B(L) SEL A(L) — MUXEN(L)

U3060 74LS253 — RDAT1-4(H) RDAT2-4(H) RDAT1-3(H) RDAT2-3(H) — TD4(H) TD3(H)
U2060 74LS253 — 1V2(H) RDAT1-2(H) 2V2(H) RDAT2-2(H) RDAT1-1(H) RDAT2-1(H) — TD2(H) TD1(H)
U2080 74LS251 — RDAT1-Ø(H) RDAT2-Ø(H) — TDØ(H)

R5028 1K +5V
R2051 10K +5V

U4120 74LS155 — RD-RBUF-2(L) LD-XBUF-2(L) LD-XCSR-2(L) LD-RCSR-2(L)

NCTS-1(H)
XBREAK1(H)
NCTS-2(H)
XBREAK2(H)
VEC-1(L)
VEC-2(L)
LA2(H)
LA1(H)
DOUT(H)
SER1(L)
SER2(L)

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

Static Sensitive Devices *See Maintenance Section*

P/O A20 UTILITY BOARD

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SYNC(H)
DAL1(H) - DAL12(H)
BS7(H)
LD-LTCR(L)

R6131 1K +5V
U5130D 74LS04
R5122 2.2K +5V

SER-2(L)
SER2(L)
LTC(H)
LTC(L)

U5110F 74LS04

U5130C 74LS04

U5070 74LS373
DAL7(H) DAL6(H) DAL5(H) DAL4(H) DAL3(H) DAL2(H) DAL1(H)
A6(H) A5(H) A4(H) A3(H) A2(H) A1(H) AØ(H)

U5080 2732
TD6(H) TD5(H) TD4(H) TD3(H) TD2(H) TD1(H) TDØ(H) TD7(H)

U5100C 74LS02

U7100 74LS133
DAL7(H) DAL3(H)

U5110 74LS04

U7120 74145
DAL1(H) DAL2(H) DAL5(H) DAL4(H)
R7121 1K +5V

U4130A 74LS74
DAL8(H)

LA2(H)
LA1(H)
H1-ROM(H)

U5090 2732
TD14(H) TD13(H) TD12(H) TD11(H) TD10(H) TD9(H) TD8(H) TD15(H)

U7130 8136
DAL8(H) DAL7(H) DAL6(H) DAL5(H) DAL4(H) DAL3(H)

U6130 8136
DAL12(H) DAL11(H) DAL10(H) DAL9(H) BS7(H)

U7110 8136
DAL8(H) DAL7(H) DAL6(H) DAL5(H) DAL4(H) DAL3(H)

U6110 8136
DAL12(H) DAL11(H) DAL10(H) DAL9(H) BS7(H)

U7130 / U6130 / U7110 / U6110 common:
T1 T6 T2 T5 T3 B4 B1 B6 B2 B5 B3 T4
STB
OUT

U5130B 74LS74
DAL11(H)

U6100 8136
BS7(H) DAL9(H) DAL10(H) DAL12(H) DAL11(H)
T5 T1 T3 T4 T2 T6 B5 B1 B6 B4 B2 B3
STB
OUT

U5110E 74LS04

R5111 1K +5V
U4110A 74LSØØ
RD-ROM(L)

R5028 1K +5V
R5131 1K +5V

U1020 74LS174
DAL5(H) DAL11(H) DAL12(H) DAL13(H) DAL14(H) DAL15(H)
CLR
DS1032 DS1031 DS1023 DS1022 DS1021
TP1058 TP1059

U3050D 74LS04

U1030A 74LS74
DAL6(H)

U1030B 74LS74
DAL7(H)

C6054 1000pF
U6040A 74LS14
U1010D 74LS08
EVENT(H)
LTC-EN(H)

R6111 1K +5V
U5110D 74LS04
R5121 2.2K +5V
SER-1(L)
SER1(L)

TDØ(H)-TDI5(H)

P/O P1 19
INIT(L)
LINE FR(H)
DIN(H)
P/O MAIN INT. BD.

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234
Assembly Number / Subassembly Number (if used) / Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O MAIN INT. B.D.

BUS DRIVER/RECEIVERS

BIAKI(L) BDOUT(L) BBST(L) BSINC(L) BDIN(L) BWTBT(L)

BDMGO(L) VECTOR(L) BDMGI(L) BRPLY(L) BEVNT(L) BIRQ(L) P/O P1

IRQ(H) EVENT(H)

LTC(H)
MUXEN(L)
RD-LTCR(L)
TDØ-TD15(H)

U4100A 74LSIØ
U5130F 74LS04
U7090 8838
RP7080 180
RP7080 390
U5040 7406
R6059 10.2K
R5053 100
U6050F 74LS14
C5056 82PF
U7040 8837
RP7030 390
R7066 330
RP7030 180
R7045 680

P/O P1
BDAL15(L)
BDAL14(L)
BDAL13(L)
BDAL12(L)

LTC(L)
SER-1(L)
SER-2(L)
RD-ROM(L)
SEL A(L)

U4100B 74LSIØ
U5130A 74LS04
U4110C 74LSØØ
U6090 8838
U4110D 74LSØØ
U6050E 74LS14
U7070 8838
U6080 8838

BDAL11(L)
BDAL10(L)
BDAL 9(L)
BDAL 8(L)
BDAL 3(L)
BDAL 2(L)
BDAL 1(L)
BDAL 4(L)
BDAL 7(L)
BDAL 6(L)
BDAL 5(L)
BDALØ(L)

P/O MAIN INT. BD.

RP7060 180
RP7060 390
RP7030 180
R7056 330
RP7055 680
U5120C 74LSØØ
U4100C 74LSIØ
U5120B 74LSØØ
U6070 8838
U5040D 7406
R4047 1K
RPLY(H)
DMGI(L)
DIN(H)
SYNC(H)
IAKI(H)
BST(H)
DOUT(H)

BUS TERMINATIONS
BIRQ 5(L)
BIRQ 6(L)
BDAL17(L)
BDAL16(L)
BREF (L)
BIRQ 7(L)
BSACK(L)

P/O MAIN INT. BD.

DAL 12(H), DALØ(H)-DAL 7(H)
DAL13(H)-DAL15(H)

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O A20 UTILITY BOARD

8560/8561/8562 SERVICE

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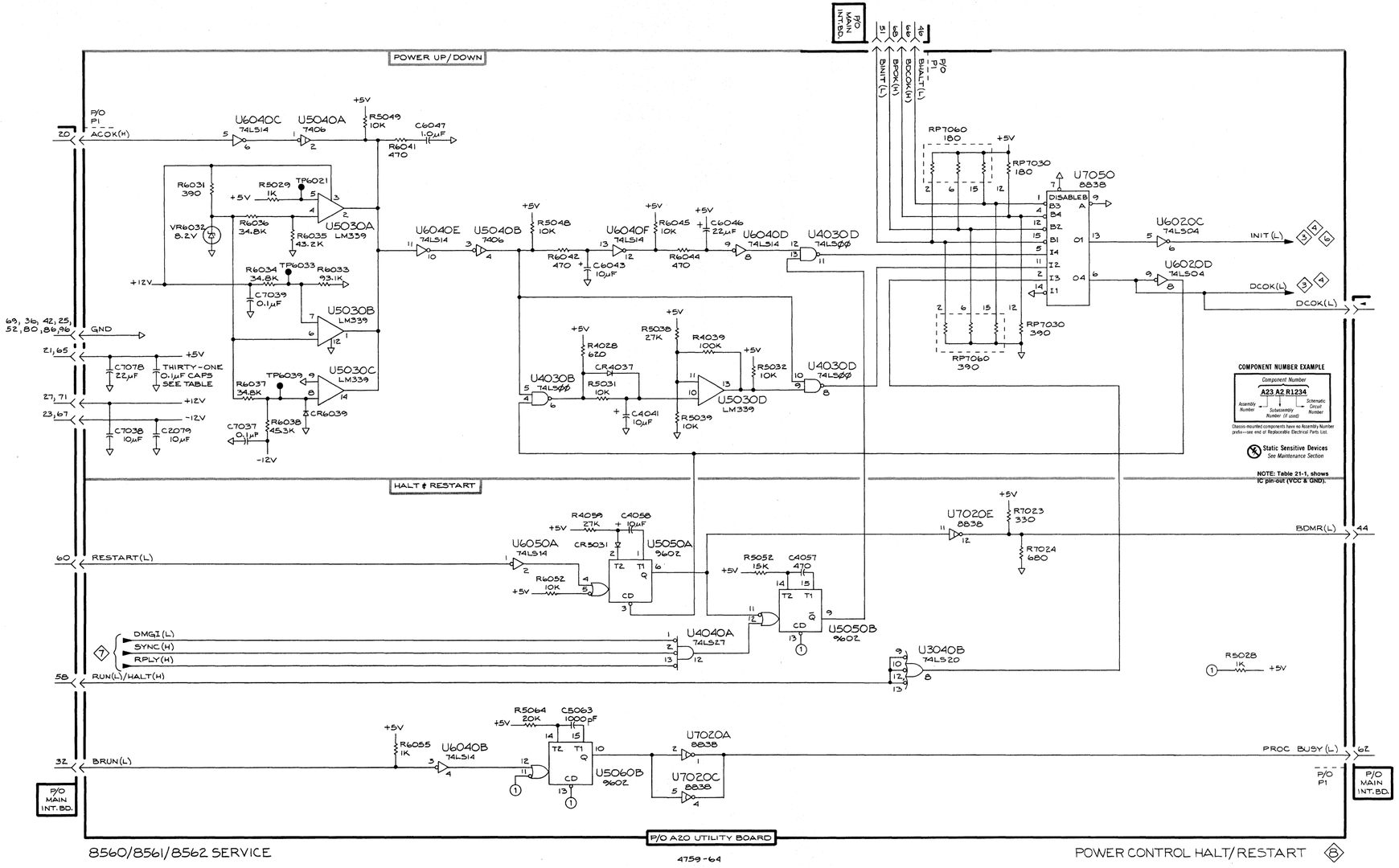
8560 BUS CONTROL 7

UTILITY BOARD 8560
BUS CONTROL

7

Table 21-2
Thirty-One 0.1μF
Decoupling Capacitors

C1022	C4079
C1033	C4109
C1054	C5119
C1057	C6011
C1063	C6022
C1092	C6053
C1108	C6139
C1119	C7037
C2082	C7039
C2121	C7041
C3031	C7059
C3069	C7067
C3093	C7091
C3131	C7092
C4029	C7117
C4051	



U2030A 74LS74
U2040D 74LSØØ
U3040A 74LS20
U2030B 74LS74
U2040C 74LSØØ
U3030 74LS175
U3020 74148
U2010 74LS139
U2020A 74LS74
U2040A 74LSØØ
U2020B 74LS74
U2040B 74LSØØ
U1010B 74LS08
U7020F 8838
U3010A 74LSØØ
U3050F 74LS04
U4060 74LS08
U3010B 74LSØØ
U4010A 74LS32
R5028 1K
R7065 330 P/O P1
R7047 680

RDAV1-INT(H)
XRDY1-INT(H)
TBMT1-EN(H)
IAK1(H)
DIN(H)
RDAV2-INT(H)
LINE-PTR1(H)
LINE-PTR2(H)
XRDY2-INT(H)
TBMT2-EN(H)

IRQ(H)
BIAKØ(L)
VECTOR(L)
1V2(H)
2V2(H)
VEC-2(L)
VEC-1(L)
+5V

P/O MAIN INT.BD.

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number; Subassembly Number (if used); Schematic Circuit Number

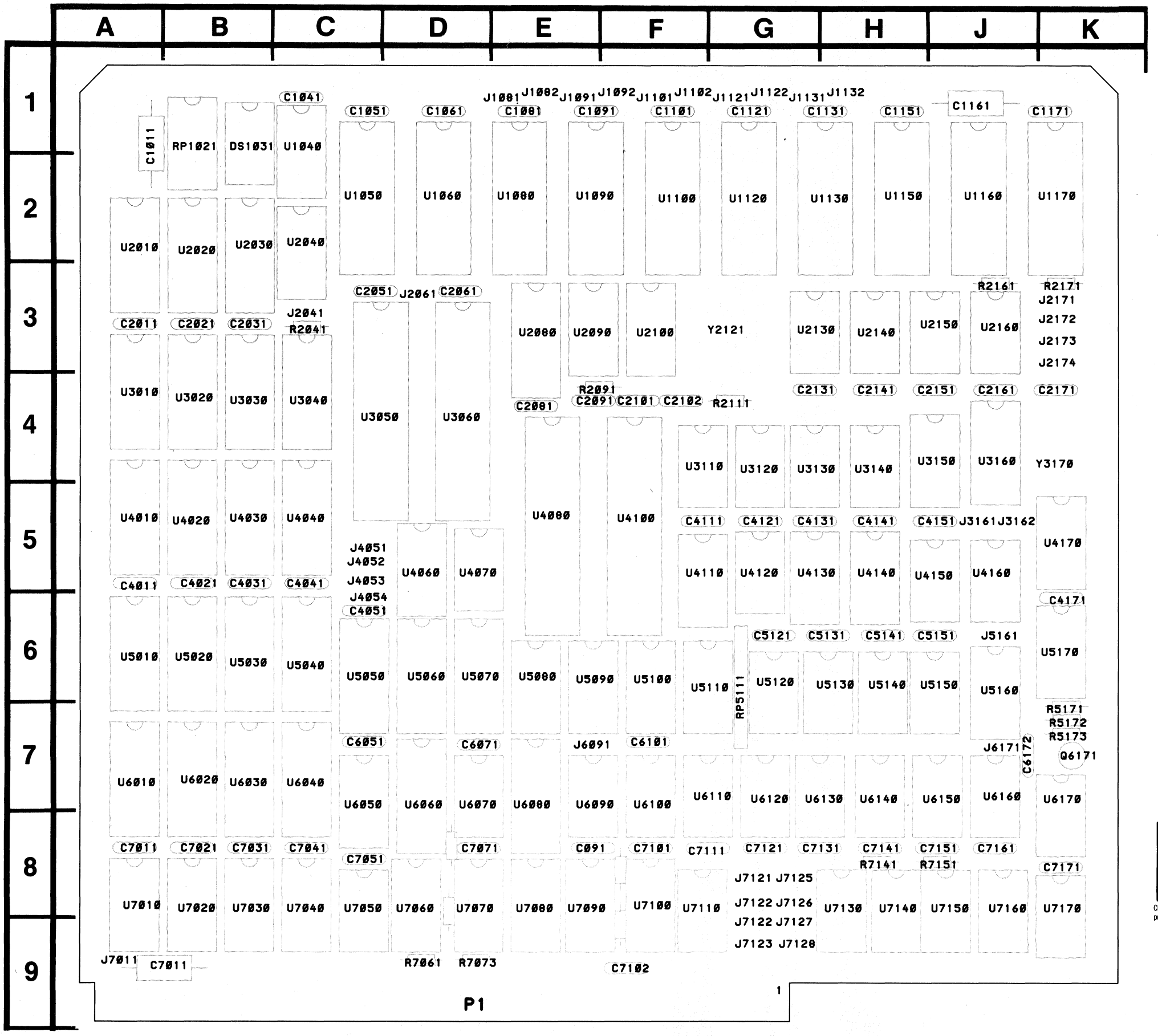
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

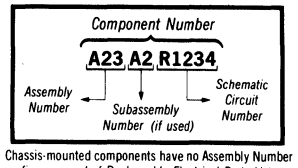
NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A20 UTILITY BOARD

I/O PROCESSOR
COMPONENT LOCATIONS



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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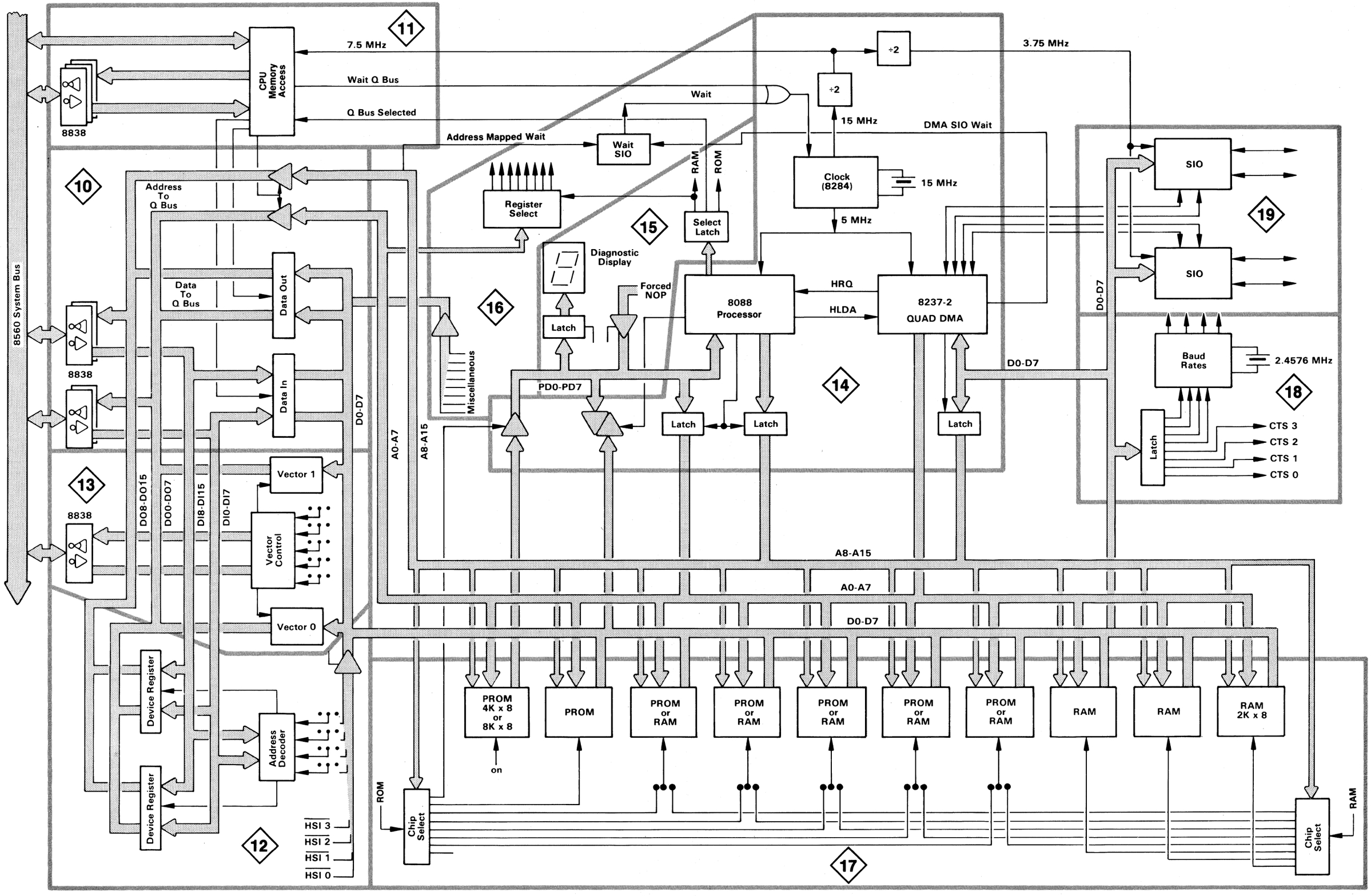
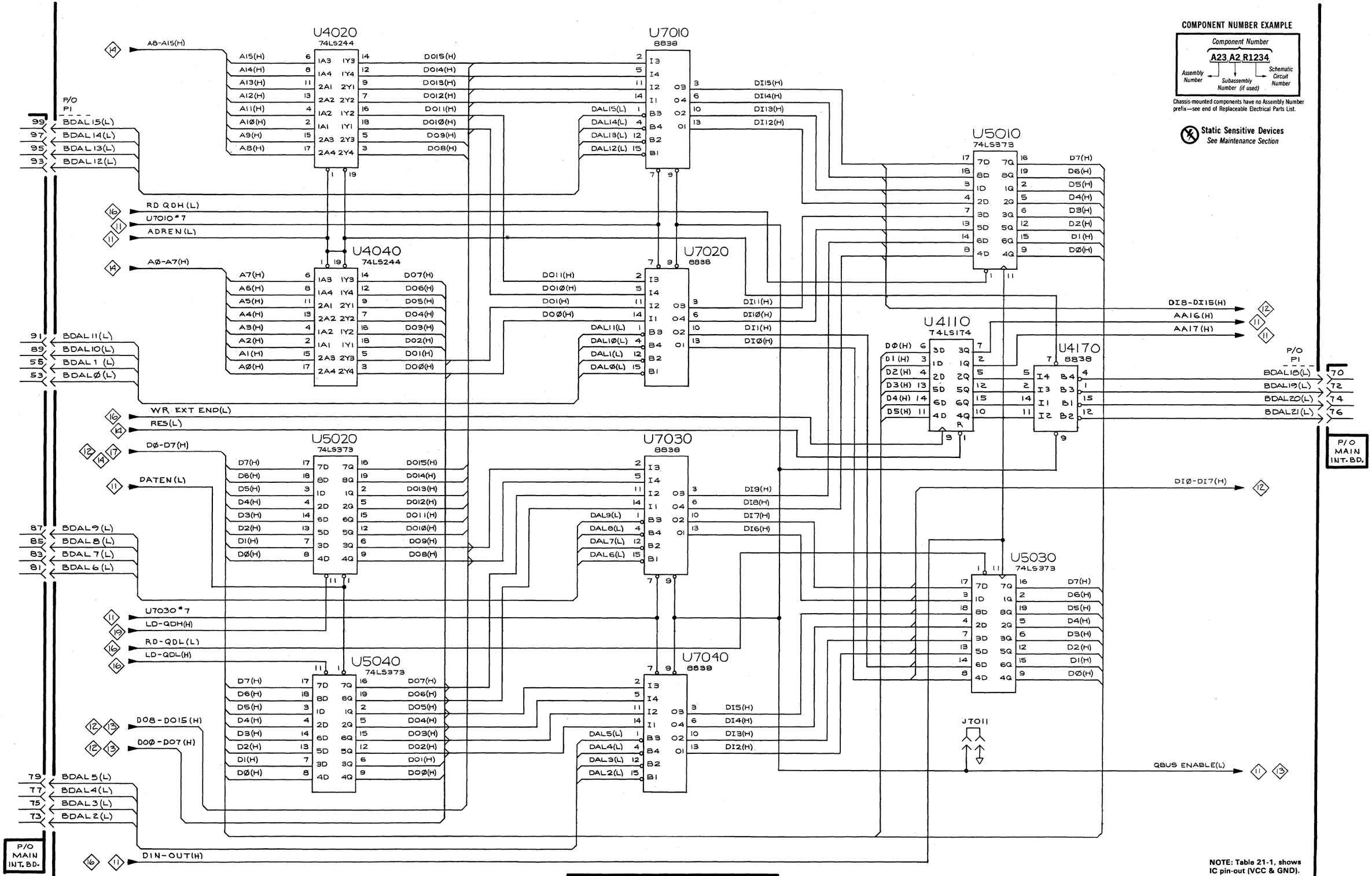
Figure 21-3. A30 I/O Processor Board.


8560 System Bus
11
CPU Memory Access
7.5 MHz
Wait Q Bus
Q Bus Selected
8838
Address Mapped Wait
Wait SIO
Wait
÷2
÷2
3.75 MHz
15 MHz
DMA SIO Wait
10
Address To Q Bus
Register Select
RAM
ROM
Clock (8284)
15 MHz
5 MHz
15
Select Latch
Diagnostic Display
Data To Q Bus
Data Out
Data In
8838
16
Latch
Forced NOP
8088 Processor
HRQ
HLDA
8237-2 QUAD DMA
SIO
SIO
19
D0-D7
Miscellaneous
PD0-PD7
14
Latch
Latch
Latch
D0-D7
Baud Rates
2.4576 MHz
18
Latch
CTS 3
CTS 2
CTS 1
CTS 0
A8-A15
A0-A7
13
8838
DO8-DO15
DO0-DO7
DI8-DI15
DI0-DI7
Vector 1
Vector Control
Vector 0
A8-A15
A0-A7
D0-D7
Device Register
Device Register
Address Decoder
PROM 4K x 8 or 8K x 8
PROM
PROM or RAM
PROM or RAM
PROM or RAM
PROM or RAM
PROM or RAM
RAM
RAM
RAM 2K x 8
on
ROM
Chip Select
12
HSI 3
HSI 2
HSI 1
HSI 0
17
Chip Select
RAM



P/O A30 10 PROCESSOR BOARD

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O P1
88 SACK(L)
35 SYNC(L)
14 RES(L)
14 AØ
15 QBUS(L)
14 5MHZ(H)
7.5 MHZ(H)
15 RD + WR(L)
33 DIN(L) DIN(L)
29 DOUT(L) DOUT(L)
12 RPLY(L)
16 BYTE(H)
31 RPLY(L)
10 DIN-OUT(H)
51 INIT(L)
10 DATEN(L)
12 RD-REG(H)
13 VECTOR(L)
14 D-T/R(H)
14 A18(H)
10 AA17(H)
10 AA16(H)
37 WTBT(L)
45 BS7(L)
28 BA17(L)
26 BA16(L)
10 QBUS ENABLE(L)

P/O MAIN INT. BD.

U6150B 74LSØ8
U5150B 74LSØ2
U7140B 74LS27
U5150C 74LSØ2
U7160B 74LSØØ
U6150D 74LSØ4
U7160C 74LSØØ
U6090 74LS74
U3140F 74LS04
U7160A 74LSØØ
U6160B 74LS04
J6091
J6171
U6080 DEC DC010
INIT
RPLY
REQ
DMR
DMGI
DMGØ
MASTER
SYNC
DIN
DOUT
QBUS DMA
CNT4
DATIO
DATIN
RSYNC
ADREN
DATEN
+5V
R7072 330
R7071 330
R7073 680
R7061 680
U6170A 74LS393
U6170B 74LS393
U6140A
U5140A 74LSØØ
U5130B 74LS32
U5140B 74LSØØ
SET QBUS ERROR(L)
WAIT QBUS(H)
P/O P1
DMR(L) 44
DMGI(L) 47
DMGO(L) 49
P/O MAIN INT. BD
U7080 8838
DOUT(H)
DIN(H)
SYNC(H)
U7150A 74LSØØ
U7090 8838
U7130A 74LSØ8
INIT(H)
U6140B 74LS14
U7140A 74LS27
U7130D 74LSØ8
P7 U7010
P7 U7030
U7070 8838
BA16(H)
BS7(H)
U6140C 74LS14
ADREN(H)

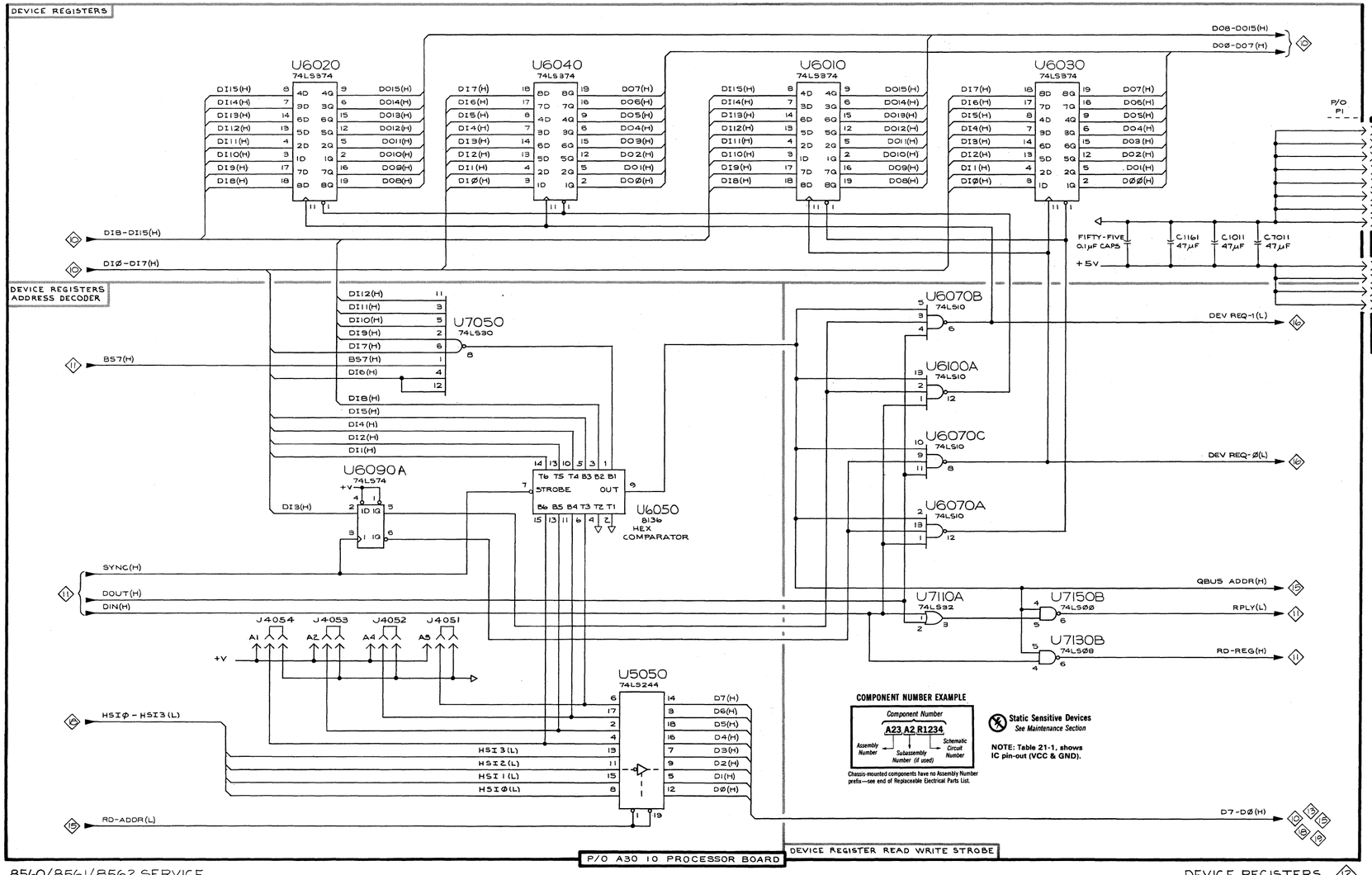
NOTE: Table 21-1, shows IC pin-out (VCC & GND).

Static Sensitive Devices
See Maintenance Section

P/O A30 10 PROCESSOR BOARD

Table 21-3
Fifty-Four 0.1μF
Decoupling Capacitors

C1041	C4111
C1051	C4121
C1061	C4131
C1081	C4141
C1091	C4151
C1101	C4171
C1121	C5121
C1131	C5131
C1151	C5141
C1171	C5151
C2011	C6051
C2021	C6071
C2031	C6101
C2051	C7011
C2061	C7021
C2081	C7031
C2091	C7041
C2131	C7051
C2141	C7071
C2151	C7091
C2161	C7101
C2171	C7111
C4011	C7121
C4021	C7131
C4031	C7141
C4041	C7151
C4051	C7161



P/O P1

39 IRQ-4(L)
22 IRQ-5(L)
24 IRQ-6(L)
43 IAKO(L)

R7101 330 +5V
R7102 330

+V

U6110B 74LS74
U6110A 74LS74

J7127 J7128 J7123 J7124

U7110D 74LS32
U7110B 74LS32
U7110C 74LS32

U7100 8838

IRQ-1(H)
IRQ-Q(H) 16

QBUS ENABLE(L) 10

J7121 J7122 J7125 J7126

U6140D 74LS14

90 IRQ-7(L)

U6120A 74LS27
U6130A 74LS74
U6120C 74LS27
U6150C 74LS08
U6150A 74LS08
U4160C 74LS08
U5140C 74LSØØ
U6100C 74LSIØ
U6120B 74LS27
U6130B 74LS74
U4120B 74LSØ8

VECTOR(L) 11

RES(L) 14
DIN(H) 11
IAKI(L) 41

+5V
R7151 330
R7141 680
U6140F 74LS14

U4010 74LS374
U4030 74LS374

D7(H) D6(H) D5(H) D4(H) D3(H) D2(H) D1(H) DØ(H)
D09(H) D08(H) D07(H) D06(H) D05(H) D04(H) D03(H) D02(H)

P/O MAIN INT. BD

WR-VECI(L) 16
WR-VECØ(L) 16

DØ-D7(H) 10 12 19

D08-D09(H)
D02-D07(H) 10

COMPONENT NUMBER EXAMPLE

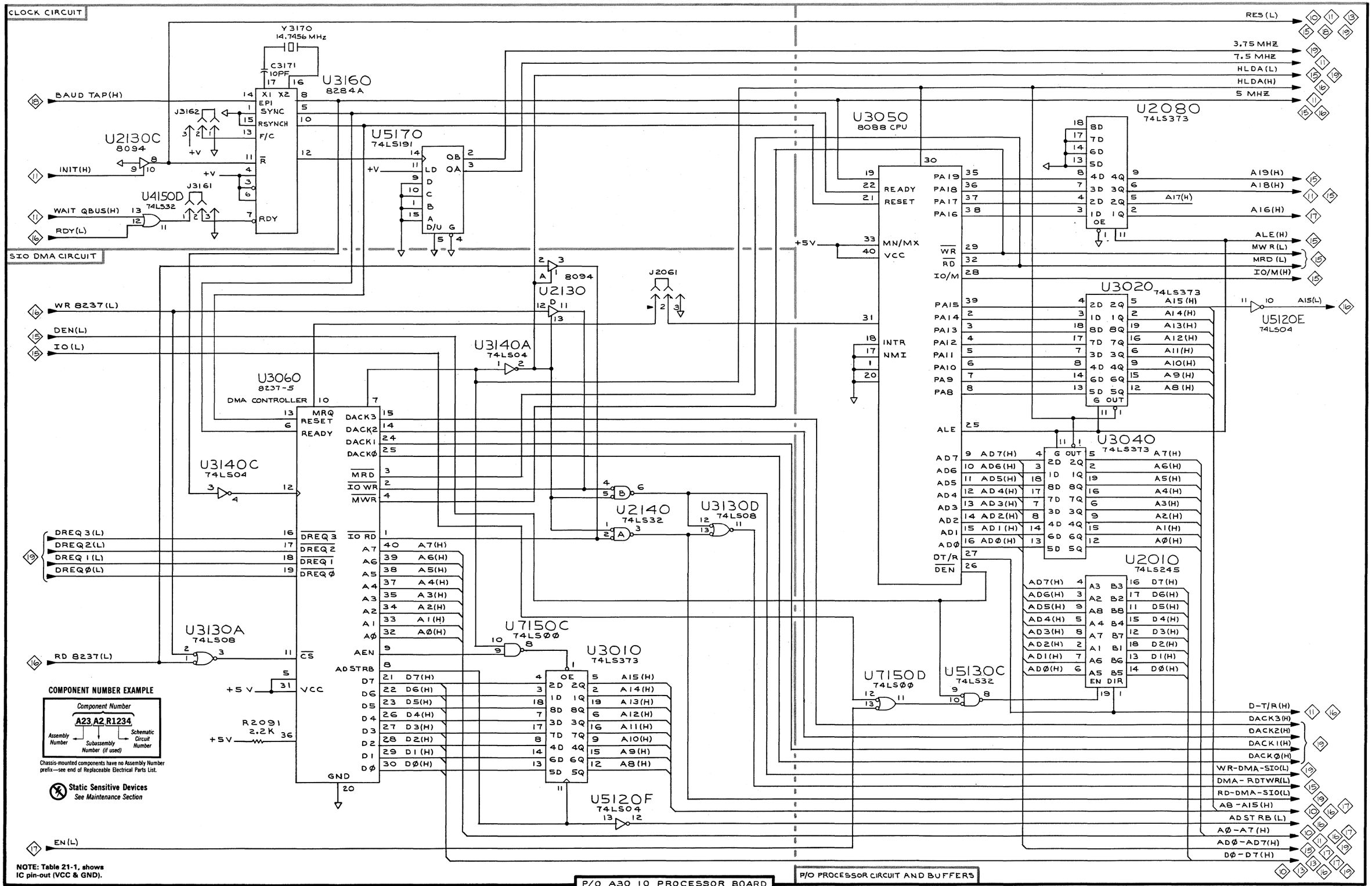
Component Number: A23 A2 R1234
Assembly Number / Subassembly Number (if used) / Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A30 10 PROCESSOR BOARD


CLOCK CIRCUIT
Y3170
14.7456 MHz
C3171
10PF
U3160
8284A
X1 X2
EFI
SYNC
RSYNCH
F/C
R
RDY
J3162
U2130C
8094
J3161
U4150D
74LS32
U5170
74LS191
OB
OA
LD
D
C
B
A
D/U
G
BAUD TAP(H)
INIT(H)
WAIT QBUS(H)
RDY(L)
+V
RES(L)
3.75 MHZ
7.5 MHZ
HLDA(L)
HLDA(H)
5 MHZ
U3050
8088 CPU
READY
RESET
MN/MX
VCC
INTR
NMI
PA19
PA18
PA17
PA16
PA15
PA14
PA13
PA12
PA11
PA10
PA9
PA8
ALE
WR
RD
IO/M
U2080
74LS373
A19(H)
A18(H)
A17(H)
A16(H)
ALE(H)
MWR(L)
MRD(L)
IO/M(H)
U3020
74LS373
A15(H)
A14(H)
A13(H)
A12(H)
A11(H)
A10(H)
A9(H)
A8(H)
U5120E
74LS04
A15(L)
U3040
74LS373
A7(H)
A6(H)
A5(H)
A4(H)
A3(H)
A2(H)
A1(H)
AØ(H)
U2010
74LS245
D7(H)
D6(H)
D5(H)
D4(H)
D3(H)
D2(H)
D1(H)
DØ(H)
SIO DMA CIRCUIT
WR 8237(L)
DEN(L)
IO(L)
U2130
8094
J2061
U3140A
74LS04
U3060
8237-5
DMA CONTROLLER
MRQ
RESET
READY
DACK3
DACK2
DACK1
DACKØ
MRD
IOWR
MWR
IO RD
AEN
ADSTRB
CS
VCC
GND
U3140C
74LS04
U2140
74LS32
U3130D
74LS08
U3130A
74LS08
RD 8237(L)
U7150C
74LS00
U3010
74LS373
U7150D
74LS00
U5130C
74LS32
U5120F
74LS04
DREQ3(L)
DREQ2(L)
DREQ1(L)
DREQØ(L)
R2091
2.2K
+5V
EN(L)
D-T/R(H)
DACK3(H)
DACK2(H)
DACK1(H)
DACKØ(H)
WR-DMA-SIO(L)
DMA-RDTWR(L)
RD-DMA-SIO(L)
A8-A15(H)
ADSTRB(L)
AØ-A7(H)
ADØ-AD7(H)
DØ-D7(H)
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTE: Table 21-1, shows IC pin-out (VCC & GND).
P/O A30 10 PROCESSOR BOARD
P/O PROCESSOR CIRCUIT AND BUFFERS

P/O PROCESSOR CIRCUIT

AIS(H)
HL DA(L)
AI8(H)
ALE(H)
MRD(L)
MRD(L)

U2150C 74LSØ8
U2150B 74LSØ8
U4150C 74LS32
U3150 74LS139
U2150D 74LSØ8
U3140D 74LSØ4
U3140E 74LSØ4

ROM(L)
QBUS(H)
QBUS(L)
MEM(L)
MEM(H)

U2160D 74LS32
U2160C 74LS32
U2160A 74LS32
U2160B 74LS32
U2150A 74LSØ8

WR(L)
RD+WR(L)
RD(L)

U6160D 74SØ4
U4160B 74LSØ8
J5161

IO(L)
IO(H)

DIAGNOSTIC LED DISPLAY

NOP CIRCUIT

R2041 2.2K
+5V
J2041
U3030 74LS244
AD7(H)
AD6(H)
AD5(H)
AD4(H)
AD3(H)
AD2(H)
AD1(H)
ADØ(H)

R2161 2.7K
R2171 2.7K
+5V

IO/M(H)
RES(L)
ADØ-AD7(H)
RD+WR(L)
AI9(H)
J2171
J2172
J2173
J2174
DMA-RD+WR(L)
DEN(L)
5MHZ
STOP(L)
START(L)

U2020 74LS273
RP1021 330Ω
DS1031 +5V

RP5111 2.7K
+5
HSI3(L)
HSI2(L)
HSI1(L)
HSIØ(L)
DEN(L)

HSIØ-HSI3(L)
QBUS ENABLE(L)
QBUS ADDR(H)

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A30 IO PROCESSOR BOARD

MISCELLANEOUS REGISTER

D-T/R(H)
DØ-D7(H)
SET QBUS ERROR(L)
BA16(H)
DIN-OUT(H)
P/O P1
20 LINE FR(H)
IRQ 1(H)
IRQ Ø(H)
DEV REQ 1(L)
DEV REQ Ø(L)

P/O MAIN INT. BD.

U3140C 74LS04
U4070D 74LS32
U4070C 74LS32
U7170A 74LS74
U6160E 74S04
U6160C 74S04
U7140C 74LS27
U6100 74LS10
U4060B 74LS279
U4060C 74LS279
U4060D 74LS279
U4060A 74LS279
U4070B 74LS32
U4070A 74LS32
U6060 74LS244
U7060 2653
U7130C 74LS08
U3150 74S139
C7102 0.001μF

BYTE(H)

MAY NOT BE INSTALLED

WR EXT END(L)
WR-VECØ(L)
WR-VEC1(L)

COMPONENT NUMBER EXAMPLE

Component Number
A23,A2,R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

AØ-A7(H)
WR(L)

I/O REGISTER DECODER STROBES

U4140 74LS138
U4130 74LS138

RD(L)
AI5(L)
QBUS(H)
QBUS(L)
MEM(H)
AI4-AI5(H)
HLDA(H)
ADSTRB(L)
5MHZ

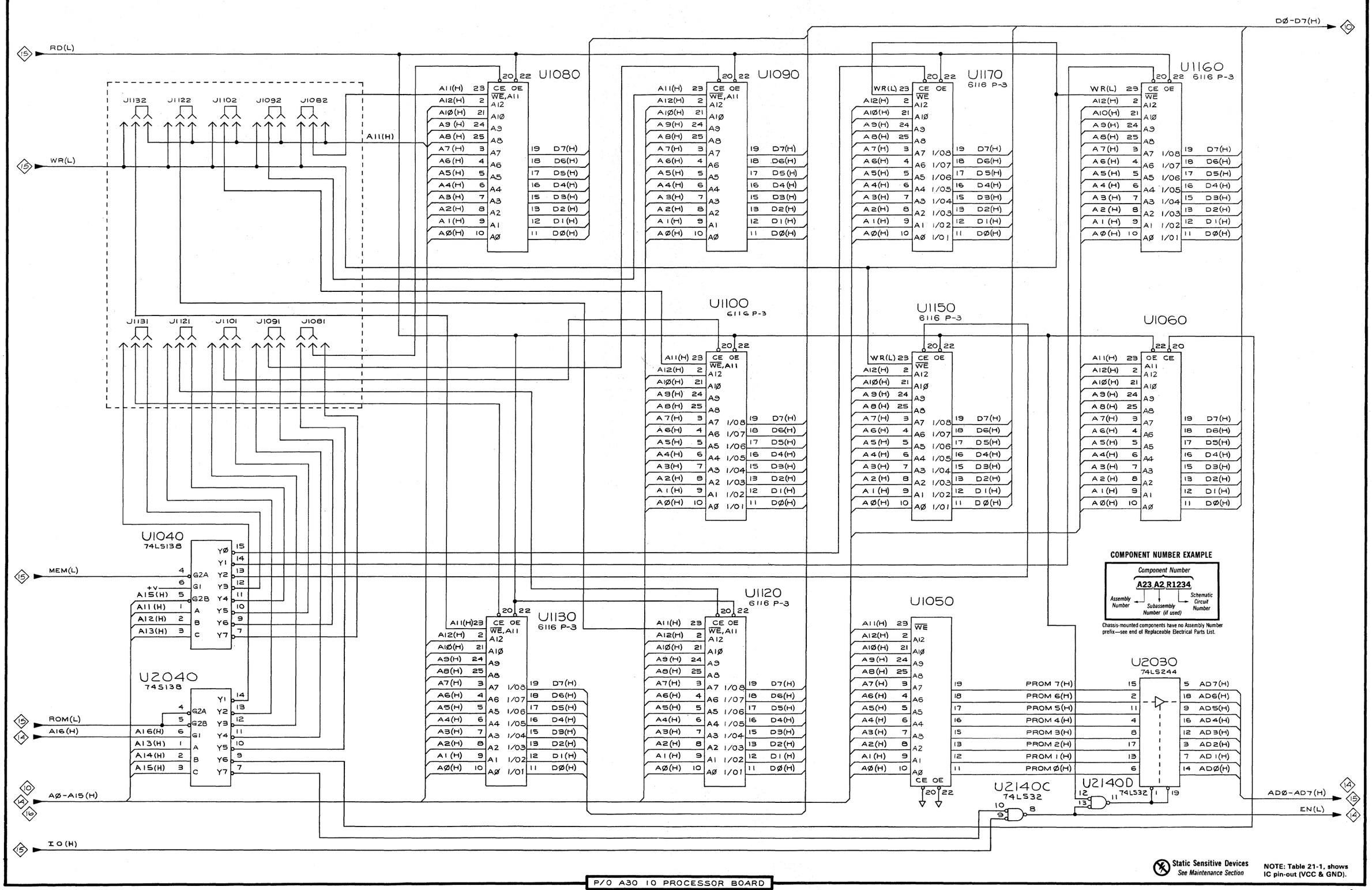
U5140D 74LSØØ
U5130D 74LS32
U4150 74LS32
U5150 74LSØ2
U3120A 74LS11
U5130A 74LS32
U4120C 74LSØ8
U5160 74LS191
U6160A 74SØ4
U4160A 74LS08
U4160D 74LS08

RD-QDH(L)
RD-QDL(L)
LD-QDH(H)
LD-QDL(H)
START(L)
WR-8237(L)
WR-BAUD,CTS(L)
WR-SIOI(L)
WR-SIOØ(L)
RD-ADDR(L)
STOP(L)
RD-8237(L)
RD-BAUD,CTS(L)
RD-SIOI(L)
RD-SIOØ(L)
RDY(L)

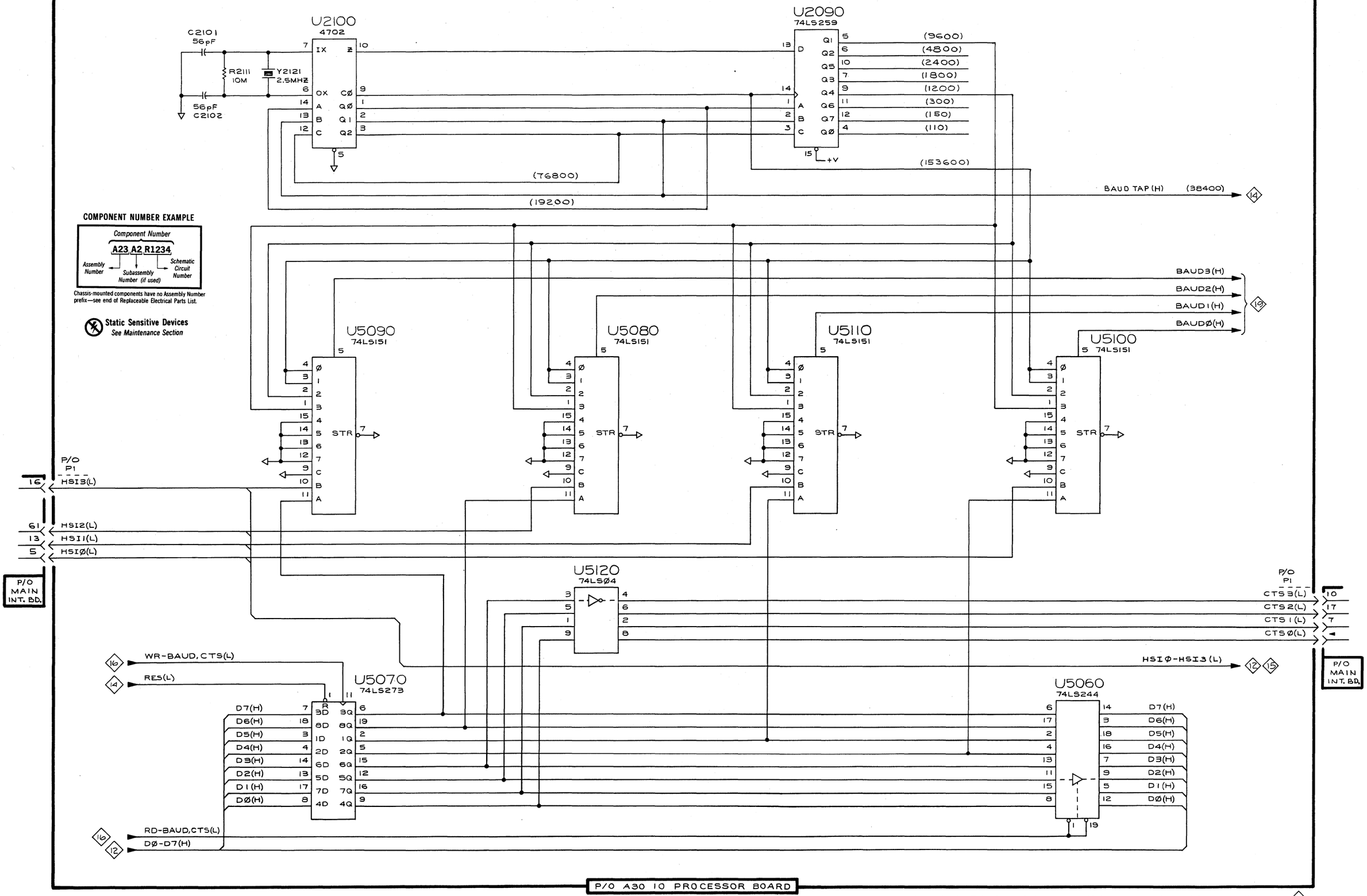
SIO WAIT CIRCUIT

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A30 IO PROCESSOR BOARD



P/O A30 IO PROCESSOR BOARD



COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
- A23 — Assembly Number
- A2 — Subassembly Number (if used)
- R1234 — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

U4080
SIO MK3885

U6160 F
74LSØ4
3.75 MHZ
R5171 1.2K
Q6171
C6172 33 pfd
R5172 220
R5173 22
+5V

P/O P1
18 SER IN 3(H)
14 RFD 3(L)
16 BAUD 3(H)
63 SER IN 2(H)
59 RFD 2(L)
18 BAUD 2(H)
14 A3-A4(H)

U3130B 74LSØ8 — A3(H)
U3130C 74LSØ8 — A4(H)

HLDA(L)
14 DACK 1(H)
DACK Ø(H)
DACK 3(H)
DACK 2(H)

U3110C 74LS32
U3110D 74LS32
U3110A 74LS32
U3110B 74LS32

U4120A 74LSØ8 — 16 RD-SIOI(L)
U4120D 74LSØ8 — 14 RD DMA SIO(L); 15 RD SIO Ø(L)
U3120B 74LS11 — 14 WR DMA SIO(L); 16 WR SIO 1(L)
U3120C 74LS11 — 16 WR SIO Ø(L)

18 BAUD 1(H)
11 RFD 1(H)
15 SER IN 1(H)
14 RES(L)
18 BAUD Ø(H)
4 RFD Ø(H)
6 SER IN Ø(H)

P/O MAIN INT. BD.

U4080			
DØ	40		
D1	1		
D2	39		
D3	2		
D4	38		
D5	3		
D6	37		
D7	4		
+5V	9, 8, 6		
RxDB	28	TxDB	25
CTSB	23	RDY/WAIT	30
RxCB, TxCB	27,26		
RxDA	12	TxDA	15
CTSA	18	RDY	10
RxCA, TxCA	13,14		
RD	32		
IORQ	36		
C/D	33		
B/A	34		
CE	35		
R	21, 31, 22, 19, 20		

P/O P1
25 SER OUT 3(H) → 12
30 DREQ 3(L) → 14
15 SER OUT 2(H) → 19
10 DREQ2 (L) → 14

U4100 MK3885 SIO

U4100			
DØ(H)	40		
D1(H)	1		
D2(H)	39		
D3(H)	2		
D4(H)	38		
D5(H)	3		
D6(H)	37		
D7(H)	4		
B/A	34		
C/D	33		
CE	35		
IORQ	36		
RD	32		
RxCB, TxCB	27,26		
CTSB	23		
RxDB	28	RDY	30
		TxDA	25
+5V	6, 8, 9		
RxCA, TxCA	13,14		
CTSA	18	RDY	10
RxDA	12	TxDA	15
R	21		
	31, 22, 19		
	20		

DREQI(L) → 14; SER OUTI(H) → 9
DREQØ(L) → 14; SER OUTØ(H) → 3

P/O MAIN INT. BD.

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number; Subassembly Number (if used); Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A30 10 PROCESSOR BOARD

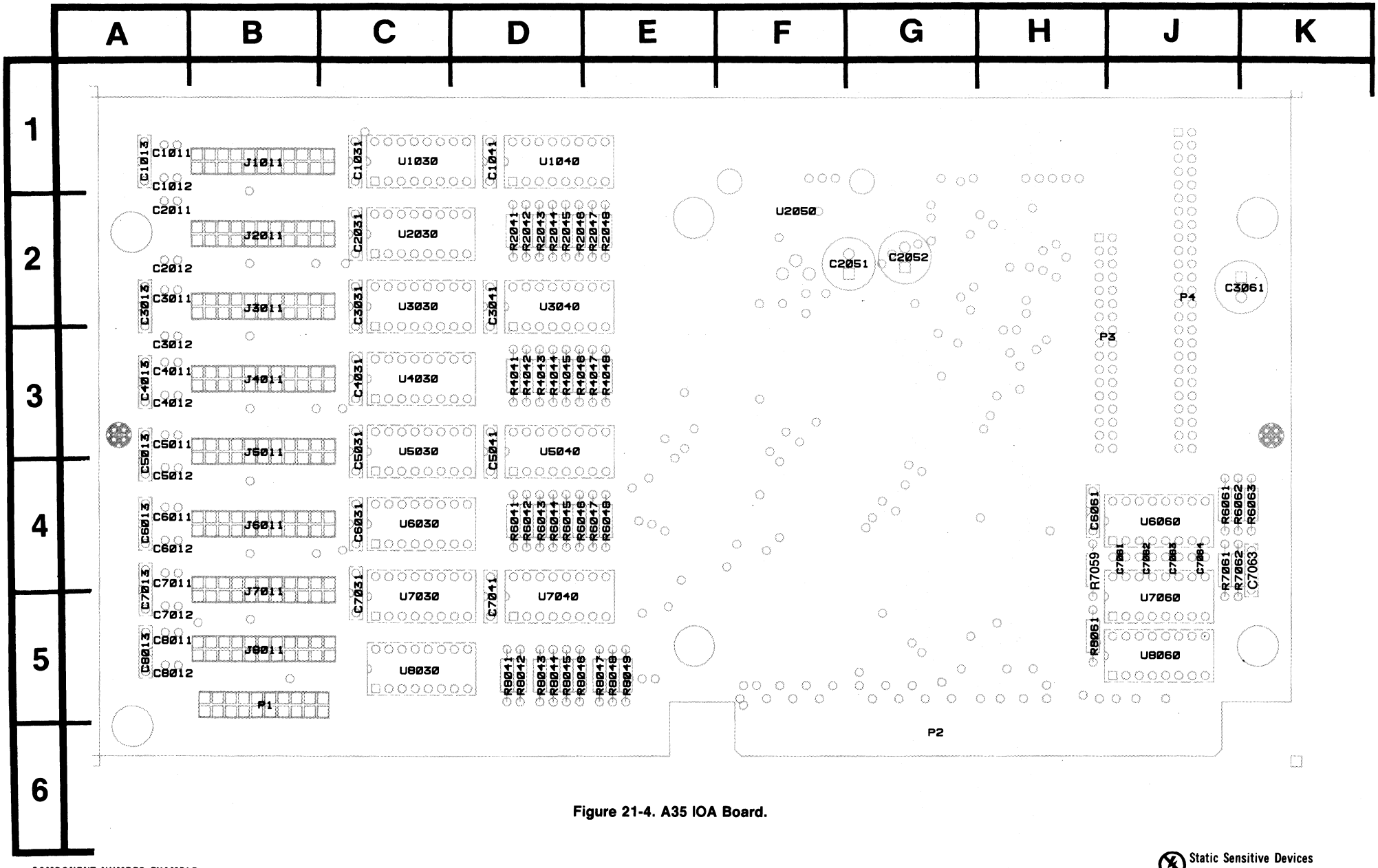
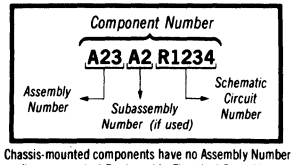


Figure 21-4. A35 IOA Board.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O J17 45 — P/O J4 45 — P/O P4 — HSI 1(L)
P/O J17 39 — P/O J4 39 — P/O P4 — DTR 1(L)
P/O J17 49 — P/O J4 49 — P/O P4 — R DATA 1(L)
P/O J17 29 — P/O J4 29 — P/O P4 — T DATA 1(L)
P/O J17 35 — P/O J4 35 — P/O P4 — CTS 1(L)
P/O J17 34 — P/O J4 34 — P/O P4 — HSI 2(L)
P/O J17 36 — P/O J4 36 — P/O P4 — DTR 2(L)
P/O J17 30 — P/O J4 30 — P/O P4 — R DATA 2(L)
P/O J17 40 — P/O J4 40 — P/O P4 — T DATA 2(L)
P/O J17 46 — P/O J4 46 — P/O P4 — CTS 2(L)

U1040B 26LS32: pins 5, 6, 7
U1040A 26LS32: pins 1, 2, 3, 4 (V1)
U2030 26LS30: pins 1 (+5V), 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15
U3040D 26LS32: pins 13, 14, 15
U3040C 26LS32: pins 9, 10, 11, 12 (V1)
U3030 26LS30: pins 1 (+5V), 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15

R2045 200
R2046 12K — -12V
R2044 200
R2043 12K — -12V
R4042 200
R4041 12K — -12V
R4047 200
R4048 12K — -12V
R8049 1K — +5V — V1

C2011 510pf
C2012 510pf
C3011 510pf
C3012 510pf

J2011: 1–21, 2–22, -5V
J3011: 1–21, 2–22, -5V

P/O P2 — P/O J8001
41, 42, 43, 44, 37, 38, 40, 39, 28, 29, 30, 31, 24, 25, 27, 26

COMPONENT NUMBER EXAMPLE

COMPONENT NUMBER: A23 A2 R1234
- A23: ASSEMBLY NUMBER
- A2: SUBASSEMBLY NUMBER (IF USED)
- R1234: SCHEMATIC CIRCUIT NUMBER

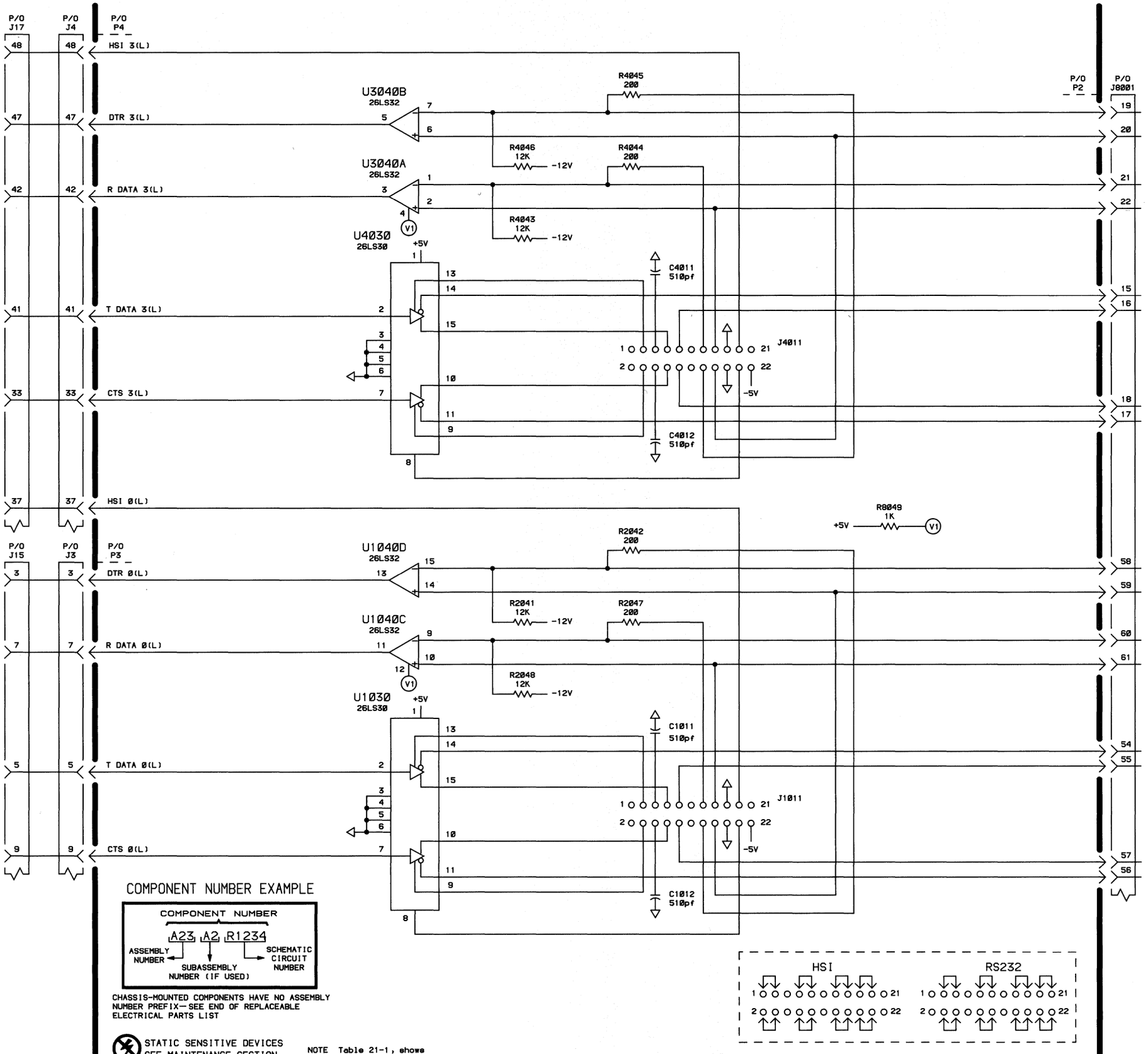
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX— SEE END OF REPLACEABLE ELECTRICAL PARTS LIST

STATIC SENSITIVE DEVICES
SEE MAINTENANCE SECTION

NOTE Table 21-1, shows IC pin-out (VCC & GND).

HSI: 1–21, 2–22
RS232: 1–21, 2–22

P/O A35 IO ADAPTOR BOARD



COMPONENT NUMBER EXAMPLE

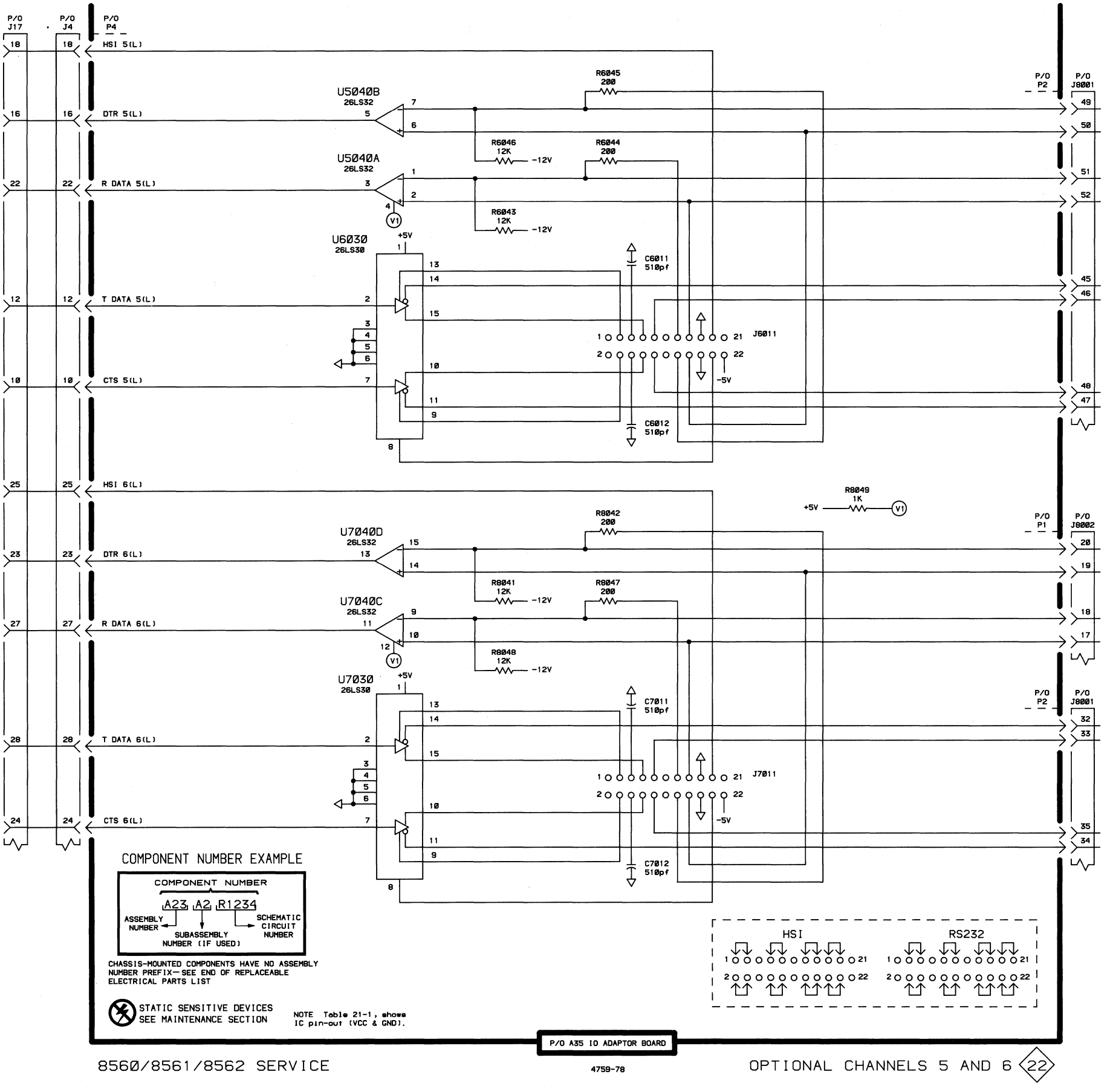
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST

STATIC SENSITIVE DEVICES
SEE MAINTENANCE SECTION

NOTE Table 21-1, shows IC pin-out (VCC & GND).

P/O A35 IO ADAPTOR BOARD

4759-77


P/O J17
P/O J4
P/O P4
HSI 5(L)
DTR 5(L)
R DATA 5(L)
T DATA 5(L)
CTS 5(L)
HSI 6(L)
DTR 6(L)
R DATA 6(L)
T DATA 6(L)
CTS 6(L)
U5040B
26LS32
U5040A
26LS32
U6030
26LS30
U7040D
26LS32
U7040C
26LS32
U7030
26LS30
R6045 200
R6046 12K
R6044 200
R6043 12K
R8042 200
R8041 12K
R8047 200
R8048 12K
R8049 1K
-12V
+5V
V1
C6011 510pf
C6012 510pf
C7011 510pf
C7012 510pf
J6011
J7011
-5V
P/O P2
P/O J8001
P/O P1
P/O J8002
HSI
RS232
COMPONENT NUMBER EXAMPLE
COMPONENT NUMBER
A23 A2 R1234
ASSEMBLY NUMBER
SUBASSEMBLY NUMBER (IF USED)
SCHEMATIC CIRCUIT NUMBER
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST
STATIC SENSITIVE DEVICES SEE MAINTENANCE SECTION
NOTE Table 21-1, shows IC pin-out (VCC & GND).
P/O A35 IO ADAPTOR BOARD
4759-78

P/O J17 5 — HSI 4(L)
P/O J4 5
P/O P4

6 — DTR 4(L)
9 — R DATA 4(L)
3 — T DATA 4(L)
4 — CTS 4(L)

U5040D 26LS32: 13, 15, 14
U5040C 26LS32: 11, 9, 10, 12 (V1)
U5030 26LS30: +5V 1; 2, 3, 4, 5, 6, 7, 8, 10, 11, 13, 14, 15, 9

R6042 200Ω
R6041 12K -12V
R6047 200Ω
R6048 12K -12V
C5011 510pF
C5012 510pF
J5011: 1 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 21; 2 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 22; -5V

P/O P2 J8001: 66, 67, 68, 69, 62, 63, 65, 64

17 — HSI 7(L)
15 — DTR 7(L)
21 — R DATA 7(L)
13 — T DATA 7(L)
11 — CTS 7(L)

U7040B 26LS32: 5, 7, 6
U7040A 26LS32: 3, 1, 2, 4 (V1)
U8030 26LS30: +5V 1; 2, 3, 4, 5, 6, 7, 8, 10, 11, 13, 14, 15, 9

R8049 1K +5V (V1)
R8045 200Ω
R8046 12K -12V
R8044 200Ω
R8043 12K -12V
C8011 510pF
C8012 510pF
J8011: 1 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 21; 2 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 22; -5V

P/O P1 J8102: 7, 5, 3, ◄, 15, 13, 9, 11

COMPONENT NUMBER EXAMPLE

COMPONENT NUMBER: A23 A2 R1234
ASSEMBLY NUMBER — SUBASSEMBLY NUMBER (IF USED) — SCHEMATIC CIRCUIT NUMBER

CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST

STATIC SENSITIVE DEVICES SEE MAINTENANCE SECTION

NOTE Table 21-1, shows IC pin-out (VCC & GND).

HSI: 1 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 21; 2 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 22
RS232: 1 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 21; 2 ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ 22

P/O A35 IO ADAPTOR BOARD

P/O J15 | P/O J3 | P/O P3 — P/O P2 | P/O J8001

12 CTS 1(L) — U7060C 26LS30 (C7063 510pf) — 4
13 RST 1(L) — U6060B 26LS32 — R6063 12K -12V — 3
14 R DATA 1(L) — U6060C 26LS32 — R6061 12K -12V — 1
15
16 T DATA 1(L) — U7060D 26LS30 (C7064 510pf) — 2
17
18 CLOCK 1 — 6
19
20 DTR 1(L) — U8060C 26LS32 — R7061 12K -12V — 5
22 +5V — C3061 22uf — 0.1uf — +5V
C1013 C4031 C7031
C1031 C5013 C7041
C1041 C5031 C7063
C2031 C5041 C8013
C3013 C6013
C3031 C6031
C3041 C6061
C4013 C7013
23 -12V — U2050 -5V REGULATOR — -5V
C2051 22uf — C2052 22uf
R7059 1K +5V — V2
26 DTR 2(L) — U6060D 26LS32 — R6062 12K -12V — 12
27
28 CLOCK 2 — 13
29
30 T DATA 2(L) — U7060B 26LS30 (C7062 510pf) — 9
31
32 R DATA 2(L) — U8060B 26LS32 — R7062 12K -12V — 8
33 RST 2(L) — U8060A 26LS32 — R8061 12K -12V — 10
34 CTS 2(L) — U7060A 26LS30 (C7061 510pf) — 11

COMPONENT NUMBER EXAMPLE

COMPONENT NUMBER: A23 A2 R1234
ASSEMBLY NUMBER
SUBASSEMBLY NUMBER (IF USED)
SCHEMATIC CIRCUIT NUMBER

CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST

STATIC SENSITIVE DEVICES
SEE MAINTENANCE SECTION

NOTE Table 21-1, shows IC pin-out (VCC & GND).

P/O A35 IO ADAPTOR BOARD

4759-80

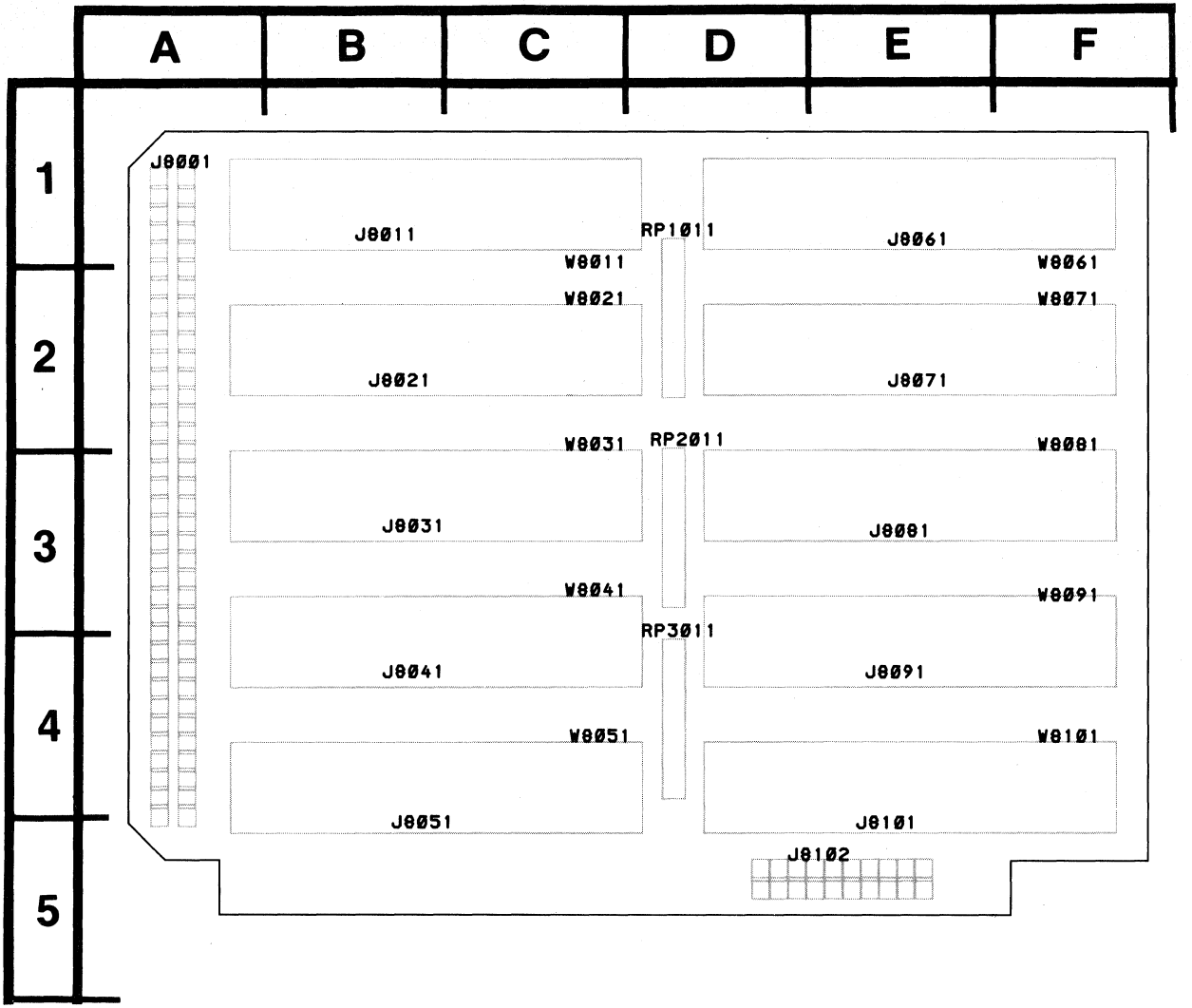
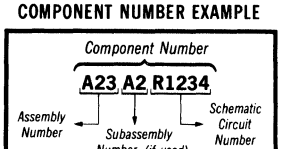


Figure 21-5. A40 IOC Board.

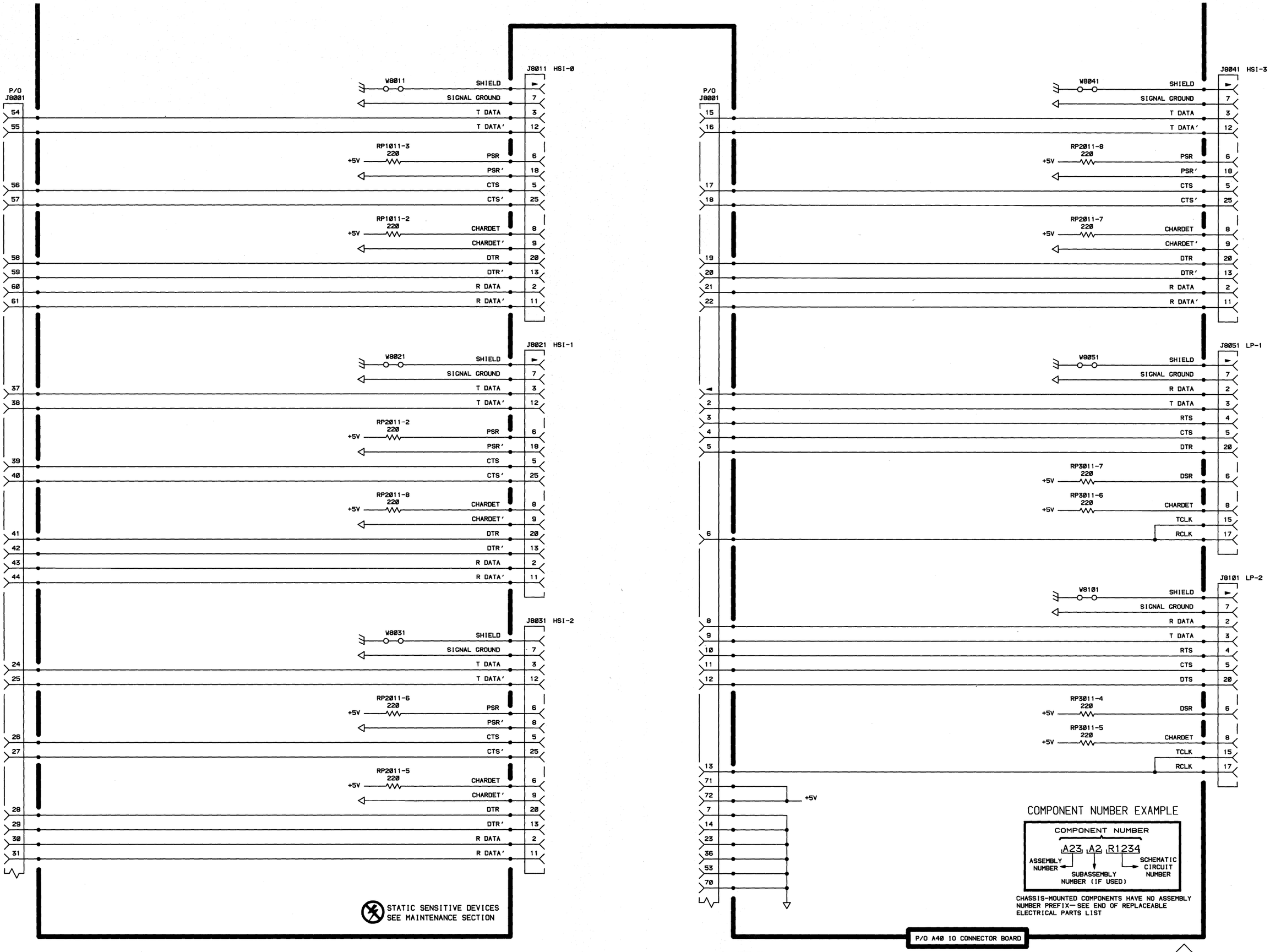
COMPONENT NUMBER EXAMPLE

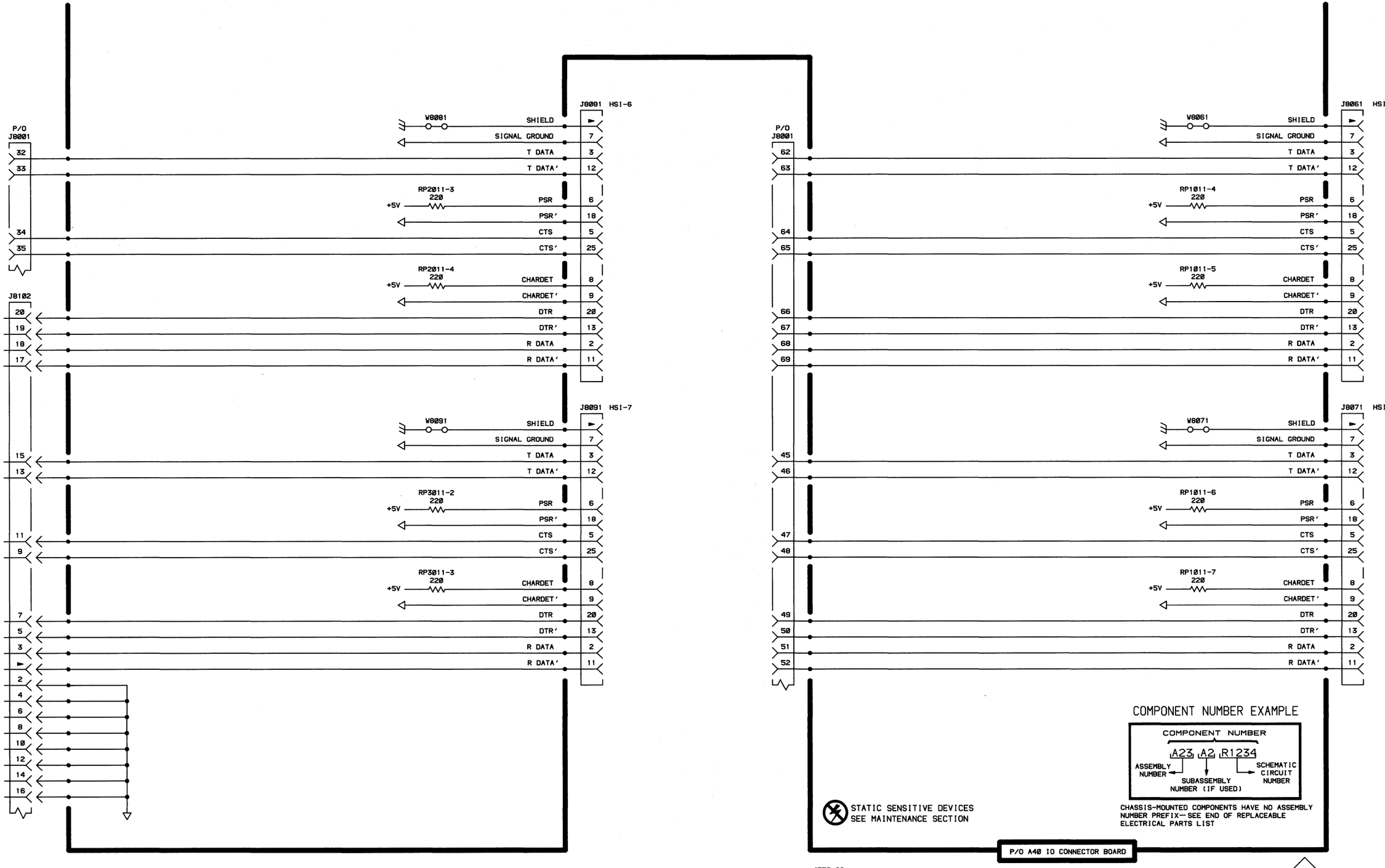


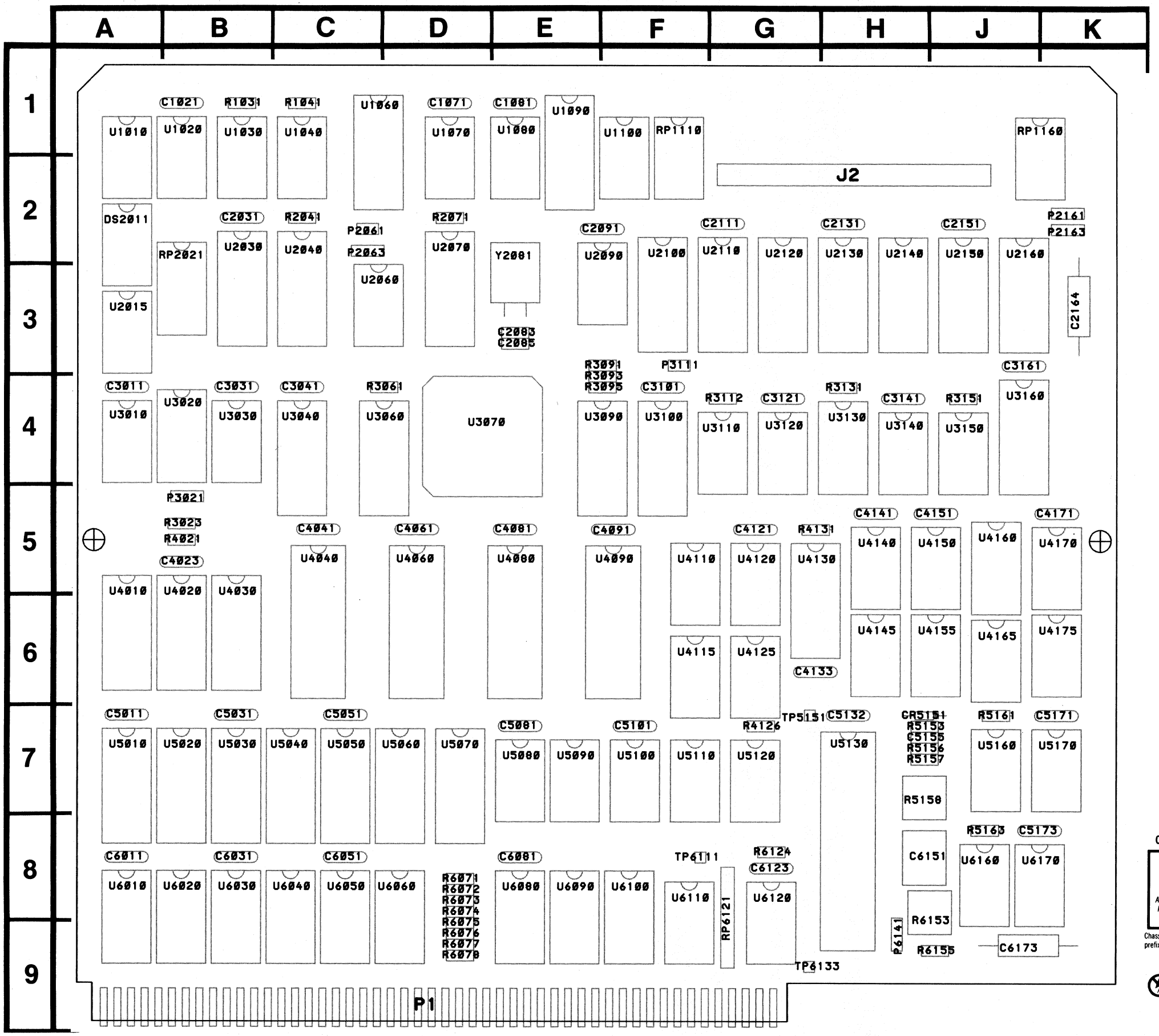
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

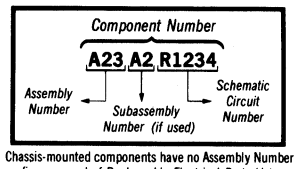
4759-49


P/O J8001
J8011 HSI-0
W8011
SHIELD
SIGNAL GROUND
T DATA
T DATA'
RP1011-3
220
+5V
PSR
PSR'
CTS
CTS'
RP1011-2
220
+5V
CHARDET
CHARDET'
DTR
DTR'
R DATA
R DATA'
J8021 HSI-1
W8021
RP2011-2
RP2011-8
RP2011-6
RP2011-5
J8031 HSI-2
W8031
J8041 HSI-3
W8041
RP2011-8
RP2011-7
J8051 LP-1
W8051
R DATA
T DATA
RTS
CTS
DTR
RP3011-7
DSR
RP3011-6
TCLK
RCLK
J8101 LP-2
W8101
RP3011-4
RP3011-5
+5V
STATIC SENSITIVE DEVICES
SEE MAINTENANCE SECTION
COMPONENT NUMBER EXAMPLE
COMPONENT NUMBER
A23 A2 R1234
ASSEMBLY NUMBER
SUBASSEMBLY NUMBER (IF USED)
SCHEMATIC CIRCUIT NUMBER
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX— SEE END OF REPLACEABLE ELECTRICAL PARTS LIST
P/O A40 IO CONNECTOR BOARD
4759-81


P/O J8001
32
33
34
35
J8102
20
19
18
17
15
13
11
9
7
5
3
2
4
6
8
10
12
14
16
J8001 HSI-6
W8001
SHIELD
SIGNAL GROUND
T DATA
T DATA'
RP2011-3
220
+5V
PSR
PSR'
CTS
CTS'
RP2011-4
220
+5V
CHARDET
CHARDET'
DTR
DTR'
R DATA
R DATA'
J8091 HSI-7
W8091
SHIELD
SIGNAL GROUND
T DATA
T DATA'
RP3011-2
220
+5V
PSR
PSR'
CTS
CTS'
RP3011-3
220
+5V
CHARDET
CHARDET'
DTR
DTR'
R DATA
R DATA'
7
3
12
6
18
5
25
8
9
20
13
2
11
P/O J8001
62
63
64
65
66
67
68
69
45
46
47
48
49
50
51
52
J8061 HSI-4
W8061
SHIELD
SIGNAL GROUND
T DATA
T DATA'
RP1011-4
220
+5V
PSR
PSR'
CTS
CTS'
RP1011-5
220
+5V
CHARDET
CHARDET'
DTR
DTR'
R DATA
R DATA'
J8071 HSI-5
W8071
SHIELD
SIGNAL GROUND
T DATA
T DATA'
RP1011-6
220
+5V
PSR
PSR'
CTS
CTS'
RP1011-7
220
+5V
CHARDET
CHARDET'
DTR
DTR'
R DATA
R DATA'
COMPONENT NUMBER EXAMPLE
COMPONENT NUMBER
A23 A2 R1234
ASSEMBLY NUMBER
SUBASSEMBLY NUMBER (IF USED)
SCHEMATIC CIRCUIT NUMBER
STATIC SENSITIVE DEVICES
SEE MAINTENANCE SECTION
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST
P/O A40 IO CONNECTOR BOARD
4759-82



COMPONENT NUMBER EXAMPLE



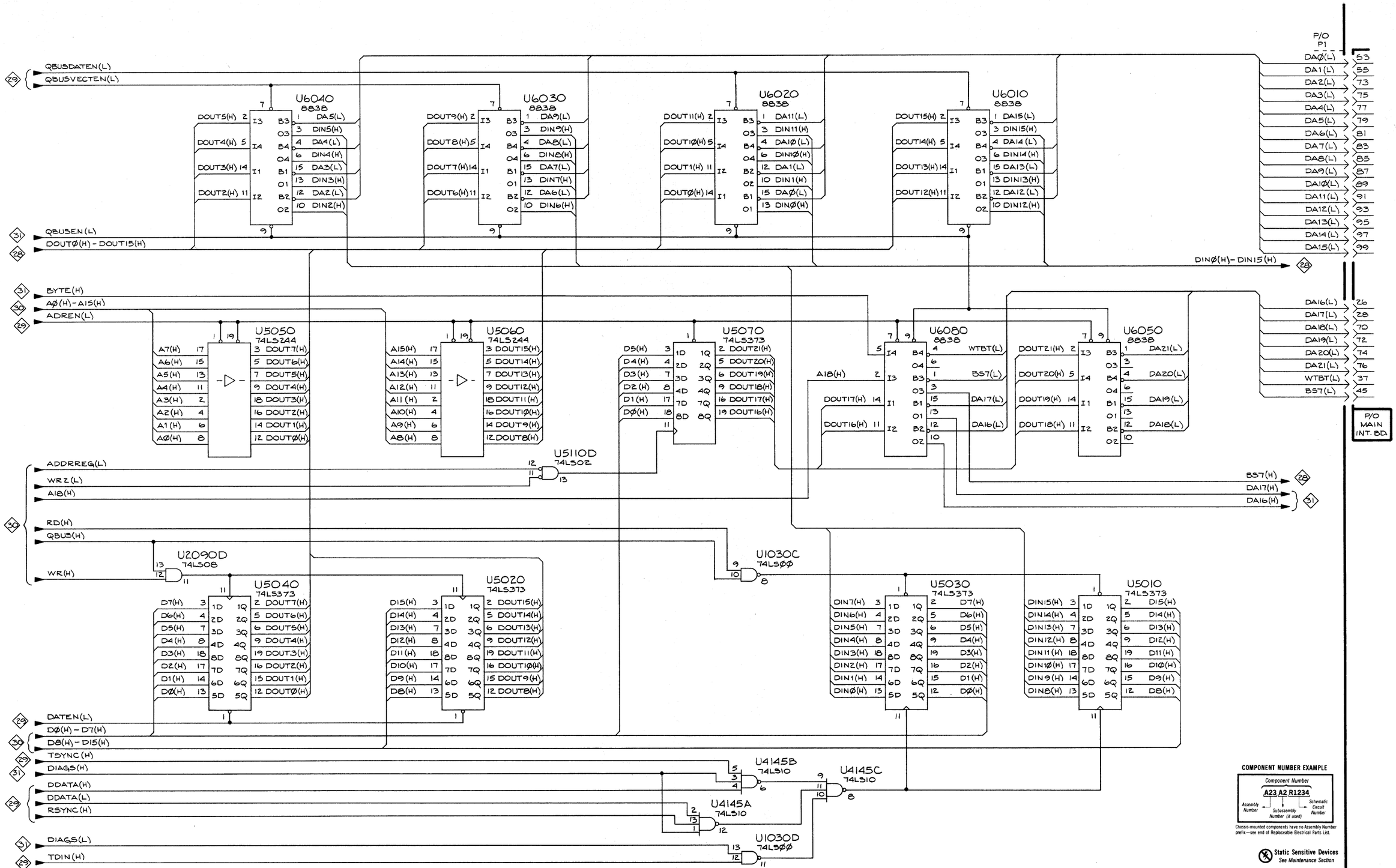
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

4759-50

MSC COMPONENT LOCATIONS

Figure 21-6. A45 MSC Board.



COMPONENT NUMBER EXAMPLE

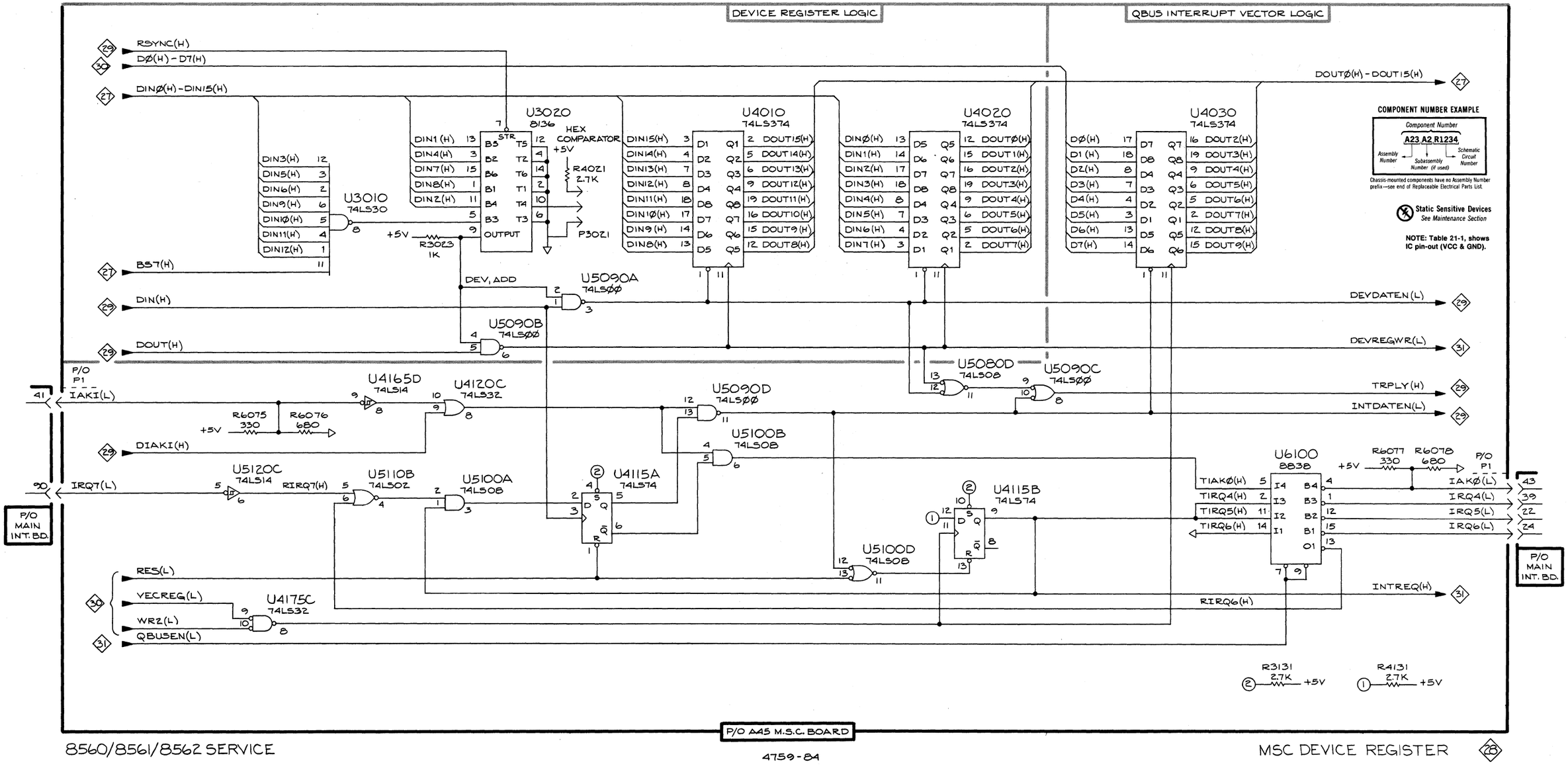
Component Number: A23 A2 R1234
(Assembly Number · Subassembly Number (if used) · Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A45 M.S.C. BOARD


DEVICE REGISTER LOGIC
QBUS INTERRUPT VECTOR LOGIC
RSYNC(H)
DØ(H) - D7(H)
DINØ(H) - DIN15(H)
DOUTØ(H) - DOUT15(H)
BS7(H)
DIN(H)
DOUT(H)
DEV, ADD
DEVDATEN(L)
DEVREGWR(L)
TRPLY(H)
INTDATEN(L)
INTREQ(H)
IAKI(L)
DIAKI(H)
IRQ7(L)
RIRQ7(H)
RES(L)
VECREG(L)
WR2(L)
QBUSEN(L)
RIRQ6(H)
U3020 8136 HEX COMPARATOR
U3010 74LS30
U4010 74LS374
U4020 74LS374
U4030 74LS374
U5090A 74LSØØ
U5090B 74LSØØ
U5090C 74LSØØ
U5090D 74LSØØ
U5080D 74LS08
U5100A 74LS08
U5100B 74LS08
U5100D 74LS08
U4165D 74LS14
U5120C 74LS14
U4120C 74LS32
U5110B 74LS02
U4115A 74LS74
U4115B 74LS74
U4175C 74LS32
U6100 8838
+5V
R3023 1K
R4021 2.7K
R6075 330
R6076 680
R6077 330
R6078 680
R3131 2.7K
R4131 2.7K
P3021
P/O P1
P/O MAIN INT. BD.
P/O A45 M.S.C. BOARD
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NOTE: Table 21-1, shows IC pin-out (VCC & GND).

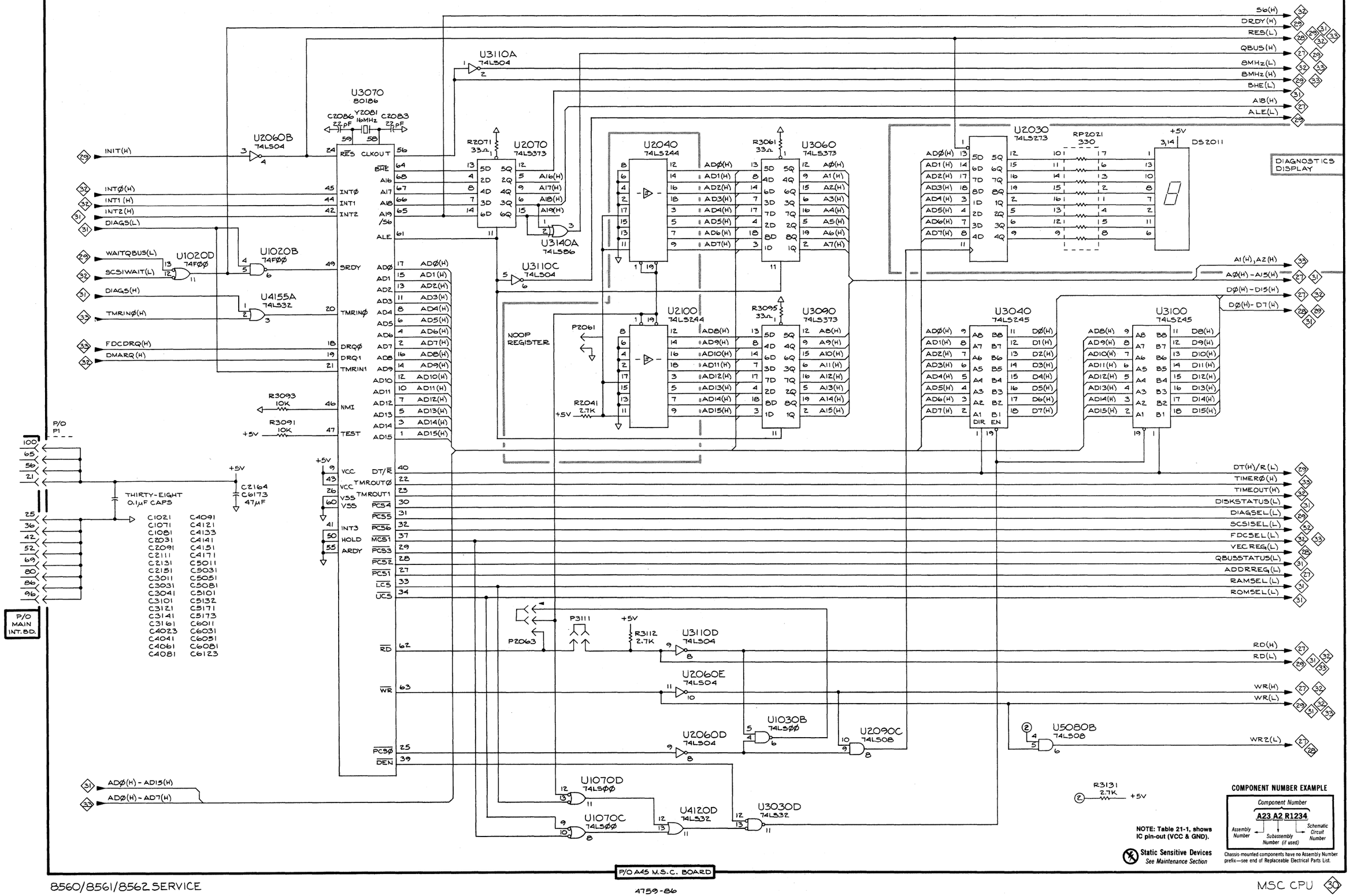
RD(L)
DIAGSEL(L)
DØ(H)-D7(H)
DRDY(H)
RES(L)
WR(L)
DT(H)/R(L)
8MHz(H)
P/O P1 DMGI(L) 47
P/O MAIN INT.BD.

U3160 74LS273
D7(H) 7 3D 3Q 6 DDATA(H)
D6(H) 17 7D 7Q 16 IAKI(H)
D5(H) 14 6D 6Q 15 DQBUS(H)
D4(H) 13 5D 5Q 12 SYNC(H)
D3(H) 8 4D 4Q 9 DDMGI(H)
D2(H) 4 2D 2Q 5 DRPLY(H)
D1(H) 3 1D 1Q 2 DREQ(H)
DØ(H) 18 8D 8Q 19 DCONT(H)
11

U4175D 74LS32
U3110E 74LS04
U4125B 74LS74
U4140D 74LS08
U4140C 74LS08
U4130 PAL16R4
DIAGCONT TSACK TSYNC SYNC DMGI RPLY INIT REQ ADREN DATEN OE NC NC
U4160 74LS399
C2 C1 B2 B1 A2 A1 D2 D1 OC OB OA OD
+5V R6073 330 R6074 680
U5120A 74LS14
U3120A 74LS11
U4175A 74LS32
U2160 74LS244
P2161 P2163
D7(H) D6(H) D5(H) D4(H) D3(H) D2(H) D1(H) DØ(H)
DATEN(L)
TDIN(H)/DOUT(H)
DDATA(H)
DDATA(L)
DIAKI(H)
TSYNC(H)
TDIN(H)
U6090 8838
P/O P1 DIN(L) 33
DIN(H)
DOUT(L) 29
DOUT(H)
SACK(L) 88
SYNC(L) 35
RSYNC(H)
U6060 8838
R6071 330 R6072 680 +5V
DMGO(L) 49
DMR(L) 44
RPLY(L) 31
INIT(L) 51
P/O MAIN INT.BD.
TSACK(H)
WRT(L)
ADREN(L)
QBUSDATEN(L)
QBUSVECTEN(L)
QBUSTIMEOUT(L)
WAITQBUS(L)
INIT(H)
DATEN(L)
U5100C 74LS08
U3120C 74LS11
U4120B 74LS32
U4150D 74LS02
U4170D 74LSØØ
U4170B 74LSØØ
U5170B 74LS393 CLR QD
U4140B 74LS08
U5080A 74LS08
U2060C 74LS04
U4110A 74LS74
U4165E 74LS14
U4170A 74LSØØ
U3110B 74LS04
U4170C 74LSØØ
U5110A 74LS02
U2015A 74LS74
INIT(H)
REQ(H)
QBUS(H)
ALE(L)
500KHz
DEVDATEN(L)
INTDATEN(L)
QBUSEN(L)
TRPLY(H)
R4131 2.7K +5V
R3131 2.7K +5V
R3151 2.7K +5V

COMPONENT NUMBER EXAMPLE
Component Number A23 A2 R1234
Assembly Number / Subassembly Number (if used) / Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices See Maintenance Section
NOTE: Table 21-1, shows IC pin-out (VCC & GND).

QBUS DMA LOGIC
P/O A45 M.S.C. BOARD


U3070
80186
U3110A
74LS04
U2060B
74LS04
U2070
74LS373
U2040
74LS244
U3060
74LS373
U2030
74LS273
RP2021
330
+5V
DS2011
DIAGNOSTICS DISPLAY
U2100
74LS244
U3090
74LS373
U3040
74LS245
U3100
74LS245
U3140A
74LS86
U3110C
74LS04
U1020D
74F00
U1020B
74F00
U4155A
74LS32
NOOP REGISTER
P2061
P2063
P3111
R2041 2.7K
R3112 2.7K
R3131 2.7K
R3093 10K
R3091 10K
U3110D
74LS04
U2060E
74LS04
U2060D
74LS04
U1030B
74LS00
U2090C
74LS08
U5080B
74LS08
U1070D
74LS00
U1070C
74LS00
U4120D
74LS32
U3030D
74LS32
THIRTY-EIGHT 0.1µF CAPS
C2164
C6173 47µF
P/O MAIN INT. BD.
P/O P1
P/O A45 M.S.C. BOARD
4759-86
8560/8561/8562 SERVICE
MSC CPU
30
MSC CPU
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
NOTE: Table 21-1, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section

QBUS STATUS REGISTER

DISK STATUS REGISTER

DKCHG(H)
TWOSIDED(H)
ONBUS(H)
RES(L)
INTREQ(H)
FDISKINT(H)
DA16(H)
DA17(H)
QBUSTIMEOUT(L)
DEVREGWR(L)
QBUSSTATUS(L)
TDIN(H)
DØ(H) - D7(H)
DISKSTATUS(L)
WRT(L)
DATEN(L)
BHE(L)
RAMSEL(L)
WR(L)
RD(L)
AØ(H) - A7(H)
AB(H) - A15(H)
ROMSEL(L)

U5080C 74LS08
U1080A 74LS74
U1080B 74LS74
U1040A 74LS74
U1040B 74LS74
U4110B 74LS74
U1100D 74LS32
U1100A 74LS32
U1100C 74LS32
U1100B 74LS32
U2060F 74LS04
U3120B 74LS11
U4155B 74LS32
U3030A 74LS32
U3030B 74LS32
U3030C 74LS32
U1090 74LS244
U3130 74LS174
U1060 74LS244

DØ(H) D1(H) D2(H) D3(H) D4(H) D5(H) D6(H) D7(H)

+5V R1031 2.7K
+5V R1041 2.7K
R3131 2.7K +5V

DS(H)
DDEN(L)
INTZ(H)
QBUSEN(L)
DIAGS(H)
ARBITRATIONEN(H)
DKT(H)/R(L)
SEL(H)
SCSINIT(L)
DISKSTATUS WR(H)
DIAGS(L)
DISKSTATUS RD(L)
BYTE(H)
WORD TRANSFER(L)
AD8(H) - AD15(H)
ADØ(H) - AD7(H)

U4040 HM6264
U4080 HM6264
U4060 27128
U4090 27128

A1(H) A2(H) A3(H) A4(H) A5(H) A6(H) A7(H) A8(H) A9(H) A10(H) A11(H) A12(H) A13(H) A14(H)

AD8(H) AD9(H) AD10(H) AD11(H) AD12(H) AD13(H) AD14(H) AD15(H)
ADØ(H) AD1(H) AD2(H) AD3(H) AD4(H) AD5(H) AD6(H) AD7(H)

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number · Subassembly Number (if used) · Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

P/O A45 M.S.C. BOARD

MSC MEMORY

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U4165B 74LS14
INTØ(H) → 30
DØ(H) - D15(H) ← 30

U2150 Z908 — DØ(H) DB0(H); D1(H) DB1(H); D2(H) DB2(H); D3(H) DB3(H)
U2140 Z908 — D4(H) DB4(H); D5(H) DB5(H); D6(H) DB6(H); D7(H) DB7(H)
U2110 Z908 — D15(H) BUS3; D14(H) BUS2; D13(H) BUS1; D12(H) BUSØ
U2120 Z908 — D11(H) BUS3; D10(H) BUS2; D9(H) BUS1; D8(H) BUSØ
RP1110 +5V 330/220
+5V RP1160 330/220
J2: DBØ(H) 2; DB1(H) 4; DB2(H) 6; DB3(H) 8; DB4(H) 10; DB5(H) 12; DB6(H) 14; DB7(H) 16
I(L)/O(H) 50; MSG(L) 42; C(L)/D(H) 46; BSY(L) 36; REQ(L) 48; ACK(L) 38; ATN(L) 32; RES(L) 40
DSELRD(L)
DSENWR(L)
31 DISKSTATUS WR(H)
31 DISKSTATUS RD(L)

30 WR(L) — U4155C 74LS32
30 SCSISEL(L) — U4155D 74LS32
30 RD(L)
31 DIAGS(L)

U4140A 74LS08; U3150D 74S38 → DBP(L) 18
U3140D 74LS86; U4150A 74LS02 → INT1(H) → 30
DMARQ(H) → 30
+5V 220/330 RP1160
SEL(L) 44
+5V 220/330 RP1110 (pin 9)
NC 22; +5V 24; NC 26; NC 28; NC 30
1-40 ODD

U5120B 74LS14
31 SCSINIT(L)
30 TIMEOUT(H) — U1070B 74LSØØ; U4120A 74LS32
U4165A 74LS14; U5120F 74LS14
U3150C 74S38
U2130 PAL16R4: BSEL, BSY, SEL, ARBEN, ACK, REQ, WR, INIT, S6; BE, BSY, Y, Z, B, A
U2090A 74LS08
31 SEL(H)
31 ARBITRATIONEN(H)
30 8MHz(L)
30 FDCSEL(L)
R4126 1K +5V
U3150A 74S38
R3151 2.7K +5V
U3150B 74S38
30 WR(H) — U2090B 74LS08; U4175B 74LS32
31 DKT(H)/R(L) — U1010D 74LS02
U6160A 74LS74
U4125 74LS74
ONBUS(H) → 31
NC; NC; NC
U4150B 74LS02
U1070A 74LSØØ
U1020C 74FØØ
SCSIWAIT(L) → 30
33 DELAYWR(L)
30 RES(L)
30 S6(H)

COMPONENT NUMBER EXAMPLE
Component Number: A23 A2 R1234 (Assembly Number; Subassembly Number (if used); Schematic Circuit Number)
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: Table 21-1, shows IC pin-out (VCC & GND).

Static Sensitive Devices — See Maintenance Section

P/O A45 M.S.C. BOARD

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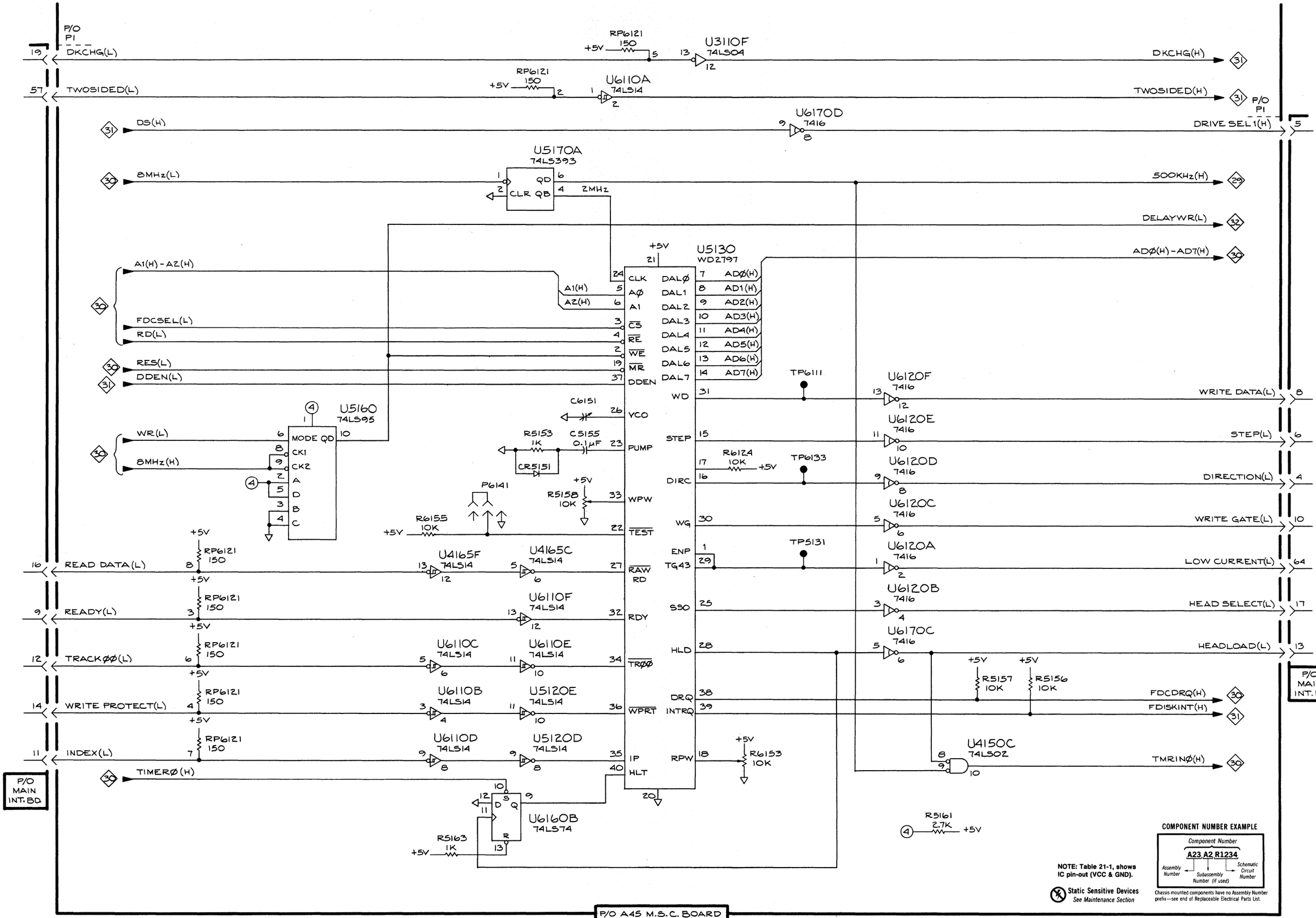

P/O P1
DKCHG(L)
RP6121 150
+5V
U3110F 74LS04
DKCHG(H)
TWOSIDED(L)
U6110A 74LS14
TWOSIDED(H)
DS(H)
U6170D 7416
DRIVE SEL 1(H)
U5170A 74LS393
8MHz(L)
QD
CLR QB
2MHz
500KHz(H)
DELAYWR(L)
ADØ(H)-AD7(H)
U5130 WD2797
A1(H)-A2(H)
FDCSEL(L)
RD(L)
RES(L)
DDEN(L)
CLK
DALØ
A1(H)
AØ
A2(H)
A1
CS
RE
WE
MR
DDEN
DAL1
DAL2
DAL3
DAL4
DAL5
DAL6
DAL7
AD1(H)
AD2(H)
AD3(H)
AD4(H)
AD5(H)
AD6(H)
AD7(H)
WD
TP6111
U6120F 7416
WRITE DATA(L)
U5160 74LS95
WR(L)
8MHz(H)
MODE QD
CK1
CK2
A
D
B
C
C6151
VCO
R5153 1K
C5155 0.1µF
CR5151
PUMP
STEP
U6120E 7416
STEP(L)
R6124 10K
TP6133
DIRC
U6120D 7416
DIRECTION(L)
P6141
R5158 10K
WPW
U6120C 7416
WRITE GATE(L)
R6155 10K
TEST
WG
TP5131
ENP
TG43
U6120A 7416
LOW CURRENT(L)
RAW RD
U4165F 74LS14
U4165C 74LS14
SSO
U6120B 7416
HEAD SELECT(L)
READ DATA(L)
RP6121 150
READY(L)
RDY
U6110F 74LS14
HLD
U6170C 7416
HEADLOAD(L)
TRACKØØ(L)
TRØØ
U6110C 74LS14
U6110E 74LS14
R5157 10K
R5156 10K
DRQ
INTRQ
FDCDRQ(H)
FDISKINT(H)
WRITE PROTECT(L)
WPRT
U6110B 74LS14
U5120E 74LS14
INDEX(L)
IP
HLT
RPW
R6153 10K
U5120D 74LS14
U4150C 74LS02
TMRINØ(H)
TIMERØ(H)
U6160B 74LS74
R5163 1K
R5161 2.7K
P/O MAIN INT. BD
P/O MAIN INT. BD
P/O A45 M.S.C. BOARD
NOTE: Table 21-1, shows IC pin-out (VCC & GND).
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

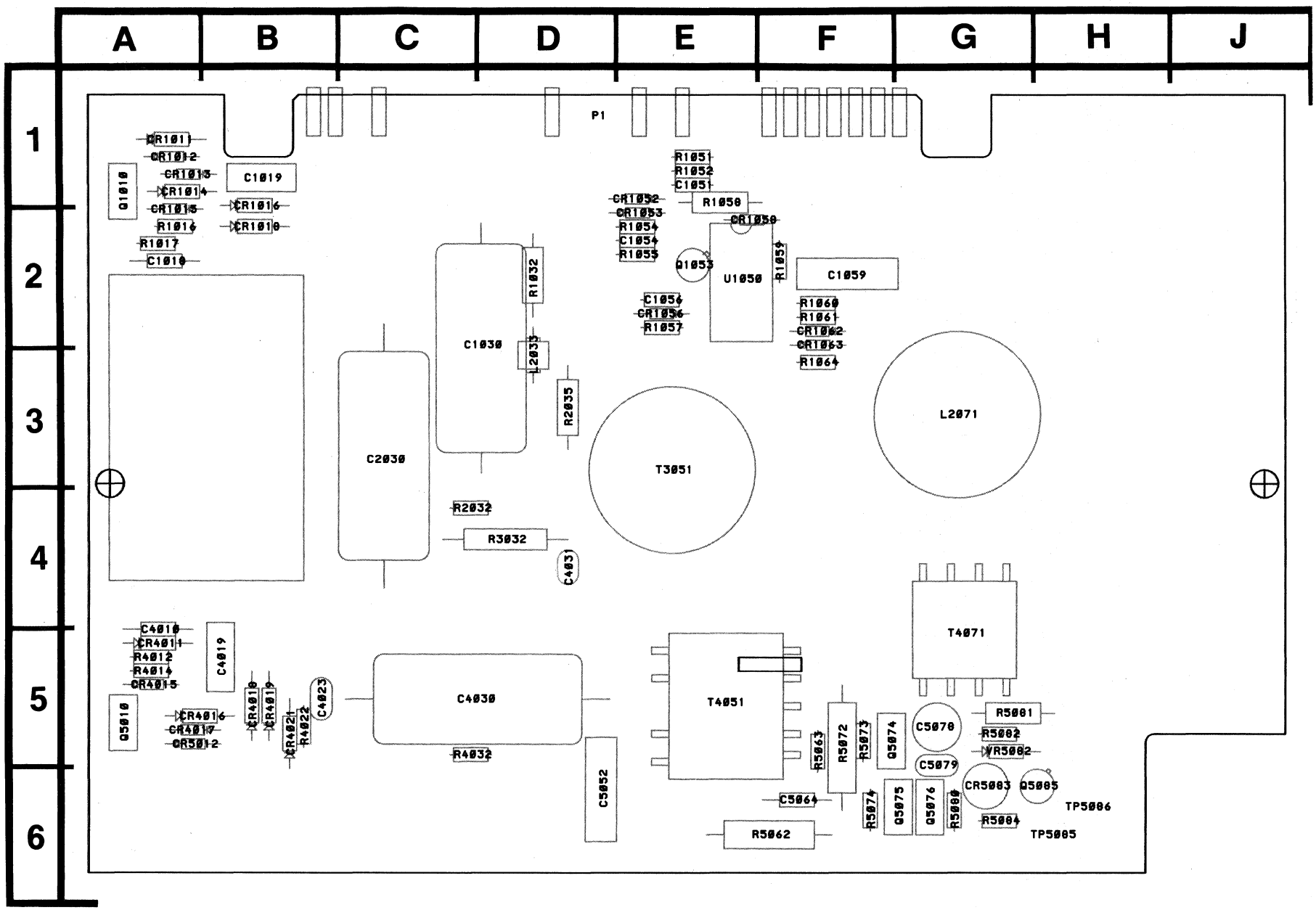
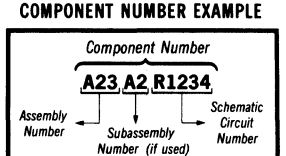


Figure 21-7. A62 Inverter Board.

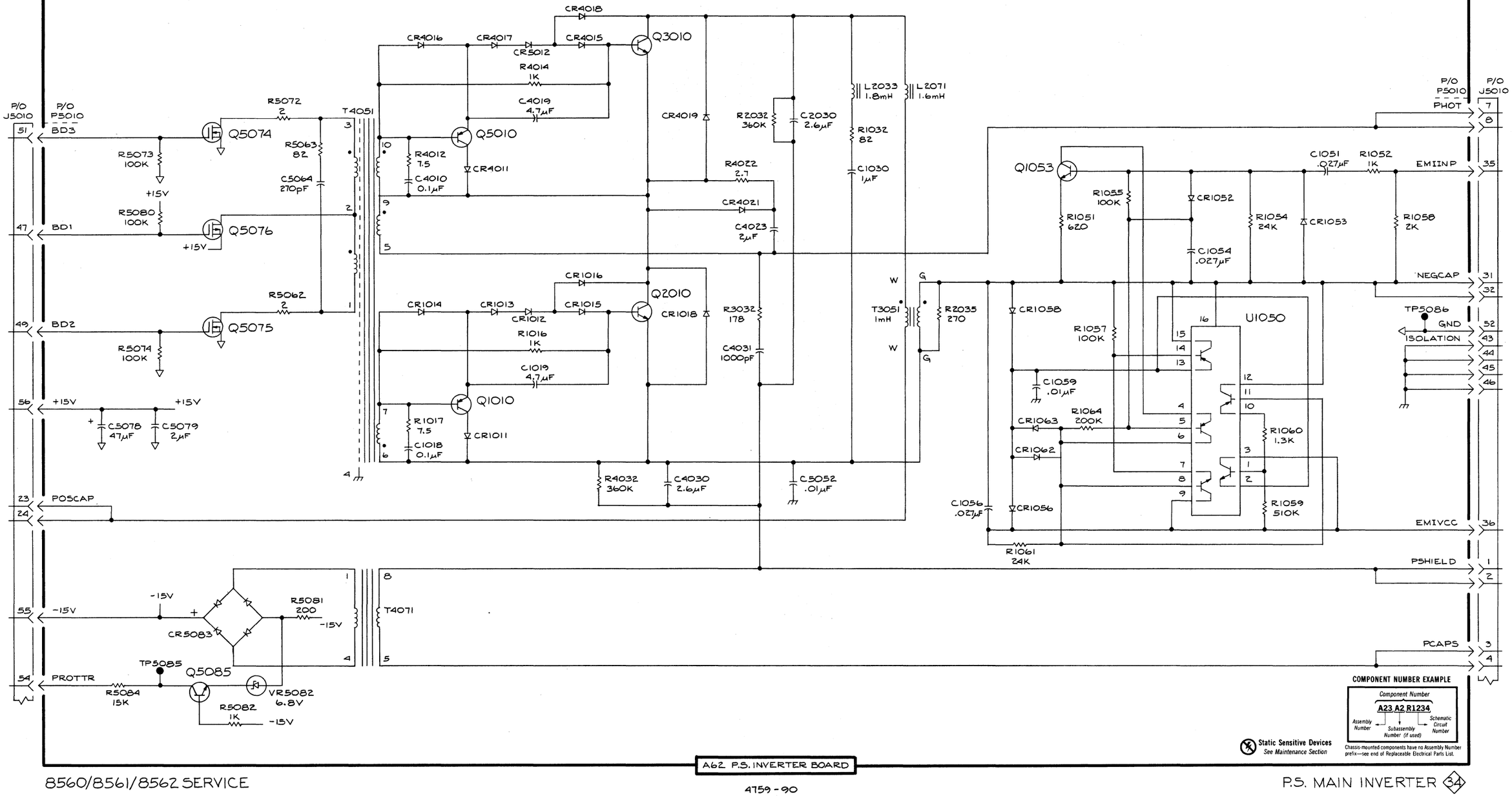
P.S. MAIN INVERTER COMPONENT LOCATIONS

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



A62 P.S. INVERTER BOARD

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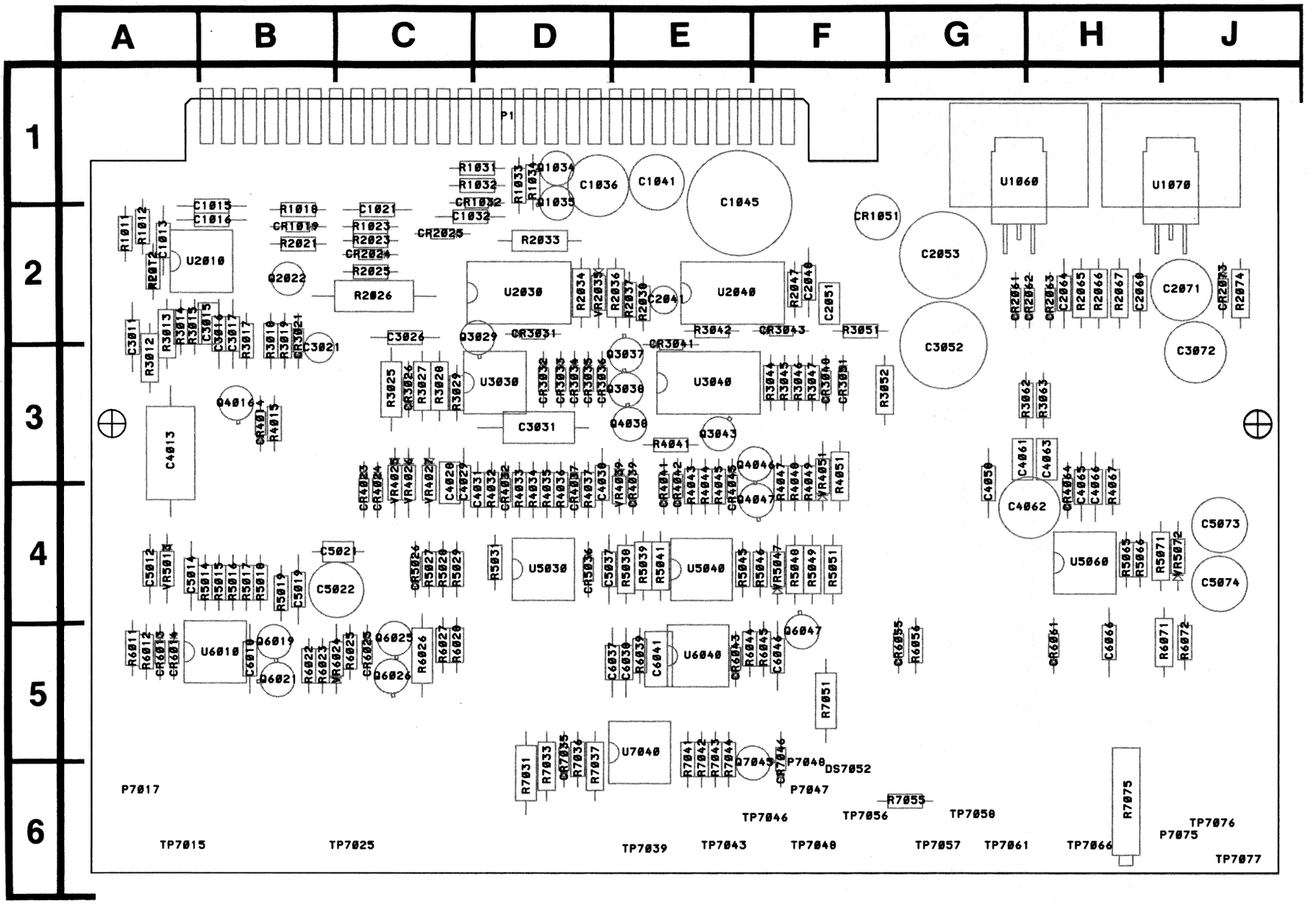
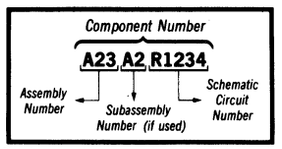


Figure 21-8. A64 Regulator Board.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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REGULATOR COMPONENT LOCATIONS

P/O J2010 18 — P/O P2010 — LNSENSE

+15V
R4015 1.3K
CR4014
C5014 1000pF
R5016 8.2K
R5017 8.2K
U6010B TL072
R5014 15K
R5015 56K
Q4016
R5019 10K

37 +12CO
R1023 1.8K
C1032 270pF
CR1032
R1032 3K

36 Vstart

VR4039 3V
R2036 3.32K
R2038 2.2K
R2037 470
CR3031
C2037 4.7µF
Q3037
VR2035 5V
R2034 5.49K
Q3038
C5021 68pF
U2040D 4011B
C5019 100pF
Q6021

CR3036
R3042 15K
U2040B 4011B
CR3043
R2047 8.2K
C2048 100pF
U2040C 4011B
CR3041
Q6019

+15V
R2033 1.5K
CR3035
CR3026
CR2025
C3031 .01µF
C3026 0.1µF
U3030 LM311
R3025 1.5K
Q3029
C4029 0.1µF
CR3034
U2030C 4023B
BD1 17

TRIGGER TP7039
U3040B 4013B
U2030A 4023B

R5018 3K
CR6014
CR6013
R6012 10K
C6018 1000pF
U6010A TL072
L31 36
R6011 22M

-15V
R3027 11.3K
R3028 887
VR4025 6.2V
CR4024
VR4026 6.2V
CR4023
R3029 1.2K
U2030B 4023B
C5012 0.1µF
C5022 47µF
VR5013 22V
BD3 24
BD2 21

36 Q6025
36 15kpd
36 U2040A
CR3032
R6026 1.5K
Vramp 37

CR4037
R4036 10K
CR4041
R4041 200
Q3043
R5027 6.2K
C4031 33pF
U5030D LM393
Q4038
R4035 100K
C4038 100pF
CR5026
R5031 18K
CR4039
R4037 2.2K
-15V
CR6025 36

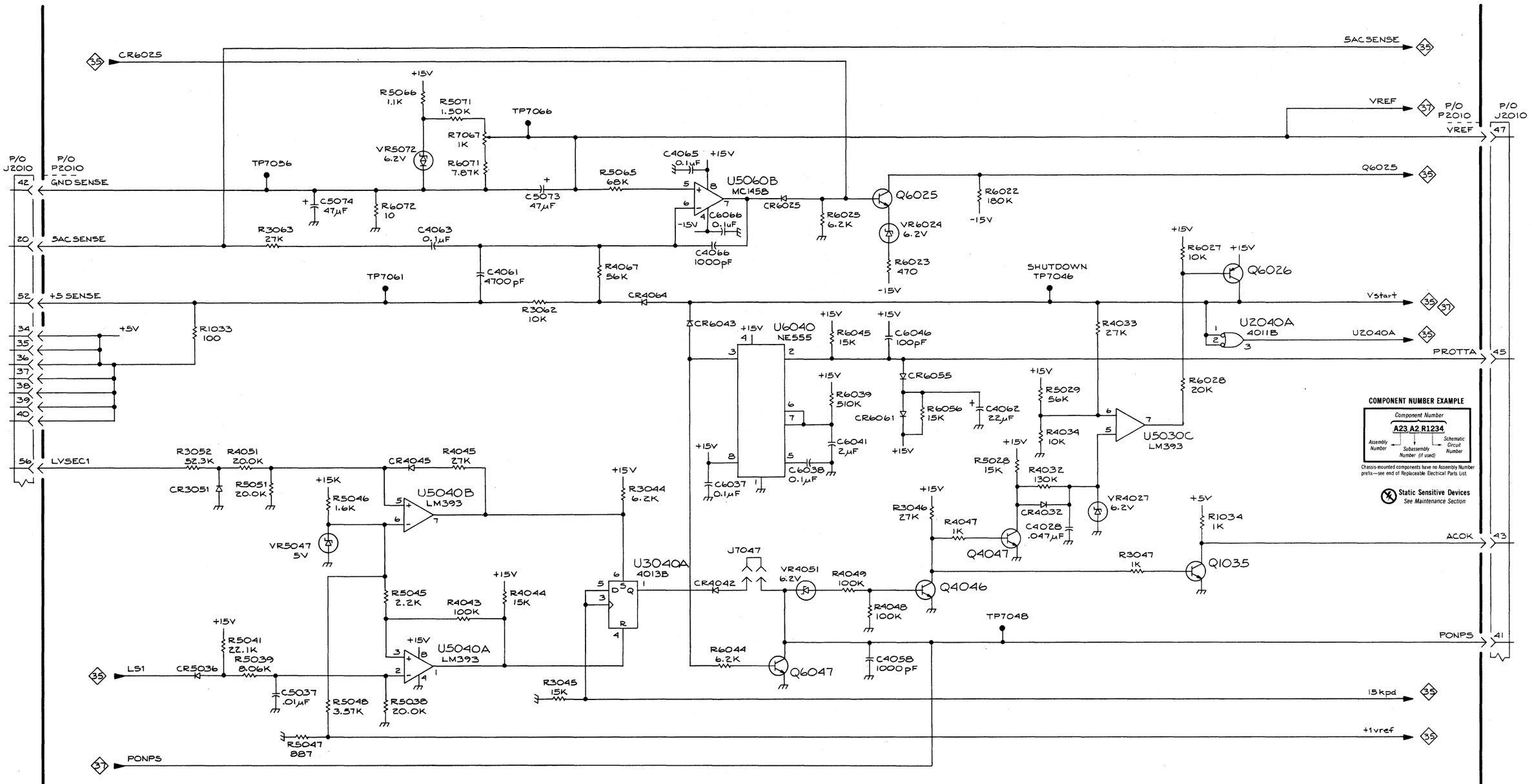
36 SAC SENSE
36 +1vref
37 Vur

TP7025 — P/O P2010 GND — P/O J2010 25 26 27 28 29 30 31 32 33
ISOLATION 13 14 15 16

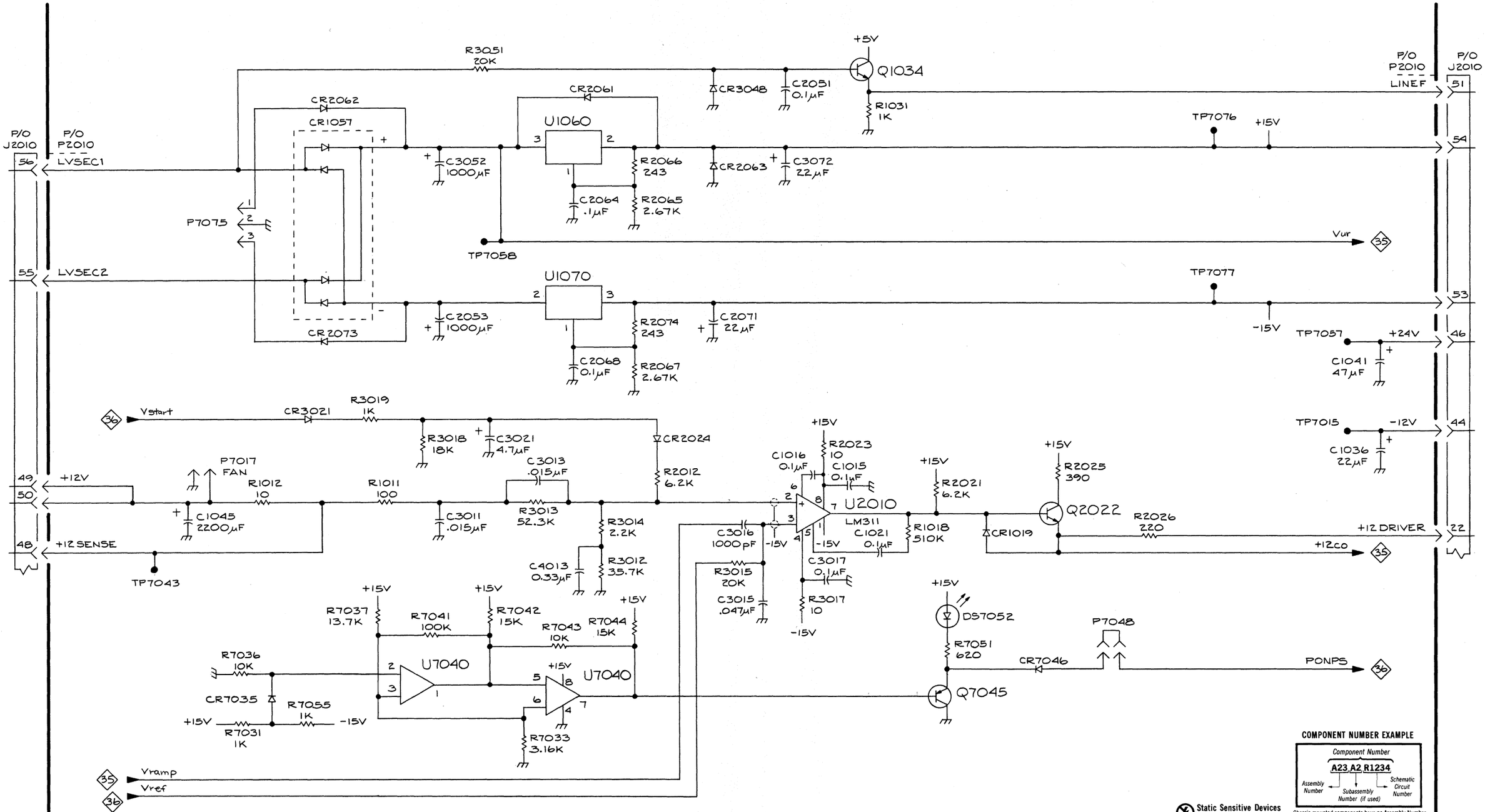
COMPONENT NUMBER EXAMPLE
Component Number: A23,A2,R1234,
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

P/O A64 P.S. REGULATOR BD.



P/O A64 P.S. REGULATOR BD.



P/O A64 P.S. REGULATOR BD.

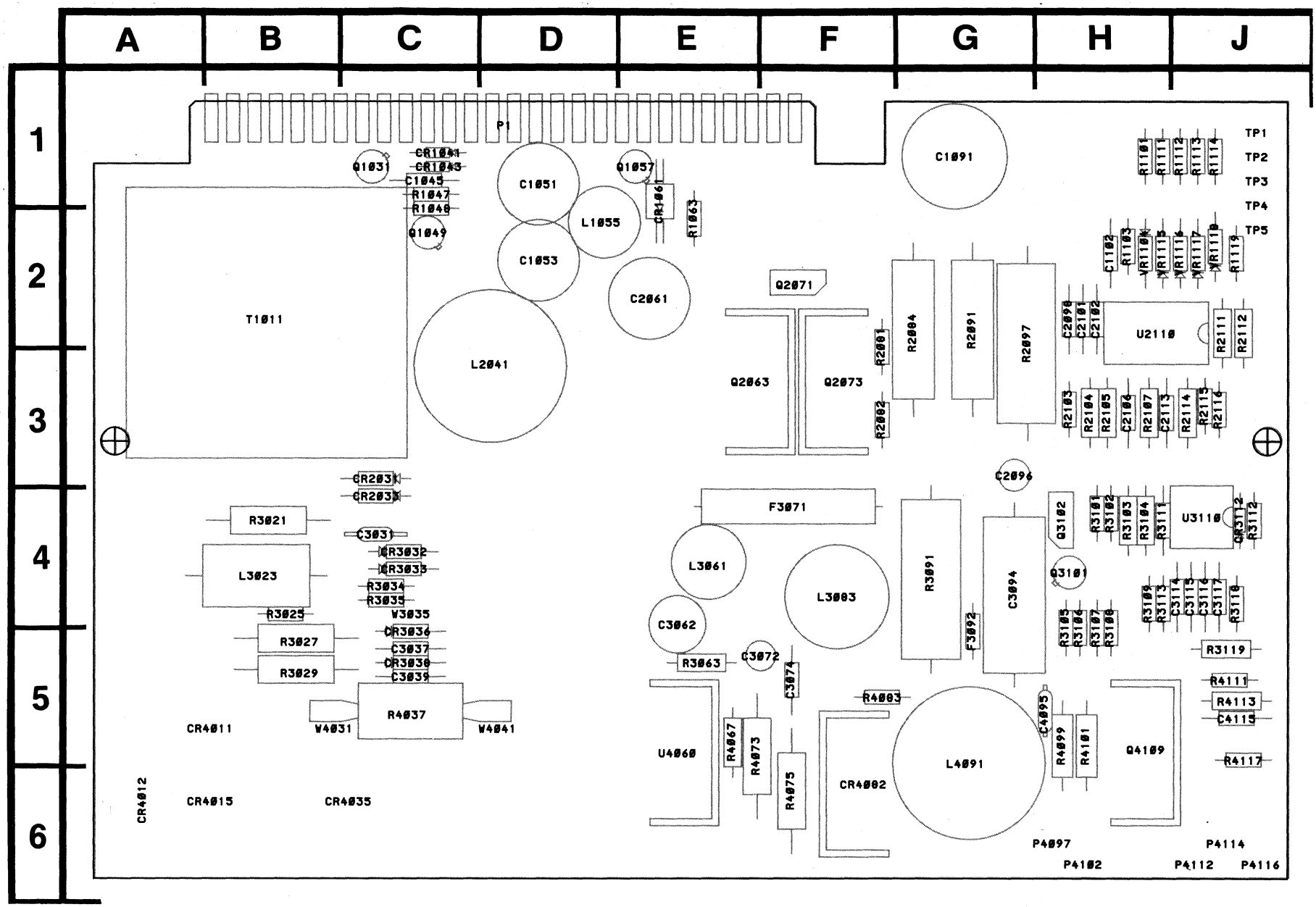
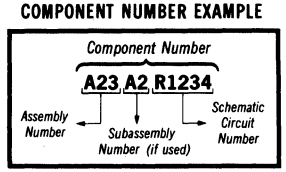


Figure 21-9. A66 Secondary Board.

SECONDARY COMPONENT LOCATIONS

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

4759-53

P/O J4010 — P/O P4010 PHOT — T1011 — CR3032 — L3083 1.3mH — F3071 3A — R3021 150 — C3031 470µF — C2096 10µF — C4095 1µF — CR3033 — C3094 220µF

-15V — R2107 57.6K — R2114 1.00K — R4101 0.2 — C2113 .01µF — R2115 1K — U2110C — P4112

R4113 69.8K — R4111 6.8M — C4115 150pF — R3091 300

R3112 22 — C3116 0.1µF — +15V — R3119 20.0K — C3117 0.1µF — U3110B — -15V — R2116 22 — C3115 0.1µF

R3107 110 — +5V — Q3102 — R3108 1K — Q4109 — R3109 51 — C3114 0.1µF — R3105 1K — R3106 100 — Q3101 — R4099 0.2 — R3101 7.5K — R3113 15K

P/O P4010 +24V — P/O J4010 46

R3118 15K — VREF 47

COMPONENT NUMBER EXAMPLE: Component Number A23 A2 R1234 (Assembly Number / Subassembly Number (if used) / Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

P/O J4010 — P/O P4010 PHOT — 25 GND — 26 — 27 — 28 — 29 — 30 — 31 — 32 — 33

53 -15V — C2101 0.1µF

54 +15V — C2102 0.1µF

CR4011 — L4091 87µH — F3092 10A — R4075 36 — C3074 .01µF — CR4082 — R4083 1K — C1091 2200µF — +12V 49 — 50

CR2033 — R2082 2K — Q2063 — R2084 50m — R2081 2K — Q2073 — R2091 50m — C2098 1000pF — U2110B — R2111 1.00K — R2112 44.2K — -15V — P4116

CR4012 — R2097 5 — Q2071 — -5V — +5V — Q1057 — -12V 44 — 12 DRIVER 22

CR2031 — L3061 4mH — C3062 100µF — U4060 — R4067 243 — R3063 2.05K — C3072 4.7µF

R4073 0.33 — CR1061 — R1063 1K — R3104 187K — R3102 1K — C3111 .01µF — U3110A — CR3112 — P4102 — R3103 1.00K

+5V — 34 — 35 — 36 — 37 — 38 — 39 — 40

C3037 .027µF — R3027 2.7 — L2041 10.5µH — L1055 2.3µH — C1053 1200µF — C1051 1200µF

P4097 — R2103 1K — +15V — R4037 5m — C2106 .01µF — R2104 1.00K — R2105 76.8K — -15V

CR4035 — CR4015 — CR3036 — CR3038 — R3029 2.7 — C3039 .027µF — C2061 270µF — -5V — L3023 270µH — R3034 51

TP5 — VR1104 15V — R1101 330 — -12V — TP3 — VR1118 5.6V — R1114 330 — +5V — TP2 — VR1117 13V — R1113 330 — +12V — TP1 — VR1115 27V — R1111 330 — +24V — TP4 — VR1116 16V — R1112 1K — +15V — R1119 15K — -15V — R1103 330 — C1102 .01µF — U2110A — P4114 — R4117 15K — PROTTR 45

3 PCAPS — 4 — 14 — 1 PSHIELD — 13 — 2 — 13 ISOLATION — 16 — 14 — 15 — 16

Q1049 — CR1041 — R1047 330 — R1048 330 — CR1043 — C1045 1000pF — Q1031 — R3035 51 — R3025 330

.5AC SENSE 20 — LNSENSE 18

A66 P.S. SECONDARY BD.

4759-94

8560/8561/8562 SERVICE — D.C. OUTPUTS 38

P.S. D.C. OUTPUTS

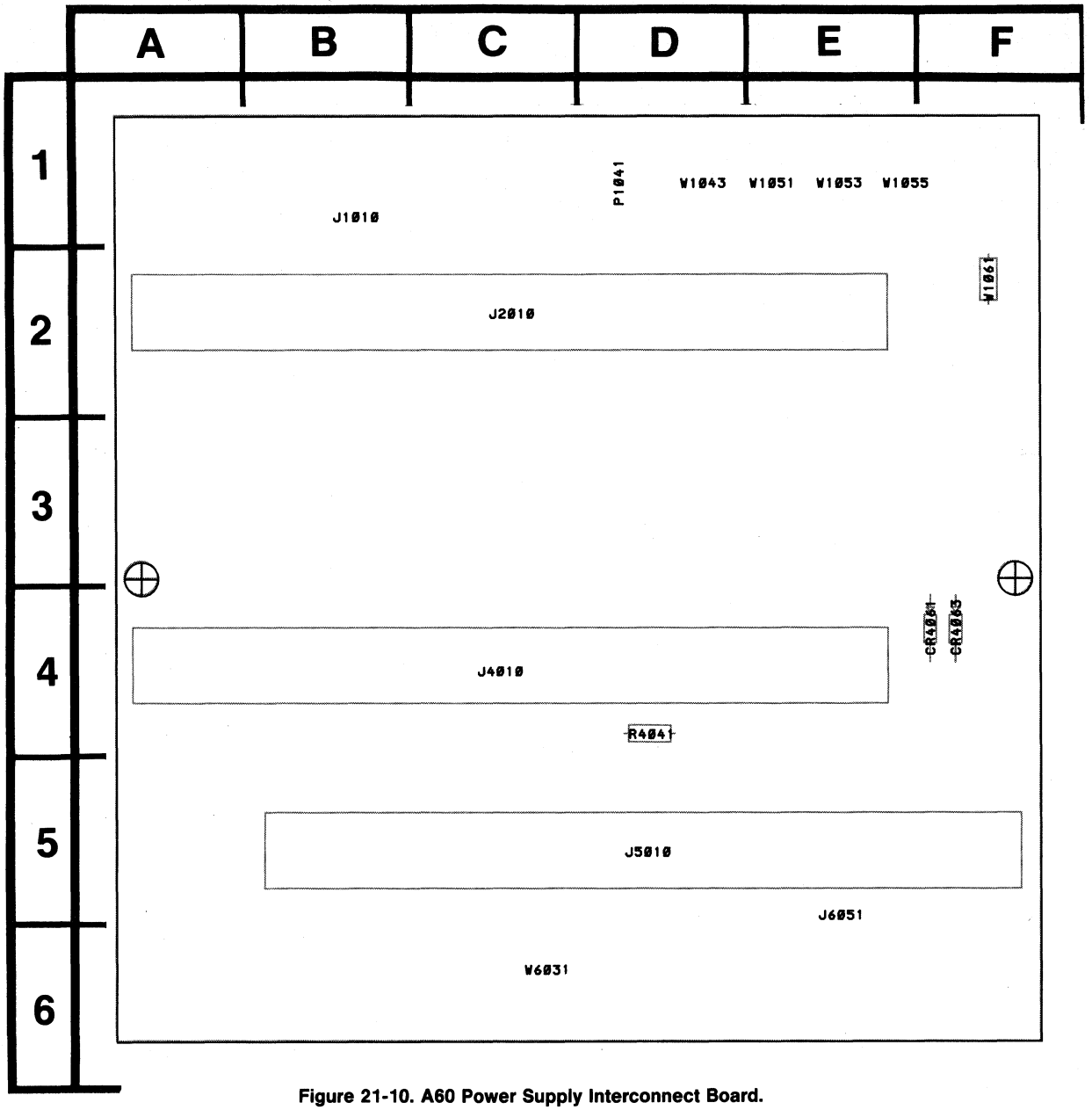
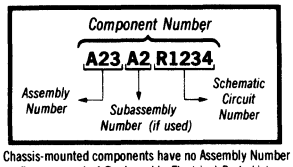


Figure 21-10. A60 Power Supply Interconnect Board.

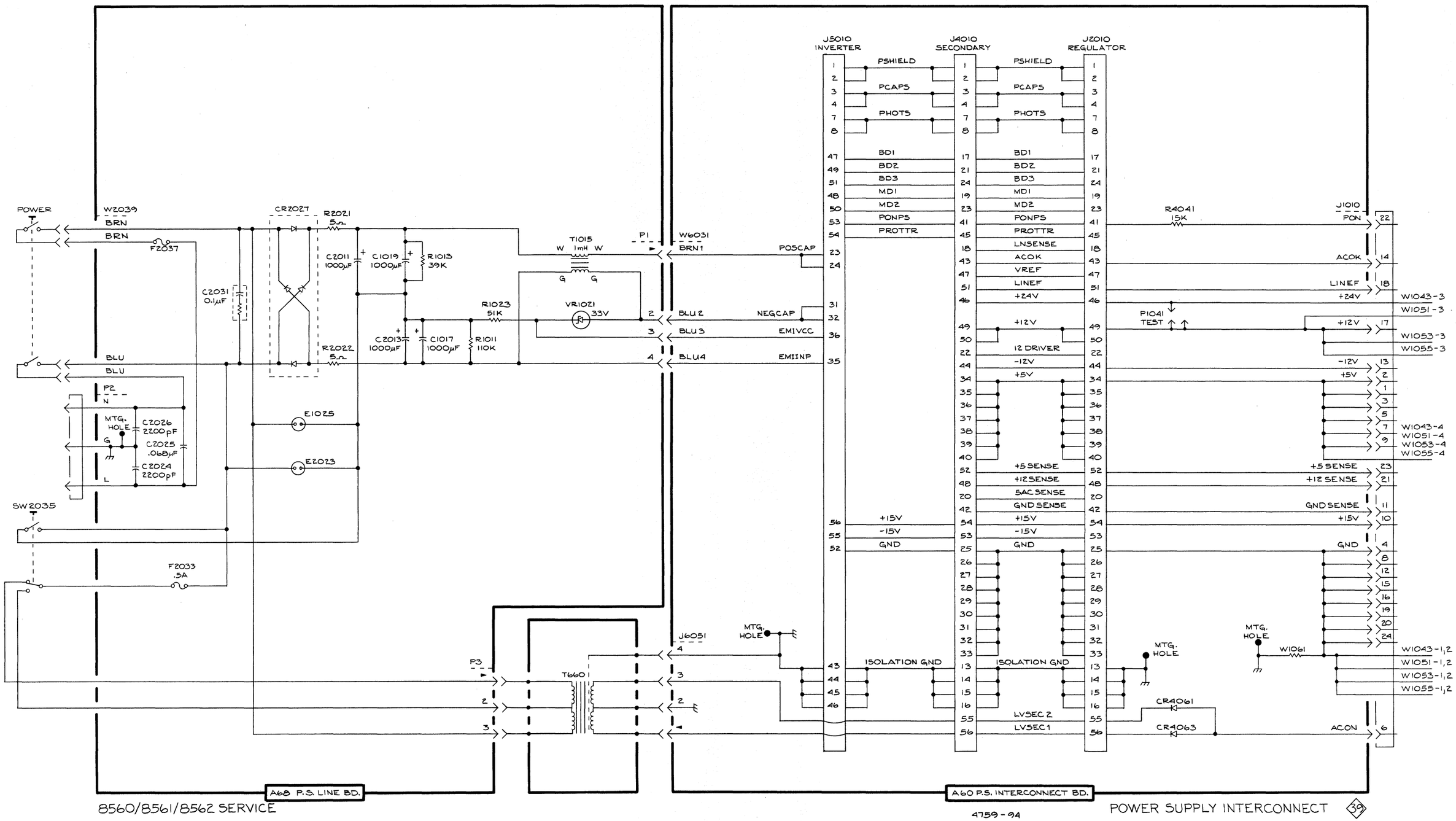
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

4759-54



8560/8561/8562 SERVICE

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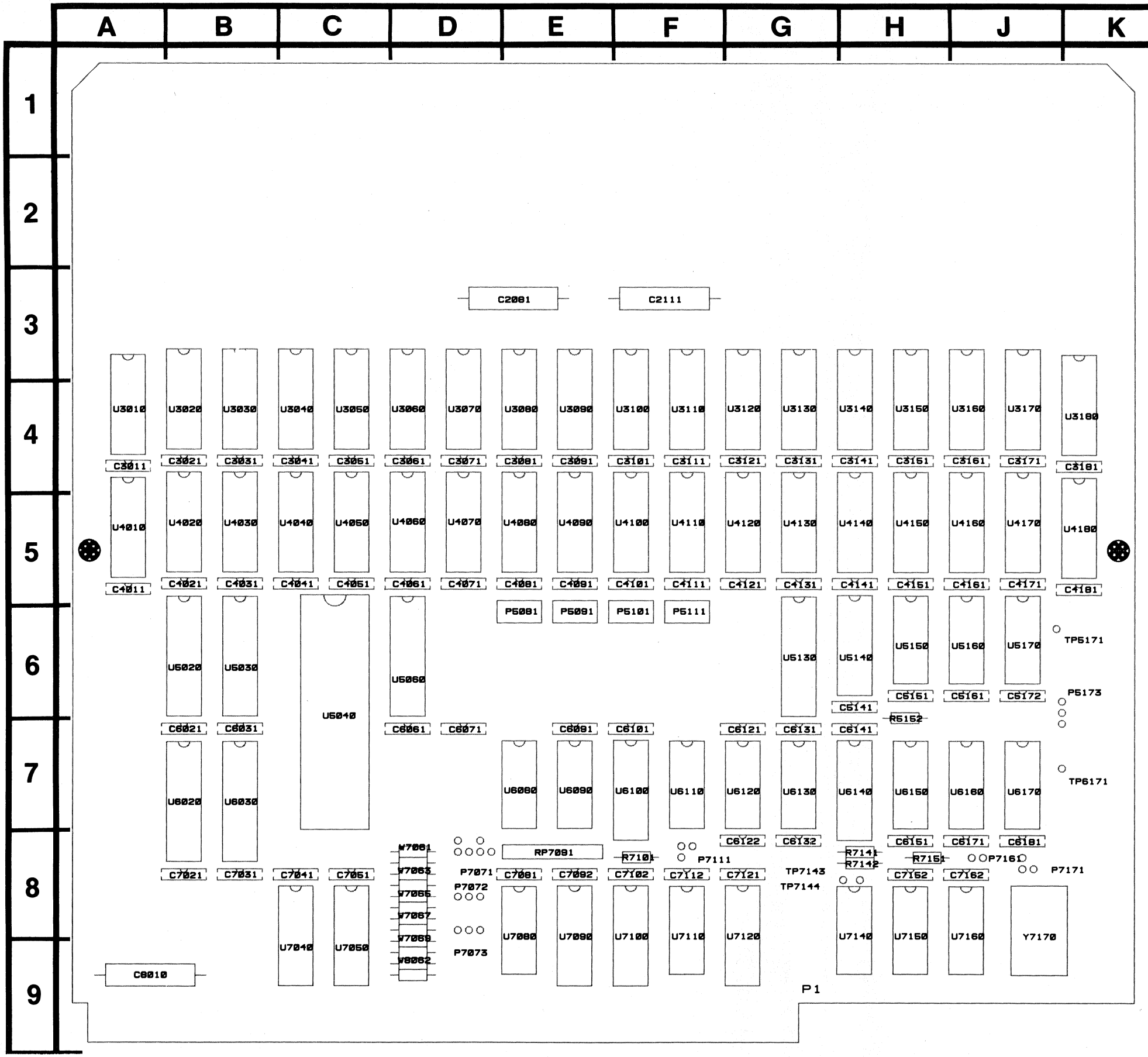
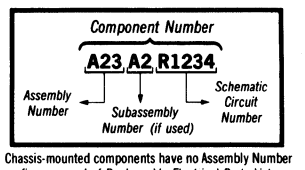
POWER SUPPLY INTERCONNECT 39

+5V
+15V
R1027 3.3K
R1026 3.3K
R1025 3.3K
R1024 3.3K
R1028 2K
RESTART
B A S1024 C
RUN/HALT
B A S1014 C
DC OFF/ON
S1045
U1010 74LSØØ
P/O J15
P/O P15
P/O P2
RST(L)
R(L)/H(H)
POWER ON(H)
P/O P2
P/O P15
P/O J15
ACON(L)
DS1032
AC ON
R1012 750
R1022 130
PROC BUSY(L)
DS1038
PROC BUSY
+5V
C1027 0.1
DS1052
ON
GND
+15V
+5V
A70 FRONT PANEL BOARD

256K-BYTE MEMORY
COMPONENT LOCATION



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

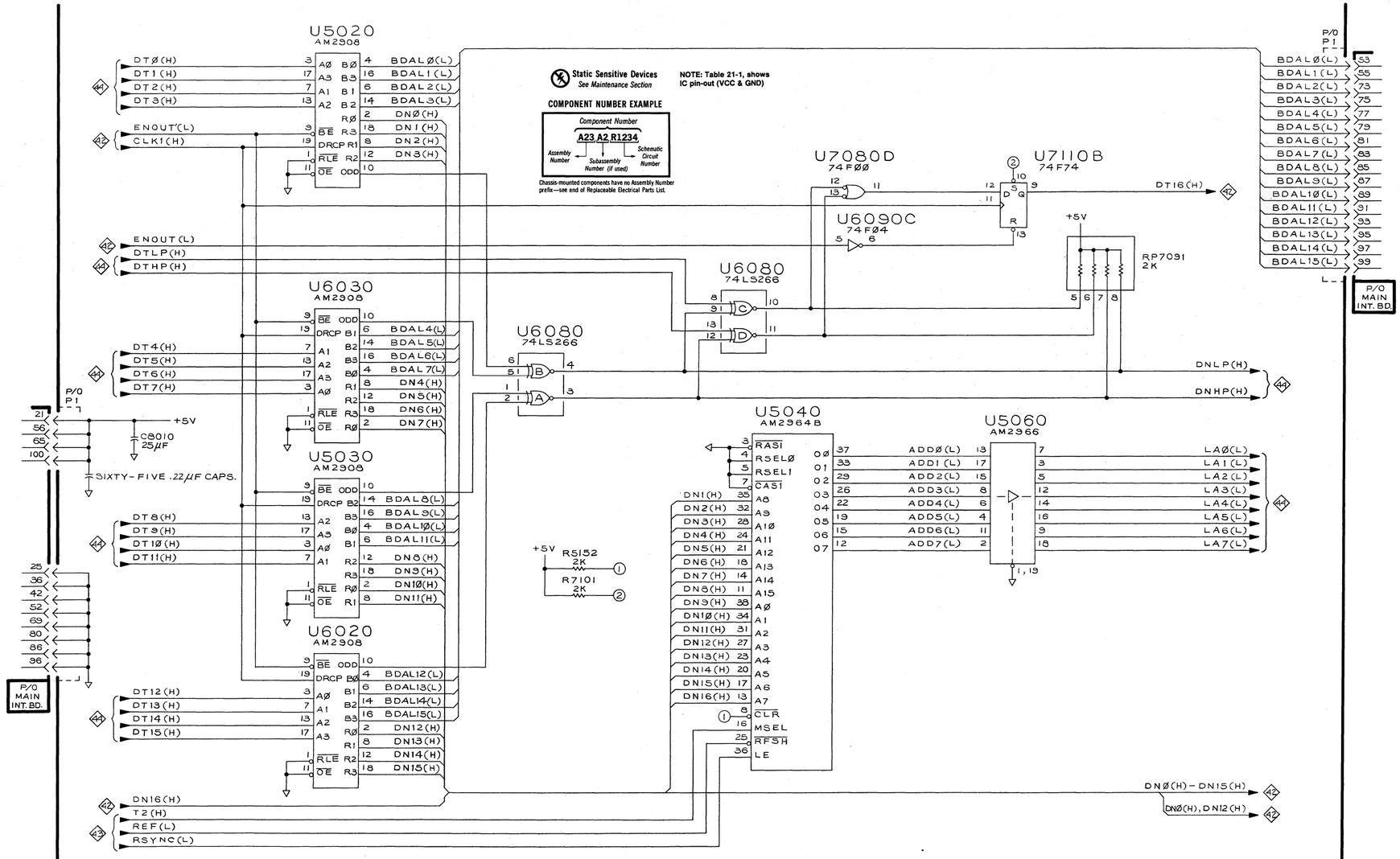
Static Sensitive Devices
See Maintenance Section

4759-55

Figure 21-11. A75 256K-Byte Memory Board.

Table 21-4
Sixty-Five 0.22μF
Decoupling Capacitors

C3011	C4161
C3021	C4171
C3031	C4181
C3041	C5141
C3051	C5151
C3061	C5161
C3071	C5172
C3081	C6021
C3091	C6031
C3101	C6061
C3111	C6071
C3121	C6091
C3131	C6101
C3141	C6121
C3151	C6122
C3161	C6131
C3171	C6132
C3181	C6141
C4011	C6151
C4021	C6171
C4031	C6181
C4041	C7021
C4051	C7031
C4061	C7041
C4071	C7051
C4081	C7081
C4091	C7092
C4104	C7102
C4111	C7112
C4121	C7121
C4131	C7152
C4141	C7162
C4151	



8560/8561/8562 SERVICE

BUS INTERFACE CIRCUITS (41)
(670-7951-00 & UP)

NOTE: Table 21-1, shows IC pin-out (VCC & GND)

Static Sensitive Devices
See Maintenance Section

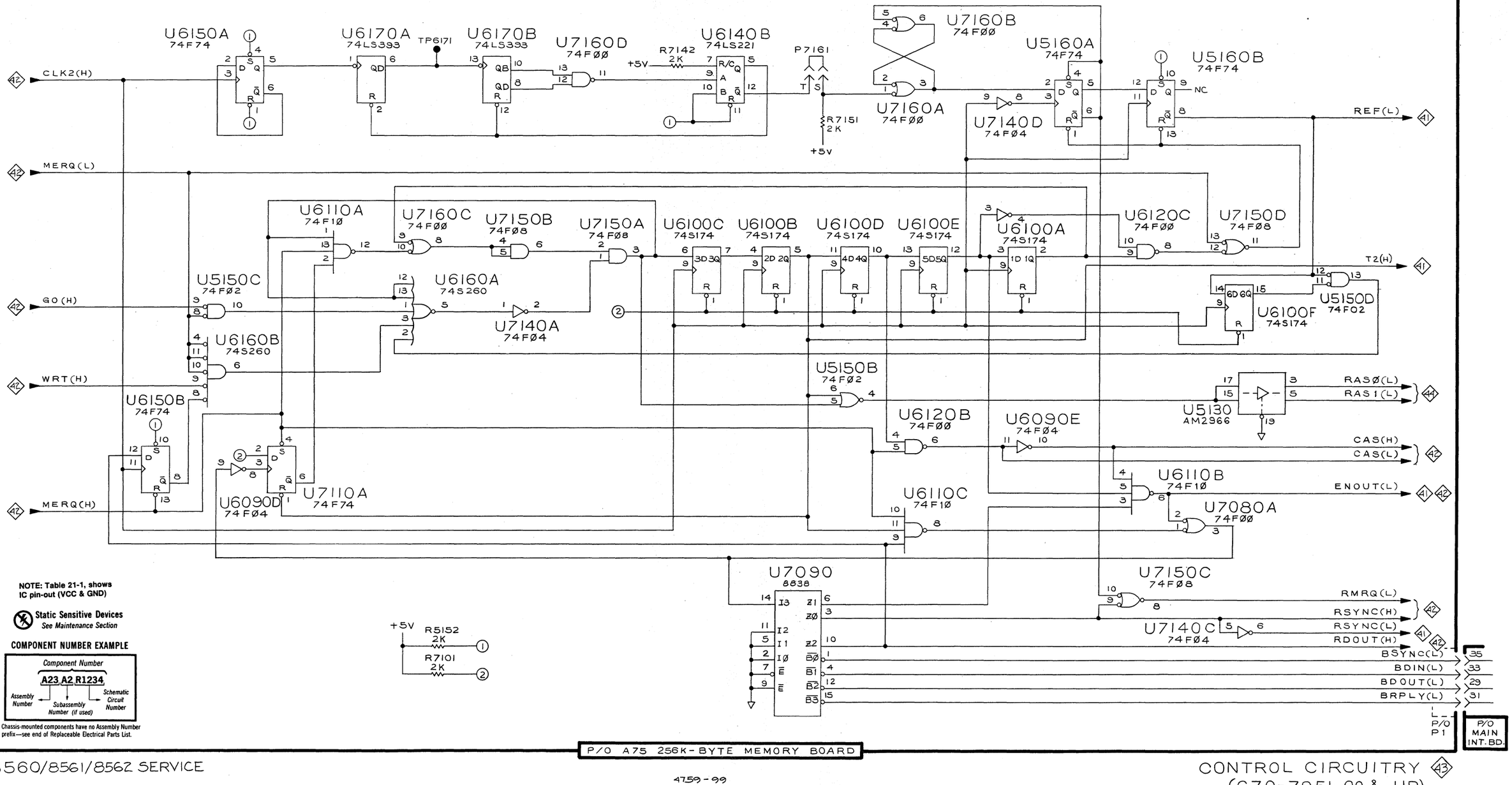
COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number | Subassembly Number (if used) | Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

RMRQ(L)
+5V
R5152 2K
R7101 2K
RP7091 2K
P7071(1)
P7071(2)
U7050 74F151
Y7170 25MHz
P7171
U7140 74F04
TP7143 TP7144
CLK2(H)
CLK1(H)
U5170A 74F74
U5170B 74F74
TP5171
GO(H)
MERQ(H)
MERQ(L)
U7080B 74F00
U7120 74S174
P7072
U7040 AM26S10
BBS7(L)
BDAL21(L)
BDAL20(L)
BDAL19(L)
U5140A 74F139
U5130 AM2966
CAS0(L)
CAS1(L)
WRT(H)
U6090A 74F04
U7080C 74F00
U5150A 74F02
U7140B 74F04
DN12(H)
DN0(H)
CAS(L)
RSYNC(H)
U7100 AM26S10
P5173
U6140A 74LS221
R7141 2K
U6130C 74F10
P7111
DT16(H)
P7073
RP7091 2K
ENOUT(L)
CAS(H)
RDOUT(H)
U6120 74F00
U6130 74F10
U5130 AM2966
U6090F 74F04
WL0(L)
WL1(L)
WH0(L)
WH1(L)
DN16(H)
BWTBT(L)
ENOUT'(L)
P/O MAIN INT. BD.
BDAL16(L)
BDAL17(L)
BDAL18(L)
BDAL19(L)
BDAL20(L)
BDAL21(L)

P/O A75 256K-BYTE MEMORY BOARD



NOTE: Table 21-1, shows IC pin-out (VCC & GND)

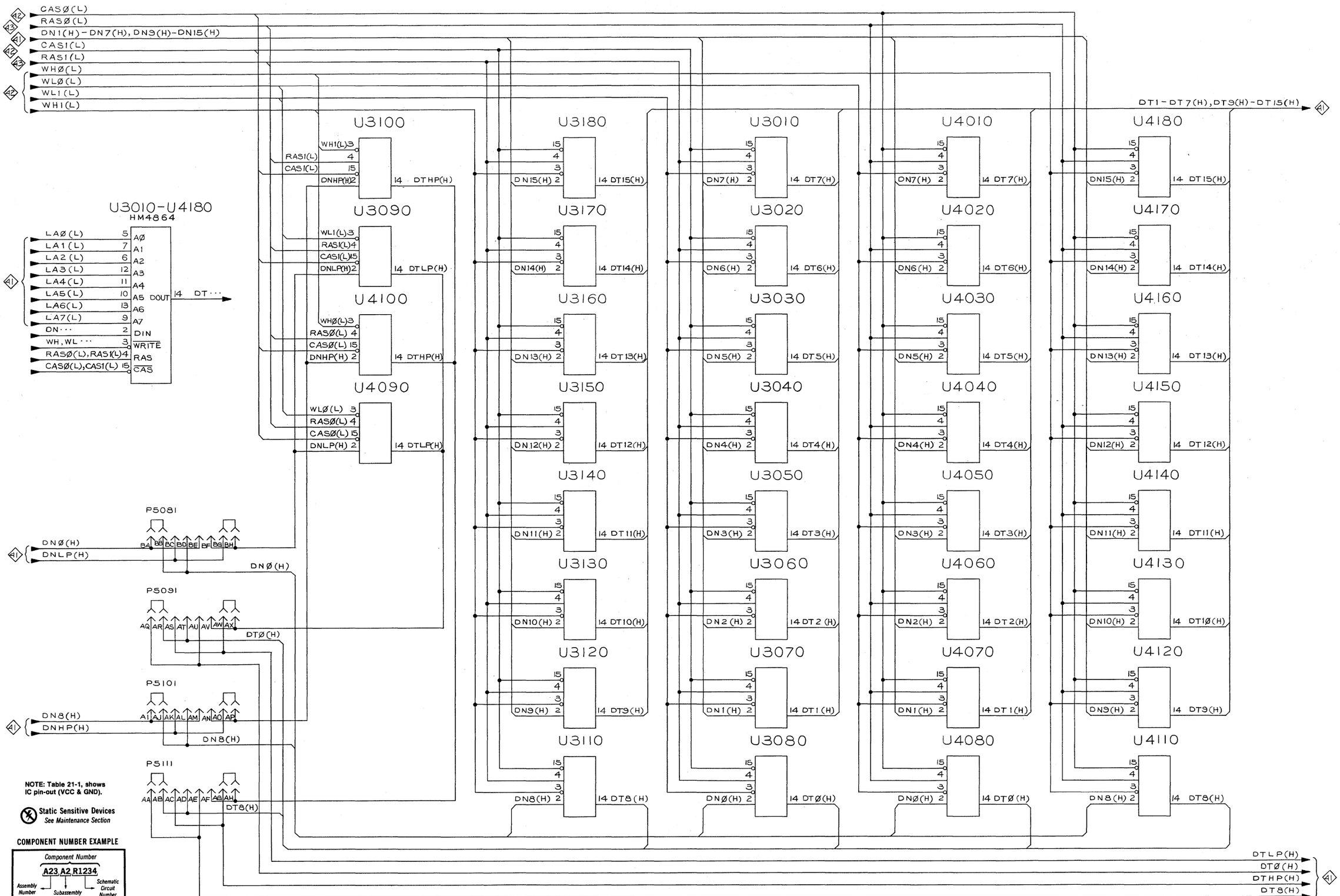
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A75 256K-BYTE MEMORY BOARD



NOTE: Table 21-1, shows IC pin-out (VCC & GND).

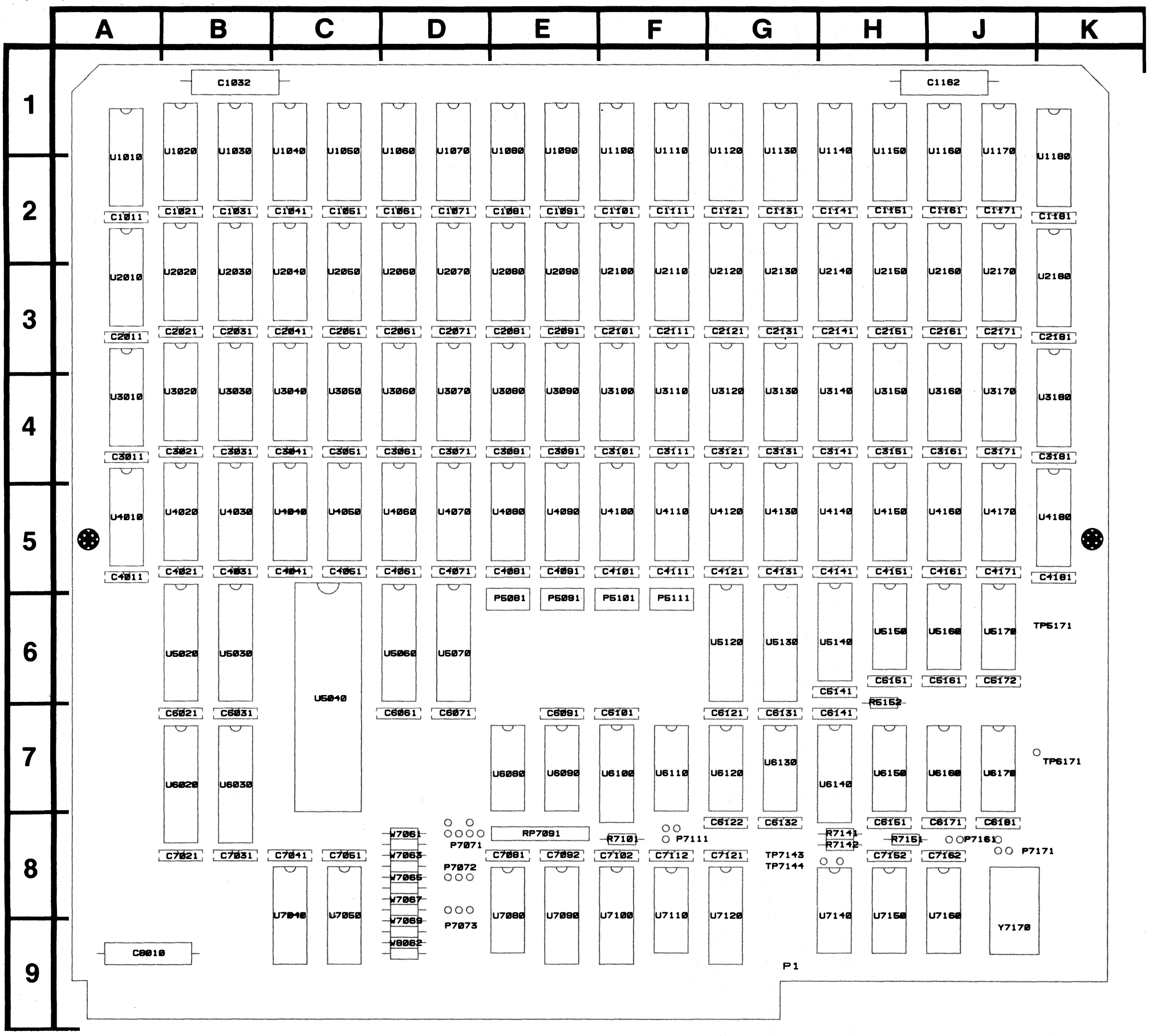
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

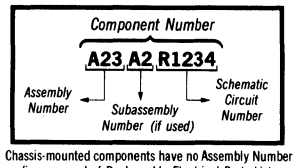
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A75 256K-BYTE MEMORY BOARD

512K-BYTE MEMORY COMPONENT LOCATION



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

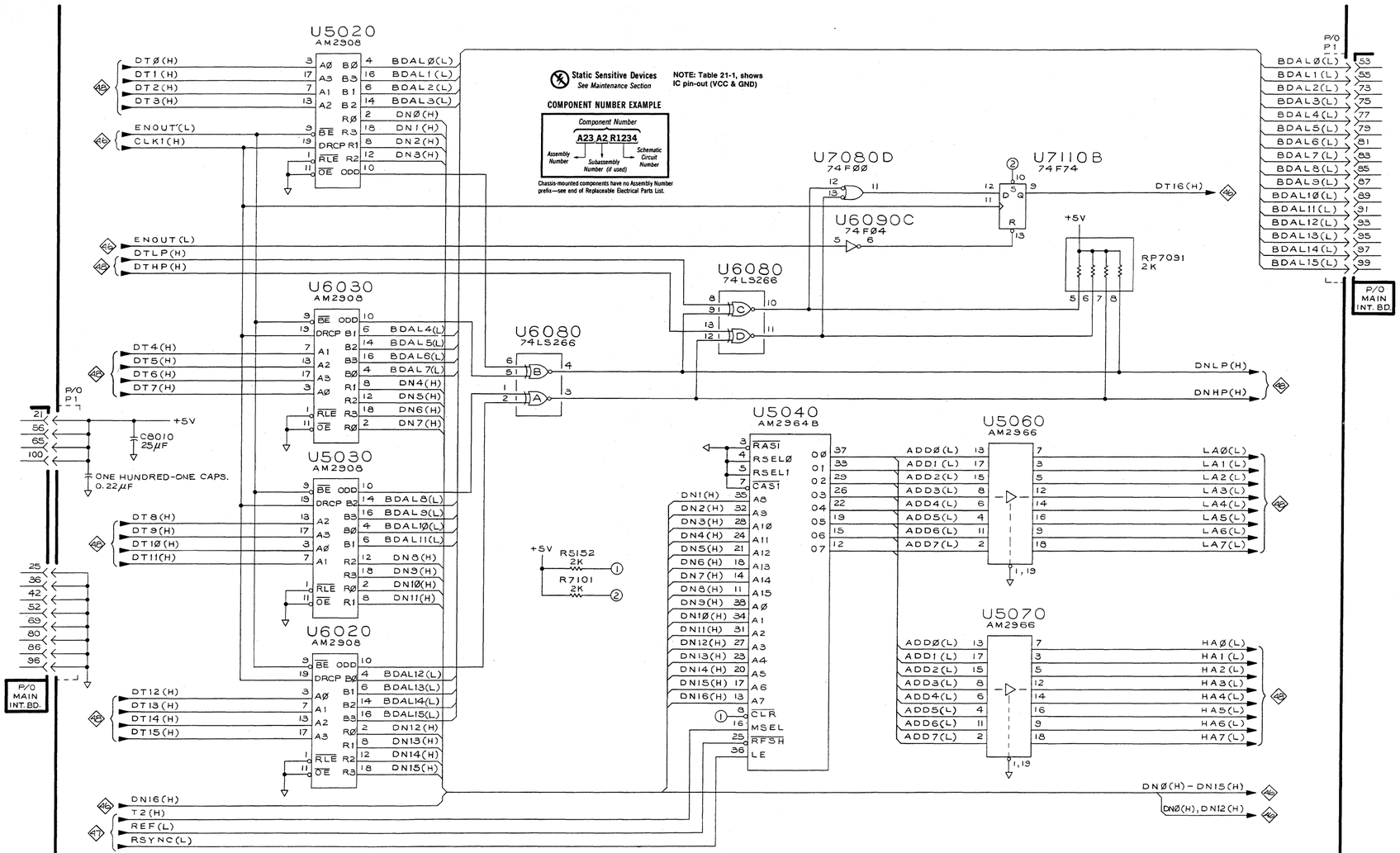
Static Sensitive Devices
See Maintenance Section

4759-56

Figure 21-12. A85 512K-Byte Memory Board.

Table 21-5
One Hundred-one 0.22μF
Decoupling Capacitors

C1011	C2171	C4161
C1021	C2181	C4171
C1031	C3011	C4181
C1041	C3021	C5141
C1051	C3031	C5151
C1061	C3041	C5161
C1071	C3051	C5172
C1081	C3061	C6021
C1091	C3071	C6031
C1101	C3091	C6061
C1111	C3101	C6071
C1121	C3111	C6091
C1131	C3121	C6101
C1141	C3131	C6121
C1151	C3141	C6122
C1161	C3151	C6131
C1171	C3161	C6132
C1181	C3171	C6141
C2011	C3181	C6151
C2021	C4011	C6171
C2031	C4021	C6181
C2041	C4031	C7021
C2051	C4041	C7031
C2061	C4051	C7041
C2071	C4061	C7051
C2081	C4071	C7081
C2091	C4081	C7092
C2101	C4091	C7102
C2111	C4101	C7112
C2121	C4111	C7121
C2131	C4121	C7152
C2141	C4131	C7162
C2151	C4141	C8010
C2161	C4151	



8560/8561/8562 SERVICE

4759-101

BUS INTERFACE CIRCUITS (670-7952-00 & UP)

NOTE: Table 21-1, shows IC pin-out (VCC & GND)

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23,A2,R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

RMRQ(L)
BBS7(L)
BDAL16(L)
BDAL17(L)
BDAL18(L)
BDAL19(L)
BDAL20(L)
BDAL21(L)
DN12(H)
DNØ(H)
CAS(L)
RSYNC(H)
DT16(H)
ENOUT(L)
CAS(H)
RDOUT(H)
DN16(H)
BWTBT(L)
ENOUT(L)
CLK2(H)
CLK1(H)
GO(H)
MERQ(H)
MERQ(L)
WRT(H)
CASØ(L)
CAS1(L)
CAS2(L)
CAS3(L)
WLØ(L)
WL1(L)
WL2(L)
WL3(L)
WHØ(L)
WH1(L)
WH2(L)
WH3(L)

+5V
R5152 2K
R7101 2K
RP7091 2K
R7141 2K
RP7091 2K

P7071(1)
P7071(2)
P7072
P7073
P7111
P7171
P/O P1

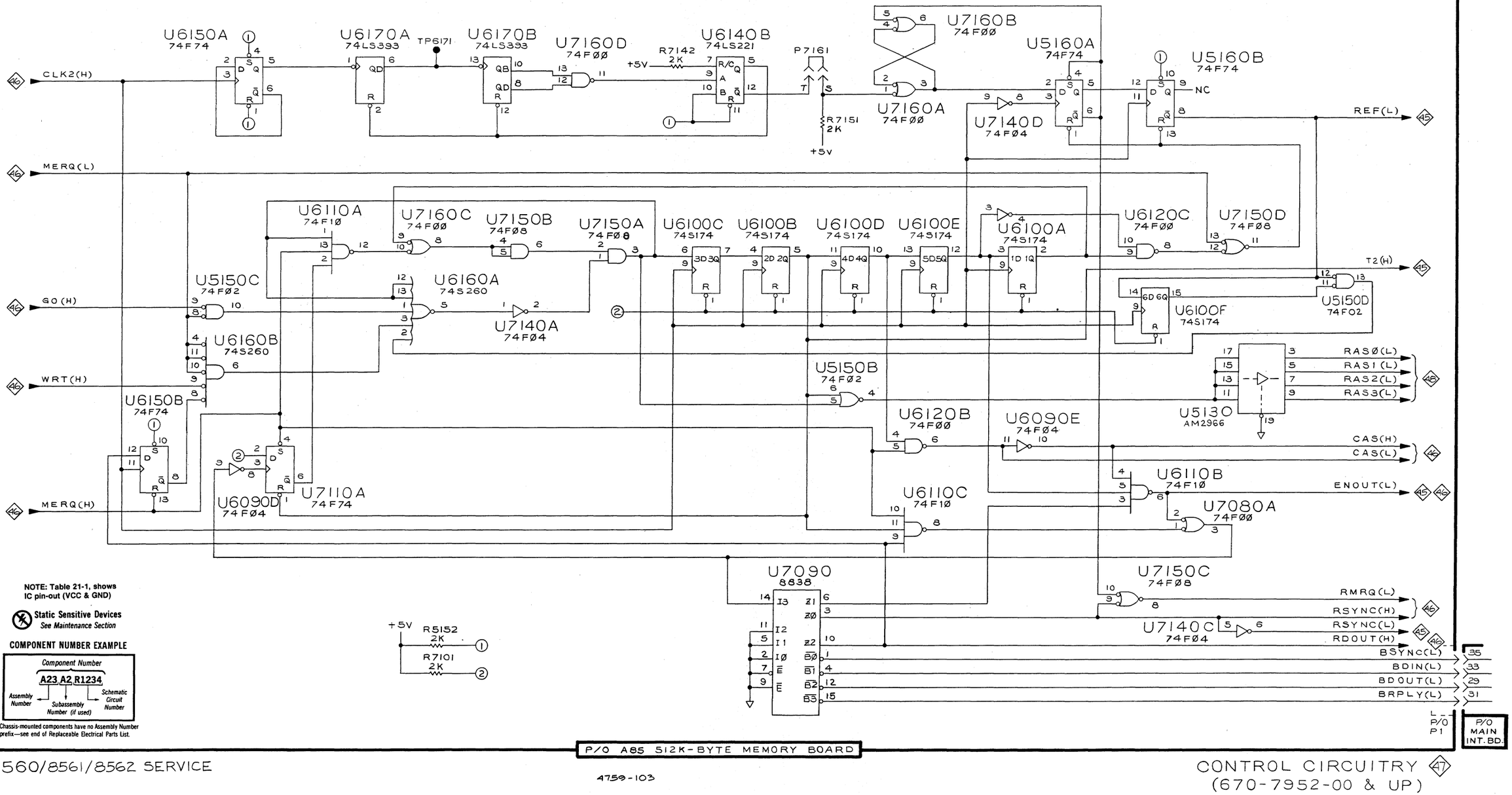
Y7170 25MHZ

U7050 74F151
U7080B 74FØØ
U7080C 74FØØ
U7120 74S174
U7140 74FØ4
U7040 AM26S1Ø
U7100 AM26S1Ø
U6090A 74FØ4
U6090F 74FØ4
U6140A 74LS221
U6120 74FØØ
U6130 74F1Ø
U5170A 74F74
U5170B 74F74
U5140A 74F139
U5130 AM2966
U5120 AM2966

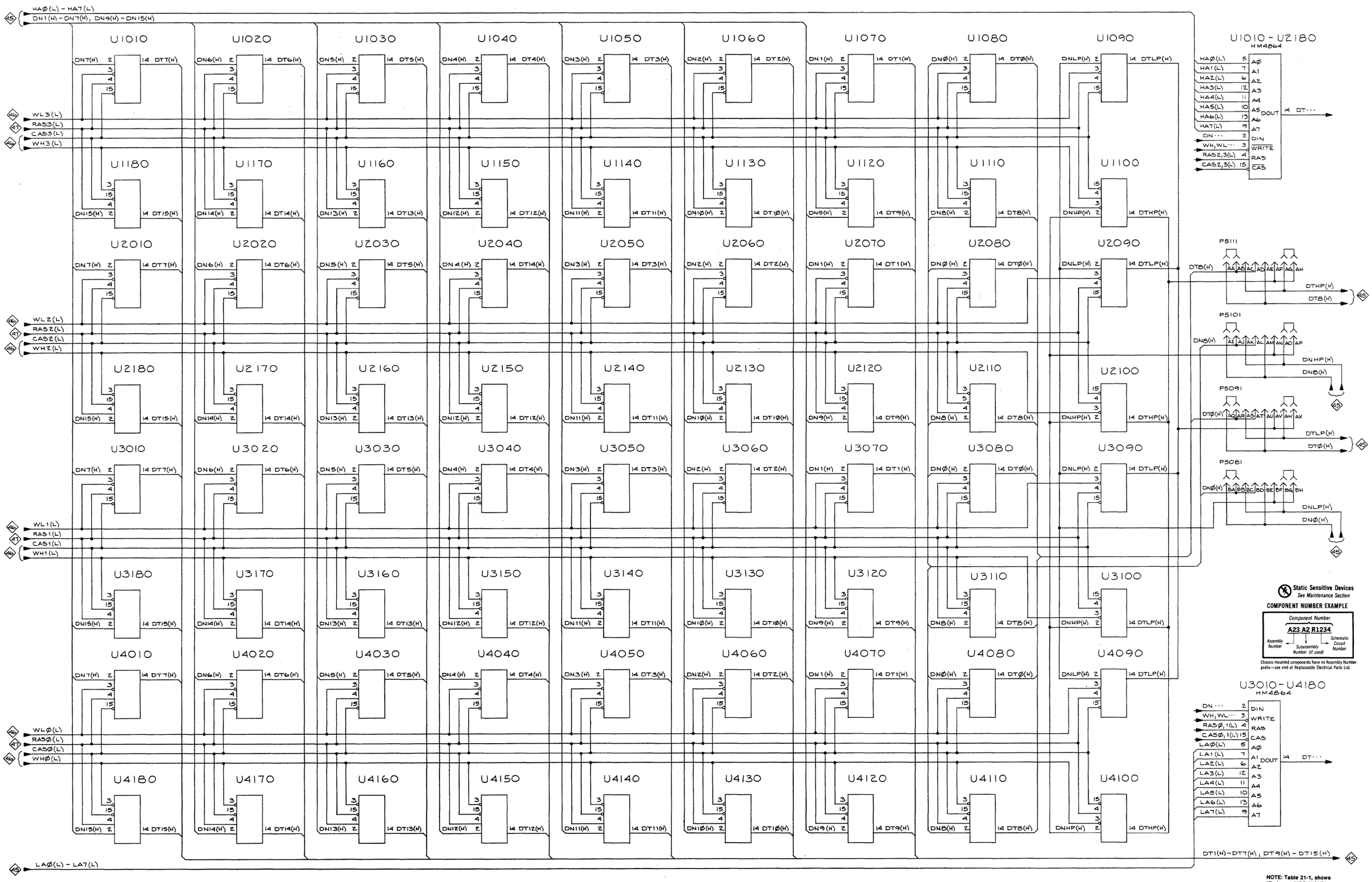
TP7143
TP7144
TP5171

P/O MAIN INT. BD.

P/O A85 512K-BYTE MEMORY BOARD



P/O A85 512K-BYTE MEMORY BOARD



P/O A85 512K-BYTE MEMORY BOARD

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AC	LINCOLN & ALLEN COMPANY	3460 NW INDUSTRIAL	PORTLAND, OR 97210
000BH	FAB-TEK	17 SUGAR HALLOW ROAD	DANBURY, CT 06810
000JA	J. PHILLIP INDUSTRIES INC.	5713 NORTHWEST HIGHWAY	CHICAGO, ILL 60646
000JL	H SCHURTER AG DIST PANEL COMPONENTS	2015 SECOND STREET	BERKELEY, CA 94170
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
06383	PANDUIT CORPORATION	17301 RIDGELAND	TINLEY PARK, IL 60477
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
15476	DIGITAL EQUIPMENT CORP.	146 MAIN ST.	MAYNARD, MA 01754
18565	CHOMERICS INC.	77 DRAGON COURT	WOBURN, MA 01801
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
26365	GRIES REPRODUCER CO., DIV. OF COATS AND CLARK, INC.	125 BEECHWOOD AVE.	NEW ROCHELLE, NY 10802
53387	MINNESOTA MINING AND MFG. CO., ELECTRO PRODUCTS DIVISION	3M CENTER	ST. PAUL, MN 55101
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
75037	MINNESOTA MINING & MFG CO. ELECTRO PRODUCTS DIV.	3M CENTER	ST. PAUL, MN 55101
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
87308	N. L. INDUSTRIES, INC., SOUTHERN SCREW DIV.	P. O. BOX 1360	STATESVILLE, NC 28677
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
S3109	C/O PANEL COMPONENTS CORP.	P.O. BOX 6626	SANTA ROSA, CA 95406
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
T1105	J PHILLIP INDUSTRIES INC	5713 NORTHWEST HIGHWAY	CHICAGO, IL 60646
T1372	ELECTRI-CORD MFG CO INC	312 E. MAIN ST.	WESTFIELD, PA 16950

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	672-1028-00			1		CKT BOARD ASSY:SD FRONT PANEL	80009	672-1028-00
-1	333-2890-00			1		.PANEL,FRONT:	80009	333-2890-00
-2	----- -----			1		.SWITCH,ROCKER:(SEE S1045 REPL)		
-3	----- -----			2		.SWITCH,TOGGLE:(SEE S1014 & S1024 REPL)		
-4	352-0157-00			3		.LAMPHOLDER:WHITE PLASTIC	80009	352-0157-00
-5	378-0602-00			1		.LENS,LIGHT:GREEN	80009	378-0602-00
	378-0602-01			2		.LENS,LIGHT:AMBER	80009	378-0602-01
-6	----- -----			3		.LT EMIT DIO:(SEE DS1032,1038,1052 REPL)		
-7	200-0935-00			1		.BASE,LAMPHOLDER:0.29 OD X 0.19 CASE	80009	200-0935-00
-8	214-2964-00			2		.SPRING,PANEL:COPPER-BERYLLIUM	80009	214-2964-00
						.**********(ATTACHING PARTS)**********		
-9	210-0586-00			4		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-10	343-0831-00			2		.RETAINER,SPR:ALUMINUM	80009	343-0831-00
						.**********(END ATTACHING PARTS)*********		
-11	----- -----			1		.CKT BOARD ASSY:FRONT PANEL(SEE A70 REPL)		
						.**********(ATTACHING PARTS)**********		
-12	211-0116-00			2		.SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
	----- -----			-		..CKT BOARD ASSY INCLUDES:		
-13	131-0608-00			8		..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	334-4471-00			1		..MARKER,IDENT:MKD 670-7474-XX	80009	334-4471-00
-14	386-4226-00			1		.SUBPANEL,FRONT:CONTROL	80009	386-4226-00
-15	175-2588-00			1		CA ASSY,SP,ELEC:8,22 AWG,9.0 L	80009	175-2588-00
-16	334-5462-00			1		MARKER,IDENT:8560 SOFTWARE DEVELOPEMENT	80009	334-5462-00
	----- -----			-		(8560 ONLY)		
	334-0011-00			1		MARKER,IDENT:MULTI-USER SOFTWARE DEVELOP	80009	334-0011-00
	----- -----			-		(8561 ONLY)		
	334-5704-00			1		MARKER,IDENT:MULTI-USER SOFTWARE DEVELOP	80009	334-5704-00
	----- -----			-		(8562 ONLY)		
-17	101-0101-00			1		TRIM.DECORATIVE:FACADE	80009	101-0101-00
-18	426-2012-00			1		FRAME SECT,CAB:OPEN FRONT	80009	426-2012-00
-19	390-0749-03			1		CABINET,BOTTOM:EARTH BROWN	80009	390-0749-03
	390-0937-00			1		CABINET,TOP:	80009	390-0937-00
-20	390-0750-03			2		CABINET,SIDE:EARTH BROWN	80009	390-0750-03
-21	124-0366-03			2		STRIP,TRIM:CORNER,BOTTOM,PVC,EARTH BR	80009	124-0366-03
-22	124-0367-03			2		STRIP,TRIM:CORNER,TOP,PVC,EARTH BROWN	80009	124-0367-03
-23	426-0015-00			2		FRAME SECT,CAB:TOP CORNER	80009	426-0015-00
						**********(ATTACHING PARTS)**********		
-24	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-25	426-0017-00			2		FRAME SECT,CAB:BOTTOM CORNER	80009	426-0017-00
						**********(ATTACHING PARTS)**********		
-26	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-27	348-0617-04			4		FOOT,CABINET:BOT,EARTH BROWN	80009	348-0617-04
-28	348-0776-00			4		GROMMET,PLASTIC:BLACK,OVAL,1.235 OVAL	80009	348-0776-00
-29	426-0072-00			2		FRAME SECT,CAB:SIDE	80009	426-0072-00
						**********(ATTACHING PARTS)**********		
-30	213-0801-00			8		SCREW,TPG,TF:8-32 X 0.312,TAPTITE,PNH	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	386-2905-00			1		SUDPANEL,FRONT:	80009	386-2905-00
						**********(ATTACHING PARTS)**********		
-2	211-0538-00			3		SCREW,MACHINE:6-32 X 0.312"100 DEG,FLH ST	83385	ORD BY DESCR
-3	211-0507-00			10		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-4	386-2920-00			1		SUPPORT,PLATE:HARD DISK,ALUMINUM	80009	386-2920-00
						**********(ATTACHING PARTS)**********		
-5	211-0507-00			6		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-6	175-9015-00			1		CA ASSY,SP,ELEC:34,28 AWG,8.5L,RIBBON	80009	175-9015-00
	175-9014-00			1		CA ASSY,SP,ELEC:34,28 AWG,12.0L,RIBBON	80009	175-9015-00
	----- -----			-		(8560 09/F09-8561 09-8561 10 ONLY)		
-7	175-9011-00			1		CA ASSY,SP,ELEC:20,28 AWG,8.0L,RIBBON	80009	175-9011-00
-8	119-1718-00			1		DISK DRIVE UNIT:5.25 WINCHESTER	80009	119-1718-00
	119-1778-00			1		DISK DRIVE UNIT:5.25 WINCHESTER,40 MEGABYT	80009	119-1778-00
-9	214-3523-00			4		PIN,LOCATING:5.25 HARD DISK	80009	214-3523-00
-10	407-2839-00			1		BRACKET,SUPPORT:5.25,HARD DISK,ALUMINUM	80009	407-2839-00
						**********(ATTACHING PARTS)**********		
-11	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-12	119-1717-00			1		FLEX DISK DRIVE:QUME TRACK 242	80009	119-1717-00
						**********(ATTACHING PARTS)**********		
-13	213-0938-00			6		SCREW,MACHINE:M4 X 8MM L,PNH,STL CD PL		
						**********(END ATTACHING PARTS)*********		
-14	407-2838-00			2		BRACKET SUPPORT:FLEXIBLE DISK,ALUMINUM	80009	407-2838-00
						**********(ATTACHING PARTS)**********		
-15	213-0538-00			6		SCREW,MACHINE:2BA X 1.0,HEX HD,STL DC PL		
						**********(END ATTACHING PARTS)*********		
-16	361-0627-00			1		SPACER,PLATE:LEFT,11.612 X 0.994 X 0.08 AL	80009	361-0627-00
						**********(ATTACHING PARTS)**********		
-17	211-0507-00			7		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-18	----- -----			1		CKT BOARD ASSY:XEBEC CONTROL(SEE A80 REPL)		
						**********(ATTACHING PARTS)**********		
-19	213-0213-00			4		SCREW,MACHINE:0.25-20 X 1.0,SKT HD,STL	83385	ORD BY DESCR
-20	211-0008-00			4		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-21	361-0046-00			4		SPACER,POST:0.5 L W/4-40 THRU,ACETAL	80009	361-0046-00
						**********(END ATTACHING PARTS)*********		
-22	252-0571-00			1		NEOPRENE EXTR:CHAN,0.234 X 0.156	85471	DIE#1353
-23	352-0482-00			1		HOLDER,CA,TIE:0.75 SQ,STICKY BACK,PLASTIC	06383	ABMM-A
-24	343-0549-00			1		STRAP,TIEDOWN,E:0.091 W X 3.62 L,ZYTEL	80009	343-0549-00
-25	441-1212-00			1		CHASSIS,CENTER:	80009	441-1212-00
						**********(ATTACHING PARTS)**********		
-26	211-0507-00			3		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.CHASSIS,CENTER INCLUDES:		
-27	351-0087-00			3		.GUIDE,CKT BOARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-28	441-1141-00			1		CHAS,CARD CAGE:FRONT	80009	441-1141-00
						**********(ATTACHING PARTS)**********		
-29	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-30	334-0130-00			1		MARKER,IDENT:CARD CAGE	80009	334-0130-00
-31	407-2844-00			1		BRACKET,CKT BD:ALUMINUM,CARD CAGE	80009	407-2844-00
						**********(ATTACHING PARTS)**********		
-32	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-33	351-0675-01			2		GUIDE,CKT BOARD:DELRIN,7.0L	80009	351-0675-01
-34	441-1209-00			1		CHAS,CARD CAGE:REAR,ALUMINUM	80009	441-1209-00
						**********(ATTACHING PARTS)**********		
-35	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-36	351-0675-02			16		GUIDE,CKT BOARD:DELRIN,7.0L	80009	351-0675-02

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-37	361-0626-00			1		SPACER,PLATE:RIGHT,12.325 X 1.562,AL	80009	361-0626-00
						**********(ATTACHING PARTS)**********		
-38	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-39	----- -----			1		CKT BOARD ASSY:IO ADAPTER(SEE A35 REPL)		
						**********(ATTACHING PARTS)**********		
-40	211-0601-00			6		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	ORD BY DESCR
-41	385-0080-00			2		SPACER,POST:0.437 L W/6-32 THD THRU,AL	80009	385-0080-00
-42	361-1018-00			4		SPACER,POST:0.518 L,W/6-32 THD THRU,AL	80009	361-1018-00
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.CKT BOARD ASSY INCLUDES:		
-43	198-4498-00			8		.WIRE SET,ELEC:	80009	198-4498-00
-44	131-0608-00			196		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-45	136-0729-00			15		.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-46	214-2518-00			1		.HEAT SINK,XSTR:T0-220 OR T0-202	000BH	106B-B-HT
-47	131-2406-00			1		.CONN,RCPT,ELEC:CKT BD,2 X 17,MALE	75037	3494-2003
-48	131-2409-00			1		.CONN,RCPT,ELEC:CKT BD,2 X 25,MALE	75037	3496-2003
-49	441-0305-00			1		CHAS,MICROCMPTR:MAINFRAME	80009	441-0305-00
						**********(ATTACHING PARTS)**********		
-50	211-0507-00			10		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-51	175-9135-00			1		CA ASSY,SP,ELEC:50,28 AWG,12.5L,RIBBON	80009	175-9135-00
-52	198-4462-00			1		WIRE SET,ELEC:	80009	198-4462-00
-53	175-4541-00			1		CA ASSY,SP,ELEC:34,28 AWG,7.625L,RIBBON	80009	175-4541-00
-54	175-4538-00			1		CA ASSY,SP,ELEC:50,28 AWG,5.0L,RIBBON	80009	175-4538-00
-55	----- -----			1		CKT BOARD ASSY:BACKPLANE(SEE A10 REPL)		
						**********(ATTACHING PARTS)**********		
-56	211-0601-00			5		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.CKT BOARD ASSY INCLUDES:		
-57	----- -----			2		.CONN,RCPT,ELEC:(SEE A10J3,J4 REPL)		
-58	131-0993-00			14		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-59	----- -----			1		.TERM. SET,PIN:(SEE A10J19 REPL)		
-60	----- -----			1		.CONN,RCPT,ELEC:(SEE A10J5 REPL)		
-61	----- -----			2		.TERM. SET,PIN:(SEE A10J14 REPL)		
-62	----- -----			1		.CONN,RCPT,ELEC:(SEE A10J16 REPL)		
-63	----- -----			1		.CONN,RCPT,ELEC:(SEE A10J17 REPL)		
-64	----- -----			1		.CONN,RCPT,ELEC:(SEE A10J15 REPL)		
-65	----- -----			8		.CONN,RCPT,ELEC:(SEE A10J6 THRU J13 REPL)		
						.**********(ATTACHING PARTS)**********		
-66	211-0016-00			16		.SCREW,MACHINE:4-40 X 0.625,PNH,STL,CD PL	83385	ORD BY DESCR
-67	210-0586-00			16		.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-68	----- -----			1		.CONTACT SET,ELE:(SEE A10J2 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	----- -----			1		CKT BOARD ASSY:UTILITY(SEE A20 REPL)		
-2	105-0792-00			2		.EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-3	214-1337-00			2		..PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-4	253-0176-00			1		.TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	ORD BY DESCR
-5	136-0751-00			2		.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-6	131-0608-00			24		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-7	131-0993-00			3		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-8	----- -----			1		CKT BOARD ASSY:I/O PROCESSOR(SEE A30 REPL)		
-9	105-0792-00			2		.EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-10	214-1337-00			2		..PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-11	131-0608-00			110		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-12	131-0993-00			22		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
	131-0993-07			7		.LINK,TERM.CONNE:2 WIRE VIOLET	00779	850100-7
-13	136-0755-00			10		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-14	136-0757-00			4		.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-15	253-0176-00			1		.TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	ORD BY DESCR
-16	----- -----			1		CKT BOARD ASSY:256K/512K(SEE A75/A85 REPL)		
-17	105-0792-00			2		.EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-18	214-1337-00			2		..PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-19	131-0608-00			59		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		.(8560/8561 ONLY)		
	131-0608-00			56		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		.(8562 ONLY)		
-20	131-0993-00			16		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
	----- -----			-		.(8560/8561 ONLY)		
	131-0993-00			15		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
	----- -----			-		.(8562 ONLY)		
-21	----- -----			1		CKT BOARD ASSY:MASS STOR CONT(SEE A45 REPL)		
-22	105-0792-00			2		.EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-23	214-1337-00			2		..PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-24	136-0755-00			2		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-25	136-0813-00			1		.SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS	19613	268-5400-00-1102
-26	131-0608-00			19		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	131-0993-00			7		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-28	214-0579-00			3		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-29	253-0176-00			1		.TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	ORD BY DESCR
-30	----- -----			1		.CONN REPT,ELEC:(SEE A45J2 REPL)		
-31	175-9013-00			1		CA ASSY,SP,ELEC:50,28 AWG,9,5L,RIBBON	80009	175-9013-00
	----- -----			-		(A45J2 TO A80)		
-32	----- -----			1		CKT BOARD ASSY:CPU/KDJ11-A(SEE A15 REPL)		
-33	367-0183-00			2		.PULL,CKT CARD:	15476	0937
-34	131-1343-00			1		.TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136

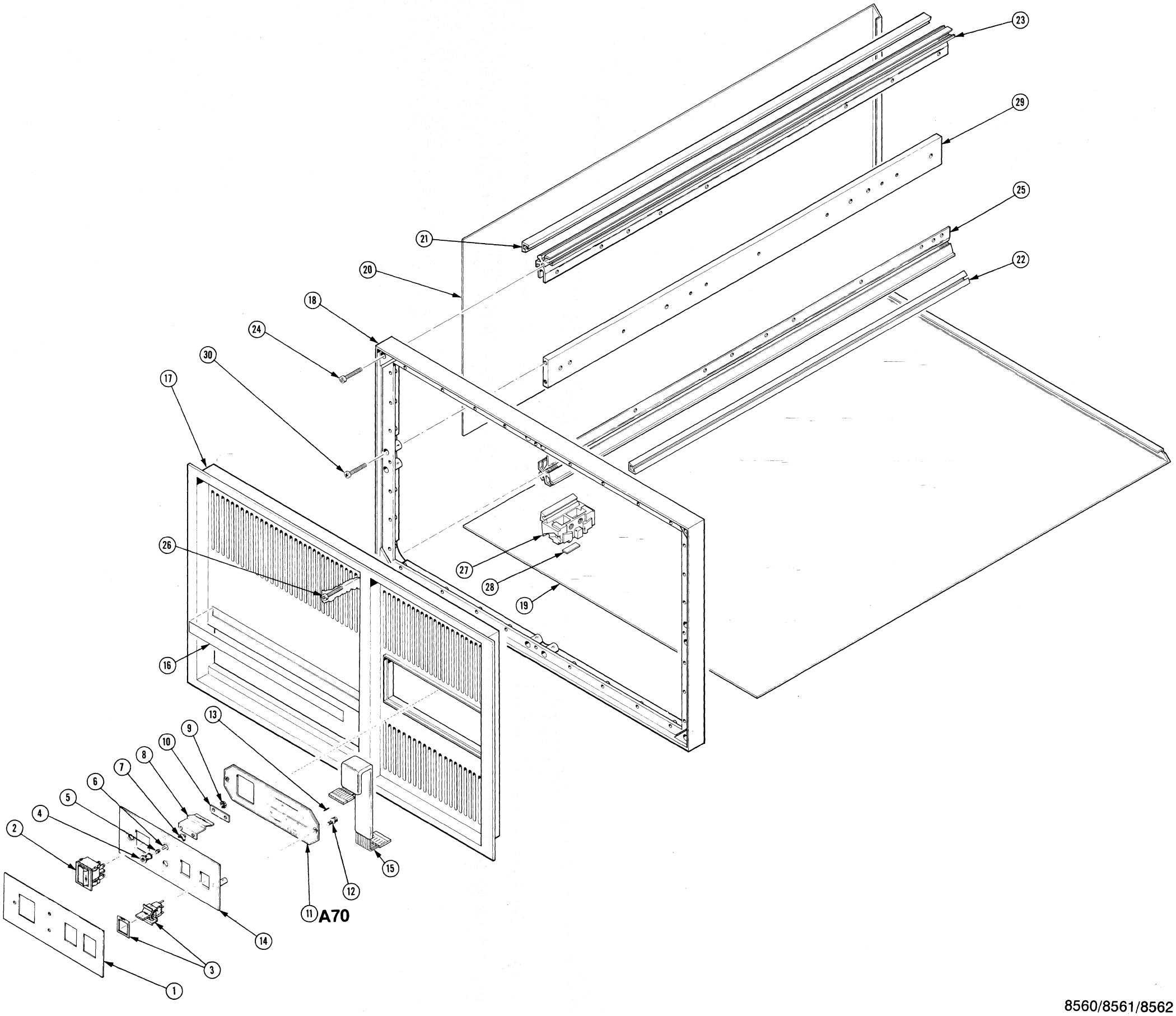

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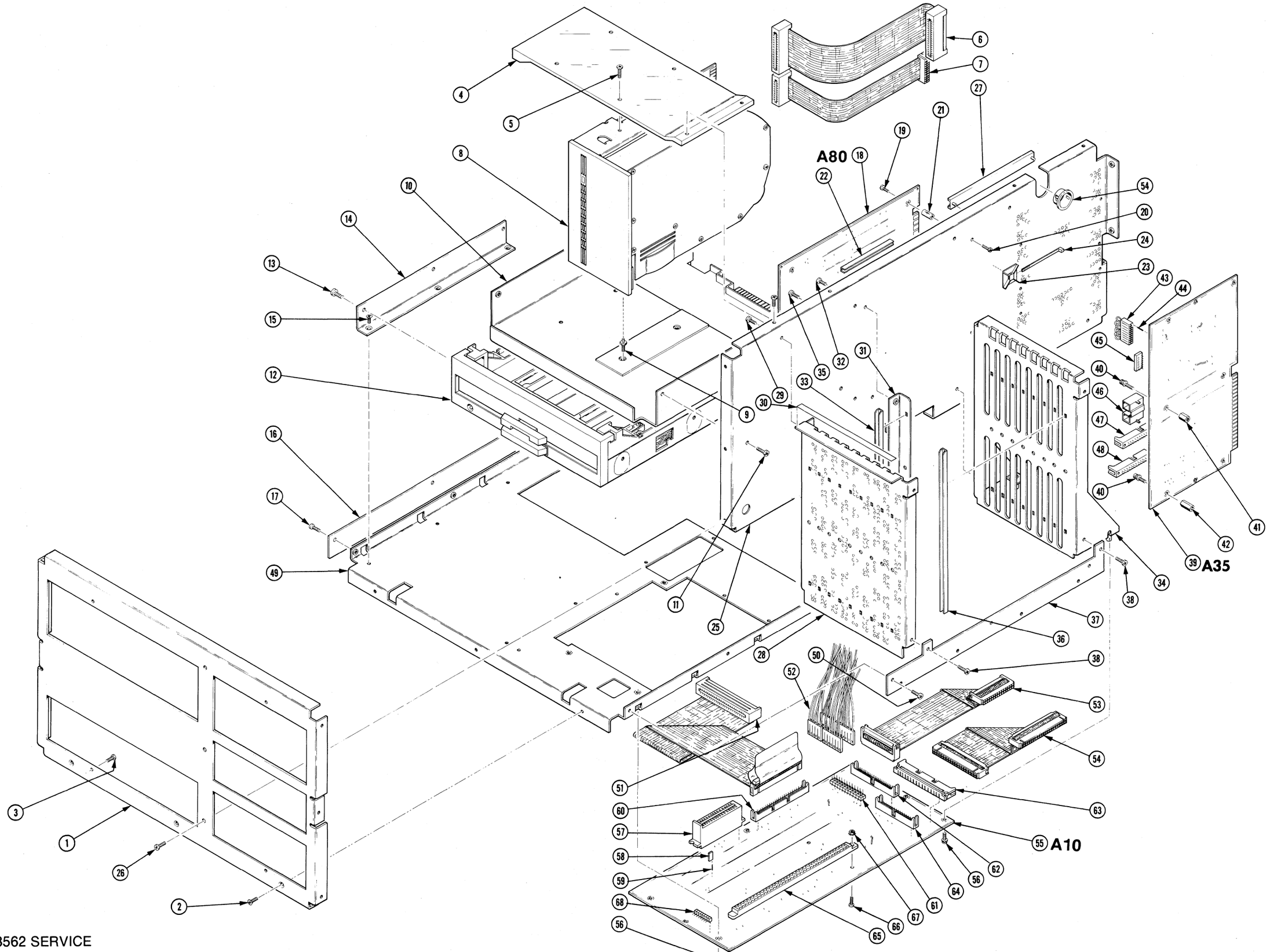
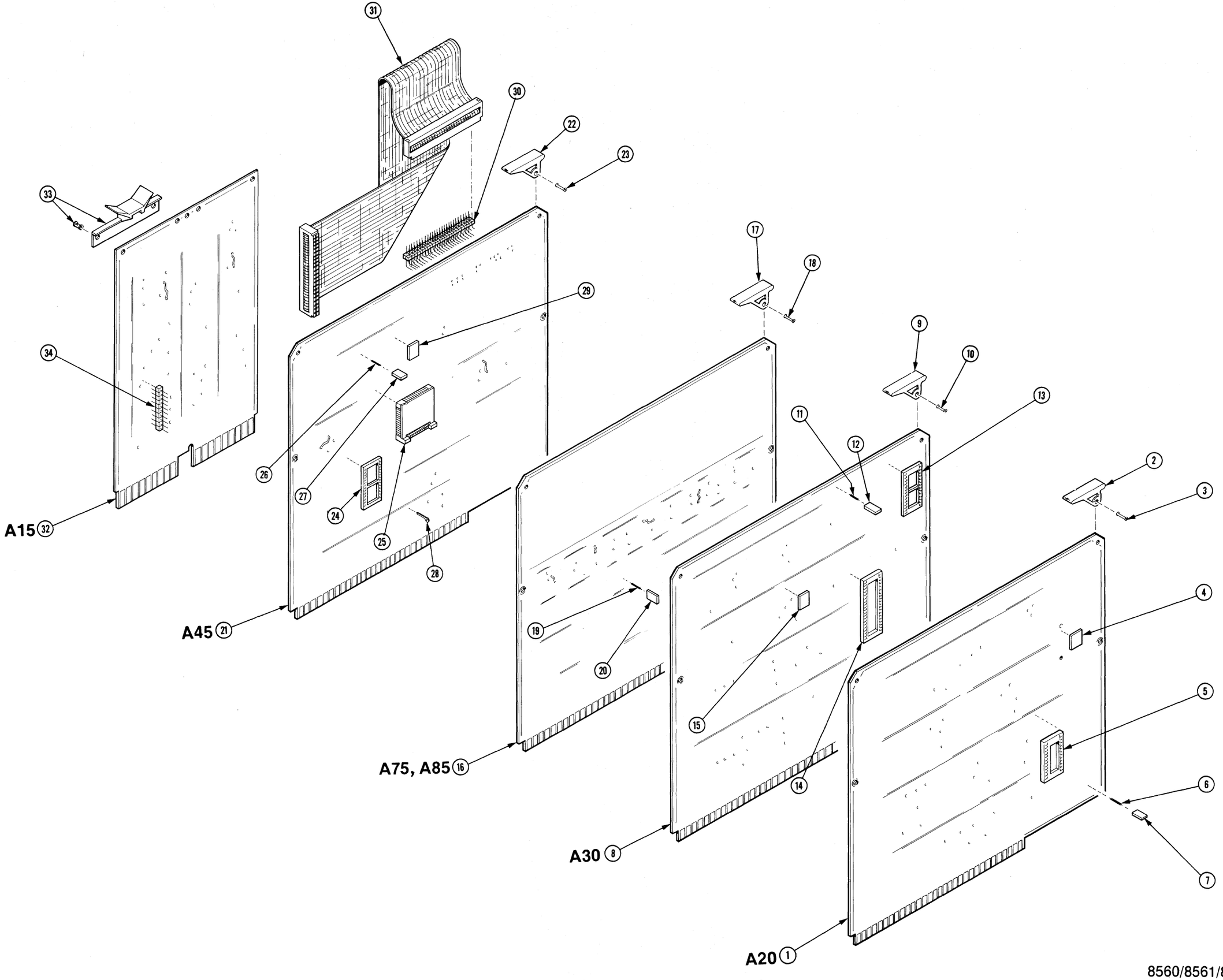
FIGURE 2 CARD CAGE

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A75, A85 16
A30 8
A20 1

FIGURE 4 POWER SUPPLY & REAR

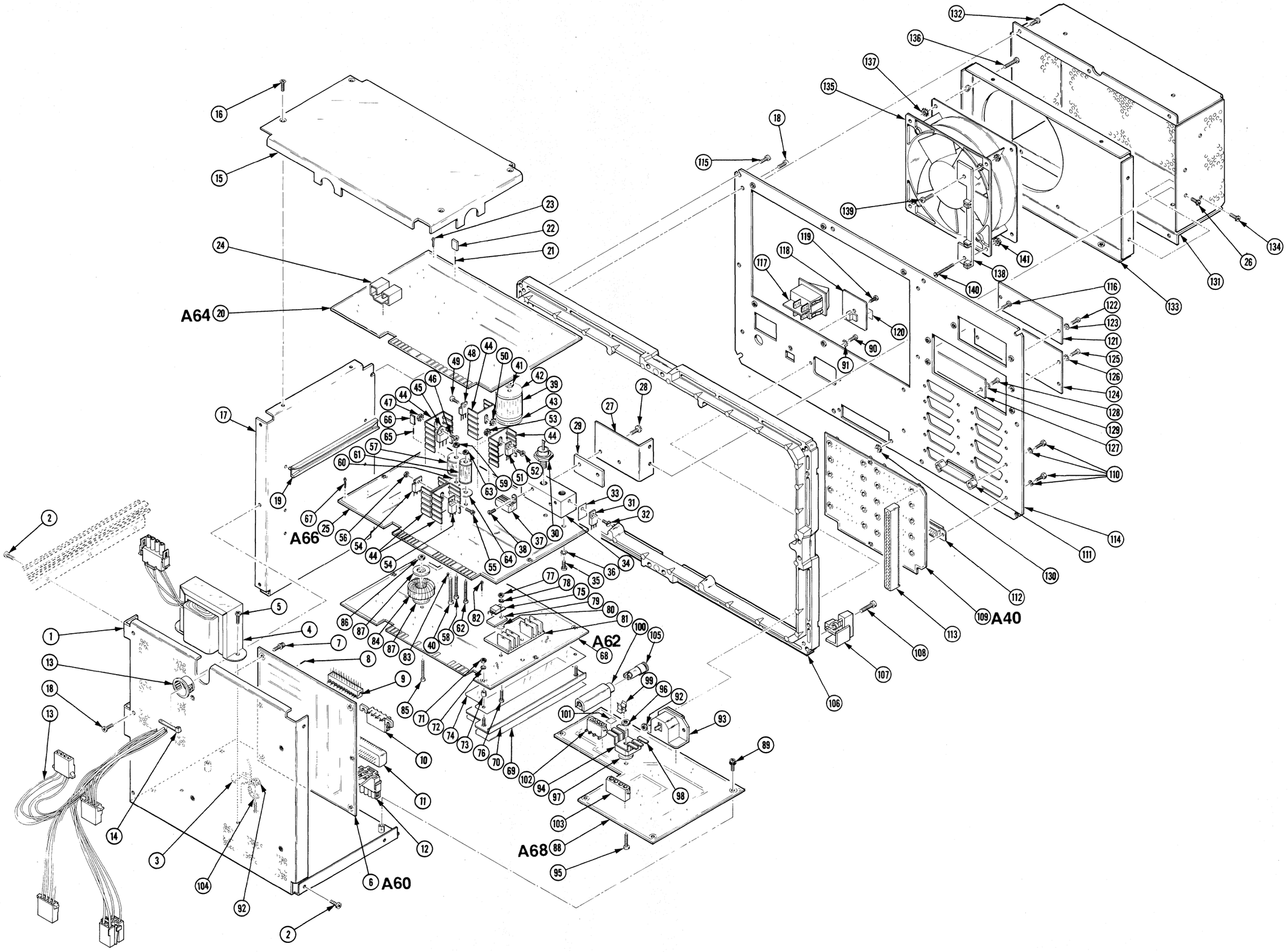

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
4-39	----- -----			1	.COIL,RF::(SEE A66L4091 REPL)		
					.**********(ATTACHING PARTS)**********		
-40	211-0553-00			1	.SCREW,MACHINE:6-32 X 1.5 INCH,PNH STL	83385	ORD BY DESCR
-41	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
-42	210-0054-00			1	.WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD S	83385	ORD BY DESCR
-43	210-1007-00			1	.WASHER,FLAT:0.156 ID X 0.062 THK	80009	210-1007-00
					.**********(END ATTACHING PARTS)*********		
-44	214-2953-00			5	.HEAT SINK,XSTR:TO-220,AL	80009	214-2953-00
-45	----- -----			1	.TRANSISTOR:(SEE A66Q4109 REPL)		
					.**********(ATTACHING PARTS)**********		
-46	211-0507-00			1	.SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-47	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-48	----- -----			1	.SEMICOND,DEVICE:(SEE A66CR4082 REPL)		
					.**********(ATTACHING PARTS)**********		
-49	211-0507-00			1	.SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-50	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-51	----- -----			1	.MICROCIRCUIT,LI:(SEE A66U4060 REPL)		
					.**********(ATTACHING PARTS)**********		
-52	211-0507-00			1	.SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-53	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-54	----- -----			2	.TRANSISTOR:(SEE A66Q2063,2073 REPL)		
					.**********(ATTACHING PARTS)**********		
-55	211-0012-00			1	.SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	ORD BY DESCR
-56	210-0406-00			1	.NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
					.**********(END ATTACHING PARTS)*********		
-57	----- -----			1	.COIL,RF:(SEE A66L3083 REPL)		
					.**********(ATTACHING PARTS)**********		
-58	211-0019-00			1	.SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	ORD BY DESCR
-59	210-0586-00			1	.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-60	210-0917-00			1	.WASHER,NONMETAL:0.191 ID X 0.625 INCH OD	86445	ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-61	----- -----			1	.COIL,RF:(SEE A66L3061 REPL)		
					.**********(ATTACHING PARTS)**********		
-62	211-0019-00			1	.SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	ORD BY DESCR
-63	210-0586-00			1	.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-64	210-0917-00			1	.WASHER,NONMETAL:0.191 ID X 0.625 INCH OD	86445	ORD BY DESCR
					.**********(END ATTACHING PARTS)*********		
-65	131-0608-00			10	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-66	131-0993-00			5	.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-67	----- -----			5	TERM,TEST POINT:(SEE A66TP1 THRU TP5 REPL)		
-68	----- -----			1	CKT BOARD ASSY:PS INVERTER(SEE A62 REPL)		
-69	334-5587-00			1	.MARKER,IDENT:CAUTION	80009	334-5587-00
-70	337-3154-00			1	.SHIELD,ELEC:1.750 X 5.55	80009	337-3154-00
					.**********(ATTACHING PARTS)**********		
-71	220-0627-00			3	.NUT,PLAIN,HEX.:2-56 X 0.156 INCH,BRS	73743	10002-56-101
-72	210-0053-00			3	.WASHER,LOCK:INTL,0.092 ID X 0.175"OD,S	83385	ORD BY DESCR
-73	361-0226-00			3	.SPACER,SLEEVE:0.11L X 0.093 ID,BRS NP	80009	361-0226-00
					.**********(END ATTACHING PARTS)*********		
-74	342-0684-00			1	.INSULATOR,PLATE:ELECTRICAL,POLYESTER	80009	342-0684-00
-75	----- -----			2	.TRANSISTOR:(SEE A62Q2010,Q3010 REPL)		
					.**********(ATTACHING PARTS)**********		
-76	211-0014-00			2	.SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	ORD BY DESCR
-77	210-0406-00			2	.NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-78	210-0054-00			2	.WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD S	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)*********		
-79	342-0420-00			2	.INSULATOR,PLATE:TRANSISTOR,PORCELAIN	80009	342-0420-00
-80	342-0577-00			2	.INSULATOR,XSTR:PLASTIC	80009	342-0577-00
-81	214-3315-00			1	.HT SK,MICROCKT:ALUMINUM,BLACK ANODIZED	80009	214-3315-00
-82	----- -----			2	.TERM,TEST POINT:(SEE A62TP5085,5086 REPL)		
-83	136-0252-07			3	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-84	----- -----			1		.COIL,RF:(SEE A62L2071 REPL)		
						.**********(ATTACHING PARTS)**********		
-85	211-0018-00			1		.SCREW,MACHINE:4-40 X 0.875 PNH,STL	83385	ORD BY DESCR
-86	210-0586-00			1		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-87	200-0848-00			2		.CAP,INSERT,KNOB:0.765 OD X 0.118 H,BLACK	80009	200-0848-00
						.**********(END ATTACHING PARTS)*********		
-88	----- -----			1		CKT BOARD ASSY:PS LINE(SEE A68 REPL)		
						**********(ATTACHING PARTS)**********		
-89	211-0601-00			4		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	ORD BY DESCR
-90	211-0012-00			2		SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	ORD BY DESCR
-91	211-0002-00			2		SCREW,MACHINE:2-56 X 0.625,RDH,STL POZ		
-92	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	----- -----			-		.CKT BOARD ASSY INCLUDES:		
-93	----- -----			1		.CONN,RCPT,ELEC:(SEE A68P2 REPL)		
-94	----- -----			1		.SEMICOND DEVICE:(SEE A68CR2027 REPL)		
						.**********(ATTACHING PARTS)**********		
-95	211-0513-00			1		.SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	ORD BY DESCR
-96	210-0457-00			1		.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-97	342-0577-00			1		.INSULATOR,XSTR:PLASTIC	80009	342-0577-00
-98	214-3258-00			1		.HEAT SINK,XSTR:ALUMINUM	80009	214-3258-00
-99	344-0326-00			2		.CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-100	204-0906-00			1		.BODY,FUSE HLDR:3AG AND 5 X 20 MM FUSES	000JL	FAU 031.3573
-101	334-4452-00			1		.MARKER,IDENT:0.5A,250V,FAST	80009	334-4452-00
-102	----- -----			1		.CONN,RCPT,ELEC:(SEE A68P3 REPL)		
-103	----- -----			1		.CONN,RCPT,ELEC:(SEE A68P1 REPL)		
-104	195-9637-00			1		.LEAD,ELECTRICAL:18 AWG,4.5L,5-4	80009	195-9637-00
-105	200-2264-00			1		CAP.,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
	----- -----			-		(STANDARD ONLY)		
	200-2265-00			1		CAP,FUSEHOLDER:5 X 20MM FUSES	S3629	FEK 031.1663
	----- -----			-		(OPTIONS A1,A2,A3,A4,A5 ONLY)		
-106	426-1891-00			1		FRAME,CABINET:REAR,10.5 X FULL BACK	80009	426-1891-00
-107	348-0544-05			4		RTNR,CAB. COVER:CORNER,EARTH BROWN,PC	80009	348-0544-05
						**********(ATTACHING PARTS)**********		
-108	213-0908-00			4		SCREW,TPG,TF:8-32 X 0.625	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-109	----- -----			1		CKT BOARD ASSY:(SEE A40 REPL)		
						**********(ATTACHING PARTS)**********		
-110	214-3106-00			10		HARDWARE KIT:JACK SOCKET	53387	3341-1S
						**********(END ATTACHING PARTS)*********		
-111	200-2707-00			4		.COVER,HOLE:CONNECTOR,POLYCARBONATE	80009	200-2707-00
	----- -----			-		.(8560 ONLY)		
	200-2707-00			6		.COVER,HOLE:CONNECTOR,POLYCARBONATE	80009	200-2707-00
	----- -----			-		.(8561 ONLY)		
-112	----- -----			6		.CONN,RCPT,ELEC:(SEEA40J8011,8021,8031,		
	----- -----			-		.8041,8051,8101 REPL)		
	----- -----			4		.CONN,RCPT,ELEC:(SEEA40J8011,8021,8051,		
	----- -----			-		.8101 REPL)		
	----- -----			10		.CONN,RCPT,ELEC:(SEEA40J8011,8021,8031,		
	----- -----			-		.8041,8051,8061,8071,8081,8101 REPL)		
-113	----- -----			1		.CONN,RCPT,ELEC:(SEE A40J8001 REPL)		
	334-5231-00			1		.MARKER,IDENT:MKD 670-8162-XX	80009	334-5231-00
	----- -----			-		.(8561 ONLY)		
	334-4828-00			1		.MARKER,IDENT:MKD 670-7307-XX	80009	334-4828-00
	----- -----			-		.(8562 ONLY)		
-114	333-1859-00			1		PANEL,REAR:	80009	333-1859-00
						**********(ATTACHING PARTS)**********		
-115	211-0510-00			10		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	ORD BY DESCR
-116	211-0507-00			5		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-117	----- -----			1		SWITCH,ROCKER:(SEE S650 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-118	200-2729-00			1		COVER,PROT:	80009	200-2729-00
						**********(ATTACHING PARTS)**********		
-119	211-0008-00			1		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-120	334-5268-00			1		MARKER,IDENT:90-130 VAC,8A FAST	80009	334-5268-00
	----- -----			-		(STANDARD ONLY)		
	334-5269-00			1		MARKER,IDENT:180-250 VAC,4A FAST	80009	334-5269-00
	----- -----			-		(OPTIONS A1,A2 A3,A4,A5 ONLY)		
-121	386-4718-00			1		PLATE,CONN:ALUMINUM	80009	386-4718-00
						**********(ATTACHING PARTS)**********		
-122	211-0097-00			2		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-123	210-0002-00			2		WASHER,LOCK:EXTERNAL #2	78189	1102-01
						**********(END ATTACHING PARTS)*********		
-124	386-4719-00			1		PLATE,CONN:BLANK,ALUMINUM	80009	386-4719-00
						**********(ATTACHING PARTS)**********		
-125	211-0097-00			4		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-126	210-0002-00			4		WASHER,LOCK:EXTERNAL #2	78189	1102-01
						**********(END ATTACHING PARTS)*********		
-127	386-5127-00			1		PLATE,CONN:ALUMINUM	80009	386-5127-00
						**********(ATTACHING PARTS)**********		
-128	211-0097-00			2		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
-129	210-0002-00			2		WASHER,LOCK:EXTERNAL #2	78189	1102-01
-130	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-131	200-2682-00			1		COVER,FAN:ALUMINUM	80009	200-2682-00
						**********(ATTACHING PARTS)**********		
-132	211-0507-00			6		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-133	407-2788-00			1		BRACKET,FAN:ALUMINUM	80009	407-2788-00
						**********(ATTACHING PARTS)**********		
-134	211-0534-00			8		SCR,ASSEM,WSHR:6-32 X 0.312 INCH,PNH STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-135	----- -----			1		FAN,TUBEAXIAL:(SEE B610 REPL)		
						**********(ATTACHING PARTS)**********		
-136	211-0511-00			4		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	ORD BY DESCR
-137	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-138	351-0724-00			1		GUIDE,CKT BD:NYLON,5.1L	80009	351-0724-00
						**********(ATTACHING PARTS)**********		
-139	211-0513-00			1		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	ORD BY DESCR
-140	211-0643-00			1		SCREW,MACHINE:6-32 X 1.0,RDH,NYL,SLOT	83385	ORD BY DESCR
-141	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		

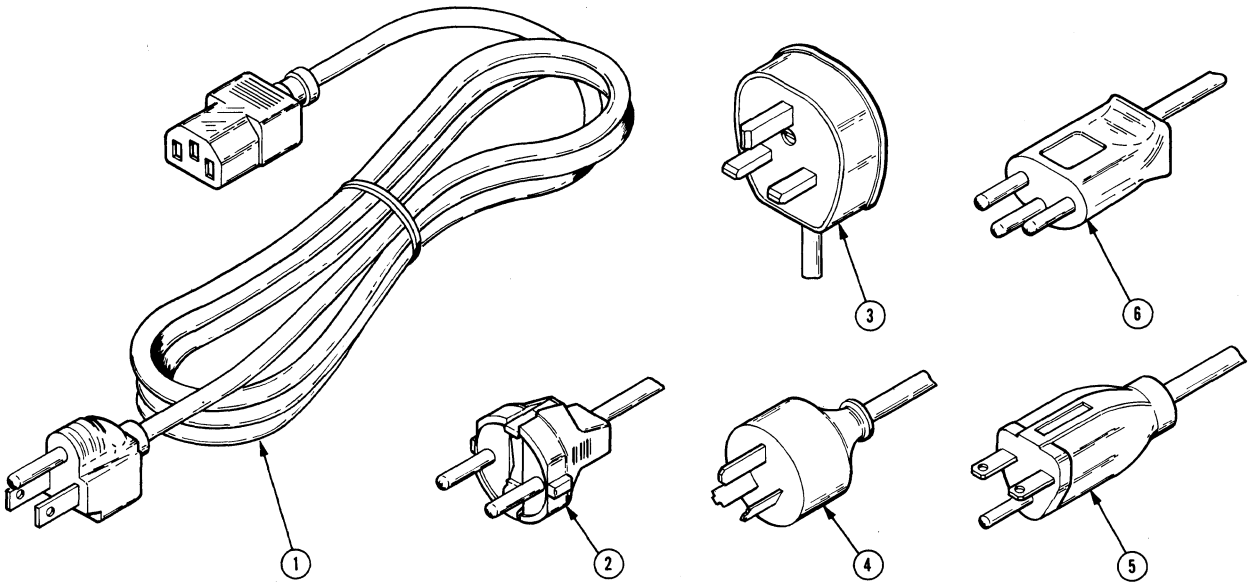

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	003-1313-00			1		SCREWDRIVER:	80009	003-1313-00
	016-0367-00			3		BDR,LOOSE-LEAF:2.0 CAP RING,VINYL COVER	80009	016-0367-00
	016-0370-00			7		DIV,LOOSE LEAF:FLEXIBLE DISK PKT,VINYL	000AC	OBD
	062-5840-03			1		SOFTWARE PKG:8560 DIAGNOSTIC,VER 1.3	80009	062-5840-03
	062-5882-06			1		SOFTWARE PKG:OPERATING SYSTEM VERS 2.1	80009	062-5882-06
	070-2552-00			2		CARD,INFO:DISC HANDLING	80009	070-2552-00
	070-3899-00			1		MANUAL,TECH:INSTALLATION GUIDE	80009	070-3899-00
	070-3940-00			1		MANUAL,TECH:USERS	80009	070-3940-00
	070-3941-00			1		MANUAL,TECH:REFERENCE	80009	070-3941-00
	070-3942-00			1		CARD,INFO:REFERENCE	80009	070-3942-00
	070-4656-00			1		MANUAL,TECH:SOFTWARE MAINT	80009	070-4656-00
	070-4730-00			1		MANUAL,TECH:USERS,8560 SERIES	80009	070-4730-00
	070-5047-00			1		MANUAL SET,TECH:SYSTEM MANAGERS PKG	80009	070-5047-00
	070-5049-00			1		MANUAL,TECH:INSTALLATION,8560 SERIES	80009	070-5049-00
	070-5050-00			1		MANUAL,TECH:OPERATORS,8560 SERIES	80009	070-5050-00
	070-5094-00			1		MANUAL,TECH:INSTALLATION,8561 HARD DISK	80009	070-5094-00
	----- -----			-		(8560F09 ONLY)		
	070-5095-00			1		MANUAL,TECH:INSTALLATION,8561 LSI 11/73	80009	070-5095-00
	----- -----			-		(8560F10 ONLY)		
	119-1182-00			1		FLOPPY DISKETTE:DOUBLE SIDED	80009	119-1182-00
5-1	161-0066-00			1		CABLE ASSY,PWR,:3,18 AWG,115V,98.0 L	T1372	ORD BY DESCR
-2	161-0066-09			1		CABLE ASSY,PWR:3,0.75MM SQ,220V,96.0 L	S3109	ORD BY DESCR
	----- -----			-		(EUROPEAN-OPTION A1)		
-3	161-0066-10			1		CABLE ASSY,PWR:3,0.75MM SQ,240V,96.0 L	S3109	ORD BY DESCR
	----- -----			-		(UNITED KINGDOM-OPTION A2)		
-4	161-0066-11			1		CABLE ASSY,PWR:3,0.75MM,240V,96.0L	S3109	1600
	----- -----			-		(AUSTRALIAN-OPTION A3)		
-5	161-0066-12			1		CABLE ASSY,PWR:3,18 AWG,240V,96.0 L	T1105	ORD BY DESCR
	----- -----			-		(NORTH AMERICAN-OPTION A4)		
-6	161-0154-00			1		CABLE ASSY,PWR:3,0.75MM SQ,240V,6A,2.5M L	000JA	A25SW
	----- -----			-		(SWITZERLAND-OPTION A5)		
	334-5504-00			1		MARKER,IDENT:MKD CAUTION	80009	334-5504-00
						OPTIONAL ACCESSORIES		
	070-4729-00			1		MANUAL,TECH:REF,8561/8560 SERIES	80009	070-4729-00
	070-4759-00			1		MANUAL,TECH:SERVICE	80009	070-4759-00

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: February 1, 1985 Change Reference: C2/285

Product: 8560/61/62 MUSDU Service Manual Part No.: 070-4759-00

DESCRIPTION Product Group 61

The 512K Memory Board is now standard on 8560 Multi-User Software Development Units. (Mod # MDP 937).

CHANGE INSTRUCTIONS

Throughout this manual, change all references to the 256K Memory Board as standard configuration for the 8560 MUSDU, to read 512K Memory Board as standard.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: April 9, 1985 Change Reference: C3/485

Product: 8560/61/62 MUSDU Service Manual Part No.: 070-4759-00

DESCRIPTION Product Group 61

Manual Revision Status:

1. Several editions of this manual may exist. Before entering this change, be sure that replacement change information relates to information in your manual.

2. This change affects editions of the manual dated:

   First Printing MAR 1984

CHANGE INSTRUCTIONS:

1. To ensure that information is incorporated in the proper sequence, enter Manual Change Information beginning with the earliest changes.

2. To implement this change:

   a. Remove old pages: 3-17/3-18

   b. Insert new pages: 3-17/3-18

3. You may wish to retain this Manual Change Information Sheet at the back of your manual as a record of the change.

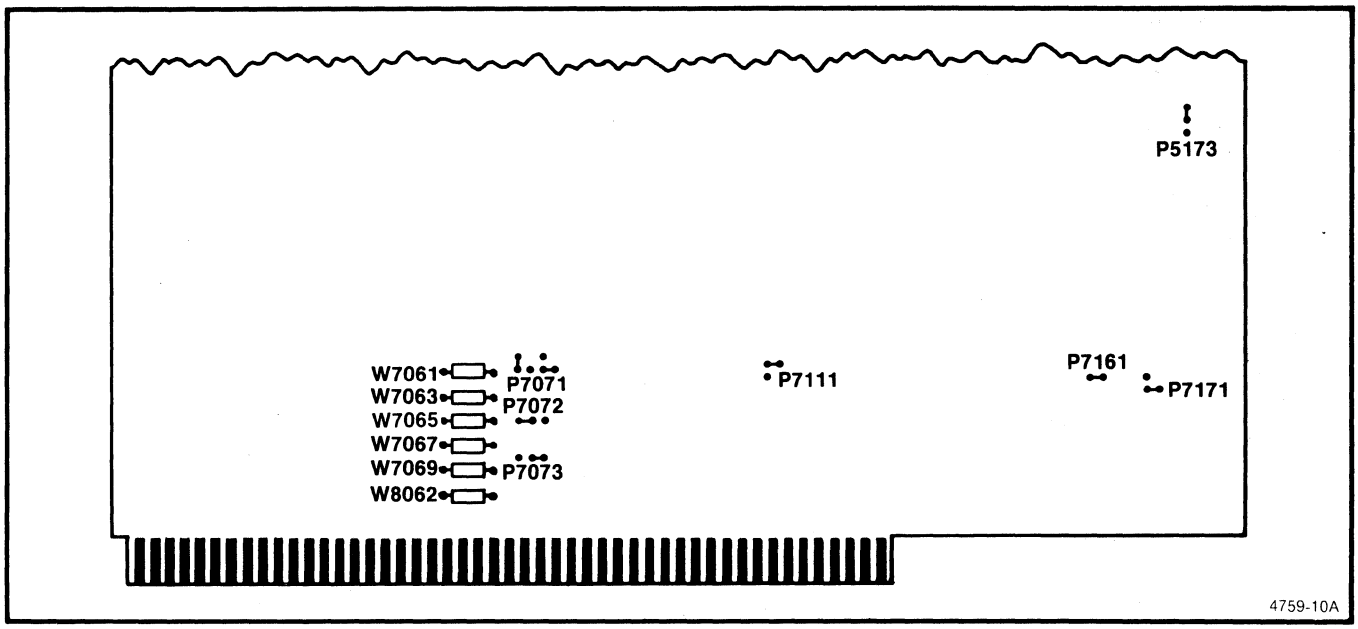

Fig. 3-11. 256K Memory Board jumper/strap locations.

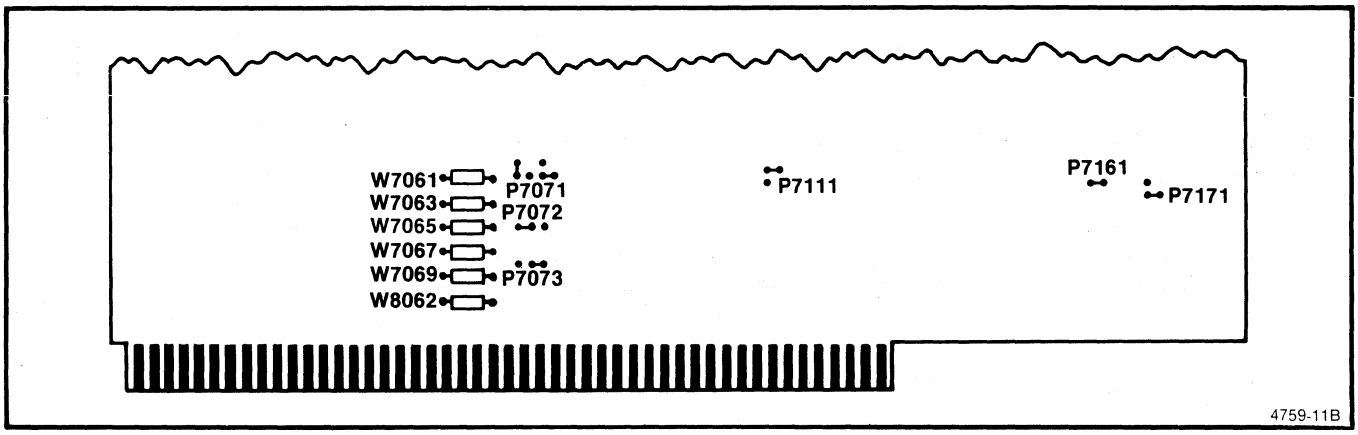

Fig. 3-12. 512K Memory Board jumper/strap locations.

Miscellaneous Straps

Table 3-10 lists the memory board miscellaneous jumpers. P7072 selects the size of the I/O space, and P5173 configures the board either as the upper or the lower memory bank. All other memory board jumpers are used for troubleshooting, to disable signals such as the input data, clock, refresh and others.

Table 3-10
Memory Board Miscellaneous Jumpers

Number	Function
P7072	Sets I/O space
P5173	Configures the board as either the upper or lower 256K-word bank
P7111	Parity enable
P7073	Read enable
P7171	Disables clock signal
P7161	Refresh enable
P5081, P5091, P5101, P5111	Parity/RAM exchange

Address Decoding for Memory Select Upgrades

Table 3-11 shows the positions of the various jumpers and straps involved in address decoding (address lines A19, A20 and A21) for the possible memory-select optional upgrades.

Table 3-11
Memory Address Selection Jumpers/Straps

Straps								Address Lines		
P7071(1)	P7071(2)	W7065	W7063	W7061	W7067	W7069	W8062	A21	A20	A19
1[a]	0[b]	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

[a] a "1" denotes a strap in the lower position.

[b] a "0" denotes a strap in the upper position.

Data and Parity Swapping

Table 3-12 lists the straps by which the low-byte parity-bit memory may be swapped with bit 0 memory, and the high-byte parity-bit memory may be swapped with bit 8 memory. Parity may therefore be read as data, allowing all memory chips on the board to be tested.

Table 3-12
Data and Parity Interchange Test Jumpers

Jumper No.	Name	Signal	Function	Default
P5081	AM-AI AO-AK AN-AJ AP-AL	DN0(H) DNLP(H) DN0(H) DNLP(H)	Swaps DT0H and DNLPH signals J6078	IN OUT OUT IN
P5091	AE-AA AG-AC AF-AB AH-AD	DT0(H) DTLP(H) DT0(H) DTLP(H)	Swaps DT0H and DTLPH signals J5077	IN OUT OUT IN
P5101	AU-AQ AW-AS AV-AR AX-AT	DN8(H) DNHP(H) DN8(H) DNHP(H)	Swaps DN8H and DNHPH signals J5091	IN OUT OUT IN
P5111	BE-BA BG-BC BF-BB BH-BD	DT8(H) DTHP(H) DT8(H) DTHP(H)	Swaps DT8H and DTHPH signals J5108	IN OUT OUT OUT

The system memory in the 8560 MUSDU consists of one or two dynamic RAM boards. Any one, or combination of any two, of the 256K-byte and 512K-byte Memory Board(s) may be used.

Memory Bank Selection

If only one memory board is installed, the board must be assigned to control the low bank of memory addresses. Jumper P7071(1) must be in the A-B position, jumper P7071(2) must be in the D-F position, and jumper P5073 (256K memory board only) must be in the W-X position. Refer to Fig. 3-13 for low-bank configuration of the 256K Memory Board. Refer to Fig. 3-14 for low-bank configuration of the 512K Memory Board (one or two 512K Memory Boards installed). Refer to Fig. 3-15 for low-bank configuration of the 512K Memory Board (256K Memory Board and 512K Memory Board installed.)

If two memory boards are used, one board must be configured as the low bank board. The second board must be configured as the high bank board. Refer to Fig. 3-13 for

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MANUAL CHANGE INFORMATION

Date: June 13, 1985 Change Reference: C4/685

Product: 8560/8561/8562 MUSDU Service Manual Part No.: 070-4759-00

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CHANGE INSTRUCTIONS

On Schematic 30, MSC CPU, add delay line as indicated in partial schematic below: