Tektronix®

8501
DATA MANAGEMENT UNIT

SERVICE

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PRELIMINARY

8501
DATA MANAGEMENT UNIT

SERVICE

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

061-2355-00

First Printing AUG 1980

WARRANTY

Tektronix warrants that this product, excluding customer-supplied equipment, is free from defects in materials and workmanship. The warranty period is ninety (90) days from the date of shipment. Tektronix will, at its option, repair or replace the product if Tektronix determines it is defective within the warranty period. CRTs are warranted for one (1) year. During the nine (9) months following expiration of the product warranty, Tektronix will replace defective CRTs at no charge for the material.

In the forty-eight (48) contiguous United States, the District of Columbia, and in other areas where Tektronix normally offers on-site service for this product, Tektronix will provide this service at no charge during the product warranty period described above. In areas where Tektronix does not offer on-site service for this product, warranty service will be provided at no charge if the product is returned, freight prepaid, to a service center designated by Tektronix.

Tektronix may use the original vendor's service organization to service any product that is supplied but not manufactured by Tektronix.

Tektronix is not obligated to furnish service under this warranty:

a. to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair, or service the product;

b. to repair damage resulting from improper use or from connecting the product to incompatible equipment;

c. if personnel other than Tektronix representatives modify the hardware or software.

There is no implied warranty of fitness for a particular purpose. Tektronix is not liable for consequential damages.

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PREFACE

INTRODUCTION

This Service Manual contains information required to repair an 8501 Data Management Unit. This manual contains few operating instructions other than those required to service the 8501.

Intended Use of this Manual

This manual is designed to be used by trained service technicians. This manual is not designed as a training tool. The intent is to provide sufficient information to allow a technician to locate a problem to a particular block of circuitry on a circuit board.

ABOUT THIS MANUAL

This Manual gives you an introduction to the software and hardware components of the 8501 Data Management Unit. In addition, this Manual describes, on a block diagram level, the operation of the hardware within the 8501. At the rear of this Manual are schematic diagrams and parts lists. The Manual is divided into the following sections:

Section 1 This section provides an overview of the hardware and software used with the 8501 Data Management Unit.

Section 2 Installation information is provided in this section, along with strap and jumper options for each circuit board.

Section 3 This section contains information on the use and interpretation of ROM-based diagnostics within the 8501.

Section 4 This section provides information on the use and interpretation of disc-based diagnostics.

NOTE

Disc-based diagnostics are not available at this printing. When they do become available, they will be released on a separate diagnostics disc.

Section 5 The operation of the 8501 is discussed in this section. Flow charts are used, illustrating the communications between elements within the 8501.

Section 6 The 8501 specifications are located in this section, along with I/O port descriptions.

Section 7 This section describes the operation of the LSI-11/2 processor used in the 8501.

Section 8 The 32K RAM board is described in this section.

Section 9 This section describes the 8501 Utility board.

Section 10 This section describes the 8501 I/O board.

Section 11 This section describes the 8501 Communications Adapter board.

Section 12 This section describes the 8501 Flexible Disc Controller board.

Section 13 This section describes the 8501 Power Supply

Section 14 This section contains the 8501 Replaceable Electrical Parts List.

Section 15 This section contains the 8501 schematics.

Section 16 This section contains the 8501 Replaceable Mechanical Parts List.

Nomenclature

NOTE

The terms DEC and LSI-11/2 are used throughout this manual. DEC and LSI-11/2 are registered trademarks of the Digital Equipment Corporation, Maynard, Massachusetts.

Octal Notation. Octal notation is used throughout this manual in reference to data and address information, unless otherwise noted.

Schematics

The schematics at the rear of this manual use a high/low convention to describe the asserted state of any signal lines. Each line name is followed in parentheses with its asserted state, I.E.:

HALT (L) -- indicates that the HALT line is asserted low
R/W (H/L) -- indicates that when high, R is asserted -- when low, W is asserted.

Change Information

Change notices are issued by Tektronix, Inc., to document changes in the manual after it has been published. Change information is located in the back of this manual, following the yellow tab marked "CHANGE INFORMATION". When you receive this manual, enter any change information into the body of the manual, as indicated on the change notice.

Revision History

As this manual is revised and reprinted, revision history information is included in the text and diagrams. Original manual pages are indicated by the "@" symbol at the bottom inside corner of the page. Existing pages of manuals that have been revised are indicated by a revision code and date (REV B SEP 1979) in place of the "@" symbol. New pages added to an existing section, whether they contain old, new, or revised information, contain the "@" symbol alongside the revision date (@ SEP 1979).

Related Manuals

The following manuals may contain information useful to the service technician.

Title	Source
Microcomputer Handbook	Digital Equipment Corporation Publication #EB-07948-53/77
Microcomputer User's Guide	Digital Equipment Corporation Publication #EK-LSI11-US-001
8301 MDU Service Manual	Tektronix, Inc.
8550 MDL Installation Guide	Tektronix, Inc.
8550 MDL Users Manual	Tektronix, Inc.

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(To be provided.)

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols

In This Manual


This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION—refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

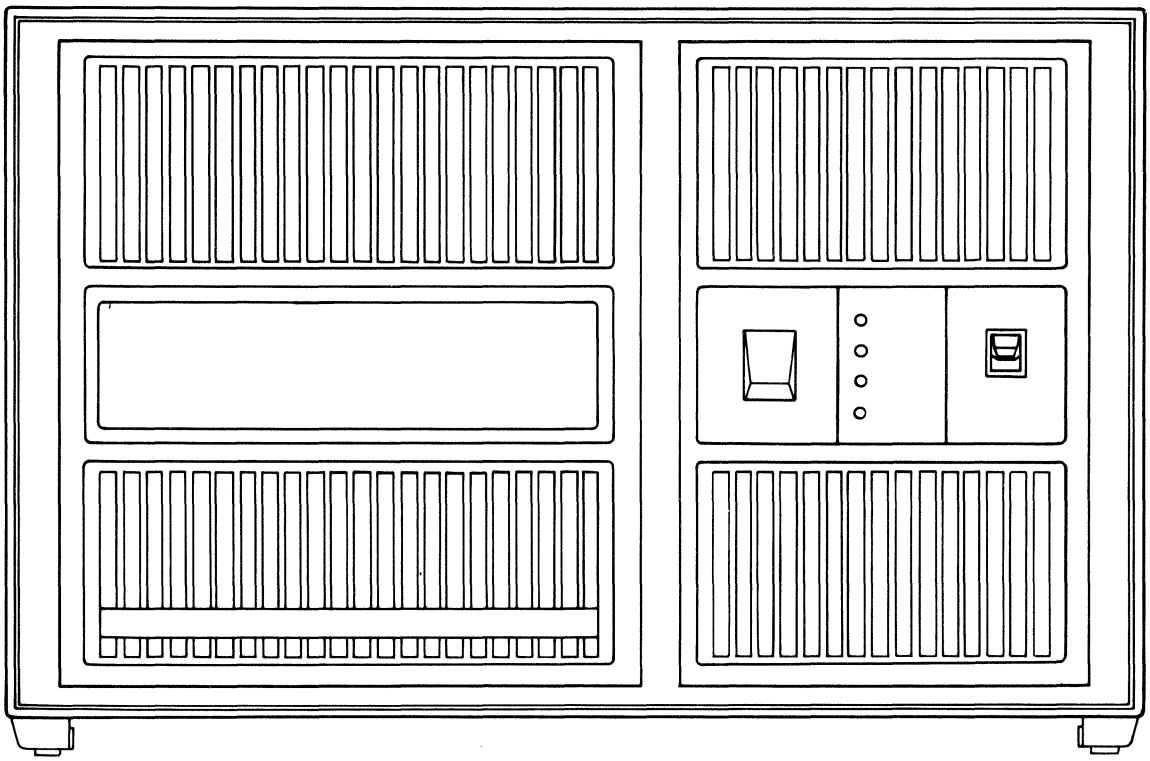
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



Section 1

GENERAL INFORMATION

INTRODUCTION

The 8501 Data Management Unit is a 16-bit bus orientated computer designed to operate in conjunction with file management software. The standard 8501 DMU includes a DEC LSI-11/2 CPU, two double density, double sided flexible disc drives with DMA control, and a 32K by 16-bit dynamic RAM memory.

SYSTEM OVERVIEW

Software Architecture

The 8501 operates under DOS/50 software control. At power-up DOS/50 is loaded from the system disc and takes up residence in the system memory where it handles file routines.

A related software control system is the High-Speed Interface (HSI). This sub-system is also loaded into memory from the system disc, and is the controlling software for 8501 communications over the High-Speed Interface (HSI) port.

The operations controlled by DOS/50 are detailed in separate user manuals (See "Related Manuals" at the end of this section).

DMA. All normal data operations in the 8501 are carried out under DMA (Direct Memory Access). This includes disc controller operations and communications using the HSI.

Interrupts. Extensive use is made in the 8501 DMU of interrupts and interrupt vectors. The interrupts can be grouped into three categories; I/O originating, CPU originating and software originating.

I/O originating interrupts occur on both the I/O and Utility boards. CPU originating interrupts are designed into the LSI 11/2's operating microcode. And, software interrupts are interrupts used to call service routines which exist as separate major software elements, e.g. DOS/50 calls the HSI program as an interrupt service routine.

Diagnostics. The 8501 has two types of diagnostics available, ROM-based and disc-based:

- o power-up diagnostics are ROM-based, and execute automatically each time power is applied to the instrument.
- o ROM-based diagnostics are interactive, and require user input.
- o Disc-based diagnostics support board level fault isolation. This is the normal field verification level which may be used where the disc system is not at fault.

Hardware Architecture

An overall 8501 DMU block diagram is shown in Fig. 1-1. The following descriptions provide a brief overview of the individual circuit boards. A discussion of the 8501 internal bus is included in the description of the LSI-11/2 processor.

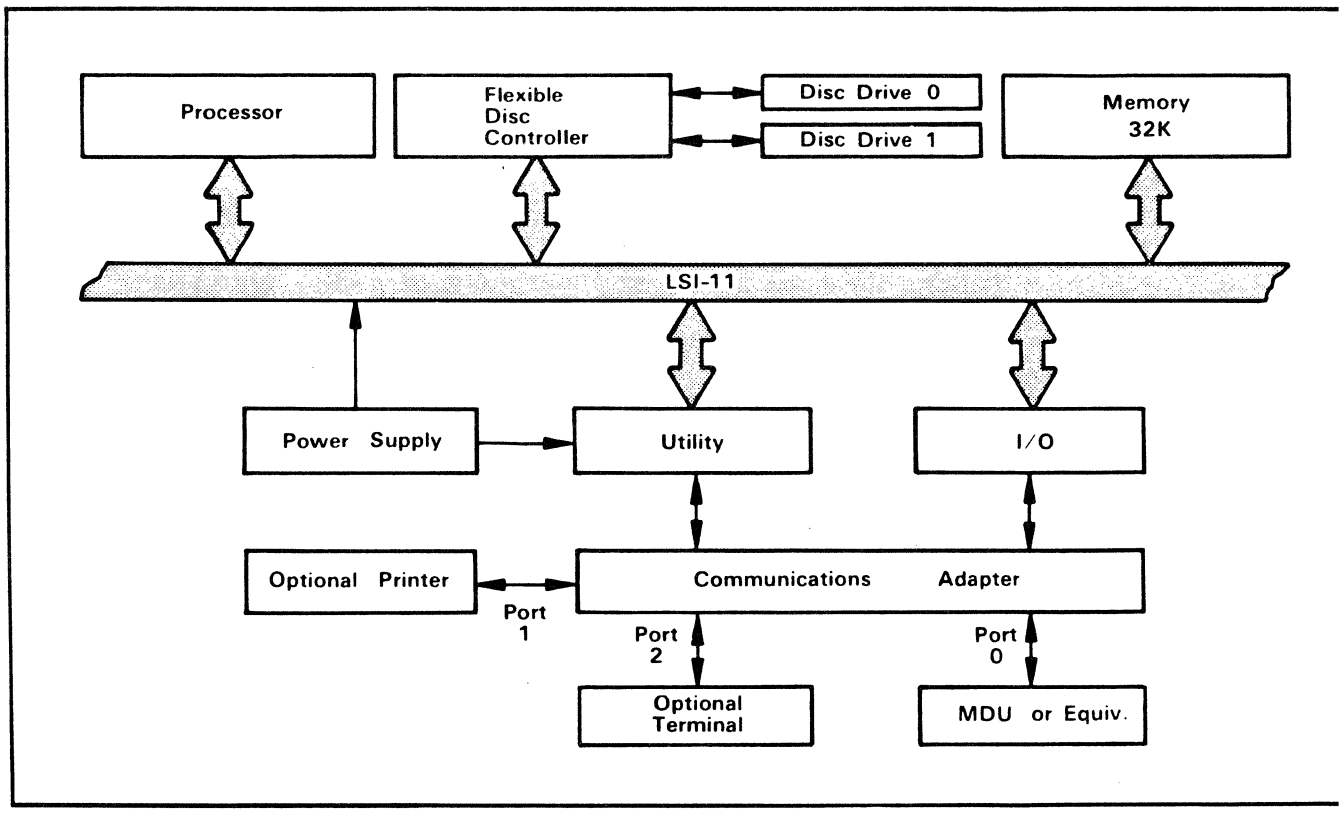


Fig. 1-1. 8501 System block diagram.

Processor. The 8501 DMU uses a Digital Equipment Corporation LSI-11/2 16-bit microcomputer as its central processing unit. The LSI-11/2 card contains a four-chip CPU, micro-instruction ROM's, control logic, bus driver/receivers, and a 2.6 MHz internal clock. A block diagram of the LSI-11/2 is shown in Fig. 1-2. The board includes a 72 pin edge connector physically arranged to prevent reversed card insertion.

The processor bus follows normal LSI-11/2 conventions. This includes 16 data/address lines, and a number of dedicated control lines. Section 6 contains a complete list of the LSI-11/2 bus signals and also includes a DEC to 8501 pin designation chart.

Other features of the LSI-11/2 processor include 32K 16-bit memory addressing (fully supported in the 8501), asynchronous operation, direct memory access processing, and fast interrupt response capability. The microcode also includes an Octal Debugging Technique (ODT) microprogram which allows any 8501 bus addressable register to have its contents both examined and changed in direct response to terminal requests (only functions in the HALT mode). For more details on the 8501 DMU processor hardware refer to Section 7. For more details on instruction processing refer to DEC's Microprocessor Handbook (listed at the rear of this Section).

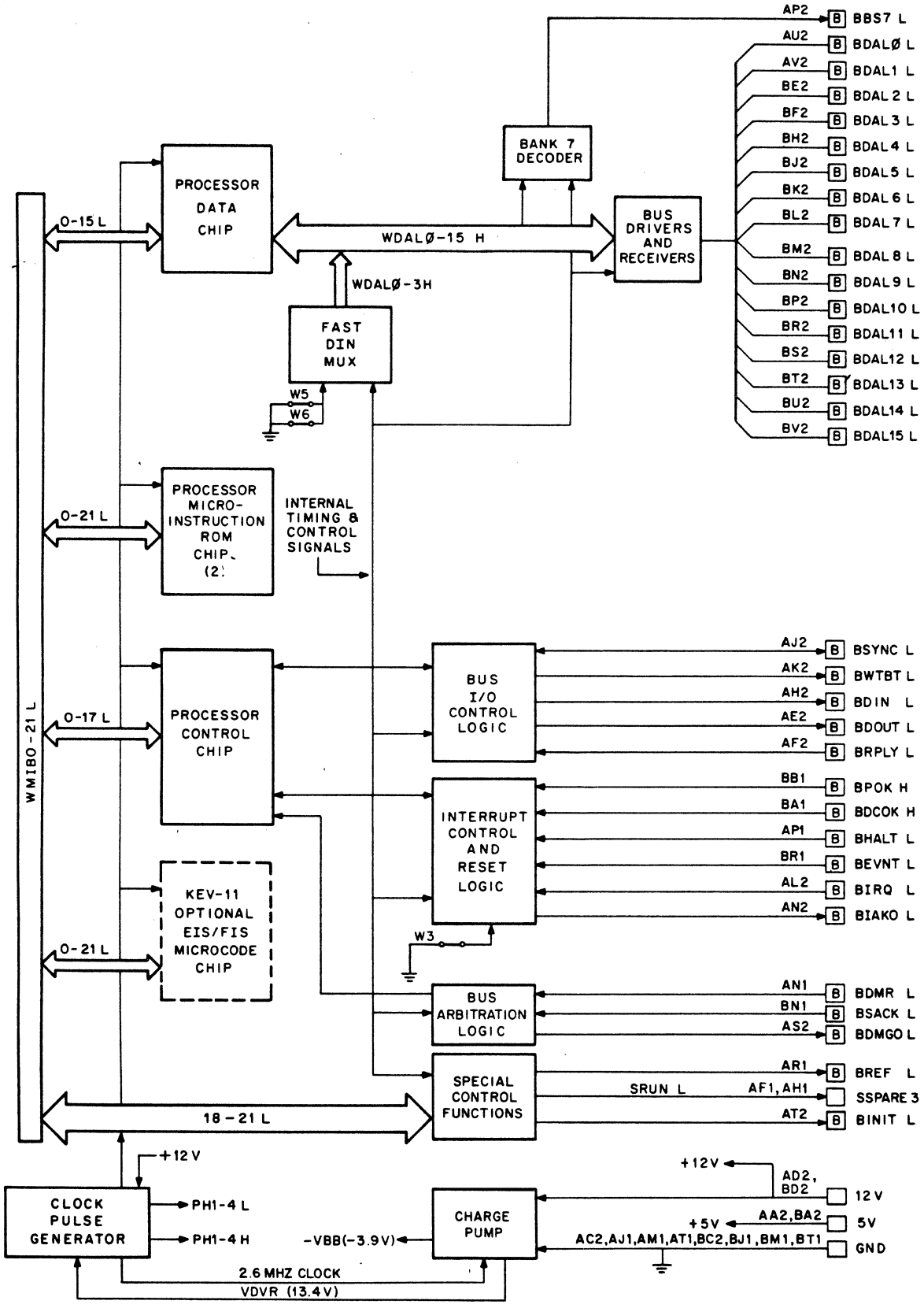


Fig. 1-2. LSI-11/2 Processor block diagram.

Memory Board. This board provides 32,768 16-bit words of dynamic RAM memory. The memory has an average read cycle access time of 210 nS and a memory cycle time of 410 nS.

Figure 1-3 shows the general configuration of the 8501 DMU memory organization. Note that this figure as well as all references to bus addressable registers or devices follow the DEC convention of octal notation.

Imbedded in DOS/50 is the High-Speed Interface (HSI) program consuming approximately 1.5K-bytes of memory. This program handles communications routed through the HSI port.

Above the file management program is an 8K area of free space designed to hold open or active files. This area will hold from one to a maximum of nine files arranged in blocks of 512 bytes.

At the top of the memory map is an 8K-byte area reserved for register and device address. Both fixed device addresses and use selectable device address ranges are discussed in the text as the need occurs.

Distributed refresh for the dynamic RAM's is provided by on-board circuitry. A dynamic RAM refresh cycle occurs either with every bus cycle (when the memory board is not selected), or after a 15 microsecond period has elapsed since the last refresh cycle. The maximum delay produced by a refresh cycle is 450 nS. All timing for the memory is provided by an on-board 24.25 MHz crystal controlled clock.

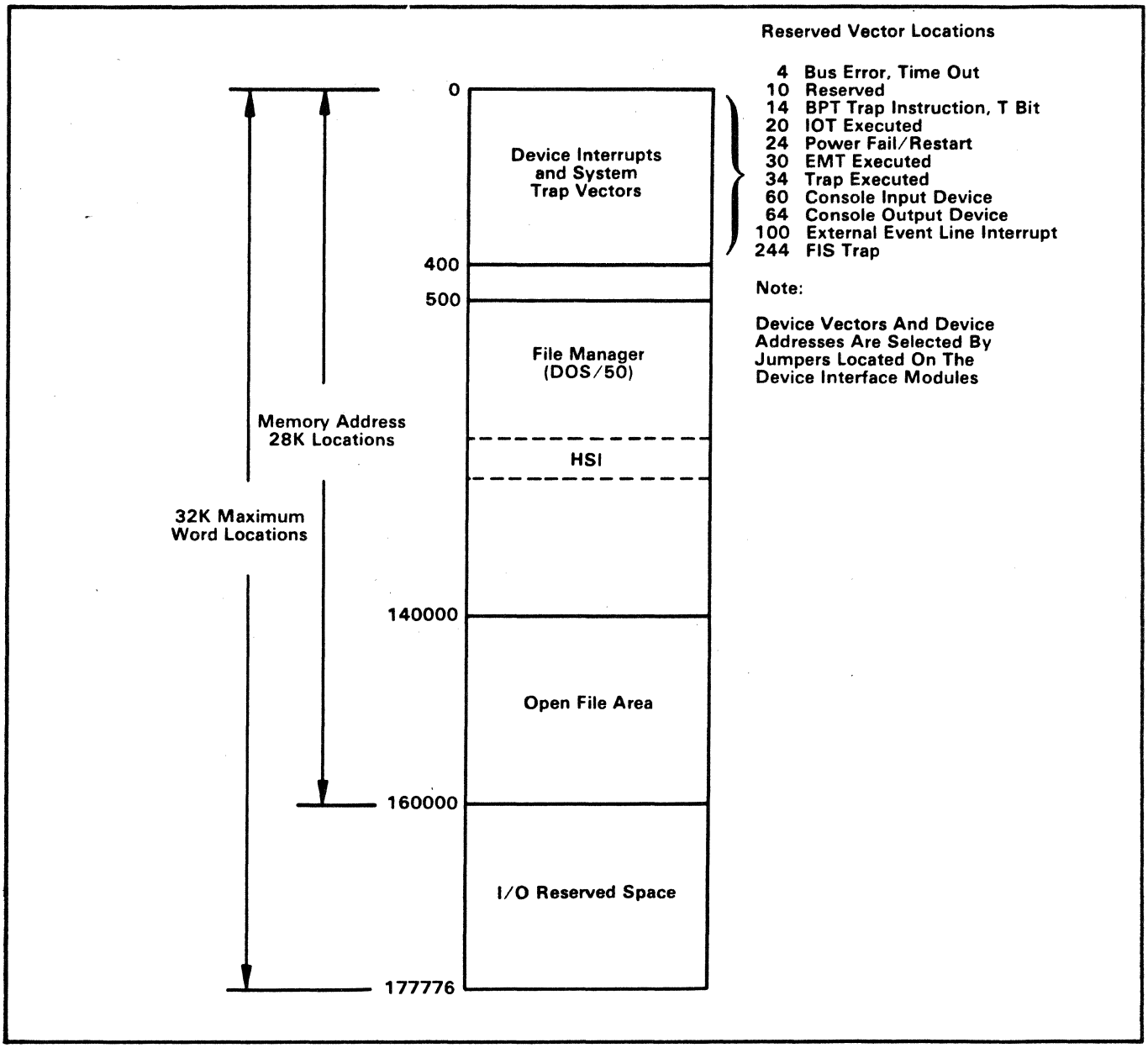


Fig. 1-3. Memory organization.

Utility Board. This board contains two RS-232-C serial interface circuits serving the AUXILIARY and PRINTER ports on the Communication Adapter board. In addition, the Utility board contains a number of circuits providing general control functions for the DMU. These circuits include a PROM-based bootstrap program for loading the disc operating system into memory, and a diagnostic program for providing the DMU with an internal self-test feature.

Other logic contained on the Utility board includes control circuits for Line-Time clock generation, interrupt processing (for the two serial interfaces), and a power-up circuit for establishing correct power levels and for providing power up/down protocols.

The two interface circuits serving the AUXILIARY and PRINTER ports are identical. The baud rate for each interface may be strap selected, provided by an external clock, or selected under program control. The minimum and maximum baud rates using strap or program control are 50 and 9600 baud respectively. The maximum external clock frequency should not exceed 350 KHz (20K baud).

A system level block diagram is provided in Fig. 1-4. The Utility blocks are briefly described in the text which follows.

Serial I/O and Line-Time Clock Interface Registers. There are a total of nine interface registers used on the Utility board: two sets of four registers for the RS-232-C serial/parallel control, and one register for providing Line-Time Clock (LTC) status. The serial interface registers are shown in Fig. 1-5.

The serial/parallel control registers (RCSR, RBUF, XCSR and XBUF) are associated with one Universal Asynchronous Receiver Transmitter (UART) for each interface, and perform the necessary input/output control. The LTC register controls the real time LSI-11/2 EVENT interrupt with input obtained from the line frequency, selection of bootstrap or diagnostic programs. The interrupt is output to the diagnostic status LED's (mounted on the Utility board).

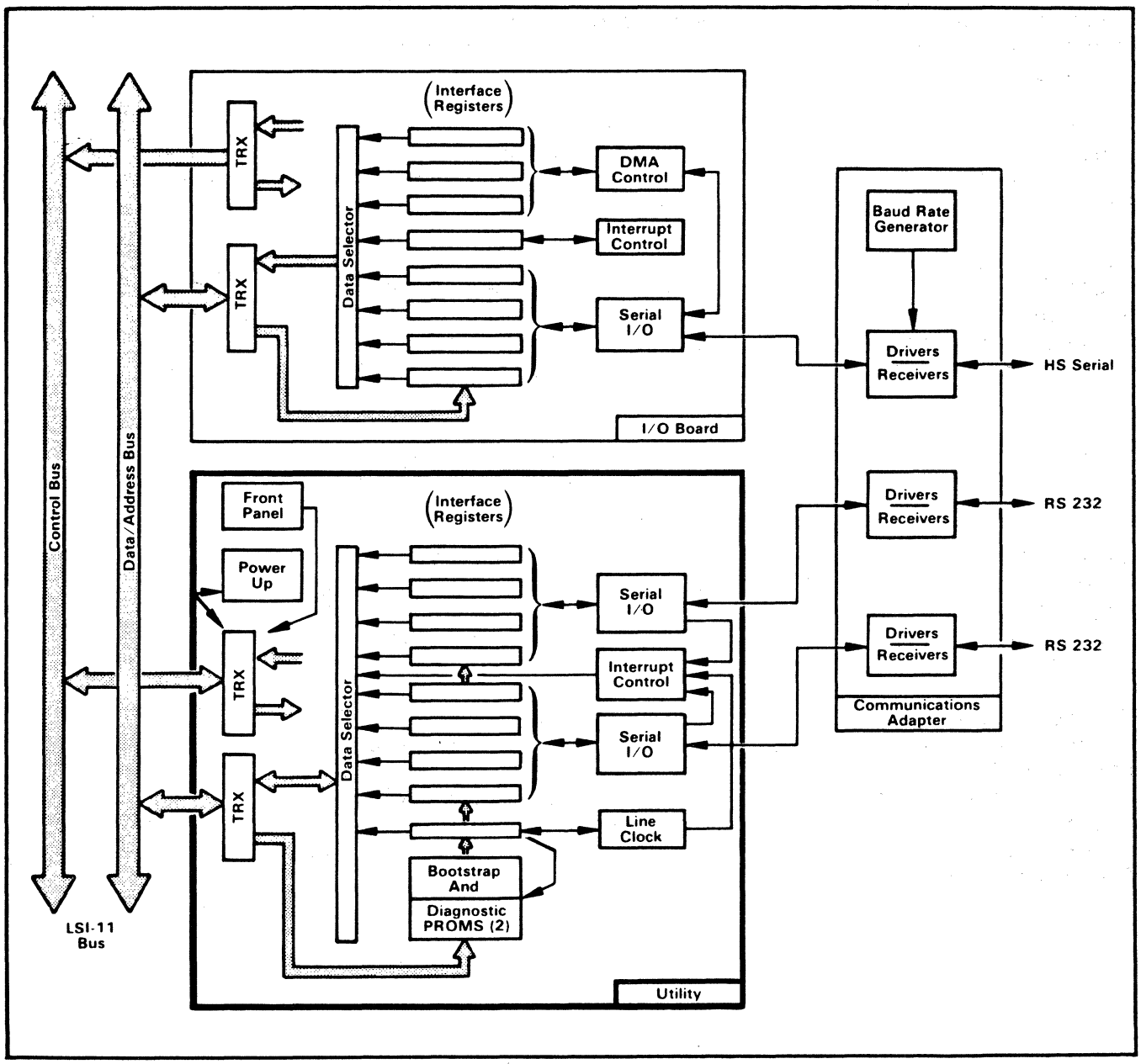


Fig. 1-4. System block diagram showing Utility Board.

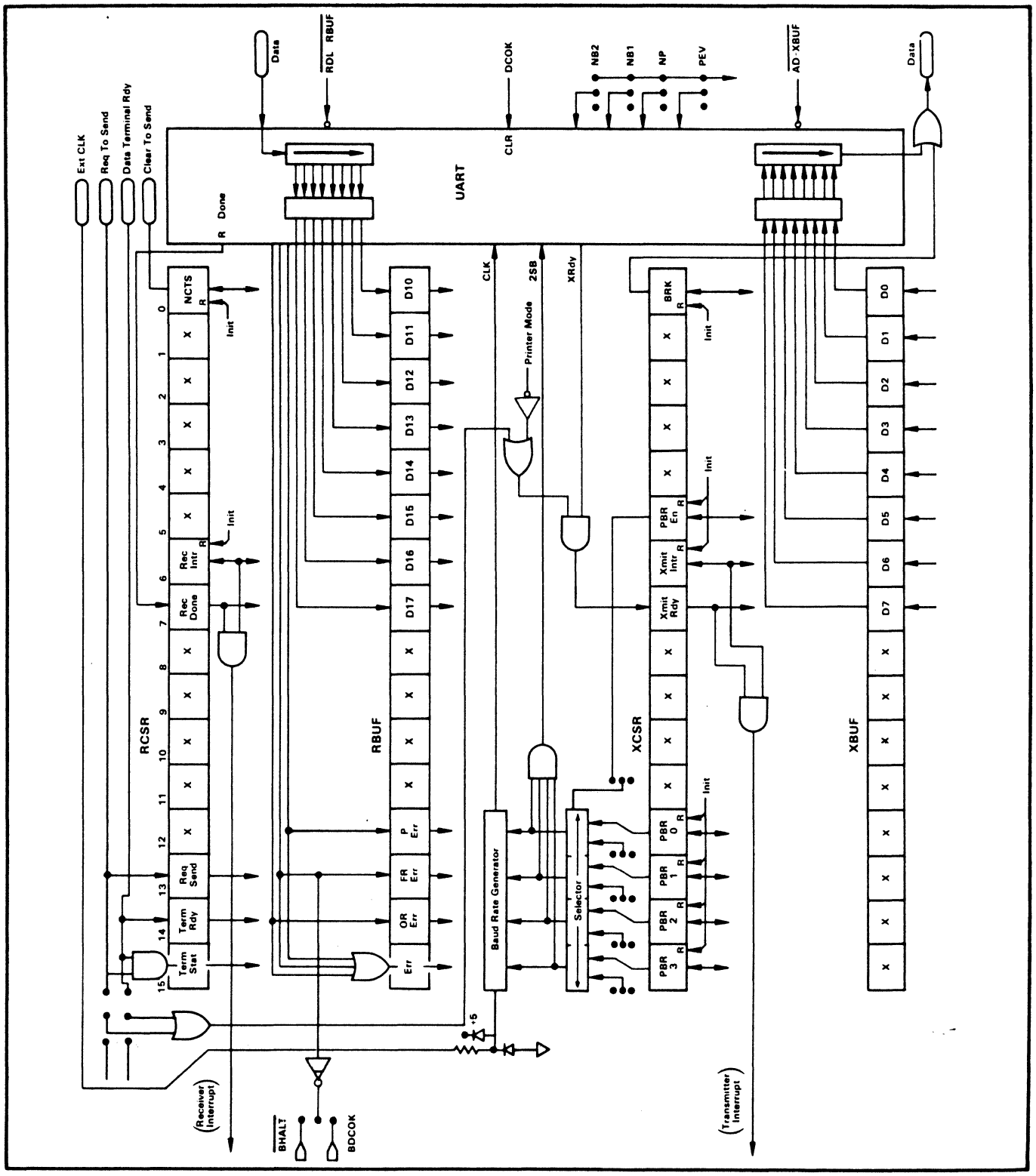


Fig. 1-5. Serial Interface Register.

Front Panel and Power-Up Circuits. The power control logic can be divided into two parts. The first part involves remote power control. The second part of the power control ensures an orderly power up sequence and voltage check-out from a cold start. This logic informs the processor of a satisfactory power-up sequence in accordance with pre-determined LSI-11/2 ground rules. The latter procedure also ensures the least software destructive power-down sequence in the event of an abrupt power failure.

Bootstrap and Diagnostic PROM Programs. The bootstrap and diagnostic programs reside in two 1K-byte Programmable Read Only Memories (PROMs) sharing identical address space (octal 173000-174776). The bootstrap program performs the primary boot from disc following a normal power-up or RESTART switch initialization. The diagnostic program performs a number of basic system diagnostic checks as described in Section 3.

The selection of diagnostic or bootstrap programs is a function of bit 5 in the LTC register. In a normal power up operation the diagnostic program will first run its diagnostic checks after which (assuming no faults are found), it will change this bit in the LTCR, thereby allowing the bootstrap program to run and boot the disc operating system into memory.

Interrupt Control. The Utility board is designed to interrupt the LSI-11/2 under two primary conditions: if either the AUXILIARY port or PRINTER port receiver buffer is full, or if either transmit buffer is empty. Each of these interrupts utilize a strap selectable vector address in the octal range 0 to 774.

Alternative vectors can be strap selected to provide interfacing of either port with DEC LAV-11 or Centronics type printers. Refer to Section 2 for all details on strapping options.

For more details on Utility board logic refer to Section 9.

I/O Board. The I/O board is used to enable high-speed serial communications over the High-Speed Interface (HSI) port. The I/O board contains fast serial to parallel and parallel to serial conversion logic, and includes Direct Memory Access (DMA) and vectored interrupt control.

The serial input/output of the I/O board is routed to the High-Speed Interface (HSI) connector at the HSI port via drivers and receivers mounted on the Communications Adapter board.

A system level block diagram of the I/O board is shown in Fig. 1-6. The I/O board blocks are briefly described in the following text.

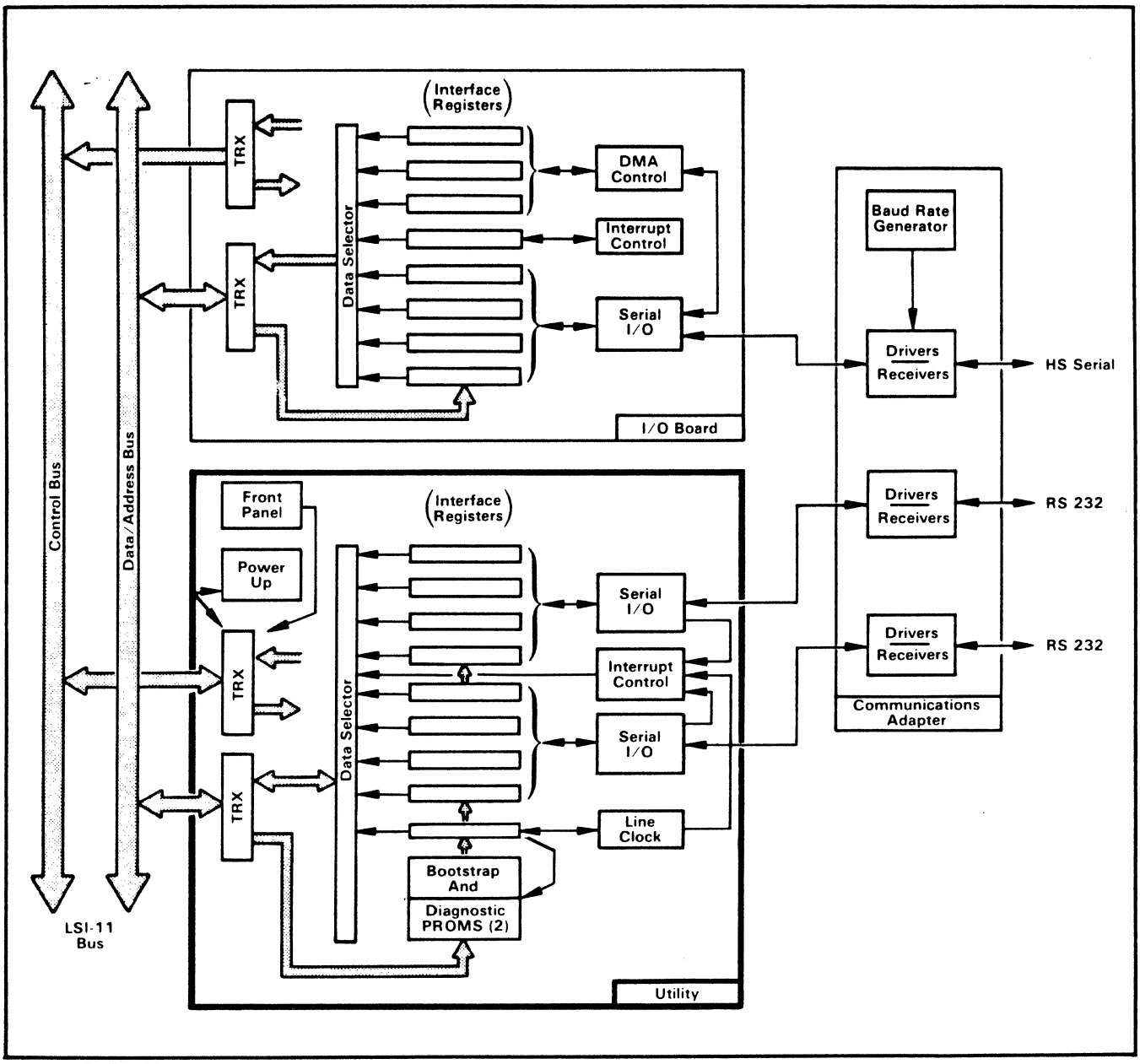


Fig. 1-6. I/O Board block diagram.

Serial I/O. The serial part of the board consists of one UART and four registers. The UART transmits and receives serial data to and from the HSI port at a rate determined by a switch mounted on the Communications Adapter board and accessible from the back panel.

There are four registers (shown in Fig. 1-7) associated with the serial/parallel transmission control. Two of these (XBUF and RBUF) are input and output buffers for the parallel data. The other two (RCSR and XCSR) are transmit and receive status registers.

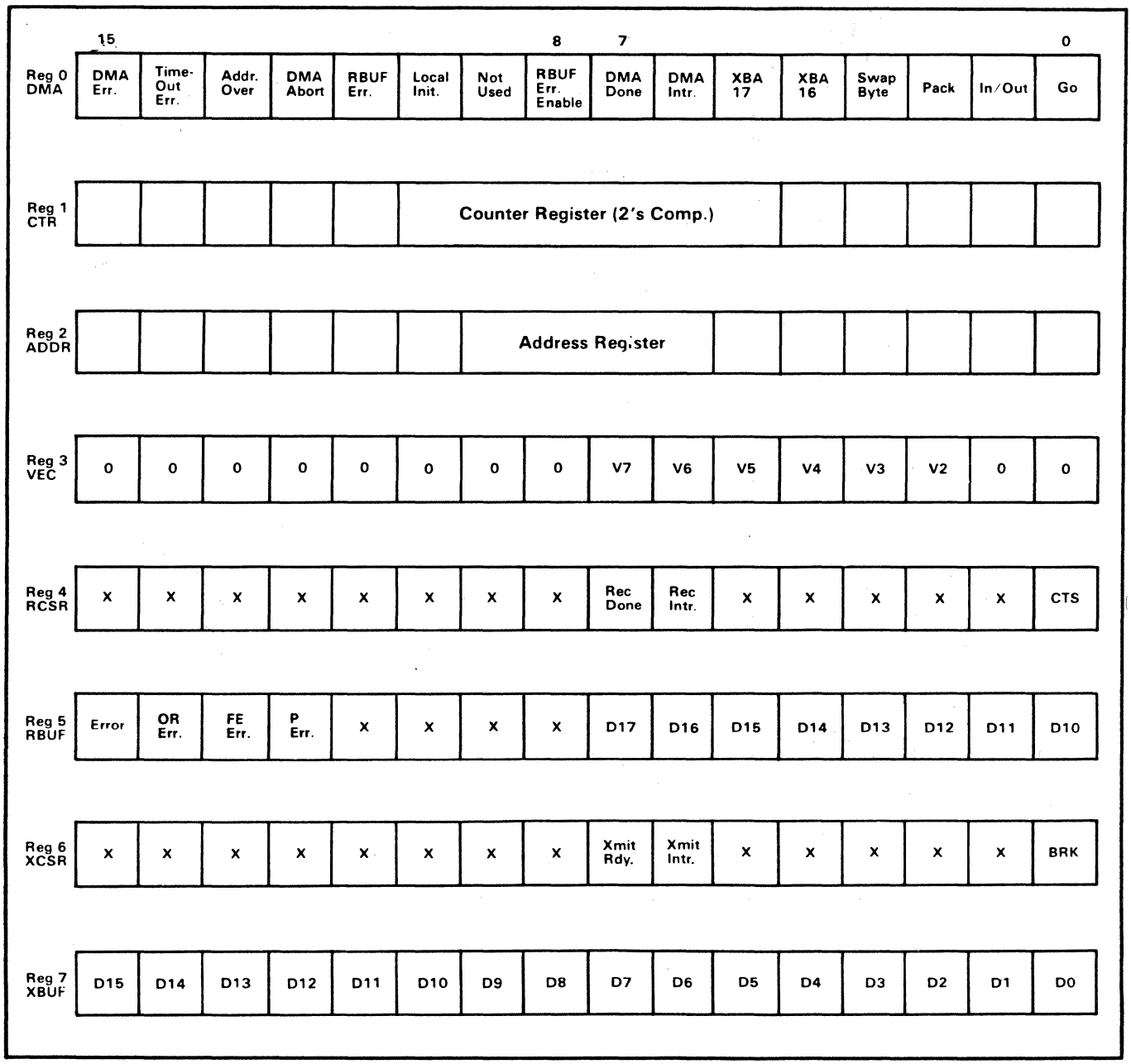


Fig. 1-7. I/O Board Registers.

DMA Control. The I/O board DMA circuit consists of a DMA register, a DMA state machine and related control logic. The DMA state machine performs the basic bus arbitration protocol necessary to rout the DMA data.

The DMA transfer is made using byte, packed, or byte-swapping-packed mode. Mode selection is under program control and is reflected in the DMA register (see Fig. 1-7).

In the byte mode, a high-order byte of memory is filled with zeros and the transferred data is placed in the low-order byte. When the packed mode is used, the first byte of data is placed in the low-order memory byte, and the second byte of data is placed in the high-order byte of memory. Byte-swapping-packed operation reverses the location of the first byte and second byte of data.

Interrupt Control. The I/O board will interrupt the LSI-11/2 processor under the following conditions.

1. Receiver buffer is full
2. Transmit buffer is empty
3. DMA operation is complete
4. An error occurred during the DMA transfer

At system power-up the I/O board interrupt vector is 060 octal. Once the system is powered up the I/O interrupt vector address may be changed under program control to any octal address within the range 000-360.

Communications Adapater. The Communications Adapter board (Comm Adapter) is a small circuit board mounted directly to the rear panel of the 8501. This unit serves as an interface and serial adapter for peripheral devices. Altogether, the Comm Adapter board has three communications connectors mounted to it (appearing through a rear panel plate), forming the HSI, PRINTER, and AUXILIARY ports.

The PRINTER and AUXILIARY ports perform driver and receiver functions for RS-232-C compatible communications. The HSI port can be configured to operate with RS-232-C, RS-422 or RS-423 communications protocols. The HSI port is routed to the 8501 I/O board. Strap-type options on the board include changes in the minimum and maximum baud rates; and a strap for selecting the number of stop bits. Primary baud rates for the HSI port are selectable by means of a slide switch mounted on the rear panel. Also included on the rear panel are two BNC connectors to receive and transmit remote power control signals.

A system block diagram of the Comm Adapter board is provided in Fig. 1-8.

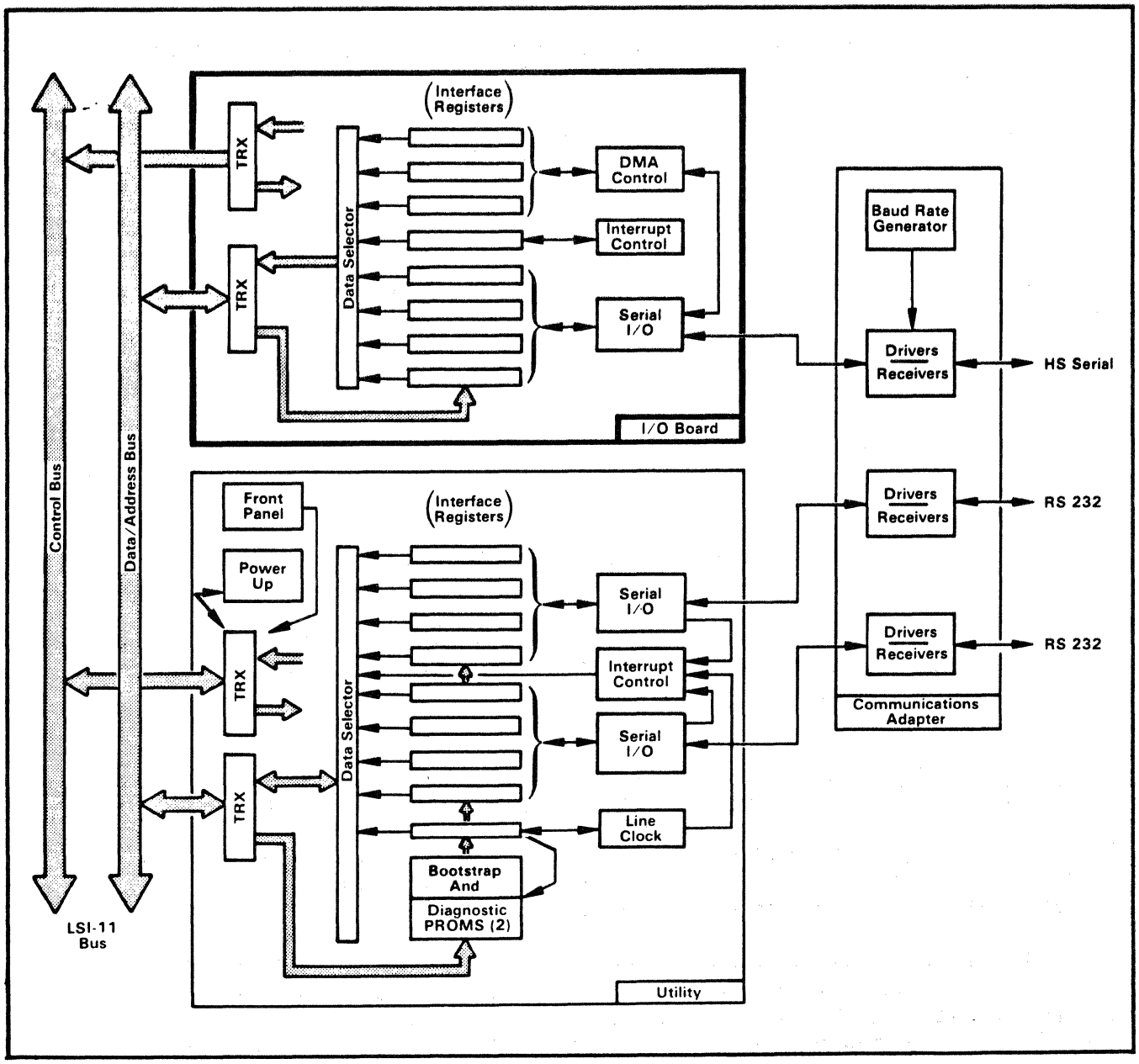


Fig. 1-8. Communications Adapter block diagram.

For more detailed information on the Communications Adapter board refer to Section 11.

Flexible Disc Drive Units. There are two disc drives housed in each 8501. These drives are the Qume DataTrak 8 or equivalent.

For full details on the Qume DataTrak 8, refer to the DataTrak 8 Flexible Disc Drive Service Manual.

Flexible Disc Controller. The Flexible Disc Controller manages the operation of the 8501 flexible disc drives. The controller formats, reads, and writes in IBM compatible single or double density format and on either single or double sided discs.

A block diagram of the Controller's hardware architecture is shown in Fig. 1-9. The PROM is used by a Z80A to reference disc format data and Z80A task routines. The RAM is used for temporary storage of internal program and register update material. The disc drive interface contains drive interface logic and includes frequency modulation encoding, write precompensation, data separation, data synchronization and CRC generation and verification logic.

The Flexible Disc Controller contains a Z80A microprocessor device which performs all data transfers under DMA control. It does this by reading an eight-bit register control buffer located at 177160 (octal) in system memory. This address is also the address of the first of ten registers contained within the controller logic. These latter registers are controlled by the Z80A and are used to record the status of, and direct the operations of, the disc drives. The two sets of reigsters are shown in Fig. 1-10 (Control Buffer) and Fig. 1-11 (Z80A addressable registers).

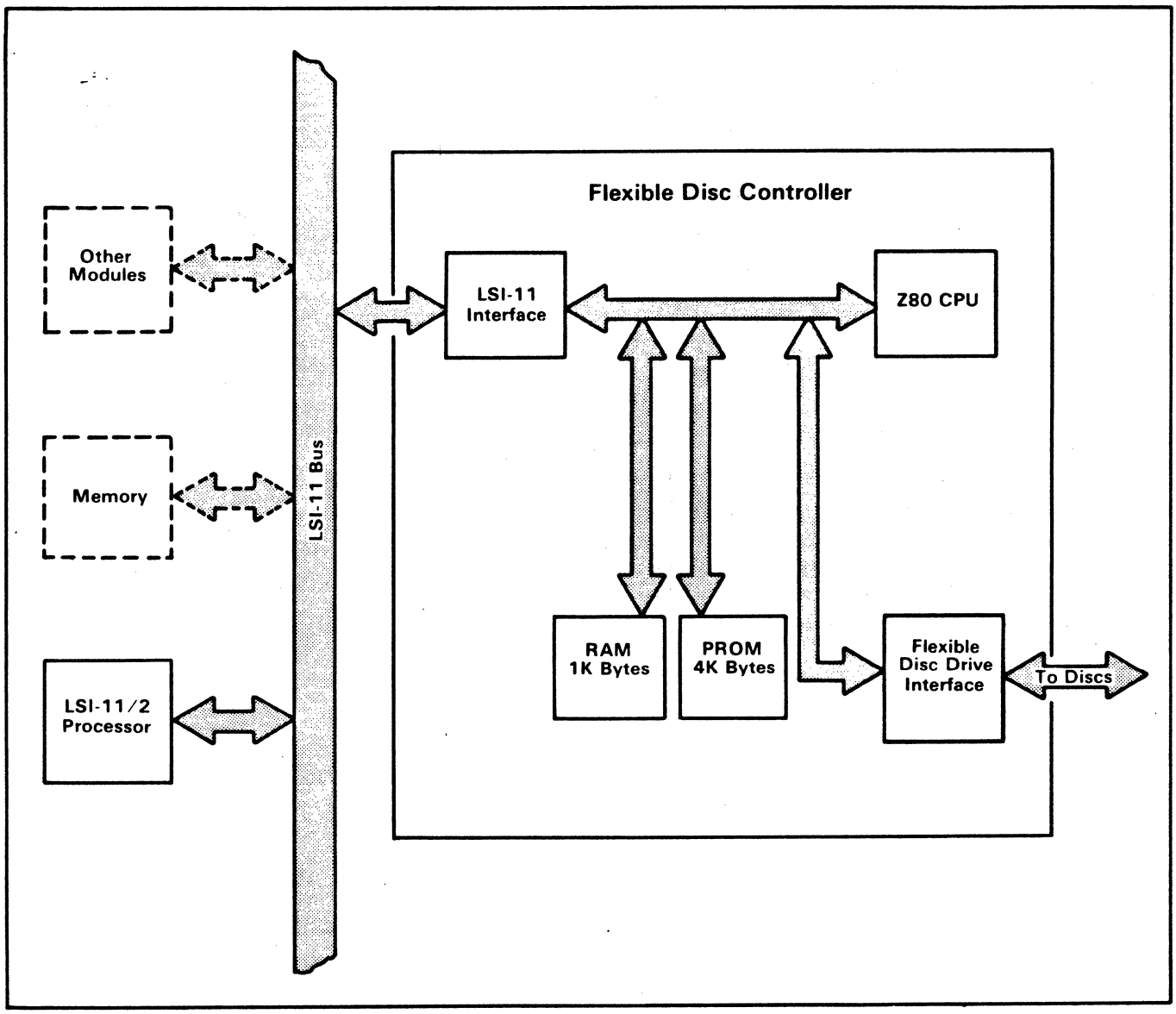


Fig. 1-9. Flexible Disc Controller block diagram.

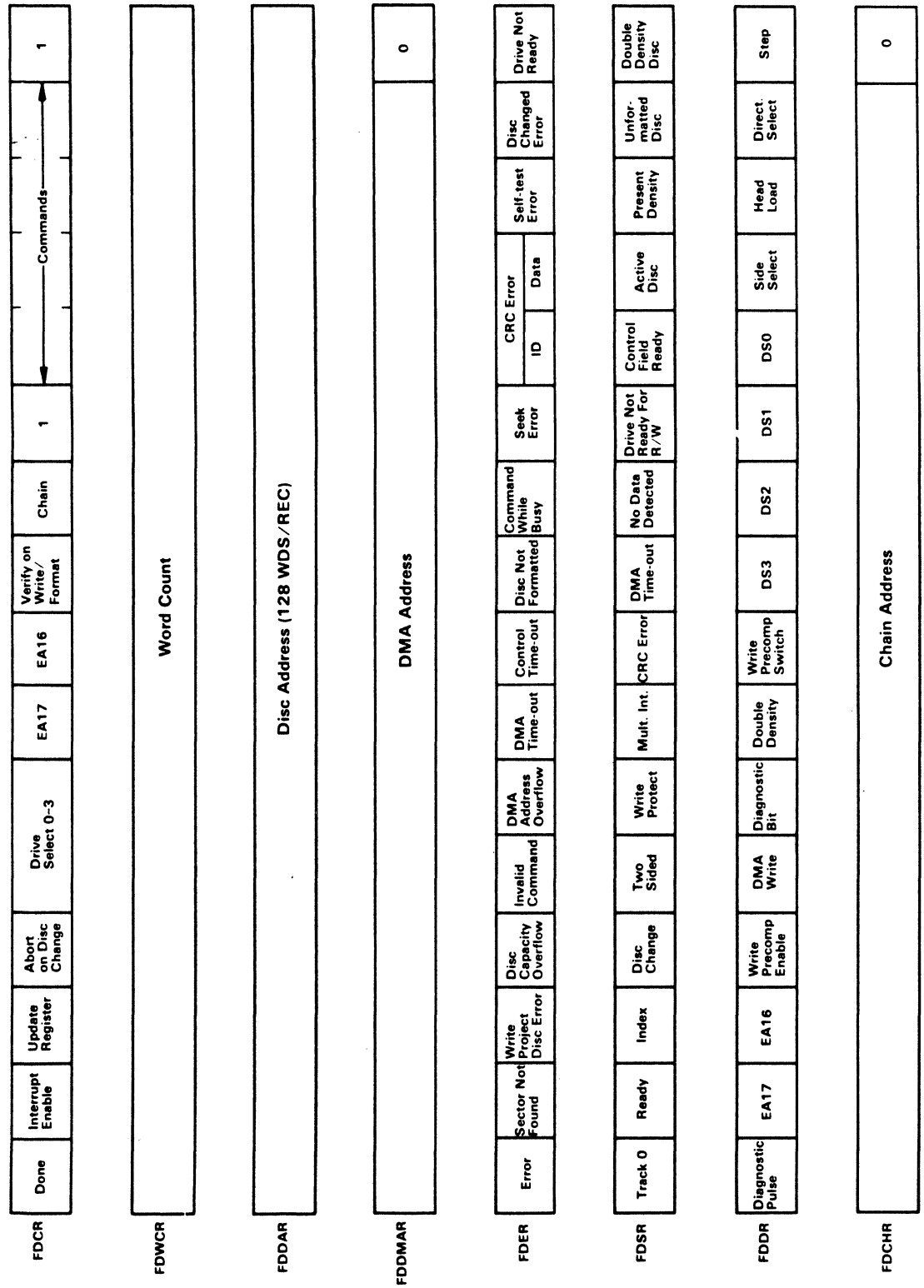


Fig. 1-10. Control Buffer Registers.

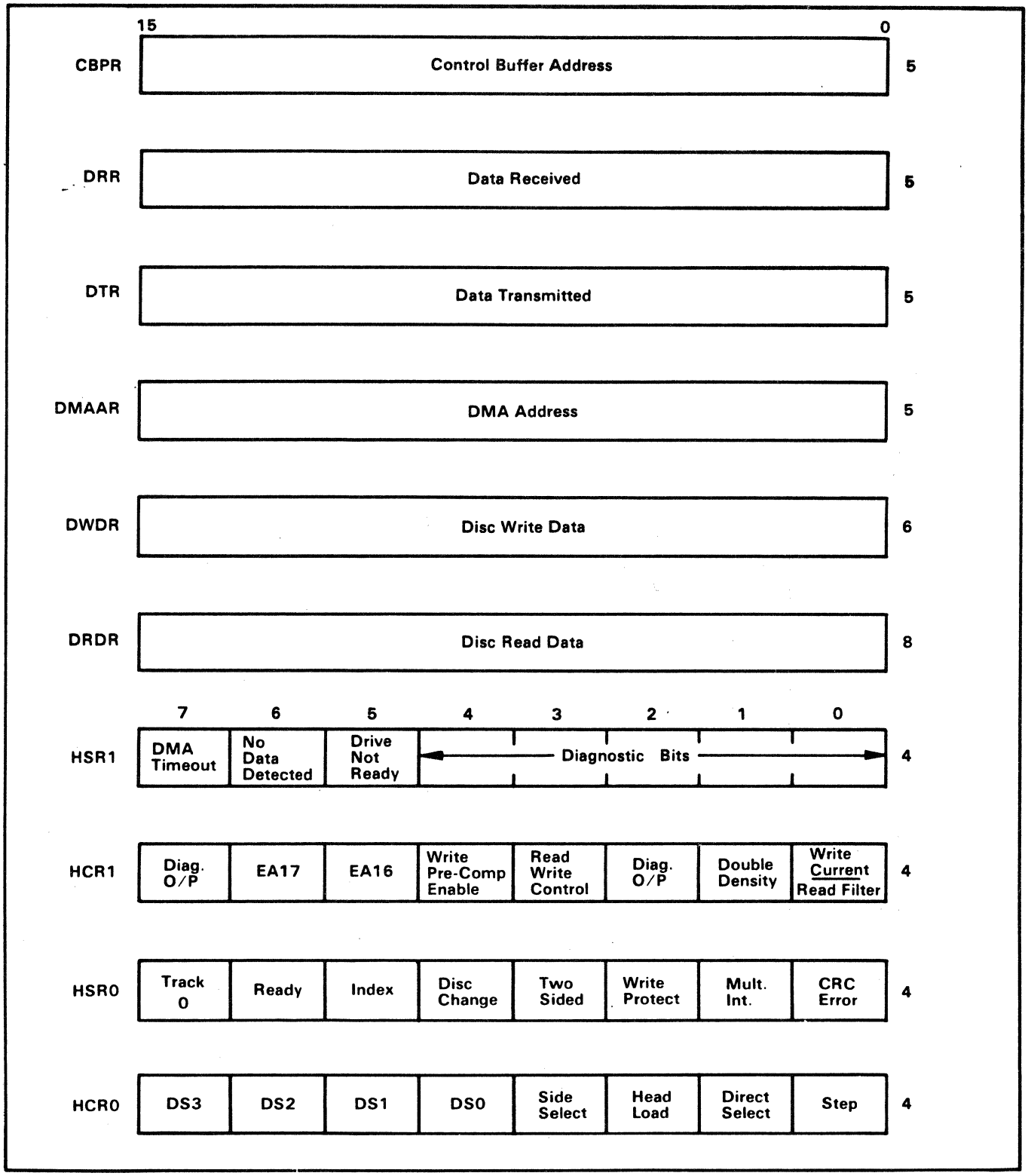


Fig. 1-11. Z80A Addressable Registers.

Power Supply. The 8501 employes a high efficiency, half bridge, switching power supply. Low line voltage protection is provided to shut down the supply at input voltages below 90 VRMS (180 VRMS for 215 VRMS line). Short circuit protection is provided by the internal current fold-back circuit which will attempt to restart every 1 to 1.5 seconds until:

1. the short is removed;
2. the AC line is disconnected;
3. the supply is turned off using the rear panel power switch; or
4. the DC switch is turned "OFF" on the front panel.

The +5 Vdc output is adjustable. The +12 Vdc and +24 Vdc supplies track the +5 Vdc supply proportional to the ratio of their output voltages. The output of the -12 Vdc supply is fixed.

A +15 Vdc line is also made available for DC power control. Note that +15 V is the only dc voltage not controlled by either the front panel or the rear panel mounted remote control connector, BNC 1. For more details on remote control functions (involving BNC 1 and BNC 2) refer to the "Communications Adapter Board" in Section 11. Further description of the power supplies is provided in Section 13. Electrical specifications for the 8501 are included in Section 6 of this volume.

OPTIONAL ACCESSORIES

- 8501 Data Management Unit Service Manual
- Extender card set, comprising:
  a. DEC dual extender card (for LSI-11/2)
  b. Card cage extender card
  c. Power supply extender card
- Blank Flexible discs (double sided, box of 10)

RELATED MANUALS

TITLE	PUBLICATIONS NO.
Microcomputer Handbook (DEC)	EB-07948-53/77
Microcomputer Users Guide (DEC)	EK-LSI11-UG-001
8301 Microprocessor Development Unit Service Manual	
8550 Microcomputer Development Lab Users Manual	
8550 Microcomputer Development Lab Reference Booklet	
8550 Microcomputer Development Lab Installation Guide	

Section 2

INSTALLATION

INTRODUCTION

This section describes installation for the 8501 Data Management Unit. The material in this section includes:

- o site preparation guidelines
- o recommended unpackaging and inspection procedures
- o installation, describing the initial set-up
- o checkout which includes both initial power-up information and an introduction to the diagnostics.

A brief guide to storage and re-shipping is also included.

SITE SELECTION

The area selected should be adequately lighted, air-conditioned, and dust-free. The area should also be as low as possible in electrostatic and electromagnetic interference in order not to degrade system performance.

General requirements for operating space and access are shown in Fig. 2-1, and include:

- o Allowance should be made for adequate air exhaust at the rear (6" Min. recommended).
- o Care should be exercised when swiveling the unit on the bench, so that the air intake at the front is not drawing in hot exhaust air from an adjacent unit.
- o A convenient operating arrangement exists when the incoming power cable is routed from the left side of the 8501 (looking from the front) and terminals and related equipment on the right. This arrangement avoids cross-over of power and signal cables.
- o Refer to the 8550 Microcomputer Development Lab Installation Guide for total system planning.

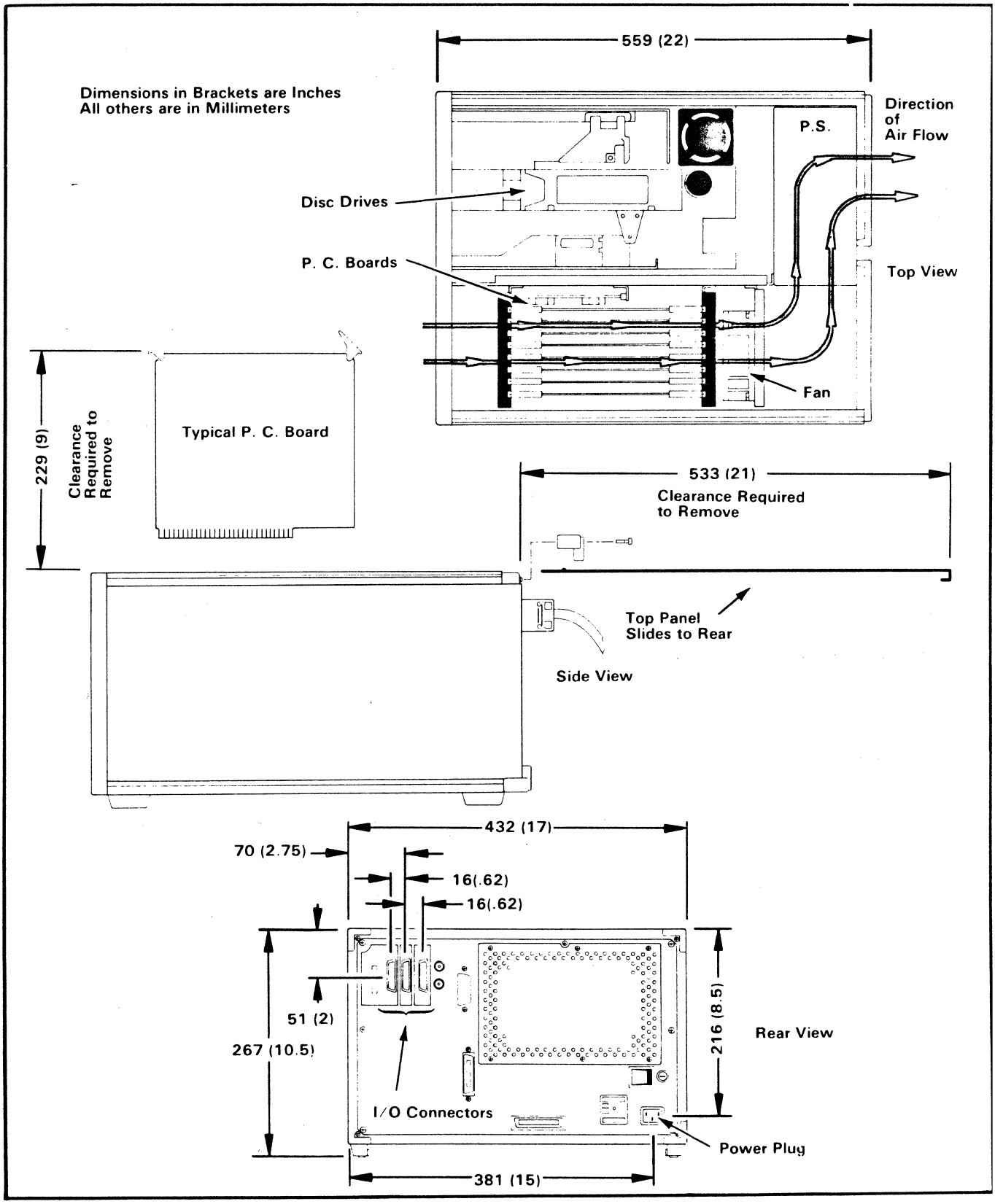


Fig. 2-1. 8501 outline dimensions.

UNPACKING

The 8501 is packaged and shipped in a heavy-duty cardboard container. Before unpacking the 8501 DMU, an inspection should be made of the outside of the carton. If any damage is evident:

1. Immediately notify the carrier who made delivery, and request inspection.

2. Immediately notify the nearest Tektronix Field Service Center.

3. Do not throw away the packing material.

4. DO NOT ATTEMPT TO REPAIR THE INSTRUMENT.

A recessed area within each container holds all cables and probes etc., which have been ordered or are standard with the unit. These items are taped down and then overlayed with foam padding. Accompanying manuals are normally shipped at the same time as the 8501, but in a separate padded cardboard container.

The unit is easily removed by carefully cutting the masking tape and laying the box on either of its two largest sides. The carton can then be slid off exposing the inner packing. Care should be taken when removing the packing material, since the recessed area containing the cables etc may be beneath the unit. Do not discard the carton or packing material. It will be required if you later have to transport the 8501.

Once the 8501 is free of external packing material, check the front openings of the two flexible disc drives for additional internal packing. These drives are OEM items and shipping techniques may alter, subject to the disc drive manufacturers recommendations and practices.

The 8501 is also supplied with an internal circuit board restrainer, however the unit will function satisfactorily with the restrainer continually in place. If the restrainer needs to be removed for any reason, access may be made by removing the screws and plastic feet at the rear of the top cover plate. Slide the cover plate to the rear (see Fig. 2-1). The retainer can now be removed by undoing two screws and lifting up one of the two fluted clamping plates at either end of the restrainer panel. The rest of the restrainer can then be lifted upwards, and clear of the circuit board edges.

INSTALLATION PROCEDURES

Line Voltage Selection

CAUTION

After arriving at the site of operation, the following procedures must be carried out before any connection to a power supply is made. Refer to Fig. 2-2 while reading this procedure.

- Ensure that both front and rear power switches are OFF.
- Check that the cover over the rear panel selector switch reads the correct line value. The inside of each cover (115 and 230 V) is designed to defeat a switch setting which is not compatible with the voltage range printed on the front.

NOTE

For line voltage changes, call your nearest Tektronix Service Center. Changes from 115 V to 230 V and vice versa, entail replacement of the fan and changes to the floppy disc drives, in addition to fuse and selector switch adjustments.

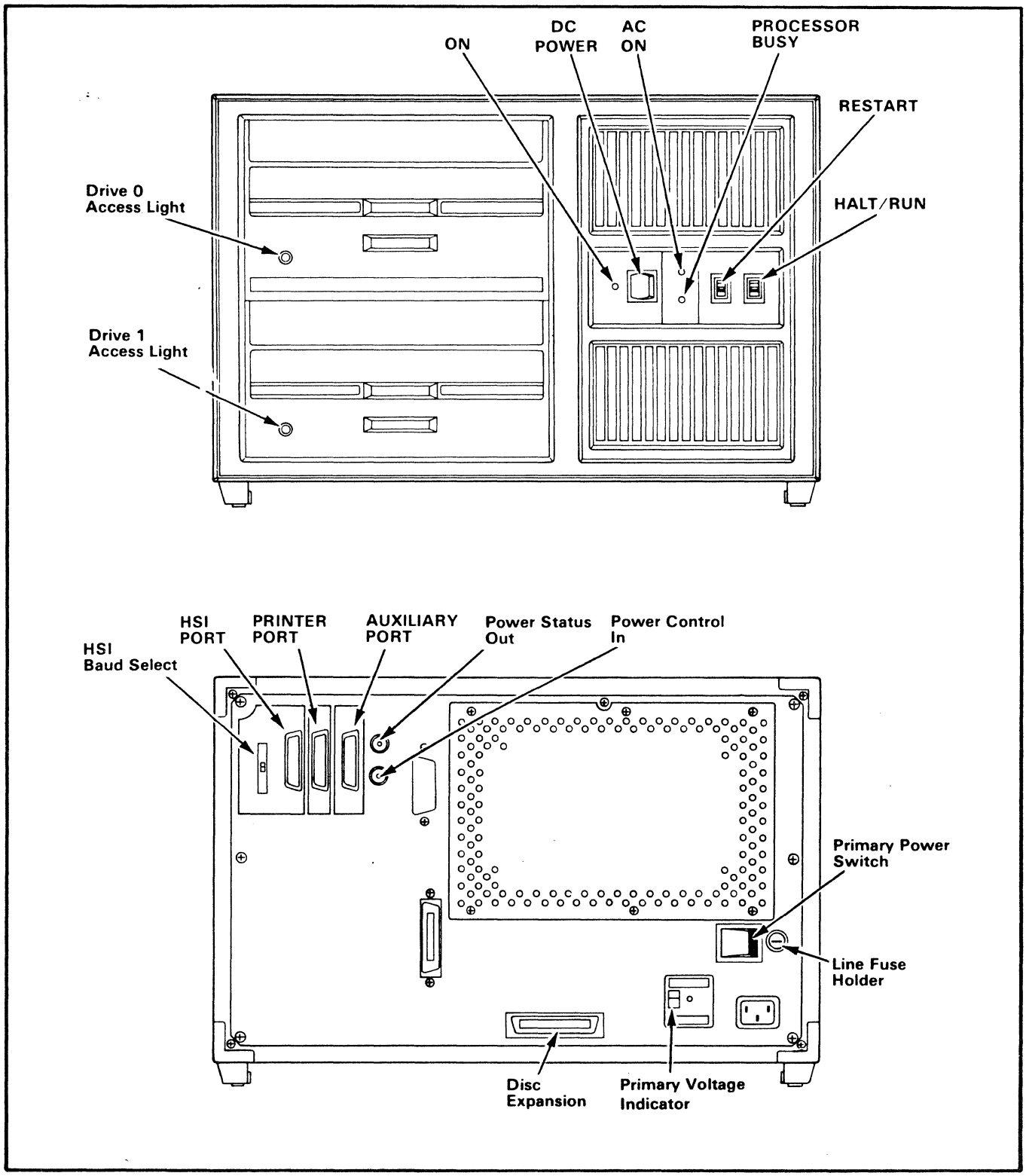


Fig. 2-2. 8501 front and rear panels.

- Remove the fuse and check that the correct value fuse is installed (250 V, 2A for 115V 60Hz operation).

Circuit Board Installation

Remove the top cover by removing the screws on the top rear corner stops, and sliding the cover to the rear. Check that the proper sequence of circuit boards are installed (refer to Fig. 2-3).

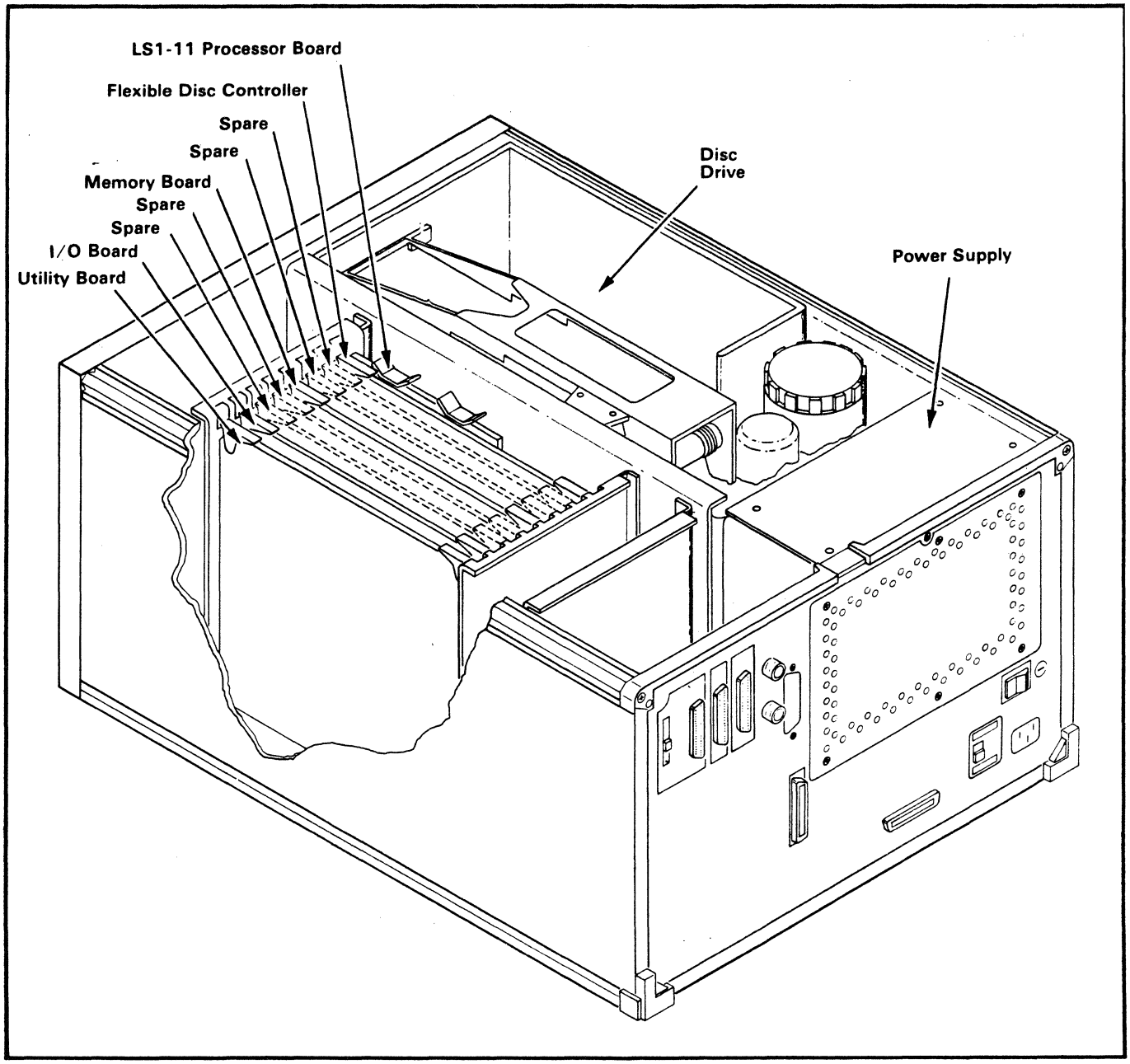


Fig. 2-3. 8501 circuit board configuration.

Bus Grant Jumpers are situated adjacent to all circuit board connectors except the Processor and Utility board. Refer to Fig. 2-4 and verify correct jumpering. Pass mode "A" is selected for all spare slots and memory. All other card slot positions should be jumpered for the no-pass condition "B". If it becomes necessary to change jumper positions, remove the adjacent board(s) and use needle nose pliers to reposition the jumper.

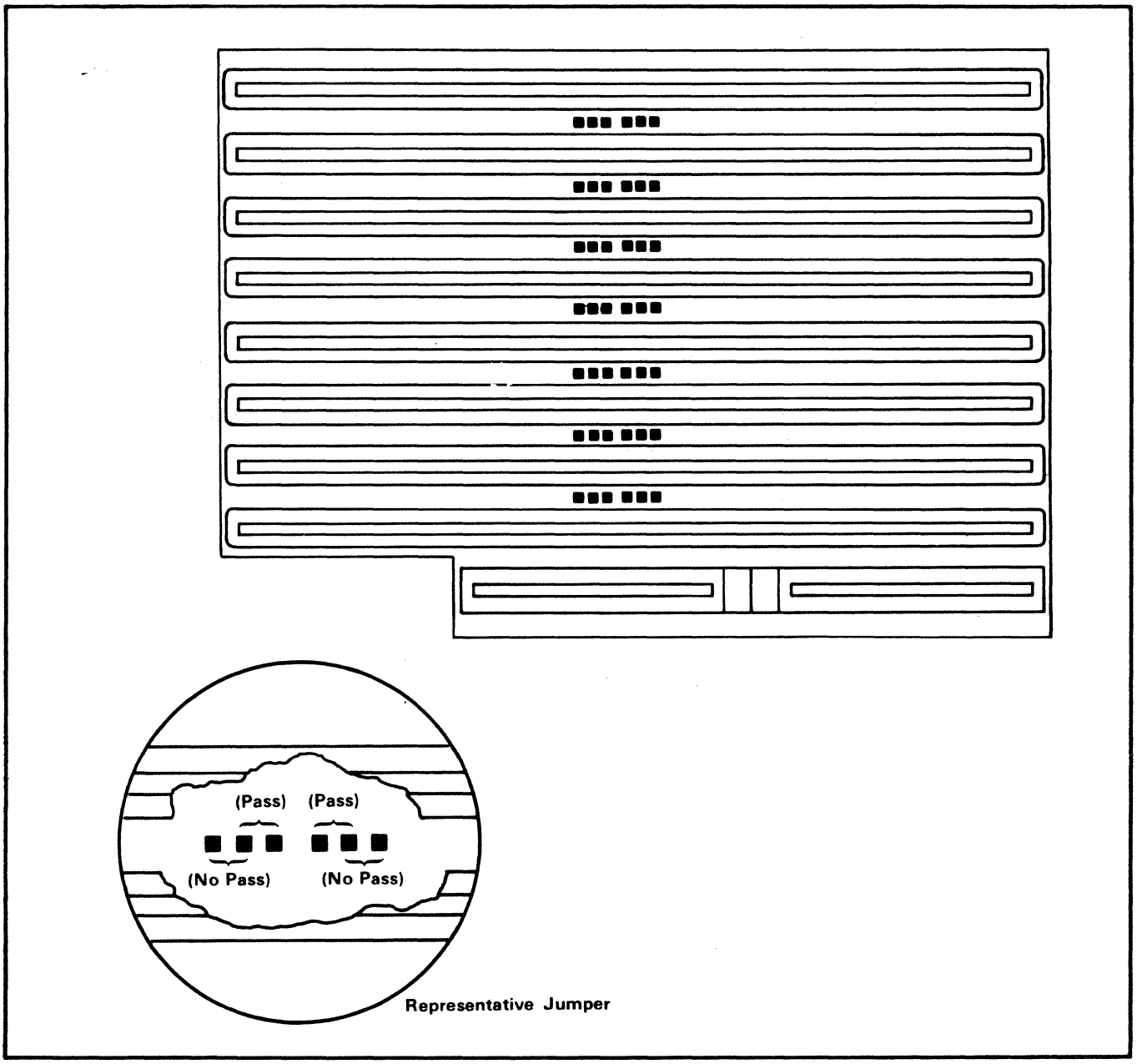


Fig. 2-4. Grant Pass jumpers.

The following steps should be made to insure proper installation.

- Refer to "Strapping Options" at the end of this section to determine circuit board strap selections.
- Check that all circuit boards are firmly seated.
- Replace top cover panel.
- Set the HSI port baud rate to HSI.

POWER-UP PROCEDURE

1. Check that all installation procedures have been carried out.
2. Connect the line cord to the 8501 power receptacle and the power source.
3. Move the rear panel power switch to the "ON" position. The front panel "STANDBY" indicator will now come on.
4. Move the front panel DC switch to the "ON" position. The (DC) "ON" indicator will come on. If the Mode switch is in the "RUN" position the "PROCESSOR BUSY" indicator will also come on.

For operating information beyond this point, refer to the appropriate system user's manual. For unit verification information, see the appropriate system installation guide.

See Sections 3 and 4 of this Manual for information concerning diagnostic messages and routines.

STORAGE AND RESHIPPING

The 8501 should be stored or reshipped in the original container. If the container is not available the following considerations should be taken into account.

Reshipping

If reshipment to the factory or service center becomes necessary the following steps should be taken:

- Note on the rear panel the serial number of the unit and any other relevant numbers or symbols applicable to identification. (This information is required for fault notification correspondence which should be sent separately.)
- Wrap the unit in a durable waterproof material such as heavy polyethylene, and tape securely. This step should only be carried out in a dry atmosphere and with the unit cool to the touch.
- Pack the unit in a sturdy box (heavy cardboard is OK for land shipment), lined with 76 mm (three inches) of medium density foam or expanded polystyrene.
- Cables and adapters, etc., should be wrapped separately and attached by tape to the inner liner at a break in the foam, or taped to a separate platform mounted above the foam or polystyrene (i.e., as used in original shipment). In the latter case a sheet of 25 mm (one inch) minimum thick foam should be taped above the cable package.
- Seal the box with reinforced sealing tape and identify the sender, the unit number, and the serial number, on the outside of the carton.
- As a general rule, notification and acknowledgment should precede dispatch of the unit.

Storage

The recommended maximum environmental conditions for unit storage:

- Temperature: -40 C to +66 C (-40 F to +151 F).
- Humidity: 10 to 90% (non-condensing).

While in storage the unit should be protected from settling dust. Avoide stacking the 8501 with other units.

STRAPPING OPTIONS

The figures contained in this sub-section illustrate the strapping options available on 8501 boards. Most strapping options consist of either a single two-pin jumper option specified in the tables as installed (IN) or removed (OUT), or a selection between two or more alternatives (typically A or B). Another strapping option used in the 8501 consists of a soldered wire strap that must be unsoldered and repositioned.

Following each figure is a table that lists the default setting of each jumper or strap on the board. A description of each jumper or strap's function follows the default table.

The circuit boards are discussed in the following order:

1. LSI-11/2 Processor
2. 32K Memory
3. Utility Board
4. Communications Adapter
5. I/O Board
6. Flexible Disc Controller

LSI-11/2 Processor

There are three straps on the LSI-11/2 processor board (shown in Fig. 2-5). Table 2-1 illustrates the default position for each strap.

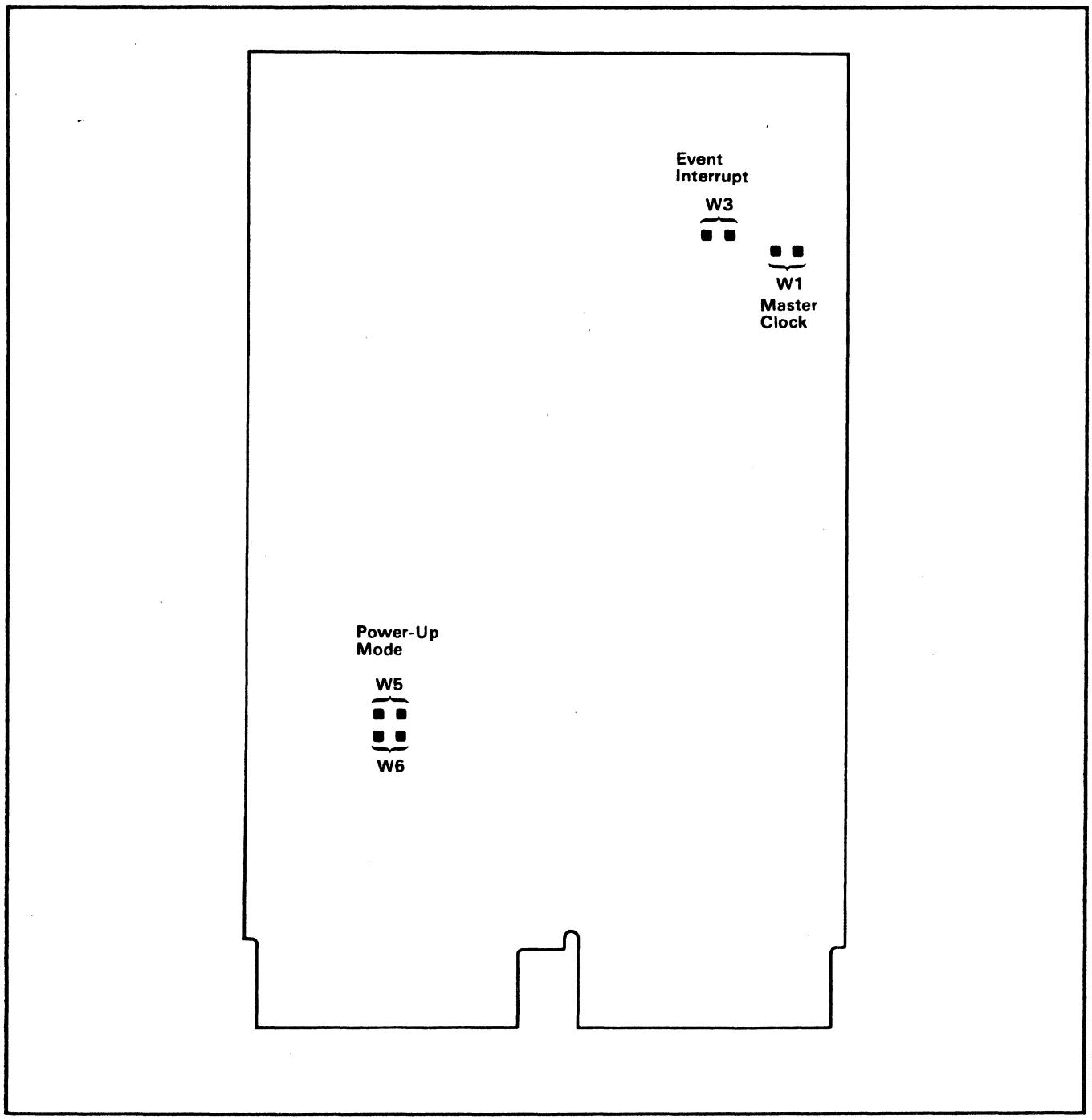


Fig. 2-5. LSI-11/2 strap selections.

Table 2-1
LSI-11/2 Default Strap Positions

Strap	Function	Default Position
W1	Master Clock	OUT
W3	Event Interrupt	OUT
W5	Power-Up Mode	OUT
W6	Power-Up Mode	IN

Master Clock Enable. Strap W1 enables the LSI-11/2 Master Clock. The strap is removed only when testing the LSI-11/2 clock circuitry.

Event Interrupt. Strap W3 enables or disables the LSI-11/2 event interrupt circuitry. When W3 is installed, the EVNT interrupt is assigned as the highest priority external interrupt.

Power-Up Mode . Straps W5 and W6 control the LSI-11/2 power-up sequence. There are four power-up modes available with the LSI-11/2. See the Microcomputer Handbook published by Digital Equipment Corporation for more information.

32K Memory

The 32K Memory board contains eight jumpers as shown in Fig. 2-6. Table 2-2 illustrates the default position for each jumper.

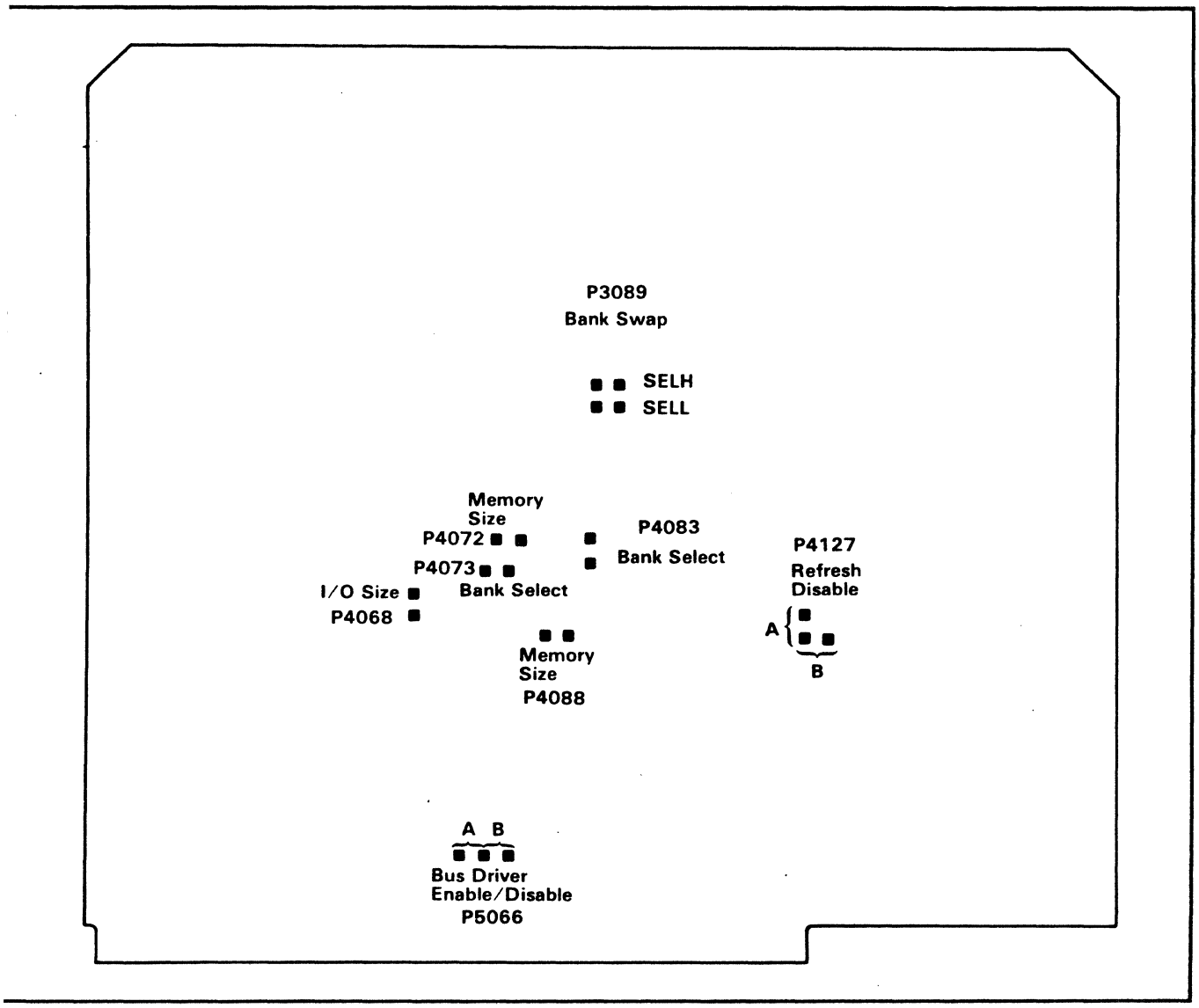


Fig. 2-6. 32K Memory jumper positions.

Table 2-2
32K Memory Default Jumper/Strap Positions

Jumper	Function	Default Position
P3089	Bank Swap	SELL
P4072	Memory Size	Don't Care
P4088	Memory Size	OUT
P4083	Bank Select	OUT
P4073	Bank Select	OUT
P4068	I/O Space	IN
P4127	Refresh Enable	B
P5066	Bus Drive Enable	A

Bank Swap. The 32K Memory board contains two banks of memory: 0 -- 77776 (low bank) and 100000 -- 177776 (high bank). Jumper P3089 matches the physical memory devices to the address banks. If P3089 is in the SELL position, devices U2010 through U2160 act as the low bank, and devices U1010 through U1160 act as the high bank. If P3089 is in the SELH position, devices U2010 through U2160 act as the high bank, and devices U1010 through U1160 act as the low bank. The default position for P3089 is SELL.

Memory Size. Jumpers P4072 and P4088 select memory size. The 32K Memory board can be configured to exist as 32K-words, or as a low-order or high-order 16K-word memory. Table 2-3 illustrates the positions of P4072 and P4088 for each circumstance.

Table 2-3
Memory Size Configuration

P4088	P4072	Memory Size
OUT	X	32K-Words
IN	OUT	Lower 16K
IN	IN	Upper 16K

Bank Select. Jumpers P4073 and P4083 select the memory address range of the 32K Memory board. Table 2-42-7 gives the address ranges you can select with P4073 and P4083.

Table 2-4
Memory Size

P4073	P4083	Starting/Ending Address
OUT	OUT	000000/177777
OUT	IN	200000/377777
IN	OUT	400000/577777
IN	IN	600000/777777

I/O Space. Jumper P4068 selects the 8501 I/O address size and location. If P4068 is OUT, 4K-words of I/O space are assigned, from 160000 -- 177777. If P4068 is IN, 2K-words of I/O space are assigned, from 170000 -- 177777.

Refresh Enable. Jumper P4127 enables or disables memory refresh. If P4127 is in position A, memory refresh is disabled. If P4127 is in position B, memory refresh is enabled. If P4127 is removed entirely, memory is contantly refreshed (jumper P5066 must be in position B before P4127 can be removed).

Bus Driver Enable. Jumper P5066 enables or disables the transfer of information from or to the 32K Memory board. In position A, the bus drivers are enabled. In position B, the bus drivers are disabled.

Utility Board

The Utility board contains a number of jumpers and wire straps that control interrupt vectors, RS-232 port baud rates, parity, line printer control, front panel power control, and diagnostic and boot ROM control. Figure 2-7 illustrates the Utility board. Table 2-5 shows all the jumpers and straps and their default positions.

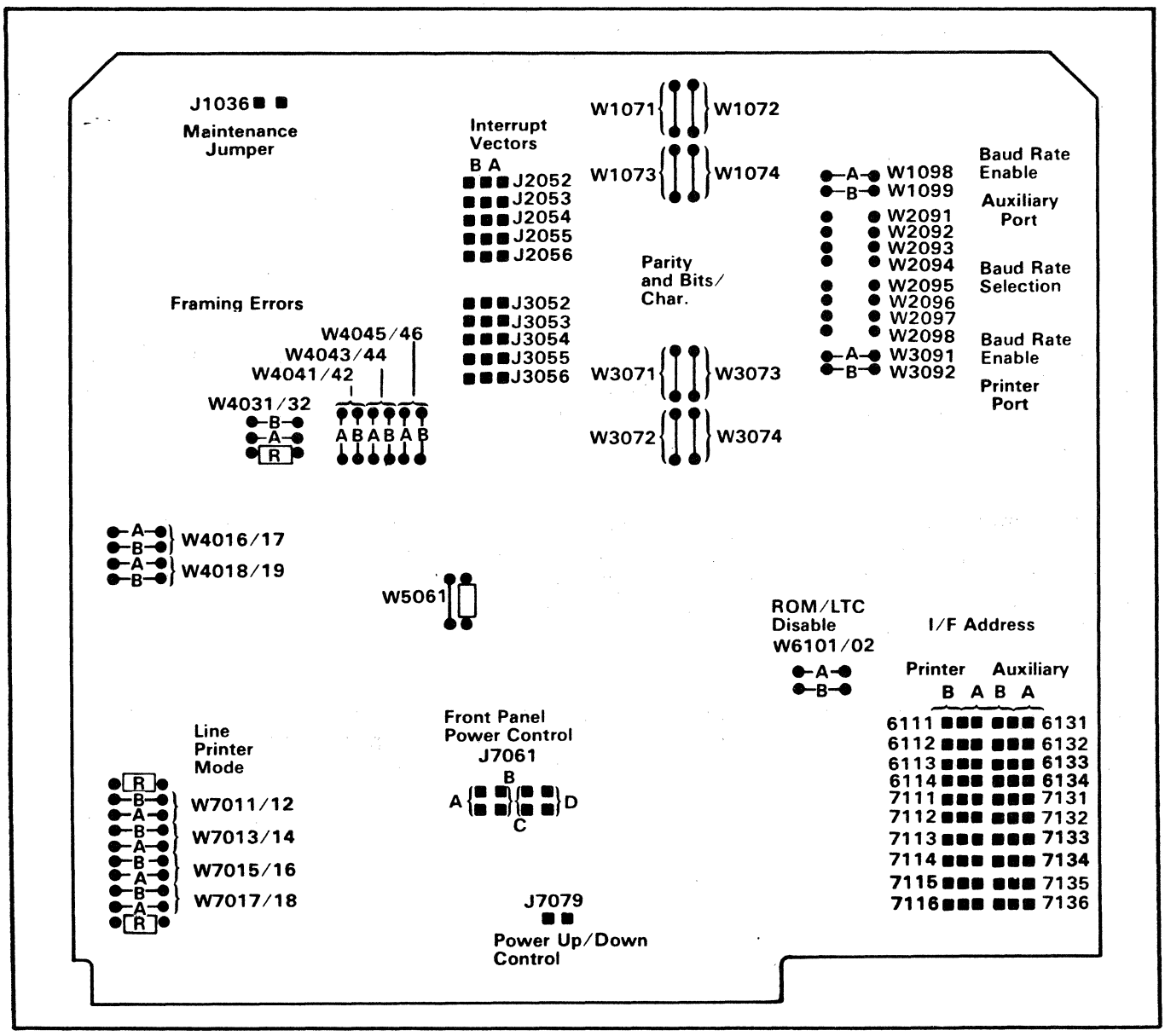


Fig. 2-7. Utility board strap and jumper locations.

Table 2-5
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
P1036	Maintenance	IN
W4031/32	Framing Error	A
W4041/42	Framing Error	A
W4043/44	Framing Error	A
W4045/46	Framing Error	B
W5061	Framing Error	IN
J2052	AUXILIARY Port Int. Vector	B
J2053	AUXILIARY Port Int. Vector	A
J2054	AUXILIARY Port Int. Vector	A
J2055	AUXILIARY Port Int. Vector	A
J2056	AUXILIARY Port Int. Vector	A
J3052	PRINTER Port Int. Vector	B
J3053	PRINTER Port Int. Vector	A
J3054	PRINTER Port Int. Vector	B
J3055	PRINTER Port Int. Vector	A
J3056	PRINTER Port Int. Vector	B

Table 2-5 (Cont.)
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
W3071	PRINTER Port 8 Bits/Char.	OUT
W3072	PRINTER Port No Parity	OUT
W3073	PRINTER Port No Parity	OUT
W3074	PRINTER Port 8 Bits/Char.	OUT
W1071	AUXILIARY Port 8 Bits/Char.	OUT
W1072	AUXILIARY Port No Parity	OUT
W1073	AUXILIARY Port No Parity	OUT
W1074	AUXILIARY Port 8 Bits/Char.	OUT
W1091	PRINTER Port Prg Baud Enbl	OUT
W1092	PRINTER Port Prg Baud Enbl	IN
W1098	AUXILIARY Port Prg Baud Enbl	IN
W1099	AUXILIARY Port Prg Baud Enbl	OUT

Table 2-5 (Cont.)
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
W2095	PRINTER Port 2400 Baud	IN
W2096	PRINTER Port 2400 Baud	OUT
W2097	PRINTER Port 2400 Baud	OUT
W2098	PRINTER Port 2400 Baud	OUT
W2091	AUXILIARY Port 2400 Baud	OUT
W2092	AUXILIARY Port 2400 Baud	OUT
W2093	AUXILIARY Port 2400 Baud	OUT
W2094	AUXILIARY Port 2400 Baud	IN
W7011/12	PRINTER Port Non LAV-11	B
W7013/14	PRINTER Port Non LAV-11	A
W4016/17	PRINTER Port Non LAV-11	B
W7015/16	AUXILIARY Port LAV-11	A
W7017/18	AUXILIARY Port LAV-11	B
W4018/19	AUXILIARY Port LAV-11	A

Table 2-5 (Cont.)
Utility Board Default Jumper/Strap Positions

Strap or Jumper	Function	Default Position
J7061	Front Panel OR Remt Pwr Cntrl	D
W6101/02	ROM and LTC Enable	A
W6112 -- W6114	PRINTER Port Interface Addr	A
W7111	PRINTER Port Interface Addr	A
W7112	PRINTER Port Interface Addr	B
W7113	PRINTER Port Interface Addr	A
W7114 -- W7115	PRINTER Port Interface Addr	B
W7116	PRINTER Port Interface Addr	A
W6131 -- W6134	AUXILIARY Port Interface Addr	A
W7131	AUXILIARY Port Interface Addr	A
W7132	AUXILIARY Port Interface Addr	B
W7133 -- W7135	AUXILIARY Port Interface Addr	A
W7136	AUXILIARY Port Interface Addr	B
J7079	Power Control Enabled	IN

Maintenance. When jumper P1036 is installed, the 8501 runs through its normal power-up sequence. If P1036 is removed, the 8501 enters the ROM-based diagnostics mode, and all communication with the 8501 will be through the AUXILIARY port.

Framing Error. The framing error straps (.bold W4031/32, W4041/42/43/44/45/46, and W5061) determine what the LSI-11/2 will do if a framing error is detected at one of the 8501 I/O ports. Table 2-6 lists the possible actions.

Table 2-6
Framing Error Straps

Port	W4031/ 4032	W4041/ 4042	W4043/ 4044	W4045/ 4046	W5061	
HSI	A	B	A	A	IN	RESTART @ 173000
	B	B	A	A	X	HALT
	A	B	A	A	OUT	HALT @ 173000
PRINTER	A	A	B	A	IN	RESTART @ 173000
	B	A	B	A	X	HALT
	A	A	B	A	OUT	HALT @ 173000
AUXILIARY	A	A	A	B	IN	RESTART @ 173000
	B	A	A	B	X	HALT
	A	A	A	B	OUT	HALT @ 173000

Port Interrupt Vectors. The AUXILIARY and PRINTER port interrupt vectors are strap selectable. The upper five bits of each eight-bit vector can be selected using J2052 through J2056 for the AUXILIARY port, and J3052 through J3056 for the PRINTER port. The "A" position for each jumper equals 0, and the "B" position equals 1. J2052 and J3052 set the most significant bits (bit 7), and J2056 and J3056 set the least significant bits (bit 3).

Parity and Bits/Character. Wire straps allow you to configure the parity and bits/character for the AUXILIARY and PRINTER ports. Table 2-7 lists the settings for each port.

Table 2-7
Parity and Bits/Character

PRINTER	W3071	W3072	W3073	W3074
AUXILIARY	W1071	W1072	W1073	W1074
8 Bits/Character	OUT	X	X	OUT
7 Bits/Character	IN	X	X	OUT
6 Bits/Character	OUT	X	X	IN
5 Bits/Character	IN	X	X	IN
Even Parity	X	OUT	IN	X
Odd Parity	X	IN	IN	X
No Parity	X	X	OUT	X

Programmable Baud Rate. The baud rate of both the PRINTER and AUXILIARY ports can be set be software, or by wire straps on the Utility board. The software programmable feature can be disabled by W1098/W1099 (AUXILIARY) and W1091/W1092 (PRINTER). To disable the programmable feature of the AUXILIARY port, remove W1098 and install W1099. To disable the programmable feature of the PRINTER port, remove W1092 and install W1091. See the appropriate system Users Manual for more information on programming the AUXILIARY and PRINTER ports.

Port Baud Rate Selection. The PRINTER and AUXILIARY port baud rates can be selected by wire straps on the Utility board. Table 2-8 lists the settings for each port.

Table 2-8
Baud Rate Selection Straps

PRINTER Port	W2095	W2096	W2097	W2098
AUXILIARY Port	W2094	W2093	W2092	W2091
External Clock	IN	IN	IN	IN
50 Baud	IN	IN	OUT	IN
75 Baud	IN	IN	OUT	OUT
110 Baud	OUT	OUT	OUT	OUT
134.5 Baud	IN	OUT	IN	IN
200 Baud	IN	OUT	IN	OUT
300 Baud	OUT	OUT	IN	OUT
600 Baud	IN	OUT	OUT	IN
1200 Baud	OUT	IN	OUT	OUT
1800 Baud	OUT	IN	OUT	IN
2400 Baud	IN	OUT	OUT	OUT
4800 Baud	OUT	IN	IN	OUT
9600 Baud	OUT	IN	IN	IN

Port Mode Selection. The AUXILIARY and PRINTER ports can be set to work in Digital Equipment Corporation's four LAV-11 modes. Or, the ports can be set to a non-LAV-11 mode. Table 2-9 lists the various modes and straps for each port.

Table 2-9
Port Mode Straps

PRINTER Port / AUXILIARY Port	W4016/4017 / W4018/4019	W7011/7012 / W7015/7016	W7013/7014 / W7017/7018
LAV-11 Mode: no TBMT hold-off	A	A	A
LAV-11 Mode: hold-off TBMT while CTS	A	B	A
LAV-11 Mode: hold-off TBMT while DSR	A	A	B
LAV-11 Mode: hold-off TBMT while CTS OR DSR	A	B	B
Non LAV-11 Mode	B	X	X

Front Panel Power Control. Jumper J7061 enables and controls the remote power control facility of the 8501. The 8501 dc power supply can be controlled by a remote device through the rear panel, or by the front panel switch, or by a combination of the two. The following is a list of options that can be selected by jumper J7061:

J7061	Control Condition
A	Remote power control only.
B	Front panel AND remote power control.
C	Front panel power control only.
D	Front panel OR remote power control.

ROM and LTC Enable. The power-up diagnostic ROM, boot-up ROM, and Line-Time Clock functions of the Utility board can be disabled for troubleshooting purposes. Straps W6101 and W6102 enable or disable the ROMs and LTC. Placing both straps in the "B" position disables the ROMs and LTC. Placing the straps in the "A" position enables both.

Port Interface Addresses. The interface addresses for the AUXILIARY and PRINTER ports can be selected by wire straps. Table 2-10 lists the straps and their address values.

Table 2-10
Port Interface Address Straps

PRINTER	W6111	6112	6113	6114	7111	7112	7113	7114	7115	7116
AUXILIARY	W6131	6132	6133	6134	7131	7132	7133	7134	7135	7136
Bit	12	11	10	9	8	7	6	5	4	3

To select a high or a low on a particular bit, set the corresponding strap to: A (= 1), or B (= 0). Bits 13 through 15 are always held high (in the A position), and are equivalent to bank 7 of I/O memory space (160000 -- 177770). Bits 1 and 2 of the address are under program control, and select one of four Utility board interface registers (see the description of the Utility board in Section 9 of this manual). Bit 0 is not used.

Power Control Enable. Jumper J7079 is used during troubleshooting to disable the power control facility of the Utility board. To disable the power control facility, remove J7079.

Communications Adapter

The Communications Adapter contains jumpers to select the interface standard, alternate baud rates, stop bits for the HSI port. Figure 2-8 illustrates the Communications Adapter board. Table 2-11 lists the default position of all jumpers.

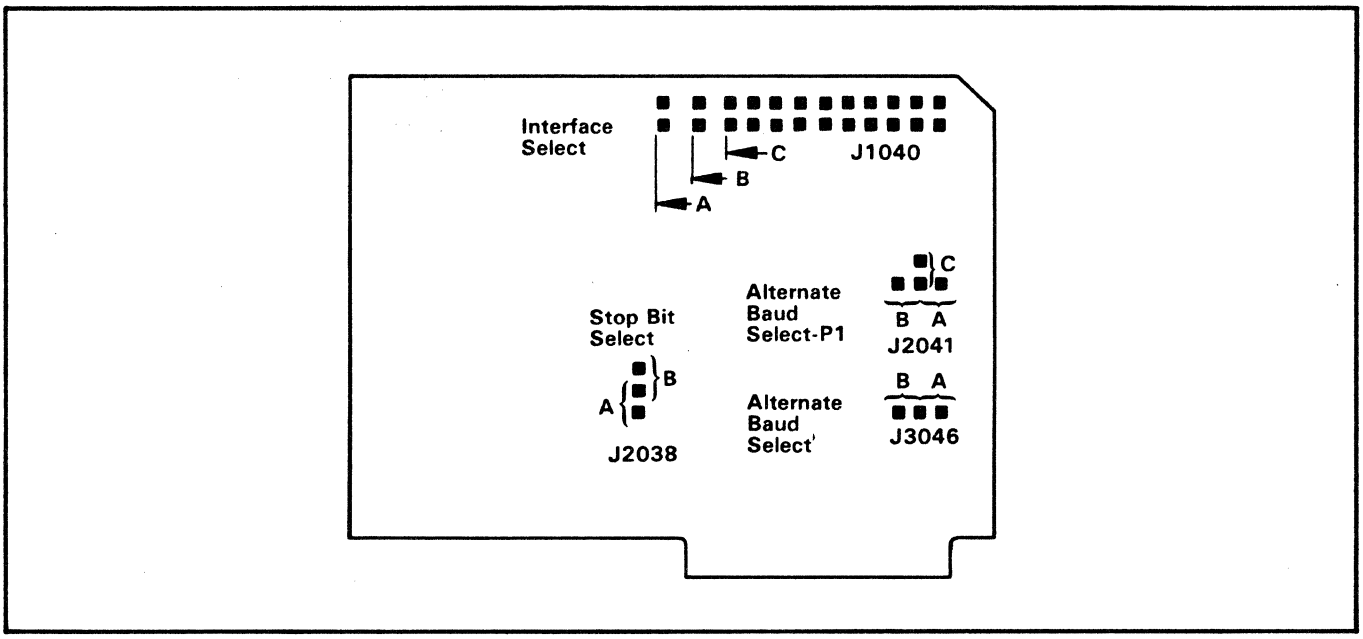


Fig. 2-8. Communications Adapter jumper locations.

Table 2-11
Communications Adapter Default Jumper Positions

Jumper	Function	Default Position
J1040	HSI Interface Type	A
J2038	HSI Stop Bit Select	A
J2041	HSI Alternate Baud @ 150 setting	A
J3046	HSI Alternate Baud @ HSI setting	A

Interface Type. The HSI port normally communicates as an RS-422 standard, but can be reconfigured to use RS-423 or RS-232. Jumper J1040 selects the standard. Set J1040 to the "B" position to select RS-423, or to the "C" position to select RS-232.

Stop Bit Select. The number of stop bits used by the HSI port can be changed from the default number (1 stop bit) to 2 stop bits by moving J2038 to the "B" position.

Alternate Baud Rates. Jumpers J2041 and J3046 alter the default baud rate of the HSI port when it is set to the 150 baud position or the HSI position. To change the default 150 baud rate to 110 baud, move J2041 to the "B" position. To change the default 150 baud rate to External Clock, move J2041 to the "C" position. To change the default HSI baud rate to 19.2K-baud, move J3046 to the "B" position.

I/O Board

Jumpers on the I/O board set the HSI port parity and bits/character, transmit ready characteristics, and I/O address. Figure 2-9 illustrates the I/O board. Table 2-12 lists the default position of all jumpers.

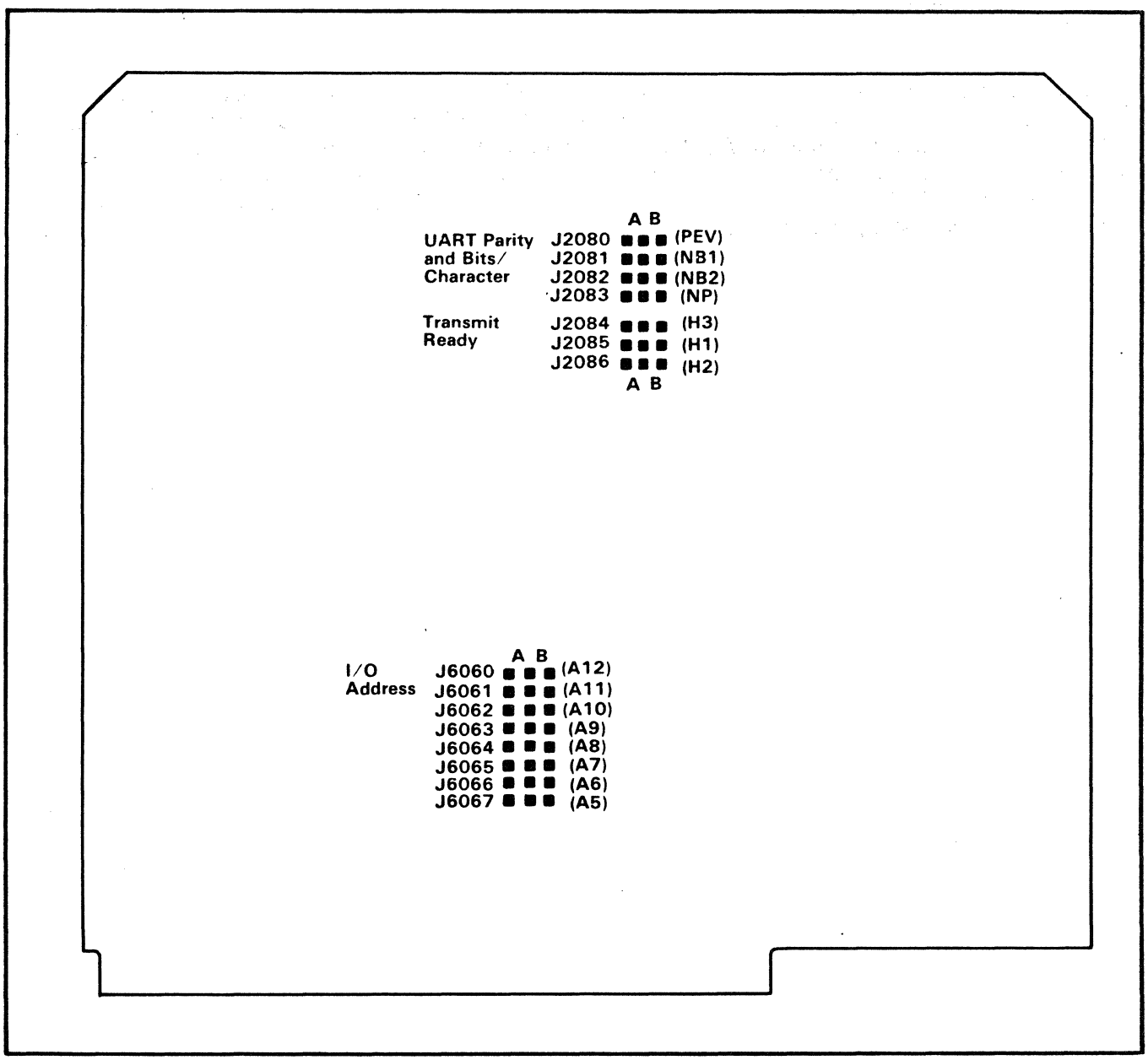


Fig. 2-9. I/O board jumper locations.

Table 2-12
I/O Board Default Jumper Positions

Jumper	Function	Default Position
J2080	Even Parity	B
J2083	Even Parity	A
J2081	8 Bits/Character	B
J2082	8 Bits/Character	B
J2084	Transmit Ready	A
J2085	Transmit Ready	A
J2086	Transmit Ready	A
J6060	Address Select	B
J6061	Address Select	B
J6062	Address Select	B
J6063	Address Select	A
J6064	Address Select	B
J6065	Address Select	A
J6066	Address Select	B
J6067	Address Select	A

Parity and Bits/Character. A universal asynchronous receiver/transmitter (UART) on the I/O board controls communications over the HSI port. The parity and number of bits per character is controlled by jumpers within on the I/O board. The parity and bits/character options are shown in Table 2-13.

Table 2-13
UART Parity and Bits/Character

Characteristic	J2080	J2081	J2082	J2083
8 Bits/Character	X	B	B	X
7 Bits/Character	X	A	B	X
6 Bits/Character	X	B	A	X
5 Bits/Character	X	A	A	X
Odd Parity	A	X	X	A
Even Parity	B	X	X	A
No Parity	X	X	X	B

Transmit Ready Straps. The transmit ready straps alter the HSI RS-422 control line protocol. There are five possible protocol configurations:

1. Transmit a BREAK. When the GO bit is set, reading the UART's XMIT RDY bit will cause the serial data out line to be asserted for 220 ns. This causes the UART to set its "framing error" flag, which is interpreted as a BREAK. To enter this mode, set: J2084 = B, J2085 = A, J2086 = A.

2. This configuration inhibits the CONSOLE MODE until the current DMA operation is complete. When the DMA operation is complete, CONSOLE MODE is entered in a normal fashion. To enter this mode, set: J2084 = A, J2085 = B, J2086 = A.

3. Abort DMA. When the GO bit is set, reading the XMIT RDY bit will cause the GO bit to be cleared and DMA ABORT to be set. To enter this mode, set: J2084 = A, J2085 = A, J2086 = B.

4. This configuration transmits a BREAK when the XMIT RDY bit is read. The CONSOLE MODE is entered in the normal manner when the DMA operation aborts and BREAK is complete. To enter this mode, set: J2084 = B, J2085 = A, J2086 = B.

5. This is the default mode. DMA and Transmit Ready are enabled. To enter this mode, set: J2084 = A, J2085 = A, J2086 = A.

I/O Board Port Address. The I/O board's port address can be altered with jumpers J6060 through J6067. Table 2-14 lists the jumpers and their corresponding address values.

Table 2-14
I/O Address Jumpers

Jumper	J6060	J6061	J6062	J6063	J6064	J6065	J6066	J6067
Bit	12	11	10	9	8	7	6	5

To set a high or low on a particular bit, set the corresponding jumper to: A (= 0), or B (= 1). Bits 13 through 15 are always held high (in the B position). This corresponds to bank 7 of the 8501's I/O space (160000 -- 177770). Bits 1 through 3 are under program control, and select one of eight I/O board interface registers (see Section 10 of this manual). Bits 0 and 4 are software control bits, and are independent of the address selection.

Flexible Disc Controller

The Flexible Disc Controller board uses jumpers to control data bus access, diagnostics, drive control, and several troubleshooting features. Figure 2-10 illustrates the jumper positions on the Flexible Disc Controller board. Table 2-15 lists the default positions for all jumpers.

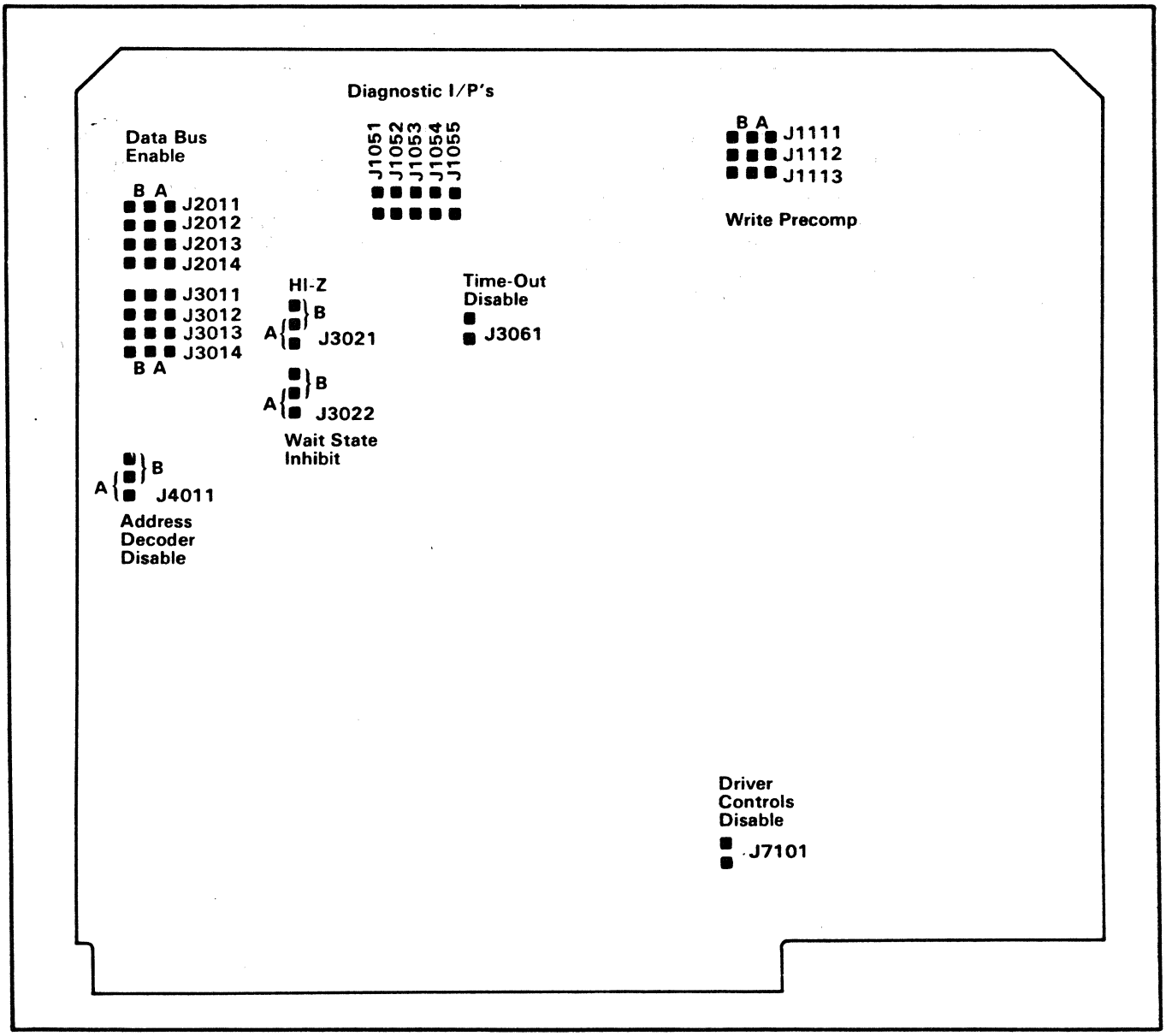


Fig. 2-10. Flexible Disc Controller Jumper Locations.

Table 2-13
Flexible Disc Controller Default Jumper Positions

Jumper	Function	Default Position
J2011 -- J2014	Data Bus Enable	B
J3011 -- J3014	Data Bus Enable	B
J1051 -- J1055	Diagnostic Input	OUT
J1111 -- J1113	Write Pre-Comp	B
J3061	Time-Out Disable	OUT
J3021	Hi-Z	B
J3022	Wait-State Inhibit	A
J4011	Addr Decode Disable	A
J7101	Driver Cntrl Disbl	OUT

Data Bus Enable. If jumpers J2011 through J2014 and J3011 through J3014 are move to the A position, the Controller's Z80 no longer has access to the 8501 bus.

Diagnostic Input. To force the Controller's register inputs to a low state, place jumpers in positions J1051 through J1055.

Write Precompensation. Jumpers J1111, J1112, and J1113 control the write pre-compensation time of the Controller. Moving J1111 through J1113 to the A position changes pre-compensation time to 250 ns. In the default position (B), write pre-compensation time is 188 ns.

Time-Out Disable. Placing a jumper in position J3061 disables the Disc Drive Controllers data time-out function.

Hi-Z. Jumper J3021 controls the Controller's Z80. When J3021 is placed in the A position, the Z80's address, data, and control lines are placed in a high-impedence state.

Wait-State Inhibit. When jumper J3022 is placed in the B position, wait-states are inhibited, and the Z80 will continue execution even if it's out of sync with the disc data transfer rate.

Address Decoder Disable. Jumper J4011 , when in the B position, disables the Disc Drive Controller's address decoder.

Drive Control Disable. When jumper J7101 is installed on the board, the Controller's drive control lines are disabled.

Section 3

ROM-BASED DIAGNOSTICS

INTRODUCTION

This section describes the selftesting diagnostics that are executed within the 8501 Data Management Unit during power-up or RESTART conditions. The diagnostics consist of five power-up tests, two verification routines, and three utility routines.

The power-up tests check the ROM, RAM, CPU, Line-Time Clock (LTC), and the Flexible Disc Controller (FDC). The verification routines verify the high-speed interface (HSI) port and the disc-track/sector alignment. The utility routines check the head alignment of the flexible disc drives, provide boot-up capability via the RS-232-C port.

Section 3 is organized into four parts:

- An introduction to the 8501 ROM-based diagnostics and some general background information. This part of the section includes test the summary.
- Detailed descriptions of the automatic power-up tests This part also describes the diagnostic diagrams and the five utility board LEDs.
- A description of the Debugging Mode including verification and utility routines.
- A troubleshooting section including descriptions of the Octal Debugging Technique (ODT), the ODT terminal, instructions for manual system boot-up, and the ODT command summary.

The Firmware

The 8501 power-up diagnostics are contained on two 1K X 8-bit ROMs. One ROM stores the high byte and the other stores the low byte of the 16-bit LSI-11/2 word. The diagnostics share the ROMs with the verification routines and utility routines, as shown in Fig. 3-1. The power-up tests reside in bank 0 and the verification and utility routines reside in bank 1.

The power-up tests are described under Test Descriptions. The verification and utility routines are covered with the Debugging Mode later in this section.

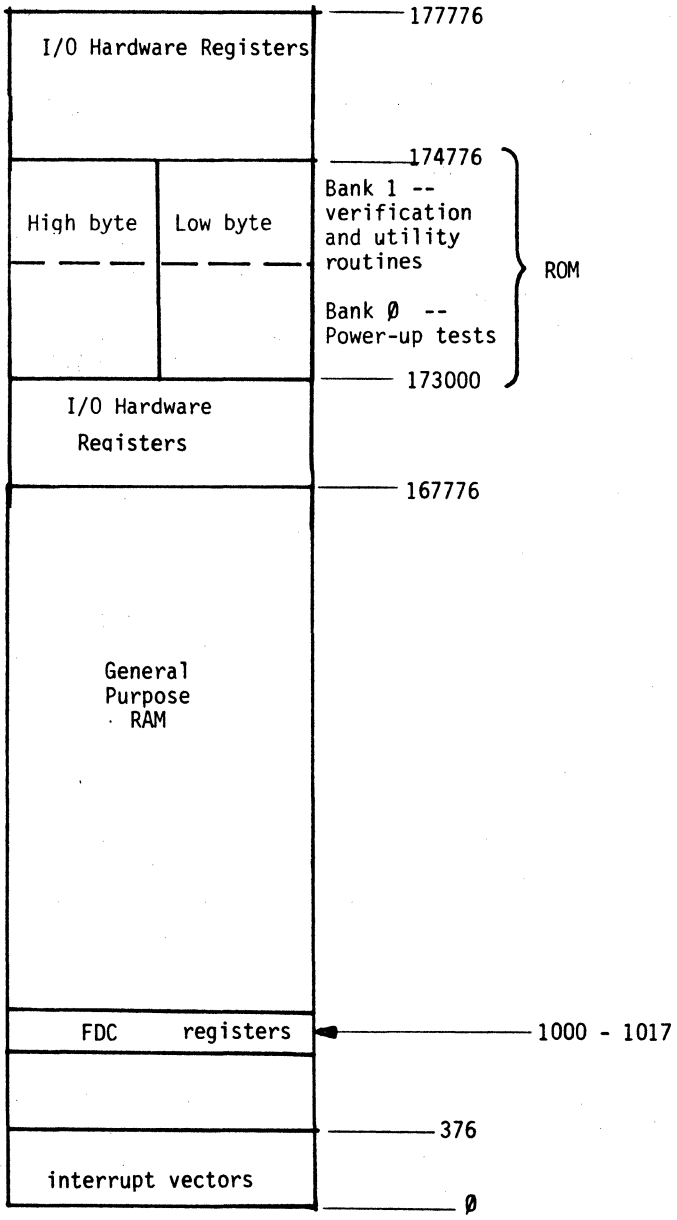


Fig. 3-1. 8501 system memory map.

Note: All addresses are shown in octal notation.

Hardware Restrictions

The power-up tests use the 8501 as the test instrument. The diagnostic firmware assumes that the LSI-11/2 processor and support circuits (power supplies, clock, and reset circuits) are operational.

The Utility Board LEDs

The Utility board contains five LEDs that represent octal numbers during the power-up sequence. You view the five LEDs with the cabinet lid removed (see the appropiate system installation guide). The LEDs are mounted along the Utility board's top edge with the least significant bit closest to the rear panel.

The power-up sequence lights the appropriate LED as the tests execute, thus allowing you to identify the last executed test or function before the sequence was HALTed. For example --**- = 06 (where the dash represents an unlit LED, and the asterisk represents a lit LED. The LED display for the power-up sequence is as follows:

37	unable to execute firmware
16	initialization error
00	RAM test error
01	PROM error (low byte)
02	ROM error (high byte)
03	CPU error
04	Line-Time clock error
05	FDC dead or missing
06	FDC interrupt error
07	FDC returned error status
11	monitor mode
12	bank switching error
10	trying to boot from flexible disc
13	starting an operator-selected test
14	8501 COMM mode
30	waiting for a bootable disc
31	executing secondary boot from flexible disc
37	operating system running

EXECUTING THE POWER-UP TESTS

The five power-up tests execute automatically every time you power up or RESTART the system. You can, however, execute any power-up test individually from the 8501 ODT terminal with the appropriate RE command. The RE commands are described in the Debugging Mode later in this section.

Operation

The five power-up tests execute every time you power up the system or toggle the front panel RESTART switch. The tests execute sequentially under control of the LSI-11/2 processor. The power-up sequence executes in about two seconds and gives reasonable assurance that the system is operational. Once all power-up tests have passed, the system boots automatically. If any power-up test fails, the diagnostics give control to the Debugging Mode. You can then use the LED readout to identify the failed circuit or run a verification or utility routine to determine the cause of the failure. You can also connect a terminal directly to the AUXILIARY port, loop on the failed test, and display the affected registers. In addition, a set of disc-based diagnostic programs, described in Section 4 of this manual, lets you delve deeper into the trouble areas.

Tables 3-1, 3-2,and 3-3 summarize the power-up , verification, and utility routines. The execution commands shown in the tables are described later in this section.

Table 3-1
Power-up Test Summary

Name	Command	Description
RAM Test	RE1	This test checks the system memory. It starts at location 10 and proceeds upward through all RAM locations. At each location, the test uses the address as data and stores it in the location. When all addresses are stored in their respective locations, the test starts at the highest address, reads its contents, and complements it. The test then proceeds downward through all lower locations reading their contents and complementing them. Upon reaching location 10 again the test reverses direction, reads all complemented addresses and clears them.
ROM Test	RE2	The ROM test performs a checksum test on the diagnostic ROMs located on the Utility board.
CPU Test	RE3	The CPU Test checks selected instructions and registers. The CPU test is a graduated test. It checks the simpler instructions first and the more complex ones last. This test also checks the contents of the sequencing registers and the CPU flags.
LTC Test	RE4	The line-time test clock uses the instruction timing to verify that the LTC interrupts the LSI-11/2 at the correct rate.
FDC Test	RE5	The FDC test verifies that the Flexible Disc Controller board is installed and at least partially operational. The FDC test also sends a status request to disc drive 0 and checks for the correct interrupt response and error status.

Table 3-2
Verification Routine Summary

Name	Command	Description
Disc Track/Sector Verification	VEn	This routine verifies tracks and sectors on both disc sides. The resulting data is stored in the interface registers and then displayed on the terminal screen.
High Speed Interface Verification	HSn	The HSI verification exercises the DMA transmit/receive logic. Upon completion it displays the HSI register contents.

Table 3-3
Utility Routine Summary

Name	Command	Description
Head Align Routine	ALn	This routine moves the head to the innermost tracks and then back to track 40 . The routine requires an alignment disc and oscilloscope to check head alignment.
Manual Boot Routine	FDn	The FDn routine boots from the system disc if the automatic boot-up routine did not work or if you had a power-up failure.
RS-232 Loader Routine	RS	The RS routine checks the operation of the RS-232-C serial port 1.

Commands

Power-up diagnostics commands are either in the format REn, or the format XXn. The REn commands are used for single execution of the five automatic tests. The n identifies the numeric order in which the test runs automatically. The Power-up test descriptions later in this section give the command for each test. The XXn command format is used by the verification and utility routines. In this format XX identifies the test mnemonic and n identifies the parameter. The Verification and Utility routine descriptions later in this section give the commands for each routine.

The Diagnostic Diagrams

The 8501 power-up tests are described with the aid of diagnostic flow diagrams. These diagrams show how the firmware exercises the various system components. The diagrams describe the overall effect of a combination of instructions. Figure 3-2 shows an example of the diagram format. Actions or conditions are contained in brackets and are normally located near the center of the page. The boxes on either side represent hardware devices or controlling devices either acting or being acted upon. Some example of hardware devices include:

- o a complete unit (system terminal)
- o a circuit board (system memory)
- o a controlling device (system processor)
- o part of a device

A small diamond leaving a device box indicates a decision. If the action described in the brackets is true the action is transfered in the direction of the arrow.

The five diagnostic LEDs are shown with the most significant position on the left. A "1" indicates that the LED is lit, and a "0" indicates that is not.

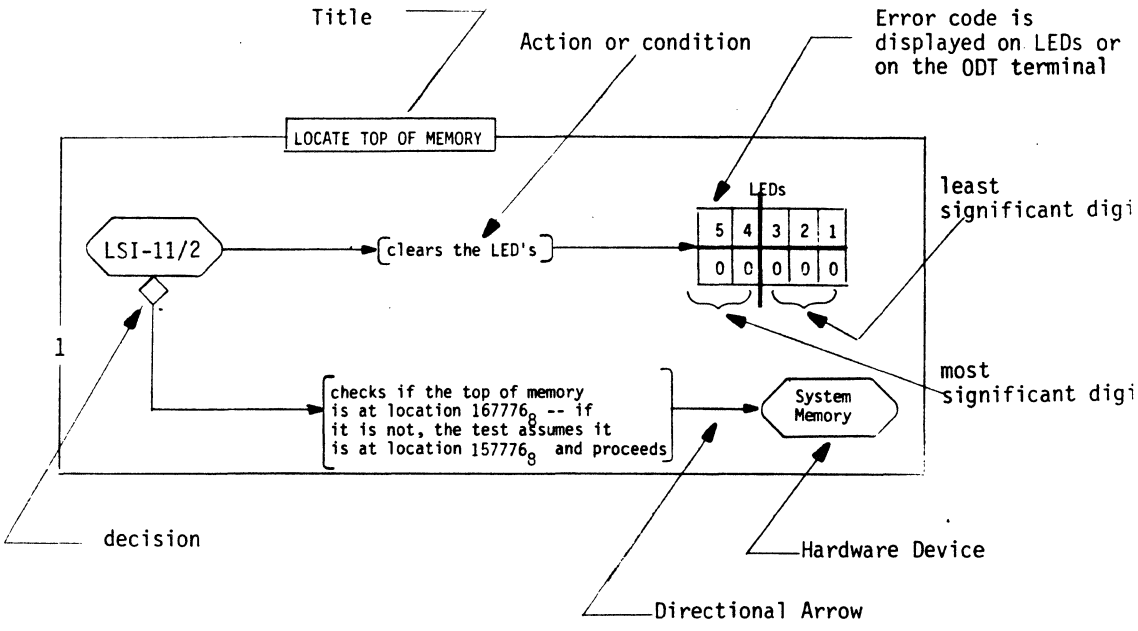


Fig. 3-2. Diagnostic diagram example.

POWER-UP TEST DESCRIPTIONS

Introduction

The 8501 Power-up Diagnostics consist of the System Memory (RAM) test, Diagnostics Memory (ROM) test, LSI-11/2 Processor (CPU) test, Line-Time Clock (LTC) test, and the Flexible Disc Controller (FDC) test. The 8501 executes these five tests in the above stated sequence. Once the sequence is started it continues until either completed or HALTed by an error. Figure 3-3 shows the power-up diagnostics sequence. As shown, the power-up diagnostics execute as follows:

a. The LSI-11/2 initializes the system and attempts to read RAM location 4. If this is not possible, the PROCESSOR BUSY light dims noticably.

b. The LSI-11/2 executes the power-up sequence starting at ROM location 2173000. When all five tests have passed, the program sets bit 5 in the LTC clock register, thus starting the bootstrap process. If a test does not pass, the LEDs remain set, identifying the failed test. If an ODT terminal is on-line the diagnostics display an error message; otherwise the test HALTs.

c. If all tests in the power-up sequence pass, the 8501 bootstrap routine searches for a bootable disc. This causes the front panel lights on the disc drives to flash briefly. If the bootstrap routine did not find a disc, the lights continue to flash every six seconds. The bootstrap routine continues to look for a disc until either a disc is inserted or the unit is turned off.

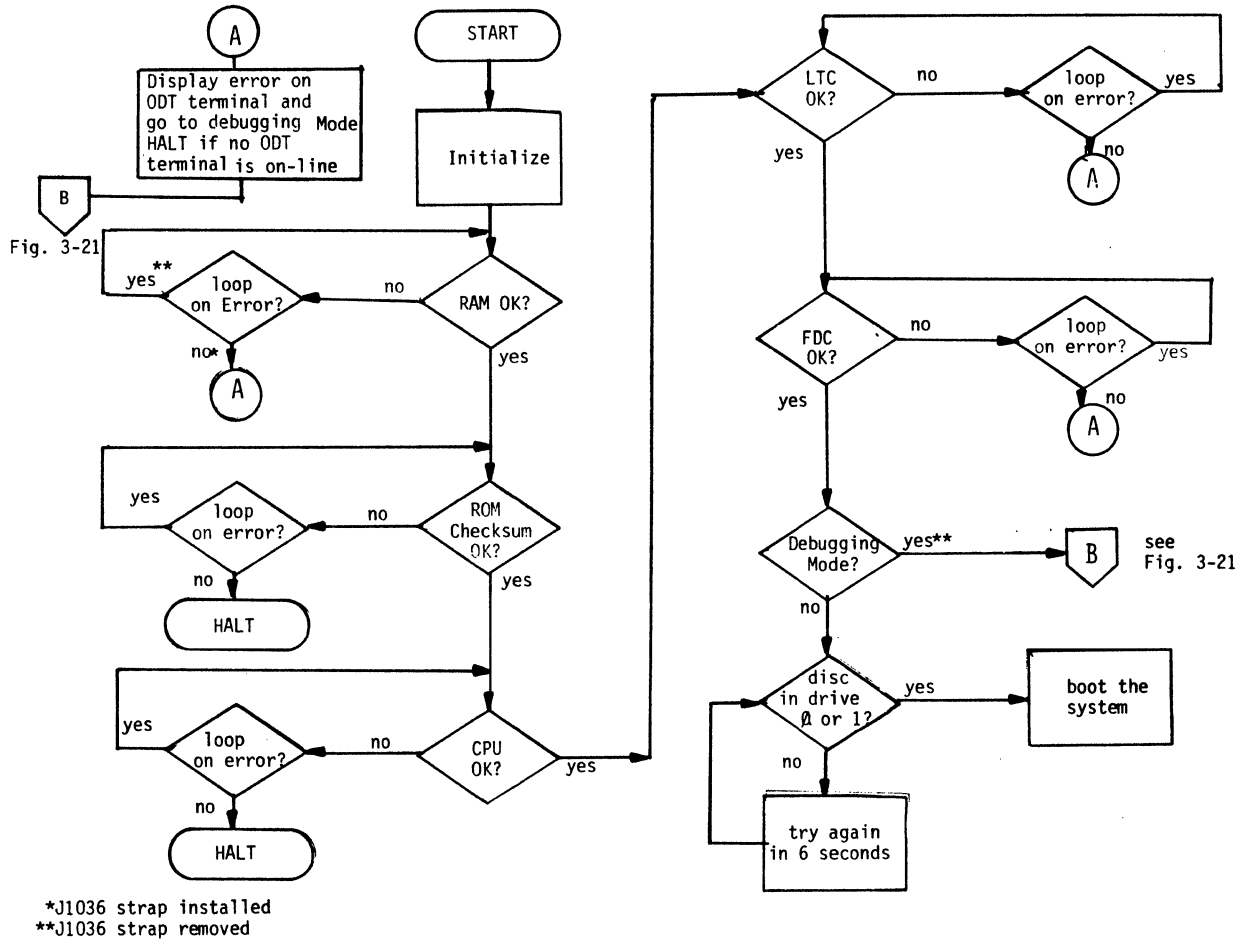


Fig. 3-3. Power-up sequence flow chart.

POWER-UP TEST NO. 1
RAM Test

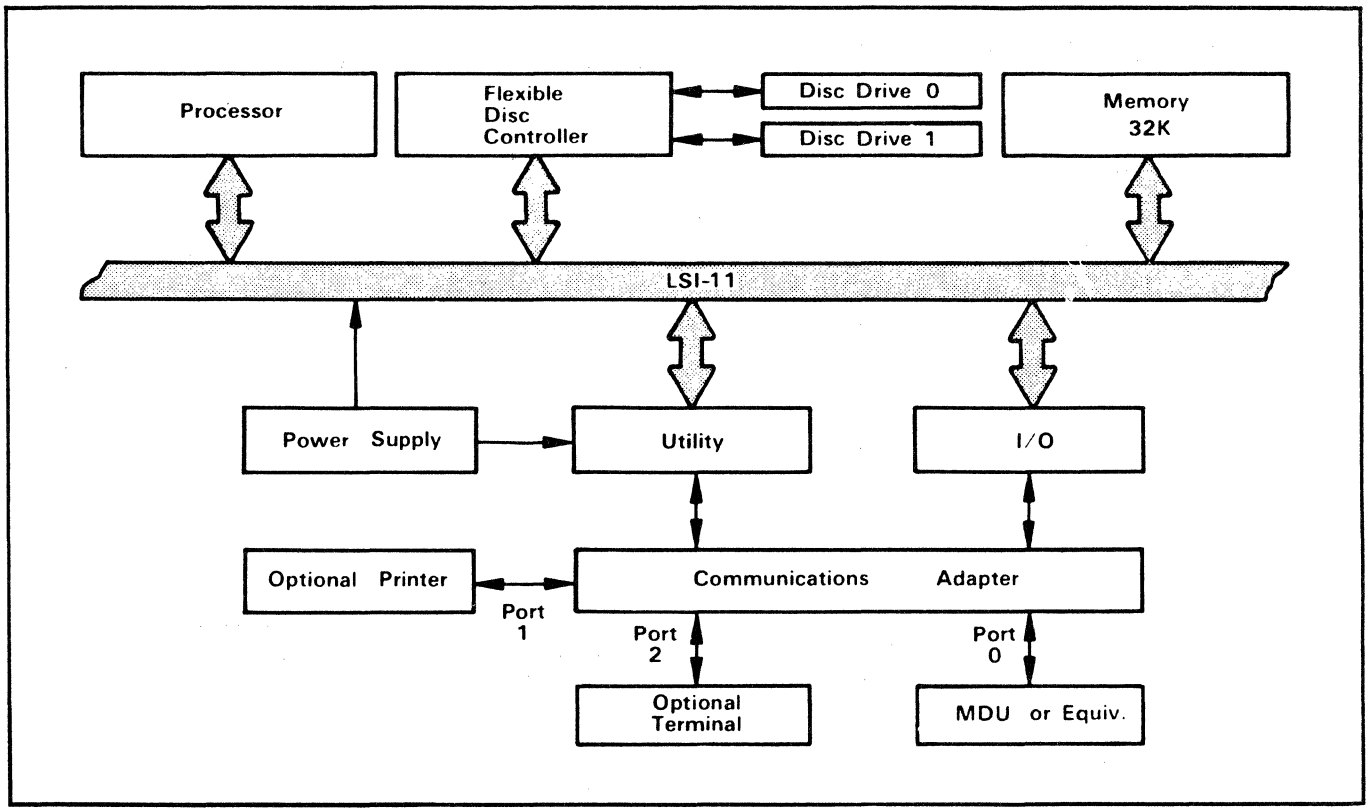


Fig. 3-4. 8501 block diagram (RAM test).

TEST NAME: RAM Test

TEST NO. 01

COMMAND: RE1

FUNCTION: To check the addressing and data storage capability of the system memory.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility Board, System Memory, ROM Memory

ERROR CODES: LED Error 00

DESCRIPTION

The RAM test consists of these four parts:

1. Locate the highest RAM address.
2. Store the address as data into every memory location.
3. Read every memory location and complement its contents.
4. Read every memory location and clear it.

This test takes approximately two seconds to execute. If the test passed, it automatically initializes the next test.

1. LOCATE TOP OF MEMORY (Fig. 3-5). The test sets the LEDs to 00 and searches for the highest memory location. Since the 8501 is shipped with 32K-words of memory, the highest memory is 167776. If the top of memory is not at location 167776, the test assumes that the unit contains only 28K-words of memory and the top of memory is at location 157776.

2. STORE ADDRESS (Fig. 3-6). The test execution continues at location 10 using its address as data and storing it in the location. The test then sequences upwards in memory through all remaining addresses, each time using the address as data and storing it in the memory location.

3. READ AND COMPLEMENT ALL ADDRESSES (Fig. 3-7). Starting with the highest address, the test reads the contents of every location, compares it to the expected data, and complements the address that it read. The test then proceeds to the next lower address, where it repeats the same sequence. This operation is repeated until all memory locations have been read, compared, and complemented. At that time, the memory pointer has returned to location 10.

4. READ AND COMPARE THE COMPLEMENTED ADDRESSES (Fig. 3-8). Starting again at location 10, the test sequences upward through memory one more time. This time it reads all complemented addresses and clears them.

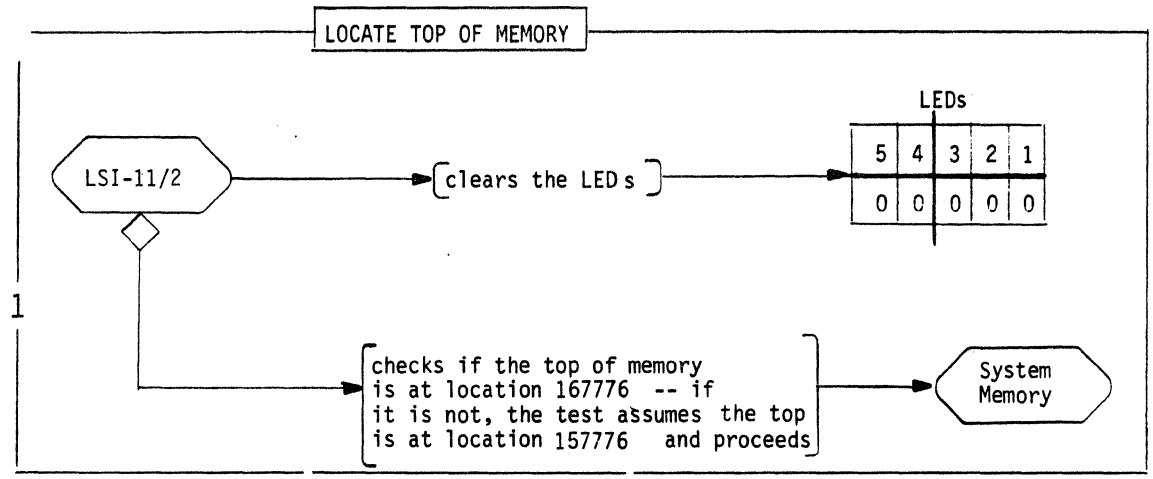


Fig. 3-5. Locate top of memory.

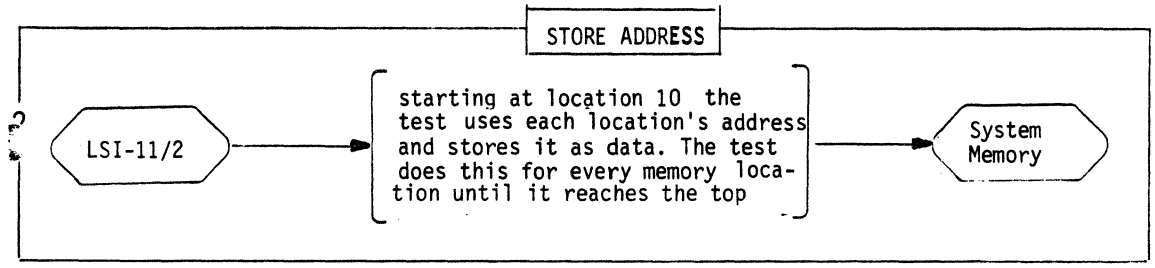


Fig. 3-6. Store address.

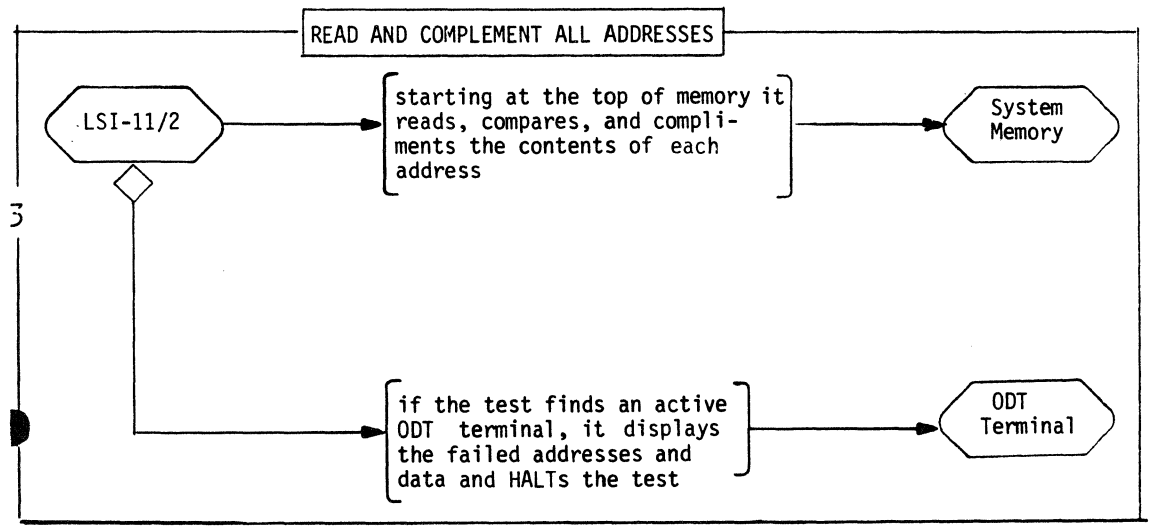


Fig. 3-7. Read and complement all addresses.

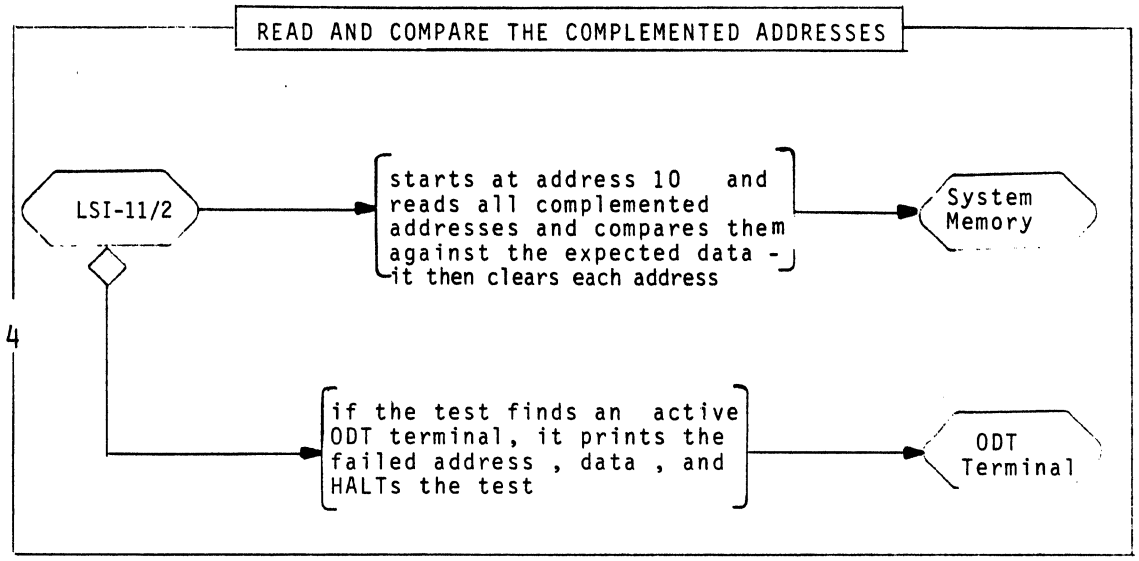


Fig. 3-8. Read and compare the complemented addresses.

POWER-UP TEST NO. 2
ROM Test

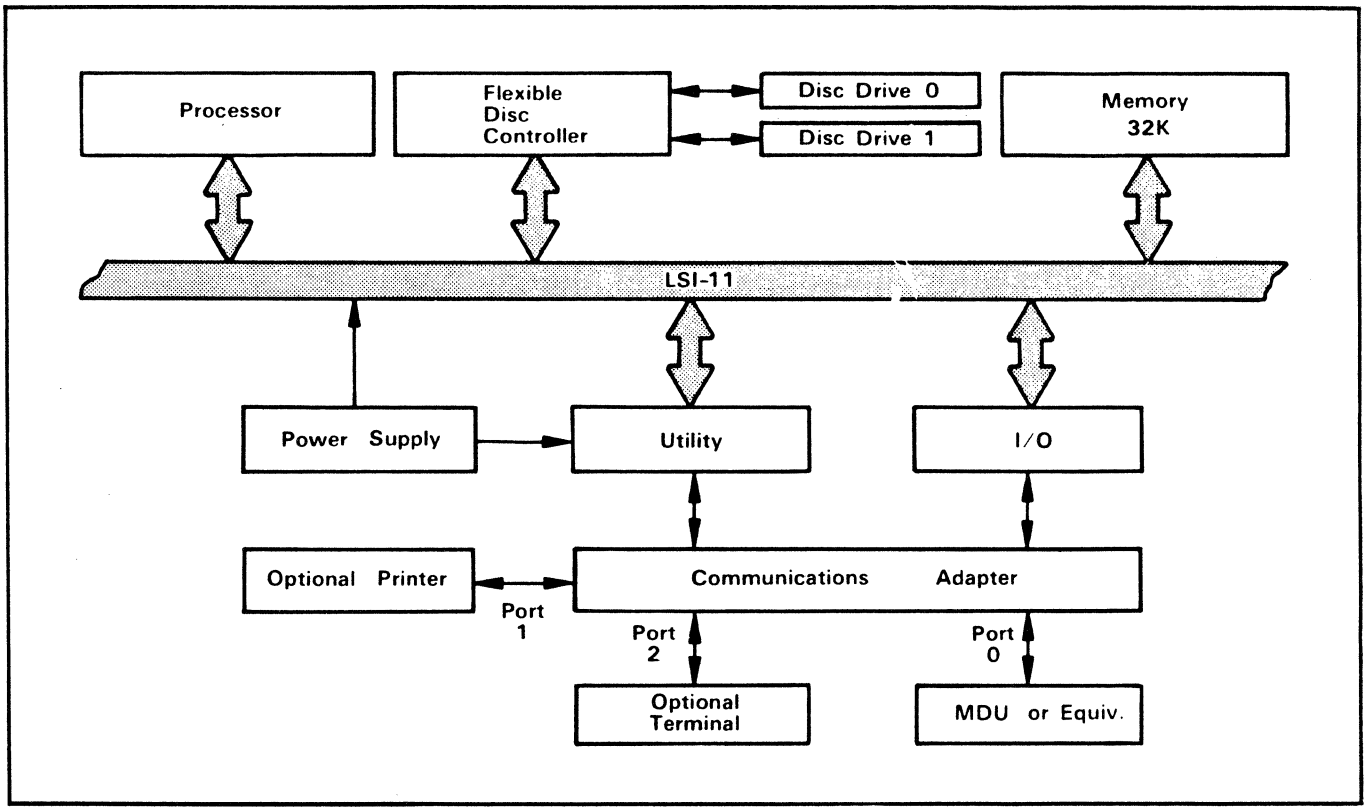


Fig. 3-9. 8501 block diagram (ROM test).

TEST NAME:	ROM Test
TEST NO.	02
COMMMAND:	RE2
FUNCTION:	To perform a checksum test on the two 8501 ROM memory devices.
BLOCKS INVOLVED:	LSI-11/2 Processor, Utility Board, System Memory, ROM Memory

DESCRIPTION

The ROM test is the second test in the verification sequence performed by the LSI-11/2 during power-up or RESTART. It performs checksum test on the two ROM memory devices located on the Utility board.The 8501 contains two 1K-byte ROMs, one for the low byte and one for the high byte. Figure 3-10 shows the program distribution within the two ROMs. As shown, bank 0 of each ROM contains the diagnostic programs and bank 1 contains the bootstrap routine.

This test checks one ROM at a time. The test starts with the low-byte ROM, checking first bank 0 and then bank 1. It continues in the same order for the high- byte ROM. Each ROM contains its part of the checksum test. The ROM test moves the test routine into system memory and executes it from there.

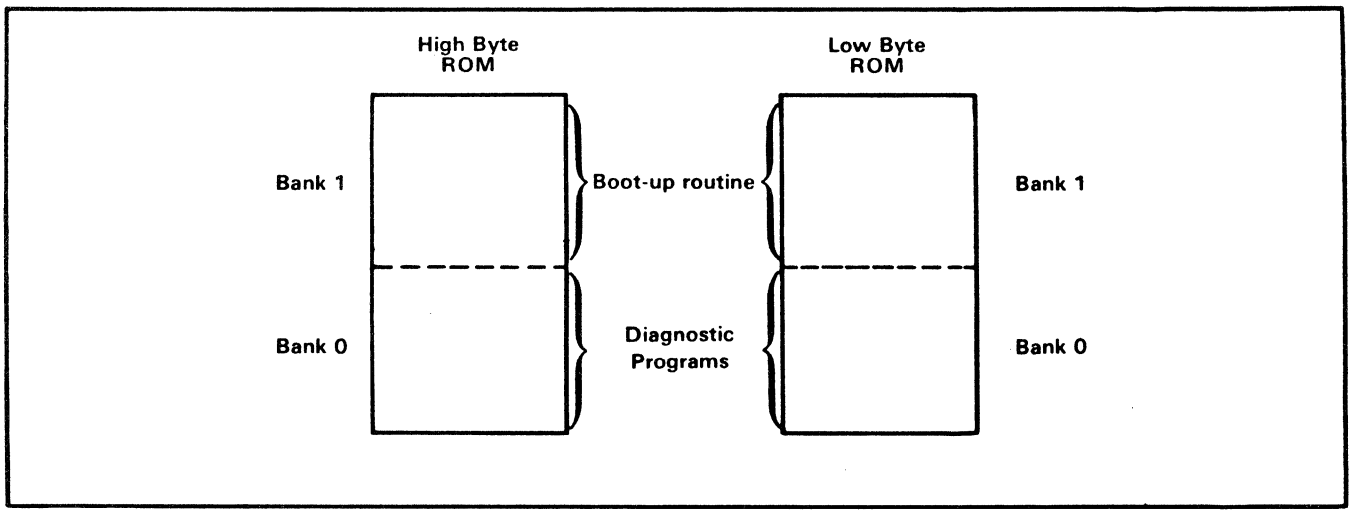


Fig. 3-10. ROM program distribution.

1. CHECK THE LOW BYTE (Fig. 3-11). The test sets the LEDs to 01 and moves the low-byte checksum test into system memory.

2. EXECUTE LOW BYTE TEST. The ROM test executes the previously stored checksum test, calculates the checksum, and compares it against the checksum stored in the ROM. If the two don't match, the program HALTS the LSI-11/2.

3. CHECK THE HIGH BYTE (Fig. 3-12). The test sets the LEDs to 02 and moves the ROM checksum test into system memory.

4. EXECUTE HIGH BYTE TEST. The ROM test executes the previously stored checksum test, calculates the checksum, and compares it against the checksum stored in the ROM. If the two don't match the program HALTs the processor.

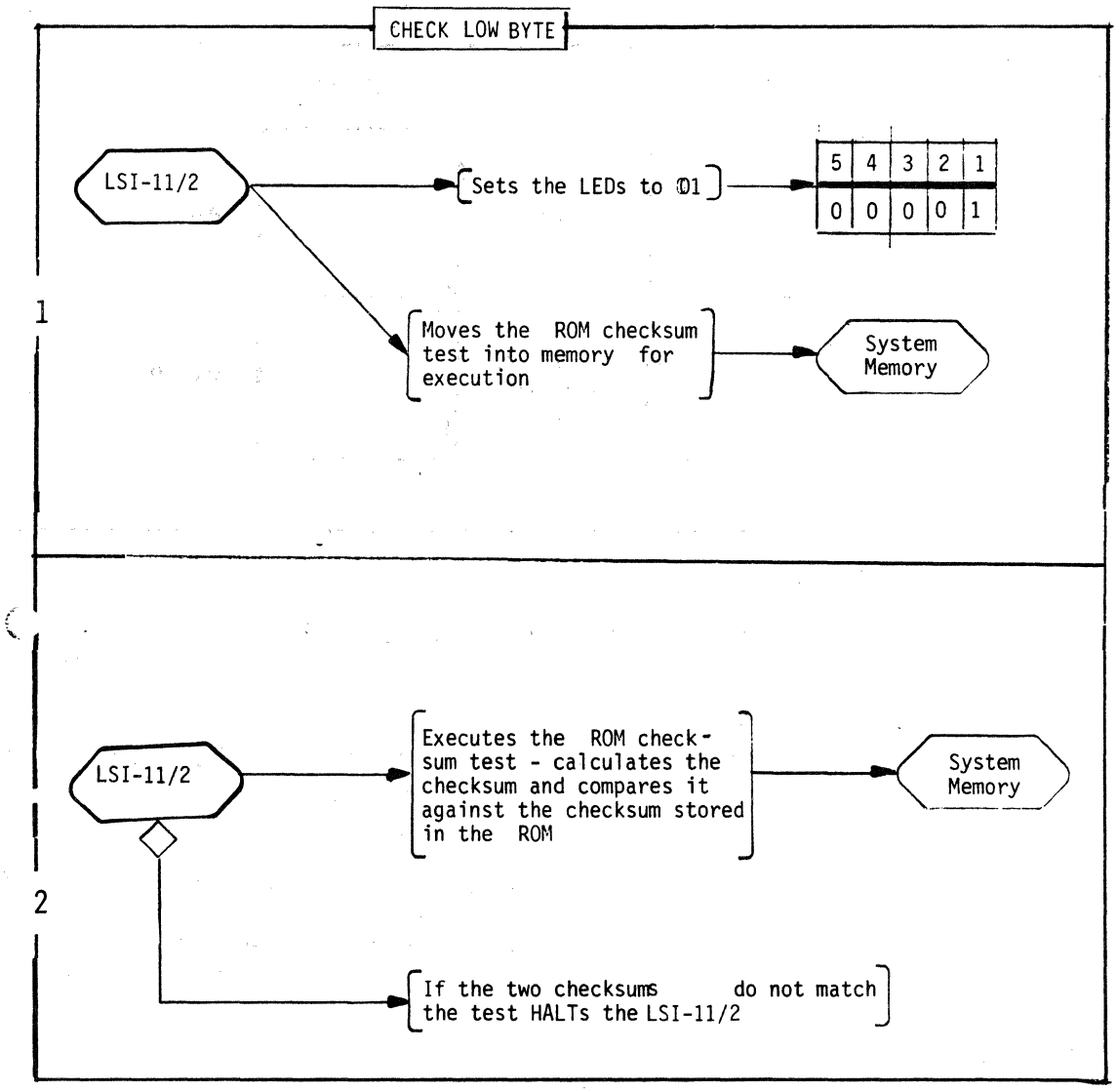


Fig. 3-11. Check low byte.

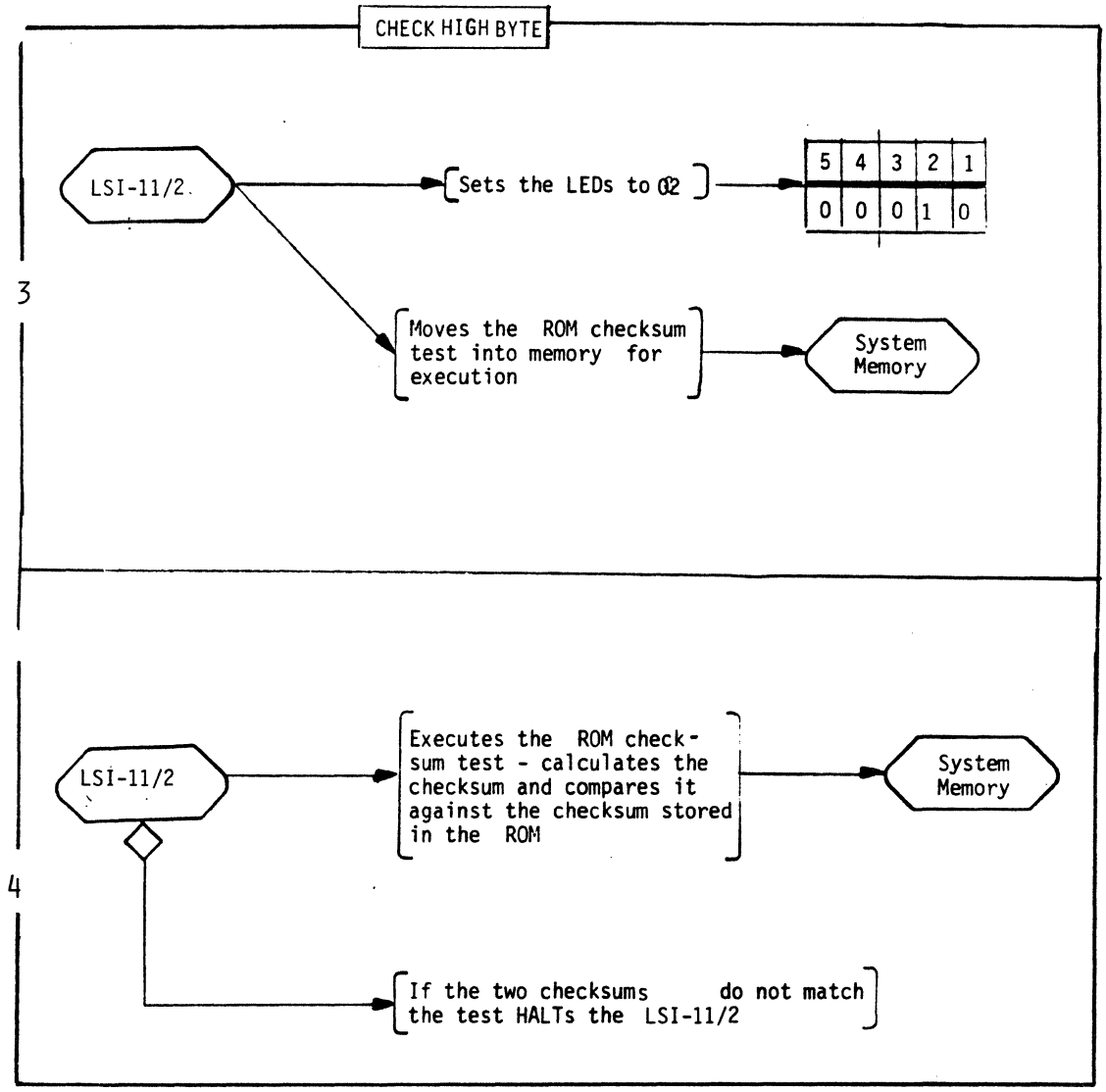


Fig. 3-12. Check high byte.

POWER-UP TEST NO. 3
CPU Status Test

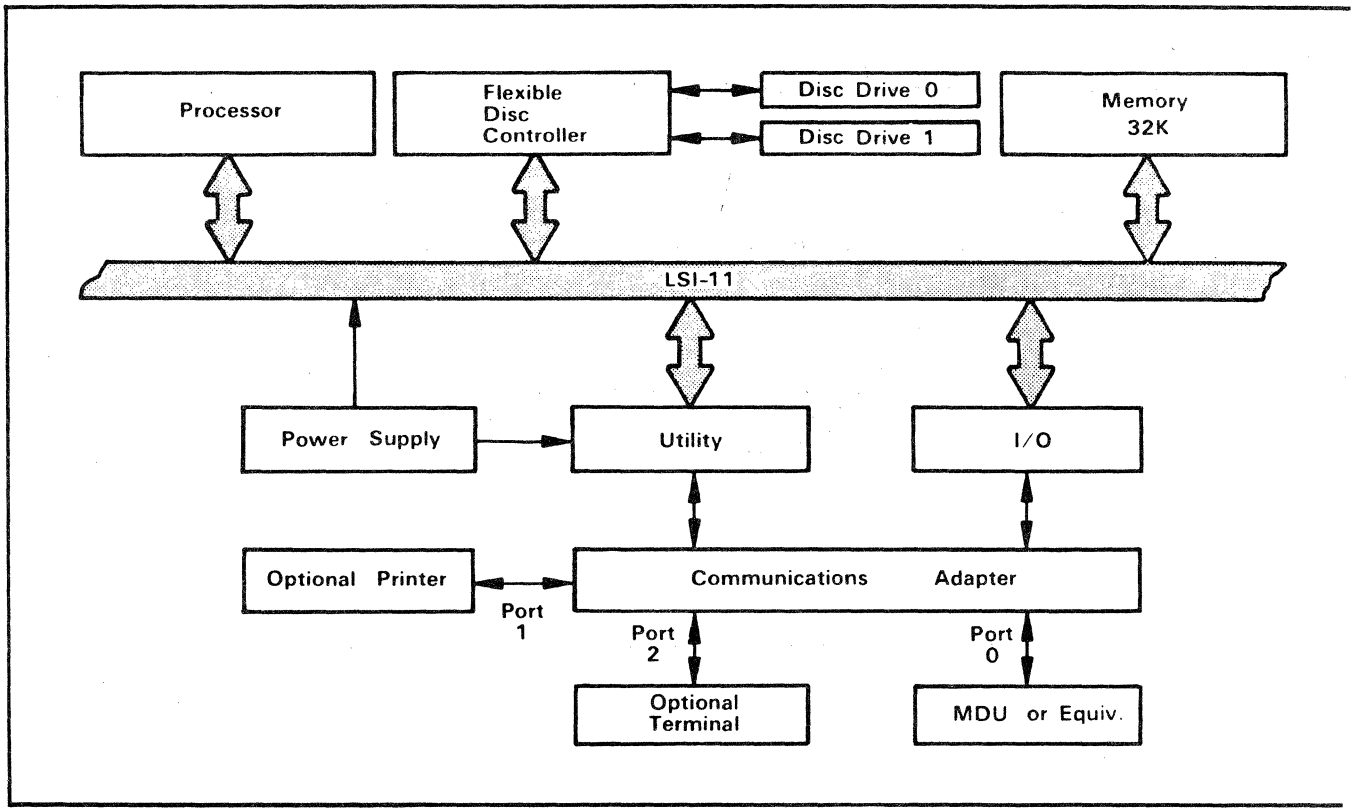


Fig. 3-13. 8501 block diagram (CPU test).

TEST NAME: CPU Status Test

TEST NO: 03

COMMAND: RE3

FUNCTION: To execute a representative LSI-11/2 instruction set which indicates whether the CPU is operational.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility Board, System Memory, ROM Memory

ERROR CODES: LED Error 03

DESCRIPTION

The CPU test is the third test in a verification sequence performed by the LSI-11/2 during a system power-up or RESTART. This test executes a representative set of LSI-11/2 instructions. Although it does not check all combinations of LSI-11/2 instructions, the CPU test checks a representative sample to determine proper operation of the CPU.

1. CPU TEST (Fig. 3-14). The test first sets the LEDs to 03, then fetches one instruction at a time from the read-only memory (ROM) and executes it. The test executes the simpler instructions first and then proceeds to more complex instructions. The CPU test verifies most LSI-11/2 operations by checking:

- o all single operand instructions;
- o all source modes for double operand instructions with destination mode 0;
- o all double operand instructions with destination mode 0, and source modes 1,2, and 3;
- o TST and TSTB instructions with all destination modes;
- o condition code operators;
- o word instructions with all destination modes; and
- o JSI and JSR instructions.

The CPU test checks the results of the executed instructions and HALTs the LSI-11/2 if any result is not correct.

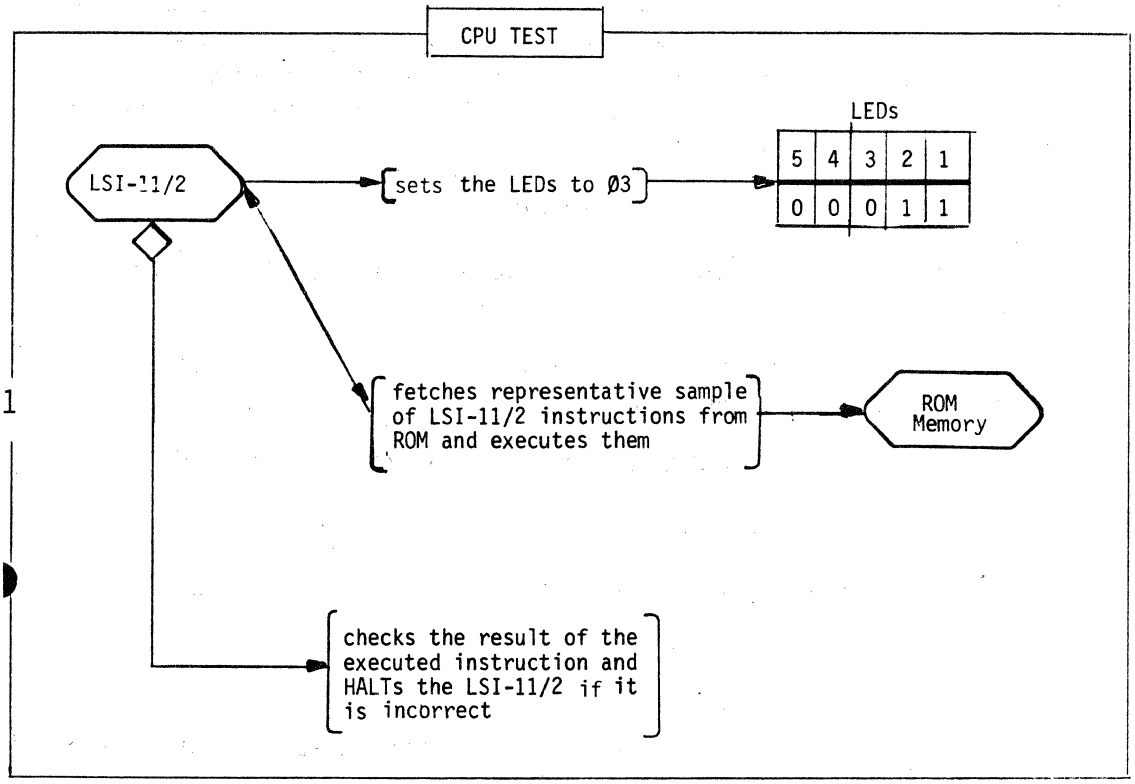


Fig. 3-14. CPU Test.

POWER-UP TEST NO. 4
Line-Time Clock Test

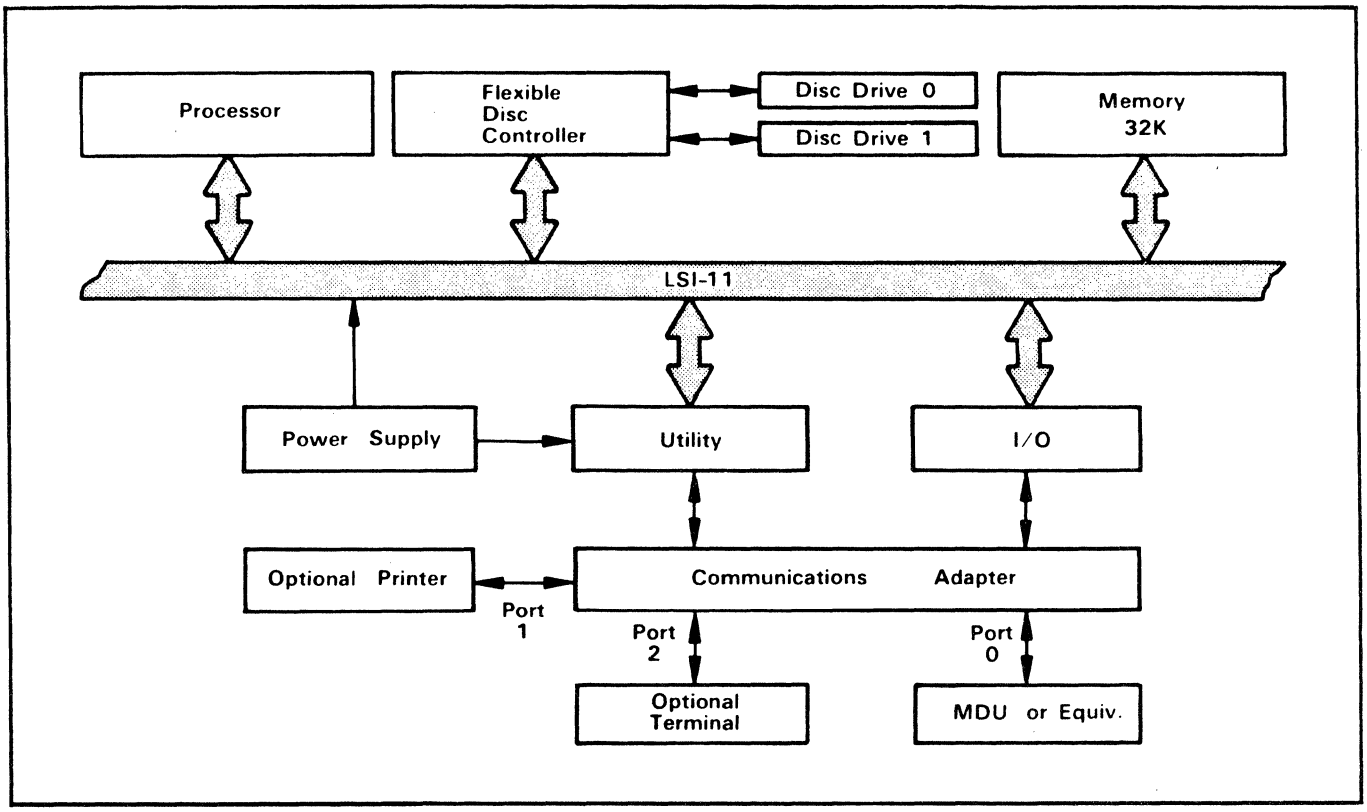


Fig. 3-15. 8501 block diagram (LTC test).

TEST NAME:	Line-Time-Clock (LTC) Test
TEST NO:	04
COMMAND:	RE4
FUNCTION:	To verify that the Line-Time Clock interrupts the LSI-11/2 at the correct rate.
BLOCKS INVOLVED:	LSI-11/2 Processor, Utility Board, System Memory, ROM Memory
ERROR CODES:	LED Error 04

DESCRIPTION

The LTC test checks that the line-time-clock interrupts occur at the proper intervals. This test is the fourth in the verification sequence that is performed by the LSI-11/2 during power-up or RESTART.

1. LTC TEST (Fig. 3-16). The LTC test starts by setting the LEDs to 04 and enabling the interrupts. The test then detects the first interrupt, fetches a series of intructions with known execution times from the system memory, and executes them (see Fig. 3-17). When the second interrupt arrives all instructions should have been executed. If the second interrupt is either too late or too early, the test HALTs the LSI-11/2 and the LEDs remain set at 04. If the test finds an active ODT terminal, it also displays the message "LTC".

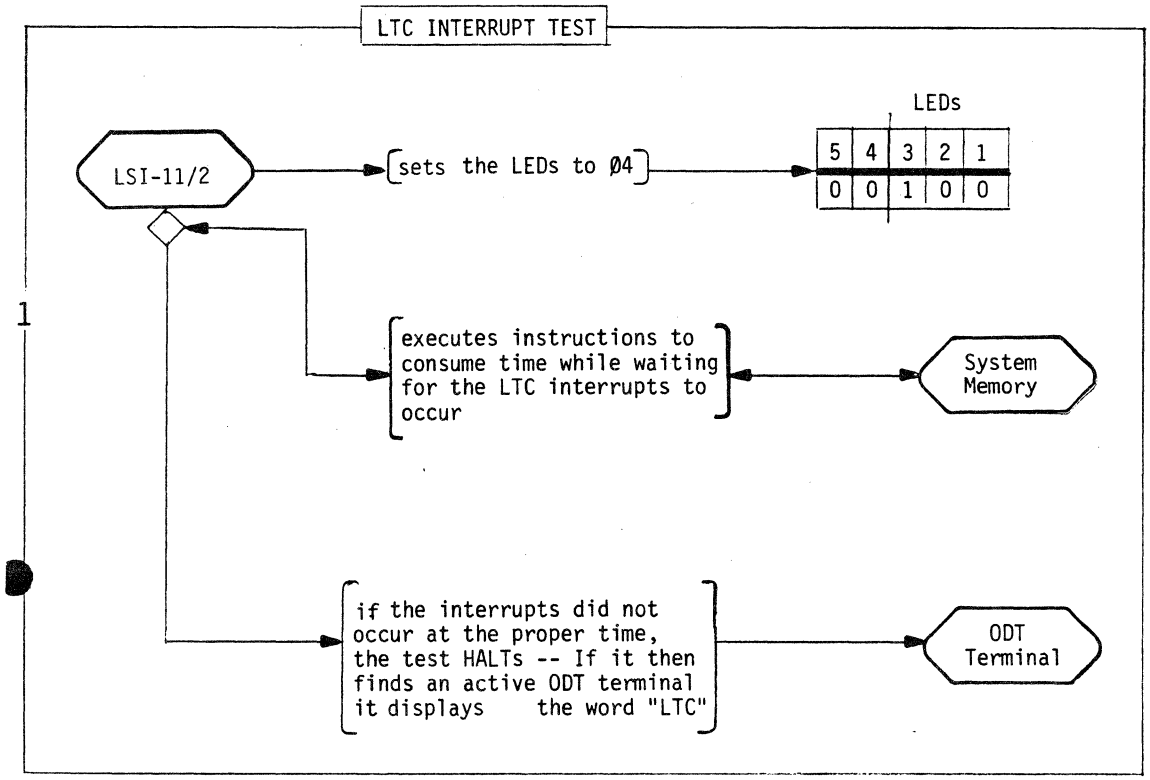


Fig. 3-16. The LTC test.

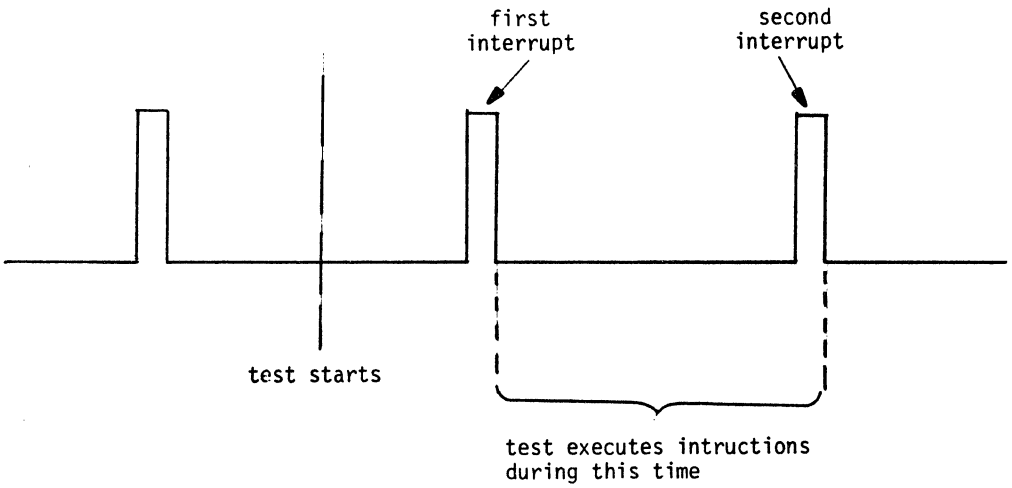


Fig. 3-17. LTC test interrupts.

POWER-UP TEST NO. 5
Flexible Disc Controller Test

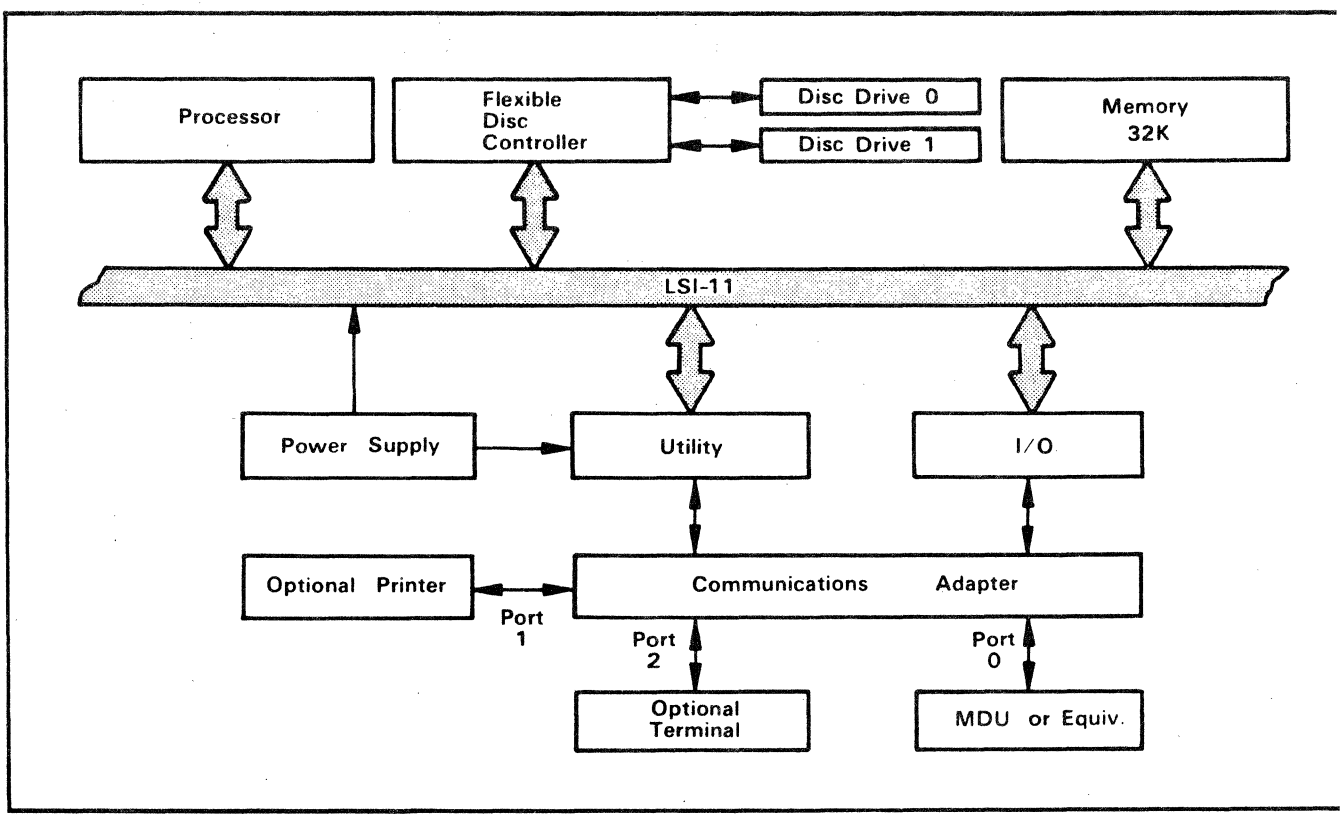


Fig. 3-18. 8501 block diagram (FDC test).

TEST NAME:	Flexible Disc Controller (FDC) Test
TEST NO:	05
COMMAND:	RE5
FUNCTION:	To check if the Flexible Disc Controller board is operational.
BLOCKS INVOLVED:	LSI-11/2 Processor, Utility Board, System Memory, Flexible Disc Drives, FDC Board, ROM Memory
ERROR CODES:	LED Error 05, LED ERROR 06, LED ERROR 07

DESCRIPTION

The FDC test is the fifth and last in the verification sequence executed by the LSI-11/2 processor during power-up or RESTART. This test does not check the disc units, only the Disc Controller board.

The FDC test consists of two parts: the WRITE/COMPLEMENT test and the STATUS REGISTER test. Figures 3-19 and 3-20 show the basic test operations. If the FDC test fails at any time, LSI-11/2 processor searches for an active ODT terminal and displays the contents of these registers:

Flexible Disc Controller Buffer Pointer Register (FDCBPR)
Flexible Disc Command Register (FDCR)
Flexible Disc Word Count Register (FDWCR)
Flexible Disc Address Register (FDAR)
Flexible Disc Memory Address register (FDMAR)
Flexible Disc Error Register (FDER)
Flexible Disc Status Register (FDSR)
Flexible Disc Diagnostic Register (FDDR)

When the test finds an error, the buffer pointer register should contain 1000 and the command register 160053. The contents of the other registers vary depending on whether the drive contains a disc, and if so, the type of disc.

1. WRITE/COMPLEMENT (Fig. 3-19). The test sets the LEDs to 05 and checks whether the Flexible Disc Controller board is powered up. Next the controller writes a value into the Flexible Disc Controller buffer pointer register (FDCBPR). The stored value is then complemented and read back, thus verifying that the board is operational. If the LSI-11/2 processor cannot access the FDCBPR, the test assumes that the board is not operational. The test then searches for an active ODT terminal and displays the contents of the flexible disc registers. If the test can not find an ODT terminal it HALTs the LSI-11/2 processor.

2. STATUS REGISTER TEST (Fig. 3-20). The test sets the LEDs to 06, sends a STATUS REQUEST command to the FDC board and asks for the status. The test then waits for the correct interrupt response. If it did not receive the proper response, it HALTs the test, searches for an active ODT terminal, and it displays the contents of the flexible disc controller registers. If the test did receive the proper interrupt response, it continues and sets the LEDs to 07. The processor then receives the STATUS DATA from system memory, examines it, and disables the interrupts. If the test did not get the status result, it HALTs the test and displays the Flexible Disc Controller registers. If the test passed, the power-up sequence sets the LEDs to 12 and then attempts to boot the operating system.

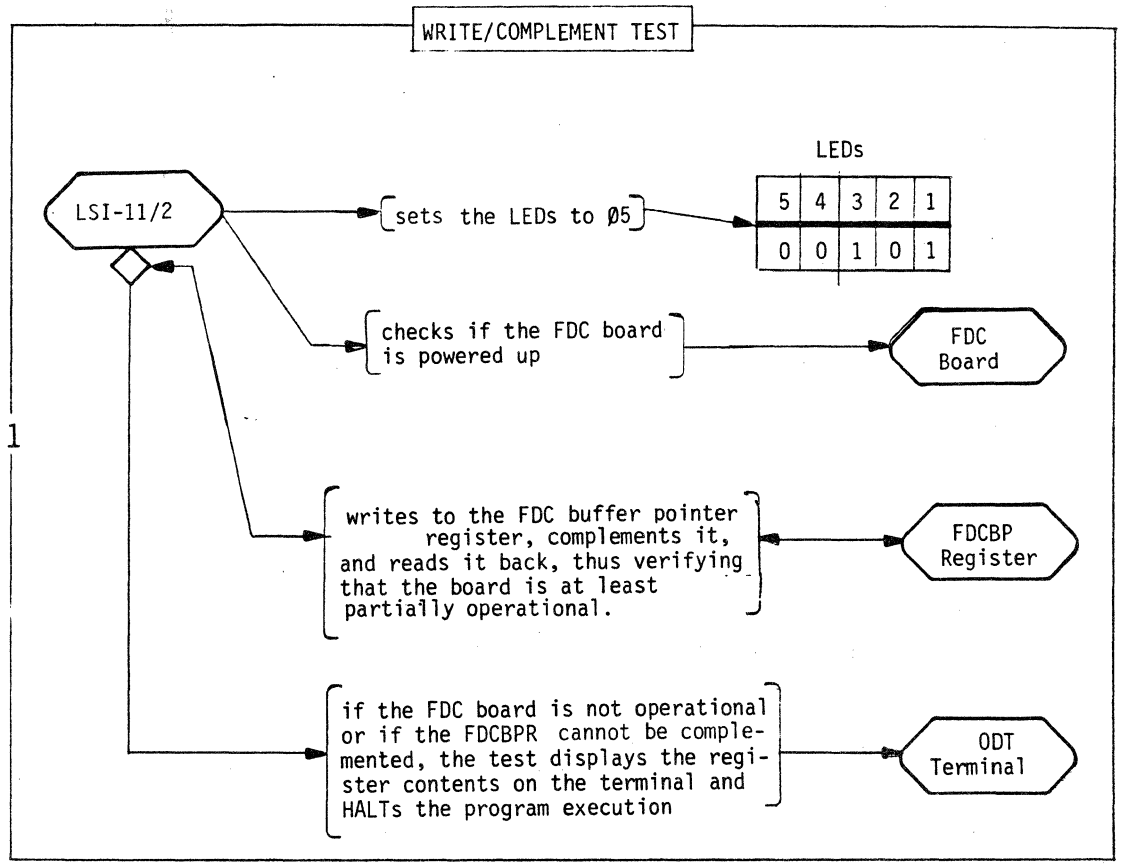


Fig. 3-19. Write/complement test.

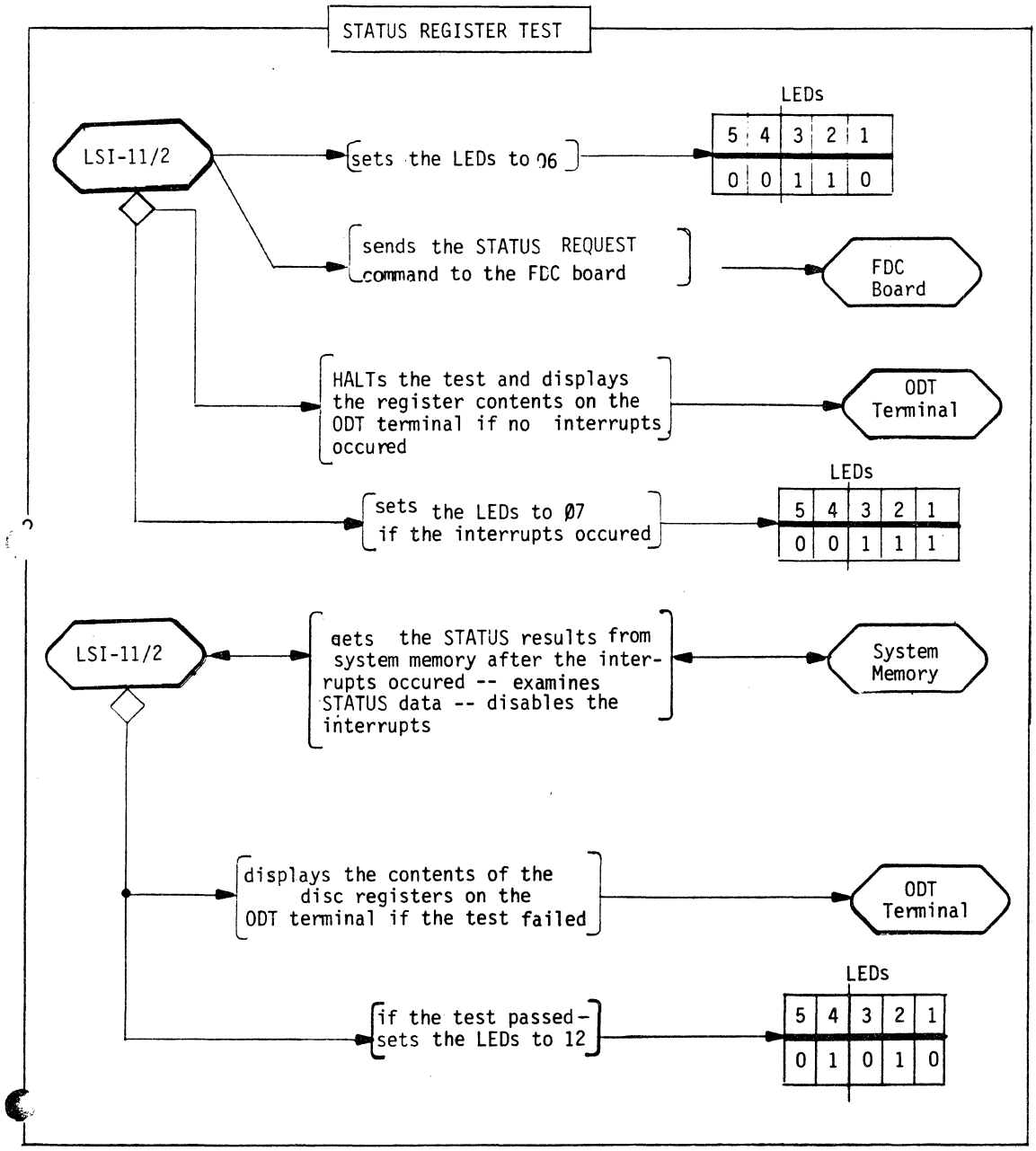


Fig. 3-20. Status register test.

THE DEBUGGING MODE

Introduction

The Debugging Mode is a firmware program that follows a predetermined operating sequence, unless interrupted by a valid Debugging Mode command. Valid commands are: REn,VEn, HSn, ALn, FDn, and RS. Figure 3-21 shows the Debugging Mode program flow.

The Debugging Mode aids in troubleshooting minor system failures prior to system boot-up. The Debugging Mode requires that a terminal is connected directly to port 2 of the 8501. The Debugging Mode lets you:

- o read the error data from the LEDs;
- o repeat any power-up test;
- o boot the system manually rather than automatically;
- o download load files via a RS-232-C port for execution in the 8501;
- o check the disc alignment with the ALn routine and an alignment disc;
- o verify the HSI channel; and
- o verify the disc tracks and sectors.

Entering the Debugging Mode

The maintenance jumper (J1036 on the Utility Board) controls the access to the Debugging Mode. You can enter the Debugging Mode under the following conditions:

- o If all automatic tests pass and the maintenance jumper is not installed, the firmware automatically selects the Debugging Mode.
- o If any test fails and the maintenance jumper is installed the firmware automatically selects the Debugging Mode.
- o You can also enter the Debugging Mode manually as described under Bypass The Power-Up Tests later in this section.

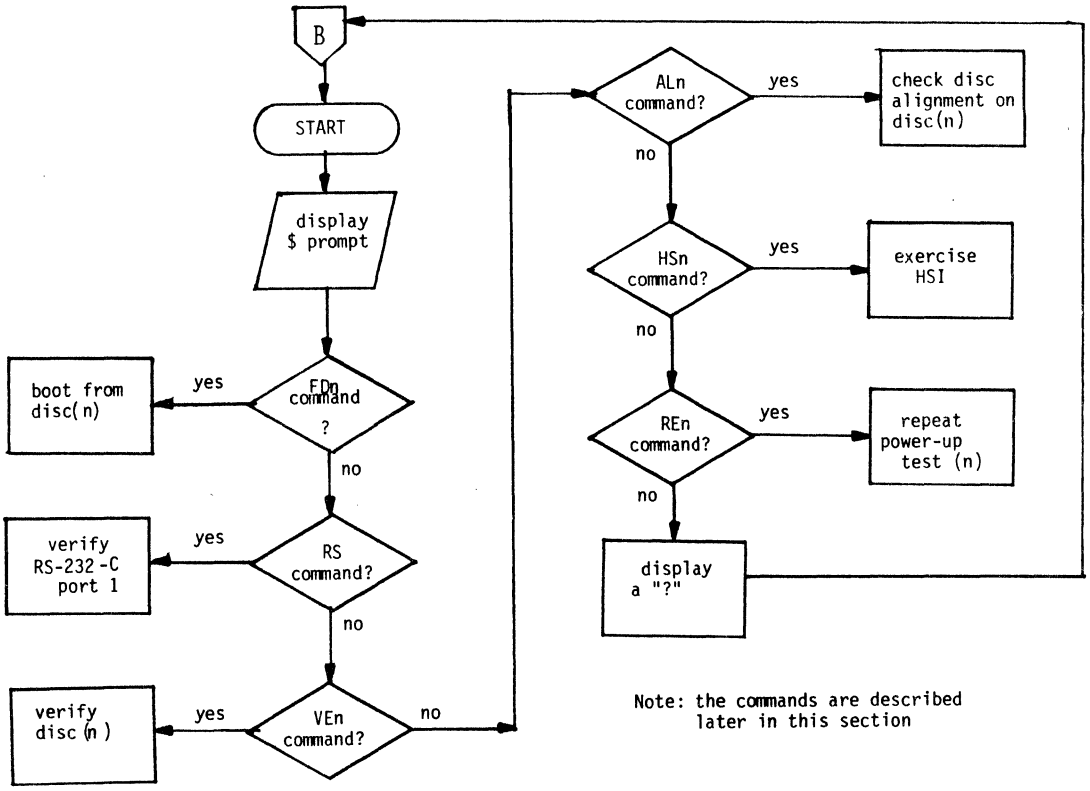


Fig. 3-21. Debugging Mode Flowchart.

The Restart (REn) Commands

The Debugging Mode gives you access to the REn commands. Thus, you can re-execute individual power-up functions or tests that normally run automatically. You can issue a REn command when the $ prompt appears on the terminal. The commands and their respective functions are as follows:

RE0 initializes the ROM diagnostic

RE1 restarts the RAM test

RE2 restarts the ROM test

RE3 restarts the CPU test

RE4 restarts the LTC test

RE5 restarts the FDC test

RE6 looks for a bootable disc

Accessories

The Debugging Mode uses two hardware accessories:

Maintenance jumper J1036 on the Utility Board
A wrap-back connector (Tektronix part no. 067-1020-00)

A wrap-back connector is a RS-232-C-type connector that is wired to feed signals output from a port back into the same port. Thus, data transmitted by the port is fed back into the same port. When you order part no. 067-1020-00, you get a male and female wrap-back connector.

To construct your own wrap-back connector, use Table 3-4 for pin-to-pin connections. Assure that the connecting wires are not shorted. When you have wired your connector, mount it in its shell.

Table 3-4
Wrap-Back Connector Connections

FROM:		TO:	
PIN	SIGNAL	PIN	SIGNAL
3	T DATA +	2	R DATA +
12	T DATA -	11	R DATA -
5	CTS +	20	DTR +
25	CTS -	13	DTR -
8	CD +	4	RTS +
6	DSR +	4	RTS +

VERIFICATION ROUTINES

The following pages describe the verification commands. Each command description contains a block diagram, description, and flow chart.

Track/Sector Verification

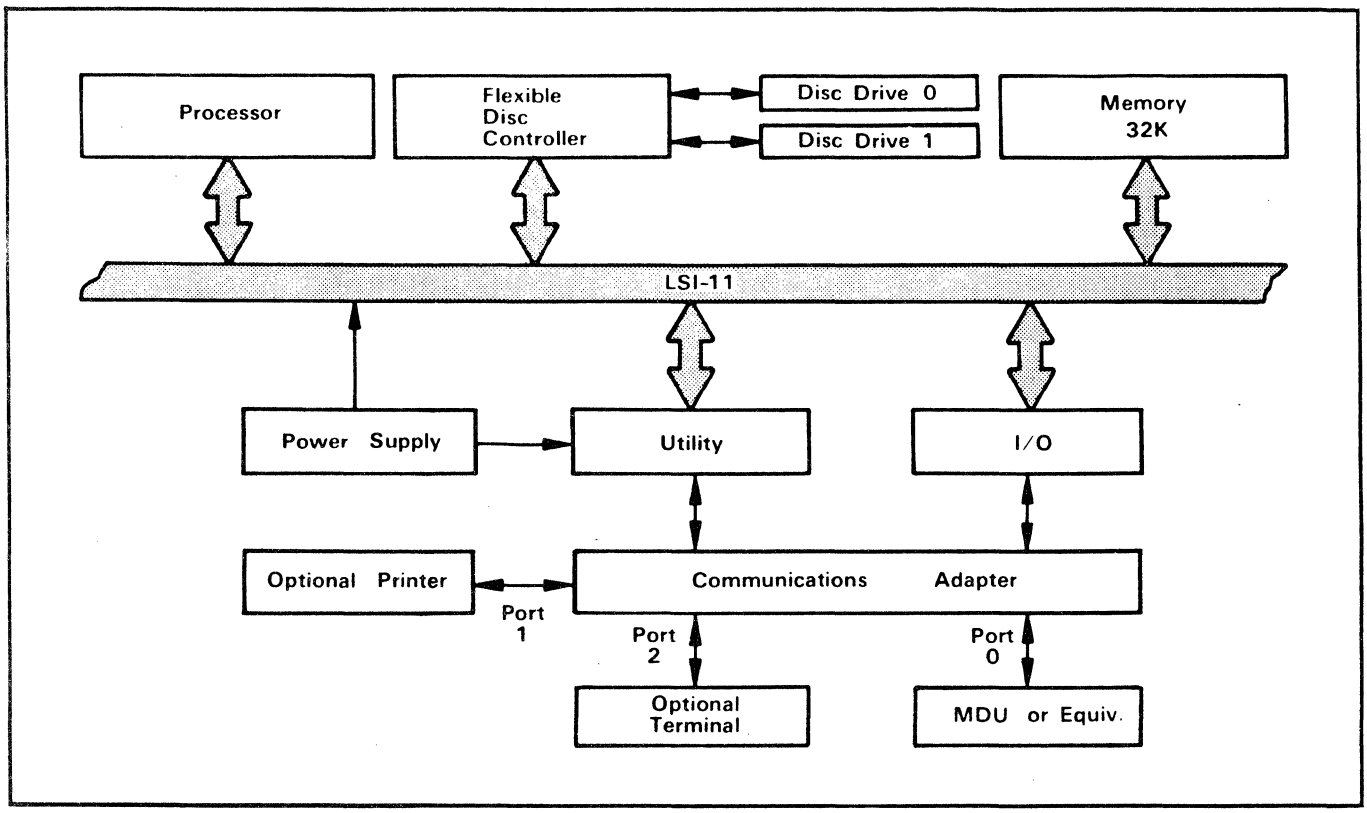


Fig. 3-22. 8501 block diagram.

TEST NAME: Track/Sector Verification

COMMAND: VEn -- (where n identifies the verified disc drive)

FUNCTION: To verify track and sector addressing of both disc sides.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility Board, Read-only Memory, Disc Drives, Flexible Disc Controller (FDC)

ERROR CODES: LED Error 13

DESCRIPTION

The Track/Sector verification routine is a use-initiated routine that verifies the track and sector addressing of the specified disc drive. The track/sector routine requires a terminal connected to the AUXILIARY port. Call the track/sector routine by typing the VE followed by the number of the drive to be verified to the $ prompt.

1. TRACK/SECTOR TEST (Fig. 3-23). The test starts by setting the LEDs to 13 and sending instructions to the Flexible Disc Controller (FDC) board to verify the specified disc.

2. READ DATA. The test responds by reading all data on all tracks on the specified disc and then comparing the resulting checksum against the checksum residing on the disc.

3. DISPLAY FDC. When the verification process is completed, the test displays the contents of the FDC interface registers on the terminal. If the FDC board is inoperative, the test waits for two minutes and then displays the unchanged disc registers. Table 3-5 lists the register contents under the two conditions.

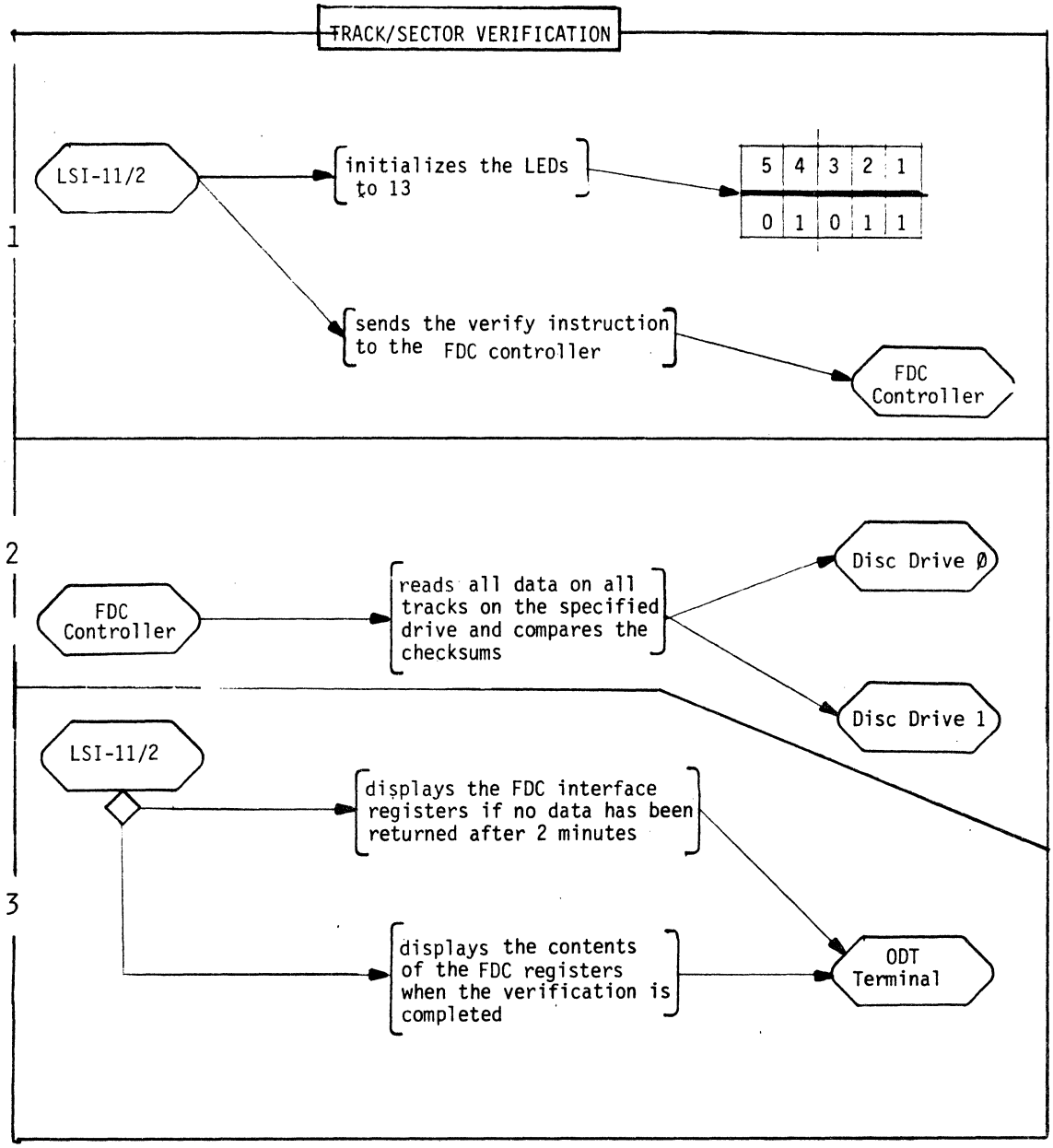


Fig. 3-23. Track/Sector verification.

Table 3-5
FDC Interface Registers

Register Name	Mnemonic	Pass*	Comment
FDC buffer pointer	FDCBPR	001 000	
command	FDCR	120 045	
word count	FDWCR	177 777	If the most significant bit is cleared, the program waited for two minutes and then aborted.
disc address	FDAR	007 627	If the test failed,the register contains the record number of the failed disc.
error	FDER	000 000	If bit 3 or 4 is set, read/seek errors occured.If bit 0 is set the LSI-11/2 did not find a disc
memory address	FDMAR	000 000	
status	FDSR	054 015	
diagnostic	FDDR	005 036 or 005 046	the register contents shown is for drive 0 -- for drive 1 the register contains 005 046

*NOTE: For a fail condition, the registers could contain any value.

High-Speed Interface Verification

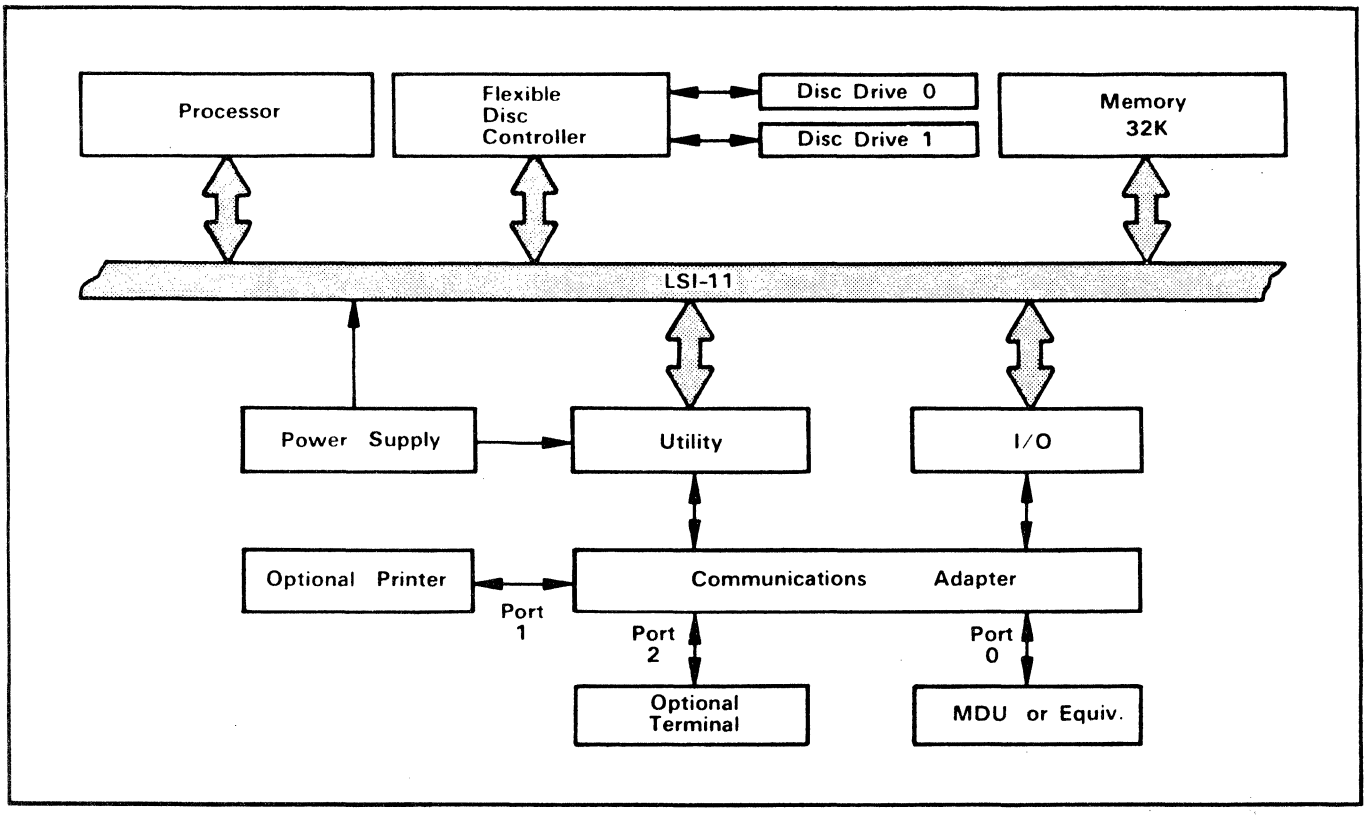


Fig. 3-24. 8501 block diagram.

TEST NAME: High Speed Interface ((HSI) Verification

COMMAND: HSn (where n is an octal number between 0 and 377)

FUNCTION: Check the DMA transmit and receive logic for proper operation.

BLOCKS INVOLVED: Utility Board, LSI-11/2 Processor, Read-Only Memory, I/O Board, Communications Adapter board

ERROR CODES: LED Error 13

DESCRIPTION

The HSI verification routine verifies the operation of the high speed interface port. You start the HSI verification by typing HS and an octal number between 0 and 377 to the $ prompt. The number is stored in the memory buffer, output to the HSI port, and then read back. This routine requires that you either install a wrap-back connector, or connect the HSI port to a Data Communications Tester such as the TEKTRONIX 832.

1. SET LEDS TO 13 (Fig. 3-25). The test starts by setting the LEDs to 13. It then continues and fills the 30 K-byte memory buffer with the specified octal number.

2. TRANSMIT NUMBERS. The LSI-11/2 sends a transmit instruction to the HSI controller to transmit all numbers from the memory buffer to the HSI port.

3. READ NUMBERS. If the HSI port is connected to either a wrap-back connector or data communications tester, the LSI-11/2 reads the data input from the HSI port and sets the LEDs. This routine uses the complement of the five most significant bits of the output number as a data indicator and ignores the lower three bits. For example: if the specified octal number is 355, the complement of 355 is 10. Thus the LED display looks like this ---*-. Only one LED is on and the others are off. The test also displays the HSI registers after the test is completed (see Table 3-6).

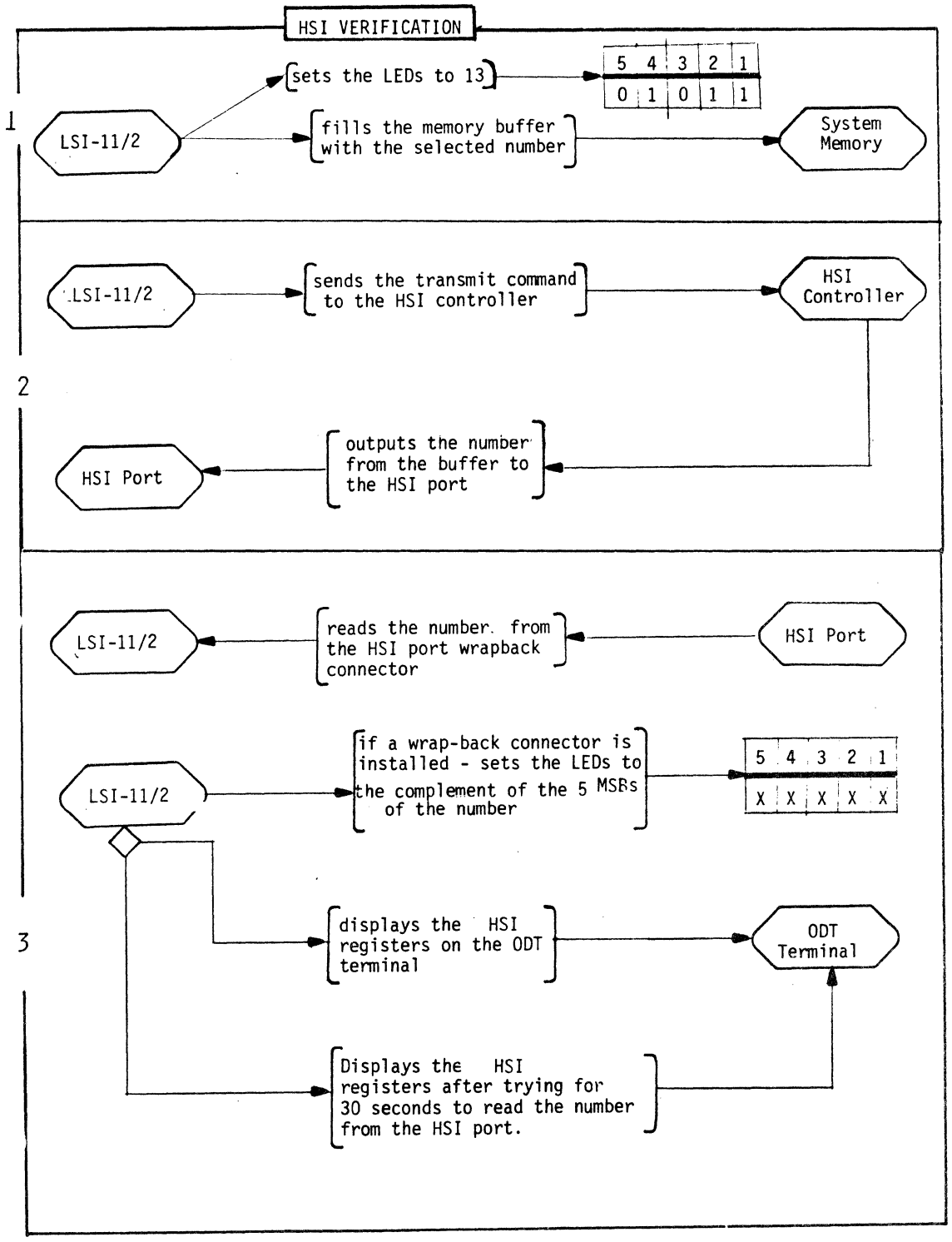


Fig. 3-25. The HSI test.

Table 3-6
High Speed Interface Registers

Register Name	Mnemonic	Pass	Fail	Comments
DMA	DMAR	000 026	000 007	A set most-significant bit usually indicates that the DMA did not finish testing within 30 seconds. This could be caused by a too low baud rate or an open HSI port.
Counter	CTR	000 000	XXX XXX	The DMA did not finish the test thus it did not decrement the counter to zero.
Address	ADDR	077 700	lower number	If the number is lower the DMA did not finish the test
Interrupt Vector	VECR	000 374	non-zero	
Receive Status	RCSR	000 000	non-zero	
Receive Buffer	RBUF	000 XXX	100 XXX	X is the number specified for HSn -- if the most-significant bit is set, a timing error occurred.
Transmit Status	XCSR	000 200	000 000	All zeros indicate an open HSI port.
Transmit Buffer	XBUFR	000 000	non-zero	A failure could indicate a hardware problem.

UTILITY ROUTINES

The Debugging Mode lets you access three utility routines that perform additional verification and system boot-up from a flexable disc. The three utility routines and their functions are:

Name	Function
ALn	verifies the disc drive head alignment with an alignment disc.
FDn	boots the system from the specified disc
RS	verifies the operation of the RS-232-C port 1

ALn The disc drive head alignment routine checks the heads for proper

alignment. Checking the head alignment requires an alignment disc (Tektronix part number 119-1354-00). The ALn routine does, however, execute with an empty drive and allows you to check if the heads are moving.

To enter the routine, type AL follwed by the number of the disc drive to be verified. The ALn routine executes in about one minute. It starts by moving the heads to the innermost track and then back out to track 40.The test then performs a perpetual read on track 40 (side 0). Stop reading by entering any RE command. After the disc alignment routine is executed, the flexible disc registers are displayed on the terminal in the following format:

FDCBPR	FDCR	FDWCR	FDAR	FDDMA	FDER	FDSR	FDDR
XXXXXX	XXXXXX	XXXXXXX	XXXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

FDn This routine allows you to boot the 8501 from a disc if the automatic boot routine did not work because of a system error. n specifies the disc drive and accepts either a 0 or a 1. For example, if you had a FILE ERROR the system could not boot automatically. To boot from the disc, type FD0 (for disc 0) and a RETURN The firmware then loads the contents of block record 0 (256 words) into program memory starting at location 0. Next, it looks for a NOP instruction at location 0 and if it finds one the firmware excutes a JSR instruction.

RS This routine is checks the operation of the RS-232-C PRINTER port. If a wrap-back connector is attached to the PRINTER port, data entered on the ODT terminal exits to the PRINTER port, returns, and is displayed on the ODT terminal. You can than compare the written and returned data and determine if the port operates properly. To call the RS routine type RS followed by a RETURN. To exit from the RS mode type a CTRL @ (hold down the control key and type an @ sign).

TROUBLESHOOTING IN ODT MODE

Description

The Octal Debugging Technique (ODT) is a built-in feature of the LSI-11/2. ODT allows you to examine and change register contents and memory locations. ODT also permits single-stepping and restarting of a user program. ODT works through the ODT terminal and responds to single character commands and octal numbers. Table 3-7 shows a summary of ODT commands. For additional information refer to DEC's Micro Computer Handbook.

Entering ODT

ODT is invoked automatically by one of the following methods:

1. you set the HALT/RUN switch to HALT; or
2. the LSI-11/2 executes a HALT instruction.

The ODT Terminal

The ODT terminal is defined as the terminal connected to the AUXILIARY port of the 8501. The AUXILIARY port is strapped to address 177760.

Table 3-7
ODT Command Summary

Command	ASCII	Function
/ (slash)	057	Opens a memory location or general purpose register (GPR)
CR (RETURN)	015	Closes an open location or GPR
LF (line-feed)	021	Closes open location or GPR and opens the next location or GPR
^ (up-arrow)	137	Closes open location or GPR and opens the previous location or GPR
@ (at-sign)	100	Closes a location and opens a second location using the first location as a pointer
< (back-arrow)	137	Interprets an opened word as an address indexed by the PC
R (register) $	122 044	When followed by a slash, opens a GPR or processor status register
G (GO)	107	Starts execution of the address specified by G
P (proceed)	107	Continues
M (maint.)	115	Prints the contents of internal maintenance registers
rubout	177	Deletes characters
L (loader)	114	Loads a program that is in bootstrap loader format

Manual System Boot-Up

If the firmware does not boot the system, you can boot it manually from the ODT mode. Enter the following:

```
1000/ 000000 41
1002/ 000000 400
1004/ 000000 0
1006/ 000000 0
177160/ 000000 1000
GO
```

These instructions read the boot-up records from disc 0. 0G starts execution of the read boot-up record.

Bypass The Power-Up Tests

You can bypass the power-up tests and enter the Debugging Mode directly while in ODT with the following method:

1. Set the RUN/HALT switch to HALT.
2. Toggle the RESTART switch.
3. Set the RUN/HALT switch to RUN.
4. Enter the following instructions:

```
177546/ 000 000 40
R6/ 000 000 167776
P
```

Maintenance Jumper

If a power-up test failed you may want to use a oscilloscope or other test equipment for further troubleshooting. Removing the maintenance jumper (J1036 on the Utility Board) permits the 8501 to loop on any error. Restart the 8501 and the system loops on any hardware failure that it finds, thus stimulating the failed circuits.

Section 4

DISC-BASED DIAGNOSTICS

GENERAL INFORMATION

Introduction

The disc-based diagnostics package consists of seven individual tests, a system interaction test, and various utility functions serving the diagnostics. The seven tests are:

1. RAM test
2. ROM test
3. CPU test
4. LTC test
5. the AUXPORT (Auxilliary port) test
6. the HSI (High Speed Interface) test
7. the flexible disc test

These tests check the same hardware as the ROM-based Diagnostics, but check it more thoroughly. The additional system interaction test checks the interaction of all 8501 system hardware. This test executes automatically every time all tests are executed in a test series.

The disc-based diagnostics tests the following circuitry:

- the 8501 system memory (RAM)
- the 8501 boot and diagnostics memory (ROM)
- the LSI-11/2 processor
- the line-time clock circuits (LTC)
- all serial data ports (including the HSI port)
- the read/write format capability of the Flexible Disc

The Software

Your DOS/50 system disc contains, along with the normal operating system, a program called DIAGS. DIAGS contains the above listed tests. DIAGS requires that you invoke it and answer the program prompts that occur while DIAGS executes. The disc-based diagnostics is executed on the 8501 from the ODT terminal connected to the AUXILIARY port. (For more information on the ODT terminal, see Section 3, The ODT Terminal.)

Hardware Restrictions

The 8501 diagnostics works only if the 8501 kernel is functional. The 8501 kernel consists of:

- power supplies,
- LSI-11/2 processor,
- That portion of the Utility board containing the boot-ROM,
- that portion of the Utility board containing the serial I/O communications circuits,
- the Communications Adapter (comm adapter) board,
- the Flexible Disc Controller (FDC), and
- a disc drive.

The Run Codes

Seven of the eight tests can be executed individually with the use of the numbered run codes. These numbers, when entered from the ODT terminal, execute the specified test. Run codes are given with a short test description in Table 4-1 on the follwing page.

Table 4-1
Diagnostic Test Summary

Name	Run Code	Description
RAM Test	1	This test checks the RAM system memory. It starts at location 0, takes the contents of location zero and moves it to a register. It then writes data into the location and reads back. This done, the test returns the data from the register and repeats the same operations on the next location. The RAM test test performs this operation on every location in the system memory
ROM test	2	The ROM test performs a checksum test on bootstrap/diagnostic ROMs, and checks for a valid ROM part number. The test consists of two parts with each part testing one ROM.
CPU test	3	The CPU test checks selected instructions and registers. The CPU test checks instructions more complex than the ROM-based CPU test
LTC test	4	The LTC test checks that the 8501 line frequency interrupts work
AUXPORT test	5	The AUPORT test checks the two RS-232-C compatible ports by sending a string of ASCII characters to the ports and reading them back
HSI test	6	The HSI test checks the operation of the HSI port and the associated DMA circuitry
FDC test	7	The flexible disc controller (FDC) test verifies the operation of the flexible disc controller and the disc drives. The test checks the read/write format on an unprotected disc or read format on a write protected disc.

EXECUTING THE DISC-BASED DIAGNOSTICS

Fixtures Required

Although the three serial ports can be tested without any additional hardware, to fully exercise the 8501 ports, requires two wrap-back connectors. Wrap-back connectors are RS-232-type connectors that are wired to feed signals output from the port back into the same port. Thus, data transmitted by the port is feed back into the same port. You can build your own wrap-back connectors from a RS-232-C-compatible connector. For more information see Section 3, Table 3-4.

Test Connections

To execute the 8501 disc-based diagnostics package, you must disconnect the 8501 from the 8301. Figure 4-1 shows the test connections that are required by the 8501 diagnostics.

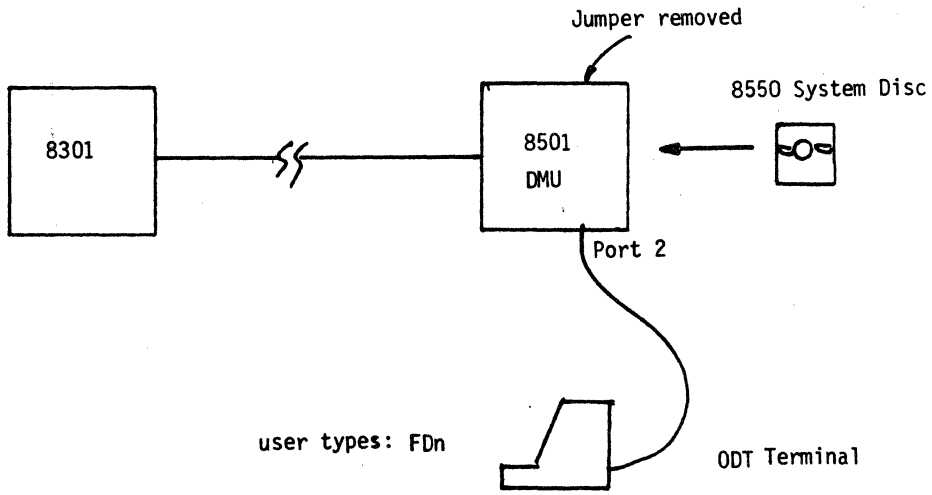


Fig. 4-1. DIAGS system connections.

Executing Procedures

Use the following procedure to execute either an individual test, or all tests sequentially in a test series.

1. Remove the 8501's top cover (Refer to the proper Installation guide for instructions).
2. Find the maintenance jumper (J1036) at the top of the Utility board and remove it.
3. Attach the terminal's RS-232-C Cable to the 8501 AUXILIARY port. Assure that both the terminal and the 8501 are set to the same baud rates.
4. Attach one wrap-back connector to the PRINTER port, and the another to the HSI port (optional)
5. Turn on the terminal, and allow it to warm up until the curser is visable.
6. Now turn on the 8501's primary power switch (on rear panel). You'll hear the 8501 cooling fan.
7. Push the front panel DC switch to ON.
8. After approximately three seconds, the terminal screen displays a $ indicating that you are in Debugging Mode.
9. Place the DOS/50 disc into drive 0 and close the drive door.
10. Enter the command FDn on the terminal, followed by a RETURN (depress the keyboard RETURN key.) The n is the number of the disc drive containing the DOS/50 disc.
11. After the FDn command is entered, the 8501 searches the disc for the DIAGS program, loads it, and begins execution.

When the 8501 diagnostics is loaded, the terminal displays an identification message followed by the first selection menu.

```
**************DMU DIAGNOSTICS - VERSION 1.0 - LOADED**************

OPTION MENU

0 - RUN ALL TESTS [DEFAULT]
1 - TEST DMU RAM
2 - TEST DMU ROM
3 - TEST DMU PROCESSOR
4 - TEST DMU LINE-TIME CLOCK
5 - TEST DMU AUX CHANNELS
6 - TEST DMU HSI CHANNEL
7 - TEST FLEXIBLE DISC DRIVES
8 - ALIGN FLEXIBLE DISC DRIVES
9 - EXIT FROM DMU DIAGNOSTICS
H - HELP

TYPE IN OPTION (0 - 9 OR H)
?
```

The disc-based diagnostics gives you the option of executing one test at the time and thus testing individual 8501 components, or running all tests in sequence by typing a RETURN or a zero. In this example we want to execute the ALL test series (all seven tests) thus we type a RETURN.

Next, DIAGS displays the loop control menu. You can ask DIAGS to loop on the test when you'll see this terminal display:

LOOP CONTROL MENU

```
1 - DO NOT LOOP ON TEST [DEFAULT]
2 - LOOP ON TEST
H - HELP

TYPE IN LOOP CONTROL (1 - 2 OR H)
?
```

We will not want to loop on a test, so enter RETURN

The next menu determines whether the run-time status of DIAGS will be displayed. The menu looks like this:

DISPLAY MODE MENU

```
1 - DISPLAY RUN-TIME STATUS [DEFAULT]
2 - NO RUN-TIME DISPLAY
H - HELP

TYPE IN MODE (1 - 2 OR H)
?
```

Enter a RETURN to display the run-time status.

The last menu selects where the device will display the diagnostic results. displayed.

DISPLAY OUTPUT MENU

```
1 - DISPLAY ON TERMINAL [DEFAULT]
2 - DISPLAY ON TERMINAL AND 8301 PRINTER
3 - DISPLAY ON 8501 CHANNEL 1
4 - DISPLAY ON 8501 CHANNEL 2
H - HELP

TYPE IN DISPLAY OUTPUT (1 - 4 OR H)
?
```

For verification purposes, we'll want the results of the test displayed on the terminal, so enter a RETURN.

At this point, DIAGS begins to execute the ALL test series.

Diagnostics Execution

When you type a RETURN (or 0) DIAGS executes the ALL test series (tests 1 through 7 as they appear on the option menu). When the tests are executed in the series, the error information for every test is displayed at the end of the series. When you execute individual tests, however, DIAGS displays errors after each test. When the ALL test series is completed, DIAGS automatically enters the system interaction test. The following example displays assume that you entered a RETURN , and thus executed the ALL test series. While DIAGS executes, it keeps you informed about test status via the ODT terminal (see The ODT Terminal, Section 3). The ODT terminal displays the name of each test as it is executed. When executing the ALL test series the ODT terminal also displays the elapsed time since the test was started.

```
INITIALIZING THE I/O REGISTERS...
BEGINNING OF PASS 1 ELAPSED TIME: 0 : 0 : 0
TESTING RAM...
VERIFYING ROM...
TESTING PROCESSOR...
TESTING LINE TIME CLOCK...
TESTING AUX CHANNELS...
AUXPORT J151
AUXPORT J152
TESTING HSI CHANNEL...
```

The next test checks the disc in drive 0 or drive 1.

CAUTION

If you enter Y after the flexible disc question, and you still have the DOS/50 disc in drive 0, the contents of the disc will be destroyed. If you want to test the read/write capability of the flexible disc drives, be sure to insert a scratch disc (a disc that has been formatted but contains no files) in drive 0 or drive 1. Blank discs can be used but the test then generates a "DISC NOT FORMATTED" error.

DIAGS will ask if it's alright to write on the flexible disc in drives 0 and 1. Unless you want to test the drives, enter N after each question.

```
TESTING FLEXIBLE DISCS...
OK TO WRITE ON FLX0 ? (Y OR N)
OK TO WRITE ON FLX1 ? (Y OR N)
```

When you are executing the ALL test series, DIAGS automatically enters the system interaction test after the seven tests have been completed.

The system interaction test is the final system test that checks if all individual system comnponents interact with each other as designed. The system interaction test can not be executed by itself; it is always part of the ALL test series. The system interaction test executes in about 2 minutes and displays the contents of the error registers on the ODT terminal. The error register contents change continously, as the system interaction test puts the system through its paces. If the system interaction test passes, you can be reasonably sure that your 8501 is operating properly.

```
BEGINNING DEVICE INTERACTION TEST...
SECONDS   ROM    RAM    CPU    INT    BUS    LTC    HSI    AUX1   AUX2   FLX
000067  000000 000000 000000 000000 000000 000000 000000 000001 000000 000000

VERIFICATION PASSED.  DO YOU WANT TO SEE MORE INFORMATION? (Y OR N)

COMMAND?
```

If you respond with a N the option menu is displayed again.

If the 8501 passed the disc-based diagnostics, replace the maintenance jumper on the Utility board, and replace the 8501 top cover.

The 8501 Failed

If DIAGS displayed any warning messages, some portion of the 8501 did not pass. You'll see messages such as:

```
***WARNING -- PROM ERROR: LOPROM
PROBABLE SOURCE: UTILITY BOARD
***WARNING -- AUXPORT J152 ERRORS
PROBABLE SOURCE: UTILITY BOARD
```

If you did answer Y after the completion of the system interaction test, a display similar to the one shown below appears on the ODT terminal.

```
                          DMU STATISTICS
        NOTE: ADDRESSES AND REGISTER VALUES ARE LISTED IN OCTAL
NUMBER OF TEST CYCLES  1      ELAPSED TIME;  0 : 2 : 0
UTILITY BOARD ROM PART NUMBERS: 160 399 0, 160 400 0
***WARNING - OBSOLETE FIRMWARE
TOP OF RAM: 167776
LINE-TIMECLOCK FREQUENCY = 60 HZ
LINE-TIME STATUS: 000340

  REGISTERS FOR AUX PORT J151
BAUD   RCSR   RBUF   XCSR   XBUF
2400  040000 000000 070200 000000

  REGISTERS FOR AUX PORT J152
BAUD   RCSR  RBUF   XCSR   XBUF
9600 160100 000000 100200 000000

  REGISTERS FOR HSI
BAUD     DMA     CTR    DDR    VEC    RCSR    RBUF    XCSR    XBUF
153.5K  000000  000000 102646 000374 000001 000000  000000  000000

FLEXIBLE DISC FIRMWARE VERSION 1.0

FLEXIBLE DISC 0 DISC TYPE: DOUBLE SIDED, DOUBLE DENSITY
RECOVERABLE ERRORS ON INNER TRACKS: NONE OUTER TRACKS: NONE
RECOVERABLE ERRORS ON SIDE 0: NONE SIDE 1 NONE

              FLEXIBLE DISC REGISTERS
FDCBPR   FDCR   FDWCR   FDDAR   FDDMAR  FDER    FDCR   FDDR
102410 100000  000000  000000  103646  000000  000000 000000

FLEXIBLE DISC 1 DISC TYPE: NONE

VERIFICATION FAILED
```

TEST PROGRAM DESCRIPTIONS

The Diagnostic Diagrams

The tests in this section are described with the aid of the diagnostic diagrams. These diagrams show how the software exercises the various system components. These diagrams show the overall effect of a combination of instructions. Figure 4-2 is an example of the diagram format. Actions or conditions are contained in brackets and are normally located near middle of the page in each diagram. The boxes on either side represent hardware devices or controlling devices either acting or being acted upon. Some examples of hardware devices include:

- o a complete unit (system terminal)
- o a circuit board (system memory)
- o a controlling device (LSI-11 processor)
- o a part of a device

A small diamand leaving a device box indicates a decision. If the action decribed in the brackets is true, the action is transferred in the direction of the arrow. The rectangular box on the right in the diagram represents a branch. The number inside the box identifies the next executed part of the test.

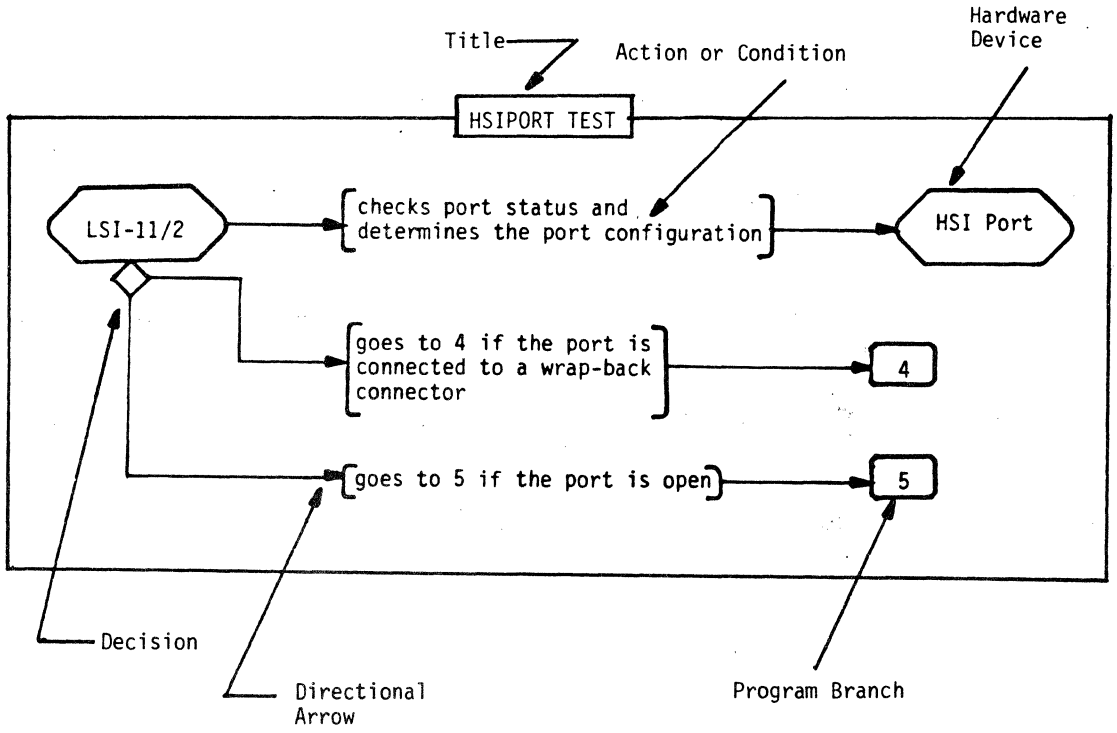


Fig. 4-2. Diagnostic diagram example.

DISC TEST NO. 1
RAM Memory test

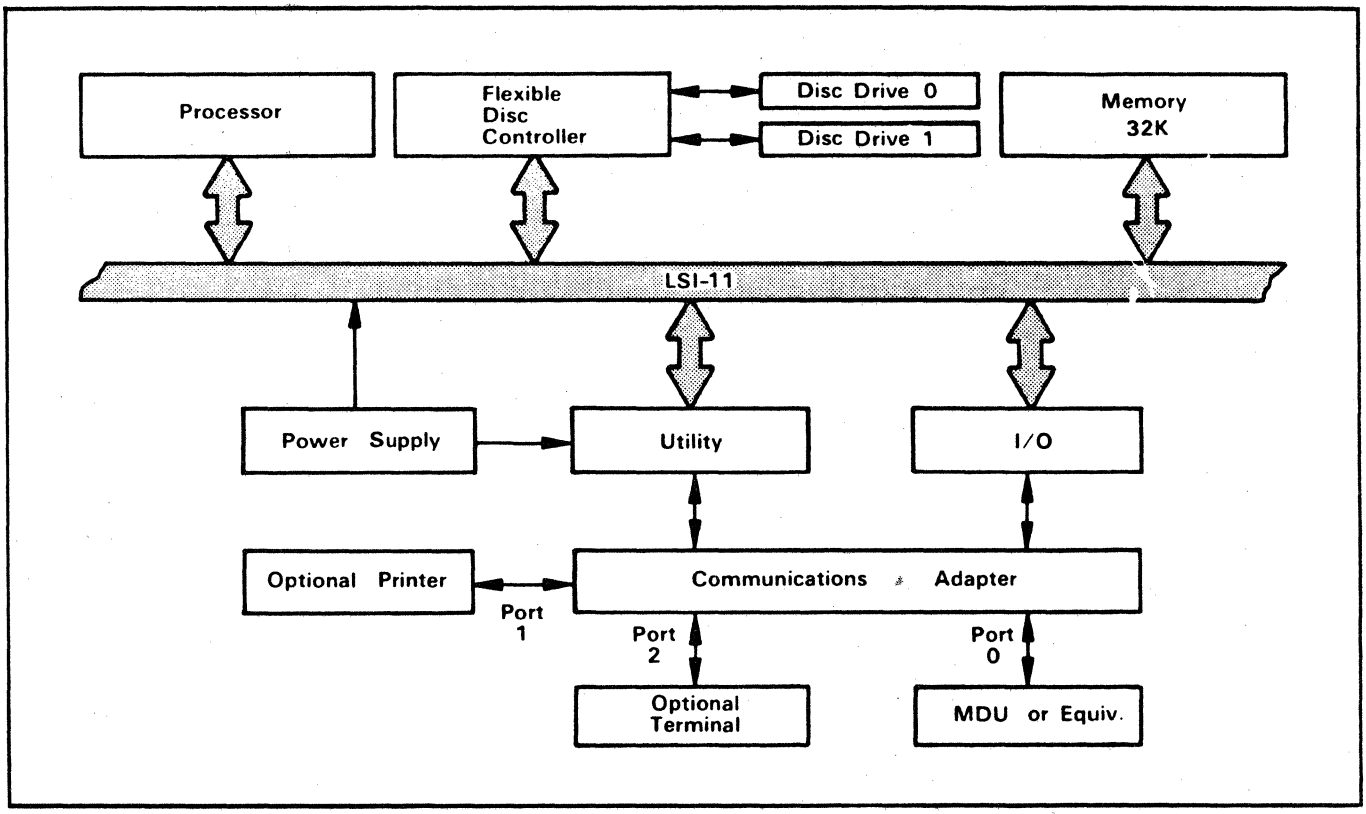


Fig. 4-3. 8501 block diagram.

TEST NAME:	RAM memory test
RUN CODE:	1
FUNCTION:	Checks the data storage capability of the system's RAM memory
BLOCKS INVOLVED:	LSI-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive
ERROR MESSAGES:	WARNING RAM ERROR, TOP OF RAM

DESCRIPTION

1. READ MEMORY (Fig. 4-4). The RAM test starts at location 0, reads its contents, and stores the contents in a general purpose register.

2. WRITE TEST DATA. The RAM test writes the test data into location 0, reads it back, and compares it against the written data. Next, the test complements the test data, writes it into the tested location, and reads it back. If on either pass the test finds an error, it stores the error in system memory for recall at the end of the test.

3. RECALL ERROR INFORMATION. If the test is executed alone, and all locations have been tested, the test recalls the error information from the memory and displays it on the ODT terminal. If the test is executed in the ALL series, the error data is displayed at the completion of the test series.

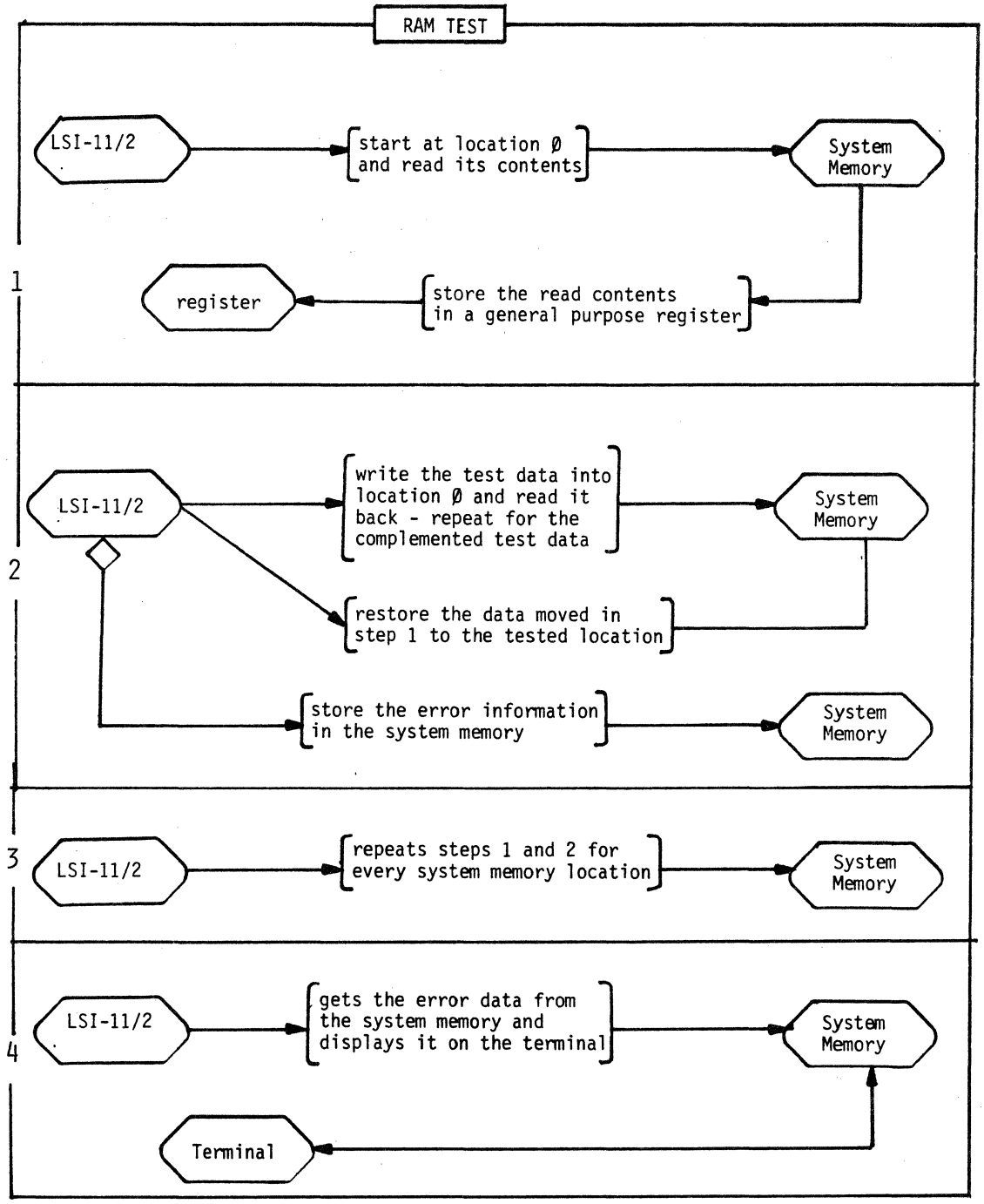


Fig. 4-4. RAM test.

DISC TEST NO. 2
ROM Test

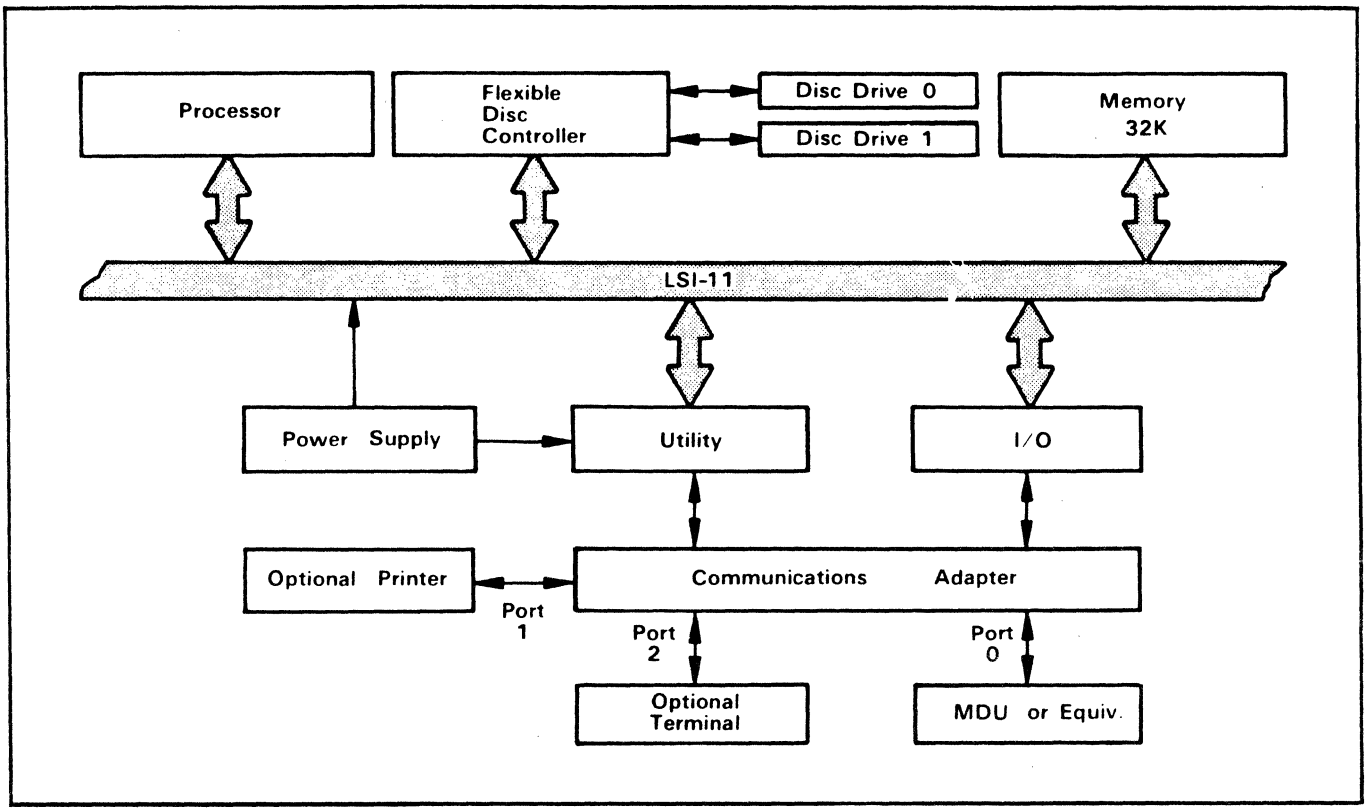


Fig. 4-5. 8501 block diagram.

TEST NAME: ROM test

RUN CODE: 2

FUNCTION: To check the data storage capability of the diagnostic/bootstrap ROM memory.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive

ERROR MESSAGES: WARNING PROM ERRORS

DESCRIPTION

1. BEGIN CHECKSUM TEST (Fig. 4-6). The disc performs the checksum test stored on the low-byte ROM, calculates the checksum and compares it against the checksum stored in the system memory. The ROM test also reads the ROM-stored part number and compares it against the part number stored in the program.

2. TEST HIGH-ORDER ROM. The test performs the checksum test stored on the high-byte ROM, calculates the checksum and compares it against the checksum stored in the system memory. The ROM test also reads the ROM-stored part number and compares it against the part number stored in the program.

3. TEST LOW-ORDER ROM. If the test is executes alone, and both ROMs have been checked the program recalls the error information from the memory and displays it on the ODT terminal.If the test is part of the ALL series, the diagnostics displays the error at the completion of the test series.

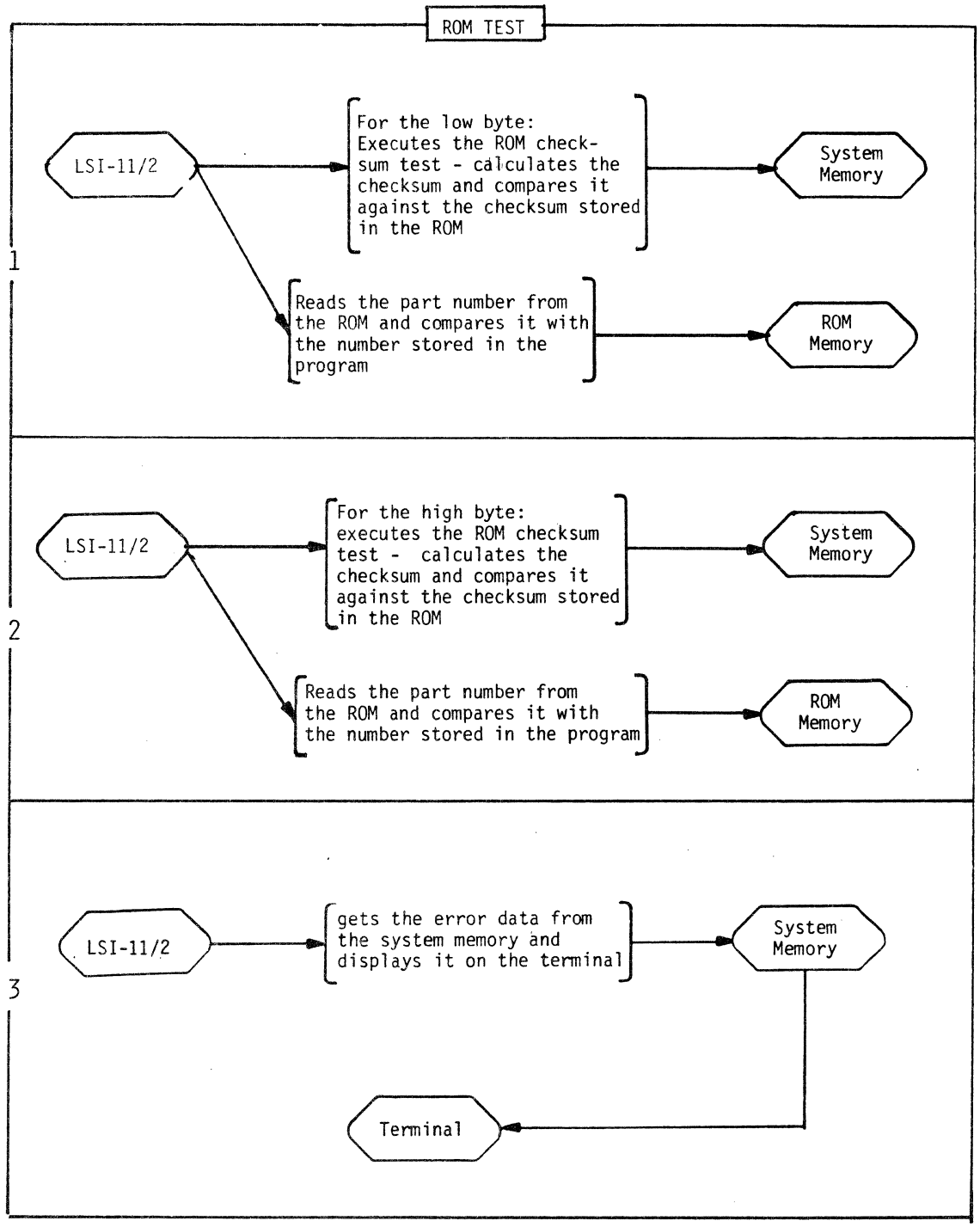


Fig. 4-6. ROM test.

DISC TEST NO. 3
CPU Test

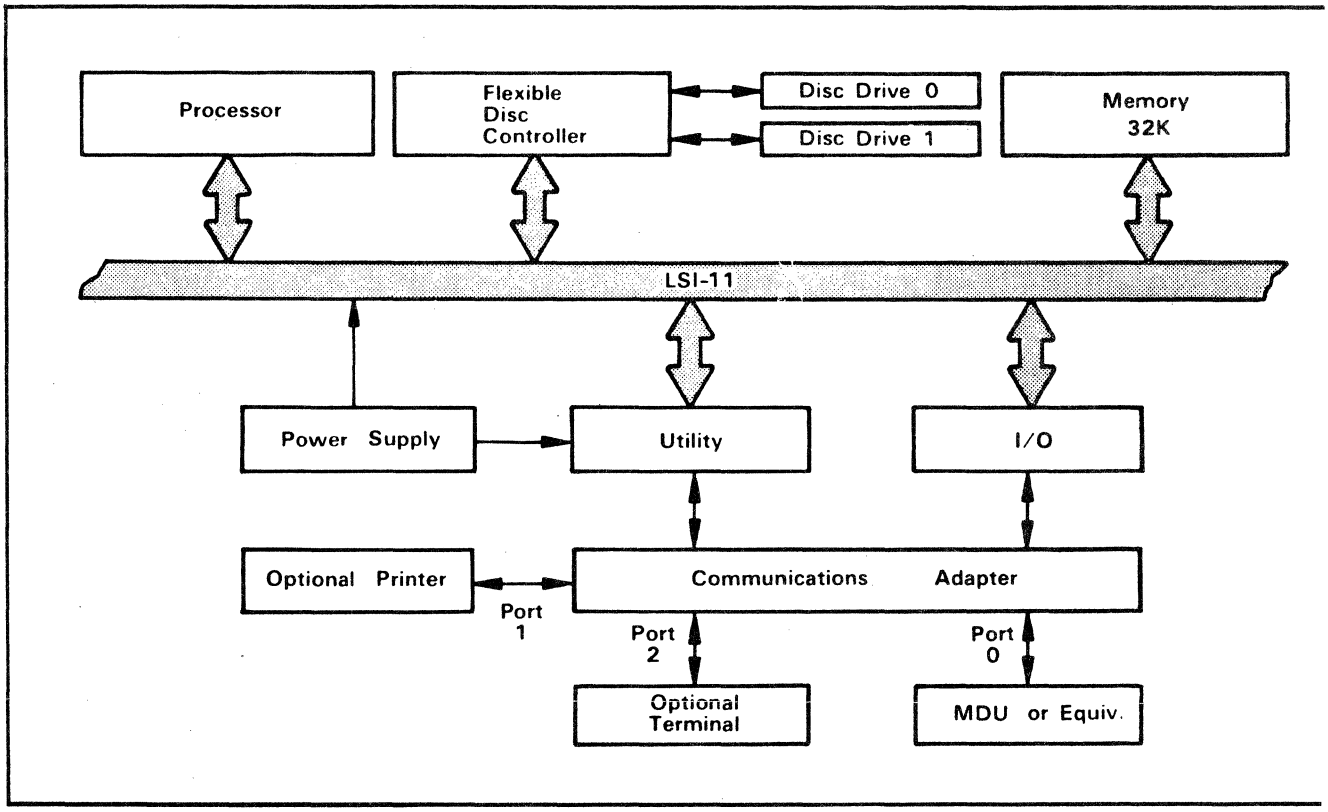


Fig. 4-7. 8501 block diagram.

TEST NAME: CPU test

RUN CODE: 3

FUNCTION: To check the operation of the CPU by executing a representative instruction set.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive

ERROR MESSAGES: WARNING PROCESSOR ERROR

DESCRIPTION

CPU TEST (Fig. 4-8). The CPU test checks execution of the LSI-11/2 instructions. The test does not check all combinations of the LSI-11/2 instruction set, but executes a representave sample of all possible LSI-11/2 instructions. This test checks a larger instruction set than the ROM-based test. The CPU test executes first the simpler instructions followed by the more complex ones. The CPU test verifies most CPU operations by checking:

- o all single operand instructions,
- o all source modes for double operand instructions, with destination mode 0,
- o all double operand instructions with destination mode 0, and source modes 1,2, and 3,
- o TST and TSTB instructions,
- o condition code operators,
- o word instructions with all destination modes,
- o JSR and RTS instructions, and
- o trap instructions.

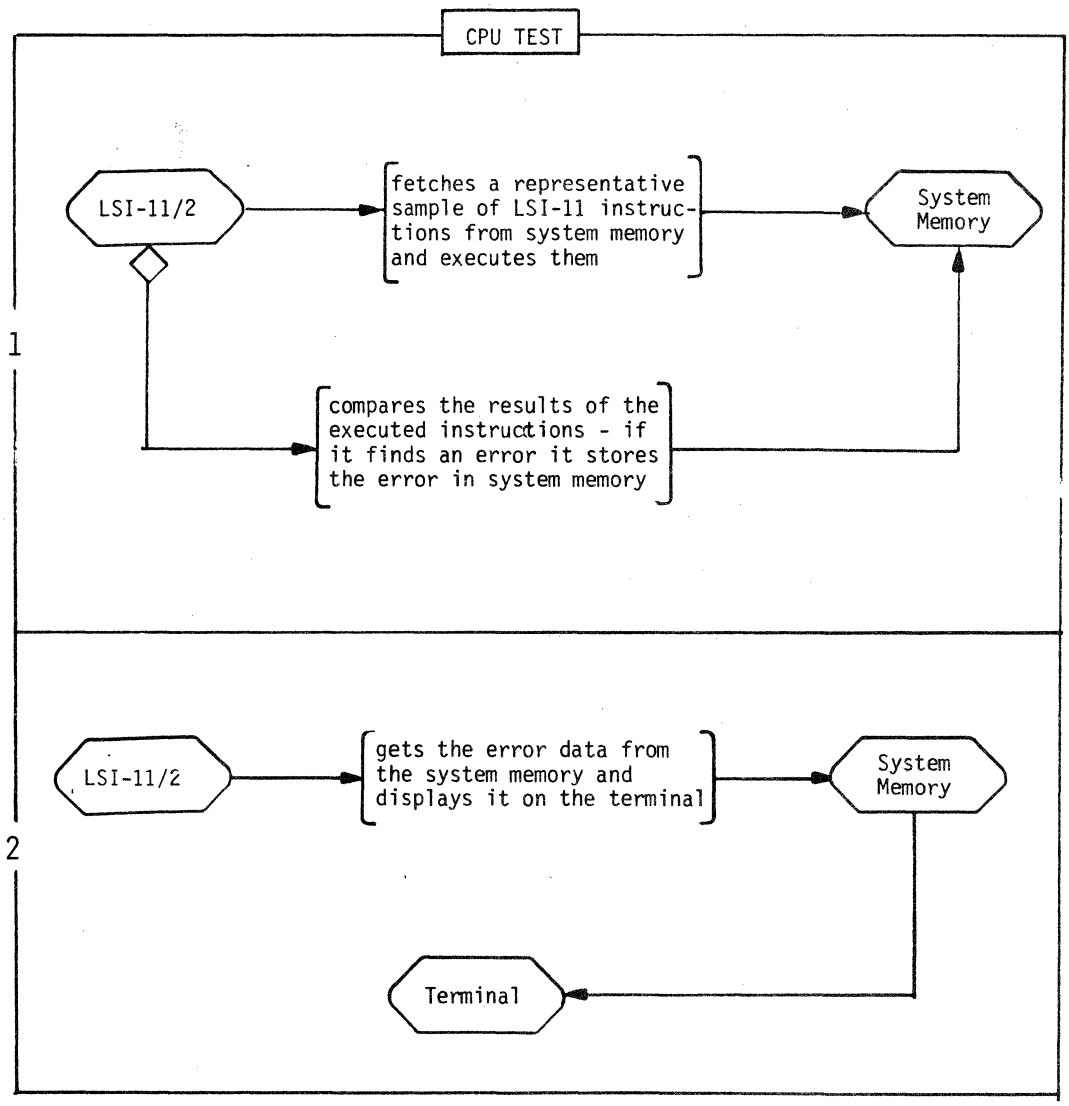


Fig. 4-8. CPU test.

DISC TEST NO. 4
LTC Test

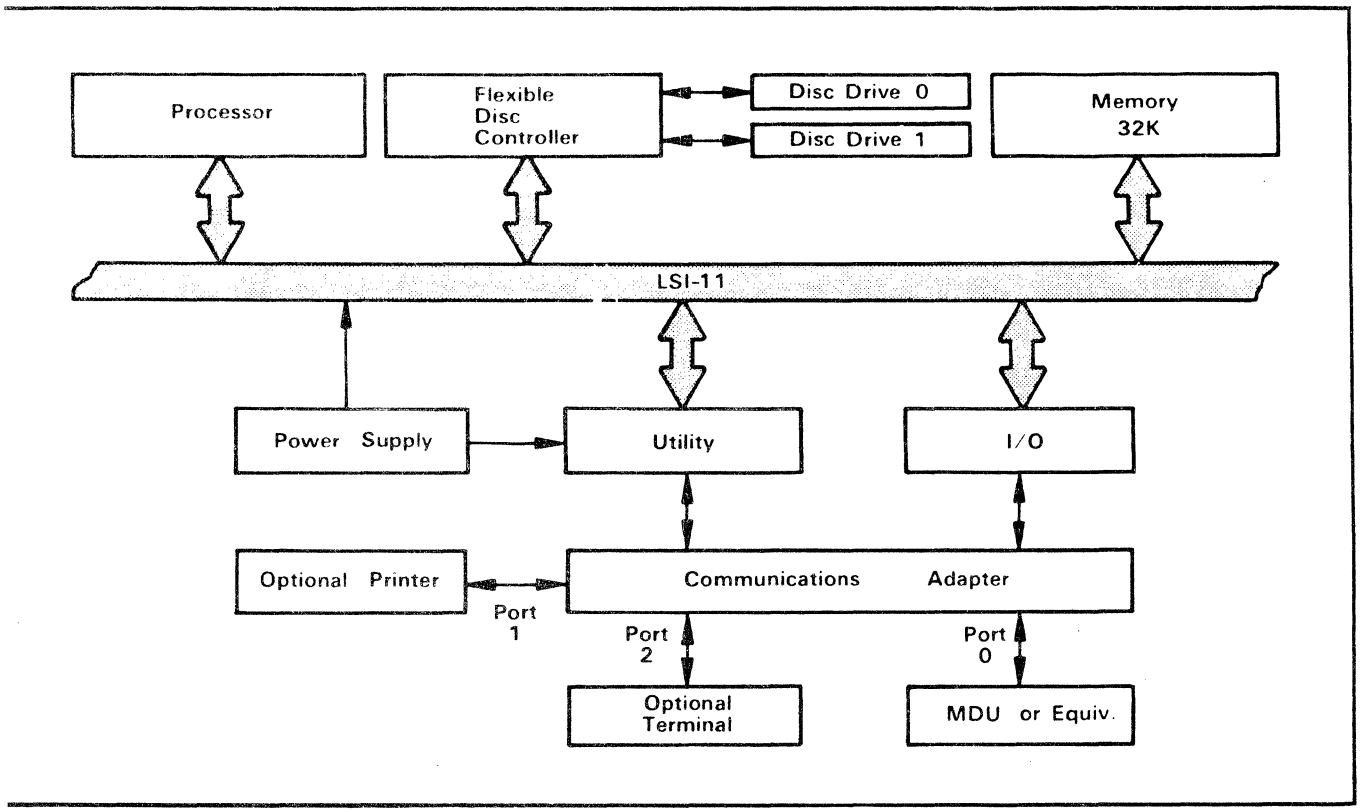


Fig. 4-9. 8501 block diagram.

TEST NAME: LTC TEST

RUN CODE: 4

FUNCTION: To check the frequency of the interrupts from the AC power source.

BLOCKS INVOLVED: LSI-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive

ERROR MESSAGES: WARNING LTC ERROR, MISSING INTERRUPTS LINE TIME CLOCK, LINE TIME CLOCK FREQUENCY = nn HZ, LINE TIME CLOCK STATUS nnnn

DESCRIPTION

This test checks that the system is connected to the power source with the correct frequency. The test uses the line-time clock to count the interrupts caused by the line frequency.

1. INITIALIZE INTERRUPTS (Fig. 4-10). The LTC test initializes the interrupts and enters a loop for one second. During that time each line frequency cycle generates one interrupt in the line time clock. The program counts these interrupts. After one second, the program compares the counted interrupts against the specified number in the program. The test accepts interrupt counts between 48 and 52 (for the 50 Hz line frequency) and between 58 and 62 (for the 60 Hz line frequency). If the interrupt count does not fall within the specified ranges the program exits.

DISPLAY ERRORS. If the test is executed alone, the program recalls the error information from the memory and displays it on the.ITEM terminal.If the part of the ALL series, the error data is displayed at the completion of the test series.

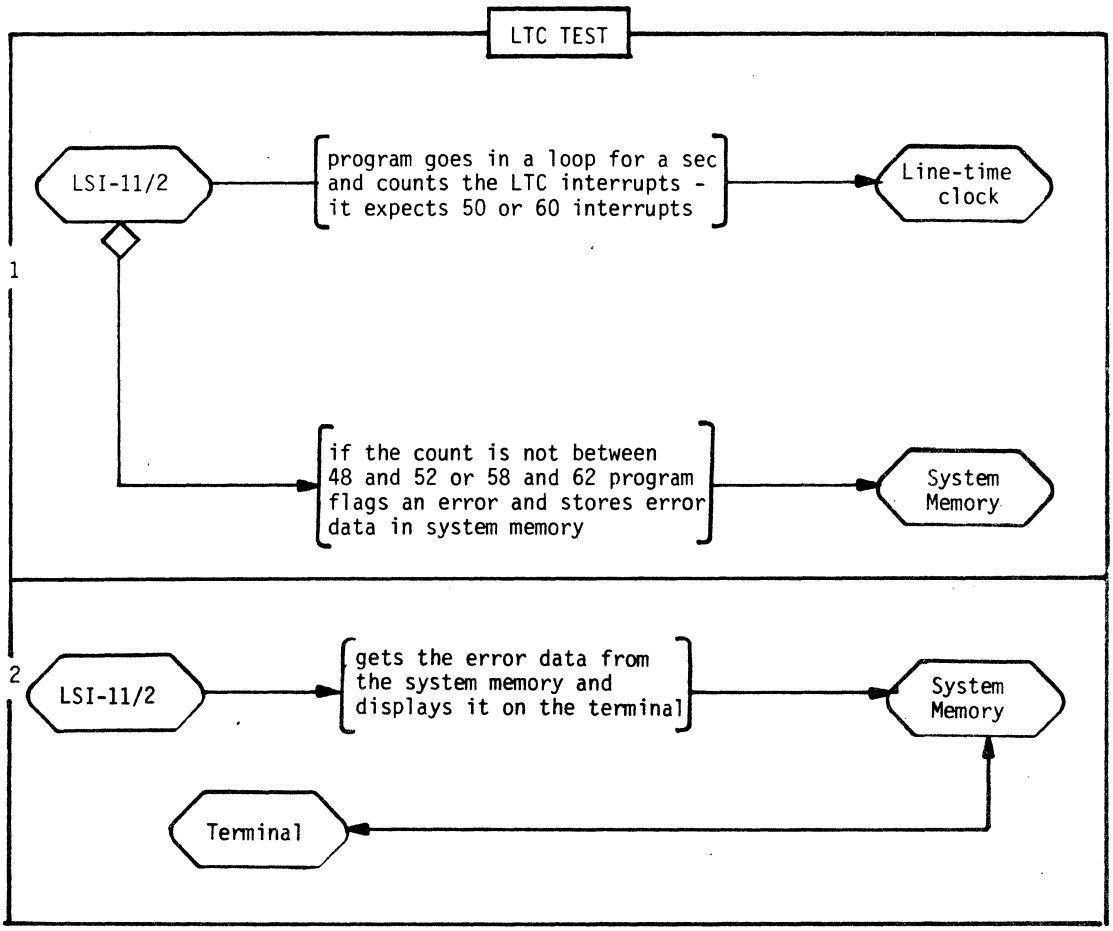


Fig. 4-10. LTC test.

DISC TEST NO. 5
AUXPORT Test

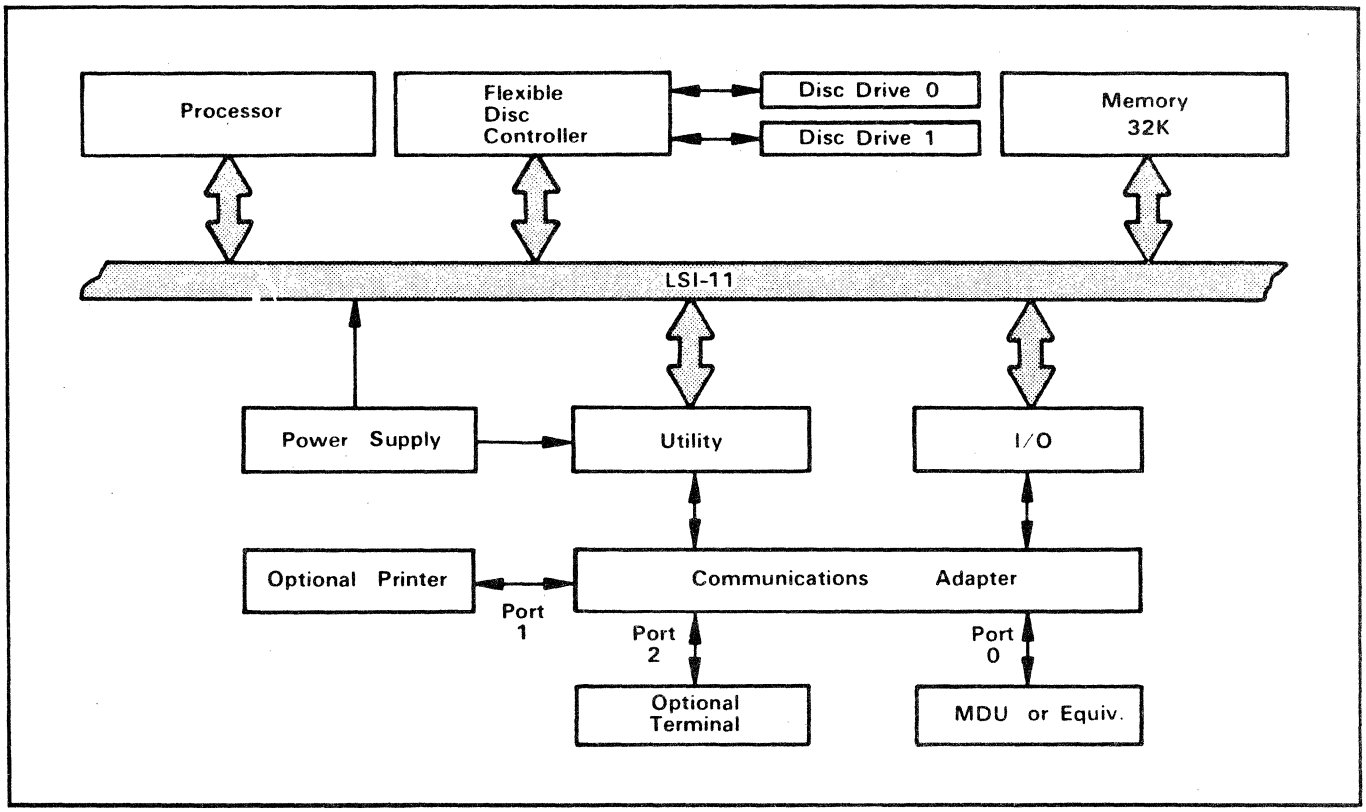


Fig. 4-11. 8501 block diagram.

TEST NAME:	AUXPORT (Auxiliary port) TEST
RUN CODE:	5
FUNCTION:	To check the two auxiliary (RS-232-C) ports
BLOCKS INVOLVED:	LS1-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive

ERROR#MESSAGES: REGISTERS FOR PORT AUXN
PORT AUXN INPUT NOT PRESENT
PORT AUX N OUTPUT NOT PRESENT
BAUD RATE FOR PORT AUXN NOT AS SHIPPED
PORT AUXN INPUT INTERRUPT NOT PRESENT
PORT AUXN OUTPUT INTERRUPT NOT PRESENT
LP MODE FOR AUXN NOT AS SHIPPED
NNN DATA ERRORS
WARNING: INCORRECT ADDRESS STRAPPING FOR PORT AUXN

DESCRIPTION

The AUXPORT test consists of two identical tests with one test checking the RS-232-C PRINTER port (J151) and the other checking the RS-232-C AUXILIARY port (J152). Furthermore, each test is divided into individual routines, the use of which depends on the system configuration. The AUXPORT test can test the two ports under the various conditions determined by the external the external port connections. The AUXPORT testchecks the port operation with the port connected to either one of the following:

a wrap-back connector,
a line printer,
the terminal from which the test is exercised, or
an open circuit.

These four conditions are described in steps 4 through 7. Steps 1 through 3 determine which of the above steps are executed. Step 8 repeats the test for the AUXILIARY port, and step 9 displays the error information if the test was executed by itself. (The ALL series displays the error information following the last test in the series).

1. INITIALIZE SOFTWARE (Fig. 4-12). The test initializes the software and identifies the location of the ODT terminal from wich the test is executed). The test initializes the ODT terminal and checks if the ODT terminal is connected to the port to be tested. The AUXPORT test also sets the interrupts vectors and enables interrupts.

2. TEST PORT RESPONSE. Next, the test checks the port response by checking if the appropiate bits in the communications (comm) registers can be set and cleared. If they do not respond, that is the bits can be neither set nor cleared, the test exits and proceeds to AUXILIARY port.

3. TEST PORT CONFIGURATION. The test determines the port configuration. That is, the test determines which of the four possible conditions applies. Once the test has found the port's condition, it exits to the appropiate routine and performs the test under the specified conditions.

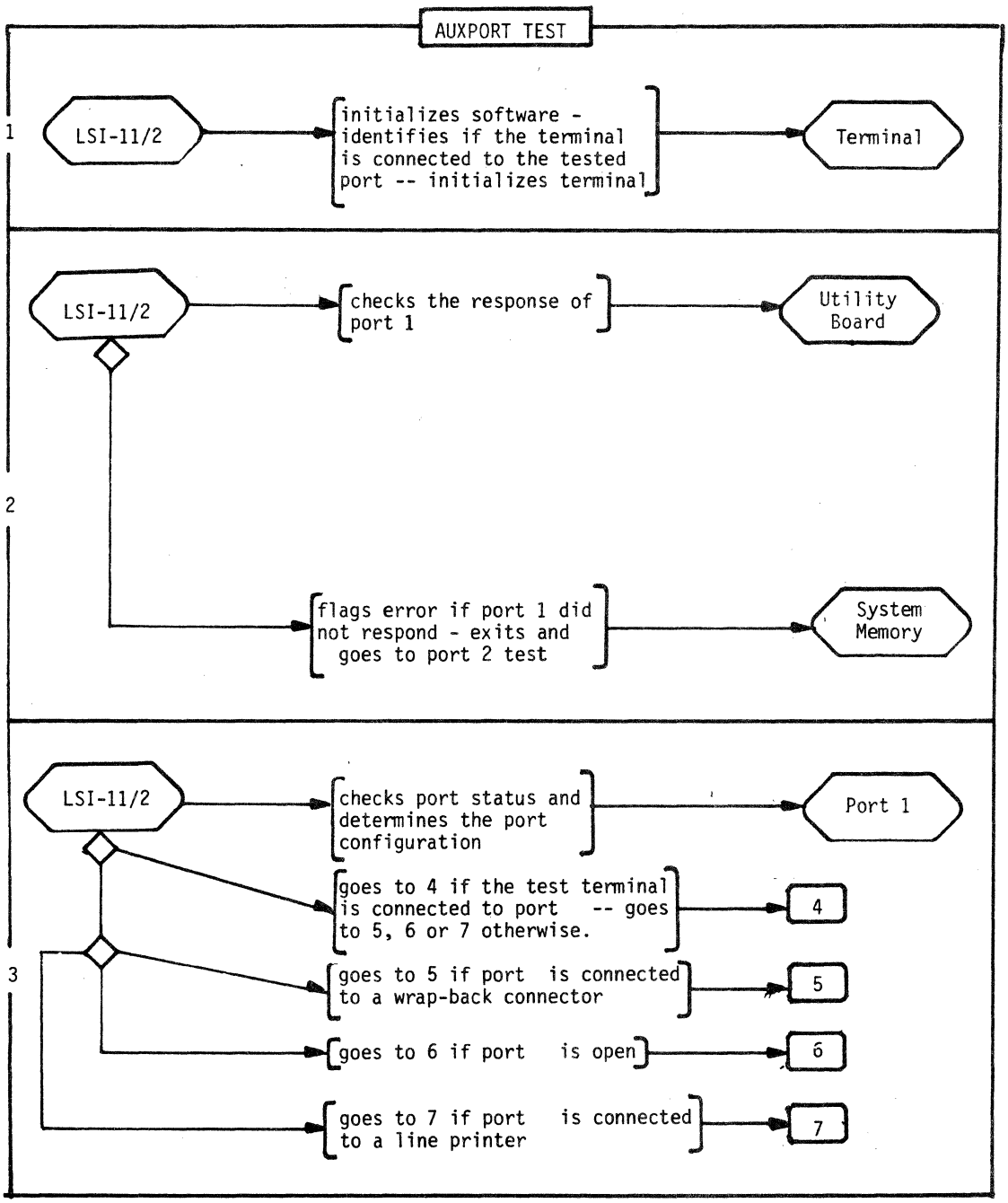


Fig. 4-12. Auxiliary port test.

4. TEST REGISTER (Fig. 4-13). This routine checks the status of the communications register bits.

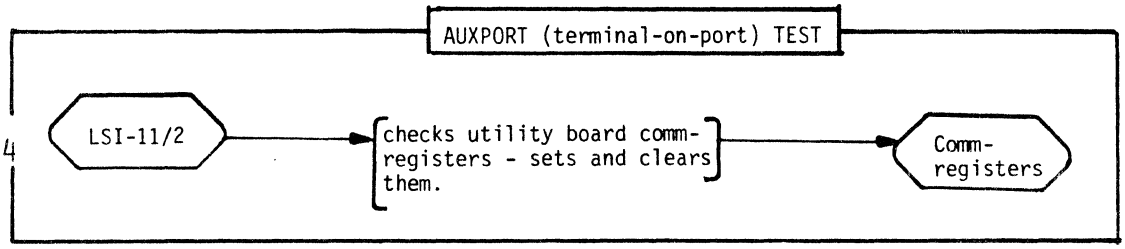


Fig. 4-13. Terminal on-port test.

5. TEST WITH WRAP-BACK (Fig. 4-14). The LSI-11/2 processor sends a set of data to the port and reads it back via the wrap-back connector. The test also checks that the appropiate communications register bit can be set and cleared.

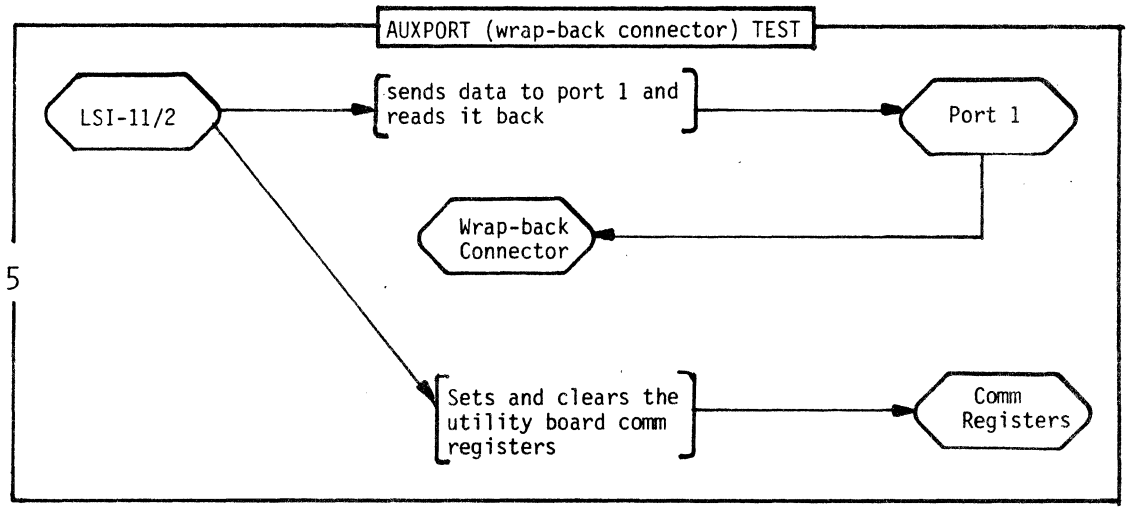


Fig. 4-14. Wrap-back test.

6. OPEN PORT TEST (Fig. 4-15). For the open port test the LSI-11/2 processor cheks the appropiate comm register bit. The test sets and clears the proper bits thus certifying that the proper port function was accessed. Since this test does not read data from the port, its function is very limited.

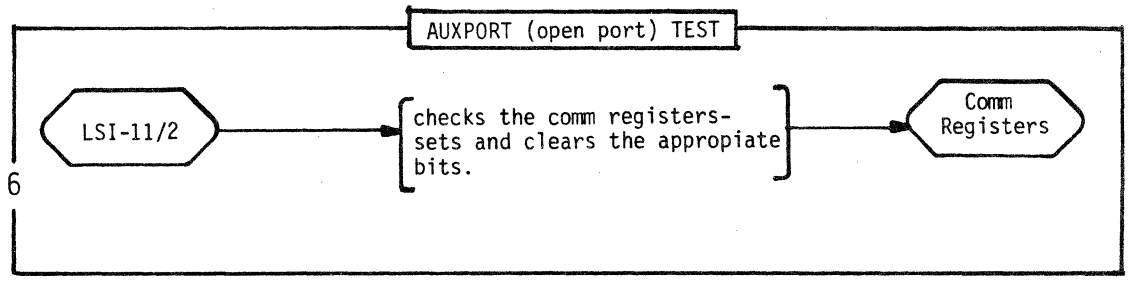


Fig. 4-15. Open port test.

7. LINE PRINTER TEST (Fig. 4-16). The LSI-11/2 processor sends a pattern of letters to the line printer via the PRINTER port. You can then visually compare the received (printed) line printer pattern to the pattern shown below. On a wide line printer, the pattern below appears on one line.

```
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^
_`abcdefghijklmnopqrstuvwxyz{|}~
```

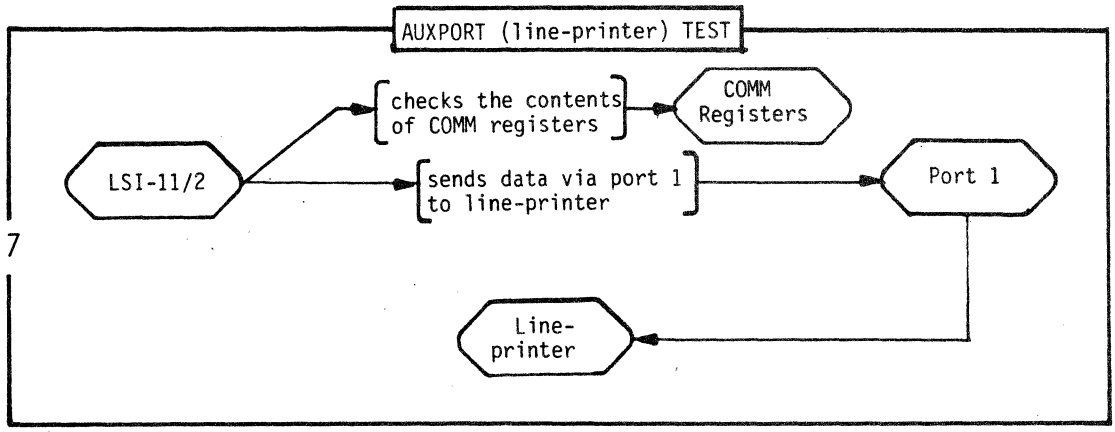


Fig. 4-16. Line printer test.

8. REPEAT 1 THROUGH 7 (Fig. 4-17). This portion of the AUXPORT test repeats steps 1 through 7 for AUXILIARY port. Otherwise, this part is identical to the PRINTER port test.

9. RETRIEVE ERRORS (Fig. 4-17). If the AUXPORT TEST is executed alone, part 9 retrives the error information from the system memory and displays it on the ODT terminal. If, however, the AUXPORT test was executed within the ALL series, the error information is displayed at the end of the series.

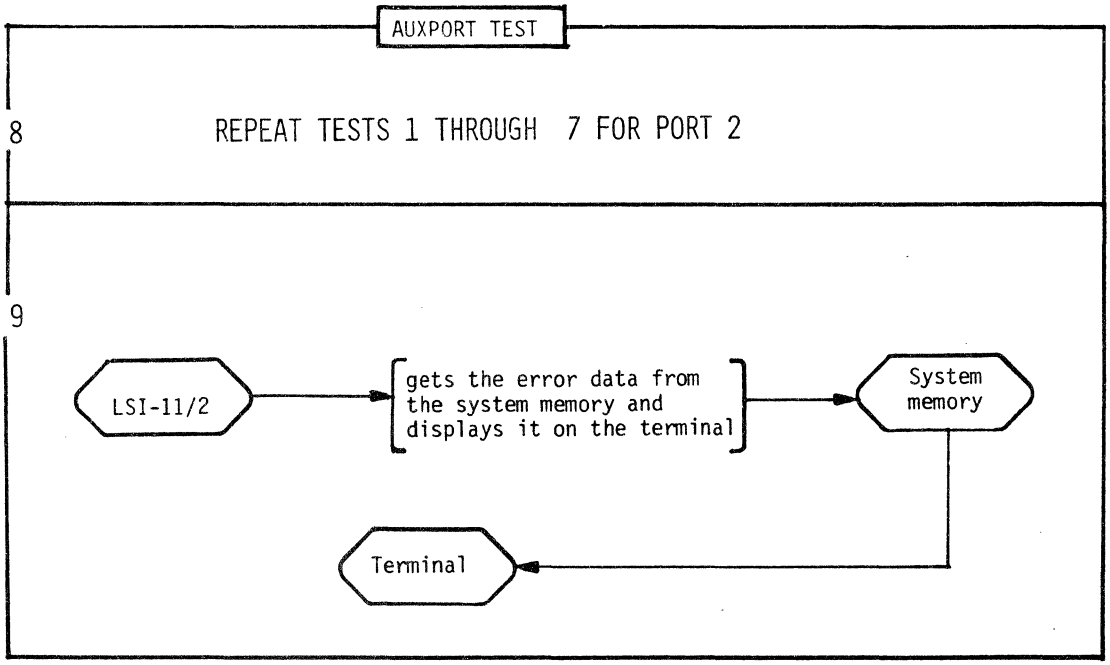


Fig. 4-17. AUXPORT test.

DISC TEST NO. 6
HSIPORT Test

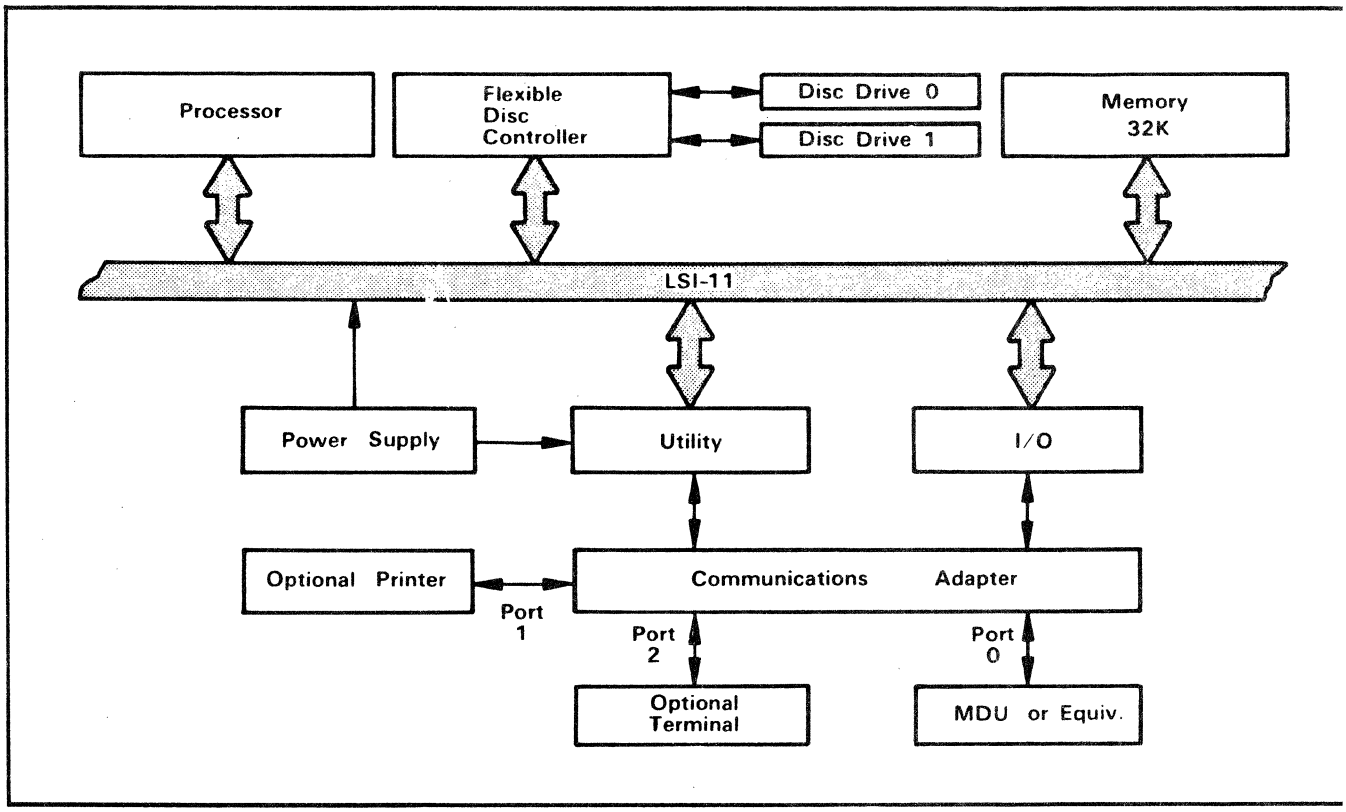


Fig. 4-18. 8501 block diagram.

TEST NAME:	HSIPORT (High-Speed Serial Interface port) TEST
RUN CODE:	6
FUNCTION:	To check the operation of the high-speed serial interface port.
BLOCKS INVOLVED:	LSI-11/2 Processor, Utility board, System memory, I/O board, Disc Controller, Disc drives

ERROR CODES:

REGISTERS FOR HSI
BAUD RATE FOR HSI NOT AS SHIPPED
WARNING--HSI CONTROL--DMA ERRORS
HSI OUTPUT INTERRUPT NOT PRESENT--
CHANNEL NOT FULLY TESTED
HSI OUTPUT NOT PRESENT--
CHANNEL NOT FULLY TESTED
HSI INPUT INTERRUPT NOT PRESENT --
CHANNEL NOT FULLY TESTED
HSI INPUT NOT PRESENT --
CHANNEL NOT FULLY TESTED
NNNN DATA ERRORS
HSI DMA INTERRUPT NOT PRESENT -
CHANNEL NOT FULLY TESTED
WARNING - INCORRECT ADDRESS STRAPPING FOR HSI

DESCRIPTION

The HSIPORT test is similar to the AUXPORT test. HSIPORT test checks the HSI port with the port either open or connected to a wrap-back connector. The HSIPORT test conditions depend on the external port connections. The two conditions are described in steps 4 and 5. Steps 1 through 3 determine which step is executed, and step 6 displays the error information if the test is executed by itself (the ALL series displays the error information following the last test). Some HSIPORT routines use the eight communication status registers located in the I/O board.

1. INITIALIZE TEST (Fig. 4-19). The test initializes the software.

2. TEST REGISTERS. Next, the test checks the port response by checking if the appropiate bits in the communications registers can be set and cleared. If the bits can not be set nor cleared, the test exits.

3. TEST CONDITION. The test determines which port condition applies. Once the the test has determined the port's condition, it exits to the appropiate routine and tests the port.

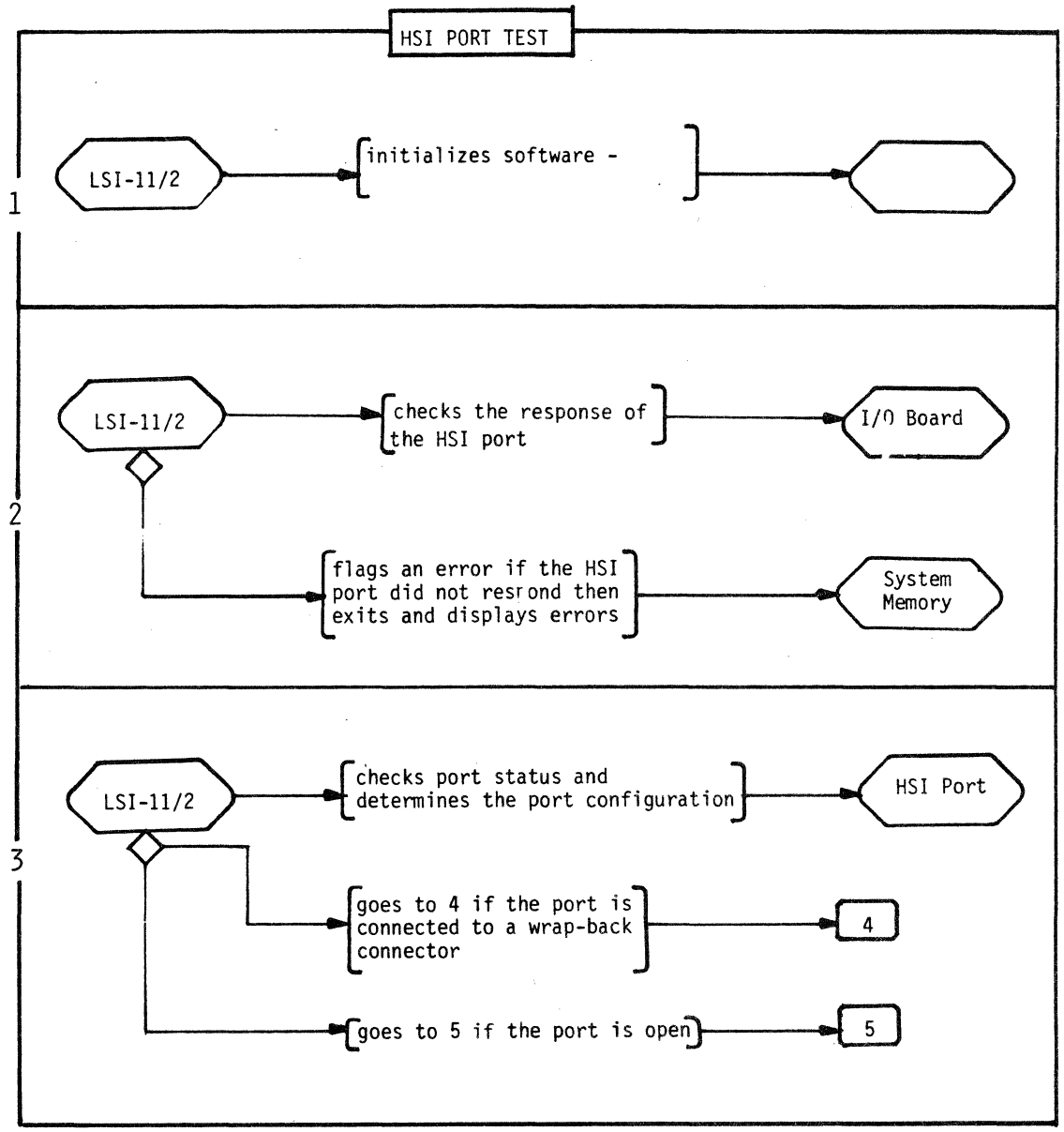


Fig. 4-19. HSI port test.

4. WRAP-BACK TEST (Fig. 4-20). The LSI-11/2 sends a set of data to the port and reads it back via the wrap-back connector. The test also checks that the appropriate communications register bit can be set and cleared.

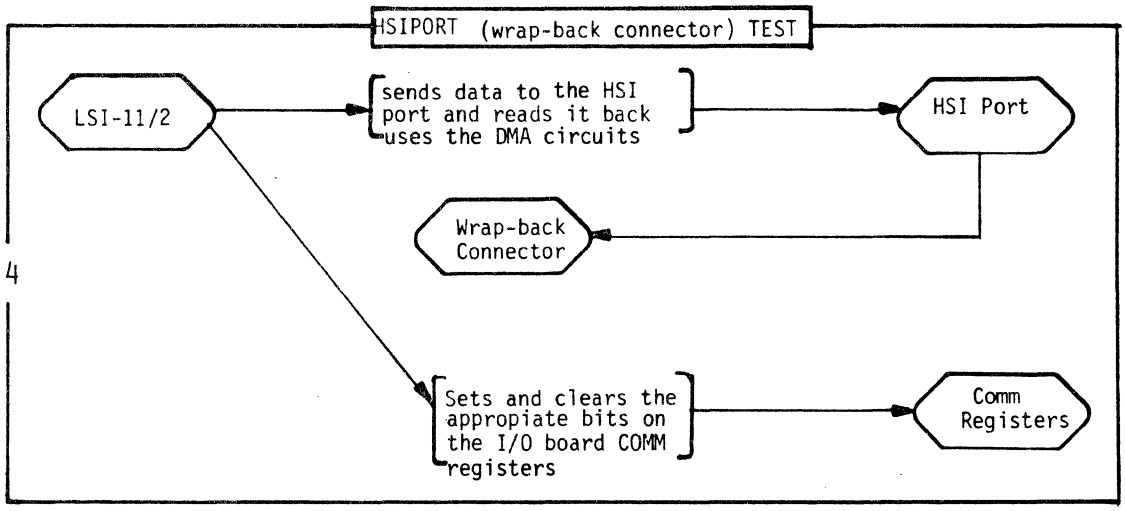


Fig. 4-20. Wrap-back test.

5. OPEN PORT TEST (Fig. 4-21). The LSI-11/2 checks the appropriate communications register bit. The test sets and clears the proper bits thus certifying that the proper port function was accessed. Since this test does not read data from the port, its usefulness is limited.

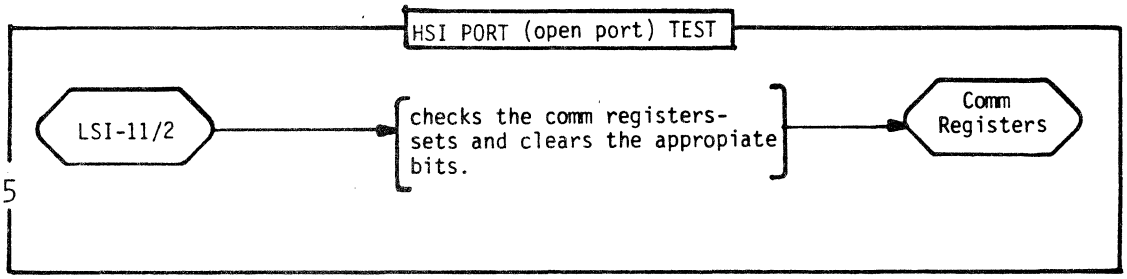


Fig. 4-21. Open port test.

6. RETRIEVE ERRORS (Fig. 4-22). If the HSI PORT test is executed alone, part 6 retrieves the error data from the system memory and displays it on the ODT terminal. If, however, the test is executed within the ALL series, the error information is displayed at the end of the series.

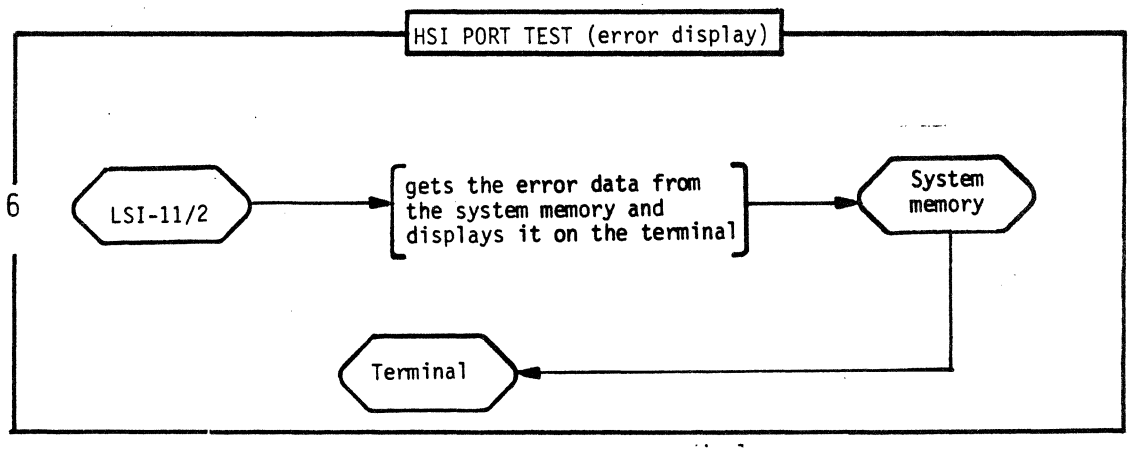


Fig. 4-22. HSI test error display.

DISC TEST NO. 7
Disc/Drive Test

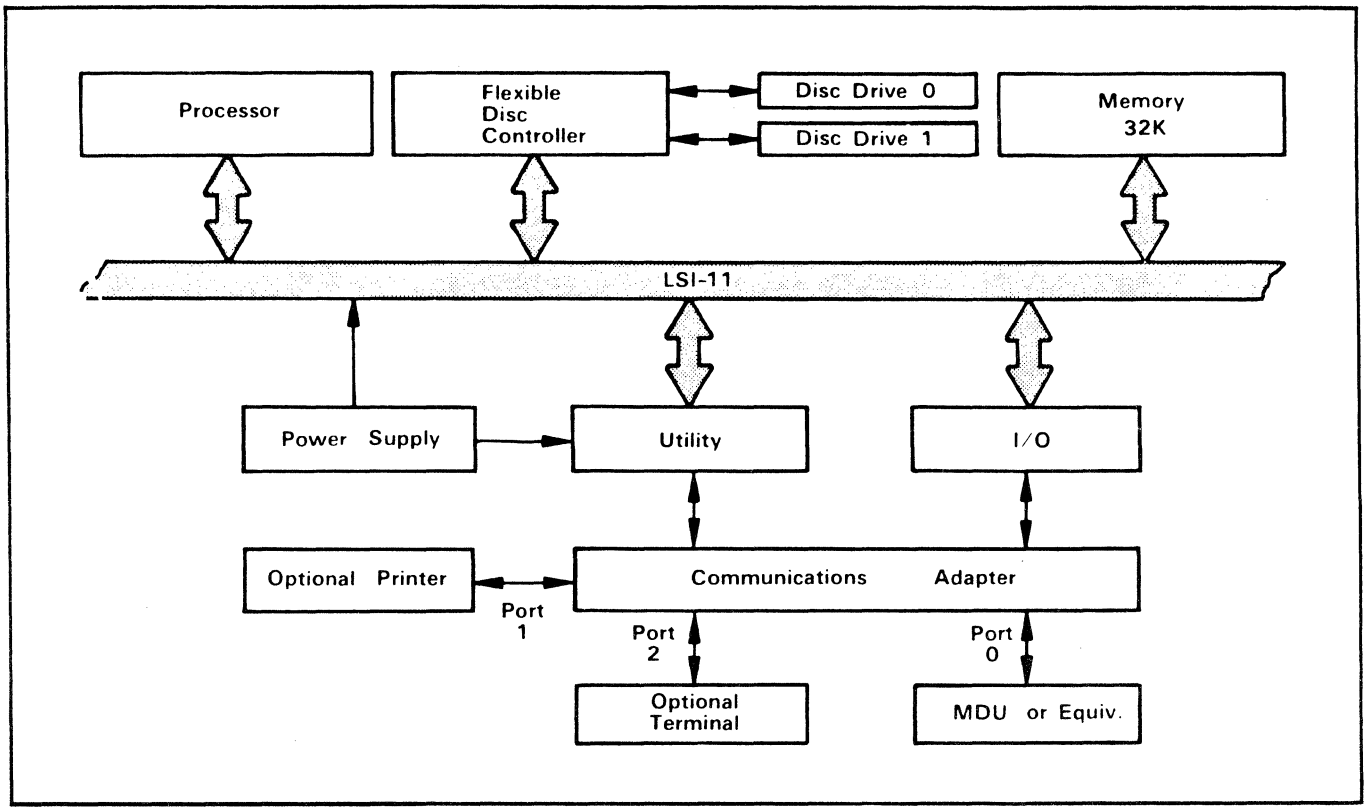


Fig. 4-23. 8501 block diagram.

TEST NAME: DISC/DRIVE test

RUN CODE: 7

FUNCTION: To check the operation of the FDC board and the disc drives

BLOCKS INVOLVED: LSI-11/2 Processor, Utility board, System memory, Disc Controller, Disc drive

ERROR MESSAGES:

WARNING BAD FDCBPR ON FDC BOARD
WARNING -- FLEXIBLE DISCS DO NOT RESPOND AT ADDRESS
MISSING INTERRUPTS:
FLEXIBLE DISC CONTROLLER BOARD
FLEXIBLE DISC N DISC TYPE:
-SIDE, -DENSITY (WRITE-PROTECTED)
IRRECOVERABLE ERRORS (**INDICATES LOCATION
RECOVERABLE ERRRORS ON ___ TRACKS,____ SIDE
RECOVERABLE SEEK ERRORS
RECOVERABLE READ ERRORS
WARNING -- CONTROLLER ERRORS
FLEXIBLE DISC REGISTERS
WARNING -- DISC TIME OUT

DESCRIPTION

1. TEST BOARD RESPONSE (Fig. 4-24). The DISC/DRIVE test checks if the Flexible Disc Controller (FDC) board will respond. If the test does not get a response, it stores an error in system memory and exits from the test.

2. SELECT DRIVE. The second step selects drive 0 as the drive and detetermines the drive status.

If the disc is write-protected, the test reads data at random from the disc. Upon finding an error, the test stores the error in the system memory.

For discs without write-protect status, the test formats the disc, writes at random locations, reads them back, and compares the written and read-back data. When the test finds an error, it stores the error data in system memory.

3. REPEAT FOR OTHER DRIVE. The DISC/DRIVE test repeats step 2 for disc drive 1.

4. RETRIEVE ERRORS. If the DISC/DRIVE test is executed alone, part 4 retrives the error data from the system memory and displays it on the ODT terminal. If, however, the test is executed in the ALL series, the error information is displayed at the end of the series.

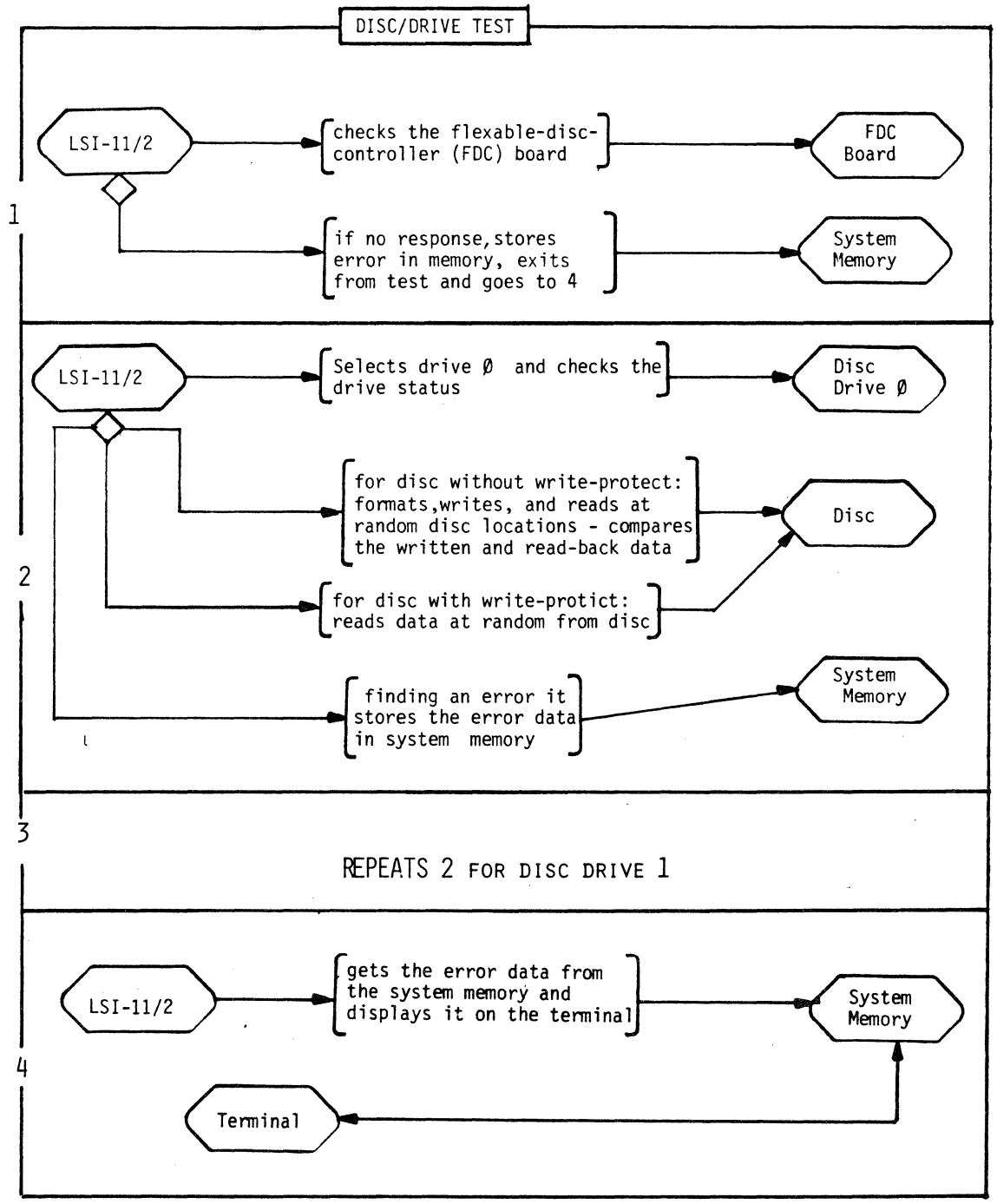


Fig. 4-24. Disc/Drive test.

ERROR MESSAGE SUMMARY

At the end of each test or the end of the ALL test series DIAGS identifies the errors with an appropiate message. DIAGS produces two different types of error messages:

- Messages printed just prior to the verification passed/failed message. Most of these are of the form:

  *** WARNING- NN X ERRORS
  PROBABLE SOURCE: Y BOARD

  Where NN is the number of errors, X is the type of error (eg. FLEXIBLE DISC ERROR), and Y is the name of the board.

- Messages printed after the verification passed/failed message. These messages include both error and system status messages.

The following pages summarize the 8501 error messages grouped according tests.

RAM Test Messages

***WARNING RAM ERRORS

A memory location that was written to by the RAM test did not read back the same data pattern. This message is usually accompanied by another message indicating the address, data expected, and data found. Incorrect top of RAM strapping also produces this error message.

TOP OF RAM NNNNNN

This message specifies the highest addressable RAM location. For an 8550 this should be 167776. If the address is different, the message is preceded by WARNING.

***WARNING -- RAM ERRORS IN RANGE NNNNNN TO NNNNNN
FAULT MASK = XXXXXX

Identifies where in memory a RAM error occurred. The message also indicates the differences in the bit pattern between the expected and the actual contents.

ROM Test Messages

***WARNING- PROM ERRORS

The utility board firmware either did not verify its checksums or it is obsolete. The guilty PROM (high byte and/or low byte) is indicated.

CPU Test Messages

***WARNING- PROCESSOR ERRORS

The LSI-11/2 failed the instruction set test.

Line-Time Clock Messages

***WARNING -- LINE-TIME CLOCK ERRORS

The power line frequency clock does not produce the interrupts at the correct intervals.

MISSING INTERRUPTS: LINE TIME CLOCK

The line frequency clock was ticking, but that no interrupts occurred. This may be due to a misplaced jumper on the processor board.

LINE-TIME FREQUENCY:NN HZ

N is the frequency at which the processor is receiving interrupts from the line frequency clock. The number should identical to the 8501 power source frequency.

LINE-TIME CLOCK STATUS: NNNNNN

This indicates cumulative contents of the LTC status register. Normally this will be 000340. For the Debugging Mode it is 000341.

AUXPORT Test Messages

XYZ DEVICE CONNECTED TO AUXPORT N

This message identifies what the diagnostics see at the port. NOTHING CONNECTED says that the DTR signal is missing.

REGISTERS FOR PORT AUX J151
BAUD RCSR RBUF XCSR XBUF

A status message showing the contents of the interface registers for auxiliary serial port N. BAUD indicates the strapped baud rate or ????. If a wrapback connector is attached, the strapped baud rate will be verified against the line clock. The RCSR and XCSR will contain the results of the last operation (or the first operation, if no errors occurred). The RBUF and XBUF are logically OR-ed from all bad operations.

PORT AUX J151 INPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

This means that no input was received on the PRINTER port. If no wrap-back connector was attached or if no characters were typed on a terminal at this port, this is not an error.

PORT AUX J152 INPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

This means that no input was received on AUXILIARY port. If no wrap-back connector was attached or if no characters were typed on a terminal at this port, this is not an error.

PORT AUX J151 OUTPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

This means that a not ready to transmit status persisted on the PRINTER port. If no wrap-back connector was attached or if the peripheral is off-line at this port. This is not an error.

PORT AUX J152 OUTPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

This means that a not ready to transmit status persisted on the AUXILIARY port. If no wrap-back connector was attached or if the peripheral is off-line at this port, this is not an error.

BAUD RATE FOR PORT AUX J151 NOT AS SHIPPED

This means that the baud rate for this port is not strapped to 2400 baud, as it was shipped. If the utility board was intentionally modified this way, this is not an error.

BAUD RATE FOR PORT AUX J152 NOT AS SHIPPED

The baud rate for this port is not strapped to 2400 baud, as it was shipped. If the utility board was intentionally modified this way, this is not an error.

PORT AUXN INPUT INTERRUPT NOT PRESENT
CHANNEL NOT FULLY TESTED

The input data was received from serial port N, but it was not accompanied by an interrupt. This may be due to incorrect vector jumpering.

PORT AUXN OUTPUT INTERRUPT NOT PRESENT
CHANNEL NOT FULLY TESTED

The output data could be sent from serial port N, but it was not accompanied by an interrupt. This may be due to incorrect vector jumpering.

LP MODE FOR PORT AUXN NOT AS SHIPPED

The line-printer strapping for the port is not the way it was manufactured. If the utility board was intentionally modified this way, this is not an error. (Normally, the PRINTER port is strapped for a line printer, and the AUXILIARY port is strapped for a terminal.)

NNNN DATA ERRORS

The data errors occurred during a transmission. The serial port N considered the data to be incorrect.

***WARNING- INCORRECT ADDRESS STRAPPING FOR PORT AUXN

The auxiliary serial port N does not respond at its standard address (177510 for AUX1, 177560 for AUX2).

HSIPORT Test Messages

REGISTERS FOR HSI
BAUD DMA CTR ADDR VEC RCSR RBUF XCSR XBUF

This is a status message showing the contents of the interface registers for the high speed interface. The BAUD catagory will either display 153.6K or *SLOW*. The DMA, CTR, ADDR, VEC, RCSR, and XCSR will contain the results of the last bad operation (exception: the high 7 bits of the DMA register are logically OR-ed from all bad operations. The RBUF and XBUF are logically OR-ed from all bad operations. If no errors occurred, the ADDR will contain the address of a data buffer and VEC will be 000374. The RCSR and the XCSR contain the intial channel status. All other registers will be 0.

BAUD RATE FOR HSI NOT AS SHIPPED

The baud rate for the high speed interface is not set to 153.6 Kbaud. This is probably due to accidentally moving the slide switch on the back of the 8501.

***WARNING- HSI CONTROL-DMA ERRORS

The control and or DMA circuitry (on I/O board) does not respond as expected.

XYZ DEVICE CONNECTED TO HSI

This message indentifies what the diagnostics see at the HSI port. A NOTHING CONNECTED message identifies a missing DTR signal.

HSI OUTPUT INTERRUPT NOT PRESENT - CHANNEL NOT FULLY TESTED

The HSI controller was able to transmit data, but that a transmit ready interrupt did not occur.

HSI OUTPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

The HSI did not receive a ready to transmit status, and therefore could not transmit.

HSI INPUT INTERRUPT NOT PRESENT - CHANNEL NOT FULLY TESTED

The HSI received data, but that the data was not accompanied by an interrupt. This may be due to incorrect vector jumpering on the I/O board.

HSI INPUT NOT PRESENT - CHANNEL NOT FULLY TESTED

The HSI did not receive any data. If no wrapback connector or 8301 was connected to the port, this is not an error.

NNNN DATA ERRORS

The HSI received data that the program considered to be invalid.

HSI DMA INTERRUPT NOT PRESENT - CHANNEL NOT FULLY TESTED

The HSI attempted to perform DMA transfers, but that the transfers were not accompanied by a DMA operation complete interrupt.

***WARNING- INCORRECT ADDRESS STRAPPING FOR HSI

This indicates that the high speed interface does not respond at its standard address (176510 octal).

<8301 RESTARTED>

This message is displayed in Debugging Mode every time the 8301 is restarted.

NNNN DOS/50 COMMUNICATION ERRORS OF TYPE NN

This message appears when the software protocol used by the 8301 and 8501 to talk to each other has been violated. Unless the number of errors is high, ignore this message. For those rare cases that require deciphering of the error codes, the codes for the different error types are given below:

1	number of retrived transmissions
2	high speed interface not ready
4,5,6	timeout, waiting for the 8301 to send data
7,8,9	invalid header received from the 8301
10	parity error
11	framing error
12	overrun error
13,14	invalid data block from 8301
15	timeout, waiting fo for the 8301 to send data
16	8301 and 8501 trying to send simultaneously
18,20	garbage received from 8301
21	message out of sequence
22	invalid header
23	8301 sending too many messages
24	invalid header received from 8301
25	number of 8501 messages refused by 8301

Disc/Drive Test Errors

***WARNING- FLEXIBLE DISCS DO NOT RESPOND AT ADDRESS

The flexible discs do not respond at 177160 octal.

***WARNING- BAD FDCBPR ON FLEX CONTROLLER BOARD

The data written to the interface register was not read back correctly.

MISSING INTERRUPTS: FLEXIBLE DISC CONTROLLER BOARD

The operations performed used the flexible disc controller, but that the operations were not accompanied by an operation complete interrupt.

FLEXIBLE DISC N DISC TYPE: -SIDED, -DENSITY (,WRITE-PROTECTED)

Indicates the type of disc is in drive N.

IRRECOVERABLE ERRORS (** INDICATES LOCATION)

If errors occurred on drive N that persisted in spite of retries, this message will be displayed.

RECOVERABLE ERRORS ON INNER TRACKS: OUTER TRACKS:
RECOVERABLE ERRORS ON SIDE 0: SIDE 1:

Indicates where on the disc the errors occurred (if any). Inner tracks are 0-42, outer are 43-76. Unless this message is preceded by the IRRECOVERABLE ERRORS message, it can be treated as a status message. Recoverable errors are errors in which the data was recovered on a retry.

RECOVERABLE SEEK ERRORS: READ ERRORS:

This message indicates whether any errors detected were due to difficulty in locating the data, or in the data itself.

***WARNING- CONTROLLER ERRORS

This message indicates that controller type errors (as opposed to drive-type errors) occurred on the flexible disc controller board.

FLEXIBLE DISC REGISTERS
FDCBPR FDCR FDWCR FDDAR FDDMAR FDER FDSR FDDR

This message is a status message, indicating cumulative results of interface registers pertaining to disc drive N. The FDCBPR shows the current contents of the FDCBPR. The FDCR, FDWCR, FDDAR, and FDDMAR only show the results of the last bad operation (exception: bit 15 of the FDCR is used as a software flag and is only cleared if the flex controller took too long to respond to a command). The FDER, FDSR, and FDDR show accumulated results from all bad operations, that is, a logical OR (exception: bit 15 of the FDER is used as a software flag for any serious error condition. It can be set by software- detected errors as well as flex controller- detected errors). If no errors occurred, the FDCBPR will show its current contents, the FDCR will contain 100000, and the FDDMAR will contain the address of a data buffer. All other registers will be 0.

***WARNING- DISC TIME OUT

This indicates that the flex controller did not respond to a command within a reasonable length of time (2 minutes).

Miscellaneous Error Messages

??? DON'T UNDERSTAND ->

This message appears following a typing mistake by the user. The program does not know what you meant by the word pointed to. Type an H for information about commands.

INTERRUPTS TOO FREQUENT TO PROCESS

A stack overflow was detected during an interrupt routine. The test in progress will be aborted and the diagnostics will be re-initialized.

***WARNING--BUS ERRORS

A device dos not answer on the bus at its expected address. This message is usually accompanied by another message concerning the device in question.

***WARNING INTERRUPT ERRORS

Interrupts occur at a vector or sequence that are not normal. This message is usually accompanied by another message indicating the interrupt vector address.

***WARNING-- HIGH SPEED INTERFACE ERRORS

A high speed serial channel did not pass the test. This message is usually accompanied by others describing the nature of the apparent failure.

***WARNING -- AUX PORT 1 ERRORS

The PRINTER port did not pass the test. This message is usually accompanied by others describing the nature of the apparent failure.

***WARNING -- AUX PORT 2 ERRORS

The AUXILIARY port did not pass the test. This message is usually accompanied by others describing the nature of the apparent failure

***WARNING -- FLEXIBLE DISC ERRORS

One or more flexible disc drives did not pass the test. This message is usually accompanied by others describing the nature of the apparent failure.

UNEXPECTED INTERRUPT VECTORED AT NNNNNN

An unsheduled interrupt occurred at vector NNN NNN. This error may be caused by incorrect strapping on a board.

UTILITY BOARD PROM PART NUMBERS: 160-NNNN-NN, 160-NNNN-NN

This message indicates the installed firmaware version. The first number is the number of the low byte ROM. The second number is the number of the high byte ROM.

***WARNING -- OBSOLETE FIRMWARE

This message follows the Utility board part numbers - it indicates that the firmware is obsolete. If it follows the flexible disc version number it indicates the flexible disc controller firmware is obsolete.

LED Error Summary

The disc-based diagnostics also use the five Utility board LEDs to display error information. (For more information on the LED error displays see Section 3, The Utility Board LEDs). A short summary of the error codes follows:

00 DIAGS was started but hang up almost instantly for unknown reasons

01 DIAGS started initializing the system and hung up in the process.

03 DIAGS was started by an 8301 command, but the 8501 did not receive the instructions of what operating mode to assume. Try starting over.

03 DIAGS is waiting for an I/O device to become ready. In the stand-alone service mode, it is waiting on the AUXILIARY port. In the DOS/50 customer mode DIAGS is trying to send a message via the high speed interface port.

04 The initialization is complete and DIAGS trys to display the first menu either via the AUXILIARY port or the HSI port.

05 The menu is printed and DIAGS waits for the user to answer prompts.

06 DIAGS gotten the answer to the prompts and continued to perform another task.

Section 5

FUNCTIONAL PROCEDURES

INTRODUCTION

This section provides a group of functional procedures to illustrate 8501 system interaction. The intent is to provide an additional tool toward fault isolation at the board level.

This section contains the following procedures:

Procedure 1 Front panel RESTART or DC power ON.

Procedure 2 8501 file access.

Procedure 3 Write to flexible disc.

Procedure 4 Write to PRINTER port.

HOW TO USE THE FUNCTIONAL PROCEDURES

Each functional procedure includes a block diagram, a flow diagram, and a description that supports the abbreviated flow diagram comments. Figure 5-1 is an example of the flow diagram format.

The functional procedures in this section represent the overall functions performed within the 8501. These procedures are provided to give you a better understanding of the interrelated actions that take place during specific operations.

It is important to remember limitations of the functional procedures. They provide general views of system interactions, but do not attempt to isolate error conditions due to software or timing errors. Other sections within this Service Manual provide in-depth information on the hardware within the 8501. Software information can be found in the appropriate system user's manual.

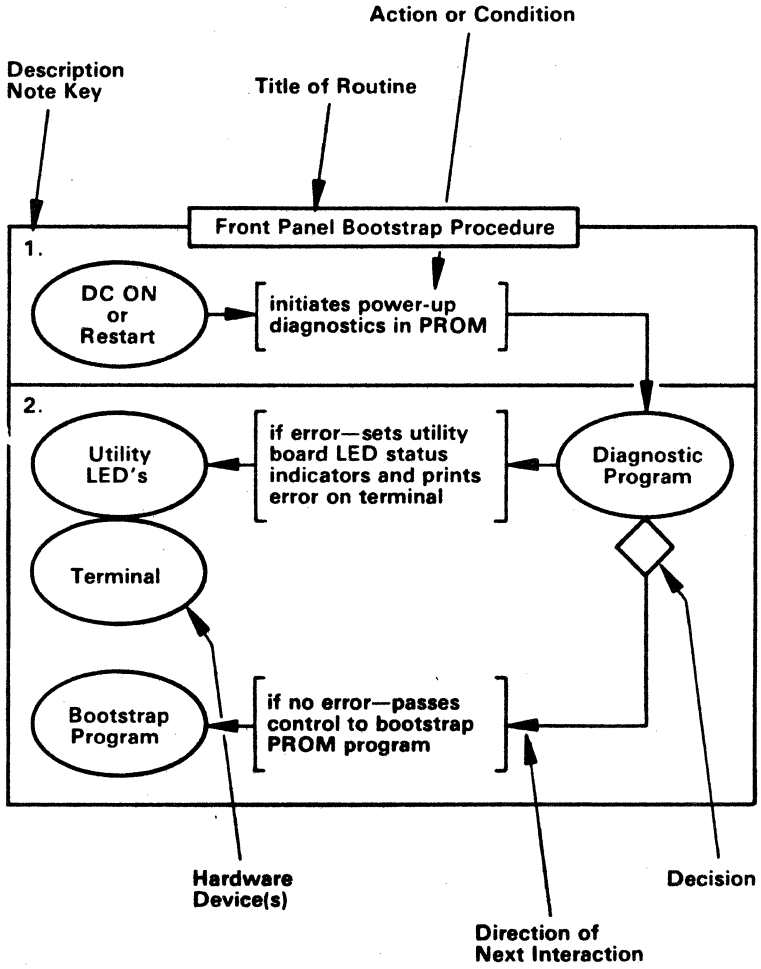


Fig. 5-1. Sample of modified flow diagram.

A small diamond leaving a hardware device block indicates a decision. If the action described in the brackets is true, the action is transferred in the direction of the arrow.

FUNCTIONAL PROCEDURE NO. 1

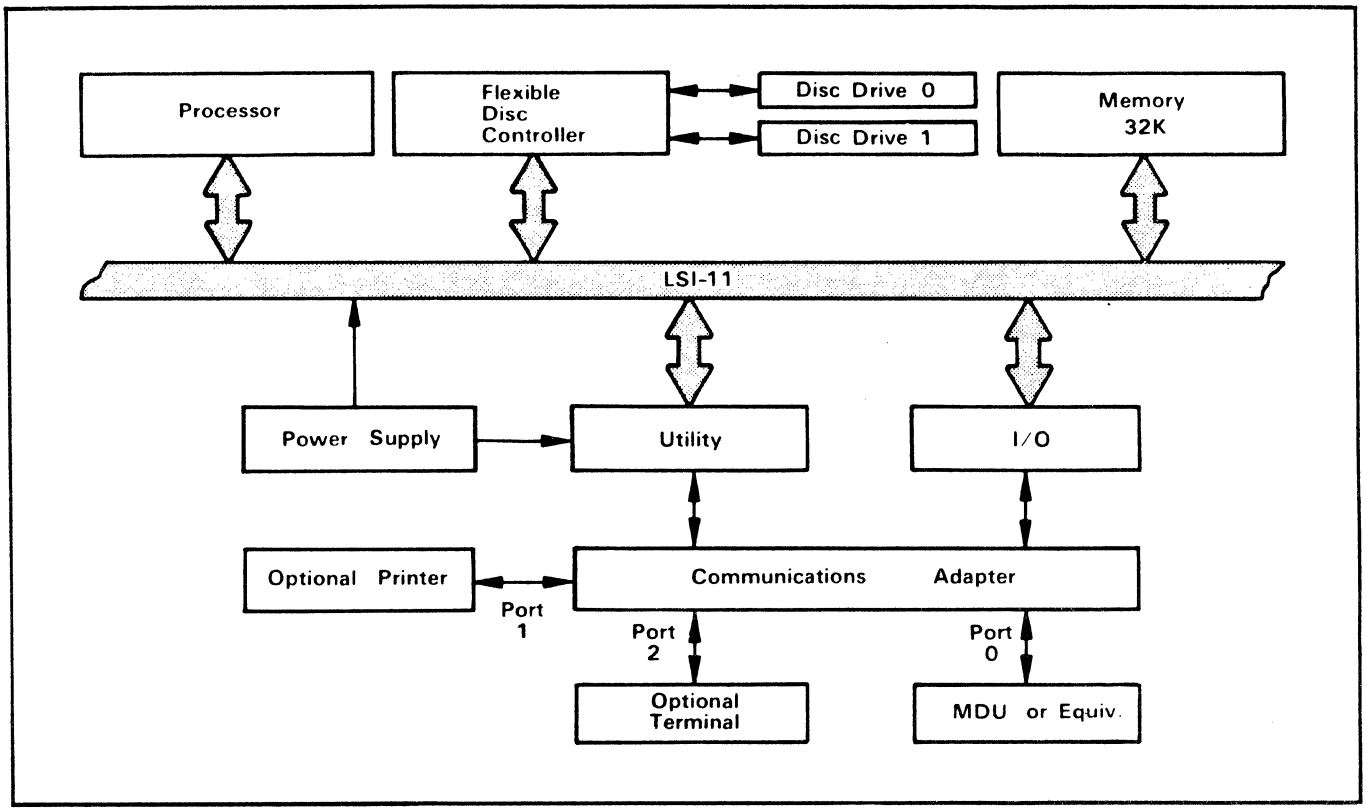


Fig. 5-2. 8501 block diagram..

PROCEDURE

Restarting the 8501 From the Front Panel.

FUNCTION

This procedure describes the sequence of actions that occur when the 8501 front panel DC ON switch is pressed, or if the RESTART switch is toggled.

BLOCKS INVOLVED

All

Description

1. When the DC ON switch is activated, or when the front panel RESTART switch is pressed, the LSI-11/2 begins execution of the diagnostics PROM program (address 173000 on the Utility board).

2. The diagnostics run automatically following normal power-up delays (total elapsed time <5 seconds). If an error is found, the diagnostics cause the LSI-11/2 to write an error code to the Utility board diagnostic LED's (and to a terminal if connected to AUXILIARY port at address 177560). If no error is found the diagnostics set bit 5 of the Line-Time Clock (LTC) register to 0, thereby passing control to the Bootstrap PROM program.

3. The Utility board uses DMA request protocol to request the bus for the PROM bootstrap program. The request is made via the Utility board front panel control logic. The request is granted if and when the DCOK signal is received from the Utility board power-up circuit.

4. On granting the bus, the boot PROM routine causes the LSI-11/2 to address the Control Buffer in memory, and through it, instruct the Flexible Disc Controller to perform a DMA read from the first data word on the disc.

5. The Flexible Disc Controller interprets the Control Buffer in memory and loads the Controller's Z80A registers with instructions to read the first data word occurring in the data field of track 0, record 0. This is read into the bottom of memory (0 --- 127).

6. The bootstrap program checks the first word to see if it is a NOP (260). If not, it will check the other disc drive before registering a non-bootable disc (error routine). If the bootstrap program finds a NOP, it will read the next block of data on the disc and carry out the instructions contained there.

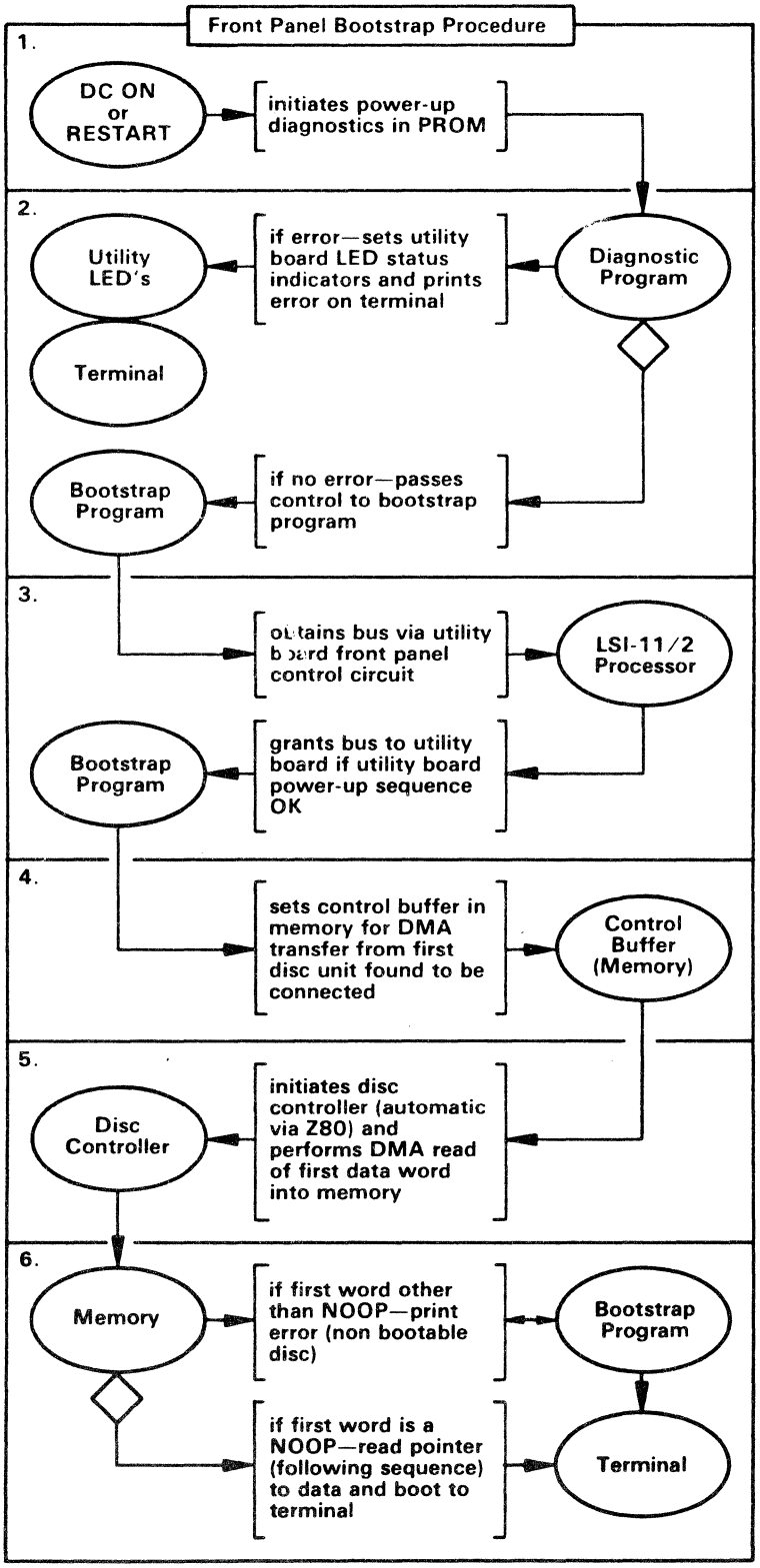


Fig. 5-3. Front panel Bootstrap flow diagram.

FUNCTIONAL PROCEDURE NO. 2

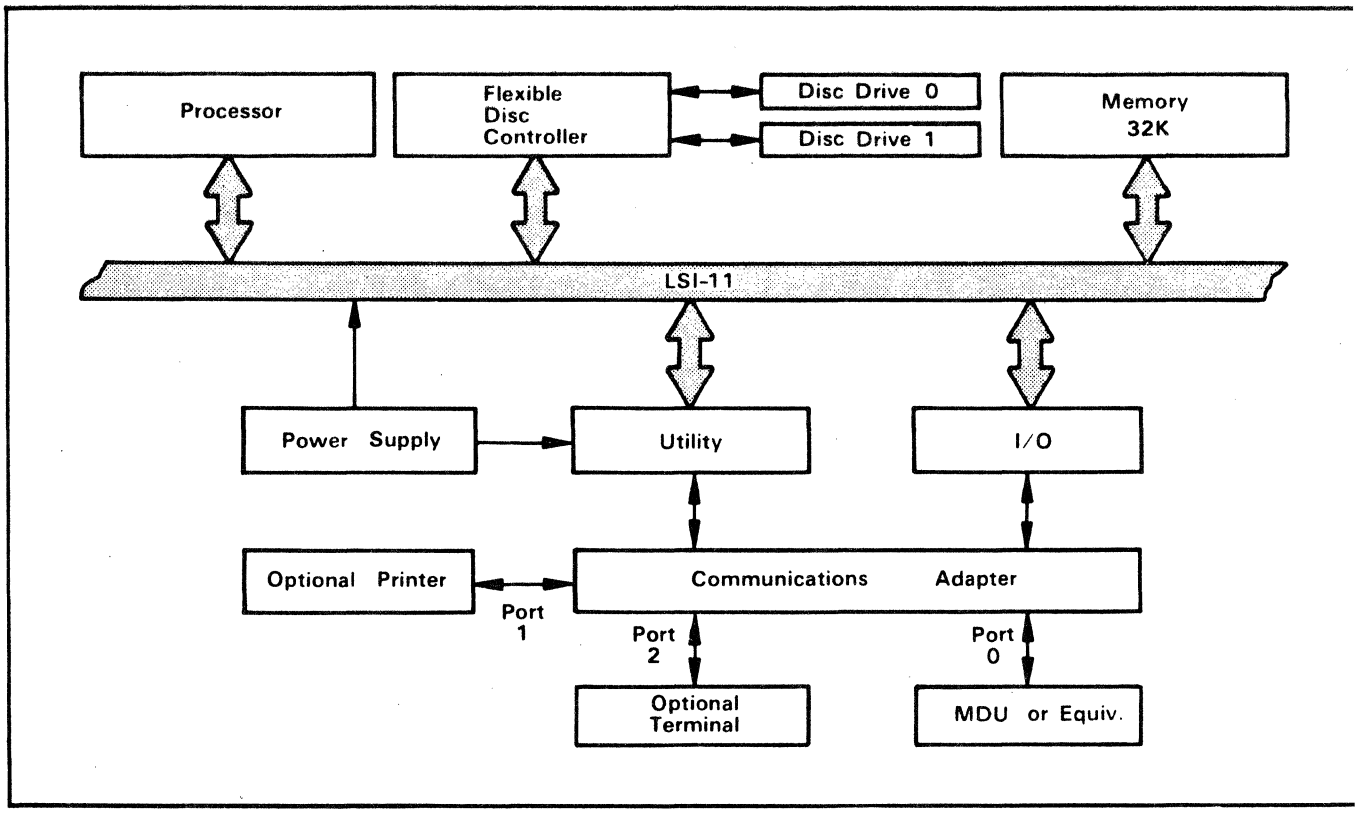


Fig. 5-4. 8501 block diagram.

PROCEDURE

8501 file access.

FUNCTION

This procedure describes the actions required when the 8501 is requested to access a flexible disc file.

BLOCKS INVOLVED

Communications Adapter, I/O Board, LSI-11/2, Flexible Disc Controller

Description

Receiving Start of Header (Fig. 5-5)

1. The unit attached to the 8501 HSI port sends the ASCII Start of Header (SOH) when the Clear To Send (CTS) line is high.

2. The SOH character is received by the I/O board (via the Comm Adapter). The I/O board then issues an interrupt request (vector 360) to the LSI-11/2 processor.

3. The processor acknowledges the interrupt request and passes the SOH character to the High-Speed Interface (HSI) program in system memory.

4. The HSI program checks the start of header for validity and sets up the DMA register on the I/O board to receive the remainder of the header (seven characters) under DMA.

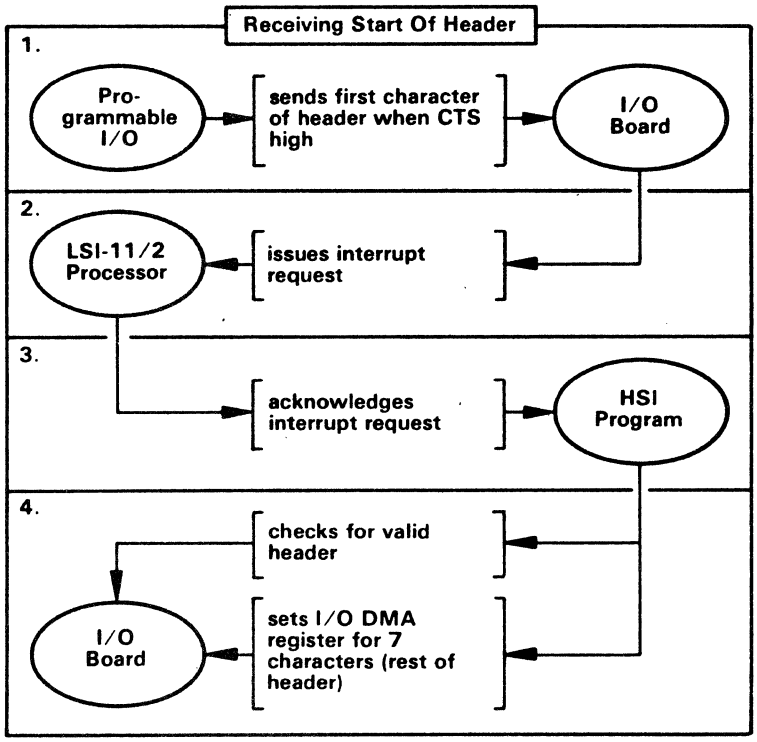


Fig. 5-5. Receive SOH .

Programming DMA Transfer (Fig. 5-6)

1. The I/O board requests a DMA interrupt from the LSI-11/2 processor. When the grant is received, the I/O board checks for Data Set Ready (DSR) high, and acknowledges the valid SOH with ASCII character ACK.

2. When CTS is high, the remaining six characters are transmitted directly to the HSI program in memory (via the Comm Adapter and I/O boards). The HSI program checks the header and set up the DMA register on the I/O board for the number of data words specified in the header.

3. The I/O board sets CTS low and waits for DTR high. The I/O board then sends an ACK to the HSI port.

4. The unit connected to the HSI port then sends its file request under DMA. The data block is surrounded by the framing characters STX (Start Of Transmission), and ETX (End Of Transmission).

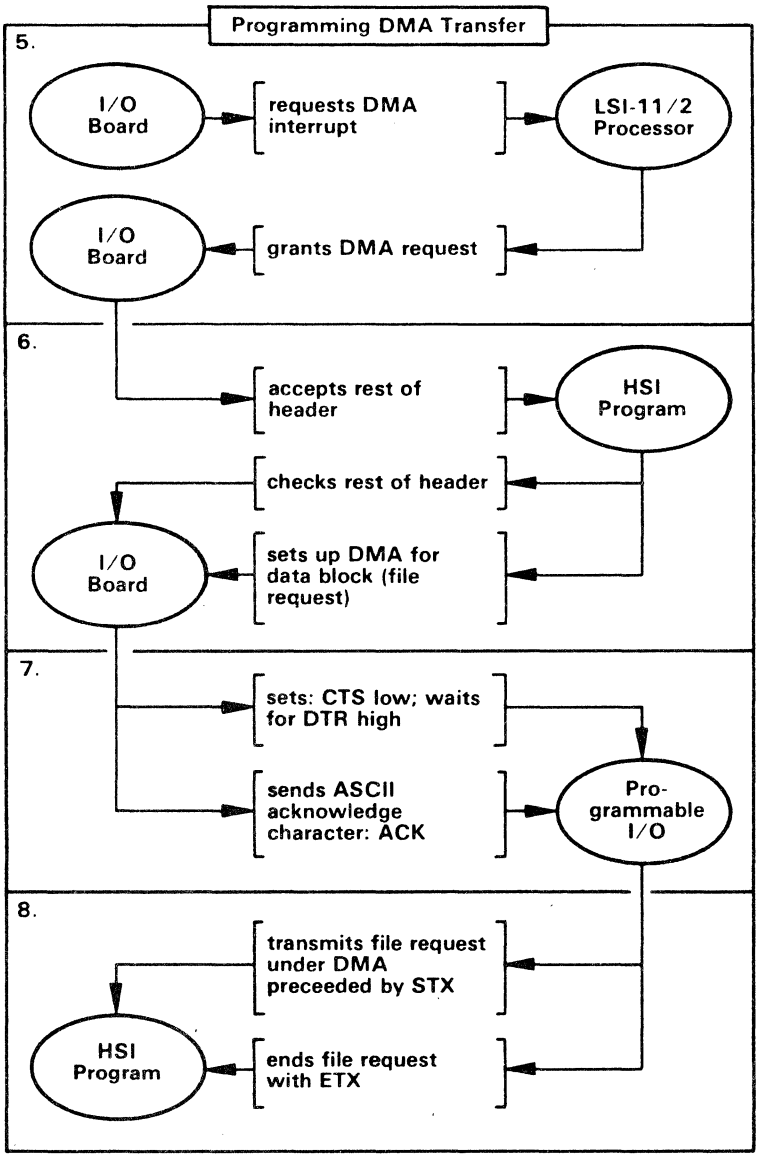


Fig. 5-6. Programming DMA transfer.

File Access Operation (Fig. 5-7)

1. The HSI program checks the parity and length of data (after temporarily loading the data in another part of memory). The HSI program then passes control to the file manager program.

2. The file manager reads the data, accesses the requested file (from disc or memory), then executes the task and/or acknowledges completion of the requested routine.

3. Upon task completion by the file manager, the HSI program repeats the header routine and sets up the I/O board for DMA transfer of the file or completion acknowledgement to the unit connected to the HSI port.

4. The I/O board sends the information (file, acknowledge, or task result) to the unit connected to the HSI port.

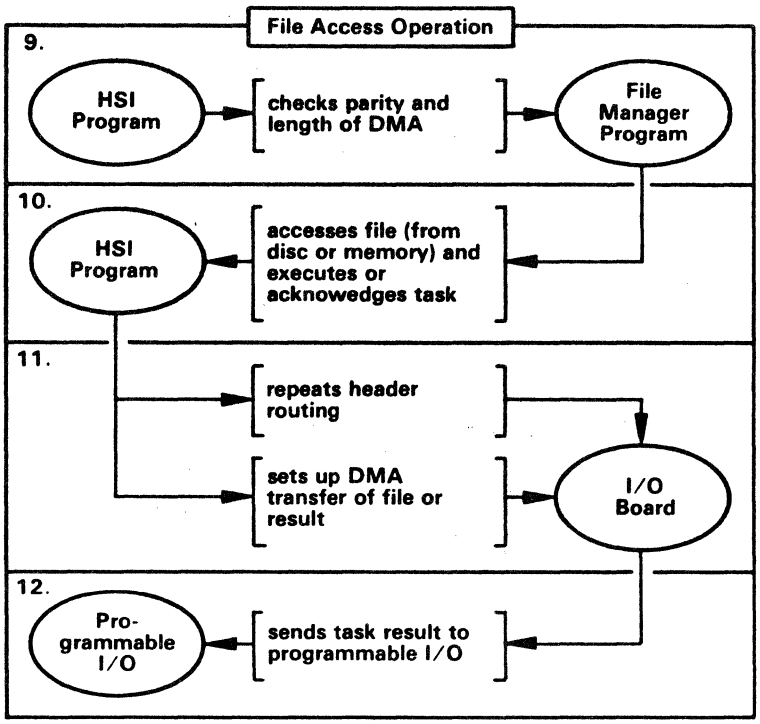


Fig. 5-7. File access.

FUNCTIONAL PROCEDURE NO. 3

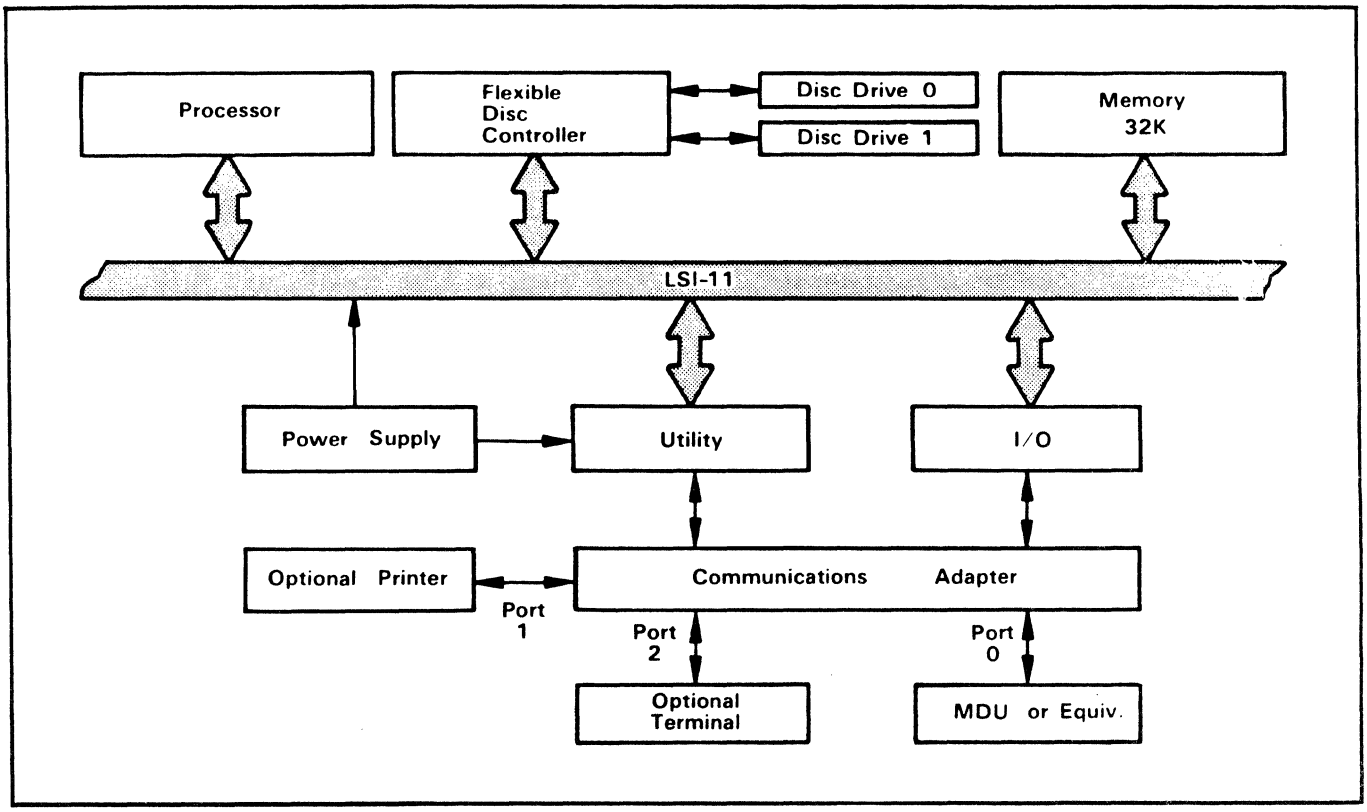


Fig. 5-8. 8501 block diagram.

PROCEDURE

Writing to the 8501 Flexible Disc

FUNCTION

This procedure describes the actions that occur when the LSI-11/2 writes data to the Flexible Disc Drive. This procedure assumes that the 8501 is operating on a stand-alone basis, and that a terminal is connected to the AUXILIARY port on the 8501 rear panel.

BLOCKS INVOLVED

LSI-11/2, Flexible Disc Controller, Utility board, Communications Adapter

Description

1. When the terminal accesses the 8501, the LSI-11/2 processor is interrupted by the Utility board via the auxiliary interrupt (vector 60).

2. The LSI-11/2 processor routs the terminal data (character by character) to the file management program in memory.

3. The file management program partitions memory according to file or block size, and sets up the memory Control Buffer with the size and attributes of the DMA transfer. The writing of the Control Buffer automatically causes the Flexible Disc Controller to address memory.

4. The Flexible Disc Controller reads the Control Buffer and translates the buffer contents into Z80 readable register format. The data is then read directly to the disc (i.e. from memory to the disc).

5. On job completion the Flexible Disc Controller writes the Control Buffer, and interrupts the LSI-11/2 processor (vector 230) if programmed to do so by bit 14 of the Flexible Disc Command Register (FDCR).

6. Steps 1 through 5 are repeated as necessary.

7. The file management program interrupts the terminal via the processor; Utility Board and Comm Adapter, and outputs the job completion acknowledgement and file status.

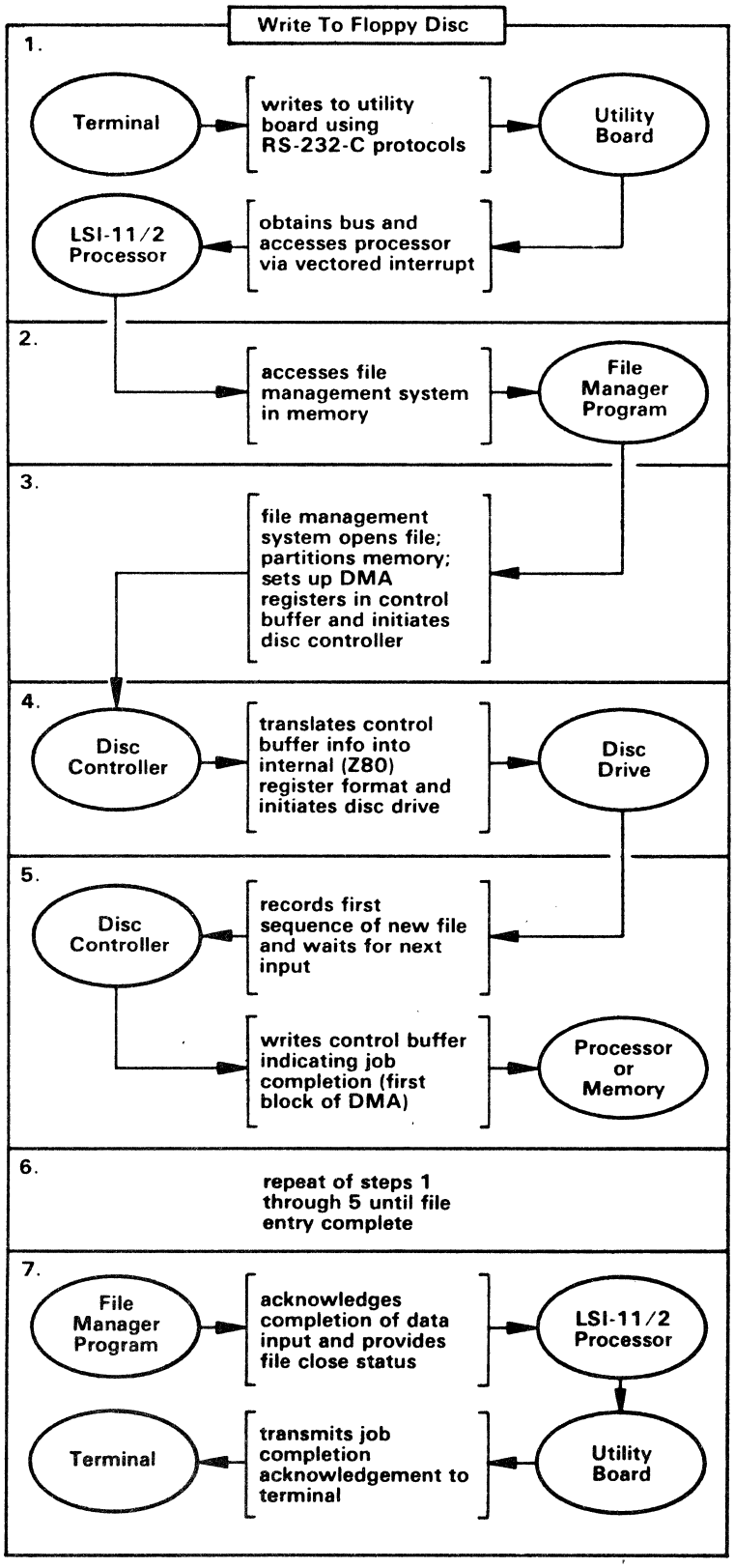


Fig. 5-9. Write to Flexible Disc.

FUNCTIONAL PROCEDURE NO. 4

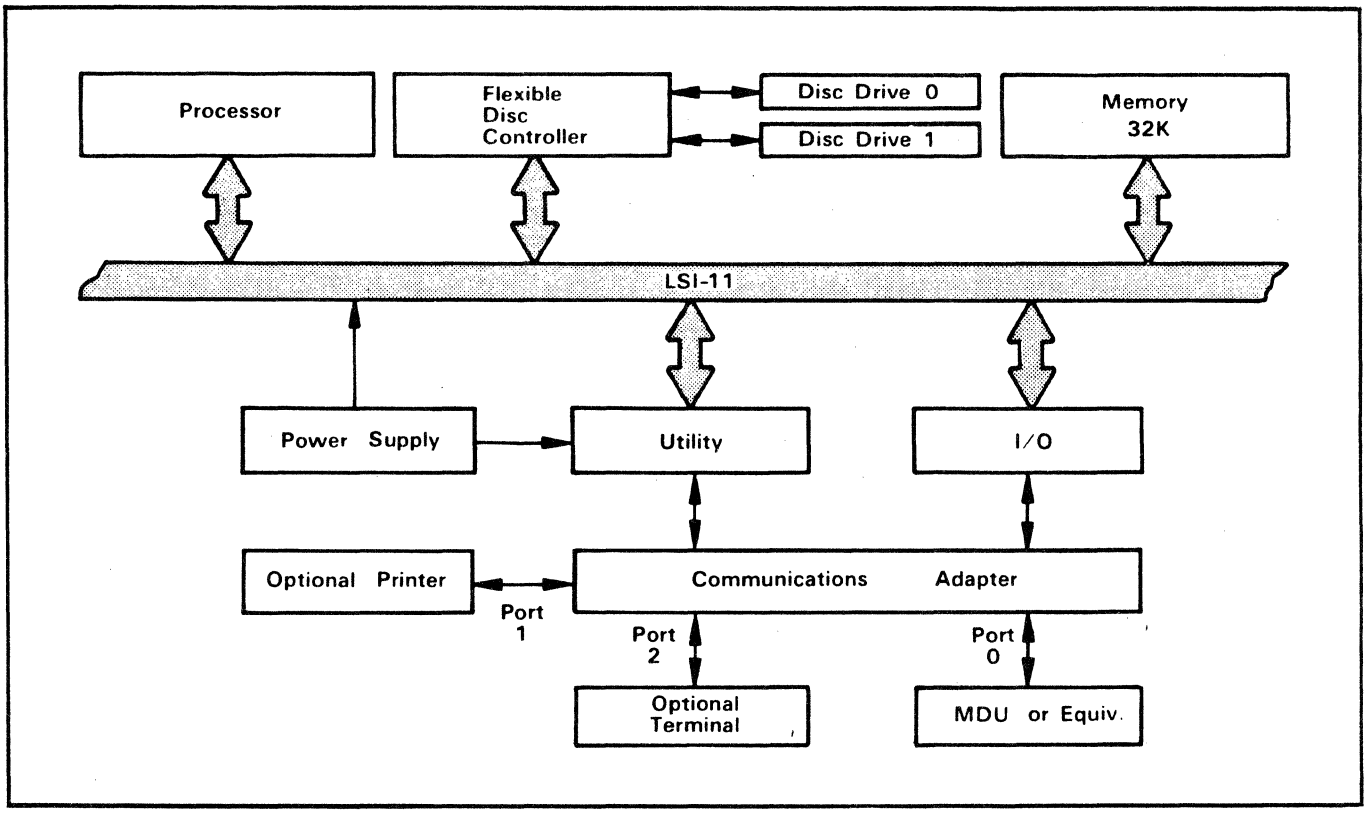


Fig. 5-10. 8501 block diagram.

PROCEDURE

Write to PRINTER Port.

FUNCTION

This procedure describes the actions that occur when the LSI-11/2 writes data to the 8501 PRINTER port. The write to the PRINTER port is activated by a command from a terminal connected to the AUXILIARY port.

BLOCKS INVOLVED

LSI-11/2, Utility Board, Communcations Adapter

Description

1. The terminal accesses the Utility board via the Comm Adapter. The Utility board interrupts the LSI-11/2 (auxiliary interrupt -- vector 60).

2. The LSI-11/2 processor uses the file management program to read the terminal data from memory.

3. The LSI-11/2 processor routs each character to the printer via the Utility board and Comm Adapter.

4. Steps 1 through 3 are repeated until all characters have been transmitted.

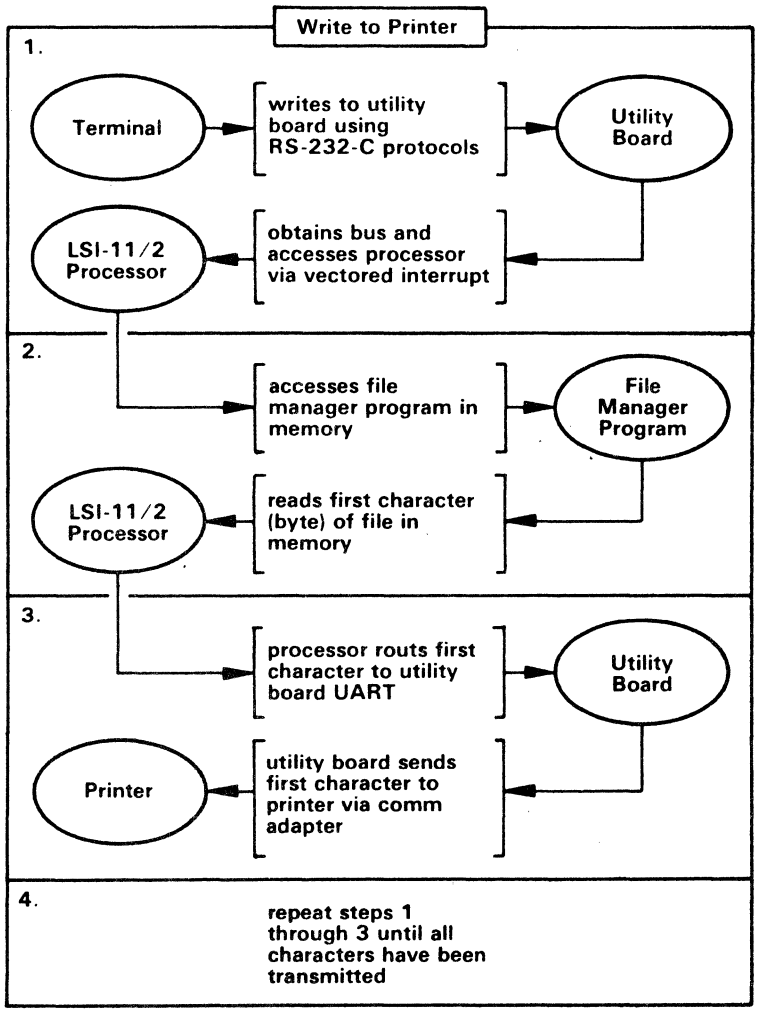


Fig. 5-11. Write to printer.

Section 6

SPECIFICATIONS

INTRODUCTION

This section provides general specifications and related information for the 8501 Data Management Unit. The following information is presented in this section:

- Electrical Characteristics
- Environmental Characteristics
- Physical Characteristics
- Processor Interface
- Port Characteristics
- ASCII Code Chart

CHARACTERISTICS

Electrical Characteristics

Power Requirements

115 V Nominal (90 - 127 VRMS)
or
230 V Nominal (180 - 250 VRMS)

Line Frequency Range: 50 Hz +1% or 60 Hz +1%

Power Consumption

385 Watts Max.

Environmental Characteristics

Temperature	
Operating	10 C to 40 C
Storage	-10 C to +45 C
Humdity	
Operating	20% to 80% (non-condensing)
Storage	8% to 80% (non-condensing)
Altitude	
Operating	2 500 (0 to 8,000 ft.) Derate maximum temperature by 1 deg. C for each 300 m above 2 400 m
Storage	15 200 m (0 to 50,000 ft.)

Physical Characteristics

Height	267 mm	(10.5 inches)
Width	427 mm	(16.8 inches)
Length	597 mm	(23.5 inches)
Weight	25 kg	(55 lbs.)

PROCESSOR INTERFACE

This sub-section details the interface connections made between the LSI-11/2 processor board and the 8501 Data Management Unit. Table 6-1 lists the LSI-11/2 signals used within the 8501, and their connection points on the 8501 main interconnect board.

Table 6-2 provides a list of all the bus mnemonies used in the 8501 and gives a description of the use of each signal. Figure 6-1 shows the relationship between the LSI-11/2 72-pin edge connector, and the 8501 100-pin bus.

Table 6-1
M7270 Module Backplane Pin Utilization

Side 1 (Component Side)

Backplane Pin	M7270 Signal Function	LSI-11 Bus Signal Name
AA1	Bus terminator	BIRQ5L
AB1	Bus terminator	BIRQ6L
AC1	Bus terminator	BDAL16L
AD1	Bus terminator	BDAL17L
AE1	STOP L	SSPARE1
AF1	SRUN L	SSPARE2
AH1	SRUN L	SSPARE3
AJ1	GND	GND
AK1	MTOE L	MSPAREA
AL1	GND	MSPAREA
AM1	GND	GND
AN1	BDMR L	BDMR L
AP1	BHALT L	BHALT L
AR1	Bus terminator	BREF L
AS1	Not Connected	+12B
AT1	GND	GND
AU1	Not Connected	PSPARE1
AV1	Not Connected	+5B
BA1	BDCOK H	BDCOK H
BB1	BPOK H	BPOK H
BC1	SCLK3 H	SSPARE4
BD1	SWMIB18 H	SSPARE5
BE1	SWMIB19 H	SSPARE6
BF1	SWMIB20 H	SSPARE7
BH1	SWMIB21 H	SSPARE8
BJ1	GND	
BK1	Not Connected	MSPAREB
BL1	Not Connected	MSPAREB
BM1	GND	
BN1	BSACK L	BSACK L
BP1	Bus terminator	BIRQ7L
BR1	BEVNT L	BEVNT L
BS1	Not Connected	+12B
BT1	GND	GND
BU1	Not Connected	PSPARE2
BV1	+5 V	+5 V

Table 6-1
M7270 Module Backplane Pin Utilization (Cont)

Side 2 (Solder Side)

Backplane Pin	M7270 Signal Function	LSI-11 Bus Signal Name
AA2	+5 V	+5 V
AB2	Not Connected	-12 V
AC2	GND	GND
AD2	+12 V	+12 V
AE2	BDOUT L	BDOUT L
AF2	BRPLY L	BRPLY L
AH2	BDIN L	BDIN L
AJ2	BSYNC L	BSYNC L
AK2	BWTBT L	BWTBT L
AL2	BIRQ L	BIRQ L
AM2	Not Connected	BIAKI L
AN2	BIAKO L	BIAKO L
AP2	BBS7 L	BBS7 L
AR2	Not Connected	BDMGI L
AS2	BDMGO L	BDMGO L
AT2	BINIT L	BINIT L
AU2	BDALO L	BDALO L
AV2	BDAL1 L	BDAL1 L
BA2	+5 V	+5 V
BB2	Not Connected	-12 V
BC2	GND	GND
BD2	+12 V	+12 V
BE2	BDAL2 L	BDAL2 L
BF2	BDAL3 L	BDAL3 L
BH2	BDAL4 L	BDAL4 L
BJ2	BDAL5 L	BDAL5 L
BK2	BDAL6 L	BDAL6 L
BL2	BDAL7 L	BDAL7 L
BM2	BDAL8 L	BDAL8 L
BN2	BDAL9 L	BDAL9 L
BP2	BDAL10 L	BDAL10 L
BR2	BDAL11 L	BDAL11 L
BS2	BDAL12 L	BDAL12 L
BT2	BDAL13 L	BDAL13 L
BU2	BDAL14 L	BDAL14 L
BV2	BDAL15 L	BDAL15 L

Table 6-2
Bus Mnemonics

Mnemonic	Description
BSPARE1 BSPARE2	Bus Spare (Not Assigned, Reserved for DIGITAL use.)
BAD16 BAD17	Extended address bits (not implemented)
GND	Ground--System signal ground and dc return.
BDMRL	Direct Memory Access (DMA) Request--A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
BHALT L	Processor Halt--When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the processor module is removed) and DMA request/grant sequences are enabled. When in the halt state, the processor executes the ODT microcode and the console device operation is invoked.
BREF L	Memory Refresh--Asserted by a processor microcode generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC L/BDIN L bus transaction.
BDCOK H	DC Power OK--Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BPOK H	Power OK--Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.

Table 6-2
Bus Mnemonics (Cont)

Mnemonic	Description
BSPARE6	Bus Spare (Not assigned. Reserved for DIGITIAL use.)
BEVNT L	External Event Interrupt Request--When asserted, the processor responds (if PS bit 7 is 00 by entering a service routine via vector address 100 (octal). A typical use of this is a line time clock interrupt.
PSPARE4	Spare (Not assigned).
PSPARE2	Spare (Not assigned).
+5	+5 V Power--Normal +5 V dc system power.
+5	+5 V Power--Normal +5 V dc system power.
-12	-12 V Power--12 V dc power for devices requiring this voltage.
+12	+12 V Power--+12 V dc system power.
BDOUT L	Data Output--BDOUT, when asserted, implies that valid data is available on BDALO-15 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
BRPLY L	Reply--BRPLY is asserted in response to BDIN L or BDOUT L and during 1AK transaction. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
BDIN L	Data Input--BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring.

Table 6-2
Bus Mnemonics (Cont)

Mnemonic	Description
BSYNC L	Synchronize--BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL0--15. The transfer is in process until BSYNC L is negated.
BWTBT L	Write/BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
BIRQ L	Interrupt Request--A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output--This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin.
BBS7 L	Bank 7 Select--The bus master asserts BBS7 L when an address in the upper 4K bank (address in the 28-32K range) is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.

Table 6-2
Bus Mnemonics (Cont)

Mnemonic	Description
BDMGI L BDMGO L	DMA Grant-input and DMA Grant Output--This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DAM device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negative BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle.
BINIT L	Initialize--BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).
BDALO L BDALI L	Data/Address Lines--These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.
+5	+5 V Power--Normal +5 V dc system power.
-12	-12 V Power-- -12 V dc power for devices requiring this voltage.
+12	+12 V Power-- +12 V system power.
BDAL2 L BDAL3 L BDAL4 L BDAL5 L BDAL6 L BDAL7 L BDAL8 L BDAL9 L BDAL10 L BDAL11 L BDAL12 L BDAL13 L BDAL14 L BDAL15 L	Data Address Lines.

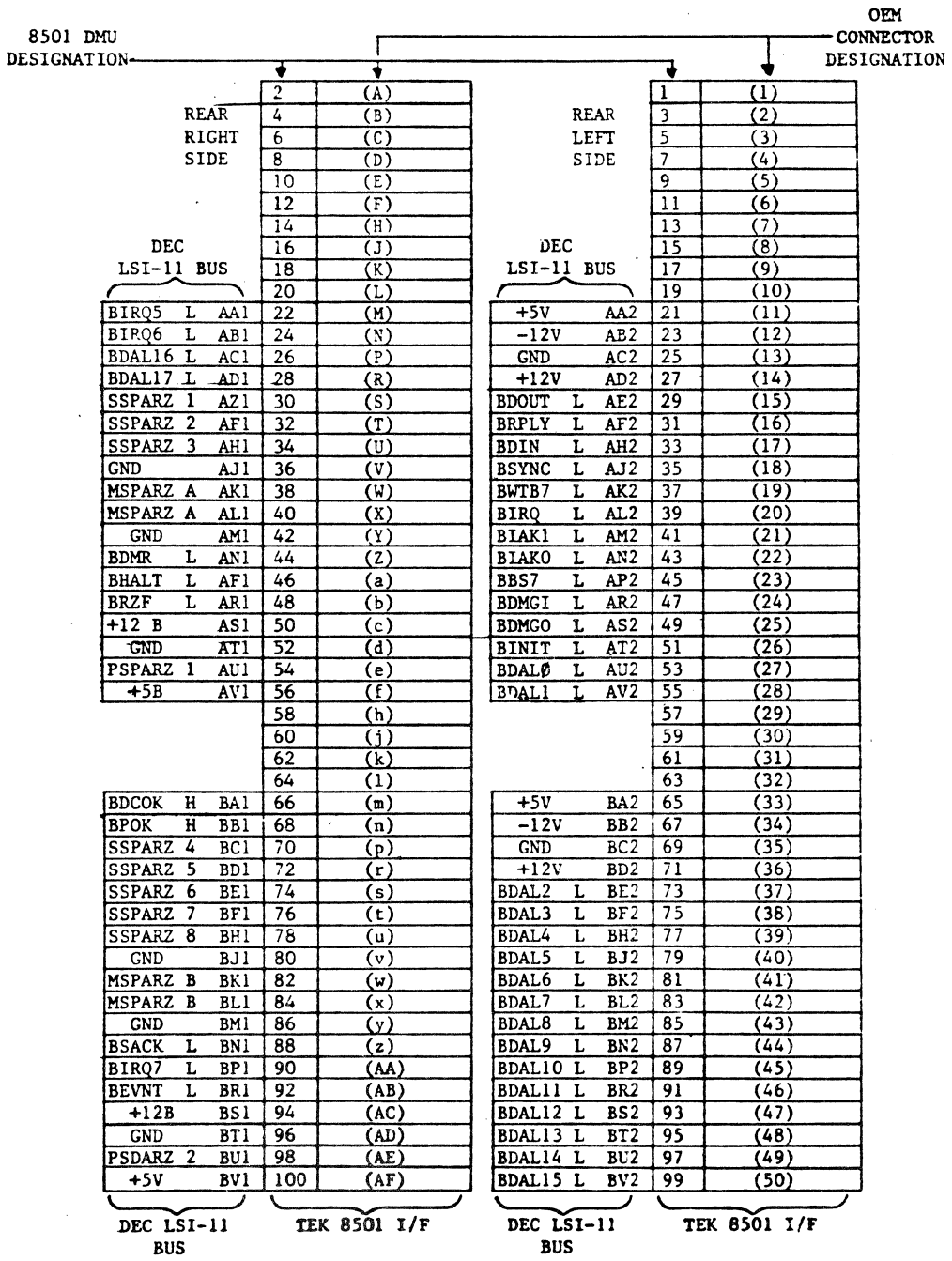


Fig. 6-1. LSI-11/2 72-Pin -- 8501 100-Pin Interface.

PORT CHARACTERISTICS

This sub-section provides details on use of the three I/O interface ports accessible at the rear of the 8501 DMU.

A schematic of the three ports is shown in Figure 6-2. These ports are located on the Comm Adapter board and extend through the rear panel.

The High-Speed Interface port (HSI) is normally used for communication over an RS-422 data line. By moving the harmonica bus selector plug located on the Comm Adapter board, the HSI port can be configured to RS-232-C and RS-423 communication standards. RS-422 is the standard communication method used between the 8501 and HSI peripherals such as the 8301 MDU. The HSI port uses a (receiver control/status) default address of 176510, and an Interrupt Vector address of 360. Both these addresses may be changed by software.

The PRINTER and AUXILIARY ports are both configured for RS-232-C communications. The PRINTER port is usually dedicated to line printer operations. The AUXILIARY port is usually dedicated to CRT/Keyboard terminal operations. Note for the PRINTER port that a type of printer vector interrupt is selectable on the Utility board (see Strapping Options-Sections 2). The PRINTER port uses a default address of 177510 and an interrupt vector address of 200. The AUXILIARY port uses a default address of 177560 and an interrupt vector address of 60. Both the PRINTER and AUXILIARY ports are identical in their wiring and communication methods.

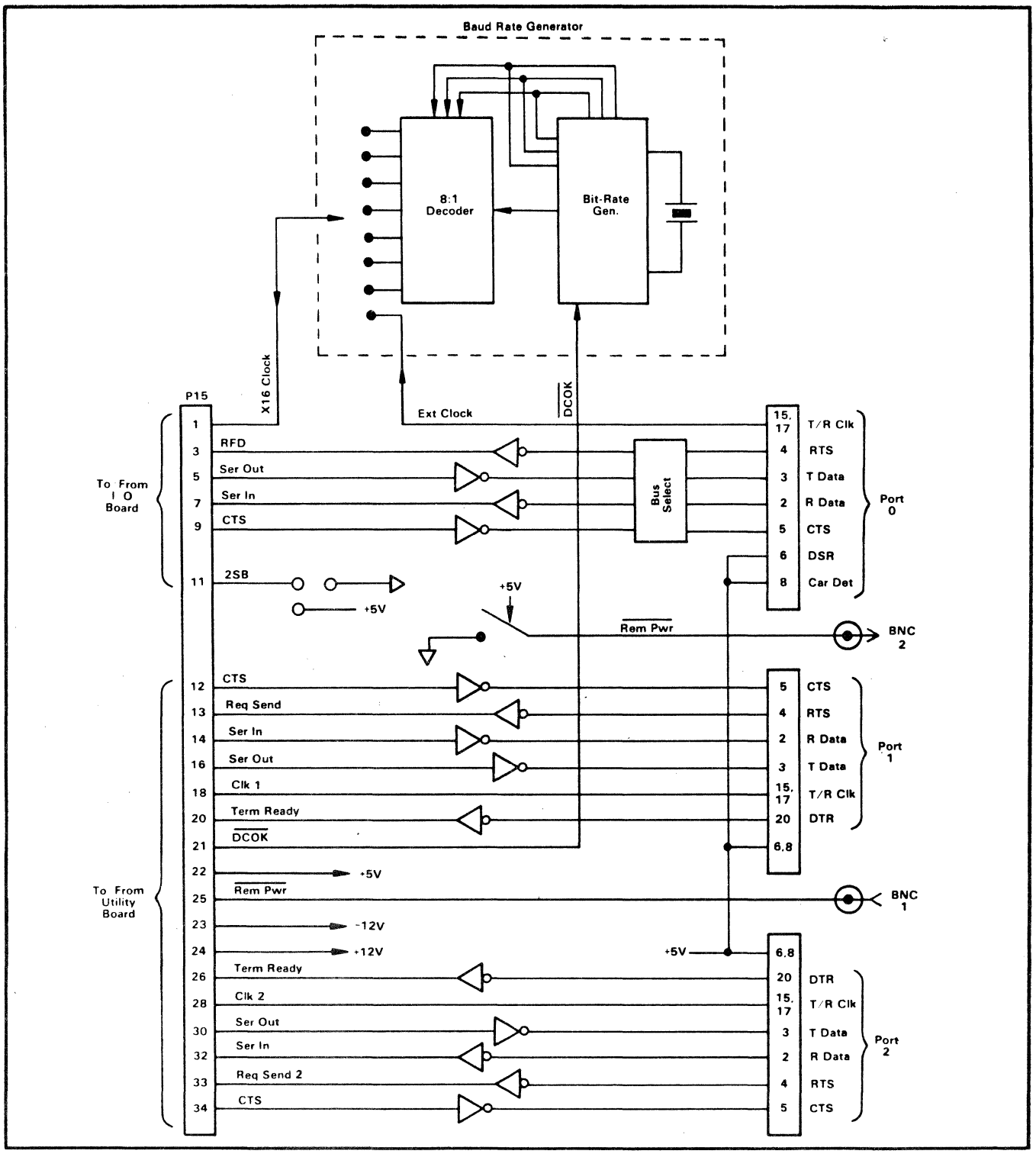


Fig. 6-2. Schematic showing Comm Adapter I/O Ports.

RS-232-C

In this protocal, data is sent from the 8501 on the IDATA line, and received on the RDATA line. All data byte communcations are preceded by one Start bit, and terminated by one or more Stop bits. The presence of the Start/Stop bits are checked, and their omission will cause a framing error. (The framing error may be disabled. See Section 2 of this manual for Utility board strapping options). Parity is also checked by the 8501 unless the NO PARITY option is selected for each port on the Utility board.

The baud rate for sending and receiving data can be set in three different ways:

- Set by the baud rate straps on the Utility board.
- Set by an external clock (the 8501 baud rate equals bit frequency divided by 16).
- Set under program control by addressing bits 12 through 15 in the Utility board Transmit Control/Status Register (XCSR).

Details for specifying baud rates using any of the above procedures are contained in Table 2-17 of Section 2, or in the appropriate system Users Manual.

The CTS (Clear to Send) line is asserted by the 8501 when the 8501 is free to receive data. The RTS (Request to Send) signal is asserted when the peripheral wishes to receive data (thereby putting the 8501 in transmit mode). The DTR signal is activated by the peripheral when it is ready to transmit or receive. Note that all signals including data are active low.

The T/R (Transmit/Receive) Clock line is an optional facility for setting communications rates by means of an external clock. This must be an even baud rate (including stop bits) determined by dividing the bit rate frequency by 16.

The 8501 DMU conforms to the Electronic Industries Association (EIA) standard. For time durations of all signals mentioned, refer to the applicable EIA documents.

RS-422 and RS-423

The RS-422 and RS-423 communications standards are similar to RS-232-C in terms of signal meanings. The difference is in the method of transmission. All four principal communication lines (RDATA, TDATA, RTS and CTS) use two lines to communicate instead of one. For example, TDATA uses pins 3 and 12 instead of just pin 3 as in RS-232. In the case of RS-422, each pair are balanced lines. In the case of RS-423 they are unbalanced lines.

Balanced lines mean that the signal is sent on one line in the normal fashion (as for RS-232-C) while the other line is exactly diametrically opposed, or a mirror image of it. The advantage to this is that the difference signal is twice as large, and any interference on the line is cancelled out by the signal opposition (ie the difference voltage remains the same).

Unbalanced lines (ie for RS-423) have one of the signal pairs grounded. In addition, while the receiving end does a voltage compare, the line driver does not invert the second signal. Thus, in this case, the voltage difference is not twice normal. Although RS-423 produces better results than RS-232-C (for long cable lengths and higher baud rates), it is still not as reliable as RS-422 for long distance communications at high speeds.

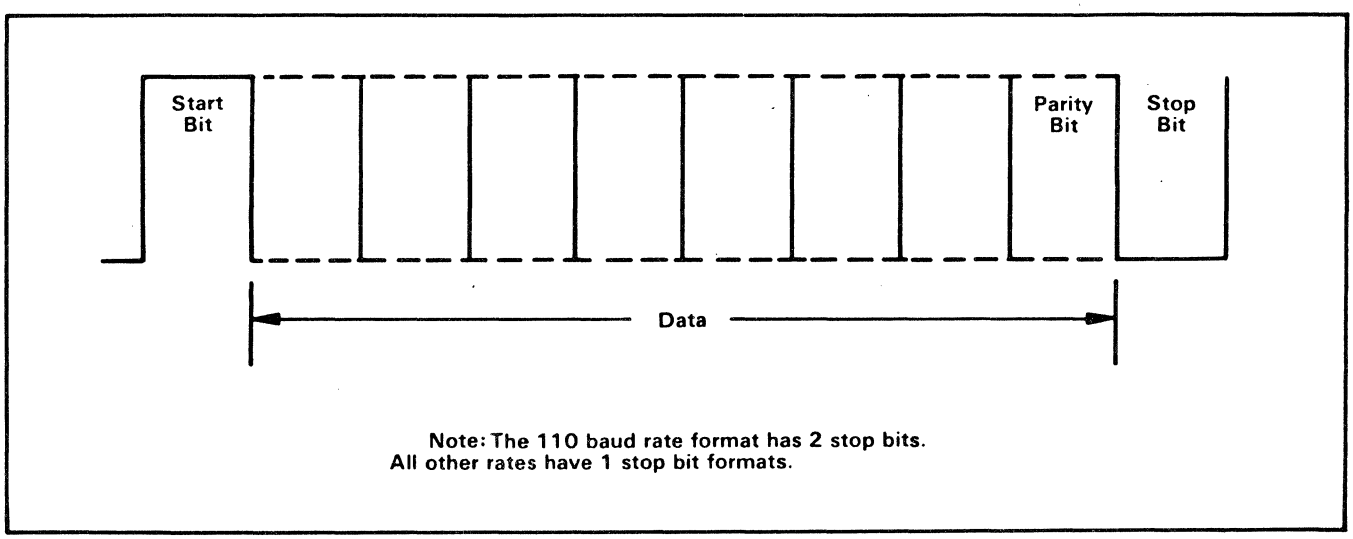


Fig. 6-3. Serial data format.

ASCII Code Chart

An ASCII code chart is reproduced in Figure 6-4. The extent of symbol usage will depend on the translation capabilities of the peripheral connected to the 8501 DMU.

LOW-ORDER BITS	HIGH-ORDER BITS: 0	1	2	3	4	5	6	7
	CONTROL		SYMBOLS		UPPERCASE		LOWERCASE	
0	NUL	DLE	SP	ø	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL (BELL)	ETB	'	7	G	W	g	w
8	BS (BACK SPACE)	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	¦
D	CR (RETURN)	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL (RUBOUT)

Fig. 6-4. ASCII code chart.

Section 7

LSI-11/2 PROCESSOR

INTRODUCTION

The 8501 processor is a Digital Equipment Corporation LSI-11/2. It plugs into a 72-pin edge connector specifically configured to accept the DEC dual width card. All power requirements (+5 Vdc, +12 Vdc) are supplied through the edge connector.

JUMPERS

The jumpers described in the following text are illustrated in Fig. 7-1.

W1 Master Clock Enable for normal operation requires that W1 be installed. It is removed only when testing the clock circuit.

W3 Event Interrupts (default configuration = enabled). External Event (EVNT) interrupts are enabled when jumper W3 is removed. The EVNT interrupt is initiated by an external device when it asserts the BEVNT bus signal. The EVNT interrupt is the highest priority external interrupt.

Power - Up Mode Select Jumpers

Four power-up modes are available for user selection. These are selected by positioning jumpers W5 and W6. Table 7-1 lists the straps, their positions, and the corresponding mode. The modes are explained in the following text.

Table 7-1
Power-UP Mode Jumpers

	JUMPERS	
MODE	W6	W5
0	OUT	OUT
1	OUT	IN
2	IN	OUT
3	IN	IN

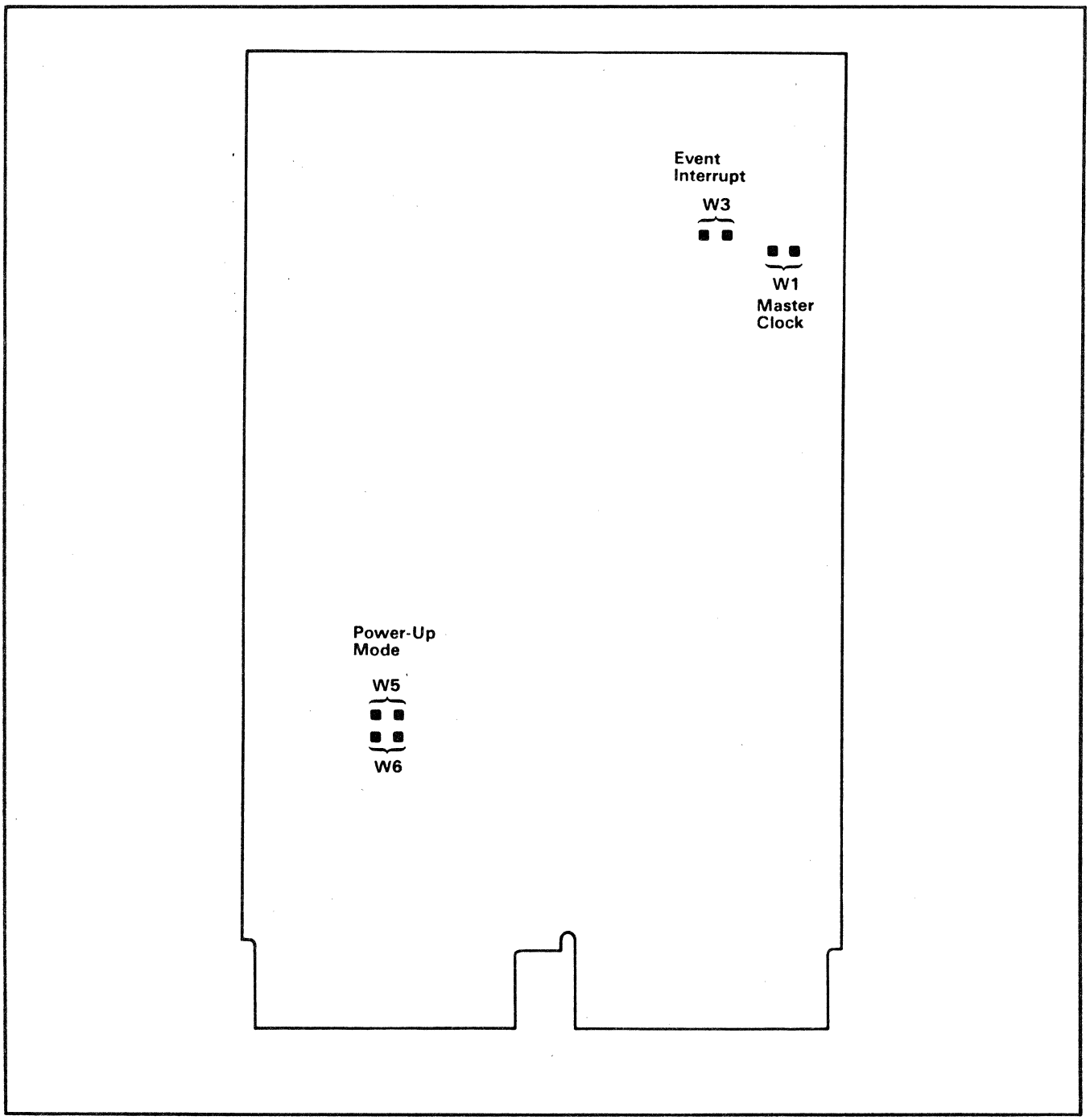


Fig. 7-1. Processor strap locations.

Mode 0 When the 8501 is powered-up this option places the processor in a microcode sequence that fetches the contents of memory locations 24 and 26 (octal), and loads their contents into R7 (program counter) and the PS (processor status word), respectively. When this condition is entered, the next operation will depend on the state of the BHALT(L) signal. If BHALT(L) is asserted low the terminal (ODT) microcode is entered. The terminal then functions as the front panel. If BHALT(L) is not asserted, program execution will begin with the address contained in R7 (program counter).

Mode 1 When the 8501 is powered-up, this mode immediately places the LSI-11/2 in the terminal microcode (ODT) mode regardless of the state of the BHALT(L) signal. This mode assumes a terminal at bus address 177560 (octal).

Mode 2 (Standard Configuration = Enabled) When the 8501 is powered-up this mode places the LSI-11/2 in a microcode sequence that loads a starting address of 173000 (octal) into R7 (Program Counter) and begins program execution at this location if the BHALT(L) signal is not asserted. Address 173000 (octal) is the starting address for the DEC diagnostic program. When the diagnostic program completes execution the bootstrap program will execute. If BHALT(L) is asserted, the LSI-11/2 will not execute the instruction at location 173000 (octal), and will immediately execute the terminal microcode (ODT).

Mode 3 This mode is used by the LSI-11/2 processor to implement a method of powering-up in the microcode address space. This mode is not supported in the 8501.

TERMINAL ODT COMMANDS

The terminal ODT commands enable a terminal to function as a front panel. The terminal keyboard replaces the front panel address, data, and function switches. The terminal display replaces the typical front panel alphanumeric displays and/or binary status indicators.

The terminal ODT commands are executed by the LSI-11/2 processor only when the processor is in the HALT mode. Once the HALT mode has been entered the ODT commands are entered from the terminal keyboard. Table 7-2 lists the ODT commands. The HALT mode is entered in one of the following ways:

- Executing a HALT instruction.
- Optionally, pressing the BREAK key on the terminal.
- During Power-Up (Mode 1).
- The BHALT(L) bus signal is asserted by toggling the 8501 front panel HALT switch.
- A double Bus Error. (Stack pointer points to non-existent memory when the stack is used after a error condition.)
- A Bus Error (timeout) when the processor is attempting to input a vector from an interrupting device.

Table 7-2
ODT Commands (Terminal Microcode)

Command	Description
RETURN	Close opened location and accept next command.
LINE FEED	Close current location; open the next sequential location.
^	(ASCII 5E) Close the open location and open the location -2.
-	(ASCII 5F) This command is used to open the location whose address is arrived at by taking the open location contents and adding it to the open location address +2.
@	Take the contents of opened location as the absolute address and open that location.
r/	Open the word at location r.
$n/ or Rn/	Open general register n (0-7) or S (PS register).
r;G or rG	Go to location r and start program execution. The 8501 initialize signal: B INIT (L), is issued for 10 uS before execution starts.
L	This command is not used. NOTE: If the 'L' command is inadvertently entered, system RESTART must be used to re-enter the command mode.
P	Proceed with program execution at the location pointed to by the current contents of the PC (R7).
RUBOUT	Erases previous numeric character. Response is a (\).
Control Shift 'S'	(ASCII 13) This is a manufacturing test command. NOTE: If this command is inadvertently entered, enter any two characters (ignore anything displayed on the terminal) to terminate this mode.
M	Print contents of an internal CPU register. The terminal will print six characters and then return to the command mode. The last octal digit displayed will indicate how the processor entered the terminal mode. Table 7-3 shows the decoded meaning of the last octal digit.

Table 7-3
CPU Register CODE

Last Octal Digit Value	Function
0	Halt instruction or BHALT L was asserted.
1 or 5	Bus error occurred while getting interrupt vector.
2,6	Bus error occurred while doing memory refresh. This should not occur in the 8501.
3	Double Bus error occurred (stack contains non-existent address.
4	Reserved instruction trap occurred.
7	A combination of 1, 2, and 4 occurred.

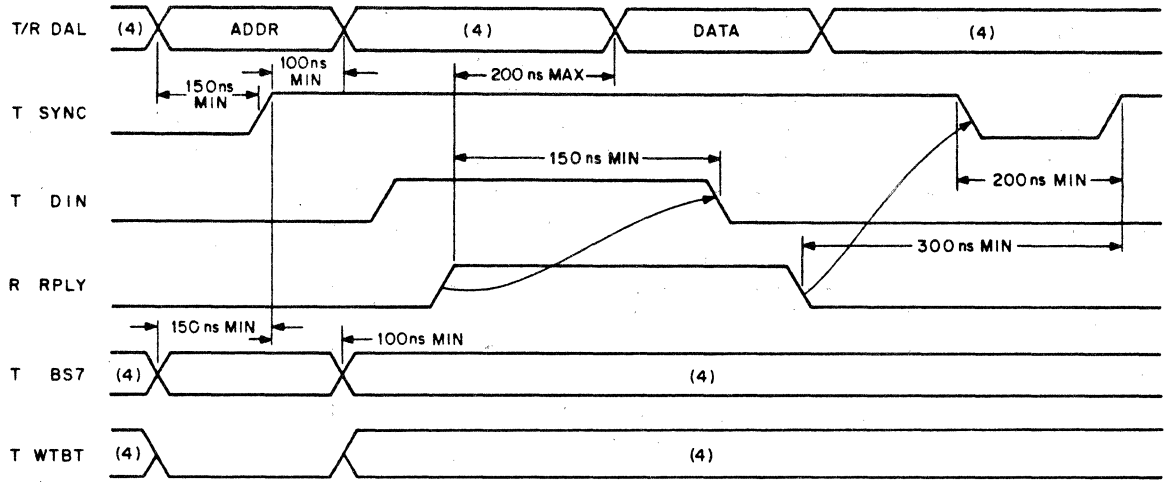
BUS PROTOCOL

The 8501 bus supports master-slave data transfers. The processor is usually the bus master, transferring data to or from slave devices such as memory or peripheral interfaces. Some types of peripheral devices are capable of direct memory access (DMA) transfers. When such a device requests bus mastership, the processor passes control to the requesting device. Only the processor and a DMA equipped device can gain bus mastership.

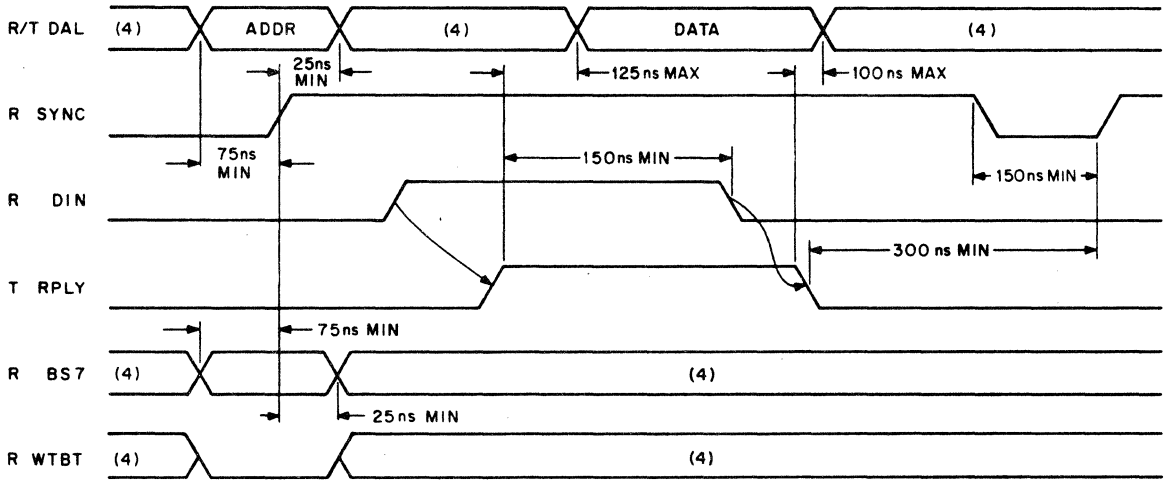
When the processor is executing instructions that do not require use of the bus, it is not bus master. It operates as a processor or arbitrator only. In the arbitrator role, the DEC processor supplies either the BIAK-0 signal for interrupting boards or the BDMG-0 signal for DMA requesting boards. Once the processor responds with BIAK-0 or BDMG-0, it is the relative position of each requesting board in the daisy-chain that actually determines the sequence in which they are serviced. Table 7-4 lists the five different types of data transfer cycles on the 8501 bus. Figures 7-2 through 7-7 show the timing diagram for each of these operations. Table 7-5 lists the DMA/Interrupt priority levels.

Table 7-4
Data Transfer Functions

Term	Function	Operation
DATI	Data Word Transfer input	Read
DATO	Data Word Transfer output	Write
DATIO	Data Word Transfer input followed by word transfer output.	Read/Modify/ Write
DATOB	Data Bytes Transfer output	Write
DATIOB	Data Word Transfer input followed by byte transfer output.	Read/Modify/ Write



TIMING AT MASTER DEVICE

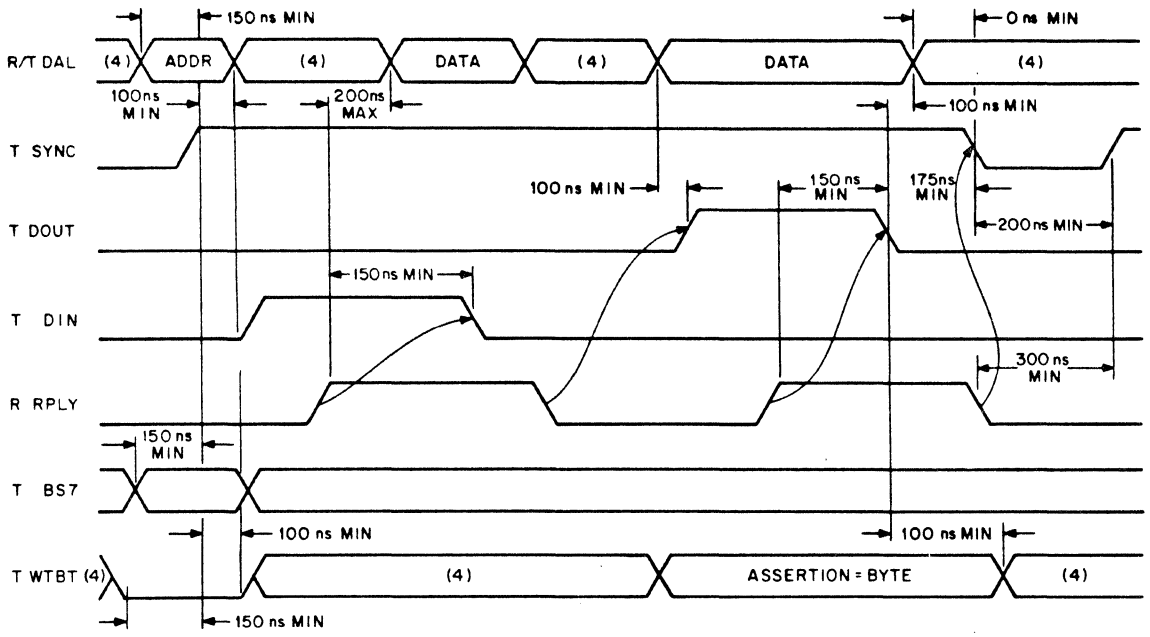


TIMING AT SLAVE DEVICE

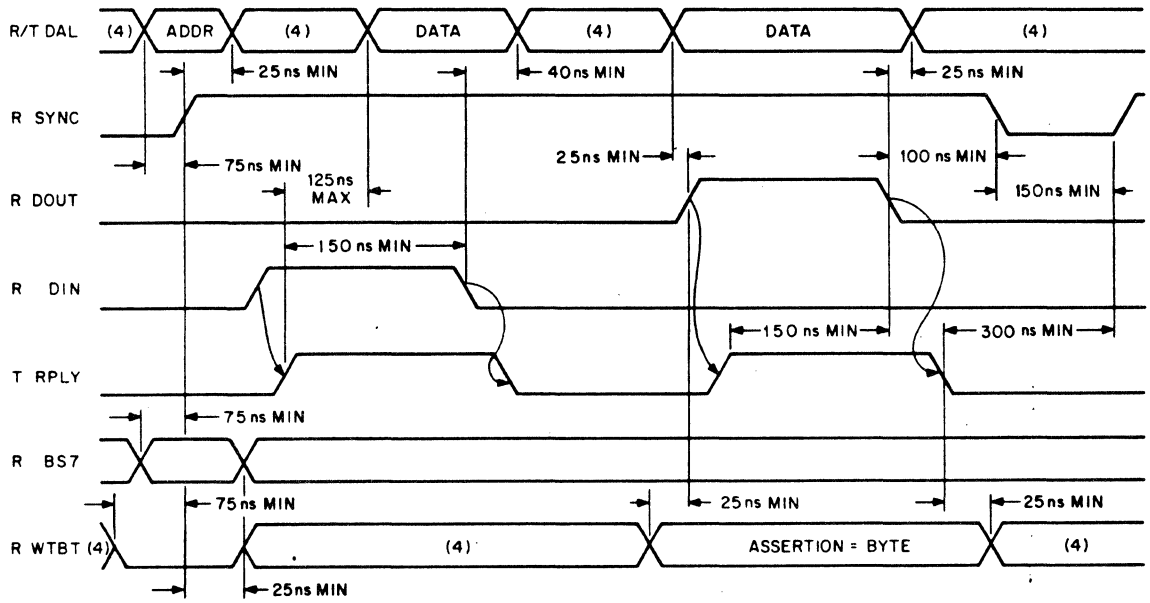
NOTES:

1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Fig. 7-2. DATI bus cycle timing.



TIMING AT MASTER DEVICE

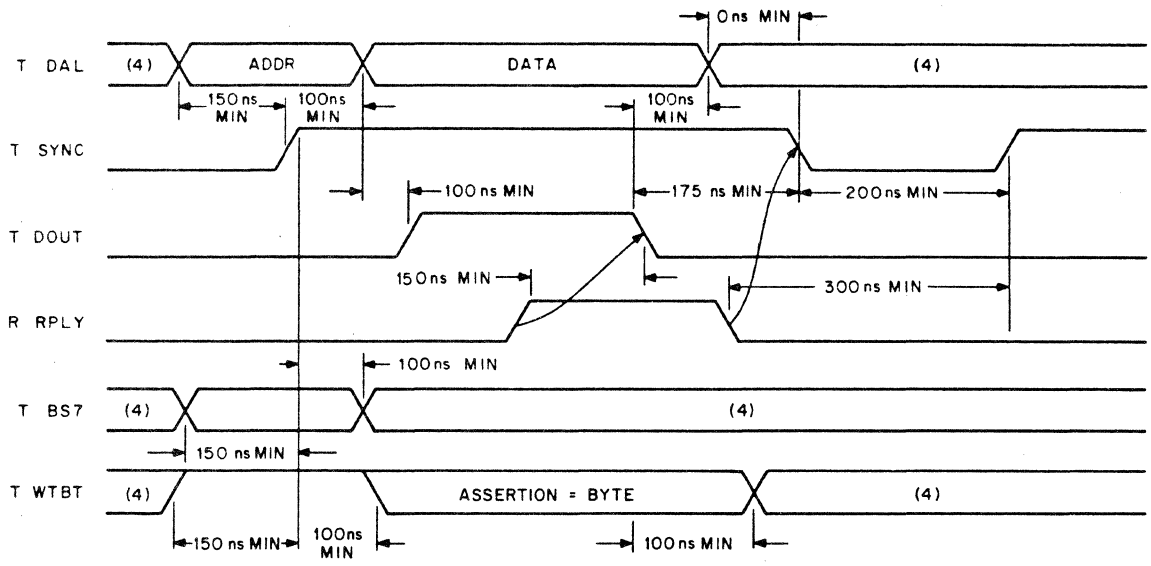


TIMING AT SLAVE DEVICE

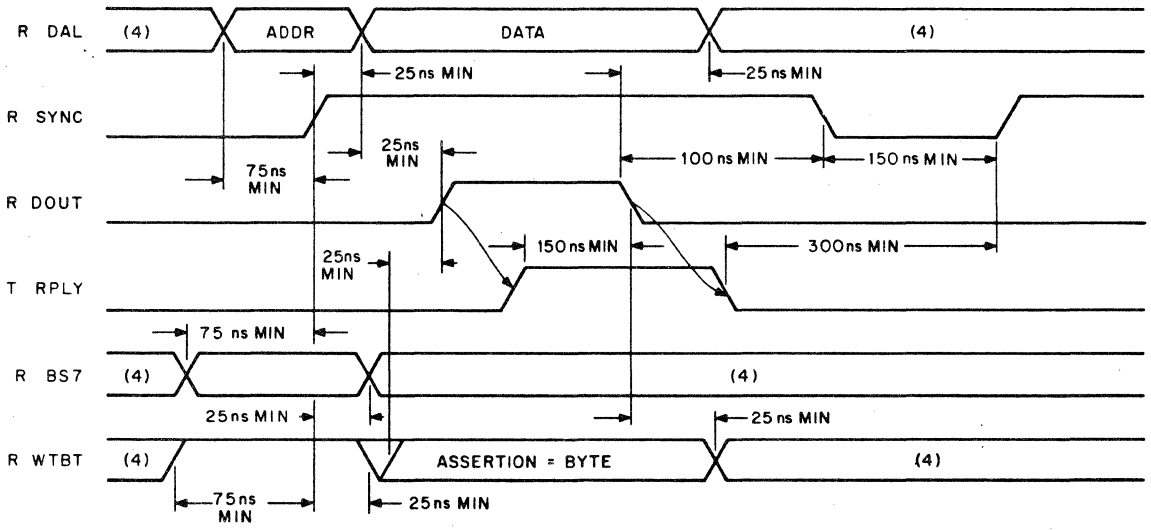
NOTES:

1. Timing shown at Requesting Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition

Fig. 7-3. DATO or DATOB bus cycle timing.



TIMING AT MASTER DEVICE

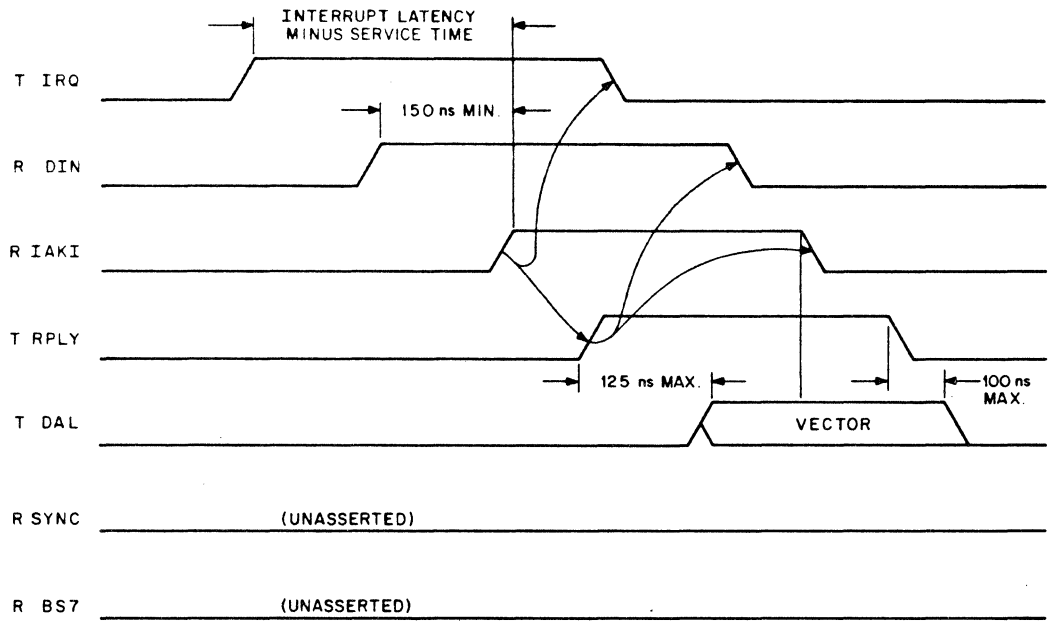


TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Fig. 7-4. DATIO or DATIOB bus cycle timing.



NOTES:
1. Timing shown at Requesting Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal Name Prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.

Fig. 7-5. Interrupt Transaction timing.

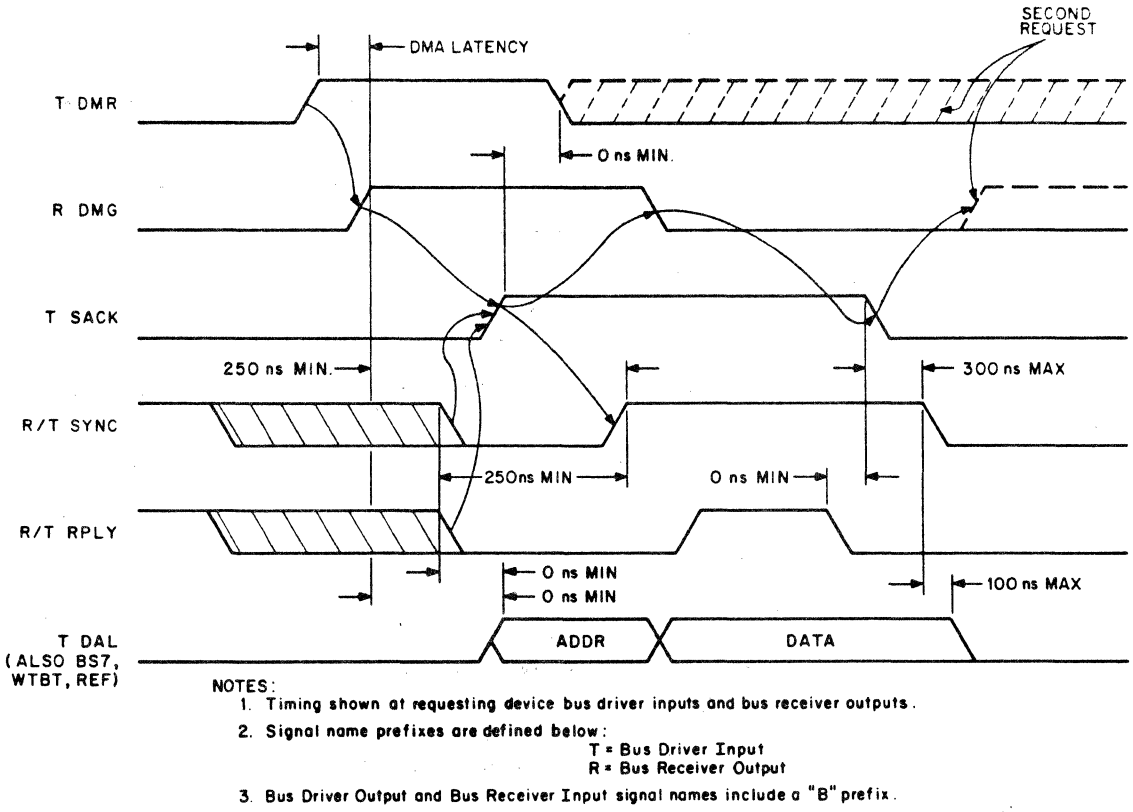


Fig. 7-6. DMA Request/Grant timing.

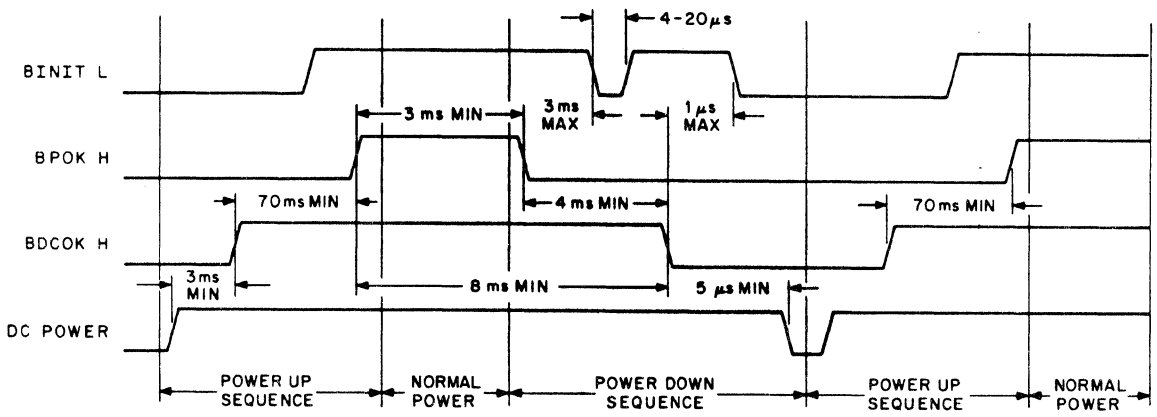


Fig. 7-7. Power-Up/Power-Down timing.

Table 7-5
DMA/Interrupt Priority

Priority	Board	Type
1	Processor	CPU
2	Flexible Disc	DMA/INTERRUPT
3	Spare	DMA/INTERRUPT
4	Memory	SLAVE
5	Spare	DMA/INTERRUPT
6	Spare	SLAVE
7	I/O	DMA/INTERRUPT
8	Utility	INTERRUPT

TRAP VECTORS

A trap is effectively an interrupt generated by software or the processor. A trap vector is two consecutive words of dedicated memory locations that contain a program counter (PC) and a processor status word (PSW) value. When a trap occurs, the contents of the current PC and PSW are pushed onto the processor stack and replaced by the contents of the two dedicated memory locations specified by the vector. Some program instructions and many error conditions generate traps. For example, if the processor references a peripheral device with an address and the addressed device fails to respond within a preset length of time, a bus time-out error occurs. When the processor detects the time-out condition, it immediately traps to memory location 004 (octal) and loads a new PC value. A new PSW is loaded from the next consecutive memory location, 006 (octal). Depending upon the software being used, the new PC and PSW usually cause the processor to begin executing a service routine to handle the error.

The return sequence from a trap involves executing an RTI or RTT instruction which restores the old PC and old PSW by popping them from the stack. Table 7-6 is a list of predefined trap vectors and trap priorities.

Table 7-6
Predefined Trap Vectors (Octal)

Condition	PC Locations	PSW Locations
CPU Reserved Location	000	002
Bus time-out error and Illegal Instruction	004	006
Reserved instruction	010	012
BPT/Trace	014	016
IOT instruction	020	022
Power fail	024	026
EMT instruction	030	032
TRAP instruction	034	036
FIS (option)	244	246
Event Line	100	102

Trap Priorities

1. Bus time out
2. Instruction trap
3. Trace traps
4. Power fail trap
5. Halt line
6. Event line
7. Device (bus) interrupt request

LSI-11/2 INSTRUCTION EXECUTION TIMES

The execution time for an instruction depends on the instruction itself, the modes of addressing used, and the type of memory referenced. In most cases the instruction execution time is the sum of a Basic Time, a Source Address (SRC) Time, and a Destination Address Time (DST).

instruction time = basic time + SRC time + DST time

basic time = fetch time + decode time + execute time

All timing information given in the following tables is in microseconds, unless otherwise noted. Times are typical; process timing can vary +20 percent. A 350 ns microcycle is assumed.

Table 7-7
Source and Destination Time

MODE	SRC TIME (Word)	SRC TIME (Byte)	DST TIME (Word)	DST TIME (Byte)
0	0	0	0	0
1	1.40 uS	1.05 uS	2.10 uS	1.75 uS
2	1.40	1.05	2.10	1.75
3	3.50	3.15	4.20	4.20
4	2.10	1.75	2.80	2.45
5	4.20	3.85	4.90	4.90
6	4.20	3.85	4.90	4.55
7	6.30	5.95	6.65	7.00

NOTE: For Mode 2 and Mode 4, if R6 and R7 are used with byte operations, add 0.35 uS to SRC time and 0.70 uS to DST time.

Table 7-8
Basic Time (Double Operand Instructions)

DOPS (Double Operand)	DM0	DM1-7
MOV	3.50 uS	2.45 uS
ADD, XOR, SUB, BIC, BIS	3.50	4.20
CMP, BIT	3.50	3.15
MOVB	3.85	3.85
BICB, BISB	3.85	3.85
CMPB, BITB	3.15	2.80

NOTE: DM0 = Destination Mode 0
DM1-7 = Destination Modes 1 through 7

Table 7-9
Basic Time (Single Operand Instructions)

SOPS (Single Operand)	DM0	DM1-7
CLR	3.85 uS	4.20 uS
INC, ADC, DEC, SEC	4.20	4.90
COM, NEG	4.20	4.55
ROL, ASL	3.85	4.55
TST	4.20	3.85
ROR	5.25	5.95
ASR	5.60	6.30
CLRB, COMB, NEGB	3.85	4.20
ROLB, ASLB	3.85	4.20
INCB, DECB, SBCB, ADC	3.85	4.55
TSTB	3.85	3.50
RORB	4.20	4.90
ASRB	4.55	5.95
SWAB	4.20	3.85
SXT	5.95	6.65
MFPS (1067DD)	4.90	6.65
MTPS (1064SS)	7.00	7.00*

Note: For MTPS use Byte DST time not SRC time.
Add 0.35 microseconds to instruction time
if Bit 7 of effective OPR = 1.

Table 7-10
JMP/JSR Destination Time

JMP/JSR Mode	DST Time
1	0.70 uS
2	1.40
3	1.75
4	1.40
5	2.45
6	2.45
7	4.20

Table 7-11
Basic Time (JMP/JSR Instructions)

Instruction	Basic Times
JMP	3.50 uS
JSR (PC=LINK)	5.25
JSR (REG.=LINK)	8.40

NOTE: Basic time = fetch time + decode time + execute time.
Instruction Execution Time = basic time + DST time.
PC = Program counter
REG = Register 0-6.

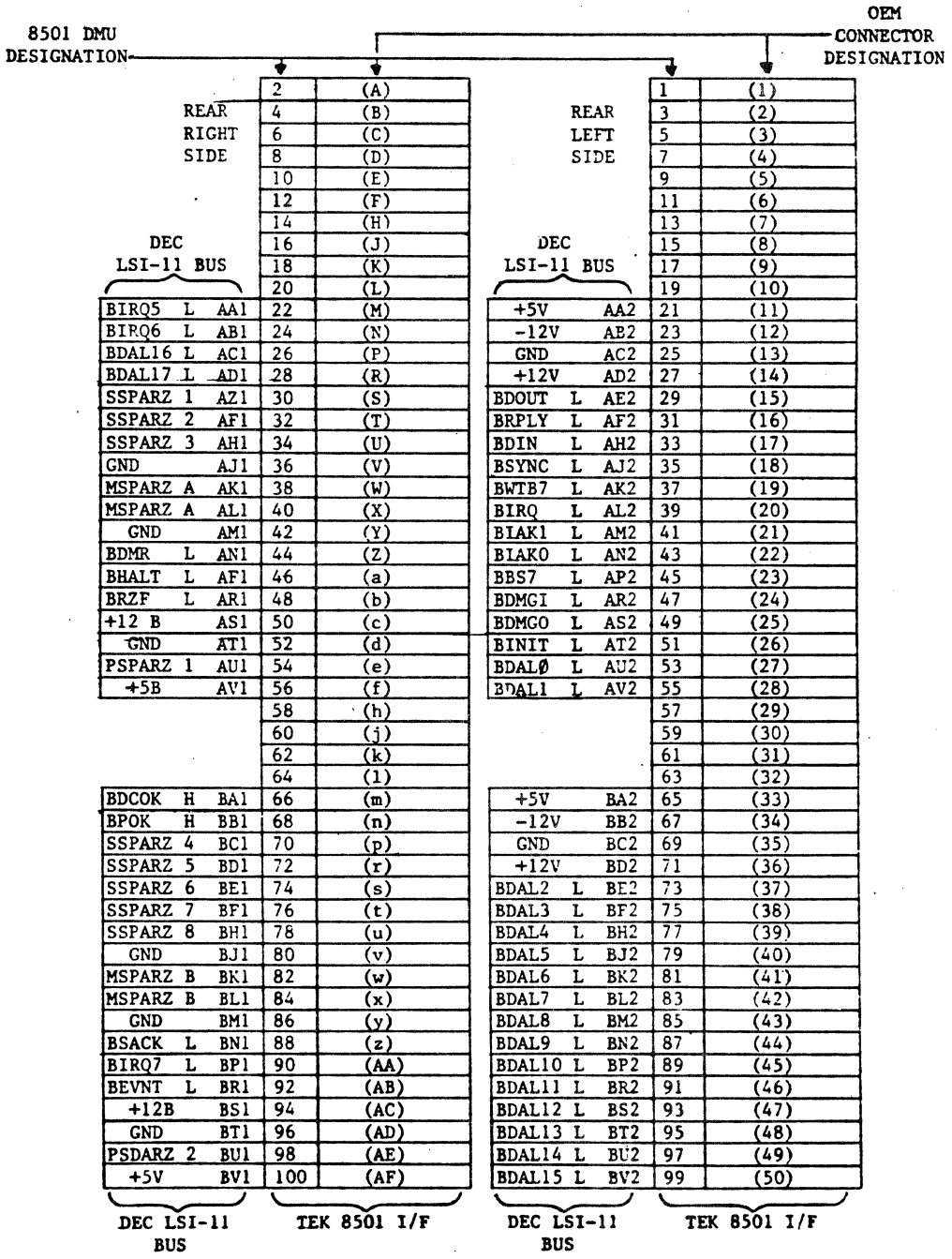
Table 7-12
Execution Time Miscellaneous Instructions

Instruction	Microseconds
All Branches	3.50
SOB (Branch)	4.90
SOB (No Branch)	4.20
SET CC	3.50
CLEAR CC	3.50
NOP	3.50
RTS	5.25
MARK	11.55
RTI	8.75*
RTT	8.75*+
TRAP, EMI	16.80*
IOT, BPT	18.55*
WAIT	6.30
HALT	5.60
RESET	5.95 + 10 for INIT + 90

Note: * = If the new PS contained a '1' in bit 4 or bit 7 add 0.35 us for each instruction.
+ = If the new PS contained a '1' in bit 4 add 2.10 microseconds.

DEC 72-PIN - 8501 100-PIN INTERFACE

A complete list of the edge card connector pins is given in Fig. 7-8 showing pin number, signal name, and interface to the 100-pin 8501 bus. (H) = signal asserted at high TTL level. (L) = signal asserted at low TTL level.



DEC LSI-11 BUS			TEK 8501 I/F		DEC LSI-11 BUS			TEK 8501 I/F	
			2	(A)				1	(1)
			4	(B)				3	(2)
			6	(C)				5	(3)
			8	(D)				7	(4)
			10	(E)				9	(5)
			12	(F)				11	(6)
			14	(H)				13	(7)
			16	(J)				15	(8)
			18	(K)				17	(9)
			20	(L)				19	(10)
BIRQ5	L	AA1	22	(M)	+5V		AA2	21	(11)
BIRQ6	L	AB1	24	(N)	-12V		AB2	23	(12)
BDAL16	L	AC1	26	(P)	GND		AC2	25	(13)
BDAL17	L	AD1	28	(R)	+12V		AD2	27	(14)
SSPARZ 1		AZ1	30	(S)	BDOUT	L	AE2	29	(15)
SSPARZ 2		AF1	32	(T)	BRPLY	L	AF2	31	(16)
SSPARZ 3		AH1	34	(U)	BDIN	L	AH2	33	(17)
GND		AJ1	36	(V)	BSYNC	L	AJ2	35	(18)
MSPARZ A		AK1	38	(W)	BWTB7	L	AK2	37	(19)
MSPARZ A		AL1	40	(X)	BIRQ	L	AL2	39	(20)
GND		AM1	42	(Y)	BIAK1	L	AM2	41	(21)
BDMR	L	AN1	44	(Z)	BIAK0	L	AN2	43	(22)
BHALT	L	AF1	46	(a)	BBS7	L	AP2	45	(23)
BRZF	L	AR1	48	(b)	BDMGI	L	AR2	47	(24)
+12 B		AS1	50	(c)	BDMGO	L	AS2	49	(25)
GND		AT1	52	(d)	BINIT	L	AT2	51	(26)
PSPARZ 1		AU1	54	(e)	BDALØ	L	AU2	53	(27)
+5B		AV1	56	(f)	BDAL1	L	AV2	55	(28)
			58	(h)				57	(29)
			60	(j)				59	(30)
			62	(k)				61	(31)
			64	(l)				63	(32)
BDCOK	H	BA1	66	(m)	+5V		BA2	65	(33)
BPOK	H	BB1	68	(n)	-12V		BB2	67	(34)
SSPARZ 4		BC1	70	(p)	GND		BC2	69	(35)
SSPARZ 5		BD1	72	(r)	+12V		BD2	71	(36)
SSPARZ 6		BE1	74	(s)	BDAL2	L	BE2	73	(37)
SSPARZ 7		BF1	76	(t)	BDAL3	L	BF2	75	(38)
SSPARZ 8		BH1	78	(u)	BDAL4	L	BH2	77	(39)
GND		BJ1	80	(v)	BDAL5	L	BJ2	79	(40)
MSPARZ B		BK1	82	(w)	BDAL6	L	BK2	81	(41)
MSPARZ B		BL1	84	(x)	BDAL7	L	BL2	83	(42)
GND		BM1	86	(y)	BDAL8	L	BM2	85	(43)
BSACK	L	BN1	88	(z)	BDAL9	L	BN2	87	(44)
BIRQ7	L	BP1	90	(AA)	BDAL10	L	BP2	89	(45)
BEVNT	L	BR1	92	(AB)	BDAL11	L	BR2	91	(46)
+12B		BS1	94	(AC)	BDAL12	L	BS2	93	(47)
GND		BT1	96	(AD)	BDAL13	L	BT2	95	(48)
PSDARZ 2		BU1	98	(AE)	BDAL14	L	BU2	97	(49)
+5V		BV1	100	(AF)	BDAL15	L	BV2	99	(50)

Fig. 7-8. DEC 72 Pin - 8501 100 Pin Interface.

Section 8

MEMORY BOARD

INTRODUCTION

This board provides 32,768 16-bit words of dynamic RAM memory. The memory board is supplied with bank select straps, and provides for either the top 2K-words or the top 4K-words to be used as I/O. The memory devices making up the top 16K-words may be removed to provide an 8501 with only 16K words of memory.

The memory board has an average read cycle access time of 210 nS and a memory cycle time of 410 nS.

Distributed refresh for the dynamic RAM's is provided by on-board circuitry. A dynamic RAM refresh cycle will occur during every cycle, providing the memory board is not selected, or after a 15 microsecond period has elapsed since the last refresh cycle. The maximum delay produced by a refresh cycle is 450 nS.

The memory board timing control is provided by a 24.25 MHz crystal controlled clock. Refresh request (RF REQ) and Bus request (BUS REQ) are each sampled once during each clock period to yield a maximum latency of 41 nS before the memory cycle is initiated.

Table 8-1 lists the power requirements of the 32K Memory board. See Section 2 of this manual for a list of Memory board jumpers and straps.

Table 8-1
Power Requirements

Voltage	Typical	Maximum
+5 Vdc	0.720 A	1.20 A
+12 Vdc	0.675 A	0.90 A
-12 Vdc	0.015 A	0.02 A

Section 9

UTILITY BOARD

INTRODUCTION

The Utility board provides some features not supplied by the other boards. Refer to Fig. 9-1 for a functional block diagram of the Utility board. Figure 9-2 illustrates the serial interface registers. See Section 2 of this manual for jumper and strap locations, and their functions.

The features supplied by the Utility board are:

- Two RS-232-C Interfaces
- Line-Time Clock Control (LTC)
- Bootstrap PROM
- Diagnostic PROM
- Front Panel Functions (RESTART, RUN/HALT)
- Power Control Logic
- Bus Termination Resistors
- Diagnostic Status Indication (LED's)

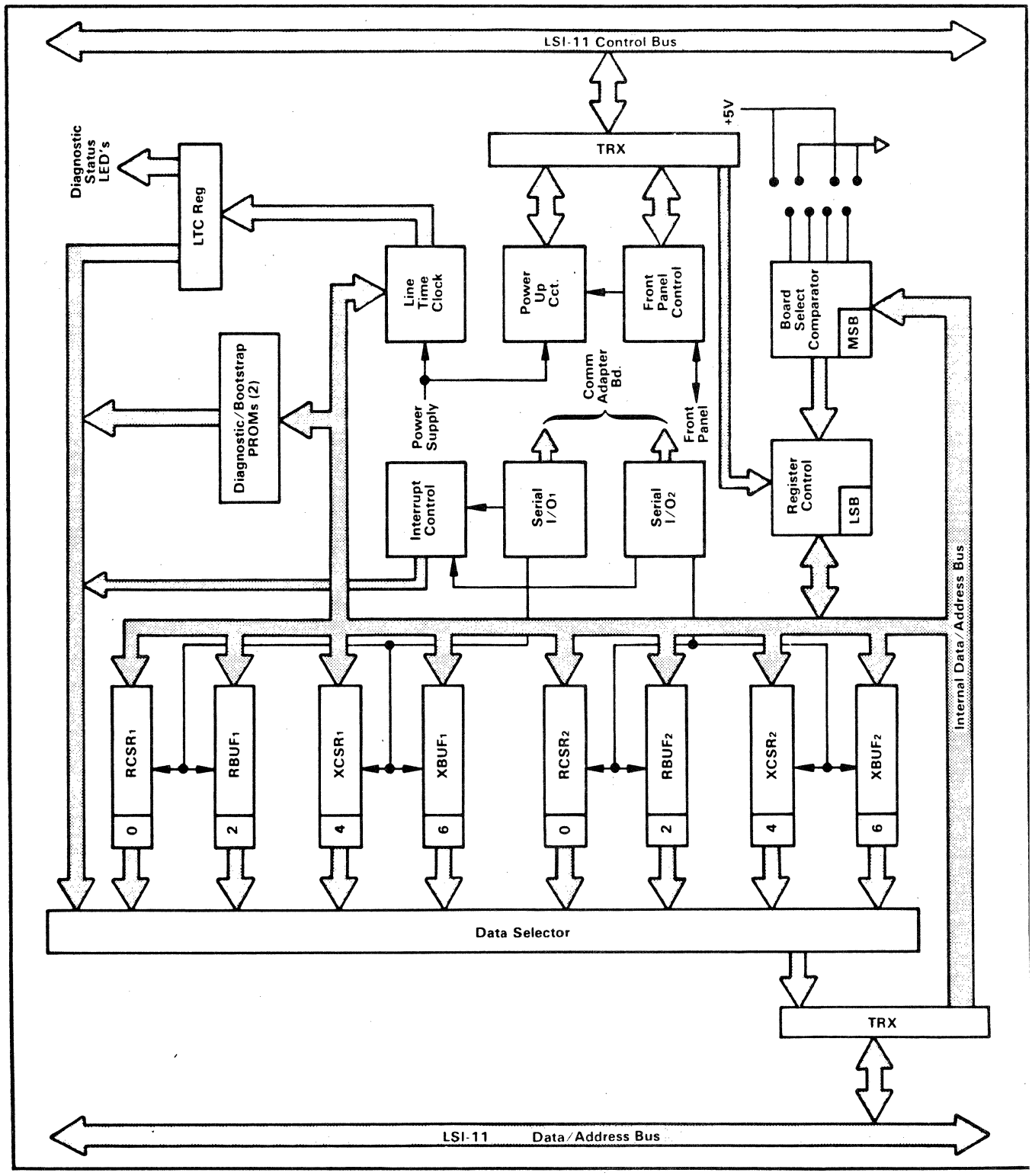


Fig. 9-1. Utility board functional block diagram.

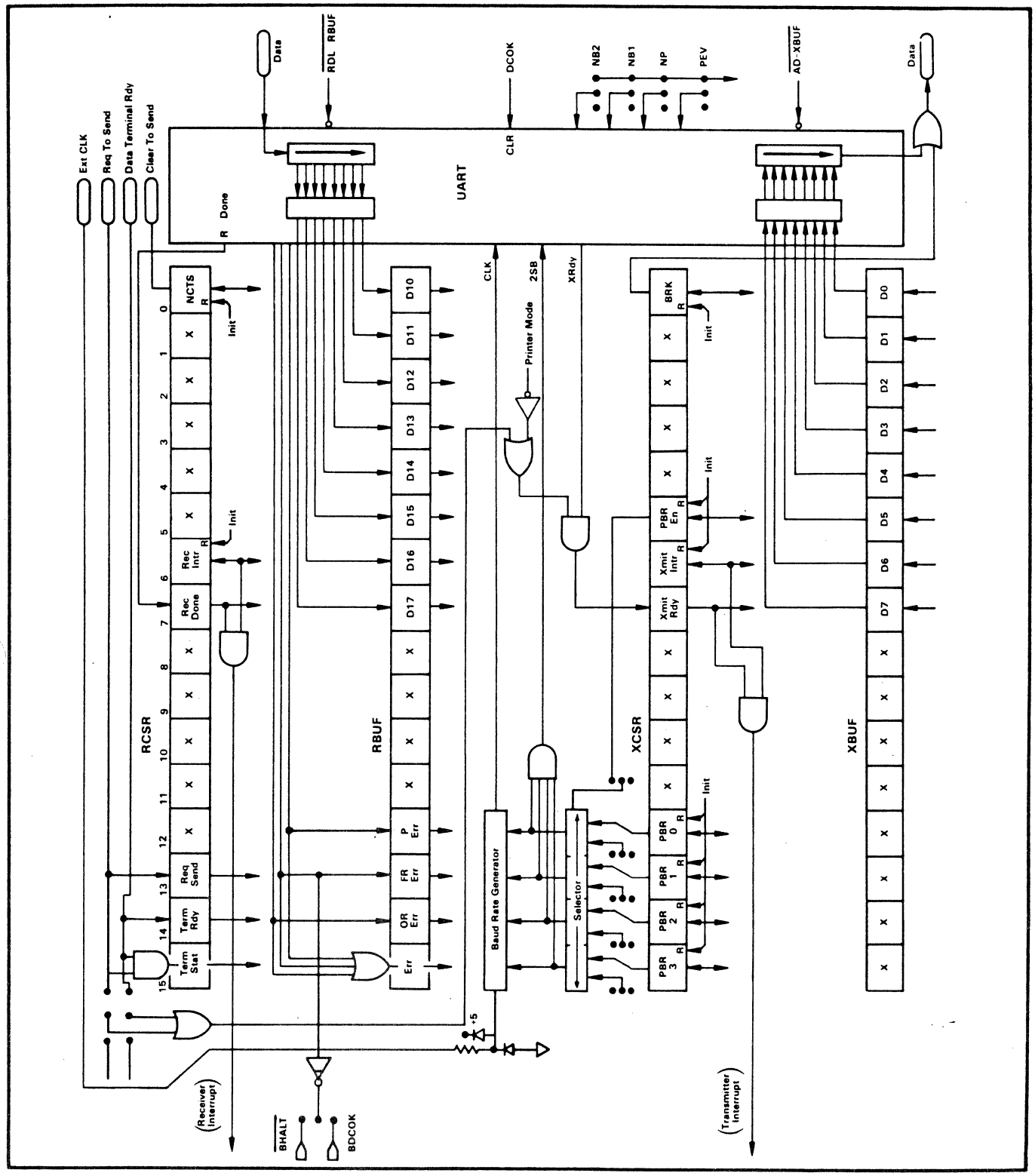


Fig. 9-2. Serial interface registers.

RS-232-C COMMUNICATIONS

The outputs and inputs of the two RS-232-C interfaces (PRINTER and AUXILIARY) are connected to the Communications Adapter Board. The Communications Adapter Board provides the translation between the TTL output/input of the Utility board and standard RS-232-C voltage levels.

The baud rate for the two RS-232-C interfaces may be selected either by software or by straps provided on the Utility board. The baud rate for the two interfaces is independently selectable over a range of 50 to 9600. Provisions are made for an external clock which will accept a TTL level signal between 0 and 320 KHz (the external clock frequency is 16 times the baud rate).

Serial Interface Register Definitions

Register 0 - Receiver Control/Status Register (RCSR)

BIT	DESCRIPTION
15	Set when Data Terminal Ready (DTR) and Request To Send (RTS) are both received true. Read-only bit.
14	Set when DTR is received true. Read-only bit.
13	Set when RTS is received true Ready-only bit.
12-8	NOT USED. Read as 0
7	Receive done. Set when an entire character has been received and is ready to be read from RBUF. This bit is automatically cleared when RBUF is read or when DCOK goes false. A receiver interrupt is sent by the interface when this bit is set and the receiver interrupt is enabled (i.e., bit 6 is also set). Read-only bit.
6	Interrupt Enable. Set under program control to generate a receiver interrupt request when a character is ready for input to the processor (i.e., bit 7 is also set). Cleared under program program control or by the INIT signal. Read/Write bit.
5-1	NOT USED. Read as 0.
0	CTS. Drives Clear To Send (CTS). 1 = not CTS, 0 = CTS. Read/Write bit, cleared by INIT (i.e. during initialization).

Register 2 - Receiver Data Buffer (RBUF)

BIT	DESCRIPTION
15	Error. "OR" of bits 14, 13, and 12. Read-only bit.
14	Overrun Error. When set, indicates that the previously received character was not read prior to receiving a new character. Cleared by DCOK false or the receipt of a new valid character after reading the overrunning character. Read-only bit.
13	Framing Error. When this bit is set, indicates that the parity of the received character does not agree with the expected parity. Always 0 if no parity is selected. Read-only bit, cleared by DCOK false or the receipt of a new valid character.
11	NOT USED. Read as 0
7-0	Contains 5 to 8 data bits in a right-justified format. Read-only bits.

Register 4 - Transmit Control/Status Register (XCSR)

BIT	DESCRIPTION
15-12	Programmable Baud Rate Select Bits. When set, these bits choose a baud rate from 50 to 9600 or external. Bit 5 of XCSR register must be set and the baud rate enable straps for the PRINTER port or AUXILIARY port must be installed before these bits are enabled (see Section 2). Read/Write bits. Reading these bits will return the actual baud rate. If the programmable baud rate is disabled, the baud rate jumpers will be read.
11-8	NOT USED. Read as 0
7	Transmitter Ready. This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided bit 6 is also set. Set during power up sequence by DCOK. Cleared by writing into XBUF. Read-only bit.
6	Interrupt Enable. When set, allows an interrupt sequence to start when bit 7 is set. Read/write bit. Cleared by INIT.
5	Programmable Baud Rate Enable. Must be set for bits 15-12 to select the baud rate. Read/Write bit, cleared by INIT.
4-1	NOT USED. Read as 0.
0	Break. When set, a continuous space is transmitted across the RS-232-C interface, giving the receiver a framing error. Read/Write bit, cleared by INIT.

Register 6 - Transmit Data Buffer (XBUF)

BIT	DESCRIPTION
15-8	NOT USED. Read as 0.
7-0	Holds the character to be transferred to the external device. Data must be right-justified if the UART is strapped to less than 8 bits. Writing to this register initiates the transmit sequence. Write-only bits. Read as 0's.

LINE-TIME CLOCK (LTC) CONTROL

The Line-Time Clock (LTC) circuitry contains a control register and supporting logic to control the bootstrap/diagnostic PROM and the processor EVENT trigger line.

The logic is named after a characteristic of the EVENT interrupt line, which is triggered on the Utility board by a 60 Hz (square wave) signal derived from the 8501 power supply.

The EVENT interrupt provides a software facility allowing for real time clock applications. The presence of this signal is controlled by LTC bit 6. It is cleared (disabled) both by setting bit 6 to a zero, and/or during initialization (INIT).

Other active bits in the LTC register are: bit 5 - controlling the PROM address space (see "Diagnostic and Bootstrap PROM's"); bit 7 - to monitor the line frequency clock (see LTC Register bit definition); bit 0, which is a strappable option (P1036) for software diagnostic purposes; and bits 15-11 which drive five LED's used for diagnostic status reporting.

Line-Time Clock Status Register (Address = 177546)

BIT	DESCRIPTION
15-11	LED's on Utility board. These are used by the power-up self test to indicate errors and conditions (refer to Section 5 for the error codes). Writing a 0 to a bit turns on an LED. The Initialize condition sets all LED's ON. Writing a 1 turns it off. Write-only bits.
10-8	NOT USED. read as 0.
7	Monitor. Set to 1 by line frequency clock signal. Cleared by program. Read/Write bit. Writing a zero clears the bit, writing a 1 does not set it. Set by INIT, or line frequency clock.
6	Interrupt Enable. When 1, the line frequency clock signal asserts the BEVNT line. Read/Write bit. Cleared by INIT.
5	Diagnostic PROM Select. When 1, bootstrap PROM is located at addresses 173000 to 174776 (octal). When 0, diagnostic PROM is located at the same address space. Read/Write bit, Cleared by INIT.
4-1	NOT USED. Read as 0.
0	Strap selected logic level for diagnostic PROM control.

DIAGNOSTIC AND BOOTSTRAP PROM'S

These are two 1K-byte PROM's which are combined in parallel to provide 1K words of diagnostic and bootstrap memory. The diagnostic program provides the 8501 with a self-test feature and is entered automatically each time the system is powered up or the front panel restart switch is activated.

The bootstrap program is used to load the disc operating system into RAM. The bootstrap program is activated automatically on successful completion of the diagnostic program.

The diagnostic and bootstrap programs both utilize an address space of octal 173000 to 174776 (or approximately 1K bytes). Whenever the RESTART switch is activated, and during initialization, bit 5 of the LTC register is set to 0. This causes the diagnostic program to run starting at address 173000 (octal). One of the final instructions in the diagnostic program sets bit 5 of the LTC register to a 1, causing the bootstrap program to run (again starting at address 173000). The LTC control technique allows two programs (Diagnostic and Bootstrap) to share the same address at different times.

A strap is provided to disable the PROM and LTC functions. See Section 2 for the operation of this strap. The PROMs would have to be disabled if two Utility boards were installed in the same system for troubleshooting.

FRONT PANEL FUNCTIONS

The Utility board controls the system restart operation when restart (BDCOK(H) is activated by the front panel RESTART switch. It will force the processor to start execution at location 173000 (boot/diagnostic PROM address). The front panel board provides the debounce circuit for the RUN/HALT and RESTART switch. When the RUN/HALT switch is placed in the HALT position the processor will halt when the current instruction is completed. See Section 2 of this manual for the proper settings of the power-up/power-down and front panel power control jumpers.

Power Control

The Utility board contains the logic for selecting between internal (front panel), and external (any peripheral via Comm Adapter connector BNC 1) dc power control of the 8501. See Section 2 of this manual for power control options.

BUS TERMINATION RESISTORS

Each bus signal is terminated on the Utility board with a resistive divider network consisting of 180 ohms to +5 Vdc and 390 ohms to ground. DMA Grant (DMG) and Interrupt Acknowledge (IAK) lines are terminated with a resistive divider network consisting of 330 ohms to +5 Vdc and 680 ohms to ground.

DIAGNOSTIC STATUS INDICATION (LED'S)

The LEDs are viewed (with the top cover of the 8501 off) from the upper right side of the box (i.e. from the side opposite the disc drives). The LED closest to the front of the box is the most significant bit of the five. The following list (in octal) defines the meanings of the LED patterns if the processor halts:

37	unable to execute firmware
16	unable to complete initialization
00	error during RAM test
01	PROM error (low byte)
02	PROM error (high byte)
03	CPU error
04	line-time clock error
05	FD controller dead or missing
06	FD controller interrupt error
07	FD controller returned error status
11	monitor mode
12	bank-switching error
13	starting an operator-selected test
14	8501 COMM mode
10	trying to boot from a flex disc
30	waiting for a disc
31	executing secondary boot from disc
37	operating system running

The normal sequence that an observer will perceive is as follows, where * represents the LEDs that are lit:

```
*****   (from power-on till the firmware starts)
.....   (first 2 seconds after startup)
..***   (rippling through self-tests)
.*...   (trying the flex drives)
**...   (waiting for 6 seconds)
 .
 .      (repeat the last 2 steps until booted)
 .
**..*   (loading the operating system)
*****   (operating system running)
```

Section 10

I/O BOARD

INTRODUCTION

The I/O board performs the serial/parallel conversion for the high-speed interface port (HSI). Figure 10-1 depicts the overall functional layout of the board. The serial registers are shown in Fig. 10-2 and Fig. 10-3.

The address for the I/O serial interface may be located anywhere in Bank 7 (160000 to 177760). The address is selected with eight straps as described in Section 2 of this manual.

I/O BOARD POWER REQUIREMENTS

Voltage	Typical	Max
+5 Vdc	1.100 amps	1.750 amps

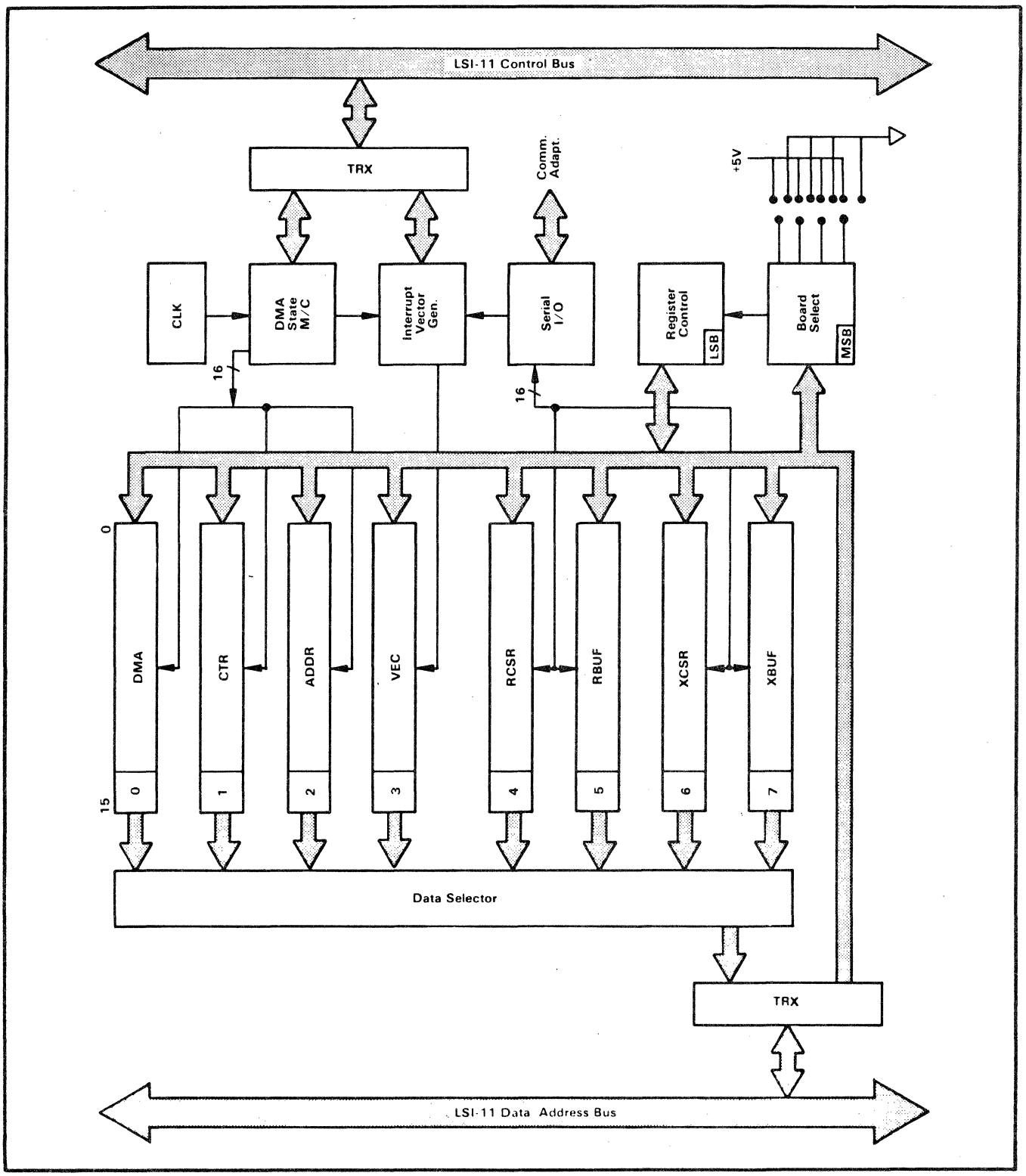


Fig. 10-1. I/O Board functional block diagram.

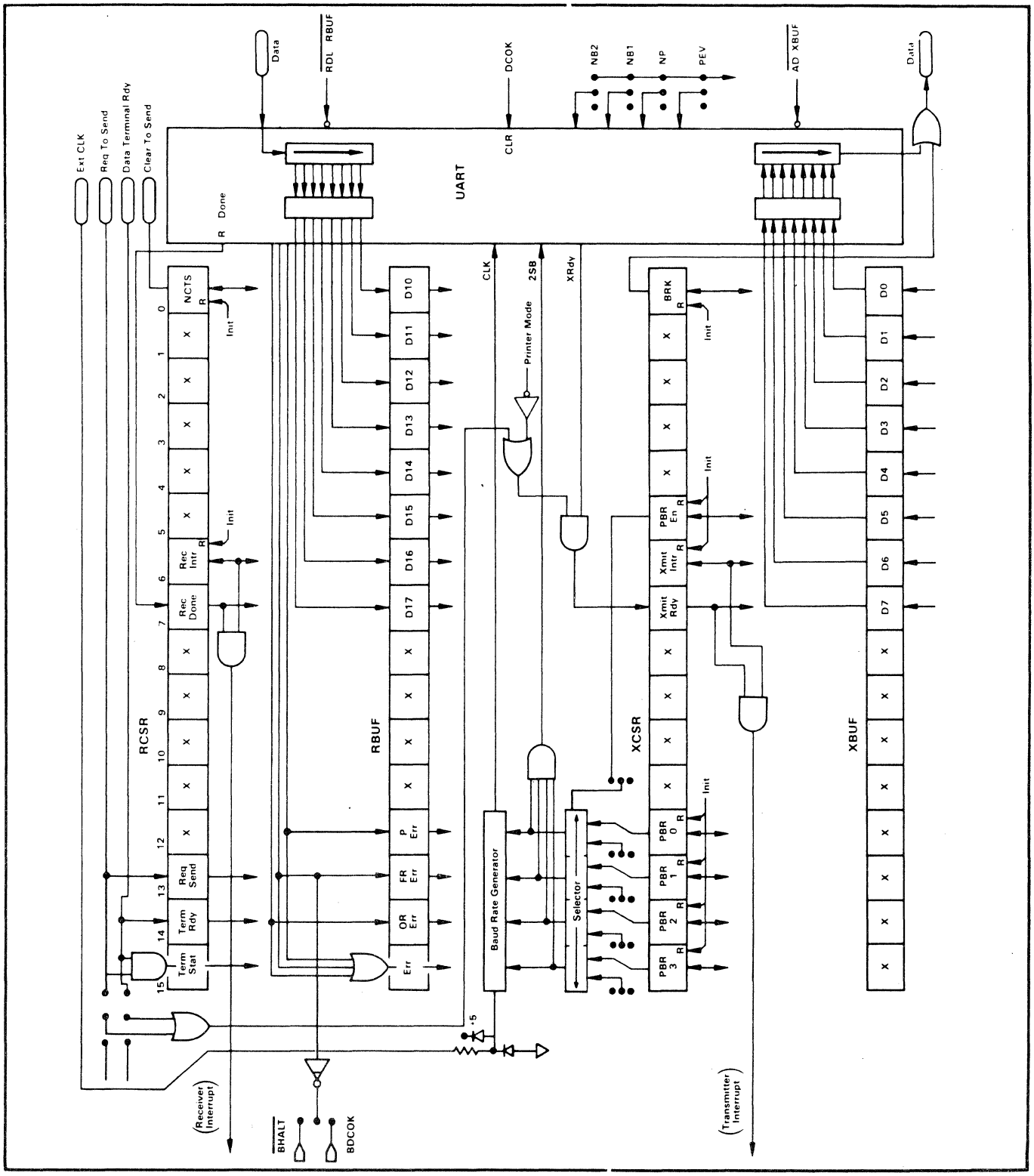


Fig. 10-2. High Speed serial interface registers.

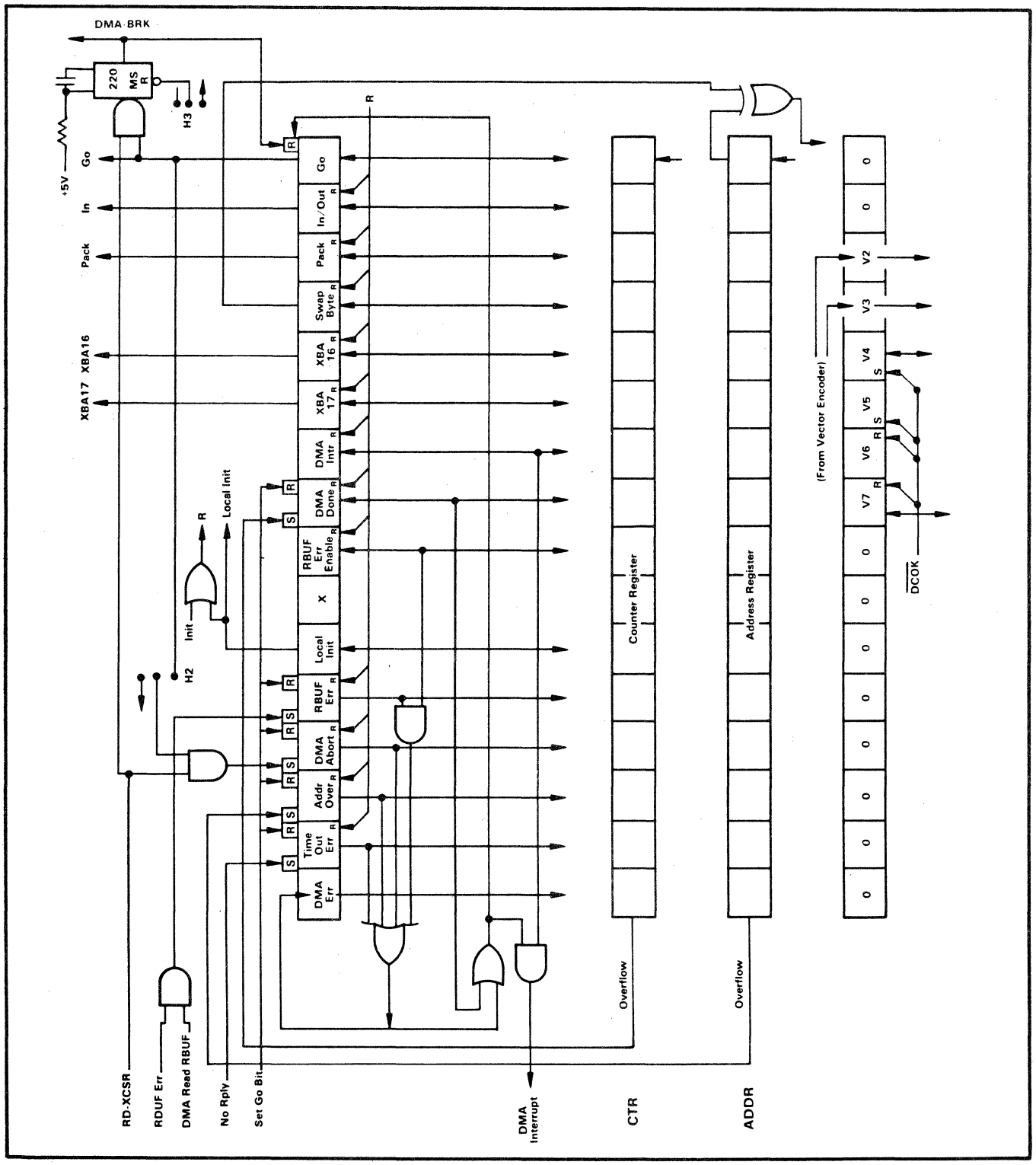


Fig. 10-3. Register contents.

INTERRUPT VECTOR ADDRESS

At system power-up, the I/O interrupt vector address is 060. Once the system is powered up, the I/O interrupt vector address may be changed under program control to any address within the range 000 to 360.

HSI DATA RATE

The HSI data rate is determined in one of two ways: a DMU supplied clock or an external clock. The DMU clock is located on the Comm Adapter board. The external clock must supply a TTL compatible signal whose frequency range may be between 0 and 2.5 MHz (156.25K baud). See Section 11 for Comm Adapter board internal baud rates.

DMA OPERATION

The memory starting address for DMA data transfers is specified by the LSI-11/2 processor. This address is contained in an 18 bit (extended range) starting address register. Two bits select the memory bank and 16 bits select the address within that bank. DMA data transfers are performed in blocks. The size of a data block may vary between zero and 65535 bytes. Sixteen bits are used to specify the block size. When the correct number of bytes have been transferred the I/O board will interrupt the LSI-11/2 processor. This interrupt informs the LSI-11/2 that the DMA operation is complete.

The DMA transfer may be made using unpacked, packed, or byte-swapping-packed modes. Mode selection is under program control. In the byte mode, the upper byte of memory is filled with the high byte (error bits) from RBUF and the transferred data is placed in the lower byte. When the packed mode is used, the first byte of data is placed in the lower byte and the second byte of data is placed in the upper byte of memory. Byte-swapping-packed operation just reverses the location of the high and low bytes of data.

INTERRUPTS

The I/O board will interrupt the LSI-11/2 processor under the following conditions:

a. Receiver buffer is full.

b. Transmit buffer is empty.

c. DMA operation is complete.

d. Error occurred during DMA transfer.

REGISTERS: CONTROL, STATUS, AND DATA.

Register 0 -- DMA Control/Status Register

BIT	DESCRIPTION
15	DMA ERROR (DERR) - This is the OR of bits 14, 13, 12 and 11 ANDed with bit 8.
14	TIME OUT ERROR (TOR) - This bit is set during a DMA cycle when a memory location does not respond to a read or write command within 10 microsecs. It is cleared when the GO bit is set of when Bus INIT or local INIT is asserted.
13	ADDRESS OVERFLOW ERROR (AOF) - This bit is set during a DMA cycle when the address register overflows and the counter is not at zero. It is cleared when the GO bit is set or when Bus INIT or Local INIT is asserted.
12	DMA ABORT (ABORT) - This bit is set during a DMA cycle if the XCSR buffer is read when strap H2 is in the 'B' position and GO = 1. It cleared when the GO bit is set or when Bus INIT or Local INIT is asserted.
11	READ BUFFER ERROR (RBE) - This bit is set if an error condition exists when the RBUF is read during a DMA cycle. It is cleared when the GO bit is set or when Bus INIT or Local INITR is asserted. This bit is used, when bit 8 is set, to abort the DMA operation. If bit 8 is not set, RBE indicates the presence of an error in the received DMA data block.
10	LOCAL INITIALIZE STROBE (INIT) - This bit is set only during the time it is being written to. When the write operation is completed this bit returns to a low state (0 logic level). Writing to this bit will initialize this interface to a known state. The counter, address, and interrupt vector are not affected.
9	NOT USED.
8	READ BUFFER ERROR ENABLE (RBEE). This bit is set by writing a 'one' to it. It is cleared by writing a 'zero' to it. Asserting Bus INIT or Local INIT will also clear it.
7	DMA OPERATION IS COMPLETED (DMA DONE) - This bit is set when the DMA operation reaches completion. It is cleared when the GO bit is set, or when Bus INIT or Local INIT is asserted.
6	DMA INTERRUPT ENABLE (DMA INTR ENBL) - This bit is set by writing a 'one' to it. It is cleared by writing a 'zero' to it or when Bus INIT or Local INIT is asserted. This bit is used to generate a interrupt when the 'DMA done' bit is set or DMA error bit is set.

4,5 EXTENDED ADDRESS BITS (XBA, 16, 17) - These bits are set by writing a 'one' to them. They are cleared by writing a 'zero' to them or when Bus INIT or Local INIT is asserted. These bits are used to select one of four memory pages during a DMA operation.

3 SWAP BYTE - This bit is set by writing a one to it. It is cleared by writing a zero to it or when Bus INIT or Local INIT is asserted. When packed mode is selected and this bit is a zero, the first byte of data is in the low memory byte and the second bye is in the high memory byte. When packed mode is selected and this bit is a one, the first byte of data is in the high memory byte and the second byte of data is in the low memory byte.

2 PACKED - This bit is set by writing a one to it. It is cleared by writing a zero to it or when Bus INIT or Local INIT is asserted. When transferring data to or from memory, if the packed bit is set, two bytes per word of memory are stored or read. The order of the bytes is determined by the swap byte bit. If the packed bit is zero, only the low byte of memory is read during OUT operations, and during IN operations the low byte will have the data byte stored in it and the upper byte will have the upper 8 bits of the RBUF stored in it.

1 IN/OUT (IN to memory, OUT from memory) - This bit is set by writing a 'one' to it. It is cleared by writing a 'zero' to it. This bit is used to control the direction of data flow during a DMA transfer.

0 ENABLE DMA (GO) - This bit is set by writing a 'one' to it. It is cleared by the following: A) writing a 'zero' to it, B) when the DMA is completed, C) when DERR (bit 5) is set, D) when Bus INIT or Local INIT is asserted.

Register 1 -- Counter for DMA Control (CTR)

BIT	DESCRIPTION

0-15 These bits are used as a 16 bit counter. This counter is set (under program control) to the 2's complement of the number of bytes being transferred this counter. When the counter overflows the DMA transfer is stopped.

Register 2 -- Address For DMA Control (ADDR)

BIT	DESCRIPTION
0-15	These bits are used as a 16 bit address pointer. This pointer (set under program control) points to the first location in memory to be used in the DMA data transfer. In the unpacked mode, this pointer will increment by two with each byte transferred. In the PACKED mode, this pointer will increment by one with each byte transferred.

Register 3 -- Vector For Interrupts (VEC)

BIT	DESCRIPTION
8-15	NOT USED
4-7	The interrupt vector address is under program control. These four bits are used by the program to specify the vector address within the range 000 to 360 (octal). These are both READ and WRITE bits. At system power-up or restart, the vector address is set to 60 (octal) by DCOK false. When DCOK becomes true, the vector address may be changed to any address within the above specified range.
2-3	These two read-only bits are encoded by the interrupt vector generator as follows:

Bit 3	Bit 2	Encoded Description
0	0	RCSR Interrupt Pending
0	1	XCSR Interrupt Pending
1	0	DMA Interrupt Pending
1	1	Not Defined - No interrupt Pending

0-1	These bits are always zero (0).

Register 4 -- Receiver Control Status Register (RCSR)

BIT	DESCRIPTION
8-15	NOT USED
7	RECEIVER DONE (REC DONE). This bit is set when a serial byte is received. It is cleared when RBUF is read, Bus DCOK is false, or assertion of Local INIT. This bit is used to signal that RUBF is ready to read.
6	RECEIVER DONE INTERRUPT ENABLE (DONE INTR ENBL). This bit is set when a 'one' is written to it. It is cleared by writing a 'zero' to it, or asserting Bus INIT or Local INIT. When this bit is set, REC DONE will generate an interrupt.
1-5	NOT USED
0	NOT CLEAR TO SEND (NCTS). This bit is set when a 'one' is written to it or a valid start bit is detected. It is cleared by writing a 'zero' or asserting Bus INIT or Local INIT or by reading the RBUF. This bit is transmitted on the interface bus to indicate that it is OK to send data.

Register 5 -- Receiver Data Buffer (RBUF)

BIT	DESCRIPTION
15	READ BUFFER ERROR (ERR). This is the logical 'OR' bits 14, 13, and 12. Bit 15 will be set if any of those bits are set.
14	OVERRUN ERROR (ORE) This is set if a second byte of data arrives before a previously received byte is read. It is cleared when another byte is properly received after the RBUF is read or when Bus DCOK is false or Local INIT is asserted. This bit signals that the previous unread byte was overwritten.
13	FRAMING ERROR (FE) This bit is set when a valid stop bit is not received after receiving a start bit. It is cleared when another byte is properly received, when Bus DCOK is false, or when Local INIT is asserted. This bit is used to signal when the transmitter has sent a BREAK.
12	PARITY ERROR (PE) This bit is set when a data byte is received with incorrect parity. It is cleared when a new data byte is received correctly. Bus DCOK is false or Local INIT is asserted. The UART may be strapped to ignore this bit (no parity).
8-11	NOT USED
0-7	RECEIVED DATA BYTE

Register 6 -- Transmit Control Status Register (XCSR)

BIT	DESCRIPTION
8-15	NOT USED
7	TRANSMIT BUFFER READY (XMIT RDY) This bit is set when RFD is true, the transmit latch is empty, and at least half of the previous byte is clocked out. It is cleared if any of the above conditions are not true, or if the GO bit is set and the HI strap is in the B position. This bit is used to signal when the XBUF can be loaded with a new byte of data.
6	TRANSMIT READY INTERRUPT ENABLE (XMIT INTR ENBL) This bit is set by writing a 'one' to its location. It is cleared by writing a 'zero' to its location, or asserting Bus INIT or Local INIT. This bit is used to enable the XMIT RDY interrupt.
1-5	NOT USED
0	BREAK This bit asserts the serial data line. It is set by writing a 'one' to its location, and cleared by writing a 'zero' to its location, or asserting Bus INIT or Local INIT. This bit is used to transmit a framing error (FE) to the serial interface receiver.

Register 7 -- Transmit Buffer (XBUF) Write-Only Register

BIT	DESCRIPTION
8-15	NOT USED
0-7	SERIAL OUTPUT DATA BYTE (Transmitter Data Byte)

Section 11

COMMUNICATIONS ADAPTER BOARD

INTRODUCTION

The Communications Adapter board (Comm Adapter) is a small circuit board mounted directly to the rear panel of the 8501 DMU (see Fig. 11-1). This unit serves as an interface and serial bus adapter for peripheral devices such as the TEKTRONIX 8301 Microcomputer Development Unit (MDU), line printers, terminals, etc. Altogether the Comm Adapter board has three bus sockets mounted to it (appearing through a rear panel plate) which form the HSI, PRINTER, and AUXILIARY ports.

SERIAL PORTS

The PRINTER and AUXILIARY ports are routed to the Utility board. They perform driver and receiver functions for RS-232-C communications only. The HSI port, which in addition to driver and receiver functions has a baud rate generator mounted integrally on the Comm Adapter board, is selectable for RS-232-C, RS-422 or RS-423 interface functions. The HSI port is routed to the I/O board.

The maximum internally generated baud rate for the two RS-232-C ports is 9600 baud. The maximum internally generated baud rate for the HSI port is 153.6K baud. The data rate of any of the ports may alternatively be controlled by external clocking up to a maximum rate of 20K baud (320 kHz).

All interface socket connections conform to standard EIA conventions. The connector pin configurations are detailed in Tables 11-1 and 11-2, and graphically illustrated in the functional block diagram of Fig. 11-2. Note that when the HSI port is strapped for RS-232-C operation, only the positive (+) side of the balanced signals depicted in Table 11-2 are used.

Table 11-1
AUXILIARY and PRINTER Port Connector Configuration

Pin Number	Description
1	Protective Ground
2	Receive Data
3	Transmit Data
4	RTS
5	CTS
6	DSR (Always on)
7	Signal Ground
8	Carrier Detect (Always On)
15, 17	External Clock
20	DTR

Table 11-2
HSI Port Connector Configuration

Pin Number	Description
1	Shield
7	Signal Ground
2	+ Received Data
11	- Received Data
3	+ Transmit Data
12	- Transmit Data
20	+ DTR
13	- DTR
5	+ CTS
25	- CTS
6	+ DSR (Always On)
18	- DSR (Always On)
8	+ CAR DET (Always On)
9	- CAR DET (Always On)
15	External Clock
17	External Clock

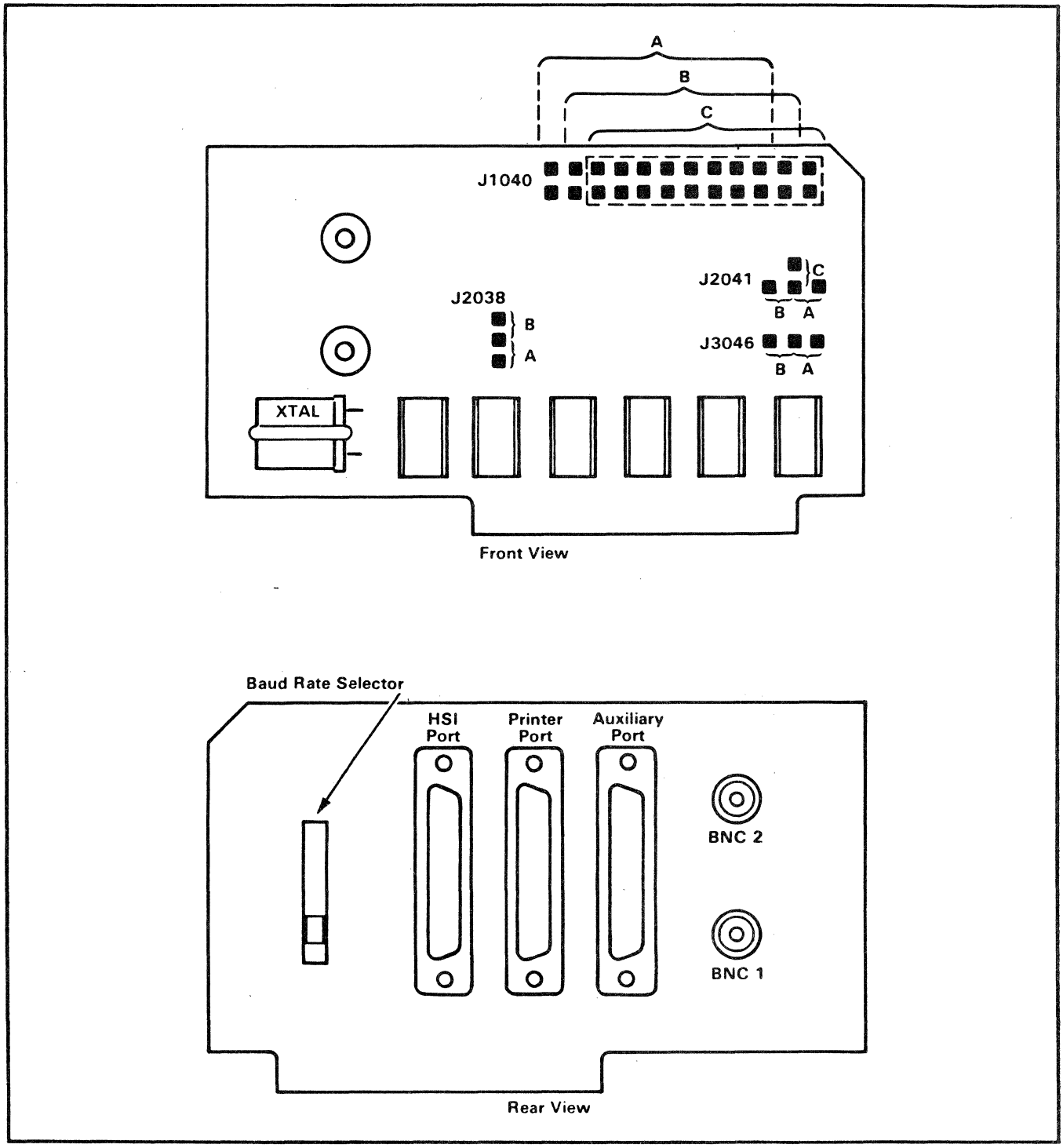


Fig. 11-1. Communications Adapter board.

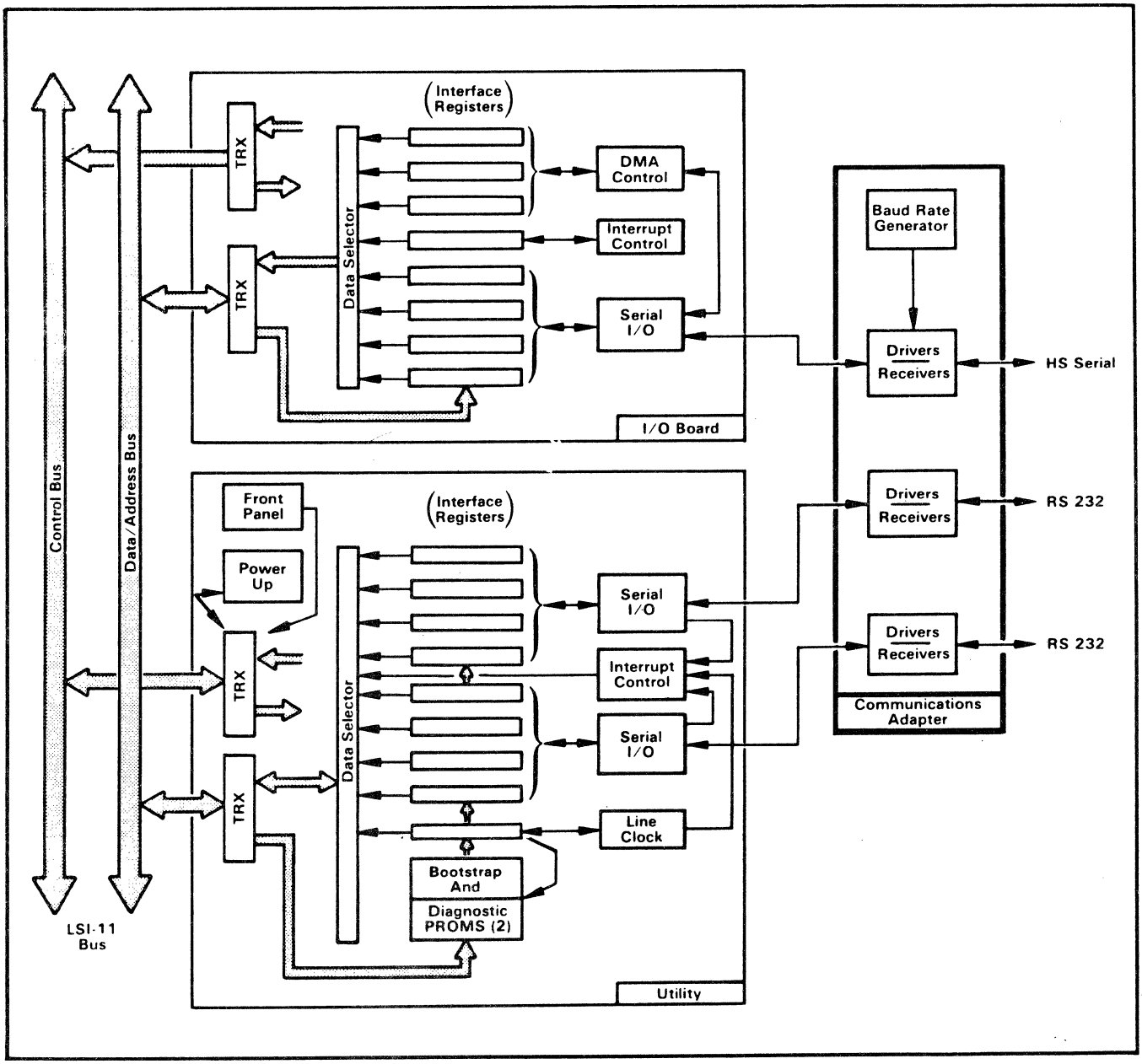


Fig. 11-2. Communications Adapter board block diagram.

REMOTE POWER CONTROL

The Comm Adapater board has two BNC connectors mounted adjacent to the rear panel I/O connectors. The BNC 1 (J154) connector is designed to receive a remote (DC) power control signal. The BNC 2 (J153) connector is designed to transmit a (DC) power control signal. The latter signal is an automatic product of DC power assertion in the 8501. Table 11-3 lists the signal conditions for these two remote power control connectors.

Table 11-3
Power Control Signal

BNC	Signal	Condition
J154 REMOTE IN	Open	8501 Power OFF
	Pulled down to < 0.5 volts	8501 Power ON
J153 REMOTE OUT	High Impendance	8501 Power OFF Indication
	TTL Low (sinks 16 mA)	8501 Power ON Indication

Section 12

FLEXIBLE DISC CONTROLLER

INTRODUCTION

The Flexible Disc Controller board controls the two flexible disc drives within the 8501. The controller formats, reads, and writes in IBM compatible single or double density format and on either signal or double sided diskettes.

FUNCTIONAL CHARACTERISTICS

The Flexible Disc Controller uses a Z80A processor, 1K byte of RAM and 4K bytes of ROM to control the flexible disc drives. Information is stored on the disc using write precompensation for track 43 or greater. Data stored on track 42 and below is not write precompensated. Figure 12-1 is a block diagram of the Flexible Disc Controller board.

INTERFACE REGISTERS

Eight registers control the operation of the Flexible Disc Controller. The locations of these registers are under program control, and may be anywhere in page zero of the system memory. Figure 12-2 illustrates the registers, and each is discussed in the following order:

1. Control Buffer Pointer Register (CBPR)
2. Flexible Disc Command Register (FDCR)
3. Word Count Register (FDWCR)
4. Disc Addresss Register (FDDAR)
5. DMA Address Register (FDDMAR)
6. Flexible Disc Error Register (FDER)
7. Flexible Disc Status Register (FDSR)
8. Flexible Disc Diagnostic Register (FDDR)
9. Flexible Disc Chain Address Register (FDCHR)

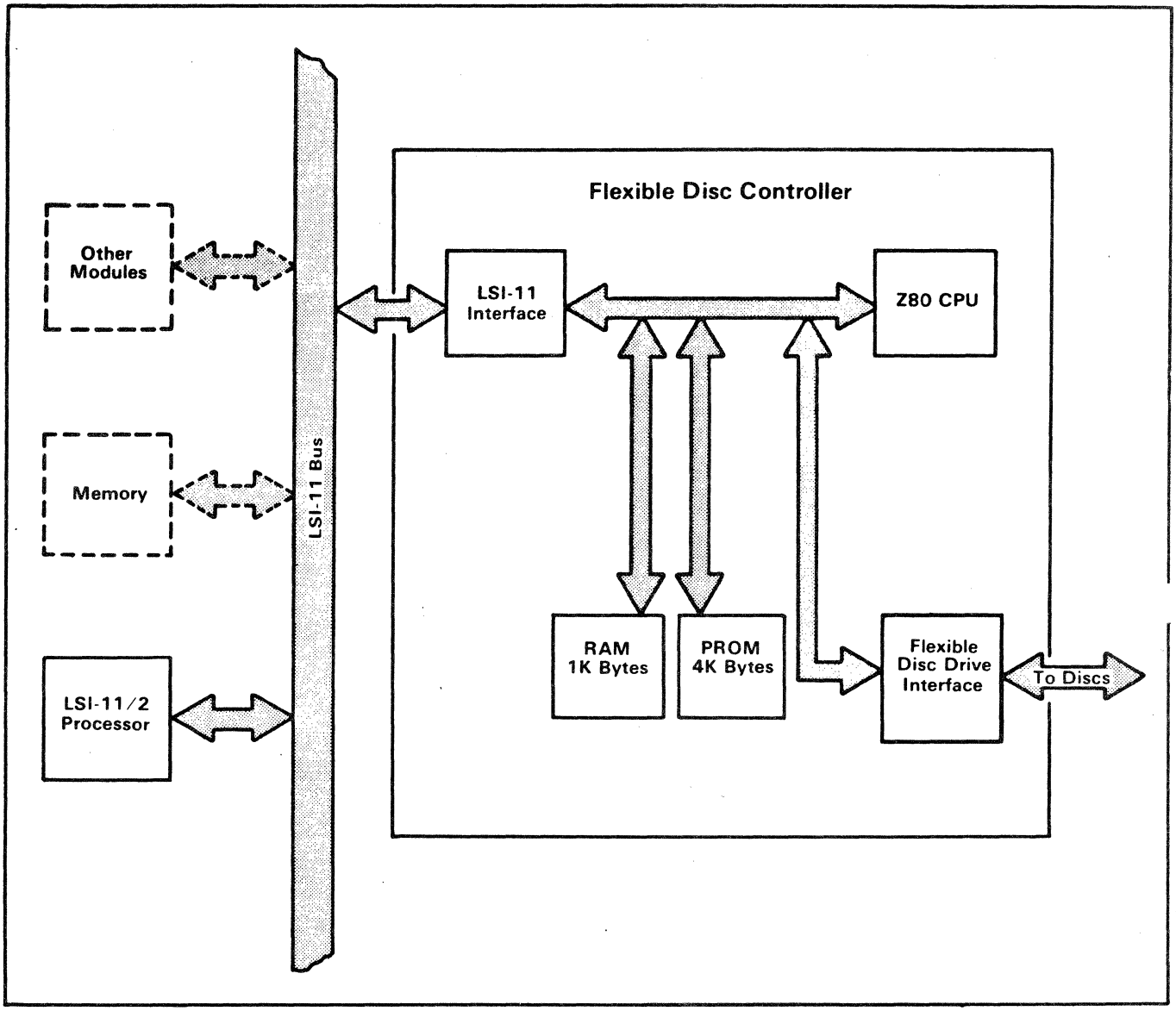


Fig. 12-1. Flexible Disc Controller block diagram.

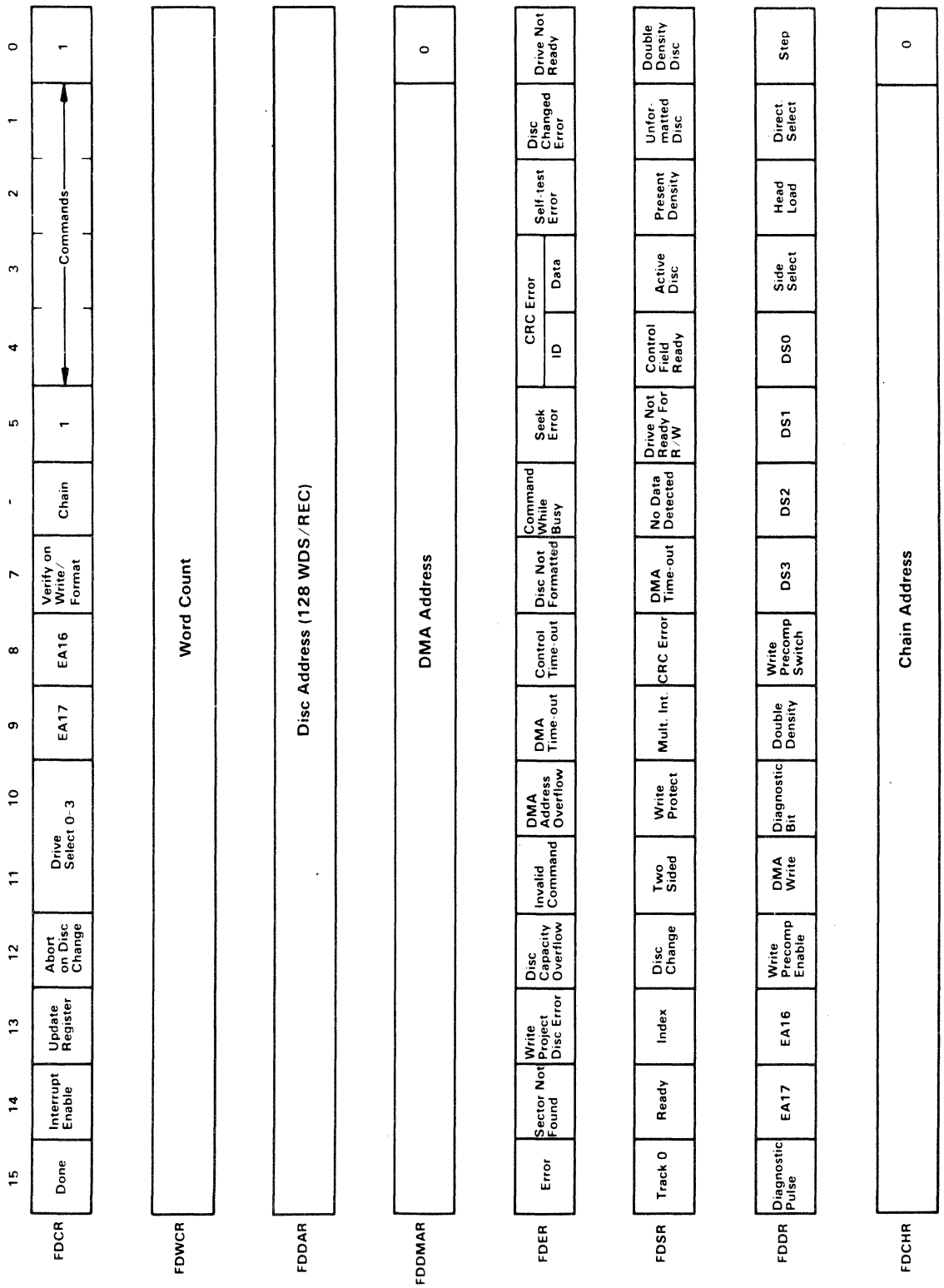


Fig. 12-2. Flexible Disc Controller Command and Status Registers.

Control Buffer Pointer Register -- CBPR

The content of the CBPR is used as a system memory pointer. The CBPR is located in bank 7 of system memory (LSI-11/2 I/O space), at address 177160. This pointer, set by the LSI-11/2, points to the starting address in system memory of the eight contiguous words representing the eight control registers. The Z80A processor is interrupted each time the LSI-11/2 processor writes to the CBPR. When the LSI-11/2 writes to the CBPR, the Z80A will begin executing the command contained in the Flexible Disc Command Register (FDCR). When the operation is completed, the disc controller will update the Error Register (FDER), the Diagnostic Register (FDDR), and the Status Register (FDSR). In addition, completion will set the 'Done' bit in the FDCR, and, if interrupts are enabled, will issue an interrupt to the LSI-11/2, with a vector address of 230. If the LSI-11/2 interrupt is disabled the LSI-11/2 may poll the DONE bit to know when the command has terminated.

Flexible Disc Command Register (address = CBPR)

The Flexible Disc Command register is used by the LSI-11/2 to specify the commands to be executed by the disc controller.

BIT	DESCRIPTION

15 DONE. This bit is set by the Z80A processor upon completion or termination of the current command. This bit is ignored by the Disc Controller when the command is issued, and is set to a '1' by the Disc Controller only on command completion. In order to give a valid 'Done' indication, it must be cleared (set to zero) by the LSI-11/2 processor before the command is issued.

14 Interrupt Enable. This bit is set to enable the Disc Controller to interrupt the LSI-11/2 upon completion of the current command. The interrupt vector is at 230. If the 'Chain' bit is set (bit 6 = 1), an interrupt will not occur unless a hard error occurs and FDCHR bit 0 is a zero.

13 Update Registers. When this bit is set the Flex Controller will update the FDWCR, FDDAR, and FDDMAR at the end of command execution as follows:

READ/WRITE/WRITE CONTROL FIELD/VERIFY: When the command terminates normally, FDWCR will be set to zero, FDDAR will point to the record following the one last operated on, and the FDDMAR will point to the word in LSI-11/2 memory following the one last read or written.

If the command terminates abnormally, the FDDAR will point to the record in which the error occurred, and the FDWCR and FDDMAR will be backed up to the start of the record.

FORMAT: If verify on Write/Format (FDCR bit 7) is 'zero', FDWCR is returned with 'zero'. If verify on Write/Format is a 'one', FDWCR is returned with the number of tracks with hard errors. In addition, FDDMAR will be unchanged, and FDDAR will be set to contain the number of the track following the last one formatted.

STATUS: The status command ignores the update register bit and always returns the registers as follows: The FDWCR is set to the version number of the firmware. Convert to decimal and divide by 100 to get the version number. The FDDMAR is set to zero, and the FDDAR is set to the capacity of the disc in the drive (capacity = the number of 256-byte records). If the drive is not is not ready or the disc is not formatted, the FDDAR is set to zero.

INITIALIZE: Sets all three registers to zero.

DIAGNOSTICS: Command dependent.

If the update registers bit is not set, the FDWCR, FDDAR, and FDDMAR will not be modified except by the status command.

12 Abort On Disc Change. This bit is set by the LSI-11/2 to enable aborting a command if the drive door of the selected drive has been opened since the last time the drive was selected. If this occurs, and the selected drive is ready, the current command will be aborted and the "Disc Changed Error" bit will be set.

11 Drive Select. These bits are set by the LSI-11/2 to specify the desired drive for the controller operation. The bits are encoded as follows:

Bits	11	10	Selected Drive
	0	0	Drive 0
	0	1	Drive 1
	1	0	Drive 2
	1	1	Drive 3

9-8 Extended Addressing. These two bits are set by the LSI-11/2 to specify the memory page (block) for DMA data transfers between memory and the controller. These bits, in conjunction with the FDDMAR, form a complete 18-bit effective address. The encoded description is as follows:

Bits	9	8	Page (Block)
	0	0	Page 0, Address 00K - 32K
	0	1	Page 1, Address 32K - 64K
	1	0	Page 2, Address 64K - 96K
	1	1	Page 3, Address 96K - 128K

7 Verify On Write/Format. This bit is ignored by all commands except Write, Write Control Field, and Format. This bit is set by the LSI-11/2 to request a verify operation for write and format commands. The written record is verified by checking for CRC errors on a subsequent read. If verification of a written record fails, the record is to be rewritten and reverified up to a total of 8 times. if all retries fail, a write command is aborted. A format command is not aborted if all retries fail, but the FDER register is updated to reflect the error condition. And, if the UPDATE Registers bit is set, the FDWCR register will contain a

count indicating the number of tracks with hard CRC errors found during the verify operation.

6 CHAIN. If this bit is set at the end of command processing, the contents of the FDCHR will be taken as a pointer to a new command buffer (replacing the CBPR) and the command will be executed. The CBPR, readable by the LSI-11/2 processor, is not changed. An interrupt is not issued if the CHAIN bit is set, but the command buffer registers are updated normally. If a hard error is encountered during a chained command sequence and bit zero of the FDCHR is a '0', the sequence is aborted (i.e. the chain bit in the command with the hard error is ignored). If the LSB of the FDCHR is a '1' a hard error will not abort a chained sequence. If a circular chain is executed, the only way to terminate command processing (other than with a 'Reset') is to issue another command (which will produce a 'command while Busy' error).

5-0 Commands: These bits are set by the LSI-11/2 to indicate to the disc controller the command to be executed. The following are valid commands.

BITS 5 4 3 2 1 0	OCTAL Value	Command
1 0 0 0 0 1	41	Read/Seek
1 0 0 0 1 1	43	Write
1 0 0 1 0 1	45	Verify
1 0 0 1 1 1	47	Format, Double Density
1 0 1 0 0 1	51	Format, Single Density
1 0 1 0 1 1	53	Status
1 0 1 1 0 1	55	Slow Status
1 0 1 1 1 1	57	Initialize
1 1 0 0 0 1	61	Write Control Field
1 1 0 0 1 1	63	Diagnostic

Read/Seek:. The data from the disc, as specified by FDWCR register and FDDAR register, is transferred to the memory. The memory page is specified by FDCR bits 8 and 9. The memory address is specified by FDDMAR. If the word count is zero (WCR - 0), a SEEK operation is performed. This advances the heads to the proper track, but does not transfer data, or verify proper head position. The following errors can occur during a Read/Seek operation, listed in the order of their possible occurrence. When a hard data field CRC error occurs, the bad record has already been read into memory.

1. Command while busy
2. Disc Changed
3. Drive not ready
4. Disc not formatted
5. Disc overflow
6. DMA overflow

NOTE

If any of the above errors occur, the command is aborted before seeking the proper track or transferring any data.

7. Controller time-out**
8. Seek error*
9. Sector not found*
10. ID field CRC error*
11. Data field CRC error*
12. DMA time-out

* If any of these conditions occur, the Flexible Disc Controller will re-attempt the operation, with the number of retries listed in the FDER description.

** A retry will occur if reading an ID field, but not if reading a data field.

Write:. The memory data specified by FDDMAR and FDWCR is transferred to the location on the disc specified by FDDAR. If the word count is zero (WCR=0), a SEEK operation is performed. If the FDWCR specifies a partial record write, the remainder of the record is filled with zeros. The following errors can occur during a write operation. They are listed here in the order of their possible occurrence.

1. Command while busy
2. Disc changed
3. Drive not ready
4. Disc not formatted
5. Disc overflow

6. DMA overflow

7. Write protected

NOTE

If any of the above errors occur, the command is aborted before seeking the proper track or transferring any data.

8. Controller time-out**

9. Seek error*

10. Sector not found*

11. ID field CRC error*

12. Data field CRC error (will occur only if FDCR bit 7 is set)*

13. DMA time-out

* If any of these conditions occur, the Flexible Disc Controller will re-attempt the operation, with the number of retries listed in the FDER description.

** A retry will occur if reading an ID field, but not if reading a Data field.

Verify:. This command verifies that the specified portion of the disc is formatted correctly. The action performed is the same as for a READ command except that the data read is not transferred to memory. The data read will include all CRC error checking and reporting.

If the FDWCR contains a minus one (WCR = 177777), the remainder of the disc will be verified, beginning with the record specified in the FDDAR. If the word count is zero (WCR=0), a SEEK operation is performed. The following errors can occur during a verify operation. They are listed here in the order of their possible occurrence.

1. Command while busy

2. Disc changed

3. Drive not ready

4. Disc not formatted

5. Disc overflow

NOTE

If any of the above errors occur, the command is aborted before seeking the proper track or verifying any data.

6. Controller time-out**
7. Seek error*
8. Sector not found*
9. ID field CRC error*
10. Data field CRC error*

* If any of these conditions occur, the Flex Controller will re-attempt the operation, with the number of retries listed in the FDER description.

** A retry will occur if reading an ID field, but not if reading a data field.

Format Single Density:. This command is issued by the LSI-11/2 when the specified tracks on the selected drive are to be formatted in IBM compatible 128 byte/sector single density format.

The data written into each sector is a sequence of eight bytes repeated through the sector. These bytes are: Track, 0, Side, 0, Sector, 0, Density, 0. Density is always 0 for single density.

FDWCR contains the number of tracks to be formatted starting at the track specified in the FDDAR. If the contents of the FDWCR, when treated as a 16-bit unsigned integer, are greater than or equal to the remaining number of tracks, the remainder of the disc starting at the track specified in the FDDAR is formatted. If FDWCR=0, a SEEK track is performed, with the additional action of making the controller think that the disc is formatted in single density, even if it is not formatted or is double density.

For a description of error handling and retries, refer to the description of FDCR bit 7 (Verify on Write/Format).

FDDAR contains the number of the starting track. A single-sided disc has 77 tracks (0-76), and a double sided disc has 154 tracks (0-153). The following is a list of possible errors.

1. Command while busy
2. Disc changed
3. Write-protected disc
4. Drive not ready
5. Disc overflow (starting track number not valid)

NOTE

If errors 1 through 5 occur, the command is aborted before seeking the starting track.

The following errors will occur only if verify after Write/Format is set in the FDCR. In the event of their occurrence, the disc controller will reformat and reverify the track until the verify is successful or eight attempts have been made.

1. Controller time-out
2. ID field CRC error
3. Data Field CRC error

Format Double Density. This command is issued by the LSI-11/2 when the specified tracks on the selected drive are to be formatted in IBM compatible 256 byte/sector double density format. Track 0, side 0 is formatted in IBM compatible 128 byte/sector single density (FM) format.

The data written into each sector is a sequence of eight bytes repeated through the sector. The bytes are: Track - 0, Side - 0, Sector - 0, Density - 0. Density is 0 on track 0, Side 0, (single density) and '1' elsewhere (i.e. remaining tracks are double density).

FDWCR contains the number of tracks to be formatted, starting at the track specified in the FDDAR. If the contents of the FDWCR, when treated as a 16-bit unsigned integer, are greater than or equal to the remaining number of tracks, the remainder of the disc, starting at the track specified in the FDDAR is formatted. If FDWCR=0, a SEEK operation is performed, with the additional action of making the controller think that the disc is formatted in double density, even if it is not formatted or is single density.

For a description of error handling and retries, refer to the description of FDCR bit 7 (Verify on Write/Format).

FDDAR contains the number of the starting track. A single-sided disc has 77 tracks (0-76) and a double-sided disc has 154 tracks (0-153). The possible errors are the same as specified for Single Density.

Status. The status command returns the disc capacity in the FDDAR. Disc capacities are:

- Single density, single sided: 1001 records
- Double density, single sided: 1989 records
- Single density, double sided: 2002 records
- Double density, double sided: 3991 records

If the disc is not formatted, or one on the following errors occur, the FDDAR will return all zeros.

The firmware version number is returned in the FDWCR. To get the version number, convert to decimal and divide by 100. The possible errors are:

1. Command while busy
2. Disc changed
3. Drive not ready
4. Disc not formatted (based on first four tracks searched only, - see "Slow Status" for full search).
5. Controller time-out
6. ID field CRC error

Slow Status. The slow status command causes the Controller to update all status registers by accessing every track until it finds one that is formatted which it will use to determine the disc density. If the disc is unformatted, it will be reported that way. The only difference between 'Status' and 'Slow Status', is the number of tracks examined to determine disc density.

Initialize. The heads of the drive selected by FDCR are moved to track 0, and the Disc Controller's internal track counter is reset. The "Track 00" signal from the drive is used to detect track 0, and no ID fields are read.

Initialize may be used to determine if a specific drive (0, 1, 2 and 3) is present in the system. If a 'self-test' error occurs, the drive is not present. Possible errors are:

1. Command while busy
2. Disc changed

Write Control Field. This operation is identical to the WRITE operation with the exception that a 'control field address mark' precedes the data field instead of a standard data address mark. This command is included because IBM format defines this type of data field.

Diagnostics. This indicates to the Z80A that a diagnostic command is contained in the WCR. Diagnostic commands are:

1. Diagnostic Read, Outside seek*
2. Diagnostic Read, Inside seek*
3. Diagnostic Write, Outside seek*
4. Diagnostic Write, Inside seek*
5. Load Z80A RAM
6. Execute Z80A RAM

* 'Inside' vs 'Outside' seeks refers to the direction from which the desired track is approached.

The register format of commands 1-4 is:

FDCR:	Diagnostic command
FDWCR:	Diagnostic command number
FDDAR:	Bits 7-0: Track
	Bits 8: Side
	Bits 9: Density (0 = Single, 1 = double).
	Bits 10: Write Pre-comp enable
	Bits 11: Write current switch enable
FDDMAR:	Two bytes of data for the 'Diagnostic Write' command (to write).

The 'Diagnostic Read' command seeks the track, and begins reading data (which it does constantly). Nothing is done with the data read from the disc.

The 'Diagnostic Write' command seeks the track and begins writing data (which is does constantly). The data written is from the FDDMAR, and the bytes are written alternately. 'Load Z80A RAM' loads from the LSI-11/2 (system) memory into the Z80A memory, starting at 2080 (hex) in the Z80A RAM. The maximum number of bytes which may be downloaded is 360 hex, (1540 octal, 864 decimal). No register update occurs. The register usage is:

FDDAR:	Byte count (Do not use zero, - valid registers in RAM will be lost).
FDDMAR:	Starting LSI-11/2 memory address.

'Execute Z80A RAM' takes the starting address from the FDDMAR. The routine is called with a 'Call' instruction, and upon exit, the command

buffer registers are updated as usual. If 'Updated Registers' (FDCR, bit-13) is set, this will cause an update to FDWCR, FDDAR, and FDDMAR.

Flexible Disc Word Counter (FDWCR) (address = CBPR + 2)

The Flexible Disc Word Count Register (FDWCR) is used to specify the number (Range = 0 to 32,768) of 16-bit words to be transferred during a DMA operation. A maximum of 32K words may be transferred from the same memory page during a DMA operation. Separate DMA data transfer commands must be used to transfer data from different memory pages. If 'Update Register' (FDCR bit 13) is set, a successful Read, Write, Verify, Format or Write Control Field operation will leave the FDWCR set to zero. Refer to the FDCR bit-13 description for further details.

BITS	DESCRIPTION
15-0	DMA word count.

Flexible Disc Address Register (FDAR) (address = CBPR + 4)

The Disc Address register is used by the LSI-11/2 processor to specify the record number of a selected drive to be used in a read, write, or verify operation, or the track number for a FORMAT operation. The valid number range for this register is from 0 to one less than the capacity of the disc. Disc Capacity is as follows:

1. Single Sided, Single Density = 1001 records
2. Single Sided, Double Density = 1989 records
3. Double Sided, Single Density = 2002 records
4. Double Sided, Double Density = 3991 records

NOTE

A record contains 128 words (256 8-bit bytes)

BITS	DESCRIPTION
15-0	Record number.

Flexible Disc DMA Address Register (FDDMAR) (address = CBPR + 6)

The DMA Address register is used by the LSI-11/2 processor to specify the system memory starting address for a DMA data transfer.

BITS	DESCRIPTION
15-0	These bits are used to specify the system memory starting address during a DMA operation. Bit 0 should be zero.

Flexible Disc Error Register (FDER) (address = CBPR + 8)

The Flexible Disc Error register is used by the LSI-11/2 to determine the response of the Controller and drives to commands issued by the LSI-11/2, and to ascertain drive status information. The FDER is updated by the Disc Controller at the completion of each command. Error processing will not abort execution of the command until a point is reached beyond which processing cannot proceed. e.g., disc capacity overflow and DMA address overflow may both be reported if both conditions are present.

BITS	DESCRIPTION
15	HARD ERROR. This bit is a cumulative error condition indicator. It is set by the Flexible Disc Controller when any of the following error conditions exist:

1. Write protected disc.
2. Disc capacity overflow.
3. Invalid command.
4. DMA address overflow.
5. DMA timeout.
6. Controller timeout.*
7. Disc not formatted.
8. Command while busy.
9. CRC error - ID field.*
10. CRC error - data field.*
11. Seek error.*
12. Self-test error.
13. Disc changed error.

14. Drive not ready.

15. Sector not found.*

* If a retry corrects this error, bit 15 is not set, and the error is a soft error (rather than a hard error).

14 Sector Not Found. This bit is set when the proper track and side are found and verified by an ID field, but the desired sector is not found. The Controller will reattempt twice to find the sector. Each (one) attempt consists of reading 26 ID fields.

13 Write Protected Disc Error. This bit is set by the Flexible Disc Controller if the selected disc drive is write protected and the command was "WRITE" or "FORMAT" or "WRITE CONTROL FIELD".

12 Disc capacity overflow. This bit is set by the Disc Controller when it is determined that the requested operation would cause the accessing of tracks outside the range of a disc of a specified drive (i.e. disc overflow). The current command will be aborted before any data is transferred.

11 Invalid Command. This bit is set by the Disc Controller when an invalid command is received from the LSI-11/2. Refer to bits 5-0 of FDCR for a list of the valid commands.

10 DMA address overflow. This bit is set by the Disc Controller when it is determined that execution of a DMA transfer would cause the memory address to increment location 177776 to 0 (i.e. 32K word memory page wrap-around). The current command will be aborted before any data is transferred.

9 DMA timeout. This bit is set by the Flexible Disc Controller when the memory fails to respond to a DMA request from the Disc Controller within 16 microseconds from the time the controller receives bus mastership. This will probably be caused by an attempt to reference non-existent memory.

8 Controller Timeout. This bit is set by the Controller when a disc write or read operation is not begun within the required time (0.33 sec. maximum timeout). The Controller will cause the head to step in or out one track, then step back one track. If looking for an ID field the operation is reattempted once. If in a data field no reattempts are made.

Read, Write, and Verify will report a Controller timeout if no data is detected (0.33 mSec max.) or the drive goes "not ready" during a read or write operation. FORMAT will report a Controller timeout only if the drive goes "not ready" while writing to the disc.

7 Disc Not Formatted. This bit is set by the Disc Controller if the selected ,disc drive is suspected to contain an unformatted disc when a command is issued.

6 Command While Busy. This bit is set by the Disc Controller when

the LSI-11/2 writes a value into the CBP register before the previous command has been executed by the Controller. The error is set in both the old and new command buffers. Both commands are aborted. Irrelevant data may be placed in the FDWCR, FDDAR, and FDDMAR by update Registers. Other registers should be unaffected (i.e. they should remain correct).

5 Seek Error. This bit is set when the Disc Controller track counter does not correspond to the track number written into the ID field of the track being read. The Disc Controller will do an INITIAlIZE (seek track 0), then reseek the desired track. Two reattempts will be made.

4 CRC Error - ID Field. This bit is set by the Disc Controller when a CRC error is detected in the process of reading a sector ID (CRC value is in the last two bytes of the ID field). The disc Controller will step in or out one track then step back and retry the read, up to a total of eight tries.

3 CRC Error - Data Field. This bit is set by the Disc Controller when a CRC error is detected in the process of reading a sector of data. The CRC value is in two bytes immediately following the data field.

NOTE

At the time this error is detected, and if the command is a 'Read', a record of "bad" data has already been transmitted to the LSI-11/2. The Disc Controller will step in or out one track, then step back and retry the read, up to a total of eight tries. (If the command is FORMAT with VERIFY, or WRITE with VERIFY, no attempts will be made to re-read the sector, but rather the data will be rewritten/formatted before a re-read is attempted).

2 Self-Test error. This bit is set by the Disc Controller if a hardware error occurs which is detectable by the Controller. Two errors are currently defined which will set this bit: One is when the Track 00 signal is never received from the drive after 76 steps outward. This condition may occur any time the controller attempts to step to track 0 in any command. The other error is when an interrupt is received by the Z80A and no bits are set in the interrupt status register.

1 Disc Changed Error. This bit is set by the Disc Controller to indicate that the disc drive door of the selected drive was opened since the last time it was accessed, if the "Abort On Disc Change" bit was set in the command register.

0 Drive Not Ready. This bit is set by the Disc Controller when any of the following conditions are present.

1. Disc not driven at required speed.
2. Drive door not closed.
3. No disc in the selected drive.
4. Drive not in system (two standard drives, two optional drives).

Flexible Disc Status Register (FDSR) (address = CBPR + 10)

The Flexible Disc Status register contains disc status information (This information is supplementary to that reported in the FDER). The FDSR is updated by the Disc Controller at the completion of each command. Bits 15-5 are copied from status registers DSR and ISR.

BITS	DESCRIPTION

15 Track 00. A status bit from the selected disc drive which is set to '1' when the Read/Write heads are positioned at track 0. It is used by the Z80A in any seek of Track 0 to detect track 0.

14 Ready. A status bit from the selected disc drive which is set to '1' when the selected disc is reporting 'Ready'. Used by the Z80A when checking for the "Drive Not Ready" error.

13 Index. A status bit from the selected disc drive which is set when the index hole is being sensed. The Z80A uses this bit when formatting a disc and to detect a controller timeout.

12 Disc Change. A status bit from the selected disc drive which is set when the drive is reporting that the disc has been changed since the last access. This bit is used by the Z80A to detect a Disc Changed Error.

11 Two Sided. A status bit from the selected drive. This bit is used by the Z80A to determine the sides/disc. A logic '1' (set) = two sided disc and a logic '0' (cleared) = single sided disc.

10 Write Protect. A status bit from the selected disc drive. This bit is used by the Z80A to detect a Write Protected disc.

9 Multiple Interrupt (Command While Busy) Used by the Z80A to detect a command while busy error, set by the hardware.

8 CRC Error. A status bit from the Disc Controller hardware. This signal is used by the Z80A to detect a CRC error in the ID field or the data field.

7 DMA Timeout. A status bit from the Disc Controller hardware. This signal is used by the Z80A to detect a DMA Timeout error.

6 No Data Detected. A status bit from the Disc Controller hardware. The Z80A uses this signal to detect a Controller Timeout Error.

5 Drive Not Ready For Read/Write. A status bit from the Disc Controller hardware which goes true if the drive goes not ready while the disc is being read or written. This signal is used by the Z80A to detect a Controller Timeout Error.

4 Control Field. Set by a read or verify command if a control address mark (written by a WRITE CONTROL FIELD command) is encountered anywhere during the read.

3 Active Disc (Drive Active) Set when the density of the disc in the selected drive is known. This bit and bit 1 (Unformatted Disc) are never both set.

2 Present Density. Always the same as bit 0 (double density disc) except for a double density disc on track 0, side 0, and which time single density is reported.

1 Unformatted Disc. This bit is set by the Disc Controller when a Read, Write, Verify, or Status operation is requested and readable data cannot be detected.

0 Double Density Disc. This bit is set by the Disc Controller to indicate the data encoding scheme used on the disc in the selected drive. This bit is a zero for single density (FM), and a '1' for double density (MFM).

Flexible Disc Diagnostic Register (FDDR) (address = CBPR + 12)

The Flexible Disc Diagnostic register is always updated at the completion of command processing, and is provided for board level testing. This register is not used in normal Controller operation. It contains flexible disc diagnostic information (control information for drives) consisting of two controller/drive registers.

BITS	DESCRIPTION

15 Diagnostic Pulse (returned zero).

14 EA17, Extended Addressing

13 EA16, Extended Addressing

12 Write precompensation enabled (set for Write, Write Control Field or Format is a Track 43 or greater).

11 DMA Write (always 'one' except for a Write or Write Control Field for which none of the first seven errors listed under the FDCR Write Command have occurred.

10 Diagnostic Bit (returned zero)

9 Double Density (should be the same as FDSR bit-2).

8 Write current switch (set for Write, Write Control Field, or Format if on track 43 or greater).

7 DS3, Drive Select

6 DS2, Drive Select

5 DS1, Drive Select

4 DS0, Drive Select

3 Side Select

2 Head Load

1 Direction Select

0 Step (returned zero).

For further details on FDDR bits 8-0, refer to "Outputs to the Drive" following the FDCHR description.

Flexible Disc Chain Register (FDCHR) (address = CBPR + 14)

This register is used only if the CHAIN bit in the FDCR is set. When the CHAIN bit in the FDCR is set, the FDCHR register will contain the address of the Command Buffer to be executed next.

If bit 0 of the FDCHR is zero, and the CHAIN bit is set, the chaining to the next command will not occur if a hard error has occurred. If bit 0 of the FDCHR is a one, chaining will occur independent of error status. Bit 0 is ignored and assumed to be zero for address of the next command buffer.

DISC DRIVE INTERFACE SIGNAL DEFINITIONS

The following text describes the disc drive control lines used by the Flexible Disc Controller. For more information on the drive, see the DataTrak 8 Flexible Disc Drive Service Manual.

NOTE

In the following definitions all drive input and output lines are 'Low True' on the controller/drive interface.

Outputs To The Drive

The first nine signals are returned in FDDR bits 8-0.

DRIVE SELECT 0-3. Four separate output lines are provided to select one of four drives in the system (two are standard). Additionally, the drive select signal will turn on the activity LED indicator in the door push button.

SIDE SELECT. This interface line is used to define which side of a two sided disc is used for reading or writing. A logical zero selects side 0, a logical one selects side 1.

DIRECTION SELECT. This interface line defines the direction of motion the R/W heads will take when the step line is asserted. A logical one defines the direction as "in" and the R/W head will move toward the center of the disc (high numbered track). A logical zero defines the direction as "out" and the R/W head will move away from the center of the disc.

STEP. A pulse on this interface line causes the R/W heads to move one track in the direction of motion defined by the "Direction Select" line.

HEAD LOAD. This interface line will load the R/W head against the disc of all drives. The head load signal also locks the drive door. The head load line is held true for 3 seconds after the last disc operation.

WRITE CURRENT SWITCH. This interface line is used to switch in 'Low Write Current' for track 43 and above.

WRITE DATA. This interface line supplies a 250 nSec wide pulse whenever a data or clock bit is intended to be written on the disc.

WRITE GATE. This interface line informs the drive unit that a 'Write operation' is in progress. This signal is ANDed with WRITE PROTECT to supply the write current.

Inputs From The Drive

TRACK 00. This interface signal is used to indicate when the drive's R/W head is positioned at track zero (the outermost track). A logical one indicates that the head is positioned at track zero.

INDEX. This interface signal is provided by the drive once each revolution of the disc (Approx. 166.7 mS) to indicate the beginning of the track (sector 1). Normally, this signal is in an unasserted state and makes the transition to the one state for a period of 1.8 mS once each revolution.

READ. This interface signal indicates that two index holes have been sensed and the drive spindle motor is at the correct speed after properly inserting a disc and closing the door.

WRITE PROTECT. This interface signal is provided by the drive to give the controller an indication when a write protected disc is installed. A logical one indicates that the disc is write protected. The drive will inhibit writing to a protected disc.

DISC CHANGE. This interface signal will indicate that a previously selected drive has gone from a "Ready" state to a "Not Ready" state while it was not selected.

TWO SIDED. This interface signal indicates whether a "two sided" or a "single sided" disc is installed. A logical one indicates that a "two sided" disc is installed.

READ DATA. This interface signal carries the incoming data stream from the diskette when WRITE GATE is inactive and the heads are loaded.

Section 13

POWER SUPPLY

INTRODUCTION

The material in this section consists of:

- o A list of power supply characteristics
- o A troubleshooting guide for the Power Supply
- o Bring-up procedure to return a repaired power supply to service.

POWER SUPPLY CHARACTERISTICS

Characteristic	Description
Line voltage range	The nominal voltages and their corresponding range are:

NOMINAL	RANGE
115 V	90 - 127 VRMS
230 V	180 - 250 VRMS

Line Frequency	50 Hz ± 1% or 60 Hz ± 1%
Power Consumption	360 Watts Max

Outputs:

Voltage Tolerance	Ripple, P-P**(a)	Max. Current	Min. Current(b)	O/V Protection(c)
+24 Vdc ± 5%	100 mV	2 A*	0.1 A	Yes
+12 Vdc ± 3%	120 mV	4 A*	0.1 A	Yes
-12 Vdc ± 5%	120 mV	540 mA	65 mA	No
+5 Vdc ± 5%	50 mV	20 A	6 A	Yes
+15 Vdc ± 10%	100 mV	20 mA	0 mA	Yes

* Output fused.
** Ripple and noise bandwidth to 1 MHz, measured at point of load.
(a) Worst case for line and load.
(b) For proper circuit operation.
(c) Supply shutdown type.
All outputs have overload and short circuit protection.

Line Protection (Located on Rear Panel)	
Low Line Range	6 amps
High Line Range	3 amps
Cooling	The DMU has one AC powered fan. This fan cools the power supply and other plug-in boards.
DC Power ON/OFF Options	*Front panel DC power switch enabled *Remote power enabled *Front panel OR remote power *Front panel AND remote power

TROUBLESHOOTING GUIDE

This sub-section is divided into two main parts as follows:

1. Major Failures
2. Minor Failures
    a. Finding what's wrong when the supply won't turn on.
    b. Troubleshooting the Secondary Regulators.

A block diagram of the 8501 power supply is shown in Fig. 13-1.

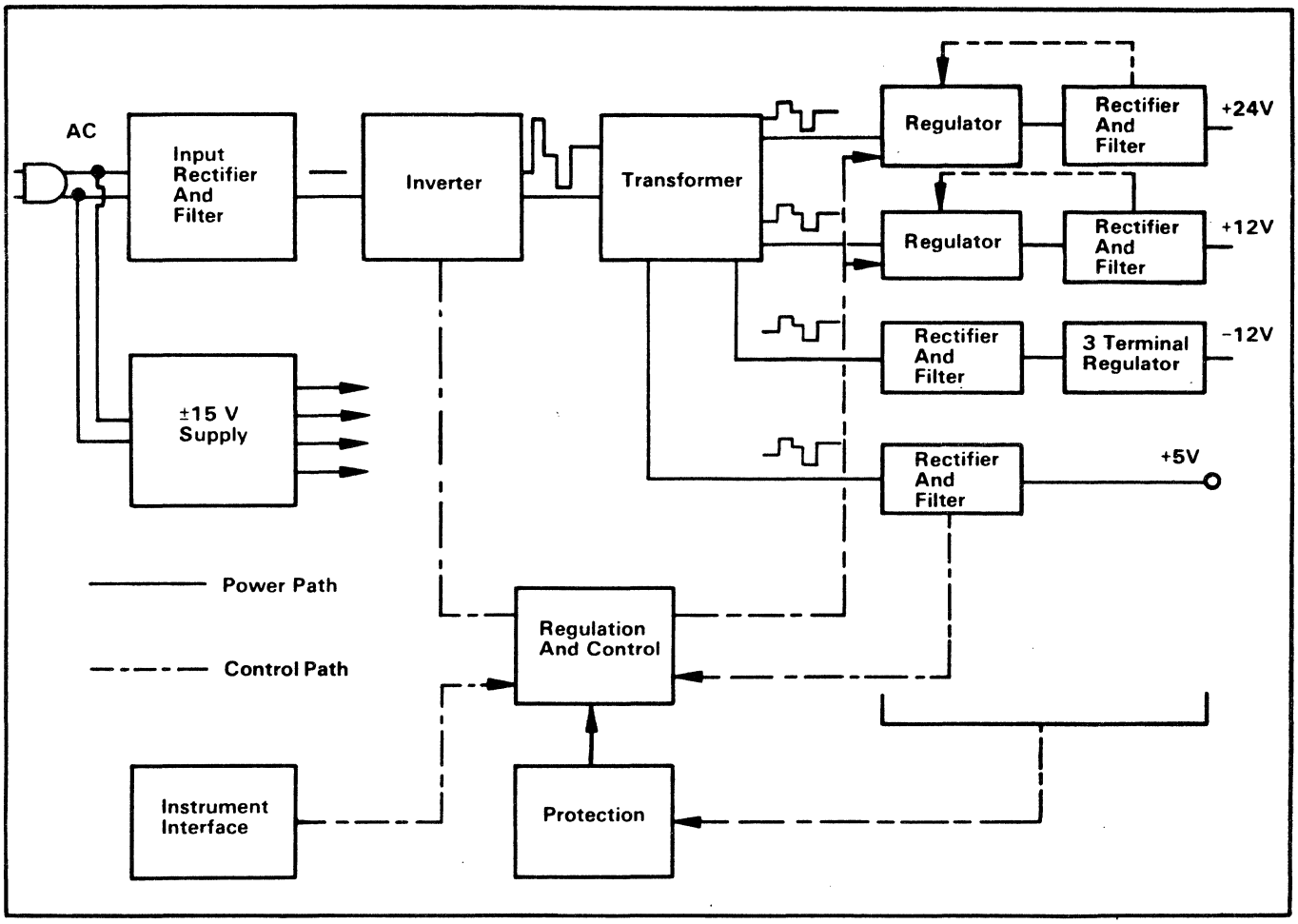


Fig. 13-1. 8501 power supply block diagram..

The following equipment is required to perform the tasks described in this section:

Equipment	Recommended Type
Needle Nose Pliers (2)	Sturdy, with plastic grips
Screwdriver	Phillips Type, medium size
Diode Meter	Fluke Model 8030A or equivalent
Oscilloscope	TEKTRONIX 400 Series (465 recommended) or equivalent.

Part 1 -- Major Failures

This type of failure will usually be accompanied by a burning odor and/or noise from the vicinity of the Power Supply circuit boards. The following inspection and repair procedure is patterned to follow the most likely causes of failure.

WARNING

Even with the Power Supply turned OFF, latent energy in the large capacitors of the Power Supply can cause severe burns and/or shock. Use insulated tools and probes at all times and heed the supplementary cautions contained in the text.

1. Make sure the instrument is disconnected from the power line.

2. Remove all eight screws holding the rear inspection panel in place. Note that the screw in the lower left hand corner is slightly longer than the others.

3. You may also want access to the top of the supply. For this, remove the top two rear corner stops, slide off the top panel, and remove the four screws holding the top shield. The shield may then be lifted off.

4. The inverter board is the lowest of the three boards visible in the rear opening. Remove it by inserting a sturdy pair of needle-nose pliers with plastic grips around the board under the small transformer to the left and pulling out firmly. Do not touch the metal on the pliers - high voltage may be present on the inverter board when it is plugged in. Once the board is removed, allow about five minutes for the capacitors on the board to discharge to safe voltages before handling the board. If desired a 220 ohm resistor can be used (with caution) to short the capacitor to ground.

5. Refer to the power supply schematics at the rear of this manual. On the Inverter board schematic, locate the main inverter circuitry. This is the circuitry clustered around Q2015 and Q3015.

6. Locate Q2015 and Q3015 on the board. They have black channel heat sinks attached.

7. Check the base-collector and base-emitter forward voltage drops of both transistors in circuit using the diode meter (see Fig. 13-2 for connections). In a good circuit, the base-collector voltage will be about 500 mV; and the base-emitter voltage will be about 130 mV (due to the 130 ohm resistor in a parallel DC path). After failure, however, both voltages will probably be about zero, indicating shorts.

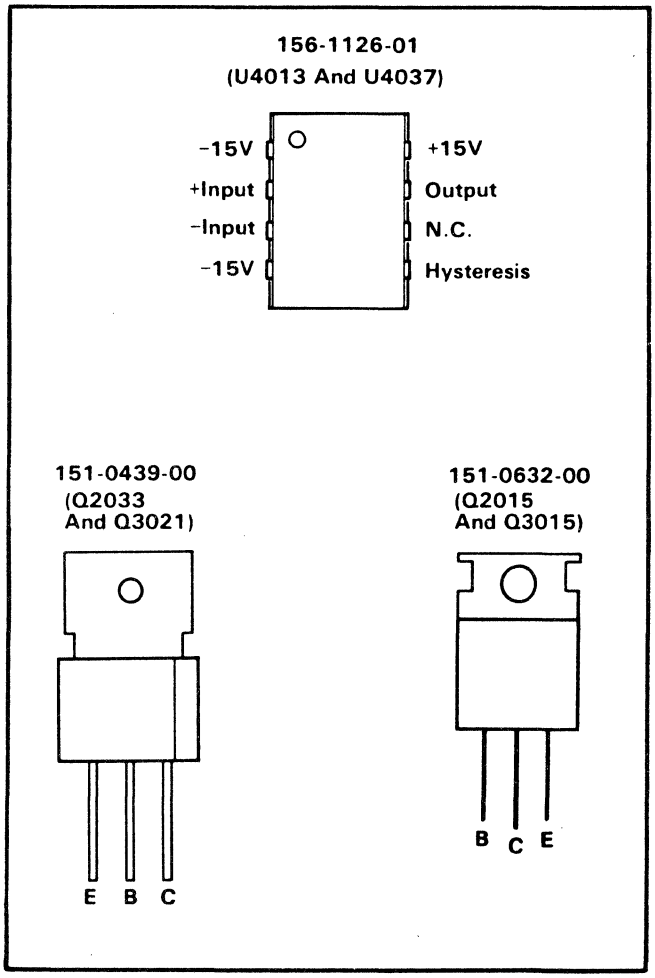


Fig. 13-2. Transistor Pinouts.

8. If either transistor shows a base-to-collector short, replace both the transistor and the heat sink. It is best to replace the heat sink since it usually gets damaged in the process of removing the transistor. To insert a transistor in a heat sink, place the heat sink on-end on a flat surface with the interior notch facing up. Apply thermally conductive grease to the mating surfaces. Insert the metal tab of the transistor into the notch as far as it will easily go. Now grasp the two channels of the heat sink with two pairs of needle nose pliers and bend them gently outward while forcing the transistor leads up against some overhanging projection. The plastic case of the transistor should seat neatly in the interior notch, with the hole in the transistor's metal tab surrounding the dimple in the heat sink below the notch. Be careful not to bend the channels outward too vigorously, since they may spring and lose their ability to hold the transistor in place.

After the appropriate transistors and heat sinks have been replaced, turn to the bring-up procedure.

9. If either Q2015 or Q3015 show a base-to-emitter short while in the circuit, remove it and check the associated CR2024/3012 with the diode meter. Be sure to check the diode in the forward, rather than the Zener direction. Either the Q2015/3015 base-emitter junction or the CR2024/3012 will be shorted. Also check the associated Q2033/3021 for base-emitter or base-collector shorts (see Fig. 13-2). This transistor has failed in about 20% of catastrophic inverter failures.

10. The capacitor and the other diodes associated with the faulty Q2015/3015 should also be checked for shorts.

11. After any defective components found in the previous procedure have been replaced, refer to the schematic of the Regulator board. Find diodes CR1043 and CR2041, connected to external lines BD1 and BD3 (pins R and S, respectively). Check the forward voltage drops of these diodes with the diode meter. They should be around 500 mV. Replace any diode which has a drop less than 400 mV, since some failures have caused one or both of these diodes to develop a low resistance parallel path.

Part 2 -- Minor Failures

The two most common minor (non-catastrophic) failures are failure of a secondary regulator to produce the correct output voltage and failure of the supply to do anything but chirp faintly every second or so when it should be on.

The Supply Won't Turn On.

1. Read and follow the first page of the Bring-Up Procedure, but exchange the Secondary and Regulator boards in their respective positions (slots).

2. Make sure the 8501 is turned OFF at the rear panel before plugging it into the power line.

3. Connect the external trigger input of the oscilloscope to the Shutdown testpoint (TP4062). The scope's timebase should be set to 10 ms/div initially. The triggering should be set to NORMal triggering, DC mode, EXTernal source, positive level, and negative slope.

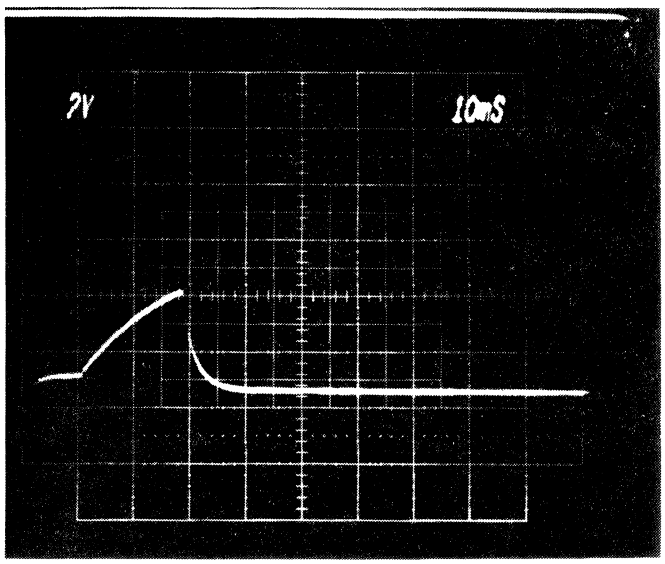
4. Turn the 8501 ON at the rear panel and at the switch labeled "DC" on the front panel. The supply should chirp faintly as it was doing before, and a single trace should be displayed on the scope with every chirp.

5. Set the scope's vertical sensitivity to 0.5 v/cm. Connect the vertical input of the scope to +5 V sense (TP4041) through a x10 probe. The two traces shown in Fig. 13-3 indicate the range of

expected waveforms. Trace #1 illustrates the "normal" chirp waveform.

If the waveform is like #2, slowing the sweep speed should reveal the fall of the voltage eventually. If at any time the voltage exceeds 5.3 V, the supply is probably being shut down by the overvoltage protection circuitry attached to the +5V output. The most likely cause is that the reference voltage has been set too high. Check this voltage by connecting a voltmeter between Vref (TP4078) and GND sense (TP4079). It should be 5.00 V, but any value between 4.75 V and 5.25 V is acceptable.

#1



#2

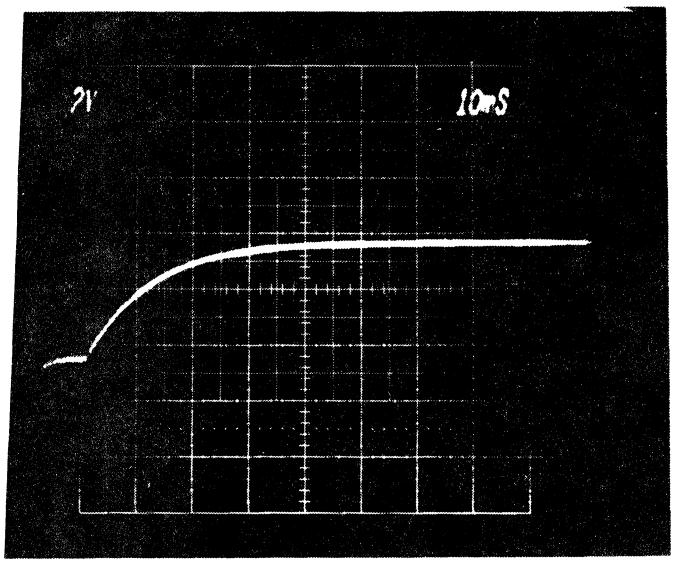


Fig. 13-3. Chirp Waveforms.

6. If the problem has not been found, connect the scope probe to +12 V sense (TP4012), +24 V (TP4031) and +15 V (TP4082) in turn. If the peak voltage on any of these lines is greater that 105% of the named voltage, the supply is probably being shut down because of it. Overvoltage on the +12 V or +24 V lines may be due to a faulty secondary regulator if the reference is set correctly (refer to Troubleshooting the Secondary Regulators).

7. If overvoltage does not seem to be the problem, there may be a short or overload on one of the supply outputs. Change the scope's vertical sensitivity to 50 mV/cm. Connect the scope probe to the ungrounded ends of the -12 V overcurrent sense resistor (R3026, 0.51 ohm), the +12 V overcurrent sense resistor (R3072, 0.1 ohm), and the +24 V overcurrent sense resistor (R2033, 0.2 ohm) in turn. All of these resistors are on the Secondary board. If the peak voltage across a resistor has a magnitude greater than .5 V, there is an overload on the corresponding output line. If not, there is probably an overload on the 5 V output line. The voltage across the +5 V overcurrent sense resistor (R2072, 0.005 ohms) may be measured with a differential amplifier, with the probe ground clips connected to ground, but since the signal level is so low -- 125 mV or so for an overcurrent condition -- it is likely to be lost in noise.

Troubleshooting the Secondary Regulators. The -12 V output is determined by a 3-terminal monolithic regulator; U1042 on the Secondary board. Any failure of regulation which is confined to this output is probably due to a failure of this component.

The +12 V and +24 V outputs are determined by similar switching regulators which are slaved to the +5 V regulator. They both have a switching transistor in the line running from ground to the center tap of the appropriate winding on the power transformer. This transistor in each regulator is driven by a comparator through a complementary emitter follower. The comparator generates a switching signal through comparison of Vref with the actual output voltage. Table 13-1 gives the circuit numbers for the relevant components in each regulator.

Table 13-1
Regulator Component Identification

		Secondary Board		Regulator Board
Regulator	Switching Transistor	Driver Transistors NPN	PNP	NE531
+12V	Q3072	Q3080	Q3078	U4037
+24V	Q2032	Q2044	Q2042	U4013

The two most common symptoms of failure in these circuits are overvoltage on the output (which would cause the supply to shut down), and insufficient voltage (usually less than half the proper value, even with light loads).

Output overvoltage is usually due to a collector-emitter short in the switching transistor. This short effectively removes the regulator from the circuit.

1. Check the base-collector and base-emitter forward voltage drops of the appropriate switching transistor, which should be about 500 mV.

2. Check for a collector-emitter short. - These measurements are easiest when made with the diode meter.

3. If the switching transistor is good, check the two driver transistors in the same way.

4. If the driver transistors are good, check the comparator while the circuit is running. A failure of this component usually shows up as an output that is incompatible with the inputs (for example, the positive input is above the negative input, but the output is low) or an input that is more than a few hundred millivolts above Vref.

The same procedure should be followed if there is insufficient voltage on the output. However, the most common causes of this problem are an open PNP driver transistor or an comparator that has failed (refer to Fig. 13-3).

BRING-UP PROCEDURE

Preconditions

The following preconditions are assumed:

- The rear, and if desired, the top power supply inspection panels have been removed.
- The circuits associated with both Q2015/3015 transistors on the Inverter board have been investigated for failures (per procedures outlined under "Major Failures"), and all discovered failed components have been replaced.
- The rear panel power switch is off, and the input capacitors (the large cans below the inverter board), have discharged to safe voltages. This occurs in the first five minutes following an AC power-down.
- The 8501's line voltage selector switch is set to the value of the supply and the power option. This value is shown in the text as: 115/230 VAC. It will be assumed that the rear panel

voltage selection, the supply and the power option agree at all times.

After checking all pre-conditions, refer to Fig. 13-4 and prepare the test set-up. For convenience, the following instrumentation (over and above that required for catastrophic failure procedures) is required:

Equipment

Isolation Transformer
Variac
Voltmeter
External Power Supply

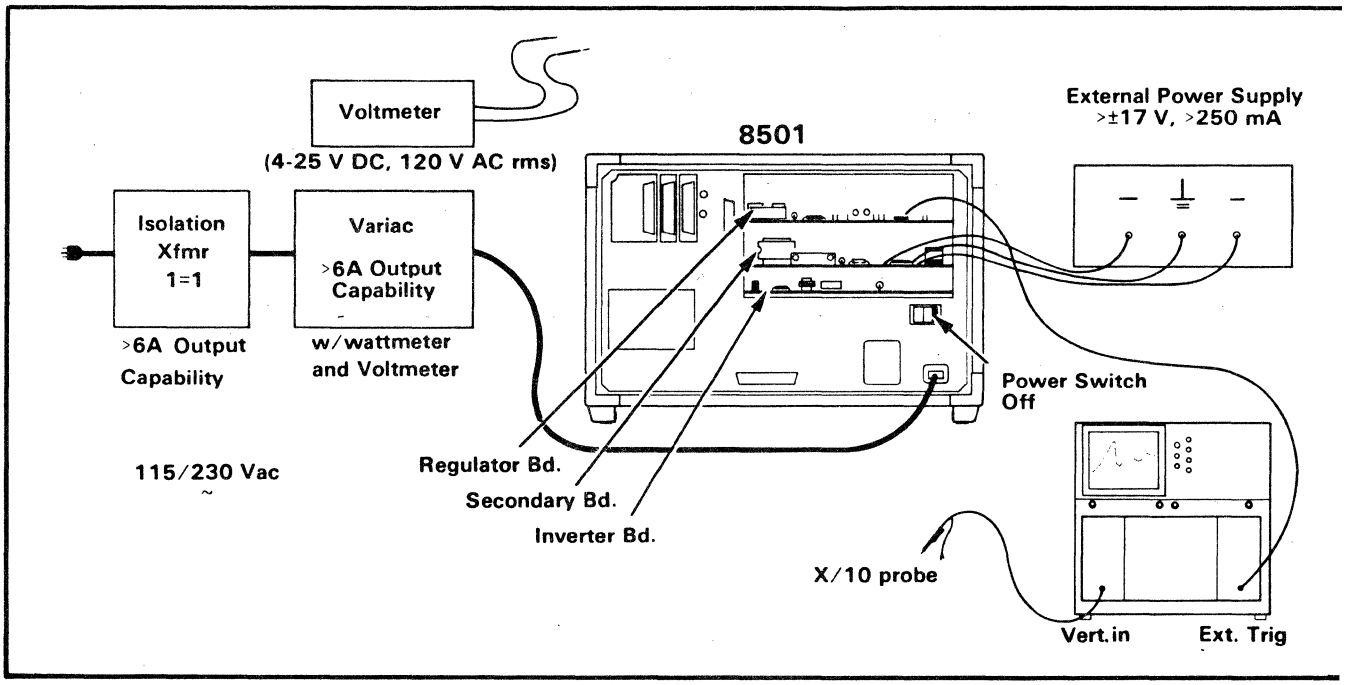


Fig. 13-4. Test equipment set-up.

After installing the test equipment check that all instrument fuses are good. This applies in particular to the Variac and the 8501 DMU.

WARNING

Even with the Power Supply turned OFF latent energy in the large capacitors of the Power Supply can cause severe burns and/or shock. Use insulated tools and probes at all times and heed the supplementary cautions contained in the text.

Procedure

1. Remove the Inverter board from its slot and plug the Inverter Extender board into the same slot. Then plug the Inverter into the Extender.

2. Make sure the external supply is OFF. Connect leads from the external supply through a 3-pin harmonica connector to the three square pins on the Secondary board (J3099). The connections should be to +Voltage, Ground, and -Voltage from left to right viewed from the rear of the instrument. The supply should be set between +17V and +40V. +20V is a nominal value.

3. Make sure there is a good Utility board and front panel in the system if the supply is being brought up in the instrument. The supply will not turn on if there is no Utility board in the leftmost card slot, viewed from the rear of the instrument.

4. With the rear panel power switch and the Variac power switch OFF, connect the 8501 power cord to the Variac and the Variac power cord to the line. Turn ON the external supply. Measure the voltage from the +15V test point (TP4082) to ground (TP4062) and from the -15V test point (TP4061) to ground (TP4063) on the Regulator board. If the measured voltages are not within 5% of the test point's assigned voltages, the standby regulators must be fixed before further testing is done. This circuitry is on the Secondary board. Make sure that the external supplies are not operating in a current-limited mode. The external supply current limits shoulw be greater than 250 mA each.

5. Measure the voltage from Vref (TP4078) to groundsense (TP4079). Adjust the trimmer pot on the Regulator board (R4076) until Vref is +5.00 V.

6. Remove the undervoltage shutdown jumper (J4081) from the Regulator board.

7. Connect the external trigger input of the scope to the Trigger test point (TP4081) on the Regulator board. The scope's timebase should be set to 20 us/cm. Be sure that the external trigger is selected.

8. Connect the vertical input of the scope through a X10 probe to the base of either Q2015/3015 transistors on the Inverter board. Connect the ground clip of the probe to the emitter of the selected transistor. Set the vertical sensitivity to .2 V/cm.

9. Push the front panel switch labeled "DC" so that the side nearest the green lamp (labeled "ON") is depressed. The scope should display the waveform shown in Fig. 13-5, or one shifted from this by 180 degree.

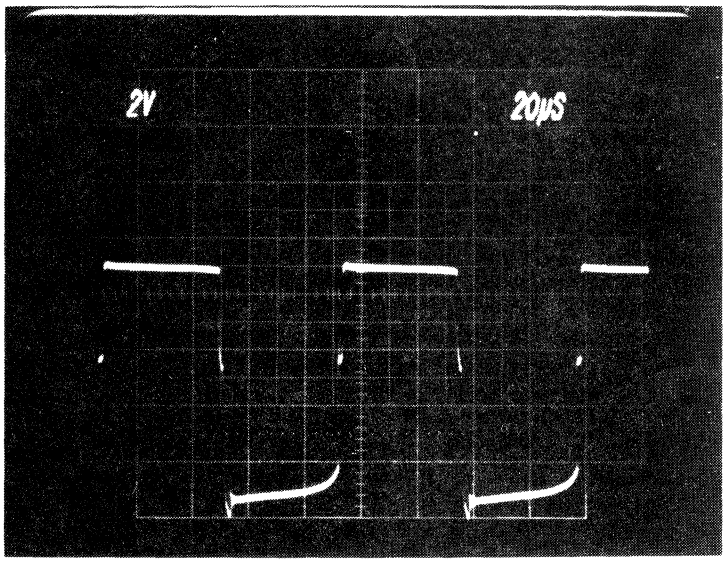


Fig. 13-5. Q2015/3015 base-emitter voltage waveform in Test Mode.

CAUTION

Don't operate the supply in this mode (that is, with the front panel switch on but green light off), for more than a few minutes at a time to prevent overheating Q2015/3015 on the Inverter board, especially if the variac is turned up.

If the waveform is correct, go to item 10.

If the voltage does not drop from 0.7V to -2V, and instead remains near ground or 0.7V until the -6.5V pulse, either one of the diodes around Q2015/3015 has failed, or the 220 uf capacitor has failed, or the associated Q2033/3021 has failed and was not replaced. Also check whether any of these components have been inserted backwards during repairs.

If the voltage remains near zero at all times or the waveform is otherwise distorted, the problem is probably on the Regulator board. Typical failures in order of frequency are:

- o One or both of the CR1043, CR2041 diodes.
- o One or both 151-0699-00's, usually as a collector - emitter short (Q2044, Q2054).

- o The Q20442 transistor.
- o The U2068 I.C.
- o The Q3064 transistor.
- o The U3044 I.C.
- o Either Q2053 or Q2052 whose bases are connected to the output of U3044.

10. Check the base-emitter voltage waveform on the other Q2015/3015. It should be identical in shape to that of the first transistor but shifted 180 degrees in phase. If the waveform does not meet this description, check for failures as outlined under item 9.

11. Both Q2015/3015 transistors should now exhibit correct base-emitter voltages. On the Inverter board connect the vertical input probe to PHOT (one convenient place is the collector of the Q2015/3015 nearest the edge connector) and its ground clip to PCAPS (at the junction of C2011/2035 which are the two large adjacent plastic film capacitors). Change the vertical sensitivity to 5 V/cm.

12. Make sure there is an adequate load on the 5V supply in the instrument. The two flexible disc drives and the Utility board,together with either the I/O or Flexible Disc Controller board, should be enough.

13. Turn the Variac output voltage control to zero. Switch ON the Variac and the 8501 from the rear panel.

14. Slowly rotate the Variac control until the output of the Variac is 20 or 30 Vrms. The waveform shown in Fig. 13-6 should now appear on the scope.

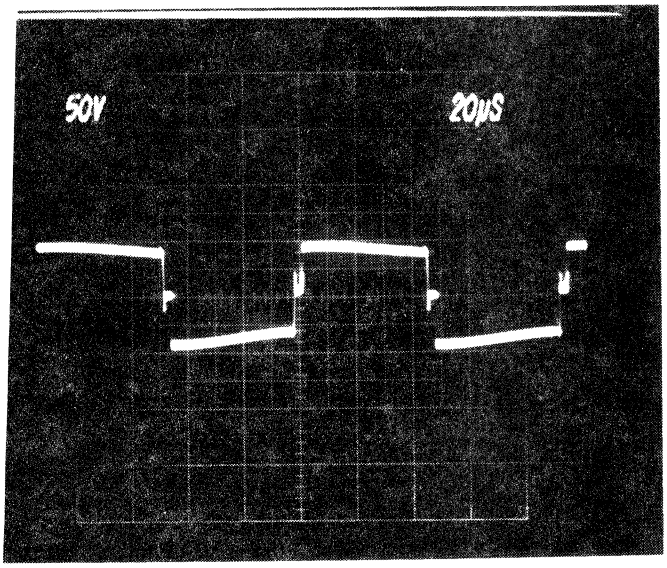


Fig. 13-6. Inverter Waveform - PHOT/PCAPS 1.

, The waveform amplitude should also rise freely with the rise of Variac output voltage. If the waveform is correct, go to item 15.

If the waveform is a square wave, the power transformer on the secondary board is not connected to the circuitry on the inverter board. If the waveform amplitude does not increase with Variac voltage, but stays near zero instead, and the Variac's wattmeter indicates a steady increase in power with rising output voltage, turn down the Variac immediately. There is probably a short across a secondary of the power transformer. This has been caused in the past by an internally shorted CR3032 diode (pair) packaged or a CR3032 whose case has shorted to its mounting bracket, which is ground. (CR3032 is the TO-3 case under the black plastic cover on the Secondary board.) If the voltage stays at zero, but the wattmeter indicates no increase in power, the line circuit to the 8501 is probably not complete. Check the Variac fuse the 8501's line fuse, and the thermal fuse on the Interconnect board (F6055).

15. Continue turning up the Variac voltage towards about 60 Vrms. The square portion of the waveform should become peaked just before it falls. If this is so, go to item 16.

If it rounds off instead of becoming peaked, one or both of the C2011/2035 capacitors have failed. Remove the probe from PHOT (Caution! High Voltage!) and, keeping the ground clip on PCAPS, attach the probe to the free end of either C2011/2035 capacitors. With the Variac set for 30-50 Vrms the voltage across the capacitor should be rounded everywhere, with a possible cusp or peak at one or two places.

If the waveform has any extended flat spots (larger than 50 us) the capacitor has failed and should be replaced. Repeat the test with the other capacitor. After finishing this step, replace the probe on PHOT.

16. Turn the Variac voltage quickly up to 90-100 Vrms. The supply may shut down for about a second, but when it comes on, the waveform on the scope should be stable and higher in frequency than the previous ones. (See Fig. 13-7).

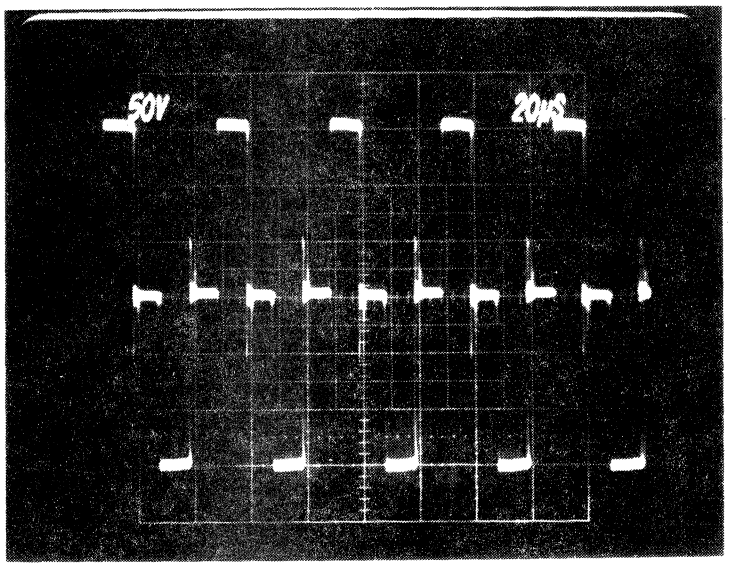


Fig. 13-7. Inverter Waveform - PHOT/PCAPS 2.

, If the waveform is correct, go to item 17.

If it is not, turn down the Variac immediately. Instability or failure to rise in frequency will usually be accompanied by an audible hissing from the supply. Instability has been caused by parasitic oscillation in the U3044 comparator on the Regulator board.

Failure to rise in frequency may be due to a failed U4062 operational amplifier on the Regulator board, or it may indicate that the 8501's line voltage selector switch is set to 230V. In any case, if the selector switch is set correctly, the fault is probably in the main regulation circuitry on the Regulator board.

If the supply fails to turn on, but continues chirping faintly every second or so, there is probably a short or overvoltage condition on one of the supply outputs. See "The Supply Won't Come Up".

17. Measure the voltage from +5V sense (TP4041) to GND sense TP4079). It should be 5.00V ± 5%. Leaving one lead of the voltmeter on GND sense, measure the voltage at +24V (TP4031), +12V sense (TP4012), and -12V (TP4011). All of the test points are on the Regulator board. The measured voltages should be between 22.8V and 25.2V, between 11.64V and 12.36V, and between -11.4 and -12.6V, respectively. If an incorrect voltage is found, see "Secondary Regulators" under "Non-catastrophic Failures".

18. Replace the Undervoltage shutdown jumper (J4081) on the Regulator board. Replace the voltmeter leads on +5V sense and GND sense test points. Turn the Variac voltage up to 132 Vrms and down to 90 Vrms. The waveform between PHOT and PCAPS should stay stable, and neither positive or negative peak should go over 200V. The voltmeter reading should remain within five percent of 5.00V.

19. Turn OFF the external power supply. The 8501 supply should stay on without change. Turn the Variac voltage below 90 Vrms until the supply shuts off. It should shut off around 80 to 85 Vrms. Turn the Variac voltage back up until the supply turns back on. This should occur below 90 Vrms, and the supply should turn on clearly, with only one chirp and no sputtering.

20. Check the overcurrent shutdown circuitry. Connect a 2 ohm resistor from the -12V test point (TP4011) to ground (TP4032). The supply should shut down immediately and chirp faintly every second or so until the resistor is removed. If it does not shut down, don't do any more overcurrent shutdown testing until this circuitry is fixed. If it does shut down, connect the resistor from +12V sense (TP4012) to ground. Then, connect the resistor from +24V (TP4031) to ground. In both cases, the supply should shut down and chirp until the resistor is removed. Finally, connect a 0.1 ohm resistor from the +5V power bus to ground near the edge connector on the Regulator board. The supply should shut down as in the other cases.

21. The fan and flexible disk drive motors should have been running at least since step 16. If they don't run, one of the U2070/3070 optocouplers on the Inverter board is probably defective. At this time, the AC RMS voltage from pin 6 to pin 4 of these optocouplers should be a few volts at most. If one of the voltages is near line voltage, the corresponding U2070/3070 is defective. If both voltages are half of line voltage, either both optocouplers are defective, or more likely, there is something wrong on the secondary side of the optocouplers. Once the motors are running, flip the front panel switch labeled "DC" back and forth a few times. The supply should turn off and on as a result.

WARNING

Even with the Power Supply turned OFF latent energy in the large capacitors of the Power Supply can cause severe burns and/or shock. Use insulated tools and probes at all times and heed the supplementary cautions contained in the text.

22. Turn OFF the 8501 from the rear panel. Unplug the 8501 and wait five minutes for the input capacitors to discharge to safe voltages (see Preconditions under first part of Bring-up Procedures). Then remove all probes from the supply boards. Remove the Inverter board and its extender and put the Inverter board into its edge connector. Be certain that the Secondary and Regulator boards are in the correct slots. Replace the top shield over the supply with its four screws. Replace the rear inspection panel with its eight screws. Replace any outside covers and feet that were removed from the instrument. The supply should now be perfect.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

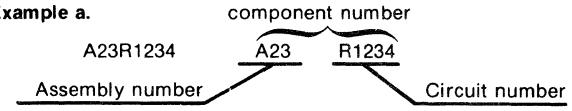
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

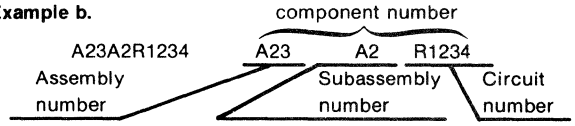
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000FJ	MARCOM SWITCHES INC.	67 ALBANY STREET	CAZENDIA, N.Y. 13035
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02111	SPECTROL ELECTRONICS CORPORATION	17070 EAST GALE AVENUE	CITY OF INDUSTRY, CA 91745
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14193	CAL-R, INC.	1601 OLYMPIC BLVD.	SANTA MONICA, CA 90404
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 F FAIRVIEW ST.	SANTA ANA, CA 92704
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27012	MICRO DEVICES, CORPORATION	1881 SOUTHLAND BLVD.	DAYTON, OHIO 45439
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32159	WEST-CAP ARIZONA	2201 E. ELVIRA ROAD	TUCSON, AZ 85706
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55210	GETTIG ENG. AND MFG. COMPANY	PO BOX 85, OFF ROUTE 45	SPRING MILLS, PA 16875
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72619	DIALIGHT, DIV. AMPEREX ELECTRONIC	203 HARRISON PLACE	BROOKLYN, NY 11237
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
87034	ILLUMINATED PRODUCTS INC., A SUB OF OAK INDUSTRIES, INC.	2620 SUSAN ST, PO BOX 11930	SANTA ANA, CA 92711
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-6226-00			CKT BOARD ASSY:SD BACK PLANE	80009	670-6226-00
A15	670-6237-00			CKT BOARD ASSY:SD PS CAPACITOR	80009	670-6237-00
A20	670-6233-00			CKT BOARD ASSY:SD PS INTERCONNECT	80009	670-6233-00
A22	670-6236-00	B010100	B010199	CKT BOARD ASSY:SD PS REGULATOR	80009	670-6236-00
A22	670-6236-01	B010200		CKT BOARD ASSY:SD PS REGULATOR	80009	670-6236-01
A24	670-6235-00			CKT BOARD ASSY:SD PS SECONDARY	80009	670-6235-00
A26	670-6234-00	B010100	B010199	CKT BOARD ASSY:SD PS INVERTER	80009	670-6234-00
A26	670-6234-01	B010200		CKT BOARD ASSY:SD PS INVERTER	80009	670-6234-01
A30	670-6232-00			CKT BOARD ASSY:SD PS FRONT PANEL	80009	670-6232-00
A40	119-1155-00			CKT BOARD ASSY:LSI 11/2	80009	119-1155-00
A50	670-6228-00			CKT BOARD ASSY:SD FLEX CONTROLLER	80009	670-6228-00
A60	670-6227-00			CKT BOARD ASSY:SD 32K MEMORY	80009	670-6227-00
A70	670-6229-00			CKT BOARD ASSY:SD I/O	80009	670-6229-00
A80	670-6231-00			CKT BOARD ASSY:SD UTILITY	80009	670-6231-00
A90	670-6230-00			CKT BOARD ASSY:SD COMM ADAPTER	80009	670-6230-00
A15	----- -----			CKT BOARD ASSY:SD PS CAPACITOR		
A15C1010	290-0885-00			CAP.,FXD,ELCTLT:1600UF,+50-10%,200V		
A15C1020	290-0885-00			CAP.,FXD,ELCTLT:1600UF,+50-10%,200V		
A15R1011	303-0623-00			RES.,FXD,CMPSN:62K OHM,5%,1W	01121	GB6235
A15R1012	303-0623-00			RES.,FXD,CMPSN:62K OHM,5%,1W	01121	GB6235
A20	----- -----			CKT BOARD ASSY:SD PS INTERCONNECT		
A20CR4065	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	80009	152-0574-00
A20CR4066	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	80009	152-0574-00
A20E6025	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	80009	119-0181-00
A20E6035	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	80009	119-0181-00
A20F6055	159-0125-00			FUSE,THERMAL:150 DEG C OPEN30A MAX,AX LDS	27012	4300A
A20Q4024	151-0190-00			TRANSISTOR:SILICON,NPN	07263	SO32677
A20R4035	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R4037	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R4046	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A20R6015	307-0353-00			RES.,FXD,FILM:5 OHM,10%,DISC	15454	5DA5RO-K-270SS
A20R6045	307-0353-00			RES.,FXD,FILM:5 OHM,10%,DISC	15454	5DA5RO-K-270SS
A20VR4036	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A20W1065	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A22	----- -----			CKT BOARD ASSY:SD PS REGULATOR		
A22C1033	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A22C1040	290-0307-00			CAP.,FXD,ELCTLT:100UF,+75-10%,40V	56289	600D107G040DG4
A22C1071	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	72982	8035D9AADX5R102M
A22C2034	290-0747-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	500D148
A22C2036	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A22C2091	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	72982	8035D9AADX5R102M
A22C3014	290-0818-00			CAP.,FXD,ELCTLT:390UF,+100-10%,40V	56289	672D397H040DS5C
A22C3041	281-0756-00			CAP.,FXD,CER DI:2.2PF,0.5%,200V	72982	0314022C0K0229D
A22C3043	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A22C3055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A22C3063	285-1049-00			CAP.,FXD,PLSTC:0.01UF,1%,200V	14752	230B1C103F
A22C3073	283-0179-00			CAP.,FXD,CER DI:0.68UF,10%,100V	72982	8151N150 C684K
A22C3076	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	72982	8005H9AADW5R472K

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A22C3080	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	72982	8141N037Z5U0225
A22C3081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C3083	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C3085	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C3087	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4010	285-1082-00			CAP.,FXD,PLSTC:0.47UF,20%,200V	14752	230B1C474
A22C4012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4014	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4020	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	72982	8141N037Z5U0225
A22C4021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4027	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4032	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A22C4036	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4040	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A22C4042	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	72982	8141N037Z5U0225
A22C4046	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4047	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4052	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A22C4055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4056	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4061	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	72982	835-515B102K
A22C4063	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104
A22C4063	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A22C4071	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	72982	835-515B102K
A22C4072	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	72982	8035D9AADX5R102
A22C4075	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A22CR1043	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A22CR1056	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR1071	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR1072	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR1091	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2041	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A22CR2051	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2052	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2062	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2065	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2084	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2085	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR2094	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR3052	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR3053	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR3057	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR3058	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR3075	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4045	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4047	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4053	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4060	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4061	152-0141-02	XB010200		SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4070	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4081	152-0141-02	XB010200		SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4082	152-0141-02	XB010200		SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22CR4083	152-0141-02	XB010200		SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A22F3010	159-0015-01			FUSE,CARTRIDGE:3AG,3A,250V,FAST-BLOW	71400	GJV3
A22F3034	159-0152-00			FUSE,WIRE LEAD:5A,125V,FAST BLOW	75915	275-005
A22L1011	108-0975-00			COIL,RF:FIXED,520UH	80009	108-0975-00

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A22L2022	108-0977-00			COIL,RF:FIXED,105UH	80009	108-0977-00
A22L2026	108-0556-00			COIL,RF:12UH	80009	108-0556-00
A22L3035	108-0556-00			COIL,RF:12UH	80009	108-0556-00
A22Q2042	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A22Q2044	151-0699-00			TRANSISTOR:SILICON,NPN	12969	U2TA508
A22Q2052	151-0302-00			TRANSISTOR:SILICON,NPN	07263	SO38487
A22Q2053	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A22Q2054	151-0699-00			TRANSISTOR:SILICON,NPN	12969	U2TA508
A22Q2056	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A22Q2080	151-0190-00			TRANSISTOR:SILICON,NPN	07263	SO32677
A22Q3051	151-1108-00			TRANSISTOR:FE,N-CHANNEL,SILICON	80009	151-1108-00
A22Q3064	151-0190-00			TRANSISTOR:SILICON,NPN	07263	SO32677
A22Q3065	151-0302-00			TRANSISTOR:SILICON,NPN	07263	SO38487
A22Q3066	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A22Q3074	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A22Q4050	151-0190-00			TRANSISTOR:SILICON,NPN	07263	SO32677
A22Q4061	151-0190-00	XB010200		TRANSISTOR:SILICON,NPN	07263	SO32677
A22Q4072	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A22R1050	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R1077	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A22R2011	301-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.50W	01121	EB2025
A22R2044	301-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.50W	01121	EB2025
A22R2045	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A22R2046	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A22R2047	315-0134-00	B010100	B010199	RES.,FXD,CMPSN:130K OHM,5%,0.25W	01121	CB1345
A22R2047	315-0103-00	B010200		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R2050	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2061	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2063	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2064	315-0103-00	B010100	B010199	RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R2064	321-0289-00	B010200		RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A22R2066	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2069	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2070	321-0333-00			RES.,FXD,FILM:28.7K OHM,1%,0.125W	91637	MFF1816G28701F
A22R2071	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2073	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2074	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R2076	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A22R2083	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A22R2092	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A22R2094	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A22R2095	321-0343-00			RES.,FXD,FILM:36.5K OHM,1%,0.125W	91637	MFF1816G36501F
A22R2096	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A22R2097	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R3011	301-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.50W	01121	EB3325
A22R3012	301-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.50W	01121	EB5115
A22R3040	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A22R3041	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A22R3042	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A22R3045	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A22R3046	321-0188-00			RES.,FXD,FILM:887 OHM,1%,0.125W	91637	MFF1816G887R0F
A22R3054	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A22R3056	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A22R3059	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A22R3060	301-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.50W	01121	EB2025
A22R3061	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A22R3062	307-0105-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.25W	01121	CB39G5

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A22R3070	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A22R3071	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A22R3077	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A22R3078	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A22R3082	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R3084	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A22R3090	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A22R3091	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A22R4021	321-0328-00			RES.,FXD,FILM:25.5K OHM,1%,0.125W	91637	MFF1816G25501F
A22R4023	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A22R4025	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A22R4026	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A22R4030	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A22R4031	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A22R4033	321-0301-00			RES.,FXD,FILM:13.3K OHM,1%,0.125W	91637	MFF1816G13301F
A22R4034	321-0377-00			RES.,FXD,FILM:82.5K OHM,1%,0.125W	91637	MFF1816G82501F
A22R4041	301-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.50W	01121	EB5115
A22R4043	321-0339-00			RES.,FXD,FILM:33.2K OHM,1%,0.125W	91637	MFF1816G33201F
A22R4044	321-0301-00			RES.,FXD,FILM:13.3K OHM,1%,0.125W	91637	MFF1816G13301F
A22R4048	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A22R4050	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A22R4051	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A22R4052	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A22R4054	315-0681-00	B010100	B010199	RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A22R4054	315-0471-00	B010200		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A22R4055	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A22R4060	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R4061	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A22R4062	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A22R4063	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A22R4064	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A22R4065	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A22R4066	315-0153-00	XB010200		RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R4070	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R4071	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R4072	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R4073	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A22R4074	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A22R4075	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A22R4076	311-1340-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	02111	43P102T621
A22R4077	321-0279-00			RES.,FXD,FILM:7.87K OHM,1%,0.125W	91637	MFF1816G78700F
A22R4081	315-0623-00	XB010200		RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A22R4082	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A22R4083	315-0272-00	XB010200		RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A22R4084	315-0103-00	XB010200		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A22R4085	315-0153-00	XB010200		RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A22R4090	321-0188-00			RES.,FXD,FILM:887 OHM,1%,0.125W	91637	MFF1816G887R0F
A22R4091	321-0246-00			RES.,FXD,FILM:3.57K OHM,1%,0.125W	91637	MFF1816G35700F
A22TP4011	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4012	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4031	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4041	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4052	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4061	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4062	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4078	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4079	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02

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A22TP4081	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4082	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22TP4091	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A22U2068	156-0680-02			MICROCIRCUIT,DI:DUAL J-K F-F,W/CLEAR,SEL	80009	156-0680-02
A22U3044	156-0742-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM318N
A22U3079	156-0402-00			MICROCIRCUIT,LI:TIMER	27014	SL34829
A22U3086	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A22U4013	156-1126-00			MICROCIRCUIT,LI:VOLTAGE COMPARATOR		
A22U4037	156-1126-00			MICROCIRCUIT,LI:VOLTAGE COMPARATOR		
A22U4062	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458V
A22VR1061	152-0195-00	XB010200		SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A22VR1071	152-0195-00	XB010200		SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A22VR2067	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A22VR2093	152-0662-00			SEMICOND DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
A22VR2096	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2
A22VR3047	152-0486-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	80009	152-0486-00
A22VR3050	152-0508-00			SEMICOND DEVICE:ZENER,0.4W,12.6V,5%	80009	152-0508-00
A22VR3072	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A22VR4050	152-0486-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	80009	152-0486-00
A22VR4054	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A22VR4083	152-0317-00			SEMICOND DEVICE:ZENER,0.25W,6.2V,5%	80009	152-0317-00
A22VR4092	152-0662-00			SEMICOND DEVICE:ZENER,0.4W,5V,1%	04713	SZG195

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A24	----- -----			CKT BOARD ASSY:SD PS SECONDARY		
A24C1032	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	72982	8141N037Z5U0225M
A24C1033	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	72982	8141N037Z5U0225M
A24C1041	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A24C1044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A24C1045	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A24C1047	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A24C1052	290-0807-00			CAP.,FXD,ELCTLT:1000UF,+100-10%,10VDC	90201	TT102N010E1C3P
A24C1056	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A24C1058	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A24C1059	290-0922-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,50V		
A24C1066	290-0922-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,50V		
A24C1076	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A24C2048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A24C2082	290-0877-00			CAP.,FXD,ELCTLT:1200UF,+100-10%,6.3V		
A24C3014	281-0771-00			CAP.,FXD,CER DI:0.0022UF,20%,200V	72982	314-0222Z5U0222M
A24C3044	281-0774-00			CAP.,FXD,CER DI:0.022UF,20%,100V	72982	8045A9ABDZ5U223M
A24C3068	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A24C3073	290-0759-00			CAP.,FXD,ELCTLT:290UF,+75-10%,15V	90201	TTX291U015C1A3
A24CR1031	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A24CR1034	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A24CR1043	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	80009	152-0581-00
A24CR1061	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A24CR1064	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A24CR1065	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A24CR1079	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A24CR1086	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,200V,1A	80009	152-0585-00
A24CR1092	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A24CR3012	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A24CR3014	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A24CR3018	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A24CR3019	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A24CR3020	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A24CR3032	152-0762-00			SEMICOND DEVICE:SIICON,35V,30A		
A24CR3046	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A24CR3049	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A24CR3056	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	80009	152-0655-00
A24CR3062	152-0655-00			SEMICOND DEVICE:SILICON,100V,3A	80009	152-0655-00
A24CR3063	152-0720-00			SEMICOND DEVICE:SIICON,100V,7A		
A24L1031	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A24L2086	108-0974-00			COIL,RF:FIXED,4UH	80009	108-0974-00
A24L3013	108-0980-00			COIL,RF:FIXED,700UH	80009	108-0980-00
A24L3052	108-0981-00			COIL,RF:FIXED,270UH	80009	108-0981-00
A24L3082	108-0976-00			COIL,RF:FIXED,11.2UH	80009	108-0976-00
A24Q1086	151-0464-00			TRANSISTOR:SILICON,NPN	80009	151-0464-00
A24Q1091	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A24Q2032	151-0647-00			TRANSISTOR:SILICON,PNP	04713	SJE795
A24Q2042	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A24Q2044	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A24Q3022	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A24Q3072	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
A24Q3078	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
A24Q3080	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A24R1035	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A24R1036	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A24R1051	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A24R1053	321-0401-00			RES.,FXD,FILM:147K OHM,1%,0.125W	91637	MFF1816G14702F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A24R1054	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A24R1055	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A24R1071	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A24R1073	321-0234-00			RES.,FXD,FILM:2.67K OHM,1%,0.125W	91637	MFF1816G26700F
A24R1084	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A24R2033	308-0795-00			RES.,FXD,WW:0.2 OHM,5%,3W	91637	RS2BR2000J
A24R2034	308-0245-00			RES.,FXD,WW:0.6 OHM,5%,2W	91637	CW-2B30.60HM 5%
A24R2036	308-0446-00			RES.,FXD,WW:15 OHM,5%,5W	91637	RS2A-K15R00J
A24R2055	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A24R2061	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A24R2062	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A24R2066	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A24R2072	308-0818-00			RES,FXD,WW:0.005 OHM,3%,10W	91637	RH10-65/.005 3%
A24R3016	303-0620-00			RES.,FXD,CMPSN:62 OHM,5%,1W	01121	GB6205
A24R3024	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A24R3026	308-0793-00			RES.,FXD,WW:0.51 OHM,5%,0.50W	75042	BW20 .51 OHM 5%
A24R3048	307-0036-00			RES.,FXD,CMPSN:6.8 OHM,10%,1W	01121	GB68G1
A24R3064	303-0360-00			RES.,FXD,CMPSN:36 OHM,5%,1W	01121	GB3605
A24R3072	308-0548-00			RES.,FXD,WW:0.1 OHM,3%,5W	91637	RS5-ER1000UH
A24R3074	308-0446-00			RES.,FXD,WW:15 OHM,5%,5W	91637	RS2A-K15R00J
A24T1012	120-1254-00			XFMR,PWR,STPDN:	80009	120-1254-00
A24TP1037	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A24TP1038	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A24TP1051	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A24TP2067	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A24U1042	156-0872-01			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-0872-01
A24U1074	156-1161-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM317T
A24U2064	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A24VR1036	152-0147-00			SEMICOND DEVICE:ZENER,0.4W,27V,5%	04713	SZ50622RL
A24VR1039	152-0702-00			SEMICOND DEVICE:ZENER,500MW,13V,2%		
A24VR1051	152-0571-00			SEMICOND DEVICE:ZENER,0.4W,16V,5%	80009	152-0571-00
A24VR1097	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	1N965B
A24VR2068	152-0175-01			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	80009	152-0175-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26	----- -----			CKT BOARD ASSY:SD PS INVERTER		
A26C2011	285-0934-00			CAP.,FXD,PLSTC:2.2UF,10%,200V	56289	430P238
A26C2034	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	54473	ECE-A10V220L
A26C2065	285-0562-00			CAP.,FXD,PLSTC:0.47UF,20%,400V	56289	410P47404
A26C3013	290-0771-00			CAP.,FXD,ELCTLT:220UF,+50-10%,10VDC	54473	ECE-A10V220L
A26C3025	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	72982	0831085Z5E00471
A26C3034	285-1192-00			CAP.,FXD,PPR DI:0.0022UF,20%,250VAC		
A26CR1035	152-0396-01			SEMICOND DEVICE:SILICON,400V,3A	12969	652-821
A26CR2021	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A26CR2024	152-0732-00			SEMICOND DEVICE:ZENER,1.5W,3.3V,5%		
A26CR2027	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A26CR2032	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A26CR2043	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A26CR2086	152-0291-00			SEMICOND DEVICE:ZENER,1W,20V,5%	04713	1N3027B
A26CR3012	152-0732-00			SEMICOND DEVICE:ZENER,1.5W,3.3V,5%		
A26CR3014	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A26CR3019	152-0398-00			SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A26F2052	158-0018-00			XTAL UNIT,QTZ:54MHZ		
A26F2052	----- -----			(OPTION 4Y ONLY)		
A26F2052	158-0158-00			XTAL UNIT,QTZ:5.98224MHZ,0.0025%,PARALLEL	75378	TX-502
A26F2052	----- -----			(OPTION 4X ONLY)		
A26L1025	108-0978-00			COIL,RF:FIXED,135UH	80009	108-0978-00
A26L2041	108-0978-00			COIL,RF:FIXED,135UH	80009	108-0978-00
A26Q2015	151-0679-00			TRANSISTOR:SILICON,NPN	04713	MJE13009
A26Q2033	151-0439-00			TRANSISTOR:SILICON,NPN	80009	151-0439-00
A26Q2061	151-0522-00			TRANSISTOR:SILICON,TRIAC,400V	03508	SC141DX164
A26Q2083	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
A26Q3015	151-0679-00			TRANSISTOR:SILICON,NPN	04713	MJE13009
A26Q3021	151-0439-00			TRANSISTOR:SILICON,NPN	80009	151-0439-00
A26R2014	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A26R2025	301-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.50W	01121	EB1315
A26R2031	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R2042	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A26R2044	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R2058	308-0106-00			RES.,FXD,WW:1K OHM,5%,5W	14193	S A50
A26R2059	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A26R2062	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A26R2063	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A26R2064	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A26R2079	301-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.50W	01121	EB3015
A26R2082	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A26R2084	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A26R3011	301-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.50W	01121	EB1315
A26R3016	304-0181-00			RES.,FXD,CMPSN:180 OHM,10%,1W	01121	GB1811
A26T3031	120-1255-00			XFMR,RF:INV BASE DRIVE	80009	120-1255-00
A26U2070	156-1317-00			CPLR,OPTOELECTR:LED & PHOTOTHYRISTOR		
A26U3070	156-1317-00			CPLR,OPTOELECTR:LED & PHOTOTHYRISTOR		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30	----- -----			CKT BOARD ASSY:SD FRONT PANEL		
A30C1027	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A30R1012	303-0751-00			RES.,FXD,CMPSN:750 OHM,5%,1W	01121	GB7515
A30R1022	301-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.50W	01121	EB1315
A30R1024	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A30R1025	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A30R1026	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A30R1027	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A30R1028	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A30U1010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A40	----- -----			CKT BOARD ASSY:LSI 11/2		
A40C1	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C2	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C3	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C4	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C5	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C6	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C7	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C8	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C9	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C10	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C11	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C12	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C13	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C14	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C15	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C16	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C17	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C18	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C19	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C20	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C21	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C22	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A40C23	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C26	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C27	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C28	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C29	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C30	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C31	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C32	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C33	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C34	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C35	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C36	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C37	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C39	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40C41	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A40C42	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A40C43	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A40C44	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A40C45	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C46	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C47	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40C48	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C49	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C50	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C51	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C52	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C53	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C54	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C55	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C56	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C57	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C58	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C59	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C60	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C61	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C62	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C63	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C64	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C65	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C66	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C67	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C68	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C69	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C70	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C71	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C72	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C73	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C74	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C76	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C77	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C78	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A40C79	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A40C80	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A40C81	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A40C82	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A40D1	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D2	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D3	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D4	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D5	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D6	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D7	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D8	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D9	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D10	118-0827-00			SEMICOND DEVICE:STABISTOR		
A40D11	118-0827-00			SEMICOND DEVICE:STABISTOR		
A40D12	152-0689-00			SEMICOND DEVICE:ZENER,0.4W,5%,3.9V	80009	152-0689-00
A40D13	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D14	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D15	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40D16	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A40E1	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM		
A40E2	156-0149-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND SCHMITT	80009	156-0149-00
A40E3	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
A40E4	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	04713	SN74LS10N OR J
A40E5	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A40E6	118-0642-00			OSCILLATOR:31.578MHZ		
A40E7	118-0646-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40E8	156-1055-00			MICROCIRCUIT,DI:QUAD NOR UNIFIED BUS RCVR	27014	DS8640N
A40E9	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
A40E10	156-0718-00			MICROCIRCUIT,DI:TRIPLE 3-INP POS-NOR GATES	80009	156-0718-00
A40E11	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
A40E12	156-0629-00			MICROCIRCUIT,DI:30MHZ PRESETTABLE BIN CTR	01295	SN74LS197N
A40E13	118-0646-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR		
A40E14	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM		
A40E15	156-0479-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	27014	DM74LS32N
A40E16	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
A40E17	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
A40E18	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
A40E19	118-0646-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR		
A40E20	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M
A40E21	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A40E22	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
A40E23	156-0311-00			MICROCIRCUIT,DI:6-BIT BINARY RATE MULT	80009	156-0311-00
A40E24	118-0648-00			MICROCIRCUIT,DI:4 BIT XCVR		
A40E25	156-0645-00			MICROCIRCUIT,DI:HEX SCHMITT-TRIG INVERTER	80009	156-0645-00
A40E26	156-0478-00			MICROCIRCUIT,DI:DUAL 4-INPUT AND GATE	01295	SN74LS21N
A40E27	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	04713	74LS174(N OR J)
A40E28	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
A40E29	118-0648-00			MICROCIRCUIT,DI:4 BIT XCVR		
A40E30	118-0644-00			MICROCIRCUIT,DI:DATA CONTROL,ROM		
A40E31	118-0643-00			MICROCIRCUIT,DI:512 X 22 N CHANNEL ROM		
A40E32	118-0649-00			MICROCIRCUIT,DI:512 X 22 N CHANNEL ROM		
A40E33	118-0645-00			MICROCIRCUIT,DI:CONTROL CHIP		
A40E35	156-0328-00			MICROCIRCUIT,DI:DUAL CLOCK DRIVER		
A40E36	307-0676-00			RES NTWK,FXD,FI:14,330 OHM,14,680 OHM,0.1M		
A40E37	156-0992-00			MICROCIRCUIT,DI:QUAD TTL-TO MOS DRIVER	80009	156-0992-00
A40E38	118-0648-00			MICROCIRCUIT,DI:4 BIT XCVR		
A40E39	118-0648-00			MICROCIRCUIT,DI:4 BIT XCVR		
A40Q1	151-0645-00			TRANSISTOR:SILICON,NPN	04713	SPS8288
A40R1	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R2	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A40R3	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A40R4	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A40R5	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R6	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R7	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R8	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R9	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A40R12	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R13	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A40R14	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A40R15	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A40R16	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A40R17	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A40R18	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A40R19	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A40R20	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A40R21	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A40R22	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	MFF1816G422ROF
A40R23	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499ROF
A40XE30	131-0623-00			TERMINAL,PIN:0.385 L X 0.048 OD,BRS	80009	131-0623-00
A40XE31	131-0623-00			TERMINAL,PIN:0.385 L X 0.048 OD,BRS	80009	131-0623-00
A40XE32	131-0623-00			TERMINAL,PIN:0.385 L X 0.048 OD,BRS	80009	131-0623-00
A40XE33	131-0623-00			TERMINAL,PIN:0.385 L X 0.048 OD,BRS	80009	131-0623-00
A40XE34	131-0623-00			TERMINAL,PIN:0.385 L X 0.048 OD,BRS	80009	131-0623-00

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A50	----- -----			CKT BOARD ASSY:SD FLEX DISC CONTROLLER		
A50C1011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C1141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C2121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C2131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C2141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C2151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C3021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C3031	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330J
A50C3041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4141	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C4151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C5101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C5111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C5131	283-0334-00			CAP.,FXD,CER DI:130PF,+1-2%,500V	72982	8121N501C0G0131G
A50C6061	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C6071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C6081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C6091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C6111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C6131	283-0334-00			CAP.,FXD,CER DI:130PF,+1-2%,500V	72982	8121N501C0G0131G
A50C7011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7021	290-0107-00			CAP.,FXD,ELCTLT:25UF,+75-10%,25V	56289	30D256G025DB9
A50C7031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7082	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A50C7091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7101	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7121	290-0107-00			CAP.,FXD,ELCTLT:25UF,+75-10%,25V	56289	30D256G025DB9
A50C7131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50C7141	283-0339-00			CAP.,FXD,CER DI:0.22UF.10%,50V	72982	8131N075W5R224K
A50C7142	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7143	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A50C7151	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7152	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7154	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50C7155	283-0159-00			CAP.,FXD,CER DI:18PF,5%,50V	72982	8111B065C0G0180J
A50C7158	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A50CR1021	150-1014-00			LAMP,LED:RED,50MA	50522	MV5054-1
A50CR1051	150-1014-00			LAMP,LED:RED,50MA	50522	MV5054-1
A50CR1061	150-1014-00			LAMP,LED:RED,50MA	50522	MV5054-1
A50CR2011	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A50CR2012	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A50CR4051	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A50Q3031	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A50R1011	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1021	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A50R1051	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A50R1061	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A50R1071	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R2051	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A50R3031	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A50R3032	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A50R3033	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A50R3034	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A50R3061	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R4051	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A50R5081	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R6081	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R6131	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	91637	MFF1816G52300F
A50R6132	321-0291-00			RES.,FXD,FILM:10.5K OHM,1%,0.125W	91637	MFF1816G10501F
A50R6141	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R7051	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7061	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A50R7062	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A50R7063	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A50R7064	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A50R7071	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R7072	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R7073	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R7074	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R7081	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A50R7082	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R7091	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7092	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7093	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7101	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7102	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7103	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A50R7121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R7141	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A50R7142	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A50R7144	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R7151	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A50R7152	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A50R7153	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A50R7154	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50R7156	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A50U1010	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A50U1020	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH		
A50U1030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U1040	156-0789-00			MICROCIRCUIT,DI:8-BIT SR,PRL LOAD	80009	156-0789-00
A50U1050	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A50U1060	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U1070	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
A50U1080	156-0789-00			MICROCIRCUIT,DI:8-BIT SR,PRL LOAD	80009	156-0789-00
A50U1090	156-0789-00			MICROCIRCUIT,DI:8-BIT SR,PRL LOAD	80009	156-0789-00
A50U1100	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U1110	156-0784-02			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT BINARY	27014	DM74LS163ANA+
A50U1120	156-0418-00			MICROCIRCUIT,DI:8-INPUT,NAND GATE	80009	156-0418-00
A50U1130	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A50U1140	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A50U2020	156-0983-00			MICROCIRCUIT,DI:MICROPROCESSOR EIGHT BIT	80009	156-0983-00
A50U2030	160-0412-00			MICROCIRCUIT,DI:4096 X 8 ROM		
A50U2040	156-1382-00			MICROCIRCUIT,DI:1024 X 8 STATIC RAM		
A50U2050	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A50U2060	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A50U2070	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A50U2080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A50U2090	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A50U2100	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U2110	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U2120	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
A50U2130	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
A50U2140	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
A50U2150	156-0651-00			MICROCIRCUIT,DI:8-BIT PRL-OUT,SER SHF RGTR	01295	SN74LS164N
A50U3040	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	80009	156-0690-03
A50U3050	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS W/3	80009	156-1111-02
A50U3060	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U3070	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A50U3080	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10NP3
A50U3090	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	80009	156-0718-03
A50U3100	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A50U3110	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A50U3120	156-0472-00			MICROCIRCUIT,DI:13-INPUT NAND GATE	01295	SN74S133N
A50U3130	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A50U3140	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U3150	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A50U4010	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A50U4020	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A50U4030	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A50U4040	156-0030-03			MICROCIRCUIT,DI:QUAD 2 INPUT NAND GATE		
A50U4050	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A50U4060	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U4070	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U4080	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A50U4090	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A50U4100	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A50U4110	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A50U4120	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A50U4130	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20NP3
A50U4140	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A50U4150	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U5010	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00

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A50U5020	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U5030	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A50U5040	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U5050	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U5060	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A50U5070	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A50U5080	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A50U5090	156-0784-02			MICROCIRCUIT,DI:SYNCHRONOUS 4 BIT BINARY	27014	DM74LS163ANA+
A50U5100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A50U5110	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A50U5120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A50U5130	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U5140	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A50U5150	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A50U6010	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U6020	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U6030	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A50U6040	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U6050	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A50U6060	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A50U6070	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH		
A50U6080	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH		
A50U6090	156-0145-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	80009	156-0145-02
A50U6100	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U6110	156-0145-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	80009	156-0145-02
A50U6120	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U6130	156-0733-03			MICROCIRCUIT,DI:DUAL MONOSTABLE		
A50U6140	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U6150	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U7010	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7020	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7030	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7040	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7050	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7060	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7070	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7080	156-0623-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	80009	156-0623-00
A50U7090	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A50U7100	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A50U7110	156-0145-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	80009	156-0145-02
A50U7120	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A50U7130	156-1314-00			MICROCIRCUIT,DI:POLYNOMINAL GENERATOR		
A50U7140	156-0124-00			MICROCIRCUIT,DI:SGL FREQ/PHASE DETECTOR	80009	156-0124-00
A50U7150	156-0121-00			MICROCIRCUIT,DI:DUAL VOLTAGE-CONT MV	80009	156-0121-00
A50Y7151	158-0202-00			XTAL UNIT,QTZ:8.0MHZ,0.015%,PARALELL		

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A60	----- -----			CKT BOARD ASSY:SD 32K MEMORY		
A60C1011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1078	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1091	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1098	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1108	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1118	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1138	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1148	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C1158	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2088	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2091	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2098	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2118	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2128	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2138	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2148	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2151	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C2158	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3018	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
A60C3064	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C3161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4053	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C4161	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C5021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C5041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104
A60C5041	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A60C5091	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A60C5121	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A60C5167	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A60C5168	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
A60C5168	283-0144-00			CAP.,FXD,CER DI:33PF,1%,500V	72982	801-547P2G330G
A60CR0000	152-0761-00			SEMICOND DEVICE:TRANSIENT SUPPR,1.5 JOULE		
A60CR5043	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	80009	152-0279-00
A60R000	308-0755-00			RES.,FXD,WW:0.75 OHM,5%,2W	75042	BWH-R7500J
A60R3061	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3062	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3063	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3065	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3066	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3067	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3068	315-0390-00			RES.,FXD,CMPSN:39 OHM,5%,0.25W	01121	CB3905
A60R3076	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A60R3082	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A60R3083	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A60R3131	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A60R3138	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R3162	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A60R4074	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4075	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4082	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4086	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4087	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4118	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4119	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4128	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R4129	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R5044	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A60R5153	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A60R5156	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60R5163	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A60R5164	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A60TP2129	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60TP2149	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60TP3011	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60TP3026	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60TP4138	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60TP5133	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A60U1010	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1020	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1030	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1040	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1050	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1060	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1070	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1080	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1090	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1100	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1110	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1120	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1130	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1140	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1150	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U1160	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02

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A60U2010	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2020	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2030	156-0968-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE	80009	156-0968-02
A60U2040	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2050	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2060	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2070	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2080	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2090	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2100	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2110	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2120	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2130	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2140	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2150	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U2160	156-0968-02			MICROCIRCUIT,DI:16384 X 1 DYNAMIC RAM	80009	156-0968-02
A60U3060	156-0965-00			MICROCIRCUIT,DI:ADRS MUX & REFRESH CNTR	04713	MC3242AL
A60U3080	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	80009	156-0321-02
A60U3090	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A60U3100	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A60U3110	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NND GATE	01295	SN74S00NP3
A60U3120	156-0738-04			MICROCIRCUIT,DI:HEX D FF W/CLEAR,BURN-IN		
A60U3140	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A60U3160	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	80009	156-0690-03
A60U4030	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A60U4040	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A60U4060	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74LS175NP3
A60U4080	156-0707-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	01295	SN74S86N
A60U4090	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A60U4100	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A60U4110	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A60U4120	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A60U4130	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	80009	156-0321-02
A60U4140	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A60U4160	156-0966-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0966-00
A60U5010	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A60U5030	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A60U5040	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A60U5060	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A60U5080	156-0455-02			MICROCIRCUIT,DI:HEX BUS RECEIVER		
A60U5090	156-0653-02			UAD UNIFIED BUS XCVR INV		
A60U5110	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A60U5120	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	80009	156-0459-02
A60U5140	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A60U5160	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	80009	156-0323-02
A60Y4168	158-0149-00			XTAL UNIT,QTZ:24.25 MHZ,0.01%,SERIES	75378	TX-411

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A70	----- -----			CKT BOARD ASSY:SD/IO		
A70C1031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C1051	283-0594-00			CAP.,FXD,MICA D:0.001UF,1%,100V	00853	D151F102F0
A70C1058	283-0077-00			CAP.,FXD,CER DI:330PF,5%,500V	56289	40C94A3
A70C1071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C1091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C1111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C1123	283-0180-00			CAP.,FXD,CER DI:5600PF,20%,200V	72982	8121N204 E 562M
A70C2021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C2051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C2091	290-0658-00			CAP.,FXD,ELCTLT:4UF,+50-10%,200V	56289	600D405F200KD4
A70C2094	283-0176-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	72982	8121B058X7R0222M
A70C2111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C3041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C3091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C3111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C3131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C4011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C4021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C4071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C4081	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C4091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C5021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C5041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C5110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C5111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C6021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C6041	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C6071	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C6091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C7011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C7049	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A70C7051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C7082	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A70C7091	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C7111	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70C7121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A70R1031	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R1041	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A70R1052	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A70R1054	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A70R1125	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A70R1127	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A70R2011	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A70R2092	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A70R2093	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A70R6050	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A70R6061	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A70R7040	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A70R7041	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A70R7042	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A70R7043	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A70R7044	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A70R7045	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A70R7046	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A70R7047	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A70U1030	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N

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A70U1040	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN-IN		
A70U1050	156-0371-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND ST	80009	156-0371-00
A70U1060	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U1070	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U1080	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U1090	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U1100	156-0165-00			MICROCIRCUIT,DI:DUAL 4-INPUT POS NOR GATE	01295	SN7425N
A70U1110	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A70U1120	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
A70U1130	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A70U2010	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74LS175NP3
A70U2020	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A70U2030	156-0470-02			8 INP DATA SEL W/3 STATE		
A70U2040	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A70U2050	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A70U2060	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A70U2070	156-1310-00			MICROCIRCUIT,DI:UART 6402,CMOS,40 PIN-DIP		
A70U2090	156-0733-03			MICROCIRCUIT,DI:DUAL MONOSTALE MV W/ST NP		
A70U2100	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
A70U2110	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE		
A70U2120	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
A70U2130	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A70U3010	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A70U3020	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U3030	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A70U3040	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U3050	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A70U3060	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A70U3080	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP & MUX	01295	SN74LS157P3
A70U3090	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U3100	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U3110	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U3120	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A70U3130	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U4010	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U4020	156-0617-00			MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N
A70U4030	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A70U4040	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U4050	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A70U4060	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A70U4070	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U4080	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U4090	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N
A70U4100	156-0798-02			SICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N
A70U4110	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N
A70U4120	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U4130	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A70U5010	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A70U5020	156-0646-02			MICROCIRCUIT,DI:4 BIT BINARY COUNTER		
A70U5030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR
A70U5040	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U5050	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U5060	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE		
A70U5070	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A70U5080	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A70U5090	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N3
A70U5100	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A70U5110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A70U5120	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A70U5130	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A70U6010	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A70U6020	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10NP3
A70U6030	156-0219-02			MICROCIRCUIT,DI:8 BIT PRIORITY ENCODER		
A70U6040	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR		
A70U6050	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A70U6070	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A70U6080	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N3
A70U6090	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A70U6100	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153N3
A70U6110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A70U6120	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A70U6130	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A70U7010	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7020	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7030	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7050	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7060	156-0455-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7080	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A70U7100	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A70U7110	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A70U7120	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80	----- -----			CKT BOARD ASSY:SD UTILITY		
A80C1007	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1022	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1057	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1063	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1108	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C1119	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C2079	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A80C2082	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C2121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C3031	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C3069	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C3093	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C3096	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	72982	855-535A560K
A80C3117	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	72982	855-535A560K
A80C3131	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C4029	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C4051	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C4057	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	72982	0831085Z5E00471J
A80C4058	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A80C4069	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A80C4079	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C4109	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C5041	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A80C5063	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
A80C5119	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C6011	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C6021	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C6043	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A80C6046	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C6047	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A80C6053	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C6054	283-0078-00			CAP.,FXD,CER DI:0.001UF,20%,500V	56289	20C114A8
A80C6063	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C6139	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7037	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7038	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A80C7039	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7059	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7069	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7078	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	10ULA22V-T
A80C7092	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7098	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80C7117	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A80CR1021	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR3011	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR3012	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR3013	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR4037	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR5051	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R
A80CR6039	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A80DS1021	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80DS1022	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80DS1023	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80DS1031	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80DS1032	150-1020-00			LAMP,LED:RED,5 VOLTS	72619	555-2007
A80R1035	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R1091	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	91637	MSP06A01-103J
A80R2051	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R3041	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80R3092	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	91637	MSP06A01-103J
A80R3107	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065
A80R4021	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R4032	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R4037	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A80R4039	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A80R4047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R4059	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A80R4068	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5028	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R5029	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R5031	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5032	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5038	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A80R5039	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5048	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5049	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5052	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A80R5062	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A80R5064	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A80R5111	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R5121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A80R5122	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A80R5129	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80R5131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R6031	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A80R6033	321-0382-00			RES.,FXD,FILM:93.1K OHM,1%,0.125W	91637	MFF1816G93101F
A80R6034	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A80R6035	321-0350-00			RES.,FXD,FILM:43.2K OHM,1%,0.125W	91637	MFF1816G43201F
A80R6036	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A80R6037	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	MFF1816G34801F
A80R6038	321-0352-00			RES.,FXD,FILM:45.3K OHM,1%,0.125W	91637	MFF1816G45301F
A80R6041	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A80R6042	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A80R6044	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A80R6045	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R6052	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R6060	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R6061	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R6111	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R6121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R6131	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A80R7010	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80R7018	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80R7023	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A80R7024	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A80R7030	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A80R7045	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A80R7047	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A80R7054	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A80R7055	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80R7056	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A80R7060	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A80R7065	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A80R7066	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A80R7080	307-0547-00			RES NTWK,FXD,FI:DUAL,180 X 390 OHM,5%,1.5W	73138	898-5-R180/390
A80R7098	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80R7099	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A80TP1040	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A80TP6021	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A80TP6033	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A80TP6039	214-0579-02			TERM,TEST POINT:BRASS	80009	214-0579-02
A80U1010	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A80U1020	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR		
A80U1030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U1040	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M
A80U1050	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U1060	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U1070	156-0361-00			MICROCIRCUIT,DI:UNIV A SYN RCVR XMTR	80009	156-0361-00
A80U1080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A80U1090	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157NP3
A80U1100	156-0850-00			MICROCIRCUIT,DI:PROGRAMMABLE BIT RATE GEN	80009	156-0850-00
A80U1110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U2010	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A80U2020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U2030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U2040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A80U2050	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U2060	156-0471-02			MICROCIRCUIT,DI:DATA 4/1 DATA SEL		
A80U2080	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U2100	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP 6 GATE	01295	SN74LS21NP3
A80U2110	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U2120	156-0219-02			MICROCIRCUIT,DI:8 BIT PRIORITY ENCODER		
A80U3010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A80U3020	156-0219-02			MICROCIRCUIT,DI:8 BIT PRIORITY ENCODER		
A80U3030	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74LS175NP3
A80U3040	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20NP3
A80U3050	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A80U3060	156-0471-02			MICROCIRCUIT,DI:DATA 4/1 DATA SEL		
A80U3070	156-0361-00			MICROCIRCUIT,DI:UNIV A SYN RCVR XMTR	80009	156-0361-00
A80U3080	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A80U3090	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A80U3100	156-0850-00			MICROCIRCUIT,DI:PROGRAMMABLE BIT RATE GEN	80009	156-0850-00
A80U3120	156-0390-00			MICROCIRCUIT,DI:DUAL 4-LINE TO 2-LINE	80009	156-0390-00
A80U3130	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A80U4010	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A80U4020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U4030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A80U4040	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	80009	156-0718-03
A80U4050	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	80009	156-0718-03
A80U4060	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A80U4080	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U4090	156-0470-02			MICROCIRCUIT,DI:8 INP DATA SEL W/3 STATE		
A80U4100	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10NP3
A80U4110	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR
A80U4120	156-0390-00			MICROCIRCUIT,DI:DUAL 4-LINE TO 2-LINE	80009	156-0390-00
A80U4130	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U5010	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A80U5020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A80U5030	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A80U5040	156-0153-02			MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A80U5050	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602 (PC OR DC)
A80U5060	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602 (PC OR DC)
A80U5070	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A80U5080	160-0399-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	160-0399-00
A80U5090	160-0400-00			MICROCIRCUIT,DI:1024 X 8 PROM	80009	160-0400-00
A80U5100	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A80U5110	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A80U5120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00NP3 OR 4
A80U5130	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A80U6010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A80U6020	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A80U6040	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A80U6050	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A80U6060	156-0767-00			MICROCIRCUIT,DI:HEX GATE	04713	MC14572UBCP OR L
A80U6070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U6080	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U6090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U6100	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A80U6110	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUX COMPTR		
A80U6130	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A80U7020	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U7040	156-0455-02			MICROCIRCUIT,DI:HEX BUS RECEIVER		
A80U7050	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U7070	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U7090	156-0653-02			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR INV		
A80U7100	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	04713	SN74LS133
A80U7110	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A80U7130	156-0539-01			MICROCIRCUIT,DI:6 BIT UNIFIED BUS COMPTR		
A80VR6032	152-0437-00			SEMICOND DEVICE:ZENER,SI,8.2V,2%,0.4W	14552	TD332679
A80W1098	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W2094	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W2095	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W3092	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4016B	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4019A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4031A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4042A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4043A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W4045B	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W5061	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W6101A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W7012B	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W7013A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W7016B	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80W7018A	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A80Y3111	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05% PARALLEL	75378	MP-024

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number	
A90	----- -----			CKT BOARD ASSY:SD COMM ADAPTER			
A90C1041	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90C1042	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90C2012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M	
A90C2014	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M	
A90C2015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M	
A90C2016	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	72982	855-535A560K	
A90C2017	283-0095-00			CAP.,FXD,CER DI:56PF,10%,200V	72982	855-535A560K	
A90C3021	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90C3022	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90C3031	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90C3032	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511(	
A90CR1041	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R	
A90CR1042	152-0141-02			SEMICOND DEVICE:SILICON,30V,50NA	01295	1N4152R	
A90Q1011	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677	
A90R1011	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325	
A90R1021	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1022	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1031	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1	
A90R1033	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1034	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1041	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1042	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R1043	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A90R2011	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R2021	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235	
A90R2022	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2023	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2035	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2036	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2037	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325	
A90R2042	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2043	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2044	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R2045	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A90R3011	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325	
A90R3012	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325	
A90R3013	315-0106-00			RES.,FXD,CMPSN:10M OHM,5%,0.25W	01121	CB1065	
A90SW2040	263-0042-00			SWITCH SL ASSY:B-SOURCE	80009	263-0042-00	
A90U2011	156-1150-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR,NEGATIVE	04713	MC79L05ACP	
A90U3020	156-0850-00			MICROCIRCUIT,DI:PROGRAMMABLE BIT RATE GEN	80009	156-0850-00	
A90U3025	156-1315-00			MICROCIRCUIT,INTFC:QUAD DIFFERENTIAL RCVR			*
A90U3030	156-1316-00			MICROCIRCUIT,INTFC:QUAD 3 STATE SINGLE ENDED			
A90U3035	156-1316-00			MICROCIRCUIT,INTFC:QUAD 3 STATE SINGLE ENDED			
A90U3040	156-1315-00			MICROCIRCUIT,INTFC:QUAD DIFFERENTIAL RCVR			*
A90U3045	156-0544-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH			
A90Y3010	158-0124-00			XTAL UNIT,QTZ:2.4576 MHZ,0.05% PARALLEL	75378	MP-024	

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B610	119-0721-00			FAN,VENTILATING:75 CFM,7W,115VAC,50/60HZ	82877	027119
DS1032	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
DS1038	150-1064-00			LT EMITTING DIO:YELLOW,585NM,40 MA MAX	50522	MV5374C
DS1052	150-0093-01			LAMP,INCAND:5V,0.06A,0.05MSCP,SEL	87034	9AS15
F000	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
F651	159-0013-00			FUSE,CARTRIDGE:3AG,6A,125V,7SEC	71400	MTH6
FL652	119-1306-00			FILTER,RFI:6A,250V,50-400HZ		
J1012	131-0955-01			CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
J2012	131-0955-01			CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
S615	260-1967-00			SWITCH,SLIDE:DPDT 5A/250V,10A/125V MKD		
S650	260-1989-00			SWITCH,ROCKER:DPST,16A,250VAC	000FJ	1602.0121
S1014	260-1867-00			SWITCH,TOGGLE:SPDT,0.4A,20V	09353	7108-J61-CB8
S1024	260-1868-00			SWITCH,TOGGLE:SPDT,0.4A,20V	09353	7101-J61-CB8
S1045	260-2028-00			SWITCH,ROCKER:DPDT,0.4VA,20VAC		
T660	120-1256-00			XFMR,PWR,STPDN:	80009	120-1256-00

BRUN(L) ◇2

J4 LSI-11/2

+5	21	22	BIRQ5(L)
-12	23	24	BIRQ6(L)
⇦ +12	25	26	BDAL16(L)
	27	28	BDAL17(L)
BDOUT(L)	29		
BRPLY(L)	31	32	BRUN(L)
BDIN(L)	33		
BSYNC(L)	35	36	▷
BWTBT(L)	37	38	
BIRQ(L)	39	40	
BIAK1(L)	41	42	▷
BIAKØ(L)	43	44	BDMR(L)
BBS7(L)	45	46	BHALT(L)
BDMGI(L)	47	48	BREF(L)
BDMGO(L)	49	50	+12
BINIT(L)	51	52	▷
BDALØ(L)	53		
BDAL1(L)	55	56	+5

J3 LSI-11/2

+5	65	66	BDCOK(H)
-12	67	68	BPOK(H)
⇦ +12	69		
	71		
BDAL2(L)	73		
BDAL3(L)	75		
BDAL4(L)	77		
BDAL5(L)	79	80	▷
BDAL6(L)	81	82	
BDAL7(L)	83	84	
BDAL8(L)	85	86	▷
BDAL9(L)	87	88	BSACK(L)
BDALIØ(L)	89	90	BIRQ7(L)
BDAL11(L)	91	92	BEVNT(L)
BDAL12(L)	93	94	+12
BDAL13(L)	95	96	▷
BDAL14(L)	97		
BDAL15(L)	99	100	+5

J5

	1	2	RD FLTR SW/ WR CUR SW(L)
	3	4	J6 63
	5	6	J6 61
	7	8	J6 59
	9	10	TWO SIDED(L)
	11	12	DISC CHANGE(L)
	13	14	SIDE SEL(L)
	15	16	IN USE(L)
	17	18	HEAD LD(L)
	19	20	INDEX(L)
	21	22	READY(L)
	23	24	J6 7
	25	26	DRIVE SEL 1(L)
	27	28	DRIVE SEL 2(L)
	29	30	DRIVE SEL 3(L)
	31	32	DRIVE SEL 4(L)
	33	34	DIRECTION(L)
	35	36	STEP(L)
	37	38	WR DATA(L)
	39	40	WR GATE(L)
	41	42	TRACKØØ(L)
	43	44	WR PROTECT(L)
	45	46	RD DATA(L)
	47	48	J6 18
	49	50	J6 20

J6 FLEXIBLE DISC CONTROLLER

DRIVE SEL 3(L)	1	2	DRIVE SEL 4(L)
DRIVE SEL 2(L)	3	4	DIRECTION(L)
DRIVE SEL 1(L)	5	6	STEP(L)
J5 24	7	8	WR DATA(L)
READY(L)	9	10	WR GATE(L)
INDEX(L)	11	12	TRACKØØ(L)
HEAD LOAD(L)	13	14	WR PROTECT(L)
IN USE(L)	15	16	RD DATA(L)
SIDE SEL(L)	17	18	J5 48
DISC CHANGE(L)	19	20	J5 50
+5	21	22	BIRQ5(L)
-12	23	24	BIRQ6(L)
⇦ +12	25	26	BDAL16(L)
	27	28	BDAL17(L)
BDOUT(L)	29		
BRPLY(L)	31		
BDIN(L)	33		
BSYNC(L)	35	36	▷
BWTBT(L)	37	38	
BIRQ(L)	39	40	
BIAKI(L)	41	42	▷
BIAKO(L)	43	44	BDMR(L)
BBS7(L)	45	46	BHALT(L)
BDMGI(L)	47	48	BREF(L)
BDMGO(L)	49	50	+12
BINIT(L)	51	52	▷
BDALØ(L)	53		
BDAL1(L)	55	56	+5
TWO SIDED(L)	57		
J5 8	59		
J5 6	61		RD FLTR SW/ WR CUR SW(L)
J5 4	63	64	
+5	65	66	BDCOK(H)
-12	67	68	BPOK(H)
⇦ +12	69		
	71		
BDAL2(L)	73		
BDAL3(L)	75		
BDAL4(L)	77		
BDAL5(L)	79	80	▷
BDAL6(L)	81	82	
BDAL7(L)	83	84	
BDAL8(L)	85	86	▷
BDAL9(L)	87	88	BSACK(L)
BDAL10(L)	89	90	BIRQ7(L)
BDAL11(L)	91	92	BEVNT(L)
BDAL12(L)	93	94	+12
BDAL13(L)	95	96	▷
BDAL14(L)	97	98	
BDAL15(L)	99	100	+5

J7 SPARE

CYL ADDR 2⁰(L)	1	2	CYL ADDR 2²(L)
CYL ADDR 2¹(L)	3	4	CYL ADDR 2³(L)
HEAD SEL(L)	5	6	CYL ADDR 2⁴(L)
DISC SEL(L)	7	8	CYL ADDR 2⁵(L)
CYL ADDR 2⁶(L)	9	10	CYL ADDR 2⁶(L)
	12		CYL ADDR 2⁷(L)
+5	21	22	BIRQ5(L)
-12	23	24	BIRQ6(L)
⇦ +12	25	26	BDAL16(L)
	27	28	BDAL17(L)
BDOUT(L)	29		
BRPLY(L)	31		
BDIN(L)	33		
BSYNC(L)	35	36	▷
BWTBT(L)	37	38	
BIRQ(L)	39	40	
BIAKI(L)	41	42	▷
BIAKO(L)	43	44	BDMR(L)
BBS7(L)	45	46	BHALT(L)
BDMGI(L)	47	48	BREF(L)
BDMGO(L)	49	50	+12
BINIT(L)	51	52	▷
BDALØ(L)	53		
BDAL1(L)	55	56	+5
+5	65	66	BDCOK(H)
-12	67	68	BPOK(H)
⇦ +12	69		
	71		
BDAL2(L)	73		
BDAL3(L)	75		
BDAL4(L)	77		
BDAL5(L)	79	80	▷
BDAL6(L)	81	82	
BDAL7(L)	83	84	
BDAL8(L)	85	86	▷
BDAL9(L)	87	88	BSACK(L)
BDAL10(L)	89	90	BIRQ7(L)
BDAL11(L)	91	92	BEVNT(L)
BDAL12(L)	93	94	+12
BDAL13(L)	95	96	▷
BDAL14(L)	97		
BDAL15(L)	99	100	+5

J8 SPARE

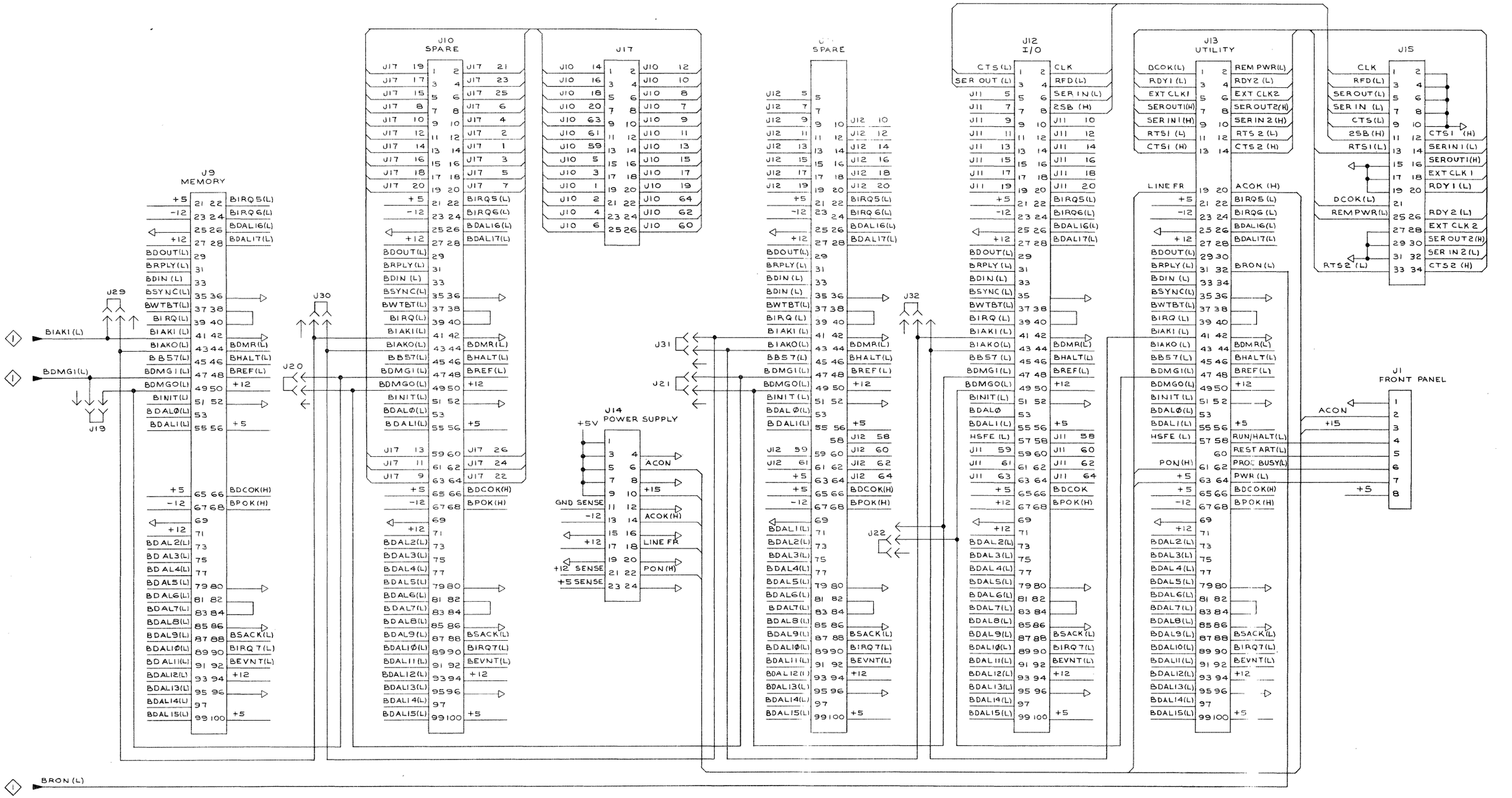
READ DATA(L)	1	2	DATA CLOCK(L)
CYL ADD. STB(L)	3	4	UNIT SELØ(L)
SECTOR(L)	5	6	INDEX(L)
SECT. ADD 2⁰(L)	7	8	UNIT SEL 1(L)
SECT. ADD 2⁴(L)	9	10	WR CHECK(L)
UNIT SEL 3(L)	11	12	WR GATE(L)
SECT. ADD 2¹(L)	13	14	READY(L)
UNIT SEL 2(L)	15	16	WR PROT(L)
SECT ADD 2³(L)	17	18	RESTORE(L)
SECT ADD 2²(L)	19	20	ILLEGAL ADD(L)
+5	21	22	BIRQ5(L)
-12	23	24	BIRQ6(L)
⇦ +12	25	26	BDAL16(L)
	27	28	BDAL17(L)
BDOUT(L)	29		
BRPLY(L)	31		
BDIN(L)	33		
BSYNC(L)	35	36	▷
BWTBT(L)	37	38	
BIRQ(L)	39	40	
BIAKI(L)	41	42	▷
BIAKO(L)	43	44	BDMR(L)
BBS7(L)	45	46	BHALT(L)
BDMG1(L)	47	48	BREF(L)
BDMGO(L)	49	50	+12
BINIT(L)	51	52	▷
BDALØ(L)	53		
BDAL1(L)	55	56	+5
ERASE GATE(L)	59	60	ADDR ACK(L)
WR DATA(L)	61	62	SEEK INCOMP(L)
RD GATE(L)	63	64	SEEK COMP(L)
+5	65	66	BDCOK(H)
-12	67	68	BPOK(H)
⇦ +12	69		
	71		
BDAL2(L)	73		
BDAL3(L)	75		
BDAL4(L)	77		
BDAL5(L)	79	80	▷
BDAL6(L)	81	82	
BDAL7(L)	83	84	
BDAL8(L)	85	86	▷
BDAL9(L)	87	88	BSACK(L)
BDAL10(L)	89	90	BIRQ7(L)
BDAL11(L)	91	92	BEVNT(L)
BDAL12(L)	93	94	+12
BDAL13(L)	95	96	▷
BDAL14(L)	97		
BDAL15(L)	99	100	+5

J16

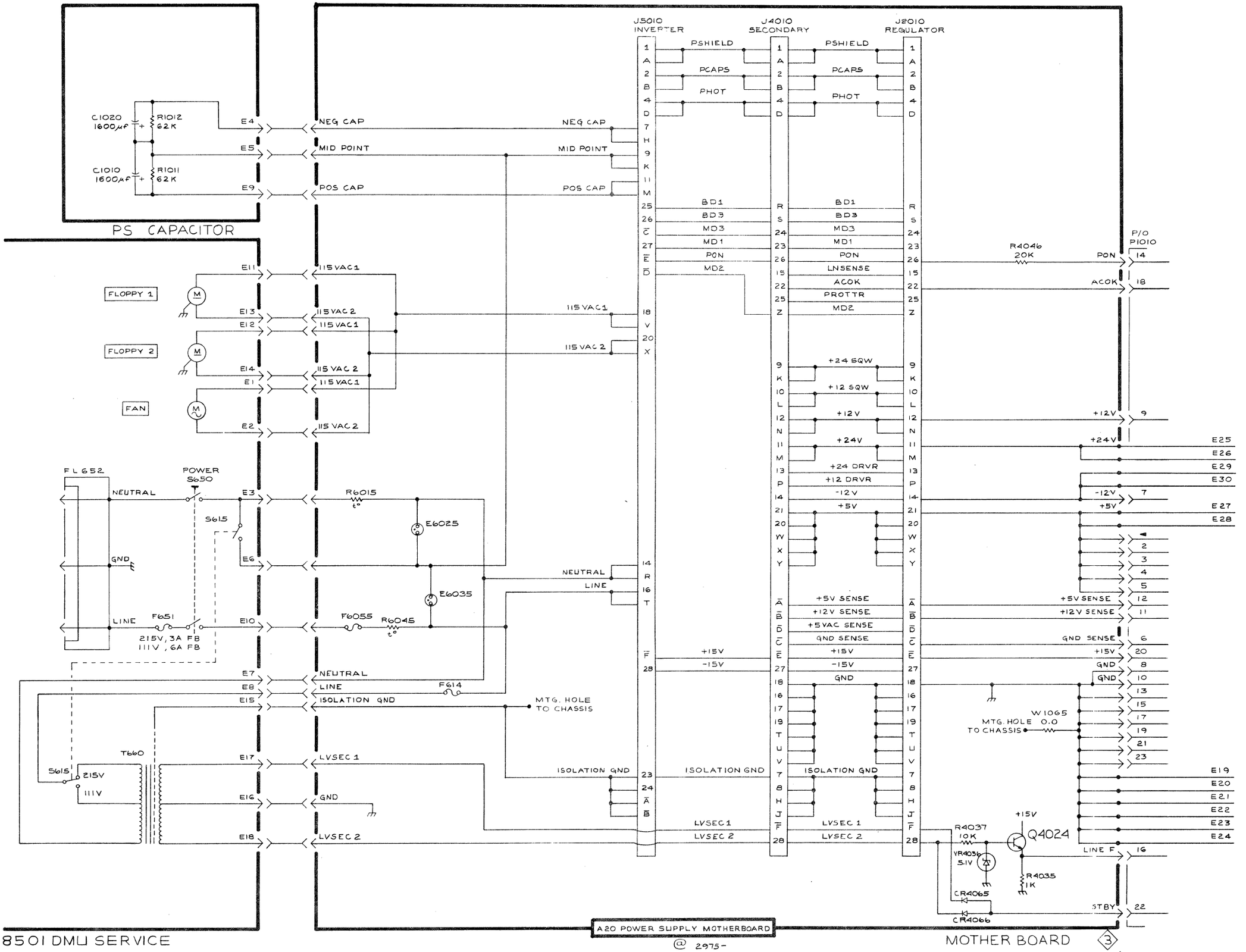
SECT ADDR 2²(L)	1	2	SECT ADDR 2¹(L)
UNIT SEL 2(L)	3	4	SECT ADDR 2⁰(L)
UNIT SEL 3(L)	5	6	SECT ADDR 2⁴(L)
CYL ADDR 2⁶(L)	7	8	SECT ADDR 2⁵(L)
	11	12	SECTOR(L)
DISC SEL(L)	11	12	RD DATA(L)
CYL ADD STB(L)	13	14	DATA CLOCK(L)
HEAD SEL(L)	15	16	INDEX(L)
UNIT SEL Ø(L)	17	18	WR CHECK(L)
UNIT SEL 1(L)	19	20	READY(L)
WR GATE(L)	21	22	WR PROT(L)
		24	ILLEGAL ADD(L)
RESTORE(L)	25	26	ADDR ACK(L)
CYL ADDR 2¹(L)	27	28	SEEK INCOMP(L)
ERASE GATE(L)	29	30	SEEK COMP(L)
WR DATA(L)	31	32	
CYL ADDR 2³(L)	33		
CYL ADDR 2²(L)	35		
CYL ADDR 2⁰(L)	37		
CYL ADDR 2⁴(L)	39		
		42	
CYL ADDR 2⁵(L)	43	44	
CYL ADDR 2⁶(L)	45	46	
RD GATE(L)	47	48	
CYL ADDR 2⁷(L)	49	50	

J26 J16 J31 J17 J28 J18

BDMG(L) ◇2
BIAK(L) ◇2



P/O A10 MAIN INTERCONNECT BOARD

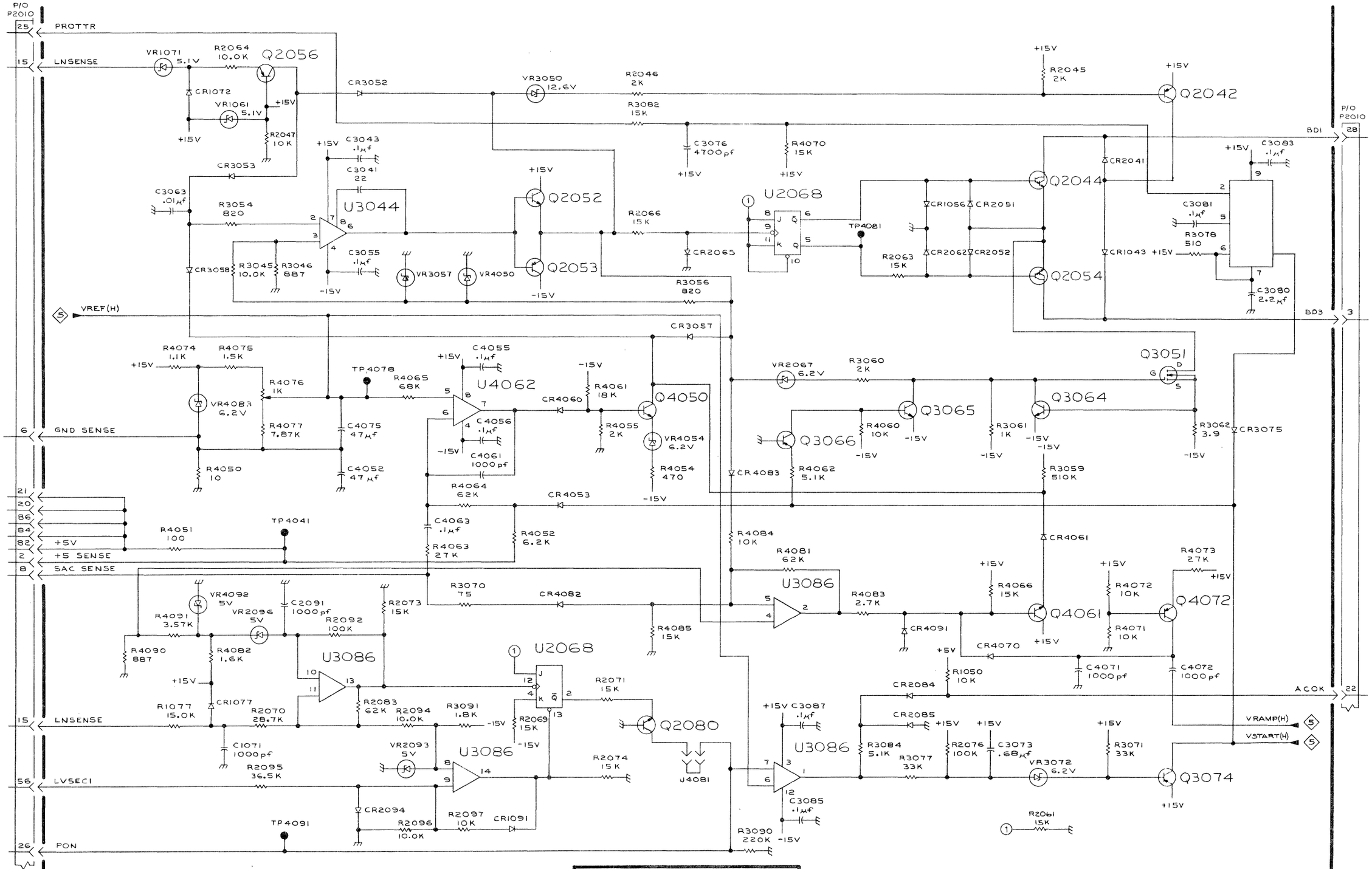


8501 DMU SERVICE

A20 POWER SUPPLY MOTHERBOARD

@ 2975-

MOTHER BOARD 3



8501 DMU SERVICE

REGULATOR 4

P/O P4010 4,D — PHOT 15 — T1012

CR3012 6 — CR3014 4 — CR3019 3 — CR3020 1

CR3056 12 — CR3062 10

+5V Q2044 R2036 15 Q2032 Q2042 -5V — R3016 62 — C3014 2200 pf — R2033 .2 — CR3018 — R2034 .6

TP1038 R1035 330 VR1036 27V

+5V Q3080 R3074 15 Q3072 Q3078 -5V — R3064 36 — C3068 .01μF — R3072 .1 — CR3063

TP1037 R1036 330 VR1039 12.6V

L3013 700μH — C1045 250μF — U1042 I G O — C1041 22μF — C1044 .1μF — CR1043

Q3022 R3024 1K — R3026 .51

L3082 11.2μH — L2086 4μH — R2072 5M — R2066 330 — TP2067 VR2068 5.6V

CR3032 CR3032 CR3049 CR3046 — C3044 0.022μF — R3048 6.8 — C2082 1200μF — C3073 290μF — L3052 270μH — C2048 .1μF — C1052 1000μF — C1047 .1μF

L1031 15μH — CR1031 — CR1034 — C1032 2.2μF — C1033 2.2μF

CR1086 — CR1065 — U1074 I G O — CR1064 — J3099 R L — R1073 2.67K — C1066 1000μF — C1059 1000μF — CR1079 — R1071 243 — R1084 1K — C1076 .1μF — Q1091 — CR1092 — VR1097 15V — C1058 22μF — Q1086 — CR1061 — C1056 22μF

R1051 1K — TP1051 — VR1051 16V

2,B PCAPS(H) 14
1,A PSHEILD(H) 13
F LVSEC 1 (H)
28 LVSEC 2 (H)

P/O P4010 K,9 — +24 SQW
11 — +24 V
13 — +24 DRVR
L,10 — +12 SQW
P — +12 DRVR
12 — +12

C4021 .1μF — R4023 360K — C4012 0.1μF — U4013 — C4014 0.1μF — C4027 0.1μF — R3012 510 — R2011 2K — +15V — -15V — R4025 20K — R4026 1M — R4033 13.3K — R4034 82.5K — R4021 25.5K — C4020 2.2μF — CR4047 — R3011 3.3K — C4010 .47μF

L1011 350μH — 3A F3010 — C3014 390μF — C1040 100μF — C1033 .1μF — TP4031 — +24V P/O P4010 M,11

VSTART
VRAMP
VREF
4

L2022 105μH — F3034 5A — L3035 12μH — C4032 290μF — C2034 100μF — C2036 .1μF — +12 N,12

C4028 0.1μF — R2044 2K — R4041 510 — C4036 .1μF — U4037 — C4046 .1μF — C4047 .1μF — R4030 20K — R4031 1M — R3041 3.3K — C4040 .47μF — CR4045 — R3040 100 — TP4012 — R3042 33.2K — R4044 13.3K — C4042 2.2μF — R4043 33.2K — +12 SENSE B̄

P/O A22 PS REGULATOR BOARD

-12V 14

U2064C — R1054 15K — -15V — J2057 — SAC SENSE D̄

U2064B — R2055 1K — J2058 — +5V 20,21,W,X,Y

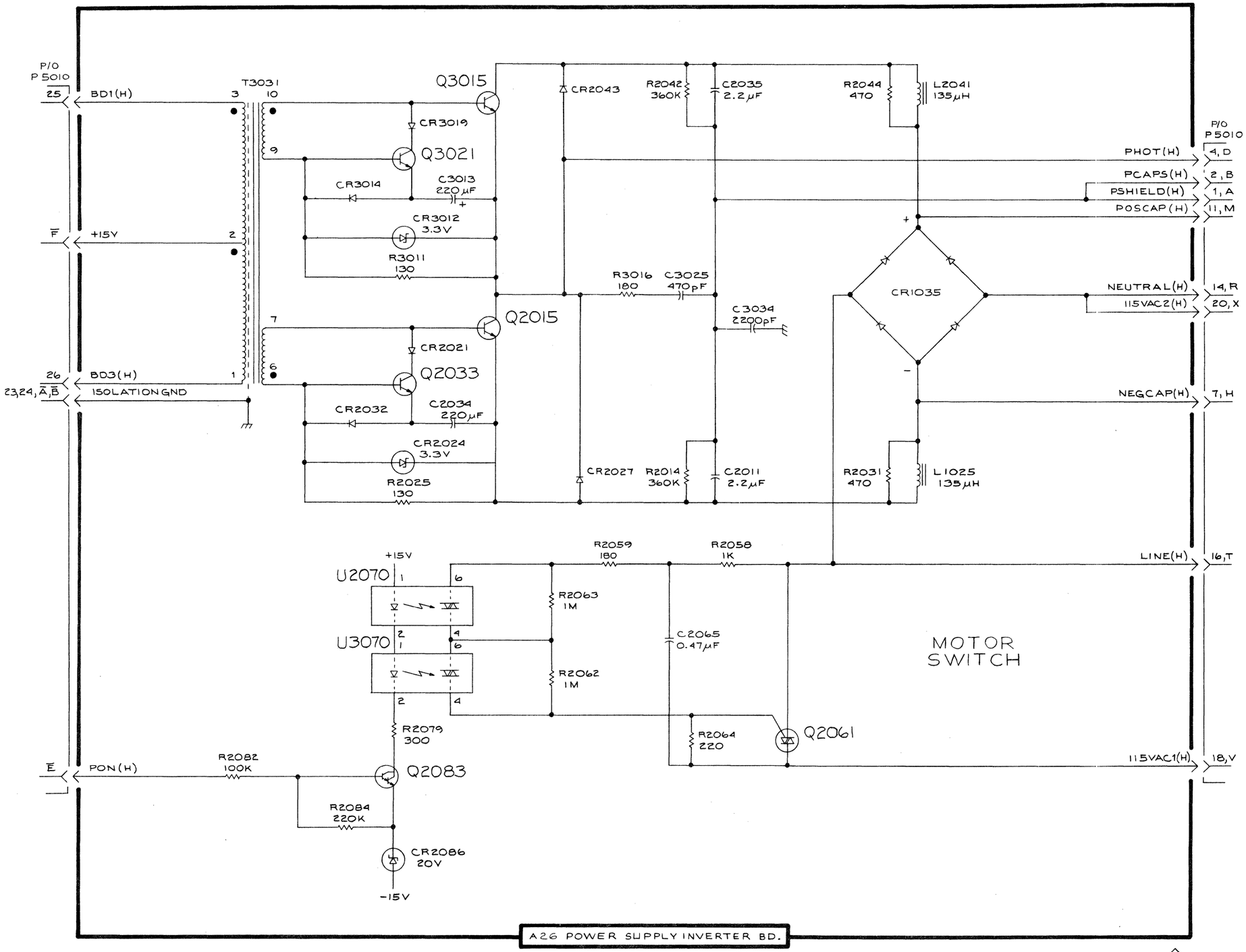
U2064A — R1055 30K — -15V — J2065 — GND 16,17,18,19,T,U,V

U2064D — R2061 1K — R2062 100K — R1053 14.7K — -15V — J2056 — PROTTR (H) 25

-5V
+15V Ē
-15V 27

LNSENSE(H) 15 L -

A24 POWER SUPPLY SECONDARY BD.



A26 POWER SUPPLY INVERTER BD.

+5V

+15V

R1027 3.3K

R1026 3.3K

R1025 3.3K

R1024 3.3K

R1028 10K

R1012 750

U1010 74LS00

RESTART

S1024

HALT/RUN

S1014

DC ON/OFF

S1045

P/O J15

RST (L)

R/H (H) (H)

POWER ON (L)

AC ON(H)

DS1032

STBY

PROC BUSY (L)

R1022 130

DS1038

PROC BUSY

GND

+15V

+5V

C1027 0.1

DS1052

DC ON

A30 FRONT PANEL BOARD

8501 DMU SERVICE

@ 2975-

FRONT PANEL 7

P1 P/O

BDAL15(L) BDAL14(L) BDAL13(L) BDAL12(L) BDAL11(L) BDAL10(L) BDAL9(L) BDAL8(L) BDAL7(L) BDAL6(L) BDAL5(L) BDAL4(L) BDAL3(L) BDAL2(L) BDAL1(L) BDAL0(L)

99 97 95 93 91 89 87 85 83 81 79 77 75 73 55 53

BDAL Ø(L) – BDAL 15(L)

+12V

R23 464 Q1

+5V R7 2K

R22 422 C82 .47μF C98 .01μF

E37 3245

+12V C34 .47μF

+3V A (SOURCE)

PH 1 L
PH 2 L
PH 3 L
PH 4 L

R2 10 RPH 1 H
R4 10 RPH 2 H
R18 10 RPH 3 H
R3 10 RPH 4 H

MSTB L

+12V
D14 RPH 1 H
D15 RPH 2 H
D13 RPH 3 H
D1 RPH 4 H

+5V R1 2K

1621-7

+12V C35 .47μF

RPH 1 H
RPH 2 H
RPH 3 H
RPH 4 H
MCOMP H

WIPI RQ H
WEVI RQ H
WIOI RQ H
WRESET L
WBUSY H
WREPLY H

CONTROL CHIP

WMIB 16 L
WMIB 17 L

WMIB Ø L … WMIB 15 L
WAIT H

C3 .47μF

E34 1631-15

+12V C39 .47μF

WMIB Ø L … WMIB 15 L

OPTIONAL

RPH 1 H
RPH 2 H
RPH 3 H
RPH 4 H
MCOMP H
MSTB L
MROM DIS L

C2 .47μF

-3.9

+5V RB 2K

E30 1611

+12V C23 .47μF

RPH 1 H … RPH 4 H
WMIB Ø L … WMIB 15 L
WAIT H

DATA CHIP

WDAL Ø H
WDAL 1 H
WDAL 2 H
WDAL 3 H
WDAL 4 H
WDAL 5 H
WDAL 6 H
WDAL 7 H
WDAL 8 H
WDAL 9 H
WDAL 10 H
WDAL 11 H
WDAL 12 H
WDAL 13 H
WDAL 14 H
WDAL 15 H

C1 .47μF

E31 1631-7

+12V C36 .47μF

WMIB Ø L … WMIB 11 L
WMIB 13 L … WMIB 21 L

MICROM Ø

RPH 1 H
RPH 2 H
RPH 3 H
RPH 4 H

MROM DISABLE L

C4 .47μF

E32 1631-10

+12V C37 .47μF

RPH 1 H … RPH 4 H
WMIB Ø L … WMIB 11 L
WMIB 13 L … WMIB 21 L

MICROM I

MROM DISABLE L

C33 .47μF

C5 33pF WMIB Ø L
C6 33pF WMIB 1 L
C9 33pF WMIB 2 L
C7 33pF WMIB 3 L
C8 33pF WMIB 4 L
C12 33pF WMIB 5 L
C21 33pF WMIB 6 L
C14 33pF WMIB 7 L
C16 33pF WMIB 8 L
C18 33pF WMIB 9 L
C20 33pF WMIB 10 L
C22 33pF WMIB 11 L
C17 33pF WMIB 12 L
C11 33pF WMIB 13 L
C13 33pF WMIB 14 L
C10 33pF WMIB 15 L
C15 33pF WMIB 16 L
C19 33pF WMIB 17 L

DC005 E39

BDAL 15 L
BDAL 14 L
BDAL 13 L
BDAL 12 L
REC
XMIT
WDAL 15 H
WDAL 14 H
WDAL 13 H
WDAL 12 H

WDAL 13 H – WDAL 15 H

DC005 E38

BDAL 11 L
BDAL 10 L
BDAL 9 L
BDAL 8 L
REC
XMIT
WDAL 11 H
WDAL 10 H
WDAL 9 H
WDAL 8 H

DC005 E29

BDAL 7 L
BDAL 6 L
BDAL 5 L
BDAL 4 L
BUSY
REC
XMIT
WDAL 7 H
WDAL 6 H
WDAL 5 H
WDAL 4 H

DC005 E24

BDAL 3 L
BDAL 2 L
BDAL 1 L
BDAL Ø L
REC
XMIT
JA3
JA2
JA1
WDAL 3 H
WDAL 2 H
WDAL 1 H
WDAL Ø H

WDAL Ø H – WDAL 3 H

WDOUT H
WWB H
WIAK H
WSYNC H
WDIN H

REC H
DMGCY H
DMGCY (Ø) H

BUS TIME OUT

P/O P1 38

TF CLR L
MTOE L
PH3 H
RPLY H
PH 4 L
INIT (1) L
WDOUT H
PH 2 L
WSYNC H
PH 3 L
PH 1 L
WIAK H
WDAL 15 H
WDAL 14 H
WDAL 13 H
WDIN H
FDIN H
EVNT H
EF CLR L
HALT H
P FAIL H
PF CLR L
DC LO H
IRQ H

E22 74LS175
E10 74LS08
E21 74LS04
E9 74LS74
E15 74LS32
E26 74LS21
E20 8097
E16 74LS08
E27 74LS174
E17 74LS74
R14
W3
E10 74LS27
AK1
+3V 7497 E23
STB
EN/IN Y
CLR
EN/OUT Z
E4 74LS10
E36 E14 E1
+5V
680 330
1 BDAL 15 L
2 BDAL 14 L
6 BDAL 13 L
4 BDAL 12 L
3 BDAL 11 L
5 BDAL 10 L
9 BDAL 9 L
7 BDAL 8 L
13 BDAL 7 L
11 BDAL 6 L
10 BDAL 5 L
12 BDAL 4 L
15 BDAL 3 L
14 BDAL 2 L
4 EVNT
5 B SACK L
7 B POK H
11 B DCOK H
10 B HALT L
9 BDMR L
1 BDAL 1
6 BDAL Ø
BIAKO L
BBS7 L
BDMGO L
BINIT L
BRPLY L
BIRQ5(L)
BIRQ6(L)
BDAL16(L)
BDOUT L
BWTBT L
BDIN L
BSYNC L
BDAL17(L)
BIRQ L

REPLY L
W REPLY H
W SYNC L
TERR H
STOP L
3V SOURCE
BPI J2-27
D OUT H
SYNC B H
SYNC H
ARI J1-9
B EVNT (L)
B SACK (L)
BPOK H
BDCOK H
B HALT L
DCLO L
BDMR L
BDAL7-BDAL15
WEV IRQ H
IAK H
WIO IRQ H
WIP IRQ H
W RESET L
BS7 H
DIN H
REC H
P FAIL H

WEV IRQ H
IAK H
W IO IRQ H
W IP IRQ H
W RESET
BS7 H
DIN H
REC H
P FAIL (L) H

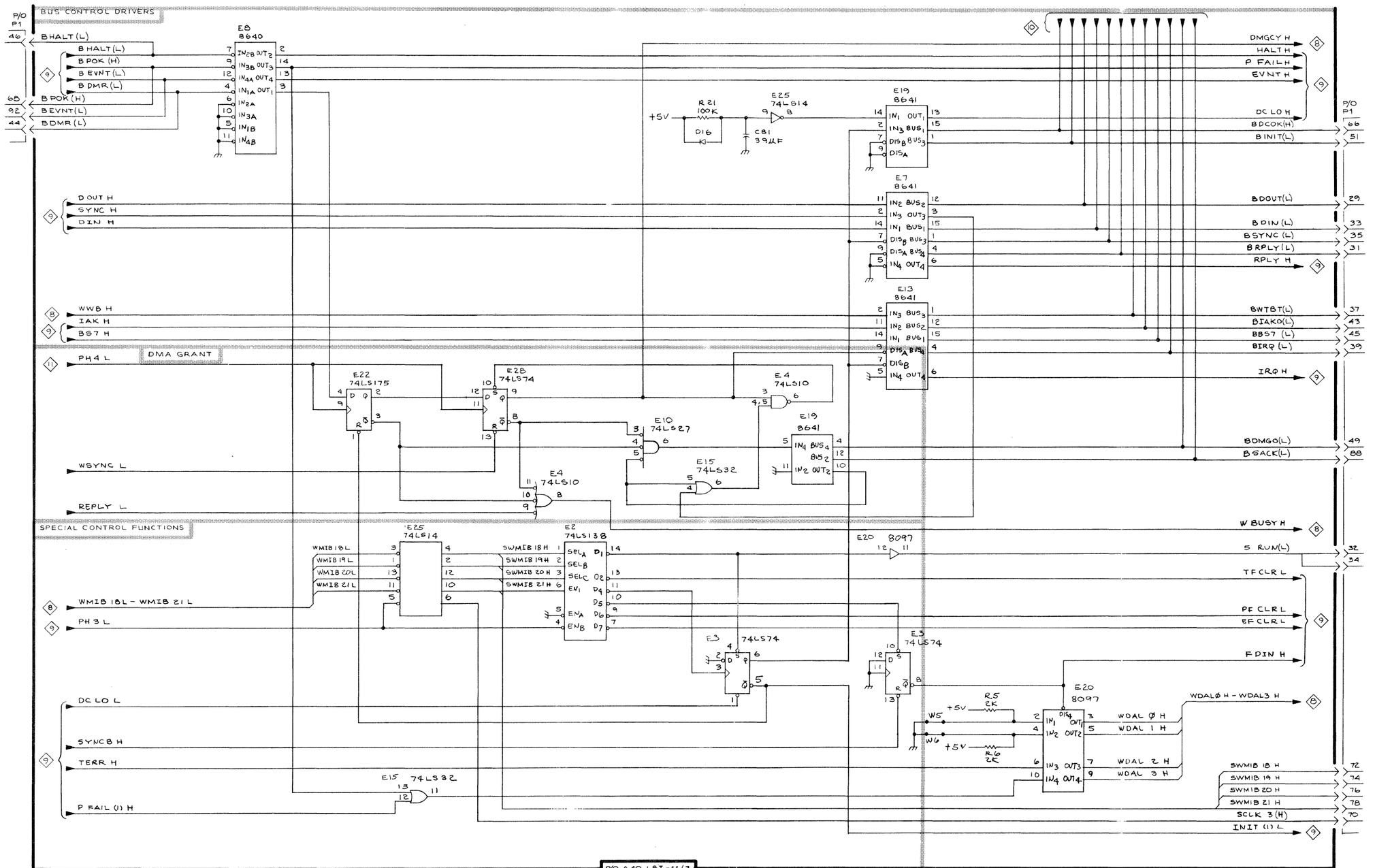
BANK 7 DECODER AND INTERRUPT CONTROL

P/O A50 LSI 11/2

BUS DRIVERS, RECEIVERS, AND TERMINATORS

8501 DMU SERVICE

BANK DECODER 9



P/O A40 LSI-11/2

8501 DMU SERVICE

@ 2975

BUS CONTROL DMA GRANT 10

FOUR PHASE CLOCK

+5V E6 31.578M

W1

+3V E5 74S74

+3V 74S74

E11 74S02

E18 74LS175

E18 74LS175

E18 74LS175

E18 74LS175

PH1L

PH2L

PH3L

PH3H

PH4L

MSTB L

+5V R12 2K

CHARGE PUMP

+12V +12V

C26 .47μF

R13 33

R15 33

+3V E12 74LS197

E11 74S02

C79 220pF

R19 470

E35 0026

+12V D2

C27 .47MF

C28 .47MF

D4

D5

D9

R9 120

R16 120

D10

D11

VDVR

+12V

C43 8μF

C44 8μF

+5V

C41 8MF

C42 8MF

C76 .01μF

C77 .01μF

C78 .01μF

C45 THRU C74 .01μF

E11 74S02

E11

C80 220 PF

R20 470

E35 0026

+12V D3

C29 .47MF

C30 .47MF

D6

D7

D8

C32 .47MF

R17 120

-VBB

C31 .47MF

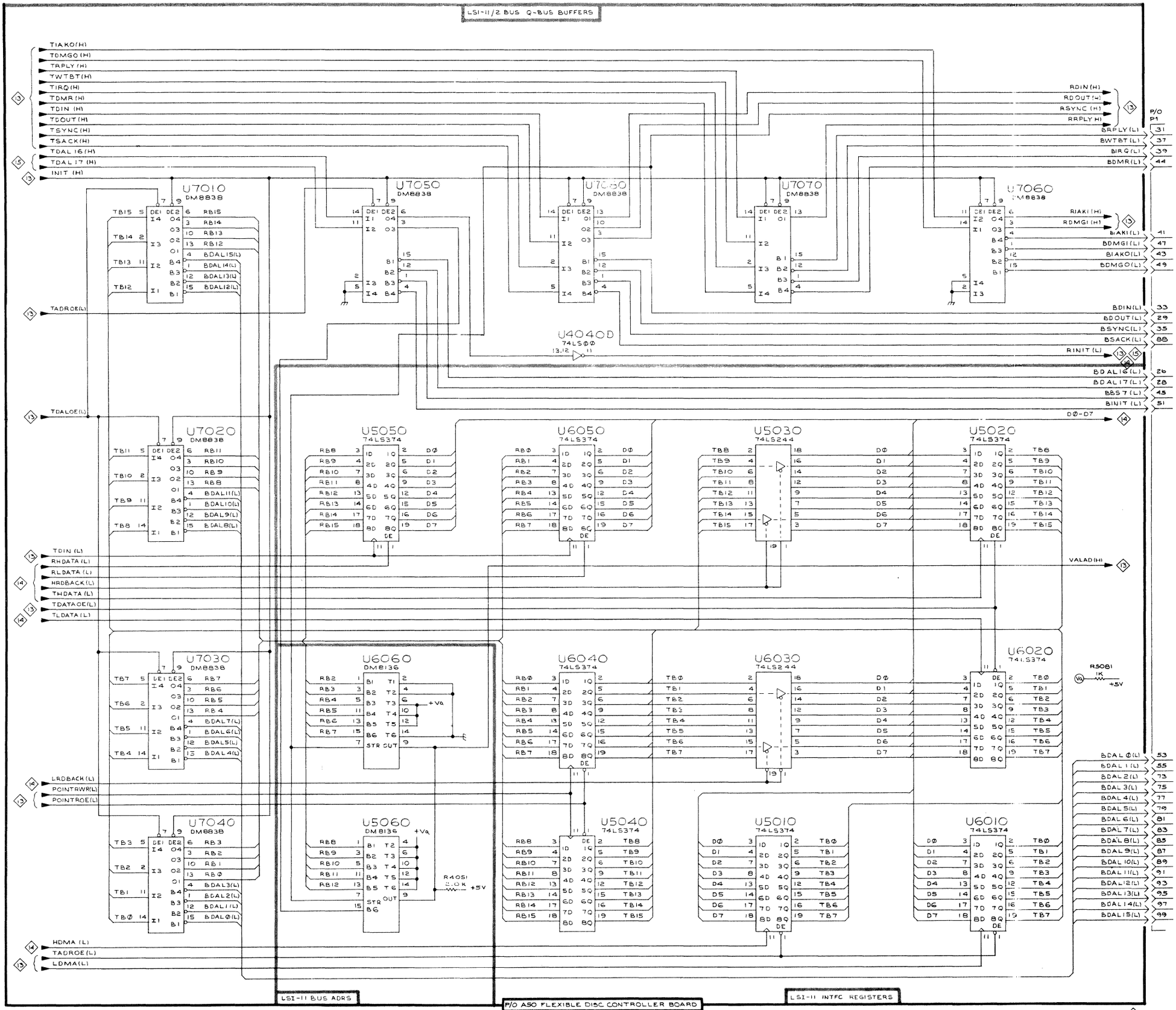
D12

P/O A40 LSI 11/2

8501 DMU SERVICE

2075- @

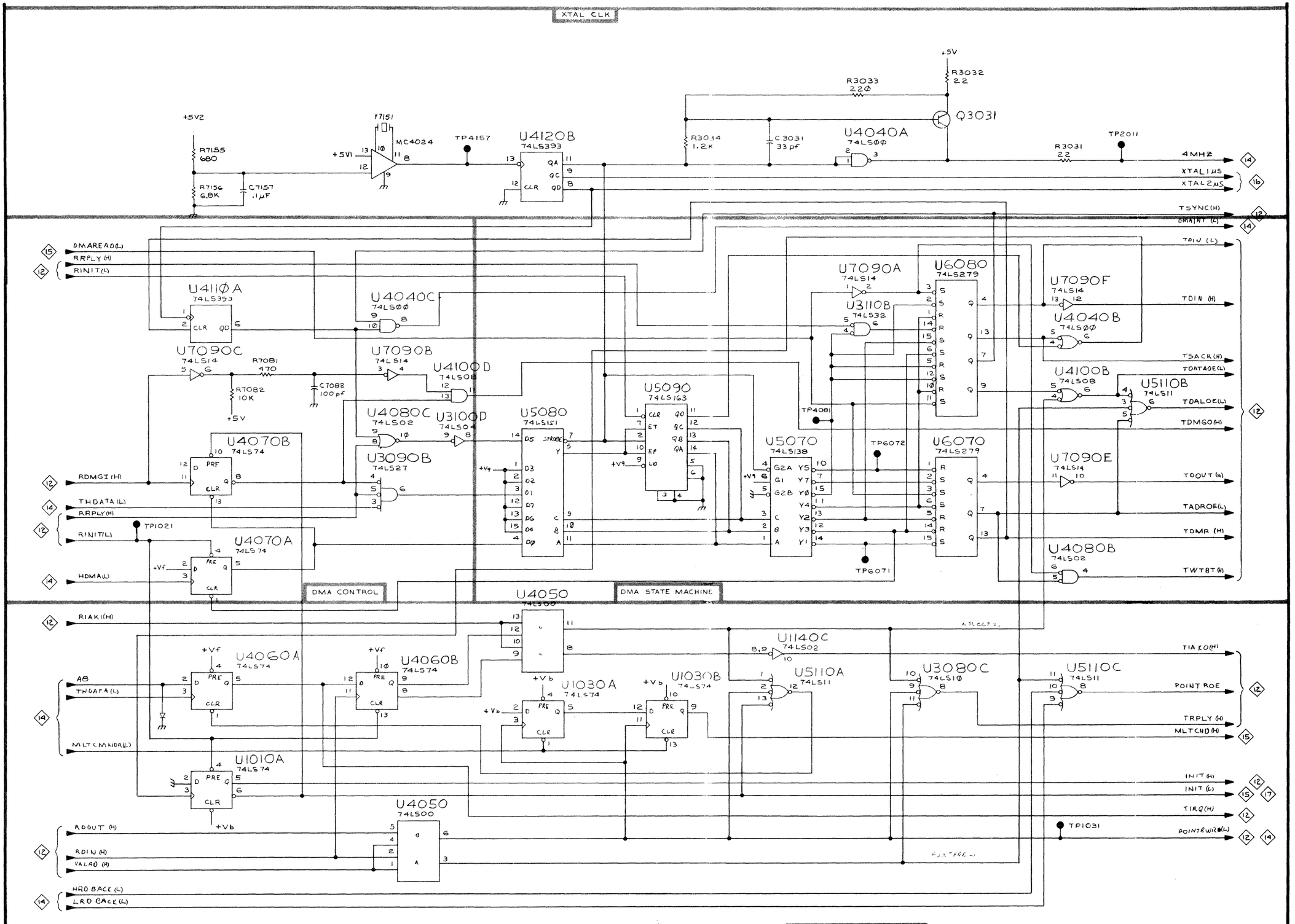
CLOCK ⟨11⟩



8501 DMU SERVICE

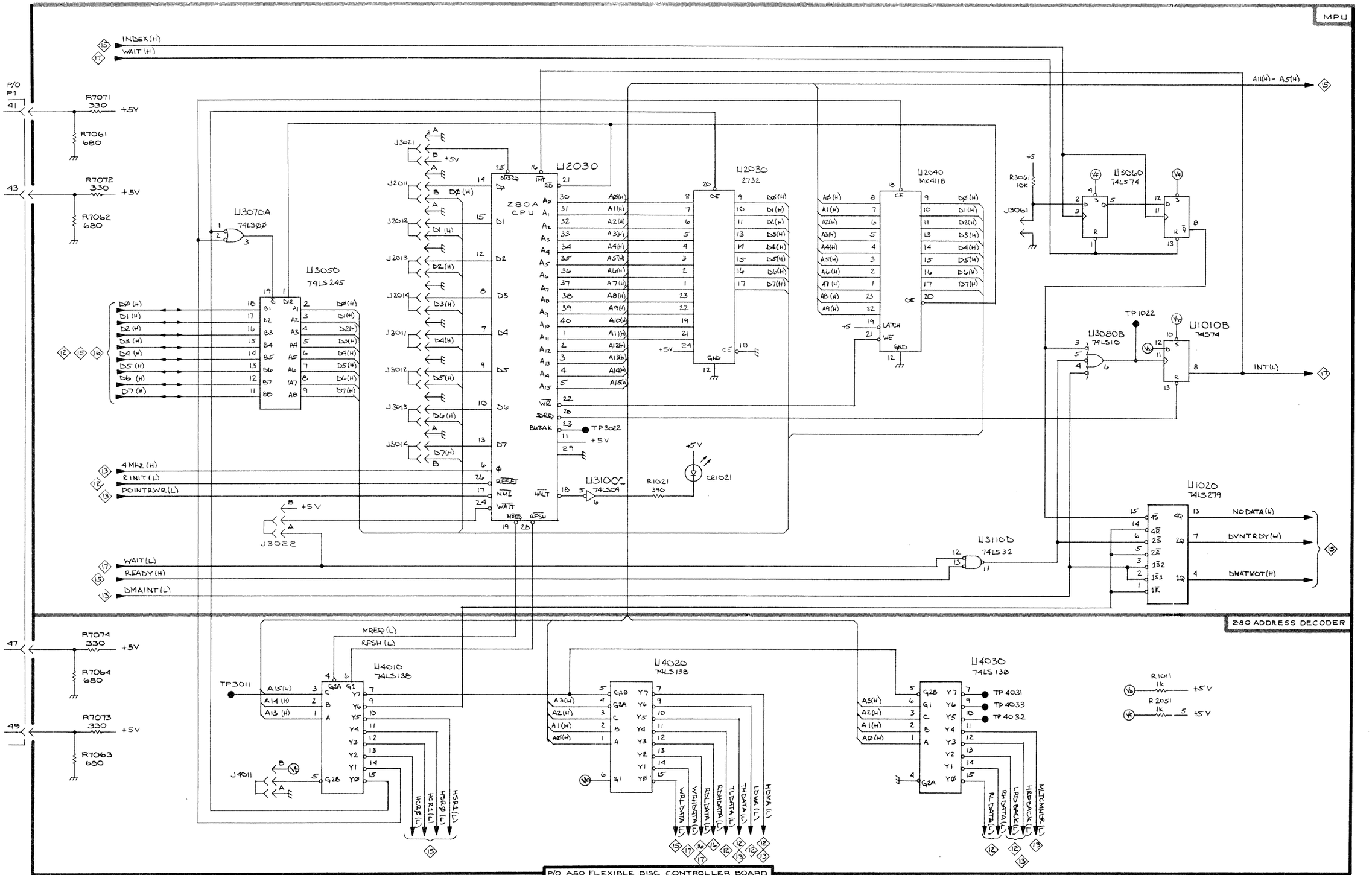
2975-

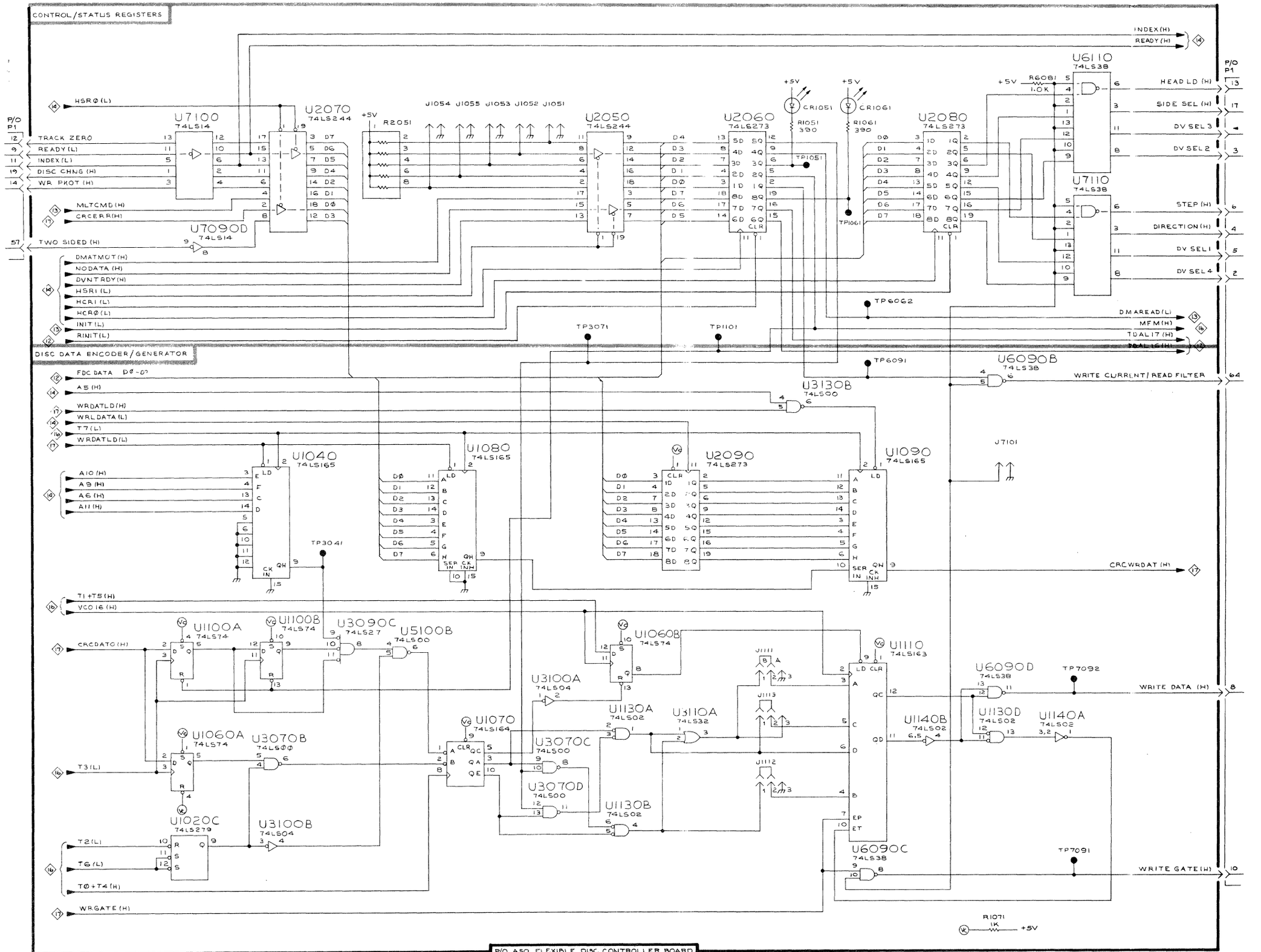
8501 BUS INTERFACE 12



8501 DMU SERVICE

DMA STATE MACHINE 13


MPU
INDEX(H)
WAIT(H)
P/O P1
41
43
47
49
R7071 330 +5V
R7061 680
R7072 330 +5V
R7062 680
R7074 330 +5V
R7064 680
R7073 330 +5V
R7063 680
A11(H)-A5(H)
U3070A 74LS00
U3050 74LS245
U2030 Z80A CPU
U2030 2732
U2040 MK4118
U3060 74LS74
U3080B 74LS10
U1010B 74S74
TP1022
INT(L)
U3110C 74LS04
R1021 390
CR1021
U3110D 74LS32
U1020 74LS279
NODATA(H)
DVNTRDY(H)
DMATMOT(H)
4MHz(H)
RINIT(L)
POINTRWR(L)
WAIT(L)
READY(H)
DMAINT(L)
J3022
Z80 ADDRESS DECODER
U4010 74LS138
U4020 74LS138
U4030 74LS138
TP3011
J4011
TP4031
TP4033
TP4032
R1011 1k +5V
R2051 1k +5V
P/O A50 FLEXIBLE DISC CONTROLLER BOARD
8501 DMU SERVICE
39% R80
Z80A 14


CONTROL/STATUS REGISTERS
DISC DATA ENCODER/GENERATOR
U7100 74LS14
U2070 74LS244
U2050 74LS244
U2060 74LS273
U2080 74LS273
U6110 74LS38
U7110 74LS38
U7090D 74LS14
R2051
R1051 330
R1061 390
R6081 1.0K
TP1051
TP1061
TP6062
TP3071
TP1101
TP6091
INDEX(H)
READY(H)
HEAD LD (H)
SIDE SEL (H)
DV SEL 3
DV SEL 2
STEP (H)
DIRECTION (H)
DV SEL 1
DV SEL 4
TRACK ZERO
READY(L)
INDEX(L)
DISC CHNG (H)
WR PROT (H)
MLTCMD (H)
CRCERR(H)
TWO SIDED (H)
HSR0 (L)
DMATMOT(H)
NODATA (H)
DVNTRDY(H)
HSR1 (L)
HCR1 (L)
HCR0(L)
INIT (L)
RINIT(L)
DMAREAD(L)
MFM(H)
TDALI7 (H)
FDC DATA D0~D7
A5 (H)
WRDATLD(H)
WRL DATA (L)
T7 (L)
WRDATLD(L)
U1040 74LS165
U1080 74LS165
U2090 74LS273
U1090 74LS165
U3130B 74LS00
U6090B 74LS38
WRITE CURRENT/READ FILTER
J7101
A10 (H)
A9 (H)
A6 (H)
A11 (H)
TP3041
CRCWRDAT (H)
T1+T5(H)
VCO16 (H)
CRCDATO(H)
U1100A 74LS74
U1100B 74LS74
U3090C 74LS27
U5100B 74LS00
U1060B 74LS74
U1110 74LS163
U3100A 74LS04
U1070 74LS164
U1130A 74LS02
U3110A 74LS32
U3070C 74LS00
U3070D 74LS00
U1130B 74LS02
U1140B 74LS02
U1130D 74LS02
U1140A 74LS02
U6090D 74LS38
TP7092
WRITE DATA (H)
T3(L)
U1060A 74LS74
U3070B 74LS00
U1020C 74LS279
U3100B 74LS04
T2(L)
T6(L)
T0+T4(H)
WRGATE(H)
U6090C 74LS38
TP7091
WRITE GATE(H)
R1071 1K
+5V
P/O P1
P/O A50 FLEXIBLE DISC CONTROLLER BOARD

DISC DATA SERIAL/PARALLEL CONVERTER

PHASE-LOCK LOOP

P/O P1 16

MFM (H)

XTAL 2MS (H)

XTAL 1MS (H)

READ DATA (L)

RDMODE (L)

RDH DATA (L)

RDMODE (H)

DATAIN (H)

R7101 150 +5V

TP2151

TP3193

TP3142

U2150 74LS3164

U2100 74LS374

U4120A 74LS393

U3140A 74LS74

U2140 74LS164

U2120 74LS164

U2130 74LS164

U5190A 74LS157

U4090E 74LS04

U5120D 74LS08

U5120A 74LS08

U5120C 74LS08

TP7101

U7100D 74LS19

R6132 10.5K

C5131 130pF

U6130B 74LS221

R6131 5.23K

C6131 130pF

U6130A 74LS221

U5140B 74LS157

U7140 4044

R7142 820

C7141 .22MF

R7144 1K

C7155 18pF

4024

R7141 2K

C7143 .001MF

VCOIG(H)

TP6053

U5150 74LS04

U6140A 74LS74

U6140B 74LS74

SHFTENCK (L)

T1+T5 (H)

CRCRDDAT (H)

CRCRDDAT(H)

R7153 20 +5V1

R7151 20 +5V2

R7152 20 +5V3

R7154 20 +5V4

C7154 0.1μF

C7152 0.1μF

C7151 0.1μF

C7153 0.1μF

ADRS MARK DETECTORS

U3090A 74LS27

U3080A 74LS10

U3120 74S133

U1120 74330

U1130C 74LS02

U5140C 74LS157

U5140D 74LS157

U6150B 74LS74

U4190 74LS393

U3150 74LS138

U3130D 74LS08

U3130A 74LS08

U3130C 74LS08

U3140B 74LS74

WRBYTE(H)

T0+T4(H)

T1+T5(H)

T2(L)

T3(L)

T4(L)

T6(L)

T7(L)

T3+T7(H)

AMDET(L)

RDWAIT(L)

RDLDATA(L)

U2110 74LS374

TP1023 TP1041 TP1151 TP3101 TP3131 TP3132 TP4034 TP4071 TP4121 TP6041 TP7041 TP7102 TP7145

TP1152 TP7011 +5V

R6141 1K +5V

D0(H)-D7(H)

P/O A50 FLEXIBLE DISC CONTROLLER BOARD

BIT CELL TIMING

DATA READ MODE CONTROL

RDLDATA (L)

P/O P1 12, 9, 11

R7092 150 +5V
R7103 150
R7102 150

U4110B 74LS393
T1+T5 (H)

U4130A 74LS20

U4080D 74LS02

U5130A 74LS74

U5130B 74LS74

U5100A 74LSØØ

TP3141

RDMODE (H) ◇16

U6100 74LS74
AMDET (L)
T3+T7 (H)

TP4131

U3040A 74S02

U1050A 74S74

U4090F 74LS04

U4130B 74LS20

U4090A 74LS04

INT (L)

RDWAIT (L) ◇16

DMA WRITE MODE CONTROL

U1050B 74S74

U3040D 74S02

TP3021

WAIT (L) ◇14

U3040B 74S02
WRHDATA (L)

U4100A 74LS08

WRBYTE (H)

U5100D 74LSØØ

U4080A 74LS02

U3040C 74S02

WAIT (H)

R7091 150 +5V
R7051 150
R7093 150

U4150A 74LS74

U4150B 74LS74

U4090B 74LS04

WRDATLD (L)
WRDATLD (H) ◇15
WRGATE (H)

INIT (L) ◇13

P/O P1 56, 65, 100

+5V — 5V PLANE — FIFTY-TWO 0.1µF CAPACITORS — C7121 2.5µF — C7021 2.5µF — GND PLANE — P/O P1 25, 36, 42, 52, 69, 80, 86, 96

CRC GENERATOR/CHECKING

U4100C 74LS08

TØ+T4 (H)

U7120B 74LS74

U7130 MC8506

U7120A 74LS74

U6100B 74LS74

CRCDATO (H) ◇15

A7 (H)

CR2012

U3110C 74LS32

U6120A 74LS74

U6120B 74LS74

TP6061

CRCERR (H)

T4 (L)
T2 (L)
CRCWRDAT (H) ◇15
CRCRDDAT (H)
A10 (H) ◇16
A8 (H) ◇14

CR2011

R1071 1K +5V
R7121 1K +5V
R6141 1K +5V

P/O A50 FLEXIBLE DISC CONTROLLER BOARD

P/O P1

53 BDAL0 (L)
55 BDAL1 (L)
73 BDAL2 (L)
75 BDAL3 (L)
77 BDAL4 (L)
79 BDAL5 (L)
81 BDAL6 (L)
83 BDAL7 (L)
85 BDAL8 (L)
87 BDAL9 (L)
89 BDAL10 (L)
91 BDAL11 (L)
93 BDAL12 (L)
95 BDAL13 (L)
97 BDAL14 (L)
99 BDAL15 (L)

P5066 RUN TEST

OUT EN (L) <20>

U5060 8838: D0(H) 11, D1(H) 14, D2(H) 5, D3(H) 2 → DA0(H) 10, DA1(H) 13, DA2(H) 6, DA3(H) 3
U5040 8838: D4(H) 11, D5(H) 14, D6(H) 5, D7(H) 2 → DA4(H) 10, DA5(H) 13, DA6(H) 6, DA7(H) 3
U5030 8838: D8(H) 11, D9(H) 14, D10(H) 5, D11(H) 2 → DA8(H) 10, DA9(H) 13, DA10(H) 6, DA11(H) 3
U5010 8838: D12(H) 11, D13(H) 14, D14(H) 5, D15(H) 2 → DA12(H) 10, DA13(H) 13, DA14(H) 6, DA15(H) 3

DA0 - DA15 (L) <19>

	WRITEL (L)	WRITEH (L)	WRITEL (L)	WRITEH (L)
	U2160	U2080	U1160	U1080
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA0 (H)	2	8	0 (H) 2	8 (H) 2
RAS (L)	4	4	4	4
	D0(H)	D8(H)	D0(H)	D8(H)
	U2150	U2070	U1150	U1070
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA1 (H)	2	9	1 (H) 2	9 (H) 2
RAS (L)	4	4	4	4
	D1(H)	D9(H)	D1(H)	D9(H)
	U2140	U2060	U1140	U1060
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA2 (H)	2	10	2 (H) 2	10 (H) 2
RAS (L)	4	4	4	4
	D2(H)	D10(H)	D2(H)	D10(H)
	U2130	U2050	U1130	U1050
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA3 (H)	2	11	3 (H) 2	11 (H) 2
RAS (L)	4	4	4	4
	D3(H)	D11(H)	D3(H)	D11(H)
	U2120	U2040	U1120	U1040
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA4 (H)	2	12	4 (H) 2	12 (H) 2
RAS (L)	4	4	4	4
	D4(H)	D12(H)	D4(H)	D12(H)
	U2110	U2030	U1110	U1030
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA5 (H)	2	13	5 (H) 2	13 (H) 2
RAS (L)	4	4	4	4
	D5(H)	D13(H)	D5(H)	D13(H)
	U2100	U2020	U1100	U1020
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA6 (H)	2	14	6 (H) 2	14 (H) 2
RAS (L)	4	4	4	4
	D6(H)	D14(H)	D6(H)	D14(H)
	U2090	U2010	U1090	U1010
CASL (L)	15	15	CASH (L) 15	CASH (L) 15
DA7 (H)	2	15	7 (H) 2	15 (H) 2
RAS (L)	4	4	4	4
	D7(H)	D15(H)	D7(H)	D15(H)

All: D_{IN} D_O, pin 3

4116: V_{DD} 8 +12V; V_{CC} 9 +5V; CAS 15; DA 2; RAS 4; WRITE 3; A0 5; A1 7; A2 6; A3 12; A4 11; A5 10; A6 13; D_{IN} D_{OUT} 14 D--; V_{BB} 1 -5V; V_{SS} 16

DRIVEN (L) <19>

WRITEL (L)
WRITEH (L)
CASL (L)
CASH (L)
RAS (L)
A0 - A6 (H) <19>

R4118 1K ① +5V

P/O BUS BUFFERS MEMORY

P/O A60 32K MEMORY BOARD

P/O BUS BUFFERS | ADDRESS LATCH | ADDRESS MUX

P/O P1

45 BBS 7 (L)
26 BDAL 16 (L)
28 BDAL 17 (L)
37 BWTBT (L)
41
43
47
49
35 BSYNC (L)
29 BDOUT (L)
33 BDIN (L)
RPLY (H)
BUS ACTIVE (H)
DAQ-DA15 (H)
RFCLK (H)
RFRSH (H)
MUXA (H)
21 65 +5V
27 71 +12V
96,89, 80,69 25,36 42,52 GND
23 67 -5V

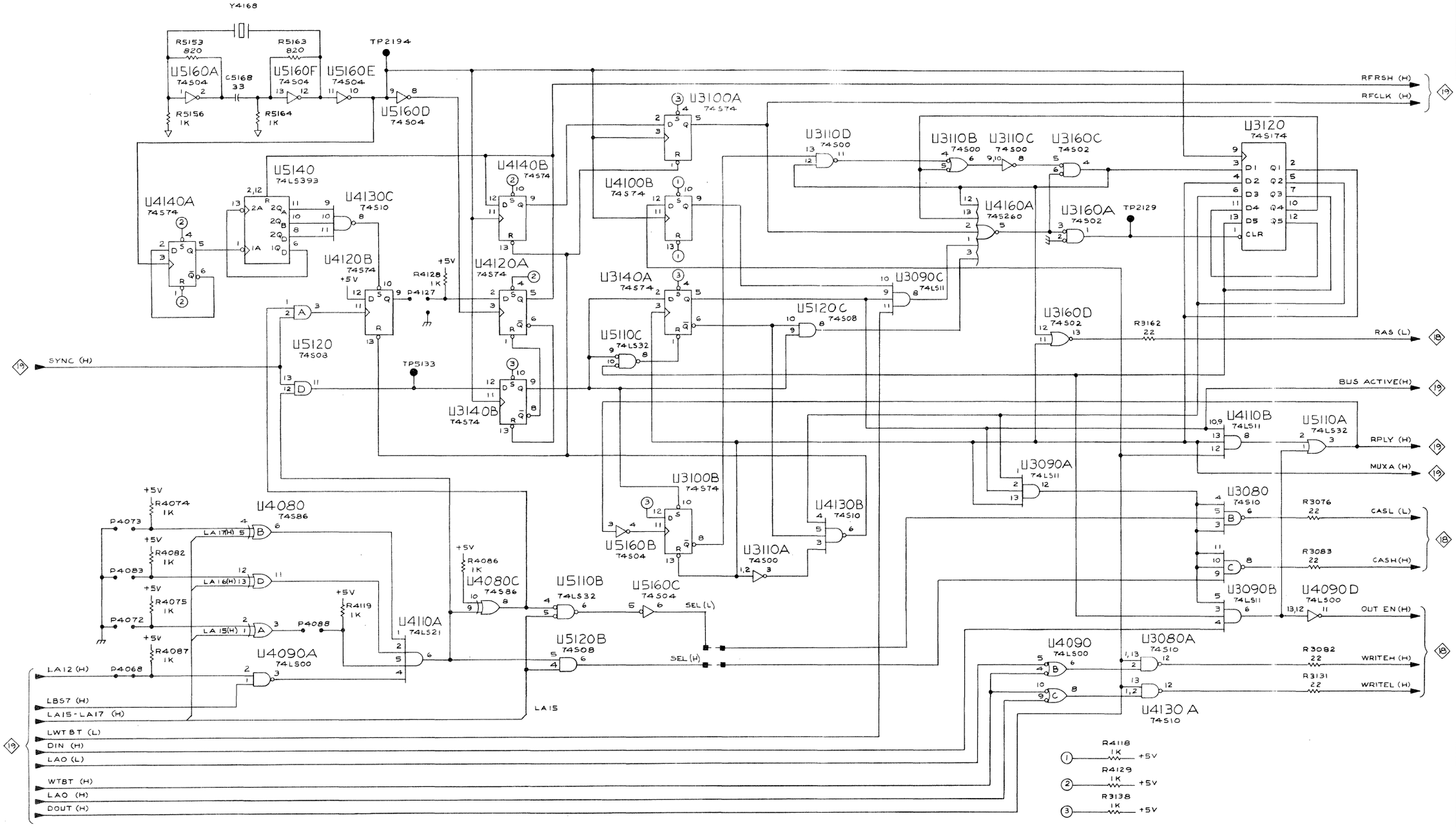
U5080 8837
U5090 8838
U4060 74LS175
U3160 74S02
U4040 74LS373
U4030 74LS373
U3060 3242

DRVEN (L)
BS7
DA16
DA17
DA1 (H)
DA2 (H)
DAQ (H)
DA3 (H)
DA4 (H)
DA5 (H)
DA6 (H)
DA7 (H)
LATCH (L)
DA8 (H)
DA9 (H)
DA10 (H)
DA11 (H)
DA12 (H)
DA13 (H)
DA14 (H)
DA15 (H)
LA1
LA2
WTBT (H)
LBS 7 (H)
LA15 - LA17 (H)
LA16 (H)
LA17 (H)
LA15 (H)
COUNT
RFRSH EN
ROW EN
R3061 39 AQ (H)
R3063 39 A1 (H)
R3062 39 A2 (H)
R3066 39 A3 (H)
R3067 39 A4 (H)
R3068 39 A5 (H)
R3065 39 A6 (H)
LA12 (H)
LAQ (H)
LAQ (L)
LWTBT (L)
SYNC (H)
DOUT (H)
DIN (H)
BPRLY (L)

TP3011
VR1505
12.6V
C5168 47
TWENTY FIVE 0.1 CAPS
.75
C3018 22
SIXTEEN 0.1 CAPS
TP4138
TP3026
VR5043 5.1V
C5041 22
SIXTEEN 0.1 CAPS
R5044 300

P/O A60 32K MEMORY BOARD

8501 DMU SERVICE @ 2975- LATCHES/BUFFERS 19



P/O A60 32K MEMORY BOARD

8501 DMU SERVICE

REFRESH & TIMING/CONTROL LOGIC

MUX

DATA/ADDRESS TRANSCEIVERS

ADDRESS

LD - CTR (L)
02 (L)
SWAP BYTE (H)
LD - ADDR (L)
DMA DATA (H)
PACKED (H)
06 (L)
04 (L)
DATA BUS (L)
TRO (H)
RED (H)
OUT (H)
TO (H)
RB ENABLE (H)

U2040A 74LS08

U4010A 74LS32

U2040B 74LS08

LD-CTR (L)
02 (L)
LD-ADDR (L)

D0(H),D1-D6(H),D8(H)
D0-D3(H)
D4-D7(H)
D0-D15(H)
DMA BYTE (H)
CTR0-CTR7(H)

U7050 8838
U3130 74LS191
U4130 74LS86
U3110 74LS191

U6100 74LS153
U5080 74LS02
U5100 74LS32
U6080 74LS153

U7030 8838
U4120 74LS191
U3100 74LS191

U7020 8838
U4070 74LS191
U7100 74LS191

U4090 74LS153
U5090 74LS153
U6090 74LS157

U7010 8838
U4080 74LS191
U3090 74LS191

CTR OVERFLOW (L)
ADDR0 - ADDR7 (H)
ADDR OVERFLOW(L)

STROBE MUX

WON (H)
BDIO (H)
RB ERR (H)
BON (H)
AOF ERR (H)
FR ERR (H)
ABORT (H)
PERR (H)
RW (H)
DNB (H)
ONB
DMA-ERR (H)
ERR (H)
TM ERR (H)
OR ERR (H)

IT S (H)
I F (H)
BO (H)
DRO (H)

3D ADDRESS

U2050B 74LS00

U6050 8136
U6070 8136

R6061 2.2K
R6050 2.2K
+V2
+5V

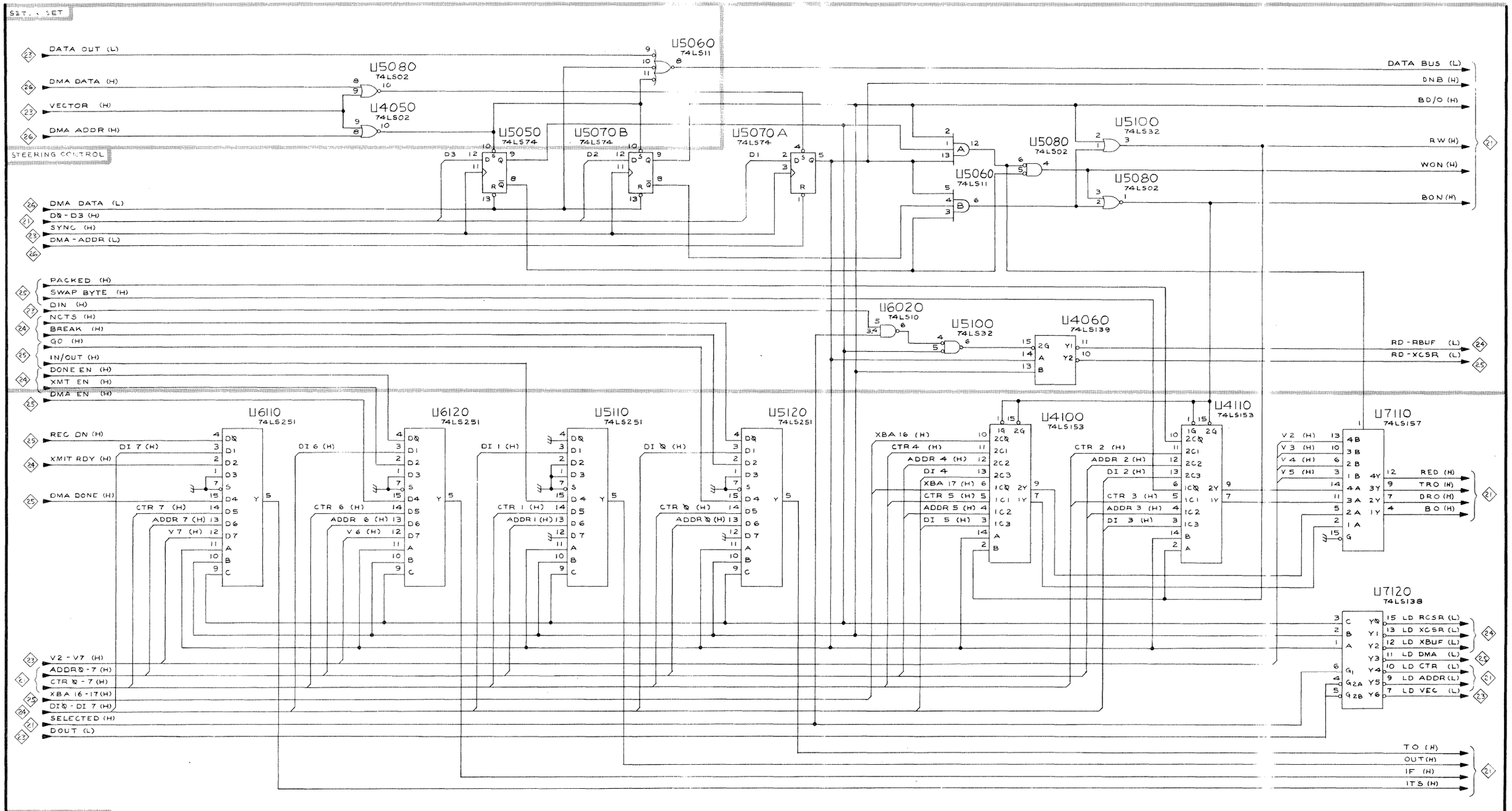
BS7 (H)
SYNC (H)

P/O P1

BAD 0 (L) 53
BAD 1 (L) 55
BAD 2 (L) 73
BAD 3 (L) 75
BAD 4 (L) 77
BAD 5 (L) 79
BAD 6 (L) 81
BAD 7 (L) 83
BAD 8 (L) 85
BAD 9 (L) 87
BAD 10 (L) 89
BAD 11 (L) 91
BAD 12(L) 93
BAD 13(L) 95
BAD 14(L) 97
BAD 15(L) 99

SELECTED (H)

P/O ATO I/O BOARD



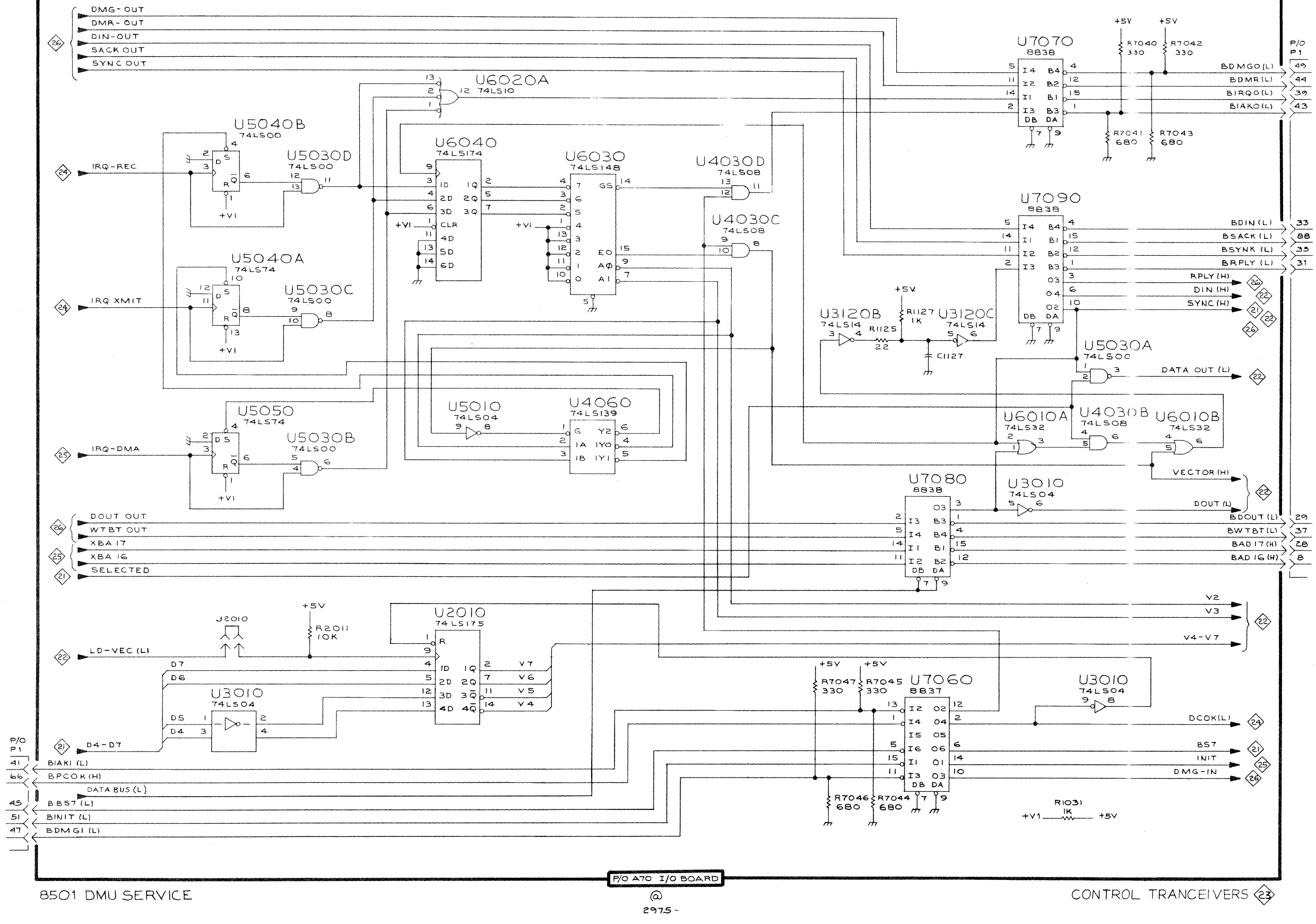
P/O A70 I/O BOARD

8501 DMU SERVICE

@

2975-

PORT SELECTION/STEERING 22


DMG-OUT
DMR-OUT
DIN-OUT
SACK OUT
SYNC OUT
U6020A
74LS10
U5040B
74LS00
U5030D
74LS00
IRQ-REC
U6040
74LS174
U6030
74LS148
U4030D
74LS08
U4030C
74LS08
U5040A
74LS74
U5030C
74LS00
IRQ XMIT
U5050
74LS74
U5030B
74LS00
IRQ-DMA
U5010
74LS04
U4060
74LS139
U7070
8838
R7040 330
R7042 330
R7041 680
R7043 680
BDMGO(L)
BDMR(L)
BIRQO(L)
BIAKO(L)
U7090
8838
BDIN(L)
BSACK(L)
BSYNK(L)
BRPLY(L)
RPLY(H)
DIN(H)
SYNC(H)
U3120B
74LS14
R1125 22
U3120C
74LS14
R1127 1K
C1127
U5030A
74LS00
DATA OUT(L)
U6010A
74LS32
U4030B
74LS08
U6010B
74LS32
VECTOR(H)
U7080
8838
U3010
74LS04
DOUT(L)
DOUT OUT
WTBT OUT
XBA 17
XBA 16
SELECTED
BDOUT(L)
BWTBT(L)
BAD 17(H)
BAD 16(H)
J2010
R2011 10K
U2010
74LS175
LD-VEC(L)
D7
D6
D5
D4
D4-D7
U3010
74LS04
V2
V3
V4-V7
U7060
8837
R7047 330
R7045 330
R7046 680
R7044 680
U3010
74LS04
DCOK(L)
BST
INIT
DMG-IN
R1031 1K
+V1
+5V
BIAKI(L)
BPCOK(H)
DATA BUS(L)
BBST(L)
BINIT(L)
BDMGI(L)
P/O A70 I/O BOARD

PARALLEL/SERIAL I/O CONVERTOR

START BIT DETECTOR

STEERING MUX

+5V
R2092 100K
C2091 4.0uf
U2090 74LS221
U1080 74LS32
U4040 74LS74
U4050B 74LS02
U4050 74LS02
U2020 74LS08
U5020 74LS93
U2060A 74LS02
U3050D 74LS08
U3040 74LS74 +V1
U3040B 74LS74 +V1
U3050A 74LS08
U1051D 74LS32
U3050C 74LS08
U2050C 74LS00
U2060B 74LS02
U2040C 74LS08
U1051E 74LS32
U3050B 74LS08
U4050D 74LS02
U4020 74LS93
U3010E 74LS04
U4030A 74LS08
U4010D 74LS32
U2070 64502
U5010E 74LS04
U6010 74LS32
U5010F 74LS04
U3060 74LS157
U3080 74LS157
U3120A 74LS14
U2110B 74LS11
R1031 1K

RD-XCSR (L)
GO (H)
J2085
H1
J2084
H3
D Ø
D 6
R (L)
GO-OUT (H)
SER IN (H)
LD-XCSR (L)
LD-RCSR (L)
RFD (L)
CLK (H)
DMA-XBUF (L)
LD-XBUF (L)
DMA-RBUF (L)
RD RBUF(L)
DC OK (L)
CLR (H)
2SB H
SER OUT(H)
BRK (H)
BREAK (H)
NCTS (H)
XMIT EN (H)
DONE EN (H)
IRQ-REC (H)
CTS(L)
IRQ-XMIT (H)
XMIT-RDY (H)
DMA -XMIT (L)
REC DN (H)
FR ERR (H)
ERR (L)
ERR (H)
P ERR (H)
OR ERR (H)
DIØ (H)
DI1 (H)
DI2 (H)
DI3 (H)
DI4 (H)
DI5 (H)
DI6 (H)
DI7 (H)
D0 (H)
D1 (H)
D2 (H)
D3 (H)
D8 (H)
D9 (H)
D10 (H)
D11 (H)
D7 (H)
D6 (H)
D5 (H)
D4 (H)
D12 (H)
D13 (H)
D14 (H)
D15 (H)
ADDR Ø (H)
PACKED (H)
SACK OUT (H)
NP
NB2
NB1
PEV
J2083
J2082
J2081
J2080
+V1
-12 V
TRC
RRC
RRI
TBRL
DRR
MR
SBS
PI
RRD
SFD
CLS2
CRL
CLS1
EPE
TBR 1 .. TBR 8
RBR 1 .. RBR 8
NC
GND
TRO
TBRE
DR
PE
OE
FE
P/O P1

U6130
74LS273

D8(H) D6(H) D5(H) D4(H) D3(H) D2(H) D1(H)

U1130C
74LS02

U2130E
74LS04

INIT(H)

U2130D
74LS04

U5130C
74LS08

U1110C
74LS00

U5130B
74LS08

DIϕ(H)

Q-LAT(L)

U2100
74LS279

+V1

U1070
74LS74

Dϕ(H)

LD-DMA(L)

U1130B
74LS02

RB-ENABLE(H)
DMA-EN(H)
XBA17(H)
XBA16(H)
SWAP BYTE(H)
PACKED(H)
IN/OUT(H)
R(L)
CLR(H)
GO-OUT(H)
TM ERR(H)
GO(H)

+V1

U1100A
74LS25

BRK(H)

U1080C
74LS32

U5130A
74LS08

U2120
74LS279

U1090C
74LS32

DMA-RBUF(L)
ERR(L)

DMA DONE(H)
RB ERR(H)

J2086
B
A
+V1

CTR OVERFLOW(L)
ϕ2(L)
RD-XCSR(L)

U1090D
74LS32

U1090B
74LS32

U1120
74LS279

ABORT(H)
AOF ERR(H)

U1090A
74LS32

ADDR OVERFLOW(L)
ϕ4(L)

U1080D
74LS32

U2040D
74LS08

11 IRQ-DMA(H)

U5130D
74LS08

U1100B
74LS25

U2130A
74LS04

DMA-ERR(H)

P/O
P1
21
65
36,25
52,42
80,69
92,86

+5V

C7049
22μf

C7082
22μf

TWENTY-SIX
0.1 μf
CAPACITORS

R1031
1K
+V1
+5V

P/O A70 I/O BOARD

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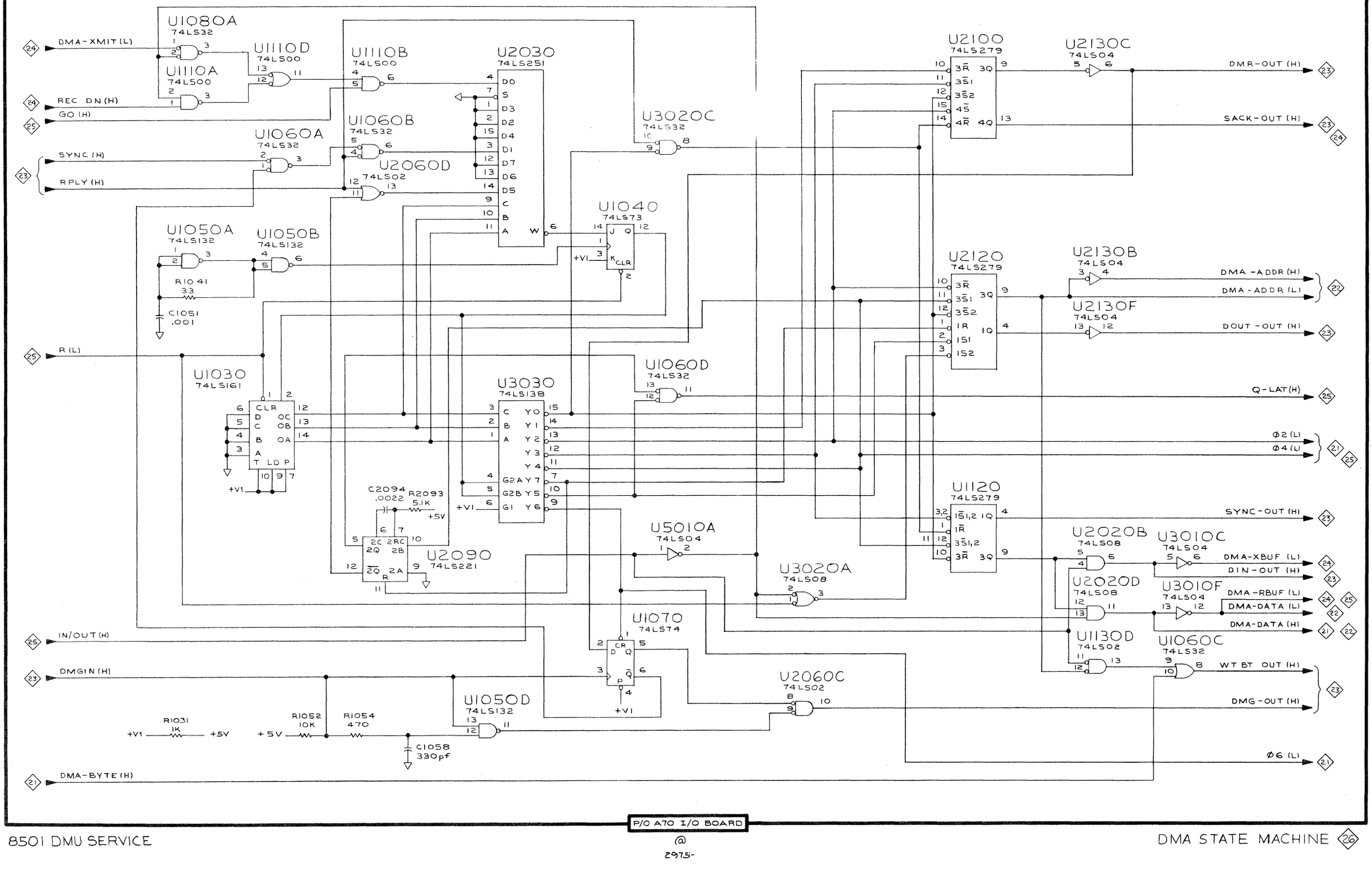
2975-

8501 DMU SERVICE

DMA REGISTERS 25



P/O A70 I/O BOARD

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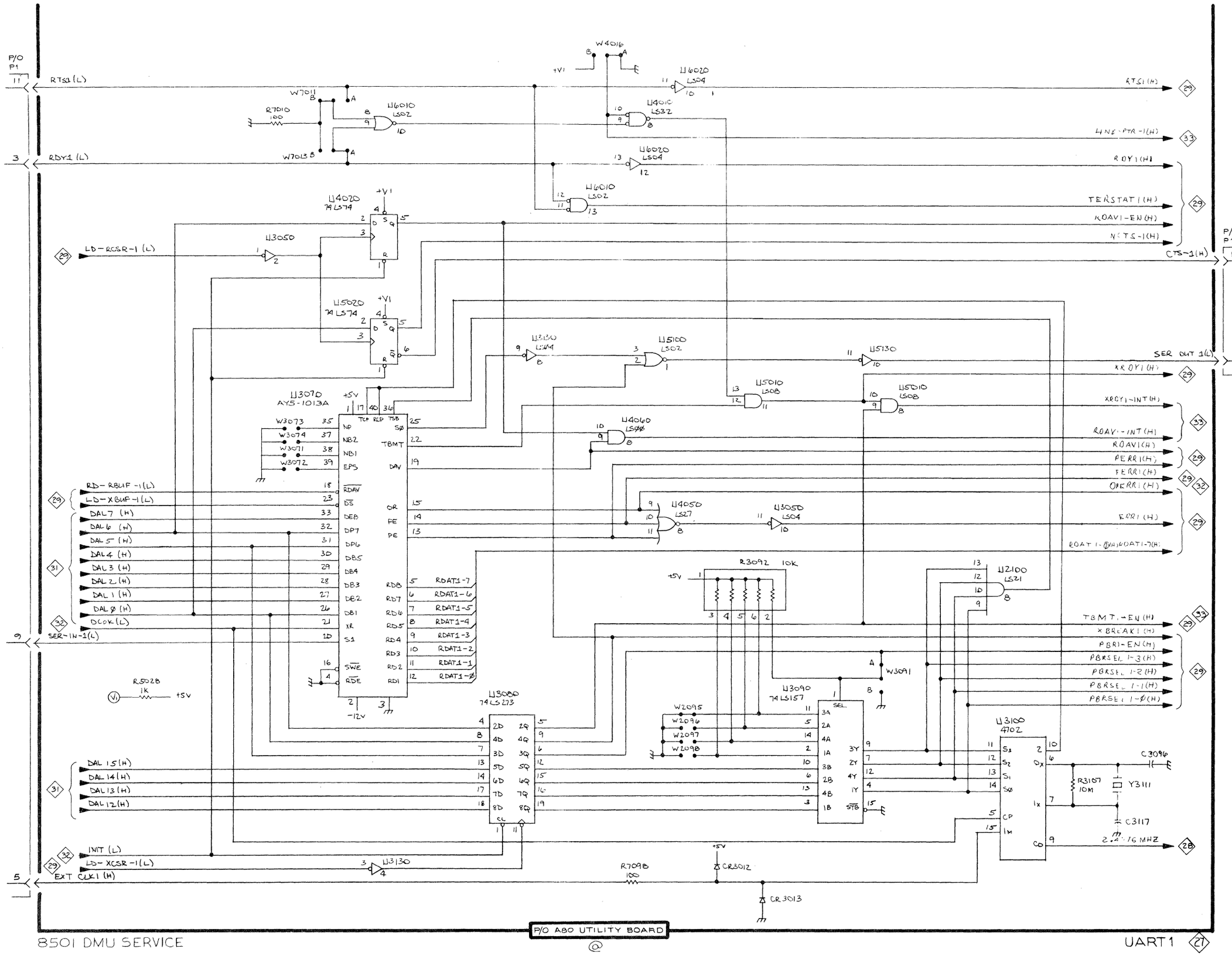
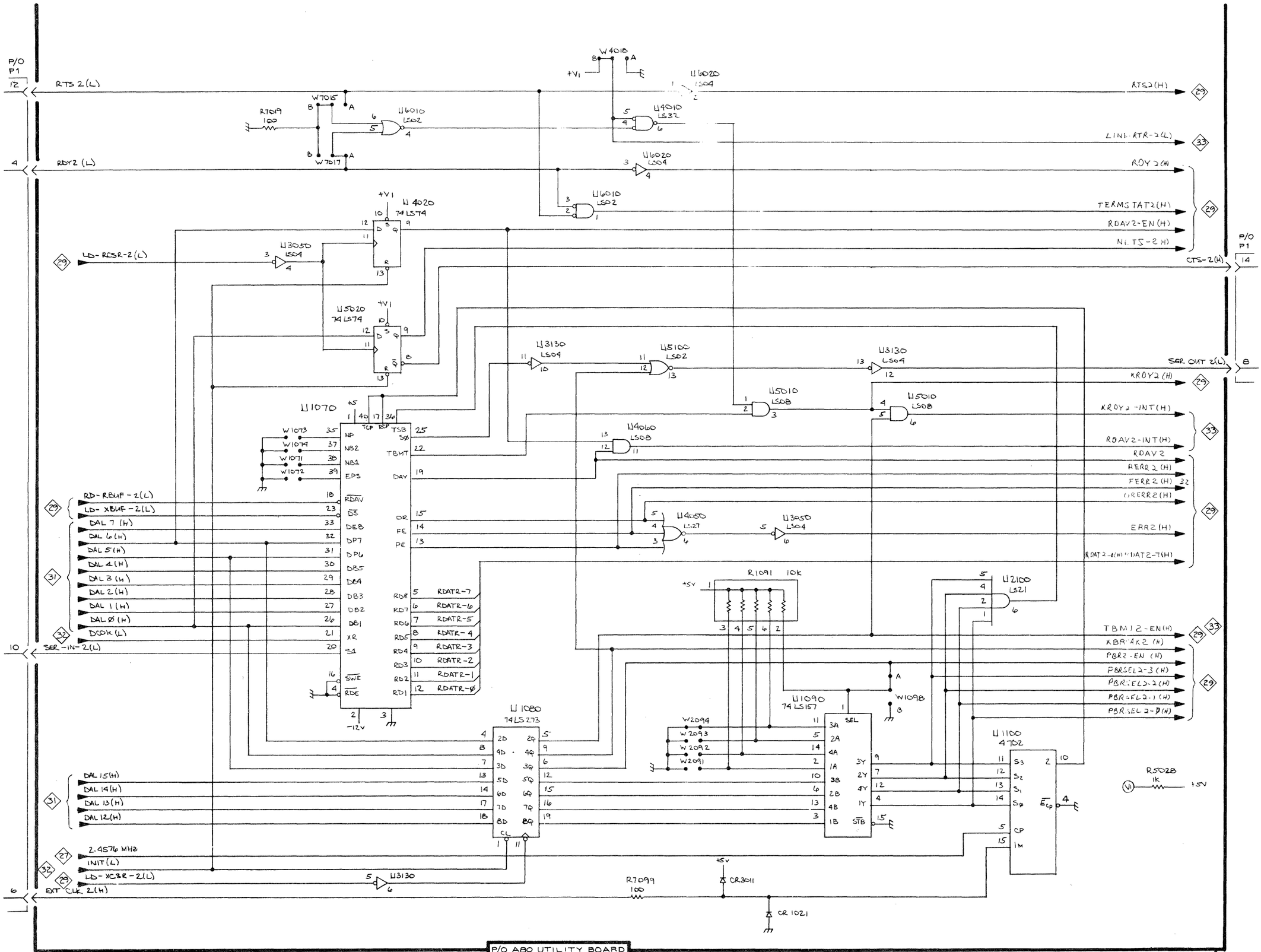
2975-

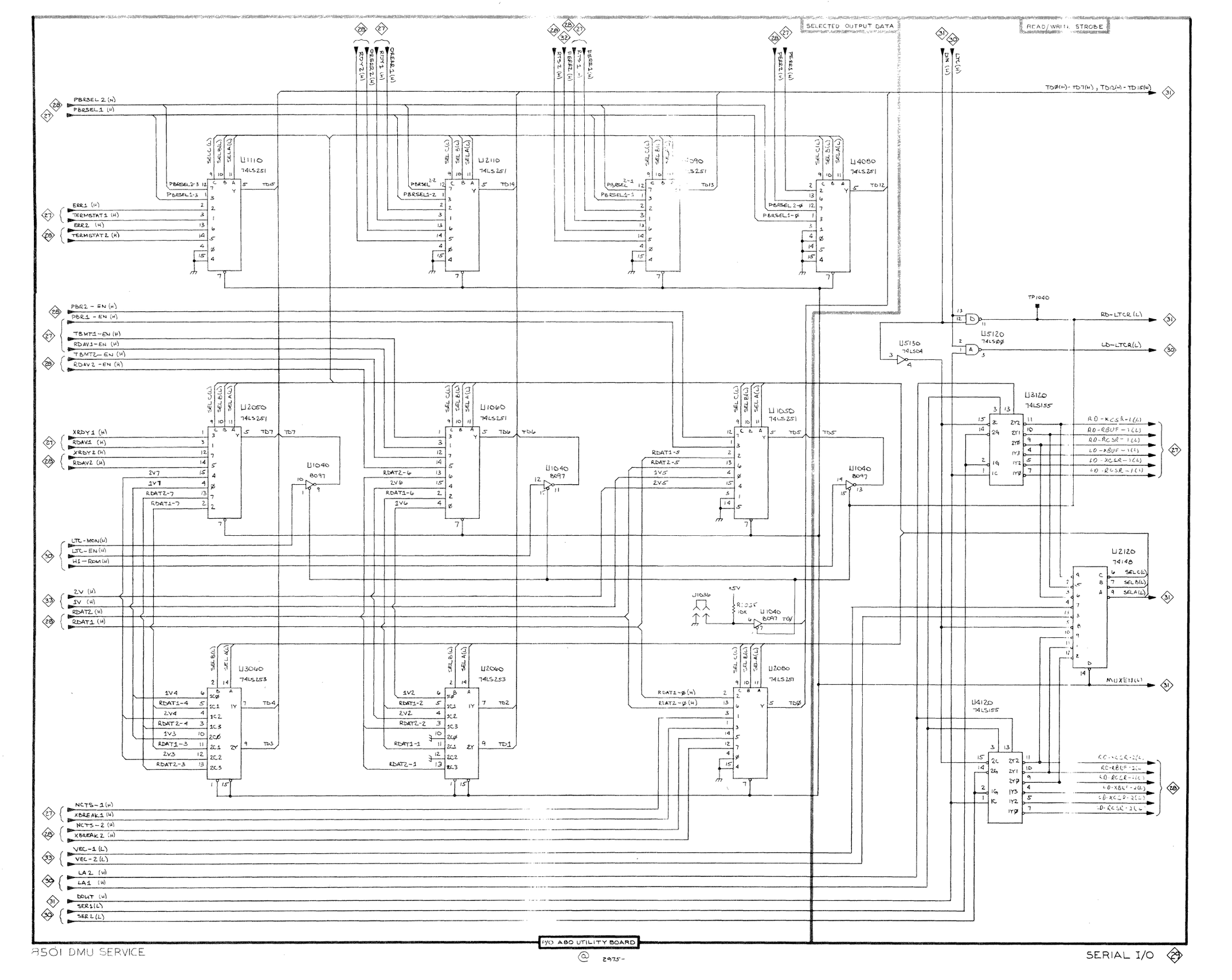
8501 DMU SERVICE

DMA STATE MACHINE 26



P/O A80 UTILITY BOARD


P/O P1 12
RTS 2 (L)
RDY2 (L)
4
W4018
+V1
U6020 LS04
RTSJ(H)
29
W7015
R7019 100
U6010 LS02
U4010 LS32
W7017
LINE RTR-2(L)
33
U6020 LS04
RDY 2(H)
U6010 LS02
TERMSTAT2(H)
RDAV2-EN(H)
NLTS-2(H)
29
P/O P1 14
CTS-2(H)
U4020 74LS74
U3050 LS04
LD-RCSR-2(L)
U5020 74LS74
U3130 LS04
U5100 LS02
U3130 LS04
SER OUT 2(L)
8
KRDY2(H)
U5010 LS08
U5010 LS08
KRDY2-INT(H)
33
U4060 LS08
RDAV2-INT(H)
RDAV2
RERR2(H)
FERR2(H)
32
OERR2(H)
29
U1070
W1073
W1074
W1071
W1072
RD-RBUF-2(L)
LD-XBUF-2(L)
DAL 7(H)
DAL 6(H)
DAL 5(H)
DAL 4(H)
DAL 3(H)
DAL 2(H)
DAL 1(H)
DAL 0(H)
DCOK(L)
31
32
SER-IN-2(L)
10
U4050 LS27
U3050 LS04
ERR2(H)
RDATR-7
RDATR-6
RDATR-5
RDATR-4
RDATR-3
RDATR-2
RDATR-1
RDATR-0
RDATR-0(H) thru RDATR-7(H)
R1091 10K
+5V
U2100 LS21
TBMT2-EN(H)
XBRK2(H)
PBR2-EN(H)
PBRSEL2-3(H)
PBRSEL2-2(H)
PBRSEL2-1(H)
PBRSEL2-0(H)
29
33
U1080 74LS273
W2094
W2093
W2092
W2091
U1090 74LS157
W1098
U1100 4702
R5028 1K
+5V
DAL 15(H)
DAL 14(H)
DAL 13(H)
DAL 12(H)
31
2.4576 MHz
INIT(L)
LD-XCSR-2(L)
EXT CLK 2(H)
27
32
29
6
U3130 LS04
R7099 100
CR3011
CR1021


SELECTED OUTPUT DATA
READ/WRITE STROBE
PBRSEL 2 (H)
PBRSEL 1 (H)
TD8(H)-TD7(H), TD12(H)-TD15(H)
U1110 74LS251
U2110 74LS251
U4080 74LS251
ERR1 (H)
TERMSTAT1 (H)
ERR2 (H)
TERMSTAT2 (H)
PBR2 - EN (H)
PBR1 - EN (H)
TBMT1-EN (H)
RDAV1-EN (H)
TBMT2-EN (H)
RDAV2 -EN (H)
U5130 74LS04
U5120 74LS08
TP1040
RD-LTCR(L)
LD-LTCR(L)
U2050 74LS251
U1060 74LS251
U1050 74LS251
U3120 74LS155
XRDY1 (H)
RDAV1 (H)
XRDY2 (H)
RDAV2 (H)
U1040 8097
RD-XCSR-1(L)
RD-RBUF-1(L)
RD-RCSR-1(L)
LD-XBUF-1(L)
LD-XCSR-1(L)
LD-RCSR-1(L)
LTC-MON(H)
LTC-EN(H)
HI-RDW(H)
U2120 74148
SELC(H)
SELB(L)
SELA(L)
MUXEN(L)
2V (H)
1V (H)
RDAT2 (H)
RDAT1 (H)
U1036
+5V
R1055 10K
U3060 74LS253
U2060 74LS253
U2080 74LS251
U4120 74LS155
NCTS-1(H)
XBREAK1 (H)
NCTS-2 (H)
XBREAK2 (H)
VEC-1 (L)
VEC-2 (L)
LA2 (H)
LA1 (H)
DOUT (H)
SER1(L)
SER2(L)

ADDR RECOG/CHANNEL "2

RECOGNIZE ADDR + LINE TIME CLK

ADDR LATCH/ROM

ROMS

SYNC(H)
BS7(H)
DAL 1(H) - DAL 12(H)
DCOK (H)
LD-LTCR (L)

R6121 1K +5

J7131 J7132 J7133 J7134 J7135 J7136

U7130 8136

J6134 J6133 J6132 J6131

U6130 8136

J7111 J7112 J7113 J7114 J7115 J7116

U7110 8136

J6114 J6113 J6112 J6111

U6110 8136

R6131 10K +5

U5130 74LS08

R5122 2.2K +5

U5110 74LS04

U7100 74LS133

U5100 74LS02

U5130 74LS04

U5070 74LS373

U5110 74LS04

SER-2(L)
SER2(L)
LTC(H)
LTC(L)

U5080 8252708

U5090 8252708

LA2(H)
LA1(H)

U4130 74LS74

U4130 74LS74

U1020 74LS174

1032 1034 1023 1022 1021 +5V

U3050 74LS04

U1030 74LS74

U4010 74LS32

U6040 74LS14

0.0054 1000pf

U1010 74LS08

U5110 74LS04

R6111 10K +5

R5121 2.2K +5

U6100 8136

R5111 10K +5

U4110 74LS08

RD-ROM(L)

W6101

R5129 100

R5028 1K +5V (V1)

R5131 1K +5V (V2)

TD0(H) - TD15(H)

LTC-MON(H)
EVNT(H)
LTC-EN(H)
SER-1(L)
SER1(L)

P/O P1 19

INIT (L)
LINE FR(H)
DIN(H)

ADDR RECOG/CHANNEL "1

P/O ABO UTILITY BOARD

LINE TIME CLK

RECOGNIZE ROM ADDR

BUS DRIVER/RECEIVERS

P/O P1 41 29 45 35 33 37 — BIAKI L (H), BSYNT L (H), BSYNC L (H), BSSYN L (H), BDIN L (H), BMTBT L (H)

P/O P1 49 47 31 43 39 — BDMGO L (H), BDMGI L (H), BAPLY L (H), BEVNT L (H), BIRQ L (H)

LTC (H) — 30

MUXEN (L)
RD-LTCR (L) — 29

U4100 74LS10 — U5130 74LS04

TDØ - TD15 (H) — 30 29

U7090 8838 — R7080 180 — +5V — R7080 390

BAD 15L (H) — 99
BAD 14L (H) — 97
BAD 13L (H) — 95
BAD 12L (H) — 93

LTC (L) — 30
SER-1 (L)
SER-2 (L)
RD-RQM (L)
SEL A (L) — 29

U4100 74LS10 — U5130 74LS10 — U4110 74LS08

U6090 8838 — R7060 180 — +5V — R7060 390

BAD 11L (H) — 91
BAD 10L (H) — 89
BAD 9L (H) — 87
BAD 8L (H) — 85

U4110 74LS08 — U6050 74LS04

U7070 8838 — R7060 180 — +5V — R7060 390

BAD 3L (H) — 75
BAD 2L (H) — 73
BAD 1L (H) — 55
BAD 4L (H) — 77

U6080 8838 — R7080 180 — +5V — R7060 180 — R7080 390 — R7060 390

BAD 7L (H) — 83
BAD 6L (H) — 81
BAD 5L (H) — 79
BAD ØL (H) — 53

R7030 390 — +5V — R7095 680 — U7050 8838 — R7030 180 — R7066 330

+5V — R7060 180 — R7080 180 — R7030 180 — R7056 330

R7060 390 — R7080 390 — R7030 390 — R7055 680

U6070 8838 — IRQ (H) — EVENT (H)

RPLY (H) — 32

U5060 7406 — +5V — 1k — DMGI (L) — 32

U5120 74LS00 — U4100 74LS10

U5120 74LS00

DIN (H) — 33 29 30
SINC (H) — 33 30 32
IAKI (H) — 33
BST (H) — 30
DOUT (H) — 29

FRONT PANEL CONTROL

U6060 MC14572 — J7061 — 6B, 8D, 5A, 7C — R6061 10K — R6060 10K — C6063 0.1

BUS TERMINATIONS

R7060 180 — +5V — R7030 180 — R7030 390 — R7060 390

P/O P1

BIRQ 5L (H) — 22
BIRQ 6L (H) — 24
BDAL 17L (H) — 28
BDAL 16L (H) — 26
BREF L (H) — 48
BIRQ 7L (H) — 90
BSACK L (H) — 88
PON (H) — 61
PWR (L) — 64
REM-PWR (L) — 2
+15V — 63

DAL Ø (H) - DAL 7 (H) — 27 28 30
DAL 12 (H) - DAL 15 (H) — 28 31

P/O A80 UTILITY BOARD

POWER UP/DOWN

P/O P1 20 — ACDK (H)

U6040 LS14 — U5040 7406 — +5V R5049 10K — R6041 470 — C6047

TP6021 — R6081 390 — R5029 1K — R6036 34.8K — R6035 43.2K — VR6032 — U5030 LM339

TP6033 — R6034 34.5K — R6033 93.1K — C7039 — U5030 LM339

TP6039 — R6037 34.8K — R6038 45.3K — CR6039 — C7037 — -12V

+12V — C7038 — C7079 — -12V

69, 36, 42, 25, 52, 80, 86, 96

21, 65 — +5V — SEE CAP TABLE

27, 71 — +12V

23, 67 — -12V

U6040 LS14 — U5040 7406 — R5048 10K — R6042 470 — C6043

U6040 LS14 — R6044 470 — +5V C6046 — U6048 LS14 — U4030 LS08

TDCOK (L)

TPOK (L)

HALT (H)

P/O P1 51 — BINIT (L)

P/O P1 66 — BPOK H (H)

P/O P1 40 — BDCOK H (H)

BHALT L (L)

R7060 180 — +5V — R7060 390

U7050 8838 — +5V R7054 10K — U7079

U6020 LS04 — INIT (L) → 27, 28, 30

U6020 LS08 — DCOK (H) → 30

DCOK (L) → 27, 28

P/O P1

+5V R4038 620 — CR4037 — R5031 10K — C5041

+5V R5038 27K — R4039 100K — R5040 10K — U5030 LM339

U4030 LS08 — U4030 LS08

HALT & RESTART

16 — RESTART (L)

U6050 LS14 — W4045 — W4043 — W4041 — R4041 100K

57 — HSFE (L)

27 — FERR 1 (H)

28 — FERR 2 (H)

+5V R4032 10K — W4031 — U4030 LS08

+5V R4059 27K — C4058 — CR5051 — U5050 9602

+5V R6052 10K

U4040 LS27 — +5V R4021 10K

31 — DMGT (L) / SYNC (H) / RPLY (H) — U4040 LS27

+5V R5057 15K — C4057 470 — U5050 9602

+V1

+5V R4068 10K — C4069 0.1 μf — U3040 LS20

+5V R5062 3.3K — W5061

V1 — R5028 1K — +5V

R7020 8838 — +5V R7023 330 — R7024 680 — BDHR L (L) → 44

58 — RUN (L) / HALT (H)

32 — BRUN L (H)

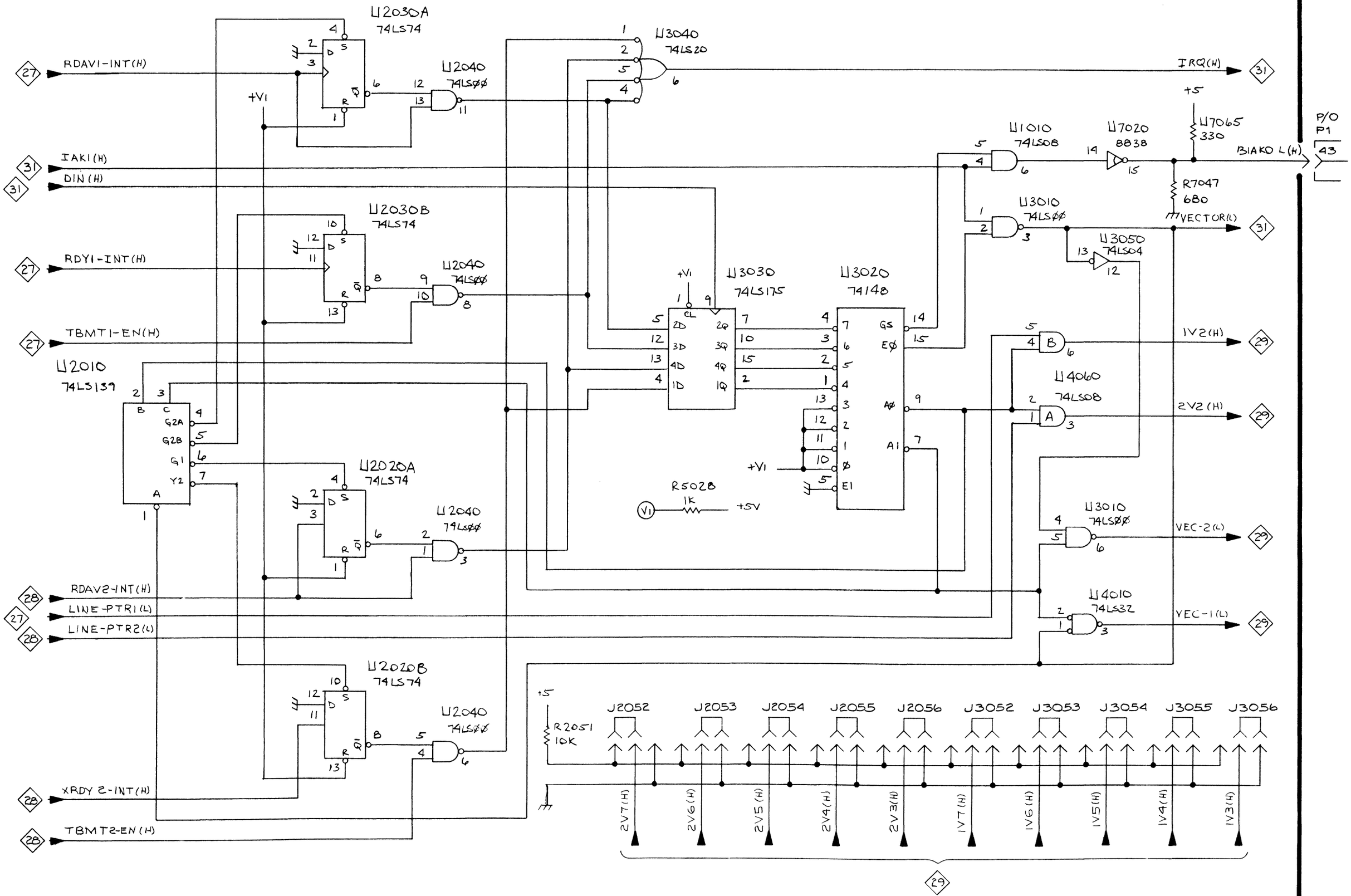
+5 R7030 180 — R7030 390

+5 R5064 20K — C6053 1000Pf — U5060 9602

U6040 LS14 — +V1

U7020 8838 — U7020 8838 — PROC BUSY (L) → 62

P/O A80 UTILITY BOARD



P/O A80 UTILITY BOARD

8501 DMU SERVICE

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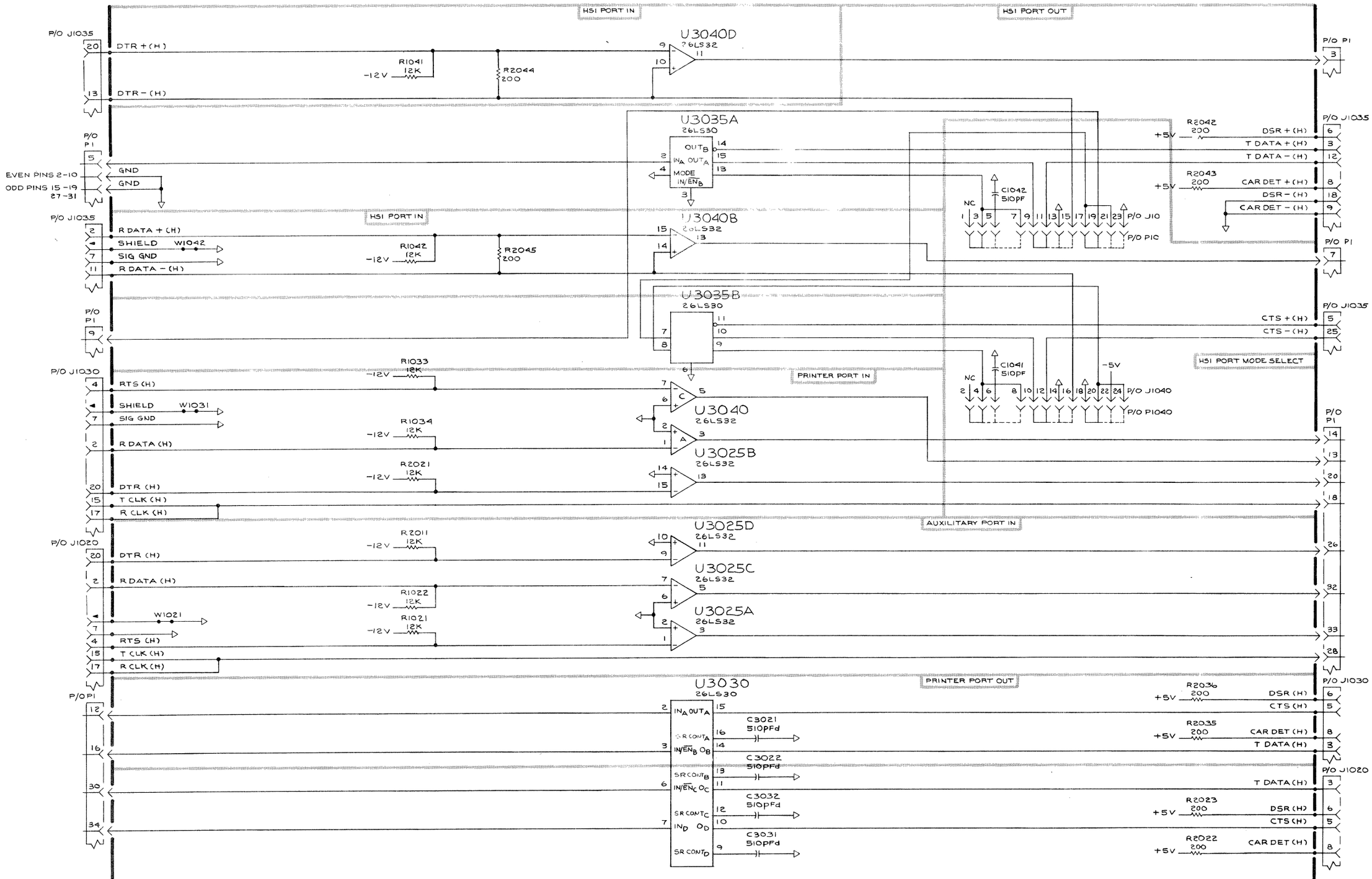
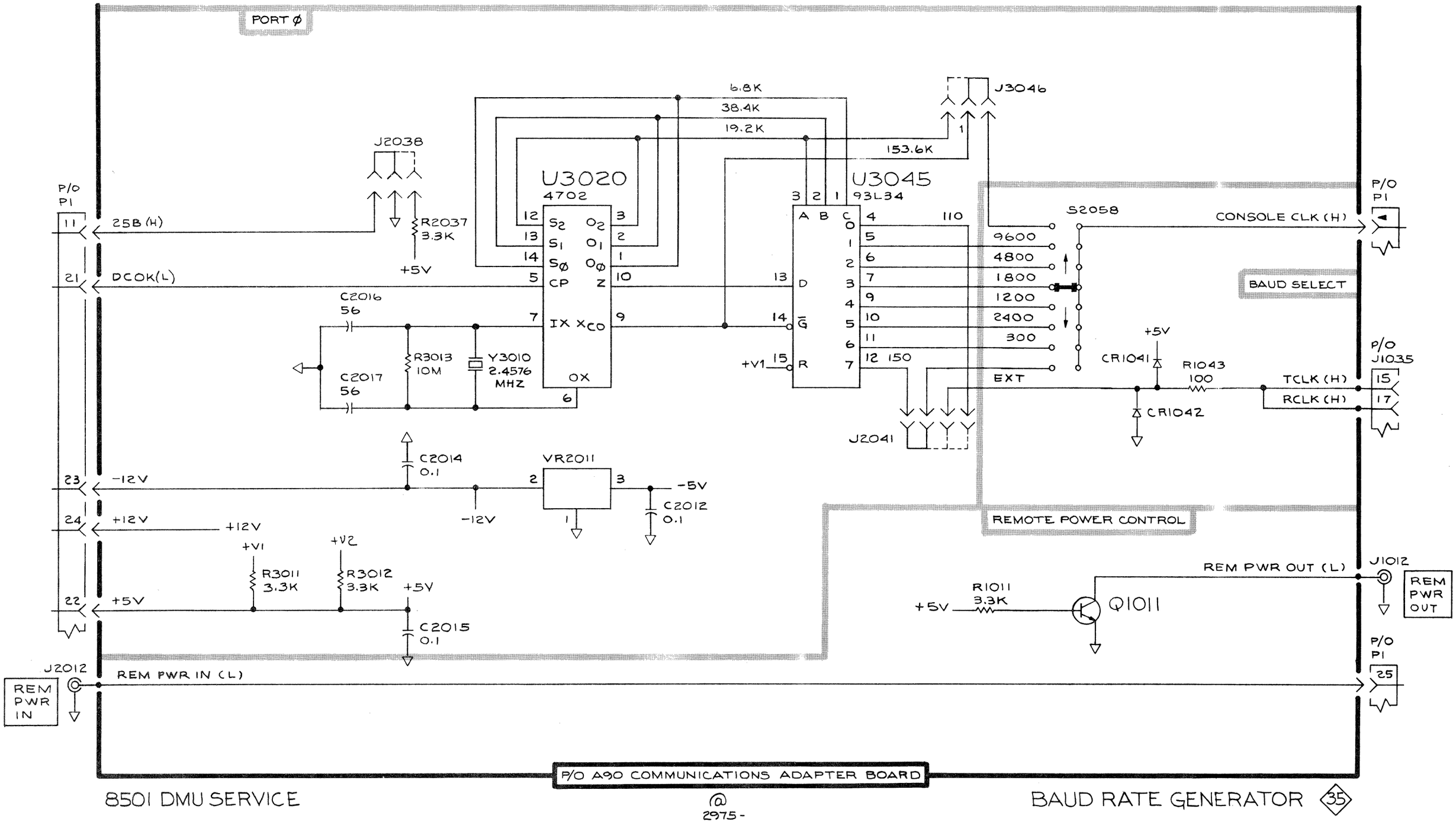
INTERRUPT CONTROL

33


HSI PORT IN
HSI PORT OUT
P/O J1035
DTR + (H)
DTR - (H)
R1041 12K -12V
R2044 200
U3040D 26LS32
P/O P1
3
P/O P1
5
EVEN PINS 2-10
ODD PINS 15-19 27-31
GND
GND
U3035A 26LS30
OUTB OUTA MODE IN/ENB
R2042 200 +5V
DSR + (H)
T DATA + (H)
T DATA - (H)
R2043 200 +5V
CAR DET + (H)
DSR - (H)
CAR DET - (H)
C1042 510PF
NC
P/O J10
P/O P1C
P/O J1035
R DATA + (H)
SHIELD W1042
SIG GND
R DATA - (H)
R1042 12K -12V
R2045 200
U3040B 26LS32
P/O P1
7
P/O J1035
9
U3035B 26LS30
CTS + (H)
CTS - (H)
C1041 510PF
NC
-5V
P/O J1040
P/O P1040
HSI PORT MODE SELECT
PRINTER PORT IN
P/O J1030
RTS (H)
SHIELD W1031
SIG GND
R DATA (H)
DTR (H)
T CLK (H)
R CLK (H)
R1033 12K -12V
R1034 12K -12V
R2021 12K -12V
U3040 26LS32
U3025B 26LS32
P/O P1
14
13
20
18
P/O J1020
DTR (H)
R DATA (H)
W1021
RTS (H)
T CLK (H)
R CLK (H)
R2011 12K -12V
R1022 12K -12V
R1021 12K -12V
U3025D 26LS32
U3025C 26LS32
U3025A 26LS32
AUXILITARY PORT IN
26
32
33
28
P/O P1
PRINTER PORT OUT
U3030 26LS30
INA OUTA
SRCONTA
IN/ENB OB
SRCONTB
IN/ENC OC
SRCONTC
IND OD
SRCONTD
C3021 510PFd
C3022 510PFd
C3032 510PFd
C3031 510PFd
P/O J1030
R2036 200 +5V
DSR (H)
CTS (H)
R2035 200 +5V
CAR DET (H)
T DATA (H)
P/O J1020
T DATA (H)
R2023 200 +5V
DSR (H)
CTS (H)
R2022 200 +5V
CAR DET (H)
P/O A90 COMMUNICATIONS ADAPTER BOARD
AUXILIARY PORT OUT



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BAUD RATE GENERATOR 35

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
000BH	FAB-TEK	17 SUGAR HALLOW ROAD	DANBURY, CT 06810
000HJ	RATEL ELECTRONICS	948 BENICIA AVE.	SUNNYVALE, CA 94086
000HL	STURGES MFG INC.	P.O. DEAWER 59	UTICA, N.Y. 13503
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01881	ANACONDA AMERICAN BRASS COMPANY, A DIV. OF ANACONDA COMPANY	414 MEADOW STREET	WATERBURY, CT 06720
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
05820	WAKEFIELD ENGINEERING, INC.	AUDUBON ROAD	WAKEFIELD, MA 01880
06383	PANDUIT CORPORATION	17301 RIDGELAND	TINLEY PARK, IL 60477
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
13103	THERMALLOY COMPANY, INC.	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS, TX 75234
15476	DIGITAL EQUIPMENT CORP.	146 MAIN ST.	MAYNARD, MA 01754
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
53387	MINNESOTA MINING AND MFG. CO., ELECTRO PRODUCTS DIVISION	3M CENTER	ST. PAUL, MN 55101
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
70485	ATLANTIC INDIA RUBBER WORKS, INC.	571 W. POLK ST.	CHICAGO, IL 60607
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
75037	MINNESOTA MINING & MFG CO. ELECTRO PRODUCTS DIV.	3M CENTER	ST. PAUL, MN 55101
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
76381	MINNESOTA MINING AND MFG. CO.	3M CENTER	ST. PAUL, MN 55101
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
91506	AUGAT, INC.	33 PERRY AVE.	ATTLEBORO, MA 02703
93907	CAMCAR SCREW AND MFG. CO.	600 18TH AVE.	ROCKFORD, IL 61101
95238	CONTINENTAL CONNECTOR CORP.	34-63 56TH ST.	WOODSIDE, NY 11377
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	333-2575-00			1		PANEL,FRONT:CONTROL	80009	333-2575-00
-2	----- -----			1		SWITCH,ROCKER:(SEE S1045 REPL)		
-3	352-0157-00			3		LAMPHOLDER:WHITE PLASTIC	80009	352-0157-00
-4	378-0602-00			1		LENS,LIGHT:GREEN	80009	378-0602-00
	378-0602-01			2		LENS,LIGHT:AMBER	80009	378-0602-01
-5	----- -----			3		LT EMITTIN DIO:(SEE DS1032,DS1038,DS1052 REPL)		
-6	200-0935-00			3		BASE,LAMPHOLDER:0.29 OD X 0.19 CASE	80009	200-0935-00
-7	214-2964-00			2		SPRING,PANEL:COPPER-BERYLLIUM	80009	214-2964-00
						(ATTACHING PARTS)		
-8	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
-9	343-0831-00			2		RETAINER,SPR:ALUMINUM	80009	343-0831-00
						- - - * - - -		
-10	----- -----			2		SWITCH,TOGGLE:(SEE S1014 AND S1024 REPL)		
-11	----- -----			1		CKT BOARD ASSY:FRONT PANEL(SEE A30 REPL)		
						(ATTACHING PARTS)		
-12	211-0116-00			2		SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-13	131-0608-00			8		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-14	386-4226-00			1		SUBPANEL,FRONT:CONTROL	80009	386-4226-00
-15	129-0851-00			3		SPACER,POST:0.709 L W/6-32 INT THD	80009	129-0851-00
-16	210-0006-00			3		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-17	210-0802-00			3		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
-18	378-0149-00			2		GRILL,PLASTIC:5.62 L X 3.12 W	80009	378-0149-00
-19	101-0065-00			1		TRIM,DECORATIVE:FACADE	80009	101-0065-00
						(ATTACHING PARTS)		
-20	211-0507-00			3		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-21	211-0511-00			4		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-22	220-0884-00			4		NUT BAR:0.312 SQ X 3.234 L	80009	220-0884-00
						(ATTACHING PARTS)		
-23	211-0512-00			8		SCREW,MACHINE:6-32 X 0.50" 100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-24	426-1624-02			1		FRAME,CABINET:OPEN FRONT,10.5 X FULL RACK	80009	426-1624-02
-25	386-4227-00			1		SUBPANEL,FRONT:	80009	386-4227-00
-26	390-0749-02			1		CABINET BOTTOM:TEK TAN	80009	390-0749-02
	390-0752-02			1		CABINET TOP:TEK TAN	80009	390-0752-02
-27	390-0750-02			2		CABINET SIDE:TEK TAN	80009	390-0750-02
-28	124-0367-02			1		STRIP,TRIM:CORNER,TOP,PVC,TEK TAN	80009	124-0367-02
-29	426-1649-00			1		FR SECT,DEV UN:UPPER LEFT/LOWER RIGHT RAIL	80009	426-1649-00
						(ATTACHING PARTS)		
-30	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-31	213-0863-00			2		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-32	348-0617-02			2		FOOT,CABINET:BOT,TEK TAN	80009	348-0617-02
-33	124-0366-02			1		STRIP,TRIM:CORNER,BOTTOM,PVC,TEK TAN	80009	124-0366-02
-34	426-1651-00			1		FR SECT,CORNER:UPPER RIGHT/LOWER LEFT RAIL	80009	426-1651-00
						(ATTACHING PARTS)		
-35	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	213-0863-00			2		SCREW,TPG,TF:8-32 X 1.375 TAPTITE	80009	213-0863-00
						- - - * - - -		
-36	441-1495-00			1		CHAS,FLEX DRUN:ALUMINUM	80009	441-1495-00
						(ATTACHING PARTS)		
-37	212-0023-00			6		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-38	211-0559-00			4		SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-39	426-1652-00			1		FR SECT,DEV UN:SIDE RAIL	80009	426-1652-00
						(ATTACHING PARTS)		
-40	213-0863-00			2		CREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		

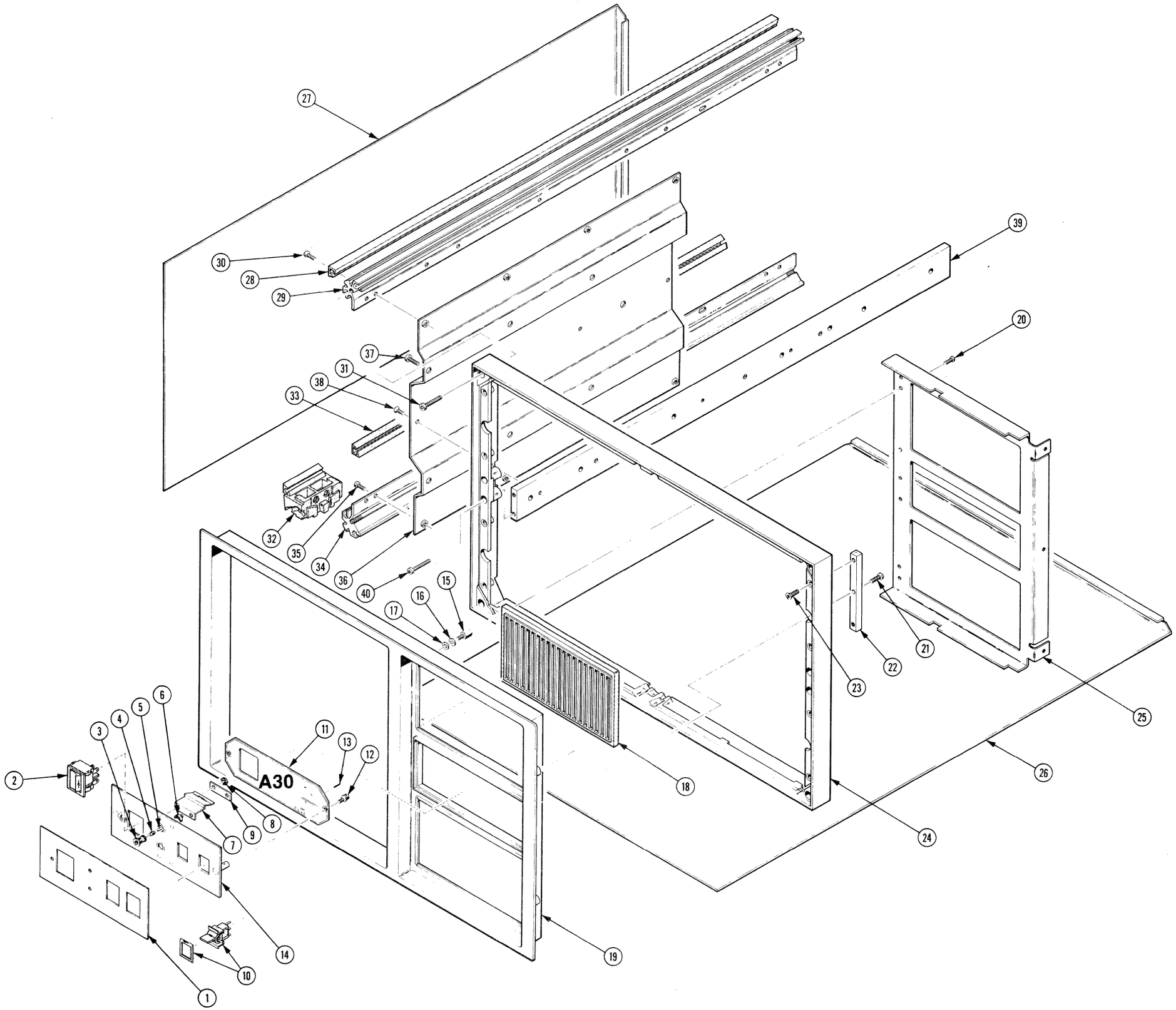


FIG. 1 FRONT

8501

FIG. 2 CARD CARRIAGE & CIRCUIT BOARDS

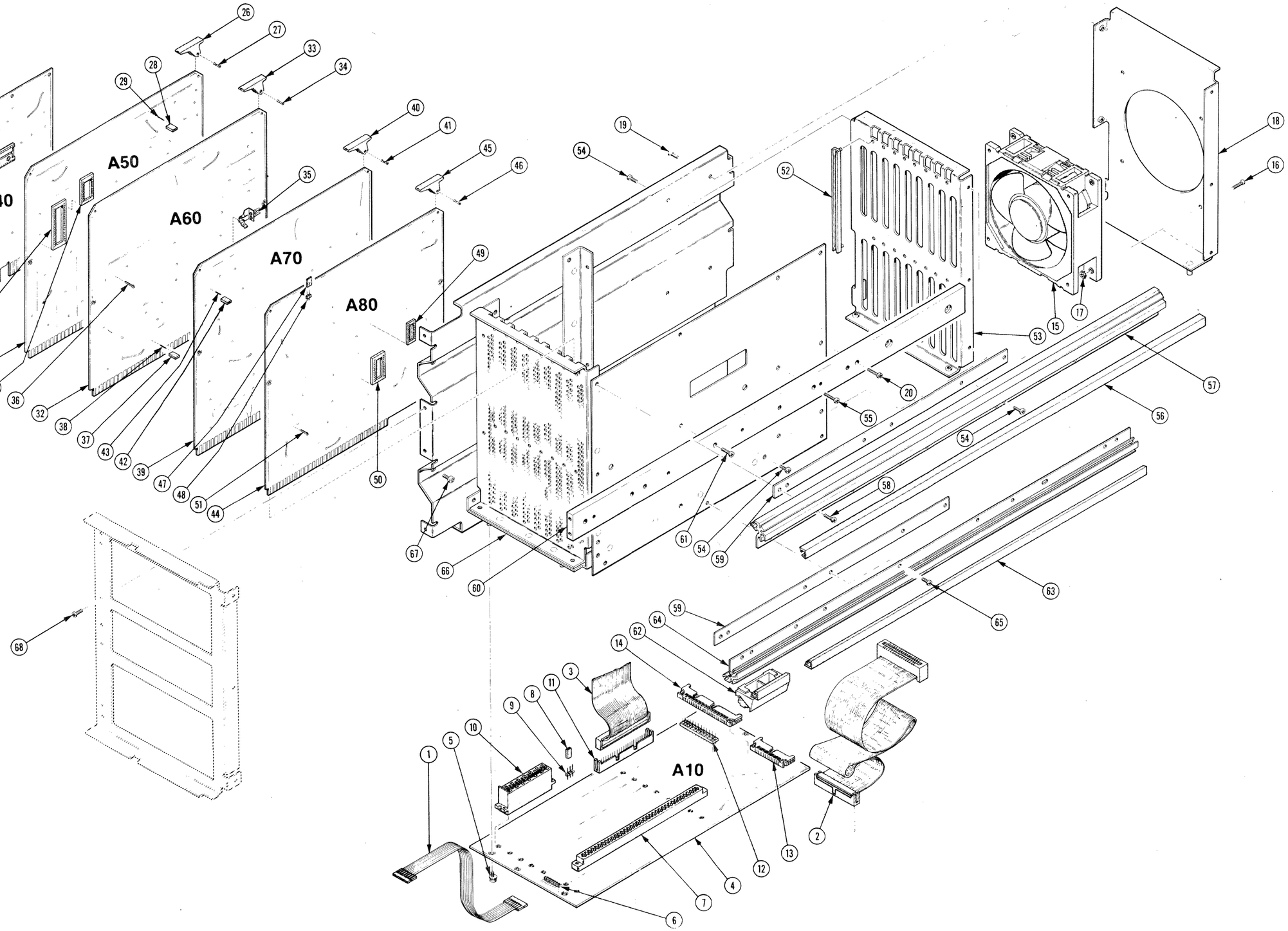
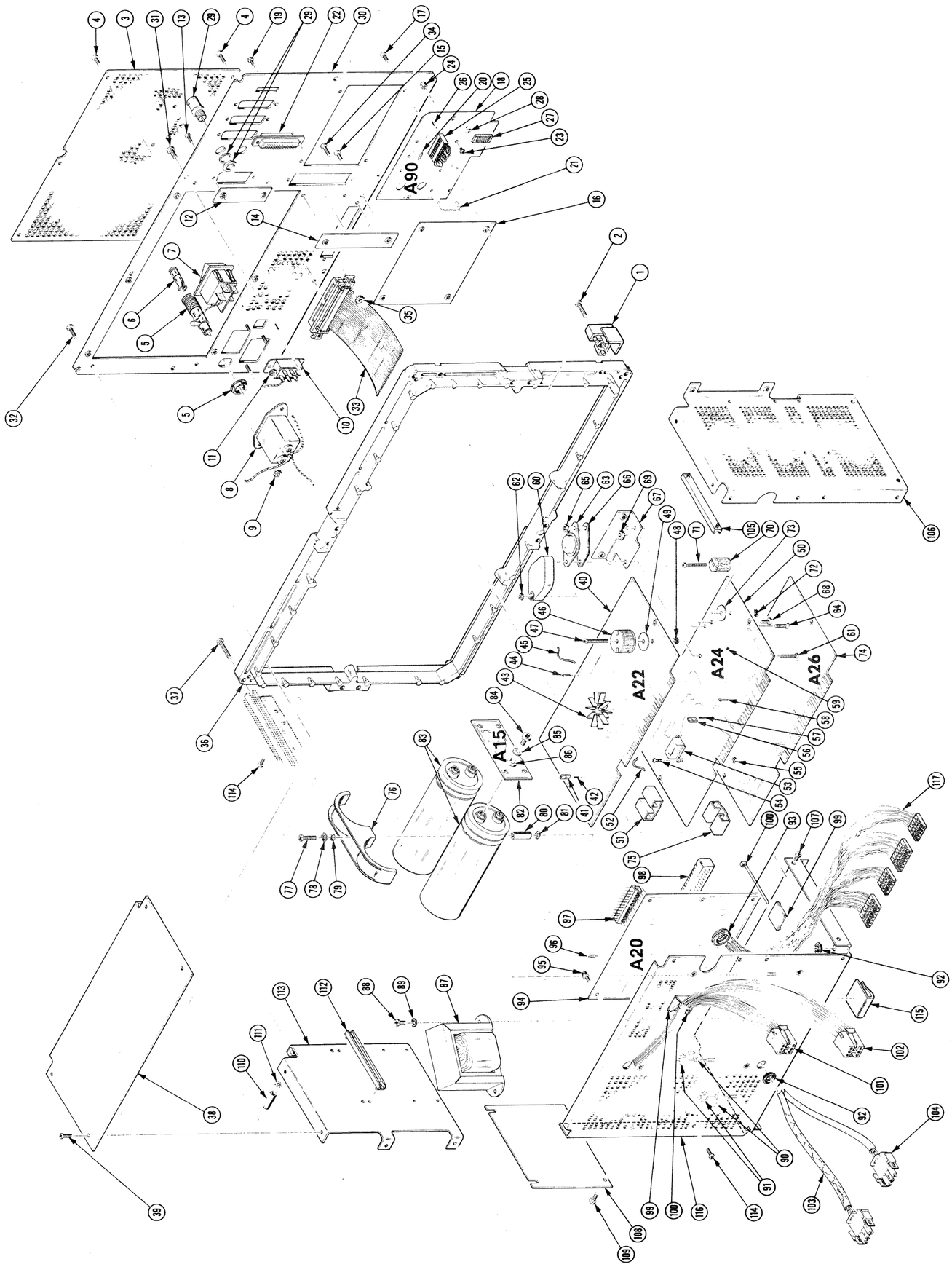


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	175-2588-00			1		CA ASSY,SP,ELEC;8,22 AWG,9.0 L	80009	175-2588-00
-2	175-2813-00			1		CA ASSY,SP,ELEC;34,28 AWG,13.875 L	000HJ	OBD
-3	----- -----			1		CABLE ASSY:(SEE FIGURE 3 INDEX 33)		
-4	----- -----			1		CKT BOARD ASSY:BACKPLANE(SEE A10 REPL)		
						(ATTACHING PARTS)		
-5	211-0601-00			5		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-6	131-1425-00			1		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-7	131-2240-00			8		. CONN,RCPT,ELEC:CKT BD,50/100CONT	05574	000201-5444
-8	131-0993-09			14		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-9	131-1343-00			1		. TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
-10	131-1973-00			2		. CONN,RCPT,ELEC:CKT BD,36 CONT W/O MTG TABS	15476	H807
-11	131-2409-00			1		. CONN,RCPT,ELEC:CKT BD,2 X 25,MALE	75037	3496-2003
-12	131-1939-00			1		. TERM. SET,PIN:1 X 14,0.15 SPACING	22526	65561-114
-13	131-2407-00			1		. CONN,RCPT,ELEC:CKT BD,2 X 13,MALE	75037	3493-1003
-14	131-2406-00			1		. CONN,RCPT,ELEC:CKT BD,2 X 17,MALE	75037	3494-2003
-15	----- -----			1		FAN VENTILATING:(SEE B610 REPL)		
						(ATTACHING PARTS)		
-16	211-0511-00			4		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-17	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-18	407-2364-00			1		BRACKET,PAN:ALUMINUM	80009	407-2364-00
						(ATTACHING PARTS)		
-19	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-20	211-0511-00			1		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-21	----- -----			1		CKT BOARD ASSY:LSI/11(SEE A40 REPL)		
-22	367-0183-00			2		. PULL,CKT CARD:	15476	23930-00
-23	131-0623-00			5		. CONN,RCPT,ELEC:EDGECARD,50/100 CONT,0.1 SP	05574	600201-3221
-24	131-0608-00			8		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-25	----- -----			1		CKT BOARD ASSY:FLEX CONTROLLER(SEE A50 REPL)		
-26	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-27	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-28	131-0993-09			14		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-29	131-0608-00			106		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-30	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-31	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
	253-0176-00			1		. TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	OBD
-32	----- -----			1		CKT BOARD ASSY:32K MEMORY(SEE A60 REPL)		
-33	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-34	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-35	136-0208-00			1		. SOCKET,PLUG-IN:CRYSTAL AUGAT	91506	8004-1G5
-36	----- -----			6		. TERM,TEST POINT:(SEE A60TP2129,TP2149,TP3011,		
	----- -----			-		. TP3026,TP4138 AND TP5133 REPL)		
-37	131-0993-09			5		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-38	131-0608-00			20		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-39	----- -----			1		CKT BOARD ASSY:I/O(SEE A70 REPL)		
-40	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-41	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-42	131-0993-09			16		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-43	131-0608-00			47		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-44	----- -----			1		CKT BOARD ASSY:UTILITY(SEE A80 REPL)		
-45	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-46	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-47	131-0993-09			33		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-48	131-0608-00			102		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-49	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-50	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-51	214-0579-02			4		. TERM,TEST POINT:BRASS	80009	214-0579-02
	253-0176-00			1		. TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	OBD
-52	351-0087-00			18		GUIDE,CKT CARD:4.75 INCH LONG,PLASTIC	80009	351-0087-00
-53	441-1496-00			1		CHAS,CKT BD CG:REAR,ALUMINUM	80009	441-1496-00
						(ATTACHING PARTS)		
-54	211-0507-00			8		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-55	211-0513-00			1		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-56	124-0367-02			1		STRIP,TRIM:CORNER,TOP,PVC,TEK TAN	80009	124-0367-02
-57	426-1651-00			1		FR SECT,DEV UN:UPPER FIGHT/LOWER LEFT RAIL	80009	426-1651-00
						(ATTACHING PARTS)		
-58	211-0507-00			3		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	211-0511-00			1		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
	213-0863-00			2		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
	211-0511-00			1		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-59	361-0982-00			2		SPACER,PLATE:0.062 THK X 12.087 L X 0.6W	80009	361-0982-00
-60	426-1652-00			1		FR SECT,DEV UN:SIDE RAIL	80009	426-1652-00
						(ATTACHING PARTS)		
-61	211-0511-00			3		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-62	348-0617-02			2		FOOT,CABINET:BOT,TEK TAN	80009	348-0617-02
-63	124-0366-02			1		STRIP,TRIM:CORNER,BOTTOM,PVC,TEK TAN	80009	124-0366-02
-64	426-1649-00			1		FR SECT,CORNER:UPPER LEFT/LOWER RIGHT	80009	426-1649-00
						(ATTACHING PARTS)		
-65	211-0510-00			4		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
	213-0863-00			2		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-66	386-4234-00			1		CAGE,CKT BD:	80009	386-4234-00
						(ATTACHING PARTS)		
-67	212-0023-00			6		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
-68	211-0507-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		

FIG. 3 REAR



8501

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	348-0544-03			4		RTNR,CAB COVER:CORNER,TEK TAN	80009	348-0544-03
						(ATTACHING PARTS)		
-2	213-0782-00			4		SCREW,TPG,TF:8-32 X 0.625 FILH,STEEL CD PL	93907	OBD
						- - - * - - -		
-3	386-4228-00			1		PANEL,ACCESS:POWER SUPPLY	80009	386-4228-00
						(ATTACHING PARTS)		
-4	211-0507-00			6		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-5	204-0832-00			1		BODY,FUSEHOLDER:3AG,5 X 20MM FUSES	S3629	031.1673(MDLFEU)
-6	200-2264-00			1		CAP.,FUSEHOLDER:3AG FUSES	S3629	031.1666(MDLFEU)
	195-0445-00			1		LEAD,ELECTRICAL:18 AWG,3.5 L	80009	195-0445-00
	195-0447-00			2		LEAD,ELECTRICAL:18 AWG,3.0 L	80009	195-0447-00
	195-0448-00			1		LEAD,ELECTRICAL:18 AWG,3.5 L	80009	195-0448-00
-7	----- -----			1		SWITCH,ROCKER:(SEE S650 REPL)		
-8	----- -----			1		FILTER,RFI:(SEE FL652 REPL)		
						(ATTACHING PARTS)		
-9	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
						- - - * - - -		
-10	----- -----			1		SWITCH,SLIDE:(SEE S615 REPL)		
						(ATTACHING PARTS)		
-11	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
						- - - * - - -		
-12	386-4215-00	B010100	B010149X	1		PLATE,CONN MTG:GPIB BLANK,AL	80009	386-4215-00
						(ATTACHING PARTS)		
-13	211-0097-00	B010100	B010149X	2		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-14	386-4217-00	B010100	B010149X	1		PLATE,CONN MTG:HARD DISC,BLANK,AL	80009	386-4217-00
						(ATTACHING PARTS)		
-15	211-0507-00	B010100	B010149X	2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-16	386-4219-00	B010100	B010149X	1		PLATE,CONN,MTG:I/O,7 CONN,BLANK,AL	80009	386-4219-00
						(ATTACHING PARTS)		
-17	211-0507-00	B010100	B010149X	4		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-18	----- -----			1		CKT BOARD ASSY:COMM ADAPTER(SEE A90 REPL)		
						(ATTACHING PARTS)		
-19	214-3106-00			6		HARDWARE KTI:JACK SOCKET	53387	3341-15
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-20	----- -----			1		. BUS CONDUCTOR:(SEE A90R1031 REPL)		
-21	346-0032-00			1		. STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2859-75-4
-22	131-1437-00			3		. CONN,RCPT,ELEC:25 FEMALE CONTACT	71468	DB25S-F179
						(ATTACHING PARTS)		
-23	211-0105-00			6		. SCREW,MACHINE:4-40 X 0.188"100 DEG,FLH STL	83385	OBD
-24	129-0105-00			6		. POST,ELEC-MECH:0.218 OD X 0.219 INCH LONG	80009	129-0105-00
						- - - * - - -		
-25	175-2748-00			1		. LEAD ASSY,ELEC:6,26 AWG,1.5 L	80009	175-2748-00
	131-0993-09			3		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-26	131-0608-00			34		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	136-0260-02			4		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-28	220-0828-00			2		. PUSH ON NUT:0.073 ID X 0.25 OD,PLASTIC	80009	220-0828-00
	253-0176-00			1		. TAPE,PRESS SENS:VINYL FOAM,0.5 X 0.062	85471	OBD
-29	----- -----			2		CONN,RCPT,ELEC:(SEE J1012 AND J2012 REPL)		
-30	333-2578-00			1		PANEL,REAR:	80009	333-2578-00
						(ATTACHING PARTS)		
-31	213-0801-00			10		SCREW,TPG,TF:8-32 X 0.312,TAPTITE,PNH	93907	OBD
-32	211-0507-00			8		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-33	175-2634-00			1		CA ASSY,SP,ELEC:50,28 AWG,38.0 L	000HJ	OBD
						(ATTACHING PARTS)		
-34	211-0511-00			2		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-35	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-36	426-1595-01			1		FRAME,CABINET:REAR,10.5 X FULL RACK	80009	426-1595-01
						(ATTACHING PARTS)		
-37	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-38	337-2702-00			1		SHIELD,ELEC:POWER SUPPLY	80009	337-2702-00
						(ATTACHING PARTS)		
-39	211-0097-00			4		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-40	----- -----			1		CKT BOARD ASSY:PS REGULATOR(SEE A22 REPL)		
-41	131-0993-09			1		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-42	131-0608-00			2		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-43	214-1254-00			1		. HEAT SINK,ELEC:0.422 H X 1.240 INCH OD	05820	209-AB
-44	214-0579-02			12		. TERM,TEST POINT:BRASS	80009	214-0579-02
-45	346-0042-00			1		. STRAP,ASSY:0.625 X 58.0 GRAY WEBBING	000HL	11097
-46	----- -----			1		. COIL,RF:(SEE A11L1011 REPL)		
						(ATTACHING PARTS)		
-47	211-0019-00			1		. SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	OBD
-48	210-0586-00			1		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
-49	210-0917-00			1		. WASHER,NONMETAL:0.191 ID X 0.625 INCH OD	86445	OBD
						- - - * - - -		
-50	----- -----			1		CKT BOARD ASSY:PS SECONDARY(SEE A24 REPL)		
-51	214-2518-00			2		. HEAT SINK,XSTR:TO-220 OR TO-202	000BH	106B-B-HT
-52	346-0032-00			2		. STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2859-75-4
-53	----- -----			1		. RES.,FXD,WW:(SEE A24R2072 REPL)		
						(ATTACHING PARTS)		
-54	211-0001-00			2		. SCREW,MACHINE:2-56 X 0.25 INCH,PNH STL	83385	OBD
-55	210-0405-00			2		. NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	2X12157-402
						- - - * - - -		
-56	131-0993-09			4		. LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-57	131-0608-00			11		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-58	214-0579-02			4		. TERM,TEST POINT:BRASS	80009	214-0579-02
-59	136-0252-07			3		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-60	200-0692-00			1		. COV,TRANSISTOR:BLACK PLASTIC	80009	200-0692-00
						(ATTACHING PARTS)		
-61	211-0016-00			1		. SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	OBD
-62	210-0586-00			1		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
						- - - * - - -		
-63	----- -----			1		. SEMICOND DEVICE:(SEE A24CR3032 REPL)		
						(ATTACHING PARTS)		
-64	211-0014-00			1		. SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
-65	210-0586-00			1		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
						- - - * - - -		
-66	342-0523-00			1		. INSULATOR,PLATE:TRANSISTOR	13103	4103
-67	214-2951-00			1		. HEAT SINK,DIODE:	80009	214-2951-00
						(ATTACHING PARTS)		
-68	212-0004-00			1		. SCREW,MACHINE:8-32 X 0.312 INCH,PNH STL	83385	OBD
-69	210-0458-00			1		. NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	78189	511-081800-00
						- - - * - - -		
-70	----- -----			1		. COIL,RF:(SEE A24L3013 REPL)		
						(ATTACHING PARTS)		
-71	211-0019-00			1		. SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	OBD
-72	210-0586-00			1		. NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
-73	210-0917-00			1		. WASHER,NONMETAL:0.191 ID X 0.625 INCH OD	86445	OBD
						- - - * - - -		
-74	----- -----			1		CKT BOARD ASSY:PS INVERTER(SEE A26 REPL)		
-75	214-2518-00			2		. HEAT SINK,XSTR:TO-220 OR TO-202	000BH	106B-B-HT
	344-0326-00			2		. CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
						(ATTACHING PARTS)		
	210-0632-00			4		. EYELET,METALLIC:0.089 OD X 0.125"LONG,BRS	01881	3168
						- - - * - - -		
-76	343-0844-00			1		RETAINER,CAP:PLASTIC	80009	343-0844-00
						(ATTACHING PARTS)		
-77	211-0513-00			1		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-78	210-0005-00			1		WASHER,LOCK:EXT #6	78189	1106-00
-79	210-0802-00			1		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
						- - - * - - -		
-80	129-0089-00			1		POST,ELEC-MECH:6-32 X 0.25 X0.83 INCH L	80009	129-0089-00
-81	210-0005-00			1		WASHER,LOCK:EXT #6	78189	1106-00
-82	----- -----			1		CKT BOARD ASSY:PS CAPACITOR(SEE A15 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-83	----- -----			2		. CAP.,FXD,ELCTLT:(SEE A15C1010 & A15C1012 REPL)		
						(ATTACHING PARTS)		
-84	212-0518-00			4		. SCREW,MACHINE:10-32 X 0.312 INCH,PNH STL	83385	OBD
-85	210-0010-00			4		. WASHER,LOCK:INT,0.20 ID X0.376" OD,STL	78189	1210-00-00-0541C
-86	210-0805-00			4		. WASHER,FLAT:0.204 ID X 0.438 INCH OD,STL	12327	OBD
						- - - * - - -		
-87	----- -----			1		XFMR,PWR,STPDN:(SEE T660 REPL)		
						(ATTACHING PARTS)		
-88	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-89	210-0005-00			2		WASHER,LOCK:EXT #6	78189	1106-00
						- - - * - - -		
-90	210-0202-00			2		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
						(ATTACHING PARTS)		
-91	210-0407-00			2		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
						- - - * - - -		
-92	348-0005-00			2		GROMMET,RUBBER:0.50 INCH DIA	70485	230
-93	348-0003-00			1		GROMMET,RUBBER:0.312 INCH DIAMETER	70485	1411B6040
	195-0440-00			1		LEAD,ELECTRICAL:18 AWG,13.0 L	80009	195-0440-00
	195-0441-00			1		LEAD,ELECTRICAL:18 AWG,11.0 L	80009	195-0441-00
	195-0442-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L	80009	195-0442-00
	195-0443-00			1		LEAD,ELECTRICAL:18 AWG,5.0 L	80009	195-0443-00
	195-0444-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L	80009	195-0444-00
	195-1600-00			1		LEAD,ELECTRICAL:18 AWG,17.0 L	80009	195-1600-00
	195-1601-00			1		LEAD,ELECTRICAL:18 AWG,6.0 L	80009	195-1601-00
-94	----- -----			1		CKT BOARD ASSY:PS INTERCONNECT(SEE A20 REPL)		
						(ATTACHING PARTS)		
-95	211-0601-00			4		SCR,ASSEM WSHR:6-32 X 0.312,DOUBLE SEMS	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-96	----- -----			1		. BUS CONDUCTOR:(SEE A20W1065 REPL)		
-97	131-2194-01			1		. CONN,RCPT,ELEC:CKT BD,12/24 MALE,R ANGLE	00779	1-87229-2
-98	131-1078-00			3		. CONNECTOR,RCPT,:28/56 CONTACT	95238	600-1156Y256DF30
-99	352-0482-00			1		HOLDER,CA,TIE:0.75 SQ,STICKY BACK,PLASTIC	06383	ABMM-A
-100	343-0549-00			4		STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY23M
-101	198-4238-00			1		WIRE SET,ELEC:	80009	198-4238-00
-102	198-4240-00			1		WIRE SET,ELEC:	80009	198-4240-00
-103	198-4239-00			1		WIRE SET,ELEC:	80009	198-4239-00
-104	198-4241-00			1		WIRE SET,ELEC:	80009	198-4241-00
-105	351-0303-00			3		GUIDE,CKT CARD:3 INCH LONG,PLASTIC	80009	351-0303-00
-106	441-1499-00			1		CHAS,PWR SUPPLY:ALUMINUM	80009	441-1499-00
						(ATTACHING PARTS)		
-107	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	211-0510-00			4		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-108	337-2701-00			2		SHIELD,ELEC:POWER SUPPLY	80009	337-2701-00
						(ATTACHING PARTS)		
-109	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	211-0510-00			4		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-110	129-0223-00			1		SPACER,POST:0.80 L,W/6-32 THD EA END	80009	129-0223-00
-111	210-0006-00			1		WASHER,LOCK:#6 INTL,0.018THK,STL CD PL	78189	1206-00-00-0541C
-112	351-0103-00			3		SLIDE,STRIP:12.6 X 0.063,AL	80009	351-0103-00
-113	407-2366-00			1		BRKT,CKT BD GUI:POWER SUPPLY	80009	407-2366-00
						(ATTACHING PARTS)		
-114	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
	211-0510-00			1		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
	334-3379-02			1		MARKER,IDENT:MARKED GROUNDSYMBOL	80009	334-3379-02
-115	343-0775-00			3		CLIP,SPR TNSN:	76381	3484-1000
-116	441-1497-00			1		CHAS,PWR SUPPLY:REAR,ALUMINUM	80009	441-1497-00
-117	198-4257-00			1		WIRE SET,ELEC:	80009	198-4257-00