MANUAL REVISION STATUS

PRODUCT: 4114 Computer Display Terminal

This manual supports the following versions of this product: Serial Numbers B010100 and up

REV.	DATE	DESCRIPTION
@	JUN 1981	Original Issue

CONTENTS

TABLES

ILLUSTRATIONS

3820-1

Section 1

INTRODUCTION

The 4114 Computer Display Terminal Service Manual is divided into two volumes. Volume 1 includes introductory information, operating information, circuit theory, a detailed description of the adjustment procedure, and maintenance information. Volume 1 is primarily a reference manual. Volume 2, on the other hand, contains frequently used information that the service technician needs to troubleshoot, repair, and adjust the terminal. This information includes an abbreviated adjustment procedure, electrical and mechanical parts lists, block and schematic diagrams, installation information, and a detailed explanation of Self Test, which is a built-in, firmware troubleshooting aid.

RELATED DOCUMENTS

Detailed information on the use of the 4114 terminal is found in the following documents.

- 4114 Computer Display Terminal Operator's Manual
- 4114 Host Programmer's Reference Manual
- 4110 Series Command Reference Manual

GENERAL DESCRIPTION

The 4114 is a high-resolution, microprocessor-controlled graphics computer terminal. The display is a 19-inch diagonal direct view storage tube. More than 12 million points on the display surface are individually addressable. By using these points, the display presents a graphic image made up of line segments. This image is displayed in either of two modes: Storage mode or Refresh mode. In Storage mode, the image is stable and permanent on the screen until it is erased. In Refresh mode, the image is continuously renewed, and therefore is easily moved around the screen surface. Graphics images can be contructed using both modes at the same time.

The 4114 uses microprocessor technology to create more than 100 primarily graphics-related commands. Using these commands, a host-resident software program run on a 4114 can create graphic images that can be displayed, modified, and sent to and received from a host computer. The 4114 carries most of the graphics processing-time burden if its local graphics commands are used.

The standard 4114 contains 32 K of RAM (read/write) memory and can contain up to 800 K of RAM memory on optional RAM Controller boards. As much as one megabyte of words can be stored on the optional flexible disks--512 K bytes per disk. The maximum host computer communication speed ("baud rate") is 19,200 bits per second for graphics and 38.4 K bits per second for text.

Set-Up mode uses English-language type commands to initialize many terminal operating parameters. Three of the major classifications are: general, dialog, and communications. In the general group, parameters like margin, echo, and Snoopy mode are set. In the dialog group, parameters like buffer size, line width, and number of lines are set. And in the communications group, parameters such as number of stopbits, kind of parity, and end-of-line string are set.

Most commands for the 4114 are encoded as three character ASCII codes beginning with the ESC character. The host computer controls the 4114 by sending it these three character ESC sequences in the order determined by each specific job to be done. (The Set-Up mode commands are encoded both as English-language type commands and as ESC sequences.)

Many features of the 4014 Computer Display Terminal are emulated by the 4114 terminal. Because of this, most application programs written for the 4014 run on the 4114 with very little or no modification. In addition, most peripheral devices that function connected to the 4014 also function when they are connected to the 4114. This includes Tektronix hard copy units and plotters.

PHYSICAL DESCRIPTION

The 4114 consists of two main parts: the display module and the pedestal. The display module sits on four plastic bumpers (feet) on top of the pedestal. After the terminal is installed, the display module and pedestal are connected by two cables--the AC Display power cable and the display cable.

The display module contains a 19-inch direct view storage tube. The mechanical package is similar to the Tektronix 618 Display Monitor. The display electronics inside the display module include high voltage and Z axis, storage, deflection amplifier, hard copy amplifier, and low voltage power supply circuitry. This circuitry is similar to that in the Tektronix GMA102A Display Monitor.

The pedestal consists of the keyboard, the low voltage power supply, the card cage, and six mounting plates on the rear panel.

The keyboard has a standard typewriter-like layout of ASCII-encoded keys. There are eight programmable and four command keys along with four LED indicator lights situated above the standard ASCII keys. There are also two thumbwheels--one moving up and down (controlling vertical motion on the screen) and one moving across (controlling horizontal motion on the screen).

Above the keyboard is the power switch. Optional flexible disk assemblies may be installed on one or both sides of the power switch.

The card cage and low voltage power supply are found inside the pedestal below the keyboard. The card cage contains plug-in circuit boards with dimensions of 8.5 by 11.5 inches.

The standard 4114 contains the following circuit boards:

- Motherboard. This has slots for five standard size circuit boards. The 80 pin bus of the Motherboard is the System Bus.
- Processor board.
- RAM/ROM board. This contains system EPROM and one 32 K RAM Array board.
- Display Controller board.
- Vector Generator board.

The 4114 may contain these optional circuit boards:

- Motherboard Extender. This increases the System Bus slots of the Motherboard to fifteen total slots. (Option 40 or 41)
- Three Port Peripheral Interface (3PPI) board. (Option 10)
- Tablet Controller board. (Part of Option 13 and 14)
- Disk Controller board. (Part of Option 42 and 43)

The low voltage power supply provides are the operating voltages for the Pedestal circuitry and is located above and to the right of the card cage--looking at the card cage from the front.

There are six removable mounting plates on the rear panel of the pedestal. One is standard and five hold optional connectors or L-brackets. The standard RS-232 host computer connector is mounted to the standard plate. The display cable connector is mounted here also.

OPTIONS

The following list of options is arranged in numerical order. Option numbers beginning with a letter designation are placed at the end of the list.

Option 1 Extended Communications (includes half-duplex, block mode, and downloader).

Option 2 Current Loop Interface (see Current Loop Interface Service Manual for detailed service information).

Option 10 Three Port Peripheral Interface (3PPI). This option supports the following peripheral devices:

4662 and 4663 Plotters
4641 and 4642 Printers
4923 Tape Recorder with Option 1 installed and other RS-232 devices

See the 4110 Series Option 10 3PPI Service and 4114 Operator's Manuals for details.

Option 13 Graphic Tablet. Size: 11 by 11-inches. Option hardware includes: Graphic Tablet (and pen), 411X Tablet Controller board, and Tablet Interface board. See the 4110 Series F13/14 Graphics Tablet Instruction and 4114 Operator's Manuals.

Option 14 Graphic Tablet. Size: 30 x 40-inch. Option hardware includes: Graphic Tablet (and pen), 411X Tabet Contoller board, and Tablet Interface board. See the 4110 Series F13/14 Graphics Tablet Instruction and 4114 Operator's manuals.

Option 24 One RAM Controller Board. Includes 32 K bytes of RAM on one RAM Array Board. Service information is in Volume 2 of this manual.

Option 25 One RAM Controller Board. Includes 64 K bytes of RAM on two RAM Array Boards. For service information, see Opt. 24.

Option 26 One RAM Controller Board. Includes 96 K bytes of RAM on three RAM Array Boards. For service information, see Opt. 24.

Option 27 One RAM Controller Board. Includes 128 K bytes of RAM on four RAM Array Boards. For service information, see Opt. 24.

Option 28 Two RAM Controller Boards. Includes 256 K bytes of RAM on eight RAM Array Boards. For service information, see Opt. 24.

Option 29 Four RAM Controller Boards. Includes 512 K bytes of RAM on sixteen RAM Array Boards. For service information, see Opt. 24.

Option 31 Color Enhanced Refresh. Display Module has special DVST that writes refreshed vectors in yellow-orange.

Option 40 Ten-Slot Peripheral Bus Extender. Includes Motherboard Extender, wire kit, and two 7 Watt fans.

Option 42 Single Flexible Disk Drive, and one Disk Controller board. The service information is located in the Option 42/43 Service Manual, and 119-0977-01/03 Drive Unit Service Manual.

Option 43 Dual Flexible Disk Drives and one Disk Controller board. The service information is located in the Option 42/43 Service Manual, and 119-0977-01/03 Drive Unit Service Manual.

Option 52 Customer-specified line voltage and frequency option.

Option A1 Universal European line voltage and frequency: 220 V, 50 Hz.

Option A2 United Kingdom line voltage and frequency: 240 V, 50 Hz.

Option A3 Australian line voltage and frequency: 240 V, 50 Hz.

Option A4 North American line voltage and frequncy: 240 V, 60 Hz.

ACCESSORIES

This list is divided into two parts: the standard accessories that are supplied with each 4114, and those accessories that may be ordered separately in addition to the standard accesories. The following accessories are also found in the parts list, where part numbers are listed for each item.

Standard Accessories:

- 4114 Operator's Manual
- Power cord set
- Host port RS-232 cable
- Eight relegendable key caps
- Six function-key overlays
- 4114 Host Programmer's Reference Manual
- 4110 Series Command Reference Manual

Optional Accessories:

- 411X Logic Extender board
- Relegendable key caps
- Function-key overlays
- 4114 Host Programmer's Reference Manual
- 4114 Service Manual, Volume 1 (final edition)
- 4114 Service Manual, Volume 2 (final edition)
- 4110 Series Option 10 (3 PPI) Service Manual
- 4110 Series F13/14 Graphics Tablet Instruction Manual
- 4110 Series F42/43 Disk Options Service manual
- 119-0977-01/03 Flexible Disk Drive Instruction Manual

Section 2

SPECIFICATIONS

GENERAL INFORMATION

This characteristics/specifications section lists two different types of specifications: those that are classified as environmental, physical, or "static" specifications (non-user verifiable specifications) and those that are verified as operational parameters of the 4114. The user verifiable specifications can be verified though the 4114 adjustment procedures in Section 10 of this manual. User verifiable specifications are noted in this section by an asterisk (*) next to the specification.

Most user verifiable specifications apply to the display module of the standard 4114 because of the amount of internal adjustments necessary in the display module to achieve a good display of characters and vectors on the crt screen. The display module contains more analog circuitry than the pedestal and so requires more adjustment than the pedestal. The digital circuitry that makes up the bulk of the pedestal circuitry requires very little adjustment. This digital circuitry is designed primarily to display information to the user by means of the crt in the display module. This circuitry does not have specific operational parameters (although the pedestal does contain some adjustments that are used to verify some specifications).

An introduction to the display module and general theory follows.

INTRODUCTION TO THE DISPLAY MODULE

The display module is a cabinetized unit that sits on top of the pedestal. The display module consists of a 19-inch bi-stable storage crt and associated input and deflection circuitry that accepts display information (a combination of analog and digital signals) from the Vector Generator board in the pedestal. The only connections with the pedestal are the AC power cord and the cable which connects to the J3000 (pedestal) and contains the control signals from the Vector Generator board. Display information can be any combination of vectors and alphanumeric characters. A bi-stable tube, as the name implies, either can store or not store an image. All stored images have the same intensity.

Storage refers to the ability of the tube to retain displayed images for long periods of time (up to an hour, sometimes longer). The displayed image only needs to be written once. The ability of the storage crt to retain the image eliminates the need for local memory and associated refresh circuitry. Character and vector generation circuitry can be simplified because a storage crt does not need to generate images at refreshed speeds. Also, the display module has two additional modes which do not feature storage. One mode allows the user to display refreshed information. The other mode permits the user to display refreshed information concurrently with the previously stored information. Both of these display modes must be constantly refreshed.

The display module circuitry is contained on four circuit boards plus an Interconnect board and Low Voltage Power Supply board.

The only external control on the display module is the REFRESH INTENSITY control.

DESCRIPTION OF THE DISPLAY MODULE

Hardware

The display module consists of four modules with provisions for options, interfacing, and additional electronic circuitry. The four modules are the following:

1. CRT MODULE. This consists of a crt, defection yoke, and crt shield. Although the Hard Copy Amplifier board is not connected to the crt shield, it is connected to the frame directly above the shield, and so, is considered part of the crt module.

2. CHASSIS MODULE. This consists of a frame that supports and provides mounting for the other three modules.

3. POWER SUPPLY MODULE. This consists of the low voltage power supply, line voltage selection, fusing, heat sink, and a cable to distribute power to the circuit module.

4. CIRCUIT MODULE. This is a card cage that has a six-slot Interconnect board. The Interconnect board contains a High Voltage and Z-Axis board, a Deflection Amplifier board, and a Storage board. The remaining three slots are for additional circuit expansion.

Display Features

The following display features are controlled by the pedestal via input lines to the display module.

- o DEFOCUS. Increases spot size slightly when displaying long vectors.
- o BRITE. Slightly increases Z-Axis drive for vector or large character drawings.
- o ERASE. Erases the display area.
- o COPY. Initiates a hard copy when a suitable Hard Copy Unit (HCU) is attached.
- o VIEW. Switches back to full brightness from a reduced intensity (Hold Mode).

The following display features are internally controlled:

- o HOLD MODE. Automatically reduces the stored image intensity after the display has been inactive for about 1.5 to 2.5 minutes.
- o DBUSY. An outgoing signal (flag) indicating that the display is busy and will not accept additional data until the signal line is inactive.
- o ANTIBURN. Prevents excessive writing beam turn-on without crt beam movement.
- o AUTO ERASE. Erases the screen after the display has been inactive for about 30 minutes (not to be confused with Hold mode, which simply reduces the stored intensity; AUTO ERASE completely erases the screen and information cannot be restored to VEIW).

INTRODUCTION TO THE PEDESTAL

The pedestal is a cabinetized unit on which the display module sits. The pedestal can be thought of as an "information processor". It takes information from the user through the keyboard, the host computer, the optional flexible disk drive(s) -- Option 42 or 43, or a variety of optional peripheral devices. This unit stores the information or makes it visible to the user via the display module. The pedestal contains a built-in keyboard, the power supply for the keyboard and pedestal circuitry, one or two optional flexible disk drives, RAM and ROM memory, and terminal circuits to process information and control output to the display.

The pedestal connects to an AC power source (at J3001) and can be wired to accept input voltages of 100 V, 120 V, 220 V, or 240 V. The pedestal supplies power (at J3002) and the necessary display information (at J3000) to the display. Any time the input voltage is changed for the pedestal, the input voltage straps for the display module must also be changed. The pedestal can communicate with a host computer through the J3006 connector. In addition, with options 1, 10, 13, or 14 installed, the 4114 can interface with a 4662 or 4663 plotter, a 4641 or 4642 line printer, a 4923 tape recorder, or a graphic tablet. The pedestal also has RAM options (24 through 29) which lets the user address up to 512K bytes of local memory.

The standard 4114 pedestal circuitry is contained on four circuit boards, a Motherboard, and the power supply module.

DESCRIPTION OF THE PEDESTAL

The 4114 pedestal consists of six modules with provisions for options, interfacing, and additional electronic circuitry. The six modules are as follows:

1. THE KEYBOARD. The keyboard is an ASCII data entry device that accepts commands, control information, and alphanumeric characters from the user, and acts as an output device for SELF TEST failure codes. The keyboard converts the alphanumeric data into an 8-bit binary code for use by the Processor board.

2. THE POWER SUPPLY. The power supply can be strapped to accept input voltages of 100 V, 120 V, 220 V, and 240 V from a single phase source. It provides a direct feed to the low voltage power supply in the display. Anytime the input straps on the power supply are set for one of the four input voltages, the straps in the display must also be set for that voltage. The pedestal power supply provides output voltages of +5.10 V, +12.00 V, -5.20 V, and -12.00 V for use by the pedestal circuitry. In addition, if Options 42 or 43 are installed, the power supply provides +24.00 V for disk drive operation.

3. THE CARD CAGE. The card cage consists of the Mother board, Mother Board Extender (Option 40), and the framework which holds the circuit boards in place. The card cage holds the RAM/ROM board (and any RAM option boards), the Vector Generator board, the Display Controller board, the Processor board, and any other circuit boards necessary for additional options. The card cage is located at the bottom of the pedestal.

4. THE RAM/ROM MEMORY. The standard 4114 contains one RAM/ROM board with 32K bytes of user addressable memory. With the extended RAM options (Options 24 through 29), the user can address up to 512K bytes of memory. The ROM contains the most of the system firmware that decodes local user commands, performs the SELF TEST routines, and other system tasks.

5. THE DISPLAY ELECTRONICS. The display electronics consists of the Vector Generator board and the Display Controller board. These two boards, in combination, provide the display with the signals telling it what to display on the screen. The output of the Vector Generator board goes directly to J3000, the communication line between the display and the pedestal.

6. THE PROCESSOR BOARD. The Processor board can be thought of as the central processing unit, or "heart", of the 4114. This microprocessor-based board takes data from the keyboard, memory, host computer, or other source, acts on it and stores it in memory, passes it to the flexible disks, and/or sends it to the display or memory.

SPECIFICATIONS

The following tables and lists specify the characteristics and performance specifications of the terminal, both display and pedestal parts. The specifications are valid only when these conditions are met:

1. The display module must be adjusted at an ambient temperature of between +20 C and +30 C (68 F to 86 F).

2. The terminal must be operating in an environment as specified under Table 2-1, Environmental Specifications.

3. Operations must be preceded by a warmup period of at least 20 minutes.

4. Specified power requirements must be met. See Section 11, Operating Voltage and Fuse Selection, and Table 2-6, Power Requirements. The terminal should be operated from a power source with its neutral at or near ground potential. It is not intended for operation from two phases of a multiphase system.

The following tables provide additional information on the indicated pages:

Table	Description
2-1	Environmental Specifications
2-2	Physical Characteristics
2-3	Display Specifications
2-4	Vertical and Horizontal Deflection
2-5	Graphics Specifications
2-6	Power Requirements
2-7	J3000, Rear Connector
2-8	J5005, Hard Copy Unit Connector

Table 2-1

ENVIRONMENTAL SPECIFICATIONS

Characteristic	Specification
Temperature	
Operating	
without flexible disks	+10 to +40 C (43 to 104 F)
with flexible disks (Options 42 & 43)	+10 to +38 C (43 to 100 F)
Non-Operating	
without flexible disks	-40 to +65 C (-40 to 149 F)
with flexible disks (Options 42 & 43)	-40 to +50 C (-40 to 122 F)
Altitude(a)	
Non-Operating	To 50,000 ft (15240 m)
Operating	To 15,000 ft (4572 m)
Humidity	
Without flexible disks:	
Non-Operating	90-95% maximum relative humidity
Operating	70-75% maximum relative humidity
With flexible disks installed (Options 42 & 43):	
Non-operating	8% to 80% non-condensing
Operating	20% to 80% non-condensing

(a) Maximum operating temperature decreases 1 degree C for every 1,000 feet above 5,000 feet in altitude.

Table 2-2

PHYSICAL CHARACTERISTICS

Characteristic	Specification
Weight of the Display Module	Approximately 100 lbs
Weight of the Pedestal	Approximately 150 lbs (This weight varies depending on the options installed; this is an average.)
Display Module Dimensions	Height 16.75 in (425.5 mm) Length 22.90 in (581.7 mm) Width 23.00 in (584.2 mm)
Pedestal Dimensions	Height 34.50 in (876.3 mm) Length 30.00 in (762.0 mm) (The greatest length -- measured from the back to the end of the keyboard.) Width 23.25 in (590.6 mm)
Total Weight of the terminal	Approximately 250 lbs
Dimensions of the terminal (See Figure 2-1.)	Total Height 51.25 in (1301.8 mm) Widest point 23.25 in (590.6 mm) Longest length 30.00 in (762.0 mm)

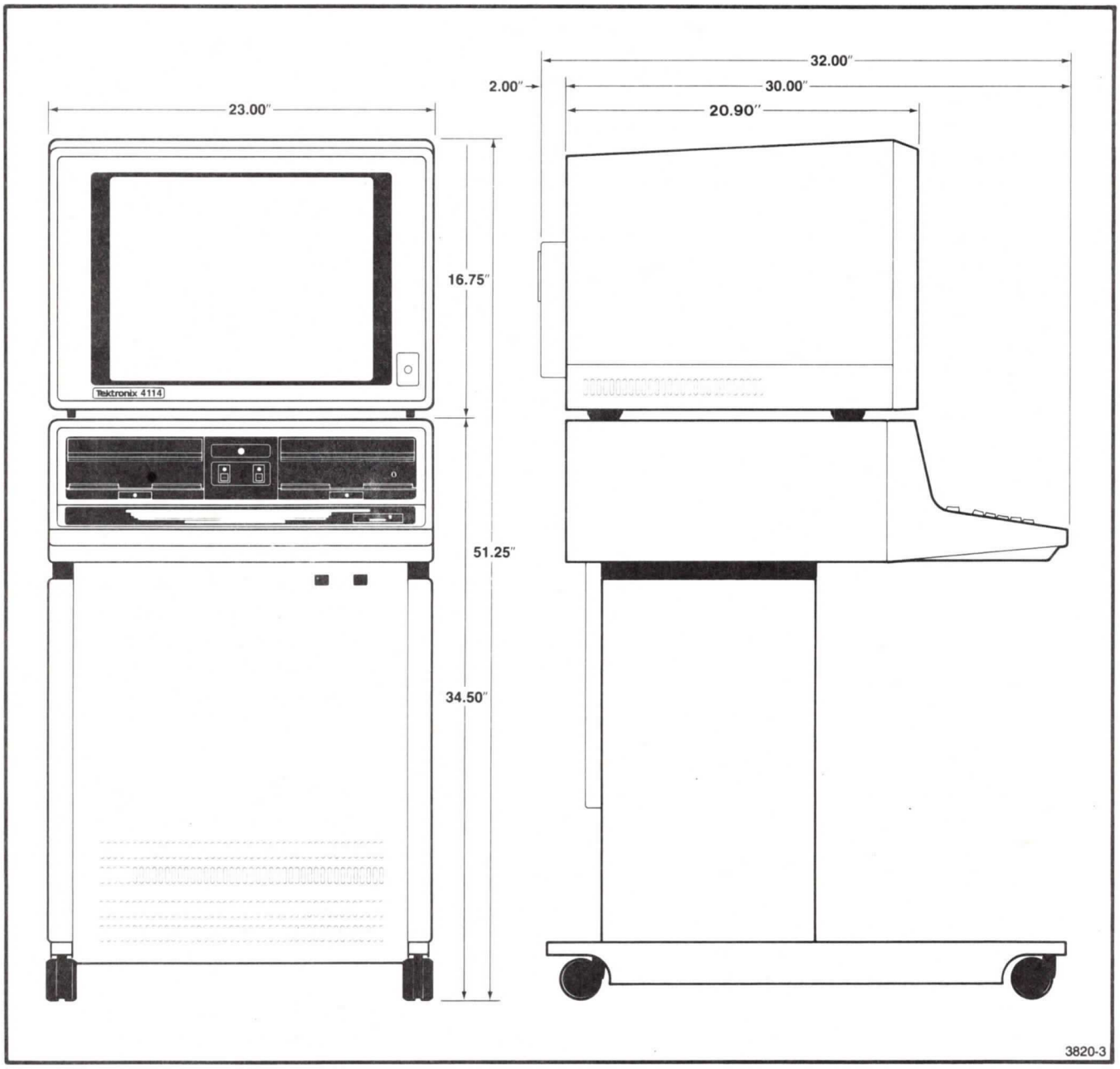


Figure 2-1. 4114 Dimensions

Table 2-3

DISPLAY SPECIFICATIONS

Characteristic	Performance Requirement
Crt	19 in (480 mm) curved face direct view storage tube.
Display Quality Area	14.5 in (368.3 mm) Long Axis 10.9 in (276.9 mm) Short Axis
User Addressable Area	13.9 x 10.5 in (353.1 x 266.7 mm)
Phosphor Type	Green P1
Heat Output	750 BTU per hour
Usable Storage Time (Viewing Time)	Recommended 15 minutes or less, but may be extended to one hour without permanent damage to the storage target. If a residual image is retained after a long viewing time, the target may be returned to normal condition by successive erasures.
Vector Writing Speed Stored Refreshed	 greater than or equal to 150 M/sec greater than or equal to 600 M/sec
Erase Time	1.5 seconds, ±12%
View Time (prior to entering hold mode)(a)	112 seconds ±20% after last display activity.
Auto Erase	Occurs 30 minutes ±20% after entering and remaining in Hold mode.
Geometry Orthogonality(a)	 Within ±1.2 degrees of 90 degrees at center screen.

(a) User verifiable specification.

Table 2-3 (cont)

DISPLAY SPECIFICATIONS

Characteristic	Performance Requirement
Parallelism(a)	Within ±1.5 degrees at edges of quality area.
Rectangle Short Axis Sides Long Axis Sides	 ±1.25% of long axis ±1.25% of long axis
Positional Accuracy	All points within the crt quality area are addressable with accuracy of ±1.25% of the long axis. The combined errors due to linearity, orthogonality, parallelism, geometry, and gain shall not cause positional inaccuracies greater than ± 1.25% of the long axis in either axis for any point of the display.
Linear Deflection Speed	Greater than or equal to 600/sec.
No. of Character Lines	64 maximum
No. of Characters per Line	133 maximum
Standard Character Set	Full ASCII character set 94 displayable characters; 128 displayable characters in "snoopy" mode.
Linearity Full Scale	 Within 1.25% (spot shall be within 1.25% of full screen width of proper position for voltage applied).
Incremental	No more than 10% difference in spacing between any two points for a given incremental voltage input.

NOTE

The earth's magnetic field may cause some noticeable display position, size, or shape changes if the display module is moved from or faced in any direction other than that in which it was adjusted.

Table 2-4

VERTICAL AND HORIZONTAL DEFLECTION

Characteristic	Performance Requirement
Input Signals	The X and Y inputs to the Deflection Amplifier are analog and differential. When driving from a single-ended source, the unused input should be grounded at the signal source.
Polarity	
+X	Positive voltage applied to positive input moves the beam right. Negative voltage moves the beam left.
-X	Positive voltage applied to the negative input moves the beam left. Negative voltage moves the beam right.
+Y	Positive voltage applied to positive input moves the beam up. Negative voltage moves the beam down.
-Y	Positive voltage applied to the negative input moves the beam down. Negative voltage moves the beam up.
Sensitivity	
Long Axis	5 V (10 V p-p) for full screen deflection horizontally.
Short Axis	3.75 V (7.5 V p-p) for full screen deflection vertically.

NOTE

Polarity is the same whether the crt has been rotated 180 degrees or not, providing the deflection input wiring on the Deflection Amplifier board is adjusted accordingly. (See Selecting X- and Y-Axis Inputs under Rotating the crt 180 degrees, Section 11.)

Table 2-5

GRAPHICS SPECIFICATIONS

Characteristic	Specification
Addressability	4096X x 4096Y Points
Graphic Command Syntax	Plot 10, 4010 Series, & IGL Syntax compatable
Line Types	Solid, dashed, and defocused
Interactive Graphics	Thumbwheels in the keyboard control a graphic cursor. The graphic cursor may have its shape defined by the user (with crosshairs as a default). The user can also control scrolling and the alpha cursor position by keyboard keys.

Table 2-6

POWER REQUIREMENTS

Performance Characteristic	Requirement
Display Module	
Power Consumption at 115 Vac, 60 Hz, full internal load.	220 W
Maximum running line current in 120 V connection.	2.6A
Line Fuse	
100 V Connection	4 A slow-blow
120 V Connection	4 A slow-blow
220 V Connection	2 A slow-blow
240 V Connection	2 A slow-blow
Line Voltage Ranges	
100 VAC	90 to 110 V
120 VAC	108 to 132 V
220 VAC	198 to 242 V
240 VAC	216 to 250 V
Pedestal Power Supply	
Maximum running line current in a 120 V connection.	6.8A
Maximum running line current in a 220 V connection.	3.4A
Line Fuse	
100 V connection	10.0 A fast-blow
120 V connection	10.0 A fast-blow
220 V connection	5.0 A fast-blow
240 V connection	5.0 A fast-blow
Line Voltage ranges	
100 VAC	90 to 110 V
120 VAC	108 to 132 V
220 VAC	198 to 242 V
240 VAC	216 to 250 V

NOTE

The 4114 has component recognition under Standard UL 478 (Data Processing) for line voltages up to 240 V. It also is certified by CSA according to standard C22.2, No. 154, for line voltages up to 125 V. It meets or exceeds DHEW X-Ray emmission standard; code of Federal Regulations, 21 CFR, sub-chapter J, parts 1020 and 1030, and TEK X-Ray standard 062-1860-00.

Table 2-7

REAR CONNECTOR (J3000)

(J3000 on the pedestal, which are also the pins on P5000 of the display)

Name	Type(a)	Pin	Signal	Description
+X	D	A	Linear	Input. Negative voltage (-V) moves beam left. Positive voltage (+V) moves beam right.
-X	D	E	Linear	Input. +V moves beam left. -V moves beam right.
X GND		K		Shield GND.
+Y	D	P	Linear	Input. +V moves beam up. -V moves beam down.
-Y	D	U	Linear	Input. -V moves beam up. +V moves beam down.
Y GND		Y		Shield GND.
Z Axis	D	a	TTL	Input. TTL true turns on Z-Axis, providing certain conditions are met. Can be strapped to accept either polarity and to reset View Timer.

(a) C designates a Control line to the display; D, a Data input line; and F, a Flag signal.

Table 2-7 (cont)

REAR CONNECTOR (J3000)

Name	Type	Pin	Signal	Description
Z GND		Z		Shield GND.
CHASSIS GND		S		Shield-chassis ground.
MAKE COPY-0	C	D	TTL	Loop-thru input. Low initiates a hard copy when the HCU is connected and ready.
HCU-0	F	J	TTL	Output. Low tells the Display Controller that a HCU is connected and will accept a MAKE COPY-0 command.
WRITE-THRU-0	C	N	TTL	Input. Initiates a reduced Z-Axis signal to prevent display storage for refreshed operation. Any prior stored information is kept in view.
NON STORE-0	C	T	TTL	Input. Low disable storage for directed beam refreshed operation. Written data storage is prevented by reducing target voltage.
BRITE-0	C	X	TTL	Input. When low, the crt writing beam intensity is increased slightly. Can be used with a focused beam to display medium sized characters or a defocused beam to display large characters or long vectors.

Table 2-7 (cont)

REAR CONNECTOR (J3000)

Name	Type	Pin	Signal	Description
DEFOCUS-0	C	b	TTL	Input. When DEFOCUS-0 is low, the crt writing beam is slightly defocused. Useful for displaying long vectors. Can be used with WRITE-THRU, NORMAL, or BRITE INTENSITY. See Table 9-1, Intensity and Focus Selections.
DBUSY-0	C	M	TTL	Output. Low indicates that the display is busy during an erase cycle, is in Hold mode, or is making a hard copy.
VIEW-0	C	L	TTL	Input. Low triggers active flood gun cycle of about 1.5 to 2.5 minutes, making it possible to store information on the crt and view previously stored information.
SLU-0	F	W	TTL	Output. Low indicates deflection system has not settled and is lagging the input deflection signal.
ERASE-0	C	R	TTL	Input. Low initiates the Erase cycle. 2 us minimum duration.

Table 2-7 (cont)

REAR CONNECTOR (J3000)

Name	Type	Pin	Signal	Description
DPC GND		F		Display Power Control ground. Goes to negative lead of solid state relay.
DPC		B		Display Power Control. Supplies power to the display module when the 4114 pedestal power is turned on. Goes to positive lead of the solid state relay.

(a) C designates a Control line to the display; D, a Data input line; and F, a Flag signal.

Table 2-8

HARD COPY UNIT CONNECTOR (J5005)

Name	Pin	Signal	Description
FAST RAMP GND	1 2	Linear	Fast scan ramp from the Hard Copy Unit (HCU). Ramp amplitude is 10 V centered at 0 V. Adjustable centering.
SLOW RAMP GND	3 4	Linear	Slow scan ramp from HCU. Ramp amplitude is 10 V, centered at 0 V. Adjustable centering.
HC Inter-0 GND	5 6	TTL	Input. Controls Z-Axis during HC Scan. 400 ns pulse width at a 1.4 us pulse repetition rate.
Tarsig-0 GND	7 8	TTL	Output. Goes low when scan crosses a written area on the crt. Causes the HCU to reproduce on paper what is stored on the crt screen.
Read-0	9	TTL	Input. Causes display unit to switch into HC mode.
Display Size-0	10	TTL	Output. Low output indicates 19-inch display to HCU (tied to ground).
Remote Copy-0	11	TTL	Output. Initiates one HC cycle. Useful for remote control. Requires ground closure (TTL low) for > 1 ms.
Copy Busy	13	TTL	Input. High when HC is busy (applies to HCUs without multiplexing capability).

Table 2-8 (cont)

HARD COPY UNIT CONNECTOR (J5005)

Name	Pin	Signal	Description
HCU-0	13	TTL	Input. Low if HCU having multiplexing capability is connected and is ready.
Wait-0	14	TTL	Input. Low until display has been scanned (does not apply to HCU without multiplex option).
Frame GND	15		Earth (Cable Shield).

Section 3

OPERATING INFORMATION

This section provides simplified operating instructions and examples so a service person may quickly exercise the 4114 in its primary operating modes. This information is intended to familiarize the service technician with the terminal's operation and show whether or not the 4114 is functioning properly from the operator's point of view. This is not intended as a hardware diagnostic tool but rather as a verification that the 4114 is functioning and interacting properly with its host computer. The Self Test routine described in Appendix E isolates any hardware malfunctions.

Section 1 gives a general introduction to the terminal and describes the controls and indicators. The Operator's Manual provides detailed information about controls and the commands needed to operate the 4114 and its options.

Most of the keyboard looks like a typewriter keyboard. There are also keys reserved for special functions. There are eight keys with no predefined meaning reserved for the user to program (see Table 3-3). Most of the regular keys can be programmed also.

The four lights on the keyboard indicate:

(1) when the keyboard is inactive (KBD LOCK),
(2) when the screen is filled with text (PAGE FULL),
(3) when the terminal is transmitting data (XMT), and
(4) when it is receiving data (RCV).

These are explained more fully in the 4114 Operator's Manual.

The thumbwheels are used to scroll the dialog area and for sending graphics information to a program (see Table 3-2 and 3-5).

All TEKTRONIX PLOT 10 software: Interactive Graphics Library, Terminal Control System, and Easy Graphing, can be used on the 4114 exactly as on previous terminals. The 4114 also supports a full complement of peripherals as well. These may include plotters, hard copy units, printers, and tape drives.

OPERATING CONTROLS

(Refer to Figure 3-1.)

The 4114 has the following user operable controls:

ON/OFF Switch	Located on the front of the pedestal on the center module between the two flexible-disk drive units. To turn on power to the terminal, push in and release. A click will be heard and the mechanical eye will open up and show green on the push-button.
DISK-DRIVE Drawer	Located in the Pedestal beside the power ON/OFF Switch module. The unit busy light, an LED in the center of the drawer on the drawer switch is on whenever the unit is energized. The drawer switch is pushed to open the drawer and change the disk.

CAUTION

Do NOT attempt to remove or insert a disk while the unit busy light is on. To do so may cause irreparable damage to the disk, the read/write heads of the unit, loss of the program on the disk, or all three.

WRITE PROTECT Switch	A rocker switch adjacent to the disk-drive drawer(s) and immediately below the power ON/OFF switch on the center module. An LED indicator light is on when write protect is enabled.
REFRESH INTENSITY	This is a potentiometer on the front of the display unit in the lower right-hand corner. Turning it CW (clockwise) increases the refresh intensity and turning it CCW (counterclockwise) decreases the intensity.

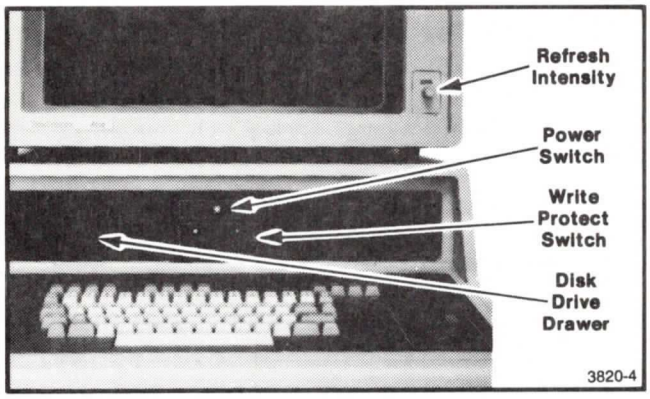


Figure 3-1. Front View Showing Operator Controls.

KEYBOARD

(Refer to Figure 3-2.)
Most of the keys on the keyboard are the same as on a typewriter.

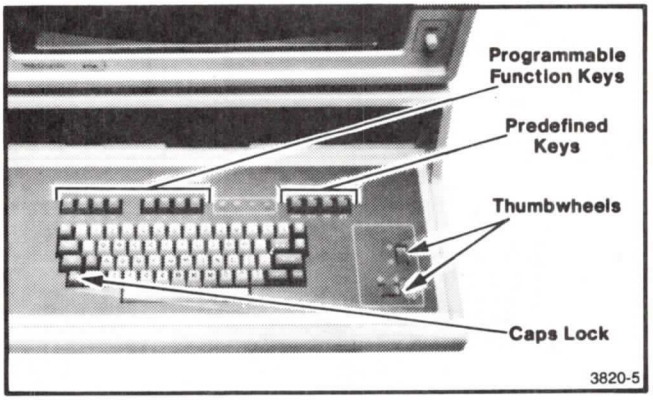


Figure 3-2. Keyboard with Function Keys and Thumbwheels.

The four predefined keys have the following functions:

DIALOG - CLEAR	Dialog causes the dialog area to be displayed. It is in use when the key is lit. Clear is the shifted function of the dialog key. It erases the dialog area.
SETUP	Set up enables the terminal to receive commands.
LOCAL - CANCEL	Local places the terminal under local control. When local is selected, the host has no effect and local echo is employed. Cancel is the shifted version of the local key. It cancels anything that the terminal is presently doing except spooling.
HARD COPY	The contents of the screen are sent to a hard copy unit if one is available.
CAPS LOCK	Caps lock causes alphabetic characters to be upper-case but does not affect numeric or special symbol keys.
FUSE	(Refer to Figure 3-3.) The fuse is a 10A FB, size 3AG, located on the back of the pedestal on the power suppply heat sink.

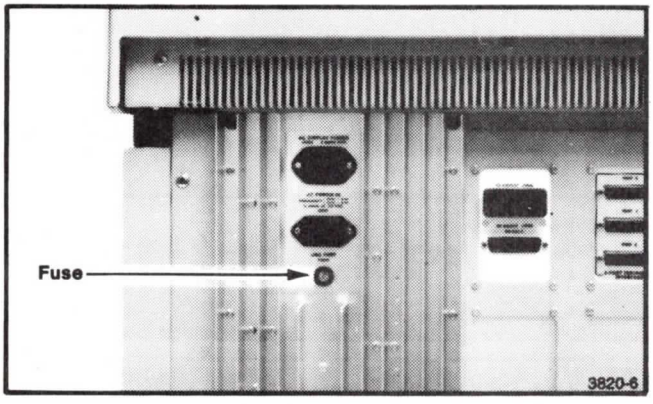


Figure 3-3. Rear View of 4114 Pedestal Showing the Fuse.

GETTING STARTED

This part of Section 3 is a tutorial exercise based on seven examples (each listed as a table). Each example can be read, or the examples may be followed, step-by-step, for hands-on understanding of the terminal.

Normally, the terminal is controlled by a host program. The operator's task is to set up the terminal for use, and to respond to the directions given by the host resident program.

Tables 3-1 through 3-4 illustrate tasks which are likely to be performed by an operator.

Tables 3-5 through 3-7 illustrate some of the terminal's features an operator will not usually access directly. They are included in this section to provide some exposure to more of the 4114's features. They do not reflect typical usage of the terminal by an operator.

The tables illustrate:

- setting up the terminal for use
- Setup mode
- the dialog area
- programming keys
- creating a graphics segment
- manipulating a graphics segment
- graphics input

Conventions: The following conventions are used in the examples.

- It is assumed that the terminal is installed and ready for operation. See Appendix A in the 4114 Service Volume 2 for installation procedures.

- Setup commands in the examples are shown in UPPER CASE. However, any English-like setup command can be entered in either upper or lower case. (An "escape sequence" entered in Setup mode must be all upper case, see Table 3-5). If you want to enter all upper case characters as shown, press the CAPS LOCK key (Figure 3-2).

- The commands are followed by the following character:

  (CR)

- This is understood to execute the command.
- Individual keys (A) are enclosed in parentheses.
- <Text strings are enclosed by angle brackets.>
- Do Table 3-1 first. The steps in Table 3-1 set up the terminal.

The information in Tables 3-2, 3, and 4 can be done independently. Table 3-5 must be done before Tables 3-6 and 3-7.

TURNING ON THE 4114

(Refer to Table 3-1).

To turn on the 4114, press the power switch (Figure 3-1) until it clicks. When you release it, you will notice a green indicator in the center of the switch.

The terminal tests certain parts of its memory and circuitry every time it is turned on. On a properly functioning terminal:

- the four indicator lights and lights in other keys all turn on,
- the light in the CAPS LOCK key turns off,
- all lights turn off,
- the XMT and RCV indicator lights flash once each,
- the cursor appears in the upper left corner of the screen, and the terminal is ready for operation.

If the test fails, the terminal bell may ring once or three times, some of the lights may remain on, and there may be a message displayed on the screen. If this happens, see Section 11 (Maintenance), or the Operator's Manual for details.

GETTING THE TERMINAL READY

Complete the steps in Table 3-1 before doing any of the other tables in this section. Table 3-1 executes a series of commands that prepare the terminal for subsequent examples. It is important for the terminal to have a specific status so the other examples will appear as illustrated.

The commands used in Table 3-1 are not explained in detail in this section. For more information on their use, see the 4114 Operator's Manual.

Table 3-1

GETTING THE TERMINAL READY

	Step	Comment
1.	If the terminal is on, skip to step two. If the terminal is off press the POWER switch, (Figure 3-1).	When you release the POWER button the green indicator appears in it. You can hear the ventilation fans in the terminal. If some of the indicator lights remain on and the terminal bell rings, it has failed the power up sequence. See the 4114 Operator's Manual for details.
2.	If the terminal is already on, press the RESET button.	This resets the terminal to its power up default status.
3.	Press the LOCAL key (Figure 3-2).	The red light in the key turns on and the terminal enters Local mode.
4.	Press the following keys: (ESC)(8)	This command sets text size of the terminal. If the text was already set to this size, there is no change. The size of the cursor changes to reflect the new text size.
5.	Press the LOCAL key.	The light in the key turns off and the terminal exits from Local mode.
6.	Press the key labeled SET UP (Figure 3-2).	The red light in the key turns on.

Table 3-1 (cont)

GETTING THE TERMINAL READY

Step	Comment
7. Enter the folowing command: <MARGIN 2>	This command causes the terminal to divide the screen into two columns when it displays text.
8. Enter the following command: PAGEFULL NONE	This command causes the terminal to not take any special action when the screen is filled with text.
9. Press the PAGE key. (Figure 3-2)	The screen is erased.
10. Press the SET UP key.	The terminal exits from Setup mode. The red light in the key turns off.

SETUP Mode

English-like commands (called "setup commands") can be executed to define the terminal's operating environment when the terminal is in the Setup mode. This includes such things as communications conditions, size and position of the dialog area, what kinds of errors the terminal displays, control of peripherals, and so on.

Communications to a host computer are suspended when the terminal is in Setup mode. Messages received from the host are stored in the terminal's memory and displayed when Setup mode is exited.

If a mistake is made in Setup mode, the terminal displays an error message immediately below the incorrect command. In most cases these messages are self-explanatory. The 4110 Command Reference Manual lists Setup mode error messages and their meanings in Appendix C.

Setup commands are a subset of the 4114's command repertoire. Setup commands are used most often by an operator and knowledge of these commands will be most useful. Setup mode also allows you to execute 4114 commands for which there are no English-like commands. These are called "ESCape sequences" because the first character in each of these commands is the "ESCape" character. Tables 3-5, 6, and 7 illustrate the use of ESCape sequence commands.

The use of a few setup commands is illustrated in this section. See the 4114 Operator's Manual for a complete description of SETUP commands.

Table 3-2 illustrates the use of Setup mode and specifically includes the STATUS and EDITCHARS setup commands. Other setup and ESCape sequence commands are demonstrated in subsequent examples.

Table 3-2

SETUP MODE

Step	Comment
1. Press the PAGE key.	The screen is erased.
2. Press the SET UP key.	The red light in the key turns on.
3. Enter the following command: STATUS	A report of the status of the terminal is displayed. The terminal remembers the new values for the status as they are entered. These values are retained after the terminal is turned off. There are four or five categories of parameters (the last category is optional): REPORT/INPUT GENERAL DIALOG COMMUNICATIONS OPTIONAL COMM The word in the left column of the status report is the name of a setup command. The current setting of each parameter of the command is listed to its right. Only those commands whose parameters are remembered when the terminal is turned off and then back on are listed.

4. Press the PAGE key.	The screen is erased. The cursor returns to the upper left corner of the screen.
5. Enter the following command: STATUS COMMUNICATIONS	A report of just the COMMUNICATIONS parameters is displayed.
6. Press the PAGE key.	The screen is erased.
7. Enter the following command: STATUS EDITCHARS	A report of the status of the EDITCHARS parameters is displayed. The first two characters shown in this report correct typing errors when the terminal is in Setup mode. RUB OUT backs up the cursor one space each time the key is struck. (CN) represents the cancellation of a character. An entire line may be cancelled by pressing (CTRL)(X). The third character is the "literal" character. It is used in a macro when the (CR) is included as part of the macro.
8. Enter the following command: STATUX	The terminal will display an error message. ">> Terminal Detects Error : "Nonexistent Command" appears on the screen on a single line.

9. Enter the following command (do not press the RETURN key): STATUX	
10. Press (RUB OUT) once.	The cursor backspaces one character.
11. Type the character "S" over the character "X" and press the carriage return.	The STATUS report is displayed. If the screen is filled before the end of the report, the cursor returns to the upper left corner and continues. If there is already text in that part of the screen, it is overwritten. This is controlled by the PAGE-FULL command, as explained in the 4114 Operator's Manual.
12. Press the PAGE key.	The screen is erased.
13. Enter the following command (do not press the RETURN key): DTATUS	An error message would be displayed if the (CR) is pressed.
14. Press (CTRL)(X)	This is the "line edit" character. When you press the line edit key, the terminal displays two asterisks and moves down to the next line.
15. Press the SET UP key.	The terminal exits from Setup mode. The red light in the key turns off.

THE DIALOG AREA

Conversation with the terminal and host can be directed to a particular area of screen called the "dialog area."

The dialog is stored in part of the terminal's memory called the dialog buffer. Depending on its size, all or part of the dialog buffer can be viewed at once. The portion of the screen on which the dialog buffer is displayed is called the "dialog area."

For example, several commands may be given to the terminal in Setup mode. Setup is then terminated by pushing the SETUP button. A graphics program may then be initiated by the operator for the host to do. By using the dialog area, separate commands can be given to the terminal and to the host by the graphics output. This prevents the dialog from cluttering up the screen.

Table 3-3 illustrates the DAENABLE, DALINES, DACHARS, and DAPOSITION setup commands as well as use of the thumbwheels.

4010-Compatibility

A program written for a TEKTRONIX 4010-series terminal can also be run on a 4114. However since 4010-series terminals do not have a dialog area, some special consideration must be made for 4010 graphics which include text.

If you execute a 4010 program with text (such as for a title or labels) on a 4114 with the dialog area enabled, the 4114 would strip the title and labels out of the picture and display that text in the dialog area.

DAENABLE prevents this. It enables or disables the dialog area as necessary. When the dialog area is "disabled," the 4114 does not intercept text and display it in the dialog area. This allows a 4010 program with text to execute on a 4114 the same as on a 4010-family terminal.

The examples used in this section are very simple. See the examples using the DAENABLE command to ensure that the dialog area is enabled. Since there is no text output in any of the examples, it is not necessary to disable the dialog area. For more detailed information on the DAENABLE command, see the 4114 Operator's Manual.

Table 3-3

THE DIALOG AREA

	Step	Comment
1.	Press the SET UP key.	The light in the key turns on as the terminal enters Setup mode.
2.	Enter the following command: DAENABLE YES	This command "enables" the dialog area, causing subsequent dialog to appear in it. When you press the (CR) key, the cursor disappears. This is because the cursor is in the dialog area, even though the dialog area is not yet visible.
3.	Press the DIALOG key.	The light in the key turns on and the cursor and prompt appear in the first line of the dialog area.
4.	Enter the following command: STATUS	The STATUS report is displayed. However, all of the report is not visible since only a part of the screen is being used for the dialog area.
5.	Press the DIALOG key.	The light in the key turns off and the dialog area is no longer visible. The cursor is not visible either. This is because the dialog area is enabled and even though it is not visible, the cursor remains in it.

6. Press the DIALOG key.	The light in the key turns on and the dialog area and cursor are visible again. Notice that no text is lost when the dialog area is turned off and then back on.
7. Rotate the Y-axis thumbwheel (Figure 3-2) down (towards yourself).	As you rotate the thumbwheel, the screen is scrolled allowing portions to be seen that were not previously visible. Notice that the cursor always remains on the last line of the dialog area.
8. Rotate the thumbwheel up (away from yourself) until the cursor is visible again.	
9. Press the SHIFT and CLEAR keys at the same time.	The dialog area is erased.
10. Enter the following command: DALINES 20	This command specifies the maximum number of lines of the dialog buffer visible on the screeen at a time. The new specified number of visible lines becomes effective the next time the dialog area is visible.
11. Toggle the DIALOG key (press it twice).	The first time you press it, the light in the key goes out and the dialog area becomes invisible. When you press it the second time, the light in the key turns back on and the dialog area reappears with the new DALINES specification.
12. Enter the following command: DACHARS 10	This command specifies the maximum number of characters on each line of the dialog area. The new line size becomes effective the next time the dialog area becomes visible.
13. Toggle the DIALOG key (press it twice)	When you press the key the second time the dialog area reappears.
14. Enter the following command: STATUS DIALOG	Notice that the lines in the dialog area are now ten characters long.

15. Enter the following command:

    DAPOSITION 1000,1000

    This command specifies the location of the dialog area. The location is updated the next time the dialog area becomes visible.

16. Toggle the DIALOG key

    When you press it the second time, the light in the key comes back on and the dialog area reappears at its new location.

17. Enter the following commands to restore the dialog area to its factory default orientation:

    ```
    DALINES 5
    DACHARS 73
    DAPOSITION 0,0
    ```

    Toggle the DIALOG key.

    The dialog area is again in its default orientation.

18. Press the SET UP key.

    The light in the key turns off and the terminal exits from Setup mode.

PROGRAMMING KEYS

Most of the 4114's keys are programmable. Eight keys have no pre-defined meaning (labeled F1 through F8). Each key can have two meanings programmed into it -- one is transmitted when you press the function key by itself, the other when you press the function and SHIFT keys at the same time time. Keys can be programmed with any character or character string -- such as commands to the terminal or to the host computer.

The keys can be programmed by commands you enter from the keyboard, or by commands received from a host resident program. They can also be programmed by a file on a flexible disk containing appropriate commands.

Predefined keys are indicated in Figure 3-2. They are not programmable because they are "command keys," reserved to perform functions you will use often.

Table 3-4 illustrates the use of the DEFINE command, which is used to program a key. There are several variations of the DEFINE command, all of which are explained in the 4114 Operator's manual.

Table 3-4

PROGRAMMING KEYS

	Step	Comment
1.	Press the PAGE key.	The screen is erased.
2.	If the light in the DIALOG key is on, press the key.	The light in the key turns off. If the dialog area is enabled, the cursor disappears. If it is not enabled, the cursor moves to the top of the screen.
3.	Press the SET UP key.	If the dialog area is enabled, the lights in the SET UP and DIALOG keys both turn on and the cursor and a prompt appear in the first line of the dialog area. If the dialog area is not enabled, follow Step two in Table 3-3 and then do step three of this example.
4.	Clear the dialog area by pressing SHIFT and CLEAR.	If there was any text in the dialog area, it is erased.
5.	Enter the following command: DALINES 20	This makes the dialog area large enough to see most of the commands entered.
6.	Toggle the DIALOG key	This updates the dialog area to its larger size. If the dialog area was already set to 20 lines, there will be no change.

7. Enter the following command: DEFINE F1 /Hi there/	When the carriage return is pressed, the asterisk moves down to the next line.
8. Clear the dialog area.	The dialog area is erased.
9. Press the SET UP key.	The red light in the SET UP key and the DIALOG key turns off and the asterisk disappears as the terminal exits from Setup mode.
10. Press the LOCAL key.	The light in the key turns on as the terminal enters Local mode. When the terminal is in Local mode, the terminal echoes information as if it were coming from the host but does not try to execute it as a command.
11. Press F1.	"Hi there" appears on the screen.
12. Press the SET UP key.	The red light in the SET UP and the DIALOG key comes on as the terminal enters Setup mode; the asterisk appears at the left margin of the line in the dialog area. Now the SET UP, LOCAL, and DIALOG lights are on. When the terminal is in both Setup and Local at the same time, the Setup mode takes priority.
13. Clear the dialog area.	The dialog area is erased.

14. Enter the following command:

    STATUS EDITCHARS

15. Enter the following command:

DEFINE F2 /Hi there<literal>(CR)(LF)/

When you type the literal character (in this case ~) it is echoed on the screen. When you press (CR), the cursor backspaces and types over the literal character.

16. Clear the dialog area.

The dialog area is erased.

17. Leave the Setup mode.

The lights in the SET UP and DIALOG keys go out.

18. Press F2 several times.

The message "Hi there" is printed on a separate line each time the key is pressed.

19. Enter Setup mode again.

The lights in the SET UP and DIALOG keys come on again.

20. Enter the following command:

    DEFINE F1

This command deletes the macro assigned to key F1.

21. Leave Setup mode, enter Local Mode and press F1.

Nothing happens since there is longer a macro associated with that key.

22. Enter Setup Mode and then enter the following command:

    DEFINE ALL

This command deletes all currently assigned macros.

23. Press the SET UP key.

The light in the SET UP key turns off.

Creating a Graphics Segment

A graphics segment is a picture or a part of a picture which can be manipulated by 4114 commands. This allows you to manipulate a part of a picture without having to continually compile and execute an entire program.

The creation of a segment is usually accomplished by a software program. This table shows you how to do it from the terminal, so you can better understand this concept, since it is used in subsequent examples.

This also illustrates the use of "escape sequence" commands with the terminal in Setup mode. Note the following conventions concerning escape sequences:

- (ESC) means press the ESCAPE key
- alphabetic characters must be upper case
- use of the space character is important; most commands consist of the (ESC) followed by two upper case alphabetic characters followed by a space and then the first numeric parameter; there is also a space between each of the following numeric parameters.

If you have a program which creates a simple picture, you can log onto your host and execute that program. Do not use a program which includes text. Using the dialog area, with a program that includes text, is described in the 4114 Operator's Manual.

At the end of the example, the segment remains on your screen. The same segment is used in Tables 3-6 and 3-7. The segment is deleted from the terminal's memory at the end of Table 3-7.

Table 3-5

CREATING A GRAPHICS SEGMENT

	Step	Comment
1.	If the DIALOG light is on, press the key to turn it off.	The light in the key turns off. If the dialog area is enabled, the cursor disappears.
2.	Enter Setup Mode.	The lights in both the SET UP and DIALOG keys turn on if the dialog area is enabled. If the dialog area is not enabled, follow Step two in Table 3-3 and then continue with Step four in this example.
3.	Clear the dialog area.	If there was any text in the dialog area, it is erased.
4.	Press the SET UP key.	The lights in the SET UP and the DIALOG keys turn off and the terminal exits from Setup mode. If the dialog area is not turned on explicitly by pressing the DIALOG key, the dialog is turned off when the terminal exits from Setup mode.
5.	Press the DIALOG key.	The light in the key turns on and the dialog area becomes visible.
6.	Log onto the host computer.	
7.	Press the SET UP key.	The lights in the SET UP and DIALOG keys turn on and the terminal enters Setup mode.
8.	Enter the following command: (ESC)<SO> 1 (CR) Use upper case.	The terminal "opens" segment one. This means that subsequent graphics data is captured into segment 1.

9. Press the SET UP key.	This allows the terminal to exit from Setup mode so it may communicate with the host computer; the light in the SET UP key turns off. The light in the DIALOG key remains lit because the key was explicitly pressed in step five.
10. Enter the necessary commands to run a graphics program on the host.	As the picture is displayed, it is being captured in segment 1.
11. When the programm is finished running, press the SET UP key.	The light in the SET UP key turns on and the terminal enters Setup mode.
12. Enter the following command in upper case. (ESC)>SC> (CR)	The terminal "closes" the open segment. Incoming data is no longer captured in a segment.
13. Press the SET UP and DIALOG keys.	The lights in the SET UP and dialog keys turn off and the terminal exits Setup mode.
15. Log off the host computer.	
16. Clear the dialog area.	The dialog area is erased.
17. Press the PAGE key.	Graphics which is not part of a segment is erased. The segment is erased momentarily and redrawn.

Manipulating a Graphics Segment

Table 3-5 illustrated how to create a graphics segment. Table 3-6 takes you a little further by showing you some of the ways you can manipulate a segment.

Table 3-6 assumes that the segment created in Table 3-5 is still on the screen. This example illustrates escape sequence commands which make the segment:

- invisible
- visible
- appear in refresh
- appear in storage
- highlighted
- unhighlighted

There is a brief description of refresh and storage graphics in the description of the dialog area, just before Table 3-3. The escape sequence command format is described prior to Table 3-5.

The manipulation of a segment is normally accomplished under program control. The simple examples shown here illustrate just a few of the ways a segment can be used. See the 4114 Host Programmer's Manual and the 4110 Command Reference Manual for details.

Table 3-6

MANIPULATING A GRAPHICS SEGMENT

	Step	Comment
1.	Turn off the DIALOG key if it is on.	The light in the key turns off. If the dialog area is enabled, the cursor disappears.
2.	Press the SET UP key.	If the dialog area is enabled, the lights in the SET UP and DIALOG keys both turn on. If the dialog area is not enabled, follow Step two in Table 3-3 and then continue with Step four in this example.
3.	Clear the dialog area.	If there was any text in the dialog it is erased.
4.	Enter the following command to make the segment invisible: (ESC)<SV 1 0>	There is no immediate effect on the segment; the asterisk appears on the next line as a prompt.
5.	Enter the following command to make the segment visible again: (ESC)<SV 1 1>	The segment becomes visible as soon as you press the RETURN key.
6.	Enter the following command to draw the segment in refresh: (ESC)<SM 1 2>	No visible change to the segment; the asterisk appears on the next line as a prompt.

7.	Turn the REFRESH INTENSITY knob to the left.	The displayed segment dims as the knob is turned. If you turn the knob all the way to the left, the segment disappears. If you turn it all the way to the right, the segment becomes bright and is stored on the screen. If that happens, turn the knob back counterclockwise and press the PAGE key.
8.	Enter the following command to draw the segment in storage: (ESC)<SM 1 1>	The segment may appear brighter again.
9.	Enter the following command to "highlight" the segment: (ESC)<SH 1 1>	The segment "blinks" slowly. Turn the REFRESH INTENSITY knob to the right to make the blinking more noticeable.
10.	Enter the following command to discountinue highlighting of the segment: (ESC)<SH 1 0>	The segment stops blinking.
11.	Press the SET UP key.	The light in the key turns off and the terminal exits from Setup mode.
12.	Press the DIALOG key.	The dialog area becomes visible.

Graphics Input

Graphics input (GIN) mode allows you to send graphics information to a program.

In a typical use of GIN mode you would log onto a host and execute a program. The program would display some graphics or text and prompt you to position the graphics cursor to send some data to the program or indicate a choice of action. The program would continue to prompt you until all of the necessary information had been sent, and then would terminate GIN mode.

Although it is typically accomplished by program control, Table 3-7 illustrates the use of escape sequence commands to enter GIN mode and use some of its features.

The information in this table assumes that a graphics segment is displayed (see Table 3-5).

Table 3-7

GIN (GRAPHICS INPUT) MODE

	Step	Comment
1.	Press the PAGE key.	The screen is erased. The segment on the screen is redrawn.
2.	Turn off the DIALOG key if it is on.	The light in the key turns off.
3.	Press the SET UP key.	If the dialog area is enabled, the lights in the SET UP and DIALOG keys both turn on. If the dialog area is not enabled, follow Step two in Table 3-3 and then continue with Step four of this example.
4.	Clear the dialog area.	If there was any text in the dialog it is erased.
5.	Enter the following command: (ESC)<IE 0 1>	The crosshair cursor becomes visible as the terminal enters GIN mode.
6.	Press the SET UP key.	The lights in the SET UP and DIALOG keys turn off as the terminal exits from Setup mode.

7. Rotate each thumbwheel.	The horizontal line of the crosshair cursor moves up and down as the right thumbwheel is rotated. The vertical line of the crosshair moves left and right as the bottom thumbwheel is rotated.
8. Press an alphanumeric key.	In an actual GIN situation, this would "locate" the point at which the crosshair cursor is positioned when you press the key. The coordinates of that point would be sent to the graphics program. In this case, when you press the key the crosshair cursor disappears and the terminal exits from GIN mode.
9. Press the SET UP key.	The red light in the key turns on and the terminal enters Setup mode; the dialog area also becomes visible.
10. Enter the following commands: (ESC)<II 0 1> (ESC)<IR 0 1> (ESC)<IE 0 5>	The terminal enters GIN mode again, with "rubber banding" and "inking" in effect. II is inking. IR is rubberbanding. IE means enter GIN. 0 means use the thumbwheels for the locator function. 5 means perform 5 GIN events.
11. Press the SET UP key.	The lights in the SET UP and DIALOG keys go out. The terminal exits from Setup mode and the dialog area becomes invisible.
12. Press an alphanumeric key.	The crosshair cursor blinks momentarily then reappears.

13. Rotate the thumbwheels to move the crosshair cursor to another point.	Notice that a line follows the cursor as you move it. This is the "rubberbanding" feature.
14. Press an alphanumeric key.	A line is drawn from the last point located to the current point. This is the "inking" feature of GIN mode.
15. Continue to move the thumbwheels and press 3 more alphanumeric keys.	A line is drawn as you press each key. When you press the third key the crosshair cursor disappears.
16. Press the PAGE key.	The screen is erased. The lines drawn while the inking feature was turned on are erased, since they are not part of a segment. Segment 1 is erased momentarily and redrawn.
17. Press the SET UP key.	The light in the SET UP and DIALOG keys turn on.
18. Enter the following commands: (ESC)<IC 0 1> (ESC)<IE 0 1>	The first command specifies that the next time the terminal enters GIN mode, segment 1 is to be the graphics cursor. The second command puts the terminal into GIN mode.
19. Press the SET UP key.	The lights in the SET UP and DIALOG keys turn off.
20. Rotate each of the thumbwheels.	Segment 1 is now the graphics cursor. As you rotate the top thumbwheel, it moves left and right; rotate the bottom the bottom thumbwheel to move it up and down.

21. Press an alphanumeric key.	The terminal exits from GIN mode.
22. Press the SET UP key.	The lights in the SET UP and DIALOG keys turn on.
23. Enter the following command: (ESC)<SK 1>	This command deletes segment 1 from the terminal's memory.
24. Press the SET UP key.	The lights in the SET UP and DIALOG keys turn off.
25. Press the DIALOG key.	The light in the key turns on and the dialog area becomes visible.

Section 4

INTRODUCTION TO CIRCUIT THEORY

INTRODUCTION

The 4114 circuitry is designed around a 16-bit microprocessor called the MPU. It has one megabyte of memory address space, which is addressed by the signals ADR0-19, and 32K bytes of IO address space, which is addressed by the signals ADR0-15. Separate read and write signals for memory space and IO space control the destination of the addresses on ADR0-15. The MPU responds to eight levels of interrupt priority by using the signals of Programmable Interrupt Controller integrated circuit. The MPU is also capable of direct memory access (DMA) operation.

The MPU communicates with two main sources of information. It receives keyboard data from and sends data and commands to a dedicated keyboard controller MPU. It also receives and sends data to and from the host computer by means of an RS-232 data communications link. The MPU acts upon commands received from the keyboard or host computer and accesses the proper firmware routine located either in ROM, on the Processor board or on the RAM/ROM board. The Display Controller and Vector Generator boards provide the signals necessary to control information displayed on the display module screen.

The Display Controller circuitry acts as an "interface" between the Processor and the Vector Generator boards. The Display Controller receives commands directly from the MPU, and also accesses commands from a display list located in main system memory. The Display Controller also controls the writing of data on the screen by controlling the Z Axis signal. The Vector Generator generates display signals that are sent to the display module through the display cable. The Vector Generator circuitry provides two functions. The set-up circuitry accepts display information from the Display Controller and passes this on to the Vector Generation circuitry. This circuitry creates the signals that operate the display module. The set-up circuitry also informs the display controller when to send more vector generation data.

SYSTEM BUS DESIGN

The system bus design allows control of the system bus to be gained and relinquished by "bus masters" and "bus slaves". At any one time, there is only one bus master, but, once the bus master is through with its operations on the bus, it gives up control of the bus to a bus slave, which then becomes the bus master. The current bus controller is the only device that can drive address lines and perform reads and writes. The Processor board and the Display Controller board are the only two potential bus masters in the standard 4114. However, the optional Disk Controller board is another potential bus master.

A bus slave is a device that obeys the bus master by sending data to the bus master during read operations and by accepting data from the bus master during write operations. The RAM/ROM and optional 3PPI boards are examples of bus slaves. When a bus master device, (for example, the optional Disk Controller board), does not have control of the bus, it may function as a bus slave. For instance, the Processor board, functioning as a bus master, may read from or write to IO registers on the Disk Controller board, which functions as a bus slave during this operation.

RELATED INFORMATION

The following sections of this manual contain the Theory of Operation for the major functional components of the 4114. In most cases the Theory of Operation is supplemented with simplified block diagrams, detailed block diagrams, and schematic references.

The major function blocks on each of the block diagrams is the same as the corresponding overlay block on the schematic diagram. The block diagrams therefore provide a functional overview of an entire circuit board which is not readily visible from the actual schematic diagrams.

The major module interconnect and block diagrams are also included in Section 12 of this manual and in Section 4 of Volume 2 for convenience and ease of cross referencing to the schematic diagrams.

Section 5

PROCESSOR AND KEYBOARD CIRCUIT THEORY

INTRODUCTION TO THE PROCESSOR BOARD

The Processor board consists of circuitry that performs the following functions:

- Processes system firmware commands and data along with interrupt data from on and off the board.
- Accepts interrupt signals from the host computer communications port, the keyboard, peripheral devices and other circuitry connected to the System bus, and from other circuitry on the Processor board itself.
- Transmits and receives data from the System bus.
- Stores part of the system firmware and the terminal initialization information.
- Provides control and status signals primarily for the microprocessor (MPU).
- Communicates with the host computer using the RS-232 communication standard.
- Communicates with the keyboard.

Each of these functions is performed by the blocks shown in the simplified block diagram of Figure 5-1.

MICROPROCESSOR (MPU)

This block consists of the microprocessor (MPU). This 16-bit machine time-multiplexes its AD0-AD19 lines: that is, at one time address information is on these lines; then later data information is on these lines. The MPU outputs three internal state identifiers (S0-S2), which are used by blocks of circuitry on the board to synchronize their operations with the MPU. Inputs to the block are primarily a clock, a reset, and an interrupt signal.

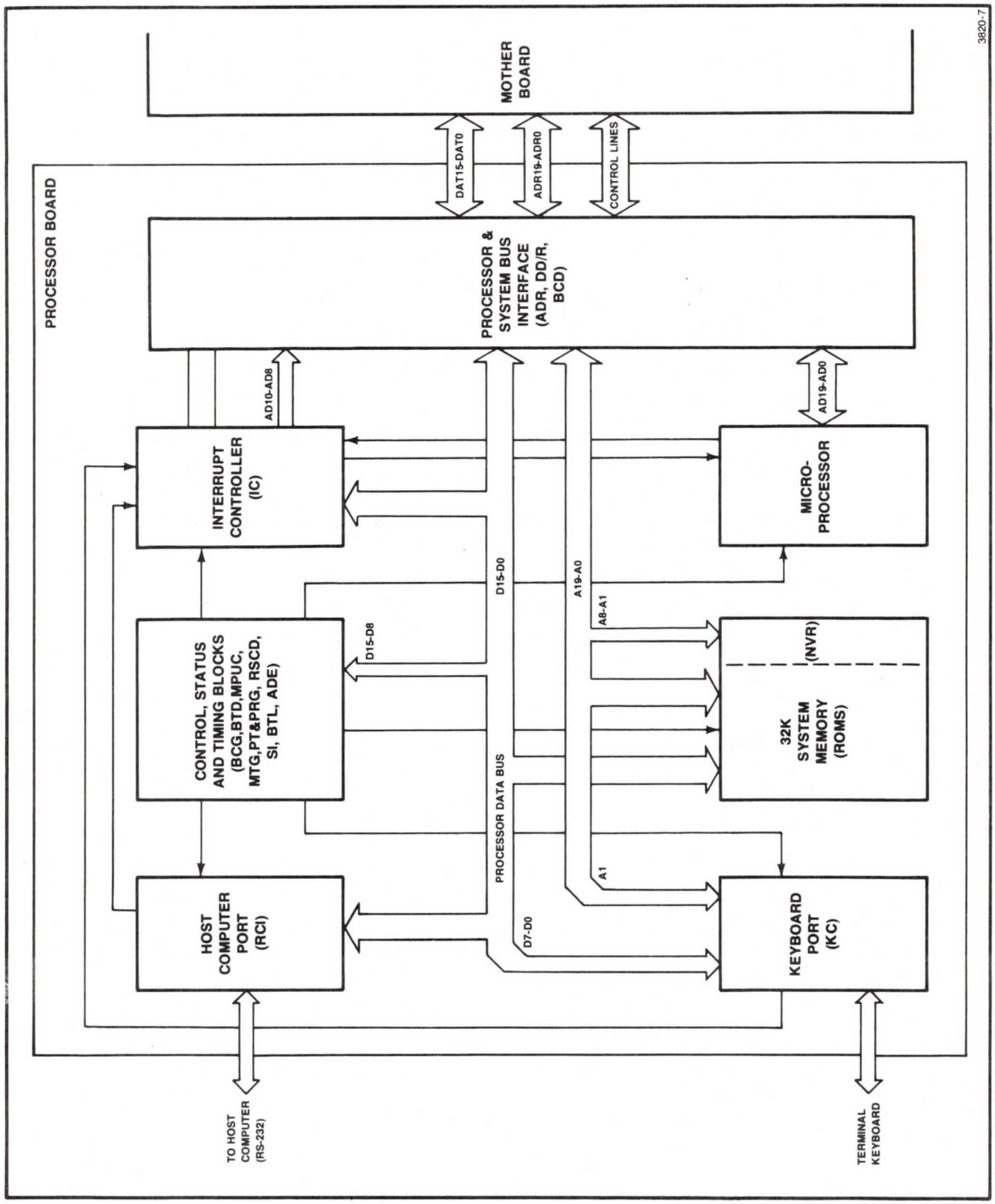


Figure 5-1. Simplified Block Diagram of Processor Board.

INTERRUPT CONTROLLER

The Interrupt Controller circuitry consists primarily of the Peripheral Interrupt Controller (PIC). This integrated circuit determines which one of eight interrupting sources is to be serviced if more than one source requests servicing at one time. Sources can be other boards in the terminal, such as the 3 Port Peripheral Interface (3PPI) board, or Processor board circuitry, such as the keyboard port or host computer port. The MPU communicates with the interrupt controller block through the Process data bus, D0-15. The PIC is programmed by the MPU shortly after the terminal is turned on. The MPU can also read the current status of the PIC and change its mode of operation by reprogramming its internal registers.

PROCESSOR AND SYSTEM BUS INTERFACE

The primary inputs to the Processor board and System Bus Interface circuitry are the lines on the multiplexed Processor address data bus (AD0-AD19), which is output directly from the MPU. The AD0-AD19 signal lines carry, at different times, data and address information. This block separates the data and address information into four distinct buses: D0-15 is the Processor data bus, A0-19 is the Processor address bus, DAT0-15 is the System data bus, and ADR0-19 is the System address bus. This block also outputs control and status signals onto the System bus.

SYSTEM MEMORY

There are approximately 32 thousand bytes of RAM in the System Memory circuitry that contains most of the basic system firmware. The Processor data and address buses connect to this block. Memory is addressed using the Processor address bus, and the selected data is placed on the Processor data bus. The System Memory also includes non-volatile RAM where set-up parameters are retained when the terminal power switch is off.

CONTROL, STATUS, AND TIMING

This circuitry consists of MPU control, status detection, and timing functions for the Processor board itself. The following blocks of circuitry are found on the schematics.

The MPU Control logic generates the 4.9152 MHz clock signal for the MPU. The block also synchronizes the reset and ready inputs of the MPU.

The Bus Transfer Logic provides signals that inform bus masters and slaves whether they can use the System bus. There is priority-determining logic on the Motherboard that works in conjunction with this circuitry.

The Address Decoding circuitry creates signals from high-order address bits which indicate what area of I/O or memory address space that data is to be sent or received.

The Bus Timeout Detector detects when a slave device fails to respond with an acknowlege signal (ACK1 or ACK2) to a command from any master device. If the circuitry does detect this failure to respond, it drives its own acknowledge signal (ACK1 or ACK2) onto the bus and sets an error status bit. This action prevents the bus from "hanging", that is, remaining in a state that cannot be responded to by any master or slave device.

The Status Input circuitry allows the MPU to read two Processor board status signals. This circuitry also outputs STATEN which is input to the Bus Timeout Detector.

The Bus Clock Generator produces a clock signal (BCLK) for the System bus.

The Microprocessor Timing Generator receives three signals from the MPU (S0-S2) that indicate whether the MPU is acknowledging an interrupt, reading or writing to IO or memory space, and fetching an instruction, in a halt state, or in a no-bus-cycle state. This information synchronizes operations both on and off the Processor board.

The Programmable Timer and Baud Rate Generator consists of a Progammable Interval Timer that primarily provides variable timing functions. This circuitry provides the transmit baud rate, a firmware interval timer, the bus timeout interval, and the RS-232 inter-character delay.

HOST COMPUTER PORT

The Host Computer Port circuitry communicates with the host computer by means of RS-232 signals. A programmable UART-type integrated circuit accepts RS-232 control and data signals from the host computer and then converts this information to parallel data and interrupts for use by the MPU. In addition to various control and status signals, the block outputs data on the Processor data bus, D0--D15.

Circuitry related to the host computer port is the RS-232 State Change Detector. This detects state changes on the incoming RS-232 status lines and generates interrupts if changes occur.

KEYBOARD PORT

The keyboard Port circuitry accepts data from the keyboard. The Peripheral Interface Microcomputer (PI MPU), dedicated to servicing the keyboard, processes this data and outputs it to part of the Processor data bus, D0-7. The PI MPU also outputs various control signals, including an interrupt (KBINT), which reaches the MPU after being processed by the Interrupt Controller circuitry.

DETAILED PROCESSOR BOARD CIRCUIT DESCRIPTIONS

Every block of circuitry that appears on the Processor board schematics is described here. For each block, the description follows the same format: Schematic number, Purpose, Signals -- input and output; Description, and Operation. The intent of this format is to give the reader a clear understanding of each block. Formatting also serves the purpose of quick reference once the circuitry is understood.

Refer to Figure 5-2 for an overall view of how the circuit blocks communicate. Note that the Address Drivers and Data Drivers/Receivers blocks perform analogous tasks for the address and data information that the MPU emits. They either output this information to the System bus or the Processor bus depending on the state of control signals from the MPU.

In the description of some blocks of circuitry, parentheses are used to enclose names that are not standard named signals. These names within parentheses are usually taken from the input or output pin name of an LSI circuit. Some examples are (CLK), (OSC), and (RDY) in the Microprocessor Control block.

Sometimes, in the spelled-out signal name that is enclosed in parentheses immediately after the signal name, there are parentheses inside parentheses. These inner parentheses enclose additional explanatory words that are not evident in the signal name. For example, in the Bus Transfer Logic circuitry, there is "BUSY ((System Bus) Busy)".

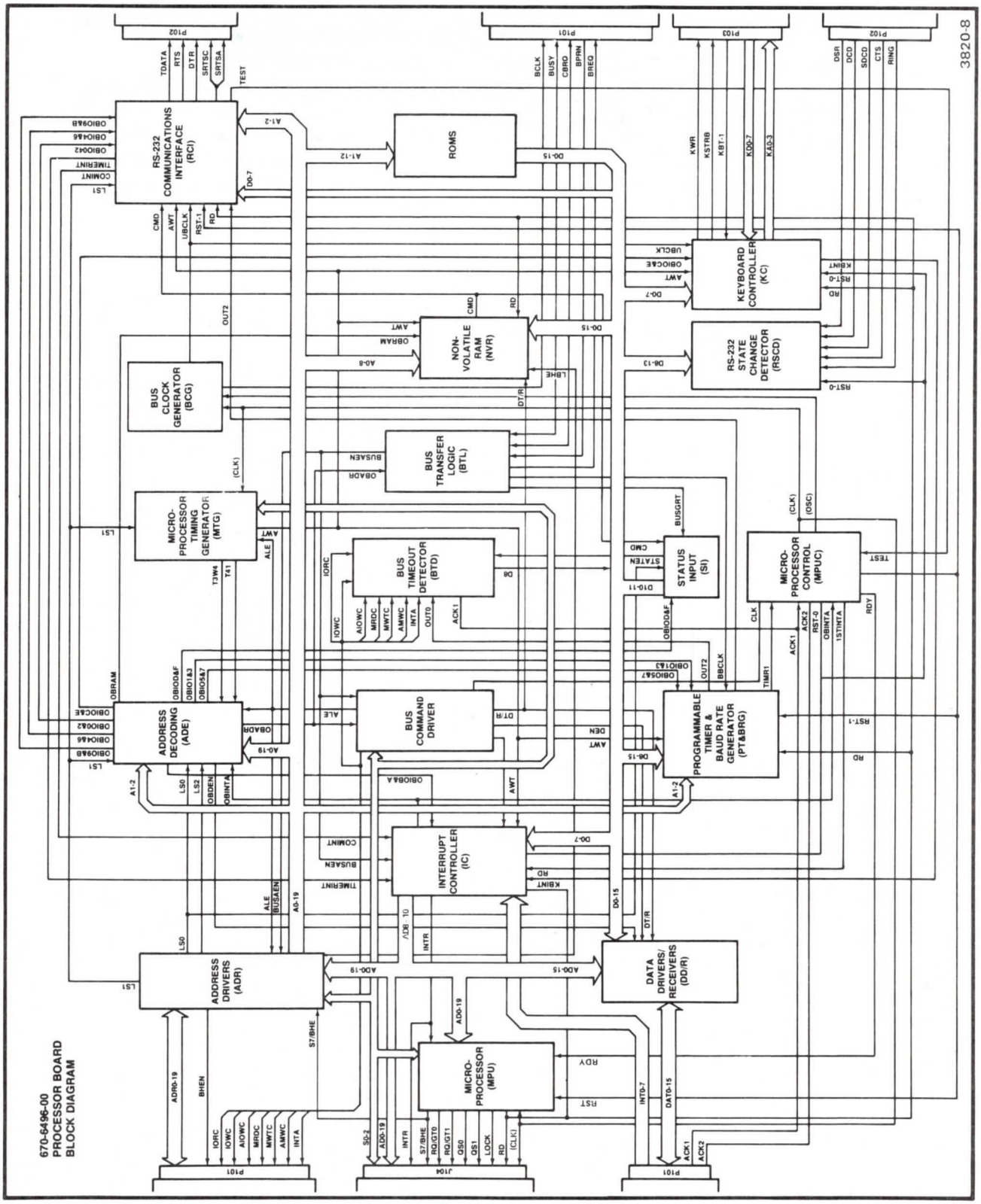


Figure 5-2. Processor Board Block Diagram.

Seven of the eighteen blocks have an LSI circuit as a main component. Many of these are programmable and all are multipurpose. The LSI circuits are used in a definite configuration (and in some cases a definite "mode") in the design of the Processor board. The block descriptions do not give complete accounts of the unused "modes" and configurations of these LSI circuits. However, reference to further information along with the abbreviations used for these LSI circuits is given in Table 5-1.

Table 5-1

MANUFACTURERS' NOMENCLATURE FOR ICS

Name	Abbrev.	Manufacturer's Number
Programmable Interrupt Controller	PIC	8259A **(a)**
Microprocessor	MPU	8086 **(a)**
Clock Generator and Driver	CGD	8284 **(a)**
Bus Controller	BC	8288 **(a)**
Keyboard Controller MPU	KC MPU	8041A **(a)**
Programmable Interval Timer	PIT	8253 **(a)**
Programmable Communications Interface	PCI	2661 **(b)**

(a) Description in Intel Component Data Catalog 1980
(b) Description in Signetics Data Manual 1980

MPU (SCHEMATIC A3-1) U45

Purpose

The MPU controls the general purpose reading and writing of data and address information for the entire terminal system. Sometimes the MPU gives up control of the System bus in favor of other bus masters.

Signals

The input signals are:

- CLK (Clock). Direct 4.9152 MHz clock signal from the Clock Generator. From U155
- RST (Reset). Directly input from the Clock Generator. Causes the MPU to stop current activity, but restarts execution when it goes high. RST must be low for at least four clock cycles to stop the MPU. From U155
- RDY (Ready). Directly input from the Clock Generator. When high, RDY signals that the addressed memory or I/O device will complete its data transfer. From U155
- TEST (Test). "Wait" instruction sets up the MPU to examine the TEST input. If TEST is low, execution continues. If TEST is high, the MPU inserts idle states between bus cycles until TEST goes low. This is available only on Test Connector J104. Pin 15
- NMI (Non-maskable interrupt). When low, the MPU stops normal execution and jumps to a predetermined subroutine in firmware. Software cannot disable this interrupt. NMI is triggered on the low to high transition. This is available only on Test Connector J104. Pin 6 & Pin 18
- INTR (Interrupt). When high, after the last clock cycle of the current instuction, the MPU enters an interrupt acknowledge operation. INTR may be disabled by software. U370

The output signals are:

- AD0-19 (Processor) Address Data bus bits 0 through 19). These bits carry both address and data information at different times. The Address Drivers circuitry outputs this information to the Processor bus or System bus according to its destination.
- LOCK (Lock). Prevents other bus masters from gaining control of the System bus. LOCK is activated when special "lock" prefixes are added to firmware instructions.
- RD (Read). When low, indicates that the MPU is performing a memory or I/O read cycle, depending on whether S2 is high (memory) or low (IO).
- QS0-1. Not used in normal operation, but available on the J104 test connector.
- RQ-0/GT0-1. Not used in normal operation, bus available on the J104 test connector.
- S0-2 (Status bits 0 through 2). These bits when taken together show which of eight states the MPU is in--interrupt acknowledge, I/O read, I/O write, halt, code access, memory read, I/O read, or passive.
- BHE (Byte High Enable). During MPU state T1, BHE enables the high byte of data onto D8-15 for read, write, and interrupt acknowledge cycles.

Description

The MPU is a general purpose microprocessor that has an address space of one megabyte. It operates at 4.9152 MHz and manipulates data in 8-bit or 16-bit word sizes. See Figure 5-3.

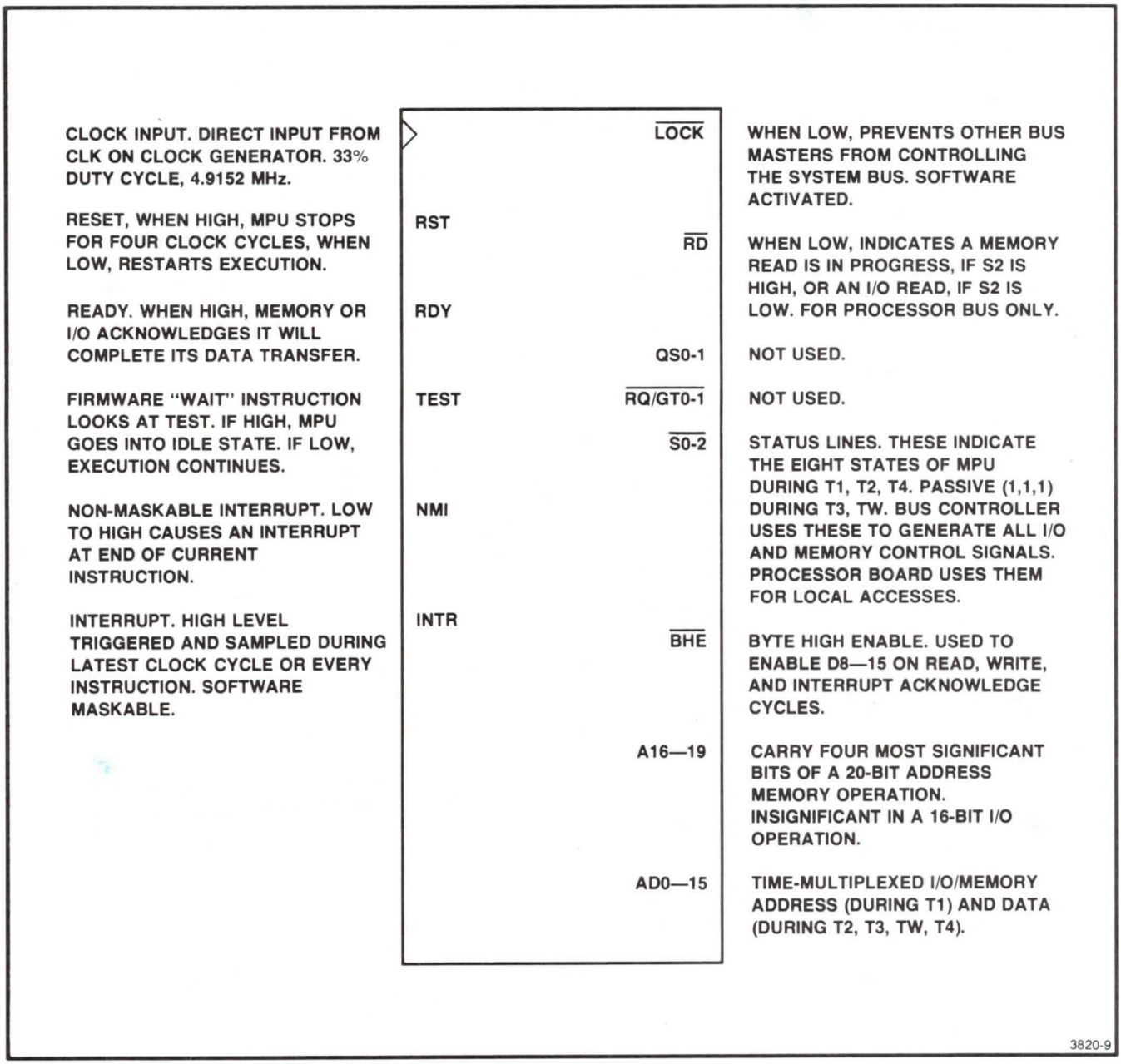


Figure 5-3. MPU Pin Descriptions.

The Bus Cycle

The MPU bus cycle consists of a variable number of clock states of approximately 200 ns each. The different kinds of clock states that can occur are T1, T2, T3, T4, Tw, and Ti. The minimum duration bus cycle is T1, T2, T3, and T4, in that order and one immediately after the other. However, some operations require that one or more clock states be inserted between T3 and T4. These states are Tw -- "wait" states. Also, sometimes states are inserted between bus cycles. These are Ti -- "idle" states. The MPU uses "idle" states for internal "housekeeping" operations.

MPU Internal States

During normal operation, the MPU performs one of eight types of bus cycles. These cycles are encoded in MPU outputs S0-2. The cycle that corresponds with each of the eight bit patterns of S0-2 is shown in Table 5-2, Status Word and Bus Controller Commands. This cylce status information is available during states T2, T3, and Tw. S0-2 become binary 111 (inactive) during T4 and last through any Ti states.

• Page 5-29

Operation

The major operations of the MPU are reading and writing to memory or I/O address space, reset and initialization, and interrupt operations.

Memory and I/O Adress Space Access

During T1, the MPU outputs an address. The MPU state information on S0-2 becomes available and the address is latched during T2. Also, during T2, if the operation is a read operation, the direction of the data bus is changed. Data is then read from or written to memory or I/O locations during T2, T3, and Tw. The information on S0-2 is used by different functional blocks of circuitry on the Processor board if the read or write access is local. Otherwise the S0-2 information is converted directly into the I/O and memory access commands for the System bus by the Command Driver.

Reset and Initialization

MPU reset occurs when (RST) from the Microprocessor Control circuitry goes high. It must stay high for at least four clock cycles. The MPU executes no operations as long as (RST) is high. When (RST) goes low, an internal reset sequence is triggered that lasts about ten clock cycles. After this, the MPU fetches the instruction in location H'FFFF0'. There must be at least 50 us between power up and the high to low transition of (RST).

Interrupt Operations

There are two hardware interrupts to the MPU--NMI and INTR. NMI is the non-maskable interrupt and INTR is the maskable interrupt request input.

Non-Maskable Interrupt. If NMI goes from low to high and stays high for more than two clock cycles, NMI is latched by the MPU and is serviced immediately after the current instruction is completed. NMI is only available on the Processor Board Test Fixture Connector and is not part of the System bus.

Maskable Interrupt. When INTR goes high during the clock cycle preceding the end of the current instruction, the MPU is triggered into a response sequence. The MPU executes two consecutive interrupt acknowledge cycles (=two bus cycles). (See Interrupt Controller description.) LOCK is held low from T2 of the first cycle to T2 of the second cycle. During the second bus cycle, a byte is fetched from the PIC. This byte specifies what source requires the interrupt and also addresses a location in ROM from which the appropriate interrupt service routine can be determined.

INTR can be disabled by resetting a status bit in the MPU by means of software instructions.

INTERRUPT CONTROLLER (SCHEMATIC A3-2)

Purpose

The Interrupt Controller handles a maximum of eight System bus and Processor board interrupt signals (INT0-7) and determines the priority of each interrupt signal in relation to the others. Also the Interrupt Controller has the capability of addressing eight other Programmable Interrupt Controllers.

Signals

The input signals are:

- COMINT (Communications Interrupt). Signals that the RS-232 Communications Interrupt has just received a character. W325A P-3
- TIMERINT (Timer Interrupt). Indicates that at least one of these signals is active: TIMR1, (TXEMT), (TXRDY), an RS-232 status change interrupt, or CUT0 (via RSCD). W470A P2
- AWT (Advanced Write). Advanced write signal for Processor board circuits. W101B P-6
- INT0-7 (Interrupt 0 to 7). System bus interrupt signals. (COMINT can generate INT0; KBDINT can generate INT4; and TIMERINT can generate INT5.)
- PUSAEN (Bus Address Enable). Shows that the MPU is bus master of the System bus.
- INTA (Interrupt Acknowledge). Causes the Programmable Interrupt Controller to place an interrupt routine address ("vectoring information") on the System data bus.
- OBIO8&A (On-board I/O 8&A). Enables the Programmable Interrupt Controller, when active low, for communication with the MPU.

- RD (Read). Read signal from the MPU.
- RST-0 (Reset active low). Initializes logic during power up and system reset.

The output signals are:

- AD8-10 (MPU Address-data bits 8-10). These carry the addresses of a maximum of eight other Programmable Interrupt Controllers.
- INTR (Interrupt). Interrupt signal to the MPU.
- 1STINTA (First Interrupt). Indicates to the MPU that no data will be transferred.
- OBINTA (On-board Interrupt). Indicates that the Programmable Interrupt Controller is placing data on D0-7. Also combines with other signals in the Address Decoding circuitry to produce OBDEN.

Description

The heart of the Interrupt Controller is the Programmable Interrupt Controller (PIC) integrated circuit. The PIC receives interrupt signals (INT0-7) and INTA from the System bus, control signals from other circuits on the board. It receives and transmits data from the Processor data bus, and it outputs INTR, OBINTA, and AD8-10 (which can carry addresses for eight other PIC's). The other circuitry in the Interrupt Controller inverts and buffers INT0-7, provides enabling for the AD8-10 drivers, and produces 1STINTA. Also, BUSAEN and INTA are ~~NANDed~~ for the INTA input of the PIC.

Actual logic: ORed

Programmable Interrupt Controller

This integrated circuit consists of five main blocks of circuitry. They are the local data bus buffer, the interrrupt registers and logic, the control logic, the read and write logic, and the cascade buffers and comparator. See Figure 5-4 and Figure 5-5.

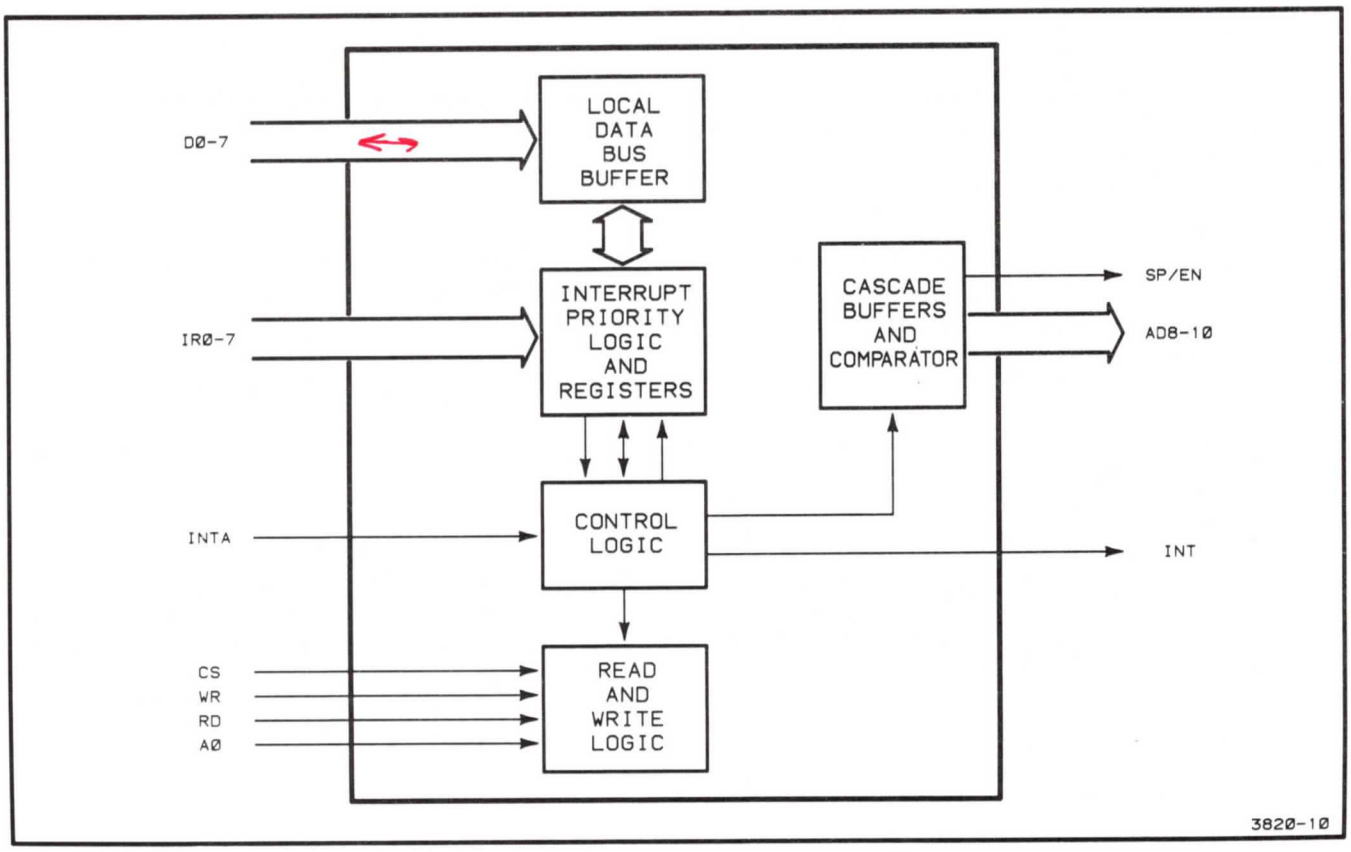


Figure 5-4. Programmable Interrupt Controller Block Diagram.

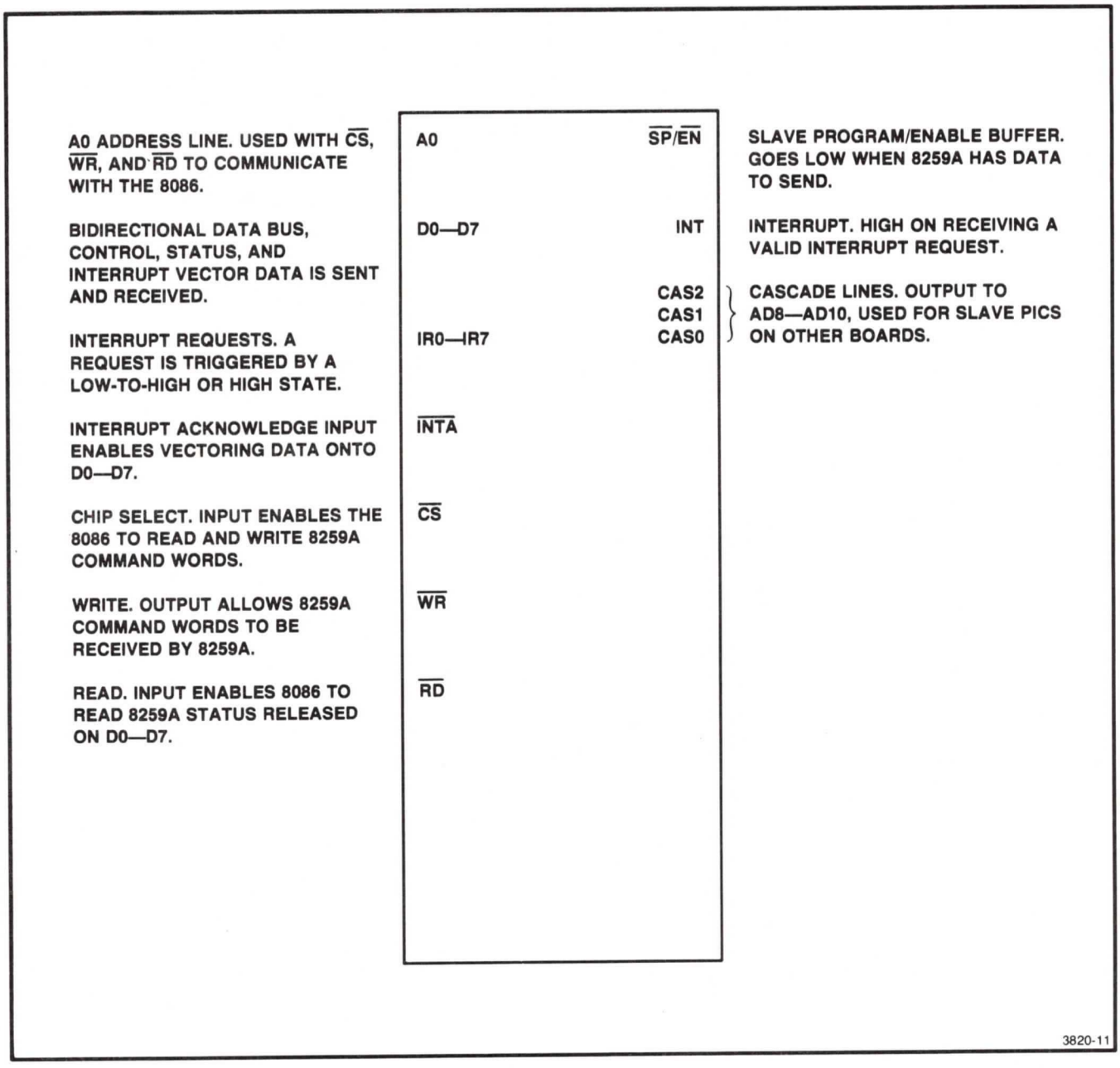


Figure 5-5. Programmable Interrupt Controller Pin Descriptions.

Local Data Bus Buffer. Eight bits, D0-7, are transmitted and received by this 3-state buffer. The system firmware supplies control words and status information to the PIC through this buffer. An internal bus connects the data bus buffer to the Interrupt Priority Logic Registers circuitry.

Interrupt Priority Logic and Registers. There are three registers in addition to the priority logic in this circuitry. The priority logic determines from the register holding INT0-7 bits (that are requesting service) which bit has the highest priority. This bit is strobed into the corresponding bit position in the "in-service" register. Firmware uses the third register to mask the INT0-7 bits in the "requesting service" register. This masking changes the priority of the INT0-7 interrupt signals.

Control Logic. When the system signal INTA goes active low, it causes the control logic to transmit interrupt service routine addresses to the System bus via the local data bus buffer. The control logic, also, issues INT to the MPU if it receives a signal from the priority logic.

Read and Write Logic. OBIO8&A goes active low to enable reading or writing access to the PIC. If RD goes active low, any of the three registers and the interrupt level of the Interrupt Priority Logic and Registers circuitry can be output to the Processor data bus. If AWT goes active low, firmware can write PIC control words to registers in the Read and Write Logic circuitry. A0 selects in conjunction with RD and AWT whether the interrupt registers or the command word registers are read from or written to.

Cascade Buffers and Comparator. If other PICs are added to the system, this circuitry addresses them. These "slave" PICs would be controlled by the "master" PIC on the Processor board. AD8-10 would carry the address of any one of eight additional PICs.

Operation

There are two phases of operation in the PIC. These are initialization and normal operation. During initialization, soon after the terminal is turned on, the system firmware sends PIC set-up data and control words to the PIC. After initialization, the PIC is ready to receive and prioritize the interrupt request signals on INT0-7.

The Interrupt Sequence

The following sequence of events occurs in the normal operation of the Interrupt Controller circuitry.

1. One or more of the INT0-7 bits goes active low. This sets (because of the inverter) the corresponding bit(s) in the "interrupt request" register in the Interrupt Priority Logic and Registers circuitry in the PIC.

2. The PIC determines the priority of these INT0-7 lines, and sends INT to the MPU if one of the INTs lines is a higher priority interrupt request than any currently being processed.

3. The MPU receives the INT signal and responds with a low on its INTA line.

4. The PIC now sets the highest priority bit in its "in-service" register and the corresponding "interrupt request" register bit is reset. No signals are sent from the PIC at this time.

5. Now the MPU sends a second low on INTA. This causes the PIC to place an eight-bit-interrupt-service routine ("vectoring") address on the Processor data bus, D0-7.

6. The MPU reads this "vectoring" address on the Processor data bus and begins the service routine. The Interrupt Controller is now done with this interrupt cycle.

If the duration of an interrupt request on INT0-7 is not long enough to be active low at step 4, the PIC automatically issues a "vectoring" address as if INT7 were active low.

1STINTA and Cascade Addresses for Slave PICs

During the interrupt sequence, the MPU sends two INTA signals. At the time of the first INTA, 1STINTA is generated by a toggling JK flip-flop and a negative logic NAND gate. At the time of the second INTA, the cascade address (AD8-10) of the slave PIC is driven onto the Processor address data bus. This is accomplished by the same toggling JK flip-flop and another NAND gate.

ADDRESS DRIVERS (SCHEMATIC A3-2)

Purpose

The Address Drivers latch 20 bits of address and BHEN, and then drive these onto the Processor address bus during a local read or write, or onto the System bus during a system read or write.

Signals

The input signals are:

- S0, S1, and S2 (Status 0, 1, & 2). Informs the Processor board whether the MPU is in an interrupt acknowledge, read IO, write IO, halt, code access, read memory, or write memory state. U45
- AD0-19 (Address and Data bits 0-19). Output directly from the MPU. AD0-19 carries both address and data information in time-multiplexed mode. U45
- BHE (Byte High Enable -- unbuffered). Directly from the MPU. U45 P5
- ALE (Address Latch Enable). Enables the local address latches. U560
- BUSAEN (Bus Address Enable). Enables the outputs of the system address latches. U275 P6

The output signals are:

- LS0, LS1, and LS2 (Latched Status 0, 1, & 2). Informs the system what internal state the MPU is in. See S0, S1, and S2. U150
- A0-19 (Processor address bus). Carries address information for the Processor board. U150 U250 U255
- ADR0-19 (System address bus). Carries address information for the system. U575 U565 U570
- LBHE (Latched Byte High Enable). Processor board equivalent of BHEN. U150

- BHEN (Byte High Enable). Enables DAT8-15 on read, write, or interrupt acknowledge cycles.

Operation

The Address Drivers circuitry consists of six packages of D-type latches. These form two sets of latches. One set outputs LS0-2, LBHE, and the Processor bus address bits. The other set outputs BHEN and the System bus address bits.

When the MPU outputs address information on AD0-19 and ALE makes a high-to-low transition, the "Processor bus" set latches this data. It also latches S0-2 and BHE. Since this set of latches is permanently enabled for output, the latched data appears immediately as A0-19, LS0-2, and LBHE.

The "System bus" set of latches operates like the "Processor bus" set, except that the latches are not permanently enabled for output. BUSAEN provides this enabling function.

DATA DRIVERS/RECEIVERS (SCHEMATIC A3-2)

Purpose

The Data Drivers/Receivers transfer MPU data on AD0-15 to or from either D0-15, the Processor data bus, or DAT0-15, the System data bus.

Signals

The input signals are:

- AD0-15 (Multiplexed address and data bits). Address and data bits directly output from the MPU.
- DT-1/R-0 (Data Transmit/Receive). Data bus direction control. U560 P-4
- DEN (Data Enable). U560 P-16
- SP-0/EN-0 (Enable Buffer). Enabling signal from the PIC. U 370 P-16
- OBDEN (On-board Data Enable).

The output signals are:

- D0-15 (Processor data bus bits). U350, U450
- DAT0-15 (System data bus bits). U550, U555

Operation

Four bus transceivers and one NAND gate make up the Data Drivers/Receivers circuitry. The bus transceivers are divided into two sets. One handles D0-15, the Processor data bus, and the other set handles DAT0-15, the System data bus. Data bits are transmitted and received in each set.

If OBDEN goes active low and DT/R-0 is high, the data bits on AD0-15 are transmitted to D0-15. But if OBDEN is low and DT-1/R-0 goes low, data on D0-15 is transmitted back through the transceivers and becomes AD0-15, which is received directly by the MPU.

Data is transmitted to the System data bus, DAT0-15 when DT-1/R-0 goes high and both DEN and SP-0/EN-0 are high. If DT-1/R-0 is low during data transmission, the System bus bits become AD0-15.

BUS COMMAND DRIVER (SCHEMATIC A3-2)

Purpose

The Bus Command Driver decodes MPU status signals in order to generate System bus read, write, and interrupt commands. Also, the Bus Command Driver generates control signals for the Processor board address and data drivers and latches.

Signals

The input signals are:

- S0-2 (Status 0-2). Three lines that indicate what type of cycle the MPU is performing--I/O read, I/O write, memory read, memory write, halt, or interrupt acknowledge.
- BUSAEN (Bus Address Enable). Shows that the MPU is System bus master, when active low.
- OBADR (On-board Address). When low, indicates that the Processor board circuitry is being accessed. When high, indicates that the System bus is being accessed.
- CLK (Clock). Synchronizing clock signal for the Processor board.

The output signals are:

- DT/R (Data Transmit/Receive). Processor and System data bus transmit and receive. P-4
- ALE (Address Latch Enable). Enables the Processor and System bus address latches. P-5
- (MCE) (Master Cascade Enable). Clocks a JK flip-flop (in the Interrupt Controller circuitry) that enables three line drivers to output AD8-10 (an address for one of eight optional Interrupt Controllers). P-17

- (DEN) (Data Enable). Enables system data drivers if OBINTA is inactive high. P-16
- INTA (Interrupt Acknowledge). Signals the Interrupt Controller to place vectoring data on the System data bus. P-14
- IOWC (I/O Write Command). P-11
- AIOWC (Advanced I/O Write Command). P-12
- IORC (I/O Read Command). P-13
- MRDC (Memory Read Command). P-7
- MWTC (Memory Write Command). P-9
- AMWC (Advanced Memory Write Command). P-8

Operation

The Bus Command Driver circuitry consists solely of the Bus Controller. This device combines control logic, MPU status decoder, control signal generator, and Command Generator circuitry. Figure 5-6 shows the signal paths among these blocks of circuitry. See also Figure 5-7.

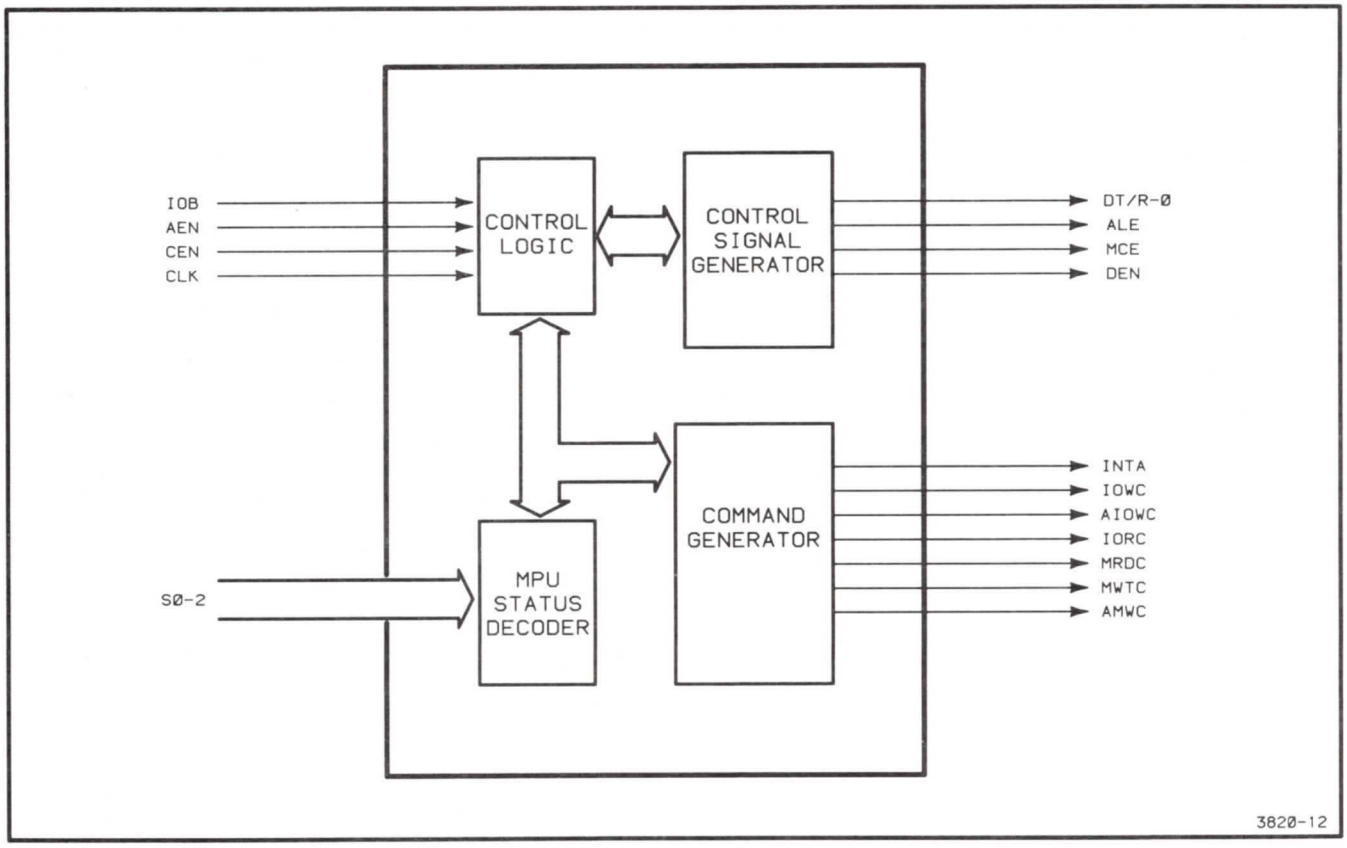


Figure 5-6. Bus Controller Block Diagram.

Control Logic

IOB is permanently tied low. This sets up the control logic so that it enables the command generator to output command signals (AIOWC, MWTC, MRDC, etc.) no sooner than 105 ns after BUSAEN goes active low. When BUSAEN is high, the control logic 3-states (places in a high impedance condition) the command signal outputs.

OBADR also affects command signal output. When OBADR is active low, all command signal outputs in addition to the DEN and MCE outputs are inactive. If OBADR goes inactive high, these same outputs are enabled.

CLK synchronizes the operations within the Bus Controller.

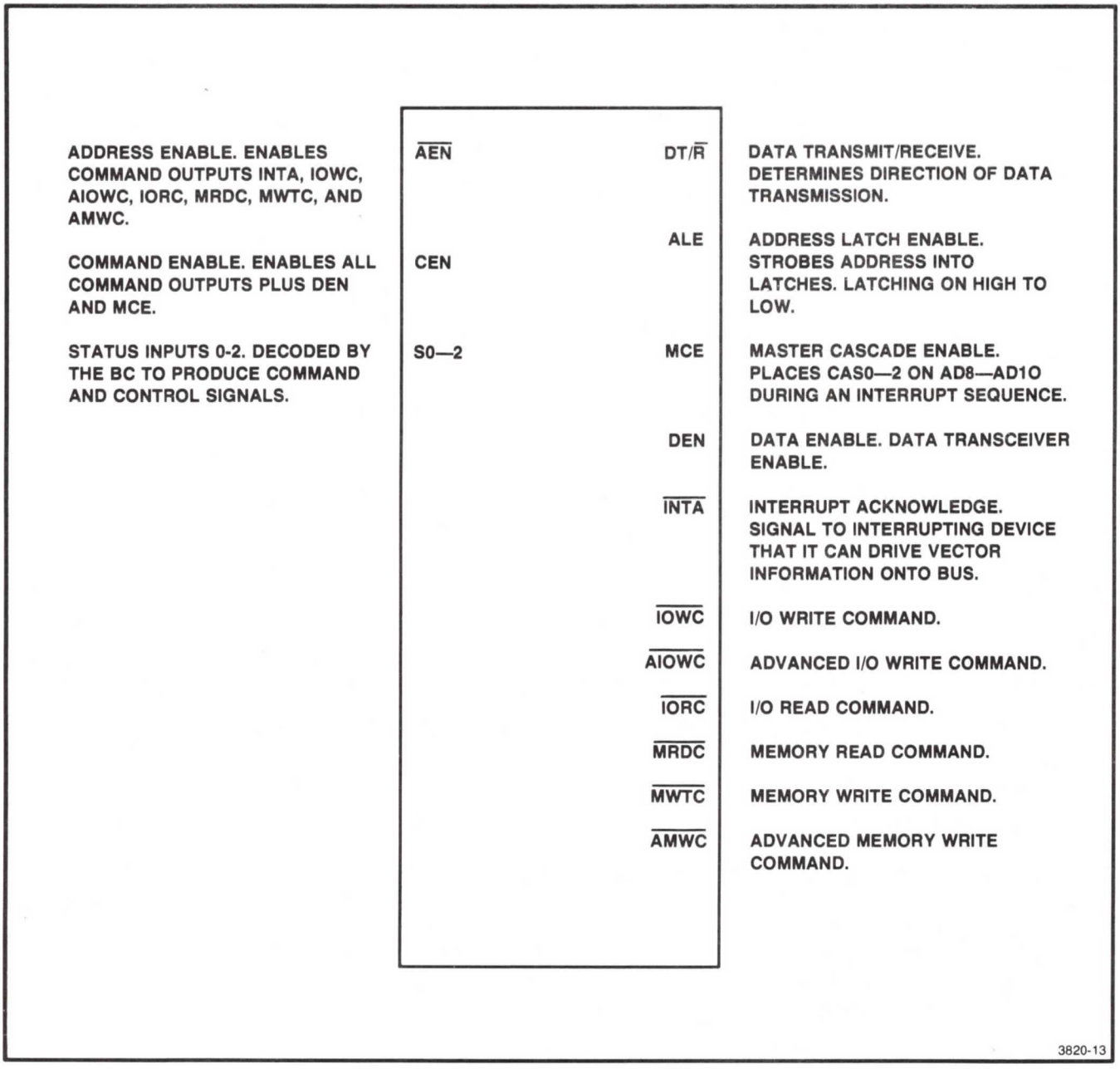


Figure 5-7. Bus Controller Pin Descriptions.

Control Signal Generator

This part of the Bus Controller outputs DT/R, ALE, MCE, and DEN. These signals control, respectively, direction of data transmission, enabling of the address latches, enabling of AD8-10 (additional Interrupt Controller addresses), and enabling of system bus data drivers if OBINTA is high.

When BUSAEN is low (MPU is bus master) and OBADR is high (MPU is not accessing a device on the Processor board), the Control Signal Generator actives its control outputs according to whether S0-2 indicate a read, write, or interrupt cycle. See Figure 5-8 for the sequencing of these signals.

MPU Status Decoder

This circuitry decodes the S0-2 signals from the MPU. These lines indicate the eight different states that the MPU can be in. Table 5-2 shows for each bit combination what MPU state corresponds to it. It also shows the corresponding command signal for each bit combination. These command signals are output only when the corresponding S0-2 bit combination is present.

Table 5-2

STATUS WORD AND BUS CONTROLLER COMMANDS

S0	S1	S2	Processor State	Bus Controller Command
0	0	0	Interrupt Ack.	INTA
1	0	0	Read I/O Port	IORC
0	1	0	Write I/O Port	IOWC, AIOWC
1	1	0	Halt	none
0	0	1	Code Access	MRDC
1	0	1	Read Memory	MRDC
0	1	1	Write Memory	MWTC, AMWC
1	1	1	Inactive	none

NOTES: These notes 1-3 and A-V appear in Figure 5-8.

1. When this line is low, it indicates that one or more of the status lines (S0, S1, or S2) is low.

2. AD0-19 are not used by the Bus Controller, but are drawn to show their relationship to ALE (Address Latch Enable).

3. MCE (Master Cascade Enable) occurs only when all three status lines are low. This signals the Interrupt Acknowledge cycle.

This diagram shows five different cycle types--memory read, memory write, IO read, IO write, and interrupt acknowledge. Only one type can occur at any one time.

A,B,C,D When the MPU drives at least one status line low (S0-2), and CLK is low, the Bus Controller generates ALE and, during an interrupt acknowledge (INTA) cycle, MCE to strobe the address latches.

E,F,G ALE is removed and the data direction is switched on write commands.

H,I,J,K MCE is removed, commands are driven onto the bus, and writing of data is enabled on a write command.

L,M Reading of data is enabled on read or INTA cycles.

N,O A write command is initiated on memory and IO write cycles. Note that the advanced write line (AIOWC and AMWC) is already true.

P,Q,R,S All commands are moved and the reading of data is disabled.

T,U,V Writing of data is diabled and data reverts back to the MPU output in anticipation of the MPU address output for the next cycle.

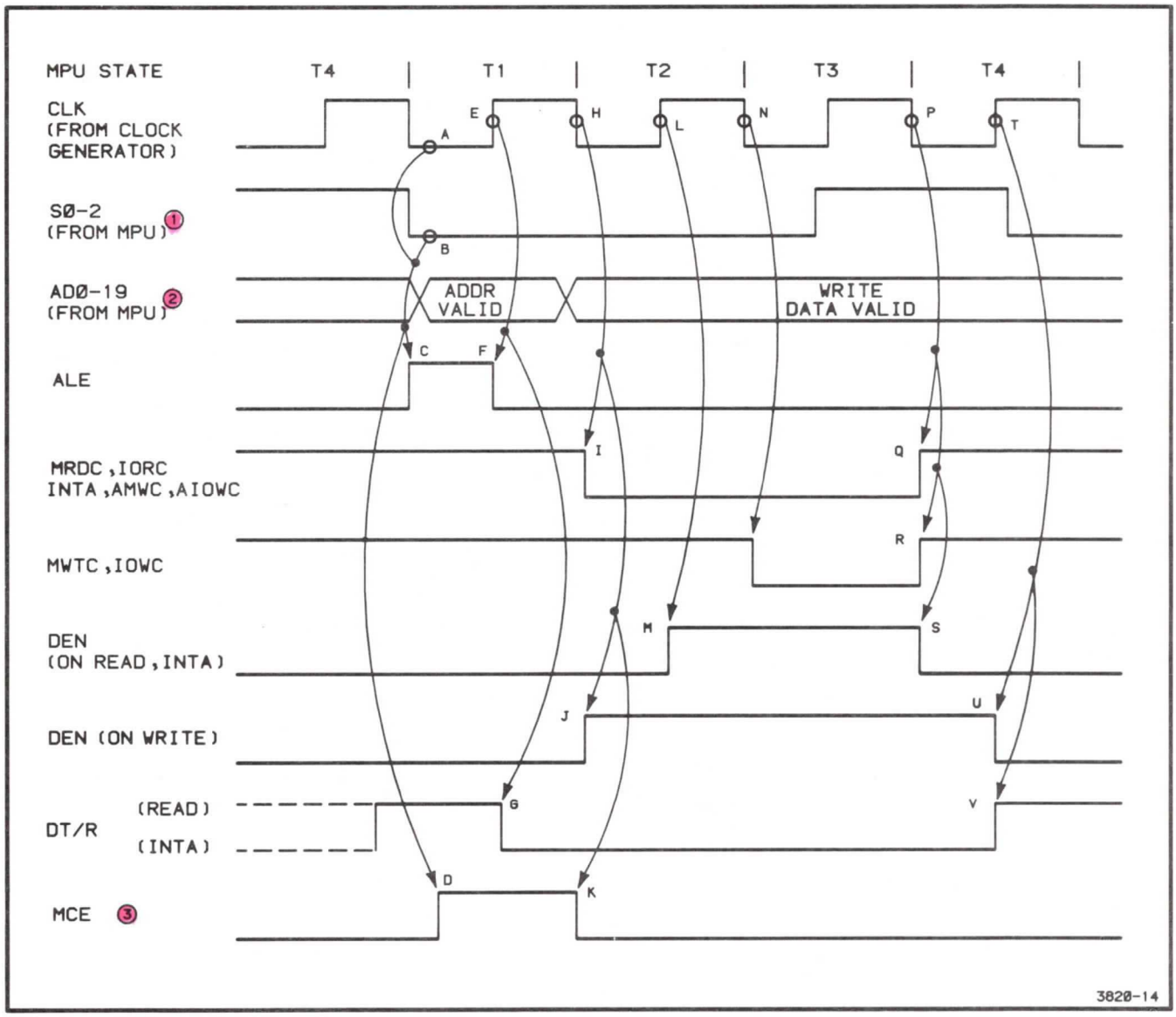


Figure 5-8. Bus Controller Timing.

Command Generator

This circuitry outputs the command signals -- MRDC, MWTC, IORC, IOWC, AMWC, AIOWC, and INTA. When BUSAEN is active low and OBADR is inactive high, the Command Generator outputs the command signals corresponding to the three bits of S0-2. See Table 5-2, Status Words and Bus Controller Commands, for this correspondence.

ROMS (SCHEMATIC A3-3)

Purpose

ROMs holds a maximum of 32K bytes of system firmware and outputs this to the Processor bus when it is addressed.

Signals

The input signals are:

- A1-14 (Processor Address bits 1 through 14). A1-14 carry word addresses (A1-11) and ROM bank selection information (A12-14).
- ALE (Address Latch Enable). ALE is used to disable the ROMs when the address is changing.
- LS1 (Latched Status bit 1). LS1 is a read/write status bit and is used to enable the ROMs during a read operation.

The output signals are:

- D0-15 (Processor Data bits 0 through 15). These bits carry data information for the MPU.

Description

ROM Configuration

The ROMS circuitry is made up of eight ROM integrated circuits, arranged in four banks of two ROMs each. The four banks supply a total of 32K bytes. Each bank contains 4K by 16 bits of memory address space. The bottom half of each bank outputs D0-7 and the top half outputs D8-15.

Firmware

Starting from the leftmost bank on the schematic, the first three banks contain system firmware in masked ROMs or EPROMs. The fourth bank contains a firmware "jump table" and "patch code" in erasable/ programmable ROMs (EPROMs).

Straps

There are three kinds of straps that affect the operation of the ROMs circuitry -- ROM-type selection jumper straps, a ROM wait-states cut strap, and two ROM address-decoding cut straps.

The ROMS circuitry is designed to accept a variety of different ROM integrated circuit packages. A chart specifying these different ROM types is found on the schematic itself (Schematic A3-3). The chart also specifies the strap positions required for each type of ROM.

Cut strap W475 selects the number of ROM wait states that the MPU inserts between state T3 and T4. If the strap is not altered, the MPU inserts one wait state. This allows the use of ROMs with chip select access time of up to 580 ns. However, if all the ROMs on the Processor board have an access time of 380 ns or less, strap W475 may be altered so that the MPU inserts no wait-states between T3 and T4. This latter position increases the speed of the MPU when executing on-board ROM firmware.

The straps at W126 allow some or all of the ROMS memory address space to be diverted from being used locally on the Processor board to being used by the system. There are three positions for the straps. See the appendix on straps to determine the settings for each of the three positions. If the straps are not altered, all 32K bytes of the Processor board ROMs are addressed in the range X'F8000' to X'FFFFF'. However, the straps may be altered to two positions. In one position, only Processor board ROMs addressed in the range X'FC000' to X'FFFFF' output data to the MPU. In the other position, there is no Processor board ROM space -- all memory space is accessed on the System bus.

Operation

The ROMS circuitry receives an address from the MPU and puts the data for that address on the Processor bus. The sequence of events when the MPU reads from a ROM bank is the following.

1. An address from the MPU is latched by the Address Driver circuitry.

2. The Address Decoding circuitry determines whether it is a Processor board ROM address, which is normally any address in the range X'F8000' to X'FFFFF'. If the address is in this range, Address Decoding drives OBROM active low.

3. The bank decoder selects one ROM bank in response to A13 and A14 in addition to ALE, LS1, LS2, and A15-19. See Figure 5-9, ROMS Bank Decoder Logic and Table 5-3, Selection Bits for ROM Banks for an exact description of how the bank decoder works.

4. The two ROMs in the selected ROM bank place their data on the Processor data bus lines, D0-15.

5. The Data Drivers/Receivers pass this data on to the MPU.

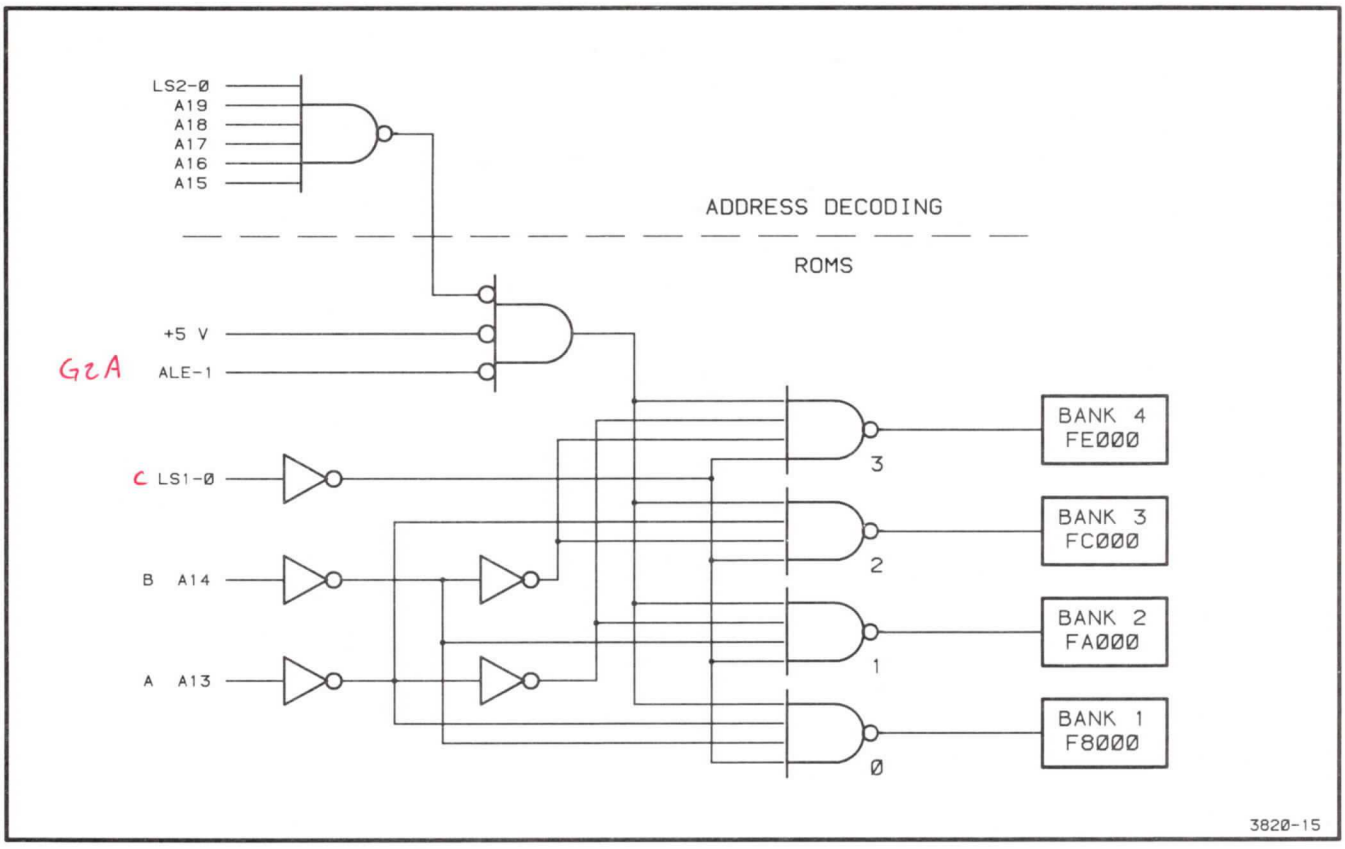


Figure 5-9. ROMs Bank Decoder Logic.

Table 5-3

SELECTION BITS FOR ROM BANKS

	Address Bits							
Banks	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**
F8000	1	1	1	1	1	0	0	X
FA000	1	1	1	1	1	0	1	X
FC000	1	1	1	1	1	1	0	X
FE000	1	1	1	1	1	1	1	X

"X" is the "don't care" condition.

NON-VOLATILE RAM (SCHEMATIC A3-4)

Purpose

The Non-Vollatile RAM stores various initialization and system parameters in 512 bytes of CMOS RAM.

Signals

The input signals are:

- RD (Read). Allows the MPU to read from the CMOS RAM.
- A0-8 (Processor address bits 0-8).
- LBHE (Latched Byte High Enable). Allows the MPU to access data bits D8-15.
- AWT (Advanced Write). Allows the MPU to write to the CMOS RAM.
- DT/R (Data Transmit or Receive) Causes the CMOS RAM to accept data when high, and to output data when low.
- OBRAM (On-board RAM). When RAM on the Processor board is addressed, OBRAM goes active low.

The output signals are:

- D0-15 (Processor data bus bits 0-15).
- CMD (Command). Created in the Non-volatile RAM circuit block by the logical OR of AWT and RD.

Description and Operation

Four 256 by 4 CMOS RAMs combine to give a total memory capacity of 512 bytes. Also included in this circuitry are six logic gates that decode various input signals that control reading and writing access.

When power to the terminal is shut off, this CMOS RAM retains its contents. A 2.4 V rechargeable NiCad battery provides the trickle current to do this.

Read Access

This RAM occupies X'FE00' to X'FFFF' in I/O address space. (See the Address Decoding description to see how CMOS can be placed in memory address space.) When the MPU presents an address in this range to the Address Decoding circuitry, OBRAM goes active low. The MPU also outputs RD active low. At this point, A0 is active low, if only the low order byte, D0-7, of the Processor data bus is needed. These conditions on OBRAM, RD, and A0 enable the two RAMs that output D0-7. Now DT/R goes active low, and the RAMs output D0-7 onto the Processor data bus.

A read access of the high order byte, D8-15, is accomplished the same way as the low order byte, except that LBHE goes active low.

Write Access

During a write access, AWT goes active low instead of RD and DT/R goes active high. OBRAM, LBHE, and A0 operate as they do in a read access.

Note that INIT disables all RAMs if it goes active low.

MICROPROCESSOR CONTROL (SCHEMATIC A3-1)

Purpose

The Microprocessor Control generates the 4.9152 MHz clock signal for the MPU. Also, it synchronizes the reset and ready lines.

Signals

The input signals are:

- INIT (Initialize). Used by the Clock Generator to generate (RST) for the MPU. Originates on the System bus.
- ACK1 (Acknowledge 1). When low, indicates that a device on the System data bus is ready to receive data or has data ready to transmit.
- ACK2 (Acknowledge 2). Has the same meaning as ACK1, but allows the MPU to insert one wait state (Tw) into the bus cycle.
- TIMR1 (Timer 1). A timer output from the Programmable Timer & Baud Rate Generator circuitry. Used for testing.
- TEST (Test). Enables the MPU to terminate an on-board or off-board read or write operation.
- RDYAND (Ready AND). Disables the (RDY) line to the MPU and causes the MPU to enter a wait state (Tw). Used for testing.
- RDYOR (Ready OR). Enables the (RDY) line to the MPU and causes the MPU to exit a wait state (Tw). Used for testing.
- 1STINTA (First Interrupt Acknowledge). Goes active low when the MPU sends the first of its two INTA signals in the interrupt sequence.

- OBINTA (On-board Interrupt Acknowledge). When active low, indicates that the PIC is placing data on the Processor data bus.

- OBROM (On-board ROM). May cause (RDY1) to activate if the cut strap W475 is altered, resulting in no ROM wait-states.

The output signals are:

- (OSC). TTL level, 14.7456 MHz square wave.

- (CLK). 4.9152 MHz, 33% duty cycle clock signal which is fed to MPU.

- (RST). Resets the MPU when high and has similar timing to INIT.

- (RDY). When high, acknowledges that an addressed memory or I/O device will complete its data transfer.

Description

This circuitry consists of one D-type flip-flop, some logic gates, and the Clock Generator and Driver integrated circuit (CGD). The CGD performs three functions. It uses a frequency derived from an external crystal to generate the (CLK) and (OSC) outputs. It synchronizes INIT to produce (RST). And it derives the (RDY) output from (RDY1) and (AEN1) or from (RDY2) and (AEN2). See Figure 5-10.

The crystal connected between (X1) and (X2) on the CGD is a series resonant, fundamental mode, type and has a frequency of 14.7456 MHz. The output of the oscillator circuitry in the CGD is buffered and output on (OSC). The (F/C) input is strapped low to select the crystal as the source of the (CLK) output frequency. Hardwiring (CSYNC) to ground is necessary to use the internal oscillator of the CGD.

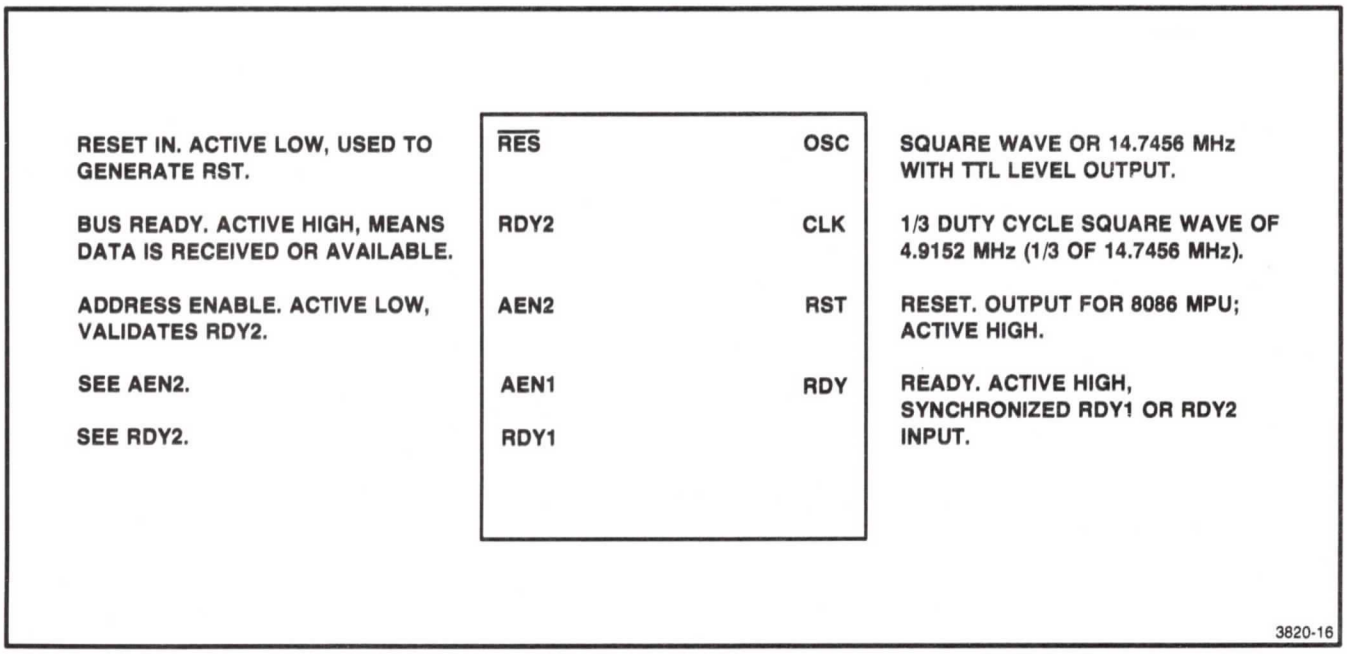


Figure 5-10. Clock Generator and Driver Pin Descriptions.

The CGD reduces noise on the INIT signal by feeding it through a Schmitt trigger and then synchronizes it with (CLK) by means of a flip-flop.

Inside the CGD, (AEN1) is inverted and ANDed with (RDY1) as is (AEN2) with (RDY2). The outputs of both ANDed pairs are ORRed and synchronized with (CLK) by a D-type flip-flop. The Q output of the flip-flop is (RDY). So, if (AEN1) is low and (RDY1) is high, (RDY) goes active high. The same is true of (AEN2) and (RDY2).

Operation

Clock and Reset

When the terminal is powered up, the CGD begins operation and generates the (OSC) and (CLK) signals until the terminal is turned off.

INIT and PFAIL, both originating in the power supply, are initially low after power up. PFAIL goes high soon after power up, and this is followed by INIT after about 40 ms. Then, at the next falling edge of (CLK), the (RST) output of the CGD goes high, resetting the MPU.

Ready Signals

Essentially, (AEN1) and (RDY1) are the Processor board ready signals and (AEN2) and (RDY2) are the "off-board" or System bus ready signals. The (AEN) signals act as qualifying or validating signals for the (RDY), bus ready, signals.

Processor Board Ready. The MPU receives a (RDY) input if any of the following conditions occur:

- RDYAND stays high and OBINTA goes low,
- RDYAND stays high and 1STINTA goes low,
- RDYAND stays high and, if cut strap W475 is altered, OBROM goes low,
- RDYAND stays high and OBADR is low while T3W4 goes high,
- RDYAND stays high and TEST, TIMR1, and T3W4 all go high, or
- RDYAND stays high and RDYOR goes low.

However, if RDYAND goes low all the above conditions are disabled and the MPU does not receive a (RDY) input.

System Bus Ready. For the MPU to receive a (RDY) input from the System bus, the (AEN2) input must be low. This occurs under the following conditions: RDYAND is high and BUSAEN is low, and at least one of the following is active low--INTA, AIOWC, IORC, MRDC, or AMWC. Once (AEN2) is active low, an ACK1 going low triggers a (RDY) input to the MPU. Or, if the device sends ACK2 signals instead, the MPU receives a (RDY) input on the next positive edge of the (CLK) signal after ACK2 goes low.

BUS TRANSFER LOGIC (SCHEMATIC A3-1)

Purpose

Bus Transfer Logic allows the Processor board to gain control of the System bus to perform data transfers, and also to relinquish control up to other bus masters.

Signals

The input signals are:

- T4I ((State) T4 and Idle). Used here to signal when the MPU leaves state T4 or the idle state.
- OBADR (On-board Address). Used here in its inactive state, which shows that a system data transfer is to be done.
- BUSY ((System Bus) Busy). When active low, BUSY indicates that another bus master is using the System bus for data transfer.
- CBRQ (Common Bus Request). CBRQ is used by a lower priority bus master to assert that it has data to transfer on the bus.
- BUSGRT (Bus Grant). Used to force Processor board control of the System bus for testing.
- BCLK (Bus Clock). BCLK clocks all three flip-flops in this circuitry.
- BPRN (Bus Priority In). The response from bus arbitration logic which grants bus mastership to the Processor board.
- LOCK (Lock). LOCK is a firmware-initiated signal, directly from the MPU, that prevents BUSY from going high so that no other bus masters can gain control of the bus.

The output signals are:

- BRQ (Bus Request). BRQ is active low, and is immediately decoded according to the priority of the Motherboard slot into which the Processor board is inserted. BPRN goes active low if no higher priority BRQ signal is asserted at the time the Processor board BRQ is asserted.

- CBRQ. (See the input signals.)

- BUSGRT. Indicates that the Processor board has control of the bus when active high.

- BUSY. (See the input signals.)

- BUSAEN (Bus Address Enable). BUSAEN triggers the Bus Command Driver to output read and write signals on the System bus. It also enables the System bus address drivers.

Description

The Bus Transfer Logic enables the Processor board to respond to the bus transfer protocol that all potential bus masters on the System bus must obey. (See the description of bus transfer protocol in Section 4.) The Processor board is just one system device that can control the System bus. The Processor board, along with the 4114 Display Controller and Disk Controller boards, can be "bus masters" of the System bus.

There are three JK flip-flops whose Q or Q-not outputs are the main output signals of this circuitry. (For the purpose of this description, these flip-flops are called the BRQ, BUSAEN, and BUSY flip-flops according to their Q or Q-not outputs.)

Note that three signals, CBRQ, BUSGRT, and BUSY, are both inputs and outputs of this circuitry. This circumstance is made necessary by the bus transfer protocol.

End-of-Data-Transfer Strap

Strap W455 in the Microprocessor Timing Generator selects one of two signals that indicate the end of a current MPU data transfer. W455 should be strapped to pins 2 and 3 only in a multi-processor board system where the MPU is not the microprocessor supplying the bus clock signal. (Note that strap W456 should be open if the MPU is not supplying the bus clock signal.)

Operation

When the MPU begins a memory, IO, or interrupt cycle, the Address Decoding circuitry drives OBADR low if the cycle is transferring data on the Processor board's internal bus. Since the MPU is not accessing the System bus, BRQ goes or stays inactive high.

However, if OBADR is driven high, BRQ goes active low and the bus transfer logic is activated. At this point the MPU is in one of two states; it either controls or does not control the System bus. If it controls the bus, then, according to the protocol, the MPU has already caused BUSY to go active low and it proceeds with its data transfer immediately, since it is currently bus master.

However, if the MPU does not currently control the bus, the following sequence of events occurs:

1. The BRQ flip-flop toggles high and drives BRQ and CBRQ both active low onto the bus.

2. When BUSY goes inactive high (bus is available) and BPRN goes active low (bus is granted to Processor board), the Bus Transfer Logic makes BUSGRT-0 active high, and BUSY active low (bus is busy and unavailable).

3. At the same time the BUSAEN flip-flop is preset by BUSY. This enables the bus controller to begin driving control signals onto the System bus.

4. BUSY remains active low until the MPU is finished transferring data. Then BUSY goes inactive high if BPRN is inactive high. There are two ways to cause BPRN to go inactive high: 1) A higher priority bus master requests bus control by driving its BRQ signal active low. If this happens, the bus priority logic on the Motherboard causes the BPRN of the Processor board to go inactive high; 2) A lower priority bus master requests bus control by making its CBRQ go active high. This causes the BRQ flip-flop to be reset to 0, which makes BRQ go inactive high due to the inverter. Thus, the Processor board no longer requests the System bus.

If no other bus master requests the bus, the Processor board maintains control. This eliminates the time delay that would be caused by having to get control of the bus for every data transfer.

ADDRESS DECODING (SCHEMATIC A3-3)

Purpose

Address Decoding decodes an MPU address, consisting of A4-19, to determine which Processor board circuitry (or the System Bus) is currently being addressed.

Signals

The input signals are:

- MDEN (Master Data Enable). Disables all MPU data drivers, when active low. MDEN is used for testing.
- T3W4 ((State) T3 Wait 4). When high, indicates that the MPU is in state T3, T4, or Tw (WAIT). T3W4 enables on-board data transceivers.
- T4I ((State) T4 Idle). Low during the MPU T4 and TI (IDLE) states. It turns off the data transceivers during T4 in on-board memory and I/O reads.
- OBINTA (On-Board Interrupt Acknowledge). When active low, indicates that the Priority Interrupt Controller is generating an interrupt vector address.
- LS0-2 (Latched Status 0 through 2). When taken together, these signals indicate which of eight states the MPU is in -- interrupt acknowledge, I/O read, I/O write, halt, instruction fetch, memory read, memory write, or no bus cycle.
- A4-7 and A9-19. (Processor address bus bits). These address the different parts of Processor board circuitry.

The output signals are:

- OBDEN (On-Board Data Enable). Enables the data transceivers so that Processor board data is put on the Processor data bus lines, D0-15.

- OBADR (On-Board Address). When low, it disables the Bus Command Driver circuitry. No read, write, or interrupt signals are output to the System Bus. The MPU is accessing circuitry only on the Processor board when OBADR is low.

- OBRAM (On-Board RAM). In conjuction with LBHE, A0, and INIT, OBRAM enables the CMOS RAMs in the Non-volative RAM block.

- OBROM (On-Board ROM). When true low, OBROM enables the 32K of ROM on the Processor board. If fast ROMs are used, OBROM may be strapped to enable the MPU to insert no WAIT states in its ROM access cycles.

- OBIOX&X. (On-Board (two byte) Input/Output locations). These eight signals basically act, sometimes in conjunction with other signals, as enabling signals for two-byte I/O space locations on the Processor board. For example, OBIO0&2 and OBIO4&6 together with CMD are chip enables for the PCI in the RS232 Communications circuitry.

Description

The Address Decoding circuitry consists of a number of logic gates arranged in a combinational logic circuit that decodes the ranges of addresses shown in Table 5-4, Processor Board Address Enabling Signals. A 3-to-8 line decoder also forms part of the circuitry, and outputs the eight OBIOX&X signals.

Note that two sets of two multiple-input AND gates are marked off by dashed lines on the schematic. Address Decoding is designed to work with one or the other set present but not both. Both of these sets of gates feed a three-input NAND gate which directly produces OBRAM. Ordinarily, the set with the four-input AND gates is present. This set decodes addresses in the range X'FE00' to X'FFFF' in I/O ADDRESS SPACE. CMOS RAM is located in this range. On the other hand, if another MPU is added to the system, the set with five-input AND gates would be present. This set decodes addresses in the range X'00000' to X'001FF' in MEMORY ADDRESS SPACE. This gives a secondary MPU local RAM.

Table 5-4

PROCESSOR BOARD ADDRESS ENABLING SIGNALS (a)

Addressed Circuit	Signal	Address Range (Hexadecimal)	
32K ROM	OBROM-0	MEMORY	F8000-FFFFF
CMOS RAM	OBRAM-0	I/O	FE00 & FFFF
PCI	OBIO0&2-0	I/O	00E0 & 00E2
PCI	OBIO4&6-0	I/O	00E4 & 00E6
Programmable Interrupt Controller	OBIO8&A-0	I/O	00E8 & 00EA
Keyboard Controller MPU	OBIOC&E-0	I/O	00EC & 00EE
Programmable Interval Timer	OBIO1&3-0	I/O	00E1 & 00E3
Programmable Interval Timer	OBIO5&7-0	I/O	00E5 & 00E7
RS-232 Interrupt Enable and Status A	OBIO9&B-0	I/O	00E9 & 00EB
Bus Timeout Reset and Status B	OBIOD&F-0	I/O	00ED & 00EF
System Bus	OBADR(-1)	MEMORY	00000-F7FFF
System Bus	OBADR-0	I/O	0000-00DF
System Bus	OBADR-0	I/O	00F0-FDFF **(b)**
System Bus	OBADR-0	I/O	8000-FDFF

(a) With all straps set to their normal positions.
(b) The I/O address space range X'0100'-X'7FFF' is defined as "not accessible" in the 4114 address space configuration.

Operation

The MPU enters bus cycle T1 during which it outputs an address on lines AD0-19 and the MPU status signals S0-2. The Address Drivers latch these signals on the trailing edge of ALE. If the address falls in one of the ranges of Processor board circuitry, the Address Decoding circuitry generates one and only one of the output signals in Table 5-X, Processor Board Address Enabling Signals, in addition to OBADR active low. Once OBADR goes active low, it generates OBDEN in conjunction with the timing signals T3W4 and T4I. T3W4 essentially turns OBDEN on and T4I turns it off. Note that a Processor board interrupt by means of OBINTA can also cause OBDEN to go active low.

All of the OBIOX&X signals are generated by the 3-to-8 decoder. Since all of the addresses for these signals fall in the range X'00E0' to X'00EF', the decoding gates examine bits A4-7 which carry the binary 1110, that is, hexadecimal E. The 3-to-8 decoder has bits A0, A2, and A3 as inputs, but NOT bit A1. Thus, the decoder cannot distinguish between, for example, X'00E0' and X'00E2', and outputs the same OBIOX&X signal for both addresses. For example, for X'00E0' and X'00E2', the decoder outputs OBIO0&2.

If MDEN goes active high, it disables both OBDEN and OBADR. This implies that the MPU cannot access either Processor board or System bus accessible locations. The 41XX Bus Test Fixture uses MDEN.

BUS TIMEOUT DETECTOR (SCHEMATIC A3-1)

Purpose

The Bus Timeout Detector detects when a System bus slave device fails to respond with an acknowledge signal (ACK1) to a command from any master device. It drives ACK1 onto the System bus and sets an error status bit (D8), which the MPU can read.

Signals

The input signals are:

- OUT0 (Output 0). OUT0 is the output of a 16-bit down counter in the Programmable Timer and Baud Rate Generator circuitry.
- OBIOD&F (On-board I/O D and F). Along with an output from the MPU Timing Generator, OBIOD&F resets the bus timeout error flip-flop.
- INTA (Interrupt Acknowledge). The MPU interrupt acknowledge.
- AIOWC (Advanced I/O Write Command).
- IORC (IO Read Command).
- MRDC (Memory Read Command).
- AMWC (Advanced Memory Write Command).

The output signals are:

- ACK1 (Acknowledge 1). ACK1 is one of two acknowledge signals in the System bus data transfer protocol.
- D8 ((Processor) Data bus bit 8). Here it carries error status information.

Description and Operation

This circuitry consists of a 4-bit binary counter, a D-type flip-flop, and some logic gates. The QD output of the binary counter drives ACK1 through an open-collector driver. The Q output of the error flip-flop becomes D8 after it passes through an output-controlled line driver.

During a normal data transfer between any bus master and any slave device, one of the bus command lines goes low, enabling the 4-bit counter to begin counting. Since the programmable clock input signal, OUT0, is normally about 20 ms, the bus command would have to be held low continuously for 160 ms before QD of the counter would go high. If this bus timeout condition does occur, QD sets the error flip-flop and drives ACK1 by means of an open-collector driver. This completes the handshake seqence for the non-responding or non-existent slave device.

If the bus commands are all less than 160 ms, the counter is always reset before it can drive QD high, and, thus, no bus timeout occurs.

Note that this circuit detects timeouts even when some other bus master is controlling the bus. In a multiple-processor board system, it may be desirable to disable the timeout function on one or more of the Processor boards by cutting cut-strap W561.

STATUS INPUT (SCHEMATIC A3-5)

Purpose

Status Input allows the MPU to read Processor board status signals--BUSGRT, (System bus) STEST, TIMR1, and bus timeout error.

Signals

The input signals are:

- BUSGRT (Bus Grant). Similar to BUSAEN but with a timing difference.
- STEST (Self Test). Goes active low when the self-test button on the terminal is pressed.
- LS0 (Latched Status 0). One of three status signals (S0-2) output by the MPU to show what state it is in.
- OBIOD&F (On-board I/O D&F). OBIOX&X signals inform the MPU what parts of Processor board circuitry are addressed.
- CMD (Command). Shows whether a local read (RD) or write (AWT) operation takes place.

The output signals are:

- STATEN (Status Enable). Enables a three-state input to a buffer in the Bus Timeout Detector.

Operation

The Status Input circuitry outputs STATEN active high if CMD is active high, LS0 is inactive high, and OBIOD&F is active low. If STATEN goes active high, this enables two buffers which put BUSGRT as D11, STEST as D10, Output 1 of the Programmable Interval Timer as D9, and bus timeout error as D8 on the Processor data bus, D0-15.

BUS CLOCK GENERATOR (SCHEMATIC A3-1)

Purpose

The Bus Clock Generator generates the 4.9152 MHz, 50% duty-cycle bus clock signal, BCLK, for the Processor board and System bus.

Signals

The input signals are:

- OSC output of the Clock Generator in the Microprocessor Control circuitry. A 14.7456 MHz square wave.
- CLK output of the Clock Generator in the Microprocessor Control circuitry. A 4.9152 MHz square wave with a 33% duty cycle. This is 14.7456 MHz divided by 3.

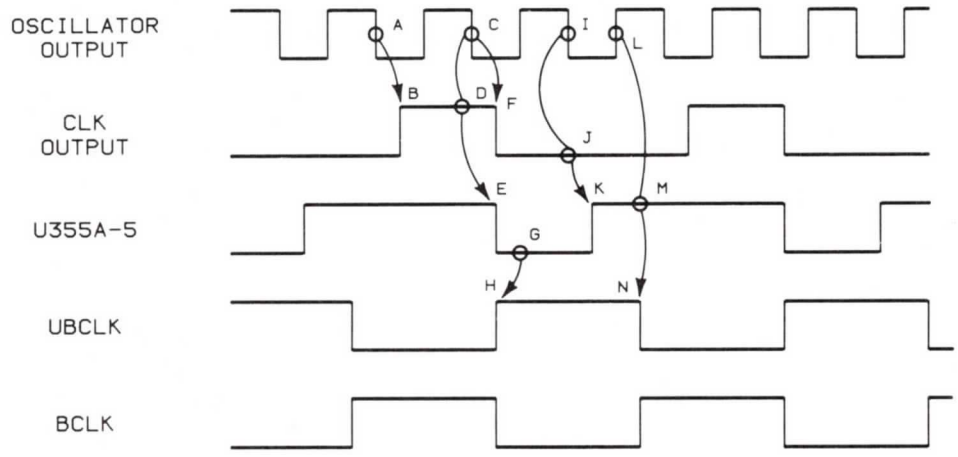
The output signals are:

- BCLK (Bus Clock). A 4.9152 MHz square wave with a 50% duty cycle. It synchronizes bus mastership transfers and provides a stable clock for various functions on other circuit boards.
- UBCLK (Unbuffered Bus Clock). Same as BCLK, but is used only on the Processor board to drive the clock inputs of the Keyboard Controller MPU and the PCI.

Description and Operation

The Bus Clock Generator consists of two JK flip-flops and two logic gates. A four-input NAND gate is used as a 50 OHM TTL driver to give extra drive to BCLK for the System bus. The NOR gate is simply an inverter for the clock input to one of the JK flip-flops. (Cut strap W456 can be cut to enable only one Processor board to generate BCLK in a multiple Processor board system.)

This circuitry transforms a 50% duty cycle, 14.7456 MHz signal (OSC output) and a 33% duty cycle, 4.9152 MHz signal (CLK output) into two 50% duty cycle, 4.9152 MHz signals, UBCLK and BCLK. Figure 5-11, Bus Clock Generator Timing, shows the timing relationships among the signals in the circuitry.



NOTES:

A,B The trailing edge of OSC causes CLK to go high.

C,D,E The trailing edge of OSC and a high on CLK cause Pin 5 of the U355A JK flip-flop to go low.

C,F The trailing edge of OSC causes CLK to go low.

G,H A low level on U355A-5 causes UBCLK to go high.

I,J,K The trailing edge of OSC and a low level on CLK causes U355A-5 to go high.

L,M,N The leading edge of OSC and a high level on U355A-5 causes UBCLK to go low.

3820-17

Figure 5-11. Bus Clock Generator Timing.

MPU TIMING GENERATOR (SCHEMATIC A3-1)

Purpose

The MPU Timing Generator provides MPU timing information for other circuitry on the Processor board.

Signals

The input signals are:

- S0-2 ((MPU) Status bits 0 through 2). Taken together show the eight possible states of the MPU -- interrupt acknowledge, I/O read, I/O write, halt, instruction fetch, memory read, memory write, and no bus cycle.
- ALE (Address Latch Enable). Clears four D-type flip-flops.
- LS1 (Latched Status bit 1). See unlatched S0-2.

The output signals are:

- T3W4 ((State) T3, TW, & T4). High when the MPU is in a T3, TW (WAIT), or T4 state. T3W4 enables on-board data transceivers.
- T4I ((State) T4, TI (idle)). Low during MPU T4 and TI (IDLE) states. It turns off data transceivers during T4 in Processor board memory and I/O READs.
- AWT (Advanced Write). Advanced write command -- analogous to the System Bus AIOWC signal -- for all Processor board circuitry.

Description

The MPU performs memory and I/O transfers by going through bus cycles. Each bus cycle consists of at least four clock states which are called T1, T2, T3, and T4. Sometimes, TW, or WAIT states, are inserted between T3 and T4. Also, TI, or IDLE states, are sometimes inserted between bus cycles. The MPU Timing Generator makes this information available to other circuitry on the Processor board.

The MPU Timing Generator comprises four logic gates and one quadruple D-type flip-flops IC. The interconnections among the four D-type flip-flops are shown in Figure 5-12.

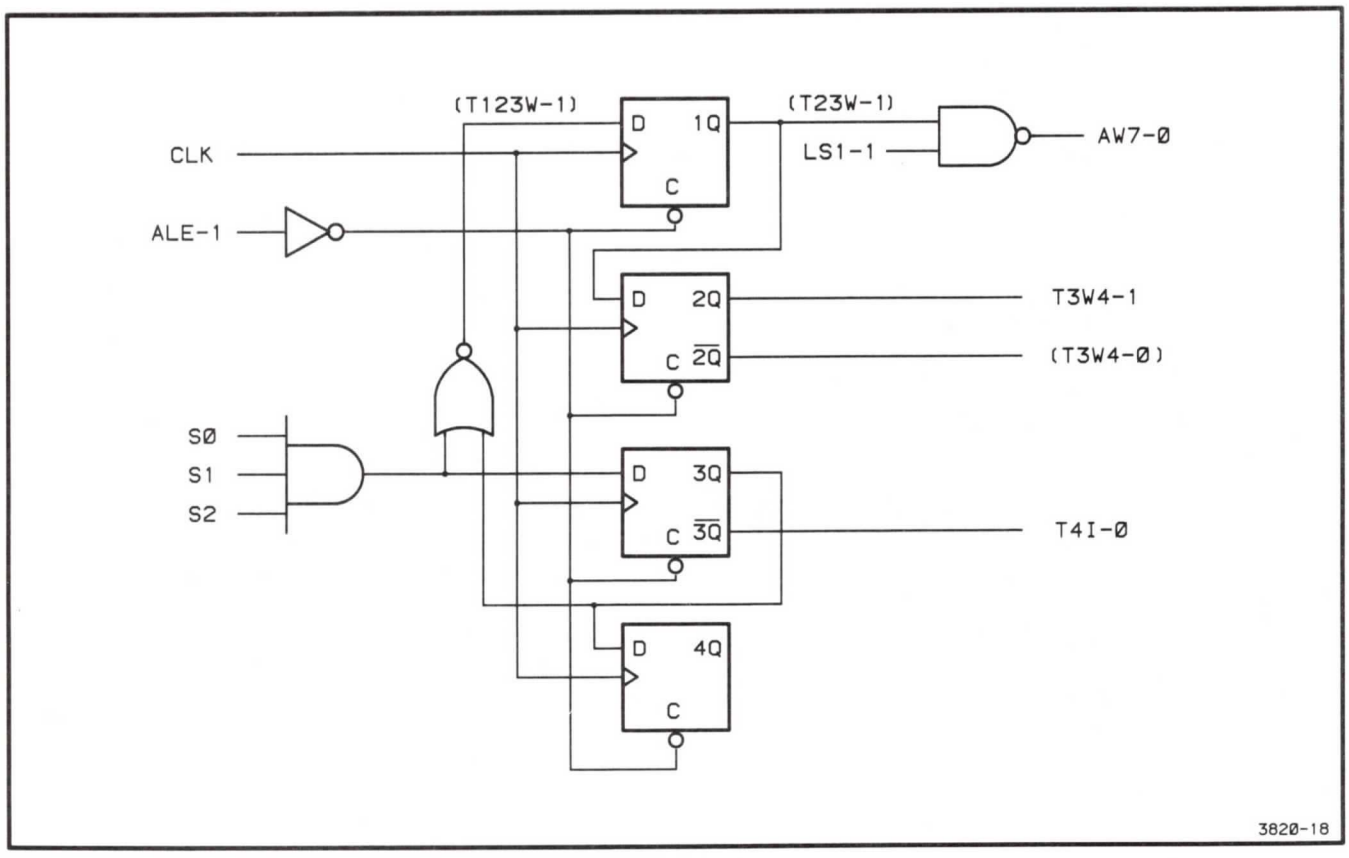


Figure 5-12. MPU Timing Generator Circuitry.

Operation

The circuit is basically a shift register. At the end of a bus cycle, the D input of flip-flop #1 is a logical one. When the next bus cycle begins, ALE resets all four flip-flops during T1. Next, T2 is entered and the Q output of flip-flop #1 becomes logical one. This condition turns AWT active low. During T3, the Q output of flip-flop #2, which is T3W4, goes active high, since it is connected directly to the Q output of flip-flop #1. After T3, it enters the TW state unless or until MPU status bits S0-2 become all logical one. Then, in state T4, the Q-not output of flip-tlop #3, which is T4I, goes active low. The MPU Timing Generator stays in state TI until the MPU issues another ALE during T1.

Table 5-5

MPU STATE AND MPU TIMING GENERATOR SIGNALS

	MPU Clock State					
Signal Name	**T1**	**T2**	**T3**	**TW(a)**	**T4**	**TI (a)**
(T123W)	True	True	True	True	False	False
(T23W)	False	True	True	True	False	False
T3W4	False	False	True	True	True	False
T4I	False	False	False	False	True	True

(a) Note that there may be multiple TW and TI states.

PROGRAMMABLE TIMER AND BAUD RATE GENERATOR (SCHEMATIC A3-5)

Purpose

The Programmable Timer and Baud Rate Generator has three programmable counters inside a Programmable Interval Timer (PIT) that generate timing signals to produce: a) transmit baud rate in the RS-232 Communications Interface logic b) TIMR1 that can generate an interrupt signal to the MPU and c) OUT0, the primary firmware interrupting timer and timing source for the bus timeout detector, which prevents the bus from "hanging".

Signals

The input signals are:

- A1, A2 ((Processor) Address bits 1, 2). Lines of the internal address bus. They address the three 16-bit down counters in the PIT and an internal register, the address control word register.
- AWT (Advanced Write). If low, enables the PIT to output counter data.
- BBCLK (Buffered Bus Clock). A 4.9152 MHz clock signal that clocks a 4-bit counter.
- OBIO1&3, OBIO5&7 (On-board I/O). Either signal, when active low, enables the PIT for reading or writing.
- RD (Read). Processor bus read signal. The PIT inputs data from D0-7 when RD is low.
- RST-1 (Reset). Local reset signal derived from System bus INIT. When high, it clears the 4-bit counter.

The output signals for this block are:

- D0-7. Processor data bus. Carries three kinds of information: a) values to load the PIT counters with, b) values read from the PIT counters, and c) data that programs the various modes of the PIT.
- OUT0 (Output 0). Output of counter 0 in the PIT.
- TIMR1 (Timer 1). Output of counter 1 in the PIT.
- (O2). Output of counter 2 in the PIT.

Description

This circuitry consists primarily of the Programmable Interval Timer (PIT). The PIT has three internal 16-bit counters numbered 0, 1, and 2. It also has a data buffer and read/write circuitry. See Figure 5-13.

This circuitry also has one positive AND gate and one 4-bit binary counter. The AND gate combines OBIO5&7 and OBIO1&3 to operate the chip select input of the PIT. The counter produces two signals by dividing the buffered bus clock signal (BBCLK) by two and eight. BBCLK-divided-by-two is input to the number 2 counter of the PIT and BBCLK-divided-by-eight is input to the number 0 and 1 counters of the PIT.

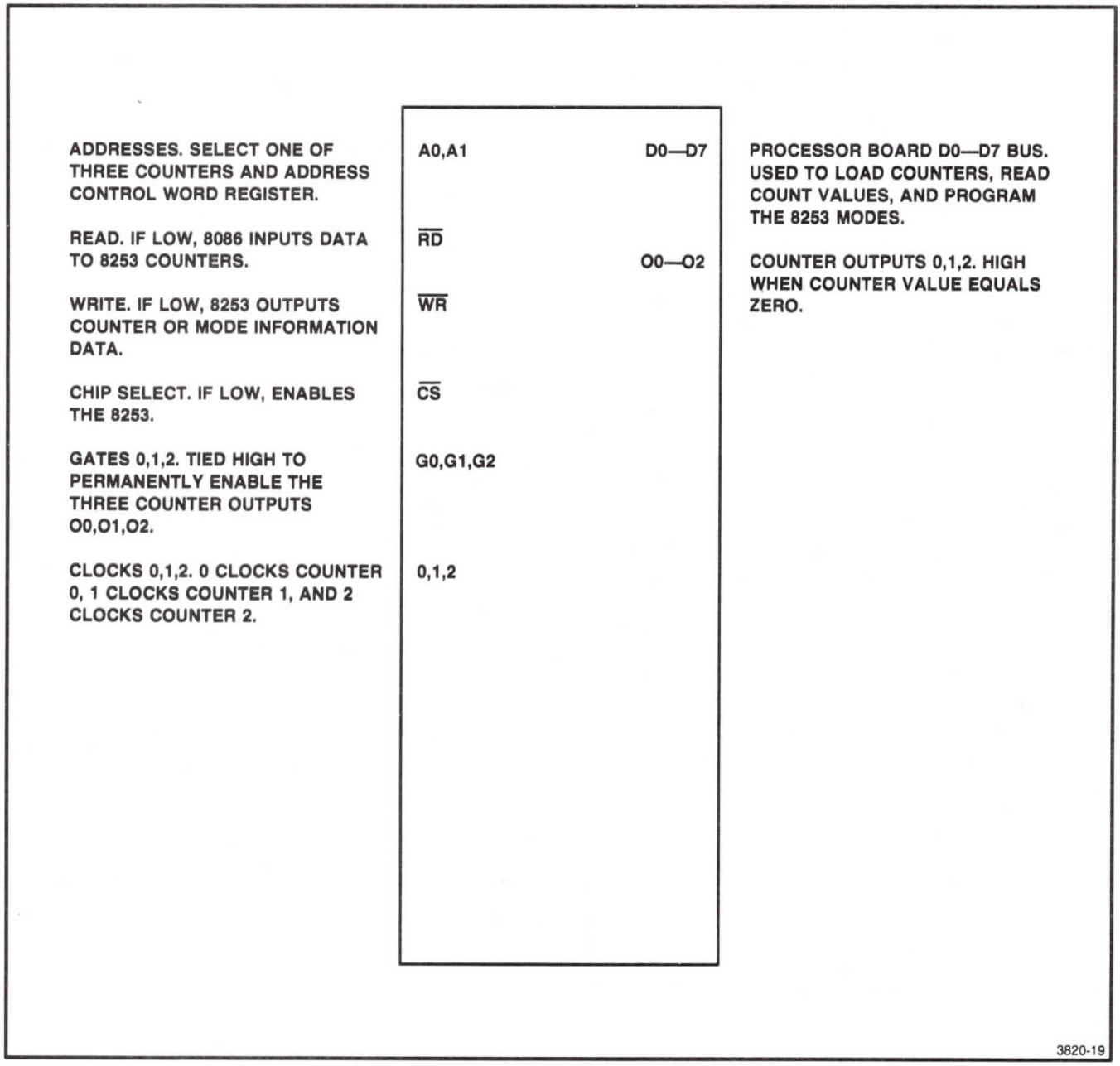


Figure 5-13. Programmable Interval Timer Pin Descriptions.

Programmable Interval Timer

There are three main blocks of circuitry in the PIT: three 16-bit down counters, an 8-bit data bus buffer, and read/write logic.

The three counters operate independently and each has its own output (O0, O1, O2). How the counters operate is controlled completely by commands from the system (or possibly other) firmware. Each counter is loaded with an initial value supplied by firmware. Firmware commands can also read the counter value of a counter at any time during its down count.

The data bus buffer is connected to D8-15, part of the Processor data bus. Firmware commands, initial counter values, and read-out counter values pass through this buffer.

The read/write logic is turned on by the chip select input to the PIT. The local Processor signals, RD and AWT, control the direction of data flow in the data bus buffer. Part of the Processor address bus, A1 and A2, select which of the three counters that commands and counter values are directed to.

Operation

The PIT has two phases of operation: initialization and normal operation. Initialization occurs shortly after the 4114 is turned on (though initialization commands may be given after this time).

After power up, the MPU initializes the PIT as follows: either OBIO1&3 or OBIO5&7 goes active low to enable the PIT and, A1 and A2 select counter 0, 1, or 2. AWT goes active low which enables firmware commands and counter values to program the selected counter via D8-15. After all three counters are programmed, initialization is done.

Note that there is no reset pin on the PIT, and that after the System bus INIT signal goes high inactive and before the MPU initializes the PIT, outputs O1, O2, and O3 are undefined and may be stable high, low, or clocking.

In normal operation, a count value may be read from one of the counters. In this case RD goes active low after the PIT and the appropriate counter are selected. The counter value then appears on D8-15.

Also in normal operation, output 2 (O2) produces the baud rate signal for the RS-232 Communications Interface, output 1 (O1) produces TIMR1 that is used by the MPU Control circuitry in combination with a number of other "interrupt"-type signals, and output 0 (O0) produces OUT0 that serves as both the primary interrupting firmware timer, and as the clock source for the bus timeout detector.

RS-232 STATE CHANGE DETECTOR (SCHEMATIC A3-5)

Purpose

The RS-232 State Change Detector detects state changes on the incoming RS-232 status lines (DSR, DCD, SDCD, CTS, and RING) and generates an interrupt (TIMERINT) when any of these change state.

Signals

The input signals are:

- DSR (Data Set Ready). Informs the RS-232 Communications Interface that the local modem is ready to operate.
- DCD (Data Carrier Detector). Informs the RS-232 Communications Interface that the carrier wave is being received by the modem.
- SDCD (Secondary Data Carrier Detector). Informs the RS232 Communications Interface that the secondary carrier wave is being received by the modem.
- CTS (Clear To Send). Informs the RS-232 Communications Interface that the modem is ready to transmit. This is a response to RTS (Request To Send) from the RS-232 Communications Interface circuitry.
- RING (Ring Indicator). Informs the RS-232 Communications Interface that the local modem is receiving a ringing signal from a remote modem.
- RST (Reset). Clears the last state latch.

The output signals are:

- (Y) (State Change Detected Signal). Produces TIMERINT in conjunction with other signals in the RS-232 Communications Interface.

Description

This circuitry consists of a 4-input line receiver, a 6-input D-type flip-flops device (latch), a bus driver, a 6-bit comparator, and part of another 4-input line receiver. (The five capacitors connected to the line receivers prevent voltage spikes -- glitches -- on the RS-232 status lines from being transmitted to the RS-232 State Change Detector circuitry.)

Operation

The MPU interacts with the RS-232 State Change Detector in two ways. It first receives an interrrupt and then determines what caused the interrupt.

The RS-232 status signals (DSR, DCD, SDCD, CTS, and RING) are input to the last state latch and to the comparator (Note also that the O0 output of the Programmable Interval Timer in the Programmable Timer and Baud Rate Generator block makes up a sixth input to the comparator and latch.) The six outputs of the latch are routed to the bus driver and to the other half of the magnitude comparator. So the comparator compares the inputs and outputs of the latch.

Suppose any one of the RS-232 status lines (or the O0 output of the PIT) changes state. The comparator then outputs an active low on (Y) which activates a NAND gate in the RS-232 Communications Interface. This causes TIMERINT to go active low. After TIMERINT is processed by the Interrupt Controller, the MPU eventually receives an interrupt.

At this point the MPU needs to determine which RS-232 status line (or O0 from the PIT) caused the interrupt. The MPU now reads either the "old" status lines or the "new" ones. To read the "old" status lines which exist at the outputs of the latch, it addresses the RS232 State Change Detector which causes OBIO9&B to go active low. Also, A1 must be active high. Now RD strobes, causing the bus driver to drive the status line data onto the Processor bus. To read the "new" status lines, OBIO9&B goes active low again, but this time A1 goes low. Now, the latch is clocked, and the bus driver drives the inputs ("new" status lines) of the latch onto the Processor data bus. From here, firmware determines which status line caused the TIMERINT interrupt.

RS-232 COMMUNICATIONS INTERFACE (SCHEMATIC A3-5)

Purpose

The RS-232 Communications Interface transmits and receives RS232 characters and control ("handshake") signals. It contains the receive Baud Rate Generator.

Signals

The input signals are:

- RDATA (Receive Data). Serial data from the host computer.
- RCLK (Receive Clock). External clock signal generated by the local modem or other source. Can be used to clock data into the Programmable Communications Interface (PCI).
- TCLK (Transmit Clock). External clock signal generated by the local modem or other source. TCLK can be used to clock data out of the PCI.
- D0-15 (Processor data bus bits 0 through 15).
- A1-2 (Processor address bus bits 1 and 2). Carry addresses that select internal registers in the PCI.
- OBIO9&B (On-board I/O 9 and B). Active low when data appears on the Processor bus for the interrupt enable latch (with inputs D8-15).
- UBCLK (Unbuffered Bus Clock). Clocks the Internal Baud Rate Generator in the PCI.
- LS1 (Latched Status bit 1). Part of LS0-2 which taken together indicate which of eight states the MPU is in. When LS1 is low, the MPU is in an interrupt acknowledge, I/O read, memory read, or instruction fetch bus transaction.

- OBIO0&2, OBIO4&6 (On-board I/O locations 0 & 2, and 4 & 6). Either signal going active low enables the PCI if CMD is active high.
- CMD (Command). When active high, it indicates that the MPU is doing a Processor board read or write.

The output signals are:

- SRTSA (or C) (Secondary Request To Send A (or C)). Half-duplex RS232 handshaking signal. Strapped to "A" or "C" depending on the type of modem used.
- DTR (Data Terminal Ready). Informs the modem that the terminal is operational.
- RTS (Request To Send). Informs the modem that the terminal is ready to transmit data.
- TDATA (Transmit Data). Data is transmitted serially on this line to the modem or directly to the host computer.
- COMINT (Communications Interrupt). COMINT goes active low, when a character is received by the PCI from the host computer.
- TIMERINT (Timer Interrupt). When TIMERINT goes active low, any one of the following interrupts has occurred: PIT timer #1 (output O1), PCI TXEMT, PCI TXRDY, RS-232 status change, or a PIT OUT0 (via RS-232 State Change Detector circuitry).

Description

This circuitry consists of a line driver, a line receiver, a number of logic gates, and a fancy USART, the Programmable Communications Interface (PCI). The PCI is the heart of this circuitry and is described below. See Figure 5-14.

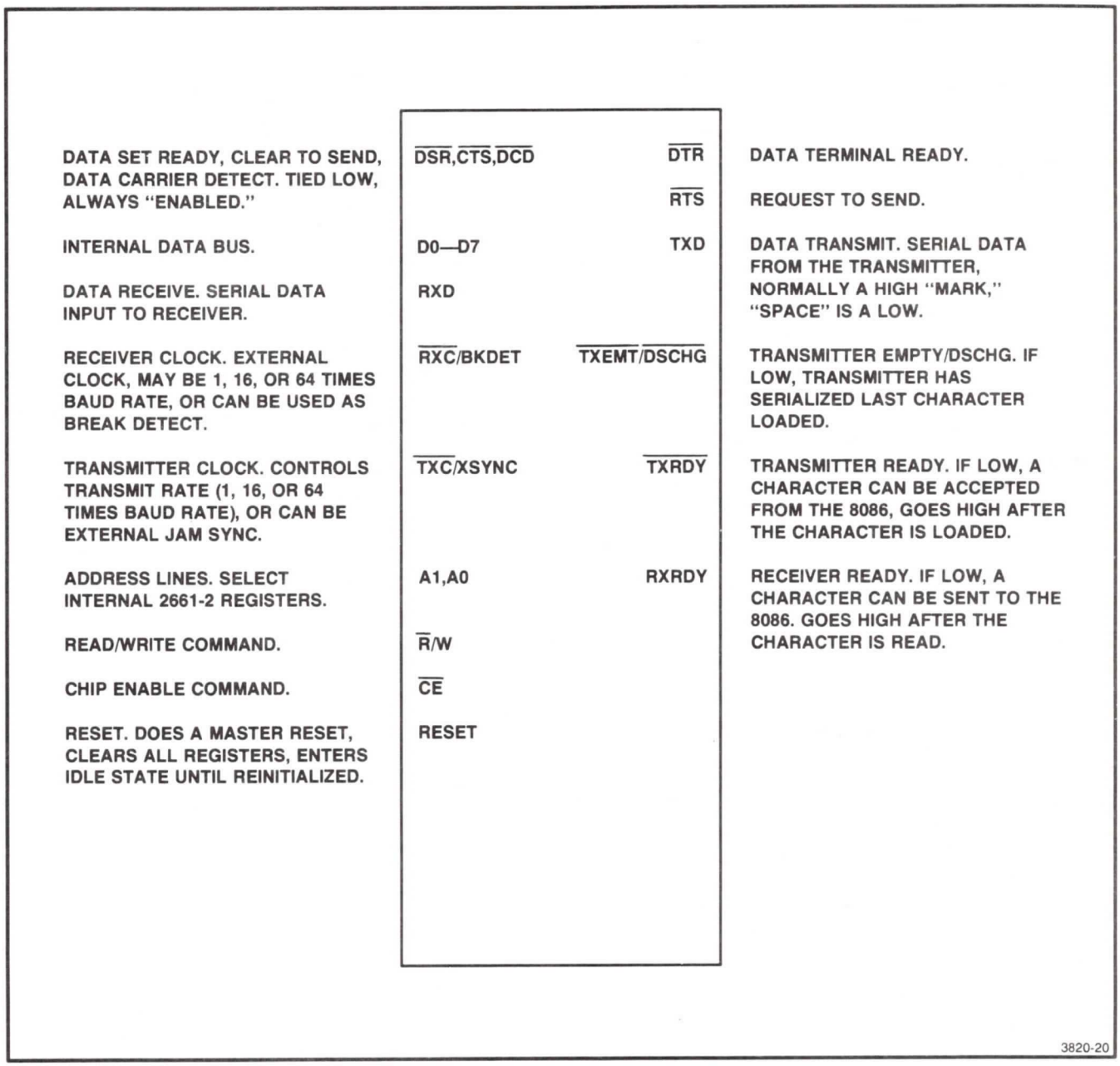


Figure 5-14. Programmable Communications Interface Pin Descriptions.

Programmable Communications Interface

This integrated circuit performs the parallel-to-serial data conversion for data sent to the host computer and also the serial-to-parallel conversion for data sent to the terminal. The PCI also has a programmable Baud Rate Generator. In order to perform these functions, the PCI has the following circuitry. See Figure 5-15.

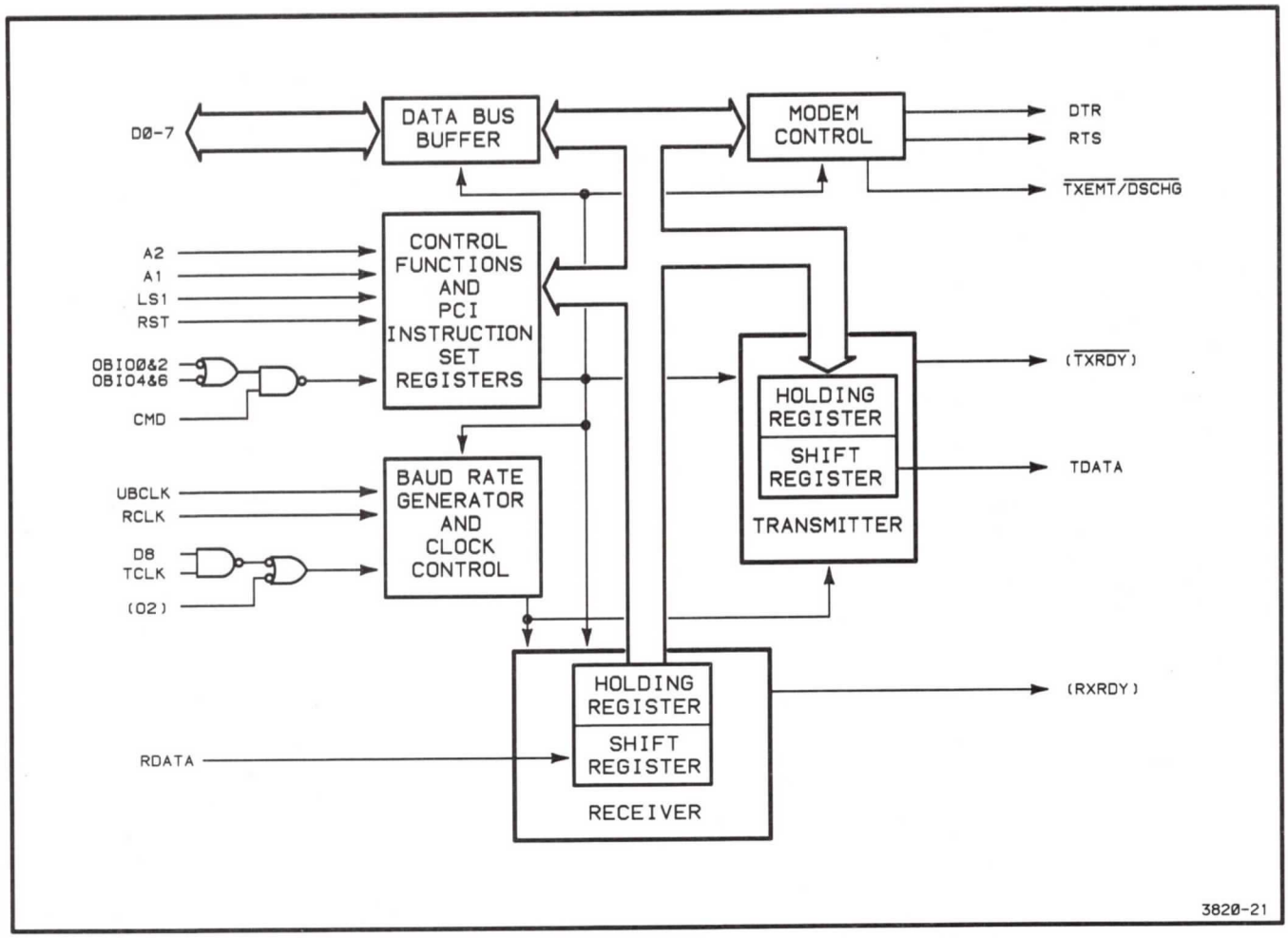


Figure 5-15. Programmable Communications Interface Block Diagram.

Data Bus Buffer. D0-7 are input and output via this 8-bit buffer. Firmware commands, status information, and data are transferred through the buffer.

Modem Control. Two "handshaking" signals, DTR and RTS, are sent directly to the host computer or modem from this block. (TXEMT-0/DSCHG-0) also originates here, and when low, indicates that the transmitter has completed the parallel-to-serial conversion of the last character loaded by the MPU. Note that DSR-0, CTS-0, and DCD-0, which are generated in this circuitry, are permanently tied low.

Control Functions. By responding to A1-2, LS1, OBIO0&2, OBIO4&6, and CMD, this circuitry controls when the PCI is written to and read from. Also, this circuitry controls the overall PCI internal operation. In addition, there are internal registers whose contents are manipulated by firmware commands.

Baud Rate Generator and Clock Control. UBCLK provides the source frequency for the internal baud rate generator. Usually, the transmit baud rate is generated by output O2 from the PIT and the receive baud rate is generated from the internal Baud Rate Generator and a software- selectable register value. However, 1X baud rate clocks from the modem may be selected for either the receive rate, transmit rate, or both. For external transmit clocks, TCLK is converted to TTL levels, multiplexed with the PIT O2, and input to (TXC-0). For external receive clocks, RCLK is converted to TTL levels, and input directly to (RXC-0), since the signal is multiplexed internally with the Internal Baud Rate Generator.

Transmitter. The holding register receives data from the MPU and passes it to the shift register. Start, stop, and parity bits are added to the data according to the current communication parameters. The data is then output serially and becomes TDATA.

Receiver. The shift register receives serial data on RDATA. This passes to the holding register and bits or characters are checked according to the current communication parameters. The data is then output to the MPU during a read of the data register.

Operation

Before the RS-232 Communications Interface can send and receive data, its operating parameters must be set by a combination of firmware and soft-ware commands and values. Communications parameters like synchronous or asynchronous mode, receive baud rate, parity, number of bits per character, etc., are sent to the PCI shortly after the terminal is powered up. Once this programming of values is done, normal data communication begins.

MPU Control

The MPU controls the PCI by activating A1-2, LS1, OBI00&2, OBI04&6, and CMD. The bit pattern of A1 and A2 together determine which of four registers in the control function circuitry is selected to be read from or written to. The MPU first selects the PCI by causing OBI00&2 or OBI04&6 to go active low, and CMD to go active high. LS1 is low for a read operation and high for a write operation.

Data Communication

Serial data on RDATA is input on the RS232 cable (via P102). The data is then converted to TTL levels by the line receiver and fed to the (RXD) input of the PIC. Serial data is output to the line driver and becomes TDATA on the RS232 cable (via Pi02). The PIC determines when to output DTR and RTS for modem control also on P102. Note that SRTS is controlled by the MPU directly and is latched, inverted, and level-converted before it reaches P102. (SRTSC -- the usual strap setting -- may be strapped to produce SRTSA if the modem requires it.)

Interrupts

The signals (TXEMT-0), (TXRDY-0), and (RXRDY-0) are status signals from the PCI that can generate interrupts to the MPU. All three signals are inverted and ANDed with "interrupt enable"-type signals from the latch. This allows the MPU to disable the PCI interrupts.

KEYBOARD CONTROLLER (SCHEMATIC A3-4)

Purpose

The Keyboard Controller scans the keyboard port for key and thumbwheel change data and informs the MPU if there is any activity. The Keyboard Controller also handles the LED and bell signals.

Signals

The input signals are:

- A1 (Processor Address line 1). Tells the KC MPU whether data on D0-7 is data or a command.
- AWT (Advanced Write). Allows the MPU to write to the Keyboard Controller MPU.
- RD (Read). Allows the MPU to read data from the Peripheral Interface MPU.
- OBIOC&E (On-Board I/O C and E). Enables the Peripheral Interface MPU.
- RST (Reset). Resets the Keyboard Controller MPU.
- UBCLK (Unbuffered Bus Clock). 4.9152 MHz square wave input to the Keyboard Controller MPU.
- KBT1 (Keyboard Test 1). Test input to the Peripheral Interface MPU.
- KD0-7 (Keyboard Data 0 to 7). Key change and thumbwheel information appear on these lines from the keyboard.

The output signals are:

- KWR (Keyboard Write). Strobes KA0-3 into the LED and Bell Logic circuitry on the Keyboard Thumbwheel board.

- KSTRB (Keyboard Strobe). Latches KA0-3 into the LED and Bell Logic and Character Decoder circuits on the Keyboard Thumbwheel board.
- KBDINT (Keyboard Interrupt). Interrupt to MPU via the Programmable Interrupt Controller.
- KA0-3 (Keyboard Address 0 to 3). Carry key matrix column addresses for the CHARACTER DECODER circuit and LED on-off data for the LED AND BELL LOGIC on the Keyboard Thumbwheel board.

Description

The main component in this circuitry is an 8-bit Keyboard Controller Microcomputer (KC MPU). Firmware written in the instruction set of the KC MPU enables it to transmit key change and thumbwheel data from the Keyboard Thumbwheel board to the Processor data bus. Also, keyboard LED and bell signals are transmitted from the Processor data bus to the Keyboard Thumbwheel board.

Other components are: an 8-bit buffer, three inverters, and seven open-collector buffer gates. The 8-bit buffer is always enabled and buffers KD0-7 for the KC MPU. Two of the Inverters are placed between UBLCK and the clock inputs, X1 and X2, to provide extra drive for the inputs. The seven buffer gates drive KWR, KSTRB, KBDINT, and KA0-3 onto the Keyboard Thumbwheel board.

Keyboard Controller Microcomputer

This microcomputer consists of the following blocks of circuitry: control logic, timing, test logic, I/O ports 1 and 2, status register, data out buffer, data in buffer, and one large block that consists of all block that do not have direct inputs from or outputs to the Keyboard Controller. See Figure 5-16 and Figure 5-17.

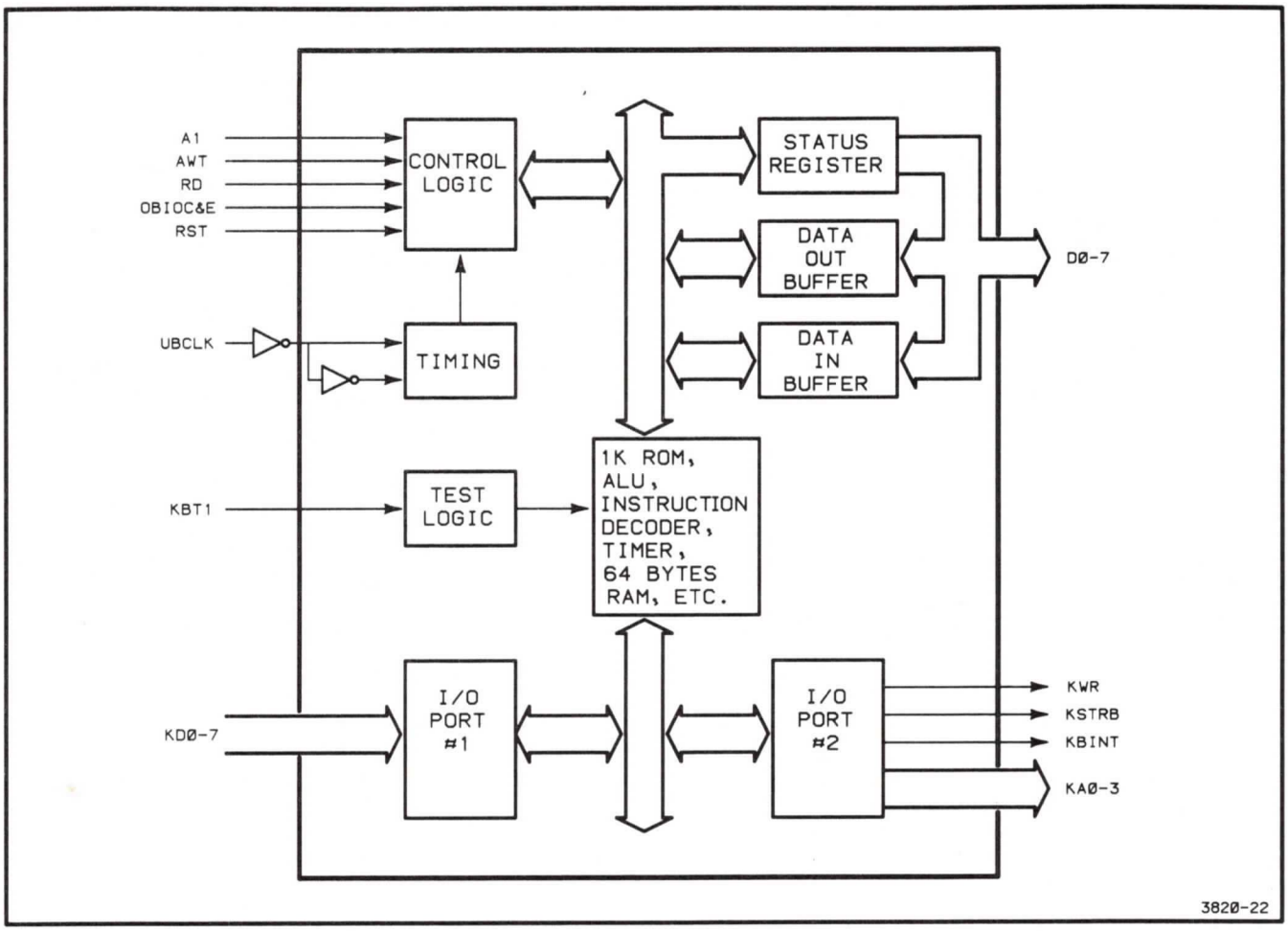


Figure 5-16. Keyboard Controller Microprocessor Block Diagram.

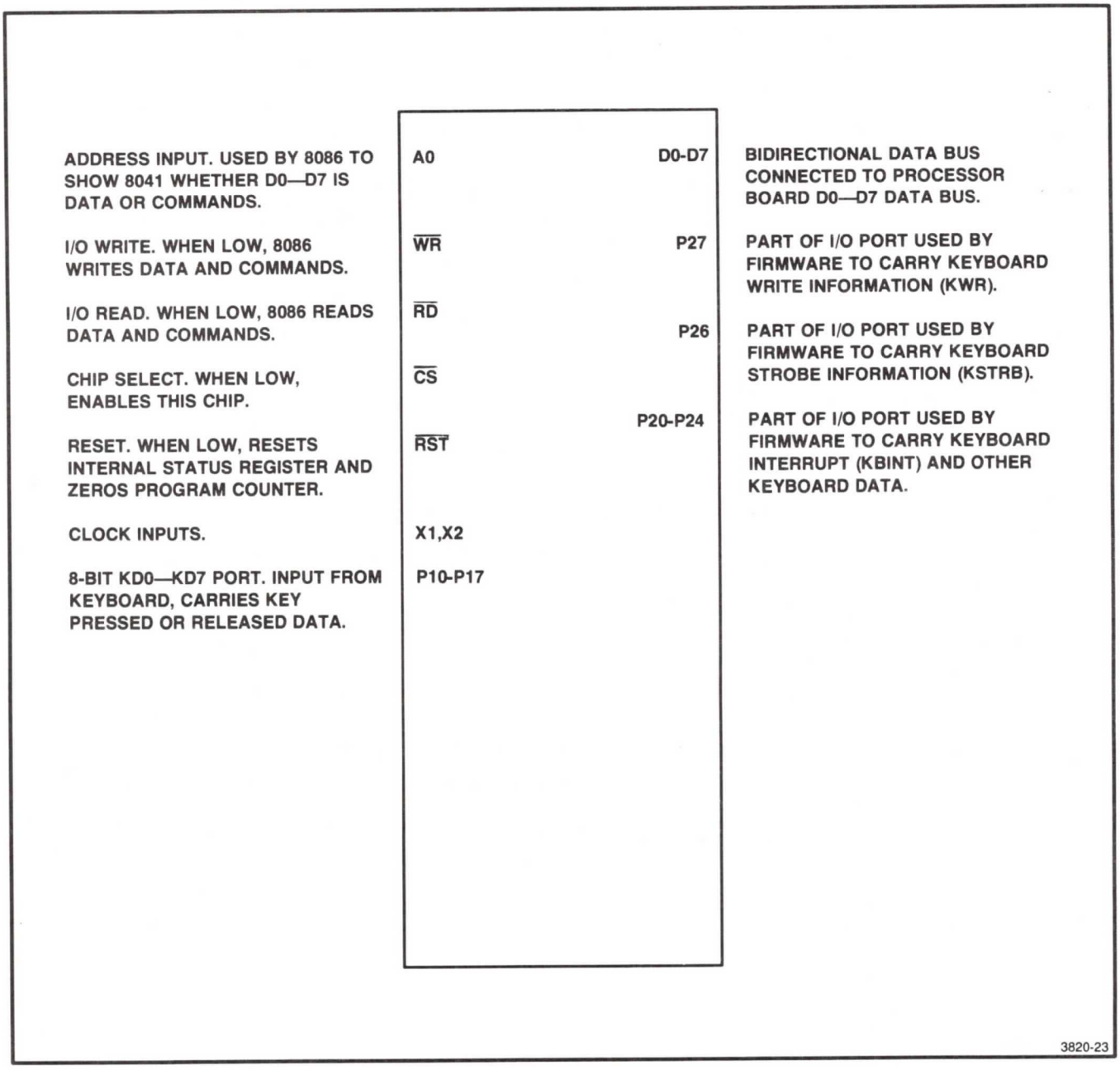


Figure 5-17. Keyboard Controller Microprocessor Pin Descriptions.

Control Logic. This logic produces internal instructions which accomplish a variety of internal control functions. The signals that determine these internal control functions are A1, AWT, RD, OBIOC&E, and RST. A1 enables the MPU to indicate to the KC MPU that information on D0-7 is data or a command. AWT, when low, allows the MPU to write data to the data in buffer. RD, when low, allows the MPU to read data from the status buffer or data out buffer. OBIOC&E enables the KC MPU. RST resets various internal counters and status flip-flops. (Note that the (SS-0) and (EA) inputs, though they are inputs to the control logic, control functions that are effectively disabled since they are tied high and grounded, respectively.)

Timing. UBCLK provides the 4.9152 clock for an internal oscillator.

Test Logic. (Test 0) has been "disabled" by tying it high, but (Test 1) is controlled by KBT1. A high on KBT1 can be read by firmware in the KC MPU during testing. This testing is done at the time of manufacture of the 4114 terminal.

I/O Ports 1 and 2. Although these ports can function as input and output ports, I/O Port 1 functions only as the input port for KD0-7 and I/O Port 2 functions only as the output port for KWR, KSTRB, KBDINT, and KA0-3.

Status Register. This register, which is accessed by the MPU through D0-7, carries status information informing the MPU what kind of data is in the data buffers and whether it should or can read from or write to the KC MPU. The MPU reads the status register at I/O address X'00EE'.

Data-Out Buffer. The MPU reads all data (key codes and thumbwheel position data) from the KC MPU from this buffer. The data out buffer I/O address is X'00EC'.

Data-In Buffer. The MPU writes data and commands to the KC MPU through this buffer. The data in buffer I/O address is X'00EC'.

Operation

The KC MPU has firmware routines masked into its 1K of ROM. These routines cause the KC MPU to operate independently of the MPU. In addition to carrying out these routines, the KC MPU responds to a set of commands that the MPU issues to it. These commands cause operations such as ringing the terminal bell, turning LEDs on and off, enabling keyboard interrupts, enabling and disabling the timer interrupt, resetting the KC MPU, and inquiring about the keyboard identity.

The KC MPU passes three kinds of data to the MPU: keycodes, thumbwheel count values, and keyboard identification data. The interactions between the MPU and KC MPU are somewhat different for each kind of data.

Keycode Data

The KC MPU has internal firmware that causes KA0-3 to scan the character decoder on the Keyboard Thumbwheel board. (See the Keyboard Thumbwheel circuitry description.) If the MPU has enabled the KC MPU interrupt and if a key is pressed or released, the KC MPU reads a keycode from KD0-7. The keycode is placed in the data-out buffer and the KC MPU issues an interrupt on KBINT. Now, the MPU reads the status register to determine which of the three kinds of data the KC MPU has for it. At this point, the MPU initiates a routine which reads the 8-bit keycode from the data-out buffer.

Suppose a key is held down. The MPU recognizes whether this is a valid repeating key and if it is, the MPU sends the command to enable the timer. The KC MPU starts a 500 ms delay. If the MPU, within this delay, has not sent the command to disable the timer, the KC MPU interrupts the MPU every 100 ms until the MPU sends the disable command (because the key was released).

Thumbwheel Count Values

Firmware routines in the KC MPU scan the thumbwheel count values from the Keyboard Thumbwheel board. When these routines detect a change in a thumbwheel count value (one counter each for the horizontal and vertical thumbwheels), the counter is adjusted and a KBINT is issued if 45 ms has passed since the previous KBINT. The MPU finds out from the status register that there is thumbwheel count data in the data-out buffer and reads it. Note that the MPU is interrupted only if the thumbwheels move since the KC MPU routines issue an interrupt only if there is a change in the counter value associated with either thumbwheel.

Keyboard Identification

When the terminal is turned on or reset, the KC MPU places the keyboard status in the status register and the keyboard identification code in the data-out buffer. Also,the MPU itself can determine the keyboard identity at any time by sending a keyboard indentification command to the KC MPU.

LED and Bell

The LED on-off state and bell sounding are controlled by sending commands to the KC MPU. In order to turn an LED on or off, the MPU sends to the KC MPU the address of the LED and the "on" command or the "off" command. The KC MPU controls the timing once it gets the address and "on" or "off" command. The bell sounds when its address and the bell command is sent. The bell sounds once for every bell command that is sent to the KC MPU.

INTRODUCTION TO THE KEYBOARD

The keyboard consists of four blocks of circuitry that drive the LEDs (LED & Bell logic circuitry), ring the terminal bell (Bell Logic), interface the thumbwheels to the character decoder (Thumbwheel Interface Logic), and output character codes when keys are pressed or released (Character Decoder logic). See Figure 5-18.

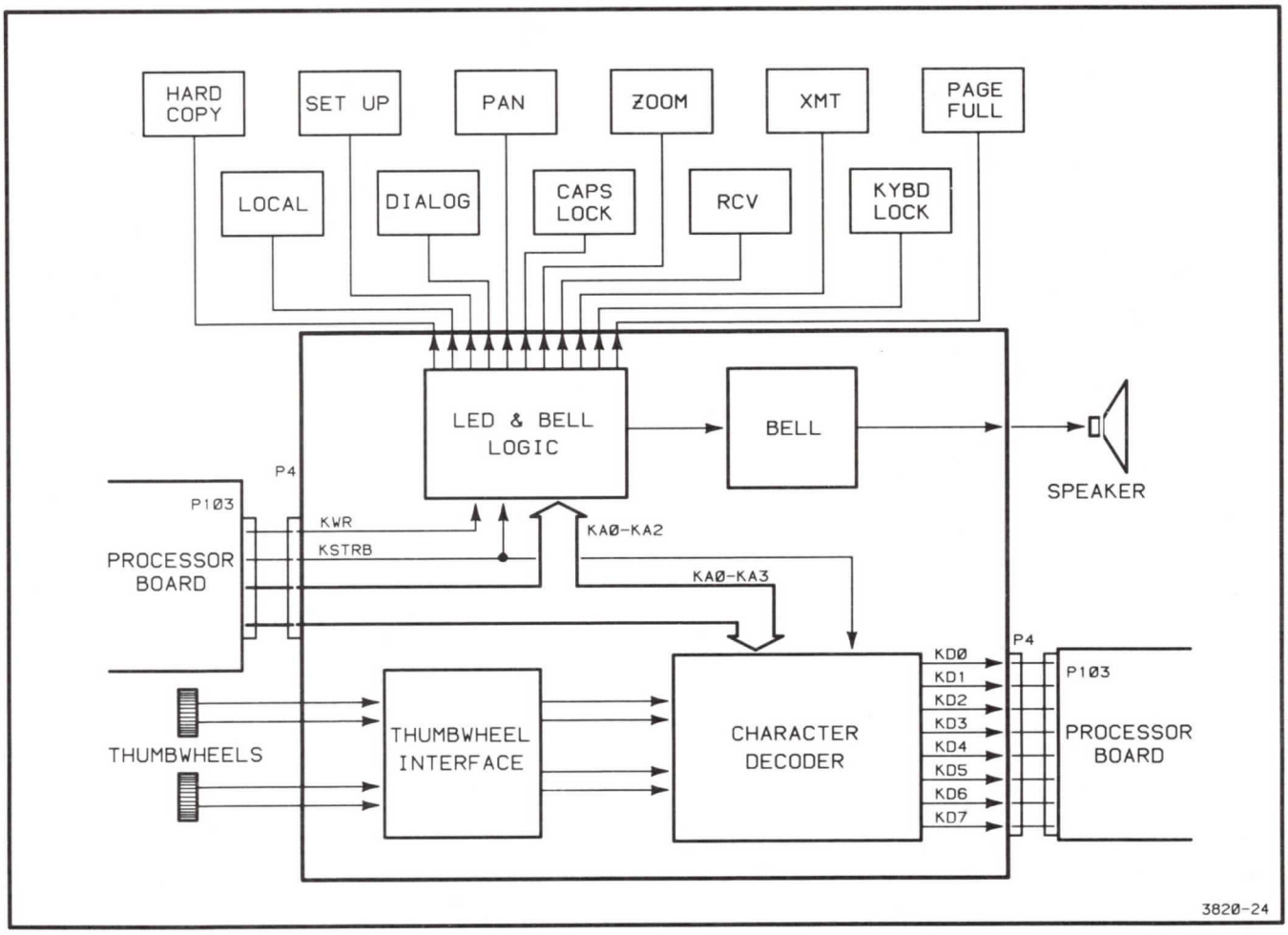


Figure 5-18. Keyboard Block Diagram.

LED & BELL LOGIC (SCHEMATIC A4-1.)

Purpose

The LED & Bell Logic lights the LEDs and rings the bell on command.

Signals

The input signals are:

- KWR (Keyboard Write). Strobes LED and bell data into two 8-bit addressable latches.
- KSTRB (Keyboard Strobe). Latches the LED address from KA0-3 and the currrently selected X line of the column interrogator IC into the Character Decoder and LED and Bell Logic circuitry.
- KA0-3 (Keyboard Address Bits 0,1,2 and 3). Carry multiplexed address and on-off information for the bell and LEDs.

This circuitry turns on or off the terminal bell and any of eleven LEDs, located on the terminal keyboard surface.

Operation

How an LED Changes State

The Keyboard Controller MPU (in the Keyboard Controller circuitry on the Processor board) sends a binary address from 000 to 111 on lines KA0 through KA2. (Note that just seven addresses are needed on one 8-bit addressable latch and only five on the other.) This binary address is latched by the D-type flip-flops.

Now the KC MPU sends the on or off information on lines KA0 and KA1. KA0 controls the state of any of the seven LEDs output from one of the 8-bit latches, and KA1 changes the state of the bell or other four outputs from the other 8-bit latch.

KWR enables the KA0 or KA1 information to be latched by

whichever latch is addressed.

BELL (SCHEMATIC A4-1.)

Purpose

The Bell circuitry provides an audible tone that the programmer can use to alert the user.

Signals

This block has one input and one output. The input is from an output of an 8-bit addressable latch in the LED and Bell Logic circuitry. The output turns on or off a speaker mounted inside the terminal.

Operation

How the Bell Rings

To ring the bell, the Keyboard Controller MPU first sends a binary address (100) over KA0 through KA2. Next a binary 1 (high) is sent on KA1. (See How an LED Changes State above.) This activates the bell circuitry.

A 555 Timer is connected to form a free running oscillator which generates a square wave signal of about 760 Hz. This 760 Hz signal feeds the base of a transistor connected in series with a Darlington amplifier. After the input to the BELL logic (KA1) switches on the Darlington amplifier, current charges and discharges a capacitor connected across the speaker. The bell tone dies out because an RC network, connected to the base of the Darlington pair, times out after about one half second.

CHARACTER DECODER (SCHEMATIC A3-1.)

Purpose

The Character Decoder detects whether a key has been pressed or released. It also detects the positions of both thumbwheels.

Signals

The input signals are:

- KSTRB (Key Strobe). A strobe signal.
- KA0-3 (Key Address bits 0 through 3). Carry address information.

In addition to these signals, each key of the keyboard changes capacitance when it is pressed or released, and each thumbwheel sends a 2-bit Grey code.

The output signals are:

- KD0-7 (Keyboard Data bits 0-7). Carry key or thumbwheel information to the keyboard port on the Processor board.

Operation

How Key Change Data Is Created

The Keyboard Controller MPU on the Processor board needs two kinds of information to recognize that a key has been pressed or released. These two kinds of information correspond to the columns and rows of the key "matrix". Each key has a unique position at the intersection of a column and row in the matrix. So, when the KC MPU receives both column data (KA0 through KA3) and row data (KD0 through KD7), it can determine which key has changed state.

The firmware driving the KC MPU repeats the following sequence of operations for each column of the key matrix.

The KC MPU outputs a low on KSTRB which disables the outputs (KD0 through KD7) of the row detector. Four bits of information representing a column of the key matrix are loaded onto lines KA0 through KA3. (Note that only ten columns are used for the keys, one is not used, and the remaining column line is used in the THUMBWHEEL INTERFACE logic.)

The column represented by the KA0 through KA3 address data is interrogated. If a key in that column is pressed or released during the interrogation, the row detector IC senses this change. KSTRB now goes high and a low appears on the row signal (KDx) corresponding to the key position.

THUMBWHEEL INTERFACE (SCHEMATIC A3-1.)

Purpose

The Thumbwheel Interface changes voltage of thumbwheel output to TTL level and gates output to KD4 through KD7 keyboard data lines.

Signals

The inputs to this block are two sets of 2-bit Grey code. One set is output by the vertical thumbwheel, the other by the horizontal thumbwheel. The outputs of the block are the two sets of Grey code changed to TTL voltage levels.

Operation

How the Thumbwheels Output 2-bit Grey Code

The thumbwheels operate identically so only one thumbwheel is described. Rigidly attached to the shaft of the thumbwheel is a disk perforated with equally spaced slots. As the wheel is turned, a light, stationary with respect to the slotted disk, activates two phototransistors in this sequence: Both phototransistors on (00); one off, the other on (01); both off (11), and one on, the other off (10). This sequence is the 2-bit Grey code. So, the thumbwheels output only four states each.

How The Thumbwheels Interface to the KD4-7 Lines

The 2-bit Grey code signals from the thumbwheels have voltage levels outside TTL levels. So, these signals are changed to TTL levels by four CMOS NAND gates. The outputs of these NAND gates connect to four TTL NAND gates. The outputs of the TTL NAND gates are passed to the row detector only when the X11 line of the column interrogator goes high. At this time, KD4 through KD7 have valid thumbwheel 2-bit Grey code data on them.

Section 6

RAM/ROM CIRCUIT THEORY

INTRODUCTION TO RAM/ROM BOARD

The RAM/ROM circuit theory describes the general architecture and operation of the RAM/ROM board in general, and then describes each block of circuitry. The order of description of the blocks follows the basic information flow, from left to right, of the block diagram. Refer to Figure 6-1.

GENERAL DESCRIPTION

This board supplies 32K bytes of RAM on one RAM Array board, in addition to a maximum of 64K bytes (32K 16-bit words) of ROM-type memory.

The circuitry of the board consists of a dynamic RAM controller IC with support circuitry, one socket where a RAM Array board plugs in, and 16 ROMs with support circuitry. (The RAM Array board is a small circuit board that holds 32K bytes of dynamic RAMs.)

GENERAL OPERATION

Three basic operations performed by this board are:

- Reading the contents of a location in RAM.
- Writing over the contents of a location in RAM.
- Reading the contents of a location in ROM.

To read the contents of a location in RAM, the bus master first drives the location address onto the System bus, and then MRDC. When the RAM Controller board receives an active MRDC signal, it responds by driving ACK2 onto the bus, and then the data from the address location.

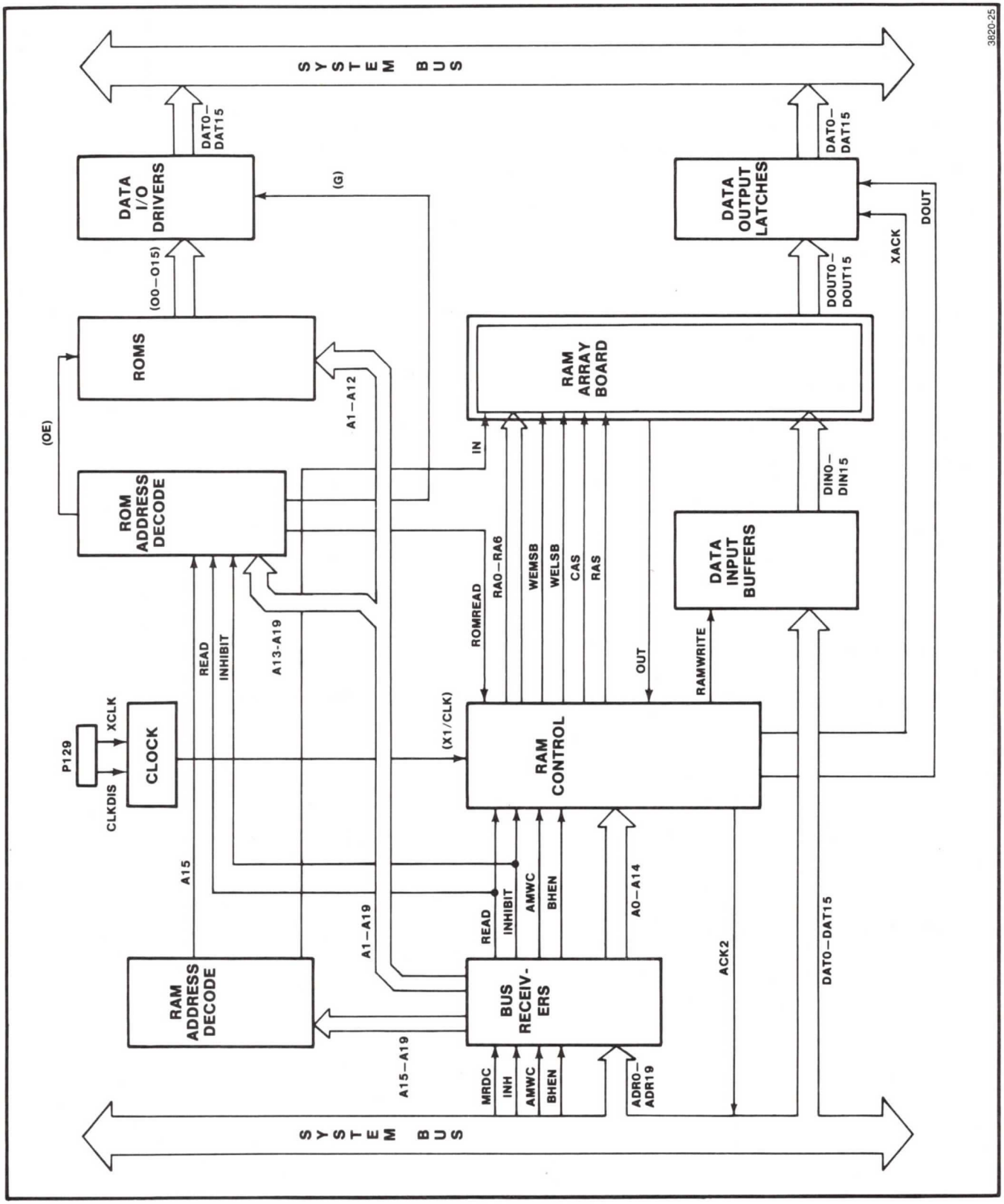


Figure 6-1. RAM/ROM Block Diagram.

To write over the contents of a location in RAM, the same sequence of events occurs except that MRDC is replaced by AMWC, and the bus master drives the data onto the bus.

To read the contents of a location in ROM, the bus master follows the same sequence of events as for a read from RAM. However, when the signals reach the board, they are routed through different circuitry than that for a read from RAM. The RAM Controller is not involved in a read access from ROM.

BUS RECEIVERS (SCHEMATIC A5-1.)

Purpose

The Bus Receivers receive signals from the System bus and buffers them for the board.

Signals

The input signals are:

- MRDC (Memory Read Command). This is the System bus memory read signal.
- INH (Inhibit). This is a signal that prevents the board from outputing data to the System bus.
- AMWC (Advanced Memory Write Command). This is the System bus advanced memory write signal.
- BHEN (Byte High Enable). During byte (8-bit) write operations to RAM, the RAM/ROM board examines BHEN and ADR0 to determine which byte is to be written. If BHEN is true (low), the high byte (D8-15) is written. If ADR0 is false (low), the low byte (D0-7) is written.
- ADR0-19 (System Bus Address bits 0 through 19). These signals are the system address lines.

The output signals are:

- A0-19 (Local Address bits 0 through 19). These are the buffered system address lines.
- READ. Buffered MRDC.
- INHIBIT. Buffered INH.

Operation

The three bus receivers in this block are permanently enabled. This means that the outputs constantly follow whatever is on the System bus. The board responds when the correct range of addresses and active (low) read (MRDC) or write (AMWC) signals appear on the System bus.

RAM CONTROL (SCHEMATIC A5-1.)

Purpose

The RAM Control's purposes include:

- Generates all control signals for the RAMs on the RAM Array board.
- Provides address multiplexing and address strobes for the RAM on the RAM Array board.
- Decides whether the RAM on the RAM Array board will be in a read, write, or refresh cycle.
- Provides signals to latch data from the RAM Array board and to drive data onto the System bus.

Signals

The input signals are:

- READ. Buffered memory read command signal.
- INHIBIT. A signal that prevents this board from outputing data.
- AMWC (Advanced Memory Write Command). The System bus advanced memory write command signal.
- BHEN (Byte High Enable). A signal that enables the most significant byte of a 16-bit word of data to be written by itself.
- A0-14 (Local Address bits 0 through 14). Buffered System bus address signals.
- ROMREAD. Active when the ROM bank is doing a read access.
- OUT. Active when the RAM Array board is addressed and is plugged in.

- CLK (Clock). A 22.008 MHz square wave TTL signal that drives the clock (X1/CLK) input to the 8202 Dynamic RAM Controller.

The output signals are:

- DOUT (Data Output). Outputs RAM data to the System bus when low.
- ACK2 (Acknowledge 2). Acknowledges that the memory operation currently requested by the bus master has begun and will soon be completed. (See discussion of the System bus in Section 4.)
- RAMWRITE. Enables the data input buffers when a write access to the RAM Array board occurs.
- WELSB and WEMSB (Write Enable Least Significant Byte and Write Enable Most Significant Byte). Strobe data into the RAMs on the RAM Array board.
- CAS (Column Address Strobe). Latches the column address into the RAMs on the RAM Array board.
- RA0-6 (RAM Address bits 0 through 6). Multiplexed buffered System bus addresses A1-14.
- RAS (Row Address Strobe). Latches the row address into the RAMs on the RAM Array board.
- XACK (Transfer Acknowledge). Latches data into the Data Output Latches.

Description

This block consists primarily of the Dynamic RAM Controller. See Figure 6-2. In addition to this, there are some logic gates that combine related signals into new signals needed by the board. There are also two flip-flops that synchronize the timing of the read and write signals to the Dynamic RAM Controller clock signal (CLK). The Dynamic RAM Controller combines into one all of the functions that are needed to operate dynamic RAM. These functions are: multiplexing 14 bits of address into two 7-bit parts, arbitrating among selecting a read, write, or refresh cycle, generating various timing and control signals. The Dynamic RAM Controller also has circuitry for the internal generation of refresh signals for the dynamic RAM on the RAM Array board.

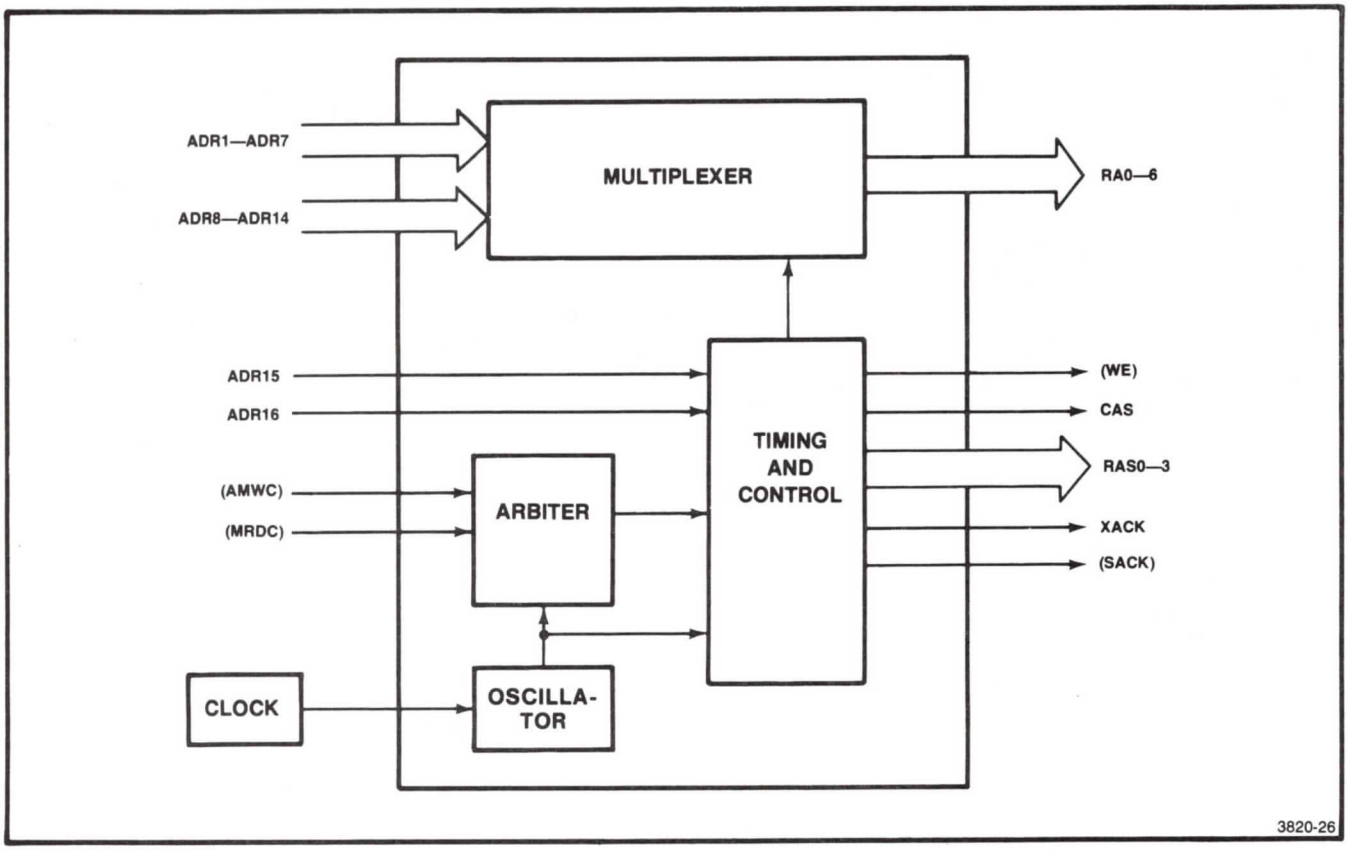


Figure 6-2. Dynamic RAM Controller Block Diagram.

Multiplexing of RAM Addresses

A1-14 are input to the multiplexer in the Dynamic RAM Controller. Because of the requirements of the 16K RAMs on the RAM Array board, A1-14 is split into a low and a high part. A1-7 is output as a 7-bit row address and then A8-14 is output as a 7-bit column address. The low and high parts of A1-14 appear one after the other on the RA0-6 lines of the RAM Control block.

Arbitration of Read, Write, and Refresh Cycles

The Arbiter circuitry in the Dynamic RAM Controller prevents requests for read or write cycles from interrupting read, write, or refresh cycles in current operation. Refresh cycles are generated internally in the Dynamic RAM Controller.

Generation of Timing and Control Signals

This block of circuitry has five functions. It executes a read, write, or refresh cycle at the request of the Arbiter block. It generates the column address strobe (CAS), the write enable (WE), and the row address strobe (RAS). It generates the transfer (XACK) and system (SACK) acknowledge signals. It sends internal control signals to the multiplexer block in the Dynamic RAM Controller. And it resets an internal refresh timer and increments an internal refresh counter.

Clock

The Clock circuitry on the board feeds a 22.008 MHz square wave to the Dynamic RAM Controller. This square wave provides the timing for the Multiplexer, Arbiter, and Timing and Control circuitry inside the Dynamic RAM Controller.

Operation

The Dynamic RAM Controller performs these operations:

- Idling
- Write cycle
- Read cycle
- Refresh cycle

Idling

The Arbiter block in the Dynamic RAM Controller monitors requests for read, write and refresh cycles. Read and write requests originate outside the Dynamic RAM Controller, but refresh requests all originate internally to the Dynamic RAM Controller.

The Dynamic RAM Controller is idling when requests are not currently being processed and cycles are not in progress. Read cycles are initiated if MRDC is active low when requests are sampled. Write cycles are initiated if AMWC is active low when requests are sampled. If a read or write cycle is requested simultaneously with a refresh cycle, the read or write cycle is executed before the refresh cycle.

Write Cycle

The steps of a write cycle occur in the following order:

1. The Multiplexer drives RA0-6 with the low order address.
2. (SACK) is activated.
3. The RAS strobes the low order row address into the RAM.
4. The Multiplexer drives RA0-6 with the high order address.
5. (WE) is activated.

6. CAS strobes the high order column address into the RAM.

7. XACK is activated.

8. All signals are deactivated and the Dynamic RAM Controller begins idling.

Read Cycle

The read and write cycles are nearly the same except that (WE) is not activated during a read cycle.

Refresh Cycle

When a refresh cycle is internally requested, the Multiplexer drives RA0-6 with a refresh address contained in an internal refresh counter. Then RAS is activated, causing a refresh cycle to occur on the RAM Array board. After some internal operations, the Dynamic RAM Controller begins idling again.

DATA INPUT BUFFERS BLOCK (SCHEMATIC A5-2.)

Purpose

The Data Input Buffers receive data signals from the System bus and buffers them for the RAM Array board.

Signals

The input signals are:

- DAT0-15 ((System) Data bits 0 through 15). Carries 16 bits of data on the System bus.
- RAMWRITE. Enables the data buffers.

The output signals are:

- DIN0-15 (Data Input bits 0 through 15). The buffered version of DAT0-15.

Operation

Whenever AMWC and OUT are active low, the RAM Control block generates RAMWRITE. This enables DAT0-15 to be driven on to the RAM Array board.

RAM ARRAY BOARD (SCHEMATIC A6-1.)

NOTE

The RAM Array board is a BOARD that plugs into the RAM/ROM board and is NOT a block of circuitry on the RAM/ROM board. However, it is treated here as a block of circuitry because it functions like a block of circuitry.

Purpose

The RAM Array Board contains 32K bytes of system dynamic RAMs.

Signals

The input signals are:

- CAS (Column Address Strobe). Latches the column address into the RAMs.
- WELSB and WEMSB (Write Enable Least Significant Byte and Write Enable Most Significant Byte). Strobe data into the RAMs.
- RA0-6 (RAM Address bits 0 through 6). Multiplexed System bus addresses ADR1-14.
- RAS (Row Address Strobe). Latches the row address into the RAMs.
- DIN0-15 (Data Input bits 0 through 15). Carry the System bus data derived from lines DAT0-15.
- IN. Shows the board whether the RAM Array board is plugged in. Works in conjunction with OUT.

The output signals are:

- DOUT0-15 (Data Output bits 0 through 15). Carry data to the Data Output Buffers.
- OUT. Shows whether the RAM Array board is plugged in. Works in conjunction with IN.

Description

The RAM Array board is a small circuit board that contains 32K bytes of dynamic RAMs. One RAM Array board plugs into a socket on the RAM/ROM board.

The 32K bytes of RAM are arranged in two banks on the board. One bank handles the least significant byte of a 16-bit word, and the other bank handles the most significant byte of a 16-bit word. Since the RAMs are 16K-by-one bit wide, there are eight RAMs in each bank.

The RAM address lines RA0-6 connect to both the LSB and MSB banks. RAS and CAS connect to both banks, but there are separate write enable signals (WELSB and WEMSB) that allow the accessing of the high and low bytes of the 16-bit word.

Operation

This board responds to the signals generated by the RAM Controller block. Look under the OPERATION heading under RAM Control for a description of accessing data on the RAM Array board.

DATA OUTPUT LATCHES (SCHEMATIC A5-2.)

Purpose

Data Output Latches accept data from the RAM Array board and buffer it for the System bus.

Signals

The input signals are:

- XACK (Transfer Acknowledge). Latches data (DOUT0-15) into the latches.
- DOUT (Data Output). Cutputs data (DAT0-15) on to the System bus.
- DOUT0-15 (Data Output bits 0 through 15). Carry data output from the RAM Array board(s).

The output signals are:

- DAT0-15 (System data bus bits 0 through 15). Carry data on the System bus.

Operation

When XACK goes active low, data on DOUT0-15 is latched into the flip-flops in each of two D-type latches. When DOUT goes active low, the data is driven onto the System data bus lines, DAT0-15.

RAM ADDRESS DECODE (SCHEMATIC A5-1.)

Purpose

The RAM Address Decode informs the RAM Control block that the RAM on this board has been addressed.

Signals

The input signals are:

- A15-19 (Local Address Bus bits 15 through 19). A15-19 carry an address of 00000 binary in order to address the RAM in the RAM Array board.

The output signals are:

- IN. Indicates that the RAM on the RAM/ROM board is being addressed.

Operation

This block consists of a NAND gate and some inverters that detect when 00000 binary is on A15-19. IN then becomes active low.

CLOCK (SCHEMATIC A5-1.)

Purpose

Clock generates a 22.008 MHz square wave that directly feeds the X1/CLK input of the 8202 Dynamic RAM Controller in the RAM Control block.

Signals

The input signals are:

- CLKDIS (Clock Disable). Prevents the clock from outputting its signal. (Used for test purposes only.)
- XCLK (External Clock). An external clock signal may be connected to this line, but used for test purposes only.

The output signals are:

- (X1/CLK). A 22.008 MHz square wave that drives the Dynamic RAM Controller.

Operation

Two NAND gates are biased into their linear region of operation by 820 ohm feedback resistors. In this mode of operation, the NAND gates act as linear inverting amplifiers. A series tank circuit and a 22.008 MHz crystal are connected in a loop with the two gate amplifiers. This causes the circuit to oscillate at 22.008 MHz. The output is connected to the X1/CLK input of the 8202 Dynamic RAM Controller. The output also clocks two flip-flops in the RAM Control block.

ROM ADDRESS DECODE (SCHEMATIC A5-3.)

Purpose

The ROM Address Decode circuitry produces one of eight ROM select signals depending on which of the eight banks of ROMs is addressed.

Signals

The input signals are:

- A13-19 (Local Address Bus bits 13 through 19). A15-19 carry 11101 binary or 11110 binary if the ROM block is addressed. A13-15 determine which of eight banks of ROMs is addressed.
- READ. Shows whether a read access is requested.
- INHIBIT. May be used to prevent the ROMS from outputting data on the System bus.

The output signals are:

- ROMSELECT. Enables the outputting of data if a ROM bank has been addressed. Actually is eight separate signals -- one to each of eight banks of ROMs.
- ROMREAD. Indicates that the ROM is being accessed.
- (ROMDOUT). Enables the ROM data I/O drivers in the Data I/O Drivers block.

Operation

This block consists of a 3-to-8 line decoder and various logic gates.

Whenever both the G2B and G2A inputs to the decoder are low, the address on A13-15 selects one of eight outputs. Each of the eight outputs enables one of the eight banks of ROMs in the ROMS block. READ is connected directly to the G2B input and A15-19 are gated through some logic before they are connected to G2A. If READ is active low and A15-19 is 11101 binary or 11110 binary, the decoder is enabled. (The ROMs in the ROMS block respond to addresses X'E8000' through X'F7FFF'.)

If the bus master initiates a read operation from ROM, the ROMREAD signal becomes active low and the RAM/ROM board drives ACK2 active low on the System bus. INHIBIT prevents the Data I/O Drivers block from outputting data to the System bus if it goes active low.

ROMS (SCHEMATIC A5-3.)

Purpose

ROMs store up to 64K bytes (32K of 16-bit words) of system firmware.

Signals

The input signals are:

- A1-12 (Local Address Bus bits 1 through 12). Address the locations of 32K 16-bit words.
- (OUTPUTENABLE). Actually, eight separate lines that enable one out of eight banks of ROMs at a time during a read operation.

The output signals for this block are sixteen lines of data that become DAT0-15 on the System bus.

Description

In the ROMS block are eight banks of two ROMs each. The banks hold 4K of 16-bit words. A set of straps is associated with each bank of ROMs. The straps allow the board to use various kinds of ROM/PROM/EPROMs that have different pin function assignments.

Operation

This block outputs 16-bit words of data to the Data I/O Drivers block if MRDC goes active low and an address in the range of X'E8000' through X'F7FFF' is presented on A1-19.

DATA OUTPUT DRIVERS (SCHEMATIC A5-3.)

Purpose

Data Output Drivers drive data from the ROMS block onto the System bus.

Signals

The input signals are:

- D0-15 (Local Data Bus bits 0 through 15). 16 bits of data from the ROMS block.
- ROMDOUT (ROM Data Output). Enables both data drivers in this block.

The output signals are:

- DAT0-15 (System data bus bits 0 through 15). System bus data lines.

Operation

Two data drivers in this block handle DAT0-7 and DAT8-15 separately. Whenever (G) is low active, whatever is present on the inputs of the two drivers is output to the System bus as DAT0-15.

Section 7

POWER SUPPLY CIRCUIT THEORY

The 4114 power supply is a high-efficiency type. It provides the advantage of lower weight, smaller volume, and a considerable reduction in power consumption. Figure 7-1 shows a simplified block diagram.

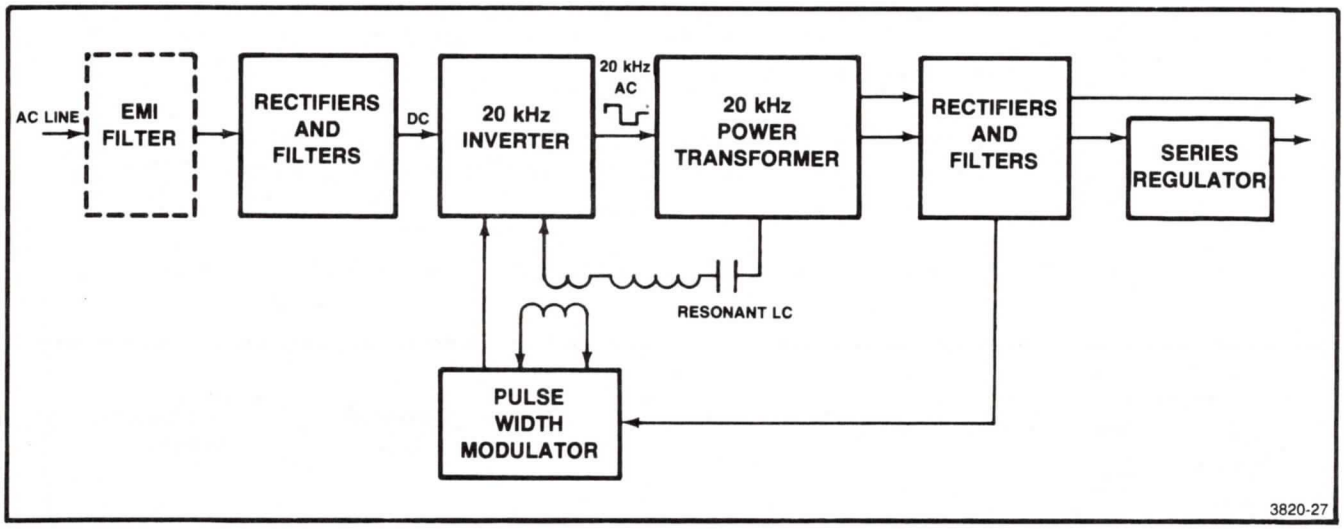


Figure 7-1. Simplified Block Diagram of a High Efficiency Power Supply.

The whole unit is a DC to DC converter. AC input is rectified to dc, fed to a 20 KHz inverter, goes to a power transformer, and is rectified and filtered as it is regulated. High currents at relatively low voltages are made available in this manner.

Current is sensed by a current feedback network which provides control to a PWM (pulse width modulator). The PWM determines the on time of the inverter's power transformer, thus providing some preliminary regulation.

The voltage regulation of the outputs also provides fail-safe overload protection by shutting the supplied voltage down if the current limit is exceeded. This feature is called at various times a "crowbar" circuit, a "foldback" circuit, or simply, a current limiter circuit.

A load of less than 4.0 A on the 5.1 V supply does not allow the other outputs to be operated at their full rated load. Regulation is also lost. None of the supply voltages exceeds its rated value under no-load conditions, but some may be out of tolerance on the low side.

INVERTER BOARD

Figure 7-2 shows that the Inverter board contains:

- Primary power distribution which includes the line voltage selector, filters, and switching transistors. The auxiliary ac to the fans and disc drives also goes through this board.
- The power supply control circuits which include the logical OFF-1/ON-0 switch, the Schmidt trigger, base drivers, and PWM.
- The shutdown circuits and the logic signals.

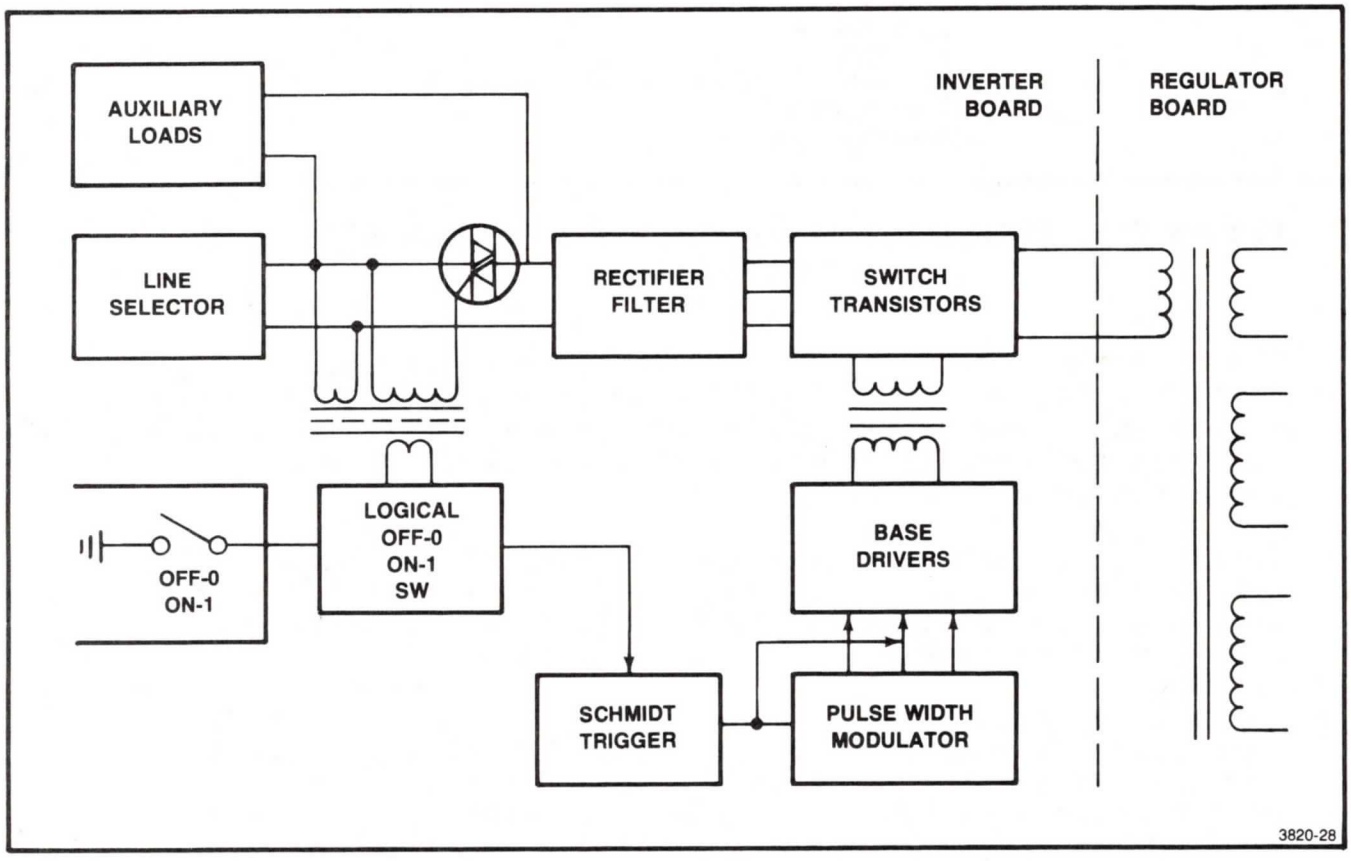


Figure 7-2. Functional Block Diagram of Inverter Board.

REGULATOR BOARD

The functional block diagram (Figure 7-3) shows that the Regulator board delivers four different voltages at varying load currents to the terminal. The four voltages that are delivered to the terminal are +5.1 Vdc, -5.2 Vdc, +12 Vdc, -12 Vdc. +24 Vdc is available for the disk drives. An SDOWN signal and +22 Vdc are delivered internally for use by the power supply.

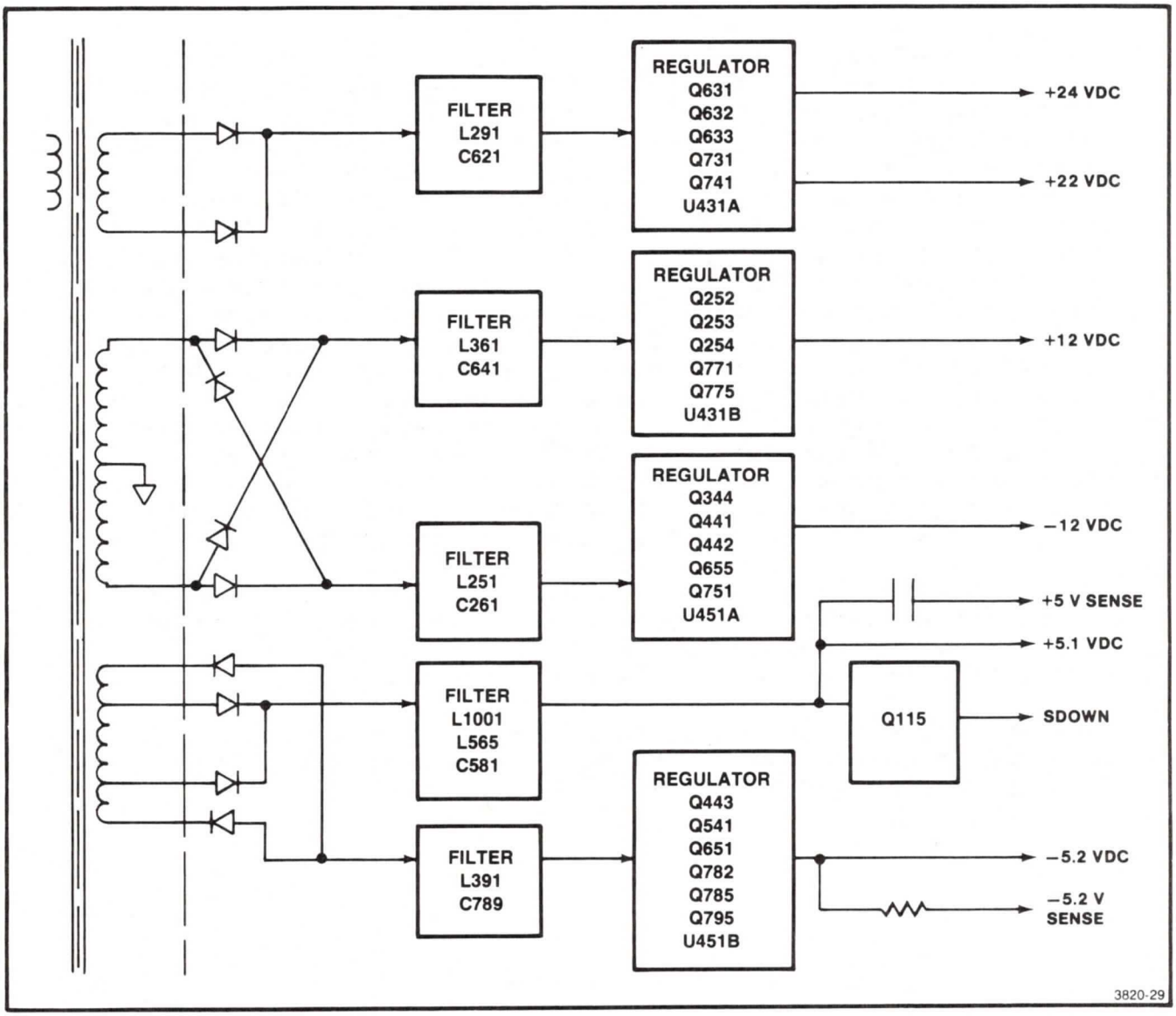


Figure 7-3. Functional Block Diagram of Regulator Board.

DETAILED THEORY OF OPERATION

Inverter Board

Primary Power Distribution

Refer to Schematic A17-1. Positioning the jumper on the inverter board of the power supply selects the line voltage. The power supply is preselected for 115 Vac. Figure 10-24 shows the jumper in position for 115 Vac operation.

The jumper places the neutral side of the line between the filter capacitors at the output of the bridge rectifier when 115 Vac is selected. This causes the capacitors to have a voltage doubler action. When 230 Vac is selected, the filter capacitors act in a regular fashion. The same voltage appears on the switching transistors regardless of the primary input voltage. The output of the rectifier filter is about 300 to 350 Vdc. A neon lamp connected across the output of the rectifier filter in a simple relaxation oscillator configuration flashes when there is high-voltage present on the capacitors. The 7.5 ohm series resistors in the bridge circuit have a negative temperature coefficient (resistance decreases as temperature increases). This limits surge current during turn-on. Since the resistors cool down faster than the bleeder resistors can bleed the filter capacitors, current surge protection is always present. Three arc-gaps are placed across the line and neutral sides of the circuit for voltage transient suppression.

An inductor is placed in the dc supply and return lines to the switching transistors as a noise filter. Two 4uF capacitors are also placed across the input of the switching transistors to provide noise suppression.

A triac acts as a switch to turn the ac input on and off. Its gate is controlled by the turn-on transformer primary which is controlled by the OFF-1/ON-0.

Power Supply Control Circuits

Logical OFF-1/ON-0 Switch

WARNING

Dangerous voltages exist in the power supply module if the power cable is not disconnected from the ac line EVEN THOUGH THE SYSTEM ON/OFF SWITCH IS OFF. Always disconnect the power cable before working on the power supply module.

Use of the OFF-1/ON-0 signal allows the terminal to keep running until operations are completed. Figure 7-4 is a simplified diagram of the logical On/Off switch. The switch acts as a short across the secondary of the turn-on transformer when the unit is turned off. This keeps the triac turned off because the low reflected impedance develops insufficient bias to turn the triac on.

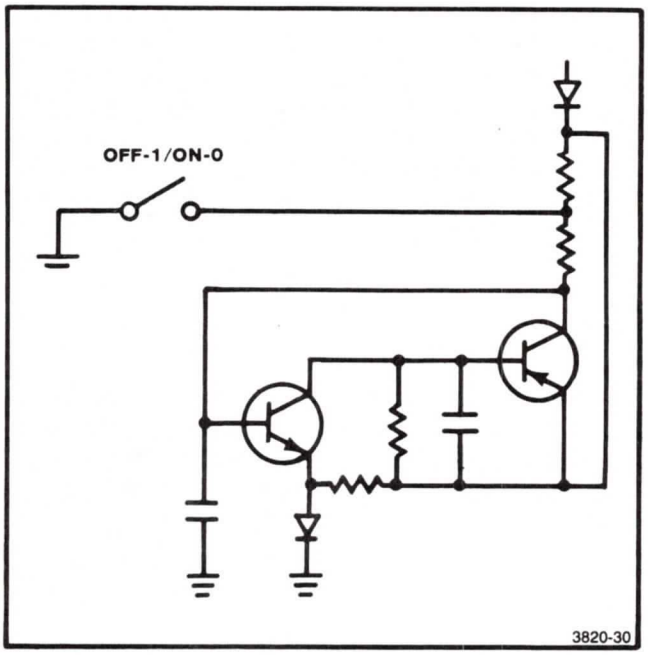


Figure 7-4. Logical OFF-1/ON-0 Switch.

Switch Off. Refer to Figure 7-2. When OFF-1/ON-0 is high, the transistors are conducting and cause a low reflected impedance to appear in the turn-on transformer primary by placing a virtual short on the secondary. The majority of the voltage on the primary of the turn-on transformer is dropped across the resistor in series with the line voltage and the primary winding. An insufficient amount of voltage is developed to enable the triac gate.

Switch On. When the power supply is turned on, the line is grounded, or goes low, the transistors turn off, removing the short from the secondary. This gates the triac on. At the same time, a capacitor on the secondary starts charging. The Schmidt trigger turns on when the capacitor reaches approximately 30 V.

Schmidt Trigger

Refer to Schematic A17-1. The Schmidt trigger supplies power to the base drivers and the pulse width modulator. It turns on when the voltage of the capacitor reaches 30 V. The base drive transistors drive the switching transistors which bring up the power supplies. The +22 V supply goes only to the Inverter board where it provides a "keep alive" voltage for the Schmidt trigger. The capacitor starts discharging through the Schmidt trigger. The voltage drops to about 16 V in about 10 ms and the Schmidt trigger turns off if the +22 V has not come up. The turn off at 16 V prevents the base drive circuit voltage from dropping too low and driving the switching transistors linear.

Pulse Width Modulator

The PWM regulates +5.1 V by controlling the on-time of the switching transistors through the base drivers. The outputs of the PWM are connected in a push-pull configuration to the bases of the drive transistors. Figure 7-5 is a block diagram of the PWM.

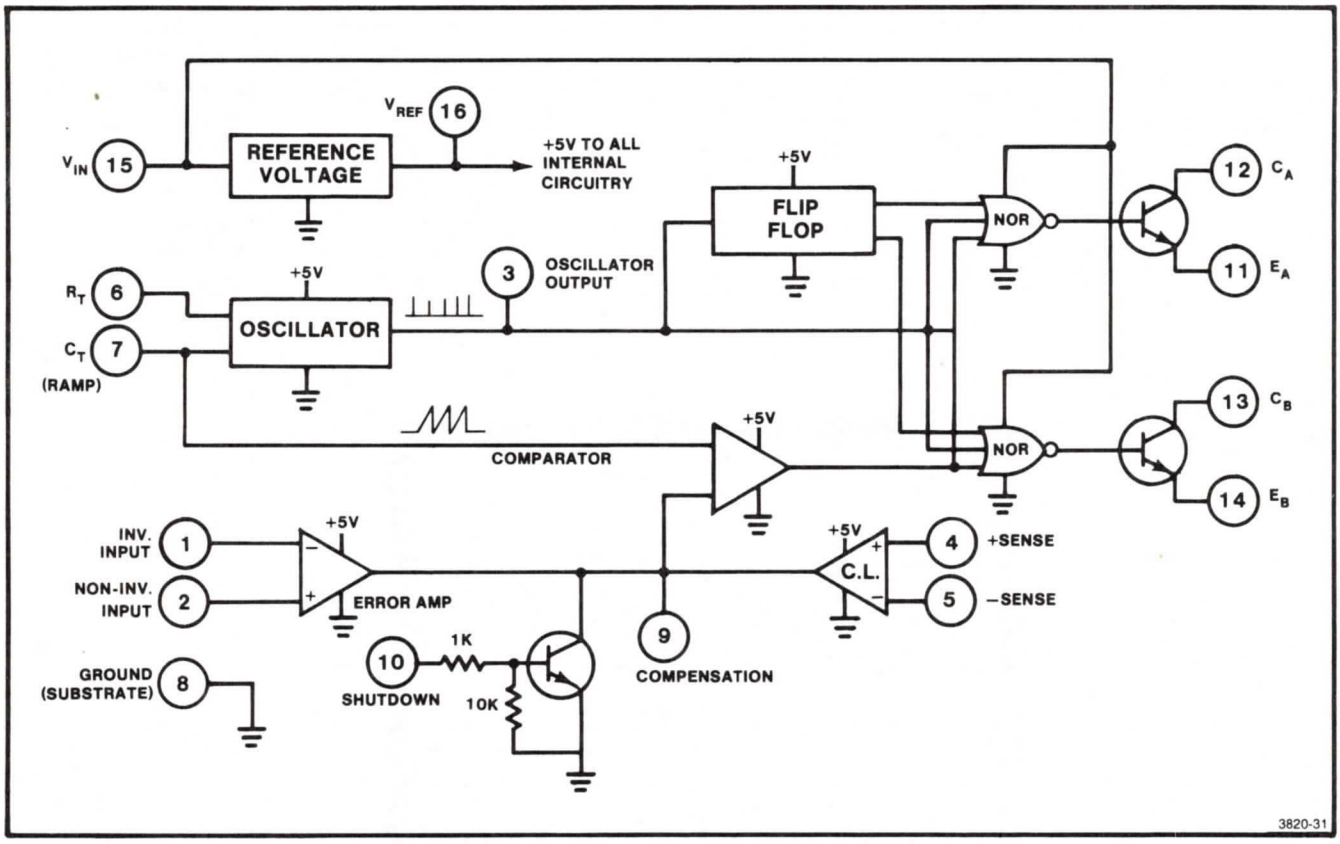


Figure 7-5. Pulse Width Modulator Block Diagram.

Four inputs go to one side of the comparator circuit. The other side goes to a frequency determining capacitor at Pin 7. The capacitor in conjunction with a resistor on Pin 6 determines the oscillator frequency of approximately 40 KHz. The oscillator output goes to a flip-flop which is used to gate the output logic for the base drivers. The oscillator also outputs to Pin 3 and goes off the board as PSYNC. Although PSYNC is not used in this terminal, it is a convenient source for a trigger for an oscilloscope.

Timing. The capacitor's charging at the input of the comparator gives a 0-3 V ramp signal. When the ramp voltage equals the input from the lowest of the other inputs, the comparator output goes low and the input to the NOR gates is low, Figure 7-6. The flip-flop alternately selects the NOR gate to be enabled and the oscillator disables the NOR gates on every discharge of the capacitor to help ensure the rapid turnoff of the switching transistors. Figure 7-6 shows the ramp signal at the top and the oscillator signal at the bottom.

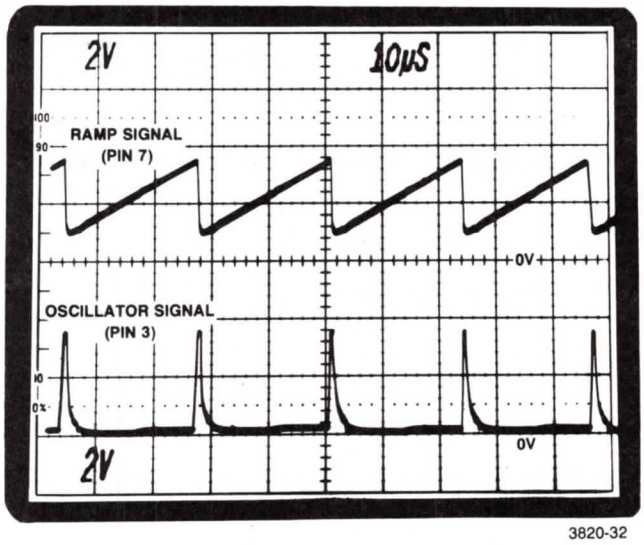


Figure 7-6. PWM Comparator Input and Oscillator Output.

Error Amplifier. The +5.1 SENSE line of the DVM provides a sample voltage from +5.1 V which goes to three places, the error amplifier, the current sense circuitry, and the shutdown circuitry. The error amplifier receives approximately 2.5 V on each of its two inputs. The +5 SENSE goes through a voltage divider network of two 1.24 K ohm resistors. At the center of these two resistors a voltage of approximately 2.5 V is fed to the inverting input, Pin 1. The non-inverting input, Pin 2, is fed from the variable side of the 5.1V adjust. The potentiometer is part of a voltage divider network off of VREF, Pin 16.

Current Sense Amplifier

Refer to the Inverter board Schematic A17-1. A current sense transformer in series with the inverter transformer drives the base of one half of a differential pair of transistors. When current increases beyond the allowable limit, one half of the pair is cut off turning the other half on. This drives the output of the limiter amplifier down and the comparator is off for an increased period of time. The output voltage is reduced which further reduces the allowed current.

Shutdown Circuits

A line voltage detector senses the line voltage on its non-inverting input and charges a capacitor on its output. When line voltage is lost, the capacitor discharges and the voltage comparator, which compares the voltage across the capacitor with the 2.5 V reference, goes low at its output. This immediately drives Pin 1 of the peripheral driver low and PFAIL-0 goes low. The voltage comparator also pulls the non-inverting input of an operational amplifier low through a diode. The output of the operational amplifier going low allows a capacitor on this output to discharge through a diode. The time delay, about 2 ms, afforded by the capacitor, ensures that PFAIL goes low first before INIT and PDWN are driven low. A capacitor on Pin 1 of the peripheral driver ensures that there is a minimum of 50 us between INIT and +5 V going down. When the collector on the PDWN peripheral driver goes low, it pulls Pin 9 of the PWM low and the base drivers are shut down. Both operational amplifier outputs to the peripheral drivers must go low to shut down the power supply.

Pressing the RESET button on the front of the pedestal under the keyboard (Figure 7-7) generates a RESET-0 signal which causes an INIT-0 signal to be initiated.

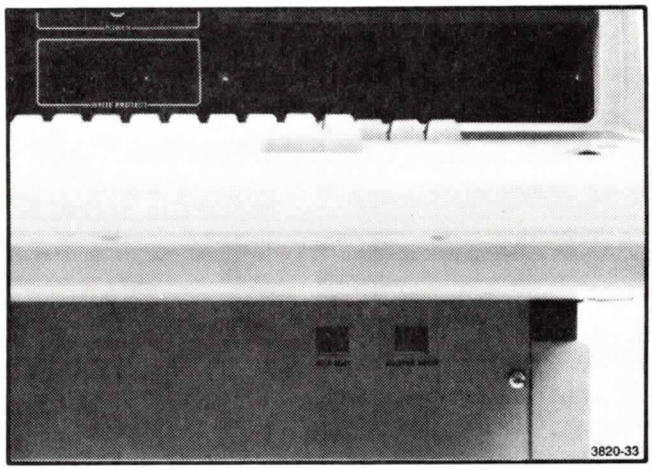


Figure 7-7. SELF-TEST and RESET Buttons.

REGULATOR BOARD

+12 V Regulated Supply

The Regulator board is best understood by looking at one regulator circuit that incorporates most of the features that are contained in all the regulators. The +12 V regulator is described in detail. Refer to Figure 7-8 when reading the following explanation.

The transformer steps the primary voltage down and the ac output is run through a bridge rectifier. The rectified dc is filtered by the LC circuit. The filtered dc is +16 V and -16 V and supplies the series pass regulator which is a Darlington transistor.

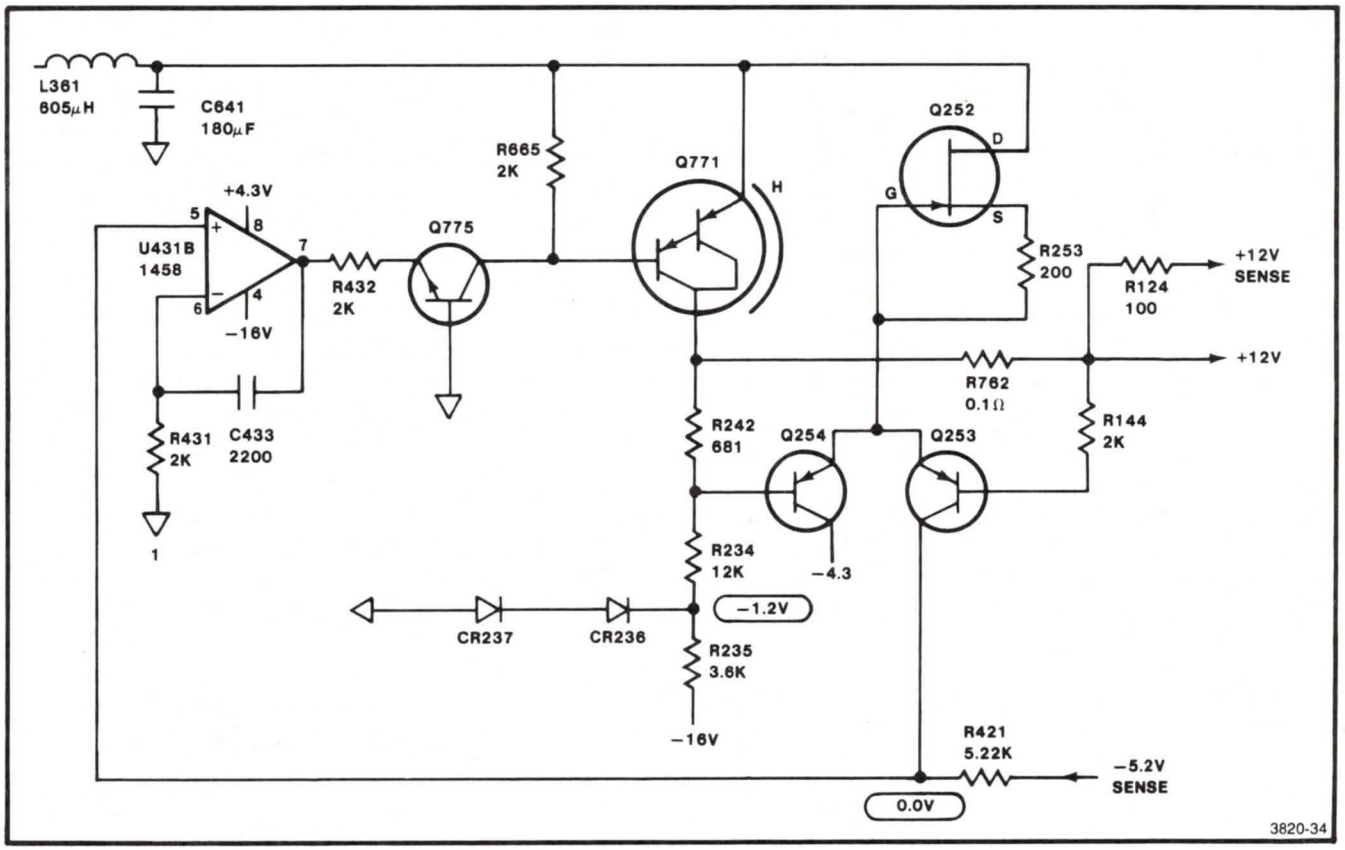


Figure 7-8. +12 V Regulator Circuit.

Overcurrent Protection

The current foldback portion of the circuit consists of the FET current source, the Comparator circuitry, the voltage divider network on the Darlington transistor's collector, the very small current sense resistor, and the diodes to ground.

At stable conditions, when the power supply is delivering 4 A at + 12 V, the transistor whose collector is tied to the non-inverting input of the operational amplifier has 12 V on its base. The Darlington transistor has 12.4 V on its collector. This 12.4 V is dropped across the voltage divider network to the -16 V supply. The two diodes hold the point above the resistor connected to -16 V at -1.2 V. The FET is connected as a current source to the emitters of the comparator transistors holding the right side cutoff. When +12 V exceeds its rated current of 4.0 A, the right side transistor is turned on and the non-inverting input goes positive. This drives the base of the Darlington transistor positive through the common base transistor reducing the output voltage.

If the overcurrent condition still exists, the voltage is further reduced as the graph in Figure 7-9 shows until the voltage reaches zero. The current is kept at some small positive value by the two diodes in the voltage divider network.

If the excessive current drain continues, the series pass transistor reduces the voltage further until the voltage is completely off.

When more current than is allowed is drawn, a situation occurs that is known as current foldback. See Figure 7-9.

Voltage Regulation

When the voltage rises above 12 V, the input to the operational amplifier goes positive which drives the operational amplifier's output postitive. The Darlington transistor's base goes positive and more voltage is dropped across the Darlington transistor bringing the output voltage back down.

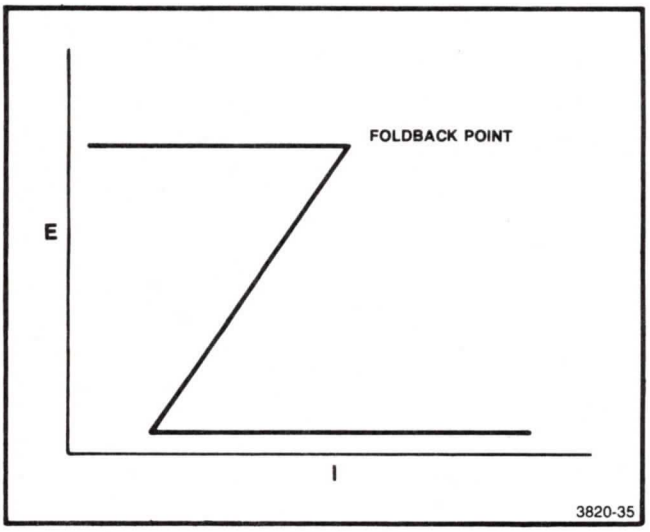


Figure 7-9. Current Foldback.

Section 8

THEORY OF OPERATION OF DISPLAY CONTROL CIRCUITRY

INTRODUCTION

The Display Control Circuitry consists of two circuit boards -- the Display Controller and the Vector Generator. The boards are connected as shown in Figure 8-1. Conversion of digital data to analog DVST display signals and control of the conversion is performed by the Display Control Circuitry.

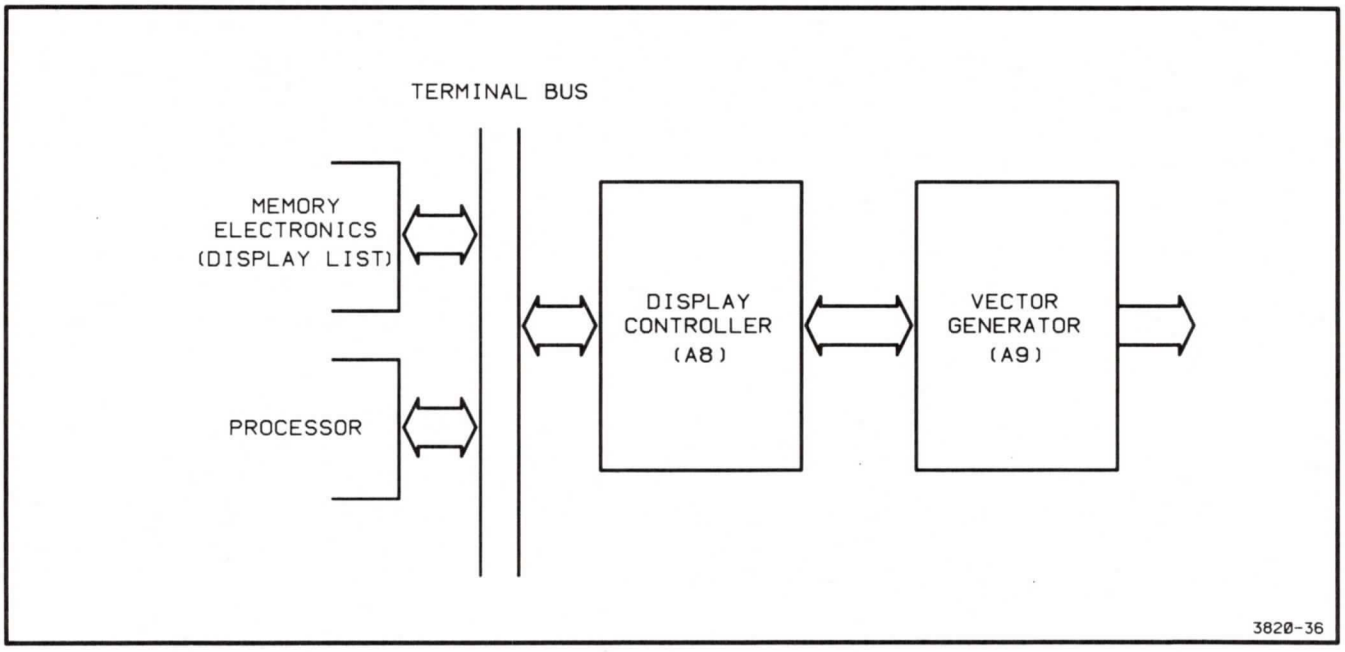


Figure 8-1. Display Control Circuitry Block Diagram.

The Display Controller performs these functions:

- Interfaces between system processor, Memory Electronics, and Vector Generator.
- Accesses Display List instructions on command from the system processor.
- Processes instructions and passes vector commands to the Vector Generator.

- Monitors Vector Generator conversion process.

The Vector Generator performs these functions:

- Executes commands from the Display Controller.
- Converts digital data to analog signals for use in the DVST Display Module.

DISPLAY CONTROLLER

The Display Controller (see Section 12) circuit board's main function is to serve as an interface between the system bus, the Vector Generator board, and several functions in the display. The controller accepts commands directly from the terminal processor and accesses commands directly from a display list stored in the terminal's main memory. These commands are then processed by the Display Controller which passes appropriate commands and data on to the Vector Generator board.

The Display Controller also controls the Z axis drive to the terminal DVST display. It turns the CRT beam on and off while vectors are drawn and when dot-dash patterns are formed.

The following circuit descriptions are referenced to the block diagrams; detailed diagrams and illustrations are provided where applicable. Compare the block diagrams with the actual Display Controller schematics (Volume 2) to get a clear understanding of the actual circuit layout and to become familiar with the schematics.

The theory of operation is presented in the following order:

- Processor Interface
- Command Decoding
- DMA Control
- Addressing Control
- Vector Control

The simplified block diagram (Figure 8-2) shows the relationship between major blocks of the Display Controller logic, the system bus, and the Vector Generator. The data busses are labeled while the smaller busses represent

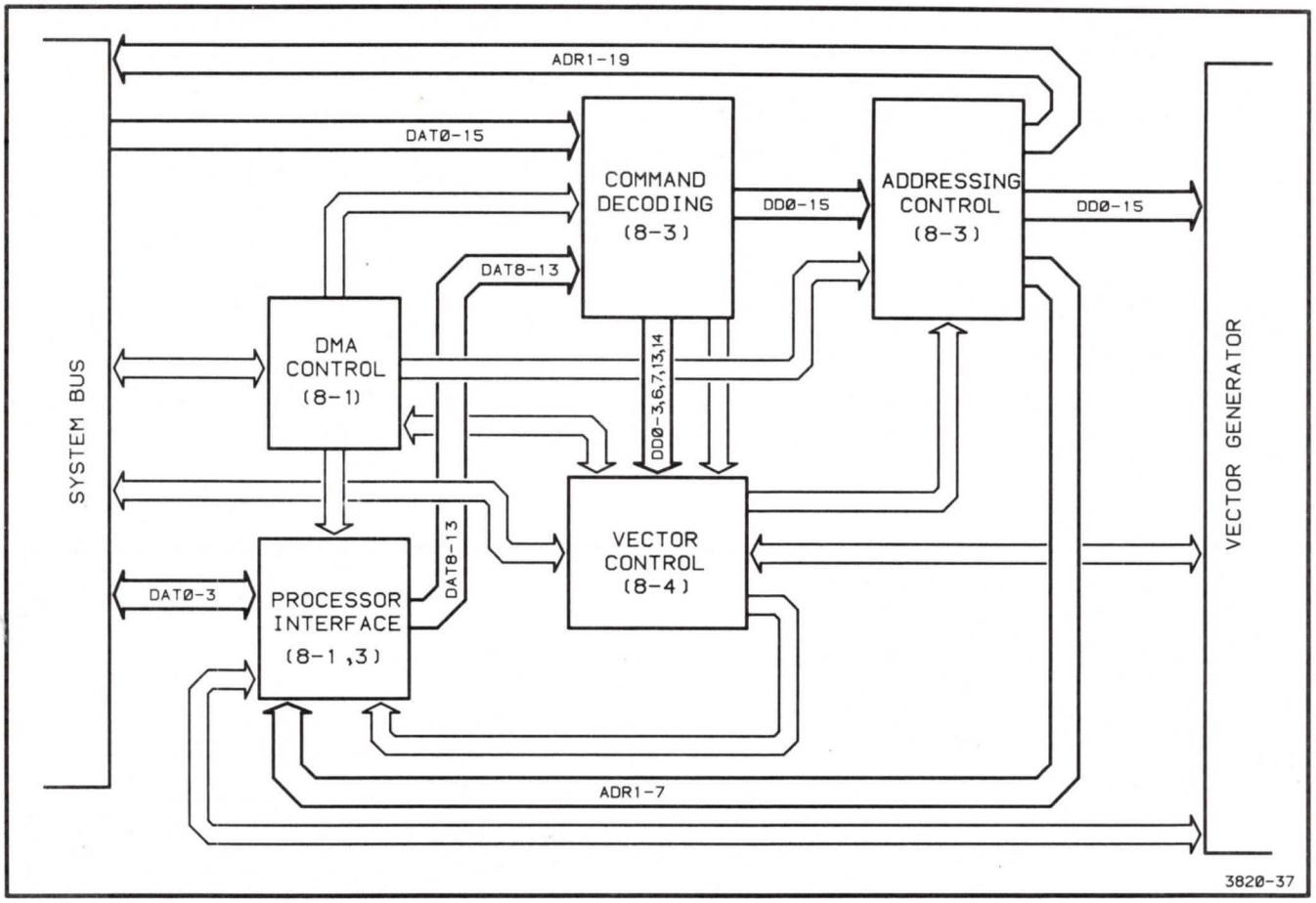


Figure 8-2. Display Controller Simplified Block Diagram.

Read/write signals from the system processor are received by the Processor Interface. The Display Controller and Vector Generator status is also read by the interface logic. The Command Decoding logic decodes display list commands and routes them to appropriate circuits for execution. Bus control and data accessing are provided by the DMA Controller. The Addressing Control Logic performs address incrementing and subroutine jumps. Logic which controls the copy, erase, dot-dash generation, and vector timing display functions is contained in the Vector Control block. This is an overview of the Display Controller board functions which are explained in the block diagram descriptions.

Address Decode

Figure 8-3 shows a simplified block diagram of the Processor Interface logic; refer to it during the following discussions.

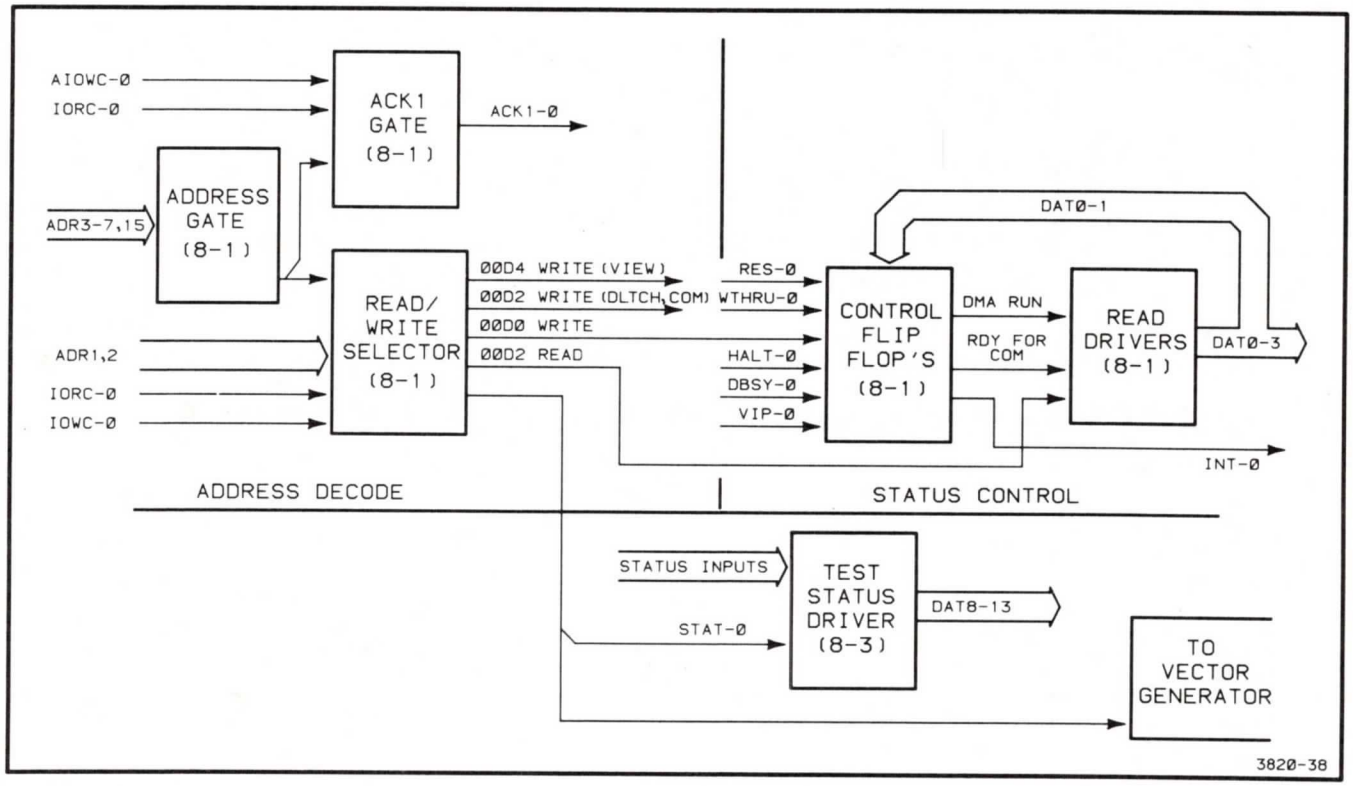


Figure 8-3. Processor Interface Simplified Block Diagram.

The Address Decode logic monitors the address lines originating on the system bus and detects when the system processor is addressing the Display Controller. When ADR3 is ~~zero~~ normal (or one depending on the A3 strap) ADR4,6,7 are one, and ADR5 and 15 are zero, the gate output goes low indicating that the processor is addressing locations 00D0 to 00D7 (or 00D8 to 00DF for the other A3 setting). If this occurs concurrently with either the AIOWC or IORC signals, the ACK1 signal is asserted indicating to the processor that a data transfer command has been acknowledged.

When IORC is low signifying a bus read (board places data on the bus) and the Address Gate output is low, the Read/Write Selector is in Read mode. If ADR1 and 2 are low, the 00D0 Read line will go low causing the Read drivers to drive the DAT0-3 lines. If ADR1 is high and ADR0 is low, 00D2 Read goes low causing a Test Status Driver read to occur.

Similarly, when the IOWC signal is asserted, the Read/Write Selector activates the write outputs; the 00D0 Write line activates the Control Flip Flop logic; 00D2 Write activates the DLTCH and COM signals in the Command Decode logic; and 00D4 activates the VIEW signal. Table 8-1 lists special input/output locations and their functions. Table 8-2 shows test bits and their functions for the 00D2 Read location.

Table 8-1

SPECIAL I/O LOCATIONS

I/O Location	Operation	Bit Value
00D0	READ	0: Display list in process 1: Ready for command 2: Hard copy unit available 3: Vector in progress
00D0	WRITE	0: Interrupt enable 1: Operation display list
00D2	WRITE	Direct command
00D2	READ	Test bits (see Table 8-2)
00D4	WRITE	Bring display into view

Table 8-2

TEST BIT MEANINGS IN I/O LOCATION 00D2

Bit(s)	Signal Name	Meaning
15,14		Unused.
13	Z-0	Z axis control at the output of the display controller board (before clipping).
12	A1-1	The least significant bit of the display controller address counter.
11	SLU-0	The slew signal from the display.
10	DBUSY-0	The display busy signal from the display. This occurs during erase, during the making of a copy, and when the display is in hold mode.
9	LJUMP-1	The first word of a long jump command has been received.
8	LVECT-1	The first word of a long vector command has been received.
7,6		Unused.
5 4	X12-1 Y12-1	The most significant bits of the vector generator counters.
3	MX11-1	The most significant bit of the X latch.
2	GRUN-1	Vector is being drawn.
1	VAVIL-1	A vector is available for vector set up.
0	MY11-1	Most significant bit of the Y latch.

NOTE: These status bits are readable at I/O location 00D2. They should only be used for test purposes.

Status Control

The Control Flip Flop logic provides the DMA Run, Ready for Command, and Interrupt Enable signals. The DMA Run signal tells the DMA Control logic when to run during a display list access sequence. It is also gated with the WTHRU and 00D4 Write signals to generate the VIEW signal for use in the DVST display circuitry. The Ready For Command signal is gated with the Interrupt Enable signal to produce the bus interrrupt (INT) signal. The DMA Run signal goes low when either the RES or HALT signals are asserted.

Test Status Driver

The Test Status Driver allows the system processor to read the status of several signal lines. The status of these lines is written on the system bus (DAT8-13) when the STAT signal goes low during 00D2 Read (see Tables 8-1,8-2).

Command Latch

The Command Latch temporarily holds command data from the sys- tem bus. This data is originated by either the system proc- essor or accessed by the Display Controller DMA Control logic. The DLTCH signal latches the 16 data bits from the system bus to the data bus.

Initiate Command

This logic generates the COM signal which is a pulse of about 200 ns duration. This signal is used in the Command Decode logic and is activated by either the DMA Control or Address Decode logic (00D2 Write).

Flip flops A and B in Figure 8-4 make up the logic for generating the COM signals. Initially, DLTCH goes low (triggered by the Address Decode or DMA Control logic) and then goes high. This sets flip flop A putting a high at the D input of flip flop B. The next rising edge of the CLK signal sets B which then resets A (Q goes low). After approximately 200 ns the CLK signal goes high again resetting B (Q goes low). Thus, the output of B is a pulse of about 200 ns duration.

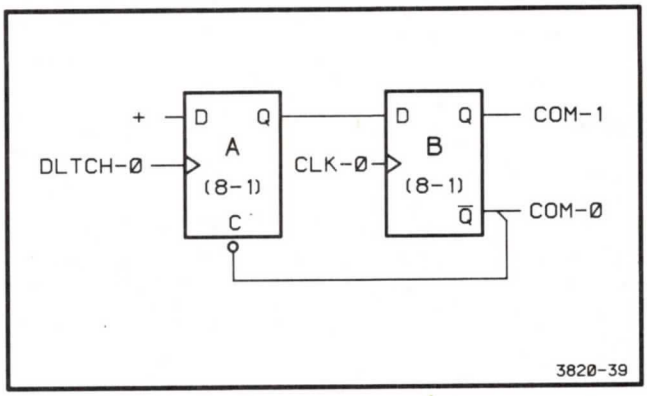


Figure 8-4. Initiate Command Logic Diagram.

Command Decode

The Command Decode logic decodes command data from the Command Latch and then executes the decoded commands. The COM signal initiates the command operation (see Figure 8-5).

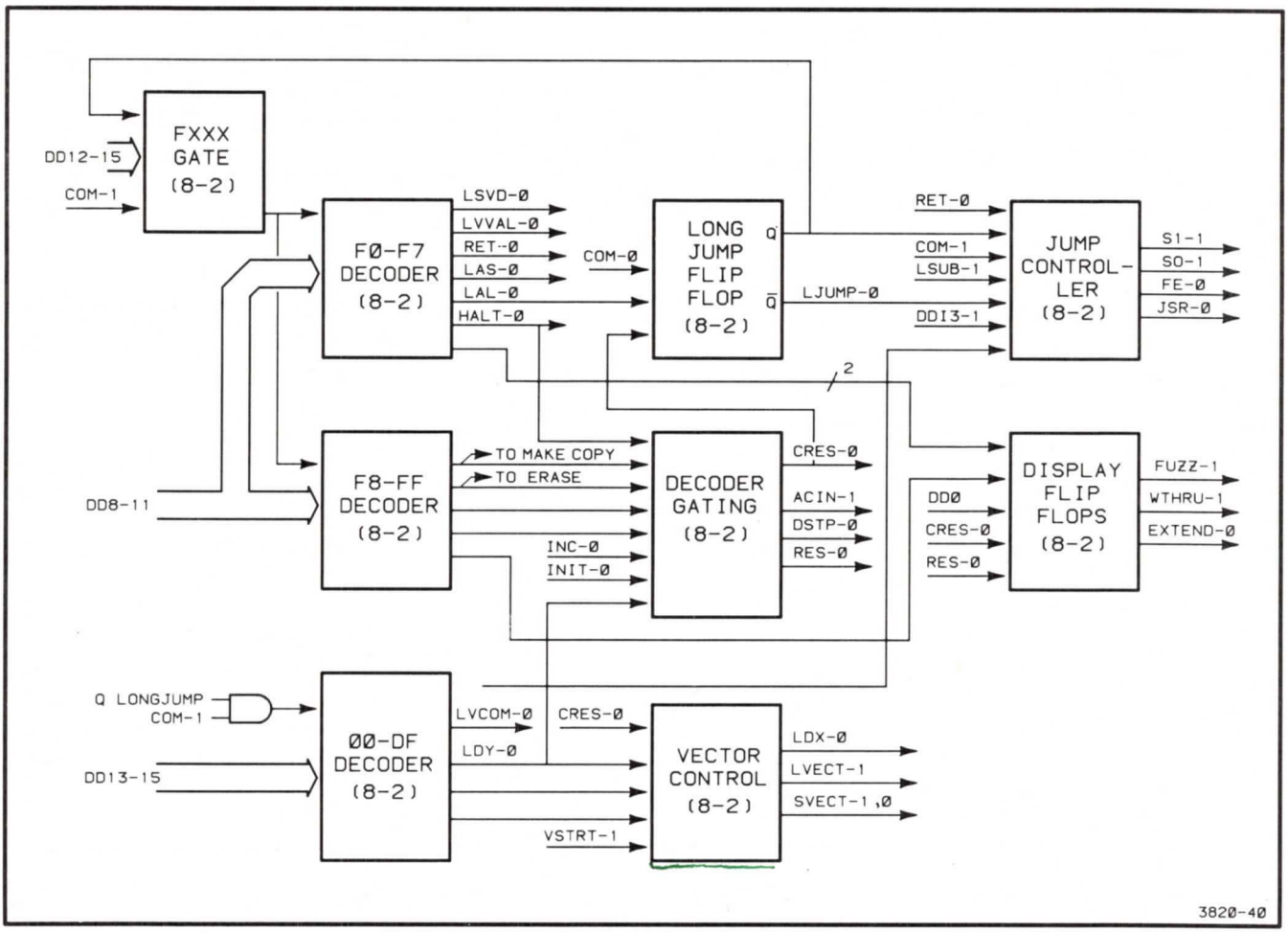


Figure 8-5. Command Decode Logic Diagram.

There are 14 commands (see Display List Summary) of FXXX (F000-FFFF) format used in the Command Decode logic. The F0-F7 and F8-FF Decoders are enabled when the FXXX Gate detects that: DD12- 15 are ones; the second word of a long jump command is not expected; and the COM-1 signal is asserted. The F0-F7 Decoder decodes commands F0XX to F7XX. The F8-FF Decoder decodes commands F8XX to FFXX. And the 00-DF Decoder decodes commands 00XX to DFXX.

F0XX is decoded HALT which causes the Status Control logic to halt the DMA run operation. Halt is also gated with other signals to produce the DSTP signal.

F1XX is decoded LAL which clears the Long Jump Flip Flop and latches the first word of a two-word command into the addressing control logic. LJUMP is asserted indicating that the second word of a long jump is expected. After receiving the long jump command, the next word is the second word of the jump which supplies the remaining 16 bits of the jump address. Since the Long Jump Flip Flop is cleared (Q low as shown in Figure 8-6), the second word is prevented from being interpreted as any other type of command.

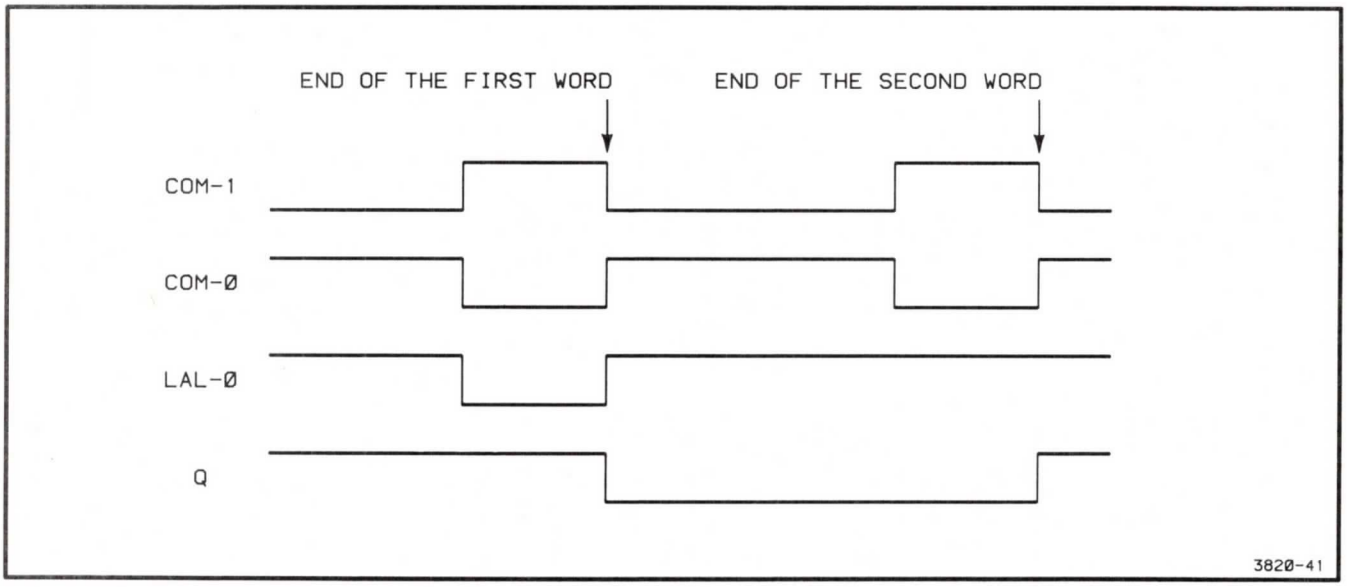


Figure 8-6. Long Jump Timing Signals.

When the COM-1 signal occurs with the second word, the Jump Controller asserts S1 and S0 and uses the LSUB signal to select between a normal jump (FE=1, JSR=1, RET= 1) and a subroutine jump (FE=0, JSR=0, RET=1). At the end of the second word the Long Jump Flip Flop is reset for a new word command cycle.

F2XX is decoded LAS which loads eight bits of the short jump address into the Character Location Register in the Jump Address Latches.

F3XX is decoded RET causing the Jump Controller to generate S1=1, S0=0, and FE=0.

F4XX causes DD0 to be loaded into the Display Flip Flops which controls defocus (FUZZ).

F5XX causes DD0 to be loaded into the Display Flip Flops which controls write through (WTHRU).

F6XX is decoded LVVAL for use in the Dot-Dash Generator logic.

F7XX is decoded LVSD for use in the Vector Generator scaling logic.

F8XX causes DD0 to be loaded into the Display Flip Flops which controls the EXTEND signal.

F9XX activates the Make Copy logic. It also temporarily halts the DMA Control state machine.

FAXX activated the Erase logic. It also temporarily halts the DMA Control state machine.

FBXX activates a limited reset (CRES) signal.

FEXX has no connection. It is a no-operation (NO-OP).

FFXX activates the ACIN signal. The word after the FFXX command is skipped.

The 00-DF Decoder detects a short jump when DD15=1, DD14=0 (commands 8XXX through BXXX), the second word of a long jump is not expected, and the COM-1 signal is high. The Jump Controller asserts S1 and S0 similarly to the second word of a long jump. It uses DD13 to select between normal (FE=1, JSR=1, RET=1) and subroutine jumps (FE=0, JSR=0), RET=1).

The first word of a long vector command (CXXX through DXXX) is detected when DD13=0, DD14=1, DD15=1, the second word of a long jump is not expected, and the COM-1 signal is high. When this occurs, the LDX signal is sent to the Vector Generator causing the least significant 13 bits of the command to be latched. Also, the Vector Control asserts LVECT indicating receipt of the first word of a long vector.

When the 00-DF Decoder detects that DD15=0, the second word of a long jump is not expected, and the COM-1 signal is high, a short vector or second word of a long vector is indicated. The Vector Control logic determines which vector format is called for. A long vector generates LDY and drives SVECT low. A short format vector generates both LDX and LDY and asserts SVECT. The buffered COM-1 signal, LVCOM, is for future options.

DMA Control

The DMA Control logic, upon command from the system processor, allows the Display Controller to read information from any memory location available on the system bus. A state machine, composed of three flip flops and associated gates, performs the control operations. The six states of the machine are:

A	000	Waiting for vector set-up circuitry to get ready for new data and DMA Run to be asserted.
B	001	Bus request (BREQ-0) asserted to system bus.
C	011	Bus busy (BUSY-0) indicates Display Controller is using bus; address of command to be processed is latched.
D	111	Memory read command (MRDC-0) instructs memory to place data on to system bus.
E	110	Increment to next address, data is latched.
F	010	Command operate (COM-1) asserted on next state machine cycle.

The complete state machine operation is shown in the flow chart in Figure 8-7. The circles contain a letter for each state. Adjacent to each circle is the condition of the three flip flops which determines the state. The diamonds indicate conditional transitions between states controlled by signals entering the machine. The rectangles contain the names of signals coming out of the machine. All signal lines are shown in the DMA Control block in Section 12.

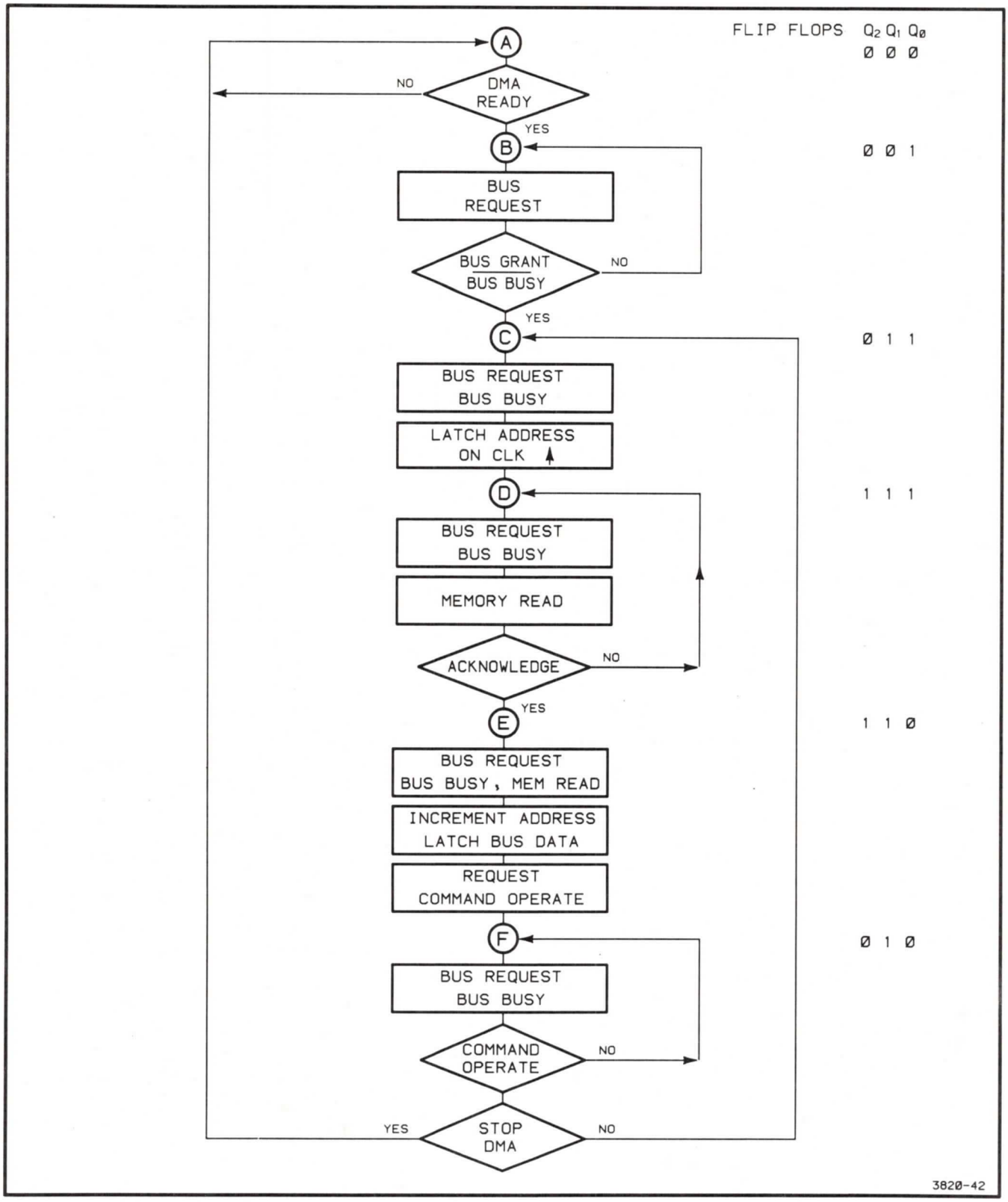


Figure 8-7. Display Controller State Machine Flow Chart.

Jump Address Latches

This logic holds jump address information during long and short data jumps. The Character Location Register (see Figure 8-8) holds data stored for a short jump. During a long jump, the Long Jump Latch latches data bits for the first word of the long jump command.

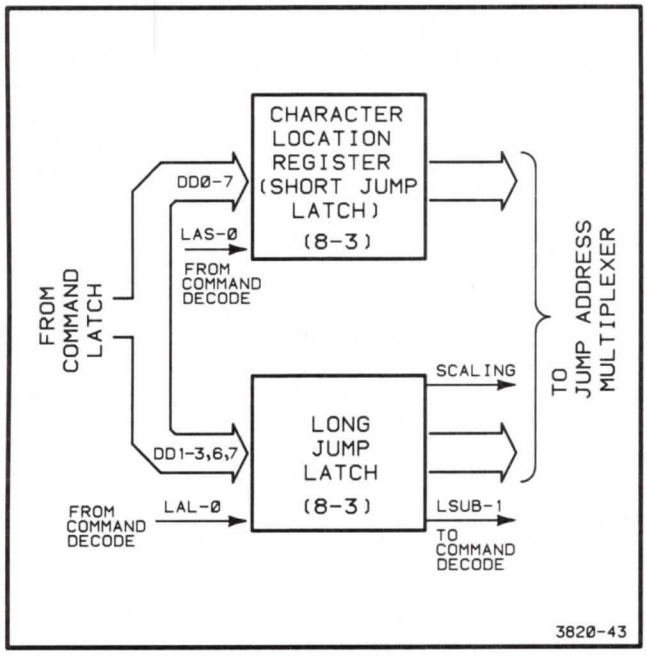


Figure 8-8. Jump Address Latches Logic Diagram.

The least significant eight bits (DDO-7) of the Load Character Location Register command are latched by the Character Location Register. This occurs when LAS is asserted after the Load Character Location Register command is decoded by the Command Decoder. The latched bits (ADR12-19) are fed to the Jump Address Multiplexer.

During the first word of a long jump command, LAL is asserted causing the Long Jump Latch to latch its data. Three address bits, ADR1-3, and the scaling bit are fed to the Jump Address Multiplexer. The LSUB signal is used in the Command Decode for second word subroutine jumps.

Jump Address Multiplexer

Jump address data is located in different positions in the command word for short and long jumps. The multiplexer logic selects the appropriate bits in the command word for the Address Controller (see Figure 8-9).

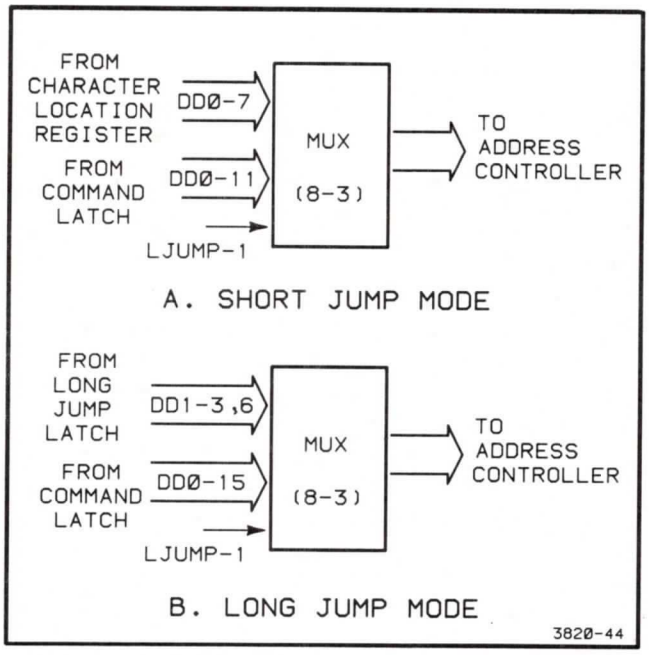


Figure 8-9. Jump Address Multiplexer Modes.

In the short jump mode, the LJUMP signal is low causing the MUX to select bits DD0-7 from the Character Location Register. Bits DD0-11 from the Command Latch are also selected.

When the LJUMP signal is high, bits DD1-3 (corresponding to the first word of the long jump) are selected. The scaling bit, DD6, is passed on to the Scaling Control logic. Second word bits DD0-15 from the Command Latch are also selected in the Long Jump mode.

Address Controllers

The Address Controllers keep track of the addresses accessed by the DMA Control during DMA operations. The controllers provide:

1. access to sequential addresses;
2. jumps to non-sequential addresses;
3. subroutine jumps in which the next sequential address is stored on a stack before the jump is performed and
4. subroutine returns in which the address of the next location to be accessed is taken from the top of the stack.

Five address controllers connected in cascade are contained in this logic block; each one controlling a 4 bit slice of the address being accessed. Thus, 19 most significant bits of the 20 bit address are used while the least significant bit (bit 0) is con- sidered to be zero. A scaling bit is also processed in the MSB of the last controller as a 20th bit. The bit is described in the Scaling Control section.

Figure 8-10 shows a simplified logic diagram of an address controller. The Counter Register holds 4 bits of address data at all times. With each rising edge of the CLK signal, the Incrementer output is loaded into the register. Register loading is controlled only by the CLK signal.

The Incrementer is controlled by the ACIN signal. When ACIN is low, the Incrementer passes its input data to its output (and the Counter Register) unmodified. When ACIN goes high, the input data is incre- mented by 1 and passed to the Counter Register. The incremented carry is fed to the next controller in cascade.

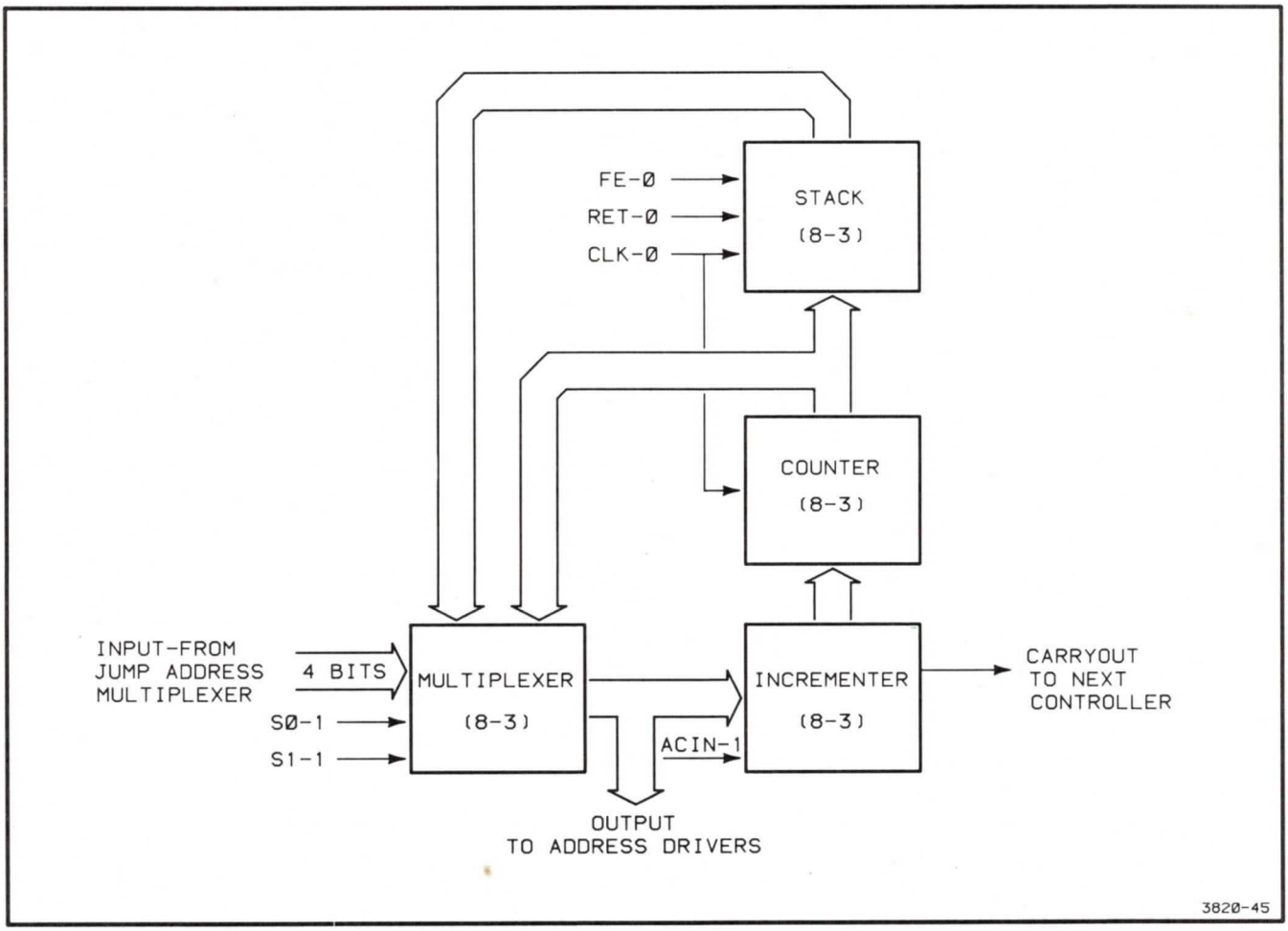


Figure 8-10. Address Controller Simplified Logic Diagram.

Input data for the Incrementer (which is also the controller output as shown in Figure 8-10) is provided by the Multiplexer from three sources. These sources (selected by the S0 and S1 signals) are: 1) The Jump Address Multiplexer providing for jump operations; 2) The Counter Register providing for progression to the next sequential location (ACIN=1) or to stay at the same location (ACIN=0) to allow for completion of the command in progress or other delays; and 3) The Stack-which stores 4 levels of data pushed on it. During a subroutine jump, the next address that would have been accessed is pushed on this stack. When a subroutine return is performed later, the top entry of the Stack is "popped" into the Counter Register via the Multiplexer. The FE and RET signals control the Stack.

Table 8-3 lists the controller operations and signal levels.

Table 8-3

CONTROLLER OPERATIONS AND SIGNAL LEVELS

Operation	S1	S0	CIN	FE	RET
Stay Put	L	L	L	H	X
Next Address	L	L	H	H	X
Normal Jump	H	H	L	H	X
Subroutine Jump	H	H	L	L	H
Subroutine Return	H	L	L	L	L

H=High Signal L=Low Signal X=Don't Care

Scaling Control

The logic shown in Figure 8-11 monitors the scaling status and determines if scaling is needed. Scaling status changes only during subroutine jumps and returns. During a subroutine jump, the scaling bit is controlled by the jump command signal, JSR. For a subroutine return, the bit level is controlled by the status of the top address in the Address Controller stack.

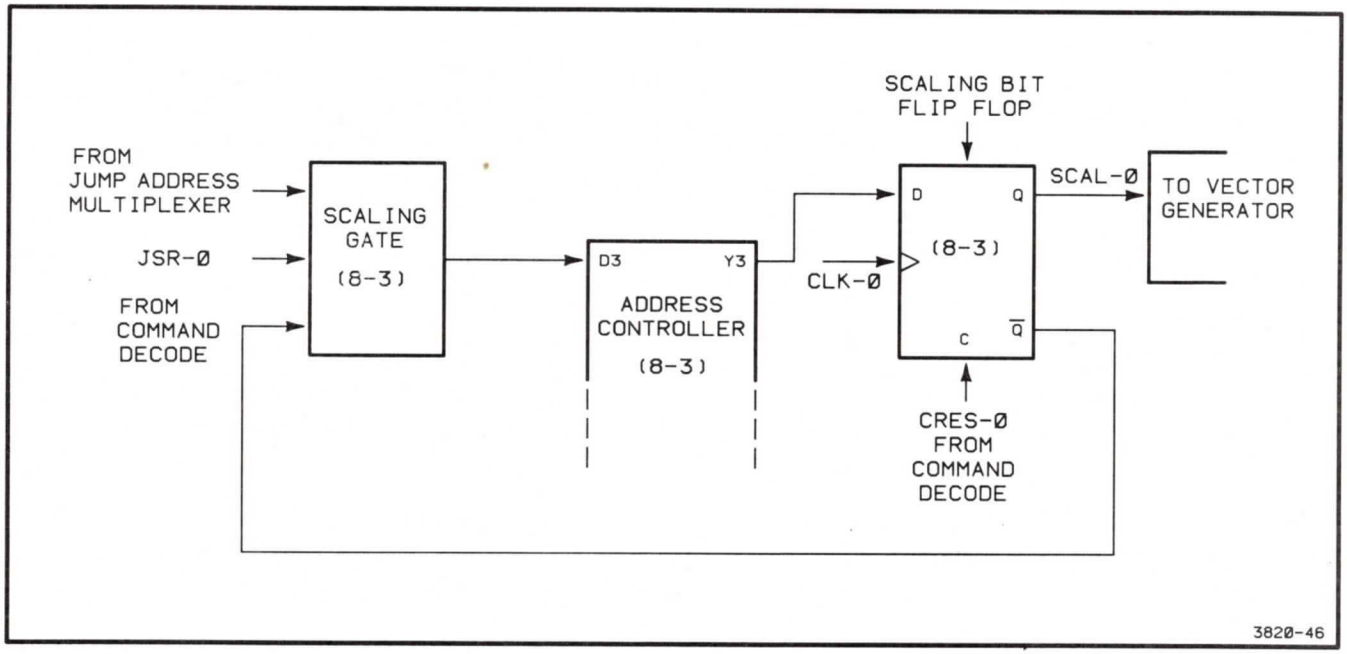


Figure 8-11. Scaling Control Logic Diagram.

The CLK signal loads the Scaling Bit Flip Flop with the MSB (Y3) of the Counter Register in the Address Controller. The Counter Register input (D3) is loaded with the output of the Scaling Gate during subroutine jumps. During normal jumps, this data will be essentially the SCAL signal (Q[bar] high is inverted in the Scaling Gate). Thus, the Counter Register bit will be loaded with the Scaling Bit Flip Flop Q[bar] output and the scaling control signal will remain unchanged. During a subroutine jump, the JSR signal gates the Jump Address Multiplexer data bit to the Scaling Gate inverted output. The next clock cycle after the one that performs the jump causes the Scaling Bit Flip Flop Q output to match this bit value.

During a subroutine return, popping the Address Controller stack causes the scaling bit to return to the value it was just before the last subroutine jump. The next positive clock transition causes the flip flop to follow.

Address Drivers

The Address Drivers provide an interface between the Address Controllers and the system bus. The drivers capture the controller output and then latch the data onto the bus as directed by the DMA control logic.

When ALTCH goes high, the drivers follow their inputs, When ALTCH goes low, the drivers hold their input data. The OUT signal latches the drivers outputs onto the bus when it is low.

Vector Control Pipeline Register

This logic latches and holds control signals for use in the Vector Timing logic. These signals are held in the "pipe-line" during the drawing of a vector. The signals are latched on the rising edge of VSTRT at the beginning of a vector.

Vector Timing

A time delay exists between the instant the Vector Generator calls for a change in the CRT deflection voltage and the instant the writing beam starts moving on the CRT display. The Vector Timing logic compensates for this delay and also keeps the CRT beam on for a short period after the Vector Generator stops running. It also compensates for delay differences between write through vectors and storage mode vectors. Write through vectors require a start delay and stop extend; stored vectors require only a longer stop extend.

Slew timing compensation is also provided by this logic. Slewing occurs when the CRT deflection output rate lags the input rate during absolute moves. The slew logic is enabled only during absolute moves; relative moves and draws are slow enough for the deflection circuits to follow without delay.

The following paragraphs describe the logic functions during various modes of operation (see Figure 8-12).

Zero length move in storage mode: At the start of a vector, VSTRT is asserted which triggers the Hold Off One Shot. Q[bar] goes low presetting the VIP Latch. After the Hold Off One Shot time delay (0.3 us to 1.2 us), the One Shot Gate output goes low triggering the SE (Storage Extend) One Shot. About 5 usec later, the SE One Shot Q output goes low clocking the VIP Latch and clearing its outputs (VIP low, VIP-0 high). Thus, during the time the VIP Latch is set (5 usec plus 0.3 usec to 1.2 usec) the VIP and GBSY signals are asserted. The Z signal remains high because the ZAX-1 signal stays low.

Zero length move in write through mode: VSTRT goes low triggering the Hold Off One Shot and setting the VIP Latch. After the Hold Off delay, the Hold On One Shot is triggered. After the Hold On delay, the VIP Latch is clocked clearing its output (VIP low, VIP-0 high). The SE One Shot's output is disabled because the WRITETHRU signal is low. Thus, the VIP and GBSY signals are asserted during the Hold Off and Hold On time delays. Z remains high because the ZAX-1 signal stays low.

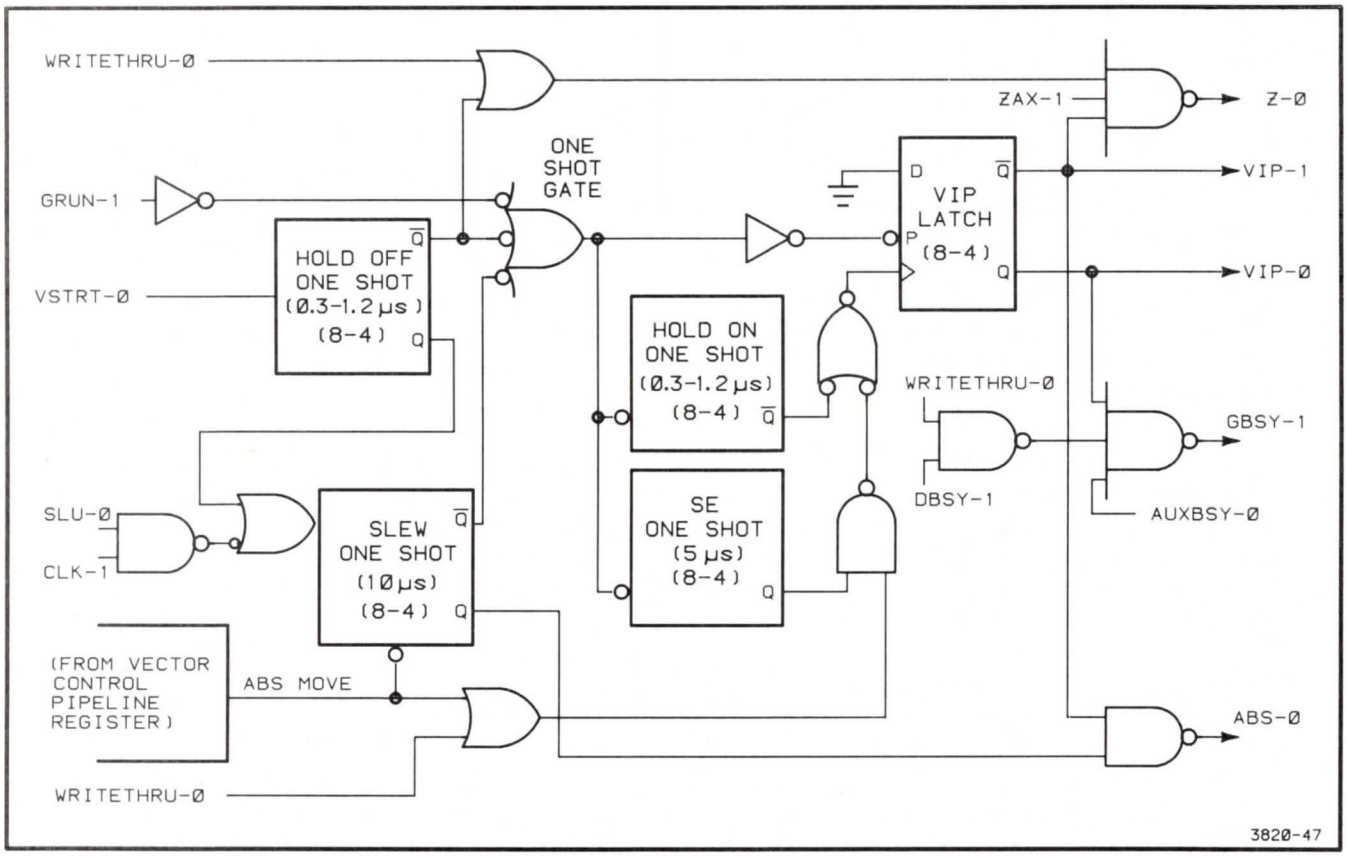


Figure 8-12. Vector Timing Simplified Logic Diagram.

Zero length vector in storage mode: VSTRT goes low triggering the Hold Off One Shot and setting the VIP Latch; the Z,VIP,and GBSY signals are asserted. After the Hold Off delay, the SE One Shot is triggered. After the SE delay, the VIP Latch is cleared and the VIP and GBSY signals become unasserted. The Z signal goes high.

Zero length vector in write through mode: VSTRT goes low triggering the Hold Off One Shot and setting the VIP Latch. The VIP and GBSY signals are asserted. After the Hold Off delay, the Z signal is asserted and the Hold On One Shot is triggered. After the Hold On delay, the VIP Latch is cleared. The VIP, GBSY, and Z signals become unasserted.

Non-zero length vector in storage mode: VSTRT goes low, GRUN goes high, the Hold Off One Shot is triggered and the VIP Latch is set. At the end of the Hold Off delay the Z signal is asserted when ZAX-1 is high. When GRUN goes low (indicating that the vector is complete), the SE One Shot is triggered. After the SE delay, the VIP Latch is cleared and the VIP, GBSY, and Z signals are unasserted.

Non-zero length vector in write through mode: VSTRT goes low, GRUN goes high, the Hold Off One Shot is triggered and the VIP Latch is set. At the end of the Hold Off delay the Z signal is asserted when ZAX-1 is high. When GRUN goes low (indicating that the vector is complete), the Hold On One Shot is triggered. After the Hold Off delay the VIP Latch is cleared and the VIP, GBSY, and Z signals are unasserted.

Absolute positioning - SLU unasserted: VSTRT goes low triggering the Hold Off One Shot and setting the VIP Latch. The VIP and GBSY signals are asserted. The Slew One Shot is triggered causing the ABS signal to go low (see Figure 8-13). After the slew delay, the SE One Shot is triggered and ABS goes high. At the end of the SE delay, the VIP and GBSY signals become unasserted.

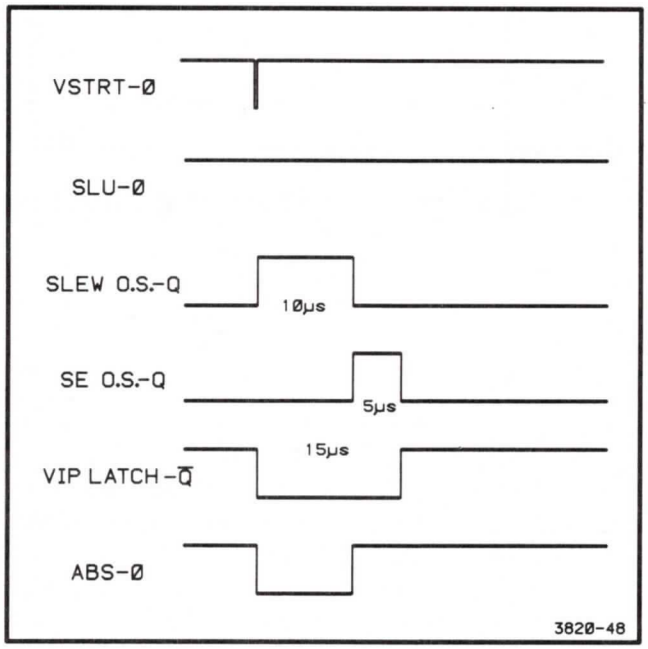


Figure 8-13. Timing Diagram for Absolute Positioning Without Slewing.

Absolute positioning - SLU asserted: Operation in this mode is the same as the above with the exception that the Slew One Shot continues to be triggered until the SLU signal goes high. The Slew One Shot then starts its time delay cycle (see Figure 8-14). The SLU signal is asserted for a period T by the display logic when the beam has not yet reached its proper position. The signal occurs only during an absolute move and is slightly delayed from the VSTRT signal.

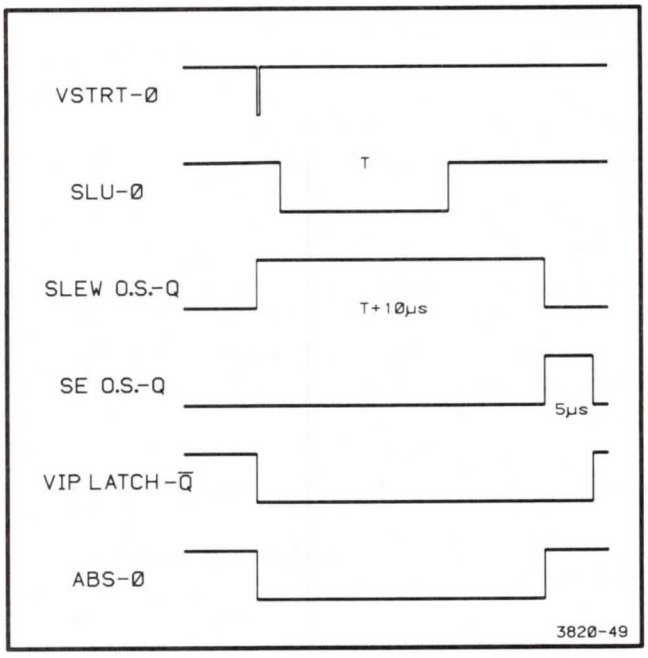


Figure 8-14. Timing Diagram for Absolute Positioning With Slewing.

Dot-Dash Generator

The Dot-Dash Generator produces dot-dash display patterns by interrupting the CRT beam at programmed intervals. The rate and length of the intervals is determined by the DCLK and display data command signals. Since vectors that are stored on the screen are drawn slower than invisible (move) or write through (refreshed) vectors, the DCLK rate is changed from 6 MHz to 1.5 MHz to accommodate the slower drawing speed. The DCLK signal is disabled when relative moves or draws are not being performed.

The logic shown in Figure 8-15 operates in two different modes: The storage mode and the write through mode. In the storage mode, the DCLK signal driving the Storage - N Counter runs at 1.5 MHz.

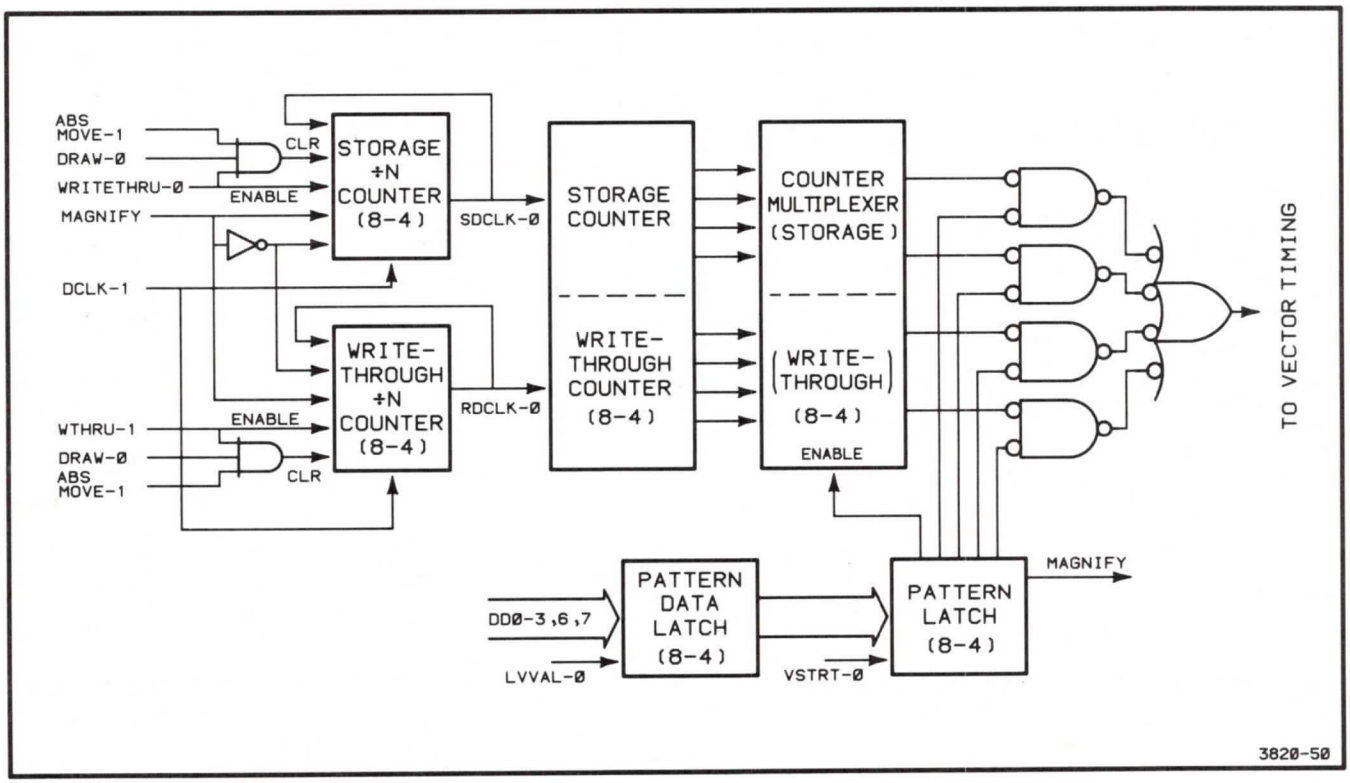


Figure 8-15. Dot-Dash Generator Simplified Logic Diagram.

When a load vector value command is executed, LVVAL goes low. The eight least significant bits of the command are latched into the Pattern Data Latch. At the beginning of a vector, VSTRT is asserted latching the data into the Pattern Latch.

As the vector is drawn, DCLK clocks the Storage - N Counter at a 1.5 MHz rate. The counter divides by 5 or 10 depending on the state of the magnify line (1=divide by 10). The SDCLK output drives the Storage Counter where it is divided down by 16. The four outputs of the Storage Counter are selected by the Counter Multiplexer and used to drive the output gates of the generator. Command pattern data is OR'd with the multiplexed output to generate the dot-dash information for the Vector Timing logic.

When a move operation occurs, the counters are cleared to receive new pattern information for the next vector.

A solid vector will be drawn when bit 7 of the load vector value command is 0 and any of its LSB's are 0.

HCU Availability

This logic determines if a hard copy unit is attached to the terminal and is ready for making copies. A signal is generated to tell the terminal when the attached unit is ready to copy. See Figure 8-16.

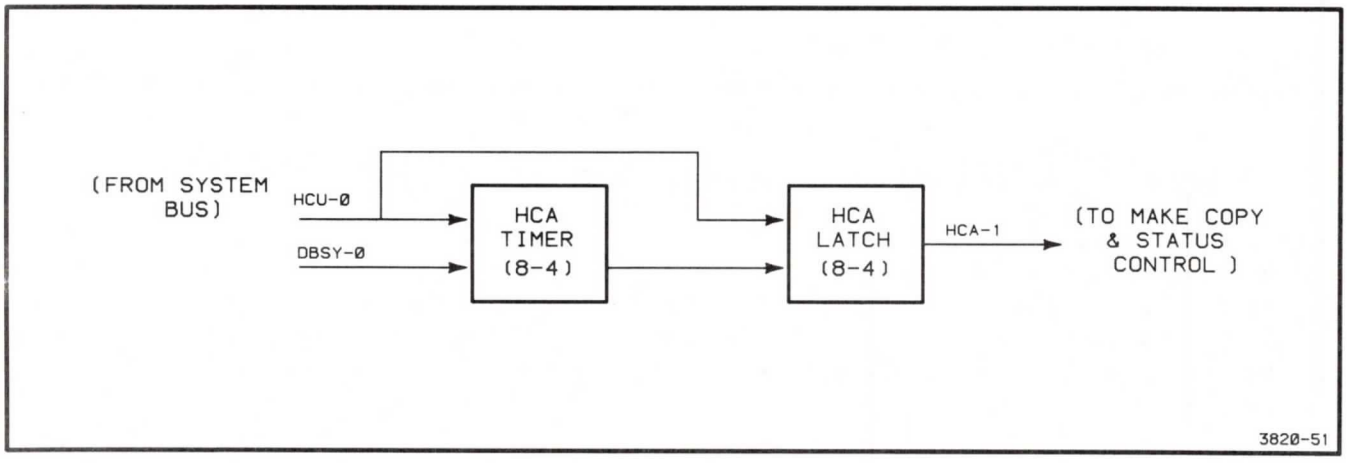


Figure 8-16. Availability Simplified Logic Diagram.

The HCA Latch asserts HCA when HCU goes low indicating a hard copy unit is attached. The latch is always set when HCU is asserted and is not affected by DBSY going low. If both HCU and DBSY go high, the output of the HCA Timer goes low after about 8 seconds and resets the HCA Latch. Thus, HCA goes low indicating that no hard copy unit is attached to the ternminal.

Make Copy

The Make Copy logic generated the MAKECOPY signal on command from the Command Decode logic. The HCA signal must be asserted before the MAKECOPY signal is generated. See Figure 8-17.

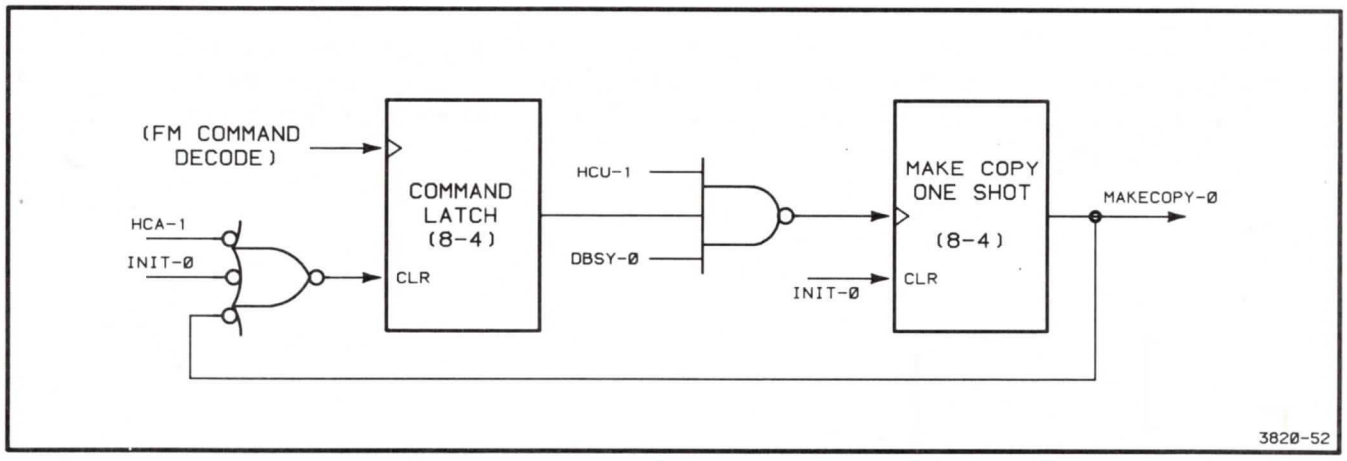


Figure 8-17. Make Copy Simplified Logic Diagram.

The Command Latch output sets high upon command from the Command Decode logic. With HCU-1 high (indicating that the hard copy unit is attached and ready) and DBSY high (indicating that the display system is ready), the Make Copy One Shot receives a trigger. A 5 msec MAKECOPY pulse is generated. The MAKECOPY pulse clears the Command Latch for the next command cycle. Note that the HCA and INIT signals also clear the latch.

Erase

This logic latches the erase command and generates the ERASE pulse for initiating the erase operation. Upon receipt of the erase command from the Command Decode logic and with DBSY high, the 25 usec ERASE pulse is generated. The logic is self clearing and the pulse width is not critical -- between 10 usec and 1 msec. The INIT signal also clears the Erase logic.

Ready For Vector

The Ready For Vector gate monitors a portion of the make copy/ erase logic output. The gate asserts the RFV signal if no make copy or erase operation is in progress or no vector is available.

VECTOR GENERATOR

The Vector Generator (see Section 12) performs the operations necessary to execute commands from the Display Controller and to convert its data into analog signals for display on the CRT screen. The generator includes the Vector Set-Up logic, X and Y Data Handler logic and Digital-to-Analog (DAC) Processing circuitry for converting the display list data into X,Y, and Z analog signals used to drive the deflection yokes and beam of the CRT.

The circuit descriptions are referenced to the block diagrams; detailed diagrams and illustrations are provided where applicable. Compare the block diagrams to the actual Vector Generator schematics (Volume 2) to get a clear understanding of the actual circuit layout and to become familiar with the schematics.

The theory of operation is presented in the following order:

- Vector Set-Up Control Logic
- X Data Handler
- X DAC Processing

NOTE

The X and Y axis circuits are basically identical so only the X axis theory is described.

The simplified block diagram in Figure 8-18 shows the relationship between the major blocks of the X channel and the vector control logic. Data from the Display Controller is fed to the X Data Handler and Vector Set-up logic. The Vector Set-Up logic executes the controller commands and tells the data handler how to process the incoming data. Conversion from digital to analog signals is performed by the DAC Processing circuits and then the signals are passed on to the DVST display circuitry.

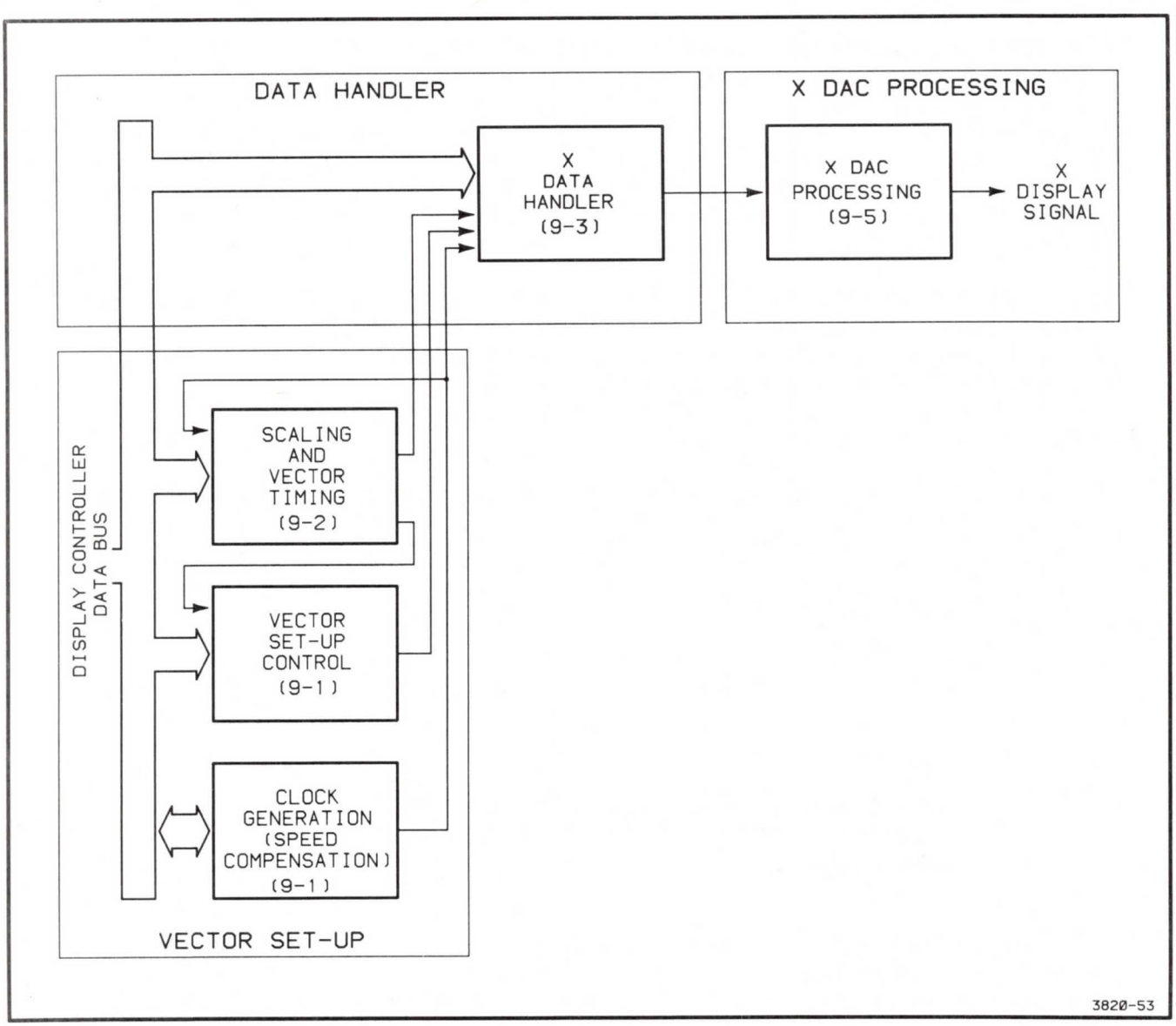


Figure 8-18. Vector Generator Simplified Block Diagram.

Vector Set-Up and Control Logic

Before the actual X axis signal processing is described, it is necessary to have a good understanding of the timing and control logic which is used in the Vector Generator. This logic consists of the Vector Set-Up Control, Clock Generation, Scaling and Vector Timing blocks in Figure 8-18.

The heart of the Vector Set-Up and Control logic is a state machine (Figure 8-19) whose purpose and operation are similar to the one used in the Display Controller. It performs the hand- shaking tasks between the Display Controller and the vector gener- ating circuitry and controls all operations. The state machine has seven states which control the operation being performed. The state machine is composed of three flip flops and associated gates. The states are:

A	000	Shift register is clear, waiting for vector.
B	001	Waits for "generator not busy".
C	101	Shift {delta}X,{delta}Y, and completion counter.
D	011	Transfer data to vector generator.
E	010	Clear VAVIL.
F	100	Wait for "generator not busy".
G	110	Increment X until displacement count = 0.

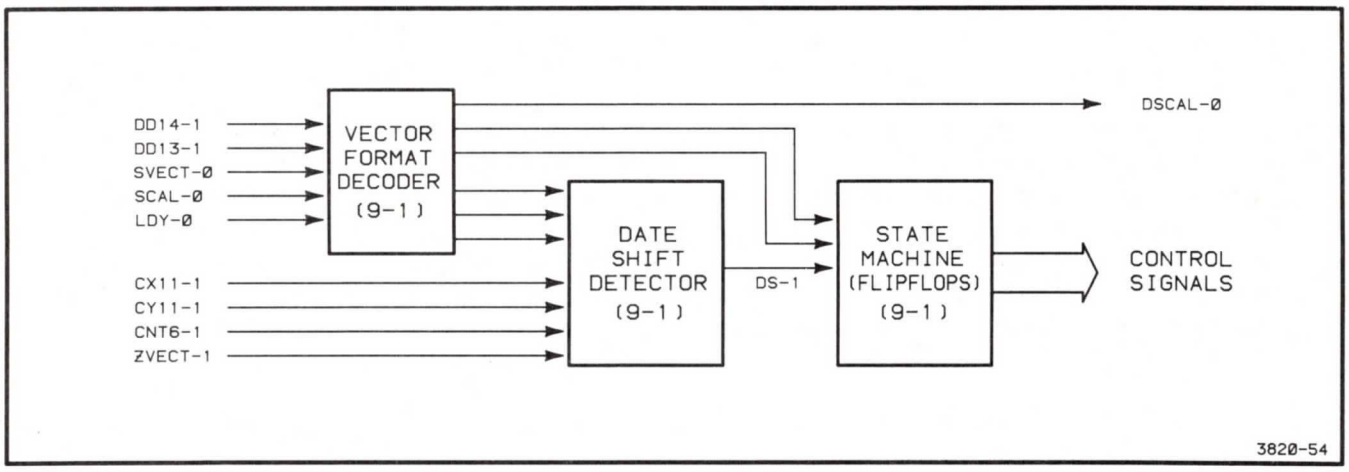


Figure 8-19. Vector Set-Up State Machine Block Diagram.

The complete state machine operation is shown in Figure 8-20.

NOTE

If the Vector Timing character displacement counter is not at count 0 and scaling is not on, the machine will jump to state F to clear the displacement counter before going to state B. The displacement counter must be cleared before continuing because the display characters are drawn by individual vectors from a display list in memory. These display lists are reached by subroutine jumps and it is only upon return from one of the subroutines that character displacement (or spacing) is performed. Thus, the state machine must use states F and G as necessary to obtain the desired displacement before any other vectors can be drawn.

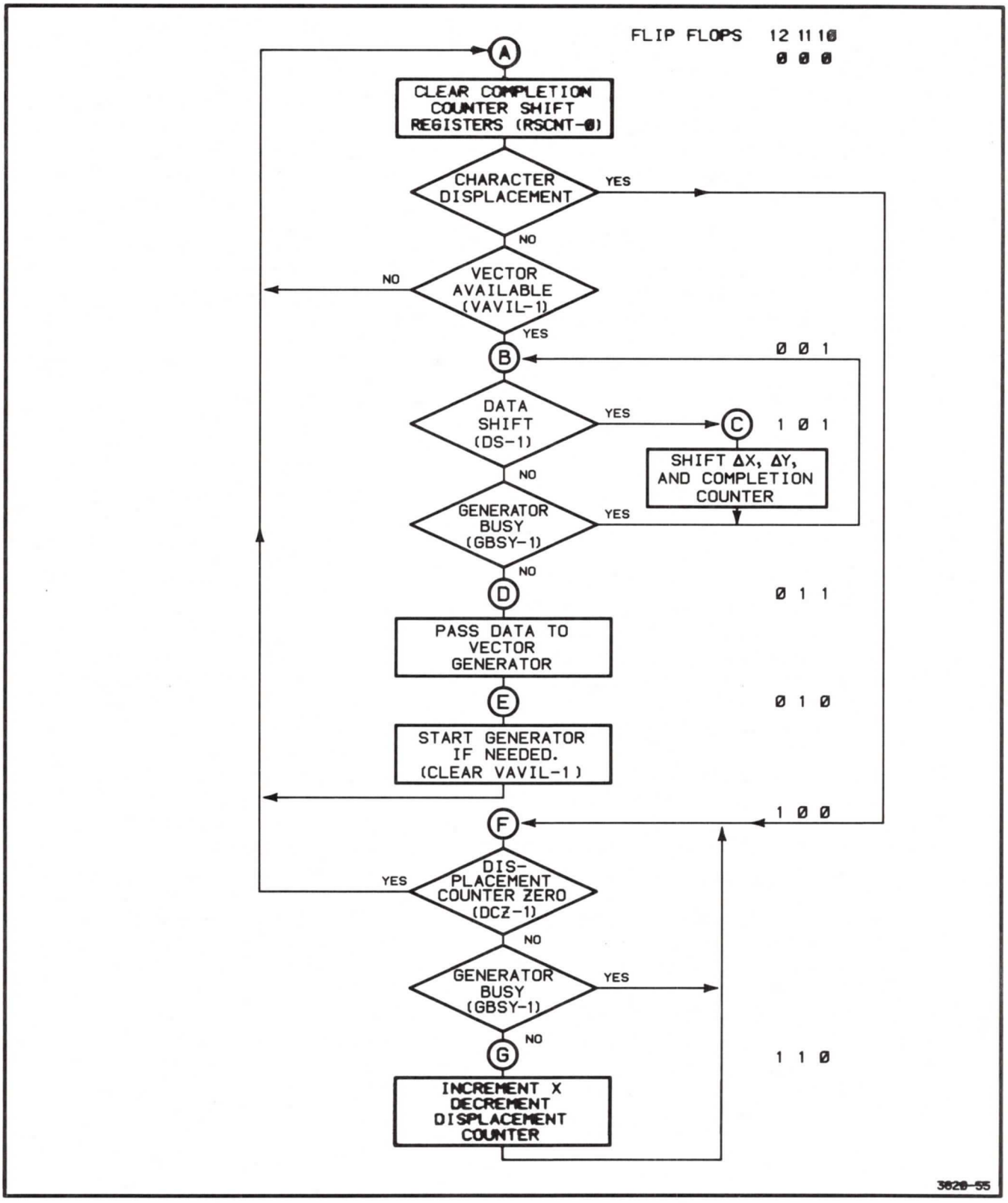


Figure 8-20. Vector Set-Up Control State Machine Flow Chart.

The state machine's data shift mode is determined by the Data Shift Detector and the Vector Format Decoder (Figure 8-19). Data bits DD13 and DD14 and signals SVECT,SCAL determine, when decoded, whether a vector will be long, short, relative, or absolute. Or whether it will be relative in the X axis and absolute in the Y axis. These signals are decoded by the Vector Format Decoder and the output sent to the state machine output gates.

Data shift signal DS goes low when the Data Shift Detector detects that the X and Y Data Handler Shift Register normalizing has been completed or is not needed. Shift normalization is explained in another section.

Clock Generation

This logic furnishes the clock signals required by the Vector Generator circuitry. It also provides speed compensating signals necessary to maintain the proper speed for the X and Y vectors as they are drawn.

The Clock Oscillator drives the Clock Divider at a 24 MHz rate. The divide by two flip flop output is 12 MHz with a 50 percent duty cycle. The clock output is reset when the INIT signal is active during power up. The clock signals are fed to the state machine, clock generation circuits, and circuitry in other sections of the generator. Further explanation of the clock signals usage is located in these sections.

In order to compensate for the variation in different vector speeds, the clock (MCLK) for the Data Handler Rate Multipliers is adjusted for each vector. This is done so that the overall vector velocity is nearly constant no matter what vector is being drawn. This is accomplished by feeding the four MSB's of X and Y (after shift normalization) to the Clock ROM (see Figure 21). The ROM selects a pre-programmed output for the correct speed compensation between X and Y of the vector being drawn. Output from the Clock ROM drives the Clock Rate Multiplier whose output becomes the MCLK signal. This signal clocks the data handler rate multipliers (F[in]) which determine the frequency of f[x] and f[y], according to the inputs from the X and Y shift registers. Thus, speed compensation is achieved and the proper ratio is maintained between the X and Y components of the vectors.

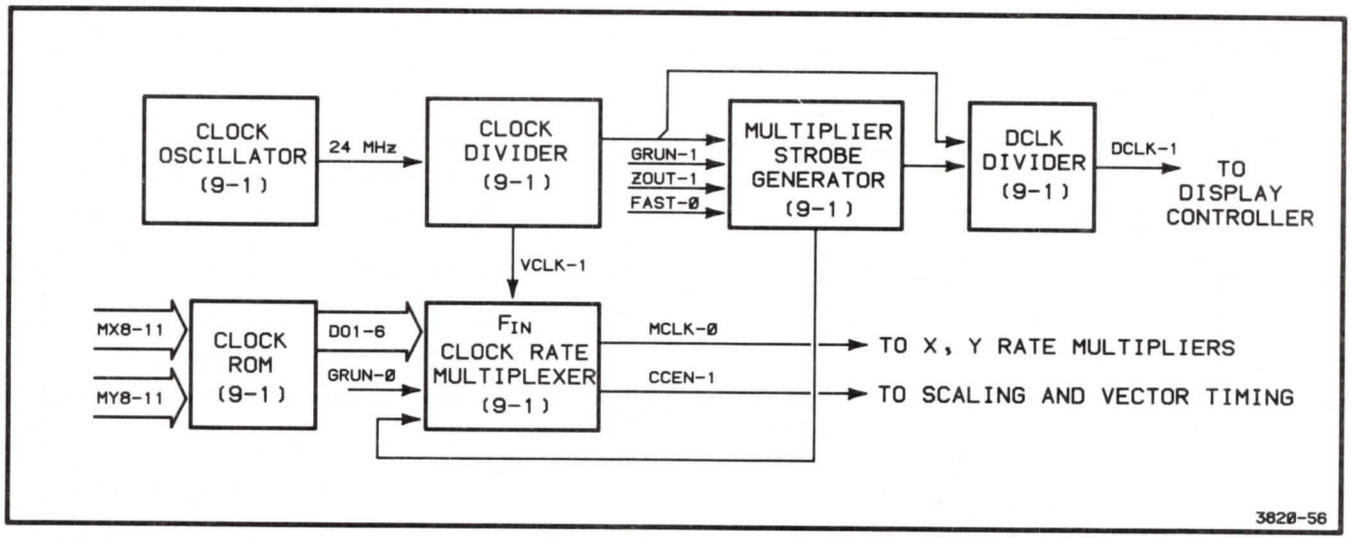


Figure 8-21. Clock Generation Simplified Diagram.

The Clock Rate Multiplier strobe input is driven by the Multiplier Strobe Generator. The generator flip flops and associated gates read the FAST,GRUN, and ZOUT signals and set the strobe frequency to 3 MHz or 12 MHz. The DCLK Divider divides the signal down to 1.5 MHz or 6 MHz to generate the DCLK signal for use in the Display Controller. This clock runs only while vectors are being generated; 6 MHz for write-through vectors and relative moves and 1.5 MHz for storage vectors.

Scaling

Figure 8-22 shows a simplified block diagram of the Scaling and Vector Timing circuitry; refer to it during the following discussions.

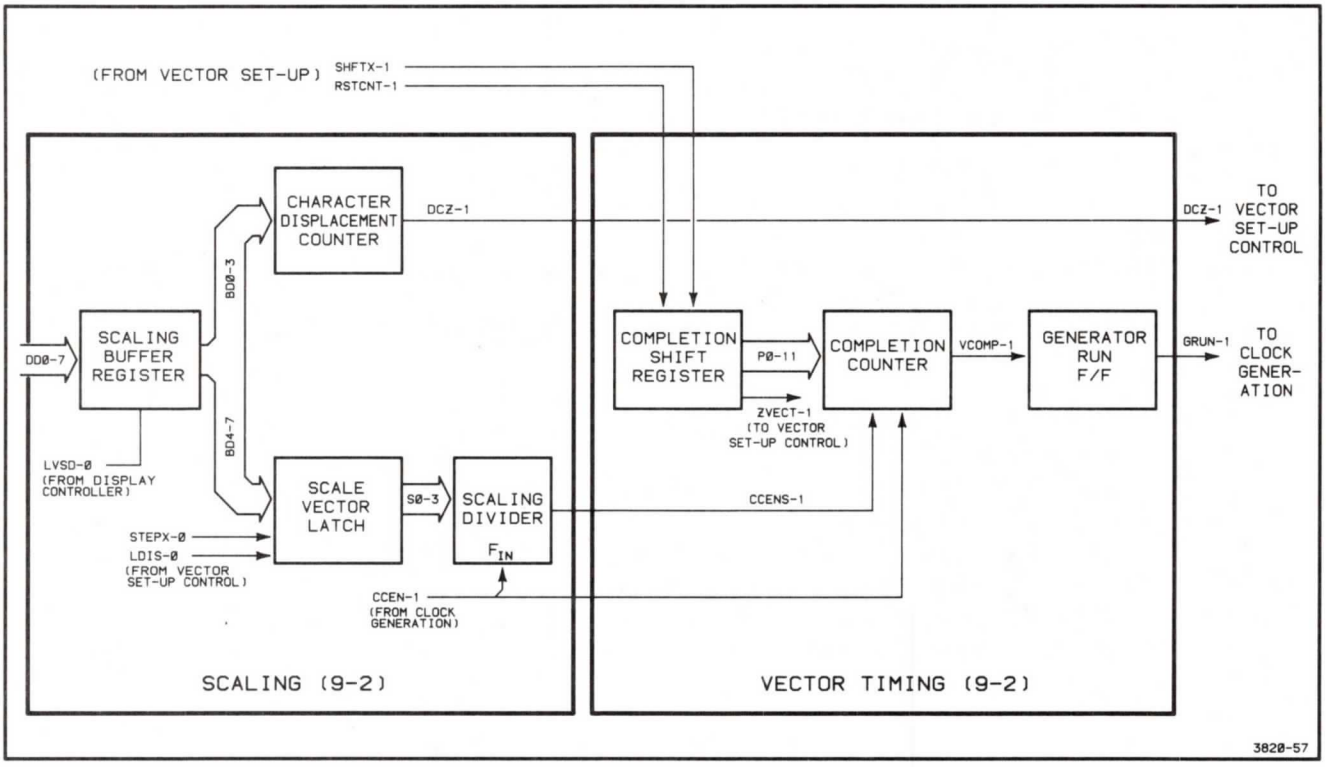


Figure 8-22. Scaling and Vector Timing Logic Block Diagram.

The scaling logic provides a scaling factor to multiply the vector length by one to sixteen times. The logic also generates a signal (DCZ) that indicates when the character displacement count is zero. Scaling is used primarily for changing character display sizes.

Data bits DD0-7 provide the scaling and character displacement information. The data is latched through the Scaling Buffer Register to the Character Displacement Counter and the Scale Factor Latch after LVSD goes low and then high. The displacement counter uses bits BD0-3 to generate a signal (DCZ) when it detects a zero displacement condition. The STEPX and LDIS signals from the state machine enable the counter to increment its count until DCZ is asserted. The handshake causes the state machine to clear its count because no further vector displacement is indicated (see Figure 8-19).

The Scale Factor Latch passes scaling bits S0-S3 to the Scaling Divider. The latch occurs when state machine flip flop 11 is set asserting LSM (see Figure 8-19). It also latches the DSCAL signal which is OR'd with the Scaling Divider output. This assures that, when a scaling factor higher than 1 is not required and DSCAL is high, the Completion Counter is activated and clocked only by the CCEN signal.

The Scaling Divider provides a scale factor that determines the number of times a count is performed by the Completion Counter. The divider is clocked by F[in] pulses (CCEN) to lengthen the vector by providing CCENS clock pulses to the Completion Counter. The scaling factor (1-16) determines the rate at which the counter runs and therefore the vector length. Thus, if the scale factor is 3, F[in] is divided by 3 and the Completion Counter rate is reduced to one third. Notice that the scaling factor only increases the vector length; it cannot decrease the length of the vector. Between vectors, (when the generator is not running, GRUN is low, and the divider has finished its count) the load input is enabled to load new data for the next completion count cycle.

Vector Timing

The Vector Timing logic consists of a Completion Shift Register, Completion Counter, and Generator Run Flip Flop. The purpose of this logic is to tell the vector generator to stop generating a vector when it is complete.

The Completion Shift Register is cleared for new shift information when RSCNT goes low at the beginning of a Vector Set-Up Control state machine cycle. The least significant bit of the shift register generates the ZVECT signal which indicates a zero length vector. ZVECT terminates the shifting operation and inhibits the GSTRT signal generated by the state machine.

The Completion Shift Register shifts data upon command from the SHFTY signal. This signal is asserted whenever the state machine calls for an X or Y data shift. (see Figure 8-20). As the data shift is completed, the Completion Counter counts the PO-11 data. The counter is enabled by the VCLK and CCEN clock signals. Upon completion of the count, VCOMP is asserted which clears the Generator Run Flip Flop. With GRUN low, the vector generator is disabled until a new vector-generate command (GSTRT) is received from the state machine. The scaling factor also enables the counter and its output gates as described in Scaling.

At the end of the vector completion count cycle when VCOMP goes high, the flip flop Q[bar] output gates the MCLR signal to the Rate Multipliers in the X and Y Data Handlers. This signal clears the multipliers between vectors in preparation to receive new vector data; further explanation follows in the X and Y Data Handler description.

The CNT6 signal is used by the decoding logic in the Vector Set-up Control to determine when the first 6 bits of X and Y data have been shifted. These data bits are shifted out when a short format vector command is being processed because they are unusable data.

In summary, the sequence of logic events is as follows:

1. The Generator Run Flip Flop and Completion Shift Register are cleared; GRUN is low.

2. SHFTY is repeatedly asserted until all data has been properly shifted and the Completion Counter is loaded with new data. (May occur concurrently with 4 or 5.)

3. The GSTRT signal pulses high, bringing GRUN high to generate a new vector.

4. The Completion Counter is enabled.

5. At the completion of the data count, VCOMP goes high.

6. The Generator Run Flip Flop is cleared which stops the generator until a new vector generate command is received. The MCLR clock signal clears the X and Y Data Handler Rate Multipliers for new data.

X Data Handler

The Shift Register, Latch, Rate Multiplier, and Counter have two operating modes determined by commands from the Display Controller board. One mode is for long or short vectors of relative length and the other is for setting the absolute position of the CRT beam. Figure 8-23 shows the simplified circuit configuration for these two modes of operation.

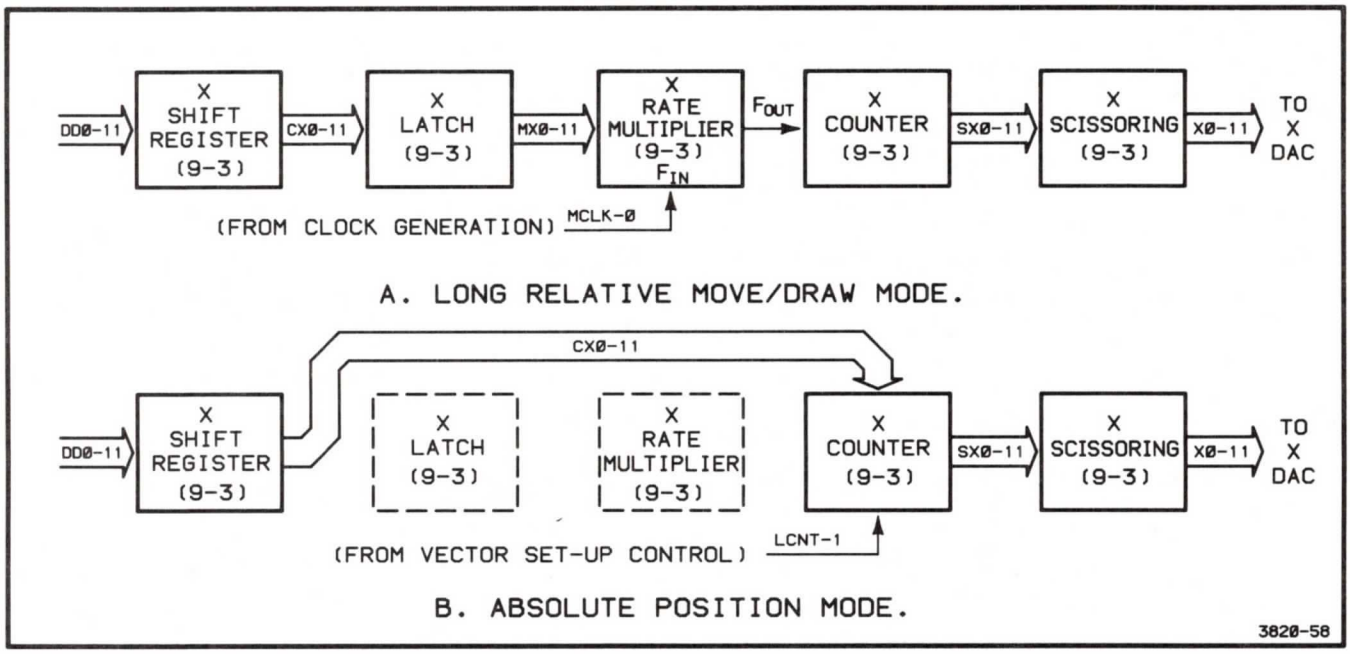


Figure 8-23. Circuit Configurations for the Relative and Absolute Position Modes.

Data Multiplexer

Data bits DD0-14 are selected and passed to the Shift Register by the circuitry in this function block. During short relative vectors, bits DD8-13 are used by the X Shift Register and during long relative vectors, bits DD0-11 are selected for the shift register. Bits DD6, DD12, and DD14 are selected to determine the X and Y sign values (XS-1,0; YS-1,0) used in the Counter and DAC Processing circuits.

Shift Register

For relative vectors, the Shift Register shifts data until it is normalized (MSB=1). This occurs when SHEN is high and SHFTY is repeatedly asserted until the MSB of either the X or Y Shift Register equals 1. The data must be normalized before it is latched to the Rate Multiplier when a relative vector is drawn on the display. In the case of a short format vector command, bits DD6-11 are shifted out before data is used at the shift register output because these bits contain useless data.

During absolute positioning of the CRT beam, when the beam is moved rapidly to a new position, the Shift Register acts as a latch. LDX and SHEN go low, disabling the clock input and enabling the load input of the register. Thus, the loaded data (CX0-11) is latched directly to the Counter.

The 13th bit of data (CX12), which is used as a sign bit for the X vector, is latched when LDX is asserted during a load X data command from the Display Controller board.

Latch

Data from the Shift Register is held and latched in this function block. The shifted (normalized) data is latched to the Rate Multiplier when LTCH goes high. The sign bit is also latched at the same time. RXSGN clears the sign bit between vectors.

Rate Multiplier

The rate multiplier input data is normalized as follows:

1. The {delta}X and {delta)Y data is doubled (doubling the length of the vector).

2. The number of rate multiplier input clock pulses (MCLK) are divided by two by shifting the Completion Count Shift Register (drawing a vector only half as long).

3. This produces the correct number of F{out} pulses at twice the original frequency which doubles the vector drawing speed.

The data doubling is continued until the {delta}X or {delta}Y has a 1 in the MSB.

Example:

	Before shifting MSB	After shifting MSB
{delta}X	001011110010	101111001000
{delta}Y	000110111111	011011111100

During the formation of a relative vector on the CRT display, the Rate Multiplier performs digital frequency division on the incoming clock, F[in](MCLK), according to the ratio:

$$\frac{\{delta\}X(\text{or } \{delta\}Y)(12 \text{ bit number})}{4096}.$$

The output frequency (F{out}) drives the Counter (see Figure 8-24) which provides the DAC with the necessary data to draw a relative vector in the X axis. Since there is also Y vector data, the following is true:

$$F[out]X = \frac{F[in](\{delta\}X}{4096} \text{ and } F[out](Y) = \frac{F[in](\{delta\}Y)}{4096}.$$

This gives the ratio:

$$\frac{\text{Y DAC Rate}}{\text{X DAC Rate}} = \frac{F[in]\ (\{delta\}Y/4096}{F[in]\ (\{delta\}X/4096} = \frac{\{delta\}Y}{\{delta\}X}$$

which maintains the proper slope for relative vectors. When the vector is complete, the MCLK clock is disabled and MCLR is asserted clearing the multipliers for new data. Thus, in the Relative Move/Draw mode, the F[in] pulses are divided (interpolated) at a different rate.

In the Absolute Position mode, the multiplier is disabled and LCNTX clocks the Counter to load data from the Shift Register. This data provides the DAC with the necessary information to rapidly move the beam to its new position.

The STEPX signal clocks the X Counter for the proper displacement between display characters (see Figure 8-21).

Counter

The Counter performs two separate functions. In the Relative Move/Draw mode it counts up or down when clocked by the F[out] pulses from the Rate Multiplier. The count direction, which determines the direction that the vector is moved or drawn (left or right in X and up or down in Y), is controlled by sign bit XS (YS in the Y Data Handler). When the 12th bit has been counted, the last carry output of the counter goes low which causes pin 8 of the 13th Bit Gate output to go high. See Figure 8-24. The next clock pulse toggles the 13th Bit F/F causing the Q[bar] output to go low when the 13th bit (bit 12) is high. This in turn changes the vector direction as explained next in Scissoring.

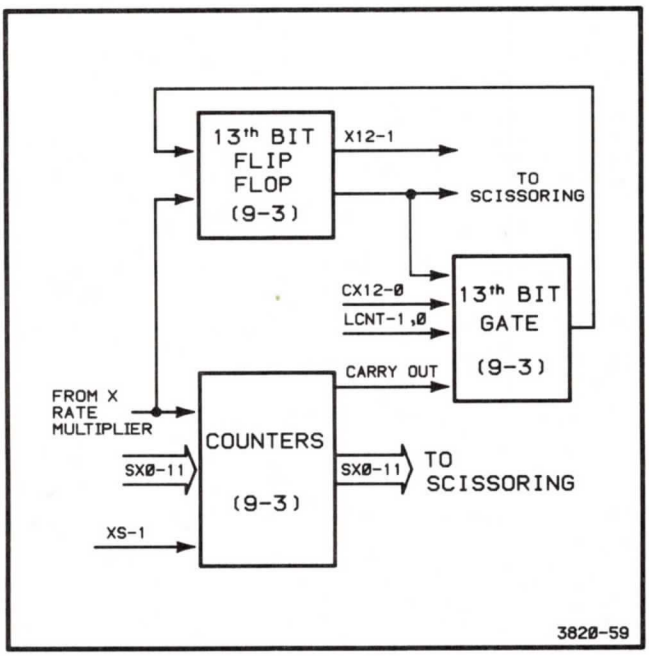


Figure 8-24. X Counter Simplified Diagram.

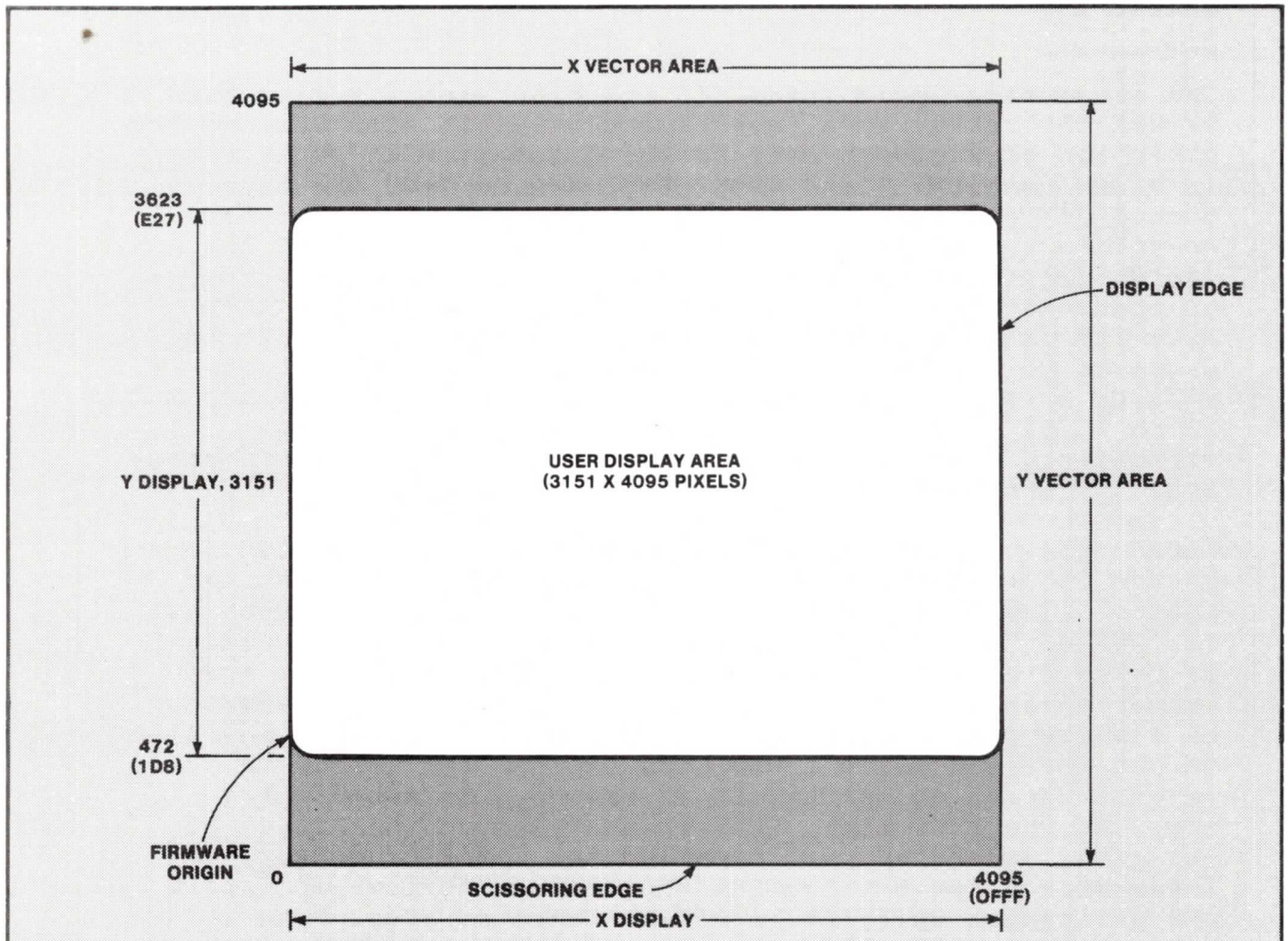
The Counter is parallel loaded in the absolute position mode (rapid movement of beam to new position). CX12 provides bit 12 in this mode when it is gated through the 13th Bit Gate to the 13th Bit F/F. This occurs during the load count cycle when LCNT and LDX are asserted. LCNT is held low to disable the carryout during this mode. When the MSB (bit 12) goes high, the data is passed through the Scissoring circuitry.

Scissoring

The scissoring logic turns off the beam when a vector goes beyond the vector area (see Figure 8-25) It also changes the direction of vector travel on the display. When an X vector is drawn past the 0 and 4095 pixel boundaries, the beam is turned off and data to the DAC is inverted. When the beam re-enters the display area it is turned on again and the vector continues to be drawn from that edge. Thus, a figure or character that is partially off the display area will have its displayed portion accurately reproduced. This applies to both the left and right edges of the normal user display area. The same is true of the top and bottom edges (0 to 4095) in the Y axis of the display. Scissoring effectively confines the CRT beam to the normal user display area (Figure 8-25) when a vector is being drawn.

Three sets of quad exclusive OR gates pass the Counter data to the DAC. Data is inverted at the gate outputs when the control line from the counter is high. This occurs when bit 12 (X12 or Y12) of the Counter is 0, indicating the vector is to be drawn in the normal user display area. When the vector moves the beam off the display area, bit 12 changes to 1 which places a low on the gate control inputs. The data is not inverted which causes the DAC and the vector to reverse direction so that it is returned to the display area. At the same time, CUTX is asserted at the output of its gate. Asserting CUTX reverses the Charge Pump and Integrator circuitry causing the beam to reverse direction and extinguish while it is off the display area. When it returns to the display area, bit 12 changes back to 0; then CUTX goes high to turn the beam back on.

Figure 8-25 shows a table with examples of the data count at different circuit points for a given vector location. Notice that if the Scissoring input is X'0FFF' hexadecimal, the Integrator output to the display is 4095 (the edge), and the beam is on. Changing the count to X'1000'(4096) causes the beam to turn off producing the scissoring effect. Also notice that between the DAC input and the Integrator output data inversion occurs. This is due to inversion inherent to the DAC and Charge Pump circuitry and is compensated for in the Scissoring circuitry.



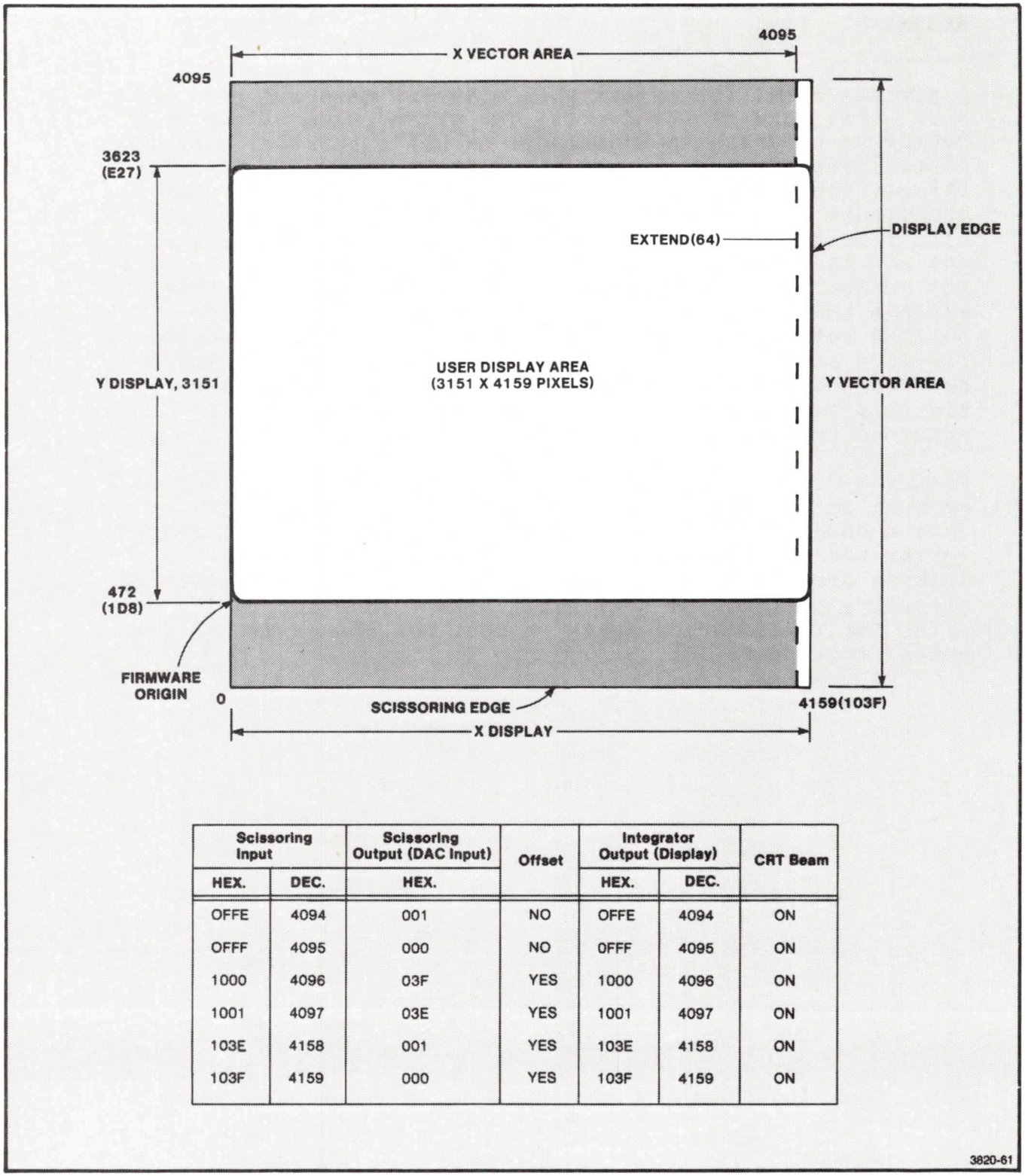
Scissoring Input		Scissoring Output (DAC Input)	Integrator Output (Display)		CRT Beam
HEX.	DEC.	HEX.	HEX.	DEC.	
OFFE	4094	001	OFFE	4094	ON
OFFF	4095	000	0FFF	4095	ON
1000	4096	000	OFFF	4095	OFF
1001	4097	001	0FFE	4094	OFF
0001	1	FFE	0001	1	ON
0000	0	FFF	0000	0	ON
1FFF	8191	FFF	0000	0	OFF
1FFF	8190	FFE	0001	1	OFF

Figure 8-25. Diagram Showing the Normal User Display Area in the X and Y Axes.

Extend

A special condition exists when a vector is drawn past the 4095 pixel edge of the X axis. The extend mode allows an X vector to be drawn an additional 64 LSB's (pixels) past the normal user display area as shown in Figure 8-26. When the Display Controller asserts XTEND, CUTX goes high. If the X coordinate is then made greater than 4095, the lower six bits from the Counter are inverted while the upper six bits are non-inverted. OFFSET goes low causing the X DAC to shift its output up the equivalent of 64 LSB's. This effectively extends the DAC input to receive the additional count shifted into the exclusive OR gates. The Display Controller firmware does not allow the vector to be drawn past the X axis edge since that area is undefined. The extend mode is simply a function that stretches the X axis to obtain the required number of characters in the display area.

Figure 8-26 shows a table with the count status at various circuit points when OFFSET is enabled or disabled. Moving from a count of X'OFFF' (beam at 4095) to a count of X'1000' causes the OFFSET to turn on which extends the vector drawing area to 4159 pixels (X'103F'). Thus, the Scissoring circuitry performs an additional extend function in the X axis. The Y Scissoring function does not change during the extend mode operation.



Scissoring Input		Scissoring Output (DAC Input)	Offset	Integrator Output (Display)		CRT Beam
HEX.	DEC.	HEX.		HEX.	DEC.	
OFFE	4094	001	NO	OFFE	4094	ON
OFFF	4095	000	NO	0FFF	4095	ON
1000	4096	03F	YES	1000	4096	ON
1001	4097	03E	YES	1001	4097	ON
103E	4158	001	YES	103E	4158	ON
103F	4159	000	YES	103F	4159	ON

Figure 8-26. Diagram Showing the User Display Area Extended in the X Axis.

DAC Processing

The X vector processing circuitry consists of a DAC, a Slew Rate Amplifier, an Integrator, a Decoder, and a Current Switch. A simplified block diagram is shown in Figure 8-27.

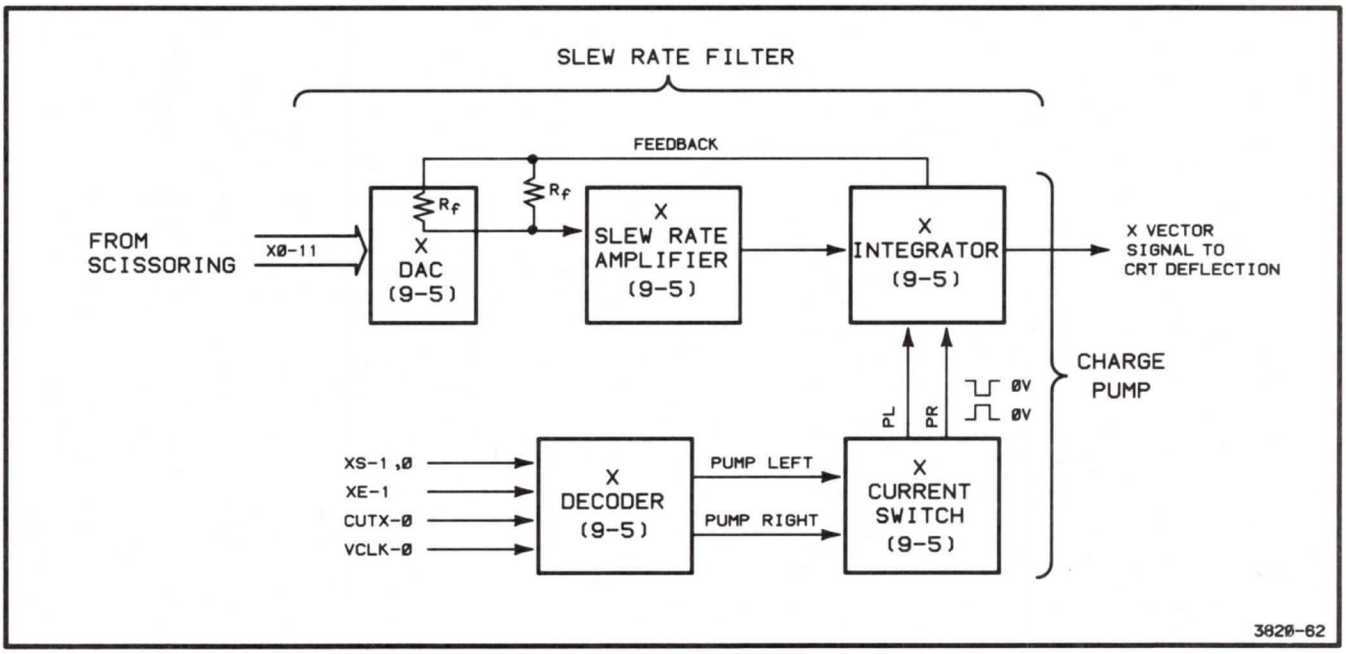


Figure 8-27. X Vector DAC Processing Diagram.

The heart of this circuitry is the Charge Pump which is composed of the Current Switch and the Integrator. It uses decoded signals to generate (pump) LSB increments in step with the DAC input data. These increments become the X analog display signal. Feed-forward compensation is provided to improve the high-pass characteristics of the Integrator stage.

The Slew Rate Filter is composed of the DAC, Slew Rate Amplifier, and Integrator. The Slew Rate Filter provides DC stability and compensates for small errors introduced by the Charge Pump.

X DAC

This circuitry provides the X vector data input to the Slew Rate Filter (Figure 8-27). It also provides a 6.4 V reference source. Data lines X0 through X11 carry data from the X Scissoring to the input of the DAC. The DAC output is fed from pins 15 and 17 to the Slew Rate Amplifier. R405 and an internal resistance between pins 15 and 18 provide feedback for the Slew Rate Filter loop. During digital to analog conversion, a change at the DAC output occurs when the DAC input is changed by one one LSB in value. This is equivalent to one pixel of change in the CRT beam position. R425 uses the 6.4 reference voltage to center the output of the DAC above and below zero volts. R424 controls the X vector size by changing the DAC gain.

Offset Current

When OFFSET is asserted during the vector extend mode, R301 current is steered from CR301 to CR302 and the DAC output. This provides the additional current (equivalent to 64 LSB's) required to write the vector past the normal 4095 LSB display area.

X Slew Rate Amplifier

Three ECL (Emitter Coupled Logic) line receivers form a cascaded amplifier with high gain-bandwidth and limited swing output. The amplifier output is fed to the following integrator stage. A differential output drives the output of the integrator. This provides feed-forward compensation to improve the high frequency stability of the Slew Rate Filter. FET's Q505 and Q406 conduct when the Absolute

Position Level Translator is activated. The output current of the amplifier is increased causing the integrator output voltage to change rapidly to its new absolute position level. R406 provides negative feedback to stabilize the amplifier when it is in the high slew rate (absolute position) mode.

X Integrator

The slewed signal drives and Charge Pump drives the integrator where it is inverted. The resulting vector voltage is applied to the CRT deflection amplifier. The output is fed back to the input of the X Slew Rate Amplifier through R405 and the DAC to provide compensation for the Charge Pump mentioned earlier in the block diagram description. Other signal lines entering this block will be discussed in the following function block descriptions.

TC Power

The -TC amplifier samples the DAC's 6.4 voltages to use as a reference in setting the temperature compensated (TC) voltages. The -TC operational amplifier senses the voltage change at CR605 due to temperature and adjusts its output accordingly to compensate the -TC current switch circuits. The +TC operational amplifier, using the compensated -TC output, provides the +TC current switch circuits with temperature compensating voltages.

X Current Switch

ECL level pulses from the decoder drive the pump left and pump right gates. These gates translate normal ECL levels to swing plus or minus 0.4 volts from ground. When the PL output goes high, CR503 turns off which steers current from R503 through CR505 to the input summing node of the integrator. At the end of the pulse, PL goes low turning on CR503 again and steering current away from the summing node. When PR goes low, CR504 turns off which steers current from R507 through CR506 to produce a negative-going current pulse at the input of the integrator. Differential output signals are fed to the output of the integrator to provide additional bootstrapping.

X Decoder

The X Decoder logic (Figure 8-27) decodes timing signals to provide the pump left and pump right pulses for the X Current Switch. The pump left signal is derived in the Pump Left Gating logic (Figure 8-28). The logic translates the TTL levels to ECL levels for use in the current switch circuitry. When XS-1, CUTX, and XE-1 are asserted, a pulse is clocked through the gates to the current switch. If CUTX goes high, the pulse is blocked and the switch does not output to the integrator. Conversely, when XS-0 is asserted and XS-1 is low, the Pump Right Gating logic is activated to provide pump right pulses so that the beam moves to the right.

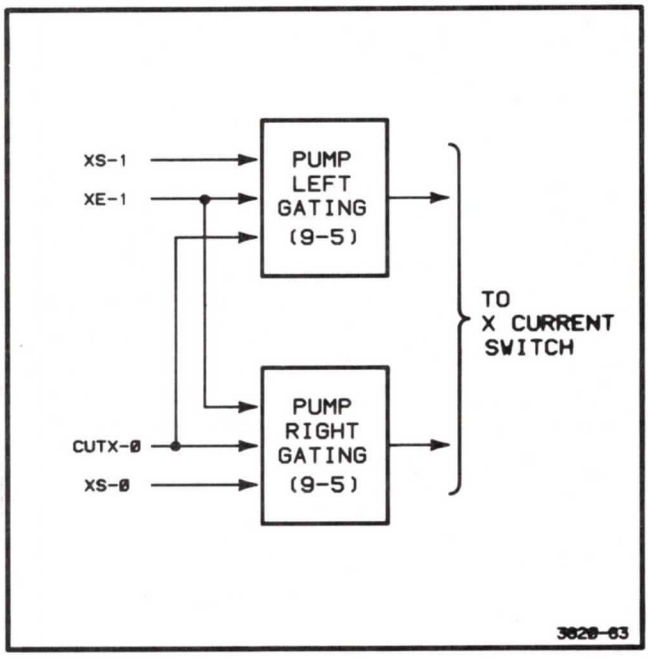


Figure 8-28. Simplified X Decoder Block Diagram.

1.3 Volt Power

Vcc for the current switches and Slew Rate Amplifiers is supplied by this circuit. The operational amplifier detects Vbb errors at its input and causes the transistor to maintain Vbb at 0 volts by adjusting Vcc accordingly.

Absolute Position Level Translator

This stage provides the gate switching voltage for the slew rate filters FET's. Switching on the FET's increases the slew rate so that the beam is rapidly moved to its new absolute position space. When ABS goes low, Q601's base-emitter bias changes and the transistor stops conducting. The rising collector voltage provides the gate voltage required to turn on the FET's.

Z Axis Controller

This circuitry accepts the Z, CUTX, and CUTY signals, controls the CRT Z axis drive, and generates the ZOUT signal. Gates control the output transistor which in turn causes the CRT beam to turn on or off. When CUTX and CUTY are high and Z is low, the transistor conducts which turns on the CRT beam.

Section 9

DISPLAY MODULE CIRCUIT THEORY

INTRODUCTION

This section of the manual explains the 4114 Display Module's operation. Circuitry is not discussed on a component basis, except in those cases where, for clarity, specific components are mentioned. This section provides sufficient information for the technician to isolate a specific block of circuitry as the problem area. The technician should then be able to locate the defective component.

GENERAL INFORMATION

Refer to the Storage Display Module Block Diagram, Figure 9-1, for a block diagram of the Display Module circuitry. The block diagram shows signals to external units such as the Hard Copy Unit and the pedestal. The Hard Copy Unit is an optional unit that can be connected to the Display via J5005.
The Display Module displays on the crt the information processed by the pedestal. Display information consists of X and Y axis inputs for deflection and Z axis inputs to turn the writing beam on or off. The pedestal inputs to the display are connected directly to the Interconnect board. Control lines between the pedestal and the display select display modes and control various operations, such as writing, copying, and erasing.

Five circuit boards, plus an Interconnect board, contain the Display Module's circuitry. The boards are the Low Voltage Power Supply board, the High Voltage and Z Axis board, the Deflection Amplifier board, the Storage board, and the Hard Copy Amplifier board.

The writing portion of the display consists of the Deflection Amplifier board, the Long and Short Axis Deflection Yoke (or coils), the High Voltage and Z Axis board and the crt writing components -- the Beam Cathode, the Control Grid, and the Focus Electrode.

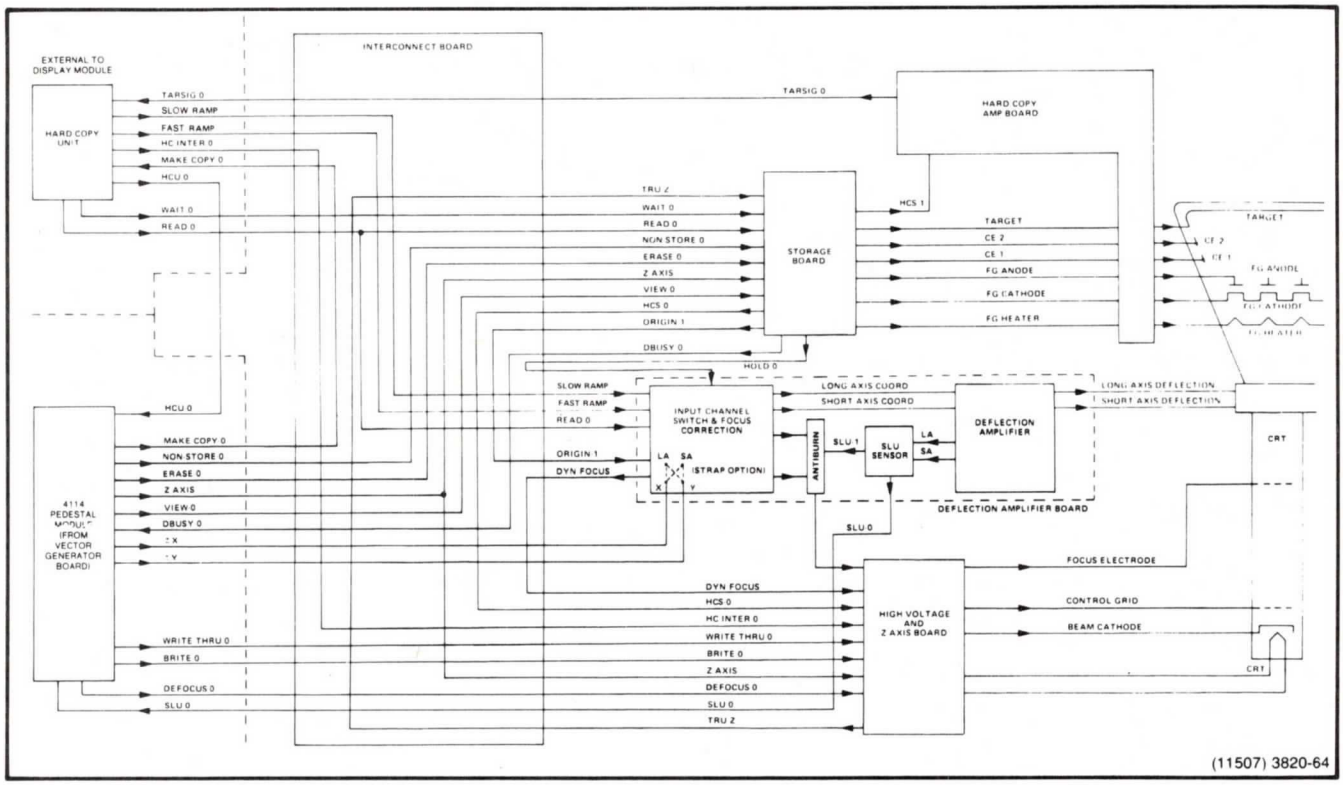


Figure 9-1. Display Module Block Diagram.

The storage portion consists of the Storage board and the crt storage components -- the Flood Gun Cathode, the Flood Gun Anode, the Collimation Electrodes (CE-1 and CE-2), and the Target.

The hard copy circuitry consists of circuitry on the Deflection Amplifier board, special logic circuitry on the Storage board, the High Voltage and Z Axis board, and the Hard Copy Amplifier board.

Appendix A contains a description of the interconnecting signals. The source and destination of each signal is also listed by schematic number.

CIRCUIT DESCRIPTION

Interconnect Board

Refer to Figure 9-1. In addition to providing the circuit board interconnections, the Interconnect board also contains the connecting points for the interface cable from the pedestal and for the connecting cable through J5005 from the hard copy unit. A diagram of the Interconnect board is found in the schematics section.

High Voltage and Z Axis Board

Refer to Figure 9-2. The High Voltage and Z Axis board regulates the writing beam focus and intensity. The following are the principle circuits:

- High Voltage Oscillator
- High Voltage Supply
- Intensity Control Logic
- Z Axis Amplifier
- Dynamic Focus Amplifier
- Control Grid DC Restorer
- Focus DC Restorer

High Voltage Oscillator

The High Voltage Oscillator is a regulated blocking oscillator that provides an alternating drive voltage to the primary winding (Pins 4 and 5 on Schematic A16-1) on the high voltage transformer, T75. The winding on Pins 3 and 6 of T75 on Schematic A16-1 provides positive feedback to drive the oscillator. Feedback from the High Voltage Supply regulates the duty cycle to compensate for both the high voltage load and power line fluctuations. Thus, the -6000 VDC output from the High Voltage Supply is maintained.

High Voltage Supply

In addition to providing feedback to the High Voltage Oscillator, the High Voltage Supply delivers -6000 VDC to the beam cathode. The High Voltage Supply also provides a -6000 V reference to the heater supply, Control Grid DC Restorer, and Focus DC Restorer circuitry.

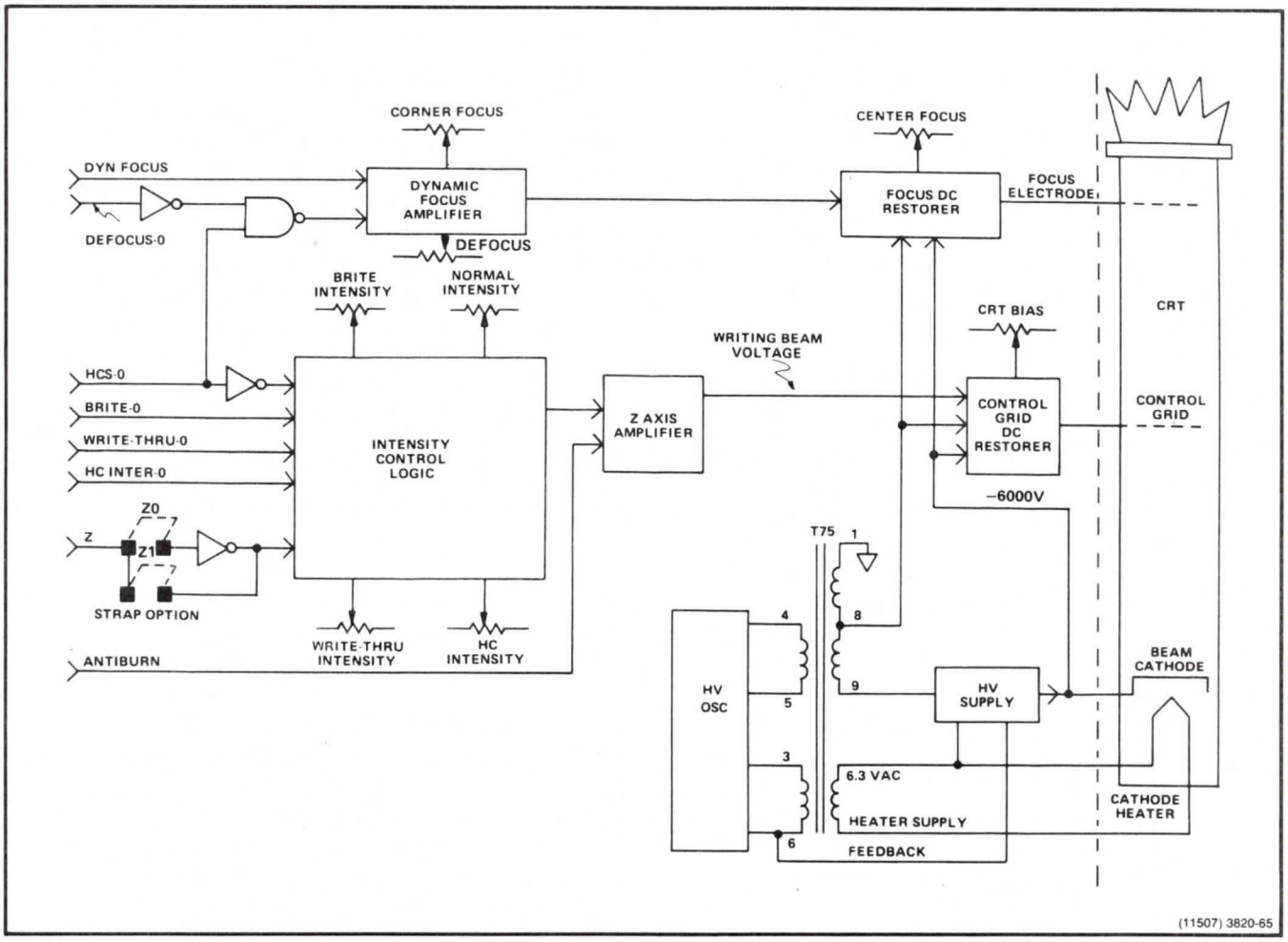


Figure 9-2. High Voltage and Z Axis Block Diagram

Intensity Control Logic

The Intensity Control Logic sets the limits of the crt writing beam intensity as selected by the logic values of HCS (Hard Copy Switch), BRITE, and WRITE-THRU. Refer to Table 9-1 for the crt writing beam intensity mode from different combinations of these three Display Controller input signals. Note that Table 9-1 also shows the Crt Writing Beam Focus mode as determined by the DEFOCUS signal. The actual focus control of the crt writing beam is discussed later.

HCS has the most influence in the Intensity Control Logic. Whenever HCS is low, all other signals, including Z Axis and DEFOCUS, are disabled. At that time, HC INTER-0 (from the hard copy unit) controls the Z Axis Amplifier and the HARD COPY INTENSITY adjustment controls the crt writing beam intensity.

When HCS is high (the display is not in Hard Copy mode), the Z Axis signal determines when the Z Axis Amplifier, and therefore the crt writing beam, is on.

If HCS is high and not influencing the Intensity Control Logic, the logic combination of WRITE-THRU and BRITE selects the intensity of the crt writing beam. If the WRITE- THRU signal is low, the Brite and Normal Intensities are inhibited and the crt writing beam intensity is controlled by the WRITE-THRU INTENSITY adjustment. If the WRITE-THRU signal is high, BRITE determines whether the crt writing beam intensity is Brite or Normal. If the BRITE signal is low, the crt writing beam becomes slightly brighter than Normal Intensity. This is accomplished by adding the control grid voltage from the BRITE signal (whose intensity is controlled by the BRITE INTENSITY adjustment) to the control grid voltage determined by the NORMAL INTENSITY adjustment.

Table 9-1

INTENSITY AND FOCUS SELECTIONS

Signals				Crt Intensity	Focus	Purpose
HCS	BRITE	DEFOCUS	WRITE-THRU			
0	X	X	X	HARD COPY	Focused	For hard copy operation.
1	X	1	0	WRITE-THRU	Focused	For write-thru operation displaying small characters and short vectors.
1	X	0	0	WRITE-THRU	Defocused	For write-thru operation displaying long vectors.
1	1	1	1	NORMAL	Focused	For small characters and high resolution vectors.
1	1	0	1	NORMAL	Defocused	For displaying large characters.
1	0	1	1	BRITE	Focused	For displaying medium or large characters.
1	0	0	1	BRITE	Defocused	For displaying wide or long vectors; large characters.

0 ▪ TTL LOW 1 ▪ TTL HIGH X ▪ "DON'T CARE"

Hard Copy Intensity is separately controlled by the HARD COPY INTENSITY adjustment.

Write-Thru Intensity is separately controlled by the WRITE-THRU INTENSITY adjustment.

Z Axis Amplifier

The Z Axis Amplifier is a logic-controlled amplifier that provides a crt writing beam voltage to the Control Grid DC Restorer. The crt control grid voltage is switched between a low level and the level which provides the desired crt writing beam intensity, which is set by the adjustments in the Intensity Control Logic. The Z Axis Amplifier turns the crt writing beam on and off according to the Z Axis signal and the logical status of HCS, BRITE and WRITE-THRU. Additionally, the Z Axis Amplifier uses a crt screen protection circuit which limits the crt writing beam intensity during low velocity (including zero velocity) deflection movements. If the Antiburn Sensor (on the Deflection Amplifier board) detects a low deflection velocity, a positive voltage is applied to the Antiburn signal line. This positive voltage reduces the Z Axis Amplifier output and, consequently, the intensity of the crt writing beam.

Dynamic Focus Amplifier

The Dynamic Focus Amplifier maintains a consistent crt writing beam focus and provides an alternative crt writing beam width. To perform these functions, a programmed modification changes the reference voltage sent to the Focus DC Restorer. The DYNAMIC FOCUS signal compensates for additional crt writing beam focus requirements at the edge of the screen. The signal provides the Dynamic Focus Amplifier with a voltage that increases with increased crt writing beam deflections. The CORNER FOCUS adjustment determines the DYNAMIC FOCUS signal magnitude necessary to maintain a focused crt writing beam. When DEFOCUS is low, except in

Hard Copy mode (when HCS is low), the crt writing beam is defocused by an amount determined by the Defocus adjustment potentiometer. Otherwise, when DEFOCUS is high or the Display is in Hard Copy mode, the crt writing beam is focused. The use of the DEFOCUS signal line allows a focused or defocused crt writing beam in combination with WRITE-THRU, BRITE, and NORMAL Intensities. See Table 9-1 and Intensity Control Logic in this section for a description of the intensity aspect of the crt writing beam.

Control Grid DC Restorer

The Control Grid DC Restorer provides the control grid voltage that regulates the crt writing beam. The CRT BIAS adjustment provides a reference voltage to set the crt writing beam cutoff bias. The output of the Z Axis Amplifier changes the control grid voltage to turn on the crt writing beam at a given intensity.

Focus DC Restorer

The Focus DC Restorer provides a controllable negative voltage to the focus electrode. The focus electrode voltage is set by the CENTER FOCUS adjustment and is dynamically modified by the Dynamic Focus Amplifier.

Deflection Amplifier Board

The Deflection Amplifier board performs the following functions:

- Provides the crt with writing beam deflection and the dynamic focus necessary for information display and hard copy production.
- Provides a signal (SLU) back to the pedestal to indicate a temporary wait while the Deflection Amplifier is catching up to the deflection inputs.
- Provides Antiburn protection to prevent crt phosphor damage due to slow moving, high-intensity beam activity.

Refer to Figure 9-3, Deflection Amplifier Board Block Diagram. The Deflection Amplifier board is divided into the

following four distinct operational areas:

- Channel Switch and Origin Shift
- Geometry and Focus Correction
- Antiburn Sensor
- Deflection Amplifiers

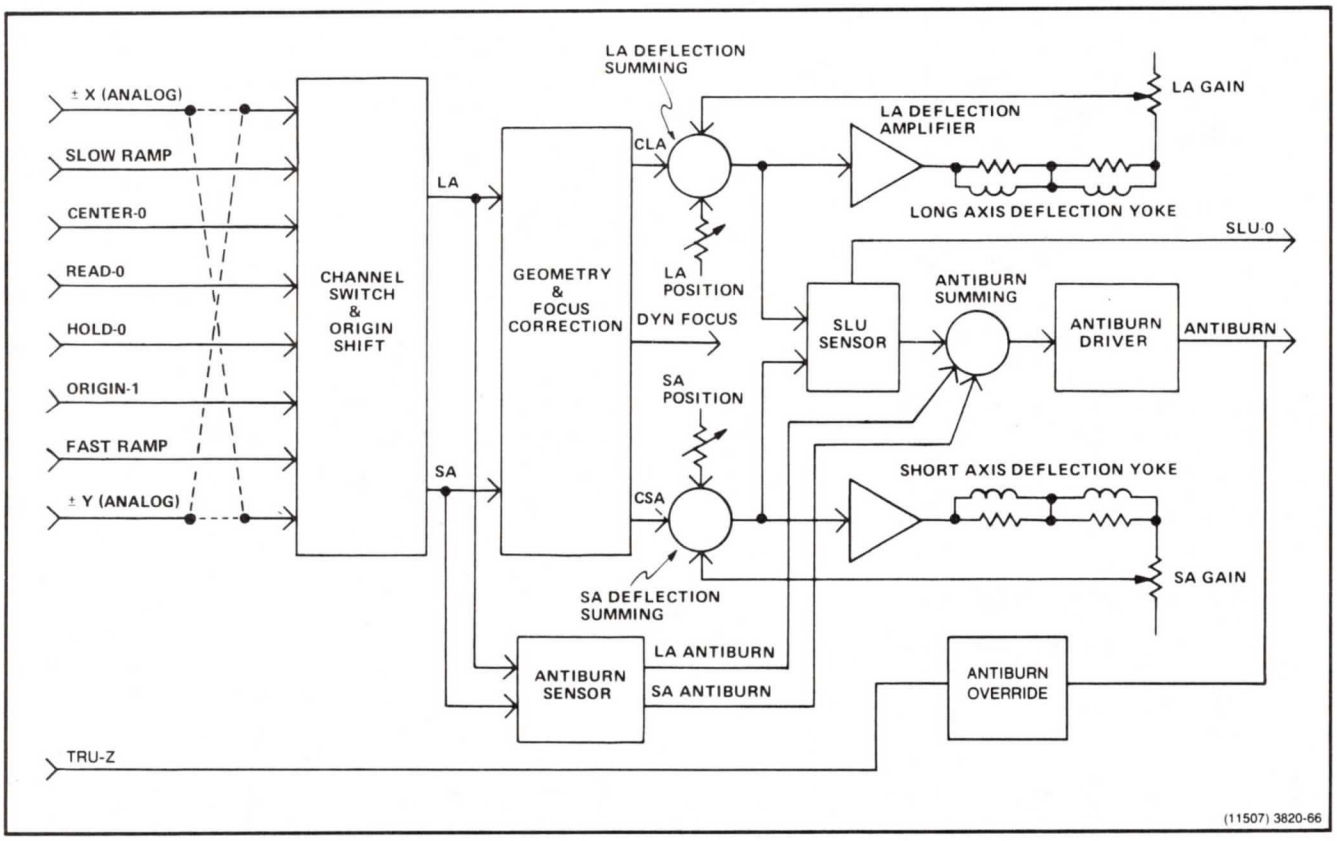


Figure 9-3. Deflection Amplifier Board Block Diagram.

Channel Switch and Origin Shift

The Channel Switch and Origin Shift provides an analog signal (LA -- Long Axis and SA -- Short Axis) to the Geometry and Focus Correction circuitry. The signal source is determined by READ and HOLD-0. READ normally is high, and the Channel Switch and Origin Shift then uses $\pm$X and $\pm$Y signal lines to reverse the long and short axes of the crt. When the crt is in the horizontal format, the X axis and LA (about 14 inches) are the same and the Y axis and the SA (about 10.5 inches) also are the same. The connector orientation is described in Section 11, Maintenance, Selecting X and Y Axis Inputs.

During hard copy operation, READ goes low, and the Channel Switch and Origin Shift then uses FAST and SLOW RAMP signals to provide outputs of LA and SA. For hard copy operation, there is no need to reverse the FAST and SLOW RAMP signals if the crt is rotated. LA HC POS, SA HC POS, LA HC GAIN, and SA HC GAIN control the position and size of the hard copy scan.

When Hold Mode is initiated and the HOLD strap option is "IN," HOLD-0 goes low and connects the Channel Switch to a separate set of inputs that are connected to ground. The grounded inputs prevent beam deflection and assure minimum deflection amplifier power dissipation during Hold mode.

The Origin Shift circuitry, which modifies the position information to prolong crt phosphor life, also is present in this block. The Origin Shift is an eight-position binary counter clocked by ORIGIN-1 (a logic pulse concurrent with the erase cycle on the Storage board). The output of the binary counter is fed through current dividers and then added to the LA and SA signals to modify the reference position for each new page. The eight positions ensure that no point on the crt is repeatedly written over from page to page.

By placing a low on the CENTER-0 signal line, the Origin Shift circuitry can be made inoperative. With zero volts on the +X and +Y signal lines, the crt writing beam is centered on the crt. See Figure 9-4.

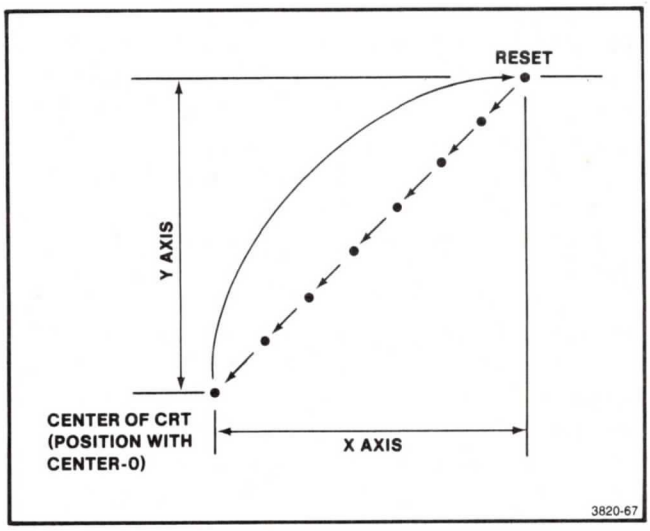


Figure 9-4. Origin Shift.

Geometry and Focus Correction

The LA and SA deflection signals are input to the Geometry and Focus Correction circuitry. Geometry correction is necessary to compensate for the "pin cushion" effect common with magnetic-type deflection systems. (See Figure 9-5.) This circuit adds or subtracts a deflection factor onto or from the LA and SA deflection signals, providing a "compensated" deflection voltage to the Deflection Amplifiers. A focus correction voltage also is output from this circuit, and again, the voltage output is dependent upon the LA and SA deflection inputs. For example, deflection inputs that place the writing beam at the edge of the display area must have a focus correction added because the distance to the edge of the display from the crt cathode is somewhat more than that to the display center. Thus, the length of the writing beam varies, which varies the focus. The DYNAMIC FOCUS Signal, input to the Focus circuitry on the High Voltage and Z Axis board, compensates for the variation in the focus point of the writing beam.

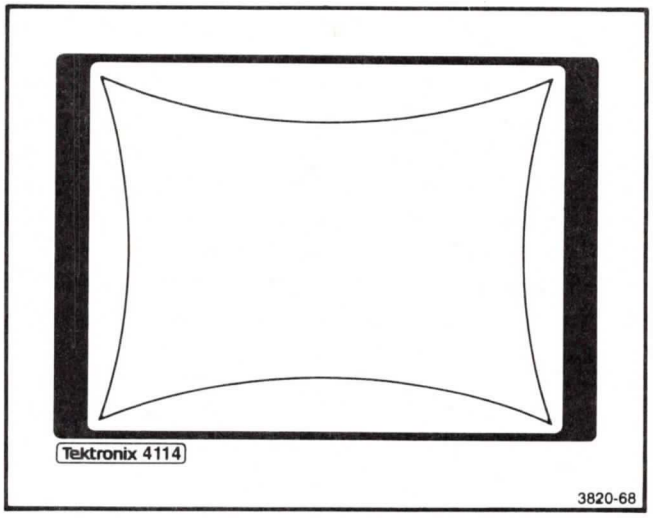


Figure 9-5. Pin Cushion Effects

Antiburn Sensor

Crt Protection Antiburn circuitry (providing the ANTIBURN strap is IN) detects the crt writing beam deflection velocity and controls the Z Axis signals through the Z Axis Amplifier (on the High Voltage and Z Axis board). If the deflection signals are absent or decrease to less than 23 V/s (800 mm/s), the Antiburn detection circuit increases the current to the Z Axis Amplifier. The Z Axis Amplifier detects this increased current and reduces the crt writing beam intensity, thereby preventing possible crt phosphor damage.

Deflection Amplifiers

The Deflection Amplifier circuitry provides the necessary deflection currents for the deflection yokes. The Deflection Amplifier circuity consists of:

- A Long Axis (LA) Deflection Amplifier,
- A Short Axis (SA) Deflection Amplifier,
- A Slu Sensor
- A deflection (current) summing point for both axes.

The four major adjustments on the Deflection Amplifier board control the display size and position. LA POS and SA POS control the position of the displayed data and LA GAIN and SA GAIN control the display size (width and height).

Refer to Schematic A15-1 and A15-2 for the Deflection Amplifiers. The LA and SA Deflection Amplifiers are high gain current amplifiers that supply drive current to the deflection coils. The drive current establishes a magnetic field in the deflection coil for crt writing beam deflection. Deflection coil current requirements are supplied by the 9 V supplies unless a high-speed move (deflection) is required. With a high-speed move, the 9 V supply is not adequate and an additional current source, the 20 V supply, is switched in by Q20 and Q30 (LA) and Q80 and Q90 (SA). Both transistor pairs normally are off and then turned on to temporarily aid instant deflection across the screen.

Input to the Deflection Amplifier is a summation of the following:

- Deflection signal from the Geometry and Focus Correction circuitry
- Position Voltage
- Feedback signal

A change in the inputs to the summing point causes the output to the Deflection Amplifier to change, altering the crt beam deflection. The gain of the Deflection Amplifier is controlled by the respective GAIN adjustment, which regulates the feedback.

The Slu Sensor circuitry generates the output signal SLU-0. This signal is made available to the Display Controller. When active (low), SLU-0 indicates that the Deflection Amplifiers are lagging behind the input deflection signal, and the display does not accept additional data until SLU-0 goes inactive.

The Slu Sensor compares the outputs of the Deflection Summing Amplifiers against a threshold of about zero volts. The Sensor is active when either Deflection Summing Amplifier has an output other than zero (the output voltages of U256 or U266 head towards the +15 V rails). The voltage out of the Deflection Summing Amplifiers is zero when the proper deflection current is established in the deflection coils. If, however, the velocity of the input slew signal is higher than what the Deflection Amplifiers can move (about 1.2 km/s or 34 kV/s), the Deflection Amplifiers lag behind (operating in an open loop manner), until they can catch up. The Slu Sensor circuitry prevents the pedestal from initiating another move before the Deflection Amplifiers have caught up with the input slew signal. The Slu Sensor generates the temporary wait flag, SLU-O.

Antiburn Driver

In the event the Deflection Amplifier fails, the Deflection Summing output never returns to zero. At this time a signal is sent to the Antiburn Summing point to turn off the crt writing beam. This protects the crt from phosphor burns due to the loss of writing beam position control. This is similar to the action of the Antiburn Sensor when the input crt writing beam deflection velocity decreases toward zero and the ANTIBURN strap option is IN. The ANTIBURN signal is then created when there is little or no movement in the X or Y axis, or the beam is on and stationary. The ANTIBURN signal (sent to the Z Axis Amplifier to reduce the beam writing intensity) is a TTL high signal.

Antiburn Override

When the ANTIBURN signal is high (antiburn is active), the Antiburn Override circuit creates a 20 percent duty cycle of the Z Axis which causes the reduced writing beam intensity. If the ANTIBURN signal were allowed to stay high and not pulled low 20 percent of the time, there would be no visible writing beam. Additionally, when the beam first begins to write, the Deflection Amplifier circuitry has a delay factor during which time the Antiburn Summing and Driving circuitry has not yet sensed that the beam is moving. The Antiburn Override then creates a duty cycle for the first few microseconds of operation so that the first part of the writing beam (or vector) is not blanked out.

Storage Board

Refer to the block diagram of the Storage Board, Figure 9-6. Refer also to the Schematics section while reading this description.
The Storage board controls electrodes in the crt to store, view, and erase displayed information. The basic circuits of the Storage board are shown in the block diagram. But, because of the complexity of circuit operations, the entire circuit operation is described by function as opposed to describing individual block functions.

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Operation of the Storage circuitry is centered around the View-Erase Counter. This circuit consists of two divide-by-16 counters in series, which provide the timing for the hold and auto erase functions. The View-Erase Multivibrator provides a 0.143 Hz square wave to the View-Erase Counter. This counter also has a Reset input from View Mode Control circuit. Refer to the two outputs from the View-Erase Counter: one output is activated if 112 seconds elapse before a Reset is initiated, but the other output is activated if a Reset does not occur in about 30 minutes. The operation of View mode, Hold mode and auto erase is discussed in the following paragraphs.

As long as the View-Erase Counter receives an active Reset at least once every 112 seconds, the Storage board circuitry maintains View mode. A reset occurs from the View mode Control when either of the following two conditions are met:

- An active Z Axis or GBUSY signal is received (depending upon placement of the View-Reset strap).
- The VIEW-0 signal goes active.

As long as either of these conditions is met, the Flood Gun Control circuit provides an output to the Flood Gun Amplifier, supplying voltage to the flood gun anode to maintain View mode.

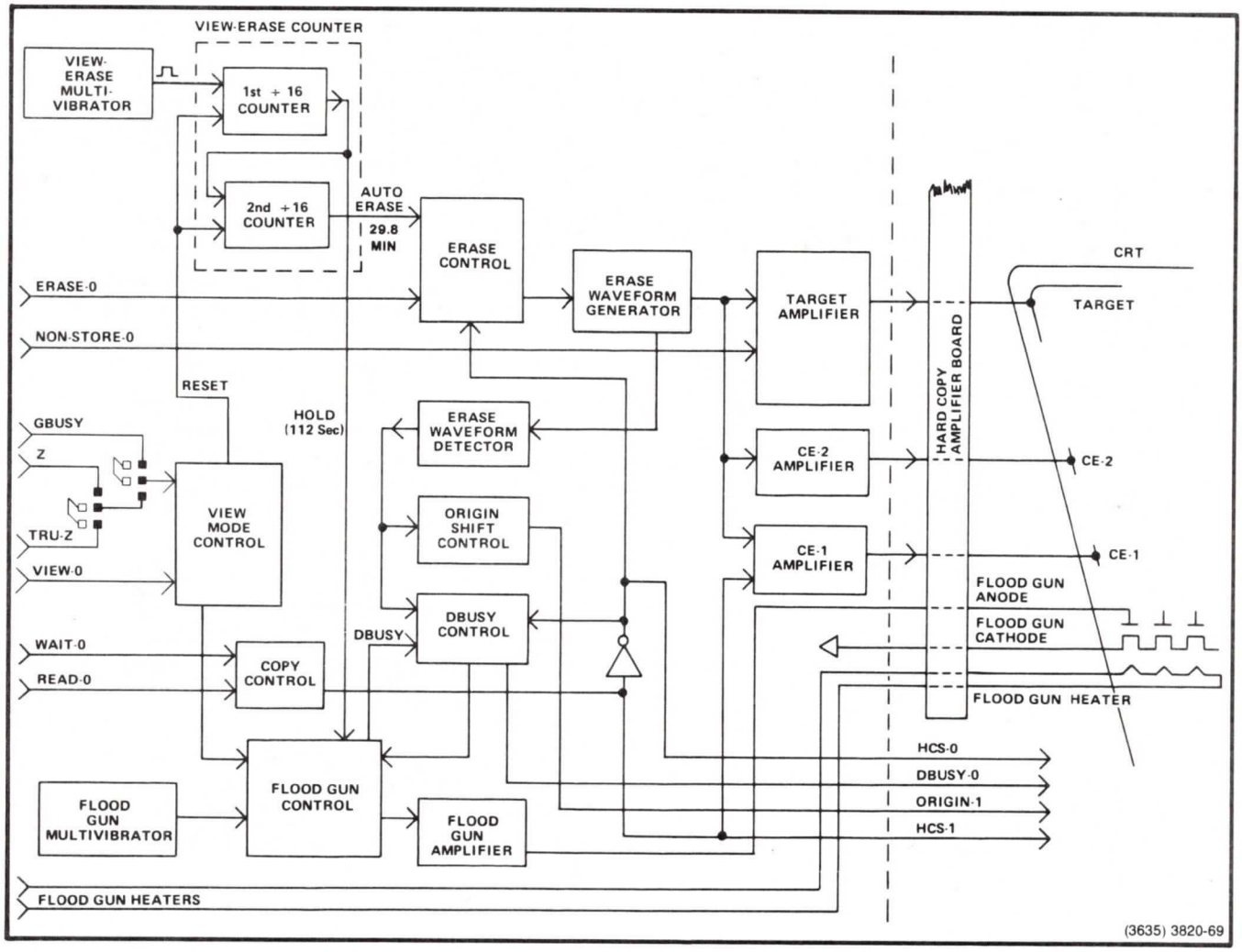

Figure 9-6. Storage Board Block Diagram.

Hold Mode

The Flood Gun Control circuitry is essentially a set-reset flip-flop that maintains a reset condition when the Display Module is in View mode. When the HOLD-0 line goes low (the first divide-by-16 counter clocks through its count, indicating 112 seconds of display inactivity), the Flood Gun Control flip-flop is set. The Flood Gun Control then transfers a 100 Hz signal with a 12 percent duty factor to the Flood Gun Amplifier. The Flood Gun Amplifier then pulses the flood gun anode at this rate, which reduces the intensity of stored information.
During Hold mode, the Flood Gun Control circuit sends a signal to the DBUSY Control circuit, which places a TTL low on the output DBUSY-0 line. This flags the pedestal that the Display Module is busy and cannot accept further information until the Display is brought out of Hold mode into View mode.

The Flood Gun Control circuit stays in Hold mode until reset (into view) with a Z AXIS signal (or GBUSY, depending upon the View Reset strap position) or a low on the VIEW-0 signal line to the View Mode Control. Notice that this is the same signal that resets the View-Erase Counters.

A one-shot multivibrator in the DBUSY Control circuit extends the length of the DBUSY-0 signal for 0.8 seconds longer than the hold and hard copy cycle it is protecting. This extra time allows the Display to stablize back into View mode.

Erase Cycle

An erase cycle can occur either automatically or by a direct command from the Display Controller or user.

Auto Erase

The 112 second, square wave signal that initiates Hold mode also starts a second divide-by-16 counter. When the output (auto erase) of this counter goes active (30 min), the screen is erased. The Erase Control circuit puts out an erase pulse that initiates an erase cycle of two complete erasures 100 ms apart. The Target Erase waveform goes to the Target via the Target Amplifier, and the CE-2 Erase waveform goes to CE-2 via the CE-2 Amplifier. (See Figure 9-7.)

An erase waveform, as it is applied to the Target or to CE-2, first goes positive and causes complete flooding of the Target (the fade positive portion). The ERASE signal then drops to zero volts to erase the Target and returns gradually to its operating level.

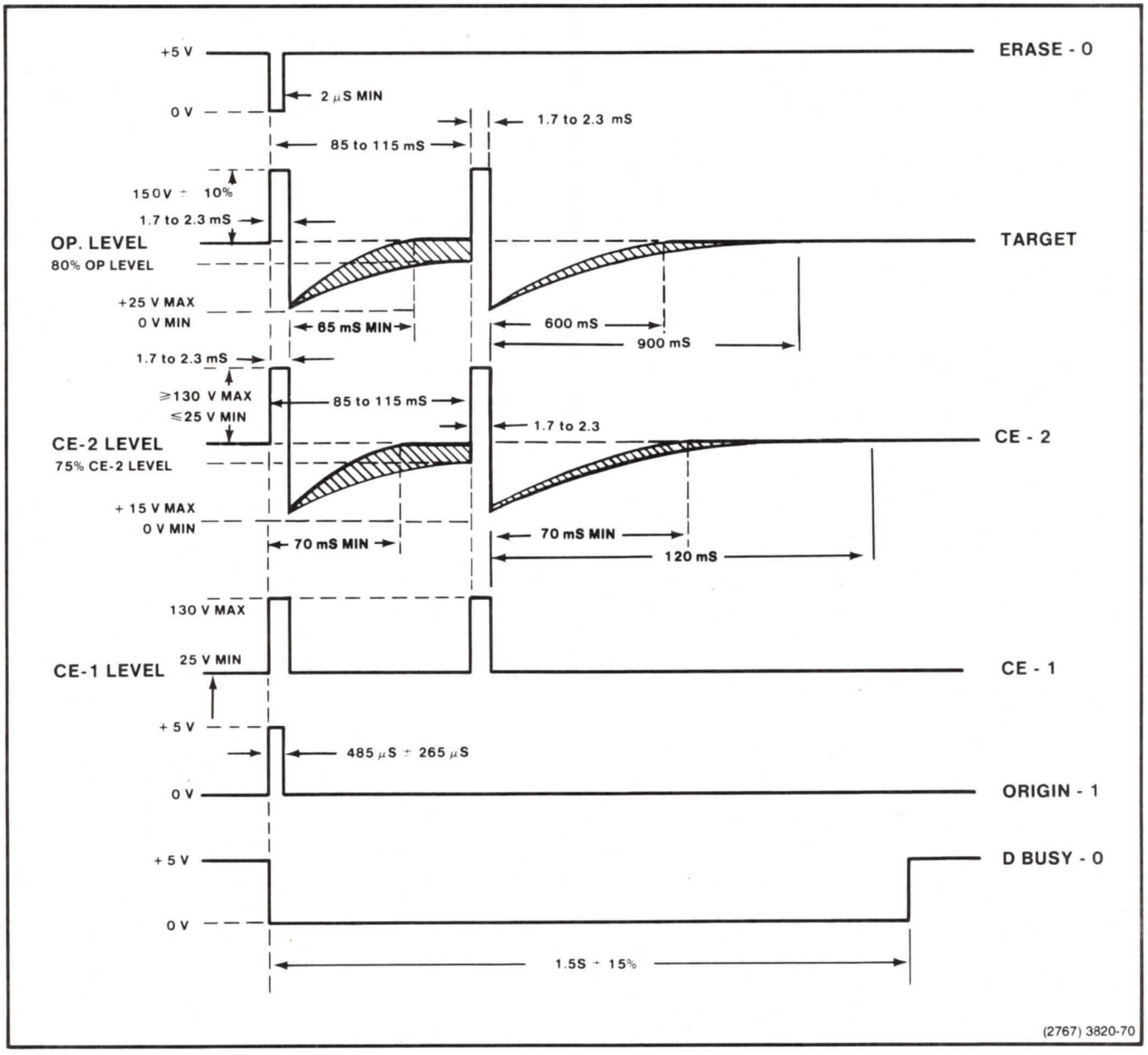

Figure 9-7. Typical Storage Board Waveforms.

Upon receipt of the erase pulse, the Erase Waveform Generator activates a 485 us, +5 V ORIGIN-1 pulse and a 1.0 second, low-going DBUSY-0 pulse. The ORIGIN-1 pulse is sent to the Deflection Amplifier board where it clocks the Origin Shift circuit. The DBUSY-0 signal is used by the Display Controller as a flag against further input to the Display. This gives the Display time to recover after an erasure.

Refer to the Storage board schematic, A13-1 and A13-2. U136B and its associated components form a protection circuit. This circuit guards against erasure when the second divide-by-16 counter, View Erase Counter, is reset by either a Z Axis signal or a low on VIEW-0 while counting past 891 seconds (the second half of the 30 minute automatic erase cycle). Without this protection, the counter could cause an undesired erasure of the screen before 30 minutes have passed.

Erase Command

An erase command into the Erase Control circuitry can come either from the Display Controller (through the ERASE-0 line) or from the keyboard PAGE key. This command has the same effect as the 30 minute auto erase signal.

A READ-0 or a WAIT-0 signal from the hard copy unit goes to Erase Control via Copy Control and prevents an erasure during a hard copy operation.

Bi-Stable Storage

The Display Module contains a bi-stable direct view storage crt. The crt consists of a display area and two separate types of electron guns. The display area consists of a glass front plate coated wth a transparent conductive layer called the target backplate. The target backplate is covered with a layer of insulating phosphor called the target or target phosphor.

The target, on which information can be displayed and stored, is bi-stable. The Display uses this bistable characteristic of the target for storage. The target backplate potential and flood gun electron beams establish the bi-stable operation of the phosphor. When the writing beam emitted by the second electron gun strikes the target phosphor, the target potential changes to a higher state.

The higher state (written area) is maintained by the flood gun beam current. In a similar manner, the flood gun beam current maintains the phosphor in the unwritten area of the target near ground potential. The difference in potential causes luminance (emitted light) in the written area and none in the unwritten area.

Target Amplifier

The Target Amplifier provides the operating voltage for the target backplate. The target backplate voltage is typically about +170 V during Storage mode. During the erase cycle, the target backplate voltage increases by 150 V for 2 ms. (See Figure 9-7.) This writes the entire screen by providing additional electron potential between the target phosphor and the flood guns. At the end of this period, the voltage drops to zero, erasing the target phosphor. Then the target voltage returns to operating voltage level at a rate such that the phosphor remains unwritten and assumes a ready-to-write state. The target backplate voltage can be set by the OP LEVEL adjustment for best storage.

During non-store operations, the target voltage is reduced to zero volts.

Collimation Amplifier

The Collimation Electrodes, CE-1 and CE-2, are electronic lenses that cause a uniform flood gun beam pattern over the target. CE-1 has a voltage set by the CE-1 potentiometer. During an erase cycle, the CE-2 electrode has a voltage pattern similar to that on the Target Backplate. (See Figure 9-7.) First the CE-2 voltage increases by 25 V to 130 V (adjustable by CE-2 Pulse potentiometer) for 2 ms. Then the voltage drops to zero and slowly returns to the operating level. The operating level is set by the CE-2 Level potentiometer.

During hard copy operation, +250 V is placed on CE-1 to prevent current oscillations within the crt that could degrade hard copy quality.

Flood Gun Amplifier

The Flood Gun Amplifier activates the flood guns with a positive voltage on the flood gun anode during View mode. This positive voltage causes a stream of electrons to accelerate toward the target. Their energy is insufficient to cause writing (except during a portion of the erase cycle). The flood gun electrons cause the excited or written portions of the phosphor on the display to emit light, thus making the stored display information visible.

Hard Copy Amplifier Board

Stored information on the crt is recovered and amplified by the Hard Copy Amplifier board. (See Figure 9-1.) The stored information is made available to the hard copy unit (HCU) from the TARSIG-0 output.

Whenever a hard copy is desired, the MAKE COPY-0 signal is applied to the HCU, where it causes several output signals. A READ-0 signal (and a WAIT-0 signal, if the HCU has multiplex capability) is applied to the Storage board indicating that a hard copy is either being made or will be made. The Storage board produces the HCS-0 (Hard Copy Switch) signal to enable hard copy operation in the Display Module. HCS-0 asserts DBUSY-0, which disables the pedestal during hard copy operation.

WAIT-0 is a flag for a hard copy with multiplex capability (more than one Display Module connected to a hard copy unit). WAIT-0 goes active to indicate to the display requesting a copy that another display is in process of making a copy. (Essentially, WAIT-0 is a "busy" signal.) The hard copy unit holds the copy request until the HCU is inactive, at which time it proceeds to make a copy of the requesting display's information.

The hard copy unit provides a negative-going slow ramp to the deflection circuits causing the Display Module to sweep once horizontally. As it sweeps, a succession of fast ramps are applied to the Y deflection circuits. This causes repetive vertical sweeps during the single horizontal sweep. When HCS-1 is high, the Channel Switch and Origin Shift on the Deflection Amplifier board select the SLOW RAMP and FAST RAMP analog signals for the deflection signals. During each fast ramp, the HCU supplies a repetitive interrogate signal (HC INTER-0) to the High Voltage and Z Axis board to turn on the writing beam (Z Axis). If previously stored data exists on the target at the position indicated by the deflection circuits, the resultant current in the target surface causes a TARSIG-0 signal from the Hard Copy Amplifier board. The HCU uses this signal to reproduce what is stored on the Display. TARSIG-0 permits both units to evaluate the same point on the display.

Low Voltage Power Supply

Refer to Schematic A12-1, Low Voltage Power Supply (LVPS), during the following description. The LVPS has several regulated and unregulated output voltages. The +15, -15, +5, and +290 V supplies are regulated. The unregulated outputs are the +490, +175, +20, -20, +9, and -9 V supplies.

NOTE

The crt flood guns are connected between the +15 and -15 V supplies. These are buses 5 and 6 on the Interconnect board.

The +15 V supply uses the unregulated +20 V supply for a source and is regulated by an integrated circuit. An adjustment allows the output of the +15 V supply to be set precisely at +15 V. The +15 V power supply provides for both the +15 V flood gun filament and the Display Module's +15V circuitry. The +15 V output current, through a power transistor mounted on the Display Module's rear heat sink, is limited to approximately 2.5 A.

The -15 V supply uses the unregulated -20 V supply for a source and is regulated by an operational amplifier. The operational amplifier uses the +15 V supply as a reference. The -15 V power supply provides current for the -15 V flood gun filament and the Display Module's -15 V circuitry. The -15 V output current, through a power transistor mounted on the Display Module's rear heat sink, is limited to approximately 2.5 A.

The +5 V supply uses the unregulated +9 V supply as a source and is regulated by a +5 V regulator (mounted near the capacitor bracket). Current is limited to approximately 8.5 A. The supply output is shorted to ground (through an SCR) should the voltage attempt to rise above approximately +5.8 V.

The +290 V supply uses a voltage divider, an operational amplifier, and a driver amplifier to control the conduction of a power transistor (mounted on the rear heat sink). The conduction of this power transistor (from the +20 V unregulated supply) determines the voltage level of the entire transformer winding. One tap of the transformer winding is held at a constant +290 V with respect to ground and is fused with a 0.25 A fuse.

Power Supply Fuses

The power supply fuses are listed in Table 9-2.

Table 9-2

POWER SUPPLY FUSES

Power Supply Voltage	Normal Current	Fuse Size (Protection)
+490 V (unregulated)	50 mA	0.15 A Fuse
+290 V (regulated)	150 mA	0.25 A Fuse
75 V (unregulated)	50 mA	0.15 A Fuse
+ 20 V (unregulated)	0.5 A	2 A Fuse
+ 9 V (unregulated)	3 A	5 A Fuse
- 9 V (unregulated)	3 A	4 A Fuse
- 20 V (unregulated)	0.5 A	2 A Fuse
+ 15 V (regulated)	2 A	2.5 A current limit
- 15 V (regulated)	2 A	2.5 A current limit
+ 5 V (regulated)	1 A	1.5 A current limit

During the erase cycle these currents can fluctuate appreciably, but the majority of the total currents are equivalent to the crt flood gun cathode current, which is specified at 190 mA maximum.

The total current drawn from both +9 and -9 V supplies should not exceed 3 A.

The crt flood guns are connected between +15V and -15V and draw 1.5 A nominally. This leaves 0.5 A nominally available for circuitry.

Section 10

ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains adjustment procedures for both the pedestal and display module parts of the terminal without any options installed. Some options for the terminal may require sightly different (or additional) adjustment procedures. If the terminal has any options installed, the service manuals for those options should be checked for variations on or additions to these adjustment procedures. The pedestal should always be adjusted before adjusting the display module so that the display vectors and measurments are correct for display adjustment.

PERFORMANCE CHECK

A performance check of the terminal circuitry is accomplished by means of Self Test. A limited test of circuitry is performed when the terminal goes through a power up sequence, or whenever the terminal is turned on. Self Test is also available for a more thorough check of the terminal circuitry. For more information on Self Test and failure codes, refer to Section 11 in this manual.

SELF TEST PATTERNS

This adjustment procedure uses patterns that are stored in ROMs in the pedestal. Whenever these patterns are needed, use the following procedure to display them on the crt screen.

1. Press the SELF TEST button and hold it in. This button is located on the front of the pedestal, below the keyboard, to the left of the MASTER RESET button.

2. Press the MASTER RESET button and then release it. The keyboard LED lights come on and go off as different parts of circuitry are tested.

3. After the keyboard LED lights begin to "cycle", release the Self Test button.

4. The terminal bell sounds at the start of the Self Test key check.

5. Press and hold the CONTROL and C keys at the same time and then release them. This displays a general "menu", which is a list of Self Test Routines.

6. From this menu, select Display -- the F1 key. This displays a second menu of the patterns to be used in adjusting the screen.

7. Once the menu has been displayed on the screen, it is not necessary to repeat the rest of Self Test in order to display the patterns needed for the adjustment procedure. Simply use CONTROL D to get back to the menu, and select the desired test pattern from this menu.

Self Test has the following commands, which can be used at any point in the Self Test procedure.

- CONTROL C. Displays the general menu.
- CONTROL D. Displays the current menu.
- CONTROL E. Exits from the current routine.
- SPACE BAR. Repeats the current pattern.

ABBREVIATED ADJUSTMENT PROCEDURES

This section is divided into two subsections, the first subsection describes the adjustment procedures for the pedestal part of the terminal. The second subsection describes the terminal display module adjustment procedure.

The abbreviated adjustment section precedes the detailed adjustment procedures.

NOTE

This abbreviated adjustment section is NOT a complete adjustment procedure. It does, however, serve as a checklist for the experienced service technician. For the complete adjustment procedures refer to "Pedestal Adjustment Procedure" and "Display Module Adjustment Procedure". THIS ABBREVIATED ADJUSTMENT SECTION DOES NOT CONTAIN "NOTES," "CAUTIONS," OR "WARNINGS."

Abbreviated Pedestal Adjustment

Gather the equipment necessary for adjusting the terminal, make sure the terminal is operating under performance specifications, remove the pedestal front panel, and do an inspection with the power off.

Low Voltage Power Supply

1. Install the 41XX Logic Extender board. (This board contains the test points needed for the power supply checks).

2. Check the +5.1 V supply (R685 adjustment) at TP 75 to make sure that the voltage lies within the tolerance of +5.105 V to +5.115 V.

3. Check the +12.00 V supply at TP 79 to make sure that the voltage lies within the tolerance of +11.88 V to +12.12 V.

4. Check the -5.2 V supply at TP 5 to make sure that the voltage lies within the tolerance of -5.05 V to -5.35 V.

5. Check the -12.00 V supply at TP 1 to make sure that the voltage lies within the tolerance of -11.88 V to -12.12 V.

6. Check the power supply ripple on the +5.1, +12.00, -12.00, and the -5.2 V supplies. All ripple should be below 100 mV.

7. Check for the INIT waveform at TP9 and the PDWN-INIT waveform at TP 75 during the power up and power down sequences. Refer to Figures 10-2 and 10-3.

8. Check for the PFAIL waveform at TP 7. Refer to Figure 10-4.

Display Controller Board

1. Display the Status message on the screen.

2. Using the letter "B" in the status message, adjust R1 and R3 for maximum vector closure. Figure 10-5 shows the location of R1 and R3.

Vector Generator Board

1. Install the Vector Generator board on the 41XX Logic Extender board.

2. Adjust R425 (X DAC offset) for a value of -4.950 V at TP 706 with the writing beam positioned to 0,0.

3. Adjust R426 (Y DAC offset) for a value of -4.873 V at TP 716 with the writing beam at 0,0.

4. Adjust R424 (X DAC gain) for a value of +4.950 V at TP 706 with the writing beam at 1023,4095.

5. Adjust R427 (Y DAC gain) for a value of +4.873 V at TP 716 with the writing beam at 1023,4095.

6. Check the values in steps 2, 3, 4, and 5 again for any changes.

7. Adjust R605 and R704 for the best waveform at TP 502 and TP 525 (externally triggered) while maintaining an optimum charge pump pattern on the display.

8. Turn off the terminal, remove the test board, install the Vector Generator board again, and replace the pedestal cover.

Abbreviated Display Adjustment

Gather the equipment necessary for adjusting the terminal, make sure the terminal is operating under performance specifications, remove the pedestal front panel, and do an inspection with the power off.

Low Voltage Power Supply

1. Turn on the terminal and press the PAGE key.

2. Do the following voltage and ripple checks, measured on the Interconnect board, for the following tolerances. The +15.00 V supply has the only adjustable voltage. R166 adjusts this.

Table 10-1

LVPS VOLTAGE TOLERANCES AND RIPPLE

Voltage	Voltage Tolerance	Maximum Ripple
+15 V (reg)	+14.97 V to +15.03 V	5 mV p-p
-15 V (reg)	-14.85 V to -15.15 V	5 mV p-p
+5 V (reg)	+4.8 V to +5.2 V	10 mV p-p
+12 V (unreg)	no tolerance (about +9 V)	1.5 V p-p
-12 V (unreg)	no tolerance (about -9 V)	1.5 V p-p
+20 V (unreg)	no tolerance	1.2 V p-p
-20 V (unreg)	no tolerance	1.2 V p-p
+175 V (unreg)	no tolerance	7.0 V p-p
+290 V (reg)	+287.0 V to +293.0 V	100 mV p-p
+490 V (unreg)	no tolerance	5.0 V p-p

High Voltage Check

1. Check pin 3 of the crt for -5700 V to -6300 V at 120 Vac. Make sure that it does not vary more than +,-60 V at 108 Vac and 132 Vac.

Storage Board

1. Check TP 91 for 142.5 V to 157.5 V.

2. Adjust R295 (OP LEVEL) so that the crt gets bright but does not store. Check the OP LEVEL voltage at TP 94.

3. Adjust R198 (CE-2) for a flood gun pattern 1/16 inch from the edge of the phosphor. Check the CE-2 voltage at TP 93.

4. Adjust R197 (CE-1) for uniform background illumination. The CE1 voltage at TP 92 should be about 5 V higher than CE-1. Make sure that oscillation does not occur due to the interaction between R197 and R198.

5. Place the DVM probe on TP 91 and press PAGE. The voltage should not change during erasure.

Storage Board Erase Waveforms

1. Turn the power off, change the N/TEST jumper to "TEST", and turn the power back on. Note that the screen erases every 3 seconds.

2. Check for the Figure 10-14 waveform at TP 94, and verify that its parts conform to the waveforms in Figures 10-15 and 10-16.

3. Check for the CE-2 waveform at TP 93 and verify that its shape conforms to the waveform in Figure 10-17.

4. Check for the CE-1 waveform at TP 92 and verify that its shape conforms to the waveform in Figure 10-18.

5. Adjust R95 (CE-1 Pulse Control) while erasing the screen and observing the edges of the screen for full coverage.

6. Adjust R195 (CE-2 Pulse Control) while erasing the screen observing the edges of the screen for full coverage. The OP LEVEL, CE-1, and CE-2 adjustments interact.

7. Turn the power off, change the N/TEST jumper to "N", and turn the power back on.

Flood Gun Anode

1. Press the PAGE key and make sure that Hold mode lasts for 90 to 135 seconds.

2. Check for the waveform in Figure 10-19 at TP 91 on the Storage board while the terminal is in Hold mode.

3. Check for a TTL low on Pin 43 of the Interconnect board while the terminal is in Hold mode.

Grid Bias

1. Turn the power off, move the antiburn strap from "IN" to "OUT", and turn the power back on.

2. Adjust R429 (CRT BIAS on the HV & Z Axis board) clockwise until a low intensity dot appears in one corner of the cursor. Retrace lines also appear around the cursor. Adjust R288 (CENTER FOCUS on the HV & Z Axis board) for a well-focussed dot, then adjust R429 until the dot just disappears.

3. Measure the voltage at C429 on the HV & Z Axis board and increase by +5 V by adjusting R429 counterclockwise.

4. Turn the power off, move the antiburn strap from "OUT" to "IN", and turn the power back on.

Normal Intensity

1. Press and hold down a character key and observe the Figure 10-20 waveform at the top of R246 on the HV & Z Axis board.

2. Adjust R427 for a 40 to 50 V difference between the most positive points ("crests") of adjacent pulses.

Origin Shift

1. Press the PAGE key eight times and watch for seven consecutive origin shifts, with the cursor returning to the upper right on the eighth.

Frequency Compensation

1. Display the X COMP pattern (key F3) by using the Self Test procedure.

2. Adjust R51 and R150 on the Deflection Amplifier board so that only one line can be seen. Refer to Figure 10-21.

3. Display the Y COMP pattern (key F4).

4. Adjust R69 and R167 on the Deflection Amplifier board so that only one line can be seen. Refer to Figure 10-21.

Gains, Positioning, and Geometry

1. Display the GAIN pattern (key F2) by using the Self Test procedure.

2. Adjust the yoke for a straight, vertical line in the middle of the pattern.

3. Adjust R250 and R267 on the Deflection Amplifier board so that the left and right vertical line midpoints and the top and bottom horizontal line midpoints are equidistant from the edges of the crt.

4. Adjust R326 on the Deflection Amplifier board for the straightest top line.

5. Measure the straightness of the bottom horizontal line.

6. Adjust R322 on the Deflection Amplifier board for the straightest lefthand vertical line.

7. Measure the straightness of the righthand vertical line.

8. Check for excessive deviation from an ideal, straight line in the top horizontal line. If there is none, tighten the yoke.

Orthogonality

1. Check for no more than ±1.2 degrees deviation from 90 degrees where the lines cross in the middle of the screen.

Dynamic Focus

1. Display the GAIN pattern (key F2).

2. Adjust R424 on the Deflection Amplifier board so that the waveform changes less than 2 V as the Corner Focus adjustment is adjusted. Measure the voltage at R235 on the HV & Z Axis board. See Figure 10-22.

Slu-O

1. Display the X COMP pattern.

2. Check for a TTL pulse at Pin 36 of the Interconnect board.

Focus

1. Display the FOCUS pattern.
2. Adjust R288 and R128 on the HV & Z Axis board for the best center and corner focus while the pattern is writing.

Dropout

1. Display the HARD COPY pattern, wait 2 1/2 minutes, and then press the SHIFT key.
2. Increase the OP LEVEL or NORMAL intensity adjustments in 5 V increments and repeat step 1 until the minimum number of breaks are seen.

Brite Intensity and Defocus

1. Display the DEFOCUS pattern.
2. Adjust R415 on the HV & Z Axis board for 10 V higher than the NORMAL INTENSITY level. See Figure 10-24.
3. Adjust R34 on the HV & Z Axis board for a difference in characters as they are displayed.

Write-Thru Intensity

1. Press the LOCAL key. Then press the ESC key followed by the CONTROL and Z keys at the same time. Use the thumb- wheels to control the cross-hairs.
2. Adjust R227 so that the lines disappear when the REFRESH INTENSITY control is fully counterclockwise and the lines store when REFRESH INTENSITY is fully clockwise.

Hard Copy

1. Connect a 4631 Hard Copy Unit, display the GRAPHIC pattern, press the HARD COPY key, and check for dimming of the screen during scanning.

2. Check pin 43 on the Interconnect board during a scan for TTL low.

3. Adjust R226 on the HV & Z Axis board for a non-storing, visible sweep during scanning.

4. Adjust R229, R426, R228, and R227 on the Deflection Amplifier board so that a scan covers the pattern with an additional 1/8 inch beyond each edge.

5. Adjust R226 for a scan just below storage level.

6. Adjust R26 on the HC Amplifier board for high contrast copies without noise. Compare three copies.

7. Press PAGE, turn off the terminal, and install the cabinet cover again.

Refer to the of the pedestal and display module adjustment procedures for a detailed description.

WARNING

The following adjustment procedures may expose the service technician to voltage levels that are potentially lethal. To avoid a potentially dangerous situation, all servicing should be done by authorized service technicians using proper servicing techniques and equipment.

PEDESTAL ADJUSTMENT PROCEDURE

Introduction to the Pedestal Adjustment Procedure

The following procedure adjusts the pedestal for optimum performance. For continued optimum performance of the terminal, check -- and adjust if necessary -- both the pedestal and display module every 1000 hours of operation or every twelve months if the terminal is used infrequently.

NOTE

If the display module is to be adjusted, this procedure must precede the display module adjustment procedure. If this is not done, measurement concerning vector placement, closure, and reproducibility in the display adjustment will not be correct. Since the Display Controller board requires visually adjusting a pattern on the screen, this adjustment should be done on a properly adjusted display module.

Test Equipment Required

- Oscilloscope (TEKTRONIX 485 or equivalent). Dual trace with a vertical deflection factor of at least 5 mV per division, and a sweep rate of at least 10 ns per division.
- Two 10X oscilloscope probes with 50 ohm terminators.
- One 1X oscilloscope probe to be used for external triggering.
- Digital Voltmeter (DVM) (TEKTRONIX DM 501 or equivalent). Range of -30 V to +30 V with at least 0.1% accuracy. This meter needs a range of -30V to +600V for adjusting the display module, if it is to be used for the display module adjustment procedure too.
- Adjustment tool. Non-conductive. One small screwdriver about 5.0 inches in overall length.

- Power module (TEKTRONIX TM 503 or equivalent). Needed if a TEKTRONIX DM 501 digital multimeter is used.
- Set of hand tools for hardware adjustment checks. Should include nut drivers, screwdrivers, etc.
- 41XX Logic Extender board (TEKTRONIX part number 670-5291-00).
- Ribbon Extender Cable.
- Small flash light -- such as a penlight.

Performance Conditions

The following three conditions must be met before the pedestal can be adjusted properly. They must also be met before the characteristics and performance specifications are valid.

- The pedestal must be adjusted at room temperature -- 20 to 30 degrees C (68 to 86 degrees F).
- The pedestal must be connected to the display module with the AC Display Power Cord. And the display module signal cable must connect to J3000 of the pedestal.
- The terminal -- both pedestal and display module -- must have power applied for at least 20 minutes.

Inspection

WARNING

Hazardous voltages are present in the terminal circuitry. Always use proper servicing techniques to avoid being injured. Only qualified service technicians should perform the following inspection procedure. Before doing this inspection procedure, MAKE SURE THE POWER CORD IS DISCONNECTED FROM THE AC POWER OUTLET.

1. Remove the cover from the front of the pedestal. This is done by loosening the six screws shown in Figure 10-1 and gently pulling forward on the cover. There are two press-fit fasteners at the top of the front panel.

2. Check for loose, damaged, or improperly mounted hardware.

3. Make sure that circuit boards are installed in the correct slots.

4. Make sure that board level numbers are correct and that circuit modifications are installed correctly.

5. Make sure that all the ground straps going to all the rear connectors are screwed tightly to the chassis.

6. Check all wiring, ribbon cables, and harmonica connectors for proper installation.

7. Check edge connectors and Motherboard insert connectors for damage.

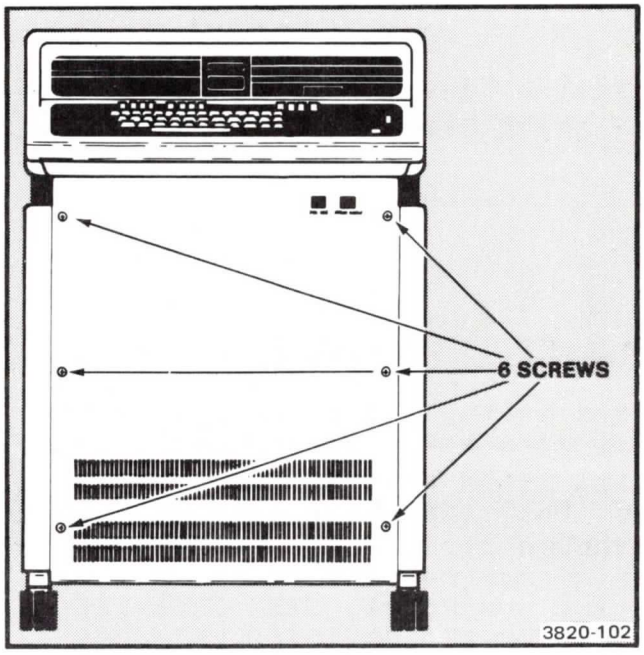

Figure 10-1. Pedestal Front Cover Screw Locations.

8. Inspect for the proper fuse for the specified line voltage and that the voltage range indicator is properly set for the line voltage that the terminal is being run from.

9. On any extended RAM Options (Options 24 though 28) make sure the jumpers are set sequentially from RAM board to RAM board. (one jumper per board). That is, one RAM board will start at a certain hexidecimal address. If there is another RAM board installed, it should start at the next pin designation (where the previous board left off). Example, if there are four optional RAM array boards installed, the first board should have the jumper set on the bottom set of pins, the second board should have the jumper set on the second set of pins, and so forth, on up to the fourth set of pins for the fourth board.

10. On the RAM/ROM board, refer to schematics A5-1,2,3 for the proper settings of J122 through J128. These settings should be factory preset for the factory ROM's and should not have to be moved.

11. On the Vector Generator board, there should be NO strap on J601. A strap on this jumper will override the charge pump and the display will not work properly.

WARNING

Hazardous voltages are present in the terminal circuitry when the terminal is on. Always use proper service techniques to avoid being injured. Only qualified service technicians should perform the following adjustment procedure.

Pedestal Adjustment Procedure

Low Voltage Power Supply

1. Disconnected the ac power cord and remove the pedestal front panel.

2. Remove the pedestal right side panel. Pull the panel out from the bottom. Use a flat-bladed screwdriver to pry the panel a short distance from the frame. This panel is not screwed on and loosens suddenly when pulled far enough away from the frame.

3. Insert the 41XX Logic Extender board into any open slot in the card cage.

4. Connect the ac power cord again and turn on the terminal.

CAUTION

Make sure that a bright spot does not appear on the screen during the first minute or so of operation. If a bright spot does appear, TURN THE TERMINAL OFF IMMEDIATELY. This could cause a phosphor burn and, thus, permanently damage the crt.

NOTE

The locations of the following test points are printed on the 41XX Logic Extender board, along with the signals and voltages at those test points.

5. Connect the positive lead of the DVM to TP 75 of the 41XX Logic Extender board. This is the +5 V TP. Use TP 77 as a ground.

6. Adjust R685 on the LVPS board for a value of 5.105 V to 5.115 V. R685 is adjusted through a hole in the chassis on the upper right side. Use a pen-light to help locate R685.

7. Move the DVM lead to TP 79 of the 41XX Logic Extender board -- the +12 V TP. Make sure that the voltage is between +11.88 V and +12.12 V.

8. Move the positive lead of the DVM to TP 77 and the negative lead to TP 5 -- the -5.2 V TP. Check for a value between -5.05 V and -5.35 V.

9. Leave the positive lead of the DVM at TP 77, and move the negative lead to TP 1. Check for a value between -11.88 V and -12.12 V.

NOTE

The pedestal power supply also has a +24 V regulated supply. This voltage is not used in the standard instrument. If options 42 or 43 are installed, this voltage can be checked. Consult the Option 42/43 Service Manual for this voltage check.

10. Remove the DVM leads.

NOTE

In the following peak-to-peak voltage (ripple voltage) checks, the signal may appear quite noisy and distorted, but should remain within the specified tolerances.

11. Set the oscilloscope as follows.

Triggering

- o Mode: AUTO
- o Coupling: AC
- o Source: CH 1
- o Slope: "+"
- o Level: set near zero

Channel 1

- o Volts/division: 50 mV/div
- o Coupling: AC

Set Time/division to 10 us/div.

12. Check ripple voltage with the oscilloscope at the voltage test points for the following values.

Test point	Voltage	Ripple value
75	+5.11 V	less than 100 mV.
79	+12.00 V	less than 100 mV.
5	-5.2 V	less than 100 mV.
1	-12.00 V	less than 100 mV.

13. Turn off the terminal and replace the right side cover, but do not replace the front pedestal cover or remove the 41XX Logic Extender board.

INIT and PFAIL

1. Set the following oscilloscope adjustments:

- o Triggering mode: CH 1
- o Channel 1 Volts/division: 2V/div
- o Channel 1 coupling: DC
- o Vertical Mode: CH 2
- o Channel 2 Volts/division: 2V/div
- o Channel 2 coupling: DC
- o Channel 2 signal: INVERT
- o Time/division: 10ms/div

2. Attach the channel 1 oscilloscope probe to TP 75 (+5.0 V) on the 41XX Logic Extender board.

3. Attach the channel 2 oscilloscope probe to TP 9 (INIT) on the 41XX Logic Extender board.

4. Turn on the terminal while watching for the INIT waveform on the oscilloscope. See Figure 10-2.

5. Verify that the observed pulse is at least 40 ms long.

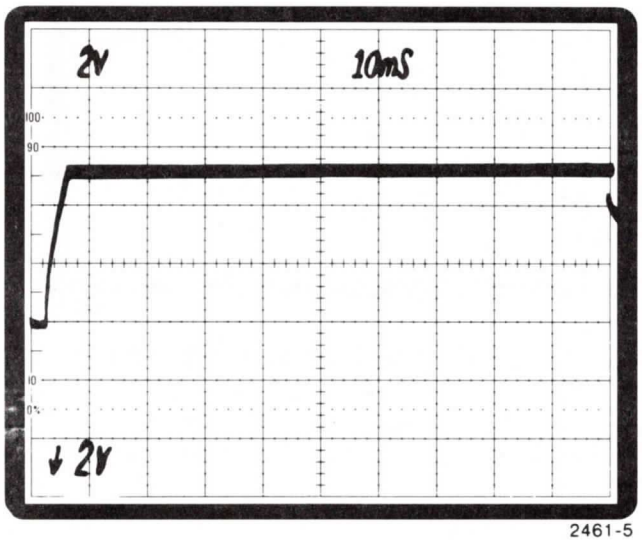

Figure 10-2. INIT Waveform.

6. Set the following oscilloscope adjustments.

   - o Trigger source: CH 2
   - o Time/division: 0.2 ms/div

7. Turn off the terminal while watching the oscilloscope for a PDWN-INIT signal. See Figure 10-3. Do not disconnect the oscilloscope probes.

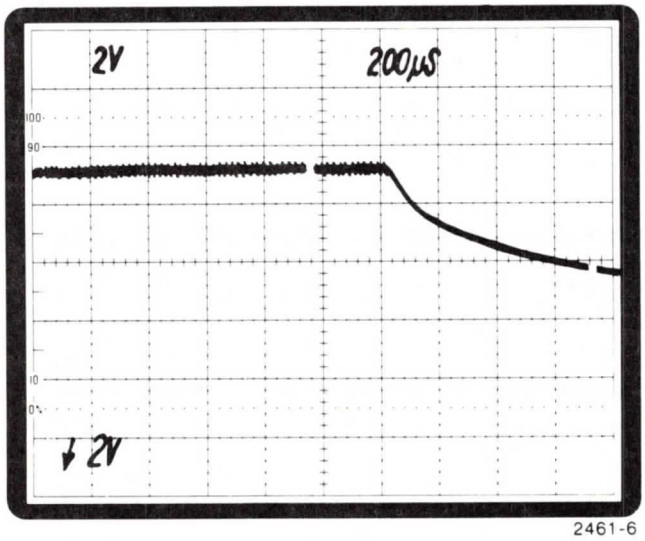

Figure 10-3. PDWN-INIT Signal.

8. Set the following oscilloscope adjustments.

   Trigger

   - o Source: channel 1
   - o Slope: "-"
   - o Level: "Just triggers when the terminal is on."

   Set the time/division to 1 ms/div.

9. Move the channel 1 probe to TP 7 (PFAIL-0) on the 41XX Logic Extender board.

10. Turn on the terminal and allow it to stabilize. The level adjustment may have to be adjusted so that the oscilloscope is triggered properly.

11. Turn the terminal off while watching the oscilloscope for a PFAIL waveform. See Figure 10-4. Verify that the pulse generated is a minimum of 2 ms.

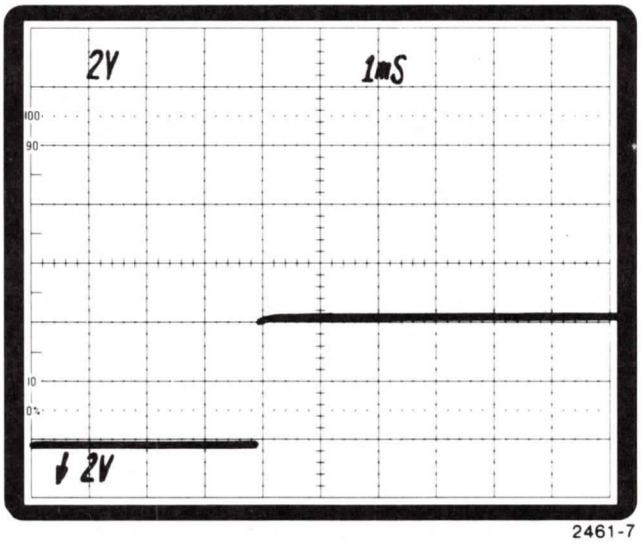

Figure 10-4. PFAIL Waveform.

12. Remove the oscilloscope probes.

Display Controller Board Adjustments

NOTE

Since the Display Controller board uses a display pattern for adjustment, this adjustment procedure should be done on a previously adjusted display module.

1. Turn on the terminal.

2. Press the LOCAL, DIALOG, and SET UP keys on the keyboard. Make sure that the LED light in each key is on.

3. Type the letters "STA". This command (STATUS) displays the terminal parameters in the dialog area of the screen. Adjust the REFRESH INTENSITY control on the display if the message is difficult to see. (Adjust the REFRESH INTENSITY so that it is just below storage level.)

4. Find the letter B in the status message. Use the vertical thumbwheel to scroll the message.

5. Adjust R1 and R3 on the Display Controller board for maximum vector closure at both ends of a vector. The letter B consists of a good number of vectors to work with. If R1 or R3 is adjusted too far, a bright spot appears at one end of the vector, depending on which resistor is adjusted. Adjust the vectors so that the bright spots are just barely perceptible. Figure 10-5 shows the locations of R1 and R3.

NOTE

If a bright dot appears and stores while the adjustment is being made, erase the screen and display the status message again before continuing. It is not always possible to eliminate all bright spots and gaps between vectors at the same time. Work with the Display Controller board adjustments until an optimum character is obtained.

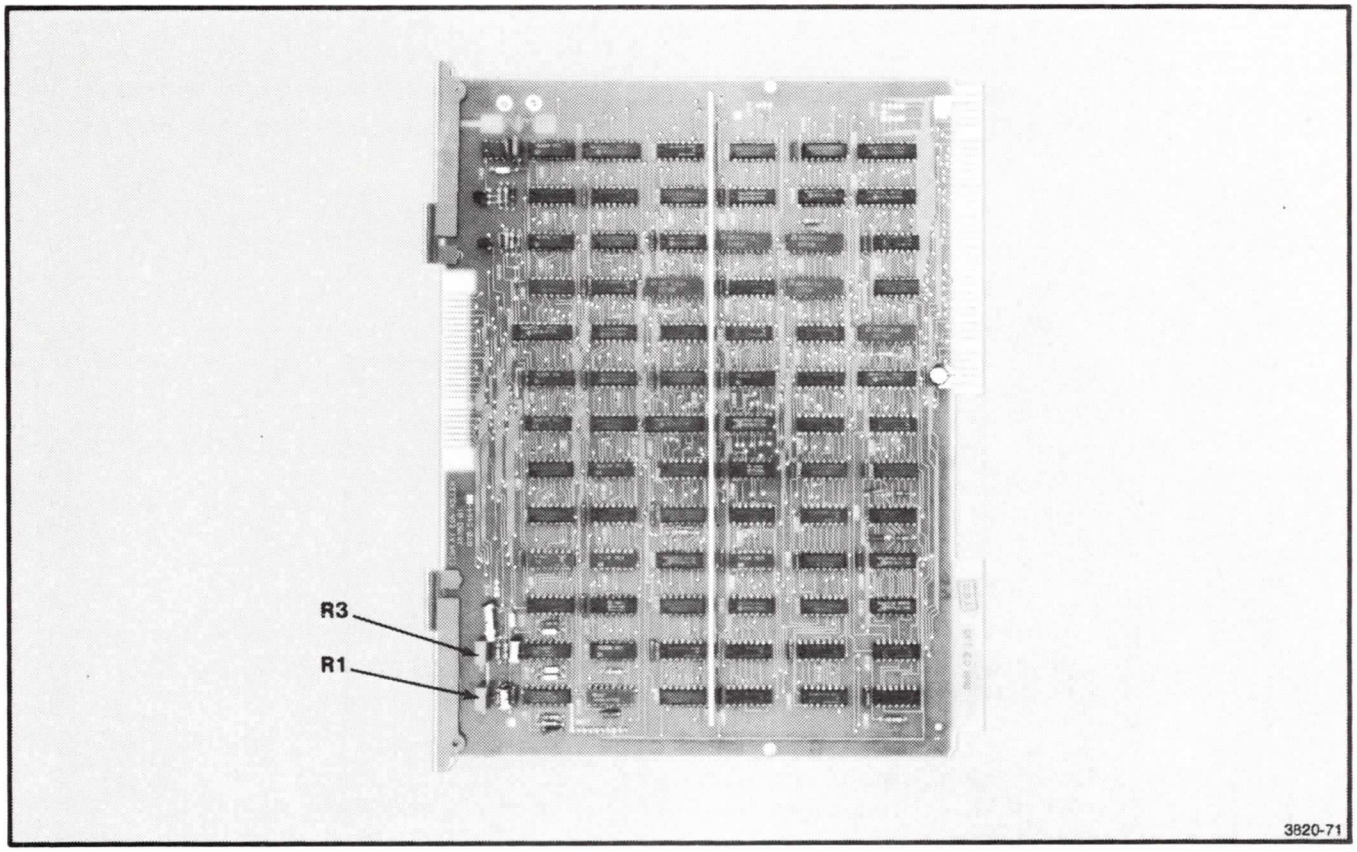

Figure 10-5. Display Controller Board Adjustments.

Vector Generator Board Adjustments

1. Turn off the terminal.

2. Remove the ribbon cable from the Vector Generator board.

3. Remove the Vector Generator board from the card cage and install it on the end of the 41XX Logic Extender board.

4. Connect the extended ribbon cable from the end of the original cable to the end of the Vector Generator board.

5. Turn on the terminal.

6. Use Self Test to display the main Self Test menu and then select "display" by pressing the F1 key. See Figure 10-6.

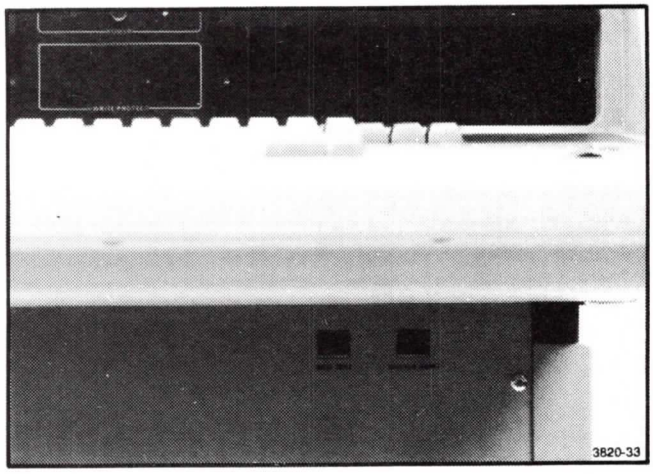

Figure 10-6. SELF TEST and MASTER RESET Buttons.

7. Position the writing beam to X and Y coordinates 0,0 by pressing the F7 key.

NOTE

All measurements made with the DVM are made with ground as the reference.

8. Connect the DVM lead to TP 706 and adjust R425 (X DAC offset) for a value of -4.950 V. See Figure 10-7.

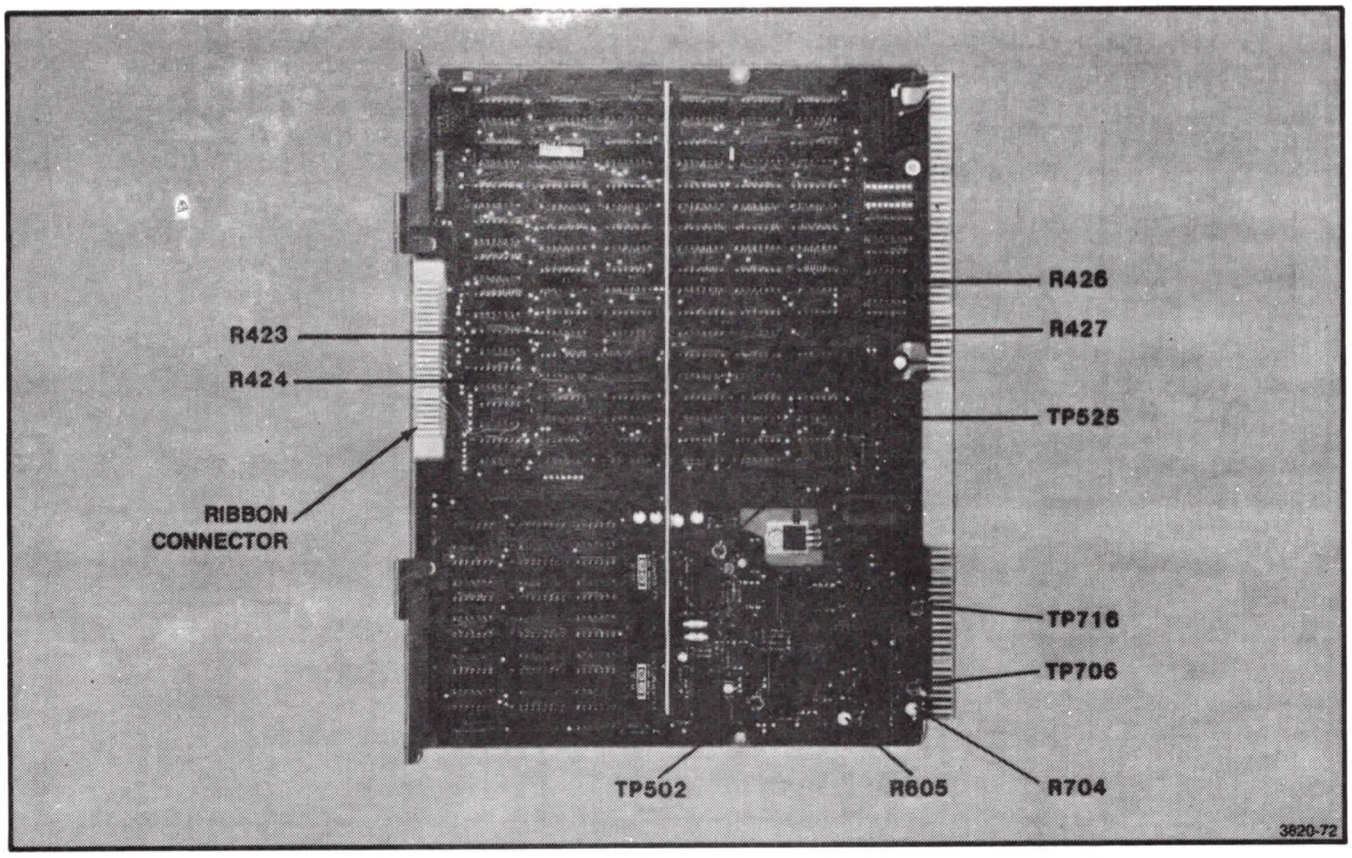

Figure 10-7. Vector Generator Board TP and Adjustments Locations.

9. Move the DVM lead to TP 716 and adjust R426 (Y DAC offset) for a value of -4.873 Vdc.

10. Position the writing beam to X and Y coordinates 1023,0FFF by pressing the F8 key.

11. Move the DVM lead back to TP 706 and adjust R424 (X DAC gain) for a value of +4.950 Vdc.

12. Move the DVM lead to TP 716 and adjust R427 (Y DAC gain) for a value of +4.873 Vdc.

13. Return to the 0,0 coordinates by pressing the F7 key.

14. Check the voltages at TP 706 and TP 716 again to make sure that they match the adjusted values in steps 9 and 10. If they do not match, readjust R425 and R426. If R425 and R426 are readjusted, readjust R424 and R427 a second time.

15. Set the oscilloscope to the following settings.

    Trigger

    - Mode: NORM
    - Slope: "+"
    - Trigger Source: EXT
    - Level: set near zero
    - Coupling: DC

    Set vertical mode to CHOP
    Set CH 1 & CH 2 V/division to 0.5 V/div
    Set CH 1 & CH 2 ac/gnd/dc switches to DC
    Set time/division to 20 us/div
    Set Horizontal Display to "A"

16. Insert the channel 1 test probe into TP 502.
    Insert the channel 2 test probe into TP 525.
    Connect the external trigger to the ABS-0 signal -- the junction of R603 and R604.

17. Press the SHIFT and F1 keys to obtain the charge pump pattern.

18. Adjust the slope level on the oscilloscope, if necessary, towards positive triggering. Observe on the oscilloscope a pattern similar to the one in Figure 10-8.

19. Note points 1 and 2 on Figure 10-8. Adjust R605 to align these points as close to the central horizontal axis as possible. See Figure 10-9.

20. Note points 3 and 4 on Figure 10-8. Adjust R704 to align these points as close to the central horizontal axis as possible.

21. Repeat steps 20 and 21 as needed until the best compromise between points 1 & 2 and 3 & 4 -- R605 and R704 adjustments -- is reached. Note that R605 and R704 interact.

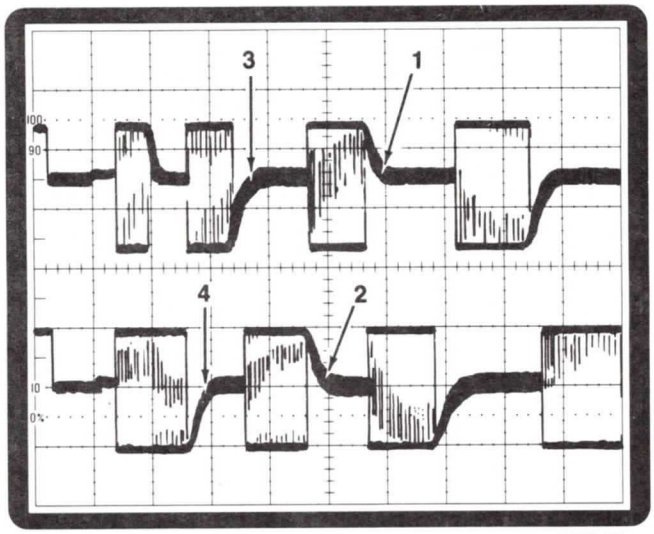

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Figure 10-8. Charge Pump Waveform.

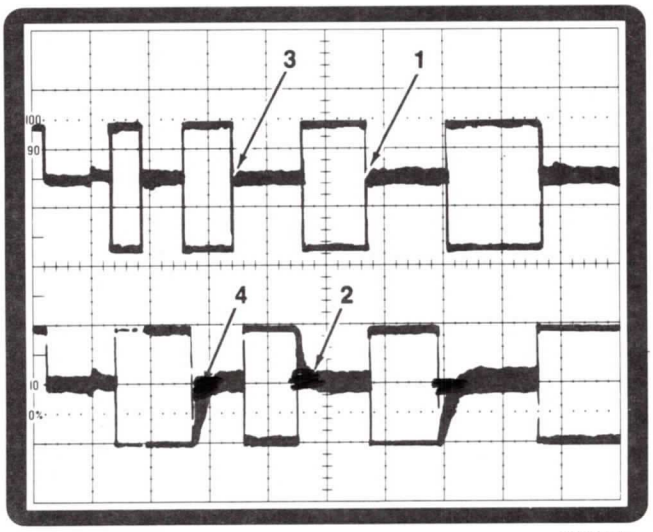

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Figure 10-9. Adjusted Charge Pump Waveform.

NOTE

It is not possible to get all the points in a perfectly horizontal plane simultaneously. The optimum adjustment is a good compromise. Watch the pattern on the display, while observing these adjustments, and adjust for the optimum-appearing vectors on the display while adjusting for the optimum-appearing pattern on the oscilloscope.

22. Turn off the terminal.

23. Remove the oscilloscope probes from the test points and the external trigger from ABS-0.

24. Remove the 41XX Logic Extender board and ribbon cable, and push the Vector Generator board into its proper card cage slot.

25. Replace the front pedestal panel.

This completes the adjustment procedure for the pedestal.

DISPLAY ADJUSTMENT PROCEDURE

Introduction to the Display Adjustment Procedure

The following adjustment procedure describes the adjustment of the display module for optimum performance. This procedure is also used to check the performance specifications of the display. For continued optimum performance, check -- and adjust if necessary -- every 1000 hours of operation or every twelve months if the terminal is used infrequently.

NOTE

In order to adjust the instrument, the cabinet cover and front panel must be removed. See the cabinet cover and front panel removal and installation procedures in Section 11.

Test Equipment Required

- Oscilloscope (TEKTRONIX 465 or equivalent). Dual trace with a vertical defection factor of at least 5 mV per division, and a sweep rate of at least 10 ns per division. Bandwidth from dc to 100 MHz.
- Digital Voltmeter (DVM) (TEKTRONIX DM 501 or equivalent). Range -30 V to +600 V with at least 0.1% accuracy. Measurement to -6400 V with 1% accuracy (if no divide-by-10 high voltage probe is used).
- TEKTRONIX 4631 Hard Copy Unit. Used for adjusting copy-making circuitry which must be adjusted if the terminal is used with a Hard Copy Unit.
- Adjustment Tools. Non-conductive. One screwdriver at least 10.0 inches in overall length, one at least 5.0 inches in overall length, and a third 1.0 to 2.0 inches in length.
- Power Module (TEKTRONIX TM 503 or equivalent). Used with the TEKTRONIX DM 501 Digital Multimeter.
- High Voltage Probe. Divide-by-10 test probe used in measuring the high voltage supply. Divide-by-100 or divide-by-1000 probes can also be used in measuring this voltage. The DVM should be adjusted for the different voltage ranges.
- Set of hand tools for hardware adjustment checks. Should include nut drivers, screwdrivers, etc.

Performance Conditions

The following two conditions must be met before the display characteristics and performance specifications are valid.

- The Display must be adjusted at room temperature -- 20 to 30 degrees C.
- The Display must have power applied for at least 20 minutes.

Inspection

WARNING

Hazardous voltages are present in the terminal circuitry. Always use proper servicing techniques to avoid being injured or killed. Only qualified service technicians should perform the following inspection procedure. Before doing this inspection procedure, MAKE SURE THE POWER CORD IS DISCONNECTED FROM THE AC POWER OUTLET.

1. Check for loose, damaged, or improperly mounted hardware.
2. Make sure that circuit boards are installed in the correct slots.
3. Make sure that board level numbers are correct and that circuit modifications are installed correctly.
4. Check the crt and shield for foreign material and scratches.
5. Make sure the crt ground straps are screwed tightly to the chassis.
6. Check all wiring and harmonica connectors for proper installation.
7. Check edge connectors and Interconnect board pins for damage.
8. Check the crt filter for proper installation; also, make sure that the ground clips are securely fastened.
9. Make sure that the crt socket is properly connected.

10. On the HV & Z-Axis board, make sure that the two Z-Axis jumpers are moved to the Z-0 position (inner position). Also, make sure that the board has a 1 A fast blow fuse in place. The location of these two jumpers as well as the potentiometer adjustments is shown in Figure 10-10.

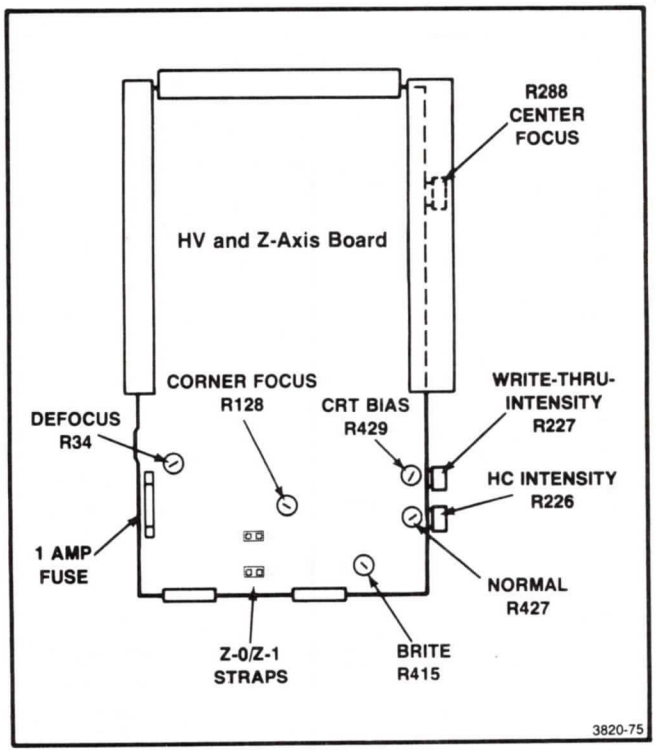


Figure 10-10. High Voltage and Z Axis Board Straps and Adjustments.

11. On the Storage board, make sure that the VIEW RESET jumper is set to the GB (lower) position, and also that the Z-TRU-Z jumper is set to the TRU-Z (lower) position. Set the NORMAL/TEST jumper to the "N" (top) position. For the location of these straps, the test points, and adjustments, see Figure 10-11.

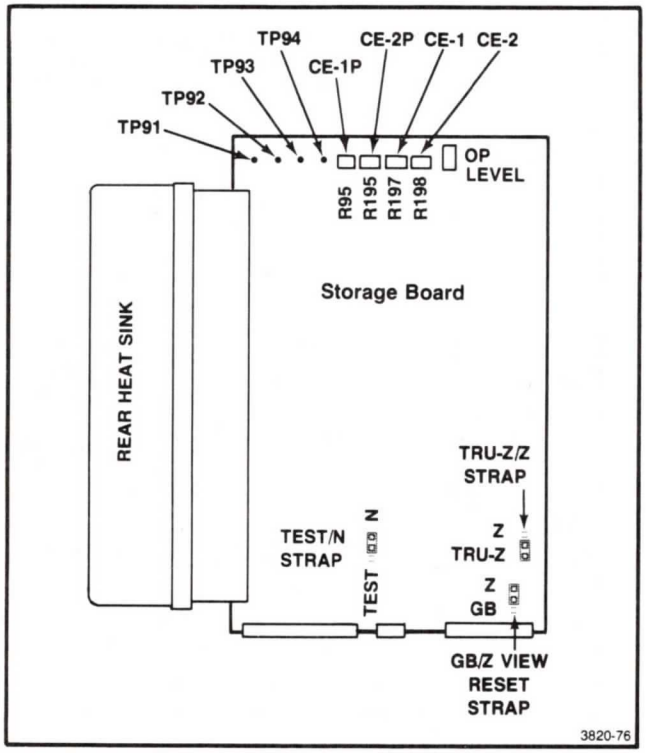


Figure 10-11. Storage Board Straps, Test Points, and Adjustments.

12. On the Deflection Amplifier board, set the ANTI-BURN jumper to the IN (lower) position. Check the J311 and J314 straps for proper installation. Make sure that the J199 4-pin jumper is set to the FAST position. And make sure that the Hold mode jumper is set to the IN position (toward the rear). See Figure 10-12 for a diagram of the Deflection Amplifier board describing the straps, test points, and adjustments.

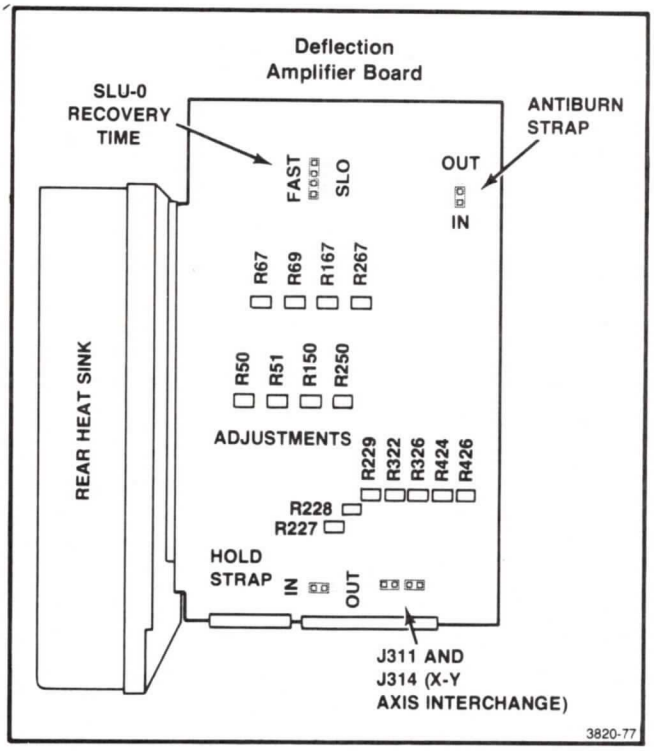


Figure 10-12. Deflection Amplifier Board Straps, Test Points, and Adjustments.

13. On the Hard Copy board, make sure that the harmonica plugs are correcly installed, and that no parts are shorted together. Also, make sure that the "Danger Warning" is in place on the plastic shield. Check the attaching screws for secureness.

14. On the Low Voltage Power Supply (LVPS) board, check the cables from the power supply to the Interconnect board for defects. Make sure that all wiring is fastened securely. Make sure that the line fuse is securely seated. Also, make sure that the following fuses have the correct ratings and are installed correctly. See Figure 10-13 for the location of these fuses.

F30	0.15 A fast
F35	0.25 A fast
F137	0.15 A fast
F139	2.00 A fast
F141	2.00 A fast
F144	5.00 A slow
F146	4.00 A slow

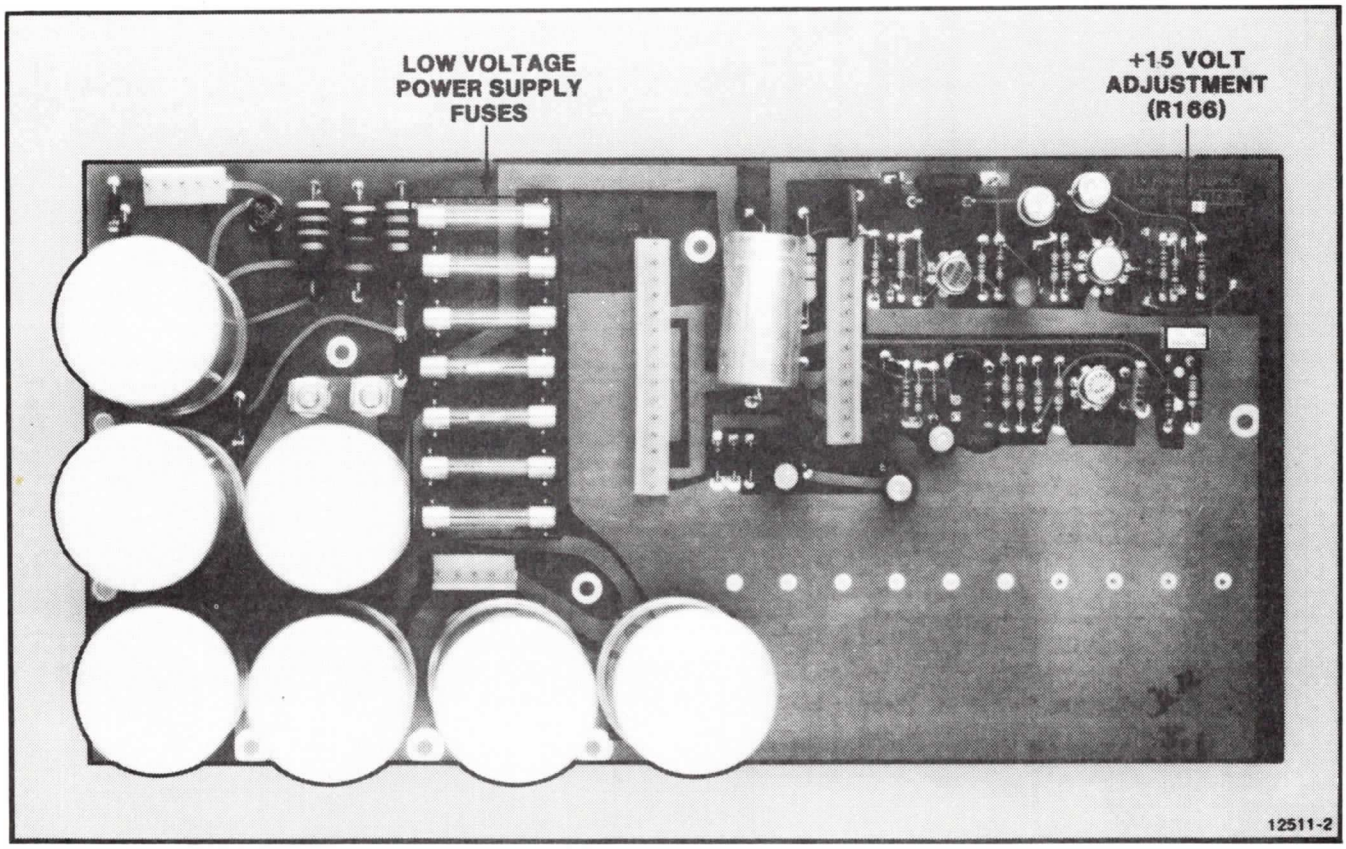


Figure 10-13. Low Voltage Power Supply Board Fuse Locations.

WARNING

Hazardous voltages are present in the terminal circuitry. Always use proper servicing techniques to avoid being injured. Only qualified service technicians should perform the following adjustment procedure.

Display Adjustment Procedure

Low Voltage Power Supply

1. Connect the terminal power cord to the ac voltage source.

2. Turn the terminal POWER switch on.

CAUTION

Observe the crt for the first minute to insure that the beam does not remain in one spot with high intensity for more than a few seconds. This would cause a permanent deterioration of the crt phosphor in that spot. If a bright spot appears, immediately turn off the terminal.

3. Erase the crt by pressing the PAGE key.

4. Connect the DVM probe to the +15 V test point on the Interconnect board. The voltage test points on the Interconnect board are all located in the rear lefthand corner of the board. For a more precise location of these test points refer to the Interconnect board schematic located in Section 5 of Volume 2 of this service manual.

5. Adjust R166 (at the upper right of LVPS board) for a value of +14.97 to +15.03 V.

6. Check the +5 V test point on the Interconnect board for a value of 4.80 to 5.20 V.

7. Check the remaining voltage TPs on the Interconnect board for the following values:

-15V (regulated)	-14.85 V to -15.15 V
+12V (unregulated)	no tolerance (about +9 V)
-12V (unregulated)	no tolerance (about -9 V)
+20V (unregulated)	no tolerance
-20V (unregulated)	no tolerance
+175V (unregulated)	no tolerance
+290V (regulated)	+287.0 V to +293.0 V
+490V (unregulated)	no tolerance

8. Set up the oscilloscope -- .5V/div, 10 us/div, ac coupled -- and check to see that the following ripple voltages are within range. These are measured at the same Interconnect board test points that the dc voltages were measured at.

+15V (regulated)	5mV p-p max
-15V (regulated)	5mV p-p max
+5V (regulated)	10mV p-p max
+12V (unregulated)	1.5V p-p max
-12V (unregulated)	1.5V p-p max
+20V (unregulated)	1.2V p-p max
-20V (unregulated)	1.2V p-p max
+175V (unregulated)	7.0V p-p max
+290V (regulated)	100mV p-p max
+490V (unregulated)	5V p-p max

High Voltage Check

WARNING

The following measurement involves a potentially lethal voltage. USE EXTREME CARE WHEN MAKING THIS MEASUREMENT.

1. Use the 10X high voltage probe of the digital voltmeter to check pin 3 of the crt for a value of -570.0 V to -630.0 V. (The actual voltage is -5700 V to -6300 V).

Storage Board Adjustments

CAUTION

The +X, - X and +Y, -Y signals from the Vector Generator board should be checked if the pedestal was not adjusted before adjusting the display module. If these signals are not adjusted properly, the crt patterns which follow are not positioned on the crt correctly.

All the test points and adjustments on the Storage board are in a line located on the top edge of the Storage board. For the location of these points, see Figure 10-11.

1. Set the DVM to 1 KVdc.
2. Connect the DVM probe to TP 91 -- the flood gun anode.
3. Check for a voltage of 142.5 V to 157.5 V.
4. Connect the DVM probe to TP 94.
5. Adjust R295 (the OP LEVEL adjustment at the top edge of Storage board) so that the crt gets bright, but does not store.

NOTE

Overhead lighting may affect how bright the crt seems to the viewer.

6. Note this voltage as the OP Level voltage.
7. Remove the DVM probe from TP 94 and connect it to TP 93 (CE-2).
8. Adjust R198 (the CE-2 adjustment -- at the top edge of the Storage board) so that the flood gun pattern is within 1/16 inch from the crt target edge, that is, the edge of the phosphor.

9. Note this voltage -- this is the CE-2 voltage. Then remove the DVM probe from TP 93 and attach it to TP 92.

10. Adjust R197 (the CE-1 adjustment -- at the top edge of the Storage board) to obtain a uniform target background illumination. Make sure the corners of the crt screen are at the same level of brightness as the center.

11. Check for oscillation in the background illumination. If background oscillation is present, readjust CE-1. CE-1 is typically set at least 5 V higher than CE-2. Note that there may be some interaction between R196 and R197.

12. Connect the DVM probe to TP 91 -- the flood gun anode.

13. Press the PAGE key and observe that the screen erases.

14. Make sure that the flood gun anode voltage does not change during an erase of the screen.

Storage Board Erase Waveforms

1. Set the oscilloscope to the following settings:

- o V/div: 50V/div
- o Time/division adjustment: 0.1 sec/div
- o Source: channel 1 (using 10X probe)
- o Trigger Mode: "Normal"
- o Trigger level: "+"
- o ac/GND/dc: dc

WARNING

Always disconnect the ac power cord AND wait at least 60 seconds before moving the test jumper on the Storage board or moving ANY jumpers on ANY boards. The capacitors on the LVPS board discharge to a safe level in 60 or MORE seconds. It is a good idea to monitor the +490 or +290 V supplies with the DVM as they are discharging as added safety before touching the boards to remove the jumpers.

2. Disconnect the ac power cord and wait at least 60 seconds before continuing.

3. Remove the test jumper (on the bottom of the Storage board) from the "N" position and place the jumper in the "TEST" position. The TEST jumper may be left in this position while making oscilloscope waveform checks on the Storage board, but must be moved back to the "N" position when making voltage checks with the DVM. If the jumper is not used in the "TEST" position, the crt screen must be erased for each waveform.

4. Connect the ac power cord again and turn on the terminal.

5. Note that the terminal goes into Hold mode and erases every three seconds.

6. Set the oscilloscope trigger mode to "AUTO".

7. Adjust the oscilloscope vertical positioning so that ground reference is lined up with the second graticule line from the bottom of the screen.

8. Set the trigger mode to "NORMAL".

9. Connect the oscilloscope probe to TP 94.

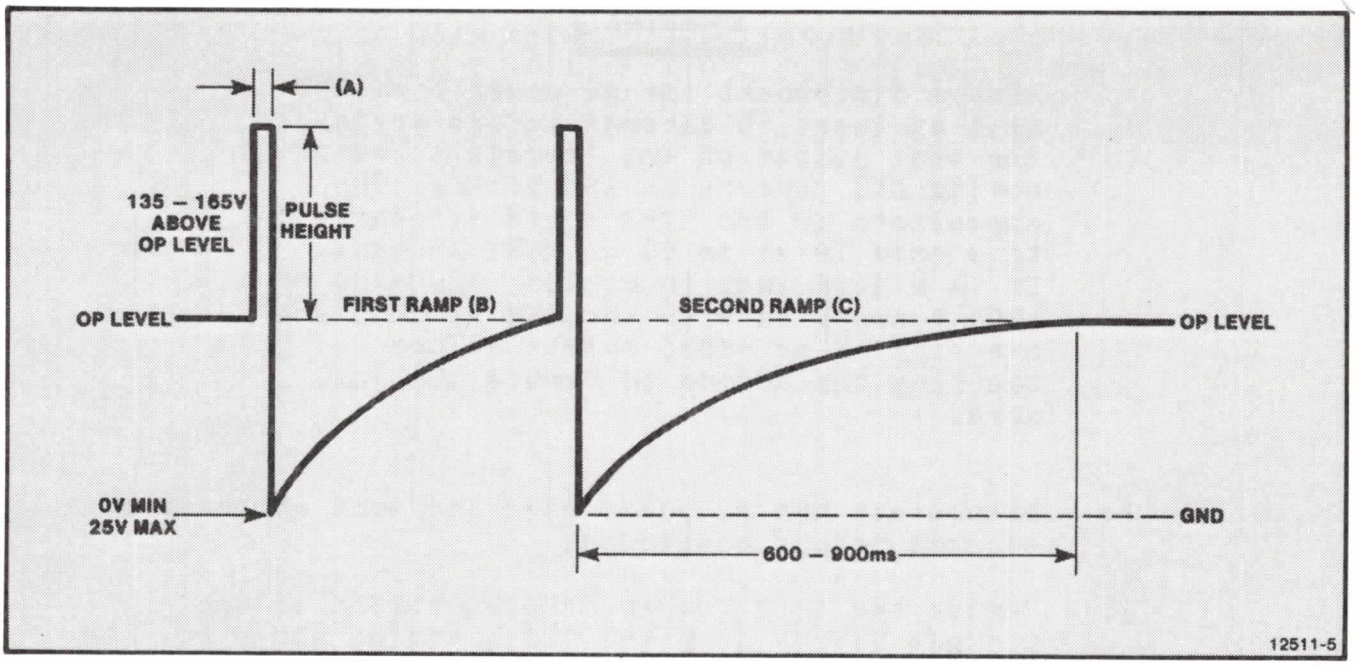


Figure 10-14. Target Erase Waveform.

10. Refer to the target erase waveform (Figure 10-14) and do the following:

    a. Verify that the second positive going ramp (c) is between 600 and 900 ms long.

    b. Verify that the most negative portion of the waveform falls between 0 V and +25 V.

    c. Verify that the pulse height (a) is 135 V to 165 V above the OP level. For example, if the OP level is 150 V, the pulse height must be between 285 V and 315 V.

11. Set the oscilloscope time/division adjustment to 20 ms/div.

12. Observe the first ramp (b).

13. Refer to the second waveform (Figure 10-15) and do the following:

    a. Verify that the time between pulses is 85 ms to 115 ms.

b. Verify that the ramp time is a minimum of 65 ms. Also make sure that the end of the ramp is not less than 80% of the OP level value. For example, if the OP level is 150 V, the end of the first ramp should not fall below 120 V (0.8 x 150 V).

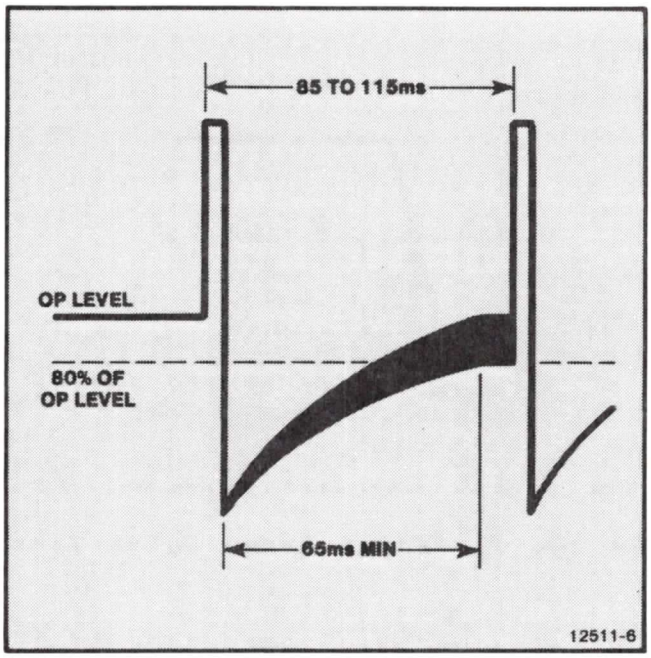


Figure 10-15. Target Erase Waveform Enlarged.

14. Set the oscilloscope time/division adjustment to 0.5 ms/div.

15. Adjust the oscilloscope so that the OP LEVEL trace is at the center of the graticule.

16. Observe the pulse waveform ([a] of Figure 10-14) shown in Figure 10-16.

17. Verify that the pulse waveform has from 1.7 ms to 2.3 ms pulse width, measuring from half way up the rising and falling edges of the pulse. This measurement measures both positive pulses.

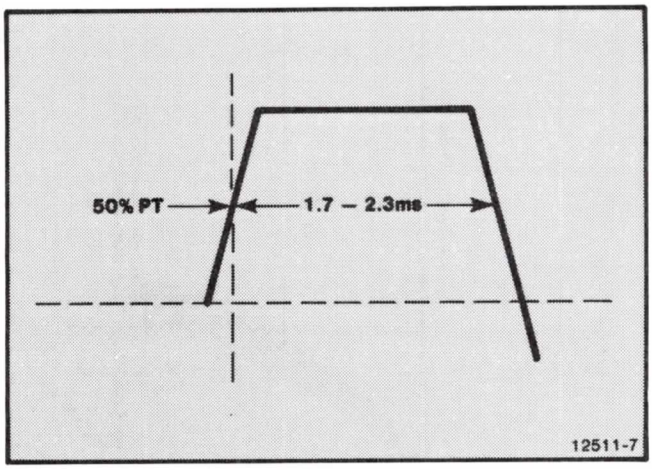


Figure 10-16. Target Erase Pulse Waveform.

18. Connect the oscilloscope probe to TP 93.

19. Set the oscilloscope time/division adjustment to 50 ms/div.

20. Using the waveform in Figure 10-17, do the following:

    a. Verify that the first ramp time is greater than 70 ms. Also, make sure that the end of the ramp is at least 75 % of the CE-2 level. For example, if the CE-2 level is 60 V, the end of the first ramp should not fall below 45 V (60 V x 0.75).

    b. Verify that the second ramp is from 70 to 120 ms long.

    c. Verify that the beginning of both ramps is between 0 V and +15 V.

d. Verify that the time between pulses is from 85 ms to 115 ms.

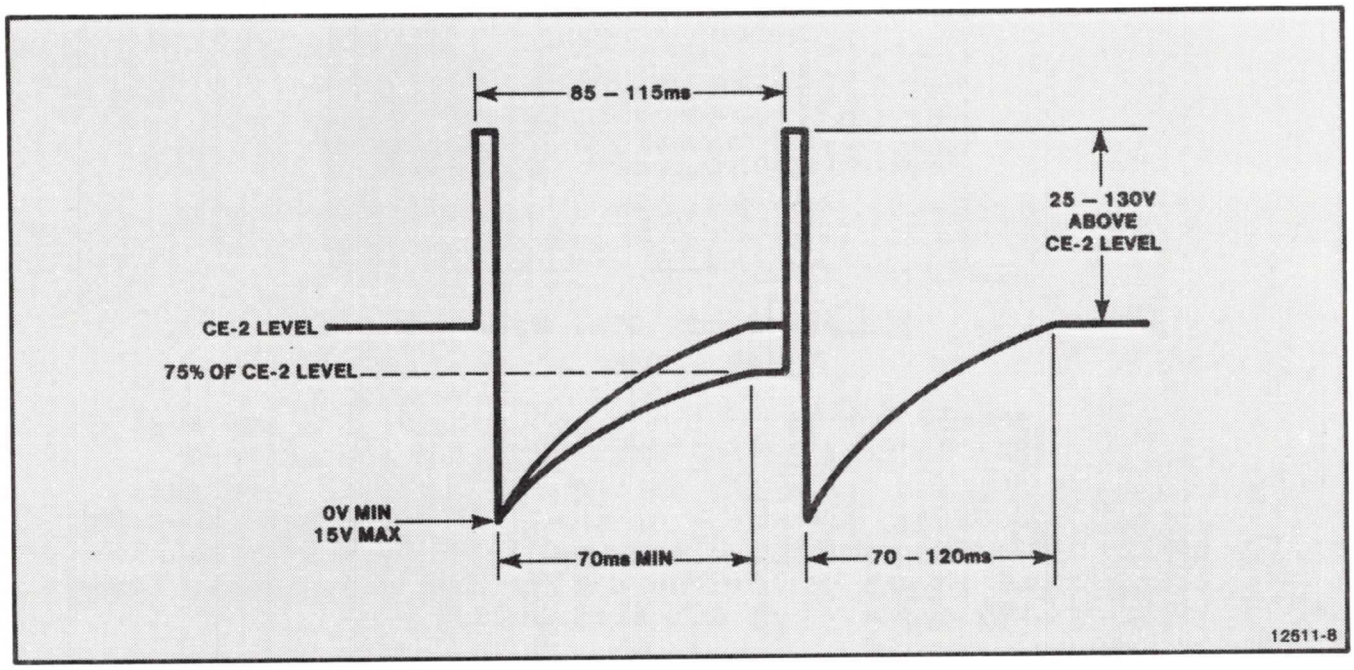


Figure 10-17. CE-2 Waveform.

21. Connect the oscilloscope probe to TP 92.

22. Set the oscilloscope time/division adjustment to 20 ms/div.

23. Observe the waveform in Figure 10-18 and make sure that the time from the beginning of the first pulse to the beginning of the second pulse is from 85 to 115 ms.

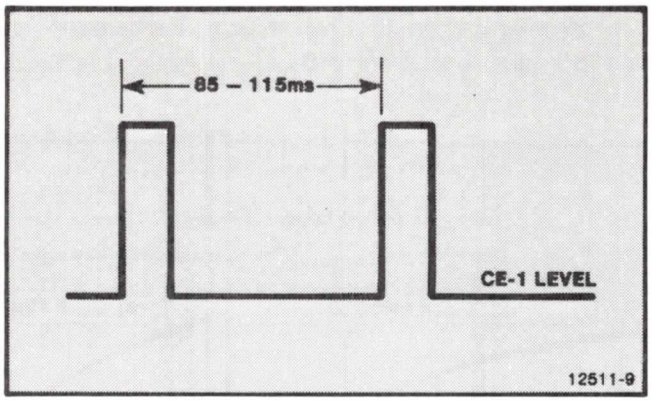


Figure 10-18. CE-1 Waveform.

24. Adjust R95 (CE-1 pulse control, on the top edge of the Storage board) while erasing the crt and observe the edges of the crt for full coverage. Usually, the erase covers the full screen when R95 is turned fully clockwise, or very nearly so. If no change is noticed during this adjustment, leave R95 adjusted at 90% clockwise.

25. Adjust R195 (the CE-2 pulse control, at the top edge of Storage board) while erasing. At the same time, make sure that the erase extends fully to the corners of the screen.

NOTE

The OP LEVEL, CE-1, and CE-2 adjustments interact. Because of this, slight readjustment of the OP LEVEL, CE-1 level, CE-2 level, and CE-2 pulse may be required to make the crt screen look right. Readjust, if necessary, for proper background appearance, full screen target coverage, and full screen erasing.

26. Turn off the terminal, disconnect the ac power cord, and wait 60 seconds before continuing.

WARNING

Always disconnect the ac power cord and wait at least 60 seconds before moving the test jumper on the storage board or moving ANY jumpers on ANY of the boards. The capacitors on the Low Voltage Power Supply board discharge to a safe level in 60 or more seconds. As an added safety measure, it is a good idea to watch the +490 or the +290 V supplies discharge using the DVM while the display is unplugged.

27. Remove the test jumper from the "TEST" position and place it back in the "N" position.

28. Connect the ac power cord again and apply power to the terminal.

Flood Gun Anode

1. Connect the oscilloscope probe to TP 91 on the Storage board.

2. Set the oscilloscope time/division adjustment to 2 ms/div.

3. Press the PAGE key. This restarts the Hold mode timer.

4. Verify that the terminal enters Hold mode from 90 to 135 seconds after pressing the PAGE key.

5. While the terminal is in Hold mode, refer to the waveform in Figure 10-19.

   a. Verify that the positive pulse is 12 to 16% of the period of the waveform. This represents a duty cycle of 12% to 16%. It may be eaisier to see if the time/division setting on the oscilloscope is taken out of the calibrated position and if the positive and negative transitions of the waveform are aligned with the graticule of the oscilloscope. The period of the wave- form, however, must have a real time of 8.3 to 12.5 ms.

b. Verify that the most negative part of the waveform is -15 V.

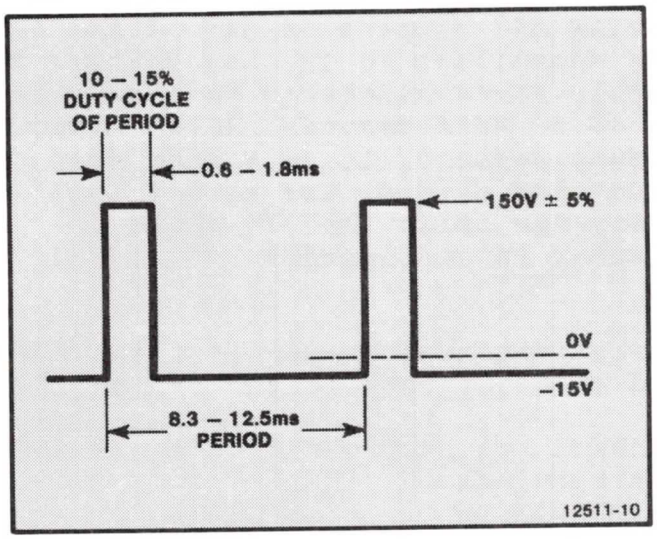


Figure 10-19. Flood Gun Anode Waveform.

6. Connect the DVM probe to Pin 43 (DBUSY) on the Interconnect board.

7. Check for less than 0.8 V (TTL low) during Hold mode.

8. Remove the oscilloscope probe from the Storage board.

Grid Bias

1. Disconnect the AC power cord and wait 60 seconds before continuing.

2. Change the ANTIBURN strap on the Deflection Amplifier board from the "IN" position to the "OUT" position.

3. Connect the AC power cord again and apply power to the terminal.

4. Use the cursor for the following adjustments.

NOTE

For the location of the following High Voltage and Z Axis board adjustments, Figure 10-10 is helpful.

5. Adjust R429 (the CRT Bias adjustment, on the lower right of the HV & Z Axis board) slowly clockwise until a low intensity dot appears in one corner of the cursor. Re- trace lines should appear around the cursor at the same time.

6. Adjust R288 (Center Focus adjustment, on the upper right of the HV & Z Axis board) for a sharp, focussed dot.

7. Adjust R429 until the dot just disappears. Erase the display if the dot stores while making the CRT Bias adjustment.

8. Measure the voltage at the upper end of C429 (lower right side of HV & Z Axis board) with the DVM and adjust R429 counterclockwise until the value increases by +5 V.

9. Disconnect the AC power cord and wait at least 60 seconds before continuing.

10. Change the ANTIBURN strap from the "OUT" position to the "IN" position.

11. Connect the AC power cord again and apply power to the terminal.

Normal Intensity

1. Connect the oscilloscope probe to the top of R246--the 20K resistor near the center of the HV & Z Axis board.

2. Set the oscilloscope volts/division adjustment to 10 V/div and the time/division adjustment to 2 ms/div.

3. Hold down a character key in order to repeat the key.

4. Adjust R427 to between 40 and 50 V measuring from the top of the small pulses to the top of the large pulses. See Figure 10-20. This voltage may later be changed to accomodate dropout or focus.

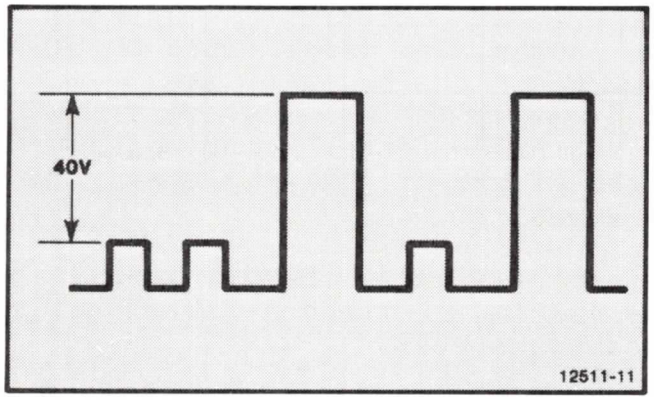


Figure 10-20. Waveform at R246.

Origin Shift

1. Press the PAGE key eight times and watch the cursor move down and to the left seven times. The eighth time it returns to the upper right. Adjusting the REFRESH INTENSITY control may make the cursor easier to see.

Frequency Compensation

The location of the adjustments on the Deflection Amplifier board listed in the following section can be found by referring to Figure 10-12.

1. Display the X COMP pattern by using the Self Test procedure. Adjusting the REFRESH INTENSITY control may make this pattern easier to see.

2. Adjust R51 and R150 on the Deflection Amplifier board so that only one line can be seen. See Figure 10-21.

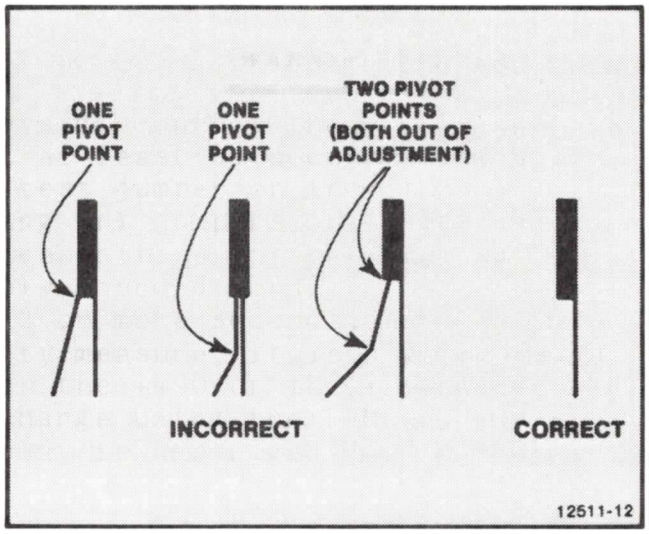


Figure 10-21. X and Y Axis Frequency Compensation Adjustments.

3. Display the Y COMP pattern by using the Self Test procedure.

4. Adjust R69 and R167 on the Deflection Amplifier board so that only one line can be seen. Refer to Figure 10-21.

Gain, Positioning, and Geometry (Including Yoke Adjustment)

NOTE

The following part of the adjustment procedure requires that the Display Controller board has been adjusted. If it has not been previously adjusted before starting the adjustment procedure for the display, and it is far out of adjustment, it may not be possible to check for gain, positioning, and geometry. To adjust this board, see the Display Controller board adjustment procedure.

1. Display the GAIN pattern by using the Self Test procedure. Note that this pattern alternates between storage and Write-Thru (refresh) modes if the SPACE BAR is pressed.

2. Adjust the REFRESH INTENSITY control -- on the bezel -- so that the lines do not store in Refresh mode.

3. Adjust the yoke using a 5/16 inch nut driver. Loosen the yoke adjustment nut and rotate the yoke so that the center vertical line is equidistant from both the left and right edges of the chassis. For example, if the top of the center vertical line is 9.85 inches from the right hand side of the chassis, the bottom of the same center vertical line should also be 9.85 inches from the right edge of the chassis. Conversely, the top and bottom measurements from the left edge of the chassis should be the same. Since the chassis is mechanically square, the vertical line should now be lined up square in relation to the chassis. Use a staight edge to measure the straightness of the line. This line should be as straight as possible.

NOTE

When adjusting the gain and positioning adjustments, the following dimensions should be maintained:

- **top horizontal line should be about 3/4 inch from the edge of the phosphor,**
- **the bottom horizontal line should be about 1/2 inch from the phosphor edge,**
- **the left vertical line should be 3/4 inch from the phosphor edge, and**
- **the right vertical line should be about 1 inch from the phosphor edge.**

4. Adjust R250 (the Long Axis Positioning control, at the bottom right of the Deflection Amplifier board) and R250 (the Long Axis Gain control, at the bottom left of the Deflection Amplifier board) so that the midpoint of the left and right vertical display lines are the same distance from the left and right edges of the crt screen (or crt filter).

5. Adjust R267 (the Short Axis Position control, at the top right of the Deflection Amplifier board) and R67 (the Short Axis Gain control, at the top left of the Deflection Amplifier board) so that the midpoint of the top and bottom horizontal lines are the same distance from the top and bottom of the crt screen (or crt filter).

6. Adjust R326 (the Long Axis Geometry control, at the lower center of the Deflection Amplifier board) for the straightest top horizontal line obtainable.

7. Make sure that the bottom horizontal line is adjusted so that any deviations of the line fall equally above and below a line placed horizontally through the middle. A clear straight edge may be used for this measurement. The deviations above and below this horizontal line must not exceed 3/16 of an inch on either side of the horizontal line. If the bottom display line does exceed 3/16 of an inch on either side of this horizontal line due to excessive deviation, a compromise between the top and bottom horizontal lines must be made, while trying to keep the top line as straight as possible.

8. Adjust R322 (the Short Axis geometry control, at the lower center of the Deflection Amplifier board) for the straightest lefthand vertical line.

9. In measuring the straightness of the righthand vertical line, as in measuring the straightness of the bottom horizontal line, pass a straightedge vertically through the righthand vertical line of the display pattern. Any deviations of the display line should fall equally on both sides of the straight edge and should not exceed 1/8 of an inch on either side of the straight edge. If the display line does fall outside these limits, a compromise can be made between the lefthand and righthand display lines while trying to keep the lefthand line as straight as possible.

NOTE

Adjusting the geometry in one axis affects the gains in the other. Readjustments in gain, therefore, are necessary when making geometry adjustments.

Orthogonality

1. Make sure, when the center vertical display line has been aligned, that the center horizontal display line is within a maximum of +,-1.2 degrees deviation from 90 degrees in relation to the vertical line. The angle between the center vertical line and the center horizontal line must not be more than 91.2 degrees or less than 88.8 degrees.

NOTE

A compromise between the line straightness and orthogonality specification may be made as long as both specifications are made at the same yoke setting.

Dynamic Focus

1. Display the GAIN pattern by using the Self Test procedure.

2. Attach the oscilloscope probe to the upper end of R235 on the HV & Z Axis board in the center.

3. Adjust R424 (the Dynamic Focus control, at the lower center of the Deflection Amplifier board) so that the lowest portion of the waveform changes less than 2 V as R128 (CORNER FOCUS adjustment -- HV & Z Axis board) is adjusted from one extreme to the other. See Figure 10-22.

4. Remove the oscilloscope probe.

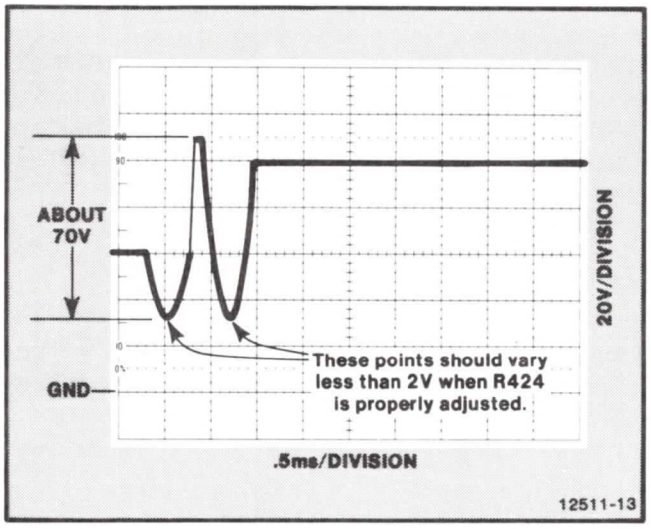


Figure 10-22. Dynamic Focus Waveform.

Slu-0

1. Display the X COMP pattern by using the Self Test procedure.

2. Set the oscilloscope time/division adjustment to 20 us/div and the volts/division adjustment to 2 V/div. Set the slope adjustment to "-".

3. Connect the oscilloscope probe to Pin 36 (SLU-0) on the Interconnect board.

4. Check for a TTL pulse -- a low of less than 0.8 V and a high of greater than 4 V.

5. Remove the oscilloscope probe.

Focus

1. Display the FOCUS pattern by using the Self Test procedure.

2. Adjust R288 (the Center Focus adjustment, at the upper right of the HV & Z Axis board) for the sharpest characters at the center of the crt while characters are being displayed.

3. Adjust R128 (the Corner Focus control, at the lower center of HV & Z Axis board) for a compromise aiming at the sharpest characters at all four corners of the crt. Do this while characters are being displayed.

Dropout

1. Display the HARD COPY pattern by using the Self Test procedure and wait 2 1/2 minutes.

2. Bring the display out of Hold Mode by pressing the SHIFT key.

3. Ideally, the Hard Copy pattern should not have any breaks. However, if breaks occur, increase the OP LEVEL adjustment or the NORMAL INTENSITY adjustment or both in 5 V increments and repeat the Hard Copy pattern until the minimum number of breaks is seen. See Figure 10-23 for an example of dropout.

4. Check the focus again if NORMAL INTENSITY adjustments are made.

5. Check the CE-1, CE-2, display gain, and positioning adjustments if OP LEVEL adjustments are made.

6. Make sure that the final setting of the NORMAL INTENSITY adjustment does not exceed 55 V. If it does and the storage specifications cannot be met by adjusting the OP LEVEL adjustment, collimation voltages, and by reducing the intensity to 55V or less, THE CRT SHOULD BE REPLACED.

Brite Intensity and Defocus

1. Display the DEFOCUS pattern by using the Self Test procedure.

NOTE

This pattern has both focussed and defocussed lines. As the following adjustment is made, the inside set of lines in the pattern should become defocussed. Ideally, a defocussed line is about twice the width of the focussed line.

2. Adjust R415 (the Brite Intensity control, at the lower center of the HV & Z Axis board) to 10 V higher than the NORMAL INTENSITY adjustment. This can be measured at R246 on the High Voltage and Z Axis board, the same place that normal intensity was measured. See Figure 10-24.

3. Adjust R34 (the Defocus adjustment, at the lower left of the High Voltage and Z Axis board) while the characters are being displayed for a noticeable difference in characters.

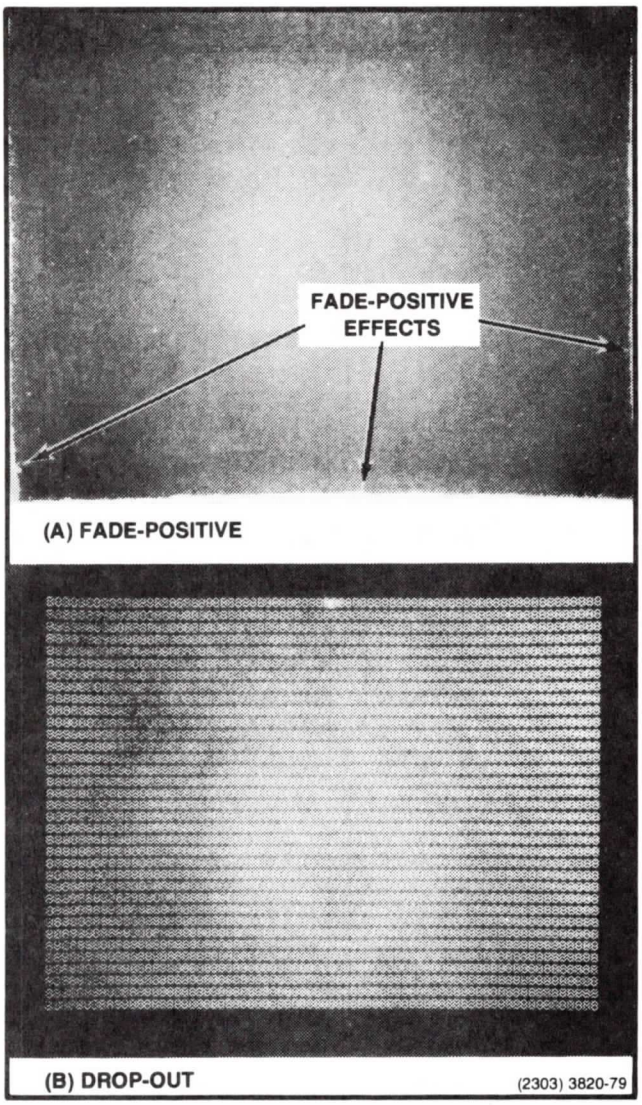


Figure 10-23. Dropout and Fade-Positive Display Effects.

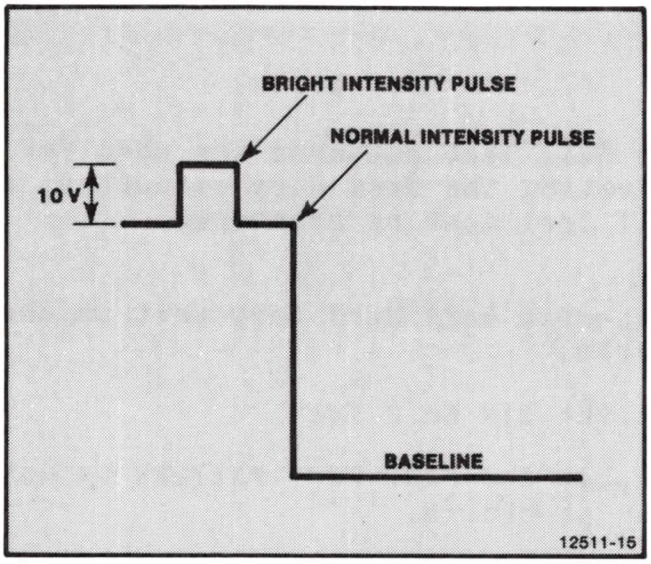


Figure 10-24. Brite Intensity Pulse.

Write-thru Intensity

1. Exit Self Test by pressing the CONTROL and E keys at the same time.

2. Press the LOCAL key. The LED light should remain lit.

3. Press the ESC key and then hold the CONTROL and Z keys down at the same time. This displays a set of crosshairs on the sreen. The position of the crosshairs can be controlled by the thumbwheels on the keyboard.

4. Turn the front panel REFRESH INTENSITY control fully counter- clockwise.

5. Adjust R227 (the Write-thru Intensity adjustment, at the lower right side of the HV & Z Axis board) so that the cross- hairs are not visible. Turn the front panel REFRESH INTENSITY control clockwise. The crosshairs should become visible and should store when the control is turned fully clockwise.

Hard Copy

NOTE

The Self Test patterns are used for adjusting the Hard Copy circuitry, so Self Test must be reentered.

1. Connect a 4631 Hard Copy Unit to the display module.
2. Set the DVM to 2 Vdc.
3. Display the HARD COPY PATTERN by using the Self Test procedure.
4. Press the HARD COPY key on the terminal.
5. Check to see that the crt screen decreases in intensity during the hard copy scan.
6. Check DBUSY (pin 43 on the Interconnect board) for a TTL low of less than 0.8 V during the hard copy scan.
7. Adjust R226 (the Hard Copy Intensity adjustment, at the side of the HV & Z Axis board) for a visible sweep which does not store on the screen during the scan. This is a rough adjustment.
8. Adjust the following potentiometers during a hard copy scan so that the sweep length and position correspond to an area 1/4 inch larger than the pattern being hard-copied -- 1/8 inch larger on each edge.
   a. R229 (the Hard Copy Long Axis position, at the lower center of the Deflection Amplifier board).
   b. R426 (the Hard Copy Short Axis position, at the lower center of the Deflection Amplifier board).

c. R228 (the Hard Copy Short Axis gain, at the lower center of the Deflection Amplifier board).

d. R227 (the Hard Copy LOng Axis gain, at the lower center of the Deflection Amplifier board).

9. Press the HARD COPY key.

10. Adjust R226 (the Hard Copy Intensity adjustment, at the side of the HV & Z Axis board) to its optimum point. Adjust it to be as bright as possible without storing on the screen.

11. Adjust R26 (the Hard Copy Threshold adjustment, center of the Hard Copy Amplifier board) for the highest contrast copies without adding extra "noise" markings.

12. Make three copies and compare them for acceptability.

NOTE

Hard copy acceptability is a visual judgement. Some things to look for are:

A. Characters that look whole with no dropout or excessive bleeding (filling in).

B. Vectors with no more than three breaks of which none can be larger than the width of a line.

C. A minimum of "noise" markings (random dark spots). Some "noise" may be acceptable.

13. If the hard copy is not acceptable, slight readjustment of the OP LEVEL, CE-1, CE-2, Normal Intensity, and Focus adjustments may improve the hard copy.

14. Record the OP LEVEL, CE-1, CE-2 adjustment values and the crt serial number on the crt adjustment tag.

15. Erase the crt using the PAGE key.

16. Turn off the terminal.

17. Replace the cabinet cover and front panel.

This completes the adjustment procedure for the display module.

Section 11

MAINTENANCE

INTRODUCTION

This section is a guide to all routine maintenance of the standard terminal. This includes routine maintenance schedules and maintenance tips, troubleshooting tips and information, all mechanical assembly/disassembly procedures for the standard terminal, and Self Test -- what it is and what it tests.

SELF TEST DIAGNOSTIC PROGRAM

The primary troubleshooting aid for the terminal is the Self Test diagnostic program. This program resides as firmware in the terminal and is designed to test the functioning of all circuitry. For the most part, Self Test does not use circuitry until it has tested it first. But after circuitry has been tested, the Self Test routines may use the tested circuitry.

A subset of Self Test is the Power Up routine. This routine runs automatically when the terminal is turned on, and performs an abbreviated check of the various circuit modules that make up the terminal circuitry. If a malfunction is detected at this point, a malfunction message advises the operator. The 4114 Operator's Manual describes the malfunction messages that may appear during the Power Up routine.

The service technician needs to use, in addition to the Power Up routine, the Self Test routines accessed by pressing the SELF TEST button. Refer to Appendix D, Self Test, for a detailed explanation of how to use Self Test to isolate circuit malfunctions.

ROUTINE MAINTENANCE

There is virtually no need for routine servicing of the terminal except for an occasional cleaning of the display module's face and other outer surfaces. There are no lubrication points, air filters, or vacuum tubes (with the exception of the crt), and the solid-state components provide stable operation.

However, if routine servicing is desired, perform the following maintenance procedures in this section.

Routine maintenance consists of cleaning the terminal, inspecting it, and checking its performance. Routine maintenance should be done every 1000 hours of operation or six months, whichever comes first.

Cleaning

CAUTION

To avoid damage to the plastics used in the terminal, do not use cleaning agents that contain benzene, toluene, xylene, acetone, or similar cleaning agents.

WARNING

To avoid personal injury, ALWAYS DISCONNECT THE AC POWER CORD OF THE TERMINAL FROM THE AC OUTLET AND WAIT AT LEAST 60 SECONDS BEFORE CLEANING THE INSIDE OF THE TERMINAL.

Clean the outside of the instrument using a soft cloth dampened with a mild detergent and water solution.

Remove dust inside the terminal occasionally. Dust conducts electricity under high-humidity conditions and may also damage components by preventing the necessary heat dissipation. The terminal is best cleaned with a vacuum cleaner. Remove any remaining dust with a soft-bristled brush (i.e., a paint brush) or a cloth dampened with a mild detergent and water solution. To clean narrow spaces, use a cotton-tipped applicator.

WARNING

If a dampened cloth is used for cleaning any parts of the terminal that are only accessable with the covers removed, extreme care should be taken not to leave any remaining water or moisture in the instrument when the covers are reinstalled. This situation could provide a potentially lethal shock hazard to the user when power is applied to the instrument.

For cleaning the crt face, the crt filter must be removed. Refer to the discussions of CRT Filter Cleaning and Replacement later in this section.

Cleaning the Keyboard

This procedure describes how to clean off the residue of liquids, such as coffee, soft drinks, and so forth, that have been spilled on the keyboard.

CAUTION

The cleaning procedure uses water, so try to avoid getting water on speakers, paper light shields, and other parts susceptible to water damage.

CAUTION

Do not crush or squeeze the exposed capacitive pads in the switch frame.

NOTE

Drying times may be shortened by forced air drying at a maximum temperature of 60 degrees C (165 degrees F).

1. Refer to the Keyboard Removal procedure in this section in order to separate the keyboard assembly into the printed circuit board and the switch and frame assembly.

2. Wash the frame assembly thoroughly in clean, lukewarm water. Avoid crushing or squeezing the foam pads.

3. Shake the excess water out of the assembly, and set it on blocks to dry in the air for about two to four days. Note that cleaning off the residue left by some liquids may require more than one washing.

4. Wash the circuit board thoroughly in clean, lukewarm water. Use a soft sponge or cloth to dry the board.

5. Set the circuit board on blocks to dry in the air for about one day.

6. Reassembly the keyboard assembly.

Visual Inspection

Inspect the terminal for such defects as broken connections, damaged circuit boards, heat damaged parts, tightness of screws and bolts, and the proper fuses. The crt mounting brackets require special attention. Refer to the Crt Replacement Procedure for appropriate details.

The corrective procedure for most visible defects is repair or replacement; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the unit. It is important to correct the cause of overheating to prevent recurrence of the damage.

Adjustment

If desired, the adjustment procedure described in Section 10 may be done during routine maintenance to verify that the 4114 is operating to its optimum performance. If no circuit boards, electrical, or mechanical parts have been changed, readjustment of the terminal should not be necessary.

TROUBLESHOOTING INFORMATION

The following features of this manual aid the service technician in troubleshooting the terminal.

Controls and Operation

Refer to the following sources for assistance in the operation of the 4114:

- Operating Information section in this manual
- 4114 Computer Display Terminal Operator's Manual
- 4114 Computer Display Terminal Host Programmers Manual
- 4110 Series Command Reference Manual
- 4110 Series Programmers Reference Booklet

Characteristics

Refer to Section 2 for information about user-verifiable specifications of the terminal.

Self Test

This provides a rapid way of checking the standard terminal for proper operation. Self Test primarily uses circuits that have already been tested as it completes the testing of the terminal. In addition, Self Test also has adjustment patterns that are used in display and pedestal adjustment (see Appendix D).

To troubleshoot the basic terminal, remove all option cards, then check the operation by using Self Test. If a failure code shows up on the keyboard, look up the failure code and begin troubleshooting the suggested problem areas. If Self Test works in the basic terminal, install option cards one at a time and repeat Self Test until the terminal fails, then troubleshoot the last installed option card and the circuits with which it interacts.

Self Test is also helpful in troubleshooting the display by using the adjustment patterns to trace a problem.

Block Diagrams and Circuit Diagrams

These diagrams and their descriptions provide an understanding of terminal operation on a circuit, and where necessary, a component level. This information is basic for efficent troubleshooting. Block diagrams are found in Sections 5 through 9, the Theory of Operations sections and in section 12. Circuit diagrams (schematics) are found in volume 2 of this manual.

Component Layout Illustrations

These appear in the Schematic Diagrams section (volume 2) and help in locating the components on the circuit boards.

Recommended Troubleshooting Equipment

A 41XX Logic Extender board (TEKTRONIX part number 670-5291-00) is used as an independent plug-in board to make all system bus signals in the pedestal available to the technician through a series of test points located on the board. The 41XX Logic Extender board is also used as an extender for other circuit boards.

A voltmeter with a dc range of -30 V to +600 V is recommended. If a 10X high voltage probe is not used, a -6000 V range is needed for troubleshooting the high voltage circuits. A 10 MHz bandwidth oscilloscope is also need. These two test instruments are useful in troubleshooting the voltage and logic circuits.

A set of hand tools may be needed for hardware adjustments, removal of cabinet covers, circuit and power modules, and other mechanical assemblies that may have to be removed in the course of terminal repair. A good set of hand tools should include nut drivers, screwdrivers, pliers, adjustment tools, sidecutters and so forth.

PARTS REPLACEMENT

Entire circuit boards, including all soldered-on components, can be replaced. Mechanical assemblies can also be replaced. Part numbers are listed in the Electrical Parts List and the Mechanical Parts List.

All circuit boards in the display module are mounted with machine screws or bolts. To remove the various circuit boards, refer to the major module removal/replacement procedures. The Low Voltage Power Supply Circuit board is located in the Power Supply module, while the Deflection Amplifier, High Voltage and Z Axis, Storage, and Interconnect boards are located in the circuit module. The Hard Copy Amplifier board is located in the crt module.

Most circuit boards in the pedestal can be easily removed by simply pulling out on the circuit board tabs and sliding the circuit boards out of the card cage. Exceptions to this are the pedestal power supply, the keyboard, the Motherboard, and the Motherboard Extender, which are held in by machine screws or bolts.

Connectors

Connectors for multi-pin connections have their jack numbers on the circuit board. On both the connectors and circuit boards, Pin 1 is indicated by a small arrow. When disconnecting cable connectors from circuit board jacks, note the jack numbers and connector color for reassembly. The connectors are color-coded to coincide with the last digit of the appropriate jack number.

This does not refer to any connectors external to the Display Module or Pedestal, such as the pedestal to display signal cable, the pedestal power cord (and display power cord), host computer connections, and the hard copy connecting cord.

Fuses

The display module has fuses on the Low Voltage Power Supply (LVPS) board, the High Voltage and Z Axis board, and on the rear panel. All fuses are readily accessible with the cover removed.

The LVPS board (in the display module) has a total of seven (7) fuses. The output voltage and fuse value is printed under the fuses. Fused power supplies are listed under Low Voltage Power Supply in Section 10.

The pedestal only contains one fuse, the line fuse, located on the rear panel. The fuse size for the operating voltage is indicated on the rear panel.

A table of all the terminal fuses appears in Table 11-1.

WARNING

Before replacing the fuses, disconnect the power cord from the power source and wait one minute for the supplies to discharge to a safe level. Capacitors in the power supply are discharged to a save voltage level after one minute.

Table 11-1

4114 FUSES

Circuit Board	Fuse	Fuse Size
Low Voltage Power Supply (Display Module)	F30 F35 F137 F139 F141 F144 F146	0.15 A fast 0.25 A fast 0.15 A fast 2.00 A fast 2.00 A fast 5.00 A slow 4.00 A slow
High Voltage and Z Axis board (Display Module)	F21	1.00 A fast
Rear Panel of Display Module	F5001	
220 V/240 V 100 V/120 V		2.00 A slow 4.00 A slow
Rear Panel of Pedestal	F3001	
220 V/240 V 100 V/120 V		5.00 A fast 10.00 A fast

Semiconductors

Replacement semiconductors should be of the original type or a direct replacement. If a replacement transistor is made by a different manufacturer, check the manufacturer's basing diagram for correct basing.

WARNING

Adequate safety precautions should be observed when handling silicon grease. Silicon grease can cause severe eye irritation. Wash hands thoroughly after use.

There are many high-power semiconductors located on heat sinks at the back of the terminal. These are insulated from the chassis by mica insulators. The insulators have silicon grease applied to both sides to improve heat dissipation. Apply silicon grease to replacement components before installation.

REMOVAL/REPLACEMENT PROCEDURES -- DISPLAY MODULE

Cabinet

Cabinet Cover Removal

1. Disconnect the ac power cord at the rear of the display module in order to remove the cover.

2. Remove the seven screws on the rear panel of the display module. Four are along the bottom of the rear panel (in a line), two are on the sides of the rear panel -- one on each side, about two inches above the bottom of the cabinet -- and the seventh is next to the J5005 connector. With these seven screws removed, the cabinet is ready to be removed.

3. Remove the cover by sliding it back until it is free of the guiding tracks.

Cabinet Cover Installation

Reverse the above procedure to replace the cover of the display module.

Front Cover Removal

1. Remove the cabinet cover as outlined above.

2. Remove the four screws which hold the front cover in place. These are located on the front of the frame, two on each side. This frees the front cover.

3. Disconnect the Refresh Intensity wires from J35 on the Interconnect board and thread them through the slot in the frame as the front cover is removed.

Front Cover Installation

To install the front cover, reverse the above procedure.

See Figure 11-1 for the locations of the following assemblies.

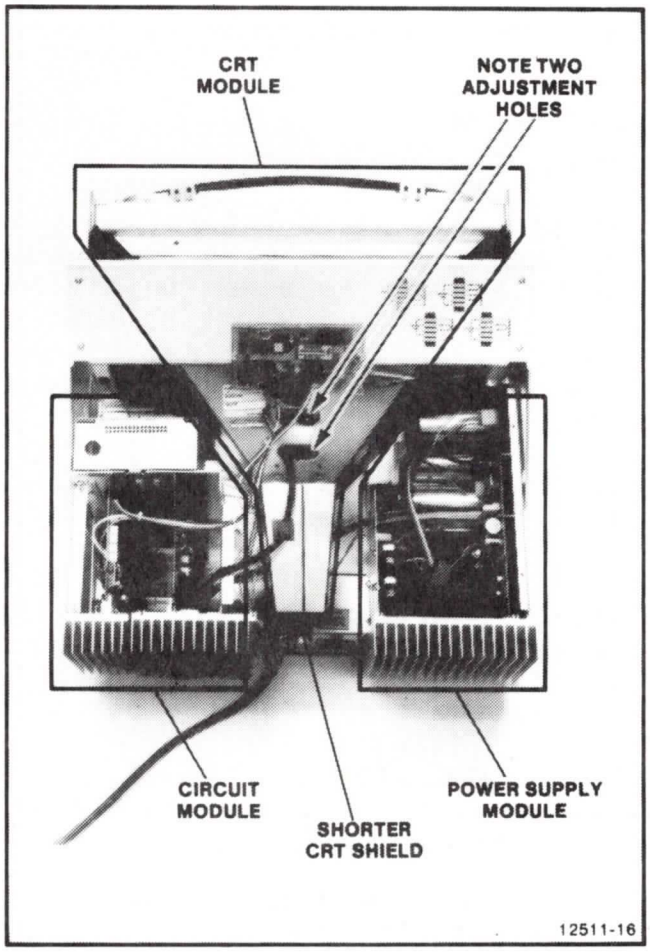


Figure 11-1. Display Module Assemblies.

NOTE

Remove the cabinet cover and front cover from the display module first in order to remove the circuit and power modules, all the circuit boards, and the crt.

Low Voltage Power Supply Module Removal

1. Disconnect the display module from the ac power source.
2. Remove the main power interconnect cable from J32 on the LVPS board and pass it through the hole in the left side of the power supply module.
3. Remove the + and - wires from the solid state relay and pass them through the same hole on the left side of the Power Supply module.
4. Remove the two screws from the top right edge of the module, which connect the module to the chassis.
5. Remove the screw on the bottom of the module next to the main power cord socket.
6. Remove the two screws on the bottom front of the module.
7. Completely loosen, but do not remove, the four main transformer mounting bolts.
8. The Power Supply module is now free of connections to the chassis. To remove it, lift the Module up slightly and then pull it back free from the chassis.

Low Voltage Power Supply Module Installation

To install the LVPS module, reverse the removal procedure.

Low Voltage Power Supply Board Removal

It is not necessary to remove the LVPS module to remove the board. Carefully note where all the connectors connect to the board before removing the board. A detailed procedure follows.

1. Remove the circuit board interconnect cables from J1, J32, J43, J134, and the two power transformer leads which are connected to two clips marked C111 (next to the LVPS fuses).

2. Remove the screw from the bottom edge of the filter capacitor holding bracket. This is screwed into the LVPS module. This bracket can then be removed by sliding the bracket out and away from the filter capacitors.

3. Remove the two mounting screws holding the circuit board to the module. These are located next to J32 and the C111 connectors.

4. The board is now free. Remove it by sliding the board upward and free of the Power Supply module.

Low Voltage Power Supply Board Installation

Reverse the above procedure.

CAUTION

It is possible to reverse the P32 and P43 connectors when installing the LVPS board. If this is done, the display module may be seriously damaged.

Circuit Module

Circuit Module Removal

1. Disconnect the display module from the ac power source.
2. Remove the connector from J35 on the Interconnect board.
3. Remove the connectors from J130, J131, and J132 from the Hard Copy Amplifier board.
4. Remove the yoke wires, which are connected to J56 and J66 on the Deflection Amplifier board.
5. Remove the crt plug from the rear of the crt.
6. Remove the main power interconnect cable from the Interconnect board (J80).
7. Remove the + and - solid state relay wires from the + and - terminals of the solid state relay on the Power Supply module.
8. Remove the screw on the left side of the circuit module, next to the CENTER FOCUS adjustment.
9. Screws holding the circuit module to the chassis that need to be removed. They are located:
   a. On the bottom back right of the module.
   b. On the bottom left front corner of the module.

c. On the bottom back left of the module. This screw also acts as a ground lug for the wire coming from J35 of the Interconnect board.

d. On the bottom right center of the module. This screw also goes through the circuit board guide support.

10. The circuit module is now ready to remove. Remove the module by lifting slightly upward while sliding the module back and away from the chassis.

Circuit Module Installation

Reverse the removal procedure to install the circuit module assembly.

Storage Board Assembly Removal

1. Remove the retaining bracket. This is held on by two screws and a nut.

2. Remove the two screws from between the cooling fins of the left-hand section of the heat sink.

3. Disconnect the cables from J3 and J4 -- if not done previously.

4. Pull up firmly on the Storage board assembly and remove it from the circuit module.

Storage Board Assembly Installation

Reverse the removal procedure to install the board, being careful to align the circuit board guides and interconnecting pins correctly.

Deflection Amplifier Board Assembly Removal

1. Remove the four screws from between the cooling fins of the right-hand section of the heat sink.
2. Remove the cables from J56 and J66 -- if not already disconnected.
3. Pull up firmly on the Deflection Amplifier board assembly and remove it from the circuit module.

Deflection Amplifier Board Assembly Installation

Reverse the removal procedure to install the assembly. Be careful to align the circuit board guides and interconnecting pins correctly.

High Voltage and Z Axis Assembly Removal

1. Loosen the retaining screw from the center top of the assembly.
2. Disconnect the crt socket connector from the crt-- if not done in a previous step.
3. Pull up and remove the assembly from the Circuit module.

Interconnect Board Removal

1. Remove the Circuit module. See Circuit Module Removal earlier in this section.
2. Remove all the circuit assemblies attached to the Interconnect board -- if not already removed.
3. Remove the four screws securing the circuit board guide support. Two are on the outside of the bracket, below the adjustment holes, and two are on the opposite side of the guide bracket.

4. Turn over the circuit module base.

5. Remove the remaining circuit module base screws.

6. Remove the Interconnect board assembly.

NOTE

Refer to Appendix A for a definition of signals on the pins of the Interconnect board and the schematics diagram section in volume 2 of this manual for a diagram of the board itself.

Interconnect Board Installation

Reverse the removal procedure to replace the Interconnect board.

Crt Module

Crt Filter Cleaning

To clean the crt face and the back of the crt filter, remove the entire crt filter assembly. Refer to Figure 11-2 for the locations of the crt filter assembly parts.

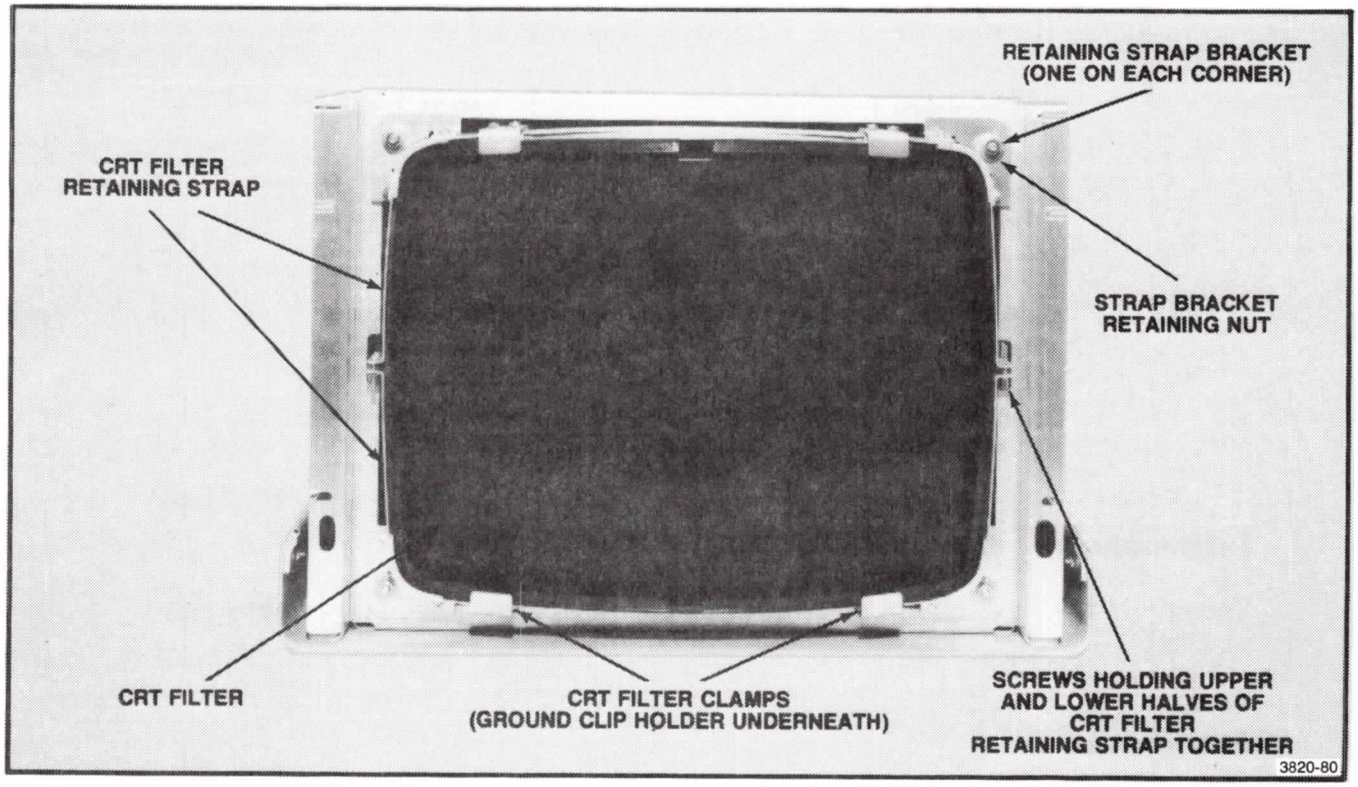


Figure 11-2. Crt Filter Bracket and Hardware.

1. Disconnect the display module from the ac power source.

WARNING

The four nuts which secure the retaining strap bracket are the only means of crt support. With these 7/16-inch nuts removed, the crt could slip out of the chassis. Implosion of the crt could possibly injure the service technician.

2. Remove the nuts on the four corners of the retaining strap bracket with a 7/16-inch wrench.

3. Remove the lock and flat washers from the same bolts.

WARNING

The filter assembly is not rigid and requires a certain amount of support. Avoid scratching or striking the crt with the filter removed because of the possibility of implosion. Implosion of the crt could injure the service technician.

4. Loosen the four posi-drive head bolts which hold together the crt filter retaining strap.

5. Pull the filter assembly firmly forward from the crt.

6. Clean the crt face and the filter's rear side with a soft cloth and a solution of mild detergent and water.

7. Dry with a soft cloth.

8. Reverse steps 1 through 5 to replace the crt filter assembly.

9. Clean the front side of the filter.

Crt Filter Replacement

Replacement requires removing the crt filter from the frame assembly.

1. Disconnect the display module from the power source.

2. Loosen with a 5/16-inch wrench the nuts holding the four crt filter clamps. Refer to Figure 11-2 to locate the crt filter parts.

3. Remove the two upper crt filter clamps -- leave the ground clip holders mounted on the filter retaining strap assembly.

4. Ease the top of the filter away from the crt. Grasp the filter firmly and lift it up and out of the lower crt filter clamps.

5. Clean the face of the crt and the underside of the new crt filter with a soft cloth and a solution of mild detergent and water. Dry both with a soft cloth.

6. Handle the filter only on the edges during installation. Replace the crt filter by carefully sliding the filter bottom down between the ground clips and the crt filter clamps.

7. Make sure that the bottom ground clips are flush against the lower rear edge of the crt filter and have not been dislodged.

8. Press the top of the crt filter back against the upper ground clips.

9. Attach the crt filter clamps to the filter retaining strap.

10. Make sure that the crt filter is centered in the retaining strap.

11. Press the crt filter clamps firmly against the filter so that they are flush with the filter. Using a 5/16 inch wrench, tighten the nuts.

12. Clean the new crt filter face and dry with a soft cloth.

Crt Replacement Procedure

WARNING

The crt may implode if it is struck or scratched. Avoid handling the crt by the neck. Wear protective clothing and a face shield when handling the crt.

Replacing the crt safely requires removing the crt module and the crt shield, with the crt filter attached. The display module should be placed on a stable work area or desk top, with adequate space that allows the crt to be removed with no danger of the crt falling from the work area to the floor.

1. Disconnect the display module from the ac power source.
2. Prepare a secure place with a soft cushion or foam pad to accept the crt module after removal.
3. Disconnect the crt plug from the rear of the crt and remove the plug wires from its retaining clamp.
4. Disconnect the yoke wire connectors from J56 and J66 on the Deflection Amplifier board and remove them from the retaining clamp.
5. Disconnect the connector plugs to J133 and J134 on the Hard Copy Amplifier board.
6. Carefully turn the display module so that it is resting on its side and remove the three screws on the bottom front of the cabinet which hold the crt shield. These three screws are in a line.
7. Turn the display module back on its base and remove the four remaining screws (two on each side) which hold the crt shield in place. Refer to Figure 11-3 for the locations of these screws.

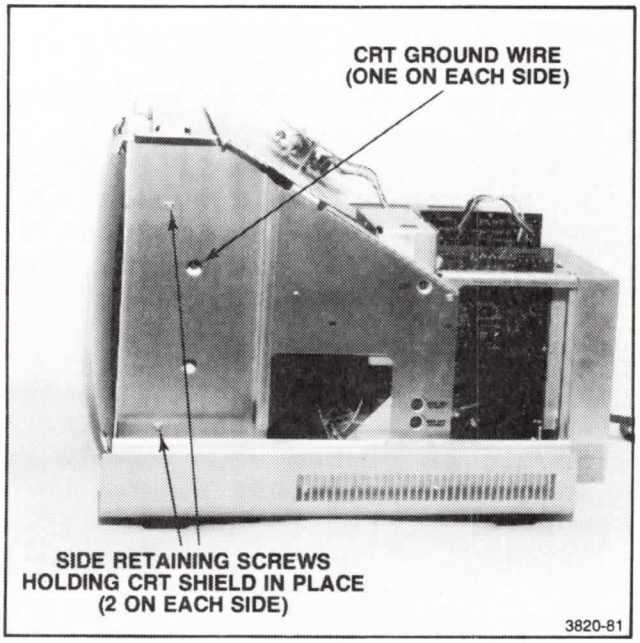


Figure 11-3. Side-View of the Display Module.

WARNING

The crt and shield are now physically disconnected from the chassis, and it is possible for the crt assembly to slip out of the chassis. Handle the crt with care because it may implode if it is scratched, struck, or dropped.

8. The crt and shield can now be removed by gently pulling forward on the crt shield assembly.

9. Lift the crt module away from the chassis and place it on the soft cushion or foam pad prepared in step 2. See Figure 11-4.

10. Loosen and remove the two ground straps -- one on each side of the crt.

11. Remove the crt filter by removing the four 7/16 inch nuts and accompaning washers and loosening the bolts which hold the two halves of the crt filter retaining strap together. The filter assembly comes off by pulling forward.

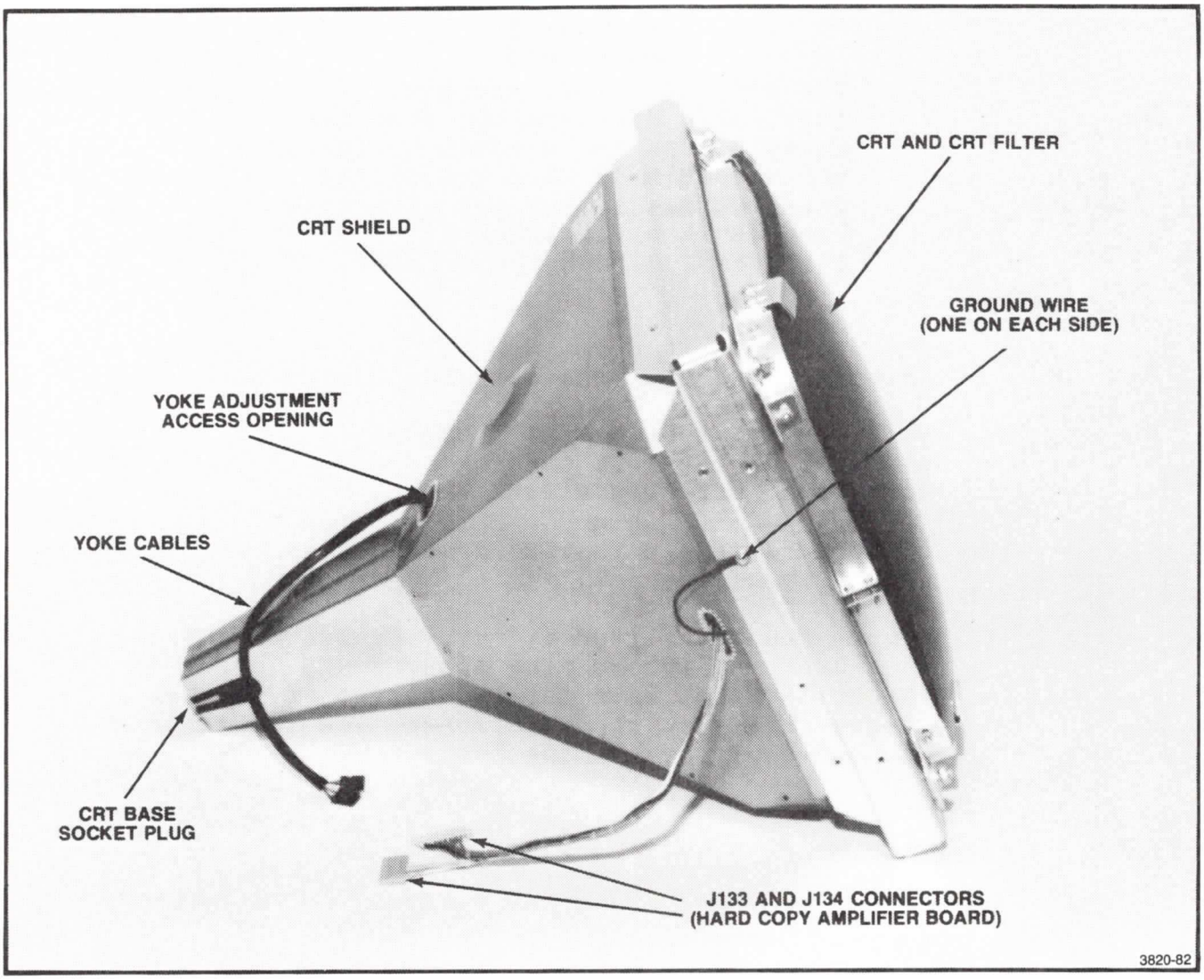


Figure 11-4. Crt Module.

WARNING

In the following step, use care to prevent the crt module from falling forward out of the shield. The crt may implode and injure the service technician.

12. While holding the crt in place, tilt the crt shield assembly forward by placing one hand on the top of the crt and shield. While doing this, hold the crt in place to keep it from slipping out of the shield. With the other hand, hold the neck of the shield so that the crt is resting face down on the foam pad. (See Figure 11-5.)

13. Lift the crt shield straight up and off the crt, being careful to avoid the yoke adjustment nut. (See Figures 11-4 and 11-6.) Thread the socket wires and the cables through their respective holes.

WARNING

The crt band is for implosion protection and must not be removed. The crt may implode and cause serious injury if it is scratched or struck severely. Avoid undue force when handling the crt near its neck.

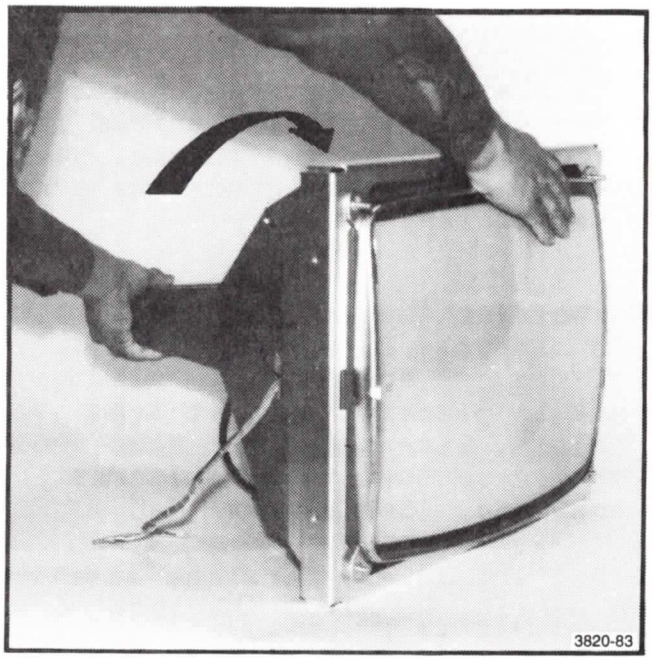


Figure 11-5. Tilting the Crt Module Forward.

14. Remove the yoke assembly by loosening the the top screw -- inside cover -- and slightly speading the clamp while lifting the yoke off the crt. (See Figure 11-6.)

15. Place the old crt in a shipping carton immediately.

16. Place the new crt in the same secure padded area and have the crt connections on your left, with the crt cables attached to the crt placed to the left.

17. Place the yoke on the crt neck with the yoke cable in the rear, the adjustment nut in the front, and the clamp screw on the right. (See Figure 11-6.)

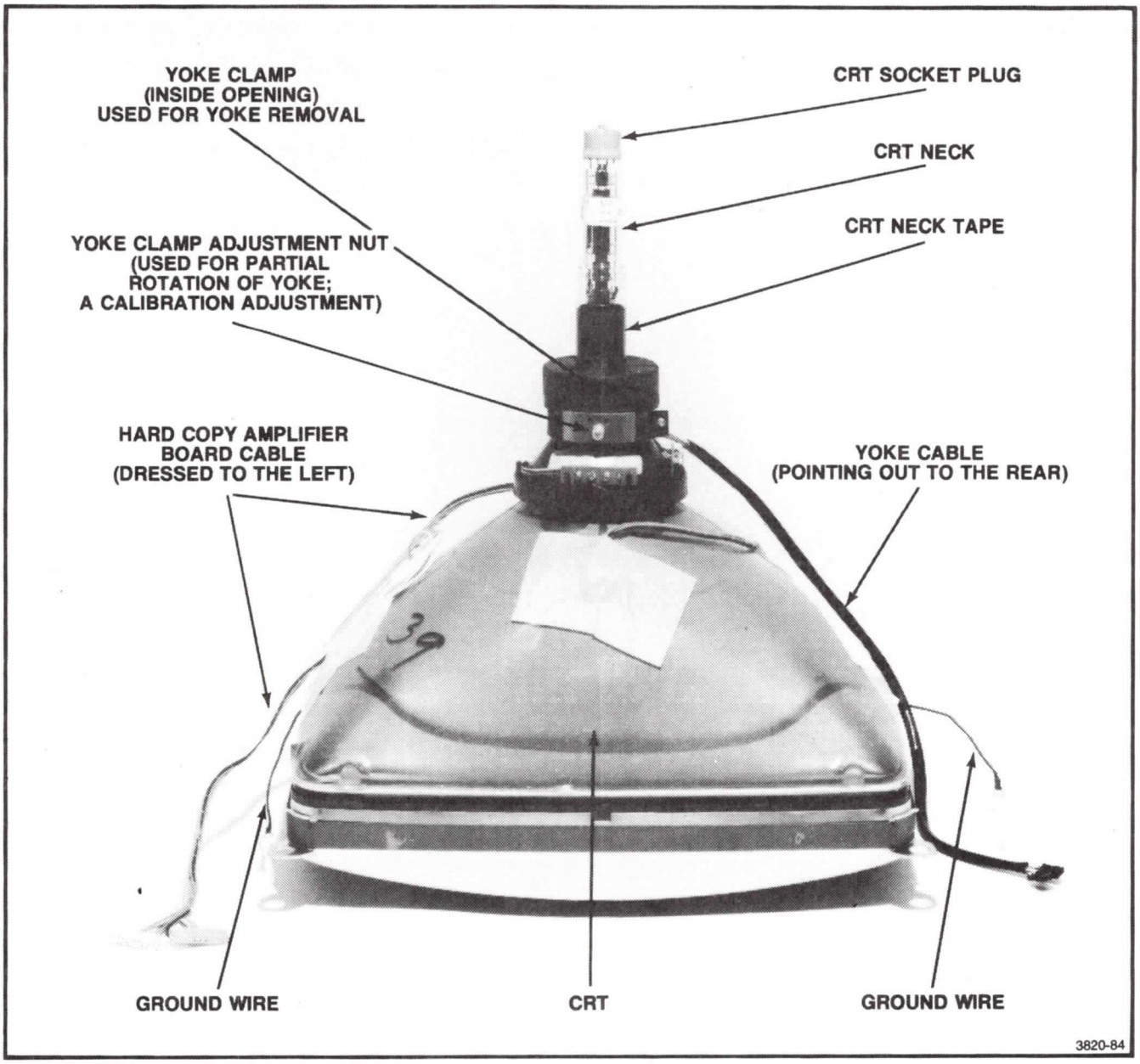


Figure 11-6. Crt and Yoke Assembly.

18. Make sure that the crt neck tape is visible above the yoke assembly and that the assembly is flush against the crt.

19. Tighten the top clamp screw on the yoke assembly. (See Figure 11-6.)

20. Route the yoke cable connectors toward the front of the crt.

21. Orient the crt shield with the yoke adjustment access opening facing the user.

22. Grasp the crt shield firmly, and gently slide it down over the crt, while passing the cables and ground connectors back through the proper shield openings.

23. Holding the new crt and shield firmly, tilt it back on the foam pad so that the assembly is resting on the front and on the neck of the shield.

24. Reconnect the ground straps.

25. Clean the face of the new crt and the underside of the crt filter with a solution of mild detergent and water. Dry with a soft cloth.

26. Replace the filter. Center the bolts through the holes of the retaining strap brackets to insure maximum alignment of the crt -- the crt is not tilted in the shield.

27. Tighten the 7/16-inch nuts and the retaining strap bolts.

28. Put the crt module back into the frame. The yoke adjustment slot should be facing up.

29. Replace the seven screws that hold the crt shield in place, two on each side and three on the bottom of the cabinet.

30. Reconnect the wiring to the Hard Copy Amplifier board, the crt plug, and the yoke wires to the Deflection Amplifier board.

31. Make sure that the J311 and J314 connectors are in the proper position. See Selecting X- and Y-Axis Inputs in this section.

Reconfiguring the CRT Module

Reconfiguring the crt consists of rotating it 180 degrees. There are two ways to do this; the first method is recommended.

In the first method, the yoke is loosened and ends up in a position rotated 180 degrees with respect to the crt, but in the original position with respect to the chassis. Readjustment of the yoke is required. (See "Display Adjustment Procedure" in Section 10.) This method allows for yoke adjustments in the future, since the yoke adjusting nut is left facing up and is easily accessible.

The second method rotates the crt with the yoke attached. Rotating the crt this way eliminates the need to readjust the yoke after rotation, but the major drawback is that the yoke cannot be readjusted because the yoke adjusting nut faces down and cannot be reached. This method requires two electrical changes to the J311 and J314 jumpers on the Deflection Amplifier board. These changes alter the X and Y deflection inputs.

Method 1 (Rotating the Yoke on the CRT)

WARNING

Repositioning the crt in this manner requires that the crt be removed from the chassis. If the crt is scratched or dropped, it may implode, possibly resulting in serious injury. Handle the crt with care to avoid this.

To rotate the crt 180 degrees, while also rotating the yoke allowing for further yoke adjustments, use the following procedure:

1. Remove the cabinet and front cover and disconnect the ac power cord to the display module.

2. Remove the crt from the chassis and then remove the crt shield from the crt using the crt replacement procedure in this section. Perform steps 1-13 in the crt replacement procedure.

3. Loosen the yoke assembly by loosening the top screw (inside cover). Rotate the yoke 180 degrees and tighten the top screw (inside cover). Refer to Figure 11-6 for the location of this screw.

4. Make sure that the crt neck tape is visible above the yoke assembly and that the assembly is flush against the crt.

5. Replace the crt shield after rotating it 180 degrees from its original position with respect to the chassis. If done correctly, the yoke access opening faces up when the crt and shield assembly is reinstalled in the chassis. Be sure to pass the crt cables through the proper openings when setting the shield down over the crt and yoke.

6. Hold the crt and shield firmly and tilt the assembly back on the foam pad so that it is resting on the bottom of the front and neck of the shield.

7. Reconnect the ground straps.

8. Clean the face of the crt and the inside of the crt filter with a solution of mild detergent and water. Dry it with a soft cloth.

9. Install the filter. Center the bolts through the holes of the retaining strap brackets to insure maximum alignment of the crt. The crt is not tilted in the shield.

10. Place the crt module back into the frame. The yoke adjustment nut and corresponding slot should be facing up.

11. Replace the three bottom screws and the four side screws which were removed in steps 6 and 7 in the crt replacement procedure.

12. Connect the plugs to J133 and J134 on the Hard Copy Amplifier board. The wires that connect to J133 and J134 may not be long enough since they come out of the crt shield on the opposite side now. If this happens, rotate the Hard Copy Amplifier board 180 degrees, so that the wires connected to J133 and J134 can reach.

13. Connect the yoke wire connectors to J56 and J66 and insert the wires into the retaining clamp.

14. Connect the crt plug to the rear of the crt. It is now turned 180 degrees from its original position. Insert the wires into the retaining clamp.

15. Since the crt has been rotated in the yoke, the yoke must be readjusted. See "Display Adjustment Procedure" in Section 10.

16. After readjusting the yoke, install the cabinet cover and front cover.

Method 2 (No Rotation of the Yoke)

NOTE

Rotation of the crt using this method does not allow for further yoke adjustments since the yoke adjustment nut faces down and is not easily accesible.

WARNING

Repositioning of the crt requires that the crt be removed from the chassis. If the crt is scratched or dropped, it may implode, possibly resulting in serious injury. Handle the crt with care to avoid this.

To rotate the crt 180 degrees without loosening the yoke, use the following procedure:

1. Disconnect the display module from the ac power source.
2. Remove the cabinet and front cover Refer to the cabinet and front cover removal procedures in this section.
3. Disconnect the crt plug from the rear of the crt and remove the plug wires from their retaining clamp.
4. Disconnect the yoke wire connectors from J56 and J66 on the Deflection Amplifier board and remove them from the retaining clamp.
5. Diconnect the connector plugs to J133 and J134 on the Hard Copy Amplifier board.
6. Remove the crt ground straps from the crt shield through the holes provided in the chassis.

7. Gently pull forward on the crt and filter. Thread the socket wires and cables through their respective holes. When the crt and yoke are clear of the chassis, rotate the assembly 180 degrees and place the assembly back into the chassis and shield. Thread the wires and cables back through the holes. Note that the ground straps must go through the opposite holes that they were removed from.

8. Connect the two ground straps.

9. Center the bolts through the holes of the retaining strap brackets to insure maximum alignment of the crt, the crt is not tilted in the shield. Put washers and nuts back on all the bolts. Tighten the four nuts.

10. Connect the wiring to the Hard Copy Amplifier board, the crt plug, and the yoke wires to the Deflection Amplifier board If the wires that connect to J133 and J134 on the Hard Copy Amplifier board do not reach to their connections, turn the Hard Copy Amplifier board 180 degrees. The wires should now reach.

11. The connectors on J311 and J314 (Deflection Amplifier board) must now be changed to compensate for the yoke rotation of the crt See Selecting X and Y Axis inputs, and Figures 11-7 and 11-8.

12. Replace the cabinet cover and front cover.

Selecting X and Y Axis Inputs

The deflection inputs can be wired to provide compatibility with the crt configuration. Two 2-pin connectors (J311 and J314) on the Deflection Amplifier board are used. See Figures 11-7 and 11-8 for illustrations of the connector/crt orientation. Corner A represents the starting point for alphanumeric writing in standard (or factory preset) horizontal format. Note the placement of corner A in the two illustrations, and its relation to the settings of J311 and J314. Use the arrows on both the circuit board and the connectors for reference to make the deflection input connector changes.

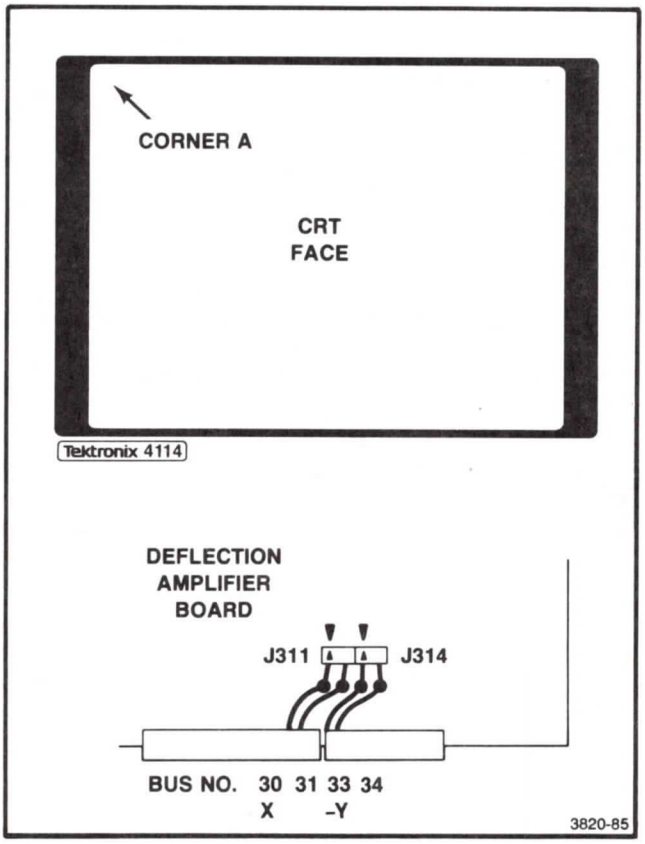


Figure 11-7. Standard Horizontal Format.

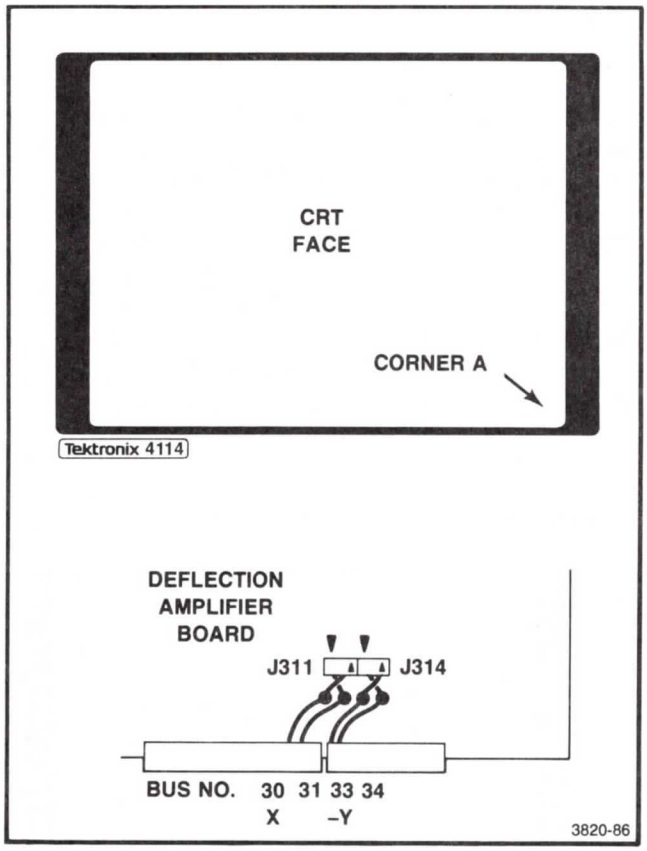


Figure 11-8. 180 Degree Rotation Horizontal Format.

REMOVAL/REPLACEMENT PROCEDURES--PEDESTAL

NOTE

The following removal/replacement procedures are for a standard terminal pedestal with no options installed. If the terminal has any options installed, see the option manual(s) for (possibly) different removal/replacement procedures.

Cabinet

Front Cover Removal

Access to the card cage and circuit boards is gained by removing the front cover.

The front cover (underneath the keyboard) is held on by six screws, three on each side. After removing these screws, the front cover is free of the chassis and can be removed. (See Figure 11-9.)

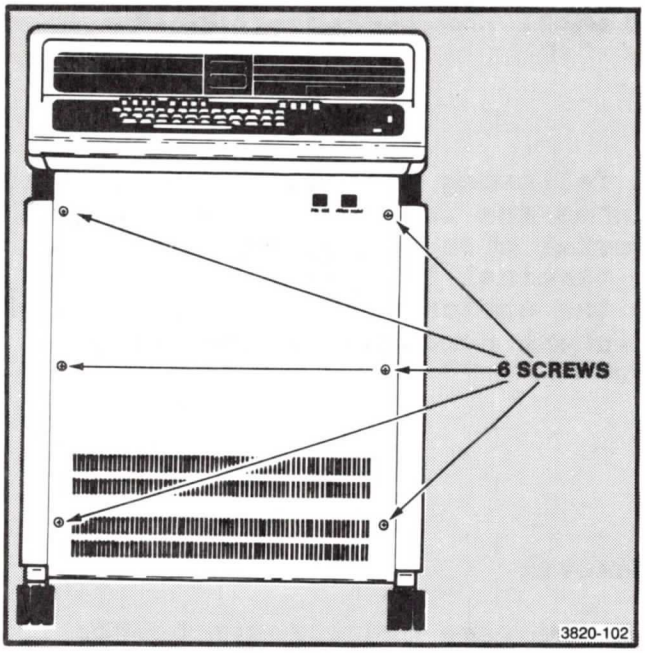


Figure 11-9. Removing the Front Cover.

Rear Panel Removal

The rear panel is removed by unscrewing eleven screws holding it to the chassis. Removing this panel exposes the edge connectors and their wiring at the rear of the card cage. (See Figure 11-10.)

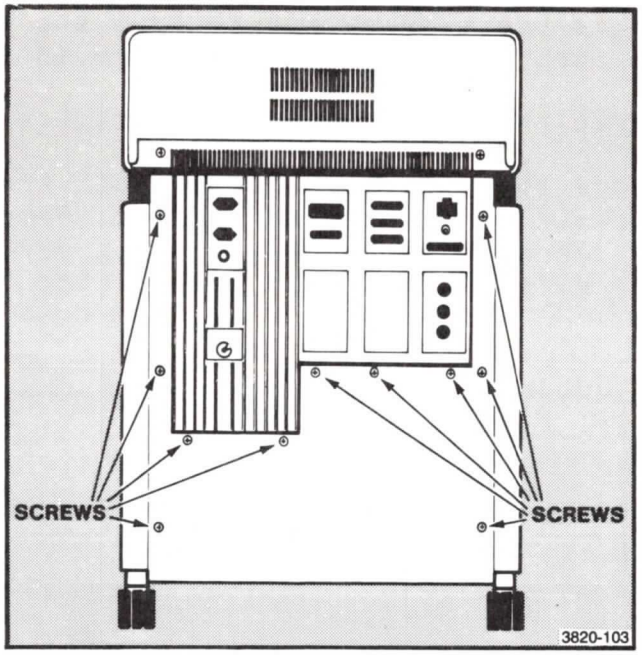


Figure 11-10. Removing the Rear Panel.

Side Cover Removal

The side covers are removed by gently pulling outward at the bottom of the panel. Once the bottom is free, the top of the panel is gently pulled free. Three "cover retainers" -- snap-in fasteners -- hold each panel. No screws hold the panels on to the pedestal chassis.

Cabinet Top Removal

The cabinet top provides the only access to removal/repair of the main power switch on the standard terminal.

1. Remove the display power cord (at J3002) and the plug at J3000 from the rear of the pedestal. This frees the display from any connections with the pedestal.

2. Remove the display module from the top of pedestal. Set it on a stable surface in a safe place.

3. Remove the front cover. (See Figure 11-9.)

4. Remove the two covers underneath the keyboard. One is fastened by thirteen screws. Remove this cover. The second cover is held by six screws -- three on each side. Remove this cover. (See Figure 11-11.)

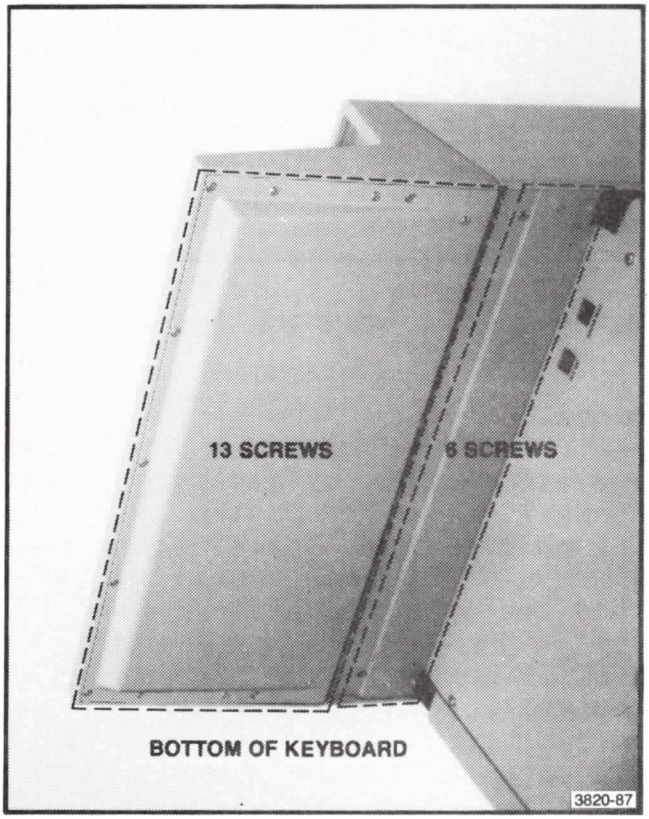


Figure 11-11. Two Covers Below Keyboard.

5. Remove the seven screws that hold the cabinet top on. Four are located in the four corners of the cabinet top -- recessed about 1.5 inches in from the bottom of the cabinet top. The last three screws are located in a line on the rear of the trim grill, pointing upward and screwed into the cabinet top. (See Figure 11-12.)

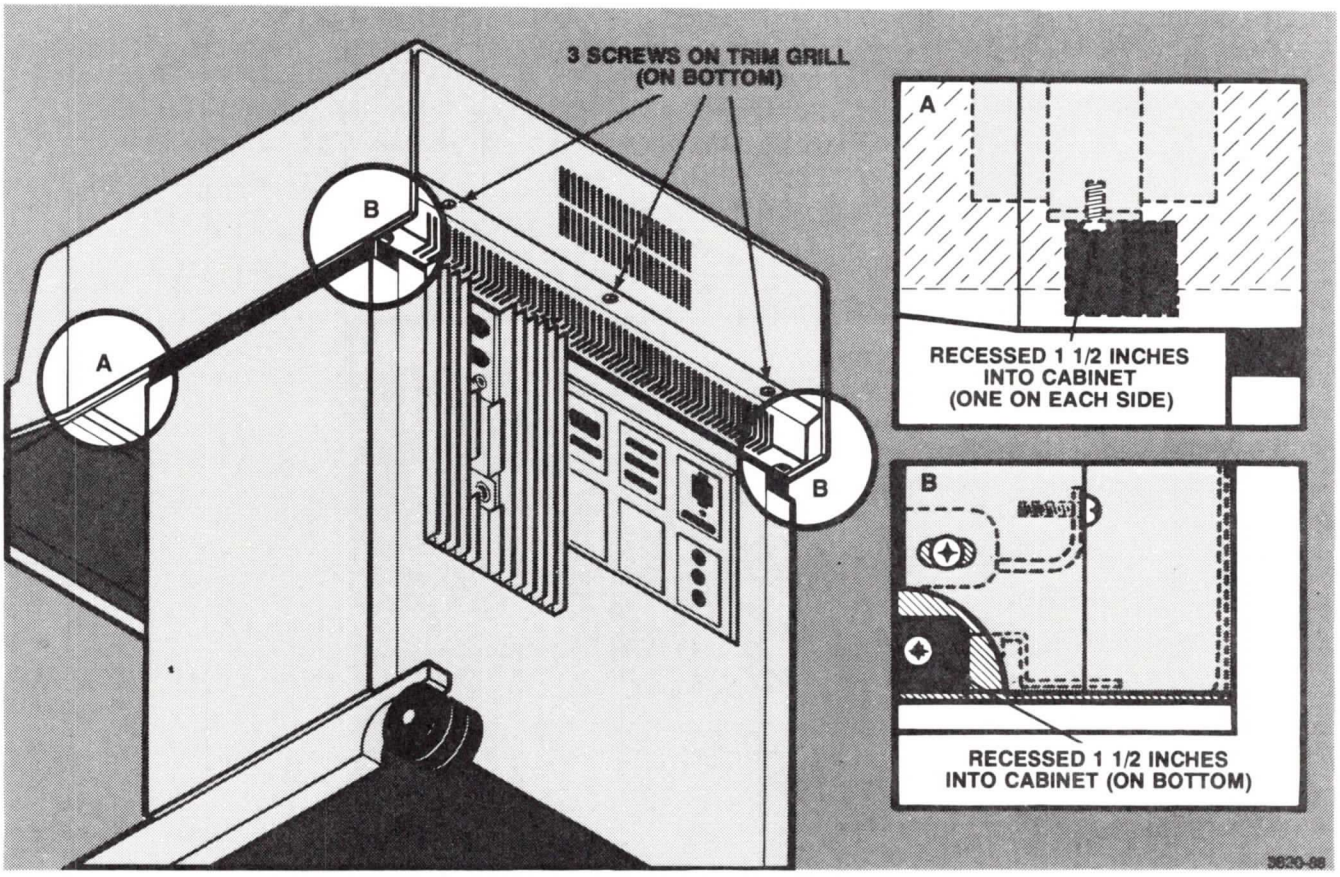


Figure 11-12. Trim Grill and Cabinet Top Screw Locations.

6. The cabinet top is now free of the chassis and ready to remove. Remove by gently sliding the panel back and upward, away from the chassis.

Keyboard Removal

1. Remove the cover directly underneath the keyboard. It is fastened by thirteen screws. (See Figure 11-11.) This exposes the bottom of the keyboard.

2. Remove the J1 and J2 connectors -- these attach to the thumbwheels. Also remove the connector attached to the speaker (J3), and the ribbon cable attached to the rear of the keyboard (J4). See Figure 11-13.

3. Remove the five screws holding the keyboard in place, while supporting the keyboard so that it does not fall. The keyboard is now free and can be removed from the chassis.

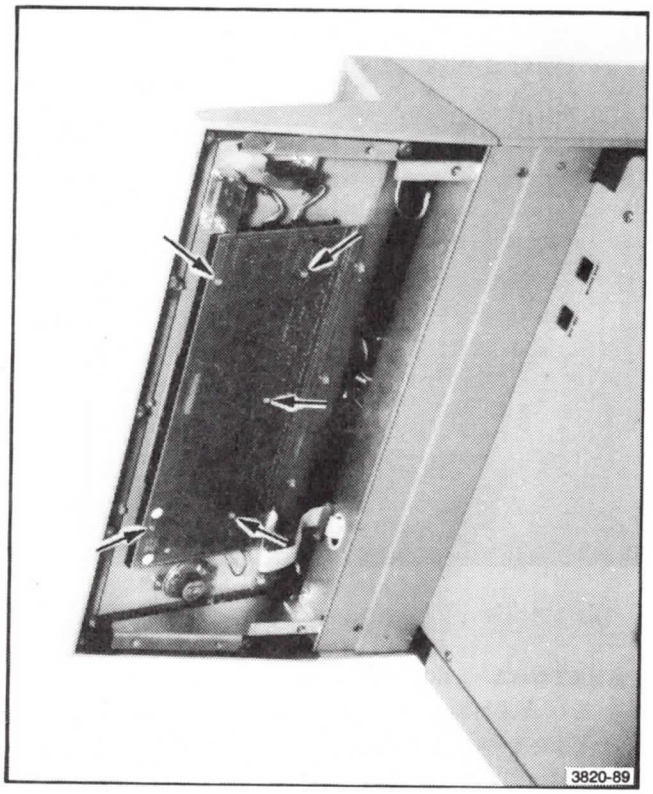


Figure 11-13. Removing the Keyboard.

Power Supply Module

Power Supply Removal

1. Turn off the terminal and remove the ac line cord from the ac power source.

2. Remove the ac line cord which goes to the display module at J3002.

3. Remove the front cover as shown in Figure 11-9.

4. Remove the plugs that attach to the fans or any disk drive units that may be installed. Note the way the plugs are removed from the power supply.

5. Remove the ON/OFF connector to the Inverter board through the hole in the backplate of the power supply.

6. Disconnect the ten spade lugs from the power supply. The four red wires are +5 V, the four black wires are the +5 V return, and the violet wires are the -5 V supply.

7. Disconnect the connectors labeled "to Motherboard", "to Flexible Disk Drives", and "to Reset, Self Test buttons".

8. Remove the two screws that pass through the cross-bar. These screws connect to the power supply and are located at the front of the pedestal.

9. Remove the eight screws on the back of the heat sink which hold the power supply in place. Six of the screws are in the first groove from the left and right edges -- three on each side. The last two screws are located in the second grooves from the left and right edges -- the lowest screws in that groove. (See Figure 11-14.)

10. Remove the power supply by pulling it straight back and away from the chassis.

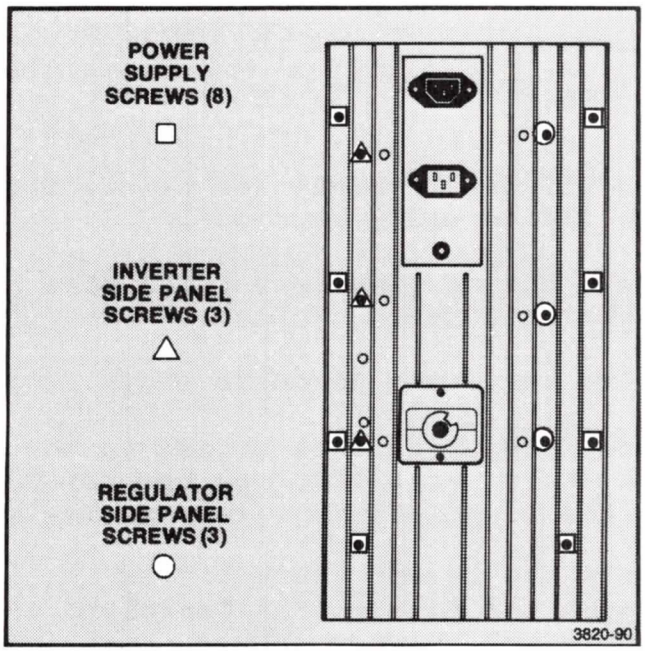


Figure 11-14. Power Supply Heatsink.

Power Supply Installation

Install the power supply in the reverse order of the removal procedure.

Inverter Board Removal

NOTE

A small wattage soldering iron must be used for Inverter board and Regulator board removal. Have one available before performing these procedures.

1. Remove the power supply as instructed in the "Power Supply Removal" procedure. Set the power supply so that it is resting on its rear heat sink, positioned on a stable work area.

2. Remove the aluminum inverter shield. There are three screws on the heatsink and three screws on the backing plate. (See Figures 11-14 and 11-15.)

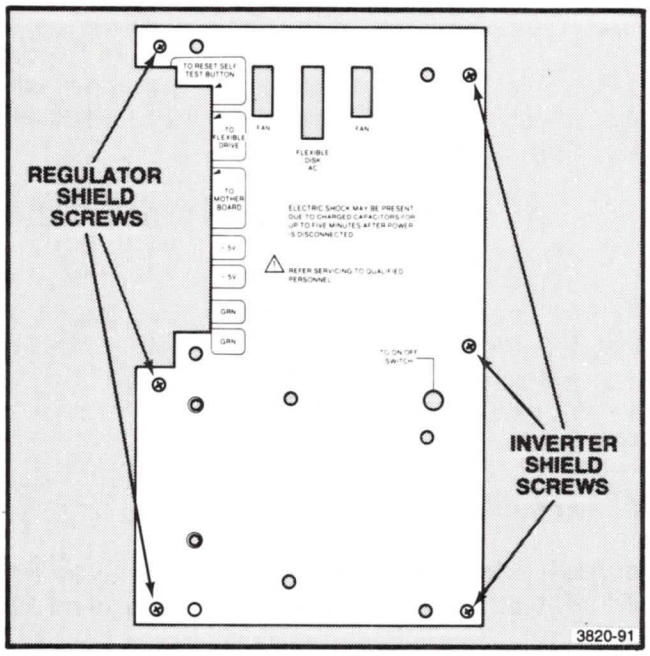


Figure 11-15. Backplate.

3. Disconnect P63 and P65. P63 is on the back of the Inverter board.

4. Unsolder the two wires from the line filter. The brown wire is in the "L" hole and the blue wire is in the "N" hole on the Inverter board.

5. Unsolder the three wires, one black and two grey, which come from the transformer. Unsolder these wires at the Inverter board. Upon reassembly, the black wire should go to the center hole.

6. Remove the square pin plug, P68.

7. Remove the two screws holding the switching transistors and plastic shield covers to the heat-sink. See Figure 11-14.

8. Remove the nine screws that hold the Inverter board in place.

9. Turn the power supply over so that the Regulator board is facing down and gently lift the Inverter board straight up. The six electrolytic capacitors come out with the board.

Inverter Board Installation

The Inverter board is installed in the reverse order that it is removed. Additional items that are needed for installing the board are:

- Heatsink compound (silicon grease).
- Eutectic solder (rosin core).
- Rosin cleaner and and acid brush.
- A pair of longnose pliers.

NOTE

When installing the plastic shield over the switching transistors, tighten the two screws alternately to insure even pressure on the transistors. The plastic shield should lie against the white alumina insulator for its complete length. Tighten the screws snugly, but DO NOT TIGHTEN EXCESSIVELY. This may crack the transistors.

When installing the one black and two grey wires (transformer wires), the black wire should be positioned in the center hole.

Regulator Board Removal

1. Remove the power supply as instructed in the section entitled "Power Supply Removal". Place the power supply so that it is resting on the heatsink on a stable work area.

2. Remove the regulator shield. There are three screws on the heatsink and three on the regulator shield.

3. Disconnect P82 at the Regulator board.

4. Remove the six screws holding the transistors to the heatsink. Do not disturb the alumina insulators or lose the insulating washers.

5. Unsolder the inductor lead going through hole "H". This wire connects to the anode of the diodes.

6. Unsolder the two black leads which run from the transformer to the cathodes of the diodes.

7. Unbolt the transformer secondary wires -- in the yellow sleeves -- from the diode cathodes using an offset screwdriver and a 1/4-inch wrench.

8. Unsolder the wire from the inductor on the Regulator board at hole "A".

9. Unsolder the three wires in holes X, Y, and Z. These are located on the back of the board.

10. Unsolder the three wires from the transformer to the back of the Inverter board (one black and two grey wires). When installing the Regulator board, the black wire must be soldered in the center hole on the Inverter board.

11. Remove the nuts from the transformer bracket on the back panel.

12. Remove the six screws holding the back panel in place.

13. Remove the eight screws holding the Regulator board in place.

14. Lift the Regulator board straight up and away from the power supply module. The transformer comes out with the Regulator board.

Regulator Board Installation

To install the Regulator board in the power supply, reverse the steps of the removal procedure. Additional items that are needed for installing the board are:

- Solder.
- Heatsink compound (silicon grease).
- Rosin cleaner and an acid brush.
- A pair of longnose pliers.

Card Cage

Card Cage Removal

1. Remove the front cover and rear panel as shown in Figures 11-9 and 11-10.

2. Remove all circuit boards from inside the card cage and any cables attached to these circuit boards.

3. Unplug the connectors at J17 and J19 on the Motherboard and the connector at J19 if the Motherboard Extender is installed (option 40).

4. Remove two screws that pass through the crossbar. Two of the screws connect the power supply to the chassis -- if the tablet interface option is installed (options 13 or 14), there are two more screws in this crossbar, making it a total of 4.

5. Remove the cable from the power supply which goes to the SELF TEST and MASTER RESET buttons.

6. Remove the plugs which go to the fans or any disk drive units that may be installed (option 42 or 43). Note the way these plugs are removed.

7. Remove the ON/OFF connector through the hole in the back-plate of the power supply.

8. Remove any 44 pin backets connected to the rear of the card cage. Be sure to disconnect the bracket which is attached to the card cage and not just the 44 pin connector. See Figure 11-16.

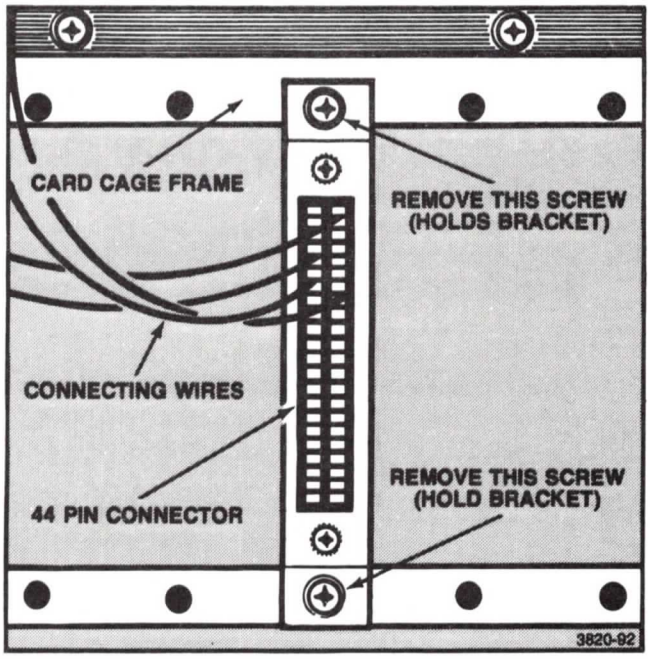


Figure 11-16. 44 Pin Connector and Bracket.

9. Remove the eleven screws which hold the inside rear panel to the chassis. Note that three of these screws are a different size than the other eight. See Figure 11-17.

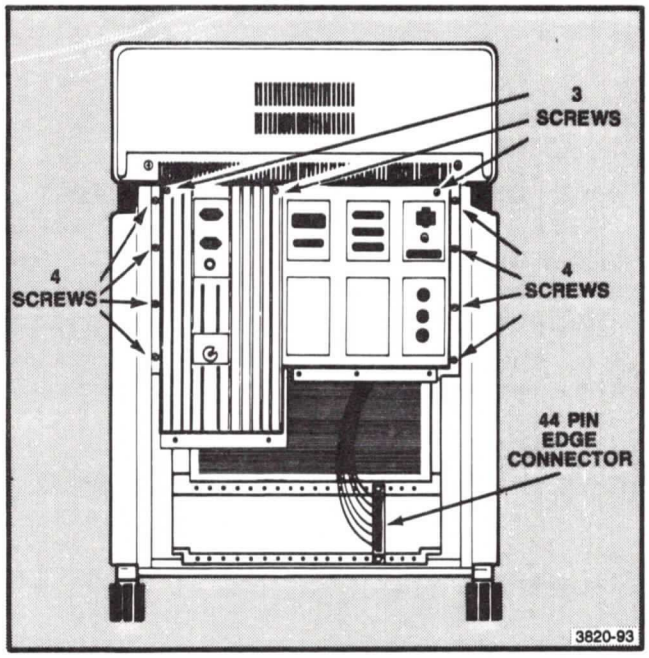


Figure 11-17. Removing the Inside Rear Panel.

10. Remove the whole upper rear assembly as a unit -- with the power supply and rear connectors attached -- by pulling it straight back and away from the chassis. The interconnecting cables come free with this assembly.

11. Remove the twelve screws holding the card cage in place -- eight in the rear of the card cage and four in the front.

12. Pull the card cage through the rear of the pedestal until it is free and clear of the chassis.

Card Cage Installation

Reverse the card cage removal procedure for installation, providing the inside rear panel has already been removed. If the rear panel and inside rear panel are still attached to the chassis, these must be removed before the card cage can be installed.

CAUTION

When installing the inside rear panel, be sure to route the wiring the same way that it was originally positioned. Pinching a wire in the chassis could result in grounding a voltage supply or signal, causing serious damage to the instrument.

Motherboard (and Motherboard Extender) Removal

1. Perform steps 1 through 10 in the Card Cage Removal procedure. If care is taken when removing the inside rear panel, step 8 may be eliminated. By eliminating this step, the rear inside panel can be removed with the 44 pin connectors still attached. The panel can then be laid on the power supply heatsink next to the pedestal chassis. This allows enough access to remove the Motherboard and Motherboard Extender.

2. Remove the eight screws holding the Motherboard to the card cage frame. This frees the Motherboard so that it can be removed.

3. The Motherboard Extender is held to the card cage frame by twelve screws and to the Motherboard by a board-to-board harmonica connector. When these screws are removed, the Motherboard Extender can be freed from the Motherboard by pulling gently to the left. This frees the harmonica connector.

Motherboard (and Motherboard Extender) Installation

1. Before the Motherboard or Motherboard Extender can be installed, the rear panel and inside rear panel must be removed. See "Card Cage Removal", steps 1-10.

2. Eight screws attach the Motherboard to the card cage frame.

3. The Motherboard Extender is installed by plugging the harmonica connector into the corresponding connector on the Motherboard and by attaching the board to the card cage frame by the twelve attaching screws.

4. Replace all cabinet covers and panels.

Circuit Board Removal

NOTE

This is a general removal procedure and applies for most boards in the card cage. For some circuit boards -- the Vector Generator board is an example -- there may be a ribbon cable that has to be disconnected before the circuit board can be removed.

1. Remove the front cover as shown in Figure 11-9.

2. Pull out on the upper and lower levers on the board. This unlocks the circuit board from the card cage. See Figure 11-18.

3. Remove the board by sliding it forward until it is free of the card cage.

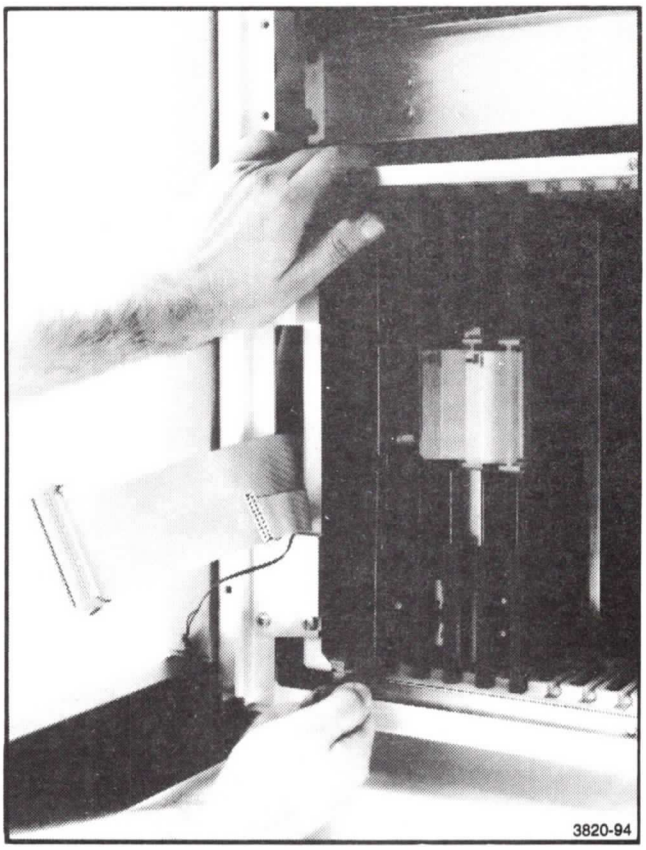


Figure 11-18. Removing Circuit Boards.

Circuit Board Installation

Reverse the removal procedure to install the circuit boards. The levers must remain extended until the circuit board is inserted all the way in the card cage. The circuit board is locked into position by pushing down and in on the levers.

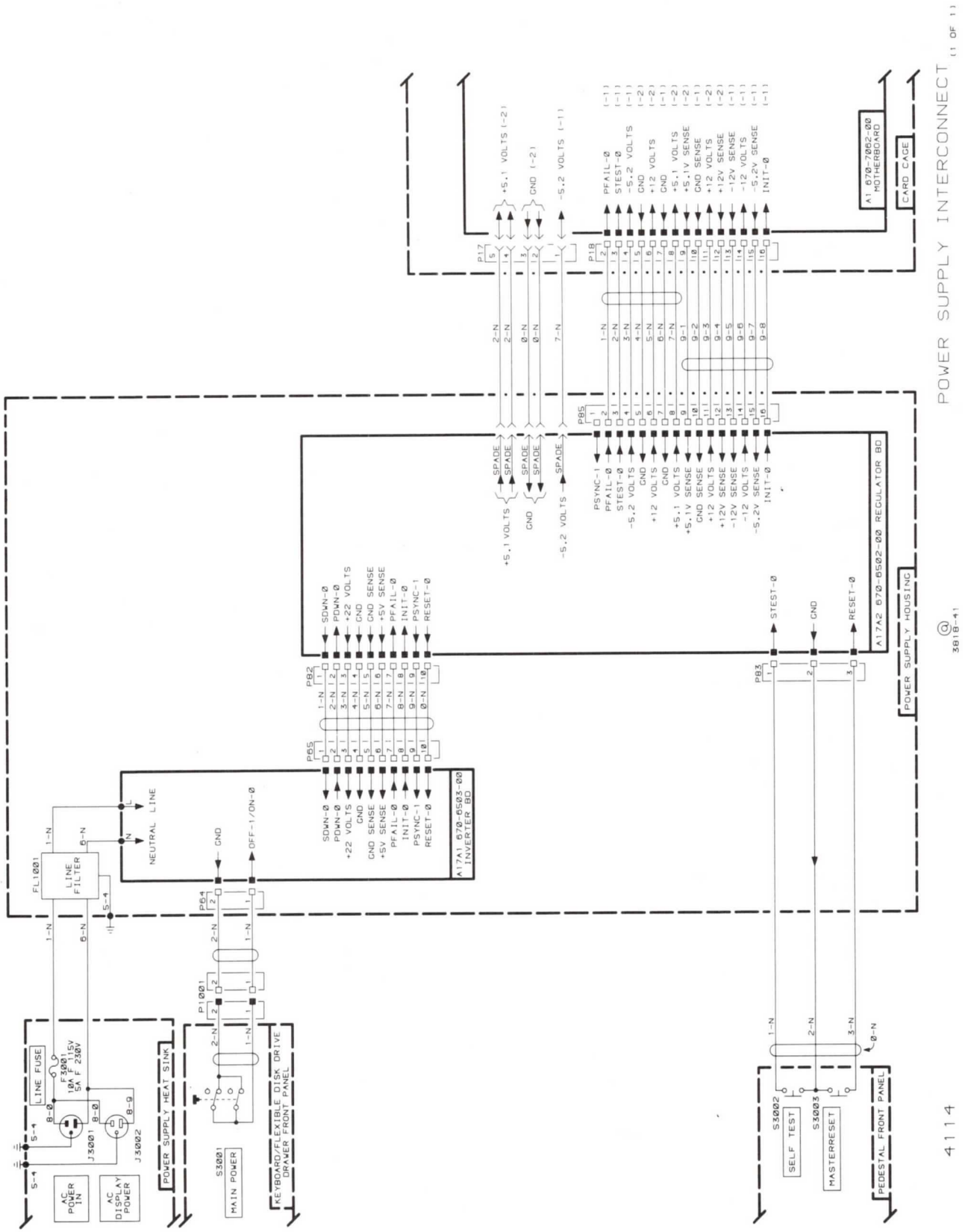
Section 12

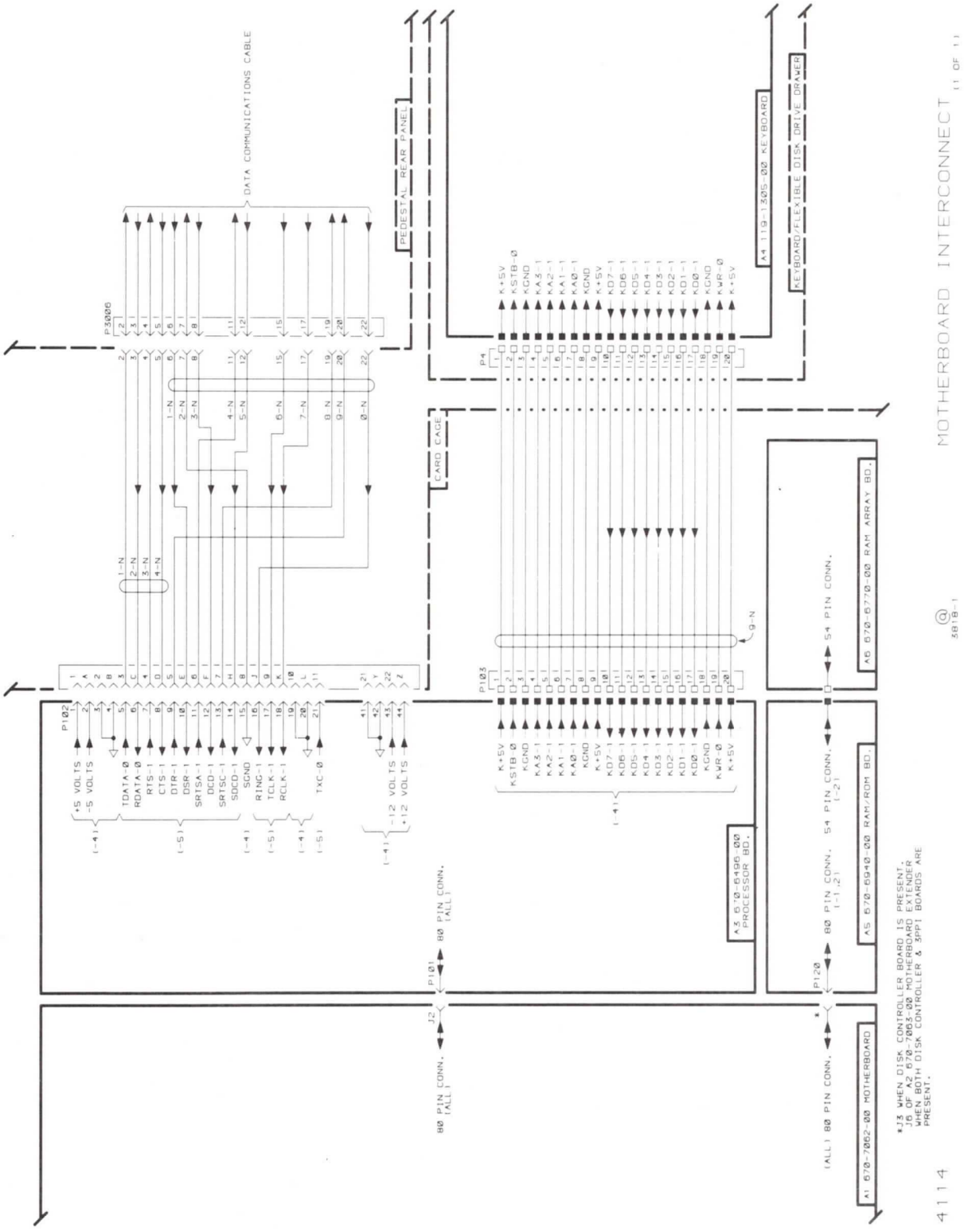
INTERCONNECT AND BLOCK DIAGRAMS

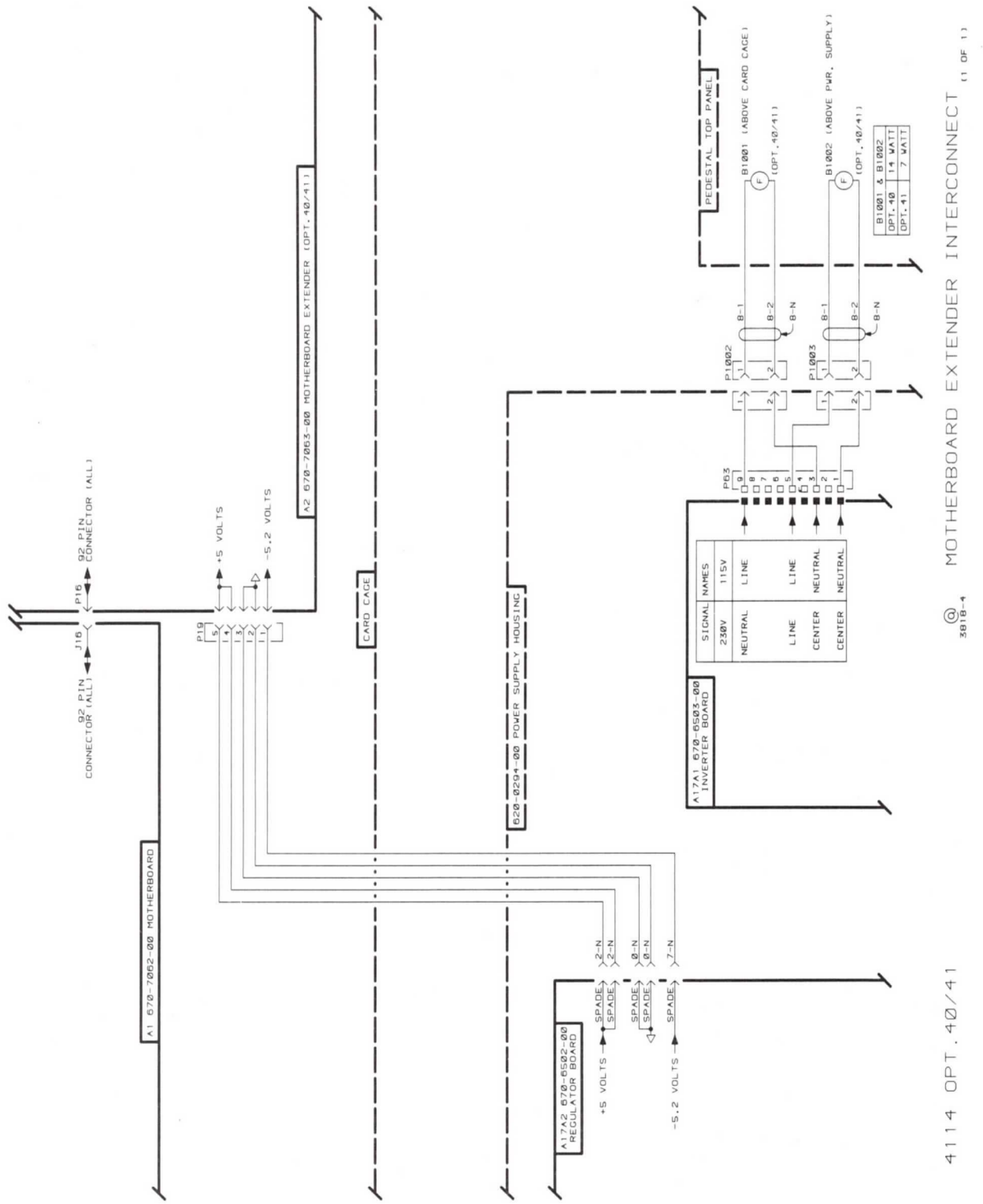
The following is a list of interconnect and block diagrams for the 4114. Some of these diagrams are also included in the Theory of Operation section but are repeated here for ease of referencing.

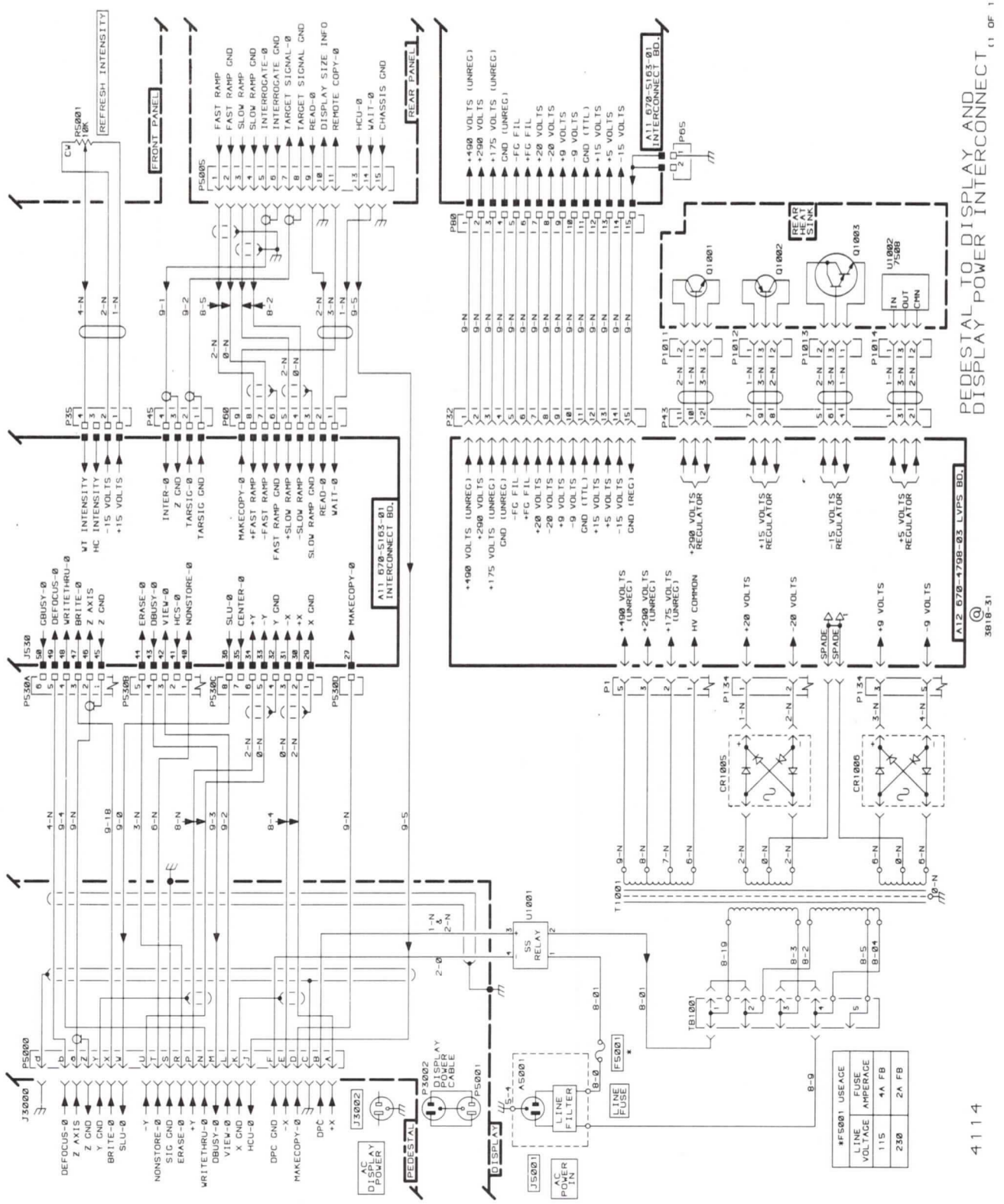
INTERCONNECT DIAGRAMS

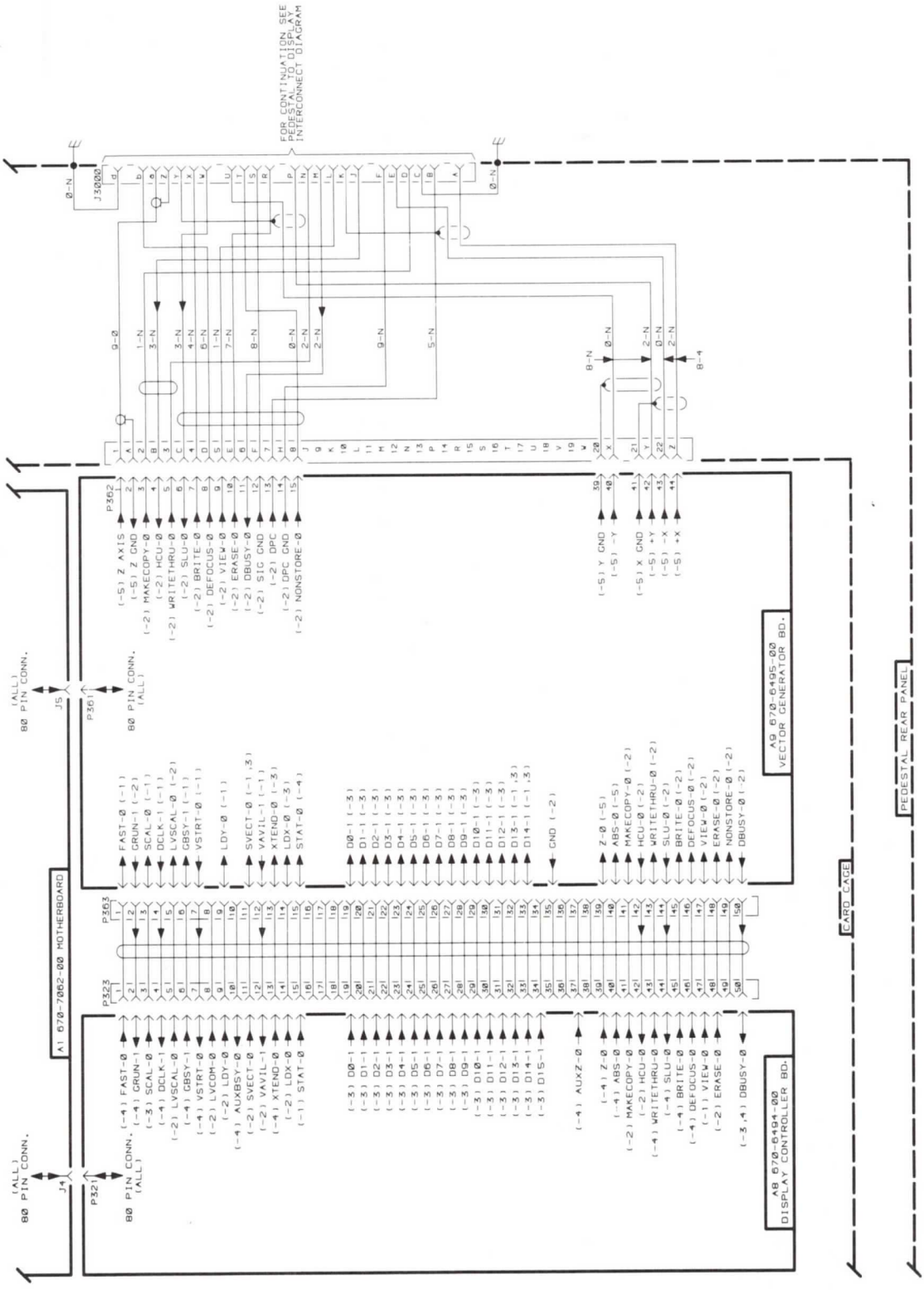
BLOCK DIAGRAMS

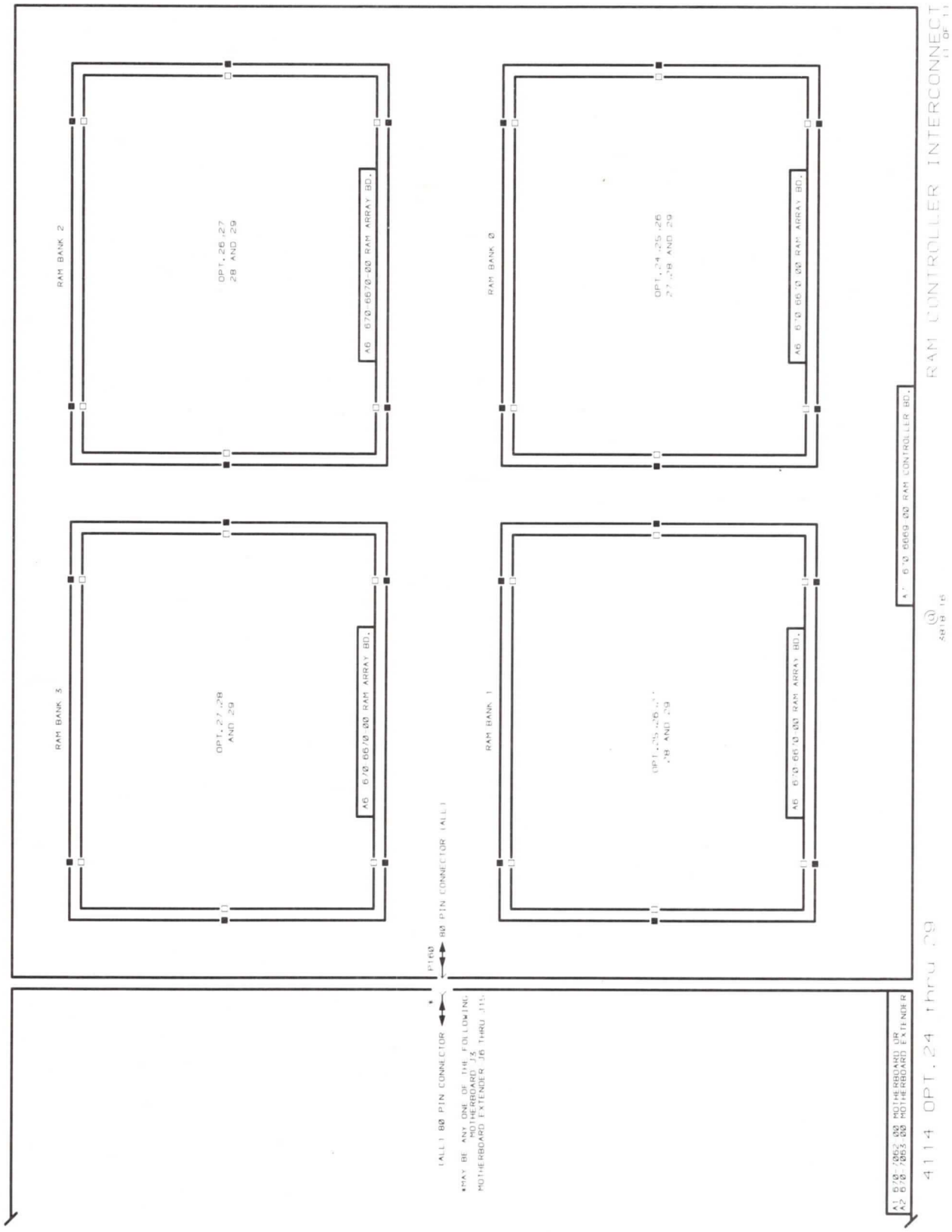

POWER SUPPLY INTERCONNECT (1 OF 1)
A1 670-7062-00 MOTHERBOARD
CARD CAGE
P17
P18
P85
+5.1 VOLTS (-2)
GND (-2)
-5.2 VOLTS (-1)
PFAIL-0
STEST-0
-5.2 VOLTS
GND
+12 VOLTS
GND
+5.1 VOLTS
+5.1V SENSE
GND SENSE
+12 VOLTS
+12V SENSE
-12V SENSE
-12 VOLTS
-5.2V SENSE
INIT-0
SPADE
PSYNC-1
A17A2 670-6502-00 REGULATOR BD
POWER SUPPLY HOUSING
STEST-0
GND
RESET-0
P83
P82
P65
SDWN-0
PDWN-0
+22 VOLTS
GND
GND SENSE
+5V SENSE
PFAIL-0
INIT-0
PSYNC-1
RESET-0
A17A1 670-6503-00 INVERTER BD
NEUTRAL LINE
OFF-1/ON-0
FL1001
LINE FILTER
P64
P1001
F3001 10A 115V 5A F 230V
LINE FUSE
J3001
J3002
AC POWER IN
AC DISPLAY POWER
POWER SUPPLY HEAT SINK
S3001
MAIN POWER
KEYBOARD/FLEXIBLE DISK DRIVE DRAWER FRONT PANEL
S3002
SELF TEST
S3003
MASTERRESET
PEDESTAL FRONT PANEL
4114
3818-41

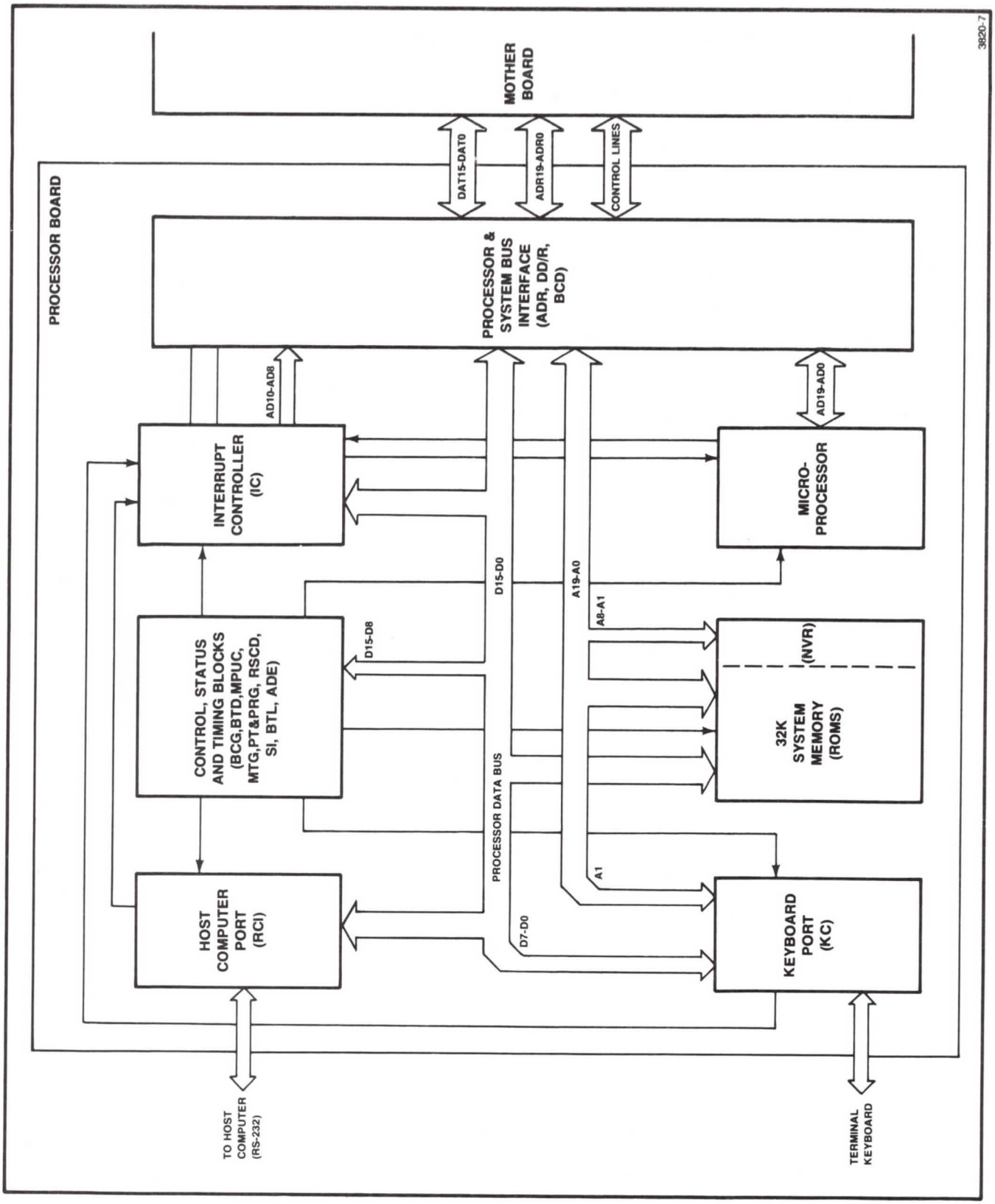

MOTHERBOARD INTERCONNECT (1 OF 1)
4114
DATA COMMUNICATIONS CABLE
PEDESTAL REAR PANEL
CARD CAGE
KEYBOARD/FLEXIBLE DISK DRIVE DRAWER
A4 119-1305-00 KEYBOARD
P3000
P4
P102
P103
P101
P120
J2
+5 VOLTS
-5 VOLTS
TDATA-Ø
RDATA-Ø
RTS-1
CTS-1
DTR-1
DSR-1
SRTSA-1
DCD-1
SRTSC-1
SDCD-1
SGND
RING-1
TCLK-1
RCLK-1
TXC-Ø
-12 VOLTS
+12 VOLTS
K+5V
KSTB-Ø
KGND
KA3-1
KA2-1
KA1-1
KA0-1
KD7-1
KD6-1
KD5-1
KD4-1
KD3-1
KD2-1
KD1-1
KD0-1
KWR-Ø
A3 670-6496-00 PROCESSOR BD.
A5 670-6940-00 RAM/ROM BD.
A6 670-6770-00 RAM ARRAY BD.
54 PIN CONN.
80 PIN CONN. (ALL)
(ALL) 80 PIN CONN. MOTHERBOARD
A1 670-7062-00 MOTHERBOARD
*J5 WHEN DISK CONTROLLER BOARD IS PRESENT.
J6 OF A1 670-7062-00 MOTHERBOARD EXTENDER
WHEN BOTH DISK CONTROLLER & SPPI BOARDS ARE PRESENT.


A1 670-7062-00 MOTHERBOARD
92 PIN CONNECTOR (ALL)
J16
P16
92 PIN CONNECTOR (ALL)
P19
+5 VOLTS
-5.2 VOLTS
A2 670-7063-00 MOTHERBOARD EXTENDER (OPT. 40/41)
CARD CAGE
620-0294-00 POWER SUPPLY HOUSING
A17A1 670-6503-00 INVERTER BOARD
A17A2 670-6502-00 REGULATOR BOARD
SIGNAL NAMES
230V LINE
NEUTRAL
LINE
LINE
CENTER NEUTRAL
CENTER NEUTRAL
P63
P1002
P1003
PEDESTAL TOP PANEL
B1001 (ABOVE CARD CAGE)
B1002 (ABOVE PWR. SUPPLY)
(OPT. 40/41)
B1001 & B1002
OPT. 40 14 WATT
OPT. 41 7 WATT
SPADE
+5 VOLTS
-5.2 VOLTS
@ MOTHERBOARD EXTENDER INTERCONNECT (1 OF 1)
3818-4
4114 OPT. 40/41

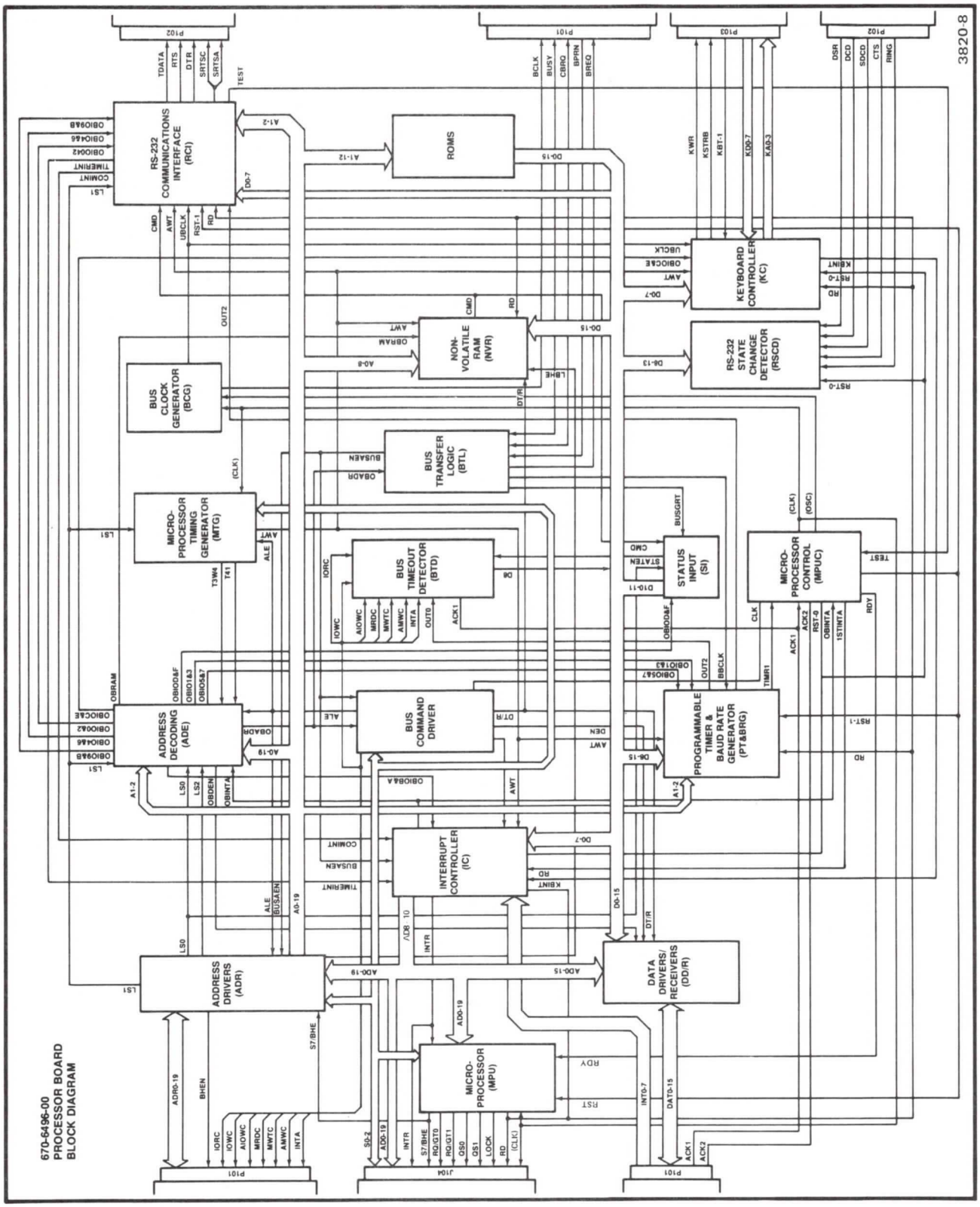

PEDESTAL TO DISPLAY AND DISPLAY POWER INTERCONNECT (1 OF 1)
4114
*FS001 USEAGE
LINE VOLTAGE
FUSE AMPERAGE
115
4A FB
230
2A FB
FRONT PANEL
REAR PANEL
PEDESTAL
DISPLAY
A11 670-5103-01 INTERCONNECT BD.
A12 670-4798-03 LVPS BD.
+100 VOLTS (UNREG)
+290 VOLTS
+175 VOLTS (UNREG)
GND (UNREG)
-FG FIL
+FG FIL
+20 VOLTS
-20 VOLTS
+9 VOLTS
-9 VOLTS
GND (TTL)
+15 VOLTS
+5 VOLTS
-15 VOLTS
GND (REG)
+290 VOLTS REGULATOR
+15 VOLTS REGULATOR
-15 VOLTS REGULATOR
+5 VOLTS REGULATOR
HV COMMON
REAR HEAT SINK
Q1001
Q1002
Q1003
U1002 7508
IN
OUT
CMN
FAST RAMP
FAST RAMP GND
SLOW RAMP
SLOW RAMP GND
INTERROGATE-0
INTERROGATE GND
TARGET SIGNAL-0
TARGET SIGNAL GND
READ-0
DISPLAY SIZE INFO
REMOTE COPY-0
HCU-0
WAIT-0
CHASSIS GND
REFRESH INTENSITY
WT INTENSITY
HC INTENSITY
-15 VOLTS
+15 VOLTS
INTER-0
Z GND
TARSIG-0
TARSIG GND
MAKECOPY-0
+FAST RAMP
-FAST RAMP
FAST RAMP GND
+SLOW RAMP
-SLOW RAMP
SLOW RAMP GND
READ-0
WAIT-0
GBUSY-0
DEFOCUS-0
WRITETHRU-0
BRITE-0
Z AXIS
Z GND
ERASE-0
DBUSY-0
VIEW-0
HCS-0
NONSTORE-0
SLU-0
CENTER-0
+Y
-Y
Y GND
-X
+X
X GND
MAKECOPY-0
DEFOCUS-0
Z AXIS
Z GND
Y GND
BRITE-0
SLU-0
-Y
NONSTORE-0
SIG GND
ERASE-0
+Y
WRITETHRU-0
DBUSY-0
VIEW-0
X GND
HCU-0
DPC GND
-X
MAKECOPY-0
DPC
+X
DISPLAY POWER CABLE
AC DISPLAY POWER
AC POWER IN
LINE FILTER
LINE FUSE
SS RELAY
CR1005
CR1006
T1001
B1001
SPADE
SPADE
3818-31


DISPLAY CONTROLLER INTERCONNECT (1 OF 1)
4114
3818-19
A1 670-7062-00 MOTHERBOARD
A8 670-6494-00 DISPLAY CONTROLLER BD.
A9 670-6495-00 VECTOR GENERATOR BD.
CARD CAGE
PEDESTAL REAR PANEL
80 PIN CONN. (ALL)
FOR CONTINUATION SEE PEDESTAL TO DISPLAY INTERCONNECT DIAGRAM

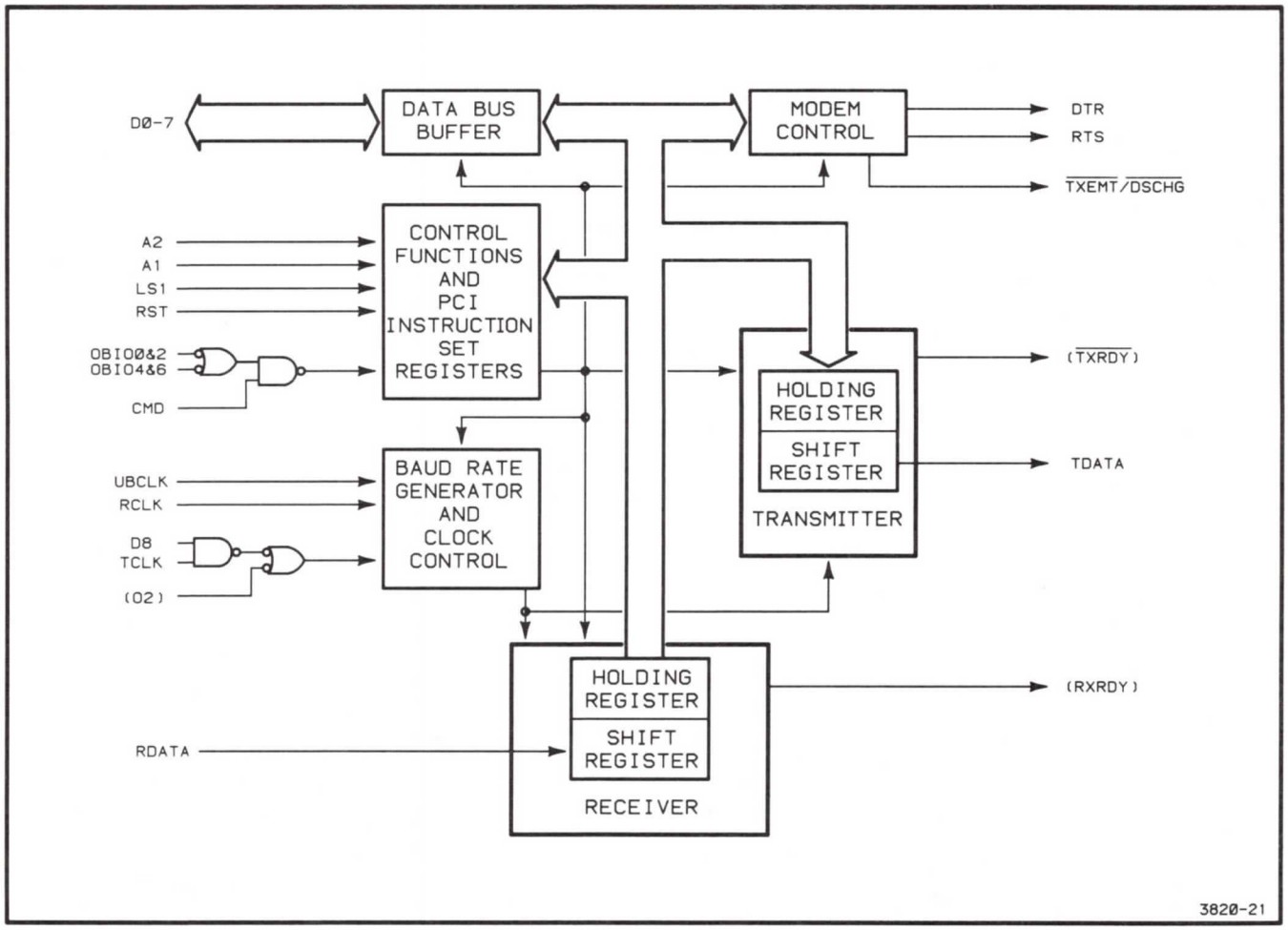

RAM CONTROLLER INTERCONNECT
11 OF 11
RAM BANK 2
OPT. 26,27
28 AND 29
A6 670-6670-00 RAM ARRAY BD.
RAM BANK 0
OPT. 24,25,26
27,28 AND 29
A6 670 6670 00 RAM ARRAY BD.
RAM BANK 3
OPT. 27,28
AND 29
A6 670 6670 00 RAM ARRAY BD.
RAM BANK 1
OPT. 25,26,27
,28 AND 29
A6 670 6670 00 RAM ARRAY BD.
A1 670 6669 00 RAM CONTROLLER BD.
P1&2
80 PIN CONNECTOR (ALL)
(ALL) 80 PIN CONNECTOR
*MAY BE ANY ONE OF THE FOLLOWING:
MOTHERBOARD J5
MOTHERBOARD EXTENDER J6 THRU J15
A1 670-7062 00 MOTHERBOARD UR
A2 670-7063 00 MOTHERBOARD EXTENDER
4114 OPT. 24 thru 29



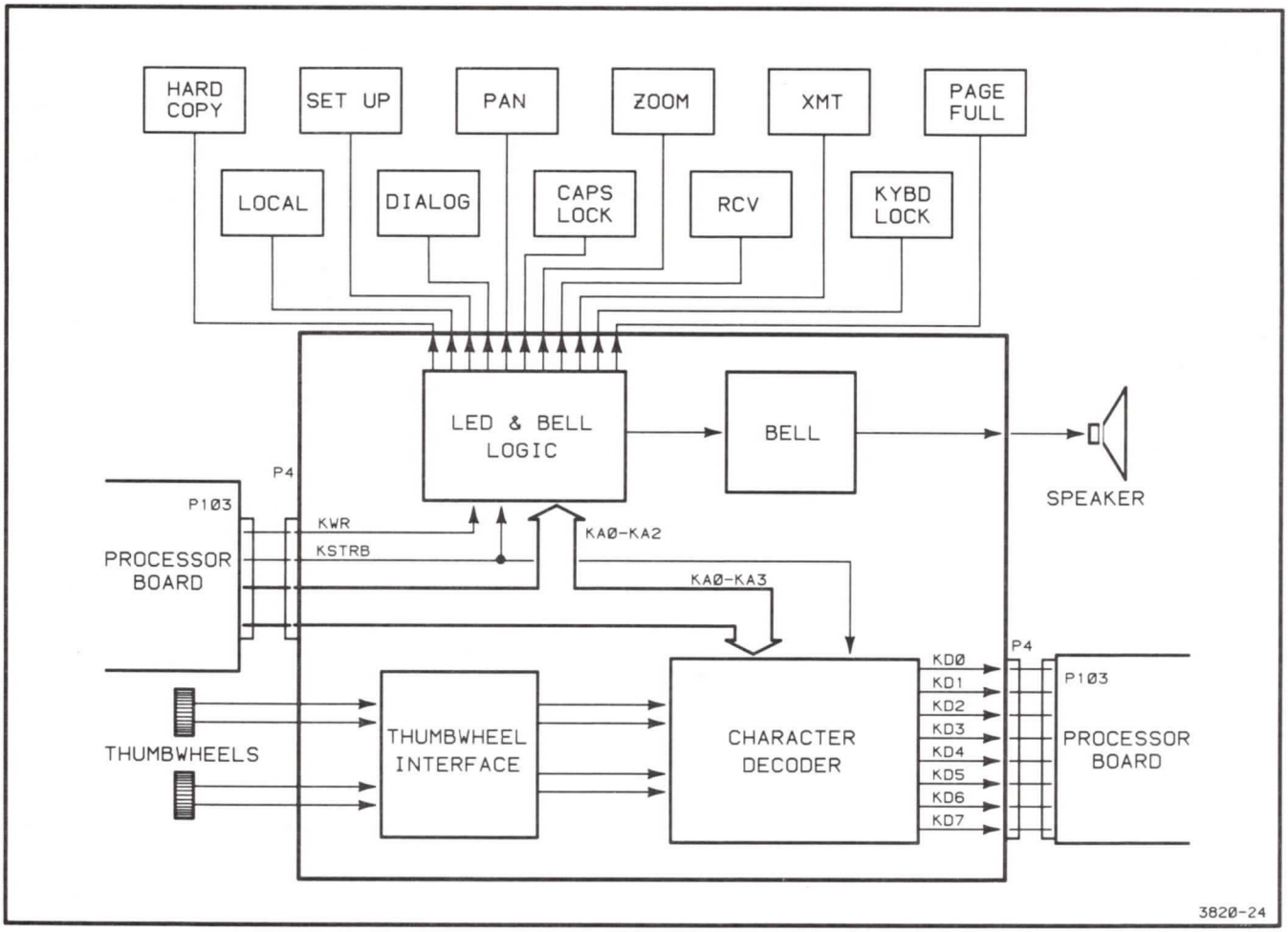
Simplified Processor Board.


3820-8
RS-232 COMMUNICATIONS INTERFACE (RCI)
ROMS
KEYBOARD CONTROLLER (KC)
NON-VOLATILE RAM (NVR)
RS-232 STATE CHANGE DETECTOR (RSCD)
BUS CLOCK GENERATOR (BCG)
BUS TRANSFER LOGIC (BTL)
MICRO-PROCESSOR TIMING GENERATOR (MTG)
BUS TIMEOUT DETECTOR (BTD)
STATUS INPUT (SI)
MICRO-PROCESSOR CONTROL (MPUC)
ADDRESS DECODING (ADE)
BUS COMMAND DRIVER
PROGRAMMABLE TIMER & BAUD RATE GENERATOR (PT&BRG)
INTERRUPT CONTROLLER (IC)
ADDRESS DRIVERS (ADR)
DATA DRIVERS/ RECEIVERS (DD/R)
MICRO-PROCESSOR (MPU)
670-6496-00
PROCESSOR BOARD
BLOCK DIAGRAM

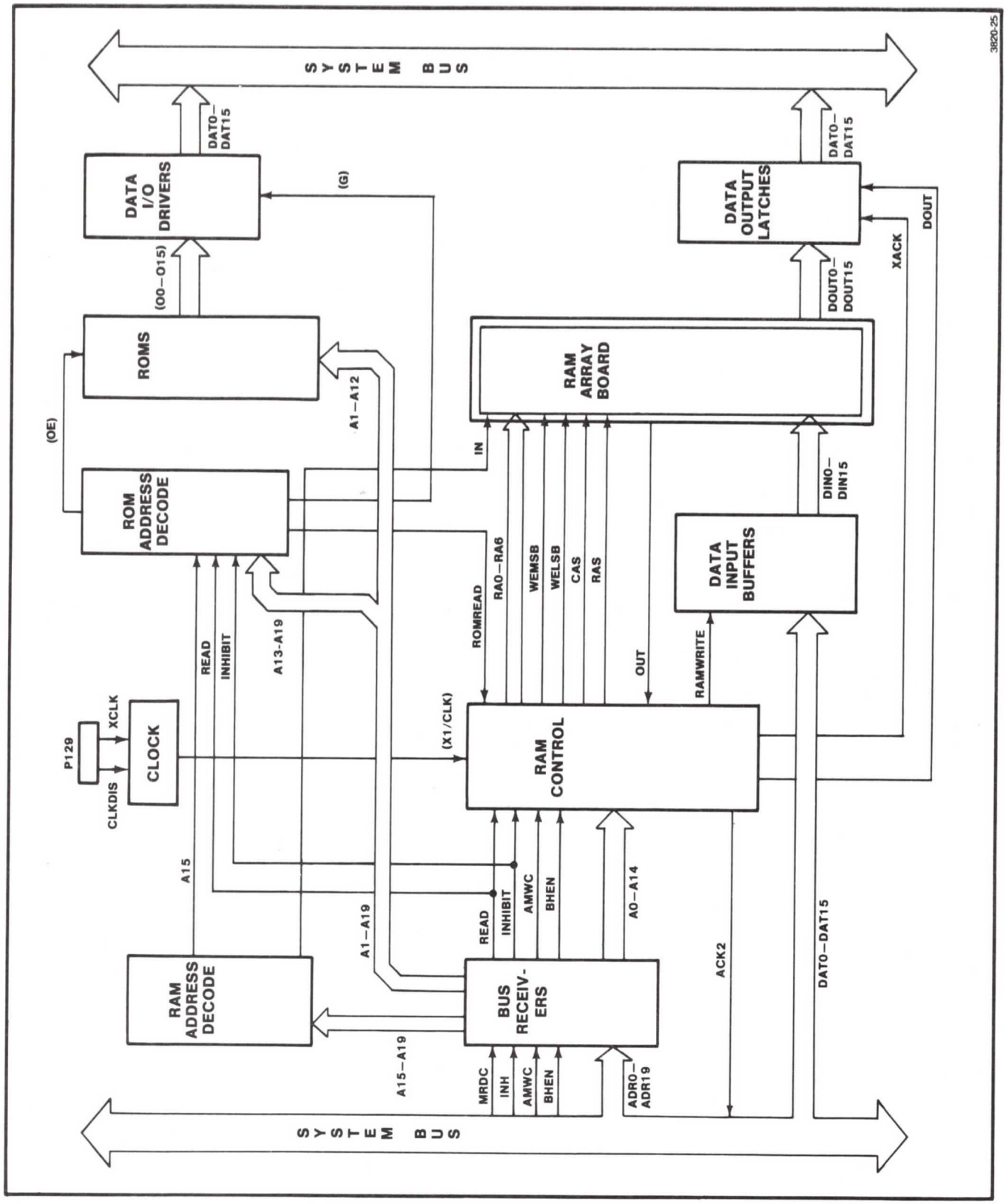
Processor.



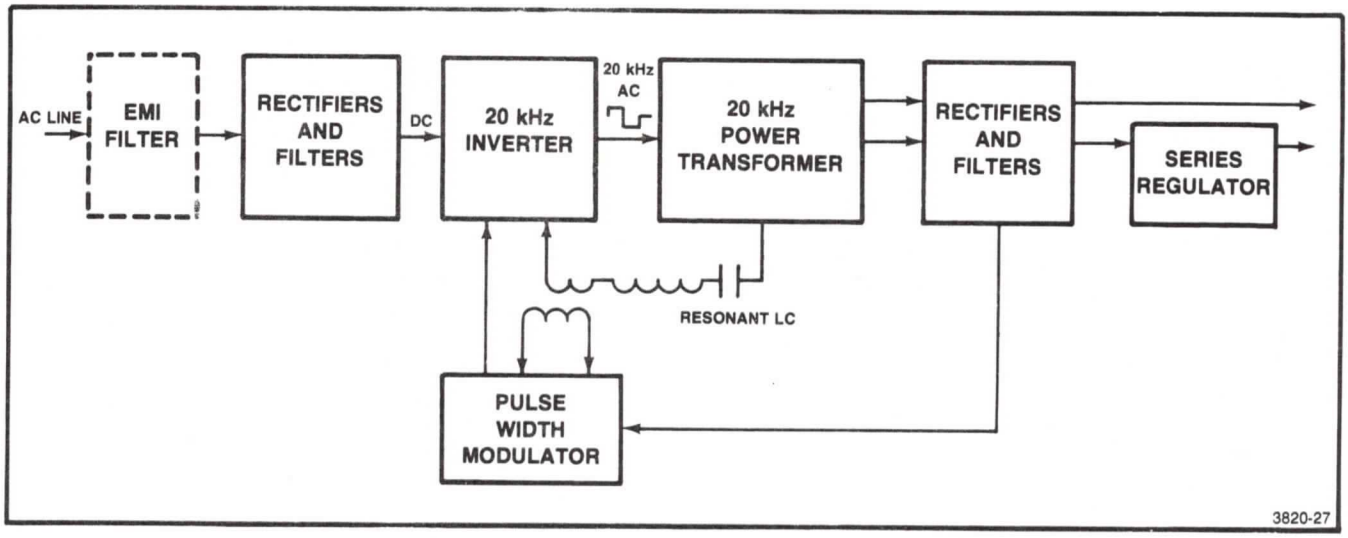
Programmable Communications Interface.


HARD COPY
SET UP
PAN
ZOOM
XMT
PAGE FULL
LOCAL
DIALOG
CAPS LOCK
RCV
KYBD LOCK
LED & BELL LOGIC
BELL
SPEAKER
P4
P103
PROCESSOR BOARD
KWR
KSTRB
KA0-KA2
KA0-KA3
THUMBWHEELS
THUMBWHEEL INTERFACE
CHARACTER DECODER
KD0
KD1
KD2
KD3
KD4
KD5
KD6
KD7
P4
P103
PROCESSOR BOARD
3820-24

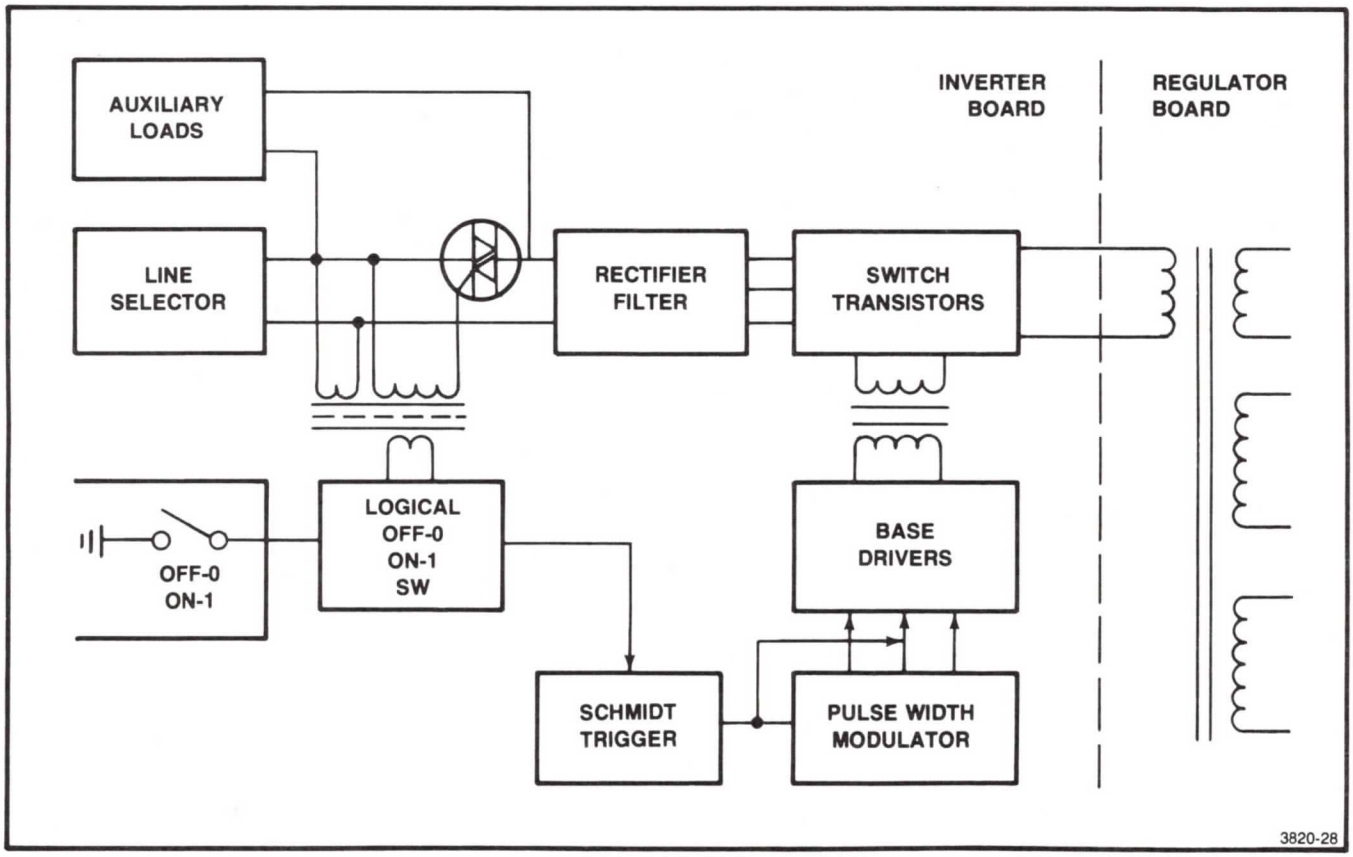
Keyboard.


3820-25
SYSTEM BUS
DATA I/O DRIVERS
DAT0–DAT15
(G)
(00–015)
ROMS
(OE)
ROM ADDRESS DECODE
A1–A12
A13-A19
READ
INHIBIT
A15
P129
XCLK
CLOCK
CLKDIS
RAM ADDRESS DECODE
A1–A19
A15–A19
MRDC
INH
AMWC
BHEN
BUS RECEIV-ERS
READ
INHIBIT
AMWC
BHEN
A0–A14
ACK2
DAT0–DAT15
ADR0–ADR19
(X1/CLK)
RAM CONTROL
ROMREAD
RA0–RA6
WEMSB
WELSB
CAS
RAS
OUT
RAMWRITE
IN
RAM ARRAY BOARD
DOUT0–DOUT15
DATA OUTPUT LATCHES
DAT0–DAT15
XACK
DOUT
DATA INPUT BUFFERS
DIN0–DIN15

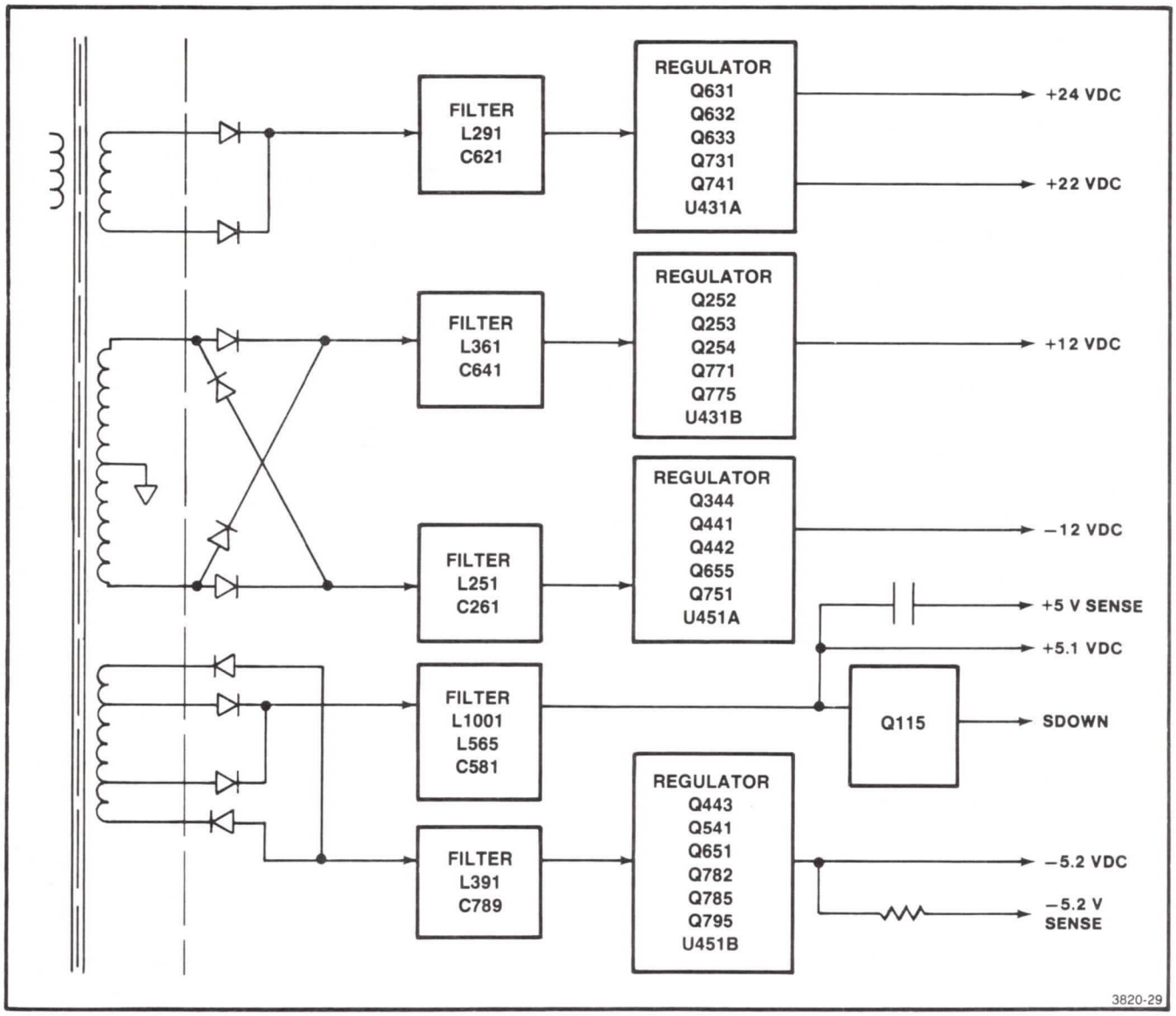
RAM/ROM.



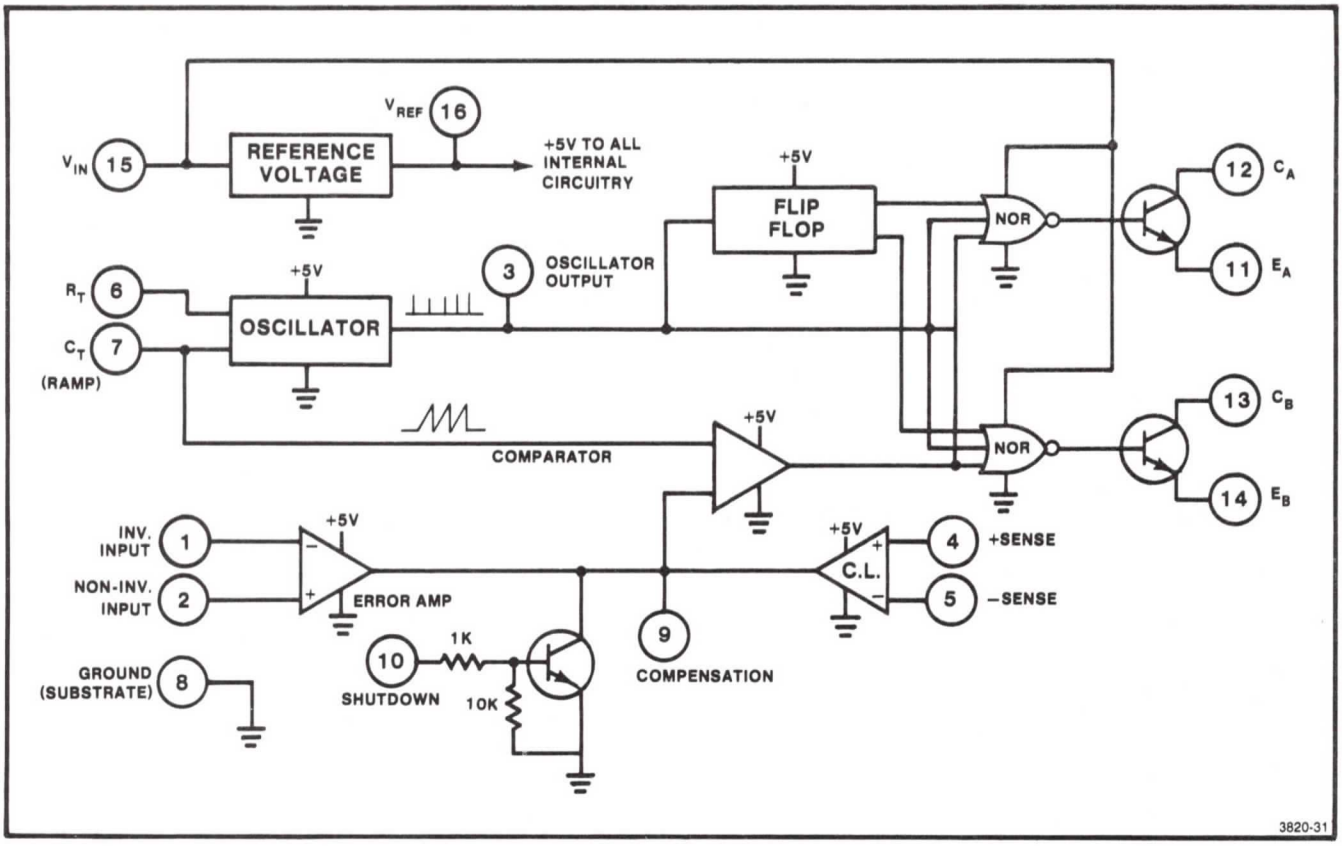
High Efficiency Power Supply.



Power Supply Inverter.



Power Supply Regulator.



Power Supply Pulse Width Modulator.

Appendix A

SIGNAL LIST

All named signals of the 4114 terminal are included in this alphabetical list. The first line of the entry under the "Explanation" column is an English-language description of the signal name mnemonic in the "Signal" column. There are two kinds of abbreviations used in the "Explanation" entries: abbreviations for blocks of circuitry named on the schematics and abbreviations for LSI integrated circuits.

Some signals on the Processor, RAM/ROM, and RAM Controller boards have the same names although they are not physically the same signals. They do, however, perform similar functions on their respective boards. Some instances are A0-19, CAS, and DIN0-15.

Bus signals are designated by their alphabetic name to which is appended the least significant bit (LSB) separated by a hyphen from the most significant bit (MSB). An example is the Processor board address bus, A0-19. There are 20 lines (bits) in this bus. A0 is the LSB and A19 is the MSB.

Processor Board Blocks

ADE	Address Decoding
ADR	address Drivers
BCD	Bus Command Driver
BCG	Bus Clock Generator
BTD	Bus Timeout Detector
BTL	Bus Transfer Logic
DD/R	Data Drivers/Receivers
IC	Interrupt Controller
KC	Keyboard Controller
MPU	Microprocessor
MPUC	Microprocessor Control
MTG	MPU Timing Generator
NVR	Non-Volatile Ram
PT&BRG	Programmable Timer & Baud Rate Generator
ROMS	Roms
RCI	RS-232 Communications Interface
RSCD	RS-232 State Change Detector
SI	Status Input

LSI Circuits

PIT	Programmable Interval Timer
PIC	Programmable Interrupt Controller
MPU	Microprocessor
PI MPU	Peripheral Interface Microprocessor
DRC	Dynamic RAM Controller
BC	Bus Controller

SIGNAL	SOURCE; DESTINATION	EXPLANATION
1STINTA-0	3-2; 3-1	First Interrupt Acknowledge. This Processor board signal indicates when the first of two interrupt acknowledge (INTA) cycles is occurring. Only the second INTA contains useful information.
A0-19	3-2;3-3,3-4, 3-5	(Local) Address (Bits 0 through 19). This is the Processor board address bus. It is created in the address drivers block from the MPU AD0-AD19 outputs. Note that some of these bits appear also on the RAM/ROM and RAM Controller boards with similar functions.
ABS-0	8-4;9-5	Absolute Position. Indicates to the Vector Generator that an absolute positioning operation is in progress.
ACK1-0	3-1; 3-1	Acknowledge 1. This system bus signal can be used as a slave response for no MPU wait states. The Processor board uses ACK1 to terminate a bus data transfer when it detects a bus timeout condition from the BTD circuitry.
ACK2-0	5-1; 3-1	Acknowledge 2. ACK2 serves as an advanced transfer acknowledge to eliminate WAIT states in the MPU. The signal derives from SACK-0 which is output by the timing and control block inside the dynamic RAM controller. SACK-0 indicates the beginning of a memory access cycle.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
AD0-19	3-1,3-2; 3-2	(MPU) Address/Data (Bits 0 through 19). These signals are the time-multiplexed memory I/O address and data bus output from the MPU. These bits are also input for data.
ADR0-19	3-2;P101	(System) Address (bits 0 through 19). These are the system bus address lines.
AIOWC-0	3-2; 3-1	Advanced IO Write Command. This signal gives system bus IO devices early indication of a write instruction. The timing is the same as a read command.
ALE-1	3-2; 3-1,3-3	Address Latch Enable. ALE-1 strobes an address into the ADE block. It also synchronizes the Microprocessor Timing Generator, and DEGLITCHES the ROM bank decoder.
AMWC-0	3-2; 3-1	Advanced Memory Write Command. AMWC-0 gives early indication of a write instruction to the system bus memory. The timing is the same as a read command--MRDC.
ANODE	18-1;19-1	(crt) Anode. Passes through a current limiting resistor in the Hard Copy Amplifier board to the anode of the crt.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
ANTIBURN	14-2;17-1	Antiburn. (Made up from LA and SA ANTI-BURN signals on schematic.) If positive, decreases the Z-Axis amplifier drive, reducing the CRT writing beam intensity. Goes positive when deflection aproaches zero velocity.
AWT-0	3-1;3-2,3-4, 3-5	Advanced Write. This is the advanced write command to all on-board devices. AWT is derived from the MPU status lines and the Microprocessor Timing Generator.
BANKIN-0	7-2;7-1	Bank In. BANKIN is used in the address decoding logic on the RAM Controller board to indicate the presence or absence of a RAM Array board.
BBCLK-1	3-1;3-5	Buffered Bus Clock. BBCLK is a 4.9152 MHz signal which synchronizes the bus transfer logic and is the frequency source for the Programmable Timer and (Transmit) Baud Rate Generator block.
BCLK-0	3-1; 3-1	Bus Clock. BCLK is the system bus clock. It is a 4.9152 MHz square wave and is used by bus devices to synchronize bus master transfers. It is also used as a stable frequency source.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
BHEN-0	3-2;P101	Byte High Enable. On the Processor board, ULBHEN is latched and then driven onto the system bus as BHEN. BHEN enables the high byte--D8-15-- on read, write, and interrupt acknowledge cycles.
BPRN-0	1-2; 3-1	Bus Priority In. BPRN is a signal from the bus priority logic on the Motherboard that informs a potential bus master board that it has permission to become bus master.
BREQ-0	3-1;P101	Bus Request. BRQ is a signal from a potential bus master board to the bus priority logic on the Motherboard that indicates that the potential bus master board needs to become the actual bus master.
BRITE-0	8-4;17-1	Brite. A TTL low from the Display Controller activates BRITE Intensity adjustable by R415 in the Intensity Control Logic. In combination with low level on DEFOCUS-0, the BRITE-DEFOCUS mode is useful for displaying wide vectors.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
BUSAEN-0	3-1; 3-2	BUS Address Enable. BUSAEN indicates that a board is bus master of the system bus. BUSAEN is input to the AEN input of the bus controller IC. AEN enables the bus controller to output the bus commands MRDC, MWTC, AMWC, IORDC, etc. BUSAEN is gated with INTA and input to the INTA input of the PIC.
BUSGRT-1	3-1;3-5	Bus Grant. This signal is similar to BUSAEN, but has a slight timinig difference.
BUSY-0	3-1; 3-1	(Bus) Busy. BUSY indicates that a bus master is currently using the system bus. BUSY delays bus master transfer until the current bus master is done.
CAS-0	7-1;7-2 5-1;5-2,6-1	Column Address Strobe. This signal is generated by the DRC on both the RAM/ROM and the RAM Controller boards. CAS strobes the seven multiplexed column address bits appearing on RA0-6 into the RAMs on the RAM Array board.
CATHODE	18-2;19-1	(crt) Cathode. Ties cathode of crt to ground.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
CBRQ-0	3-1; 3-1	Common Bus Request. CBRQ is used by potential bus masters to request bus mastership from higher priority bus masters. CBRQ is generated by the Processor board along with BRQ. The Processor board also listens to CBRQ and gives up the bus when another board asserts CBRQ.
CCEN-1	9-1;9-2	Completion Counter Enable. Enables Completion Counter during vector generation.
CE1 & CE2	18-2;19-1	Collimation Electrodes, 1 and 2. The collimation electrodes, CE1 and CE2, are electronic lenses that cause a uniform flood gun beam pattern over the target.
CENTER-0	15-1;14-1	Centering. When low, it inhibits and resets the operation of the Origin Shift Counter. (not used in the 4114 display)
CLK-1	3-1; 3-2	Clock. CLK is a direct output of the Clock Generator IC. It outputs a 4.9152 MHz square wave with a one third duty cycle. All blocks that must be synchronized with the local processor bus use this signal.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
CLKDIS-0	P129;5-1 P166;7-1	Clock Disable. A TTL logic low level applied to this input pin disables the clock circuitry on the RAM/ROM or the RAM Controller board. (This is a test point for factory use only).
CMD-1	3-4;3-5	Command. CMD is the logical OR of RD and AWT on the Processor board.
COMINT-0	3-5; 3-2	Communications Interrupt. COMINT is the RS-232 Communications Interface received character interrupt signal. Other RS-232 interrupts are included in the TIMERINT signal.
CTS-1	P102;3-5	Clear To Send. CTS is an RS-232 status input.
CUTX-0	9-3;9-5	Cut X (axis). Cuts off CRT beam when scissoring occurs in the X axis.
CUTY-0	9-4;9-5	Cut Y (axis). Cuts off CRT beam when scissoring occurs in the Y axis.
CX0-11	9-3;9-2	X Shift Register Data. Parallel load data for X Counter.
CY0-11	9-4;9-4	Y Shift Register Data. Parallel load data for Y Counter.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
D0-15	3-2;3-3,3-4, 3-5	(Local) Data (Bus). These lines are the local data bus for the Processor board.
DAT0-15	3-2;P101,8-3	(System) Data (Bus). These line are the system data bus.
DBUSY-0	18-1;8-1,8-2, 8-3,8-4, 9-2	Display Busy. When low, it indicates that the display is busy in HOLD mode, erasing the screen, or in Hard Copy operation. This line states that the monitor is busy and cannot accept further information until brought out of one of these modes.
DCD-1	P102;3-5	Data Carrier Detect. DCD is an RS-232 status input.
DCLK-1	9-1;8-4	Dot (or dash) Clock. Clock for dot (or dash) pattern.
DCZ-1	9-2;9-1	Displacement Counter Zero. Indicates that the displacement between characters is either completed or not to be done.
DD0-15	8-3;9-1,-3	Display Data Bits 0 to 15. Sixteen bits of data transferred between the Display Controller and the Vector Generator (or optional board).

SIGNAL	SOURCE; DESTINATION	EXPLANATION
DEFOCUS-0	8-4;17-1	Defocus. When low, the focus of the crt writing beam is reduced, producing a slightly wider trace (defocused). When high, the writing beam is focused. The use of the DEFOCUS-0 signal line allows a focused or defocused crt writing beam when used in combination with WRITE-THRU, BRITE, and NORMAL.
DIN0-15	5-2;6-1 7-2;6-1	Data In Bits 0 through 15. During RAM write operations, these 16 data bits contain the data that is written into RAM on the RAM Array board.
DINLSB-0	7-1;7-2	Data Input Enable Least Significant Byte. During RAM write operations, DINLSB enables the data input buffer for the least significant byte of data to drive data from the bus onto RAM data lines DIN0-7 to the RAM Array boards.
DINMSB-0	7-1;7-2	Data Input Enable Most Significant Byte. During RAM write operations, DINMSB enables the data input buffer for the most significant byte of data to drive data from the bus onto RAM data lines DIN8-15 to the RAM Array boards.
DIS. SIZE IN.	J5005;HCU	Display Size Information. Tied to ground (logical low). When tied low, it informs the hard copy unit that it is scanning a 19 inch display.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
DOUT-0	7-1;7-2 5-1;5-2	Data Output Enable. During RAM read operations, DOUT enables the Data Output Latches to output their data to the system bus.
DOUT0-15	6-1;5-2 6-1;7-2	Data Output Bits 0 through 15. These 16 data bits from the RAM Array board contain the RAM data output bits during RAM read operations.
DPC	9-2;15-1	Display Power Control. Causes display ac power to be turned on. 10mA at +9 to +12 V.
DS-1	9-1;9-1	Data Shift. Indicates the data in the shift registers is not normalized and requires shifting.
DSCAL-0	9-1;9-2	Delayed Scale. Scale signal for vector being set up.
DSR-1	P102;3-5	Data Set Ready. DSR is an RS-232 status input.
DT-1/R-0	3-2;3-4	Data Transmit/Receive. DT-1/R-0 is a direct output of the bus controller. A high on this line indicates a WRITE to IO or memory and a low is a READ.
DTR-1	3-5;P102	Data Terminal Ready. DTR is an RS-232 status output.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
DYNAMIC FOCUS	14-1;17-1	Dynamic Focus. This signal modifies the focus electrode voltage to maintain a consistently focused writing beam over the display screen.
ERASE TRIGGER	18-1;18-2	Erase Trigger. Triggers the crt to erase via ERASE-0 line.
ERASE-0	8-2;18-1	Erase. Initiates the erase cycle in the storage board circuits. Erases the crt. Must be greater than 2us. A READ-0 or WAIT-0 signal prevents erasure during hard copy operation.
FAST RAMP	HCU;14-1	Fast Ramp. Analog deflection voltage from the HCU which controls the vertical deflection during the hard copy scan. (There are "+" and "-"FAST RAMPs on the schematics.)
FG FIL	16-1;19-1	Flood Gun Filaments. Flood Gun filaments (+,- FG FIL on schematic) of crt. Driven by +,- 15 v from low voltage power supply.,
GBSY-1	8-4;9-1	Generator Busy. Vector generator is not ready to accept new vector data.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
GBUSY	8-4;18-1	Generator Busy Optional signal that can be used to reset the view erase counters. A 100ns or greater pulse is required. A VIEW-0 signal also resets the view erase counters. (There is a view reset strap option between GBUSY and Z-AXIS.)
GRUN-1	9-2;8-4	Generator Running. Vector generator is drawing a vector.
HC INTENSITY	HCU;17-1	Hard Copy Intensity. Controls the crt writing beam intensity by adjustment of R228 (Hard Copy intensity adjustment).
HCS-0	18-1;17-1	Hard Copy Scan. Enables operation of Hard Copy circuitry. HCS-0 is asserted by either READ-0 or WAIT-0 (from the hard copy unit) going low. Initiates crt scan by the HCU.
HCS-1	18-1;18-2, 19-1	Hard Copy Scan. Inverted HCS-0. Enables operation of Hard Copy circuitry. Refer to signal HCS-0.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
HCU-0	HCU;8-2	Hard Copy Unit. Indicates to the display controller that the Hard Copy Unit is capable of accepting a MAKECOPY-0 request.
HOLD-0	18-1;14-1	Hold. Connects the channel switch to a separate set of inputs that are connected to ground when Hold mode is initiated. The grounded inputs prevent beam deflection and assure minimum deflection amplifier power dissipation during Hold mode. (Strap option on Deflection Amplifier board, operational in the IN position.)
IN-0	5-2;6-1	In. IN is used with OUT to indicate the presence or absence of a RAM Array board.
INH-0	--;5-1	(Read) Inhibit. When true low, INH inhibits memory circuitry from outputting its data onto the system bus during a read operation of the memory circuitry. See INHIBIT. INH may be output by test circuitry. Currently not used.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
INHIBIT-0	5-1;5-3	Inhibit. This signal is a buffered version of the system bus signal INH. This signal, when true low, inhibits the RAM/ROM board from outputting its data during RAM read or ROM read operations.
INIT-0	17-1;3-1,3-4,	Initialize. 9-1 INIT is used to generate reset which goes directly to the MPU and does a power-up reset operation. It also resets much of the sequential logic on the Processor board.
INT0-7	P101;3-2	Interrupt 0 through 7. INT0--7 are interrupt request signals to the Processor board. INT0,4, or 5 can be generated by Processor board devices.
INTA-0	3-2; 3-1, 3-2	Interrupt Acknowledge. INTA is generated on the Processor board and is received by slave PICs on other boards. INTA notifies the slave PIC that its interrupt is acknowledged and it can put vectoring data on the System data bus.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
INTER-0	HCU;17-1	Interrogate. This is the hard copy interrogate pulse from the hard copy unit (HCU). As a result the crt writing beam is pulsed (100 ns pulse width) and a target information signal, TARSIG-0 is developed.
INTR-1	3-2; 3-1	Interrupt. INTR is a direct output of the INT pin of the PIC in the IC block. The signal is input directly to the MPU INTR input. INTR is the interrupt to the MPU.
IORC-0	3-2; 3-1	IO Read Command. This signal, when low, indicates that an IO device should drive its data onto the system bus.
IOWC-0	3-2;P101	IO Write Command. This signal, when low, indicates that an IO device should read data on the system bus.
KA0-3	3-4;P103	Keyboard Address 0 through 3. These signal lines carry key matrix column addresses in addition to LED address and on-off information.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
KD0-7	4-1;3-4	Keyboard Data 0 through 7. These lines carry key matrix data in addition to thumbwheel Grey code data.
KBDINT-0	4-1;3-2	Keyboard Interrupt. This signal is the interrupt for the keyboard. It is output from Pin 24 of the PIMPU and input to the IC block as INT4 into the PIC.
KBT3-1	P104;3-4	Keyboard Test. KBT is the test input to the KC MPU Keyboard Controller.
KSTRB-0	3-4;4-1	Keyboard Strobe. KSTRB latches KA0-KA3 data into the Keyboard board circuitry.
KWR-0	3-4;4-1	Keyboard Write. KWR latches KA0--KA3 into the Keyboard circuitry that controls the LEDs.
LBHE-0	3-2;3-4	Latched Byte High Enable. LBHE is the Processor board equivalent of the system bus signal, BHEN.
LCNT-0,-1	9-1;9-3,-4	Load Count. Enables counter parallel load.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
LCNTX-0	9-1;9-3	Load Count X axis. Loads X Counter with data for absolute position operation.
LCNTY-0	9-1;9-4	Load Count Y axis. Loads Y Counter with data for absolute position operation.
LDIS-0	9-1;9-2	Load Displacement Counter. Enables displacement counter parallel load.
LDX-0	8-2;9-3	Load X Registers. X vector data is on data lines.
LDY-0	9-1;9-4	Load Y Registers. Y vector data is on data lines and start vector set up.
LOCK-0	3-1;3-1	Lock. If LOCK is low, it indicates that other system bus masters may not take control of the bus from the Processor board. This signal is manipulated by a "lock" prefix to any firmware instruction.
LS0-2	3-2; 3-3,3-5	Latched Status 0 through 2. These signals are the latched outputs of the MPU S0--S2 signals. S0--S2 indicate what state the MPU is in-- interrupt acknowledge, read IO, write IO, halt, code access, read memory, or write memory.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
LSF-1	9-1;9-2	Load Scale Factor. Clocks Scale Factor Latch.
LTCH-1	9-1;9-3,-4	Latch. Enables X and Y Latches.
LVSD-0	8-2;9-2	Load Vector Scaling Data. Latches scaling data through Scaling Buffer Register.
MAKECOPY-0	8-2;HCU	Make a Copy. Caused by Display Controller or Hard Copy Key going low. Initiates a hard copy cycle (makes a copy). Requires ground closure of TTL low for more than 1 ms.
MCLK-0	9-1;9-3,-4	Multiplier Clock. Rate Multiplier clock signal.
MCLR-0	9-2;9-3,-4	Multiplier Clear. Clears X and Y Rate Multipliers.
MDEN-1	J104; 3-3	Memory Data Enable. When driven low, this signal disables data drivers on the Processor board.
MRDC-0	3-2; 3-1,P101	Memory Read Command. MRDC instructs memory to release data to the system bus.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
MWTC-0	3-2; P101	Memory Write Command. This signal indicates that memory should latch and store data on the system bus.
MX0-11	9-3;9-3	Multiplier X Axis Data. Latched data to X Rate Multiplier.
MY0-11	9-4;9-4	Multiplier Y Axis Data. Latched data to Y Rate Multiplier.
NMI-0	J104; 3-1	Non-Maskable Interrupt. This is the non-maskable interrupt for the MPU microprocessor. The 4114 system does not use it, but it is available for use by a test device via J104.
NMI-1	3-1;J104	Non-Maskable Interrupt. This is NMI-0 inverted.
NON-STORE-0	9-2;18-2	Non-Store. When low, causes reduced target voltage; permits the crt writing beam to write without storing. (Not used in 4114.)
OBADR-0	3-3; 3-1,3-2	On-Board Address. OBADR indicates that the MPU microprocessor is accessing a device on the Processor board.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
OBDEN-0	3-3; 3-2	On-Board Data Enable. OBDEN enables the data transceivers during an on-board data access.
OBINTA-0	3-2; 3-1,3-3	On-Board Interrupt Acknowledge. OBINTA indicates that the PIC is generating an interrupt vector address.
OBIOX&X	3-3;3-1,-2, -4,-5	On-Board IO (Select) Signals. Local address lines A0,A2, and A3 select one of eight signals: OBIOD&F, OBIOC&D, OBIO9&B, OBIO8&A, OBIO5&7, OBIO4&6, OBIO1&3, and OBIO0&2. These are used to enable the RCI, PT&BRG, IC, KC, BTD, or SI blocks. These signals are selected during Processor board IO reads and writes to X'00E0' through X'00EF'.
OBRAM-0	3-3;3-4	On-Board RAM. OBRAM enables the CMOS RAM for a READ or WRITE operation.
OBROM-0	3-3;3-1	On-Board ROM. OBROM enables the 32K of ROM on the Processor board for READ operations.
OFFSET-0	9-3;9-4	Offset. Increases X DAC output current in Extend mode.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
ORIGIN-1	18-1;14-1	Origin. During erase cycle from Storage board, triggers the origin shift counter on the Deflection Amplifier board to shift the axes slightly on the next page of screen written data. Feature increases crt screen life.
OUT-0	6-1;5-2 6-1;7-2	Out. OUT is used with IN to indicate the presence or absence of a RAM Array board.
OUT0-1	3-5; 3-1	Output 0. OUT0 is the output of a 16-bit programmable down counter. This provides variable timing delays for the system firmware. In the BTD block, it clocks the bus timeout counter whose output to the system bus is ACK1.
PD-0,-1	9-5;9-5	Pump Down. X axis current switch signal.
PL-0,-1	9-5;9-5	Pump Left. Y axis current switch signal.
PR-0,-1	9-5;9-5	Pump Right. Y axis current switch signal.
PU-0,-1	9-5;9-5	Pump Up. X axis current switch signal.
QS1-2	3-1;J104	Queue Status 1 and 2. QS1--2 are direct outputs of the MPU that are not used on the Processor board.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
RA0-6	5-1;5-1 7-1;7-2	RAM Address Bits 0 through 6. These signals contain the seven multiplexed row and column addresses from the DRC to the dynamic RAMs on the RAM Array board.
RAMWRITE-0	5-1;5-2	RAM Write. RAMWRITE indicates to the DRC and the data input receivers on the RAM/ROM board that a RAM write operation has been requested.
RAS-0	5-1;5-2	Row Address Strobe. RAS is generated by the DRC on the RAM/ROM board. RAS strobes the seven multi-plexed row address bits appearing on RA0-6 into the RAMs on the RAM Array board.
RAS0-3	7-1;7-2	Row Address Strobe 0 through 3. These signals are generated by the DRC on the RAM Controller board. RAS0-3 strobe the seven multiplexed row address bits appearing on RA0-6 into the RAMs on the appropriate RAM Array board (RAM Bank 0 through 3).
RCLK-1	P102;3-5	Receive Clock. RCLK is an RS-232 external clock signal generated by a modem or other external device. RCLK can be used to clock data into the Processor board's UART.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
RD-0	3-1; 3-2,3-4, 3-5	Read. If RD is low, it indicates the the MPU is performing an IO or memory read cycle, either to the local or system bus.
RDATA-1	P102; 3-5,	Receive Data. RDATA is the RS-232 serial data input from a modem or other external device to the Processor board.
RDY-1	J104;3-1	Ready. RDY is the MPU RDY signal output to test connector J104.
RDYAND-0	J104; 3-1	Ready And. RDYAND is an input from a test device connected to J104 that can disable the RDY line to the MPU, causing the MPU to enter a WAIT state.
RDYOR-0	J104; 3-1	Ready Or. RDYOR is an input from a test device connected to J104 that can activate the RDY line to the MPU, causing the MPU to exit a WAIT state.
READ-0	5-1;5-3	Read. READ is the buffered version of the system bus signal MRDC.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
READ-0	HCU;18-1,14-1	Read. Develops HCS-0 and HCS-1 in the copy control section. READ-0 causes the channel shift and origin shift to use the the SLOW and FAST RAMP signals (also from the HCU) to provide LA and SA outputs from the Deflecton Amplifier.
RELX-0,-1	9-1;9-1	Relative X Axis. The vector operation is relative in the X axis.
RELY-0,-1	9-1;9-1	Relative Y Axis. The vector operation is relative in the Y axis.
REMOTE COPY-0	8-2;HCU	Remote Copy. Caused by Display Controller switch going low. Initiates a hard copy cycle (makes a copy). A direct line from the MAKE COPY-0 signal, which acts as a reference for the Hard Copy Unit. Informs the HCU that it is being triggered from a source remote to the HCU.
RING-1	P102 ;3-5	Ring. RING is an RS-232 status input indicating that an auto-answering modem is ringing.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
ROMREAD-1	5-3;5-1	ROM Read. ROMREAD indicates that a ROM read operation is in progress. This signal is used to generate an acknowledge signal (ACK1 or ACK2) to the bus master.
RQ-0/GT[0/1]	3-1; J104	Request/Grant. RQ/GT0 is the local MPU bus request/grant signal. It is available to J104 test connector, but is not used on-board.
RSCNT-0	9-1;9-2	Reset Count. Clears completion shift register for new shift data.
RST-0	3-1; 3-2,3-4, 3-5	Reset. RST-0 is RST-1 inverted.
RST-1	3-1; 3-2,3-4, 3-5	Reset. RST is derived from the system bus signal INIT and is synchronized to the MPU clock. RST resets the MPU and other devices on the Processor board.
RTS-1	3-5;P102	Request To Send. RTS is an RS-232 signal generated by the RCI block on the Processor board.
RXSGN-0	9-1;9-3	Reset X Sign. Clears X sign bit between vectors.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
S0-2	3-1; 3-2	Status 0 through 2. These status lines have eight states taken together and indicate whether an interrupt acknowledge read IO, write IO, halt, code access, read memory, or write memory is occurring. The bus controller IC in the BCD block interprets the S0, S1, and S2 signals and outputs INTA, IOWC, AIOWC, IORC, MRDC, MWTC, AMWC.
S7-1/BHE-0	3-1; 3-2	Status 7/Byte High Enable. This signal is interpreted as BHE during the MPU state T1. It enables D8--D15 onto the local data bus. During T2, T3, or T4 this signal is interpreted as S7.
SCAL-0	8-3;9-1	Scale Enable. Enables the vector scaling logic.
SDCD-1	P102; 3-5	Secondary Data Carrier Detect. SDCD is the RS-232 secondary data carrier detect signal.
SHEN-1	9-1;9-3,-4	Shift Enable. Enables the X and Y Shift Registers.
SHFTX-1	9-1;9-3	Shift X Axis. Shifts X data.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
SHFTY-1	9-1;9-2,-4	Shift Y Axis. Shifts Y data.
SLOW RAMP	HCU;14-1	Slow Ramp. Analog deflection voltage from the HCU which controls the horizontal deflection during the hard copy scan. (There are "+" and "-"SLOW RAMPs on the schematics.)
SLU-0	14-2;8-3,-4	Slew. Indicates a temporary wait for the display controller while the deflection circuits are lagging the deflection inputs and establishing the new deflection position.
SRTS(A)-1	3-5; P102	Secondary Request To Send (RS-232A). SRTS(A) is the RS-232A secondary request to send output. SRTS is defined on a different connector pin for RS-232C, and so is strappable on the board.
SRTS(C)-1	3-5;P102	Secondary Request To Send (RS-232C). SRTS(C) is the RS-232C counterpart to SRTS(A) above.
STATEN-0	3-5; 3-1	Status Enable. STATEN is low during an MPU read of status at IO location X'00ED' or X'00EF'.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
STEPX-0	9-1;9-2,-3	Step X Axis. Clocks X Counter to set character spacing.
STEST-0	P101;3-5	Self Test. STEST is a line on the system bus which the Processor can read via a 3-state driver. The line is low when the self-test button is pressed.
SVECT-0	8-2;9-1,-3	Short Vector. Data is in short vector format (during vector data transfer).
SVECT-1	8-2;8-4	Short Vector. Data is in short vector format (during vector data transfer).
T3W4-1	3-1; 3-3	(State) T3, Wait, 4. T3W4 is high when the MPU is in a T3, T4, or TW (WAIT) state. T3W4 enables on-board data transceivers.
T4I-0	3-1; 3-3	(State) T4, Idle. T4I is low during MPU T4 and TI (idle) states. It turns off data transceivers during T4 in on-board memory and IO READs.
TARGET	18-2;19-1	Target. Voltage established at the inside face (screen) of the crt.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
TARSIG-0	19-1;HCU	Target. Display information signal from the target sent to the HCU when a hard copy is being made. Goes low when the scan crosses a written area on the crt screen.
TCLK-1	P102; 3-5	Transmit Clock. TCLK is the RS-232 transmit clock output from the Processor board.
TDATA-1	3-5;P102	Transmitted Data. TDATA is the RS-232 signal on which serial data is transmitted from the Processor board.
TEST-0	J104;3-1	Test. TEST is an input to the MPU Processor. It is available at Pin 50 on the test connector, but is not used on-board.
TEST-1	3-5; 3-1	Test. TEST is a signal that the processor can set to enable the Clock Generator to locally terminate an on-board or off-board READ or WRITE operation. The signal is used for testing purposes, and is similar in function to the BTD circuit.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
TIMERINT-0	3-5; 3-2	Timer Interrupt. TIMERINT indicates the presence of either a PIT timer1 interrupt, a UART TXEMT interrupt, a UART TXRDY interrupt, an RS-232 status change interrupt, or an PIT TIMER0 interrupt (via RSCD).
TIMR1-1	3-5; 3-1	Timer 1. This signal is output from the O1 pin of the PIT. O1 is the output of a 16-bit programmable down counter.
TRU Z	17-1;18-1, 14-2	True Z (axis). Represents the true Z-Axis (always active high). Turns on crt writing beam depending on the status of the intensity control logic section. Overrides Antiburn circuitry in the first few microseconds of operation, due to the time lag of the Antiburn circuitry, so as not to blank out any beginning information. (See also Z AXIS signal definition.)
TXC-0	3-5; P102	Transmit Clock. TXC is the buffered output of the PIT timer1 to RS-232 connector. It is not presently used.
UBCLK-1	3-1;3-4,3-5	Unbuffered Bus Clock. UBCLK is a 4.9152 MHz square wave clock provided to clock the UART and PIMPU.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
ULBHEN-0	3-1; 3-2	Unlatched Byte High Enable. ULBHEN is an MPU output. See BHEN for a description of this signal.
VAVIL-1	9-1;8-2,9-4	Vector Available. Vector data is available to vector set-up logic but has not yet been completely processed.
VCLK-0,-1	9-1;9-2,-5	Vector Clock. 12 MHz clock signal.
VCLKA-1	9-1;9-5	Vector Clock A. 12 MHz clock signal.
VCOMP-1	9-2;9-2	Vector Completed. Completion Counter has detected end of vector.
VIEW-0	8-1;18-1	View. Resets the view erase counters. (GBUSY or Z-AXIS will also do this, depending on the placement of the view reset strap).
VSTRT-0	9-1;8-4	Vector Start. Vector generation has started.
VSTRT-1	8-4;8-2	Vector Start. Vector generation has started.
WAIT-0	HCU;18-1	Wait. Remains low until the display screen has been scanned. (Applies only to a hard copy unit with multiplexer option.)

SIGNAL	SOURCE; DESTINATION	EXPLANATION
WELSB-0	5-1;5-2 7-1;7-2	Write Enable Least Significant Byte. WELSB is a control strobe to the RAM Array board indicating that a write operation to the least significant byte of RAM is in progress.
WEMSB-0	5-1;5-2 7-1;7-2	Write Enable Most Significant Byte. WEMSB is a control strobe to the RAM Array board indicating that a write operation to the most significant byte of RAM is in progress.
WRITETHRU-0	8-4;17-1	Write Thru. Selects WRITE-THRU INTENSITY CONTROL (R227-Coarse Write Thru) and disables NORMAL and BRITE INTENSITY controls.
WT INTENSITY	15-1;17-1	Write-Thru Intensity. Controls the WRITE-THRU INTENSITY by R227 adjustment (see WRITE-THRU-0).
X+	9-5;14-1	X (axis). X-axis input to monitor. (Written +X and -X on schematics.)
X0-11	9-4;9-5	X DAC Input Data Bits. Scissored data to X DAC.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
XACK-0	5-1;5-2 7-1;7-2	Transfer Acknowledge. The DRC generates XACK to acknowledge that a RAM read or write operation is in progress. This signal latches the RAM output data into the Data Output Latches.
XCLK-0	P129;5-1 P166;7-1	External Clock. When the Clock circuitry is disabled using CLKDIS , an external TTL clock signal may be fed into XCLK to control the DRC. (This is a test point for factory use only.)
XE-1	9-3;9-5	X Enable. Enables X Decoder gates.
XS-0	9-3;9-5	X Sign. Sets X vector directions.
XTRA-1	6-1;none	Extra. EXTRA is an extra line of the RAM Array board that is currently not used. It may be used in the future.
Y+	9-5;14-1	Y (Axis). Y axis input to the monitor. (There are "+" and "-"Y axis signals on the schematics.)
YO-11	9-4;9-5	Y DAC Input Data. Scissored data for Y DAC.
YE-1	9-4;9-5	Y Enable. Enables Y Decoder gates.

SIGNAL	SOURCE; DESTINATION	EXPLANATION
YS-1	9-4;9-5	Y Sign. Sets y vector direction.
Z-AXIS	9-5;18-1,17-1	Z-axis. True signal turns on the crt writing beam depending upon the status of the intensity control logic section. Also can be strapped to accept either TTL state (high or low) input signal.
ZOUT-1	9-5;9-1	Z Axis Output. CRT beam current control.
ZVECT-0	9-2;9-1	Zero Length Vector. Indicates vector length is zero.

Appendix B

OPTIONS

INTRODUCTION TO RAM CONTROLLER BOARD THEORY

The RAM Controller circuit theory describes the general architecture and operation of the RAM Controller board in its entirety first, and then describes each block of circuitry. The order of description of the blocks follows the basic information flow, from left to right, of the block diagram. Refer to the RAM Controller Board Block Diagram, Figure B-1.

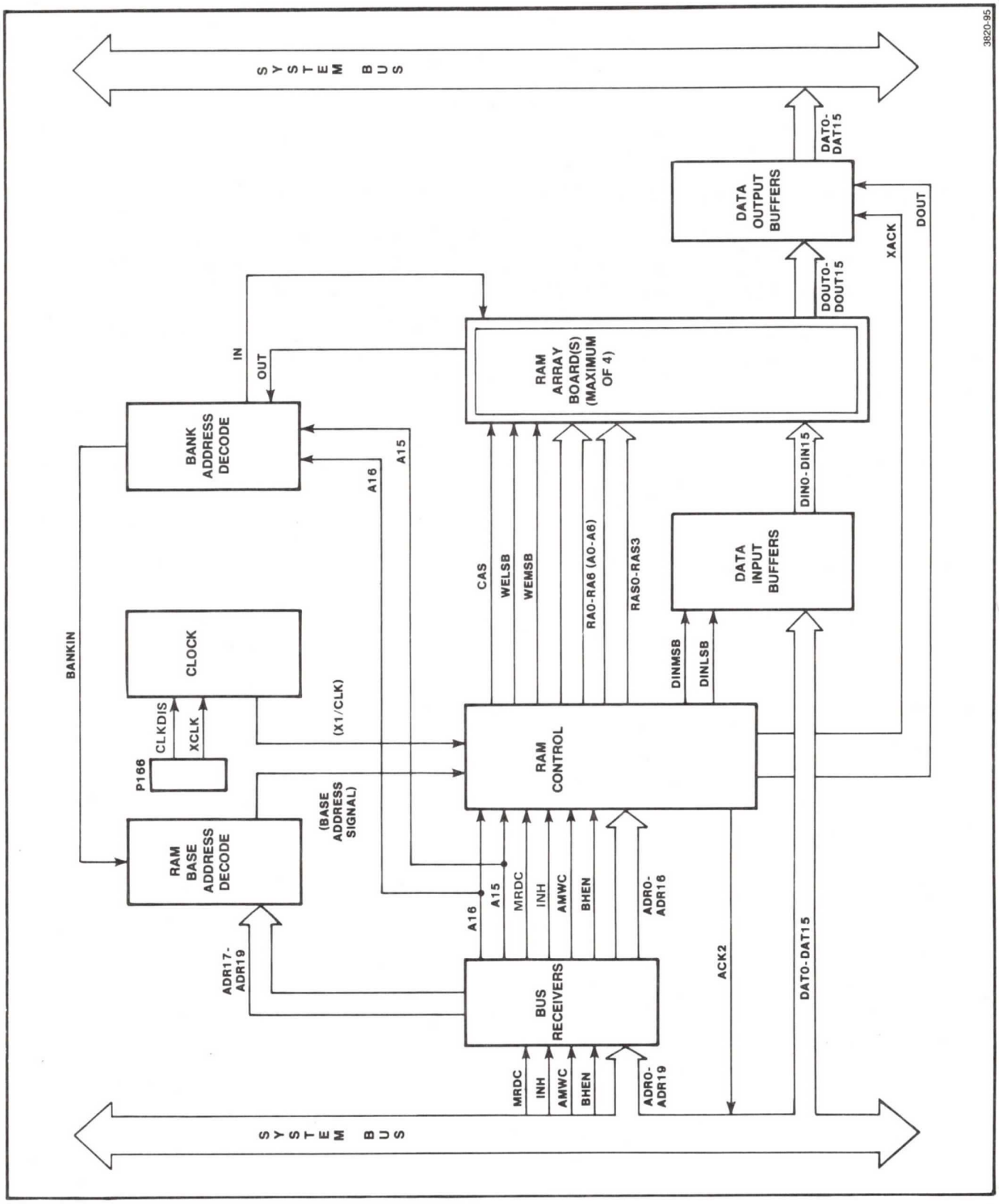


Figure B-1. RAM Controller Board Block Diagram.

GENERAL DESCRIPTION

This board supplies the optional system RAM memory that the Processor board and other bus masters use.

It consists of a dynamic RAM controller (with support circuitry), in addition to four sockets where up to four RAM Array boards plug in. (RAM Array boards are small circuit boards that hold 32K bytes of dynamic RAMs.) See Figure B-2.

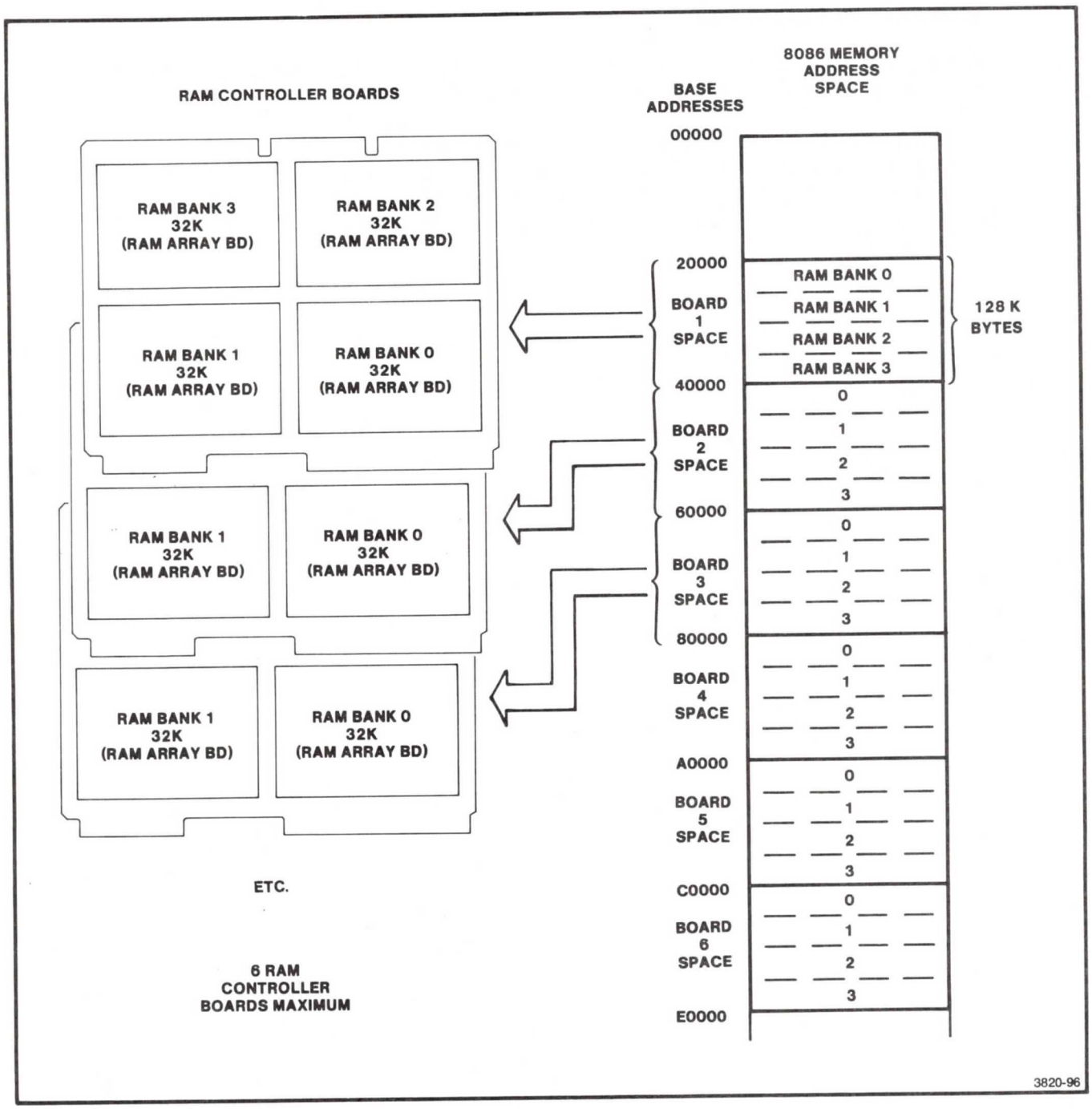


Figure B-2. RAM Controller Boards and Memory Address Space.

GENERAL OPERATION

Two basic operations are performed by the RAM Controller: reading the contents of a location in RAM and writing over the contents of a location in RAM.

To read the contents of a location in RAM, the bus master first places the location address on the system bus, and then MRDC (Memory Read Command). When the RAM Controller board receives an active MRDC signal, it responds by driving ACK2 (Acknowledge 2) onto the bus, and then the data from the addressed location.

To write to a location in RAM, the same sequence of events occurs except that AMWC (Advanced Memory Write Command) is enabled instead of MRDC and the bus master drives the data onto the bus.

BUS RECEIVERS

(See Schematic A7-1.)

Purpose

This circuitry receives signals from the system bus and buffers them for the board.

Signals

The input signals are:

- MRDC (Memory Read Command). This is the system bus memory read signal.
- INH (Inhibit). This signal prevents the board from outputing data to the system bus.
- AMWC (Advanced Memory Write Command). This is the system bus advanced memory write signal.
- BHEN (Byte High Enable). During byte (8-bit) write operations, the RAM Controller board examines BHEN and ADR0 to determine which byte is to be written. If BHEN is true (low), the high byte (D8-15) is written. If ADR0 is false (low), the low byte (D0-7) is written.
- ADR0-19. System address lines.

The output signals for this circuitry are the same as the input signals above.

Operation

The three bus receivers are permanently enabled. This means that the outputs constantly follow whatever is on the system bus. The board responds when MRDC or AMWC is enabled and a valid address is on the system bus.

RAM CONTROL

(See Schematic A7-1.)

Purpose

This circuitry:

- Generates all control signals for the RAMs on the RAM Array board(s).
- Provides address multiplexing and address strobes for the RAM on the RAM Array board(s).
- Determines whether the RAM on the RAM Array board(s) will be in a read, write, or refresh cycle.
- Provides signals to latch data from RAM Array board(s) and place the data on the system bus.

Signals

The input signals are:

- MRDC (Memory Read Command). This signal enables system memory to output data to the system bus.
- INH (Inhibit). This prevents the Processor board from outputing data.
- AMWC (Advanced Memory Write Command). This signal gives early indication of a memory write on the system bus.
- BHEN (Byte High Enable). This signal enables the most significant byte of a 16-bit word of data to be output by itself.

- ADR0-16. (System bus address bits 0 through 16). ADR0-14 carry RAM address information. The 8202 Dynamic RAM Controller uses ADR15 and ADR16 to select which bank (RAM Array board) of RAM ADR0-14 will address.

- BDSELECT (Board Select). A signal that is active when memory on this RAM Controller board (out of a possible six) is addressed. A RAM Controller board places data on the system bus if this signal is active (low).

- CLK (Clock). This 22.008 MHz square wave TTL signal drives the clock (X1/CLK) input of the Dynamic RAM Controller.

The output signals are:

- DOUT (Data Out). DOUT outputs data to the system bus when low.

- ACK2 (Acknowledge 2). This signal acknowledges that the memory operation currently requested by the bus master has begun and will soon be completed. (See discussion of the system bus elsewhere.)

- DINLSB and DINMSB (Data Input Least Significant Bit and Most Significant Bit). These enable data from the system bus to be accepted by the Data Input Buffers. DINLSB enables DAT0-7 to be accepted and DINMSB enables DAT8-15 to be accepted.

- WELSB and WEMSB (Write Enable Least Significant Bit and Most Significant Bit). These strobe data into the RAMs on the RAM Array board(s).

- CAS (Column Address Strobe). CAS latches the column address into the RAMs on the Ram Array board(s).

- RA0-6 (RAM Address bits 0 through 6). Multiplexed system bus addresses ADR1-14.

- RAS0-3 (Row Address Strobe bits 0 through 3). These latch the row address into RAMs on the RAM Array board(s).

- XACK (Transfer Acknowledge). XACK latches data into the Data Output Latches.

Description

This circuitry consists primarily of the Dynamic RAM Controller (DRC). See Figure B-3.

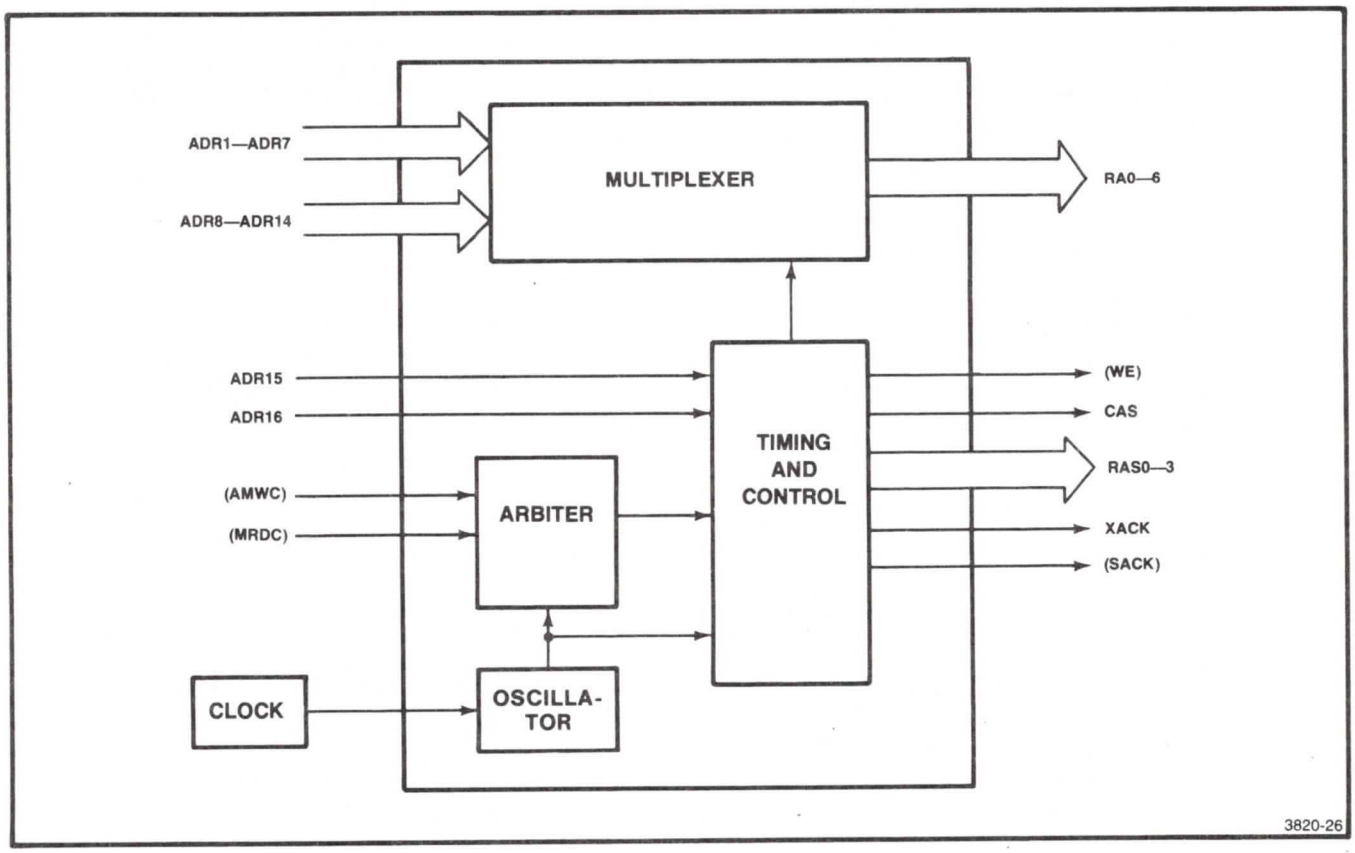


Figure B-3. Dynamic RAM Controller Block Diagram.

In addition to the DRC, there are some logic gates that combine related signals into new signals needed by the board. There are also two flip-flops that synchronize the timing of the read and write signals to the DRC clock signal (CLK).

The DRC combines all of the functions that are needed to operate dynamic RAM. These functions are: multiplexing 14 bits of address into two 7-bit parts, arbitrating among selecting a read, write, or refresh cycle, generating various timing and control signals. The DRC also has circuitry for the internal generation of refresh signals for the dynamic RAM on the RAM Array board.

Multiplexing of RAM Addresses

ADR1-14 are input to the multiplexer in the Dynamic RAM Controller. Because of the requirements of the 16K RAMs on the RAM Array board(s), ADR1-14 is split into a low and a high order word. ADR1-7 is output as a 7-bit row address and then ADR8-14 is output as a 7-bit column address. The low and high order words of ADR1-14 appear one after the other on the RA0-6 lines of the RAM Control circuitry.

Arbitration of Read, Write, and Refresh Cycles

The Arbiter circuitry in the DRC prevents requests for read or write cycles from interrupting read, write, or refresh cycles in current operation. Refresh cycles are generated internally in the Dynamic RAM Controller.

Generation of Timing and Control Signals

This block of circuitry has five functions:

- Executing a read, write, or refresh cycle at the request of the Arbiter circuitry.
- Generating CAS (Column Address Strobe), WE (Write Enable), and the RAS0-3 (Row Address Strobes).
- Generating XACK and SACK, the transfer and system acknowledge signals.
- Sending internal control signals to the multiplexer circuitry in the DRC.
- Resetting an internal refresh timer and incrementing an internal refresh counter.

Clock

The Clock circuitry on the board feeds a 22.008 MHz square wave to the DRC. This square wave provides the timing for the Multiplexer, Arbiter, and Timing and Control circuitry in the DRC.

Operation

The Dynamic RAM Controller performs these operations:

- Idling
- Write cycle
- Read cycle
- Refresh cycle

Idling

The Arbiter logic in the DRC monitors requests for read, write and refresh cycles. Read and write requests originate from the system bus, but refresh requests all originate internally to the DRC.

The DRC is in the idle state when no requests are currently being processed and no cycles are in progress. Read cycles are initiated if MRDC is active low when requests are sampled. Write cycles are initiated if AMWC is active low when requests are sampled. If a read or write cycle is requested simultaneously with a refresh cycle, the read or write cycle is executed before the refresh cycle.

Write Cycle

The steps of a write cycle occur in the following order:

1) The Multiplexer drives RA0-6 with the low order address.

2) SACK is activated.

3) The appropriate RAS0-3 signal strobes the low order row address into the RAM.

4) The Multiplexer drives RA0-6 with the high order address.

5) WE is activated.

6) CAS strobes the high order column address into the RAM.

7) XACK is activated.

8) All signals are deactivated and the DRC enters the idling state.

Read Cycle

The read and write cycles are identical except that WE is not activated during a read cycle.

Refresh Cycle

When a refresh cycle is internally requested, the Multiplexer drives RA0-6 with a refresh address contained in an internal refresh counter. RAS0-3 are all simultaneously activated causing a refresh cycle to occur on all RAM Array boards. After some internal operations, the DRC enters the idling state again.

DATA INPUT BUFFERS

(See Schematic A7-2.)

Purpose

Receives data signals from the system bus and buffers them for the RAM Array board(s).

Signals

The input signals are:

- DAT0-15 (System Data bits 0 through 15). DAT0-15 carry 16 bits of data on the system bus.
- DINLSB and DINMSB (Data Input Leas Significant Bit and Data Input Most Significant Bit). These enable data from the system bus to be accepted by the data buffers. DINLSB enables DAT0-7 to be accepted and DINMSB enables DAT8-15 to be accepted.

The output signals are:

- DIN0-15 (Data Input bits 0 through 15). These are the buffered version of DAT0-15.

Operation

Whenever a write operation is requested and ADR0 is active low on the system bus, the RAM Control logic generates DINLSB. This enables the least significant byte (DAT0-7) of data to be transmitted to the RAM Array board(s). And whenever a write operation is requested and BHEN is active low on the system bus, the RAM Control circuitry generates DINMSB. This enables the most significant byte (DAT8-15) of data to be transmitted to the RAM Array board(s).

RAM ARRAY BOARD(S)

(See Schematic A6-1.)

Purpose

Contains 32K bytes of system dynamic RAMs.

Signals

The input signals are:

- CAS (Column Address Strobe). CAS latches the column address into the RAMs.
- WELSB and WEMSB (Write Enable Least Significant Bit and Write Enable Most Significant Bit). These strobe data into the RAMs.
- RA0-6 (RAM Address bits 0 through 6). These are multiplexed system bus addresses ADR1-14.
- RAS0-3 (Row Address Strobe). These latch the row address into the RAMs.
- DIN0-15 (Data Input bits 0 through 15.) These are the buffered version of DAT0-15.
- IN ((RAM Array board) In). IN indicates the presence of a RAM Array board. It works in conjunction with OUT.

The output signals are:

- DOUT0-15 (Data Output bits 0 through 15). These carry data to the Data Out Buffers.
- OUT ((RAM Array board) Out). OUT indicates the presence of a RAM Array board. It works in conjunction with IN.

Description

The RAM Array board is a small circuit board that contains 32K bytes of dynamic RAMs. A maximum of four RAM Array boards plug into sockets on the RAM Controller board.

The 32K bytes of RAM are arranged in two banks on the board. One bank handles the least significant byte of a 16-bit word, and the other bank handles the most significant byte of a 16-bit word. Since the RAMs are 16K by one bit wide, there are eight RAMs in each bank.

The RAM address lines RA0-6 connect to both the LSB and MSB banks. RAS and CAS connect to both banks, but there are separate write enable signals (WELSB and WEMSB) that allow the accessing of the high and low bytes of the 16-bit word.

Operation

The RAM Array board responds to the signals generated by the RAM Controller circuitry. See the RAM Controller for a description of accessing data on the RAM Array board.

DATA OUTPUT LATCHES

(See Schematic A7-2.)

Purpose

Data Output Latches accepts data from the RAM Array board and buffers it for the system bus.

Signals

The input signals are:

- XACK. This signal latches data (DOUT0-15) into the latches.
- DOUT. This outputs data (DAT0-15) onto the system bus.
- DOUT0-15. DOUT0-15 carry data output from the RAM Array board(s).

The output signals are:

- DAT0-15. These signals carry data on the system bus.

Operation

When XACK goes active low, data on DOUT0-15 is latched into the flip-flops in each of two D-type latches. When DOUT goes active low, the data is driven onto the system data bus lines DAT0-15.

RAM BASE ADDRESS DECODE

(See Schematic A7-1.)

Purpose

RAM Base Address Decode informs the RAM Control logic that a particular RAM Controller board has been addressed.

Signals

The input signals are:

- ADR17-19. These signals carry an address that falls within one of six possible ranges--each range corresponding to one of a maximum of six RAM Controller boards.
- BANKIN. BANKIN indicates that the RAM bank being addressed is present on this RAM Controller board.

The output signals are:

- BDSELECT. This signal indicates that this particular RAM Controller board is being selected by the address on the system bus.

Operation

This circuitry consists of one 3-to-8 decoder. ADR17-19 carry one of eight possible addresses of which only six correspond to one of six ranges of addresses in system RAM. If BANKIN is active low and ADR17-19 carry a valid address, the decoder pulls one of its six strappable pins low. If the correct decoder output pin is strapped, this circuitry asserts BDSELECT.

CLOCK

(See Schematic A7-1.)

Purpose

Clock generates a 22.008 MHz square wave that directly feeds the X1/CLK input of the Dynamic RAM Controller in the RAM Control circuitry.

Signals

The input signals are:

- CLKDIS (Clock Disable). CLKDIS prevents the clock from outputting its signal (used for test purposes only.)
- XCLK (External Clock). An external clock signal may be connected to this line. (Used for test purposes only.)

The output signals are:

- CLK (Clock). This is a 22.008 MHz square wave that drives the Dynamic RAM Controller.

Operation

Two NAND gates are biased into their linear region of operation by 820 ohm feedback resistors. In this mode of operation, the NAND gates act as linear inverting amplifiers. A series tank circuit and a 22.008 MHz crystal are connected in a loop with the two gate amplifiers. This causes the circuit to oscillate at 22.008. MHz. The output is connected to the X1/CLK input of the DRC. The output also clocks two flip-flops in the RAM Control circuitry.

BANK ADDRESS DECODE

(See Schematic 7-2.)

Purpose

Bank Address Decode produces a signal that indicates whether the RAM Array board being addressed is plugged into the RAM Controller board.

Signals

The input signals are:

- A15 and A16 (Local address bits 15 and 16). These signals carry an address for one of four possible RAM Array boards.
- OUT. OUT shows whether the RAM Array board being addressed is plugged into the RAM Controller board.

The output signals are:

- IN. This signal connects directly to OUT through the RAM Array board. See OUT above.
- BANKIN. BANKIN indicates that the RAM Array board being addressed is plugged into the RAM Controller board.

Operation

A15 and A16 can address any one of four RAM Array boards. The Bank Address Decode logic contains a 2-to-4 line decoder that responds to the address placed on its inputs by A15 and A16. If the RAM Array board corresponding to a received address is plugged in, IN is connected to OUT through the board and BANKIN goes active low.

Appendix C

STRAP INFORMATION

The terminal has straps on the various circuit boards, which provide flexibility in its operating parameters. There are two kinds of straps: cut straps and jumper straps. In cases where the terminal was designed to function one way, but provisions were made for future design enhancements, cut straps are often used. Cut straps are also used for straps that are changed infrequently. Jumper straps, however, are changed much more often than cut straps. Most straps in the terminal are jumper straps.

This summary gives the strap settings for each standard circuit board or module in the terminal.

PROCESSOR BOARD STRAPS

Several cut and jumper straps are provided on the Processor board. Straps labeled "Jxxx" have square pins with movable jumpers. Straps labeled "Wxxx" are cut straps; they consist of circuit traces on layer 1 of the ECB with no square pins. Table C-1 lists these strap settings.

Table C-1

PROCESSOR BOARD STRAP SETTINGS

Strap Label	Definition
ROM Logic Straps:	
ROM Size Strap (W126)	Selects either 16K bit or 32K bit ROMs, or disable all Processor board ROMs.
ROM Wait States (W475)	Normally strapped for ONE wait state. If all the ROMs on the Processor board are fast enough, this strap may be changed to indicate ZERO wait states.
ROM Type Straps (J226, J326, J426, (J427)	There is one set of straps for each two-ROM bank of ROMs. These straps configure the board for the pin-out of the ROM being used.
BLCK Source: (W455, W456)	Normally strapped to "on-board." If more than one Processor board is used in the system, only one should be strapped to "on-board;" all others should be strapped to "off-board."
Interrupt Level Straps: (W470)	The Processor can generate three different interrupts to the 8086 bus. These straps define the interrupt priority levels of the three different interrupts. Normally, the "host port receiver interrupts" are set to interrupt level 0, "keyboard interrupts" set to level 4, and "host port transmitter" are set to interrupt level 5.

Table C-1 (cont)

PROCESSOR BOARD STRAP SETTINGS

Strap Label	Definition
Bus Timout Enable: (W561)	Prevents the Processor board from driving ACK1-0 on a bus timeout. Used for multi-Processor board systems.
Test 1 and Test 2 (J150 and J125)	Tests 1 and 2 disable clocks on the Processor board for ATE (automated test equipment) testing.
RS-232-C/RS-232-A: (J522)	This is normally set for RS-232-C. When restrapped for RS-232-A, the SRTS (Secondary Request To Send) signal is sent to Pin 11 of the 25-pin RS-232 connector rather than to Pin 19.

KEYBOARD STRAPS

The Keyboard has a set of cut straps that allows the firmware to interpret key strokes according to languages other than English. This strap consists of four indidvidual cut straps labeled W1 through W4. The combinations of these straps are read as one hexadecimal number which corresponds to certain keyboard options. See Table C-2.

Table C-2

KEYBOARD LANGUAGE OPTION STRAPS

Language	Option Number	Open Cut Strap	Hex Code
Standard	--	none	00
United Kingdom	4A	W4	08
Swedish	4C	W2	02
APL	4E	W1	01
Danish/Norwegian	4F	W2 & W3	06

RAM/ROM AND RAM BOARD CONTROLLER STRAPS

To install optional RAM memory, one or more RAM Controller boards must be installed in the card-cage. Each RAM Controller board has sockets for four RAM Array boards. The RAM Array boards contain 32K-byte banks of memory. Since six RAM Controller boards can be installed in the terminal, it is necessary to specify the starting address of the four RAM banks on each RAM Controller board.

Strap J165 sets the Base Address for all memory on the board. Set the strap to "1," for the RAM Controller nearest the processor. Set the strap on the other RAM Controller boards to "2", "3", "4", etc., as they are placed in order farther away from the Processor board. Strap J165 allows strapping for a maximum of six RAM Controller boards.

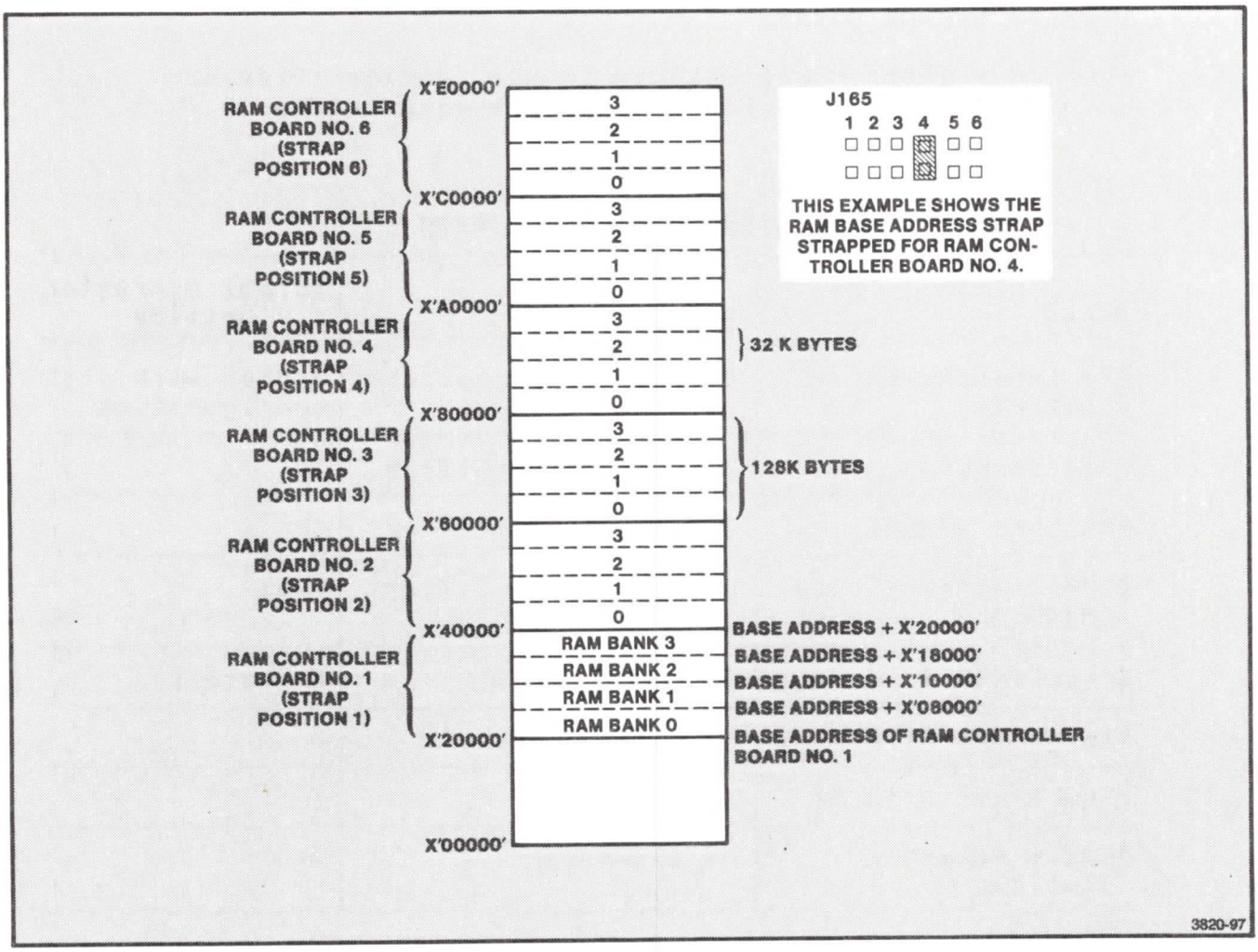


Figure C-1. Strapping RAM Controller Board Base Address.

DISPLAY MODULE STRAPS

There are eight strap options in the terminal display module. They are located on the following boards.

Table C-3

DISPLAY MODULE STRAPS

Strap	Board	Normal Operation Setting
X-Y Interchange Polarity	Deflection Amplifier	Varies with crt configuration
Hold IN/OUT	Deflection Amplifier	IN
Antiburn IN/OUT	Deflection Amplifier	IN
SLU-0 recovery time FAST/SLO	Deflection Amplifier	FAST
Erase TEST/N	Storage	N (normal)
View Reset Z/TRUZ	Storage	Z
View Reset Z/GBUSY	Storage	Z
Z Axis Polarity Z-1/Z-0	HV & Z Axis	Z-0

Five of the eight strap options are used to match the operational requirements of the pedestal. These are preset and are not changed during normal use. They are:

- Z Axis input polarity on the High Voltage and Z Axis board for selecting the Z-Axis polarity.
- View Reset on the Storage board for selecting the signal line TRU-Z or GB to reset the View Timer Control.
- Hold mode control on the Deflection Amplifier board for selecting between active and inactive Amplifier inputs during Hold mode.
- Antiburn on the Deflection Amplifier board selects between active and inactive beam intensity control during periods of little or no writing beam movement.
- Fast/Slo on the Deflection Amplifier board selects between SLU-0 fast or slow recovery time.

The factory setting for each of the options is as follows: Z-Axis Polarity, Z-0; View Reset, Z; Hold, IN; Antiburn, IN; SLU-0 recovery time, FAST.

The following is a detailed description of the display module straps.

X and Y Input Interchange (Deflection Amplifier Board)

These straps are used when the crt needs to be rotated 180 degrees due to aging crt phosphors. See "Rotating the CRT 180 degrees" in Section 11 (Maintenence). Altering these straps interchanges the +,-X and +,-Y deflection inputs, which causes the crt to write in a different direction. The normal writing pattern is from left to right across the screen, and from top to bottom down the screen.

Selecting Hold IN/OUT (Deflection Amplifier Board)

This strap connects the deflection inputs while in Hold mode either to ground or to the Deflection Amplifier board input connectors. In the IN position, when the display enters Hold mode, the deflection inputs are connected to ground. This centers the deflection amplifier again and minimizes the amplifier power dissipation. In the OUT position, when the display enters Hold mode, the deflection inputs remain directly connected to the deflection amplifier input connectors.

Selecting Antiburn IN/OUT (Deflection Amplifier Board)

Antiburn protects the crt from slow-moving, high-intensity beams. In the IN position, the antiburn amplifier controls the beam intensity. In the OUT position, there is no antiburn control and a slow-moving, high-intensity beam may damage the crt.

WARNING

This strap is always factory preset to the IN position. To avoid possible crt damage, it should not be set to the OUT position except for the adjustment of the display module.

Selecting FAST/SLO (Deflection Amplifier Board)

This strap option is used for a setting of SLU fast or slow recovery time. In the FAST position, the SLU signal provides only enough time for the settling of the deflection amplifier. In the SLO position, the SLU time is increased which provides additional settling time.

The display module is designed to be compatible with the pedestal with the FAST/SLO signal set in the FAST position. THIS SETTING SHOULD NOT BE MOVED.

Selecting N/TEST (Storage Board)

This strap is used only during display adjustment and should be left in the N position for normal operation. TEST will cause the crt to erase approximatrly every three seconds.

Selecting Z Reset Select (Storage Board)

This strap chooses the TRU-Z signal or a transition signal on the GBUSY signal line (GB) to reset the view counter. Resetting the view counter prevents the display module from going into Hold mode and ultimately into Auto Erase mode. In the TRU-Z position, each Z Axis positive transition resets the view counter, while in the GB position, any positive transition (from either a positive or negative pulse) of the GBUSY-0 signal line resets the view counter. An additional signal line, VIEW-0, also controls the view counter. A low on the VIEW-0 signal line always resets the view counter.

Selecting Z Axis Input Polarity (HV & Z Axis Board)

The display module is designed to accept either a low or high true TTL signal. To accomplish this, a set of two straps--labeled Z-1 and Z-0--on the High Voltage and Z Axis board is set to choose which true level of Z is used by the display control. If a low true TTL signal is used for Z, the two straps must be set in the Z-0 position. The writing beam is then turned off when the Z Axis input signal rises to at least +2 V, and turns on with a signal of less than +0.8 V. Conversely, if a high true TTL signal is used for Z, the two straps must be set in the Z-1 position. The writing beam is then turned on when the Z Axis input signal rises to at least +2 V, and turns off with a signal of less than +.8 V.

CAUTION

The display module uses a factory setting of Z-0 in order to be compatible with the pedestal. THIS SETTING SHOULD NOT BE CHANGED.

VECTOR GENERATOR BOARD STRAPS

There is only one strap on the Vector Generator board. This is strap J601, which overrides the charge pump for troubleshooting purposes. The Vector Generator board has no jumper strap on J601 during normal use.

DISPLAY CONTROLLER BOARD STRAPS

The Display Controller board has two cut straps on it, W370 and W570.

W570 selects one of seven bus interrupt levels, 0 through 7. The factory setting is wired to the 6 position.

W370 has two possible positions that select for address decoding. The positions are 0 and 1. The 0 position selects addresses X'00D0' through X'00D7' for decoding, while the 1 position selects addresses X'00D8' through X'00DF' for decoding. The factory preset position is 0.

Appendix D

ASCII CHARTS

This appendix includes a standard ASCII code chart and additional ASCII code charts which define the specific characters used as parameters (indicated by unshaded areas).

The code charts are:

Table	Description
D-1	ASCII Code Chart
D-2	Characters Used in <Char> Parameters
D-3	Characters Used in <Int> and <Int+> Parameters
D-4	Characters Used in <Int-Report> Parameters
D-5	Characters Used in <Xy> Parameters
D-6	Characters Used in <Xy-Report> Parameters

Table D-1

ASCII (ISO-7-US) CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| * 124
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

* | on some keyboards or systems

Table D-2

CHARACTERS USED IN <CHAR> PARAMETERS

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
1 1 Ø 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

* | on some keyboards or systems

Table D-3

CHARACTERS USED IN <INT> AND <INT+> PARAMETERS

<Hil> Characters

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| * 124
1 1 Ø 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

* | on some keyboards or systems

<Lol> Characters

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| * 124
1 1 Ø 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

Table D-4

CHARACTERS USED IN <INT-REPORT> PARAMETERS

<Hil-Report> Characters

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

* | on some keyboards or systems

<Lol-Report> Characters

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

Table D-5

CHARACTERS USED IN <XY> PARAMETERS

<HiY>,<HiX> Characters

BITS B7 B6 B5 / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U	e	u
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V		
0 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W		
1 0 0 0	BS 8	CAN 24	(40	8 56	H 72	X		
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y		
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z		
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[		
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\		
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	]		
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^		
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_		

<LoY>,<Extra> Characters

BITS B7 B6 B5 / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} *25
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

*| on some keyboards or systems

<LoX> Characters

* 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
TROL	FIGURES		UPPERCASE		LOWERCASE	
DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
CAN 24	(40	8 56	H 72	X 88	h 104	x 120
EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
GS 29	- 45	= 61	M 77	] 93	m 109	} 125
RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

Table D-6

CHARACTERS USED IN <XY-REPORT> PARAMETERS

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL 7	ETB 23	/ 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	|* 124
1 1 Ø 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

* | on some keyboards or systems

APPENDIX E

SELF TEST DIAGNOSTIC PROGRAM

USING THE SELF-TEST PROGRAM

The primary troubleshooting aid for the 4114 is the Self Test diagnostic program. This program resides in firmware and is arranged so that it checks all hardware--starting with the initial error reporting mechanism (keyboard LEDs). Self Test, primarily, does not depend on any portion of the hardware until it has tested it; it may then use such hardware to aid in other tests.

A subset of Self Test is the Power Up sequence. The Power-Up sequence runs automatically when the terminal is turned on, and performs a quick check of the various hardware modules. If a major or fatal error is detected at this point, an error mesage advises the user (A major error is when the Setup Default (cmos) Reset option fails and is mapped out; when a fatal error occurs, the terminal will not run). The 4114 operators manual describes the error messages that may appear during the Power-Up sequence. For detailed diagnostic examination of terminal hardware, use Self Test. Self Test will perform additional tests as well as repeating the same tests that were done during the Power-Up sequence.

Start the program running by pressing the RESET and SELF-TEST buttons. Press and hold RESET and SELF-TEST. then release RESET. After the Keyboard LEDs have begun to "cycle", release SELF TEST.

The test begins by turning on all the keyboard lights ("CAPS LOCK" key, four function key LEDs, and four indicator LEDs). The CAPS key light should turn off immediately (while the other eight LEDs remain lit). If the CAPS key light remains lit, this indicates a major malfunction in the processor.

While Self Test is running, the eight keyboard lights blink as they ripple through the codes for the various tests. When a fatal error occurs during a particular test, its identifying light pattern starts blinking, and the bell rings three times. These lights are the binary equivalent of a hexidecimal value assigned to each major set of tests. These light codes are displayed on the eight indicator LEDs. The error message tables (in this section) list and define these error codes, giving an explanation for the error condition and suggesting which piece of circuitry malfunctioned. After the major error codes have been displayed, most problems can be narrowed down through the use of submessages. Submessages are displayed by first noting the major error codes, pressing RETURN, and noting the next set of lights displayed as the submessage. In some instances, there may be up to three levels of submessages.

After the display has been checked, most error messages are printed on the display screen. Such screen-displayed error messages first print the name of the test or the hardware module being tested. Then a submessage on the next line tells which part of the test failed.

If Self Test encounters a problem, which caused it to simply stop during a particular test, this results in the light pattern for that test remaining lit indefinitely. This type of problem is highly unlikely, but could be caused by a bad ROM. Read the error code on the lights and use this to help determine where the test is "hung up".

During the Delay Memory check (associated with table E-7, RAM Test Errors) there is a 14 second wait for each 32K of RAM being tested. In a fully loaded instrument (one with all RAM options attached) this test can take up to four minutes to run. Do not be suprised about this delay; it does not mean that Self Test is "hung". This lengthy test can be overriden by entering CONTROL D during the keyboard check.

In the following discussion, tests are grouped in modules according to the hardware being tested. Under each heading (test module name) is a short general description of the test and hardware it checks. Each table of error messages define those messages that may appear while that test is running. To determine which piece of circuitry malfunctioned, read the list of active circuits for each test. Since many circuits are used in several tests, eliminate as good those circuits that passed all previous tests. These tables are grouped together for referencing convienence rather than in the order in which the tests occur (see Table E-1). Tables start with the error code FE (1111 1110) and are listed in descending order of the binary codes.

Table E-10 lists the error codes and the order in which the tests are actually performed during Self Test.

Table E-1

SELF TEST ERRORS DIRECTORY

TEST MODULE	TABLE NUMBER
KEYBOARD/PROCESOR	E-2
PROCESSOR BOARD	E-3
RAM/BUS AND HOST PORT	E-4
SYSTEM/OPTION ROMS	E-6
RAM TEST	E-7
CMOS MEMORY	E-8
DISPLAY CONTROLLER, VECTOR GENERATOR, AND DISPLAY MODULE	E-9
SELF TEST OPTION ERRORS DIRECTORY	
3PPI (OPTION 10)	E-11
DISK (OPTION 42/43)	E-12
TABLET (OPTION 13/14)	E-13

Keyboard Check and Lights (F)

When Self Test starts, the indicator LEDs show FF (1111 1111). As the test continues the light pattern approach 00.

During the keyboard lights check, each light is slowly turned on and off in a sequential loop beginning with the keypad, going across the eight LEDs (right to left), and down to the CAPS key. This circling light pattern is then repeated quickly.

At the beginning of the keyboard keys test the 4114 rings the bell once, and the CAPS key light starts blinking. This prompts the user to press a key (any key) after waiting a few seconds. When the bell rings and the CAPS key blinks, the test is susposed to stop and wait for a key stroke. If the test proceeds without pressing a key, this means spurious key strokes are being generated. This type of problem could be caused by dirt or corrosion in the keyboard, or a poor connection in the keyboard-to-processor board ribbon cable. If the test waits for a key entry, then press a key, allowing the tests to continue. Figure E-1 shows the locations of the keyboard ROMs.

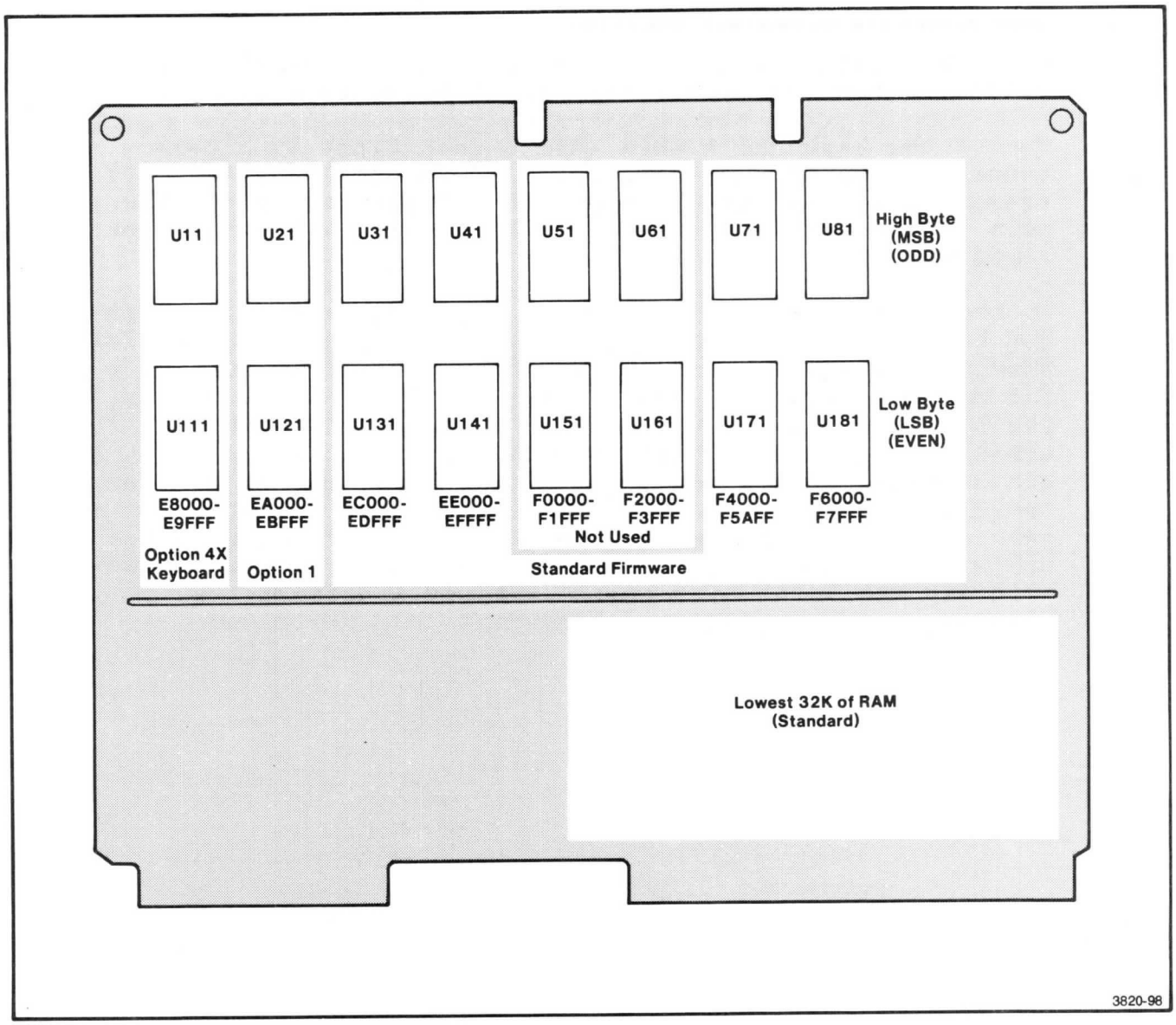


Figure E-1. RAM/ROM Board.

Table E-2

KEYBOARD/PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1111 1110	FE	Error at beginning of keyboard lights test. (Circling lights test happens here.)
1111 1101	FD	Error at end of keyboard lights test.
1111 1100	FC	Error during keyboard keys test.
1111 1010	FA	Error while loading Keyboard Identification Code.

Submessage: (printed on screen)

"Keybrd -ID XX"

XX will be the option number of the keyboard attached (example: a Swedish keyboard is option 4C). This test then checks the validity of that number against the ROM option number installed, and displays this message if the wrong ROMs or no ROMs (for the option) are present.

"Keybrd -ID fail"

The identification test will fail when the 4114 cannot reset the keyboard and read the keyboard option number. This may be caused by a broken or loose connection.

CIRCUITS USED: Look for problems on Keyboard, Keyboard I/F on Processor board, and keyboard ribbon cable and connectors.

Processor Check (E)

At this time, Self Test does a more thorough test of Processor board and Keyboard functions. The processor and its related hardware are systematically exercised. Figure E-2 shows location of the Processor board ROMs.

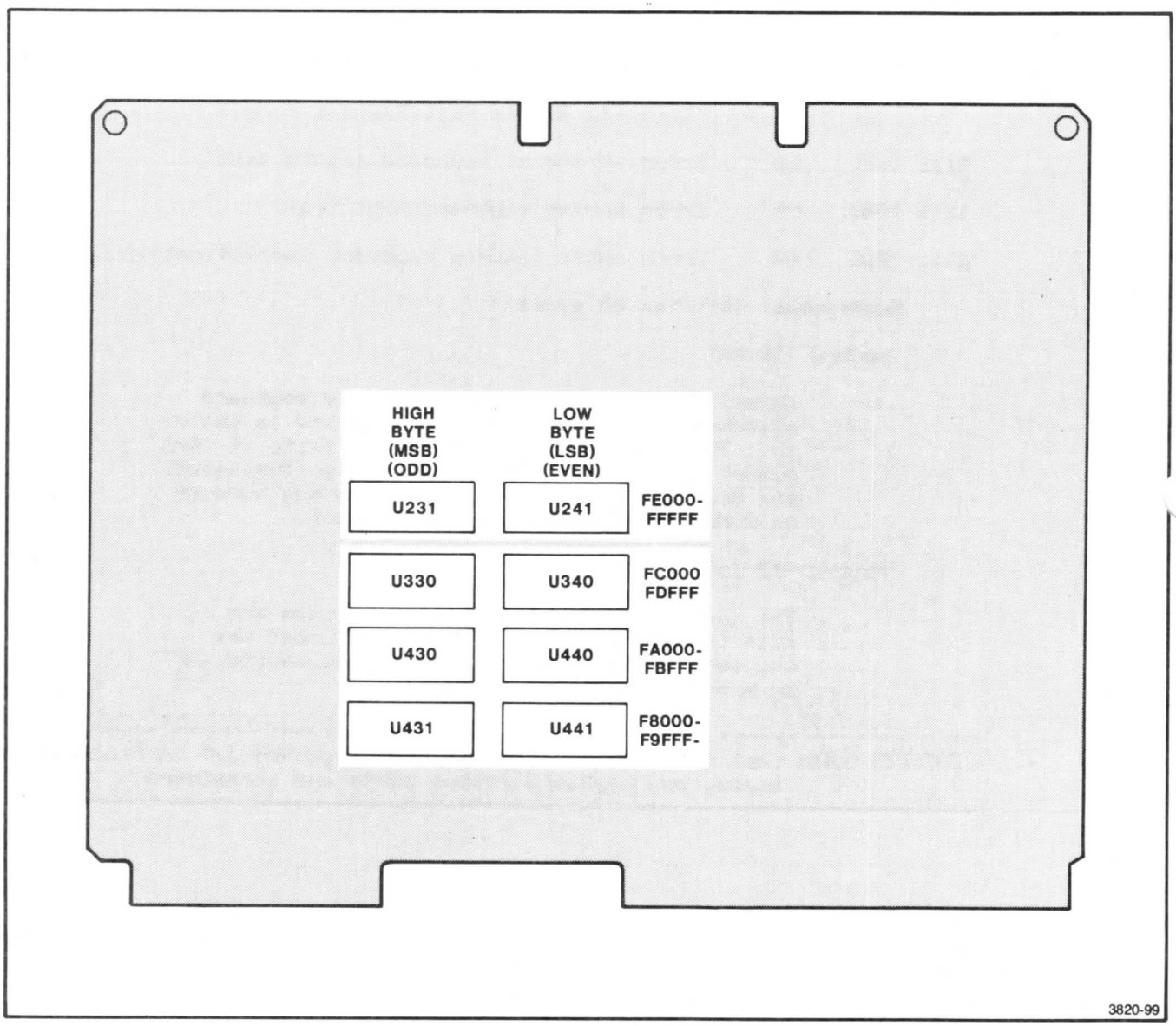


Figure E-2. Processor Board ROMs.

Table E-3

PROCESSOR BOARD ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1110 1111 EF	Error detected during Timer test.
(a) Submessage: Bell; press RETURN, read light code.	
The submessage for the timer test will consist of the following parts: the highest four bits will be one of two codes, the lower four bits will be one of two possible codes. These codes are listed below.	
0001 ----	Failed static test; tests timers' outputs for high/low values.
0010 ----	Failed dynamic test; tests timers for correct count vs. processor execution.
---- 0000	Failure in Timer 0 (I/O address 00E1).
---- 0001	Failure in Timer 1 (I/O address 00E3).
1110 1110 EE	Failure during timer initialization.
1110 1100 EC	Error during standard ROM checksum test.
(a) Submessage 1:	Bell, press RETURN, read light code.
X X nnnn nnnn	Address of ROM problem in Hex XX000. (i.e., 1111 1110 = FE --> Address where problem found is FE000 'X'. This is first ROM pair on the Processor board.)
(a) Submessage 2:	Bell; press RETURN again, read light code.
This submessage consists of two parts, with the highest four bits consisting of one of three codes, and the lowest four bits of the message consisting of one of these three possible codes.	
0001 ---- 0010 ---- 0011 ----	ROM(s) not present. ROM(s) checksum error. Standard ROMs position check.
---- 0001 ---- 0010 ---- 0011	Problem isolated to high ROM of pair. Problem isolated to low ROM of pair. Problem found in both ROMs of pair.

NOTE - Timer 2 cannot be tested at this point. It is checked later during the Host Port check.

Table E-3 (cont.)

ERROR CODE Binary / Hex		EXPLANATION
1110 1011	EB	Error detected in Interrupt Handler Check
Submessages: (printed on screen)		
Interrupts - Static Error:XX		Bits that cannot be set in Interrupt Register (I/O base address 00EA).
Interrupts - Dynamic Address:XX		Level 5 interrupt performed. Failed to reach interrupt vector address: XX + (4 x 5). (b)
Interrupts - Div by 0 Address:XX		A divide by 0 instruction was performed, but did not vector through location 0. XX equals base interrupt address. (c)

CIRCUITS USED: Interrupts circuit block on Processor board.

(a) Submessages are obtained in the following manner: when an error is noted, the bell will ring before each submessage. After noting the error bits (read from the keyboard LEDs), press RETURN, then read the submessage as the next set of lights displayed.

(b) Level five is the easiest level of interrupt to force (hence x5). Each time an increment of a level is made, it moves up four bytes in memory (hence the 4). XX equals the base interrupt address.

(c) This message with XX=00 most likely implies an earlier version of a 8086 processor chip not acceptable for Processor board operation.

NOTE - If either T1 or T2 inputs to the interrupt chip are stuck at a TTL low, Self Test cannot detect this condition. Also, if an "interrupt level" output (from the interrupt chip) is stuck at a TTL low, Self Test cannot detect this condition, either. If the interrupt chip seems to be causing a problem, examine the outputs with an oscilloscope, or replace the Processor board.

Communications and Bus Checks (D)

This set of tests examines the operation of the main terminal bus and the host I/O port. This is accomplished by writing to low RAM (located between 0000 and 7FFF) its own address as data. It then reads this address back, using the comparison as a bus check. This assumes RAMs are good.

Table E-4
RAM/BUS AND HOST PORT ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1101 1111 DF	Problems with low bits of main terminal bus or addressing via this bus.
(a) Submessage 1: Bell, press RETURN, read light code.	
X X nnnn nnnn	XX indicates the base address of the RAM that caused the bus problem: XX000 'X'. (i.e., 00 = 00000 and 20 = 20000.)
(a) Submessage 2: Second Bell, press RETURN, read light code.	
Y Y nnnn nnnn	YY is the Low data byte, showing which bit(s) are in error.
(a) Submessage 3: Third Bell, press RETURN, read light code.	
Z Z nnnn nnnn	ZZ is the High data byte, showing which bit(s) are in error. NOTE: If YY and ZZ are all 1s, this indicates a time-out problem while attempting to access a RAM.
1101 1110 DE	Problem with the high bits of the main bus or addressing via this bus. Here it is writing high RAM (between 8000 and highest address) its address as data; then reading it back.

(a) Submessages 1 to 3: Bell rings before each submessages; after noting the error bits, press RETURN, read submessage as the next set of lights. These submessages have the same scheme as indicated above (under low bits error test and error messages).

NOTE - Self Test cannot check the following signals if they are tied to a TTL low: MWTC; PFAIL; BCLK; INT1; INT2; INT3; INT4; INT6; INT7; BREQ; BGT.

CIRCUITS USED: All RAM locations 0000 to 7FFF and 8000 to top RAM address, bus lines connecting Processor and RAM/ROM board.

Table E-4 (continued)

ERROR CODE Binary / Hex		EXPLANTION
1101 1101	DD	Error detected during host port I/O address check

Submessage: (printed on screen)

"Host Port - Registers
Expect: XX Receive: YY"

This test checks the reset of the USART. After resetting USART, it reads the data at status I/O address E2.
It expects to read XX. If instead it receives YY (where XX not = YY) this means the test failed and the USART cannot be reset.

"Host Port - Register
Expect: XX - YY Receive: ZZ - AA"

The test checks USART Latch (I/O address EB), and USART Interrupt Request (" " EB).

XX - Latch status expected; is 0 if no bits are in error.

YY - Interrupt Request bits in error; if 0, no bits are in error.

ZZ - Latch Status bits in error.

AA - Interrupt Request bits in error.

1101 1100	DC	Error detected during host port baud rate/ character check

Submessage: (printed on screen)

"Host Port - Baud/Character
Baud: XXXX Expect: YY-AA Receive: ZZ-BB"

XXXX - Baud rate in hex (see table E-5).
YY - character sent.
AA - USART data status bits in error, expect zero (I/O address E4). See Figure E-3.
ZZ - character received.
BB - USART Data Status bits in error.

CIRCUITS: All RAM locations 0000 to 7FFF and 8000 to top RAM address bus lines connecting Processor and RAM/ROM board.

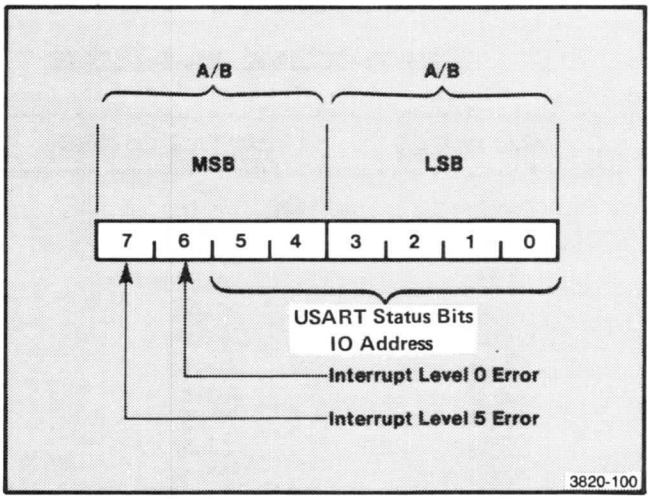


Figure E-3. I/O Address X 'E8'--Status Byte.

The following table may be used to convert Hex numbers received into decimal numbers.

Table E-5

HEX-TO-DECIMAL EQUIVALENTS

HEX NUMBER	DECIMAL NUMBER
12C	300
25B	600
4B0	1200
708	1800
7D0	2000
960	2400
E10	3600
12C0	4800
1C20	7200
2580	9600
4B00	19200
9600	38400

MEMORY TESTS

ROM Check (C)

This set of tests examines the operation of all ROMs on the RAM/ROM board and all option ROMs. The ROMs on the Processor board were tested along with the processor in previous tests. Refer back to Figure E-1 for the locations of ROMs on the RAM/ROM Board.

Table E-6

SYSTEM/OPTION ROMS ERRORS

ERROR CODE Binary / Hex		EXPLANATION
1100 1111	CF	Failure during ROM Map generation.
1100 1110	CE	Error found during ROM checksums test.
Submessages:		Error messages are same as for main ROMs; see Table E-3.
1100 1101	CD	ROMs found in wrong position (options only).

Submessages: (Displayed on screen)

"ROM - Position
Address: XXXX Expect: YY-ZZ Receive: AA-BB
ROM Set: CC-Fail"

Address XXXX -- the base address of the ROM pair being checked.

Expect YY-ZZ --
1) YY is the ROM Set number (same as option number).
2) ZZ indicates even or odd ROM of pair. (If ZZ is odd, then odd ROM is problem; if ZZ is even, then even ROM " " .)

Receive AA-BB --
found ROM Set number AA (instead of YY); BB (like ZZ) indicates odd vs. even of pair.

ROM Set CC-Fail -- CC is option (ROM Set) number of ROM that failed.

Example> Address: 1600 Expect: 42-17 Receive: 42-15
ROM Set: 42-Fail

Means -- that the base address of the ROM pair being checked is 16,000.
42 is the ROM set number expected (disk).
17 is base address + 1 (odd ROM of pair).
If 16 is base address + 0 (even ROM " ").
The test found 42-15 at the address; 42 was the ROM Set, and 15 means the odd ROM for location 14,000 was found there (instead of ROM for 16,000).

Table E-6 (continued)

ERROR CODE Binary / Hex		EXPLANATION
1100 1100	CC	ROM version compatibility problem

Submessage: (printed on screen)

"ROM - Version
ROM Set: XX-VV Expect: YY-ZZ Receive: AA-BB"
ROM Set: CC-Fail

ROM Set used for reference is XX (Note 1), and its version number is VV.
"Expect YY-ZZ" refers to the expected ROM option name YY, and version number ZZ for for the ROM Set being checked.
"Receive AA-BB" reports the actual ROM name (AA) and version (BB) in same socket.

Example> ROM Set: 00-05 Expect: 42-03 Receive: 42-01
Means — The main system firmware (called 00) is version 5. It expects Option 42 ROMs with version 3 or higher to be installed.

Instead, it finds Option 42 ROMs, with only version 1 firmware, installed.

ROM Set: CC-Fail
ROM failure — CC is number of Option where version problem appeared. This ROM set is mapped out of the option.

CIRCUITS USED: RAM/ROM board ROMs and circuits, and ROMs on option boards.

Note 1: XX is option number. System ROMs number is always 00.

RAM Check (B)

This series of tests perform a systematic check of all system RAMs. Each set of tests is grouped, and each group uses the same type of error reporting scheme (light codes). Refer back to Figure E-1 for the locations of the lower 32K RAM.

Table E-7

RAM TEST ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1011 1111 BF	Lowest 32K of RAM, walking ones check. (Here each bit is set and tested, in order from left to right, hence the "walking ones" term). This light code is accompanied by the following light code submessages.
(a) Submessage 1: Bell rings, press RETURN, read light code.	
X X nnnn nnnn	XX indicates the address of the RAM problem at XX0000 'X'.
(a) Submessage 2: Second bell, press RETURN, read light code.	
Y Y nnnn nnnn	YY is the Low Data byte, showing which bit(s) are in error.
(a) Submessage 3: Third bell, press RETURN, and read light code.	
Z Z nnnn nnnn	ZZ is the High Data byte, showing which bit(s) are in error.

(a) Submessages are obtained in the following manner: When an error is noted, the bell will ring. After noting the error bits (read from the keyboard LEDs), press RETURN, then read the submessage as the next set of lights displayed.

Table E-7 (cont.)

ERROR CODE Binary / Hex			EXPLANATION
			NOTE An error is indicated by a bell accompanied by a light code which stays on indefinately. In the memory delay test (BB), the light code may remain lit for as much as 14 seconds while the test is running; this does not indicate an error. This lengthy Delay Memory check can be overridden by entering CONTROL D during the keyboard check.
1011 1110	BE	(b)	Error in "walking zeroes check;" lower 32K RAM.
1011 1101	BD	(b)	Error in "all ones check;" lower 32K RAM.
1011 1100	BC	(b)	Error in "init (zero check);" lower 32K RAM..
1011 1011	BB	(b)	Error in "RAM memory delay check." During the RAM memory delay check, data is held for 14 seconds and then rechecked. The light code will remain lit (stationary) during this check.
1011 1010	BA	(b)	"RAM Memory Map Generation" error. This test checks for RAM and the absence of RAM and generates a corresponding memory map.
1011 1001	B9	(b)	Error in "walking ones check;" upper 32K RAM.
1011 1000	B8	(b)	Error in "walking zeroes check;" upper 32K RAM..
1011 0111	B7	(b)	Error in "all ones check;" upper 32K of RAM.
1011 0110	B6	(b)	Error in "init (zero check);" upper 32K RAM.
1011 0101	B5		Error during RAM stack building.
1011 0100	B4		Error is operating system vector table (lowest 32K of RAM).

(b) If one of these submessages is displayed as an error (the bell rings), the three submessages earlier in the table will have to be read in order to locate the problem.

CMOS Check (AF)

When a CMOS memory error is detected, the LEDs show the "AF" pattern (1010 1111), and a message is written on the display screen. The only time a full CMOS check is performed is during the Adjustment Self Test.

NOTE: The following CMOS error messages report a change in default parameters. This may be caused by either: changing EPROMs, or by a CMOS battery/circuit failure.

Table E-8

CMOS MEMORY ERRORS

ERROR MESSAGE Binary / Hex	EXPLANATION
1010 1111 AF	CMOS Check
Submessages: (printed on screen)	
"Cmos-Error I/O Address: XXXX Expect: YY41 Receive: ZZZZ"	XXXX = Address of problem. If it is addressing correctly, the address reads FFFE. YY41 = YY is the system version number (taken from EPROM) and 41 indicates 4110 series product. ZZZZ = this is what is actually read, instead of YY41.
"Cmos-Checksum"	Checksum error detected.
"Setup Defaults Reset"	CMOS parameters have been updated. This is the same as the Power-up message.

DISPLAY CHECKS (9)

The Self Test program tests the two circuit boards that control how information is displayed on the display module screen: the Display Controller and Vector Generator boards. This set of tests also determine whether the display module is functioning, but does not isolate problems to individual boards or circuits in the display module.

If the Direct Memory Access (DMA) controller is malfunctioning, it can "hang" the system bus. If this happens, the processor will not be able to access the display test code. The terminal will then appear to "hang" on one of the light codes shown in Table E-9.

Table E-9

DISPLAY CONTROLLER, VECTOR GENERATOR, AND DISPLAY MODULE ERRORS

ERROR CODE Binary / Hex	EXPLANATION
1001 1111 9F	4114 PowerUp/Reset Check

(a) Submessage 1: Bell, press RETURN, read light code:

0000 0001	Display Module
0000 0010	Vector Generator
0000 0011	Display Module or Vector Generator
0000 0100	Display Controller
0000 0101	Display Module or Display Controller
0000 0110	Display Controller or Vector Generator
0000 0111	Cannot isolate problem

If 0001 appears as the four most significant bits (leftmost), this indicates a fatal error—these circuits will not work at all or will always generate errors.

(a) Submessage 2: Bell, press RETURN, read light code:

Error code	Explanation	I/O port read	Bit Checked (b)
0000 0001	No I/O port D0 read	D0	0 - 15
0000 0010	Vector in process (bit active)	D0	3
0000 0011	Display list in progress (bit active)	D0	0
0000 0100	No I/O port D2 read	D2	0 - 15
0000 0101	SLU bit active	D2	11
0000 0110	Z bit active	D2	13
0000 0111	Long jump latch active	D2	9
0000 1000	Long vector latch active	D2	8
0000 1001	Generator running active	D2	2
0000 1010	Vector available active	D2	1

Note that these light codes are in consecutive binary order. This is the order in which the tests are done. Thus, if the light code, for example, 0000 0111 appears, all of the tests previous to this have been done and are functioning.

(a) Submessages are obtained in the following manner: When an error is noted, the bell will ring. After noting the error bits (read from the keyboard LEDs), press RETURN, and read the submessage as the next set of lights displayed.

(b) The 0 bit is the least significant bit (furthest to the right) and the 15 bit is the most significant bit.

Table E-9 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
1001 1110 9E	Display Check Display Controller Check

(a) Submessage 1: Bell, press RETURN, read light code.

0000 0001	Display Module
0000 0010	Vector Generator
0000 0011	Display Module or Vector Generator
0000 0100	Display Controller
0000 0101	Display Module or Display Controller
0000 0110	Display Controller or Vector Generator
0000 0111	Cannot isolate problem

If 0001 appears as the four most significant bits (leftmost), this indicates a fatal error. These circuits do not work at all or always generate errors. The terminal hangs with flashing lights.

(a) Submessage 2: Bell, press RETURN, read light code.

Error Code	Explanation	I/O port read	Bit Checked
0000 0001	No I/O port D2 read	D2	0 - 15
0000 0010	DBUSY active after View mode is reset	D2	10
0000 0011	Ready for command bit not active	D0	1
0000 0100	Long jump latch won't set	D2	9
0000 0101	Long jump latch won't reset	D2	9
0000 0110	Long vector latch won't set	D2	8
0000 0111	Long vector latch won't reset	D2	8
0000 1000	No DBUSY reponse to erase command	D2	10
0000 1001	DBUSY on after erase	D2	10
0000 1010	X12 won't load to 0	D2	5
0000 1011	Y12 won't load to 0	D2	4
0000 1100	X12 won't load to 1	D2	5
0000 1101	Y12 won't load to 1	D2	4
0000 1110	Vector execution not started	D0	3
0000 1111	Relative move execution took too long	D0	3
0001 0000	Relative move execution not completed	D0	3
0001 0001	X12 not 1: 0-4095 (1)	D2	5
0001 0010	Y12 not 1: 0-4095 (1)	D2	4
0001 0011	X12 not 0: 4095-4096 (1)	D2	5
0001 0100	Y12 not 0: 4095-4096 (1)	D2	4
0001 0101	X12 not 0: 8091-4096 (1)	D2	5
0001 0110	Y12 not 0: 8091-4096 (1)	D2	4
0001 0111	X12 not 1: 4096-4095 (1)	D2	5
0001 1000	Y12 not 1: 4096-4095 (1)	D2	4
0001 1001	X12 not 1: 4032-4095 (1)(2)	D2	5
0001 1010	Y12 not 1: 4032-4095 (1)(2)	D2	4
0001 1011	X12 not 0: 4095-4096 (1)(2)	D2	5
0001 1100	Y12 not 0: 4095-4096 (1)(2)	D2	4
0001 1101	MX11 stuck high	D2	3

Table E-9 (cont.)

ERROR CODE Binary / Hex	EXPLANATION		
Error Code	**Explanation**	**I/O Port Read**	**Bit Checked**
0001 1110	MY11 stuck high	D2	0
0001 1111	MX11 stuck low	D2	3
0010 0000	MY11 stuck low	D2	0
0010 0001	4095 stored vector too fast (<2.0 ms)	D2	1
0010 0010	4095 stored vector too slow (>3.0 ms)	D2	1
0010 0011	Vector clipping failure	D2	1
0010 0100	Refreshed vector too slow	D2	1
0010 0101	Dot dash not working	D2	1
0010 0110	Speed compensation failure	D2	1

1001 1101 9D — Display DMA check
Vector Generator board

(a) Submessage 1: Bell, press RETURN, read light code.

0000 0001	Display Module
0000 0010	Vector Generator
0000 0011	Display Module or Vector Generator
0000 0100	Display Controller
0000 0101	Display Module or Display Controller
0000 0110	Display Controller or Vector Generator
0000 0111	Cannot isolate problem

If 0001 appears as the four most significant bits (leftmost), this indicates a fatal error. These circuits do not work at all or always generate errors. The terminal hangs with flashing lights.

(a) Submessage 2: Bell, press RETURN, read light code.

0000 0001	Long Jump does not work
0000 0010	Scaling displacement failure
0000 0011	Time too short on timing test
0000 0100	Time too long on timing test
0000 0101	Display Controller not ready

1001 1100 9C — Character Font Initialization

CIRCUITS: Replace Vector Generator or Display Controller boards. Check bus connection and cable connection to display module. Check Display Module.

(a) Submessages are obtained in the following manner: when an error is noted, the bell will ring before each submessage. After noting the error bits (read from the keyboard LED's), press RETURN, then read the the submessage as the next set of lights displayed.

(1) These numbers correspond to the X or Y Display Address Counters. The first number is the starting address during the test and the second is the ending address during the test(see submessage 2 under the error code 9E, located on the previous page).

(2) Short vector format was used (see submessage 2 under the error code 9E, located on the previous page).

Control Flow of Self-Test

Table E-10 shows the logical flow of Self Test. This is the order in which the self diagnostic checks are made when Self Test is initialized. This table does not include any submessages.

A subset of Self Test is the Power Up sequence. This sequence checks approximately 30% of the 4114 circuitry and is performed everytime the 4114 is turned on.

In the following table, the diagnostic checks that are performed during the power up sequence are marked by the letters PUP. When the full version of Self Test is run, all the tests are performed, including a repeat of the power up checks. This table only contains the tests executed by a standard 4114 terminal. The firmware used to check the options (such as the disk drives or Tablet interface board) are contained on those optional boards.

NOTE

The light codes FD (1111 1101), CF (1100 1111), and BB (1011 1011) are not found in this table even though they are listed in the previous tables. These codes are not tested in Self Test, but are generated as error messages by the routine if an error is found during tests. For a definition of these codes, see the previous tables.

Table E-10
SELF TEST/POWER UP TESTS SEQUENCE

ERROR CODE Hex / Binary		EXPLANATION	WHEN EXECUTED
FE	1111 1110	Light checking routine	SLF
FC	1111 1100	Keyboard key check	SLF
EF	1110 1111	Timer check	SLF/PUP
EE	1110 1110	Timer set up routine	SLF/PUP
EC	1110 1100	Standard system ROM check	SLF/PUP
DF	1101 1111	Lowest 32K bus address check	SLF/PUP
BF	1011 1111	Lowest 32K RAM walking ones check	SLF
BE	1011 1110	Lowest 32K RAM walking zeros check	SLF
BD	1011 1101	Lowest 32K RAM all ones check	SLF/PUP
BC	1011 1100	Lowest 32K RAM all zeros check	SLF/PUP
B5	1011 0101	RAM stack building	SLF/PUP
BA	1011 1010	RAM/ROM memory tables building	SLF/PUP
DE	1101 1110	Upper address bus check	SLF/PUP
B9	1011 1001	Upper RAM walking ones check	SLF
B8	1011 1000	Upper RAM walking zeros check	SLF
B7	1011 0111	Upper RAM all ones check	SLF/PUP
B6	1011 0110	Upper RAM all zeros check	SLF/PUP
B4	1011 0100	System vector table expansion	SLF/PUP
FA	1111 1010	Keyboard Identification set	SLF/PUP
CE	1100 1110	Processor ROM check	SLF/PUP
9F	1001 1111	Power up screen check	PUP
9E	1001 1110	Self Test screen check	SLF
9D	1001 1101	Direct memory address check	SLF
9C	1001 1100	Font initialization	SLF
AF	1010 1111	CMOS and RAM to ROM load	SLF/PUP
EB	1110 1011	Interrupt checker	SLF/PUP
DD	1101 1101	Host port register checker	SLF/PUP
DC	1101 1100	Host port baud/character checker	SLF
CD	1100 1101	Option numbers checker	SLF/PUP
CC	1100 1100	Verson compat checker	SLF/PUP

SLF means the test is performed during Self Test.
PUP means the test is performed during the Power Up sequence.

SELF TEST FOR 4114 OPTIONS

Self test is extended to three options that can be installed in the 4114. Options 42/43 (one or two disk drives) require a Disk Controller board. This circuit board contains ROMs which allow it to test itself when Self Test is run. Likewise, the 3PPI board and Tablet Interface board (options 10 and 13/14 respectivly) also contain ROMs which allow these circuit boards to test themselves when Self Test is run. Options 24 through 29 (extended RAM options) are also checked during Self Test, but by the normal firmware, and not by firmware in ROMs on the RAM boards. RAM above the standard 32K bytes is noted as "Upper RAM" in the RAM test (located earlier in this section).

Error messages for the Disk Controller board, Tablet Interface board, and 3PPI board are the same for both the 4114 and 4112 terminals, since these boards are interchangable in both terminals.

ADJUSTMENT TEST FOR THE 3PPI BOARD

(This test checks the cables).

1. Press SELF TEST button.
2. Press and release RESET button.
3. As soon as the LED lights begin to "cycle", release the SELF TEST button.
4. Watch LED check (if no errors occur, the 4114 will go to the keyboard check).
5. Listen for bell to ring on keyboard check.
6. Type control C.
7. When the menu is placed on the screen, select function key associated with 3PPI.
8. When testing 3PPI:
   - A. Connect host port cable to PPI to be tested.
   - B. Type number of port to be tested (0, 1, or 2).
   - C. Press RETURN key (ERROR messages will be the same as 3rd. 3PPI SELF TEST (baud rate check).
9. Prompt will be placed on the screen when done.

Table E-11

3PPI ERRORS

ERROR CODE Binary / Hex			EXPLANATION
0110	1111	6F	Error detected during Register check.

Submessage:(printed on screen)

"3PPI-Register
Sent: XX Expect: YY Receive: ZZ"

Explanation:
The 3PPI control register pattern sent was XXXX. During the test, the register was checked for the expected YYYY (hex). The actual contents read were reported as ZZZZ.

0110	1110	6E	Error detected during 3PPI Character check.

Submessage (printed on screen):

"3PPI-Baud/Character
Sent: XXXX Expect: YY-ZZ Receive: AA-BB

Explanation:
The baud rate was set to XXXX (hex). During the test, the character sent was YY (hex). The character received was ZZ (hex). Interrupt bits expected are ZZ (00), what was received was BB.

The Character check test uses internal loop-back testing. There is no interaction between this test and external equipment. The equipment is operation at either the system preset rate or 1200 baud, whichever is higher.

NOTE - Refer to Table E-5 earlier in this section to convert the hexidecimal numbers received into decimal numbers.

Option 42/43 Error Messages

The 4114 terminal, when equipped with any options such as the disk, amounts to a minisystem. The Self-Test routines help to isolate problems to a part of this system. However, trouble shooting procedures should check the first and most obvious kinds of faults first: diskette problems, or line voltage fluctuations. Avoid blindly zeroing in on the disk options, thus overlooking a possible problem in the main terminal hardware. When problems occur that seem to be the fault of the terminal's disk option, be sure to have the 4114 service manual, option 42/43 service manual, and the disk drive unit service manual on hand for referencing.

Hard and Soft Errors

When disk operations fail to execute properly, they are classified as:

- "Soft errors" - recoverable and random in nature, or
- "Hard errors" - persist after several retries.

  Soft errors, related to the disk, happen when the R/W head can't find a file header, or when R/W data does not match expected data. The mechanical limitations of the disk and drive unit allows: temporary misalignments, oxide dropout on the disk, dirt particles under the R/W head, etc. To keep these transitory problems from hanging-up the system, the terminal's processor recognizes the condition and issues ten retries. If the problem persists, the processor issues a head move command and again calls for another ten retries. If this is unsuccessful, a hard error is reported.

  Hard errors, related to processing on the Disk Controller board, cause the main processor to issue ten retries. If the problem remains the processor gives up and reports the condition as a hard error.

Another kind of hard error occurs when a write command finds that the disk is not inserted, the disk is write-protected, or a similar operator oversight. In such a case the problem appears constant, so no retries are made. The command/operation is aborted, and a message prompts the user to correct the problem.

Trouble Shooting; Initial/Visual Checks

If your terminal is communicating properly with its host system but fails to read or write to its disk, look for disk related problems. Check the media, cables and connectors, or the part of the power supply module that provides disk unit power.

Disk Media Problems. One of the first and easiest tests to make for disk related problems, is to remove the current diskette and replace it with a known good diskette. Try writing to the good disk and then read it, and see if the problem persists. If the problem remains, it is either in the drive unit or the disk controller board or in the connecting cables or power supply.

Disk Unit Faults. See the 119-0977-00 (or equivalent) Disk Drive Unit service manual.

Using Self-Test Program to test the Disk options

Start the program running in the same manner as the normal Self Test (by pushing the SELF TEST and MASTER RESET keys in the proper sucession).

NOTE

Do NOT insert or remove a disk while Self Test is running as this will generate unexpected interrupts.

Table E-12

DISK OPTION ERRORS

ERROR CODE Binary / Hex	EXPLANATION
0101 1111 5F	Board Status Register Check

This test validates the operation of the hardware comprising the Board Status Register (at X'FC00'). Each Read/Write bit in the register is set (set=0) and tested; it is again reset and tested.

Submessage: (printed on screen)

"Disk - Board Status Register"	These tests check each bit in the BSR (Board Status Register).
"Disk - ADR19-1 not = 0"	Wrote a 0 to ADR19 (D3 of FC01) and read back a 1.
"Disk - ADR19-1 not = 1"	Wrote a 1 to ADR19, but read back a 0
"Disk - ADR19-1 not reset, =1"	Wrote a 0 to reset ADR19, but read a 1.
"Disk - INTE-0 not working"	Did not read back what was written at D6.
"Disk - BUSW-0 not working"	Did not read back what was written at D5.
"Disk - HDL3-0 not working"	Did not read back what was written at D3.
"Disk - HDL2-0 not working"	Did not read back what was written at D2.
"Disk - HDL1-0 not working"	Did not read back what was written at D1.
"Disk - HDL0-0 not working"	Did not read back what was written at D0.

Circuits used: Address Decode, Input Data Buffer, and Board Status Register.
NOTE: The first three submessages listed check the ADR19 Address Counter.

Table E-12 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
0101 1110 5E	Initialize and check Disk Controller

The FDC is put into its command phase (regardless of its present state) via a series of command reads and writes. The following bits are tested for correct state:

Under X'FC00' -- D7 (EOC-1)
Under X'FC08' -- D7 (RQM-1) and D6 (DIO-1).

A SPECIFY command is then issued by the processor.

Submessages: (printed on screen)

"Disk - Controller Protocol" "EOC-0 is 0 after init"	FDC generates an unexpected interrupt, bit is in wrong state after initialization.
"Disk - DIO-1 is 0 - Write required"	FDC required a write to it, while processor expects to read from it.
"Disk - DIO-1 is 1 - Read required"	FDC requires a read from it, but processor expects to write to it.
"Disk - DIO-1 is 1 after init"	Bit D6 is in wrong state after initialization.
"Disk - RQM-1 remains 0"	FDC never sends RQM-1 (fails in 1000 tries).
"Disk - Cannot restore Protocol"	Runs initialization sequence, but cannot put FDC into a known state. (Processor has no idea what FDC is doing).

Circuits used: FDC, Board Status, Control Strobes, Data MUX, and Address Decode.

0101 1101 5D	Drive present check

The processor issues a SENSE DRIVE 0 STATUS (SDS) command. Drive 0 should be present. The D7 (RQM-1) and D6 (DIO-1) are tested for correct states before and during the command.

Submessage: (printed on screen)

"Disk- F0: not present"	Drive 0 should always be present. This message means the FDC or Disk Drive control cannot find drive unit 0.

Circuits used: FDC's disk control I/F, and Disk Drive Control circuits.

Table E-12 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
0101 1100 5C	Intersystem Interrupt check

The following procedure is used to generate an interrupt: The heads are unloaded (should already be unloaded from last test), and the processor issues a RECAL DRIVE 0 command. Recal is executed, but the head does not move. The FDC does not know that the heads were unloaded, so it generates an interrupt. An error is also reported, unless head was already at Track 0.

The processor then issues the SENSE INTERRUPT STATUS (SIS) command to read the results of the RECAL command. The results of the SIS command are checked as well as RAM-1 and DIO-1.

Submessages: (printed on screen)

"Disk - Intersystem Interrupt Check"	
"Disk -Bad FC00 init"	Board Status Register contains error (different state than expected).
"Disk -Bad FC08 init"	FDC status register contains an error (different state than expected).
"Disk -Bad FC00 RECAL-1 status"	Error in Board Status Register (BSR) after first byte of RECAL command written.
"Disk -Bad FC08 RECAL-1 status"	Error in FDC after first RECAL byte written.
"Disk -Bad FC00 RECAL-2 status"	Error in BSR after second RECAL byte written.
"Disk -Bad FC08 RECAL-2 status"	Error in FDC after second RECAL byte written.
"Disk -Level 7 interrupt not present"	Expected interrupt not present.

Table E-12 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
"Disk -Bad FC00 SIS status"	Error in BSR after Sense Interrupt status byte written.
"Disk -Bad FC08 SIS status"	Error in FDC after Sense Interrupt status byte written.
"Disk -ST0 data error"	Error in ST0, read at FDC.
"Disk -Bad FC00 ST0 status"	Error in BSR after ST0 status byte read.
"Disk -Bad FC08 ST0 status"	Error in FDC after STO status byte read.
"Disk -Track error"	Error in track number (PCN), read at FDC.
"Disk -Bad FC00 Track status"	Error in BSR after track number read.
"Disk -Bad FC08 Track status"	Error in FDC after track number read.
"Disk -Level 7 interrupt still present"	Interrupt still present.

Circuits used: Address Decode, Board Status, Control Strobes, Data MUX, and FDC.

Table E-12 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
0101 1011 5B	DMA Operation check
Submessage: (printed on screen)	
"Disk - DMA transfer failed"	Data ('00') not found at current DMA address (RAM only).

Circuits: DMA State Machine, Data MUX, Control Strobes, Address Decode, Address Counters, Input Data Buffers, and Board Status blocks.

0101 1010 5A — DMA addressing check

Both this test and the previous test must be completed before the DMA State Machine and the DMA Address Counters are fully tested; the testing of one requires the operation of the other.

The DMA Address Counters are write only. The only way to look at these counters is to examine the most significant bit (MSB), which is at D4 of the Board Status Register (X'FC00').

The twenty bit counters are subdivided into three groups: High Nibble (FC01), Middle Byte (FC02), and Low Byte (FC03). Each group is tested individually in the following manner.

— HIGH NIBBLE TEST —

Test high nibble first because all bits must ripple through the high nibble while testing the middle and low bytes.

STEP SET-UP

1. Load High Nibble with 0.
2. Does D4 = 0 ? See NOTE.

TEST

3. Load Middle Byte and Low Byte with X'FF.'
4. Step DMA.
5. Does D4 = 0 ?

TEST

6. Repeat steps 3 through 5 eight times.
7. On eighth time, does D4 = 1 ?
8. Repeat another eight times. (D4 should = 1 for these eight.)
9. On sixteenth time, does D4 = 0 ?

NOTE- If D=1 an error message is reported. All "D=N?" steps will cause an error unless the number is as expected. Error messages are in the accompanying tables.

Table E-12 (cont.)

ERROR CODE Binary / Hex	EXPLANATION

DMA Address Check (continued)

— MIDDLE BYTE TEST —

STEP SET-UP
10. Load High Nibble with 7.
11. Does D4 = 0 ?
12. Load Middle Byte X'FF.'

TEST
13. Load Low Byte with X'FF.'
14. Step DMA.
15. Does D4 = 0 ?
16. Reload Low Byte witX'FF' (leave Middle Byte since we are testing it).
17. Repeat steps 13 through 15; on 256th does D4 = 1? (Does High Nibble equal eight?).

SET-UP
18. Reload High Nibble with F.
19. Does D4 = 1 ?

TEST
20. Reload Low Byte with X'FF,' and Step DMA.
21. Repeat step 19 twohundred fiftysix times.
22. On 256th time does D4 = 0 ? (High Nibble = 0)

— LOW BYTE TEST —

Same procedure as Middle Byte test except the Low Byte and Middle Byte are reversed.

Submessages for DMA Address Counters (printed on screen):

"Disk - DMA Address Counters
- ADR19-1 Error

"Early 0-1 @ FC01"	Error detected at steps 2 or 5 (Counter reached 8 too soon)
"No 0-1 @ FC01"	Error detected at step 7.
"Early 1-0 @ FC01"	Error detected at step 8.
"No 1-0 @ FC01"	Error detected at step 9.
"Early 0-1 @ FC02"	Error detected at steps 11 or 15.
"No 0-1 @ FC02"	Error detected at step 17.
"Early 1-0 @ FC02"	Error detected at step 19.
"No 1-0 @ FC02"	Error detected at step 22.
"Early 0-1 @ FC03"	Same explanation as for FC02 messages, above, except substitute FC03 for FC02 in explanation of Middle Byte tests.
"No 0-1 @ FC03"	
"Early 1-0 @ FC03"	
"No 1-0 @ FC03"	

These tests check the clocking and carries of one counter to the next.

Circuits used: Same circuit blocks as used in DMA Operation Check, except Data MUX not used.

Tablet Self Test Error codes

The light codes for the tablet are indicative of failure of the tablet to complete a Self Test sequence and the operation of the Tablet Controller board should be investigated.

During the tablet test, the proper error message is printed on the terminal screen if a test fails to pass. These submessages are accompanied by one of the follow light codes (listed in table E-13).

A soft error will allow the tablet to be used. It alerts the operator that a problem exists.

A fatal error removes the tablet from the interrupt routine of the terminal. The tablet can not be used until the problem is corrected and the error cleared.

Table E-13

TABLET ERRORS

ERROR CODE Binary / Hex		EXPLANATION
0100 1111	4F	Board Communications check error.

Submessage: (printed on screen)

"Tablet -Board I/O Timeout"

May appear during either the Power Up sequence or Self Test. It indicates that the terminal firmware is unable to communicate with the Tablet Controller board, and that a processor timeout occurred wheen communication was attempted. This is a FATAL error.

0100 1110	4E	Data Register bit check error.

Submessage: (printed on screen)

"Tablet -Data Register Bit Error"

Each individual bit of the data register is tested for set and reset. Message indicates at least one bit is not acting properly. This is a SOFT error.

0100 1100	4C	Digitization check error.

Submessage: (printed on screen) - One of the following submessages will accompany the light code:

"Tablet -Digitization Timeout Error"

A start digitization command was given to the tablet and one of the FIRE pulses was not returned within 0.5 seconds. This is a SOFT error.

"Tablet -Digitization Firing Sequence Error"

The status bits, indicating which data firing (X1, X2, Y1, Y2) is present, were out of sequence. This is a SOFT error.

Table E-13 (cont.)

ERROR CODE Binary / Hex	EXPLANATION
0100 1101 4D	Data Register count check error

Submessage: (printed on screen) - Only one of the following submessages will accompany the light code:

"Tablet -Data Register Counting Error (Low)"

Indicates that the data register was incapable of counting from 0 to 31 by one. This is a SOFT error.

"Tablet -Data Register Counting Error (High)"

Indicates that the data register was incapable of counting from 0 to 65539 by 29. This is a SOFT error.

"Tablet -Erroneous Interrupting Indication"

The tablet status indicates that it is trying to interrupt the processor when it should not. This is a SOFT error.

"Tablet -failed To Interrupt"

Indicates the tablet status is not trying to interrupt the processor when it should. This is a SOFT error.

"Tablet -Data Register Counting Error (Digitization)"

The data register failed to count at all during a start digitization. This is a SOFT error.