TANDY®

Service Manual

26-6021/2

TANDY®

6000/6000 HD

Catalog Number 26-6021/2

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

SERVICE MANUAL

TANDY® 6000/6000-HD

Catalog Number 26-6021/2

TANDY® 6000/6000-HD Service Manual

Contents Page No.

List of Figures

List of Tables

1/ Introduction

The TANDY 6000/6000-HD Microcomputer is a powerful disk-based desk-top business computer with many advanced features. These features include portable software, 512K of memory expandable to 1M, detachable typewriter-format keyboard with numerical keypad and 8 programmable function keys, green CRT Monitor screen, and one parallel and two serial ports for external connection to a variety of printers and communications links.

Optional features include an external floppy Disk Bay Expansion Unit (1-drive unit or 2-drive unit), a 15 Megabyte or larger Hard Disk System for mass storage, an ARCNET™ system for local area communications network, a graphics board for video graphics capability, and a multi-terminal interface board.

This manual is intended as a guide to assist in the diagnosis of system problems to the subassembly level. It contains detailed instructions on disassembly and assembly of major subassemblies as well as some troubleshooting hints for the PCBs and subassemblies contained in the system. It also includes a section on the theory of operation that describes board operation and some individual component functions. It does not, however, provide a component by component analysis of the system.

The basic TANDY 6000 is supplied with two floppy Disk Drives and five PCB assemblies; the TANDY 6000-HD is supplied with one floppy disk and one internal 15-meg hard disk. Two of the PCB assemblies are mounted in the Electronics Module, which is attached to the Base Assembly. These include the I/O Processor PCB and the Power Supply PCB. The Sound PCB, is mounted inside the Base Assembly at the left front corner. The CRT Monitor PCB mounted on the Base Assembly, is the electronics for the CRT assembly. The seven slot expansion unit plugs into the I/O Processor PCB, and the 16-bit CPU and memory board plug into the expansion unit along with the Video/Keyboard Interface PCB.

™ - Datapoint Corporation

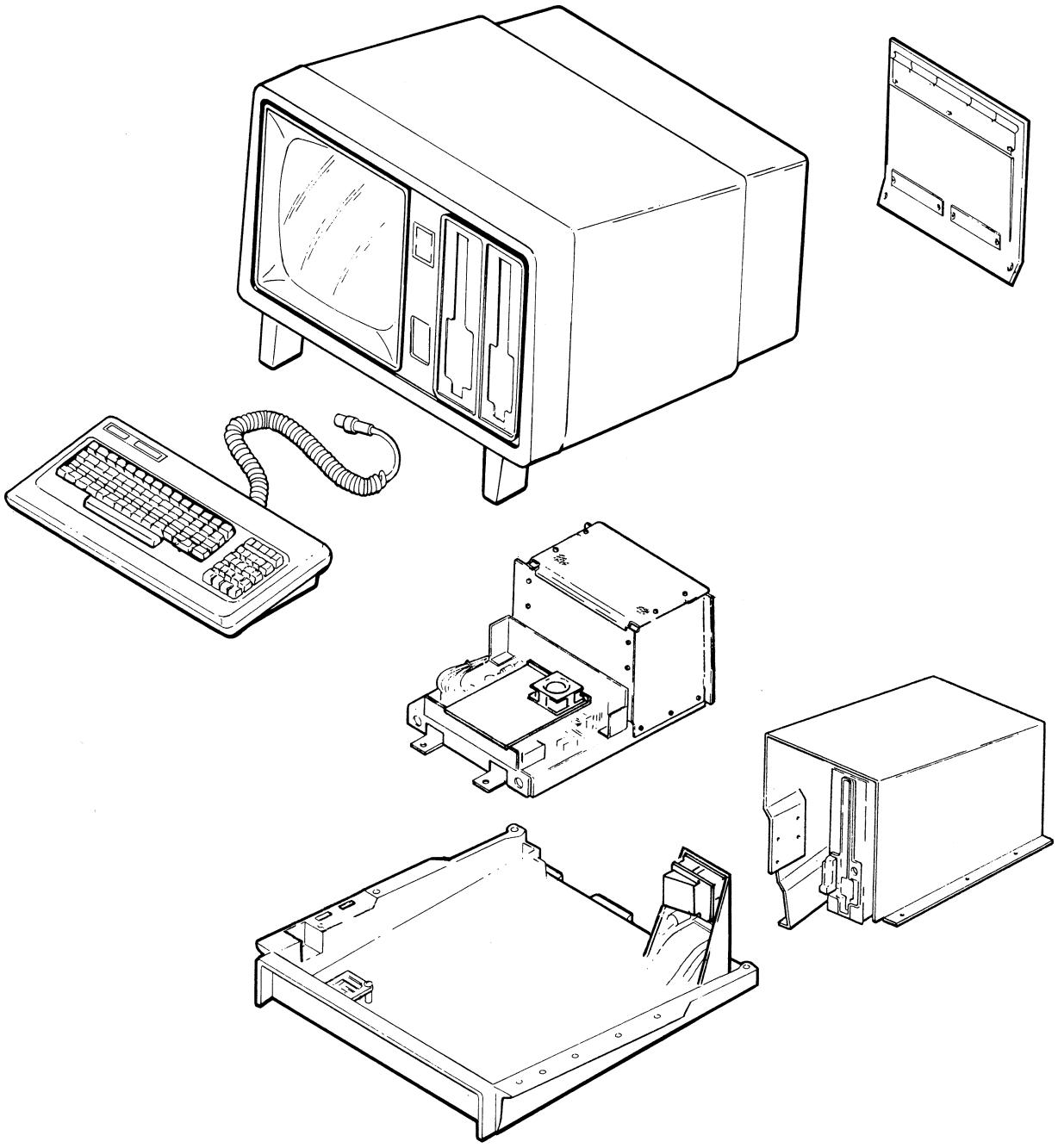


Figure 1-1. Major Assemblies, TANDY 6000/6000-HD

A simplified exploded view of the TANDY 6000/6000-HD (Figure 1-1) helps locate major sub-assemblies as they are described in the following paragraphs. Disassembly procedures noted in Section 3 must be followed in the order presented due to the mounting locations of the individual components.

The major subassemblies that comprise the TANDY 6000/6000-HD include (1) the Base Assembly, (2) the Electronics Module, (3) the RESET Switch/Power-On Indicator Module with cable assembly, (4) the Disk Drive/Drive Support structure, (5)Top Cover Assembly, (6) the Bezel/CRT Assembly, (7) Card Cage Assembly, and (8) the Keyboard Assembly. The disassembly of each of these assemblies is discussed in Section 3. Care should be exercised in handling plastic components to prevent scratching or marring of the surface finish.

1.1 Base Assembly

The Base Assembly consists of the molded plastic base, power and signal I/O component mounting brackets, power ON/OFF switch, and Sound PCB that is responsible for generating an audible tone when key closure is achieved. The other assemblies of the TANDY 6000/6000-HD are mounted to the Base Assembly. The Base Assembly has rubber feet to protect the surface on which the TANDY 6000/6000-HD is placed for operation.

1.2 Electronics Module

The Electronics Module consists of a formed metal chassis, three component mounting brackets, two printed circuit boards, and a card cage assembly with three additional boards. It is mounted to the instrument Base Assembly with four screws that are accessible when the Top Cover Assembly is removed from the computer. When these screws and the electrical connections to the assembly are removed, the Electronics Module may be removed from the Base Assembly as a unit. The module mounts the I/O Processor PCB, the Video/Keyboard Interface PCB, 16-bit CPU/Memory PCBs, the Power Supply PCB, and the power supply cooling fan. Three ribbon cables connected to the I/O Processor Board exit the module through a slot in the right side of the chassis and connect to the rear terminal input connectors or the disk drive(s). The Power Supply Assembly covers the front half of the assembly. The Mother Board mounts vertically in the edge card connector in the middle of the I/O Processor Board. It is rigidly supported by the card cage sheet metal at the rear of the module.

1.3 RESET Switch/Power-On Indicator Module

The RESET Switch/Power-On Indicator module is mounted to the Drive Support Structure and consists of the power ON/OFF indicator, the RESET Switch, and cable assembly. The RESET switch, when pressed, blanks the screen and flashes the command INSERT DISKETTE on the screen. To remove this module from the unit, it is necessary to first remove the Top Cover Assembly. When reinstalling the assembly, it must be properly positioned with respect to the Bezel/CRT Assembly cutout.

1.4 Drive Support Structure

The Drive Support Structure is a rugged, formed sheet metal design that is attached to the Base Assembly with six mounting screws. Its design permits circulating air flow to the disk drives for improved performance. It contains shielding to protect the floppy disk drive electronics from RF interference by the switching power supply or video display. It mounts two slim line floppy Disk Drive assemblies (TANDY 6000), or one slim line floppy Disk Drive and one 15 Megabyte Hard Disk (TANDY 6000-HD). The 6000-HD is supplied with one floppy disk and one hard disk.

1.5 Top Cover Assembly

There are three mounting screws on the right side of the case, three on the left, one in the back that mount the Top Cover to the Base.

Once these are removed, the Top Cover Assembly may be tilted up and lifted off the Base Assembly.

1.6 Bezel/CRT Assembly

The Bezel/CRT Assembly is a molded plastic cover that contains the cathode ray tube (CRT). The CRT monitor PCB and associated hardware are mounted to the base. The Bezel/CRT Assembly is attached to the base with mounting screws that are accessible from the underside of the unit.

CAUTION

The cables between the Video/Keyboard Interface PCB, Power Supply and the Monitor PCB are short and may be damaged if care is not exercised during their removal. Exercise care to prevent damage to the components mounted to the Base Assembly. Do not drop or otherwise mishandle the Bezel/CRT Assembly as the CRT may implode, causing harm to personnel and components.

Plug-in connectors attach the Bezel/CRT Assembly electrically to the Base Assembly. To detach the Bezel/CRT Assembly completely, disconnect these connectors. Handle the assembly carefully to prevent scratching or marring the Bezel surface.

The Video Monitor PCB forms the Video Monitor Assembly for the TANDY 6000/6000-HD. The Video Monitor PCB is mounted on the inside on the Base Assembly. Signal and power cables interconnect it with the Video/Keyboard Interface PCB and Power Supply Assembly on the Electronics Module.

The Rear Door Assembly is a removable assembly that allows easy access to the rear compartment and card cage (when installed). It slides into a groove at the top of the Bezel/Cover Assembly and is attached to the Base Assembly by two thumb screws that secure it at the bottom.

1.7 Keyboard Assembly

The Keyboard Assembly is mechanically separate from the Base/Bezel/Cover Assembly and is electrically connected through a 5-pin DIN connector located on the front lower lip of the Base Assembly. The two units are connected by a coiled cable assembly attached to the Keyboard Assembly that allows it to be moved up to 3 feet away from the Base Assembly. A strain relief bushing provides protection for the signal cable to prevent accidental pullout of the cable from the Keyboard Assembly. The keyboard is a thin-line design with standard typewriter key pad and numeric key pad. Contained as part of the numeric key pad section are eight function code buttons, F1 through F8, which allow application dependant programmable functions to be selected. Cork feet provide protection for the mounting surface on which the Keyboard Assembly is mounted.

2/ Technical Specifications

2.1 Physical Characteristics

2.1.1 Case/Bezel/Base Assembly

Width 21.0 inches (53.3 cm)
Height 13.5 inches (34.3 cm)
Depth 20.5 inches (52.1 cm)
Weight 49.9 pounds (22.5 kgm)

2.1.2 Keyboard

Width 18.0 inches (45.7 cm)
Height 2.5 inches (6.4 cm)
Depth 7.5 inches (19.1 cm)
Weight 3.3 pounds (1.49 kgm)

2.2 System Operating Characteristics

		Min	Typ	Max	Units
Ambient Temperature		55	75	85	Degree F
		12	23	30	Degree C
Voltage Range	(USA)	95	115	135	VAC
	(Europe)	190	230	270	VAC
Current Drain		---	1.5	2.0	A
Line Frequency		47	50/60	63	Hz

2.3 Peripheral Interfaces

Serial Interface

Channel A allows asynchronous or synchronous communication.

Channel B allows asynchronous communication only.

Both channel A and B conform to the RS-232C Standard

Both use DB-25 connectors on the back of the display console. Pin-out connections are shown in Section 5, Cable Wiring/Pin Designations.

Parallel Interface

Connects to a line printer via the 34-pin connector on the back of the display console. See Section 5, Cable Wiring/Pin Designations.

Outputs 8 data bits in parallel. Inputs 4 data bits. All levels are TTL compatible

Multi-Slot Card Cage

Provides four additional slots to accommodate hard disk drive interface, graphics board, ARCNET board, multi-terminal interface board.

Disk Bay Expansion Unit

Optional extra unit contains either one or two disk drives, 8" floppy diskette, 500K byte storage per diskette (single sided, double density or 1 megabyte with double sided, double density).

16-Bit CPU Board

Provides 16-bit operation for high-level language tasks. Hardware allows 8 levels of vectored interrupts, 4 levels of fixed priority bus arbitration, a Z80 to MC68000 memory interface controller, and direct access for up to 7 megabytes of memory. Software supports only a level 5 interrupt. Software supports 1 Megabyte of memory.

The main components of this board are the MC68000 CPU and the AM9519A Interrupt Controller.

512K-Byte, 16-Bit Memory Board

Offers optional byte parity checking and detection logic and selecting to map memory on any 256K boundry within 7-Meg memory space. 1 megabyte of memory is supported by software. Other chip locations are only screened on the board and sockets aren't installed.

3/ Disassembly/Assembly Procedures

The TANDY 6000 Microcomputer is designed for table-top operation. Dimensions of the main housing assembly and the keyboard assembly are given in Technical Specifications, Section 2. A desk assembly may be used that allows mounting of optional extra disk drives used with the TANDY 6000/6000-HD system. Adequate space should be left around the unit to allow sufficient air flow to all components.

If the TANDY 6000 has the fan enclosed in a metal housing on the back of the access panel you need to follow the disassembly and assembly instructions in the Model 16B Service Manual (See Figures 5-2 and 5-3). Otherwise, follow the disassembly and assembly instructions contained in the following procedures (See Figures 5-4 and 5-5). Exercise care in handling the Top Cover and Bezel/CRT Assemblies to prevent scratching or marring the surface finish.

3.1 Top Cover Assembly

1. Remove all power from the unit by disconnecting the power cord. Remove peripheral cables (if required).

2. Remove from the disk drives, the cardboard inserts that protect the drive during shipment. (Save for later use.)

3. Place the unit upside down on a smooth, padded surface to prevent scratching the painted surfaces.

4. Remove seven (7) screws that attach the Top Cover Assembly to the Base Assembly. There should be three screws on the right side, three screws on the left, and one screw at the rear. See Figure 3-1, which shows the location of the screws.

5. Hold the two assemblies together and turn the unit rightside up.

6. Remove the Rear Access Door by removing the two screws at the bottom and pushing down and out on the door.

7. Lift up the rear of the top cover and angle it towards the front panel, then lift the top cover away from the base assembly.

8. Once the Top Cover Assembly is clear, lay it off to the side.

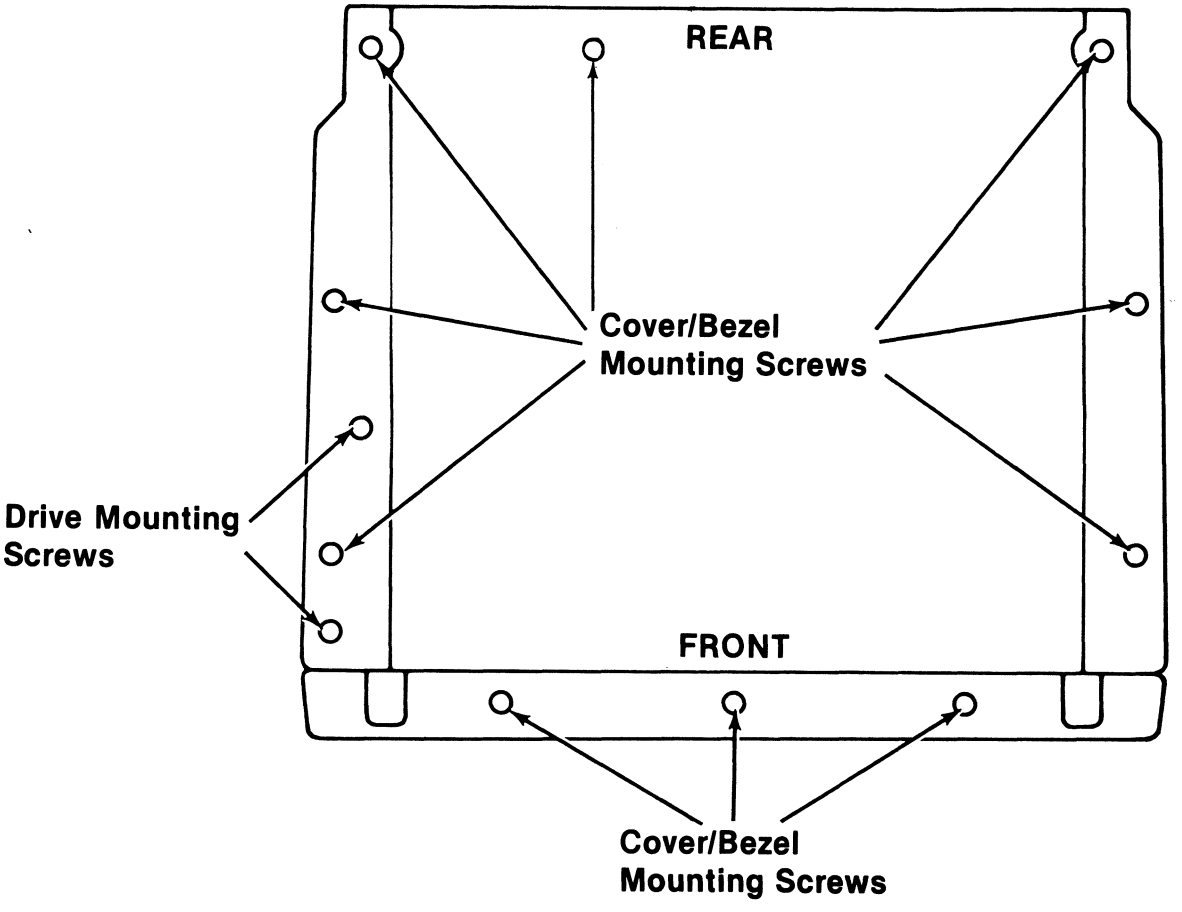


Figure 3-1. Cover Assembly and Bezel Assembly Mounting Screws

3.2 Bezel/CRT Assembly Removal

1. Loosen the three (3) screws at the front of the unit that attach the Bezel/CRT Assembly to the Base Assembly. See Figure 3-1, which shows the location of these screws.

2. Remove the two (2) screws, at the top of the Drive Support Structure, which attach the Bezel/CRT Assembly support bar to the Drive Support Structure.

3. Remove the two (2) screws, at the left of the unit, which attach the CRT Monitor PCB Bracket to the Base Assembly.

4. Separate the two units (Base and Bezel/CRT) by disconnecting the attaching harnesses (one to the Video/Keyboard Interface PCB and an in-line connector to the Power Supply Assembly).

5. Remove the ground wire spade lug terminal from the CRT Monitor PCB. This completely separates the Bezel/CRT Assembly from the Base Assembly.

3.3 CRT Removal

1. Disconnect the tube socket from the rear of the CRT.

2. Disconnect the deflection coil wire connector at the CRT Monitor PCB.

CAUTION

Make sure the high voltage is discharged from the CRT (use grounded screwdriver to discharge).

3. Disconnect the high voltage clip.

4. Disconnect the in-line connector which attaches the CRT Monitor PCB to the ground wire around the rear of the CRT.

5. Remove the two left mounting nuts and washers that attach the CRT Monitor PCB bracket to the Bezel/CRT Assembly and remove the bracket and board from the assembly.

6. Remove the other two nuts and washers from the CRT. Carefully lift the CRT from the Bezel/CRT Assembly.

CAUTION

Handle the CRT very carefully to prevent injury due to CRT implosion. Do not handle tube using the neck of the tube. ALWAYS USE GOGGLES OR SAFETY GLASSES.

7. Assemble the Bezel/CRT Assembly in the reverse order of disassembly. Make sure that the grounding wire from the Electronics Module is connected to the lug on the CRT Monitor PCB lower rear mounting screw.

3.4 Brightness and Contrast Controls

1. The brightness and contrast controls are accessible after the Bezel/CRT Assembly has been removed from the Base Assembly.

2. Remove either control by first removing the knob attached to the POT shaft.

3. Remove the connector from the pot, noting the manner in which the connector is mounted. The connector is not keyed, so it would be possible to put it on backward when reassembling. The numbers on the connector should be down and not able to be read.

4. Remove the attaching nut and slide the control off the bracket.

5. The brightness control (500K ohms) is to the front of the assembly, contrast control (500 ohms) is to the rear.

6. Reassemble in the reverse order, making sure the knobs are fully pushed onto the pot shafts to align with the cutout slots in the Base Assembly.

3.5 CRT Monitor PCB

1. Remove the 10 Pin Edge Connector.
2. Remove the four (4) screws which attach the CRT Monitor PCB to the bracket.
3. Re-assemble in the reverse order.

3.6 Drive Support Structure

The Drive Support Structure is a formed sheet metal part that houses the thin line Floppy Disk Drive Assembly(s) and the Hard Disk Drive Assembly. It is attached to the Base Assembly with six screws, two of which are on the right-hand side of the structure. The other four screws are on the lefthand side of the structure.

1. Remove the Top Cover Assembly (see Paragraph 3.1).
2. Remove the power and signal connectors from the rear of the floppy and hard disk unit(s).
3. Loosen the 2 rear screws and remove the middle screw that mount the RESET Switch/Power-ON Indicator Module mounting bracket and remove the bracket by sliding it forward.
4. Remove the Hard Disk Power Supply by removing the four mounting screws, one in each corner.
5. Remove the Drive Support structure by removing the four screws at the left side of the structure and the two at the right.
6. Remove the structure from the base.
7. Remove the floppy disk drive from the support structure by removing two screws at the top and two screws at the bottom of the Drive Support Assembly.
8. Slide the disk drive forward to remove it from the support structure.

9. If a drive is to be replaced, remove the front bezel by removing the mounting screws (two at the top and two at the bottom front lip).

10. Remove the Hard Disk Drive from the support structure by removing the two screws at the lower left of the drive support structure and the three nuts at the lower left.

11. Reassemble in the reverse order of disassembly.

3.7 Electronics Module

The Electronics Module is mounted to the Base Assembly with four screws that are accessible when the Bezel/CRT Assembly is removed from the unit. The module may be removed as a complete assembly or individual parts, depending on which parts troubleshooting procedures indicate may be faulty. Contained on this assembly are six PCB assemblies (I/O Processor PCB Assembly, Video/Keyboard Interface PCB Assembly, Mother Board, 16-bit CPU, 16-bit Memory, and Power Supply PCB), and the instrument cooling fan. Interconnection of the I/O Processor PCB and other components is accomplished by the use of edge-card connectors.

1. Remove the shield from the Power Supply Assembly by removing the attaching screws and clips.

2. Disconnect the plug from the sound board at the left front of the Base Assembly.

3. Disconnect the switched AC input (blue and brown wires) from the terminal strip at the left rear of the Power Supply Assembly. The wires going to the fan assembly may be left connected as they are part of the Electronics Module.

4. Remove the plug from connector J2 on the Video/Interface PCB.

5. Remove the wiring (brown and blue twisted pair) from clips on the front and right side of the electronics chassis.

6. Unplug the ground wire connected from the front of the Electronics Module to the Keyboard Assembly plug.

7. Disconnect the inline fuse to the Keyboard Assembly plug.

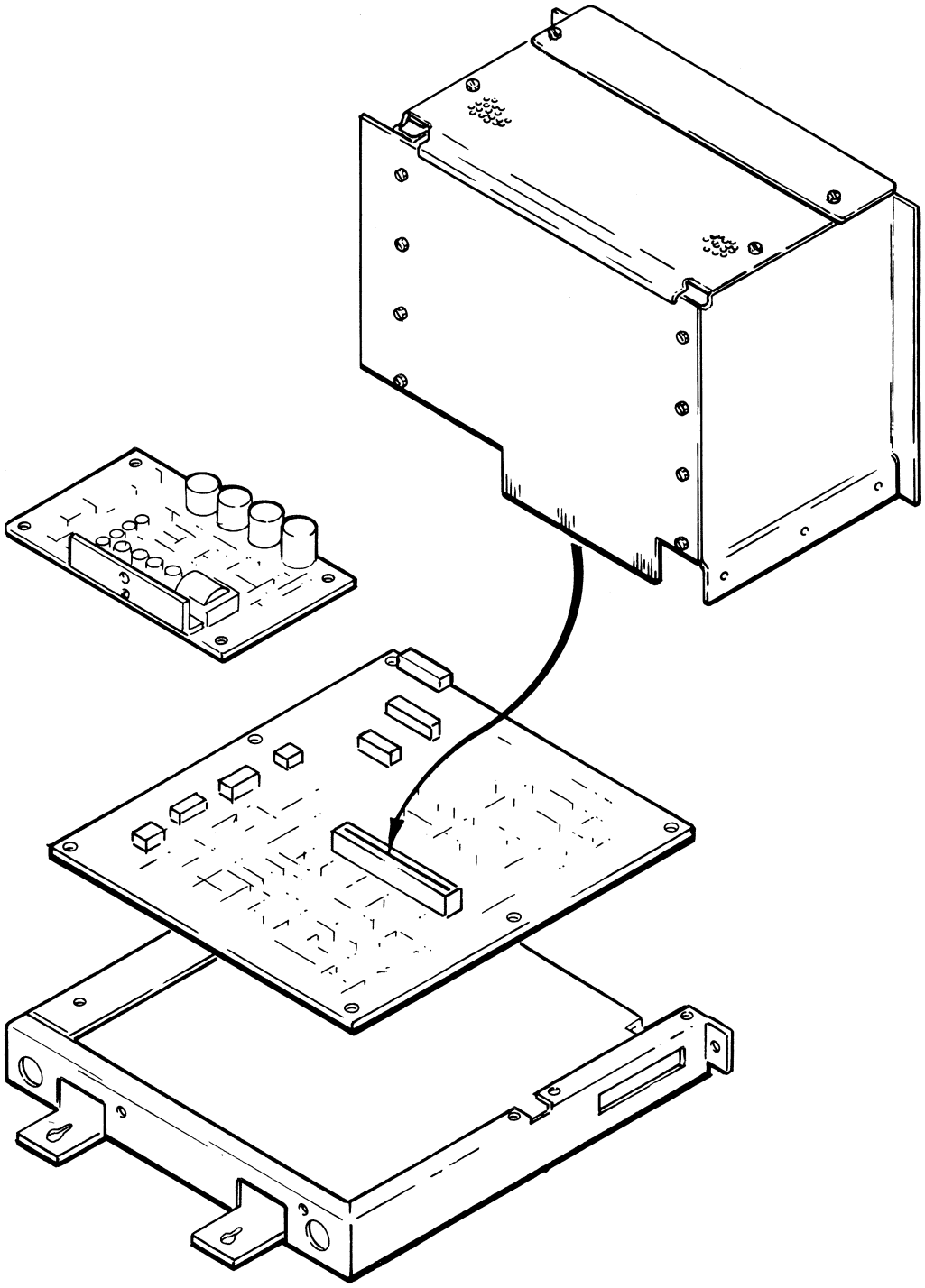


Figure 3-2. Electronics Module Assembly

8. Disconnect the grounds from the two cables attached to the Video/Keyboard Interface PCB on the grounding lugs of the RH Board Retainer.

9. Remove the PC Board Retainers (one on each side) that secure the PCBs in the Mother Board assembly.

10. Disconnect the Bezel/CRT cable assembly connector and the Keyboard cable connector from the Video/Keyboard Interface Board.

11. Remove the boards from the Card Cage, making note of their position for re-assembly. Boards must be re-installed in the relative position listed below. The lowest slot is position 1.

Relative Board Position	Description	Priority
1	ARCNET	1 (lowest position)
2	Hard Disk Interface	2
3	Multi-Terminal Interface	3
4	Graphics	None
5	Video/Keyboard Interface	None
6	512K Memory Board	None
7	16-Bit CPU Board	None

All the listed boards might not be included in all units.

12. Unplug P5 from the J8 connector on the RH side of the Mother Board. Then remove the screws on the RH side of the Card Cage, which mount the Card Cage to the Electronics Module chassis.

13. Remove the four screws that hold the Card Cage Cover; remove the Cover.

14. Remove the screws that hold the Chassis Rear Panel; remove the Rear Panel.

15. Remove the three screws that hold the RH Card Cage Panel. The middle screw will release the grounding lug that goes to the CRT Monitor PCB.

16. Remove the three screws on the LH side of the chassis. The middle screw will release the ground wire.

17. Remove the Mother Board assembly from the Electronics Module chassis.

18. Remove the Power Supply Assembly from the Electronics Module chassis by removing two screws at the left and right rear of the Power Supply and two screws at the front vertical lip.

19. Disconnect plug P5 from J5 on the I/O Processor PCB and lift the Power Supply Assembly out of the way. The fan and power connections to the disk drives should still be attached. Pull the cable to the Sound PCB through the hole in the chassis.

20. Unplug from the front of the I/O Processor PCB the connector and ground lug that go to the Reset Switch/Indicator Assembly.

21. Remove the seven Phillips machine thread screws that attach the I/O Processor PCB to the Electronics Module chassis (one attaches the ground lug at the front right side of the chassis).

    Note: Make sure that on reassembly the insulated standoffs are inserted between the I/O Processor PCB and the metal chassis.

22. Slide the I/O Processor PCB to the rear, exercising care to prevent damage to board components, and remove it from the bottom metal chassis bracket.

23. The three ribbon cable connectors may now be removed from the board. Note the manner in which the cables are routed to clear the connector for the Video/Keyboard Interface PCB. Make sure that on reassembly this routing is followed so that the connector (J0) on I/O Processor PCB is clear.

24. Reassemble in the reverse order, making sure that all cabling is clear and not pinched between any parts of the metal chassis brackets.

3.8 Keyboard

The Keyboard Assembly is a separate assembly that is attached to the main computer unit by a five-wire cable terminated in a DIN plug. A coiled cable assembly allows the keyboard to be separated from the main computer unit by up to three feet.

To disassemble the keyboard, proceed as follows:

1. Turn the keyboard upside down on a padded surface to prevent damage to the keypads.

2. Remove from the underside of the assembly the seven screws that tie the two halves of the keyboard together.

3. Hold the two halves together and turn them right-side up.

4. Lift off the top cover.

5. Lift off the black keyboard bezel.

6. Disconnect the connector from the PCB and remove the keyboard/PCB assembly from the keyboard base.

7. On reassembly, be sure that the pins on the keyboard/PCB assembly are properly seated in the four mounting bosses of the keyboard base before installing the top cover.

8. Reassemble in the reverse order of disassembly.

4/ Adjustments

The only adjustments on the TANDY 6000/6000-HD Microcomputer are associated with the Floppy Disk Drive Interface and are required to be made only if disk drives are changed or components have drifted due to aging. The adjustments are located on the I/O Processor PCB and in the standard unit are not accessible without removing the card cage assembly. It is not necessary to have the unit completely interconnected in order to make these adjustments. The only requirement is that power be supplied to the I/O Processor PCB. Follow the procedure noted below to achieve the correct adjustments.

Exercise care in moving the cables that will run over the components that require adjustment. Make sure that no cables are pulled loose when gaining access for the adjustments. (See Figure 4-1.)

1. Move the Video/Keyboard Interface PCB to the first unused slot below the 16-bit CPU and Memory Boards, or completely remove the PCB.

2. Turn power ON and engage the manual RESET on the front panel. Move the jumper from the storage position E31-E49 to the test position E30-E31.

3. Connect a scope to test point TP9 (located on the right side of the board looking from the rear of the unit) and verify the presence of a square wave pulse train.

4. Connect a frequency counter to TP9 and adjust C61 (located in the middle of the board just to the left of jumper installed in Step 2) for a frequency of 265 KHz, if less than 60 seconds has elapsed since power was turned on. If more than 60 seconds has elaspsed since power was applied, wait at least eight minutes and adjust to 255 KHz.

5. Hard disk alignment is covered in the Appendix C Hard Disk Assembly (OEM Operating and Service Manual)

6. Connect the scope lead to test point TP10 (located just to the right of TP9 looking from the rear of the unit).

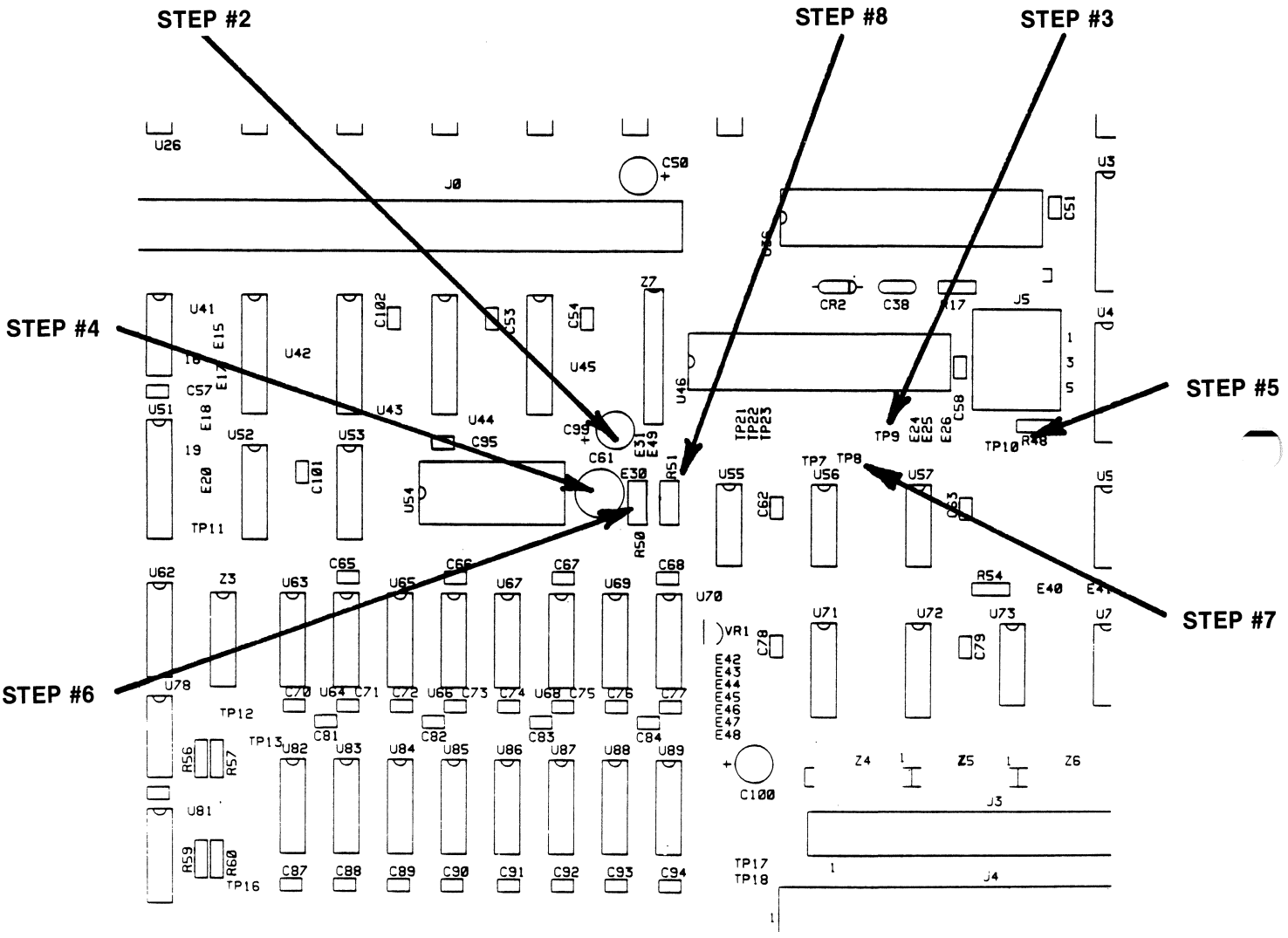


Figure 4-1. Adjustments

7. Adjust R50 (located just to the right of C61 looking from the rear of the unit) for a positive pulse width of 200 nanoseconds.

8. Connect the scope lead to test point TP8 (located just to the left of TP9 looking from the rear of the unit).

9. Adjust R51 (located just to the right of R50 looking from the rear of the unit) for a positive pulse width of 500 nanoseconds.

10. Remove the jumper installed between points E30 and E31 and reposition it between points E31 and E49.

11. Turn power OFF and ensure that all components of the TANDY 6000/6000-HD are electrically interconnected properly. It is not necessary at this time to mechanically reassemble the unit.

12. Turn the power ON. Re-install Video Board, if removed in step 1.

13. When the screen shows "INSERT DISKETTE", insert the test floppy diskette and boot up the system.

14. Run the following test to verify adjustments:

    DISKDG8 (You will need one or two blank double-sided diskettes to run this rest.)

15. If the test is completed correctly, reassemble the TANDY 6000/6000-HD mechanical components in the reverse order of disassembly noted at the first part of this procedure or reinstall the cards removed.

To verify complete operation of the TANDY 6000/6000-HD, run the following tests:

SYSTEM (need serial loop-back and PRINTER-FDC EXT TEST cable)

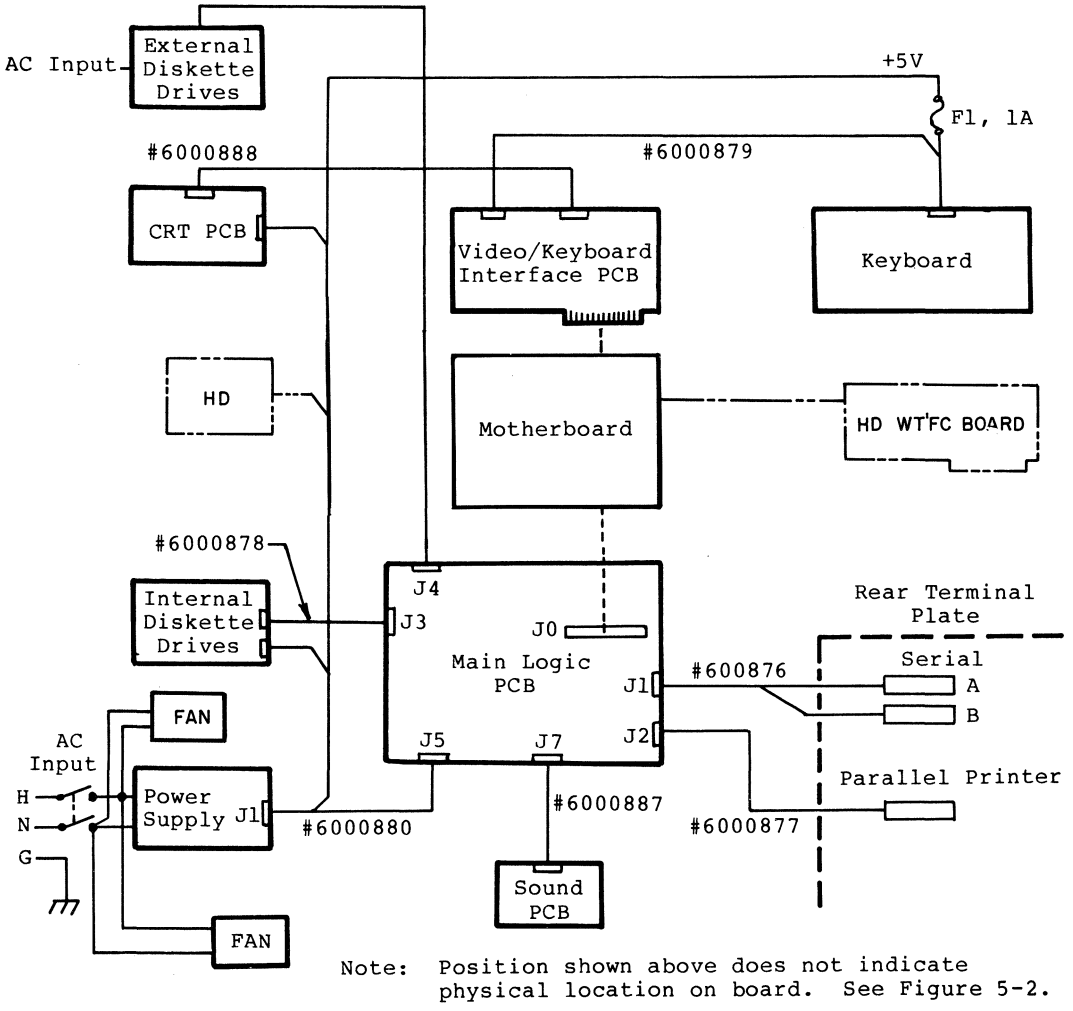
MEM II

DISKDG8 (One double-sided diskette per drive is required.)

HQII/HDREL (hard drive diagnostics)

5/ Cabling Diagrams/Pin Designations

Contained in this section is a cable block diagram of the TANDY 6000/6000-HD System, and pin designations of all the connectors of the TANDY 6000/6000-HD. The Video/Keyboard Interface PCB plugs into the Mother Board. The Mother Board plugs into the Main Logic PCB at connector J0. All other connections are cable connectors that plug into receptacles on the various boards of the system.



Note: Position shown above does not indicate physical location on board. See Figure 5-2.

Figure 5-1. Cable Interconnection Layout

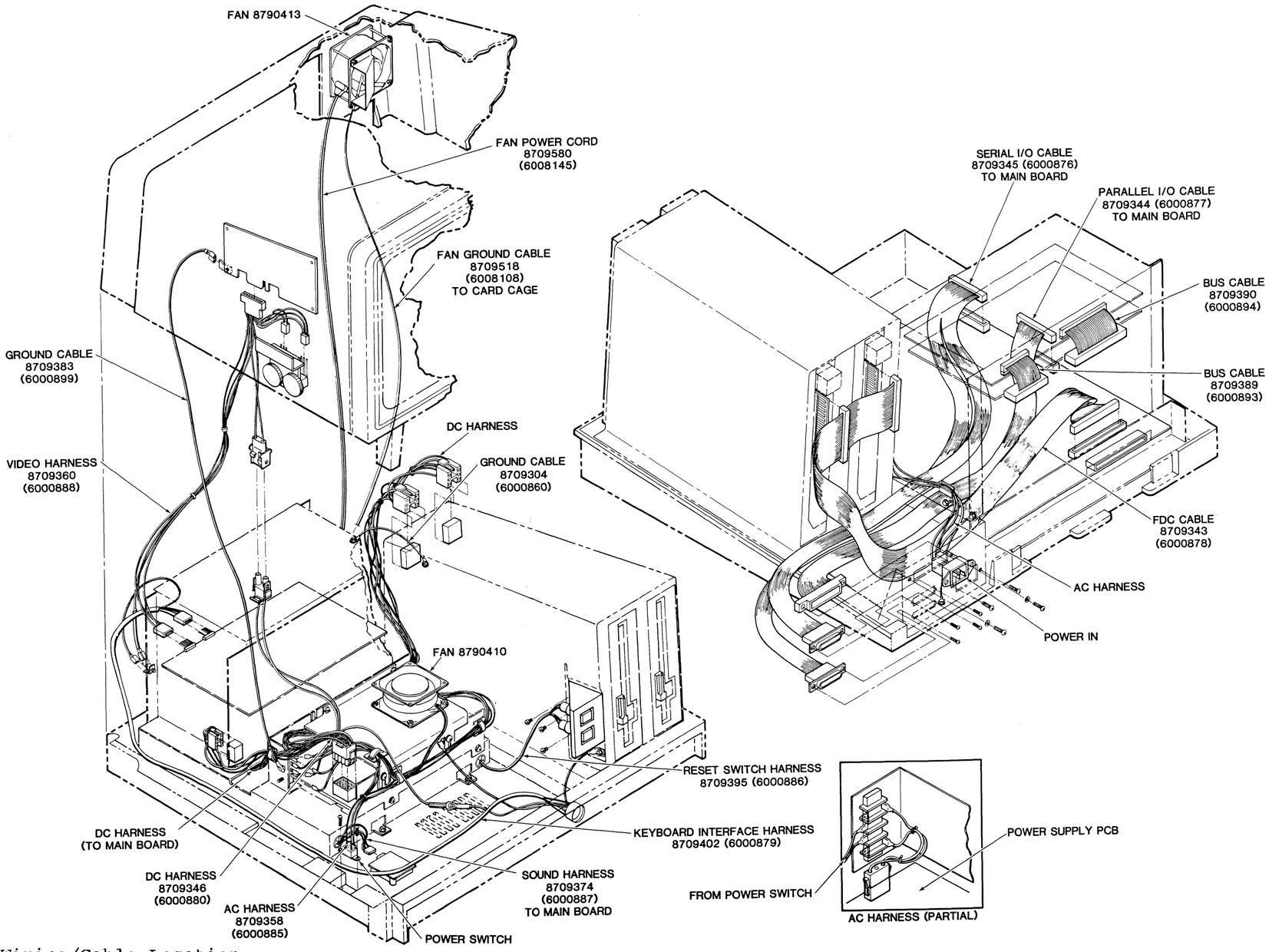


Figure 5-2. Cable Wiring/Cable Location - Floppy Disk Drives Version 1

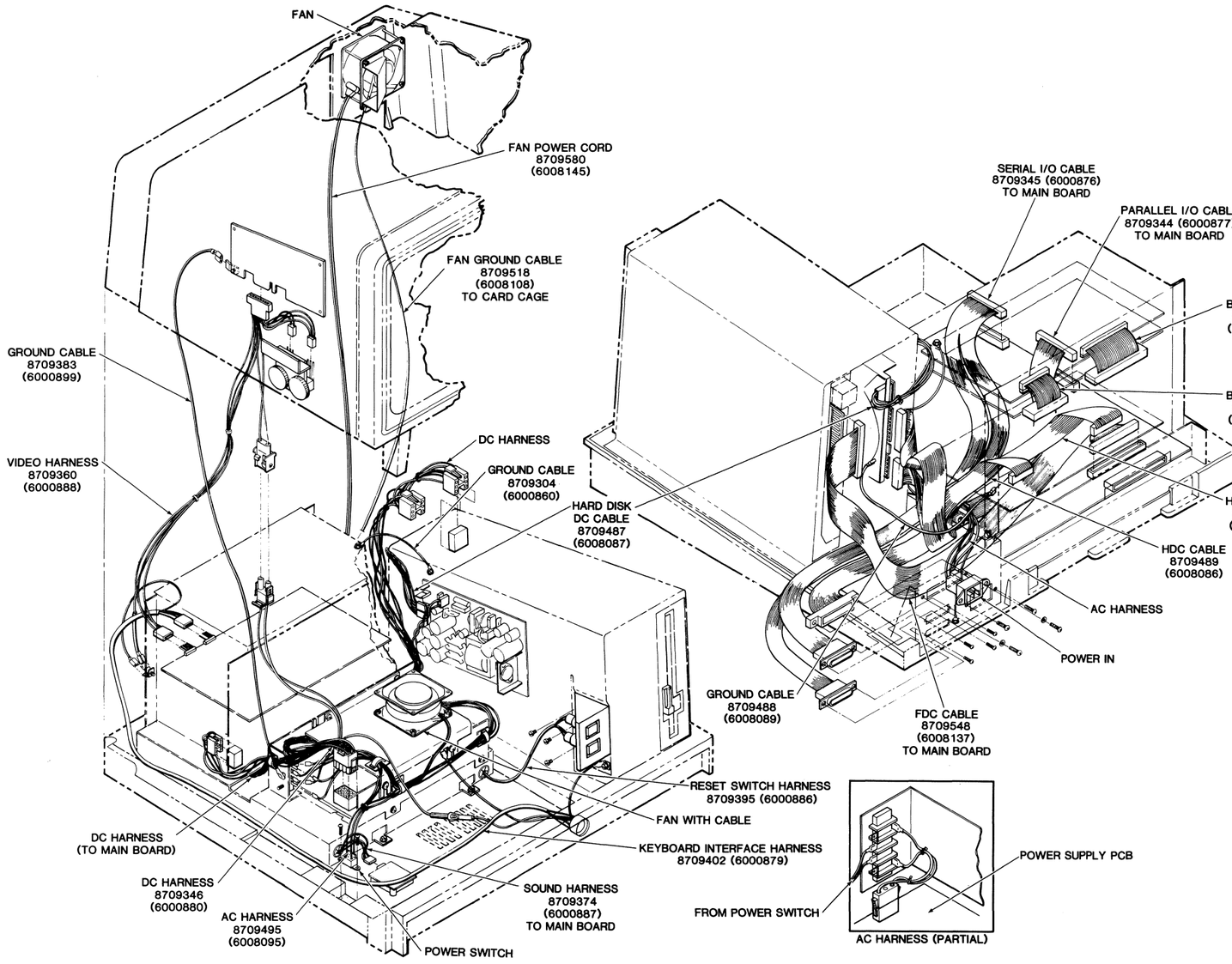


Figure 5-3. Cable Wiring/Cable Location - Hard Disk Drives Version 1

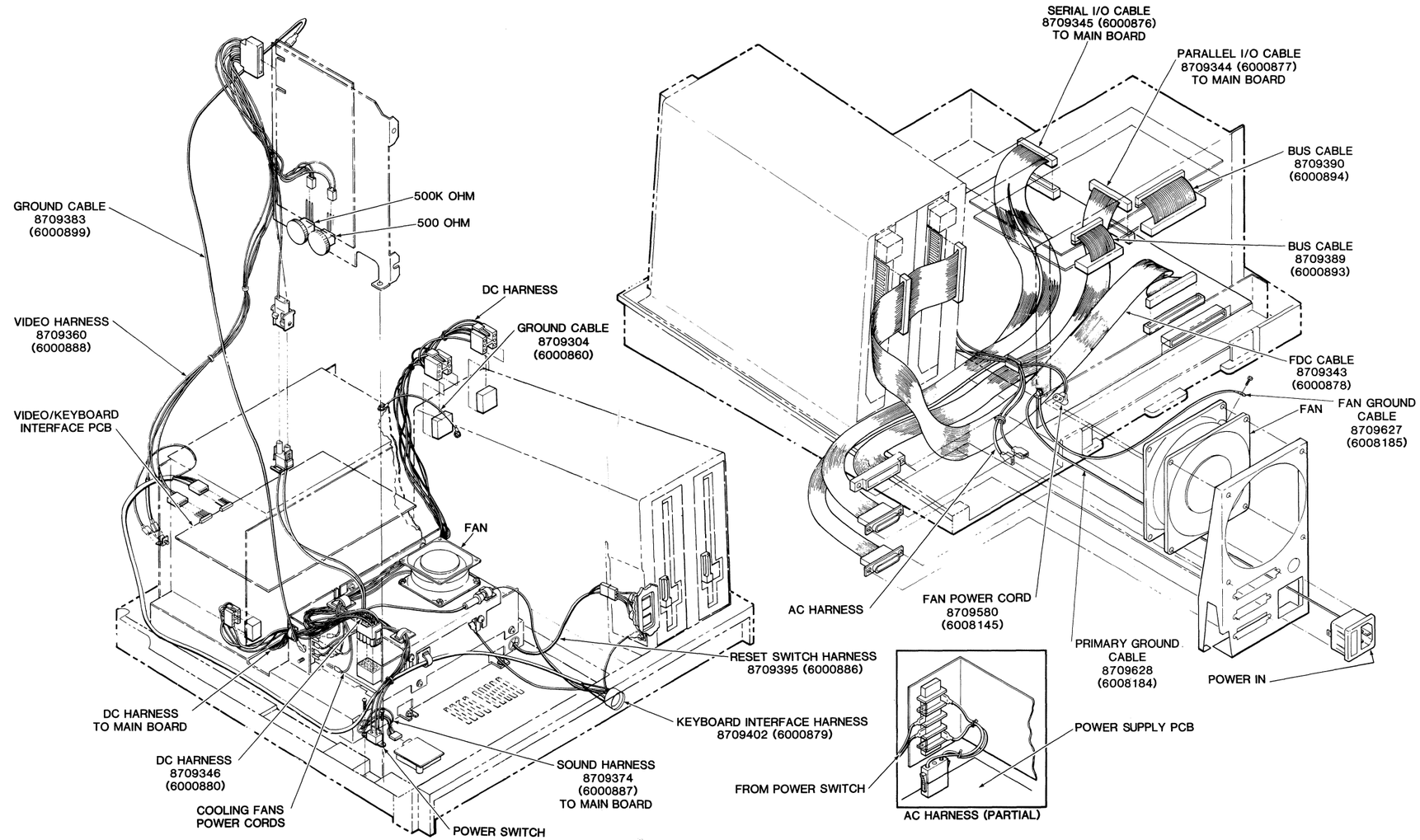


Figure 5-4. Cable Wiring/Cable Location - Floppy Disk Drives Version 2

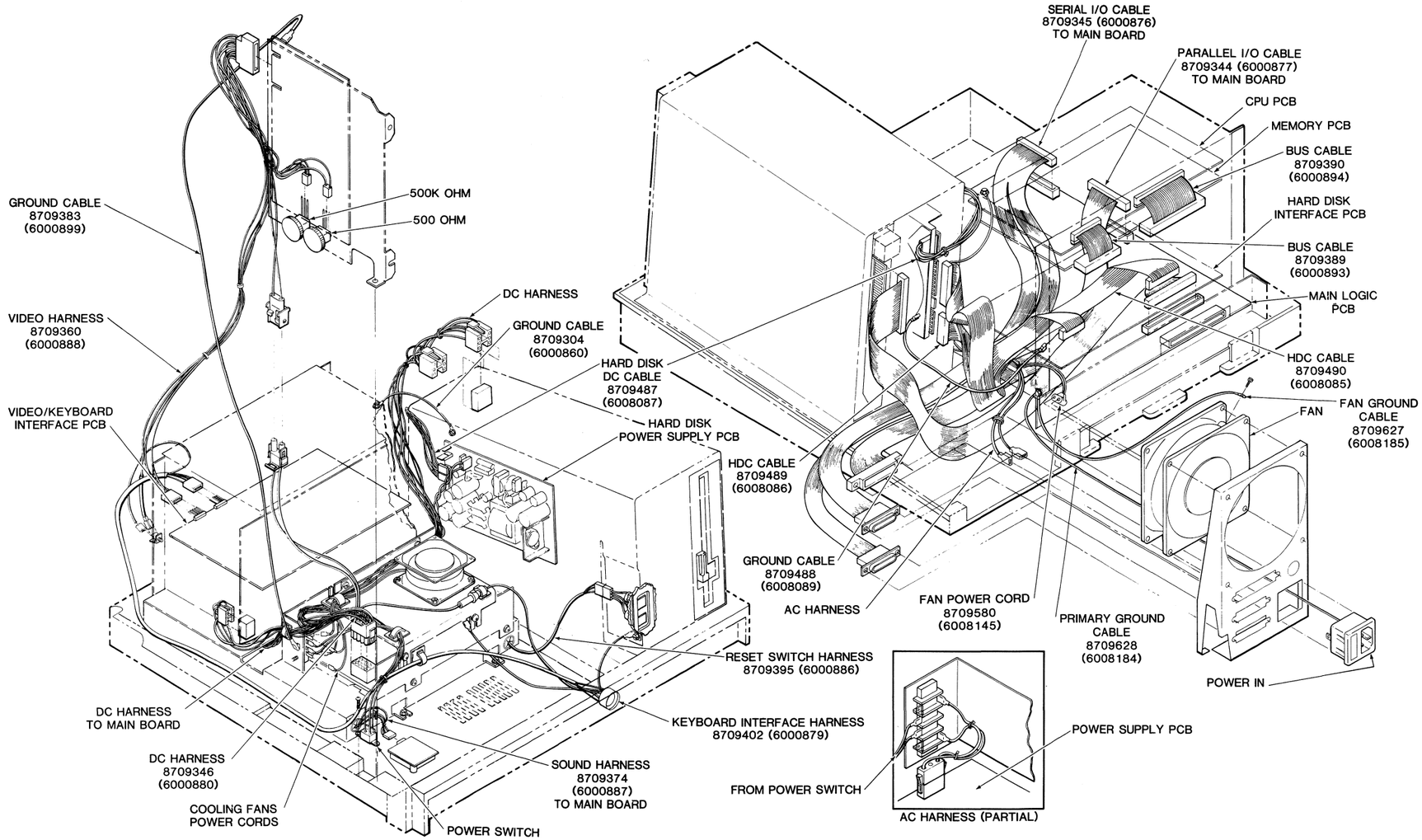


Figure 5-5. Cable Wiring/Cable Location - Hard Disk Drives Version 2

Cable Assembly 8000876, RS-232 Serial Interface

Main PCB Connector P1/J1			Rear Input Channel A
Pin	Name	Description	Pin Number
1	GND	Power Ground	1
2	-	No Connection	14
3	TDCA	Transmit Data, Channel A	2
4	TSET	Transmit S.E.T.	15
5	RDCA	Received Data, Channel A	3
6	-	No Connection	16
7	RTSA	Request to Send, Channel A	4
8	RCLKA	Receiver Clock, Channel A	17
9	CTSA	Clear To Send, Channel A	5
10	-	No Connection	18
11	DSRA	Data Set Ready, Channel A	6
12	-	No Connection	19
13	GND	Power Ground	7
14	DTRA	Data Terminal Ready, Channel A	20
15	CDETA	Carrier Detect, Channel A	8
16-21		No Connection	
22	TCLKA	Transmit Clock, Channel A	24
23		No Connection	12
24		No Connection	25
25	-	GND	13
			Rear Input Channel B
26	GND	Power Ground	1
27	-	No Connection	14
28	TDCB	Transmit Data, Channel B	2
29	-	No Connection	15
30	RDCB	Received Data, Channel B	3
31	-	No Connection	16
32	RTSB	Request to Send, Channel B	4
33	RTCLKB	Rec/Transmit Clock, Channel B	17
34	CTSB	Clear To Send, Channel B	5
35	DSRB	Data Set Ready, Channel B	18
36	-	No Connection	6
37	GND	Ground	19
38	GND	Power Ground	7
39	DTRB	Data Terminal Ready, Channel B	20
40	CDETB	Carrier Detect, Channel B	8

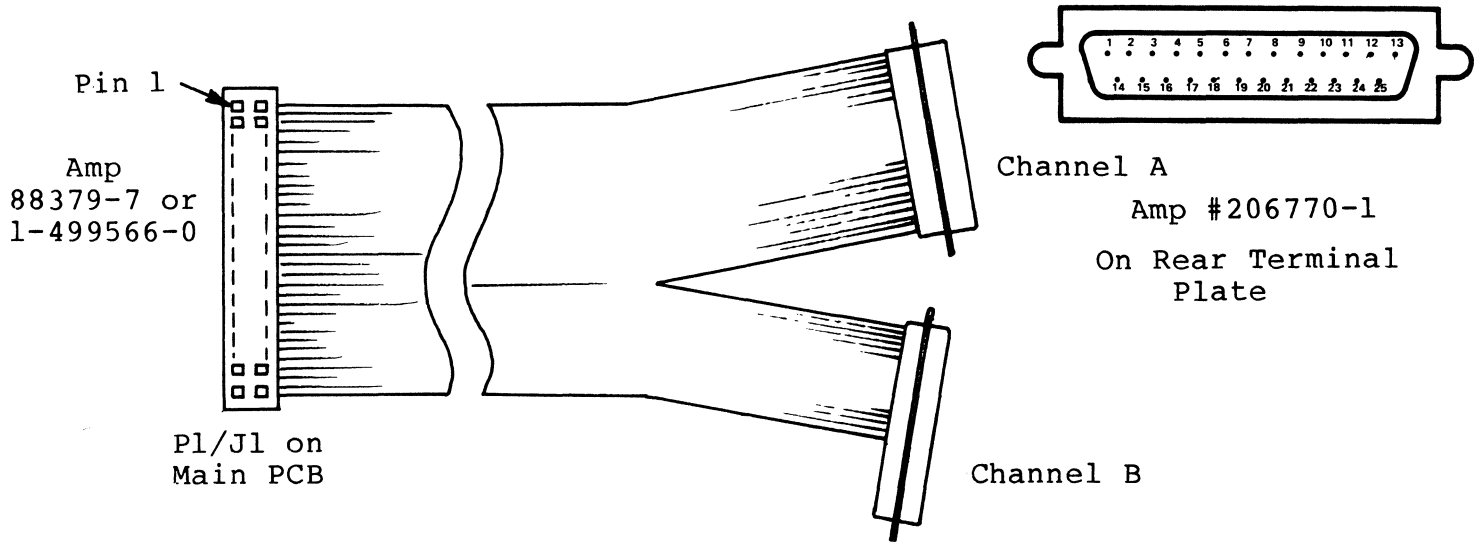


Figure 5-6. RS-232 Serial Interface Cable

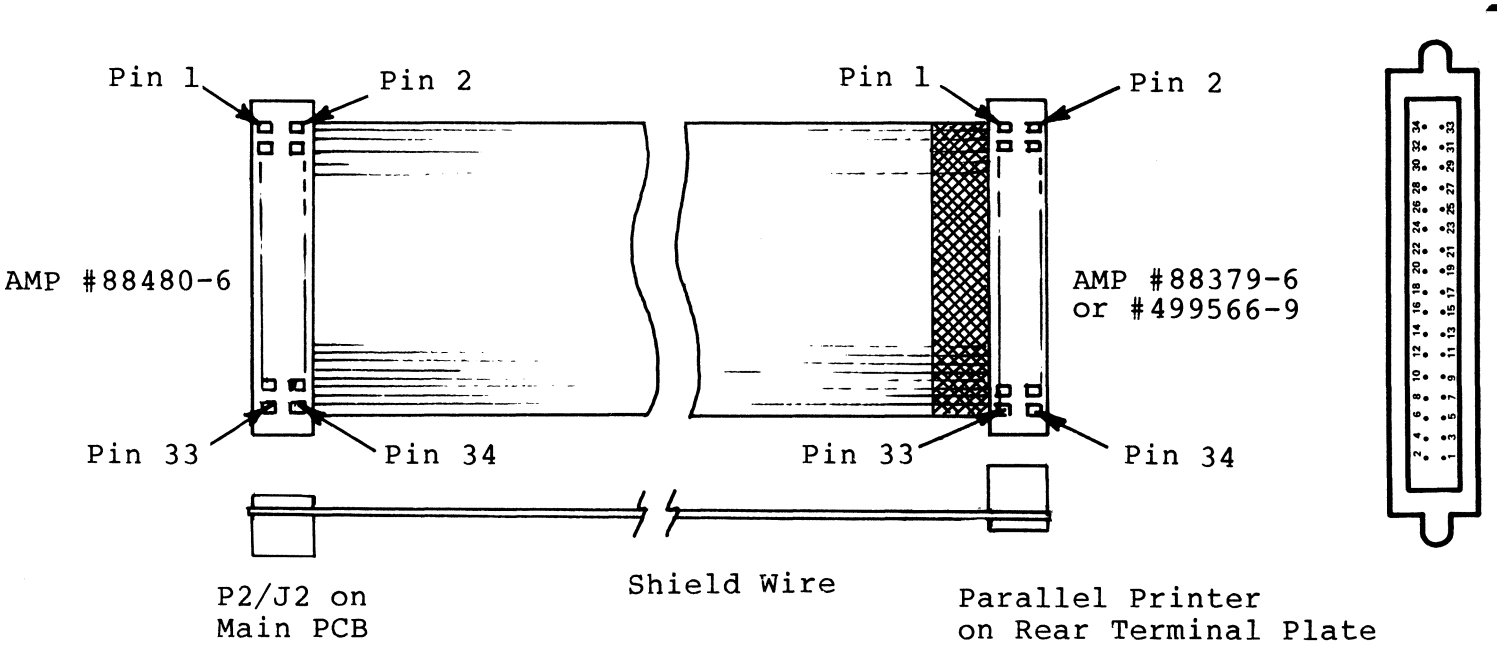


Figure 5-7. Line Printer/Parallel Output Cable

Cable Assembly 6000877, Line Printer/Parallel Output

Wiring for this cable is pin to pin from one connector to the other.

Main PCB P2/J2 to Rear Input Line Printer

Pin	Signal	Description
1	PSTB	Data Strobe
2	GND	Power Ground
3	PDAT0	Data Bit 0 to Printer
4	GND	Power Ground
5	PDAT1	Data Bit 1 to Printer
6	GND	Power Ground
7	PDAT2	Data Bit 2 to Printer
8	GND	Power Ground
9	PDAT3	Data Bit 3 to Printer
10	GND	Power Ground
11	PDAT4	Data Bit 4 to Printer
12	GND	Power Ground
13	PDAT5	Data Bit 5 to Printer
14	GND	Power Ground
15	PDAT6	Data Bit 6 to Printer
16	GND	Power Ground
17	PDAT7	Data Bit 7 to Printer
18	GND	Power Ground
19	PACK*	Printer Data Acknowledge
20	GND	Power Ground
21	BUSY	Printer Busy
22	GND	Power Ground
23	PE	Paper Empty
24	GND	Power Ground
25	PSEL	Printer Selected
26	PRIME	Printer Reset
27	GND	Power Ground
28	FAULT	Printer Fault
29	-	No Connection
30	-	No Connection
31	GND	Power Ground
32	-	No Connection
33	GND	Power Ground
34	-	No Connection

Cable Assembly 6000878, FDC to Internal Drive

Wiring is pin to pin from one connector to the other.
Main PCB P3/J3 to Floppy Diskette Drive(s)

Pin	Name	Description
2	LOCURI*	Reduced Write Current
4,6,8	-	No Connection
10	TWOSIDI*	Two Sided Diskette Installed
12	DSKCHGI*	Drive Door Opened Since Last Select
14	SDSELI*	Side Select;low=side 0, high=side 1
16	-	No Connection
18	HLDI*	Head Load
20	IPI	Index Pulse
22	READYI	Drive Ready
24	-	No Connection
26	DS0I*	Drive Select Zero (Internal)
28	DS1I*	Drive Select One (Internal)
30	DS2E*	Drive Select Two (External)
32	DS3E*	Drive Select Three (External)
34	DIRI*	Step Direction
36	STEP1*	Step Head One Track
38	WDI*	Write Data
40	WGI*	Write Gate
42	TRK0I*	Track Zero Indication
44	WPRTI*	Write Protected Diskette
46	RDI*	Read Data
48,50	-	No Connection

*Inverted or active low. Power Grounds on odd terminals.

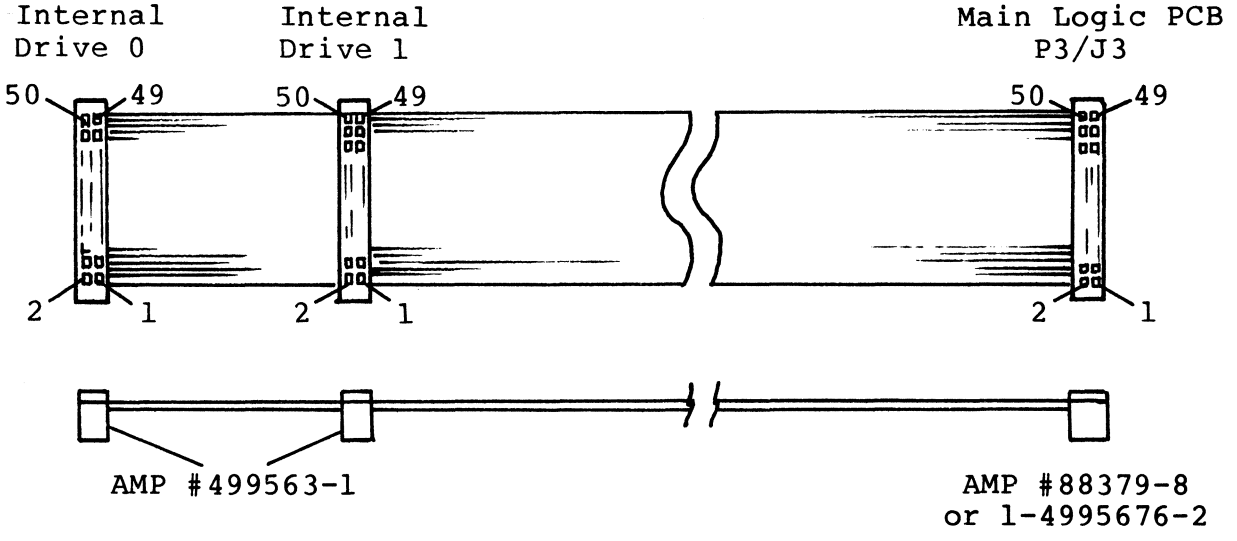


Figure 5-8. FDC to Internal Drive Cable

Cable Assembly 6000879, Video/Keyboard PCB to Keyboard

Video/Keyboard Interface P2/J2			Keyboard Receptacle
Pin	Name	Description	Pin
1	DATA	Data from Keyboard	1
2	-	No Connection	-
3	CLOCK	Clock From Keyboard	2
4	BUSY	Busy to Keyboard	3
	-	+5 Volt	4
5	-	No Connection	-
6	GND	System Ground	5

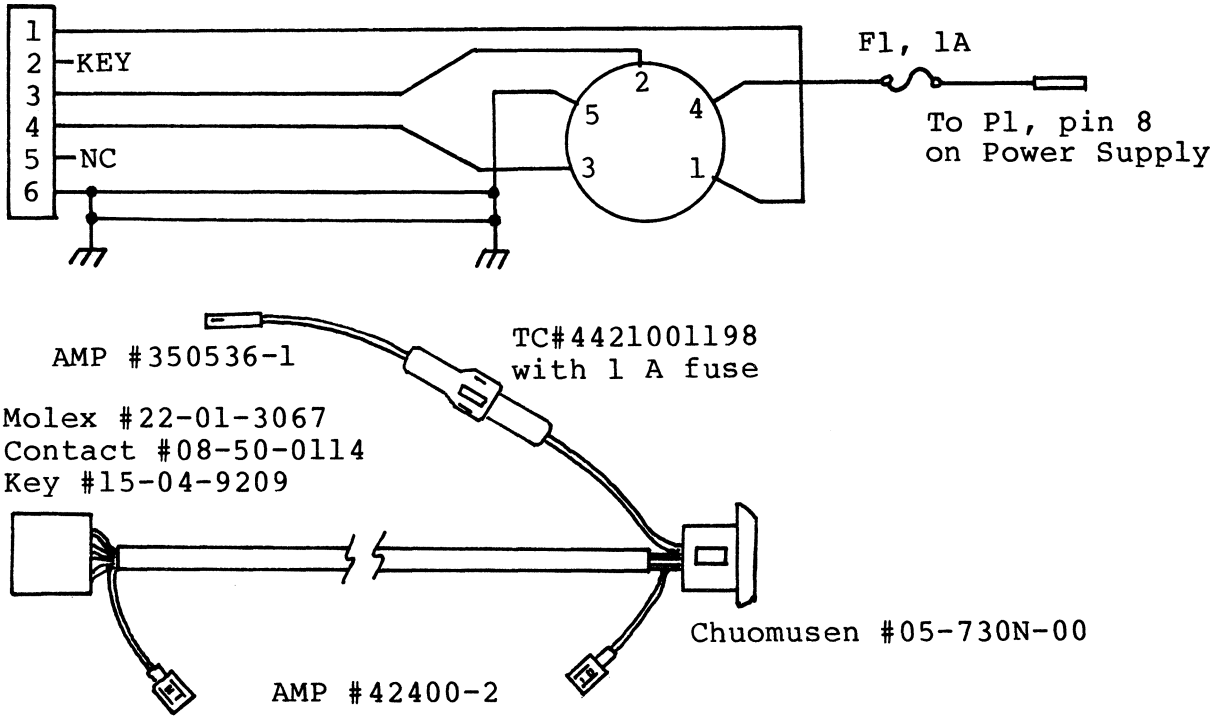


Figure 5-9. Video/Keyboard PCB to Keyboard Cable

Cable Assembly 6000880, DC Power to System

This cable supplies DC power from the Power Supply to the Disk Drives, the CRT Monitor PCB, and the Mother Board. It also supplies +5 volts (at pin 8) to the Keyboard via the keyboard connector on the front panel of the Base Assembly. This voltage is fused by a 1 ampere fuse. All wires in the cable assembly are 18 gage except pins 9, 11, and 12, which are 16 gage (+5 volt supply to Disk Drives and Mother Board.

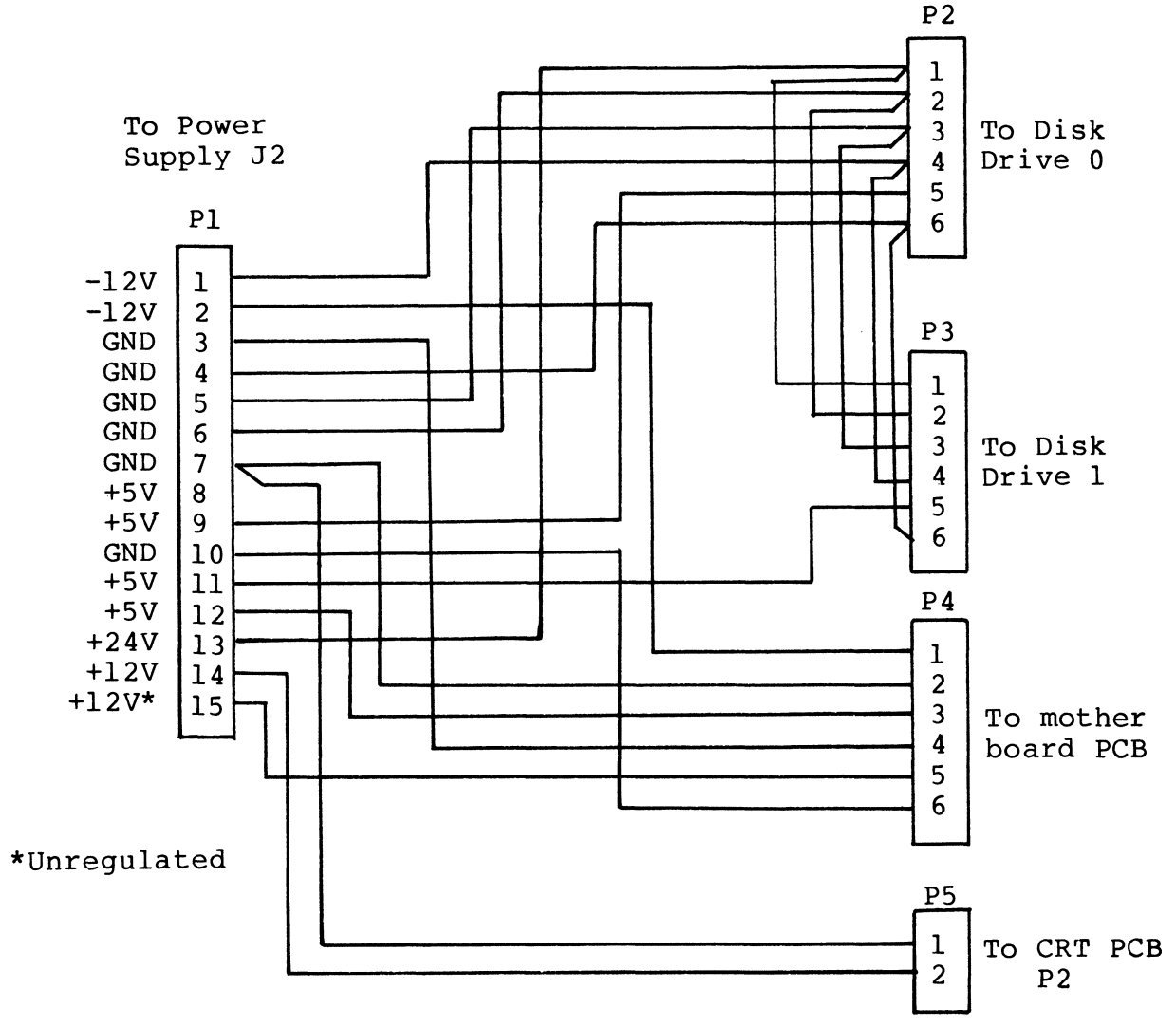


Figure 5-10 DC Power Cable

Cable Assembly 6000885, AC Input

This cable assembly provides switched AC input from the Rear Connector Panel/Fan Support of the TANDY 6000/6000-HD to the Power Supply Assembly. A terminal junction in the circuit after the switch also supplies power to the cooling fan mounted on the Rear Connector Panel/Fan Support. Input wiring is grounded through this cable by a terminal at the Rear Connector Panel. The AC wiring from the Rear Connector Panel is twisted to minimize the effect of magnetic fields.

The terminal strip junction (TB1) is mounted at the left side of the Power Supply on the mounting bracket.

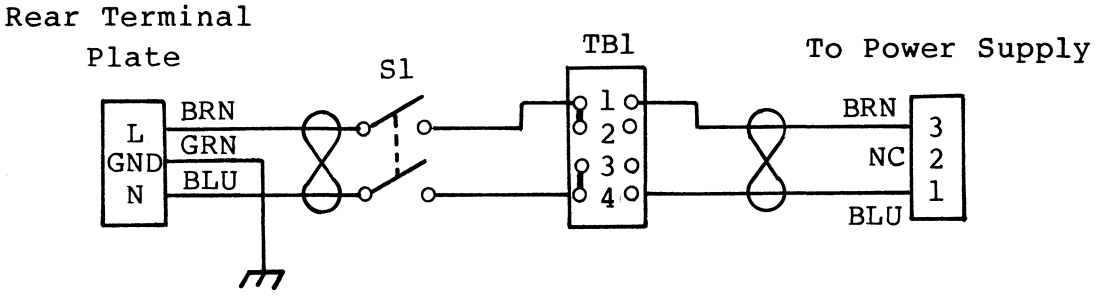


Figure 5-11. AC Input Cable

Cable Assembly 6000887, I/O Processor Board to Sound Board

This cable assembly interconnects the I/O Processor PCB to the Sound Board located at the left front corner of the Base Assembly. The cable is symmetrical and may be connected at either end to the Sound Board.

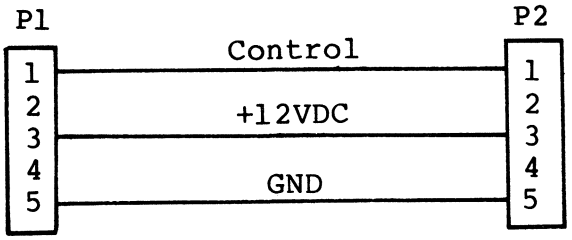


Figure 5-12. I/O Processor Board to Sound Board Cable

Harness Assembly 6000888, Video

The Video Harness contains the wiring that supplies +12 volts to the Video Monitor Assembly, wiring to the brightness and contrast controls mounted on the Base Assembly, and control circuitry from the Video/Keyboard Interface PCB.

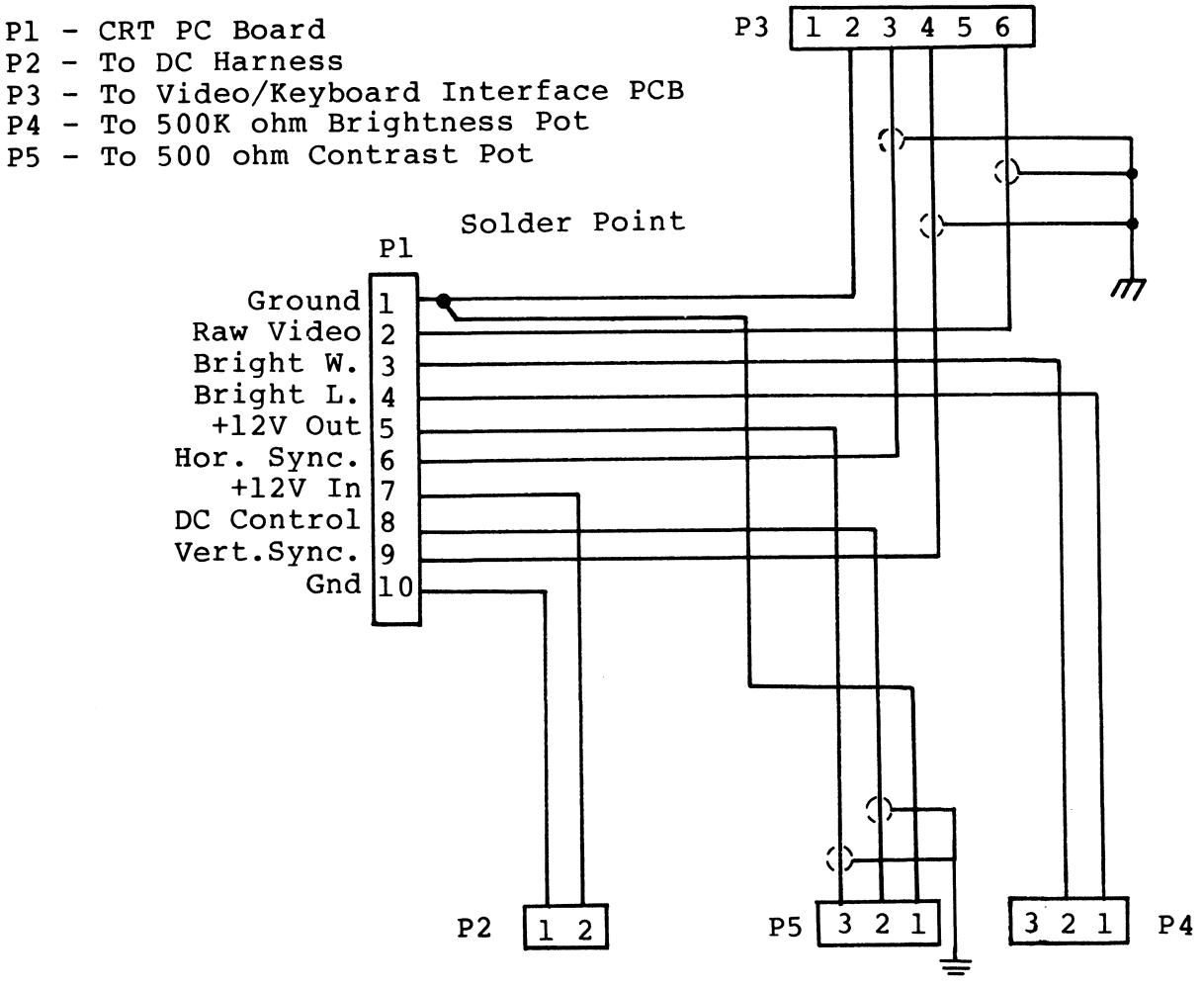


Figure 5-13. Video Cable

Harness Assembly 6008046, Fan Power

The Fan Harness consists of a twisted pair that picks up AC power at the terminal strip on the Power Supply Assembly. It is controlled by the ON-OFF switch located at the left underside lip of the TANDY 6000/6000-HD Base Assembly.

Pin Designations, I/O Processor Board J0, and all Mother Board Connector Positions

This connector accepts the Motherboard Assembly.

Pin	Signal	Description
1	68INTRQ	68000 to Z80 Interrupt Request
2	USER1	User Definable
3	GND	Power Ground
4	GND	Power Ground
5	+12V	Positive 12 Volt Power
6	+12V	Positive 12 Volt Power
7	GND	Power Ground
8	GND	Power Ground
9	+5V	Positive 5 Volt Power
10	+5V	Positive 5 Volt Power
11	INTRQ*	Maskable Interrupt Request (in)
12	NMIRQ*	Non-Maskable Interrupt Request (in)
13	IEIN	Interrupt Enable In (in)
14	IEOUT	Interrupt Enable Out (out)
15	BAKIN*	Bus Acknowledge In (in)
16	BAKOUT*	Bus Acknowledge Out (out)
17	BUSRQ*	Bus Request (in)
18	SYNC*	Z-80 M1 (indicates Op-Code Fetch) (out)
19	RD*	Read In Progress (out)
20	WR*	Write In Progress (out)
21	MEMCYC*	Z-80 MEMRQ (Memory Cycle In Progress) (out)
22	IOCYC*	Z-80 IORQ (I/O Cycle In Progress) (out)
23	A00*	Address Bit 0 Inverted (out)
24	A01*	Address Bit 1 Inverted (out)
25	A02*	Address Bit 2 Inverted (out)
26	A03*	Address Bit 3 Inverted (out)
27	A04*	Address Bit 4 Inverted (out)
28	A05*	Address Bit 5 Inverted (out)
29	A06*	Address Bit 6 Inverted (out)
30	A07*	Address Bit 7 Inverted (out)
31	A08*	Address Bit 8 Inverted (out)
32	A09*	Address Bit 9 Inverted (out)
33	A10*	Address Bit 10 Inverted (out)
34	A11*	Address Bit 11 Inverted (out)
35	A12*	Address Bit 12 Inverted (out)
36	A13*	Address Bit 13 Inverted (out)
37	A14*	Address Bit 14 Inverted (out)
38	A15*	Address Bit 15 Inverted (out)
39	RES	Reserved for System Expansion
40	DISRO*	Disable RAM Output (in)

Pin Designations, I/O Processor Board J0, and all Mother Board Connector Positions

(con't)

Pin	Signal	Description
41	XFERRQ	DMA Transfer Request (in)
42	KBIRQ*	Keyboard Interrupt Request (in)
43	SELECT*	Keyboard Selected (out)
44	CLOCK	4MHz System Clock (out)
45	REFRSH*	Z-80 RAM Refresh Signal (out)
46	8MHz	Times Two System Clock (out)
47	RTC	Real Time Clock Heart Beat (30 or 60Hz)(out)
48	WAIT*	Z-80 Wait Request (in)
49	GND	Power Ground
50	GND	Power Ground
51	DAT0*	Data Bit 0 Inverted (input/output)
52	DAT1*	Data Bit 1 Inverted (input/output)
53	DAT2*	Data Bit 2 Inverted (input/output)
54	DAT3*	Data Bit 3 Inverted (input/output)
55	DAT4*	Data Bit 4 Inverted (input/output)
56	DAT5	Data Bit 5 Inverted (input/output)
57	DAT6*	Data Bit 6 Inverted (input/output)
58	DAT7*	Data Bit 7 Inverted (input/output)
59	DAT8*	Data Bit 8 Reserved for System Expansion
60	DAT9*	Data Bit 9 Reserved for System Expansion
61	DAT10	Data Bit 10 Reserved for System Expansion
62	DAT11*	Data Bit 11 Reserved for System Expansion
63	DAT12*	Data Bit 12 Reserved for System Expansion
64	DAT13*	Data Bit 13 Reserved for System Expansion
65	DAT14*	Data Bit 14 Reserved for System Expansion
66	DAT15*	Data Bit 15 Reserved for System Expansion
67	RESET*	System Reset (out)
68	HALT*	Z-80 Halt Indication (out)
69	GND	Power Ground
70	GND	Power Ground
71	+5V	Positive 5 Volt Power
72	+5V	Positive 5 Volt Power
73	GND	Power Ground
74	GND	Power Ground
75	-12V	Negative 12 Volt Power
76	-12V	Negative 12 Volt Power
77	+12V	Positive 12 Volt Power
78	+12V	Positive 12 Volt Power
79	GND	Power Ground
80	GND	Power Ground

Pin Designations, I/O Processor Board J1

Pin	Signal	Description
1	BD1*	Data Bit 1 Inverted (input/output)
2	BD0*	Data Bit 0 Inverted (input/output)
3	BD3*	Data Bit 3 Inverted (input/output)
4	BD2*	Data Bit 2 Inverted (input/output)
5	BD5*	Data Bit 5 Inverted (input/output)
6	BD4*	Data Bit 4 Inverted (input/output)
7	BD7*	Data Bit 7 Inverted (input/output)
8	BD6*	Data Bit 6 Inverted (input/output)
9	BD9*	Data Bit 9 Inverted (input/output)
10	BD8*	Data Bit 8 Inverted (input/output)
11	BD11*	Data Bit 11 Inverted (input/output)
12	BD10*	Data Bit 10 Inverted (input/output)
13	BD13*	Data Bit 13 Inverted (input/output)
14	BD12*	Data Bit 12 Inverted (input/output)
15	BD15*	Data Bit 15 Inverted (input/output)
16	BD14*	Data Bit 14 Inverted (input/output)
17	GND	Signal Ground
18	GND	Signal Ground
19	GND	Signal Ground
20	BAS*	Bus Address Strobe
21	BUDS*	Bus Upper Data Strobe
22	BLDS*	Bus Lower Data Strobe
23	GND	Signal Ground
24	BR/W*	Bus Read/Write Signal
25	BDTACK*	Bus Data Transfer Acknowledge
26	GND	Signal Ground
27	GND	Signal Ground
28	BA1*	Address Bit 1 Inverted (output)
29	BA3*	Address Bit 3 Inverted (output)
30	BA2*	Address Bit 2 Inverted (output)
31	BA5*	Address Bit 5 Inverted (output)
32	BA4*	Address Bit 4 Inverted (output)
33	BA7*	Address Bit 7 Inverted (output)
34	BA6*	Address Bit 6 Inverted (output)
35	BA9*	Address Bit 9 Inverted (output)
36	BA8*	Address Bit 8 Inverted (output)
37	BA11*	Address Bit 11 Inverted (output)
38	BA10*	Address Bit 10 Inverted (output)
39	BA13*	Address Bit 13 Inverted (output)
40	BA12*	Address Bit 12 Inverted (output)
41	BA15*	Address Bit 15 Inverted (output)
42	BA14*	Address Bit 14 Inverted (output)
43	BA17*	Address Bit 17 Inverted (output)
44	BA16*	Address Bit 16 Inverted (output)
45	BA19*	Address Bit 19 Inverted (output)
46	BA18*	Address Bit 18 Inverted (output)
47	BA21*	Address Bit 21 Inverted (output)

48	BA20*	Address Bit 20 Inverted (output)
49	BA23*	Address Bit 23 Inverted (output)
50	BA22*	Address Bit 22 Inverted (output)

Pin Designations, I/O Processor Board J2

Pin	Signal	Description
1	BVMA*	Bus Valid Memory Address
2	GND	Signal Ground
3	BE	Bus 6800 Peripheral Enable
4	VPA*	Valid peripheral Address
5	GND	Signal Ground
6	BRESET*	Bus 68000 System Reset
7	HALT*	68000 Halt Signal
8	BERR*	Bus Error Signal
9	GND	Signal Ground
10	PCLOCK	68000 Processor Clock
11	GND	Signal Ground
12	BINTAK*	Bus Interrupt Acknowledge
13	GND	Signal Ground
14	BR0*	Bus Request Level 0
15	BG0*	Bus Grant Level 0
16	BR1*	Bus Request Level 1
17	BG1*	Bus Grant Level 1
18	BR2*	Bus Request Level 2
19	BG2*	Bus Grant Level 2
20	RES	Reserved
21	RES	Reserved
22	GND	Signal Ground
23	GND	Signal Ground
24	IRQ8*	Interrupt Request Level 8
25	IRQ7*	Interrupt Request Level 7
26	IRQ6*	Interrupt Request Level 6
27	IRQ5*	Interrupt Request Level 5
28	IRQ4*	Interrupt Request Level 4(Parity Error Int.)
29	IRQ3*	Interrupt Request Level 3
30	IRQ2*	Interrupt Request Level 2
31	IRQ1*	Interrupt Request Level 1
32	BREFRESH*	Bus 68000 Memory Refresh
33	BERR*	Bus Error Signal
34	GND	Signal Ground

Pin Designations, I/O Processor Board J4

Pin designations for this connector are the same as those for cable assembly 6000878 except for the Name designations. All references to I become E for this connector.

Example:
LOCURI* is now LOCURE*
TWOSIDI* is now TWOSIDE*, etc.

6/ Troubleshooting Procedures

6.1 TANDY 6000/6000-HD I/O Processor System

This section of the manual will guide service personnel through the system checkout procedure. The troubleshooting steps are organized in a flowchart manner. Following these steps will guide you to the faulty component or components. This procedure is intended to isolate only to the field replaceable units such as the power supply, i/o processor board, socketed ICs, etc. The following sections describe the theory of operation and troubleshootng for the I/O Processor System. The 16-bit CPU and Memory Boards are covered in section 6.2.

6.1.1 Setup

First, disconnect the unit from the AC power source. Next, separate the Top Cover Assembly from the Base Assembly. See Section 3 for complete instructions on disassembly. Verify the monitor remains electrically connected to the Video/Keyboard PCB and the Power Supply. Verify there are no disk(s) inserted in the drive(s). Verify that the power switch on the underside of the left lip of the Base assembly is OFF, then connect the unit to the AC source and continue.

6.1.2 Power-on Diagnostics

When the power switch on the TANDY 6000/6000-HD is turned ON, the microprocessor starts executing the program in the BOOTSTRAP ROM. This program is divided into several sections that are executed in order if the previous section passed. These diagnostics are of a stair-step nature in that individual functions are tested before being put together to perform the complete task. This will be detailed in the following paragraphs.

1. Power ON. System RESET furnished by the hardware is applied. This causes the Z80 to begin executing program code from the BOOTSTRAP ROM at address 0000H.

2. The initialization of the system begins by disabling interrupts and deselecting all RAM memory but Page 0.

3. Initialize CRTC (CRT Controller). Specify horizontal sync, vertical sync, enable video, select 80 character mode, white-out the entire screen.

4. Check ROM integrity by calculating checksum and comparing it against a value in the ROM. If it matches, continue. If there is a mismatch, the unit will print "BOOT ERROR CK" and stop.

5. Check integrity of Z80 registers by passing a specific bit pattern from register to register. If it passes unchanged, continue. If different, unit will print "BOOT ERROR Z8" and stop.

6. Check lower RAM (1000H to 7000H, i.e, above ROM) by reading a memory location, complement the data and write back into memory, compare memory with accumulator and then return memory location to original contents.

7. Flush the KEYBOARD of any/all extraneous characters due to power-up.

8. Initialize the HARD DISK (if available) and FLOPPY DISK systems. Software reset the controllers, seek track 5, then issue "restore" commands (set heads to track 0).

Now, the system is ready to boot the operating system. The floppy disk controller is set to single density recording mode. If the system is to boot from the FLOPPY DISK, the words "INSERT DISKETTE" are printed in the middle of the all-white screen. When a diskette is inserted and the drive latch closed, the system begins to boot, indicated by a "blank" screen with a blinking cursor in the middle.

The floppy disk drive controller commands the head to move to Track 0. After a 3 second wait, a status is taken.

1. If the drive status is "busy", "not track 0", or "seek error", the message "BOOT ERROR DC" is displayed on the screen.

2. If the drive status is "not ready", the message "BOOT ERROR D0" is displayed.

If everything is in order, then the controller is directed to read data from track 0 and place it in the RAM .

1. If a "record" is not found (no properly formatted data was readable from disk), the message "BOOT ERROR TK" is displayed.

2. If all the records are not found, the message "BOOT ERROR LD" - lost data - is displayed.

3. If a CRC error occurs, the data from the floppy disk was read incorrectly and the message "BOOT ERROR SC" is displayed.

After the data is successfully loaded into RAM, then:

4. The data strings "BOOT" and "DIAG" are looked for. If both are found, the process continues. If these strings are not found, the screen will display the message "BOOT ERROR RS" - Not a Radio Shack diskette.

The data read in from the disk is a "diagnostic" routine that tests the DMA, PIO functions and the RAM memory. (This is all that is required to load the operating system using a polled, non-interrupt method). The memory is tested from 2000H up to FFFFH. This is to determine if the system memory size is 32k or 64k and operational. The following error messages can occur:

1. "BOOT ERROR DM" - DMA failed.
2. "BOOT ERROR PI" - PIO failed.
3. "BOOT ERROR LM" - lower memory failed.
4. "BOOT ERROR HM" - higher memory failed.

Now if at least 32k of memory was found ok (i.e. memory errors occurred on a word boundary and above address 8000H), the message "32K MEMORY" is displayed in the center of the screen. If all 64K of memory responds, the message "64K MEMORY" is displayed. Either of these messages indicates the diagnostic has passed.

Next, the message "LOADING" or "INITIALIZING" is displayed in the upper left corner of the screen indicating that a "loader" routine is being read in to load the operating system.

A word of caution. If the OS is TRSDOS 4.0 or later, then an extra 16K of memory above 64K is required but not tested for. As a result, if this memory

does not exist or is bad, the loading process may not be completed and no error messages will be displayed. The machine "hangs up" with "LOADING" message in the upper left corner of the CRT. The extra memory required for the 4.X operating system will be a 16K byte segment of Z80 memory or the 16-bit CPU's memory.

A complete listing of the possible error messages that can occur is tabulated below.

Hard Disk Errors

HT	Timeout waiting for ready
HC	CRC error - data
HI	CRC error - ID
HN	ID not found
HA	Aborted command
HO	Track 0 error
HM	Data Address mark not found
HD	Any other error

Floppy Disk Errors

DC	FDC or drive error - busy not reset
DO	Drive not ready
SC	CRC error
TK	Record not found reading track 0
LD	Lost data on read from floppy
RS	Not Radio Shack format disk

Other Errors

CK	Bad ROM checksum
Z8	CPU failure
MF	RAM failure
ML 01	Low RAM failure (0-3FF)
MH 02	High RAM failure
DM 03	DMA data failure
DM 13	DMA - No interrupt
DM 23	DMA - Extra interrupt
PI 04	PIO data failure
PI 14	PIO - No interrupt
PI 24	PIO - Extra interrupt
CT 05	CTC - No interrupt ch 0
CT 15	CTC - No interrupt ch 1
CT 25	CTC - No interrupt ch 2
CT 45	CTC - Extra interrupt

TEST PROCEDURES

The following is a list of software routines that will thoroughly test the I/O Processor system.

1. SYSTEM - Version dated 11/29/1982, Tests SIO (serial channels A, B), PIO (printer I/F, external floppy I/F), DMA and Z80 interrupts and bus structure. Special loopback test cables required.

2. MEMII - Version 1.3. Video refresh RAM, Shadow ROM checksum, Checkerboard, Modified address and Coincidence RAM tests and Bank Select Tests.

3. DISKDG8 - Thinline floppy drive tests.

4. DOVIDAL - Video alignment and centering test.

6.2 TANDY 6000/6000-HD CPU and 512K/1 Meg Memory Board

In order to isolate trouble in the TANDY 6000/6000-HD boards, run all current Model II diagnostics. If any failures are detected, refer to the Model II Technical Reference Manual. If the TANDY 6000/6000-HD boards are suspected as being at fault, remove the TANDY 6000/6000-HD CPU and memory boards and rerun the Model II diagnostics to verify the problem area.

If it is determined that the problem area is in the TANDY 6000/6000-HD MC68000 CPU or 512K/1 Meg Memory Board, use the following troubleshooting chart for locating the trouble.

Run Diagnostics	Condition	Possible Fault	Recommended Action
6000/6000HD Memory Test (uses Z80A to test memory)	Test locked-up	Z80A to 68000 interface circuit	Check interface controller U36 and select logic
	Test locked-up	Bus arbitration circuit controller U6	Check latch U7 and bus arbitrator
	Test locked-up	Refresh logic	Check all logic in refresh circuit
	Bad RAM reported	Bad RAM	Calculate and replace bad RAM ICs
	Bad RAM reported	Z80A to MC68000 interface circuit	Check all logic in interface circuit
	Bad RAM reported	Memory board	Refer to Trouble Shooting the TANDY 6000/6000-HD Memory Board
	No errors		Refer to Trouble Shooting the TANDY 6000/6000-HD Memory Board

Run Diagnostics	Condition	Possible Fault	Recommended Action
6000/6000-HD Interrupt Test	Test locked up on software interrupt	Interrupt circuit	Check interrupt controller U15, ICs U34,40,26.
		MC68000 CPU	Replace MC68000
		Clock Logic	Check clock circuit
	Test locked up hardware interrupt	Interrupt circuit	Check interrupt controller U15 and all hardware interrupt inputs into U15
		MC68000 CPU	Replace MC68000
		Clock logic	Check clock circuit
	Software interrupt received was not interrupted generated	Interrupt controller	Replace interrupt controller U15
	Hardware interrupt received was not interrupt generated	Interrupt circuit	Check for shorts on interrupt input lines.
6000/6000-HD OBERROR in user Offset/Limit Test	Offset/Limit range	Check output registers	address lines for shorts
	Protected memory modified	U15, U41	Check listed ICs
	OBERROR not generated	4-bit full adders	Check U23, U24, U38

Run Diagnostics	Condition	Possible Fault	Recommended Action
6000/6000-HD Offset Limit Test	Random errors	I/O decoding and strobes	Check I/O and strobe circuit

Mother Board Troubleshooting

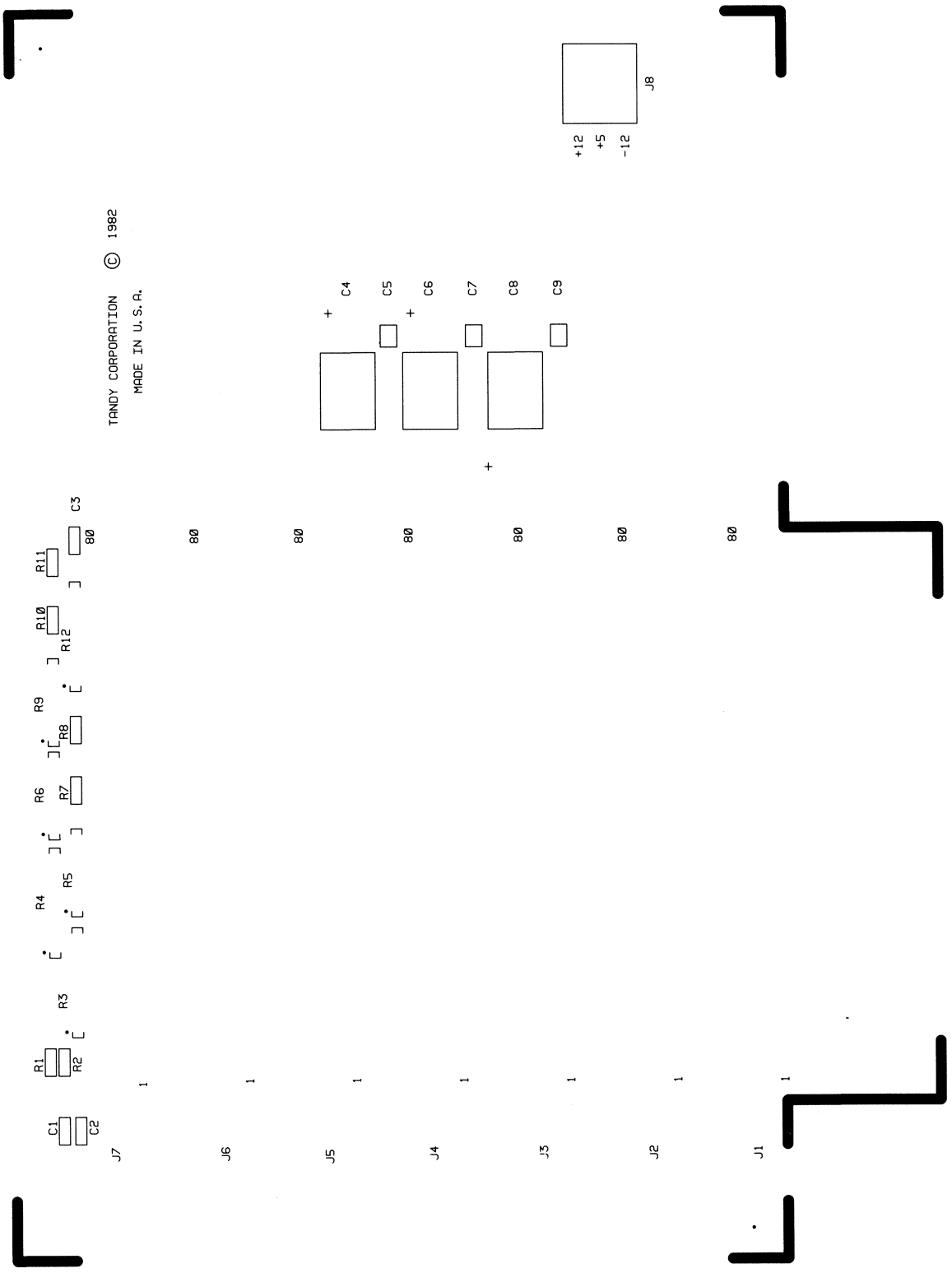
Run Diagnostics	Condition	Possible Fault	Recommended Action
6000/6000-HD Memory Modified Address Test	Bad RAM reported	Bad RAM	Calculate and replace bad RAM ICs
		Data Buffers	Check buffers U5 - U8
		Address Buffers	Check U3, U4 and U9 for A17
		Memory Control	Check U9 and signal control logic and multiplexers

7/ Theory of Operation

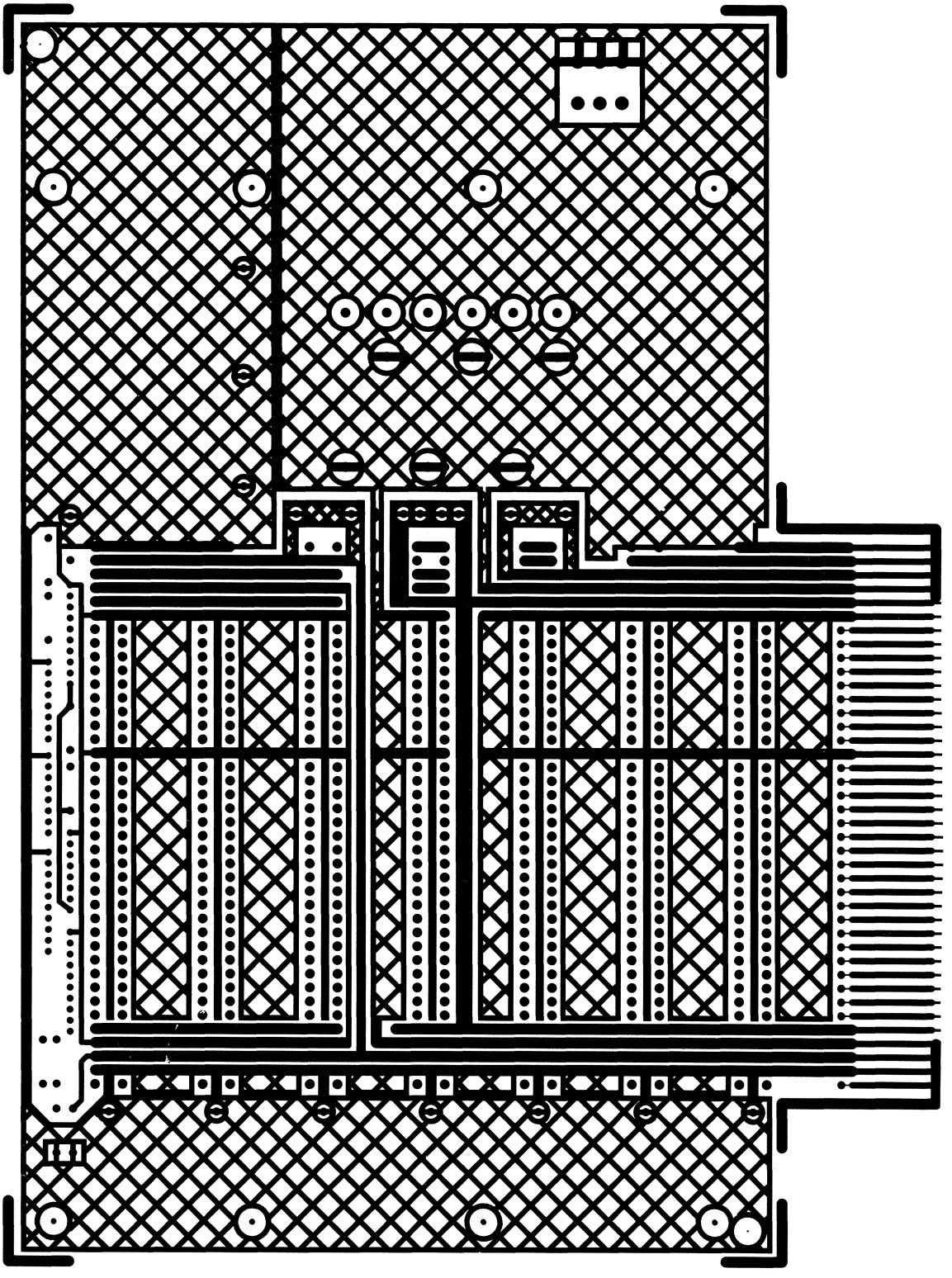
7.1 Mother Board

The mother board contains seven receptacles into which optional boards for the TANDY 6000/6000-HD are plugged. The connector receptacles are numbered from J1 through J7, beginning at the bottom of the board. The power supply input connector, P5, plugs into receptacle J8 at the RH side of the board.

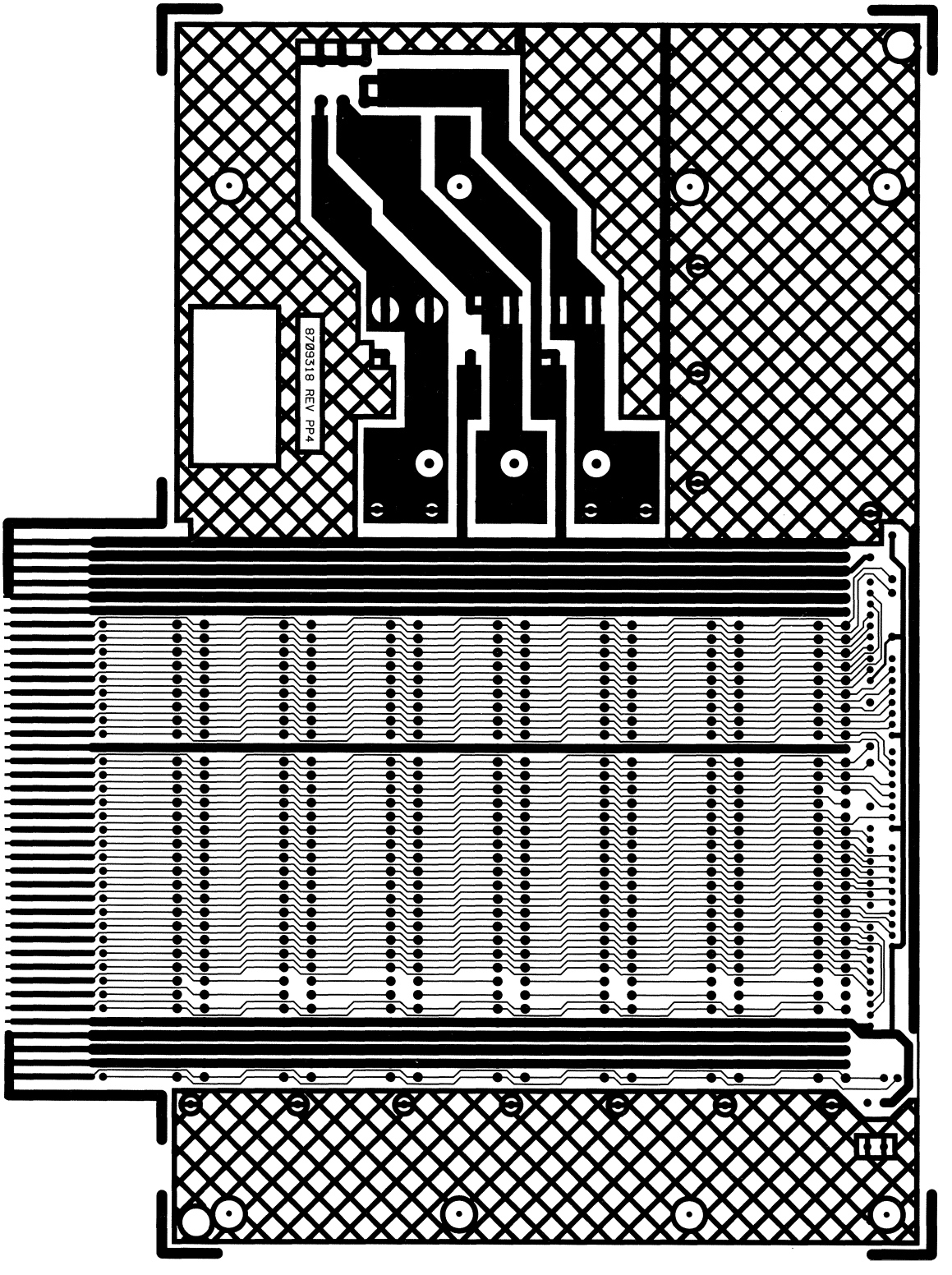
Also included on the mother board are capacitors C4-C9, which serve to additionally filter the input voltage from the power supply. Other resistors and capacitors located at the top of the board serve as signal line terminators.



Component Location, Mother Board 8897701



Circuit Trace, Mother Board 8897701, Component Side



Circuit Trace, Mother Board 8897701, Solder Side

Parts List, Mother Board, 8897701

Ref No.	Description	Part No.
---	PCB, Mother Board	8709318
Capacitors		
C1	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C2	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C3	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C4	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C5	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C6	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C7	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C8	Capacitor, 470 uF, 16V, Elect, Axial	8317471
C9	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
Connectors		
J1	Connector, 80-pin Card Edge	8519014A
J2	Connector, 80-pin Card Edge	8519014A
J3	Connector, 80-pin Card Edge	8519014A
J4	Connector, 80-pin Card Edge	8519014A
J5	Connector, 80-pin Card Edge	8519014A
J6	Connector, 80-pin Card Edge	8519014A
J7	Connector, 80-pin Card Edge	8519014A
J8	Connector, 6-pin Power	8519015
Resistors		
R1	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R2	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R3	Res. Network, 220/330 ohm, 10-pin, SIP	8290019
R4	Res. Network, 220/330 ohm, 10-pin, SIP	8290019
R5	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R6	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R7	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R8	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R9	Res. Network, 220/330 ohm, 8-pin, SIP	8290019
R10	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R11	Resistor, 4.7K ohm, 1/4 W, 5%	8207247
R12	Res. Network, 220/330 ohm, 10-pin, SIP	8290019

7.2 MC68000 CPU Board

The theory of operation for the MC68000 board has been divided into several major sections, each corresponding to a logical unit of LSI, MSI, and SSI parts on the CPU board. They are as follows:

7.2.1 Central Processing Unit (CPU)
7.2.2 Interrupt Logic
7.2.3 Z80A to MC68000 Memory Interface Circuitry
7.2.4 Memory Management Circuitry
7.2.5 Bus Arbitration Logic
7.2.6 Data Transfer Acknowledge Logic
7.2.7 MC68000 I/O Decoding and Strobes
7.2.8 Clock Logic
7.2.9 Refresh Logic
7.2.10 Bus Error Logic

Note: The terms "assertion" and "negation" are used to avoid confusion when talking about active-high or active-low signals. "Assert" or "assertion" is used to indicate a true or active state, regardless of its high or low potential. "Negate" or "negation" indicates a false or inactive state.

7.2.1 Central Processing Unit (CPU)

The TANDY 6000/6000-HD CPU board uses the Motorola MC68000, which contains 16 data lines, 23 address lines, and 20 control lines.

1. Data Lines

The data lines (KD0-KD15) are interfaced to the bus via transceivers U12 and U13 (AMD 8303s). When high, the CD control line (pin 9) on the transceivers tri-states the data bus. This signal is driven by Bus Grant Acknowledge (BGACK), which indicates that a device other than the MC68000 CPU is bus master.

The T/R* control line (pin 11 on the 8303) controls the direction the transceiver is pointing and is driven by Data Bus Transmit/Receive (DBTR). (See sheet 2 of the CPU schematic.) The active-low output DBTR from U9 pin 13 enables the data receivers during an off-board interrupt acknowledge sequence (INTAKL6*) or during a read from external memory.

The active-high state of DBTR enables the data drivers. It follows, therefore, that the data receivers are disabled when:

A read or write is in progress from the Interrupt Controller chip (INTCS*)
A board interrupt acknowledge sequence is in progress (PRIORINTAK*)
A write to external memory (R/W*) occurs

It should be noted that the CD control line overrides the T/R* control line, and that both drivers and receivers are disabled (tri-stated) if BGACK is asserted.

2. Address Lines

The MC68000 address lines are interfaced to the address bus via tranceivers U11, U28, and U30, which are the same type used for the data lines. The CD control line ON U11 AND U28 is connected directly to ground, which always enables address lines KA1-KA11, and KA20-KA23 to the address bus unless BGACK* is active. The CD Input of U30 is controlled by MMA which indicates if the MC68000 is in supervisor or user mode. If it is in supervisor mode U30 is enabled and KA12-KA19 is enabled to BA12-BA19. If it is in the user mode U30 is disabled and BA12-BA19 is driven by the Memory Management Circuitry. Refer to section 7.2.4. The direction control line (T/R*) is switched by BGACK*, which indicates who has bus mastership. If the MC68000 CPU is bus master, then BGACK* is negated and the address lines are driven onto the bus. If an external device is bus master, BGACK* will be asserted and the address contained on the bus will be gated onto the CPU address lines.

The CPU control lines may be divided into six major groups. These are:

Memory Access Control Lines
Bus Arbitration Lines
Interrupt Priority Lines
Function Code Lines
MC68000 Peripheral Interface Lines
System Control Lines

Memory Access Control Lines

The memory access control lines include Address Strobe (AS*), Lower Data Strobe (LDS*), Upper Data Strobe (UDS*), Read/Write (R/W*), and Data Transfer Acknowledge (DTACK*). AS* indicates there is a valid address on the address lines of the MC68000 CPU and it is connected directly to the MC68000 subsystem devices.

The Bus AS* (BAS*) is a delayed AS* which is required to allow the extra time needed for address checking of the memory management unit. AS* is delayed through 4 74F32s to generate GAS*, which is interfaced to the bus by U14.

LDS*, UDS*, and R/W* are directly interfaced to the bus using a non-inverting buffer U14 (ALS244). The enable inputs are controlled by BGACK, which will disable (tri-state) the drivers when an external device is bus master.

LDS* indicates that data bits BD0-BD7 are being accessed, and UDS* indicates that data bits BD8-BD15 are being accessed. If both are asserted at the same time, all 16 data bits are accessed. R/W* indicates whether the data bus transfer is a read or write cycle. An active high indicates a read cycle and an active low indicates a write.

Data Transfer Acknowledge (DTACK*) is the asynchronous handshake signal used by memory and peripheral devices to indicate to the MC68000 that a bus cycle has been completed. DTACK* is connected directly to the bus and becomes BDTACK*. For more details, see Paragraph 7.2.6 Data Transfer Acknowledge Logic.

Bus Arbitration Lines

The bus arbitration lines consist of Bus Request (BR*), Bus Grant (BG*), and Bus Grant Acknowledge (BGACK*). BR* and BGACK* are inputs to the MC68000 CPU and BG* is an output. These signals are used to determine which device will be the next bus master.

All three signals connect with the bus arbitration controller chip U6. This chip interfaces with the bus to provide four levels of bus requests and grants. For details, see Paragraph 7.2.5 Bus Arbitration Logic.

Interrupt Priority Lines

The Interrupt Priority Lines (IPL0*-IPL2*) are CPU inputs that indicate the encoded priority of the interrupt-requesting device. The highest priority is Level 7. Level 0 indicates that interrupts are not requested.

IPL1* is pulled high and IPL0*, IPL2* are tied together which only allows level 5 to be active.

For more details on interrupt operation, see Paragraph 7.2.2 Interrupt Logic.

Function Code Lines

Function Code Lines (FC0, FC1, and FC2) are outputs from the processor chip that feed a 3-to-8 decoder (U34). U34 is used to detect accesses to User Space (either code or data) or to decode the Interrupt Acknowledge sequence (INTAK*).

Bus grant acknowledge (BGACK) disables the decorder to prevent the memory management unit from providing the memory protect function during bus cycles under external control (i.e., Z80A, CPU, or DMA transfers).

MC6800 Peripheral Interface Lines

The MC6800 Peripheral Interface Lines (E, VMA*, and VPA*) allow the CPU to interface easily to MC6800-type devices. The outputs (E and VMA*) are interfaced to the 16-bit bus with a buffer U14. U14's enables are controlled by the BGACK signal.

If BGACK is active, the buffer is disabled and the outputs are tri-stated. Another device is then allowed to drive the bus control lines (i.e., Z80A, CPU, or DMA). The MC6800 Peripheral Interface lines are not currently implemented in the TANDY 6000/6000-HD operation.

System Control Lines

The System Clock input (CLK) to the MC68000 CPU is driven by a 8 MHz output of the clock logic (PCLOCK). The RESET*, HALT*, and BERR* lines are connected directly to the MC86000 bus. These lines are driven in a wired-OR fashion by open collector inverter U33. RESET* and HALT* are directly controlled by the Z80A CPU. This is done by setting or resetting latched bits in a special Z80A I/O port.

RESET* is a bidirectional signal allowing the Z80A I/O port latch or the MC68000 CPU to reset the MC68000 subsystem. For the MC68000 CPU to recognize the assertion of RESET*, HALT* must be asserted at the same time.

HALT* is also a bidirectional signal. When the Z80A I/O port latch asserts HALT*, the MC68000 CPU will stop at the end of the current bus cycle. If HALT* is asserted by the MC68000 CPU, it indicates the processor has stopped, as in the case of a double bus fault. See Paragraph 7.2.3 Z80A to MC68000 Memory Interface Circuitry for more information.

Assertion of Bus Error (BERR*) to the MC68000 CPU indicates that a major error has occurred during the current bus cycle.

Errors can be a result of:

A device that does not respond with BDTACK*.
An attempt by the user to access memory outside the extents defined by the memory management unit.
No interrupt vector received during an interrupt acknowledge sequence.

See Paragraph 7.2.10 Bus Error Logic for more information.

7.2.2 Interrupt Logic

The Interrupt Control function for the MC68000 subsystem is implemented with an AM9519 interrupt controller. A single AM9519 (U15) manages up to eight maskable interrupt request inputs, resolves priorities, and supplies the vector number response to the MC68000 CPU at interrupt acknowledge time. When the AM9519 controller receives an unmasked interrupt request, it issues a group interrupt request to the MC68000 CPU. When the interrupt is acknowledged, the controller outputs the pre-programmed vector number corresponding to the highest-priority unmasked interrupt request.

Operating Mode Register

The mode register in the AM9519 specifies the various combinations of operating options that the programmer may use. The following is a list of the operating options used by the system.

Bit Number	Option
0	Priority Mode
1	Vector Selection
2	Interrupt Mode
3	GINT Polarity
4	IREQ Polarity
5	Selects internal register to be read on subsequent read operation
6	Selects internal register to be read on subsequent read operation
7	Master mask bit that enables or disables all interrupts without modifying the interrupt mask register

Interrupt Request Inputs

Table 7-1 lists, in order from the highest to the lowest priority, the interrupt inputs implemented in the MC68000 subsystem.

For more information, see the AM9519 data sheet section in the AM9500 Peripheral Products Guide published by Advanced Micro Devices.

7.2.3 Z80A to MC68000 Memory Interface Circuitry

Communication between the two CPUs is accomplished with the Z80A CPU initiating interrupts to the MC68000, indicating I/O completion, etc. The Z80A CPU can periodically poll an MC68000 memory location to recognize requests for service from the MC68000.

Optionally, the MC68000 can generate an interrupt to the Z80A by accessing a decoded MC68000 memory location (not available on Model II/16 upgrades). Once a request for service has been recognized by the Z80A CPU, a descriptor block is read into Z80A memory from MC68000 memory to determine the specific service required.

Interrupt	Description	Vector Location
CONT4*	Initiated by the Z80A	234H
CONT5*	Initiated by the Z80A	238H
CONT6*	Initiated by the Z80A	23CH
ADERR*	Address error, generated by the memory management unit when a user attempts memory access outside the defined range.	240H
TIMERRI*	Time-out error, generated when no DTACK is received with the MC68000 as the bus master.	244H
TMERRE*	Time-out error, generated when no DTACK is received and the MC68000 is not the bus master.	248H
IPER*	Parity error, generated on a memory parity error when the MC68000 is the bus master.	24CH
EPER*	Parity error, generated on a memory parity error when the MC68000 is not the bus master.	250H

Table 7-1. Interrupt Inputs

Prior to attempting a memory transfer by the Z80A subsystem to or from the MC68000 memory, all Z80A memory pages must be deselected by resetting the lower nibble of port 0FFH. This implies that certain precautions must be observed. The stack and control program must be located in the lower 32K of the Z80A address space, since page zero cannot be disabled.

Additionally, two control ports must be initialized to determine the addresses involved and the mode of the transfer.

The two ports are described in the tables and text below.

Upper Address Latch (port 0DFH)

Description: Output only, latches the upper address bits (A22-A15) for a Z80A transfer to or from MC68000 memory.

Data Bit	Function
7	A22
6	A21
5	A20
4	A19
3	A18
2	A17
1	A16
0	A15

Transfer Control Latch (port 0DEH)

Description: Output only, latches one address bit and seven control outputs.

Data Bit	Function
7	A14
6	CONT6
5	CONT5
4	CONT4
3	RESET
2	HALT
1	CONT1
0	BURST

Two Modes are available for transferring data between the MC68000 and the Z80A memory. These are the Byte Mode and the Burst Mode which are controlled by bit 0 of the Transfer Control Latch (Port 0DEH).

In the Byte Mode (Burst Mode Bit negated) the MC68000 bus is requested, transfer is made and the bus is released for every byte. In Burst Mode (Burst Mode Bit on) the MC68000 bus is requested and held as long as the Burst Mode Bit is set. The following rules must be observed when transfering data so that refresh violations will not occur.

RESET controls the MC68000 Memory REFRESH circuit. If RESET is asserted it will disable refresh to the MC68000 memory boards. To observe the refresh requirement of the MC68000 memory RESET should not be asserted longer than 15 microseconds.

When using the DMA to tranfer data, the DMA should not be programmed to transfer data longer than 2 ms (milliseconds) and then should allow the Z80A to execute at least 128 opcodes. This combination of data transfer and execution calculates to a maximum of 256 bytes with DMA in continuous mode when in Byte Mode (Burst Mode Bit negated). When in the Burst Mode (Burst Mode Bit asserted) it calculates to a maximum of 512 bytes with DMA is in continuous mode.

It should also be noted that as long as the Burst Mode Bit is asserted (in Burst Mode) the MC68000 is halted and has released the MC68000 bus to the Z80A-to-MC68000 Memory Interface Circuit. This can slow down the MC68000 CPU if many Burst Mode transfers are made.

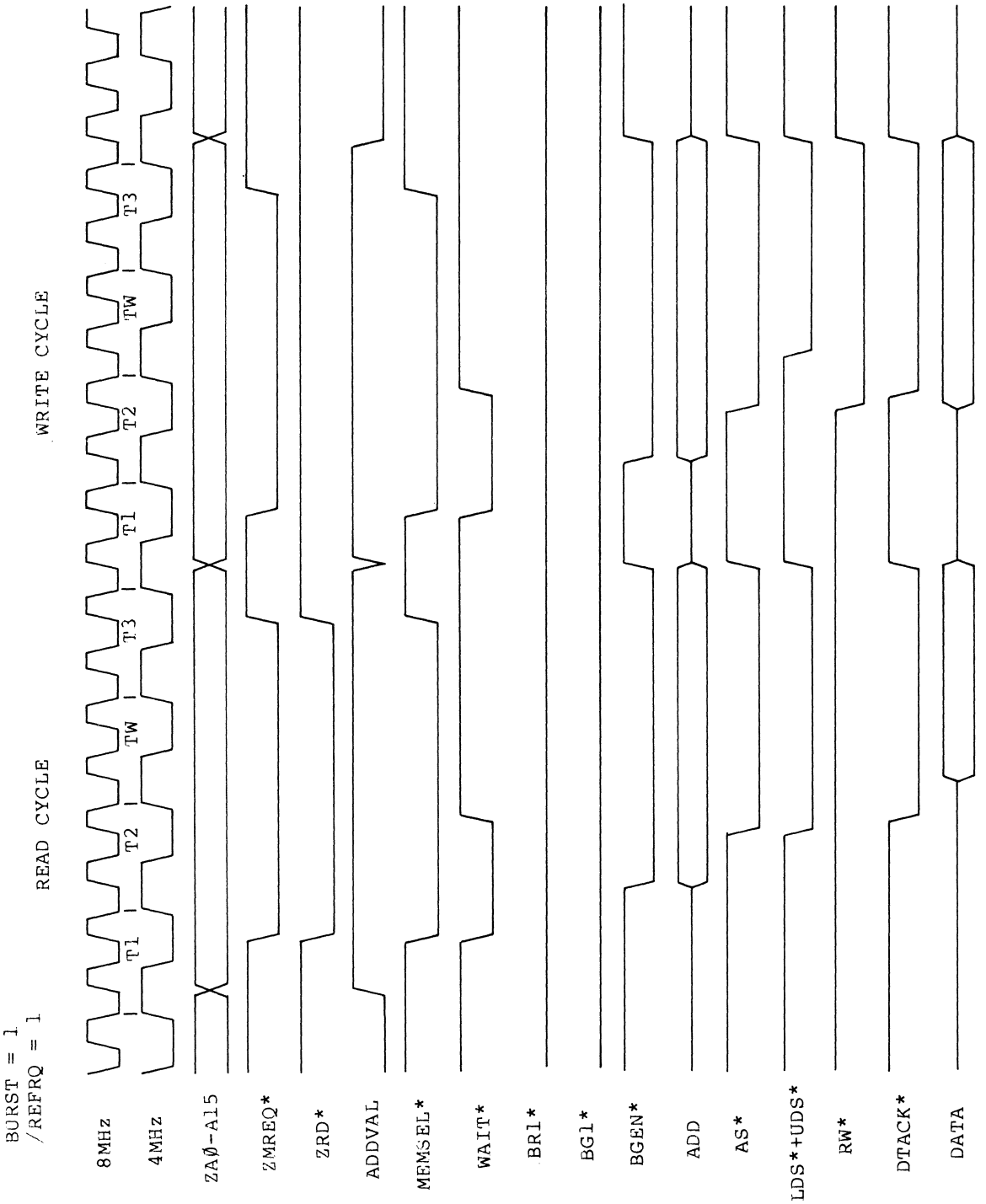


Figure 7-1. Read and Write Cycle Timing

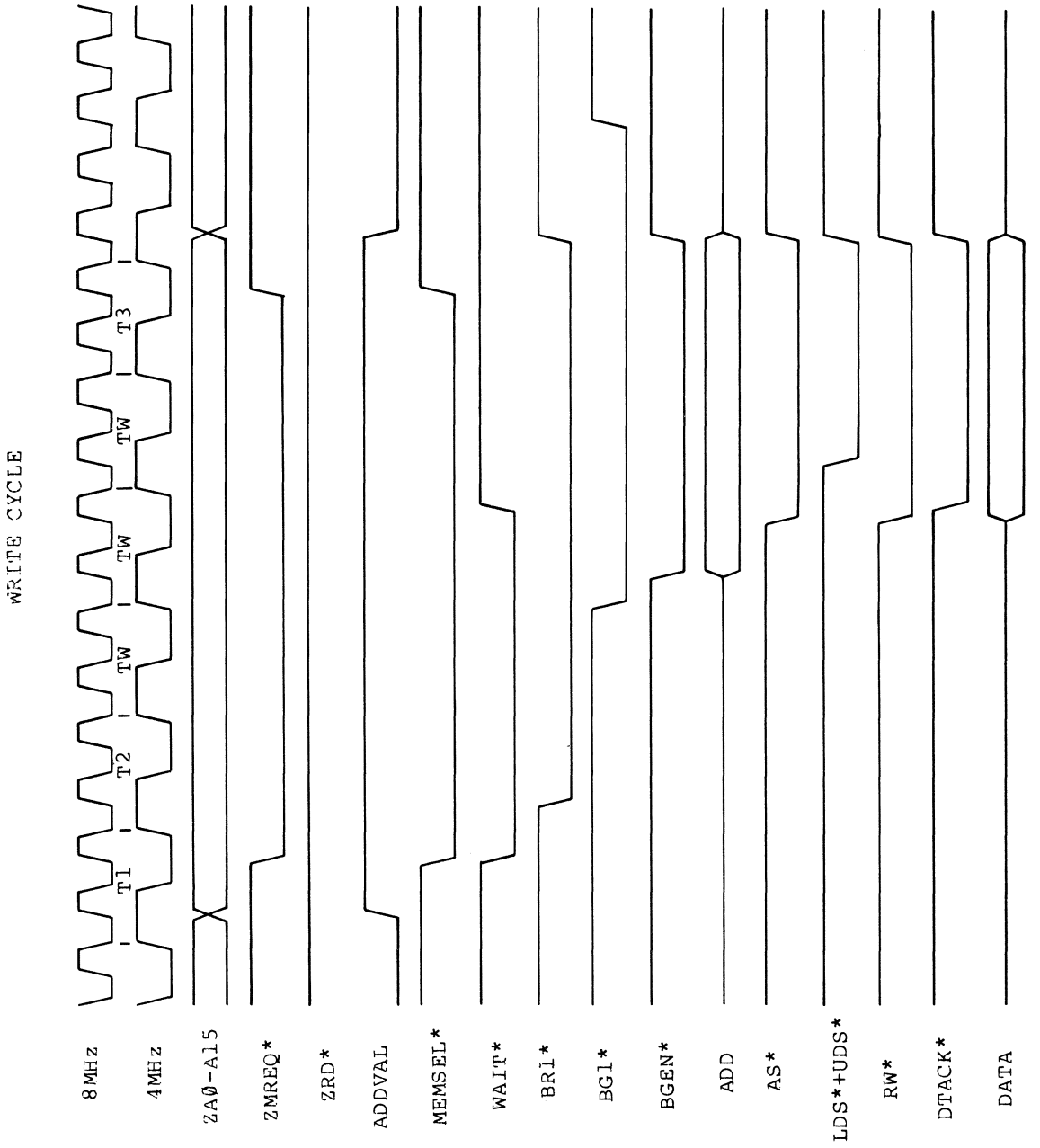


Figure 7-2. Write Cycle Timing

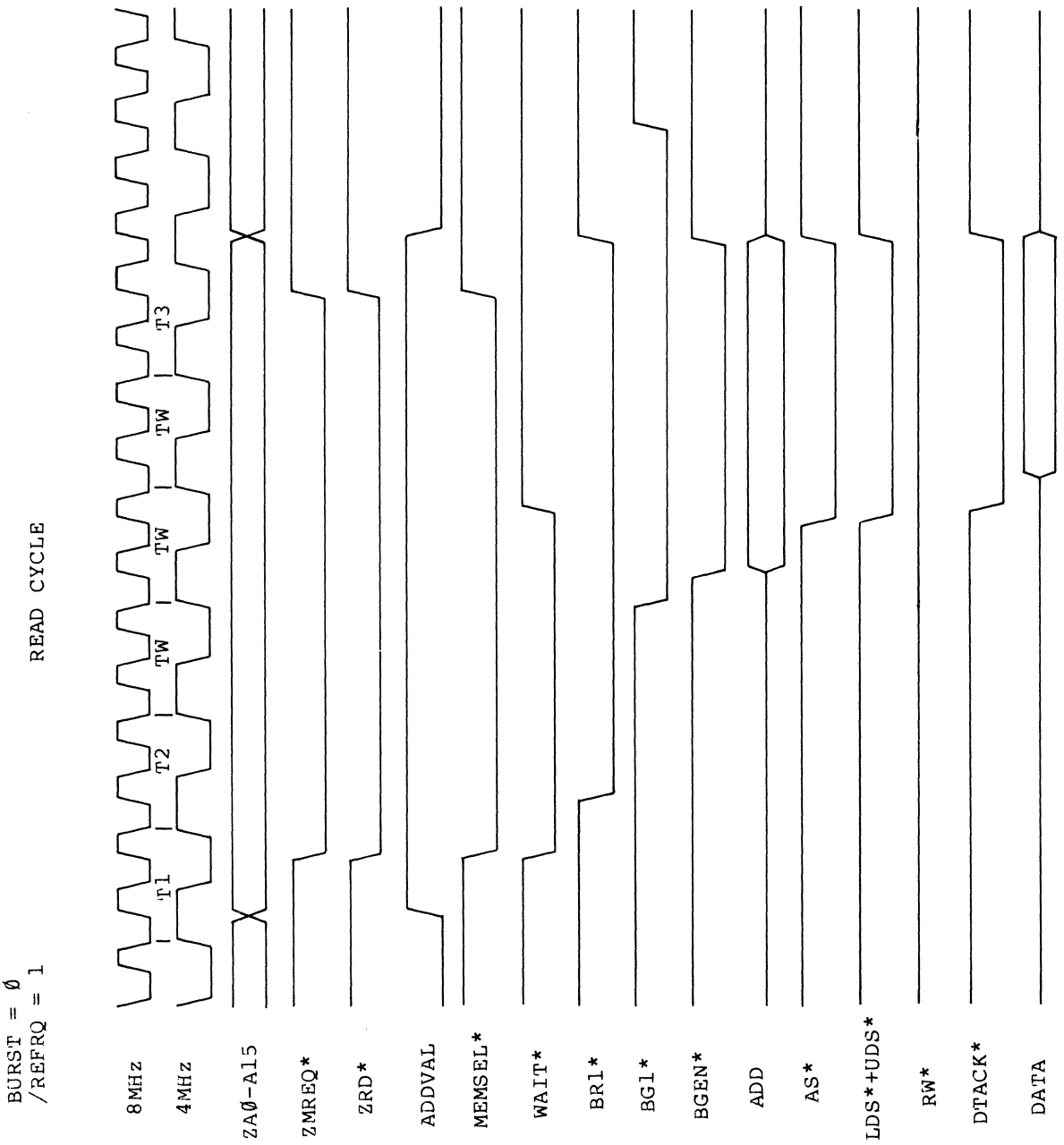


Figure 7-3. Read Cycle Timing

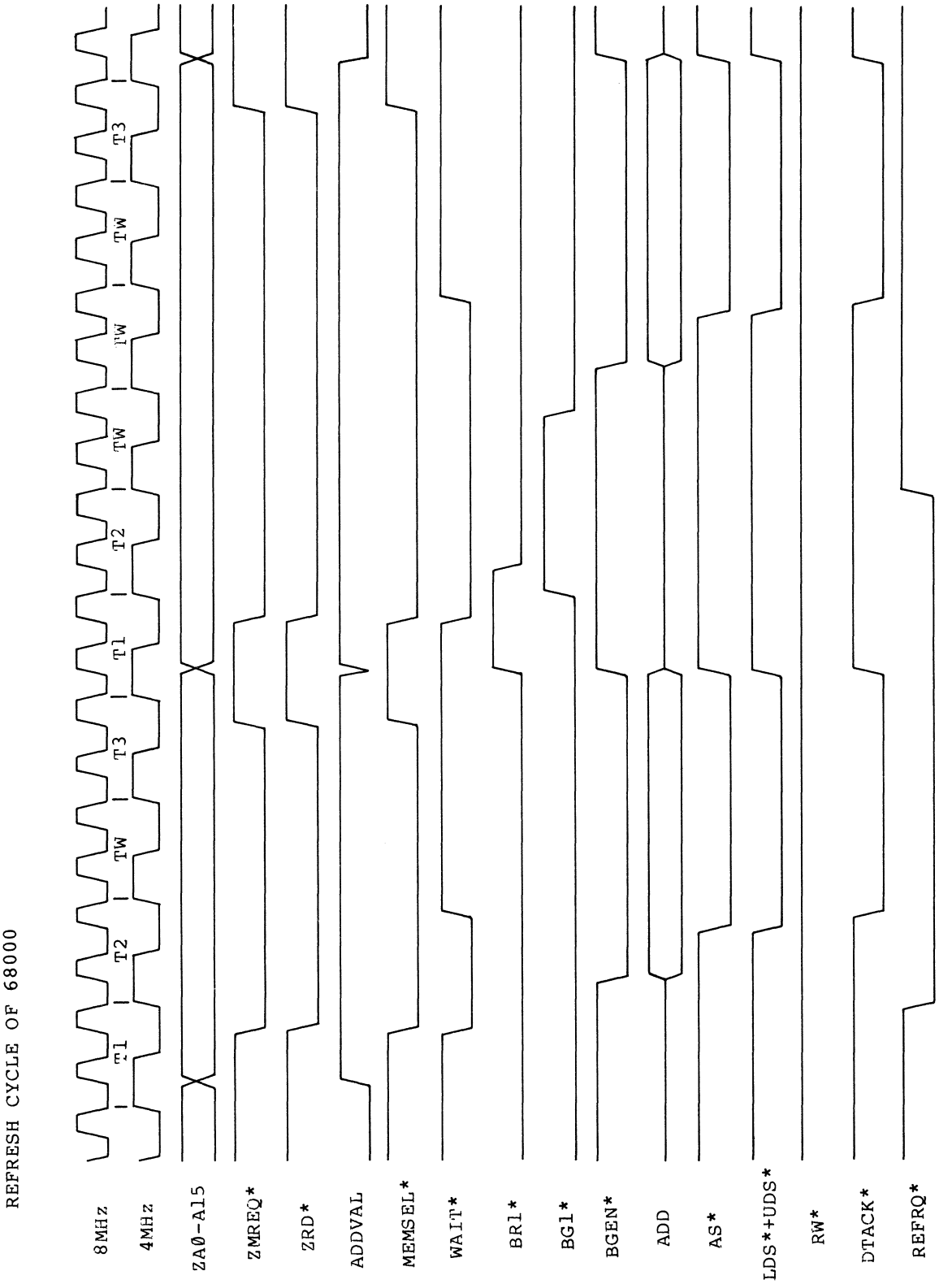


Figure 7-4. Refresh Cycle Timing of 68000

Details of Control Outputs (port 0DEH)

BURST
- 0 = Byte Mode enabled
- 1 = Burst Mode enabled

CONT1
- 0 = Enables Z80A to initiate memory transfers to or from MC68000 memory space
- 1 = Transfers by Z80A disabled

HALT
- 0 = MC68000 processor not halted
- 1 = Halts MC68000 processor

RESET
- 0 = RESET negated, enable Refresh to MC68000 memory
- 1 = Asserts RESET to MC68000 processor, disable Refresh to MC68000 memory

CONT4
Interrupt to MC68000 processor
Transition generates interrupt

CONT5
Interrupt to MC68000 processor
Transition generates interrupt

CONT6
Interrupt to MC68000 processor
Transition generates interrupt

7.2.4 Memory Management Circuitry

A fast memory management scheme provides two sets of offset and limit registers. The offset and limit registers define the relocation base address and the absolute limit address allowed by the current user program. Providing two sets of limit and offset registers allows all user programs to access a common kernel of the operating system or the run-time package.

Memory is allocated in 4K byte increments and relocation is done on 4K byte boundaries. Memory management is not active in system mode or during memory transfers initiated by bus masters other than the MC68000 CPU.

Write protection for the memory outside a user's partition is provided. Accesses outside of the user's defined partition result in the generation of a bus error exception. An interrupt can also be generated if the interrupt controller is properly initialized.

There are two things that cause the generation of a bus error:

The user addresses outside his partition
A bus time-out occurs

A bus time-out results when nonexistent memory or I/O accesses are attempted. The source of the bus error can be determined by reading the status register of the interrupt controller.

The hardware that accomplishes the memory management function works as described in the following paragraphs.

The MC68000 processor address bits A12 through A19 are added to the 8-bit value that is stored in the active offset register. The result of this addition is the effective address that is presented to the address bus.

The effective address is compared to the 8-bit value that is stored in the active limit register. If the effective address is larger than the contents of the active limit register, or if the addition results in a carry overflow from the adder, a bus error is generated.

The MC68000 processor address A23 determines which set of offset and limit registers are used. If A23 is high, then offset and limit registers two will be active. If A23 is low, then offset and limit registers one will be active.

Each of the two extents is implemented with an offset register and a limit register, which are 74LS374 8-bit D-type registers. The 8-bit value in the offset register is added to the eight processor address lines (KA12 to KA19) to form User Extent Address lines (UEA12 to UEA19).

The effective address is then compared with the value in the limit register. If the EA is greater than the limit, an out-of-bounds error is generated.

A carry out of the adder (2F83) also generates an OBERROR. If OBERROR occurs when MMA and GAS are active, then an Address Error is generated (ADERR). This signal (ADERR) is one of the interrupt sources.

The source of the user extent address is selected by A23 and the signal MMA (memory management active) determines which set of buffers (U31 or U30) drive the address bus. If MMA is high, the user effective address is driven to the bus by U31. If MMA is low, the addresses directly from the 68000 are driven to the bus by U30.

For a one-megabyte memory space, eight bits of memory management allow 4K minimum granule sizes to be protected.

Note: KA22 asserted selects the I/O device address space. The I/O device strobe generation logic generates the I/O strobes necessary to communicate with interrupt controller and memory management registers by decoding KA21 and KA22.

7.2.5 Bus Arbitration Logic

Bus arbitration allows other devices capable of being bus master to request, be granted, and acknowledge bus mastership. The bus arbitration sequence is as follows:

1. The device asserts a Bus Request (BR*).

2. The MC68000 CPU asserts a Bus Grant (BG*) to indicate that the bus will be released at the end of the current bus cycle.

3. The device acknowledges the bus grant by asserting a Bus Grant Acknowledge (BGACK*) and assuming bus mastership. A requesting device should not assert BGACK* or assume bus mastership until the following conditions are met:

   A bus grant has been received

   BAS* has been negated, indicating that the CPU has completed the current bus cycle

   BDTACK* has been negated, indicating that memory or peripherals are not using the bus

   BGACK* has been negated, indicating that no other device still has bus mastership.

4. The device negates the Bus Request (BR*).

The bus arbitration control is performed by the bus arbitration controller chip U6. In addition to controlling the bus arbitration sequence, U6 manages four levels of bus requests and grants.

The sources for the four levels are Refresh Request (REFRQ*), Bus Request 2 (BR2*), Bus Request 1 (BR1*), and Bus Request 0 (BR0*), with REFRQ* having the highest priority and BR0* the lowest. The bus requests are pre-latched by a quad D-type latch U7 clocked at a 12 MHz rate.

The bus request is latched at a Q output of U7 and asserts a bus request input to U6 (pins 3-6). The bus arbitration controller will, in turn, assert BR* to the MC68000 CPU. After some internal synchronization time, the MC68000 will assert BG* to U6, which indicates that it will release the bus at the end of the current bus cycle.

When the current bus cycle has ended (i.e., when BAS* and BDTACK* are negated), U6 will assert a bus grant to the requesting device with the highest priority. The bus arbitration controller U6 will also assert BGACK* and negate BR* to the MC68000 CPU. BGACK* is inverted by 1/6th of U2 and both signals are used to indicate to other bus-controlling circuitry that an external device has become bus master.

The MC68000 CPU will negate BG* and wait until BGACK* has been negated before re-assuming bus mastership. The requesting device can then assume bus mastership and perform any data transfers needed.

When the current bus master is finished, it negates the bus request to the bus arbitration controller through U7. Then, if there is a bus request still pending, a bus grant will be asserted to the next requesting device and BGACK* will remain asserted until all pending bus requests have been satisfied.

If no bus requests are pending, the bus arbitration controller will negate BGACK* and allow the MC68000 CPU to assume bus mastership. See Figure 7-5 for the timing relationships of this circuit.

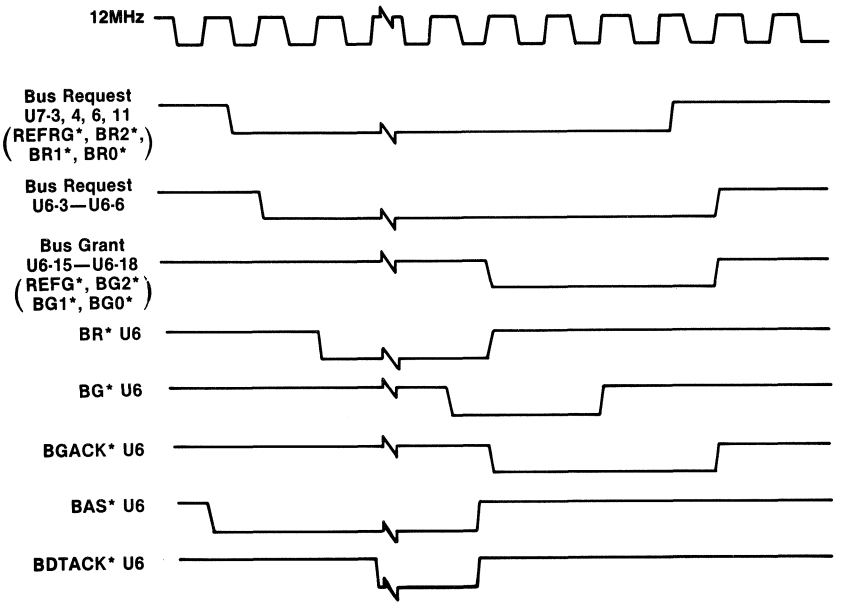


Figure 7-5. Bus Arbitration Circuit Timing

7.2.6 Data Transfer Acknowledge Logic

Data Transfer Acknowledge (DTACK*) is the asynchronous handshake signal used by memory and peripheral devices to complete a bus cycle. When BDTACK* is asserted during a read bus cycle (after approximately one and one half PCLOCK cycles) the data is latched into the MC68000 CPU and the bus cycle is terminated. Assertion of BDTACK* during a write cycle causes the MC68000 CPU to terminate the bus cycle after approximately one and one half PCLOCK cycles. There are two main sources of BDTACK* from the CPU's point of view:

Onboard devices, such as the AM9519 interrupt controller chip and the memory management registers.

Offboard devices, such as memory or peripherals connected to the MC68000 bus.

Two signals can trigger the generation of an onboard BDTACK* -- IODTACK* and RIP*.

If IODTACK* is asserted, a read or write to an onboard I/O device is in progress.

If RIP* is asserted, an interrupt acknowledge cycle is in progress and the interrupt vector data is valid from the interrupt controller chip U15.

IODTACK* and RIP* are ORed together at U8 pins 9 and 10 and the resultant output at U8 pin 8 clocks a low into the D flip-flop (1/2 of U49). This results in a high output at U49 pin 6, which is inverted by 1/6th of U33 and used to drive BDTACK* line low.

Address Strobe (AS) sets the flip-flop and negates BDTACK* for the next bus cycle. Figure 7-6 shows the timing relationships for onboard BDTACK* generation.

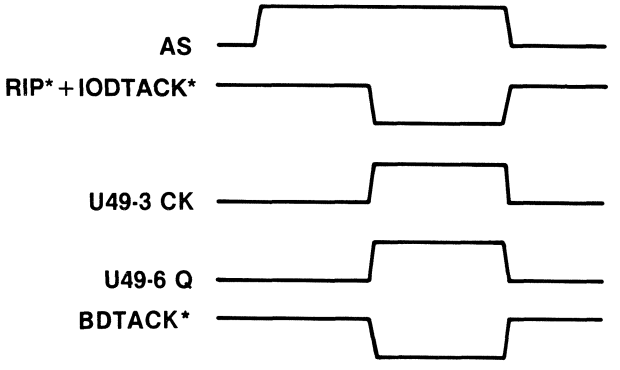


Figure 7-6. Onboard BDTACK Generation

Generation of BDTACK* from offboard devices is only from the MC68000 memory boards. BDTACK* being asserted from an MC68000 memory board indicates that the data transfer has been completed.

During a write cycle, BDTACK* indicates that the data from the data bus has been written into memory and has completed the transfer. During a read cycle, BDTACK* indicates that the data requested is present on the data bus. For more details on memory BDTACK* generation, refer to Paragraph 7.2 Memory Board Theory of Operation.

BDTACK* is also generated when an External time-out (TMERRE) occurs. This allows the WAIT* signal from U36 to the Z80A to be negated and release the Z80A CPU. During an internal time-out (TMERRI), BDTACK* is not required because BERR* is asserted which will terminate to the MC68000 cycle.

7.2.7 MC68000 I/O Decoding and Strobes

The I/O devices in the MC68000 subsystem are memory-mapped and consist of the:

Interrupt controller chip
Memory management registers
Z80A interrupt (NOT implemented in the Model II upgrades)

All other I/O devices and peripherals in the TANDY 6000/6000-HD are still controlled by the Z80A CPU.

The main I/O decoding is managed by chip U48, which is the I/O controller. The I/O controller interfaces the MC68000 CPU to the MC68000 subsystem I/O devices, thereby providing all necessary signals.

Sheet 2 of the MC68000 CPU schematic should be referenced unless otherwise noted. The current I/O devices are mapped at address locations 7800D0H to 7800D7H. Address bits KA20-KA22 are decoded by a 3 input AND gate (1/3 of U10) that generates the signal VMIIAD.

VMIIAD and mIO (KA19) are connected to the I/O controller and generate the I/O signals during access to the memory space 780000H to 78FFFFH. When an I/O access is executed, R/W*, KA19, VMIIAD, AS*, and the 8 MHz CK start a 3 bit internal counter. This counter is used to time the assertion of BIORQ*, BRD*, and BWR*, and IODTACK*.

R/W* and AS* determines the assertion of BRD* or BIOR*. BIORQ* is used to enable a 1 of 8 decoder U41 that decodes address bits KA1-KA7.

KA4, KA6, and KA7 are decoded by a 3-input AND gate, 1/3rd of U27, and the output is connected to the active-high enable input U41 pin 6. KA5 enables the third enable input U41 pin 4 when an active low occurs.

KA1-KA3 are decoded to determine the output of U32 that selects the I/O device. Table 7-2 outlines the memory-mapped I/O locations currently implemented in the MC68000 subsystem. See Figure 7-7 for the timing relationships of the I/O controller U48.

Address	Function
7800D0	Interrupt controller data register
7800D1	Interrupt controller command register
7800D2	Limit register two
7800D3	Offset register two
7800D4	Limit register one
7800D5	Offset register one
7800D6	Interrupt request to Z80A
7800D7	Interrupt request to Z80A

Table 7-2. Memory-Mapped I/O Locations

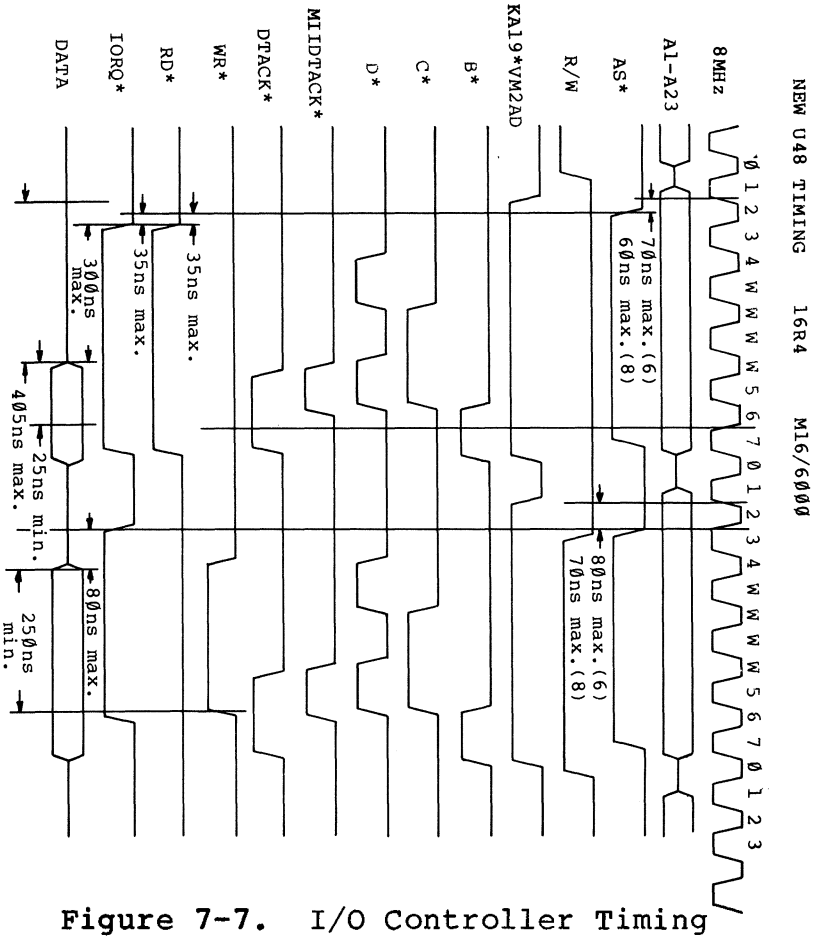


Figure 7-7. I/O Controller Timing

Table 7-3 outlines the memory map of the MC68000 subsystem:

SYSTEM RAM

Start Address	End Address	Total Bytes
Total Available RAM Space in Supervise Mode		
000000	6FFFFF	7 MEG
Total Available Protected RAM Space in User Mode		
000000	0FFFFF	1 MEG
One 128K Memory Board Installed		
000000	01FFFF	128K
Two 128K (or one 256K) Memory Boards Installed		
000000	03FFFF	256K
One 256K and One 128K Memory Board Installed		
000000	05FFFF	384K
Two 256K Memory Boards or One 512K Memory Board Installed		
000000	07FFFF	512K
Three 256K Memory Boards Installed or One 512K and One 256K Memory Board Installed		
000000	09FFFF	768K
One 1 MEG Memory Board Installed		
000000	0FFFFF	1 MEG

Table 7-3. Memory Map of the MC68000 Subsystem

7.2.8 Clock Logic

The clock logic provides the clocks and timing for the MC68000 subsystem. The heart of the clock logic is a 48 MHz crystal oscillator (Y1). See the top left-hand corner of sheet 2 of the MC68000 CPU schematic. The 48 MHz output of Y1 is buffered by 1/4 of U47 which is input to the clock inputs of U46 (F161) and U53 (F175). U46 is a 4 bit synchronous counter and is used to divide the 48 MHz input into 4 output clocks. The counter is preloaded with a count of 9 or 1 depending on the state of QD output (U46 pin 11). the counter will count to X110 and preload again. This generates a divide by 2 at U46 pin 14 (24 MHz), a divide by 4 at pin 13 (non symmetrical 12 MHz), a divide by 6 at pin 12 (8MHz), and a divide by 12 at pin 11 (4MHz). The 24 MHz output is divided by 2 by 1/4 of U52 (F86) and U53 (F175). the 8 and 4 MHz outputs are also clocked through U53 to assure all three clocks are synchronous with each other.

7.2.9 Refresh Logic

The refresh logic provides the necessary timing and control for generating the refresh pulses required for the dynamic RAMs on the MC68000 memory board(s). It provides refresh by becoming the bus master and supplying the refresh strobe REFRSH. The timing is generated by an LS393 counter (U39) and a PAL device (U46).

The timing logic generates a bus request (REFRQ*) every 15.5 or 31 usec, depending on the configuration of the jumper on E1, E2, and E3. If E1 and E2 are jumpered, U46 triggers the D flip-flop (1/2 of U25) on the count of 62, which equals 15.5 usec. This will meet the minimum requirement of 128 refreshes every 2 msec. If E2 and E3 are jumpered, the D flip-flop will be triggered on the count of 124, which will equal 31 usec. This configuration will generate less refresh bus request cycles, thus allowing more CPU running time. However, to meet the 2 msec refresh specification, two refresh pulses are generated during each refresh period.

The generation of the single- or double-refresh pulse is the function of a refresh state machine implemented with a PAL device, U46. Figure 7-8 shows the timing relationships of the refresh logic. The double refresh (31µsec) mode does not work with 512K/1Meg memory board.

7.2.10 Bus Error Logic

Bus error logic is driven low when one of two events occurs, an attempt by the user to access memory outside the extents defined by the memory management registers or a time-out error on an MC68000 memory access. The bus error signal drives the BERR* bus signal to all MC68000 memory boards, which instructs the 16-bit memory board to abort a memory cycle. This provides a write-protect feature for accesses outside the user's defined extents. (A 100 usec one-shot (1/2 of U32) is used to define the maximum time allowed for a memory cycle.) The bus Address Strobe (BAS*) is used to repeatedly trigger the one-shot. The active-low output of the one-shot is the clock input to a D flip-flop (1/2 of U21). If the one-shot ever times out, the rising edge of the active-low output will clock the state of BDTACK* into the D flip-flop.

If, on a timeout, BDTACK* is high, indicating that the memory or I/O device did not respond, TMERR* is driven by the Q-not output of the flip-flop. Thus, if a device on the bus fails to respond within the timespan allotted by the time-out circuit, a bus error will be generated.

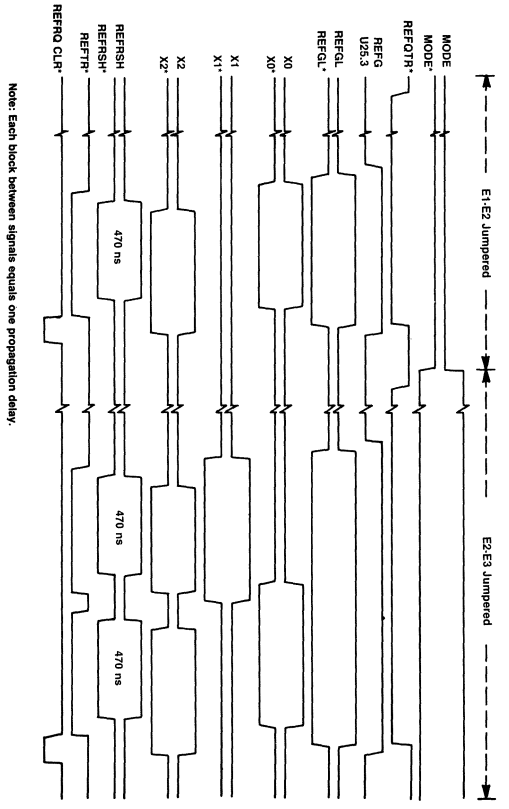


Figure 7-8. Timing for Refresh Logic

7.2.10 CPU PAL Pin Assignments and Equations

PAL 16R4 (U48)

Pin Assignments:

```
8MHZ   2   /SRW   KA19   5   6   VM2AD   /AS   /RESET   GND
/E    12   /IORQ   /WR    /B  /C  /D     /RD   /DTACK   VCC
```

Equations:

```
IF (VCC) DTACK = /B * C * D * AS * VM2AD * KA19                    */RESET

IF (VCC)   RD  =                   AS * VM2AD * KA19 */SRW */RESET

           D   :=          /D * AS * VM2AD * KA19                  */RESET
               +  B * C * D * AS * VM2AD * KA19                    */RESET

           C   :=      /C * D * AS * VM2AD * KA19                  */RESET
                       C */D * AS * VM2AD * KA19                   */RESET
               +  B * C * D * AS * VM2AD * KA19                    */RESET
```

```
          B  := /B * C * D * AS * VM2AD * KA19        */RESET
              +  B         * AS * VM2AD * KA19        */RESET

         WR  := /B */C     * AS * VM2AD * KA19 * SRW */RESET
              + /B * C */D * AS * VM2AD * KA19 * SRW */RESET

IF (VCC) IORQ  =             AS * VM2AD * KA19 */SRW */RESET
              + /B           * AS * VM2AD * KA19 * SRW */RESET
```

PAL 16R6 (U6)

Pin Assignments:

```
12MHZ /RESET /REFRQ /BR0 /BR1 /BR2 /BG /AS /DTACK GND
/E /BPER /BGACK /PER /BG0 /BG1 /BG2 /REFG /BR VCC
```

Equations:

```
IF (VCC) BR = /RESET* REFQ*/BGACK
            + /RESET* BR0 */BGACK
            + /RESET* BR1 */BGACK
            + /RESET* BR2 */BGACK

     BGACK := /RESET* BG*/DTACK*/AS* REFRQ
            + /RESET* BG*/DTACK*/AS* BR0
            + /RESET* BG*/DTACK*/AS* BR1
            + /RESET* BG*/DTACK*/AS* BR2
            + /RESET* BGACK* REFRQ
            + /RESET* BGACK* BR0
            + /RESET* BGACK* BR1
            + /RESET* BGACK* BR2

     REFG  := /RESET* REFRQ* BGACK* BG2*/BR2
            + /RESET* REFRQ* BGACK* BG1*/BR1
            + /RESET* REFRQ* BGACK* BG0*/BR0
            + /RESET* REFRQ* BGACK* BG2*/BG1*/BG0
            + /RESET* REFRQ* BGACK* REFG

     BG2   := /RESET* BGACK* BR2*/REFRQ* REFG
            + /RESET* BGACK* BR2*/REFRQ* BG1*/BR1
            + /RESET* BGACK* BR2*/REFRQ* BG0*/BR0
            + /RESET* BGACK* BR2*/REFRQ*/BG1*/BG0*/REFG
            + /RESET* BGACK* BR2* BG2
```

```
BG1   := /RESET* BGACK* BR1*/REFRQ*/BR2* REFG
       + /RESET* BGACK* BR1*/REFRQ*/BR2* BG2
       + /RESET* BGACK* BR1*/REFRQ*/BR2* BG0*/BR0
       + /RESET* BGACK* BR1*/REFRQ*/BR2*/BG2*/BG0*/REFG
       + /RESET* BGACK* BR1* BG1

BG0   := /RESET* BGACK* BR0*/REFRQ*/BR2*/BR1* REFG
       + /RESET* BGACK* BR0*/REFRQ*/BR2*/BR1* BG2
       + /RESET* BGACK* BR0*/REFRQ*/BR2*/BR1* BG1
       + /RESET* BGACK* BR0*/REFRQ*/BR2*/BR1*/BG2*/BG1*/REFG
       + /RESET* BGACK* BR0* BG0

IF (VCC) PER = /BPER
```

PAL 16R6A (U36)

Pin Assignments:

```
8MHZ 4MHZ ADDVAL /ZRD /REFRQ ZA0 /BG1 /DTACK /MEMSEL GND
/E BURST /LDS /UDS /AS /BR1 /BGEN /RW /WAIT VCC
```

Equations:

```
BR1   := ADDVAL * MEMSEL * 4MHZ
       + BR1 * /4MHZ
       + BURST * /REFRQ

BGEN  := BG1 * ADDVAL * MEMSEL * 4MHZ
       + BGEN * /4MHZ

AS    := BGEN * MEMSEL
       + AS * /4MHZ

UDS   :=BGEN * MEMSEL *  ZRD * ZA0
       +BGEN * MEMSEL * /ZRD * ZA0 * AS
       +UDS * /4MHZ

LDS   :=BGEN * MEMSEL *  ZRD * /ZA0
       +BGEN * MEMSEL * /ZRD * /ZA0 * AS
       +LDS * /4MHZ

RW    :=BGEN * MEMSEL * /ZRD * WAIT
       +RW * MEMSEL
       +RW * /4MHZ

IF (ADDVAL * MEMSEL) WAIT = /BGEN * ADDVAL * MEMSEL
                          +  BG1  * ADDVAL * MEMSEL * /DTACK
```

PAL 16L8 (U40)

Pin Assignments:

```
1B 1C 1D REFRSH REFGL MODE RESET 2A 2B GND
2C RFQTR /X0 /X1 /X2 /REFRQCLR /REFTR 18 19 VCC
```

Equations:

```
IF(VCC) REFRQCLR = /RESET* X2*/X1*/X0
                 +  RESET

IF(VCC) REFTR    = /RESET*/X2*/X1* X0
                 +  RESET*/X2* X1*/X0

     IF(VCC) X2  = /RESET    */X1* X0      * REFRSH* REFGL
                 + /RESET* X2*/X1*         */REFRSH* REFGL
                 + /RESET    * X1*/X0* MODE*/REFRSH* REFGL
                 + /RESET* X2* X1*/X0* MODE*/REFRSH* REFGL

     IF(VCC) X1  = /RESET*/X2    */X0* MODE*/REFRSH* REFGL
                 + /RESET    * X1*/X0* MODE* REFRSH* REFGL
                 + /RESET* X2* X1    * MODE*/REFRSH* REFGL

     IF(VCC) X0  = /RESET*/X2*/X1    */MODE*/REFRSH* REFGL
                 + /RESET    */X1* X0      */REFRSH* REFGL
                 + /RESET*/X2    * X0* MODE*/REFRSH* REFGL
                 + /RESET    * X1* X0* MODE*/REFRSH* REFGL
                 + /RESET* X2* X1    * MODE*/REFRSH* REFGL

  IF(VCC) /RFQTR = /RESET*/MODE* 1B* 1C* 1D* 2A* 2B
                 + /RESET* MODE    * 1C* 1D* 2A* 2B* 2C
                 + /RESET      * 1B* 1C* 1D* 2A* 2B* 2C
```

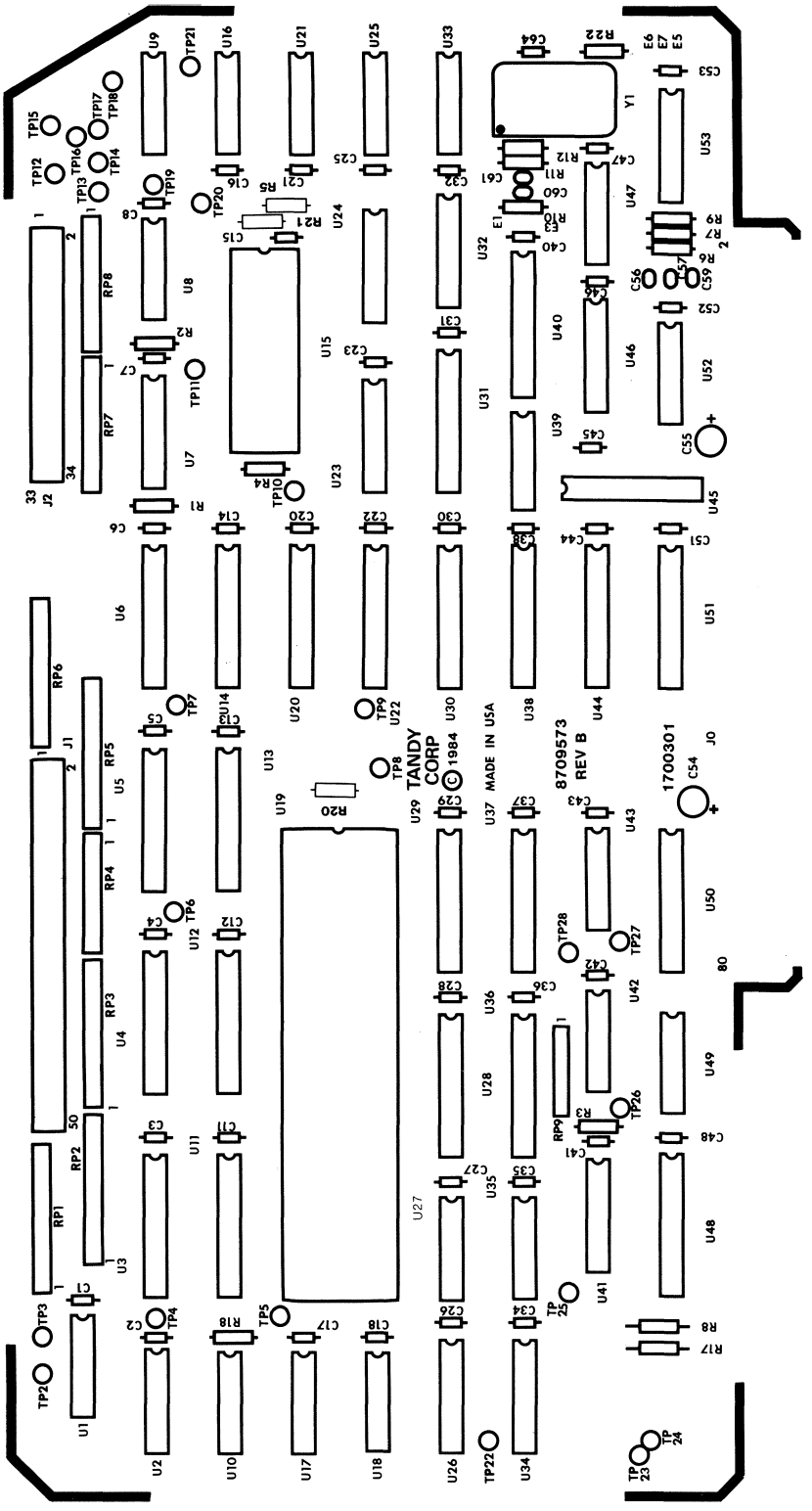
82S153 (U45)

Pin Assignments:

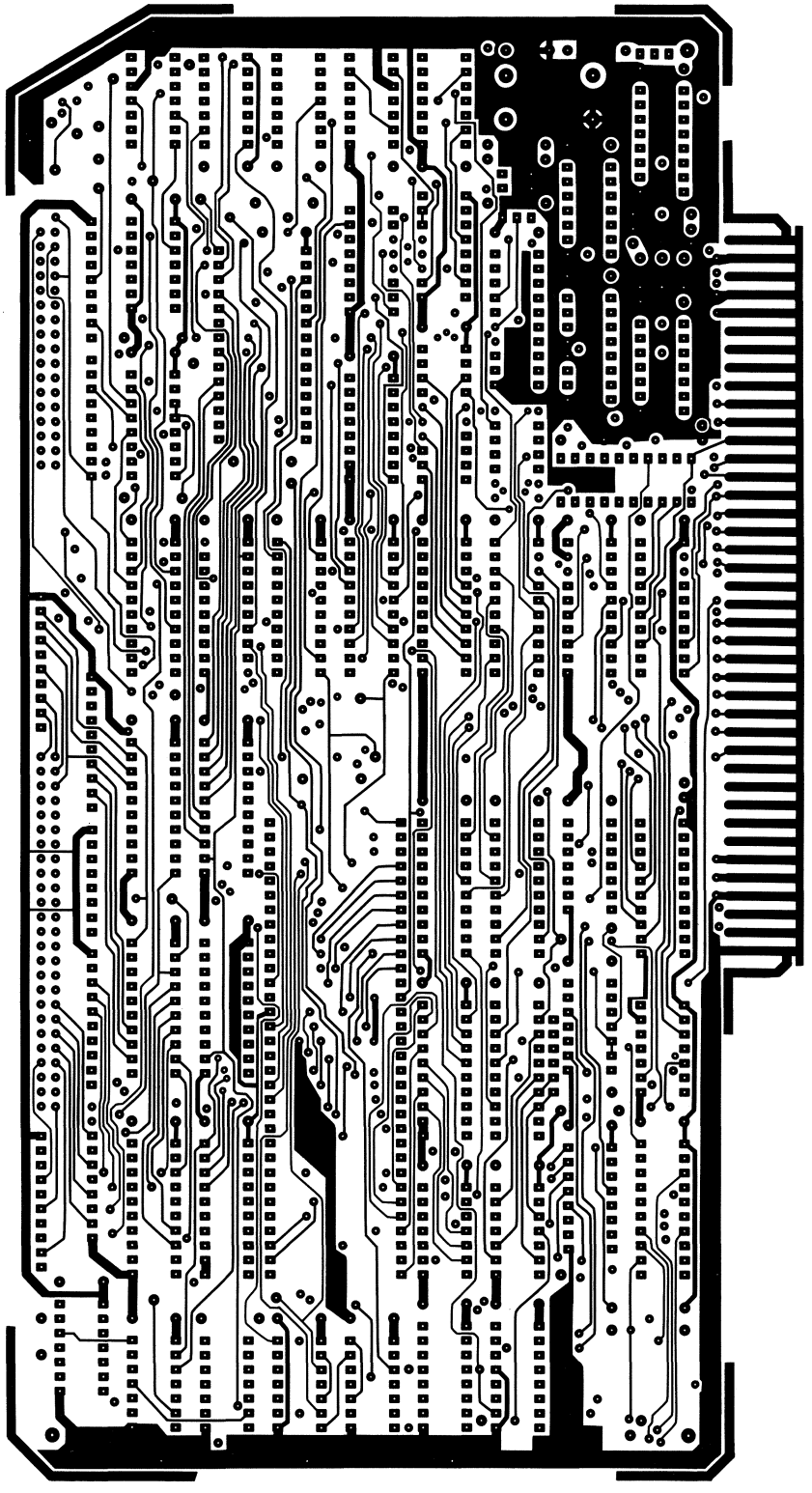
```
/REFRESH  2  /WR  /A14  /A15  /IOCYC  /A0  A3  A2  GND
/A1  /A5  /A4  OUTDE  OUTDF  16  ADDVAL  /A7  /A6  VCC
```

Equations:

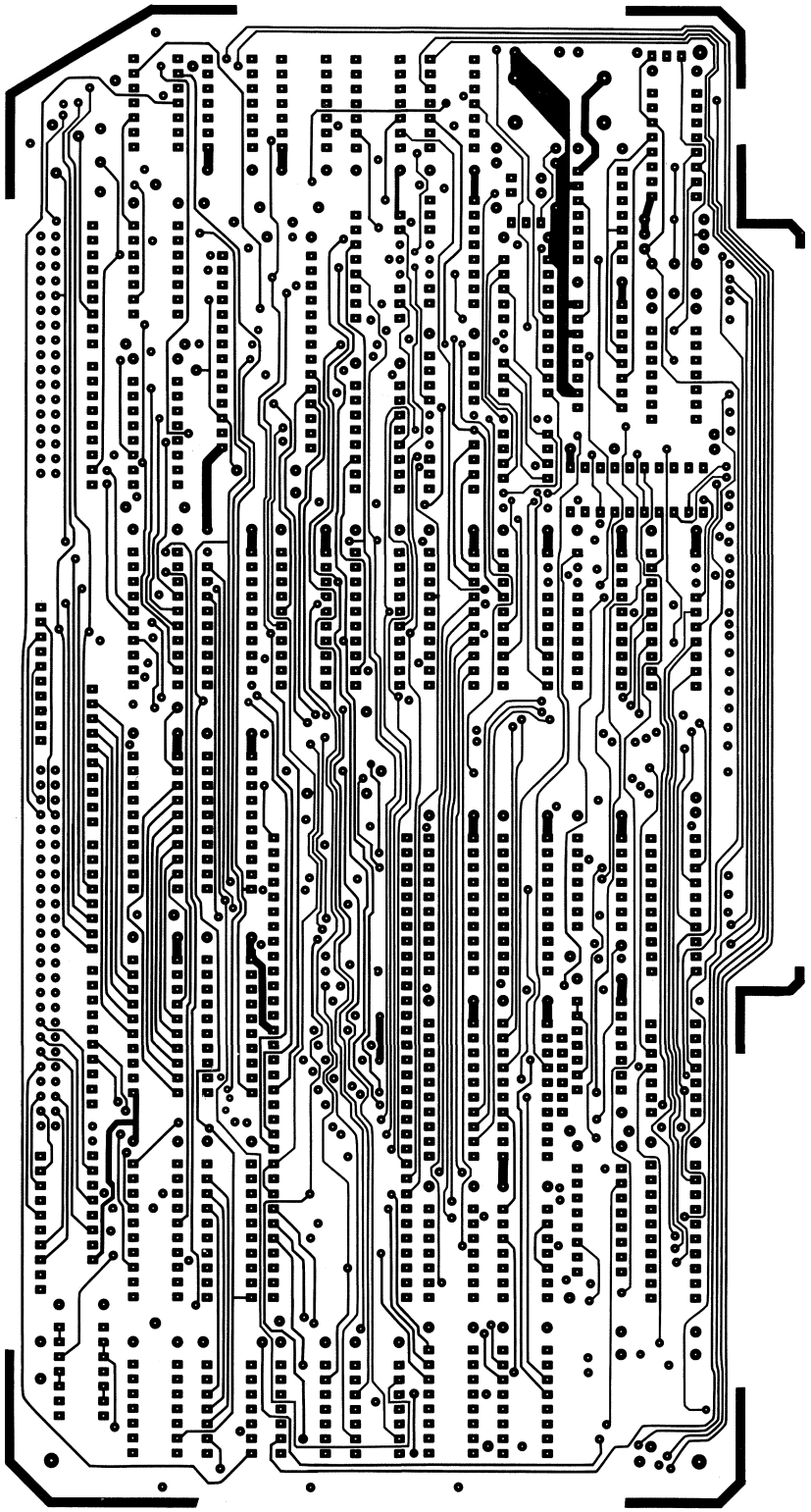
```
OUTDE = A7*A6*/A5*A4*A3*A2*A1*/A0* WR* IOCYC

OUTDF = A7*A6*/A5*A4*A3*A2*A1*A0* WR* IOCYC

ADDVAL = /A15* A14*/REFRESH
```



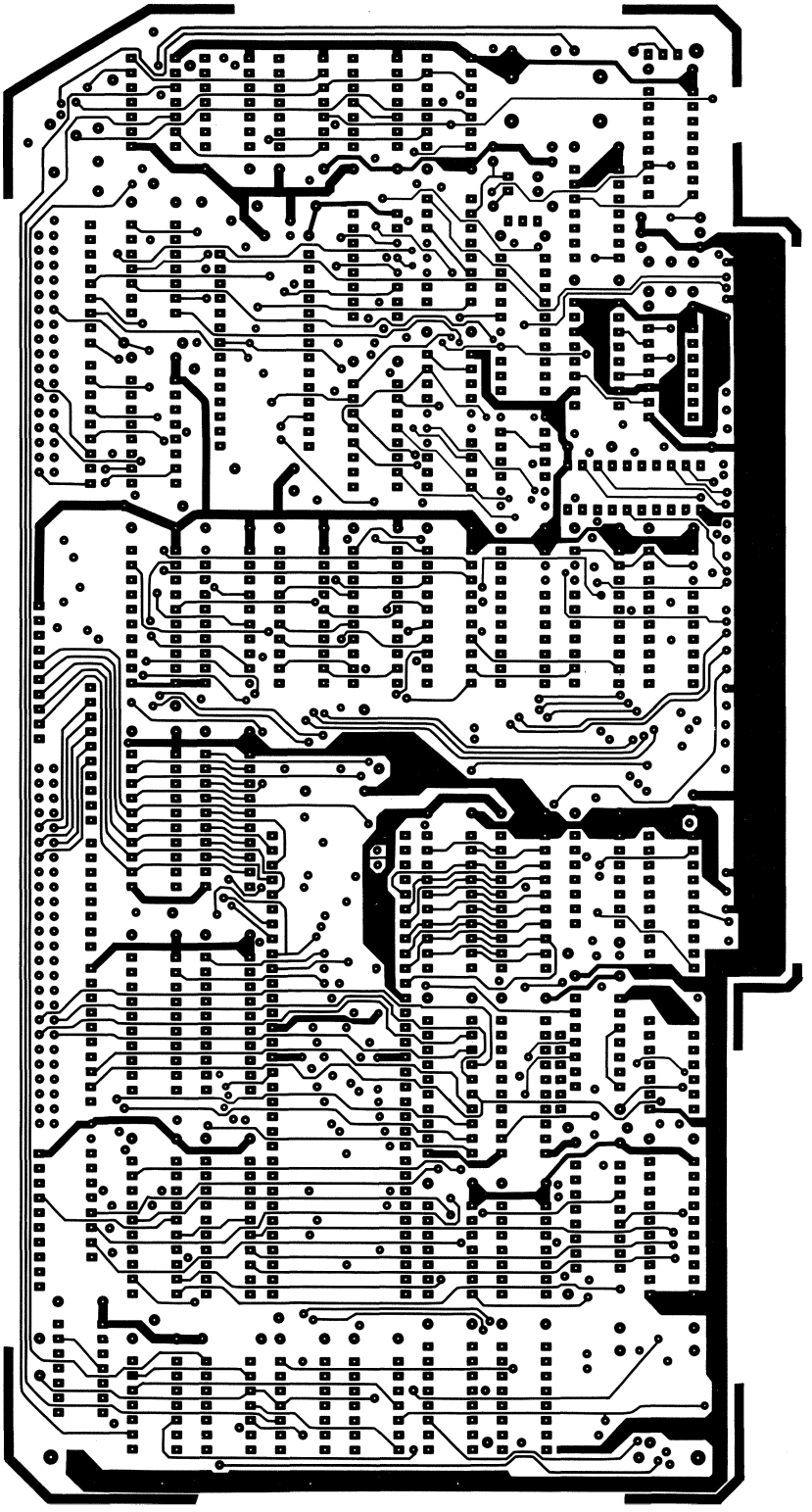
Component Layout, MC68000 CPU Board 8709573



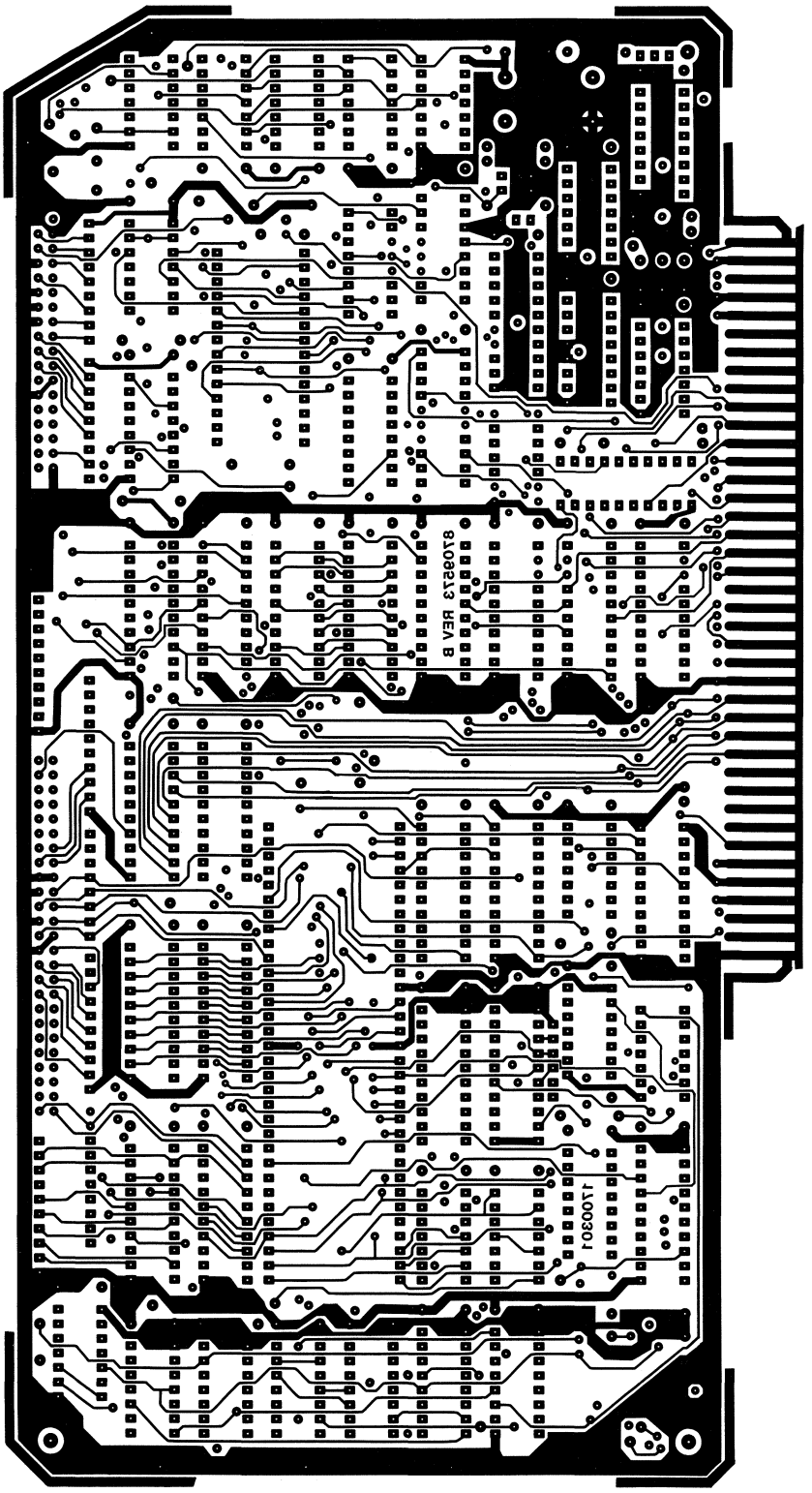
Circuit Trace, MC68000 CPU Board 8709573, Component Side



Circuit Trace, MC68000 CPU Board 8709573, Layer 2



Circuit Trace, MC68000 CPU Board 8709573, Layer 3



Circuit Trace, MC68000 CPU Board 8709573, Solder Side

Parts List, MC68000 CPU Board, 8898855

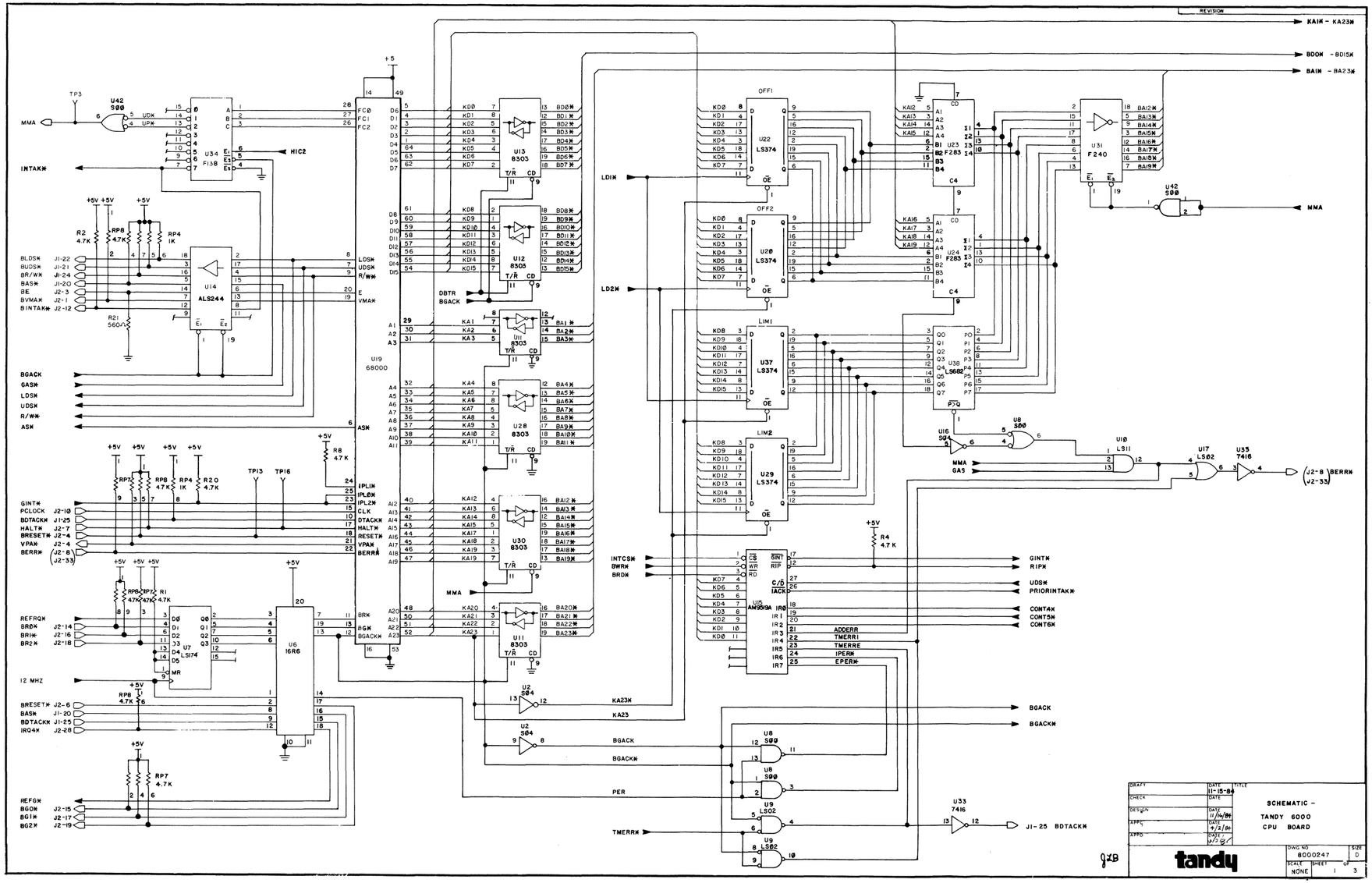
Ref No.	Description	Part No.
PC Board, CPU (Rev A)		8709573
Capacitors		
C1-C8	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C11-18	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C20-23	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C25-32	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C34-38	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C40-48	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C51-53	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C54,55	Capacitor, 100 uF, 16V, Elect. Rad.	8327101
C56,57	Capacitor, 68 pF, 50V, C. Disk	8300683
C59	Capacitor, 68 pF, 50V, C. Disk	8300683
C60	Capacitor, 0.001 uF, Ceramic, 10%, Z5P	8302104
C61	Capacitor, 27 pF, 50V, C. Disk, 5%	8300273
C64	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
Staking Pins		
E1-E3	Staking Pin	8529014
E5-E7	Staking Pin	8529014
Jumper Plugs		
E2,E3	Jumper Plugs	8519021
E6,E7	Jumper Plugs	8519021
Headers		
J1	Header, Dual 25-Pos. PCB MT.	9519117
J2	Header, Dual 17-Pos. PCB MT.	8519120
Resistors		
R1-R5	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R6,R7	Resistor, 560 ohm, 1/4W, 5%	8207156
R8	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R9	Resistor, 560 ohm, 1/4W, 5%	8207156
R10	Resistor, 220 kohm, 1/4W, 5%	8207422
R11	Resistor, 30.1 kohm, 1/4W, 1%	8200330
R12	Resistor, 4.7 kohm, 1/4W, 5%	8207247

Parts List, MC68000 CPU Board, 8898855

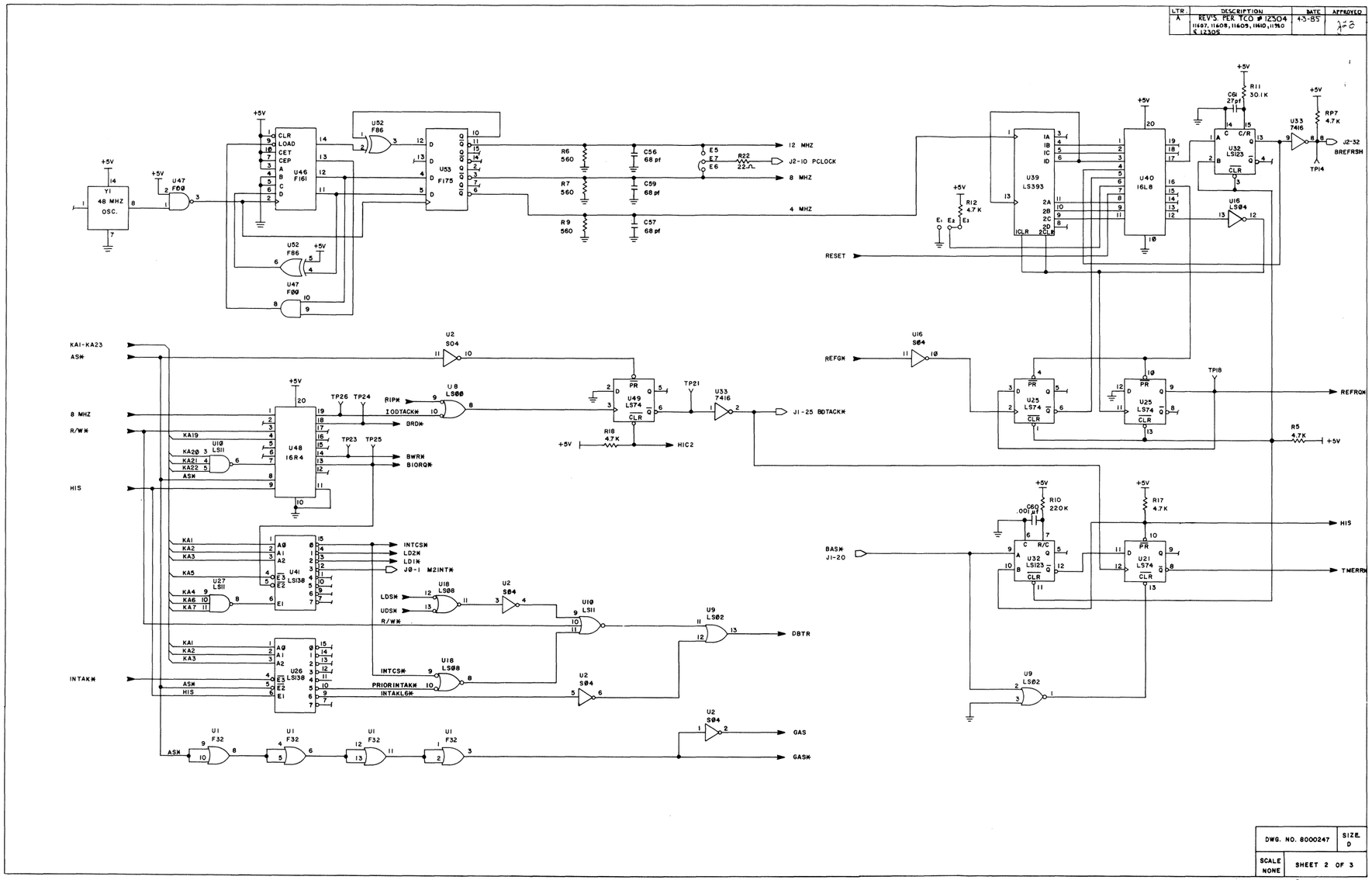
Ref No.	Description	Part No.
Resistors		
R17,R18	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R20	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R21	Resistor, 560 ohm, 1/4W, 5%	8207156
R22	Resistor, 22 ohm, 1/4W, 5%	8207022
Resistor Paks		
RP1-RP3	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP4	Res. Pak, 1k ohm SIP, 8-Pin	8290212
RP5,RP6	Res. Pak, 220-330 ohm SIP, 10-Pin	8290020
RP7,RP8	Res. Pak, 4.7k ohm SIP, 9-Pin	8292247
RP9	Res. Pak, 4.7k ohm SIP, 6-Pin	8293247
Intergrated Circuits		
U1	IC, 74F32 Quad 2-IN OR, 16-Pin	8015032
U2	IC, 74S04 Hex Inverter, 14-Pin	8010004
U3	IC, MCM3482B 8-Bit Latch, 20-Pin	8051482
U4,U5	IC, 74LS245 Octal Transceiver, 20-Pin	8020245
U6	IC, PAL16R6 Custom Array, 20-Pin	8040166
U7	IC, 74LS174 Hex D-Type Flip-FLop, 16-Pin	8020174
U8	IC, 74S00 Quad 2-IN NAND, 14-Pin	8010000
U9	IC, 74LS02 Hex Inverter, 14-Pin	8020002
U10	IC, 74LS11 Triple 3-IN AND, 14-Pin	8020011
U11-U13	IC, 8303B 8-Bit Transceiver, 20-Pin	8060303
U15	IC, AM9519A Interrupt Controller, 28-Pin	8040519
U16	IC, 74S04 Hex Inverter, 14-Pin	8010004
U17	IC, 74LS32 Quad 2-IN OR, 14-Pin	8020032
U18	IC, 74LS08 Quad 2-IN AND, 14-Pin	8020008
U19	IC, MCM68000 8 MHz 64-Pin	8041000
U20	IC, 74LS374 Octal Flip-Flop, 20-Pin	8020374
U21	IC, 74LS74 Dual Flip-Flop, 14-Pin	8020074
U22	IC, 74LS374 Octal Flip-Flop, 20-Pin	8020374
U23,U24	IC, 74LF283 Binary Full Adder, 16-Pin	8015283
U25	IC, 74LS74 Dual Flip-Flop, 14-Pin	8020074
U26	IC, 74LS138 Decoder Mux, 16-Pin	8020138
U27	IC, 74LS11 Triple 3-IN AND, 14-Pin	8020011
U28	IC, 8303B 8-Bit Transceiver, 20-Pin	8060303
U29	IC, 74LS374 Octal Flip-Flop, 20-Pin	8020374
U30	IC, 8303B 8-Bit Transceiver, 20-Pin	8060303

Parts List, MC68000 CPU Board, 8898855

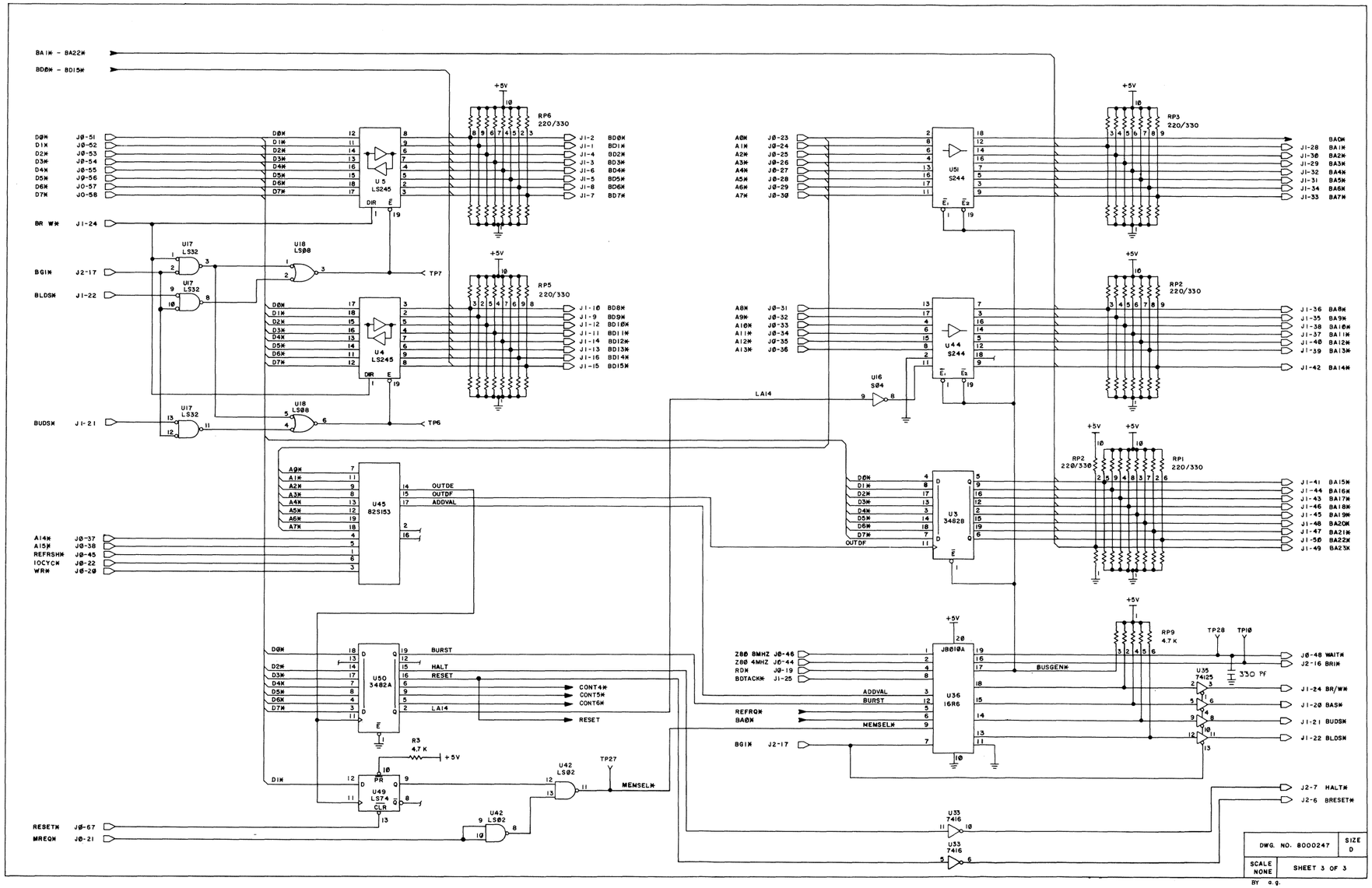
Ref No.	Description	Part No.
Intergrated Circuits		
U31	IC, 74F240 8-Bit Buffer Inv, 20-Pin	8015240
U32	IC, 74LS123 Dual Mul., 16-Pin	8020123
U33	IC, 7416 Hex Invert Buf Driv, 14-Pin	8000016
U34	IC, 74F138 Multiplexer, 16-Pin	8015138
U35	IC, 74LS125 Tri-state Buffer, 14-Pin	8020125
U36	IC, PAL16R6A Custom Array, 20-Pin	8041166
U37	IC, 74LS374 Octal Flip-Flop, 20-Pin	8020374
U38	IC, 74LS682 8-Bit Comparator, 20-Pin	8020682
U39	IC, 74LS393 4-Bit Binary Counter, 14-Pin	8020393
U40	IC, PAL16L8A Custom Array 20-Pin	8042168
U41	IC, 74LS138 Decoder Mux, 16-Pin	8020138
U42	IC, 74S00 Quad 2-IN NAND 14-Pin	8010000
U44	IC, 74S244 Octal Buffer, 20-Pin	8010244
U45	IC, 82S153, 20-Pin	8040153
U46	IC, 74F161 Counter, 16-Pin	8015161
U47	IC, 74F00 Quad 2-IN NAND, 14-Pin	8015000
U48	IC, PAL16R4 Custom Array, 20-Pin	8_____
U49	IC, 74LS74 Dual Flip-Flop, 14-Pin	8020074
U50	IC, MCM3482A 8-Bit Latch, 20-Pin	8050482
U51	IC, 74S244 Octal Buffer 20-Pin	8010244
U52	IC, 74F86 Quad 2-IN OR, 14-Pin	8015086
U53	IC, 74F175 Quad Flip-Flop 16-Pin	8015175
Sockets		
---	Socket, 20-Pin (U3)	8509009
---	Socket, 20-Pin (U6)	8509009
---	Socket, 28-Pin (U15)	8509007
---	Socket, 64-Pin (U19)	8509016
---	Socket, 20-Pin (U36)	8509009
---	Socket, 20-Pin (U40)	8509009
---	Socket, 20-Pin (U45)	8509009
---	Socket, 20-Pin (U48)	8509009
---	Socket, 20-Pin (U50)	8509009
Miscellaneous		
Y1	Oscillator, 48.0 MHz, 0.01%, HC-18	8409040



Schematic, MC68000 CPU Board, 8000247, Page 1 or 3



Schematic, MC68000 CPU Board, 8000247, Page 2 or 3



Schematic, MC68000 CPU Board, 8000247, Page 3 or 3

7.3 Memory Board

The TANDY 6000/6000-HD Memory board is a Random Access Memory (RAM) with a total capacity of 512K words (1 MEG bytes) of data with optional byte parity for error detection. It is designed for use with the MC68000 processor system. The MC68000 has a 16-bit wide data bus and, therefore, the memory is 16 bits wide.

Because the MC68000 needs to handle both 8- and 16-bit wide data transactions, the memory is further divided into upper and lower bytes (8-bit). Actually, all transfers to and from memory are treated as byte transfers. If a full 16-bit transfer is desired, an upper and lower byte transaction is performed simultaneously. Thus, the memory is organized as two parallel byte memories that share a common memory space.

Since parity is checked on all transfers, if the option is enabled, the parity generating/checking has to be set up on a byte basis. Therefore, each byte has a ninth bit added called a parity bit. Parity is a scheme where the total number of bits that equal one in every valid memory location is either EVEN or ODD. The TANDY 6000/6000-HD memory uses the ODD scheme. Thus, if the data has an even number of bits equaling 1 (0, 2, 4, 6, or 8), the parity bit will equal 1, making the total number of bits equal 1 or ODD parity. Otherwise, the parity bit equals 0 or EVEN.

The TANDY 6000/6000-HD Memory Board can be functionally divided into four main parts:

Memory

Address Circuits

Control/Timing Circuits

Parity Circuits

7.3.1 Memory

By understanding the requirements of the memory ICs, the address and timing circuits are more easily understood. The basic memory element is a DRAM (Dynamic Random Access Memory) IC containing 65,536 (64K) or 262,144 (256K) single-bit locations. Therefore, to store each byte with parity, nine ICs are required.

Two particulars of dynamic RAMs are address multiplexing and refresh. There are 16 address lines required to access 64K DRAMs and 18 address lines are required for 256K DRAMs. Address line A0, internal to the MC68000 CPU, is used to distinguish between upper (if A0=1) and lower (if A0=0) bytes. Since this least significant bit is used to determine selection of the upper or lower byte, the address is then contained in bits A1 through A16 for the 64 DRAMs and A1 through A18 for 256K DRAMs.

The address lines are loaded into memory in two parts:

First the Row address (A1-A8, A17), by the Row Address Strobe (RAS)

Second the Column address (A9-A16, A18), by the Column Address Strobe (CAS)

Once the addresses are loaded, the memory alters or presents the data at that location, depending on the state of the Read/Write (R/W*) signal. Refresh is required to maintain the information stored in the RAMs.

Every 2 milliseconds the entire contents of the RAM must be refreshed. This requires 128 refresh-only accesses every 2.0 msec, or one every 16.0 usec for the 64K DRAMs. The 256K DRAMs require 256 refresh-only accesses every 4 msec. The refresh cycle is the same as a read cycle, except AMUX and CAS are not generated.

7.3.2 Address Circuits

Address lines BA1* through BA19* are routed to the board through three-line receiver-inverting buffers U2, U3 and U4 (74F240), which are permanently enabled.

The row address bits (A1-A8) are multiplexed with column address bits (A9-A16) by U48 and U29 (74F257). When enabled, during a non-refresh cycle, the outputs become the 8 multiplexed memory Address lines (MA0-MA7) after being routed through series resistors to reduce ringing and overshoot. A ninth memory address line is required for the 256K DRAMs and is generated by U15 (74F157). U15 multiplexes A17 and A18 to generate MA8.

Address lines A17 and A19 are optionally jump connected to the select input of U24 (74F158). This selects which row of RAM is to be read or written to during a memory cycle. When A17 is jumped for select is low, RAS1L* and RAS1U* will be enabled to select the first 64K word (128K bytes) in the 1st row of RAM. If A17 is high then RAS2L* and RAS2U* will be enabled to select the first 64K word or (128K bytes) in the second row of RAM. When A19 is jumped for select it changes the increments of the 64K words (128K bytes) to 256K words (512K bytes).

Address lines BA18*-BA22* are used to enable the memory board at a specific location within the MC68000 subsystem memory map allocation.

These address lines are connected to an 8-bit magnitude comparator U1 (74F521) that compares two 8-bit inputs. The address lines are compared to a preset value by the use of DIP switch S1. If the address lines BA18*-BA22* equal the preset value, the output of the comparator is asserted and enables the memory board. Refer to Table 7-4 for the proper setting of S1 and jumper options E1-E9.

7.3.3 Control/Timing

The control and timing signals consist of Bus Address Strobe (BAS*), Bus Upper Data Strobe (BUDS*), Bus Lower Data Strobe (BLDS*), Bus Read/Write (BR/W*), Memory Disable (BERR*), Bus Data Transfer Acknowledge (BDTACK*), and REFRESH (REFRESH*).

All control signals except BTACK* are input signals from the MC68000 CPU board and are interfaced to the memory board through U9 (74F244). Half of U9 is enabled continuously with U9 pin 19 grounded which buffers REFRESH*, BAS*, and BERR*. The other half of U9 controls BR/W*, BLDS*, and BULS* which allows memory cycles to the memory board. The address comparator (U1) enables these control lines when the address is within the correct address space.

The control lines are decoded by U10 (74F64) to start a memory cycle. When the correct decode occurs the output of U10 pin 8 (MEMCYC) clocks the D flip-flop (1/2 of U12) to start a pulse down the Delay Line U13. MEMCYC also enables the RASXX signals to issue RAS at time = 0. At time = 30 ns the output of U13 pin 12 switches the address of the multiplexers U48, U29, and U15. The 30 ns tap clocks 1/2 of U11 (74F74). The 60 ns tap clocks 1/2 of U12 (74F74) to enable CASX Signals to DRAMS. The 240 ns tap clocks 1/2 of U11 (74F74) which clears MEMCYC and limits the pulse to 240 ns.

Taps, 0, 140, and 180 of the Delay Line are used to generate BDTACK*. Each tap after 0 will insert 2 wait states in the memory cycle to enable the use of slower DRAMs. 150ns DRAMs are required for no wait state operation.

BERR* is a signal generated by the Memory Management Unit on the CPU board to prevent access to memory, especially writes. If BERR* is issued after a memory cycle has started, BERR* is inverted by 1/6 of U17 and disables the address comparator. This will disable half of U9 to negate BR/W*, BLDS*, BUDS*. This will negate the WRX and CASX signals to DRAM to abort the cycle. RASXX signals are allowed to finish to prevent short cycling of the DRAM. RAS without CAS becomes a refresh cycle.

REFRESH* signal will cause all present memory boards to issue a refresh cycle. REFRESH* (REFRESH) will first disable address multiplexers U48, U29 and U15 and then enable buffer U28 (74F244). This buffers the refresh address to the DRAMs. The refresh address is generated by an 8 bit counter U14 (74LS393). At the end of each refresh cycle, the counter is clocked to the next 256 byte address. REFRESH* also asserts MEMCYC and clocks 1/2 of U12 to assert 700. The 30 nsec tap then clocks 1/2 of U11 (74F74) to disable U24 (74F158) this will bring all outputs of U24 to a low state and asserts all RAS* signals to the DRAMs. The 30 ns tap is used to allow the address to be properly setup before the RAS* signals are asserted. At time = 240 MEMCYC is cleared, which negates the RAS* signals. This allows the RAS* signals to be asserted for a minimum of 210ns which meets the requirements for 200ns DRAMs.

	S1							
			(B18)		(B19)	(B22)	(B20)	(B21)
	1	2	3	4	5	6	7	8
Disable Board	X	0	X	X	X	X	X	X
000000-03FFFF	X	1	0	X	0	0	0	0
040000-07FFFF	X	1	1	X	0	0	0	0
080000-0BFFFF	X	1	0	X	1	0	0	0
0C0000-0FFFFF	X	1	1	X	1	0	0	0
100000-13FFFF	X	1	0	X	0	0	1	0
140000-17FFFF	X	1	1	X	0	0	1	0
180000-1BFFFF	X	1	0	X	1	0	1	0
1C0000-1FFFFF	X	1	1	X	1	0	1	0
200000-23FFFF	X	1	0	X	0	0	0	1
240000-27FFFF	X	1	1	X	0	0	0	1
280000-2BFFFF	X	1	0	X	1	0	0	1
2C0000-2FFFFF	X	1	1	X	1	0	0	1
300000-33FFFF	X	1	0	X	0	0	1	1
340000-37FFFF	X	1	1	X	0	0	1	1
380000-3BFFFF	X	1	0	X	1	0	1	1
3C0000-3FFFFF	X	1	1	X	1	0	1	1
400000-43FFFF	X	1	0	X	0	1	0	0
440000-47FFFF	X	1	1	X	0	1	0	0
480000-4BFFFF	X	1	0	X	1	1	0	0
4C0000-4FFFFF	X	1	1	X	1	1	0	0
500000-53FFFF	X	1	0	X	0	1	1	0
540000-57FFFF	X	1	1	X	0	1	1	0
580000-5BFFFF	X	1	0	X	1	1	1	0
5C0000-5FFFFF	X	1	1	X	1	1	1	0
600000-63FFFF	X	1	0	X	0	1	0	1
640000-67FFFF	X	1	1	X	0	1	0	1
680000-6BFFFF	X	1	0	X	1	1	0	1
6C0000-6FFFFF	X	1	1	X	1	1	0	1

0 = Off = Open
1 = On = Closed
X = Don't Care

128K or 256K Board Jumpers E1-E2 64K
E4-E5 64K
E8-E9 64K

128K or 256K Memory Map Select Table

Table 7-4. Memory Map Select Tables

	S1							
					(BA19)	(BA22)	(BA20)	(BA21)
	1	2	3	4	5	6	7	8
Disable Board	X	0	X	X	X	X	X	X
000000-07FFFF	X	1	X	X	0	0	0	0
080000-0FFFFF	X	1	X	X	1	0	0	0
100000-17FFFF	X	1	X	X	0	0	1	0
180000-1FFFFF	X	1	X	X	1	0	1	0
200000-27FFFF	X	1	X	X	0	0	0	1
280000-2FFFFF	X	1	X	X	1	0	0	1
300000-37FFFF	X	1	X	X	0	0	1	1
380000-3FFFFF	X	1	X	X	1	0	1	1
400000-47FFFF	X	1	X	X	0	1	0	0
480000-4FFFFF	X	1	X	X	1	1	0	0
500000-57FFFF	X	1	X	X	0	1	1	0
580000-5FFFFF	X	1	X	X	1	1	1	0
600000-67FFFF	X	1	X	X	0	1	0	1
680000-6FFFFF	X	1	X	X	1	1	0	1

512K Board Jumpers E1-E2 64K
E5-E6 256K
E7-E8 256K

512K Memory Map Select Table

	S1							
						(BA22)	(BA20)	(BA21)
	1	2	3	4	5	6	7	8
Disable Board	X	0	X	X	X	X	X	X
000000-07FFFF	X	1	X	X	X	0	0	0
080000-0FFFFF	X	1	X	X	X	0	1	0
100000-17FFFF	X	1	X	X	X	0	0	1
180000-1FFFFF	X	1	X	X	X	0	1	1
200000-27FFFF	X	1	X	X	X	1	0	0
280000-2FFFFF	X	1	X	X	X	1	1	0
300000-37FFFF	X	1	X	X	X	1	0	1

1MEG Board Jumpers E2-E3 256K
E5-E6 256K
E7-E8 256K

1MEG Memory Map Select Table

Table 7-4. Memory Map Select Tables (Cont.)

7.3.4 Parity

There are two parity circuits:

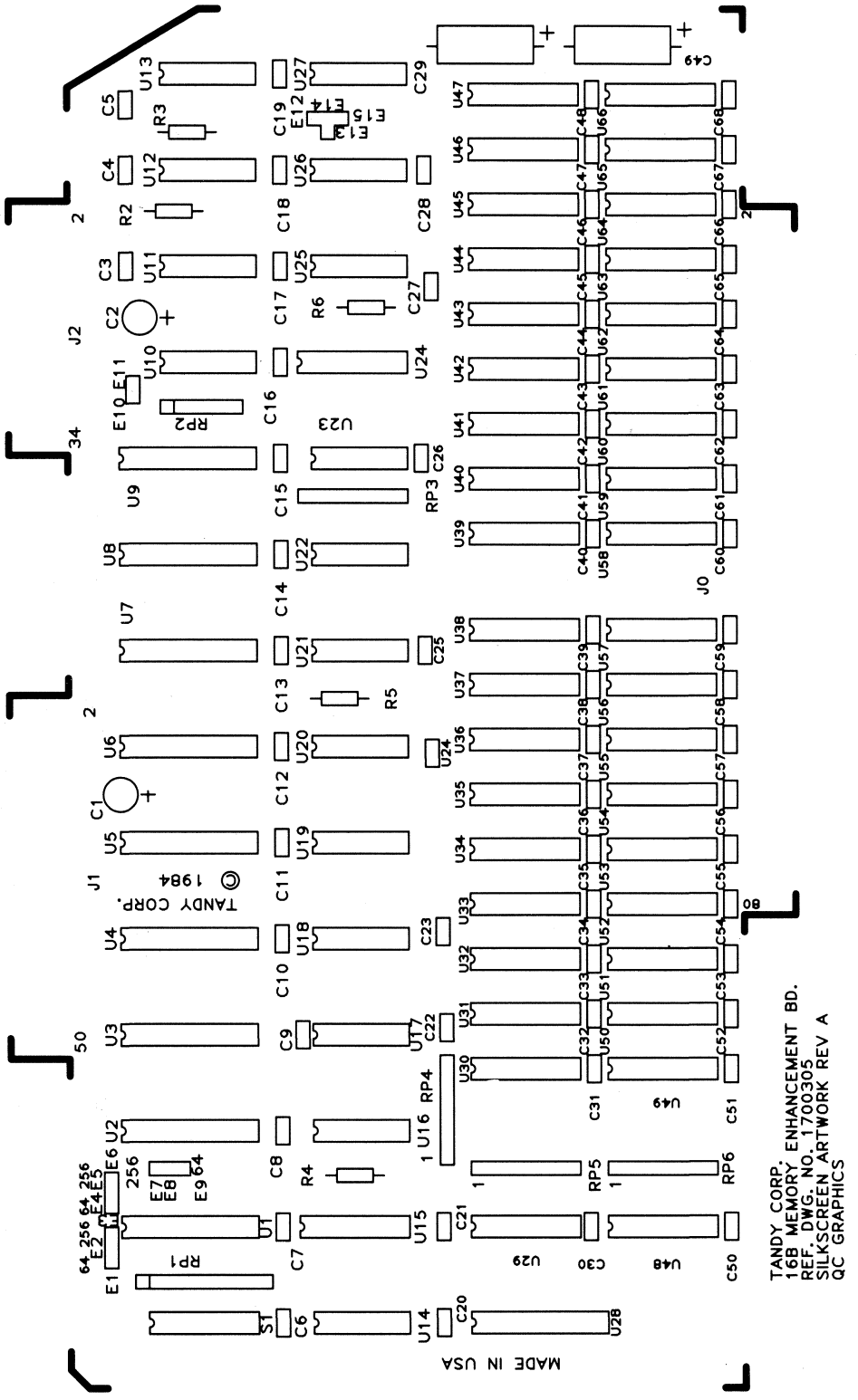
. Input parity generators

. Output parity checkers

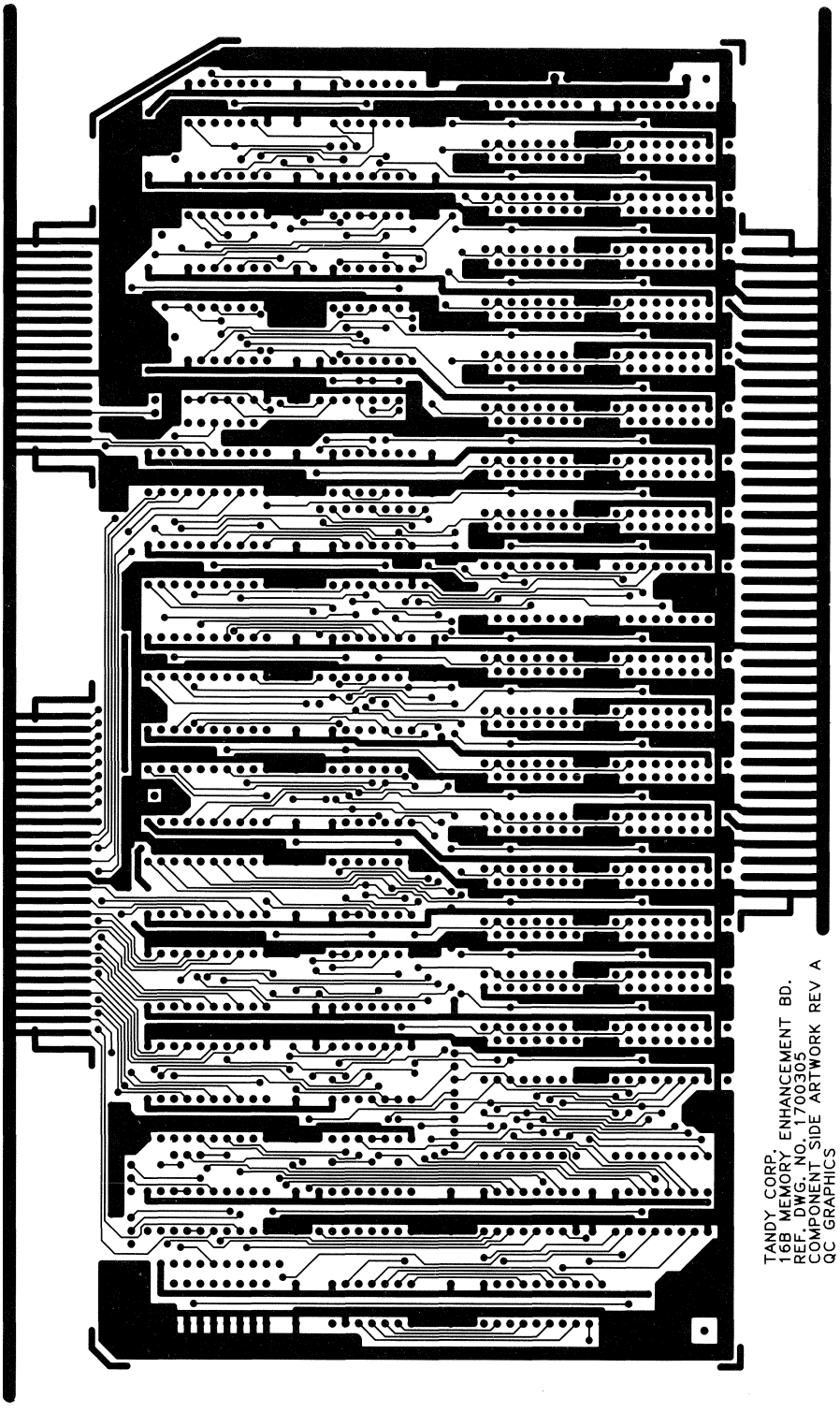
Since there is byte parity, there is one parity bit for each byte. When data is being written to a memory location, the data is monitored by the input parity generators.

The output of this generator is written into the same memory location as the ninth or parity bit. When a byte is being read from a memory location, all nine bits are monitored by the output parity checkers (the parity bit is not passed on to the bus). If the parity is correct, the output is a logic 1.

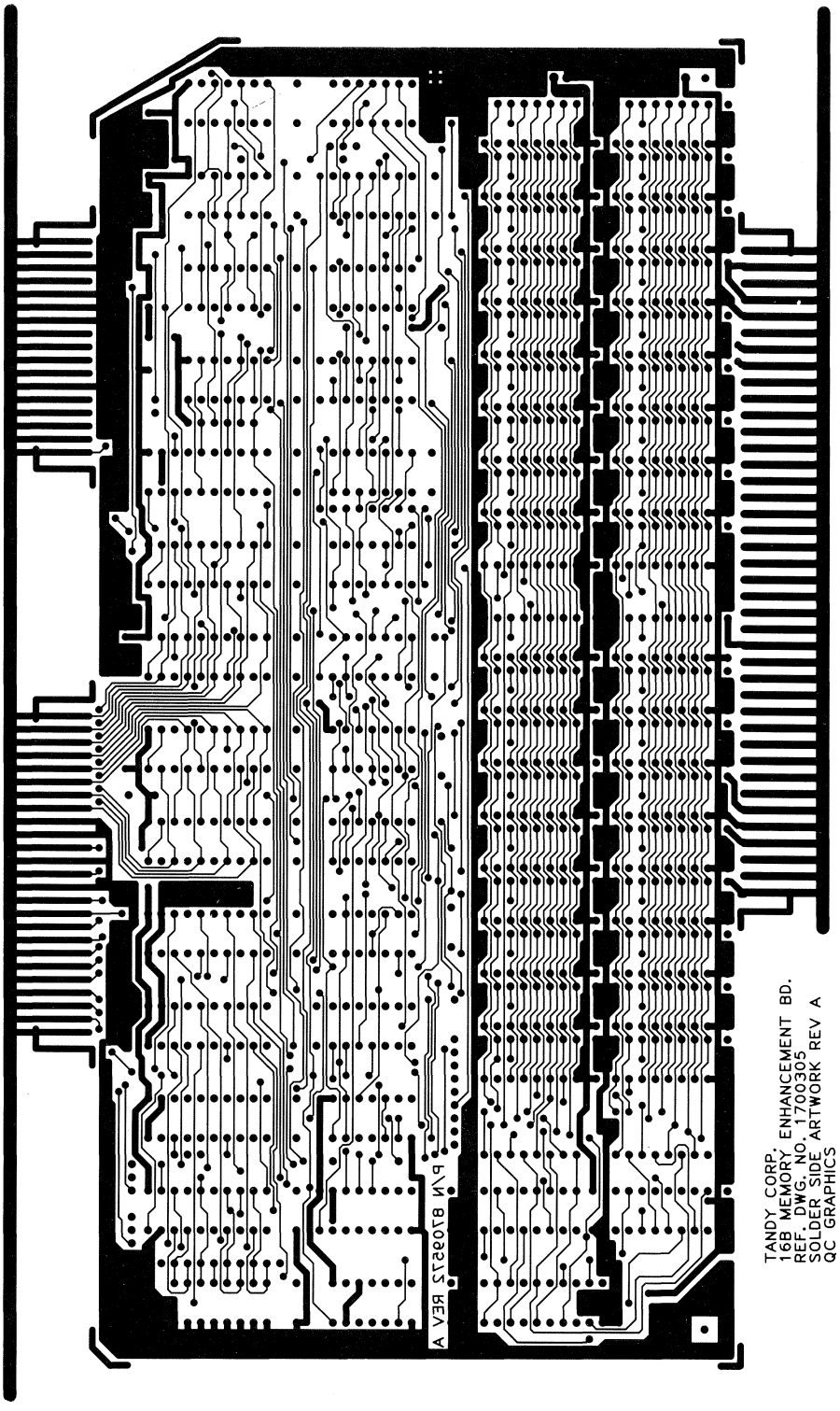
If the parity is incorrect, a logic 0 is strobed into D flip-flop U27 by CAS*. This signal is then routed to the next selected system interrupt. The signal is cleared by the next good parity memory cycle. Parity is an optional feature. The lack of it does not alter the memory operation.



Component Layout, 512K Memory Board



Circuit Trace, 512K Memory Board, Component Side



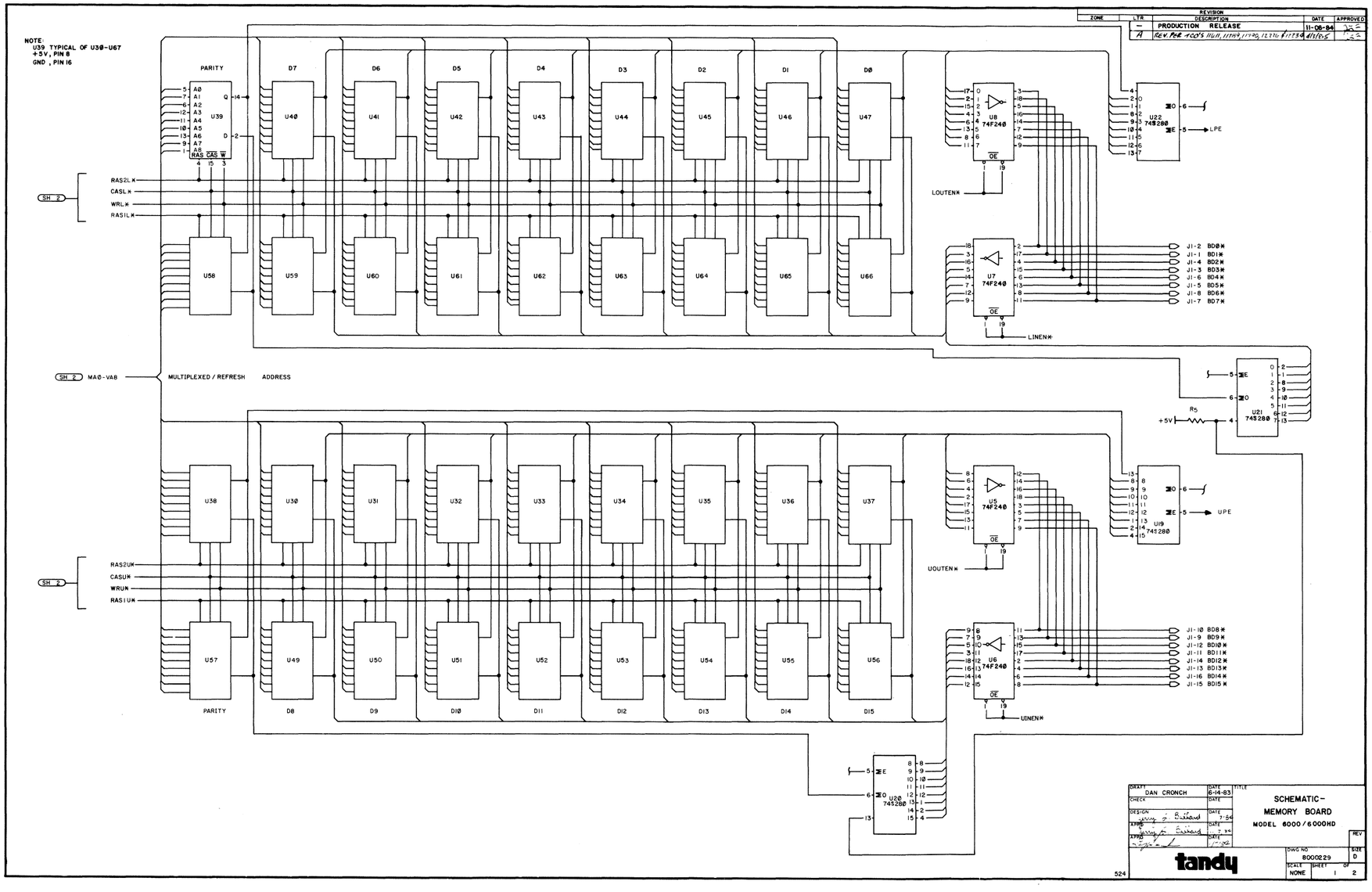
Circuit Trace, 512K Memory Board, Solder Side

Parts List, Memory Board, 8898854

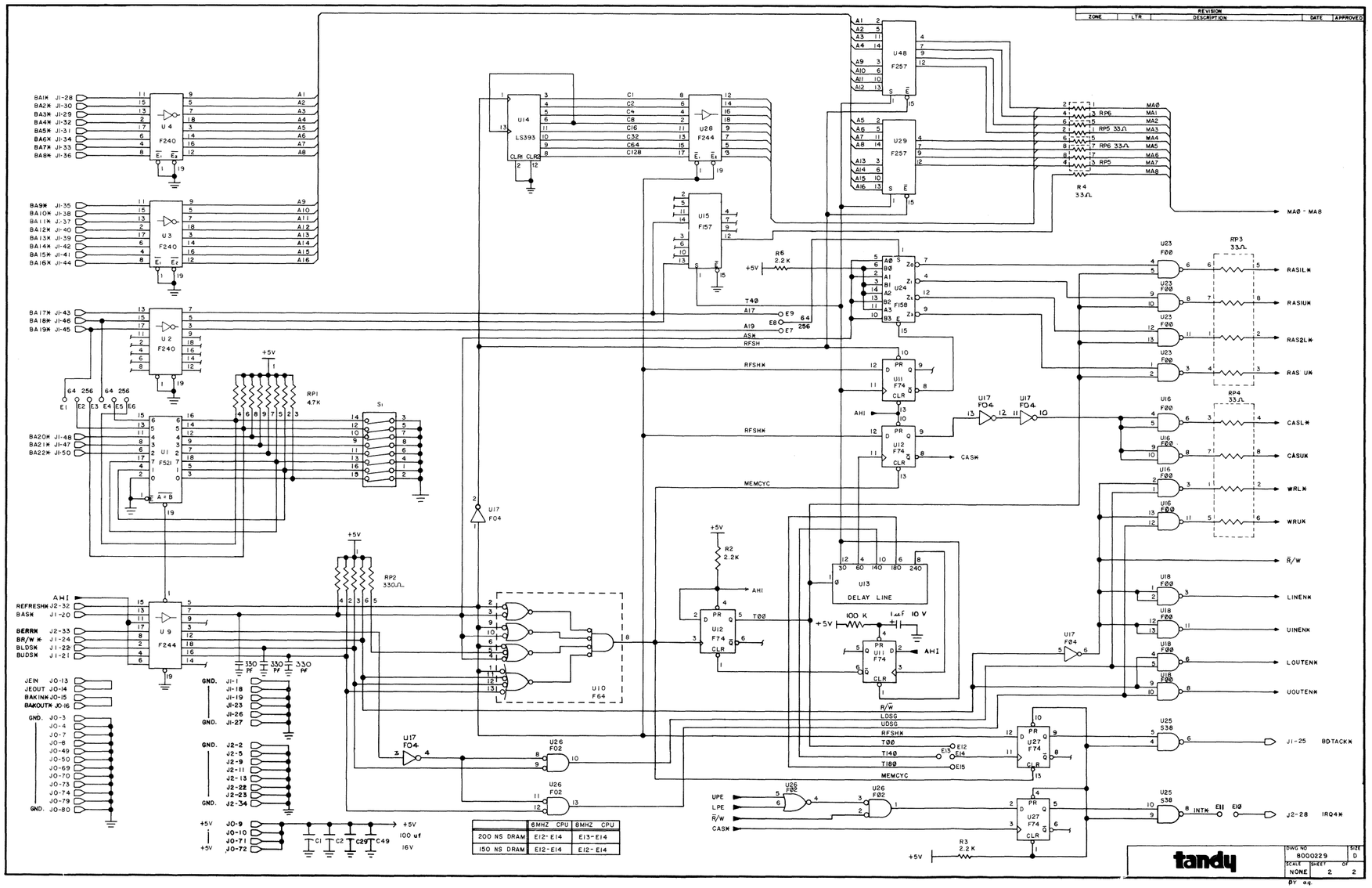
Ref No.	Description	Part No.
	6000 Memory PC Board Rev. A	8709572
---	Cable, 34 Pos, Int. Bus. Ext. II	8709391
---	Cable, 50 Pos, Int. Bus. Ext. II	8709387
Capacitors		
C1	Capacitor, 100 uF, 16V, Mono-Axial	8327101
C2	Capacitor, 100 uF, 16V, Mono-Axial	8327101
C3-23	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C26-28	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C29	Capacitor, 100 uF, 10V, Elect. Ax.	8317100
C30-38	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C41-48	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C49	Capacitor, 100 uF, 10V, Elect. Ax.	8317100
C50-58	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
C61-68	Capacitor, 0.1 uF, 50V, Mono-Axial	8374104
	Capacitor, 1 MFD,16V,	8325101
Jumper Plugs		
E1,E2	Jumper Plug	8519021
E5,E6	Jumper Plug	8519021
E7,E8	Jumper Plug	8519021
E12-E14	Jumper Plug	8519021
Stacking Pins		
E1-E15	Stacking Pin	8529014
Resistors		
R2,R3	Resistor, 2.2k Ohm, 1/4W, 5%	8207222
R4	Resistor, 33 Ohm, 1/4W, 5%	8207033
R5,R6	Resistor, 2.2k Ohm, 1/4W, 5%	8207222
	Resistor, 100k Ohm, 1/4W, 5%	8207410
Resistor Paks		
RP1	Network, 4.7 kohm, 10-Pin SIP	8294247
RP2	Network, 330 ohm, 6-Pin SIP	8295053
RP3-6	Network, 33 ohm, 8-Pin SIP	8295033
Switches		
S1	Switch, Dip 8-POS	8489004

Parts List, Memory Board, 8898854

Ref No.	Description			Part No.
Integrated Circuits				
U1	IC,	74F521, Comparator	20-Pin	8015521
U2-4	IC,	74S240, Octal Bus Line Driver,	20-Pin	8015240
U5-8	IC,	74ALS240,	20-Pin	8025240
U9	IC,	74F244, Octal Buffer,	20-Pin	8015244
U10	IC,	74F64, AND-OR Inverter,	14-Pin	8015064
U11-12	IC,	74F74, Dual JK Flip-Flop,	14-Pin	8015074
U13	IC,	, Delay Line(240ns)	14-Pin	8429027
U14	IC,	74LS393, Dual 4-Bit Binary Counter		8020393
U15	IC,	74F157, Multiplexer	16-Pin	8015157
U16	IC,	74F00, Quad 2-IN NAND,	14-Pin	8015000
U17	IC,	74F04, Hex Inverter,	14-Pin	8015004
U18	IC,	74F00, Quad 2-IN NAND,	14-Pin	8015000
U23	IC,	74F00, Quad 2-IN NAND,	14-Pin	8015000
U24	IC,	74F158, Quad Multiplexer,	16-Pin	8015158
U25	IC,	74S38, Quad 2-IN NAND OPEN-C,	20-Pin	8015521
U26	IC,	74F02, Quad 2_IN NOR	14-Pin	8015002
U27	IC,	74F74, Dual $\overline{JK}$ Flip-Flop,	14-Pin	8015074
U28	IC,	74F244, Octal Buffer,	20-Pin	8015244
U29	IC,	74F257, Quad Multiplexer,	16-Pin	8015257
U48	IC,	74F257, Quad Multiplexer,	16-Pin	8015257
U49-56	IC,	256K, Dynamic RAM (150ns),	16-Pin	8049008
U59-66	IC,	256K, Dynamic RAM (150ns),	16-Pin	8049008
Sockets				
	Socket, 20-Pin (U5-8)			8509009
	Socket, 16-Pin (U30-37, 40-47) (U49-56, 59-66)			8509003



Schematic, Memory Board, 8000229, Page 1 of 2



Schematic, Memory Board, 8000229, Page 2 of 2

7.4 Main Logic Board

The Main Logic board is a complete eight-bit microprocessor system minus the video interface. The board features the Z80A family of ICs which provides two serial communications channels (RS-232), a printer interface (parallel) and DMA capability. Additionally, it has two Floppy Disk interfaces and 64K bytes of RAM memory expandable to 128K bytes. The system is functionally equivalent and software compatible with the TRS-80 MODEL II.

A block diagram of the board is shown in Figure 7-9. From this diagram, it can be seen that the board is divided functionally into three sections; CPU, MEMORY and PERIPHERAL. The CPU section consists of a Z80A micro-processor, Z80A DMA, and the support circuitry to control the bus. The MEMORY section consists of 64K/128K of dynamic RAM, 2K of ROM, and the necessary timing control circuity. The PERIPHERAL section consists of a Z80A CTC, SIO (serial), PIO(printer), a FLOPPY DISK CONTROLLER and a sound circuit interface.

7.4.1 CPU Section

1. Processor

The PROCESSOR subsection consists of the Z80A CPU and DMA VLSI ICs. For particular details, refer to the manufacturer's specifications for these parts in Appendix A. The Z80A CPU operational particulars are 4.0 MHz clock rate, Mode 2 interrupt processing and control of memory refresh. The DMA and the CPU are both 'bus masters' and share the same bus support and buffer circuity.

2. Support

The SUPPORT subsection consists of the Reset, Clock and Wait circuits.

*RESET (schematic, sheet 2)- consists of two parts - "power-on" and "manual". Before power is applied, all capacitors are discharged. Upon power application, the first comparator (1/4 of U4, output pin 14) waits until the +5 VDC has risen above +4 V at which time it triggers (pin 8 is reference input 4V determined by CR1). C24 slows +5V input into pin 9, starting the charging of C3. The second

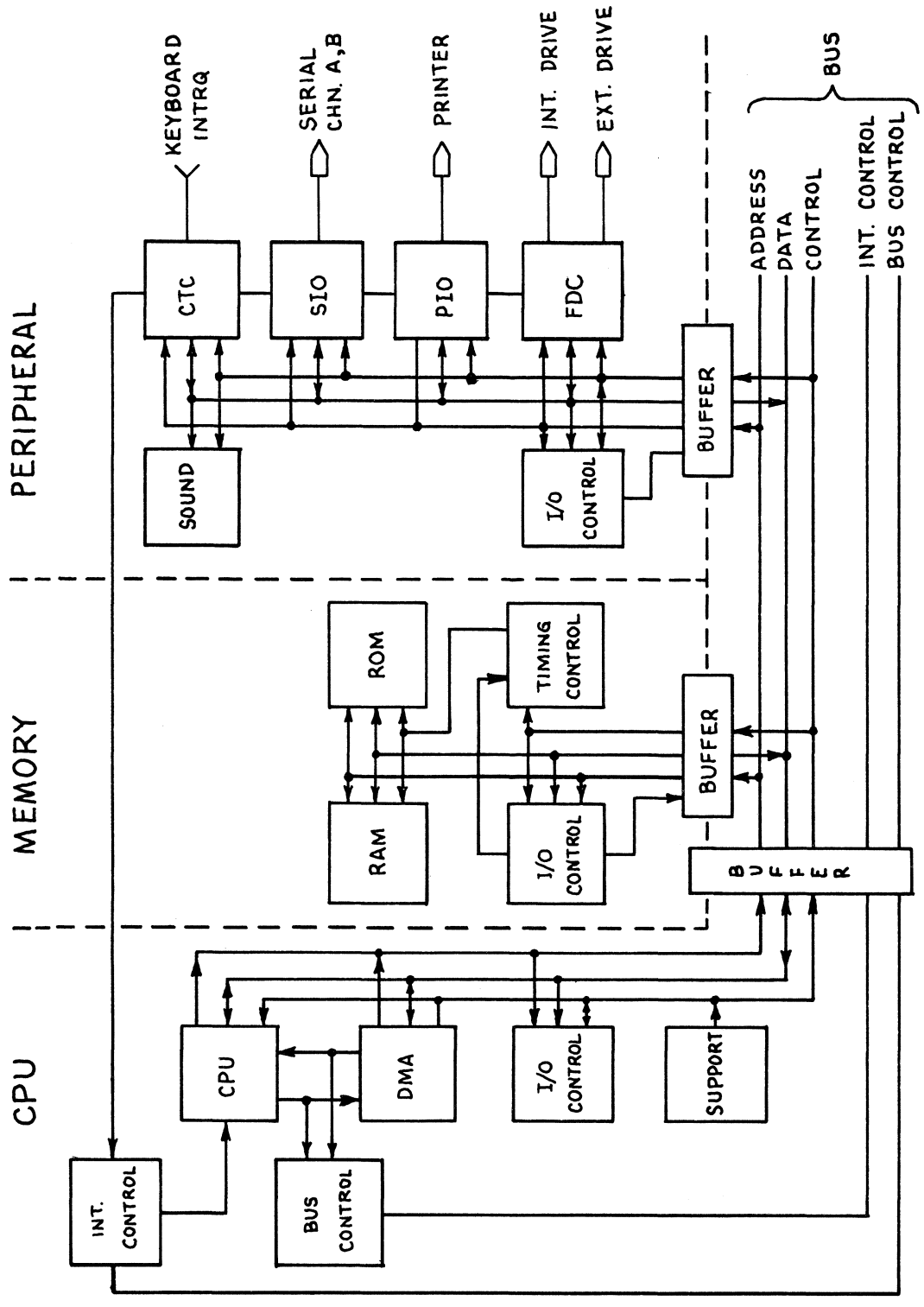


Figure 7-9. I/O Processor PCB Block Diagram

comparator triggers when C3 is charged to generate a pulse of at least 100 microseconds. On a "manual" reset (front panel switch), a third comparator generates a pulse longer than the (normal) switch bounce. The trailing edge of this pulse triggers a one-shot pulse of at least 50 microseconds. The two pulses -- "power on" and "manual" -- are logically ORed together to make the system reset signal RST/.

*CLOCK (schematic, sheet 2)- consists of an oscillator (half of U13), a divider (U6) and a buffer (half of U13). The oscillator frequency is 8.00 MHz and is crystal-controlled for stability. It is connected to the frequency divider by jumper E4-E5, which is provided to isolate the clock for testing purposes. The divider converts the 8.0 MHz into a 4 MHz clock and a 2 MHz clock that are then buffered by TTL gates for system use. In addition, the 4 MHz clock is also applied to a special buffer to generate the Z80 family high level clock. This special buffer uses a transistor (Q1) with a low Vce saturation as an active pull-up to obtain the required Voh of +4.6/5.2 V. The '04 TTL gate provides the Vol of +0.8/-0.3 V and switches the transistor on/off through the resistor network (R19,R20,C6).

*WAIT (schematic,sheet 1) - consists of two parts; a "fixed" wait circuit and an "user" wait circuit. The "fixed" wait circuit (U3) generates a "wait" request signal under two conditions. The first is when the boot ROM is enabled. The ROM has an access time longer than a normal CPU memory cycle and therefore it is necessary to insert a "wait" cycle for every memory access cycle. The second condition is when the ROM is disabled. The fetch (M1) cycle of every memory access is followed by a memory refresh cycle. To ensure sufficient dynamic RAM precharge time, a "wait" is inserted each time. The "user" wait circuit receives the signal EWAIT/ from any user on the BUS that requires longer access times than the CPU normally provides (example is the Video /Keyboard Interface PCB). Each user has an open-collector buffer for a wired-OR connection to the BUS. the CPU section simply provides the pull-up for the common output. For the CPU, the "fixed" and the "user" wait signals are ORed together and applied directly to the CPU. For the DMA, the "wait" and "chip select" signals share the same IC pin. These two signals are logically combined with BUSACK and BAO to choose between F8 (chip select) and EWAIT/. If BUSACK/ is false, F8 is applied. If BUSACK/ and BAO are true, the DMA is the bus master and EWAIT/ is applied. The DMA uses only the "user" wait signal EWAIT/.

3. Buffers

The CPU and DMA are bus masters; they transmit the address and control signals onto the bus. Data is both transmitted and received by all entities on the bus.

*Address buffers (U24,U25)- Disabled only if external bus master has control (BAO = lo)

*Control buffers (U26,U27)- Disabled only if external bus master has control (BAO = lo).

*Data transceiver (U30)- directional control signals IN (read), OUT (write). OUT is the defaulted direction; disabled if external bus master has control. IN equals CPU/DMA READ unless:

1. CPU I/O read of DMA (DMARD) = lo

2. CPU reading the DMA interrupt vector (INACKOFF/) = lo.

4. I/O Control

The I/O Control decodes the address and control signals to create the CPU section port read/write strobes MEMCFG/, SYSCFG/, OPSCFG/ and F8 plus the logic discretes F8IO and DMARD. The decoder is U10, a custom logic array. See Table 7-5 for a listing of each port strobe and its use.

5. Bus Control

The Bus Control circuity receives the "bus requests" from the DMA and other bus masters on the BUS and provides the logic for arbitrating the "bus grant" from the CPU. The Bus Control circuit has two parts, input and output. The input circuit ORs the "bus request" signals BUSREQ/ (from the DMA) and BUSREQ* (from the BUS) for the CPU. Each bus master is connected to the BUS through an open-collector buffer to wire-OR all requests. The CPU provides the common pull-up for the output. The output circuit buffers the DMA daisy-chain acknowledge signal BAO onto the BUS for any external bus master (none at present).

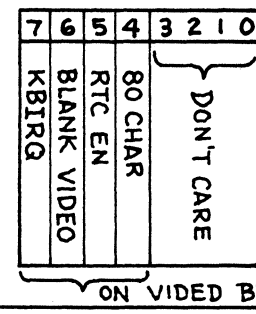
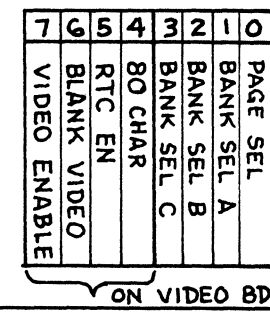
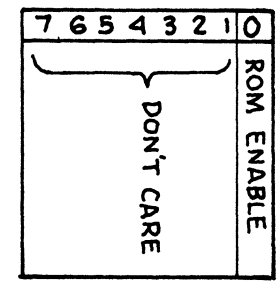
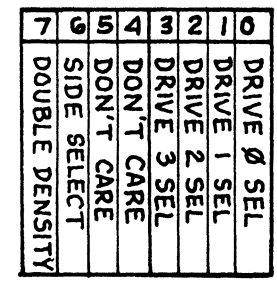
PORT	STROBE NAME	READ	WRITE
FF	MEMCFG/		
F9	SYSCFG/	NO FUNCTION	
F8	F8/	DMA STATUS	DMA COMMAND
F4-F7	SIOCE/	SIO STATUS AND DATA	SIO COMMAND AND DATA
FØ-F3	CTCCE/	CTC	CTC
EF	DRVSEL/	NO FUNCTION	

Table 7-5. Input/Output Port Map

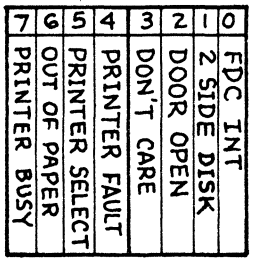
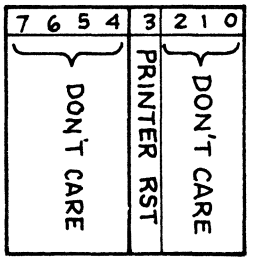
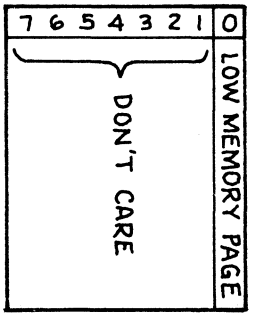
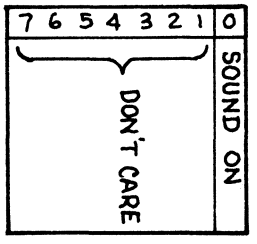
E8	SOFTMR/	NO FUNCTION	FDC RESET
E4-E7	FDCCE/	FDC STATUS AND DATA	FDC COMMAND AND DATA
EØ-E3	PIOCE/		PIO COMMAND AND DATA
EØ			
A8	OPSCFG/	NO FUNCTION	
AØ	SNDCE/	NO FUNCTION	

Table 7-5. Input/Output Port Map (con't)

6. Interrupt Control

The CPU has two types of interrupts; maskable (INT/) and non-maskable (NMI/). The non-maskable interrupt (bus name NMIRQ*) is a Method 1 type interrupt (see Z80 specification). The sources for this signal are on the BUS only. Like the "wait" and "bus request" signals, the sources apply their signal onto the bus through an open-collector buffer and the CPU section provides the pull-up resistor for the wired-OR output. At present, the only source for this signal is the REAL TIME CLOCK on the Video/Keyboard Interface PCB. The maskable interrupt (INTRQ/) is a Mode 2 type interrupt. All sources are on a daisy-chain priority scheme where interrupt requests from all sources are ORed together but who gets to make the request is established by the acknowledge from the CPU being passed from the highest priority IC down until the requestor stops it, preventing lower priority ICs from responding (IEI,IEO). The requestors are divided into two groups; internal (INTRQ/) from the BOARD, and external (INTRQ*) from the bus. The priority scheme has the four Z80A functions on the board assigned the highest priority with a descending priority of CTC, SIO, DMA and PIO. The bus continues the priority scheme and establishes priority by position (provided a back plane with connectors is present) by daisy-chaining the acknowledges IEIN* (IEI), IEOUT* (IEO). If a board slot is empty, that stops the chain.

7.4.2 Memory Section

1. RAM

The RAM memory section consists of two sets of 8 dynamic RAM ICs and an address multiplexer. The first or base set of RAM (U82-U89) is 64K in size; the second set (U63-U70) is either 16K or 64K in size. The RAM memory is divided into 32K size groups called Pages of which there can be as many as 16 (0-15). See Table 7-6 for a memory map. Page 0 is called the Base Page and is always available at address 0-32K (if LOW PAGE = low; if LOW PAGE = hi, address 32K-64K). The other Pages are selected one at a time by a value (01-0F) at port FF and respond in the address range 32K-64K (if LOW PAGE = low; if = hi address 0-32K). The addresses for dynamic RAMs require multiplexing. This is done by U52, U53, and U79. The upper address bits are combined with the lower address in pairs to form RAC*s.

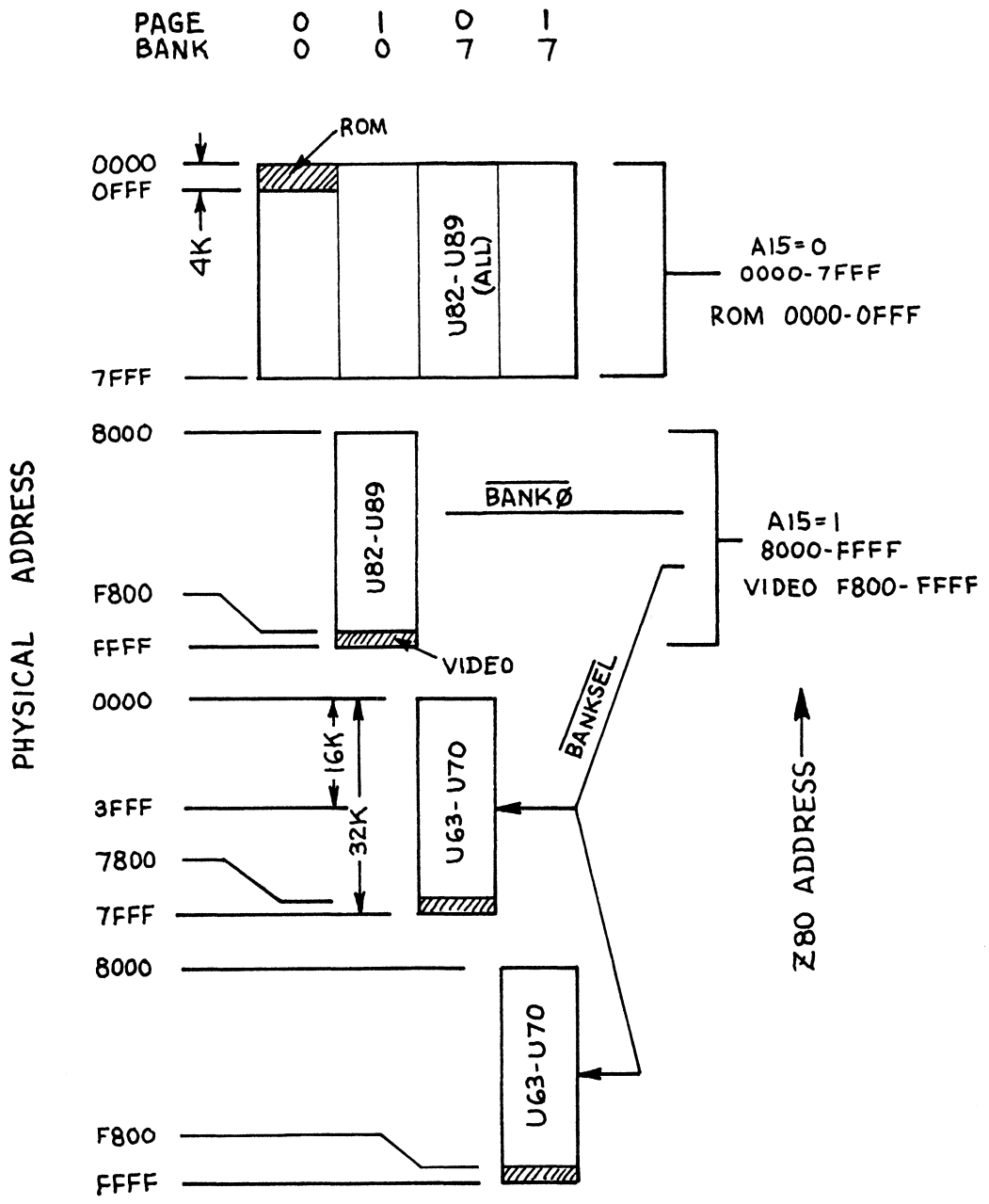


Table 7-6. Memory Map

RAC0 through RAC5 are usable for 16K and 64K RAMs, both banks. Unique address combinations are 16RAC6 (16K only, address bit 6), 64RAC6 (64K only, address bit 6), L64RAC7 (lower 64K address bit 7), and U64RAC7 (upper 64K address bit 7). Jumper options in the RAM section allow different configurations to be selected. See Table 7-7 for details.

Timing signals come from the TIMING/CONTROL section, which will be covered later.

2. ROM

The ROM memory subsection consists of U54, a 2K x 8 PROM called the BOOT ROM. This ROM memory shadows the RAM memory address space in the range 0-2K. This memory is available only if the discrete signal ROM from the port F9 is true. When the BOOT ROM is enabled, the shadowed RAM memory is write only (read disabled). An option to upgrade to a 4K x 8 part is provided by a jumper option for the address bit 11. Timing signals come from the TIMING/CONTROL section, which will be covered later.

3. I/O Control

The I/O CONTROL consists of a latch U51. The data is stored in the latch by the I/O Port strobe MEMCFG/ from the CPU Section. The outputs PAGE, BASEL, BBSEL, BCSEL are converted to BANK0 (Page 0, 1) and BANKSEL (Page 2,3 OR 4,5 OR....14,15) by U61. See Table 7-7 for page select jumper options. The VIDEO discrete enables the video RAM memory, which shadows the memory address range F800-FFFF. The I/O port discretes ROM and LOW PAGE originate from a latch in the CPU section.

E18, E19, E20	ROM SIZE OPTION		
*	E18-E19	2K x 8 ROM A11 = +5V	
	E19-E20	4K x 8 ROM A11 = A11	
E24, E25, E26	FLOPPY DRIVE HEAD LOAD DELAY OPTION		
*	E24-E25	NO DELAY	
	E25-E26	60 MILLISECOND DELAY	
E27, E28, E29	FLOPPY DRIVE SIGNAL "READY" SOURCE		
*	E27-E28	FROM FLOPPY DRIVE	
	E28-E29	SELECT LOGIC	
E30, E31, E49	FLOPPY CONTROLLER TEST MODE		
	E30-E31	TEST	
	E31-E49	NORMAL	
E40, E41	INTERNAL FLOPPY DRIVE OPTION		
*	E40-E41	1 INTERNAL DRIVE (Ø)	
	OPEN	2 INTERNAL DRIVES (Ø,1)	
E42, E43, E44, E45, E46, E47, E48	RAM U63-U70 CONFIGURATION OPTION		
	FOR 16K (PIN 4116)		
*	E42-E45	-5VDC TO PIN 1	(NO CONNECTION TO E48)
	E44-E45	-12VDC TO PIN 8	
	E46-E47	+5VDC TO PIN 9	
	FOR 64K (PIN 6665)		
	E45-E46	+5VDC TO PIN 8	(NO CONNECTION TO E42, E43, E44)
	E47-E48	URAC7 TO PIN 9	
E32 THRU E39	RAM BANK SELECTION OPTION, U63-U70		
	E32-E39	BANKSEL = PAGE 2,3	
*	E38-E39	BANKSEL = PAGE 15,16	
		(E33 THRU E37 NOT INSTALLED)	

* FACTORY SETTING

Table 7-7. Jumper Options

E1, E2, E3	RAM WAIT STATE OPTIONS	
*	E1-E2	WAIT STATE INSERTED DURING M1 CYCLE
	E2-E3	NO WAIT STATES
E4, E5	CLOCK OSCILLATOR OPTION	
*	E4-E5	8 MHZ OSCILLATOR CONNECTED TO CLOCK DIVIDER
	OPEN	NO CONNECTION
E6, E7, E8	OPTIONS FOR SERIAL CHANNEL B BAUD CLOCK	
*	E7-E8	INTERNAL (CTC) CLOCK SOURCE
	E6-E7	EXTERNAL CLOCK SOURCE
E9, E10, E11, E12	OPTIONS FOR SERIAL CHANNEL A BAUD CLOCK	
*	E10-E11	INTERNAL (CTC) CLOCK SOURCE
	E11-E12	EXTERNAL CLOCK SOURCE
	E9-E10	INTERNAL CLOCK ROUTED TO EXTERNAL- IN ADDITION TO E10-E11
E13, E14	PRINTER INTERFACE SIGNAL "PRIME" OPTION	
	E13-E14	CONNECTED
*	OPEN	NO CONNECTION
E15, E16, E17	RAM ADDRESS BIT 6 OPTION, U62-U69	
	E15-E16	16K OPERATION: 16RAC6
	E16-E17	64K OPERATION: 64RAC6

* FACTORY SETTING

Table 7-7. Jumper Options (con't)

E50, E51, E52	RAM UPPER BANK SIZE OPTION	
	E50-E52	64K SIZE
	E51-E52	16K SIZE
E53, E54, E55	OPTIONS FOR SERIAL CHANNEL A RECEIVE BAUD CLOCK	
*	E53-E54	INTERNAL (CTC) CLOCK SOURCE
	E53-E55	EXTERNAL CLOCK SOURCE

* FACTORY SETTING

Table 7-7. Jumper Options (con't)

4. TIMING/CONTROL

The TIMING/CONTROL subsection (schematic, sheet 5, 6) provides the necessary signals to access the memory and control the data transceiver. This circuity includes the memory controller U50, RAM timing generator circuit U39, U62, U80, U81 and ROM timing and data transceiver control U60, U49. The memory controller U50 decodes the addresses A11-A15, memory configuration discretes ROM, VIDEO, BANK0, BANKSEL, LOW PAGE and 16K to determine if a memory access should be in progress and, if it is, whether it is for ROM or for RAM. For ROM (ROM = hi, address range 0000-0FFF), the outputs ROMSEL and ROMAD are true (hi). If for RAM, BANK0 = lo, PAGE = hi (address 0000-FFFF unless VIDEO = hi, then address 0000-F800), the outputs RASEN0, CASEN are set true (hi). If for RAM, BANKSEL = lo (address 8000-FFFF unless VIDEO = hi, then address 8000-F800 unless 16K = hi then address 8000-BFFF) RASEN1, CASEN are set true (hi). If for Video memory, (VIDEO = hi, address F800-FFFF), the outputs are all false (lo). The input REFRESH sets all the outputs false during its true time. The AND-OR gate U39 is the RAM memory access decoder generating MEMREQ/, which triggers the RAS-CAS timing sequencer U61, U80, and U81. The equation for U39 is (MREQ*WRITE + MREQ*ROM*ROMAD*READ + MREQ*RAM*READ). Basically, this allows write access to the RAM memory for all addresses but limits the read accesses to only those addresses not shadowed by the ROM memory if ROM is true.

The RAM timing sequencer generates the RAS, CAS and MUXSEL to read, write and refresh the dynamic RAM ICs. For the lower memory bank RAS0, MUXSEL and CAS are required; for the upper bank RAS1, MUXSEL and CAS are needed. (RASEN0 and RASEN1 never occur together). The fixed timing sequence is generated by the delay line U80. When MEMREQ/ goes true (lo), (and for instance, RASEN0, CASEN are true) U81.6, U62.6 are set lo, and U81.7 stays hi. U81.6 sets RAS0P lo and U62.6 starts a negative level through the delay line. The 150 nanosecond tap clears U62.6, thereby creating a 150 ns negative pulse. This pulse, delayed 30 ns, = MUXSEL/, which switches the address multiplexer from the row address to the column address. The pulse delayed 60 ns sets U62.7 or CASP lo. The pulse delayed 240 ns clears RAS0P (U62.7). CASP flip-flop U81.7 is cleared by the trailing edge of MEMREQ/. This establishes a minimum length RAS* (240 ns) to insure the minimum pre-charge time for the RAS only REFRESH cycle to follow (if M1 cycle). Now, RASP (RAS Prime) is ORed with (MREQ*REFRESH) (RAS refresh) and applied to U82-U89 through damping resistor R60. CASP (CAS Prime) is buffered to U63-U89 through damping resistor R59.

The ROM timing seguence is simply (MREQ*ROMSEL) = ROMCE/; chip select and (ROMSEL*READ) = ROMOE/; output enable. REFRESH clears ROMSEL during refresh.

5. BUFFERS

The address buffers U42-43 receive the addresses from the BUS and apply them to the multiplexers, ROM and the memory controller.

The data transceiver is U44. Directional control is provided by logic gates U41, U49 and U60. The signals IN/ and OUT/ are normally off (hi) unless access is being made to the memory. U60 ORes the five signals that define the timing windows for this access - [(RAS0P*CASP + RAS1P*CASP) + ROMCE/ + MEMCFG/]. A disable signal DISO* (DISable Output, not presently used) negates the enable of U60.

7.4.3 Peripheral

1. CTC

The CTC is the Z80A COUNTER/TIMER CIRCUIT. It has two functions. One, it is used as a baud rate generator for the SIO function. Here channel 0 and 2 are tied together to provide a square wave clock for both channels of the SIO serial interface. Second, it is an interrupt processor for two interrupt signals; one from the keyboard KBIRQ* and USEIRQ* a growth input on the BUS. See schematic, sheet 3.

2. SIO

The SIO is the Z80A SERIAL INPUT/OUTPUT CONTROLLER. It provides two channels of serial (RS-232-C) communication. The two channels are labeled Channel A and Channel B. Channel A can be either synchronous or asynchronous. Channel B can be asynchronous only. They are available through flat ribbon cables at connectors at the rear of the chassis. The serial input/ output interface of the SIO is buffered by U7, U8, U14, U15 and U23 - line drivers and receivers operating from +12/-12VDC. Jumper options allow either external or internal (CTC) clocks for operation. See Table 7-7 for jumper details. See schematic, sheet 3. See Section 5 for a description of the SIO connector pin designations.

3. PIO

The PIO is the Z80A PARALLEL INPUT/OUTPUT CONTROLLER. It provides two parallel data interfaces; one is used as the data port for the printer and the other is used as an input port for status from the Floppy Disk Drive and Printer. Since both ports are interrupt driven, the second port (B) is used as an interrupt controller by the Floppy Disk Controller for data transfers. The printer interface (B), uses the output ready signal BRDY to trigger a one-shot to provide a 2.0 microsecond pulse for the printer handshake. See schematic, sheet 4. See Section 5 for a description of the PIO connector pin designations.

4. FDC

The FDC is the FLOPPY DISK CONTROLLER function. This circuit is designed to read and write an 8" Floppy Disk Drive (FDD) using single or two sided media in both single and double density formats. The major component in this circuit is the WD 2793 VLSI IC. This part synchronizes, reconstructs and reads the data, reads/writes status and provides write data in the proper format for a floppy disk drive. Additionally, it communicates with the CPU as an I/O device. Interface circuity is provided to interface with two sets of FDDs - 1 or 2 internal drives (in chassis) and 1 or 2 external expansion drives. Since the FDDs in a set are connected in parallel, only one set of drivers and receivers is required for each, the internal and the external set. The drivers are open-collector inverter gates designed to drive into a 150 ohm load to +5 vdc provided by one of the FDDs in a set. The receivers are 2:1 multiplexers - one channel for internal, one for external. The board provides the 150 ohm pull-up for the FDDs. FDD drive select logic is provided by programmable logic array U47. Here, the CPU via I/O port EF elects a single drive it wishes to communicate with, selects data density - single or double, and determines which channel of the input status mux to select. The head load timing circuit is provided for FDDs that have a seperate circuit for this function that times out the mechanical bounce. (In some newer FDDs, the head is loaded when the disk is installed but the motor is turned ON/OFF.) The one-shot is set-up for 3.0 milliseconds. See Table 7-7 for jumper options. See schematic, sheet 4. See Section 5 for a description of the FDC connector pin designations.

See Disk Drive Manual for alignment instructions.

5. SOUND

The SOUND function is an oscillator of fixed frequency and variable duration under software control. The oscillator is located on a separate satellite board. Power and tone duration control are provided by the I/O Processor PCB. The tone control circuit is 1/2 of D flip-flop U38. The sound is enabled as long as the signal SOUND = low. SOUND is the complement of U38.6, which is equal to CPU data bit 0 when I/O port strobe SNDCE/ (A8) is applied. See schematic, sheet 2 for the oscillator and sheet 4 for the control circuit.

6. I/O CONTROL

The I/O CONTROL circuit for the Peripheral section is U21, a programmable logic array. See Table 7-5 for address and function of the I/O ports CTCCE/, SIOCE/, PIOCE/, FDCCE/, SNDCE/, DRVSEL, SOFTMR/ and PGSEL/.

7. BUFFERS

The address and control buffers U31, U32, U56 are straight-forward, simple line receivers. The data transceiver control circuitry -- U5, 20, 29, 55 -- determines the direction of data flow. The default direction is in or write. To switch to read (drive the BUS), two conditions must occur. The first is that {PGSEL*READ} is true (low). (PGSEL is true if any of the other outputs of U47 is true). The second condition is that one of the three functions CTC, SIO or PIO has an interrupt acknowledge pending. See schematic, sheet 3.

PAL 12L6 (U10)

Pin Assignments:

```
READ CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 GND
IORQ WRITE SELECT FB SYSCFG MEMCFG DMARD OPSCFG F8IO VCC
```

Equations:

```
/MEMCFG = CA7*CA6*CA5*CA4*CA3*CA2*CA1*CA0*/IORQ*/WRITE
                                          ;FF*IORQ/*WRITE/
SYSMCFG = CA7*CA6*CA5*CA4*CA3*/CA2*/CA1*CA0*/IORQ*/WRITE
                                          ;F9*IORQ/*WRITE/
F8 = CA7*CA6*CA5*CA4*CA3*/CA2*/CA1*/CA0*/IORQ; DMA CHIP SELECT
DMARD = F8IO*/READ    ;DISABLE TRANSCEIVER DURING DMA I/O READ

/OPSCFG = CA7*/CA6*CA5*/CA4*CA3*/CA2*/CA1*/IORQ*/WRITE
                                    ;MEMORY LOW, PAGE SWAP

/SELECT = CA7*CA6*CA5*CA4*CA3*CA2*CA1*CA0*/IORQ*/WRITE
                                    ;CPU GROUP I/O SELECT
        + CA7*CA6*CA5*CA4*CA3*/CA2*/CA1*CA0*/IORQ*/WRITE
        + CA7*CA6*CA5*CA4*CA3*/CA2*/CA1*/CA0*/IORQ*
        + CA7*/CA6*CA5*/CA4*CA3*/CA2*/CA1*/CA0*/IORQ*/WRITE
```

PAL 16L8 (U21)

Pin Assignments:

```
PA7 PIORQ PA6 PA4 PA5 PA2 PA3 PA0 PA1 GND
PWRITE CTCCE SIOCE PIOCE FDCCE SOFTMR DRVSEL SNDCE PGSEL VCC
```

Equations:

```
IF (VCC) /CTCCE = PA7*PA6*PA5*PA4*/PA3*/PA2*
                                    ; COUNTER TIMER CHIP SELECT
                                    ; PORT F0-F3

IF (VCC) /SIOCE = PA7*PA6*PA5*PA4*/PA3*PA2*
                                    ; SERIAL INTERFACE CHIP
                                    : SELECT
                                    ; PORT F4-F7

IF (VCC) /PIOCE = PA7*PA6*PA5*/PA4*/PA3*/PA2*
                                    ; PARALLEL INTERFACE CHIP
                                    ; SELECT
                                    ; PORT E0-E3

IF (VCC) /FDCCE = PA7*PA6*PA5*/PA4*/PA3*PA2*/PIORQ
                                    ; FLOPPY DISK CNTLR CHIP
                                    ; SELECT
                                    ; PORT E4-E7

IF (VCC) /SOFTMR = PA7*PA6*PA5*/PA4*PA3*/PA2*/PA1*/PA0*
                                              /PIORQ*/PWRITE
                                    ; FDC SOFTWARE RESET
                                    ; E8*IORQ*WRITE

IF (VCC) /DRVSEL = PA7*PA6*PA5*/PA4*PA3*PA2*PA1*PA0*/PIORQ*
                                                    /PWRITE
                                    ; FLOPPY DISK DRIVE SELECT
                                    ; EF*IORQ*WRITE

IF (VCC) /SNDCE = PA7*/PA6*PA5*/PA4*/PA3*/PA2*/PA1*/PA0*/PIORQ
                                   ; SOUND FUNCTION CHIP SELECT
                                   ; PORT F0-F3

IF (VCC) /PGSEL = PA7*PA6*PA5*/PA3*/PIORQ
                + PA7*PA6*PA5*/PA4*PA3*/PA2*/PA1*/PA0*/PIORQ*
                                                    /PWRITE
                + PA7*PA6*PA5*/PA4*PA3*PA2*PA1*PA0*/PIORQ*
                                                    /PWRITE
                + PA7*/PA6*PA5*/PA4*/PA3*/PA2*/PA1*/PIORQ*
                                                    /PWRITE
                                    ; ENABLE FOR PERIPHERAL
                                    ; GROUP INTERFACE
```

PAL 16R6 (U47)

Pin Assignments:

```
CLOCK PD6 PD7 PD0 PD1 PD3 PD2 2DRVIN RST GND
GND MOTOR DDENP SIDESEL DS3 DS2 DS1 DS0 INTERNAL VCC
```

Equations:

```
/DS0 :=/PD0*PD1*PD2*PD3*RST                    ;SELECT DRIVE #0

/DS1 := PD0*/PD1*PD2*PD3*RST                   ;SELECT DRIVE #1

/DS2 :=PD0*PD1*/PD2*PD3*RST                    ;SELECT DRIVE #2

/DS3 :=PD0*PD1*PD2*/PD3*RST                    ;SELECT DRIVE #3

IF (VCC) /MOTOR = /DS0 + /DS1 + /DS2 +/DS3     ;TURN ON DRIVE
                                                MOTOR
IF (VCC) /INTERNAL = 2DRVIN*/DS0 = 2DRVIN*/DS1+
                     2DRVIN*/DS0               ;SELECT EXTERNAL
                                                DRIVE

/SIDESEL := /PD6                               ;DISK SIDE SELECT

/DDENP := /PD7                                 ;DOUBLE DENSITY
                                                RECORDING
```

82S153 (U50)

Discretes:

```
LOWP = Low Page
       False for normal TRSDOS operation
       True for CPM operation
       System Reset sets to False

BANK0 = Primary 64K Memory Selected

BANKSEL = Secondary Memory Selected
          Jumper Selectable from 1 to 7

16K = Secondary memory size
      True - Limited to 16K
      False - Equal to full 64K
```

These signal effect only the memory on the Main Logic Board

RASEN0: Controls Access to Primary 64K

TRSDOS Operation- 0-32K Base, Not Switchable
32-64K Switchable

Address Range 0-32: RASEN0 = RFSH* LOWP* A15*

Address Range 32-64K:

```
RASEN0 =  RFSH* LOWP* A15 BANK0* PAGE VIDEN*  (NO VIDEO)
          RFSH* LOWP* A15 BANK0* PAGE A14*    (VIDEO, <F800)
          RFSH* LOWP* A15 BANK0* PAGE A13*    (VIDEO, <F800)
          RFSH* LOWP* A15 BANK0* PAGE A12*    (VIDEO, <F800)
          RFSH* LOWP* A15 BANK0* PAGE A11*    (VIDEO, <F800)
```

CPM Operation- 0-32K Switchable; 32-64K Base, Not Switchable

Address Range 0-32: RASEN0 = RFSH* LOWP A15* BANK0* PAGE*

Address Range 32-64K:

```
RASEN0 =  RFSH* LOWP* A15 VIDEO*  (NO VIDEO)
          RFSH* LOWP* A15 A14*    (VIDEO, <F800)
          RFSH* LOWP* A15 A13*    (VIDEO, <F800)
          RFSH* LOWP* A15 A12*    (VIDEO, <F800)
          RFSH* LOWP* A15 A11*    (VIDEO, <F800)
```

RASEN1: Controls Access to Additional Memory 64K or 16K

TRSDOS Operation- Address Range = 32-64K

A15 Replaced by Page to Memory (Hardwired)

For Full 64K RAMs:

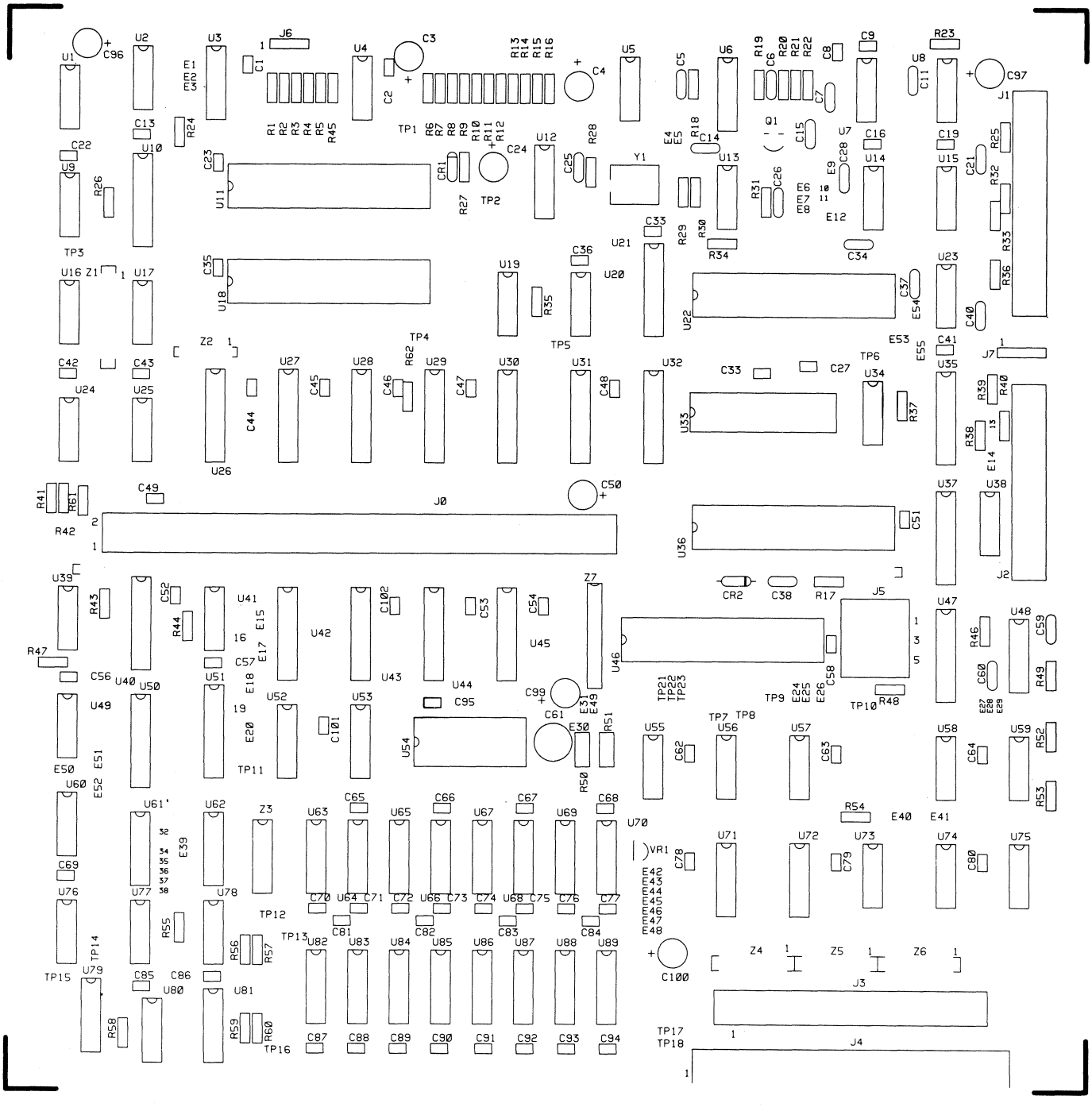
```
RASEN1 =  RFSH* LOWP* A15 BANKSEL VIDEN* 16K*
          RFSH* LOWP* A15 BANKSEL A14* 16K*
          RFSH* LOWP* A15 BANKSEL A13* 16K*
          RFSH* LOWP* A15 BANKSEL A12* 16K*
          RFSH* LOWP* A15 BANKSEL A11* 16K*
```

For 16K RAMs (16K=True) - RASEN1 = RFSH* LOWP* A15 BANKSEL A14*

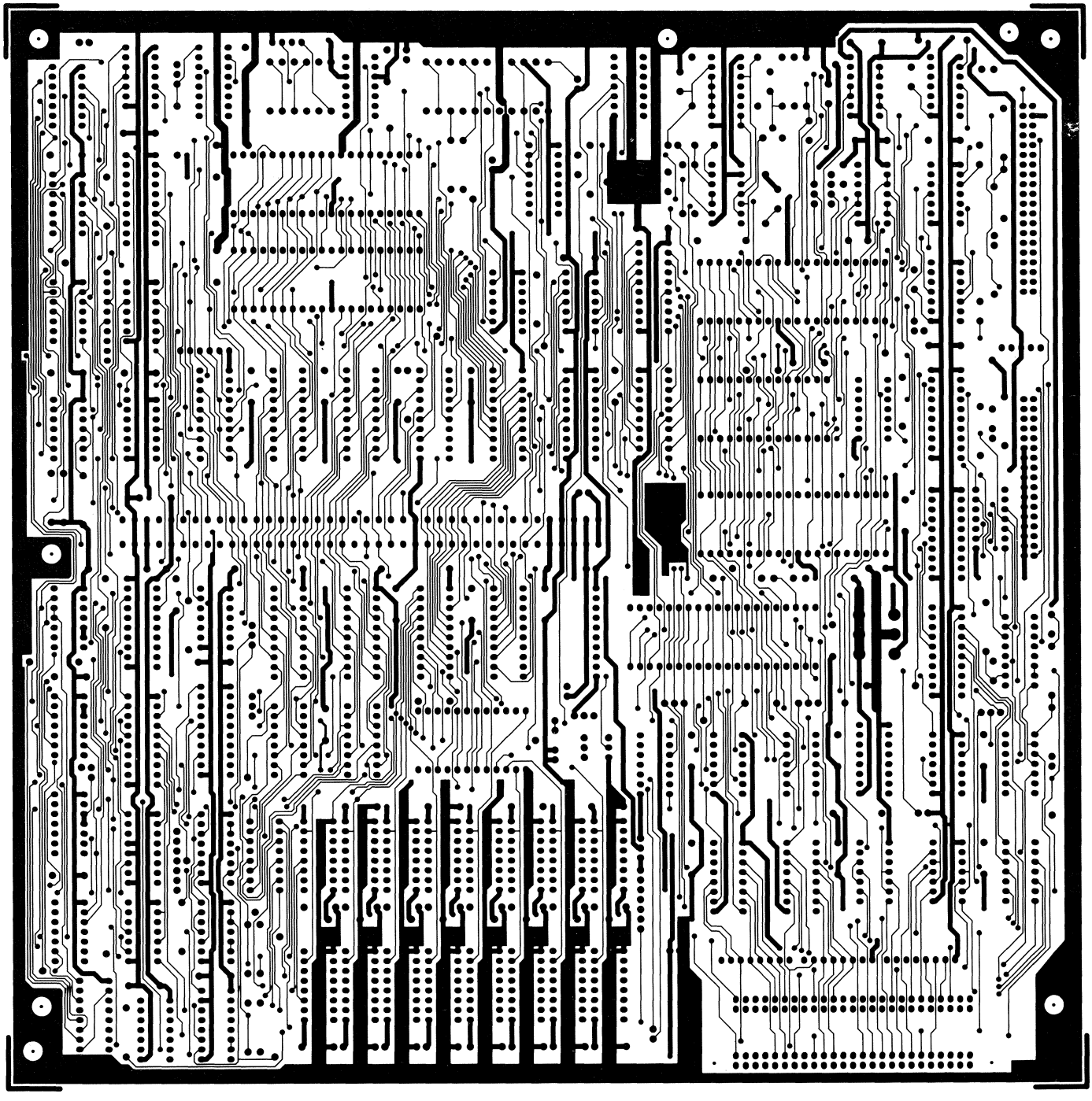
CPM Operation - Address Range 0-32K
A15 to Memory replaced by Page (Hardwired)

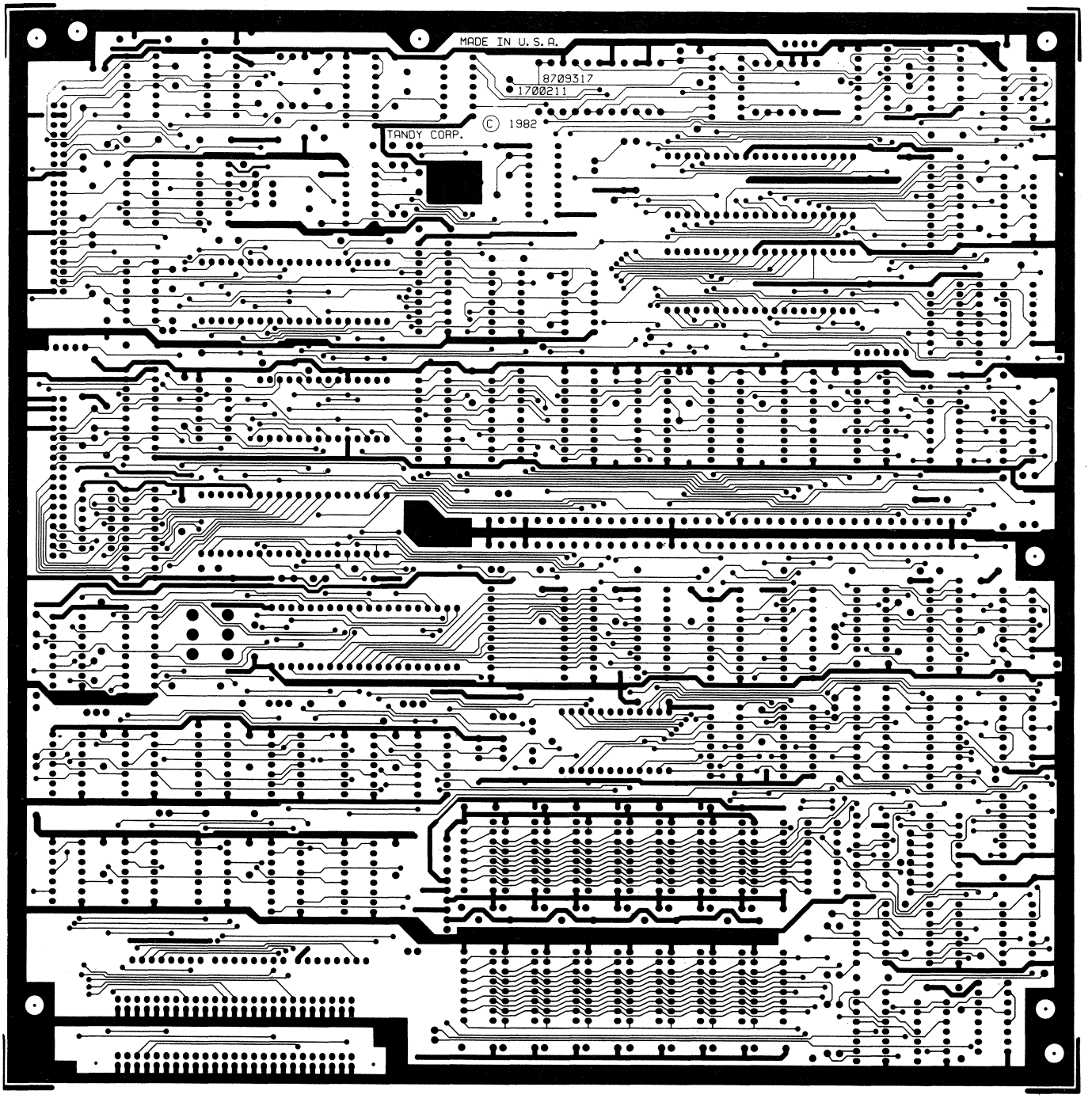
For Full 64K RAMs - RASEN1 = RFSH* LOWP A15* BANKSEL

For 16K RAMs - RASEN1 = RFSH* LOWP A15* BANKSEL A14*



Component Layout, I/O Processor PCB 8898423





Circuit Trace, I/O Processor PCB 8898423, Solder Side

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
C1	Capacitor, 0.1 uF, 50V	8374104
C2	Capacitor, 0.1 uF, 50V	8374104
C3	Capacitor, 1 uF, 16V, Elec Rad	8325101
C4	Capacitor, 10 uF, 16V, Elec Rad	8326101
C5	Capacitor, 100 pF, 50V, C Disk	8301104
C6	Capacitor, 33 pF, 50V, C Disk	8300334
C7	Capacitor (For future design use)	-------
C8	Capacitor, 0.1 uF, 50V	8374104
C9	Capacitor, 0.1 uF, 50V	8374104
C10	Not Used	
C11	Capacitor (For future design use)	-------
C12	Not Used	
C13	Capacitor, 0.1 uF, 50V	8374104
C14	Capacitor, 470 pF, 50V, C Disk	8301474
C15	Capacitor, 100 pF, 50V, C Disk	8301104
C16	Capacitor, 0.1 uF, 50V	8374104
C17	Not Used	
C18	Not Used	
C19	Capacitor, 0.1 uF, 50V	8374104
C20	Not Used	
C21	Capacitor (For future design use)	-------
C22	Capacitor, 0.1 uF, 50V	8374104
C23	Capacitor, 0.1 uF, 50V	8374104
C24	Capacitor, 1 uF, 16V, Elec Rad	8325101
C25	Capacitor, 1000 pF, 50V, C Disk	8302105
C26	Capacitor, 100 pF, 50V, C Disk	8301104
C27	Capacitor, 0.1 uF, 50V	8374104
C28	Capacitor (For future design use)	-------
C29	Not Used	
C30	Not Used	
C31	Not Used	
C32	Not Used	
C33	Capacitor, 0.1 uF, 50V	8374104
C34	Capacitor (For future design use)	-------
C35	Capacitor, 0.1 uF, 50V	8374104
C36	Capacitor, 0.1 uF, 50V	8374104
C37	Capacitor (For future design use)	-------
C38	Capacitor, 0.1 uF, 63V, 10%, Mtl Flm	8394103
C39	Not Used	
C40	Capacitor (For future design use)	-------
C41	Capacitor, 0.1 uF, 50V	8374104
C42	Capacitor, 0.1 uF, 50V	8374104
C43	Capacitor, 0.1 uF, 50V	8374104
C44	Capacitor, 0.1 uF, 50V	8374104
C45	Capacitor, 0.1 uF, 50V	8374104

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
C46	Capacitor, 0.1 uF, 50V	8374104
C47	Capacitor, 0.1 uF, 50V	8374104
C48	Capacitor, 0.1 uF, 50V	8374104
C49	Capacitor, 0.1 uF, 50V	8374104
C50	Capacitor, 10 uF, 16V, Elec Rad	8326101
C51	Capacitor, 0.1 uF, 50V	8374104
C52	Capacitor, 0.1 uF, 50V	8374104
C53	Capacitor, 0.1 uF, 50V	8374104
C54	Capacitor, 0.1 uF, 50V	8374104
C55	Not Used	
C56	Not Used	
C57	Not Used	
C58	Not Used	
C59	Capacitor, 390 pF, NPO, C Disk	8301394
C60	Capacitor, 0.68 uF, 35V, Tant.	8334683
C61	Capacitor, 5-60 pF, NPO, Trim	8360550
C62	Capacitor, 0.1 uF, 50V	8374104
C63	Capacitor, 0.1 uF, 50V	8374104
C64	Capacitor, 0.1 uF, 50V	8374104
C65	Capacitor, 0.1 uF, 50V	8374104
C66	Capacitor, 0.1 uF, 50V	8374104
C67	Capacitor, 0.1 uF, 50V	8374104
C68	Capacitor, 0.1 uF, 50V	8374104
C69	Capacitor, 0.1 uF, 50V	8374104
C70	Capacitor, 0.1 uF, 50V	8374104
C71	Capacitor, 0.1 uF, 50V	8374104
C72	Capacitor, 0.1 uF, 50V	8374104
C73	Capacitor, 0.1 uF, 50V	8374104
C74	Capacitor, 0.1 uF, 50V	8374104
C75	Capacitor, 0.1 uF, 50V	8374104
C76	Capacitor, 0.1 uF, 50V	8374104
C77	Capacitor, 0.1 uF, 50V	8374104
C78	Capacitor, 0.1 uF, 50V	8374104
C79	Capacitor, 0.1 uF, 50V	8374104
C80	Capacitor, 0.1 uF, 50V	8374104
C81	Capacitor, 0.1 uF, 50V	8374104
C82	Capacitor, 0.1 uF, 50V	8374104
C83	Capacitor, 0.1 uF, 50V	8374104
C84	Capacitor, 0.1 uF, 50V	8374104
C85	Capacitor, 0.1 uF, 50V	8374104
C86	Capacitor, 0.1 uF, 50V	8374104
C87	Capacitor, 0.1 uF, 50V	8374104
C88	Capacitor, 0.1 uF, 50V	8374104
C89	Capacitor, 0.1 uF, 50V	8374104
C90	Capacitor, 0.1 uF, 50V	8374104

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
C91	Capacitor, 0.1 uF, 50V	8374104
C92	Capacitor, 0.1 uF, 50V	8374104
C93	Capacitor, 0.1 uF, 50V	8374104
C94	Capacitor, 0.1 uF, 50V	8374104
C95	Capacitor, 0.1 uF, 50V	8374104
C96	Capacitor, 33 uF, 16V, Elec Rad	
C97	Capacitor, 33 uF, 16V, Elec Rad	
C98	Not Used	
C99	Capacitor, 10 uF, 16V, Elec Rad	8326101
C100	Capacitor, 33 uF, 16V, Elec Rad	
C101	Capacitor, 0.1 uF, 50V	8374104
C102	Capacitor, 0.1 uF, 50V	8374104
Connectors		
J0	Connector, 80-Pin, Edge Card	8519014A
J1	Connector, 40-Pin, Vertical Hood	8519159
J2	Connector, 34-Pin, Vertical Hood	8519158
J3	Connector, 50-Pin, Vertical Hood	8519160
J4	Connector, 50-Pin, Rt. Angle	8519164
J5	Connector, 6-Pin, Power	8519015
J6	Connector, 4-Pin, Rt. Anlge	8519053
J7	Connector, 5-Pin, Straight	8519161
Diodes		
CR1	Diode, 1N5222, 2.5V Zener	8150222
CR2	Diode, 1N914	8150148
Integrated Circuits		
---	IC, DDU-7J-300, Delay Line	8429017
---	IC, Z80A, SIO/O	8047884
---	IC, 2716, EPROM	8040716
U1	IC, 74LS74 Dual Flip-Flop	9020074
U2	IC, 74S10 Triple3-In NAND	9010010
U3	IC, 74LS175 Quad Flip-Flop	9020175
U4	IC, LM339 Linear Quad Comparator	9050339
U5	IC, 74LS04 Hex Inverter	9020004
U6	IC, 74LS161 Counter	9020161
U7	IC, MC1488 Quad Line Driver	9050188
U8	IC, MC1489 Quad Line Receiver	9050189
U9	IC, 74LS00 Quad 2-In NAND	9020000
U10	IC, PAL12L6	8040126
U11	CI, Z80A CPU	8047880
U12	IC, 74LS123 Multivibrator	9020123
U13	IC, 7404 Hex Inverter	9000004
U14	IC, MC1488 Quad Line Driver	9050188

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
U15	IC, MC1489 Quad Line Receiver	9050189
U16	IC, 74LS04 Hex Inverter	9020004
U17	IC, 7407 Hex Buffer	9000007
U18	IC, Z80A DMA	8047883
U19	IC, 74LS20 Dual 4-In NAND	9020020
U20	IC, 74LS08 Quad 2-In AND	9020008
U21	IC, PAL16L8	8041168
U23	IC, MC1489 Quad Line Receiver	9050189
U24	IC, 74S08 Quad 2-In AND	9010008
U25	IC, 74LS32 Quad 2-In OR	9020032
U26	IC,74ALS244 Octal Buffer	9025244
U27	IC,74ALS240 Octal Buffer, Inv.	9025240
U28	IC,74ALS240 Octal Buffer, Inv.	9025240
U29	IC,74ALS244 Octal Buffer	9025244
U30	IC, AMD8307 Transceiver	8060307
U31	IC,74ALS244 Octal Buffer	9025244
U32	IC,74ALS240 Octal Buffer, Inv.	9025240
U33	IC, Z80A CTC	8047882
U34	IC, 74LS04 Hex Inverter	9020004
U35	IC,74ALS244 Octal Buffer	9025244
U36	IC, Z80A PIO	8047881
U37	IC,74ALS244 Octal Buffer	9025244
U38	IC, 74LS74 Dual Flip-Flop	9020074
U39	IC, 74S64 ADN-OR	9010064
U40	IC,74ALS240 Octal Buffer, Inv.	9025240
U41	IC, 7407 Hex Buffer	9000007
U42	IC,74ALS240 Octal Buffer, Inv.	9025240
U43	IC,74ALS240 Octal Buffer, Inv.	9025240
U44	IC, AMD8307 Transceiver	8060307
U45	IC, AMD8307 Transceiver	8060307
U46	IC, WD2793 FDC Control	8040793
U47	IC, PAL16R6	8040166
U48	IC, 74LS123 Multivibrator	9020123
U49	IC, 74LS00 Quad 2-In NAND	9020000
U50	IC, 82S153	8040153
U51	IC, 74LS273 Octal Flip-Flop	9020173
U52	IC, 74LS157 Multiplexer	9020157
U53	IC, 74LS157 Multiplexer	9020157
U55	IC, 74LS32 Quad 2-In OR	9020032
U56	IC, 7407 Hex Buffer	9000007
U57	IC, 74LS125 Quad Buffer	9020125
U58	IC, 74LS04 Hex Inverter	9020004
U59	IC, 7407 Hex Buffer	9000007
U60	IC, 74LS30 8-In NAND	9020030
U61	IC, 74LS138 Decoder	9020138

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
U62	IC, 74S112 Flip-Flop	9010112
U63	IC, 16K DRAM	8040016
U64	IC, 16K DRAM	8040016
U65	IC, 16K DRAM	8040016
U66	IC, 16K DRAM	8040016
U67	IC, 16K DRAM	8040016
U68	IC, 16K DRAM	8040016
U69	IC, 16K DRAM	8040016
U70	IC, 16K DRAM	8040016
U71	IC, 74LS158 Multiplexer	9020158
U72	IC, 74LS157 Multiplexer	9020157
U73	IC, 7416 Hex Driver	9000016
U74	IC, 7416 Hex Driver	9000016
U75	IC, 7407 Hex Buffer	9000007
U76	IC, 74LS04 Hex Inverter	9020004
U77	IC, 74S00 Quad 2-In NAND	9010000
U78	IC, 74S08 Quad 2-In AND	9010008
U79	IC, 74LS157 Multiplexer	9020157
U81	IC, 74S112 Flip-Flop	9010112
U82	IC, 64K DRAM	8040655
U83	IC, 64K DRAM	8040655
U84	IC, 64K DRAM	8040655
U85	IC, 64K DRAM	8040655
U86	IC, 64K DRAM	8040655
U87	IC, 64K DRAM	8040655
U88	IC, 64K DRAM	8040655
U89	IC, 64K DRAM	8040655
Resistors		
R1	Resistor, 10k ohms, 1/4W, 5%	8207310
R2	Resistor, 15k ohms, 1/4W, 5%	8207315
R3	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R4	Resistor, 56k ohms, 1/4W, 5%	8207356
R5	Resistor, 22k ohms, 1/4W, 5%	8207322
R6	Resistor, 51k ohms, 1/4W, 5%	8207351
R7	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R8	Resistor, 150 ohms, 1/4W, 5%	8207115
R9	Resistor, 10k ohms, 1/4W, 5%	8207310
R10	Resistor, 2k ohms, 1/4W, 5%	8207220
R11	Resistor, 10k ohms, 1/4W, 5%	8207310
R12	Resistor, 15k ohms, 1/4W, 5%	8207315
R13	Resistor, 56k ohms, 1/4W, 5%	8207356
R14	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R15	Resistor, 22k ohms, 1/4W, 5%	8207322
R16	Resistor, 1k ohms, 1/4W, 5%	8207210

Parts Lists, I/O Processor PCB, 8898423(11/17/82)

Ref.No.	Description	Part No.
R17	Resistor, 1k ohms, 1/4W, 5%	8207210
R18	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R19	Resistor, 1.2k ohms, 1/4W, 5%	8207212
R20	Resistor, 220 ohms, 1/4W, 5%	8207122
R21	Resistor, 10k ohms, 1/4W, 5%	8207310
R22	Resistor, 560 ohms, 1/4W, 5%	8207156
R23	Resistor, 10k ohms, 1/4W, 5%	8207310
R24	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R25	Resistor, 10k ohms, 1/4W, 5%	8207310
R26	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R27	Resistor, 7.5k ohms, 1/4W, 5%	8207275
R28	Resistor, 160k ohms, 1/4W, 5%	8207416
R29	Resistor, 680 ohms, 1/4W, 5%	8207168
R30	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R31	Resistor, 560 ohms, 1/4W, 5%	8207156
R32	Resistor, 10k ohms, 1/4W, 5%	8207310
R33	Resistor, 10k ohms, 1/4W, 5%	8207310
R34	Resistor, 22 ohms, 1/4W, 5%	8207022
R35	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R36	Resistor, 10k ohms, 1/4W, 5%	8207310
R37	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R38	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R39	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R40	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R41	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R42	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R43	Resistor, 2.2k ohms, 1/4W, 5%	8207222
R44	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R46	Resistor, 390k ohms, 1/4W, 5%	8207349
R48	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R49	Resistor, 10k ohms, 1/4W, 5%	8207310
R50	Trim Pot, 50k ohms, 3-Pin	8289351
R51	Trim Pot, 50k ohms, 3-Pin	8289351
R52	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R53	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R54	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R55	Resistor, 51 ohms, 1/4W, 5%	8207051
R56	Resistor, 51 ohms, 1/4W, 5%	8207051
R57	Resistor, 51 ohms, 1/4W, 5%	8207051
R58	Resistor, 51 ohms, 1/4W, 5%	8207051
R59	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R60	Resistor, 51 ohms, 1/4W, 5%	8207051
R61	Resistor, 4.7k ohms, 1/4W, 5%	8207247
R62	Resistor, 4.7k ohms, 1/4W, 5%	8207247

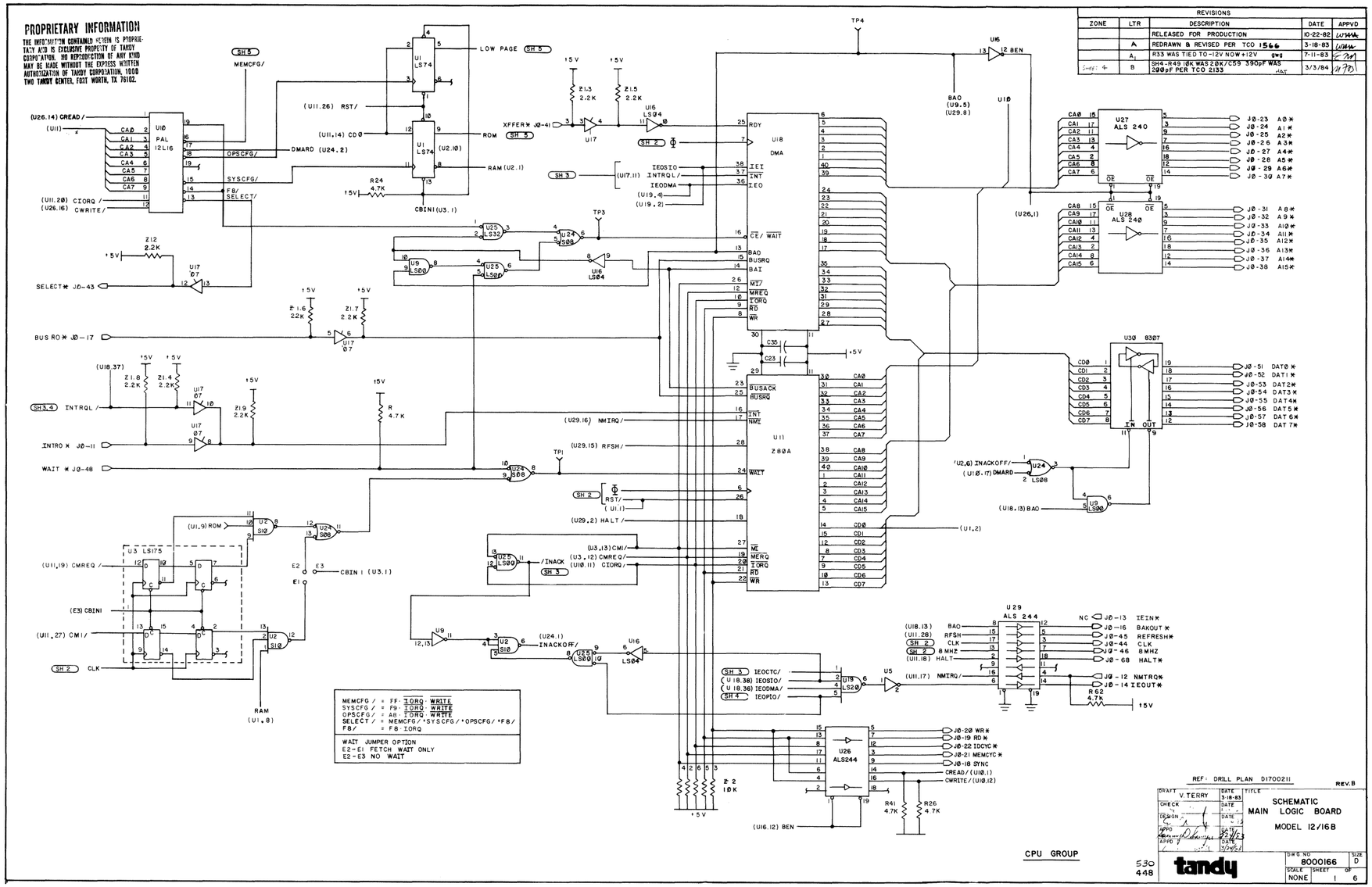
Parts Lists, I/O Processor PCB, 8898423(11/17/82)

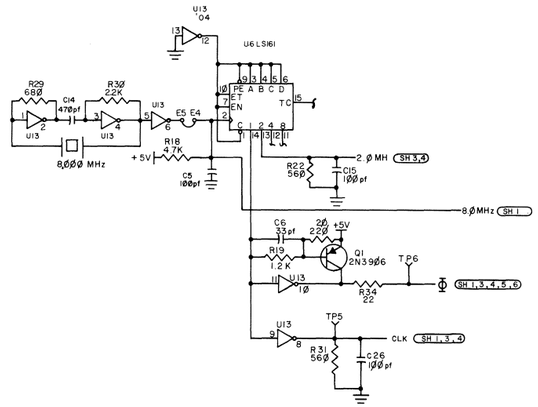
Ref.No.	Description	Part No.
Resistor Paks		
Z1	Resistor Pak, 2.2k ohms, SIP 10-Pin	8290031
Z2	Resistor Pak, 10k ohms, SIP 6-Pin	8290032
Z3	Resistor Pak, 56k ohms, DIP	8290034
Z4	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z5	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z6	Resistor Pak, 150 ohms, SIP 8-Pin	8293316
Z7	Resistor Pak,220/330 ohms, SIP 10-Pin	8290020
Staking Pins		
TP6	Staking Pin	8529014
TP8	Staking Pin	8529014
TP8	Staking Pin	8529014
TP9	Staking Pin	8529014
TP10	Staking Pin	8529014
TP21	Staking Pin	8529014
TP22	Staking Pin	8529014
TP23	Staking Pin	8529014
E1	Staking Pin	8529014
E2	Staking Pin	8529014
E4	Staking Pin	8529014
E5	Staking Pin	8529014
E6	Staking Pin	8529014
E7	Staking Pin	8529014
E8	Staking Pin	8529014
E9	Staking Pin	8529014
E10	Staking Pin	8529014
E11	Staking Pin	8529014
E12	Staking Pin	8529014
E15	Staking Pin	8529014
E16	Staking Pin	8529014
E17	Staking Pin	8529014
E18	Staking Pin	8529014
E19	Staking Pin	8529014
E24	Staking Pin	8529014
E25	Staking Pin	8529014
E27	Staking Pin	8529014
E28	Staking Pin	8529014
E30	Staking Pin	8529014
E31	Staking Pin	8529014
E32	Staking Pin	8529014
E38	Staking Pin	8529014
E39	Staking Pin	8529014
E40	Staking Pin	8529014

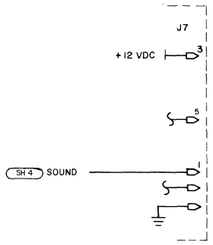
Parts Lists, I/O Processor PCB, 8898423(11/17/82)

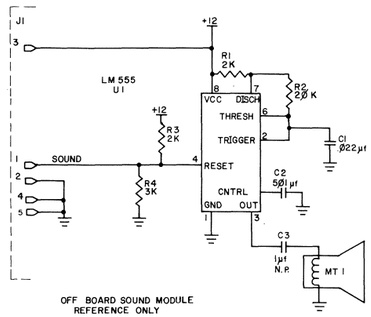
Ref.No.	Description	Part No.
Staking Pins		
E41	Staking Pin	8529014
E42	Staking Pin	8529014
E43	Staking Pin	8529014
E44	Staking Pin	8529014
E45	Staking Pin	8529014
E46	Staking Pin	8529014
E47	Staking Pin	8529014
E48	Staking Pin	8529014
E49	Staking Pin	8529014
E50	Staking Pin	8529014
E51	Staking Pin	8529014
E52	Staking Pin	8529014
E53	Staking Pin	8529014
E54	Staking Pin	8529014
E55	Staking Pin	8529014
Transistors		
Q1	Transistor, 2N3906	8100906
Miscellaneous		
Y1	Crystal, 8.0000MHz	8409006
VR1	Voltage Regulator, 79L05	8051905

Quanity	Description	Part No.
1	Bus Bar, 8.5"	8439008
1	Printed Circuit Board	8709317
16	Socket, 16-Pin	8509003
18	Socket, 20-Pin	8509009
1	Socket, 24-Pin	8509001
1	Socket, 28-Pin	8509007
5	Socket, 40-Pin	8509002

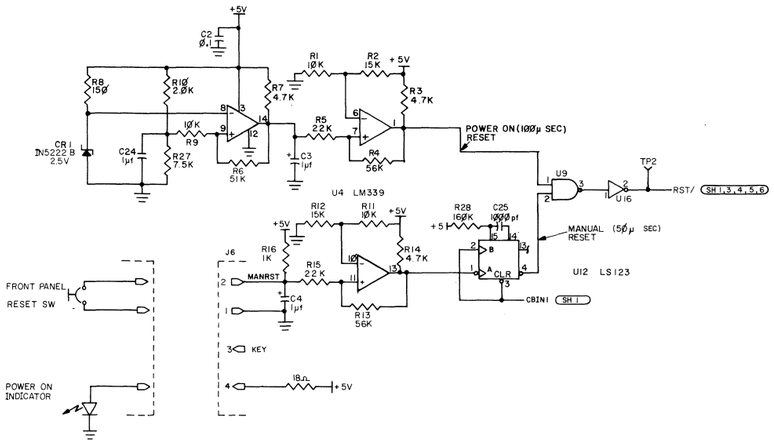

PROPRIETARY INFORMATION
THE INFORMATION CONTAINED HEREIN IS PROPRIETARY AND IS EXCLUSIVE PROPERTY OF TANDY CORPORATION. NO REPRODUCTION OF ANY KIND MAY BE MADE WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF TANDY CORPORATION, 1000 TWO TANDY CENTER, FORT WORTH, TX 76102.
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPVD
RELEASED FOR PRODUCTION 10-22-82
A REDRAWN & REVISED PER TCO 1566 3-18-83
A1 R33 WAS TIED TO -12V NOW +12V 7-11-83
Sheet 4 B SH4-R49 10K WAS 20K/C59 390pF WAS 200pF PER TCO 2133 3/3/84
MEMCFG/
SYSCFG/
OPSCFG/
SELECT/
F8/
SELECT
MEMCFG / = FF·IORQ·WRITE
SYSCFG / = F9·IORQ·WRITE
OPSCFG / = AB·IORQ·WRITE
SELECT / = MEMCFG/*SYSCFG/*OPSCFG/*F8/
F8/ = F8·IORQ
WAIT JUMPER OPTION
E2-E1 FETCH WAIT ONLY
E2-E3 NO WAIT
CPU GROUP
REF: DRILL PLAN D170021
REV.B
DRAFT V.TERRY 3-18-83
CHECK
DESIGN
APPD
SCHEMATIC
MAIN LOGIC BOARD
MODEL 12/16B
tandy
DWG NO 8000166
SIZE D
SCALE NONE
SHEET 1 OF 6
530
448

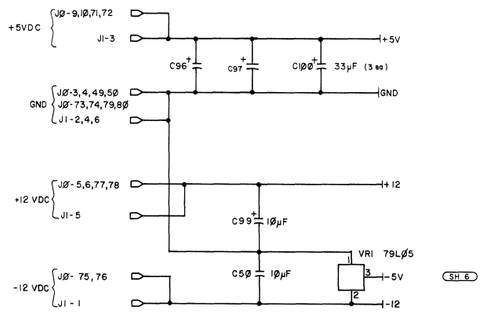




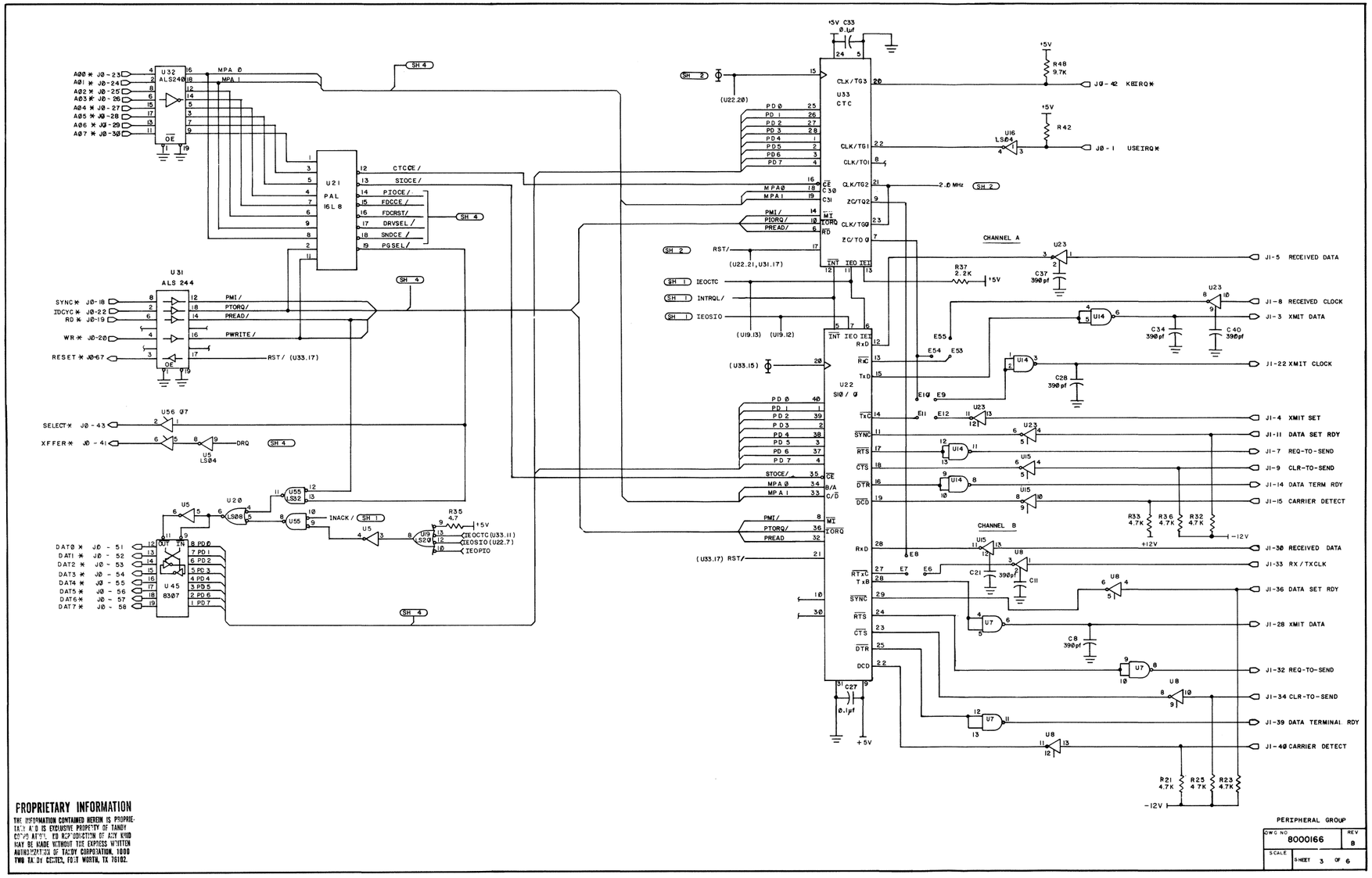


OFF BOARD SOUND MODULE
REFERENCE ONLY





DWG NO	REV
8000166	B
SCALE: NONE	SHEET: 2 OF 6

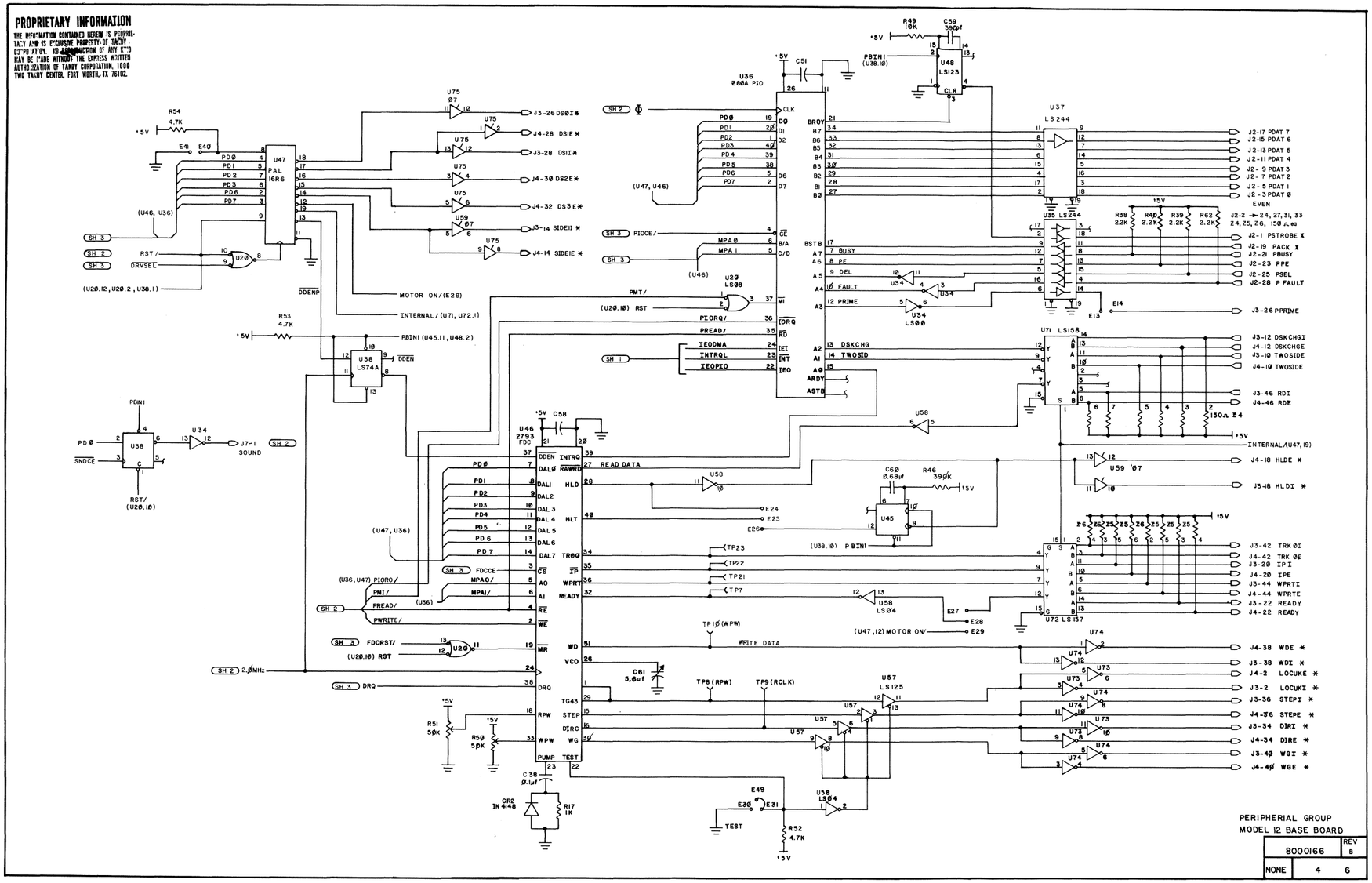


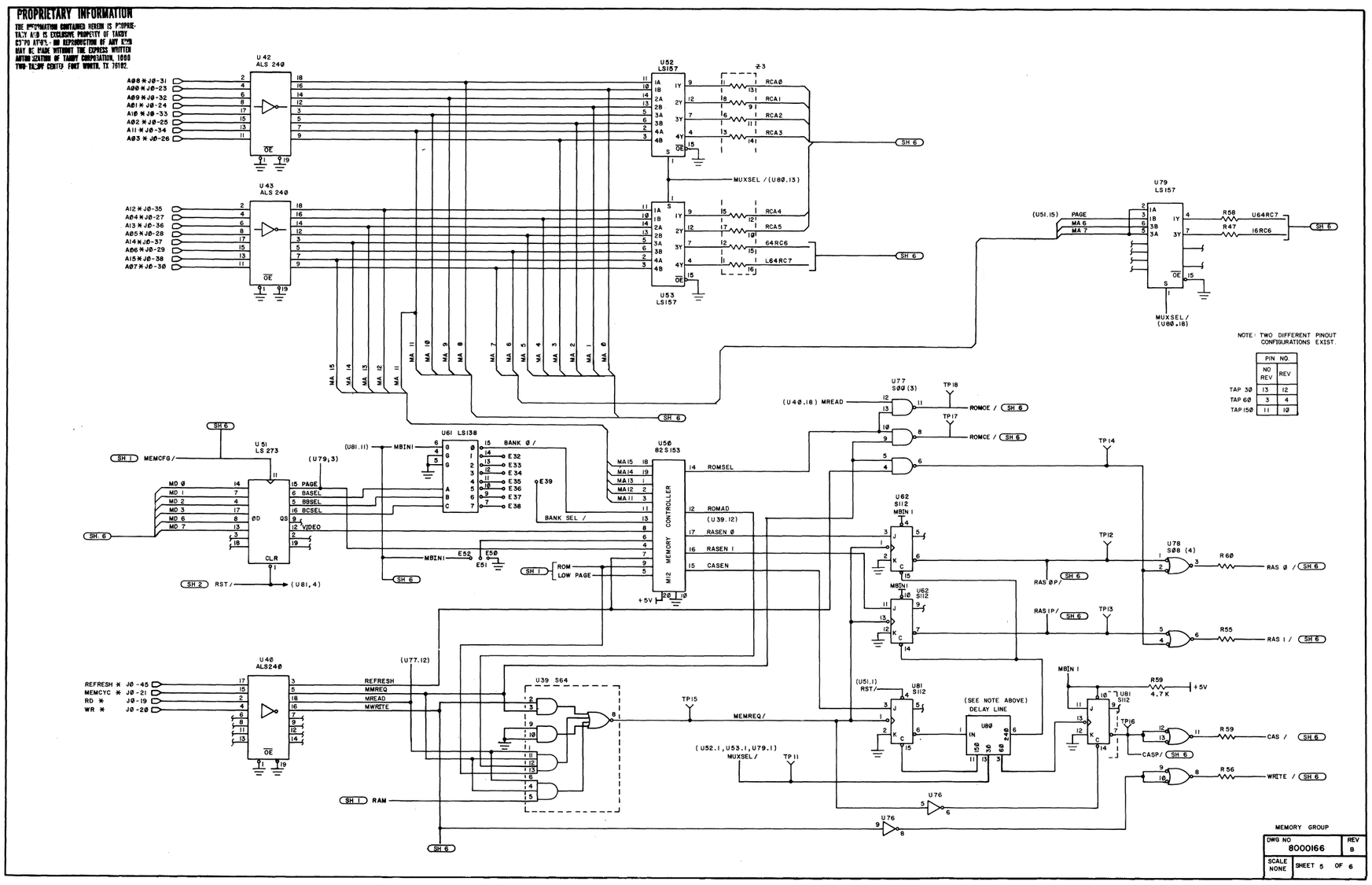
PROPRIETARY INFORMATION

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY AND IS EXCLUSIVE PROPERTY OF TANDY CORP'S ANY'S. TO REPRODUCTION OF ANY KIND MAY BE MADE WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF TANDY CORPORATION, 1000 TWO TANDY CENTER, FORT WORTH, TX 76102.

PERIPHERAL GROUP

DWG NO	REV
8000166	B
SCALE	SHEET 3 OF 6





NOTE: TWO DIFFERENT PINOUT CONFIGURATIONS EXIST:

	PIN NO.	
	NO REV	REV
TAP 30	13	12
TAP 60	3	4
TAP 150	11	10

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

1. C65-C68, -5V BYPASS IF U63-U70 P/N 4116
2. C81-C84, +5V BYPASS IF U63-U70 P/N 4116
3. C70-C77, +12V BYPASS IF U63-U70 P/N 4116
   +5V BYPASS IF U63-U70 P/N 6665,4516
4. C87-C74, +5V BYPASS

BANKSEL PAGE Ø.1

OPTION	1	MCM 6665-15 E16-E17,E45,E46,E47-E48 VR1 NOT INSTALLED
OPTION	2	MCM 4516 E15-E16, E46-E45 VR1 NOT INSTALLED
OPTION	3	MCM 4116 E42-E43,E44-E45,E46-E47 VR1 INSTALLED

BANK Ø PAGE Ø.1
MCM66655-15 64K x 1 SRAM'S

REMAINING 7

U54 2716,2734 BOOTROM

U44 8307

U76

U49 LS08 (4)

U41 '07 (3)

REV B

DWG NO	SIZE
8000166	
SCALE NONE	SHEET 6 OF 6

7.5 Video/Keyboard Interface Board

The Video/Keyboard Interface board has two major functions. One is to control a built-in, high-resolution video monitor capable of displaying 24 lines of either 80 normal characters or 40 expanded characters in both upper and lower cases. The other is to control a keyboard that includes the normal set of key functions plus eight software-programmable function keys.

Figure 7-10 shows a block diagram of this PCB assembly. It includes a high speed oscillator (U1) whose frequency (12.48Hz) is the rate at which information is shifted to the CRT and video dots are written, and a CRT controller providing diversified functions such as video timing and display refresh memory addressing. A multiplexer switches the control of the Display RAM address source to either the CRTC or the CPU, depending on the RAM/Video RAM Logic Selection. The block diagram also shows a video-board select logic which controls a 3-state buffer, the keyboard control, and enables the video and Real Time Clock. Data is latched from the Display RAM into a ROM character generator, then shifted to the video output to finally appear on the display monitor.

Figure 7-10 includes as many blocks as possible for clarity. For example, the pulse-width adjuster block in the block diagram is simply an MSI monostable multivibrator with Schmitt-trigger inputs. Its main function is to provide noise immunity and pulse width stability to the horizontal sync signal, which is one of the CRTC ouputs. Also, the vertical sync goes through the RTC & NMIRQ* Logic to generate a Real Time Clock signal (30 or 60 Hz) and a non-maskable interrupt request signal.

All the different blocks describing the control system (Video/Keyboard) are described in the following sections.

7.5.1. Theory of Operation

1. High Speed Timing (refer to Video/Keyboard schematic)

The timing for the system is derived from a crystal oscillator. This oscillator is shown in the upper LH corner of the schematic. It consists of a 12.48 MHz fundamental-cut crystal in a parallel resonant circuit that is composed of two inverters (part of U1) that are biased into their linear region by resistors R2 and R3 (470 ohms each).

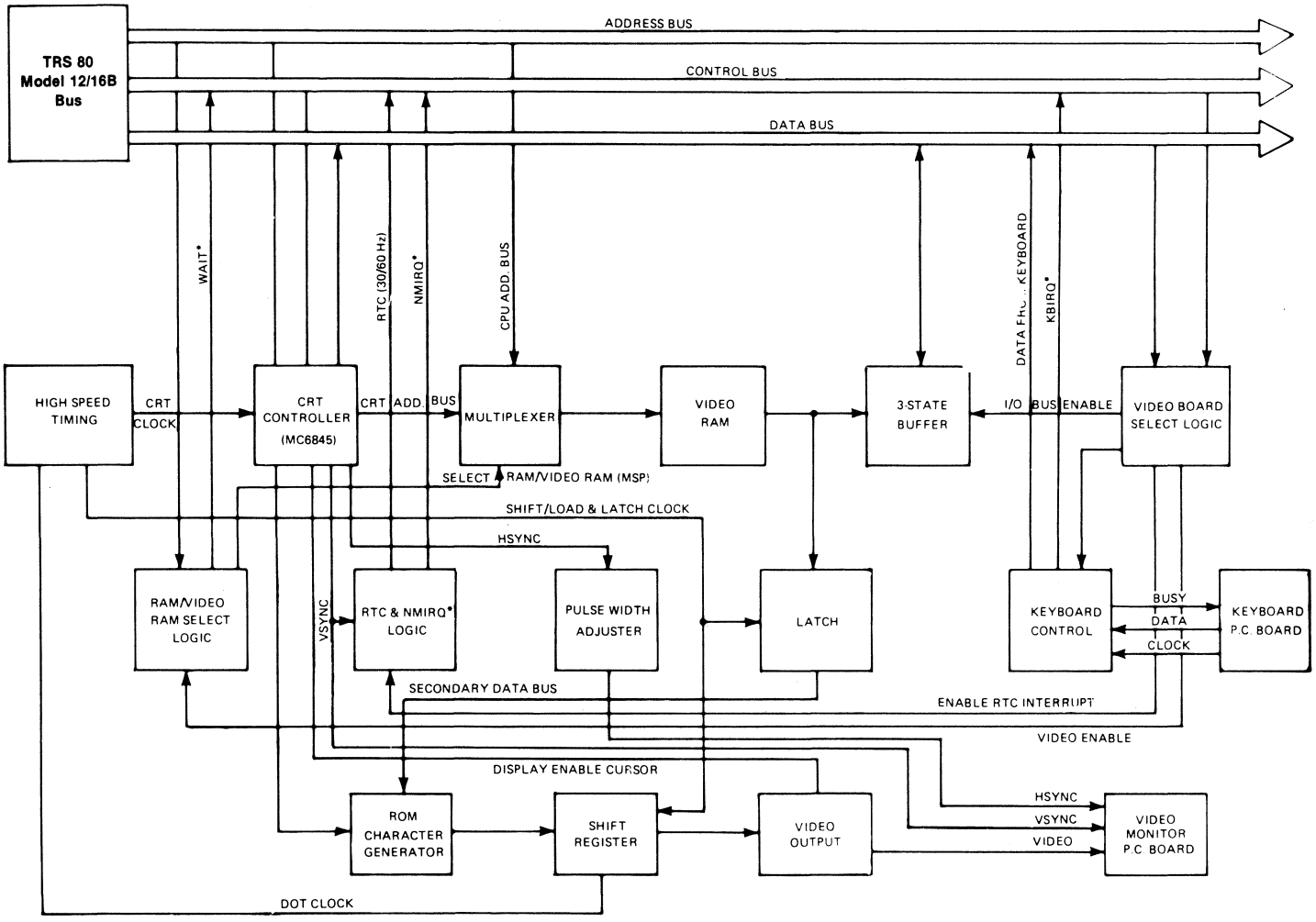


Figure 7-10. Video/Keyboard Interface PCB Block Diagram

The waveform at pin 8 of U1 resembles a "raw" square wave with a frequency of approximately 12.48 MHz.

At pin 2 of the same chip, the signal appears more like a "clean" square wave. It is labeled RCLOCK and is fed through inverter U1 pin 13 and exits pin 12 as RCLOCK*. The asterisk indicates that the signal is an active low, i.e. if RCLOCK is normally an active high, RCLOCK* will be an active low.

At pin 3 of U1, RCLOCK* goes through an inverter to give RCLOCKP (RCLOCK prime) and through a second inverter to yield RCLOCKP*. Up to this point, all clock pulses have the same frequency (12.48 MHz) but different phases.

All these different clock pulses are generated to provide the timing to synchronize the various activities of the video system. Some activities should take place before others while some should occur three or four times as often as others. RCLOCK is divided by 2 by a D Flip-Flop, pins 3 and 5 of U17. This provides a frequency of 6.24 MHz, which is then NANDed with the 80*/40 character Enable. When this signal is low (active), 80 characters per line will be displayed on the screen. When the signal is high, only 40 characters will appear on the screen.

CLOCK (at pin 6 of U28, test point TP26) is either 12.48 MHz (for 80 characters) or 6.24 MHz (for 40 characters). Note that the NAND gate (U28 pins 1, 2, and 3) is used here as an inverter. CLOCK goes through inverter U33 (pins 1 and 2) to become DCLK, which is the DOT CLOCK. Its frequency (either 6.24 or 12.48 MHz) is the rate at which video information is shifted to the CRT.

CLOCK, which is a phase-shifted DOT CLOCK, is divided by the 4-bit counter (U26) to produce the character-rate clock labeled as CCLK with a frequency of 1.56 MHz (for 80 characters) or 0.78 MHz (for 40 characters). This 4-bit counter (LS163) is synchronous (all its flip-flops are clocked simultaneously) so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. The DOT CLOCK triggers the four flip-flops on the rising edge of its wave form. The count is accomplished as follows (in HEX): 0, 9, A, B, C, D, E, F, 0, 9, A, B, C,...etc. This is best described by the timing diagram in Figure 7-11. Notice that both 40 and 80 character modes are represented here and that the signals TCLK* and PLCLK* are also shown on this diagram.

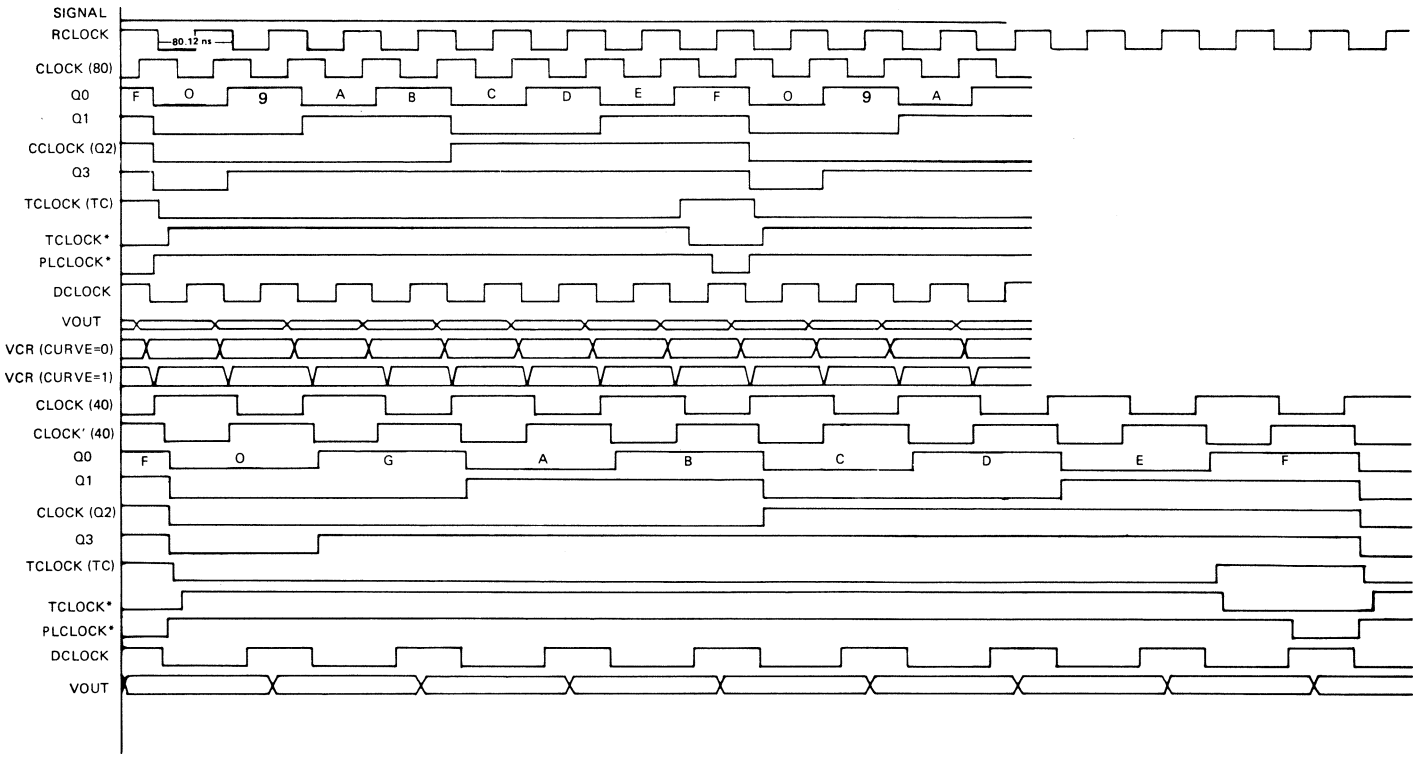


Figure 7-11. Timing Diagram

All these different signals are needed to allow the proper synchronization of the functions. The diagram represents accurately the propagation delay times provided by the different gates.

An example of this follows: the CCLK triggers the MC6845 CRT controller that, if enabled, sends an address to the video RAM requesting data to be sent to the Latch (U8) inputs. TCLK* then latches it into the character ROM that, at its turn, would send the appropriate dots to the shift register U10. PLCLK* then shift loads them in parallel into the 8-bit shift register (U10) and DCLK shifts them out serially toward the Video.

2. Cathode Ray Tube Controller (CRTC)

The video monitor display uses the Motorola Controller MC6845, a reliable processor that controls the monitor with no CPU intervention until the video memory receives new data to be processed.

The MC6845 simplifies not only the design and the architecture, but also the troubleshooting of the video control board. It sharply reduces the number of IC chips normally required. This CRTC commands the interface to raster scan the CRT display. It also provides video timing and refresh memory addressing. The CRTC is a collection of registers, counters and comparators that time all logic activities as the interfaced raster scan proceeds. Its logic consists of programmable horizontal and vertical timing generators, linear register, cursor logic, light-pen capture register and control circuitry for interfacing to a processor bus. The CRTC permits easy timing and synchronization of signals. It also handles raster graphics as well as alphanumeric applications. It is fully programmable through the CPU data bus, thus generating timing for almost any alphanumeric screen density. Therefore, it is up to the designer to choose any screen density desired, for instance 80 x 24, 132 x 20, etc.

In the Tandy 6000/6000HD either an 80 x 24 or a 40 x 24 character screen density is used. This can be set by programming the registers of the CRTC. The CPU communicates with the CRT controller through a buffered 8-bit data bus by reading or writing into the 18 registers of the CRTC.

Other functions of the CRT controller are to generate refresh addresses, row addresses, video monitor timing (horizontal and vertical sync), cursor and display enable.

The best way to describe the MC6845 controller is to refer to the pin descriptions as noted in Figure 7-12. The following paragraphs describe the function of each pin on the CRTC chip. The MC6845 is identified as U11 on the schematic.

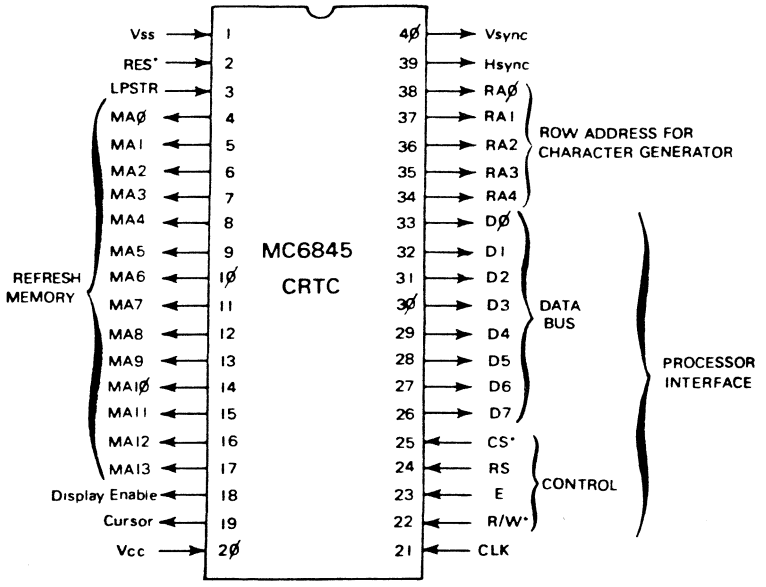


Figure 7-12. MC6845 Pin Identification

Processor Interface

The CRTC interfaces to the processor bus on the bidirectional data bus (D0-D7) using CS*, RS, E and R/W* for control signals. The data bus lines are used for data transfers between the CRTC internal register file and the processor.

The enable signal (pin 23) of U11 is a high impedance TTL/MOS compatible input that enables the data bus input/output buffers and clocks data to and from the CRTC. In the schematic, the CRTC is enabled by either the RD* or WR* (U42, pins 11, 12, and 13). The high-to-low transition is its active edge.

The chip select (CS*), when low, selects the CRTC to read or write the internal register file. It is active (low) only when there is a valid stable address being decoded from the

processor. It is active when either I/O port FC* or FD* is active (U31, pins 6 and 7). The register select line (RS) is an input that selects either the address register (RS=0) or one of the data registers (RS=1) of the internal register file. The read/write signal (R/W*) determines whether the internal file gets written (signal low) or read (signal high).

CRT Control

The CRTC provides horizontal sync (HS), vertical sync (VS), and Display Enable signals. The vertical sync is an active high signal that drives the monitor. It determines the vertical position of the displayed data. The horizontal sync is also an active high signal that drives the monitor to determine the horizontal position of the displayed data.

The Display Enable is an active high signal that indicates the CRTC is providing addressing in the display area.

Refresh Memory/Character Generator Addressing

The CRTC provides memory addresses (MA0-MA13), which scan the refresh RAM. Only MA0 through MA10 are used, since the video memory capacity is only 2K bytes. Also provided are Raster addresses (RA0-RA4) for the character ROM. The refresh memory addresses (MA0-MA10) are used to refresh the CRT screen with pages of data located in the 2K block of Display RAM.

The raster addresses (RA0-RA4) determine the row of a character in the character ROM.

Other Pins

The clock input is used to synchronize all CRT control signals. This signal is the character-rate clock CCLK (1.56/0.78 MHz). The active transition is high to low.

The Light Pen Strobe (LPSTR) is not used in the Model 6000/6000HD. The cursor, which is an active high signal, indicates cursor display to external video processing logic.

The Reset (RES*) input is used to reset the CRTC. It is an active low. When this signal is active, the CRTC is forced into the following status:

All the counters in CRTC are cleared and the device stops the display operation.

All the outputs go to a low level.

The control registers of the CRTC are not affected.

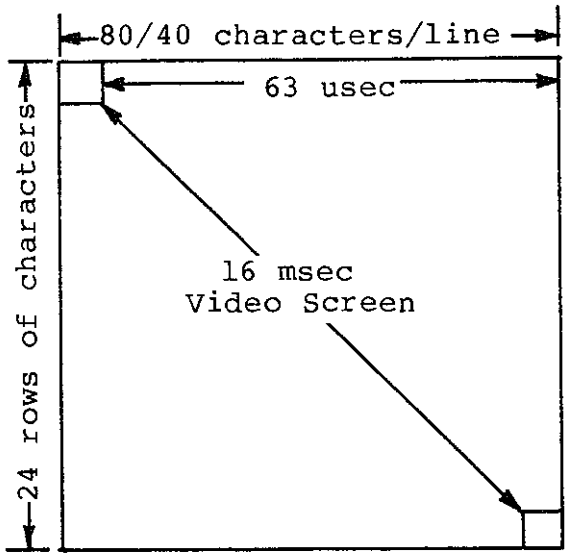
Display Refresh

The CRTC internal register file is programmed to display either a 80 x 24 or 40 x 24 alphanumeric character format. The address of each of these characters is stored in the display memory. That is why only 2K of Video RAM is required (just enough to store the entire screen density). Everything that is displayed on the screen must be refreshed continuously or it will fade and disappear. Each character is a dot matrix of 8 x 10 cells and every cell is refreshed approximately 60 times a second. The CRT beam scans the screen from top to bottom, refreshing every dot whose location is indicated by the coordinates that the display memory and the character ROM receive from the CRTC (memory refresh address and Row address).

The CRTC takes care of this particular chore while the CPU takes care of other more important tasks. However, every time the CPU addresses its upper 2K bytes of memory, it automatically takes control of the Video RAM. The reason is that these 2K bytes, locations F800H through FFFFH, overlap the video memory in its entirety. Thus the display RAM can be accessed by either the CPU or the CRTC, but not by both at the same time.

The processor (CPU) gets priority access anytime, but is synchronized by an interrupt to perform accesses only during the vertical retrace time. The vertical retrace time is defined as the time it takes the CRT beam to return from the end of the very last scan line back to the start of the very first one. The CRT beam is shut off during the retrace time.

The CRTC sends its addresses as follows: The first set of address lines, consisting of MA0 through MA10, cycles binarily through the display memory and is incremented with each clock pulse (CCLK), one per character displayed. The second set (RA0-RA4) addresses the row-address select lines



Video Screen density: 80/40 x 24 characters.

Only $(1920)_{10}$ locations are displayed of the 2K RAM contents

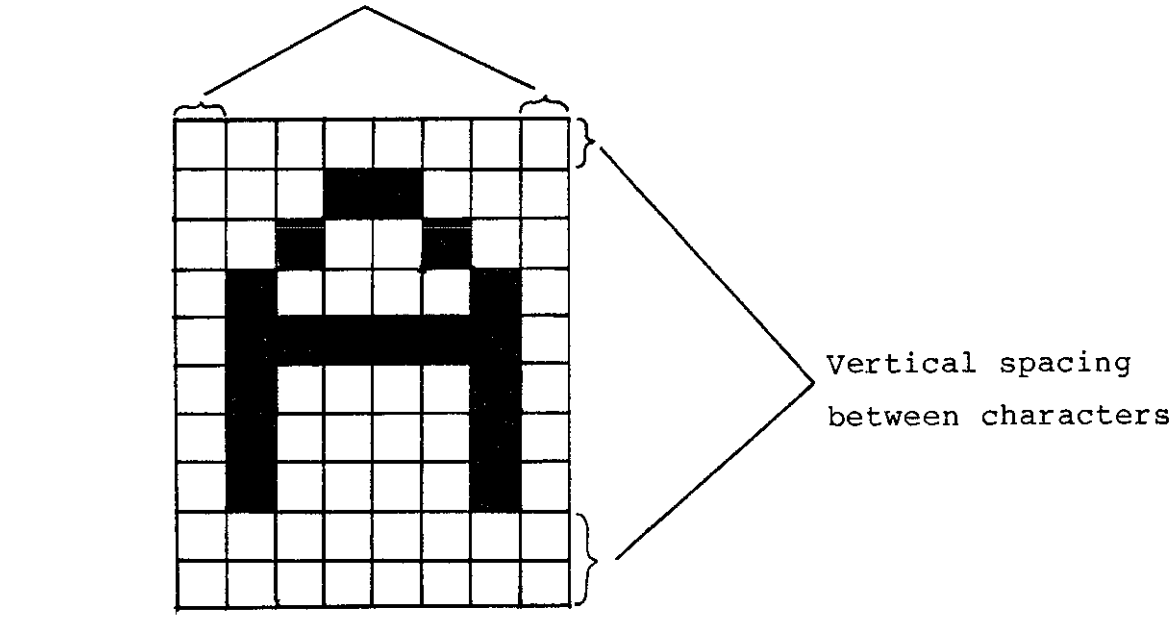


Figure 7-13. Character Dot Pattern

of the character generator. These also cycle binarily, but are incremented with each horizontal retrace time. The horizontal retrace time is the period in which the CRT beam returns from the end of a scan line back to the beginning of the next one.

The CTRC's linear address generator repeats the same sequence of character addresses for each scan line within the same character row.

The character block in our case is 10 rows high, so it takes 10 separate accesses of a given character to write its 10 dot-rows on the screen. Putting 80 x 24, or 1920, characters on the screen requires 10 x 1920, or 19200, character accesses 60 times every second.

Multiplexers

As you can see in the schematics, LS157 multiplexers (U23, 24, and 25) are used for multiplexing refresh memory addresses between the processor and the CRTC.

The processor is in control when the select inputs (pin 1 of each chip) are high. When these inputs are low, the control of the display is switched to the CRTC. MSP, the signal that controls multiplexing, is derived from the RAM/VIDEO RAM Select Logic block.

RAM/VIDEO RAM Select Logic

The block labeled RAM/VIDEO RAM Select Logic on the diagram in Figure 7-13 is a decoder. That is, when the CPU is addressing its upper 2K bytes of memory located at F800H through FFFFH, address lines AD11 through AD15 become high (active). Also, the Memory request signal or memory cycle (MEMCYC) is activated by the CPU. This signal is activated every time the CPU addresses any part of its memory. Another important signal is the input to pin 4 of NAND gate LS30, U41. This signal is used to enable the CPU to access the Video RAM only if the software says to. That time is when Port FFWR* is activated and bit 7 (D2 of U18) is set to 1. If all these conditions are met, then pin 8 of U41 goes low and MSEL (U30 pin 6) becomes high.

MSEL is ANDed with MSLP (U13 pins 1, 2, & 3) to finally give MSP, the select input to the multiplexers. When this MSP signal is high, the Video RAM is under the processor control. Note that when the RESET* button is pressed (U32 pin 8), the CPU loses that control (MSP becomes low).

Since the CRTC clock CCLK and the processor (Z80) clock are asynchronous, there must be some way to resolve conflict between the CRTC and the CPU for Display RAM access. This is done by MSEL* creating a WAIT* request to the CPU.

This is one of two configurations as set by jumpers E1-E2-E3 and E4-E5-E6.

E1-E2, E5-E6

This configuration allows the CPU access whenever requested (CCLK is low). MSEL* sets WAIT*. MSEL is not created until CCLK goes low, which holds off MSP. When MSP goes true, false MSP ANDed with Q1 clears WAIT*. When the CPU access is over, the control is returned to the CRTC on the next CCLK high period.

E2-E3, E4-E5

This configuration allows the CPU access only during vertical and horizontal retrace periods as defined by the CRTC signal DISPEN. Thus, if the CPU makes an access request, WAIT* is created as before by MSEL but MSELP is not allowed to become true until DISPEN is true.

Video Board Select Logic

This part of the system is called the port addressing block. It uses the lower eight lines of the address bus as shown by U27 (LS30) for the dual 2 to 4 line decoder (U31 LS155). One of the decoders is enabled only by Read NANDed with I/O Cycle signal (IOCYC) to give 3 Read ports (FCRD*, FERD*, and FFRD* pins 9, 11, and 12). The other is enabled only by the IOCYC signal and its outputs could actually be used for Read or Write ports. In our design, either one of the FC* or FD* ports could chip select the MC6845 controller. Port FF* NANDed with WR* gives FFWR* (U3 pins 11, 12, and 13). Also, the Input/Output address select (U27 pin 8 and U33 pins 5 and 6) is ANDed with IOCYC to give the I/O Select (IOSEL) to enable the 3-state buffers (U34 and U35) to either Read from the CRTC (IOBIE:I/O Bus Input Enable) or Write into it (IOBIE*:I/O Bus Output Enable). Note that test points TP22 (U13 pin 6) and TP21 (U2 pin 11) will show us if we are reading from or writing into the CRTC. The following table shows the port addressing and the function of every port.

PORT ADDR.	READ FUNCTION	WRITE FUNCTION
FC	Read Keyboard data Clear Keyboard Interrupt	Load CRTC address Register
FD	Read CRTC Data Register	Load CRTC data Register
FE	Clear Real Time clock (RTC) interrupt.	
FF	Read Non-maskable Interrupt Register and Non-maskable Interrupt Mask Register.	Load Memory Bank Select Register and load Non-maskable Interrupt Mask Register and Video enable.

Table 7-8. Port Addressing

For example, Port FF is used as follows:

Non-maskable Interrupt Mask Register and Bank Select Register: Write only.

D7 D6 D5 D4 D3 D2 D1 D0

Bit 7 (D7)

- if set (1), enables the 2K bytes RAM, disables the upper 2K bytes of the Bank's RAM (F800H to FFFFH)

- if reset (0), disables Video RAM, enables Bank RAM F800H to FFFFH.

Bit 6 (D6)

- if 0, enables Video display (on)
- if 1, Video display off

Bit 5 (D5)

- Set (1), enables the Real Time Clock (RTC) interrupt
- Reset (0), disables the RTC interrupts

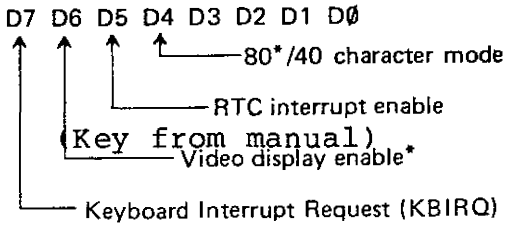
Bit 4 (D4)

- 1, enables the 40 character mode and disables the 80 character mode
- 0, enables the 80 character mode and disables the 40 character mode.

Bit 3 through 0 (D3 - D0)

- Selects 1 of 16 memory banks. Note that if we hit the Reset, the RTC interrupt is disabled.

Non-maskable Interrupt mask Register:
Read only



Bit 7 (D7)

- **1, Keyboard interrupting**
- **0, No Keyboard interrupting**

Bit 6 (D6)

- 1, Video Display disabled
- 0, Video Display enabled

Bit 5 (D5)

- RTC interrupt enable

Bit 4 (D4)

- 80*/40 character mode*

Bits 3 through 0 (D3-D0)

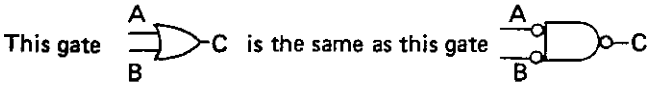
- They are "don't care" bits (not used)

Now that we know how these different ports will be used, we can set the control bits, say in Port FF, the way we want to. This means that we will be writing into Port FF. Therefore, the FFWR* signal is activated. If, for example, we set bit 7 to 1, bit 6 to 0, bit 5 to 1, and bit 4 to 0, FFWR* will latch this data vector into our system and the following results will be obtained:

Pin 11 of U41 will be high, thus enabling the 2K byte Video RAM. BLNKVID*, Q3 (pin 14 of U18), will go high and disable the blank Video (Video on).

The Real Time Clock (RTC), U18 pin 3, is enabled. This produces a low (0) at U18 pin 7. This generated signal is what we previously called the 80*/40 character mode. In this case, the 80* character mode is enabled (low). It is inverted at U30 pins 1, 2, and 3 and NANDed with RCLOCK* to appear at the output of the NAND gate U28, pins 8, 9, and 10 as CLOCK (TP26).

Note that the OR gate (U3 pins 4, 5, and 6) is drawn as a NAND gate.



The OR gate is sometimes shown as above because we are using mostly active low signals. You can go from one gate to another by using DeMorgan's Theorem.

For the above example, the following equation applies:

$$\overline{\overline{A}\,\overline{B}} = \overline{A} + \overline{B} = A + B = C$$

If we want to Read the Status of Port FF, we activate the FFRD* signal to enable the 3-state buffers LS240, U38. This will produce the status of the KBIRQ*, the BLNKVID*, the 80*/40 character mode*, and the ENABLE RTC INT* as shown at the inputs 2, 4, 6, and 8 of U38.

Other Blocks

The 3-state Buffers (U36, U37) are enabled by either the Video Read (VRD) or Write* (WR*). VRD is the result of the RD signal ANDed with MSP (U13 pins 11, 12, and 13). VWR* is the output of WR NANDed with MSP (U2 pins 11, 12, and 13).

When the CPU wants to write data into the Video RAM, WR* goes low (U36, U37 pin 1). When it does, a reading from the Video RAM, VRD (high) is active (pin 15 of U36, U37). Test points TP2 and TP24 will help detect if data is read from or written into the Display RAM by the CPU.

The keyboard control consists of an LS74 Flip-Flop (U17, pins 9, 11, and 12) showing the keyboard mode. That is, when data is being clocked in from the keyboard, a busy signal is sent to the system bus at the end of every word (8 bits of data). A busy (active low) signal goes from pin 9 of U17 back to the keyboard processor, telling it to stop sending data. Also, the same signal goes toward the CPU under the name of Keyboard Interrupt Request (KBIRQ*), telling it that a word of data is ready to be read. Data is clocked serially out of the keyboard into the shift register (U6) and then latched into the system data bus when FCRD* port is activated. Note that when FCRD* is activated (low), the Flip-Flop (U17 pins 11 and 12) becomes set and the KBIRQ* or BUSY* signal goes high (disable). Now that the keyboard logic does not receive the active busy signal, it will start sending data again.

The timing diagram of Figure 7-14 shows how data leaves the keyboard in serial fashion. Notice the narrower pulse labeled End Of Data pulse. It is generated at the end of an 8 data bit sequence. Its rising edge latches a low to the output of U17 pin 9. This low signal (KBIRQ* or BUSY*) informs the CPU that a word is ready to be read. It also prevents the keyboard from sending more data until the

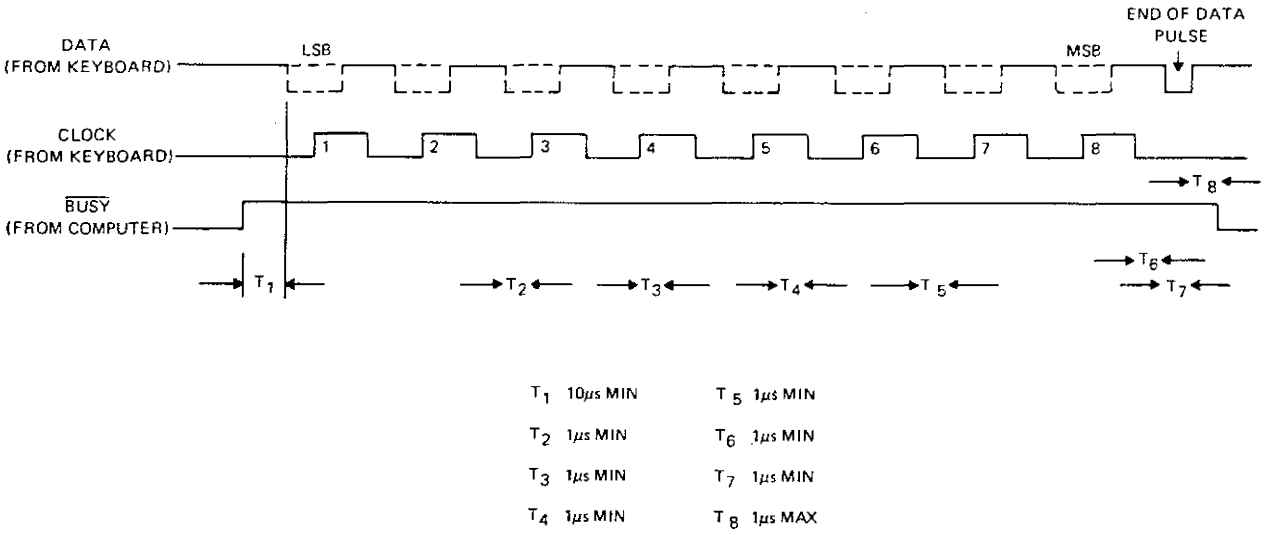


Figure 7-14. Keyboard Timing Diagram

actual 8 bit word at the output of the shift register (U6) is buffered into the data bus (in other words, read by the CPU).

The RTC and NMIRQ* logic block takes the VSYNC signal, divides it by 2 (U16 pins 8, 9, 11, and 12) to yield a 30 Hz RTC. The 60/30 Hz RTC signal clocks a high into the output of U16 pin 5 to generate an RTC interrupt (RTCINT) signal that is ANDed with ENABLE RTC INT (U29 pins 1 and 2). The output of U29 (pin 13) is then inverted and sent to the system bus as a Non-maskable Interrupt Request (NMIRQ*). Note that this signal is cleared by activating Port FERD* (Flip-Flop U16 pin 1).

The pulse-width adjuster is as defined in the earlier section of this text. It consists of a monostable multivibrator with Schmitt-trigger inputs that provide noise immunity and pulse-width stability to the horizontal sync signal (U5, 74121). The remaining parts of the system block diagram, such as the Latch, the character ROM, the Shift Register, etc., can be better defined by tracing the data path as follows:

The CPU writes a word of data into the Video RAM. The CRT controller, which automatically displays the information represented by Video RAM contents on the Video screen, moves that word and stores it temporarily in the Latch. The Latch will retain the byte for processing so that the RAM can get ready to send the next byte. The Latch is an LS273. When activated (by TCLK*), U8 latches the data. This data, along with RA0-RA3 from the CRTC, constitute an address for the ROM. The data from Memory (U8) specify a character. The RA0-RA3 specifies the row of the character matrix to be displayed in ASCII form. Note that the 8th bit is used as a Reverse Video signal (REVID). U9 is the character generator. The seven-bit ASCII word applied to its inputs would address a certain area in it. These ASCII inputs are considered the higher seven bits of an address. The lower part of the address comes from the CRTC (RA0-RA4). This lower part selects the row position of the addressed dot pattern.

Each character consists of a dot matrix, 8 dots wide and 10 dots high. Since each character consists of a pattern of dots, there must be some method to determine which dot should be on and which dot should be off to form any one character. The character generator controls the dot patterns on the screen.

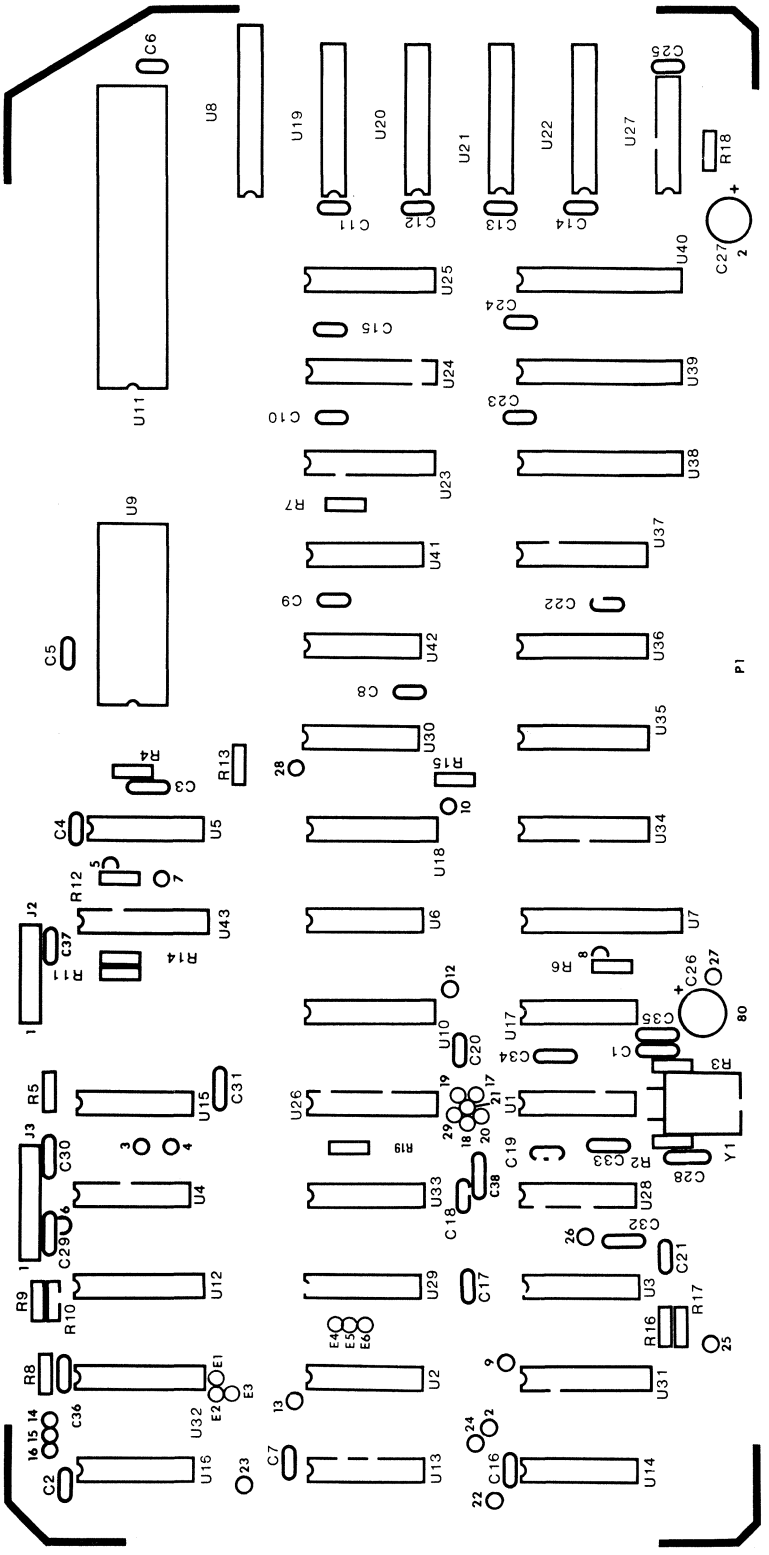
U9 outputs 8 dots (on or off) at the same time. RA0 through RA4 selects the row of the addressed pattern. The character generator must output 10 times to build one character.

Here is how a typical character line is written:

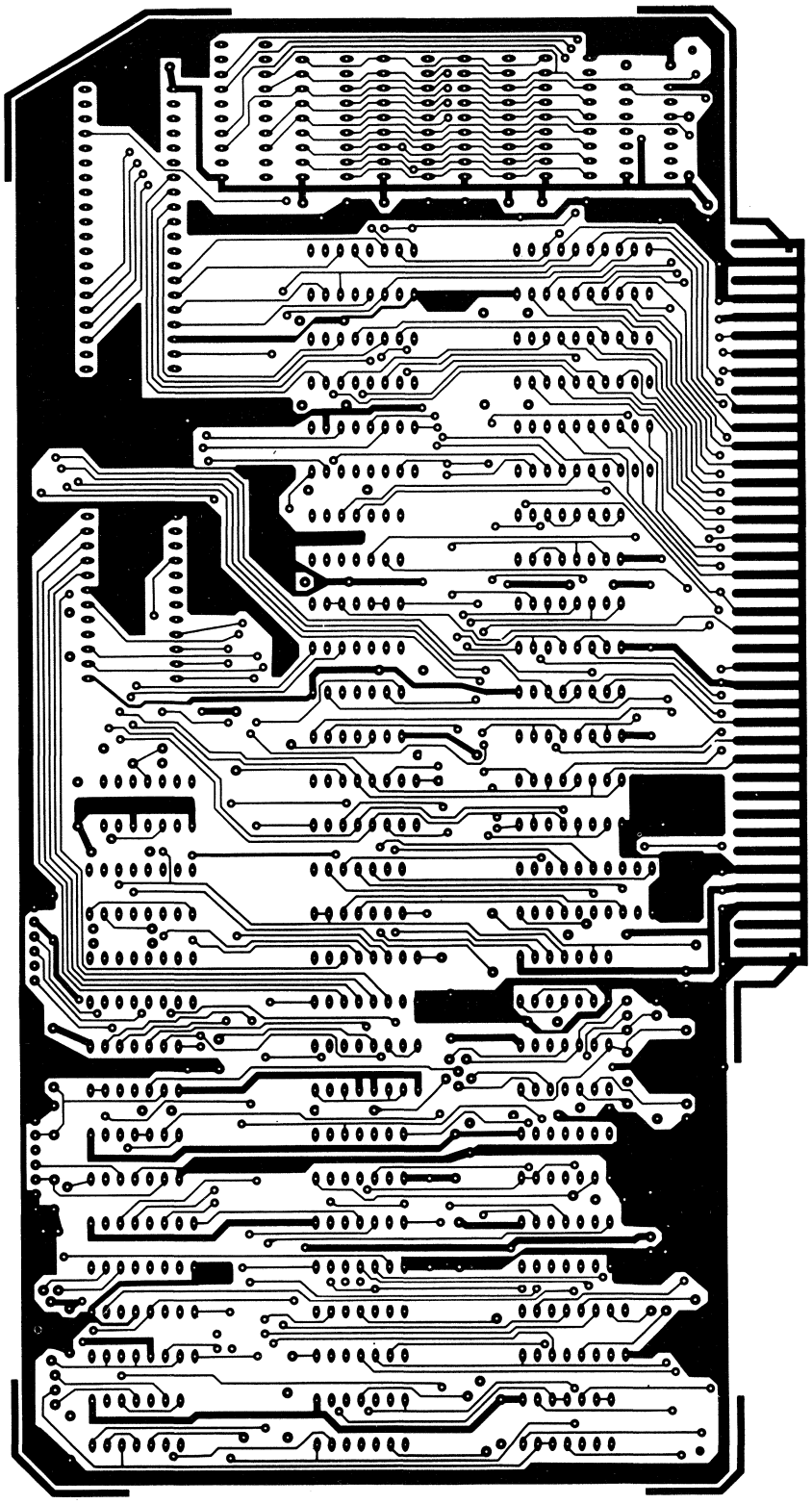
Assume an ASCII word is in the Latch. The electron beam is on the first scan line of the character. Therefore, the row address is binary "0". That is, RA0 through RA4 are low, U9 outputs the first dot pattern for that particular ASCII character. The next ASCII character is applied to U9. At the same time, the row address is incremented. It is now binary "1" pointing to the second scan line. Keep in mind that the electron beam does not stop at the last dot of the first pattern, but continues scanning the rest of the entire scan line. By the time the second dot pattern goes out, the third ASCII word comes in. This process goes on until the entire character (10 rows) is written on the screen.

The various dot patterns are loaded into the shift register U10 in parallel and are shifted out of it serially. All of this is done so fast that it seems that the entire character

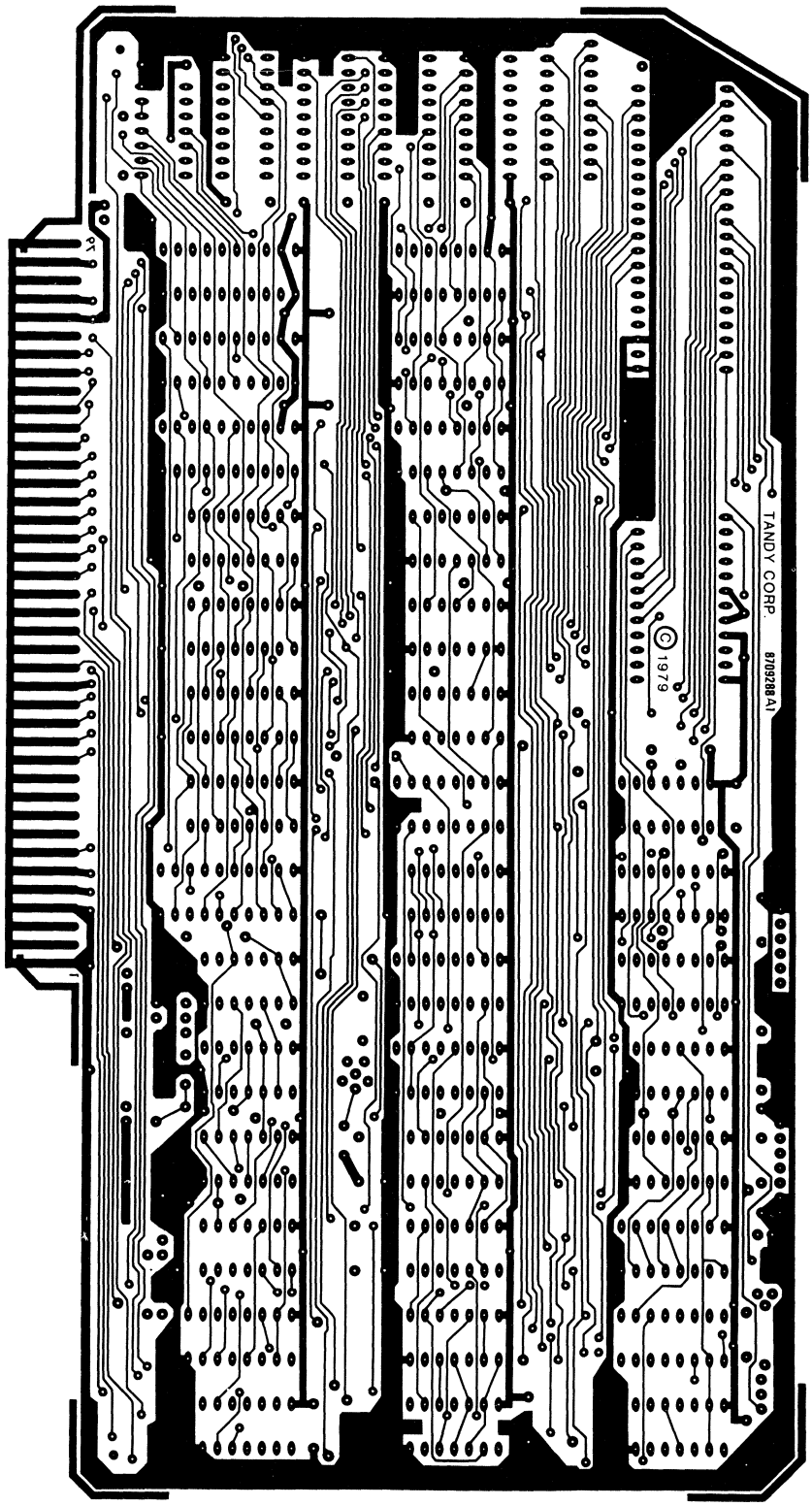
is displayed "not in pieces" but as a single entity. After the eight dot scans are output, the electron beam is turned off and two rows (the 9th and 10th) of blank dots are output. This provides separation between character lines. Once these two rows are output, the system is ready to output the first row of the second character line. Following the path the data goes through before being output at pin 9 of U10 (Vout), the Vout signal is delayed quite a bit with respect to the Display Enable and Cursor signals. For this reason, the two signals are delayed by two TADCLK cycles and Reverse Video (REVID) is delayed by one TADCLK cycle with respect to the Vout signal. This is shown by U12. Note how the delayed cursor and DREVID are exclusive ORed (U4 pins 12 and 13). The resulting signal at pin 11 of U4 is also exclusive ORed with Vout (U4 pins 9 and 10). Either the cursor, the Reverse Video or the Video will be displayed in a character location, but not two of them at the same time. The signal output at pin 8 of U4 is finally enabled by the Display enable and either one of the RCLOCK, RCLOCK*, RCLOCKP, or RCLOCKP* signals. One of these signals is chosen to achieve the best result. The final signal at pin 12 of U15 is simply called VIDEO. The VIDEO, HSYNC, and VSYNC signals are separately shielded and sent to the CRT Logic board (ground signals are wrapped around them).



Component Layout, Video/Keyboard PCB 8898022



Circuit Trace, Video/Keyboard PCB 8898022, Component Side



Circuit Trace, Video/Keyboard PCB 8898022, Solder Side

Parts Lists, Video/Keyboard Interface, 8898022

Ref. No.	Description	Part No.
Capacitors		
C1	Capacitor, 0.01 uF 50V	8303102
C2	Capacitor, 0.1 uF, 50V	8374104
C3	Capacitor, 1000 pF, 50V	8302104
C4	Capacitor, 0.1 uF, 50V	8374104
C5	Capacitor, 0.1 uF, 50V	8374104
C6	Capacitor, 0.1 uF, 50V	8374104
C7	Capacitor, 0.1 uF, 50V	8374104
C8	Capacitor, 0.1 uF, 50V	8374104
C9	Capacitor, 0.1 uF, 50V	8374104
C10	Capacitor, 0.1 uF, 50V	8374104
C11	Capacitor, 0.1 uF, 50V	8374104
C12	Capacitor, 0.1 uF, 50V	8374104
C13	Capacitor, 0.1 uF, 50V	8374104
C14	Capacitor, 0.1 uF, 50V	8374104
C15	Capacitor, 0.1 uF, 50V	8374104
C16	Capacitor, 0.1 uF, 50V	8374104
C17	Capacitor, 0.1 uF, 50V	8374104
C18	Capacitor, 0.1 uF, 50V	8374104
C19	Capacitor, 0.1 uF, 50V	8374104
C20	Capacitor, 0.1 uF, 50V	8374104
C21	Capacitor, 0.1 uF, 50V	8374104
C22	Capacitor, 0.1 uF, 50V	8374104
C23	Capacitor, 0.1 uF, 50V	8374104
C24	Capacitor, 0.1 uF, 50V	8374104
C25	Capacitor, 0.1 uF, 50V	8374104
C26	Capacitor, 33 uF, 16V	8326331
C27	Capacitor, 33 uF, 16V	8326331
C28	Capacitor, 15 pF, 50V	8300154
C29	Capacitor, 100 pF, 50V	8301104
C30	Capacitor, 150 pF, 50V	8301154
C31	Capacitor, 100 pF, 50V	8301104
C32	Capacitor, 100 pF, 50V	8301104
C33	Capacitor, 100 pF, 50V	8301104
C35	Capacitor, 100 pF, 50V	8301104
C36	Capacitor, 0.1 uF, 50V	8374104
C37	Capacitor, 0.1 uF, 50V	8374104
C38	Capacitor, 100 pF, 50V	8301104
Connectors		
J2	Connector, RT Angle, 6-Pin	8519017
J3	Connector, RT Angle, 7-Pin	8519022

Parts Lists, Video/Keyboard Interface, 8898022

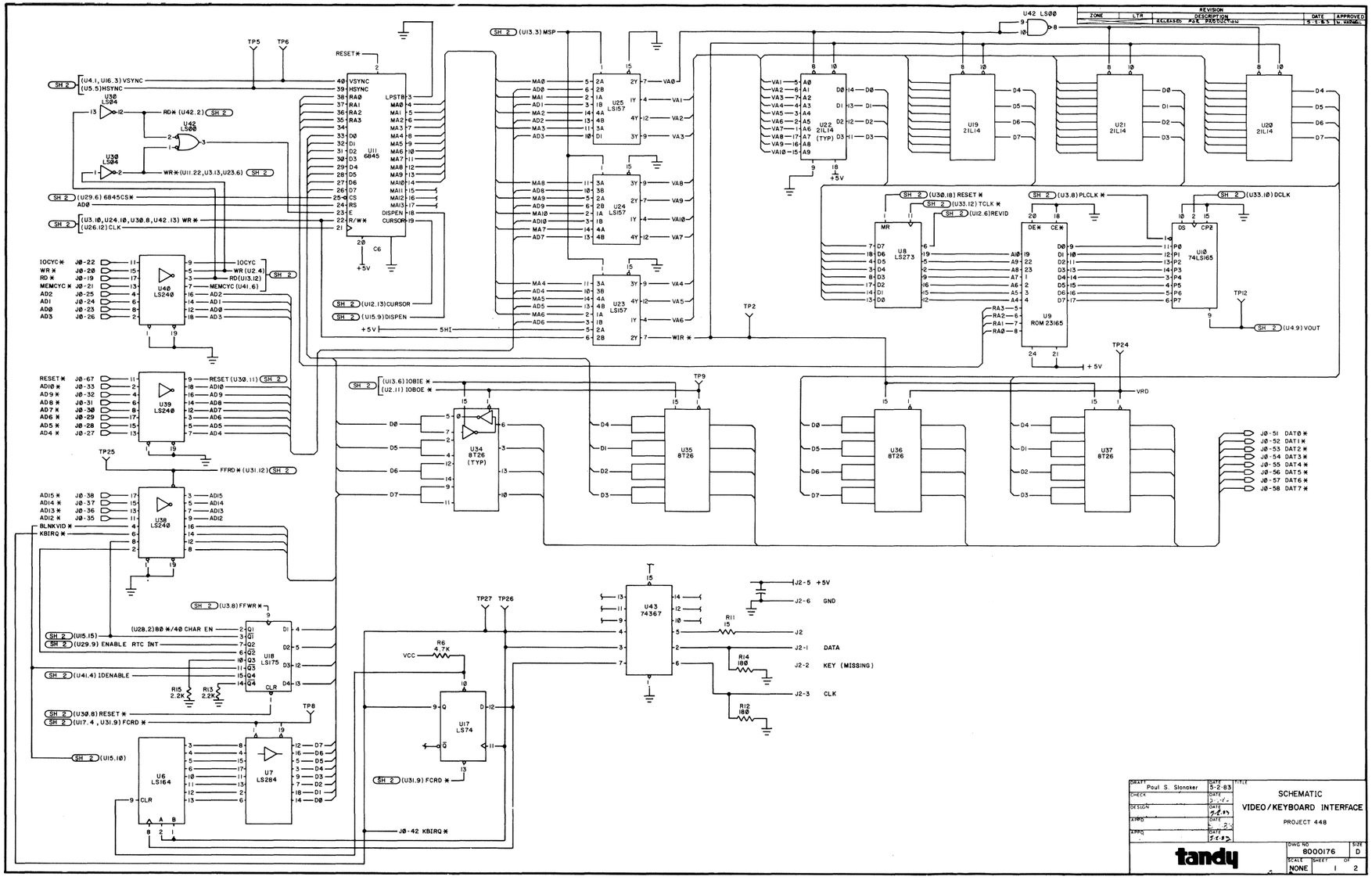
Ref No.	Description	Part No.
Resistors		
R2	Resistor, 470 ohm, 1/4W 5%	8207147
R3	Resistor, 470 ohm, 1/4W 5%	8207147
R4	Resistor, 39k ohm, 1/4W 5%	8207339
R5	Resistor, 4.7k ohm, 1/4W 5%	8207247
R6	Resistor, 4.7k ohm, 1/4W 5%	8207247
R7	Resistor, 4.7k ohm, 1/4W 5%	8207247
R8	Resistor, 4.7k ohm, 1/4W 5%	8207247
R9	Resistor, 2.2k ohm, 1/4W 5%	8207222
R10	Resistor, 2.2k ohm, 1/4W 5%	8207222
R11	Resistor, 15 ohm, 1/4W 5%	8207015
R12	Resistor, 180 ohm, 1/4W 5%	8207118
R13	Resistor, 2.2k ohm, 1/4W 5%	8207222
R14	Resistor, 180 ohm, 1/4W 5%	8207118
R15	Resistor, 2.2k ohm, 1/4W 5%	8207222
R16	Resistor, 2.2k ohm, 1/4W 5%	8207222
R17	Resistor, 2.2k ohm, 1/4W 5%	8207222
R18	Resistor, 4.7k ohm, 1/4W 5%	8207247
R19	Resistor, 8.2k ohm, 1/4W 5%	8207282
Integrated Circuits		
U1	IC, SN74LS04NDS	9020004
U2	IC, SN74LS00NDS	9020000
U3	IC, SN74LS32NDS	9020032
U4	IC, SN74LS86NDS	9020086
U5	IC, N7412NB	9000121
U6	IC, SN74LS164NDS	9020164
U7	IC, SN74LS244NDSW	9020244
U8	IC, SN74LS273NDS	9020273
U9	IC, 2316	_____
U10	IC, SN74LS165NDS	9020165
U11	IC, 6845	_____
U12	IC, SN74LS174NDS	9020174
U13	IC, SN74LS08NDS	9020008
U14	IC, SN74LS33NDS	9020033
U15	IC, SN74LS11NDS	9020011
U16	IC, SNB74LS74ANDS	9020074
U17	IC, SNB74LS74ANDS	9020074
U18	IC, SN74LS175NDS	9020175
U19	IC, 21L14	_____
U20	IC, 21L14	_____
U21	IC, 21L14	_____
U22	IC, 21L14	_____
U23	IC, SN74LS157NDS	9020157
U24	IC, SN74LS157NDS	9020157

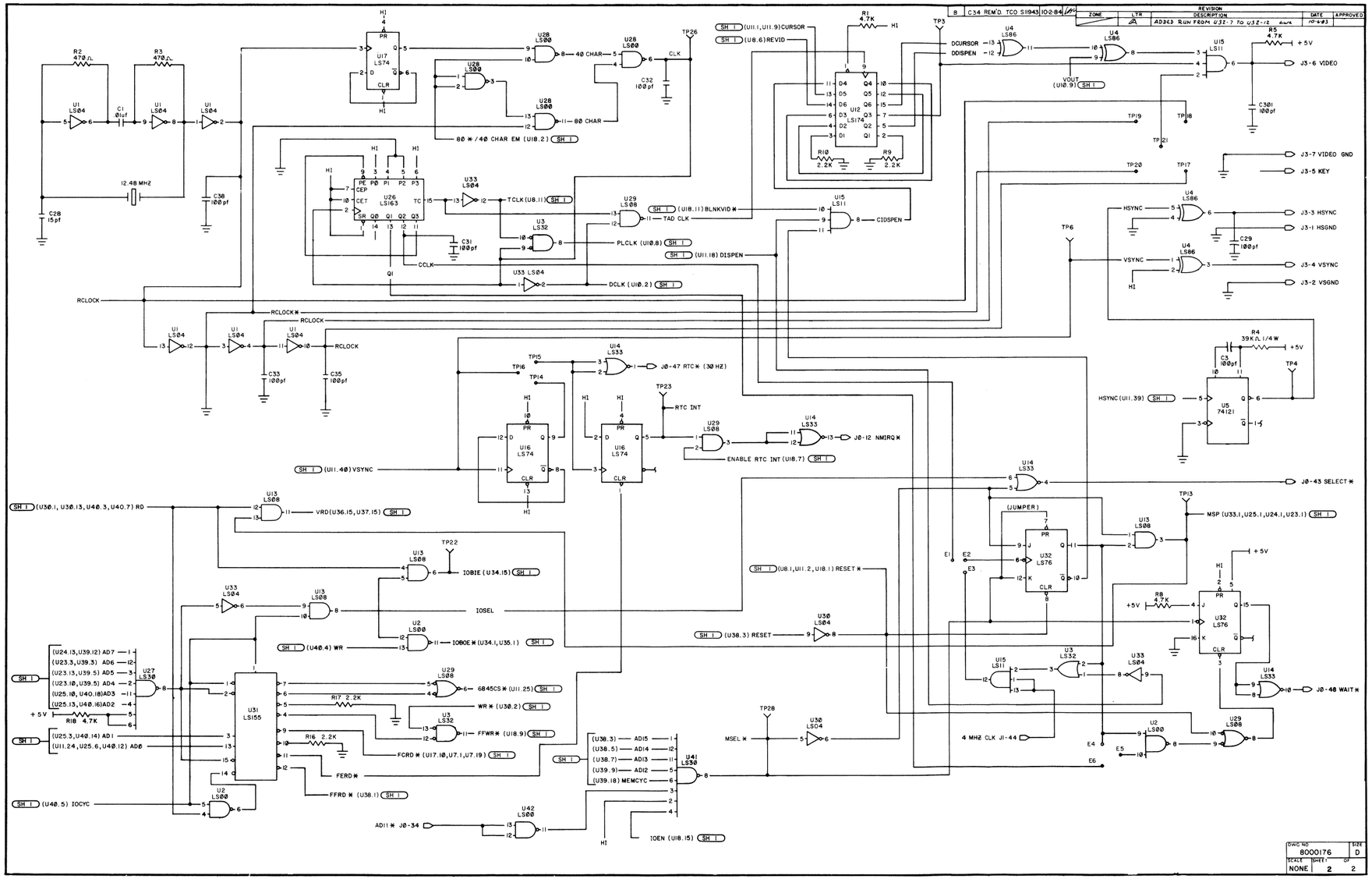
Parts Lists, Video/Keyboard Interface, 8898022

Ref No.	Description	Part No.
U25	IC, SN74LS157NDS	9020157
U26	IC, SN74LS161NDS	9020161
U27	IC, SN74LS30NDS	9020030
U28	IC, SN74LS00NDS	9020000
U29	IC, SN74LS08NDS	9020008
U30	IC, SN74LS04NDS	9020004
U31	IC, SN74LS155NDS	9020155
U32	IC, SN74LS76NDS	9020076
U33	IC, SN74LS04NDS	9020004
U34	IC, MC8T26APDS	9060026
U35	IC, MC8T26APDS	9060026
U36	IC, MC8T26APDS	9060026
U37	IC, MC8T26APDS	9060026
U38	IC, SN74LS240NDS	9020240
U39	IC, SN74LS240NDS	9020240
U40	IC, SN74LS240NDS	9020240
U41	IC, SN74LS30NDS	9020030
U42	IC, SN74LS00NDS	9020000
U43	IC, 74LS367	9020367

Miscellaneous

Item	Qty	Description	Part No.
PCB	1	Video/Keyboard Interface	8709288A
Socket	1	24-pin DIP (for U9)	8509001
Socket	1	40-pin DIP (for U11)	8509002
Socket	4	18-pin DIP (for U19-U22)	8509006
Y1	1	Crystal, 12.48 MHz	8409004


REVISION
ZONE | LTR | DESCRIPTION | DATE | APPROVED
RELEASED FOR PRODUCTION 5-6-83 L. HANNEL
U42 LS00
U30 LS04
U40 LS240
U39 LS240
U38 LS240
U6 LS164
U7 LS284
U11 6845
U18 LS175
U24 LS157
U25 LS157
U23 LS157
U22 21L14 (TYP)
U19 21L14
U21 21L14
U20 21L14
U8 LS273
U9 ROM 23165
U10 74LS165
U34 8T26 (TYP)
U35 8T26
U36 8T26
U37 8T26
U43 74367
U17 LS74
TP5
TP6
TP2
TP9
TP24
TP25
TP27
TP26
TP8
TP12
RESET*
VSYNC
HSYNC
RD* (U42.2)
WR* (U11.22,U3.13,U23.6)
6845CS*
CLK
WR*
IOCYC*
RD*
MEMCYC*
AD2
AD1
AD0
AD3
RESET (U30.11)
AD10*
AD9*
AD8*
AD7*
AD6*
AD5*
AD4*
FFRD* (U31.12)
AD15*
AD14*
AD13*
AD12*
BLNKVID*
KBIRQ*
FFWR* (U3.8)
(U28.2)80*/40 CHAR EN
ENABLE RTC INT
IDENABLE
RESET*
FCRD*
CURSOR
DISPEN
MSP
IOBIE*
IOBOE*
VRD
+5V
5HI
VCC
R6 4.7K
R15 2.2K
R13 2.2K
R11 15
R14 180
R12 180
J2-5 +5V
J2-6 GND
J2
J2-1 DATA
J2-2 KEY (MISSING)
J2-3 CLK
J0-42 KBIRQ*
J0-51 DAT0*
J0-52 DAT1*
J0-53 DAT2*
J0-54 DAT3*
J0-55 DAT4*
J0-56 DAT5*
J0-57 DAT6*
J0-58 DAT7*
PLCLK*
DCLK
REVID
TCLK*
VOUT
DRAFT Paul S. Stonaker 5-2-83
CHECK
DESIGN 7-6-83
APPRO 5-2-83
APPRO 7-6-83
SCHEMATIC
VIDEO/KEYBOARD INTERFACE
PROJECT 448
tandy
DWG NO 8000176
SIZE D
SCALE NONE
SHEET 1 OF 2


REVISION
B C34 REM'D TCO SI1943 10-2-84
ZONE LTR DESCRIPTION DATE APPROVED
A ADDED RUN FROM U32-7 TO U32-12 mwk 10-6-83
12.48 MHZ
RCLOCK
RCLOCK*
CCLK
TCLK(U8.11) SH 1
PLCLK(U10.8) SH 1
DCLK(U10.2) SH 1
(SH 1)(U8.11)BLNKVID*
TAD CLK
(SH 1)(U11.18) DISPEN
CIDSPEN
(SH 1)(U11.1,U11.9)CURSOR
(SH 1)(U8.6)REVID
DCURSOR
DDISPEN
VOUT (U10.9) SH 1
+5V
J3-6 VIDEO
J3-7 VIDEO GND
J3-5 KEY
HSYNC
VSYNC
J3-3 HSYNC
J3-1 HSGND
J3-4 VSYNC
J3-2 VSGND
HSYNC(U11.39) SH 1
J0-47 RTC* (30 HZ)
RTC INT
J0-12 NMIRQ*
ENABLE RTC INT(U18.7) SH 1
(SH 1)(U11.40)VSYNC
J0-43 SELECT*
(SH 1)(U36.1, U36.13, U40.3, U40.7) RD
VRD(U36.15, U37.15) SH 1
MSP(U33.1, U25.1, U24.1, U23.1) SH 1
(JUMPER)
IOBIE(U34.15) SH 1
IOSEL
(SH 1)(U8.1, U11.2, U18.1) RESET*
(SH 1)(U40.4) WR
IOBOE*(U34.1, U35.1) SH 1
(SH 1)(U38.3) RESET
J0-48 WAIT*
(U24.13, U39.12) AD7
(U23.3, U39.3) AD6
(U23.13, U39.5) AD5
(U23.10, U39.5) AD4
(U25.10, U40.18) AD3
(U25.13, U40.16) AD2
(U25.3, U40.14) AD1
(U11.24, U25.6, U40.12) AD0
6845CS*(U11.25) SH 1
WR*(U30.2) SH 1
FFWR*(U18.9) SH 1
FCRD*(U17.10, U7.1, U7.19) SH 1
FERD*
FFRD*(U38.1) SH 1
(SH 1)(U40.5) IOCYC
(U38.3) AD15
(U38.5) AD14
(U38.7) AD13
(U39.9) AD12
(U39.18) MEMCYC
AD11* J0-34
IOEN(U18.15) SH 1
MSEL*
4 MHZ CLK J1-44
DWG NO 8000176
SIZE D
SCALE NONE
SHEET 2 OF 2

7.6 Power Supply Board

7.6.1 Functional Specifications

The Power Supply Assembly for the Tandy 6000/6000HD is a 140 watt switching power supply. The Printed Circuit Board is mounted to the electronic chassis bracket. Line input to the power supply module is made through an amp wafer with locking 3-pin socket header.

Pin 1	Line - Neutral
Pin 2	Blank
Pin 3	Line - High

Outputs are taken from an amp wafer with locking 15-pin PCB socket header.

Pin 1	-12 V	Pin 9	+5 V
Pin 2	-12 V	Pin 10	Common
Pin 3	Common	Pin 11	+5 V
Pin 4	Common	Pin 12	+5 V
Pin 5	Common	Pin 13	+24 V
Pin 6	Common	Pin 14	+12 V
Pin 7	Common	Pin 15	+12 V
Pin 8	+5 V		

In theory, the power supply rectifies the AC line to DC, then chops it at 20 kHz. The chopped DC voltage is then transformed to the required output voltages and rectified to low voltage isolated DC. Feedback loops are provided for voltage regulation and over-current protection.

The power supply may be jumper selected for either of the following ratings:

Vin -- 90 to 135 VAC @ 47 to 63 Hz input frequency
or 190 to 270 VAC @ 47 to 63 Hz input frequency

The Power Supply Assembly can withstand the following maximum ratings:

Vin (AC continuous) -- 140 V (input select 115 V)
or -- 280 V (input select 230 V)

Short Circuit, any output -- indefinite

		Min	Typ	Max	
Output Voltages	VO1	4.95	5.00	5.25	V
	VO2	11.40	12.00	12.60	V
	VO3	See Notes			
	VO4	21.60	24.00	26.40	V
	VO5	-11.40	-12.00	-12.60	V

VO4, no load tolerance

Note: 1) VO3 must not change from its initial value by more than + 100 millivolts under the following load conditions on the VO4 output.
a) A step increase in output current from 0.0A (initial condition) to 2.5A Max. decaying to 0.92A total within 350 msec.
b) A step increase in output current from 0.55A (initial condition) to 3.05A Max. decaying to 1.45A total within 350 msec.
2) The VO3 output may vary + 5% under all other conditions of rated line, load, and temperature.

		Min	Typ	Max	
Output Loads	IO1	3.0	4.3	13.36	A
	IO2	0.25	0.50	0.75	A
	IO3	0.10	1.0	1.5	A
	IO4	0	1.3	2.0	A
	IO5	0.05	0.1	0.2	A

		Min	Typ	Max	Units
OCP, Current Limit					
	ICL1	14.0	15.0	16.0	A
	ICL2	1.1	1.6	2.0	A
	ICL3	1.6	2.3	3.0	A
	ICL4	2.1	2.5	3.0	A
	ICL5	---	1.0	2.0	A

Note: VO5 is a thermally protected IC regulator.

		Min	Typ	Max	
OVP, Crowbar VCB1		5.94	6.25	7.00	V
Output Noise	VO1	---	---	50	mV p-p
	VO2	---	---	100	mV p-p
	VO3	---	---	100	mV p-p
	VO4	---	---	250	mV p-p
	VO5	---	---	50	mV p-p
Efficiency		70	80	---	%

	Min	Typ	Max	
Hold Up Time:				
Full Load Lo Line	10	18	---	mSec
Full Load Nom Line	16	30	---	mSec
Insulation Resistance				
Input to Output	100	1000	---	M ohm
Input to Ground	100	1000	---	M ohm
Output to Ground	100	1000	---	M ohm
Isolation				
Input to GND and Output	4.25	---	---	KVDC

Line Conducted EMI must meet FCC Part 155 requirement for a Class A computing device with a 10db margin.

7.6.2. Equipment for Test Set-Up

1. Isolation Transformer (minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-140 V Variable Transformer (Variac) -- used to vary the input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

3. Voltmeter -- Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

4. Oscilloscope -- Need X10 and X1 probes.

5. Load board with connectors -- See Table 7-5 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

Note: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without at least the minimum load shown in Table 7-5.

6. Ohmmeter

7.6.3 Set-Up Procedure

1. Set up as shown in Figure 7-15. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 V output, with DVMs. Also monitor the +5 V output with the oscilloscope using 50 mV/div sensitivity. The DVM monitoring the +5 V output can also be used to check the other outputs. See Paragraph 7.3.4 for test points within the power supply.

Output	Min Load Amps	R for Min Load	Max Load Amps	R for Max Load	J2 Pins
+5V V01	3.0	1.66 ohm 30 W	13.36	.34 ohm 130 W	8,9, 11,12
+12 V02	.25	48 ohm 6 W	.75	16 ohm 20 W	15
+12 V03	.10	120 ohm 4 W	1.5	8 ohm 40 W	14
+24 V04	0	Infinity	2.0	12 ohm 100 W	13
-12 V05	.05	2.4 ohm 1 W	.2	60 ohm 5 W	1,2

Table 7-9. Power Supply Voltage Chart

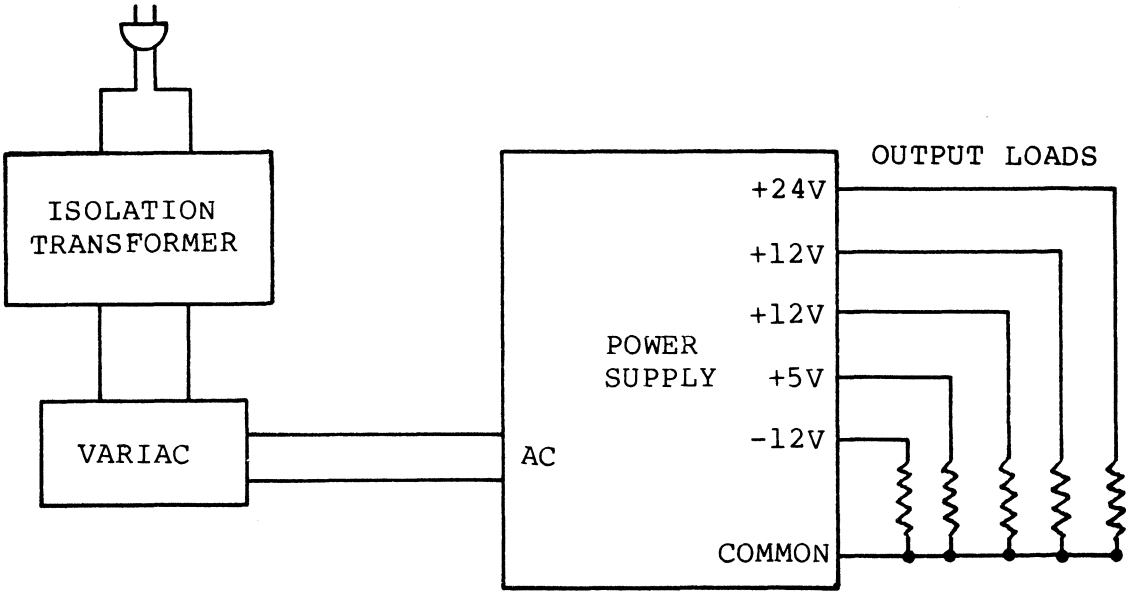


Figure 7-15. Test Layout, Power Supply

2. Visual Inspection

   Check power supply for any broken, burned, or obviously damaged components. Visually check the fuse. If any questions, check with an ohmmeter.

3. Start-Up

   Load power supply with minimum load as specified in Table 7-5. Bring up power slowly with the variable transformer while monitoring the +5 V output with the oscilloscope and DVM. The power supply should start with approximately 40-60 volts applied, and should regulate when 95 VAC is reached. If the output has reached 5 volts, complete a performance test as shown in Section 7.3.5. If there is no output, refer to Section 7.3.4.

4. Bracket Removal

   The main PCB is held to the bracket with screws and uses spacers to separate the PCB from the bracket. An insulator is inserted between the PCB and the mounting bracket to ensure that the bracket cannot short any of the pins of the PCB.

7.6.4. No Output

1. Check Fuse

   If a fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components

   Check diode bridge (DB1), power transistor (Q7), and catch diode (Q7) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check of Major Secondary Components

   Use an ohmmeter to check for shorted outputs on the various output lines. If the +5 V output is shorted, check also crowbar SCR (SCR1) and zener diode (Z1).

4. Check for B+

Set up power supply and attach the X10 scope probe ground to the cathode side of D5. Slowly turn up the power and check for B+ on the cathode side of D9. With an input of 95 VAC, this point should be betweeen 130 and 170 VDC. If this is not correct, check DB1, the fuse (F1), and if necessary, R5, D12, and D13. Also check input capacitors C5, C6, C7 and C8.

CAUTION

Your scope should be powered by an isolation transformer.

5. Check Q1 Waveforms

Using X10 probe on the case of TO-3 package of Q7, check the collector waveform. The transistor should be switching. The correct waveform is shown in Figure 7-16. If switching is not present, check for shorted junctions on Q7. If Q7 is not shorted, check the base waveform.

The base of Q7 (looking under the PCB) is the pin from the center of Q7 closest to the PCB edge. The correct waveform is shown in Figure 7-17. If the waveform is there, the problem is on the secondary side of the supply. If the wave form is not correct, the problem is in the control section of the supply and the supply should be returned to the repair depot.

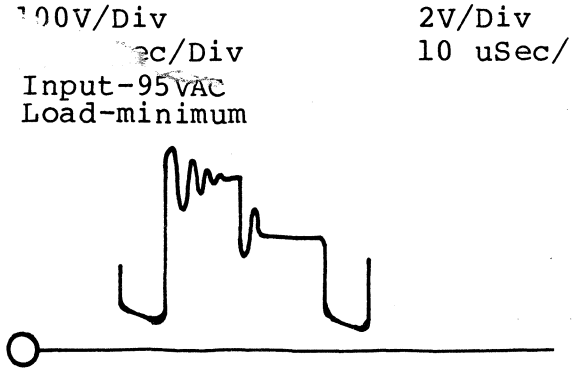


Figure 7-16. Q7 Collector Waveform

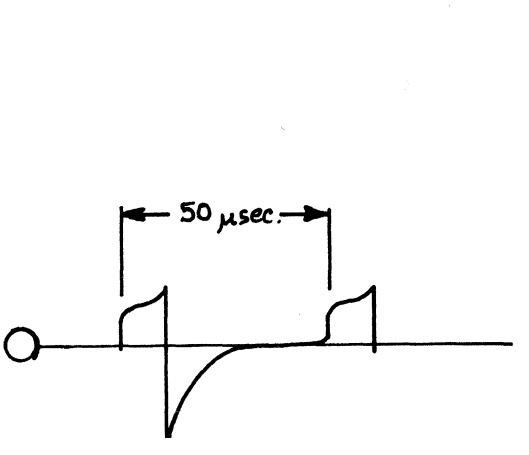


Figure 7-17. Q7 Base Waveform

7.6.5 Performance Test

Each of these test conditions should be set up and noted to be within the limits specified in Table 7-9.

Test	Input	+5 Load	+12 Load	+24 Load	-12 Load
1	95 VAC	Max	Max	Max	Max
2	135 VAC	Max	Max	Max	Max
3	*135 VAC	Max	Max	Max	Max
4	135 VAC	Min	Min	Min	Min
5	95 VAC	Min	Min	Min	Min

*On Test 3, input voltage should be varied over the full range to search for instability after correct outputs are noted at 135 VAC.

Output	Min	Max	No Load	Ripple
V01/+5 Volt	4.90V	5.10V	-	50 mV P-P
V02/+12 Volt	11.40V	12.60V	-	100 mV P-P
V03/+12 Volt	See Note 1	See Note 1	-	100 MV P-P
V04/+24 Volt	21.20V	26.40V	30.0V	250 mv P-P
V05/-12 Volt	-11.40	-12.60V	-	50 mV P-P

Table 7-10. Voltage and Ripple Specifications

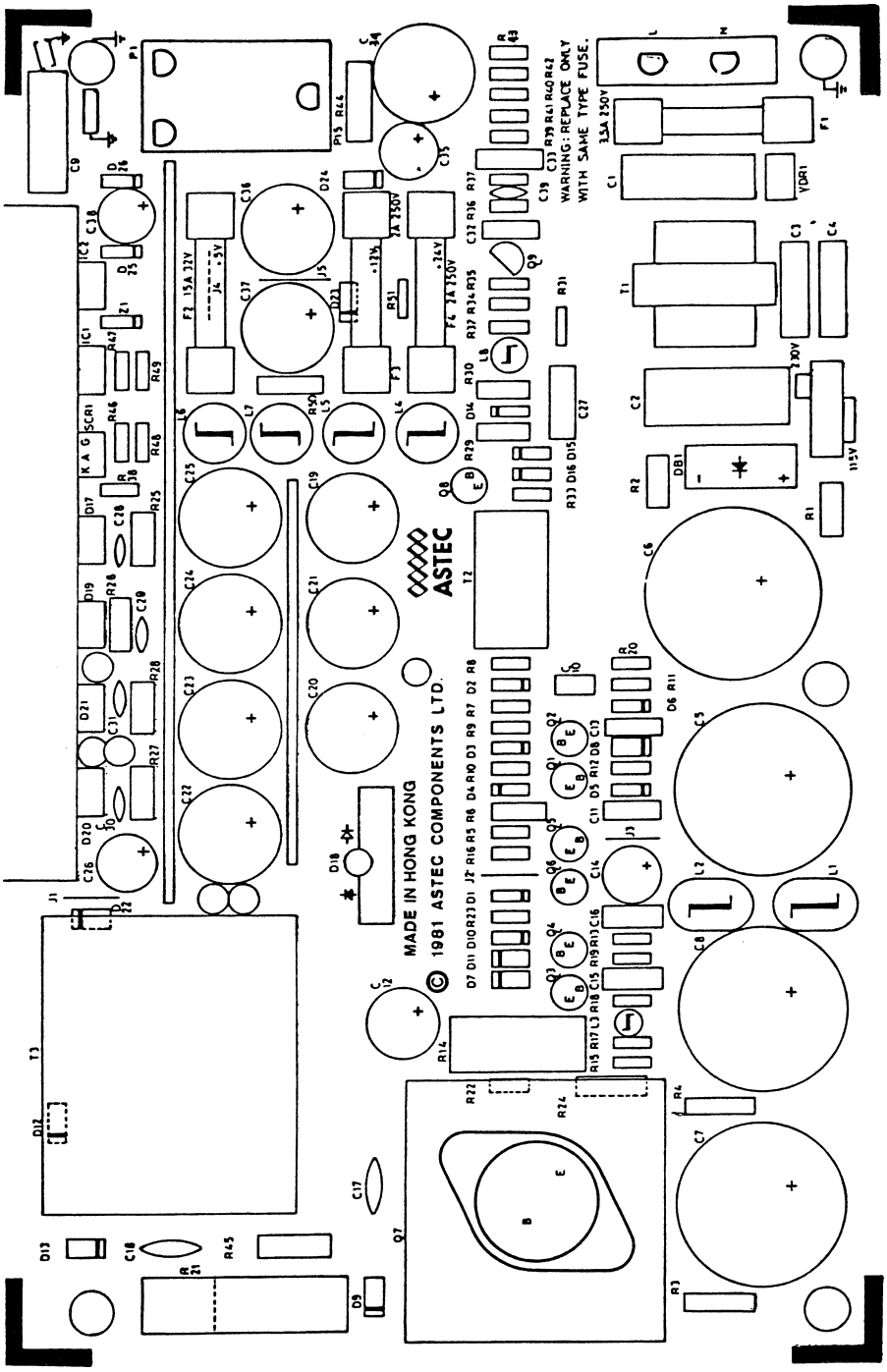
Notes:

1. V03 must not change from its initial value by more than +/- 100 mV under the following load conditions on the V04 output.

   A step increase in output current from 0.0A to 2.5A maximum decaying to 0.92A total within 350 ms.

   A step increase in output current from .55A to 3.05A maximum decaying to 1.45A total within 350 ms.

2. V03 output voltage may vary +/-5% under all other conditions of rated line load and temperature.



Component Layout, Power Supply 8790047

Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description	Mfr. Part No.
Capacitors		
C1	Capacitor, 0.1 uF, 250VAC, 20%	068-10400010
C2	Capacitor, 0.22 uF, 250VAC, 10%	068-22400010
C3	Capacitor, 2200 pF, 400VAC, 20%4)	055-22220001
C4	Capacitor, 2200 pF, 400VAC, 20%	055-22220001
C5	Capacitor, 220 uF, 250V, +100/-10%	057-22120200
C6	Capacitor, 220 uF, 250V, +100/-10%	057-22120200
C7	Capacitor, 220 uF, 250V, +100/-10%	057-22120200
C8	Capacitor, 220 uF, 250V, +100/-10%	057-22120200
C9	Capacitor, 0.01 uF, 250VAC, 20%	068-10300010
C10	Capacitor, 2200 pF, 50V, 10%	058-22200020
C11	Capacitor, 0.047 uF, 250V, 10%	058-47300090
C12	Capacitor, 330 uF, 25V, 20%	057-33120160
C13	Capacitor, 0.22 uF, 100V, 10%	058-22400120
C14	Capacitor, 220 uF, 10V, 20% SxA	059-22120300
C15	Capacitor, 0.22 uF, 100V, 10%	058-22400120
C16	Capacitor, 0.1 uF, 100V, 10%	058-10400110
C17	Capacitor, 1000 pF, 3KV, 20% Z5P	055-10267728
C18	Capacitor, 0.01 uF, 1KV, 20% Z5V	055-10368925
C19	Capacitor, 470 uF, 35V, 20% SxA	057-47120230
C20	Capacitor, 470 uF, 25V, 20% SxA	057-47120220
C21	Capacitor, 470 uF, 25V, 20% SxA	057-47120220
C22	Capacitor, 2200 uF, 25V, 20% SxA	057-22220130
C23	Capacitor, 2200 uF, 25V, 20% SxA	057-22220130
C24	Capacitor, 2200 uF, 25V, 20% SxA	057-22220130
C25	Capacitor, 2200 uF, 25V, 20% SxA	057-22220130
C26	Capacitor, 100 uF, 25V, 20% SxA	057-10120270
C27	Capacitor, 0.22 uF, 100V, 10%	058-22400120
C28	Capacitor, 1000 pF, 100V, 10%	055-10250528
C29	Capacitor, 0.01 uF, 100V, +80/-20%	055-10382125
C30	Capacitor, 0.01 uF, 100V, +80/-20%	055-10382125
C31	Capacitor, 0.01 uF, 100V, +80/-20%	055-10382125
C32	Capacitor, 0.022 uF, 100V, 20%	058-22300080
C33	Capacitor, 0.022 uF, 100V, 10%	058-22400120
C34	Capacitor, 1000 uF, 35V, 20% SM	057-10220190
C35	Capacitor, 100 uF, 25V, 20% SxA	057-10120270
C36	Capacitor, 1000 uF, 16V, 20% SxA	057-10220180
C37	Capacitor, 470 uF, 25V, 20% SxA	057-47120220
C38	Capacitor, 100 uF, 25V, 20% SxA	057-10120270
C39	Capacitor, 1000 pF, 100V, 10%	055-10250528
Coils		
L1	Toroid	124-00000110
L2	Toroid	124-00000110
L3	Choke, 1.5 mH	328-00100010

Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description	Mfr. Part No.
Coils (con't)		
L4	Choke Coil Assy	852-20100010
L5	Choke Coil Assy	852-20100010
L6	Filter Choke Coil Assy	852-20100220
L7	Filter Choke Coil Assy	852-20100220
Diodes		
D1	Diode, 1N4606	212-10700210
D2	Diode, 1N4606	212-10700210
D3	Diode, 1N4606	212-10700210
D4	Diode, 1N4606	212-10700210
D5	Diode, 1N4606	212-10700210
D6	Diode, 1N4606	212-10700210
D7	Rectifier, 1N4001GP	226-10400080
D8	Diode, 1N4606	212-10700210
D9	Rectifier, RGP10J	226-10400060
D10	Diode, 1N4606	212-10700210
D11	Rectifier, 1N4001GP	226-10400080
D12	Rectifier, RGP10J	226-10400060
D13	Rectifier, RGP10J	226-10400060
D14	Diode, 1N4606	212-10700210
D15	Diode, 1N4606	212-10700210
D16	Diode, 1N4606	212-10700210
D17	Rectifier, S6K20	226-11300010
D18	Rectifier, RG3B	226-10700010
D19	Rectifier, S6K20	226-11300010
D20	Diode, SCK S10SC3M	211-10300210
D21	Diode, SCK S10SC3M	211-10300210
D22	Rectifier, RGP10B	226-10400070
D23	Rectifier, 1N4001GP	226-10400080
D24	Rectifier, 1N4001GP	226-10400080
D25	Rectifier, 1N4001GP	226-10400080
D26	Rectifier, 1N4001GP	226-10400080
DB1	Bridge Rectifier, KBL08	226-30800010
Z1	Diode, Zener, 5.6V, 5%, 40mA	222-56086002
Fuses		
F1	Fuse, 3.5A, 250V, 3AG	084-00300110
F2	Fuse, 15A, 32V	084-00400020
F3	Fuse, 2A, 250V, 3AG	084-00300020
F4	Fuse, 2A, 250V, 3AG	084-00300020

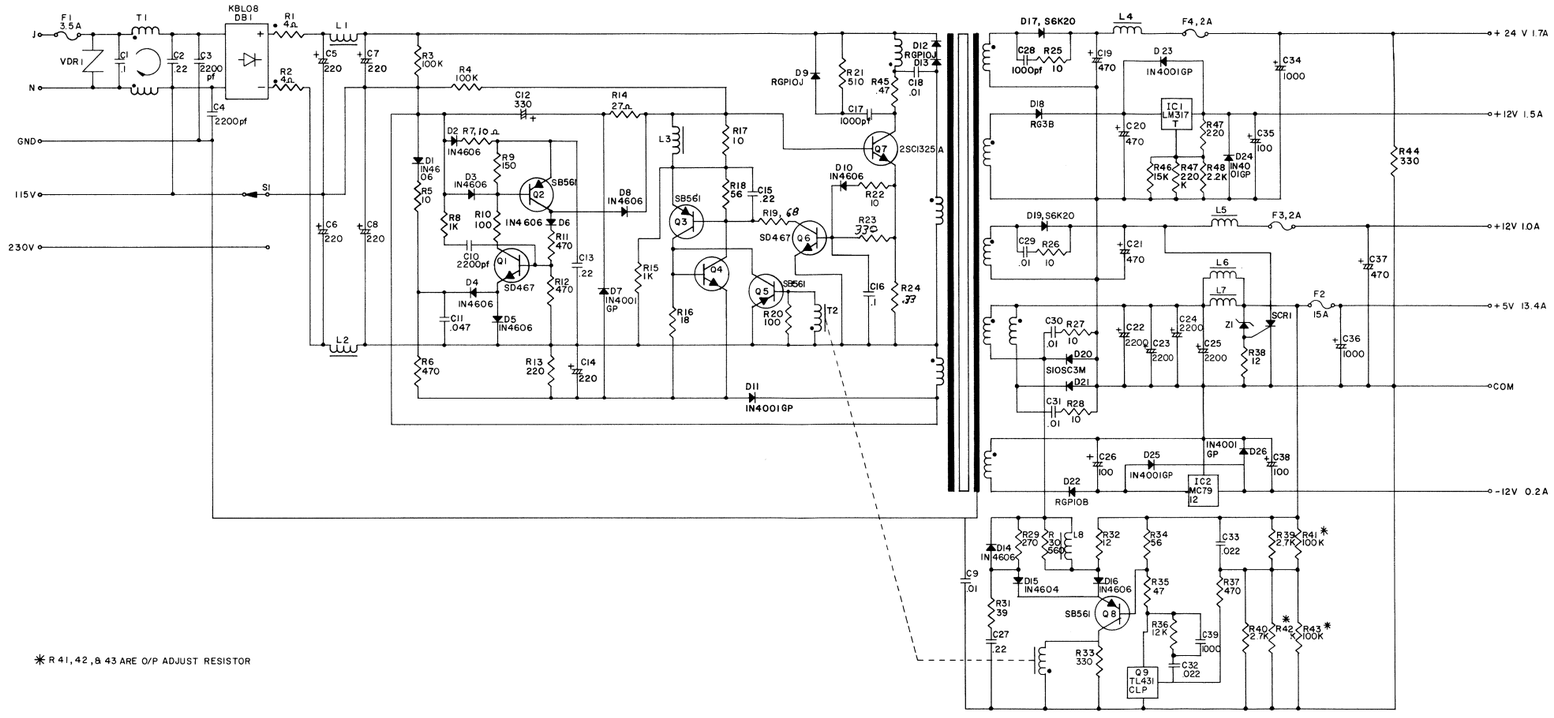
Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description	Mfr. Part No.
Jumpers		
J1	Jumper Wire, 12.7 mm	358-80800001
J2	Jumper Wire, 12.7 mm	358-80800001
J3	Jumper Wire, 12.7 mm	358-80800001
J4	Jumper Wire, 17 mm	358-80800001
J5	Jumper Wire, 17 mm	358-80800001
Integrated Circuits		
IC1	Regulator, LM317T	211-10300100
IC2	Regulator, MC7912	211-10300210
Resistors		
R1	Thermistor, 4 ohm, 10%	258-40970015
R2	Thermistor, 4 ohm, 10%	258-40970015
R3	Resistor, 100K ohm, 5% 1W	248-10406052
R4	Resistor, 100K ohm, 5% 1W	248-10406052
R5	Resistor, 10 ohm, 5% 1/4W	240-10006022
R6	Resistor, 470 ohm, 5% 1/2W	240-47106033
R7	Resistor, 10 ohm, 5% 1/4W	240-10006022
R8	Resistor, 1K ohm, 5% 1/4W	240-10206022
R9	Resistor, 150 ohm, 5% 1/4W	240-15106022
R10	Resistor, 100 ohm, 5% 1/4W	240-10106022
R11	Resistor, 470 ohm, 5% 1/4W	240-47106022
R12	Resistor, 470 ohm, 5% 1/4W	240-47106022
R13	Resistor, 220 ohm, 5% 1/4W	240-22106022
R14	Resistor, 27 ohm, 5% 5W, WW	257-27006120
R15	Resistor, 1K ohm, 5% 1/4W	240-10206022
R16	Resistor, 18 ohm, 5% 1/4W	240-18006022
R17	Resistor, 10 ohm, 5% 1/4W	240-10006022
R18	Resistor, 56 ohm, 5% 1/4W	240-56006022
R19	Resistor, 68 ohm, 5% 1/4W	240-68006022
R20	Resistor, 100 ohm, 5% 1/4W	240-10106022
R21	Resistor, 510 ohm, 5% 1/4W	257-51106120
R22	Resistor, 10 ohm, 5% 1/4W	240-10006022
R23	Resistor, 330 ohm, 5% 1/4W	240-33106022
R24	Resistor, .33 ohm, 5% 2W	
R25	Resistor, 10 ohm, 5% 1/2W	240-10006033
R26	Resistor, 10 ohm, 5% 1/2W	240-10006033
R27	Resistor, 10 ohm, 5% 1/2W	240-10006033
R28	Resistor, 10 ohm, 5% 1/2W	240-10006033
R29	Resistor, 270 ohm, 5% 1/2W	240-27106033
R30	Resistor, 560 ohm, 5% 1/2W	240-56106033
R31	Resistor, 39 ohm, 5% 1/4W	240-39006022
R32	Resistor, 12 ohm, 5% 1/4W	240-12006022
R33	Resistor, 330 ohm, 5% 1/4W	240-33106022

Parts List, Power Supply 8790047 (Astec Components AA11082)

Ref No.	Description	Mfr. Part No.
Resistors (con't)		
R34	Resistor, 56 ohm, 5% 1/4W	240-56006022
R35	Resistor, 47 ohm, 5% 1/4W	240-47006022
R36	Resistor, 12K ohm, 5% 1/4W	240-12306022
R37	Resistor, 470 ohm, 5% 1/4W	240-47106022
R38	Resistor, 12 ohm, 5% 1/4W	240-12006022
R39	Resistor, 2.7K ohm, 2% 1/4W	247-27015022
R40	Resistor, 2.7K ohm, 2% 1/4W	247-27015022
R41	Resistor, 100K ohm, 5% 1/4W	240-10406022
R42	Resistor, 68K ohm, 5% 1/4W	
R43	Resistor, 100K ohm, 5% 1/4W	240-10406022
R44	Resistor, 330 ohm, 5% 2W	248-33106063
R45	Resistor, 0.47 ohm, 5% 1W	247-04786054
R46	Resistor, 15K ohm, 5% 1/4W	240-15306022
R47	Resistor, 220 ohm, 2% 1/4W	247-22005022
R48	Resistor, 220K ohm, 5% 1/4W	240-22406022
R49	Resistor, 2.2K ohm, 1% 1/4W	247-22014022
Transformers		
T1	Transformer Assy	852-10200680
T2	Transformer Assy	852-10200680
T3	Transformer Assy, Power	852-10201300
Transistors		
Q1	Transistor, NPN, SD467	209-11700460
Q2	Transistor, PNP, SB561	210-11700350
Q3	Transistor, PNP, SB561	210-11700350
Q4	Transistor, NPN, SD467	209-11700460
Q5	Transistor, PNP, SB561	210-11700350
Q6	Transistor, NPN, SD467	209-11700460
Q7	Transistor, NPN, 2SC1325A	209-10200040
Q8	Transistor, PNP, SB561	210-11700350
Q9	IC, TL431CLP	211-10800100
Miscellaneous		
SCR1	SCR, C1 2u	227-13000010
VDR1	VDR, 260VAC	256-26100014

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		RELEASED FOR PRODUCTION	2-4-83	[illegible]
		UPDATED	4-7-83	SDS



* R41, 42, 43 ARE O/P ADJUST RESISTOR

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT DONALD R. BOOTH	DATE 2/3/83	TITLE SCHEMATIC-POWER SUPPLY MODEL 12
FINISH	TOLERANCES .XX= ± .010 .XXX = ± .005 ANGLES = ±1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			CHECK	DATE 2-4-83	
				DESIGN	DATE	
				APPD	DATE 2/1/83	
				~~APPD~~	DATE 2/9/83	REF. ASTEC AA11082
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING		448	tandy	DWG NO 8000194	SIZE D
	DO NOT SCALE THIS DRAWING	NEXT ASSY	USED ON		SCALE —	SHEET 1 OF 1

7.7 Sound Board

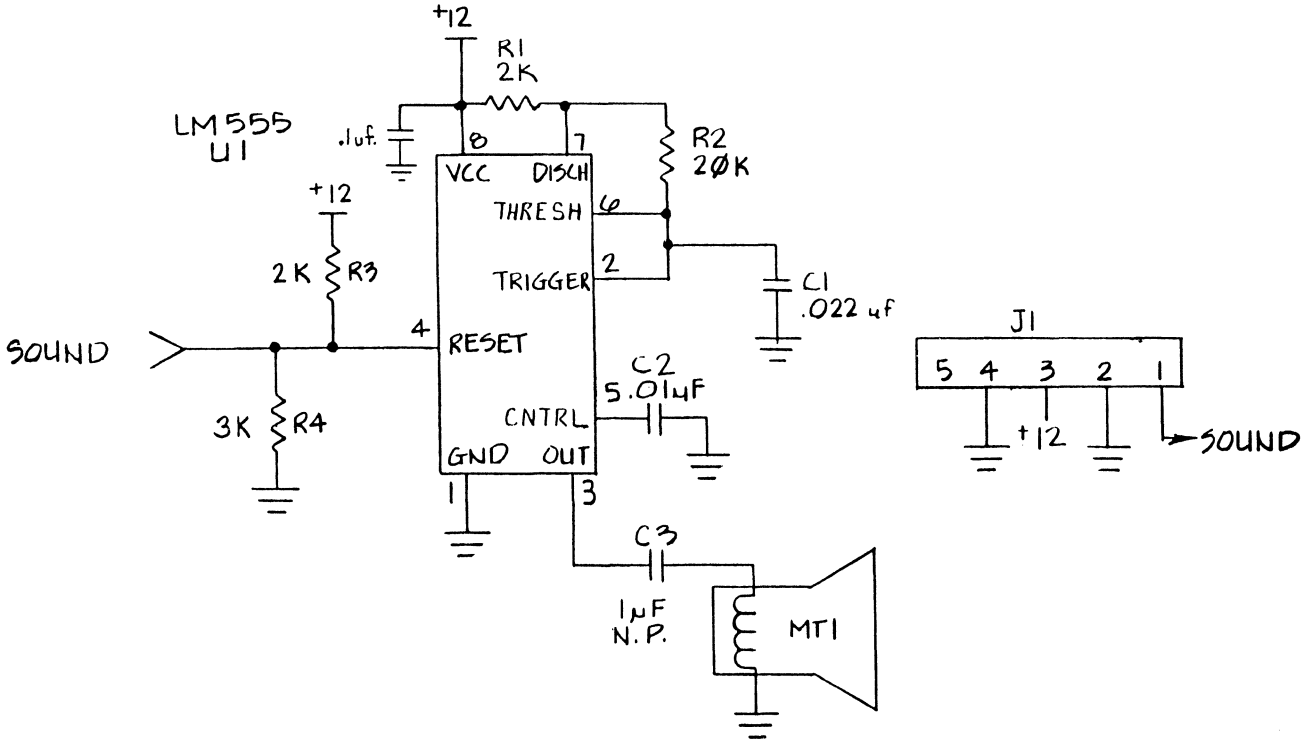
The Sound PCB is a small board located in the front left corner of the Base Assembly; it is accessible when the Cover/Bezel Assembly is removed from the Base Assembly (see Section 3 for disassembly procedures). It is connected to the I/O Processor PCB by a cable that has a connector on either end.

The function of the Sound PCB is to generate an audible signal whenever a key is depressed on the keyboard.

Contained on this board is an LM555 timer/oscillator that generates a 1558 Hz tone when a pulse is received from the computer. The voltage required to operate the circuit is 12 volts supplied from the computer at pin 3 of the input jack J1. The frequency of the device is controlled by R1, R2, and C1. There is no provision for varying the volume of the tone generated by the Sound PCB.

Parts List, Sound PCB, 8898429

Ref No.	Description	Part No.
C1	Capacitor, .022 mF, 50V, +50/-10%	8353224
C2	Capacitor, 0.01 mF, 50V	8303104
C3	Capacitor, 1 mF, 16V Elec Axial	8395111
C4	Capacitor, 0.1 mF, 50V Mono	8374104
C5	Capacitor, 10 mF, 16V Elec Radial	8326101
J1	Connector, 5-pin	8519162
---	PCB, Sound, Rev PP1	8709368
R1	Resistor, 2K ohm, 1/4W 5%	8207220
R2	Resistor, 3K ohm, 1/4W 5%	8207230
R3	Resistor, 2K ohm, 1/4W 5%	8207220
R4	Resistor, 20K ohm, 1/4W 5%	8207320
MT1	Transducer, QMB-12, 12V	8490002
U1	IC, NE555N	8050555



Schematic 8000165, Sound Board 8898429

7.8 CRT Assembly

The CRT Assembly on the Tandy 6000/6000HD is supplied from several different manufacturers. The assembly consists of the CRT, the CRT Monitor PCB, which is mounted to the inside of the Cover/Bezel Assembly, and the associated mounting hardware. Information concerning each of these assemblies is contained in the Appendix Section at the rear of this manual. This information includes a theory of operation of the CRT Assembly, schematic diagrams of the various configurations, and parts lists.

Disassembly procedures for the CRT Assembly are contained in Section 3 of this manual. Exercise care when handling the CRT as improper handling may cause personal injury.

When replacing the CRT, it must be replaced as an assembly, i.e., both the CRT and the CRT Monitor PCB must be replaced at the same time. Adjustment procedures, where applicable, are noted in the sections contained in the Appendix.

7.9 Keyboard Assembly

The keyboard of the Tandy 6000/6000 HD is an 82-key, low profile capacitive keyboard that utilizes an 8021 microprocessor chip.

The microprocessor and its associated circuitry scan the key matrix, convert switch closures to an 8-bit digital code and then transmits that code serially to the keyboard interface on the Video/Keyboard Interface PCB.

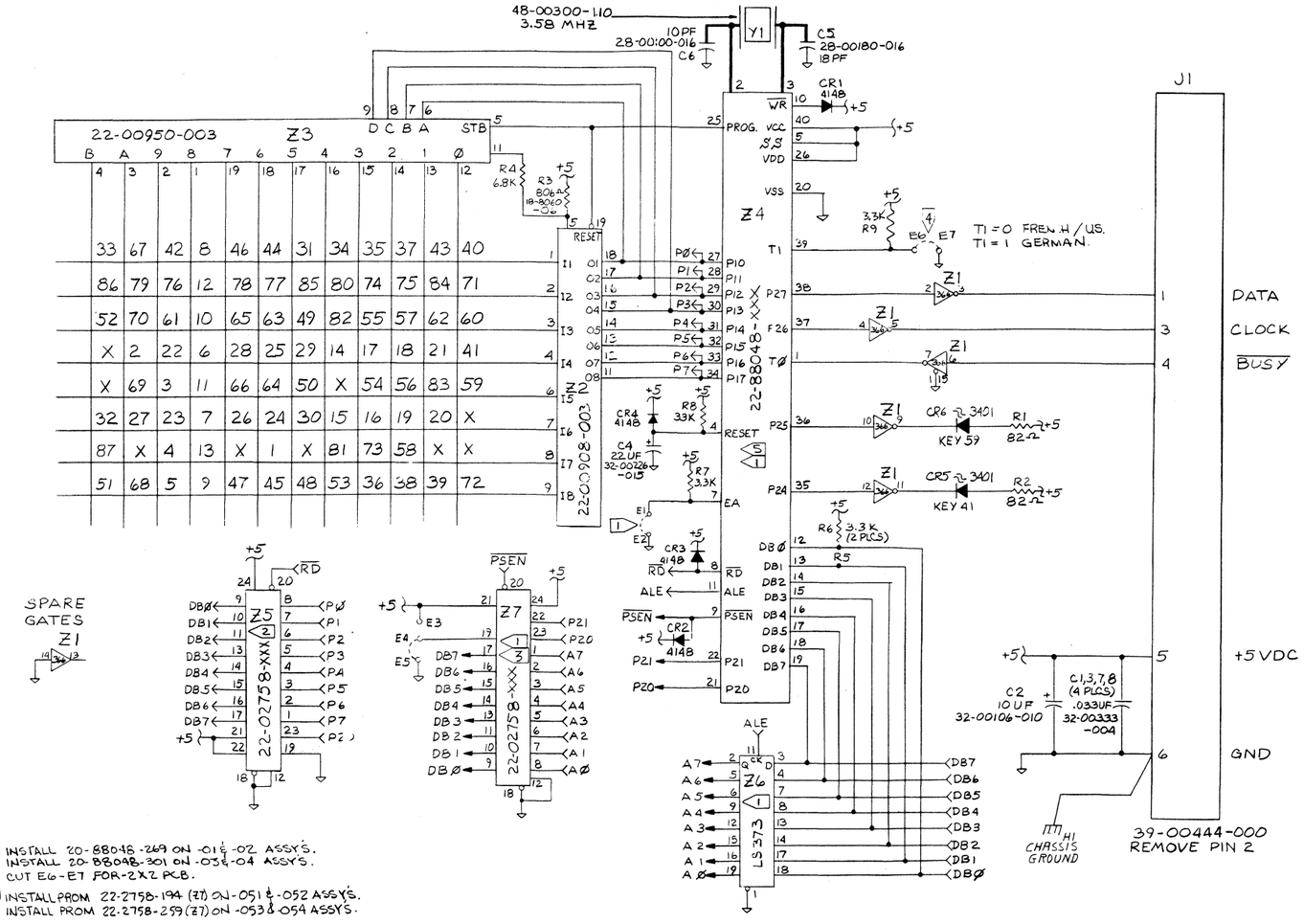
The keyboard is connected to the main console by a built-in cable that plugs into a connector mounted on the front surface of the Base Assembly. The interconnecting mating cable assembly is shown in Figure 5-9.

Parts List, Low Profile Keyboard 8790522

Ref No.	Description	Mfr. Part No.
Capacitors		
C1	Capacitor, C .033 uF, 25V	32-00333-004
C2	Capacitor, T 10 uF, 10V	32-00106-010
C3	Capacitor, C .033 uF, 25V	32-00333-004
C4	Capacitor, T 22 uF, 15V	32-00226-015
C5	Capacitor, C 18 pF, 50V	28-00180-016
C6	Capacitor, C 10 pF, 50V	28-00100-016
C7	Capacitor, C .033 uF, 25V	32-00333-004
C8	Capacitor, C .033 uF, 25V	32-00333-004
---	PCB, 1/16	01-02424-201
Diodes		
CR1	CRO, IN4148	21-04148-000
CR2	CRO, IN4148	21-04148-000
CR3	CRO, IN4148	21-04148-000
CR4	CRO, IN4148	21-04148-000
CR5	LED, 3401 RD LT	21-03401-001
CR6	LED, 3401 RD LT	21-03401-001
Integrated Circuits		
Z1	IC, 74366N	22-74366-001
Z2	IC, 908	22-00908-003
Z3	IC, 950	22-00950-003
Z4	Mup, masked	20-88048-269
Resistors		
R1	Resistor, 82 ohms, 5% 1/4W	25-00820-000
R2	Resistor, 82 ohms, 5% 1/4W	25-00820-000
R3	Resistor, 806, 1% 1/4W	18-08060-006
R5	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R6	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R7	Resistor, 3.3k ohms, 5% 1/4W	25-00332-000
R8	Resistor, 33K ohms, 5% 1/4W	25-00333-000
R4	Resistor, 6.8K ohms, 5% 1/4W	25-00682-000
	Connector, Right Angle 6 (J1)	39-00444-000
	Mount, S/B LP	44-00102-000
	Bar, S/B 30mm	44-00173-000
	Leg, S/B 30mm	44-00174-000
	Spring, 1.5 oz, 30mm, yellow	45-00053-015
	Spring, 3 oz	45-00053-030
	Screw, PH 4-40 .250	47-00008-002
	Screw, #2 high/low	47-00368-000

Parts List, Low Profile Keyboard 8790522

XTAL, 3.58 MHz, Dip (Y1)	48-00300-110
Mounting Plate	49-01143-000
Switch, 30mm Capacitor Assy	61-04024-001
Switch, 30mm Capacitor Assy Lt	61-04024-002
Switch, Capacitor 30mm	61-04031-001
Switch, Capacitor 30mm	61-04031-002
KYTP Set	



<5> INSTALL 20-88048-269 ON -016-02 ASSY'S.
INSTALL 20-88048-301 ON -036-04 ASSY'S.
<4> CUT E6-E7 FOR-2X2 PCB.
<3> INSTALL PROM 22-2758-194 (Z7) ON -051 & -052 ASSY'S.
INSTALL PROM 22-2758-259 (Z7) ON -053 & -054 ASSY'S.
<2> DO NOT INSTALL.
<1> ON -050 SERIES ASSYS. ONLY, INSTALL 20-88035-000 AT Z4, INSTALL Z6 & Z7, PER NOTE 3
DELETE CONNECTION E1 TO E2.

NOTES:

Schematic Diagram 8000196, Keyboard Assembly 8790522

7.10 Hard Disk Controller

7.10.1 System Overview

The Tandy 6000 with built in hard disk is identical to the standard 6000, except for the additional 15-meg HD drive, identical to the standard 16B (Cat. No. 26-6004), except for the addition of a 15-megabyte (formatted) hard disk drive, controller PC board, drive power supply, and associated cables. The drive is mounted next to the existing floppy drive in place of a second internal floppy. The power supply for the hard disk is mounted to the outside of the drive mounting tower. The controller PC board is located in the bottom slot of the card cage. There are two cables connecting the controller and the internal hard drive. There are also connectors on the controller for adding a secondary, external hard drive. The extra power supply is used to power the internal hard drive and a small cooling fan located under the drive tower. The controller PC board is powered from the main card cage.

7.10.2 Hard Drive Controller Board

The hard drive controller (HDC) board is a two sided PC board with the same form and size as those used in the Model II and Model 16. This board is designed to provide all control and data signals for connecting one internal and one external 5.25" Winchester technology drives.

1. Host System Interface

The HDC is connected to the 6000 motherboard via an 80-position card edge connector, J1. Data lines are passed through an AMD 8303 inverting transceiver, U39. Eight address lines are buffered by a 74lS240, U40. Most control signals are buffered by another 74lS240, U41. This board uses the Z80 interrupt priority daisy chain, so the board must be placed in either the bottom card slot, or the next one up, if the system also has an Arcnet board installed.

2. Port Decoding

The HDC uses a range of 16 consecutive eight bit port locations with the standard range being C0 to CF. Decoding of the correct range is done by U33, a 74S138 using the upper 4 address lines and M1 and IORQ*. A 4 position jumper enables changing of the range to be recognized. For normal use, the jumper should be installed between E1 and E2. See the following table for other configurations.

Jumper Location	Port Range Decoded
E1 to E2	C0 to CF Hex
E1 to E3	70 to 7F HEX
E1 to E4	60 to 7F HEX
E1 to E5	50 to 5F HEX

Table 7-11. Port Decoding

Further decoding is done by U34, a 74S139 that determines one of four 4 byte ranges. The first range is indicated by the signal SELDIR*, which indicates a select of ports C0-C3. This signal enables one half of another 74S139, U42, depending on a read or write operation. Only two outputs of U42 are used, those being WRDIR1* and RDDIR1*. WRDIR1* is used to clock data onto an octal latch, U12, and RDDIR1* is used to enable a read from that latch by turning on U21.

Normally the host data bus transceiver is turned to pass data to the controller board by the state of the signal M2DEN. A multiple and-nor gate, U15, is used to determine one of the following conditions and switch the direction of data flow toward the host system. The conditions are: a read from a port in the selected range, a read of one of the onboard CTC channels, or an interrupt acknowledge cycle.

The individual ports and their functions will now be listed referenced to the standard C0-CF range. A more detailed description will be given later.

Port Address	Description/Use
C0	Write protect status--read only
C1	Control-enable--write/read.
C2	Not used
C3	Not used
C4	CTC channel 0 control
C5	CTC channel 1 control
C6	CTC channel 2 control
C7	CTC channel 3 control
C8	Drive data register
C9	Read--drive error register
	Write--write precompensation
CA	Sector count register
CB	Sector number register
CC	Cylinder LSB register
CD	Cylinder MSB register
CE	SDH register
CF	Read--drive status register
	Write-- command register

Table 7-12. Ports and Functions

3. Drive Control and Interface

The main device on the controller board is the Western Digital WD1010 (U26). This is a MOS/LSI part that performs the function of drive controller/formatter. The WD1010 is software compatible with WD1000 series controllers with certain minor differences.

The WD1010 has an 8-bit bi-directional data bus through which it communicates with the host bus transceivers. Selection of the internal registers is accomplished by activating the appropriate address lines (A0-A2) and the chip select (CSI) line along with either read or write. The signals WR*IB and RD*IB are passed through a 74LS368 (U38) to the WD1010,the WD1100-11, and the sector buffer. This is done because the WD1010 uses CSI (U26-8) as a bi-directional signal. When the WD1010 is reading or writing data to the sector buffer it activates the signal BCS* (U26-1). This signal in the active high state, called DISHDB, is used to isolate the read and write lines from the rest of the board. DISHDB is also fed to the data bus transceiver (U39-9) to isolate the internal data bus from that of the system. Should the host attempt an access of the controller status register while the WD1010 is using the internal bus, the host will see a busy condition and should not attempt to issue any commands until the bus is free.

The WD1100-11 is essentially a gate array device that serves multiple functions on the controller board. First, it provides the drive and head select output lines to the drive interface. Also, it has two internal 1-shots -- one is used to shape the incoming drive data pulses to a specified width, the other is used to provide the signal DRUN, which tells the WD1010 when to begin attempting an ID read. Finaly, the WD1100-11 is the sector buffer managing device that handles the transfer of data, through the WD1010, between the host and the drive.

The sector buffer, U28, is a 2K x 8-bit static RAM with an access time of 150 nsec or faster. Data from the drive is loaded into it by the WD1010 and WD1100-11 for the host system to read. Data that is to be written onto the drive is placed into the sector buffer by the host, where the WD1010 will access it as needed.

The WD1010 and WD1100-11 provide a drive interface compatible with seagate ST506 type drives. Each drive has a separate data and control cable. The data and control signals for the internal primary drive are routed through connectors J4 and J5. For the external secondary drive,

data and control signals appear at connectors J3 and J2. By utilizing separate control output signal drivers for each drive, the need to terminate only the last logical drive has been eliminated. All drive terminators are left in. However, control signals coming into the controller board are fed from both drives into a 74LS14 (U19) and then to the WD1010. Drive select outputs determine which drive is producing these control input signals. Read and write data lines are transferred between drives and controller by means of an RS-422 standard driver-receiver pair, (U4 and U5).

4. Data Recovery

a. System Clock Oscillator

The fundamental clock frequency for the controller board is provided by a 20 MHz crystal oscillator, U2. One-half of U3 divides this down to a 10 MHz square wave signal called 2XDR, which is 2 times the drive data transfer rate. This clock is again divided down by U18 to provide a 5 MHz clock called WCLK, which is used to run the WD1010.

b. Phase Comparator

The phase comparator circuitry is comprised of a PAL16R6A (U18), a 60 nsec delay line (U37), and 3 D-type flip-flops (U1 and U7). When data is being inspected from the drive, its phase relationship must be determined with respect to the Vco clock. The function of the circuitry is to provide windows during which the leading edge of the incoming data is compared to the leading edge of the Vco. The windows are approximately 50 nsec in width. The window is initiated by the leading edge of any data bit as it enters U7-3 (INDATA). The window is terminated by the same data bit, delayed by 60 nsec, at U7-11 (DLYDATA) or by the Vco output (OSC*) at U1-3. When both DLYDATA and the nearest OSC* edge arrive at the detector, the detector is reset (by U17-6) until the next data bit arrives. DLYDATA sets its detector latch to produce a pump-up condition at the error amplifier, while the Vco (OSC*) sets its detector latch to produce a pump-down condition at the error amplifier.

c. Error Amplifier and Vco

The error amplifier is comprised of a transistor pack, U30, and a low pass filter. U30 is wired as a balanced current mirror device that sources or sinks current to the filter stage. Whenever the Vco is running slower than the incoming data stream, the error amp receives pump-up pulses. The filter integrates these pulses to provide an average

increase in the voltage reference to Vco (TP 3), causing the Vco to speed up. Whenever the Vco is running too fast,the error amp receives pump-down pulses and provides the Vco with an average decrease in control voltage (TP 3) which in turn slows down the Vco. The Vco is a 74S124, U16, which is initially set by C11 to a free running frequency of 10 MHz. Supply voltage for the Vco and error amplifier circuits is provided by a 78M05 +5 volt regulator (VR1). This insures noise isolation from TTL devices using the system +5 volt bus.

d. Write Precompensation

Write precompensation is accomplished by two means. First by the activation of the signal RWC which is produced by the WD1010 and driven onto the drive control interface. The WD1010 activates this signal whenever the heads are positioned at or inside of a pre-determined cylinder of the drive. The drive uses this signal to reduce the current flow through the heads while writing data. The other means of precomping is done by writing data either 12 nsec early or late when the heads are in the precomp area. The WD1010 continually puts out the signals EARLY* and LATE*, which are fed into U18 along with RWC. When RWC is active the PAL, U18, outputs a delayed and latched (by 2XDR) version of EARLY* and LATE* called EELD and LELD. When RWC is not active, the signal is not output by U18. These three signals are used as enables for U31 to pass one of three WDATA signals, which are separated 12 nsec by the delay line, through to the RS-422 driver, U4. The PAL output INDATA will be either RDATA or WDATA depending upon the signal WGATE.

5. Controller Alignment

The controller alignment should be done after any servicing to the board or drive components.

1. Move jumper plug from E6-E7 position to E7-E8 position. This feeds a 4 MHz clock into the read-data path so the drive does not have to be connected (but may be) at this time.

2. Adjust R3 until a high going pulse of 70-80 nsec is seen on the DLYDEATA signal. this signal is available on U26-37 or U7-11 for PP-2 boards or on test point 8 for rev A or later boards.

3. Adjust R2 until the DRUN signal just begins to toggle. DRUN may be found on U27-15 for rev A boards or on test point 7 for all other board revisions. This is only a preliminary adjustment and does not need to be exact at this time.

4. Replace jumper to position E6-E7 and be sure the primary drive is connected and powered on.

5. Adjust trim capacitor C11 until a 100 nsec square wave (10 MHz) signal is seen at TP 6 and the DC level of TP 3 is between 2 and 3 volts.

6. Using a diagnostic, such as HQII or HDREL, format track 1 (diagnostic track).

7. Next, do a continuous track read of the diagnostic track.

8. Set the scope for 2 msec sweep and trigger one channel on index (active high) at U19-6. Place the other channel on DRUN. You should see two index pulses spaced 16.67 msec apart.

9. Adjust R2 until you can define seventeen separate low pulses on DRUN between the two index marks. By adjusting R2 in both directions you can find the location where the pulses on DRUN are distinguished most clearly. The diagnostic should be incrementing the pass counter without error.

10. Next recheck the 10 MHz signal at TP 6 and the Vco reference at TP 3 and readjust C11, if needed for a stable setting.

11. If drive has a good format on it, execute random reads and check for proper operation.

12. If drive does not have a good format (ie. a new drive), format the entire drive and then execute a random read test.

6. Register specifications

The important controller ports will now be listed in greater detail. For more information on controller register functions and programming, see the WD1010 specification booklet.

1. C0 -- Write Protect Register
   This port is for read only use and only bits D7 and D6 should be looked at. A logic one in location D7 indicates the primary drive is write protected and a logic one in D6 indicates the secondary drive is write protected.

2. C1 -- Control Enable Register
   This port is a write/read register which enables certain functions of the controller board.

D0	Logic one enables dma operation
D1	Logic one enables interrupts
D2	Not used
D3 -- DEVEN	Logic one enables access to the WD1010
D4 -- SFTRST	Logic one triggers a 10 usec reset one-shot
D5	Not used
D6	Not used-must be written as 0
D7	Not used-must be written as 0

3. C8 -- Data Register
   Data to and from drive passes through this port.

4. C9
   Write -- This value in hex is the cylinder divided by 4 where write precompensation starts.

   Read -- This is the controller error register.

D0	Not used-forced to zero
D1	Logic one indicates track 0 was not located when expected
D2	Aborted command
D3	Not used-forced to zero

D4	ID not found-set to one if desired cylinder,head,sector, or size cannot be found after 8 disk revolutions or if a CRC error was encountered in the desired ID field
D5	Not used-forced to zero
D6	When set to one indicates a CRC error was encountered in a data field or if a data address mark was not found
D7	This bit is set when an ID field is encountered with a bad block mark used for bad sector mapping

5. CA -- Sector Count
This register contains the number of sectors to be transferred. It is used only when multiple sector reads or writes are used.

6. CD -- Sector Number
This register holds the number of the desired sector to be accessed during read or write sector commands. This must be loaded with the number of bytes to be used for gaps 1 and 3, during a format track command.

7. CC -- Cylinder LSB
Contains the LSB of the desired cylinder to be accessed.

8. CD -- Cylinder MSB
Contains the MSB of the desired cylinder to be accessed; only bits D0 and D1 may be used.

9. CD -- SDH register
This is loaded with the desired sector size, drive number, and head number parameters using the following form.

Bits 6 5	Sector Size
0 0	256
0 1	512
1 0	1024
1 1	128

Bits 4 3	Drive Select
0 0	Drive 0
0 1	Drive 1

Bits 2 1 0	Head Selected
0 0 0	HD 0
0 0 1	HD 1
0 1 0	HD 2
0 1 1	HD 3
1 0 0	HD 4
1 0 1	HD 5
1 1 0	HD 6
1 1 1	HD 7

Location D7 should be written as a zero always.

10. CF -- Command/Status
Write -- The desired command is loaded here, see the WD1010 manual for available commands.

Read -- Controller Status Register

D0	When set indicates an error has occurred; error register should then be checked.
D1	When set indicates a command is still in progress and no new command should be issued.
D2	Not used - forced to zero.
D3	This bit is set whenever the sector buffer should be written to or read from by the host, depending upon the command.
D4	This bit reflects the state of the seek complete line from the drive.
D5	This bit reflects the state of the write fault line from the drive.

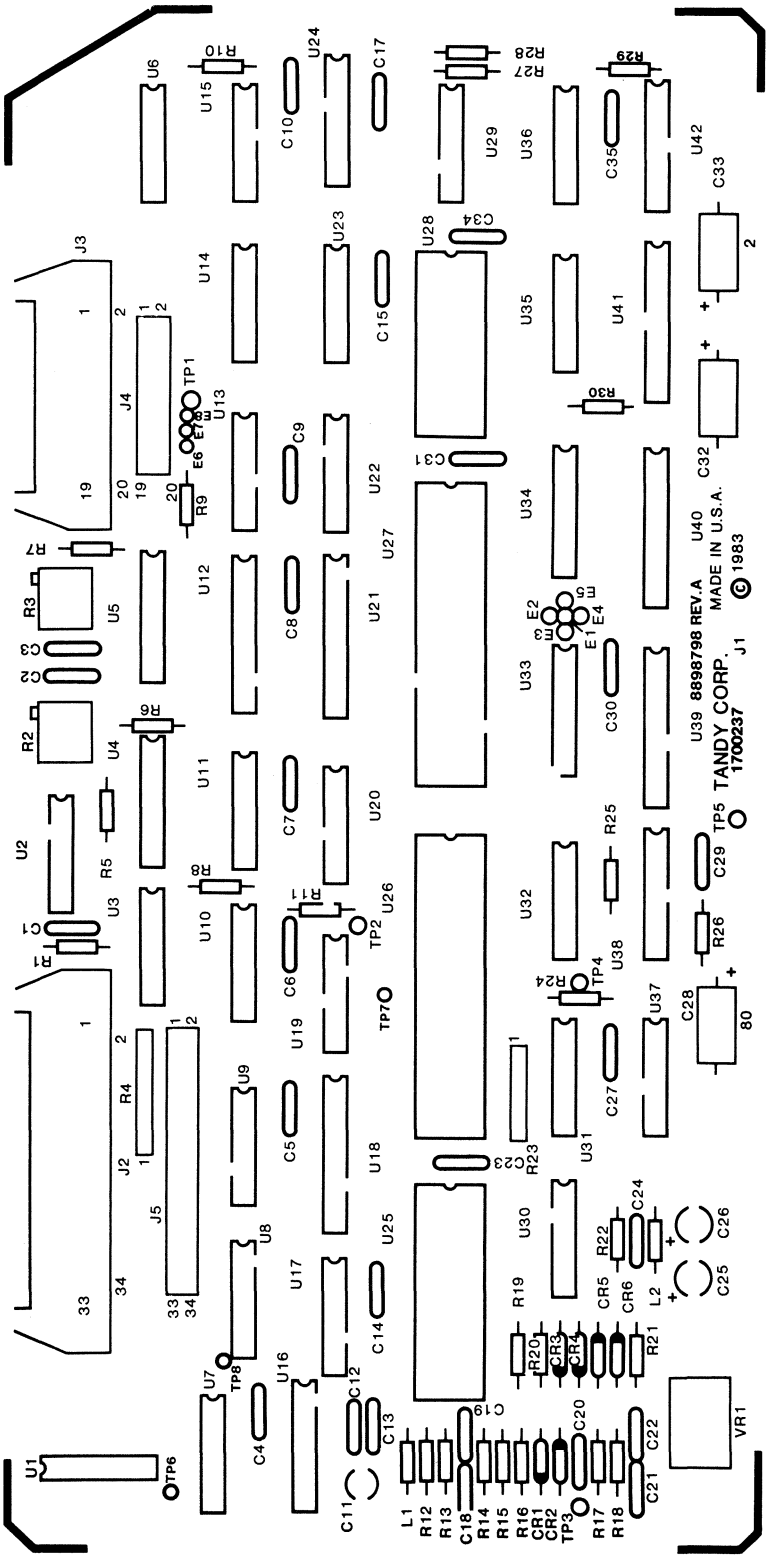
D6	This bit reflects the state of the ready line from the drive. Upon an interrupt for an error this bit is frozen until the status register is read.
D7	This bit is set whenever the WD1010 is busy accessing the drive or the sector buffer.

7.10.3 Hard Disk Drive

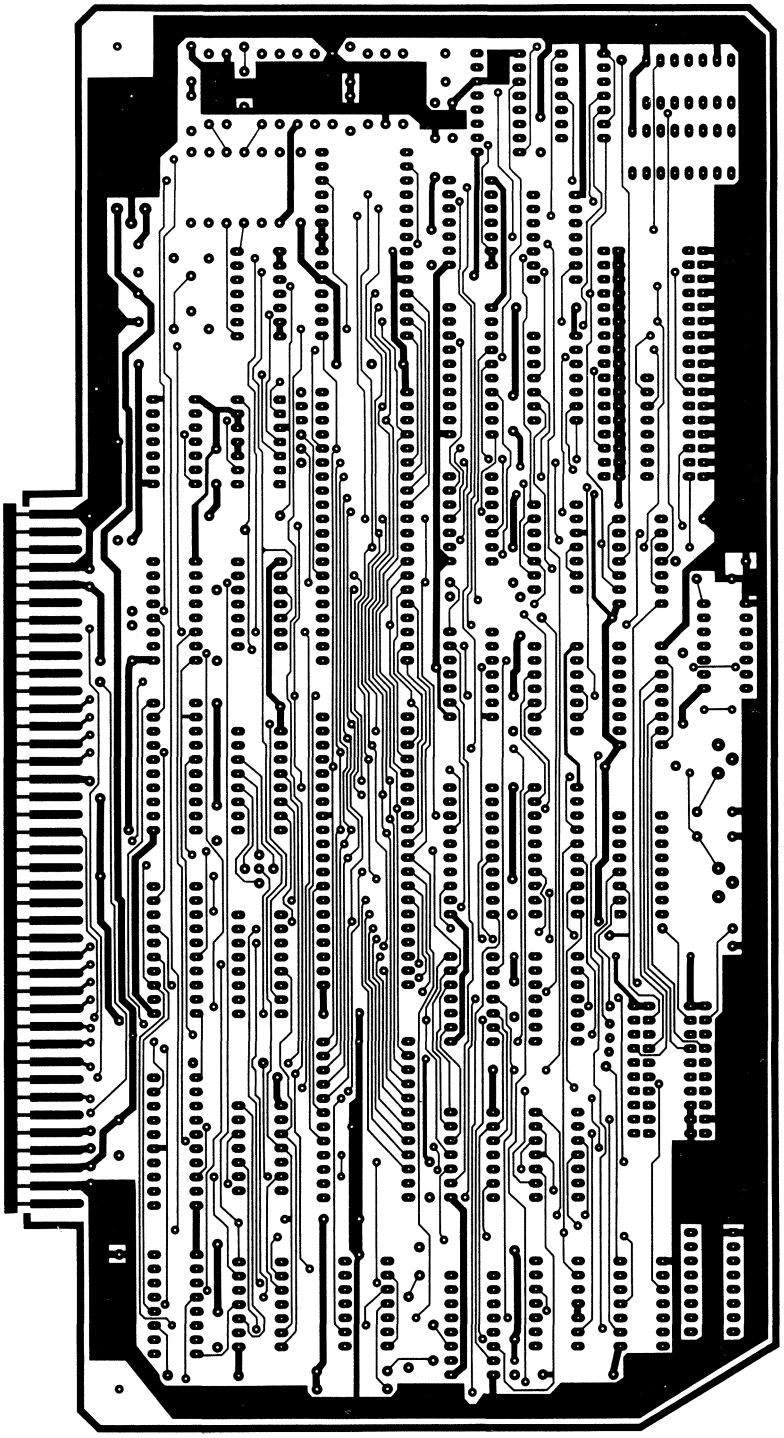
The hard disk that is installed in the Tandy 6000 is a 15-megabyte Tandon TM503. It has 3 5.25" Platters, each with 2 read/write surfaces for a total of 6 recording surfaces. Each surface has a dedicated read/write head attached to a common stepper arm mechanism. Each surface has a total of 306 cylinders giving a total track count of 1836. For more detailed information on this drive and its servicing, refer to the Tandon TM500-Series manual.

7.10.4 Hard Disk Power Supply

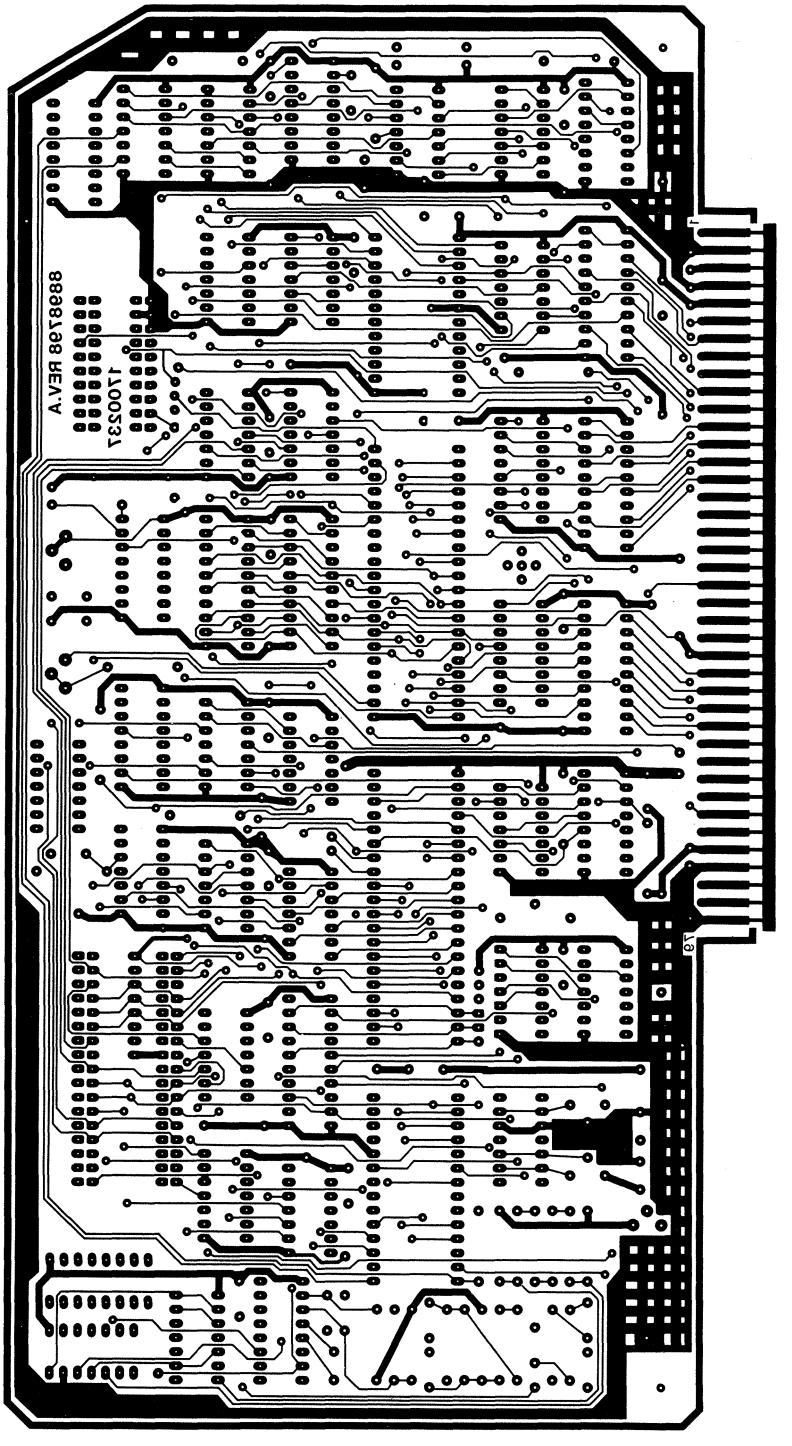
The power supply that is used to run the Tandon drive is a 38 watt Aztec switching power supply, Model Number AA 11330. This supply also powers a 12 volt DC ventilation fan located under the drive mounting tower. For service information of the power supply refer to the appropriate enclosed manual.



Component Layout, Hard Disk Controller 8898798 Rev. A



Circuit Trace, Hard Disk Controller 8898798 Rev. A, Component Side



Circuit Trace, Hard Disk Controller 8898798 Rev. A, Solder Side

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

Ref No.	Description	Part No.
Capacitors		
C1	Capacitor, 100 pF, 50V, C. Disk	8301104
C2	Capacitor, 100 pF, 50V, C. Disk, NPO	8301103
C3	Capacitor, 100 pF, 50V, C. Disk, NPO	8301103
C4	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C5	Not Used	
C6	Not Used	
C7	Not Used	
C8	Not Used	
C9	Not Used	
C10	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C11	Capacitor, 7-60 pF, Trim	8360607
C12	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C13	Not Used	
C14	Not Used	
C15	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C16	Not Used	
C17	Capacitor, 0.001 uF, 50V, C. Disk, 10%	8302104
C18	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C19	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C20	Capacitor, 330 pF, 50V, C. Disk, NPO	8301332
C21	Capacitor, 150 pF, 50V, C. Disk, NPO	8301153
C22	Capacitor, 0.0068 uF, 50V, C. Disk, 10%	8302684
C23	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C24	Capacitor, 0.1 uF, 50V, C. Disk, 10%	8304104
C25	Capacitor, 10 uF, 16V, Elect. Rad.	8326101
C26	Capacitor, 0.47 uF, 16V, Elect. Rad.	8324471
C27	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C28	Capacitor, 100 uF, 16V, Elect. Arial	8317101
C29	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C30	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C31	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C32	Capacitor, 100 uF, 16V, Elect. Arial	8317101
C33	Capacitor, 100 uF, 16V, Elect. Arial	8317101
C34	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
C35	Capacitor, 0.1 uF, 50V, Mono Axial	8374104
Connectors		
J2	Connector, 34-Pos. Shrouded Rgt. Ang.	8519196
J3	Connector, 20-Pos. Shrouded Rgt. Ang.	8519197
J4	Connector, 20-Pos. Straight Header	8519121
J5	Connector, 34-Pos. Straight Header	8519120

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

Ref No.	Description	Part No.
Diodes		
CR1	Diode, 1N4148	8150148
CR2	Diode, 1N4148	8150148
CR3	Diode, 1N4148	8150148
CR4	Diode, 1N4148	8150148
CR5	Diode, 1N4148	8150148
CR6	Diode, 1N4148	8150148
Resistors		
R1	Resistor, 560 ohm, 1/4W, 5%	8207156
R2	Pot., 10 kohm	8279312
R3	Pot., 10 kohm	8279312
R4	Res. Pak, 220/330 ohm	8290019
R5	Resistor, 470 ohm, 1/4W, 5%	8207147
R6	Resistor, 1 kohm, 1/4W, 5%	8207210
R7	Resistor, 100 ohm, 1/4W, 5%	8207110
R8	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R9	Resistor, 100 ohm, 1/4W, 5%	8207110
R10	Resistor, 1 kohm, 1/4W, 5%	8207210
R11	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R12	Resistor, 5.6 kohm, 1/4W, 5%	8207256
R13	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R14	Resistor, 2.43 kohm, 1/4W, 1%, MF	8200224
R15	Resistor, 200 ohm, 1/4W, 1%, MF	8200120
R16	Resistor, 2.43 kohm, 1/4W, 1%, MF	8200224
R17	Resistor, 680 ohm, 1/4W, 5%	8207168
R18	Resistor, 330 ohm, 1/4W, 5%	8207133
R19	Resistor, 1 kohm, 1/4W, 5%	8207210
R20	Resistor, 274 ohm, 1/4W, 1%, MF	8200427
R21	Resistor, 274 ohm, 1/4W, 1%, MF	8200427
R22	Resistor, 261 ohm, 1/4W, 1%, MF	8200126
R23	Res. Pak, 1 kohm, 6-Pin SIP	8290210
R24	Resistor, 1 kohm, 1/4W, 5%	8207210
R25	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R26	Resistor, 1 kohm, 1/4W, 5%	8207210
R27	Resistor, 16 kohm, 1/4W, 5%	8207316
R28	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R29	Resistor, 4.7 kohm, 1/4W, 5%	8207247
R30	Resistor, 22 ohm, 1/4W, 5%	8207022
Intergrated Circuits		
U1*	IC, 74F74, Dual Flip-Flop, 14-Pin	8015074
U2	IC, Osc., 20 MHz 14-Pin	8409029

* Note: 74S74 may be substituted for 74F74

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

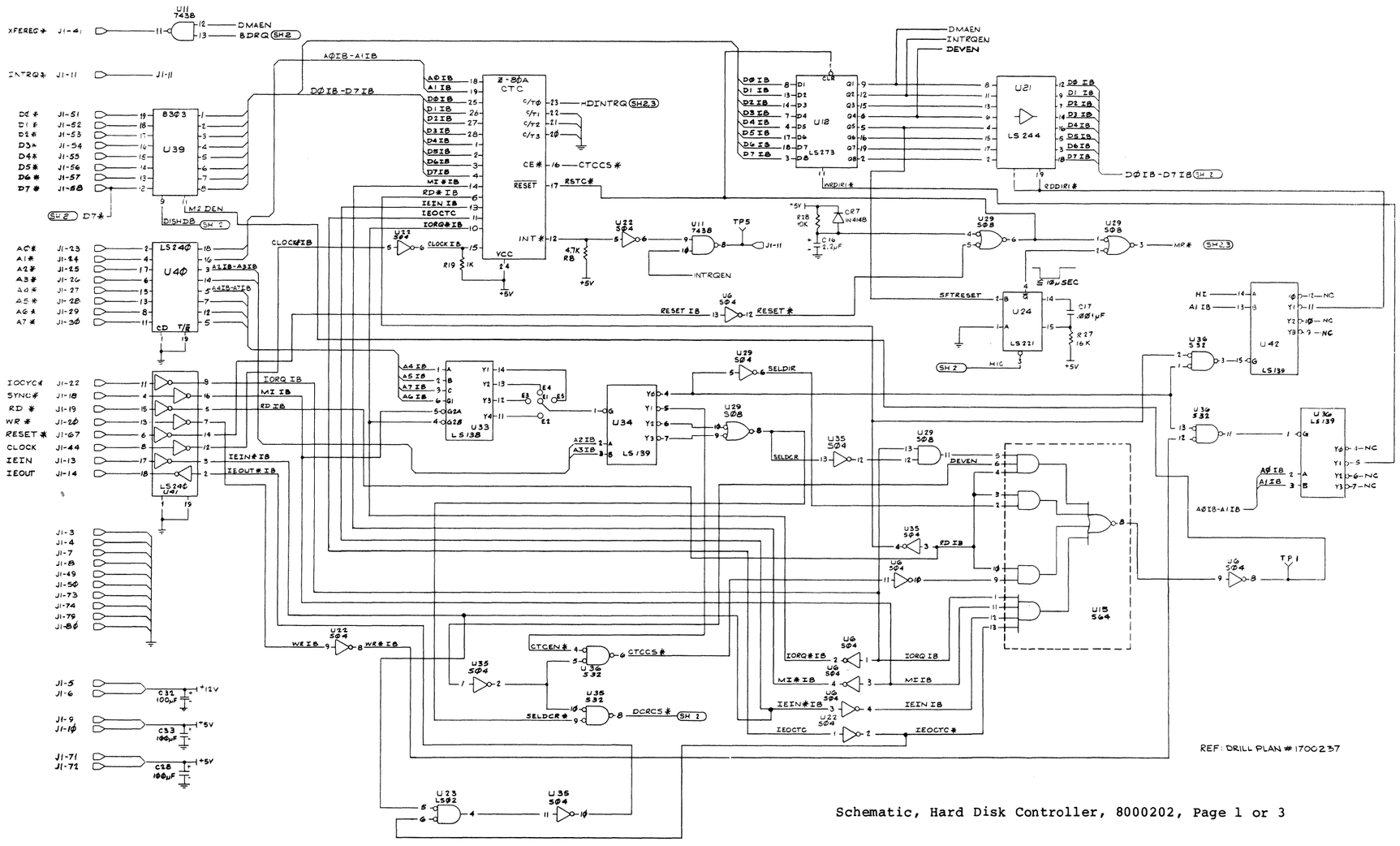
Ref No.	Description			Part No.
Integrated Circuits				
U3*	IC,	74F74, Dual Flip-Flop,	14-Pin	8015074
U4	IC,	MC3487, Line Driver,	16-Pin	8050487
U5	IC,	MC3486, Line Receiver,	16-Pin	8050486
U6	IC,	74S04, Hex Inverter,	14-Pin	8010004
U7*	IC,	74F74, Dual Flip-Flop,	14-Pin	8015074
U8	IC,	7407, Hex Buffer,	14-Pin	8000007
U9	IC,	7407, Hex Buffer,	14-Pin	8000007
U10	IC,	7438, Quad 2-IN NAND,	14-Pin	8000038
U11	IC,	7438, Quad 2-IN NAND,	14-Pin	8000038
U12	IC,	74LS273, Octal Flip-Flop,	20-Pin	8020273
U13	IC,	7416, Hex Inverter,	14-Pin	8000016
U14	IC,	74LS293, Binary Counter,	14-Pin	8020293
U15	IC,	74S64, AND OR Invert,	14-Pin	8010064
U16	IC,	74S124, Oscillator,	16-Pin	8010124
U17	IC,	74S00, Quad 2-IN NAND,	20-Pin	8010000
U19	IC,	74LS14, Hex Inverter,	14-Pin	8020014
U20	IC,	74LS04, Hex Inverter,	14-Pin	8020004
U21	IC,	74LS244, Octal Buffer,	20-Pin	8020244
U22	IC,	74LS04, Hex Inverter,	14-Pin	8020004
U23	IC,	74LS02, Quad 2-IN NOR,	14-Pin	8020002
U24	IC,	74LS221, Multivibrator,	16-Pin	8020221
U29	IC,	74S08, 2-IN AND,	14-Pin	8010008
U30	IC,	MPQ6700, Transistor Array,	14-Pin	8180700
U31	IC,	74S64, AND OR Invert,	14-Pin	8010064
U32	IC,	74LS02, Quad 2-IN NOR,	14-Pin	8020002
U33	IC,	74S138, Decoder,	16-Pin	8010138
U34	IC,	74S139, Decoder,	16-Pin	8010139
U35	IC,	74S04, Hex Inverter,	14-Pin	8010004
U36	IC,	74S32, Quad 2-IN OR,	14-Pin	8010032
U37	IC,	Delay Line (60 ns)		8429016
U38	IC,	74LS368, Hex Bus Driver	16-Pin	8020368
U39	IC,	AM8303, Bus Transceiver,	20-Pin	8060303
U40	IC,	74LS240, Octal Buffer,	20-Pin	8020240
U41	IC,	74LS240, Octal Buffer,	20-Pin	8020240
U42	IC,	74S139, Decoder,	16-Pin	8010139

* Note: 74S74 may be substituted for 74F74

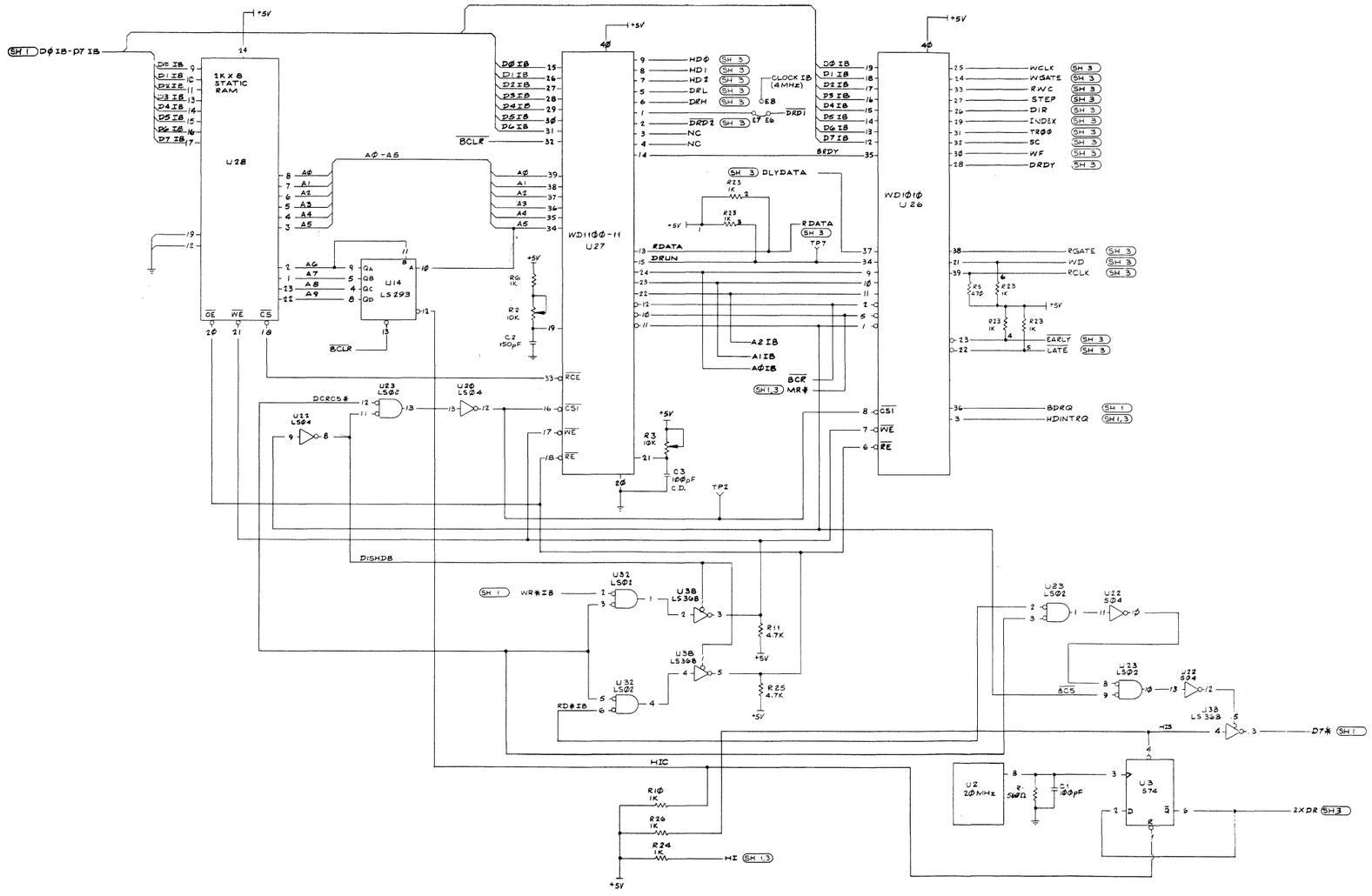
Sockets		
U18	Socket, 20-Pin DIP	8509009
U25	Socket, 28-Pin DIP	8509007
U26	Socket, 40-Pin DIP	8509002
U27	Socket, 40-Pin DIP	8509002
U28	Socket, 24-Pin DIP	8509001

Parts List, Hard Disk Controller PCB, 8898798 Rev. A

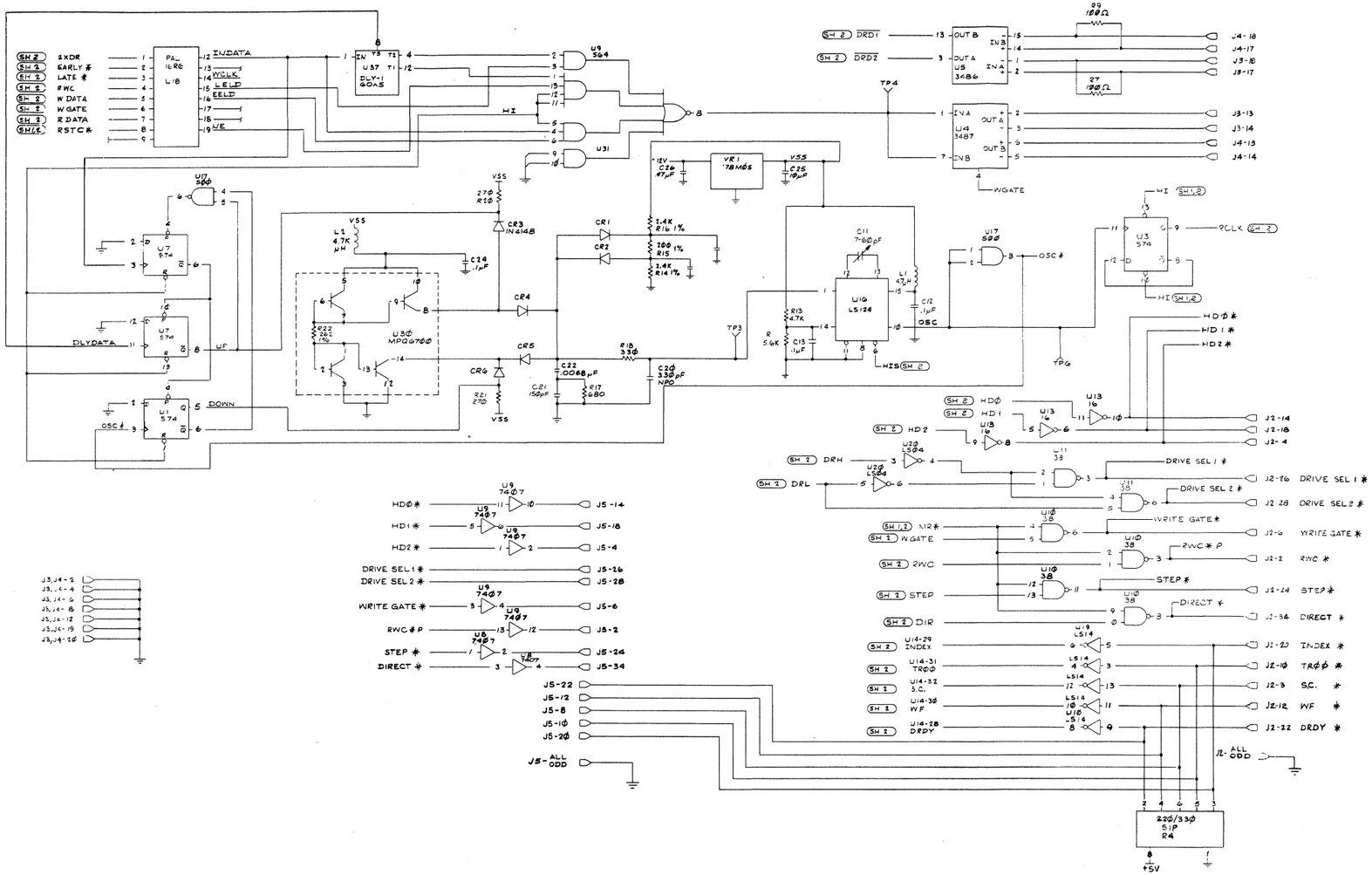
Ref No.	Description	Part No.
Staking Pins		
TP1	Staking Pin	8529014
TP2	Staking Pin	8529014
TP3	Staking Pin	8529014
TP4	Staking Pin	8529014
TP5	Staking Pin	8529014
TP6	Staking Pin	8529014
TP7	Staking Pin	8529014
E1	Staking Pin	8529014
E2	Staking Pin	8529014
E3	Staking Pin	8529014
E4	Staking Pin	8529014
E5	Staking Pin	8529014
E6	Staking Pin	8529014
E7	Staking Pin	8529014
E8	Staking Pin	8529014
Miscellaneous		
---	PCB Logic Board Rev.	8709474
L1	Inductor, 4.7 uH, 10%	8419017
L2	Inductor, 4.7 uH, 10%	8419017
VR1	Regulator, 78M05	8051805



Schematic, Hard Disk Controller, 8000202, Page 1 or 3



Schematic, Hard Disk Controller, 8000202, Page 2 or 3



Schematic, Hard Disk Controller, 8000202, Page 3 or 3

8/ Parts Lists/Exploded Views

Contained in this section are the parts lists and exploded views for the various subassemblies of the Tandy 6000/6000-HD. Some parts are noted but may not be available as individual items. Consult the factory for replacement part availability.

8.1 Base Assembly S/A 889CC11, Tandy 6000/6000-HD Computer

Item	Quan	Description	Part No.
1	1	Plug, Hole (Data Link)	8729125
2	1	Connector, Power Cord	8519207
3	6	Nut, KEPS Lock #4-40	8579003
4	1	Base, Computer	8719476
5	4	Feet, Bumpon	8590128
6	1	Cable, Keyboard	8709402
7	1	Power On Switch/ AC Harness	8709596
8	1	PCB, Sound	8898429
9	2	Screw, #6 x 3/8 Plastite	8569077
10	1	Deflector, Air	8729506
11	1	Fan, Rotron #WX2H1	8790417
12	1	Panel, Fan/Connector	8729516
13	1	Guard, Fan	8719452

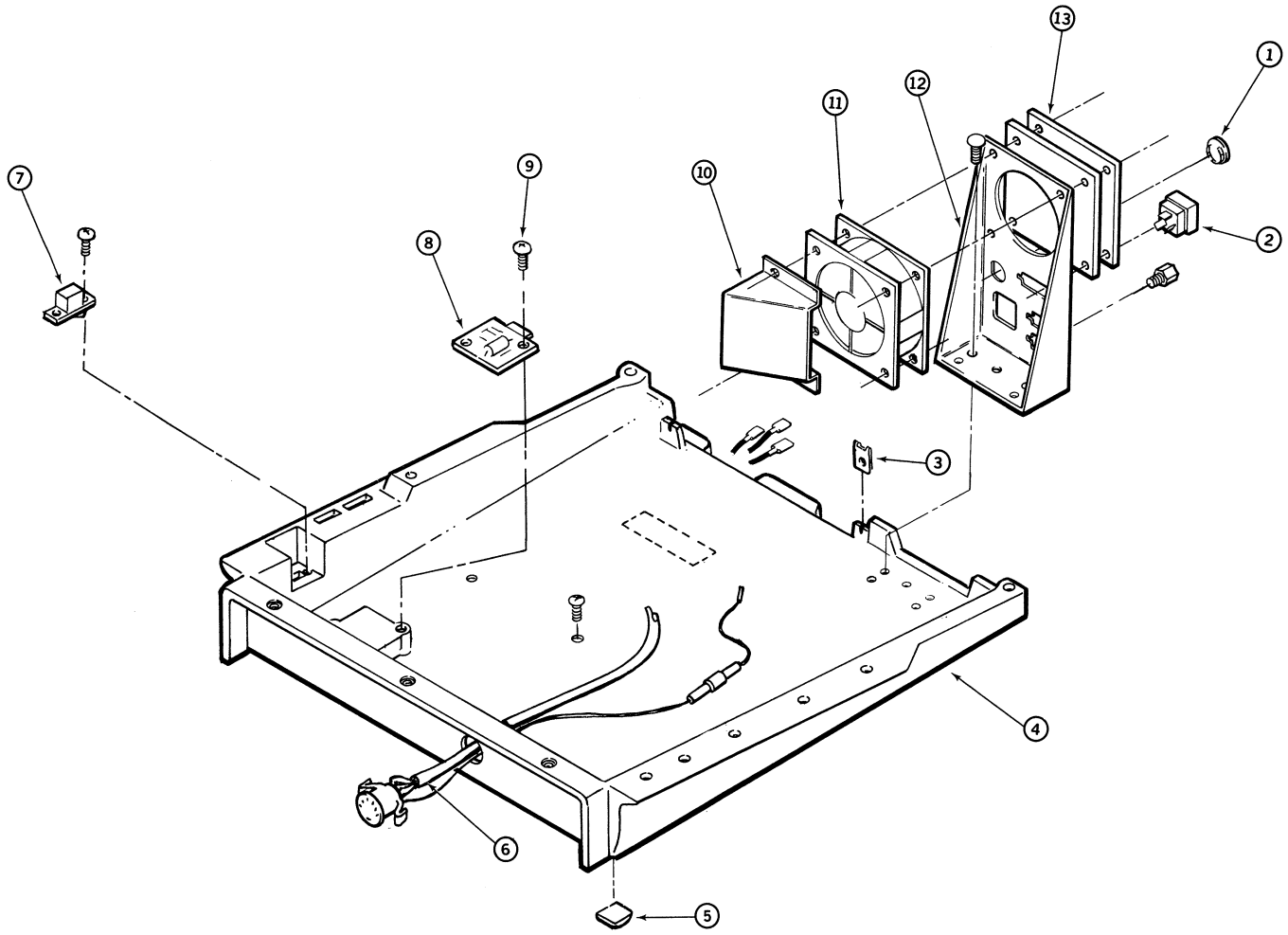


Figure 8-1. Exploded View, Base Assembly

8.2 Card Cage, Main Chassis, and Power Supply

Item	Quan	Description	Part No.
1	1	Panel, Right Card Cage	8729249
2	1	Cover, Card Cage	8729211
3	2	Strips 3/8" x 1/4" x 7"	8719482
4	1	Retainer, Card Cage	8719525
5	1	Panel, Left Card Cage	8729286
6	1	Motherboard	8897701
7	1	Main logic Board	8897702
8	1	Chassis, Main	8729142
9	1	Shield, Power Supply	8729207
10	2	Strain Relief	8559046
11	1	Insulator	
12	1	Power Supply	8790040
13	1	Cover, Power Supply	8729504
14	1	Fan, Rotron #SU2G1	8790410

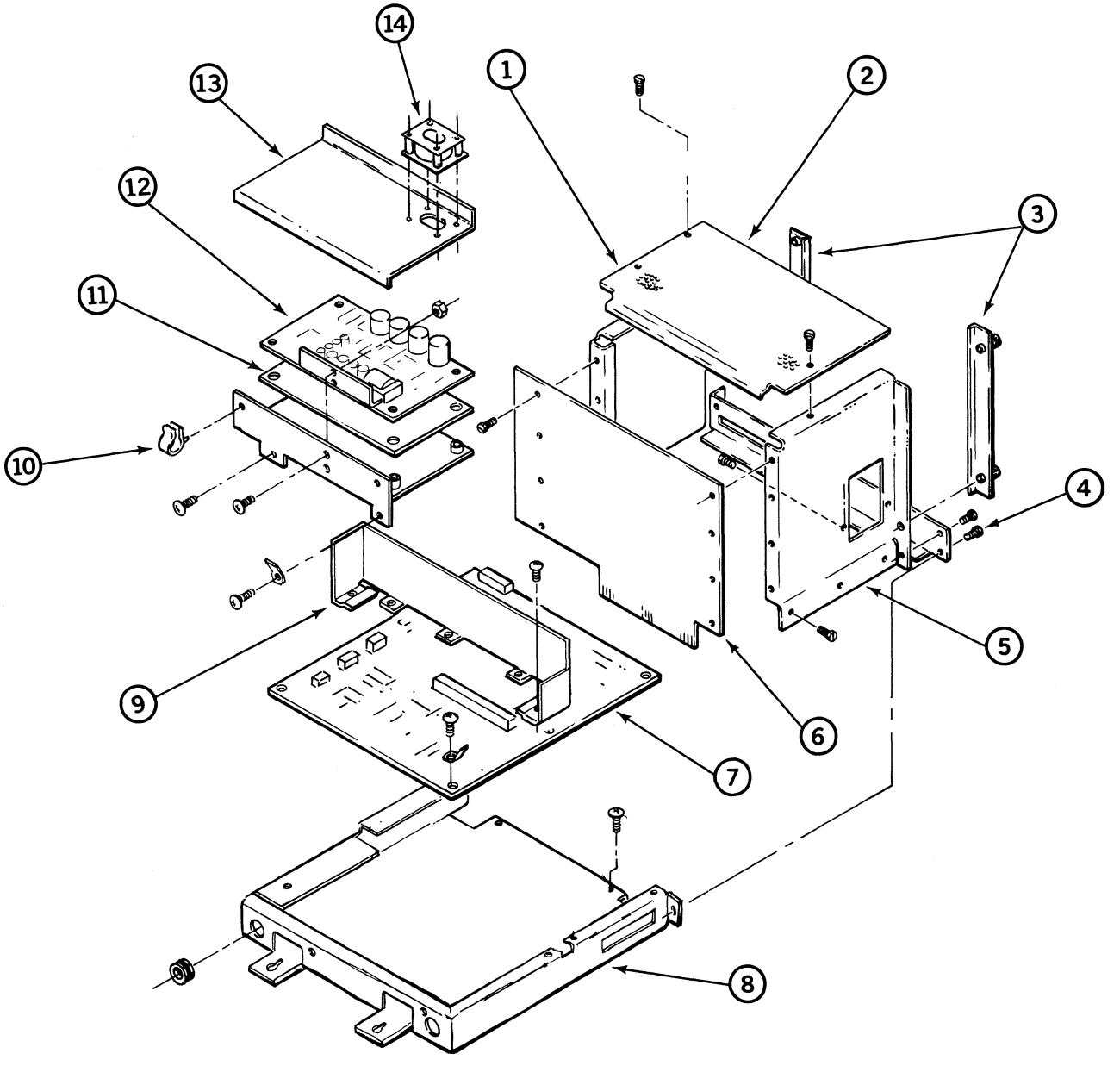


Figure 8-2. Exploded View, Card Cage, Main Chassis and Power Supply

8.3 Floppy Disk Drive

Item	Quan	Description	Part No.
1	1	Mount, Disk Drive	8729261
2	2	Disk Drive Assembly	8790123
3	1	Bar, Rear Mounting	8729262
4	1	Bar, Front Mounting	8729263
5	1	Lens, LED	8719294
6	1	Bezel, Drive	9719295

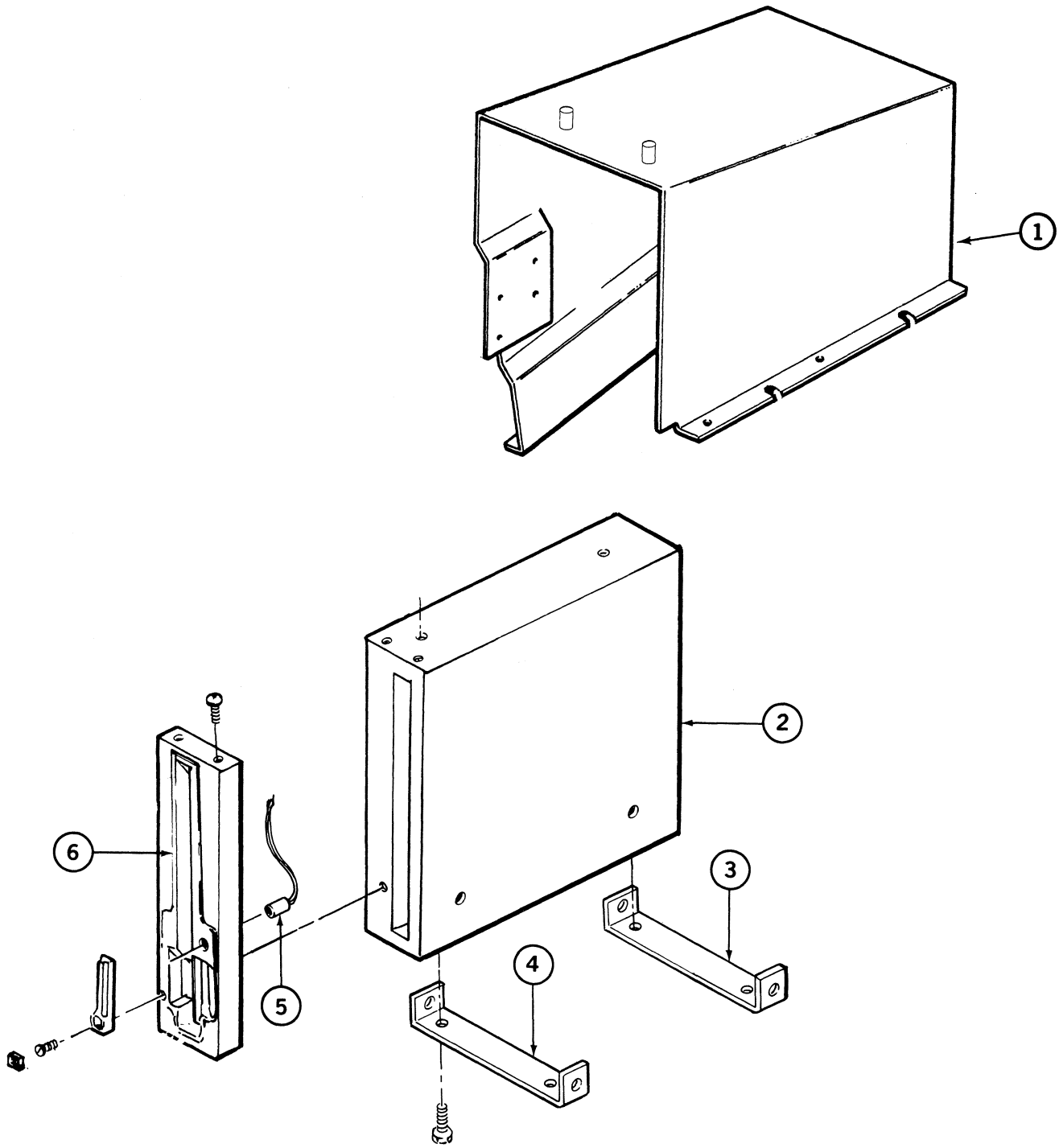


Figure 8-3. Exploded View, Floppy Disk Drive Assembly

8.4 Hard Disk Drive Assembly

Item	Quan	Description	Part No.
1	1	Cable Assembly, 34-Pin Connector	8709490
2	1	Cable Assembly, 20-Pin connector	8709489
3	1	Drive, Hard Disk	8790205
4	1	Mount, Disk Drive	8729261
5	2	Spacer, Plastic	8589097
6	1	Bar, Rear Mounting	8729262
7	1	Bar, Front Mounting	8729263
8	1	Bracket, Lower Hard Disk	8729259
9	5	Spacer, Antivibration	8589096
10	2	Wing Clips, Bezel Overlay	8559057
11	1	Bezel Overlay	8719397
12	1	Panel, Card Cage Left	8729286
13	1	Cable Assembly, AC	8709486
14	1	Terminal Block	8529045
15	1	Cover, Card Cage	8729211
16	1	PCB, Hard Disk Controller	889F005
17	1	Power Supply, 38W	8790025
18	1	Cable Assembly, DC Wiring	8709446
19	1	Bracket, Upper Hard Disk	8729260

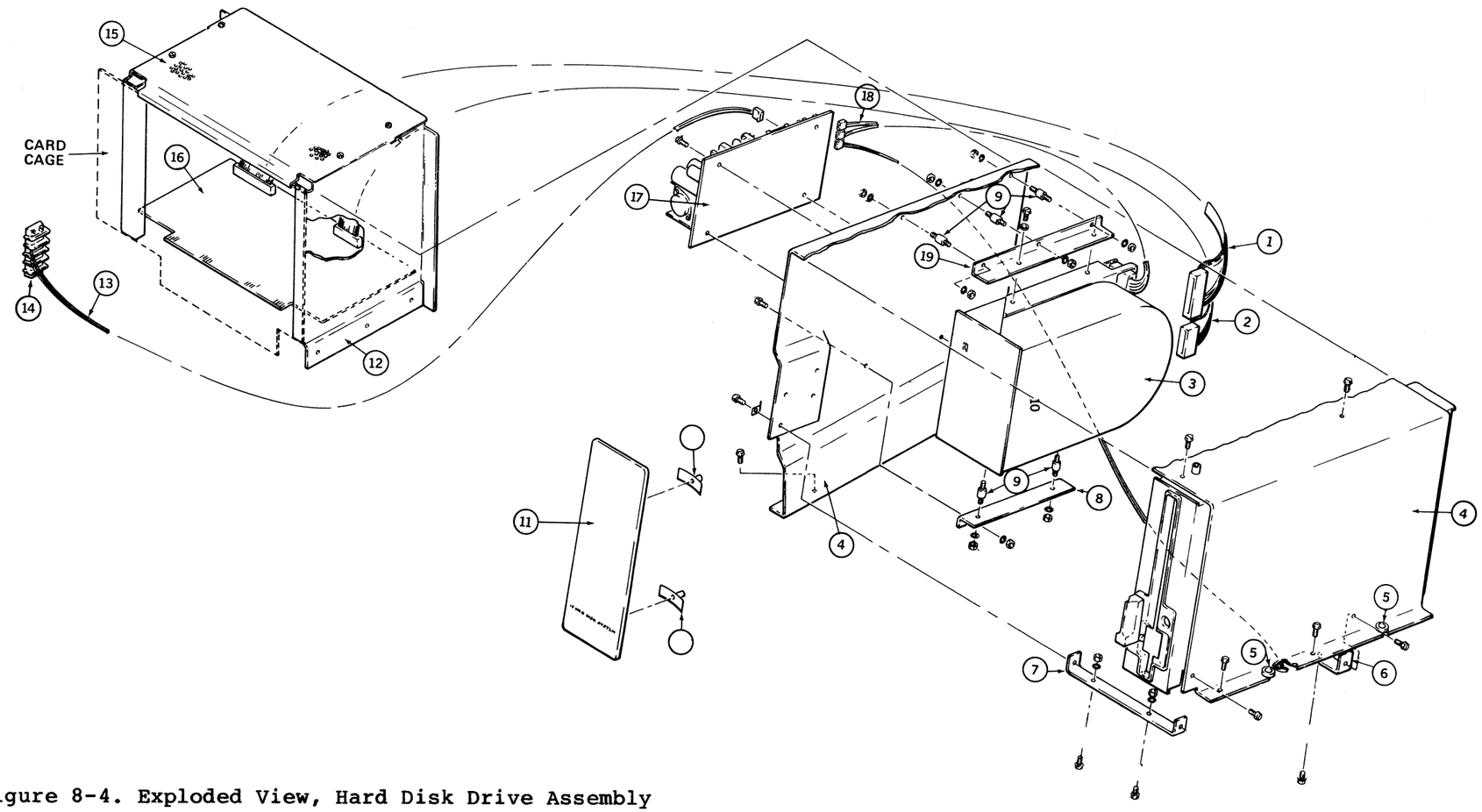


Figure 8-4. Exploded View, Hard Disk Drive Assembly

8.5 Bezel Assembly

Item	Quan	Description	Part No.
1	1	Stiffener, Bezel	8729515
2	1	Bezel, Front	8729261
3	1	Video PCB	8898018
4	1	Video Mount	8729517
5	1	CRT Assembly (TCE)	8790614
6	1	Contrast Control	8261150
7	1	Brightness Control	8262450

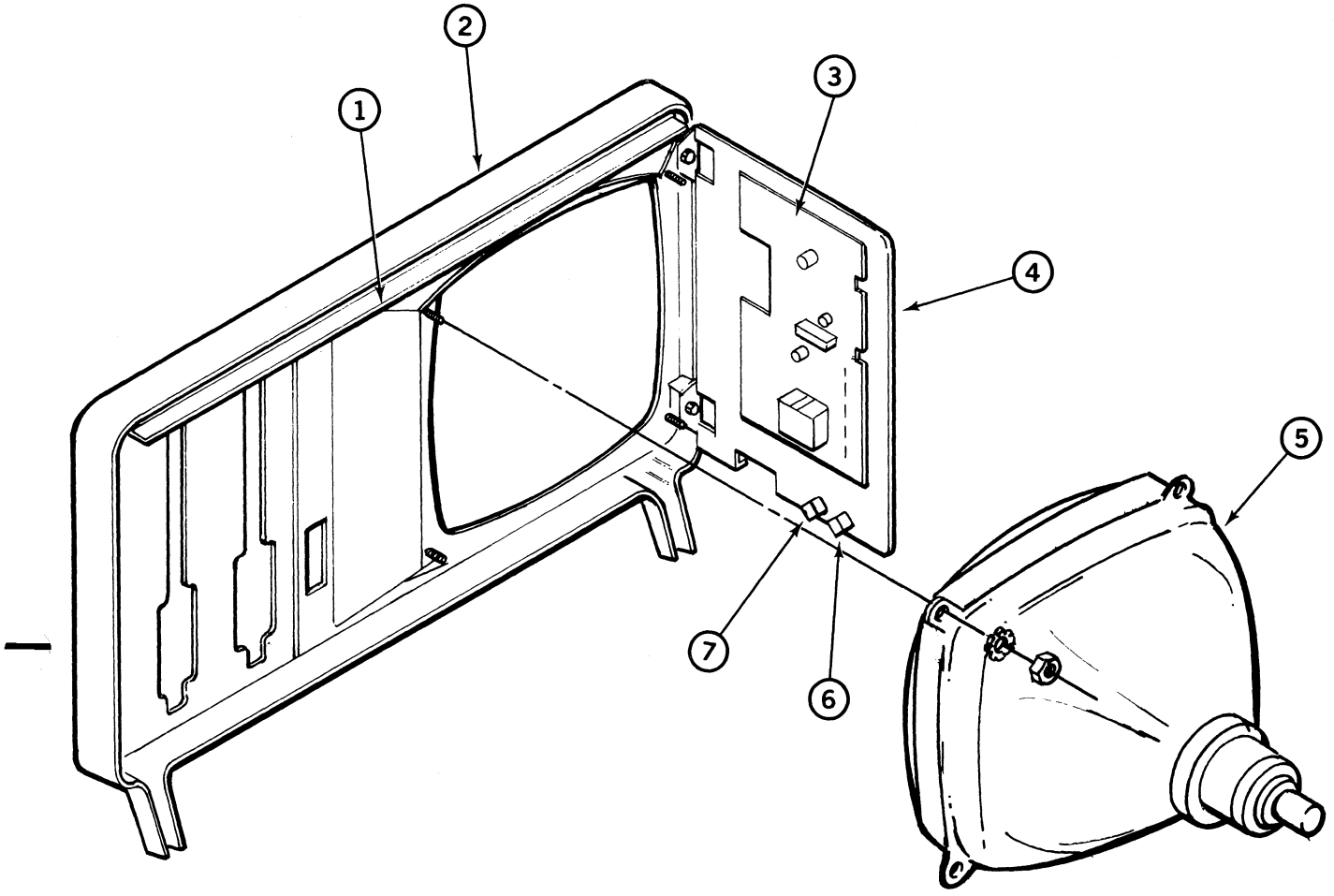


Figure 8-5. Exploded View, Bezel Assembly

8.6 Reset/Power On Indicator Module

Item	Quan	Description	Part No.
1	1	Indicator, Power On	8469011
2	1	Switch, Reset	8489055
3	1	Cable, Reset Switch	8709395

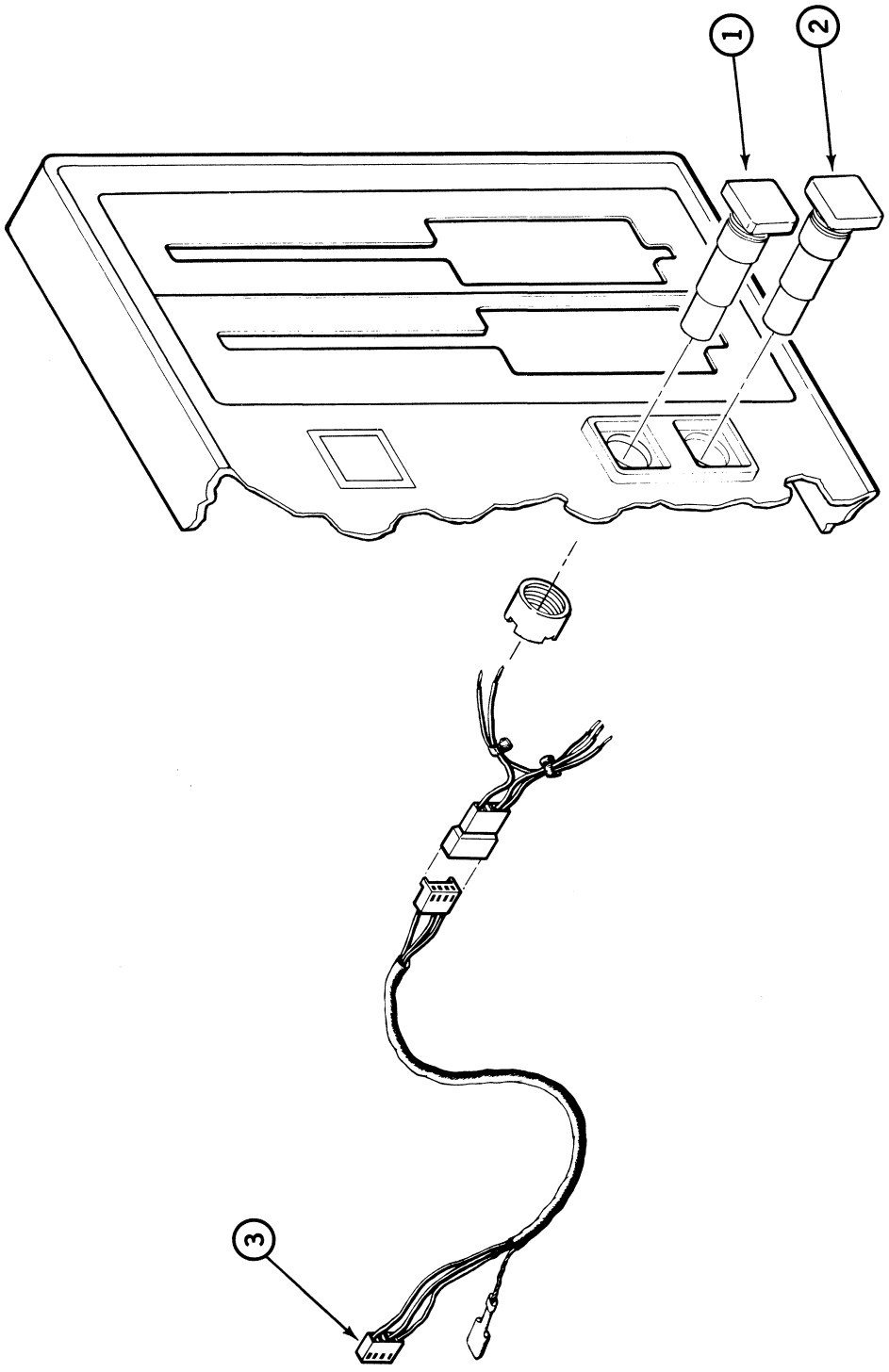


Figure 8-6. Exploded View, Reset/Power On Indicator Module

8.7 Case Top Assembly

Item	Quan	Description	Part No.
1	1	Case, Top	8719469
2	1	Spring, Bar	8729158
3	1	Door, Rear	8719248
4	2	Bracket, Strain Relief	8729194

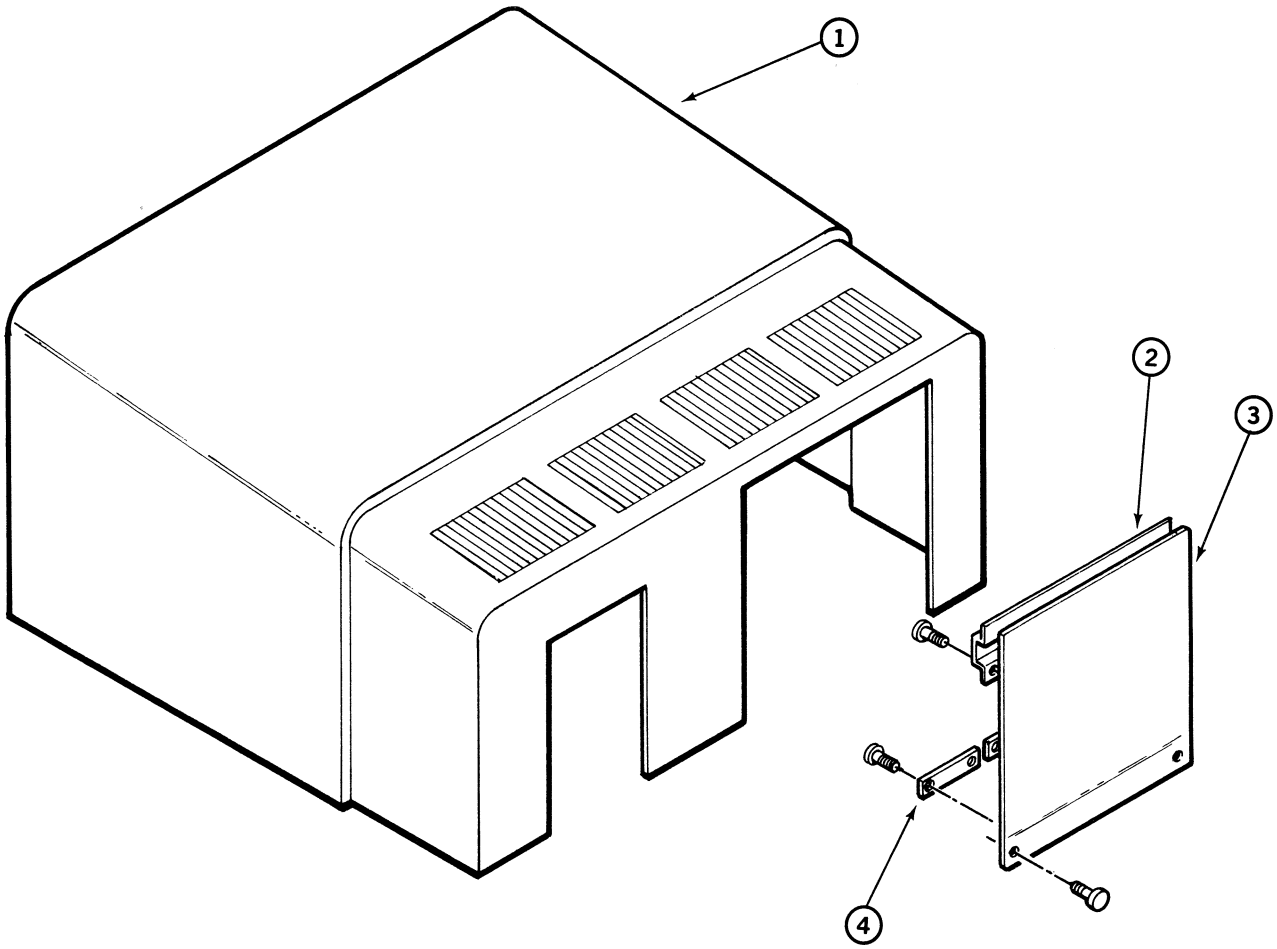


Figure 8-7. Exploded View, Case Top Assembly

8.8 Keyboard Assembly

Item	Quan	Description	Part No.
1	1	Nameplate, Keyboard	8729261
2	1	Cover, Keyboard	8719479
3	1	Bezel, Keyboard	8719467
4	1	Keyboard, Low Profile	8790554
5	1	Cable, Keyboard	8709396
6	1	Base, Keyboard	8719299
7	1	Bushing	8719156
8	4	Feet, Cork	8591001
9	1	Label, Keyboard	87891277

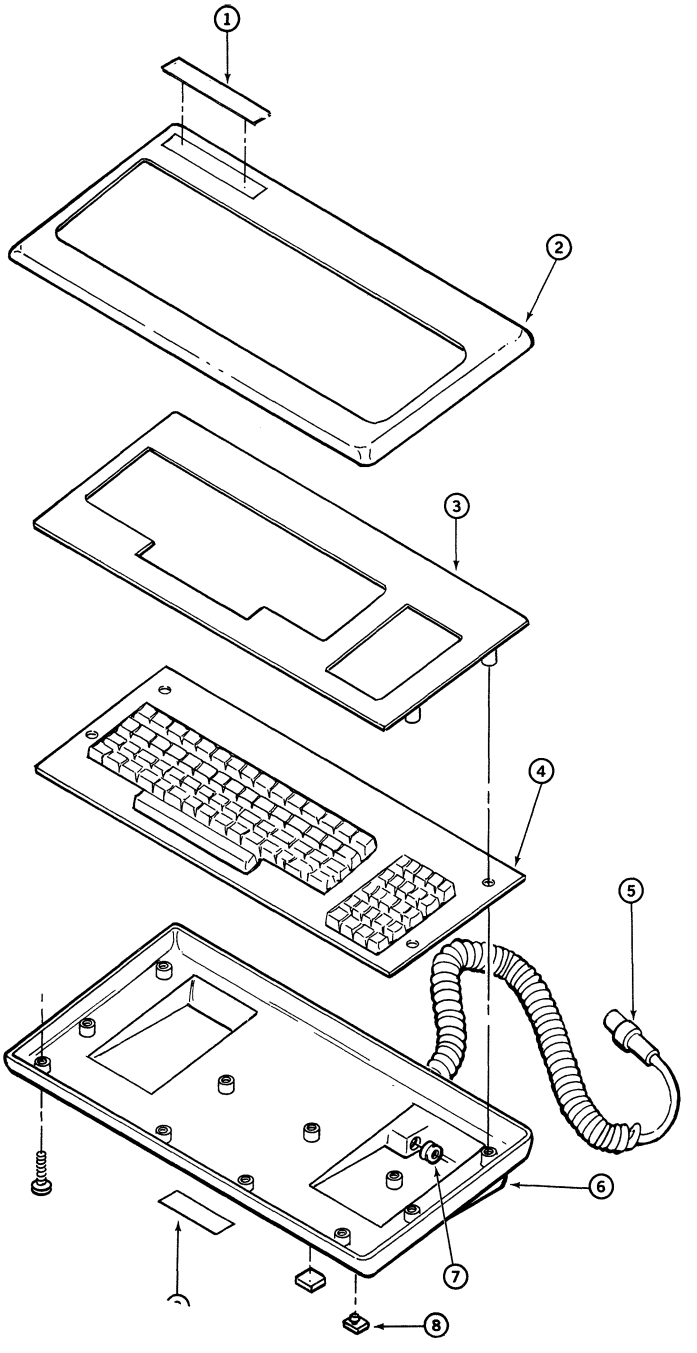


Figure 8-8. Exploded View, Keyboard Assembly

Appendices

Video Monitor Assembly 8790614 (TCE)

Ref. No.	Description	Part No.
Capacitors		
C101	Capacitor, 4.7 uF, 50V, 20%	CE04(RB)475M
C102	Capacitor, 180 pF, 50V, 10%	CK45B1H181K
C103	Capacitor, 0.1 uF, 50V, 10%	CQ92M1H104K
C104	Capacitor, 22 uF, 100V, 20%	CE04C226M
C105	Capacitor, 2200 pF, 500V,+100-0%	CK45E2H222P
C201	Capacitor, 0.022 uF, 50V, 10%	CQ92M1H223K
C202	Capacitor, 0.022 uF, 50V, 10%	CQ92M1H223K
C203	Capacitor, 0.01 uF, 50V, 10%	CQ92M1H103K
C204	Capacitor, 0.33 uF, 50V, 10%	CE04(RB)334K
C205	Capacitor, 4.7 uF, 35V, 20%	CS15E475M
C206	Capacitor, 4.7 uF, 35V, 20%	CS15E475M
C207	Capacitor, 33 uF, 16V, 20%	CE04C336M
C208	Capacitor, 33 uF, 16V, 20%	CE04C336M
C209	Capacitor, 1000 uF, 16V, 20%	CE04C108M
C210	Capacitor, 0.033 uF, 50V, 10%	CQ92M1H333K
C211	Capacitor, 220 uF, 16V, 20%	CE04C227M
C212	Capacitor, 100 uF, 16V, 20%	CE04C107M
C301	Capacitor, 220 pF, 50V, 10%	CK45B1H221K
C302	Capacitor, 0.47 F, 50V, 10%	CE04(RB)474K
C303	Capacitor, 56 pF, 50V, 10%	
C304	Capacitor, 0.022 uF, 50V, 10%	CQ92M1H223K
C305	Capacitor, 0.018 uF, 50V, 10%	CQ92M1H183K
C306	Capacitor, 0.018 uF, 50V, 10%	CQ92M1H183K
C307	Capacitor, 4.7 uF, 50V, 20%	CE04C475M
C308	Capacitor, 0.01 uF, 50V, 10%	CQ92M1H103K
C309	Capacitor, 220 uF, 16V, 20%	CE04C227M
C310	Capacitor, 27 pF, 50V, 5%	
C311	Capacitor, 4700 pF, 50V, 5%	CQ92P1H472J
C312	Not Used	
C313	Capacitor, 1000 uF, 25V, 20%	CE04C108M
C314	Capacitor, 0.033 uF, 400V, 5%	CQ92P2G333J
C315	Capacitor, 0.047 uF, 400V, 10%	CQ92P2G473K
C316	Capacitor, 1 uF, 250V, 20%	CE04C105M
C317	Capacitor, 0.01 uF, 630V, 10%	CQ92P2J103K
C318	Capacitor, 0.01 uF, 630V, 10%	CQ92P2J103K
C319	Capacitor, 4700 pF,1000V,+100-0%	CK45E3A472P
C320	Capacitor, 2200 pF, 500V,+100-0%	CK45E2H222P
C321	Capacitor, 2200 pF,1000V,+100-0%	CK45E3A222P
C322	Capacitor, 15 uF, 25V, 20%	CE04(RP)A01M
C323	Capacitor, 2200 pF, 500V,+100-0%	CK45E2H222P
C324	Capacitor, 2200 pF, 500V,+100-0%	CK45E2H222P

Video Monitor Assembly 8790614 (TCE)

Ref. No.	Description	Part No.
C401	Capacitor, 220 uF, 16V, 20%	CE04C227M
C501	Capacitor, 1000 pF,1000V,+100-0%	CK45E3A102P
Coils		
L301	Coil, Linearity	143410020A
L302	Coil, Width	143310140A
Diodes		
D101	Diode, Si 10E-1	----------
D201	Diode, Si 10E-1	----------
D202	Diode, Si VD1221	----------
D203	Diode, Si VD1221	----------
D301	Diode, Si RGP25D or MR852	----------
D302	Diode, Si BBT4 or IN4936	----------
D303	Diode, Si BBT4 or IN4936	----------
D304	Diode, Si BBT4 or IN4936	----------
D305	Diode, Si BBT10 or MR818	----------
D306	Diode, Si BBT4 or IN4936	----------
Fuses		
FU401	Fuse, 2A, 250V	251000790A
Integrated Circuits		
IC201	IC, AN5763, V-Process	----------
IC301	IC, AN5753, H-Process	----------
Resistors		
R101	Resistor, 470 ohms, 1/4W, 5%	RD1/4MZ(S)471J
R102	Resistor, 15k ohms, 1/4W, 5%	RD1/4MZ(S)153J
R103	Resistor, 1M ohms, 1/4W, 5%	RD1/4MZ(S)105J
R104	Resistor, 220 ohms, 1/4W, 5%	RD1/4MZ(S)221J
R105	Resistor, 33 ohms, 1/4W, 5%	RD1/4MZ(S)330J
R106	Resistor, 100 ohms, 1/4W, 5%	RD1/4MZ(S)101J
R107	Resistor, 47k ohms, 1/4W, 5%	RD1/4MZ(S)473J
R108	Resistor, 1k ohms, 1/4W, 5%	RD1/4MZ(S)102J
R109	Resistor, 1k ohms, 1/4W, 5%	RD1/4MZ(S)102J
R110	Resistor, 1.5k ohm, 3W, 5%	RSM3P1152J
R111	Resistor, 5.6k ohms	
R201	Resistor, 4.7k ohms, 1/4W, 5%	RD1/4MZ(S)472J
R202	Resistor, 4.7k ohms, 1/4W, 5%	RD1/4MZ(S)472J
R203	Resistor, 100 ohms, 1/4W, 5%	RD1/4MZ(S)101J
R204	Resistor, 56k ohms, 1/4W, 5%	RD1/4MZ(S)563J

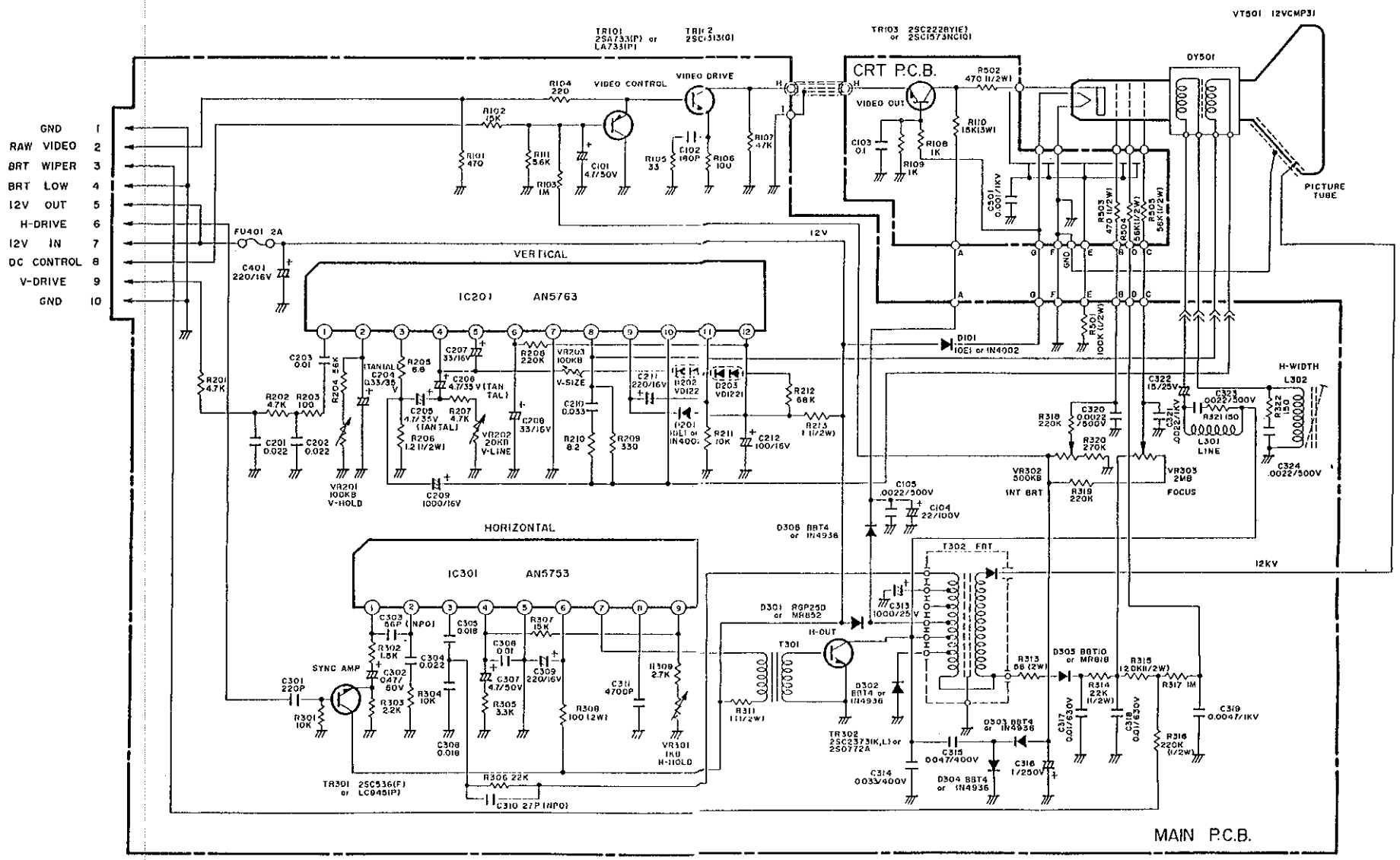
Video Monitor Assembly 8790614 (TCE)

Ref. No.	Description,	Part No.
R205	Resistor, 6.8 ohms, 1/4W, 5%	RD1/4MZ(S)6R8J
R206	Resistor, 1.2 ohms, 1/2W, 5%	
R207	Resistor, 4.7k ohms, 1/4W, 5%	RD1/4MZ(S)472J
R208	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)224J
R209	Resistor, 330 ohms, 1/4W, 5%	RD1/4MZ(S)331J
R210	Resistor, 8.2 ohms, 1/4W, 5%	RD1/4MZ(S)8R2J
R211	Resistor, 10k ohms, 1/4W, 5%	RD1/4MZ(S)103J
R212	Resistor, 68k ohms, 1/4W, 5%	
R213	Resistor, 1 ohm, 1/2W, 5%	RD1/4MZ(S)6R8J
R301	Resistor, 10k ohms, 1/4W, 5%	RD1/4MZ(S)103J
R302	Resistor, 1.5 ohms, 1/4W, 5%	
R303	Resistor, 2.2k ohms, 1/4W, 5%	RDI/4MZ(S)222J
R304	Resistor, 10k ohms, 1/4W, 5%	RDI/4MZ(S)103J
R305	Resistor, 3.3k ohms, 1/4W, 5%	RDI/4MZ(S)332J
R306	Resistor, 22k ohms, 1/4W, 5%	RDI/4MZ(S)223J
R307	Resistor, 15k ohms, 1/4W, 5%	RDI/4MZ(S)153J
R308	Resistor, 100 ohms, 2W, 5%	RSM2P 560J
R309	Resistor, 2.7k ohms, 1/4W, 5%	RD1/4MZ(S)272J
R310	Not Used	
R311	Resistor, 1 ohm, 1/2W, 5%	RD1/2MZ(S)1R0J
R313	Resistor, 56 ohms, 2W, 5%	RSM2P 560J
R314	Resistor, 22k ohms, 1/2W	
R315	Resistor, 120k ohms, 1/2	
R316	Resistor, 220k ohms, 1/2W, 5%	RD1/2MZ(S)224J
R317	Resistor, 1M ohms, 1/4W, 5%	RD1/4MZ(S)105J
R318	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)24J
R319	Resistor, 220k ohms, 1/4W, 5%	RDI/4MZ(S)224J
R320	Resistor, 270k ohms	
R321	Resistor, 150 ohms, 1/4W, 5%	RD1/4MZ(S)151J
R322	Resistor, 150 ohms, 1/4W, 5%	RD1/4MZ(S)151J
R323	Not Used	
R324	Not Used	
R325	Not Used	
R326	Not Used	
R327	Not Used	
R328	Not Used	
R329	Resistor, 220k ohms, 1/4W, 5%	RD1/4MZ(S)24J
R501	Resistor, 100k ohms, 1/2W,10%	RC1/2GF104K
R502	Resistor, 470 ohms, 1/2W,10%	RC1/2GF471K
R503	Resistor, 470 ohms, 1/2W,10%	RC1/2GF471K
R504	Resistor, 56k ohms, 1/2W, 5%	RC1/2GF563K
R505	Resistor, 56k ohms, 1/2W, 5%	RC1/2GF563K

Video Monitor Assembly 8790608 (TCE)

Ref. No.	Description,	Part No.
Variable Resistors		
VR201	Variable Resistor, 100k ohms	176910730A
VR202	Variable Resistor, 20k ohms	176910710A
VR203	Variable Resistor, 100k ohms	176910730A
VR301	Variable Resistor, 1k ohms	176910670A
VR302	Variable Resistor, 500k ohms	176910750A
VR303	Variable Resistor, 2M ohms	176910640A
Transformers		
T301	Transformers, Drive	10851001MA
T301	Transformers, Flyback	10801003YA
Transistors		
TR101	Transistor, PNP, 2SA733(P) or	--------
	LA733(P)	--------
TR102	Transistor, NPN, 2SC1313(G)	--------
TR103	Transistor, NPN, 2SC228Y(E) or	
	2SC1573NC (Q)	--------

TR301	Transistor, NPN, 2SC536(F) or	
	LC945(P)	
TR302	Transistor, NPN, 2SC2373(K,L) or	
	2SD772A	
Miscellaneous		
VT501	Cathode Ray Tube	559010030A
VT501	Deflection Yoke	581510020A
	Clip, Fuse	197303080A
	Connector, 4-Pin	194110780A
	Socket, 4-Pin	194010370A
	Sockey, Cylindrical	196310010A
	Spring Tension, Ground Wire	434010020A
	Wire Ground, (Code Terminal)	316010110A



NOTE (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" (K=10^3 OHM, M=10^6 OHM)
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10^6 μF)

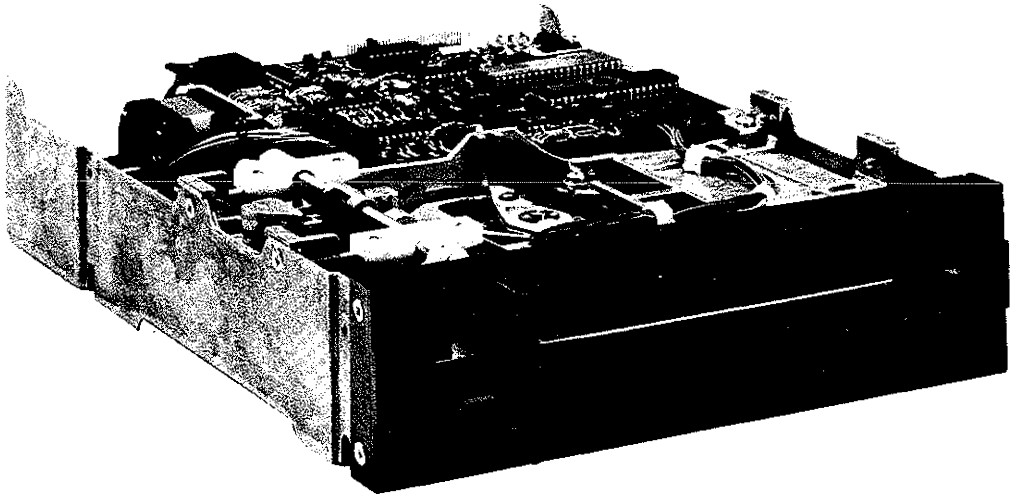
ISSUED FEB 13 1985 T.E.JAPAN

Revised on May 16, 1983

APPROVED BY	TITLE	
CHECKED BY	SCHEMATIC DIAGRAM	
DESIGNED BY	MODEL: VIDEO MONITOR 8790614	DRAWING NO.: D-23505C

OEM

OPERATING AND SERVICE MANUAL
TM848-1E AND TM848-2E
THINLINE™ FLEXIBLE DISK DRIVES
48 TRACKS PER INCH



Tandon CORPORATION
20320 PRAIRIE STREET
CHATSWORTH, CALIFORNIA 91311

NOTICE

This document is intended to provide the user with detailed information adequate for the efficient installation, operation, and service of the equipment involved.

However, while every effort has been made to keep the information contained herein current and accurate as of the date of publication, no guarantee is given or implied as to its accuracy.

CONTENTS

ILLUSTRATIONS

FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This document provides required information in order to evaluate or incorporate Tandon's disk drive into a system.

Tandon Corporation's Model Numbers TM848-1E and TM848-2E, eight-inch flexible drives are full-feature, microprocessor-controlled drives. They may be installed in one-half the space normally required for an eight-inch drive. They are compact data storage devices that use an IBM-formatted, industry standard, eight-inch diskette. Both drives are 48 tracks per inch recording devices.

The Model TM848 series of drives are capable of reading and writing in single-density format on a diskette, using a proprietary read/write head patented by Tandon. In addition, both drives have a double density capability when Modified Frequency Modulation (MFM) or other appropriate recording techniques are used. The encoding and decoding of the data is done by the user's controller. The Model TM848-1E drive uses one side of the diskette for data storage. The Model TM848-2E drive doubles data storage capabilities by using both sides of the diskette.

1.1 SCOPE OF THE DOCUMENT

This document contains a description of the major features, physical and functional specifications, mounting and power requirements, the interface, and typical timing characteristics of the TM848-1E and TM848-2E drives. In addition, there is a theory of operation, checks and adjustment procedures, troubleshooting guide, replacement procedures, assembly drawings and schematics.

1.2 PURPOSE OF THE DRIVE

The TM848-1E and TM848-2E drives are rotating disk memories designed for random access data entry, storage, and retrieval applications. Typical applications include intelligent terminal controllers, microcomputers, word processing systems, data communication systems, error logging, program loading, and point-of-sale terminals.

1.3 MAJOR FEATURES

MICROPROCESSOR CONTROL

The TM848-1E and TM848-2E drives feature an onboard microprocessor providing six major features:

1. Buffered seek capabilities.
2. Improved head positioning accuracy with reduced hysteresis.
3. Write current switching for optimal data recording quality.
4. True Ready signal.
5. Internal diagnostics (strappable).
6. Power on self-tests.

WRITE PROTECT

When a write protected diskette is inserted into the drive, the write electronics are disabled.

DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

INTERNAL TRIM ERASE

The drive provides the control signals necessary for proper trim erasure of data.

INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an industry standard interface.

ACTIVITY INDICATOR

An activity indicator, located on the front panel, is automatically illuminated when the drive is selected. This front panel L.E.D. is also used as an indicator in the diagnostic mode.

DIRECT DRIVE, BRUSHLESS D. C. MOTOR

The spindle motor is a crystal controlled, direct drive, brushless D. C. motor for improved motor start time, and speed accuracy.

COMPACT SIZE

The reduced size of the drive occupies only one-half the mounting space required for a conventional drive.

DISKETTE LEVER LOCK SOLENOID (OPTIONAL)

The diskette lever lock solenoid is controlled by the host system.

1.4 FUNCTIONAL DESCRIPTION

The drives are fully self-contained, and require no operator intervention during normal operation. Each drive consists of a direct drive, spindle system, a head positioning system, and a read/write system.

The TM848-1E is a single-sided drive. The TM848-2E is a double-sided drive. The only difference between the two drives is the number of heads. The circuit board is identical for both models.

When the diskette lever is opened, access is provided for the insertion of a diskette. The diskette's jacket is accurately positioned by plastic guide rails. Its location is ensured by the back stop and disk ejector.

Closing the diskette lever activates the cone/clamp system, resulting in accurate centering and clamping of the diskette to the drive hub. The drive hub is driven at a constant speed of 360 RPM by a crystal-controlled, direct drive, brushless D. C. motor. The head is loaded into contact with the recording medium whenever the diskette lever is latched.

The heads are positioned over the desired track by means of a stepper motor/band assembly and its associated electronics. This positioner uses a 3.6 degree rotation to cause a one track linear movement.

When a write-protected diskette is inserted into the drive, the Write Protect sensor disables the write electronics of the drive, and a Write Protect status output signal is available to the interface. When performing a write operation, a 0.013-inch wide, nominal, data track is recorded. Then, this track is tunnel erased to 0.012-inch, nominal.

Data recovery electronics include a low-level read amplifier, filter, differentiator, zero crossover detector, and digitizing circuits. No data-clock separation is provided.

In addition, the drive is supplied with the following sensor systems:

1. A Track 0 sensor detects when the Head/Carriage Assembly is positioned over Track 0.

2. The TM848-2E has two index sensors, each consisting of an infrared L.E.D. light source and a phototransistor, positioned to generate a signal when an index hole on the diskette is detected. The drive can determine if a single-sided or double-sided diskette is installed. This output signal is present at the interface.

3. A Write Protect sensor disables the write electronics when a write-enable tab is removed from the diskette.

SELF-TESTS

The drive conducts a power on self-test as part of the normal power on sequence. The two power on tests do not require a diskette to be inserted. These tests are: the head carriage stepping in (away from Track 0), and the head carriage stepping out (toward Track 0). Failure of either of these tests is indicated on the front panel L.E.D. by the following flashing sequence:

3 flashes, then 2: Fails to step in from Track 0 or Track 0 sensor is always equal to zero.

3 flashes, then 3: Fails to step out to Track 0 or Track 0 sensor is always equal to one.

A third test monitors the index sensors whenever the diskette lever is closed. A diskette must be inserted into the drive for this test. If the diskette lever is closed without a diskette in place, or the spindle motor fails to operate, an error message flashes on the front panel L.E.D. in the following sequence:

3 flashes, then 4: No index pulse with lever closed.

Opening and closing the diskette lever is required to repeat a test that has failed. The diskette lever must be left open for one complete error message cycle.

1.5 PHYSICAL DESCRIPTION

A representative drive is shown in Figure 1-1. The drive can be mounted in a vertical or horizontal plane. However, the logic circuit board must be on the uppermost side when the drive is mounted horizontally.

The spindle is rotated by a direct drive, brushless D. C. motor with an integral tachometer. The crystal-controlled servo circuit and tachometer control the speed of the spindle.

Operator access for diskette loading is provided via a horizontal slot located at the front of the drive.

The read/write double-head assembly is positioned by a split band positioner mounted to a microprocessor-controlled stepper motor. The read/write heads are glass-bonded, ferrite/ceramic structures with a life expectancy of 15,000 operating hours.

The control electronics of the drive are mounted on a printed circuit board located above the chassis. Power and interface signals are routed through connectors plugging directly into the logic circuit board. A second circuit board, mounted under the drive, operates the brushless D.C. spindle motor.

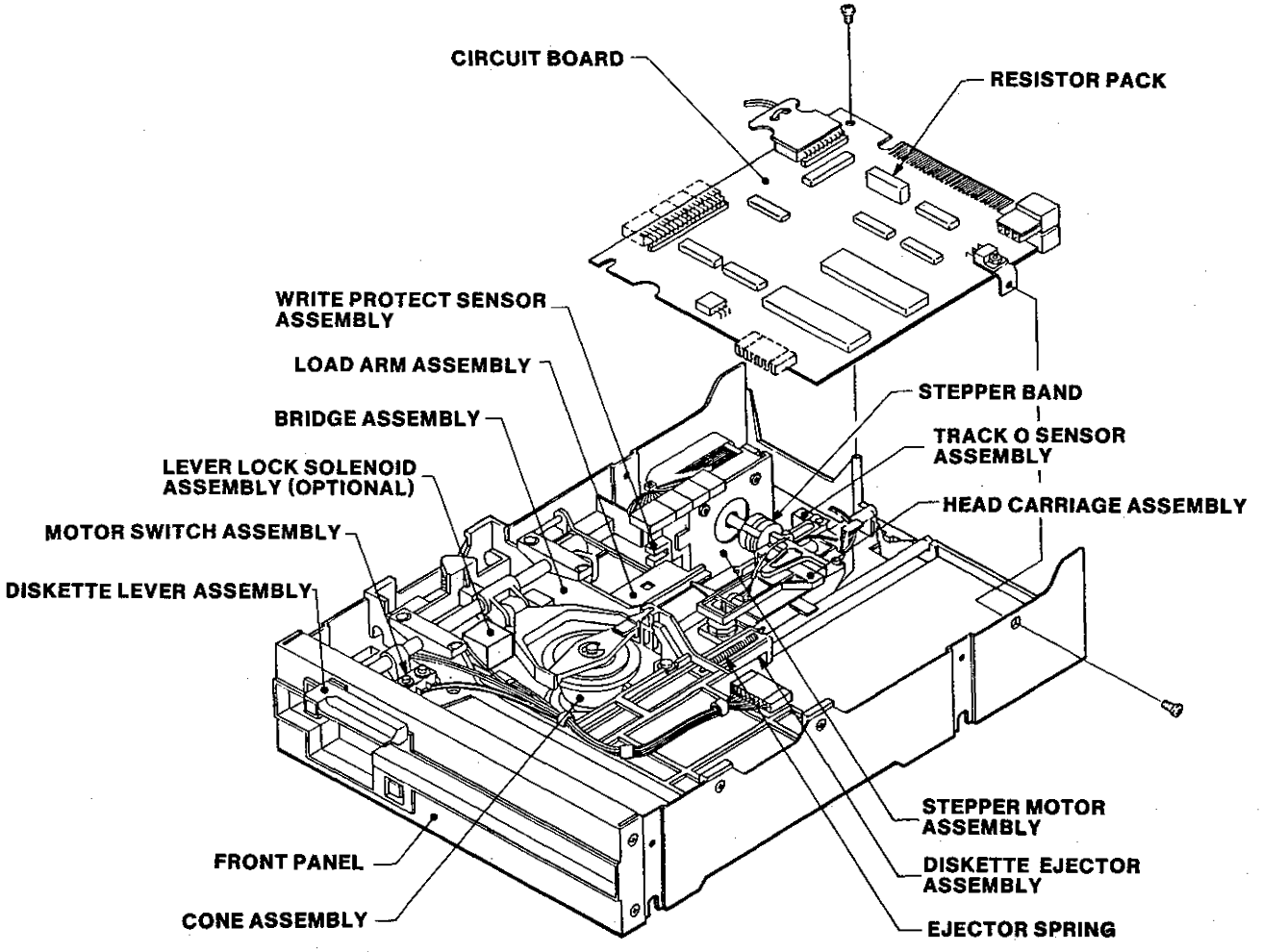


FIGURE 1-1
DISK DRIVE

SECTION 2

PRODUCT SPECIFICATIONS

INTRODUCTION

This section contains the mechanical, electrical, reliability, and environmental specifications for the TM848-1E and TM848-2E drives.

2.1 MECHANICAL SPECIFICATIONS

Figure 2-1 contains the physical dimensions of the drive.

2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

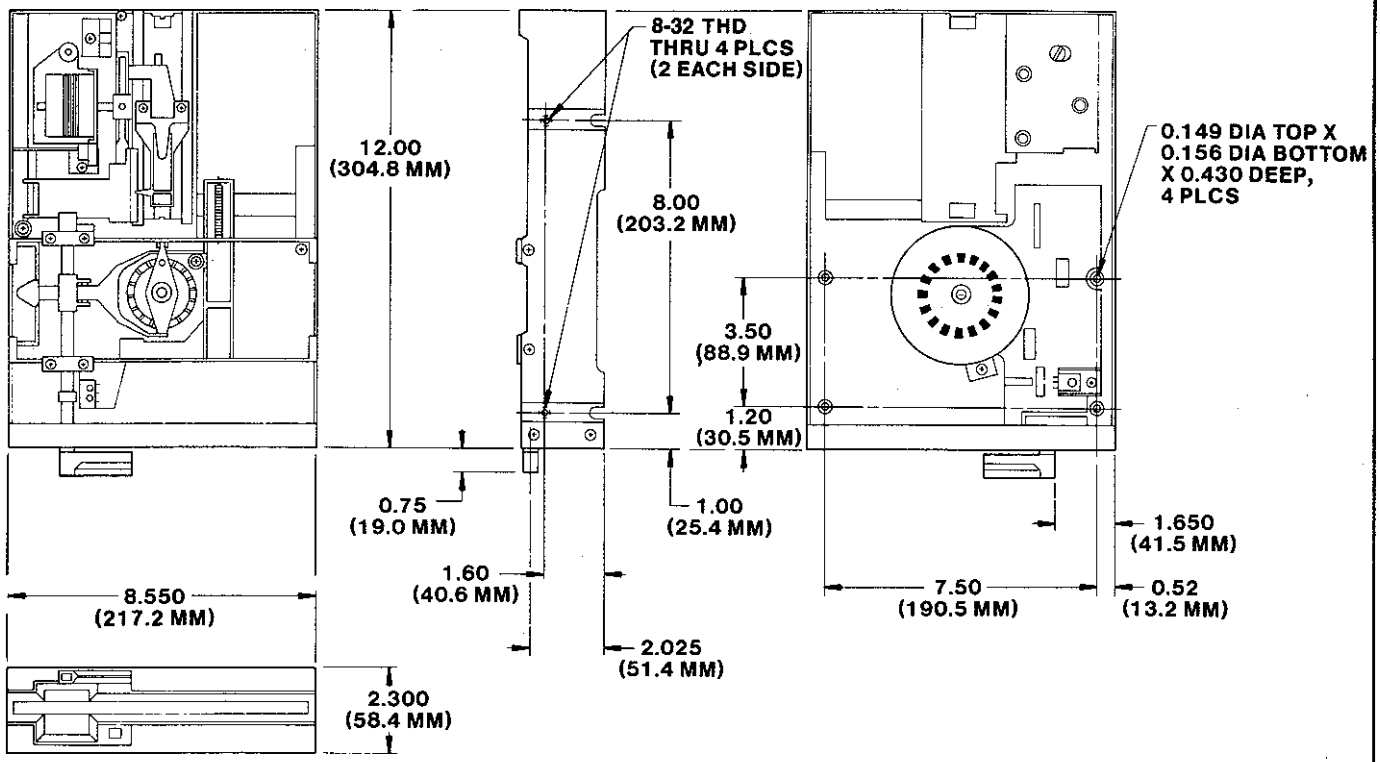
The electrical and operational specifications are located in Table 2-1.

2.3 RELIABILITY SPECIFICATIONS

The reliability specifications are located in Table 2-2.

2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are located in Table 2-3.



NOTES: 1. DIMENSIONS ARE GIVEN IN INCHES. METRIC EQUIVALENTS ARE IN PARENTHESES.
2. TOLERANCE ON ALL DIMENSIONS IS ±.020 INCH (±.508 MM).
3. WEIGHT IS APPROXIMATELY 5.7 POUNDS.

FIGURE 2-1
DISK DRIVE OUTLINE DRAWING

TABLE 2-1
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	203.20 millimeter, 8-inch, IBM industry- standard diskette
Media Life (for reference only)	3×10^6 passes per track
Tracks Per Inch	48 TPI, both drives
Tracks Per Drive	
TM848-1E	77 tracks per drive
TM848-2E	154 tracks per drive, 77 per side
Track Spacing	0.529 millimeter, 20.8 milinches
Inside Track Radius	
Both Drives, Side 0	51.50 millimeters, 2.03 inches
TM848-2E, Side 1	49.42 millimeters, 1.95 inches
Outside Track Radius	
Both Drives	91.75 millimeters, 3.61 inches
TM848-2E, Side 1	89.64 millimeters, 3.53 inches
Head Life	15,000 media contact hours
Disk Rotational Speed, microprocessor controlled	360 RPM $\pm$1.5 percent
Instantaneous Speed Variation (ISV)	$\pm$1 percent
Motor Start Time	150 milliseconds, maximum
Seek Time, track to track	3 milliseconds, minimum
Head Settling Time	15 milliseconds
Average Track Access Time, including head settling time	91 milliseconds
Data Transfer Rate	500,000 bits per second

TABLE 2-1 (CONTINUED)
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Flux Reversals Per Inch (FRPI), inside track	
Both Drives, Side 0	6,536 FRPI
TM848-2E, Side 1	6,816 FRPI
Unformatted Recording Capacity	
TM848-1E	0.8 megabyte per disk
TM848-2E	1.6 megabytes per disk
D. C. Voltage and Current Requirements	
+24 volts D. C. Power	+24 volts, ±10 percent at 700 milliamperes, typical. For surge current requirements, see Figures 2-2 and 2-3.
+5 volts D. C. Power	+5 volts, ±5 percent at 450 milliamperes, typical
Typical Current Requirements For +24 volts D. C.	
Spindle Motor	170 milliamperes
Stepper Motor	400 milliamperes
Electronics	130 milliamperes
Power Dissipation	20 watts, typical
Shipment	When prepared for shipment by Tandon, the drive meets the requirements of NSTA preshipment test procedure Project 1A.

Configured for stepper motor enabled during motor start, 2.25 amps typical surge.

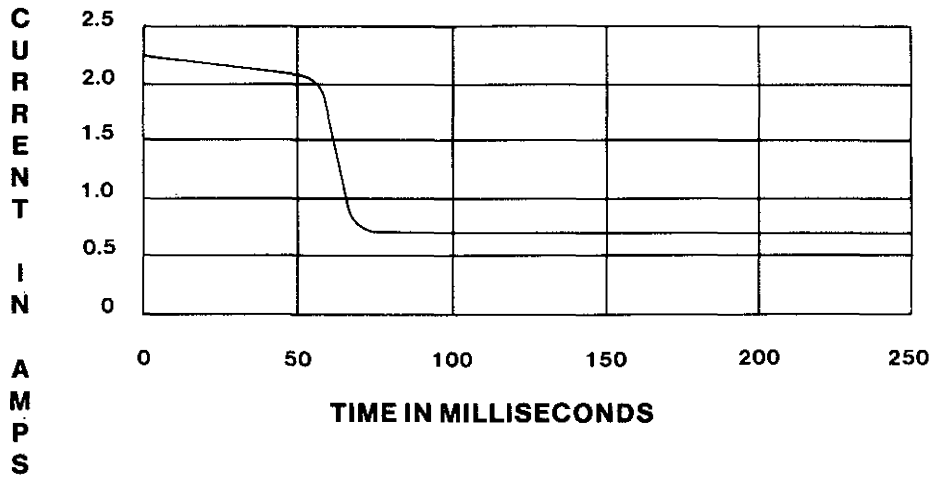


FIGURE 2-2
+24 VOLT D. C. CURRENT, CONFIGURATION 1

Configured for stepper motor disabled until motor comes up to speed, 1.8 amps typical surge.

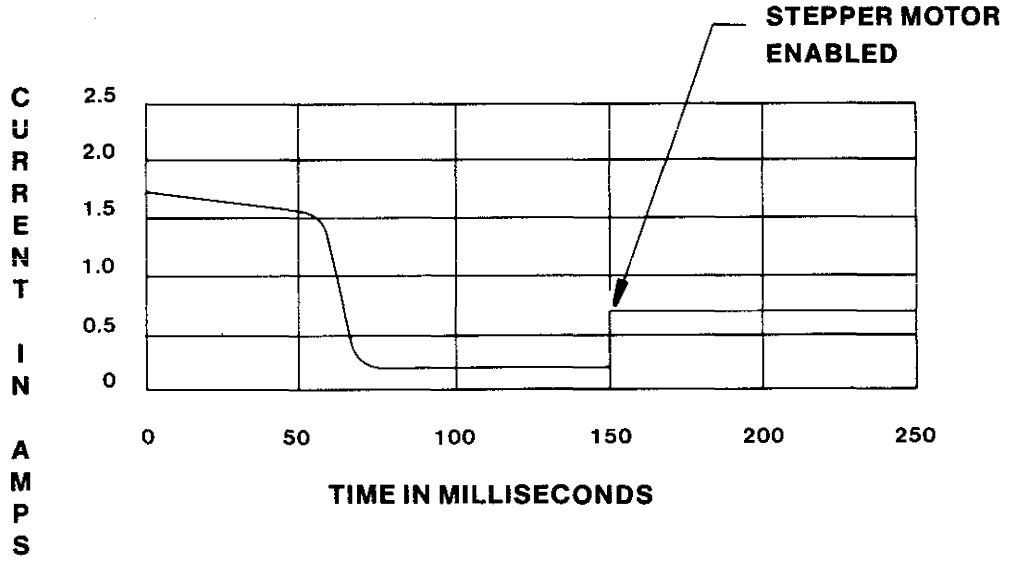


FIGURE 2-3
+24 VOLT D.C. CURRENT, CONFIGURATION 2

TABLE 2-2
RELIABILITY SPECIFICATIONS

Error Rates, maximum, exclusive of external sources, e.g.: electronics, defective and contaminated diskettes	
Soft Errors (Recoverable)	One in 10^9 bits
Hard Errors (Nonrecoverable)	One in 10^{12} bits
Seek Errors	One in 10^6 seeks
Mean Time Between Failures	10,000 power-on hours
Mean Time To Repair	30 minutes

TABLE 2-3
ENVIRONMENTAL SPECIFICATIONS

Temperature	
Operating, media dependent	4.4°C to 46°C, 40°F to 115°F
Nonoperating	−40°C to 71°C, −40°F to 160°F
Relative Humidity	
Operating, noncondensing, media dependent	20-to-80 percent
Nonoperating, noncondensing	5-to-95 percent

SECTION 3

OPERATION

INTRODUCTION

This section contains information on how to unpack, check out, install, and operate the TM848-1E and TM848-2E drives.

3.1 UNPACKING THE DRIVE

The drives are packaged in protective containers to minimize the possibility of damage during shipment. The following list is the recommended procedure for unpacking the drive.

1. Place the container on a flat work surface.
2. Remove the upper half of the container.
3. Remove the drive from the lower half of the container.
4. Check the contents of the container against the packing slip.
5. Investigate the contents of the container for possible damage.
6. Notify the carrier immediately if any damage is found.

3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, the following inspection should be conducted:

1. Check to ensure that the diskette lever opens and closes.
2. When the lever is moved to an open position, the head arm raises.
3. Remove the cardboard shipping insert, and retain for future shipment.
4. Ensure that the front panel is secure.
5. Ensure that the circuit board is secure.
6. Ensure that the connectors are firmly seated.

3.3 MOUNTING THE DRIVE

The drive has been designed so it may be mounted in any plane, i.e.: upright, horizontal, or vertical. When mounted horizontally, the Logic circuit board side of the chassis must be the top side.

Eight holes are provided for mounting: two on each side and four on the bottom of the housing (see Figure 2-1). The two mounting holes on each side are tapped for 8-32 screws. The four mounting holes on the bottom require 8-32 thread forming screws. When installed in either plane, horizontal or vertical, only two mounting screws are required to securely hold the drive in place.

Optional straps are available to permit two drives to be attached together for installation in standard width drive openings.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances. In addition, it is recommended that mounting schemes include no more than two mounting surfaces.

The drive is manufactured and tested with some critical internal alignments that must be maintained. Hence, it is important that the mounting hardware not introduce significant stress on the chassis.

DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e.g., dust, lint, and paper chad since the drive does not have a dust cover.

COOLING

Heat dissipation from a single drive is normally 20 watts, 68 BTU per hour, under high load conditions. When the drive is mounted so the components have access to a free flow of air, normal convection cooling allows operation within the specified temperature range.

When the drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors, printed circuit boards, and diskettes.

When forced air is used, air flow must be directed outward from the drive. Do not intake air through the drive or heads and diskettes.

3.4 INTERFACE CONNECTIONS

Interface connections for the TM848-1E and TM848-2E are made via a user-supplied, fifty-pin, flat ribbon connector, 3M Scotchflex, Part Number 3415, or its equivalent. This connector mates directly with the circuit board connector at the rear of the drive.

The interface description of the connectors, and the location of each one, is contained in this section. Interface lines are located in Table 3-1. D. C. power connector pin assignments are located in Table 3-2, Section 3.5 of this manual.

The signal wire harness should be of the flat ribbon or twisted pair type, have a maximum length of ten feet, and have a 26-to-28 gauge conductor compatible with the connector to be used. It is recommended that the interface cable have a characteristic impedance of 100 ohms.

All interface signals are TTL compatible. Logic true (low) is +0.4 volt maximum. Logic false (high) is +2.4 volts minimum.

INPUT CONTROL LINES

These input lines are individually terminated through a 150 ohm resistor pack installed in the dip socket located at RP1. In a single-drive system, this resistor pack should be installed to provide the proper terminations. In a multiple-drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed.

The drive can terminate the following input lines:

1. Direction
2. Step
3. Write Data
4. Write Gate
5. In Use
6. Side Select (TM848-2E only)
7. Write Current Switch
8. Head Load

MOTOR ON CONTROL

The Motor On Control lines are used to control the spindle motor. With the MOL jumper in (factory installed), the Motor On Control lines are low true. With the MOH jumper installed (optional), the Motor On Control lines are high true (see Table 3-3 located in Section 3.6).

DRIVE SELECT LINES

The Drive Select lines provide a means of selecting and deselecting a drive. These four lines, DS1 through DS4, allow independent selection of up to four drives attached to the controller.

When the signal logic level is true (low), the drive electronics are activated, and the drive is conditioned to respond to Step or to Read/

TABLE 3-1
DRIVE INTERFACE LINES AND PIN ASSIGNMENTS

Ground	Pin	Signal
1	2	Write Current Switch
3	4	Motor On Control 1
5	6	Motor On Control 2
7	8	True Ready (Motor On Control 3, Optional)
9	10	Two Sided (Strappable) (TM848-2E only)
11	12	Disk Change (Strappable)
13	14	Side Select (TM848-2E only)
15	16	In Use Indicator (Strappable)
17	18	Head Load Line/Motor Control
19	20	Index
21	22	Ready
23	24	Motor On Control 4
25	26	Drive Select 1 (Side Select Option, TM848-2E only)
27	28	Drive Select 2 (Side Select Option, TM848-2E only)
29	30	Drive Select 3 (Side Select Option, TM848-2E only)
31	32	Drive Select 4 (Side Select Option, TM848-2E only)
33	34	Direction Select (Side Select Option, TM848-2E only)
35	36	Step
37	38	Write Data
39	40	Write Gate
41	42	Track 0
43	44	Write Protect
45	46	Read Data
47	48	Alternate I/O
49	50	Alternate I/O

Write commands. When the signal logic level is false (high), the input control lines and the output status lines are disabled.

The Drive Select address is determined by a select shunt on the circuit board. Drive Select lines 1 through 4 provide a means of daisy chaining a maximum of four drives to a controller. Only one can be true (low) at a time. An undefined operation might result if two or more drives are assigned the same address or if two or more Drive Select lines are in the true (low) state simultaneously. A Drive Select line must remain stable in the true (low) state until any operation in progress (Step, Read/Write) is completed.

Using Side Select options 1B through 4B, Drive Select lines may be used as Side Select lines for the TM848-2E (see Section 3.6).

DIRECTION SELECT AND STEP LINES (TWO LINES)

When the drive is selected, a true (low) pulse on the Step line, with a time duration greater than one microsecond, initiates the access motion. The direction of motion is determined by the logic state of the Direction Select line when a step pulse is issued. The motion is toward the center of the disk if the Direction Select line is in the true (low) state. The direction of motion is away from the center of the disk if the Direction Select line is in the false (high) state.

To ensure proper positioning, the Direction Select line should be stable at least 1 microsecond prior to the corresponding rising edge of the step pulse, and remain stable 100 nanoseconds after it.

NOTE

TM848-1E and TM848-2E drives include a microprocessor-controlled buffered seek capability. The controller may issue step pulses of one microsecond minimum width, and fifteen microseconds minimum spacing between trailing edges. Internal drive electronics issue step commands at a rate of three milliseconds.

The drive electronics ignore step pulses when one of five conditions exists:

1. The Write Gate is true (low).
2. The Direction Select is false (high), and the head is positioned at Track 0.
3. The drive is not selected.
4. When trying to seek beyond Track 76.
5. When the diskette lever is opened.

COMPOSITE WRITE DATA

When the drive is selected, this interface line provides the bit serial Composite Write Data pulses that control the switching of the Write Current in the selected head. The write electronics must be conditioned for writing by the Write Enable line.

For each high-to-low transition on the Composite Write Data line, a flux change is produced at the write head gap. This causes a flux change to be recorded on the media.

When a single-density (FM) type encoding technique is used in which data and clock form the combined Write Data Signal, it is recommended that the repetition of the high-to-low transitions, while writing all zeros, be equal to one-half the maximum data rate, 250 kilohertz ± 0.1 percent. The repetition of the high-to-low transitions while writing all ones should be equal to the maximum data rate, 500 kilohertz ± 0.1 percent.

Host controllers may implement write precompensation circuits that recognize worst case patterns and adjust the Write Data waveform. Although a value cannot be specified for write precompensation, Tandon suggests a value of 125 nanoseconds for systems using MFM double density recording format.

WRITE GATE

When this signal is true (low), the write electronics are prepared for writing data and the read electronics are disabled. This signal turns on Write Current in the selected Read/Write head. Data is written under the control of the Composite Write Data and Side Select input lines. When the Write Gate line is false (high), all write electronics are disabled.

When a write protected diskette is installed in a drive, the write electronics are disabled, irrespective of the state of the Write Gate or Side Select lines. With the NP jumper installed, a diskette cannot be write protected.

NOTE

Changes of state of the Write Gate line should occur before the first Write Data pulse.

IN USE

This strappable feature controls the lever lock solenoid when the DL option is installed.

WRITE CURRENT SWITCH

Normally, Write Current switching is accomplished by the host controller. A true (low) level on this line reduces the Write Current. Using option IC, the drive automatically reduces Write Current at Track 43.

SIDE SELECT

The Side Select interface line, available only on Tandon's TM848-2E, defines which side of a two-sided diskette is used for reading or writing. An open circuit, false (high) level

selects the Read/Write head on side zero, the lower head of the drive. A true (low) level on this line selects the Read/Write head on side one, the upper head of the drive. When switching from one head to the other, a 100 microsecond delay is required before any Read or Write operation can be initiated.

HEAD LOAD LINE/MOTOR CONTROL

This line may be used to control the spindle motor and/or the lever lock solenoid (see Section 3.6).

OUTPUT CONTROL LINES

There are eight output lines, five of which are standard and three of which are strappable features. The standard output signals are: Index/Sector, Track 0, Write Protect, Read Data, and Ready. The strappable output signals are Disk Change, Two-Sided, and True Ready.

INDEX

The Index signal represents the output of the Index sensor. An Index pulse is provided once every revolution, 166.67 milliseconds nominal, to indicate the beginning of a track to the controller. The leading edge of this signal must always be used to ensure timing accuracy. The Index line remains in the true (low) state for the duration of the Index pulse, which is nominally four milliseconds.

TRACK 0

When the drive is selected, the Track 0 interface signal indicates to the controller that the Read/Write head is positioned on Track 0, the outermost track. This signal remains true (low) until the Read/Write head is moved away from Track 0. This signal is false (high) when the selected drive's Read/Write head is not on Track 0.

WRITE PROTECT

The Write Protect signal is provided to indicate to the user that a write protected diskette is installed. This signal is true (low) when the diskette's Write Protect notch is uncovered. When the Write Protect signal is false (high), the write electronics are enabled, and write operations can be performed.

READ DATA

The Read Data line transmits data to the controller when the drive is selected and not writing. It provides a pulse for each flux transition recorded and detected on the diskette by the drive electronics. Normally, this signal is false (high). It becomes true (low) for the active state. The Read Data output line goes true (low) for a duration of 200 nanoseconds, ± 50 nanoseconds, for each change recorded on the diskette.

READY

The Ready interface signal indicates a diskette has been inserted into the drive. Ready will not return to the false state until the lever is opened, and is not affected by Spindle Motor Control.

When a single-sided diskette is installed, Ready is active (low) if side zero is selected. Ready is false (high) if side one is selected on the TM848-1E. When a two-sided diskette is installed, Ready is active when either side of the diskette is selected on the TM848-2E.

TRUE READY

The True Ready interface signal indicates the diskette is rotating at 360 RPM, and a seek operation is complete, i.e., the head has settled. This may be used to indicate seek complete when using the buffered seek operation.

NOTE

This is a strappable feature with the Motor Control 3 input signal line.

DISK CHANGE

This strappable feature provides a true (low) signal to the interface when Drive Select is activated if the drive has gone from a Ready to a Not Ready condition while deselected. This line is reset on the true-to-false transition of Drive Select if the drive has gone to a Ready condition.

TWO-SIDED

This option is available only on Model TM848-2E. True (low) indicates that a two-sided diskette is installed.

TYPICAL INTERFACE CHARACTERISTICS

Lines between the controller and the drive have the following characteristics:

V_{out} True = +0.4 volt maximum at I_{out} = 48 milliamperes, maximum

V_{out} False = +2.4 volts minimum open collector at I_{out} = 250 microamperes, maximum

Figure 3-1 contains the electrical interface characteristics. Figure 3-2 contains the control and data timing requirements.

3.5 D. C. POWER

D. C. power is supplied to the drive through a six-pin AMP connector, J2, mounted on the circuit board. The mating connector, not supplied, is AMP Part Number 1-480270-0, using AMP contact Part Number 606191-1. Pin assignments are found in Table 3-2.

The chassis should be connected to earth ground to ensure proper operation.

TABLE 3-2
D. C. POWER CONNECTOR PIN ASSIGNMENTS

Pin	Supply Voltage
1	+24 volts D. C.
2	24 volts Return
3	5 volts Return
5	+5 volts D. C.
6	Return

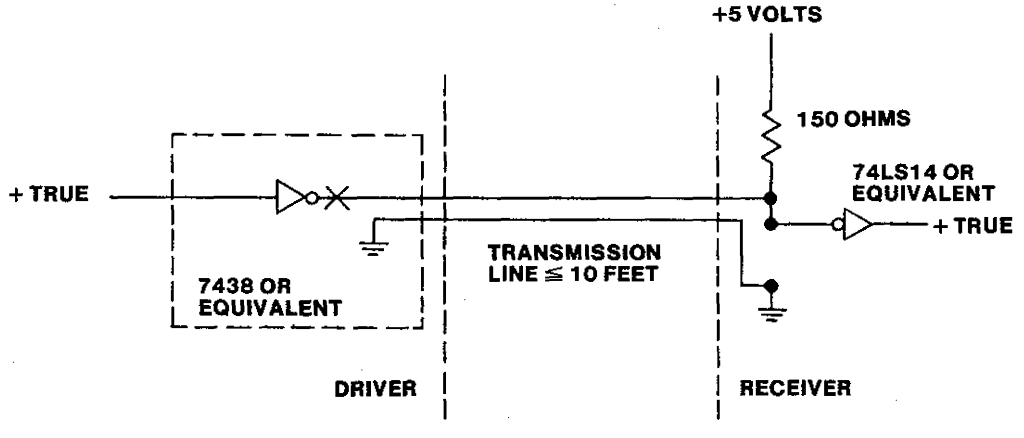
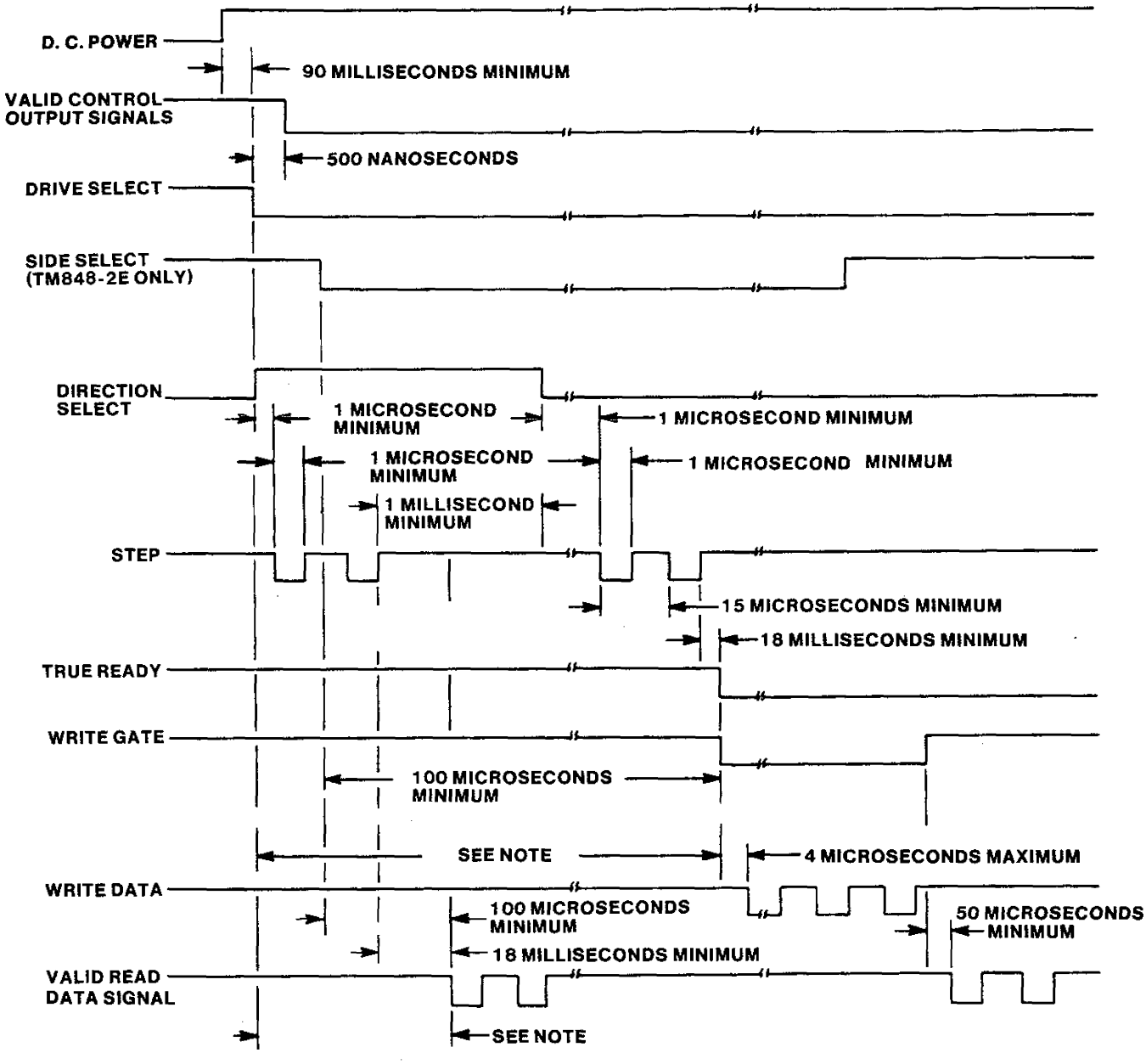


FIGURE 3-1
ELECTRICAL INTERFACE CHARACTERISTICS



NOTE: 150 MILLISECONDS, MINIMUM, DELAY MUST BE INTRODUCED AFTER DRIVE SELECT TO ALLOW TIME FOR THE D.C. MOTOR TO REACH 360 RPM OR THE OPTIONAL TRUE READY LINE MUST BE MONITORED.

FIGURE 3-2
CONTROL AND DATA TIMING REQUIREMENTS

3.6 DRIVE ADDRESS AND OPTION STRAPPING

The drive address and option strapping is determined by the different jumper configurations required for specific system applications. If jumper configurations are changed, power should be cycled off and on so the microprocessor can recognize the new configuration.

The description of user-selectable options should be used in conjunction with Table 3-3.

Throughout Section 3.6, an X denotes jumper installation, and a dash denotes jumper removed.

DRIVE SELECT (DS1—DS4)

This option allows the user to daisy chain up to four drives, and to enable one drive at a time. Drive Select is implemented by shorting one of the four connections, using a shorting plug. The drive comes equipped from the factory with DS1 installed. All outputs are gated with drive select, as set-up at the factory.

NOTE

The terminator resistor pack RPI, located on the logic circuit board should be installed in the last drive of the daisy chain. All other drives on the interface must have resistor packs removed.

DS1	DS2	DS3	DS4	DRIVE SELECT
X	–	–	–	Selects Drive 0 via J1-26.
–	X	–	–	Selects Drive 1 via J1-28.
–	–	X	–	Selects Drive 2 via J1-30.
–	–	–	X	Selects Drive 3 via J1-32.

HEAD SELECT OPTIONS (S1—S3 and 1B—4B)

The Side Select options allow the user to select the heads by various means. They are implemented by removing the shorting plug from the DS1—DS4 option pads.

HEAD SELECT USING DRIVE SELECT

To use the Drive Select lines to select the heads, etch cut S2 and install S3 along with one of the 1B—4B jumpers. The 1B—4B control signal selected may not be the same control line used for Drive Select, or an undefined condition results. When the control line that corresponds to the Drive Select jumper is driven low (true), the drive is enabled, and the lower head, Head 0, is selected. When the control line that corresponds to the 1B—4B jumper is driven low (true), the drive is enabled, and the upper head, Head 1, is selected.

HEAD SELECT USING DIRECTION SELECT

During a Read or Write operation, the state of the Direction Select line is undefined. Hence, it may be used to select the desired head. A high enables Head 0. A low enables Head 1. To incorporate this option, etch cut S2 and install S1.

S1	S2	S3	1B	2B	3B	4B	HEAD SELECT
–	X	–	–	–	–	–	Head Select via J1-14.
–	–	X	X	–	–	–	Head Select via J1-26.
–	–	X	–	X	–	–	Head Select via J1-28.
–	–	X	–	–	X	–	Head Select via J1-30.
–	–	X	–	–	–	X	Head Select via J1-32.
X	–	–	–	–	–	–	Head Select via J1-34.

TABLE 3-3
OPTION PATCHING

Option	Trace Designator	As Shipped	
		Installed	Not Installed
Drive Select	DS1—DS4	DS1	DS2—DS4
Head Select	S1—S3	S2	S1, S3
Head Select Using Drive Select	1B—4B		X
Power Save	PS	X	
Stepper Power From Head Load Line	HL		X
Spindle Motor Control	M1, M3, M4	M1, M3	M4
Motor Control Signal, Low True	MOL	X	
Motor Control Signal, High True	MOH		X
Motor Control Select	MC1—MC4		X
Ready	R	X	
True Ready	TR		X
Lever Lock Solenoid	DL		X
In Use, Lever Lock Option	D		X
In Use, Latched	LL		X
In Use, Not Latched	NL	X	
Disk Change	DC	X	
Two-Sided Diskette Installed	2S	X	
Inhibit Write When Write Protected	WP	X	
Allow Write When Write Protected	NP		X
External Write Current Switch	XC	X	
Internal Write Current Switch	IC		X
Diagnostic Mode	DM		X

STEPPER MOTOR POWER (PS, PS*, DS, HL)

When the PS jumper is installed, stepper motor power is controlled by the Drive Select line, DS, or the Head Load line, HL. When either line is true (low), the stepper motor is driven with full power, and is ready for a Seek, Read, or Write operation. When either line is false (high), +5 volt stand-by current is supplied to the stepper motor to hold the head carriage assembly in position. When the PS* option is in, the stepper motor continuously receives full power. PS* is diametrically opposite PS (see Figure 3-3).

PS	PS*	DS	HL	STEPPER POWER
–	X	–	–	Stepper power continuously on.
X	–	X	–	Stepper power on with Drive Select.
X	–	–	X	Stepper power on with Head Load line J1-18.

SPINDLE MOTOR CONTROL OPTIONS (M1, M3, M4, MOL, MOH, MC1–MC4)

M1 is used to enable the motor off delay timer. When this jumper is installed, a five second turn off delay of the spindle motor is activated on the trailing edge of the Motor Control signal.

With Motor Control using Drive Select or Head Load, the M3 and M4 jumpers determine which method of Motor Control is enabled. If option M3 or M4 jumpers are installed, the Motor On Control, MC1–MC4, options operate in a logical OR manner with the control signal(s) selected by the M3 and M4 jumpers.

NOTE

If the Motor Delay Timer option (M1) is installed, the five second turn off delay is in effect regardless of which M3/M4 configuration is implemented.

M1	M3	M4	MOTOR CONTROL
X	–	–	Enables five-second motor off delay timer.
–	–	–	Motor Control only with MC1–M4 options.
–	X	–	Motor Control using Drive Select.
–	–	X	Motor Control using Head Load.
–	X	X	Motor Control using Drive Select and Head Load, logical AND.

MOL	MOH	MC1	MC2	MC3	MC4	MOTOR CONTROL
X	–	–	–	–	–	Motor Control signals are low (true) active.
–	X	–	–	–	–	Motor Control signals are high (true) active.
X	–	X	–	–	–	Motor Control selected via J1-4.
X	–	–	X	–	–	Motor Control selected via J1-6.
X	–	–	–	X	–	Motor Control selected via J1-8.
X	–	–	–	–	X	Motor Control selected via J1-24.

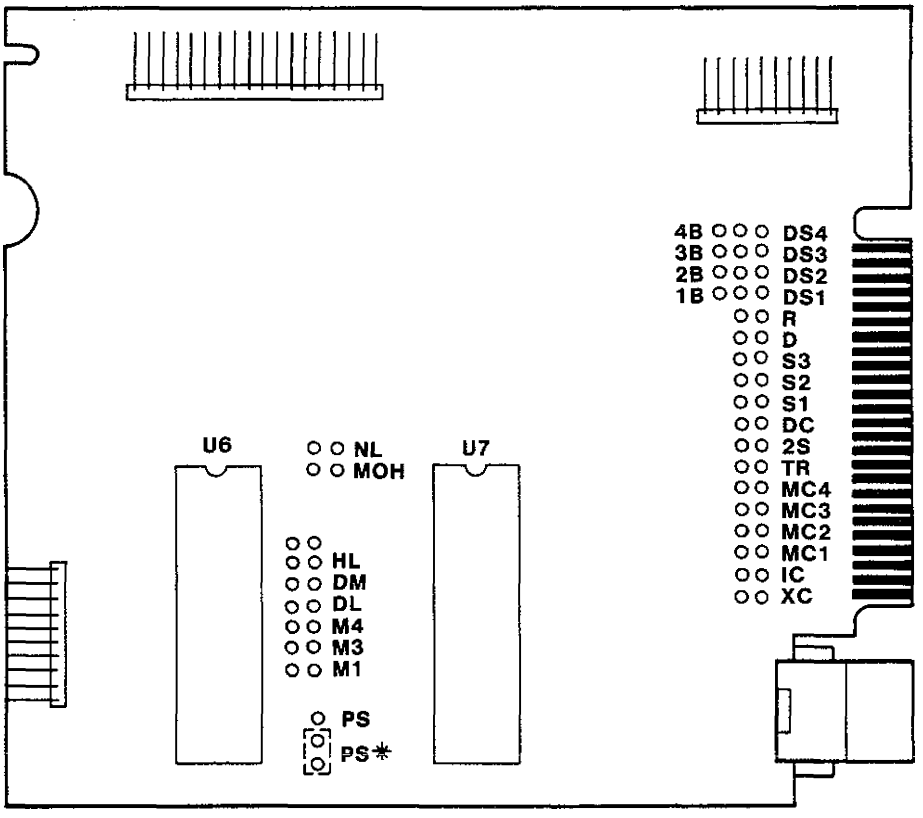


FIGURE 3-3
LSI CIRCUIT BOARD ASSEMBLY

READY AND TRUE READY (R AND TR)

When the R jumper is installed, the Ready signal is available at the interface. When the TR jumper is installed, the True Ready signal is available at the interface.

The R jumper is standard, while the TR jumper is optional. These two lines are independent functions, and may be used separately or together.

R	TR	READY OR TRUE READY
X	–	Ready signal via J1-22.
–	X	True Ready signal via J1-8.

NOTE

When using the True Ready option, Motor Control 3 may not be used.

LEVER LOCK OPTIONS (D, DL, LL, NL)

The lever lock solenoid, an optional feature, can be controlled by the In Use interface line J1-16.

D	DL	LL	NL	LEVER LOCK SOLENOID
–	–	–	–	Latched with Drive Select.
X	X	–	X	Latched by In Use via J1-16, true (low). Active energizes solenoid.
X	X	X	–	Latched by In Use via J1-16. Active low, in conjunction with Drive Select, latches the solenoid. The solenoid remains latched until In Use is false (high) on the leading edge of Drive Select.

DISK CHANGE (DC)

This output is used to indicate to the controller that a disk change has been made. The internal signal is gated with Drive Select. When the lever is opened, the Disk Change line goes low (true), and remains low until the trailing edge of the next Drive Select.

DC	DISK CHANGE
–	Disk Change signal not available.
X	Disk Change signal available via J1-12.

TWO-SIDED DISKETTE INSTALLED (2S)

When a two-sided diskette is installed, internal circuitry gates this signal with Drive Select. It sends a low (true) signal to the controller, indicating that a double-sided diskette is installed (index hole two is present). This option is factory installed.

2S	TWO-SIDED DISKETTE
–	Two-sided diskette signal not available.
X	Two-sided diskette signal available via J1-10.

WRITE PROTECT (WP AND NP)

This WP option is used to lock out the Write Gate when a write protected diskette is installed. It is factory installed.

The NP option allows the controller to write on any diskette, whether or not it is write protected. It does not stop the Write Protect signal from being sent on the interface line. This option is implemented by removing WP, and installing NP.

WP	NP	WRITE PROTECT
X	–	Disables Write Protect, for write protected diskette.
–	X	Allows writing on any diskette.

WRITE CURRENT SWITCH (XC AND IC)

The XC option allows the host controller to switch the Write Current independently of the drive's onboard microprocessor. It is factory installed.

To implement the IC option, remove the XC jumper, then install a jumper at IC.

XC	IC	WRITE CURRENT SWITCHING
X	–	External Write Current switch.
–	X	Microprocessor automatically switches Write Current at Track 43.

DIAGNOSTIC MODE OF OPERATION (DM, DL, M1, M3, M4)

The test programs allow the user to test some aspects of drive operation without the use of special test equipment. The programs allow the user to isolate the problems of the drive. The diagnostic mode provides 16 tests (see Table 3-4).

To enter the diagnostic mode:

1. Make a note of which jumpers are installed for normal operating conditions (see Table 3-3).
2. Remove the DL, M1, M3, and M4 jumpers.
3. Install the DM jumper, and supply power to the drive.
4. Using the DL, M1, M3, and M4 jumpers, select the diagnostic test desired by inserting the jumper according to Table 3-4.

To exit the diagnostic mode:

1. Remove power from the drive.
2. Remove the DM, DL, M1, M3, and M4 jumpers.
3. Reinstall the jumpers in their original configuration.
4. Power on the drive.

3.7 DISKETTES

The TM848-1E and TM848-2E drives use an IBM-compatible, eight-inch diskette. Diskettes are available with a single index hole or with multiple (index and sector) holes.

Diskettes with a single hole are used when soft sector format is required. Multiple hole diskettes provide sector information through the use of an index sensor and electronics.

Figure 3-5 illustrates the diskette used with the drive. This recording media is a flexible diskette enclosed in a protective jacket. The diskette, free to rotate within the jacket, is continuously cleaned by its soft fabric lining during normal operation.

LOADING THE DISKETTE

The drive is loaded by inserting the diskette, with its head aperture forward, into the front slot of the drive. Access to the diskette loading slot is obtained by opening the front lever.

The diskette should be carefully inserted until it is solidly against the back stop.

CAUTION

Damage to the center of the diskette may result if the door is closed when the diskette is not properly inserted. This prevents reliable recovery of the recorded data.

WRITE PROTECT TAB

The drive is equipped with a Write Protect Sensor Assembly. This sensor operates in conjunction with the diskette, which has a slot cut in the protective jacket.

TABLE 3-4
DIAGNOSTIC MODE OF OPERATION

DL	M4	M3	M1	Test	Description of Test
–	–	–	–	0	**Seek to Track 0, and turn on spindle motor.** This test seeks the carriage to Track 0, and turns on the spindle motor. It may be used to check the Track 0 status.
–	–	–	X	1	**Seek to Track 1, and turn on spindle motor.** This test seeks the carriage to Track 1, and turns on the spindle motor. It may be used for index-to-data burst testing with an alignment diskette.
–	–	X	–	2	**Seek to Track 38, and turn on spindle motor.** This test seeks the carriage to Track 38. It may be used for radial alignment adjustment with an alignment diskette.
–	–	X	X	3	**Alternate seek between Track 0 and Track 76 with spindle motor on.** This test continuously moves the carriage between Tracks 0 and 76. This test is used to exercise the positioner system.
–	X	–	–	4	**Toggle front panel L.E.D. with each revolution of the disk.** This test toggles the front panel L.E.D. at the leading edge of each side zero index pulse. A single-sided disk should be used for this test.
–	X	–	X	5	**Toggle front panel L.E.D. with each revolution of the disk.** This test toggles the front panel L.E.D. at the leading edge of each side one index pulse. A double-sided disk should be used for this test.
–	X	X	–	6	**Seek to Track 76, and turn on spindle motor.** This test seeks the carriage to Track 76, and turns on the spindle motor. This test may be used to check index-to-data burst and azimuth.
X	–	–	X	9	**Seek to Track 2, and monitor the Track 0 sensor.** This test moves the carriage to Track 2, and displays, using the front panel L.E.D., the state of the Track 0 sensor. The Track 0 sensor should change state at Track 2. The L.E.D. is on at Track 0.

TABLE 3-4 (CONTINUED)
DIAGNOSTIC MODE OF OPERATION

DL	M4	M3	M1	Test	Description of Test
X	–	X	–	10/A	**Monitor the write protect sensor.** This test checks the write protect sensor. The front panel L.E.D. should turn on and off by moving a disk, which has the write protect notch covered, in and out of the drive. The L.E.D. is on when write protect is true.
X	X	–	–	12/C	**Monitor the status of the lever position switch.** This test is used to check the lever position switch. The front panel L.E.D. flashes on and off with the opening and closing of the diskette lever position switch. The L.E.D. is on when the lever is closed.
X	X	X	X	15/F	**Flash version number.** This test outputs the firmware version number to the front panel L.E.D.

Notes: X = Jumper In
– = Open

When the slot is covered with an optically opaque, self-adhesive tab, the diskette is write enabled. When the tab is removed, the diskette is write protected.

DISKETTE HANDLING AND STORAGE

It is important the diskette be handled and stored correctly so the integrity of the recorded data is maintained. A damaged or contaminated diskette can impair or prevent recovery of data, and can result in damage to the Read/Write heads.

Figure 3-4 contains an illustration of the physical configuration of the diskette. The 7.88-inch diskette is oxide-coated, flexible mylar. It is enclosed in an eight-inch square protective jacket. In addition, openings for the drive hub and diskette index hole are provided.

Figure 3-5 provides some helpful hints on the care and handling of the drive and diskettes. In addition, to ensure trouble-free operation and to enhance the service life of the diskette, the following handling procedure should be observed.

1. Return the diskette to the protective jacket when not in use.

2. Avoid exposing the diskette to any magnetizing force in excess of 50 oersted.

   NOTE

   The 50-oersted level magnetizing force is reached approximately three inches from a typical source, e.g., motors, generators, or transformers.

3. To avoid warping the diskette, do not store it in direct sunlight.

4. Do not use a lead pencil or a ballpoint pen to write on the label. Use a felt tipped pen, and mark lightly on the label.

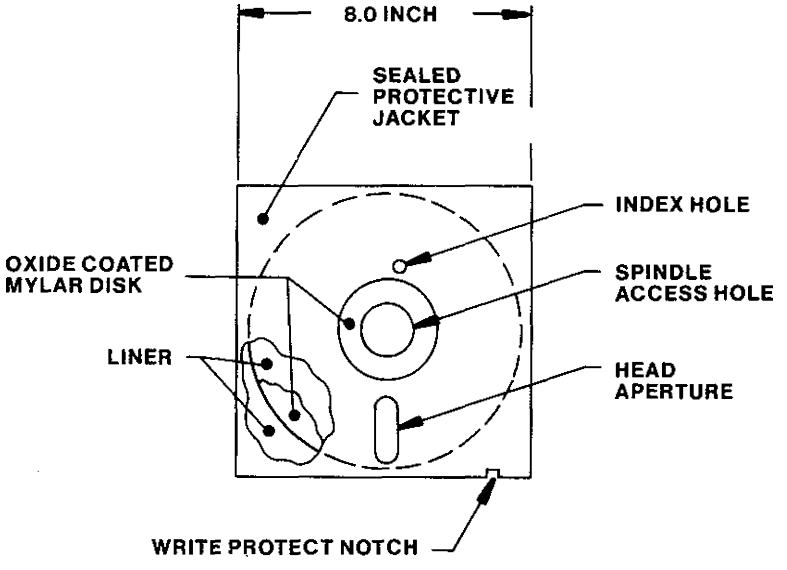
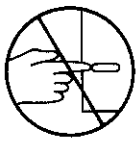


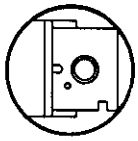
FIGURE 3-4
RECORDING MEDIA

DO NOT WRITE ON THE DISKETTE WITH PEN OR PENCIL. USE A FELT TIPPED PEN.

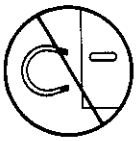


DO NOT TOUCH PRECISION SURFACE WITH YOUR FINGERS.

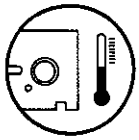
TO AVOID DAMAGE TO THE DISKETTE AND DRIVE, INSERT DISKETTE CAREFULLY UNTIL THE BACKSTOP IS ENCOUNTERED.



RETURN THE DISKETTE TO ITS JACKET WHEN NOT IN USE.



KEEP THE DISKETTE AWAY FROM MAGNETIC FIELDS.



DISKETTES SHOULD BE STORED AT 10°C to 52°C 50°F to 125°F

HANDLE WITH CARE; BENDING AND FOLDING MAY DAMAGE DISKETTE.

FIGURE 3-5
DISKETTE CARE AND HANDLING

SECTION 4

THEORY OF OPERATION

INTRODUCTION

This section contains a description on the theory of operation of the drive. The discussion begins with a general summary of magnetic data recording, followed by a description of each major function of the drive.

Circuit block diagrams and schematics are located in the appendices. They are useful to show the interconnections between the electronic circuits and the mechanical components.

4.1 DATA RECORDING

Digital information is represented by a sequence of bits: either 0 or 1. Small areas of the medium in which such binary information is stored, for example the iron oxide coating of a magnetic disk, must be put in one state or the other to represent the data.

Recording of data on a magnetic medium is based on the principles of electromagnetics. When current flows in a coil of wire it produces a magnetic field. The field is confined in a core of magnetic material around which the wire is wound. A narrow slot, called the air gap, is placed in the core located closest to the media. It is the magnetic field in the vicinity of the air gap that magnetizes the magnetic medium (Figure 4-1). When the current is reversed, the polarity of magnetization is reversed.

Information can be recorded on the diskette by using a double-frequency code. The magnetization profiles in each bit cell for the number sequence shown for frequency modulation (FM) recording are shown in Figure 4-2.

When data is read, the same head that writes the data is used. The data stored is a digital bit representing a 0 or 1. In each bit cell, the first flux reversal represents a clock bit. A second reversal represents a stored bit 1. The absence of a second reversal represents a bit 0.

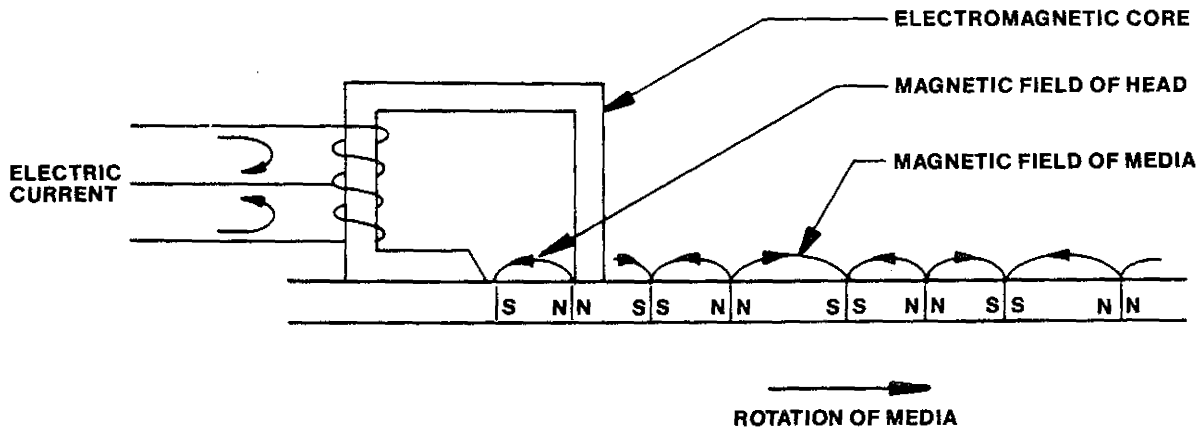


FIGURE 4-1
ELECTROMAGNETIC CORE

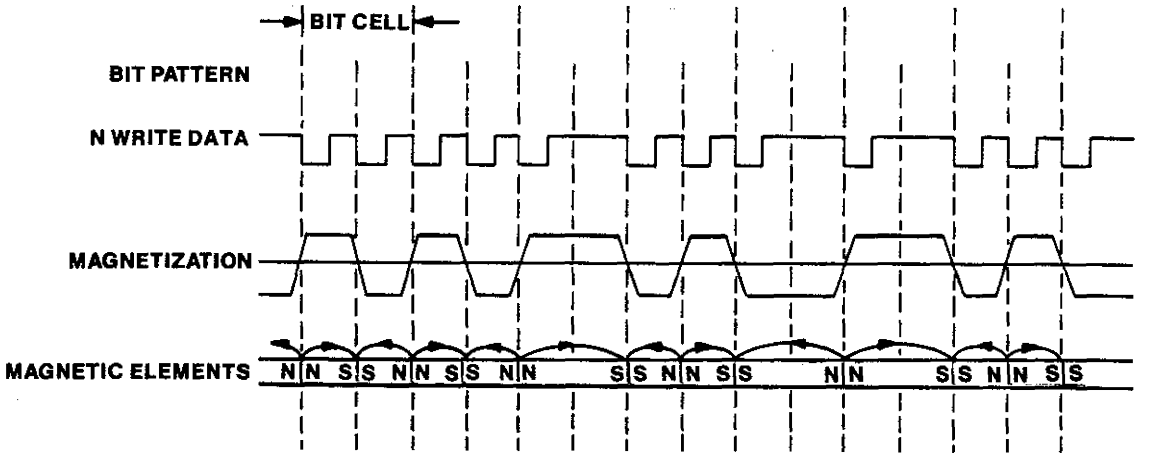


FIGURE 4-2
FM RECORDING MAGNETIZATION PROFILES

As the disk spins, the magnetic fields of the stored data pass successively under the head. The changing fields induce, in the head, an A. C. voltage signal which is then amplified and filtered, differentiated, and digitized (Figure 4-3).

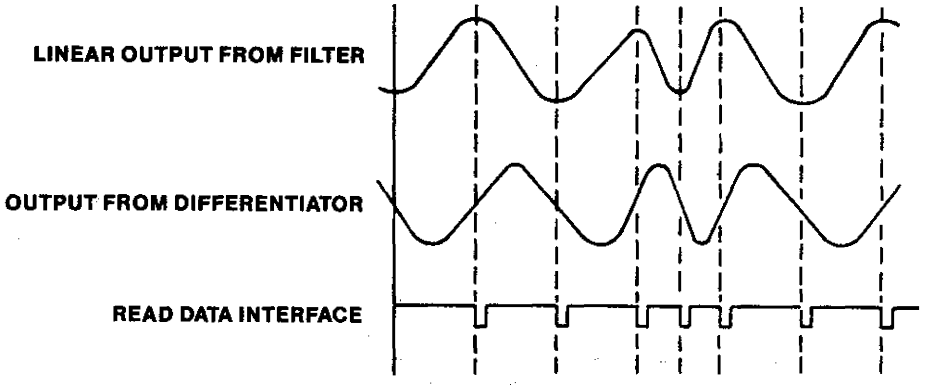


FIGURE 4-3
READ TIMING DIAGRAM

4.2 COMPONENTS OF THE DRIVE

The drive contains the electrical and mechanical components required to perform four major functions:

1. Generate and interpret control and status signals.
2. Position the read/write head(s) to the desired track.
3. Write and read data.
4. Control the spindle.

The electrical and mechancial components of the drive are connected together via multi-pin connectors (Figure 4-4). This allows the individual assemblies to be removed.

All major functions, other than the read data circuits, and part of the write data circuits, are monitored by the LSI chip and the microprocessor. The microprocessor generates the required output status signals and controls the functions of the drive.

4.3 GENERATE AND INTERPRET CONTROL AND STATUS SIGNALS

The components of the drive required to generate and interpret the control signals are:

1. Index Sensor(s)
2. Write Protect Sensor
3. Track 0 Switch
4. Lever Closed Switch
5. Lever Lock Solenoid

INDEX SENSOR(S)

The index signal is derived from an infrared L.E.D. and phototransistor detector. When the index/sector hole in the diskette passes through the index sensor, the light from the L.E.D. is allowed to turn on the index detector, producing a positive pulse on Test Point 1, for index number two sensor, and Test Point 2 for index number one sensor.

This signal is supplied to the microprocessor for timing. It is also gated internally in the LSI chip with drive select for an output control signal at the interface (Figure 4-5).

WRITE PROTECT SENSOR

When a write protected diskette is installed, light from the write protect L.E.D. is detected by the write protect sensor transistor, causing the output of the sensor to be high at Test Point 5. The signal, gated internally in the LSI chip with DR SEL +, generates the Write Protect signal. If a write protected diskette is inserted, write gate is disabled.

TRACK 0 SENSOR

The Track 0 sensor signal is derived from an optical sensor internal to the drive. As the head carriage moves back toward Track 0, the sensor is deactivated between Tracks 1 and 2 (Figure 4-6).

This signal produces a low output on Test Point 3, which is supplied to the LSI chip. The combination of the Track 0 sensor being deactivated and the proper step motor phase (Phase Zero) produces the proper Track 0 signal, gated internally with Drive Select, to the interface connector, P1 Pin 42.

LEVER CLOSED SWITCH

The Lever Closed Switch signal is derived from a mechanical switch mounted internally in the drive. When the lever is closed, a high (true) signal is produced on P3, Pin 12, and supplied to the LSI chip.

DRIVE SELECT

The drive select signal is sent from the host controller to the interface connector.

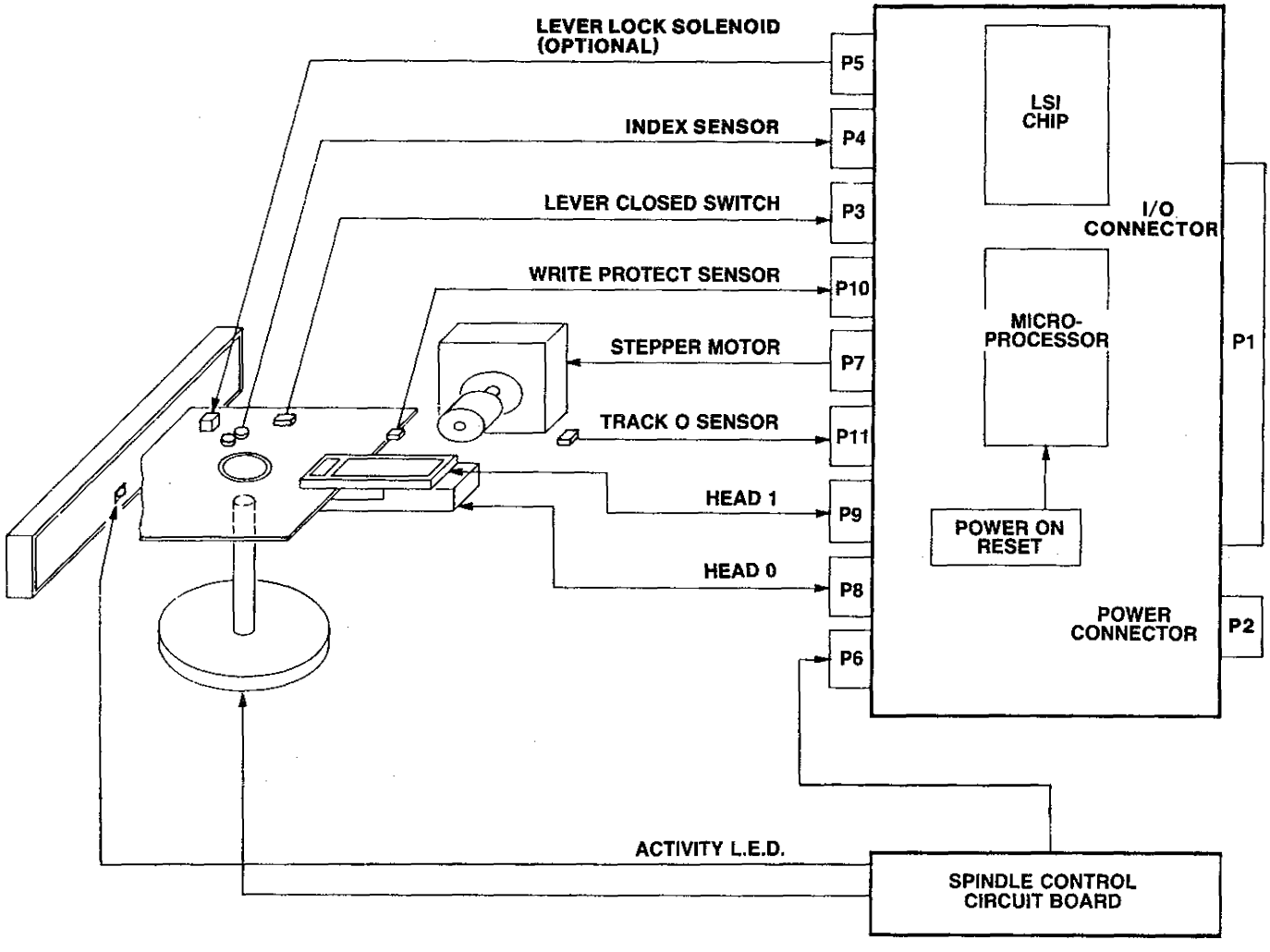


FIGURE 4-4
INTERCONNECT BLOCK DIAGRAM

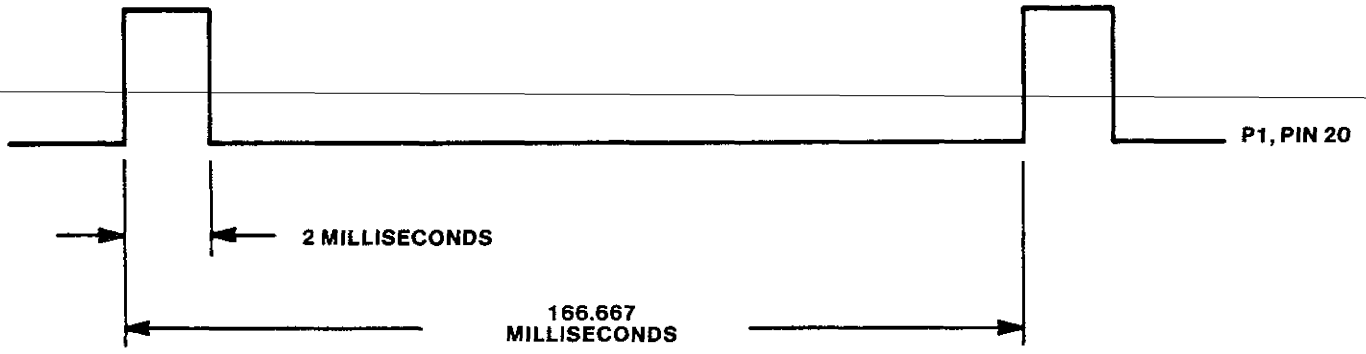


FIGURE 4-5
INDEX PULSE

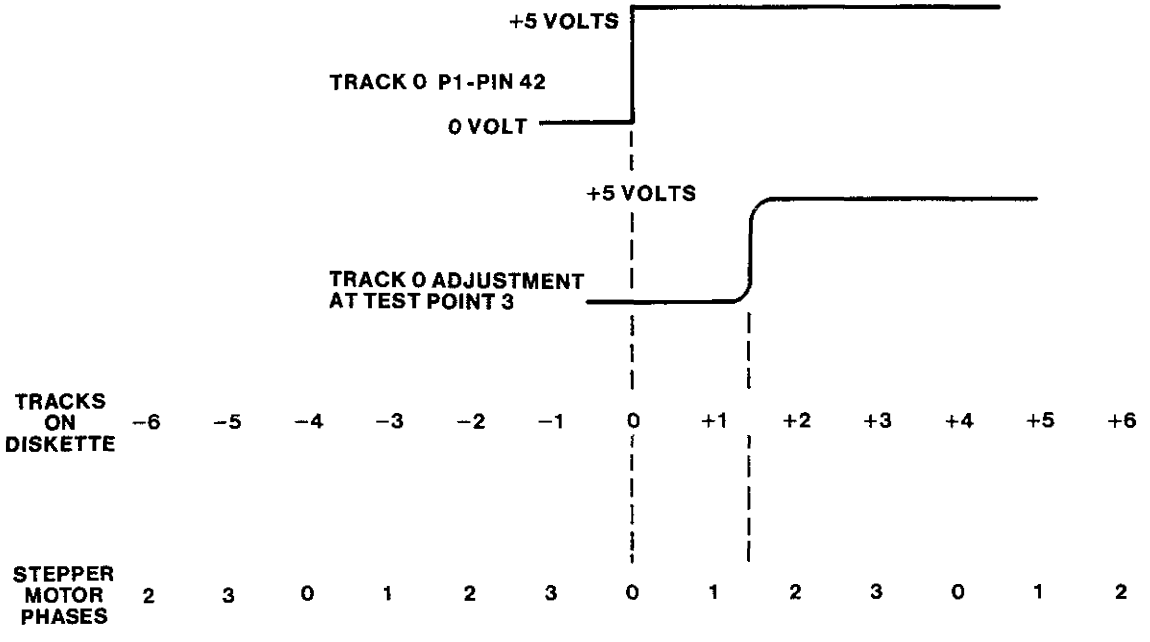


FIGURE 4-6
TRACK 0 TIMING

A low, active signal is supplied to the LSI chip, which supplies an active signal to the microprocessor and enables the input and output signals internally.

LEVER LOCK SOLENOID

When the lever lock solenoid option jumpers are installed and the drive is selected, there is a high output on Pin 16 of the microprocessor. This signal is inverted and energizes the lever lock solenoid.

4.4 READ/WRITE HEAD POSITIONER

The components of the drive required to position the read/write heads at the desired track are:

1. Step and Direction Circuits
2. Stepper Motor Control Circuits
3. Stepper Motor

STEP AND DIRECTION

The Step and Direction signals are derived from the host controller via interface connector P1, Pin 36, and P1, Pin 34, respectively.

The Step and Diection signal is supplied to the LSI chip and gated internally with drive select. If the drive is not selected, or the drive is trying to write data, step pulses are disabled.

The Step and Direction signals are then supplied to the microprocessor.

STEPPER MOTOR CONTROL

The microprocessor generates the four phases of the step sequence based on information from the step and direction inputs. These four phases are fed to the stepper motor drivers, which produce the current through the motor's coils (Figure 4-7).

STEPPER MOTOR

The stepper motor is a bipolar, four-phase motor, which rotates 1.8 degrees for each phase (Table 4-1). The capstan and split band translates this rotation to a one track linear movement of the head carriage assembly.

TABLE 4-1
STEPPER LOGIC TRUTH TABLE

Step Out Toward Track 0						Step In Toward The Inner Tracks					
Pin Number	Phase					Pin Number	Phase				
	0	3	2	1	0		0	1	2	3	0
P7-1	0	1	1	0	0	P7-1	0	0	1	1	0
P7-2	1	0	0	1	1	P7-2	1	1	0	0	1
P7-3	0	0	1	1	0	P7-3	0	1	1	0	0
P7-4	1	1	0	0	1	P7-4	1	0	0	1	1

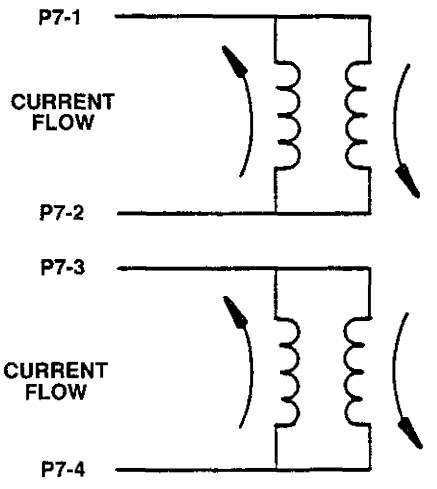


FIGURE 4-7
STEPPER MOTOR CURRENT

4.5 READ/WRITE DATA

The components of the drive required to read and write data are:

1. Read/Write Head Assembly
2. Side Select circuits
3. Write/Erase circuits
4. Read Data circuits

READ/WRITE HEAD ASSEMBLY

The read/write head(s) are glass bonded, ferrite cores mounted in a ceramic structure. The lower head structure is mounted in a fixed position to a plastic carriage. The upper head is mounted to a gimballed flexure to conform to the diskette.

The head carriage assembly is attached to the chassis on guide rails. It is positioned by a split band attached to the stepper motor.

SIDE SELECT CIRCUITS

The Side Select signal is derived from the host controller via the interface connector P1, Pin 14. If the signal is high at the interface, Side 0 is selected by applying a voltage potential on the center tap of Head 0, and allows current to flow in the coils of Head 0. If the signal at the interface is low, Side 1 is selected, by applying a voltage potential on the center tap of Head 1 allowing current to flow in the coils of Head 1.

In the read mode, a low potential is applied to the selected head diode matrix. The write mode increases the voltage applied to the selected head diode matrix to +12 VDC from the beginning of Write Gate until the end of the trim erase time.

WRITE/ERASE CIRCUITS

The write electronics consist of a write current source, Q2, a write waveform generator, an erase current source, the trim erase control, and the side select logic, U3.

The signals required to control the data electronics provided by the host controller are:

1. Drive Select
2. Write Gate
3. Write Data
4. Side Select

The winding on the head is center tapped. During a write operation, current from the write current source follows in alternate halves of the winding, under control of the write waveform genrator.

When the drive is selected and write protect is false, Write Gate initiates the write logic. Seven events occur as follows:

1. The pre-erase delay one shot is started at 190 microseconds.
2. The post-erase delay one shot is started at 550 microseconds.
3. The Inhibit (INH) signal is used to disable the read data output circuit.
4. The write current source is enabled only when the +5 volts D.C. supplied to the drive is at the correct value.
5. Input diodes to the read amplifier are reverse biased to protect the read amplifier during the write operation.
6. The write data input is used to clock the waveform generator which selects a write driver, providing a ground to forward bias a diode allowing current to flow through the coil.

When the pre-erase delay of 190-microseconds time out, the erase current source is turned on.

The clocking of the waveform generator during the write operation provides a trigger to the post-erase delay one shot, and does not allow it to time out until all data is written.

The Inhibit signal is active until the end of the post-erase delay. It keeps +12 volts D.C. on the read/write diode matrix during the erase time.

The duration of a write operation is from the true going edge of Write Gate to the false going edge of Trim Erase. This is indicated by the Inhibit waveform (Figure 4-8).

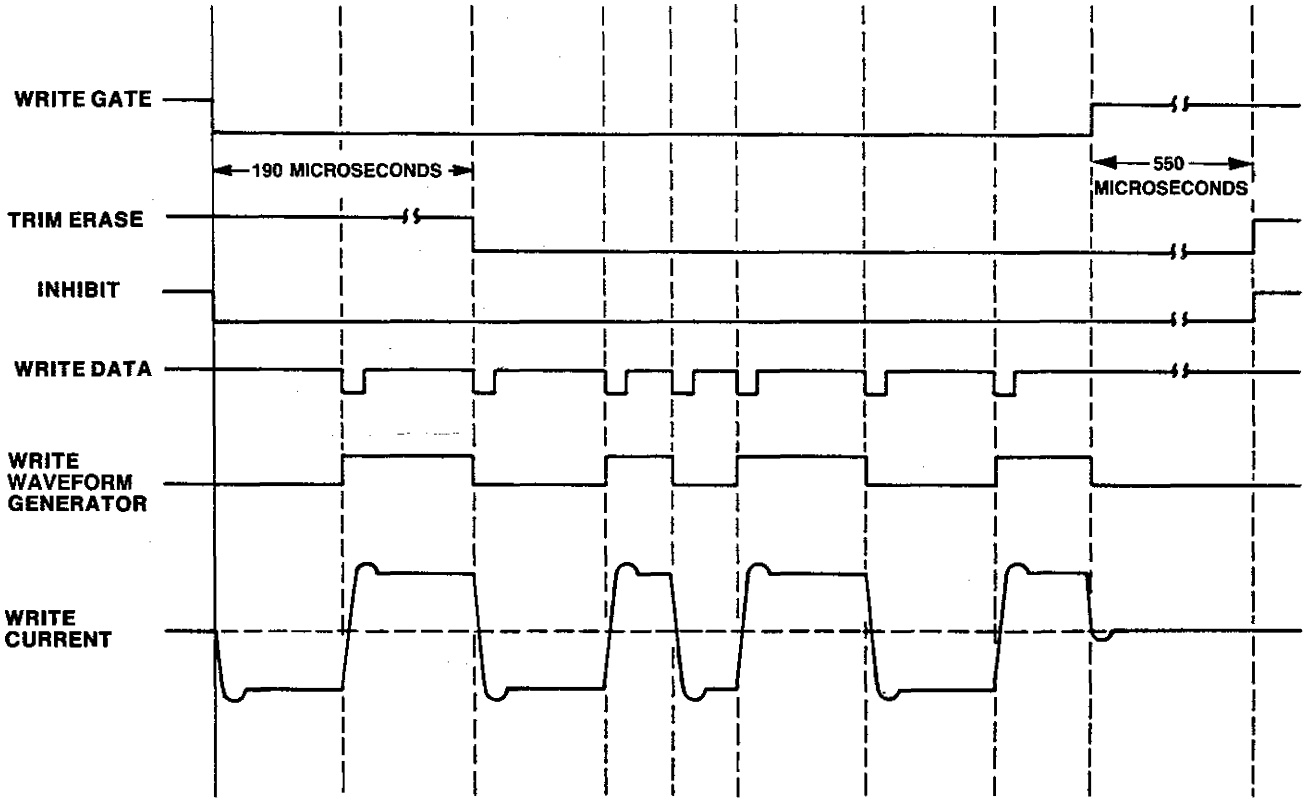


FIGURE 4-8
WRITE OPERATION TIMING DIAGRAM

READ DATA CIRCUITS

The read electronics consist of:

1. Read Only and Side Select circuit
2. Read Amplifier and Linear Phase Filter
3. Differentiator
4. Comparator, Time Domain Filter, and Digitizer

The Read only circuits are used to isolate the read amplifier from the voltage excursion across the head during a write operation. The side select is used to enable one of the read/write heads.

The output signal from the read/write head is amplified by a read amplifier, and filtered by a linear phase filter to remove noise. The linear output from the filter is passed to the differentiator, which generates a waveform whose zero crossovers correspond to the peaks of the Read signal. Then, this signal is fed to a comparator, time domain filter, and digitizer circuitry. Subsequently, the signal is supplied to the LSI chip, then to the interface.

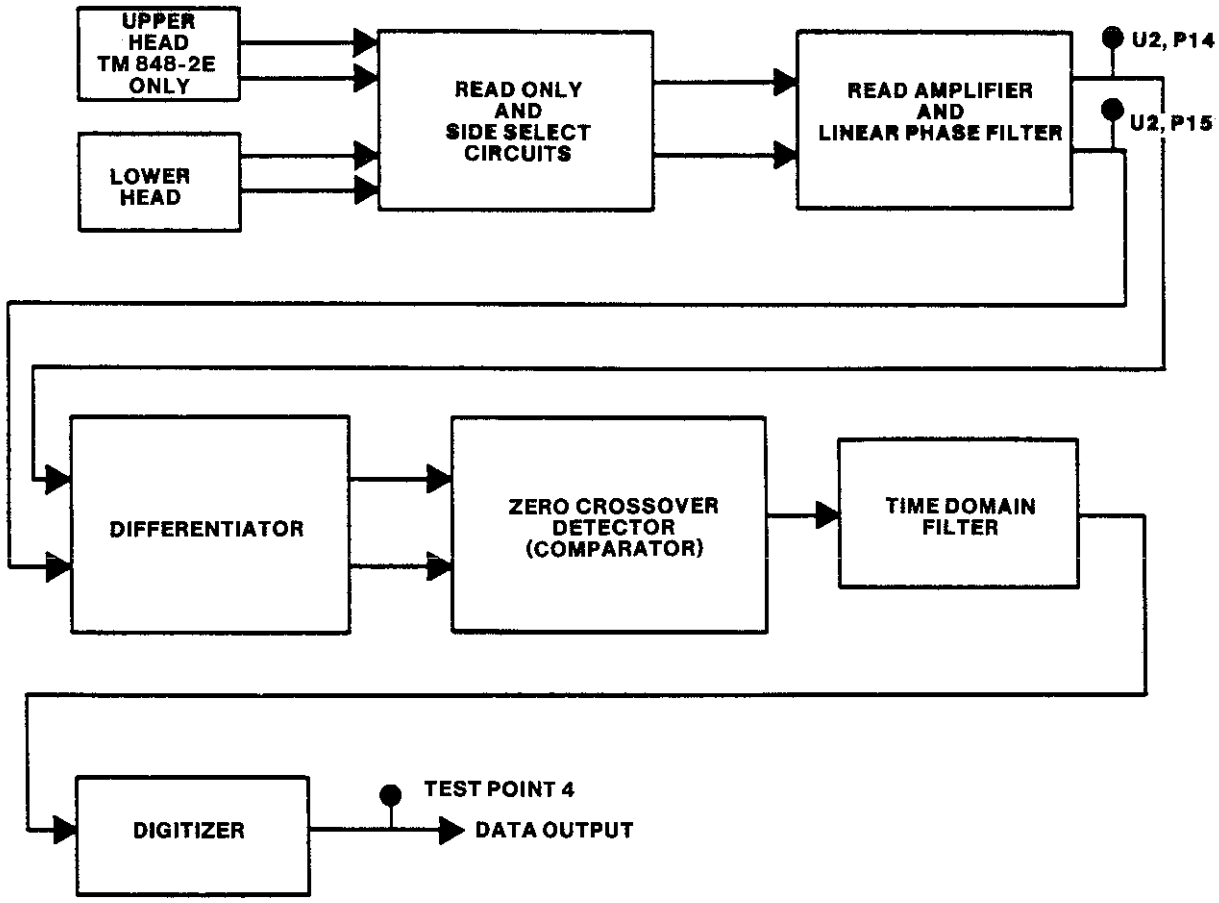


FIGURE 4-9
READ BLOCK DIAGRAM

4.6 SPINDLE CONTROL

The components of the drive required to control the spindle are:

1. Spindle Motor Enable circuit
2. Spindle Motor Control circuit

SPINDLE MOTOR ENABLE CIRCUIT

The Motor On signal is derived from the host controller to the interface connector. This signal is supplied to the LSI chip, which uses it to enable the motor current circuit of the spindle motor control.

SPINDLE MOTOR CONTROL CIRCUIT

The Motor On/Off signal turns the spindle motor current on or off. This current is controlled by a crystal phase-locked loop control circuit when the spindle motor is enabled.

SECTION 5

MAINTENANCE CHECKS AND ADJUSTMENTS

INTRODUCTION

This section is for the use of the OEM Repair and Service Departments. It contains the maintenance checks and adjustments used during the normal life of the drive. The purpose of this section is to outline the steps necessary to verify the operation of the drive during troubleshooting or after replacing a part or assembly.

If a fault is suspected with a drive, following the checks and adjustments in the order presented will help to isolate the problem area. Then, one may refer to the proper section of the troubleshooting guide. However, if a specific check and adjustment is required, the preceding checks do not necessarily need to be conducted.

The values and tolerances stated in the checks and adjustments are typical values for working drives. If the values measured are within tolerance or close to the limits, the suspected fault is normally caused by some other problem. Completing other checks and adjustments may disclose the actual problem.

Refer to the schematics and assembly drawings in the appendices, and the theory of operation in Section 4 for circuit descriptions. Test point locations are contained in Figure 5-1.

5.1 VISUAL INSPECTION

Before applying power to the drive, or doing any checks or adjustments, visually inspect the drive:

1. Check for loose or missing hardware.
2. Ensure the front lever opens and closes. The head arm raises when the door is opened.
3. Ensure the front panel is secure.
4. Manually rotate the drive motor. It should rotate freely.
5. Ensure the circuit boards are secure.
6. Ensure the connectors are firmly seated, and installed correctly.
7. Check for damaged or missing components on the circuit boards.
8. Ensure a diskette can be inserted and removed easily.

5.2 EQUIPMENT REQUIRED

The following equipment is required for checks and adjustments.

1. A dual-channel, wideband oscilloscope, Hewlett Packard Model 1740A or equivalent.
2. An exerciser, AVA Model 103C or equivalent, or a software routine capable of stepping the drive to any track, selecting the upper or lower head, and writing a 1F, all zeros in FM, or 2F, all ones in FM, pattern.
3. A power supply.
4. A certified alignment diskette, Dysan Model 360/2A or equivalent.
5. A certified output diskette, nonwrite protected, Dysan Model Number 3740/2D with tab or equivalent.
6. A certified output diskette, write protected, Dysan Model Number 3740/2D or equivalent.

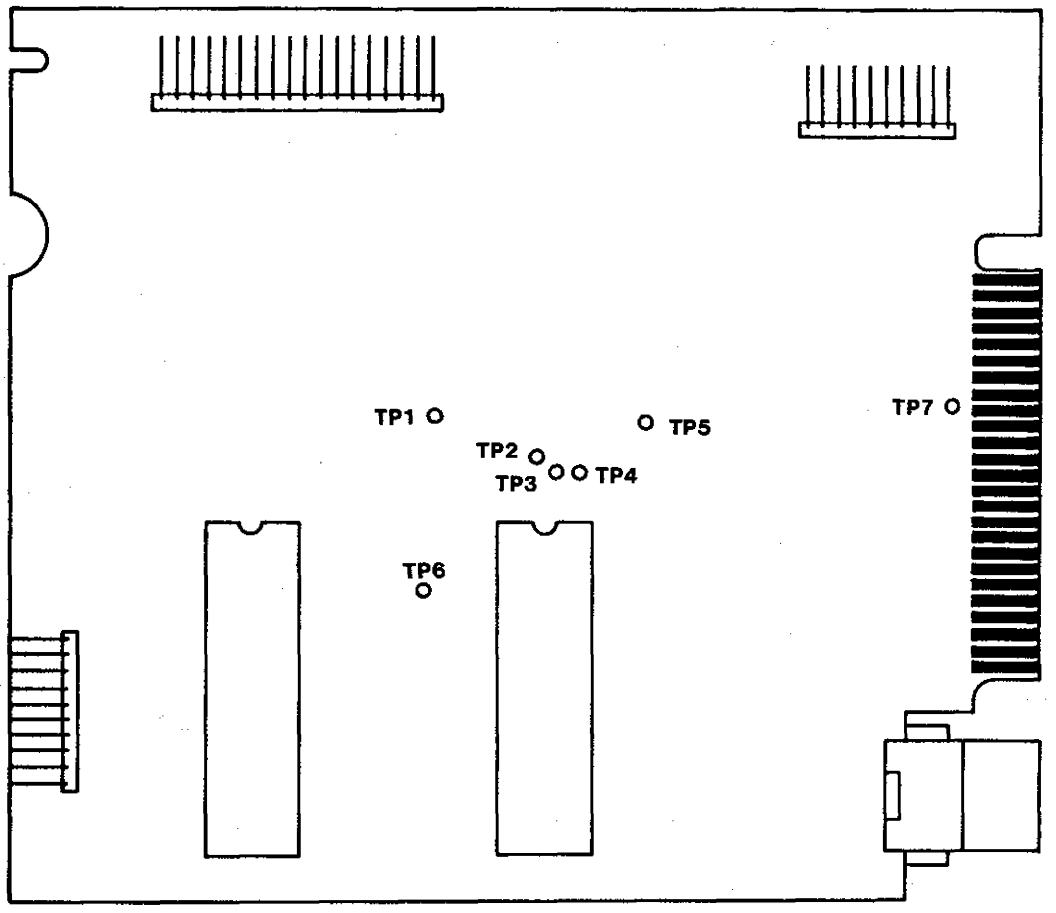


FIGURE 5-1
LOGIC CIRCUIT BOARD WITH TEST POINTS

7. Associated power and interface cables.
8. A number 1 Phillips screwdriver.
9. A number 2 Phillips screwdriver.
10. A set of Allen wrenches.
11. A flat blade screwdriver.
12. A chip clip.

Test equipment must be in calibration. This may be verified by observing the calibration due date on the calibration sticker affixed to the equipment.

5.3 POWER/DRIVE SELECT CHECK

The drive select check verifies the activity L.E.D. can be illuminated, and power is supplied to the drive. If the check fails, measure the power supply voltages to ensure they are correct, or refer to the troubleshooting guide.

1. Turn off power to the drive.
2. Connect the interface cable that goes from the exerciser to the drive.
3. Apply power to the drive.

4. Verify the power supply voltages are within tolerances.
5. Ensure a drive select jumper is in place.
6. Select the drive.
7. Verify the front panel L.E.D. is illuminated
8. Deselect the drive.
9. Ensure the front panel L.E.D. extinguishes.

5.4 WRITE PROTECT SENSOR CHECK

The write protect sensor check establishes the correct operation of the write protect sensor, i.e., the write electronics are disabled when a write protected diskette is used. If the sensor is faulty, refer to the troubleshooting guide.

1. Connect the drive to an exerciser or computer with a direct monitor of the write protect output (P1, Pin 44).
2. With a nonwrite protected diskette inserted, verify there is a nonwrite protected output to the exerciser, i.e., a high at P1, Pin 44.
3. With a write protected diskette inserted, verify there is a write protect true output to the controller or exerciser, i.e., a low at P1, Pin 44.

NOTE

A defective circuit board can be responsible for a write protect problem. Test Point 5 should be high for a write protected diskette, low for a nonwrite protected diskette.

5.5 DRIVE MOTOR SPEED CHECK

The drive motor's speed check ensures the speed is within the specified tolerance. The motor speed is 360 RPM ± 1.5 percent. If the motor speed is out of tolerance, refer to the troubleshooting guide.

1. Apply power to the drive.
2. Insert a work diskette.
3. Activate the drive motor.
4. Observe the timing disk on the drive motor under ambient fluorescent lighting (Figure 5-2).
5. Verify the 60 Hertz ring is stationary.

5.6 RADIAL TRACK ALIGNMENT CHECK AND ADJUSTMENT

The Radial Track alignment procedure locates the read/write head at the proper radial distance on the hub center line, ensuring the track location is accurate (Figure 5-3). Adjustment is necessary only after servicing or if diskette interchange problems are suspected. If the cats eye pattern cannot be verified or cannot be adjusted, refer to the troubleshooting guide.

NOTE

Alignment diskette and drive must be allowed to stabilize at room temperature for one hour before checks and adjustments are made.

RADIAL TRACK ALIGNMENT CHECK

1. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

   Ground: Test Point 8

   Read Differentially: A plus B, B inverted

   Time Base: 20 milliseconds per division

   External Trigger: Test Point 10, positive edge

2. Adjust the amplitude for at least four divisions on the oscilloscope.
3. Apply power to the drive.

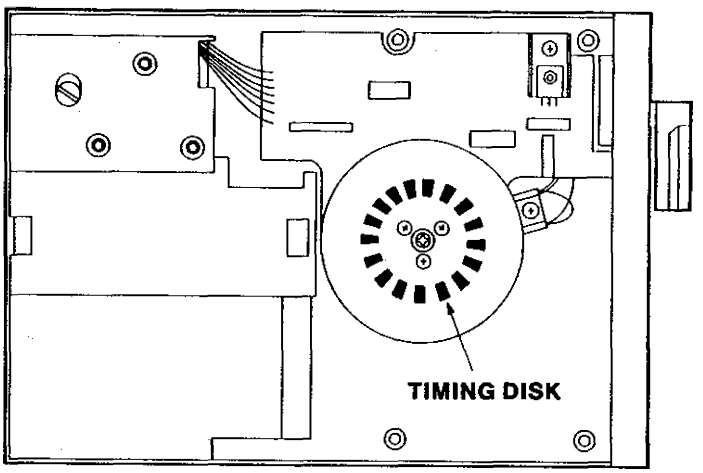


FIGURE 5-2
TIMING DISK

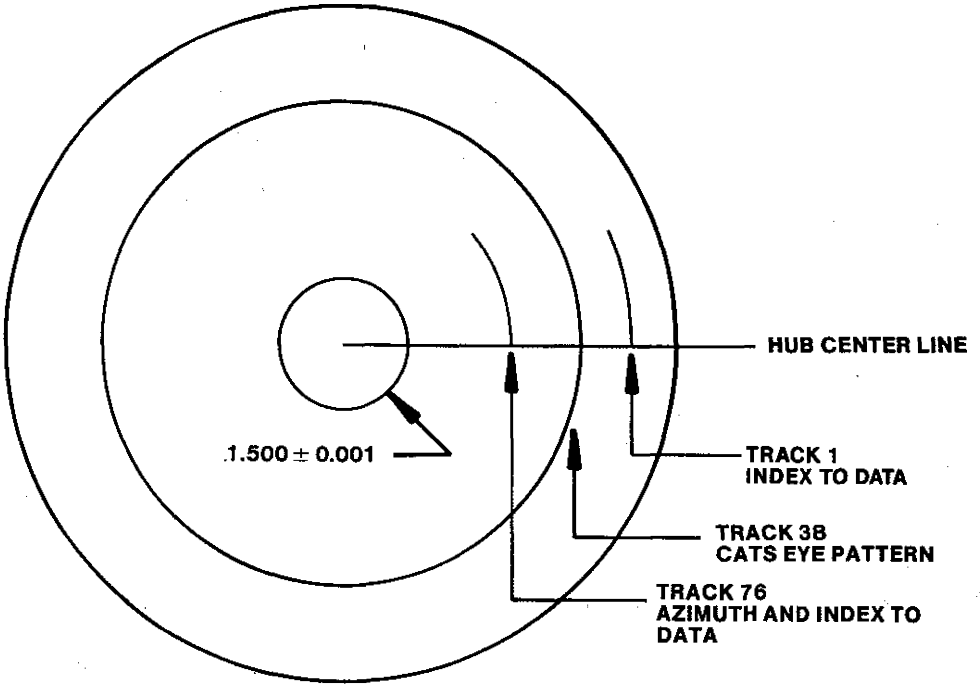


FIGURE 5-3
HUB CENTER LINE AND TRACK LOCATION

NOTE

The Track 38 radius is 2.8207 ± .0020 inches from the center of the hub. Other track locations are computed based upon 48 TPI.

4. Select the drive.

5. Insert a Radial Track alignment diskette, Dysan Number 360/2A, into the drive.

6. Select Head 0, the lower head.

7. Read Track 38 for Radial Track alignment of the lower head.

8. Adjust the oscilloscope to observe a Cats Eye pattern (Figure 5-4).

9. Verify the smaller of the two Cats Eye patterns is not less than 75 percent in amplitude of the other one.

NOTE

The 75 percent figure is for use with an alignment diskette verified against a standard alignment diskette.

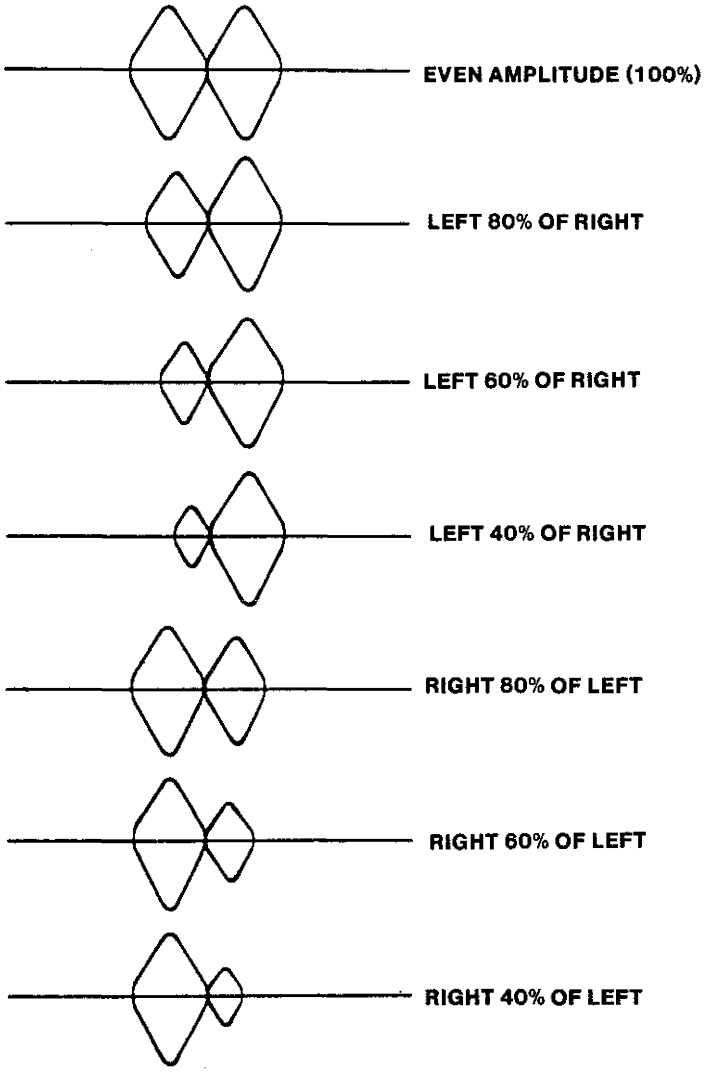


FIGURE 5-4
CATS EYE PATTERNS

10. Step the drive to Track 0, then step it back to Track 38.

11. Verify the Cats Eye pattern.

12. Step the drive to Track 42 or higher; then, step it back to Track 38.

13. Verify the Cats Eye pattern.

14. Switch to Head 1, the upper head.

15. Read Track 38 to verify the alignment of the upper head, if applicable.

16. Verify the Cats Eye pattern.

17. Step the drive to Track 0; then, step it back to Track 38.

18. Verify the Cats Eye pattern.

19. Step the drive to Track 42 or higher; then, step it back to Track 38.

20. Verify the Cats Eye pattern.

21. If all the checks verify, the Radial Track alignment is acceptable.

22. If any check does not verify, the head carriage mst be adjusted.

RADIAL TRACK ALIGNMENT ADJUSTMENT

1. Loosen the three head carriage retaining screws one-half turn with an Allen wrench (Figure 5-5).

2. Turn the cam screw counterclockwise.

3. Observe the Cats Eye pattern of the head farthest out of alignment.

4. Turn the cam screw until the Cats Eye patterns are equal in amplitude (Figure 5-4).

5. Tighten the carriage retaining screws with an Allen wrench.

6. Recheck the Radial Track alignment.

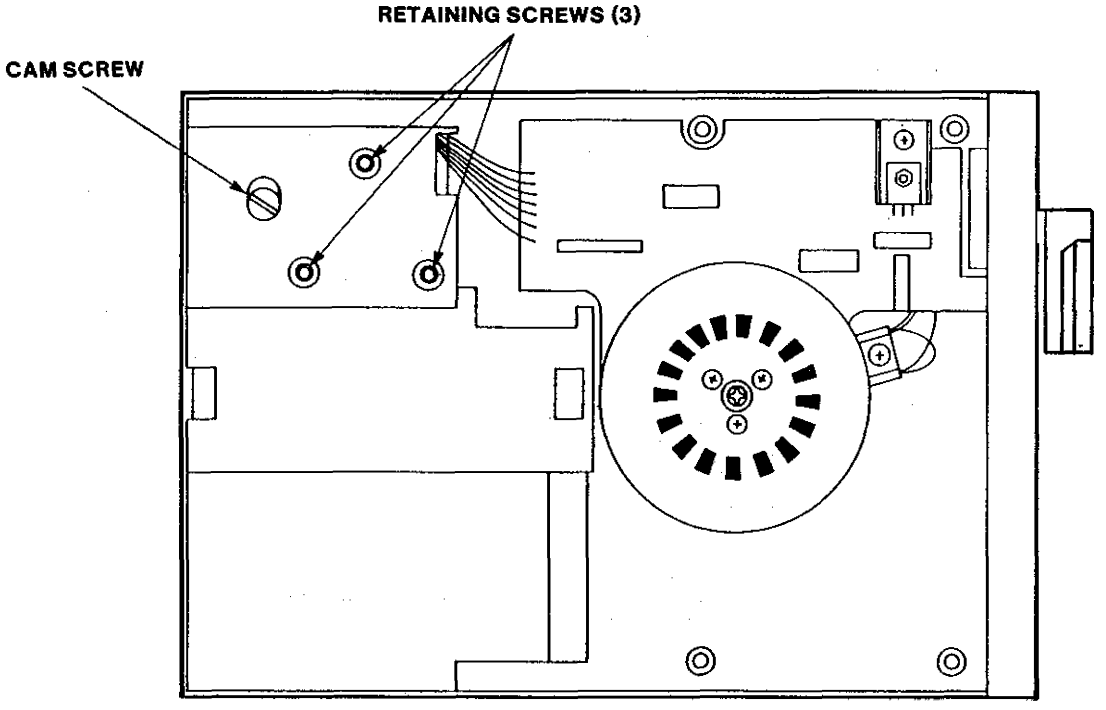


FIGURE 5-5
HEAD CARRIAGE RETAINING AND CAM SCREWS

5.7 INDEX CHECKS AND ADJUSTMENT

The index adjustment changes the time period from the index pulse to the start of the data in hard sectored diskettes. The adjustment should be checked after the drive has been aligned or when diskette interchange errors are suspected. If the index checks and adjustments fail, refer to the troubleshooting guide.

INDEX-TO-DATA BURST CHECK

1. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

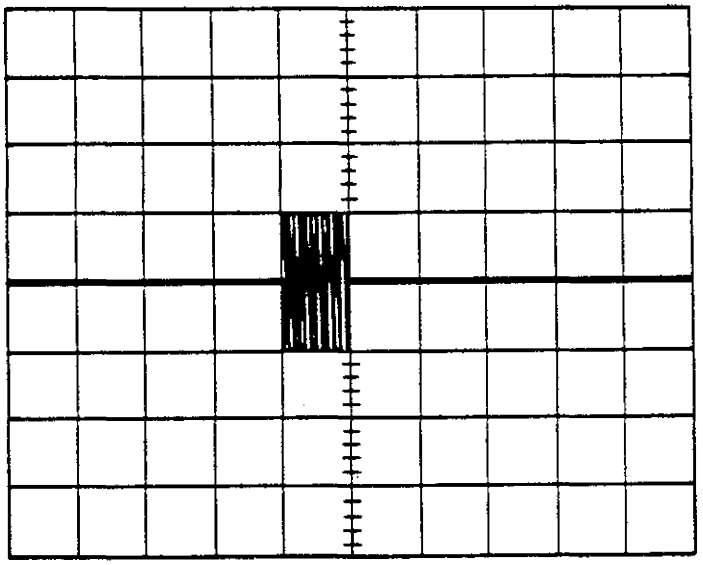
   Ground: Test Point 8

   Read Differentially: A plus B, B inverted

   Time Base: 50 microseconds per division

   External Trigger: Test Point 10, positive edge

2. Adjust the amplitude for at least two divisions on the oscilloscope.
3. Apply power to the drive.
4. Select the drive.
5. Check the motor speed of the drive.
6. Insert an alignment diskette.
7. Seek to Track 1.
8. Select Head 0, the lower head.
9. Ensure the index-to-data burst occurs at 200 ± 100 microseconds from the leading edge of the index pulse (Figure 5-6).
10. For double-sided drives, select Head 1, and repeat the steps above.



TIME SCALE: 50 MICROSECONDS PER DIVISION

FIGURE 5-6
INDEX-TO-DATA BURST

NOTE

Head 1 should meet the same tolerance.

11. If either Head 0 or Head 1 does not meet the tolerance, adjust the index sensor.

12. When both index measurements on a double-sided drive or the one index measurement on a single-sided drive meet the tolerance, check the index-to-data burst on Track 76.

13. On a double-sided drive, check Heads 1 and 0, the upper and lower heads.

NOTE

If any index measurement does not meet the tolerance, the index sensor must be adjusted.

Index Sensor Adjustment

1. Loosen the index sensor's retaining screw located on the underside of the chassis (Figure 5-7).

2. Adjust the index sensor with a flat blade screwdriver until the index-to-data burst occurs 200 ± 100 microseconds from the leading edge of the index pulse.

3. Tighten the index sensor's retaining screw.

4. Recheck the index-to-data bursts.

5.8 AZIMUTH CHECK

Azimuth checks the read/write head(s) relative angle to the center line of the diskette. The Dysan 360/2A alignment diskette has three azimuth bursts, with the first burst having acceptable limits of 12 minutes, the second one of 15 minutes, and the third one of 18 minutes. The third burst of 18 minutes should be used for the check.

The head(s) azimuth is not adjustable. If the head(s) fail the azimuth check, replace the module assembly.

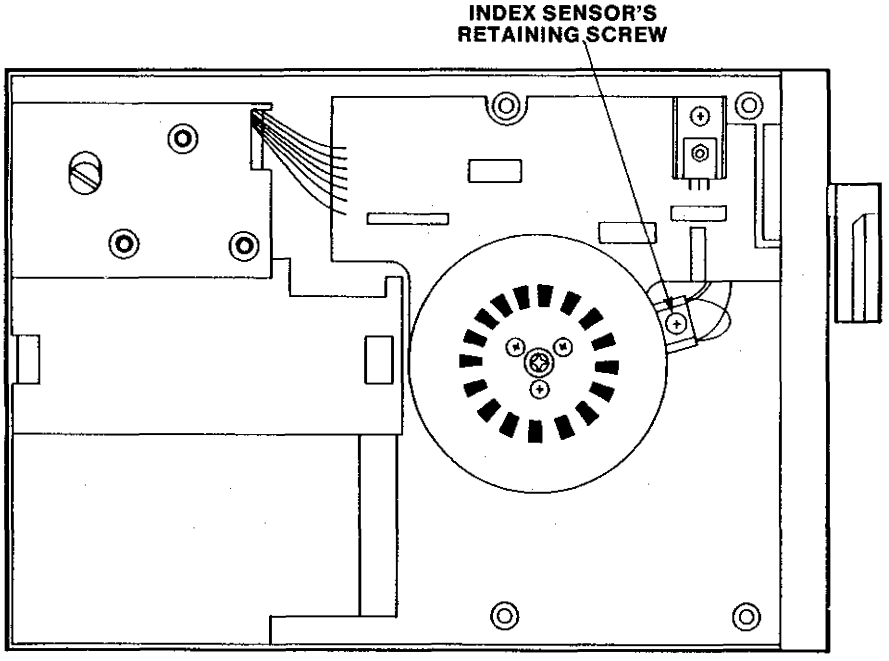


FIGURE 5-7
INDEX SENSOR'S RETAINING SCREW

1. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

   Ground: Test Point 8

   Read Differentially: A plus B, B inverted

   Time Base: 0.5 millisecond per division

   External Trigger: Test Point 10, positive edge

2. Adjust the amplitude for at least four divisions on the oscilloscope.

3. Seek to Track 76.

4. Select Head 0, and observe the third pulse burst on the oscilloscope.

5. Verify the head azimuth is no greater than ± 18 minutes by comparing the third set of pulse bursts to those in Figures 5-8, 5-9, and 5-10.

6. Select Head 1, and verify the head azimuth.

Figure 5-8 depicts an azimuth of exactly zero minutes. This is the optimum head azimuth alignment.

Figure 5-9 depicts an azimuth of exactly minus 18 minutes. This is the lower limit of allowable azimuth error.

Figure 5-10 depicts an alignment of exactly plus 18 minutes. This is the upper limit of allowable azimuth error.

5.9 TRACK 0 SENSOR CHECK AND ADJUSTMENT

The Track 0 sensor provides a signal identifying Track 0 to the LSI chip. The electronics disable the step-out function when Track 0 is reached. In addition, a Track 0 signal is sent to the controller on Pin 42 of the interface. If the Track 0 sensor cannot be adjusted, refer to the troubleshooting guide.

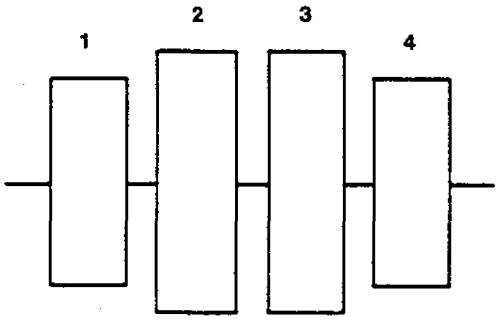


FIGURE 5-8
OPTIMUM HEAD AZIMUTH ALIGNMENT

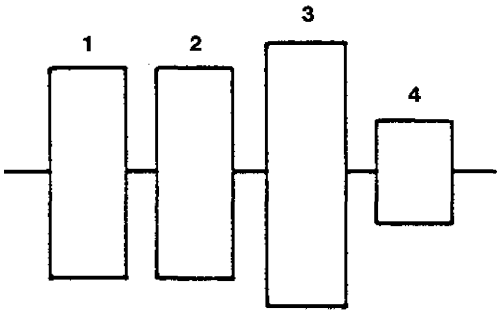


FIGURE 5-9
HEAD AZIMUTH ALIGNMENT
OF ACCEPTABLE LOWER LIMITS

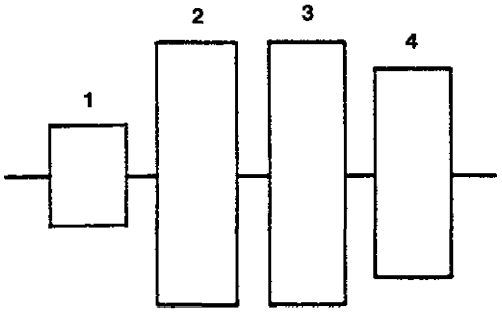


FIGURE 5-10
HEAD AZIMUTH ALIGNMENT
OF ACCEPTABLE UPPER LIMITS

TRACK 0 SENSOR CHECK

1. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

   Ground: Test Point 8

   Read Differentially: A plus B, B inverted

   Time Base: 20 milliseconds per division

   External Trigger: Test Point 10, positive edge

   Vertical Display: 0.1 volt per division

2. Apply power to the drive.

3. Insert an alignment diskette into the drive.

4. Close the front lever.

5. Step the carriage to the radial alignment track.

6. Confirm the position by observing the Cats Eye pattern.

7. Set up the oscilloscope to monitor the signal at Test Point 3.

8. Step the carriage to Track 1.

9. Ensure the signal at Track 1 is less than 0.5 volts.

10. Step the carriage out to the radial alignment track.

11. Step the carriage back to Track 2.

12. Verify the logic level at Test Point 3 is at least 2.5 volts.

13. If all of these checks are satisfactory, no adjustment is required.

14. If any of these checks is unsatisfactory, adjust the Track 0 switch.

TRACK 0 SENSOR ADJUSTMENT

1. Loosen the retaining screw on the base of the Track 0 bracket (Figure 5-11).

2. Retighten the screw slightly to provide some friction on the bracket.

3. Slide the Track 0 Sensor toward the rear of the chassis as far as it will go without forcing it.

4. Step the carriage back from the radial alignment track to Track 1, but do not restore it to Track 0.

5. Slide the Track 0 Sensor forward very slowly until the signal at Test Point 3 is less than 0.5 volts at Track 1 and greater than 2.5 volts at Track 2.

6. Retighten the retaining screw.

7. Repeat the Track 0 Sensor check to ensure the correct setting has been attained.

5.10 HEAD OUTPUT CHECK

The head output check measures the head's output amplitude relative to the diskette being used. When using certified, quality media, typical values will be 200 millivolts peak to peak or greater. However, values may be significantly less, 100 millivolts peak to peak typical, if inferior or defective media is used, and does not indicate a faulty head.

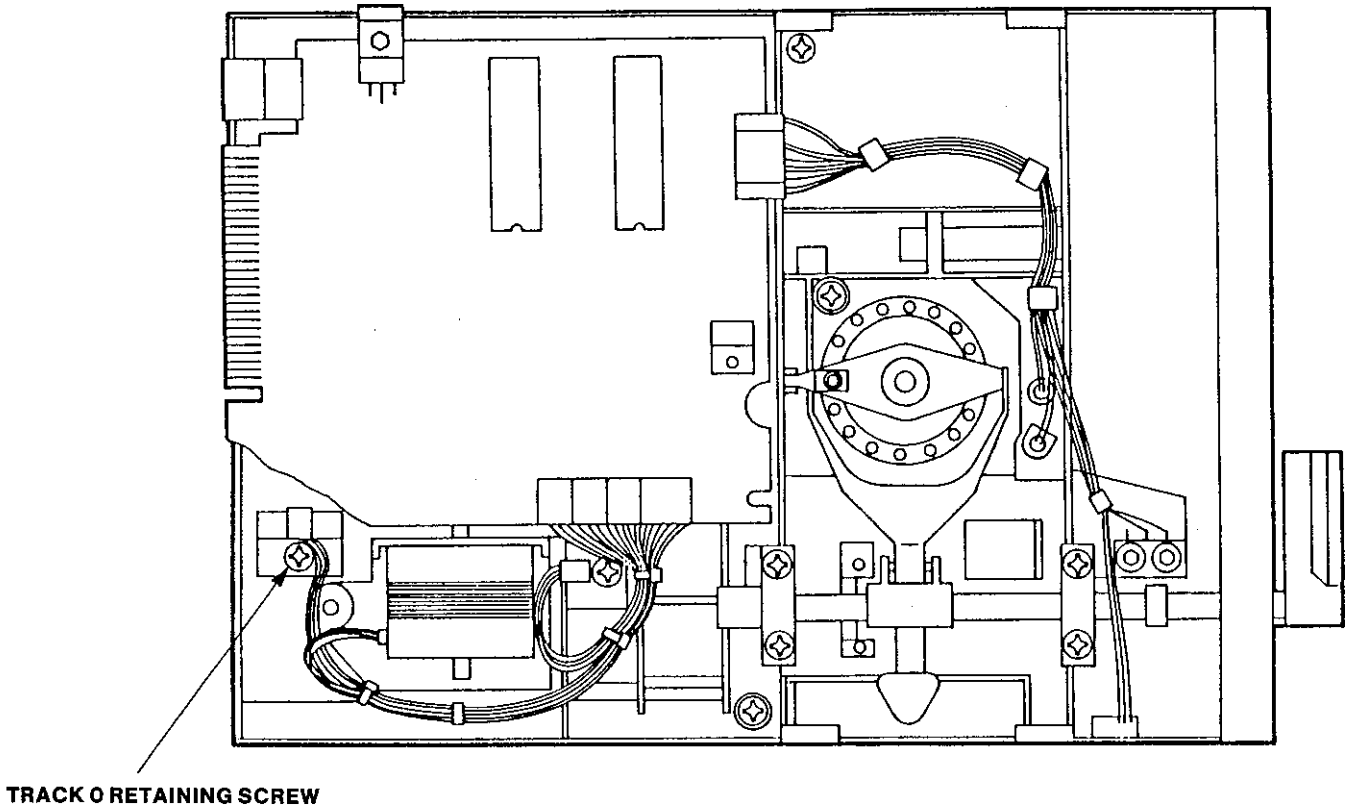


FIGURE 5-11
TRACK 0 RETAINING SCREW

Head amplitude can be verified by establishing a nominal value of amplitude for the diskette on a known working drive. In all cases, amplitudes above 200 millivolts peak to peak are acceptable. If head amplitude is suspected as being faulty, refer to the troubleshooting guide.

1. Remove the alignment diskette, and insert a nonwrite protected diskette into the drive.

2. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

   Vertical Amplitude: 50 millivolts per division

   Ground: Test Point 8

   Read Differentially: A plus B, B inverted

   Time Base: 20 milliseconds per division

   External Trigger: Test Point 10, positive edge

3. Seek to Track 0.

4. Write a 2F, all ones, pattern on Head 0.

5. Verify the amplitude is 200 millivolts or greater, peak-to-peak.

6. Write a 2F, all ones, pattern on Head 1.

7. Verify the amplitude is 200 millivolts or greater, peak-to-peak.

5.11 CONE CENTERING CHECK

Cone centering is the ability of the cone clamping mechanism to center the diskette on the hub causing it to rotate concentrically. This check should be made whenever the cone lever assembly has been removed or replaced. If cone centering cannot be achieved, verify the measurement with a second diskette. Otherwise refer to the troubleshooting guide.

1. Set up the oscilloscope to read:

   Channel A: U2, Pin 14

   Channel B: U2, Pin 15

   Vertical Amplitude: 50 millivolts per division

   Ground: Test Point 8

   Read Differentially: A and B, B inverted

   Time Base: 10 microseconds per division

   External Trigger: Test Point 10, positive edge

2. Apply power to the drive.
3. Select the drive.
4. Seek to Track 0.
5. Write a 2F pattern on Head 0.
6. Measure the amplitude of the signal by positioning the deepest dip in the signal on the center vertical graticule.
7. Release the front lever, and remove the diskette.
8. Reinsert the diskette, and close the front lever.
9. Repeat Steps 7 and 8 until the deepest dip in the waveform is produced.
10. Measure the amplitude of the deepest dip.
11. Divide this measurement by the measurement in Step 6, and multiply it by 100. This result should be above 85 percent.
12. The signal amplitude should not decrease below 85 percent of the average amplitude at any point on the track.

SECTION 6

TROUBLESHOOTING GUIDE AND REPLACEMENT PROCEDURES

INTRODUCTION

This section is designed to help locate and correct failures related to the drive. Table 6-1 is a troubleshooting guide outlining the problem, its possible cause, and the recommended action. This section also contains parts removal and replacement procedures.

The recommended spare parts list and assembly drawings in Appendix A are useful when replacing assemblies. In addition, the checks and adjustment procedures in Section 5 must be used to verify proper installation and ensure the drive's performance.

6.1 SYMPTOM DIAGNOSTIC TECHNIQUES

When trying to diagnose a fault attributed to drive failure, a visual inspection of the drive may reveal an obvious misalignment or broken part on the drive. Always check the power supply voltages before proceeding with the troubleshooting guide.

In some cases, errors attributed to the drive actually may be caused by incorrect operating procedures, faulty system programming, incorrect drive option patching, and damaged or incorrect certified diskettes. Review Section 3 to ensure correct configuration of the drive.

6.2 SOFT ERRORS

Soft errors can be caused by airborne contaminants, random electrical noise, excessive temperature, and other external causes. To correct soft errors:

1. Ensure proper grounding between power supply, drive, and host system.
2. Verify there is no random electrical noise to the drive.
3. Verify there is no radiated noise to the drive.
4. Ensure temperature in the vicinity of the drive is within specification.
5. Try to verify and duplicate the fault on a second diskette.
6. Usually, quality media is sufficient to clean the heads. When contamination of the heads is extreme due to poor quality media or airborne contaminants, cleaning diskettes may be used in accordance with the manufacturer's instructions.

CAUTION

Do not use cotton swabs, solvents, or otherwise clean the heads by hand since damage to the heads may result.

6.3 TROUBLESHOOTING GUIDE

The troubleshooting guide is presented in the form of a table. The table includes:

1. A statement representing the condition.
2. A list of possible causes.
3. The recommended action to be taken.

NOTE

Check the power supply voltages to ensure they are within specification before proceeding with the troubleshooting guide.

TABLE 6-1
TROUBLESHOOTING GUIDE

Condition	Possible Cause	Recommended Action
No index.	Diskette not inserted.	Insert diskette.
	Lever not closed.	Close lever.
	Unit not selected.	Verify unit select and jumper configuration.
	Index sensor not connected.	Check P4.
	Index sensor defective.	Replace index sensor.
	Spindle not turning.	See: Spindle Not Turning.
	Defective Logic circuit board.	Replace logic circuit board.
Spindle speed out of tolerance or spindle not turning.	Drive Motor not turning.	Verify interface motor on signal. Verify Motor Control option jumpers.
	Connector loose or disconnected.	Check connector P6.
	Defective Servo circuit board.	Replace Drive Motor Assembly.
	Defective Logic circuit board.	Replace Logic circuit board.
	Defective drive motor.	Replace Drive Motor Assembly.
Will not seek or restore.	Interface not enabled.	Verify interface direction, step, and select signals.
	Connector loose or disconnected.	Check Connector P7.
	Defective step logic.	Replace Logic circuit board.
	Defective stepper motor.	Replace Stepper Motor Assembly.

TABLE 6-1
TROUBLESHOOTING GUIDE (CONTINUED)

Condition	Possible Cause	Recommended Action
Will not write.	Diskette is write protected.	Install write tab on diskette.
	Interface not enabled.	Verify write enable, select, and write data interface lines.
	Head(s) or write protect sensor not connected.	Check Connectors P8, P9, and P10.
	Write protect sensor faulty.	Check write protect sensor operation.
	Defective write logic.	Replace Logic circuit board.
	Defective head(s).	Replace Head Carriage Assembly.
Will not read.	Interface incorrect.	Verify select is true and write enable is false.
	Alignment off.	Verify Radial Track alignment index pulse, and Track 0 sensor adjustment.
	Defective read electronics.	Replace Logic circuit board.
	Defective head(s).	Replace Head Carriage Assembly.
No Track 0 indication.	Defective seek.	See: Will not seek or restore.
	Track 0 sensor not loose or disconnected.	Check P11.
	Track 0 sensor not adjusted.	Adjust Track 0 sensor.
	Defective logic.	Replace Logic circuit board.
	Defective Track 0 sensor.	Replace Track 0 Sensor Assembly.

TABLE 6-1
TROUBLESHOOTING GUIDE (CONTINUED)

Condition	Possible Cause	Recommended Action
Fails drive select check.	Power not applied to the drive.	Verify power supply voltages.
	Drive not selected.	Verify proper jumper configuration (see Section 3).
	Faulty activity L. E. D.	Replace activity L. E. D.
	Faulty Logic circuit board.	Replace Logic circuit board.
Fails write protect sensor check.	Defective write protect sensor.	Replace write protect sensor.
	Faulty Logic circuit board.	Replace Logic circuit board.
Fails drive motor speed check.	— —	See: Spindle speed out of tolerance or not turning.
Fails Radial Track alignment check and adjustment.	Cannot read.	See: Will not read.
	Cannot step.	See: Will not seek or restore.
	Track 0 sensor misadjusted.	Perform Track 0 switch adjustment procedure.
	Alignment diskette defective.	Verify alignment diskette and replace if necessary.

TABLE 6-1
TROUBLESHOOTING GUIDE (CONTINUED)

Condition	Possible Cause	Recommended Action
Fails Index checks and adjustment.	— —	See: No index.
	Diskette not centering.	See: Fails centering check.
	Alignment diskette defective.	Verify alignment diskette and replace if necessary.
Fails Track 0 sensor check and adjustment.	— —	See: No Track 0 indication.
Fails head output check.	Defective media.	Replace media.
	Cannot read.	See: Will not read.
Fails cone centering check.	Defective diskette.	Replace diskette.
	Defective Cone Assembly.	Replace Cone Assembly.
	Defective Bridge Assembly.	Replace Bridge Assembly.
	Defective drive motor.	Replace drive motor.

6.4 REPLACEMENT PROCEDURES

This section contains the replacement procedures for the major parts and assemblies. After replacing a part or assembly, perform the appropriate check and adjustment recommended in Table 6-2. Checks and adjustment procedures are in Section 5.

TABLE 6-2
CHECKS AND ADJUSTMENT GUIDE

PARTS OR ASSEMBLIES REPLACED	RECOMMENDED CHECKS AND ADJUSTMENTS									
	POWER/DRIVE SELECT CHECK	WRITE PROTECT SENSOR	DRIVE MOTOR SPEED	RADIAL TRACK ALIGNMENT	INDEX	AZIMUTH	TRACK 0 SENSOR	HEAD OUTPUT	CONE CENTERING	
Logic Circuit Board	X		X					X		
Cone Assembly					X				X	
Diskette Lever Assembly										
Front Panel	X									
Bridge Assembly					X				X	
Drive Motor Assembly	X		X						X	
Load Arm Assembly								X		
Track 0 Sensor							X			
Write Protect Sensor		X								
Motor Switch Assembly	X		X							
Index Sensor Assembly					X					
Diskette Ejector Assembly									X	
Ejector Spring									X	
Stepper Band				X	X	X	X			
Stepper Motor Assembly				X	X	X	X			
Head Carriage Assembly				X	X	X	X	X		

LOGIC CIRCUIT BOARD

REMOVAL

1. Remove all connectors from the circuit board (Figure 6-1). Note their location.
2. Remove the two circuit board mounting screws.
3. Slide the circuit board toward the back of the drive about one-half inch.
4. Remove it from the drive.

REPLACEMENT

1. Place the new circuit board on the drive.
2. Install the two mounting screws attaching the circuit board to the rails.
3. Plug in all connectors, ensuring they are in the proper slots.
4. Perform all checks indicated in Table 6-2.

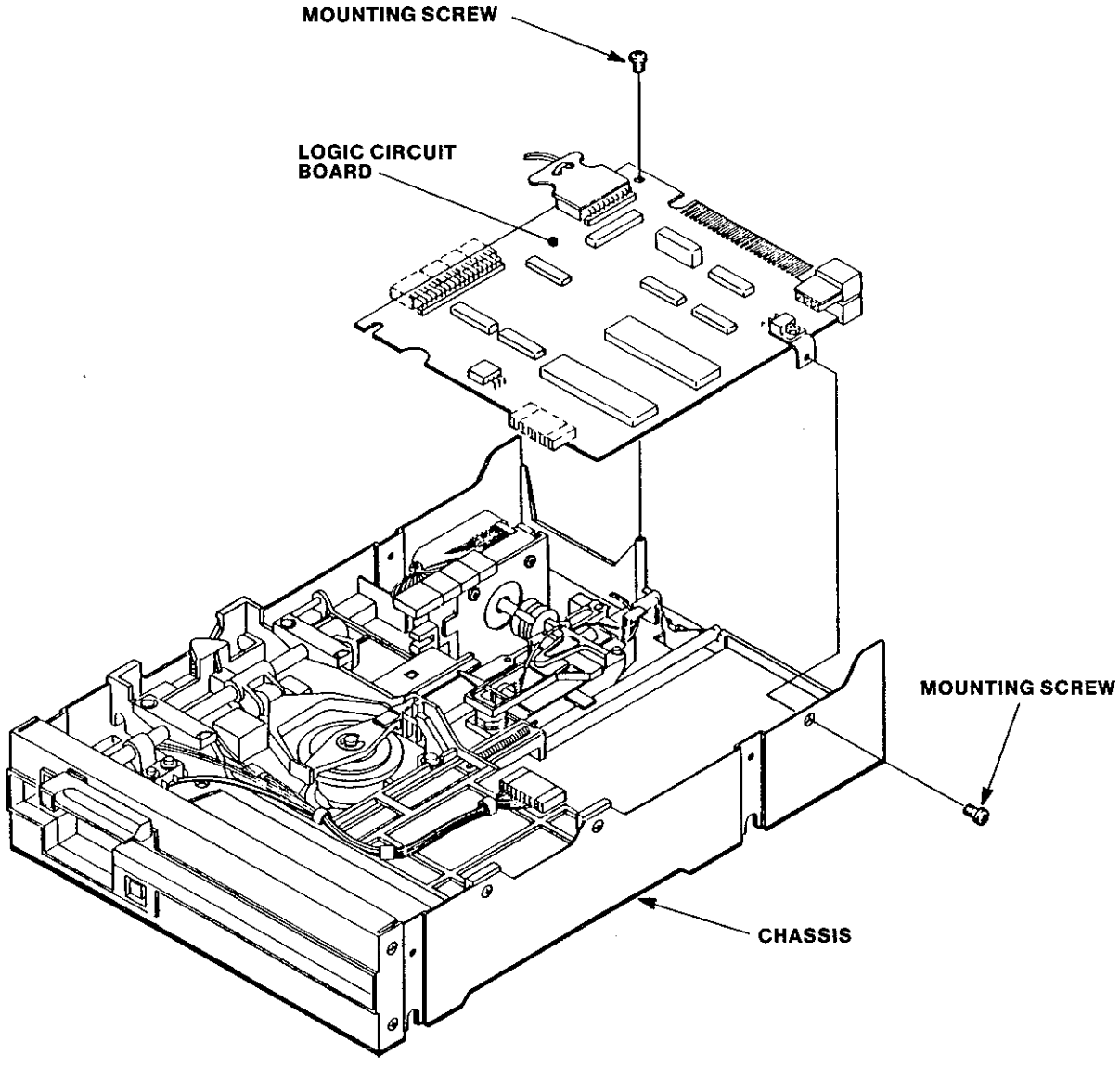


FIGURE 6-1
LOGIC CIRCUIT BOARD CONNECTORS AND MOUNTING SCREWS

CONE ASSEMBLY

REMOVAL

1. Remove the screw that attaches the cone bracket to the cone alignment arm (Figure 6-2).

2. Unlatch the diskette lever.

3. Swing the Cone Assembly up 90 degrees so that it points toward the side of the drive.

4. Carefully remove the E-Ring, flat washer, and washer that holds on the cone shaft.

5. Gently lift out the Cone Assembly.

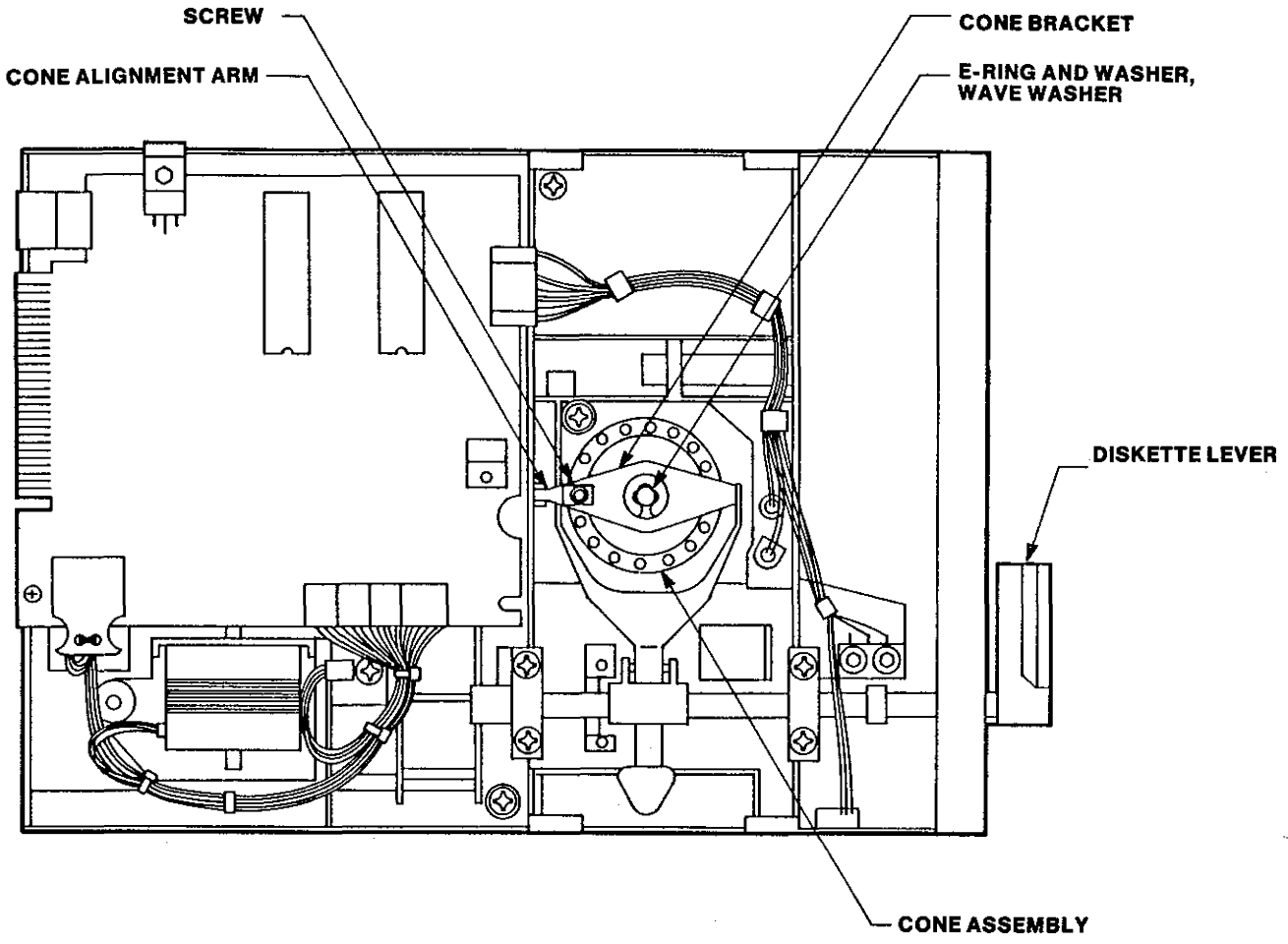


FIGURE 6-2
CONE BRACKET

INSTALLATION

1. Gently insert the Cone Assembly.
2. Carefully insert the E-Ring, flat washer, and wave washer that holds on the cone shaft (see Figure 6-3).
3. Swing the Cone Assembly down 90 degrees so that it points toward the bottom of the unit.
4. Latch the diskette lever.
5. Insert the screw that attaches the cone bracket to the cone alignment arm (Figure 6-2).
6. Ensure the Cone Assembly turns freely.
7. If not, reverify that the Cone Assembly has been installed correctly.
8. Insert a diskette.
9. Ensure the diskette is clamped properly by the cone.
10. Perform the checks and adjustments indicated in Table 6-2.

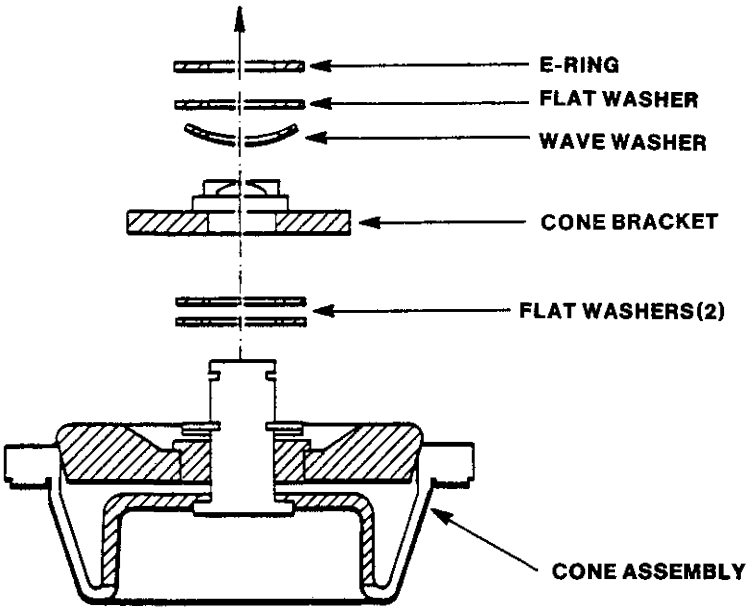


FIGURE 6-3
CONE ASSEMBLY

DISKETTE LEVER

REMOVAL

1. Pry off the cover that hides the diskette lever's retaining screw (Figure 6-4).
2. Remove the diskette lever's retaining screw.
3. Carefully remove the diskette lever.

INSTALLATION

1. Put the diskette lever on the shaft.
2. Put a drop of Locktite Number 234 on the threads of the diskette lever's screw.
3. Install and tighten the diskette lever's screw.
4. Put the cover back on the diskette lever.
5. Ensure the diskette lever is perpendicular to the drive when the diskette is clamped.
6. Ensure the diskette lever is parallel to the drive when the diskette is unclamped.

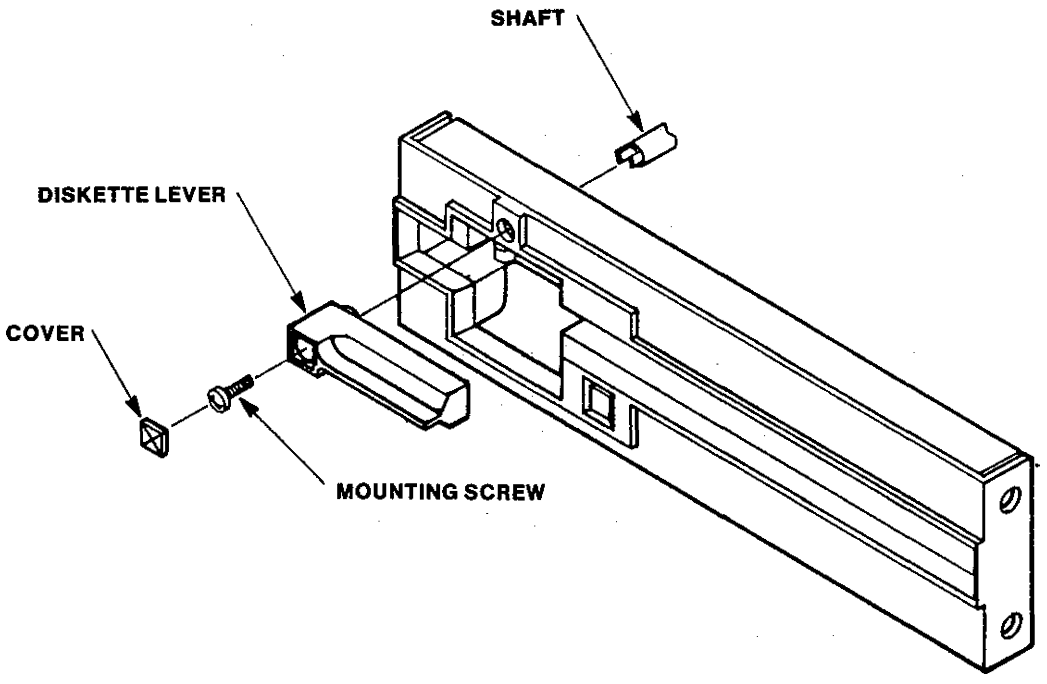


FIGURE 6-4
DISKETTE LEVER

FRONT PANEL

REMOVAL

1. Remove the diskette lever.
2. Remove the four mounting screws, two on each side, that attach the front panel to the chassis (Figure 6-5).
3. Lift off the front panel, being careful that the Activity L.E.D. comes out of its mounting with no binding.

INSTALLATION

1. Put the front panel on the drive, ensuring the Activity L.E.D. goes into its holder.
2. Install the four mounting screws attaching the front panel to the chassis.
3. Reinstall the diskette lever.
4. Ensure the diskette lever clamps the cone and loads the heads.
5. Perform the checks indicated in Table 6-2.

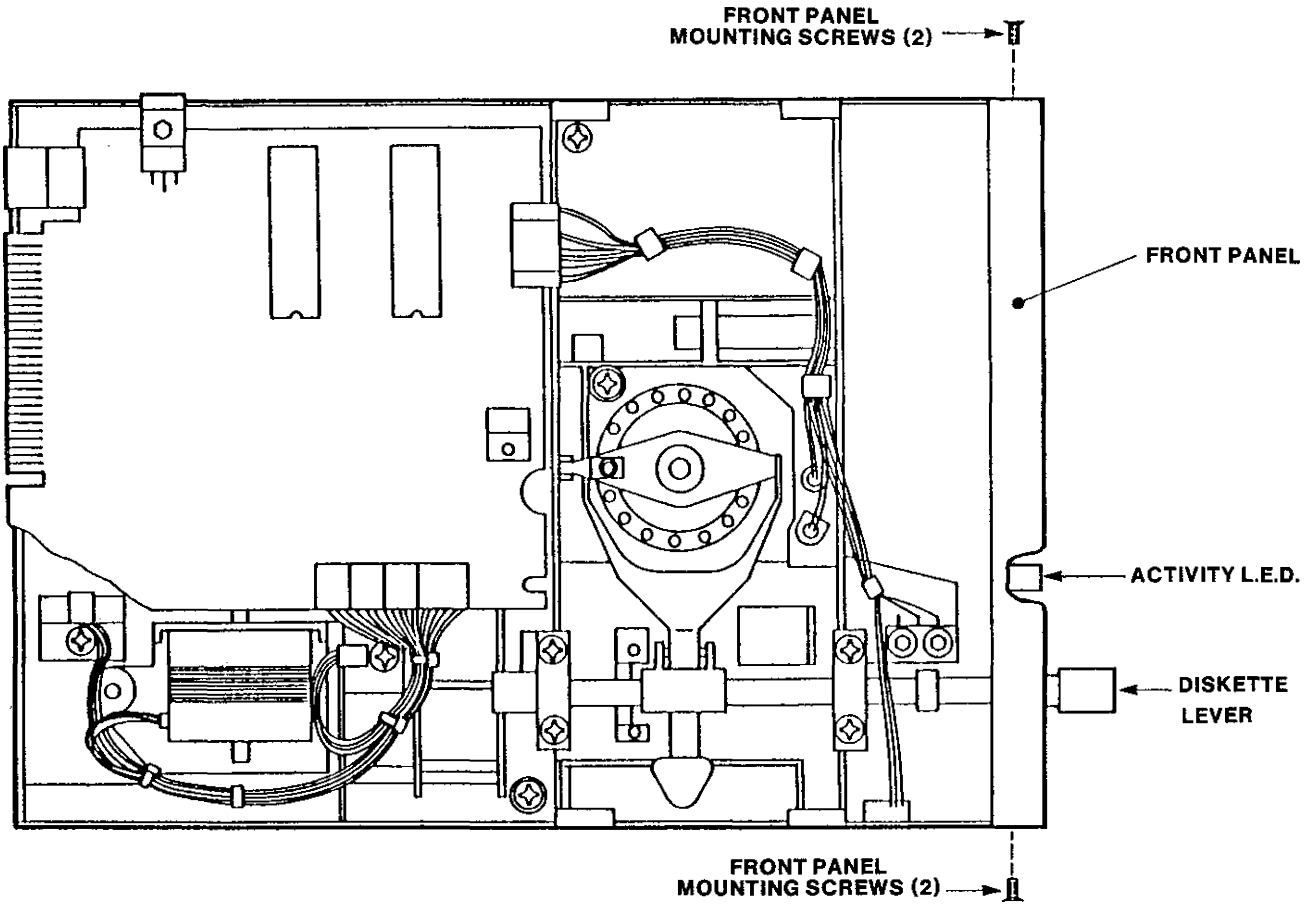


FIGURE 6-5
FRONT PANEL

BRIDGE ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the diskette lever.
3. Remove the four bridge mounting screws attaching the Bridge Assembly to the chassis (Figure 6-6).
4. Carefully pull out the two index L.E.D.'s from the Bridge Assembly.
5. Carefully lift out the Bridge Assembly toward the back of the drive. The shaft must clear the front panel (Figure 6-7).

INSTALLATION

1. Insert the shaft into the front panel, and lay the Bridge Assembly in place.

NOTE

Ensure the upper head lift arm is on top of the load arm assembly.

2. Install and tighten the four bridge mounting screws attaching the Bridge Assembly to the chassis.
3. Install the two index L.E.D.'s into the Bridge Assembly.
4. Install the diskette lever.
5. Install the circuit board.
6. Ensure the diskette lever clamps the cone and loads the head(s).
7. Perform the checks and adjustments in Table 6-2.

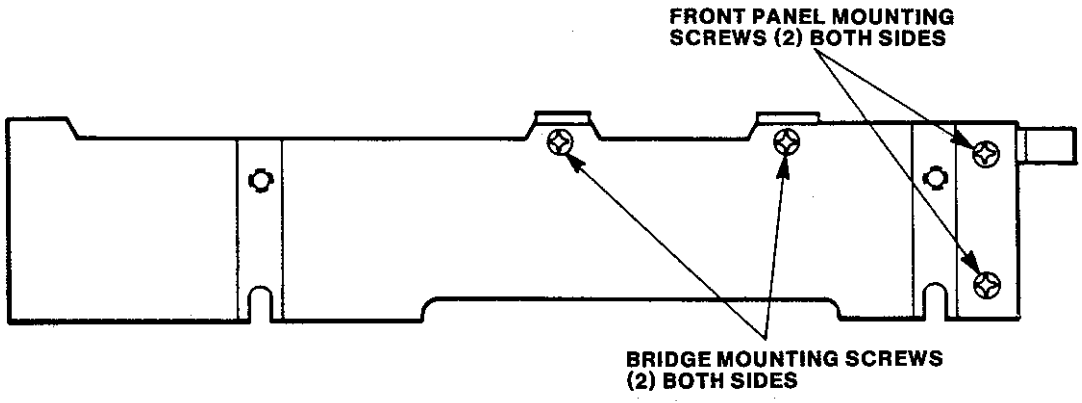


FIGURE 6-6
BRIDGE ASSEMBLY MOUNTING SCREWS

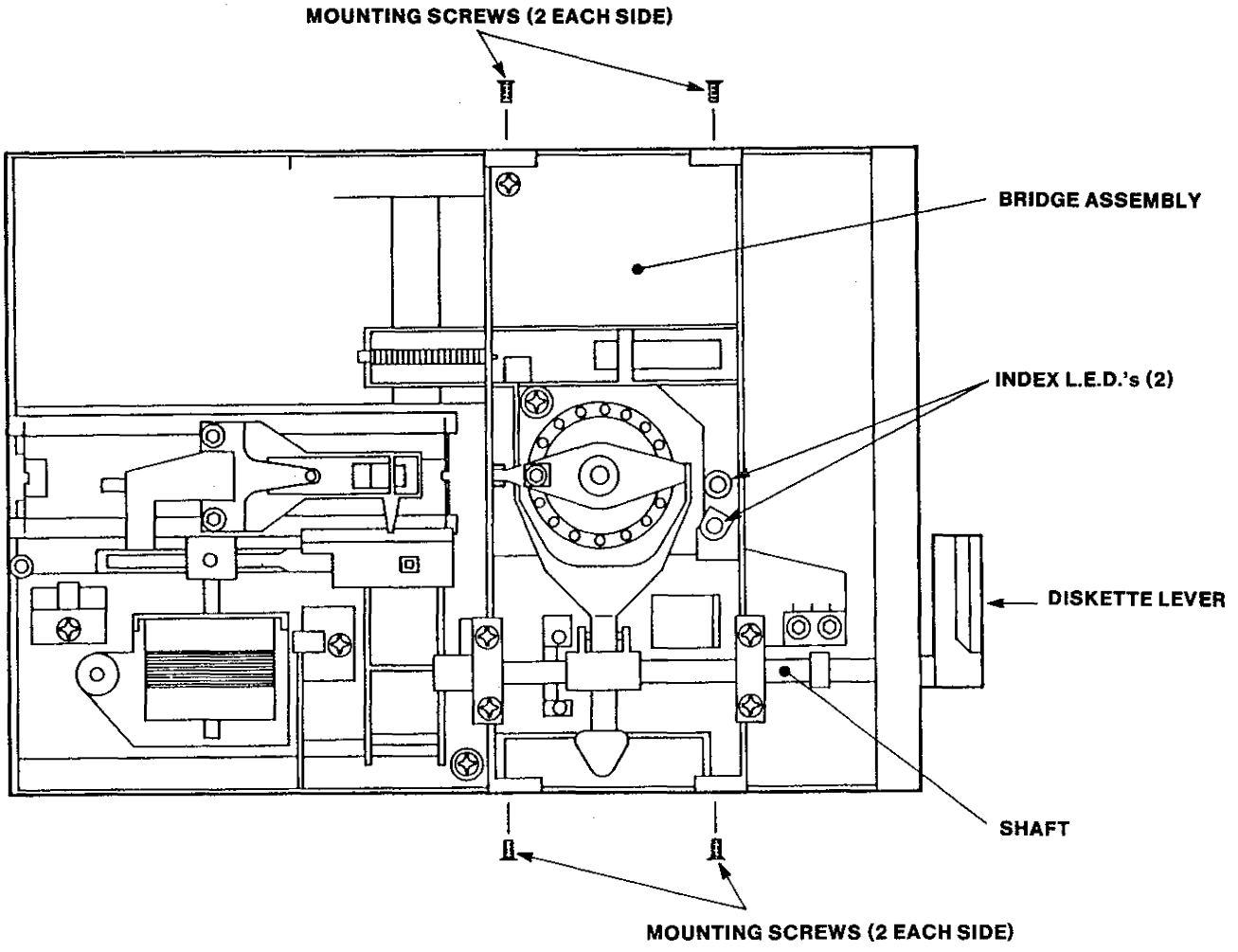


FIGURE 6-7
BRIDGE ASSEMBLY

DRIVE MOTOR

REMOVAL

1. Remove the Logic circuit board.
2. Remove the diskette lever.
3. Remove the front panel.
4. Remove the Bridge Assembly.
5. Cut the tie wraps attaching the drive motor connector to the cable harness (Figure 6-8).
6. Remove the mounting screw attaching the heat sink to the chassis. The heat sink is located on the drive motor servo board (Figure 6-9).
7. Remove the three drive motor mounting screws.
8. Lift the drive motor from the bottom of the drive, pulling the cable through the slot in the chassis.

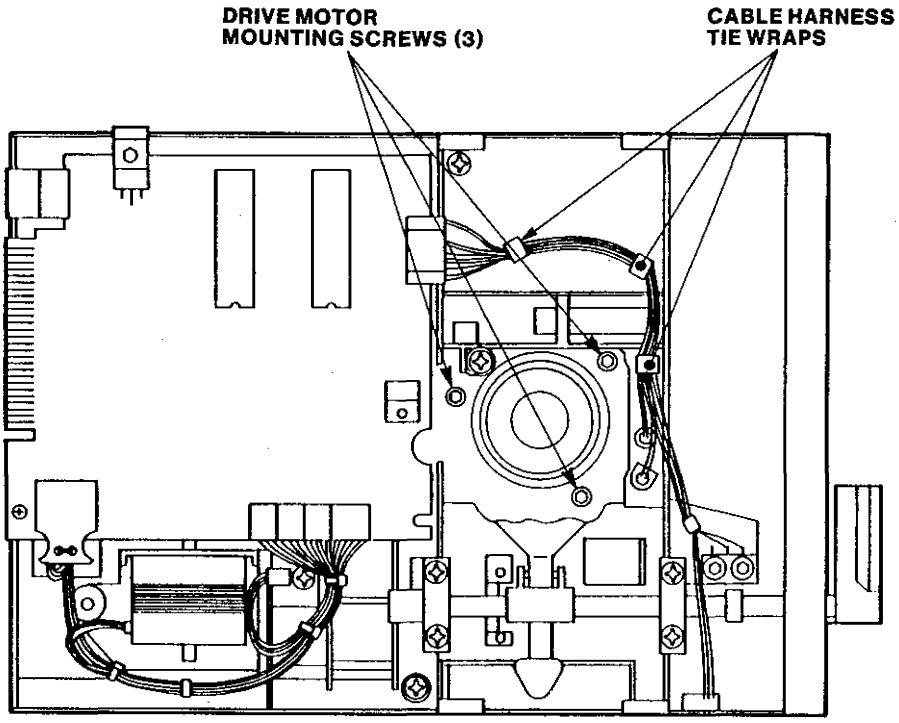


FIGURE 6-8
DRIVE MOTOR MOUNTING SCREWS

INSTALLATION

1. Install the new drive motor assembly, aligning the mounting hole on the top side of the chassis.
2. Install and tighten the three mounting screws (Figure 6-8).
3. Install and tighten the heat sink mounting screw.
4. Route the connector through the cable slot (Figure 6-9).
5. Bundle the cable harness with two tie wraps.
6. Install the bridge assembly.
7. Install the front panel.
8. Install the diskette lever.
9. Install the logic circuit board.
10. Perform the checks in Table 6-2.

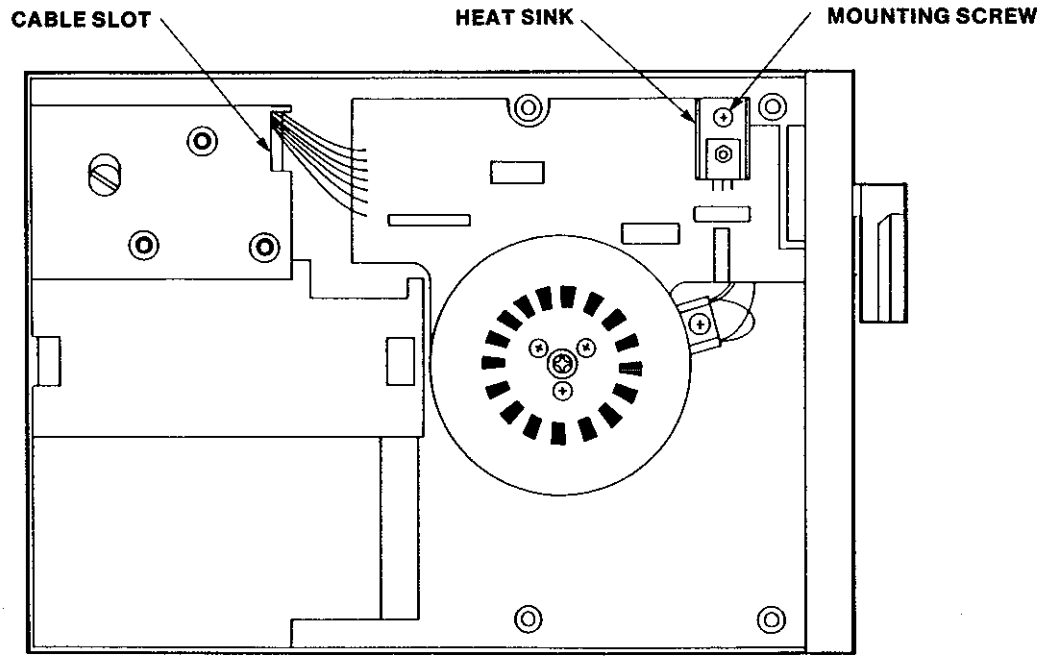


FIGURE 6-9
HEAT SINK AND CABLE SLOT

LOAD ARM ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the mounting screw and washer that are used to attach the Load Arm Assembly to the Bridge Assembly (Figure 6-10).
3. Carefully slide out the Load Arm Assembly toward the rear of the chassis.

INSTALLATION

1. Slide the Load Arm Assembly into position from the rear of the chassis, ensuring the load arm pin is sitting under the front of the mounting screws and washer.
2. Install and tighten the mounting screw attaching the Load Arm Assembly to the chassis, ensuring the washer is under the screw and the head lift arm is over the Load Arm Assembly.
3. Install the Logic circuit board.
4. Insert a diskette into the drive.
5. Ensure the head is loaded when the diskette lever is activated and adequate clearance is attained for diskette insertion and ejection.
6. Perform the checks indicated in Table 6-2.

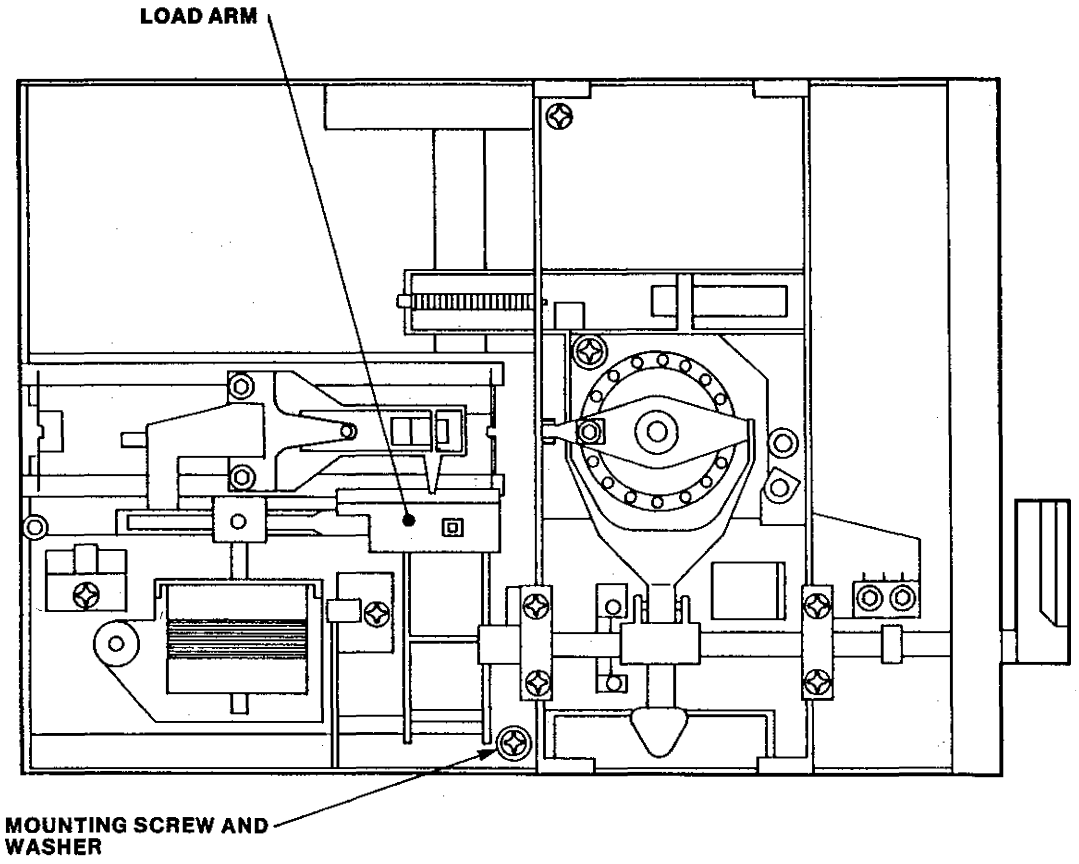


FIGURE 6-10
LOAD ARM ASSEMBLY

TRACK 0 SENSOR ASSEMBLY

REMOVAL

1. Remove P11 from the Logic circuit board.
2. Cut the tie wraps that hold the cable harness, and remove the P11 wires (Figure 6-11).
3. Remove the P11 wires from the chassis.
4. Remove the mounting screw holding down the Track 0 Sensor Assembly bracket.
5. Remove the bracket.
6. Lift off the Track 0 Sensor Assembly.

INSTALLATION

1. Install the Track 0 Sensor Assembly.
2. Install the Track 0 sensor mounting bracket with the mounting screw.
3. Loop the P11 wires from the Track 0 Sensor Assembly through the bracket attached to the chassis.
4. Using tie wraps, cable harness the P11 wires and the other wires together.
5. Plug P11 into the circuit board.
6. Perform the checks and adjustments in Table 6-2.

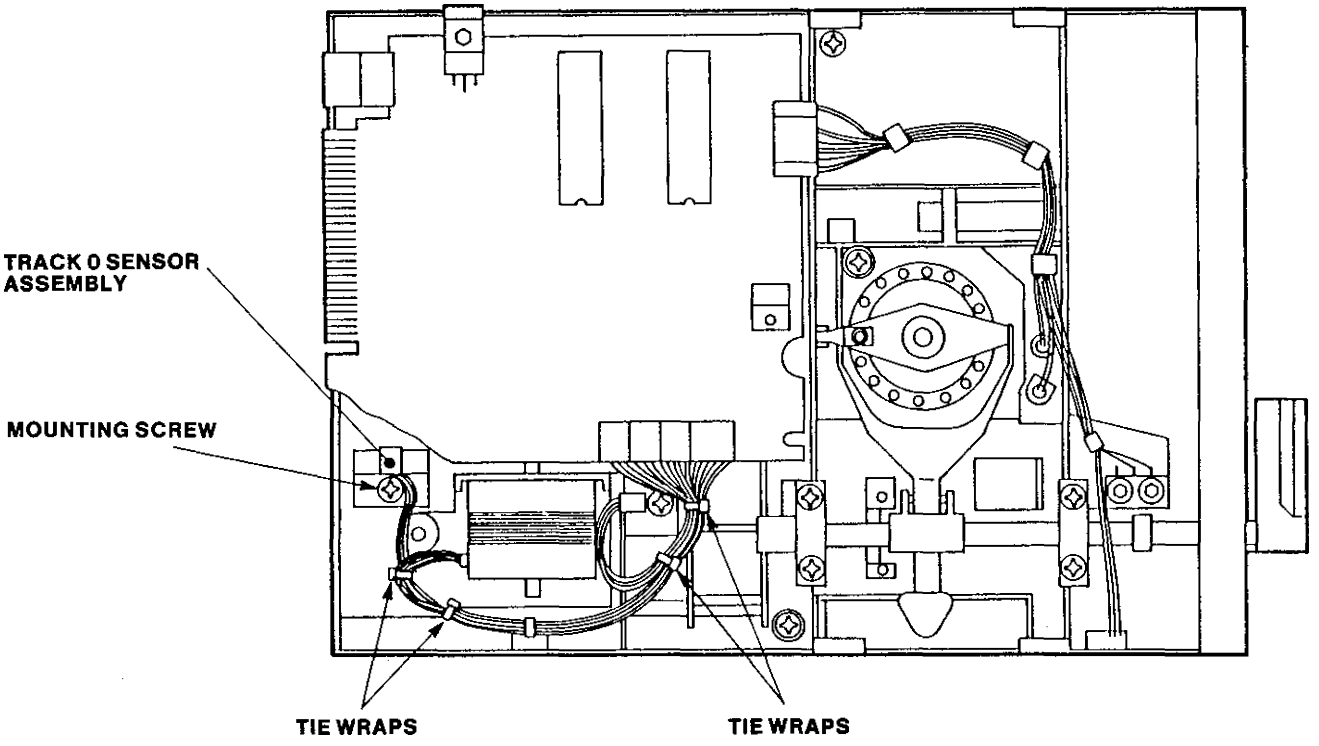


FIGURE 6-11
TRACK 0 SENSOR ASSEMBLY

WRITE PROTECT SENSOR ASSEMBLY

REMOVAL

1. Remove P10 from the circuit board.
2. Remove the mounting screws attaching the Write Protect Sensor Assembly to the chassis (see Figure 6-12).
3. Cut the tie wraps that hold the wires to the cable harness, and lift out the Write Protect Sensor Assembly.

INSTALLATION

1. Using the original mounting bracket, attach the Write Protect Sensor Assembly to the chassis.
2. Plug P10 into the circuit board.
3. Tie wrap the Write Protect wires to the cable harness.
4. Perform the checks and adjustments in Table 6-2.

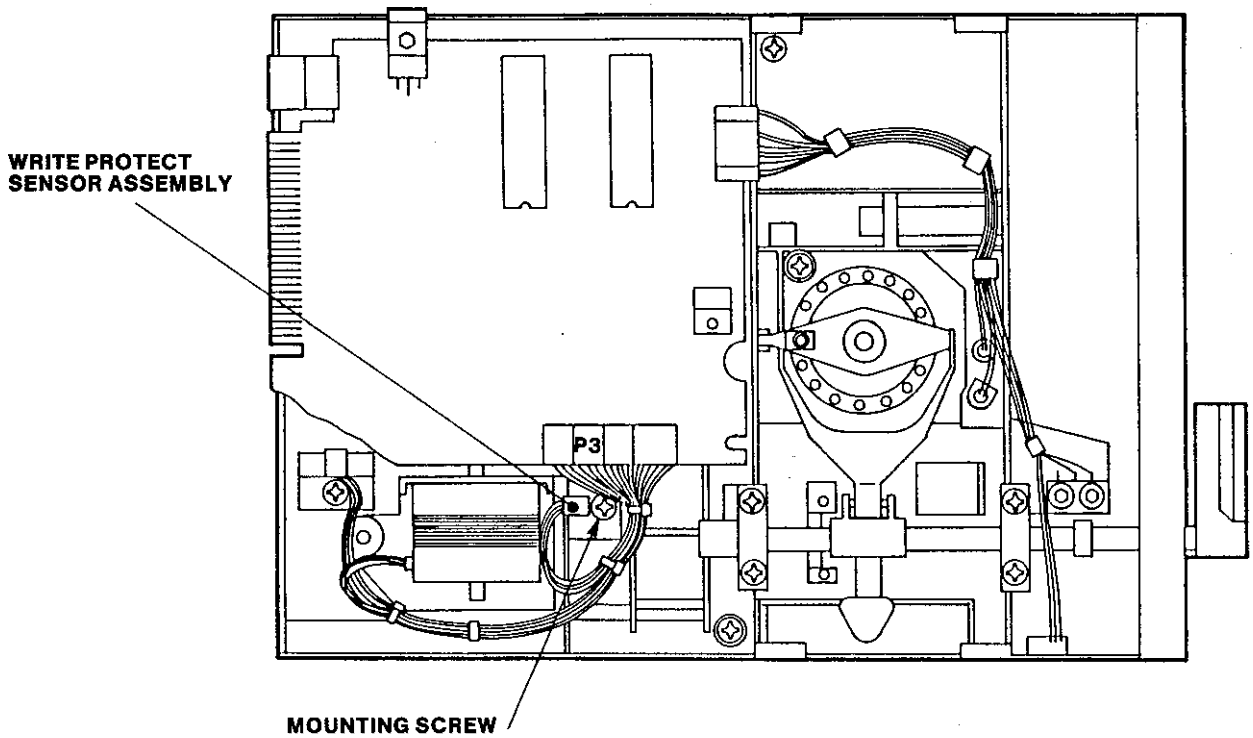


FIGURE 6-12
WRITE PROTECT SENSOR ASSEMBLY

MOTOR SWITCH ASSEMBLY

REMOVAL

1. Remove P3 from the circuit board.
2. Remove the mounting screws from the motor switch (Figure 6-13).
3. Remove the cable harness tie wraps leading to P3.
4. Lift out the Motor Switch Assembly.

INSTALLATION

1. Mount the Motor Switch Assembly to the bridge, using the original mounting screws and nut plate.
2. Route the motor switch cables using the cable harness tie wraps.
3. Plug P3 into the circuit board.
4. Perform the checks and adjustments in Table 6-2.

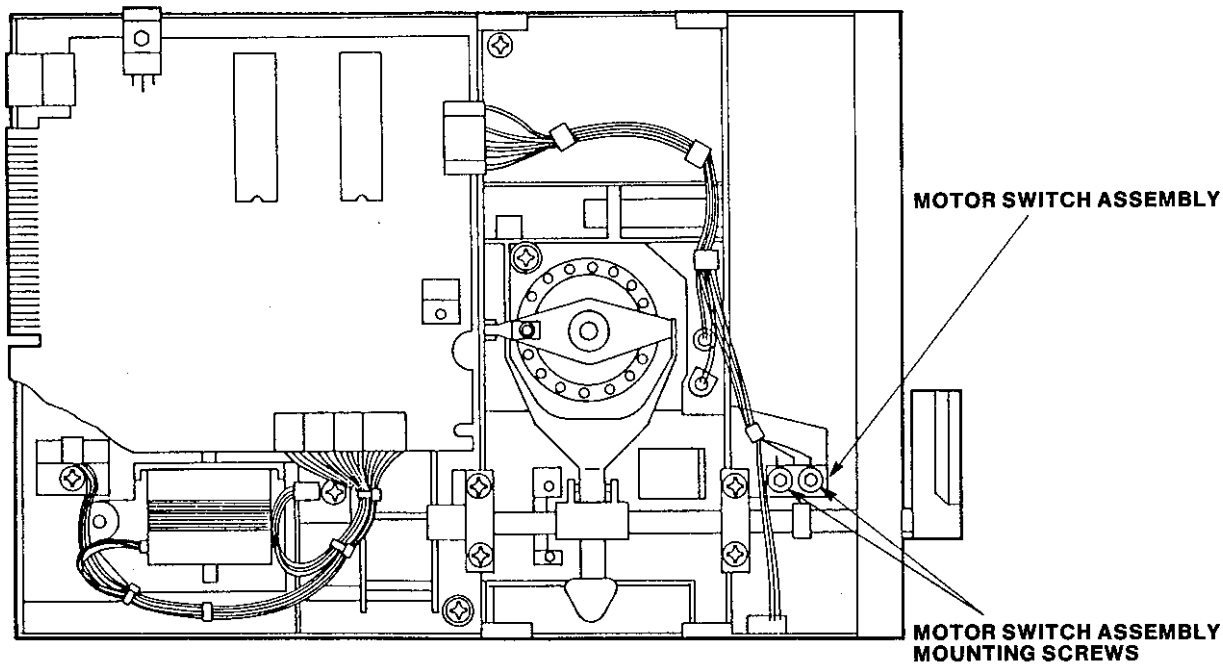


FIGURE 6-13
MOTOR SWITCH ASSEMBLY

INDEX SENSOR ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the diskette lever.
3. Remove the front panel.
4. Remove the Bridge Assembly, and upper index sensors (Figure 6-14).
5. Remove the drive motor.
6. Remove the left guide rail by pushing in on the center tab of the rail, and push the rail out (Figure 6-15).
7. Remove the lower index sensor mounting screw.
8. Slide the index cable and connector through the slot in the chassis. Remove the index sensor.

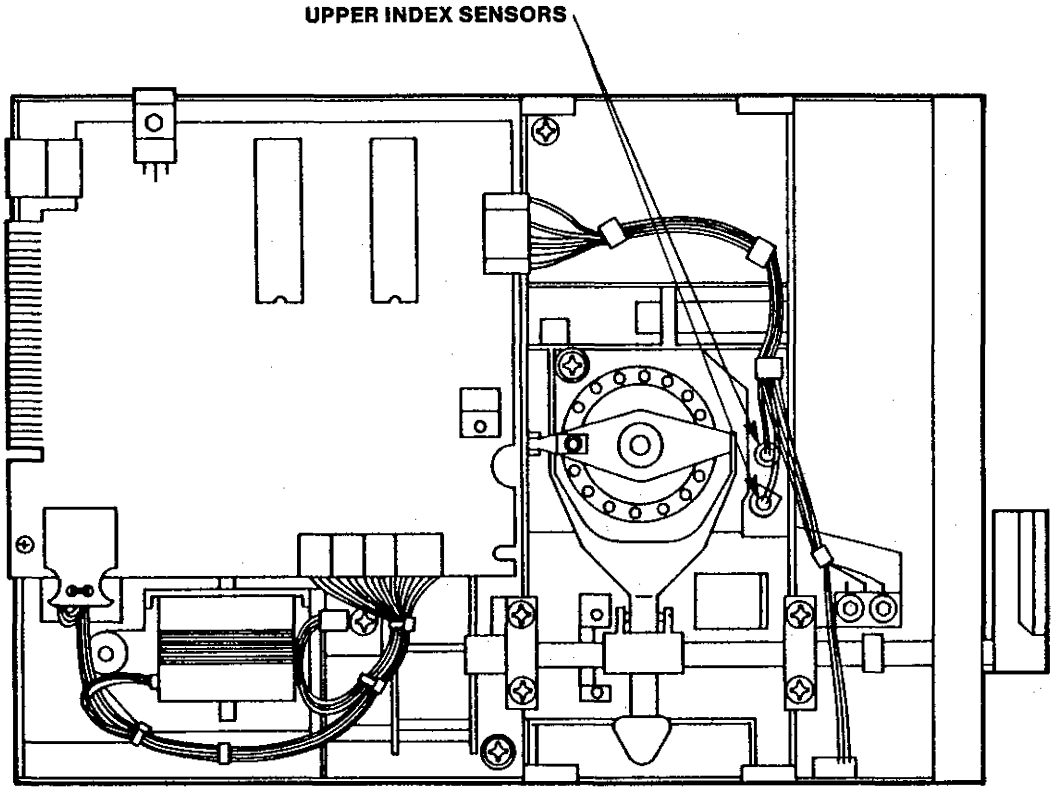


FIGURE 6-14
INDEX SENSOR ASSEMBLY, TOP VIEW

INSTALLATION

1. Mount the lower index sensor to the chassis.
2. Slide the upper index sensor cable and connector through the slot in the chassis.
3. Install the left rail by pressing it into its mounting slots in the chassis.

NOTE

Ensure the index sensor cables are between the chassis and rail.

4. Install the drive motor
5. Install the Bridge Assembly, and upper index sensor.
6. Install the front panel.
7. Install the diskette lever.
8. Install the Logic circuit board.
9. Perform the checks and adjustment in Table 6-2.

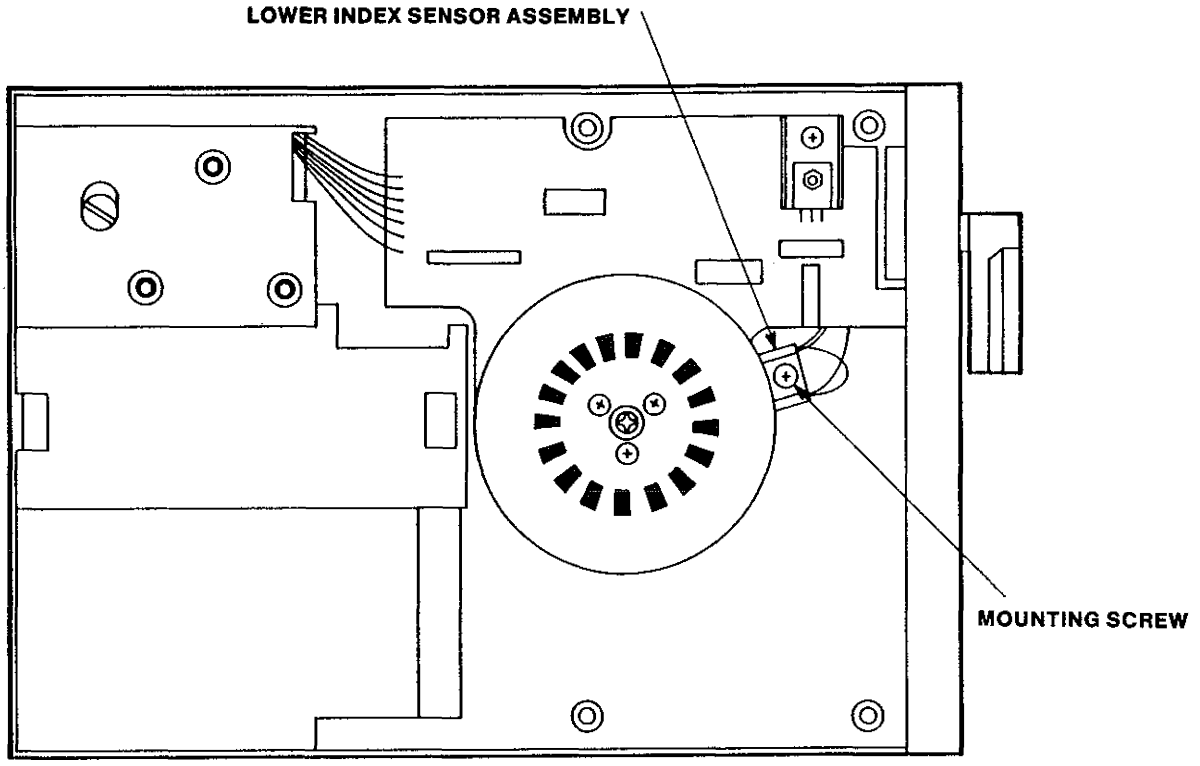


FIGURE 6-15
INDEX SENSOR ASSEMBLY, BOTTOM VIEW

DISKETTE EJECTOR ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the diskette lever.
3. Remove the Bridge Assembly.
4. Remove the Trigger Assembly (Figure 6-16).
5. Release the spring attached to the rear of the ejector.
6. Remove the ejector by sliding it out.

INSTALLATION

1. Ensure the ejector spring is hooked to the bridge.
2. Insert the ejector.
3. Pull the spring back, attaching it to the rear of the ejector.
4. Install the Trigger Assembly.
5. Reinstall the Bridge Assembly.
6. Install the diskette lever.
7. Reinstall the Logic circuit board.
8. Insert a work diskette into the drive.
9. Ensure the diskette stays in prior to being closed.
10. Close and open the diskette lever.
11. The diskette should eject.

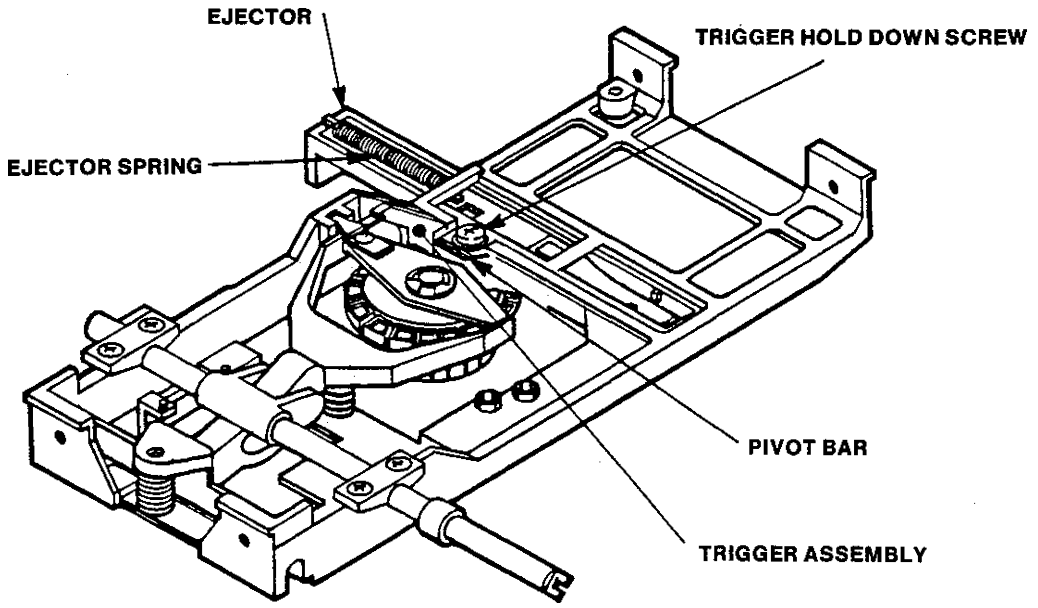


FIGURE 6-16
DISKETTE EJECTOR ASSEMBLY

STEPPER BAND

REMOVAL

1. Remove the circuit board.
2. Lift off the stepper band from the spring tensioner (Figure 6-17).
3. Lift off the stepper band where it attaches to the front of the Head Carriage Assembly.
4. Remove the mounting screw attaching the stepper band to the stepper pully.
5. Lift out the stepper band.

INSTALLATION

1. Loop the front of the stepper band into the Head Carriage Assembly (Figure 6-17).
2. Loop the stepper band around the stepper pulley.
3. Attach the rear of the band to the spring tensioner.
4. Attach the stepper band to the stepper pulley loosely with the mounting screw.
5. Move the Head Carriage Assembly back and forth at least five times.
6. Visually inspect the stepper band to ensure it is centered on the stepper pulley.
7. Tighten the mounting screw attaching the stepper band to the stepper pulley.
8. Reinstall the Logic circuit board.
9. Perform the checks and adjustments in Table 6-2.

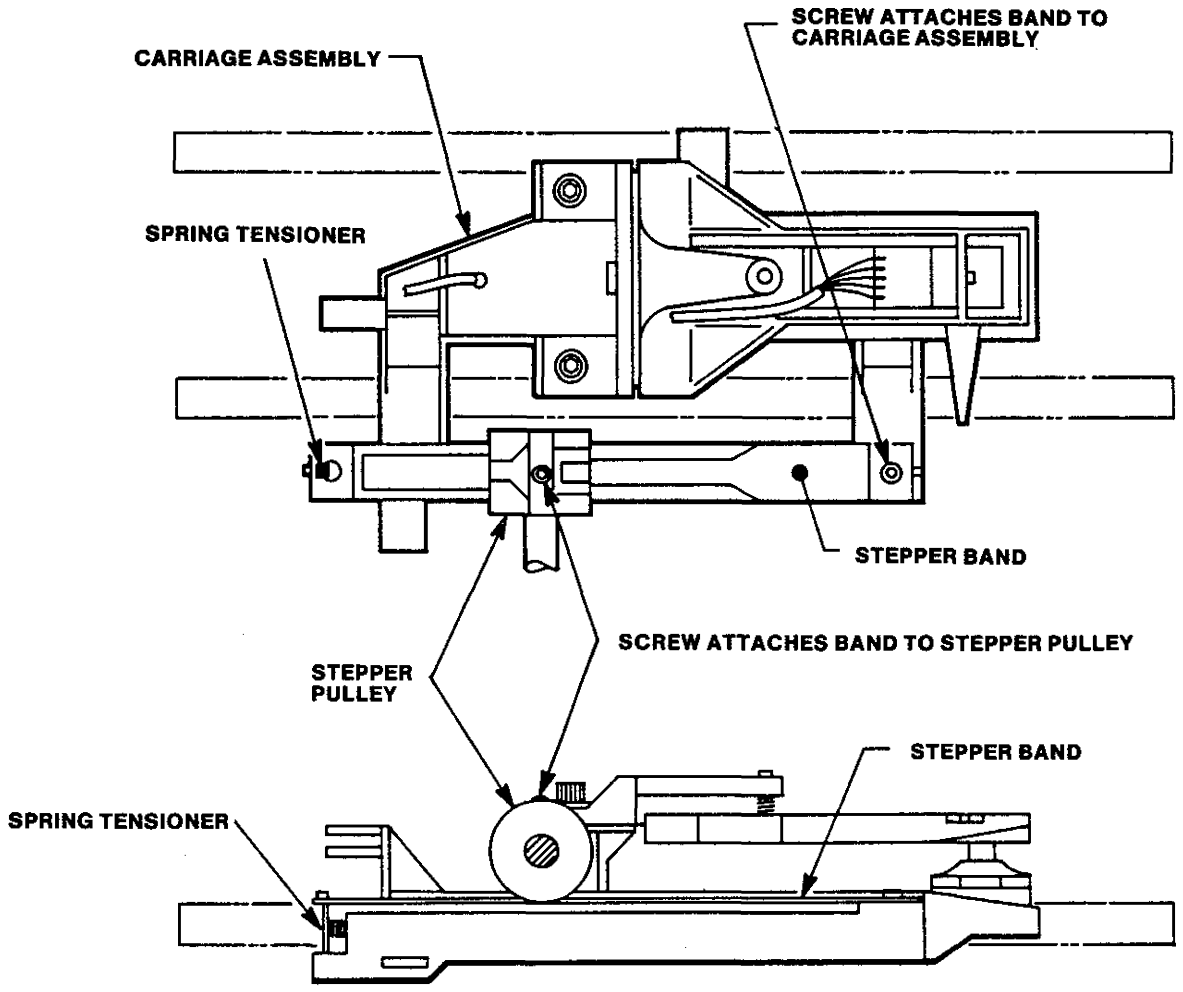


FIGURE 6-17
STEPPER BAND

STEPPER MOTOR ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the stepper band.
3. Remove the three mounting screws attaching the Stepper Motor Assembly to the chassis (Figure 6-18).
4. Cut the tie wraps connecting the stepper motor wires to the cable harness.
5. Lift out the Stepper Motor Assembly.

NOTE

Be careful not to damage the stepper band.

INSTALLATION

1. Place the Stepper Motor Assembly into the drive's chassis.
2. Using the original three mounting screws, attach the Stepper Motor Assembly to the chassis.
3. Install the stepper band.
4. Replace the Logic circuit board.
5. Rebundle the cable harness and connect it with two tie wraps.
6. Perform the checks and adjustments in Table 6-2.

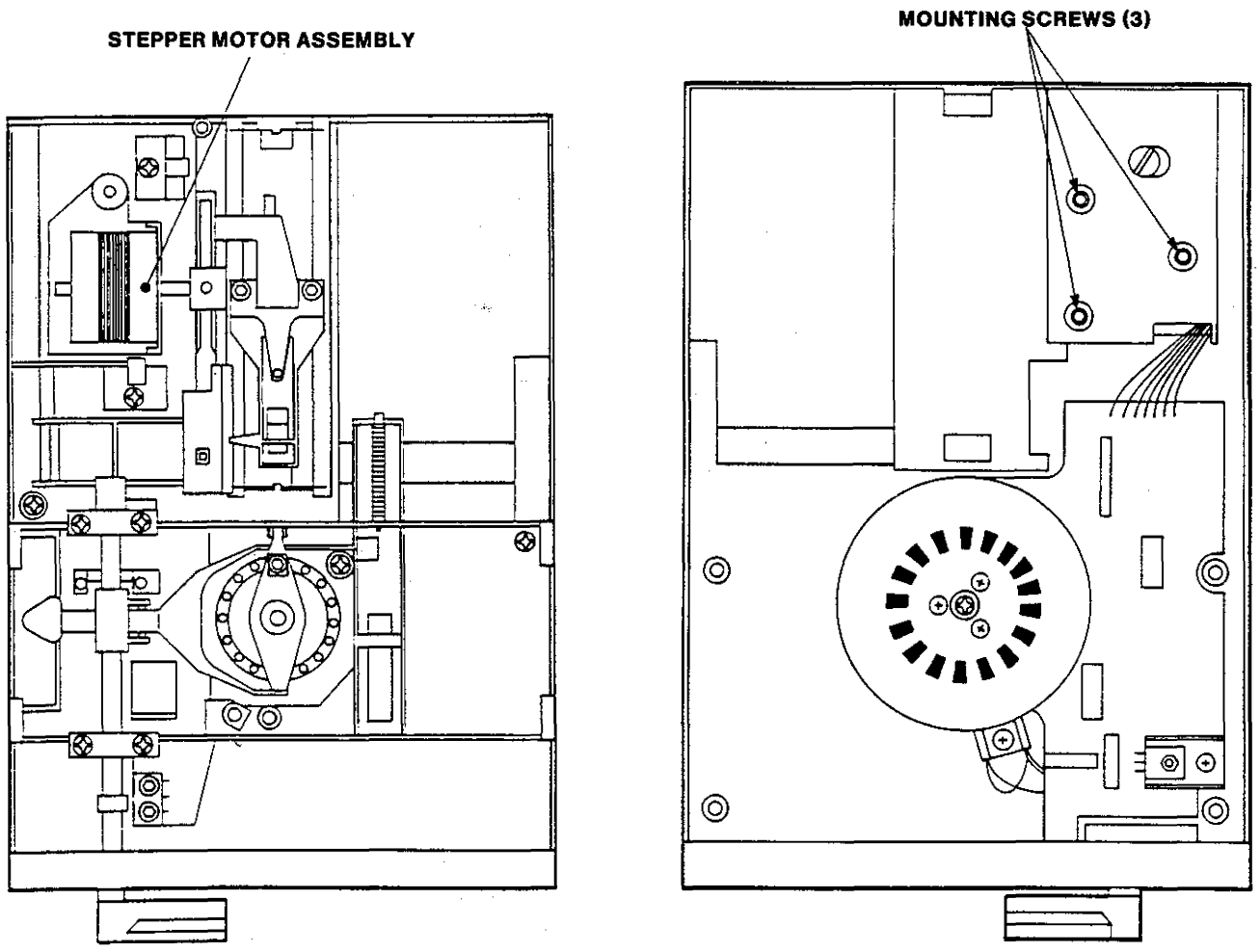


FIGURE 6-18
STEPPER MOTOR

HEAD CARRIAGE ASSEMBLY

REMOVAL

1. Remove the Logic circuit board.
2. Remove the stepper band.
3. Remove the two clips that hold the carriage guide rails to the chassis (Figure 6-19).
4. Carefully lift out the Head Carriage Assembly.
5. Remove the carriage guide rails from the Head Carriage Assembly.

INSTALLATION

1. Install the carriage guide rails into the carriage.
2. Using the two clips, attach the carriage guide rails to the chassis.
3. Install the stepper band.

NOTE

Take care not to damage the stepper band.

4. Install the Logic circuit board.
5. Perform the checks and adjustments in Table 6-2.

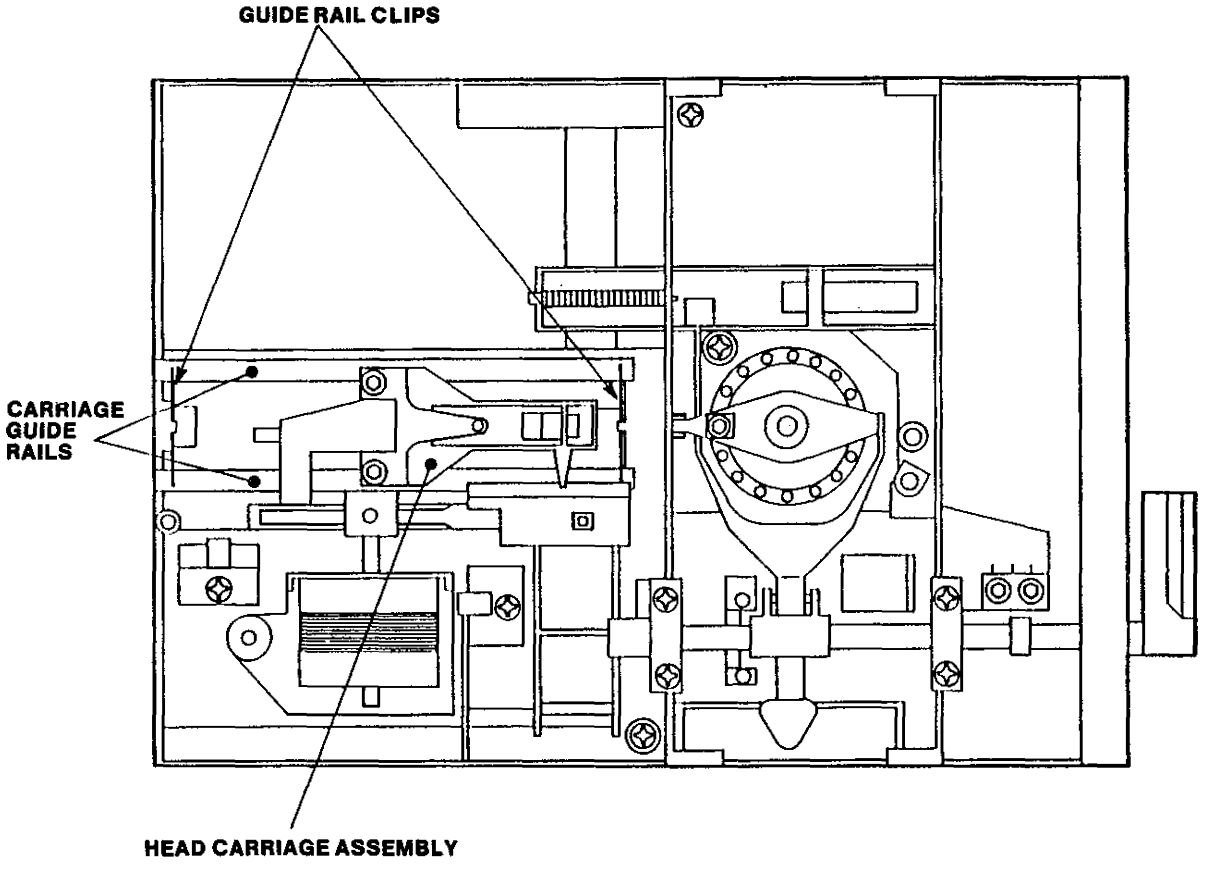


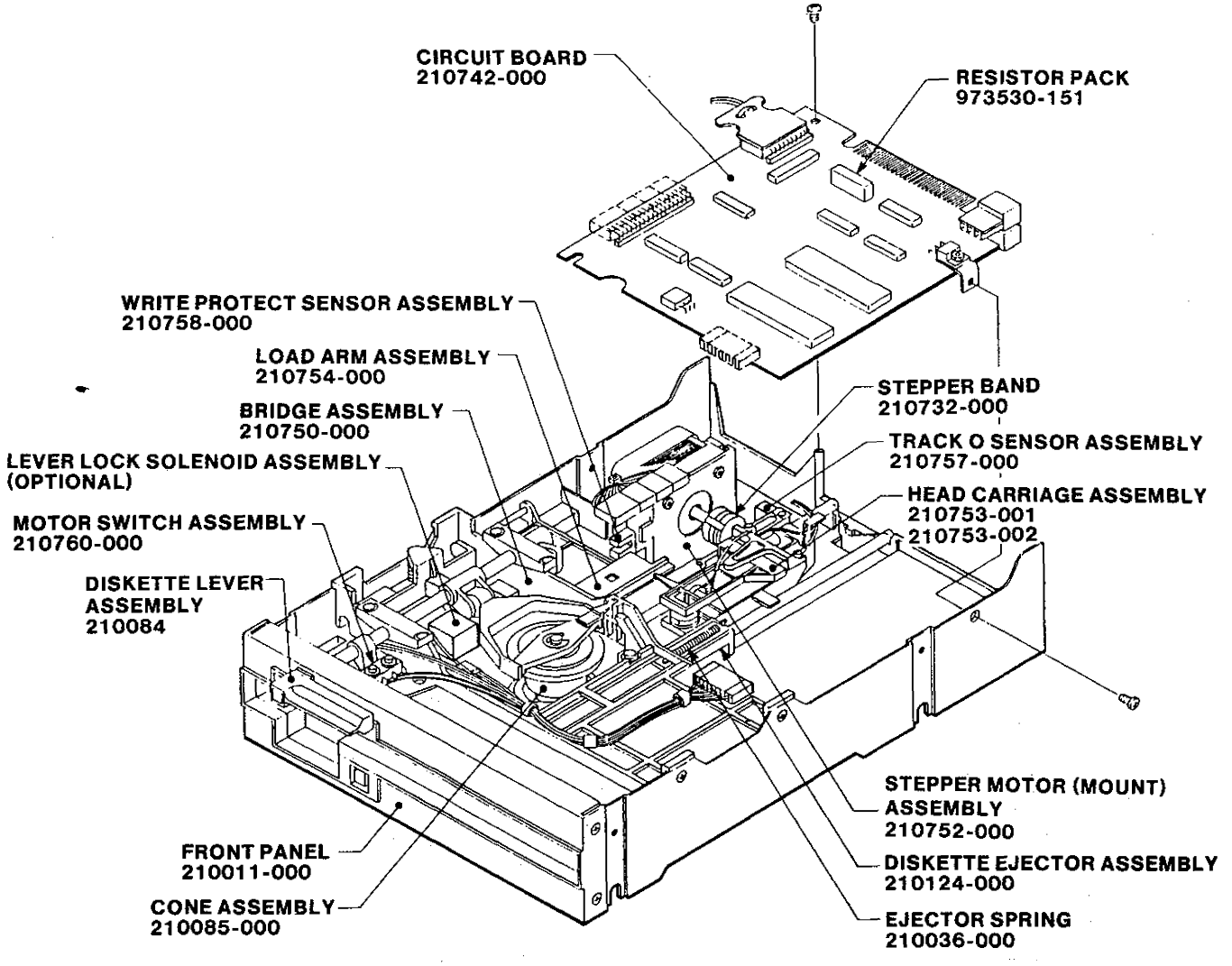
FIGURE 6-19
HEAD CARRIAGE

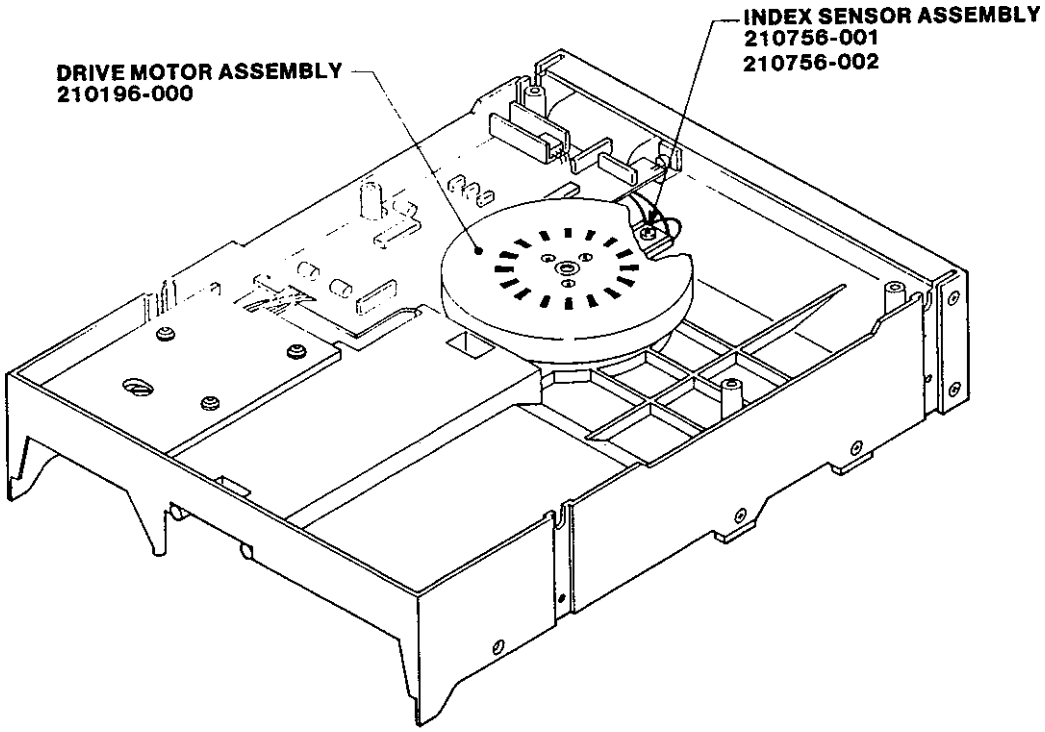
APPENDIX A

RECOMMENDED SPARE PARTS AND MAJOR ASSEMBLIES

This appendix contains the recommended spare parts and the major assembly drawings for the drive. Part numbers on this list should be used for ordering spare parts. A spare parts list with prices for parts and services is available from Tandon Corporation.

Part Number	Description
210742-000	Circuit Board
210085-000	Cone Assembly
210084-000	Diskette Lever Assembly
210011-000	Front Panel
210750-000	Bridge Assembly
210196-000	Drive Motor
210754-000	Load Arm Assembly
210757-000	Track 0 Sensor Assembly
210758-000	Write Protect Sensor Assembly
210760-000	Motor Switch Assembly
210756-001	Index Sensor Assembly, Single-Sided
210756-002	Index Sensor Assembly, Double-Sided
210124-000	Diskette Ejector Assembly
210036-000	Ejector Spring
210732-000	Stepper Band
210752-000	Motor Mount Assembly
210753-001	Head Carriage Assembly, Single-Sided
210753-002	Head Carriage Assembly, Double-Sided
973530-151	Resistor Pack
210140-000	Filler Panel Kit (Not Shown)
210132-000	Mounting Strap Kit (Not Shown)
210106-000	Shipping Insert (Not Shown)

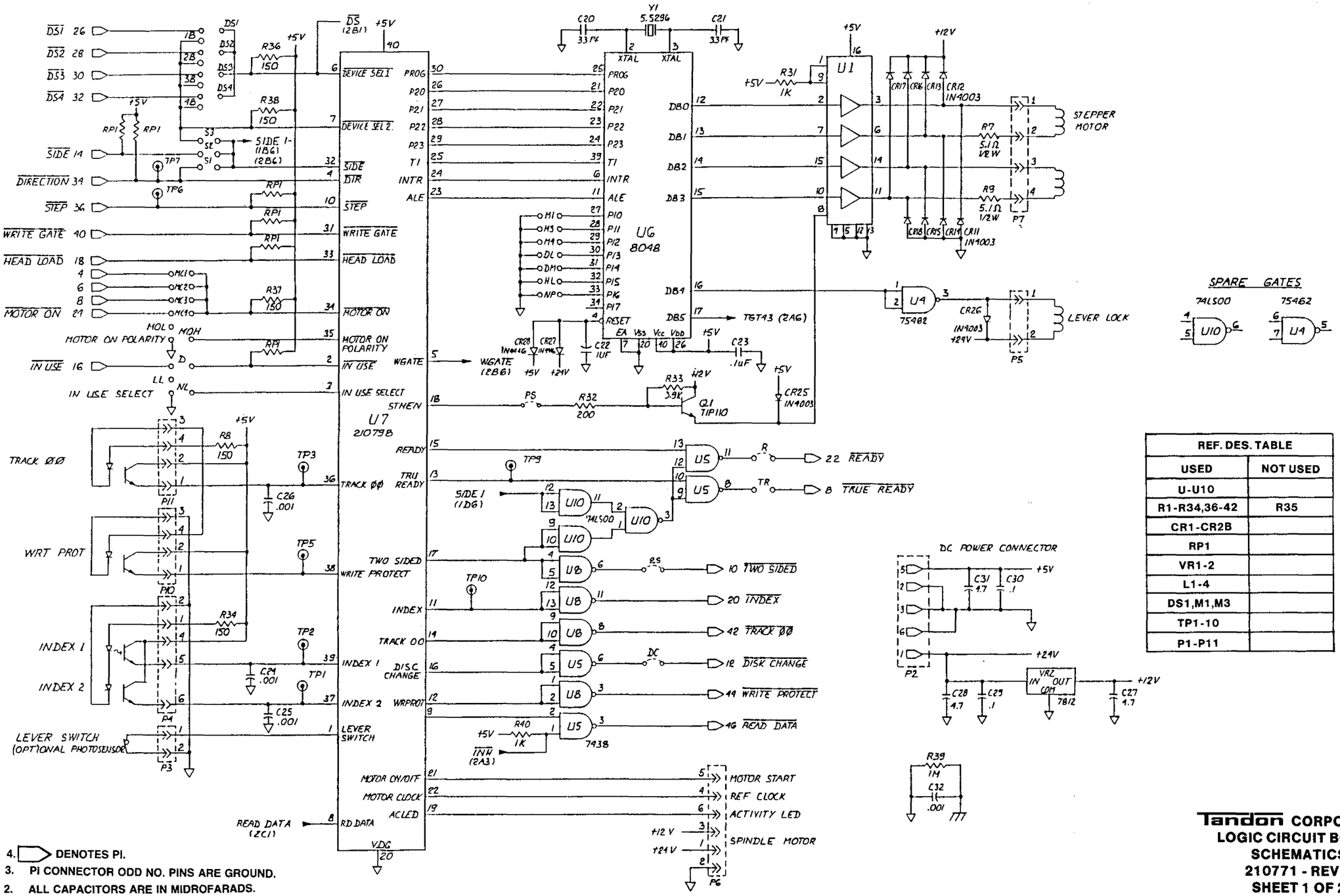

CIRCUIT BOARD
210742-000
RESISTOR PACK
973530-151
WRITE PROTECT SENSOR ASSEMBLY
210758-000
LOAD ARM ASSEMBLY
210754-000
BRIDGE ASSEMBLY
210750-000
LEVER LOCK SOLENOID ASSEMBLY
(OPTIONAL)
MOTOR SWITCH ASSEMBLY
210760-000
DISKETTE LEVER
ASSEMBLY
210084
STEPPER BAND
210732-000
TRACK O SENSOR ASSEMBLY
210757-000
HEAD CARRIAGE ASSEMBLY
210753-001
210753-002
STEPPER MOTOR (MOUNT)
ASSEMBLY
210752-000
DISKETTE EJECTOR ASSEMBLY
210124-000
EJECTOR SPRING
210036-000
FRONT PANEL
210011-000
CONE ASSEMBLY
210085-000


INDEX SENSOR ASSEMBLY
210756-001
210756-002
DRIVE MOTOR ASSEMBLY
210196-000

APPENDIX B

CIRCUIT BOARD SCHEMATICS AND DRAWINGS

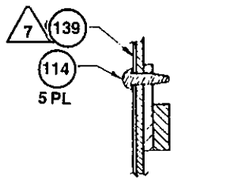
This appendix contains the current circuit board schematics and circuit board drawings for the TM848-1E and TM848-2E.



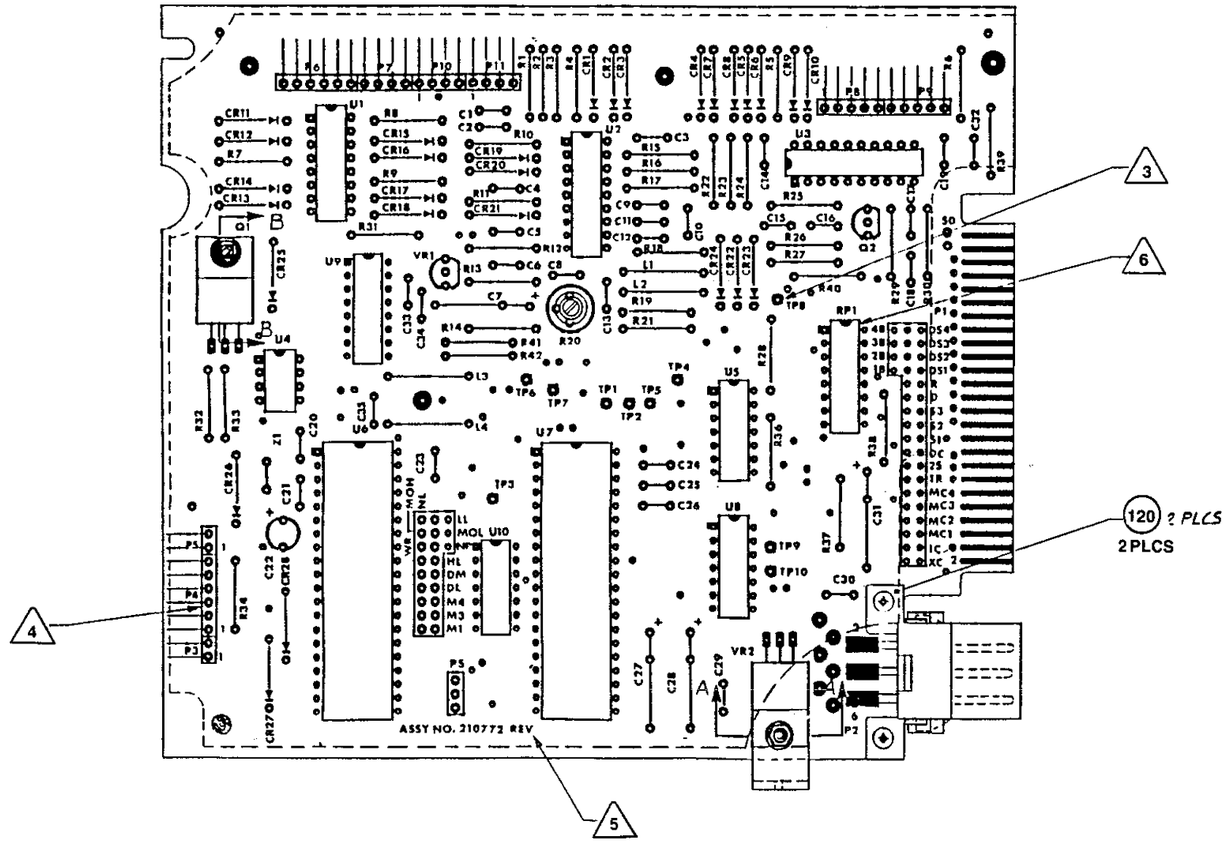
REF. DES. TABLE	
USED	NOT USED
U-U10	
R1-R34,36-42	R35
CR1-CR2B	
RP1	
VR1-2	
L1-4	
DS1,M1,M3	
TP1-10	
P1-P11	

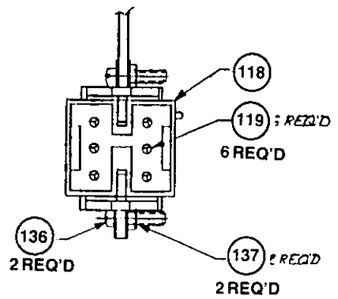
4. ⇨ DENOTES PI.
3. PI CONNECTOR ODD NO. PINS ARE GROUND.
2. ALL CAPACITORS ARE IN MIDROFARADS.
1. ALL RESISTORS ARE IN OHMS.

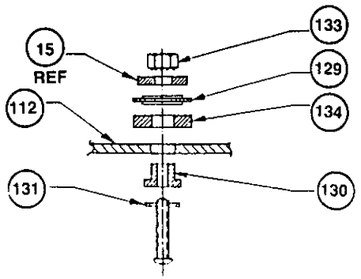
Tandon CORPORATION
LOGIC CIRCUIT BOARD
SCHEMATICS
210771 - REV C
SHEET 1 OF 2
B-3



SECTION B-B
INSERT PLASTIC RIVET
INTO Q1 & SHIELD
5 PLACES AS SHOWN







SECTION A-A
HEATSINK ASSY

7 ITEM 139 (SHIELD) TO BE MOUNTED ON CIRCUIT SIDE OF BOARD.

6 RPI IS INSTALLED AT FINAL ASSY.

5 MARK REV. LETTER IN AREA INDICATED.

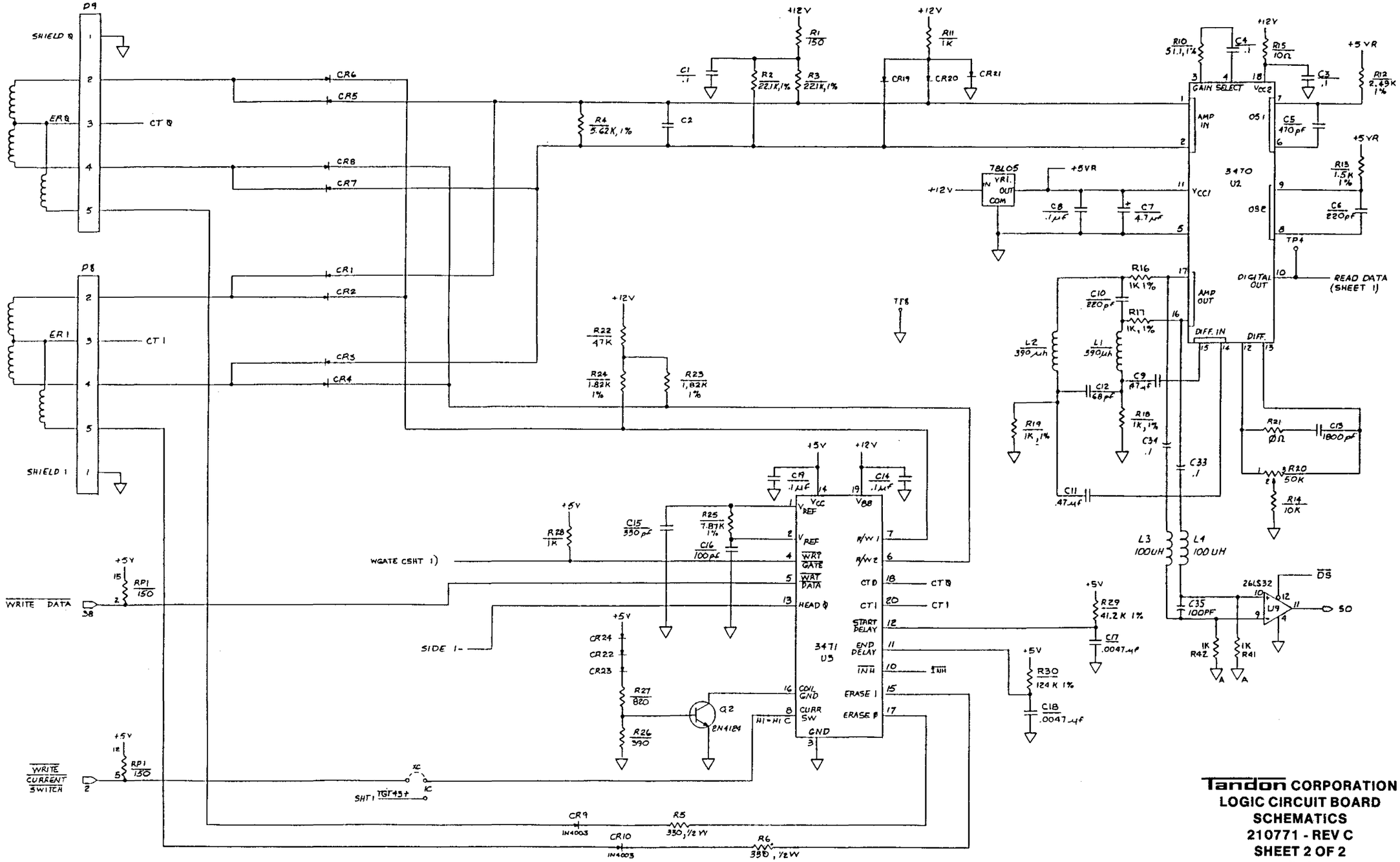
4 REMOVE OR CUT FLUSH CONNECTOR P4 PIN 3 AS SHOWN.

3 TEST POINTS DENOTED BY □ SYMBOL.

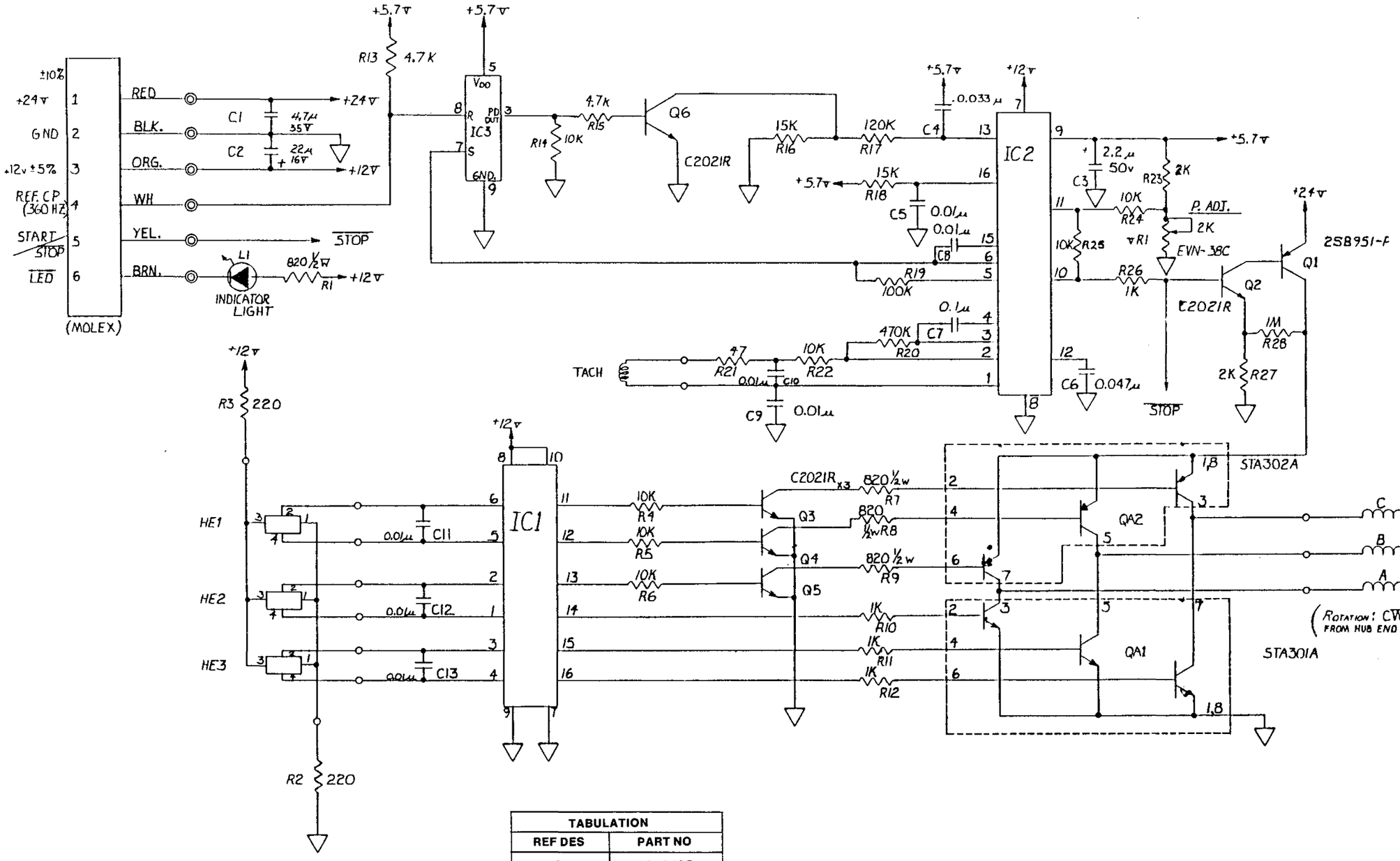
2 REF: SCHEMATIC DRAWING 210771.

1 REF: FABRICATION DRAWING 210773.

Tandon CORPORATION
LOGIC CIRCUIT BOARD
ASSEMBLY DRAWING
210772 - REV E
SHEET 1 OF 1
B-2



Tandon CORPORATION
LOGIC CIRCUIT BOARD
SCHEMATICS
210771 - REV C
SHEET 2 OF 2
B-4



TABULATION	
REF DES	PART NO
IC1	μPC1246C
IC2	μPC1043C
IC3	TC5081P

4. REFERENCE: NIDEC DIRECT DRIVE MOTOR ASSEMBLY 88PTDN8003.

5. "IDENTIFY CONNECTOR BY MARKING "P6" ON SOLID PLASTIC SURFACE."

Tandon CORPORATION
DIRECT DRIVE MOTOR
SCHEMATIC
210196 - REV C
SHEET 1 OF 1
B-5

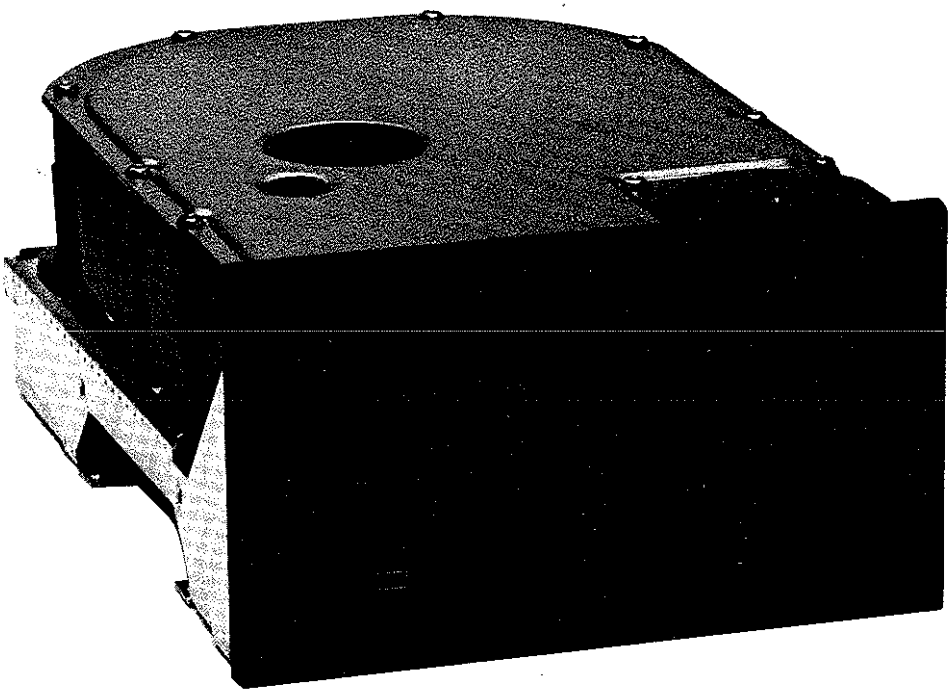
Tandon
CORPORATE OFFICES
20320 PRAIRIE STREET
CHATSWORTH, CA 91311

TELEPHONE NO.: (213) 993-6644
TELEX NO.: 194794
TWX NO.: 910-494-1721

PRINTED IN U.S.A.

P/N 179056-001A (T5014A 11-83)

OEM
OPERATING AND SERVICE MANUAL
TM501, TM502, TM503 DISK DRIVES
345 TRACKS PER INCH



Tandon CORPORATION
20320 PRAIRIE STREET
CHATSWORTH, CA 91311

NOTICE

This document is intended to provide the user with detailed information adequate for the efficient installation, operation, and service of the equipment involved.

However, while every effort has been made to keep the information contained herein current and accurate as of the date of publication, no guarantee is given or implied as to its accuracy.

CONTENTS

ILLUSTRATIONS

FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This manual provides useful information to assist the customer when incorporating the Tandon rigid disk drive into a system.

Tandon Corporation's TM500 series of drives are full feature, 5-1/4-inch, rigid disk drives. They are compact data storage devices that contain one or more 130-millimeter plated aluminum platters within a sealed housing.

The TM500 series includes Model Numbers TM501, TM502, and TM503, which have one, two, and three recording platters, and use two, four, and six recording heads, respectively.

1.1 SCOPE OF THE DOCUMENT

Section 1 of this manual contains a general description of the disk drives. Section 2 contains the product specifications. Section 3 provides information on operation of the drives. Section 4 is a troubleshooting guide and replacement procedure. Assemblies and schematics are included in the appendices.

1.2 PURPOSE OF THE DRIVE

The 5-1/4-inch disk drive is a rotating disk memory device designed for random access data storage and retrieval. Typical applications include word processing systems, entry level microprocessor systems, intelligent calculators, program storage, small business computer systems, and any application in which low cost, random access data storage is required.

1.3 MAJOR FEATURES

MICROPROCESSOR CONTROL

The TM500 series of drives feature an onboard microprocessor. The microprocessor provides five major functions:

1. Self-calibration on power-up.
2. Buffered seek timing for improved access times.
3. Improved positioning with reduced hysteresis.
4. Write current switching for optimal recording quality.
5. Power and track fault detection.

DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an industry standard interface.

ACTIVITY INDICATOR

The activity indicator is located on the front panel of the drive. It is automatically illuminated when the drive is selected.

AIR FILTRATION

A self-contained, recirculating air filtration system supplies clean air through a 0.3-micron filter. A secondary absolute filter is provided to allow pressure equalization with the ambient atmosphere without contamination. The entire head-disk-actuator compartment is maintained at a slightly positive pressure to futher ensure an ultraclean environment.

1.4 FUNCTIONAL DESCRIPTION

The drive is fully self-contained and requires no operator intervention during normal operation. During the power-up sequence, the spindle motor reaches 3600 RPM, and the positioning mechanism recalibrates the recording heads back to Track 0. At this time, a Ready signal on the interface indicates the drive is ready for operation.

The head is positioned over the desired track by means of a four-phase stepper motor/band assembly and its associated electronics. This positioner uses a one-step rotation to cause a one-track radial movement. Subsequently, the recording heads can be positioned over the desired cylinders, and the data can be read or written from the appropriate track by selecting the desired head.

Typically, the drive uses MFM write and read recording methods. Data recovery electronics include a low-level read amplifier, differentiator, a zero-crossover detector, and digitizing circuits. No data decoding feature is provided on the drives.

The drive has the following sensor systems:

1. An optical Track 0 switch senses when the Head/Carriage Assembly is positioned at Track 0.
2. An index sensor, which consists of a magnetic pick-up and index hole positioned to provide an analog signal when an index hole is detected.

1.5 PHYSICAL DESCRIPTION

The TM500 drive is shown in Figure 1-1. The drives contain 130 millimeter storage media that rotate at 3600 RPM, using a direct drive, brushless D. C. motor. The recording is accomplished by noncontact standard recording heads that are moved by a precision split band positioning device and stepper motor.

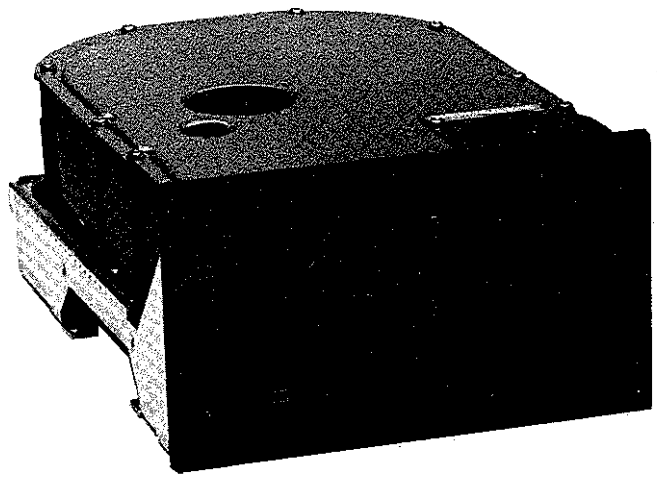


FIGURE 1-1
DISK DRIVE

The Head Disk Assembly is enclosed in a sealed cast aluminum housing, which includes an air filtration system to ensure a contamination-free environment. The housing is shock mounted to a metal frame that has the front panel attached, and threaded holes on the sides and bottom for mounting the drive onto a chassis.

In addition, the drive includes the read/write control electronics, the servo spindle control electronics, an index sensor, a brake assembly, and a front panel indicator.

SECTION 2

PRODUCT SPECIFICATIONS

INTRODUCTION

This section contains the mechanical, electrical and operational, reliability, and environmental specifications for the TM501, TM502, and TM503 disk drives.

2.1 MECHANICAL SPECIFICATIONS

The mechanical and physical dimensions are contained in Figure 2-1.

2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

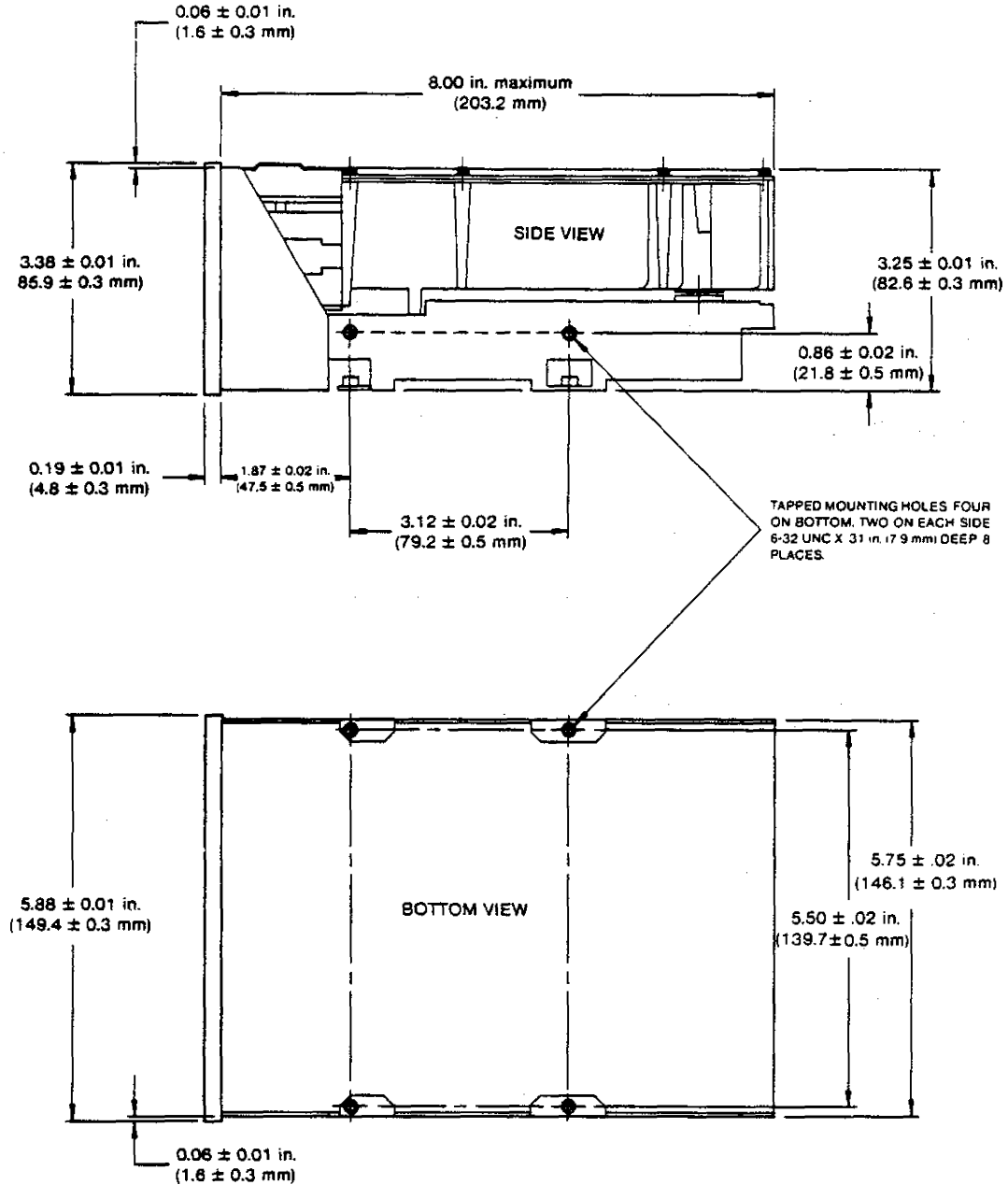
The electrical and operational specifications are contained in Table 2-1. Typical starting current requirements at nominal voltage are contained in Figure 2-2.

2.3 RELIABILITY SPECIFICATIONS

The reliability specifications are contained in Table 2-2.

2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are contained in Table 2-3.



Note: Weight is 3.0 kilograms, 6.5 pounds maximum

FIGURE 2-1
DISK DRIVE OUTLINE DRAWING

TABLE 2-1
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	Lubricated, 130 millimeter, plated aluminum disk
Tracks Per Inch	345 TPI
Spacing, Track to Track	2.9 milinches
Number of Cylinders	306 cylinders
Number of Tracks	
TM501	612 tracks
TM502	1224 tracks
TM503	1836 tracks
Disk Speed	3600 RPM ± 1 percent
Average Latency	8.33 milliseconds
Start Time	15 seconds maximum
Stop Time	15 seconds maximum
Seek Time	3 milliseconds track to track
Head Settling Time	15 milliseconds, last track accessed
Average Access Time, Including Head Settling Time, 3 Millisecond Step Rate	321 milliseconds
Average Access Time Using Buffered Seek, Including Head Settling Time	85 milliseconds
Transfer Rate	5 megabits per second

TABLE 2-1 (CONTINUED)
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Maximum Flux Reversal Density	9090 FRPI
Unformatted Capacity Per Drive	
TM501	6.38 megabytes
TM502	12.76 megabytes
TM503	19.14 megabytes
Unformatted Capacity Per Surface	3.19 megabytes
Unformatted Capacity Per Track	10.4 kilobytes

POWER REQUIREMENTS

+12 volts D. C. ±10 percent, 1.5 amperes typical, 5 amperes maximum during motor start-up, not to exceed 12 seconds, 2 amperes maximum running, with no more than 50 millivolts Periodic and Random Deviation (PARD).

+5 volts D. C. ±5 percent, 0.8 amperes typical, 1.2 amperes maximum running, with no more than 50 millivolts PARD.

There are no restrictions in sequencing power supplies on or off.

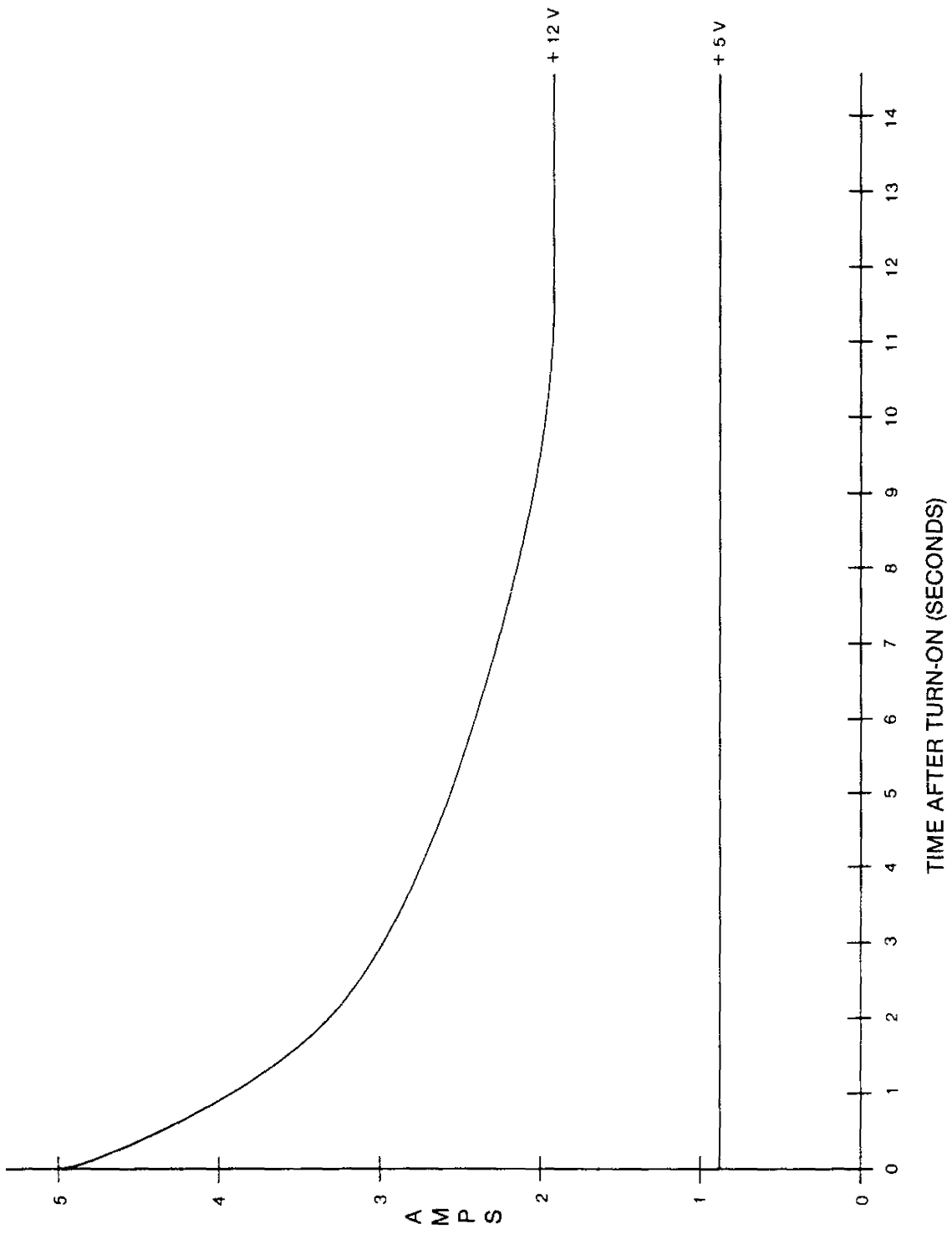


FIGURE 2-2
TYPICAL STARTING CURRENTS

TABLE 2-2
RELIABLILITY SPECIFICATIONS

SOFT AND HARD READ ERROR RATES, EXCLUSIVE OF MEDIA DEFECTS

For data that has been verified previously as error free, and when used in conjunction with a data separator and phase lock loop of good design, the recoverable (soft) read error rate for any subsequent read operation shall not exceed one error in 1×10^{10} bits transferred. A recoverable read error is an error that may be corrected within five attempts to reread the data.

The nonrecoverable (hard) read error rates shall not exceed one error in 1×10^{12} bits transferred. A nonrecoverable read error is an error that may not be corrected within five attempts to reread data, providing that the writing of the data previously has been verified as correct. The seek error rate is not to exceed one error in 1×10^{6} seeks.

MEDIA DEFECTS

Any defects on the media surface will be identified on a defect map provided with each drive. This defect map will indicate the head number, track number, and number of bytes from index for each defect. Each defect shall be no longer than 16 bits. Cylinders 000 and 001 are guaranteed error free.

The map is offered as a guide only. The number of defects and their location can change due to customer system variations such as data separators.

Mean Time Between Failures	11,000 power on hours
Mean Time To Repair	30 minutes
Component Design Life	5 years
Preventative Maintenance	Not required

TABLE 2-3
ENVIRONMENTAL SPECIFICATIONS

Ambient Temperature	
Operating	4°C to 50°C, 39°F to 122°F
Nonoperating	-40°C to 60°C, -40°F to 140°F
Temperature Gradient	
Operating	10°C per hour, 18°F per hour
Nonoperating	Below that causing condensation
Relative Humidity	8-to-80 percent, noncondensing
Relative Humidity Gradient	
Operating	20 percent per hour
Nonoperating	Below that causing condensation
Maximum Wet Bulb Temperature	26°C, 78.8°F, without condensation
Elevation	
Operating	Density Altitude: -457 to 2,972 meters, -1,500 to 9,750 feet
Nonoperating	Sea level to 3,650 meters, Sea level to 12,000 feet

SECTION 3

OPERATION

INTRODUCTION

This section contains information pertinent to the handling, inspection, installation, and operation of the TM500 series of drives.

3.1 UNPACKING THE DRIVE

Each drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment.

Visually examine the shipping container for possible damage. Notify the carrier immediately if any damage is found.

The following procedure is recommended for unpacking the drive.

1. Place the shipping container on a flat work surface.
2. Cut the tape on the shipping container.
3. Remove the foam lid and pads from the shipping container.
4. Remove the inner container.
5. Remove the drive from the inner container.
6. Place the drive on a foam lined surface.

CAUTION

Do not manually rotate the stepper motor or spindle motor. Damage to the heads and disk may result.

NOTE

The inside chamber of the drive is a sealed compartment that must not be opened.

When returning the drive to the service center, be sure to use prior steps in reverse order, and ensure the foam stiffeners in the proper location, with the cardboard dividers properly in place between the drives (see Figure 3-1).

3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, inspect for the following:

1. Ensure the front panel is secure.
2. Ensure the circuit board is secure.
3. Ensure the connectors are firmly seated.
4. Ensure there is no debris or foreign material between the frame and the head/disk casting.
5. Ensure the head/disk housing can move freely on the shock mounts of the frame.
6. Ensure the termination resistor pack and jumper blocks are firmly seated and in the correct configuration.

3.3 MOUNTING THE DRIVE

The drive can be mounted in any vertical or horizontal plane. Eight 6-32 tapped holes are provided for mounting: two on each side and four on the bottom of the frame (see Figure 2-1, page 2-2). The drive is manufactured with some critical internal alignments that must be maintained. Hence, it is important the mounting hardware does not introduce significant stress on the drive.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

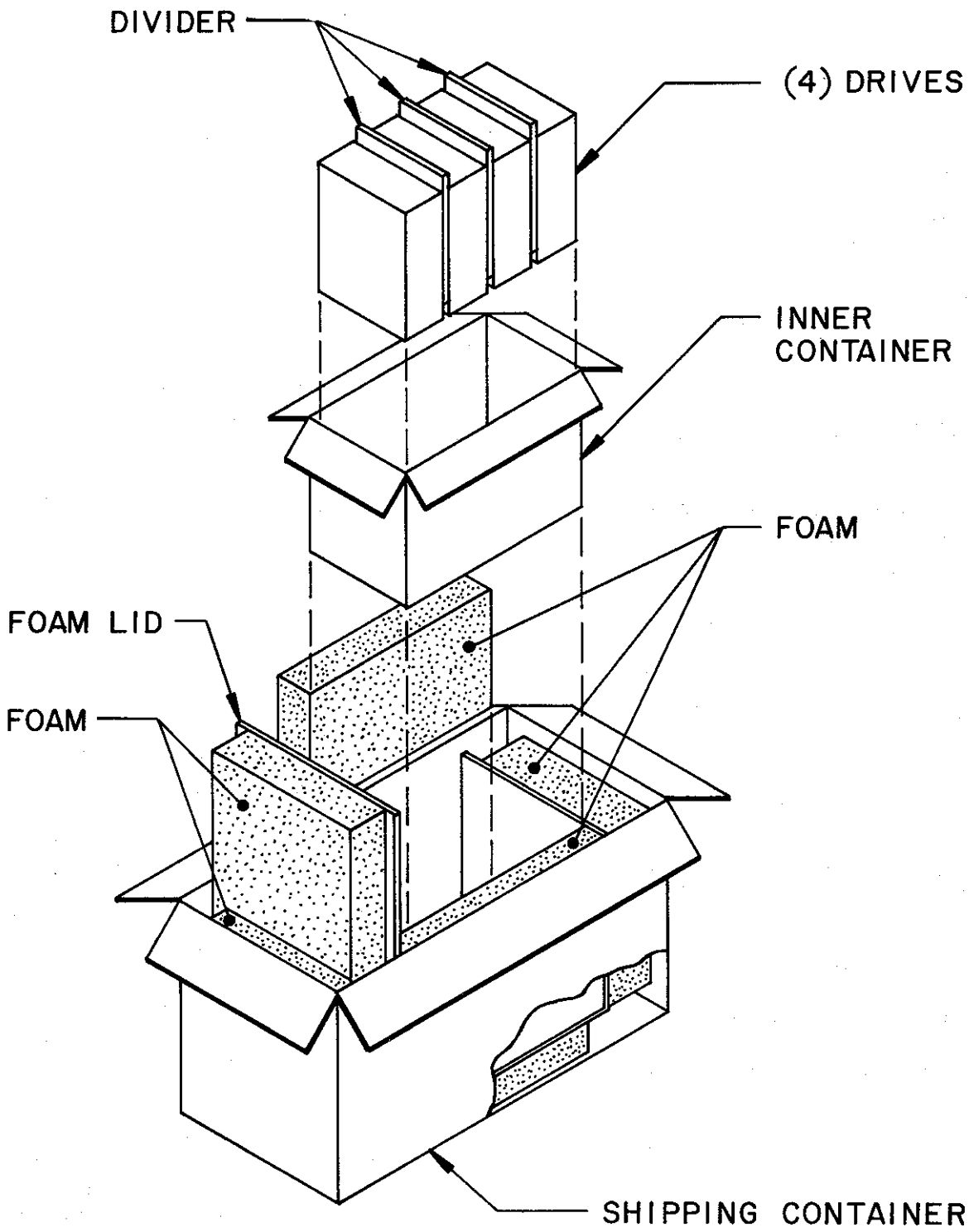


FIGURE 3-1
4-PACK SHIPPING CONTAINER

DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e.g., dust, lint, and paper chad since the drive does not have a dust cover.

FREE AIR FLOW

When the drive is mounted so the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range (see Table 2-3, page 2-7).

CONFINED ENVIRONMENT

When the drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors and the circuit boards.

3.4 INTERFACE CONNECTORS

The electrical interface between the drive and the host system is via three connectors. J1 provides control signals for the drive (see Figure 3-2). J2 provides for the radial connection of read/write data signals (see Figure 3-3). J3 provides for D.C. power (see Figure 3-4).

Table 3-1 contains interface lines. The interface description of the connectors, and the location of each, is contained in this section.

J1/P1 CONNECTOR

Connection to J1 is through a thirty-four-pin circuit board connector. Figure 3-2 contains the dimensions of this connector. The pins are numbered 1 through 34. The even pins are located on the component side of the circuit board. Pin 2 is located on the end of the circuit board connector closest to the D. C. power connector J3/P3, and is labeled. A key slot is provided between Pins 4 and 6. The recommended mating connector for P1 is 3M ribbon connector P/N 3463-0001, without ears.

J2/P2 CONNECTOR

Connection to J2 is through a 20-pin circuit board edge connector. Figure 3-3 contains the dimensions of this connector. The pins are numbered 1 through 20. The even pins are located on the component side of the circuit board. The recommended mating connector for P2 is 3M ribbon connector P/N 3461-0001, without ears. A key slot is provided between Pins 4 and 6.

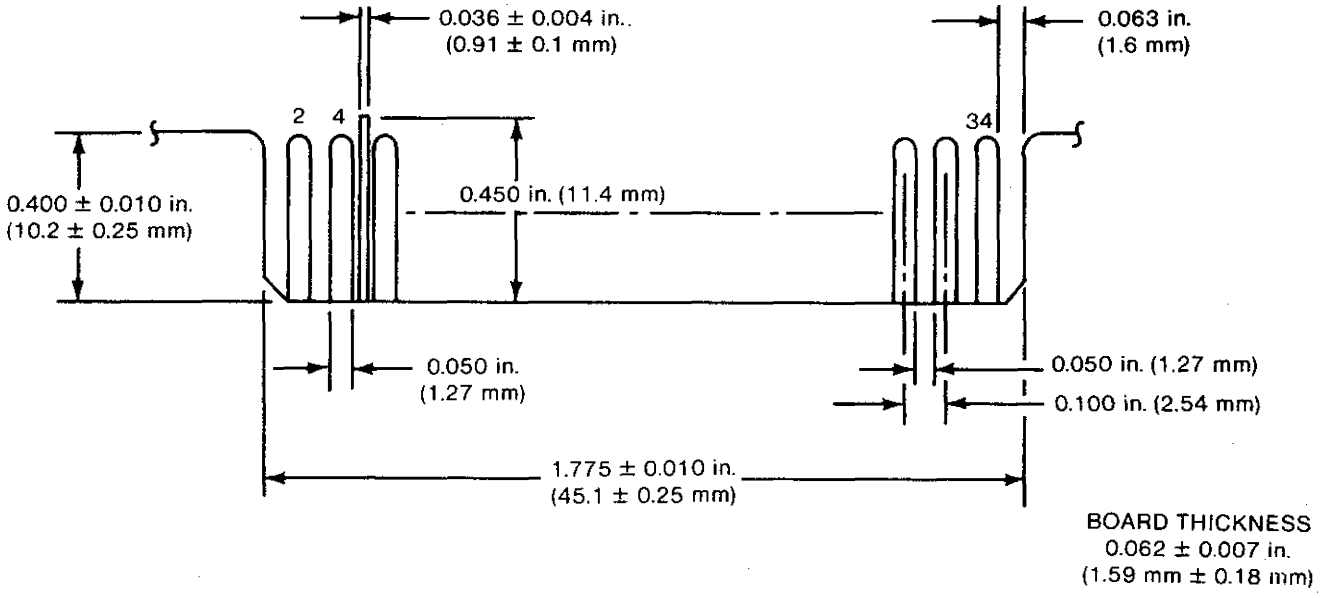


FIGURE 3-2
J1 EDGE CONNECTOR DIMENSIONS

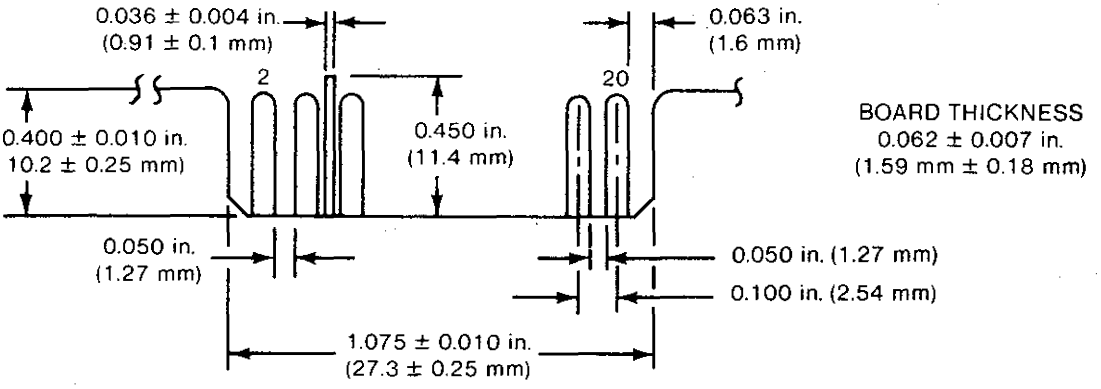


FIGURE 3-3
J2 EDGE CONNECTOR DIMENSIONS

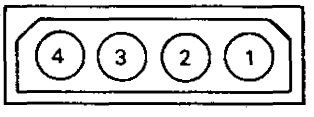


FIGURE 3-4
J3 POWER CONNECTOR

TABLE 3-1
DRIVE INTERFACE SIGNALS AND PIN ASSIGNMENTS

Connector	Interface Pin Number Signal	Ground	Signal Type	I/O	Name of Signal
P1	2	(1)	S	I	Spare
↑	4	(3)	S	I	Head Select 2^2
	6	(5)	S	I	Write Gate
	8	(7)	S	O	Seek Complete
	10	(9)	S	O	Track 0
34-Pin	12	(11)	S	O	Fault
Ribbon	14	(13)	S	I	Head Select 2^0
Daisy	16	(15)	—	—	Reserved (To J2 - 7)
Chain	18	(17)	S	I	Head Select 2^1
	20	(19)	S	O	Index
	22	(21)	S	O	Ready
	24	(23)	S	I	Step
	26	(25)	S	I	Drive Select 0
	28	(27)	S	I	Drive Select 1
	30	(29)	S	I	Drive Select 2
	32	(31)	S	I	Drive Select 3
P1	34	(33)	S	I	Direction In
P2	1	(2)	S	O	Drive Select
↑	3	(4)	S	—	Spare
	5	(6)	—	—	Reserved
	7	(8)	—	—	Reserved (To J1-16)
20-Pin	9	(10)	—	—	Spare
Ribbon	11	(12)	—	—	Ground
Radial	13	—	D	I	+ Write Data
	14	—	D	I	− Write Data
	15	(16)	—	—	Ground
	17	—	D	O	+ Read Data
	18	—	D	O	− Read Data
P2	19	(20)	—	—	Ground
P3	1			—	+ 12 volts D. C. In
↑	2			—	+ 12 volts D. C. Return
Radial	3			—	+ 5 volts D. C. Return
P3	4			—	+ 5 volts D. C. In

NOTES:
1. S = Single Ended
2. D = Differential
3. I = Drive Input
4. O = Drive Output

J3/P3 CONNECTOR

D. C. power connector J3 is a four-pin AMP Mate-N-Lok connector, P/N 350211-1, mounted on the solder side of the circuit board. The recommended mating connector, P3, is AMP P/N 1-480424-0, utilizing AMP pins P/N 60619-4. J3 pins are labled on the J3 connector (see Figure 3-4). J3 cabling must be 18 AWG, minimum.

FRAME GROUND CONNECTOR

The frame ground connector is Faston AMP P/N 61761-2. The recommended mating connector is AMP P/N 62187-1. To realize error rates (see Table 2-2), it must be connected directly to the centrally located system ground via an 18 AWG, minimum, cable.

3.5 INTERFACE LINE DESCRIPTIONS

The interface for the TM500 series drive is available in one configuration. It is compatible with industry standard drives. Compatibility is defined as using the same pin assignment where the signal and function are common. Table 3-1 contains pin assignments.

The interface may be connected in the radial or daisy chain configuration (see Figures 3-5 and 3-6).

INPUT CONTROL SIGNALS

The input control signals are of two kinds: those to be multiplexed in a multiple drive system and those that do the multiplexing. The input control signals to be multiplexed are: Reduced Write Current, Write Gate, Head Select Line 2^0, Head Select Line 2^1, Head Select Line 2^2, Step, and Direction In. The multiplexing signal is Drive Select 0, Drive Select 1, Drive Select 2 or Drive Select 3.

The input signals have the following electrical specifications, as measured at the drive. Figure 3-7 illustrates the recommended circuit.

True: 0.0 volt D. C. to 0.4 volt D. C. at I = -40 milliamperes, maximum

False: 2.5 volts D. C. to 5.25 volts D. C. at I_L = 250 microamperes, maximum (open)

All input signals share a 220/330 ohm resistor pack for line termination. Only the last drive in the chain should have the resistor pack installed.

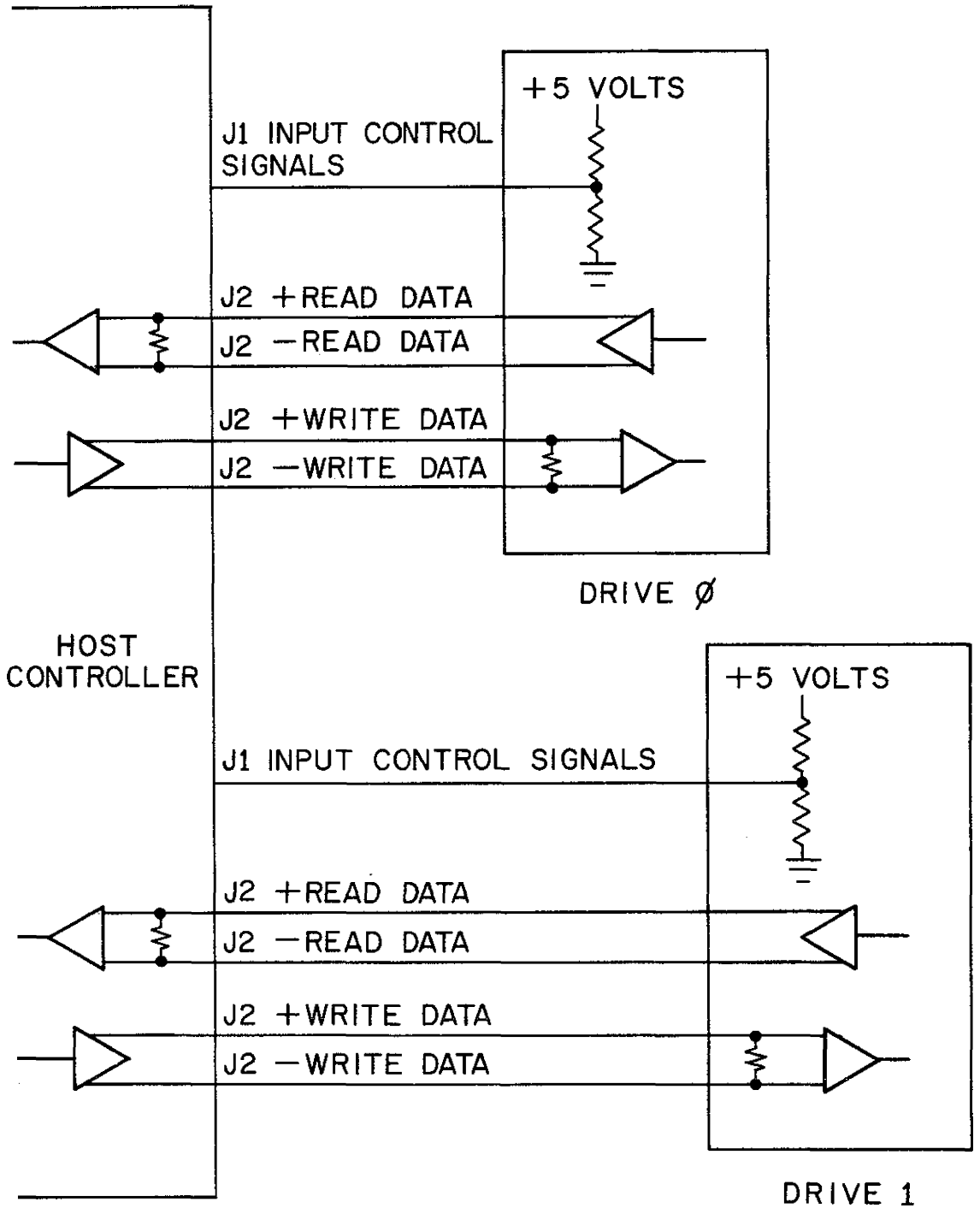


FIGURE 3-5
RADIAL CONFIGURATION

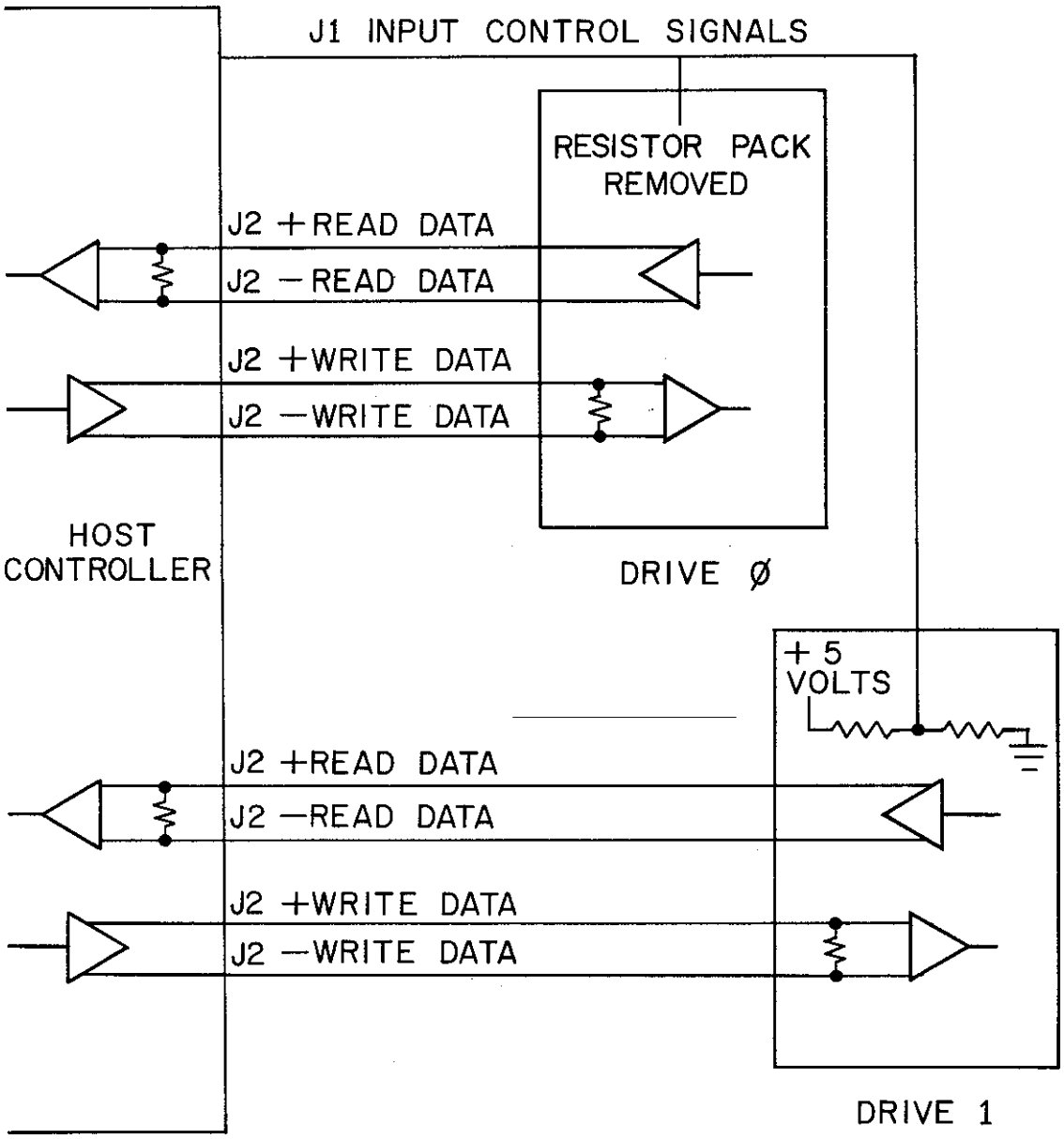


FIGURE 3-6
DAISY CHAIN CONTROL LINES

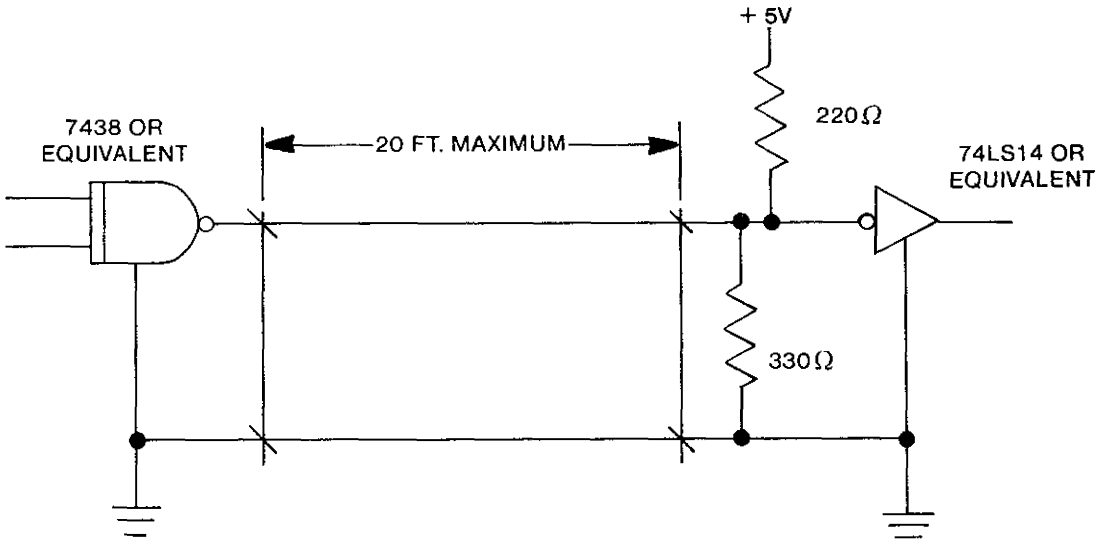


FIGURE 3-7
CONTROL SIGNAL/DRIVER RECEIVER CIRCUIT COMBINATION

WRITE GATE

The active state of this signal or logical zero level enables write data to be written on the disk. The inactive state of this signal enables the data to be transferred from the drive. In addition, the inactive state enables the step pulse to step the read/write actuator.

HEAD SELECT LINES 2^0, 2^1, 2^2

These three lines provide for the selection of each read/write head in a binary coded sequence. Head Select Line 2^0 is the least significant line. The heads are numbered 0 through 5. When all Head Select Lines are false, Head 0 is selected. Table 3-2 describes which head is selected for the head select lines.

TABLE 3-2
HEAD SELECT LINES

Head Select Line			Head Selected	
2^2	2^1	2^0	Jumper 3 PW13 OUT TM501, TM502	Jumper 3 PW13 IN TM503
1	1	1	0	0
1	1	0	1	1
1	0	1	2	2
1	0	0	3	3
0	1	1	0	4
0	1	0	1	5
0	0	1	2	0
0	0	0	3	1

Head recovery time (head-to-head select, write-to-read recovery, or read-to-write recovery) is 2.4 microseconds maximum.

STEP

This interface line is a control signal that causes the read/write heads to move with the direction of motion defined by the Direction In line.

The access motion is initiated at the logical true-to-logical false transition or the trailing edge of this signal pulse. Any change in the Direction in line must be made at least 100 nanoseconds before the true-to-false edge of the step pulse. The quiescent state of this line should be held logically false.

The read/write head moves at the rate of the incoming step pulses. The minimum time between successive steps is three milliseconds, except during execution of a buffered seek. The minimum pulse width is one microsecond. Figure 3-8 illustrates the step timing.

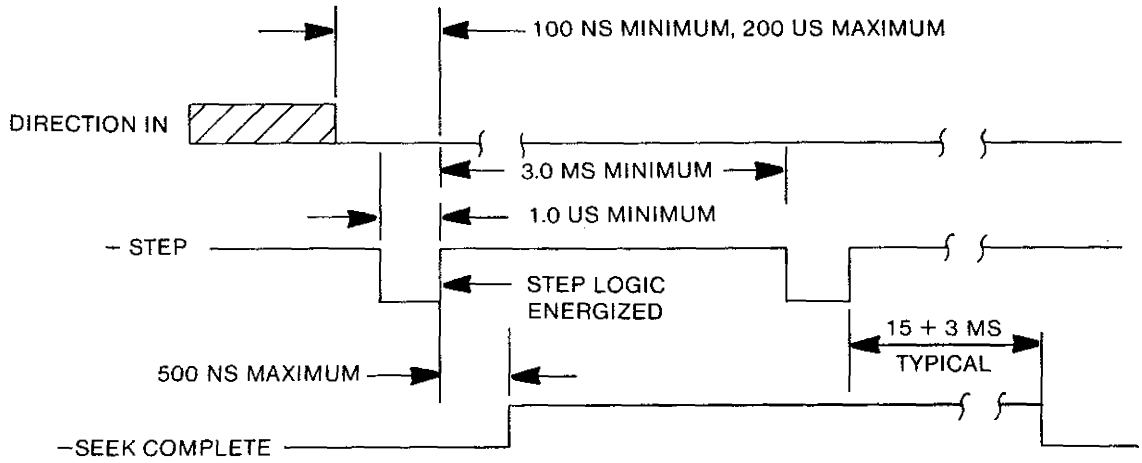


FIGURE 3-8
STEP MODE TIMING

BUFFERED SEEK

The buffered seek uses an onboard microprocessor that calculates the most efficient seek algorithm for the user. The user need only issue step pulses in accordance with the timing shown (see Figure 3-9). Step pulses are issued in a 1:1 ratio to the cylinders moved. If more pulses are issued than there are cylinders left to move, the heads soft stop at the last cylinder.

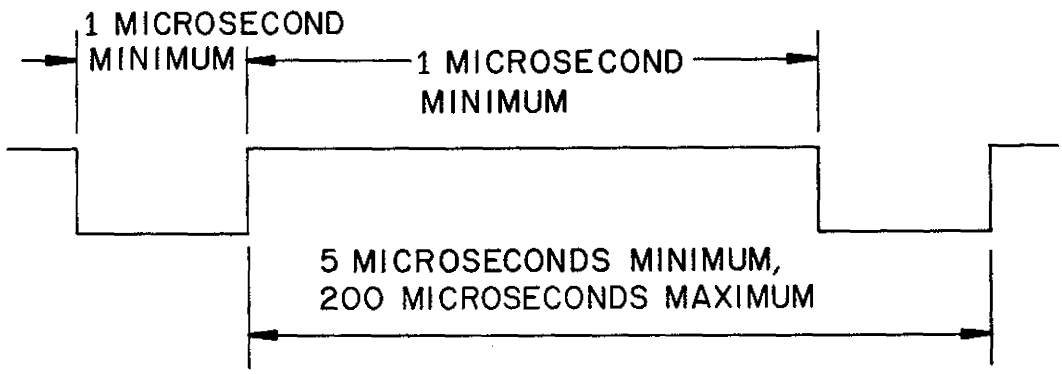


FIGURE 3-9
BUFFERED SEEK STEP PULSES

DIRECTION IN

This signal defines the direction of motion of the read/write head when the Step line is pulsed. An open circuit or logical false defines the direction as "out". If a pulse is applied to the Step line, the read/write heads move away from the center of the disk. If this line is true, the direction is defined as "in", and the read/write heads move in toward the center of the disk.

Seek Complete must be true prior to changing directions and the application of additional step pulses.

REDUCED WRITE CURRENT

The Reduced Write Current input line is terminated, but is not used in the TM500 series drives. The microprocessor automatically switches write current.

DRIVE SELECT 0 THROUGH DRIVE SELECT 3

These control signals enable the selected drive's input receivers and output drivers. When logically false, the output drivers are open circuits and the input receivers do not acknowledge signals presented to them.

Selecting the appropriate jumper block at W9 through W12 determines which select line activates the drive.

NOTE
Only one drive may be selected at a time.

OUTPUT CONTROL SIGNALS

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40 milliamperes in a true state, with a maximum voltage of 0.4 volt measured at the driver. When the line driver is in the false state, the driver transistor is off, and the collector cutoff is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective Drive Select lines.

SEEK COMPLETE

The Seek Complete signal goes true when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when Seek Complete is false.

Seek Complete goes false:

1. When a recalibration sequence is initiated by the microprocessor at power on because the read/write heads are not over Track 0.
2. 500 nanoseconds, maximum, after the trailing edge of a step pulse or a series of step pulses.
3. When power is momentarily lost, Seek Complete is false when power is restored and remains false until an automatic recalibration is completed.

TRACK 0

The Track 0 signal indicates a true state only when the drive's read/write heads are positioned at Track 0, the outermost data track.

FAULT

The Fault signal is used to indicate a condition exists in the drive that could cause improper writing on the disk. When this line is true, further writing is inhibited, as are other drive functions, until the condition is corrected.

This condition is caused by either the +12 volt or +5 volt supply dropping below the specified limits, and on power up until a successful recalibration sequence is completed.

INDEX

The Index signal is provided once each revolution, 16.7 milliseconds nominal, to indicate the beginning of the track. Normally, this signal is false and makes the transition to true to indicate Index. Only the transition from logical false to logical true is valid.

READY

When true, the Ready signal, together with Seek Complete, indicates that the drive is ready to read, write or seek, and the I/O signals are valid. When this line is false, all controller-initiated functions are inhibited.

The typical time after power on for Ready to be true is fifteen seconds. Track 0, Seek Complete, and Ready come true sequentially during power on.

SELECT STATUS

A Status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The Drive Selected line is driven by a TTL open collector drive (see Figure 3-7). This signal goes active only when the drive is programmed as Drive X, X = 0, 1, 2, or 3, by programming the shunt on the drive, and the Drive Select X line at J1/P1 is activated by the host system.

DATA TRANSFER SIGNALS

All lines associated with the transfer of data between the drive and the host system are differential in nature and may be multiplexed. These lines are provided at the J2/P2 connector on all drives. Signal levels are defined by RS-422A.

Two pairs of balanced lines are used for the transfer of data: MFM Write Data and MFM Read Data. Figure 3-10 illustrates the driver/receiver combination used with the drive for data transfer signals.

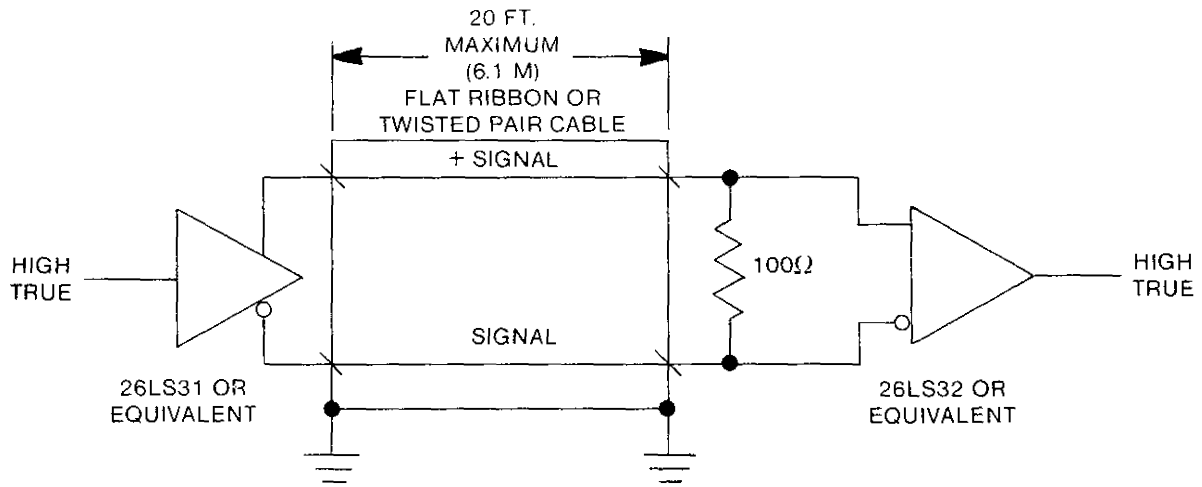


FIGURE 3-10
DATA TRANSFER LINE DRIVER RECEIVER

MFM WRITE DATA

This is a differential pair of lines that define the flux transition to be written on the track. The transition of the +MFM Write Data line going more positive than the -MFM Write Data line causes a flux reversal on the track if Write Gate is active. This signal must be driven to an inactive state, +MFM Write Data more negative than -MFM Write Data, by the host system when in a read mode.

The delay from the leading edge of Write Gate to the Write Data pulse is 400 nanoseconds, maximum.

MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM Read Data line going more positive than the -MFM Read Data line represents a flux reversal on the track of the selected head.

3.6 DRIVE ADDRESS AND OPTION SELECTION

The drive address and option selection is determined by the programmable jumper blocks located on the logic circuit board. If jumper configurations are changed, power should be cycled off and on, so that the microprocessor can recognize the new configuration.

The option programming guide is contained in Table 3-3.

3.7 SHIPPING PACK AND HANDLING

Figures 3-11 through 3-13 provide basic information on recommended design guidelines for packaging systems.

From various drop tests conducted, it has been established that drives subjected to shock loads in excess of twenty G's may be damaged and consequently not meet published performance specifications for data reliability, margins, and function.

In order to avoid media or head damage, it is recommended that:

1. Drive mounting designs incorporate some type of shock dampening consideration.

2. Shipping cartons protect the drive within the system to withstand twenty G's.

3. Individual drives are handled carefully, e.g., receiving and in-process personnel are properly trained, surface mats are used on working surfaces to prevent the possibility of "handling shock," and padding is placed on racks and carts.

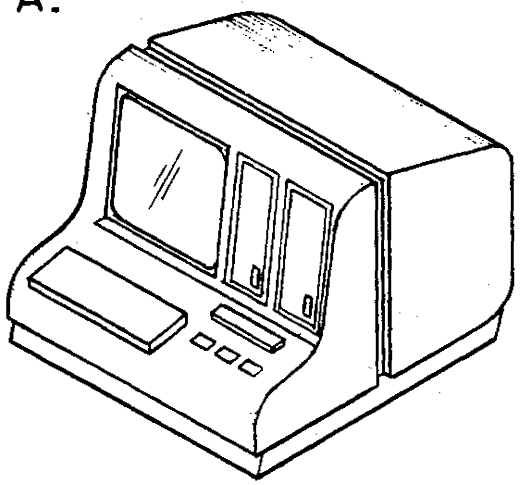
Please emphasize the critical aspects of handling these drives to all concerned people. In addition, Tandon provides technical assistance on packing and handling to customers upon request.

TABLE 3-3
OPTION PROGRAMMING GUIDE

1-W3 Jumper	Function	Factory Programmed	Usage
W1	Track Fault	O	Install for excess track fault.
W2	Test	O	Install for factory test.
W3	Disable Limit	O	Install to disable soft limits.
W4	Spin Select	O	Install for spin select.
W5	Tracks	S	Install for standard version only.
W6	Motor Type	—	Install for Type 1.8° motor.
RTW7	Read Terminator	I	Close only at end drive of daisy chain data. Closed for radial data.
WTW8	Write Terminator	I	
S4W9	Drive Select 4	O	Install one of four plugs only.
S3W10	Drive Select 3	O	Plug corresponds to drive address.
S2W11	Drive Select 2	O	
S1W12	Drive Select 1	I	
3PW13	Three Disk	503	Close for Model TM503 only.
U22	Terminator Pack	I	Install in end drive of daisy chain.

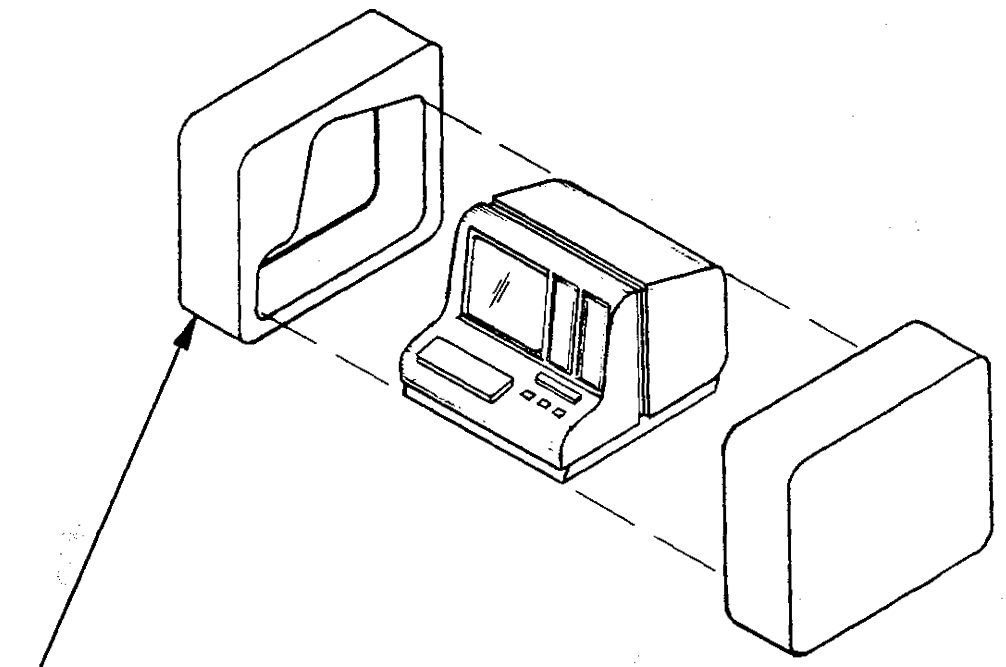
NOTES:
O = Omit
I = Install
S = Close jumper for standard version only.
503 = Close jumper for TM503 only.

STEP A.



ENCLOSE UNIT IN POLY G
TO AVOID SURFACE
SCRATCHES AND
OTHER DAMAGE

STEP B.



MOLD POLYURETHANE
"CLAMSHELL" TO "CUBE" UNIT

FIGURE 3-11
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 1

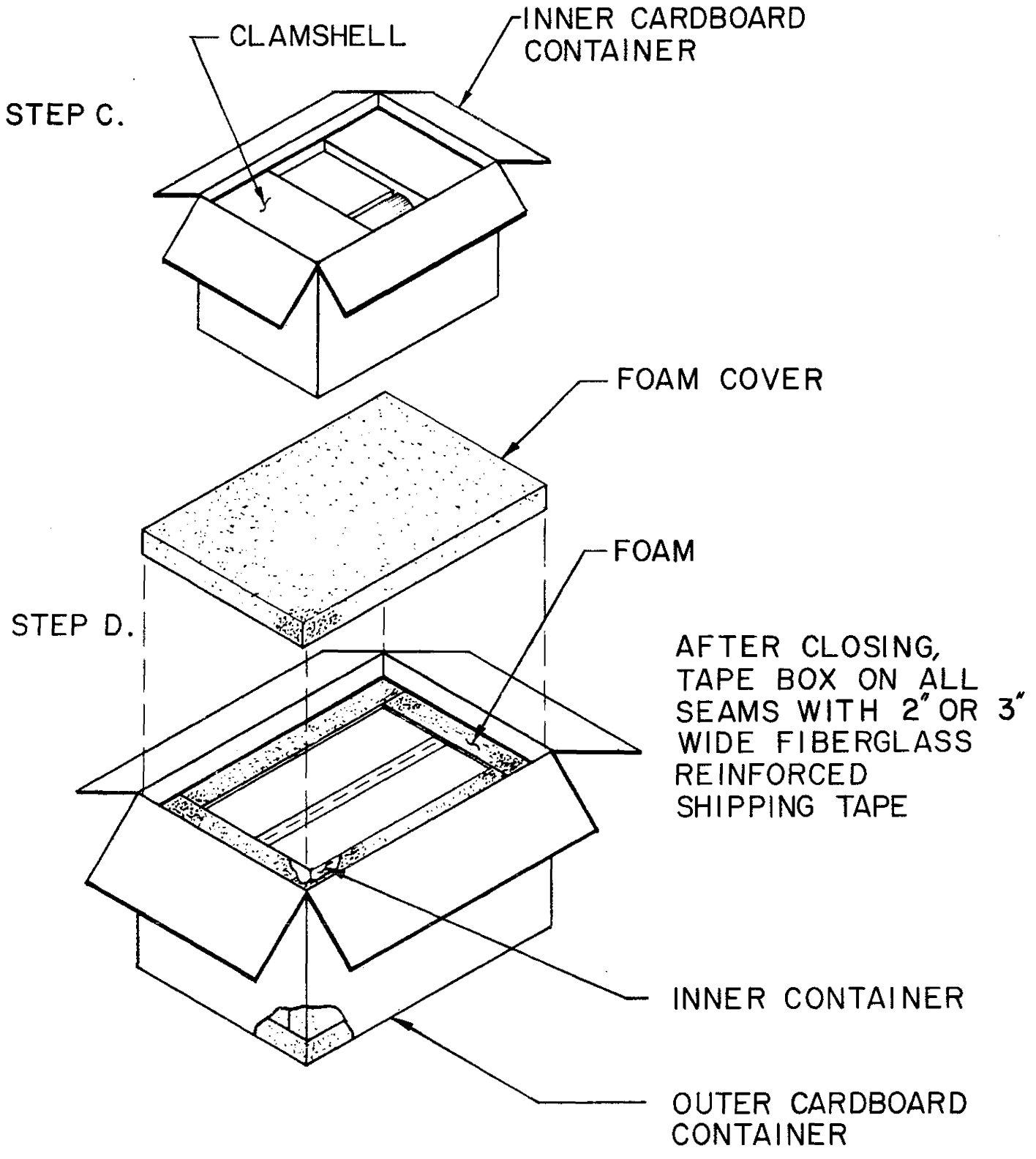


FIGURE 3-11 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 1

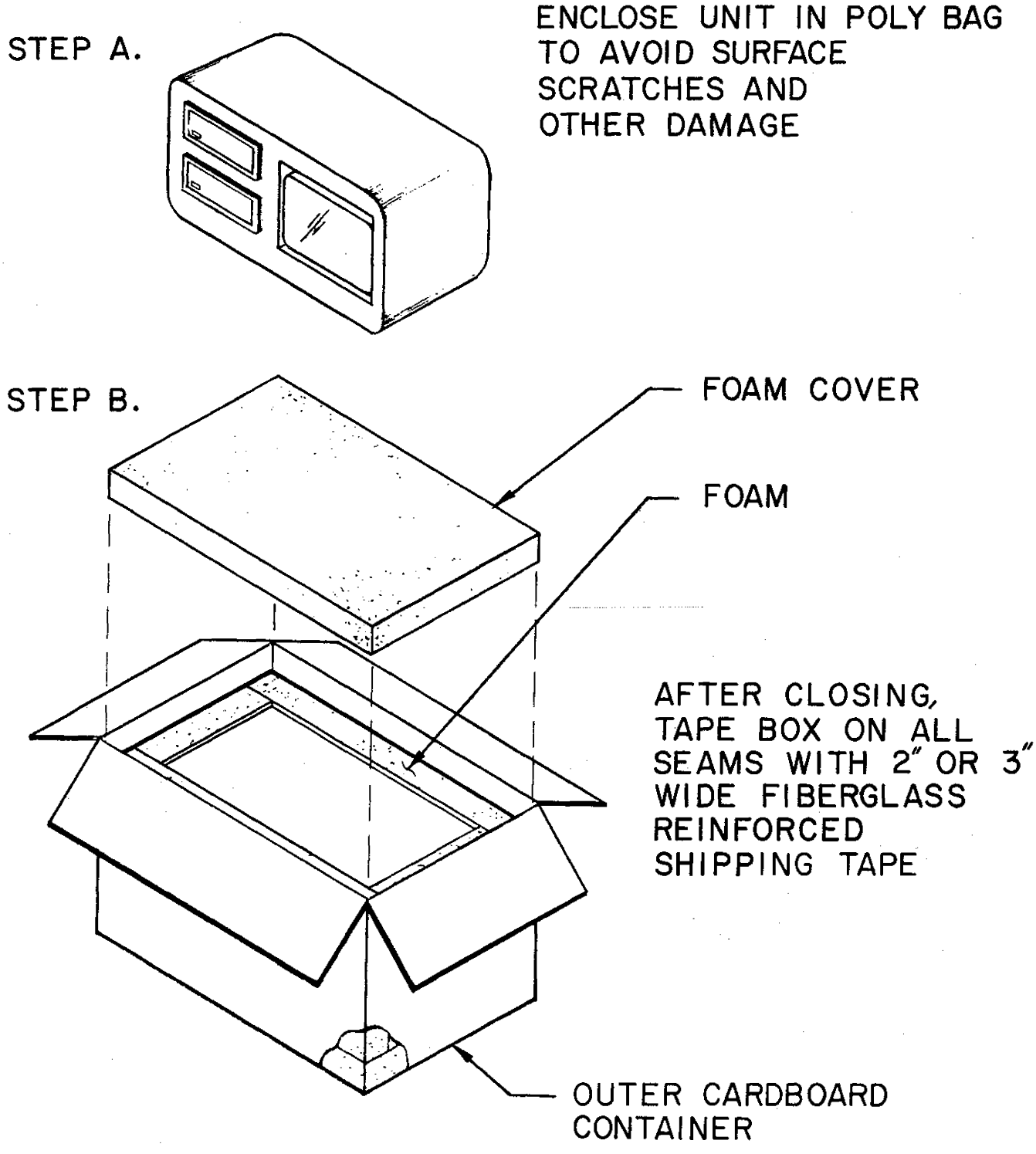
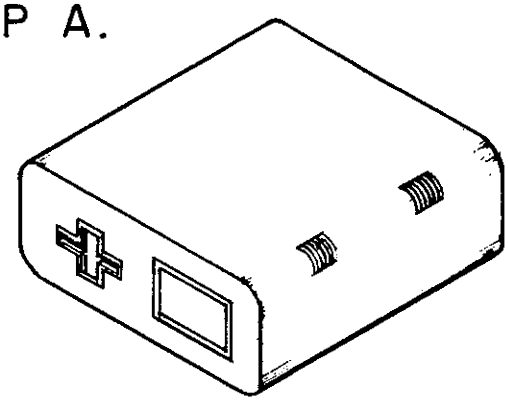


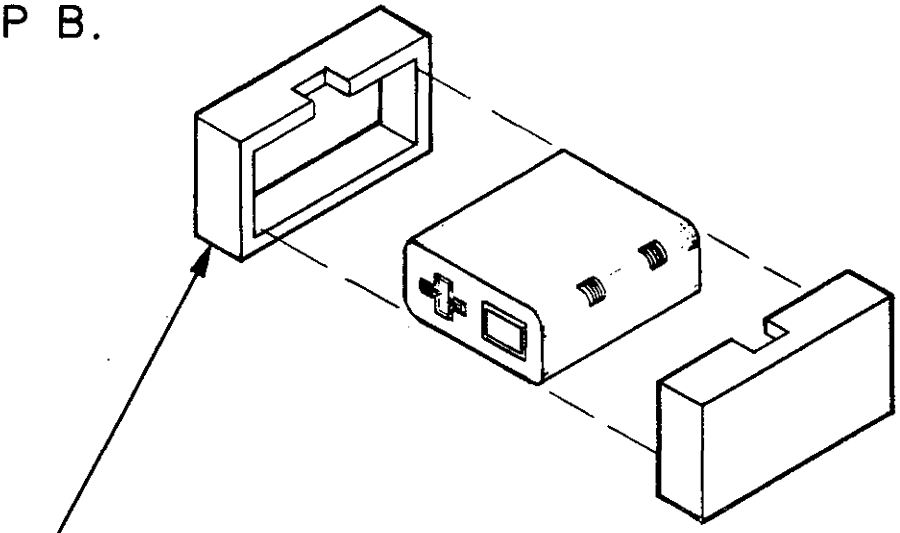
FIGURE 3-12
RECOMMENDED SHIPPING PACK DESIGN, CONFIGURATION 2

STEP A.



ENCLOSE UNIT IN POLY BAG TO AVOID SURFACE SCRATCHES AND OTHER DAMAGE

STEP B.



MOLDED POLYURETHANE "CLAMSHELL" TO "CUBE" UNIT

FIGURE 3-13
RECOMMENDED SHIPPING PACK DESIGN, CONFIGURATION 3

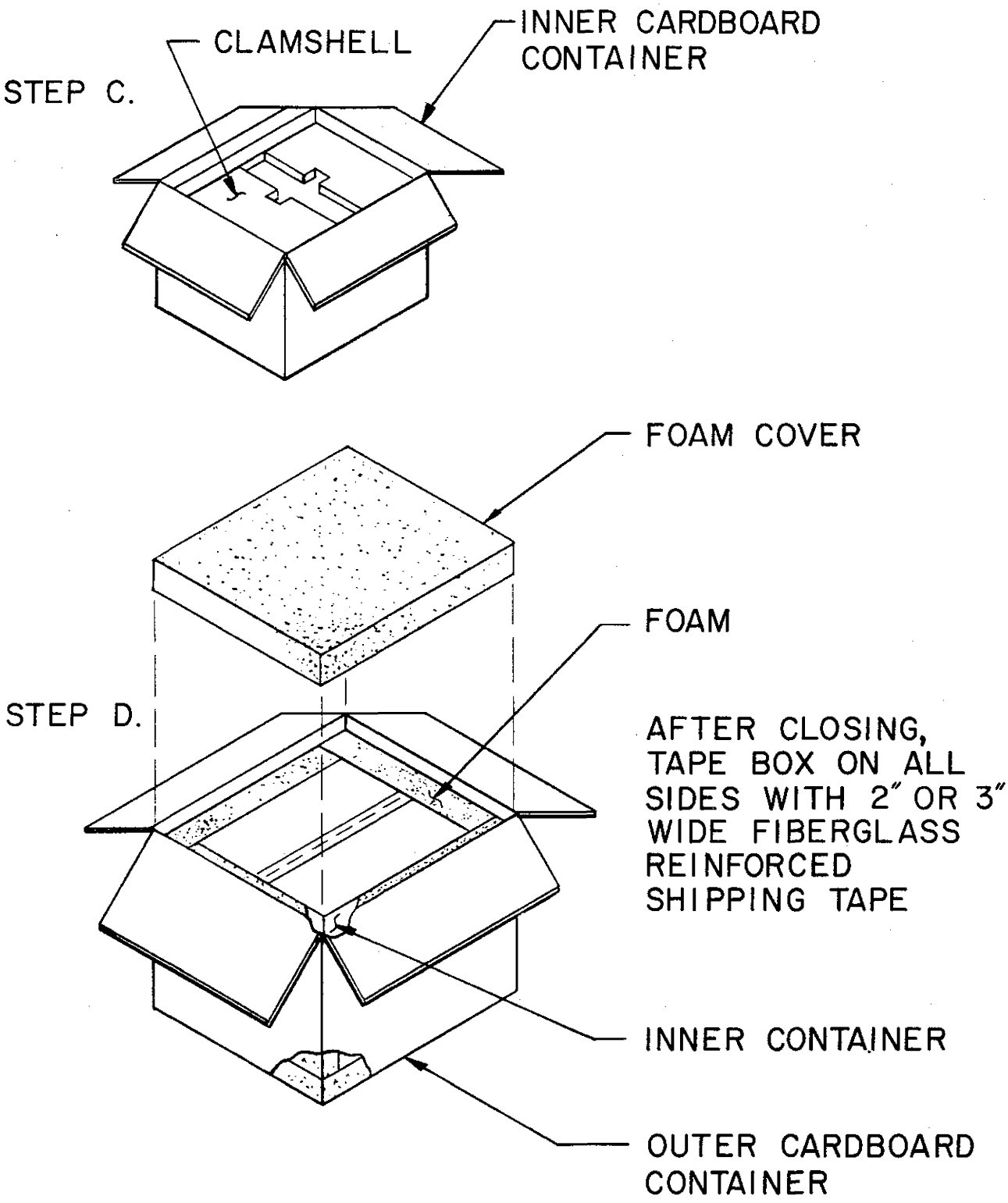
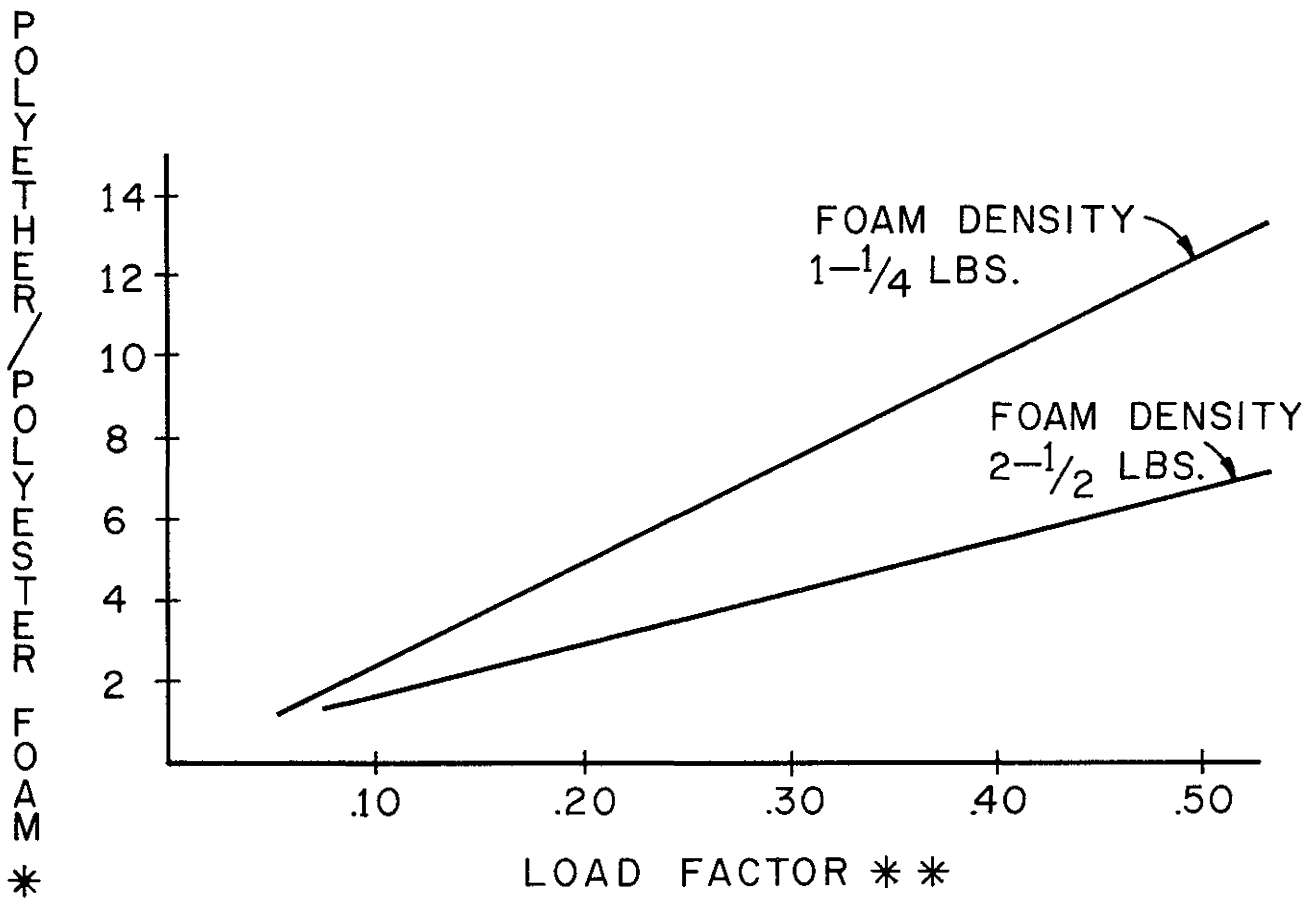


FIGURE 3-13 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 3



NOTE

THE GRAPH GIVES FOAM THICKNESSES TO SATISFY 10 G MINIMUM SHOCK LOADS ON STANDARD 30-INCH DROP TEST. HENCE, ALL PACKAGE DESIGNS SHOULD BE TESTED TO VERIFY THEIR ULTIMATE PERFORMANCE.

* THICKNESS IS IN INCHES.

** THE LOAD FACTOR IS IN LBS. PER SQ. INCH.

THE FORMULA IS : $\text{LOAD FACTOR} = \frac{\text{UNIT'S WEIGHT (LBS.)}}{\text{SMALLEST SIDE OF UNIT (SQ. INCHES)}}$

FIGURE 3-14
LOAD GRAPH

SECTION 4

TROUBLESHOOTING GUIDE AND REPLACEMENT PROCEDURE

INTRODUCTION

This section is designed to help locate and correct failures related to the drive. Table 4-2 is a troubleshooting guide outlining the problem, its possible cause, and the recommended action. This section also contains parts removal, replacement, and adjustment procedures.

In all cases, the power supply voltages should be checked before proceeding.

4.1 TROUBLESHOOTING GUIDE

TEST EQUIPMENT

The following test equipment, or its equivalent, is recommended:

1. Oscilloscope, Tektronix 465—vertical and horizontal sensitivity plus three percent specified accuracy—with three 10X probes, each with individual ground leads.

2. Counter Timer, Monsanto Model 100B.

3. Digital Voltmeter (DVM), John Fluke Model 800A.

TEST POINTS

Table 4-1 contains each test point by function name. All test points referred to are on the logic board. Figure 4-1 illustrates their locations.

TABLE 4-1
TEST POINTS

Test Point	Signal
1, 4, 9, 11, 12, 13, 16, 17	Logic Ground
2	Direction
3	Index
5	Photo Sensor, Track 0
6	Track 0
7	Step
8	Seek Complete
10	Pulse Read Data
14	− Analog Read Data
15	+ Analog Read Data
18	Reserved + 5 volts D. C.
19	Cable Detect + 5 volts D. C.

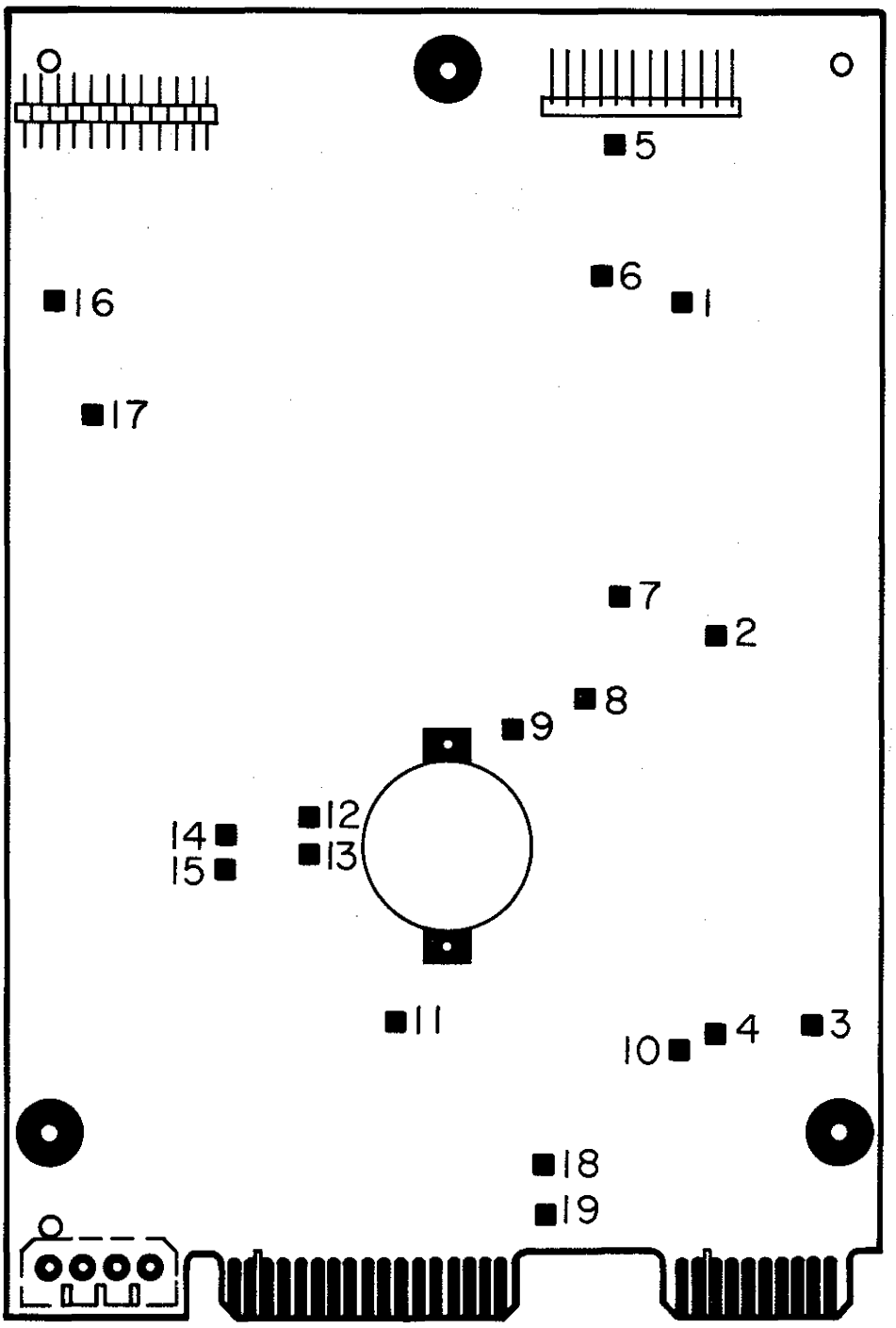


FIGURE 4-1
TEST POINT LOCATIONS

TABLE 4-2
TROUBLESHOOTING GUIDE

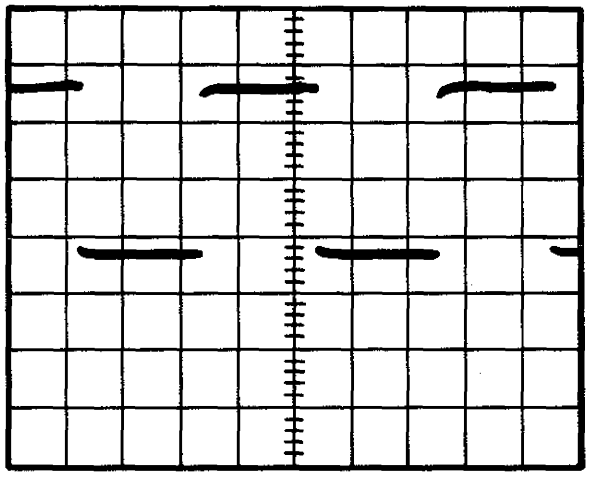
Problem	Possible Cause	Recommended Action
No activity lamp.	Not selected.	Check for correct drive select jumper.
	Lamp not plugged in.	Check Connector P-7.
	Lamp faulty.	Replace lamp.
	Logic board faulty.	Replace logic board.
No index.	Not selected.	Check drive select jumper.
	Index sensor not plugged in.	Check Connector P-5
	Index sensor misadjusted.	Readjust Index sensor.
	Index sensor faulty.	Replace sensor.
	Logic board faulty.	Replace logic board.
No Track 0.	Not selected.	Check drive select jumper.
	Track 0 sensor not plugged in.	Check Connector P-9.
	Track 0 sensor misadjusted.	Readjust Track 0 sensor.
	Track 0 sensor faulty.	Replace Track 0 sensor.
	Logic board faulty.	Replace logic board.
Drive not ready.	Not selected.	Check drive select jumper.
	No index.	See "No index."
	No Track 0.	See "No Track 0."
	Motor not up to speed or not turning.	See "Motor not up to speed, not turning."
	Drive does not seek. Drive does not restore.	See "Drive does not seek or restore."

TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

Problem	Possible Cause	Recommended Action
Drive does not seek or restore.	Drive not selected.	Check drive select jumper.
	Stepper motor not plugged in.	Check Connector P-8.
	Logic board faulty.	Replace logic board.
	Spindle motor speed misadjusted.	Readjust spindle motor's speed.
	Stepper motor faulty.	Return to factory for repair.
	Foreign object interfering with positioning arm or damper.	Remove foreign object.
Motor not up to speed, not turning.	Spindle circuit board not plugged in.	Check Connector P-12.
	Spindle motor not plugged in.	Check Connectors P-10 and P-11.
	Faulty Spindle circuit board (see Figure 4-2).	Replace circuit board.
	Motor not up to speed.	Adjust spindle speed.
	Motor faulty.	Return to factory for repair.
	Brake misadjusted.	Readjust brake.
Does not read.	Not selected.	Check drive select jumper.
	Heads not selected.	Check head select interface lines.
		Check jumper 3P W13, installed for Model Number TM503 (see Table 3-2, page 3-10).
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty (see Figure 4-3).	Replace logic board.
	Defective head.	Return to factory for repair.

TABLE 4-2 (CONTINUED)
TROUBLESHOOTING GUIDE

Problem	Possible Cause	Recommended Action
Does not read.	Improper position.	See "Drive does not seek or restore."
	Drive not ready.	See "Drive not ready."
Does not write.	No Write Gate for writing.	Check Write Gate interface line.
	Not selected.	Check drive select jumper.
	Heads not selected.	See "Does not read."
	Head cable not plugged in.	Check Connector P-6.
	Logic board faulty.	Replace logic board.
	Defective head.	Return to factory for repair.
	Drive not ready.	See "Drive not ready."



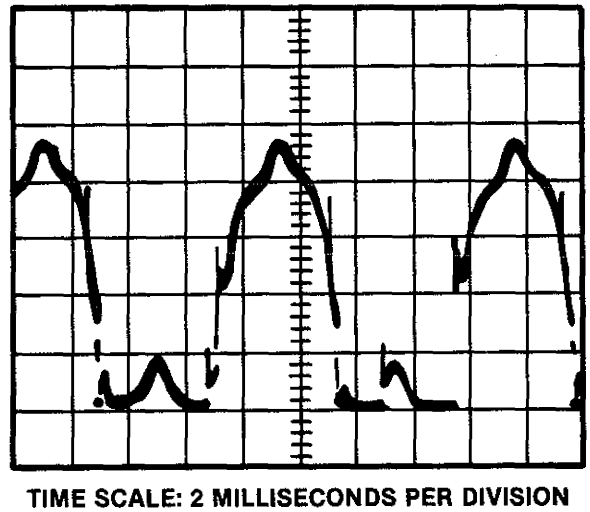
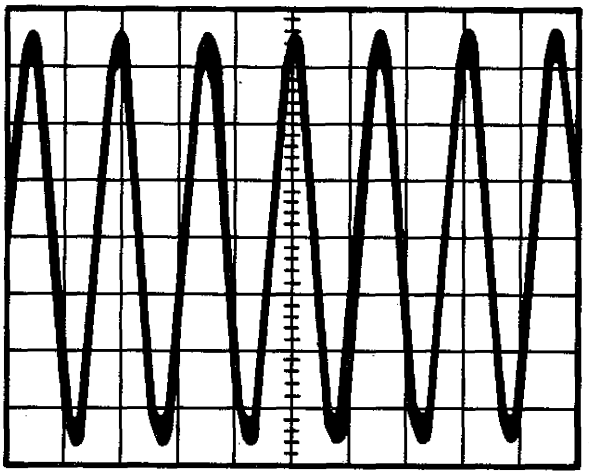
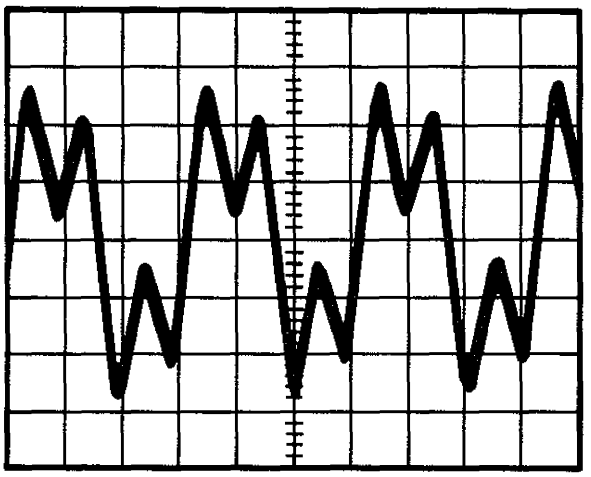


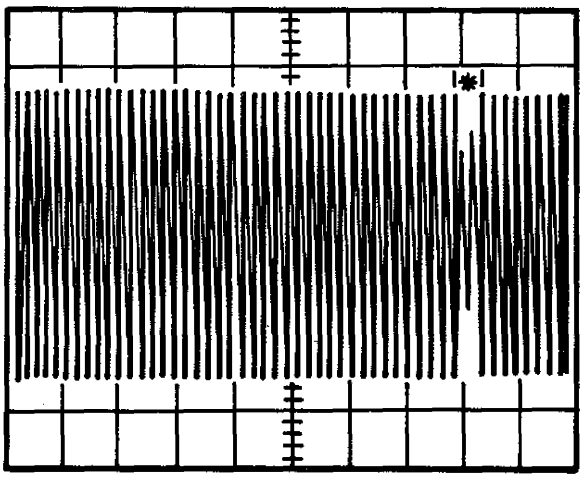
FIGURE 4-2
SPINDLE MOTOR CIRCUIT BOARD WAVEFORMS



ALL ZERO PATTERN



ALTERNATING ONES AND ZEROS



*BIT DROPOUT CAUSED BY MEDIA DEFECT

FIGURE 4-3
READ DATA WAVEFORMS 15 TPR + AND 14 TPR —

4.2 REPLACEMENT PROCEDURES

Do not rotate spindle motor or head positioning mechanism. Damage to heads and/or media may occur.

Remove power prior to replacing parts.

The following assemblies may be replaced:

Control and Data Circuit Board Assembly
Front Panel L.E.D. Assembly
Linear Brake Assembly
Front Panel
Index Assembly
Spindle Control Circuit Board Assembly
Frame Assembly
Track 0 Sensor Assembly

TOOLS REQUIRED

Number 2 Phillips screwdriver
3/16'' nut driver
5/16'' nut driver
.008'' or .010'' feeler gauge

CONTROL AND DATA CIRCUIT BOARD ASSEMBLY

REMOVAL

To remove the Control and Data Circuit Board Assembly:

1. Remove the three screws that attach the circuit board to the chassis.
2. Remove the Connectors J4 and J5 from the circuit board.
3. Slide the circuit board toward the side of the frame, lift up on the free side of it, and remove remaining connectors.

REPLACEMENT

To replace this assembly, reverse Steps 1 through 3.

FRONT PANEL L.E.D. ASSEMBLY

REMOVAL

To remove the Front Panel L.E.D. Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove the L.E.D. Assembly by pressing the center of the Front Panel L.E.D. Assembly with a blunt tool.

   NOTE
   Press from the inside to the outside of the panel.

3. Remove the square retainer from the assembly.

REPLACEMENT

To replace this assembly, reverse Steps 1 through 3.

LINEAR BRAKE ASSEMBLY

REMOVAL

To remove the Linear Brake Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove Connector J11 from the Spindle Control circuit board.
3. Remove the 5/16-inch nut and washer from the mounting stud.
4. Remove the Linear Brake Assembly.

REPLACEMENT

To replace the assembly, reverse Steps 1 through 4.

ADJUSTMENT

To adjust the Linear Brake Assembly:

1. Loosen the 5/16-inch mounting nut.
2. Set the feeler gauge, adjusted to 0.014 inches, between the brake pad and the spindle drive motor rotor.
3. Push the brake pad up against the feeler gauge.
4. Align the brake shoe with the Spindle Drive Motor rotor.
5. Tighten the 5/16-inch mounting nut.
6. Remove the feeler gauge.

INDEX ASSEMBLY

REMOVAL

To remove the Index Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Loosen the lock nut on the Index Assembly bracket.
3. Unscrew the Index Assembly, and remove.

REPLACEMENT

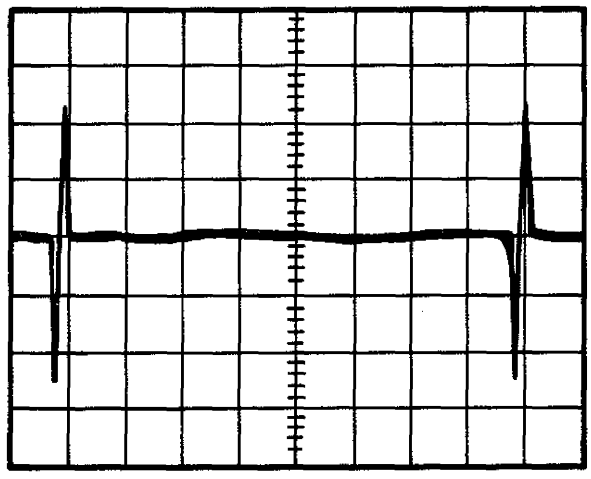
To replace the Index Assembly, reverse Steps 1 through 3.

ADJUSTMENT

To adjust the Index Assembly:

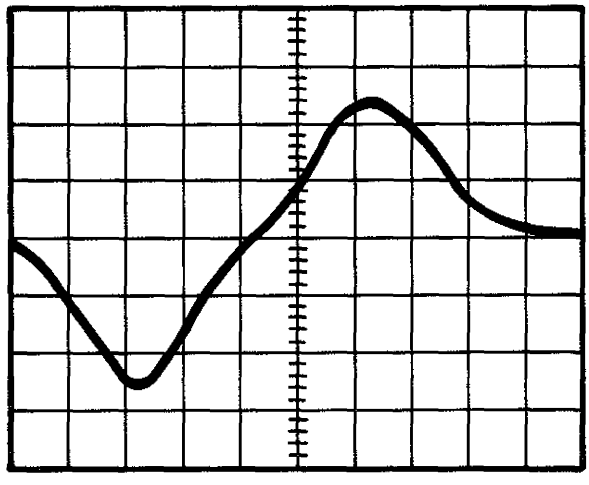
1. Loosen the 3/8-inch locking nut.
2. Adjust the Index Assembly to between 0.008 and 0.010 inches from the motor rotor.
3. Use a 100 megahertz or greater bandwidth oscilloscope.
4. Verify the A. C. signal as seen at U9, Pin 6, is greater than one volt peak to peak (see Figure 4-4).
5. There must not be more than 100 millivolts peak ripple on the base line.

VOLTAGE SCALE
1 VOLT PER DIVISION



TIME SCALE: 2 MILLISECONDS PER DIVISION
LOCATION U9-6

VOLTAGE SCALE
1 VOLT PER DIVISION



TIME SCALE: 50 MICROSECONDS PER DIVISION
LOCATION U9-6

FIGURE 4-4
INDEX SENSOR

FRONT PANEL

REMOVAL

To remove the front panel:

1. Wedge a taper shim 0.030 inch under the edge of the front panel.
2. Remove the front panel from the drive frame.
3. Clean the front panel thoroughly with solvent.

REPLACEMENT

To replace the front panel, apply new double back tape, and fit the panel over the drive frame.

SPINDLE CONTROL CIRCUIT BOARD ASSEMBLY

REMOVAL

To remove the Spindle Control Circuit Board Assembly:

1. Remove the Control and Data Circuit Board Assembly.
2. Remove Connectors J10 and J11 from the Spindle Control circuit board.
3. Remove the three screws that attach the board to the chassis.
4. Lift the board straight up and out.

REPLACEMENT

To replace the board, reverse Steps 2 through 4. When replacing connectors, ensure the proper pin orientation.

ADJUSTMENT

To adjust the Spindle Control circuit board:

1. Set potentiometer R23 (closest to interface connectors, single turn) to its approximate center position.
2. Using a dual channel oscilloscope, connect one channel to R26 (resistor lead closest to the power transistor leads on Spindle Control Circuit Board), and set scope to 100 millivolts per division. Connect the other channel of the scope to test point three on the logic board (index), and set the voltage scale at one volt per division and the time base at two milliseconds per division.
3. Apply power to the drive and wait 15 seconds for the spindle motor to come up to speed.
4. While the scope is triggered on index, adjust the speed control potentiometer R5 on the spindle control board (10 turn pot closest to the front of the drive), so the time between index pulses is between 16 and 17 milliseconds.
5. Trigger the scope to the line frequency (60 Hertz). Adjust R5 so index pulses are stationary on the scope screen.
6. Adjust R23 so voltage spikes, both positive and negative going, across R26 are minimal (see Figure 4-5).
7. Repeat Steps 5 and 6 until no further improvement can be made.

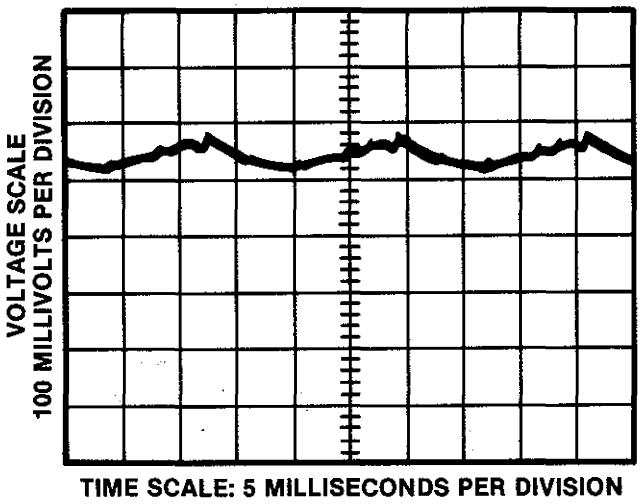


FIGURE 4-5
VOLTAGE SPIKES

FRAME ASSEMBLY

REMOVAL

To remove the Frame Assembly:

1. Remove the Control and Data circuit board.
2. Remove the Spindle Control circuit board.
3. Remove the three frame nuts and the six washers.
4. Remove the Frame Assembly.

REPLACEMENT

To replace the Frame Assembly, reverse Steps 1 through 4 above.

TRACK 0 SENSOR ASSEMBLY

Do not move the positioning mechanism or Track 0 stop.

REMOVAL

To remove the Track 0 Sensor Assembly:

1. Remove the Circuit Board Assembly.
2. Loosen the screw on the Track 0 Sensor Assembly mount.
3. Swing the mount clear, and remove the screw that holds the Track 0 Sensor Assembly.

REPLACEMENT

To replace the Track 0 Sensor Assembly, reverse Steps 1 through 3 above.

ADJUSTMENT

To adjust the Track 0 Sensor Assembly:

1. Loosen the screw.
2. Adjust the sensor so that it is 2.5 $\pm$1 volt at Test Point 5, while stepping out from Track 5 to Track 0, and the positioner is on Track 2 plus or minus one track.
3. Verify that Test Point 6 changes logic level at Track 2, plus or minus one track (see Figure 4-6).

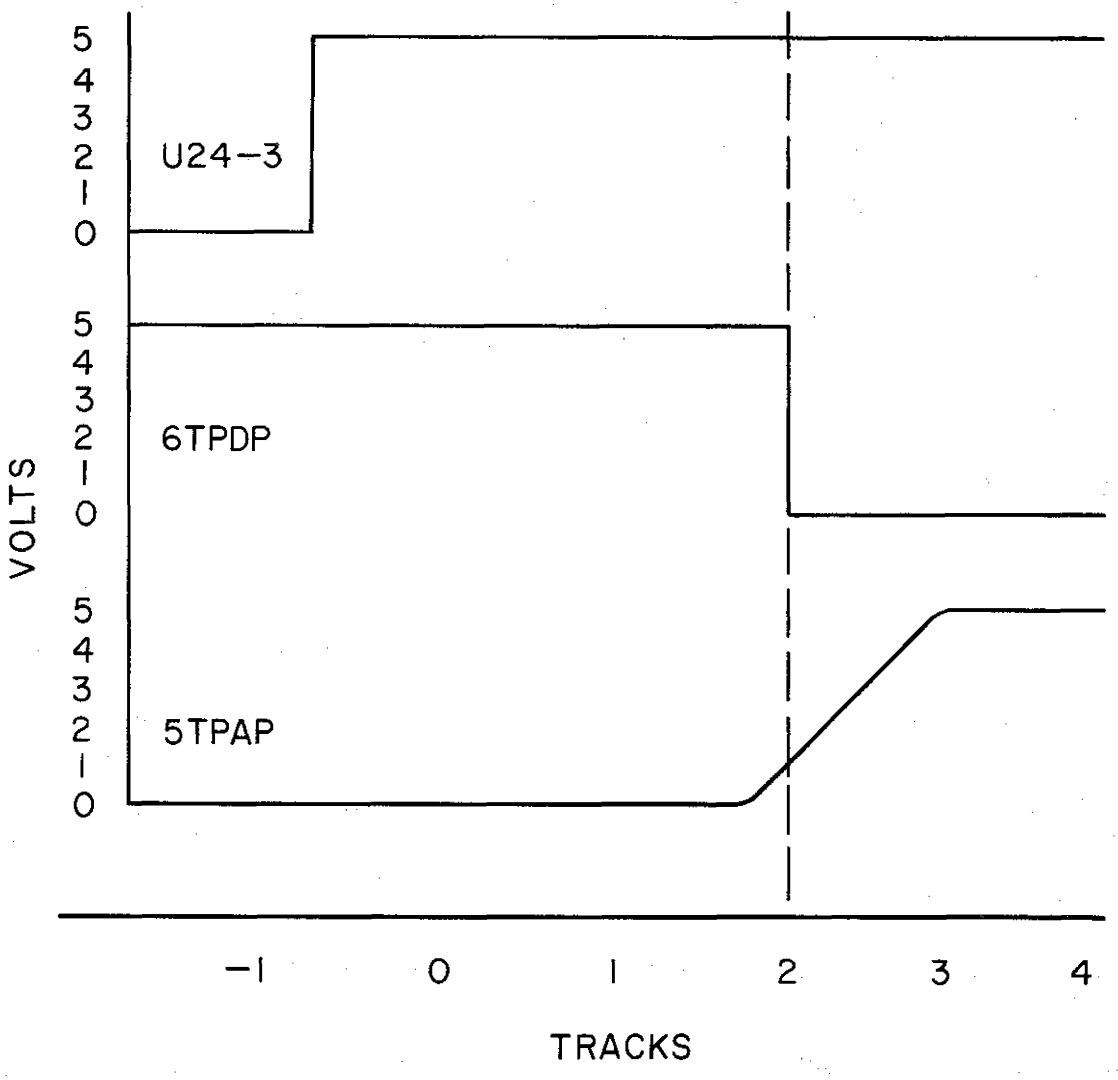


FIGURE 4-6
TRACK 0 ADJUSTMENT

APPENDIX A

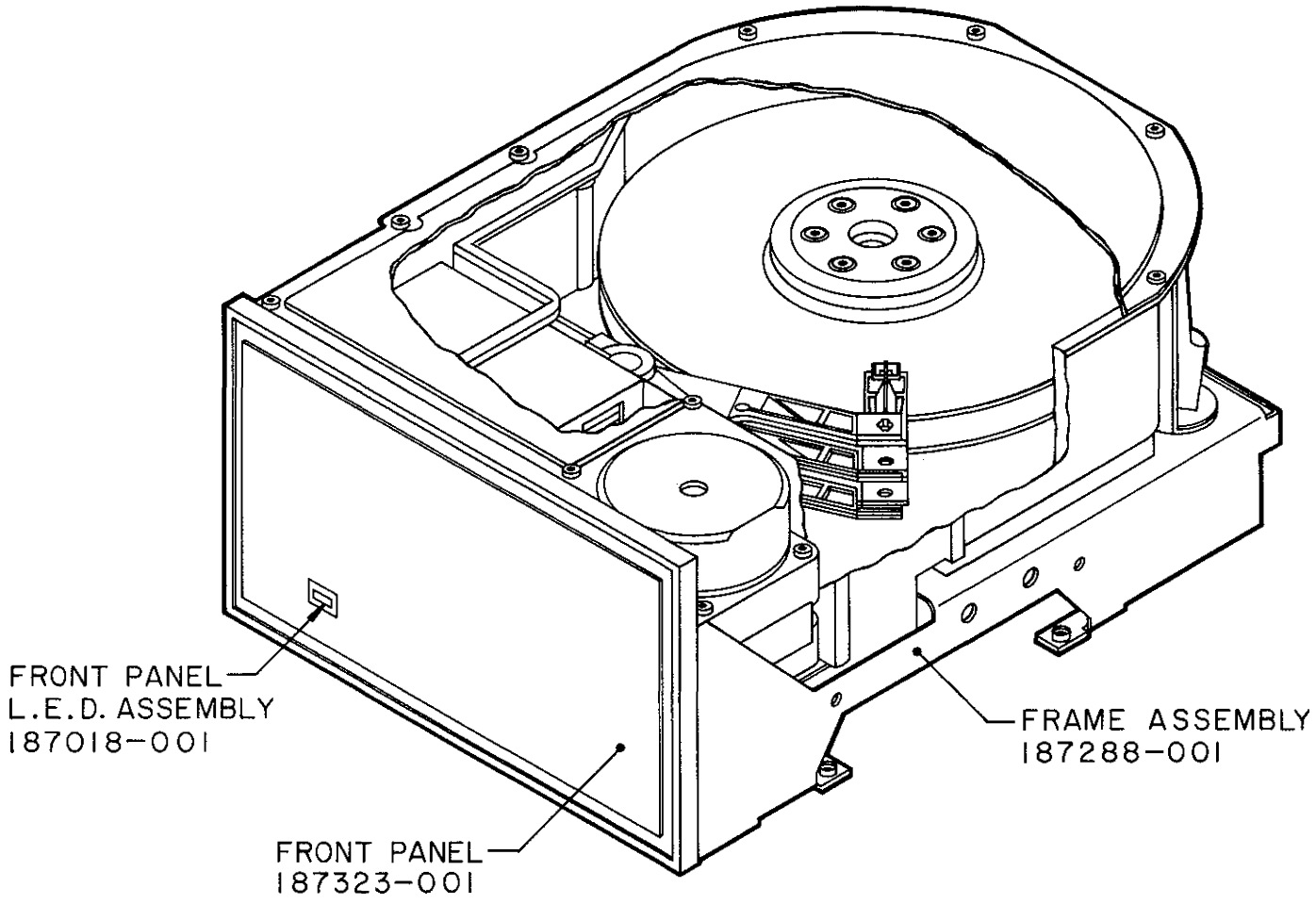
RECOMMENDED SPARE PARTS LIST AND MAJOR ASSEMBLIES

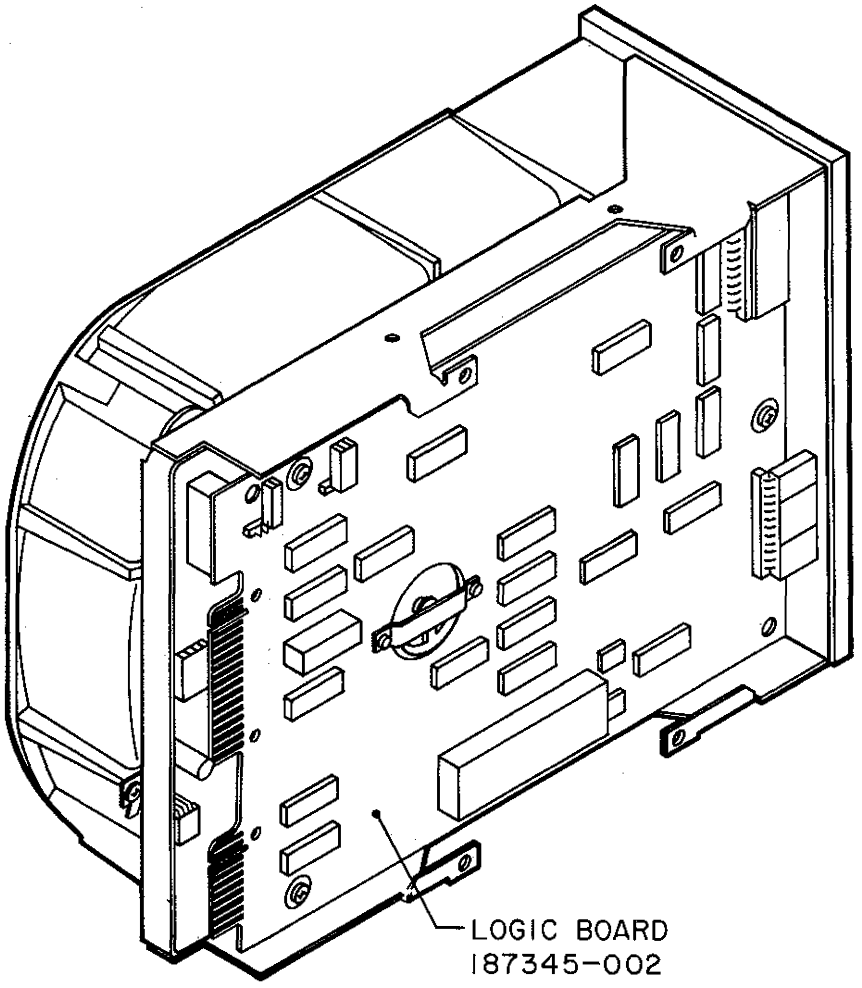
All assemblies with part numbers are available for purchase as spare replacement parts. The items without alpha designators on the drawings are for reference only, and cannot be purchased as spare replacement parts.

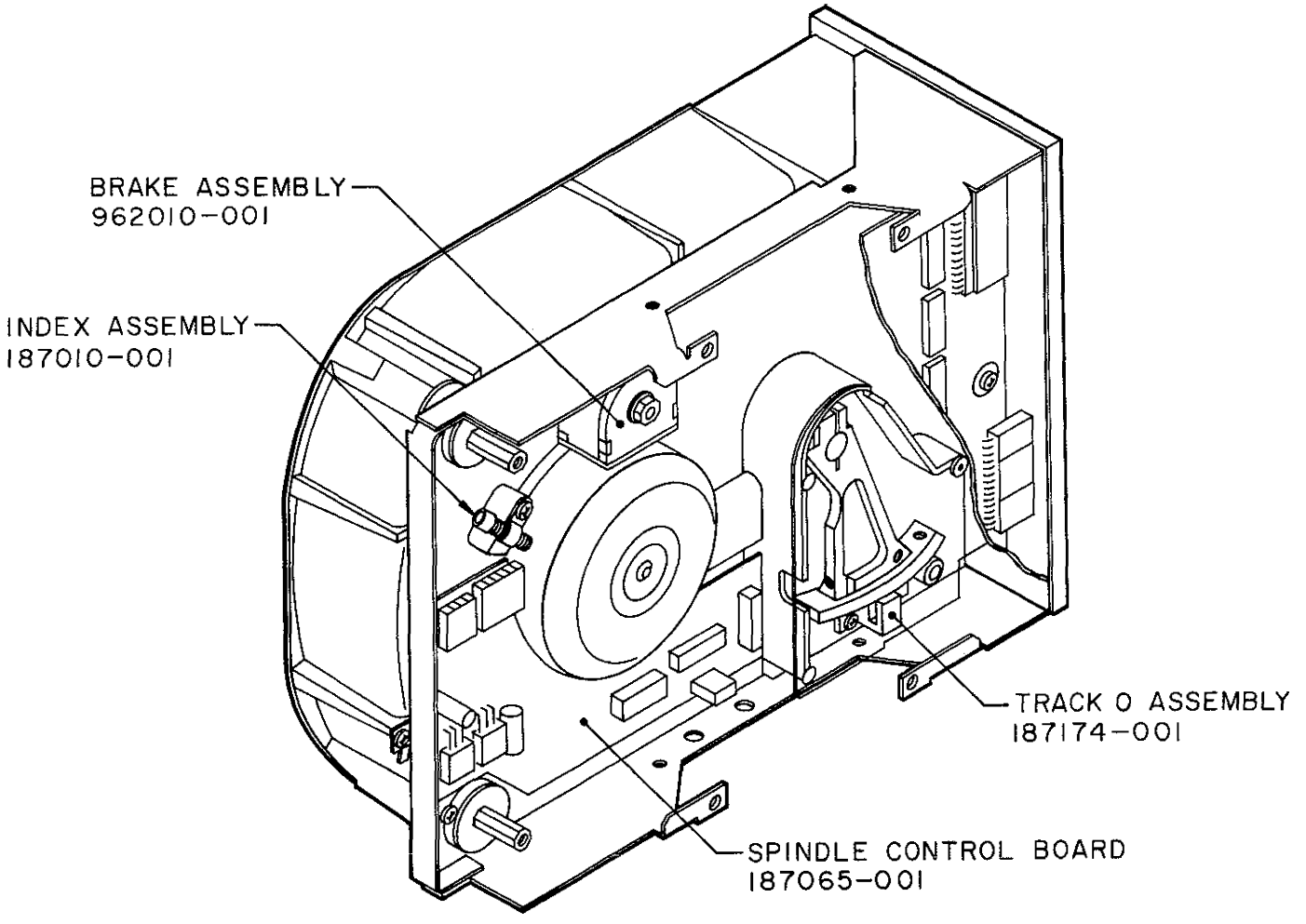
If an assembly has been determined faulty, and is not listed as a spare replacement, the drive must be returned to the manufacturer for repair.

RECOMMENDED SPARE PARTS LIST

Description	Part Number
Brake Assembly	962010-001
Index Assembly	187010-001
Track 0 Assembly	187174-001
Frame Assembly	187288-001
Front Panel	187323-001
Spindle Control Board	187065-001
Logic Board	187345-002
Front Panel L.E.D. Assembly	187018-001
Single Pack Shipping Container	187125-001 (Not Shown)
Four Pack Shipping Container	187125-002 (Not Shown)


FRONT PANEL
L.E.D. ASSEMBLY
187018-001
FRONT PANEL
187323-001
FRAME ASSEMBLY
187288-001

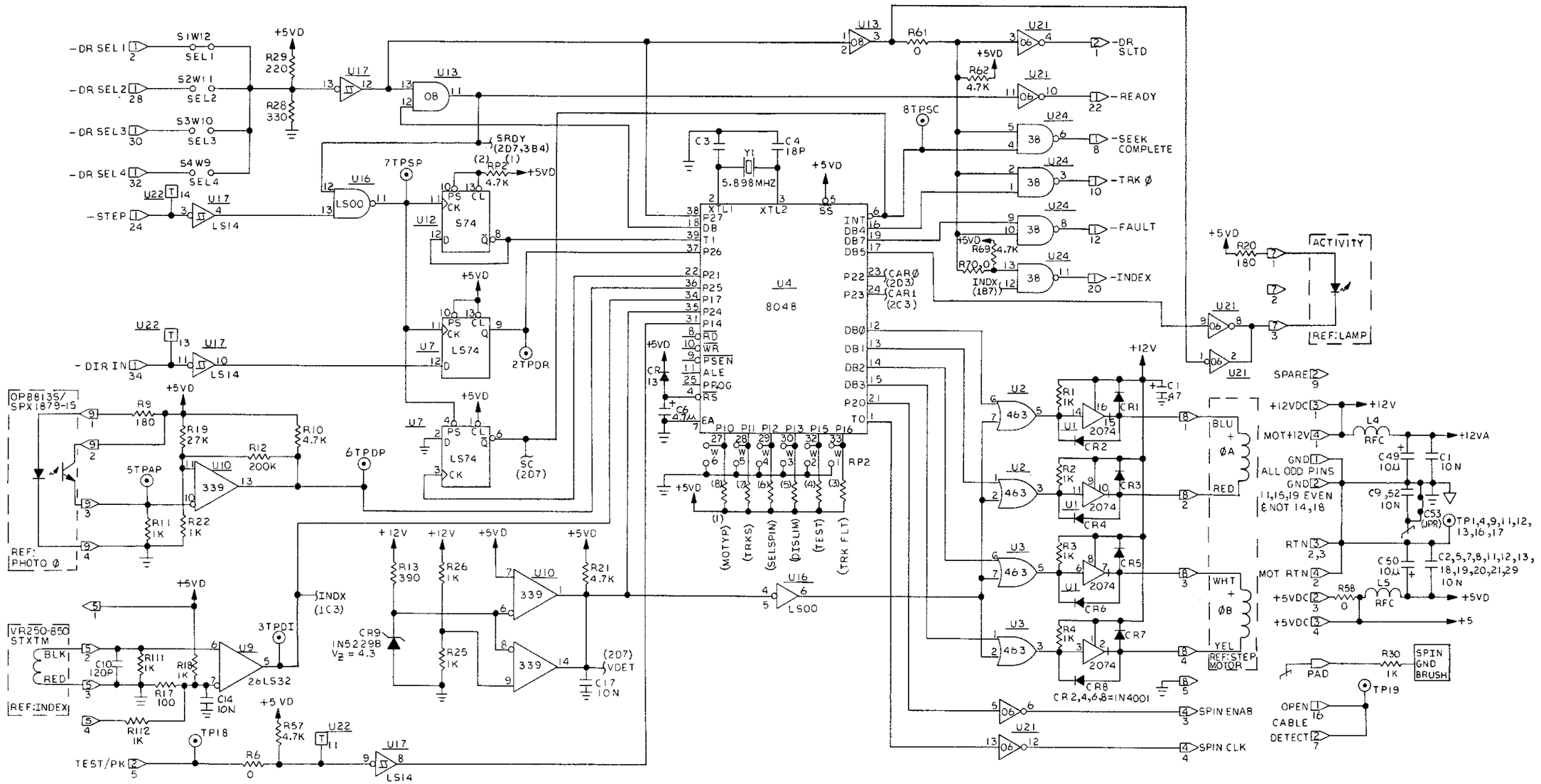

LOGIC BOARD
187345-002


BRAKE ASSEMBLY
962010-001
INDEX ASSEMBLY
187010-001
TRACK 0 ASSEMBLY
187174-001
SPINDLE CONTROL BOARD
187065-001

APPENDIX B

CIRCUIT BOARD SCHEMATICS AND ASSEMBLY DRAWINGS

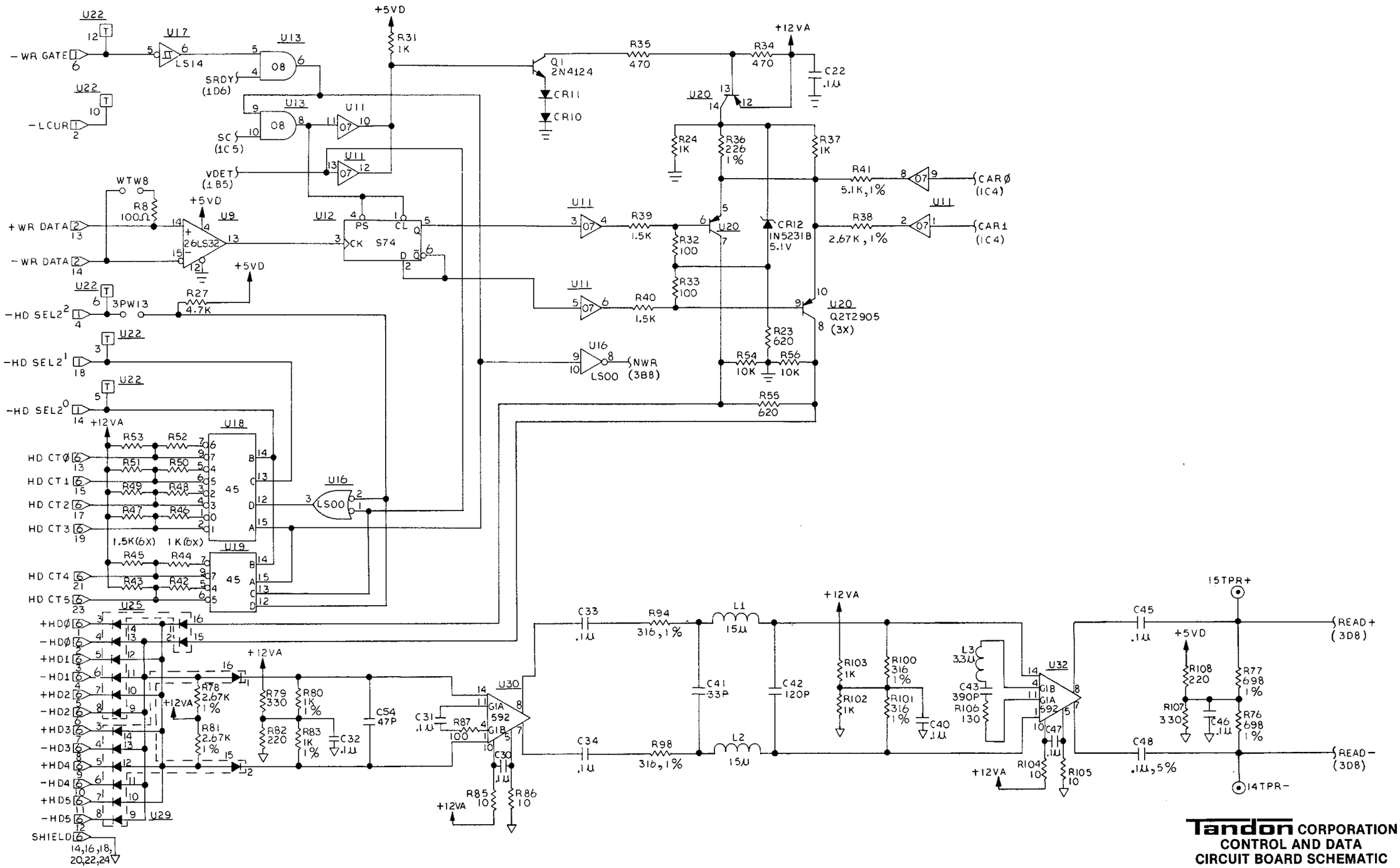
This appendix contains the current circuit board schematics and assembly drawings for the TM500 series of disk drives.



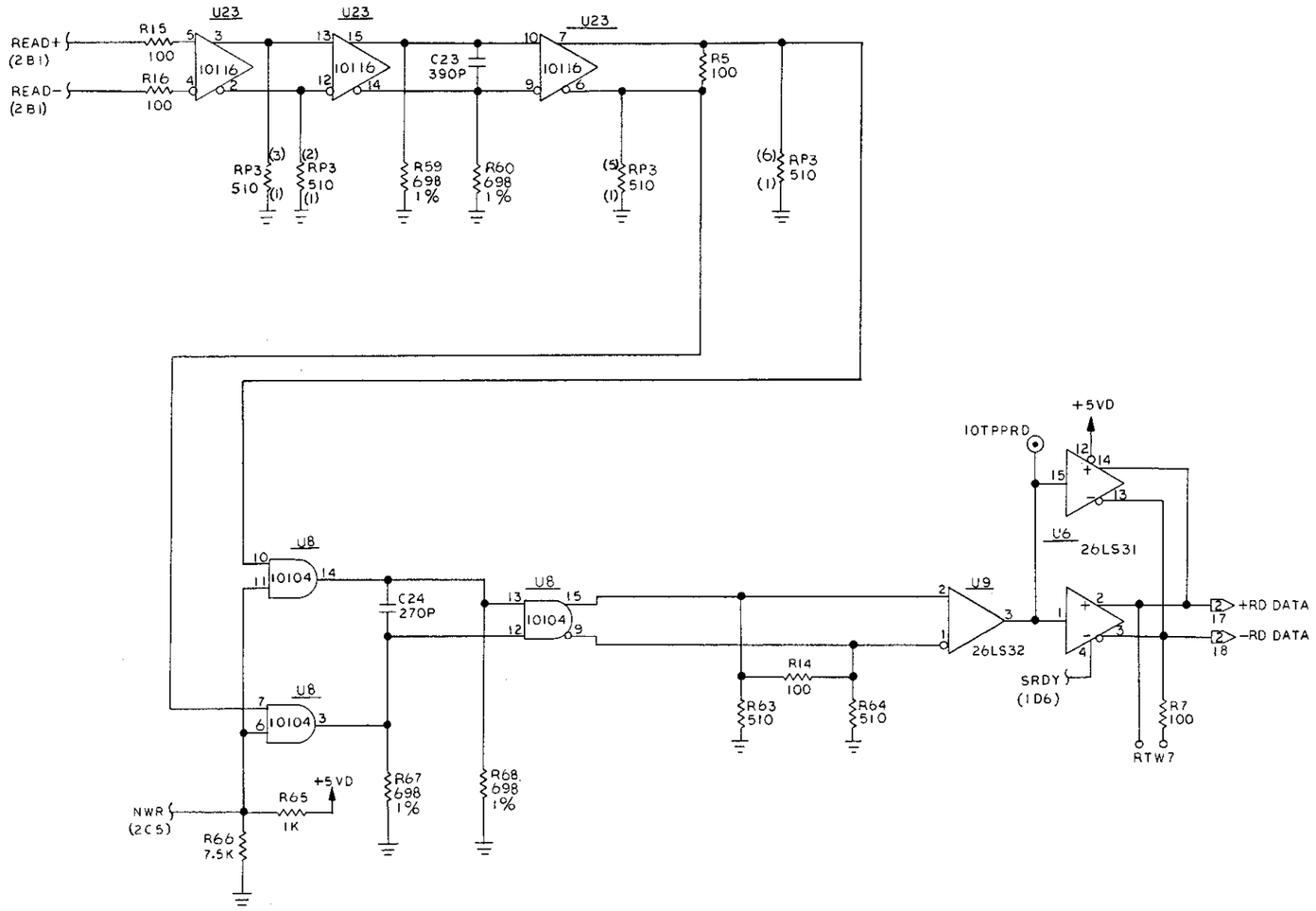
6. [X] Y DENOTES CONNECTOR JX, PIN Y.
5. INDUCTORS ARE IN µH, 10%.
4. DIODES ARE IN4446 OR EQUIV.
3. CAPS ARE IN PF, NF, OR µF, 25V MIN. TOLERANCE IS 10% FOR VALUES ABOVE 1N, 5% OTHERWISE.
2. 1% RESISTORS ARE 1/8 W.
1. RESISTORS ARE IN OHMS, 1/4 W 5%.

9. UNVALUED COMPONENTS ARE OMITTED.
8. [T] X DENOTES PIN X OF (U22) TERM PAK. = 220 330 X
7. DENOTES TEST POINT.

Tandon CORPORATION
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 1 OF 3



Tandon CORPORATION
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 2 OF 3

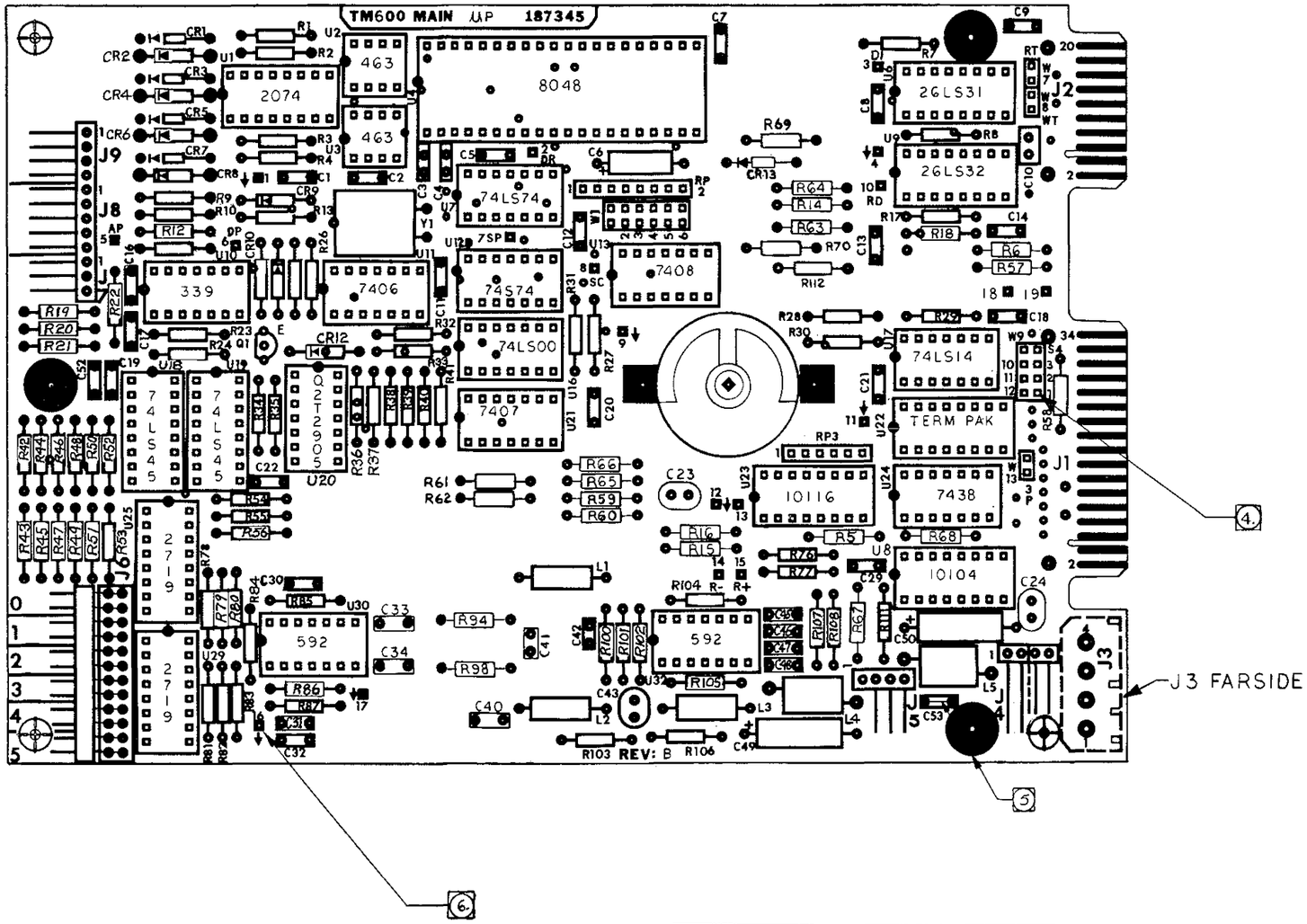


I.C. LOCATION AND VOLTAGE CHART					
LOCATION	TYPE	+5	+12	GND	UNUSED
U16	74LS00	14		7	
U21	7406	14		7	
U11	7407	14		7	
U13	7408	14		7	
U17	74LS14	14		7	1/6
U24	7438	14		7	
U18,U19	74.15	16		8	
U7	74LS74	14		7	
U12	7474	14		7	
U10	339		3	12	1/4
U2,U3	463	8		4	
U30,U32	592		NOTED	NOTED	
U1	UNL2074		NOTED	4,5,12,13	
U6	26LS31	16		8	2/4
U9	26LS32	16		8	1/4
U25,U29	2719				
U20	Q2T2905		NOTED		1/4
U4	8048	26,40		20	
U8	10104	1,16		8	1/4
U23	10116	1,16		8	
U14					
U22	TERM PAK	16		7,8	4/12

SHUNT PLUG PROGRAMMING			
W1-W13 SHUNT	FUNCTION	FACTORY PROGRAMMED	USAGE
W1	TRK FAULT	O	INSTALL FOR EXCESS TRK FAULT
W2	TEST	O	INSTALL FOR FACTORY TEST
W3	DISABLE LIMIT	O	INSTALL TO DISABLE SOFT LIMITS
W4	SPIN SELECT	O	INSTALL FOR SPIN SELECT
W5	TRACKS	S	INSTALL FOR S VERSION ONLY
W6	MOTOR TYPE	–	INSTALL FOR TYPE 18 MOTOR
RTW7	READ TERMINATOR	I	CLOSE ONLY @ END DRIVE OF DAISY CHAIN DATA
WTW8	WRITE TERMINATOR	I	CLOSED FOR RADIAL DATA
S4W9	DRIVE SELECT 4	O	INSTALL 1 OF 4 PLUGS ONLY
S3W10	DRIVE SELECT 3	O	PLUG CORRESPONDS TO
S2W11	DRIVE SELECT 2	O	DRIVE ADDRESS
S1W12	DRIVE SELECT 1	I	
3PW13	3 DISC	603	CLOSE FOR MODEL 603 ONLY
U22	TERMINATOR PAK	I	INSTALL IN END DRIVE OF DAISY CHAIN
O = OMIT I = INSTALL		S = CLOSE FOR S VERSION ONLY 603 = CLOSE FOR TM603 ONLY	

REFERENCE DESIGNATORS	
LAST USED	UNUSED
C54	C15,25-28,35-39,44,51
CR13	
J9	
L5	
Q1	
R111	R71 THRU 75,84,88-93,95-97,99,109,110
RP3	RP1
TP19	
U32	U5,14,15,26-28,31
W13	
Y1	

Tandon CORPORATION
CONTROL AND DATA
CIRCUIT BOARD SCHEMATIC
187340-001 REV L
SHEET 3 OF 3



6. T.P. WIRE TO EXTEND .25 MIN, .30 MAX ABOVE COMPONENT SIDE OF P.C. BOARD 19 PLACES.

5. SOLDER #24AWG UNINSULATED TIN COATED SOLID COPPER WIRE MAY SUBSTITUTE 1/4W RESISTOR LEAD WIRE.

4. .025 SQ. SHUNT JUMPER POSTS (W1-W13) TO BE INSTALLED ⊥ TO BOARD SURFACE WITH FLATS TO BE || TO BOARD EDGES, 26 PLACES.

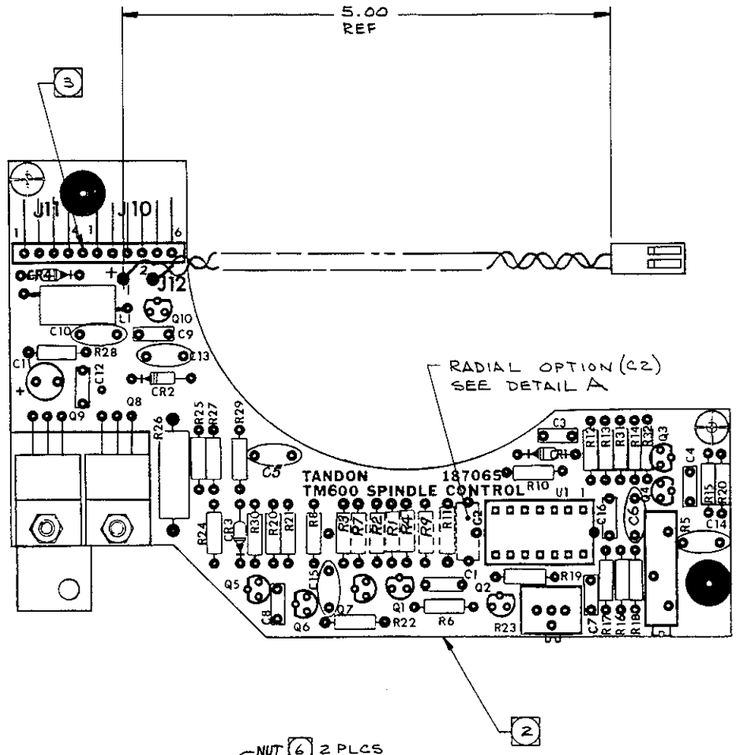
3. SOLDER #24 AWG UNINSULATED TIN COATED SOLID COPPER WIRE MAY SUBSTITUTE 1/4 W RESISTOR LEAD WIRE.

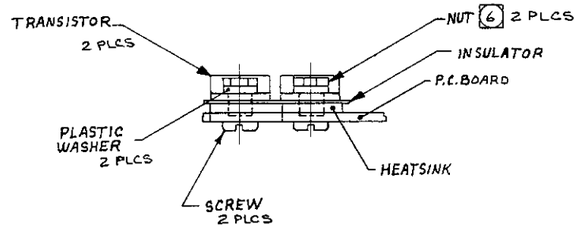
2. REF. DOCUMENT: 187340-001-CIRCUIT SCHEMATIC
187341-001 ARTWORK

1. SEE SHEET 1 THRU 3 FOR PART LIST.

REFERENCE DESIGNATORS	
LAST USED	UNUSED
C53	C15,25-28,35-39,44,51
CR13	
J9	
L5	
Q1	
R111	R71 THRU 75,88,93,95-97,99,109,110
RP3	RP1
TP19	
U32	U5,14,15,26-28,31
W13	
Y1	

Tandon CORPORATION
CONTROL AND DATA
CIRCUIT BOARD ASSEMBLY
187345-001 REV S
SHEET 1 OF 1





7. REF DOCUMENT: 187060-001 CIRCUIT SCHEMATIC
   187061-001 ARTWORK

[6] TORQUE 4 5 INCH LBS NOMINAL.

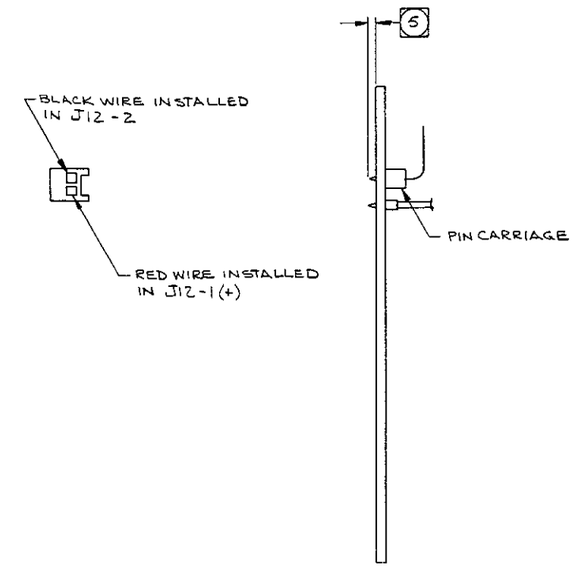
[5] MAX LENGTH OF COMPONT LEADS BELOW SOLDER SIDE BOARD AFTER ASSEMBLY & TRIMMING SHALL NOT EXCEED .08 INCH.

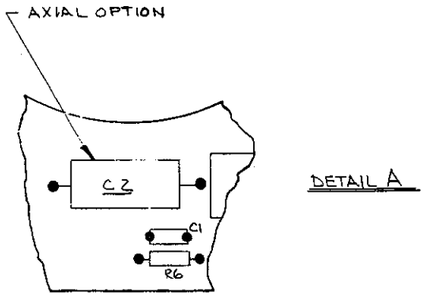
4. COMPONENT HEIGHT EXCEPT C11, SHALL NOT EXCEED .45 INCH ABOVE BOARD. CAPACITOR C11, NOT TO EXCEED .50 INCH ABOVE BOARD.

[3] CUT PIN TANGENT TO PIN CARRIAGE.

[2] THIS ASSEMBLY SHALL BE MADE FROM P.C.B. DETAIL 187060-001.

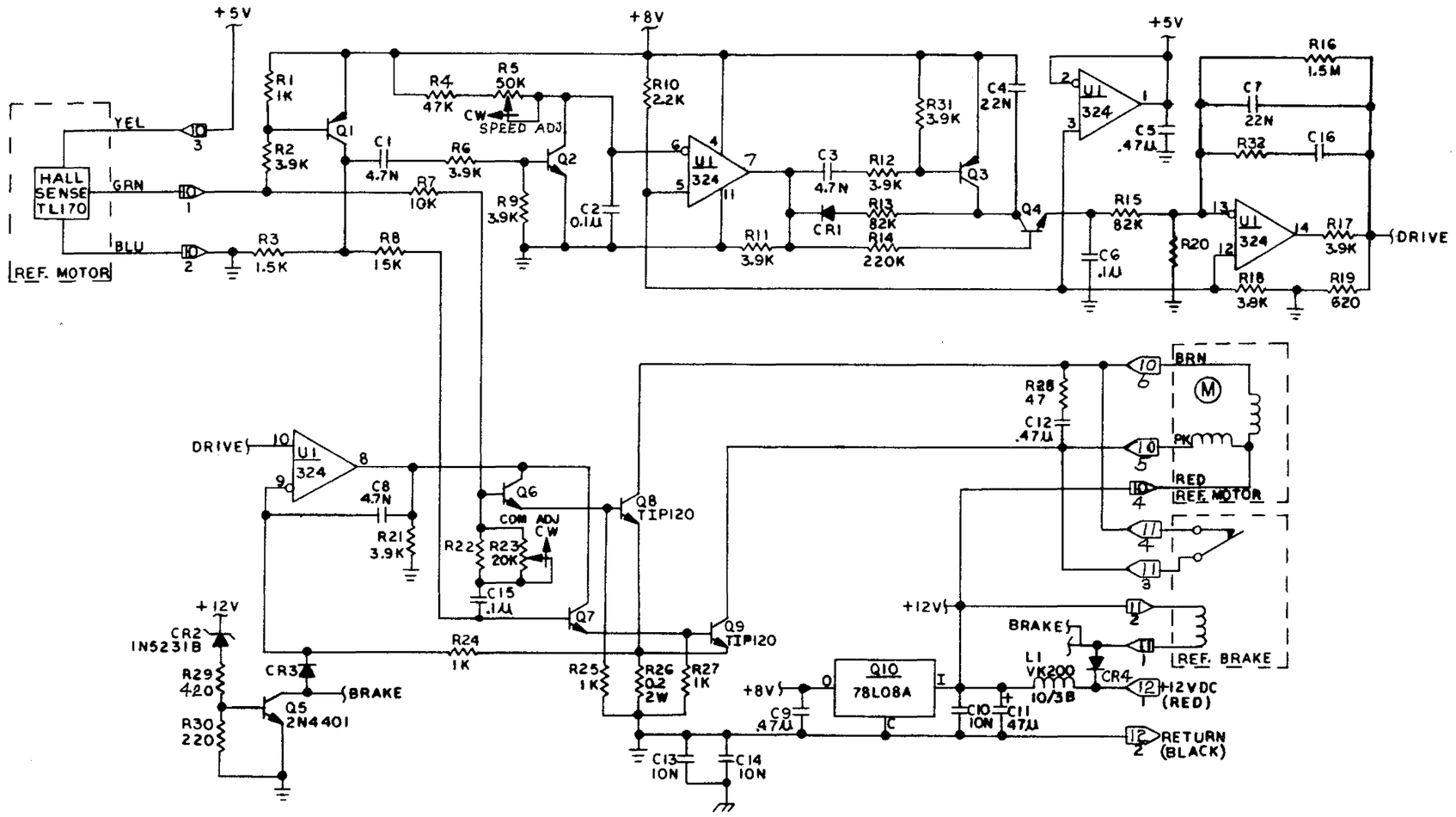
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.





DETAIL A

Tandon CORPORATION
SPINDLE CONTROL
CIRCUIT BOARD ASSEMBLY
187065-001 REV J
SHEET 1 OF 1



7. UNVALUED COMPONENTS ARE OMITTED.
   ⊠ ⊲
6. Y OR Y DENOTES CONNECTOR X, PIN Y.
5. PNP TRANSISTORS ARE 2N4125.
4. NPN TRANSISTORS ARE 2N4124.
3. DIODES ARE 1N4446 OR EQUIV.
2. CAPACITORS ARE 25V, 10%, PF, NF, OR UF.
1. RESISTORS ARE IN OHMS, 1/4 W, 5%.

Tandon CORPORATION
SPINDLE CONTROL
CIRCUIT BOARD SCHEMATIC
187060-001 REV E
SHEET 1 OF 1

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

AUSTRALIA	BELGIUM	U. K.
91 KURRAJONG AVENUE MOUNT DRUITT, N.S.W. 2770	PARC INDUSTRIEL 5140 NANINNE (NAMUR)	BILSTON ROAD WEDNESBURY WEST MIDLANDS WS10 7JN

MS 2606021-185

Printed in U.S.A.