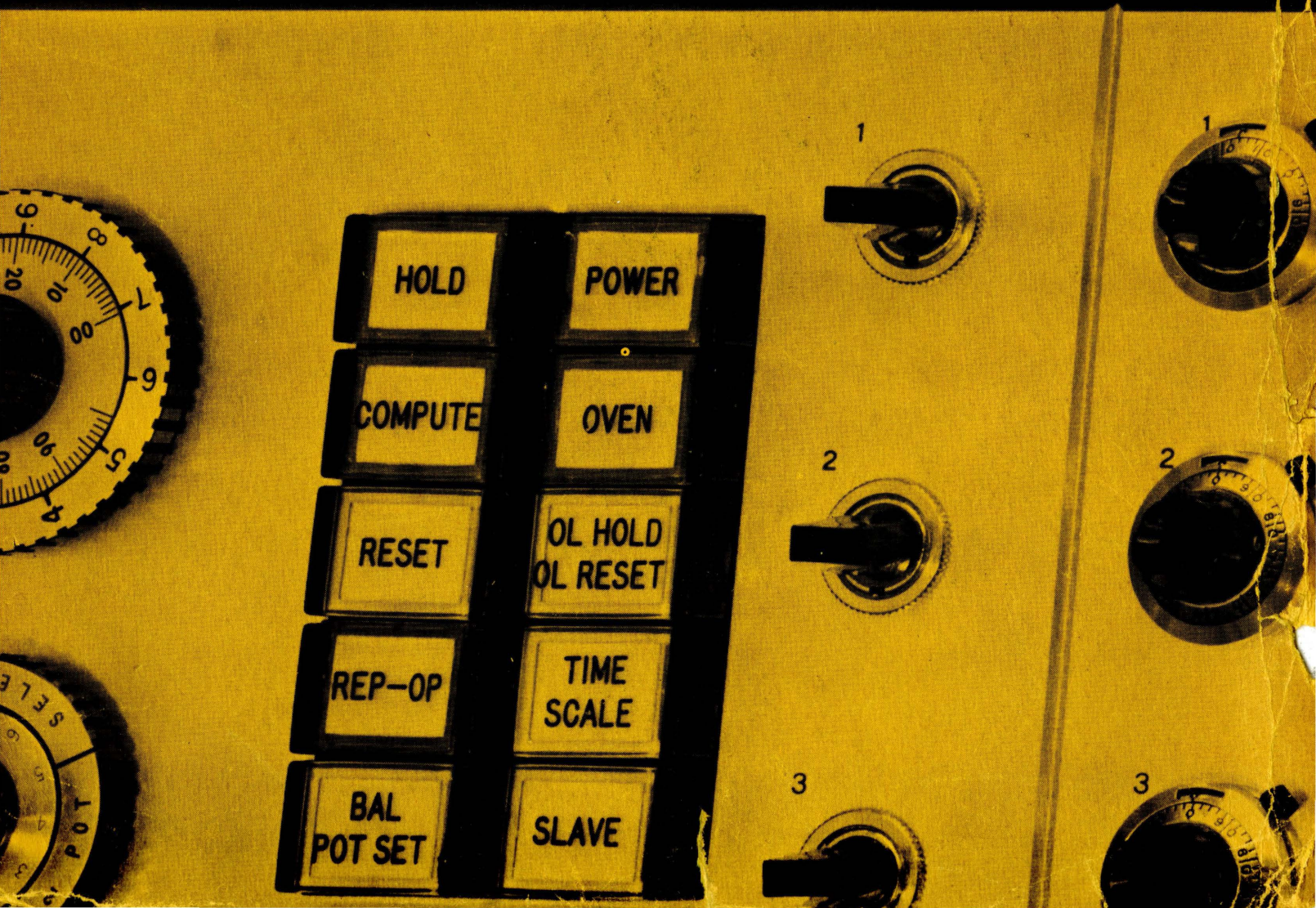
SYSTRON DONNER CORPORATION

SD 40/80

MAINTENANCE MANUAL

Instruction Manual

ELECTRONIC AND INERTIAL INSTRUMENTATION FOR MEASUREMENT, SIMULATION, CONTRCL



INTRODUCTION

The SD 40/80 computer has been designed to give trouble-free performance with a minimum of calibrating and maintenance. Although the following chapters are not intended as a comprehensive guide, they should be sufficient for most routine maintenance and calibration. Many of the procedures included in the manual are not intended for normal use, but for use as references or as special checks.

UNIT IDENTIFICATION

The top view of the Model SD 40/80 as shown below, identifies the five major sections of the computer. These sections are designated A1 through A5, and are divided into subsections as outlined in Table 1. This identification code will enable one to quickly locate and trace the circuits used in the SD 40/80. An example of the use of the code is:

> A1-3-S319-9C (Arm) indicating that the signal goes to sections A1-3 (Address System) and in that section is connected to the arm of section 9C on S319.
>
> A3-4-34A indicating that the signal goes to section A3-4 (Control Center Logic Distribution) and is connected to point 34A in that section.

Schematic number 15062 gives a more detailed breakdown of the individual sections. Note that sections A3-2, A3-3A, A3-3B, and A3-4 consist of connectors with shorting plugs installed and are used to distribute power supply voltage and control logic.

This manual follows the numeral sequence of the identification code. It is arranged with the description and calibration procedures in the first section in their code order. The schematic drawings which follow, are again arranged in their code order.

Section	Sub-Section	Function	Schematic
A1	-1	Function Generators	14259
	-2	DVM Readout	--
	-3	Address System	14920
	-4	Meter, Pots, Ref Pot	14921
	-5	Logic Control	12286
A2	--	DVM Electronics	--
A3	-1	Ground Buss	
	-2	Pot Logic Distribution	
	-3A	P.S. Voltage Distribution	
	-3B	±112v Distribution	
	-4	Logic Control Distribution	
	-5	Module 1-7 Connector	
	-6	Module 8-14 Connectors	
	-7	Module 15-21 Connector	
	-8	Trunk Lines (1-75)	
	-9	Module 22-28 Connectors	
	-10	Module 29-35 Connectors	
	-11	Module 36-42 Connectors	
	-12	Trunk Lines (76-169)	
A4	-1 to 6	Pot Panels	12925
A5	-1	±100v Ref. Supply	12549
	-2	±112v Supply	12709
	-3	±28v Supply	11877
	-4	+28v Relay Supply	12700
	-5	AC Supply	12859 (Block Diagram)

(See Schematic 15062 for Pictorial View.)

TABLE 1.

FUNCTION GENERATORS (A1-1)

The model SD 40/80 has provisions for fifteen diode function generators (Model 3351). The input junction and output terminals for each function generator are connected to the terminals provided for them on either a summer (3321) or inverter (3322) module. The function generators are numbered from left to right, 1 through 15. They are connected to the patchboard in the following manner: Number 1 function generator will be connected to the first inverter or summer available in the upper left-hand section of the patchboard (section A3-5), each successive function generator will be connected to the next available summer or inverter. The Table below shows the typical wiring connections.

Signal	M3351 (F.G.)	Module Rec'pt (A3-5, 6, 7, 9, 10, 11)	Patchboard
Input	A1-1-J3E	A3-5-J6-29	Module #6 B-8
Junct #1	A1-1-J3-A	A3-5-J6-32	Module #6 C-8
Out #1	A1-1-J3F	A3-5-J6-31	Module #6 D-8
Junct #2	A1-1-J3-B	A3-5-J6-34	Module #6 E-8
Out #1	A1-1-J3-4	A3-5-J6-33	Module #6 F-8

TABLE 2. FUNCTION GENERATOR WIRING (Typical).
Shown for F.G. #3 connected to Module #6
(AMPS 11 & 12)

DVM READOUT (A1-2)

Section A1-2 contains the readout section of the optional Digital Voltmeter. If the digital voltmeter is not purchased, the section consists of a blank panel. If the digital voltmeter is included, or if a digital voltmeter is purchased after initial receipt of the SD 40/80, the blank panel is removed and the readout section of the DVM is installed. The DVM readout consists of 4-digit indicators: one 0-1 indicator, one "+" or "-" indicator, and one decimal indicator.

Connection to the DVM electronics, located in section A-2, is made through a cable. For a more complete description of this section, refer to the supplement on the DVM.

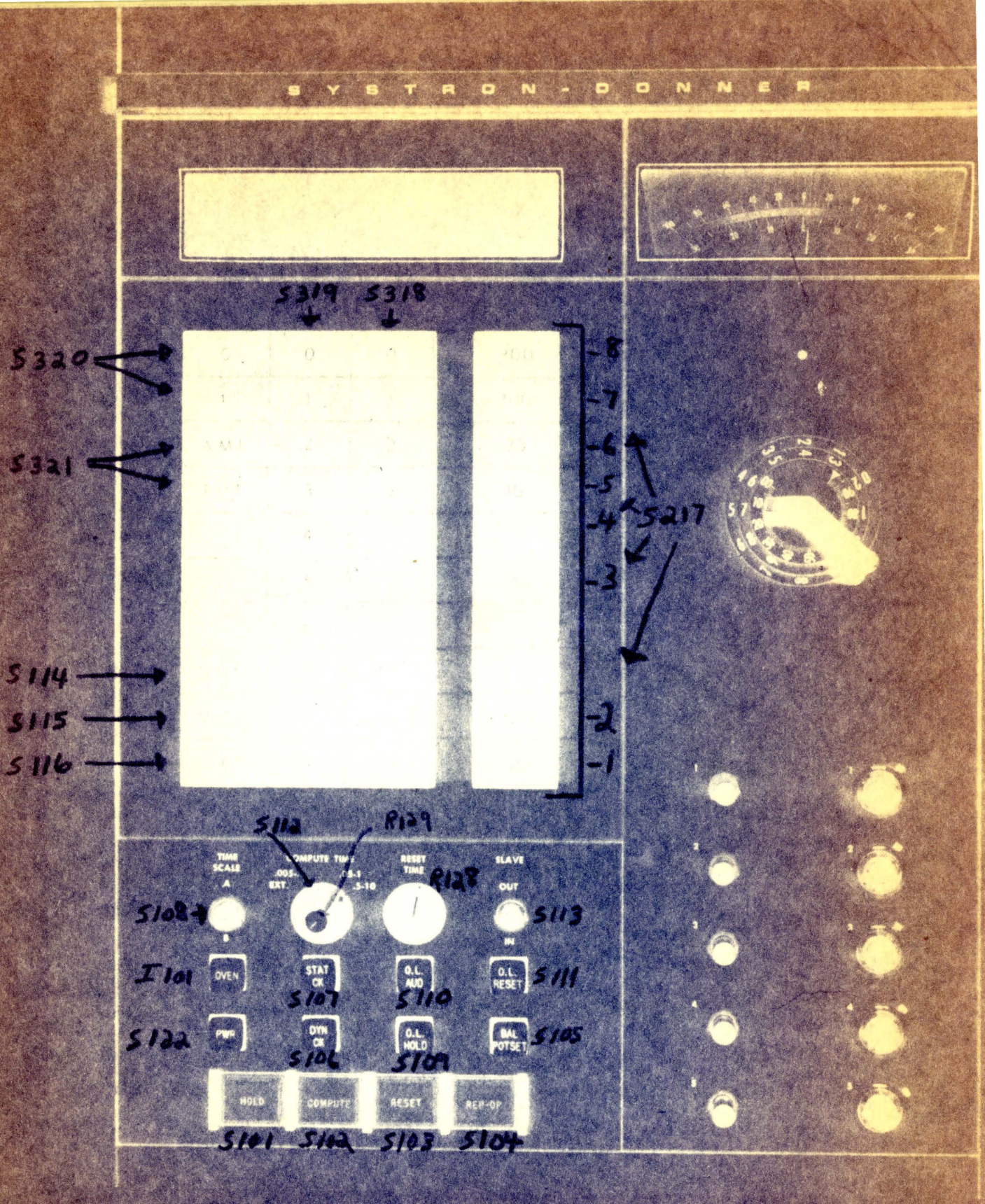
ADDRESS SYSTEM (A1-3)

The Address System contains a logic matrix and switching system that enables the operator to monitor the output of any potentiometer or amplifier in the computer. Figure 1 shows a front view of the address system with the switches identified by number. The routing of a typical potentiometer and amplifier from their outputs to the meter circuitry is shown in Figure 2. The logic is straight forward and is similiar to that shown for any amplifier or potentiometer.

Note that amplifier and potentiometer addresses are 3-digit numbers, (i.e. Pot 017 or Amp 021); therefore, the "0" or "1" hundreds switch must be depressed to select any address.

Included in the address section are the meter select and meter range switches. The DVM (S114), METER (S115), and EXT (S116) switches, when depressed, apply the selected address to the meter circuit. The meter select switches are mechanically interlocked to prevent more than one switch at a time from being depressed. The meter select switches also control the DVM and "meter" inputs on the problem board. These inputs, located on module 7 E-1(D) and F-1(M) are connected to the meter whenever one of the meter select switches is depressed. The switching logic is such that no meter will have inputs from the address selector and the problem board simultaneously. The address system has priority and thus when the Meter switch is depressed, the meter input from the problem board is disconnected. With the EXT switch depressed, both DVM and meter inputs from the problem board are connected.

The meter range switch (S-217) provides six DC ranges and "+", "-" null ranges. Accuracy of the DC ranges is approximately 2% of full scale. The "+", "-" null range provides ±.01% accuracy of its full scale range of ±100v. Note that meter ground is provided through the normally closed contacts of the "+", "-" null section of S217. Refer to schematic 14921 for a detailed schematic of the meter select switches and the meter circuitry.



Address System, Front View

Figure 1

METER, REFERENCE POTENTIOMETER, FUNCTION SWITCHES, and COEFFICIENT POTENTIOMETERS 1 through 5 (A1-4)

The meter movement located in section A1-4 is of the moving coil type. The movement requires 10 μa (10-0-10 μa) for full scale deflection and has a resistance of 4K ohm.

The reference potentiometer (R271 on schematic 14921) is a 10K ohm decade. type potentiometer. The outer dial represents 1K ohm steps (10v when referenced to ±100v), the middle dial 100 ohm steps (1.0v), and the inner dial a 100 ohm continuous variable potentiometer calibrated with 1 ohm divisions. F206, a 10 ma fuse in series with the reference potentiometer arm, protects the circuit.

Function switches #1 through #5 are also located in section A1-4. Normally they are connected to the first five even-numbered modules (shown on schematic 14921). They may, however, be connected to any requested module at the factory. In all cases, they will be connected to pins 11A (no contact), 12B (Arm), and 9A (NC contact) of the module connector.

Potentiometers #1 through #5, located in section A1-4, are connected to the first five potentiometer connections available, these normally will be located in the first two modules. Schematic 17921 shows the circuit connections for potentiometers 1 through 5. Note that pots #2 and #5 have their bottom ends connected to J1-30 and J2-30, respectively. See section A4 (potentiometer panels) for a more detailed description of potentiometer wiring.

LOGIC CONTROL (Section A1-5

The logic control section provides the relay voltages necessary to change operating states within the computer. The Hold, Compute, and Re-set modes of operation are similar in their circuitry. Using Re-set as an example, see figure 3, the operation of these circuits is as follows: +28v is supplied to S103, the re-set switch through the normally closed contacts of the Compute and Hold switches. When S103 is pressed, it supplies +28v to the coil of K103, the Re-set relay. Ground for the relay coil is supplied through the normally closed contacts of the Pot Set/Bal relay. Once K103 is energized, it is locked up through its own contacts (6 and 7) which supply +28v. +48v from CR117 is supplied through contacts 12 and 13 and through the normally closed contacts of K104 to Q111 and 112. This positive voltage turns both transistors on, which supplies +28v to the Re-set buss to energize the Re-set relays in the modules.

Operation of the Compute and Hold circuits is the same as that of the re-set circuit. Operation of the Pot Set/Bal (K105) circuit is similar with the exception that +28v is supplied to the busses directly, rather than through a transistor stage.

The Overload Hold circuit will operate whenever an overload occurs if the O.L. Hold switch has been previously pressed. A positive signal indicating an overload condition is supplied to Q102 from the Overload buss. This signal turns on Q102 which in turn, turns Q103 off. When in the off condition, Q103 has +28v at its collector. This +28v is supplied through the closed contacts of the O.L. Hold switch to K106, the O.L. Hold relay. The now energized K106 supplies +28v through contacts 9 and 10, and through the normally closed contacts (5 and 6) of the Hold relay (K101) to Q109 and Q110, which supply +28v to the Hold relays in the modules. This same +28v from the O.L. Hold relay turns on Q115 which, through the reset relay (K-103), forward biases CR124 and CR125. This action gives the Reset and Compute drive signals, a low impedance path to ground and removes the +28v reset and compute signals from their busses, deenergizing the relays in the modules.

	Logic Control	Distribution M3-4-	Module Connection	
Dynamic Check	P102-3	-1H	PIN 42	
Balance	P103-H	-9H	PIN 44	
Forward Hold	P103-V	-17H	PIN 19	
Forward Reset	P103-U	-25H	PIN 20	
Static Check	P102-4	-33H	PIN 2	
Real Time Reset	P102-21	-41H	PIN 37	
Overload	P103-H	-2H	PIN 43	
Reverse Hold	P103-K	-10H	PIN 17	
Reverse Reset	P103-R	-18H	PIN 18	
T. S. Change	P102-5	-26H	PIN 40	
Pot Set	P103-C	-34H	PIN 10	

CONTROL LOGIC DISTRIBUTION

TABLE 3

Module Receptical (section A-3)

The Module Receptical contains the connectors for the individual modules, the busses for the Control Logic and Pot Logic, the Trunk Line Terminals, and the Main Ground Buss.

Section A3-1 is, physically, a heavy copper buss running down the center of the module receptical. (Down the left edge of the module receptical on the SD 40). All grounds are connected to this buss. Note the capacitors located at approximately the center of A3-1. These capacitors are connected from ground to plus and minus 112V; A3-1 to A3-3A-3 (+112V) and A31 to A3-3-1-15 (-112V) to provide additional filtering at the module receptical.

Section A3-2 contains the potentiometer logic buss and the buss for the +100V used in setting potentiometer coefficients. Figure 2 and ___ outline the wiring logic. Physically, section A3-2 is a connector with 44 double pin connections.

Section A3-3A and A3-3B are the distribution centers for the DC power supply voltages. Physically, they too are 44 pin connectors.

Section A3-4 is the control logic distribution center, As such it is the intermediate point between the control logic and the individual modules. Table 3 shows the wiring sequence of the various logic paths. (Reverse reset = compute.)

Each of the connectors comprising sections A3-2, 3A, 3B and 4 has a shorting plug inserted. The shorting plugs are marked with the section number to which

they belong and with the number '2'. They should be inserted with the '2' at the upper left hand corner. (caution do not mix the shorting cards.)

Section A3 also contains the Computing Modules. A discription of the Model 3310 Operational Amplifier is given next as it is the basis of each of the Computing Modules.

Model 3310 Operational Amplifier

The Model 3310 contains two identical chopper stabilized operational amplifiers. Each amplifier is capable of a ±100V output at 25 ma. Both amplifiers are contained on a simple Printed circuit card for ease of removal.

Referring to drawing number 11293 a discription of the amplifiers is as follows: Drive for the chopper transistors is provided by the multivibrator formed by Q301 and Q302. The output of this circuit is a 400 cps (approx) square wave with an amplitude of approximately 8 volts peak-to-peak.

The input is applied through R170 and is limited to approximately ±0.5V by CR108 and CR109. The input is split and the DC component of the input is fed to the chopper (Emitter Q101) stage; the AC component of the input to the wide band amplifier (Base, Q109).

The DC component is chopped to ground by the action of Q101. Q101 is turned on and off at a 400 cps rate by the output of the multivibrator and has the effect of grounding the DC signal at a 400 cps rate. The chopped DC error component is then amplified through the four stages (Q102, Q103, Q104, Q105) of the A.C. amplifier. (Note: the chopped D.C.

may be considered as a low frequency AC signal). The signal is demodulated by the action of Q106 which is driven by the output of the multivibrator. The signal which is now the amplified DC error is filtered by C110 and limited by the CR104, 105, 106, 107 combination. It is then applied to the base of Q110 in the wide band amplifier. Note that there are two feedback paths in the AC amplifier a) DC feedback from the collector of Q105 through R110 and R114 to the base of Q102, b) AC feedback from C110 through C106 to the input of the chopper.

The AC component of the input signal is applied to Q109 where it is amplified and fed to the base of Q110. At this point it is joined by the amplified DC signal and both are amplified through Q110 and Q111. The output of Q111 is applied to Q112 which is one input of a differential amplifier formed by Q112 and Q113. The other input to the differential amplifier, applied to Q113, is the output of the amplifier. The output of the differential amplifier from Q112 collector, is applied to Q118. The output stage (Q117 and Q118) is, basically, of the piggyback or cascode type and can be summarized as follows: when the signal from Q112 is in the positive direction it will tend to turn Q118 on and the voltage at the output will go in the negative direction. Simultaneously the negative going output of Q118 will tend to turn Q117 off which also causes the output to go in the negative direction. Conversely a negative going signal to Q118 will reverse the procedure and the output will swing positive. Q114 is driven by the signal from Q118 and acts as a current source for drive to Q117. Q115 and Q116 provide overvoltage and excess current protection for the amplifier. An excessive voltage or current output will cause the drop across R166 or 168 to become sufficiently large enough-

to begin to turn Q115 or Q116 on. The drive voltage for Q117 or Q118 will now begin to be shunted through Q115 or Q116 which effectively turns the output transistors (Q117 and Q118) off and protects the amplifier.

The circuit that drives the Overload lamp is part of the AC amplifier. An excessively large output voltage or current will cause the input to the AC amplifier to become large enough that the amplified AC at the collector of Q105 will turn Q107 off. The positive going output of Q107 will turn Q108 on. Q108 emitter is tied to ground (through 680 ohms) in the overload hold circuitry on the logic board so that as it turns on the overload hold circuitry will receive a positive going signal and be activated. At the same time the overload lamp which has ±112V on one side and the collector of Q108 through R127 on the other side will be turned on due to the voltage drop at the collector of Q108.

Model 3320, Dual Integrator

The Model 3320, Dual Integrator, contains all the components necessary for integration and the relays necessary for control.

The integrating components consist of 3, 1M resistors and 2, 100K resistors for inputs and 2 each 1 μfd, 0.1 μfd and 0.01 μfd capacitors. The 1 μfd and 0.1 μfd capacitors are contained in an oven. Refer to schematic 15108 for the actual circuitry.

The Model 3320 contains seven relays two of which (K302 and K303) are reed type relays. The following chart outlines the energizing sequence of the relays.

OPERATING MODE

RELAY	Bal/Pot Set	Reset	Compute	Hold	Static ck	Dynamic ck
Pot Set (K301)	Eng	No	No	No	No	No
Hold (K302)	No	Eng	No	Eng	No	No
Reset (K303)	No	Eng	No	No	No	No
Balance (K304)	Eng	No	No	No	No	No
Static (K305)	No	No	No	No	Eng	No
Time Scale (K306	Dependant only upon position of Time Scale Switch					
Dynamic (K307)	No	No	No	No	Eng	Eng

As a further reference see the chart on page 6 of the Operating Manual.

Model 3321, Dual Summer

The Dual Summer Module contains in addition to a Model 3310, Dual Amplifier a selection of input and feedback resistors. These are 5 1M and 4 0.1M resistors for input and feedback. Additional uncommitted components are four 20K resistors and four diodes.

NOTE: Do not use the input resistors associated with one amplifier as input or feedback resistors for another amplifier.

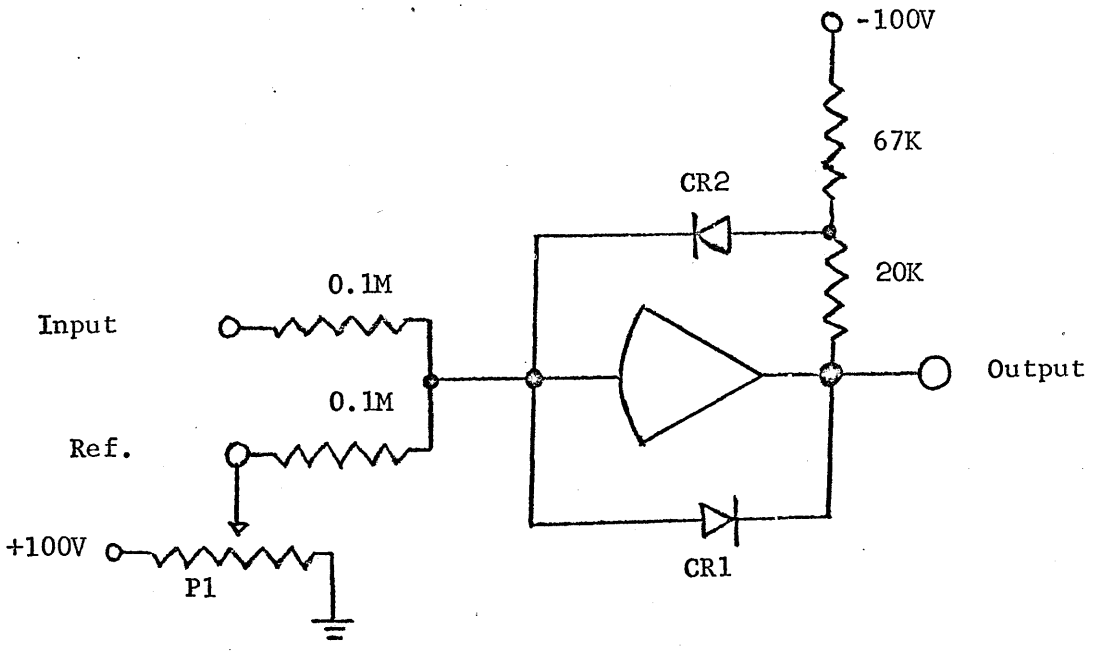
There are two relays on the Model 3321, the Pot Set Relay (K301) and the Balance Relay (K302). Both are energized in the Bal/Pot Set mode of operation. Refer to schematic 15106 for circuit details.

Model 3322, Dual Invertor

The Model 3322 contains 100K feedback and input resistors for an inverting function. Note that the connection from the summing junction to the junction of the amplifier must be made externally. The module also contains 20K resistors and diodes for limiting and comparator operation.

This module has two function relays included. Normally these relays are connected to energize from 0 ±100V signal. They can, however, operate from ±28V with minor modification. For 28V operation: 1) replace the relays with a 5.8 ma. 2.5K coil type. This type of relay is used as a balance relay (K301) and is available from the factory. 2) replace R308 and/or R309 with a 1.8K, 1/2w, 10% resistor. The relays will now operate from ±28V.

NOTE: ±100V will not damage the relays, during short periods of operation, but can cause heat damage if applied for a long period of time. It is <u>not</u> recommended that ±100V be used on modified functional relays. As these relays are often energized by a comparitor circuit, the following comparitor circuit is recommended for use with modified functional relays.



POTENTIOMETER PANELS (Section A4)

Section A4 has provisions for up to 120 potentiometers. The potentiometers are arranged in modules each containing 20 potentiometers. The modules are identical and each contains five logic relays, 20 1/32A (30ma) fuses, and 20, 30K, 10 turn potentiometers. When the "Pot Set" mode is engaged +100V is applied to the top of the potentiometers selected by the '10's switch (5319) in the Address Selector. By also engaging the '100's and units switches the operators can monitor the voltage at the arm of any selected potentiometer. See figures 2 and 12925 for potentiometer logic schematics. Figure 3 is a pictorial view of the rear of a potentiometer module indicating the positions of the relays and fuses.

POWER SUPPLY (Section A5)

Section A5, the power supply, consists of five sections: the AC supply (A5-5) a ±28V relay supply, a ±112 VAC supply, a ±28V supply, and a ±100 VAC reference supply. (refer to schematic 12859 page____for a block diagram of the power supplies). The supplies are interconnected and no attempt should be made to use the computer while any supply is removed.

The AC section (A5-5) is located at the bottom of the power supply wiring. Figure____outlines its principle components. The main power switch connects the AC line voltage, through F1 and F2, to T-102 (oven and relay supply transformer) which in turn supplies the +28V relay supply (6A).

T-101 (Amplifier and reference supply transformer) is supplied AC voltage through a parallel path from the main power switch when the following conditions are met:

10 Amp circuit breakers on ground

K501 is energized. (Amplifier power relay)

K501 is energized only when: S503 (thermal cutout) is closed, S601-2 (Problem board interlock switch) is closed and S122 (Power Switch on control center) is closed.

During normal operation the main power switch should be left on at all times so as to maintain oven temperatures. Thus, normal turn on of the computer will consist of energizing the Power switch on the control center.

Transformers, T-101 and T-102 both have dual primary windings connected in parallel and are capable of operation from 50 to 400 cycles. Wiring changes for 220V operation are shown on Figure____.

T-101 has six secondary windings. The chart below shows their ratings, uses and wire color.

Wire Color	Rating	Use
Wht/Grn	34V min at 1A	AC for +28V supply
Green	34V min at 1A	AC for -28V supply
Violet	128V min at 600 ma	AC for +100V supply
Wht/Red	132V min at 1.6A	AC rof +112V supply
Red	132V min at 2A	AC for -112V and -100V supplies
Brown	115V oms at 1.2A	AC for fan and DVM

The ratings with the exception of that for the fan and DVM supply, are for AC volts at the output of a bridge rectifier.

T-102 has two secondary windings: the Blue leads are 38V min at 6 amps, used to supply the +28V relay supply; the Brown leads are 115V rms at 100 ma, they are not used at present.

+28V, GA, relay supply (Section A5-5)

The +28V relay supply is composed of a bridge rectifier, parallel series regulators, and a two stage amplifier. CR105 in series with the +28V (R) sense input provides an emitter reference for Q404, the first amplifier. Base drive for Q404 is supplied through R415, the ±28V (R) adjustment potentiometer. The output of Q404 is fed to the base of Q403 which, in turn, supplies drive current to Q401 and Q402, the series regulators.

R401, R406, and the diodes CR405, 406, 407, 410, 411 form the elements of the overcurrent protection circuit. Operation of the circuit is as follows: as the load current increases the voltage drop through R401 and R406 increases. When this voltage drop reaches approximately 2.5V the series string of diodes becomes forward biased. The now forward biased diodes provide a low impedance path and shunt drive current from the series regulators. Thus, in the extreme case, a short circuit in the load causes virtually all of the drive current to be shunted around the series regulators and protects them from damage. Potentiometer, R401, is connected as a rheostat and provides adjustment of the circuit to the ~~tolerences~~ tolerances of a particular supply.

The circuit of CR410, CR411, R421, and R422 provides overvoltage protection for the supply to ground, through R422; should the output rise to +30V (approx), CR411 will conduct. When CR411 conducts it supplies a signal to the gate lead of CR410 (CR410 is a TCR); this signal turns CR410 on. With

CR410 on the output of the supply has a very low impedance path to ground (through CR410 and R421) which causes the output current to rise to its maximum value of 6 amps. As the current attempts to rise further the overvoltage circuit begins to operate and the supply is effectively turned off.

NOTE: If the overvoltage circuit is activated the supply must be turned OFF to reset it.

±28V Supply (Section A5-3)

The ±28V supply is a 1 ampere supply primarily used for bias voltages in the Model 3310, Operational Amplifier. It is a dual supply consisting of two nearly identical sections with the output taken from opposite sides of the bridge rectifier to produce the two polarities. The only difference in the supplies is the location of the series regulator, in the +28Volt section the regulator is in series with the output voltage, while in the -28Volt section the regulator is in series with ground. Using the -28Volt as an example, a brief description of the supplies operation is as follows: The -28V sense input is applied to resistor the network (R321, 322, 323, 329) and taken from the arm of R329 (which also serves as the adjustment potentiometer) to supply base drive to Q306. Q306 and Q305 form a differential amplifier. Note that the base drive for Q305 is supplied from a reference diode. The output from the differential amplifier provides drive for Q304, which in turn drives Q307, the series regulator. Current protection is provided by CR316 and CR318 in much the same manner as the +28V (R) supply R301 provides a current protection adjustment.

±112V Supply (Section A5-2)

This supply produces the ±112V necessary for the output stages of the Model 3310 Operational Amplifier. It is capable of delivering 1.5 ampere. In operation it is similar to the +28V (R) supply. Q208 and Q206 (in the +112V section) form a two stage amplifier which drives Q203 the series regulator. The input and reference connections are the same as those in the +28V (R) supply. Current protection is provided by the series diodes, CR211, 212, 224, 225. In this case when the diodes become forward biased,

due to excess voltage drop across the series regulator, Q202 is turned on and shunts drive from the series regulator. When the voltage drop across the regulator reaches approximately 47V the Zener diode, CR215, will trigger. The series combination of R240, CR215, and R210 will then determine the current the supply produces will in a short circuit condition. Except for the value of the components the overvoltage circuit is identical to that in the +28V (R) supply.

±100V Reference Supply (Section A5-1)

MAINTENANCE AND TROUBLESHOOTING

Introduction

Maintenance of the SD 40/80 is straightforward and consists, mainly, of periodic adjustments. The routine adjustments required as outlined in sections 2.5 through 2.11 of the SD 40/80 Operating Manual. A complete adjustment of the computer will take about 15 minutes, less for an SD 40. The frequency of adjustment will vary as it is a function of the accuracy of solution required. The other principle factor that affects time between adjustments is whether the computer is turned on and off frequently. If the computer is left on continuously the adjustments will maintain accuracy for a much longer period of time.

NOTE: If the computer has been turned off (with control panel switch) allow a minimum of 30 minutes warm-up time before adjustment.

If the computer has been turned off (with main power switch) allow 16 hours warm-up (overnight).

Other non-routine adjustments are covered in the sections on each module. Test Equipment required to maintain the computer is outlined in the following listing:

1) Multimeter, E-1-R Model 110 or equivalent
2) Oscilloscope, Techtronix 561 with 2A63 plug-in
3) Differential Voltmeter, Fluke, Model 801 or equivalent
4) Time Interval Meter, S-D Model 1013 or equivalent
5) Module Extender, Furnished with computer

Section A1-1 Function Generator

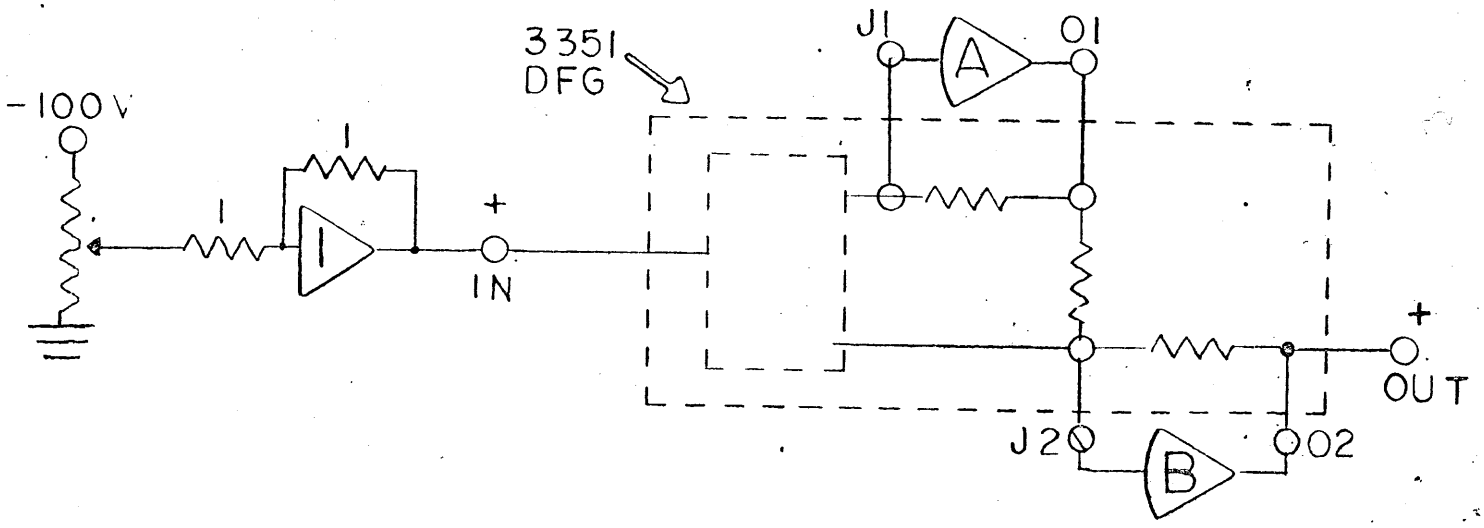
Maintenance: No maintenance or adjustment is required in this section.

Troubleshooting: If a Model 3351 is suspected of being faulty first substitute another in its place. If this does not cure the problem check the Function Generator wiring for continuity to the problem board (see Table 2) in addition check Pin 5 of the receptical for +100V, pin 2 for -100V and Pin 3 for ground.

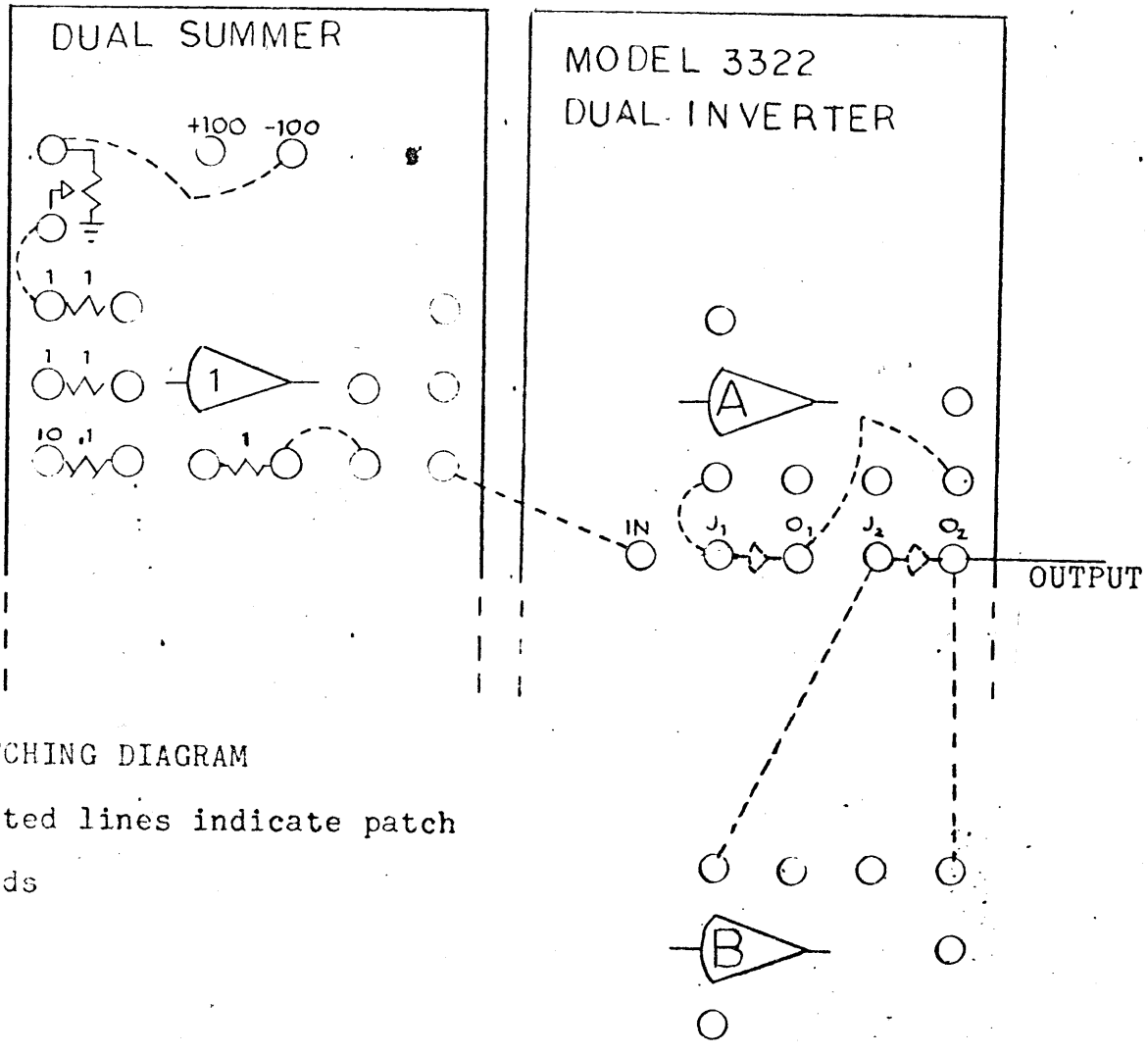
If by substitution the Function Generator is proved to be faulty follow the procedure outlined below. Table shows the set-up for this test. The faulty section of the Function Generator will make one or more of the slopes or break points impossible to set properly. The faulty component in that section can then be isolated by resistance checks. (see schematic 14259).

A) Check adjustability of break and slope adjustments by setting up a linear function with a slope of unity as follows:

1. Set all positive break and slope adjustments to most CW position.
2. With e_{1N}= + 25V, set 1st +break point to zero (most CCW), adjust 1st +slope for an output of +37.5V.
3. With e_{1N}= + 25V, set 2nd +break point to zero, adjust 2nd +slope for an output of +25V.
4. With e_{1N}= +25V, set 3rd +break point until a detectable change of output is observed. Change e_{1N} to +50V and adjust 3rd +slope for an output of +62.5V.
5. With e_{1N}= +25V, set 4th +break point until a detectable change of output is observed. Change e_{1N} to +50V and adjust 4th slope for an output of +50V.



FUNCTION GENERATOR TEST SET-UP



PATCHING DIAGRAM

Dotted lines indicate patch cords

6. With e_{1N} = +50V, set 5th +break point until a detectable change of output is observed. Change e_{1N} to +75V and adjust 5th +slope for an output of +87.5V.
7. With e_{1N} = +50V, set 6th +break point until a detectable change of output is observed. Change e_{1N} to +75V and adjust 6th +slope for an output of +75V.
8. Repeat above steps from 1 to 7 for negative portion of the function.

Section A1-2 DVM Readout

Maintenance: The only maintenance required in this section is an occasional cleaning of the Bezel which covers the DVM readout indicators. A glass cleaning compound such as GTC-59 is recommended for this purpose. Care should be taken to use a soft cloth or tissue while cleaning so as to avoid scratching the Bezel.

To remove the Bezel the four nuts located on the rear of the Bezel at each corner must be removed using a 5/8" Nut Driver or socket wrench. The entire assembly may then be pulled back and the Bezel removed.

Troubleshooting: The most likely sources of trouble in the DVM readout are the indicator tubes. They may be checked by substitution. If this does not cure the problem refer to the supplement on the DVM.

Section A1-3 Address System

Maintenance: No maintenance or adjustment is required in this section.

Troubleshooting: The best means of troubleshooting the address system is by continuity checks. Following the sequence of the simplified routing diagram on page____will quickly locate a faulty switch or wiring. Refer to drawings 13553, 14920 and 14921 for location details. The ohm meter leads may be connected between the Ext jack at the side of the control wing (be sure to select EXT) and the problem board. With the proper address selected the ohm meter should read a short. If the reading is 'open' check back from the selected address towards the EXT jack until the problem area is located.

NOTE: It is advisable to check with the factory before attempting any repair of the Address selector switch.

Section A1-4 Meter Section.

Maintenance: The only maintenance required is an occasional adjustment of the mechanical zero on the meter movement. Access to this screw-driver adjustment is through the small hole immediately below the meter face.

Troubleshooting: The meter circuitry is straightforward and may be trouble-shot in the same manner as any meter circuit. Points to remember are the 10 ma fuse in series with the arm of the reference pot and that the meter select switches are interlocked.

Section A1-5 Logic Control

Maintenance: No maintenance or adjustment other than changing bulbs in the switches is required for this section.

To change a bulb pull the cover from the bulb, this may require quite a firm pull as the covers fit tightly. The bulb may then be removed using the special tool that is furnished with the computer.

Troubleshooting: Checking the voltages on the Logic Control test panel (see page 6 of the Operating Manual) is the first step in troubleshooting. If a voltage is missing make a visual check of the relays to insure that they are energizing. If the relays are energizing check the base of the first transistor in the driver circuit for a positive going signal as the Mode button is pressed. If the signal is present check both driver transistors.

The above procedure will locate most problems, for detailed information refer to the schematic diagram.

Section A2 (DVM Electronics)

Maintenance: There are two adjustments for the DVM; a zero adjust and a 100V calibration adjust. To make these adjustments proceed as follows:

1) Ground the input to the DVM
2) Set the zero adjust (see figure____for location) for a minimum reading on the DVM readout. The adjustment should be made to a tolerance of ±1 count
3) Adjust computer plus and minus one hundred volts as accurately as possible (see Section A5-1 for procedure)
4) Apply +100V to the input of the DVM
5) Set the 100 volt calibration adjust for a reading of +100.00. The tolerance is ±1 count.

Troubleshooting: see the DVM supplement for troubleshooting procedures.

Section A3-1 Through 12

Maintenance: No maintenance other than routine cleaning is necessary in this section. Maintenance and adjustment of the individual modules is discussed in the sections on each module.

Troubleshooting: There are no specific troubleshooting procedures for this section. Problems which occur in this area will normally be found by following the procedure for the module or logic function that is affected.

Computing Modules

The following sections detail the maintenance and troubleshooting for each of the various types of computing modules.

To remove a computing module first remove the problem board; then remove the holding bars at the top and bottom edges of the module. The module may now be removed using the special tool provided with the computer.

Maintenance: The only normal maintenance required for the computing modules is a periodic cleaning of their problem board contacts. Alcohol is recommended for this purpose.

Troubleshooting

The first step in troubleshooting any computing module is to replace its amplifier with a known good amplifier. After this step is accomplished the rest of the module is easily checked out using a Volt/Ohmeter.

The Volt/Ohmeter checks fall into two categories: checks with power off and checks with power applied. Charts of resistance and voltage readings for each type of module will be given in the next section. A study of tha applicable module schematic will quickly locate the faulty component should the resistance or voltage reading be abnormal.

Model 3320

Make the following resistance and voltage checks.

POWER OFF CHECKS

Check	Read
A3-B3	1 Meg
A4-B4	1 Meg
A5-B5	100K
A10-B10	1 Meg
A11-B11	1 Meg
A1-A2	0 to 30K as pot is turned
A12-A14	" " "
B13-B14	" " "
J5-E5	50K
E5-F5	50K
D10-E10	50K
E10-F10	50K
C3-D1	OPEN
C3-D2	OPEN
C3-D3	OPEN
C12-D12	OPEN
C12-D13	OPEN
C12-D14	OPEN

POWER ON CHECKS

In Balance/Pot Set Mode

B4-C3	OPEN
B3-Gnd	Short
B10-C12	OPEN
B10-Gnd	Short

POWER ON CHECKS (jumpers in for Logic)

	Bal/Pot set	Reset	Compute	Hold
B3-C3	OPEN	OPEN	Short	OPEN
B3-Grd	Short	OPEN	over 50K	OPEN
C3-E5	OPEN	Short	OPEN	OPEN
B10-C12	OPEN	OPEN	Short	OPEN
B10-Gnd	Short	OPEN	over 50K	OPEN
C12-E10	OPEN	Short	OPEN	OPEN

POWER ON CHECKS (no Logic jumpers)

B1	+28V (Heat off) .5V Heat on, cycle is approximately 2 min to 30 min dependant upon how long the computer power supply has been on.
F7	+28V in RESET (or in RESET cycle of REP-OP)
F8	+28V in HOLD only
E6	+28V in RESET only
D7	+28V in COMPUTE only
D8	+28V in COMPUTE only
C4	+112V normally, 0V when amp is in Overload
D4	+112V at all times
C11	+112V normally, 0V when amp is in Overload
D11	+112V at all times

MODEL 3321, Dual Summer

POWER OFF CHECKS

Check	Read
A3-B3	1 MEG
A4-B4	1 MEG
A5-B5	100K
A6-B6	1 MEG
A10-B10	1 MEG
A11-B11	100K
A9-B9	1 MEG
D2-E2	20K
E2-F2	20K
D13-E13	20K
E13-F13	20K
C6-D6	100K
C9-D9	100K
E6-F6	Check both directions for diode polarity
D3-E3	" " " " " "
E9-F9	" " " " " "
D12-E12	" " " " " "

POWER ON CHECKS

	Bal/Pot set	All other Modes
B3-C3	OPEN	Short
B3-Gnd	Short	OPEN
B10-C10	OPEN	Short
B10-Gnd	Short	OPEN

MODEL 3322, Dual Inverter/Function RELAY

POWER OFF CHECKS

Check		Read
A4-B4		100K
A5-B5	100	100K
A10-B10		100K
A11-B11		100K
F2-F3		20K
F3-F4		20K
F13-F12		20K
F12-F11		20K
D2-E2		Check both directions for diode polarity
D3-E3		" " " " " "
D12-E12		" " " " " "
D13-E13		" " " " " "

POWER ON CHECKS

Check	Read	Read
B9-A9	Short-Apply +100V to C7	OPEN
B8-C8	Short- " " "	OPEN
E9-D9	Short-Apply +100V to F7	OPEN
E8-F8	Short- " " "	OPEN
A8-A9	OPEN- Apply +100V to C7	Short
C8-C9	OPEN- " " "	Short
D8-D9	OPEN- Apply +100V to F7	Short
F8-F9	OPEN- " " "	Short

MODEL 3323, Dual Multiplier

POWER OFF CHECKS

Check	Read
A4-B4	100K
A5-B5	100K
A10-B10	100K
A11-B11	100K
F7-B7	40K
C6-B7	60K
C6-D7	40K
F7-D7	40K
F8-B8	40K
C9-D8	40K
B8-D8	50K
C9-B8	40K

GENERAL PURPOSE COMPUTER CHECK

A general computer check may be accomplished by patching all computing modules in three basic systems. These systems will give the operator a quick check on the operation of each of his computing modules and in the event of a failure aid the troubleshooting process. The test systems should be set up on a spare problem board and left on that board at all times. A chart should be made which indicates the correct reading at the output of each amplifier in each of the operating modes. (See the attached sample).

By following the procedure outlined below a thorough check of the computer will be made.

Step 1. Patch the systems as shown on the "Computer Test Circuits" diagram. The Integrator and Multiplier systems may have to be repeated several times until all integrators and multipliers are in a system. The integrator system may be expanded to contain more than five Integrators but the Multiplier systems should be limited to four multipliers to prevent loading effects. As was mentioned before it is best to construct the checkout systems on a spare problem board and keep them on that board.

Step 2. Turn the Computer ON and check the Balance of all amplifiers. Next set all potentiometers used in the test systems. ±0.1Volt is a satisfactory balance for most applications.

Step 3. Adjust the + and - 100V power supplies, check all other power supplies and adjust if necessary.

Step 4. Check all Integrators for the correct output.

Step 5. With the computer still in the RESET mode place the function switches associates with each multiplier system in the UP position. Note the reading at each multiplier output. Place the Function Switches in the DOWN position note the readings and adjust the X gain until the difference (if any) between the UP and DOWN positions is at a minimum.

Place one function Switch in each system UP and the other DOWN, note the readings at the outputs of the multipliers. Reverse both function switches, note the reading and adjust the Y gain if necessary.

Step 6. Check the output of all amplifiers in the summer system. Note that it is correct. The outputs of amplifiers near the end of a long series of summers may have noticable errors. The allowable error may be calculated by number of summers times 0.03%. For instance the sixth summer in a series has an allowable error of 0.18% (NS x 0.03%) (6 x 0.03% = 0.18%).

Step 7. Place the computer in the COMPUTE mode. The computer should transfer to the HOLD mode after 9 seconds. Again check all integrators and the summers connected to them for the correct output.

Step 8. (Optional) Place the computer in the RESET mode and place the time scale switch to B. Repeat step 7. The computer should transfer to HOLD in 0.9 seconds.

When taking readings a tolerance of ±2V should be observed. Although these checks are not designed to check accuracy, but operation, any voltage reading outside a ±2V tolerance should be checked for out of tolerance components.

AMP	BALANCE	RESET		HOLD	
		Correct	Observed	Correct	Observed
#1					
#2					
#3					
#4					
#5					
#6					
#7					
#8					
#9					
#10					
#11					
#12					
#13					
#14					
#15					
#16					
#17					
#18					
#19					
#20					
#21					
#22					
#23					
#24					
#25					
#26					
#27					

MP	BALANCE	RESET		HOLD		
		Correct	Observed	Correct	Observed	
#28						
#29						
#30						
#31						
#32						
#33						
#34						
#35						
#36						
#37						
#38						
#39						
#40						
#41						
#42						
#43						
#44						
#45						
#46						
#47						
#48						
#49						
#50						
#51						
#52						
#53						
#54						
#55						

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SCHEMATICS

1. Dual Integrators – M3320 15108E
2. Dual Summer – M3321 15106D
3. Dual Inverter/Function Relay – M3322A 15105C
4. Dual Inverter/Multiplier – M3323 15107E
5. Dual Inverter/Quad. Electric Switch – M3324 14918D
6. Quad Summer – M3325 17078A
7. Flip-Flop Module – M3326 17550A
8. Logic "And" Gate Module – M3327 17549A
9. Digital Clock – M3328 17565A
10. Flip-Flop/Gate Module – M3326A 19546A
11. Quad Integrator – M3329 17946-XP4
12. Squaring Net Works ¼ Sq. Mult. QSM 19331-XP2
13. Function Generator – Model 3351 14259E
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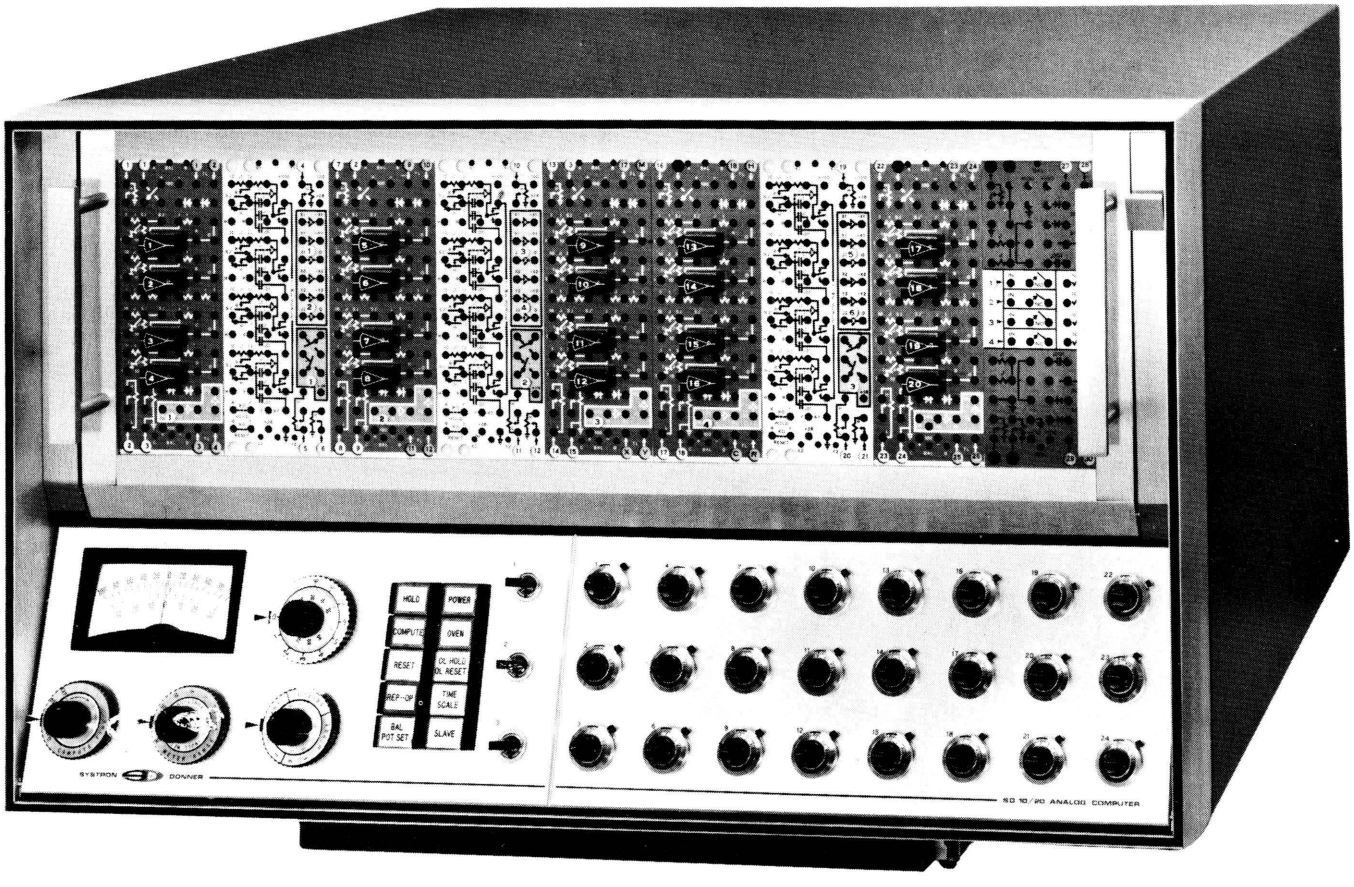


MODEL 10/20 ANALOG COMPUTER

SYSTRON DONNER
CORPORATION

WARRANTY

Systron-Donner instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. This warranty does not apply to vacuum tubes, except as they are warranted by tube manufacturers. The liability of Seller under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer at his expense during such period and which has not been subjected to misuse, neglect, improper installations, repair, alteration, or accident. Seller shall have the right of final determination as to the existence and cause of a defect. In no event shall Seller be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, express, implied or statutory, and no agreement extending or modifying it will be binding upon Seller unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Systron Donner instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the unit is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company.

REPAIRS

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

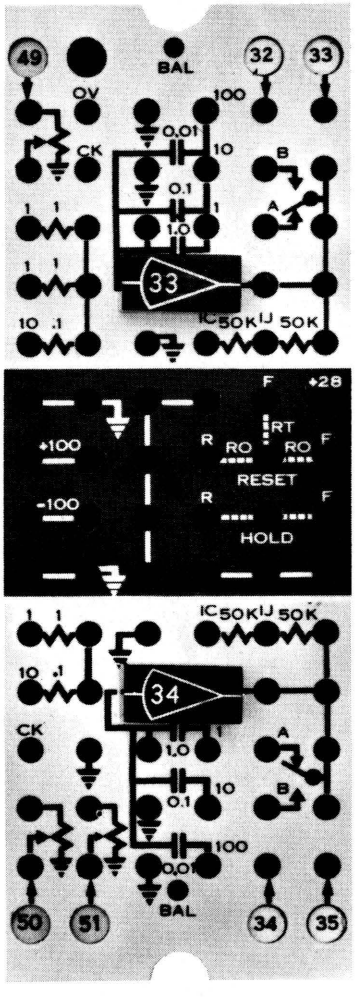
Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative or Sales Manager, Instruments, Systron-Donner Corporation, 888 Galindo Street, Concord, California.

Chapter I — INTRODUCTION

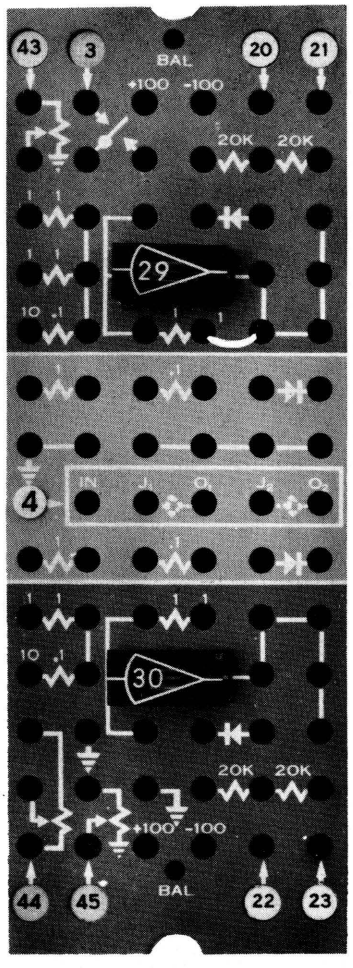
I. INTRODUCTION

The Model SD 10 20 is an all solid state Analog computer with an operating range of ±100V and expansion capabilities for up to 24 operational amplifiers. The principle features of the computer are full ±100V computing range, all solid-state design, compact modular construction of all computing components, removable problem board which mates directly with computing modules to eliminate all problem board cabling, a control center with readout selectors for amplifiers and potentiometers, high-speed reed relays and solid-state switches, complete logic capability for rep-op and iterative operations, 0.01% accuracy of computing resistor and capacitor networks, a panel voltmeter having a null mode of measurement with 0.02% (of full scale) resolution. The amplifiers are protected against accidental grounding of their outputs as are all power supplies.

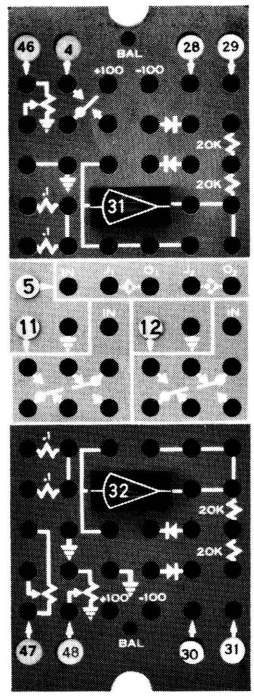
All computing components in the Model SD 10/20 are modular plug-in units which allow the user a wide choice of computing capabilities. There are several types of computing modules available for use in the SD 10/20. The listing which follows gives a brief description of each type.



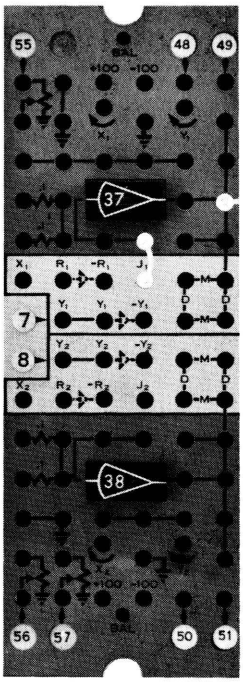
Model 3320: Dual integrator with two uncommitted operational amplifiers.



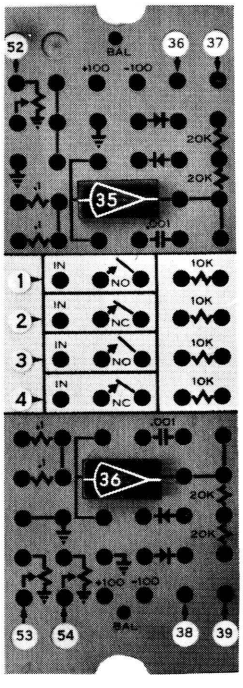
Model 3321: Dual summer with two uncommitted operational amplifiers.



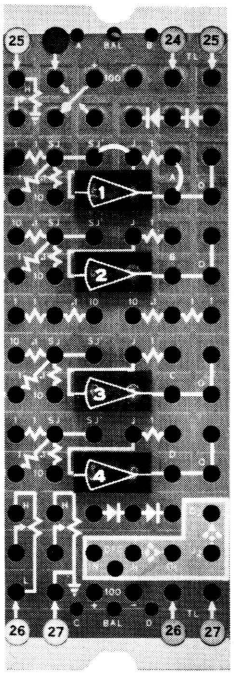
Model 3322A: Dual inverter, dual operational relay. Two uncommitted operational amplifiers with two operational relays.



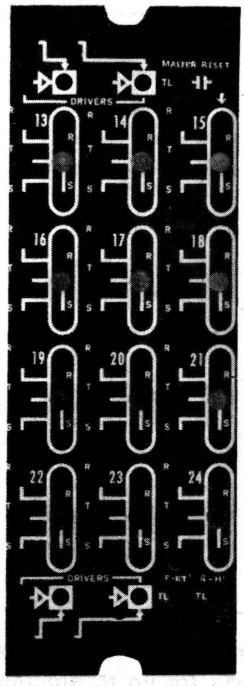
Model 3323: Dual multiplier, two four quadrant quarter square type multipliers with two uncommitted operational amplifiers.



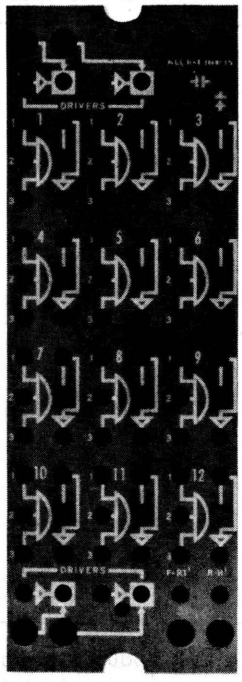
Model 3324: Electronic switch, four high speed electronic switches with two uncommitted operational amplifiers.



Model 3325: Quad summer, four summing networks with four uncommitted operational amplifiers.

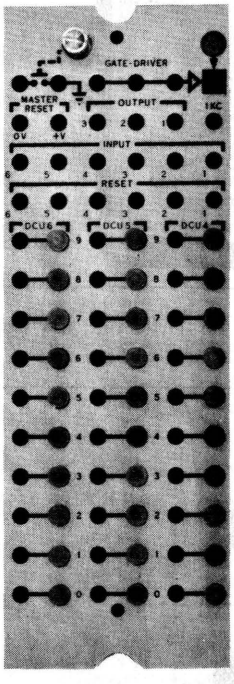


Model 3326: Flip-flops, twelve RST flip-flops with four relay drivers.

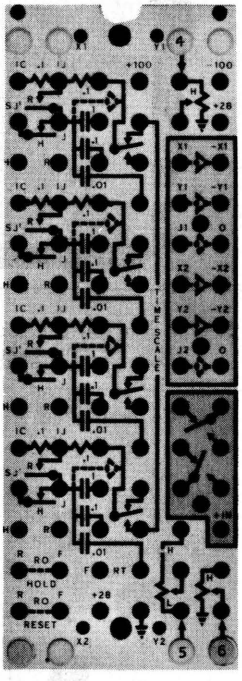


Model 3327: Gates, twelve three-input AND gates with four relay drivers.

Model 3326A: Six RST flip-flops, six AND gates and four relay drivers.



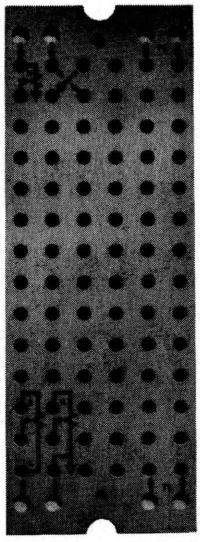
Model 3328: Time-event control. One kilocycle clock with three decade dividers, three decade counters and one gated relay driver.



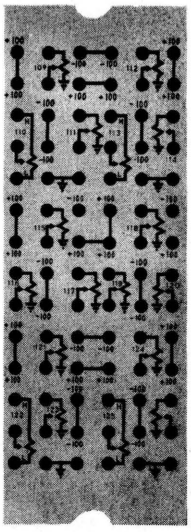
Model 3329: Quad integrator, dual multiplier, operational relay. Contains four integrating networks, two four-quadrant multipliers and one operational relay.

Model 3329A: Same as Model 3329, less multipliers.

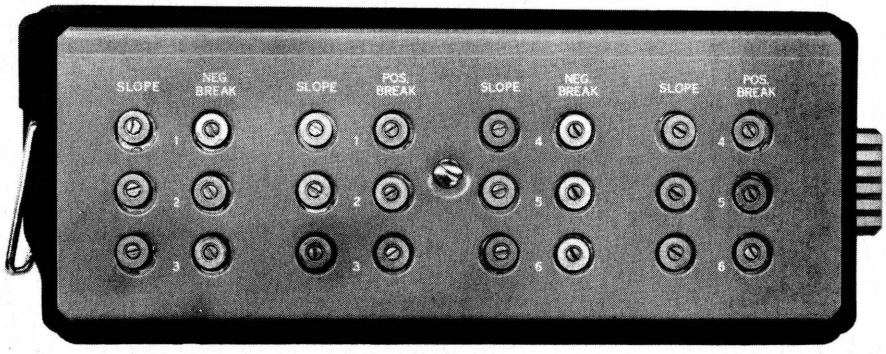
Other accessory units for the Model SD 10/20 are as follows:



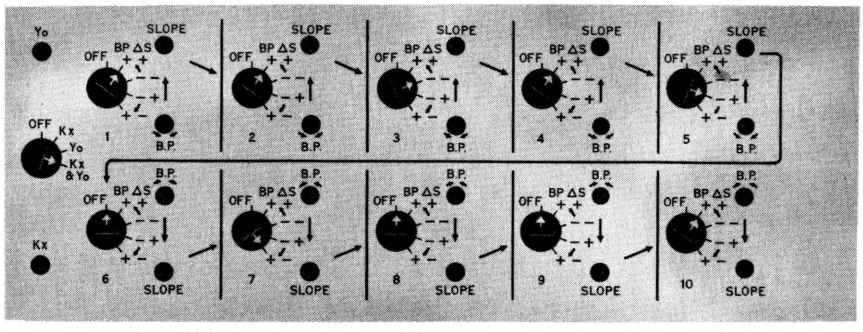
Model 3346: Utility module, contains vector board and connections to enable user to connect special networks and circuits into the computer.



Model 3347: Potentiometer Terminator provides terminations for up to eighteen potentiometers should application require more than the normal three potentiometers terminated in each computing module.



Model 3351: Variable Diode Function Generator has 12 segments, six positive and six negative, each adjustable for slope.



Model 3352: Variable Diode Function Generator, has 11 segments each adjustable for slope and break point polarity. Offers higher resolution and lower noise levels than the Model 3351.

1.2 *Maximum Capacities*

The listing which follows gives the maximum number of the various elements that may be used in the SD 10/20. If no maximum is given, it may be assumed that the physical limitations of the computer are the only considerations to be borne in mind.

	Maximum Capability
Modules	9
Amplifiers	24
Integrators	16
Potentiometers	24
Variable Diode	
Function Generators	5
Logic Modules	3
(the total of integrator and logic *modules* must not exceed four)	

If the complement required for any particular application exceeds any of the maximums above consult the factory for information regarding special modification of the computer.

1.3 *Installation*

The chapters that follow detail the operation of the Model SD 10/20. It is important that all operating procedures be followed and that the recommended maintenance checks are performed at regular intervals and that the section on special operating and protective features be observed. Adherence to the instructions and procedures set forth in this manual will assure long life and trouble-free operation of the Model SD 10/20.

The Model SD 10/20 should be uncrated as soon as possible after receipt and given a thorough mechanical inspection. If the mechanical inspection is satisfactory it should be followed immediately by the electrical inspection recommended in Chapter IV.

The SD 10/20 may be mounted on any convenient flat surface or portable base provided that air flow to the cooling fan on the rear of the computer is not restricted. The computer will operate satisfactorily in ambient air temperatures from 40°F to 100°F. For operation outside these limits consult the factory.

Power requirements are as follows:

Power consumption: 550 watts maximum
250 watts typical

Power source: Connections provided for 115V, 220V, 230V, 240V, 250V, ±10%, 50-400 cps.

The computer is normally connected for 115V, 60 cycle operation. Instructions for other connections will be found inside the rear door of the computer.

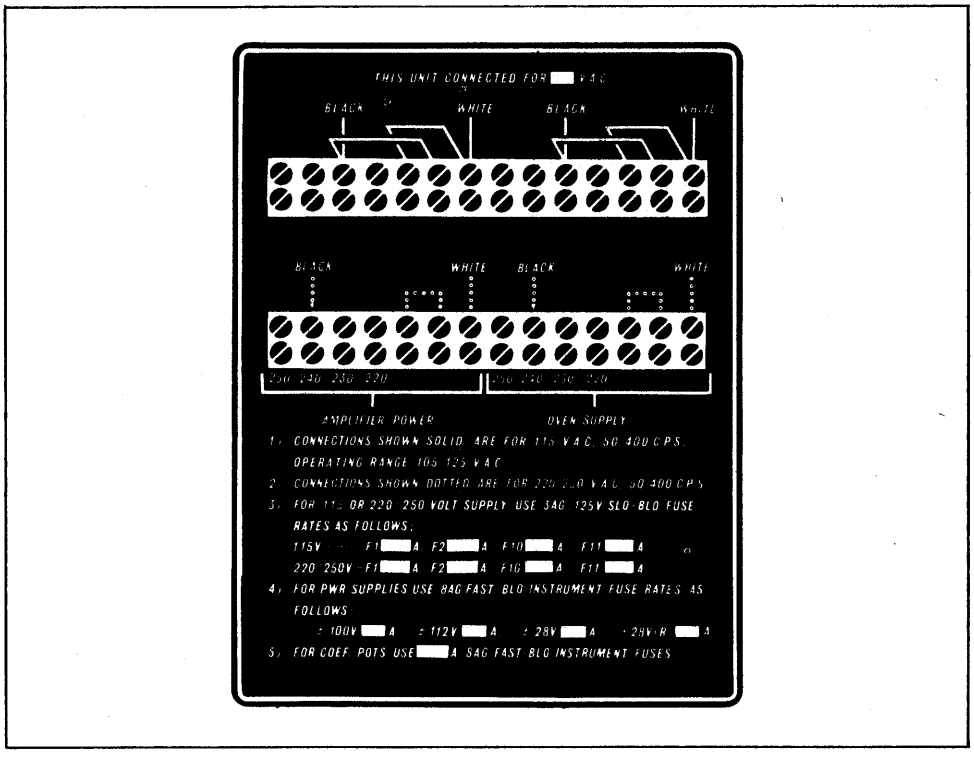


Figure 1: Line Voltage Connections

DUAL INTEGRATOR – MODULE 3320

Feedback Capacitors (in oven) 1 μF, 0.1 μF: Trimmable to better than 0.01%.
Feedback Capacitor 0.01 μF: ±1%
Tolerance of Input Resistors and Resistors in Reset Circuit: ±0.01%
Temperature Coefficient of 0.01% Resistors: ±5 ppm/°C
Nominal Temperature in Oven: 45°C
Temperature Regulatilon of Oven: ±1°C
Reset and Hold Relays: Reed Relay switching speed 1 msec, differential time <500 μsec typical
Integrator Drift (R_{in}= 1M, C_{fb}= 1 μF): 50 μv/sec typical, 100 μv/sec max.
Noise at output (with C_{fb}= 1 μF): <2 mv p-p (0 to 2 kc)
Bandwidth as Summer (R_c = 1M): >13 kc (within 3 db)

DUAL SUMMER – MODULE 3321
QUAD SUMMER – MODULE 3325

Tolerance of Input and Feedback Resistors: 0.01%
Temperature Coefficient of 0.01% Resistors: ±5 ppm/°C
Bandwidth (R_{in}= R_{fb}= 100k, no capacitive loading at summing junction or output): >200 kc (within 3 db)
Bandwidth (R_{in}= R_{fb}= 1M): >50 kc (within 3 db)
Velocity limit: $>3 \times 10^6$ volt/second
Noise at output (R_{in}= R_{fb}= 1M with R_{in} grounded): <10 mv p-p (0 to 2 kc).
Cross talk at 100 cps (R_{in}= R_{fb}= 1M): <–66 db
Phase shift at 100 cps: <0.03°

DUAL FUNCTION RELAY/COMPARATOR MODULE 3322 & 3322A

Two Function Relays: Two Form C
Tolerance of Input and Feedback Resistors: 0.01%
Temperature Coefficient of 0.01% Resistors: ±5 ppm per °C
Bandwidth (R_{in} = R_{fb}= 100k): >200 kc (within 3 db)
Noise at Output (R_{in}= R_{fb} = 100 k): <5 mv p-p (0 - 2 kc)
Phase Shift at 100 cps: <0.03°
Pull-in Time:
Module 3322 — 10 millisec
Module 3322A — 1 millisec
Energizing Voltage: ±28v to ±100v.

DUAL MULTIPLIER/DUAL INVERTER MODULE 3323

Frequency Response
Amplitude: X = ±100, Y = 1 sin ωt. } <3 db at 50 kc
Y = ±100, X = 1 sin ωt. }
Phase Shift: <0.1° at 100 cps
Input Resistance: Multiplier mode approx. 20 kΩ (varies with input levels)
Drift: X = Y = ±100 25 mv per 2 hrs.
X = Y = 0 5 mv per 8 hrs.
Noise: 20 mv p-p (0 to 10 kc)
Zero Offset: X = Y = 0 20 mv max.
X or Y = 0 60 mv
Static Accuracy: 0.05%, 100 mv error typical

HIGH ACCURACY MULTIPLIER/DUAL INVERTER MODULE 3323-1

Input Range: ±100 v max.
Output Range: ±100 v max.
Static Errors: X = 0, Y = 0 ±2 mv
X = 0, Y = ±100 v ±15 mv
X = ±100 v, Y = 0 ±15 mv
X = ±100 v, Y = ±100 v ±30 mv
Frequency Response: –3 db point above 20 kc
Noise — Wide Band: <25 mv p-p
Multiply Mode: Inputs: X and Y, range ±100 v
Output: 0.01 XY, range ±100 v
Divide Mode: Inputs: X range ±100 v
Y always negative –100 v ≤Y <0 and |X/Y| ≤1
Output: 100 X/Y, range ±100 v
Squaring Mode (two independent channels):
Input: X, range ±100 v. Output: 0.01 $|X|^2$, range ±100 v.
Input: Y, range ±100 v. Output: –0.01 $|Y|^2$, range ±100 v.

QUAD ELECTRONIC SWITCH MODULE 3324

Excitation Voltage: +20 to +100 v
Excitation Current: <2 ma
Max. Current passable through Switch: 3 ma
Max. Voltage across Switch with one side grounded: ±10 volt
Impedance with switch "ON": <200Ω
Rise Time of Switch (into a resistive load): 1 μsec
Error Current: $<5 \times 10^{-7}$ amps with Switch "ON"; $<10^{-9}$ amps with Switch "OFF."
Switch Rate: 1 kc max.
10 kΩ Resistors: Tolerance, 0.01%; Temp. Coefficient, 5 ppm/°C
0.001 μF Capacitors: Tolerance, ±1%, 500 w.v.d.c.

MODEL 3351

Input Voltage: ±100 v max.
Output Voltage: Arbitrary function of input volt. within range ±100 v.
Frequency Response: 1 kc
Input Impedance: Greater than 45 kΩ (depends on function)
Output Impedance: Less than 0.1Ω (output Z of amplifier).
Function Simulation: Straight-line approximation of 12-line segments.
Line Segments: 12 breakpoints total
6 adjustable between 0 & +100 v, 6 adjust. between 0 & –100 v.
Slopes: Each segment has a max. adjustable slope of 2.5 v/v input. (Larger slopes are obtainable by adding individual line segments.)
Noise: 150 mv p-p Power Requirements: ±100 v, ±6 ma

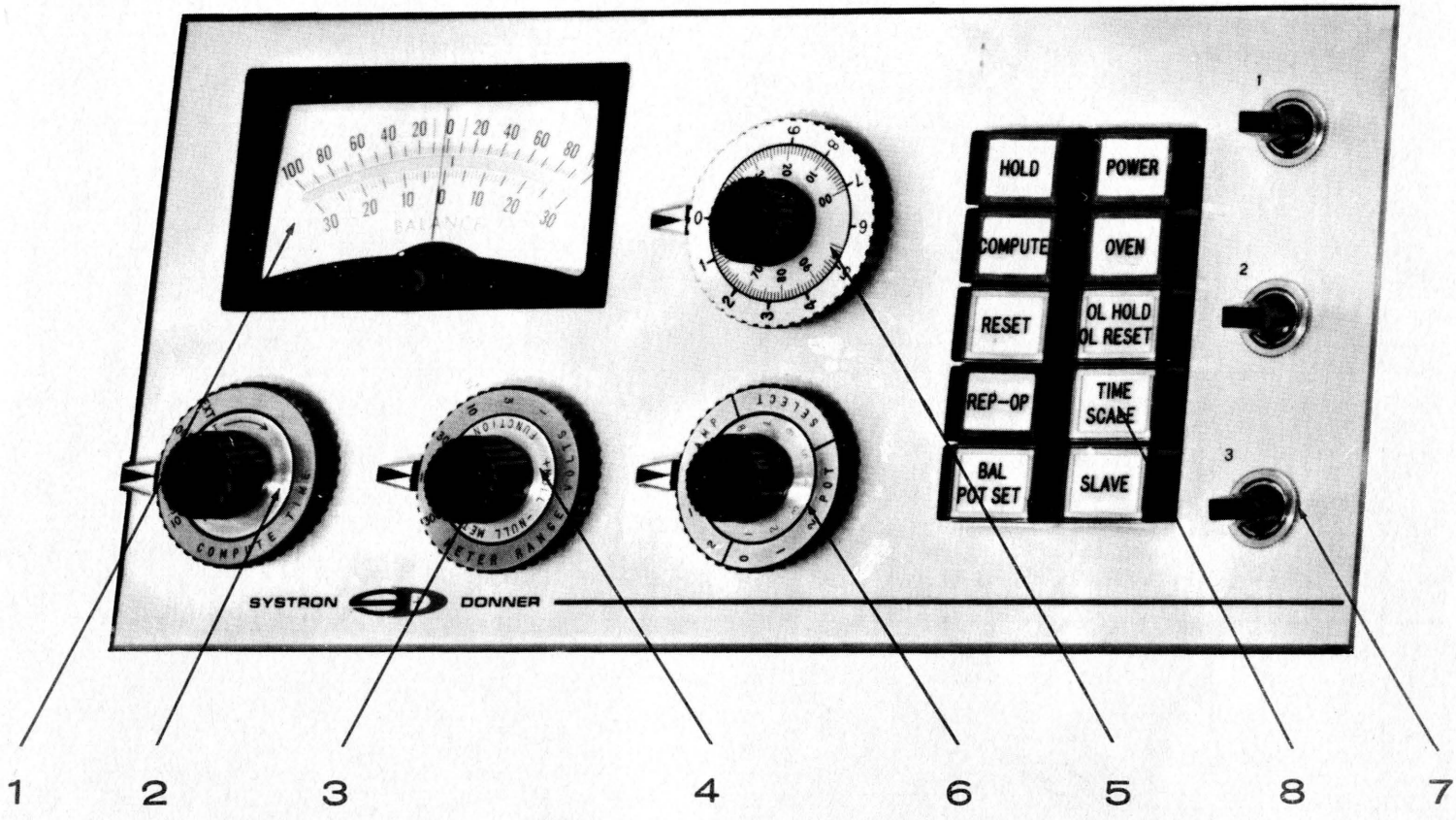
MODEL 3352

Inputs Required: ±X (±X can be common for several functions of X)
Input Voltage: ±100 v max.
Output Voltage: Arbitrary function of input volt. within range ±100 v.
Input Impedance: Greater than 39 kΩ (depends on function)
Output Impedance: Less than 0.1Ω (output Z of amplifier).
Function Simulation: Straight-line approximation with 11 segments.
Noise: 50 mv p-p (DC to 2 kc)
Linear Segment Complement:
K_X adjustment: sets initial slope through origin of ±5 v/v max.
Y_O adjustment: sets Y at X = 0 (between ±100 v)
10 breakpoint-slope controls, each programmable to any of the following five combinations:

	No. 1	No. 2	No. 3	No. 4	No. 5
Breakpoint	+	–	–	+	off
Slope Change	+	–	+	–	off

Max. Slope Change per Breakpoint: 2.5 v/v, breakpoints may be stacked together for increased slope change; 22-segment function generation possible by paralleling two Model 3352 VDFG cards.

1.5 Control Panel



[1] **Meter Readout Ranges:** 1, 3, 10, 30, 100, and 300 volts, and ± null. Full scale accuracy: 3%. Null position provides 0.02% F.S. resolution with reference potentiometer having a ±0.05% linearity at 25°C.

[2] **Compute Time Selector** — compute time continuously variable from 5 msec to 10 sec. Reset time varies from 5 msec to 5 sec, depending upon coarse steps of compute range.

[3] **Meter Range Selector** — with positions for 300 v, 100 v, 30 v, 10 v, 3 v, and 1 v. Serves also as sensitivity adjustment for ± null.

[4] **Function Selector** — for rapid choice of: + null, − null, Meter, External (connects selected bus to external jack).

[5] **Null Reference Potentiometer** — provides high accuracy readout using null method with 0.02% F.S. resolution. Linearity is ±0.05% at 25°C.

[6] **Address Selector** — address capability of 20 amplifiers and 24 potentiometers.

[7] **Function Switches** — provide manual switching flexibility in problem solutions.

[8] **Mode Selection** (lighted pushbuttons):

Hold — places problem solution on all integrators into hold position.

Compute — applies problem voltages to all integrators.

Reset — applies initial condition voltages to integrators.

Rep-Op — places integrators into a repetitive operation cycle. Compute time variable from 5 msec to 10 sec.

Bal/Pot Set — disconnects junction and grounds the input resistor summing junctions of all amplifiers. Each amplifier is converted to a gain of 2500 for precision monitoring of junction offset.

Pwer On/Off — energizes and de-energizes computer.

Oven — indicates +28-volt oven power is on to maintain constant temperature of computing capacitors.

OL Hold, OL Reset — lights up when any amplifier is overloaded. When depressed, computer goes into Hold; when released, normal operation is resumed.

Time Scale — activates relays in each integrator module to change computing capacitor. (x 10, x 100, x 1000, depending on patchpanel connections.)

Slave — permits operation of computer control circuitry from a second console.

Chapter 2 — OPERATION

2.1 *General Procedures*

A logical point to begin the procedures for operating an analog computer is with the computer problem diagram complete and ready to be patched. The subject matter leading up to this point, including principles of analog computation, applications of the computer, problem analysis, and programming techniques leading to the preparation of the patching diagram is adequately discussed in a number of common text books now available, some of which are listed below:

1. "Electronic Analog Computers" by Korn and Korn Second Edition, McGraw-Hill Book Company New York, 1956, 450 pages.
2. "Analog Computer Techniques" by Clarence L. Johnson, McGraw-Hill Book Company, New York, 1956, 264 pages.
3. "Analog Computation in Engineering Design" by Rogers and Connolly, McGraw-Hill Book Company, New York, 1960, 450 pages.
4. "Analog Computation" by Albert S. Jackson, McGraw-Hill Book Company, New York, 1960, 645 pages.
5. "Computer Handbook" by Korn and Huskey, McGraw-Hill Book Company, New York, 1961, 1288 pages.

In addition, "The Beginner's Software in Analog Computers for Education and Research" by Dr. Maxwell Gilliland is available from Systron-Donner. This book is especially valuable to the SD 10/20 user as it was written with Systron-Donner computers in mind.

2.2 *Symbols for Computing Components*

The symbols used for computing components in computer problem diagrams are shown on the following pages. These symbols have been proposed by the Simulation Council* and are used throughout this manual.

*Refer to "Uniform Graphics for Simulation" pp 137-140, "Simulation, March 1966"

Presenting...

Uniform graphics for *SIMULATION*

The symbols and the methods of laying out analog and hybrid computer diagrams presented here are advocated to alleviate the confusion caused by the uncoordinated invention of new symbols and diagramming practices. The increasing use of hybrid techniques and equipment has aggravated an already bad situation to the point that it is often no longer possible for one worker in our field to read another's diagram. Usually this is because symbols are devised and diagrams are drawn to include details peculiar to a particular kind of equipment. Such a wiring, or "patching," diagram is of course necessary for setting up and checking out an actual simulation, but hardware-peculiar details are only confusing to those with other kinds of equipment. With few exceptions, the use of a simplified signal-flow diagram to illustrate technical articles is much more effective.

With the foregoing in mind an SCi committee composed of

GEORGE BURGIN
JOE HUSSEY
HANS JORGENSEN
GRANINO KORN
JOHN McLEOD

selected the symbols and offers the following suggestions for their use. Primary considerations were current usage, clarity, and simplicity. We devised no new symbols and, unless there were overriding indications to the contrary, we adopted those already in widest use. Clarity and simplicity, we believe, will be enhanced by the choice of unique shapes to represent different components, and the elimination of all unnecessary details in diagrams.

There was no intent on the part of our committee to set up standards for the industry. However, all diagrams appearing in *SIMULATION* will be prepared according to the committee's recommendations (as they may be modified from time to time), and we hope that these recommendations will prove attractive to others. Suggestions for modifications and additions are solicited.

General rules

The following methods and symbols are recommended for the illustration of *technical articles* prepared for *publication*. Unless the purpose of the article is to describe the use of a particular kind of equipment, and the hardware details are pertinent to the subject, such illustrations should *not* be "hardware-peculiar." In other words, the objective should be to show signal flow, rather than "patching" details.

The primary, or overall, system diagram should show only the essential signal flow. Where it is necessary to show details, separate diagrams should be made and referenced to the primary diagram by enclosing the detailed area of the primary diagram in dotted lines with suitable notation.

The direction of signal flow should be indicated by arrowheads except where the shape of the symbols makes the direction of flow obvious. Primary signal flow (with the exception of feedback loops) should be from left to right, and, if practical, each "line" of symbols should be made to read like the mathematical relation it represents.

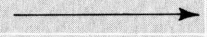
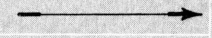
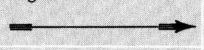
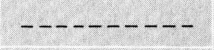
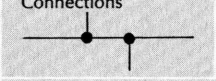
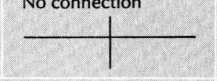
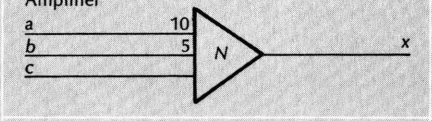
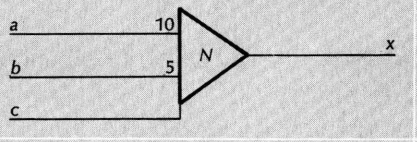
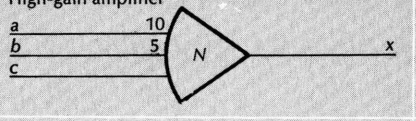
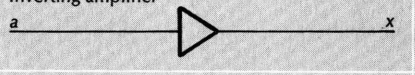
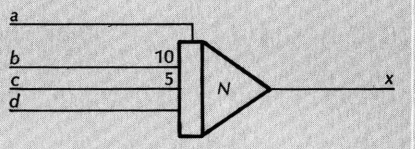
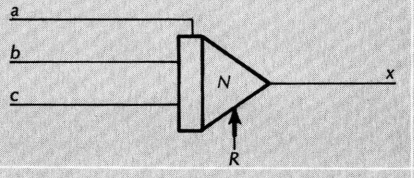
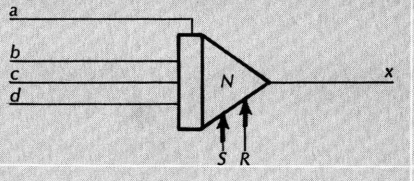
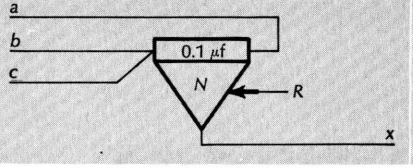
The choice of whether to end a line and label it (preferably with the symbol of the variable that the signal represents) when it reaches the right-hand side of the diagram, and then indicate its continuation with the same label as it enters again at the left-hand side, instead of drawing in the connection, should be made on the basis of clarity; if a line returning the signal from right to left will cross many other lines and be hard to follow, it should not be drawn in.

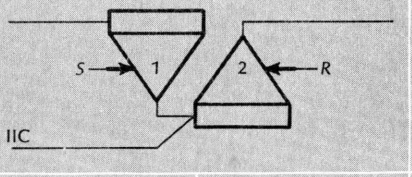
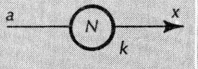
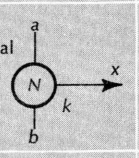
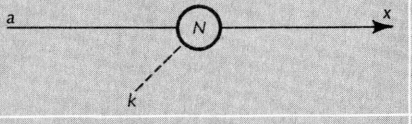
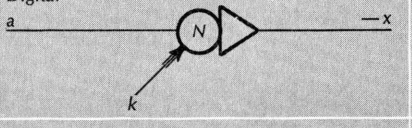
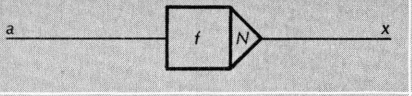
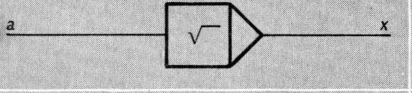
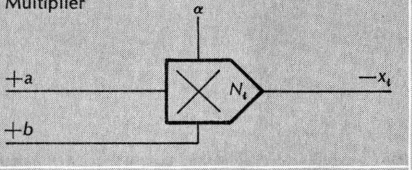
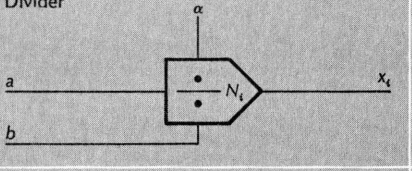
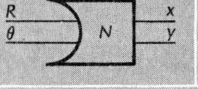
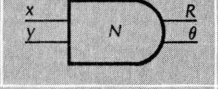
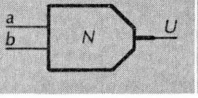
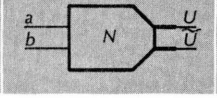
If a diagram involves a number of identical circuits, only one should be shown in detail, while the others should be indicated by boxes with appropriate notation.

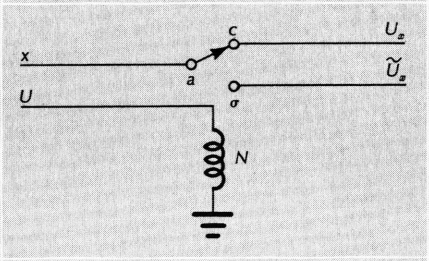
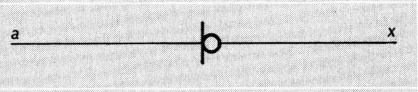
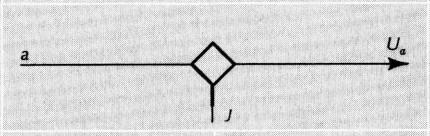
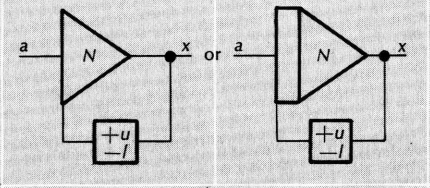
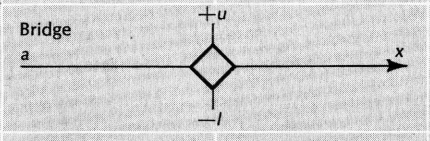
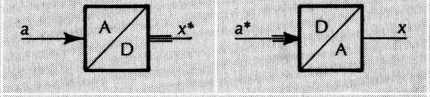
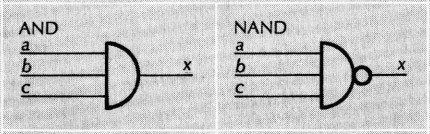
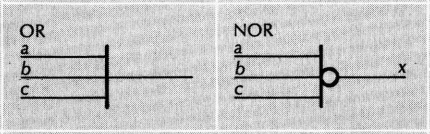
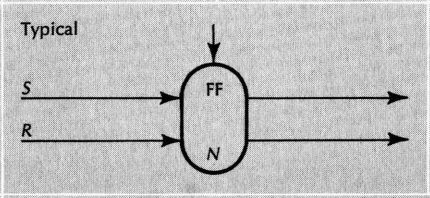
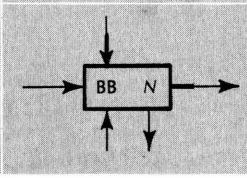
Components should not be numbered unless they are referred to by number in the text.

All amplifier gains should be shown just outside the amplifier at the point where the input enters. Unity gains should not be labeled.

Always apply the test of clarity and simplicity. Ask yourself: "Is this the most understandable way to diagram this *for those unfamiliar with the hardware, and less familiar with the subject, than I?*"

ELEMENT	SYMBOL	FUNCTION	NOTES
Signal flow	Analog  Binary  Digital word  Mechanical  Connections  No connection 		Distinction as to kind of signal is made only at beginning and end of line, and then only where there are two or more kinds of signals to be shown on one diagram. Arrowheads should be omitted only if direction of signal flow is obvious.
Summers	Amplifier 	$x = -(10a + 5b + c)$	No arrows; shape clearly indicates direction of flow. No label on unity-gain input. "N" indicates where number of amplifier should be placed if, *and only if*, referred to in text.
	Summing amplifier (with high-gain input) 	$x = -(10a + 5b + \mu c)$	Label high-gain input "SI" or "G" only if pertinent; the point at which c enters (at top or bottom of symbol) indicates a gain of μ.
	High-gain amplifier 	$x = -\mu(10a + 5b + c)$	Note that the numbers at the inputs are now only relative gains; μ, an unspecified large number which is a function of the particular amplifier, is the overall gain.
	Inverting amplifier 	$x = -a$	When amplifiers are used *only* to change signal sign they should be smaller. Orientation should be that which makes for greatest graphical simplicity, *i.e.*, they may be shown in vertical, or in feedback, paths.
Integrators	Standard 	$x = -a - \int_0^t (10b + 5c + d)dt$	Standard integrator mode is that of basic problem. The point at which a enters (at top *or* bottom of symbol) indicates that it sets the initial value of x, so it is redundant to label it IC.
	Two-mode 	RESET when $R = 1$ COMPUTE when $R = 0$	Arrows indicating mode control should be shown only when two or more integrators are operating in different modes simultaneously. The mode-control input should then be labeled or coded to indicate the controlling mode.
	Three-mode 	RESET when $R = 1$ or $R = S = 1$ HOLD when $S = 1, R = 0$ COMPUTE when $R = S = 0$	
	Track-hold 	TRACK when $R = 1$ HOLD when $R = 0$	When used in this way the size of the integrating capacitor may be important, as it affects the tracking lag. In such cases the value should be indicated as shown. The quantity tracked or held is $-(a + b + c)$.

ELEMENT	SYMBOL	FUNCTION	NOTES
Integrators (continued)	Memory pair 	Integrator 1 in Track for $S=1$ Integrator 2 in Track for $R=1$	Integrator 1 in TRACK for $S=1$, integrator 2 is TRACK for $R=1$. In certain iterative problems y is required to have some value for the first iteration; thus an "initial" initial condition must be furnished as shown.
Potentiometers	Two-terminal  Three-terminal 	$x=ka$ (load connected) $a=1, b=0$ (load connected)	The mathematical relationship shown for the three-terminal pot is given only to define k. It will not usually hold during problem solution because if b were always zero a two-terminal pot could be used. If it is desirable to define k in any other way, its meaning should be clearly indicated.
	Servo-set 	$x=ka$	This should be used only if the fact that N is servo-set is significant to the solution of the problem, as, for instance, when it must be automatically reset after each run of an iterative problem.
	Digital 	$x=k*a$	As shown, the symbol indicates a digital pot with integral (committed) inverting amplifier. The symbol for non-inverting digital pots should not include the amplifier. *Indicates quantized value.
Function generators	Arbitary 	$x=f(a)$	The number N should be used only when the function generator is referred to by number in the text, *or* when it is desirable to explain what the function f is, either by a footnote, or by a separate graph.
	Mathematical functions (typical) 	$x=\sqrt{a}$	In cases where the function generated can be represented by a standard mathematical symbol, the f should be replaced by the symbol.
	Multiplier 	$x=\frac{ab}{\alpha}$ $x=\frac{\alpha a}{b}$ $\alpha=$ reference voltage	These symbols should be used for all analog multipliers and dividers; if the *kind* is significant to the solution of the problem, it should be so stated in the text and/or noted on the diagram. Because equipment differs, the sign of the output for specified signs of both inputs should be given, otherwise inversion will be assumed. The number N should be used only if the component is referenced in the text, *or* if more than one channel of a multichannel device is used. In the latter case the subscript, in this case i, identifies the channel. In many cases, it will be found that a drawing can be simplified and clarified by drawing the same multichannel device in more than one signal flow path. In this case the number would be the same, but the subscript would be different for each channel.
	Divider 		
	Resolvers Polar to rectangular  Rectangular to polar 	$x=R\cos\theta$ $y=R\sin\theta$ $\theta=\arctan y/x$ $R=\sqrt{x^2+y^2}$	If a resolver has additional outputs they should be shown only if used.
	Comparators With binary output  With true and false binary outputs 	$U=1\ (a<b)$ $U=0\ (a>b)$ $\bar{U}\neq U$	The symbol for a relay comparator can, of course, be made by combining either of these symbols with that of a relay.

ELEMENT	SYMBOL	FUNCTION	NOTES
Relay		$U_x = x \quad (U=0)$ $\tilde{U}_x = x \quad (U=1)$	If the diagram is drawn as shown, the designations of arms and contacts are superfluous. However, it is often desirable, for clarity, to show the relay coil in one place on a diagram and the contacts in signal-flow paths elsewhere. In this case, N_{oa} would designate the normally Open ($U=0$) contact of channel a, relay N; N_{aa} the Arm of channel a of relay N, etc.
Digital inverter		$x = \tilde{a}$	The tilde ($\sim$) is used instead of a bar to indicate negation. This is recommended because of the many other meanings of a bar over a variable.
Digital/analog switch		$U_a = a \quad (U=1)$	ON when binary signal, U, is digital "one."
Limiters	Feed-back 	$x = -a \quad (l < a < u)$ $x = -l \quad (a < l)$ $x = -u \quad (a > u)$	u = larger value at which output is limited l = smaller value at which output is limited
	Bridge 	$x = a \quad (l < a < u)$ $x = l \quad (a < l)$ $x = u \quad (a > u)$	
Converters	Analog-to-digital Digital-to-analog 	$x^* = a$ $x = a^*$	*Indicates quantized value.
Diode	Solid state 	$x = a \quad (a > x)$ $x = 0 \quad (a < x)$	
Diode gates	AND NAND 	AND $x = a \cdot b \cdot c$	Output is high (logic 1) if and only if all inputs are high.
		NAND $x \neq a \cdot b \cdot c$	Output is low (logic 0) if and only if all inputs are high.
	OR NOR 	OR $x = a + b + c$	Output is high (logic 1) if and only if at least one input is high (*i.e.*, any or all of the inputs are high).
		NOR $x \neq a + b + c$	Output is low (logic 0) if and only if at least one input is high (*i.e.*, any or all of the inputs are high).
Flip-flop	Typical 		As there are many kinds of flip-flops, symbolic representation of the operation of any but the simplest is not advised; if the operation is not obvious, an explanation in the text or a footnote with the diagram is recommended.
Black box		This is Black Box number N, to be used if no symbol is given here, *or in case of doubt!* It can have any number of inputs and outputs, but the nature of the signals should be indicated and all signal-flow directions should be designated by arrowheads. Here there are three analog inputs giving rise to one analog and one binary output.	The function of a "black box" can often be made obvious by properly labeling the inputs and outputs. However, if it is not obvious, the function should be explained in the text or by a footnote with the diagram. If internal details are of interest, they should be shown in an appropriately labeled auxiliary diagram.

2.3 *Alternate Symbols*

Conventional rectangular blocks may be used in place of the foregoing symbols when they are identified by the following abbreviations (proposed IEEE standards):

A	Amplifier	LIM	Limiter
ADC	Analog-to-digital converter	P	Potentiometer
		PB	Plotting Board
DAC	Digital-to-analog-converter	REC	Recorder
		REF	Reference voltage
DVM	Digital voltmeter	SA	Servo amplifier
EM	Electronic Multiplier	SM	Servomultiplier
EXT	External connections or trunk	SR	Servo resolver
		RA	Relay amplifier
FG	Function generator	REL	Relay
IC	Initial Condition	SW	Switch
INT	Integrator	TD	Time delay

We strongly urge that the circuit symbol format be used when working with the SD 10/20. The problem board of the SD 10/20 has been carefully designed to conform to circuit symbolism as closely as is possible. This type of problem board attempts to match the problem diagram and thus facilitate placing the problem on the computer. The discussions that follow are, as far as is possible, limited to operating procedures only. A careful reading of these procedures coupled with practice on the computer will enable the operator to quickly familiarize himself with the machine and proceed to problem solving.

2.4 *Operating Modes*

The Analog computer has four basic modes of operation: Reset, (or Initial Condition) Compute, Hold and Rep-OP (Repetitive Operation) and several auxiliary or convenience modes of operation. In the SD 10/20, operating modes are activated by pressing the appropriate push-button switch on the control center. Each switch is clearly marked by function or mode and is illuminated when engaged. The following list briefly describes each mode of operation.

HOLD – Opens a relay between the junction and summing junction on all integrator amplifiers, thus holding computer solution.

COMPUTE – Closes a relay between the junction and summing junction on all integrator amplifiers. Simultaneously opens the Reset (IC) relay. Allows computation to begin.

RESET – Closes Reset, opens Hold relays allowing Initial Condition voltages to be placed on all integrators.

REP-OP – Automatically switches computer between Reset and Compute modes of operation. Solves problem repetitively.

BAL/POT SET – Converts all amplifiers to gain of 2500 for accurate monitoring and adjustment of junction offset. Grounds summing junction of Models 3320, 3321, 3322A, and 3325 to allow potentiometer setting under load conditions. Also grounds IJ of Model 3329.

POWER/ON-OFF – Turns all power supply voltages, except +28V relay and oven supply, on and off.

OVEN – On whenever +28V relay and oven supply is on.

O. L. HOLD – Blinking light indicates when an overload has occurred.

O. L. RESET – When engaged automatically switches computer to Hold mode when an Overload occurs. When overload is removed the button must be pressed to clear the overload circuitry.

TIME SCALE – Selects between integrator capacitors patched to A and B terminals on the integrator patch board.

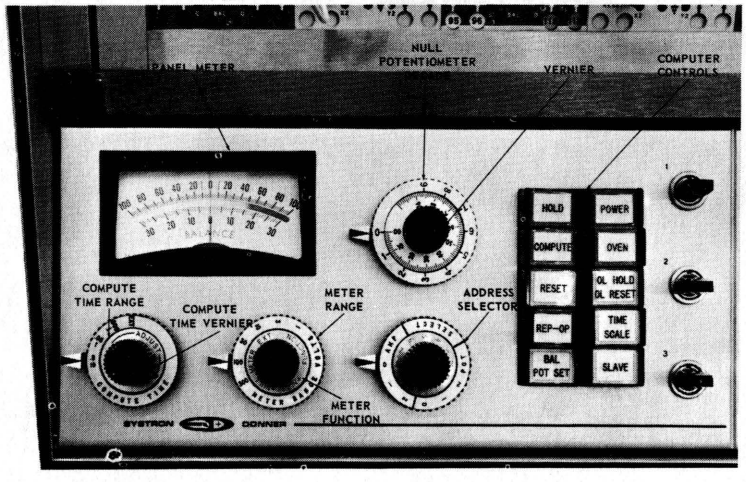


Figure 2: Control Panel, Model SD 10/20

2.5 *Computer Logic*

Each operating mode switch energizes a logic buss which is then distributed to the logic relays in the computing modules (primarily to the integrators). The logic levels in the Analog sections of the computer are:

+28V = True = logical 1
0V = False = logical 0

A logical one energizes a buss and places the computer in that mode of operation. All contradictory modes have their switches mechanically interlocked to prevent two modes of operation from being energized at the same time.

The table that follows outlines the logic busses and operating modes.

In most cases the nomenclature for each logic buss is self-explanatory. The following explanations should clarify the remainder of the logic nomenclature.

Logic Buss	Description
F. R. (R. O.)	Forward Reset (Repetitive Operation). This is the normal Reset buss and also is the Reset buss energized in the reset portion of Repetitive operation.
R. R. (R. O.)	Reverse Reset (Repetitive Operation). This buss is the logical complement of forward reset. It is used for complementory integrators and track/store circuits in iterative computation. Energized in the Compute mode of operation and in the Compute portion of Rep-Op.
F. R. (R. T.)	Forward Reset (Real Time). This buss is used to reset non-repetitive operation integrators. It is energized only when the reset switch is engaged.
F. H.	Forward Hold is the normal Hold buss. It is energized in the Hold mode of operation or if an overload occurs when the Overload Hold switch is engaged.
R. H.	Reverse Hold. Reverse Hold is the logical complement of F.R.R.T. It is used for complementary integrators and Track/Store circuits in iterative computation. Energized in the compute mode of operation and in Rep-Op.

NOTES to Table 1:

(1) Blank indicates either 0 or +28 exists.
(2) All modes actuated by pushbutton switch on Logic Control Panel except Problem Hold & Overload initiation.
(3) Problem Hold is actuated by application of +20v to +100v to Problem Hold Trunkline on Problem Board.
(4) O. L. Hold is actuated by operation of "O. L. HOLD" switch followed by either a temporary or permanent O. L. condition at any amplifier in the computer.

The Test Points (TP) referred to in the Control Logic Table are located at the rear of the computer on the Control Logic board. The test points are numbered consecutively from the bottom, with the bottom (black) test point a ground point. *All test points except the bottom one must never be grounded or damage will result.*

Table 1. SD 10/20 Control Logic Table Operating Mode

LOGIC BUSS	POT-SET BALANCE	RESET	COMPUTE	REP-OP	HOLD	PROBLEM HOLD	O.L.HOLD O.L. RESET	TIME SCALE CHANGE
Bal Buss (TP 4)	+28	0	0	0	0			
Pot-Set Buss (TP 4)	+28	0	0	0	0			
F.R.(R.O.) Buss (TP6)	0	+28	0	0, +28	0			
R.R.(R.O.) Buss (TP8)	0	0	+28	+28, 0	0	0	0	
F.R. (R.T.) Buss (TP 2)	0	+28	0	0	0			
F.H. Buss (TP 7) (Problem Hold Off)	0	0	0	0	+28	+28	+28	
R.H. Buss (TP3)	0	0	+28	+28	0			
Time Scale Change Buss (TP 5)								+28

2.6 *Controls*

There are four control dials located on the front panel of the SD 10 20. These are all dual types with an outer dial and a concentric inner dial. The function of each is explained below.

Null Potentiometer: This control is a decade potentiometer. The outer dial is calibrated in 10 volt steps with the inner dial continously variable from 0 to 10 volts. Used with the + or – null position of the **meter select control** to convert the panel meter to a .02% Null Voltmeter. The potentiometer arm is fused at 1/32 amp to protect it from accidental damage.

Address Select Control: The outer dial of this switch selects either an amplifier output or the arm of a potentiometer; it also selects the ten's digit of the address. The inner dial selects the units digit of the address. As an instance to select the output of Amplifier 8, turn the outer dial to the AMP section, position 0 and the inner dial to position 8. The address selected is automatically. connected to the input of the meter.

Meter Select Control: The outer dial selects the Meter Range or relative null sensitivity and is marked for full scale voltage in each range. The ranges available are 1v, 3v, 10v, 30v, 100v, and 300v. Accuracy is 3% of full scale. The inner dial selects the mode of operation for the meter. in the METER position circuitry is connected for normal voltmeter operation; the selected address is automatically connected to the meter circuit. In the EXT position the selected address is connected to the EXT jack located on the left side of the computer, the meter input is connected to the M jack on the problem board. In the + and – Null positions, the arm of the reference potentiometer is connected to one side of the meter and the selected address is connected to the other side of the meter.

Compute Time Control: The outer dial selects one of the three ranges of time for the compute portion of Rep-Op. The ranges are 10 sec to 0.5 sec, 1 sec to 0.05 sec, and 0.1 sec to 0.005 sec. The fourth position of the dial is external (EXT) which allows external circuitry to drive the Rep-Op mode of the computer. The inner dial provides a vernier adjustment for each of the ranges. (Note that Reset time is a fixed fraction of the decade compute setting.)

2.7 *Computing Modules*

The instructions that follow detail the operating procedures for each of the computing modules. It is recommended that this portion of the manual be read and understood before actually using the Model SD 10/20. It is for this reason that the actual turn-on and detailed operating procedures follow this section of the manual.

A few general procedures should be borne in mind when patching a problem on the computer. While none of these procedures are mandatory, they will facilitate patching and help eliminate patching errors.

a. Patch each computing module into the desired configuration, then interconnect the module into the problem layout.
b. Use the single and double shunt plugs as much as possible so as to reduce the number of patch cords on the board.
c. Use the squid patchcords as much as possible. Again, this will reduce the number of patchcords.
d. When patching in a reference voltage, always patch from the connection to the voltage. This will prevent grounding the reference voltages to the problem board or computer chassis. (As a general rule patch the cold end first and remove it last.)
e. Always patch a feedback resistor or shunt around all unused amplifiers. This will prevent them from drifting into saturation.

WARNING

Dangerous voltages are present on the problem board. Use caution to avoid electrical shock.

2.8 *Operational Amplifiers (General)*

Basic Equations: The operational amplifier is a high gain DC amplifier employed in a negative feedback type circuit. Its primary uses in the computer are for integrating, summing and inverting operations. The following figure shows the connections as an inverting amplifier.

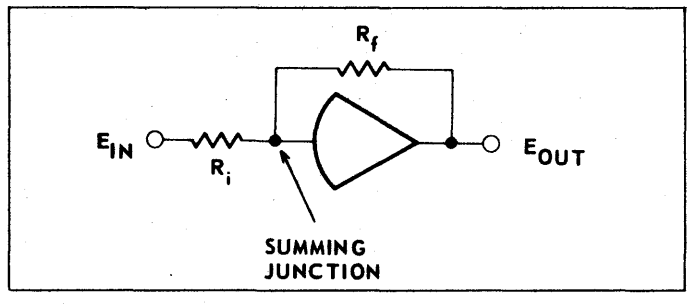


Figure 3. Basic Inverting Amplifier Circuit

In this closed-loop configuration, the characteristic high gain of the amplifier tends to cancel out whatever voltage may appear at the summing junction by means of the negative feedback through the resistor R_f. The summing junction is effectively at 0V and virtually no input current flows through the amplifier input terminal. Under these conditions, the following equations for the amplifier can be written:

Equation (3) states that the gain of the amplifier for input E_i is equal to the feedback ratio R_f/R_i. Note also that the output voltage is always opposite in polarity to the input voltage. The summing amplifier is a special case with multiple inputs where:

$$E_o = -\left(\frac{R_f E_1}{R_1} + \frac{R_f E_2}{R_2} + \frac{R_f E_3}{R_3}\right)$$

In this case, the gain of the individual inputs is controlled by the gain of the individual feedback-to-input resistor ratios.

When the feedback resistor is replaced by a capacitor, the expression for the output voltage becomes:

$$E_o = \frac{1}{C}\int i_i dt$$

(1) $i_{in} = -i_{out}$ or (2) $\frac{E_i}{R_i} = \frac{-E_o}{R_f}$

or (3) $E_o = \frac{-R_f}{R_i} \cdot E_i$

Substituting $i_i = \frac{-E_i}{R_i}$, we get: $E_o = \frac{-1}{R_i C}\int E_i dt$

where $\frac{1}{R_i C}$ is the integrator gain.

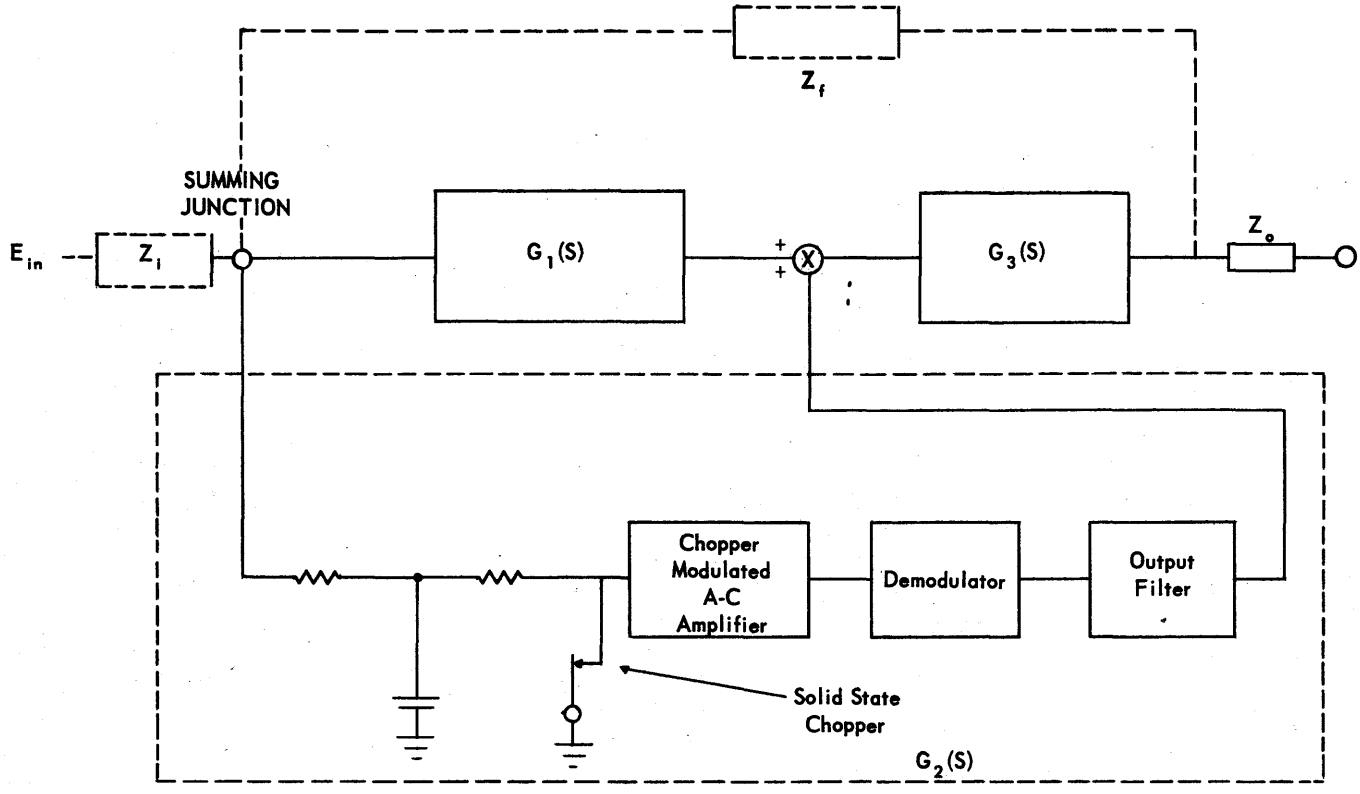
High-Gain Amplifier/Saturation. One other basic circuit configuration should be considered: the high gain amplifier. In comparator circuits, for example, the amplifier is used open-loop (no feedback resistor) to drive a relay or electronic switch. In this type of circuit, the high amplifier gain amplifies whatever voltage appears at the summing junction by a factor of more than 10^7 (for the Model 3310 amplifiers in the SD 10/20 Computer). Effectively, a signal of less than a millivolt at the summing junction will cause the output of the amplifier to swing almost instantly to its maximum voltage level and trigger the relay or switch. When this happens, the amplifier is said to saturate and may not immediately respond to a change of input signal. To prevent saturation, a diode limiting circuit is connected which limits the output voltage swing to the normal computing range of ±100V or less.

When an amplifier is left in the open-loop, it tends to drift immediately into saturation, even with no input voltage applied. For this reason, idle amplifiers should have a feedback resistor connected between their junctions and output terminals.

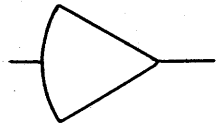
Amplifier Overload. Overload is synonymous with "saturation" as applied to the computing amplifier. Normally, all input voltages in a computer problem are scaled down so that the output of any amplifier never exceeds ±100V, which assures that an amplifier will not go into saturation. (The amplifier is actually capable of at least a +105V output with 1 ma load current without overload.) To assure a full +100V range without overloading, it should not be expected to furnish more than 25 ma of current to the loading circuits. (In normal operation, seldom more than a few milliamperes of current are drawn from the amplifier output.) A single 100K-ohm input resistor to the following amplifier will draw 1 ma at +100V; a coefficient potentiometer will draw 3⅓ ma at the same voltage.

When the amplifier exceeds the limit of its operating voltage and current range, it will not be able to perform linearly. The equations previously stated will no longer hold true. When this happens, the amplifier summing junction voltage begins to rise above the virtual 0V level and causes the overload indicators to operate, indicating a true overload.

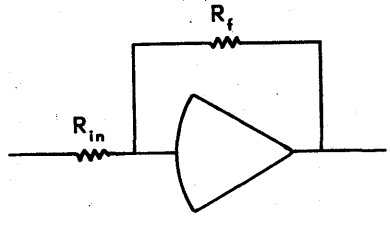
Amplifier Balance. For accurate computation, the inverting amplifier output voltage must be 0 volts when the input voltage is 0 volts. All computing amplifiers are subject to internal drift which will produce an undesirable offset voltage at the output over a long period of time. The fact that the amplifiers are chopper-stabilized minimizes this offset. In addition, the amplifier has an external balance adjustment which provides a compensating DC bias to cancel the offset error.



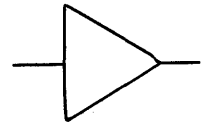
BLOCK DIAGRAM OF A TYPICAL CHOPPER STABILIZED D-C AMPLIFIER



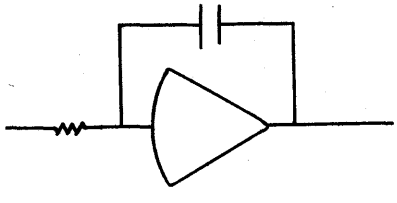
HIGH GAIN AMPLIFIER SYMBOL



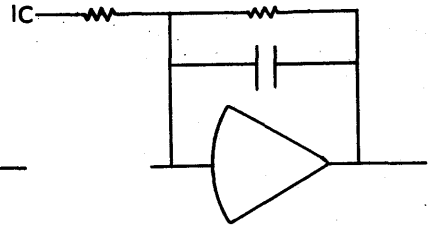
INVERTER SCHEMATIC



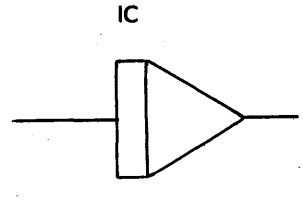
INVERTER SYMBOL



INTEGRATOR IN COMPUTE MODE



INTEGRATOR IN RESET MODE



INTEGRATOR SYMBOL

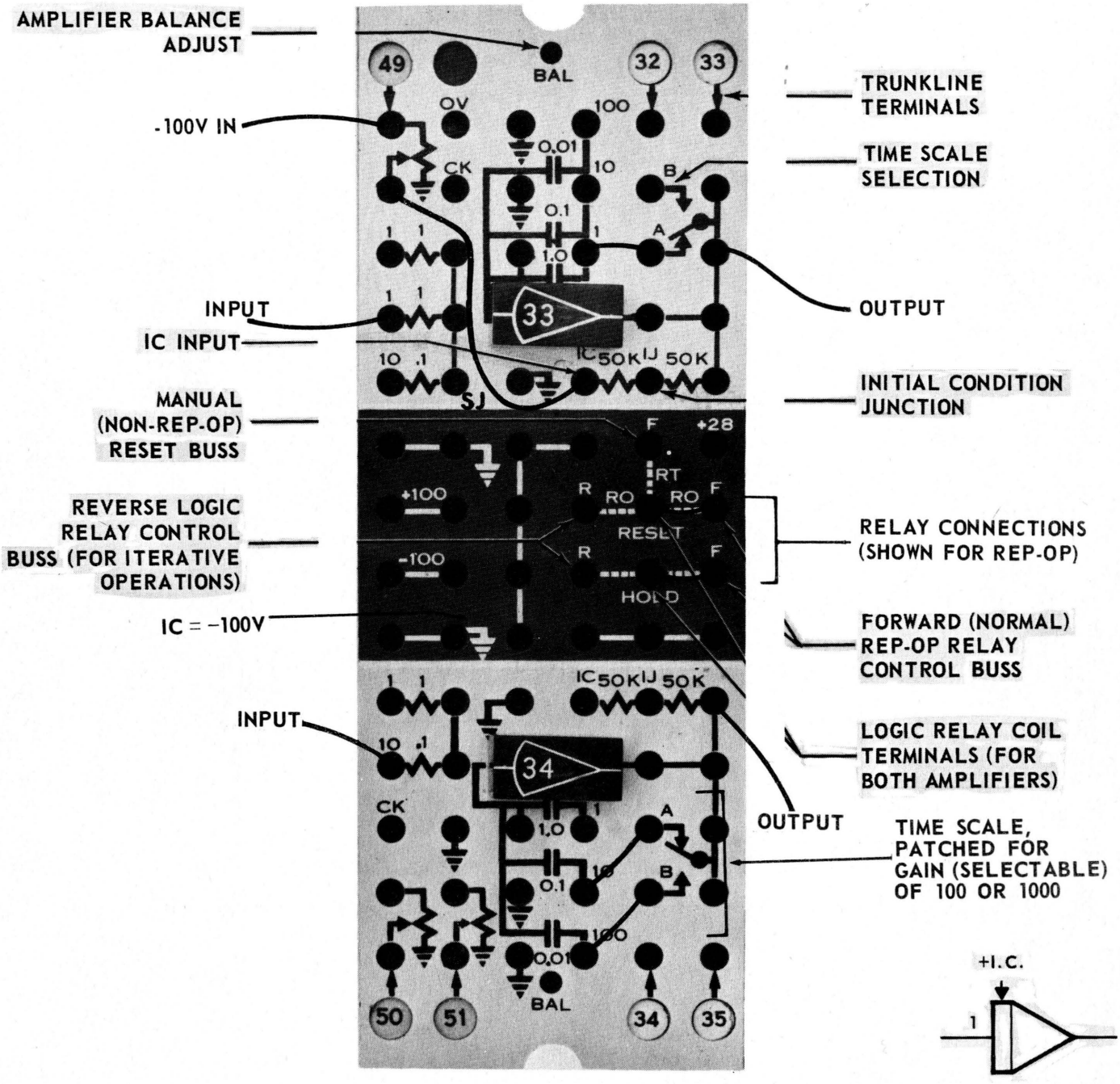


Figure 4. MODEL 3320 DUAL INTEGRATOR (WITH PATCHING SHOWN FOR BASIC CIRCUIT)

2.9 *Model 3320, Dual Integrator*

The Model 3320 is divided into three sections: the top and bottom integrators and a logic section common to both. Basic patching of the integrator requires only a patch from the end of the integrating capacitor to the A terminal of the time scale relay. By patching the end of another capacitor to the B terminal a second time scale is set up and is controllable by the TIME SCALE switch on the control panel.

Initial conditions (IC) are applied at the IC terminal. The source of the IC voltage may be a pot, amplifier output, the reference voltage, or from an external source.

The logic section consists of a 7-terminal matrix near the center of the patching block. The nomenclature is the same as that explained in the Logic Control section of this manual. The two center terminals of the matrix are connected to the coils of the Reset and Hold relays. For normal and repetitive operation, patch from the F (forward) terminals to the relay coils. For reverse and iterative operation, patch from the R (reverse) terminals to the relay coils. For nonrepetitive operation, patch from the F(RT) terminal to the reset relay coil. (In this mode the integrators will reset ONLY when the reset button in the control panel is pushed.) Note that the logic patching controls both integrators in this module.

To use the integrator as a summer, patch from the input side of one of the resistors to the output of the integrator. This will connect a resistive feedback around the amplifier; the other resistors may be used as summer inputs.

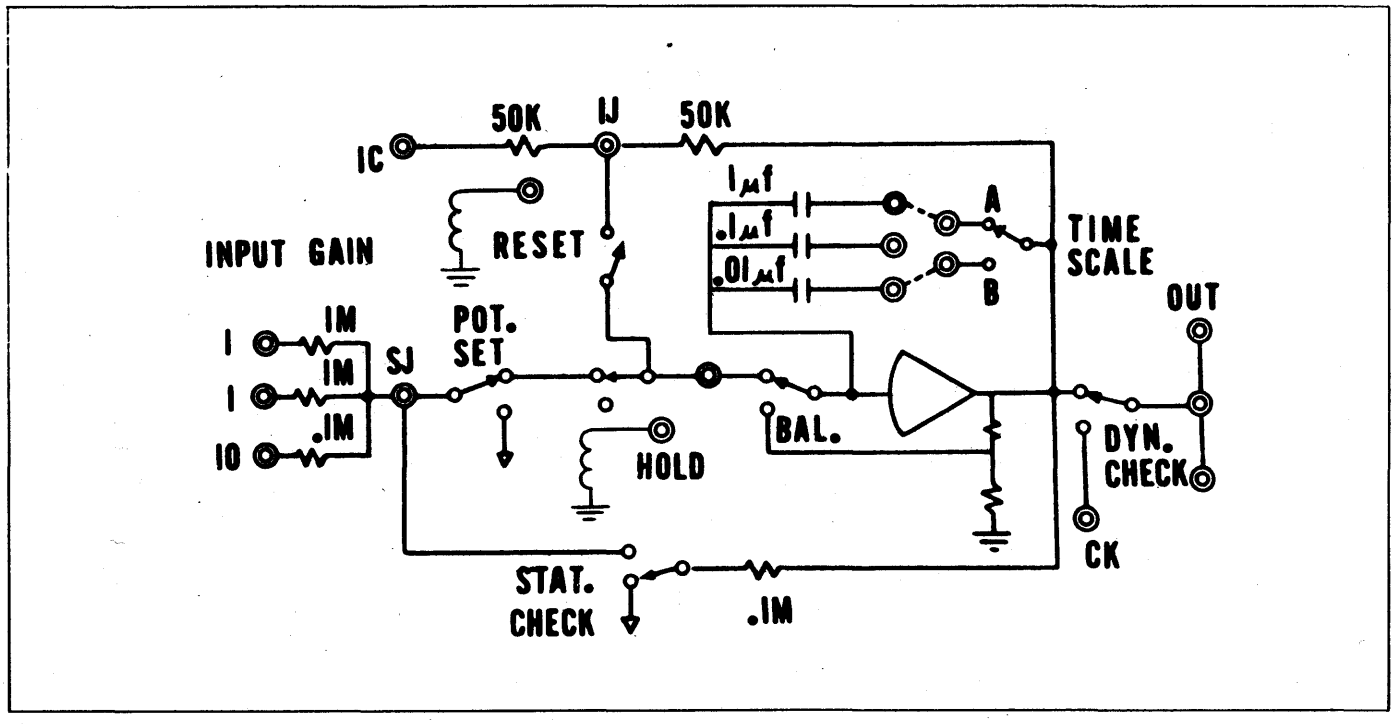


Figure 5. Integrator Block Diagram

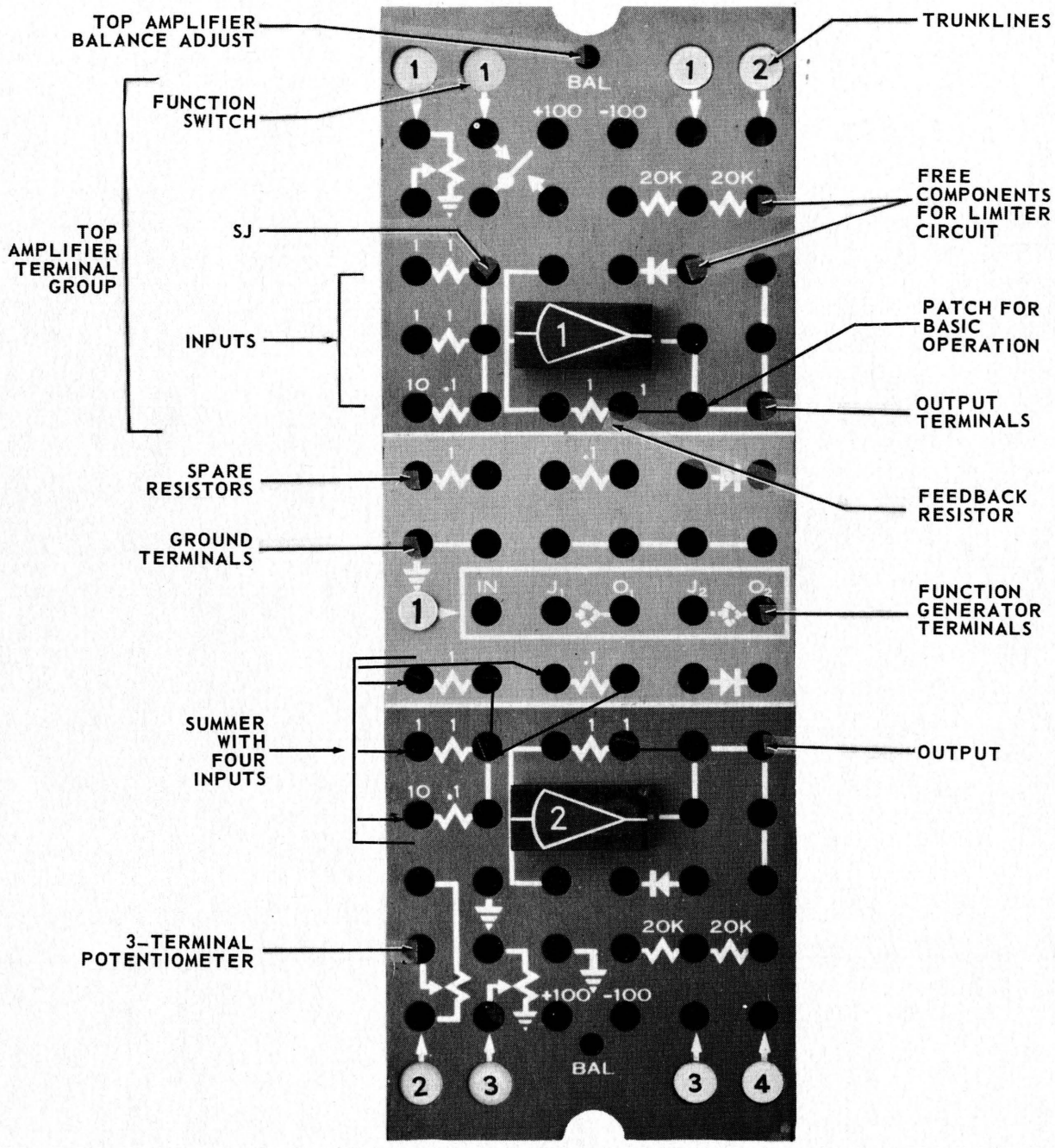


Figure 6. DUAL SUMMING AMPLIFIER MODEL 3321

2.10 *Model 3321 – Dual Summer*

The Model 3321 contains two operational amplifiers and the components necessary for summing operations. Basic patching consists of connecting one end of the feedback resistor to the output. The top summer has three input resistors, the bottom summer two input resistors. There are four spare summing resistors located in the center section of the module which may be used as either input or feedback resistors with either of the summers.

The module also has two 20 kilohm resistors and two uncommitted diodes associated with each summer. These may be used to patch the summer as a limiter-comparator or for any of the common diode circuits used in computation.

A function switch termination is provided on each summer module. The function switch is a single pole-double throw type switch and is physically located near the control center. Normally only the first three summing modules will have switches terminated in them.

The center section of the summing module has termination for a diode function generator. Use of these terminations and of the diode function generator is explained in that section of this manual.

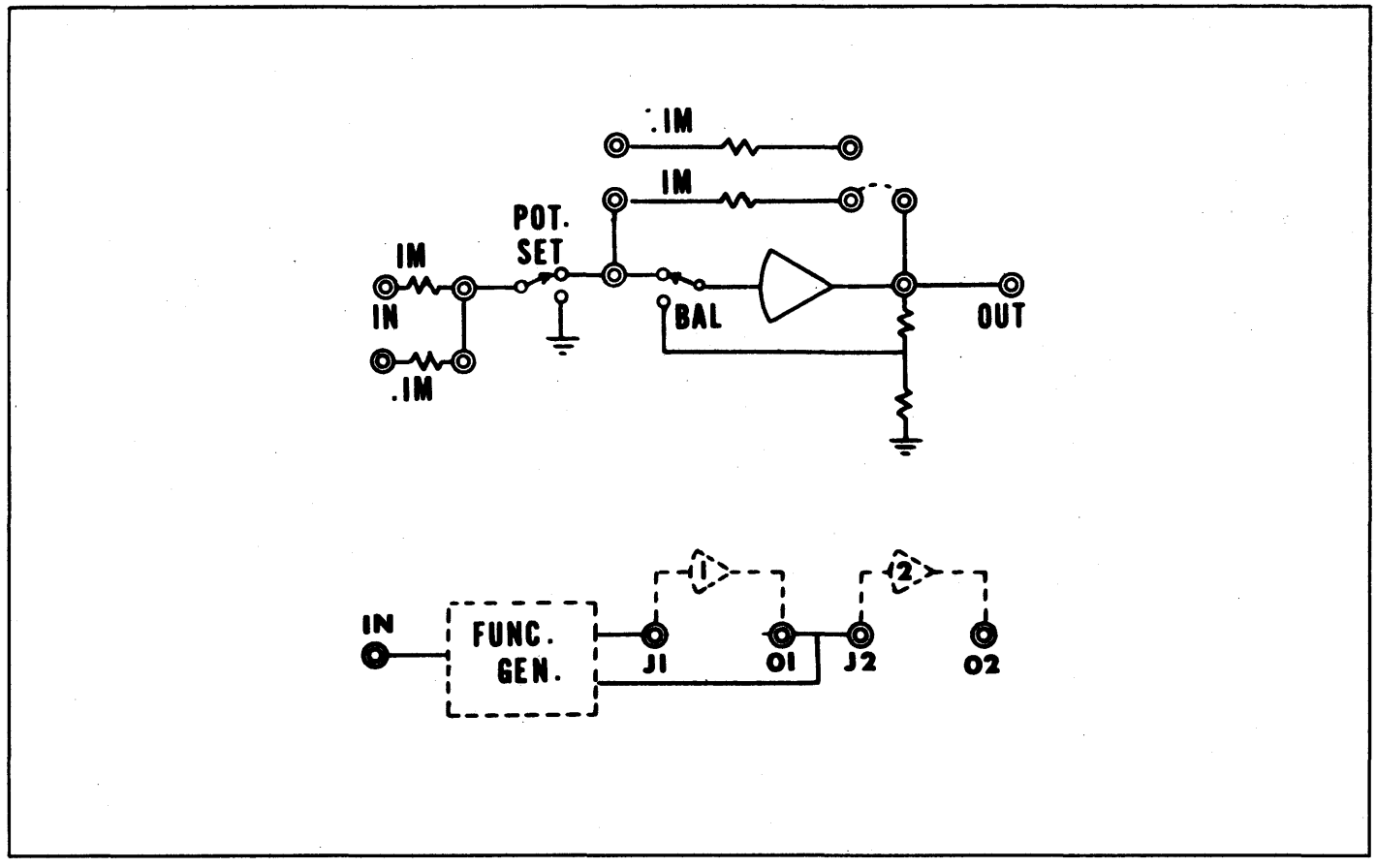


Figure 7: Summer Block Diagram

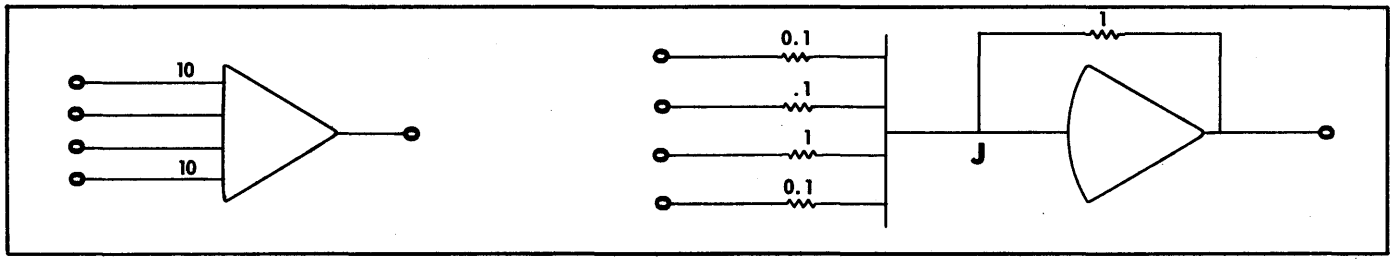


Figure 8: Notation for Four Input Summer shown in Patching Illustration

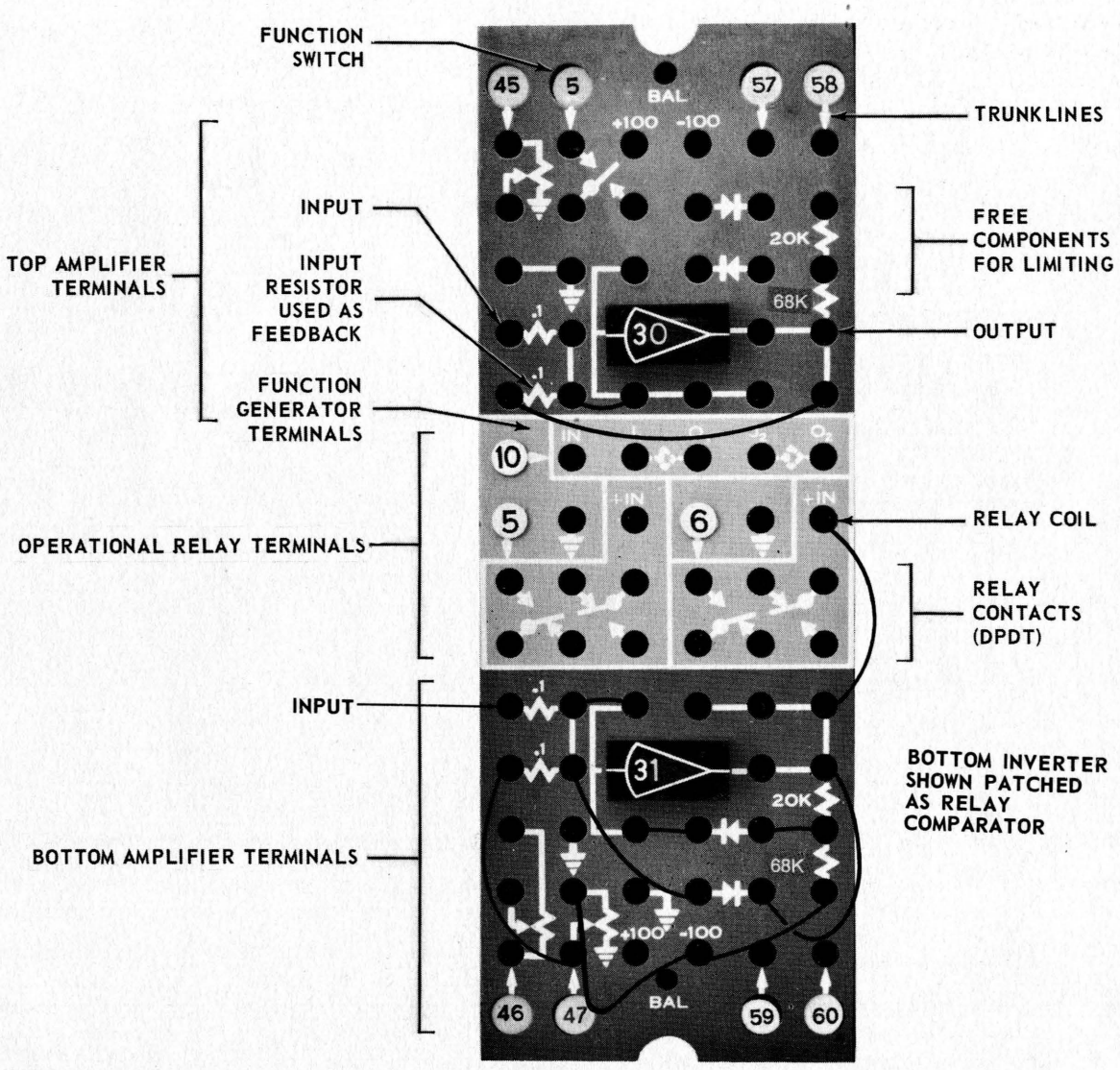


Figure 9. DUAL INVERTER, MODEL 3322 (WITH INVERTER CONNECTIONS SHOWN)

2.11 *Model 3322A – Dual Inverter, Dual Function Relay*

The Dual Inverter contains two operational amplifiers for use as inverters or high gain amplifiers in comparator and limiter circuits. Operation as an inverter requires two patches: (1) From the summing junction to the junction. (2) From the input side of one of the resistors to the amplifier output. The inverter may be used as a summer by patching additional resistors into the summing junction. (Note: Potentiometers used as inputs to the Model 3322A should be set in the Reset mode of operation.)

The Model 3322A also contains two function relays. Each is a two form C (2FC) relay corresponding to a double pole-double throw (DPDT) switch. The relays may be energized by any voltage from +28 volts to +100 volts. The energizing source is typically the output of an amplifier or a logic signal, but any source within the +28 volt to +100 volt range will energize the relays. Any voltage in the range plus and minus 100 may be applied without damage.

As in the Dual Summer, the Dual Inverter contains uncommitted diodes, limiter resistors, terminations for a Function Switch and Diode Function Generator terminations. The use and operation of these elements is the same as that described in the section on the Model 3321.

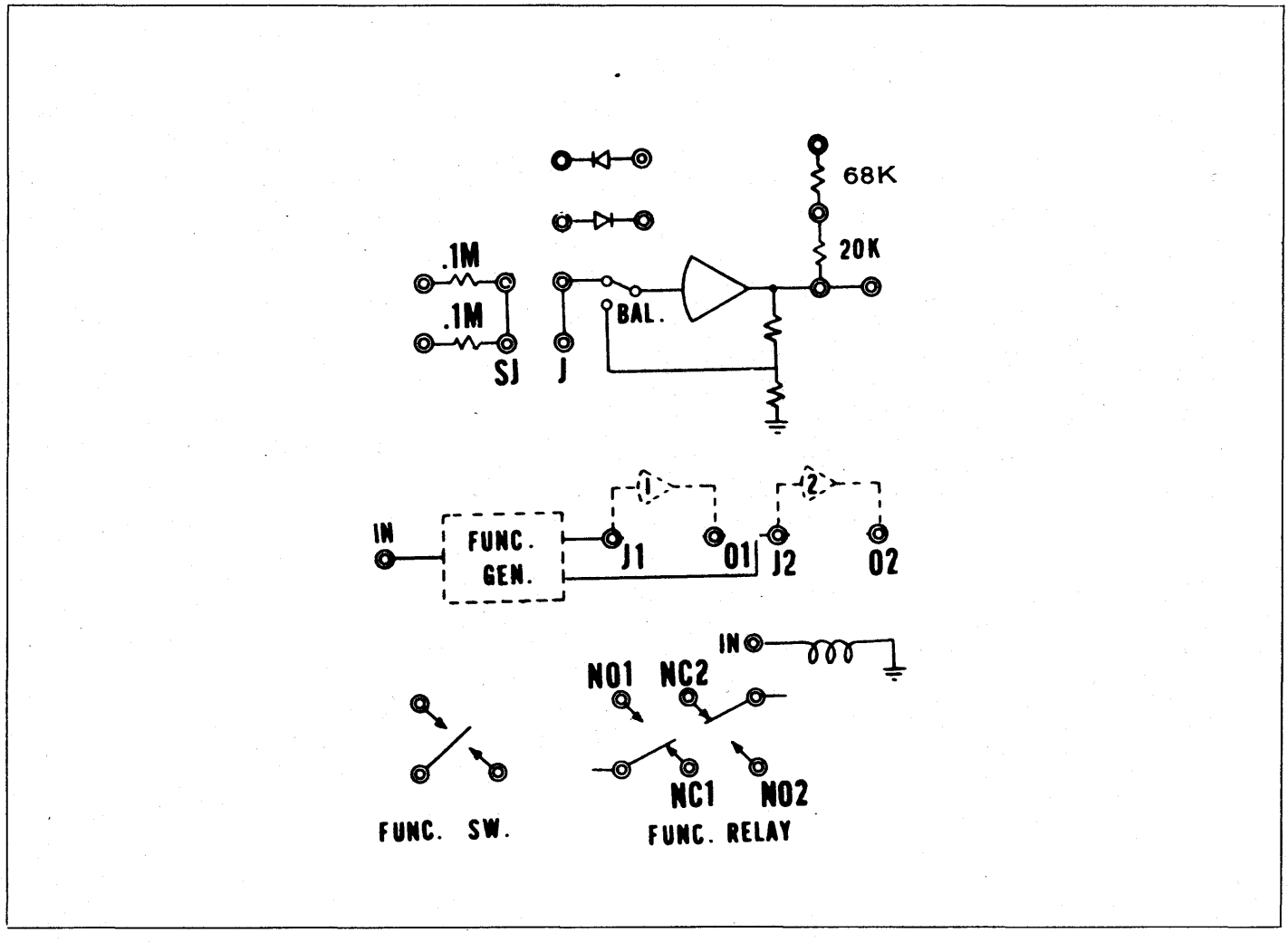


Figure 10. Inverter Block Diagram

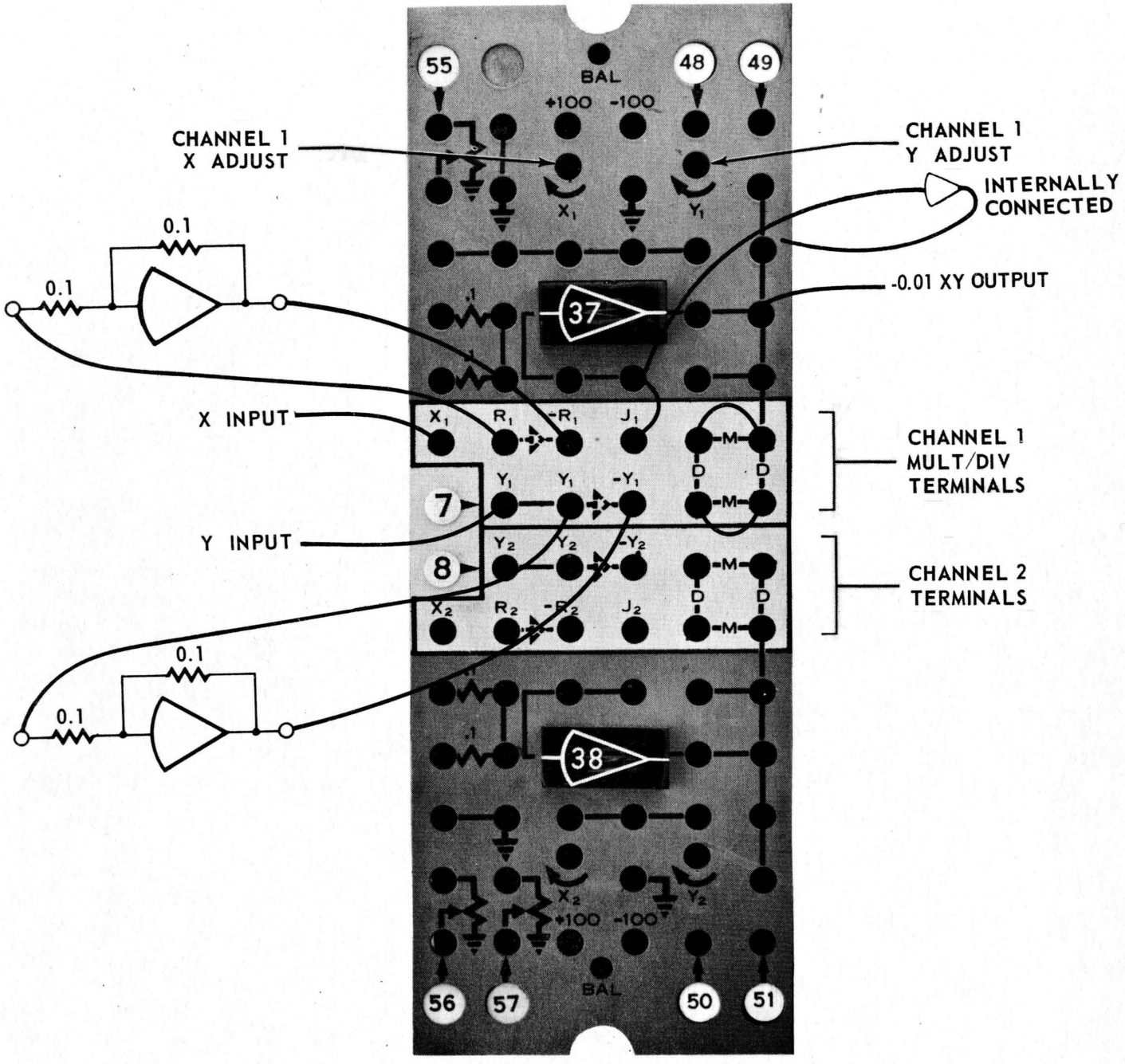


Figure 11. DUAL INVERTER AND DUAL MULTIPLIER/DIVIDER, MODEL 3323 (SHOWING CONNECTIONS FOR MULTIPLICATION)

2.12 *Model 3323 – Dual Inverter, Dual Multiplier*

The Inverter sections of the Model 3323 are similar to those described for the Model 3322A. The two basic patches required for inverter operation are: From the summing junction to the junction and from the input side of one of the resistors to the output of the amplifier.

The center section of the module contains the terminations for the multipliers. The section is divided into two identical halves, one for each multiplier. The multiplier will also perform division, squaring, and square root operations when patched as shown in the accompanying drawings. There are two adjustments located on the patch panel of the Model 3323. Normally, these adjustments may be made as parts of the periodic maintenance checks. If, however, maximum possible accuracy is required in a particular problem, these adjustments should be set immediately before running the problem. The procedure for making these adjustments will be found in the Maintenance section of this manual.

Multiplication Operation. The multiplier/divider is based upon the quarter-square principle, in which the following relationship holds:

$$1/4 \left[(X + Y)^2 - (X - Y)^2 \right] = XY$$

In ±100 volt computers, the multiplier output voltage is always scaled to -0.01 XY.

The circuitry consists mainly of two diode squaring networks, one based upon positive polarities and the other upon negative. For four-quadrant operation, voltages representing X, -X, Y, and -Y must be present at the inputs to the squaring networks regardless of the polarity of input voltages. The accompanying figures show the necessary connections for multiplication. Both input and output voltages may vary between +100 volts and -100 volts.

Division Operation. Division is accomplished by the terminal connections shown in the figure below. The concept is illustrated by the circuit diagram in the same illustration. If the output of amplifier 1 is designated Z, the output of the multiplier must be +.01YZ. By reference to the basic discussion on operational amplifiers (paragraph 2.8.), it follows that X = -.01YZ, or Z = -100X/Y. Since +.01YZ and Z must always be opposite in polarity to X, it also follows that Y must always be positive in order to maintain this relationship.

If Y occurs in the problem only as a negative voltage, apply it to the -Y multiplier terminal and patch the input and output terminals of the inverting amplifier to the -Y and Y terminals, respectively. Z still equals -100X/Y. The absolute value of Y must always be larger than X; otherwise, the output would tend to be larger than 100 volts, causing an overload.

Squaring. Squaring is performed as a special case of multiplication where X = Y. Only one input inverter amplifier is required. Patch together the R and Y input terminals and the -R and -Y terminals. Leave the other connections as for multiplication. The output voltage taken at the amplifier output terminal represents $-0.01X^2$

A $+0.01X^2$ output is obtained by the alternate connections shown in Figure 16. (Patch R to -Y, -R to Y.)

Squareroot Operation. The squareroot operation is a special case of division where Z = Y. The relationship $Z = -100X/Y$ of division becomes $Z^2 = -100X$ for $-100 \leq X < 0$, $Z = 10\sqrt{X}$, for $0 < X \leq +100$, $Z = -10\sqrt{X}$.

If X is always negative, patch together the R and Y terminals and the -R and -Y. If X is always positive, patch R to -Y and -R to Y. Leave all other connections as for division. See Figure 17.

Steps:

1. Turn on the computer and allow the amplifiers and power supply to warm up for approximately 30 minutes. Balance the amplifiers according to the instructions given in paragraph 2.21.
2. Make all connections for multiplication according to paragraph 2.12.
3. Apply input voltage of X = Y = +100V. (Computer reference.)
4. Connect the null voltmeter or DVM to the output terminal of the output amplifier. Adjust the X Gain Control for a reading of exactly -100V.

4a. (OPTIONAL) Reverse the polarity of both input voltages and remeasure the output voltage. Readjust the X Gain Control for an output reading exactly halfway between the two values measured in Steps 4 and 4a.

5. Change the polarity of one input voltage only. Adjust the Y Gain Control for a reading of exactly +100V at the output.

5a. (OPTIONAL) Reverse the polarity of both input voltages and remeasure the output voltage. Readjust the Y Gain Control for an output reading exactly halfway between the two values measured in Steps 5 and 5a.

NOTE: Multiplier circuits cannot be driven from potentiometers due to their variable input impedance characteristics.

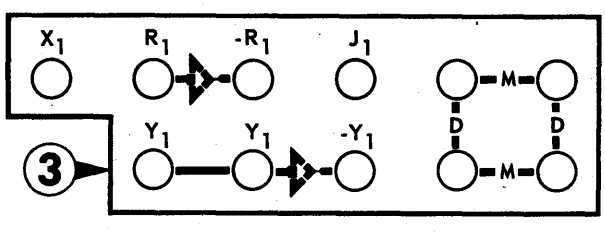


Figure 12. Connections for Multiplication (Model 3323 Dual Multiplier/Divider)

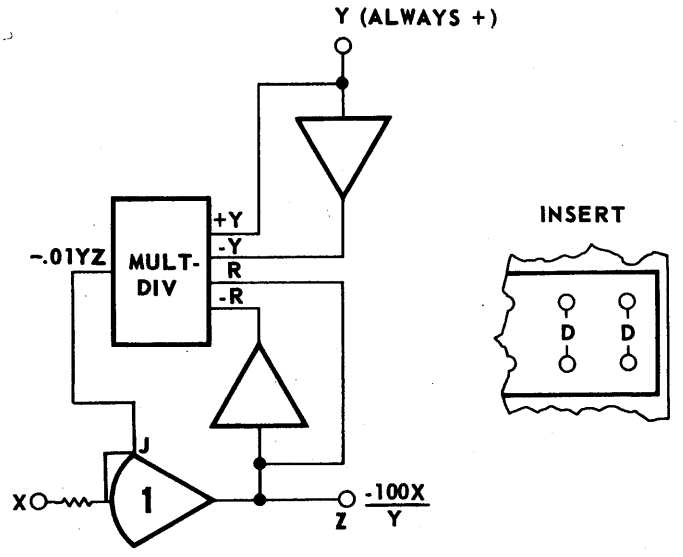


Figure 13. Circuit for Division Operation with insert showing how to convert from Multiplier Patching.

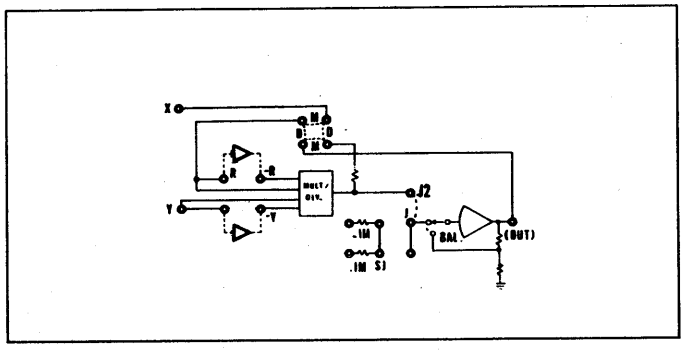


Figure 14: Multiplier, Block Diagram

Alternate Model 3323 Patching

The alternate methods of multiplier patching (as shown below) have in some modes distinct advantages over the conventional methods shown on the preceding pages. Using the alternate method, patching is the same for all modes of operation. All that changes is the position of the shunt plug that selects multiplication or division.

Note that in the division and square root modes the restrictions imposed upon the input polarities are less severe than those imposed with conventional patching.

In the multiplier mode, the restrictions are more severe and limit the usefulness of the circuit. The advantage of the alternate patching, here, is that it saves one amplifier.

The squaring mode is the same except that the output is $-.01$ (sign X) X^2 or $-.01\ X|X|$. The X times the magnitude of X result is useful as it is required in certain problems and can be obtained without the use of separate absolute value circuits.

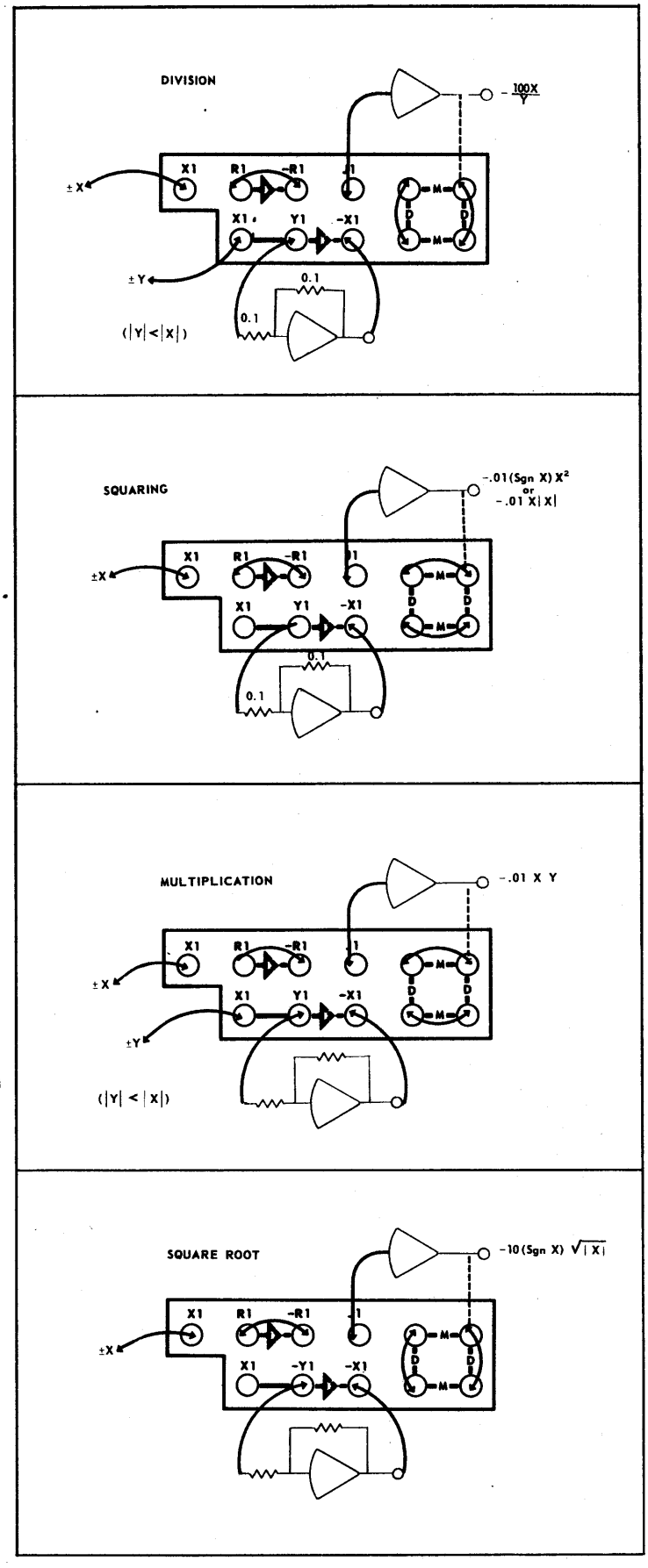
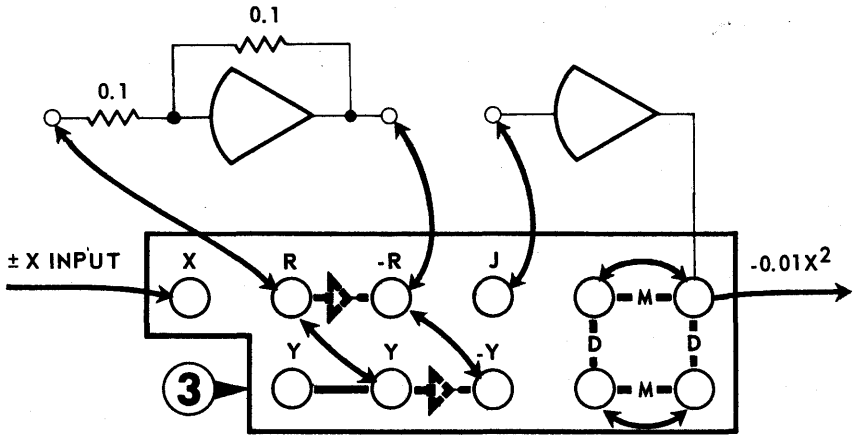
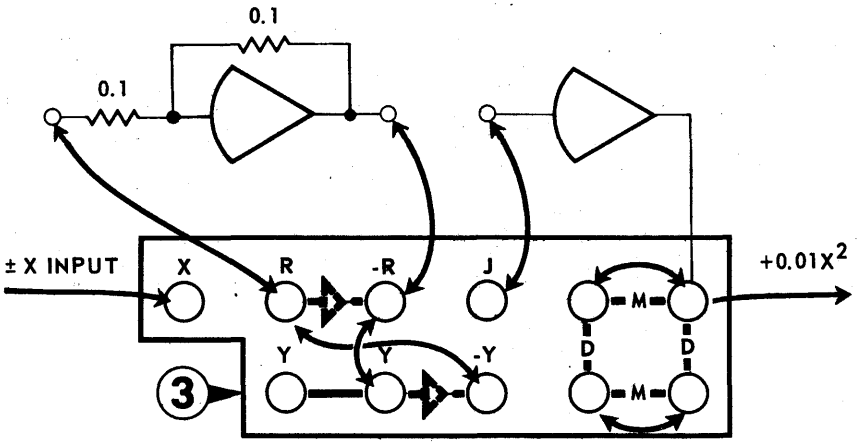


Figure 15: Alternate Model 3323 Patching

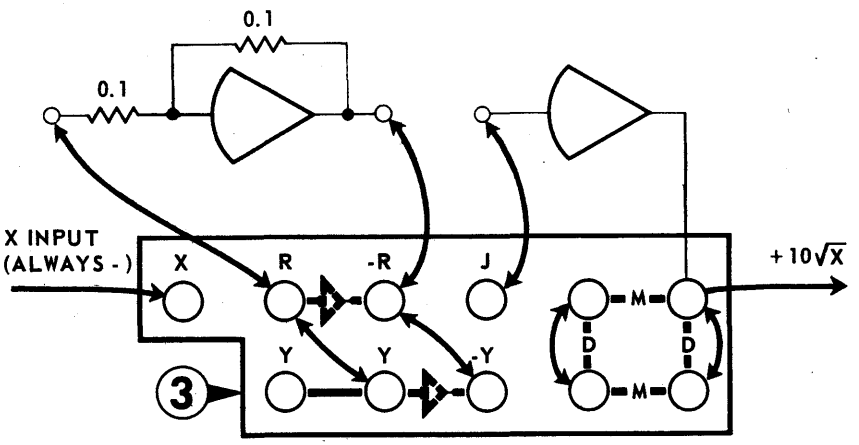


A. ($-0.01X^2$ OUTPUT)

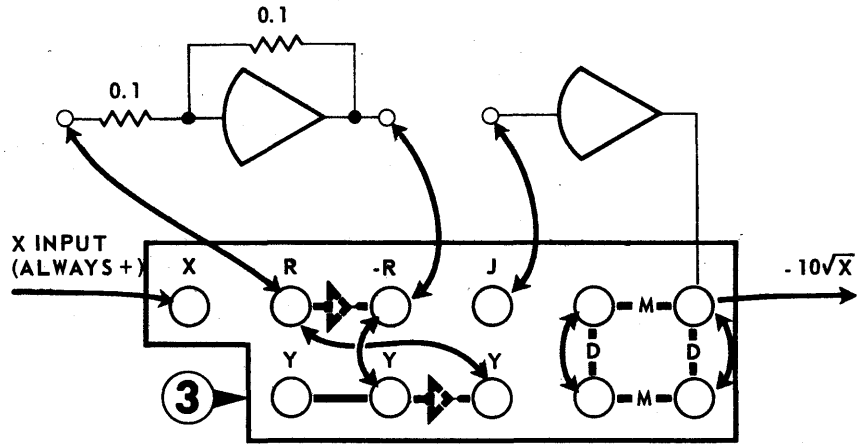


B. ($+0.01X^2$ OUTPUT)

FIGURE 16. CONNECTIONS FOR SQUARING (MODEL 3323 MULTIPLIER/DIVIDER)

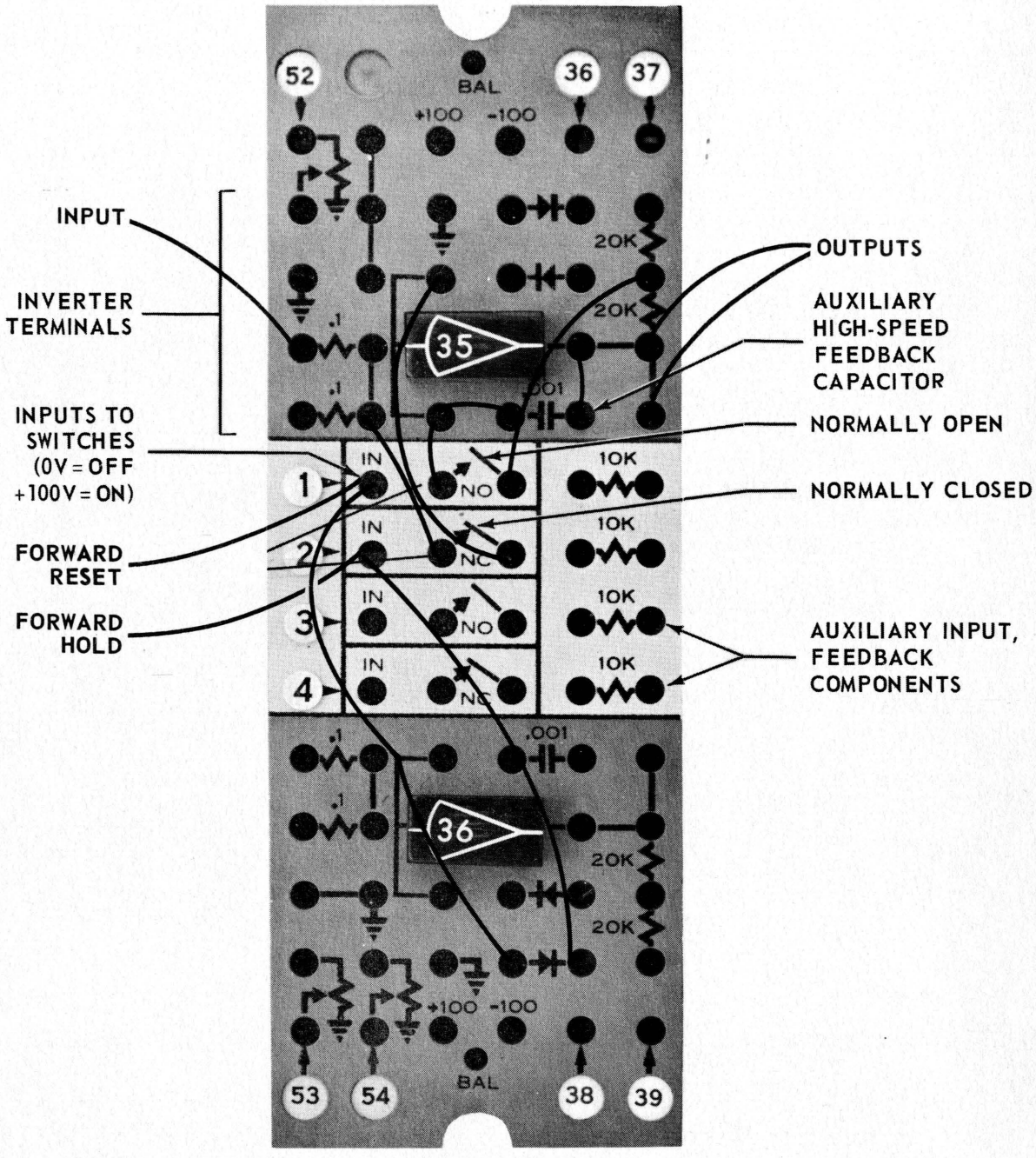


A



B

FIGURE 17. CONNECTIONS FOR SQUARE ROOT (MODEL 3323 MULTIPLIER/DIVIDER)



Model 3324
patched as
an Integrator
(Gain = 10,000)

	A	B
R	On	On
C	Off	Off
H	Off	On

Figure 18. DUAL INVERTER WITH FOUR ELECTRONIC SWITCHES, MODEL 3324

2.13 *Model 3324 – Dual Inverter, Quad Electronic Switch*

The inverter sections of the Model 3324 are identical in operation and performance to those of the Model 3322A. Patching is identical to that of the Model 3322A and the instructions for that Model may be used.

The center section of the Model 3324 contains four electronic switches. There are two normally open (NO) and two normally closed (NC) switches. The normal voltage required to excite the switch is a nominal +28 volts, however, voltages of up to ±100 volts will not damage the switch. The current required to excite the switch is less than three milliamperes at 28 volts.

The Electronic switches were designed and are normally used to replace the reed type relays in the integrator modules. The Electronic switches may be used as normal switches as long as the input voltage and current through the switch limitations are observed (See Model 3324 Specifications, page 6.)

Patching to the Model 3320, Dual Integrator is shown in the accompanying illustration. Patching to the Model 3329, Dual Integrator is similar. Also included in the Model 3324 are two .001 mfd. capacitors and four .01%, 10 K ohm resistors for use in high speed Sample-Hold circuits.

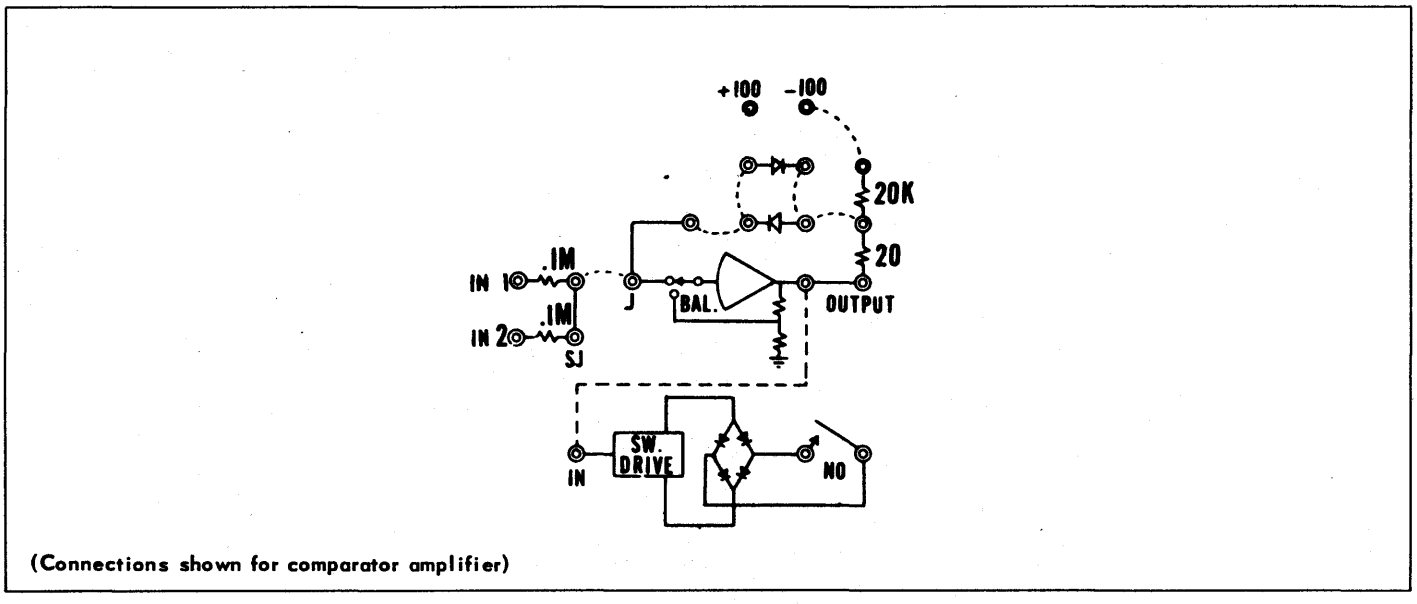


Figure 19. Electronic Switch Block Diagram

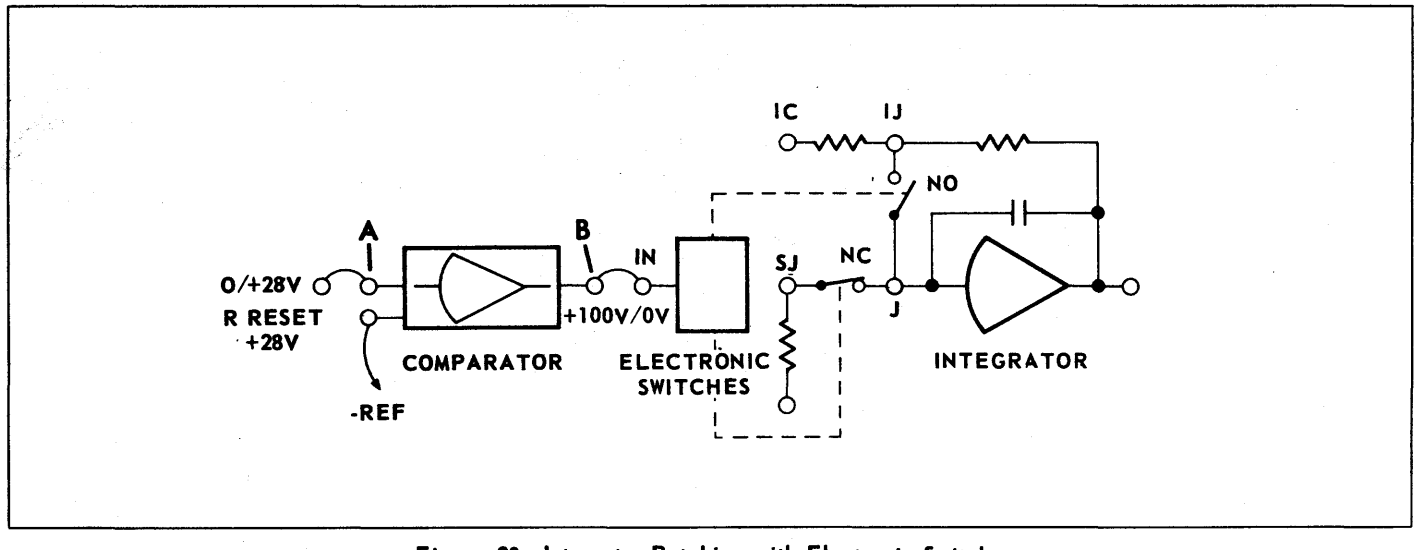


Figure 20. Integrator Patching with Electronic Switches

Note: H Relay Coil must be patched to +28V, see Patching Diagram Figure 22.

2.14 *Model 3325 – Quad Summer*

The Model 3325, Quad Summer is identical in performance to the Model 3321, Dual Summer. As illustrated, patching of the Model 3325 is, however, considerably different than that of the Model 3321. Basic patching for any of the four summers in the module consists of patching the SJ' terminal to the J terminal and patching the right end of the feedback resistor to any of the output terminals. Any of the resistor input networks may be used with any amplifier. Thus summers with six, nine or twelve inputs may be patched.

The Model 3325 also contains four spare resistors, four diodes and four trunk lines. In addition, it has terminations for a Function Switch and for a Diode Function Generator.

The Model 3325 is also used as a source of amplifiers for the Model 3329. When used in this manner, the Model 3325 furnishes the amplifier and input resistors for the integrator circuit. The illustration below shows the circuits of both the Model 3325 and 3329. Dotted lines indicate patching connections.

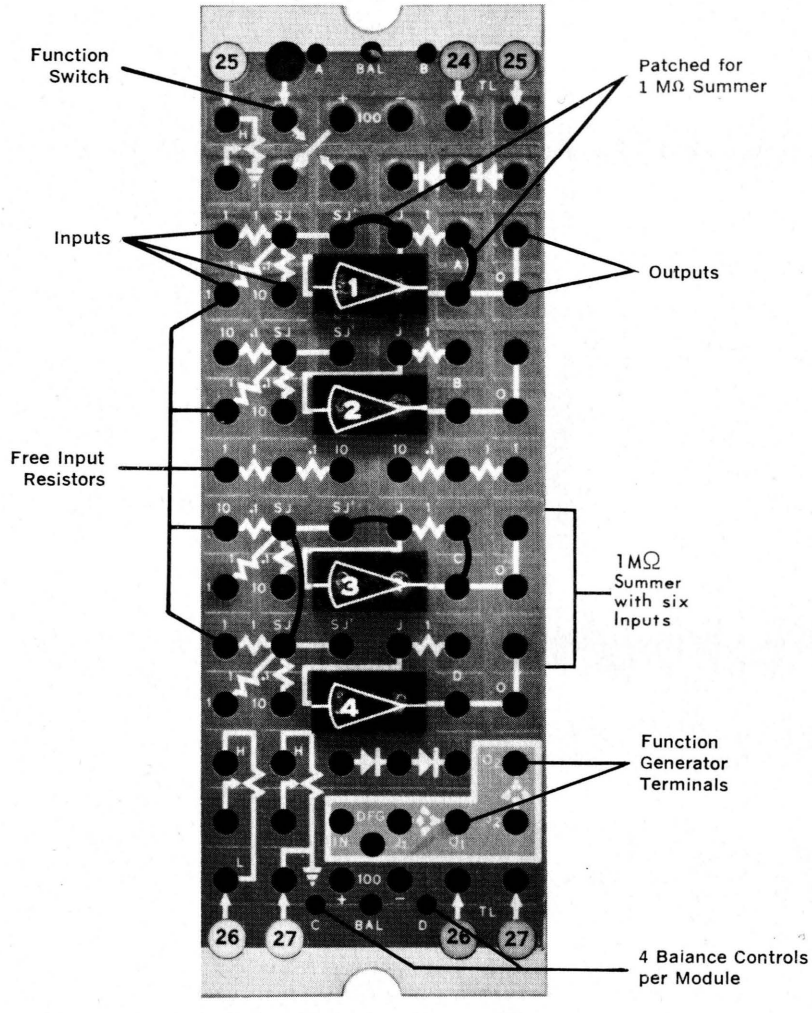


Figure 21. MODEL 3325 WITH SUMMER PATCHING SHOWN

MODEL 3320 MODEL 3324

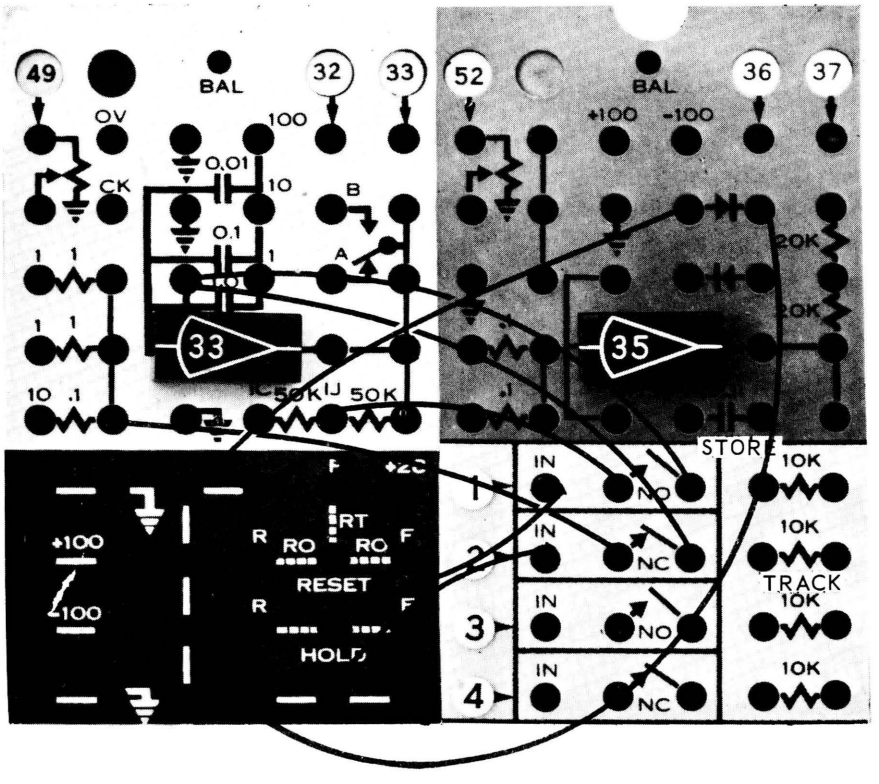


Figure 22. INTEGRATOR PATCHING WITH ELECTRONIC SWITCHES

2.15 *Models 3326, 3327, and 3328 Digital Logic Elements*

Because of their nature the digital logic elements will be presented in a different manner than that used for the Analog Modules. A brief, general discussion on the Digital Logic Elements is followed by the detailed operating procedures.

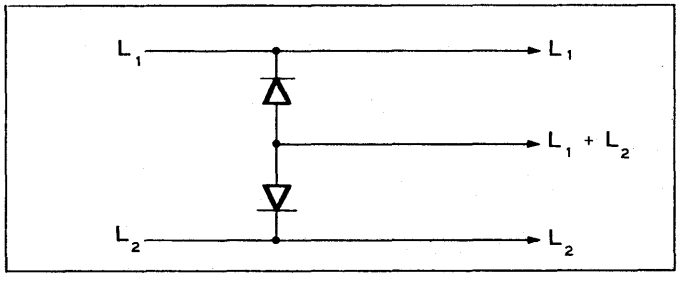
BASIC OPERATION OF DIGITAL LOGIC ELEMENTS

Digital logic can be included in an analog computer. It is used for making program decisions based on events occurring during the analog simulation and is also used for program control. This section describes the basic operation of the logic elements.

Logic levels for the elements are

+28 volts = false (logical zero)
0 volts = true (logical one)

Most of the elements have a logically complemented output in addition to the normal output. All of the elements, except the drivers and the dividers, have status lights. When the light is on, the element is in the ''true'' state. All of the elements, with the exception of the drivers, are designed so that their outputs can be connected together without damage. This feature is very important because it permits an OR operation by connecting two or more outputs to the same point on the patchboard. (Driver outputs must never be connected to any other digital or analog output.) However, when two outputs are connected together in this way, they cannot be used as separate logical variables. To avoid this difficulty diodes can be used. Thus, if L_1, L_2 are two logical outputs and $L_1 + L_2$, L_1, L_2 are all required for logical inputs elsewhere in the program, the circuit below can be used



OR is the logical sum of logical variables. The table below shows the OR operation for two logical variables, denoted by L_1 and L_2.

L_1	L_2	$L_1 + L_2$ (L_1 or L_2)
0	0	0
0	1	1
1	0	1
1	1	1

AND is the logical product of logical variables. The table below shows the AND operation for two logical variables, L_1 and L_2.

L_1	L_2	$L_1 \cdot L_2$ (L_1 and L_2)
0	0	0
0	1	0
1	0	0
1	1	1

Each of the logic elements will drive any reasonable number of others. However, the logic elements are not capable of activating analog control relays or function relays. For this purpose drivers are supplied. The driver acts as both a power buffer and logical inverter. It should be noted that the logic levels for mode control and function relays are the opposite or complement of those for digital logic. That is

0 volts = false (relay de-energized)
+28 volts = true (relay energized)

Thus, the driver not only delivers the current necessary to operate several relays but also provides the logic level inversion required. To use a driver, the output of the logic element is connected to the driver and the output of the driver to the relay input. These connections are made readily at the patchboard. It should be noted that the driver is a special element and its output cannot be used as an input to the flip-flop's or DCU's. It can be used as a GATE input.

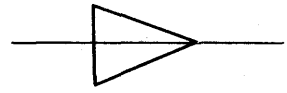
The remainder of this section describes the operation of the digital logic elements.

DRIVER

The driver is used as a power buffer and logical inverter from digital logic elements to analog mode control, function relays, and electronic switches. Its logic levels are

INPUT	OUTPUT
0 (false)	0 volts
1 (true)	+28 volts

The program symbol is



Important: The driver outputs must never be connected to any other digital logic output. Connecting a driver output to ground (logical 1) will destroy the output transistor.

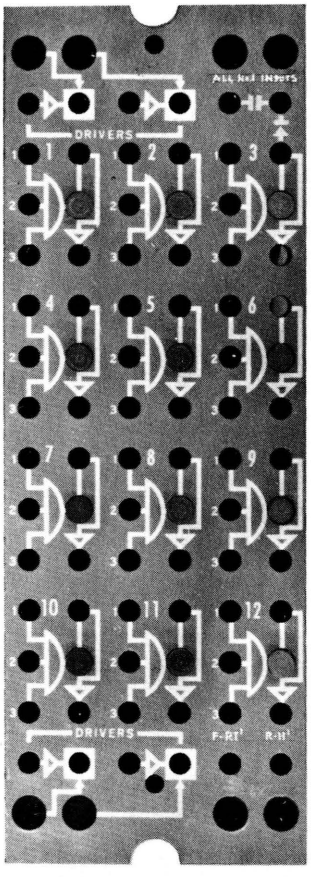


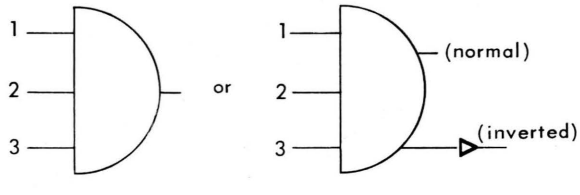
Figure 23. Logic Gate Module

GATE

The logical gates are of the coincidence type. With the exception of input number 1, they operate as AND gates only on the inputs connected. That is, if no logical variable is connected to one of the inputs at the patchboard, then this input is essentially de-activated. Note that this is the same as connecting a logical one to the input.

Input number 1 is different because it must be connected; otherwise, the gate will not operate. However, if only input 1 is connected, the gate will act as an inverter if its complemented output is used.

The program symbol for the gate is



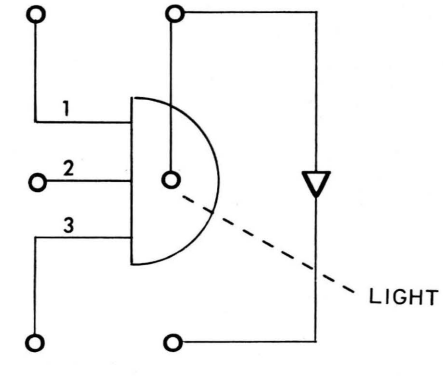
where the input numbers are shown.

The truth tables below will clarify the operation of the gate.

INPUTS			NORMAL OUTPUT	INVERTED OUTPUT
1	2	3		
none	any	any	0	1
1	2	3		
0	none	none	0	1
1	none	none	1	0
1	2	3		
0	0	none	0	1
0	1	none	0	1
1	0	none	0	1
1	1	none	1	0
1	2	3		
0	none	0	0	1
0	none	1	0	1
1	none	0	0	1
1	none	1	1	0

INPUTS			NORMAL OUTPUT	INVERTED OUTPUT
1	2	3		
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

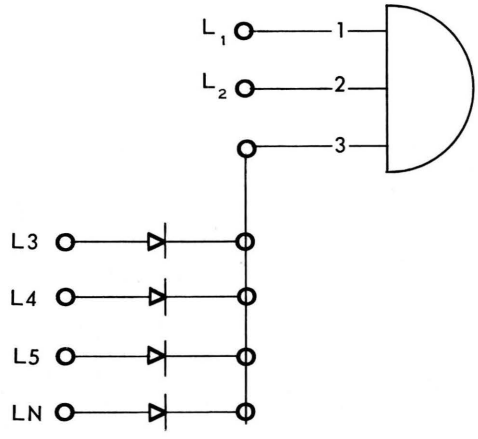
The gate is shown on the patchboard as



The inverter may be used individually. That is, the programmer can connect a logical variable to the complemented (inverted) output of the gate to obtain an OR function, without affecting the AND gate function to the normal output.

The true state response to inputs 1 and 2 is delayed by 50 μ sec, while input 3 is not. This allows the gates to be used in connection with flip-flops to form a shift register. Also, this feature frequently obviates the necessity of using one-shots for delays in a logic program.

Each gate has three inputs on the patchboard. If the logical product of more than three variables is desired, the additional elements can be connected in through externally patched diodes, as shown below.

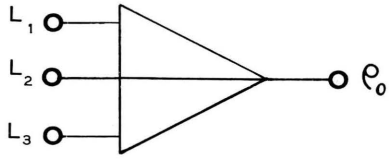


The additional elements can be connected to any of the patchboard inputs with the exception of input number 1 unless one of the input diodes is omitted.

The gate can also be used for pulse-shaping. It is on (logical 1 at the output) when no input voltage is greater than 4 volts and off when any input is greater than 6.5 volts. When the net input is between 4 and 6.5 volts, the output corresponds to the last state of the gate.

Gate–Driver

There is a special element found in the TIME/EVENT CONTROL MODULE. It is a power buffered, logically inverted AND gate which performs the combined function of AND gate and driver. The program symbol is



where L_1, L_2, and L_3 and P_0 are respectively logical input variables and the output voltage. This gate is the same in logical operation as the AND gate except there is no delay introduced at any input. When $L_1 \cdot L_2 \cdot L_3 \pm 1$, the output of the gate is 28 volts and otherwise zero. The primary use of this gate is for implementing analog mode control changes based on logic outputs. For example, in this way a multiple decade counter can be used either to stop the analog computer after a prescribed number of runs or in conjunction with a clock to specify precisely the length of time the analog computer is in one of several modes. This is accomplished by switching the output of a gate-driver to either the C, R, or H inputs on the patchboard.

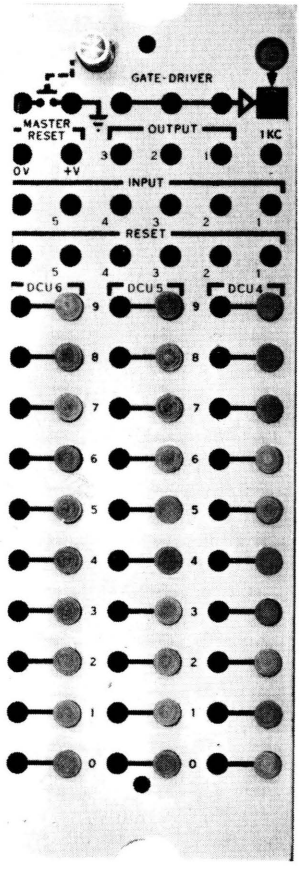


Figure 24. Time-Event Control Module

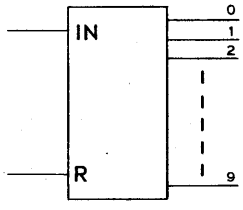
Decade Counting Unit (DCU)

The DCU is either a decade divider or a decade counter. It contains ten internal binary states which correspond to integers from 0 to 9. Note that this is different than a binary counter which counts in the binary number system. There are two types of DCU's in the computer. Both of these are in the TIME/EVENT CONTROL MODULE. One has all the integer binary states available as a "ten line" output. This element is called a decade counter. A status light is associated with each of the integer binary states. The other type has only the decade output available and is called a decade divider.

There are two master resets for each group of 3 decade counters together with 3 decade dividers. These are the OV and +V terminals. The OV input is directly coupled to the clock. As long as a logical one is applied to this terminal the clock will be stopped. A state change from zero to one will cause all the counters and dividers to be reset. As long as a logical one is maintained at this terminal, all other reset signals are inhibited. A state change from one to zero at the +V terminal will cause all the counters and dividers to be reset. The +V input does not inhibit other reset signals. It also does not turn off the clock.

All counter or divider inputs (including reset inputs) require a change from a logical zero to a logical one (or a negative-going voltage pulse) for operation. Thus, the application of a logical one to an input will cause it to operate once. It will not operate again until the logical one is removed and re-applied. This is true also for the master reset for each counter/divider group.

The program symbol for the decade counter is



The outputs are the ten integer counts from 0 to 9. Whenever a negative going pulse or a logical one is applied to the reset terminal, the counter will return to count zero. Whenever a negative going pulse or a logical one is applied to the input terminal, the counter will advance to the next higher integer count. The counter is cyclic: when it is in count 9 and receives an input pulse it returns to count zero.

Note that the counters can be used in series. This is accomplished by connecting any output from the first counter to the input of the second counter. Then, whenever the transition from a logical 0 to a logical 1 occurs at the output of the first counter, a transition from 0 to 1 is applied to the input of the second counter. This causes the second counter to advance one count. Normally, the second counter receives its input from the "0" digit of the first. Then when a transition from count 0 to count 1 occurs in the first counter, the output from count 0 goes from 1 to 0 and the second counter will not be advanced in count: its input is activated only on a change of state from zero to one.

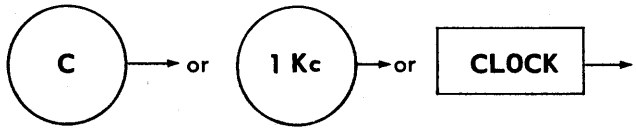
The program symbol for the decader divider is

The divider has ten internal integer states in the same way as the counter. However, these are not available as logical outputs. An input to the reset terminal will cause the divider to return to zero count internally. If the logical variable applied to the input terminal changes state from 0 to 1 then the divider will count internally. The divider is cyclic: count 0 follows count 9. With a sequence of input pulses, the output is a logical 1 except when the internal counter is in count 8 or count 9. Thus, when the internal transition from count 9 to count zero occurs, there is a transition from 0 to 1 at the output which can be used as input to other logic elements.

However, it should be remembered that if the divider is reset during the time when internally it is in count 8 or count 9, the transition from 0 to 1 will occur at the output then.

Clock

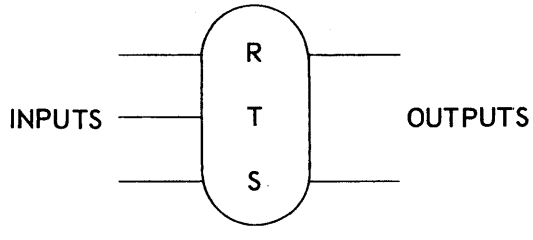
Each TIME/EVENT CONTROL MODULE provides a 1000 cycle per second clock output at the patchboard. Maintaining a logical one at the 0V master reset terminal will stop the clock. The program symbol for the clock is-



The logical cycle of the clock is repetitively a logical 1 for 800 μ sec and logical 0 for 200 μ sec.

Flip-Flop

A flip-flop (FF) is a one-bit memory. It has a set (S) and a reset (R) state. The set state corresponds to true (logical 1) and the reset state to false. The program symbol is



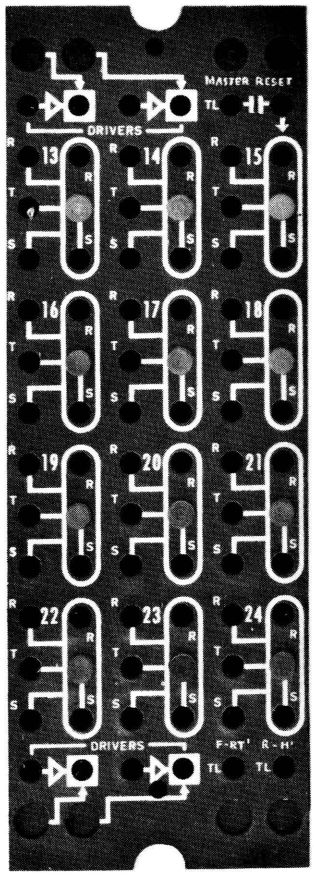


Figure 25. Flip-Flop Module

There is a status light connected to the S output so that when the FF is in the S state the light will be on. The FF can be placed in the S state by applying a logical 1 or negative-going pulse to the S input. It can be placed in the R state by applying a logical 1 or negative-going pulse to the R input. Applying a logical state change from 0 to one or a negative-going pulse to the T input will cause the FF to change to the opposite state. The flip-flop R, S inputs are direct coupled. Each can be A-C coupled by inserting a 200 pf capacitor in series with the input so that these inputs will be activated by only logical state changes from 0 to 1 and not by logic levels.

Internally, the application of a logical 1 to the S input turns off the R output, and a logical 1 at the R input turns off the S output. The R and S inputs are level sensitive in contrast to the T input which is activated by state changes. Consequently, if a logical 1 is applied to both the R and S inputs simultaneously, both the R and S outputs will be a logical 0, and a state change at the T input will have no effect on the state of the FF. If both R and S inputs are a logical 1 and then both are changed to a logical 0 simultaneously, the final state of the FF will be either R or S with nearly equal probability. If the change to 0 does not occur simultaneously, the input which sees the logical 1 last will control the state of the FF.

If either the R or S input is connected to the S or R output, and if a pulse or logical variable state change is applied to the T input, the FF will act like a one-shot (mono-stable multivibrator). That is it will make a transition to the opposite state for about 5 μsec.

Two master reset terminals are located at the patchboard for each FF module. One will put all FF's in the R state for a transition from 0 to 1. The other reset is level sensitive: as long as a logical one is applied all the FF's are constrained to be in the R state.

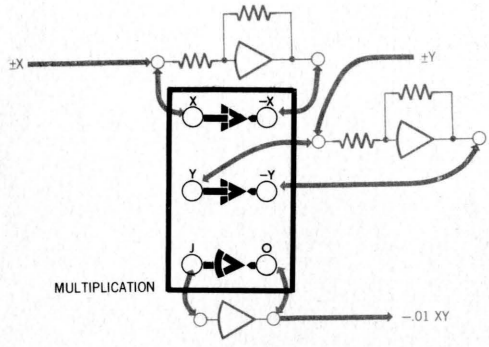
COMPUTER CONTROL LOGIC OUTPUTS

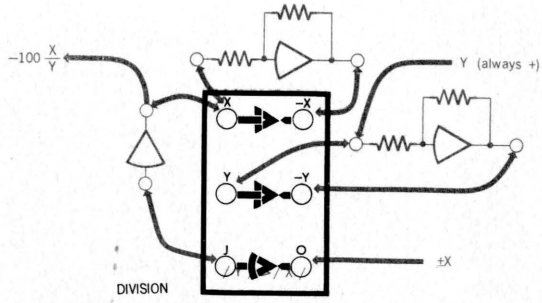
The normal analog control logic outputs in the integrator module cannot be used as an input to any logic element except a gate, therefore special F-RT and RH outputs are located in the F-F and Gate modules. These can be used as an input to any of the logic elements. The outputs are identified as F-RT' and RH'. The logic levels for both F-RT and F-RT' are consistent with the digital logic elements. There is a logical inversion between F-RT and F-RT' as well as RH and RH'. For example, when F-RT' is connected to a flip-flop's R input the F-F will be in Reset when the F-RT bus is energized. When the F-RT bus is denergized, the F-F's are free to respond to signals at their T and S inputs.

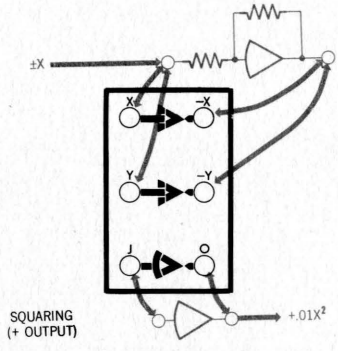
Note that the F-RT and RH buses operate in complementary fashion.

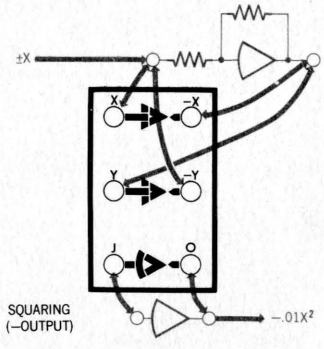
LOGIC SWITCH

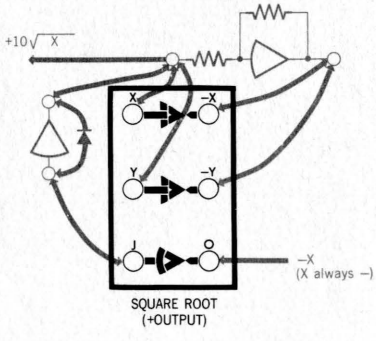
There is a manual logic switch on the Time/Event Control module which is convenient for single-stepping programs.











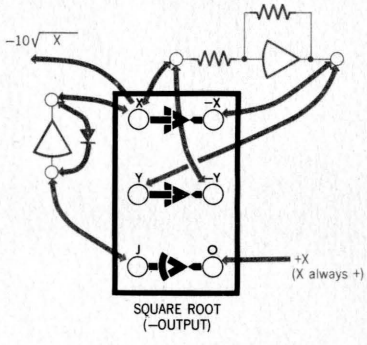


Figure 26. MODEL 3329 MULTIPLIER, PATCHING DIAGRAM

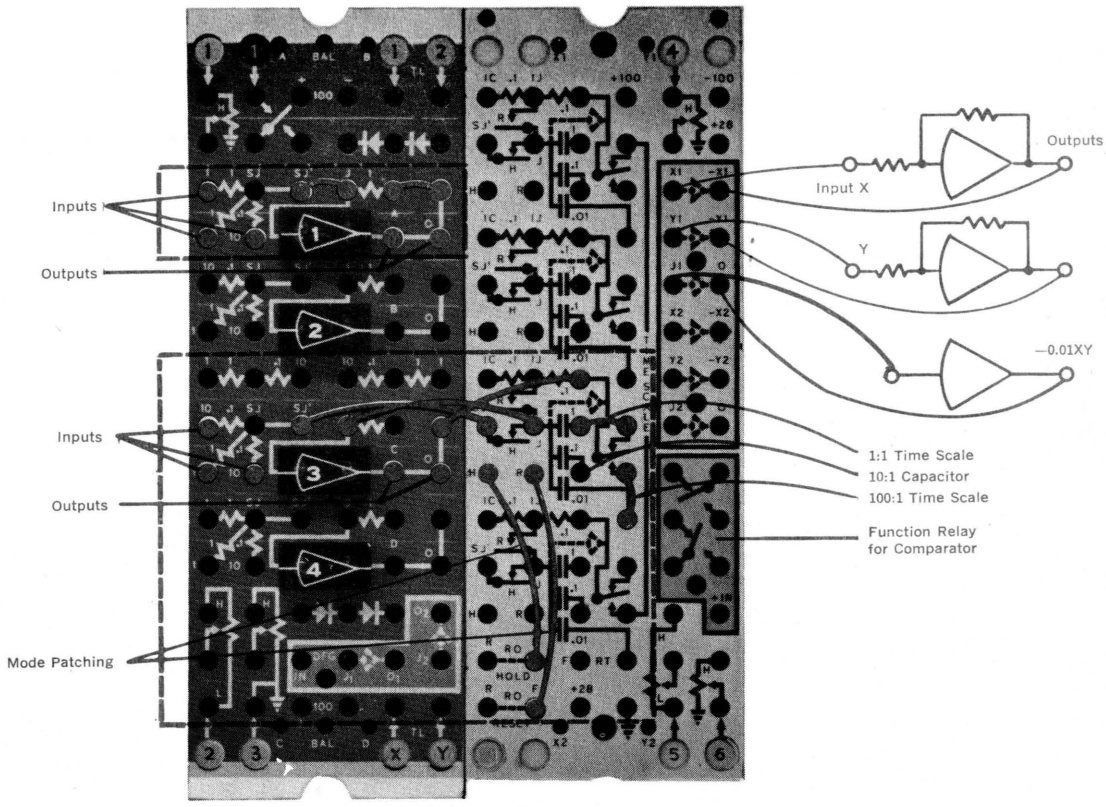


Figure 27. PATCHING TO MODEL 3325 FROM MODEL 3329

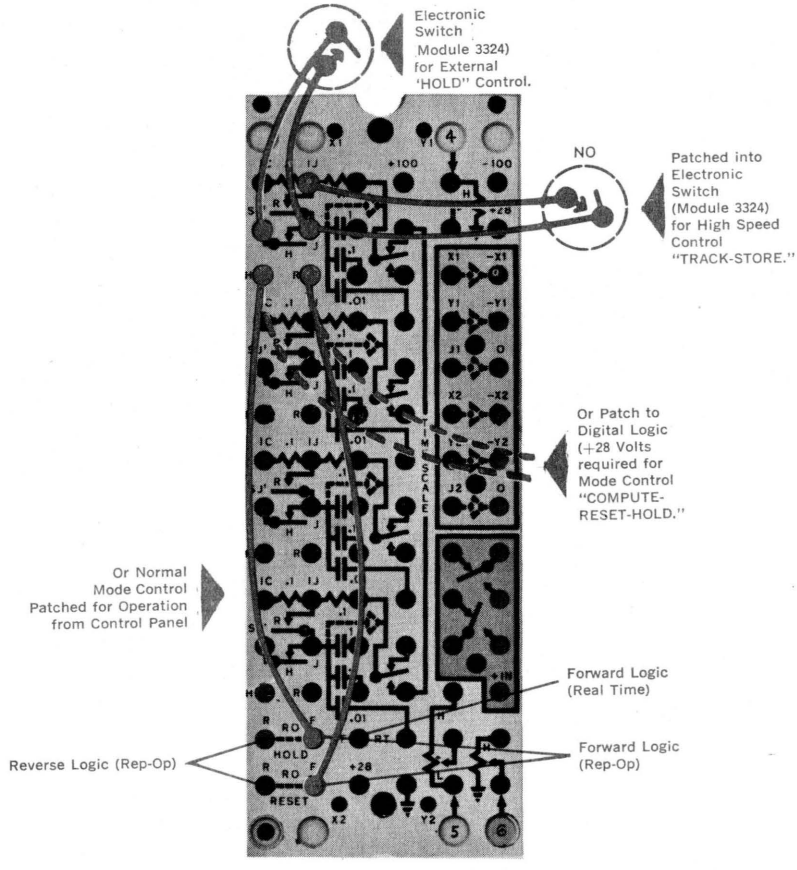


Figure 27. LOGIC CONNECTIONS, MODEL 3329

2.16 *Model 3329 – Dual Integrator, Dual Multiplier, Function Relay*

The Model 3329 has four integrating networks without operational amplifiers. As illustrated, the operational amplifiers necessary for integration are normally patched into the Model 3329 from an adjacent Model 3325. The input resistor network of the Model 3325 then becomes the input to the integrator. Relay logic connections are in the lower left hand section of the Model 3329 patchboard. Nomenclature is the same as that used on the Model 3320, Dual Integrator. Each Integrator Network has a Hold (H) and Reset (R) terminal associated with it, these terminals must be individually patched to the Relay Logic terminals. The Squid (multiple) patch cords should be used when more than one integrating network is to be used at the same time.

The Dual Multiplier section of the Model 3329 may be patched for division, squaring and square root functions as well as for multiplication. For multiplication or division operation, three operational amplifiers are required, as illustrated. In the division and square root functions arbitrary limitations as to polarity and relative amplitude of the inputs are imposed. As an instance in division the Y input must always be positive and equal to or greater than the X input. Note that in square root an external diode must be patched into the circuit.

Patching and operation of the Function Relay in the Model 3329 is identical to that of the Function Relays in the Model 3322A. The relay is energized by a nominal +28 volt signal and will not be damaged by a signal of up to ±100 volts.

Alternate Multiplier Patching

The alternate methods of multiplier patching have in some modes distinct advantages over the conventional methods shown on the preceding pages. Using the alternate method, the X and -X terminals of the multiplier are patched together in all modes.

Note that in the division and square root modes the restrictions imposed upon the input polarities are less severe than those imposed with conventional patching.

In the multiplier mode, the restrictions are more severe and limit the usefulness of the circuit. The advantage of the alternate patching, here, is that it saves one amplifier.

The squaring mode is the same except that the output is $-.01\ (\text{sign X})\ X^2$ or $-.01\ X\,|\,X|$. The X times the magnitude of X result is useful as it is required in certain problems and can be obtained without the use of separate absolute value circuits.

	Restrictions	Output
MULTIPLY	$\|Y\| < \|X\|$	$-.01X\,\|\,Y\|$
DIVIDE	$\|Y\| < \|X\|$	$-\frac{100X}{\|Y\|}$
SQUARE	None	$-.01X\,\|\,X\|$ or $-.01\ (\text{Sgn X})\ X^2$
SQUARE ROOT	None	$-10\ (\text{Sgn X})\ \sqrt{\|X\|}$

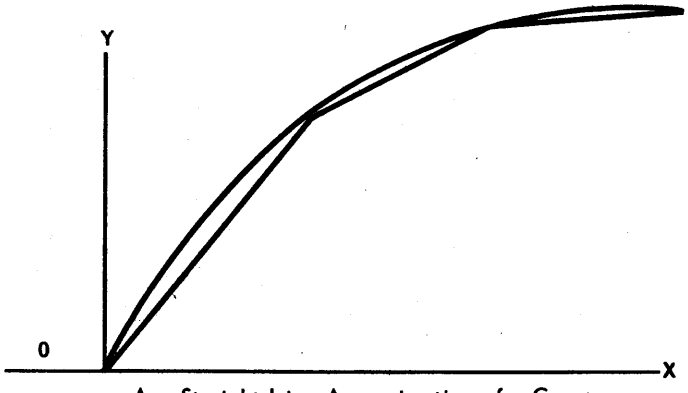
2.17 *Model 3351 – Function Generator*

Principle of Operation: The Model 3351 Function Generator approximates the curve of an arbitrary function with a series of connected straight-line segments as shown in Figure 28A. This graph represents the sum of the individual line segments shown in Figure 28B. Each line segment corresponds to the output voltage of a diode network in the function generator. The point along the X axis where each line begins corresponds to the selected bias or "breakpoint" voltage. The diode networks are arranged so that six conduct when the X input is positive (0 to +100 volts) and six when the X input is negative (0 to -100 volts). For better accuracy, the input voltage may be biased to use all 12 networks above or below zero. (See "Expanded Scaling"). Two Model 3351 units can be operated as a single-channel of 24 segments for more accurate simulation.

The slope of each line segment corresponds to the ratio of output voltage per volt-change of input and can be varied between the values of +2 and -2 by adjusting the current flow through the diode network. For steeper changes of line slope at any point, two or more networks can be operated in parallel by shifting to the same breakpoint.

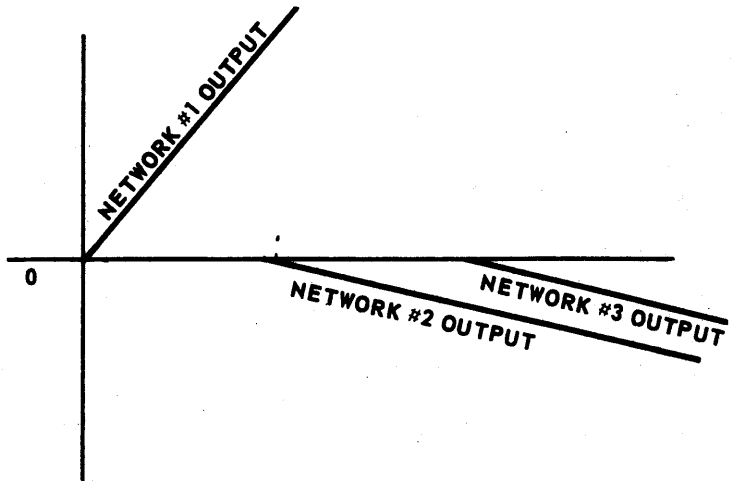
When the individual outputs of all diode networks are added together by an operational summing amplifier, the total output over the entire range of X-input will reproduce the original straight-line approximation. No output is produced when X = 0; therefore, a constant voltage, Y_0, must be added at the output summing amplifier, when Y is not equal to 0 at X = 0.

Set Up Procedure: A function may be set up on the function generator either by the preparation of a table of values to which the individual slope and breakpoint potentiometers are adjusted, or by adjusting the potentiometers so that a trace of the output voltage on an XY plotter will match a prepared graph as closely as possible (visual method). The second method may be faster but is limited in accuracy by the read-out instrument.



A. Straight Line Approximation of a Curve.

A of Figure 28A



B. Outputs of individual Diode Bridge Networks, the sum of which produces the Straight Line Approximation shown in Figure 28A.

Figure 28B. Simulation of a Function with Diode Bridge Network Outputs

Tabular Method of Adjustment

(1) Prepare a graph of the function to be simulated as in Figure 29. Select six points of +X value and six points of -X value that best approximate the curve when connected by straight lines. Crowd the points together where the slope changes rapidly. If the values of X are all of one polarity, expanded scaling may be used. (See 3 below.)

(2) Scale the X and Y coordinates of the selected points into appropriate voltages utilizing the full voltage range of the function generator (X = Y = ±100 volts), if possible.

Expanded Scaling: Figure oo illustrates how a single-quadrant function may be expanded so that all twelve line segments can be used for simulation. Each X breakpoint value is changed to 2X - 100 as shown in Table 3.

The modified input circuit of Figure 31 must be used.

(3) Connect the function generator using the set-up circuit in Figure 32. All connections are performed at the function generator terminals on the problem board. Resistor R_k is not used if Y = 0 at the point X = 0.

(4) Adjust the Break and Slope potentiometers as follows:

a. Turn all Break and Slope controls to their maximum clockwise position. This moves all line segments away from the origin and sets their slopes at maximum.

b. Set the input voltage source to zero volts.

c. Adjust the Y_0 (in) source until the output has the proper value of Y for Point 0.

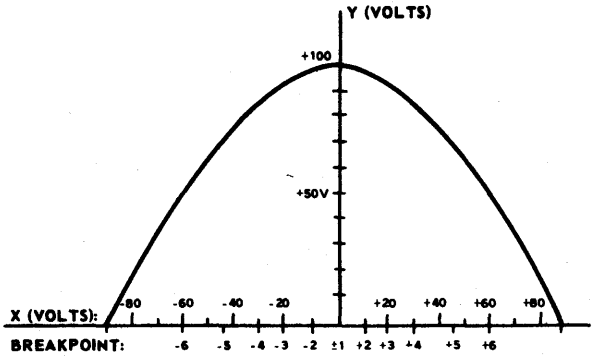


Figure 29. Typical Graph prepared for setting up the Function Y = COSX.

d. Set the X input voltage to X_1, the X value of the first breakpoint, if $Y_0 = 0$, $X_1 = 0$ normally. Turn the +1 BREAKPOINT control counter clockwise until the output shifts from its previous value by about .1 to .2 volts. Set X to the value X_2, and adjust the +1 SLOPE control to make the output equal to Y_2.

e. Next, adjust the first negative line segment by turning the -1 BREAK VOLTAGE control fully counter-clockwise. Adjust the input voltage to the value of X at Point -1 and turn the -1 SLOPE control until the output has the proper value of Y at Point -1.

f. Repeat steps b, c and d. (There may be a slight interaction between the values for the first positive and negative line segment adjustments and the value of Y_0.)

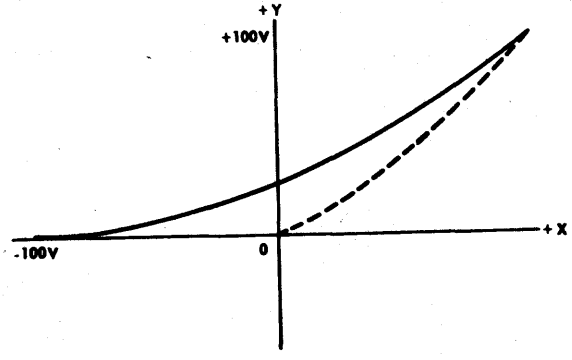
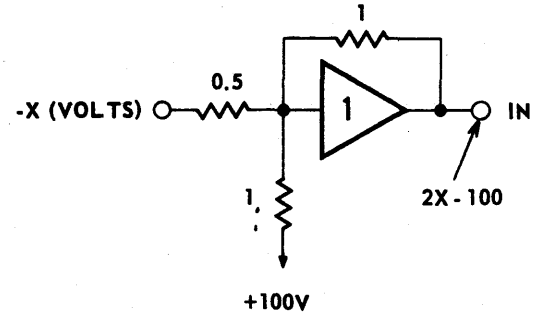


Figure 30. Curve of Function $Y = X^2$ (Dotted Line) and same Function with Expanded X Scaling (Solid Line)



REFER TO FIGURE 20 FOR COMPLETE CONNECTIONS.

Figure 31. Input Connections for Expanded X-Scaling.

g. Adjust the second positive line segment in the following manner: Set the input voltage to a value of X at Point +1 and turn the +2 BREAK VOLTAGE control counter-clockwise until the output starts to change, indicating that the second line segment has begun to add to the first.

h. Change the input voltage to the value of X at Point +2 and adjust the +2 SLOPE control until the output is equal to the value of Y at Point +2.

i. If the slope control will not turn far enough to give the proper reading, repeat the entire line segment adjustment using simultaneously two successive Break controls and the two related Slope controls.

j. Complete the adjustments for the remaining positive line segments by repeating Steps f and g.

k. Set up the function for negative values of X by repeating Steps f and g for the remaining negative line segments.

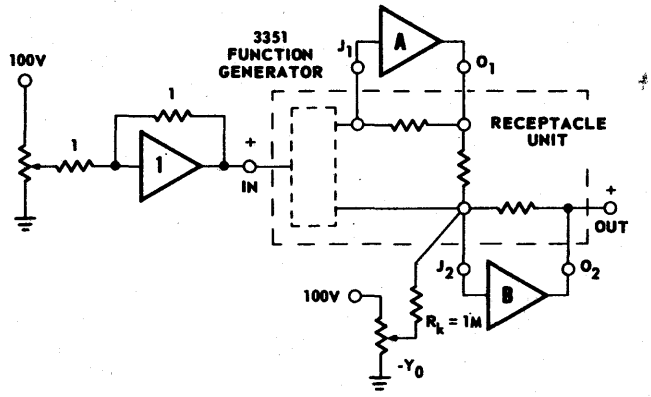


Figure 32. Function Generator Set-up Circuit.

TABLE 2. DATA FOR SETTING UP FUNCTION Y = COSX (See Figure 00)

X (DEGREES)	Y (COSINE)	X (VOLTS)	Y (VOLTS)	CONTROL* BREAK	CONTROL* SLOPE	POINT
-90	0	-90	0		-6	-6
-60	+0.500	-60	+50.0	-6	-5	-5
-45	+0.707	-45	+70.7	-5	-4	-4
-30	+0.866	-30	+86.6	-4	-3	-3
-20	+0.940	-20	+94.0	-3	-2	-2
-10	+0.985	-10	+98.5	-2	-1	-1
0	+1.00	0	+100	±1		
+10	+0.985	+10	+98.5	+2	+1	+1
+20	+0.940	+20	+94.0	+3	+2	+2
+30	+0.866	+30	+86.6	+4	+3	+3
+45	+0.707	+45	+70.7	+5	+4	+4
+60	+0.500	+60	+50.0	+6	+5	+5
+90	0	+90	0		+6	+6

* Arrows indicate sequence of adjustments.

TABLE 3. NORMAL AND EXPANDED SCALING FOR FUNCTION $Y = X^2$

1 NORMAL X*	2 EXPANDED 2X-100	3 NORMAL Y	4 CONTROL (EXPANDED SCALING) BREAK	4 CONTROL (EXPANDED SCALING) SLOPE
0	-100	0		-6
(5)	- 90	.25	-6	-5
10	- 80	1.0	-5	-4
(15)	- 70	2.25	-4	-3
20	- 60	4.0	-3	-2
30	- 40	9.0	-2	-1
50	- 0	25.0	±1	
(60)	+ 20	36.0	+2	+1
70	+ 40	49.0	+3	+2
(80)	+ 60	64.0	+4	+3
(90)	+ 80	81.0	+5	+4
100	+100	100.0		+5

* ( ) Indicates values not obtainable without expanded scaling.

Curve-Fitting (Visual) Method of Adjustment

1. Prepare the graph and make circuit connections as in Steps 1 and 4 of paragraph 2.17. Use an 11x17 sheet of graph paper and mount on the XY plotter or face of the large screen oscilloscope. Use a color of ink on the graph that will not be confused with that of the XY plotter. Calibrate the X and Y scaling of the instrument to correspond to the graph.

2. Apply a repetitive input ramp voltage to the function representing the full ±100V sweep of X. This may be done by using the output voltage of an integrator amplifier in the rep-op mode following the input potentiometer.

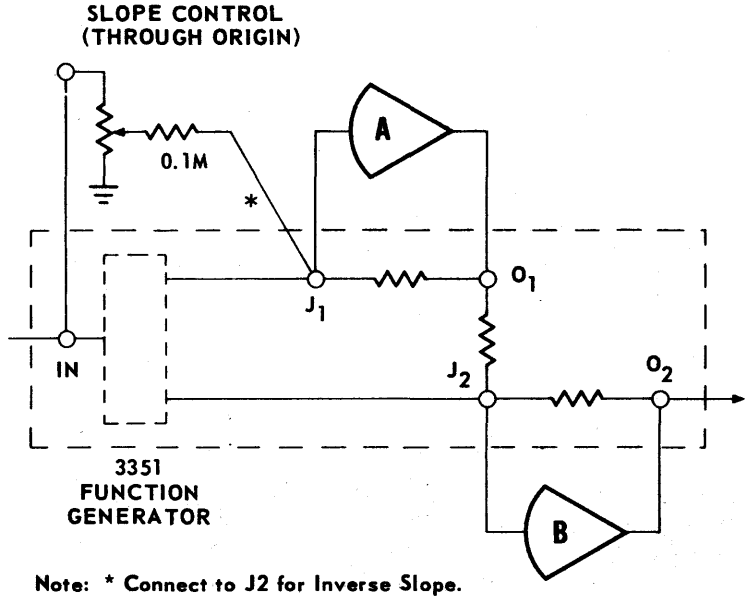
3. Adjust the breakpoint and slope controls in the same sequence as described for the tabular method of adjustment so that a series of line segments are traced out which correspond as closely as possible with the prepared graph.

   Observe that each breakpoint does not have a sharp angle but is slightly rounded; caused by the characteristics of the diode network as it begins to conduct. This curvature can be used to advantage to produce a trace more faithful to the original curve.

Increasing the Number of Segments for Improved Accuracy: Two function generators can be operated in parallel to give a total of 24 segments (12 positive and 12 negative) to simulate the curve. To make connections, patch together the IN, J_1, J_2 and O_1 terminals of the two instruments. Connect the external amplifiers as for one function generator only. Connect to only one O_2 terminal.

The First Line Segment: The line segment going through the origin should always be made with the first diode network (Break Control #1) which is specially biased. The other networks cannot start conducting exactly at zero because of the normal starting characteristics of a diode. They may actually be used in any other sequence, however.

If the slope of the first segment is too steep to be produced by the first network, the alternate external connection shown in Figure 33 should be used with the slope determined by adjusting the external potentiometer. None of the diode networks are used for this line segment, therefore.



Note: * Connect to J2 for Inverse Slope.

Figure 33. Special Connections for Steep Slope at Origin.

2.18 *Model 3352 – Diode Function Generator*

The initial steps in using the Model 3352, preparing a graph and determining slope and break point values, are the same as those outlined for the Model 3351. Once these preparations are complete the Model 3352 may be set up as follows.

Tabular Method

General: The maximum slope change for all segments, except the first, Kx, segment, is ±2.5 : 1. The first, Kx, segment has a maximum slope change of ±5 : 1. Breakpoints may be stacked to achieve greater slope changes.

Step 1: Set all Break-point/slope change (polarity) switches to the correct combination of polarities as determined by the function to be simulated. (See previous discussion on tabulating a function.)

Step 2: Set all Slope potentiometers to approximately center position. Set all Break-point potentiometers to one end as determined by the arrows associated with the polarity switches. (E.g., if the polarity switch is in the +BP, +ΔS or in the −BP, −ΔS position the break-point potentiometers should be set to the counter-clockwise end.) During this procedure the output amplifier may go into overload. Although no harm is being done, the computer may be placed in the Pot Set/Bal mode to prevent overload. The computer must be returned to Reset before proceeding with the adjustments.

Step 3: Set the Kx/Yo switch as determined by the function and by the following instructions:

a. The Yo potentiometer sets the value of Y when X equals zero. This value may be set anywhere within the range of plus to minus 100 volts.
b. The Kx potentiometer sets the slope of the first line segment. The Kx slope is adjustable within the range of plus to minus five (5).
c. If the Kx/Yo switch is placed in the Off position both Yo and Kx will be zero.
d. If the Kx/Yo switch is placed in the Kx position Yo will be zero, Kx will be adjustable over its range.
e. If the Kx/Yo switch is placed in the Yo position, Kx will be zero, Yo will be adjustable over its range.
f. If the Kx/Yo switch is placed in the Kx & Yo position both Kx and Yo are adjustable over their ranges.

When the switch has been set, the Yo adjustment should be made. With X = 0, the potentiometer may be adjusted for the proper value of Y_0 at the output of the Model 3352 (O_2). The Null voltmeter or a precision external meter should be used for this and all succeeding voltage adjustments in this procedure.

Step 4: The Kx adjustment should be made next. Apply the value of X at the first break-point (BP) to the input of the Model 3352. (If a potentiometer is used to obtain the X value its output should be applied through an inverter to the Model 3352. This will prevent errors due to the diode function generator loading the potentiometer.) Adjust the Kx potentiometer until the proper value of Y is obtained at the output of the Model 3352.

Step 5: The first break-point (BP) is now adjusted. Adjust the first break-point potentiometer until the Kx value previously set is offset by approximately 150 millivolts. (0.15 volts) This offset compensates for the diode characteristics and will help produce a more accurate function.

Step 6: Set the input to the value of X at the second break point. Adjust the slope potentiometer associated with the first break-point until the output is equal to the value of Y at the second break-point.

Step 7: Adjust the B.P. potentiometer associated with the next segment until the value of Y set in the preceding specification is offset approximately 150 millivolts. (See discussion in Step 5).

The remaining slope and break-point potentiometers are set alternately as indicated by the large arrows on the panel, by repeating Steps 6 and 7 until all segments have been adjusted.

Notes:
If two or more break-points are to be stacked to obtain large slope changes, the first is adjusted to offset the preceding Y value, the second to an additional offset, the third . . . The next value of X is then applied to the input and the slope potentiometers associated with the break-points adjusted to the desired value of Y.

If several Model 3352's have a common X input, only one X inverter is required. The X and -X signals may be paralleled. This may be done for up to six DEG's with common X inputs.

If all polarity switches are set to either −BP, −ΔS or +BP and −ΔS, then −X is not required and the amplifier normally connected to the J_1, O_1 patchboard terminals may be omitted. If, however, under these conditions the Kx potentiometer is to be used the O_1 terminal must be grounded.

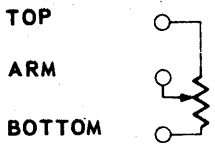
Caution: Do not ground O_1 accidentally or on purpose if an amplifier is connected to O_1, J_1.

2.19 *Coefficient Potentiometers*

The coefficient potentiometer functions as a variable voltage divider. The voltage at the output arm represents a selected fraction of the total voltage applied across the resistive element. Without a load resistor attached to the arm, the fraction would be exactly proportional to the physical displacement of the selector arm, as measured by the indicating dial. With a load element attached, there is no longer a linear relationship between the coefficient and the position of the selector arm. To avoid this difficulty, the potentiometer is correctly set with the load resistor connected by turning the dial of the potentiometer arm until the output voltage measured represents the desired fraction of the total input voltage (±100V). The dial reading is used only as a record of the correct setting but not as an indication of the actual coefficient value.

Patching the Potentiometers

Three groups of potentiometer terminals are located on each computing module. Each Model 3321, 3322A, 3325, and 3329 has one 3-terminal group, as illustrated:



All other groups are two-terminal with the bottom of the potentiometer internally grounded. The input voltage to the potentiometer is always applied to the top terminal and the output is always taken at the arm terminal.

Adjusting the Potentiometers

The potentiometers are adjusted in an identical manner whether being used as a constant voltage source, for an initial condition voltage for integrators, or to obtain a coefficient of a variable input voltage.

1. Before adjusting the potentiometer, patch it into the problem circuit so that it will be operating under actual problem loading conditions.
2. Select the number of the potentiometer to be adjusted on the address selector.
3. Potentiometers connected to Models 3320, 3321, 3322A and the IC terminal of Model 3329 may be set with the computer in the BAL/POT SET mode. These potentiometers will have +100V connected to their tops automatically. All other potentiometers should be set with the computer in the RESET mode. The reference voltage must be manually connected to the top of these potentiometers.
4. Using the Null voltmeter, set the Reference potentiometer on the control panel to the desired reading (or ratio) and adjust the individual coefficient potentiometer for a null (zero) indication on the panel meter.

   The potentiometer output voltage may also be monitored and adjusted during any operating mode. In this case, the direct reading panel meter may be used for approximate results.

The potentiometer circuitry is shown in the above illustration. The 30 kilohm potentiometer will draw 3-1/3 milliamperes which determines the limit of seven potentiometers connected to the output of any amplifier. Also note the 1/32 Amp fuse connected in series with the arm of the potentiometer. The fuse protects the potentiometer from excessive current and from accidental grounding. The fuses are mounted at the back of the potentiometers behind the front panel which tilts forward for access.

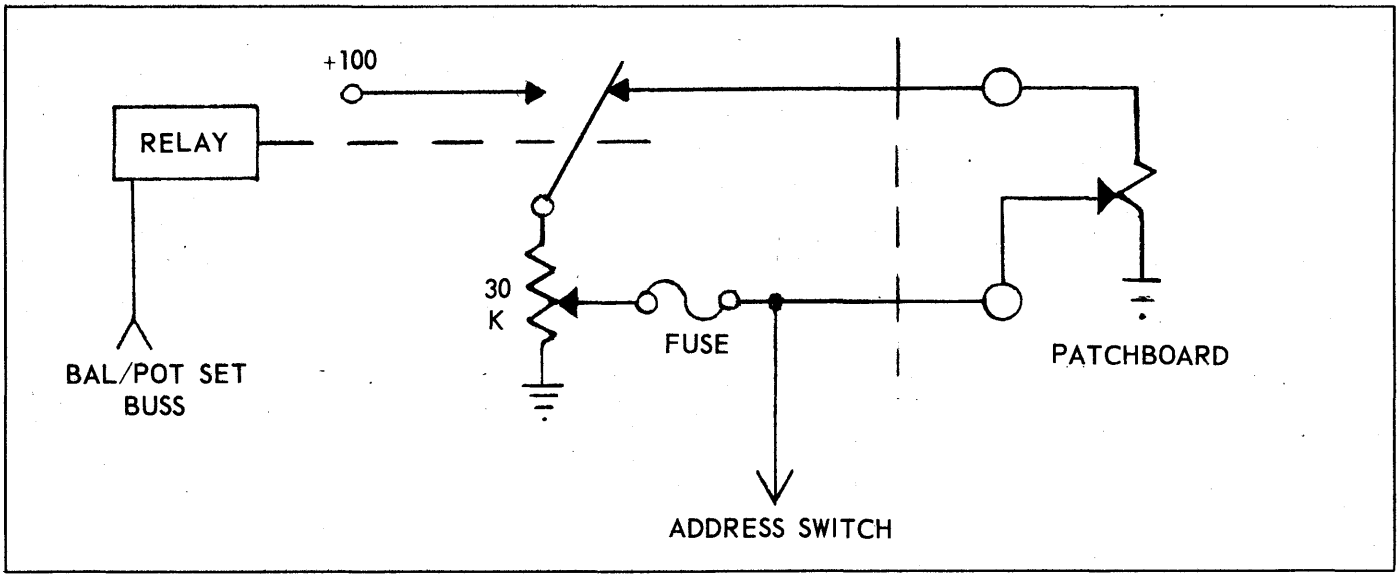


Figure 34. Typical Potentiometer Circuit

2.20 *Operation of Controls*

Turn On Procedure

The procedure for initial turn-on or turn-on from a cold start is as follows:

(1) Plug the power cord into an AC receptacle. The computer normally requires 115 V AC ±10%, but may be, if desired, connected for other voltages. To change input AC voltages follow the instructions given on the inside of the rear door of the computer. The computer will accept any AC line frequency from 50 to 400 cycles per second. A fully expanded Model 10/20 will use approximately 300 watts of power, maximum power at peak load will be approximately 550 watts.

(2) Place the Reference (REF) switch in Internal (INT). If an external reference is to be used, from another SD 10/20 for instance, a +100 volt signal must be connected. See paragraph on slaving in section 2.20 for additional instructions.

(3) Turn the main power switch on rear panel to the ON position. This will turn the +28V relay and oven power supply on. This supply should always be left on as it supplies power to the ovens which stabilize the integrating capacitors. (The capacitor values will be in error by about .1 to .2% when cold. They require approximately three hours to stabilize to the correct value).

(4) Place the computer in the BAL/POT set mode of operation. Depress the POWER switch on the control center. The computer is now on and ready to operate. If power fails to come on, check circuit breakers or AC fuses on rear panel. From a completely cold start it takes approximately three hours for all power supplies and integrator ovens to fully warm up and settle out. During this time maximum accuracies will not be realized, however, accuracy will be sufficient for all but the most critical problems.

Normally, the computer is turned on and off with the Power switch on the control center and steps one through three may be ignored. These preliminary steps need only be gone through when the computer is moved or if it has been out of service for an extended period of time.

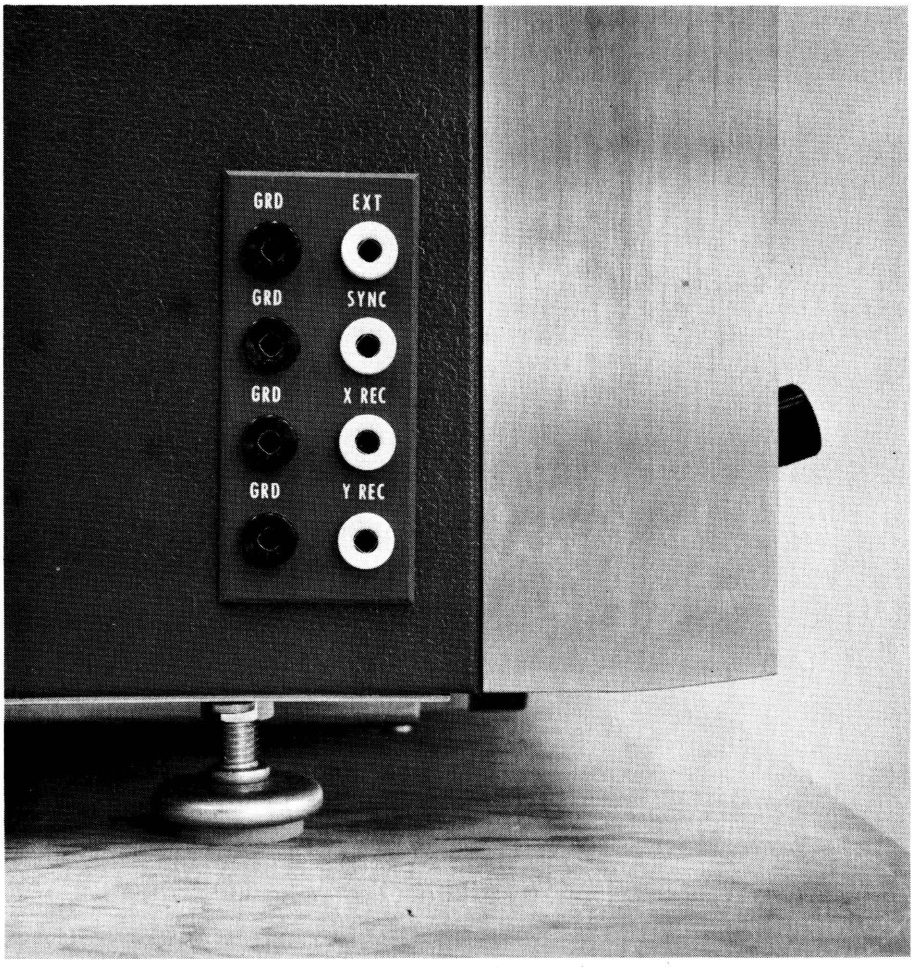


FIGURE 35. AUXILLARY OUTPUTS, MODEL SD 10/20

2.21 *General Operational Procedures*

Problem Patching

When the problem diagram is complete and all amplifiers and potentiometers assigned, the problem is ready to be patched onto the problem board. Patching is normally done with the problem board removed from the computer.

Patching may be done with the board in place if care is used. If extensive patching is to be done, put the computer in BAL/POT SET.

All unused amplifiers MUST have feedback patched around them to prevent them from drifting into saturation.

As noted before, the best approach to patching is to do the basic module patching first, then interconnect the individual modules. As a general rule use shunt plugs and multiple (squid) patchcords whenever possible as this will reduce clutter on the problem board and facilitate problem checking.

Removing and Replacing the Problem Board

The problem board may be either removed or replaced with the computer turned on or off. Care should be taken to insure that while the problem board is removed, the contact pins, now exposed, are not bent or contaminated.

Removal of Problem Board

1. Pull the arm, located to the right of the problem board, down to a horizontal position.
2. Grasp both handles of the problem board and pull down and out firmly. The top of the problem board should come out first as the bottom pivots on its cam.
3. Pull the problem board straight out.

Replacement of Problem Board

1. To replace the problem board, reverse the procedure just described.

Place the bottom of the problem board on its cam mechanism making sure it is seated properly. Push in and up firmly until the problem board locks in place. Move the arm up to the vertical position.

WARNING

The Problem Board must be in place and the arm up for the computer to operate.

Use of the Mode Controls

The mode controls are of the push button type with mechanical interlocks to prevent two contradictory modes from being energized at the same time.

As noted previously, all control in the computer is accomplished in the integrators. Thus, when a mode is energized it opens or closes a relay in each integrator. Reference to the illustration, Integrator Block Diagram, while reading the following explanations will assist in understanding the control system.

Reset

The Reset or Initial Condition (IC) mode enables the integrators to be set to their initial values before starting computation. When the Reset relay is energized an input and a feedback resistor are placed around the integrator amplifier making it, in effect, an inverter. Applying a voltage to the input resistor (in this case the IC terminal) will cause that input to appear at the output and to simultaneously charge the integrator capacitor to the same voltage. (Note: Although not shown in the illustration the Hold relay is also energized in the Reset mode.)

Potentiometers connected to Models 3322, 3323 and 3324 as inputs should also be set with the computer in the Reset mode to prevent loading errors. Potentiometers used with all other computer modules should be set in the Pot Set/Bal mode.

Compute

In the compute mode there are no energized relays. The logic is such that if the computer is not in Hold and not in Reset, it is in compute.

Hold

In the Hold mode a normally closed relay contact is opened which disconnects the input signal from the amplifier. As there is no discharge path for the integrator capacitors the output will remain at its last computed value. In this manner outputs may be read or recorded and the problem resumed at will by returning to Compute.

WARNING

The Integrators will drift while in Hold. Although the amount of drift is small a considerable error may accumulate over a period of time.

Rep-Op

In the Rep-Op (Repetitive Operation) mode the computer is automatically switched between the Reset and Compute modes of operation. This mode enables the user to obtain repetitive solutions which are easily monitored on an oscilloscope.

The amount of time the computer stays in the compute mode is determined by the setting of the Compute Time switch located at the lower left of the control center. The outer dial of the switch may be positioned in any of three ranges: .005 to .1 sec, .05 to 1 sec, and .5 to 10 sec or in the External (EXT) position. The inner dial adjusts the compute time over the range selected.

Reset time is adjusted at the rear of the computer by a thumb wheel potentiometer. The range of adjustment available is determined by the range selected on the Compute Time Switch. The three ranges for Reset are: .005 to .05 sec, .05 to .5 sec and .5 to 5 sec.

The compute and reset times may be adjusted arbitrarily by observing the solution to the problem and adjusting the times until the desired display is obtained. If more precise compute and reset times are required the Compute-Reset cycle may be observed on an oscilloscope. Connect the oscilloscope to any of the FORWARD RESET terminals on the integrators or to Test Point 6 at the rear of the computer. A rectangular waveform will be observed. The positive (+28V) portion is Reset, the negative (0V) portion Compute. The Reset and Compute time controls may then be adjusted to give the desired times.

If the Compute Time switch is placed in the External (EXT) position external circuits may be used to generate the Rep-Op cycle. The drive signals must be compatible with the logic used in the computer (+28V = True, 0V = False) and should be connected to the R (reset) and C (Compute) terminals located on the second module from the left on the problem board.

WARNING

Grounding the computer logic terminals on the integrators or other modules will destroy the relay driver transistors on the logic control board.

Bal/Pot Set

The Balance and Pot Set modes are energized by the same switch. This mode should be used when turning the computer on as it places feedback around all amplifiers automatically.

The Balance mode connects, through a relay closure, special input and feedback resistors. The values of these resistors are such that the closed loop gain of the amplifier is 2500. This high gain amplifies any error at the junction of the amplifier and allows the amplifier to be balanced more accurately.

To balance an amplifier, place the computer in the BAL/POT SET mode and select the output of the amplifier to be balanced on the address selector. Select METER and the 1 volt range. Using the special screwdriver supplied, adjust the balance potentiometer associated with the amplifier. The amplifier should be adjusted until the meter reading is within the red lines on the meter face. This will bring the junction offset to within ±40 microvolts.

Note: There will be fluctuations in the meter reading. These are normal and should be ignored.

The Pot Set mode disconnects the summing junction of the amplifier from the junction. At the same time it grounds the summing junction and loads any potentiometers connected to the input resistors. **This mode is included in Models 3320, 3321, 3322A, 3325 and 3329 (IJ) only.** As previously noted all other models should have the potentiometers associated with their inputs set with the computer in Reset.

Power

The POWER on-off switch is the normal means of turning the computer on and off. It turns off all power to the amplifiers. It does not turn the +28 volt oven and relay supply off. The main power switch in the rear should be left on unless the computer is to be out of use for a long period of time.

Oven

This light is on whenever the +28 volt oven and relay supply is on. It must be on before the POWER on-off switch can be used.

OL Hold – OL Reset

When engaged, the Overload Hold portion of this switch will cause the computer to automatically switch to the Hold mode at the occurrence of an overload in any amplifier. When the overload is found and eliminated, the switch is re-engaged to reset the overload hold circuitry.

If an overload occurs, the light within the OL Hold /OL Reset will begin to blink on and off and will continue to do so until the overload is removed.

Power Supplies

The +28V relay and oven and the ±112V power supplies are protected against excessive output voltage. One or more of these voltages will go to zero if the computer AC line input voltage is momentarily or continuously excessive. These voltages may be restored by turning off the main power switch at the rear or the POWER on-off switch, as appropriate, and observing the same procedures as for a power interruption.

Time Scale

The Time Scale switch determines which of the integrator capacitors connected to the A and B terminals on the integrator modules is in the circuit. With the Time Scale switch not engaged, the capacitor connected to the A terminal is in the circuit. When the Time Scale switch is engaged the capacitor connected to the B terminal is in the circuit. Any two of the three available capacitors may be patched to the A and B terminals. If time sealing is not required the capacitors may be patched directly to the output.

Slave

If two Model SD 10/20s or a Model SD 10/20 and a Model SD 40/80 are to be operated together the SLAVE switch should be engaged on the unit that is to be a slave except that an SD 10/20 cannot operate as a master for an SD 40/80. This unit will then be controlled by the other (master) unit. To complete the control circuits, a special cable must be constructed. The connectors necessary are included in the accessory kit that accompanies the computer. The schematic section of this manual contains a drawing outlining the construction of the slaving cable. Consult the factory for information when more than two SD 10/20s are to be operated together or when remote control is required.

Note that the Slaving Cable does not connect the ground terminals of the two computers together. Always be sure the computer cabinet grounds are electrically interconnected through the third (ground) wire in the power cord, or for best results, use a line isolation plug on one of the two computers and electrically connect the cabinets together using a heavy ground strap or wire. This ground connection is also the ground return for slaving the 100 volt power supplies.

Amp-Pot Select

The Amp-Pot Select switch connects either the output of an amplifier or the arm of a potentiometer to the meter circuit. Each 'address' is a two digit number. Thus to read the output of amplifier No. 9 select 0 in the AMP section of the outer dial and select 9 on the inner dial. To read the arm of potentiometer No. 12 select 1 in the POT section of the outer dial and select 2 on the inner dial.

Meter Select

The inner dial of the meter select switch determines which meter function the selected 'address' is routed to: The available meter functions are as follows:

Meter, the addressed voltage is connected for normal voltmeter operation.

– Null and + Null, the addressed voltage is connected to a null meter circuit. The REFERENCE POTENTIOMETER is connected to the other side of the meter with the + or – 100 volt reference applied to its top. The Reference Potentiometer is then adjusted until the meter indicates a null. The setting of the Reference Potentiometer is equal to the addressed voltage.

EXT (External) in this function the addressed signal is connected to the EXT jack on the left side of the computer where it may be read out on an external device.

The Meter Range Switch functions as a sensitivity switch (maximum sensitivity at "1V") when the meter FUNCTION switch is in the +NULL or –NULL function. The null meter will read less than full scale with any Reference Potentiometer setting and address voltage, when the RANGE switch is set to the 300V position, so that the operator can determine if he is adjusting toward or away from null.

Reference Potentiometer

The Reference Potentiometer, as previously noted, is used in conjunction with the Null functions of the meter. The Reference Potentiometer is connected to the opposite side of the meter from the input signal and has either the plus or minus 100 volt reference connected to its top. As the resistance of the Reference Potentiometer is 10 kilohms when the arm of the Reference Potentiometer is set to a point where the current through the meter is zero (null point), the setting of the Ref. Pot is proportional to the input voltage. Thus a Ref. Pot setting of 56.20 is equal to 5.620 kilohms from the arm of the Ref. Pot to the bottom (ground) of the Ref. Pot and is also equal to the voltage applied to the other side of the meter. Consequently, a reading of 56.20 on the Ref. Pot indicates an input voltage of 56.20 volts.

Special Trunklines

There are six special trunklines located on the problem board of the Computer. These are located on the first and third modules from the left. The first module contains the M, X and Y special trunk lines and the third module contains the H, C and R special trunklines. The special trunklines are used as follows:

M: This line is connected to the panel meter or the EXT jack as determined by the position of the Meter Select Switch. If the Meter Select Switch is in the METER function the M line is connected to the EXT jack; if the Meter Select Switch is in the EXT function, the M line is connected to the panel meter. One special condition exists. With the Meter Select switch in Meter and address A00 selected the M line is connected to the meter.

X & Y: The X and Y lines are connected directly to the X and Y terminals on the left side panel of the computer. These lines are intended for use with an X-Y plotter but may be used to connect signals to any external device or they may be used to connect external inputs into the computer.

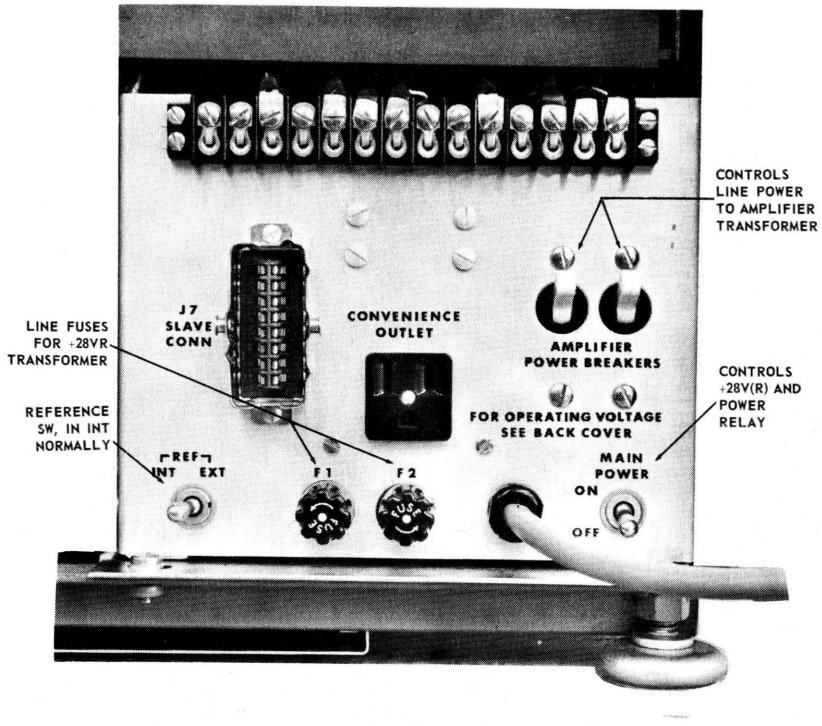


Figure 36. POWER CONTROL PANEL

NOTE: SD 10/20's S/N 124 and above have fuses rather than circuit breaker in the amplifier power line.

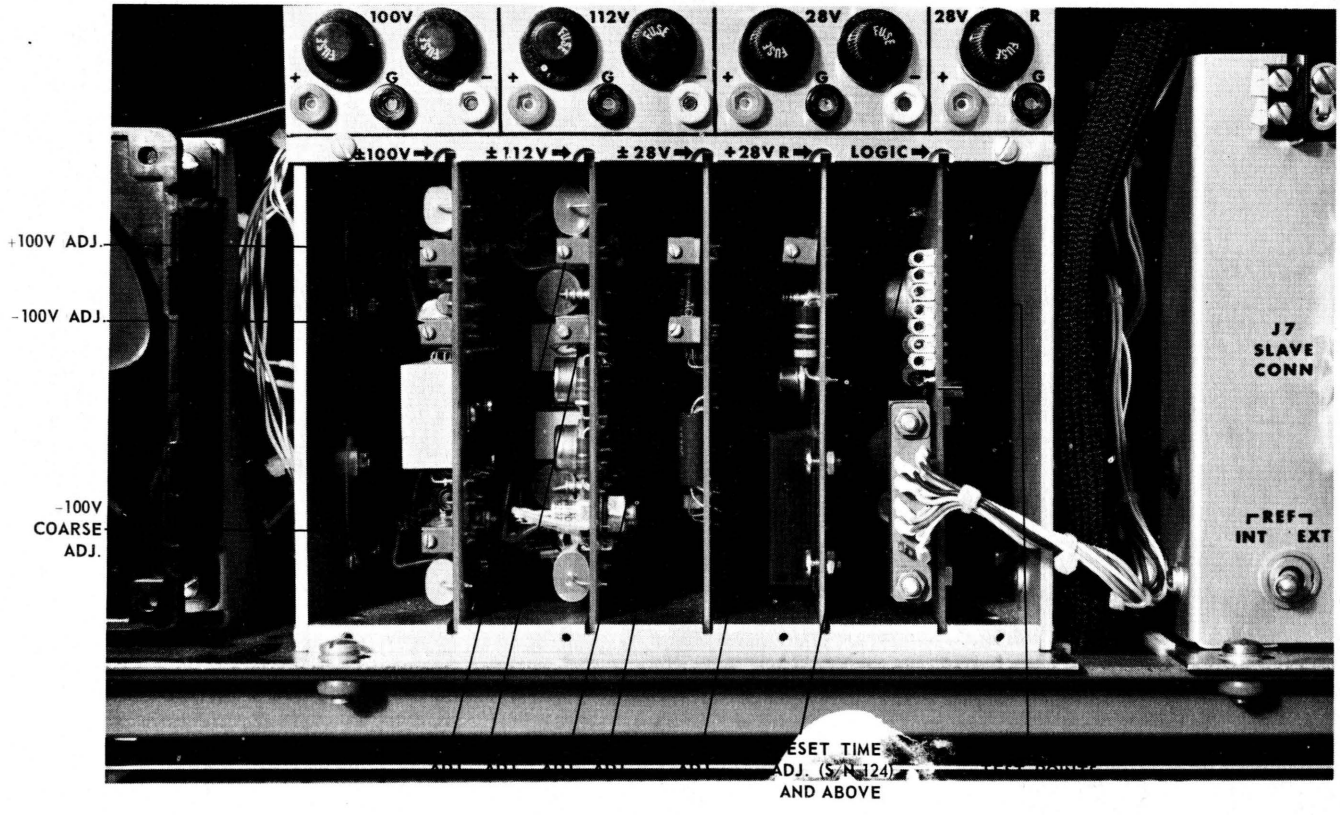


Figure 37. LOGIC CONTROL AND POWER SUPPLY ADJUSTMENTS

H, C & R: The H (Hold), C (Compute), and R (Reset) lines are used as external input lines to the Control Logic circuitry. A logical 1 applied to any of the lines will place the computer in that mode of operation. To use these lines the computer must be in REP-OP and the Compute Time switch must be in EXT.

2.21 Special Operating and Protective Features

Power

A power interruption to all or part of the computer, whether due to external causes, blown fuses, operation of the main power switch, operation of the POWER on-off switch or operation of the problem board interlock switches should be followed by a pause of fifteen to thirty seconds before the power is reapplied. An insufficient delay will result in incomplete restoration of computer operating voltages.

Continuous or repeated overloading or short circuiting of any of the power supplies is not recommended. A power supply voltage that is lost, however, because of accidental overloading or short circuiting may be restored simply by first turning off the main power switch or the POWER on-off switch, as appropriate, and observing the same procedures as for a power interruption.

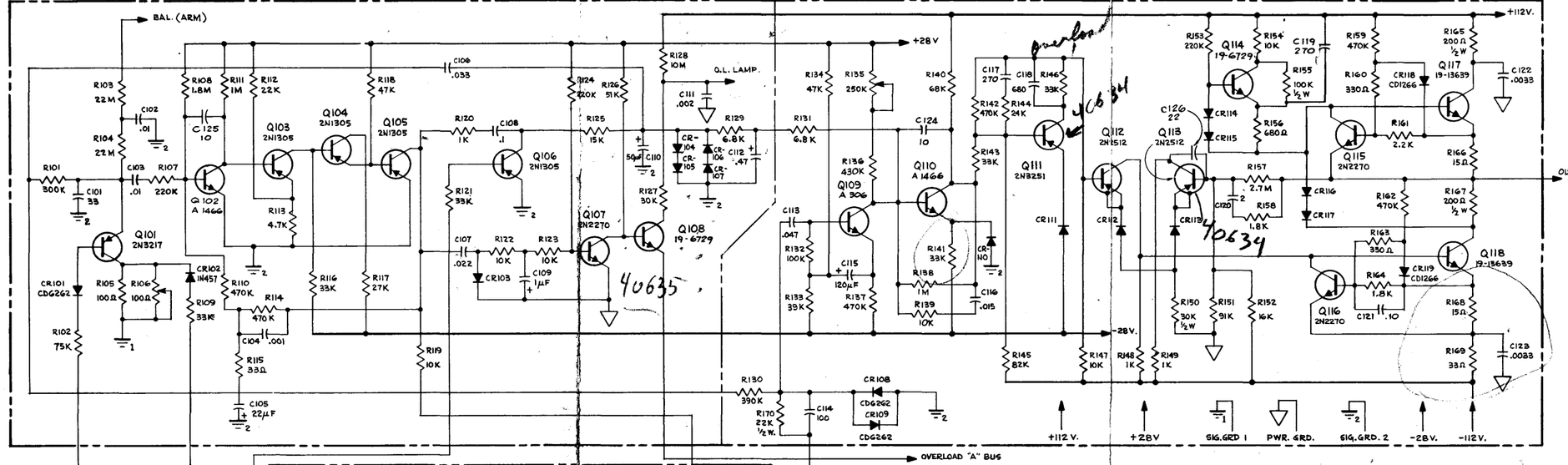
Cooling

Protective circuitry is included which has much the same effect as turning off the POWER on-off switch. This circuitry will operate if there are excessive loads on the ±112V power supplies, if the ambient air temperature is excessive or if the cooling airflow is severly restricted for any reason. Normal operation may be resumed by correcting the problem and observing the same turn-off and turn-on procedures as for power supply short circuits except that the pause should be one minute or more.

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY.
PILOT LOT EVALUATION		B	9/21/64	JBG

"A" AMPLIFIER

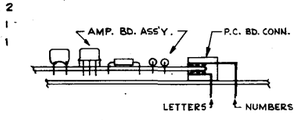
CHOPPER — A.C. AMPLIFIER — DEMODULATOR — OVERLOAD AMPLIFIER — WIDE BAND AMPLIFIER



"B" AMPLIFIER (SAME AS "A" AMPLIFIER ABOVE)

DETAIL No's. OF COMPONENTS ON "B" AMPLIFIER; ALL IN 200 SERIES

AMP "A"	BAL (ARM)	Ⓐ +112V
	LAMP	Ⓑ +28V
		Ⓒ SIG. GRD. 2
	JUNCTION	Ⓓ SIG. GRD. 1
		Ⓔ " " 1
	PWR. GRD.	Ⓕ
	OUTPUT	Ⓗ
	"	Ⓙ -28 V.
	"	Ⓚ -112 V.
	(+) BAL.	Ⓛ
	O.L. BUS	Ⓜ
AMP "B"	BAL (ARM)	Ⓝ +112V
	O.L. LAMP	Ⓟ +28V
		Ⓡ SIG. GRD. 2
	JUNCTION	Ⓢ SIG. GRD. 1
		Ⓣ " " 1
	PWR. GRD.	Ⓤ
	OUTPUT	Ⓥ
	"	Ⓦ -28 V
	"	Ⓧ -112 V
	(-) BAL.	Ⓨ
	O.L. BUS	Ⓩ



NOTE:- UNLESS OTHERWISE SHOWN ~

1. ALL RESISTORS ¼W. 5% COMP. CARBON.
2. ALL DIODES TYPE IN463.
3. ALL CAPACITOR VALUES GREATER THAN 1 IN µµF's.
4. REF: CHECKOUT PROCEDURE DWG. 14593.
5. R161 & R164 MAY BE SELECTED FOR OPTIMUM SHORT CKT PROTECTION.

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	MFR'S PART NO.

DRAWN		DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE X .XX .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD CALIFORNIA
CHECK		DATE		
ELEC.		DATE		
MFG.		DATE		
QUALITY APPROVAL		DATE		
3310	12371	SCALE	DO NOT SCALE DRAWING	DWG SIZE D
USED ON	NEXT ASSY			SHT 1 OF 1
APPLICATION				

MATERIAL: SEE PARTS LIST 12371

SCHEMATIC, DUAL HIGH GAIN AMPLIFIER MODEL 3310

A-No. 11293 REV. B

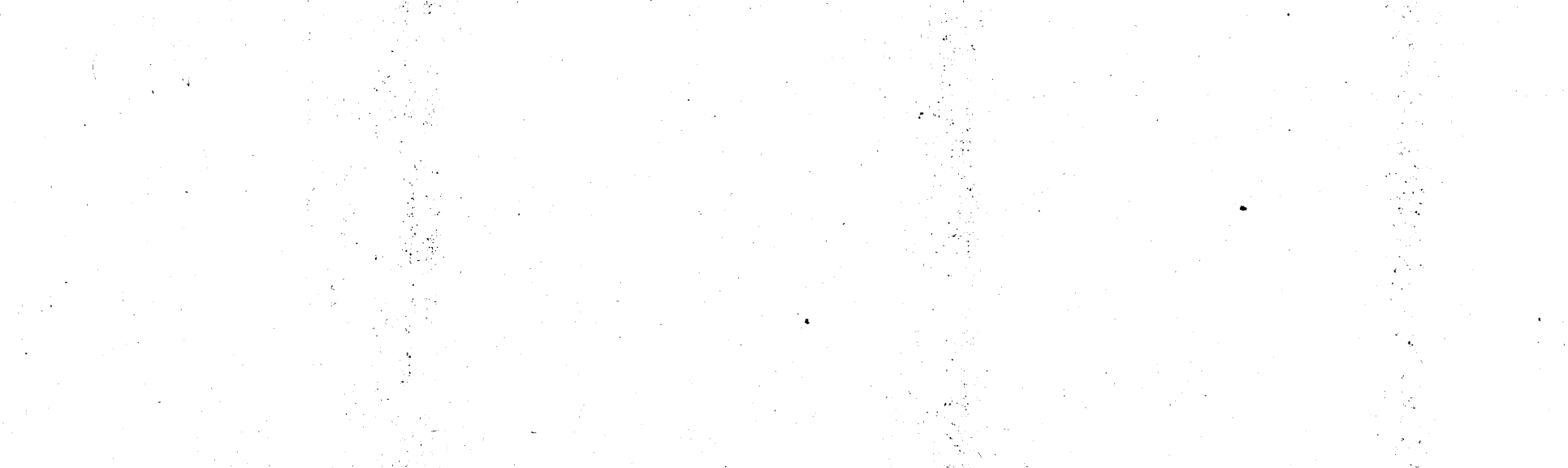
14857

PNP SK3114

33K

4712

REVISIONS					
ISSUE	DESCRIPTION	SER. NO.	ECO NO.	DATE	APP. BY:
XP-6	REVISED	—	—	7/30/64	
B	PILOT LOT EVALUATION	—	—	4/9/69	



NOTES:

1 - R111 & R112 ARE FACTORY SELECT RESISTORS. STARTING VALUES ARE SHOWN.

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

SD 40/80	12549-1		
USED ON	NEXT ASSY		
APPLICATION			

DRAWN OLSON 11-7-64 DATE
CHECK 8-3-64 DATE
ELEC. 8-3-64 DATE
MECH. DATE
PROJECT 8-3-64 DATE
APPROVAL 11-11-64 DATE
SCALE — DO NOT SCALE DRAWING
DWG SIZE B
SH 2 OF 2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X
.XX —
.XXX
ANGLES ±

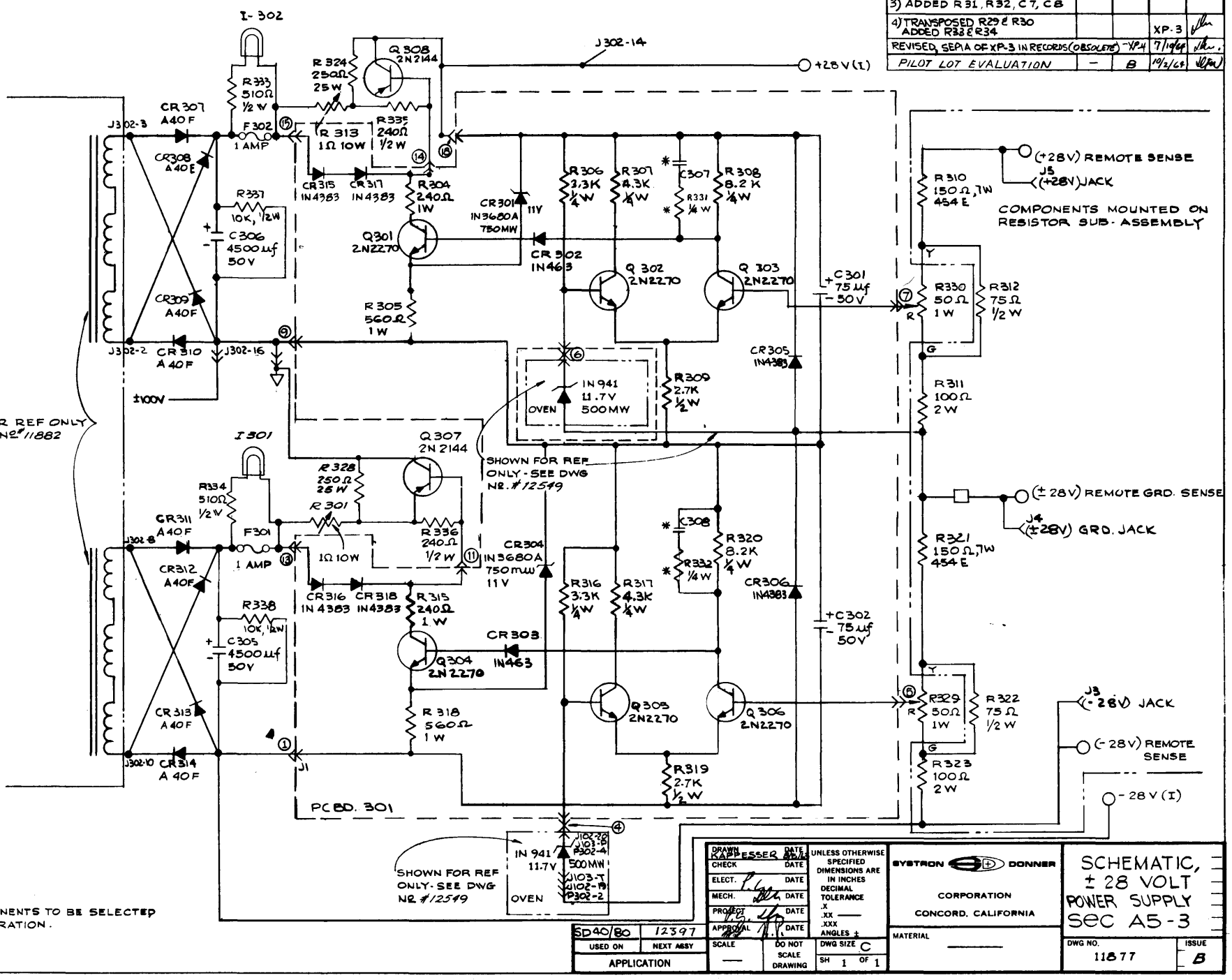
SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA

MATERIAL

SCHEMATIC- ±100V REFERENCE SUPPLY & OVEN SECTION A5-1

DWG NO. 12549 ISSUE B

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
1) CHANGED VALUES OF R10, 11, 12, 21, 22, 23 & RELOCATED FROM P.C. BOARD TO CHASSIS.				
2) CHANGED R4, R15 FROM 1/2 WATT TO 1 WATT	—	—	XP-2	
3) ADDED R31, R32, C7, C8				
4) TRANSPOSED R29 & R30 ADDED R33 & R34			XP-3	
REVISED, SEPIA OF XP-3 IN RECORDS (OBSOLETE)	-XP4		7/19/64	
PILOT LOT EVALUATION	—	B	10/2/64	

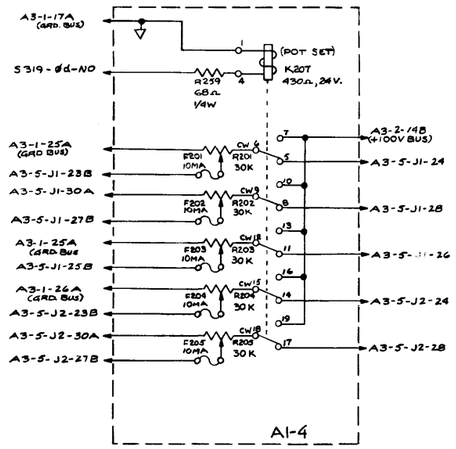


1-* THESE COMPONENTS TO BE SELECTED DURING CALIBRATION.

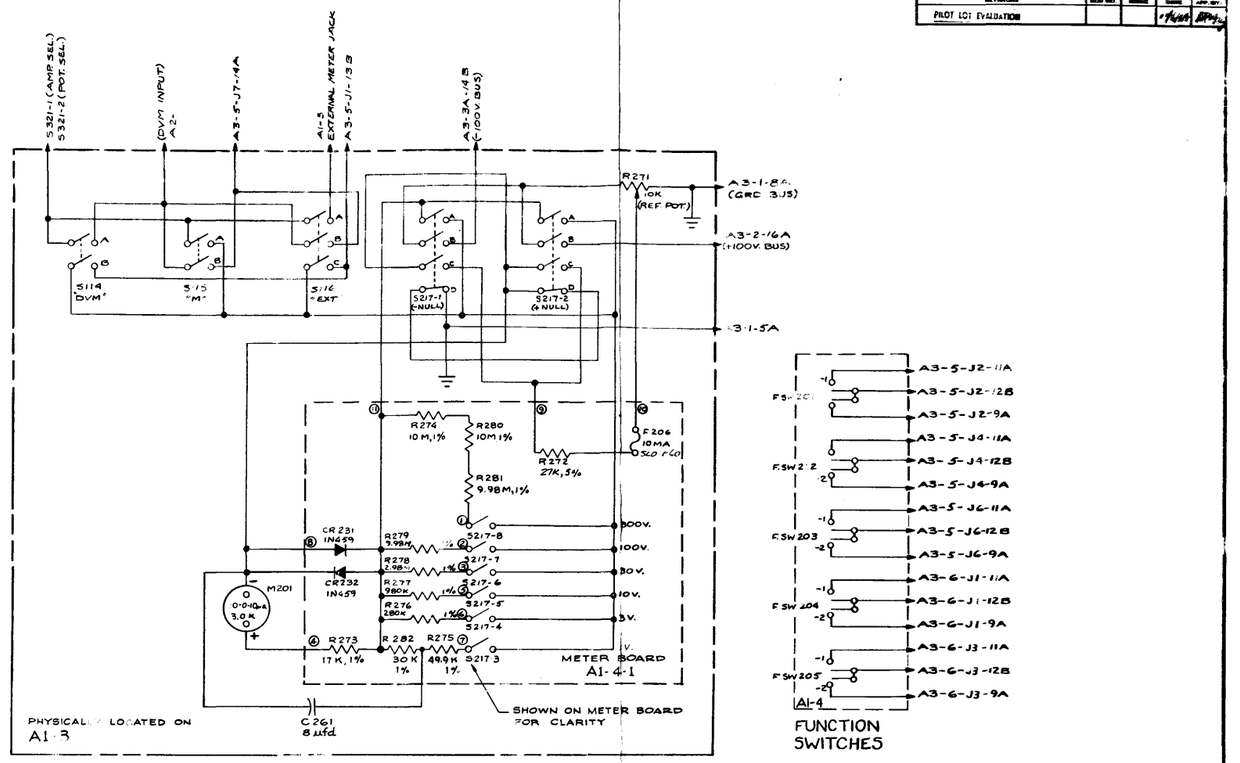
NOTES

DRAWN KAPPESSER DATE 8/5/64	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX —— .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	SCHEMATIC, ± 28 VOLT POWER SUPPLY Sec A5-3
CHECK DATE			
ELECT. DATE			
MECH. DATE			
PROJECT DATE			
APPROVAL DATE		MATERIAL ——	DWG NO. 11877 ISSUE B
SD40/80 12397 USED ON NEXT ASSY	SCALE —— DO NOT SCALE DRAWING	DWG SIZE C SH 1 OF 1	
APPLICATION			

REVISIONS	ECO NO.	REMARKS	DRAWN	APP. BY
PILOT LOT EVALUATION				



POTENTIOMETERS 1 TO 5



METER CIRCUITRY

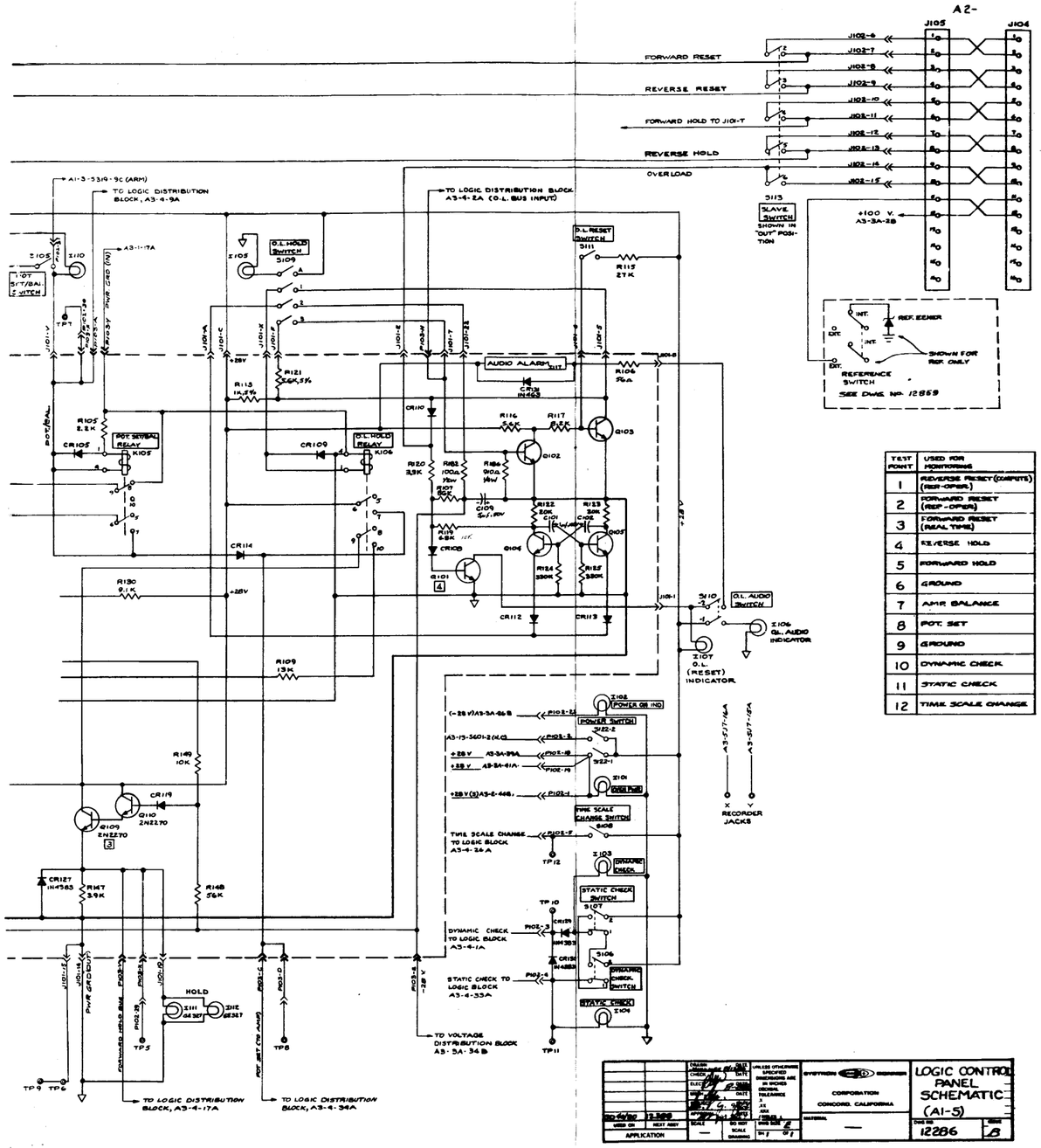
FUNCTION SWITCHES

2. REFERENCE :- UNIT IDENTIFICATION DWG # 15026

1. SWITCH GROUPS S114, S115, S116 & S117 ARE MECHANICALLY INTERLOCKED.

NOTES:

DRAWN BY: J.CUMMINGS	DATE 8/17/64	UNLESS SPECIFIED DIMENSIONS ARE IN	
CHECKED BY:	DATE	TOLERANCES: DECIMAL ANGULAR	
PROD. ENGR.	DATE	SURFACE FINISH	SCT. NO. / ITEM / MATERIAL / DWG./UNIT
APPROVED BY:	DATE	SCALE	CONCORD CALIFORNIA
MODEL: 5D 40/80	NEXT ASSEM: 12388	TITLE: METER PANEL SCHEMATIC SECTION A1-4	DWG. NO. 14921 / ISS-LTR B



TEST POINT	USED FOR MONITORING
1	REVERSE RESET (CONTACTS) (REF-OPER.)
2	FORWARD RESET (REF-OPER.)
3	FORWARD RESET (REAL TIME)
4	REVERSE HOLD
5	FORWARD HOLD
6	GROUND
7	AMP BALANCE
8	POT. SET
9	GROUND
10	DYNAMIC CHECK
11	STATIC CHECK
12	TIME SCALE CHANGE

		DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	LOGIC CONTROL PANEL SCHEMATIC (A1-5)
		CHECK	DATE	DECIMALS TOLERANCE .X ±.1 .XX ±.05 .XXX ±.010		
		ELEC. ENG.	DATE			
		MECH. ENG.	DATE			
30-64/80	3-1868	APPROVED	DATE		MATERIAL —	DWG NO. 12886 REV. B
USED ON	NEXT ASSY	SCALE —	DO NOT SCALE DRAWING	SHEET 1 OF 1		
APPLICATION						

A2-

TEST POINT	USED FOR MONITORING
1	REVERSE RESET (COMPUTE) (REP-OPER.)
2	FORWARD RESET (REP-OPER.)
3	FORWARD RESET (REAL TIME)
4	REVERSE HOLD
5	FORWARD HOLD
6	GROUND
7	AMP. BALANCE
8	POT. SET
9	GROUND
10	DYNAMIC CHECK
11	STATIC CHECK
12	TIME SCALE CHANGE

UNIT IDENTIFICATION #1502G

6. REFERENCE DWGS:-
LOGIC CONTROL PANEL ASS'Y #12988
METER PANEL SCHEMATIC-DWG 14931.
TYPICAL L.T.T.B. SWITCH WIRING, ADDRESS SELECTOR-DWG 14920.
RELAYS SHOWN IN DE-ENERGIZED POSITION
USE IRC TYPE MHW-HEAT DISSIPATORS.
USE WAKEFIELD TYPE NF-209 HEAT DISSIPATORS.
POT. CONTROL RELAY BUS - DWG. 12925

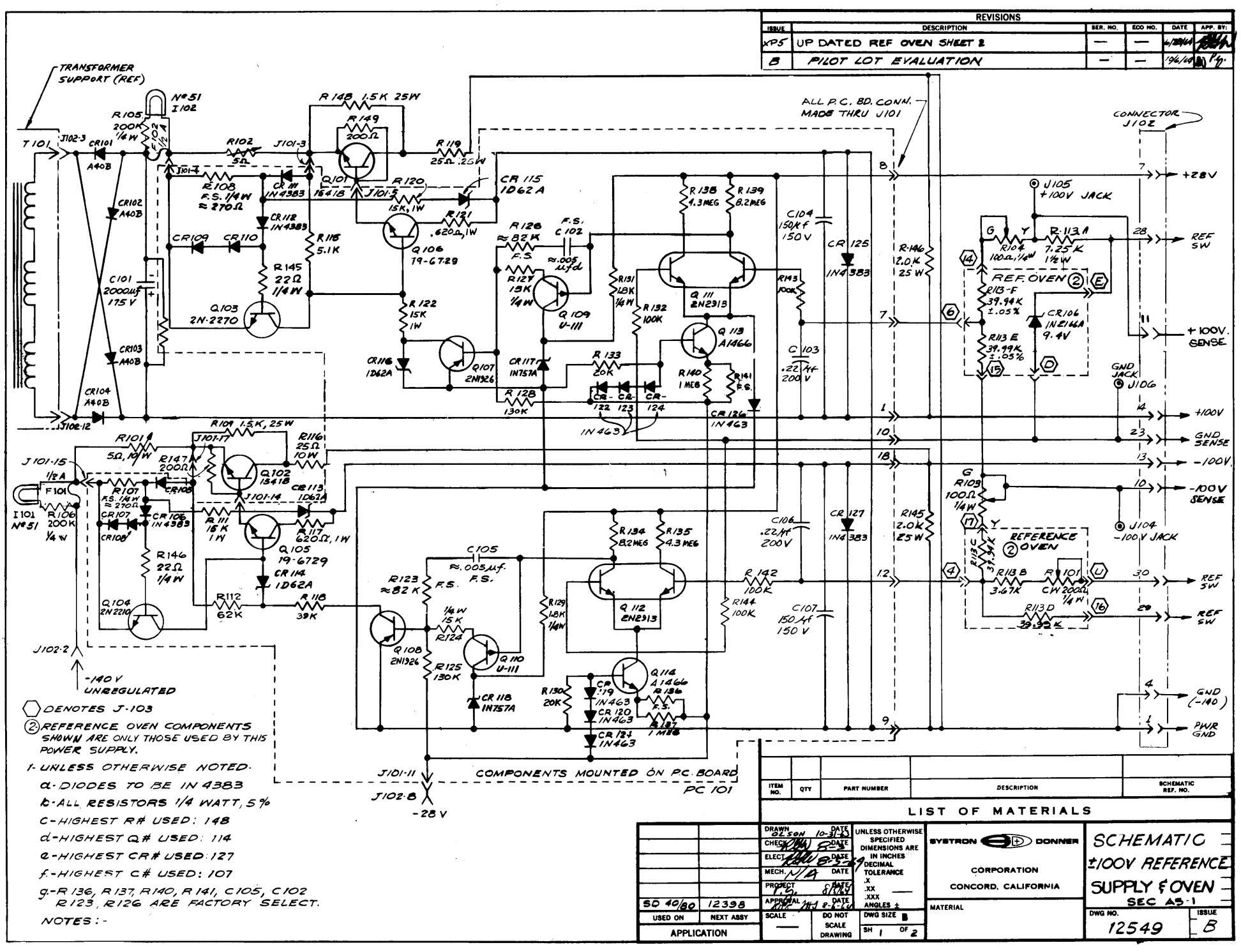
7. UNLESS OTHERWISE NOTED-RESISTORS, COMP CARB., ½W, ±5%
TRANSISTORS, 2N2270
DIODES, IN463
LAMPS GE 327

NOTES:

TRUNKLINE (RESET A3-5-XX-15 D)
TRUNKLINE (COMPUTE A3-5-XX-16 A) } EXT. REP OPER. DRIVE.

		DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE x ±.1 xxx ±.005 ANGLES ± 1°	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	LOGIC CONTROL PANEL SCHEMATIC (A1-5)	
		CHECK	DATE				
		ENG	DATE				
		APPROVED	DATE				
30-44/80	12-3080	SCALE	DO NOT SCALE DRAWING	SHT 2 OF 2	MATERIAL —	DWG NO. 12286	REV. B
USED ON	NEXT ASSY						
APPLICATION							

REVISIONS					
ISSUE	DESCRIPTION	SER. NO.	ECO NO.	DATE	APP. BY:
XP5	UP DATED REF OVEN SHEET 2	—	—	4/22/64	
B	PILOT LOT EVALUATION	—	—	1/16/64	Fig.



⬡ DENOTES J-103

(2) REFERENCE OVEN COMPONENTS SHOWN ARE ONLY THOSE USED BY THIS POWER SUPPLY.

1- UNLESS OTHERWISE NOTED.
- a- DIODES TO BE IN 4383
- b- ALL RESISTORS 1/4 WATT, 5%
- c- HIGHEST R# USED: 148
- d- HIGHEST Q# USED: 114
- e- HIGHEST CR# USED: 127
- f.- HIGHEST C# USED: 107
- g.- R 136, R 137, R 140, R 141, C 105, C 102 R 123, R 126 ARE FACTORY SELECT.

NOTES: -

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

SD 40/80	12398
USED ON	NEXT ASSY
APPLICATION	

DRAWN O.L.SON 10-31-63 DATE
CHECK [illegible] DATE
ELECT. [illegible] 8-2-64 DATE
MECH. N/A DATE
PROJECT L.D. 8/11/64 DATE
APPROVAL [illegible] 8-2-64 DATE
SCALE — DO NOT SCALE DRAWING
DWG SIZE B
SH 1 OF 2

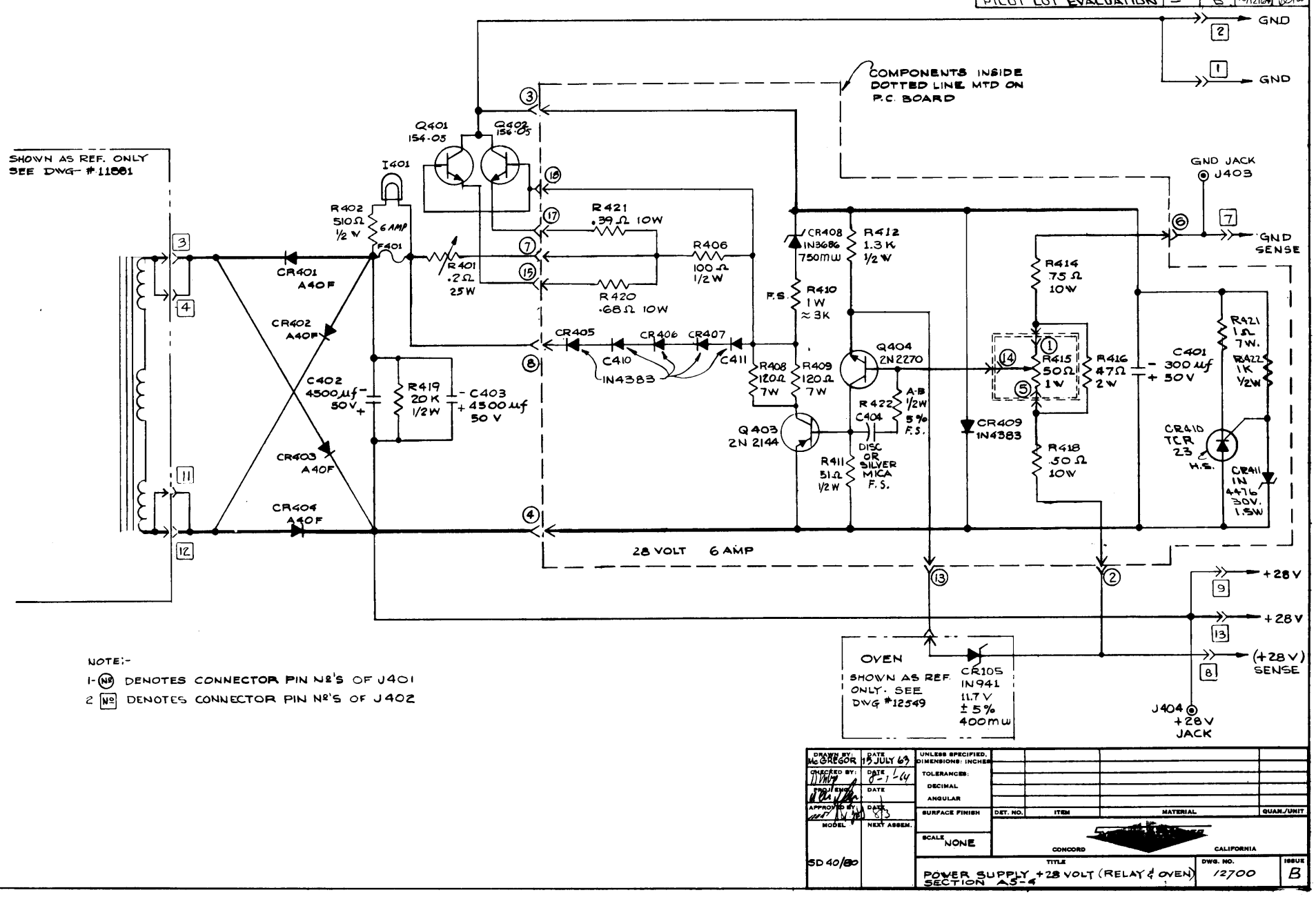
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE .X ± .XX — .XXX ANGLES ±

SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
MATERIAL

SCHEMATIC ±100V REFERENCE SUPPLY & OVEN SEC A5-1

DWG NO. 12549
ISSUE B

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
1) RETURNED R 16 & R17 TO "REMOTE SENSE" INSTEAD OF +28	–	XP-2	9/30/69	
2) RETURNED R 13 & 14 TO "GRD SENSE" INSTEAD OF "POWER GRD"	"	"	"	
3) ADDING CKT SYMBOLS TO CAPACITORS	"	"	"	
4) CHANGING PIN CONNECTIONS TO COMPLY WITH XP-2 PC BOARD	"	"	"	
PILOT LOT EVALUATION	–	B	10/12/69	



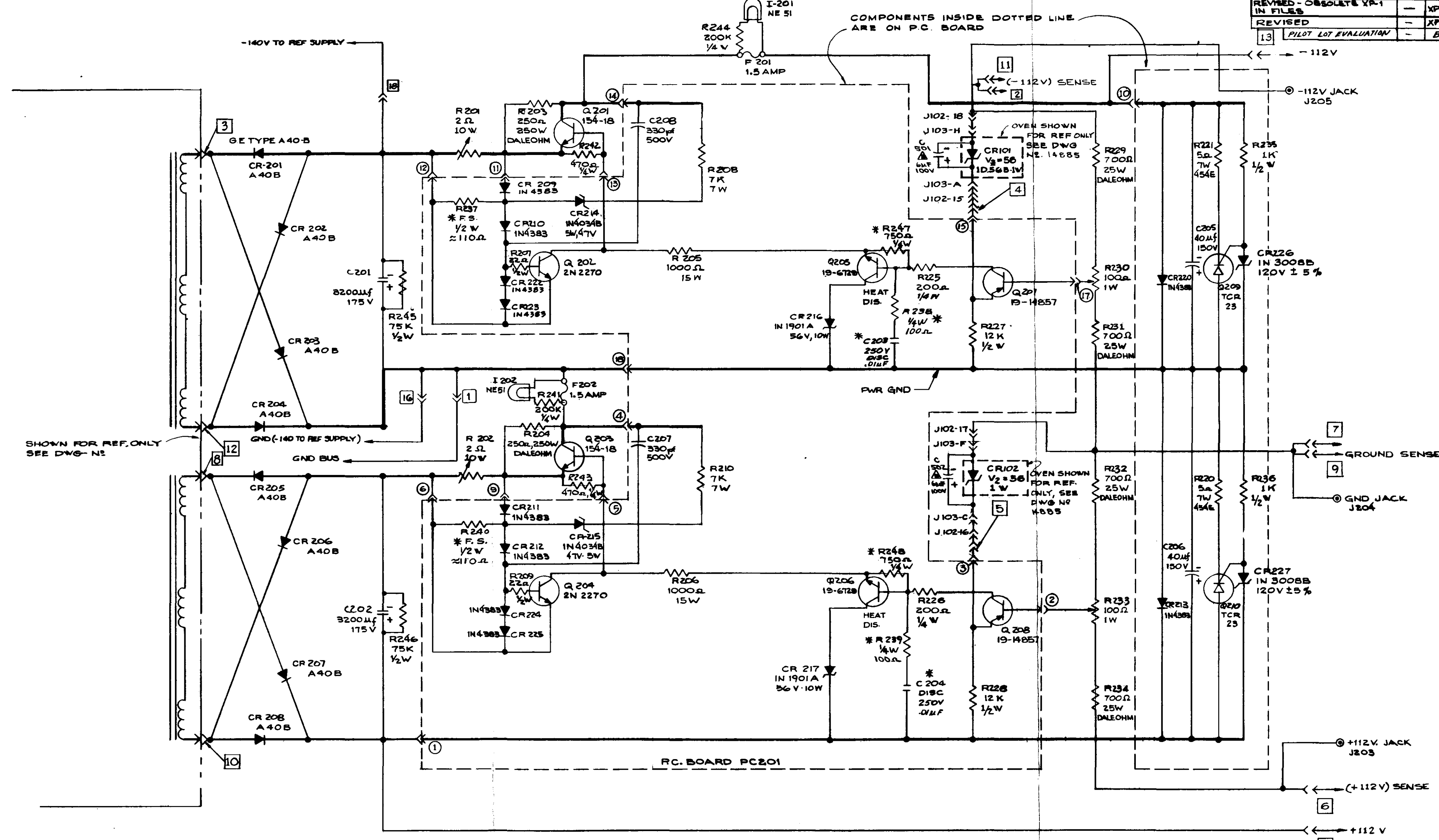
NOTE:-

1- (№) DENOTES CONNECTOR PIN №'S OF J401

2 [№] DENOTES CONNECTOR PIN №'S OF J402

DRAWN BY: McGREGOR	DATE 12 JULY 69	UNLESS SPECIFIED, DIMENSIONS: INCHES			
CHECKED BY:	DATE 8-1-69	TOLERANCES: DECIMAL			
ENGR'G APPR.	DATE	ANGULAR			
APPROVED BY:	DATE 8/5	SURFACE FINISH	DET. NO.	ITEM	MATERIAL / QUAN./UNIT
MODEL SD 40/80	NEXT ASSEM.	SCALE NONE	CONCORD, CALIFORNIA		
TITLE: POWER SUPPLY +28 VOLT (RELAY & OVEN) SECTION A5-4		DWG. NO. 12700	ISSUE B		

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
REVISED - OBSOLETE XP-1 IN FILES	—	XP-2	7/10/64	
REVISED	—	XP-3	7/30/64	
13 PILOT LOT EVALUATION	—	B	9/4/64	



▲ DENOTES MOUNTED ON CABINET WALL.

✱ DENOTES FACTORY SELECT. STARTING VALUES SHOWN

(Nº) DENOTES PC CONN (J201)

[Nº] DENOTES CHASSIS CONN (J202)

HIGHEST R
C-208
CR 227
Q-210
J-205
F-202
I-202
PC-201

DRAWN BY: McGREGOR	DATE 15 JULY 64
MODEL SD 40/80	NEXT ASSEM. 12396
SCALE	NONE

AS-2

SCHEMATIC - ±112 VDC POWER SUPPLY — DWG. NO. 12709 — ISSUE B

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
PILOT LOT EVALUATION	—	B	9/6/66	

P 102
± 100 V
REFERENCE POWER SUPPLY
(A5-1)
POWER SUPPLY REFERENCE OVEN

P 202
± 112 V
POWER SUPPLY
(A5-2)

P 302
± 28 V
POWER SUPPLY
(A5-3)

(A5-4)
P 402
+ 28 V
OVEN/RELAY POWER SUPPLY

B (A5-5) TRANSFORMER TERMINAL

'C' (A5-5) TRANSFORMER TERMINAL

'D' (A5-5) TRANSFORMER TERMINAL

T-101 AMPLIFIER POWER SUPPLIES TRANSFORMER

T-102 OVEN AND POWER RELAY SUPPLY (A5-5)

'A' (A5-5)

POWER GROUND AND POWER SUPPLY DISTRIBUTION
(A3-1)
(A3-2)
(A3-3A)
(A3-3B)

C501 6 µf
C502 6 µf
C504 39 µf
C503 39 µf

104 VAC

BLOWER
DVM

K501 AMR POWER RELAY

+100V BUS

J104-11 J104-12 SLAVE CONNECTOR

THERMO CUTOUT S303

S601-B PROB. BD. INTERLOCK SW.

PWR. SW (CONT. CTE.)

+28V(R) FROM CONTROL CENTER

+28V(R) SENSE TO CONTROL CENTER

10 AMR POWER CIRC BREAKERS

MAIN POWER SWITCH

117 VAC

S601-1

F1 1.6A SLO BLO

F2 1.6A SLO BLO

18Ω 3W 18Ω 3W

D1 D2

L502 L503

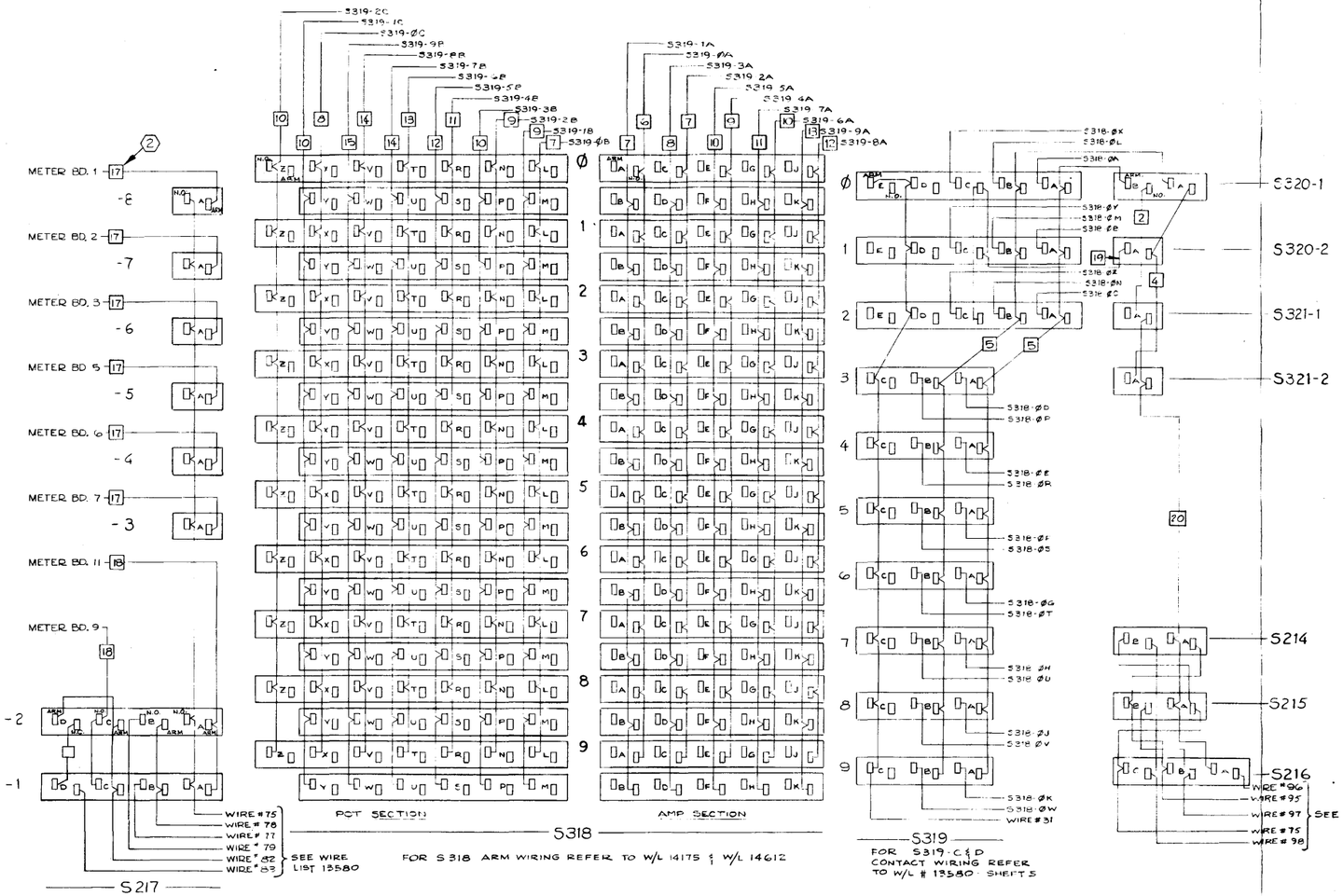
PROB. BD. RELEASE SOLENOIDS

REFERENCE SWITCH

EXT. INT. INT. EXT.

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE X .XX .XXX ANGLES ±	EVTRON DONNER CORPORATION CONCORD, CALIFORNIA	BLOCK DIAGRAM POWER SUPPLIES	
CHECK	DATE				
ENGR.	DATE				
MECH.	DATE				
PROJECT	DATE				
APPROVAL	DATE				
SCALE NONE	DO NOT SCALE DRAWING	DWG SIZE D	MATERIAL	DWG NO. 12859	ISSUE B
SD 50/80	12400	SH 1 OF 1			
USED ON	NEXT ASSY				
APPLICATION					

REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
REDRAWN	—	XP2	6/30/64	
" "	—	B	9/23/64	



(2) NUMBERS ☐ REFER TO TYPE Nos ON WIRE PREPARATION LIST 14814

1. REF: WIRE PREPARATION LIST Nº 14814

NOTES:

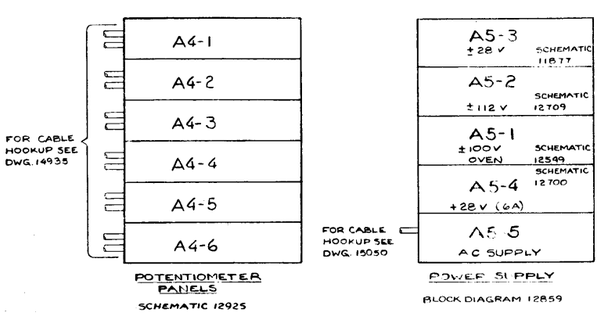
DRAWN BY: [illegible]	DATE 6/30/64	UNLESS SPECIFIED DIMENSIONS ARE IN INCHES				
CHK'D BY: [illegible]	DATE 7-10-64	TOLERANCES:				
PROJ. ENGR.: [illegible]	DATE 7-10-64	DECIMAL —				
APPROVED BY: [illegible]	DATE 7-10-64	ANGULAR —				
MODEL	ASSEM	SURFACE FINISH —	DET. NO.	ITEM	MATERIAL	QUAN./UNIT
50 80	12591	SCALE —				

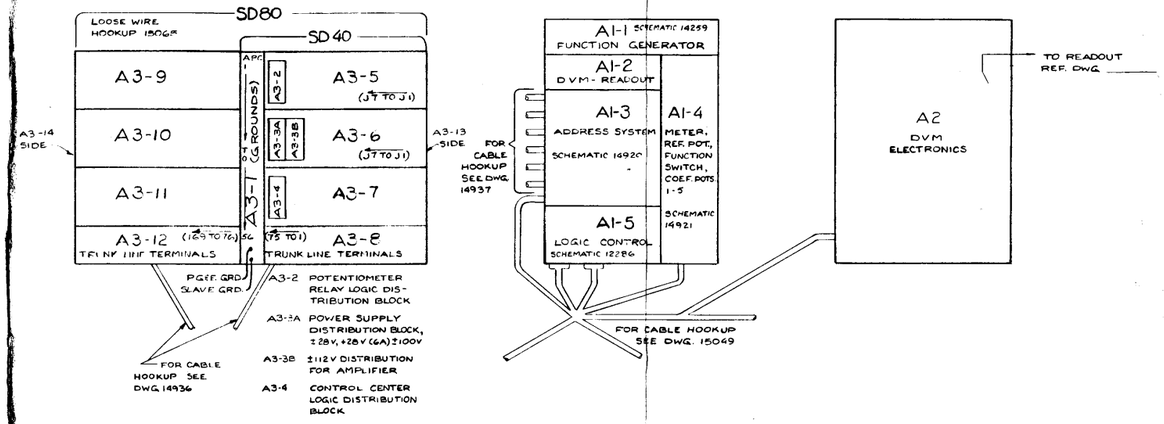
CONCORD CALIFORNIA

WIRING DIAGRAM, ADDRESS SELECTOR

DWG. NO. 13553 | GROUP B

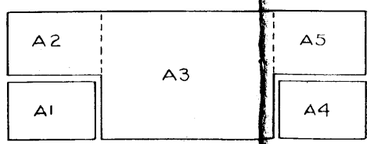
REVISIONS	ECO NO.	ISSUE	DATE	APP. BY
		E	- -	DW





TYPICAL MODULE CONNECTOR

COMPONENT SIDE		NON-COMPONENT SIDE	
1	+112 V	2	STATIC CHECK
3	+28 V	4	+100 V.
5	SIGNAL GROUND	6	-100 V.
7	reserved for future use	8	OUTPUT A
9	FUNCTION SWITCH (N.O. 1 UPPER)	10	POT. SET
11	FUNCTION SWITCH (N.O. 2 LOWER)	12	FUNCTION SWITCH (ARM)
13	TRUNK LINE (2)	14	TRUNK LINE (1)
15	TRUNK LINE (4)	16	TRUNK LINE (3)
17	REVERSE HOLD	18	REVERSE RESET (R.O)
19	FORWARD HOLD	20	FORWARD RESET (R.O)
21	OVEN, RELAY PWR. GRD.	22	AMPLIFIER PWR. GRD.
23	POT. (1 ARM)	24	POT. (1 TOP)
25	POT. (3 ARM)	26	POT. (3 TOP)
27	POT. (2 ARM)	28	POT. (2 TOP)
29	F. GENERATOR (IN)	30	POT. (2 BOTTOM)
31	F. GENERATOR (O_1)	32	F. GENERATOR (J_1)
33	F. GENERATOR (O_2)	34	F. GENERATOR (J_2)
35	reserved for future use	36	OUTPUT B
37	FORWARD RESET (REAL TIME)	38	+28 (R)
39	-28 V.	40	TIME SCALE CHANGE
41	-112 V.	42	DYNAMIC CHECK
43	OVERLOAD BUS.	44	BALANCE



SD 40/80
TOP VIEW

A3-2

POTS 6-9 98-109 "00"	1 3 5	POTS 6-9 98-109 "00"	POTS 78-89 "80"	2 4 6	POTS 78-89 "80"		
POTS 10-21 114-125 "10"	7 9 11	POTS 10-21 114-125 "10"	POTS 90-101 "90" RESERVED FOR FUTURE	8 10 12	POTS 90-101 "90" RESERVED FOR FUTURE		
POTS 18-29 118-125 "20"	13 15 17	POTS 18-29 118-125 "20"	+100 VDC FOR POTS	14 16 18	+100 VDC FOR POTS		
POTS 30-61 "30"	19 21	POTS 30-61 "30"		20 22 24			
POTS 38-49 "40"	23 25 27	POTS 38-49 "40"		26 28			
POTS 50-61 "50"	29 31	POTS 50-61 "50"	TIE POINT	30 32 34	T. PT.		
POTS 58-69 "60"	33 35 37	POTS 58-69 "60"	T. PT.	36 38	T. PT.		
POTS 70-81 "70"	39 41 43	POTS 70-81 "70"	T. PT. T. PT. T. PT.	40 42 44	T. PT. T. PT. T. PT.		

A3-3A

+112 VDC	1 3 5 7 9 11	+112 VDC	+100 VDC (REF)	2 4 6 8 10 12	+100 VDC (REF)		
-112 VDC	13 15 17 19 21 23	-112 VDC	-100 VDC (REF)	14 16 18 20 22 24	-100 VDC (REF)		
+28 VDC	25 27 29 31 33 35	+28 VDC	-28 VDC	26 28 30 32 34 36	-28 VDC		
+28 VDC (6A)	37 39 41 43	+28 VDC (6A)	+28 VDC	38 40 42 44	+28 VDC		

A3-3B

+112 VDC	1 3 5 7 9 11	+112 VDC	-112 VDC	2 4 6 8 10 12	-112 VDC		
	13 15 17 19 21 23			14 16 18 20 22 24			
	25 27 29 31 33 35			26 28 30 32 34 36			
	37 39 41 43			38 40 42 44			

A3-4

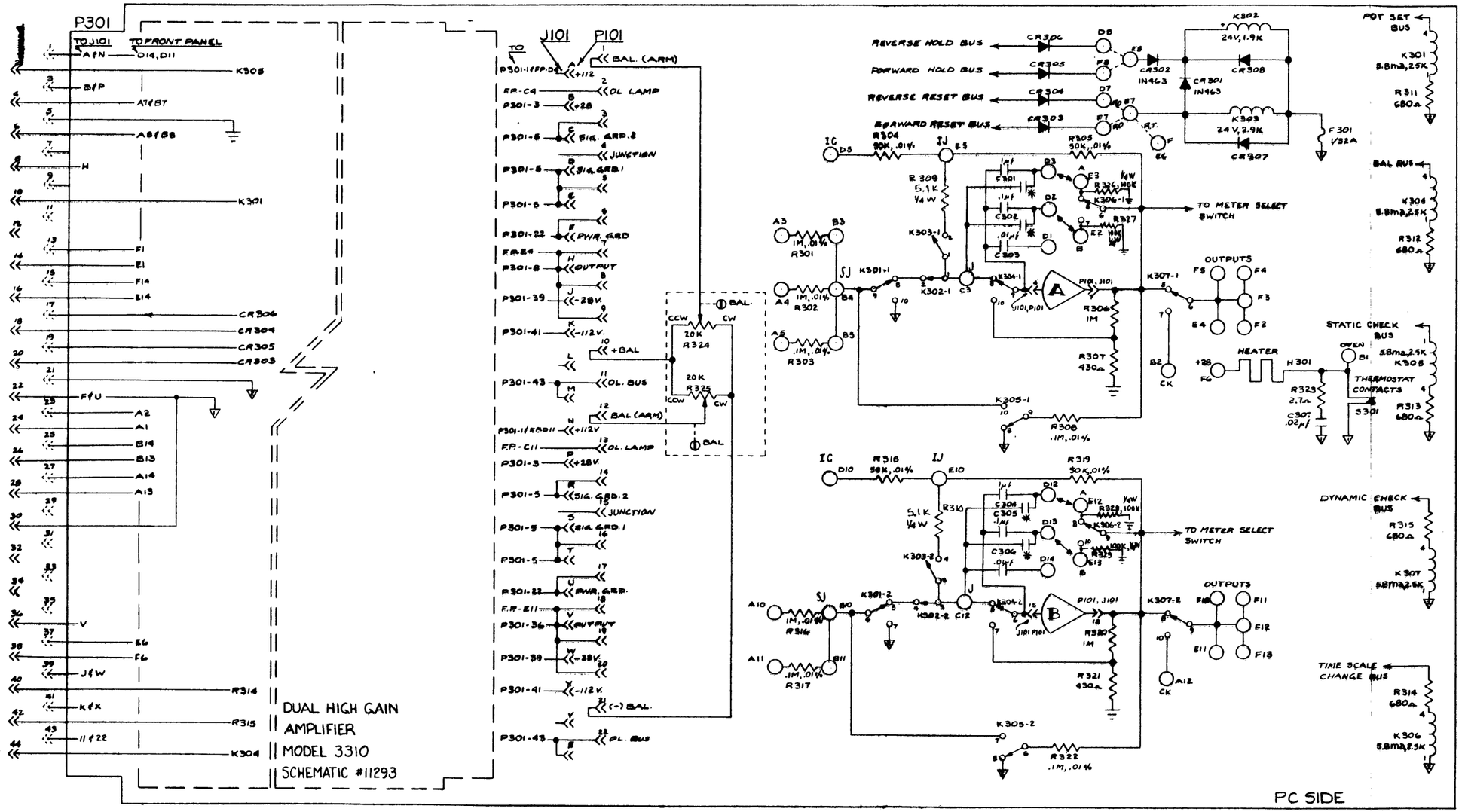
DYNAMIC CHECK	1 3 5 7	DYNAMIC CHECK	OVERLOAD	2 4 6 8	OVERLOAD		
BALANCE	9 11 13 15	BALANCE	REVERSE HOLD	10 12 14 16	REVERSE HOLD		
FORWARD HOLD	17 19 21 23	FORWARD HOLD	REVERSE RESET	18 20 22 24	REVERSE RESET		
FORWARD RESET	25 27 29 31	FORWARD RESET	TIME SCALE CHANGE	26 28 30 32	TIME SCALE CHANGE		
STATIC CHECK	33 35 37 39	STATIC CHECK	POT. SET	34 36 38 40	POT. SET		
REAL TIME RESET	41 43	REAL TIME RESET	REAL TIME RESET	42 44	REAL TIME RESET		

NOTE:

1. HEAVY LINES INDICATE COMMON SECTIONS.

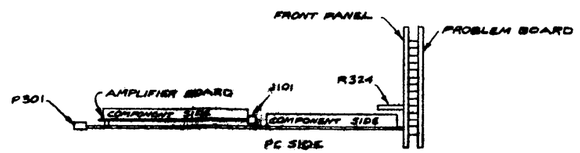
DRAWN BY: J. KANNING	DATE 8/24/64	UNLESS SPECIFIED DIMENSIONS INCHES	
CHECKED BY: [illegible]	DATE 8-28	TOLERANCES DECIMAL ANGULAR	
PROJ. ENGR. [illegible]	DATE 8/25/64	SURFACE FINISH —	
APPROVED BY: [illegible]	DATE - - 64	SCALE NONE	
MODEL	NEXT ASSEM	CONCORD CALIFORNIA	
SD 40	13895		
SD80	14672	TITLE UNIT IDENTIFICATION	DWG. NO. 15062 ISSUE B

DET. NO. | ITEM | MATERIAL | QUAN./UNIT

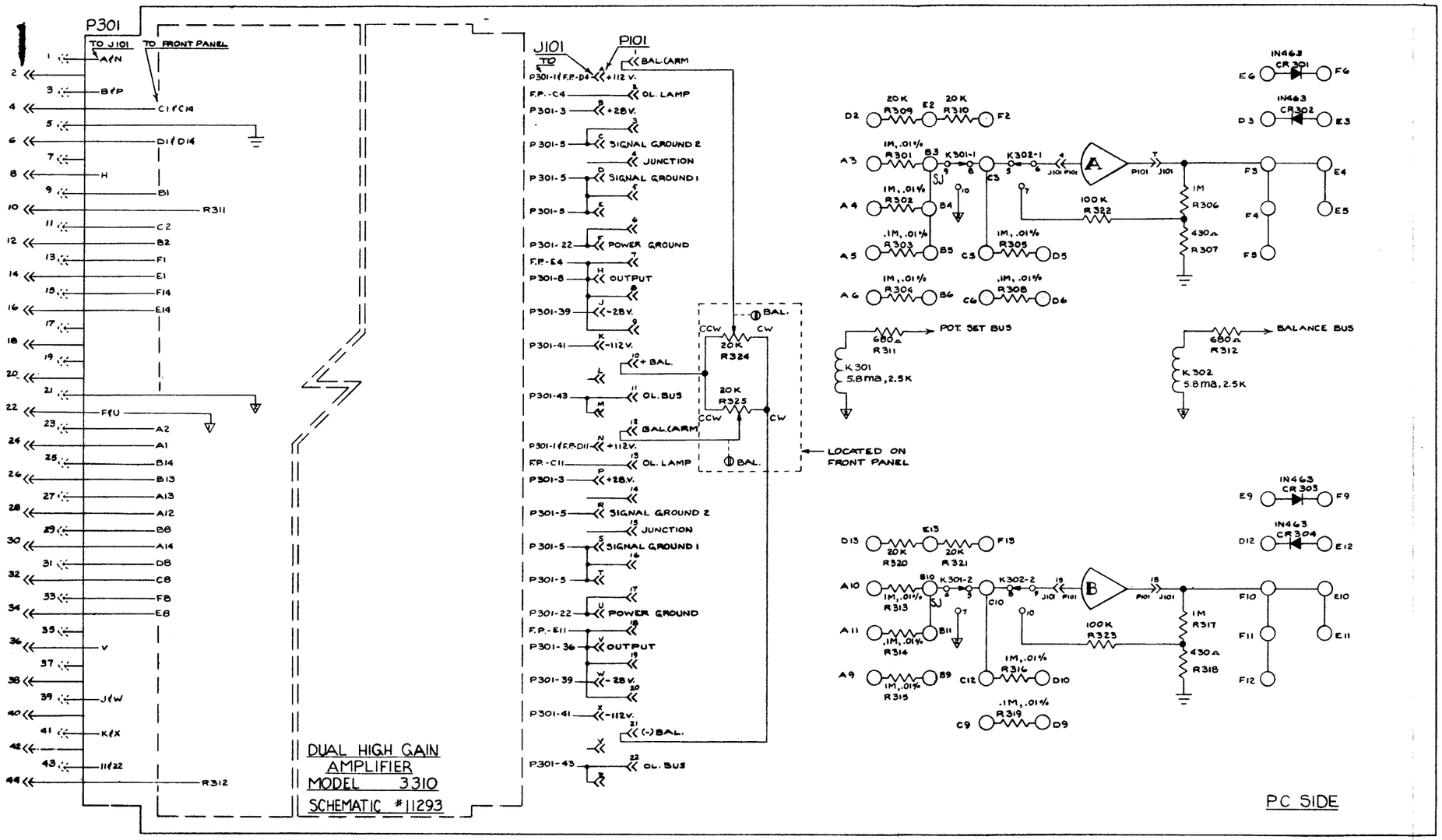


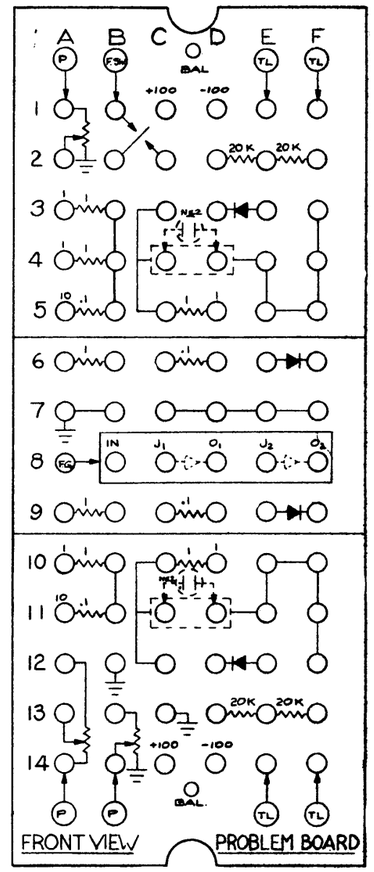
4. * TRIMMER CAPACITORS TO ADJUST VALUES OF 1MF AND 0.1MF. COMPUTING CAPACITORS.
3. ⏚ POWER GROUND ⏚ SIGNAL GROUND
2. RESISTORS - COMP. CARB, 1/2W, 5% UNLESS OTHERWISE SPECIFIED.
1. ALL DIODES IN4383 UNLESS OTHERWISE SPECIFIED.

NOTES:



REF. P/L 11880



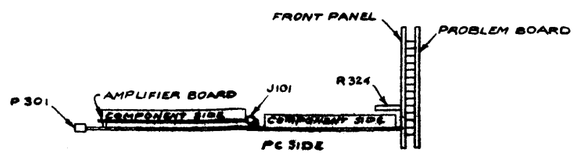


DUAL HIGH GAIN AMPLIFIER
MODEL 3310
SCHEMATIC #11293

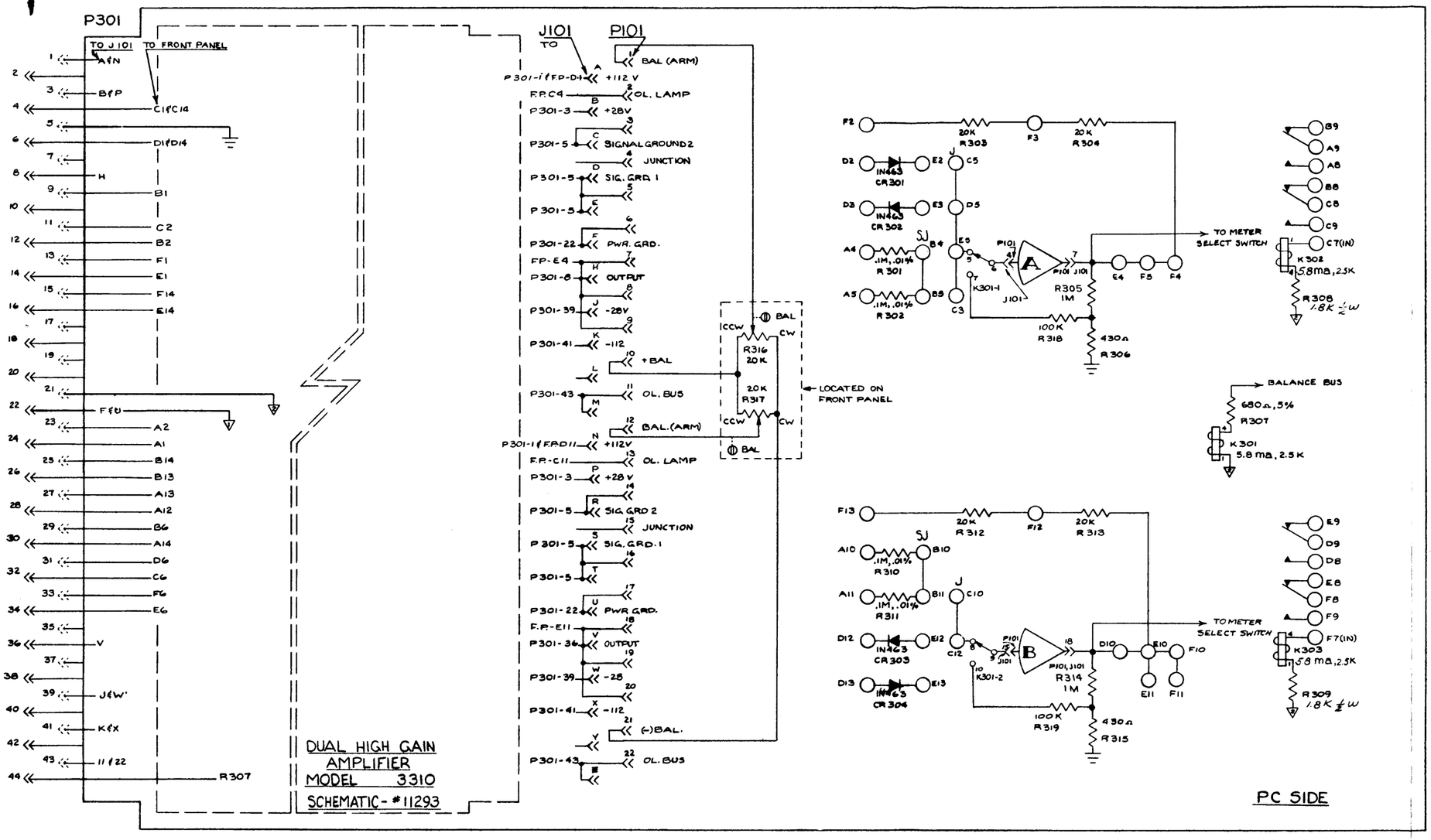
2. POWER GROUND SIGNAL GROUND

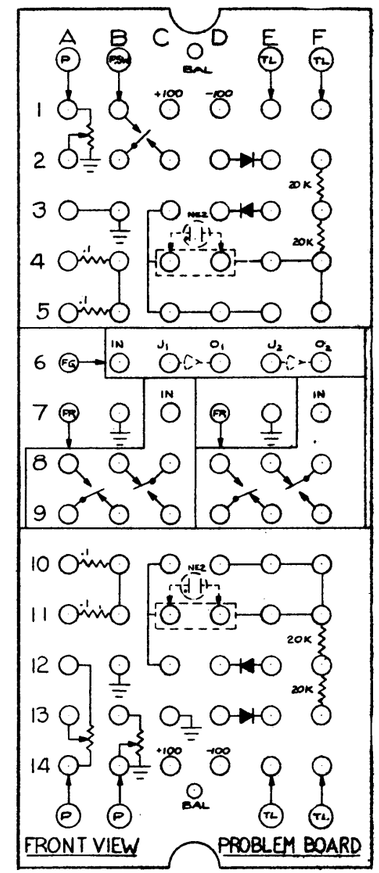
1. RESISTORS - COMP CARB, 1/2 W, 5% UNLESS OTHERWISE SPECIFIED.

NOTE:



DUAL SUMMER M3321 – 15106D

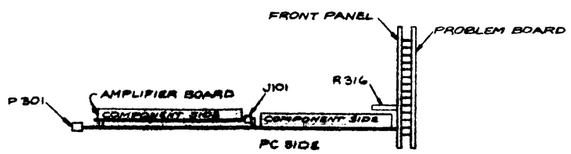




2. ⏚ POWER GROUND ⏚ SIGNAL GROUND

1. RESISTORS - COMP. CARB., ½W, 5%, UNLESS OTHERWISE SPECIFIED.

NOTE:



DUAL INVERTER/FUNCTION RELAY M3322A – 15105C

P301

TO J101 TO FRONT PANEL

1 A¢N
2
3 B¢P
4
5 C1¢C14
6 D1¢D14
7
8 H
9
10
11
12
13 F1
14 E1
15 F14
16 E14
17
18
19
20
21
22 F¢U — K301
23 A2
24 A1
25 B14
26 B13
27 A14
28 A13
29
30
31
32
33
34
35
36 V
37
38
39 J¢W
40
41 K¢X
42
43 11¢22
44 R308

DUAL HIGH GAIN AMPLIFIER
MODEL 3310
SCHEMATIC #11293

J101 P101

TO

P301-1 (F.P.-D4) — A — +112 V.
F.P.-C4 — B — OL. LAMP
P301-3 — C — +28 V.
P301-5 — D — SIGNAL GROUND 2
4 JUNCTION
P301-5 — E — SIGNAL GROUND 1
5
P301-5 — F
6
P301-22 — G — POWER GROUND
F.P.-E4 — 7
P301-8 — H — OUTPUT
8
P301-39 — J — -28 V.
9
P301-41 — K — -112 V.
10 — +BAL.
L
P301-43 — M — OL. BUS
11
12 — BAL. (ARM)
P301-1 (F.P.-D11) — N — +112
F.P.-C11 — 13 — OL. LAMP
P301-3 — P — +28 V.
14
P301-5 — R — SIGNAL GROUND 2
15 JUNCTION
P301-5 — S — SIGNAL GROUND 1
16
P301-5 — T
17
P301-22 — U — POWER GROUND
F.P.-E11 — 18
P301-36 — V — OUTPUT
19
P301-39 — W — -28 V.
20
P301-41 — X — -112 V.
21 — (-) BAL.
Y
P301-43 — Z — OL. BUS
22

BAL.
CCW CW
20K R361
20K R362
CCW CW
BAL.

A4 R351 B4 .1M, .01% SJ
A5 R352 .1M, .01% B5
C5 J R363 100K D5
J101 P101 5
K301-1 7
100K R353
P101 J101 A
1M R354
430Ω R355
278.9K R206

A10 R356 B10 .1M, .01% SJ
A11 R367 .1M, .01% B11
C10 J R364 100K D10
J101 P101 8 9
K301-2 10
100K R358
P101 J101 B
1M R359
430Ω R360
278.9K R406

BAL. BUS
680Ω R308
K301 4

25K, 0.5%, W.W. R101 — CR101
25K, 0.5% W.W. R103 — CR102
25K, 0.5% W.W. R201 — CR201
25K, 0.5% WW R203 — CR202
25K, 0.5%, W.W. R204
25K, 0.5%, W.W. R301 — CR301
25K, 0.5%, W.W. R303 — CR302
25K, 0.5%, W.W. R401 — CR401
25K, 0.5% WW R403 — CR402
R102, R104, R202, R204, R302, R304, R402, R404

F7 M D E7 A6
F6 M D E6 B6 +17 Y C6 J1
F5 B7
F4 C7 +17 Y D7
F3
F2 E5
E4

F8 M D E8 A9
F9 M D E9 B9 +17 Y C9 J2
F10 B8
F11 C8 +17 Y D8
E10
E11
F12
F13

D6 D9

C2 X1' ADJ. R105 1K
C13 X2' ADJ. R305
E2 Y1' ADJ. R205 1K
E13 Y2' ADJ. R405
LOCATED ON FRONT PANEL

(X)²
(Y1)²
(X2)²
(Y2)²

PC SIDE

FRONT PANEL
PROBLEM BOARD
P301
AMPLIFIER BOARD
J101
COMPONENT SIDE
COMPONENT SIDE
R361
PC SIDE

+100 V. — R107 OR R307 100K 3W CC — CR104 OR CR304 — CR103 OR CR303

TO CR101, CR102 OR CR301, CR302 — R109 OR R309 5.365K — R108 OR R308 1.713M, 1%

R111 R311 18.22K
R113 R313 17.59K
R115 R315 15.72K
R117 R317 13.51K
R119 R319 12.24K
R121 R321 10.63K
R123 R323 9.548K
R125 R325 8.199K
R127 R327 7.080K
R129 R329 6.399K
R131 R331 5.417K
R133 R333 4.746K
R135 R335 3.966K
R137 R337 3.220K
R139 R339 2.430K
R141 R341 1.907K
R143 R343 1.293K
R145 R345 206.5K

CR105 OR CR305 — CR106 OR CR306 — CR107 OR CR307 — CR108 OR CR308 — CR109 OR CR309 — CR110 OR CR310 — CR111 OR CR311 — CR112 OR CR312 — CR113 OR CR313 — CR114 OR CR314 — CR115 OR CR315 — CR116 OR CR316 — CR117 OR CR317 — CR118 OR CR318 — CR119 OR CR319 — CR120 OR CR320 — CR121 OR CR321

R112 R312 2.24M, 1%
R114 R314 1.957M, 1%
R116 R316 1.800M, 1%
R118 R318 1.682M, 1%
R120 R320 1.417M, 1%
R122 R322 1.259M, 1%
R124 R324 1.080M, 1%
R126 R326 936.0K
R128 R328 793.4K
R130 R330 647.3K
R132 R332 519.0K
R134 R334 397.7K
R136 R336 291.4K
R138 R338 220.3K
R140 R340 140.8K
R142 R342 72.66K
R144 R344 54.31K

"X1" OR "X2" BOARD

TO FP-D6

TO CR201, CR202 OR CR401, CR402 — R208 OR R408 1.713M, 1% — R209 OR R409 5.365K

R212 R412 2.24M, 1%
R214 R414 1.957M, 1%
R216 R416 1.800M, 1%
R218 R418 1.682M, 1%
R220 R420 1.417M, 1%
R222 R422 1.259M, 1%
R224 R424 1.080M, 1%
R226 R426 936.0K
R228 R428 793.4K
R230 R430 647.3K
R232 R432 519.0K
R234 R434 397.7K
R236 R436 291.4K
R238 R438 220.3K
R240 R440 140.8K
R242 R442 72.66K
R244 R444 54.31K
R246 R446 C.C.(F.S.)
R245 R445 206.5K

CR205 OR CR405 — CR206 OR CR406 — CR207 OR CR407 — CR208 OR CR408 — CR209 OR CR409 — CR210 OR CR410 — CR211 OR CR411 — CR212 OR CR412 — CR213 OR CR413 — CR214 OR CR414 — CR215 OR CR415 — CR216 OR CR416 — CR217 OR CR417 — CR218 OR CR418 — CR219 OR CR419 — CR220 OR CR420 — CR221 OR CR421

R211 OR R411 18.22K
R213 OR R413 17.59K
R215 OR R415 15.72K
R217 OR R417 13.51K
R219 R419 12.24K
R221 OR R421 10.63K
R223 OR R423 9.548K
R225 OR R425 8.199K
R227 OR R427 7.080K
R229 OR R429 6.399K
R231 OR R431 5.417K
R233 OR R433 4.746K
R235 OR R435 3.966K
R237 OR R437 3.220K
R239 OR R439 2.430K
R241 OR R441 1.907K
R243 OR R443 1.293K

CR204 OR CR404 — R210 OR R410 100K 3W CC — R207 OR R407 — CR203 OR CR403 — -100 V.

"Y1" OR "Y2" BOARD

R198 OR R350 CC(F.S.) 51.1K — R199 OR R349 — CR346 — R197 OR R347 — CCW R105 OR R305 CW — -100 V. 5.23K R198 OR R348 — REF. ONLY FRONT PANEL

R248 OR R448 CC(F.S.) — +100 V. 5.23K R247 OR R447 — CCW R205 OR R405 CW

R249 OR R449 51.1K — R250 OR R450 CC(F.S.)

REF. SCHEMATIC SQUARING NETWORKS 19331

3. ALL DIODES EXCEPT THOSE LISTED IN NOTE 2 ARE TO BE SELECTED FOR LEAKAGE OF 1 NANO AMP OR LESS @ 36V REVERSE BIAS SDC PART # CR0168
2. CR101, CR102, CR201, CR202, CR301, CR302, CR401, CR402 } MATCHED TO 1MV @ .75 MA SDC PART # CR0167 (SET OF 2)
1. R101, R102, R103 & R104, R201, R202, R203 & R204, R301, R302, R303 & R304, R401, R402, R403 & R404 } WIRE WOUND, ±0.5%, MATCHED TO 0.01%.

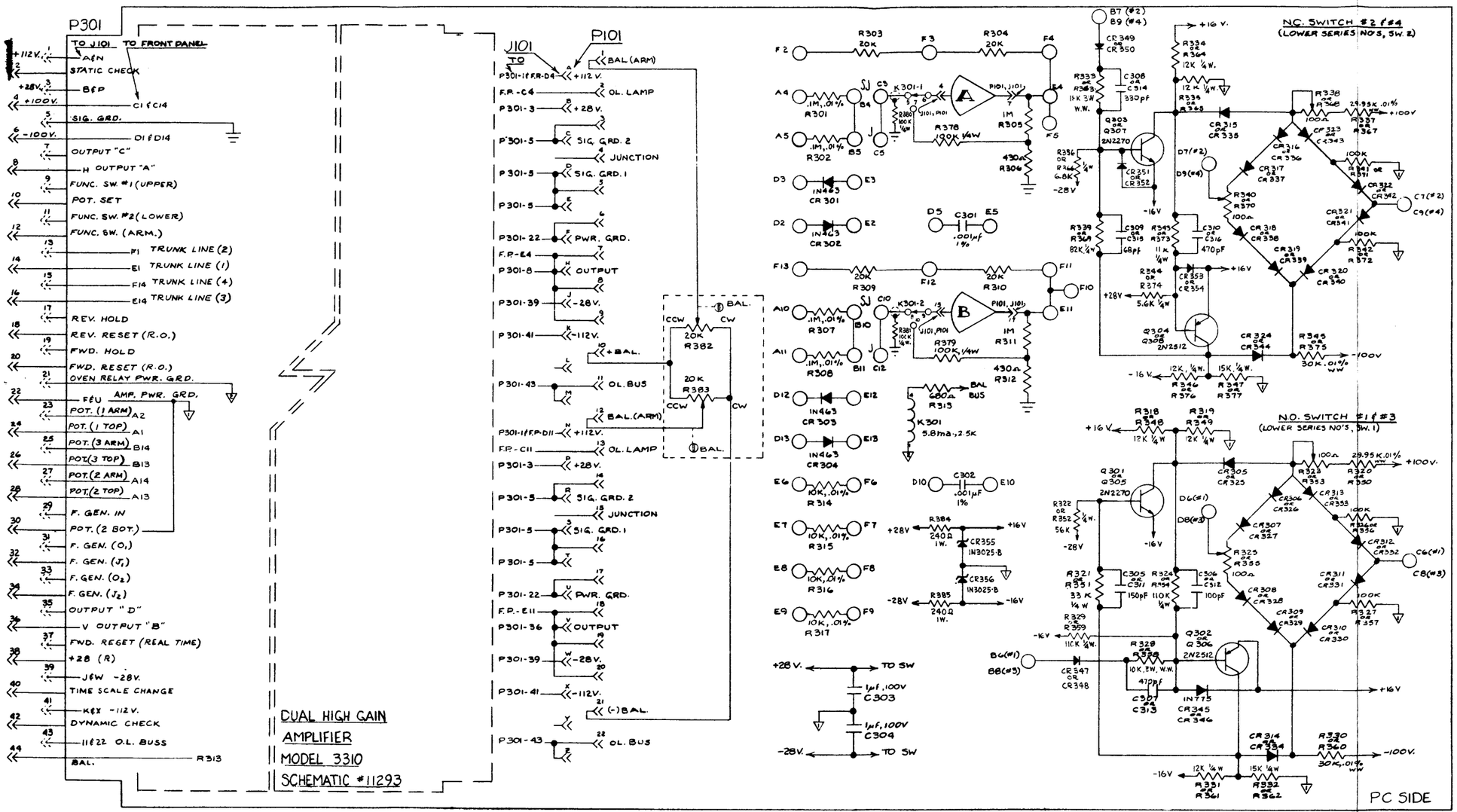
NOTES:

	A	B	C	D BAL.	E	F
1	P		+100	-100	TL	TL
2			X1		Y1	
3						
4						
5						
6	X1	R1	-R1	J1	M	
7	Y1	Y1	-Y1		M	
8	Y2	Y2	-Y2		M	
9	X2	R2	-R2	J2	M	
10						
11						
12						
13	X2		Y2			
14	P	P	+100	-100	TL	TL

BAL.

FRONT VIEW — PROBLEM BOARD

DUAL INVERTER/MULTIPLIER M3323 – 15107E



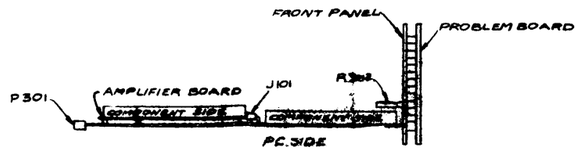
4. LAST R & CR Nos. - R385 , CR356

3. POWER GROUND ⏚ SIGNAL GROUND

2. RESISTORS - COMP CARB., 1/2W, 5% UNLESS OTHERWISE SPECIFIED

1. ALL DIODES CD 6544 UNLESS OTHERWISE SPECIFIED

NOTES:



REF P/L 14548

DUAL INVERTER/QUAD. ELECT. SWITCH M3324 - 14918D

P501

TO J502 & J503

1 +112V. A&N
2 STATIC CHECK
3 +28V. B&P
4 +100V.
5 SIG. GROUND
6 -100V. DIG.
7 OUTPUT C (J502-18)
8 OUTPUT A (J502-7)
9 FUNC. SW. UP. NO.1 B1
10 POT SET R501
11 FUNC. SW. LOW. NO.2 C2
12 FUNC. SW. ARM B2
13 TRUNK LINE (2) F1
14 TRUNK LINE (1) E1
15 TRUNK LINE (4) F14
16 TRUNK LINE (3) E14
17 REV. HOLD
18 REV. RESET (R.O.)
19 FWD. HOLD
20 FWD. RESET (R.O.)
21 OVEN RELAY PWR. GROUND
22 AMP. PWR. GROUND F&U
23 POT. (1 ARM) A2
24 POT. (1 TOP) A1
25 POT. (3 ARM) B13
26 POT. (3 TOP) B12
27 POT. (2 ARM) A13
28 POT. (2 TOP) A12
29 F. GEN. (IN) C13
30 POT. (2 BOT.) A14
31 F. GEN. (O1) E13
32 F. GEN. (J1) D13
33 F. GEN. (O2) F12
34 F. GEN. (J2) F13
35 OUT. D J503-18
36 OUT. B (J503-7)
37 FWD. RESET REAL TIME
38 +28 (R)
39 -28V. J&W
40 TIME SCALE CHANG
41 -11½V. K&X
42 DYN. CAL.
43 ½ -11&22
44 BAL. R502

TO FRONT PANEL

DUAL HIGH GAIN AMPLIFIER
MODEL 3310
SCHEMATIC #11293

J502 TO P501-1 & F.P. A +11.2V.
F.P. - C5 (J501) C6 (J502) OL. LAMP
P501-3 B +28V.
4 JUNCTION "A"
P501-5 D SIG GRD.
P501-22 6 PWR. GRD.
F.P. E4 7 OUTPUT "A"
P501-8
P501-39 J -28V.
P501-41 K -11.2V
10 + BAL.
P501-43 11 OL. BUS
12 BAL. (ARM)
P501-1 & F.P. D9 N D10 +11.2V.
F.P. - C9 (J501) C10 (J502) P 13 OL. LAMP
P501-3 +28V.
14
15 JUNCTION "C"
P501-5 T SIG. GRD.
P501-22 17 PWR. GRD.
F.P. E9 18 OUTPUT "C"
P501-7
P501-39 W -28V.
P501-41 X -11.2V
21 (-) BAL.
Y
P501-43 22 OL. BUS
P501-36 F.P. E6 7 (P503) OUTPUT "B"
P501-35 F.P. E11 18 (P503) OUTPUT "D"

CONNECTIONS FOR CHANNELS "A" & "C" SHOWN

BAL. ARM J503-12
+BAL. J503-10
+BAL. J503-21

BAL. R408 20K CCW CW
BAL. R308 20K CCW CW
BAL. R108 20K CCW CW
BAL. R208 20K CCW CW

POT SET BAL. BUS — CHANNELS A & B — R501 39Ω — K501 8.4 ma. 4 FC 24VDC
POT SET BAL. BUS — CHANNELS C & D — R502 39Ω — K502 8.4 ma. 4 FC 24VDC

J503-1 BAL. ARM

LOGIC RELAYS

SCHEMATIC DETAIL NO.'S

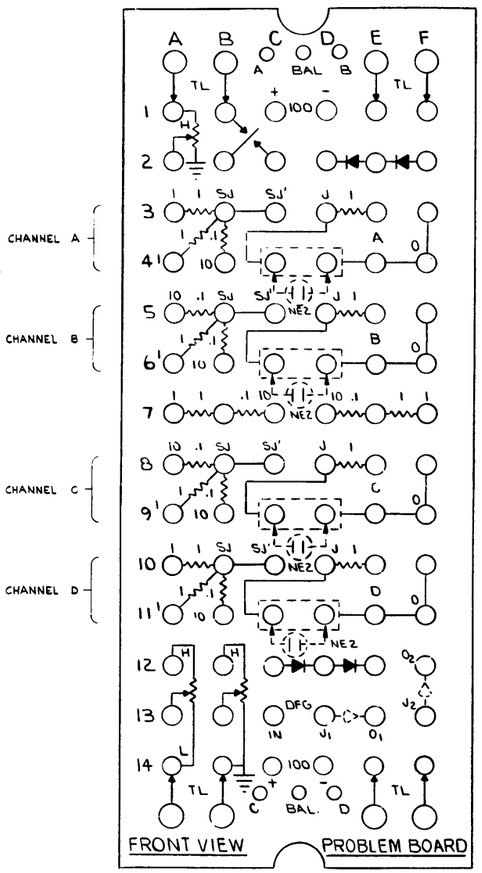
100 SERIES - "A" CHANNEL AMPLIFIER
200 SERIES - "B" " "
300 SERIES - "C" " "
400 SERIES - "D" " "
500 SERIES - ALL COMMON

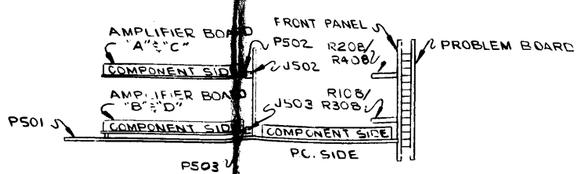
FRONT PANEL COMPONENTS

A7 R503 0.1M B7 R504 1M C7
D7 R505 0.1M E7 R506 1M F7
D2 CR501 IN463 E2 CR502 IN463 F2
C12 CR503 IN463 D12 CR504 IN463 E12

TYPICAL SUMMER CIRCUIT
(CHANNEL "A" SHOWN)

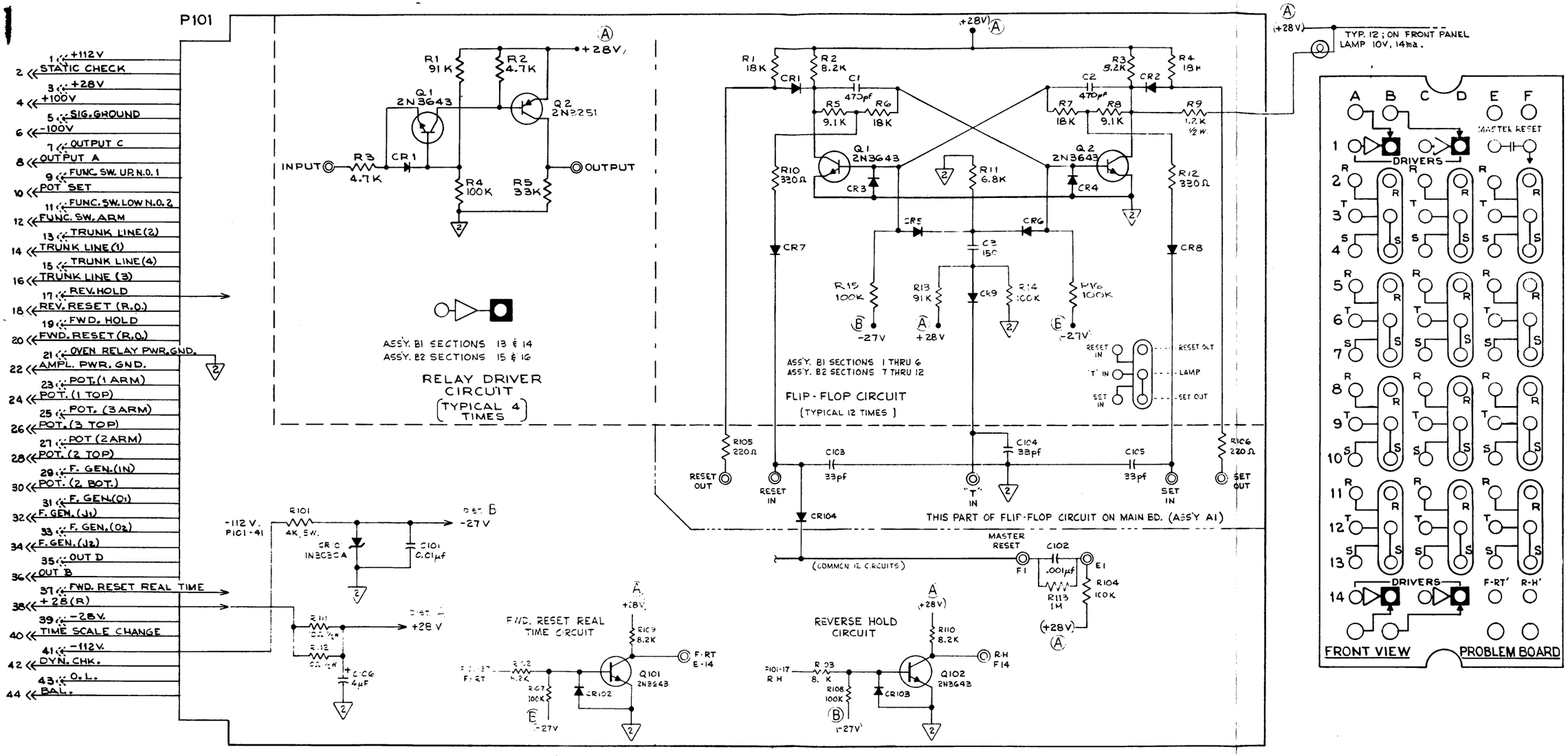
A3 R101 1M .01% B3
A4 R102 1M .01%
B4 R103 0.1M .01%
POT SET K501 C3
BAL. K501 D3
"A"
BAL.
TO ARM R108 (FRONT PANEL)
E3 R104 1M .01%
E4 R106 1M
R105 100K
R107 430Ω
F3
F4





2. ⏚ POWER GROUND ⏚ SIGNAL GROUND
1. RESISTORS: COMP CARB. 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
NOTE:

QUAD SUMMER - M3325 - 17078A



NOTES:

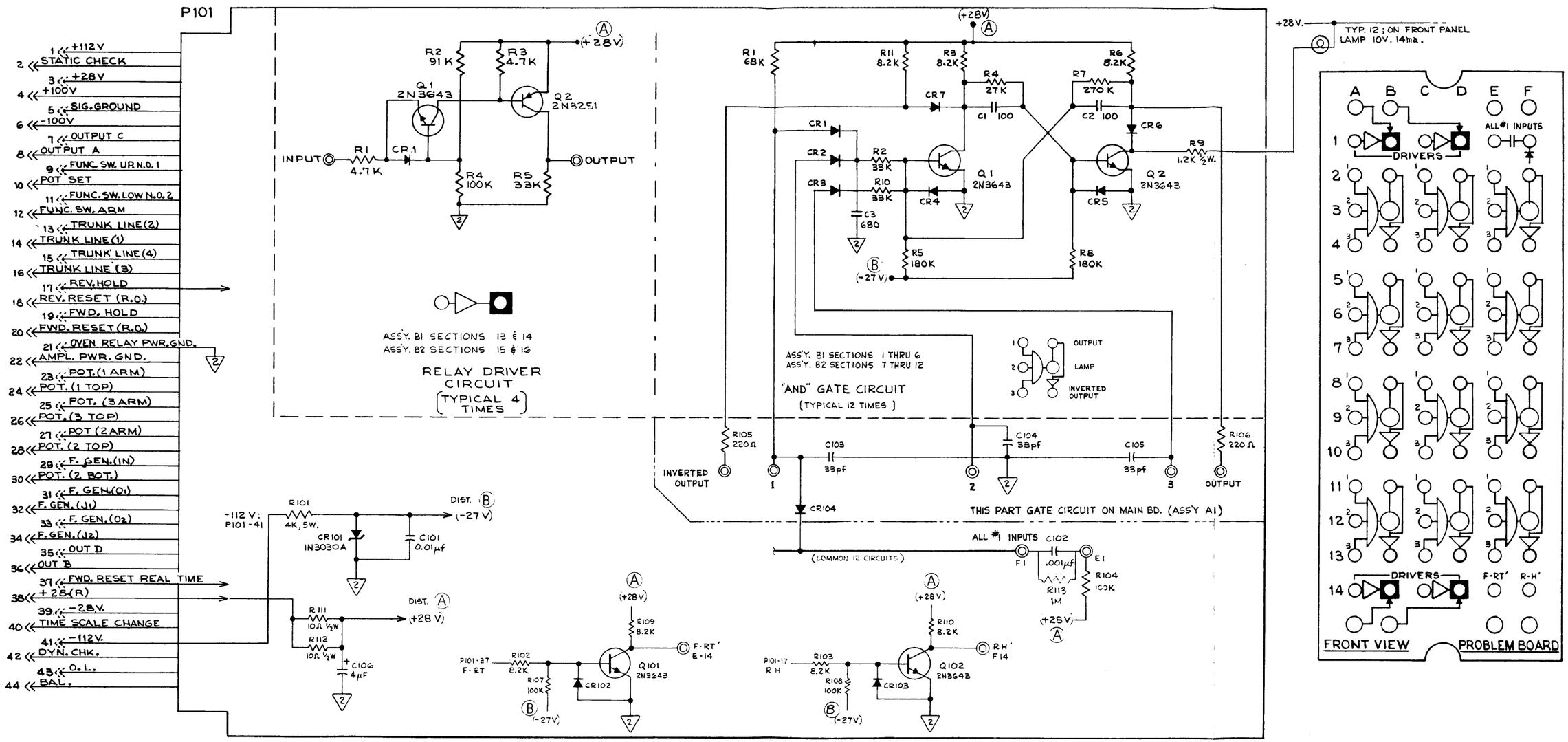
UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE ±5% 1/4 W.
2. DIODES ARE 1N3064
3. ALL DETAIL Nos. PREFIXED TO ASSY Nos. & SECTION Nos.

LAST DETAIL NO'S. USED.

	DRIVER	FLIP-FLOP	A1 & A4 BD. (A1)
TRANSISTORS —	Q2	Q2	Q 2
DIODES —	CR1	CR9	CR104
RESISTORS —	R5	R16	R113
CAPACITORS —	—	C3	C106

FLIP-FLOP MODULE M3326 - 17550A



NOTES:

UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE ±5% ¼ W.
2. DIODES ARE 1N3064
3. ALL DETAIL Nos. PREFIXED TO ASS'Y No's. & SECTION No's.

LAST DETAIL NO'S. USED.

	DRIVER	"AND" GATE	MAIN BD. (A1)
TRANSISTORS —	Q2	Q2	Q102
DIODES —	CR1	CR7	CR104
RESISTORS —	R5	R11	R113
CAPACITORS —		C3	C106

LOGIC "AND" GATE MODULE M3327 – 17549A

DCU 1 | DCU 2 & 3 | DCU 4 | DCU 5 | DCU 6

OSC./DECADE DWG. 17243 — J-101

DUAL 300KC DECADE DWG. 17504 — J-104

DUAL 300KC DECADE — J-102

DECADE/DRIVERS DWG. 7503 — J-106

DECADE/DRIVERS — J-103

DECADE/DRIVERS — J-105

A1 1KC T — OUTPUT — INPUT — CR113 — A2 0V

F3 D4 INPUT 1 — C107 33 pf

F2 — 1KC

E3 INPUT 2 T — C110 33 pf

D3 INPUT 3 — D4 — C111 33 pf

HE7 E2 — OUTPUT 1

Z — D2 — OUTPUT 2

HE7 C2 — OUTPUT 3

C3 INPUT 4 — C116 33 pf

B3 INPUT 5 — C119 33 pf

INPUT 6 A3 — C122 33 pf

TO LAMPS TYP 3

F4 RESET 1 — R136 1M — C108 .001 µF — R130 100K — C109 33 pf

E4 RESET 2 — R137 1M — C112 .001 µF — C113 33

D4 RESET 3 — R138 — C114 .001 µF — R131 — R132 100K — C115 33 pf

C4 RESET 4 — R139 1M — C117 .001 µF — R133 100K — C118 33 pf

B4 RESET 5 — R140 1M — C120 .001 µF — C121 33 pf — R134 100K

A4 RESET 6 — R141 1M — C123 .001 µF — C124 33 pf — R135 100K

+28V | GRD | -27V

P101

+28V 38 | -112V. 41 | OVEN GRD 21 | 5 SIG GRD

R115 2K 5W — R101 2K 5W

CR101 IN3030B — C101 .01 µF

R124 68K — C1 — CR102 — D1 — CR103 — E1 — CR104

R102 33K — R103 180K — CR105

Q1 2N3643

R104 8.2K — C102 100pf — R105 27K

Q2 2N3643 — R106 180K — CR106

R107 8.2K — R108 4.7K — CR107

R109 91K — R110 4.7K

Q3 2N3643

Q4 2N3251 — F1

R111 100K — R112 33K

CR114 — R125 1M — A2 0V — C105 .01 — B2 +V — MASTER RESET

R113 27K

Q5 2N3643 — CR108 — R114 180K

A1 RITE — S1 — B1 — C106 .047 µF — J101-5

RESET AMPLIFIER "A" (TYPICAL 6 PLACES)

R116 15K — R119 8.2 K — R118 2.7K — +28V

Q6 2N3643 — C103 470 — Q7 2N3643 — C104 .01 — R123 470Ω — TO DCU RESET

R117 330Ω — R120 100 K — CR111 — R121 8.2 K — +28V — R122 180 K — CR112 — -27V

RESET 1-6 — CR109

MASTER RESET 0V — CR110

J-106 DCU-4 | J-104 DCU-1 | J-102 DCU-2 & 3

J-105 DCU-6 | J-103 DCU-5 | J-101 OSC-DCU

FRONT PANEL PROBLEM BOARD — P101

NOTES:
ALL RESISTORS 5%, 1/4 W UNLESS OTHERWISE STATED.
ALL DIODES ARE IN3064 UNLESS OTHERWISE STATED.

FINAL DETAIL NOS.	
TRANSISTOR	Q7
DIODE	CR14
RESISTOR	R141
CAPACITOR	C124

B5 — B14 — A5 — A14 — 10V. @14MA.

R127 (DCU4) 1.2K 1/2 W — +28V

LAMP CKT. TYP. 3

R128 (DCU5)

R129 (DCU6)

A B C D E F

GATE-DRIVER — 1KC

MASTER RESET — 0V — +V

OUTPUT 3 2 1

INPUT 6 5 4 3 2 1

RESET 6 5 4 3 2 1

DCU6 9 8 7 6 5 4 3 2 1 0

DCU5 9 8 7 6 5 4 3 2 1 0

DCU4 9 8 7 6 5 4 3 2 1 0

FRONT VIEW — PROBLEM BOARD

DIGITAL CLOCK – M3328 – 17565A

P101

1 +112V STATIC CHECK
2 +28V
3 +100V
4 SIG. GND.
5 -100V
6 OUTPUT "C"
7 OUTPUT "A"
8 F.S. UPPER N.O.1
9 POT SET
10 F.S. LOWER N.O.2
11 F.S. ARM
12 T.L.(2)
13 T.L.(1)
14 T.L.(4)
15 T.L.(3)
16 REV. HOLD
17 REV. RESET (R.O.)
18 FWD. HOLD
19 FWD. RESET (R.O.)
20 OVEN RELAY PWR. GND.
21 AMP. PWR. GND.
22 POT (1 ARM)
23 POT (1 TOP)
24 POT (3 ARM)
25 POT (3 TOP)
26 POT (2 ARM)
27 POT (2 TOP)
28 F. G. (IN)
29 POT (2 BOT.)
30 F. G. (O_1)
31 F. G. (J_1)
32 F. G. (O_2)
33 F G (J_2)
34 OUTPUT "D"
35 OUTPUT "B"
36 FWD. RESET (R.T.)
37 +28V (R)
38 -28V
39 TIME SCALE CHG.
40 -112V
41 DYN CHECK
42 OVERLOAD
43 BALANCE
44

Ⓐ(+28V)

Q1 2N3643, R1 91K, R2 4.7K, Q2 2N3251
INPUT, R3 4.7K, CR1, R4 100K, R5 33K, OUTPUT

IN, OUT

ASS'Y. B1 SECT. 13 & 14
ASS'Y. B2 SECT. 15 & 16
RELAY DRIVER CIRCUIT
(4 REQ'D.)

-112V, R101 4K, 5W, CR101 1N3030A, C101 .01 MFD, DIST Ⓑ (-27V) SUPPLY

MAIN BRD.
ASS'Y. A1

Ⓐ(+28V), R109 6.2K, E14 F-RT', R107 100K, CR102, Q101 2N3643, R102 6.2K
Ⓐ(+28V), R110 8.2K, R103 6.2K, Q102 2N3643, R108 100K, CR103
(-27V)Ⓑ

FWD. RESET REAL TIME AND REVERSE HOLD CIRCUITS

R111 10Ω 1/2W, DIST. Ⓐ (+28V) SUPPLY
R112 10Ω 1/2W, C106 4MFD
R104 100K, C102 .001MFD, R113 1 MEG.
E1, F1, MASTER RESET

Ⓐ(+28V)
R1 18K, R2 8.2K, C1 470PF, CR1
R5 9.1K, R6 18K
Q1 2N3643, CR3
R10 330Ω, CR7
R15 100K, CR5, R11 6.8K, C3 150PF, CR6, R16 100K
R13 91K, CR9, R14 100K
Ⓑ(-27V), (+28V)Ⓐ, (-27V)Ⓑ

FLIP-FLOP CIRCUIT
(6 REQ'D.)
ASS'Y. B1 SECT. 1 THRU 6

R3 8.2K, R4 18K, C2 470PF, CR2
R7 18K, R8 9.1K, R9, 1.2K 1/2W
2N3643 Q2, CR4
R12 330Ω, CR8

LAMP, 10V 14MA (6 REQ'D.)
(+28V)Ⓐ

R105 220Ω, C103 33PF, C104 33PF, C105 33PF, R106 220Ω
RESET OUT Ⓡ, Ⓡ RESET IN, CR104, "T" IN Ⓣ, SET IN Ⓢ, Ⓢ SET OUT

COMMON 6 CIRCUITS

R-H (F14)

Ⓐ(+28V)
R1 68K, R11 8.2K, R3 8.2K, R4,27K C1,100PF, R7, 270K C2,100PF, R6 8.2K
CR1, CR2, CR3, CR7, R2 33K, Q1 2N3643, R10 33K, CR4, C3 680PF, R5 180K
2N3643 Q2, CR6, CR5, R8 180K
R9,1.2K 1/2W
Ⓑ(-27V)

"AND" GATE CIRCUIT
(6 REQ'D.)
ASS'Y. B2 SECT. 7 THRU 12

LAMP, 10V 14MA (6 REQ'D.)
(+28V)Ⓐ

R105 220Ω, C103,33PF, C104,33PF, C105,33PF, R106 220Ω
1, CR104, 2, 3, OUTPUT
COMMON 6 CIRCUITS

INVERTED OUTPUT

LAMP

LAMP
R, T, S

A B C D E F
1 2 3 4 5 6 7 8 9 10 11 12 13 14
MASTER RESET
DRIVERS
R A R B R C dc
R D R E R F
DRIVERS F-RT' R-H'

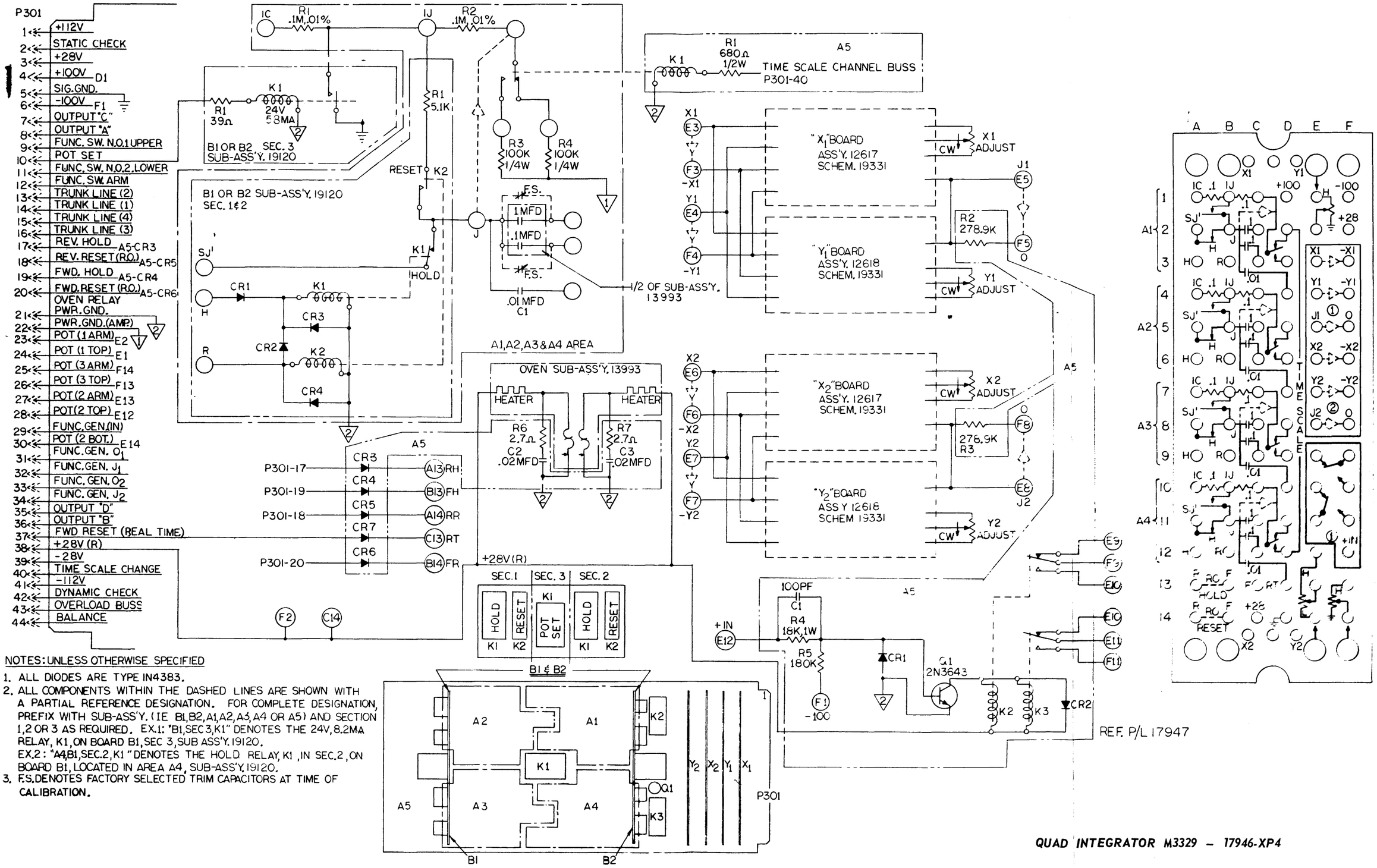
REF. P/L 19545

NOTES: UNLESS OTHERWISE SPECIFIED
1 RESISTORS ARE 1/4W, 5%.
2 DIODES ARE 1N3064.
3 ALL DETAIL NO'S. PREFIXED TO ASS'Y. NO'S. & SECTION NO'S.

LAST DETAIL NO'S. USED

	DRIVER	FLIP-FLOP	GATE	MAIN BD. A1
TRANSISTORS	Q2	Q2	Q2	Q102
DIODES	1	CR5	CR7	CR104
RESS	R1	R16	R11	R113
CAP'S.	—	C3	C3	C106

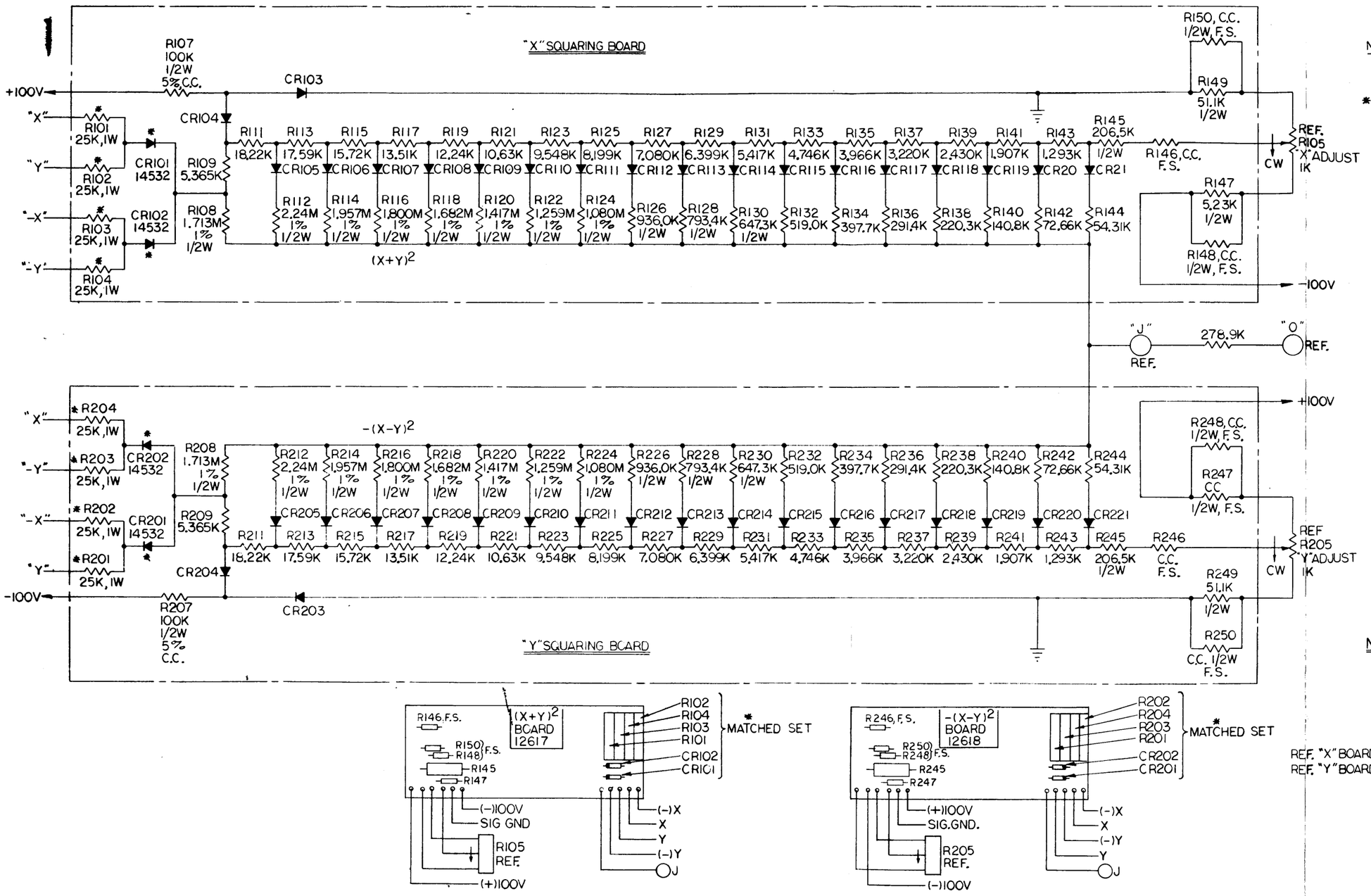
FLIP-FLOP/GATE MODULE M3326A – 19546A



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIODES ARE TYPE IN4383.
2. ALL COMPONENTS WITHIN THE DASHED LINES ARE SHOWN WITH A PARTIAL REFERENCE DESIGNATION. FOR COMPLETE DESIGNATION, PREFIX WITH SUB-ASS'Y. (IE B1, B2, A1, A2, A3, A4 OR A5) AND SECTION 1, 2 OR 3 AS REQUIRED. EX.1: "B1, SEC 3, K1" DENOTES THE 24V, 8.2MA RELAY, K1, ON BOARD B1, SEC 3, SUB ASS'Y. 19120.
   EX.2: "A4, B1, SEC. 2, K1" DENOTES THE HOLD RELAY, K1, IN SEC. 2, ON BOARD B1, LOCATED IN AREA A4, SUB-ASS'Y. 19120.
3. F.S. DENOTES FACTORY SELECTED TRIM CAPACITORS AT TIME OF CALIBRATION.

QUAD INTEGRATOR M3329 – 17946-XP4



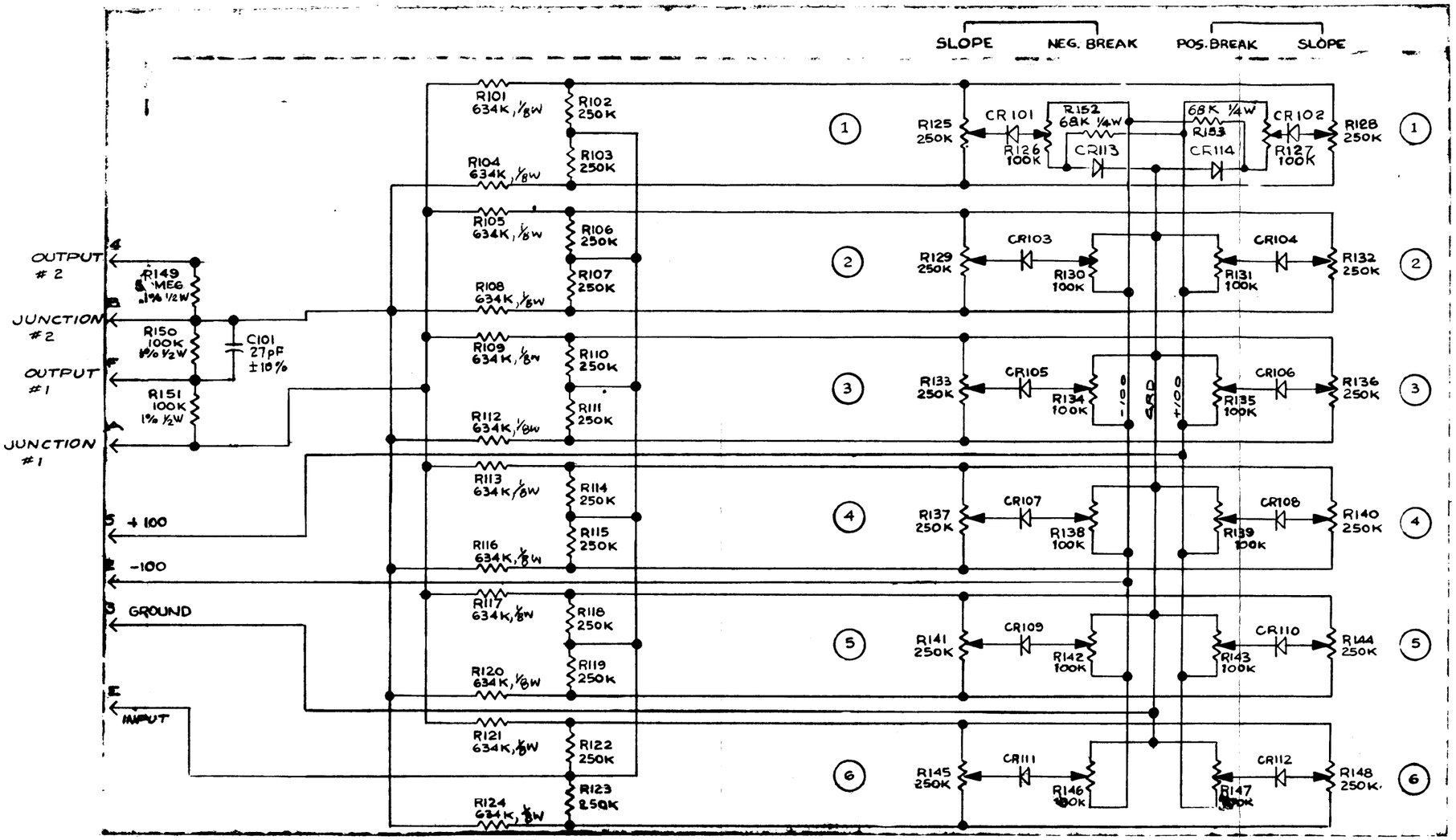
NOTES: UNLESS OTHERWISE SPECIFIED

1. DIODES TO BE PER DWG. 14531.
2. ALL RESISTORS 1/4W, 1/2%, MET. FILM.
3. * R101 THRU R104, CR101, CR102, R201 THRU R204, CR201 & CR202 ARE A MATCHED SET FOR EACH BOARD. REF. 13529-2 & 14532.
4. F.S. DENOTES RESISTORS FACTORY SELECTED AT TIME OF CALIBRATION.

NOTE THIS SCHEMATIC ALSO APPEARS ON DWG. 15107

REF. "X" BOARD P/L 12617
REF. "Y" BOARD P/L 12618

SQUARING NET WORKS ¼ SQ. MULT. QSM – 19331-XP2



3. ALL FIXED RESISTORS ARE 1%, 1/2 W., D.C. UNLESS OTHERWISE NOTED
2. ALL POTS ARE 1/4 W., ± 20 %.
1. DIODES ARE IN459
UNLESS OTHERWISE NOTED.

NOTES:

FUNCTION GENERATOR – MODEL 3351 – 14259E