DISK STORAGE SYSTEM

TECHNICAL MANUAL

System Industries

REFERENCE MANUAL

3050 DISK STORAGE SYSTEM FOR MICRODATA COMPUTERS

SYSTEM INDUSTRIES

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CONTENTS

I. INTRODUCTION

The System Industries Model 4400/4500 Disk Systems are designed to provide a wide range of bulk storage capabilities to users of various minicomputers. All of these systems incorporate the System Industries 3040 Disk Controller combined with either the Diablo Systems Inc. Model 40 Series moving-head disk drives, or the Applied Magnetics Corporation (AMC) fixed-head disk drives, or combinations of both. The moving-head drives provide a large on-line capacity plus the convenience and flexibility of a removable storage medium, while the fixed-head drives provide very fast access. Thus, these storage systems can be configured to meet in an efficient fashion the needs of a variety of minicomputer system requirements and applications.

This manual describes the Model 4400/4500 Disk System when the Model 3040 Disk Controller is interfaced to the Microdata computers.

The manual includes the functional descriptions and capabilities of the system, procedures on its operational aspects, and includes checkout and diagnostic data. The appendixes contain information regarding installation procedures along with all the necessary diagrams and schematics for a complete understanding of the system.

2. FUNCTIONAL CAPABILITIES

System Configuration

The Model 4400 Disk Storage Systems employ fixed-head disks only and are used in those applications requiring very fast access to limited amounts of data. Model 4500 Systems employ moving-head disk drives and are best suited for those applications requiring large capacity, or the flexibility and convenience of a removable medium for off-line storage. With either system, the user has the option of adding one or more of the other type of disk. Such combinational systems can provide rapid access to those parts of the data or program files that require it, and at the same time, offer large-capacity on-line data storage.

The Model 4400/4500 Systems utilize both the Program I/O and direct memory access facilities of the minicomputer. All commands from the minicomputer to the disk system and status information from the disk system to the computer are transferred via Program I/O. All data transfers between the computer memory and the disk use the DMA facility.

The Model 3040 Controller, which is the heart of the disk storage system, has four independent parallel peripheral ports. Each port can accomodate one of the following:

- One Diablo Model 43 Disk Drive
- One Diablo Model 44 Disk Drive
- One AMC Model 200-D Disk Drive

Any combination of the 3 disk drives may be attached to the 3040 Controller to form a storage system. Since the same set of instructions is used for both the moving-head and the fixed-head disks, the programming is independent of the particular storage system configuration.

Changes to the Model 4400 or 4500 Disk System's configuration can be made conveniently in the field by plugging the cable interfaces for the additional disk drives into the unused ports of the 3040 Controller.

Table 2-1 summaries the capacities, access times, and transfer rates for the Model 4500 Systems and Table 2-2 provides that information for the Model 4400 Systems.

Data Transfer Operation

The main functions of a disk controller are to provide the user with a method of addressing the blocks of data on the disk and to control the parallel to serial or serial to parallel conversions of the data when writing onto or reading from the disk respectively. This subsection describes the methods employed by the Model 3040 Disk Controller when used in the Model 4400/4500 Systems.

- Disk Addressing

  The smallest addressable block of data in a Model 4400/4500 Disk System is called a sector. For 16-bit minicomputers, each sector contains either 128 or 256 16-bit words, depending upon whether a track is divided into 24 or 12 sectors respectively. The number of tracks in any one disk drive is a function of the type of disk drive and can be obtained from either Table 2-1 or 2-2. In order to address a sector, the user must specify a Block Address which contains both the track and sector information for that particular block of data. The maximum block address for each disk platter is a function of the number of tracks on that disk platter and the number of sectors on each track. Starting

TABLE 2-1

Moving-Head Disk Specifications for 16-bit Computers

	Model 43	Model 44
Number of Tracks per Drive	816	1632
Number of Sectors per Track	12/24	12/24
Number of Words per Sector	256/128	256/128
Total Drive Capacity (Words)	2,506,752	5,013,504
Maximum System Capacity (Words)	10,027,008	20,054,016
Bit Transfer Rate	2500 Khz	2500 Khz
Word Transfer Rate	156 Khz	156 Khz
Average Rotational Latency	12.5 ms	12.5 ms
Head Movement Times, Max.:		
Cylinder to Cylinder	12 ms	12 ms
Average	38 ms	38 ms

TABLE 2-2

Specifications for a Maximum Capacity Fixed-Head System for 16-bit Computers.

Maximum Number of Tracks*	128
Number of Sectors/Track	12/24
Number of Words/Sector	256/128
Total Disk Capacity (Words)	393,216
Maximum System Capacity (Words)	1,572,864
Bit Transfer Rate	3.4 MHz
Word Transfer Rate	191 Khz
Average Access Time	8.3 ms

*AMC drives are available with 1-16 heads. Each head records on 8 tracks. Formatting is performed prior to shipment.

with sector zero of track zero and going to the last sector of the last track, each sector is identified with an ascending 15-bit binary value which will be unique for each sector. Thus to address a sector, the user must specify its unique 15-bit block address, and from that value, the Model 3040 Controller will automatically calculate the correct track and sector values. This alleviates the user from having to work with the numbers 12 or 24, which are not multiples of two, when specifying a disk address.

- Data Transfer Specification

Besides the starting disk address, only two other parameters need to be specified to initiate a data buffer of any size - from one word up to 32,768 words. These two other parameters are the word count and the starting core address. These parameters are initialized prior to a data transfer initiation by a single I/O instruction and are automatically maintained and updated by the 3040 Controller throughout the ensuing transfer.

NOTE: A "word" is defined to be 16 bits in length.

Once these three parameters have been initialized and the data transfer is started, the 3040 Controller will transfer the exact number of words as specified by the word count and will automatically cross any sector, track, or cylinder boundary to access these words. This word count/current address approach to data transfer operations enables the user to transfer large blocks of data with just a single sequence of I/O instructions, without regard to disk boundaries. Sectors of data are transferred consecutively, even when going across track boundaries.

A revolution of time is lost only on moving-head disks when going across cylinder boundaries to allow time for the heads to move to the next cylinder.

- Read and Write Operations

  The I/O instructions which initiate the read or write operation actually initiate a command seek-read or a seek-write operation. This concept thus helps simplify the programming steps to start a data transfer since the user doesn't have to separately preposition the head before a read or write instruction is executed. The longer time it takes to do a seek-read or seek-write over just a read or write after the head has been positioned does not affect the total system, since the disk ports are parallel in construction and overlap seeks on any other port may be initiated at any time. In addition, the combined seek-read (or write) operation makes the moving-head disk appear to the user to be no different than the fixed-head disk except for the response time, allowing programming to be done independently of the disk type.

- Address Verification

  For the moving-head drives, the Model 3040 Controller automatically verifies that the correct sector has been located before a read or write operation can take place on any sector. This is done for each and every sector to be read or written, and is especially important for the write operation where an inaccurate head movement would cause a loss of data without this verification. This address verification is accomplished by comparing the address of the desired block address and the actual address written at the

beginning of each sector on the disk. These block addresses are written on each disk cartridge prior to its use by means of a disk formatting program. Should an addressing error be sensed, an automatic restore is done on that disk port by the Model 3040 Controller to alleviate the programmer from having to accomplish this by additional instructions.

- Double Buffering

In order to allow the computer some timing leeway while still keeping up with the high transfer rates of the disk drives, a double buffering data transfer scheme is employed.

Data coming off the disk during a read operation comes in in a bit serial fashion and shifts into the Data Shift Register in the 3040 Controller. When this shift register is full, a parallel transfer must take place from the shift register into a buffer interface register which holds the data for a computer DMA cycle while the shift register is busy shifting in the next word. If only one buffer interface register were employed, this would require that the computer answer the DMA request within the time it takes to shift in one word to the disk controller. This would place limitations on both system architectures and the types of instructions one could use while the data transfer was taking place.

To alleviate this problem, a double buffering scheme using a second buffer interface register was employed. This gives the

computer twice the amount of time it takes the disk to transmit one word to the controller for it to answer a DMA request. This scheme is also utilized when writing onto the disk. This gives the system designer and programmer the flexibility needed without worrying about the speed of the disk transfers.

- Error Checking

  The Model 4400/4500 Disk Systems are constantly sensing for the occurrence of nine different errors. Four of these, which are sensed by the disk drives themselves, are the File Ready, Write Check, Logical Address Interlock and Seek Incomplete Errors. The other five, which are sensed by the Model 3040 Controller, are the Address Verification, Cyclic Redundancy Check, Computer Timing, Write-Lockout and Format errors. When any of these errors are sensed, the operation is terminated with the cause of the termination displayed in the Control and Error Register of the Model 3040 Controller.

- Post-Transfer Status Information

  At the completion of a data transfer, as well as during it, the contents of both the Block Address Register and the Control and Error Register in the Model 3040 Controller are available via program I/O instructions. The information in the Block Address Register will contain either the block address of the sector on the disk following the last one involved in the transfer operation if the transfer was successfully completed, or the block address of the sector on the disk when one of the nine error was sensed. The

contents of the error portion of the Control and Error Register indicates which errors, if any, occurred during the transfer operation.

Additional Features

The following features, in addition to those directly involved in the data transfer operation, enhance the capabilities and ease of use of the Model 4400/4500 Disk Systems.

- Bad Sector Indication

  Bad sectors on a disk cartridge used in moving-head drives can be identified and then flagged by means of a format program. This is done by incorrectly formatting the bad sector, thus forcing an address verification error. Software look-up tables may then be used to identify the replacement sector.

- Write Protection

  For moving-head disks, any sector on a cartridge can be write-protected by setting the write-protect bit in the Block Address Word. The setting of this bit is done when the sector is formatted prior to its use. When it is set and during the course of normal operation (when the format switch is in the "NORMAL" position), an attempt to write that sector will result in the generation of a write-protect error and a termination of the write operation. The initial writing of write-protected sectors or the updating of information in write-protected

sectors can be accomplished through manual intervention by switching the format switch to the "FORMAT" position before attempting to write on those sectors. In this case, the format switch serves as a write-protect override switch.

Write-protection in the fixed-head disks may only be accomplished if the disk is equipped with the write-protect option. With this option, groups of eight tracks may be protected against write operations by setting the write-protect switch (located on the front panel of the disk) associated with the set of tracks. As with the cartridge disk, if a write operation is attempted on any sector in a set of tracks whose write-protect switch has been set, the write operation will be terminated and the occurrence of the write-protect error will be indicated in the Status Register of the controller.

- Overlap Seeking

With four parallel ports and separate Seek Address and Block Address Registers, the design of the Model 3040 Disk Controller allows the user to initiate overlap seeks (head-positioning actions without data transfers automatically following) on a disk port at any time, even if a data transfer is in progress on another disk port. This capability can greatly enhance system response times by overlapping the longer head movement times with other system actions and reducing the access times of data transfers down to the lower limit of the average rotational delay of the drive.

- Interrupt Generation

The Model 4400/4500 Disk Systems are designed to fully utilize both the skip-on-condition (either "done" or "busy") instructions and the interrupt capabilities of the Microdata series computers to which it is interfaced. The programmer may read the CER and test either the done or busy flags at any time, and can control interrupts locally in the Model 3040 Disk Controller via the interrupt enable bit of the Control and Error Register. If the interrupt enable bit is set when the done flag gets set, an interrupt request will be generated to the computer.

The done flag will be set when a data transfer completes, either successfully or with the sensing of an error, or when a head movement terminates from an overlap seek while there is no data transfer in progress.

The information needed to interpret the cause of the interrupt is contained in the Control and Error Register of the Controller for data-transfer-related interrupts and in the Seek Status Register for interrupts generated at the completion of a seek operation. Both of these registers may be interrogated by an I/O instruction in an interrupt subroutine.

- Instruction Timing

The Model 4400/4500 Systems have been designed to eliminate timing problems that could result under certain sequences of disk system comands. For example:

- The controller will automatically queue a data transfer instruction for a cartridge disk drive that is presently seeking and will execute that data transfer instruction upon the completion of the seek operation.

- The controller will automatically queue a data transfer instruction until the completion of the sequence that sets up the Word Count Register and Current Address Register. This relieves the CPU of any waiting when initiating the data transfer operation.

- Overlap seeks may be initiated on any port at any time. However, the execution of an overlap seek on a port is ignored when that port is presently seeking or performing a data transfer.

- The registers in the controller that receive commands from the computer are always available; the programmer does not have to observe any minimum waiting time restrictions.

3. SYSTEM DESCRIPTION

This chapter contains the description of the Model 3040 Controller and is presented in terms of the registers whose contents control the controller operation and provide information to the CPU, and the instructions which control these registers.

See Appendix B, Drawing # 3050-9006-1, for a block diagram of the 3040 Controller interfaced with a Microdata computer and a single disk drive. Using programmed I/O instructions, information moves to or from the Control and Error Register and the Block Address Register, only to the Seek Address Register, and only from the Seek Status Register. The two buffer interface registers are connected to the DMA facility of the computer for data transfers and the Current Address Register is attached to the DMA facility for specifying the locations in the CPU memory to (or from) which the data is to be transferred.

REGISTER DESCRIPTIONS

The following controller registers are those with which the programmer has direct contact (either establishing or interogating their contents):

- Control and Error Register

  The Control and Error Register (CER) is a 16-bit register, whose upper half consist of seven error-indicator bits and whose lower half provides seven data transfer control and status buts. One bit is unused.

  A total of nine different errors are sensed by the controller during a data transfer operation. They have been divided into

three equal groups so that a two-bit field may describe which of the three errors in a group has occurred or that none of the three has occurred. One bit, the error flag, is used to indicate if any of the nine possible errors has occurred.

The control portion of the CER contains the busy and done flags to indicate the current status of a controller data transfer operation, the disk unit select bits used to select one of the four ports for a data transfer, the interrupt enable and format enable bits, and a read disk indicator bit used to control the direction of all data transfers on the data channel.

The specific bit assignments for this register are as follows:

BIT		FUNCTION
15		Error Flag. Indicates that an error occurred.
14,13	00	No Format, Select, or Timing Errors.
	01	Format Error. Indicates an attempt to format a disk without having the format switch in the FORMAT position, or to format a fixed-head disk.
	10	Select Error. Disk command assigned to a port that either has no disk or has a disk which is not in a condition to operate.
	11	Timing Error. Computer did not respond in time to receive or supply a data word from/to the controller.
12,11	00	No Logical Address Interlock, Address Verification, or Seek Incomplete Errors.
	01	Logical Address Interlock. Indicates that the track address given to the controller is greater than the maximum track value for the disk selected.

	10	Address Verification Error. Indicates that the controller has detected a difference between the Block Address Word in the sector it is attempting to read or write and the Block Address it expects to fine there. The controller initiates an automatic restore on that disk.
	11	Seek Incomplete Error. Indicates a hardware malfunction in the disk. The controller initiates an automatic restore on that disk.
10,9	00	No Write Lock Out, Write Check or Cyclic Redundancy Check errors.
	01	Write Lock Out Error. Indicates an error occurred when the program attempted to write onto a write-protected sector. The format switch can override the write-protected capability in the moving-head disk.
	10	Write Check Error. Indicates a malfunction in the disk that makes it incapable of writing data.
	11	Cyclic Redundancy Check Error. Indicates that an error was detected in the cyclic redundancy check word when reading the data from the disk.
8		Identical to Bit 0.
7		Unused. Will always read as zero.
6		Interrupt Enable. When set, this bit will allow the controller to generate an interrupt request when the done bit gets set.
5		Format Enable. When set, this bit will allow a sector to be formatted on a moving-head disk.
4,3		Disk Unit Select. A two bit field selecting one of four ports for a data transfer.
2		Read Disk Enable. This bit, which is automatically controlled by the controller, is used to indicate the direction of a data transfer. When set, the controller is reading from the disk; when clear the controller is writing onto the disk.
1		Busy Flag. Indicates the controller is busy transferrring data to or from the selected disk.
0		Done Flag. When set, this bit indicates that either (1) a data transfer operation has been completed, or (2) an independent seek operation has been completed while there is no data transfer active to any of the other three ports.

- Seek Status Register

The Seek Status Register (SSR) is a 16-bit register and is used to hold the status and results of all seek operations. It is composed of four 3-bit registers, each of which is associated with a disk port. Four bits are unused. In each 3-bit register, two bits are used to indicate the results of the last seek on the port while the third bit is a dynamic indication of whether the port is ready to receive a seek command. This register may only be read back to the accumulator, while the two bits used to indicate the seek results are automatically cleared upon a seek being initiated on that port. Those ports are having disks connected to them will have their 3-bit register read back as a 7_8. The complete bit assignments are as follows:

BIT	FUNCTION
12-14	Status register corresponding to disk port 3.
8-10	Status register corresponding to disk port 2.
4-6	Status register corresponding to disk port 1.
0-2	Status register corresponding to disk port 0.
3,7,11,15	Unused. Will always read as ones.
2,6,10,14	Indicates that a Hardware Seek Error has occurred. This can occur from either seeking to a non-existent cylinder (i.e., a Logical Address Interlock Error) or if the disk was unsuccessful in seeking to a legal cylinder number does occur, the controller will automatically generate a restore command to the disk.
1,5,9,13	Indicates that a Busy Error has occurred. This can occur from initiating a seek on a port when it was either active doing a data transfer or was not in a condition to receive a seek operation. In either case, the seek command is ignored when this error occurs.
0,4,8,12	A dynamic indicator for whether the port is in a condition to receive a seek command. A zero indicates it is ready while a one indicates that either the head is presently moving or that the drive is not ready.

- Seek Address Register

The Seek Address Register (SAR) is a 16-bit register used to temporarily hold the port and block address information while an overlap seek is initiated. It is also used as a communication path for those program I/O instructions entering the Block Address Register. The Seek Address Register may not be read back into the accumulator, but is always free to receive programmed information without any timing restrictions. The specific bit assignments are as follows:

BIT	FUNCTION
15, 14	A two-bit field used to select the port on which the overlap seek operation is to be initiated.
13-0	The block address containing the cylinder value to which the head will move when the overlap seek is executed. For 12 sector per track operation, this will be the full block address number. For 24 sector per track operation, this field will be the 14 most significant bits of the 15-bit block address number.

- Block Address Register

The Block Address Register (BAR) is a 16-bit register used to hold the block address for read and write operations. It is entered with the starting block address when the read or write operation is initiated, and is automatically updated when data transfers require going across sector boundaries. The specific bit assignments are as follows:

BIT	FUNCTION
15	Disk Select: A zero will select the non-removeable disk and a one will select the removeable disk for a moveable-head disk. This bit should be a zero for the fixed-head disk.
14-0	The block address to or from which the controller will transfer data.

OTHER REGISTERS

The registers described below are also used by the 3040 Controller, but are not available for programmer contact.

- Word Count Register (WCR)

  This 16-bit register stores the number of words remaining to be transferred and is updated as the transfer of each word takes place.

- Current Address Register (CAR)

  This 16-bit register holds the core memory address for the word being transferred and is incremented after each transfer occurs.

- Data Shift Register (DSR)

  During a read operation the Data Shift Register takes the data from the disk in a bit-serial fashion (least significant bits first) and when a complete word has been assembled that word is transferred in parallel to one of the buffer interface registers. The transfers alternate between Buffer Interface

Register #1 and Buffer Interface Register #2. During a write operation, data from the buffer interface registers are alternately transferred a word at a time into the Data Shift Register which in turn transmits the data in a bit-serial fashion (least significant bit first) out to the disk.

- Buffer Interface Register (BIR)

  As mentioned above, the data coming from the disk to the computer or vice versa pass through one of the two buffer interface registers. For a sequence of words being transferred, the registers are used alternately (first Register #1, then Register #2, then Register #1, and so on). This double buffering scheme gives the computer twice the one-word transfer time to respond to a data transfer request. With the high bit-transfer rates of these disk drives, this is particularly important if time-consuming instructions, such as indirect addressing sequences, are being used.

- Arithmetic Check Register (ACR)

  This register accumulates the arithmetic checksum word generated during the transfer of data to or from a sector. After writing a sector, this word is written at the end of the sector. After a read operation, the previously written checksum word is compared to the contents of this register to verify the correctness of the data transfer operation.

- Sector Address Register (SCR)

  This 5-bit register, whose inputs are the sector information out of the address divide network, holds the current sector value for only the read or write operations. This register is not altered when an overlap seek is executed.

- Sector Counter

  This register contains the number of the sector currently under the read/write heads. As the disk revolves, the Sector Counter is updated by the sector pulses from the disk and is compared with the contents of the Sector Address Register in order to determine when a data transfer operation should begin. This counter is located in the disk drive for moveable-head drives and on the disk interface cable for fixed-head drives.

DISK SECTOR FORMAT

This section describes the format of each sector on the cartridge disks and the fixed-head disks.

Moveable-Head Disk Sector Format

The format for a moveable-head disk sector is illustrated in Figure 3-2. Each item in this sector is described below:

- First Preamble

  The preamble at the beginning of each sector consists of thirteen 16-bit words written on the disk. The first 207 bits in the preamble are zeros; the last bit is a one.

- Block Address Word

This 16-bit word written on the disk contains the block address of the particular sector. The block address is written on a cartridge when it is formatted. Before a data transfer operation takes place, this block address is read and compared with the disired address in order to verify that the correct sector has been located. Bits 14-0 of the Block Address Word must correspond directly with bits 14-0 of the Block Address Register for the verify to be completed. Bit 15 of the Block Address Word is used as the write protect bit for the sector. If it is a zero, normal operation will occur. If it is set to a one, the sector will be write-protected and a write lock out error will occur if an attempt is made to write in a write-protected sector. Placing the format switch in the "FORMAT" position will override this write protect bit and allow updating of data in a write-protected sector.

- Second Preamble

The Second Preamble contains a 51.2 us string of bits (all zeros except for the last bit which is a one). This preamble envelopes the write amplifier turn-off and turn-on for the format and data sections respectively, and provides the read circuitry with a zero field for resynchronization during a read operation.

- Data

The data portion of the sector contains either 256 or 128 16-bit words for 12 or 24 sector per track operation, respectively.

- Cyclic Redundancy Check Word

This 16-bit word is the one's complement sum of the 256 or 128 data words in the sector. This word is automatically computed by the controller and written on the disk during a write operation. It is read and compared with a recalculated value from the disk data to verify the validating of the data transfer during a read operation.

- Overhead

The overhead is the unused portion of the sector. It is nominally 278 or 66 us for 12 or 24 sectors per track respectively, but will vary as a function of the instantaneous speed tolerances of the disks and with interchangability tolerances of the disk cartridges.

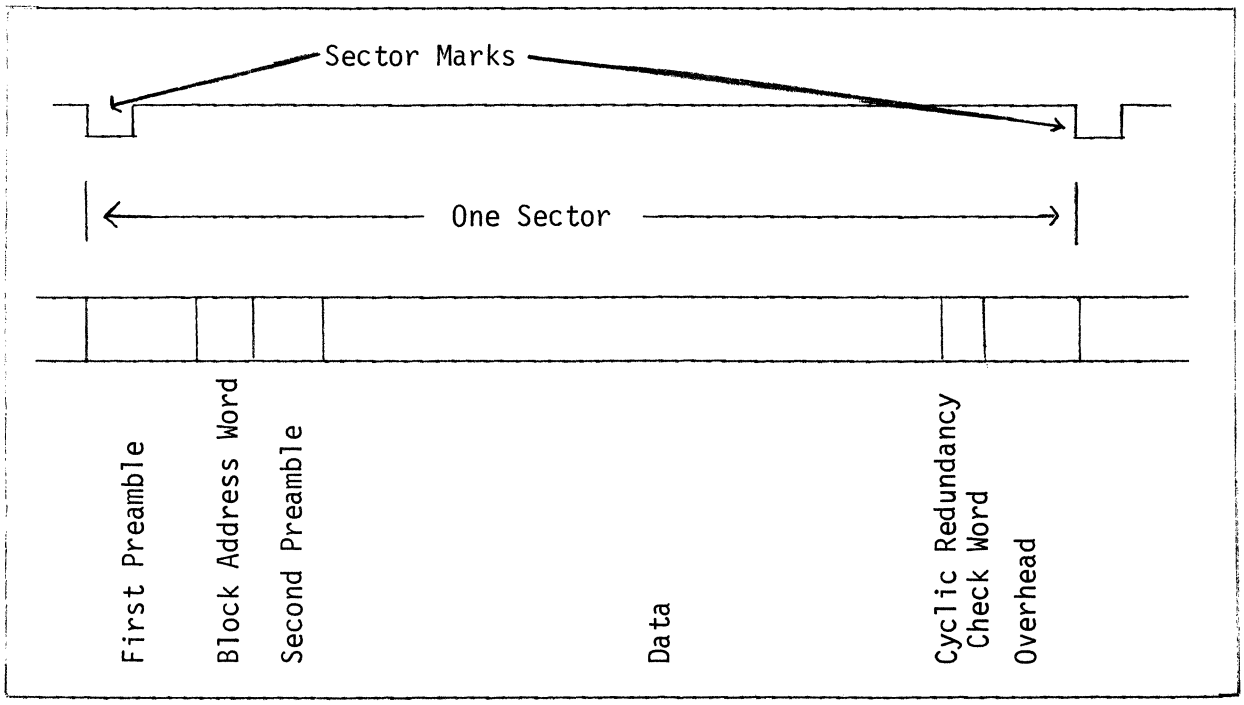


Figure 3.2
Moveable-Head Disk Sector Format

Fixed-Head Disk Sector Format

The format for a fixed-head disk sector is illustrated in Figure 3.3. Each item in this sector is described below:

- Preamble

  The preamble at the beginning of each sector consists of nine bits. The first seven bits are ones followed by a zero-one combination for the last two bits.

- Data

  The data portion of the sector contains either 256 or 128 16-bit words for 12 and 24 sector per track operation, respectively.

- Cyclic Redundancy Check Word

  This 16-bit word is the one's complement sum of the 256 or 128 data words in the sector. This word is automatically computed by the controller and written on the disk during a write operation. It is read and compared with a recalculated value from the disk data to verify the validity of the data transfer during a read operation.

- Overhead

  The overhead is the unused portion of the sector. It has a nominal value of 20 us.

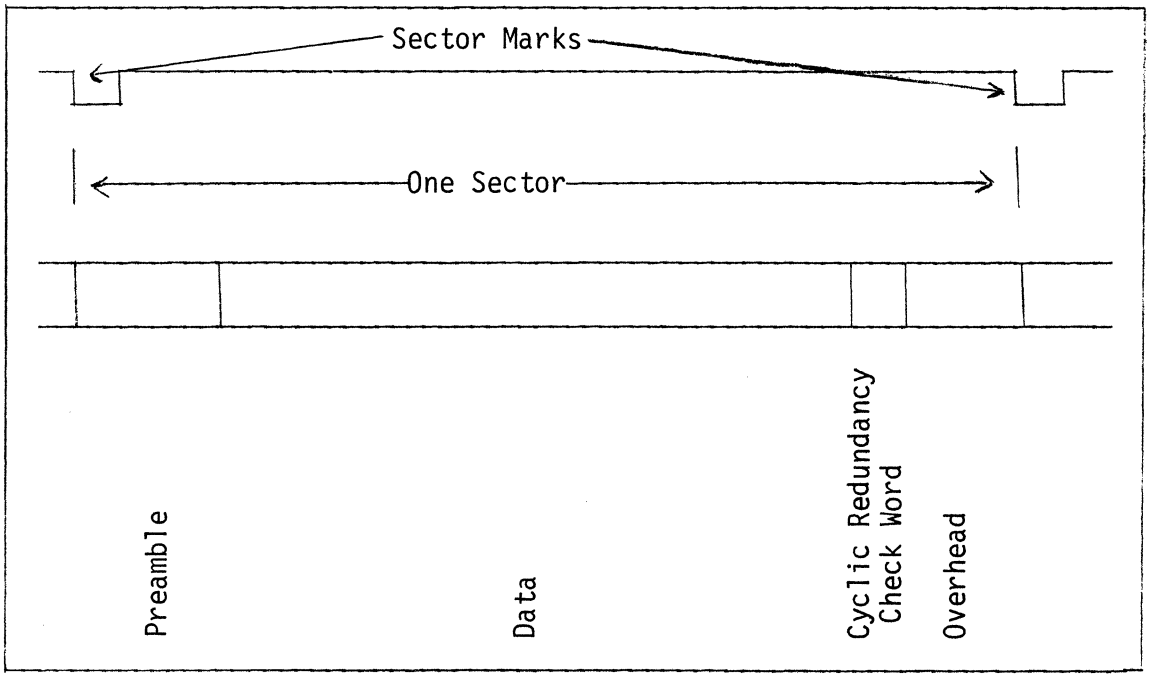


Figure 3.3
Fixed-Head Disk Sector Format

NOTE: The formatting of the fixed-head disk is done by the writing of a clock track on the disk with special equipment.

INTERFACE OPERATIONS

There are several differences between the Microdata 800/1600 version and other 16-bit versions of the System Industries 3040 Controller, specifically:

1) A General Buffer Register has been added to the controller. While the Microdata computer has 16-bit accumulators, it can only transfer 8 bits of information at a time. The General Buffer Register enables the controller to work with 16-bit words but transfer control information to and from the computer in 8-bit bytes. Figure 3.4 shows how the General Buffer Register has been incorporated into the controller.

A transfer of information from an accumulator to a controller register, (all but the Control and Error register), requires the following steps:

a) Accumulator bits 7 through 0 are transferred to the General Buffer Register.

b) Bits 15 through 8 of the accumulator are shifted into accumulator bit positions 7 through 0.

c) The information from the upper half of the accumulator, (that which has been shifted into bit locations 7 through 0), is transferred into bit positions 15 through 8 of the controller register. The contents of the General Buffer Register, (per step a), are also transferred to the controller register - bits 7 through 0.

When transferring information from a controller register to an accumulator in the computer, the following steps occur:

a) The contents of register bit locations 15 through 8 are transferred into accumulator bit positions 7 through 0 as register bit locations 7 through 0 are transferred to the General Buffer Register.

b) The information in the accumulator is shifted into bit positions 15 through 8.

c) The contents of the General Buffer Register are read into accumulator bit positions 7 through 0.

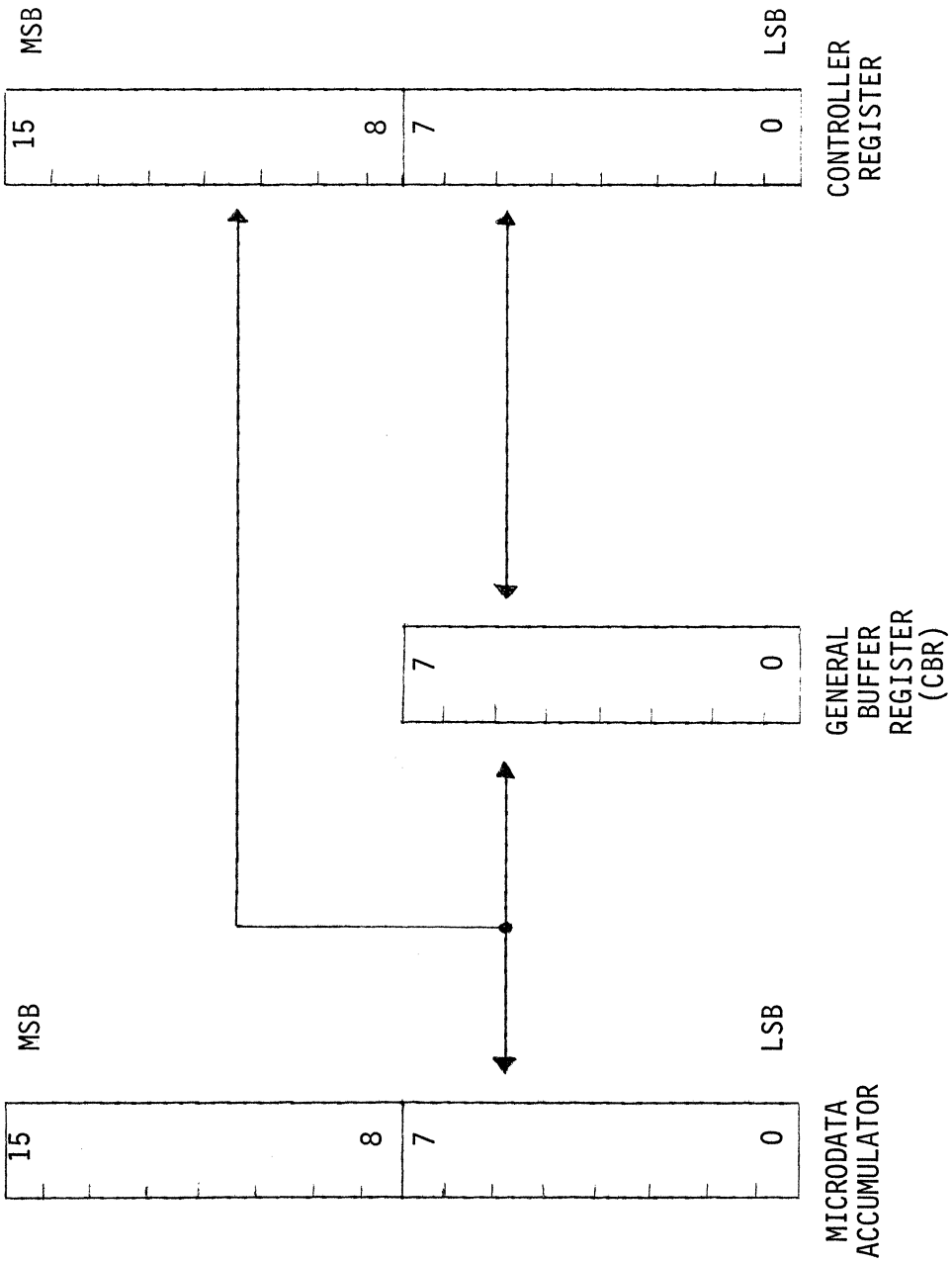


Figure 3.4
GENERAL BUFFER REGISTER OPERATION

Controller registers may also be entered using an output byte from memory (OBM) instruction. This instruction is functionally the same to the controller as an output byte from an accumulator. The following steps occur in transferring information from the computer memory to a controller register:

a) The contents of the desired memory location are transferred to the General Buffer Register.

b) The contents of another memory location are transferred to bit positions 15 through 8 of the desired controller register. At the same time the information in the General Buffer Register is also transferred to the controller register - bits 7 through 0.

Information is transferred from a controller register to the computer memory in the following manner:

a) The contents of register bit positions 15 through 8 are transferred into the desired memory location as register bit positions 7 through 0 are transferred into the General Buffer Register.

b) The contents of the General Buffer Register are transferred into another memory location.

2) The Control and Error (CER) Register has been modified to simplify disk operations with the Microdata byte I/O environment. One output byte from an accumulator or memroy location with an Order Code of 1

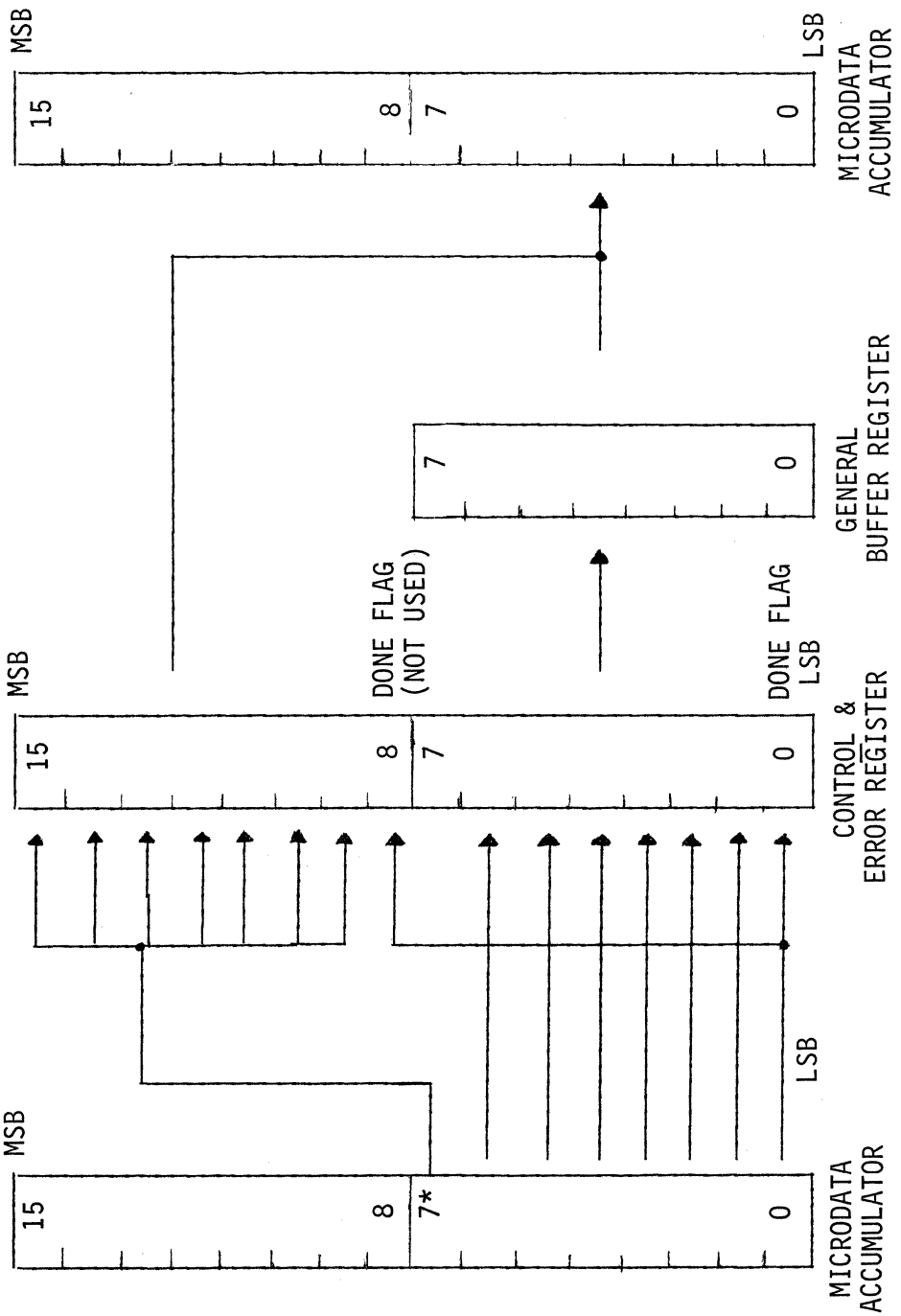
loads the control commands into the C&E Register (bits 8, 6-0), and selectively clears the error portion of this register (bits 15-9) if the most significant bit (MSB) of the output byte is a zero. Figure 3.5 shows the interaction between the C & E Register in the controller and an accumulator in the Microdata computer.

3) In the Microdata controller, a '1' in bit 6 of C & E Register will ENABLE an interrupt to be generated by the controller. There are three (3) ways in which the local interrupt control flip-flop (i.e. bit 6 of the C & E Register) can be controlled:

   a) A Master Clear instruction (output with order code = 7) or depressing the "SAVE" or "RESET" switches on the computer front panel will clear bit 6 of the C & E Register (i.e. disable local interrupts).

   b) Enter the C & E Register (output with order code = 1) with bit 6 in the output byte = 1 to enable interrupts, or bit 6 in the output byte = 0 to disable interrupts.

   c) Output instruction with order code = 6, where bit 6 of the output byte = 1 enables interrupts and bit 6 of the output byte = 1 disables interrupts.



* Bit 7=1 Produces no change in bits 9-15,
Bit 7=0 clears bits 9-15.

Figure 3.5
MICRODATA ACCUMULATOR INERACTION WITH
THE CONTROL & ERROR REGISTER

DISK CONTROLLER INSTRUCTIONS

This section describes the instructions used to specify the operations of Model 3040 Controllers when they are interfaced to a Microdata computer. These instructions are used for both moving-head and fixed-head disks.

Instruction Set

The standard device code address for the Model 3040 Controller will be hexadecimal 06 for the MICRO 800 and MICRO 1600 series computers and has a corresponding interrupt address of $10C_{16}$. The device address and corresponding interrupt address may be modified per user requirements. In the description of the instruction set which follows, "lower half" refer to the least significant and most significant halves of the 16-bit controller registers. Output and Input Buffer Registers are used in the interface to convert the byte I/O commands into 16-bit command transfers and reduce the I/O input commands into two 8-bit byte transfers.

There are no instruction time programming restrictions with the Model 3040 Controller and it uses the standard Byte I/O instructions repertoire of the Microdata computers. The user should refer to the Microdata 800 and Microdata 1600 Reference and Interface manuals for the detailed description of these instructions.

Output Instructions

These instructions are accomplished using an output byte from A, OBA; output byte from B, OBB; or output byte from memory, OBM. Functionally, to the controller they are equivalent. The significant information is in the F field which is 3 bits in length. The following is a description

of the F field corresponding to these three instructions and shows what operation occurs in each of these cases.

- Order Code 0: Load the Output Buffer Register with I/O bus data.

- Order Code 1: Load the Control and Error Register.
  This single byte command transfers bits 0-6 of the selected accumulator into bits 0-6 of the Control and Error Register and does a selective clear on bits 9-15 of the Control and Error Register using bit 15 of the selected accumulator. If bit 15 of the accumulator is a zero, bits 9-15 are cleared; if bit 15 of the accumulator is one, bits 9-15 remain unchanged.

- Order Code 2: Load the Seek Address Register and initiate an Overlap Seek.
  This command will load the upper half of the Seek Address Register with the I/O bus data and load the lower half of the Seek Address Register from the Output Buffer Register and initiate an overlap seek (a head movement without a following data transfer). Bits 15 and 14 specify on which of the disk ports the seek is to take place, and bits 13-0 contain the block address from which the controller can determine which cylinder it should seek to. For 24 sector per track operation, bits 13-0 contain the 14 most significant bits of the 15 bit block address. This instruction can be initiated at any time and will be ignored if on that port,

another seek or a data transfer is currently being executed. The busy error flag for that port's Seek Status Register will be set if this conflict occurs.

- Order Code 3: Load the Seek Address Register and initiate a Word Count/Current Address Sequence.
  This command will load the upper half of the Seek Address Register with the I/O data bus and load the lower half of the Seek Address Register from the Output Buffer Register and initiate the following sequence:
  1. The controller interprets the contents of the Seek Address Register as an address, and transfers it through the Block Address and Arithmetic Check Registers to the Current Address Register.
  2. It then uses this address as a pointer and initiates a two word DMA sequence.
  3. The first word retrieved is interpreted as the initial word count for the ensuing data buffer and is transferred into the Word Count Register.
  4. The second word retrieved is interpreted as the initial core address for the ensuing data buffer and is transferred into the Current Address Register.

- Order Code 4: Load the Block Address Register and initiate a Read.

  This command will load the upper half of the Block Address Register with the I/O bus data and load the lower half of the Block Address Register from the Output Buffer Register and initiate the following sequence:

  1. A seek is initiated to the sector specified by the Block Address Register on the disk port specified by bits 4 and 3 of the Control and Error Register.

  2. When the track and sector are reached, the controller goes through an address verification sequence where it verifies that the correct sector has been reached by reading the Block Address Word and comparing it with the contents of the Block Address Register. This verification sequence is done only for moving-head disks to verify the head movements, and is not needed to verify the electronic head selection circuitry of the fixed head disks.

  3. After the verification sequence is done (if needed), the read sequence will commence where the controller will convert the serial data on the disk into parallel 16-bit words and transfer them into core using the Current Address Register as the pointer as to where to store each word in core.

  4. The read operation will continue until the number of words initially specified in the Word Count Register

has been transferred. As the data is read in from each sector on the disk, a one's complement sum is calculated from the data and compared with the cyclic redundancy check word in that sector to verify the validity of the data.

5. The controller operates on a total sector each time, but transfers only the initial Word Count Register number of words into core. Should the initial value be less than or equal to a sector length, the read operation will terminate at the end of the initial sector after checking the validity of the data. Should the initial value be greater than a sector length, the read operation will go automatically from sector to sector (checking for address verification on each sector if necessary) and will cross both track and cylinder boundaries until the initial Word Count Register value of words has been transferred.

   NOTE: For moveable-head disks, it will take an additional revolution when reading across cylinder boundaries to allow time for the heads to move. Except for this case, all large transfers will go from sector to sector without losing any time between sectors.

6. As each sector is read successfully, the Block Address Register is incremented to point to the next sector. Thus, at the conclusion of the data transfer, the

Block Address Register will point to the sector immediately following the last sector read if the transfer terminated successfully.

7. At the conclusion of the data transfer or whenever an error has been sensed, the Done Flag will be set, the Busy Flag will be cleared, and an interrupt request to the computer will be generated if the interrupt Enable Bit (bit 6 of the Control and Error Register) is set.

- Order Code 5: Load the Block Address Register and initiate a Write.

  This command will load the upper half of the Block Address Register with the I/O bus data and load the lower half of the Block Address Register from the Output Buffer Register and initiate a write sequence. This sequence is the same as for the read sequence with the following exceptions:

  1. In the address verification sequence, the most significant bit of the Block Address Word is tested to see if the sector is write-protected. Trying to write into a write-protected sector will terminate the write operation and set both bits 15 and 9 in the Control and Error Register.

  2. The write operation will transfer words from core to the disk until the initial value of the Word Count Register has been reached. It will

then write the remaining words in the sector (should there be any) as zeros.

3. While it is transferring data to each sector, the controller computes the one's complement sum of the data in the sector and then writes this value as the Cyclic Redundancy Check Word immediately after the data in each sector.

- Order Code 6: Enable or Disable the Interrupt control flip-flop of the disk system using bit 6 of the I/O bus. If bit 6 is a zero, disable the interrupt. If bit 6 is a one, enable the interrupt.

- Order Code 7: Master Clear the controller. This instruction initializes the controller and is equivalent to depressing the Reset or Save switches on the computer front panel.

Input Instructions

The input buffer instructions IBA, IBB, and IBM are also functionally equivalent to the controller. The order code definitions are:

- Order Code 0: Read the Input Buffer Register.

- Order Code 1: Read the upper half of the Control and Error Register. The lower half of the Control and Error Register may then be obtained by reading the Input Buffer Register.

- Order Code 2: Read the upper half of the Seek Status Register. The lower half of the Seek Status Register may then be obtained by reading the Input Buffer Register.

- Order Code 3: Read the upper half of the Block Address Register. The lower half of the Block Address Register may then be obtained by reading the Input Buffer Register.

- Order Code 4-7: Not used.

CONTROLLER OPERATIONS

The following information is provided to help the user better understand the Model 3040 Controller and aid in its programming.

- Master Clear

  The Model 3040 Controller contains its own master clear generator circuit and also receives the master clear signal of the program I/O bus. The master clear function clears all the error information bits, format enable, busy and done bits in the Control and Error Register, clears the interrupt enable bit in the Control and Error Register, and clears all sequence control logic in the controller necessary to initialize the controller.

- The Overlap Seek and the Seek Status Register

  The purpose of the Seek Address and Seek Status Registers is to give the Model 4400/4500 Disk Systems a true overlap seek capacity, which is independent of whether a data transfer is in progress on

another port. An overlap seek is initiated by the execution of the Load SAR and Initiate OVL Seek instruction. There bits 15 and 14 of the Seek Address Register define which of the four disk ports the seek is to take place on, and bits 13-0 define the block address for 12 sector per track operation or the 14 most significant bits of the block address for 24 sector per track operation to which the heads should be moved to. The Disk Select Bit, bit 15 of the Block Address Register, does not need to be defined for the overlap seek operation since all four heads in the moving-head disk drive are attached to the same head positioner mechanism. The overlap seek capability can be used even in a single disk drive system, since any read or write initiation will be automatically queued in the controller until the port on which the data transfer is to take place becomes ready. This queue also alleviates any timing restrictions on when to initiate a read or write sequence.

The completion of an overlap seek on any port will set the done flag in the Control and Error Register, if and only if a data transfer is not active at that time. A program interrupt will also be generated if interrupts are enabled at the time the done flag gets set. Should any overlap seek operations terminate during a data transfer on another port, this fact will not be identified to the program at that time, and it will be up to the user to interrogate the Seek Status Register (bits 12, 8, 4 and 0 for ports 3, 2, 1, and 0, respectively) to determine if any other head movements did terminate during the data transfer should this information be needed.

The hardware will automatically protect against the initiation of overlap seeks if the port in question is presently either active with a data transfer or has its head moving and is not in a condition to enact another seek. In both cases, the seek initiation is ignored and the busy error bit in that port's Seek Status Register is set.

- The Control and Status Registers

Except for the done flag's capability of being set at the end of an overlap seek, the Control and Error Register is used exclusively for data transfers. The error portion of this register, which contains any error information resulting from a data transfer, can be cleared only by program control and set only by the controller upon the detection of any of the nine errors. This portion of the register should be cleared prior to a data transfer initiation, so that any information in it after the data transfer can be only a result of that data transfer.

The control portion of the register contains both control and status information for data transfer operations. The five bits comprising the interrupt enable, format enable, disk unit select bits and the busy bit must be appropriately set by the programmer according to their usage. However, while the read disk, busy and done flags may be set or cleared by a Load CER instruction, they are also under automatic control of the controller. The read disk bit is used to control the direction of DMA transfers and must be controlled for both the word count/current address sequence as well as the read or write operations. The busy flag is automatically set at the time of an Initiate Write or Read instruction and cleared when the data

transfer terminates. The done flag will automatically be cleared (if it is not already) at the time of the Initiate Write or Read instruction and will be set when the data transfer terminates.

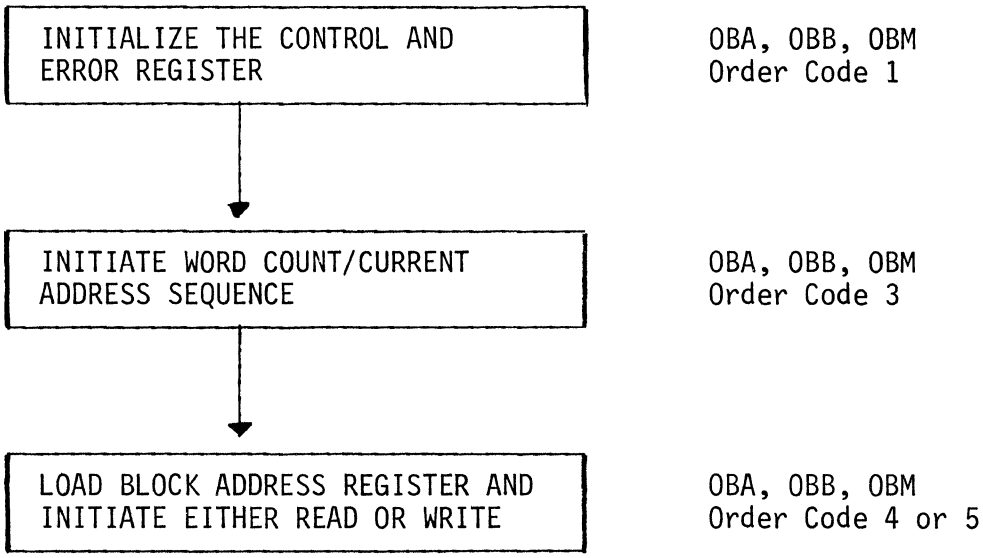
- Word Count/Current Address Sequence

  The word count/current address sequence was designed to allow the user to initialize two of the three basic parameters needed to initiate a data transfer with one programmed I/O instruction. The controller interprets the information transferred during an Initiate WCCA instruction as the address of the first of two consecutive words in core, and initiates a two word DMA sequence to retrieve them. The word count register is a 16-bit register and allows for a full 64K byte transfer from a single data transfer initiation.

- Read or Write Operations

  The design concept of the Model 3040 Controller was to minimize the programming sequence needed to set up and initiate a data transfer and have this one sequence capable of transferring from 1 word to 32,768 without regard to any disk boundaries.

  The sequence to initiate a data transfer is described by the following flow diagram along with the I/O instruction mnemonic used to accomplish each action:



As seen from this flow diagram, the same sequence is used for both read and write operations with the only difference being whether Order Code 4 or 5 is used.

- Data Transfer Monitoring

The Model 3040 Controller is designed to utilize the Read CER and test instructions and interrupt capabilities of the computer. Once the data transfer has been initiated, the user may periodically test for the completion of the data transfer by executing the Jump If Busy or Done is Nonzero instructions with the result of jumping to the specified address if the specified condition is met. If the user chooses not to periodically test for the data transfer completion, he may set the interrupt enable bit at the time he initializes the Control and Error Register for the data transfer, which will result in an interrupt generation upon the completion of the data transfer.

Once the controller has been identified as the interrupting device, or if the periodic done flag testing was used to determine the data transfer completion, the Jump If Error is Nonzero instruction can be used to test if any errors occurred during the data transfer. If any error did occur, the description of the error can be obtained by interrogating bits 14-9 of the Control and Error Register.

The action taken by the program in case of errors will depend on the specific application. However, certain errors may allow recovery techniques while others are invariably fatal. Address Verification, Write Check, Cyclic Redundancy Check, Timing, and Seek Incomplete errors may sometimes be corrected by repeating the current operation (which includes reinitializing the Control and Error Registers). If the error is a recoverable one, it will not persist for more than seven attempts. Beyond seven attempts, it should be considered fatal. If the interrupt scheme was used, the programmer should clear the done flag prior to the execution of an interrupt enable instruction to prevent any false interrupts from occurring.

- Disk Formatting

Before data can be written onto a moving-head disk sector, and hence read from the sector, the sector must be formatted by writing a preamble and Block Address Word at the beginning of each sector. This is accomplished by initiating a write sequence on each sector, the same sequence as if writing data except for the following conditions:

1. The format switch must be manually placed in the FORMAT position.

2. The format enable bit (bit 5 of the Control and Error Register) must be set to a one.

3. The word count must be specified as E_{16} (14_{10}).

4. The data buffer must be following:

   a. the first C_{16} (12_{10}) words must be zero.

   b. the D_{16} (13_{10}) word must be 8000.

   c. the last word of the data buffer is the Block Address word.

Thus, each sector is formatted separately by initiating a write sequence with the above special requirements. It will result in a string of 207 zeros being placed on the disk starting at the sector notch with a one being written on the disk in the 208th bit time (83.2us). The sixteen bits immediately following the single one bit will be the Block Address Word.

- Block Address Word and Sector Write Protection

The last word of the data buffer when formatting a sector is the Block Address Word. For normal operation (i.e., not write-protecting a sector) the most significant bit of this word should be a zero and bits 14-0 are identical to the bits 14-0 which are loaded into the Block Address Register when the write sequence was initiated to format the sector. If it is desired to format the sector in the write-protect mode, the most significant bit (bit 15) of the Block Address Word must be set to a one. Once it is formatted in the write-protect mode, data may be written into the sector by leaving the

format switch in the FORMAT position, which performs as a write protect override switch.

When a sector is formatted, data must be first written into the sector before any valid read operation may be initiated on that sector. Thus, when reformatting a normal sector into a write-protected sector, the data in the sector, if it is to be saved, must first be read into a temporary storage area while the sector is reformatted, and then rewritten into the sector after it has been reformatted.

4. OPERATIONS CHECKOUT

A diagnostic program is used to checkout the disk system. The program is composed of three sections:

- Parameter Specifications, in which the user specifies the configuration parameters and desired controls on diagnostic software;
- Controller Tests, in which the register transfers and interrupt operation of the controller are checked; and
- Disk System Tests, in which Seeking, Reading and Writing Operations, Format features, and Error indicators are checked.

A portion of the Disk System Tests section is the format program which may be used independently to format new disk cartridges.

- Loading the Diagnostic Program

  This sub section describes the procedures for loading the Diagnostic Program into a Microdata 800/1600 computer.

  Required Equipment

  The Diagnostic requires an equipment configuration consisting of:

  - Microdata with 16384 bytes of memory
  - Teletype
  - 3040 Controller
  - One or more disk drives

Diagnostic Program Loading Procedure

- Load the Teletype Operating System (TOS)
- Place the Diagnostic Program paper tape in the paper tape reader;
- Set front panel sense switch 1:

  OFF for serial TTY

  ON for parallel TTY
- Type "R" on TTY

The program will be read in and upon successful loading, the Diagnostic will automatically assume control and the input dialogue will begin.

Note: The program occupies location $0\text{-}1FD2_{16}$ and is not relocatable.

Alternate Diagnostic Program Loading Procedure

- Load the proper bootstrap (i.e., for either serial or parallel TTY) in the following manner:

  1) Place the TTY in the off-line mode, place the reader control lever to the "free" position and enable the Teletype reader. Type control and Q.

  2) Place the TTY in the on-line mode and insert the bootstrap tape in the reader with the first rub-out character at the read station. Set the reader control lever in the stop (center) position.

  3) Set the front panel sense swtiches as follows:

  4) Sense switch 1: off for serial TTY interface
     on for parallel TTY interface

  5) Sense switch 2: Must be off.

6) Sense switch 3: Must be off.

7) Sense switch 4: Must be on. This selects the bootstrap loader whenever the run switch is selected and was preceded by a reset.

8) Press the reset and the run switches and the system will wait for the Teletype reader to be started.

9) Press the TTY reader lever to the start position.

- After the bootstrap has been read into the system, set the TTY reader control lever in the stop position.

- Remove the bootstrap tape from the reader and insert the diagnostic program tape.

- Press the TTY reader level to the start position.

The program will be read in and upon successful loading, the Diagnostic will automatically assume control and the input dialogue will begin.

If the diagnostic program has been loaded into the computer memory, the TOS can be used to restart the program. Type a "G" and then a zero to initiate the first prompt.

- Specifying the Test Parameters

The parameters that control the operation of the Diagnostic are input by the user through the front panel switch register in response to prompts typed out on the teletype. The specification dialogue is divided into five parts:

- Describing the disk configuration;
- Indicating the portion of the disk to be tested;
- Indicating the interrupt address;
- Indicating whether or not disk formatting between passes is desired;
- Specifying a variety of Diagnostic operation and error type-out controls.

Disk Configuration Specification

The dialogue begins with the prompt:

ENTER DISK TEST INFORMATION

Set the front panel sense switches using the code described below to describe the configuration of the disk on each port (0-3).

NOTE: Each of the four switches must be set three times to completely define each port. Further, after all ports have been defined, switch no. 4 must be set to a "1" to proceed to the next prompt and continue running the diagnostic program.

DISK TEST SPECIFICATION CODE

FIRST DISK TEST INFORMATION ENTRY

Switch	Information Entered	Code
1,2	Unit (port) number	The port number, 0-3, expressed as a binary number.
3	Type of disk	0 = fixed head disk 1 = moving head disk
4	Are all disk parameters specified	0 = enter additional parameters 1 = done - all parameters specified

After the sense switches are set to the desired positions, depress the Run switch.

DISK TEST SPECIFICATION CODE

SECOND DISK TEST INFORMATION ENTRY

Switch	Information Entered	Code
1	Track Density	0 = 100 tracks/inch (Model 43) 1 = 200 tracks/inch (Model 44)
2	Number of sectors per track	0 = 12 sectors/track 1 = 24 sectors/track
3	(not used)	0
4	Partial disk test specification	0 = test full disk *1 = test less than full disk

*If a "1" is specified:

a) For a fixed-head disk - you will be given the prompt:

TYPE NUMBER OF HEADS

Type the number (hexadecimal) of heads to be tested.

b) For a moving-head disk - you will be given the prompt:

TYPE MAX CYLINDER

Type the maximum number (hexadecimal) of cylinder to be tested.

DISK TEST SPECIFICATION CODE

THIRD DISK TEST INFORMATION ENTRY

Switch	Information Entered	Code
1	Removable cartridge test indicator	0 = do not test removeable cartridge 1 = test removeable cartridge
2	Fixed cartridge test indicator	0 = do not test fixed cartridge 1 = test fixed cartridge
3	(not used)	0
4	(not used)	0

When all these parameters have been entered correctly the prompt:

ENTER DISK TEST INFORMATION

will be repeated. In response, enter the description of the next port to be tested. If information on all ports to be tested has been entered, set sense switch No. 4 to "1" and depress Run to go on to the next prompt. The Diagnostic will go on to the next prompt automatically when the disks on all four ports have been specified.

Controller Device Code

The diagnostic next types out

TYPE CONTROLLER DEVICE CODE

In response, type the assigned device code on the TTY (hexadecimal 6 is standard) and depress the return key on the TTY.

Disk Formatting Control

The next prompt in the dialogue is

ENTER FORMAT LOOP CONTROL

In response, set the front panel sense switches using the code described below:

FORMAT LOOP CONTROL CODE

Switch	Information Entered	Code
1	Controls the number of times the disk is to be formatted	0 = format the disk and run the seek all blocks test only once 1 = reformat the disk and run seek all blocks test on every pass of the test
2	Controls whether entire diagnostic or just formatting portion is to be run.	0 = run complete diagnostic 1 = run formatting routine only
3	Controls whether or not a special format test is run	0 = special format test not run 1 = special format is run
4	(Not used)	0

After the switches have been set, depress the Run switch on the front panel of the computer.

Diagnostic Operation/Type Out Controls

The final prompt is

ENABLE FORMAT SWITCH, ERROR AND TYPE OUT CONTROLS

Set the format switch on the rear of the controller to the "FORMAT" position. Then, set the sense switches on the front panel according to the code described below to indicate which of a variety of operation and type-out options are desired.

DIAGNOSTIC CONTROL CODES

Switch	Control Description	Code
1	Controls whether Diagnostic repeats current operation or continues on with test.	0 = continues with test 1 = repeats current operation (Always set to zero initially)
2	Controls whether or not the Diagnostic halts on an non-recoverable error	0 = halts after seven occurrences of an error 1 = continues on errors
3	Controls whether or not error type outs are made	0 = type out all errors 1 = delete type outs
4	Controls typing out of data errors detected on a data compare operation	0 = types out only first eight data errors 1 = types out all data errors

After the switches have been set, depress the Run switch.

- Diagnostic Program Operation

After having received all of the control parameter inputs, the diagnostic tests the controller registers, formats the disk, tests the features of the disk controls, and tests the reading and writing of the disk for each port being exercised.

The following describes these tests in somewhat more detail and indicates how to use an option of the diagnostic to assist with trouble shooting. If any of the tests described below are not performed satisfactorily, an error results and an error number is printed out. See Chapter 5 for descriptions of these error messages:

- Controller Tests

  The test section of the diagnostic begins with three controller tests. These tests, which check the controller only, do not require a disk be on the system in order to be performed.

  1) Control and Error Register Test:

     The transmission paths between the computer and the Control and Error Register are checked by sequentially setting and reading back bits. A reset command is issued after each bit is set and the register is checked to assure that the bit cleared properly.

  2) Interrupt Test:

     The diagnostic generates an interrupt by setting the Done bit in the Control and Error Register using the CER Load instruction and then checks to see that an interrupt is properly generated, that it used the correct vector address, and that it occurs within the maximum allowable time.

  3) Word Count and Current Address Test:

     The transmission paths between the controller Block Address Register and the computer are checked by transmitting back and forth various sequences of zeros and ones. This test

also verifies that the word count and current address sequence terminates.

- Disk Operation Tests

The next sequence of tests checks the operation of the entire disk system.

1) Logical Address Interlock and Overlap Seek Test:

The Seek Status Register is examined to see if the selected disk is ready to Seek, Read, or Write, then an overlap seek is performed to sector zero, and the disk unit is checked to make sure that the hardware and busy error flags clear within 300 milliseconds. Then five more overlap seeks are done to check for various timing and logical address interlock errors. They are:

- Seek to maximum sector plus one to test logical address interlock.
- Seek to sector zero to check proper operation.
- Seek to maximum sector to check proper operation.
- Overlap seek while simulating a data transfer on the same port to test the busy error indication.
- Overlap seek while simulating a data transfer on another port to check proper operation.

2) Format Test:

NOTE: The Format Enable switch must be in the FORMAT position during this test.

This test formats the disk and then writes the block address in the data portion of each sector. It then reads back each

sector comparing the block address with the data written in the sector to check that the formatting was done correctly. Then two other tests of controller functions are performed:

- Write an incorrect block address in sector zero and verify that it causes an address verification error.
- Format disk in Write Protect mode to check for proper operation.

Then the disk is reformatted normally and the test continues.

3) Special Format Test:

If sense switch No. 3 was set to a "1", in response to the Format Loop Control prompt, two additional tests are performed. The message DISABLE FORMAT SWITCH is typed out on the Teletype and the user disables the Format Switch and depresses RUN. The diagnostic will attempt to format the disk and check for the proper error indications. Also a Write operation will be attempted in a write-protected sector to test the error indicators. After these two tests, the message ENABLE FORMAT SWITCH will be typed out, and after the RUN key is pressed, the tests will continue.

4) Seek All Blocks Test:

Seeks are performed to sector zero, then to the maximum sector, then sector one, then to maximum sector minus one, and so on through the disk, verifying on each seek that the proper location was reached.

5) Random Seek Test:

A series of 512 random block addresses are generated and Seek/Read operations are performed to these sectors. The diagnostic verifies that the correct location is reached on each seek.

6) Single Block Data Test:

This test writes a fixed data pattern in each sector of the disk using single block transfers, reads back the data in single- and multiple-block transfers, and checks all data transfers for accuracy.

7) Multiple Block Data Test:

This test writes the entire disk with a fixed data pattern using multiple block transfers and then reads it back using multiple block transfers, and single- and partial block transfers. All transfers are checked for accuracy.

When these tests have been completed for the fixed and removable disks on the first port, as indicated by the disk test information, the test automatically runs for each of the other ports indicated, and then recycles back to the first port again. If the format portion of the test is not to be redone (as indicated by the test control inputs), a message DISABLE FORMAT SWITCH will be typed out. Set the Format Switch to the NORMAL position and press RUN. The diagnostic will continue to recycle until stopped manually or until an error halt has occurred.

- Trouble Shooting Aid

  Sense switches 1, 2, and 3 can be used as a trouble shooting aid. If an error occurs and the computer halts, setting switches 1, 2, and 3 and depressing RUN forms a continuous scope loop on the test which caused the error.

  Whenever switch 1 is set, the test currently being performed will be repeated continuously until switch 1 is reset.

- Formatting Disk Cartridges

  When using only the format portion of the diagnostic, enter all the normal parameters for the port on which the disk to be formatted is attached. Be sure the Format Enable switch is in the FORMAT position and that sense switch 2 is set in the Format Loop Control prompt. When the formatting operation is complete, the message END FORMAT OPERATION will be typed out and the program will halt.

5. DIAGNOSTIC PROGRAM

This chapter presents a detailed description of the Diagnostic Program for a Model 3040 Disk System when it is interfaced with a Microdata computer.

PROGRAM DESCRIPTION

The Table of Tests and Errors provides a fast reference for the error messages and the tests that produce them. Following the table is an explanation of what each test does and how to interpret the error messages.

TABLE 5-1

TESTS AND ERRORS

TEST NO.	TEST DESCRIPTION	ERROR NUMBER
1	Control and Error Register Test	1,2
2	Interrupt Test, Skip on Busy Test, Skip on Done Test	0,3
3	Word Count/Current Address Test	4
4	Logical Address Interlock and Overlap Seek Test	
4.1	Test Unit Ready to Seek, Read or Write	5
4.2	Seek to Sector 0, Hardware Error and Busy Flags clear	6, 206
4.3	Overlap Seek to maximum sector +1; test Logical Address Interlock	7, 11-14
4.4	Overlap Seek to Sector 0	15, 17-22
4.5	Overlap Seek to Maximum Sector	23, 25-30
4.6	Overlap Seek with Simulated Data Transfer	31, 33-36

TABLE 5-1 (continued)

TEST NO.	TEST DESCRIPTION	ERROR NUMBER
4.7	Overlap Seek with simulated data transfer on another port.	37, 41-44
4.8	Seek/Read Maximum sector +1; test logical Address Interlock, Skip on Error Test	45-47
4.9	Seek/Write Maximum Sector +1; test logical Address Interlock, Skip on Error Test	50-52
5	Format Test (for Moving-Head Disks only)	
5.1	Format disk with Write Protect Bit = 0	53-55
5.2	Write block number in data portion of each block	75-100
5.3	Read each block and verify block address is in data portion	101-104
5.4	Format Sector 0 with incorrect block address	173-175
5.5	Attempt to read Sector 0, check for Address Verification Error	176-177
5.6	Attempt to write Sector 0, check for Address Verification error	200-201
5.7	Format all sectors in write-protect mode Write Protect Bit = 1	56-60
5.8	Write maximum block number minus block number in data portion of each sector	105-110
5.9	Read and verify that maximum block number minus block number is in data portion of each sector	111-114
5.10*	Attempt to format with format switch normal; check for format error	202-203
5.11*	Attempt to write with format switch normal and sectors write-protected; check for Write Lockout Error	204-205
5.12	Reformat the disk with Write Protect Bit = 0	64-65

*Special format tests which are executed only if requested by the user in the test specification sector of the Diagnostic Operation.

TABLE 5-1 (continued)

TEST NO.	TEST DESCRIPTION	ERROR NUMBERS
6	One Word Write/Read Test	
6.1	Write the block number in the data portion of all sectors	115-120
6.2	Read all sectors and verify that they were written correctly	121-124
7	Seek All Blocks Test	125-130
8	Random Seek Test	131-134
9	Single Sector Write/Read Test	
9.1	Write entire disk with data pattern one sector at a time	135-141
9.2	Read entire disk one sector at a time and verify accuracy	142-146
9.3	Read entire disk 1-1/2 sectors at a time and verify accuracy	147-153
10	Multiple Sector Write/Read Test	
10.1	Write entire disk 1-1/2 sectors at a time with fixed data pattern	154-160
10.2	Read entire disk 1-1/2 sectors at a time and verify accuracy	161-165
10.3	Read entire disk one sector at a time and verify accuracy	166-172

NOTE: A "WORD" is defined to be 16 bits in length, unless specifically stated otherwise.

TEST NO. 1 - Control and Error Register Test

Description:

This test sequentially transmits one bit at a time out from the computer and reads it back from the Control and Error Register (CER) to verify the transmission. It checks bit numbers 1-6, one bit at a time, and bits 0 and 8 together. After each bit has been successfully received and read back from the controller, a Reset command is issued and the test checks to verify that the proper bit was cleared. Note that bits 2-4 are not affected by a Reset command, so they are ignored in this portion of the test.

Errors:

001 - Indicates that a bit did not get set in the CER when transmitted from the computer.

002 - Indicates that one of the bits set in the CER did not clear when a Reset command was issued.

TEST NO. 2 - Interrupt Test

Description:

An interrupt receive address is loaded into the interrupt vector location and an interrupt is generated by setting the interrupt enable and done bits in the CER. The program verifies that an interrupt is generated to the proper address within the maximum amount of time.

Errors:

000 - Indicates that the interrupt was to an improper address. The message "ILLEGAL INTERRUPT FROM ADDRESS _____" is typed

out, where the address is the point in the program being executed when the interrupt occurred. This error message will be printed at any time during the program when an illegal interrupt occurs.

003 - Indicates that no interrupt occurred when the interrupt enable and done bits were set in the CER.

TEST NO. 3 - Word Count/Current Address Test

Description:

This test transmits selected values from the computer to the Block Address Register (BAR) in the controller using the word count/current address sequence command. Each value is loaded into an accumulator and transmitted to the BAR. Then the contents of the BAR are checked. The first value transmitted is all zeros, initiating the word count/current address function to address 0. The second value transmitted is 177775. The next value transmitted is alternating ones and zeros, starting with a zero in the least significant bit position (125252). The final value transmitted is 52524.

Errors:

004 - Indicates that the word count/current address sequence did not load the proper value into the BAR.

TEST NO. 4 - Logical Address Interlock and Overlap Seek Test

This test is composed of the following sub-tests described below:

Sub-Test 4.1

Description:

This sub-test interrogates the Seek Status Register (SSR) to verify that the selected disk is ready to seek, read, or write.

Errors:

005 - Indicates that the disk is not ready to seek, read or write.

Sub-Test 4.2

Description:

This sub-test performs an overlap seek to Sector 0 and verifies that the hardware error and busy flags are both cleared.

Errors:

006 - Indicates that the hardware error and/or busy flags did not clear with a seek to Sector 0.

206 - Indicates that the Ready to Seek, Read or Write line did not return to zero within the maximum allowable 300 milliseconds when the seek to Sector 0 was attempted.

Sub-Test 4.3

Description:

This sub-test executes a seek to the maximum sector plus one and tests the Logical Address Interlock. This test and the following overlap seek tests are subroutine L4 to perform the seeks and the error checking.

Subroutine L4 operates as follows: It first clears the error and done flags in the CER, issues the overlap seek, checks to see if the Ready to Seek, Read, or Write line returns to zero within a maximum of 300 milliseconds. Next the values in the SSR and all ports other than the

port being tested are checked to make sure they have not changed, and the flags that were set during this operation are checked to verify they were handled properly. These include busy, hardware error and the done flags.

Seeking to the maximum sector plus one should generate a Logical Address Interlock hardware error. Also, the done flag should be set but the busy flag should not be set.

Errors:

007 - Indicates that the Ready to Seek, Read, or Write line did not return to zero within 300 milliseconds after an overlap seek was executed.

011 - Indicates that a portion of the SSR associated with a port other than the port being tested changed during the execution of an overlap seek.

012 - Indicates that the busy flag was set during an overlap seek when it should not have been.

013 - Indicates that a hardware error failed to occur but should have during an overlap seek.

014 - Indicates that the done flag failed to get set upon completion of an overlap seek.

Sub-Test 4.4

Description:

This sub-test performs an overlap seek to Sector 0 and does the checking described in Sub-Test 4.3. In this case, since the proper operation of the Logical Address Interlock in Sub-Test 4.3 insures that the head will be positioned over Sector 0, the done flag should be set. The test

verifies that it is set and that no false errors are set during this operation.

Errors:

015 - Indicates that the Ready to Seek, Read, or Write line did not return to zero within 300 milliseconds after an overlap seek was executed.

017 - Indicates that a portion of the SSR associated with a port other than the port being tested changed during the execution of an overlap seek.

020 - Indicates that the busy flag was set during an overlap seek when it should not have been.

021 - Indicates that a hardware error occurred on the overlap seek when it should not have.

022 - Indicates that the done flag failed to get set upon completion of an overlap seek.

Sub-Test 4.5

Description:

This sub-test performs an overlap seek to the maximum sector and performs the checks described in Test 4.3. In this case, the done flag should be set but neither the hardware error nor the busy flags should be set in the SSR.

Errors:

023 - Indicates that the Ready to Seek, Read, or Write line did not return to zero within 300 milliseconds after an overlap seek was executed.

025 - Indicates that a portion of the SSR associated with a port other than the port being tested changed during the execution of an overlap seek.

026 - Indicates that the busy flag was set during an overlap seek when it should not have been.

027 - Indicates that a hardware error occurred on the overlap seek when it should not have.

030 - Indicates that the done flag failed to get set upon completion of an overlap seek.

Sub-Test 4.6

Description:

This sub-test attempts an overlap seek to the maximum sector while simulating a data transfer on the same port. The data transfer is simulated by setting the Pseudo Busy Flag flip flop using the Word Count/Current Address operation and also loading the number of the port being tested into the CER. When the overlap seek is attempted under these conditions, a busy flag should be set and the hardware error and done flags should not be set.

Errors:

031 - Indicates that the Read to Seek, Read, or Write line did not return to zero within 300 milliseconds after an overlap seek was executed.

033 - Indicates that a portion of the SSR associated with a port other than the port being tested changed during the execution of an overlap seek.

034 - Indicates that the busy flag was not set on the overlap seek when it should have been.

035 - Indicates that a hardware error occurred during the overlap seek operation when it should not have.

036 - Indicates that the done flag was erroneously set during the overlap seek operation.

Sub-Test 4.7

Description:

This sub-test performs an overlap seek while a simulated data transfer on another port is being executed. The data transfer is simulated by leaving the Pseudo Busy Flip flop set but alternating the unit select in the CER to the number of a port other than the one being tested. Then a seek to the maximum sector is performed. No changing of cylinders is required since the head was properly positioned over this maximum sector before the test was initiated. During the test, the busy flag should be cleared. No hardware error should occur, and the done flag should not be set since there is a data -transfer in progress.

Errors:

037 - Indicates that the Ready to Seek, Read, or Write line did not return to zero within 300 milliseconds after an overlap seek was executed.

041 - Indicates that a portion of the SSR associated with a port other than the port being tested changed during the execution of an overlap seek.

042 - Indicates that the busy flag was set during an overlap seek when it should not have been.

043 - Indicates that a hardware error occurred on the overlap seek when it should not have.

044 - Indicates that the done flag was erroneously set during the overlap seek operation.

Sub-Test 4.8

Description:

In this sub-test, a Seek/Read operation to the maximum sector plus one is attempted using subroutine L5. The Seek/Read command is issued and the program waits for the done flag to be set. It verifies that a hardware error is indicated in the SSR and that the Logical Address Interlock error is properly displayed in the CER.

Errors:

045 - Indicates that the controller did not terminate the operation attempting to read the maximum sector plus one in the maximum allowable time.

046 - Indicates that the CER failed to show the occurrence of a Logical Address Interlock after an attempt to read the maximim sector plus one.

047 - Indicates that the SSR did not properly show a hardware error after the attempt to read the maximum sector plus one.

Sub-Test 4.9

Description:

This test attempts to perform a Seek/Write to the maximum sector plus one doing the same checks as in Sub-Test 4.8.

Errors:

050 - Indicates that the controller did not terminate the operation attempting to write the maximum sector plus one in the maximum allowable time.

051 - Indicates that the CER failed to show the occurrence of a Logical Address Interlock after attempt to write the maximum sector plus one.

052 - Indicates that the SSR did not properly show a hardware error after the attempt to write the maximum sector plus one.

TEST NO. 5	- Format Test (For Moving-Head Disks Only)

This test is composed of the sub-tests described below:

Sub-Test 5.1

Description:

In this part of the test, the disk is formatted for normal operation (Write Protect bit is zero) using the subroutine F15. This subroutine is used whenever a format operation is being performed. It sets the format enable bit in the CER, moves the proper word count pointer to the Word Count Register, initiates a Word Count/Current Address sequence, and then initiates a format write to the selected sector. The program then checks that the done flag gets set within the maximum allowable time. When the done flag has been set, the CER is checked to verify that no error has occurred and that the busy flag is not set. Then the program compares the value of the Block Address Register (BAR) with the address of the block to be written. Note that the BAR is not incremented at the end of a format sequence as it is at the end of a normal write operation.

Errors:

053 - Indicates that the done flag did not get set in the maximum allowable time after a sector was formatted. Note that the BAR should contain the number of the block being formatted at the time the error occurred.

054 - Indicates that the CER indicated an error occurred when a

sector was being formatted.

055 - Indicates that the contents of the BAR, which should equal the number of the block being formatted, are incorrect.

Sub-Test 5.2

Description:

In this sub-test the block address of each sector is written in the first word of the data portion of that sector using subroutine W11.

Errors:

075 - Indicates that the done flag was not set in the maximum allowable time when attempting to write the block number in the data portion of a sector.

076 - Indicates that the CER indicated an error occurred during the data transfer when attempting to write the block number into the data portion of a sector.

077 - Indicates that the data in the buffer was modified during the write operation.

100 - Indicates that the second word in the buffer was modified during the one-word write operation when attempting to write the block number in the data portion of the sector.

Sub-Test 5.3

Description:

In this sub-test, each sector is read to verify that the block address was written correctly in the data portion of the sector. Upon successful completion of this test, if the third Format Loop Control digit typed was a one, the message "END OF FORMAT OPERATION" is typed out and the computer halts.

Errors:

101 - Indicates that the done flag was not set in the maximum allowable time when attempting to read the block number in the data portion of a sector.

102 - Indicates that the CER indicated an error occurred during the data transfer wehn attempting to read the block number from the data portion of a sector.

103 - Indicates that the data in the buffer was modified during the read operation.

104 - Indicates that the word in the buffer which is one greater than the word count was modified during the single sector read when attempting to read the block number in the data portion of the sector.

Sub-Test 5.4

Description:

This sub-test formats the entire disk with incorrect block numbers.

Errors:

173 - Indicates that the done flag did not get set in the maximum allowable time after a sector was formatted.

174 - Indicates that the CER indicated an error occurred when a sector was being formatted.

175 - Indicates that the contents of the BAR, which should equal the number of the block being formatted, are incorrect.

Sub-Test 5.5

Description:

In this sub-test an attempt is made to read Sector 0 by issuing a read

instruction. The value in the CER should be 9105_{16} indicating an Address Verification error occurred during the read operation.

Errors:

176 - Indicates that the controller did not terminate the read operation in the maximum allowable time.

177 - Indicates that the contents of the CER at the end of the read operation were not waht they should have been.

Sub-Test 5.6

Description:

In this sub-test, an attempt is made to write in Sector 0. The expected value in the CER is 9101_{16} indicating an Address Verification error occurred during the write operation.

Errors:

200 - Indicates that the controller did not terminate the write operation in the maximum allowable time.

201 - Indicates that the contents of the CER at the end of the write operation were not what they should have been.

Sub-Test 5.7

Description:

In this sub-test, subroutine F15 is used to format the disk with every sector being write-protected. This is done by setting the write-protect bit (the most significant bit) in the Block Address Word.

Errors:

056 - Indicates that the done flag did not get set in the maximum allowable time after a sector was formatted.

057 - Indicates that the CER indicated an error occurred when a

sector was being formatted.

060 - Indicates that the contents of the BAR, which should equal the number of the block being formatted, are incorrect.

Sub-Test 5.8

Description:

This sub-test using subroutine W11 writes in the data portion of each sector a value equal to the maximum block number minus the block number of the sector being written. If the format switch is enabled these write operations should be executed.

Errors:

105 - Indicates that the done flag was not set in the maximum allowable time when attempting to write the block number in the data portion of a sector.

106 - Indicates that the cer indicated an error occurred during the data transfer when attempting to write the block number into the data portion of a sector.

107 - Indicates that the data in the buffer was modified during the write operation.

110 - Indicates that the second word in the buffer was modified during the one word write operation when attempting to write the block number in the data portion of the sector.

Sub-Test 5.9

Description:

In this sub-test, each sector is read to verify that the value of the maximum block number minus the block number was correctly written in the sector.

Errors:

111 - Indicates that the done flag was not set in the maximum allowable time when attempting to read the block number in the data portion of a sector.

112 - Indicates that the CER indicated an error occurred during the data transfer when attempting to read the block number from the data portion of a sector.

113 - Indicates that the data in the buffer was modified during the read operation.

114 - Indicates that the word in the buffer which is one greater than the word count was modified during the single sector read when attempting to read the block number in the data portion of the sector.

Sub-Test 5.10

Description:

If sense switch 3 was set when the Format Loop Control parameters were entered, a message requesting that the operator disable the format switch will be typed out; otherwise the diagnostic will continue with Sub-Test 5.12. Once the format switch has been disabled and the RUN key has been depressed, subroutine F5 will be used to attempt to format Sector 0. This attempt to format the disk with the format switch disabled should result in the value $A101_{16}$ being displayed in the CER.

Errors:

202 - Indicates that the controller did not terminate the read operation in the maximum allowable time.

203 - Indicates that the contents of the CER at the end of the read operation were not what they should have been.

Sub-Test 5.11

Description:

In this sub-test, an attempt is made to write into Sector 0 with the format switch disabled. This should result in a Write Lockout error indicated by the value 8301_{16} in the CER since the sector is write protected. At the conclusion of this test, a message telling the operator to enable the format swtich will be typed out so that the format test can be continued.

Errors:

204 - Indicates that the controller did not terminate the write operation in the maximum allowable time.

205 - Indicates that the contents of the CER at the end of the write operation were not what they should have been.

Sub-Test 5.12

Description:

This sub-test formats the entire disk in the normal mode (Write Protect Bit = 0) using subroutine F15.

Errors:

064 - Indicates that the done flag did not get set in the maximum allowable time after a sector was formatted.

065 - Indicates that the CER indicated an error occurred when a sector was being formatted.

066 - Indicates that the contents of the BAR, which should equal the number of the block being formatted, are incorrect.

TEST NO. 6	- One Word Write/Read Test

This test is composed of the sub-tests described below:

Sub-Test 6.1

Description:

In this sub-test, the block address of each sector is written in the first word of the data portion of that sector. This test is performed by subroutine W11, which is also used in the Sub-Tests 5.2 and 5.8.

The operation of W11 is as follows: It sets up the parameters for the read/write subroutine and then writes all sectors, beginning with sector zero and writing every other sector. The reason for this interlace is to get maximum efficiency by providing the program with the time it needs to perform the diagnostic checks between sectors rather than wasting entire disk revolutions.

Errors:

115 - Indicates that the done flag was not set in the maximum allowable time when attempting to write the block number in the data portion of a sector.

116 - Indicates that the CER indicated an error occurred during the data transfer when attempting to write the block number into the data portion of a sector.

117 - Indicates that the data in the buffer was modified during the write operation.

120 - Indicates that the second word in the buffer was modified during the one word write operation when attempting to write the block number in the data portion of the sector.

Sub-Test 6.2

Description:

In this sub-test, all sectors are read, beginning with sector zero and reading every other sector, to verify that the information written in Sub-Test 6.1 was written correctly.

Errors:

121 - Indicates that the done flag was not set in the maximum allowable time when attempting to read the block number in the data portion of a sector.

122 - Indicates that the CER indicated an error occurred during the data transfer when attempting to read the block number from the data portion of a sector.

123 - Indicates that the data in the buffer was modified during the read operation.

124 - Indicates that the word in the buffer which is one greater than the word count was modified during the single sector read when attempting to read the block number in the data portion of the sector.

TEST NO. 7 - Seek All Blocks Test

Description:

Using subroutine W11, the combination Seek/Read instruction is executed on Sector zero, and since the first word of the data portion of all sectors contains their respective block numbers, it can verify that the appropriate sector is reached and read. The same operation is performed on the maximum sector, then on Sector one, then on the maximum sector minus one, and so on

until all sectors have been read. This test exercises the head positioning movement and verifies the operation of the Sector Counter on the moving-head disk, and verifies the head selection electronics and the Sector Counter on the fixed-head disk. Notice that for the moving-head disk, this method of operation verifies that moving the head across the center track a large number of times does not distort the information on that track.

Errors:

125 - Indicates that the done flag was not set in the maximum allowable time when attempting to read the block number in the data portion of a sector.

126 - Indicates that the CER indicated an error occurred during the data transfer when attempting to read the block number from the data portion of a sector.

127 - Indicates that the data in the buffer was modified during the read operation.

130 - Indicates that the word in the buffer which is one greater than the word count was modified during the single sector read when attempting to read the block number in the data portion of the sector.

TEST NO. 8 - Random Seek Test

Description:

In this test, a series of 512 seeks to random sectors is performed. After each seek, the data portion of the sector (which contains the block number) is read to verify that the correct sector was reached. Subroutine W11 is

used to perform these operations.

Errors:

131 - Indicates that the done flag was not set in the maximum allowable time when attempting to read the block number in the data portion of a sector.

132 - Indicates that the CER indicated an error occurred during the data transfer when attempting to read the block number from the data portion of a sector.

133 - Indicates that the data in the buffer was modified during the read operation.

134 - Indicates that the word in the buffer which is one greater than the word count was modified during the single sector read when attempting to read the block number in the data portion of the sector.

TEST NO. 9 - Single Block Write/Read Test

Sub-Test 9.1

Description:

In this test, a data pattern that fills the entire sector is written in each sector - one sector at a time. The pattern used is constructed as follows: (a) the first word of every sector is the complement of the block number to help in the identification of an incorrect sector; (b) each of the next fifteen 16-bit words contains a pattern of alternating ones and zeros expressed as 125252_8; (c) the next sixteen words are all zeros; (d) the next sixteen words are formed by shifting a zero through a pattern of ones starting with the zero in the least significant bit position and moving it

to the most significant position; (e) the next sixteen words are alternating patterns of 107070_8 and its complement repeated eight times; (f) the next sixteen words are alternating ones and zeros expressed as 52525_8; (g) the next sixteen words are a data pattern which shifts a one through a pattern of zeros, starting with the one in the least significant bit position and moving it to the most significant bit position; (h) the next sixteen words are all ones (177777); (i) the last sixteen words are alternating words of all ones and all zeros starting with the word of all ones. The above data pattern of 128 words is repeated as necessary to fill the sector.

The subroutine that writes the data on the disk for this test is DRW. It controls the interlacing to insure that maximum disk efficiency is obtained. It sets up the parameters for RW. This routine can be used for either reading or writing.

RW operates as follows: After initiating the write or read operation, it waits for the done flag to be set. After the done flag is set, the CER is checked for the occurrence of erros and the Block Address Register value is checked to be sure it was incremented by the correct amount. The contents of buffer location BUF1 (data) is compared with the contents of buffer location BUF2 (read/write buffer) to insure that the data was not modified during the write operation and was read correctly during the read operation.

If switch 4 is set, the computer will print all data errors; if not, the program will print only the first eight data errors found. The word following the last word in the read/write buffer is always checked to make sure it was not modified during the operation.

The RW subroutine is entered for the write portion of the test from DRW. This subroutine writes every third or every sixth sector on the disk depending upon whether a one sector or two sector write is being employed. This interlacing, which requires three passes through the disk in order to write every sector, is done to provide enough program time to do the necessary comparison between writes without losing an entire disk revolution.

Between every write operation, the block n-mber in BUF1 and BUF2 is changed but no other changes are made in the data pattern.

Errors:

135 - Indicates that the controller did not complete the write function in the maximum allowable time.

136 - Indicates that the CER indicated an error occurred during the transfer of the data pattern.

137 - Indicates that the BAR did not have the proper value after the termination of the operation.

140 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during this buffer compare test are typed out.

141 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

Sub-Test 9.2

Description:

In this sub-test, the entire disk is read one sector at a time. The subroutine DRW is used to call RW. DRW reads every fourth or every eighth sector depending

upon whether a one or two sector read is required. This interlacing permits the checks to be done between read operations rather than wasting an entire disk revolution after each read operation.

The data pattern in each sector is compared against what it should be to verify that the write operation in sub-test 9.1 were done correctly.

Errors:

142 - Indicates that the controller did not complete the read function in the maximum allowable time.

143 - Indicates that the CER indicated an error occurred during the transfer of the data pattern.

144 - Indicates that the BAR did not have the proper value after the termination of the operation.

145 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during this buffer compare test are typed out.

146 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

Sub-Test 9.3

Description:

In this sub-test, DRW is used to read the entire disk 1 1/2 sectors at a time while verifying the data portions on each sector. This tests the multiple sector read operations.

Errors:

147 - Indicates that the controller did not complete the read function in the maximum allowable time. Note that if the value in the BAR is one greater than it should be, the error occurred during the reading of the second sector of the multiple sector operation.

150 - Indicates that the CER indicated an error occurred during the transfer of the data pattern.

151 - Indicates that the BAR did not have the proper value after the termination of the operation.

152 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during this buffer compare test are typed out.

153 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

TEST NO. 10 - Multiple Sector Write/Read Test

Sub-Test 10.1

Description:

In this sub-test, subroutines DRW and RW are used to write the data patterns described in sub-test 9.1 onto the entire disk in 1 1/2 sector segments.

Errors:

154 - Indicates that the controller did not complete the write function in the maximum allowable time. Note that if the

value in the BAR is one greater than it should be, the error occurred during the writing of the second sector of the multiple sector operation.

155 - Indicates that the CER indicated an error occurred during the transfer of the data portion.

156 - Indicates that the BAR did not have the proper value after the termination of the opeation.

157 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during the buffer compare test are typed out.

160 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

Sub-Test 10.2

Description:

In this sub-test, the entire disk is read and the data patterns verified in segments of 1 1/2 sectors, just as they were written in sub-test 10.1. The subroutines DRW and RW are used for these operations.

Errors:

161 - Indicates that the controller did not complete the read function in the maximum allowable time. Note that if the value in the BAR is one greater than it should be, the error occurred during the reading of the second sector of the multiple sector operation.

162 - Indicates that the CER indicated an error occurred during the transfer of the data pattern.

163 - Indicates that the BAR did not have the proper value after the termination of the operation.

164 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during the buffer compare test are typed out.

165 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

Sub-Test 10.3

Description:

In this sub-test, the entire disk is read one sector at a time and the data patterns are verified.

Errors:

166 - Indicates that the contoller did not complete the read function in the maximum allowable time.

167 - Indicates that the CER indicated an error occurred during the transfer of the data pattern.

170 - Indicates that the BAR did not have the proper value after the termination of the operation.

171 - Indicates that there was an error in the data comparison during a data transfer operation. If the first Format Loop Control digit typed was a one, all errors detected during this buffer compare test are typed out.

172 - Indicates that the word in the buffer which is one greater than the word count during a data transfer operation, was modified during the operation.

```
LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
                    0001  * SYSTEM INDUSTRIES INC.                                    0000
                    0002  * MSI 800 SERIES DISK DIAGNOSTIC                           0001
                    0003  *                                                          0002
                    0004  * DIABLO DISK DIAGNOSTIC VERSION 2 MODIFIED 04/10/75      0003
                    0005  *                                                          0004
                    0006  *TO RELOCATE DIAGNOSTIC REDEFINE 'EXEC' AND 'DDAT'        0005
     1000           0007  EXEC   EQU   X'1000'                                       0006
     2000           0008  DDAT   EQU   X'2000'                                       0007
     2040           0009  BF1    EQU   DDAT+64                                      0008
     2340           0010  BF2    EQU   BF1+768                                      0009
0000                0011         ORG   X'0'                                         0010
0000 34             0012         NOP                                                0011
0001 08             0013         RO1                                                0012
0002 662000         0014         JMP/  DDAT                                         0013
                    0015  * PAGE ZERO - DATA TRANSFER LOCATIONS                      0014
0005 0000           0016  DATA1  DC    0          R-W CONTROL                        0015
0007 0000           0017         DC    0          WAIT TIME                          0016
0009 0000           0018         DC    0          ERROR VALUE                        0017
0008 0000           0019         DC    0          BAR CHK FLG                        0018
000D 0000           0020         DC    0          FAST EXIT FLG                      0019
000F 0000           0021  EOS1   DC    0                                             0020
                    0022  * PAGE ZERO - CONTROL SETTINGS                             0021
0011 0000           0023  WCCA   DC    0                                             0022
0013 2340           0024         DC    BF2                                           0023
0015 0000           0025  SECTOR DC    0                                             0024
0017 0000           0026         DC    0                                             0025
0019 0000           0027  BLOCKS DC    0                                             0026
                    0028  * PORT PARAMETERS                                          0027
001B 0000           0029  TDSK   DC    0          0=MOVING HEAD, -1=FIXED HEAD       0028
001D 0000           0030  MTSC   DC    0          MAX TEST SECTOR                    0029
001F 0000           0031  MRSC   DC    0          MAX REAL SECTOR                    0030
0021 0000           0032  SINSEC DC    0          BYTES/SECTOR                       0031
0023 0000           0033  MULSEC DC    0          1.5 * BYTES/SECTOR                 0032
0025 0000           0034  FULL   DC    0          0=FULL,-1=LESS THAN FULL           0033
0027 0000           0035  UNIT   DC    0          IN TWO MOST SIGNIFICANT BITS       0034
0029 0000           0036  DAISY  DC    0               IF BIT 15=1, TEST FIXED DISC  0035
                    0037  *               IF BIT 14=1, TEST REMOVABLE DISC           0036
                    0038  *                                                          0037
002B 0000           0039  MSEC   DC    0                                             0038
002D 0000           0040  ADDRES DC    0          CONTROLLER DEVICE CODE             0039
002F 0000           0041  DAVAL  DC    0               0=FIXED, 8000=REMOVABLE       0040
0031 0000           0042  EFG    DC    0                                             0041
0033 0000           0043  EF1    DC    0                                             0042
0035 0000           0044  ERNUM  DC    0                                             0043
0037 0000           0045  PORTS  DC    0                                             0044
0039 0000           0046  PASS1  DC    0                                             0045
003B 0000           0047  LPFORM DC    0          IF NOT 0, FORMAT FOR EACH TEST     0046
003D 0000           0048  FOY    DC    0          IF NOT 0, FORMAT ONLY              0047
003F 0000           0049  SFT    DC    0          IF NOT 0, RUN SPECIAL FORMAT TE    0048
0041 0000           0050  SW     DC    0                                             0049
                    0051  * PAGE ZERO - IO ROUTINE LOCATIONS                         0050
0043 1F32           0052  CLSTAT DC    ELST            CLEAR STATUS                 0051
0045 1EED           0053  SKPDON DC    ESKDN           SKIP ON NOT DONE IN 6MS      0052
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LOC  OBJECT     ER  STMT  LABEL   OP    OPERANDS                                    0053
0047 1EE5           0054  RDSTAT  DC    ERT             READ STATUS                 0053
0049 1F09           0055  RDBAR   DC    ERB             READ BAR                    0054
004B 1F2A           0056  LDCON   DC    ELCON           LOAD CONTROL                0055
004D 1F54           0057  LDRD    DC    ELR             LOAD BAR & READ             0056
004F 1F60           0058  LDWR    DC    ELW             LOAD BAR & WRITE            0057
0051 1F3D           0059  IOLS    DC    EOLS            SEEK                        0058
0053 1F49           0060  IWCCA   DC    EIWC            LOAD WORD CNT/CURRENT ADD   0059
0055 1F01           0061  RSSR    DC    ERS             READ SEEK STATUS            0060
0057 1F6C           0062  RESET   DC    EIO             MASTER RESET CONTROLLER     0061
0059 1F9E           0063  TI.     DC    TIN             TTY IN                      0062
005B 1FBD           0064  TO.     DC    TOT             TTY OUT                     0063
                    0065  *                                                         0064
0082                0066          ORG   X'82'                                      0065
0082 1DC9           0067          DC    ILTRP     I82                               0066
0084 1DC9           0068          DC    ILTRP                                       0067
0086 1DC9           0069          DC    ILTRP     I82                               0068
0088 1DC9           0070          DC    ILTRP                                       0069
008A 1DC9           0071          DC    ILTRP     I82                               0070
008C 0200           0072          DC    X'200'                                      0071
008E 1E46           0073          DC    PWF                                         0072
0090 1E4C           0074          DC    PWS                                         0073
0094                0075          ORG   X'94'                                      0074
                    0076  * PAGE ZERO - SUBROUTINE CALLS                            0075
0094 1D2B           0077  TERR    DC    EERR                                        0076
0096 1D99           0078  HLTLP   DC    EHP                                         0077
0093 1BE4           0079  TDAT    DC    EDAT                                        0078
009A 1C19           0080  TADD    DC    ETDD                                        0079
009C 1E63           0081  SADD    DC    ESCAD                                       0080
009E 1E53           0082  WRITE   DC    EXWR                                        0081
00A0 1E5B           0083  READ    DC    EXRD                                        0082
00A2 1E9A           0084  M12     DC    EM12                                        0083
00A4 1EB1           0085  CLR2    DC    EL21                                        0084
00A6 1B99           0086  TDIS    DC    EDIS            DISABLE                     0085
00A8 1BAE           0087  TENA    DC    EENA            ENABLE                      0086
00AA 1B7B           0088  TTEX    DC    ETEX                                        0087
00AC 1C95           0089  TSI     DC    SRI             SSR ----                    0088
00AE 1CA0           0090  TSRB    DC    SRB             SSR SB ----IS----           0089
00B0 1C52           0091  TCI     DC    ECI             CER----                     0090
00B2 1B37           0092  CRLF    DC    ECF                                         0091
00B4 1B90           0093  TQQ     DC    EQQ                                         0092
00B6 1D0E           0094  TYPWD   DC    EWD             TYPE 4 HEX                  0093
00B8 1C5D           0095  TSB     DC    ETSB            SB                          0094
00BA 1C68           0096  TIS     DC    ETIS            IS                          0095
00BC 1C74           0097  TTAB    DC    ETB             BAR SB----IS----            0096
00BE 1C27           0098  TCNB    DC    ECB             CER SB----IS----            0097
00C0 1E78           0099  M.      DC    MOV                                         0098
00C2 1DC9           0100  IT.     DC    ILTRP                                       0099
00C4 1CCD           0101  HI.     DC    HXI                                         0100
00C6 1CEE           0102  HO.     DC    HXO                                         0101
00C8 1ECA           0103  ES.     DC    ESP                                         0102
00CA 1D62           0104  TPD     DC    ETP                                         0103
                    0105  * MAJOR TESTS                                           0104
00CC 1000           0106  EX.     DC    EXEC                                        0105
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS                                  0106
00CE 1995           0107  PA.    DC    PARAM                                     0106
00D0 1094           0108  CT.    DC    CTST                                      0107
00D2 1155           0109  IN.    DC    ITST                                      0108
00D4 119B           0110  WC.    DC    WTST                                      0109
00D6 11E6           0111  LA.    DC    LAITST                                    0110
00D8 141B           0112  FR.    DC    FTST                                      0111
00DA 165B           0113  WR.    DC    W11                                       0112
00DC 1700           0114  SA.    DC    SABTST                                    0113
00DE 1757           0115  RN.    DC    RANTST                                    0114
00E0 1792           0116  BD.    DC    BDATST                                    0115
00E2 17D3           0117  MD.    DC    MDST                                      0116
00E4 151E           0118  F.     DC    F15                                       0117
00E6 159B           0119  RW.    DC    RW                                        0118
00E8 12EE           0120  L5.    DC    L5                                        0119
00EA 0000           0121  SCV    DC    0                                         0120
00EC 2401           0122        LRA   1                                         0121
00EE 62EA           0123        JMP*  SCV                                       0122
00F0 0006           0124  L41    DS    6                                         0123
1000                0125        ORG   EXEC                                      0124
                    0126  * EXECUTIVE ROUTINE FOR MSI 800 COMPUTERS             0125
1000 6ACE           0127        RTJ*  PA.          GET PORT PARAMETERS           0126
1002 6AD0           0128        RTJ*  CT.       CONTROL & ERROR REG TEST         0127
1004 6AD2           0129        RTJ*  IN.       INTERRUPT TEST                   0128
1006 6AD4           0130        RTJ*  WC.       WORD COUNT & CURRENT ADDR TES    0129
1008 E72000         0131        LDA=  DDAT                                      0130
100B F106           0132        STA   E21                                       0131
100D E037           0133        LDA   PORTS                                     0132
100F F16E           0134        STA   EX3+1                                     0133
1011 6AC0           0135        RTJ*  M.         GET PORT PARAMETER             0134
1013 0000           0136  E21    DC    0                                         0135
1015 0018           0137        DC    TDSK                                      0136
1017 0010           0138        DC    MSEC-TDSK                                 0137
1019 873434         0139        LDX=  X'3434'                                   0138
101C E018           0140        LDA   TDSK                                      0139
101E 1911           0141        NAZ   EX1                                       0140
1020 E021           0142        LDA   SINSEC                                    0141
1022 2807           0143        ALA   7                                         0142
1024 1103           0144        JAZ   *+5                                       0143
1026 872401         0145        LDX=  X'2401'                                   0144
1029 E02F           0146        LDA   DAVAL                                     0145
102B 1904           0147        NAZ   EX1                                       0146
102D E029           0148        LDA   DAISY                                     0147
102F 1C32           0149        NAN   NEXT                                      0148
1031 88EC           0150  EX1    STX   SCV+2                                     0149
1033 6ACA           0151        RTJ*  TPD                                       0150
1035 6A82           0152        RTJ*  CRLF                                      0151
1037 E01F           0153        LDA   MRSC                                      0152
1039 F028           0154        STA   MSEC                                      0153
103B 6AD6           0155        RTJ*  LA.        OVERLAP SEEK - LAI TEST        0154
103D E01D           0156        LDA   MTSC                                      0155
103F F028           0157        STA   MSEC                                      0156
1041 E018           0158        LDA   TDSK                                      0157
1043 1938           0159        NAZ   *+10                                      0158
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OBJECT     ER  STMT  LABEL  OP     OPERANDS                                  0159
E039           0160         LDA    PASS1                                     0160
A03B           0161         ADA    LPFORM                                    0161
1102           0162         JAZ    *+4                                       0162
6AD8           0163         RTJ*   FR.          FORMAT                       0163
               0164  *ONE WORD WRITE/READ TEST                               0164
6ADA           0165         RTJ*   WR.                                       0165
0040           0166         DC     X'0040'                                   0166
0000           0167         DC     0                                         0167
0001           0168         DC     1                                         0168
E039           0169         LDA    PASS1                                     0169
A03B           0170         ADA    LPFORM                                    0170
1102           0171         JAZ    *+4                                       0171
6ADC           0172         RTJ*   SA.                                       0172
6ADE           0173         RTJ*   RN.                                       0173
6AE0           0174         RTJ*   BD.                                       0174
6AE2           0175         RTJ*   MD.                                       0175
E02F           0176  NEXT   LDA    DAVAL                                     0176
190A           0177         NAZ    EX5                                       0177
E029           0178         LDA    DAISY                                     0178
2801           0179         ALA    1                                         0179
1104           0180         JAZ    EX5                                       0180
F02F           0181         STA    DAVAL                                     0181
61A0           0182         JMP    E21-2                                     0182
08             0183  EX5    RO1                                              0183
EF00           0184         LDV=   H'0'                                      0184
F02F           0185         STA    DAVAL                                     0185
E198           0186         LDA    E21                                       0186
A19D           0187         ADA    E21+4                                     0187
F197           0188         STA    E21                                       0188
7901           0189         DWM    EX3+1                                     0189
E70000         0190  EX3    LDA=   0                                         0190
198E           0191         NAZ    E21-2                                     0191
E039           0192         LDA    PASS1                                     0192
110A           0193         JAZ    EX4                                       0193
EF00           0194         LDV=   H'0'                                      0194
F039           0195         STA    PASS1                                     0195
E03B           0196         LDA    LPFORM                                    0196
1902           0197         NAZ    *+4                                       0197
6AA6           0198         RTJ*   TDIS                                      0198
661002         0199  EX4    JMP/   EXEC+2                                    0199
               0200  * CONTROL AND ERROR REGISTER TEST                        0200
               0201  *                                                        0201
0000           0202  CTST   DC     **                                        0202
08             0203         RO1                                              0203
EF02           0204         LDV=   H'2'                                      0204
693E           0205  C2     RTJ    RGTRT                                     0205
6A46           0206         RTJ*   LDCON                                     0206
6A47           0207         RTJ*   RDSTAT                                    0207
007F           0208         DC     X'007F'                                   0208
6ABE           0209         RTJ*   TCNB                                      0209
0001           0210         DC     1                                         0210
61F2           0211         JMP    C2                                        0211
6E111F         0212  C3     RTJ/   RGRES                                     0212
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LOC  OBJECT     ER  STMT  LABEL  OP     OPERANDS
10AA 6A47           0213         RTJ*   RDSTAT                    0212
10AC FE03           0214         DC     X'FE03'                   0213
10AE 6ABE           0215         RTJ*   TCNB                      0214
10B0 0002           0216         DC     2                         0215
10B2 61F3           0217         JMP    C3                        0216
10B4 1404           0218         JAN    *+6                       0217
10B6 2001           0219         LLA    1                         0218
10B8 61DF           0220         JMP    C2                        0219
10BA E70101         0221         LDA=   X'101'                    0220
10BD 691A           0222  C1     RTJ    RGTRT                     0221
10BF 6A4B           0223         RTJ*   LDCON                     0222
10C1 6A47           0224         RTJ*   RDSTAT                    0223
10C3 017F           0225         DC     X'017F'                   0224
10C5 6ABE           0226         RTJ*   TCNB                      0225
10C7 0001           0227         DC     1                         0226
10C9 61F2           0228         JMP    C1                        0227
10CB 6BDB           0229  C4     RTJ*   C3+1                      0228
10CD 6A47           0230         RTJ*   RDSTAT                    0229
10CF 017F           0231         DC     X'017F'                   0230
10D1 6ABE           0232         RTJ*   TCNB                      0231
10D3 0002           0233         DC     2                         0232
10D5 61F4           0234         JMP    C4                        0233
10D7 63BB           0235         JMP*   CTST                      0234
                    0236  *REGISTER TRANSFER TEST                 0235
                    0237  *CALL  LDA=VALUE                        0236
                    0238  *      RTJ    RGTRT                     0237
                    0239  *      RTJ*   LDSBR                     0238
                    0240  *      RTJ*   RDSBR                     0239
                    0241  *      DC     MASK                      0240
                    0242  *      RTJ*   TYPOUT                    0241
                    0243  *      DC     ERRNO                     0242
                    0244  *                                       0243
10D9 0000           0245  RGTRT  DC     **                        0244
10DB F12F           0246         STA    RT1                       0245
10DD 81FA           0247         LDX    RGTRT                     0246
10DF 6931           0248         RTJ    RT2                       0247
10E1 692F           0249         RTJ    RT2                       0248
10E3 D4             0250         ANA-                             0249
10E4 F128           0251         STA    RT1+2                     0250
10E6 E124           0252         LDA    RT1                       0251
10E8 D4             0253         ANA-                             0252
10E9 44             0254         INX                              0253
10EA 44             0255         INX                              0254
10EB 89EC           0256         STX    RGTRT                     0255
10ED F121           0257         STA    RT1+4                     0256
10EF B11D           0258         SBA    RT1+2                     0257
10F1 110D           0259         JAZ    RT3                       0258
10F3 E4             0260         LDA-                             0259
10F4 F106           0261         STA    RT4                       0260
10F6 E502           0262         LDA+   2                         0261
10F8 6A94           0263         RTJ*   TERR                      0262
10FA E114           0264         LDA    RT1+4                     0263
10FC 0000           0265  RT4    DC     0                         0264
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS                                  0265
10FE 81D9           0266         LDX   RGTRT                                     0265
1100 0B             0267  RT3    RO4                                             0266
1101 46             0268         AWX                                             0267
1102 08             0269         RO1                                             0268
1103 6A96           0270         RTJ*  HLTLP                                    0269
1105 6102           0271         JMP   *+4                                       0270
1107 44             0272         INX                                             0271
1108 44             0273         INX                                             0272
1109 E101           0274         LDA   RT1                                       0273
110B 64             0275         JMP-                                            0274
110C 0006           0276  RT1    DS    6                                         0275
110E 0000           0277  RT2    DC    **                                        0276
1110 E4             0278         LDA-                                            0277
1111 F104           0279         STA   RT5                                       0278
1113 44             0280         INX                                             0279
1114 44             0281         INX                                             0280
1115 E1F1           0282         LDA   RT1                                       0281
1117 0000           0283  RT5    DC    0                                         0282
1119 63F3           0284         JMP*  RT2                                       0283
                    0285  * REGISTER RESET TEST - SAVES AC                       0284
                    0286  * CALL RTJ   RGRES                                    0285
                    0287  *      RTJ*  RDSCR                                    0286
                    0288  *      DC    MASK                                     0287
                    0289  *      RTJ*  TYPOUT                                   0288
                    0290  *      DC    ERRNO                                    0289
111F 0000           0291  RGRES  DC    **                                       0290
1121 F12F           0292         STA   RR1+1                                     0291
1123 81FA           0293         LDX   RGRES                                     0292
1125 E4             0294         LDA-                                            0293
1126 44             0295         INX                                             0294
1127 44             0296         INX                                             0295
1128 89F5           0297         STX   RGRES                                     0296
112A F105           0298         STA   RR2                                       0297
112C 04             0299         DIN                                             0298
112D 6A57           0300         RTJ*  RESET                                     0299
112F 39E0           0301         OBA   7,0                                       0300
1131 0000           0302  RR2    DC    0                                         0301
1133 05             0303         EIN                                             0302
1134 81E9           0304         LDX   RGRES                                     0303
1136 D4             0305         ANA-                                            0304
1137 44             0306         INX                                             0305
1138 44             0307         INX                                             0306
1139 89E4           0308         STX   RGRES                                     0307
113B 1109           0309         JAZ   RR3                                       0308
113D E4             0310         LDA-                                            0309
113E F104           0311         STA   *+6                                       0310
1140 E502           0312         LDA+  2                                         0311
1142 6A94           0313         RTJ*  TERR                                      0312
1144 0000           0314         DC    0                                         0313
1146 81D7           0315  RR3    LDX   RGRES                                     0314
1148 0B             0316         RO4                                             0315
1149 46             0317         AWX                                             0316
114A 08             0318         RO1                                             0317
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS                                  0318
1148 6A96           0319         RTJ*  HLTLP                                     0318
114D 6102           0320         JMP   *+4                                       0319
114F 44             0321         INX                                             0320
1150 44             0322         INX                                             0321
1151 E70000         0323  RR1    LDA=  0                                         0322
1154 64             0324         JMP-                                            0323
                    0325  *                                                       0324
                    0326  *INTERRUPT TEST                                         0325
                    0327  *                                                       0326
1155 0000           0328  ITST   DC    **                                        0327
1157 08             0329         RG1                                             0328
1158 E02D           0330         LDA   ADDRESS                                   0329
115A 2801           0331         ALA   1                                         0330
115C A70100         0332         ADA=  X'100'                                    0331
115F 4C             0333         TAX                                             0332
1160 8926           0334         STX   IT2-2                                     0333
1162 E4             0335  IT0    LDA-                                            0334
1163 F126           0336         STA   IT2+1                                     0335
1165 E71184         0337         LDA=  IT1                                       0336
1168 F4             0338         STA-                                            0337
1169 6A57           0339         RTJ*  RESET                                     0338
116B 39E0           0340         GBA   7,0                                       0339
116D 05             0341         EIN                                             0340
116E EF40           0342         LDV=  X'40'                                     0341
1170 6A4B           0343         RTJ*  LDCON                                     0342
1172 EF41           0344         LDV=  X'41'                                     0343
1174 6A4B           0345         RTJ*  LDCON                                     0344
1176 874E20         0346         LDX=  F'20000'                                  0345
1179 45             0347         DCX                                             0346
117A 18FD           0348         NXZ   *-1                                       0347
117C EF03           0349         LDV=  H'3'                                      0348
117E 6A94           0350         RTJ*  TERR                                      0349
1180 6AB0           0351         RTJ*  TCI                                       0350
1182 6103           0352         JMP   IT2-3                                     0351
1184 04             0353  IT1    DIN                                             0352
1185 04             0354         DIN             FOR 820                         0353
1186 04             0355         DIN                                             0354
1187 670000         0356         LDX=  0                                         0355
118A E70000         0357  IT2    LDA=  0                                         0356
118D F4             0358         STA-                                            0357
118E EF00           0359         LDV=  H'0'                                      0358
1190 F88D           0360         STV   X'8D'     RESET STACK POINTER             0359
1192 6A4B           0361         RTJ*  LDCON                                     0360
1194 05             0362         EIN                                             0361
1195 6A96           0363         RTJ*  HLTLP                                     0362
1197 61C9           0364         JMP   IT0                                       0363
1199 63BA           0365         JMP*  ITST                                      0364
                    0366  *                                                       0365
                    0367  *WORD COUNT & CURRENT ADDRESS TEST                      0366
                    0368  *                                                       0367
119B 0000           0369  WTST   DC    **                                        0368
119D E711CC         0370         LDA=  WT3                                       0369
11A0 F011           0371         STA   WCCA                                      0370
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LOC  OBJECT     ER  STMT  LABEL   OP     OPERANDS                                  0371
11A2 08             0372          RO1                                              0372
11A3 EF00           0373          LDV=   H'0'                                      0373
11A5 6910           0374          RTJ    WT2                                       0374
11A7 EFFD           0375          LDV=   H'-3'                                     0375
11A9 690C           0376          RTJ    WT2                                       0376
11AB E7AAAA         0377          LDA=   X'AAAA'                                   0377
11AE 6907           0378          RTJ    WT2                                       0378
11B0 E75554         0379          LDA=   X'5554'                                   0379
11B3 6902           0380          RTJ    WT2                                       0380
11B5 63E4           0381          JMP*   WTST                                      0381
11B7 0000           0382  WT2     DC     **                                        0382
11B9 6E10D9         0383          RTJ/   RGTRT                                     0383
11BC 6A11           0384          RTJ*   WCCA                                      0384
11BE 6A49           0385          RTJ*   RDBAR                                     0385
11C0 7FFF           0386          DC     X'7FFF'                                   0386
11C2 6ABC           0387          RTJ*   TTAB                                      0387
11C4 0004           0388          DC     4                                         0388
11C6 61F1           0389          JMP    WT2+2                                     0389
11C8 63ED           0390          JMP*   WT2                                       0390
11CA 3960           0391          OBA    3,0                                       0391
11CC 0000           0392  WT3     DC     **                                        0392
11CE F10C           0393          STA    *+14                                      0393
11D0 E1F8           0394          LDA    WT3-2                                     0394
11D2 A02D           0395          ADA    ADDRESS                                   0395
11D4 F10C           0396          STA    *+14                                      0396
11D6 D7FF1F         0397          ANA=   X'FF1F'                                   0397
11D9 F103           0398          STA    *+5                                       0398
11DB E70000         0399          LDA=   0                                         0399
11DE 0000           0400          DC     0                                         0400
11E0 2C08           0401          ARA    8                                         0401
11E2 0000           0402          DC     0                                         0402
11E4 63E6           0403          JMP*   WT3                                       0403
                    0404  *LOGICAL ADDRESS INTERLOCK & OVERLAP SEEK TEST           0404
                    0405  *                                                        0405
11E6 0000           0406  LAITST  DC     **                                        0406
11E8 08             0407          RO1                                              0407
11E9 EFF8           0408          LDV=   H'-8'                                     0408
11EB 4C             0409          TAX                                              0409
11EC 4F             0410          TXB                                              0410
11ED E027           0411          LDA    UNIT                                      0411
11EF 2002           0412          LLA    2                                         0412
11F1 4C             0413          TAX                                              0413
11F2 EF01           0414          LDV=   H'1'                                      0414
11F4 1307           0415          JXZ    *+9                                       0415
11F6 2804           0416          ALA    4                                         0416
11F8 2104           0417          LLB    4                                         0417
11FA 45             0418          DCX                                              0418
11FB 18F9           0419          NXZ    *-5                                       0419
11FD 08             0420          RO4                                              0420
11FE F8F0           0421          STV    L41                                       0421
1200 08             0422          RO1                                              0422
1201 6A55           0423  L22     RTJ*   RSSR                                      0423
1203 D0F0           0424          ANA    L41                                       0424
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS                          0424
1205 1106           0425         JAZ   L3                                0425
1207 EF05           0426         LDV=  H'5'                              0426
1209 6A94           0427         RTJ*  TERR                              0427
120B 6AAC           0428         RTJ*  TSI                               0428
120D 6A96           0429  L3     RTJ*  HLTLP                             0429
120F 61F0           0430         JMP   L22                               0430
1211 EF00           0431         LDV=  H'0'                              0431
1213 F015           0432         STA   SECTOR                            0432
1215 6A57           0433         RTJ*  RESET                             0433
1217 39E0           0434         OBA   7,0                               0434
1219 6A55           0435         RTJ*  RSSR                              0435
121B D0F2           0436         ANA   L41+2                             0436
121D F0F4           0437         STA   L41+4                             0437
121F EF00           0438  L31    LDV=  H'0'                              0438
1221 6A51           0439         RTJ*  IOLS                              0439
1223 E0F0           0440         LDA   L41                               0440
1225 2001           0441         LLA   1                                 0441
1227 F109           0442         STA   L2+1                              0442
1229 2001           0443         LLA   1                                 0443
122B A105           0444         ADA   L2+1                              0444
122D F103           0445         STA   L2+1                              0445
122F 6A55           0446         RTJ*  RSSR                              0446
1231 D70000         0447  L2     ANA=  0                                 0447
1234 1106           0448         JAZ   L32                               0448
1236 EF06           0449         LDV=  H'6'                              0449
1238 6A94           0450         RTJ*  TERR                              0450
123A 6AAC           0451         RTJ*  TSI                               0451
123C E7FC8D         0452  L32    LDA=  F'-883'                           0452
123F F1F1           0453         STA   L2+1       TIME OUT 300 MSEC      0453
1241 6E12C5         0454         RTJ/  L7                                0454
1244 1108           0455         JAZ   L34                               0455
1246 E1EA           0456         LDA   L2+1                              0456
1248 48             0457         INA                                     0457
1249 19F4           0458         NAZ   L32+3                             0458
124B EF86           0459         LDV=  X'66'                             0459
124D 6A94           0460         RTJ*  TERR                              0460
124F 6AAC           0461         RTJ*  TSI                               0461
1251 6A96           0462  L34    RTJ*  HLTLP                             0462
1253 61CA           0463         JMP   L31                               0463
1255 E02B           0464         LDA   MSEC                              0464
1257 6B39           0465         RTJ*  L4A                               0465
1259 0000           0466         DC    0                                 0466
125B 0004           0467         DC    4                                 0467
125D 0001           0468         DC    1                                 0468
125F 0007           0469         DC    7                                 0469
1261 61F2           0470         JMP   L34+4                             0470
1263 EF00           0471         LDV=  H'0'                              0471
1265 6B2B           0472         RTJ*  L4A                               0472
1267 0000           0473         DC    0                                 0473
1269 0000           0474         DC    0                                 0474
126B 0001           0475         DC    1                                 0475
126D 000D           0476         DC    X'000D'                           0476
126F 61F2           0477         JMP   *-12                              0477
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LOC  OBJECT     ER  STMT  LABEL  OP     OPERANDS
1271 EFFF           0478          LDV=   H'-1'                              0477
1273 A02B           0479          ADA    MSEC                               0478
1275 6B16           0480          RTJ*   L4A                                0479
1277 0000           0481          DC     0                                  0480
1279 0000           0482          DC     0                                  0481
127B 0001           0483          DC     1                                  0482
127D 0013           0484          DC     X'0013'                            0483
127F 61F0           0485          JMP    *-14                               0484
1281 EF01           0486          LDV=   H'1'                               0485
1283 F011           0487          STA    WCCA                               0486
1285 6A53           0488          RTJ*   IWCCA                              0487
1287 E027           0489          LDA    UNIT                               0488
1289 2005           0490          LLA    5                                  0489
128B 6A4B           0491          RTJ*   LDCON                              0490
128D EFFF           0492          LDV=   H'-1'                              0491
128F A02B           0493          ADA    MSEC                               0492
1291 6E134D         0494          RTJ/   L4                                 0493
     1292           0495  L4A     EQU    *-2                                0494
1294 0002           0496          DC     2                                  0495
1296 0000           0497          DC     0                                  0496
1298 0000           0498          DC     0                                  0497
129A 0019           0499          DC     X'0019'                            0498
129C 61EF           0500          JMP    *-15                               0499
129E E027           0501          LDA    UNIT                               0500
12A0 2002           0502          LLA    2                                  0501
12A2 4A             0503          GCA                                       0502
12A3 48             0504          INA                                       0503
12A4 AF03           0505          ADV=   H'3'                               0504
12A6 2003           0506          LLA    3                                  0505
12A8 6A4B           0507          RTJ*   LDCON                              0506
12AA EFFF           0508          LDV=   H'-1'                              0507
12AC A02B           0509          ADA    MSEC                               0508
12AE 6BE2           0510          RTJ*   L4A                                0509
12B0 0000           0511          DC     0                                  0510
12B2 0000           0512          DC     0                                  0511
12B4 0000           0513          DC     0                                  0512
12B6 001F           0514          DC     X'001F'                            0513
12B8 61F0           0515          JMP    *-14                               0514
12BA E027           0516          LDA    UNIT                               0515
12BC 2005           0517          LLA    5                                  0516
12BE 6A4B           0518          RTJ*   LDCON                              0517
12C0 6910           0519          RTJ    L6                                 0518
12C2 6711E6         0520          JMP=   LAITST                             0519
                    0521  *WAIT 300 USEC & READ SSR                         0520
                    0522  *292 USEC                                         0521
12C5 0000           0523  L7      DC     **                                 0522
12C7 EFFB           0524          LDV=   H'-5'                              0523
12C9 48             0525          INA                                       0524
12CA 19FD           0526          NAZ    *-1                                0525
12CC 6A55           0527          RTJ*   RSSR                               0526
12CE D0F0           0528          ANA    L41                                0527
12D0 63F3           0529          JMP*   L7                                 0528
12D2 0000           0530  L6      DC     **                                 0529
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                          0530
12D4 E02B            0531         LDA    MSEC                              0530
12D6 F015            0532         STA    SECTOR                            0531
12D8 6914            0533         RTJ    L5                                0532
12DA 6A4D            0534         RTJ*   LDRD                              0533
12DC 05DC            0535         DC     F'1500'                           0534
12DE 0025            0536         DC     X'0025'                           0535
12E0 61F6            0537         JMP    *-8                               0536
12E2 690A            0538         RTJ    L5                                0537
12E4 6A4F            0539         RTJ*   LDWR                              0538
12E6 05DC            0540         DC     F'1500'                           0539
12E8 0028            0541         DC     X'0028'                           0540
12EA 61F6            0542         JMP    *-8                               0541
12EC 63E4            0543         JMP*   L6                                0542
                     0544  *CHECK FOR LAI ERROR GENERATION                  0543
                     0545  *CALL  RTJ    L5                                0544
                     0546  *      RTJ*   SEEK  READ/WRITE                   0545
                     0547  *      DC     WAIT IN 200 USEC UNITS            0546
                     0548  *      DC     ERROR NO.                         0547
12EE 0000            0549  L5     DC     **                                0548
12F0 09              0550         R02                                      0549
12F1 81FB            0551         LDX    L5                                0550
12F3 E4              0552         LDA-                                     0551
12F4 F10C            0553         STA    L50                               0552
12F6 46              0554         AWX                                      0553
12F7 E4              0555         LDA-                                     0554
12F8 F111            0556         STA    L51+1                             0555
12FA 46              0557         AWX                                      0556
12FB 89F1            0558         STX    L5                                0557
12FD 08              0559         R01                                      0558
12FE 6A57            0560         RTJ*   RESET                            0559
1300 39E0            0561         OBA    7,0                               0560
1302 0000            0562  L50    DC     **                                0561
1304 6A45            0563         RTJ*   SKPDON                           0562
1306 611F            0564         JMP    L52                               0563
1308 7901            0565         DWM    L51+1                             0564
130A E70000          0566  L51    LDA=   0                                 0565
130D 19F5            0567         NAZ    L50+2                             0566
130F EF02            0568         LDV=   H'2'                              0567
1311 A3DB            0569  L53    ADA*   L5                                0568
1313 71D9            0570         IWM    L5                                0569
1315 71D7            0571         IWM    L5                                0570
1317 6A94            0572         RTJ*   TERR                              0571
1319 6AB0            0573         RTJ*   TCI                               0572
131B 6AAC            0574         RTJ*   TSI                               0573
131D 6A96            0575  L54    RTJ*   HLTLP                             0574
131F 63CD            0576         JMP*   L5                                0575
1321 71C8            0577         IWM    L5                                0576
1323 71C9            0578         IWM    L5                                0577
1325 63C7            0579         JMP*   L5                                0578
1327 6A47            0580  L52    RTJ*   RDSTAT                            0579
1329 D7FF63          0581         ANA=   X'FF63'                           0580
132C 878901          0582         LDX=   X'3901'                           0581
132F 4F              0583         TXB                                      0582
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1330 43              0584          XRB                                0583
1331 EF01            0585          LDV=  H'1'                         0584
1333 1ADC            0586          MBZ   L53                          0585
1335 E027            0587          LDA   UNIT                         0586
1337 2002            0588          LLA   2                            0587
1339 4C              0589          TAX                                0588
133A 6A55            0590          RTJ*  RSSP                         0589
133C 1305            0591          JXZ   *+7                          0590
133E 2404            0592          LRA   4                            0591
1340 45              0593          DCX                                0592
1341 18FB            0594          NXZ   *-3                          0593
1343 DF04            0595          ANV=  X'4'                         0594
1345 11CA            0596          JAZ   L53                          0595
1347 71A5            0597          IWM   L5                           0596
1349 71A3            0598          IWM   L5                           0597
134B 61D0            0599          JMP   L54                          0598
                     0600 *LAI & OVERLAP SEEK TEST                    0599
                     0601 *CALL    LDA=SECTOR                         0600
                     0602 *        RTJ   L4                           0601
                     0603 *        DC    BUSY VALUE                   0602
                     0604 *        DC    HDW VALUE                    0603
                     0605 *        DC    DONE VALUE                   0604
                     0606 *        DC    ERROR                        0605
1340 0000            0607 L4       DC    **                           0606
134F 08              0608          RD1                                0607
1350 F167            0609          STA   L42+6  SECTOR                0608
1352 6A43            0610          RTJ*  CLSTAT                       0609
1354 E150            0611          LDA   L42                          0610
1356 A020            0612          ADA   ADDRES                       0611
1358 F119            0613          STA   L43+4                        0612
135A F12E            0614          STA   L45+4                        0613
135C A70040          0615          ADA=  X'0040'                      0614
135F F10E            0616          STA   L43                          0615
1361 F123            0617          STA   L45                          0616
1363 E150            0618          LDA   L42+2                        0617
1365 F150            0619          STA   L42+4                        0618
1367 EF00            0620          LDV=  H'0'                         0619
1369 F152            0621          STA   L42+10                       0620
136B E14C            0622          LDA   L42+6                        0621
136D 6A51            0623          RTJ*  TOLS                         0622
136F 0000            0624 L43      DC    0                            0623
1371 2808            0625          ALA   8                            0624
1373 0000            0626          DC    0                            0625
1375 D0F0            0627          ANA   L41                          0626
1377 1902            0628          NAZ   *+4                          0627
1379 7142            0629          IWM   L42+10                       0628
137B 713A            0630          IWM   L42+4                        0629
137D E138            0631          LDA   L42+4                        0630
137F 19EE            0632          NAZ   L43                          0631
1381 E7FC18          0633          LDA=  F'-1000'                     0632
1384 F131            0634          STA   L42+4                        0633
1386 0000            0635 L45      DC    0                            0634
1388 2808            0636          ALA   8                            0635
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
138A 0000          0637         DC    0                                  0636
138C F12B          0638         STA   L42+6                             0637
138E D0F0          0639         ANA   L41                                0638
1390 114F          0640         JAZ   L47                                0639
1392 E125          0641         LDA   L42+6                              0640
1394 D0F2          0642         ANA   L41+2                              0641
1396 B0F4          0643         SBA   L41+4                              0642
1398 1125          0644         JAZ   L44-5                              0643
139A 8181          0645         LDX   L4                                 0644
139C 0A            0646         ROB                                      0645
139D 46            0647         AWX                                      0646
139E 46            0648         AWX                                      0647
139F 08            0649         ROI                                      0648
13A0 89AB          0650         STX   L4                                 0649
13A2 EF02          0651         LDV=  H'2'                               0650
13A4 A4            0652         ADA-                                     0651
13A5 6A94          0653         RTJ*  TERR                               0652
13A7 E0F4          0654         LDA   L41+4                              0653
13A9 6AAE          0655         RTJ*  TSRB                               0654
13AB 81A0          0656  L46    LDX   L4                                 0655
13AD 6A96          0657         RTJ*  HLTLP                              0656
13AF 6502          0658         JMP+  2                                  0657
13B1 6504          0659         JMP+  4                                  0658
13B3 3100          0660  L42    IBA   0,0                                0659
13B5 FFFB          0661         DC    F'-5'                              0660
13B7 0008          0662         DS    8                                  0661
13BF EFF7          0663         LDV=  H'-9'                              0662
13C1 48            0664         INA                                      0663
13C2 19FD          0665         NAZ   *-1                                0664
13C4 71F1          0666  L44    IWM   L42+4                              0665
13C6 E1EF          0667         LDA   L42+4                              0666
13C8 19BC          0668         NAZ   L45                                0667
13CA 8181          0669         LDX   L4                                 0668
13CC 44            0670  L48    INX                                      0669
13CD 44            0671         INX                                      0670
13CE 44            0672         INX                                      0671
13CF 44            0673         INX                                      0672
13D0 44            0674         INX                                      0673
13D1 44            0675         INX                                      0674
13D2 8B1A          0676         STX*  L48                                0675
13D4 A4            0677         ADA-                                     0676
13D5 6A94          0678         RTJ*  TERR                               0677
13D7 E1DE          0679         LDA   L42+4                              0678
13D9 1102          0680         JAZ   *+4                                0679
13DB 6AB0          0681         RTJ*  TCI                                0680
13DD 6AAC          0682         RTJ*  TSI                                0681
13DF 61CA          0683         JMP   L46                                0682
13E1 E027          0684  L47    LDA   UNIT                               0683
13E3 2004          0685         LLA   4                                  0684
13E5 F903          0686         STV   *+5                                0685
13E7 E1D0          0687         LDA   L42+6                              0686
13E9 2C00          0688         ARA   0                                  0687
13EB F1CC          0689         STA   L42+6                              0688
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                                  0689
13ED 86134D          0690        LDX/   L4                                        0690
     13EE            0691  L48   EQU    *-2                                       0691
13F0 EF02            0692        LDV=   H'2'                                      0692
13F2 D1C5            0693        ANA    L42+6                                     0693
13F4 B4              0694        SBA-                                             0694
13F5 1104            0695        JAZ    *+6                                       0695
13F7 EF03            0696        LDV=   H'3'                                      0696
13F9 61D1            0697        JMP    L48                                       0697
13FB 44              0698        INX                                              0698
13FC 44              0699        INX                                              0699
13FD EF04            0700        LDV=   H'4'                                      0700
13FF D1B8            0701        ANA    L42+6                                     0701
1401 B4              0702        SBA-                                             0702
1402 1108            0703        JAZ    *+10                                      0703
1404 E018            0704        LDA    TDSK                                      0704
1406 1904            0705        NAZ    *+6                                       0705
1408 EF04            0706        LDV=   H'4'                                      0706
140A 61C2            0707        JMP    L48+2                                     0707
140C 44              0708        INX                                              0708
140D 44              0709        INX                                              0709
140E 6A47            0710        RTJ*   RDSTAT                                    0710
1410 DF01            0711        ANV=   H'1'                                      0711
1412 B4              0712        SBA-                                             0712
1413 44              0713        INX                                              0713
1414 44              0714        INX                                              0714
1415 1196            0715        JAZ    L46+2                                     0715
1417 EF05            0716        LDV=   H'5'                                      0716
1419 61B7            0717        JMP    L48+6                                     0717
                     0718  *FORMAT TEST (FOR MOVING HEAD DISKS ONLY)               0718
                     0719  *                                                       0719
141B 0000            0720  FTST  DC     **                                        0720
141D 6AE4            0721        RTJ*   F.                                        0721
141F 0000            0722        DC     0                                         0722
1421 0000            0723        DC     0                                         0723
1423 002B            0724        DC     X'002B'                                   0724
1425 6ADA            0725        RTJ*   WR.                                       0725
1427 003D            0726        DC     X'003D'                                   0726
1429 0000            0727        DC     0                                         0727
142B 0001            0728        DC     1                                         0728
142D E03D            0729        LDA    FDY                                       0729
142F 1103            0730        JAZ    *+5                                       0730
1431 6614AA          0731        JMP/   F3                                        0731
1434 E02B            0732        LDA    MSEC                                      0732
1436 F102            0733        STA    *+4                                       0733
1438 6AE4            0734        RTJ*   F.                                        0734
143A 0000            0735        DC     0                                         0735
143C 0000            0736        DC     0                                         0736
143E 007B            0737        DC     X'007B'                                   0737
1440 6B0F            0738        RTJ*   F5A                                       0738
1442 0000            0739        DC     0                                         0739
1444 6A4D            0740        RTJ*   LDRD                                      0740
1446 0800            0741        DC     F'2048'  WAIT                             0741
1448 9105            0742        DC     X'9105'                                   0742
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS
144A FF67            0743         DC    X'FF67'                          0742
144C 007E            0744         DC    X'007E'                          0743
144E 61F0            0745         JMP   *-14                             0744
1450 6E14CC          0746         RTJ/  F5                               0745
     1451            0747  F5A    EQU   *-2                              0746
1453 0000            0748         DC    0                                0747
1455 6A4F            0749         RTJ*  LDWR                             0748
1457 0800            0750         DC    F'2048'                          0749
1459 9101            0751         DC    X'9101'                          0750
145B FF67            0752         DC    X'FF67'                          0751
145D 0080            0753         DC    X'0080'                          0752
145F 61EF            0754         JMP   *-15                             0753
1461 6AE4            0755         RTJ*  F.                               0754
1463 0000            0756         DC    0                                0755
1465 8000            0757         DC    X'8000'                          0756
1467 002E            0758         DC    X'002E'                          0757
1469 EFFF            0759         LDV=  H'-1'                            0758
146B A02B            0760         ADA   MSEC                             0759
146D F104            0761         STA   F4                               0760
146F 6ADA            0762         RTJ*  WR.                              0761
1471 0045            0763         DC    X'0045'                          0762
1473 0000            0764  F4     DC    0                                0763
1475 FFFF            0765         DC    -1                               0764
1477 E03F            0766         LDA   SFT                              0765
1479 1124            0767         JAZ   F7                               0766
147B 6AA6            0768         RTJ*  TDIS                             0767
147D 694D            0769         RTJ   F5                               0768
147F 0020            0770         DC    X'0020'                          0769
1481 6A4F            0771         RTJ*  LDWR                             0770
1483 0100            0772         DC    F'256'                           0771
1485 A121            0773         DC    X'A121'                          0772
1487 FF67            0774         DC    X'FF67'                          0773
1489 0082            0775         DC    X'0082'                          0774
148B 61F0            0776         JMP   *-14                             0775
148D 693D            0777         RTJ   F5                               0776
148F 0000            0778         DC    0                                0777
1491 6A4F            0779         RTJ*  LDWR                             0778
1493 05DC            0780         DC    F'1500'                          0779
1495 8301            0781         DC    X'8301'                          0780
1497 FF67            0782         DC    X'FF67'                          0781
1499 0084            0783         DC    X'0084'                          0782
149B 51F0            0784         JMP   *-14                             0783
149D 6AA8            0785         RTJ*  TENA                             0784
149F 6AE4            0786  F7     RTJ*  F.                               0785
14A1 0000            0787         DC    0                                0786
14A3 0000            0788         DC    0                                0787
14A5 0034            0789         DC    X'0034'                          0788
14A7 67141B          0790         JMP=  FTST                             0789
                     0791  *                                             0790
14AA 6AB2            0792  F3     RTJ*  CRLF                             0791
14AC 6AAA            0793         RTJ*  TTEX                             0792
14AE C5CEC4A0        0794         DC    C'END OF FORMAT OPERATION.'      0793
14B2 CFC6A0C6
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
14B6 CFD2CDC1                                                                0794
14BA D4A0CFD0                                                                0795
14BE C502C1D4                                                                0796
14C2 C9CFCEAE                                                                0797
14C6 00              0795          DC    H'0'                                0798
14C7 6A82            0796          RTJ*  CRLF                                0799
14C9 00              0797          HLT                                       0800
14CA 61FD            0798          JMP   *-1                                 0801
                     0799  *SPECIAL ROUTINE FOR FORMAT CHECKS                 0802
                     0800  *CALL  RTJ F5                                      0803
                     0801  *      DC    CONTROL REG SET                     0804
                     0802  *      RTJ*  LDRD/LDWR                           0805
                     0803  *      DC    WAIT                                0806
                     0804  *      DC    STATUS                              0807
                     0805  *      DC    MASK                                0808
                     0806  *      DC    ERROR =                             0809
14CC 0000            0807  F5    DC    **                                  0810
14CE 08              0808          R01                                       0811
14CF EF00            0809          LDV=  H'0'                                0812
14D1 F015            0810          STA   SECTOR                              0813
14D3 81F7            0811          LDX   F5                                  0814
14D5 E027            0812          LDA   UNIT                                0815
14D7 2005            0813          LLA   5                                   0816
14D9 A4              0814          ADA-                                      0817
14DA 6A4B            0815          RTJ*  LDCON                               0818
14DC 09              0816          R02                                       0819
14DD 46              0817          AWX                                       0820
14DE E4              0818          LDA-                                      0821
14DF F101            0819          STA   F51                                 0822
14E1 08              0820          R01                                       0823
14E2 0000            0821  F51     DC    0                                   0824
14E4 09              0822          R02                                       0825
14E5 46              0823          AWX                                       0826
14E6 E4              0824          LDA-                                      0827
14E7 F1F9            0825          STA   F51                                 0828
14E9 46              0826          AWX                                       0829
14EA E4              0827          LDA-                                      0830
14EB 46              0828          AWX                                       0831
14EC D4              0829          ANA-                                      0832
14ED F112            0830          STA   F54+1                               0833
14EF 6A45            0831          RTJ*  SKPDON                              0834
14F1 611C            0832          JMP   F52                                 0835
14F3 79ED            0833          DWM   F51                                 0836
14F5 E1CB            0834          LDA   F51                                 0837
14F7 19F6            0835          NAZ   *-8                                 0838
14F9 46              0836          AWX                                       0839
14FA 89D0            0837  F53     STX   F5                                  0840
14FC A4              0838          ADA-                                      0841
14FD 08              0839          R01                                       0842
14FE 6A94            0840          RTJ*  TERR                                0843
1500 E70000          0841  F54     LDA=  0                                   0844
1503 6ABE            0842          RTJ*  TCNB                                0845
1505 81C5            0843          LDX   F5                                  0846
```

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LOC  OBJECT     ER  STMT  LABEL  OP     OPERANDS                          0843
1507 09             0844         RO2                                      0843
1508 46             0845  F55    AWX                                      0844
1509 6A96           0846         RTJ*   HLTLP                             0845
150B 04             0847         JMP-                                     0846
150C 34             0848         NOP                                      0847
150D 6502           0849         JMP+   2                                 0848
150F 08             0850  F52    RO1                                      0849
1510 0A47           0851         RTJ*   RDSTAT                            0850
1512 D4             0852         ANA-                                     0851
1513 81EC           0853         SBA    F54+1                             0852
1515 09             0854         RO2                                      0853
1516 46             0855         AWX                                      0854
1517 11EF           0856         JAZ    F55                               0855
1519 08             0857         RO1                                      0856
151A EF01           0858         LDV=   H'1'                              0857
151C 61DC           0859         JMP    F53                               0858
                    0860  *FORMAT ROUTINE                                 0859
                    0861  *                                               0860
                    0862  *CALL  RTJ    F15                               0861
                    0863  *      DC     BLOCK ADDRESS                     0862
                    0864  *      DC     WRITE PROTECT                     0863
                    0865  *      DC     ERROR =                           0864
151E 0000           0866  F15    DC     **                                0865
1520 08             0867         RO1                                      0866
1521 EF0C           0868         LDV=   H'12'                             0867
1523 F170           0869         STA    F11                               0868
1525 4C             0870         TAX                                      0869
1526 4F             0871         TXB                                      0870
1527 48             0872         OCB                                      0871
1528 49             0873         INB                                      0872
1529 872340         0874         LDX=   BF2                               0873
152C EF00           0875         LDV=   H'0'                              0874
152E 09             0876         RO2                                      0875
152F F4             0877         STA-                                     0876
1530 46             0878         AWX                                      0877
1531 49             0879         INB                                      0878
1532 1AFB           0880         NBZ    *-3                               0879
1534 E73000         0881         LDA=   X'8000'                           0880
1537 F4             0882         STA-                                     0881
1538 46             0883         AWX                                      0882
1539 E3E3           0884         LDA*   F15                               0883
153B 71E1           0885         IWM    F15                               0884
153D 71DF           0886         IWM    F15                               0885
153F A3DD           0887         ADA*   F15                               0886
1541 F4             0888         STA-                                     0887
1542 8953           0889         STX    F11+2                             0888
1544 E3D8           0890         LDA*   F15                               0889
1546 F151           0891         STA    F11+4                             0890
1548 46             0892         AWX                                      0891
1549 71D3           0893         IWM    F15                               0892
154B 71D1           0894         IWM    F15                               0893
154D 08             0895         RO1                                      0894
154E EF02           0896         LDV=   H'2'                              0895
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
1550 A143            0897         ADA    F11                    0896
1552 F011            0898         STA    WCCA                   0897
1554 EF00            0899         LDV=   H'0'                   0898
1556 F015            0900         STA    SECTOR                 0899
1558 F019            0901         STA    BLOCKS                 0900
155A E09E            0902         LDA    WRITE                  0901
155C F005            0903         STA    DATA1                  0902
155E E705DC          0904         LDA=   F'1500'                0903
1561 F007            0905         STA    DATA1+2                0904
1563 E339            0906         LDA*   F15                    0905
1565 F009            0907         STA    DATA1+4                0906
1567 7185            0908         IWM    F15                    0907
1569 7183            0909         IWM    F15                    0908
156B EFFF            0910         LDV=   H'-1'                  0909
156D F00B            0911         STA    DATA1+6                0910
156F F00D            0912         STA    DATA1+8                0911
1571 E02B            0913         LDA    MSEC                   0912
1573 F120            0914         STA    F11                    0913
1575 E027            0915         LDA    UNIT                   0914
1577 2005            0916         LLA    5                      0915
1579 AF20            0917         ADV=   X'20'                  0916
157B 6A4B            0918         RTJ*   LDCON                  0917
157D 6AE6            0919  F13    RTJ*   RW.                    0918
157F 61F4            0920         JMP    F13-8                  0919
1581 E015            0921         LDA    SECTOR                 0920
1583 F017            0922         STA    SECTOR+2               0921
1585 48              0923         INA                           0922
1586 F015            0924         STA    SECTOR                 0923
1588 A10F            0925         ADA    F11+4                  0924
158A F30B            0926         STA*   F11+2                  0925
158C 7907            0927         DWM    F11                    0926
158E E105            0928         LDA    F11                    0927
1590 19EB            0929         NAZ    F13                    0928
1592 67151E          0930         JMP=   F15                    0929
1595 0006            0931  F11    DS     6                      0930
                     0932  *READ - WRITE ROUTINE                0931
                     0933  *CALL  RTJ    RW                     0932
                     0934  *      ERROR                         0933
                     0935  *      OK                            0934
1598 0000            0936  RW     DC     **                     0935
159A 6A05            0937         RTJ*   DATA1                  0936
159F 8007            0938         LDX    DATA1+2                0937
15A1 6A45            0939         RTJ*   SKPDON                 0938
15A3 6114            0940         JMP    RW2                    0939
15A5 45              0941         DCX                           0940
15A6 1BF9            0942         NXZ    *-5                    0941
15A8 EF00            0943         LDV=   H'0'                   0942
15AA 6E1643          0944         RTJ/   RW3                    0943
15AD 6A57            0945         RTJ*   RESET                  0944
15AF 39E0            0946         OBA    7,0                    0945
15B1 81E8            0947  RW0    LDX    RW                     0946
15B3 6A96            0948         RTJ*   HLTLP                  0947
15B5 64              0949         JMP-                          0948
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                    0949
15B6 34              0950         NOP                                0949
15B7 6502            0951         JMP+   2                           0950
15B9 1C06            0952  RW2    NAN    RW4                         0951
15BB EF01            0953         LDV=   H'1'                        0952
15BD 6BEC            0954         RTJ*   RW0-6                       0953
15BF 6115            0955         JMP    RW9                         0954
15C1 E00B            0956  RW4    LDA    DATA1+6                     0955
15C3 1111            0957         JAZ    RW9                         0956
15C5 E02F            0958         LDA    DAVAL                       0957
15C7 A015            0959         ADA    SECTOR                      0958
15C9 A019            0960         ADA    BLOCKS                      0959
15CB 4C              0961         TAX                                0960
15CC 6A49            0962         RTJ*   RDBAR                       0961
15CE 1706            0963         JAX    RW9                         0962
15D0 EF02            0964         LDV=   H'2'                        0963
15D2 697B            0965         RTJ    R31                         0964
15D4 61D7            0966         JMP    RW0-4                       0965
15D6 E00D            0967  RW9    LDA    DATA1+8                     0966
15D8 19D7            0968         NAZ    RW0                         0967
15DA 8011            0969         LDX    WCCA                        0968
15DC 4F              0970         IXB                                0969
15DD 4B              0971         DCB                                0970
15DE 49              0972         INB                                0971
15DF E72040          0973         LDA=   BF1                         0972
15E2 F106            0974         STA    RW1+1                       0973
15E4 872340          0975         LDX=   BF2                         0974
15E7 09              0976         RD2                                0975
15E8 E4              0977         LDA-                               0976
15E9 B60000          0978  RW1    SBA/   **                          0977
15EC 1915            0979         NAZ    RW6                         0978
15EE 71FA            0980         IWM    RW1+1                       0979
15F0 71F8            0981         IWM    RW1+1                       0980
15F2 46              0982         AWX                                0981
15F3 49              0983         INB                                0982
15F4 1AF2            0984         NBZ    RW1-1                       0983
15F6 08              0985  RW7    RD1                                0984
15F7 E4              0986         LDA-                               0985
15F8 B7DB6D          0987         SBA=   X'DB6D'                     0986
15FB 11B4            0988         JAZ    RW0                         0987
15FD EF04            0989         LDV=   H'4'                        0988
15FF 694E            0990         RTJ    R31                         0989
1601 61AE            0991         JMP    RW0                         0990
1603 08              0992  RW6    RD1                                0991
1604 8912            0993         STX    RW8-2                       0992
1606 4D              0994         TBX                                0993
1607 8912            0995         STX    RW8+1                       0994
1609 EF03            0996         LDV=   H'3'                        0995
160B 6942            0997         RTJ    R31                         0996
160D EFF8            0998  R13    LDV=   H'-8'                       0997
160F F120            0999         STA    R11+1                       0998
1611 8105            1000         LDX    RW8-2                       0999
1613 E105            1001  R12    LDA    RW1+1                       1000
1615 6A98            1002         RTJ*   TDAT                        1001
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                    1002
1617 870000          1003         LDX=   0                           1003
161A 770000          1004   RW8   IWM=   0                           1004
161D E1FC            1005         LDA    *-2                         1005
161F 09              1006         KO2                                1006
1620 46              1007         AWX                                1007
1621 1103            1008         JAZ    RW7                         1008
1623 71C5            1009         IWM    RW1+1                       1009
1625 71C3            1010         IWM    RW1+1                       1010
1627 E4              1011         LDA-                               1011
1628 83C0            1012         SBA*   RW1+1                       1012
162A 11EE            1013         JAZ    RW8                         1013
162C 89EA            1014         STX    RW8-2                       1014
162E 7101            1015         IWM    R11+1                       1015
1630 E70000          1016   R11   LDA=   0                           1016
1633 190E            1017         NAZ    R12                         1017
1635 08              1018         KO1                                1018
1636 02              1019         ESW                                1019
1637 14D4            1020         JAN    R13                         1020
1639 E011            1021         LDA    WCCA                        1021
163B 2801            1022         ALA    1                           1022
163D A72340          1023         ADA=   BF2                         1023
1640 4C              1024         TAX                                1024
1641 61B3            1025         JMP    RW7                         1025
1643 0000            1026   RW3   DC     **                          1026
1645 A009            1027         ADA    DATA1+4                     1027
1647 6A94            1028         RTJ*   TERR                        1028
1649 6A9A            1029         RTJ*   TADD                        1029
164B 6A43            1030         RTJ*   CLSTAT                      1030
164D 63F4            1031         JMP*   RW3                         1031
164F 0000            1032   R31   DC     **                          1032
1651 6A9C            1033         RTJ*   SADD                        1033
1653 69EE            1034         RTJ    RW3                         1034
1655 E017            1035         LDA    SECTOR+2                    1035
1657 F015            1036         STA    SECTOR                      1036
1659 63F4            1037         JMP*   R31                         1037
                     1038   *CALL RTJ    W11                         1038
                     1039   *     DC     ERROR =                     1039
                     1040   *     DC     START DATA VALUE            1040
                     1041   *     DC     MODIFY VALUE                1041
165B 0000            1042   W11   DC     **                          1042
165D 08              1043         KO1                                1043
165E E3FB            1044         LDA*   W11                         1044
1660 F009            1045         STA    DATA1+4                     1045
1662 EF00            1046         LDV=   H'0'                        1046
1664 F008            1047         STA    DATA1+6                     1047
1666 F00D            1048         STA    DATA1+8                     1048
1668 E705DC          1049         LDA=   F'1500'                     1049
166B F007            1050         STA    DATA1+2                     1050
166D E09E            1051         LDA    WRITE                       1051
166F F005            1052         STA    DATA1                       1052
1671 EF01            1053         LDV=   H'1'                        1053
1673 F019            1054         STA    BLOCKS                      1054
1675 F011            1055         STA    WCCA                        1055
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LOC  OBJECT    ER  STMT  LABEL  OP     OPERANDS
1677 E027          1056         LDA    UNIT                    1055
1679 2005          1057         LLA    5                       1056
167B 6A4B          1058         RTJ*   LDCON                   1057
167D 09            1059         R02                            1058
167E 81DB          1060         LDX    W11                     1059
1680 46            1061         AWX                            1060
1681 E4            1062         LDA-                           1061
1682 F118          1063         STA    W12                     1062
1684 46            1064         AWX                            1063
1685 E4            1065         LDA-                           1064
1686 F116          1066         STA    W12+2                   1065
1688 46            1067         AWX                            1066
1689 89D0          1068         STX    W11                     1067
168B 08            1069         R01                            1068
168C 6912          1070         RTJ    W13                     1069
168E E0A0          1071         LDA    READ                    1070
1690 F005          1072         STA    DATA1                   1071
1692 EF04          1073         LDV=   H'4'                    1072
1694 A009          1074         ADA    DATA1+4                 1073
1696 F009          1075         STA    DATA1+4                 1074
1698 6906          1076         RTJ    W13                     1075
169A 63BF          1077         JMP*   W11                     1076
169C 0004          1078  W12    DS     4                       1077
16A0 0000          1079  W13    DC     **                      1078
16A2 6944          1080         RTJ    W18                     1079
16A4 6950          1081         RTJ    W17                     1080
16A6 694E          1082         RTJ    W17                     1081
16A8 EF02          1083         LDV=   H'2'                    1082
16AA F015          1084         STA    SECTOR                  1083
16AC 6914          1085         RTJ    W15                     1084
16AE 6938          1086         RTJ    W18                     1085
16B0 6944          1087         RTJ    W17                     1086
16B2 EF01          1088         LDV=   H'1'                    1087
16B4 F015          1089         STA    SECTOR                  1088
16B6 690A          1090         RTJ    W15                     1089
16B8 692E          1091         RTJ    W18                     1090
16BA EF00          1092         LDV=   H'0'                    1091
16BC F015          1093         STA    SECTOR                  1092
16BE 6902          1094         RTJ    W15                     1093
16C0 63DE          1095         JMP*   W13                     1094
16C2 0000          1096  W15    DC     **                      1095
16C4 E005          1097  W16    LDA    DATA1                   1096
16C6 B09E          1098         SBA    WRITE                   1097
16C8 1904          1099         NAZ    *+6                     1098
16CA 6AA2          1100         RTJ*   M12                     1099
16CC 6102          1101         JMP    *+4                     1100
16CE 6AA4          1102         RTJ*   CLR2                    1101
16D0 6AE6          1103         RTJ*   RW.                     1102
16D2 61F0          1104         JMP    W16                     1103
16D4 6A9C          1105         RTJ*   SADD                    1104
16D6 6A9C          1106         RTJ*   SADD                    1105
16D8 6A9C          1107         RTJ*   SADD                    1106
16DA 691A          1108         RTJ    W17                     1107
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LOC  OBJECT      ER  STMT  LABEL   OP     OPERANDS
160C 6918            1109          RTJ    W17                    1108
160E 6916            1110          RTJ    W17                    1109
16E0 E015            1111          LDA    SECTOR                 1110
16E2 B028            1112          SBA    MSEC                   1111
16E4 14DE            1113          JAN    W16                    1112
16E6 63DA            1114          JMP*   W15                    1113
16E8 0000            1115  W18     DC     **                     1114
16EA E180            1116          LDA    W12                    1115
16EC F62040          1117          STA/   BF1                    1116
16EF E1AD            1118          LDA    W12+2                  1117
16F1 F62042          1119          STA/   BF1+2                  1118
16F4 63F2            1120          JMP*   W18                    1119
16F6 0000            1121  W17     DC     **                     1120
16F8 E1A4            1122          LDA    W12+2                  1121
16FA A3F1            1123          ADA*   W18+5                  1122
16FC F3EF            1124          STA*   W18+5                  1123
16FE 63F6            1125          JMP*   W17                    1124
1700 0000            1126  SABTST  DC     **                     1125
1702 08              1127          RO1                           1126
1703 EF00            1128          LDV=   H'0'                   1127
1705 F118            1129          STA    S1                     1128
1707 EF55            1130          LDV=   X'55'                  1129
1709 6918            1131          RTJ    S2                     1130
1708 E112            1132  S5      LDA    S1                     1131
170D 6939            1133          RTJ    S3                     1132
170F E110            1134          LDA    S1+2                   1133
1711 6935            1135          RTJ    S3                     1134
1713 790C            1136          DWM    S1+2                   1135
1715 E108            1137          LDA    S1                     1136
1717 7106            1138          INM    S1                     1137
1719 B106            1139          SBA    S1+2                   1138
171B 19EE            1140          NAZ    S5                     1139
171D 63E1            1141          JMP*   SABTST                 1140
171F 0004            1142  S1      DS     4                      1141
1723 0000            1143  S2      DC     **                     1142
1725 F009            1144          STA    DATA1+4                1143
1727 802B            1145          LDX    MSEC                   1144
1729 45              1146          DCX                           1145
172A 89F5            1147          STX    S1+2                   1146
172C E0A0            1148          LDA    READ                   1147
172E F005            1149          STA    DATA1                  1148
1730 E705DC          1150          LDA=   F'1500'                1149
1733 F007            1151          STA    DATA1+2                1150
1735 EF00            1152          LDV=   H'0'                   1151
1737 F008            1153          STA    DATA1+6                1152
1739 F003            1154          STA    DATA1+3                1153
173B 48              1155          INA                           1154
173C F019            1156          STA    BLOCKS                 1155
173E F011            1157          STA    #CCA                   1156
1740 E027            1158          LDA    UNIT                   1157
1742 2005            1159          LLA    5                      1158
1744 6A4B            1160          RTJ*   LOCON                  1159
1746 63D8            1161          JMP*   S2                     1160
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LOC  OBJECT     ER  STMT  LABEL   OP     OPERANDS
1748 0000           1162  S3      DC     **
174A F015           1163          STA    SECTOR
174C F62040         1164          STA/   BF1
174F 6AA4           1165          RTJ*   CLR2
1751 6AE6           1166          RTJ*   RW.
1753 61FA           1167          JMP    *-4
1755 63F1           1168          JMP*   S3
                    1169  *RANDOM SEEK TEST
1757 0000           1170  RANTST  DC     **
1759 E70200         1171          LDA=   F'512'
175C F116           1172          STA    RA1+1
175E 08             1173          ROI
175F EF59           1174          LDV=   X'59'
1761 69C0           1175          RTJ    S2
1763 6917           1176  RA3     RTJ    GRN
1765 2401           1177          LRA    1
1767 F015           1178          STA    SECTOR
1769 B026           1179          SBA    MSEC
176B 1CFA           1180          NAN    *-4
176D E015           1181          LDA    SECTOR
176F 6907           1182          RTJ    S3
1771 7901           1183          DWM    RA1+1
1773 E70000         1184  RA1     LDA=   0
1776 19EB           1185          NAZ    RA3
1778 63DD           1186          JMP*   RANTST
177A ABCD           1187          DC     X'ABCD'
177C 0000           1188  GRN     DC     **
177E E1FA           1189          LDA    GRN-2
1780 08             1190          ROI
1781 DF0F           1191          ANV=   H'15'
1783 F906           1192          STV    *+8
1785 E1F3           1193          LDA    GRN-2
1787 A78CA1         1194          ADA=   F'-29535'
178A 2000           1195          LLA    **
178C A1EC           1196          ADA    GRN-2
178E F1EA           1197          STA    GRN-2
1790 63EA           1198          JMP*   GRN
                    1199  *
                    1200  *SINGLE BLOCK WRITE/READ TEST
1792 0000           1201  BDATST  DC     **
1794 E021           1202          LDA    SINSEC
1796 6E182E         1203          RTJ/   DRW
1799 009E           1204          DC     WRITE
1798 05DC           1205          DC     F'1500'
179D 005D           1206          DC     X'005D'
179F 0180           1207          DC     F'384'
17A1 0001           1208          DC     1
17A3 0000           1209          DC     0
17A5 0001           1210          DC     1
17A7 FFFF           1211          DC     F'-1'
17A9 E021           1212          LDA    SINSEC
17AB 6BEA           1213          RTJ*   BDATST+5
17AD 00A0           1214          DC     READ
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
17AF 05DC            1215         DC     F'1500'                    1214
17B1 0062            1216         DC     X'0062'                    1215
17B3 0180            1217         DC     F'384'                     1216
17B5 0001            1218         DC     1                          1217
17B7 0000            1219         DC     0                          1218
17B9 0001            1220         DC     1                          1219
17BB FFFF            1221         DC     F'-1'                      1220
17BD E023            1222         LDA    MULSEC                     1221
17BF 6BD6            1223         RTJ*   BDATST+5                   1222
17C1 00A0            1224         DC     READ                       1223
17C3 05DC            1225         DC     F'1500'                    1224
17C5 0067            1226         DC     X'0067'                    1225
17C7 0180            1227         DC     F'384'                     1226
17C9 0002            1228         DC     2                          1227
17CB 0000            1229         DC     0                          1228
17CD 0001            1230         DC     1                          1229
17CF FFFF            1231         DC     F'-1'                      1230
17D1 63BF            1232         JMP*   BDATST                     1231
                     1233  *                                        1232
                     1234  *MULTIPLE BLOCK WRITE/READ TEST          1233
17D3 0000            1235  MDST   DC     **                         1234
17D5 E023            1236         LDA    MULSEC                     1235
17D7 6955            1237         RTJ    DRW                        1236
17D9 009E            1238         DC     WRITE                      1237
17DB 05DC            1239         DC     F'1500'                    1238
17DD 006C            1240         DC     X'006C'                    1239
17DF 0180            1241         DC     F'384'                     1240
17E1 0002            1242         DC     2                          1241
17E3 0000            1243         DC     0                          1242
17E5 0001            1244         DC     1                          1243
17E7 FFFF            1245         DC     F'-1'                      1244
17E9 E023            1246         LDA    MULSEC                     1245
17EB 6941            1247         RTJ    DRW                        1246
17ED 00A0            1248         DC     READ                       1247
17EF 05DC            1249         DC     F'1500'                    1248
17F1 0071            1250         DC     X'0071'                    1249
17F3 0180            1251         DC     F'384'                     1250
17F5 0002            1252         DC     2                          1251
17F7 0000            1253         DC     0                          1252
17F9 0001            1254         DC     1                          1253
17FB FFFF            1255         DC     F'-1'                      1254
17FD E021            1256         LDA    SINSEC                     1255
17FF 692D            1257         RTJ    DRW                        1256
1801 00A0            1258         DC     READ                       1257
1803 05DC            1259         DC     F'1500'                    1258
1805 0076            1260         DC     X'0076'                    1259
1807 0180            1261         DC     F'384'                     1260
1809 0001            1262         DC     1                          1261
180B 0000            1263         DC     0                          1262
180D 0002            1264         DC     2                          1263
180F FFFE            1265         DC     F'-2'                      1264
1811 E021            1266         LDA    SINSEC                     1265
1813 2C02            1267         ARA    2                          1266
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
1615 F10A            1268         STA    MD2                                1267
1817 E021            1269         LDA    SINSEC                             1268
1819 6913            1270         RTJ    DRW                                1269
181B 00A0            1271         DC     READ                               1270
181D 050C            1272         DC     F'1500'                            1271
181F 0076            1273         DC     X'0076'                            1272
1821 0000            1274  MD2    DC     0                                  1273
1823 0001            1275         DC     1                                  1274
1825 0001            1276         DC     1                                  1275
1827 0002            1277         DC     2                                  1276
1829 FFFE            1278         DC     F'-2'                              1277
182B 6717D3          1279         JMP=   MDST                               1278
                     1280  *READ/WRITE ENTIRE DISK-DATA PATTERN.             1279
                     1281  *CALL  LDA=WORD COUNT                             1280
                     1282  *      RTJ    DRW                                1281
                     1283  *      DC     READ/WRITE                         1282
                     1284  *      DC     WAIT TIME                          1283
                     1285  *      DC     BASE ERROR =                       1284
                     1286  *      DC     PATTERN LENGTH (IN WORDS)          1285
                     1287  *      DC     = BLOCKS                           1286
                     1288  *      DC     START                              1287
                     1289  *      DC     INTERLACE                          1288
                     1290  *      DC                                        1289
182E 0000            1291  DRW    DC     **                                 1290
1830 2C01            1292         ARA    1                                  1291
1832 F011            1293         STA    WCCA                               1292
1834 81F8            1294         LDX    DRW                                1293
1836 09              1295         RO2                                       1294
1837 E4              1296         LDA-                                      1295
1838 F005            1297         STA    DATA1                              1296
183A E205            1298         LDA*   DATA1                             1297
183C F005            1299         STA    DATA1                              1298
183E 46              1300         AWX                                       1299
183F E4              1301         LDA-                                      1300
1840 F007            1302         STA    DATA1+2                            1301
1842 46              1303         AWX                                       1302
1843 E4              1304         LDA-                                      1303
1844 F009            1305         STA    DATA1+4                            1304
1846 46              1306         AWX                                       1305
1847 89E5            1307         STX    DRW                                1306
1849 08              1308         RO1                                       1307
184A EF00            1309         LDV=   H'0'                               1308
184C F00D            1310         STA    DATA1+8                            1309
184E 4A              1311         OCA                                       1310
184F F00B            1312         STA    DATA1+6                            1311
1851 E4              1313         LDA-                                      1312
1852 6E13D1          1314         RTJ/   PATGEN                             1313
1855 81D7            1315         LDX    DRW                                1314
1857 09              1316         RO2                                       1315
1858 46              1317         AWX                                       1316
1859 E4              1318         LDA-                                      1317
185A F019            1319         STA    BLOCKS                             1318
185C 46              1320         AWX                                       1319
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                    
185D E4              1321         LDA-                        1320
185E F16F            1322         STA    DK2+4                1321
1860 46              1323         AWX                         1322
1861 E4              1324         LDA-                        1323
1862 F169            1325         STA    DK2+2                1324
1864 46              1326         AWX                         1325
1865 E4              1327         LDA-                        1326
1866 F163            1328         STA    DK2                  1327
1868 46              1329         AWX                         1328
1869 89C3            1330         STX    DRW                  1329
186B 08              1331         RU1                         1330
186C E021            1332         LDA    SINSEC               1331
186E A10C            1333         ADA    DK1+1                1332
1870 F115            1334         STA    DK3-2                1333
1872 E027            1335         LDA    UNIT                 1334
1874 2005            1336         LLA    5                    1335
1876 6A4B            1337         RTJ*   LDCON                1336
1878 E155            1338  DK5    LDA    DK2+4                1337
187A 4A              1339         OCA                         1338
187B F62040          1340  DK1    STA/   BF1                  1339
187E E14F            1341         LDA    DK2+4                1340
1880 F015            1342         STA    SECTOR               1341
1882 E14B            1343         LDA    DK2+4                1342
1884 48              1344         INA                         1343
1885 4A              1345         OCA                         1344
1886 F60000          1346         STA/   **                   1345
1889 E005            1347  DK3    LDA    DATA1                1346
188B B09E            1348         SBA    WRITE                1347
188D 1904            1349         NAZ    *+6                  1348
188F 6AA2            1350         RTJ*   M12                  1349
1891 6102            1351         JMP    *+4                  1350
1893 6AA4            1352         RTJ*   CLR2                 1351
1895 6AE6            1353         RTJ*   RW.                  1352
1897 61F0            1354         JMP    DK3                  1353
1899 E130            1355         LDA    DK2                  1354
189B F10B            1356         STA    DK6+1                1355
189D 6A9C            1357  DK4    RTJ*   SADD                 1356
189F E30B            1358         LDA*   DK1+1                1357
18A1 B019            1359         SBA    BLOCKS               1358
18A3 F3D7            1360         STA*   DK1+1                1359
18A5 7101            1361         IWM    DK6+1                1360
18A7 E70000          1362  DK6    LDA=   0                    1361
18AA 19F1            1363         NAZ    DK4                  1362
18AC 4A              1364         OCA                         1363
18AD A3CD            1365         ADA*   DK1+1                1364
18AF F3D6            1366         STA*   DK3-2                1365
18B1 E015            1367         LDA    SECTOR               1366
18B3 B02B            1368         SBA    MSEC                 1367
18B5 14D2            1369         JAN    DK3                  1368
18B7 8114            1370         LDX    DK2+2                1369
18B9 EF00            1371         LDV=   H'0'                 1370
18BB A019            1372         ADA    BLOCKS               1371
18BD 45              1373         DCX                         1372
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LOC  OBJECT      ER  STMT  LABEL   OP    OPERANDS                    1373
18BE 1BFB            1374          NXZ   *-3                         1374
18C0 4A              1375          OCA                               1375
18C1 48              1376          INA                               1376
18C2 A10B            1377          ADA   DK2+4                       1377
18C4 F109            1378          STA   DK2+4                       1378
18C6 1CB0            1379          NAN   DK5                         1379
18C8 67182E          1380          JMP=  DRW                         1380
18CB 0006            1381  DK2     DS    6                           1381
                     1382  *PATTERN GENERATION                       1382
                     1383  *CALL   LDA= LENGTH                       1383
                     1384  *       RTJ   PATGEN                      1384
18D1 0000            1385  PATGEN  DC    **                          1385
18D3 4C              1386          TAX                               1386
18D4 4F              1387          IXB                               1387
18D5 4B              1388          OCB                               1388
18D6 49              1389          INB                               1389
18D7 E7FE80          1390          LDA=  F'-384'                     1390
18DA F119            1391          STA   PG1+1                       1391
18DC 872040          1392          LDX=  BF1                         1392
18DF 691A            1393          RTJ   PG3                         1393
18E1 610F            1394          JMP   PG1-2                       1394
18E3 6916            1395          RTJ   PG3                         1395
18E5 610B            1396          JMP   PG1-2                       1396
18E7 6912            1397          RTJ   PG3                         1397
18E9 6107            1398          JMP   PG1-2                       1398
18EB 63E4            1399          JMP*  PATGEN                      1399
18ED EF00            1400          LDV=  H'0'                        1400
18EF F4              1401          STA-                              1401
18F0 44              1402          INX                               1402
18F1 44              1403          INX                               1403
18F2 7101            1404          IWM   PG1+1                       1404
18F4 E70000          1405  PG1     LDA=  0                           1405
18F7 19F4            1406          NAZ   *-10                        1406
18F9 63D6            1407          JMP*  PATGEN                      1407
18FB 0000            1408  PG3     DC    **                          1408
18FD E7AAAA          1409          LDA=  X'AAAA'                     1409
1900 F157            1410          STA   PG5                         1410
1902 E7197E          1411          LDA=  P42                         1411
1905 6955            1412          RTJ   P41                         1412
1907 63F2            1413          JMP*  PG3                         1413
1909 EF00            1414          LDV=  H'0'                        1414
190B F14C            1415          STA   PG5                         1415
190D E1F4            1416          LDA   *-10                        1416
190F 6946            1417          RTJ   P41                         1417
1911 63E3            1418          JMP*  PG3                         1418
1913 EFFE            1419          LDV=  H'-2'                       1419
1915 F142            1420          STA   PG5                         1420
1917 E71982          1421  PG6     LDA=  P43                         1421
191A 6940            1422          RTJ   P41                         1422
191C 6364            1423          JMP*  P43                         1423
191E E78E38          1424          LDA=  X'8E38'                     1424
1921 F136            1425          STA   PG5                         1425
1923 E7198C          1426          LDA=  P44                         1426
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS                    1426
1926 6934            1427         RTJ   P41                         1426
1928 63D1            1428         JMP*  PG3                         1427
192A E75555          1429         LDA=  X'5555'                     1428
192D F12A            1430         STA   PG5                         1429
192F E1D2            1431         LDA   PG3+8                       1430
1931 6929            1432         RTJ   P41                         1431
1933 63C6            1433         JMP*  PG3                         1432
1935 EF01            1434         LDV=  H'1'                        1433
1937 F120            1435         STA   PG5                         1434
1939 E1DD            1436         LDA   PG6+1                       1435
193B 691F            1437         RTJ   P41                         1436
193D 63BC            1438         JMP*  PG3                         1437
193F EFFF            1439         LDV=  H'-1'                       1438
1941 F116            1440         STA   PG5                         1439
1943 E1BE            1441         LDA   PG3+8                       1440
1945 6915            1442         RTJ   P41                         1441
1947 63B2            1443         JMP*  PG3                         1442
1949 EF00            1444         LDV=  H'0'                        1443
194B F1DC            1445         STA   PG5                         1444
194D E1D5            1446         LDA   PG6+13                      1445
194F 6908            1447         RTJ   P41                         1446
1951 63A8            1448         JMP*  PG3                         1447
1953 71A6            1449         IWM   PG3                         1448
1955 71A4            1450         IWM   PG3                         1449
1957 63A2            1451         JMP*  PG3                         1450
1959 0000            1452  PG5    DC    0                           1451
1958 66              1453         DC    X'66'                       1452
195C 0000            1454  P41    DC    **                          1453
195E F108            1455         STA   *+13                        1454
1960 08              1456         RO1                               1455
1961 EFF0            1457         LDV=  H'-16'                      1456
1963 F10E            1458         STA   *+16                        1457
1965 E1F2            1459         LDA   PG5                         1458
1967 F4              1460         STA-                              1459
1968 44              1461         INX                               1460
1969 44              1462         INX                               1461
196A 6E0000          1463         RTJ/  **                          1462
196D 49              1464         INB                               1463
196E 12E8            1465         JBZ   P41-1                       1464
1970 7183            1466         IWM   PG1+1                       1465
1972 E70000          1467         LDA=  0                           1466
1975 48              1468         INA                               1467
1976 19E8            1469         NAZ   P41+7                       1468
1978 71E2            1470         IWM   P41                         1469
197A 71E0            1471         IWM   P41                         1470
197C 63DE            1472         JMP*  P41                         1471
197E 0000            1473  P42    DC    **                          1472
1980 63FC            1474         JMP*  P42                         1473
1982 0000            1475  P43    DC    **                          1474
1984 E1D3            1476         LDA   PG5                         1475
1986 2001            1477         LLA   1                           1476
1988 F1CF            1478         STA   PG5                         1477
198A 63F6            1479         JMP*  P43                         1478
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS                                    
198C 0000            1480  P44    DC    **                                          1479
198E E1C9            1481        LDA   PG5                                         1480
1990 4A              1482        CCA                                               1481
1991 F1C6            1483        STA   PG5                                         1482
1993 63F7            1484        JMP*  P44                                         1483
                     1485  * PARAMETER INPUT ROUTINE                               1484
1995 0000            1486  PARAM  DC    **                                          1485
1997 EF00            1487        LDV=  H'0'                                        1486
1999 F02F            1488        STA   DAVAL                                       1487
199B F031            1489        STA   EFG                                         1488
199D EFF9            1490        LDV=  H'-7'                                       1489
199F F033            1491        STA   EF1                                         1490
19A1 EF01            1492        LDV=  H'1'                                        1491
19A3 F039            1493        STA   PASS1                                       1492
19A5 EFFC            1494        LDV=  H'-4'                                       1493
19A7 F118            1495        STA   PR1+1                                       1494
19A9 E72000          1496        LDA=  DDAT                                        1495
19AC F109            1497        STA   PR2                                         1496
19AE 6E1A6A          1498  PR3    RTJ/  UNPAR       GET UNIT PARAMETERS           1497
19B1 6115            1499        JMP   P21                                         1498
19B3 6AC0            1500        RTJ*  M.          SAVE THEM                     1499
19B5 0018            1501        DC    TDSK                                        1500
19B7 0000            1502  PR2    DC    0                                           1501
19B9 0010            1503        DC    MSEC-TDSK                                   1502
19BB E1FA            1504        LDA   PR2                                         1503
19BD A1FA            1505        ADA   PR2+2             INCR PARAMETER ADDR      1504
19BF F1F6            1506        STA   PR2                                         1505
19C1 7101            1507        IWM   PR1+1                                       1506
19C3 E70000          1508  PR1    LDA=  0                                           1507
19C6 19E6            1509        NAZ   PR3         DONE                          1508
19C8 E1FA            1510  P21    LDA   PR1+1                                       1509
19CA AF04            1511        ADV=  H'4'                                        1510
19CC 11C9            1512        JAZ   PARAM+2                                     1511
19CE F037            1513        STA   PORTS                                       1512
19D0 6AB2            1514  P22    RTJ*  CRLF                                        1513
19D2 6AAA            1515        RTJ*  TTEX                                        1514
19D4 D4D9D0C5        1516        DC    C'TYPE CONTROLLER DEVICE CODE  '            1515
19D8 A0C3CFCE
19DC D4D2CFCC
19E0 CCC5D2A0
19E4 C4C5D6C9
19E8 C3C5A0C3
19EC CFC4C5A0
19F0 A0
19F1 00              1517        DC    H'0'                                        1516
19F2 6AC4            1518        RTJ*  HI.         READ HEX                      1517
19F4 F02D            1519        STA   ADDRESS                                     1518
19F6 870100          1520        LDX=  X'100'      SET ALL INTERRUPT LOC TO ILP  1519
19F9 EFC0            1521        LDV=  H'-64'                                      1520
19FB 2E10            1522        ARL   16                                          1521
19FD E0C2            1523        LDA   IT.                                         1522
19FF 09              1524        R02                                               1523
1A00 F4              1525        STA-                                              1524
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS
1A01 46              1526        AWX
1A02 49              1527        INB
1A03 1AFB            1528        NBZ   *-3
1A05 08              1529        RU1
1A06 6A82            1530        RTJ*  CRLF
1A08 6AAA            1531        RTJ*  TTEX
1A0A C5CED4C5        1532        DC    C'ENTER FORMAT LOOP CONTROL'
1A0E D2A0C6CF
1A12 D2CDC1D4
1A16 A0CCCFCF
1A1A D0A0C3CF
1A1E CED4D2CF
1A22 CC
1A23 00              1533        DC    H'0'
1A24 EF00            1534        LDV=  H'0'
1A26 F038            1535        STA   LPFORM
1A28 F03D            1536        STA   FUY
1A2A F03F            1537        STA   SFT
                     1538  * SW  3 2 1
                     1539  *     S R F
                     1540  *F=0   FORMAT ONCE.
                     1541  *F=1   FORMAT AT BEGIN OF EACH PASS.
                     1542  *R=0   RUN COMPLETE DIAGNOSTIC.
                     1543  *R=1   FORMAT ONLY.
                     1544  *S=0   SPECIAL FORMAT TEST NOT RUN.
                     1545  *S=1   SPECIAL FORMAT TEST RUN.
1A2C 6AC8            1546        RTJ*  ES.
1A2E 2801            1547        ALA   1
1A30 1C02            1548        NAN   *+4
1A32 703F            1549        IWM   SFT
1A34 2801            1550        ALA   1
1A36 1C02            1551        NAN   *+4
1A38 7038            1552        IWM   FUY
1A3A 2801            1553        ALA   1
1A3C 1C02            1554        NAN   *+4
1A3E 7038            1555        IWM   LPFORM
1A40 6E18B7          1556        RTJ/  ETNA1
1A43 6AAA            1557        RTJ*  TTEX
1A45 A0C5D2D2        1558        DC    C' ERROR AND TYPE OUT CONTROLS'
1A49 CFD2A0C1
1A4D CEC4A0D4
1A51 D9D0C5A0
1A55 CFD5D4A0
1A59 C3CFCED4
1A5D D2CFCCD3
1A61 8D3A00      *   1559        DC    X'8D8A00'
                     1560  *SW  4  5  2  1
                     1561  *    A  I  H  R
                     1562  *R=0   CONTINUES WITH TEST.
                     1563  *R=1   REPEATS CURRENT OPERATION.
                     1564  *H=0   HALTS ON EACH ERROR.
                     1565  *H=1   CONTINUES ON ERRORS.
                     1566  *T=0   TYPE OUT ALL ERRORS.
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
                    1567  *T=1   DELETE TYPE OUT.                                                    1566
                    1568  *A=0   TYPE OUT ONLY FIRST 8 ERRORS.                                       1567
                    1569  *A=1   TYPE OUT ALL ERRORS.                                               1568
1A64 00             1570         HLT                                                               1569
1A65 05             1571         EIN              ENABLE INTERRUPT                                 1570
1A66 671995         1572         JMP=  PARAM                                                       1571
                    1573  * ENTER PARAMETERS FOR A DISK PORT                                        1572
                    1574  *                                                                         1573
                    1575  * SW 4 3 2 1                                                             1574
                    1576  *    D T U U          UU=UNIT, T=TYPE OF DISC,D=DONE                      1575
                    1577  *    F  S Z                Z=TRACKS/INCH,S=SECTORS/TRACKS,F=FULL         1576
                    1578  *       X R                                                             1577
                    1579  *T=0   FIXED HEAD DISK.                                                   1578
                    1580  *T=1   MOVING HEAD DISK.                                                  1579
                    1581  *D=0   ENTER PARAMETERS.                                                  1580
                    1582  *D=1   DONE.                                                              1581
                    1583  *                                                                         1582
                    1584  *Z=0   100 TPI                                                            1583
                    1585  *Z=1   200 TPI                                                            1584
                    1586  *S=0   12 SECTORS/TRACK.                                                  1585
                    1587  *S=1 24 SECTORS/TRACK, 128 WORDS/SECTOR                                   1586
                    1588  *F=0   TEST FULL DISK.                                                    1587
                    1589  *F=1   TEST LESS THAN FULL DISK.                                          1588
                    1590  *                                                                         1589
                    1591  *R=0   DON'T TEST REMOVABLE DISK                                          1590
                    1592  *R=1   TEST REMOVABLE DISK                                                1591
                    1593  *X=0   DON'T TEST FIXED DISK                                              1592
                    1594  *X=1   TEST FIXED DISK                                                    1593
1A69 66             1595         DC    X'66'                                                       1594
1A6A 0000           1596  UNPAR  DC    **                                                          1595
1A6C 6AB2           1597         RTJ*  CRLF                                                        1596
1A6E 6AAA           1598         RTJ*  TTEX                                                        1597
1A70 C5CED4C5       1599         DC    C'ENTER DISK TEST INFORMATION'                              1598
1A74 D2A0C4C9
1A78 D3CBA0D4
1A7C C5D3D4A0
1A80 C9CEC6CF
1A84 D2C0DC1D4
1A88 C9CFCE
1A8B 00             1600         DC    H'0'                                                        1599
1A8C 6AC8           1601         RTJ*  ES.                                                         1600
1A8E 14D9           1602         JAN   UNPAR-1      DONE                                           1601
1A90 2801           1603         ALA   1            NO                                             1602
1A92 4C             1604         TAX                X =TUU                                         1603
1A93 2801           1605         ALA   1                                                           1604
1A95 D7C000         1606         ANA=  X'C000'                                                     1605
1A98 F027           1607         STA   UNIT                                                        1606
1A9A EF00           1608         LDV=  H'0'                                                        1607
1A9C 1501           1609         JXN   *+3                                                         1608
1A9E 4A             1610         DCA                FIXED HEAD                                     1609
1A9F F01B           1611         STA   TDSK                                                        1610
1AA1 6AC8           1612         RTJ*  ES.                FYSZ                                     1611
1AA3 2002           1613         LLA   2                                                           1612
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LOC  OBJECT      ER  STMT  LABEL   OP    OPERANDS                                  1613
1AA5 4C              1614          TAX                                             1613
1AA6 08              1615          K04                                             1614
1AA7 EF0200          1616          LDV=  512                                       1615
1AAA 000C            1617          DC    12                                        1616
1AAC 1D05            1618          NXN   *+7                                       1617
1AAE EF0100          1619          LDV=  256                                       1618
1AB1 0018            1620          DC    24                                        1619
1AB3 08              1621          K01                                             1620
1AB4 F021            1622          STA   SINSEC                                    1621
1AB6 2C01            1623          ARA   1                                         1622
1AB8 A021            1624          ADA   SINSEC                                    1623
1ABA F023            1625          STA   MULSEC                                    1624
1ABC 2210            1626          LLL   16                                        1625
1ABE F13A            1627          STA   NUMSEC                                    1626
1AC0 E041            1628          LDA   SW                                        1627
1AC2 2003            1629          LLA   3                                         1628
1AC4 4C              1630          TAX                                             1629
1AC5 E70198          1631          LDA=  408                                       1630
1AC8 1D02            1632          NXN   *+4                                       1631
1ACA 2301            1633          ALA   1                                         1632
1ACC F12F            1634          STA   NTK                                       1633
1ACE E018            1635          LDA   TDSK                                      1634
1AD0 1C27            1636          NAN   U51                                       1635
1AD2 6AB2            1637          RTJ*  CRLF                                      1636
1AD4 6AAA            1638          RTJ*  TTEX        FIXED HEAD                    1637
1AD6 D4D9D0C5        1639          DC    C'TYPE NUMBER OF HEADS  '                 1638
1ADA A0CED5CD
1ADE C2C5D2A0
1AE2 CFC6A0C8
1AE6 C5C1C4D3
1AEA A0A0
1AEC 00              1640          DC    H'0'                                      1639
1AED 6AC4            1641          RTJ*  HI.                                       1640
1AEF 112C            1642          JAZ   UER                                       1641
1AF1 4C              1643          TAX                                             1642
1AF2 D7FFE0          1644          ANA=  X'FFE0'          .= 16                    1643
1AF5 1926            1645          NAZ   UER                                       1644
1AF7 8904            1646          STX   NTK                                       1645
1AF9 870000          1647  U51     LDX=  0                                         1646
     1AFA            1648  NUMSEC  EQU   *-2                                       1647
1AFC E71AFC          1649          LDA=  *                                         1648
     1AFD            1650  NTK     EQU   *-2                                       1649
1AFF 6922            1651          RTJ   U6                                        1650
1B01 F01F            1652          STA   MRSC                                      1651
1B03 F01D            1653          STA   MTSC                                      1652
1B05 EF00            1654          LDV=  H'0'                                      1653
1B07 F025            1655          STA   FULL                                      1654
1B09 E041            1656          LDA   SW                                        1655
1B0B 1C02            1657          NAN   *+4                                       1656
1B0D 6927            1658          RTJ   U7                                        1657
1B0F 6AC8            1659          RTJ*  ES.                                       1658
1B11 2002            1660          LLA   2                                         1659
1B13 D7C000          1661          ANA=  X'C000'                                   1660
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS                          1661
1816 F029            1662         STA   DAISY                             1662
1818 861A6A          1663         LDX/  UNPAR                             1663
181B 6502            1664         JMP+  2                                 1664
181D 6AB4            1665  UER    RTJ*  TQQ                               1665
181F 661A6C          1666         JMP/  UNPAR+2                           1666
                     1667  * MAX SECTOR                                   1667
1822 66              1668         DC    X'66'                             1668
1823 0000            1669  U6     DC    **                                1669
1825 4F              1670         TXB                                     1670
1826 48              1671         DCB                                     1671
1827 49              1672         INB                                     1672
1828 F104            1673         STA   *+6                               1673
182A 49              1674         INB                                     1674
182B 12F5            1675         JBZ   U6-1                              1675
182D A70000          1676         ADA=  0                                 1676
1830 61F8            1677         JMP   *-6                               1677
1832 6AB4            1678  U73    RTJ*  TQQ                               1678
1834 6102            1679         JMP   U7+2                              1679
1836 0000            1680  U7     DC    **                                1680
1838 6AB2            1681         RTJ*  CRLF                              1681
183A 6AAA            1682         RTJ*  TTEX                              1682
183C D4D9D0C5        1683         DC    C'TYPE MAX CYLINDER  '            1683
1840 A0CDC1D8
1844 A0C3D9CC
1848 C9CEC4C5
184C D2A0A0
184F 00              1684         DC    H'0'                              1684
1850 6AC4            1685         RTJ*  HI.                               1685
1852 F01D            1686         STA   MISC                              1686
1854 801B            1687         LDX   TDSK                              1687
1856 1B0C            1688         NXZ   U74                               1688
1858 11D8            1689         JAZ   U73                               1689
185A 2801            1690         ALA   1                                 1690
185C B19F            1691         SBA   NTK                               1691
185E 1CD2            1692         NAN   U73                               1692
1860 E01D            1693         LDA   MTSC                              1693
1862 2801            1694         ALA   1                                 1694
1864 8194            1695  U74    LDX   NUMSEC                           1695
1866 6988            1696         RTJ   U6                                1696
1868 F01D            1697         STA   MTSC                              1697
186A 801B            1698         LDX   TDSK                              1698
186C 1306            1699         JXZ   U72                               1699
186E E01F            1700         LDA   MRSC                              1700
1870 B01D            1701         SBA   MTSC                              1701
1872 14BE            1702         JAN   U73                               1702
1874 EFFF            1703  U72    LDV=  H'-1'                             1703
1876 F025            1704         STA   FULL                              1704
1878 63BC            1705         JMP*  U7                                1705
                     1706  *                                             1706
                     1707  * TYPE TEXT                                    1707
187A 64              1708         JMP-                                    1708
187B 0000            1709  ETEX   DC    **                                1709
187D 81FC            1710         LDX   ETEX                              1710
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LOC  OBJECT      ER  STMT  LABEL   OP    OPERANDS                    1710
187F EC              1711          LDV-                              1710
1880 44              1712          INX                               1711
1881 11F7            1713          JAZ   ETEX-1                     1712
1883 6A5B            1714          RTJ*  TO.                         1713
1885 61F8            1715          JMP   *-6                         1714
                     1716  * TYPE CRLF                              1715
1887 0000            1717  ECF     DC    **                          1716
1889 69F0            1718          RTJ   ETEX                        1717
188B 8D8A00          1719          DC    X'8D8A00'                   1718
188E 63F7            1720          JMP*  ECF                         1719
                     1721  * TYPE                                   1720
1890 0000            1722  EQQ     DC    **                          1721
1892 69E7            1723          RTJ   ETEX                        1722
1894 BFBF            1724          DC    C'  '                       1723
1896 00              1725          DC    H'0'                        1724
1897 63F7            1726          JMP*  EQQ                         1725
1899 0000            1727  EDIS    DC    **                          1726
189B 6AB2            1728          RTJ*  CRLF                        1727
189D 6AAA            1729          RTJ*  TTEX                        1728
189F C4C9D3C1        1730          DC    C'DISABLE'                  1729
18A3 C2CCC5
18A6 00              1731          DC    H'0'                        1730
18A7 691F            1732          RTJ   FRSW                        1731
18A9 6AB2            1733          RTJ*  CRLF                        1732
18AB 00              1734          HLT                               1733
18AC 63EB            1735          JMP*  EDIS                        1734
18AE 0000            1736  EENA    DC    **                          1735
18B0 6905            1737          RTJ   ETNA1                       1736
18B2 6AB2            1738          RTJ*  CRLF                        1737
18B4 00              1739          HLT                               1738
18B5 63F7            1740          JMP*  EENA                        1739
18B7 0000            1741  ETNA1   DC    **                          1740
18B9 6AB2            1742          RTJ*  CRLF                        1741
18BB 6AAA            1743          RTJ*  TTEX                        1742
18BD C5CEC1C2        1744          DC    C'ENABLE'                   1743
18C1 CCC5
18C3 00              1745          DC    H'0'                        1744
18C4 6902            1746          RTJ   FRSW                        1745
18C6 63EF            1747          JMP*  ETNA1                       1746
18C8 0000            1748  FRSW    DC    **                          1747
18CA 6AAA            1749          RTJ*  TTEX                        1748
18CC A0C6C6D2        1750          DC    C' FORMAT SWITCH'           1749
18D0 CDC1D4A0
18D4 D3D7C9D4
18D8 C3C8
18DA 00              1751          DC    H'0'                        1750
18DB 63EB            1752          JMP*  FRSW                        1751
18DD 870000          1753          LDX=  0                           1752
18E0 E70000          1754          LDA=  0                           1753
18E3 66              1755          DC    X'66'                       1754
18E4 0000            1756  EDAT    DC    **                          1755
18E6 08              1757          R01                               1756
18E7 F1F8            1758          STA   EDAT-3                      1757
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS
1BE9 89F3            1759         STX   EDAT-6                1758
1BEB 02              1760         ESW                         1759
1BEC 2801            1761         ALA   1                     1760
1BEE 14F0            1762         JAN   EDAT-4                1761
1BF0 6AAA            1763         RTJ*  TTEX                  1762
1BF2 A0D7CFD2        1764         DC    C' WORD '             1763
1BF6 C4A0
1BF8 00              1765         DC    H'0'                  1764
1BF9 E1E3            1766         LDA   EDAT-6                1765
1BFB B72340          1767         SBA=  BF2                   1766
1BFE 6AB6            1768         RTJ*  TYPWD                 1767
1C00 6AAA            1769         RTJ*  TTEX                  1768
1C02 A0C4C1D4        1770         DC    C' DATA '             1769
1C06 C1A0
1C08 00              1771         DC    H'0'                  1770
1C09 6AB8            1772         RTJ*  TSB                   1771
1C0B E3D4            1773         LDA*  EDAT-3                1772
1C0D 6AB6            1774         RTJ*  TYPWD                 1773
1C0F 6ABA            1775         RTJ*  TIS                   1774
1C11 E3CB            1776         LDA*  EDAT-6                1775
1C13 6AB6            1777         RTJ*  TYPWD                 1776
1C15 6AB2            1778         RTJ*  CRLF                  1777
1C17 61C4            1779         JMP   EDAT-7                1778
                     1780  *                                  1779
1C19 0000            1781  ETDD   DC    **                    1780
1C1B 02              1782         ESW                         1781
1C1C 2801            1783         ALA   1                     1782
1C1E 1404            1784         JAN   *+6                   1783
1C20 6AB0            1785         RTJ*  TCI                   1784
1C22 6ABC            1786         RTJ*  TTAB                  1785
1C24 63F3            1787         JMP*  ETDD                  1786
                     1788  *                                  1787
1C26 66              1789         DC    X'66'                 1788
1C27 0000            1790  ECB    DC    **                    1789
1C29 F119            1791         STA   STOR1                 1790
1C2B 08              1792         RO1                         1791
1C2C EF00            1793         LDV=  H'0'                  1792
1C2E F90E            1794         STV   STOR1-6               1793
1C30 02              1795         ESW                         1794
1C31 2801            1796         ALA   1                     1795
1C33 14F1            1797         JAN   ECB-1                 1796
1C35 6AAA            1798         RTJ*  TTEX                  1797
1C37 C3C5D2A0        1799         DC    C'CER  '              1798
1C3B A0
1C3C 00              1800         DC    H'0'                  1799
1C3D EF00            1801         LDV=  H'0'                  1800
1C3F 1909            1802         NAZ   STOR1+6               1801
1C41 6AB8            1803         RTJ*  TSB                   1802
1C43 E70000          1804         LDA=  0                     1803
     1C44            1805  STOR1  EQU   *-2                   1804
1C46 6AB6            1806         RTJ*  TYPWD                 1805
1C48 6ABA            1807         RTJ*  TIS                   1806
1C4A 6A47            1808         RTJ*  RDSTAT                1807
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
1C4C 6AB6            1809         RTJ*   TYPWD                    1808
1C4E 6AB2            1810         RTJ*   CRLF                     1809
1C50 63D5            1811         JMP*   ECB                      1810
                     1812  *                                       1811
1C52 0000            1813  ECI    DC     **                       1812
1C54 E1FC            1814         LDA    ECI                      1813
1C56 F1CF            1815         STA    ECB                      1814
1C58 08              1816         RG1                             1815
1C59 EFFF            1817         LDV=   H'-1'                    1816
1C5B 61D1            1818         JMP    ECB+7                    1817
                     1819  *                                       1818
1C5D 0000            1820  ETSB   DC     **                       1819
1C5F 6AAA            1821         RTJ*   TTEX                     1820
1C61 D3C2A0A0        1822         DC     C'SB  '                  1821
1C65 00              1823         DC     H'0'                     1822
1C66 63F5            1824         JMP*   ETSB                     1823
                     1825  *                                       1824
1C68 0000            1826  ETIS   DC     **                       1825
1C6A 6AAA            1827         RTJ*   TTEX                     1826
1C6C A0C9D3A0        1828         DC     C' IS '                  1827
1C70 00              1829         DC     H'0'                     1828
1C71 63F5            1830         JMP*   ETIS                     1829
                     1831  * BAR SB ---- IS ----                   1830
1C73 66              1832         DC     X'66'                    1831
1C74 0000            1833  ETB    DC     **                       1832
1C76 02              1834         ESW                             1833
1C77 2801            1835         ALA    1                        1834
1C79 14FB            1836         JAN    ETB-1                    1835
1C7B 6AAA            1837         RTJ*   TTEX                     1836
1C7D C2C1D2A0        1838         DC     C'BAR  '                 1837
1C81 A0
1C82 00              1839         DC     H'0'                     1838
1C83 6AB8            1840         RTJ*   TSB                      1839
1C85 E015            1841         LDA    SECTOR                   1840
1C87 A02F            1842         ADA    DAVAL                    1841
1C89 6AB6            1843         RTJ*   TYPWD                    1842
1C8B 6ABA            1844         RTJ*   TIS                      1843
1C8D 6A49            1845         RTJ*   RDBAR                    1844
1C8F 6AB6            1846         RTJ*   TYPWD                    1845
1C91 6AB2            1847         RTJ*   CRLF                     1846
1C93 63DF            1848         JMP*   ETB                      1847
                     1849  *                                       1848
1C95 0000            1850  SRI    DC     **                       1849
1C97 E1FC            1851         LDA    SRI                      1850
1C99 F105            1852         STA    SRB                      1851
1C9B EFFF            1853         LDV=   H'-1'                    1852
1C9D 6107            1854         JMP    SRB+6                    1853
1C9F 66              1855         DC     X'66'                    1854
1CA0 0000            1856  SRB    DC     **                       1855
1CA2 F118            1857         STA    SR2+1                    1856
1CA4 EF00            1858         LDV=   H'0'                     1857
1CA6 F90E            1859         STV    SR1+1                    1858
1CA8 02              1860         ESW                             1859
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS
1CA9 2801            1861         ALA   1                                1860
1CAB 14F2            1862         JAN   SRB-1                            1861
1CAD 6AAA            1863         RTJ*  TTEX                             1862
1CAF D3D3D2A0        1864         DC    C'SSR '                          1863
1CB3 A0
1CB4 00              1865         DC    H'0'                             1864
1CB5 EF00            1866  SR1    LDV=  H'0'                             1865
1CB7 1909            1867         NAZ   SR3                              1866
1CB9 6AB8            1868         RTJ*  TSB                              1867
1CBB E70000          1869  SR2    LDA=  0                                1868
1CBE 6AB6            1870         RTJ*  TYPWD                            1869
1CC0 6ABA            1871         RTJ*  TIS                              1870
1CC2 6A55            1872  SR3    RTJ*  RSSR                             1871
1CC4 6AB6            1873         RTJ*  TYPWD                            1872
1CC6 6AB2            1874         RTJ*  CRLF                             1873
1CC8 63D6            1875         JMP*  SRB                              1874
                     1876  * READ HEX                                    1875
1CCA 2A10            1877         ALL   16                               1876
1CCC 66              1878         DC    X'66'                            1877
1CCD 0000            1879  HXI    DC    **                               1878
1CCF 2620            1880         LRL   32                               1879
1CD1 6A59            1881         RTJ*  TI.                              1880
1CD3 BFB0            1882         SBV=  C'0'                             1881
1CD5 14F3            1883         JAN   HXI-3                            1882
1CD7 BF0A            1884         SBV=  X'A'                             1883
1CD9 1C07            1885         NAN   HI1+5                            1884
1CDB AF0A            1886         ADV=  X'A'                             1885
1CDD 2904            1887  HI1    ALB   4                                1886
1CDF 42              1888         ORB                                    1887
1CE0 61EF            1889         JMP   HXI+4                            1888
1CE2 BF07            1890         SBV=  X'7'                             1889
1CE4 14E4            1891         JAN   HXI-3                            1890
1CE6 BF06            1892         SBV=  X'6'                             1891
1CE8 1CE0            1893         NAN   HXI-3                            1892
1CEA AF10            1894         ADV=  X'10'                            1893
1CEC 61EF            1895         JMP   HI1                              1894
                     1896  * TYPE 2 HEX                                  1895
1CEE 0000            1897  HXO    DC    **                               1896
1CF0 81FC            1898         LDX   HXO                              1897
1CF2 891A            1899         STX   EWD                              1898
1CF4 870002          1900         LDX=  F'2'                             1899
1CF7 2608            1901         LRL   8                                1900
1CF9 611A            1902         JMP   EWD+7                            1901
1CFB 0000            1903  OCT    DC    **                               1902
1CFD 81F6            1904         LDX   HXO+7                            1903
1CFF 2606            1905         LRL   6                                1904
1D01 DF07            1906         ANV=  X'7'                             1905
1D03 AFB0            1907         ADV=  C'0'                             1906
1D05 6A58            1908         RTJ*  TO.                              1907
1D07 2203            1909         LLL   3                                1908
1D09 45              1910         DCX                                    1909
1D0A 1DF5            1911         NXN   *-9                              1910
1D0C 63ED            1912         JMP*  OCT                              1911
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
                     1913  * TYPE 4 HEX                                    1912
1D0E 0000            1914  EWD    DC     **                               1913
1D10 870004          1915         LDX=   4                                1914
1D13 2610            1916         LRL    16                               1915
1D15 EF00            1917         LDV=   X'0'                             1916
1D17 2A04            1918         ALL    4                                1917
1D19 BF0A            1919         SBV=   X'A'                             1918
1D1B 1402            1920         JAN    *+4                              1919
1D1D AF07            1921         ADV=   X'7'                             1920
1D1F AF8A            1922         ADV=   X'BA'                            1921
1D21 6A58            1923         RTJ*   TO.                              1922
1D23 45              1924         DCX                                     1923
1D24 1BEF            1925         NXZ    EWD+7                            1924
1D26 63E6            1926         JMP*   EWD                              1925
                     1927  *                                               1926
1D28 6AB2            1928  EE2    RTJ*   CRLF                             1927
1D2A 66              1929         DC     X'66'                            1928
1D2B 0000            1930  EERR   DC     **                               1929
1D2D 08              1931         ROI                                     1930
1D2E F035            1932         STA    ERNUM                            1931
1D30 EFFF            1933         LDV=   H'-1'                            1932
1D32 F031            1934         STA    EFG                              1933
1D34 02              1935         ESW                                     1934
1D35 2801            1936         ALA    1                                1935
1D37 14F1            1937         JAN    EERR-1                           1936
1D39 6AB2            1938         RTJ*   CRLF                             1937
1D3B 6AAA            1939         RTJ*   TTEX                             1938
1D3D C5D2D2CF        1940         DC     C'ERROR  '                       1939
1D41 D2A0A0
1D44 00              1941         DC     H'0'                             1940
1D45 E035            1942         LDA    ERNUM                            1941
1D47 69B2            1943         RTJ    OCT                              1942
1D49 E035            1944         LDA    ERNUM                            1943
1D4B B70005          1945         SBA=   F'5'                             1944
1D4E 14D8            1946         JAN    EE2                              1945
1D50 E035            1947         LDA    ERNUM                            1946
1D52 B70087          1948         SBA=   X'0087'                          1947
1D55 1CD1            1949         NAN    EE2                              1948
1D57 6AAA            1950         RTJ*   TTEX                             1949
1D59 A0CFCEA0        1951         DC     C' ON '                          1950
1D5D 00              1952         DC     H'0'                             1951
1D5E 6ACA            1953         RTJ*   TPD                              1952
1D60 61C6            1954         JMP    EE2                              1953
1D62 0000            1955  ETP    DC     **                               1954
1D64 E027            1956         LDA    UNIT                             1955
1D66 2002            1957         LLA    2                                1956
1D68 08              1958         ROI                                     1957
1D69 AF80            1959         ADV=   C'0'                             1958
1D6B F907            1960         STV    EE3                              1959
1D6D 6AAA            1961         RTJ*   TTEX                             1960
1D6F D5CEC9D4        1962         DC     C'UNIT '                         1961
1D73 A0
1D74 0000            1963  EE3    DC     0                                1962
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS                                  1963
1D76 E018            1964        LDA   TDSK                                      1963
1D78 1900            1965        NAZ   EE4-2                                     1964
1D7A E02F            1966        LDA   DAVAL                                     1965
1D7C 1908            1967        NAZ   EE4                                       1966
1D7E 6AAA            1968        RTJ*  TTEX                                      1967
1D80 ADC6C9D8        1969        DC    C'-FIXED'                                 1968
1D84 C5C4
1D86 00              1970        DC    H'0'                                      1969
1D87 63D9            1971        JMP*  ETP                                       1970
1D89 6AAA            1972  EE4   RTJ*  TTEX                                      1971
1D8B ADD2C5CD        1973        DC    C'-REMOVABLE'                             1972
1D8F CFD6C1C2
1D93 CCC5
1D95 00              1974        DC    H'0'                                      1973
1D96 63CA            1975        JMP*  ETP                                       1974
                     1976  *                                                     1975
1D98 66              1977        DC    X'66'                                     1976
1D99 0000            1978  EHP   DC    **                                        1977
1D9B 08              1979        RO1                                             1978
1D9C E031            1980        LDA   EFG                                       1979
1D9E 1123            1981        JAZ   EH1                                       1980
1DA0 EF00            1982        LDV=  H'0'                                      1981
1DA2 F031            1983        STA   EFG                                       1982
1DA4 7033            1984        IWM   EF1                                       1983
1DA6 E033            1985        LDA   EF1                                       1984
1DA8 19EE            1986        NAZ   EHP-1                                     1985
1DAA EFFF            1987        LDV=  H'-1'                                     1986
1DAC F033            1988        STA   EF1                                       1987
1DAE 02              1989        ESW                                             1988
1DAF 2802            1990        ALA   2                                         1989
1DB1 1401            1991        JAN   EH2                                       1990
1DB3 00              1992        HLT                                             1991
1DB4 02              1993  EH2   ESW                                             1992
1DB5 2803            1994        ALA   3                                         1993
1DB7 14DF            1995        JAN   EHP-1                                     1994
1DB9 71DE            1996        IWM   EHP                                       1995
1DBB 71DC            1997        IWM   EHP                                       1996
1DBD EFF9            1998        LDV=  H'-7'                                     1997
1DBF F033            1999        STA   EF1                                       1998
1DC1 63D6            2000        JMP*  EHP                                       1999
1DC3 EFF9            2001  EH1   LDV=  H'-7'                                     2000
1DC5 F033            2002        STA   EF1                                       2001
1DC7 61EB            2003        JMP   EH2                                       2002
                     2004  * ILLEGAL TRAP                                        2003
                     2005  *810 ENTRY                                            2004
1DC9 0000            2006  ILTRP DC    **                                        2005
1DCB 04              2007        DIN                                             2006
1DCC 6955            2008        RTJ   ISV              SAVE REG                 2007
1DCE 02              2009        ESW                                             2008
1DCF 2801            2010        ALA   1                                         2009
1DD1 1423            2011        JAN   ILL                                       2010
1DD3 6AAA            2012        RTJ*  TTEX                                      2011
1DD5 C9CCCCC5        2013        DC    C'ILLEGAL TRAP FROM ADDRESS '             2012
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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
1DD9 C7C1CCA0
1DDD D4D2C1D0
1DE1 A0C6D2CF
1DE5 CDA0C1C4
1DE9 C4D2C5D3
1DED D3A0
1DEF 00              2014         DC    H'0'                          2013
1DF0 E1D7            2015         LDA   ILTRP                         2014
1DF2 6AB6            2016         RTJ*  TYPWD                         2015
1DF4 6A62            2017         RTJ*  CRLF                          2016
1DF6 EFFF            2018  IL1    LDV=  H'-1'                         2017
1DF8 F031            2019         STA   EFG                           2018
1DFA 48              2020         INA                                 2019
1DFB F035            2021         STA   ERNUM                         2020
1DFD 6A96            2022         RTJ*  HLTLP                         2021
1DFF 34              2023         NOP                                 2022
1E00 34              2024         NOP                                 2023
1E01 6935            2025         RTJ   IRR          RESTORE REG      2024
1E03 05              2026         EIN                                 2025
1E04 63C3            2027         JMP*  ILTRP                         2026
                     2028  *820 ENTRY                                 2027
1E06 04              2029  I82    DIN                                 2028
1E07 08              2030         R01                                 2029
1E08 808C            2031         LDX   X'8C'                         2030
1E0A EC              2032         LDV-                                2031
1E0B F936            2033         STV   IRR+11.                       2032
1E0D 09              2034         R02                                 2033
1E0E 46              2035         AWX                                 2034
1E0F E4              2036         LDA-                                2035
1E10 F1B7            2037         STA   ILTRP                         2036
1E12 46              2038         AWX                                 2037
1E13 E4              2039         LDA-                                2038
1E14 F12B            2040         STA   IRR+9                         2039
1E16 46              2041         AWX                                 2040
1E17 E4              2042         LDA-                                2041
1E18 F125            2043         STA   IRR+7                         2042
1E1A 46              2044         AWX                                 2043
1E1B E4              2045         LDA-                                2044
1E1C F11D            2046         STA   IRR+3                         2045
1E1E 888C            2047         STX   X'8C'                         2046
1E20 08              2048         R01                                 2047
1E21 61AB            2049         JMP   ILTRP+5                       2048
                     2050  * SAVE REG                                 2049
1E23 0000            2051  ISV    DC    **                            2050
1E25 8914            2052         STX   IRR+3                         2051
1E27 870007          2053         LDX=  7                             2052
1E2A 46              2054         AWX                                 2053
1E2B 1802            2055         NOV   *+4                           2054
1E2D 08              2056         R04                                 2055
1E2E 46              2057         AWX                                 2056
1E2F 08              2058         R04                                 2057
1E30 F90D            2059         STV   IRR+7                         2058
1E32 08              2060         R01                                 2059
```

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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
1E33 4E              2061         TXA
1E34 F90D            2062         STV    IRR+11
1E36 63EB            2063         JMP*   ISV
                     2064  * RESTORE REG
1E38 0000            2065  IRR    DC     **
1E3A 670000          2066         LDX=   0
1E3D 08              2067         R04
1E3E EF00000000      2068         LDV=   X'00000000'
1E43 00              2069         DC     H'0'
1E44 63F2            2070         JMP*   IRR
1E46 0000            2071  PWF    DC     **
1E48 04              2072         DIN
1E49 6908            2073         RTJ    ISV
1E4B 00              2074         HLT
1E4C 0000            2075  PWS    DC     **
1E4E 69E6            2076         RTJ    IRR
1E50 661002          2077         JMP/   EXEC+2
                     2078  *
1E53 0000            2079  EXWR   DC     **
1E55 6A53            2080         RTJ*   IWCCA
1E57 6A4F            2081         RTJ*   LDWR
1E59 63F8            2082         JMP*   EXWR
                     2083  *
1E5B 0000            2084  EXRD   DC     **
1E5D 6A53            2085         RTJ*   IWCCA
1E5F 6A4D            2086         RTJ*   LDRD
1E61 63F6            2087         JMP*   EXRD
                     2088  *
1E63 0000            2089  ESCAD  DC     **
1E65 F108            2090         STA    **+13
1E67 E015            2091         LDA    SECTOR
1E69 F017            2092         STA    SECTOR+2
1E6B E019            2093         LDA    BLOCKS
1E6D A015            2094         ADA    SECTOR
1E6F F015            2095         STA    SECTOR
1E71 E70000          2096         LDA=   0
1E74 63ED            2097         JMP*   ESCAD
                     2098  * MOVE
                     2099  * CALL  RTJ* M.
                     2100  *       DC     FROM
                     2101  *       DC     TO
                     2102  *       DC     = BYTES
1E76 08              2103         P01
1E77 66              2104         DC     X'66'
1E78 0000            2105  MOV    DC     **
1E7A 61FC            2106         LDX    MOV
1E7C 09              2107         R02
1E7D E4              2108         LDA-
1E7E F10E            2109         STA    MV1+1
1E80 46              2110         AWX
1E81 E4              2111         LDA-
1E82 F10D            2112         STA    MV2+1
1E84 46              2113         AWX
```

```
LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS
1E85 E4              2114         LDA-
1E86 46              2115         AWX
1E87 89EF            2116         STX    MOV
1E89 4C              2117         TAX
1E8A 08              2118         ROI
1E8B 13E9            2119         JXZ    MOV-2
1E8D EE0000          2120  MV1    LDV/   **
1E90 FE0000          2121  MV2    STV/   **
1E93 71F9            2122         IWM    MV1+1
1E95 71FA            2123         IWM    MV2+1
1E97 45              2124         DCX
1E98 61F1            2125         JMP    MV1-2
                     2126  *
1E9A 0000            2127  EM12   DC     **
1E9C E011            2128         LDA    WCCA
1E9E 2801            2129         ALA    1
1EA0 F106            2130         STA    *+8
1EA2 6AC0            2131         RTJ*   M.
1EA4 2040            2132         DC     BF1
1EA6 2340            2133         DC     BF2
1EA8 0000            2134         DC     0
1EAA E7DB6D          2135         LDA=   X'DB6D'
1EAD F3E2            2136         STA*   MV2+1
1EAF 63E9            2137         JMP*   EM12
                     2138  *
1EB1 0000            2139  EL21   DC     **
1EB3 8011            2140         LDX    WCCA
1EB5 4F              2141         TXB
1EB6 48              2142         DCB
1EB7 49              2143         INB
1EB8 872340          2144         LDX=   BF2
1EBB E76DB6          2145         LDA=   X'6DB6'
1EBE F4              2146         STA-
1EBF 44              2147         INX
1EC0 44              2148         INX
1EC1 49              2149         INB
1EC2 1AFA            2150         NBZ    *-4
1EC4 2801            2151         ALA    1
1EC6 48              2152         INA
1EC7 F4              2153         STA-
1EC8 63E7            2154         JMP*   EL21
                     2155  * ENTER SWITCHES
1ECA 0000            2156  ESP    DC     **
1ECC 6AB2            2157         RTJ*   CRLF
1ECE 00              2158         HLT
1ECF 02              2159         ESW
1ED0 F041            2160         STA    SW
1ED2 240C            2161         LKA    12
1ED4 08              2162         ROI
1ED5 DF0F            2163         ANV=   X'F'
1ED7 BF0A            2164         SBV=   X'A'
1ED9 1402            2165         JAN    *+4
1EDB AF07            2166         ADV=   X'7'
```

```
LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS                    2166
1EDD AFBA           2167         ADV=  X'BA'                       2166
1EDF 6A5B           2168         RTJ*  10.                         2167
1EE1 E041           2169         LDA   SW                          2168
1EE3 63E5           2170         JMP*  ESP                         2169
                    2171  * I/O SUBROUTINES                        2170
                    2172  * DISK                                   2171
                    2173  *                                        2172
                    2174  *READ STATUS                             2173
                    2175  * 166.46 USEC                            2174
1EE5 0000           2176  ERT    DC    **                          2175
1EE7 6928           2177         RTJ   ERG                         2176
1EE9 3120           2178         IBA   1,0                         2177
1EEB 63F8           2179         JMP*  ERT                         2178
                    2180  * SKIP ON NOT DONE                       2179
                    2181  * 200 USEC                               2180
1EED 0000           2182  ESKDN  DC    **                          2181
1EEF 69F4           2183         RTJ   ERT                         2182
1EF1 F10A           2184         STA   *+12                        2183
1EF3 D70001         2185         ANA=  X'0001'                     2184
1EF6 1904           2186         NAZ   *+6                         2185
1EF8 71F3           2187         IWM   ESKDN                       2186
1EFA 71F1           2188         IWM   ESKDN                       2187
1EFC E70000         2189         LDA=  0                           2188
1EFF 63EC           2190         JMP*  ESKDN                       2189
                    2191  * READ SEEK STATUS                       2190
                    2192  * 166.46 USEC                            2191
1F01 0000           2193  ERS    DC    **                          2192
1F03 690C           2194         RTJ   ERG                         2193
1F05 3140           2195         IBA   2,0                         2194
1F07 63F8           2196         JMP*  ERS                         2195
                    2197  *READ BLOCK ADDRESS                      2196
1F09 0000           2198  ERB    DC    **                          2197
1F0B 6904           2199         RTJ   ERG                         2198
1F0D 3160           2200         IBA   3,0                         2199
1F0F 63F8           2201         JMP*  ERB                         2200
                    2202  * READ REGISTER                          2201
                    2203  * 137.2 USEC                             2202
1F11 0000           2204  ERG    DC    **                          2203
1F13 E3FC           2205         LDA*  ERG                         2204
1F15 A02D           2206         ADA   ADDRES                      2205
1F17 F105           2207         STA   *+7                         2206
1F19 D7FF1F         2208         ANA=  X'FF1F'                     2207
1F1C F104           2209         STA   *+5                         2208
1F1E 0000           2210         DC    0                           2209
1F20 2308           2211         ALA   8                           2210
1F22 0000           2212         DC    0                           2211
1F24 71EB           2213         IWM   ERG                         2212
1F26 71E9           2214         IWM   ERG                         2213
1F28 63E7           2215         JMP*  ERG                         2214
                    2216  * LOAD CONTROL REGISTER                  2215
1F2A 0000           2217  ELCON  DC    **                          2216
1F2C 693E           2218         RTJ   EIO                         2217
1F2E 3920           2219         OBA   1,0                         2218
```

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LOC  OBJECT     ER  STMT  LABEL  OP    OPERANDS
1F30 63F8           2220         JMP*  ELCON                    2219
                    2221  * CLEAR STATUS                        2220
1F32 0000           2222  ELST   DC    **                       2221
1F34 69AF           2223         RTJ   ERT                      2222
1F36 D7007E         2224         ANA=  X'007E'                  2223
1F39 69EF           2225         RTJ   ELCON                    2224
1F3B 63F5           2226         JMP*  ELST                     2225
                    2227  *LOAD SEEK ADDRESS                    2226
1F3D 0000           2228  EOLS   DC    **                       2227
1F3F 68EA           2229         RTJ   SCV                      2228
1F41 A027           2230         ADA   UNIT                     2229
1F43 693C           2231         RTJ   ELG                      2230
1F45 3940           2232         OBA   2,0                      2231
1F47 63F4           2233         JMP*  EOLS                     2232
                    2234  * LOAD WORD COUNT/CURRENT ADDRESS     2233
1F49 0000           2235  EIWC   DC    **                       2234
1F4B E70011         2236         LDA=  WCCA                     2235
1F4E 6931           2237         RTJ   ELG                      2236
1F50 3960           2238         OBA   3,0                      2237
1F52 63F5           2239         JMP*  EIWC                     2238
                    2240  * LOAD BAR & READ                     2239
1F54 0000           2241  ELR    DC    **                       2240
1F56 E02F           2242         LDA   DAVAL                    2241
1F58 A015           2243         ADA   SECTOR                   2242
1F5A 6925           2244         RTJ   ELG                      2243
1F5C 3980           2245         OBA   4,0                      2244
1F5E 63F4           2246         JMP*  ELR                      2245
                    2247  * LOAD BAR & WRITE                    2246
1F60 0000           2248  ELW    DC    **                       2247
1F62 E02F           2249         LDA   DAVAL                    2248
1F64 A015           2250         ADA   SECTOR                   2249
1F66 6919           2251         RTJ   ELG                      2250
1F68 39A0           2252         OBA   5,0                      2251
1F6A 63F4           2253         JMP*  ELW                      2252
                    2254  * DISK IOT - INTERRUPT & CLEAR        2253
1F6C 0000           2255  EIO    DC    **                       2254
1F6E F70000         2256         STA=  0                        2255
1F71 E3F9           2257         LDA*  EIO                      2256
1F73 71F7           2258         IWM   EIO                      2257
1F75 71F5           2259         IWM   EIO                      2258
1F77 A02D           2260         ADA   ADDRESS                  2259
1F79 F102           2261         STA   *+4                      2260
1F7B E1F2           2262         LDA   EIO+3                    2261
1F7D 0000           2263         DC    0                        2262
1F7F 63EB           2264         JMP*  EIO                      2263
                    2265  * LOAD REGISTER                       2264
1F81 0000           2266  ELG    DC    **                       2265
1F83 08             2267         R01                            2266
1F84 F116           2268         STA   EG1                      2267
1F86 E02D           2269         LDA   ADDRESS                  2268
1F88 F905           2270         STV   *+7                      2269
1F8A A3F5           2271         ADA*  ELG                      2270
1F8C F905           2272         STV   *+7
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LOC  OBJECT      ER  STMT  LABEL  OP     OPERANDS                                  2272
1F8E 3B001F9D        2273         OBM    0,0,EG1+1 LOAD GBR                        2273
1F92 3B001F9C        2274         OBM    0,0,EG1                                   2274
1F96 71E9            2275         IWM    ELG                                       2275
1F98 71E7            2276         IWM    ELG                                       2276
1F9A 63E5            2277         JMP*   ELG                                       2277
1F9C 0000            2278  EG1    DC     0                                         2278
                     2279  *                                                        2279
                     2280  * TTY                                                    2280
                     2281  *                                                        2281
1F9E 0000            2282  TIN    DC     **                                        2282
1FA0 3000            2283         IBS    0,0          OR  RTJ   PIN                2283
1FA2 D7007F          2284         ANA=   X'007F'                                   2284
1FA5 A70080          2285         ADA=   X'0080'                                   2285
1FA8 F103            2286         STA    *+5          ECHO                         2286
1FAA 6A5B            2287         RTJ*   TO.                                       2287
1FAC E70000          2288         LDA=   0                                         2288
1FAF 63ED            2289         JMP*   TIN                                       2289
1FB1 0000            2290  PIN    DC     **                                        2290
1FB3 3120            2291         IBA    1,0                                       2291
1FB5 DF02            2292         ANV=   X'2'                                      2292
1FB7 11FA            2293         JAZ    *-4                                       2293
1FB9 3100            2294         IBA    0,0                                       2294
1FBB 63F4            2295         JMP*   PIN                                       2295
1FBD 0000            2296  TOT    DC     **                                        2296
1FBF 3800            2297         OBS    0,0                                       2297
1FC1 63FA            2298         JMP*   TOT                                       2298
1FC3 0000            2299  POT    DC     **                                        2299
1FC5 F107            2300         STA    *+9                                       2300
1FC7 3120            2301         IBA    1,0                                       2301
1FC9 DF04            2302         ANV=   X'4'                                      2302
1FCB 11FA            2303         JAZ    *-4                                       2303
1FCD E70000          2304         LDA=   0                                         2304
1FD0 3900            2305         OBA    0,0                                       2305
1FD2 63EF            2306         JMP*   POT                                       2306
2000                 2307         ORG    DDAT                                      2307
2000 34              2308         NOP                                              2308
2001 34              2309         NOP                                              2309
2002 34              2310         NOP                                              2310
                     2311  *      ESW    IF SW 1=1, USE PARALLEL TTY               2311
                     2312  *      ALA    3                                         2312
                     2313  *      NAN    IZ1                                       2313
2003 E7690F          2314         LDA=   X'690F'                                   2314
2006 F61FA0          2315         STA/   TIN+2                                     2315
2009 E71FC3          2316         LDA=   POT                                       2316
200C F05B            2317         STA    TO.                                       2317
                     2318  *820 INITIALIZE                                         2318
200E 2510            2319         LRB    16                                        2319
2010 E08C            2320         LDA    X'8C'                                     2320
2012 908C            2321         DC     X'908C'                                   2321
2014 110F            2322         JAZ    IZ1          811                          2322
2016 1E0D            2323         NAB    IZ1          810                          2323
2018 E71E06          2324         LDA=   I82                820                    2324
201B F0C2            2325         STA    IT.                                       2325
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LOC  OBJECT      ER  STMT  LABEL  OP    OPERANDS
2010 F082            2326         STA   X'82'          2325
201F F086            2327         STA   X'86'          2326
2021 F08A            2328         STA   X'8A'          2327
2023 F08E            2329         STA   X'8E'          2328
2025 E0CC            2330  IZ1    LDA   EX.            2329
2027 F003            2331         STA   X'03'          2330
2029 6000            2332         JMP   X'0'           2331
202B 0000            2333         END   0              2332
```

MICRO 810 CROSS ASSEMBLER CROSS REFERENCE LISTING

04/10/75 PAGE 001

SYMBOL	DEFN	REFERENCES																	
ADDRES	0040	0330	0395	0612	1519	2206	2260	2269											
AD.	0116	0174																	
BDATST	1201	0116	1213	1223	1232														
BF1	0009	0010	0973	1117	1119	1164	1340	1392	2132										
BF2	0010	0024	0874	0975	1023	1767	2133	2144											
BLOCKS	0027	0901	0960	1054	1156	1319	1359	1372	2093										
CLR2	0085	1102	1165	1352															
CLSTAT	0052	0610	1030																
CRLF	0092	0152	0792	0796	1514	1530	1597	1637	1681	1728	1733	1738	1742	1778	1810	1847	1874	1928	1936
		2017	2157																
CT.	0108	0128																	
CTST	0202	0108	0235																
C1	0222	0228																	
C2	0205	0211	0220																
C3	0212	0217	0229																
C4	0229	0234																	
DAISY	0036	0148	0178	1662															
DATA1	0016	0903	0905	0907	0911	0912	0937	0938	0956	0967	1027	1045	1047	1048	1050	1052	1072	1074	1075
		1097	1144	1149	1151	1153	1154	1297	1298	1299	1302	1305	1310	1312	1347				
DAVAL	0041	0146	0176	0181	0185	0958	1488	1842	1966	2242	2249								
DDAT	0003	0009	0014	0131	1496	2307													
DK1	1340	1333	1358	1360	1365														
DK2	1381	1322	1325	1328	1338	1341	1343	1355	1370	1377	1378								
DK3	1347	1334	1354	1366	1369														
DK4	1357	1363																	
DK5	1338	1379																	
DK6	1362	1356	1361																
DRW	1291	1203	1237	1247	1257	1270	1294	1307	1315	1330	1380								
ECB	1790	0098	1797	1811	1815	1818													
ECF	1717	0092	1720																
ECI	1813	0091	1814																
EDAT	1756	0079	1758	1759	1762	1766	1773	1776	1779										
EDIS	1727	0086	1735																
EENA	1736	0087	1740																
EERR	1930	0077	1937																
EE2	1928	1946	1949	1954															
EE3	1963	1960																	
EE4	1972	1965	1967																
EFG	0042	1489	1934	1980	1983	2019													
EF1	0043	1491	1984	1985	1988	1999	2002												
EG1	2278	2268	2273	2274															
EHP	1978	0078	1986	1995	1996	1997	2000												
EH1	2001	1981																	
EH2	1993	1991	2003																
EID	2255	0062	2213	2257	2258	2259	2262	2264											
EINC	2235	0060	2239																
ELCON	2217	0056	2220	2225															
ELG	2206	2231	2237	2244	2251	2271	2275	2276	2277										
ELR	2241	0057	2246																
ELST	2222	0052	2226																
ELW	2248	0058	2255																
EL21	2139	0085	2154																
EM12	2127	0084	2137																
EOLS	2228	0059	2233																
EOS1	0021																		
EQQ	1722	0093	1726																

SYMBOL	DEFN	REFERENCES										
ERB	2198	0055	2201									
ERG	2204	2177	2194	2199	2205	2213	2214	2215				
ERNUM	0044	1932	1942	1944	1947	2021						
ERS	2193	0061	2196									
ERT	2176	0054	2179	2183	2223							
ES.	0103	1546	1601	1612	1659							
ESCAD	2089	0081	2097									
ESKUN	2182	0053	2187	2188	2190							
ESP	2156	0103	2170									
ETB	1833	0097	1836	1848								
ETDD	1781	0080	1787									
ETEX	1709	0068	1710	1713	1718	1723						
ETIS	1826	0096	1830									
ETNAL	1741	1556	1737	1747								
ETP	1955	0104	1971	1975								
ETSB	1820	0095	1824									
EWD	1914	0094	1899	1902	1925	1926						
EX.	0106	2330										
EXEC	0007	0106	0125	0199	2077							
EXRD	2084	0083	2087									
EXWR	2079	0082	2082									
EX1	0150	0141	0147									
EX3	0190	0134	0189									
EX4	0199	0193										
EX5	0183	0177	0180									
E21	0136	0132	0182	0186	0187	0188	0191					
F.	0118	0721	0734	0755	0786							
FGY	0046	0729	1536	1552								
FR.	0112	0163										
FRSW	1748	1732	1746	1752								
FTST	0720	0112	0790									
FULL	0034	1655	1704									
F11	0931	0869	0889	0891	0897	0914	0925	0926	0927	0928		
F13	0919	0920	0929									
F15	0866	0118	0884	0885	0886	0887	0890	0893	0894	0906	0908	0909	0930
F3	0792	0731										
F4	0764	0761										
F5	0807	0746	0769	0777	0811	0837	0843					
F5A	0747	0738										
F51	0821	0819	0825	0833	0834							
F52	0850	0832										
F53	0837	0859										
F54	0841	0830	0853									
F55	0845	0856										
F7	0786	0767										
GRN	1188	1176	1189	1193	1196	1197	1198					
HI.	0101	1518	1641	1685								
HII	1887	1885	1895									
HLTLP	0078	0270	0319	0363	0429	0462	0575	0657	0846	0948	2022	
HO.	0102											
HXI	1879	0101	1883	1889	1891	1893						
HXO	1897	0102	1898	1904								
ILTRP	2006	0067	0068	0069	0070	0071	0100	2015	2027	2037	2049	
ILI	2018	2011										
IN.	0109	0129										
IOLS	0059	0439	0623									

SYMBOL	DEFN	REFERENCES
IRR	2065	2025 2033 2040 2043 2046 2052 2059 2062 2070 2076
ISV	2051	2008 2063 2073
IT.	0100	1523 2325
ITST	0328	0109 0365
ITO	0335	0364
IT1	0353	0337
IT2	0357	0334 0336 0352
INCCA	0060	0488 2080 2085
IZ1	2330	2322 2323
I02	2029	2324
LA.	0111	0155
LAITST	0405	0111 0520
LDCON	0056	0206 0223 0343 0345 0361 0491 0507 0518 0815 0918 1058 1160 1337
LDRD	0057	0534 0740 2086
LDWR	0058	0539 0749 0771 0779 2081
LPFORM	0047	0161 0170 0196 1535 1555
L2	0447	0442 0444 0445 0453 0456
L22	0423	0430
L3	0429	0425
L31	0438	0463
L32	0452	0446 0458
L34	0462	0455 0470
L4	0607	0494 0645 0650 0656 0669 0690
L4A	0495	0465 0472 0480 0510
L4B	0691	0676
L41	0124	0421 0424 0436 0437 0440 0528 0627 0639 0642 0643 0654
L42	0660	0609 0611 0618 0619 0621 0622 0629 0630 0631 0634 0638 0641 0666 0667 0679 0687 0689 0693 0701
L43	0624	0613 0616 0632
L44	0666	0644
L45	0635	0614 0617 0668
L46	0656	0683 0715
L47	0684	0640
L48	0670	0697 0707 0717
L5	0549	0120 0533 0538 0551 0558 0569 0570 0571 0576 0577 0578 0579 0597 0598
L5.	0120	
L50	0562	0553 0567
L51	0566	0556 0565
L52	0580	0564
L53	0569	0586 0596
L54	0575	0599
L6	0530	0519 0543
L7	0523	0454 0529
M.	0099	0135 1500 2131
MD.	0117	0175
MDST	1235	0117 1279
MD2	1274	1268
MOV	2105	0099 2106 2116 2119
MRSC	0031	0153 1652 1700
MSEC	0039	0138 0154 0157 0464 0479 0493 0509 0531 0732 0760 0913 1112 1145 1179 1368 1503
MTSC	0030	0156 1653 1686 1693 1697 1701
MULSEC	0033	1222 1236 1246 1625
MV1	2120	2109 2122 2125
MV2	2121	2112 2123 2136
M12	0034	1100 1350
NEXT	0176	0149

SYMBOL	DEFN	REFERENCES														
NTK	1650	1634	1646	1691												
NUMSEC	1648	1627	1695													
OCT	1903	1912	1943													
PA.	0107	0127														
PARAM	1486	0107	1512	1572												
PASS1	0046	0160	0169	0192	0195	1493										
PATGEN	1385	1314	1399	1407												
PG1	1405	1391	1394	1396	1398	1404	1466									
PG3	1408	1393	1395	1397	1413	1418	1428	1431	1433	1438	1441	1443	1448	1449	1450	1451
PG5	1452	1410	1415	1420	1425	1430	1435	1440	1445	1459	1476	1478	1481	1483		
PG6	1421	1436	1446													
PIN	2290	2295														
PORTS	0045	0133	1513													
POT	2299	2306	2316													
PR1	1508	1495	1507	1510												
PR2	1502	1497	1504	1505	1506											
PR3	1498	1509														
PWF	2071	0073														
P.S	2075	0074														
P21	1510	1499														
P22	1514															
P41	1454	1412	1417	1422	1427	1432	1437	1442	1447	1465	1469	1470	1471	1472		
P42	1473	1411	1474													
P43	1475	1421	1423	1479												
P44	1480	1426	1484													
RANTST	1170	0115	1186													
RA1	1184	1172	1183													
RA3	1176	1185														
RDBAR	0055	0385	0962	1645												
RDSTAT	0054	0207	0213	0224	0230	0580	0710	0851	1808							
READ	0083	1071	1148	1214	1224	1248	1258	1271								
RESET	0062	0300	0339	0433	0560	0945										
RGRES	0291	0212	0293	0297	0304	0308	0315									
RGTRT	0245	0205	0222	0247	0256	0266	0383									
RN.	0115	0173														
RR1	0323	0292														
RR2	0302	0298														
RR3	0315	0309														
RSSR	0061	0423	0435	0446	0527	0590	1872									
RT1	0276	0246	0251	0252	0257	0258	0264	0274	0282							
RT2	0277	0248	0249	0284												
RT3	0267	0259														
RT4	0265	0261														
RT5	0283	0279														
RW	0936	0119	0947													
RW.	0119	0919	1103	1166	1353											
RW0	0947	0954	0966	0968	0988	0991										
RW1	0978	0974	0980	0981	0984	1001	1009	1010	1012							
RW2	0952	0940														
RW3	1026	0944	1031	1034												
RW4	0956	0952														
RW6	0992	0979														
RW7	0985	1008	1025													
RW8	1004	0993	0995	1000	1013	1014										
RW9	0967	0955	0957	0963												
R11	1016	0999	1015													

```
SYMBOL  DEFN  REFERENCES
R12     1001  1017
R13     0998  1020
R31     1032  0965  0990  0997  1037
SA.     0114  0172
SABTST  1126  0114  1141
SADD    0081  1033  1105  1106  1107  1357
SCV     0121  0123  0150  2229
SECTOR  0025  0432  0552  0810  0900  0921  0922  0924  0959  1035  1036  1084  1089  1093  1111  1163  1178  1181  1342
              1367  1641  2091  2092  2094  2095  2243  2250
SFT     0049  0766  1537  1549
SINSEC  0032  0142  1202  1212  1256  1266  1269  1332  1622  1624
SKPDON  0053  0563  0831  0939
SRB     1856  0090  1852  1854  1862  1875
SRI     1850  0089  1851
SR1     1866  1859
SR2     1869  1857
SR3     1872  1867
STORI   1805  1791  1794  1802
SW      0050  1628  1656  2160  2169
S1      1142  1129  1132  1134  1136  1137  1138  1139  1147
S2      1143  1131  1161  1175
S3      1162  1133  1135  1168  1182
S5      1132  1140
TADD    0080  1029
TCI     0091  0351  0573  0681  1785
TCNB    0093  0209  0215  0226  0232  0842
TDAT    0079  1002
TDIS    0086  0198  0768
TDSK    0029  0137  0138  0140  0158  0704  1501  1503  1611  1635  1687  1698  1964
TENA    0087  0785
TERR    0077  0263  0313  0350  0427  0450  0460  0572  0653  0678  0840  1028
TI.     0063  1881
TIN     2282  0063  2289  2315
TIS     0096  1775  1807  1844  1871
TO.     0064  1714  1908  1923  2168  2287  2317
TOT     2296  0064  2298
TPD     0104  0151  1953
TQQ     0093  1665  1678
TSB     0095  1772  1803  1840  1868
TSI     0089  0428  0451  0461  0574  0682
TSRB    0090  0655
TTAB    0097  0387  1786
TTEX    0083  0793  1515  1531  1557  1598  1638  1682  1729  1743  1749  1763  1769  1798  1821  1827  1837  1863  1939
              1950  1961  1968  1972  2012
TYPWD   0094  1768  1774  1777  1806  1809  1843  1846  1870  1873  2016
UER     1665  1642  1645
UNIT    0035  0411  0489  0501  0516  0587  0684  0812  0915  1056  1158  1335  1607  1956  2230
UNPAR   1596  1498  1602  1663  1666
U51     1647  1636
U6      1669  1651  1675  1696
U7      1680  1658  1679  1705
U72     1703  1699
U73     1678  1689  1692  1702
U74     1695  1688
WC.     0110  0130
WCCA    0023  0371  0384  0487  0898  0969  1021  1055  1157  1293  2128  2140  2236
```

SYMBOL	DEFN	REFERENCES						
WR.	0113	0165	0725	0762				
WRITE	0082	0902	1051	1096	1204	1238	1348	
WTST	0369	0110	0381					
WT2	0382	0374	0376	0378	0380	0389	0390	
WT3	0392	0370	0394	0403				
W11	1042	0113	1044	1060	1068	1077		
W12	1078	1063	1066	1116	1118	1122		
W13	1079	1070	1076	1095				
W15	1096	1085	1090	1094	1114			
W16	1097	1104	1113					
W17	1121	1081	1082	1087	1108	1109	1110	1125
W18	1115	1080	1086	1091	1120	1123	1124	

ERRATA SHEET

Refer to the section in the manual concerning line voltage selection. This information is on Page 1 of Appendix A.

This paragraph should be changed to read:

"The A.C. power comes into the controller through the combination AC cord /fuse holder/voltage select assembly. This assembly, on the rear panel of the controller, provides a safety interlock mechanism when changing fuses or the line voltage selector card between 115 volt and 230 volt operation.

In order to change from 115 volt to 230 volt operation, or vice-versa, remove the A.C. cord from the assembly and slide the clear plastic cover to the left, thereby exposing the fuse assembly. Remove the fuse by pulling on the fuse removal lever, then remove the voltage selector card. Reinsert the card with the correct line voltage as stamped on the card visible to you. Insert the appropriate fuse for the selected voltage into the fuse holder. Slide the plastic cover back to the right over the fuse holder and replace the A.C. power cord."

APPENDIX A

OPERATING CHARACTERISTICS, UNPACKING AND INSTALLATION

Controller Switches and Indicators

The Model 3040 Disk Controller has two control switches on the rear panel. The power switch on the left side of the rear panel turns on the power to the controller. When power is on, the indicator light on the front panel will be lit. The switch on the right side of the rear panel is the format switch. When in the down or NORMAL position, it prevents the disk format information on the cartridge from being altered. However, when it is in the up or FORMAT position, writing of format information on the moving-head disk cartridges can take place, as can writing on the write-protected sectors.

The AC power comes into the controller through the combination AC cord/fuse holder/power switch assembly. This assembly on the rear panel of the controller provides a safety interlock mechanism when changing fuses and switching between 115-volt operation and 230-volt operation.

In order to switch from 115-volt operation to 230-volt operation, remove the AC cord from the assembly and slide the clear plastic cover to the left, thereby exposing the fuse assembly. Remove the fuse by pulling on the fuse removal lever and push the voltage switch from the 115-volt to the 230-volt position. Insert the appropriate fuse for 230-volt operation into the fuse holder. Slide the plastic cover back to the right over the fuse holder and replace the AC cord.

Switching from 230-volt operation to 115-volt operation is accomplished by a similar procedure.

Fixed-Head Drive Switches and Indicators

All controls and indicators for the fixed-head disk drive are on the front panel of the drive. The off-on push button power switch, which is located on the lower middle section of the front panel, lights up when the power is turned on.

If the drive is equipped with the write lock-out option, there will be a series of 16 switches in two rows of eight switches each in the upper left hand corner of the front panel. Each switch controls the writing of data for eight data tracks. The switches are numbered from 1 through 16. Switch 1 corresponds to the first eight data tracks on the disk (Track 0 through Track 7), and the remainder of the switches correspond to sets of eight tracks in ascending order. Switch 16 controls writing on Tracks 120-127.

When the Write Lock-Out switches are in the "down" position, the disk may be operated normally with no write protection in effect. When they are switched to the "up" position, any writing on those tracks corresponding to switches in the "up" position will be inhibited, and attempts to do so will result in setting the write lock-out error flag in the Status Register of the Controller.

The Moving-Head Drive

Control Switch (Load-Run Switch)

This two-position rocker type switch provides a means for starting and stopping the disk drive. Cartridges may be removed and inserted when the switch is in the LOAD position. With a cartridge inserted, switching to the RUN position starts the disk drive and brings it up to its normal operating speed in about 60 seconds. When the

switch is switched back to the LOAD position, the disk decelerates to a stop in about 15 seconds. After the disk stops, the cartridge receiver interlock releases and the cartridge can be removed.

NOTE: Switching to the LOAD position during a write operation may result in garbling the data. The operator must make sure that a write operation is not in progress when switching to LOAD.

Indicator Lights

Load

This white indicator light is on when the spindle is not rotating and tells the operator that cartridges can be loaded or unloaded. The light goes off whenever the load-run switch is set to the RUN position.

Ready

This yellow signal light (when on) indicates that the disk drive is ready to accept and execute seek, read, or write commands from the controller. The light comes on when the disk is rotating at its correct speed with its heads in position and no other conditions present that prevent those operations.

Check

This orange light (when on) indicates that the disk drive is not capable of writing due to low power. The light may be reset (to off) by setting the load-run switch to the LOAD position and then back to the RUN position.

Power

This red light (when on) indicates the presence of full power to the disk drives.

The 4090 Power Supply

Power for each moving-head disk drive is supplied by a 4090 Power Supply module. One or two of these modules can be mounted in a 4090 Power Supply enclosure which is a rack mountable cabinet of the same dimensions as the 3040 Controller. It has a power indicator light on the front panel and a power switch on the rear panel. The power switch turns the power on to both power supply moduhes when it is in the "up" position. The rear of the enclosure also contains the AC cord and fuse holder.

Operating Precautions

The following precautions and practices should be observed while operating the moving-head disk drives in order to obtain the best performance and longest life out of the equipment. No special precautions are necessary for the other components in the Model 3040 Disk Systems except when the enclosures are opened.

Keep the dust cover on the moving-head disk drive to prevent unnecessary entry of atmospheric dust.

A sustained audible tinging or scratching sound may be caused by a head in contact with the disk. The cartridge should be removed from the drive immediately to prevent further damage to the cartridge and/or read/write head.

The operator must not force or attempt to override the various protection interlocks in the moving-head disk drive. There are three such interlocks. The dust cover must be installed, the cartridge holding clamps must be closed, and the disk drive must be pushed fully into the rack.

Disk Cartridge Handling and Storage

The following practices should be observed when handling and storing disk cartridges. Refer to the manufacturer's instructions for more detailed maintenance and cleaning procedures.

Before use, the cartridge should be allowed to reach a stable temperature equilibrium.

The cartridge should be kept in the dust cover when it is out of the disk drive to prevent dust from getting on the disks.

Cartridges may be stored flat or on edge. Several can be stacked on top of one another, but avoid heavy top loading.

Operating Procedures and Installation of Cartridges

The following procedure should be followed when installing disk cartridges in moving-head disk drives:

- Make sure that the front panel LOAD light is on.
- Pull the disk drive forward on its slides and open the cartridge holding clamps.
- Push the sliding tab on the cartridge handle to the left and lift the cartridge handle, this lifts the cartridge out of its dust cover.
- Insert the cartridge on the spindle, making sure that the opening for the heads is to the rear. Lower the cartridge handle to lock it in place and place the dust cover, upside down, over the cartridge.
- Close the holding clamps, push the drive fully into the rack, and depress the load/run switch to RUN.

- If the READY light does not come on in about 60 seconds or the CHECK light comes on, consult the drive manufacturer's maintenance manual.

To remove a cartridge, the above procedure is reversed:

- Depress the load/run switch to LOAD. Wait for the spindle to stop rotating and the LOAD light to come on.
- Pull the disk drive forward on its slides and open the cartridge holding clamps.
- Remove the dust cover. Push the sliding tab on the cartridge handle to the left, and lift the cartridge handle to remove the cartridge from the spindle.
- Place the dust cover over the cartridge and lower the handle to lock the cover in place.

Unpacking and Installation

This section describes the procedures to be followed unpacking (or repacking) each component of a Model 3040 Disk System and the procedures for cabling the components of a system together and mounting those components in a standard 19-inch rack with 30 inches of depth. It is best to read through this section before unpacking the equipment or attempting to cable it together.

Be careful when opening the cases to avoid scratching the finished surfaces of the unit. Do not destroy the containers or the packing material since they are required for reshipment of the controller.

All exposed parts of the controller should be inspected for evidence of shipping damage. If any damage is detected, please notify the Manager of Customer Services at System Industries; also notify the transfer company.

After the components of a storage system are unpacked, it is recommended that they be arranged on a large bench or table, cabled up together and to the computer, and the diagnostic checkout performed before they are installed in the rack. That way, if a problem is detected, access to the components will be easier.

Unpacking Instructions

The controller is enclosed in a plastic bag and packed in a form-fitting cardboard box with a cardboard floater on the top and bottom to prevent the controller from moving inside (See Figure 2-1). When the controller is shipped with the computer or disk cables plugged in, some loose fill packing material is put in around the cables to prevent them from bouncing around during shipment. This box is packed inside a larger cardboard container with three inches of packing material on all sides. The rack slides and the AC power cord for the controller are taped to the top of the inner box for shipment.

Installing the Computer and Disk Interfaces

Generally, the controller will be shipped with the computer and disk interfaces (including the cables and connectors) plugged in. However, in some instances they are shipped in a separate container in the outer box containing the controller box. They may be plugged into the controller using the following procedures:

1. Remove the top from the controller enclosure. The top of the controller enclosure is removed by unscrewing the six screws - three in front and three in the rear - that secure it to the chassis and, lifting the front end first, raising it away from the controller. Figure 2-2 illustrates the location of the

printed circuit card cage and five-volt power supply that are contained inside.

2. Raise the card cage. The card cage assembly consists of a wire-wrapped back panel and twenty-one card slots to accept and interconnect the logic of the controller, the disk interfaces, and the computer interface. The long side of the card cage to which the wire wrapped back panel is attached is the back panel side, and the opposite side is the card opening side.

   Figure 2-3 specifies the printed circuit board location in the card cage (viewed from the card opening side) when the controller is interfaced to a Microdata computer. Card slots X1 through X4 are the disk ports corresponding to port numbers 0 through 3, respectively. An interface cable assembly for either a moving-head drive or a fixed-head drive may be plugged into any of these four card slots.

   In order to get access to the back panel connections or to remove printed circuit cards or interfaces, it is necessary to raise the card cage. Raise the back panel side of the card cage first by inserting the thumb and forefinger of each hand in the two pairs of holes on that side of the card cage, squeezing to release the card cage and pivoting the backpanel side of the card cage assembly up until the cantilever springs lock into place. In this tilted position, with the back panel side up and the card opening side down, access is provided to the pins of the printed circuit board connectors.

In order to gain access to the card openings, repeat the squeezing and pivoting process on the card opening side of the assembly until the entire card cage has clicked into the "up" position.

3. Remove the card clamp. The printed circuit cards are held securely in place by a card clamp attached to the center of the card opening side of the card cage. Lifting up the tab of the card clamp will disengage it for removal.

4. Remove the disk and computer cable clamps. Two clamps at the rear opening of the controller assembly secure the cables going to the disks and the computer. These clamps may be removed by unscrewing the two thumb screws that hold each down and by sliding forward on each clamp assembly until it is unhooked from the chassis. Note: Sometimes the plastic material on the bottom of the clamp will inhibit its sliding forward; lifting up slightly as you slide it forward will make removal easier.

5. Insert the CPU Interface. The Microdata interface to the 3040 Controller consists of two 5" x 7" printed circuit board assemblies, attached by a flat ribbon cable to an 8 1/2" x 12 1/2" printed circuit board assembly.

   Install the assembly by plugging the 3020-6004 board into the card slot X7 - the bottom card slot at the rear end of the card cage. Push the card into the connector until it clicks. When the equipment first arrives, the connectors will be a little tight, so it may require more force than normal in

order to plug the card into the connector. When fully inserted, the card should not extend beyond the card cage opening.

Next, insert interface card number 3020-6002 (components side up) into slot X5.

6. Dress and clamp the CPU Interface Cables. Carefully fold the two flat cables coming out of the computer interface cards one-half revolution clockwise and make a 90-degree bend so that the cable extends out the rear of the controller chassis over the cable clamp position furtherest from the card cage. Line up the mark on each interface cable with the inside edge of the cable tray in order to provide enough slack for movement of the card cage to its operating position without straining the cable or pulling on the interface board. Insert the cable clamp in the two slots on each side of the cable and slide it back until it is hooked securely in the cable tray. Notice that the round side of the cable clamp matches the curvatures of the rear of the cable tray. Tightening the two thumb screws of the cable will secure the computer interface cables.

7. Insert the disk drive interfaces. Insert the disk drive interfaces, with cables attached, into the appropriate ports (components side up). Make sure that they are fully plugged in so that the printed circuit boards do not extend out of the card cage.

   Holding all cables from the disk interfaces, stacked on top

of one another, straight out from the card cage, carefully turn the stack of cables one-half revolution counterclockwise so that the smooth side of the interface cable plugged into the lowest port will be on top. Then carefully route all cables at a 90-degree angle so that they come out the rear of the controller over the cable tray. Align the mark on the smooth side of the top cable with the inside edge of the card tray and align the marks on those cables underneath the top cable about three tenths of an inch inside one another in order to provide a little space between each cable.

Clamp the interface cables securely, using the same procedure as you used for clamping the computer cables.

8. Re-install the card clamp and lower the card cage. Re-install the card clamp to secure the printed circuit boards in the card cage by hooking the bottom of the clamp over the inside of the lower hem of the center section of the card cage and pushing on the top of the clamp until it is in a vertical position and the tab clicks in place over the center of the card cage.

   IMPORTANT: Make sure the cards are all the way into the connectors before installing the card clamp.

   Lower the card opening side of the card cage first by pressing inwardly on the cantilever springs that hold that side of the card cage in the "up" position. Be sure to hold on to the card cage assembly as you do this so that it can be pivoted gently into the tilted position and click into place. When the card opening side is down and latched, follow the same procedure to gently lower the back panel side of the card cage into place.

Check to see that the card cage is securely latched in the "down" position.

Replace the top of the enclosure, inserting the rear end first and then lowering the front end. Make sure that the air flow vents in the enclosure top are on the right side of the controller.

Rack Mounting the Controller

Rack mounting the controller requires two steps. The first is to attach the interior portion of the rack slides onto the sides of the controller. The three threaded holes on each side of the controller are used for that purpose. Make sure that the interior portion of each rack slide is mounted as in Figure 2-4 so that the spring tab end extends beyond the rear of the controller. This is necessary in order to make the controller entirely accessible in its extended position from the rack.

Next, mount the outside portions of the rack slide assembly in your rack, making sure that when the controller is inserted in the rack the outer portion of each slide will be matched with the inner part that came with it. The outer portions of the rack slides are mounted in the rack so that the permanent mounting ears are attached to the front mounting strips and the adjustable mounting brackets, which are assembled as shown in Figure 2-5, are attached to the rear mounting strips.

For EIA standard racks, the holes on the mounting strips are spaced in 1/2" and 5/8" increments. Attach the mounting ears on the rack slides using the upper pair of a set of the three holes spaced 5/8" apart. When attached in this fashion, the top and bottom of the controller front panel will line up midway between pairs of the holes spaced 1/2" apart. Attaching the rack

slides in any other fashion will result in gaps between the components of the system when they are rack mounted.

IMPORTANT: When sliding the controller into its rack slides or pulling it out of the rack, make sure that the cables to the disks and the computer do not slide over rough surfaces or get crimped or pinched in any way.

Repacking Instructions

When repacking the Model 3040 Controller and interfaces for reshipment, follow the instructions illustrated in Figure 2-1.

- Place the lower floater in the inner container.
- Pull the plastic bag over the controller and, after carefully holding the cables along the side of the controller, insert it in the inner container so that it matches the notches in the floater.
- Fill the area around the controller with loose fill material, place upper floater over the controller, and seal the inner box.
- Tape the rack slides, brackets, and AC cord to the top of the inner box.
- Fill the bottom of the outer container with at least 3" of loose fill packing material and place the inner box inside, being careful to center it.
- Place loose fill packing material all around and on top of the inner box so that there is at least 3" all around. Seal the outer container with tape for shipping.

Unpacking and Installing the Disk Drives

For information describing the unpacking and installation procedures for the drives used in the System Industries Model 3040 Disk Systems, refer to instructions provided by the disk drive manufacturer.

Unpacking and Installation Instructions for the 4091 Power Supply

This section describes the unpacking and installation instructions for the Model 4091 Power Supply Enclosure for the moving head disks.

Unpacking Instructions

The 4091 Power Supply Enclosure is enclosed in a plastic bag and packed in a form-fitting cardboard box.

The inner container is packed inside a larger cardboard container with three inches of loose fill packing material on all sides. The rack slides are taped to the top of the inner box for shipment.

Mounting the 4091 Power Supply Enclosure

The Model 4091 Power Supply Enclosure is rack mounted in exactly the same way as the 3040 Controller. Refer to Figure 2-6.

Repacking the Model 4091 Power Supply Enclosure

When repacking the Model 4091 Power Supply Enclosure for shipment, follow these instructions:

- Put three inches of loose fill packing material in the bottom of the outer container. Place the Power Supply Assembly with the rack slides removed inside a plastic bag and in the inner cardboard shipping container.

- Put the cardboard filler pad on top of the packed unit and seal the inner container.
- Place the inner container in the outer container and fill all around with three inches of loose fill packing material, making sure that three inches is on top of the inner container as well as around the sides.
- Seal the outer container with tape for shipping.

Cabling Instructions for Model 3040 Disk Systems

This section will describe procedures for cabling a Model 3040 Disk System and connecting it to a Microdata computer.

Cabling the Moving-Head Disk Drives

Two cable connections are required for each moving-head disk drive: an interface cable and a power cable. Connect a power cable from a Model 4090 Power Supply to the power connector - the right connector on the rear of the drive above the terminator. Next, the 50-pin connector on the end of the flat cable from the controller disk interface should be plugged into and screwed down to the input side of the moving-head disk drive, immediately to the left of the power connector.

A terminator board should be plugged into the output side of the disk drive, below the other two connectors.

Cabling the Fixed-Head Disk Drive

The power for the fixed-head disk drive is supplied through a standard AC cord coming out from the drive. The only cabling required is to attach the connector on the end of the fixed-head disk interface cable to the rear of the drive.

Connecting the Disk System to a Microdata Computer

The controller is connected to the CPU by installing the large interface board (3020-6006) into the next available I/O position in the computer.

Once the system has been cabled together it is ready for operation. Insert the AC power cord into the AC cord/fuse assembly on the rear of the 3040 Controller and plug in all of the system components. Turn on the power switches to the computer, the 3040 Controller, the 4090 Power Supply and/or the fixed-head disk. Then start up the disk system and run the system diagnositc to check its operation.

Installation of a Second Model 4090 Power Supply in a Model 4091 Power Supply Enclosure

The Model 4091 Power Supply Enclosure is designed to hold one or two Model 4090 Power Supply Modules. To install a second module into an existing single module system, pull the power supply enclosure forward on its slides, refer to Figures 2-6 and 2-7, and perform the following operations:

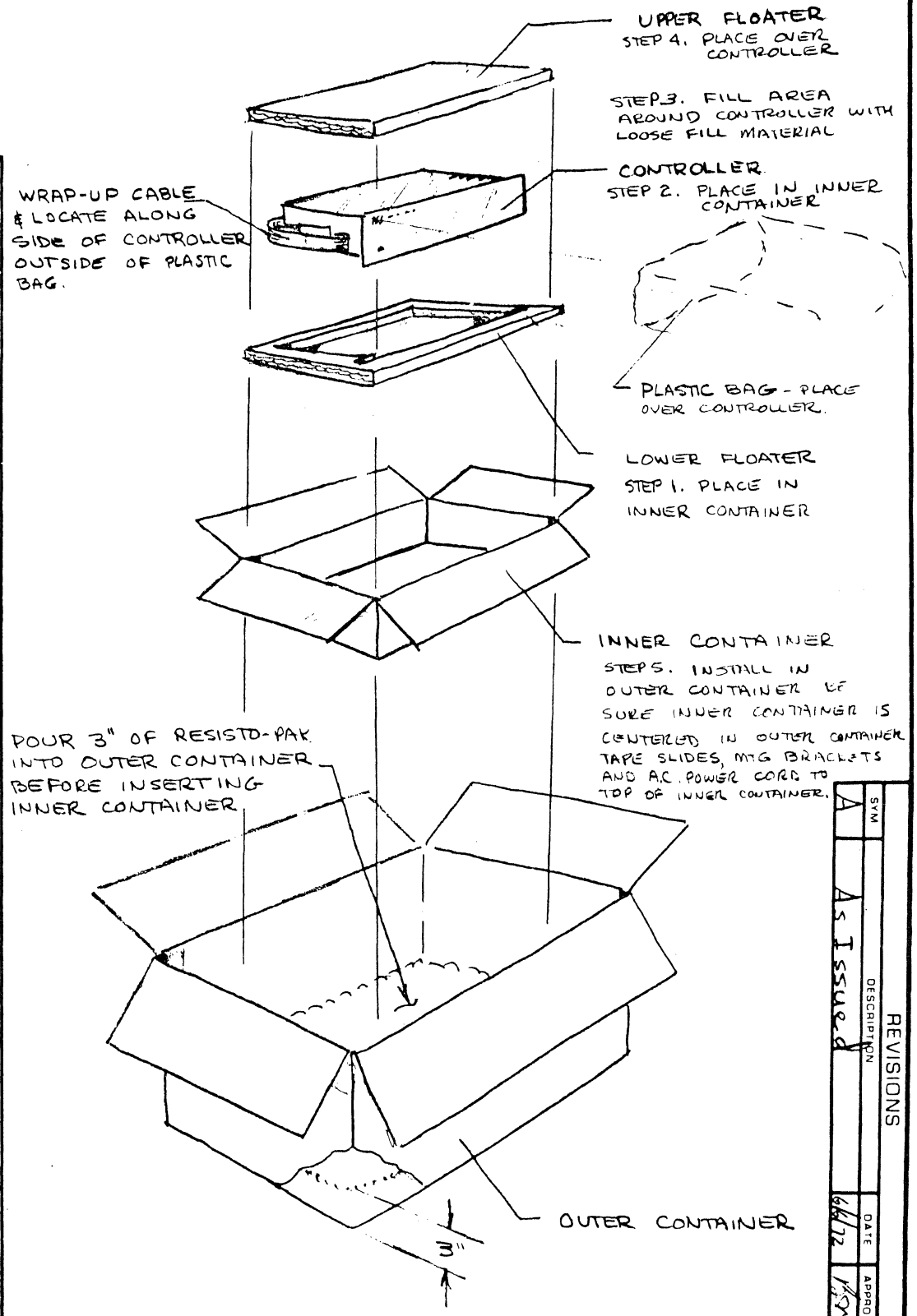
1. Set the second supply on its side across the midsection of the first (installed) supply with the top of the supply facing the front of the drawer, and the AC cord end resting above the vacant mounting space.

2. Coil the AC cord loosely in the bottom of the drawer and plug it into the remaining AC receptacle in the rear support bracket.

3. Lift the supply and lower it, AC cord end first, onto the front support bracket, guiding the cord through the slots in the front support bracket as the supply is moved forward.

4. Continue sliding the supply forward until it butts against the forward retaining bracket, then lower the fan end of the supply onto the rear support bracket.

5. Install the four hex-head screws provided, securing the supply to the front and rear retaining brackets.



DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES XX ± 02 XXX ± 005
ANGULAR ± 1°

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC

DRAWN BY: RDMichael — DATE: 11-5-71
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG

FINISH
SCALE

NEXT ASSEMBLY

System Industries
SUNNYVALE, CALIFORNIA

TITLE: C2 CONTROLLER PACKING INSTRUCTIONS

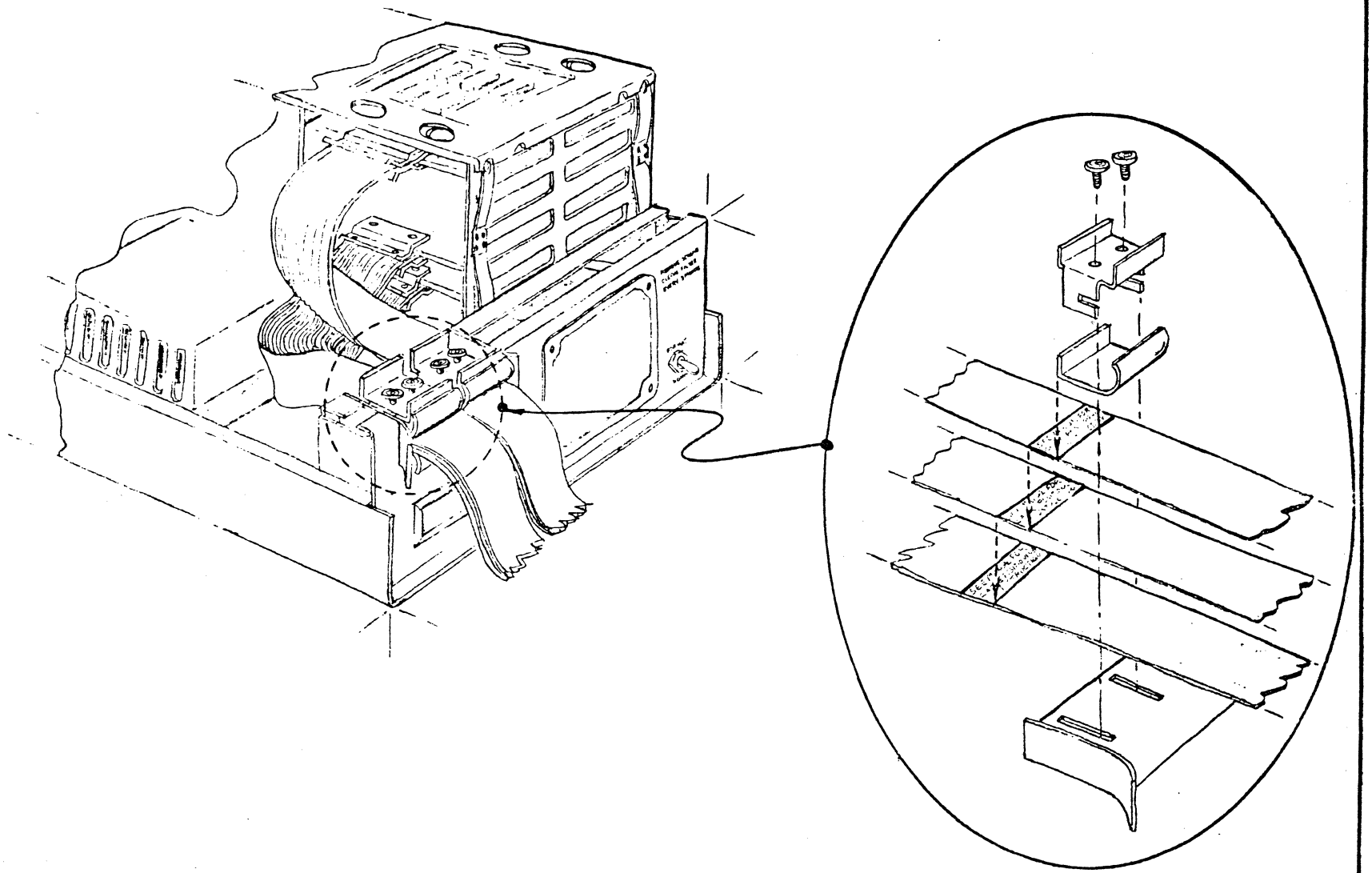
PART NUMBER: B-9901-9039-1

REVISIONS

SYM	DESCRIPTION	DATE	APPROVAL
A	As Issued	6/8/72	

FIG 2-1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	A: Issued	6/5/72	



DO NOT SCALE THIS DRAWING	ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .xx ± .02 .xxx ± .005 ANGULAR ± 1°	DRAWN BY: RDMICHELL	DATE: 12-9-71	System Industries SUNNYVALE CALIFORNIA		TITLE: CABLE EGRESS ~ CLAMPING SCHEME	
	ENGINEER					
	RELEASE TO PROD		NEXT ASSEMBLY		PART NUMBER	
	SUPERSEDES DWG		FINISH	SCALE	C-9901-9039-2	

SHEET OF

FIG 2-2

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	Revised 4-1-77	4-1-77	

Z	Y	X
3010-6008 F442	3010-6002 C232	*
3040-6007 C516	3010-6002 C232	*
3010-6006 D511	3010-6002 C232	*
3040-6005 B403	3010-6002 C232	*
3017-6008 F539	3015-6012 B416	3020-6002 A207
3010-6003 F429	3015-6011 C517	
		3020-6004 C507

*CABLE BOARD NUMBERS:

3041-6001 Moving-Head F525
3012-6002 Fixed-Head E441

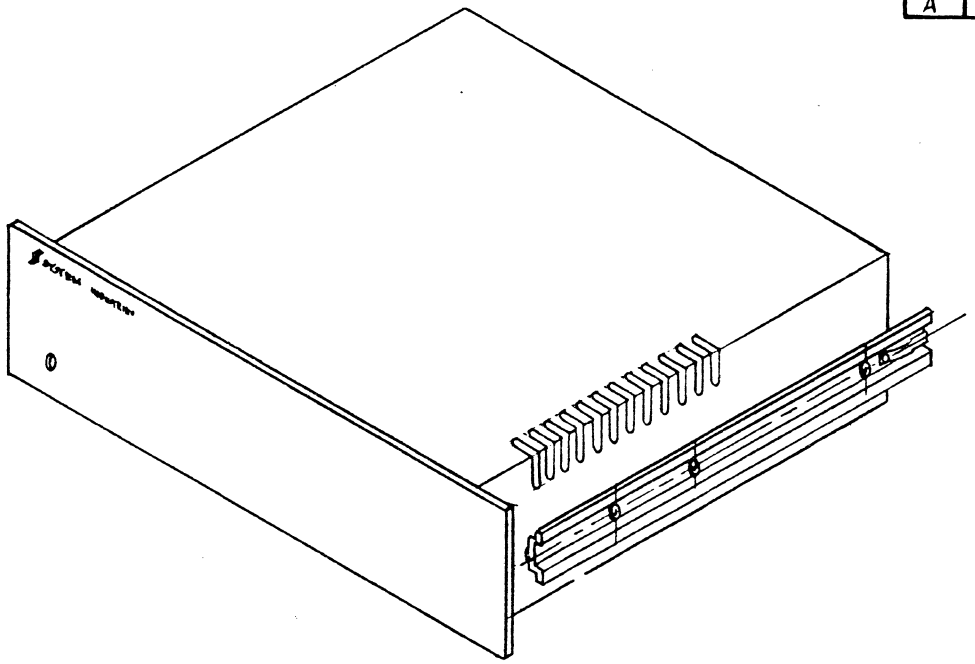
DO NOT SCALE THIS DRAWING	ITEM	QTY.	MATERIAL-DESCRIPTION	MATL. PART NO.	MATL. DWG. NO.	MATL. SPEC.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES xx ± 02 xxx ± 005 ANGULAR ± 1°	B. Holland DRAWN BY	3/26/75 DATE	System Industries SUNNYVALE, CALIFORNIA	P C BOARD LOCATION MICRODATA 3040 CONTROLLER TITLE
	ENGINEER			
	RELEASE TO PROD		FINAL NEXT ASSEMBLY	PART NUMBER
	SUPERSEDES DWG.		FINISH / SCALE	A-3050-9002-1

SHEET 1 OF 1

FIG. 2-3

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	As Issued	6/6/72	



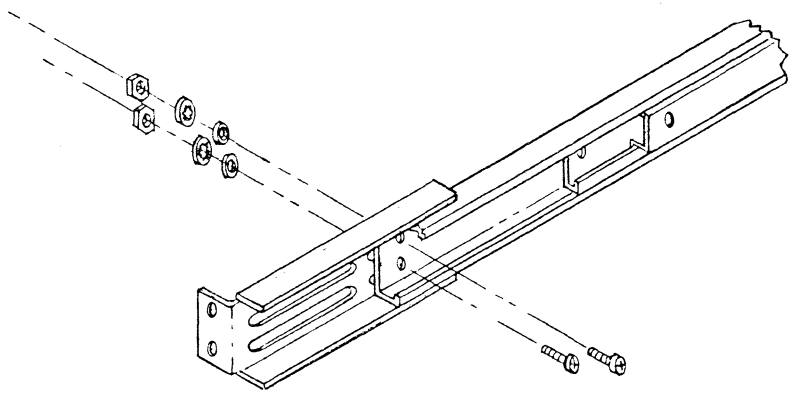
PROPER SLIDE MOUNTING

DO NOT SCALE THIS DRAWING	ITEM	QTY	MATERIAL-DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES xx ± .02 xxx ± .005 ANGULAR ± 1°	D. MATTHEWS DRAWN BY	12/22/71 DATE	System Industries SUNNYVALE, CALIFORNIA		SLIDE BAR MOUNTING INSTRUCTION TITLE	
	ENGINEER					
	RELEASE TO PROD		NEXT ASSEMBLY		PART NUMBER	
	SUPERSEDES DWG		FINISH	SCALE	B-9901-9039-3	

SHEET OF

FIG. 2-4

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	As Issued	6/7/72	[illegible]



NOTES:

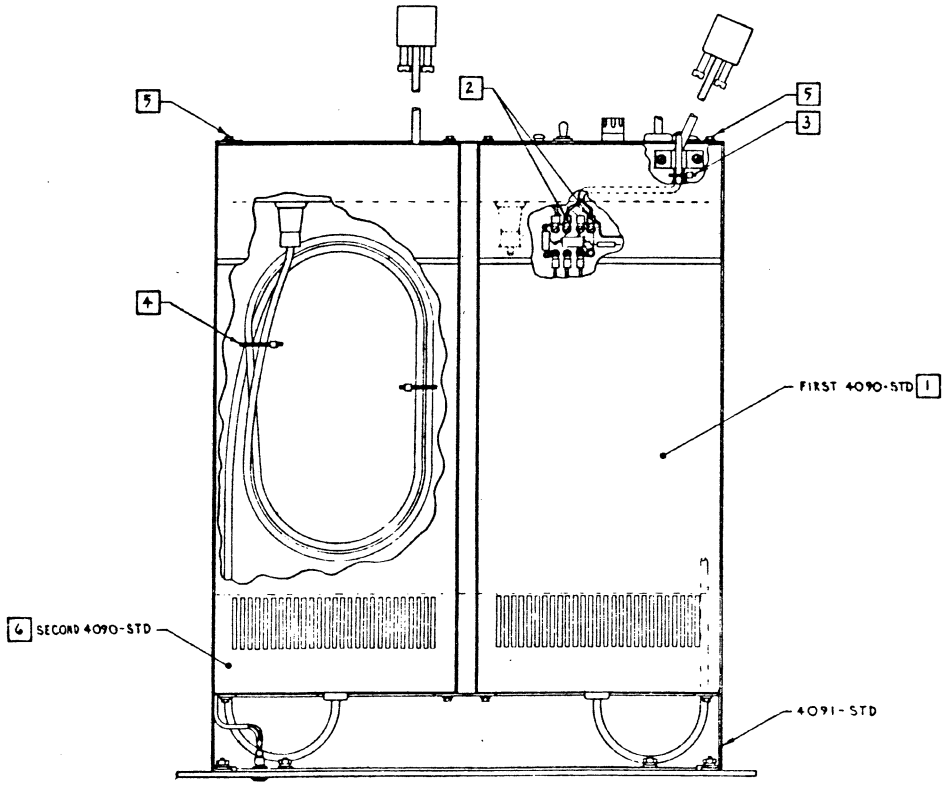
1. ASSEMBLY OF REAR MOUNTING BAR ON:
   3010 CONTROLLER SLIDES
   3090 POWER SUPPLY SLIDES

DO NOT SCALE THIS DRAWING	ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES XX ± 02 XXX ± 005 ANGULAR ± 1°	D. MATTHEWS DRAWN BY	12/22/71 DATE	System Industries SUNNYVALE, CALIFORNIA		SLIDE EXTENSION MOUNTING INSTRUCTION TITLE	
	ENGINEER					
	RELEASE TO PROD		NEXT ASSEMBLY		PART NUMBER	
	SUPERSEDES DWG		FINISH	SCALE	B-9901-9039-4	

SHEET OF

FIG. 2-5

REVISIONS			
SYM		DATE	APPROVED
A	AS ISSUED	8-28	BCS

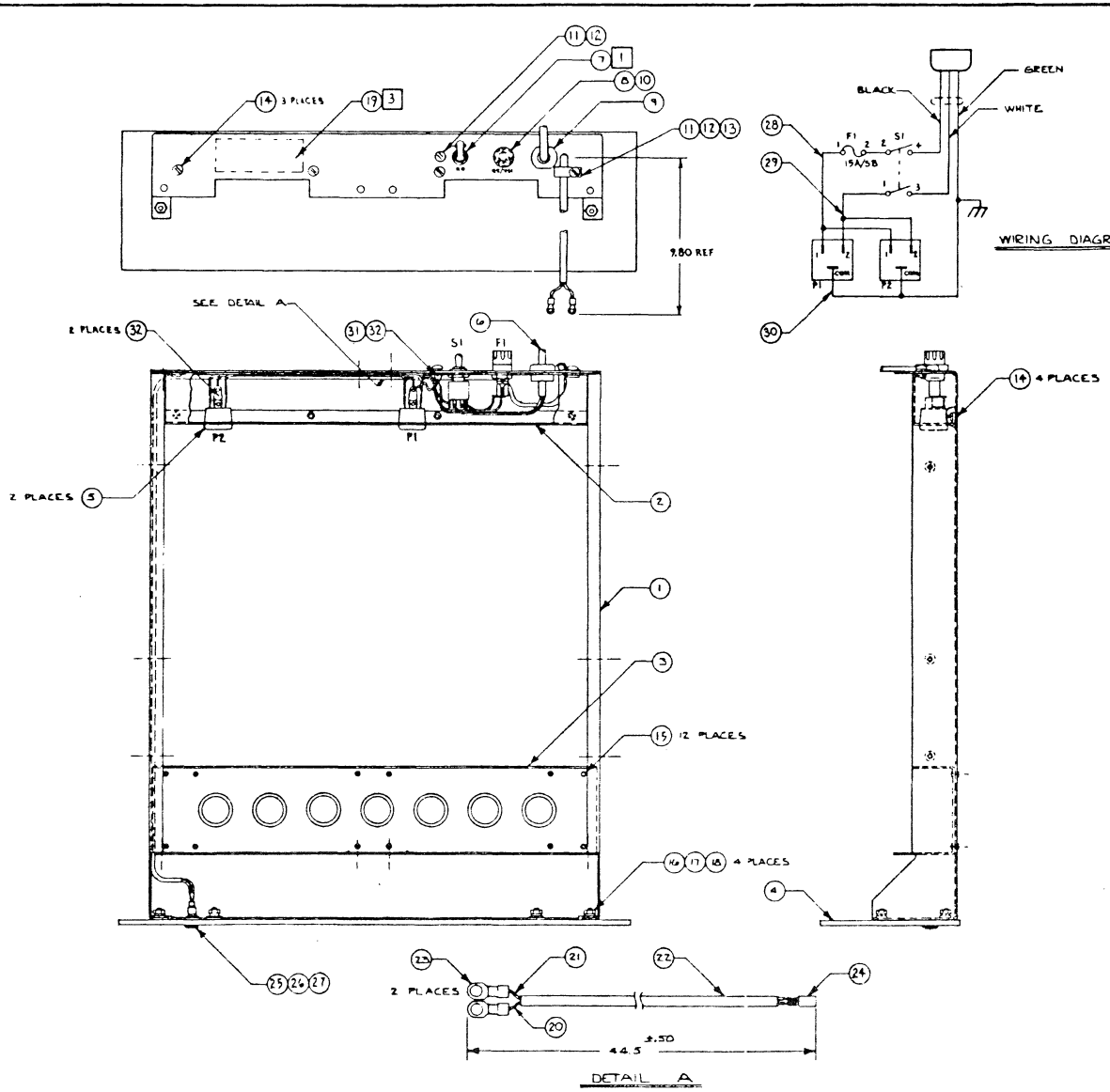


NOTES:

1. FIRST 4090-STD MUST BE INSTALLED ON THIS SIDE AS SHOWN.
2. CONNECT PILOT LIGHT CABLE TERMINAL LUGS AS SHOWN.
3. SECURE PILOT LIGHT CABLE WITH TIE WRAP SUPPLIED WITH 4090-ETC.
4. FOR EACH 4090-STD SECURE AC POWER CORD WITH TIE WRAPS AND PLUG INTO RECEPTACLE AS SHOWN.
5. SECURE EACH 4090-STD (POWER SUPPLY) TO 4091-BTD (DRAWER ASSY) WITH 4 HEX SCREWS SUPPLIED WITH 4090-STD.
6. UNIT MAY BE ASSEMBLED WITH ONE OR TWO 4090-STDS DEPENDING UPON THE NUMBER OF DRIVES IN THE SYSTEM.

DRAWN BY		8-27-73	Shugart Associates	ASSEMBLY INSTRUCTIONS 4090-STD & 4091-STD
ENGINEER		8-29-73		
MFG. APPROVAL		9-29-73	FINAL ASSEMBLY	
			1/2	D-4090-9001-1

FIG. 2-6



REVISIONS			
DTM	DESCRIPTION	BY	APPROVED
A	AS ISSUED		

NOTES:

1. INSERT SWITCH ITEM 7 WITH KEYWAY UP
2. TYPICAL REAR VIEWS OF COMPONENTS NUMBERS ARE FOR REFERENCE ONLY.

3. IDENTIFY ASSEMBLY USING SERIAL TAG (ITEM 19)
   MODEL - 4091 - STD
   SERIAL - (ASSIGNED BY MFG) FREQ - 49-61 HZ
   VOLTS - 115/220 ±10% VA - 1500 (2 UNITS)

WIRING TABLE

FROM	TO	INSULATION LENGTH	COLOR	WIRE
AC PWR CORD	S1-4		BLK	16 STR 30V
AC PWR CORD	S1-3		WHT	"
AC PWR CORD	TERMINAL LUG		GRN	"
TERMINAL LUG	P1-COM		"	"
P1-COM	P2-COM		"	"
S1-2	F1-2		BLK	"
F1-1	P1-1		"	"
P1-1	P2-1		"	"
S1-1	P1-2		WHT	"
P1-2	P2-2		"	"

		8-24-79	ASSEMBLY POWER SUPPLY	
		8-29-79		
		9/(illegible)	4090-9001-1	4091-STD
				D 4091 -7001-1

FIG. 2-7

APPENDIX B

3050 SCHEMATICS

3010-6002-42,43,44,45

3010-6003-9

3010-6006-8,9

3010-6008-7,8

3012-6002-5

3015-6011-4

3015-6012-4

3017-6008-9

3020-6002-4

3020-6004-4

3020-6006-3,4,5

3040-6005-4

3040-6007-3,4

3041-6001-3

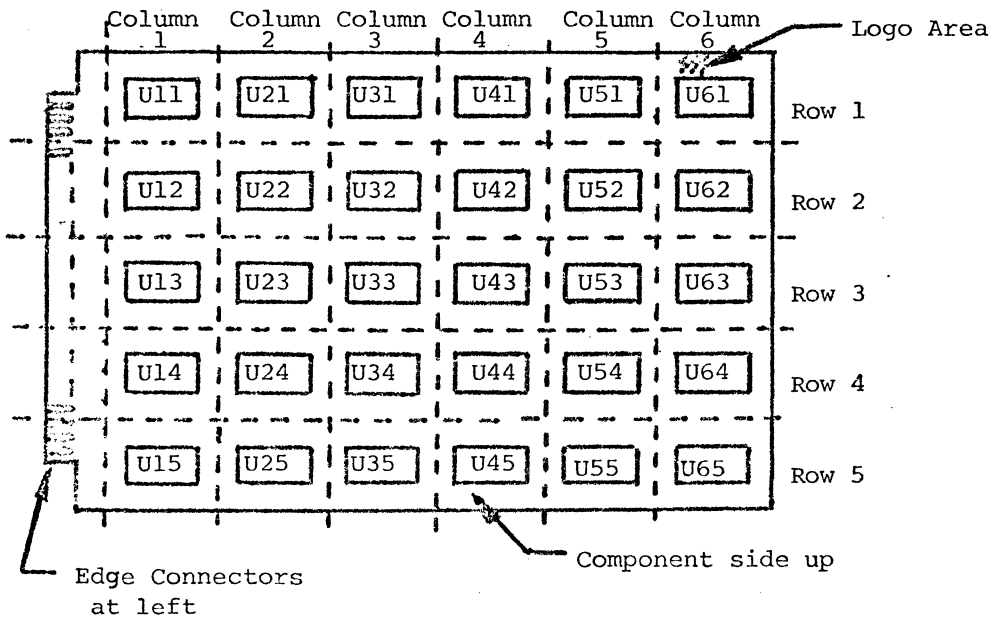
3050-9006-1

3050-9007-1

SI IC MATRIX AND DATE CODES

I. IC MATRIX

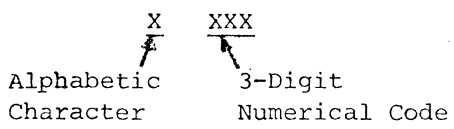
The integrated circuits on SI printed circuit boards are identified by a row and column number as shown in the diagram below. The IC identified as U11 (column 1, row 1) is the DIP package in the upper left hand corner of the board when it is held component-side-up with the edge connectors on the left side.



The number of columns or rows may exceed 9 without ambiguity; e.g. U310 is the package at column 3, row 10. U103 is the package at column 10, row 3, while U13 is the package at column 1, row 3. On no board does both the number of columns and the number rows exceed 10.

II. DATE CODES

The PC assemlby date code is in the following format.



The alpha character is simply the revision level of the artwork used to produce the etched patterns on the PC board. It is not an indication of the electrical level of the finished board, because the original etched pattern may have been changed by rework to incorporate Engineering Change Orders.

The number describing the electrical configuration is a three digit code representing the approximate date of the last electrical (logical) change made to the board. A date code of E610 is interpreted to mean a board which last changed in the 10th week of 1976. The board is said to be at electrical level 610; the logic drawing referencing this date code is the appropriate drawing to use to obtain a description of that particular electrical revision. A board bearing the date code A610 is at the same electrical level and is interchangeable with the E610 board, although the two may look different because two different etch patterns are involved.

A13 FH+W DSR LOAD EN
B9 DSR CLOCK
B16 DSR LOAD EN
B15 /DISK DATA
B8 BIR 2 INTP
B4 /GATE → BIR 1U
B12 READ DISK
B31 /MDB 7
B23 /MDB 6
B22 /MDB 5
B18 /MDB 4
B20 /EN BIR 1U → BUS
A21 /EN BIR 2U → BUS
A22 /ADD → 1B
B5 /GATE → BIR 2U
B24 WCR 11
B30 /LOAD WCR
A12 NU
A19 NU
B29 CAR 11
A23 WCCA 2
B27 /LOAD CAR
A29 ACR CLOCK
A31 ACR LOAD EN
A30 Σ
A24 EN ADD → ACR
A26 DISK SELECT
B26 BAR 14
A27 BAR 13
A25 BAR 12
A3 /SET WLO ER
A8 /CL ERROR REG
A7 /SET TIMING ER
B3 /READ CrE REG U
A20 CAR 12
A15 /(ACR LOAD EN) (WEN)
A16 /W DSR LOAD EN

/FH+W DSR LOAD EN A14
/DSR MSB B11
NU B6
/DSR 12 B10
/MD 7 B19
/MD 6 B21
/MD 5 A10
/MD 4 B13
(WCR 15) NU B17
WCR 0-3=1's B7
CAR 15 B25
CAR 14 B28
NU A11
CAR 13 A9
CAR 12 B14
ACR 12 A28
/IB 01 A4
/IB 06 A6
/IB 05 A5
FH+W DSR LOAD EN A17

NOTES:
1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6002-42 AT DATE CODE 232.

A1, B1 +5V
A18, A2, B2 GND
C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01, R1 +Y

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO
DRAWN	ROBINSON 4-20-75 DATE	System Industries SUNNYVALE CALIFORNIA	MATL DWG NO
CHECKED	DATE	TITLE DATA SHIFT REG BITS	MATL SPEC
ENGR	DATE	PART ASSEMBLY	
		PART NUMBER B-3010-6002-42	

REVISIONS			
SYM	DESCRIPTION	DATE	APPR
A	AS ISSUED	4-16-75	

V1

A13 PSEUDO BUSY — U12 7400 — /PSEUDO BUSY A14

B9 DSR CLOCK

B16 DSR LOAD EN

B15 /DSR 12

B8 BIR 2 INTP

B4 /GATE → BIR 1U

B12 READ DISK

B31 /MDB 3

B23 /MDB 2

B22 /MDB 1

B18 /MDB 0

B20 EN BIR 1U → BUS

A21 EN BIR 2U → BUS

A22 /ADD → IB

B5 /GATE → BIR 2U

B24 WCR 07

B30 /LOAD WCR

A12 Ø2

A19 /FH INIT

B29 CAR 07

A23 WCCA 2

B27 /LOAD CAR

A29 ACR CLOCK

A31 ACR LOAD EN

A30 ACR 12

A24 EN ADD → ACR 1

A26 BAR 11

B26 BAR 10

A27 BAR 09

A25 BAR 08

A3 /SET DISK SEL ER

A8 /CL ERROR REG

A7 /SET PARITY ER

B3 /READ C&E REG U

A20 CAR 08

A15 /FH INIT

A16 /DATA DSR CLOCK

(/DSR 11) NU B11

NU B6

/DSR 08 B10

/MD 3 B19

/MD 2 B21

/MD 1 A10

/MD 0 B13

WCR 11 B17

WCR 4-7=1's B7

CAR 11 B25

CAR 10 B28

/FH DELAYED ACR CLOCK A11

CAR 09 A9

CAR 08 B14

ACR 08 A28

/IB 06 A4

/IB 02 A6

/IB 01 A5

DSR CLOCK A17

NOTES:

1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6002-43 AT DATE CODE 232.

A1, B1 +5V — C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01, R1 — +V

A18, A2, B2 GND

DRAWN BY	ROBINSON	4-10-75	
ENGINEER			
PROJECT ENGINEER		4-16-75	
SUPERVISOR DEPT		4-16-75	

System Industries, SUNNYVALE CALIFORNIA

TITLE: DATA SHIFT REG BITS

PART NUMBER: B-3010-6002-43

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	4-25-75	

A13 SET WRITE EN

B9 DSR CLOCK

B16 DSR LOAD EN -

B15 /DSR 08

B8 BIR 2 INTP

B4 /GATE → BIR 1L

B12 READ DISK

B31 /MDB 7

B23 /MDB 6

B22 /MDB 5

B18 /MDB 4

B20 /EN BIR 1L → BUS

A21 /EN BIR 2L → BUS

A22 /ADD → IB

B5 /GATE → BIR 2L

B24 WCR 03

B30 /LOAD WCR

A12 (01) (WCCA DONE)

A19 /COMP IR

B29 CAR 03

A23 WCCA 2

B27 /LOAD CAR

A29 ACR CLOCK

A31 ACR LOAD EN

A30 ACR 08

A24 EN ADD → ACR

A26 BAR 07

B26 BAR 06

A27 BAR 05

A25 BAR 04

A3 /SET WRITE CHK ER

A8 /CL ERROR REG

A7 /SET SEEK INC ER

B3 /READ C&E REG U

A20 CAR 04

A15 /FH INIT

A16 /DATA SET WEN

A14 /SET WRITE EN

B11 (/DSR 07) NU

B6 NU

B10 /DSR 04

B19 /MD 7

B21 /MD 6

A10 /MD 5

B13 /MD 4

B17 WCR 07

B7 WCR 8-11=1's

B25 CAR 07

B28 CAR 06

A11 /INIT READ

A9 CAR 05

B14 CAR 04

A28 ACR 04

A4 /IB 02

A6 /IB 04

A5 /IB 03

A17 SET WRITE EN

NOTES:

1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6002-44 AT DATE CODE 232.

A1, B1 +5V

A18, A2, B2 GND

C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01, R1 +V

SIZE	DWG	ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO
ENGINEER	ROBINSON	DRAWN BY			
APPROVED		DATE	4-10-75		MATL DWG NO
FINISH		SHEET ASSEMBLY			MATL SPEC
SCALE					
PART NUMBER	B-3010-6002-44	TITLE	DATA SHIFT REG BITS		

REVISIONS			
DASH	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	4/16/75	T3

LOC Y3

A13 /DATA ACR LOAD EN

DATA ACR LOAD EN A14

B9 DSR CLOCK

B16 DSR LOAD EN

B15 /DSR 04

(/DSR 03) NU B11

B8 BIR 2 INTP

NU B6

B4 /GATE → BIR 1L

B12 READ DISK

B31 /MDB 3

/DSR LSB B10

B23 /MDB 2

B22 /MDB 1

/MD 3 B19

B18 /MDB 0

B20 /EN BIR 1L - BUS

A21 /EN BIR 2L → BUS

A22 /ADD → IB

/MD 2 B21

B5 /GATE → BIR 2L

B24 /INC WCR

B30 /LOAD WCR

/MD 1 A10

A12 (Φ1) (WCCA DONE)

A19 /COMP IW

B29 INC CAR

A23 WCCA 2

/MD 0 B15

B27 /LOAD CAR

WCR 03 B17

A29 ACR CLOCK

WCR 12-15=1's B7

A31 ACR LOAD EN

CAR 03 B25

A30 ACR Φ4

CAR 02 B28

A24 EN ADD → ACR

/INIT WRITE A11

A26 BAR 03

CAR 01 A9

B26 BAR (LSB+2)

(CAR 00) NU B14

A27 BAR (LSB+1)

ACR LSB A28

A25 BAR LSB

/IB 03 A4

/IB 04 A6

NU A5

/(ACR LOAD EN) (WEN) A17

A3 /SET LAI ER

A8 /CL ERROR REG

A7 /SET ADD VER ER

B3 /READ C¢E REG U

A20 CAR 00

A15 DATA ACR LOAD EN

A16 WRITE EN FF

NOTES:

1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6002-45 AT DATE CODE 232.

A1, B1 +5V

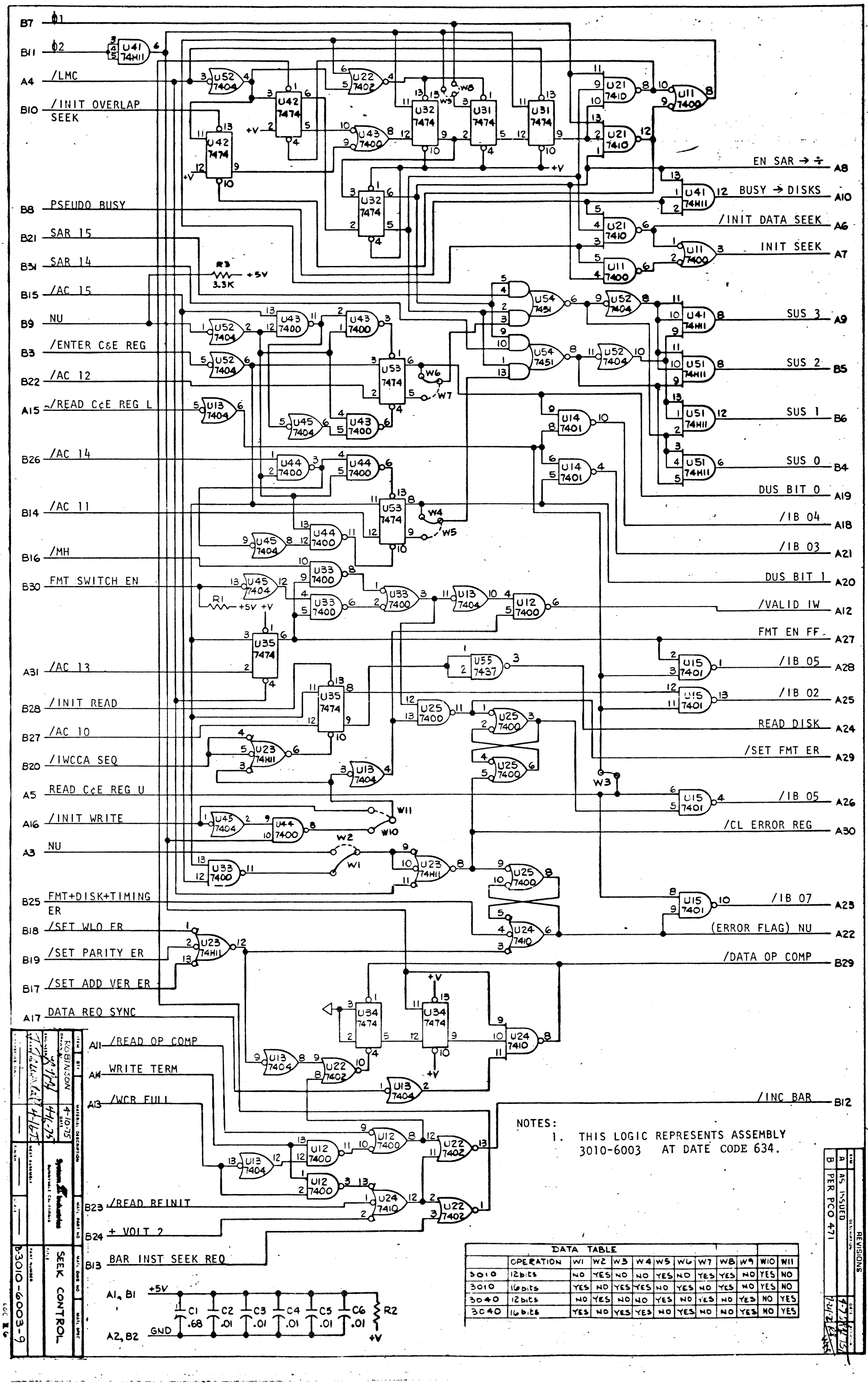
A18, A2, B2 GND

C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01, R1 +V

REVISIONS			
ITEM	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	4-23-74	

SUPERSEDES DWG	ITEM	QTY	MATERIAL DESCRIPTION		
ENGINEER	ROG/KEON	4-10-75			
DRAWN BY		DATE			
ENGINEER		4-16-75			
FINISH	NEXT ASSEMBLY		System Science Instruments SUNNYVALE CALIFORNIA	MATL PART NO	
STAGE					
PART NUMBER	TITLE			MATL DWG NO	MATL SPEC
B-3010-6002-45	DATA SHIFT REG BITS				

CON Y4



NOTES:

1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6003 AT DATE CODE 634.

DATA TABLE

	OPERATION	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11
3010	12bits	NO	YES	NO	NO	YES	NO	YES	YES	NO	YES	NO
3010	16bits	YES	NO	YES	YES	NO	YES	NO	YES	NO	YES	NO
3040	12bits	NO	YES	NO	NO	YES	NO	YES	NO	YES	NO	YES
3040	16bits	YES	NO	YES	YES	NO	YES	NO	NO	YES	NO	YES

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	4-7-75	
B	PER PCO 471	4-4-75	

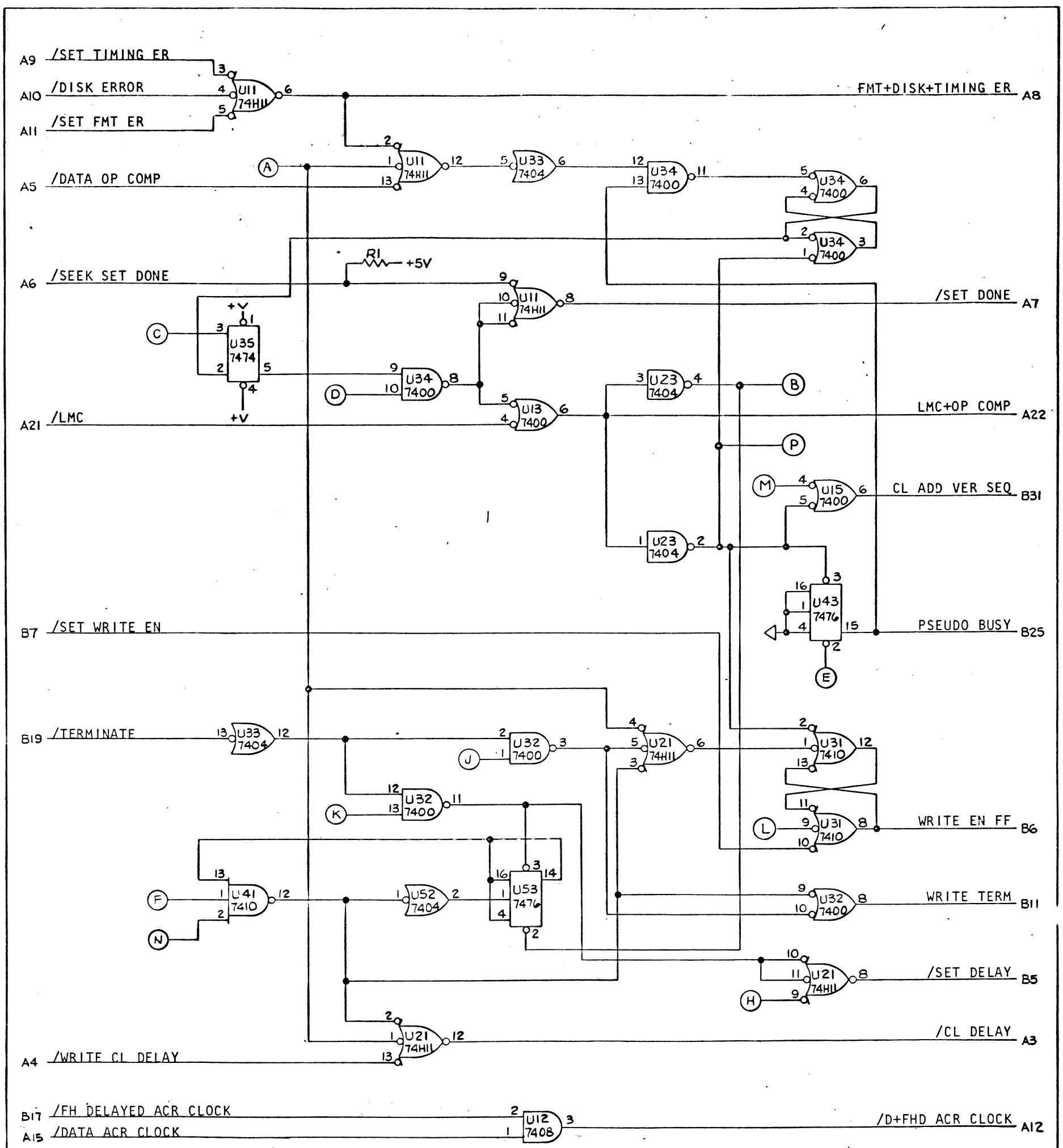
ROBINSON DRAWN 4-10-75

SYSTEMS & SCIENCE SUNNYVALE CALIFORNIA

SEEK CONTROL

PART NUMBER D-3010-6003-9

SIZE E6



NOTES: 1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6006 AT DATE CODE 511.

REVISIONS			
SYM	DESCRIPTION	DATE	APPR.
A	AS ISSUED	8-9-72	RLS
B	PER PCO 291	4-75	RMT ST

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
DRAWN BY Thompson	DATE 8-9-72	System Industries SUNNYVALE CALIFORNIA	TITLE FORMAT SEQUENCE		
ENGINEER Knudsen	DATE 8-24-72				
MFG APPROVAL Knudsen	DATE 9/22	NEXT ASSEMBLY	PART NUMBER 3010-6006-8		
OPERATIONS DWG	FINISH —	FINISH —			

LCC Z3
SHEET 2 OF 2

B21 READ DISK
A20 /BUS→BIR
A18 /VALID IW
A19 /INIT DATA SEEK
B8 ϕ1E
B28 ϕ2
B15 /MH
A29 ϕ1
B27 /SECTOR COIN
A28 UNIT READY
B23 /INC BAR
B24 /INIT DATA SEQ
A13 /MH INIT WRITE SEQ
A17 /MH INIT READ SEQ
B20 FMT EN FF
A30 /FH+W DSR LOAD EN
A23 WCR 12-15=1's
B16 MH WRITE CLOCK
B10 WBC FULL
B14 MH DATA CLOCK
A26 WCR 0-3=1's
A25 WCR 4-7=1's
B9 19.2us
A24 WCR 8-11=1's
B13 /FH INIT

MH B29
/IW SEQ A14
/IR SEQ A16
/INIT ADD VER SEQ B12
FMT SEQ FF B22
/FMT SET WEN B4
DSR LOAD EN A31
/FMT DSR CLOCK B30
FMT BIR→DSR B26
/WCR=1's A27
/FMT INC WCR B18
/FMT INC WBC B3

A1, B1 +5V
A2, B2 GND
C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01, R2 +V

DATA CODE									
	OPERATIONS	W1	W2	W3	W4	W5	W6	W7	W8
3010	12 bits	NO	YES	NO	YES	NO	YES	YES	NO
3010	16 bits	YES	NO	YES	NO	YES	NO	YES	NO
3040	12 bits	NO	YES	YES	NO	YES	NO	NO	YES
3040	16 bits	YES	NO	YES	NO	YES	NO	NO	YES

NOTES: 1. THIS LOGIC REPRESENTS ASSEMBLY 3010-6006 AT DATE CODE 511.

REVISIONS			
ECM	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	10-12	
B	PER PCO 291	4-75	TST

ITEM	DATE	MATERIAL DESCRIPTION	MATL PART NO
	10-4-72	System Industries SUNNYVALE CALIFORNIA	MATL DWG NO
	10-12		MATL SPEC
DRAWN BY		TITLE FORMAT SEQUENCE	
		PART NUMBER B-3010-6006-9	

LOC Z3
SHEET 1 OF 2

B14 FMT SEQ FF
B13 ACR LSB
B12 /DSR LSB
B24 MH WRITE CLOCK
B25 51.2us
B31 MH WRITE CLOCK
B30 FH WRITE CLOCK
B21 FH WRITE BUSY
B15 MH DATA CLOCK
B7 WBC FULL
B8 FMT BIR→DSR

WRITE DATA B6
/WRITE DATA PRE B5
/DATA SET WEN B26
/WRITE CL DELAY B28
/FH INIT B11
/WRITE DSR CLOCK A31
/TERMINATE B4
/INC SWC B20
/W DSR LOAD EN A10
/BIR→DSR B9
DATA INC WCP B3
/DATA ACR CLOCK B29

R2 +5V
R3 +5V
R4 +5V
R5 +5V
R7 +5V
R8 +5V
+V

U21 74H11
U23 7410
U22 7440
U24 7404
U31 7404
U32 7476
U41 7400
U42 7402
U43 7401
U44 7476
U45 7410
U51 7410
U52 7400
U53 7400
U54 74122
U55 74H11
U61 7476
U62 7400
U63 7410
U64 74122
U65 7451

REVISIONS			
SYM	DESCRIPTION	DATE	APPD
A	AS ISSUED	9/24/72	JCS
B	PER PCO 176	5/17/73	JM

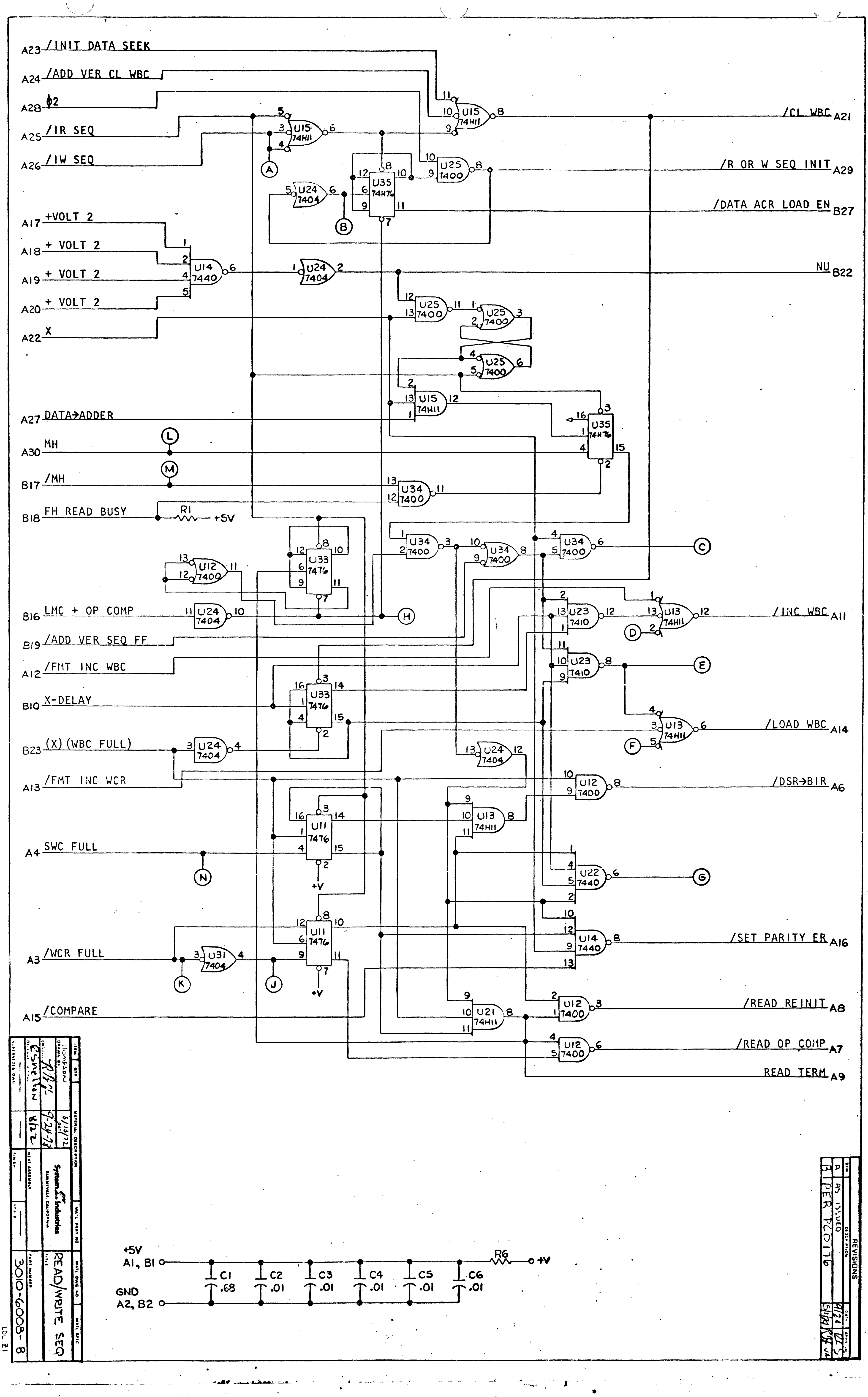
ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO
DRAWN BY	Thompson	8/14/72	
ENGINEER	[illegible]	9/24/73	
MFG APPROVAL	[illegible]	9/22	
SUPERVISOR'S OMNI	—	NEXT ASSEMBLY	
FINISH	—	SCALE	

System Industries
SUNNYVALE CALIFORNIA

TITLE: READ/WRITE SEQ

MATL DWG NO
MATL SPEC
PART NO. 300-6008-7

LOC 21


A23 /INIT DATA SEEK
A24 /ADD VER CL WBC
A28 ϕ2
A25 /IR SEQ
A26 /IW SEQ
A17 +VOLT 2
A18 + VOLT 2
A19 + VOLT 2
A20 + VOLT 2
A22 X
A27 DATA→ADDER
A30 MH
B17 /MH
B18 FH READ BUSY
R1
+5V
B16 LMC + OP COMP
B19 /ADD VER SEQ FF
A12 /FMT INC WBC
B10 X-DELAY
B23 (X) (WBC FULL)
A13 /FMT INC WCR
A4 SWC FULL
A3 /WCR FULL
A15 /COMPARE
/CL WBC A21
/R OR W SEQ INIT A29
/DATA ACR LOAD EN B27
NU B22
/INC WBC A11
/LOAD WBC A14
/DSR→BIR A6
/SET PARITY ER A16
/READ REINIT A8
/READ OP COMP A7
READ TERM A9
U15 74H11
U25 7400
U24 7404
U35 74H76
U14 7440
U34 7400
U12 7400
U33 7476
U23 7410
U13 74H11
U11 7476
U22 7440
U31 7404
U21 74H11
A B C D E F G H J K L M N
+V
+5V
A1, B1
GND
A2, B2
C1 .68
C2 .01
C3 .01
C4 .01
C5 .01
C6 .01
R6
+V
ITEM
QTY
MATERIAL DESCRIPTION
MAT'L PART NO
MAT'L DWG NO
MAT'L SPEC
DRAWN BY Thompson
DATE 8/16/72
ENG.
9-24-73
RELEASE TO MFG. E. Snelton
8/72
SUPERSEDES DWG.
NEXT ASSEMBLY
FINISH
SCALE
System Industries
SUNNYVALE, CALIFORNIA
TITLE READ/WRITE SEQ
PART NUMBER 3010-6008-8
REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
A AS ISSUED 9/24
B PER PCO176 5/1/74

A29 CYC ADD 6
A30 CYC ADD 5
B28 CYC ADD 4
B27 CYC ADD 3
B26 CYC ADD 2
B29 CYC ADD 1
B30 CYC ADD 0
B18 HEAD SELECT
A19 CYC ADD 8
A28 CYC ADD 7
A7 INIT SEEK
A13 SUS (*)
B4 BUSY→DISKS
B19 /DUS (*)
A16 /PSEUDO BUSY
A22 Ø2
A26 /LMC
B25 /PMC
B15 LMC+OP COMP
B16 /IW SEQ
B17 /IR SEQ
C15 /FILE READY
C17 /READ BUSY
C19 /WRITE BUSY
C3 /READ DATA
C5 /READ CLOCK
B31 WRITE DATA
C7 /WRITE CLOCK
C13 /INDEX MARK
B5 TP-/INDEX
C11 /SECTOR MARK
B8 TP-/SECTOR
C25 /WRITE LOCKOUT ER

U35 7475
U45 7475
U21 7404
U51 7410
U25 7404
U22 7410
U43 7438
U52 7474
U24 7401
U31 7476
U23 7401
U41 7474
U55 7476
U53 7401
U11 7493
U33 7438
U34 7438
U44 7438
U42 7483
U13 7401
U14 7401
U15 7438
U12 7401

W1 W2 W3 W4 W5 W6

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27
1.2K +5V
91Ω +5V
330Ω +5

TA7 C27
TA6 C29
TA5 C31
TA4 C33
TA3 C35
TA2 C37
TA1 C39
NU A14
SSR-UNIT(*) BUSY ER A27
/SEEK SET DONE A17
/256 EN B10
SEEK INCOMPLETE B21
WRITE CHECK B24
/SEL DISK READY B3
LOG ADD INT B22
/WRITE COMMAND C23
/MEMORY SELECT C21
13 FILE NOT READY B23
FH READ BUSY A21
FH WRITE BUSY A23
FH DATA A25
FH READ CLOCK B14
/DATA INPUT C9
10FH WRITE CLOCK B13
/SC04 A11
/SC03 A8
/SC02 A12
/SC01 A9
/SC00 A10
/FH WLO ER A20
/SSR-UNIT(*) READY A18
SSR-UNIT(*) HDW ER B11

HEAD JUMPER TABLE

HEAD	W2	W3	W4	W5
1	--	--	--	--
2	--	--	--	Y
3	--	--	Y	--
4	--	--	Y	Y
5	--	Y	--	--
6	--	Y	--	Y
7	--	Y	Y	--
8	--	Y	Y	Y

HEAD	W2	W3	W4	W5
9	Y	--	--	--
10	Y	--	--	Y
11	Y	--	Y	--
12	Y	--	Y	Y
13	Y	Y	--	--
14	Y	Y	--	Y
15	Y	Y	Y	--
16	Y	Y	Y	Y

C40 C38 C36 C34 C32 C30 C28
C26 C24 C22 C20 C18 C16 C14
C12 C10 C8 C6 C4 C2 C1

A1,B1 +5V
A2,B2 GND
C1 .68 C2 .01 C3 .01 C4 .01 C5 .01 C6 .01 R19 1.2K +V

		W1	W6
3010	12ST	YES	NO
3010	24ST	NO	YES
3040	12ST	YES	NO
3040	24ST	YES	YES

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	9/24/73	RF
B	PER PCO 172	5/17/74	RF
C	PER PCO 246	11/5/74	RF

SUPERSEDES DWG	
ENGINEER	TIMPSON
DATE	8/9/72
FINISH	
SCALE	
MATERIAL DESCRIPTION	
NEXT ASSEMBLY	3012-00
TITLE	FIXED HEAD INTERFACE 3040 SERIES
MASK PART NO	
MASK DWG NO	
PART NUMBER	3012-6002
MASK SPEC	

B-3012-6002-5
LOC(A)

A10 /READ BAR L
B8 /READ SEEK STATUS REG L
B16 SSR-UNIT 1 HDW ER
B17 SSR-UNIT 1 BUSY ER
B15 /SSR UNIT 1 READY
B12 SSR UNIT 0 HDW ER
B9 SSR UNIT 0 BUSY ER
B11 /SSR UNIT 0 READY
B24 /AC07
B23 /AC06
B22 /AC05
B21 /AC04
A9 /LOAD SAR
A25 /LOAD BAR
B31 /AC03
B30 /AC02
B29 /AC01
B28 /AC00 LSB
A26 /INC BAR
B18 /IB07 MSB
A18 /IB06
A17 /IB05
A16 /IB04
A12 /IB03
A11 /IB02
A15 /IB01
A13 /IB00 LSB
A5 /R2
A14 R0
B25 BAR 08
A8 EN SAR → ÷
B14 /304024 SEL

U11 7404 · U34 74175 · U33 74193 · U35 74175 · U32 74193 · U31 74153 · U61 74153 · U45 74153 · U21 74153 · U23 7401 · U24 7401 · U12 7401 · U22 7401 · U13 7416 · Q1 R1 +5 1.5K · Q2 R2 +5 1.5K · Q3 R3 +5 1.5K · Q4 R4 +5 1.5K · Q5 R5 +5 1.5K · Q6 R6 +5 1.5K · Q7 R7 +5 1.5K · Q8 R8 +5 1.5K · R9 +5 · R10 +5 · R11 +5 · R12 +5 · R13 +5 · R14 +5 · R15 +5 · R16 +5 · R17 +5 1.5K

BAR 07 B13
BAR 06 B19
BAR 05 A19
BAR 04 A20
BAR 03 B27
BAR (LSB+2) A27
BAR (LSB+1) B7
BAR LSB B10
GND RETURN A21 A22 A23 A24 A28 A29 A30 A31

U62 7400 · U65 7400 · U51 7404 · U64 7402 · U63 7451 · U44 7404 · U55 7400 · U54 7451 · U53 7400 · U52 7402 · U43 7400 · U42 7451 · U41 7400

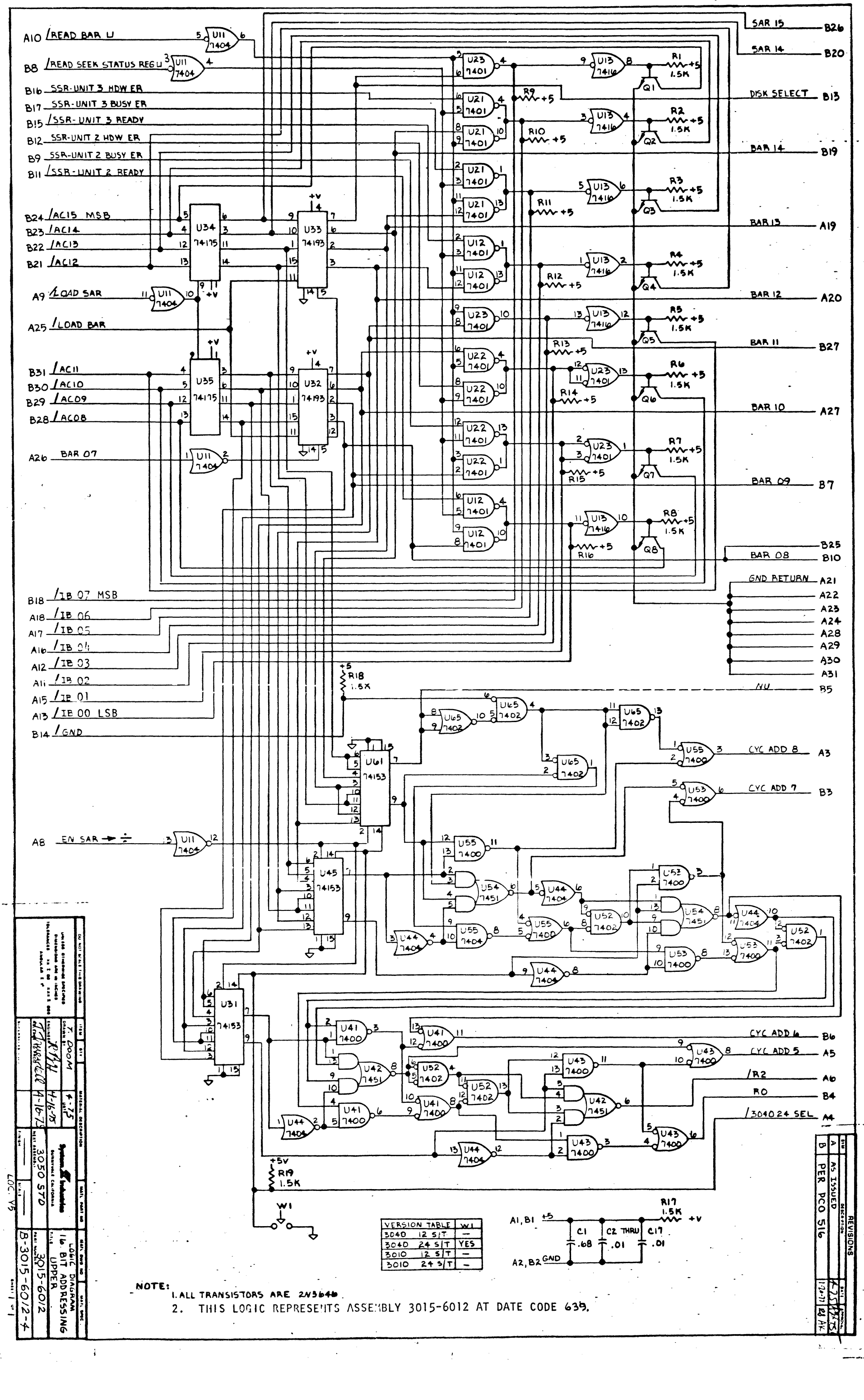
CYC ADD 4 A4
CYC ADD 3 B20
CYC ADD 2 A3
CYC ADD 1 B26
CYC ADD 0 B5
24 SEC ADD 04 A6
24 SEC ADD 03 A7
HEAD SELECT B6
12 SEC ADD 03 B3
12 SEC ADD 02 B4

+5 A1, B1 · GND A2, B2 · C1 .68 · C2 THRU .01 · C17 .01 · +V

NOTE:
1. ALL TRANSISTORS ARE 2N3646
2. THIS LOGIC REPRESENTS ASSEMBLY 3015-6011 AT DATE CODE 639.

B PER PCO 516 1/4/77 RA AP
A AS ISSUED 4-25-74 AP

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX ± .02 .XXX ± .005 ANGULAR ± 2°
ITEM QTY MATERIAL OR DESCRIPTION MANUF. PART NO. MANUF. SPEC.
DRAWN BY T. DOOM 4-75
ENGINEER [illegible] 4-16-75
MFG. ASSEMBLY 4-16-75
FINISH
SCALE
Sunnyvale California
TITLE LOGIC DIAGRAM 16 BIT ADDRESSING LOWER
PART NUMBER 3015-6011
B-3015-6011-4
SHEET 1 OF 1
LOC. Y6



VERSION TABLE	W1
3040 12 S/T	—
3040 24 S/T	YES
3010 12 S/T	—
3010 24 S/T	—

NOTE:
1. ALL TRANSISTORS ARE 2N3646
2. THIS LOGIC REPRESENTS ASSEMBLY 3015-6012 AT DATE CODE 639.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	1-20-77	RB AK
B	PER PCO 516		

DRAWN BY	J. DOOM	4-16-75	
ENGINEER	R. HARRELL	4-16-75	
MATERIAL			
FINISH			
SCALE			
NEXT ASSEMBLY	3050 570		
TITLE	LOGIC DIAGRAM 16 BIT ADDRESSING UPPER		
PART NUMBER	B-3015-6012-4		

Sunnyvale California

LOC. V5

A16 /ADD → BUS
B08 LOG ADD INT
B4 /SET DISK ER SENSE
A11 LMC+OP COMP
A9 FILE NOT READY
A3 WRITE CHECK
A8 SEEK INCOMPLETE
A22 /R OR W SEQ INIT
A18 /D+FHD ACR CLOCK
B11 /IWCCA SEQ
A28 /BUS → BIR
B10 INIT DATA SEQ
B12 /VALID IW
A12 /INIT READ
B28 /BIR → BUS
B31 /DSR → BIR
B27 /BIR → DSR
A29 5.083 MHZ
A31 /FMT SET WEN
B7 /MH
A24 /R OR W SEQ INIT
A23 /DATA DSR CLOCK
A26 ACR LSB
A25 DATA→ADDER
B18 WRITE DATA
B26 + VOLT 1
A13 DATA INC WCR
A21 /FMT SET WEN
A20 /FMT INC WCR

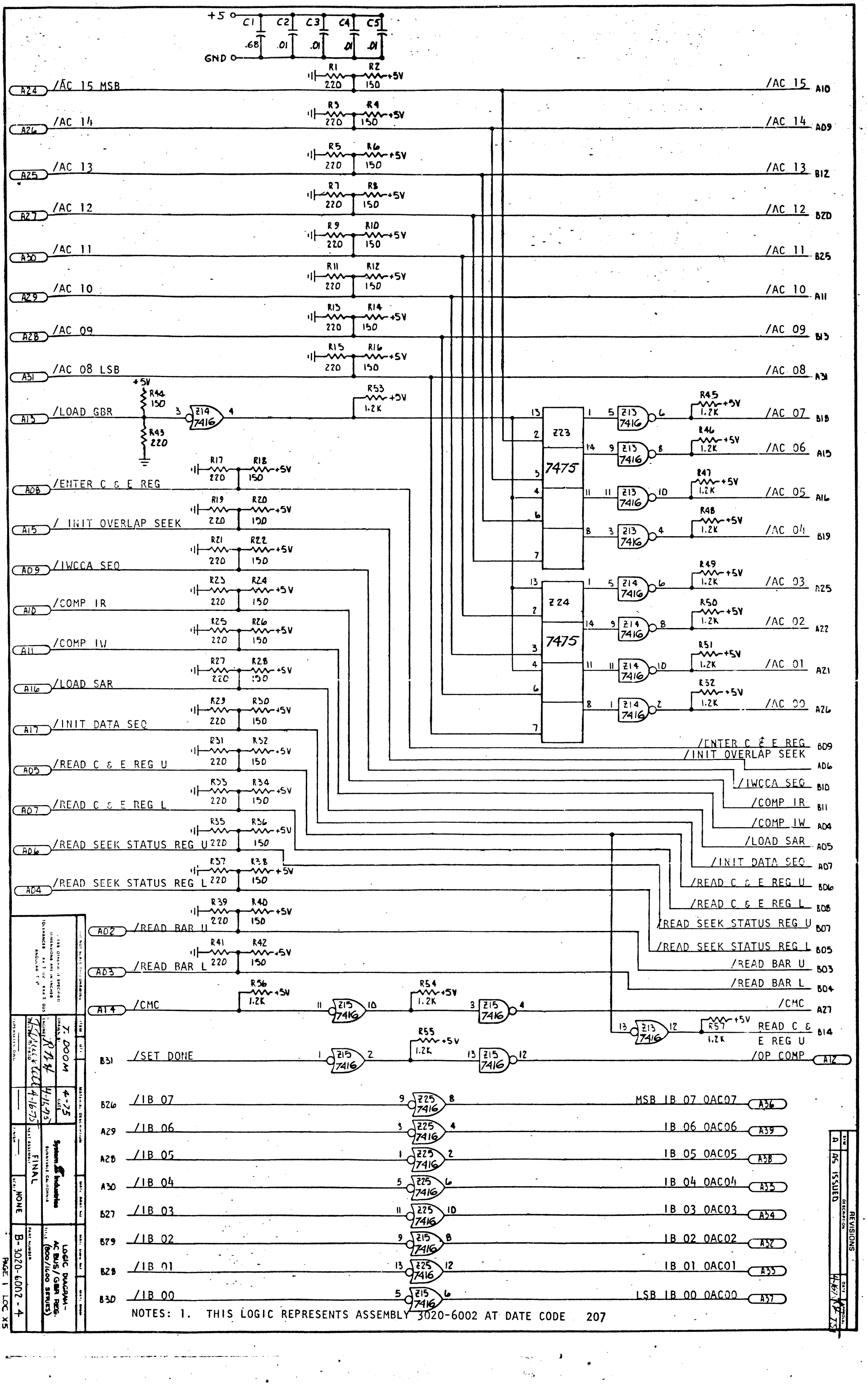
INC CAR A17
/SET LAI ER A10
/DISK ERROR A14
/SET DISK SEL ER A6
/SET WRITE CHK ER A5
/SET SEEK INC ER B5
ACR CLOCK A19
WCCA 2 B3
/LOAD WCR B6
SET BOTH REQ B14
/LOAD CAR B15
/LOAD BAR B9
(01) (WCCA DONE) A7
BIR 2 EXTP B23
(/EN BIR 1→AC) NU A30
(/EN BIR 2→AC) NU B29
/GATE → BIR 1 B30
/GATE → BIR 2 B25
01 B16
02 B13
BIR 2 INTP B24
01E B22
(010) NU B21
Σ A27
MH WRITE CLOCK B20
MH WC+D B17
MH DATA CLOCK B19
/INC WCR A15

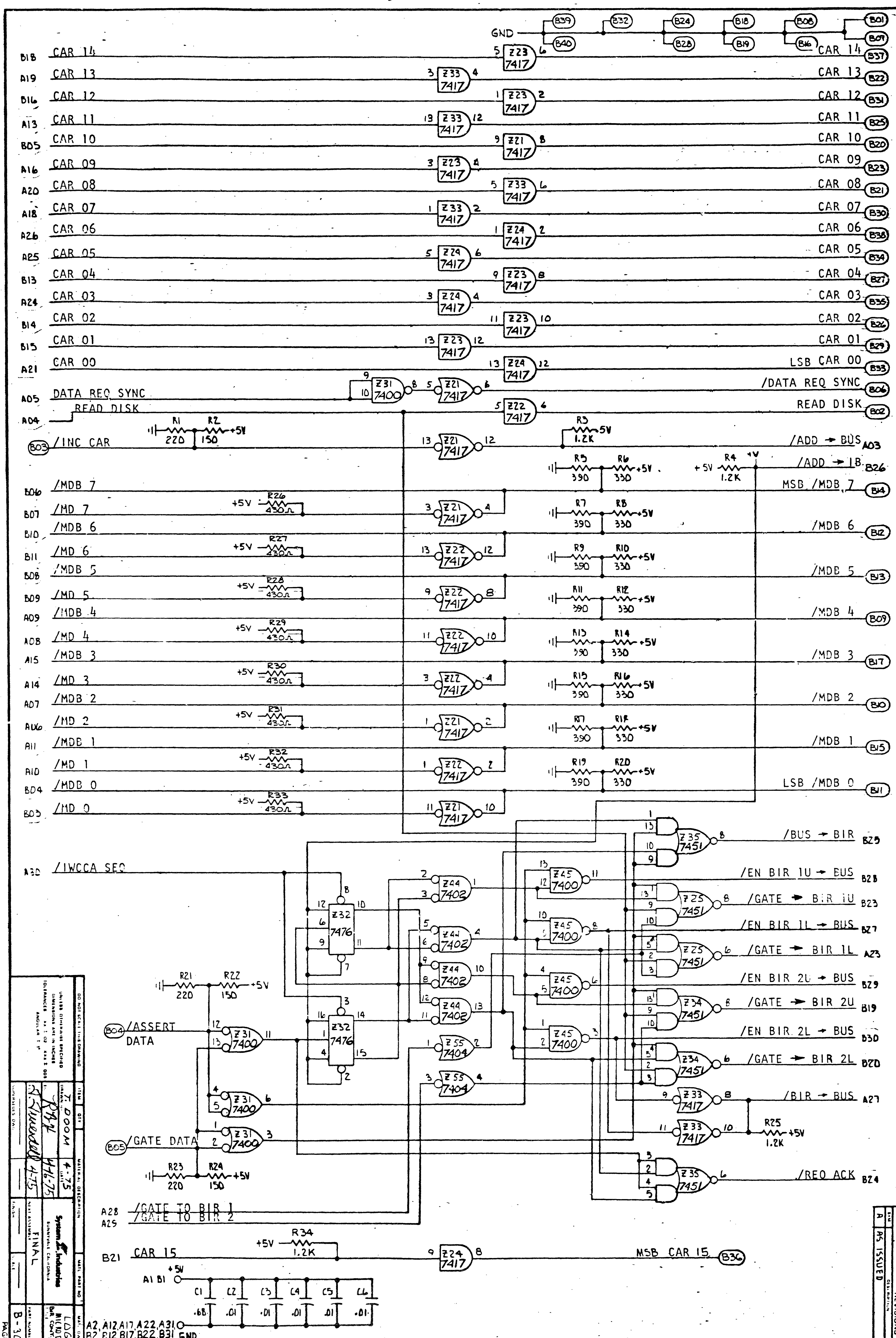
A1, B1 +5V
A2, B2 GND
C1 .68, C2 .01, C3 .01, C4 .01, C5 .01, C6 .01
R1 +V

NOTES:
1. THIS LOGIC REPRESENTS ASSEMBLY 3017-6008 AT DATE CODE 806.

REVISIONS
A AS ISSUED 4-7-74
B PER PCO# 371 4-17-74
C PER PCO 658

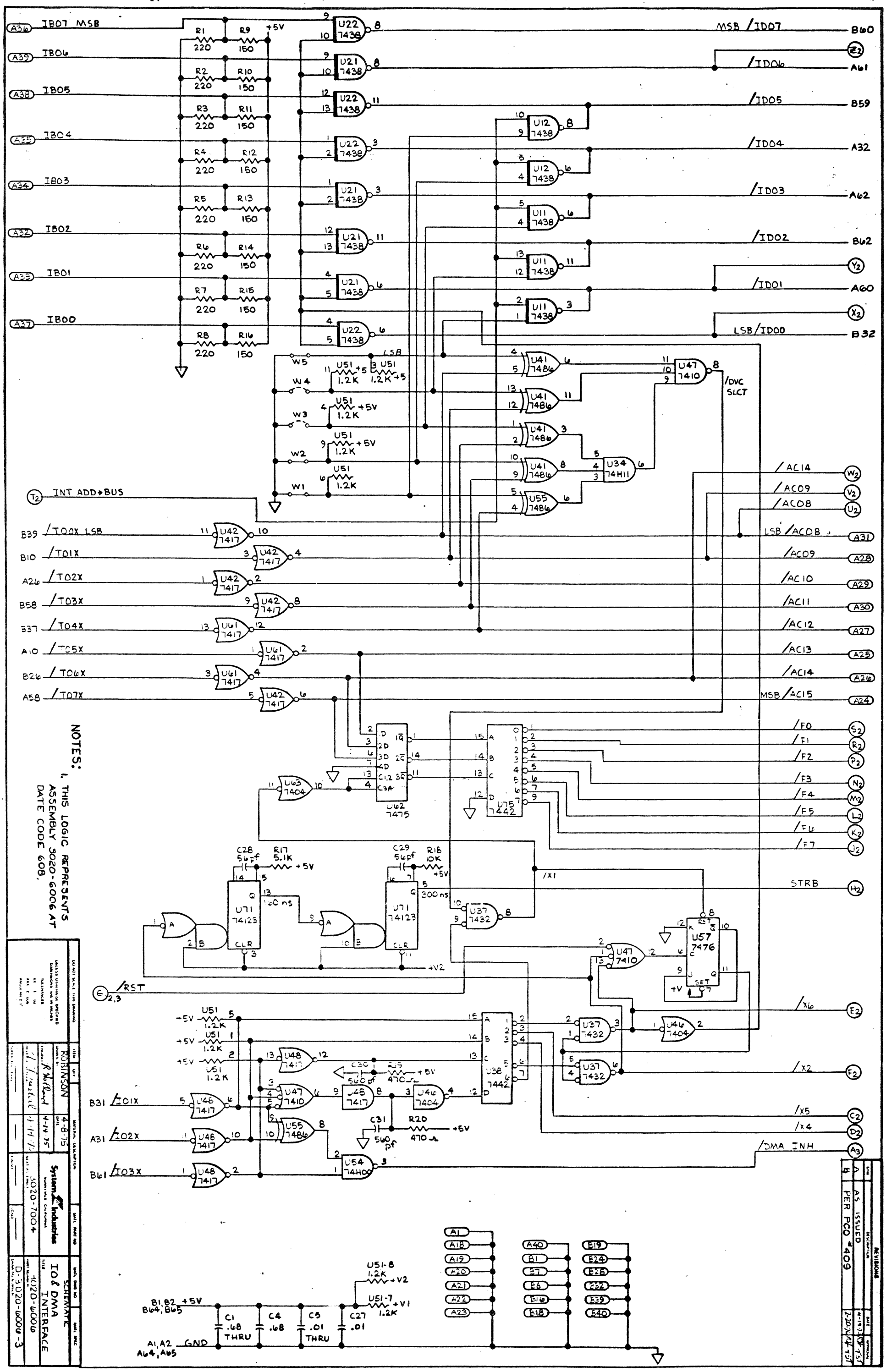
DISK ER, WCCA, CLOCKS
3017-6008
B 3017-6008-5
LOC B5


+5
C1 .68
C2 .01
C3 .01
C4 .01
C5 .01
GND
A24 /AC 15 MSB
A26 /AC 14
A25 /AC 13
A27 /AC 12
A30 /AC 11
A29 /AC 10
A28 /AC 09
A31 /AC 08 LSB
A13 /LOAD GBR
AD8 /ENTER C & E REG
A15 / INIT OVERLAP SEEK
AD9 /IWCCA SEQ
A10 /COMP IR
A11 /COMP IW
A16 /LOAD SAR
A17 /INIT DATA SEQ
AD5 /READ C & E REG U
AD7 /READ C & E REG L
AD6 /READ SEEK STATUS REG U
AD4 /READ SEEK STATUS REG L
AD2 /READ BAR U
AD3 /READ BAR L
A14 /CMC
B31 /SET DONE
B26 /IB 07
A29 /IB 06
A28 /IB 05
A30 /IB 04
B27 /IB 03
B29 /IB 02
B28 /IB 01
B30 /IB 00
Z23 7475
Z24 7475
/AC 15 A10
/AC 14 AD9
/AC 13 B12
/AC 12 B2D
/AC 11 B25
/AC 10 A11
/AC 09 B13
/AC 08 A31
/AC 07 B18
/AC 06 A15
/AC 05 A16
/AC 04 B19
/AC 03 A25
/AC 02 A22
/AC 01 A21
/AC 00 A26
/ENTER C & E REG BD9
/INIT OVERLAP SEEK AD6
/IWCCA SEQ B10
/COMP IR B11
/COMP IW AD4
/LOAD SAR AD5
/INIT DATA SEQ AD7
/READ C & E REG U BD6
/READ C & E REG L BD8
/READ SEEK STATUS REG U B07
/READ SEEK STATUS REG L B05
/READ BAR U B03
/READ BAR L B04
/CMC A27
READ C & E REG U B14
/OP COMP A12
MSB IB 07 OAC07 A36
IB 06 OAC06 A39
IB 05 OAC05 A38
IB 04 OAC04 A35
IB 03 OAC03 A34
IB 02 OAC02 A32
IB 01 OAC01 A33
LSB IB 00 OAC00 A37
NOTES: 1. THIS LOGIC REPRESENTS ASSEMBLY 3020-6002 AT DATE CODE 207
REVISIONS
A AS ISSUED 4-16-75
LOGIC DIAGRAM - AC BUS/GBR REG. (600/1600 SERIES)
PART NUMBER B-3020-6002-4
SCALE NONE
FINAL
System Industries SUNNYVALE CALIFORNIA
T. DOOM 4-75
4-16-75



NOTES:

1. This LOGIC REPRESENTS ASSEMBLY 3020-6004 AT DATE CODE 507.

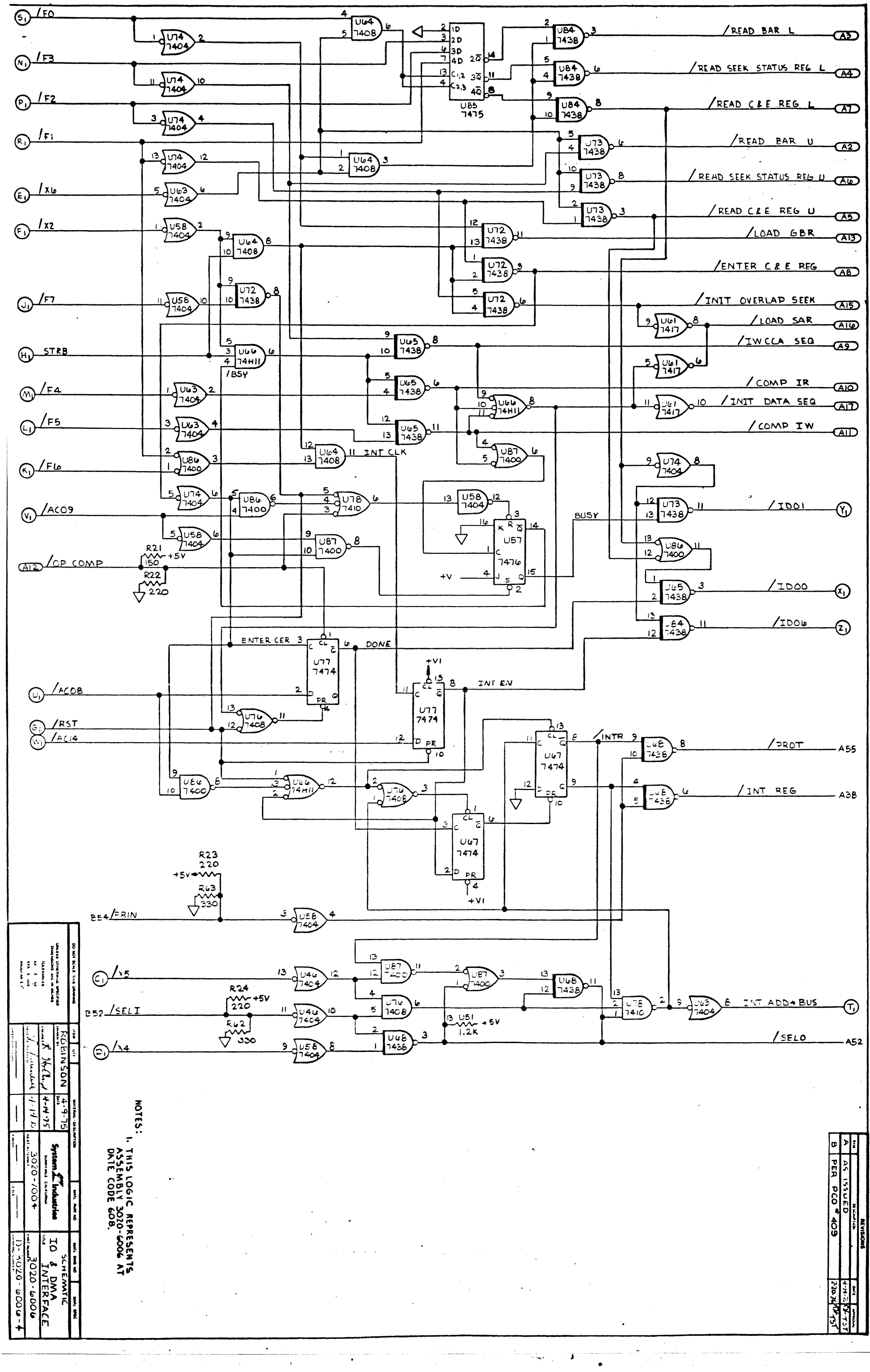


NOTES:

1. THIS LOGIC REPRESENTS ASSEMBLY 3020-6006 AT DATE CODE 608.

DRAWN	R. ROBINSON	4-8-75	System Industries	SCHEMATIC
ENGR		4-14-75		IO & DMA INTERFACE
			3020-7004	3020-6006
				D-3020-6006-3

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	4-19-74	
B	PER PCO #409	2-20-74	



NOTES:
1. THIS LOGIC REPRESENTS ASSEMBLY 3020-6006 AT DATE CODE 608.

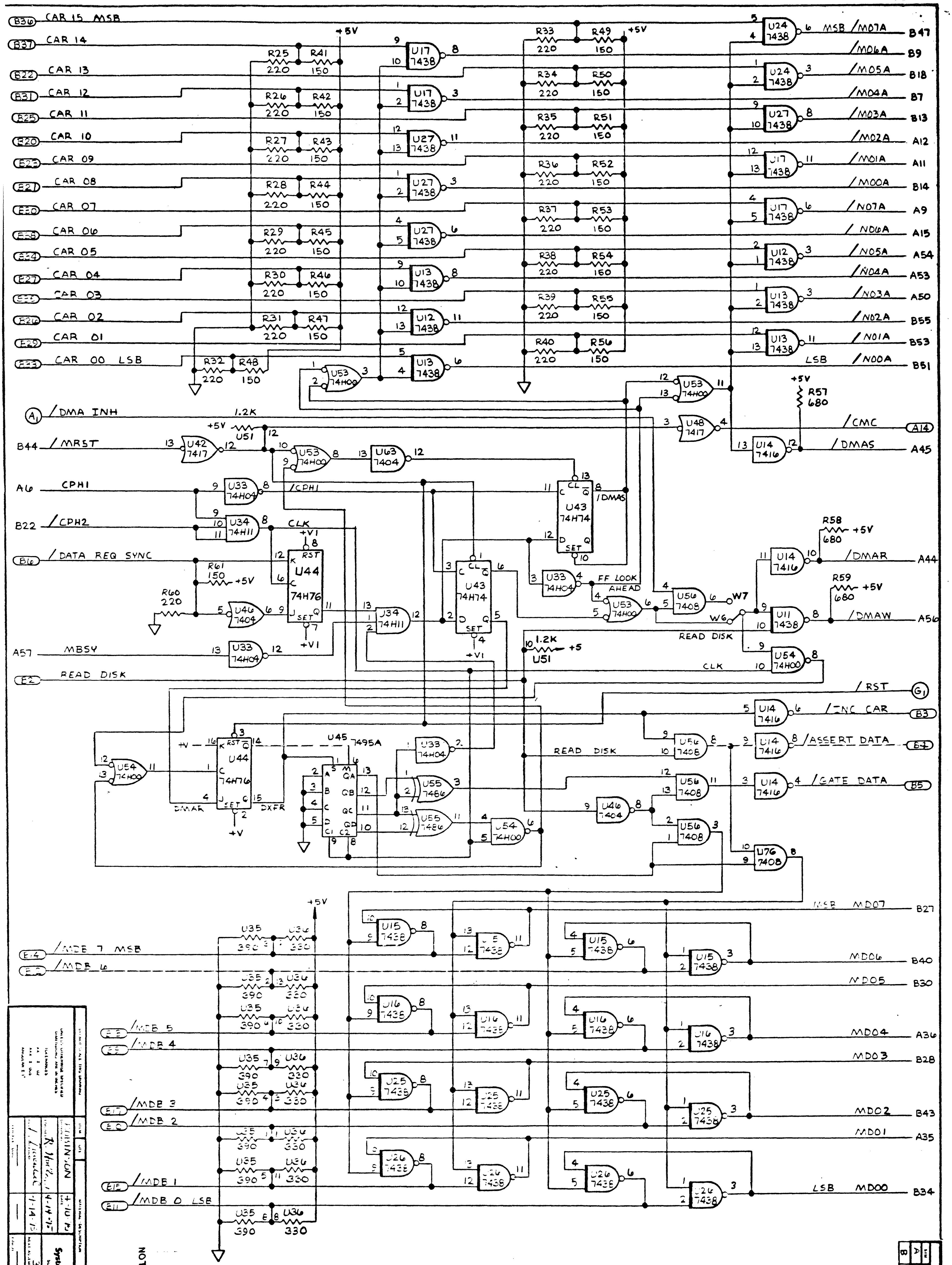
REVISIONS			
ITEM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	4-14-75	KF TST
B	PER PCO # 409	220.74	KF TST

DRAWN	ROBINSON	4-9-75
ENGINEER	K. Hall	4-14-75
PROJECT ENGINEER		4-11-75
MATERIAL		
FINISH		
TOLERANCES		

System Industries
SUNNYVALE CALIFORNIA

TITLE	SCHEMATIC IO & DMA INTERFACE
PART NUMBER	3020-6006
MASTER PART NO	3020-1004
MASTER DWG NO	D-3020-6006-4

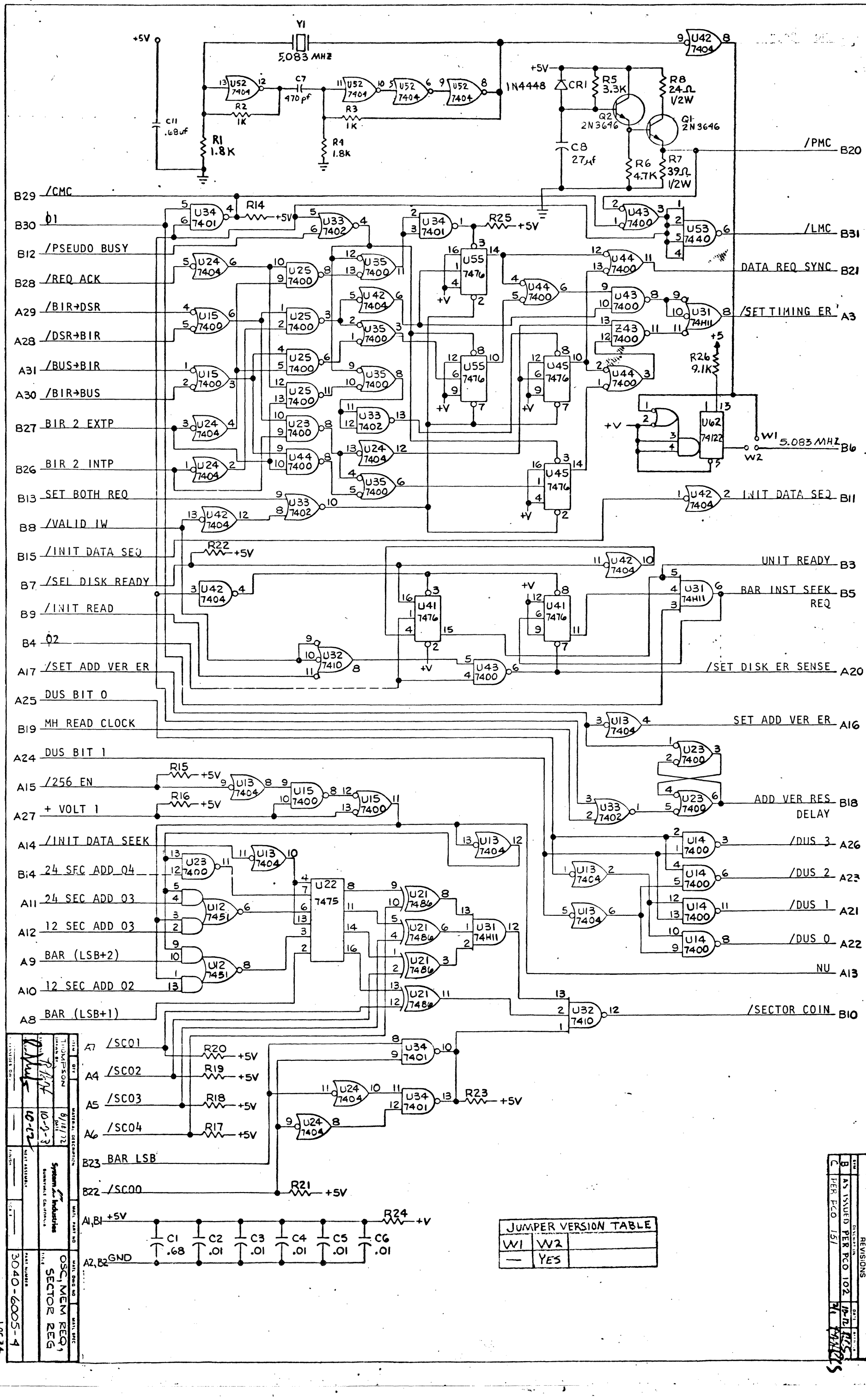
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE IN INCHES
XX ± .03
XXX ± .010
ANGULAR ± 1°



NOTES:
1. THIS LOGIC REPRESENTS ASSEMBLY 3020-6006 AT DATE CODE 608.

ROBINSON 4-10-75
R. Hart 4-14-75
1-14-75
System Industries
SUNNYVALE, CALIFORNIA
3020-7004
SCHEMATIC
IO & DMA INTERFACE
3020-6006
D-3020-6006-5

REVISIONS
A AS ISSUED 4-14-75 TST
B PER PCO #409 2-20-76 TST

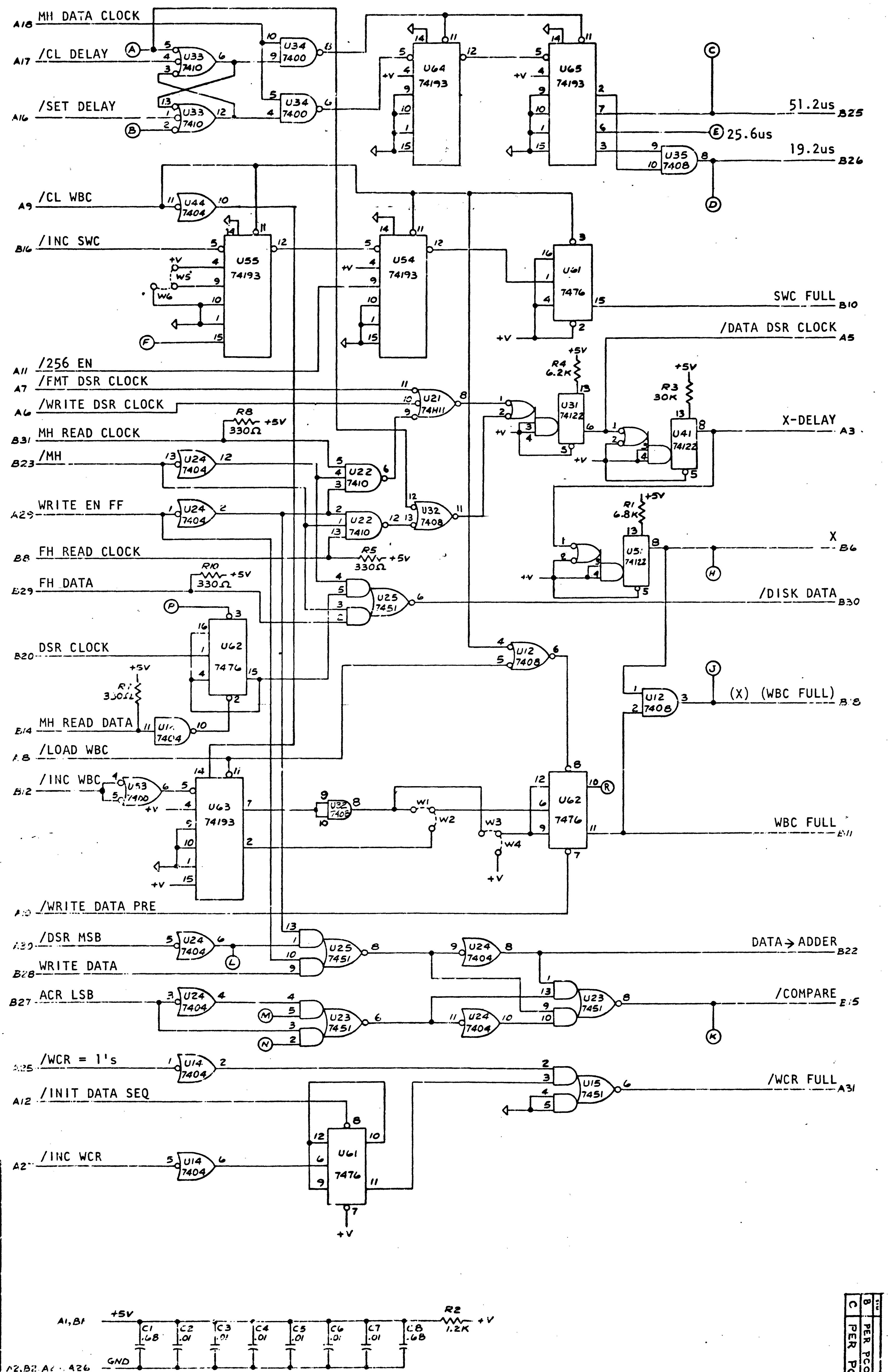


JUMPER VERSION TABLE		
W1	W2	
—	YES	

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
B	AS ISSUED PER PCO 102	10-17	RLS
C	PER PCO 151	11-2-73	RLS

DRAWN BY THOMPSON	DATE 8/14/72	SYSTEM INDUSTRIES SUNNYVALE CALIFORNIA	SIZE
CHECKED BY	DATE 10-2-72	MATERIAL DESCRIPTION	MASTER PART NO
ENGINEER DATE		NEXT ASSEMBLY	MASTER DWG NO
FUNCTION DATE			MASTER SPEC
		PART NUMBER 3040-6005-4	TITLE OSC, MEM REQ, SECTOR REG

LOC Z4



VERSION TABLE						
OPERATION	W1	W2	W3	W4	W5	W6
12 BITS	—	YES	YES	—	—	YES
16 BITS 128 OR 256 WDS/SEC	YES	—	—	YES	—	YES
16 BITS 120 WDS/SEC	YES	—	—	YES	YES	—

NOTE:
1. THIS LOGIC REPRESENTS ASSEMBLY 3040-6007 AT DATE CODE 516.

System Industries
SUNNYVALE, CA

LOGIC DIAGRAM
ADDRESS VARIFICATION
SEQUENCE

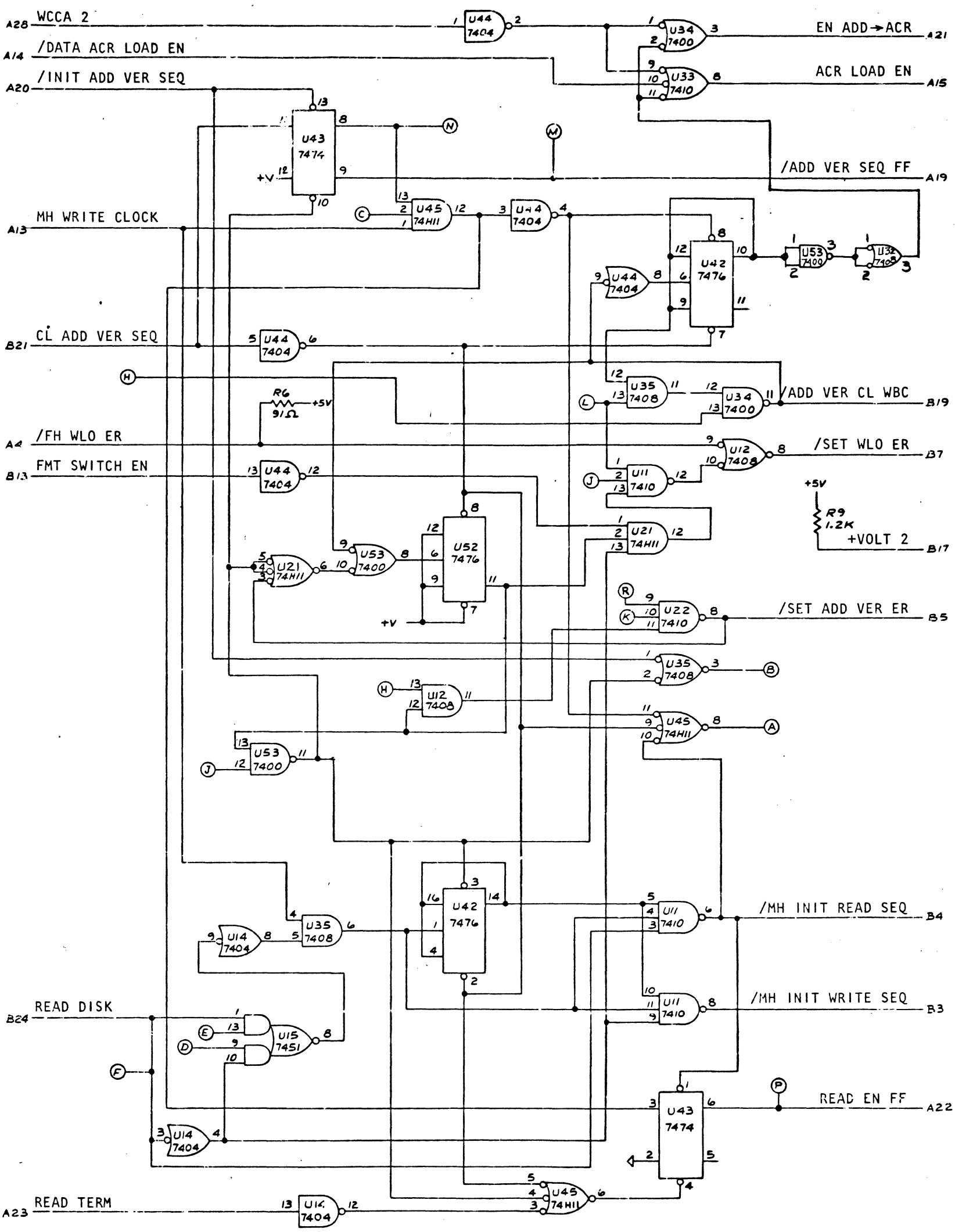
D-3040-6007-3

DRAWN 6/20/73
ENGINEER 9-24-73
RELEASED TO PROD 4-30-75

SHEET 1 OF 2

LOC 7.2

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
B	PER PCO 086	10-12	[illegible]
C	PER PCO 318, 323	4-75	[illegible]



NOTE:

1. THIS LOGIC REPRESENTS ASSEMBLY 3040-6007 AT DATE CODE 516.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
B	PER PCO 086	10-12-72	
C	PER PCO 318,323	4-75	

DRAWN BY	6/21/73	System 7 Industries	LOGIC DIAGRAM ADDRESS VERIFICATION SEQUENCE
ENGINEER	8-24-73		
RELEASE BY	4-30-75		D-3040-6007-4

SHEET 2 OF 2

LOC 2 2

C03 /READY TO S/R/W
R2 300Ω R3 120Ω +5V
A13 SUS (*)
A7 INIT SEEK
B4 BUSY→DISKS
A26 /LMC
A16 /PSEUDO BUSY
A22 Φ2
C34 /200TPI +5V R4 1.2K
C29 /ADD ACK
A6 TP-ADD ACK R5 300Ω R6 120Ω +5V
A24 ADD VER RES DELAY
C38 /SEEK INCOMPLETE R7 300Ω R8 120Ω +5V
C39 /LOGICAL ADD INTERLOCK R9 300Ω R10 120Ω +5V
B19 /DUS (*)
A4 SET ADD VER ER
C22 /WRITE CHECK
C13 /FILE READY
B20 MH WC+D
B25 /PMC
A5 WRITE EN FF
A3 READ EN FF
C02 /READ CLOCK
C05 /READ DATA
C15 /INDEX MARK
C14 /SECTOR MARK
C30 /SECTOR - BIT 16
C28 /SECTOR - BIT 8
C25 /SECTOR - BIT 4
C27 /SECTOR - BIT 2
C19 /SECTOR - BIT 1
R23 300Ω R24 120Ω +5V R25 300Ω R26 120Ω +5V
R13 300Ω R14 120Ω +5V R11 300Ω R12 120Ω +5V
R17 300Ω R18 120Ω +5V
R19 300Ω R20 120Ω +5V R21 300Ω R22 120Ω +5V
R27 300Ω R28 120Ω +5V W2 R29 1.2K +5V
R15 300Ω R16 120Ω +5V
R30 1.2K +5V R31 1.2K +5V
W1 R32 1.2K +5V
W5 W4
B12 DISK SELECT
A19 CYC ADD 8
A28 CYC ADD 7
A29 CYC ADD 6
A30 CYC ADD 5
B28 CYC ADD 4
B27 CYC ADD 3
B26 CYC ADD 2
B29 CYC ADD 1
B30 CYC ADD 0
B18 HEAD SELECT
+V R1 1.2K +V
A1 B7 +5V
A2 B2 GND
C1 .68 C2 .01 C3 .01 C4 .01 C5 .01 C6 .01 C7 C8 .01 C9 .01 C10 .01 C11 .01 C12 .68

U31 7404 U55 7400 U21 7408 U45 7474 U53 7400 U35 7474 U33 7438 U13 7438 U41 7400 U34 7401 U43 7410 U42 7408 U44 7474 U54 7438 U32 74157 U22 7404 U23 74175 U15 74175 U14 74175 U11 7438 U12 7438 U24 7438 U25 7438

/SSR-UNIT(*) READY A18
/SEL DISK READY B3
SSR-UNIT(*) BUSY ER A27
/SEEK SET DONE A17
SSR-UNIT(*) HDW ER B11
/RESTORE C35
/256 EN B10
/ADDRESS STROBE C31
LOG ADD INT B22
SEEK INCOMPLETE B21
WRITE CHECK B24
FILE NOT READY B23
/WRITE DATA+CLOCK C04
/WRITE GATE C21
/ERASE GATE C09
/READ GATE C07
MH READ CLOCK A15
MH READ DATA B6
TP-/INDEX B5
TP-/SECTOR B8
/MH B7
/SC04 A11
/SC03 A8
/SC02 A12
/SC01 A9
/SC00 A10
/DISK SELECT C37
/CA8 C26
/CA7 C36
/CA6 C18
/CA5 C10
/CA4 C23
/CA3 C16
/CA2 C06
/CA1 C33
/CA0 C08
/HEAD SELECT C17

C01 C11 C12 C20 C24 C32 C40

VERSION TABLE			
OPERATION	W1	W2	W3
12 S/T	YES	YES	YES
16 S/T	YES	—	YES
24 S/T	—	—	—

DISK SELECT TABLE		
DISK SELECT	W4	W5
STANDARD	YES	—
REMOVABLE PLATTER - UNIT 0	—	YES

NOTES:
1. THIS LOGIC REPRESENTS ASSEMBLY 3041-6001 AT DATE CODE 525.

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	6-22-76	RLS
B	PER PCO 140	11-4-76	RLS
C	PER PCO 474	6-76	RLS

DRAWN BY	DATE	MATERIAL DESCRIPTION	ITEM
ENGINEER	6/26/75		QTY
MILITARY SPEC	9-24-75		
—	6127		
NEXT ASSEMBLY	System Industries. SUNNYVALE CALIFORNIA		MATL PART NO
—			MATL DWG NO
PART NUMBER 3041-6001-3	TITLE 3040 DIABLO INTERFACE		MATL SPEC
	3041-6001		

LOC (*)

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	AS ISSUED	4-75	

PROGRAM I/O DATA BUS

BUFFER DATA BUS

BUFFER ADDRESS BUS

GENERAL BUF REG 8

SEEK ADDRESS REG 16

BLOCK ADDRESS REG 16

CONTROL & ERROR REG 16

WORD COUNT REG 16

CURRENT ADDRESS REG 15

BUFFER INTERFACE REG #1 16

BUFFER INTERFACE REG #2 16

CFF

CO

Σ

CI

DATA SHIFT REG 16

ARITHMATIC CHECK REG 16

÷12, ÷24 NETWORK

SECTOR REG 5

COMPARE

COINCIDENCE

DISK SELECT (1)

CYLINDER ADDRESS (9)

HEAD SELECT (1)

UNIT X-TRACK ADDRESS REG 9

UNIT X-SECTOR COUNTER 5

UNIT X-SEEK STATUS REG 3

TRACK ADDRESS

INDEX PULSE

SECTOR PULSE

DATA FROM DISK

DATA TO DISK

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SRC

DRAWN BY T. DOOM	DATE 4-75	System Industries SUNNYVALE CALIFORNIA	3040 CONTROLLER BLOCK DIAGRAM 8 BIT
ENGINEER [signature]	4-16-75		
RELEASED TO PROD [signature]	4-16-75	NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG		FINISH SCALE	B-3050-9006-1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	4/5/75	

COMPUTER I/O BUS

COMPUTER INTERFACE

PROGRAM I/O DATA BUS
BUFFER DATA BUS
BUFFER ADDRESS BUS
READ CONTROL & ERROR REGISTER U OR L
READ SEEK STATUS REGISTER U OR L
READ BLOCK ADDRESS REGISTER U OR L
ENTER CONTROL & ERROR REGISTER L
INITIATE OVERLAP SEEK
INITIATE WORD COUNT/CURRENT ADDRESS SEQ
INITIATE READ SEQUENCE
INITIATE WRITE SEQUENCE
ENTER SEEK ADDRESS REGISTER
ENTER GENERAL BUFFER REGISTER
MASTER CLEAR
DATA REQUEST ACKNOWLEDGE
BUFFER ADDRESS→BUS
INCREMENT CURRENT ADDRESS REGISTER
BUFFER INTERFACE REGISTER→BUS
BUS→BUFFER INTERFACE REGISTER
DATA REQUEST SNYC
READ DISK ENABLE
OPERATION COMPLETE

COMMON CONTROLLER

+5V POWER SUPPLY

CYLINDER ADDRESS LINES (9)
HEAD SELECT
DISK SELECT
SEEK UNIT SELECT X
INITIATE SEEK
SECTOR ADDRESS COUNTER (4)
MH/FH ENABLE
128/256 WORDS PER SECTOR ENABLE

READ ENABLE
DATA UNIT SELECT X
WRITE ENABLE
WRITE DATA & CLOCK
PERIPHERAL MASTER CLEAR
MH READ CLOCK
MH READ DATA
FILE NOT READY/THERE
LOGICAL ADDRESS INTERLOCK
SEEK INCOMPLETE
WRITE CHECK
(DUS)(UNIT READY TO SEEK/READ/WRITE)
SET DONE
SSR - UNIT READY TO SEEK/READ/WRITE
SSR - BUSY ERROR
SSR - HDW ERROR
(BUSY)(DATA UNIT SELECT)
PSEUDO BUSY
Φ2
LOGIC MASTER CLEAR
ADDRESS VERIFICATION ERROR
ADDRESS VERIFICATION RESTORE DELAY
FH WRITE CLOCK
FH WRITE BUSY
WRITE DATA
FH READ CLOCK
FH READ BUSY
FH DATA
INITIATE READ
INITIATE WRITE
OP COMPLETE + MASTER CLEAR
FH WRITE LOCKOUT

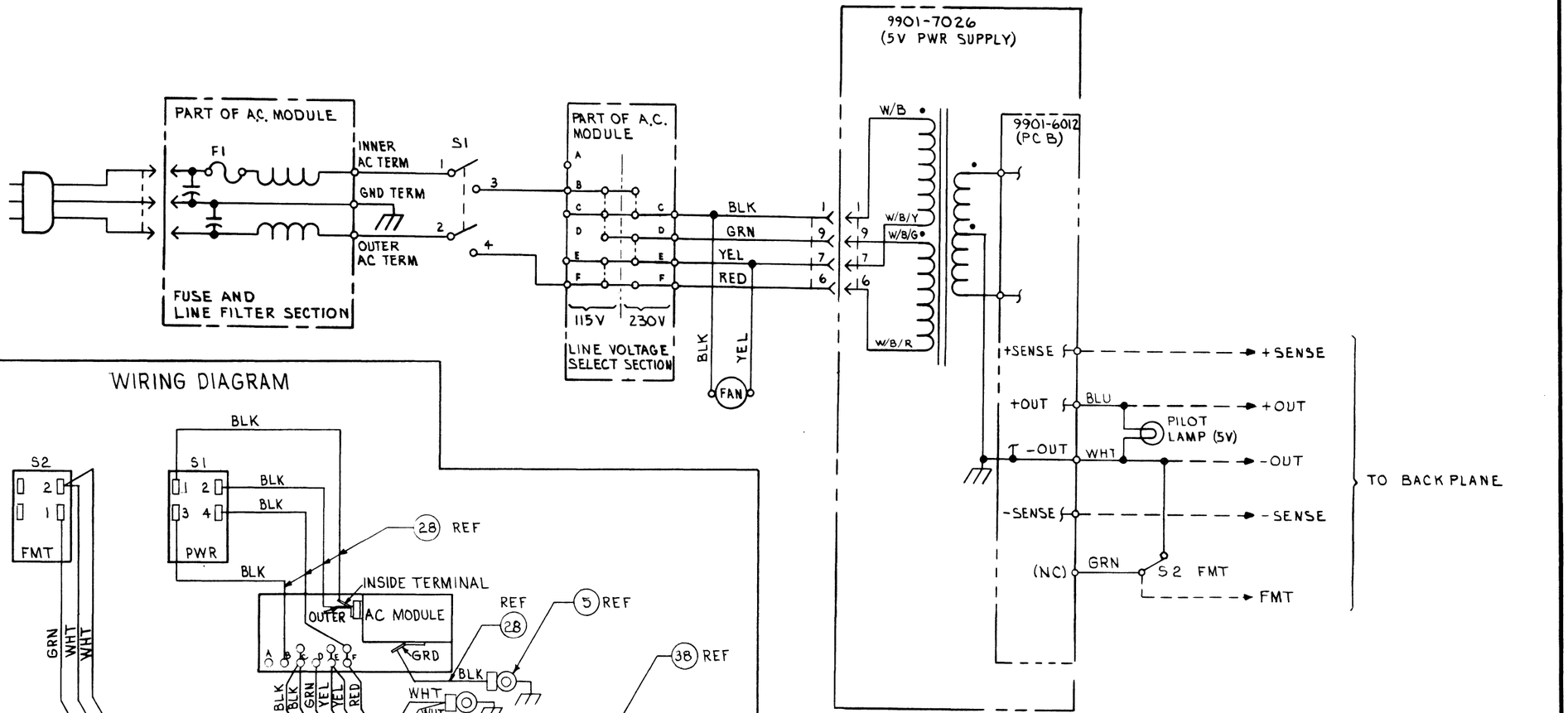
PERIPHERAL INTERFACE

UNIQUE FIXED HEAD SIGNALS

DISK CABLE

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
DRAWN BY: T. DOOM	DATE: 4-75	System Industries SUNNYVALE CALIFORNIA		3040 FUNCTIONAL INTERFACE 8 BIT	
ENGINEER: [illegible]	DATE: 4-16-75	NEXT ASSEMBLY		TITLE	
ENGINEERING GROUP: T. Trussell	DATE: 4-16-75			PART NUMBER	
SUPERSEDES DWG		FINISH	SCALE	B-3050-9007-1	

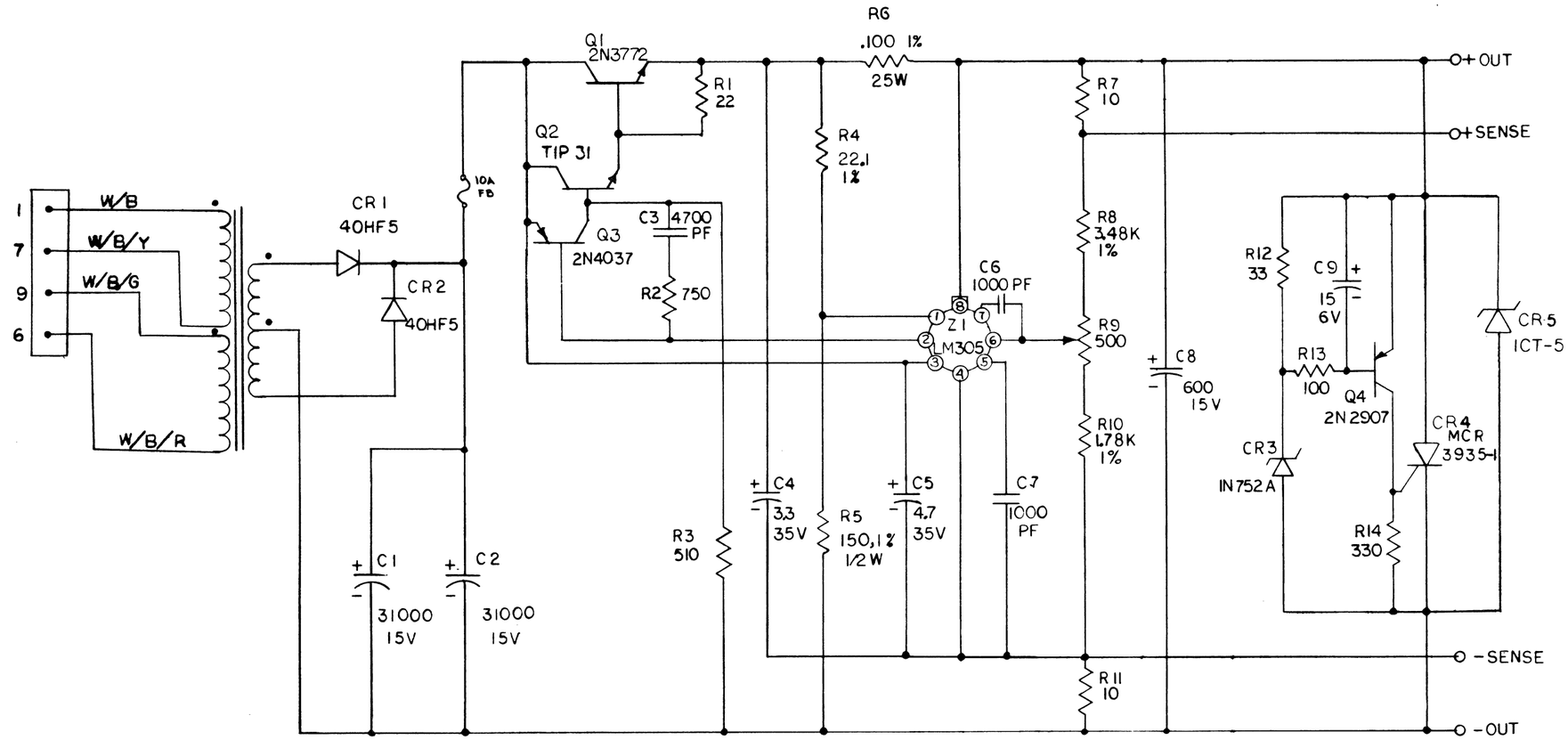
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED PER PCO 498	11-9-76	



DO NOT SCALE THIS DRAWING	ITEM	QTY	MATERIAL-DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES xx ± 02 xxx ± 005 ANGULAR ± 1°	DRAWN BY Ron Doom 10-76 DATE		System X Industries SUNNYVALE, CALIFORNIA		AC WIRING DIAGRAM & SCHEMATIC, 3010/ 3040 CONTROLLERS	
	ENGINEER B. Yamada 11-9-76				TITLE	
	RELEASE TO PROD A. Khanbaba 11-9-76		NEXT ASSEMBLY		3010-7001	
	SUPERSEDES DWG		FINISH	SCALE	PART NUMBER C-3010-7001-4	

SHEET 1 OF 1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	12-2-71	CSM
B	SCHEMATIC RE DESIGN (PCO-008)	11-23-71	

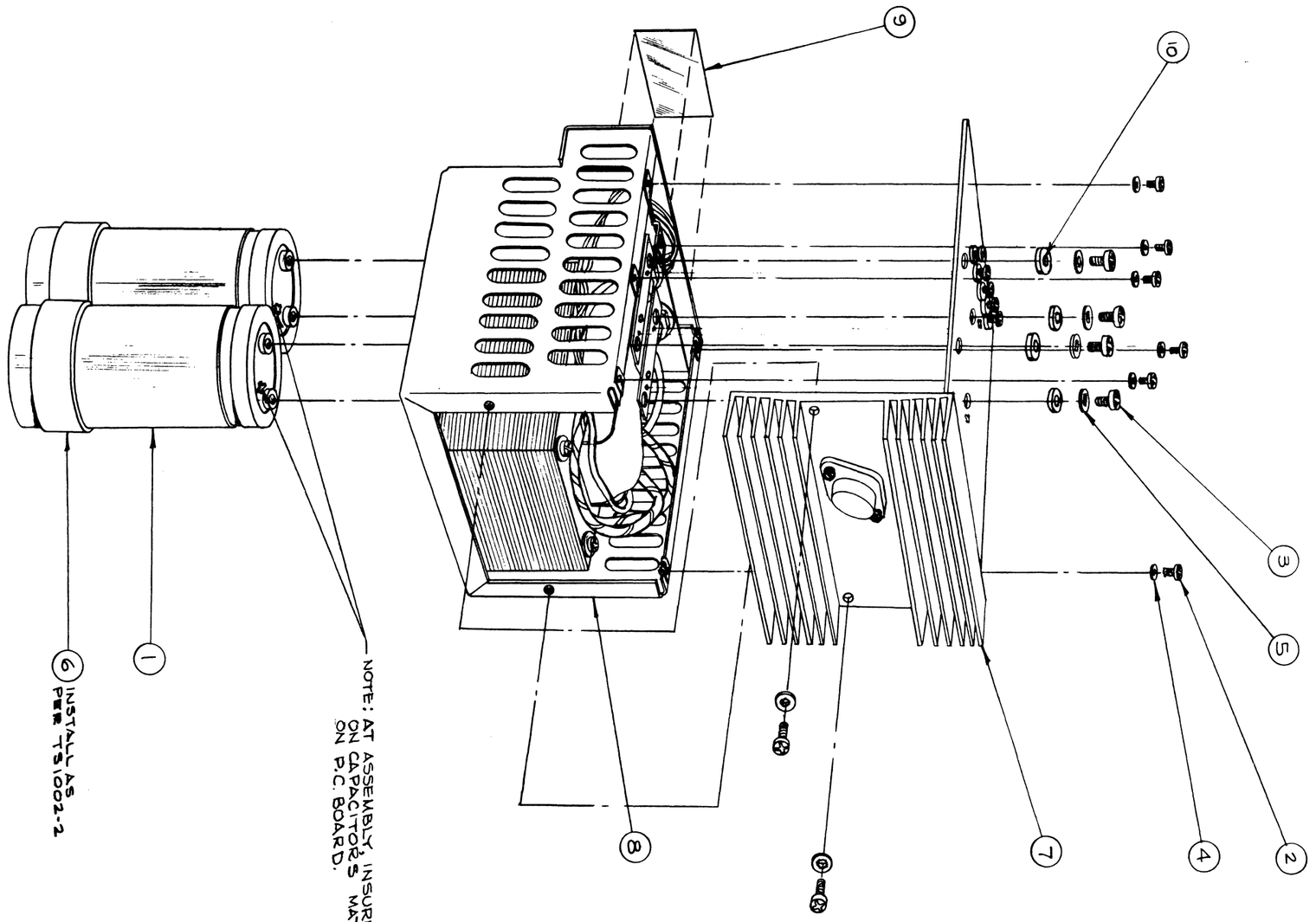


DO NOT SCALE THIS DRAWING	ITEM	QTY.	MATERIAL - DESCRIPTION	MATL. PART NO.	MATL. DWG. NO.	MATL SPEC.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .xx ± .02 .xxx ± 005 ANGULAR ± 1°						

DRAWN BY M. HIJMANS	1-18-71 DATE	System Industries SUNNYVALE, CALIFORNIA	5 VOLT POWER SUPPLY SCHEMATIC (TITLE)
ENGINEER	4-16-71		
CSM RELEASE TO PROD.	4-23-71	9901-7026 NEXT ASSEMBLY	9901-7026 PART NUMBER
SUPERSEDES DWG.		FINISH —	SCALE — C-9901-6012-8

SHEET 1 OF 1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	AS ISSUED	4-23-71	CSM
B	SEE PCO #027	2-28-72	



6 INSTALL AS PER TS 1002-2

NOTE: AT ASSEMBLY, INSURE POLARITY (+) SIGNS ON CAPACITORS MATCH POLARITY (+) SIGNS ON P.C. BOARD.

DO NOT SCALE THIS DRAWING	ITEM	QTY.	MATERIAL - DESCRIPTION	MATL PART NO.	MATL DWG. NO.	MATL SPEC.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX ± .02 .XXX ± .005 ANGULAR ± 1°					5 V POWER SUPPLY ASS'Y	
DRAWN BY A.P	12 MAR 71 DATE		System Industries SUNNYVALE, CALIFORNIA		TITLE	
ENGINEER ALBERTO PREZ	12 MAR 71				9901-7026	
RELEASE TO PROD. CSM	4-23-71		NEXT ASSEMBLY		PART NUMBER	
SUPERSEDES DWG.			FINISH	SCALE NONE	C-9901-7026-1	

SHEET 1 OF 1

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
Ø1																A29	B30	B16	B7
(Ø1)(WCCA DONE)									A12	A12								A7	
Ø2	A22	A22	A22	A22				A12						A28		B28	B4	B13	B11
ØIE																B8		B22	
12 SEC ADD 02												B4					A10		
12 SEC ADD 03												B3					A12		
19.2 us															B26	B9			
24 SEC ADD 03												A7					A11		
24 SEC ADD 04												A6					B14		
/256 EN	B10	B10	B10	B10											A11		A15		
5.083 MHZ																	B6	A29	
51.2 us														B25	B25				
/304024 SEL											A4	B14							
Σ							A30											A27	
/AC00					A26							B28							
/AC01					A21							B29							
/AC02					A22							B30							
/AC03					A25							B31							

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/AC04					B19							B21							
/AC05					A16							B22							
/AC06					A15							B23							
/AC07					B18							B24							
/AC08					A31						B28								
/AC09					B13						B29								
/AC10					A11						B30								B27
/AC11					B25						B31								B14
/AC12					B20						B21								B22
/AC13					B12						B22								A31
/AC14					A9						B23								B26
/AC15					A10						B24								B15
ACR 04									A28	A30									
ACR 08								A28	A30										
ACR 12							A28	A30											
ACR CLOCK							A29	A29	A29	A29								A19	
ACR LOAD EN							A31	A31	A31	A31					A15				

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/(ACR LOAD EN)(WEN)							A15			A17									
ACR LSB										A28				B13	B27			A26	
/ADD→BUS						A3												A16	
/ADD→IB						B26	A22	A22	A22	A22									
/ADD VER CL WBC														A24	B19				
ADD VER RES DELAY	A24	A24	A24	A24													B18		
/ADD VER SEQ FF														B19	A19				
BAR 03										A26		B27							
BAR 04									A25			A20							
BAR 05									A27			A19							
BAR 06									B26			B19							
BAR 07									A26		A26	B13							
BAR 08								A25			B25 B10	B25							
BAR 09								A27			B7								
BAR 10								B26			A27								
BAR 11								A26			B27								
BAR 12							A25				A20								

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																	
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
BAR 13							A27				A19								
BAR 14							B26				B19								
BAR INST SEEK REQ																	B5		B13
BAR LSB										A25		B10					B23		
BAR (LSB+1)										A27		B7					A8		
BAR (LSB+2)										B26		A27					A9		
/BIR→BUS						A27											A30	B28	
/BIR→DSR														B9			A29	B27	
BIR 2 EXTP																	B27	B23	
BIR 2 INTP							B8	B8	B8	B8							B26	B24	
/BUS→BIR						B25										A20	A31	A28	
BUSY→DISKS	B4	B4	B4	B4															A10
CAR 00						A21				A20 B14									
CAR 01						B15				A9									
CAR 02						B14				B28									
CAR 03						A24			B29	B25									
CAR 04						B13			A20 B14										

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																		
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
CAR 05						A25			A9										
CAR 06						A26			B28										
CAR 07						A18		B29	B25										
CAR 08						A20		A20 B14											
CAR 09						A16		A9											
CAR 10						B5		B28											
CAR 11						A13	B29	B25											
CAR 12						B16	A20 B14												
CAR 13						A19	A9												
CAR 14						B18	B28												
CAR 15						B21	B25												
CL ADD VER SEQ															B21	B31			
/CL DELAY															A17	A3			
/CL ERROR REG							A8	A8	A8	A8									A30
/CL WBC														A21	A9				
/CMC					A27												B29		
/COMPARE														A15	B15				

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/COMP IR					B11				A19										
/COMP IW					A4					A19									
CYC ADD 0	B30	B30	B30	B30								B5							
CYC ADD 1	B29	B29	B29	B29								B26							
CYC ADD 2	B26	B26	B26	B26								A3							
CYC ADD 3	B27	B27	B27	B27								B20							
CYC ADD 4	B28	B28	B28	B28								A4							
CYC ADD 5	A30	A30	A30	A30							A5								
CYC ADD 6	A29	A29	A29	A29							B6								
CYC ADD 7	A28	A28	A28	A28							B3								
CYC ADD 8	A19	A19	A19	A19							A3								
DATA→ADDER														A27	B22			A25	
/DATA ACR CLOCK														B29		A15			
DATA ACR LOAD EN										A15 A14									
/DATA ACR LOAD EN										A13				B27	A14				
/DATA DSR CLOCK								A16							A5			A23	
DATA INC WCR														B3				A13	

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																		
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/DATA OP COMP																A5			B29
DATA REQ SYNC						A5											B21		A17
/DATA SET WEN									A16					B26					
/D+FHD ACR CLOCK																A12		A18	
/DISK DATA							B15								B30				
/DISK ERROR																A10		A14	
DISK SELECT	B12	B12	B12	B12			A26				B13								
/DSR 04									B10	B15									
/DSR 08								B10	B15										
/DSR 12							B10	B15											
/DSR→BIR														A6			A28	B31	
DSR CLOCK							B9	A17/B9	B9	B9					B20				
DSR LOAD EN							B16	B16	B16	B16						A31			
/DSR LSB										B10				B12					
/DSR MSB							B11								A30				
/DUS 0	B19																A22		
/DUS 1		B19															A21		
/DUS 2			B19														A23		

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																	
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/DUS 3				B19													A26		
DUS BIT 0																	A25		A19
DUS BIT 1																	A24		A20
EN ADD→ACR							A24	A24	A24	A24					A21				
/EN BIR 1L→BUS						B27			B20	B20									
/EN BIR 2L→BUS						B30			A21	A21									
/EN BIR 1U→BUS						B28	B20	B20											
/EN BIR 2U→BUS						B29	A21	A21											
EN SAR→÷											A8	A8							A8
/ENTER C & E REG					B9														B3
FH DATA	A25	A25	A25	A25											B29				
/FH DELAYED ACR CLOCK								A11								B17			
/FH INIT								A15 A19	A15					B11		B13			
FH READ BUSY	A21	A21	A21	A21										B18					
FH READ CLOCK	B14	B14	B14	B14											B8				
FH+W DSR LOAD EN							A13 A17												

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																			
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/FH+W DSR LOAD EN							A14									A30			
/FH WLO ER	A20	A20	A20	A20											A4				
FH WRITE BUSY	A23	A23	A23	A23										B21					
FH WRITE CLOCK	B13	B13	B13	B13										B30					
FILE NOT READY	B23	B23	B23	B23														A9	
FMT BIR→DSR														B8		B26			
FMT+DISK+TIMING ER																A8			B25
/FMT DSR CLOCK															A7	B30			
FMT EN FF																B20			A27
/FMT INC WBC														A12		B3			
/FMT INC WCR														A13		B18		A20	
FMT SEQ FF														B14		B22			
/FMT SET WEN																B4		A21 A31	
FMT SWITCH EN	A31														B13				B30
/GATE→BIR 1						A28												B30	
/GATE→BIR 2						A29												B25	
/GATE→BIR 1L						A23			B4	B4									
/GATE→BIR 2L						B20			B5	B5									

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/GATE→BIR 1U						B23	B4	B4											
/GATE→BIR 2U						B19	B5	B5											
HEAD SELECT	B18	B18	B18	B18								B6							
/IB 00					B30						A13	A13							
/IB 01					B28		A4	A5			A15	A15							
/IB 02					B29			A6	A4		A11	A11							A25
/IB 03					B27				A5	A4	A12	A12							A21
/IB 04					A30				A6	A6	A16	A16							A18
/IB 05					A28		A5				A17	A17							A28 A26
/IB 06					A29		A6	A4			A18	A18							
/IB 07					B26						B18	B18							A23
/INC BAR												A26				B23			B12
INC CAR										B29								A17	
/INC SWC														B20	B16				
/INC WBC														A11	B12				
/INC WCR										B24					A27			A15	
/INIT ADD VER SEQ															A20	B12			

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																		
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/INIT DATA SEEK														A23		A19	A14		A6
INIT DATA SEQ																	B11	B10	
/INIT DATA SEQ					A7										A12	B24	B15		
/INIT OVERLAP SEEK					A6														B10
/INIT READ									A11								B9	A12	B28
INIT SEEK	A7	A7	A7	A7															A7
/INIT WRITE										A11									A16
/IR SEQ	B17	B17	B17	B17										A25		A16			
/IWCCA SEQ					B10	A30												B11	B20
/IW SEQ	B16	B16	B16	B16										A26		A14			
/LMC	A26	A26	A26	A26												A21	B31		A4
LMC+OP COMP	B15	B15	B15	B15										B16		A22		A11	
/LOAD BAR											A25	A25						B9	
/LOAD CAR							B27	B27	B27	B27								B15	
/LOAD SAR					A5						A9	A9							
/LOAD WBC														A14	A8				
/LOAD WCR							B30	B30	B30	B30								B6	
LOG ADD INT	B22	B22	B22	B22														B8	

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																	
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/MD 0						B3		B13		B13									
/MD 1						A10		A10		A10									
/MD 2						A6		B21		B21									
/MD 3						A14		B19		B19									
/MD 4						A8	B13		B13										
/MD 5						B9	A10		A10										
/MD 6						B11	B21		B21										
/MD 7						B7	B19		B19										
/MDB 0						B4		B18		B18									
/MDB 1						A11		B22		B22									
/MDB 2						A7		B23		B23									
/MDB 3						A15		B31		B31									
/MDB 4						A9	B18		B18										
/MDB 5						B8	B22		B22										
/MDB 6						B10	B23		B23										
/MDB 7						B6	B31		B31										
MH														A30		B29			

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/MH	B7	B7	B7	B7										B17	B23	B15		B7	B16
MH DATA CLOCK														B15	A18	B14		B19	
/MH INIT READ SEQ															B4	A17			
/MH INIT WRITE SEQ															B3	A13			
MH READ DATA	B6	B6	B6	B6											B14				
MH READ CLOCK	A15	A15	A15	A15											B31		B19		
MH WC+D	B20	B20	B20	B20														B17	
MH WRITE CLOCK														B24 B31	A13	B16		B20	
/PMC	B25	B25	B25	B25													B20		
PSEUDO BUSY								A13								B25			B8
/PSEUDO BUSY	A16	A16	A16	A16				A14									B12		
RO											B4	A14							
/R2											A6	A5							
/READ BAR L					B4							A10							
/READ BAR U					B3						A10								
/READ C & E REG L					B8														A15
READ C & E REG U					B14														A5

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																	
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/READ C & E REG U					B6		B3	B3	B3	B3									
READ DISK						A4	B12	B12	B12	B12					B24	B21			A24
READ EN FF	A3	A3	A3	A3											A22				
/READ OP COMP														A7					A11
/READ REINIT														A8					B23
/READ SEEK STATUS REG L					B5							B8							
/READ SEEK STATUS REG U					B7						B8								
READ TERM														A9	A23				
/REQ ACK						B24											B28		
/R OR W SEQ INIT														A29				A24 A22	
SAR 14											B20								B31
SAR 15											B26								B21
/SC00	A10	A10	A10	A10													B22		
/SC01	A9	A9	A9	A9													A7		
/SC02	A12	A12	A12	A12													A4		
/SC03	A8	A8	A8	A8													A5		
/SC04	A11	A11	A11	A11													A6		

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																		
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/SECTOR COIN																B27	B10		
SEEK INCOMPLETE	B21	B21	B21	B21														A8	
/SEEK SET DONE	A17	A17	A17	A17												A6			
/SEL DISK READY	B3	B3	B3	B3													B7		
/SET ADD VER ER										A7					B5		A17		B17
SET ADD VER ER	A4	A4	A4	A4													A16		
SET BOTH REQ																	B13	B14	
/SET DELAY															A16	B5			
/SET DISK ER SENSE																	A20	B4	
/SET DISK SEL ER								A3										A6	
/SET FMT ER																A11			A29
/SET LAI ER										A3								A10	
/SET PARITY ER								A7						A16					B19
/SET SEEK INC ER									A7									B5	
/SET TIMING ER							A7									A9	A3		
/SET WLO ER							A3								B7				B18
SET WRITE EN									A13 A17										

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
/SET WRITE EN									A14							B7			
/SET WRITE CHK ER									A3									A5	
/SET DONE					B31											A7			
SSR-UNIT 0 BUSY ER	A27											B9							
SSR-UNIT 1 BUSY ER		A27										B17							
SSR-UNIT 2 BUSY ER			A27								B9								
SSR-UNIT 3 BUSY ER				A27							B17								
SSR-UNIT 0 HDW ER	B11											B12							
SSR-UNIT 1 HDW ER		B11										B16							
SSR-UNIT 2 HDW ER			B11								B12								
SSR-UNIT 3 HDW ER				B11							B16								
/SSR-UNIT 0 READY	A18											B11							
/SSR-UNIT 1 READY		A18										B15							
/SSR-UNIT 2 READY			A18								B11								
/SSR-UNIT 3 READY				A18							B15								
SUS 0	A13																		B4
SUS 1		A13																	B6

MODEL 3050 DISK CONTROLLER	PC BOARD LOCATION																	
	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
BUS 2			A13																B5
BUS 3				A13															A9
BWC FULL														A4	B10				
/TERMINATE														B4		B19			
UNIT READY																A28	B3		
/VALID IW																A18	B8	B12	A12
+VOLT 1																	A27	B26	
+VOLT 2														A17 A18 A19 A20	B17				B24
WBC FULL														B7	B11	B10			
WCCA 2							A23	A23	A23	A23					A28			B3	
WCR 03									B24	B17									
WCR 07								B24	B17										
WCR 11							B24	B17											
/WCR=1's															A25	A27			
WCR 0-3=1's							B7									A26			
WCR 4-7=1's								B7								A25			

MODEL 3050
DISK CONTROLLER

PC BOARD LOCATION

	X1	X2	X3	X4	X5	X7	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Z1	Z2	Z3	Z4	Z5	Z6
WCR 8-11=1's									B7							A24			
WCR 12-15=1's										B7						A23			
/WCR FULL														A3	A31				A13
/W DSR LOAD EN							A16							A10					
WRITE CHECK	B24	B24	B24	B24														A3	
/WRITE CL DELAY														B28		A4			
WRITE DATA	B31	B31	B31	B31										B6	B28			B18	
/WRITE DATA PRE														B5	A10				
/WRITE DSR CLOCK														A31	A6				
WRITE EN FF	A5	A5	A5	A5						A16					A29	B6		A4	
WRITE TERM																B11			A14
X														A22	B6				
X-DELAY														B10	A3				
(X)(WBC FULL														B23	B18				

GLOSSARY

Address Verification	At the beginning of each sector is a block address word. When a sector is to be used, the disk controller can verify that it has the right track by first reading the block address word and comparing it with the number of the block required. There is a disk formatting program to initially address the sectors.
Arithmetic Check Register	It is in this register that the Cyclic Redundancy Check Word is generated. During a write operation the Check Word is generated and written at the end of the data. During a read operation a Check Word is generated and compared to the one read at the end of the data to verify the correctness of the data transfer.
Block Address Register	This register contains the block number of the sector that the controller is now operating on.
Block Address Word	At the beginning of each sector is a block address word that is written there for the disk controller to use for address verification.
Block Number	The block number is the sequential, contiguous numbering scheme which has a one-for-one correspondence with the track and sector numbers.

Buffer Interface Register	Two registers that are the link between the Data Shift Register and the Computer. Two registers are employed so that one can be transferring data to/from the Data Shift Register while the other is transferring data from/to the computer. If the double buffer approach were not used, the word just shifted into the Buffer Interface Register would have to be transferred into the computer by the time the Data Shift Register is filled again. This timing requirement cannot always be met. The double buffering approach allows the computer twice the amount of time to respond to the presence of data to be transferred.
Control and Error Register	A register containing the control information such as Interrupt Enable, Port Select, Busy Indicator, and Done Indicator, and the error indicators such as Illegal Operation Flag, Select Error Flag, Address Verification Flag, Parity Error Flag. This register can be loaded or read by program control.
Current Address	The core memory address for the word being transferred during a disk operation.
Current Address Register	A register in the disk controller that holds the core memory address for the word being transferred. It is incremented after each transfer occurs.

Cyclic Redundancy Check Word	This is a word generated by the controller at the time a sector is written onto the disk. When the sector is read the data read operation is checked by comparing the Check Word just read from the disk to the one the controller creates as it is reading the data. If the two compare when the read operation is successful. If not, then the error is noted by setting a flag in the Control and Error Register.
Cylinder Number	A number which refers to the cylinder on a disk where a disk operation will take place.
Data Shift Register	A register in the disk controller that is the link between the disk pack and the Buffer Interface Registers. It operates in a serial fashion when transferring data between the disk and itself, and operates in a parallel fashion when transferring data between the Buffer Interface Registers and itself.
Direct Memory Access (DMA)	The Model 3040 Systems utilize the direct memory access facility of the minicomputer. This is a direct line between the minicomputer's memory and the disk system. The disk controller steals memory cycles from the computer and transfers data between the memory and the disk controller. This eliminates the need for the CPU to watch over the entire operation.

Disk Formatting Program	A program that initializes the disk pack. One of its functions is to write the block address word at the beginning of each sector.
Double Buffering	Double Buffering is providing two registers to act as links between the computer and the disk controller. One can be transferring data to/from the disk drive while the other is transferrring data from/to the computer. This allows the computer more flexible timing requirements in picking up data from the disk.
Interrupt Generation	An interrupt is generated whenever interrupts are enabled, (the interrupt enable bit in the Control and Error Register is set) and one of two conditions is present. The two conditions are: the done flag in the Control and Error Register or Status Register is set and it is the end of a data transfer operation; or the done flag in the Control and Error Register or Status Register is set, and it is the completion of and overlap seek with no data transfer operation in progress.
Latency	The time spent waiting for the disk to rotate beneath the read/write head until the head is positioned at a spot to begin transferring the data.
Overlap Seek	The process of having one or more drives on three of the controllers ports executing seek operations while

	the fourth port is performing a read or write operation.
Read/Seek	Combining the head-positioning seek operation with the data-acquiring read operation reduces the number of instructions required for a data transfer. The CPU can start the transfer operation and then ignore the process until it is completed.
Sector Number	A number which refers to the sector in a disk where a disk operation will take place.
Seek Address Register	This register contains the information needed by the controller to execute a seek operation: the port number and the cylinder to which the drive is to seek.
Seek Status Register	A register that contains information pertaining to possible errors while attempting to complete a seek operation. The register is broken into four parts, one for each port of the controller. Each port contains three bits corresponding to three possible error conditions.
Track Number	A number which refers to the track on a disk where a disk operation will take place. The track number is contained in block number (when a block addressing scheme is used) and may be found by either extracting a specific field from the block number of using a divide network

on the block number.

Word Count	The number of data words to be transferred in a disk operation.
Word Count/Current Address Sequence	The word count/current address approach to data transfer enables the transfer of large blocks of data with just a single sequence of I/O instructions. Such large transfers are performed using this approach without tying up the computer while the data transfer operations are taking place. This sequence is initiated with a single computer instruction that passes a CPU memory location to the disk controller. That location is the first of two CPU memory locations that contain the word count and current address parameters respectively.
Word Count Register	A register in the disk controller that stores the number of words remaining to be transferred during a disk operation. It is updated as the transfer of each word takes place.
Write Protection	Any sector on a disk may be write-protected by having a write-protect indicator set in its Block Address Word by a special disk formatting program. Any write operation attempted on this sector will result in a write lockout error and the write operation will be terminated.

Write/Seek	Combining the head-positioning seek operation with the data-writing write operation reduces the number of instructions required for a data transfer. The CPU can start the transfer operation and then ignore the process until it is completed.

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European Offices:

SI Computer Systems, Inc.
Guildford Road
Woking, Surrey
England GU22 7HB
Phone: (04862) 5077
Telex: 859124

System Industries (Deutschland) GmbH
AM Forsthaus Gravenbruch 9-11
D. 6078 Neu Isenburg, 2,
West Germany
Phone: 6102-5464
Telex: 417606

System Industries, Inc.
Grev Magnigatan 5,
S114 55 Stockholm
Sweden
Phone: 08/63 62 74
Telex: 12697