SYSGEN™ SC4000

INTELLIGENT TAPE CONTROLLER

PRODUCT SPECIFICATION

NOTE: All specifications are subject to change without notice.

REV	DESCRIPTION	DATE	CHNG	APPV
	P R E L I M I N A R Y	3/15/83	KLP	
	R E L E A S E D	6/11/83	NL	
	Switch bit reverse; Add 9.0	7/21/83	NL	

DOC. NO. 4000-500-00

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0.0 SCOPE

This document describes the features, functionality and specification of the SC4000, a controller for QIC II compatible Streaming Tape Drives, for attachment to existing SASI or SCSI based disk storage system.

0.1 REFERENCE DOCUMENTS

QIC II Tape drive product specification
Existing disk controller product specification

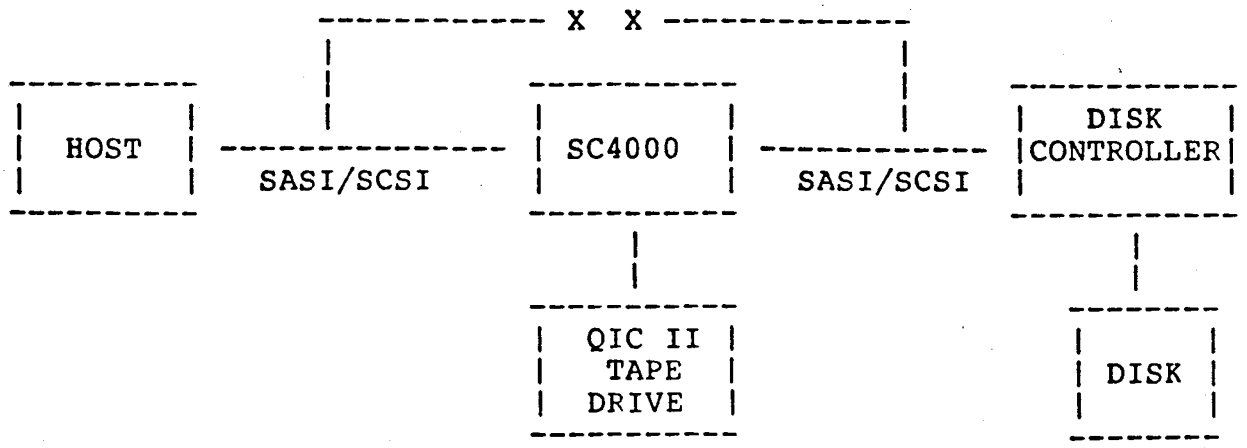
1.0 GENERAL DESCRIPTION

SC4000 allows the user to add an intelligent tape drive to an existing SASI or SCSI based disk storage system. When used in this manner, the SC4000 is installed in between the host adaptor and the disk controller.

Alternatively, the SC4000 may also be used as a standalone tape-only controller on a SASI or SCSI buss.

The SC4000 is connected directly to the host adaptor via a SASI or SCSI interface. All the existing disk controller(s) are connected indirectly to the host adaptor through the SC4000. Thus, the SC4000 has total control over communication between the host adaptor and the the disk storage system.

The SC4000 will screen all commands issued by the host adaptor. It will intercept commands directed to the tape drive, and will pass on all non-tape commands to the disk controller(s). Additionally, it will coordinate disk to tape and tape to disk data transfers all by itself, without involving the host adaptor and the host computer.



The broken path shown might have been the orginal system set up before installing SC4000 and QIC II tape drive.

3.0 CONTROLLER SELECTION MODES (LUN MODE AND ID MODE)

3.1 LUN MODE

For older SASI host adaptors not capable of selecting different Controller IDs, this mode allows the host computer to direct commands to the SC4000 by using an LUN between 4 and 7. To choose this mode of operation, set Key 4 on the Dip Switch to ON. The LUN for SC4000 can be set as follows:

LUN	Key 4	Key 3	Key 2	Key 1
4	ON	ON	OFF	OFF
5	ON	ON	OFF	ON
6	ON	ON	ON	OFF
7	ON	ON	ON	ON

3.2 ID MODE

For host adaptors capable of selecting different Bus Devices (a maximum of 8 under SCSI), this mode allows the host to select the SC4000 controller by asserting the corresponding Data Bus line in the Device Selection Phase. To choose this mode of operation, set Key 4 on the Dip Switch to OFF. The Controller ID for the SC4000 can be set as follows:

Controller ID	Key 4	Key 3	Key 2	Key 1
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON

4.1 COMMAND DESCRIPTOR BLOCK DEFINITION:

Since SC4000 does not intercept commands involved disk operations only, the commands described here are for disk/tape or tape only operations.

The host sends commands to the controller in the form of 6-byte command descriptor blocks (CDB). The first byte of the block is always the command code.

Because of variation of formats in commands, refer to Section 4.2 for each command's CDB format.

Some general comments deserves special mentions here. On power-up and reset, the ONLINE to the tape drive signal is deasserted. On the very first command to the tape drive which should be Request Sense, ONLINE is asserted and remains asserted at all time. The only command that will deassert ONLINE is Rewind, which will also reassert ONLINE at the end of the rewind operation.

Most commands are translated into the corresponding QIC II commands and pass on to the tape drive. Therefore, the tape drive product specification should be consulted for specific details of tape operation; in particular, the meaning of status/sense bytes.

opcode 03 Request sense bytes - This command must be issued immediately after detecting an error. (The host detects error by checking the composite error bit of completion status byte). Note that this command is mandatory on power up for most QIC II tape drives.

CDB

	7	6	5	4	3	2	1	0
byte 0	0	0	0	0	0	0	1	1
1	<	LUN	>	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	1	0	0	0	0
5	0	0	0	0	0	0	0	0

The SC4000 will return a total of 16 bytes.

Bytes 0,1,2,3 = four bytes returned from the disk controller.

Bytes 4,5,6,7,8,9 = six bytes returned from QIC II tape drive.

Bytes 10,11,12 = bytes containing number of blocks been transferred in the last disk operation. Byte 10 is the MSB.
These 3 bytes are generated by SC4000 and will be cleared after the current Request Sense command has been processed.
Also note the blocks reported here could be either 256 or 512 bytes per block.

Bytes 13,14,15 = bytes containing number of blocks been transferred in the last tape operation. Byte 13 is the MSB.
These 3 bytes are gererated by SC4000 and will be cleared after the current Request Sense command has been processed.
The blocks reported here are based on 512 bytes per block.

opcode 08 Read blocks - Reads the specified number of blocks starting from the current tape position.

Because of QIC II tape drive characteristics, Error condition will be set when the last block of data is read from the tape drive. Therefore, the host should expect Error bit set in Completion Status. The host should then issue Request Sense to clear the error condition.

CDB

	7	6	5	4	3	2	1	0
byte 0	0	0	0	0	1	0	0	0
1	< LUN >			0	0	0	0	0
2	MSB number of blocks							
3	number of blocks							
4	LSB number of blocks							
5	0	0	0	0	0	0	0	0

opcode 0A Write blocks - Writes the specified number of blocks starting at the current tape position.

CDB

	7	6	5	4	3	2	1	0
byte 0	0	0	0	0	1	0	1	0
1	<	LUN	>	0	0	0	0	0
2	MSB number of blocks							
3	number of blocks							
4	LSB number of blocks							
5	0	0	0	0	0	0	0	0

opcode 11 Space -- skips over the specified number of blocks or the specified number of file marks, depending on the value of the Code Field: 00 means blocks, and 01 means file marks. The number of blocks or file marks is specified by the Count Field. If a file mark is encountered during a skip block operation, the file mark will not be skipped over; instead, an error condition is reported.

CDB

	7	6	5	4	3	2	1	0
byte 0	0	0	0	1	0	0	0	1
1	< LUN >			0	0	0	< code >	
2	MSB count							
3	count							
4	LSB count							
5	0	0	0	0	0	0	0	0

A special case is when the Code Field is 11 (in binary), which causes the tape to move to the end of data, in preparation for appending to the tape.

Please note that with most QIC II tape drives, in order to allow proper detection of the end of tape data, a cartridge must be erased before the first write operation is made to the tape. Use the erase command for this purpose.

PARAMETER LIST

	7	6	5	4	3	2	1	0
byte 0	function code							
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	< SID >				0	0	< SLUN	>
5	< DID >				0	0	< DLUN	>
6	0	0	0	0	0	0	<1>	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	MSB number of disk sectors							
10	number of disk sectors							
11	LSB number of disk sectors							
12	0	0	0	0	0	0	0	0
13	MSB logical disk address							
14	logical disk address							
15	LSB logical disk address							

The three bytes of Number of Disk Sectors defined in the parameter list are based on the counts on the disk side. Since there are always 512 bytes per block for QIC II, SC4000 will read/write exactly half that number of blocks from/to tape if the disk controller is in the 256 bytes per sector mode. In such case, the Number of Disk Sectors must be even.

5.0 CONNECTOR DEFINITION

5.1 HOST INTERFACE CONNECTION

PIN#	NAME	DRIVEN BY	DESCRIPTION
02	DB0-	HT/CL	Bidirectional data bus 0
04	DB1-	HT/CL	Bidirectional data bus 1
06	DB2-	HT/CL	Bidirectional data bus 2
08	DB3-	HT/CL	Bidirectional data bus 3
10	DB4-	HT/CL	Bidirectional data bus 4
12	DB5-	HT/CL	Bidirectional data bus 5
14	DB6-	HT/CL	Bidirectional data bus 6
16	DB7-	HT/CL	Bidirectional data bus 7
18	PARITY-	HT/CL	Bidirectional parity bit
20	N/A		Not used
22	N/A		Not used
24	N/A		Not used
26	N/A		Not used
28	N/A		Not used
30	N/A		Not used
32	N/A		Not used
34	N/A		Not used
36	BSY-	CL	Busy
38	ACK-	HT	Acknowledge
40	RST-	HT	Reset
42	MSG-	CL	Message
44	SEL-	HT	Select controller
46	C/D-	CL	Command/Data mode select
48	REQ-	CL	Request
50	I/O-	CL	Input/Output mode select

Note: All odd pins are connected to ground.

HT = Host
CL = Controller
- = negative true signals

Signals received at the host side should be terminated with 220 ohms to +5V and 330 ohms to Gnd.

6.0 SPECIFICATIONS

6.1 MECHANICAL SPECIFICATION

Width	5.75 inches / 14.6 cm
Length	8 inches / 20.3 cm

6.2 ELECTRICAL SPECIFICATION

Voltage requirement	+5VDC +/- 5%	
Current requirement	+5VDC @ 2	Amps maximum
	1.6	Amps typical

6.3 ENVIRONMENTAL REQUIREMENTS

	Operating	Storage
Temp. degree F/C	32/0 to 131/55	-40/-10 to 167/75
Relative Humidity @ 40 degrees F	10% to 95%	10% to 95%
Altitude from sea level	0 to 10,000 ft	0 to 15,000 ft

7.1.3 Unidirectional Signals driven by Host

ACK	Acknowledge. This signal is asserted as a handshake response to controller's REQ.
SEL	Select. The host uses this signal to gain controller's attention at the beginning of command processing.
RST	Reset. Asserted-then-deasserted on this bit reinitializes the controller. Minimum requirement of Reset pulse (duration of this assertion) is 20 microseconds.

7.2 Operational Description

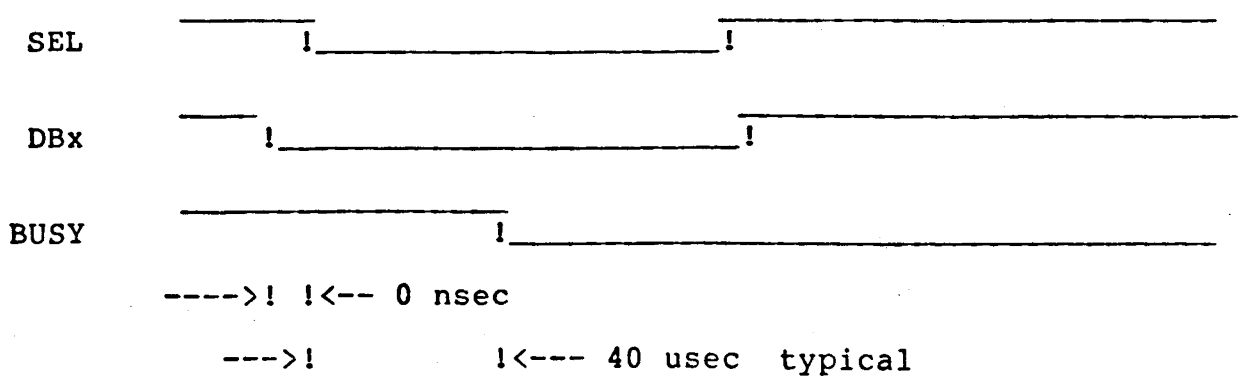
The following outlines the sequence of steps to issue a command to the controller:

1) Host polls on BUSY signal until deasserted to show the controller is ready to accept command.

2) Host asserts SEL and DBx (controller address bit) to gain the controller's attention and waits for the BUSY asserted by the controller indicating it has recognized the selection.

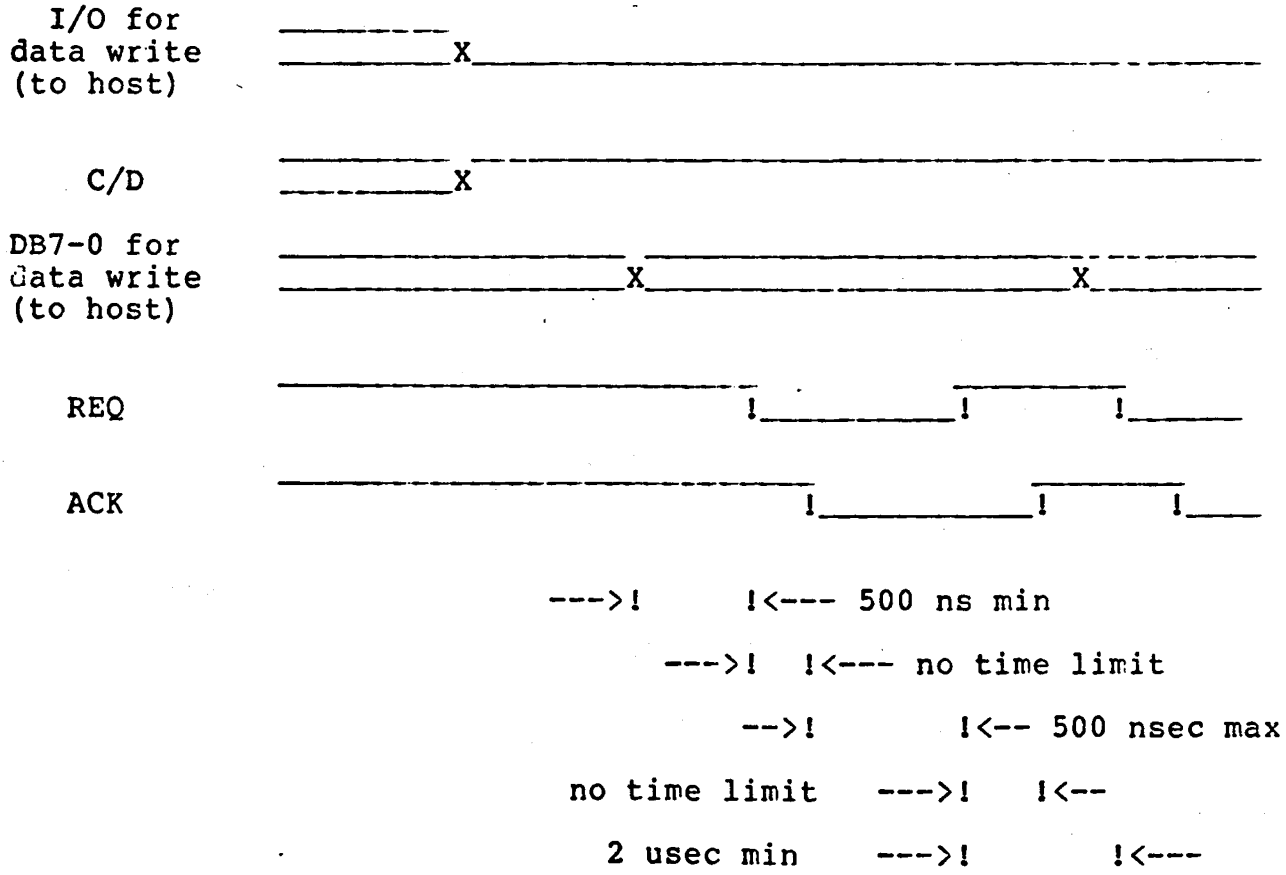
3) Host deasserts SEL and DBx. The controller from now has the control of the bus and is ready to accept Command from the host.

SELECTION TIMING ILLUSTRATION



5) For commands involving Data transfer, the controller deasserts C/D to indicate data mode transfer on the bus. I/O is to asserted for READ command and deasserted for WRITE command. REQ/ACK form the same handshake as in command transfer case.

WRITE DATA TRANSFER TIMING ILLUSTRATION
(from controller to host)



6) Upon completion of any command, the controller puts a completion status byte on the data bus, with C/D and I/O asserted. REQ/ACK handshake is used to transfer this completion status byte to the host.

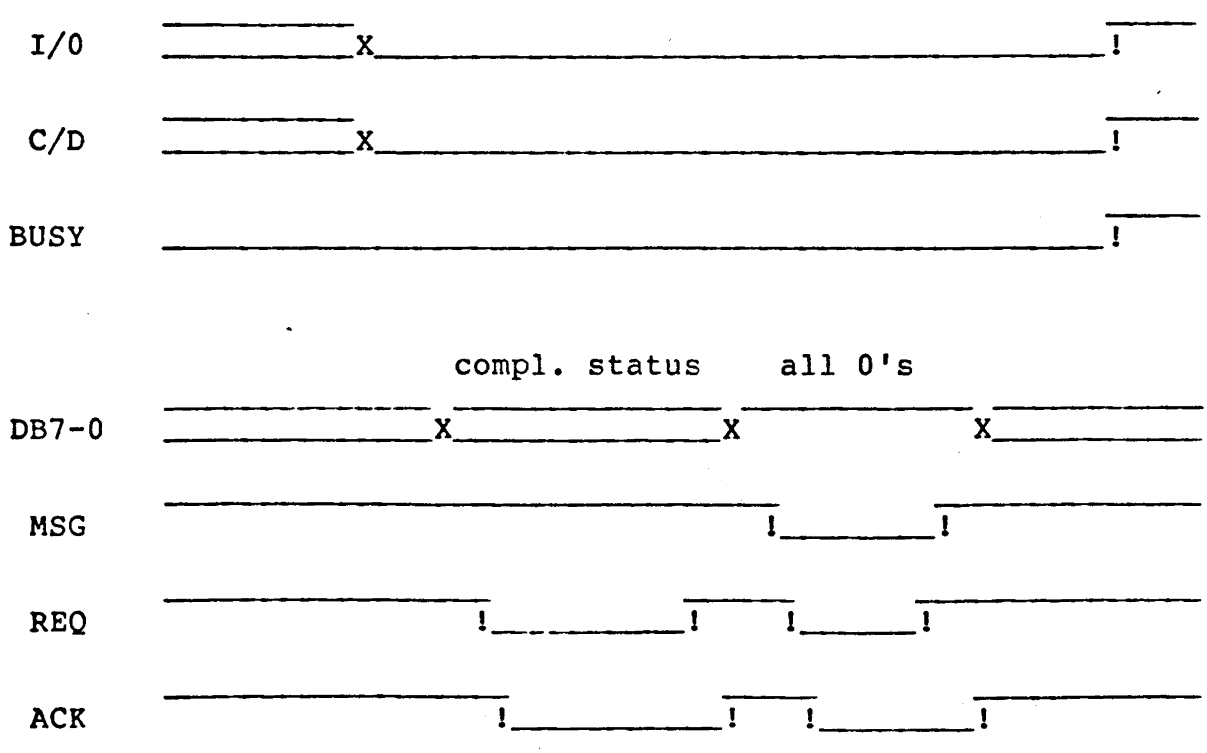
Completion status byte definition

7	6	5	4	3	2	1	0
0	0	0	<	SPARE	>	*	0

* = composite error bit

7) Then the controller places all zero's on the data bus with MSG asserted. The same REQ/ACK handshake to transfer this Message byte to the host.
Such message byte returned by the controller can be used to generate an interrupt to system to signify the completion of the command.

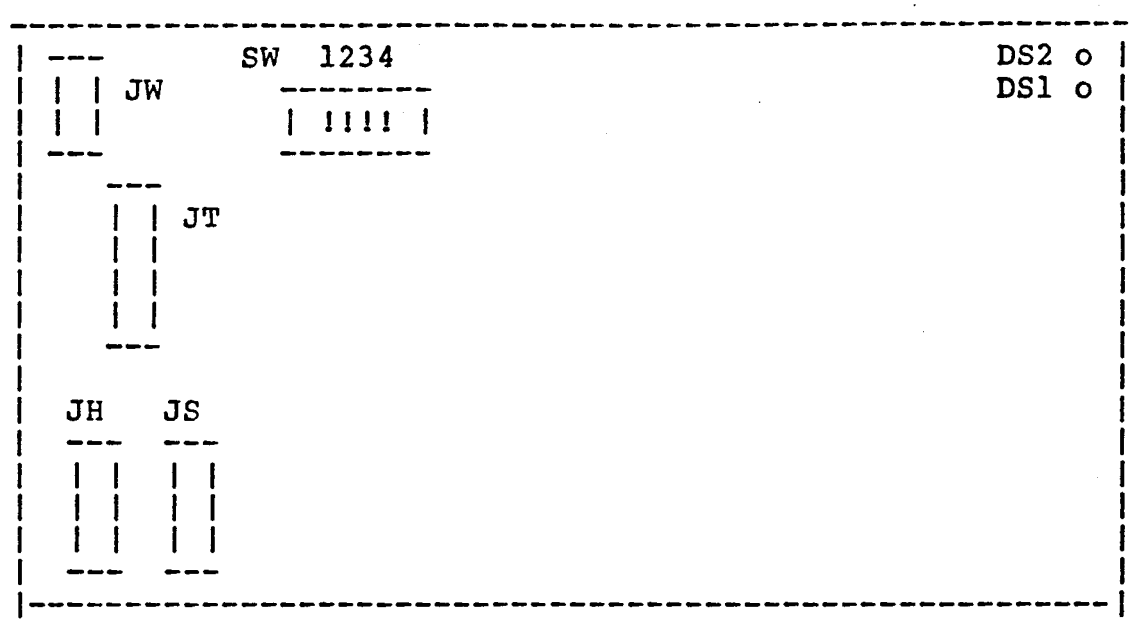
COMPLETION STATUS AND MESSAGE BYTES TRANSFER TIMING ILLUSTRATION



timing requirements are same as I/O data write case above

8.0 USER GUIDE FOR HARDWARE SETUP

8.1 SC4000 board layout



JW	4 pin power connector to power cable where pin 1 is not connected pins 2,3 are grounded pin 4 connected to +5V
JT	50 pin 0.10" spacing connector to QIC II drive
JS	50 pin 0.10" spacing connector to DK controller
JH	50 pin 0.10" spacing connector to Host cable
DS1	ON to indicate there is an error condition detected either by SC4000 or QIC II drive.
DS2	ON to indicate SC4000 is busy in processing a command.

9.0 ON-BOARD MICRODIAGNOSTICS

The SC4000 is equipped with on-board microdiagnostics to diagnose and isolate hardware faults on the board.

9.1 Modes of test operation determined at power up

Modes	Keys 4	3	2	1
Individual Test	ON	OFF	OFF	OFF
Continuous Go/No Go Test	ON	OFF	OFF	ON

The DIP-switch must be set as indicated before powering on or resetting the controller. Reset can be accomplished by momentarily shorting pins 10 and 11 of U1E (I8284A).

These test operations can be run in stand-alone (no interface cables connected) or under system configuration (with all interface cables connected).

9.1.1 Individual Tests

After power up, keys 3,2,1 carry the binary value of the test number.

	Keys 3	2	1
Test 0 - RAM check	OFF	OFF	OFF
Test 1 - SASI data path check	OFF	OFF	ON
Test 2 - TAPE data path check	OFF	ON	OFF
Test 3 - DMA chip memory to memory check	OFF	ON	ON
Test 4 - LED's check	ON	X	X

Without selection, a built-in PROM checksum test is run before going into any of these 5 tests.

Key4 in OFF position starts the test and ON position stops the test.

Note that LED2 will blink each time the test is repeated. This will happen as long as no failure occurs. If the test fails, LED1 will light, and the failing operation will be continuously repeated so that it can be probed by a scope. The controller must be reset to get out of this endless loop.

(See 9.2 for detailed explanation of each individual test.)

d) TAPE data path test - A data pattern is written to the data buffering registers (U9A and U10A) and then checked by reading it back. A different pattern is used each time the LED2 is blinked, but because the operation lasts no more than a millisecond, the blinking will not be discernable.

e) DMA chip memory to memory test - The same kind data pattern for the RAM test is used here. After the pattern is written, data in the entire memory region is shifted down one location towards location 0 using the memory to memory transfer operation of the DMA chip. Contents of location 1 is moved to location 0, location 2 to location 1, and so on. After the transfer is completed, the relocated data is checked for transfer error. Again, as in the RAM test, a different pattern is used with each blink of LED2.