United States Patent [19]

Anderson

[11] **Patent Number: 4,507,592**

[45] **Date of Patent: Mar. 26, 1985**

[54] **MICROPROCESSOR CONTROLLED TAPE CAPSTAN**

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[21] Appl. No.: **601,809**

[22] Filed: **Apr. 19, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 459,720, Jan. 21, 1983, abandoned, which is a continuation of Ser. No. 321,070, Nov. 13, 1981, abandoned.

[51] **Int. Cl.**[3] **H02P 1/22**

[52] **U.S. Cl.** **318/268**; 318/270; 318/618

[58] **Field of Search** 318/3, 6, 7, 398, 369, 318/270, 271, 463, 464, 618, 268; 364/550, 570, 579; 360/73, 74.1; 242/46

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,706,020	12/1972	Klang	318/270
3,836,833	9/1974	Harris et al.	318/270
3,904,943	9/1975	Klang	318/395
3,969,663	7/1976	Arthur et al.	318/561
4,302,785	11/1981	Mussatt	360/72.1
4,321,517	3/1982	Touchton et al.	318/618

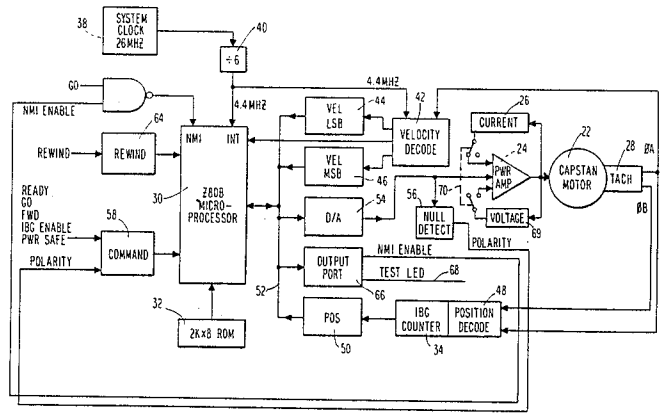
Primary Examiner—Ulysses Weldon

Attorney, Agent, or Firm—Woodcock, Washburn, Kurtz, Mackiewicz & Norris

[57] **ABSTRACT**

An improved magnetic tape drive having high performance specifications is achieved by microprocessor control of the capstan motion. Possible velocity profiles are stored in read-only memory and are selected on the basis of new input commands and last previous actions taken, whereby excitation of mechanical resonance inherent in the system is avoided.

8 Claims, 8 Drawing Figures



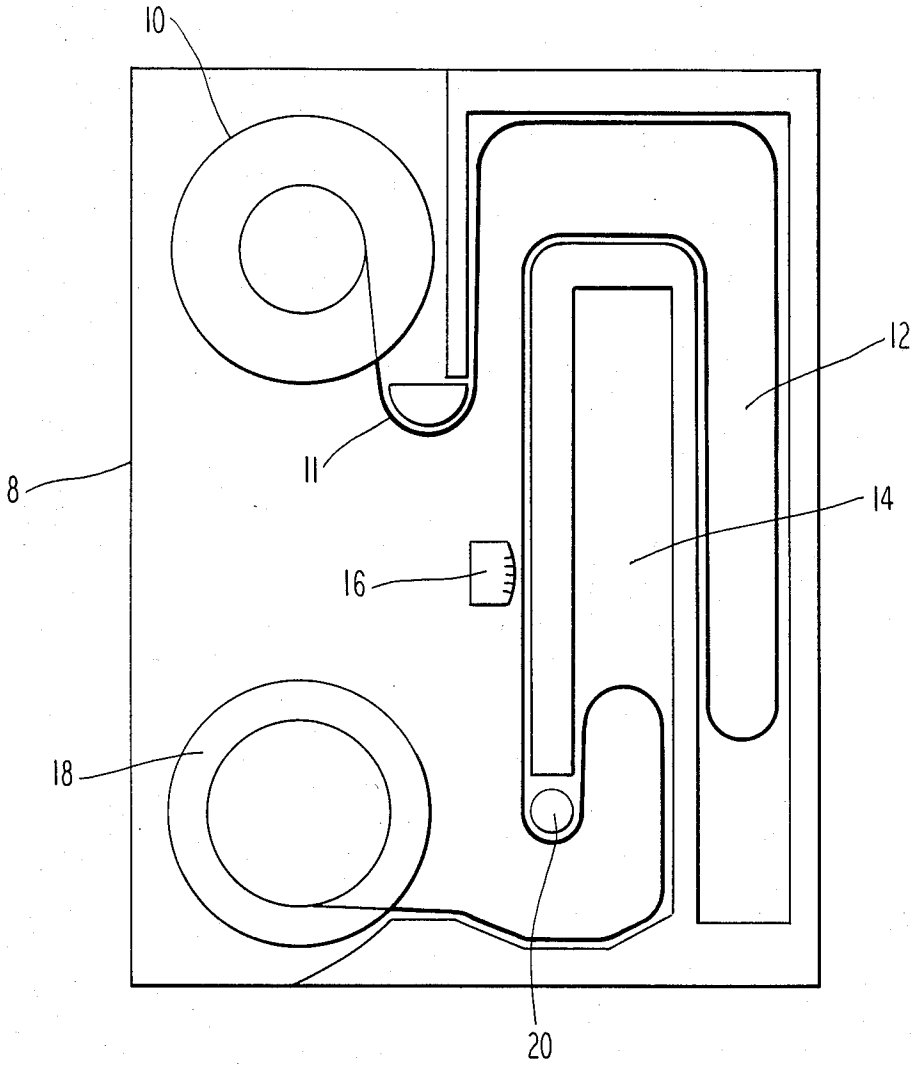
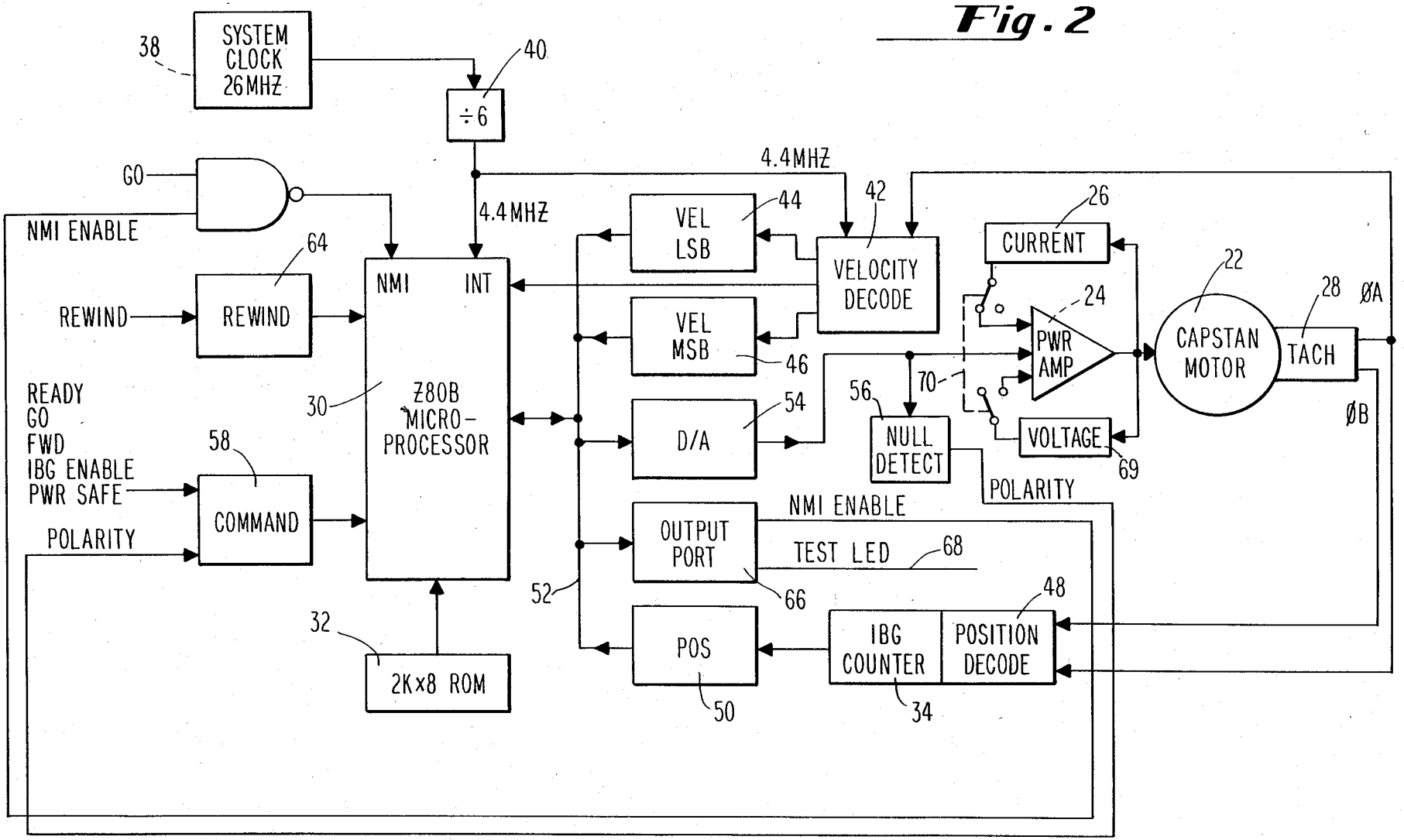


Fig. 1

Fig. 2


38
SYSTEM CLOCK 26MHZ
40
÷6
4.4MHZ
4.4MHZ
GO
NMI ENABLE
64
REWIND
REWIND
NMI
INT
30
Z80B MICRO-PROCESSOR
READY
GO
FWD
IBG ENABLE
PWR SAFE
58
COMMAND
POLARITY
32
2K×8 ROM
VEL LSB
44
VEL MSB
46
D/A
54
OUTPUT PORT
52
66
POS
50
42
VELOCITY DECODE
26
CURRENT
24
PWR AMP
22
CAPSTAN MOTOR
28
TACH
ØA
ØB
56
NULL DETECT
70
VOLTAGE
69
POLARITY
NMI ENABLE
TEST LED
68
48
IBG COUNTER
POSITION DECODE
34

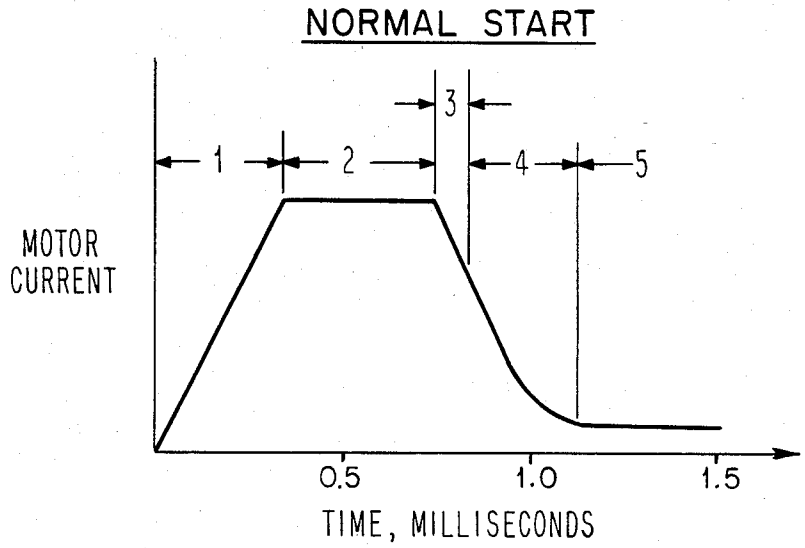

NORMAL START
1
2
3
4
5
MOTOR CURRENT
0.5
1.0
1.5
TIME, MILLISECONDS

Fig. 3

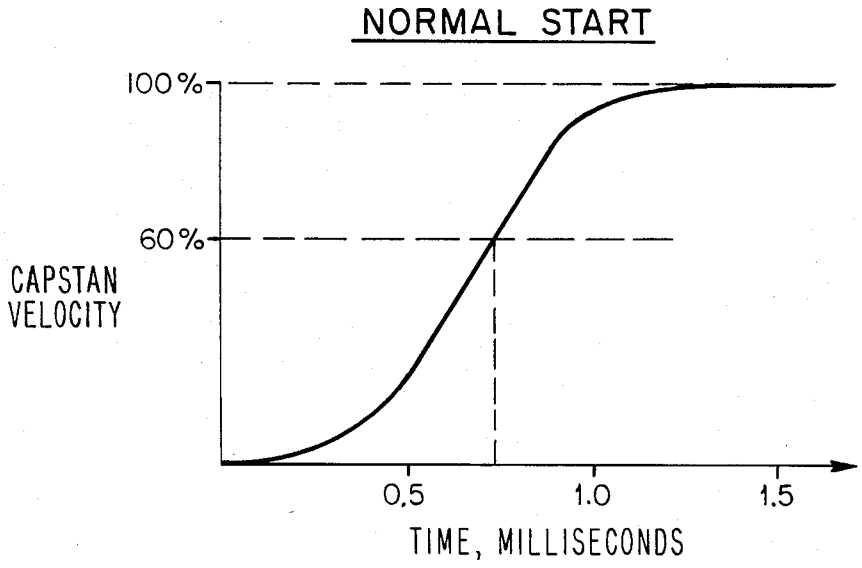

NORMAL START
100%
60%
CAPSTAN VELOCITY
0.5
1.0
1.5
TIME, MILLISECONDS

Fig. 4

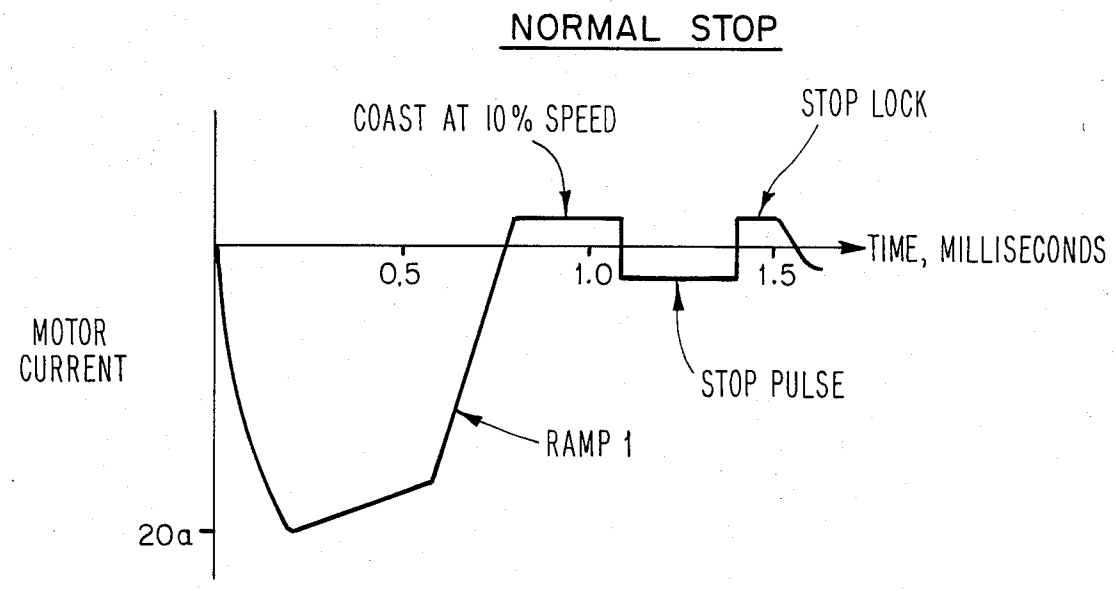

NORMAL STOP
COAST AT 10% SPEED
STOP LOCK
TIME, MILLISECONDS
0.5
1.0
1.5
MOTOR CURRENT
STOP PULSE
RAMP 1
20a

Fig. 5

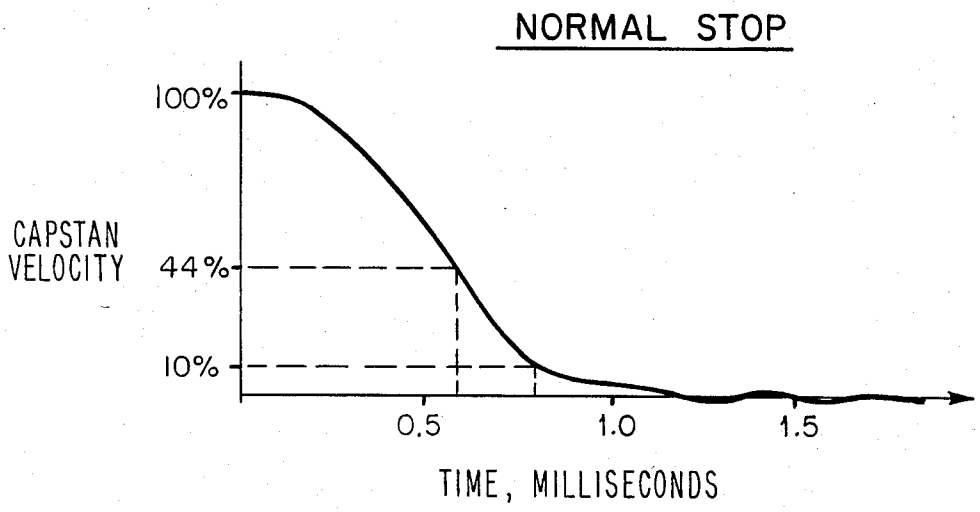

NORMAL STOP
100%
CAPSTAN VELOCITY
44%
10%
0.5
1.0
1.5
TIME, MILLISECONDS

Fig. 6

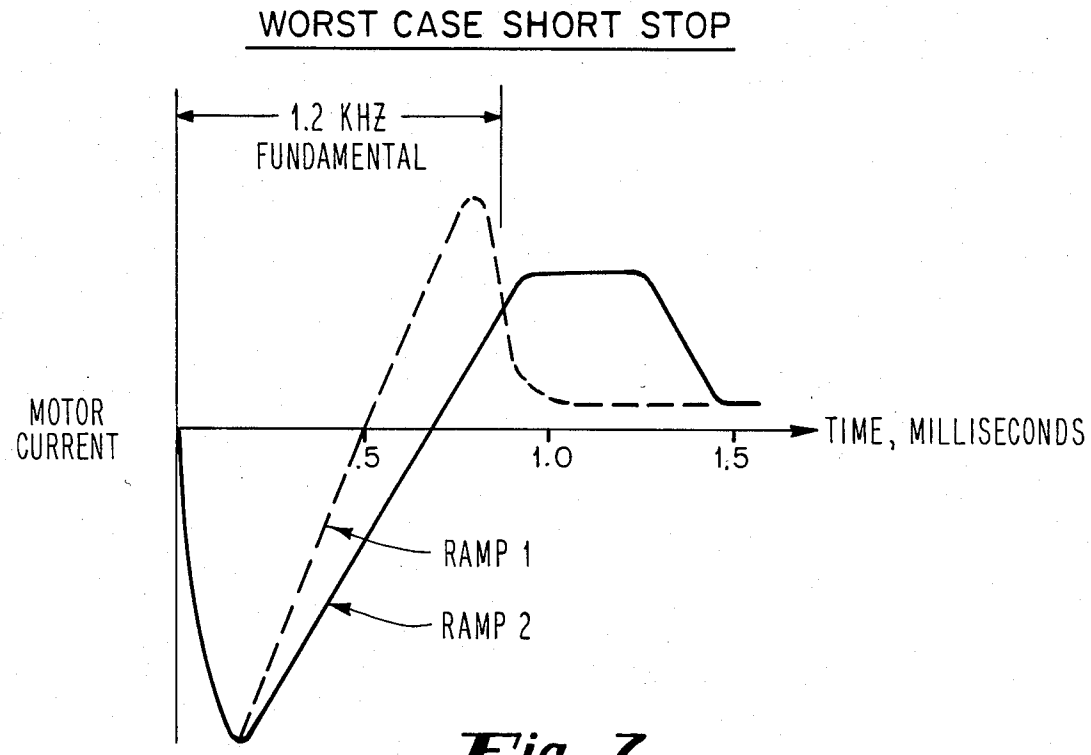

WORST CASE SHORT STOP
1.2 KHZ
FUNDAMENTAL
MOTOR
CURRENT
.5
1.0
1.5
TIME, MILLISECONDS
RAMP 1
RAMP 2

Fig. 7

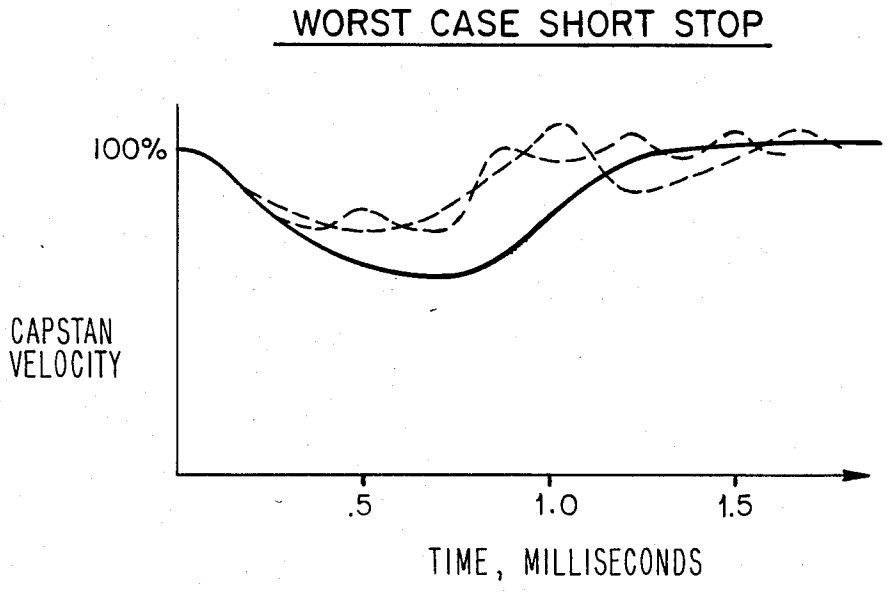

WORST CASE SHORT STOP
100%
CAPSTAN
VELOCITY
.5
1.0
1.5
TIME, MILLISECONDS

Fig. 8

MICROPROCESSOR CONTROLLED TAPE CAPSTAN

This is a continuation, of application Ser. No. 459,720, filed Jan. 21, 1983, now abandoned, which is a continuation of application Ser. No. 321,070, filed Nov. 13, 1981 now abandoned.

FIELD OF THE INVENTION

This invention relates to control of the capstan used to drive magnetic tape for the storage of data. More particularly, the invention relates to improved methods of control of the rotational motion of such capstans, whereby high rates of acceleration to a target tape speed can be achieved without excitation of torsional vibration.

BACKGROUND OF THE INVENTION

The American National Standards Institute (ANSI) has defined certain standards for the performance of magnetic data storage tape drive apparatus. In particular, data to be recorded according to ANSI standards is recorded in blocks separated from one another by no less than 0.280 inches. This interblock gap is therefore that space in which a tape drive starting in the interblock gap must accelerate to its full design speed. Various tape velocities are standard, including up to 200 inches per second (ips). The goal of providing a tape drive which can accelerate to 125 ips within the 0.075 inch start distance (which is an acceleration of some 500 times the acceleration of gravity or 500 g's) is a requirement of a commercial tape drive.

The art has traditionally separated the mass of the tape carried on supply and take up reels from that portion of the tape in the vicinity of the read/write head (which is that portion of the tape which in fact must be accelerated to satisfy the requirements mentioned above) by decoupling that portion from the bulk of the tape, using vacuum columns in which loops of tape are carried. In this way, only the relatively small portion of the total tape in the vicinity of the head need be accelerated at very high rates, whereas the bulk of the tape carried on the reels can be accelerated relatively slowly. However, high acceleration of the portion of the tape in the vicinity of the heads is a significant engineering problem. To this end a vacuum capstan is typically used. Such a capstan is a hollow, cylindrical wheel having many holes in its periphery in contact with the tape. A vacuum is applied to the center of the hollow capstan so as to suck the tape into firm, non-sliding contact with the capstan. The capstan is made very light and of low inertia, so that it can be very quickly accelerated to speed, whereby the tape in contact with the capstan quickly reaches the design speed of the tape drive. See, for example, U.S. Pat. No. 4,065,044 to Painter et al for an example of such capstans.

The control of the acceleration of a capstan, even a relatively lightweight, low inertia one such as that disclosed in the Painter et al patent, remains a difficult problem. To this extent, numerous motion control schemes have been devised. According to the present invention, a microprocessor is used to continuously sample the actual speed of the tape drive and accelerate, decelerate or hold it at a steady angular velocity, as indicated by comparison of the actual velocity signal with a velocity command signal. The use of the microprocessor allows considerable versatility of the system

to adapt to conditions encountered and allows long-term stability without regard to variations in, e.g., component tolerance and the like.

OBJECTS OF THE INVENTION

It is therefore an object of the invention to provide an improved drive for a magnetic tape system.

A further object of the invention is to provide a magnetic tape drive system in which a microprocessor controls the motion of a vacuum capstan used to move that portion of the tape juxtaposed to the head at any given time.

Still a further object of the invention is to achieve extremely high rates of acceleration of a tape to a steady, carefully controlled running speed without undue fluctuations in tape speed due to mechanical resonances in the device or to "hunting" of an analog servo loop.

SUMMARY OF THE INVENTION

The above needs of the art and objects of the invention are satisfied by the present invention in which a microprocessor utilizing look up tables for velocity profiles is used to control the motion of the tape capstan. The microprocessor examines each incoming command to determine whether it is likely to excite a vibration and, if so, modifies the capstan control so as to avoid the vibration.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood if reference is made to the accompanying drawings, in which:

FIG. 1 shows an schematic elevation view of the face plate of a tape drive using the capstan control system of the invention;

FIG. 2 shows a schematic diagram of the layout of the capstan control system;

FIG. 3 shows a graph of motor current versus time in a normal start operation;

FIG. 4 shows velocity versus time for the start operation;

FIG. 5 shows current versus time for a normal stop operation;

FIG. 6 shows velocity versus time for a normal stop operation;

FIG. 7 shows the motor current versus time for two possible courses of action taken in a worst case short stop situation; and

FIG. 8 shows velocity versus time for the several possibilities of the worst case short stop operation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As discussed above, the invention relates to control of the vacuum capstan used in a magnetic tape drive, in particular one for storage of data. Copending application Ser. No. 123,729, filed Feb. 22, 1980, in the name of Epina et al incorporated herein by reference shows a tape drive in detail in which the capstan and control circuitry of the invention has application. In particular, that copending application describes a tape drive which is capable of achieving 200 ips performance while remaining within the ANSI standards with respect to interblock gap as described above. The invention of that application involves the particular tape path along which the magnetic tape passes between the take-up and supply reels. The present invention relates to the capstan which is used to accelerate the tape up to speed

upon, for example, a host computer command, and is accordingly not limited to the particular tape path shown in the copending application referred to above, but instead has applicability to many other forms of tape transport systems.

FIG. 1 shows a schematic layout of a tape drive. For example, a vertically extending face plate 8 carries a supply reel 10 from which tape 11 is supplied. The tape passes through a first vacuum column 12, past a read/write head 16, into and out of a second vacuum column 14, and is taken up upon the tape-up reel 18. The tape 11 is passed through the vacuum columns 12 and 14 so that the mass of tape carried on the reels 10 and 18 is decoupled from that in the vicinity of the read/write head 16. Thus, when it is desired that a stopped tape be accelerated to its design speed or stopped from that design speed, a capstan 20 can accelerate the relatively small portion of the tape 11 juxtaposed to the read/write head 16 while the columns allow this part of the total mass of tape to move at a different rate than that carried on the reels 10 and 18. When the reels come up to speed, the loops of tape within the vacuum columns 12 and 14 regain their original sizes, these having varied during the start operation, as is well understood in the art.

As noted, the present invention relates to microprocessor control of the motor driving the capstan. A schematic overview of the system used is shown in FIG. 2. The capstan motor 22, which drives the capstan 20 (FIG. 1) operates under the control of a power amplifier 24 which has both current 26 and voltage 69 feedback. Mounted on the motor shaft is a tachometer 28 providing two phase output signals ϕA and ϕB. The tachometer 28 is a 1000 line two-phase incremental encoder whose full period is 45.2 microseconds at running speed. It is these output signals which provide the computational workload for the system, which is based on a microprocessor 30 supplied with its operating program, and certain look-up tables discussed in detail below, by a 2K by 8-byte ROM 32. As noted, at 125 ips the tachometer period is 45.2 microseconds. To get $\frac{1}{2}$% period measurement resolution requires a count rate of 4.4 mHz. This is supplied by a system clock 38 operating at 26 mHz, the output of which is divided by 6 in a divide-by-6 network 40, the output of which is supplied to a transistor-transistor-logic (TTL) counter 42, operating as a velocity decoder. The output of the decoder 42 is stored in registers 44 and 46 which feed the microprocessor bus, thus providing a signal of the instantaneous velocity once every tach period.

Direction detection and position counting are also implemented in logic outboard of the processor in order to minimize computation delay. FIG. 2 shows the two phase outputs of the tachometer 28, ϕA and ϕB, being supplied to a position decode network 48 which feeds an interblock counter 34 so as to keep an accurate register of the position of the tape in a non-running situation. The position output is supplied to the microprocessor via a position register 50, connected to the microprocessor bus 52. The output of the microprocessor 30 is supplied to a digital-to-analog (D/A) converter 54, supplying the analog signal which controls the power amplifier 24 which drives the capstan motor 22. The output of the D/A converter 54 is also supplied to a null detect network which supplies a D/A zero-adjust signal, including a polarity signal supplied to a command register 58, in which are also stored operator or host initiated commands supplied to the microprocessor 30.

Thus, the microprocessor 30 is provided with digital velocity and position signals so that it requires very few program steps to determine the next current command to be supplied to the D/A converter 54 and thence to the power amp 24 to control the further motions of the motor 22. In a preferred embodiment, a Zilog Z80B microprocessor was chosen because it has enough speed to complete the required program steps safely within less than 1 tachometer period. Its internal registers are sufficient to implement the design without use of external RAM which satisfies the goal of the invention of simplicity. A single 2K by 8-byte ROM 32 is used to store both the program instructions and certain look-up tables discussed in detail below. The rewind command is supplied to the Z80B through a rewind command register 64. Also supplied as an output of the Z80B is a "NMI enable" signal, which is stored in an output port register 66 and gates the NMI input of the Z80B. It is combined with the GO signal in an inverted-output AND gate to generate the NMI input. A test LED appearing on the card is lit as indicated at 68 as an aid in diagnostics.

As discussed above, the capstan control arrangement of the invention was originally designed to be incorporated within the pre-existing drive which is the subject matter of copending application Ser. No. 123,729, filed Feb. 22, 1980. That particular drive, as do all drives, has certain mechanical components and tape path geometries which have resonant frequencies which can be excited by motor current profiles and program commands executed at the appropriate frequencies. For example, the motor used to drive the capstan has a torsional resonance at 4500 Hz, the vacuum columns have resonant frequencies of 35 and 55 Hz, and the tape stretched between the capstan and vacuum column has a resonance frequency between 1.2 and 1.6 KHz. Clearly it is desirable to control the capstan motor in such a way that all these resonances and the attendant physical instabilities are eliminated. Careful control by the microprocessor of the capstan motor, as will be discussed in detail below, allows all these resonances to be avoided, and smooth operation achieved. Similarly, the other objects of the invention, achieving 1 millisecond starts, that is, within the 0.075 inch start distance and settling within ANSI standards for velocity within about 1.2 milliseconds, are achieved with this design. Microprocessor use also permits better velocity control and simpler design, yielding a lower chip count and reduced hardware costs.

FIGS. 3 through 8 show current and velocity profiles for several of the more usual operations undergone by the system according to the invention. FIGS. 3 and 4 show current and velocity profiles, respectively, for a normal start; FIGS. 5 and 6 show current and velocity profiles for a normal stop; and FIGS. 7 and 8 current velocity profiles, respectively, for the worst case short stop situation in which the 1.2 KHz resonance mentioned above can be encountered if the appropriate steps are not taken.

FIG. 3 shows motor current during a conventional start operation from zero velocity and FIG. 4 shows the accompanying velocity profile. The current supplied is, as noted, divided into five phases. During phase 1, current is increased at a constant rate to a limit which is maintained during phase 2. The programmed current build up in phase 1 reduces the excitation of the motor's torsional resonance at 4500 Hz. Transition from phase 2 to phase 3, in which reduction of current begins, occurs

at approximately 60% of full speed. However, capstan speed is changing too fast, approximately a 15% change occurring per tach period, to accurately determine when 60% of full speed occurs. The solution chosen was to watch the tach period during phase **2** and, knowing that acceleration is proportional to current, compute the time remains until 60% of full speed is reached. When that time is reached, the timed ramp-down of phase **3** is initiated without having to wait for another whole tach period to be consumed. In a preferred embodiment, the computation of time remaining is actually done by table look-up. In phase **4**, the velocity is high enough to use simple proportional control with current proportional to velocity error. That is to say, full design velocity would be compared with that in the two actual velocity registers **44** and **46**. In this operation, the use of the microprocessor **30** provides another important advantage. Speed in this phase is still changing by as much as 10% per tach period making measured speed lag actual speed at sampling times. This effect is eliminated by using another look up table stored in ROM **32** to contain the current values modified by the known sampling lag.

Integral action is added to proportional action during phase **5** when the capstan is at nearly full speed. Two integrators are used, both implemented by registers within the processor **30**. The first integrator starts with zero initial condition at the beginning of phase **5** and responds fast enough to correct for the varying tape tension load imposed by the two vacuum columns **12** and **14** (in FIG. **1**) whose resonant frequencies are 35 to 55 Hz. Whenever the "GO" command to the tape drive is dropped and the motor stops, the contents of the first integrator register are used to increment the second by a fixed amount. The second integrator has a slower response time than the first, but is not reset when "GO" is dropped. It is, therefore, capable of compensating for variations in drag, torque constant and analog circuit offsets. The switching and memory capabilities of the microprocessor **30** thus make the advantages of error integration possible, without the usual overshoot problems that one would expect with an analog integrator.

It will be observed by those skilled in the art that there is a relatively smooth transition between phases **4** and **5**. This is done in order to eliminate the errors caused by shaft wind up between the motor and the tachometer disk as suggested in the prior art, for example, see U.S. Pat. No. 3,904,943 to Klang.

FIGS. **5** and **6** show, respectively, motor current and velocity versus time for a normal stop operation. When the "GO" command to the drive drops, the microprocessor initiates the "STOP" routine. The power amplifier which is in the current mode for the "START" and "RUN" operations is switched **70** to voltage mode **69** for "STOP". As will be observed, the motor stop current is increased to approximately 20 amps in the case of a particular motor chosen, which draws a like figure, typically 24 amps at 30 volts for a one millisecond start operation as described above. The current is gradually decreased during the "STOP" operation in the area marked Ramp **1**, in a preferred embodiment beginning when the motor velocity is expected to have dropped to 44% of full speed. The higher initial current is used to insure that position overshoot is avoided. This wave shape minimizes shaft windup towards the end of a "STOP" operation when another "GO" command may occur. This situation will be discussed below in connection with FIGS. **7** and **8**. "Ramp **1**" is continued until the motor has slowed to approximately 10% of full speed, as shown. This speed is maintained by a small positive current until the desired stop position, in the preferred embodiment 0.075 inches, is approached. At this point a stop pulse reduces the speed of the capstan to nearly zero. Thereafter, the "STOP LOCK" phase is entered. It will be appreciated that the two-phase tachometer described above measures position error with a resolution of 0.0014 inches. Use of the "STOP LOCK" algorithm resulting in the "STOP LOCK" current shape shown in FIG. **5** avoids the need for lead lag compensation as practiced by the prior art, by applying motor current correction for only a short pulse followed by dynamic braking until the next tach transition is sensed.

As was discussed above, the low rate of change of current in START is very effective in avoiding excitation of the 4.5 KHz torsional resonance of the motor/capstan combination. In the particular tape drive design shown in the copending application referred to and incorporated by reference above, another broader, less peaked resonance exists between 1.2 and 1.6 KHz, attributable to the stretch between capstan and vacuum column. This resonance can be excited, for example, if the "GO" signal is dropped for approximately 200 microseconds, causing "STOP" to begin, and "GO" is then reapplied. Without detection of and compensation for this sequence, the capstan control will respond with the usual Ramp **1** current increase upon "STOP", and will continue it into the positive current region as shown in the dashed line of FIG. **7**. Since the resultant current profile required to return to full speed has a shape which has almost all its energy at 1.2 KHz, resonance would occur. However, up to 300 microseconds into the stop routine, the motor speed is still above 50% and can be recovered to 100% within the alloted time while using a slower rate of change of current and a reduced start current limit (for example, 14 amps instead of 24) resulting in the shape shown as Ramp **2**. Accordingly, the microprocessor is programmed to detect the possibility of excitation of this resonance, and applies Ramp **2** when it does so.

FIG. **8** shows velocity as a function of time for the several possibilities shown. The solid line indicates the current profile which is followed when it is detected by the microprocessor that the possibility of excitation of the 1.2 KHz resonance exists and Ramp **2** is used instead. The several dotted lines are possible velocity profiles which can occur if Ramp **2** is not followed that is, if Ramp **1** is used. Those skilled in the art will recognize the problems inherent in the velocity fluctuations shown.

In the case when "GO" comes back up after 300 microseconds into the "STOP" operation and before Ramp **1** is completed, the speed has been reduced so that Ramp **2** can no longer be used. The microprocessor therefore simply delays responding to such commands until Ramp **1** has reached the near zero current value. This avoids putting too much energy into the system near the resonant frequency and makes up for any theoretical increase in access time by reducing settling time, i.e., the time required for the tape velocity to settle within the ANSI standards.

It will be appreciated that there has been described a microprocessor system which allows extremely low access times, that is, very fast start or stop operations, while simultaneously meeting ANSI velocity standards. Torsional vibrations are substantially reduced by adap-

tively adjusting the motor current profile to avoid possible resonances, while use of the look-up tables in ROM to determine the particular current profile to be used at any given time allows versatility in the tape drive of the invention. In particular, it can easily be converted from 125 to 75 or 50 ips. The control circuitry is substantially simplified over that which had previously been used; further reductions would be made possible by large-scale integration. Use of the microprocessor also allows several automatic calibration routines and diagnostic aides, e.g. the test LED indication, and the automatic nulling of the D/A converter, to be built in to the extent that no manual adjustments are required in the commercial embodiment of the capstan servo control system of the invention.

Attached hereto is a document marked appendix A entitled, "Capstan Digital Servo System". This document will be recognized by those skilled in the art as a complete microcode version of the control programming of the capstan servo control of the invention. Those skilled in the art provided with this document and the above disclosure, including the control system schematic diagram of FIG. 2 would have no difficulty in implementing the invention.

It will be appreciated that there are additional modifications and improvements which can be made to the invention without departing from its essential spirit and scope which should therefore not be limited by the above disclosure, but only by the following claims.

```
LINE  ADDR  B1 B2 B3 B4      CAP125          12-JUN-81          Version A02          PAGE    1

                    TITLE    'CAP125          12-JUN-81          Version A02
                    LIST X,A
```

STC-153

APPENDIX A

```
                    ************************************************************
                    * ********************************************************** *
                    * *                                                        * *
                    * *            CAPSTAN DIGITAL SERVOSYSTEM                 * *
                    * *                                                        * *
                    * *                                                        * *
                    * *                                                        * *
                    * *                                                        * *
                    * *                  SPEED:  125 IPS                       * *
                    * *                                                        * *
                    * *                                                        * *
                    * ********************************************************** *
                    ************************************************************
                    *
                    ************
                    *
                    *                 *   *   U P D A T E S   *   *
                    ************
                    * 15-Jun          ..increase backward starting current at GOINT6
                    * A02             ..test HP bit for stopping current
                    *
                    ************
                    * 25-Feb          ..adjusted stop current's (because of bastard JP in 1950
                    * A00             ..double sample of position in STOPLOCK
                    *                 ..integrator's reset in servo
                    *                 ..installed STOPLCK routine from CAP75 PROGRAM
                    ************
                    * 13-JAN-81       ..repaired EXX's in stoplock
                    *   3.9
                    ************
                    *  5-JAN-81       changed most JP's to JR to claim more room
                    *   3.8           removed HIGAIN code in stoplock
                    *                 re-arranged IDLE and NULLSET
                    *                 corrected VELOCITY x-fer to sequencer
                    ************
                    *
0000
0000
0000
                    *     GO          START CAPSTAN MOTION  (NMI INTERRUPT)
                    *                 1)  START ROUTINES; NORMAL OR SHORT GO-DOWN
                    *                 2)  RAMP CURRENT TO 20 AMP IN 200 USEC; HOLD TO 65 IPS
                    *                 3)  RAMP DOWN TO 13 AMPS AND SWITCH TO LOOK-UP TABLES
                    *                 4)  RUN ROUTINE USES INTEGRATOR TO MAINTAIN VELOCITY
```

9 10

65 60

```
53                      *           5)  MOTOR UPDATES ARE SYNCHRONOUS WITH TACH LINES
54                      ;
55                      ;
56                      *   STOP    STOP MOTION AND MAINTAIN STOP LOCK POSITION
57                      *           1)  VELOCITY PROGRAMMED DECELERATION TO 12 IPS
58                      *           2)  RUN AT 12 IPS TO IBG COUNT 125
59                      *           3)  STOP PULSE TO DECELERATE TO ZERO VELOCITY
60                      *           4)  ENTER STOP LOCK ROUTINE -- MAINTAIN IBG COUNT 125
61                      ;
62                      ;
63                      *   READY   ENABLES STOP LOCK
64                      ;
65                      ;
66                      *   REWIND  HIGH SPEED REVERSE MOTION
67                      *           1)  ADD REWIND REGISTER TO VELOCITY TARGET
68                      *           2)  IF REWIND REGISTER IS ZERO THEN MAINTAIN -125 IPS
69                      *           3)  VELOCITY INTERRUPT IS NOT USED
70                      ;
71                      ;
72                      *  D/A OUTPUT  NULL = 94 --- MAXIMUM CURRENT = +85/-85 = +8.3V/-8.3V
73                      ;
74                      *  HP CARD     USE CURRENT FEEDBACK FOR RUN AND VOLTAGE FEEDBACK FOR STO
75                      ;
76                      ************************************************************
77                      ************************************************************
78                      *                                                          *
79                      *                    INPUT/OUTPUT MAP                      *
80                      *                                                          *
81                      ************************************************************
82                      ************************************************************
83                      ;
84                      ;  I/O IS MEMORY MAPPED (NOTE: 1000H AND 9008H ARE EQUIVALENT ADDRESSES)
85                      ;  THERE IS NO RAM MEMORY -- SUBROUTINES ARE ILLEGAL
86                      ;  PROGRAM MEMORY IS 0 TO 0FFF
87                      ;  ADDRESS BIT 12 HIGH:  I/O ENABLED; ROM DISABLED
88                      ;  ADDRESS BITS 11 AND 12 HIGH:  I/O AND ROM DISABLED
89                      *------------------------------------------------------------*
90                      *
91                      *         Relative port addressing within memory-map
92                      *
93  0000                POSTN:    EQU   0
94  0001                VMSB:     EQU   1
95  0002                VLSB:     EQU   2
96  0003                VSEQ:     EQU   3
97  0004                MOTR:     EQU   4
98  0005                CMD:      EQU   5
99  0006                CONT:     EQU   6
100 0007                REW:      EQU   7
101 0000
102                     ;
103                     ;
104                     *******************IBG COUNT REGISTER**********************
105                     *
106 1000                POSITION: EQU   1000H        IBG POSITION  CNT REG       SET IBG COUNTER
107                     *                                                        STOP
```

```
                                *                                                    END OF GAP
                                *
                                ************VELOCITY REGISTER MOST SIGNIFICANT BYTE********
                                ;
1001                            VELMSB:   EQU   1001H          VELOCITY COUNT BITS 8,9,A,B
                                *
0005                            SEL125:   EQU   5              SELECT BIT FOR 125 IPS (ACTIVE LOW)
0006                            SEL75:    EQU   6              SELECT BIT FOR 75 IPS (ACTIVE LOW)
0007                            SEL50:    EQU   7              SELECT BIT FOR 50 IPS (ACTIVE LOW)
                                ;
                                ***********VELOCITY REGISTER LEAST SIGNIFICANT BYTE*******
                                ;
1002                            VELOCITY  EQU   1002H          VELOCITY CNT,NUMBER OF CLOCKS BETWEEN TACHS
                                ;                              CLEARS INTERRUPT FLIP-FLOP) CLOCK= .226 NAN
                                ;
                                ;
                                ****************VELOCITY OUTPUT REGISTER*****************
                                ;
1003                            VELTEST:  EQU   1003H          VELOCITY REGISTER FOR SEQUENCER 'A' BUS
                                ;
                                ;
                                ************D/A CONVERTER PRESET REGISTER*****************
                                ;
1004                            MOTOR:    EQU   1004H          OUTPUT TO D/A CONVERTER FOR CAPSTAN MOTOR
                                ;
                                ;
                                *****************   COMMAND REGISTER   ******************
                                ;
1005                            COMMAND:  EQU   1005H          COMMANDS INPUT REGISTER
                                ;
0000                            POLARITY: EQU   0              POLARITY TEST BIT
0001                            PWRSAFE:  EQU   1              POWER SAFE LINE STATUS
0002                            IBGCNTR:  EQU   2              IBG COUNT ENABLE (ACTIVE LOW)
0003                            HP:       EQU   3              HP card present test
0004                            RWND:     EQU   4              REWIND SIGNAL FOR CAPSTAN (ACTIVE LOW)
0005                            READY:    EQU   5              READY SIGNAL FOR CAPSTAN (ACTIVE LOW)
0006                            FORWARD:  EQU   6              FORWARD MOTION COMMAND (ACTIVE LOW)
0007                            GO:       EQU   7              GO COMMAND (ACTIVE LOW)
                                ;
                                *****************   CONTROL REGISTER   *******************
                                ;
1006                            CONTROL:  EQU   1006H          CONTROL OUTPUTS
                                ;
0000                            NMIENBL:  EQU   0              NMI ENABLE LINE
0001                            TESTLED:  EQU   1              TEST LED OUTPUT
0002                            PARKED:   EQU   2
                                *
                                *****************   REWIND REGISTER    *****************
                                ;
1007                            REWIND:   EQU   1007H          REWIND INPUT FROM SEQUENCER ('B' BUS)
                                ;
                                ;
4200                            CRTBUF:   EQU   4200H          (CRT display for debugging)
0842                            SHOWDE: EQU 0842H
0877                            SHOWBC:   EQU 0877H
```

```
163  088F                SHOWA:      EQU 088FH
164                      ;
165                      ***************************************************************
166                      *                                                             *
167                      *                  REGISTER ASSIGNMENTS                       *
168                      *                                                             *
169                      ***************************************************************
170  0000
171  0000
172  0000
173                      *   REGISTER BANK 0  B  FORWARD TRIM
174                      *                    C  REVERSE TRIM
175                      *                    DE TIME DELAY COUNTER
176                      *                    D  DIRECTION FLAG FOR STOP (BIT 0)
177                      *                    HL ADDRESS POINTER (START)/(STOP)
178                      *                    H  STOP LOCK NULL (STOP LOCK)
179                      *                    L  LAST POSITION (STOP LOCK)
180  0000
181  0000
182  0000
183                      *   REGISTER BANK 1  B'  TACH LINE COUNT
184                      *                    C'  TRIM IN USE
185                      *                    DE' LOOKUP TABLE POINTER (ACC)
186                      *                    D'  ERROR INTEGRATOR (RUN)
187                      *                    E'  VELOCITY COUNT (RUN)
188                      *                    HL' I/O POINTER
189                      *                    A'  TEMPORARY STORAGE
190  0000
191  0000
192                      *                    IX INTERRUPT VECTOR
193                      *                    IY SSTACK POINTER RESET CONSTANT
194                      *                    I       D/A NULL        BITS 0, 1, 2
195                      *                            SET TO '1'      BITS 3, 4
196                      *                            NULL POLARITY   BIT  7
197  0000
198  0000
199  0000
200                      *******   CONSTANTS
201                      ;
202                      ;
203  005E                NULL:       EQU   94            MOTOR NOMINAL NULL COMMAND
204  0056                NULLMIN:    EQU   86
205  004E                MAXSTP:     EQU   4EH           MAXIMUN CURRENT COMMAND TO STOP
206  0055                MAX:        EQU   85            MAXIMUM CURRENT COMMAND
207  000F                MASK:       EQU   0FH           VELOCITY MSB MASK
208  0007                BANK:       EQU   7             Z80 REGISTER BANK SELECT
209  0002                LEDNMIOF:   EQU   2             LED OFF AND NMI DISABLED
210  0003                NOLEDNMI:   EQU   3             LED OFF AND NMI ENABLED
211  0007                NULLPOL:    EQU   7             NULL POLARITY
212  007D                STOPDIST:   EQU   125           STOP DISTANCE
213  0000                STOPDIR:    EQU   0             STOP DIRECTION FLAG
214  4000                SSTACK:      EQU   4000H
215  0080                INTEGR:     EQU   80H           servo integrator constant
216                      ;
```

```
                ;*****************************************************
                ;*                                                   *
                ;*                  INTERRUPT STRUCTURE              *
                ;*                                                   *
                ;*****************************************************
                ;
                ;   NON-MASKABLE INTERRUPT      SET ON +GO; EXECUTES 'GO' ROUTINE AT 6
                ;                               NMI INPUT IS DISABLED BY BIT 0 OF 'CON
                ;
                ;   MASKABLE INTERRUPT          SET ON TACH LINE BY VELOCITY SEQUENCER
                ;       (MODE 1)                FLIP-FLOP (K42) LATCHES INTERRUPT
                ;                               FLIP-FLOP CLEARED BY READ TO 'VELTEST'
                ;                               EXECUTES ROUTINE AT 38H
                ;
0000
                ;*****************************************************
                ;*****************************************************
                ;*                                                   *
                ;*                INITIALIZATION ROUTINE             *
                ;*                                                   *
                ;*****************************************************
                ;*****************************************************
                ;
                ;
0000 00         A0:     NOP             THIS REPROGRAMS 'RESET' KEY TO PERFORM A 'BREAK'
0001 00             NOP
0002 00             NOP
                ;                           SET TO 00,00,00 FOR EPROM
                ;       DI
                ;       LD      HL,0D800H   CRT ADDRESS TO DISPLAY WORKING REGISTERS
                ;       LD      (CRTBUF),HL
                ;
                ;
0003 AF         START:  XOR     A
0004 32 06 10           LD      (CONTROL),A TEST LED ON,NMI DISABLE,CAPSTAN PARKED BIT
0007 F3                 DI
0008 C3 65 05           JP      NULLSET     FIND D/A NULL
                ;
                        ORG     10H
0010 C3 42 08           JP      SHOWDE      DISPLAY DE AND RETURN
                ;
                        ORG     18H
0018 C3 77 08           JP      SHOWBC
                ;
                        ORG     20H
0020 3A 00 10           LD      A,(1000H)
0023 C3 8F 08           JP      SHOWA
0026
                        ORG     30H
                ;
0030 C3 44 04   A30:    JP      00444H      SOFTWARE BREAK -- AMOS SYSTEM
0033
0033
                ;
```

```
                                ;*****************************************************************
                                ;*                                                               *
                                ;*                      VELOCITY INTERRUPT                       *
                                ;*          ON PHASE A TACH (IF INTERRUPTS ARE ENABLED)           *
                                ;*                                                               *
                                ;*****************************************************************
                                ;
                                        ORG   38H
                                ;
0038  DD E9                     VELINT: JP    (IX)          VECTOR TO START/RUN ROUTINE (SPEED DEPENDEN
                                ;
                                ;*********
                                ;*
                                ;*       COMMAND IDLE LOOP
                                ;*
                                ;*********
                                ;*
                                ;
003A  ED 57                     PREIDLE: LD   A,I           0; compute real_null for motor
003C  CB 7F                              BIT  NULLPOL,A
003E  20 08                              JR   NZ,PREID
0040  E6 07                              AND  7H
0042  ED 44                              NEG
0044  C6 5E                              ADD  A,NULL          add negetive bias
0046  18 04                              JR   PREIDL
0048  E6 07                    PREID:    AND  7H              add positive bias
004A  C6 5E                              ADD  A,NULL
004C                            PREIDL:
004C  32 04 10                           LD   (MOTOR),A
                                ;
004F                            IDLE:
004F  3E 02                              LD   A,2            0; disable NMI, reset park-bit
0051  32 06 10                           LD   (CONTROL),A    0;
0054  3A 05 10                  IDLE1:   LD   A,(COMMAND)    0;
0057  CB 7F                              BIT  GO,A           0; TEST -GO
0059  CA 66 00                           JP   Z,GOINT
005C  CB 6F                              BIT  READY,A        0; TEST -RDY
005E  CA 48 03                           JP   Z,STOPLOCK
0061  18 F1                              JR   IDLE1
                                ;
0063
                                ;*****************************************************************
                                ;*                                                               *
                                ;*                         GO INTERRUPT                          *
                                ;*                                                               *
                                ;*****************************************************************
                                        ORG   66H
                                ;
                                ;     ROUTINE MUST START AT ADDRESS 66H   (NMI VECTOR)
                                ;
0066  3E 02                     GOINT:   LD   A,LEDNMIOF    7; DISABLE NMI,RES CAPSTAN PARKED BIT
0068  32 06 10                           LD   (CONTROL),A   7;
                                ;
```

```
0068  CB 7C          BIT   BANK,H        7; TEST REGISTER BANK SELECTION
006D  CA 71 00       JP    Z,GOINT1
0070  D9             EXX                 0; SELECT REGISTER BANK 0
                     ;
0071  3E 00          GOINT1: LD  A,0       0; SET VELOCITY COUNT TO SEQUENCER TO '00'
0073  32 03 10       LD    (VELTEST),A
                     ;
                     ;
0076  21 01 10       GOINT2A: LD HL,VELMSB 0; LOAD VELOCITY MSB INPUT
0079  7E             GOINT2: LD  A,(HL)
007A  BE             CP    (HL)          0; VERIFY STABLE INPUT
007B  20 FC          JR    NZ,GOINT2
007D  E6 0F          AND   MASK
007F  1E 55          LD    E,MAX         0;  PRESET CURRENT LIMIT
0081  FE 02          CP    2
0083  D2 F3 00       JP    NC,ACC125     0; NORMAL STOP TIME
0086
0086  FE 01          CP    1             0; SHORT GO-DOWN
0088  28 3F          JR    Z,GOINT5
                     ;
                     ********* VELOCITY > 96 IPS
008A  21 02 10       GOINT3: LD  HL,VELOCITY  0;LOAD VELOCITY COUNT LSB
008D  7E             LD    A,(HL)        0;
008E  BE             CP    (HL)          0'
008F  20 F9          JR    NZ,GOINT3     0;
0091  5F             LD    E,A           0;
                     ;
0092  3A 01 10       LD    A,(VELMSB)    0;
0095  E6 0F          AND   MASK          0;
0097  FE 00          CP    0             0;
0099  20 CB          JR    NZ,GOINT      0;BAD INPUT; TRY AGAIN
                     ;
009B  78             LD    A,E           0;
009C  FE 9B          CP    155           0;
009E  DA 03 00       JP    C,START       0;CAPSTAN RUN-AWAY
                     ;
00A1  2E 05          LD    L,CMD         0; Index HL to command reg
00A3  CB 76          BIT   FORWARD,(HL)  0;
00A5  1E 34          LD    E,NULL-(MAX/2)    set current limit for reverse
00A7  C2 44 04       JP    NZ,ST125R     0;
                     ,
00AA  FE D2          CP    210           0;
00AC  38 06          JR    C,NOSTOP      0;
00AE  26 00          LD    H,0           0;
00B0  6F             LD    L,A           0;
00B1  C3 DE 00       JP    GOINT6        0;
                     ;                   0;
                     ;                   0;
00B4  78             NOSTOP: LD  A,B     0;CAPSTAN SPEED ABOVE 110 IPS
00B5  D9             EXX                 1;
00B6  4F             LD    C,A           1;
00B7  32 04 10       LD    (MOTOR),A     1;
00BA  5F             LD    E,A           1;
00BB  16 07          LD    D,.HIGH.(TABLE2)  1;SET PAGE POINTER
00BD  21 01 90       LD    HL,09001H     1; INITIALIZE I/O POINTER TO VELOCITY INPUT
```

65 60 55

```
00C0  DD 21 E5 01          LD    IX,ST125F3   1;
00C4  3A 02 10             LD    A,(VELOCITY) 1; CLEAR PENDING INTERRUPT
00C7  FB                   EI
00C8  76                   HALT
                    ;
                    ;
                    ******** VELOCITY GREATER THAN 48 IPS
00C9  21 02 10      GOINT5:  LD    HL,VELOCITY  0; INPUT VELOCITY COUNT LSB
00CC  7E                   LD    A,(HL)       0;
00CD  BE                   CP    (HL)         0;
00CE  20 F9                JR    NZ,GOINT5    0;
00D0  5F                   LD    E,A          0;
                    ;
00D1  3A 01 10             LD    A,(VELMSB)   0; VERIFY VELOCITY COUNT MSB IS STILL GOOD
00D4  E6 0F                AND   MASK         0;
00D6  FE 01                CP    1            0;
00D8  C2 86 00             JP    NZ,GOINT     0;BAD INPUT TRY AGAIN
00DB  26 01                LD    H,1          0;
00DD  6B                   LD    L,E          0;
                    ;
                    ;
                    ******** LOOK-UP CURRENT LIMIT
                    ;
00DE  29            GOINT6:  ADD   HL,HL        0; MULTIPLY BY 8
00DF  29                   ADD   HL,HL         0;
00E0  29                   ADD   HL,HL         0;
00E1  3E A1                LD    A,.LOW.(TABLE2)  0;COMPUTE LOOK-UP TABLE ADDRESS
00E3  84                   ADD   A,H
00E4  6F                   LD    L,A
00E5  26 07                LD    H,.HIGH.(TABLE2)
00E7  5E                   LD    E,(HL)       0;LOOK-UP MAXIMUM ACCELERATE CURRENT
00E8  3A 05 10             LD    A,(COMMAND)
                    * * * * * * * * * * * * *
                    *
                    *  THE NEXT TEST SHOULD BE "BIT HP"..BUT WAS CHANGED SO TOBE
                    *  COMPATIABLE WITH THE V.A02 EPROM...WHICH IS IN ERROR!!!
                    *
                    * * * * * * * * * * * * *
00EB
00EB  CB 77                BIT   FORWARD,A            test for HP card present
00ED  28 04                JR    Z,ACC125
00EF  3E 14                LD    A,14H           max that can be added (unless TABLE2 cha
00F1  83                   ADD   A,E
00F2  5F                   LD    E,A
00F3
                    ************************************************************
                    *                                                          *
                    *               ACCELERATION  CURRENT PROFILE              *
                    *                                                          *
                    ************************************************************
                    ;
                    ******** RAMP UP +CURRENT
                    ;
00F3  3A 05 10      ACC125:  LD    A,(COMMAND)  0;
```

```
435  00F6  CB 77          BIT   FORWARD,A     0;FORWARD?
436  00F8  20 10          JR    NZ,ACC125R    0;NO!
437                       ;
438  00FA  3E 5E          LD    A,NULL        0;
439  00FC  83             ADD   A,E           0;
440  00FD  5F             LD    E,A           0;
441  00FE  3E 68          LD    A,NULL+10     0;
442  0100  C6 03          ADD   A,3           0;CURRENT RAMP
443  0102  32 04 10       LD    (MOTOR),A
444  0105  BB             CP    E             0;TEST FOR MAXIMUM CURRENT
445  0106  38 F8          JR    C,ACC125A     0;
446  0108  18 0E          JR    ACC125B       0;
447                       ;                   0;
448                       ******* RAMP UP -CURRENT   0;
449                       ;
450  010A  3E 5E          LD    A,NULL        0;SUBTRACT CURRENT LIMIT FROM NULL
451  010C  93             SUB   E             0;
452  010D  5F             LD    E,A           0;
453  010E  3E 54          LD    A,NULL-10     0;
454  0110  D6 03          SUB   3             0;CURRENT RAMP
455  0112  32 04 10       LD    (MOTOR),A     0;
456  0115  BB             CP    E             0;TEST FOR MAXIMUM CURRENT
457  0116  30 F8          JR    NC,ACC125S    0;
458                       ;
459                       ;
460                       ********* HOLD CURRENT TILL VELOCITY = 65 IPS
461  0118  DD 21 24 01    LD    IX,ACC125C    0;LOAD VELOCITY INTERRUPT ADDRESS
462  011C  31 00 40       LD    SP,SSTACK      0;       REFRESH SSTACK POINTER
463  011F  3A 02 10       LD    A,(VELOCITY) 0; CLEAR ANY PENDING INTERRUPT
464  0122  FB             EI                  0;
465  0123  76             HALT                0;
466                       ;                   0;
467  0124  3A 01 10       LD    A,(VELMSB)    0;LOOK FOR VELOCITY COUNT < 200H
468  0127  E6 0F          AND   MASK          0;
469  0129  FE 01          CP    1             0;
470  012B  28 15          JR    Z,ACC125E     0;
471  012D  FE 00          CP    0             0;
472  012F  28 3C          JR    Z,ACC125J     0;
473  0131  3A 05 10       LD    A,(COMMAND)   0;
474  0134  CB 7F          BIT   GO,A          0;TEST GO FOR SHORT GO UP
475  0136  28 08          JR    Z,ACC125D
476  0138  CB 77          BIT   FORWARD,A
477  013A  CA 58 02       JP    Z,EXITGOF1
478  013D  C3 5F 02       JP    EXITGOR1
479  0140  FB             ACC125D: EI
480  0141  76             HALT
481                       ;
482  0142  3A 02 10       ACC125E: LD   A,(VELOCITY)   SYNC TO VELOCITY COUNT 180H
483  0145  FE F0          CP    0F0H
484  0147  30 F7          JR    NC,ACC125D
485  0149  D6 60          SUB   60H
486  014B  38 04          JR    C,ACC125G
487  014D  D6 08          ACC125F: SUB  8       DELAY .59 USEC FOR EACH COUNT OF VELOCITY E
488  014F  30 FC          JR    NC,ACC125F              (4.8 USEC PER LOOP)
```

```
489
490
491  0151  3A 05 10          ;
492                          ********  RAMP DOWN CURRENT
493  0154  CB 77             ACC125G:  LD    A,(COMMAND)
494  0156  C2 37 04          ;
495  0159  CB 7F             ACCHIS:   BIT   FORWARD,A     FORWARD MOTION?
496  015B  C2 58 02                    JP    NZ,ACC125T
497                                    BIT   GO,A
498  015E  7B                          JP    NZ,EXITGOF1
499  015F  D6 04             ;
500  0161  5F                ACC125H:  LD    A,E           RAMP CURRENT DOWN
501  0162  32 04 10                    SUB   4
502  0165  00                          LD    E,A
503  0166  00                          LD    (MOTOR),A
504  0167  FE A8                       NOP
505  0169  30 F3                       NOP
506  016B  18 08                       CP    168           LOOK FOR RAMP END POINT
507                                    JR    NC,ACC125H
508                                    JR    ST125F
509  016D  3A 05 10          ;
510  0170  CB 77             ;
511  0172  C2 44 04          ACC125J:  LD    A,(COMMAND)
512                                    BIT   FORWARD,A
513                                    JP    NZ,ST125R
514                          ;
515                          ;
516  0175  7B                ********  INITIALIZE REGISTER BANK 1 REGISTERS
517  0176  D9                ;
518  0177  4F                ST125F:   LD    A,B           0;SET FORWARD TRIM
519                                    EXX                 1;
520  0178  D9                          LD    C,A           1;
521  0179  7B                ;
522  017A  D9                          EXX                 0;
523  017B  D6 03                       LD    A,E           0; RAMP CURRENT DOWN
524  017D  32 04 10                    EXX                 1;
525  0180  5F                          SUB   3             1;
526                                    LD    (MOTOR),A     1;
527  0181  16 07                       LD    E,A           1;
528  0183  21 01 90          ;
529  0186  DD 21 97 01                 LD    D,.HIGH.(TABLE3)  1;SET PAGE POINTER
530  018A  3A 02 10                    LD    HL,09001H     1;INITIALIZE I/O POINTER TO VELOCITY INPUT
531  018D  FB                          LD    IX,ST125F1    1;
532                                    LD    A,(VELOCITY)  1; CLEAR PENDING INTERRUPT
533  018E  7B                          EI                  1;
534  018F  D6 01             ;
535  0191  32 04 10          ST125FA:  LD    A,E           1;
536  0194  5F                          SUB   1             1;WAIT FOR NEXT TACH LINE
537  0195  18 F9                       LD    (MOTOR),A     1;
538                                    LD    E,A           1;
539                                    JR    ST125FA       1;
540                          ;
541                          ;
542  0197  7E                ********  USE LOOK-UP TABLES TO ACCELERATE TO 115 IPS  (1/2 GAIN)
543  0198  E6 0F             ;
                             ST125F1:  LD    A,(HL)        1;LOAD VELOCITY COUNT MSB
                                       AND   MASK          1;
```

```
544  019A  FE 00
545  019C  CA C6 01
546  019F  FE 01
547  01A1  C2 B4 01
548  01A4  2C
549  01A5  7E
550  01A6  CB 3F
551  01A8  CB 3F
552  01AA  CB 3F
553  01AC  C6 81
554  01AE  5F
555  01AF  1A
556  01B0  81
557  01B1  32 04 10
558  01B4  2E 01
559  01B6  31 00 40
560  01B9  3A 02 10
561  01BC  3A 05 10
562  01BF  CB 7F
563  01C1  C2 57 02
564  01C4  FB
565  01C5  76
566
567
568  01C6  2C
569  01C7  7E
570  01C8  FE CD
571  01CA  38 19
572  01CC  2F
573  01CD  23
574  01CE  77
575  01CF  2F
576  01D0  CB 3F
577  01D2  5F
578  01D3  1A
579  01D4  81
580  01D5  2C
581  01D6  77
582
583  01D7  2C
584  01D8  7E
585  01D9  CB 7F
586  01DB  C2 57 02
587
588  01DE  31 00 40
589  01E1  2E 01
590  01E3  FB
591  01E4  76
592
593  01E5  16 80
594  01E7  79
595  01E8  D6 8F
596  01EA  4F
597  01EB  2E 02
```

```
                CP    0               1;VELOCITY > 96 IPS?
                JP    Z,ST125F2       1;
                CP    1               1;
                JP    NZ,ST125F1A     1;
                INC   L               1;COMPUTE LOOK-UP TABLE ADDRESS
                LD    A,(HL)          1;
                SRL   A               1;
                SRL   A               1;
                SRL   A               1;
                ADD   A,.LOW.(TABLE3)  1;
                LD    E,A             1;
                LD    A,(DE)          1;LOOK-UP DESIRED CURRENT
                ADD   A,C             1;
                LD    (MOTOR),A       1;OUTPUT CURRENT
ST125F1A:       LD    L,1             1;
                LD    SP,SSTACK        1;
                LD    A,(VELOCITY)    1; CLEAR INTERRUPT FLIP-FLOP
                LD    A,(COMMAND)     1;
                BIT   GO,A
                JP    NZ,EXITGOF
                EI
                HALT
;
;
ST125F2:        INC   L
                LD    A,(HL)          1;LOAD VELOCITY COUNT
                CP    205             1;TEST FOR END OF LOOK-UP TABLE
                JR    C,ST125F3       1;
                CPL                   1; COMPLEMENT SPEED COUNT
                INC   HL              1;POINT TO VELOCITY OUTPUT REGISTER
                LD    (HL),A          1;OUTPUT VELOCITY COUNT TO SEQUENCER
                CPL                   1;
                SRL   A               1;DIVIDE BY 2
                LD    E,A             1;SET UP LOOK-UP TABLE ADDRESS
                LD    A,(DE)          1;
                ADD   A,C             1;
                INC   L               1;POINT TO MOTOR
                LD    (HL),A          1;OUTPUT CURRENT TO MOTOR
;                                     1;
                INC   L               1;POINT TO COMMAND REGISTER
                LD    A,(HL)          1;
                BIT   GO,A            1;GO COMMAND?
                JP    NZ,EXITGOF      1;NO!
;                                     1;
                LD    SP,SSTACK        1;       REFRESH SSTACK POINTER
                LD    L,1             1;
                EI                    1;
                HALT                  1;
;                                     1;
ST125F3:        LD    D,INTEGR        1;INITIALIZE INTEGRATOR
                LD    A,C             1;
                SUB   191             1;ADJUST OFFSET FOR 1 AMP RUNNING CURRENT
                LD    C,A             1;
                LD    L,2             1;POINT TO VELOCITY REGISTER
```

```
598  01ED  UD 21 F1 01          .       LD    IX,RUN125F   1;SET FORWARD MOTION ROUTINE
599  01F1
600  01F1
601                             ********************************************************
602                             *                                                      *
603                             *                  RUN 125 IPS FORWARD                 *
604                             *   NOTE:   Integrator set for  128 TACH               *
605                             *               12 msec (0.7 inch or 4K record         *
606                             ********************************************************
607                             ;
608  01F1  7E                   RUN125F1  LD    A,(HL)       1;LOAD VELOCITY COUNT / CLEAR INTERRUPT FLI
609  01F2  2F                             CPL                 1;COMPLEMENT SPEED COUNT
610  01F3  2C                             INC   L             1;POINT TO VELOCITY OUTPUT REGISTER (VELTES
611  01F4  77                             LD    (HL),A        1;  OUT VELOCITY COUNT TO SEQUENCER
612  01F5  2F                             CPL
613  01F6  5F                             LD    E,A           1;
614  01F7  81                             ADD   A,C           1;ADD TRIM
615  01F8  30 51                          JR    NC,ERROR      1;TEST FOR SPEED OUT OF LIMITS
616  01FA  2C                             INC   L
617  01FB  77                             LD    (HL),A        1;OUTPUT ACCELERATE COMMAND
618  01FC
619  01FC
620  01FC
621                             ********  TEST COMMANDS (EVERY TACH LINE)
622                             ;
623  01FC  2C                             INC   L             1;POINT TO COMMAND REGISTER
624  01FD  7E                             LD    A,(HL)        1;LOAD COMMAND BITS
625  01FE  E6 C0                          AND   0C0H          1;TEST FOR STOP OR REVERSE COMMANDS
626  0200  20 2C                          JR    NZ,EXIT125F   1;
627                             !
628  0202  31 00 40                       LD    SP,SSTACK       RESET SSTACK POINTER
629  0205  2E 02                          LD    L,2           1;RESET I/O POINTER
630  0207
631  0207
632                             ********  TRIM INTEGRATION ROUTINE
633                             ;
634  0207  7B                             LD    A,E           1;TEST COUNT FOR ERROR
635  0208  D6 C4                          SUB   196
636  020A  38 12                          JR    C,RUN125F2    1;NEGATIVE ERROR
637  020C  28 03                          JR    Z,RUN125F0    1;ZERO ERROR
638                             ;
639  020E  14                             INC   D             1;INCREMENT INTEGRATOR  (CAPSTAN SLOW)
640  020F  28 02                          JR    Z,RUN125F1    1;ADJUST TRIM IF COUNTER OVERFLOW
641  0211  FB                   RUN125F0: EI
642  0212  76                             HALT
643                             !
644                             ;
645                             ;
646  0213                       RUN125F1:
647  0213  16 80                          LD    D,INTEGR      1;reset integrator
648  0215  0C                             INC   C             1;    INCREMENT TRIM REGISTER
649  0216  3E 80                          LD    A,080H
650  0218  B9                             CP    C
651  0219  30 01                          JR    NC,RUN125FA   1;TEST UPPER LIMIT OF TRIM
```

```
652  0218  4F                LD    C,A
653  021C  FB          RUN125FA: EI                  1;
654  021D  76                  HALT                  1;
655                     ;
656  021E  15          RUN125F2: DEC   D             1;DECREMENT INTEGRATOR  (CAPSTAN FAST)
657  021F  28 02               JR    Z,RUN125F3      1;
658  0221  FB                  EI                    1;
659  0222  76                  HALT                  1;
660                     ;                           1;
661  0223              RUN125F3:
662  0223  16 80               LD    D,INTEGR        1; reset integrator
663  0225  0D                  DEC   C               1;DECREMENT TRIM REGISTER
664  0226  3E 70               LD    A,70H           1;'
665  0228  B9                  CP    C                1;
666  0229  38 01               JR    C,RUN125F4      1;TEST LOWER TRIM LIMIT
667  022B  4F                  LD    C,A             1;
668  022C  FB          RUN125F4: EI                  1;
669  022D  76                  HALT                  1;
670                     ;
671                     ;
672                     ********  EXIT RUN ROUTINE
673                     ;
674  022E  F3          EXIT125F: DI
675  022F  79                  LD    A,C             1;
676  0230  C6 BF               ADD   A,191           1;CONVERT TO D/A OFFSET  (ADD VELOCITY TARG
677  0232  D9                  EXX                   0;
678  0233  47                  LD    B,A             0; SAVE NEW D/A OFFSET FOR +125 IPS
679                     ;                           0;
680  0234  3E 02               LD    A,2             0;DISABLE NMI,TURN LED OFF,RES.CAPS.PARKED
681  0236  32 06 10            LD    (CONTROL),A     0;
682  0239  3A 05 10            LD    A,(COMMAND)
683  023C  CB 5F               BIT   HP,A                test for HP card present
684  023E  3E 10               LD    A,NULL-MAXSTP       SET MAXIMUM DECELERATE CURRENT
685  0240  28 02               JR    Z,NOHP
686  0242  D6 0A               SUB 10                    increase stopping current for HP
687  0244              NOHP:
688  0244  32 04 10            LD    (MOTOR),A       0;
689                     ;                           0;'
690  0247  16 00               LD    D,0             0;SET FOWARD STOP FLAG
691  0249  18 18               JR    STOP125         0;
692                     ;
693                     ;
694
695  0248  D9          ********  OVERSPEED/UNDERSPEED FAULT
696  024C  3A 01 10    ERROR:    EXX                 1;SELECT REGISTER BANK 0
697  024F  E6 0F               LD    A,(VELMSB)      0;
698  0251  C2 66 00            AND   MASK            0;
699  0254  C3 03 00            JP    NZ,GOINT        0;UNDER SPEED EXIT
                               JP    START           0;OVER SPEED EXIT
701                     ;
702                     ;
703                     ;
```

```
704
705
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720
721  0257  D9              ********************************************************
722  0258  3E 20           ********************************************************
723  025A  16 00           *                                                      *
724  025C  18 05           *                      S T O P                         *
725                        *      |-----------------------------------------|     *
726  025E  D9              *      |  NOTE: unless otherwise noted STOP routine |     *
727  025F  3E 9C           *      |        uses register bank-0               |     *
728  0261  16 01           *      |-----------------------------------------|     *
729  0263  32 04 10        *                                                      *
730                        ********************************************************
731                        ********************************************************
732                        ;
733  0266  1E 00           ;
734  0268  FD 21 00 10     ********  MAINTAIN MAXIMUM DECELERATION TO 55 IPS
735                        ;
736  026C  1C              *         EXITGO ENTRIES FROM A SHORT GO-UP TIME
737  026D  FD 7E 02        ;
738  0270  2F              EXITGOF:  EXX                 0;
739  0271  FD 77 03        EXITGOF1: LD    A,NULL-(MAXSTP-16)
740  0274  FD CB 05 7E              LD    D,0
741  0278  20 1D                    JR    EXITGO
742                        ;
743  027A  CB 42           EXITGOR:  EXX                 0;
744  027C  20 5A           EXITGOR1: LD    A,NULL+(MAXSTP-16)
745                                 LD    D,1
746  027E  7B              EXITGO:   LD    (MOTOR),A
747  027F  FE 04           *
748  0281  3E 38           **********
749  0283  38 46           *
750                        STOP125:  LD    E,0           INITIALIZE COUNTER
751  0285  7B                       LD    IY,POSITION   index to I/O ports
752  0286  FE 0F           ;
753  0288  30 3F           STOP125A: INC   E
754                                 LD    A,(IY+VLSB)
755  028A  3E 22                    CPL                 sent velocity to "A"-bus
756  028C  C6 01                    LD    (IY+VSEQ),A
757  028E  32 04 10                 BIT   GO,(IY+CMD)   command to start capstan set?
                                    JR    NZ,STOP125B   NO!
                           ;
                                    BIT   STOPDIR,D     EXIT VIA RAMP 1 IF REVERSE MOTION
                                    JR    NZ,RAMP1            (STOP DIRECTION FLAG IS BIT  0 OF 'D')
                           ;
                                    LD    A,E           EXIT VIA RAMP 0 IF STOP < 100 USEC
                                    CP    4
                                    LD    A,NULL-35     SET START POINT FOR RAMP
                                    JR    C,RAMP00
                           ;
                                    LD    A,E           EXIT VIA RAMP 0 IF STOP > 300 USEC
                                    CP    15
                                    JR    NC,RAMP0
                           ;
                                    LD    A,NULL-60     EXIT VIA RAMP 2 IF STOP BETWEEN 100-300 USE
                           RAMP2:   ADD   A,1
                                    LD    (MOTOR),A
```

```
0291  FE 56              CP    NULL-8
0293  38 F7              JR    C,RAMP2
0295  18 4C              JR    STOP125F
                    ;
0297                    STOP1258:
0297  FD 7E 01           LD    A,(IY+VMSB)
029A  FD BE 01           CP    (IY+VMSB)     VERIFY INPUT
029D  20 F8              JR    NZ,STOP1258
029F  E6 0F              AND   MASK
02A1  28 C9              JR    Z,STOP125A    loop till velocity < 97ips (count <100h)
02A3  FE 01              CP    1
02A5  C2 E3 02           JP    NZ,STOP125F   INVALID STOP
                    *
                    **********
                    *
                    *         Entry for velocity < 97ips
                    *           took about 500usec to deaccelerate
                    *
                    **********
                    *
02A8  FD 36 03 00        LD    (IY+VSEQ),0   set sequencer 'A'-bus =0
02AC  FD 7E 02      STOP125C: LD   A,(IY+VLSB)
02AF  FD BE 02           CP    (IY+VLSB)     VERIFY INPUT
02B2  20 F8              JR    NZ,STOP125C
                    ;
                    *                         SET UP DELAY COUNT
02B4  C6 80              ADD   A,80H         ADD 128
02B6  30 02              JR    NC,STOP125E
02B8  3E FF              LD    A,0FFH        NO DELAY
                    ;
02BA                    STOP125E:
02BA  FD CB 05 7E        BIT   GO,(IY+CMD)   GO COMMAND?
02BE  28 05              JR    Z,RAMP        YES!
                    ;
02C0  C6 0E              ADD   A,14          delay to approx 65ips
02C2  00                 NOP
02C3  30 F5              JR    NC,STOP125E
                    ;
02C5  CB 42              RAMP:     BIT   STOPDIR,D     STOP DIRECTION FLAG ON?
02C7  20 0F              JR    NZ,RAMP1
                    *
                    **********
                    *         200usec ramp
                    *
02C9  3E 18              RAMP0:    LD    A,NULL-70     SET STARTING POINT FOR RAMP
02CB  C6 03              RAMP00:   ADD   A,3
02CD  32 04 10           LD    (MOTOR),A
02D0  FE 56              CP    NULL-8
02D2  00                 NOP
02D3  00                 NOP
02D4  38 F5              JR    C,RAMP00
02D6  18 08              JR    STOP125F
                    ;
02D8  3E A4              RAMP1:    LD    A,NULL+70
02DA  D6 03              RAMP11:   SUB   3
```

```
0813  02DC  32 04 10                    LD    (MOTOR),A
0814  02DF  FE 66                       CP    NULL+8
0815  02E1  30 F7                       JR    NC,RAMP11
0816                                ;
0817                                ************
0818                                *
0819                                *  if  IBG enabled
0820                                *       set motor current = null
0821                                *          while  (position count) < 125
0822                                *                if  1.2msec timeout
0823                                *                    enter STOPLOCK
0824                                *                if  position counter indicates a direction change
0825                                *                    enter STOPLOCK
0826                                *                loop
0827                                *           then compute STOP_PULSE
0828                                *       then STOPLOCK
0829                                *   else goto IDLE
0830                                *
0831                                ************
0832  02E3                          STOP125F:
0833  02E3  FD 36 04 5E                    LD    (IY+MOTR),NULL
0834                                *                             ENABLE NMI,TURN LED OFF,RES CAPS.PARKED
0835  02E7  FD 36 06 03                    LD    (IY+CONT),NOLEDNMI
0836  02EB  FD CB 05 58                    BIT   IBGCNTR,(IY+CMD)
0837  02EF  C2 3A 00                       JP    NZ,PREIDLE      exit if IBG COUNTER disabeled
0838  02F2  16 48                          LD    D,75            START COUNT
0839  02F4  1E D0                          LD    E,0D0H          set 1.2msec timer
0840                                ;
0841  02F8                          STOP125H:
0842  02F6  FD 7E 00                       LD    A,(IY+POSTN)
0843  02F9  FD BE 00                       CP    (IY+POSTN)      VERIFY STABLE INPUT
0844  02FC  20 F8                          JR    NZ,STOP125H
0845                                ;
0846  02FE  1C                             INC   E               TEST TIME LIMIT
0847  02FF  28 47                          JR    Z,STOPLOCK
0848                                ;
0849  0301  BA                             CP    D               TEST FOR direction change
0850  0302  38 44                          JR    C,STOPLOCK
0851  0304  57                             LD    D,A             save 'last' position
0852                                ;
0853  0305  FE 7D                          CP    125             position = 125?
0854  0307  38 ED                          JR    C,STOP125H      WAIT LOOP
0855                                ************
0856                                *
0857                                *         COMPUTE AND OUTPUT .7 MSEC STOP PULSE
0858                                *
0859                                ************
0860  0309                          STOP125L:
0861                                *         ASSEMBLE THE 5 MSB O VELOCITY COUNT
0862
0863  0309  FD 7E 01                       LD    A,(IY+VMSB)
0864  030C  FD BE 01                       CP    (IY+VMSB)
0865  030F  20 F8                          JR    NZ,STOP125L
0866  0311  E6 0F                          AND   MASK                          (EACH BIT = 128 COUNTS)
0867  0313  5F                             LD    E,A
```

```
868  0314  FD 7E 02
869  0317  FD BE 02
870  031A  20 F8
871  031C  17
872  031D  CB 13
873  031F  16 08
874  0321  3E B5
875  0323  83
876  0324  FE C4
877  0326  30 04
878  0328  6F
879  0329  26 07
880  032B  56
881  032C
882  032C  FD CB 05 76
883  0330  7A
884  0331  28 09
885  0333  CB 3F
886  0335  CB 3A
887  0337  CB 3A
888  0339  82
889  033A  ED 44
890  033C  ED 44
891  033E  C6 5E
892  0340  32 04 10
893
894  0343  3E A0
895  0345  3D
896  0346  20 FD
897
898
899
900
901
902
903
904
905
906
907
908  0348
909  0348  ED 57
910  034A  CB 7F
911  034C  20 08
912  034E  E6 07
913  0350  ED 44
914  0352  C6 5E
915  0354  10 04
916  0356  E6 07
917  0358  C6 5E
918  035A  32 04 10
919  035D  08
920
921  035E  3A 05 10
```

```
STOPL1:  LD    A,(IY+VLSB)
         CP    (IY+VLSB)
         JR    NZ,STOPL1
         RLA                    MULTIPLY BY 2
         RL    E
         LD    D,0              DEFAULT CURRENT
         LD    A,.LOW.(PULSETBL) COMPUTE LOOK-UP TABLE ADDRESS
         ADD   A,E
         CP        .LOW.(PULSETBL+15)  TEST FOR END OF TABLE
         JR    NC,STOP125M
         LD    L,A
         LD    H,.HIGH.(PULSETBL)
         LD    D,(HL)           LOOK-UP PULSE CURRENT
STOP125M:
         BIT   FORWARD,(IY+CMD)  FORWARD MOTION?
         LD    A,D
         JR    Z,STOP125N       YES!
         SRL   A                NO! USE 3/4 GAIN FOR REVERSE STOP
         SRL   D
         SRL   D
         ADD   A,D
         NEG
STOP125N: NEG
         ADD   A,NULL
         LD    (MOTOR),A        OUTPUT CURRENT TO MOTOR
;
         LD    A,160
STOP125P: DEC  A                TIME OUT  (.7 MSEC)
         JR    NZ,STOP125P
;
*****************************************************************
*****************************************************************
*                                                               *
*          STOP-LOCK: MAINTAINS 18G COUNT AT:125                *
*                                                               *
*****************************************************************
*****************************************************************
;
*        COMPUTE real_null
;
STOPLOCK:
         LD    A,I
         BIT   NULLPOL,A
         JR    NZ,SPLK0A
         AND   7H
         NEG
         ADD   A,NULL           add negative bias
         JR    STPLOCK
SPLK0A:  AND   7H
         ADD   A,NULL           add positive bias
STPLOCK: LD    (MOTOR),A
         EX    AF,AF'           save real_null
;
         LD    A,(COMMAND)
```

```
922  0361  E6 24              AND   24H           TEST FOR -READY AND IBG ENABLED
923  0363  C2 4F 00           JP    NZ,IDLE
924  0366  3E 07              LD    A,7           ENABLE NMI INPUT; TURN OFF TEST LAMP
925                                                SET CAPSTAN PARKED BIT
926  0368  32 06 10           LD    (CONTROL),A
927
928  0368  CB 7C              BIT   BANK,H        REGISTER BANK ZERO?
929  036D  28 01              JR    Z,STP1        YES!
930  036F  D9                 EXX                 NO!SELECT REGISTER BANK 0
931
932
933  0370                    STP1:
934  0370  08                 EX    AF,AF'        restore real_null
935  0371  67                 LD    H,A            'H'-reg = real_null
936
937  0372  2E 7D              LD    L,7DH         seed 'LAST POSITION' storage reg
938
939
940
941                           ******************************************************
942                           *         STOP LOCK POSITION SERVO                   *
943                           *         STOP-LOCK (TARGET = 7DH)                   *
944                           *         uses register bank-0                       *
945                           *    NOTE...no test of command lines during this     *
946                           *         20msec timer!!                             *
947                           ******************************************************
948
949  0374                    STOPLCK:
950  0374  FD 21 00 10           LD    IY,POSITION
951  0378  11 E8 03           LD    DE,1000       SET COUNTER (USED FOR PULSE, DELAY, VELOCIT
952  037B  7C                 LD    A,H           NULL CURRENT TO MOTOR
953  037C  32 04 10           LD    (MOTOR),A
954  037F                    SPOS2:
955  037F  FD 7E 00           LD    A,(IY+POSTN)
956  0382  FD BE 00           CP    (IY+POSTN)
957  0385  20 F8              JR    NZ,SPOS2
958  0387  FE 7D              CP    STOPDIST      does current position = target position
959  0389  20 06              JR    NZ,SPLK1H     JUMP TO OUTPUT ROUTINE IF DIFFERENT
960
961
962  038B  1B                 DEC   DE            AFTER 4000 TESTS RUN CURRENT OUTPUT
963  038C  7B                 LD    A,E
964  038D  B2                 OR    D
965  038E  C2 7F 03           JP    NZ,SPOS2      complete 20msec delay
966
967                           *
968                           *         COMPUTE CORRECTION CURRENT
969                           *
970  0391                    SPLK1H:
971  0391  FD 7E 00           LD    A,(IY+POSTN)
972  0394  FD BE 00           CP    (IY+POSTN)
973  0397  20 F8              JR    NZ,SPLK1H
974  0399  FE 7D              CP    STOPDIST      determine which side of target position
975  039B  28 07              JR    Z,STOPLCK     do another delay if position = 125
976  039D  30 39              JR    NC,PASTSTPH   current position > target position (125)
```

```
977
978
979  039F  BD
980  03A0  6F
981  03A1  38 10
982  03A3  D6 7D
983  03A5  ED 44
984  03A7  FE 10
985  03A9  30 06
986  03AB
987  03AB  11 C5 07
988  03AE  83
989  03AF  5F
990  03B0  1A
991  03B1
992  03B1  18 0E
993
994  03B3  D6 7D
995  03B5  ED 44
996  03B7  FE 10
997  03B9  30 06
998  03BB
999  03BB  11 C5 07
1000 03BE  83
1001 03BF  5F
1002 03C0  1A
1003 03C1  FE 55
1004 03C3  38 02
1005 03C5  3E 55
1006 03C7  5F
1007 03C8  3A 05 10
1008 03CB  CB 77
1009 03CD  78
1010 03CE  28 02
1011 03D0  ED 44
1012 03D2  84
1013 03D3  32 04 10
1014 03D6  18 33
1015 03D8
1016 03D8
1017
1018
1019 03D8  BD
1020 03D9  6F
1021 03DA  30 0E
1022 03DC  D6 7D
1023 03DE  FE 10
1024 03E0  30 06
1025 03E2
1026 03E2  11 C5 07
1027 03E5  83
1028 03E6  5F
1029 03E7  1A
1030 03E8
1031 03E8  18 0C
```

```
;                                  else current position < target position
;
                CP      L          COMPARE TO LAST POSITION
                LD      L,A        SAVE NEW POSITION
                JR      C,SPLK3H   VELOCITY TOWARDS ZERO POSITION
                SUB     STOPDIST
                NEG
                CP      16         POS COUNT DIFFERENCE =< 16?
                JR      NC,SPLK1H1 NO!
SPLK1H1A:
                LD      DE,STLCKTBL
                ADD     A,E
                LD      E,A
                LD      A,(DE)             FETCH TABLE VALUE
SPLK1H1:
                JR      SPLK4H
;
SPLK3H:         SUB     STOPDIST
                NEG
                CP      16         POS COUNT DIFFERENCE =< 16?
                JR      NC,SPLK4H  NO!
SPLK3H1A:
                LD      DE,STLCKTBL
                ADD     A,E
                LD      E,A
                LD      A,(DE)     FETCH TABLE VALUE
SPLK4H:         CP      MAX        TEST FOR CURRENT LIMIT
                JR      C,SPLK5H
                LD      A,MAX
SPLK5H:         LD      E,A
                LD      A,(COMMAND) POINT TO COMMAND REGISTER
                BIT     FORWARD,A  FORWARD MOTION?
                LD      A,E
                JR      Z,SPLK6H   YES!
                NEG                NO!NEGATE ERROR FOR REVERSE COMMAND
SPLK6H:         ADD     A,H        ADD D/A OFFSET
                LD      (MOTOR),A  MOTOR CURRENT = POSITION ERROR
                JR      SPLKTIME

********  PAST STOP POINT (POSITION > 125)
;
PASTSTPH:       CP      L
                LD      L,A        SAVE NEW POSITION
                JR      NC,SPLK7H
                SUB     STOPDIST
                CP      16         POS COUNT DIFFERENCE =< 16?
                JR      NC,PASTSTP1 NO!
PSTSTP1A:
                LD      DE,STLCKTBL
                ADD     A,E
                LD      E,A
                LD      A,(DE)     FETCH TABLE VALUE
PASTSTP1:
                JR      SPLK8H
```

```
1032
1033  03EA  D6 7D
1034  03EC  FE 10
1035  03EE  30 06
1036  03F0
1037  03F0  11 C5 07
1038  03F3  83
1039  03F4  5F
1040  03F5  1A
1041  03F8  FE 55
1042  03F8  38 02
1043  03FA  3E 55
1044  03FC  5F
1045  03FD  3A 05 10
1046  0400  CB 77
1047  0402  7B
1048  0403  20 02
1049  0405  ED 44
1050  0407  84
1051  0408  32 04 10
1052
1053
1054
1055
1056  0408  1E 14
1057
1058  040D  1D
1059  040E  28 1B
1060
1061  0410  3A 05 10
1062  0413  CB 7F
1063  0415  CA 66 00
1064  0418  E6 24
1065  041A  C2 3A 00
1066
1067  041D
1068  041D  FD 7E 00
1069  0420  FD BE 00
1070  0423  20 F8
1071  0425  BD
1072  0426  00
1073  0427  00
1074  0428  00
1075
1076
1077  0429  18 E2
1078
1079
1080
1081  042B
1082  042B  7C
1083  042C  32 04 10
1084  042F  1E 80
1085  0431  1D
1086  0432  20 FD
```

```
;
SPLK7H:   SUB   STOPDIST
          CP    16              POS COUNT DIFFERENCE =< 16?
          JR    NC,SPLK8H       NO!
SPLK7H1A:
          LD    DE,STLCKTBL
          ADD   A,E
          LD    E,A
          LD    A,(DE)          FETCH TABLE VALUE
SPLK8H:   CP    MAX             TEST FOR CURRENT LIMIT
          JR    C,SPLK9H
          LD    A,MAX
SPLK9H:   LD    E,A
          LD    A,(COMMAND)
          BIT   FORWARD,A       FORWARD MOTION?
          LD    A,E
          JR    NZ,SPLKAH       NO!
          NEG
SPLKAH:   ADD   A,H
          LD    (MOTOR),A       MOTOR CURRENT = POSITION ERROR
;
********  TIME OUT MAXIMUM CURRENT PULSE
*         delay = aprox 650usec
;
SPLKTIME: LD    E,14H           PRESET DELAY COUNTER
;
SPLKTM1:  DEC   E
          JR    Z,STMDEAD
;
          LD    A,(COMMAND)
          BIT   GO,A            GO COMMAND?
          JP    Z,GOINT         YES!
          AND   024H            NOITEST  RDY, IBG
          JP    NZ,PREIDLE
;
SPOS4
          LD    A,(IY+POSTN) has position changed
          CP    (IY+POSTN)
          JR    NZ,SPOS4
          CP    L
          NOP
          NOP
          NOP
*         JP    NZ,SPLK1H
;
          JR    SPLKTM1         LOOP UNTILL PULSE IS TIMMED OUT
*
*         set 100 usec dead time between current pulses
*             to give motor time to move and not over-correct
STMDEAD:
          LD    A,H
          LD    (MOTOR),A
          LD    E,80H
XDELAY:   DEC   E
          JR    NZ,XDELAY
```

```
1087  0434  C3 74 03              JP    STOPLCK
1088                          *
1089                          ;
1090                          ***************************************************
1091                          *                                                 *
1092                          *                  REVERSE START                  *
1093                          *                                                 *
1094                          ***************************************************
1095                          ;
1096                          ;
1097                          *******   RAMP CURRENT DOWN
1098  0437  78                ACC125T:  LD    A,E           RAMP CURRENT DOWN
1099  0438  C6 04                     ADD   A,4
1100  043A  5F                        LD    E,A
1101  043B  32 04 10                  LD    (MOTOR),A
1102  043E  00                        NOP
1103  043F  00                        NOP
1104  0440  FE 14                     CP    20
1105  0442  38 F3                     JR    C,ACC125T
1106                          !
1107                          ;
1108                          *******   INITIALIZE REGISTER BANK 1 REGISTERS
1109                          !
1110  0444  79                ST125R:   LD    A,C           SET FORWARD TRIM
1111  0445  D9                        EXX                 1;
1112  0446  4F                        LD    C,A           1;
1113                          !
1114  0447  D9                        EXX                 0;
1115  0448  7B                        LD    A,E           0;
1116  0449  D9                        EXX                 1;
1117  044A  C6 0A                     ADD   A,10          1;
1118  044C  32 04 10                  LD    (MOTOR),A     1;
1119  044F  5F                        LD    E,A           1;
1120                          ;
1121  0450  16 07                     LD    D,.HIGH.(TABLE1)  1;SET PAGE POINTER
1122  0452  21 01 10                  LD    HL,VELMSB     1;INITIALIZE I/O POINTER TO VELOCITY INPUT
1123  0455  DD 21 66 04               LD    IX,ST125R1    1;
1124  0459  3A 02 10                  LD    A,(VELOCITY)  1;
1125  045C  FB                        EI                  1;
1126  045D  7B                ST125RZ:  LD    A,E           1;
1127  045E  C6 02                     ADD   A,2           1;
1128  0460  32 04 10                  LD    (MOTOR),A     1;
1129  0463  5F                        LD    E,A           1;
1130  0464  18 F7                     JR    ST125RZ       1;
1131  0466
1132                          ********  USE LOOK-UP TABLES TO ACCELERATE TO 115 IPS
1133                          ;
1134  0468  7E                ST125R1:  LD    A,(HL)        1;LOAD VELOCITY COUNT MSB
1135  0467  E6 0F                     AND   MASK          1;
1136  0469  FE 00                     CP    0             1;VELOCITY > 96 IPS?
1137  0468  CA 7E 04                  JP    Z,ST125R2     1;
1138  046E  31 00 40                  LD    SP,SSTACK      1;
1139  0471  3A 02 10                  LD    A,(VELOCITY)  1;
1140  0474  3A 05 10                  LD    A,(COMMAND)   1;
1141  0477  CB 7F                     BIT   GO,A          1;
```

```
1142  0479  C2 5E 02                JP    NZ,EXITGOR   1;
1143  047C  FB                       EI                 1;
1144  047D  76                       HALT               1;
1145                                 ;
1146                                 ;
1147  047E  2C                ST125R2: INC   L
1148  047F  7E                       LD    A,(HL)       1; LOAD VELOCITY COUNT
1149  0480  2F                       CPL                1;COMPLEMENT SPEED COUNT
1150  0481  23                       INC   HL           1;
1151  0482  77                       LD    (HL),A       1;OUTPUT VELOCITY COUNT TO SEQUENCER
1152  0483  2F                       CPL                1;
1153  0484  FE CD                    CP    205          1;       IF END OF LOOK-UP TABLE
1154  0486  DA A0 04                 JP    C,ST125R3    1;
1155  0489  CB 3F                    SRL   A            1;DIVIDE BY 2
1156  048B  5F                       LD    E,A          1;SET UP LOOK-UP TABLE ADDRESS
1157  048C  1A                       LD    A,(DE)       1;
1158  048D  ED 44                    NEG                1;
1159  048F  81                       ADD   A,C          1;
1160  0490  2C                       INC   L            1;
1161  0491  77                       LD    (HL),A       1;OUTPUT CURRENT TO MOTOR
1162                                 ;                  1;
1163  0492  2C                       INC   L            1;INPUT COMMAND
1164  0493  7E                       LD    A,(HL)       1;
1165  0494  CB 7F                    BIT   GO,A         1;GO COMMAND?
1166  0496  C2 5E 02                 JP    NZ,EXITGOR   1;NO!
1167  0499  31 00 40                 LD    SP,SSTACK     1;
1168  049C  2E 01                    LD    L,1          1;
1169  049E  FB                       EI                 1;
1170  049F  76                       HALT               1;
1171                                 ;                  1;
1172  04A0  16 80              ST125R3: LD    D,INTEGR     1;INITIALIZE INTEGRATOR
1173  04A2  06 14                    LD    B,20         1;
1174  04A4  2E 02                    LD    L,2          1;
1175  04A6  DD 21 AC 04              LD    IX,RUN125R   1;SET FORWARD MOTION ROUTINE
1176  04AA  FB                       EI                 1;
1177  04AB  76                       HALT               1;
1179  04AC
1180
1181                                 ********************************************************
1182                                 *                                                      *
1183                                 *                  RUN 125 IPS REVERSE                 *
1184                                 *                                                      *
1185                                 ********************************************************
1186  04AC  7E                       ;
1187  04AD  FE 9B              RUN125R: LD    A,(HL)       1;LOAD VELOCITY COUNT / CLEAR INTERRUPT FLI
1188  04AF  DA 48 02                 CP    155          1;
1189  04B2  2F                       JP    C,ERROR      1;
1190  04B3  2C                       CPL                1;COMPLEMENT SPEED COUNT
1191  04B4  77                       INC   L            1;
1192  04B5  2F                       LD    (HL),A       1;OUTPUT VELOCITY COUNT TO SEQUENCER
1193  04B6  5F                       CPL                1;
1194  04B7  D6 BF                    LD    E,A          1;
1195  04B9  ED 44                    SUB   191          1;
1196  04BB  81                       NEG                1;
1197  04BC  2C                       ADD   A,C          1;ADD TRIM
                                     INC   L            1;
```

```
1198  048D  77                  LD    (HL),A       1;'OUTPUT ACCELERATE COMMAND
1199  048E
1200  048E
1201  048E
1202                     ******** TEST COMMANDS (EVERY TACH LINE)
1203                     ;
1204  048E  2C                  INC   L
1205  048F  7E                  LD    A,(HL)       1;LOAD COMMAND BITS
1206  04C0  EE 50               XOR   050H        1;TEST FOR FORWARD AND REWIND COMMANDS
1207  04C2  E6 C0               AND   0C0H         1;TEST FOR STOP COMMAND        (NO REWIND)
1208  04C4  20 45               JR    NZ,EXIT125R  1;
1209                     ;
1210  04C6  31 00 40            LD    SP,SSTACK     1:       RESET SSTACK POINTER
1211  04C9  2E 02               LD    L,02         1;RESET I/O POINTER
1212  04CB
1213  04CB
1214                     ******** TRIM INTEGRATION ROUTINE
1215                     ;
1216  04CB  10 0E               DJNZ  RUN125RC     1;UPDATE TRIM INTEGRATOR EVERY 3RD TACH LIN
1217  04CD  06 03               LD    B,3          1; RESET DELAY COUNTER
1218  04CF  7B                  LD    A,E          1;TEST COUNT FOR ERROR
1219  04D0  D6 C4               SUB   196          1,
1220  04D2  38 25               JR    C,RUN125R2   1;NEGATIVE ERROR
1221  04D4  28 03               JR    Z,RUN125R0   1;ZERO ERROR
1222                     ;
1223  04D6  15                  DEC   D            1;INCREMENT INTEGRATOR  (CAPSTAN SLOW)
1224  04D7  28 13               JR    Z,RUN125R1   1;ADJUST TRIM IF COUNTER OVERFLOW
1225  04D9  FB                  EI
1226  04DA  76                  HALT
1227                     ;
1228  04DB  3A 07 10            LD    A,(REWIND)   1;TEST FOR REWIND OFFSET
1229  04DE  FE 00               CP    0
1230  04E0  28 F7               JR    Z,RUN125R0
1231  04E2  FE FF               CP    0FFH         1;ACCEPT 'FF' SAME AS '00'
1232  04E4  28 F3               JR    Z,RUN125R0   1;
1233                     ;                         1;
1234  04E6  DD 21 27 05         LD    IX,REWINDR   1;SET REWIND MODE
1235  04EA  FB                  EI                 1;
1236  04EB  76                  HALT               1;
1237                     ;                         1;
1238  04EC
1239  04EC  16 80               LD    D,INTEGR
1240  04EE  0D                  DEC   C            1;INCREMENT TRIM REGISTER
1241  04EF  16 80               LD    D,080H       1;RESET INTEGRATION REGISTER
1242  04F1  3E 3E               LD    A,NULL-20H   1;
1243  04F3  B9                  CP    C            1;
1244  04F4  38 01               JR    C,RUN125RA   1;TEST UPPER LIMIT OF TRIM
1245  04F6  4F                  LD    C,A          1;
1246  04F7  FB                  EI                 1;
1247  04F8  76                  HALT               1;
1248                     ;                         1;
1249  04F9  14                  INC   D            1;DECREMENT INTEGRATOR  (CAPSTAN FAST)
1250  04FA  28 02               JR    Z,RUN125R3   1;
1251  04FC  FB                  EI                 1':
```

RUN125R0: RUN125RC: RUN125R1: RUN125RA: RUN125R2:

53 54 55 60 65

```
1252  04FD  76                HALT
1253                  ;
1254  04FE              RUN125R3:
1255  04FE  16 80             LD    D,INTEGR
1256  0500  0C                INC   C               1:DECREMENT TRIM REGISTER       (TEST LIMIT
1257  0501  16 80             LD    D,080H          1; RESET INTEGRATION REGISTER
1258  0503  3E 7E             LD    A,NULL+20H      1;
1259  0505  B9                CP    C               1;
1260  0506  30 01             JR    NC,RUN125R4     1; TEST LOWER TRIM LIMIT
1261  0508  4F                LD    C,A             1;
1262  0509  FB          RUN125R4: EI                  1;
1263  050A  76                HALT                  1;
1264                  ;
1265                  ;
1266                  ******** EXIT RUN ROUTINE
1267                  ;
1268  050B  F3          EXIT125R: DI
1269  050C  79                LD    A,C             1; SAVE NEW FORWARD TRIM
1270  050D  D9                EXX                   0;
1271  050E  4F                LD    C,A             0;
1272                  ;                             0;
1273  050F  3E 02             LD    A,2             DISABLE NMI,RESET CAPSTAN PARKED
1274  0511  32 06 10          LD    (CONTROL),A
1275  0514  3A 05 10          LD    A,(COMMAND)
1276  0517  CB 5F             BIT   HP,A                test for HP card present
1277  0519  3E AC       REVSTOP:  LD    A,NULL+MAXSTP     SET MAXIMUM DECELERATE CURRENT
1278  051B  28 02             JR    Z,NOHP1
1279  051D  C6 0A             ADD   A,10                increase for HP card
1280  051F              NOHP1:
1281  051F  32 04 10           LD    (MOTOR),A
1282                  ;
1283  0522  16 01             LD    D,1             SET REVERSE STOP FLAG
1284  0524  C3 66 02          JP    STOP125
1286  0527
1287
1288
1289
1290
1291
1292
1293  0527
1294  0527
1295  0527
1296  0527  21 01 10    REWINDR:  LD    HL,VELMSB       INPUT VELOCITY MSB
1297  052A  7E                LD    A,(HL)          VERIFY
1298  052B  BE                CP    (HL)
1299  052C  20 F9             JR    NZ,REWINDR
1300  052E  E6 0F             AND   MASK            MASK SPEED SELECT BITS
1301  0530  28 07             JR    Z,REWIND2
1302  0532  3E 3E       REWIND1:  LD    A,NULL-20H      IF VELOCITY < 98 IPS MAINTAIN START CURRENT
1303  0534  32 04 10          LD    (MOTOR),A
1304  0537  18 EE             JR    REWINDR
1305                  ;
1306  0539  21 07 10    REWIND2:  LD    HL,REWIND       LOAD REWIND SPEED COMMAND
1307  053C  7E                LD    A,(HL)
```

```
1308  053D  BE                CP    (HL)            VERIFY STABLE INPUT
1309  053E  20 F9             JR    NZ,REWIND2
1310  0540  4F                LD    C,A
1311  0541  21 02 10          LD    HL,VELOCITY
1312  0544  7E          REWIND3: LD    A,(HL)          LOAD VELOCITY COUNT
1313  0545  BE                CP    (HL)
1314  0546  20 FC             JR    NZ,REWIND3      VERIFY
1315  0548  81                ADD   A,C             ADD REWIND OFFSET
1316  0549  38 E7             JR    C,REWIND1       MAINTAIN 1/4 MAX CURRENT IF TOO SLOW
1317  054B  D6 C4             SUB   196
1318  054D  ED 44             NEG                   COMPUTE MOTOR CURRENT
1319  054F  87                ADD   A,A
1320  0550  C6 5E             ADD   A,NULL
1321  0552  32 04 10          LD    (MOTOR),A
1322                          ;
1323  0555  3A 05 10          LD    A,(COMMAND)
1324  0558  CB 7F             BIT   GO,A            TEST FOR STOP COMMAND
1325  055A  20 04             JR    NZ,REWINDX
1326  055C  CB 77             BIT   FORWARD,A       TEST FOR FORWARD AND REWIND COMMANDS
1327  055E  20 C7             JR    NZ,REWINDR
1328  0560  D9          REWINDX: EXX                   0:    switch back to bank-0
1329  0561  AF                XOR   A                       set Z-flag
1330  0562  C3 19 05          JP    REVSTOP
1331                          ;
1332                          ;
1333                          ********  EXIT REWIND ROUTINE
1334  0565
1336                          ;*************************************************************
1337                          ;*************************************************************
1338                          ;*                                                           *
1339                          ;*                      SERVICE ROUTINES                     *
1340                          ;*          -- uses register bank-0 --                       *
1341                          ;*                                                           *
1342                          ;*************************************************************
1343                          ;*************************************************************
1344                          ;
1345                          ;-------------------------------------------------------------*
1346                          ; NULLSET:THIS ROUTINE WILL FIND AND STORE THE DIFFERENCE    *
1347                          ; BETWEN THE CONVERTER TRUE AND NOMINAL NULLS,AND WILL       *
1348                          ; BLINK THE TEST LED IF THE TRUE NULL CAN NOT BE             *
1349                          ; DETERMINED                                                 *
1350                          ; Bit's 3,4 of I-reg set to prevent interrupt MODE-1 vector *
1351                          ; from conflicting with memory I/O ports                     *
1352                          ;-------------------------------------------------------------*
1353                          ;
1354                          ******** FIND D/A NULL
1355                          ;
1356                          NULLSET:
1357  0565                          DI
1358  0565  F3                LD    A,0
1359  0566  3E 00             LD    (VELTEST),A
1360  0568  32 03 10          LD    (CONTROL),A     LED..on, NMI..disab, CAPSTAN park bit..rese
1361  0568  32 06 10          LD    HL,MOTOR
1362  056E  21 04 10          LD    (HL),NULL-8     set d/a to voltage diff then null
1363  0571  36 56
```

```
1364  0573  2C
1365  0574  CB 46
1366  0576  CA FA 05
1367  0579  3E 56
1368  057B  3C
1369  057C  FE 66
1370  057E  28 7A
1371  0580  2E 04
1372  0582  77
1373  0583  2C
1374  0584  00
1375  0585  00
1376  0586  CB 46
1377  0588  20 F1
1378  058A  3D
1379  058B  47
1380  058C  FE 5E
1381  058E  30 08
1382  0590  3E 5E
1383  0592  90
1384  0593  E6 07
1385  0595  F6 18
1386  0597  ED 47
1387  0599  18 08
1388
1389  059B  D6 5E
1390  059D  E6 07
1391  059F  F6 98
1392  05A1  ED 47
1393
1394  05A3  21 38 50
1395  05A6  11 02 00
1396  05A9  19
1397  05AA  30 FD
1398
1399  05AC  3E 02
1400  05AE  32 06 10
1401
1402  05B1  21 38 50
1403  05B4  11 01 00
1404  05B7  19
1405  05B8  30 FD
1406
1407
1408
1409
1410  05BA  3E 00
1411  05BC  32 06 10
1412
1413  05BF  3A 01 10
1414  05C2  E6 0F
1415  05C4  5F
1416
1417  05C5  3E 72
```

```
              INC   L
              BIT   POLARITY,(HL)
              JP    Z,LIGHTOFF      error..if not positive
              LD    A,NULL-8        SET MINIMUN ADJUST VALUE
INCNULL:      INC   A               real_null < 94
              CP    102             INC. VALUE EQUAL TO MAXIMUM VALUE?
              JR    Z,LIGHTOFF      ERROR exit
              LD    L,4             POINT TO MOTOR
              LD    (HL),A          NEW VALUE INTO MOTOR
              INC   L               POINT TO COMMAND REG
              NOP
              NOP
              BIT   POLARITY,(HL)
              JR    NZ,INCNULL
              DEC   A
              LD    B,A             set B= real_null
              CP    NULL
              JR    NC,NULLPOS      real_null >= nominal null
              LD    A,NULL
              SUB   B
              AND   7
              OR    18H             real_null <94 ,NULL POLARITY=0
              LD    I,A             INITIALIZE TRIM OFFSET REGISTER
              JR    LAMPTEST
;
NULLPOS:      SUB   NULL
              AND   7               ..only save 3-bits for null-offset
              OR    98H             real_null > 94 , NULL POLARITY=1
              LD    I,A             NULL OFFSET INTO I REG.
;
LAMPTEST:     LD    HL,-45000       DELAY 250 MSEC
              LD    DE,2
DELAY1:       ADD   HL,DE
              JR    NC,DELAY1
;
              LD    A,LEDNMIOF      TURN OFF TEST LED; NMI DISABLED;PARKED BIT
              LD    (CONTROL),A
;
              LD    HL,-45000
              LD    DE,1
DELAY2:       ADD   HL,DE
              JR    NC,DELAY2
;
;
********      WAIT FOR FIRST TACH LINE  (INITIALIZE VELOCITY COUNTER)
;
FIRSTTAC:     LD    A,0             DISABLE NMI,TURN LED ON RES CAPS,PARKED
              LD    (CONTROL),A
;
              LD    A,(VELMSB)
              AND   MASK
              LD    E,A
;
              LD    A,NULL+20       SET CURRENT TO OBTAIN FIRST TACH LINE
```

```
1418  05C7  32 04 10
1419
1420  05CA  3A 01 10
1421  05CD  E6 0F
1422  05CF  B8
1423  05D0  CA CA 05
1424
1425  05D3  78
1426  05D4  32 04 10
1427
1428  05D7  48
1429
1430  05D8  21 01 10
1431  05DB  7E
1432  05DC  E6 E0
1433  05DE  FE C0
1434  05E0  C2 FA 05
1435  05E3  3E 03
1436  05E5  32 06 10
1437
1438  05E8  DD 21 03 00
1439  05EC  31 00 40
1440  05EF  26 00
1441  05F1  D9
1442  05F2  26 80
1443  05F4  D9
1444  05F5  ED 56
1445  05F7  C3 4F 00
1446
1447
1448  05FA  3E 02
1449  05FC  32 06 10
1450  05FF  06 03
1451  0601  21 48 77
1452  0604  11 02 00
1453  0607  19
1454  0608  D2 07 08
1455  0608  10 F4
1456  060D  3E 00
1457  060F  32 06 10
1458  0612  06 03
1459  0614  21 48 77
1460  0617  11 01 00
1461  061A  19
1462  061B  D2 1A 06
1463  061E  10 F4
1464  0620  C3 03 00
1465  0623
1466
1468  0623
1469  0623
```

```
              LD    (MOTOR),A
;
FT1:          LD    A,(VELMSB)      WAIT FOR EPO RELAY TO CLOSE
              AND   MASK
              CP    E
              JP    Z,FT1
;
              LD    A,B             load (real_null) to motor
              LD    (MOTOR),A
*
                                       set forward and reverse RUN current's
              LD    C,B                reverse
;
              LD    HL,VELMSB       LOAD VELOCITY MSB INPUT
              LD    A,(HL)
              AND   0E0H            only look at speed select bits
              CP    0C0H            TEST 125IPS SELECT
              JP    NZ,LIGHTOFF     NO wrong speed setting...>>> ABORT <<<
              LD    A,NOLEDNMI      ENABLE NMI,TURN LED OFF,RES.CAPS.PARKED
              LD    (CONTROL),A
*
              LD    IX,START        0; interrupts not enabeled yet..but just in
              LD    SP,SSTACK        0; defalt value
              LD    H,00            0; SET BIT 7 LOW  (REGISTER BANK 0)
              EXX                   1; SELECT REGISTER BANK 1
              LD    H,80H           1; SET BIT 7 HIGH (REGISTER BANK 1)
              EXX                   0; SELECT REGISTER BANK 0
              IM 1                   0; SELECT INTERRUPT MODE 1
              JP    IDLE            0;
;
;
LIGHTOFF:     LD    A,LEDNMIOF      DISABLE NMI,TURN LED OFF RES.CAPS.PARKED
              LD    (CONTROL),A
              LD    B,3             275 MSEC DELAY
OFFDLY:       LD    HL,-35000
              LD    DE,2
OFFDLY1:      ADD   HL,DE
              JP    NC,OFFDLY1
              DJNZ  OFFDLY
              LD    A,0             TURN LED ON,DISABLE NMI,RES.CAPS.PARKED
              LD    (CONTROL),A
              LD    B,3             775 MSEC. DELAY
ONDLY:        LD    HL,-35000
              LD    DE,1
ONDLY1:       ADD   HL,DE
              JP    NC,ONDLY1
              DJNZ  ONDLY
              JP    START
```

```
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482   0760   00
1483   0761   02
1484   0762   03
1485   0763   05
1486   0764   06
1487   0765   08
1488   0766   09
1489   0767   0B
1490   0768   0C
1491   0769   0E
1492   076A   0F
1493   076B   11
1494   076C   12
1495   076D   14
1496   076E   15
1497   076F   16
1498   0770   18
1499   0771   19
1500   0772   1B
1501   0773   1C
1502   0774   1E
1503   0775   1F
1504   0776   21
1505   0777   22
1506   0778   24
1507   0779   25
1508   077A   27
1509   077B   28
1510   077C   2A
1511   077D   2B
1512   077E   2D
1513   077F   2E
1514   0780   2F
1515   0781
1516   0781
1517   0781
1518
1519
1520
1521
1522   0781   30
1523   0782   33
```

```
;*****************************************************************
;*                                                               *
;*                        LOOK-UP TABLES                         *
;*                                                               *
;*****************************************************************
;
;
********  VELOCITY CONTROLLED RAMP
          ORG   760H          FOR COUNT OF 192:  OFFSET = 192/2 = 96 = X'
;
;                                 VELOCITY      VELOCITY
;              CURRENT             COUNT          (IPS)
TABLE1    DB      0                 192
          DB      2                 194
          DB      3                 196
          DB      5                 198
          DB      6                 200
          DB      8                 202
          DB      9                 204
          DB     11                 206
          DB     12                 208
          DB     14                 210
          DB     15                 212
          DB     17                 214
          DB     18                 216
          DB     20                 218
          DB     21                 220
          DB     22                 222
          DB     24                 224
          DB     25                 226
          DB     27                 228
          DB     28                 230
          DB     30                 232
          DB     31                 234
          DB     33                 236
          DB     34                 238
          DB     36                 240
          DB     37                 242
          DB     39                 244
          DB     40                 246
          DB     42                 248
          DB     43                 250
          DB     45                 252
          DB     46                 254
          DB     47                 256


********  VELOCITY CONTROLLED RAMP  -- COUNT > 256
;
;                                 VELOCITY      VELOCITY
;              CURRENT             COUNT          (IPS)
TABLE3    DB     48                 100H
          DB     51                 108
```

```
1524  0783  36
1525  0784  39
1526  0785  3C
1527  0786  3F
1528  0787  42
1529  0788  45
1530  0789  48
1531  078A  4B
1532  078B  4E
1533  078C  51
1534  078D  51
1535  078E  51
1536  078F  51
1537  0790  51
1538  0791  51
1539  0792  51
1540  0793  51
1541  0794  51
1542  0795  51
1543  0796  51
1544  0797  52
1545  0798  52
1546  0799  52
1547  079A  52
1548  079B  52
1549  079C  52
1550  079D  52
1551  079E  52
1552  079F  52
1553  07A0  52
1554  07A1
1555
1556
1557
1558
1559
1560  07A1  00
1561  07A2  00
1562  07A3  00
1563  07A4  00
1564  07A5  00
1565  07A6  00
1566  07A7  00
1567  07A8  28
1568  07A9  2C
1569  07AA  30
1570  07AB  34
1571  07AC  38
1572  07AD  3C
1573  07AE  40
1574  07AF  44
1575  07B0  48
1576  07B1  4E
1577  07B2  52
```

```
      DB    54          110
      DB    57          118
      DB    60          120
      DB    63          128
      DB    66          130
      DB    69          138
      DB    72          140
      DB    75          148
      DB    78          150
      DB    81          158
      DB    81          160
      DB    81          168
      DB    81          170
      DB    81          178
      DB    81          180
      DB    81          188
      DB    81          190
      DB    81          198
      DB    81          1A0
      DB    81          1A8
      DB    82          1B0
      DB    82          1B8
      DB    82          1C0
      DB    82          1C8
      DB    82          1D0
      DB    82          1D8
      DB    82          1E0
      DB    82          1E8
      DB    82          1F0
      DB    82          1F8

*******  ACCELERATION CURRENT FOR SHORT GO-DOWN
;
;
;                 CURRENT      VELOCITY      VELOCITY
;                MAX = 85      COUNT/32       (IPS)
TABLE2  DB          0             0            -
        DB          0             1           768
        DB          0             2           368
        DB          0             3           256
        DB          0             4           189
        DB          0             5           153
        DB          0             6           127
        DB         40             7           110
        DB         44             8            96
        DB         48             9            85
        DB         52            10            77
        DB         56            11            70
        DB         60            12            64
        DB         64            13            59
        DB         68            14            55
        DB         72            15            51
        DB         78            16            48
        DB         82            17            45
```

```
1578  0783  52
1579  0784  52
1580  0785
1581  0785
1582  0785
1583
1584
1585
1586
1587  0785  10
1588  0786  0F
1589  0787  0E
1590  0788  0D
1591  0789  0C
1592  078A  0B
1593  078B  0A
1594  078C  09
1595  078D  08
1596  078E  07
1597  078F  06
1598  07C0  05
1599  07C1  04
1600  07C2  03
1601  07C3  03
1602  07C4  03
1603  07C5
1604
1605
1606
1607
1608
1609
1610
1611  07C5  00 00 08 08
1612  07C9  08 08 08 0A
1613  07CD  0A 0C 0C 0E
1614  07D1  0E 10 10 10
1615  07D5  12 12 12 14
1616  07D9  14 14 16 16
1617
1618  07DD
1619
1620  07E0
1621  07E0  43 41 50 31
1622  07E4  32 35 20 20
1623  07E8  56
1624  07E9  65 72
1625  07EB  20 41 30 32
1626  07EF  20
1627  07F0  31 32 2D 4A
1628  07F4  55 4E 38 31
1629  07F8
1630  07F8
```

```
        DB      82              18              43
        DB      82              19              40


********** STOP PULSE CURRENT TABLE **********
;
;                                       VELOCITY    VELOCITY
;               CURRENT                 COUNT/128     (IPS)
PULSETBL  DB      16                      0             -
          DB      15                      1           189
          DB      14                      2            96
          DB      13                      3            64
          DB      12                      4            48
          DB      11                      5            39
          DB      10                      6            32
          DB       9                      7            28
          DB       8                      8            24
          DB       7                      9            22
          DB       6                     10            19
          DB       5                     11            18
          DB       4                     12            18
          DB       3                     13            15
          DB       3                     14            14
          DB       3                     15            13

*************************************************************
*                                                           *
*                       STOPLOCK TABLE                      *
*                                                           *
*************************************************************
;
;
STLCKTBL: DB    0,0,8,8,8,8,8,10

          DB    10,12,12,14,14,16,16,16

          DB    18,18,18,20,20,20,22,22
;

          ORG   7E0H
VERSION:
          DB    'CAP125  '

     DB     'V'
     DB     65H,72H ;"ER"
     DB     ' A02 '

          DB    '12-JUN81'


          END
```

CROSS REFERENCE

LABEL	VALUE	REFERENCE							
A0	0000	-241							
A30	0030	-267							
ACC125	00F3	340	420	-434					
ACC125A	0100	-442	445						
ACC125B	0118	446	-461						
ACC125C	0124	461	-467						
ACC125D	0140	475	-479	484					
ACC125E	0142	470	-482						
ACC125F	014D	-487	488						
ACC125G	0151	486	-491						
ACC125H	015E	-498	505						
ACC125J	016D	472	-509						
ACC125N	00FC	-439							
ACC125R	010A	436	-450						
ACC125S	0110	-454	457						
ACC125T	0437	494	-1098	1105					
ACCHIS	0154	-493							
BANK	0007	-208	325	928					
CMD	0005	-98	361	740	789	836	882		
COMMAND	1005	-136	304	411	434	473	491	509	561
		682	921	1007	1045	1061	1140	1275	1323
CONT	0006	-99	835						
CONTROL	1006	-149	251	303	323	681	926	1274	1361
		1400	1411	1436	1449	1457			
CRTBUF	4200	-160							
DELAY1	05A9	-1396	1397						
DELAY2	05B7	-1404	1405						
ERROR	0248	615	-695	1188					
EXIT125F	022E	628	-674						
EXIT125R	0508	1208	-1268						
EXITGO	0263	724	-729						
EXITGOF	0257	563	586	-721					
EXITGOF1	0258	477	496	-722					
EXITGOR	025E	-726	1142	1166					
EXITGOR1	025F	478	-727						
FIRSTTAC	05BA	-1410							
FORWARD	0006	-144	362	419	435	476	493	510	882
		1008	1046	1326					
FT1	05CA	-1420	1423						
GO	0007	-145	305	474	495	582	585	740	789
		1062	1141	1165	1324				
GOINT	0068	308	-322	355	398	698	1063		
GOINT1	0071	326	-329						
GOINT2	0079	-334	338						
GOINT2A	0076	-333							
GOINT3	008A	-346	349						
GOINT5	00C9	343	-387	390					
GOINT6	00DE	370	-403						
HP	0003	-141	683	1276					
IBGCNTR	0002	-140	836						

65 60 55 50

IDLE	004F	-301	923	1445					
IDLE1	0054	-304	309						
INCNULL	0578	-1368	1377						
INTEGR	0080	-215	593	647	662	1172	1239	1255	
LAMPTEST	05A3	1387	-1394						
LEDNMIOF	0002	-209	322	1399	1448				
LIGHTOFF	05FA	1366	1370	1434	-1448				
MASK	000F	-207	337	353	394	468	543	697	766
		866	1135	1300	1414	1421			
MAX	0055	-206	338	363	1003	1005	1041	1043	
MAXSTP	004E	-205	684	722	727	1277			
MEMORY	0000	0							
MOTOR	1004	-131	299	376	443	455	501	524	535
		557	688	729	757	804	813	892	918
		953	1013	1051	1083	1101	1118	1128	1281
		1303	1321	1362	1418	1428			
MOTR	0004	-97	833						
NARG	0000	0							
NMIENBL	0000	-151							
NOHP	0244	685	-687						
NOHP1	051F	1278	-1280						
NOLEDNMI	0003	-210	835	1435					
NOSTOP	0084	367	-373						
NULL	005E	-203	294	297	363	438	441	450	453
		684	722	727	748	755	758	802	805
		811	814	833	891	914	917	1242	1258
		1277	1302	1320	1363	1367	1380	1382	1389
		1417							
NULLMIN	0056	-204							
NULLPOL	0007	-211	290	910					
NULLPOS	0598	1381	-1389						
NULLSET	0565	253	-1357						
OFFDLY	0601	-1451	1455						
OFFDLY1	0607	-1453	1454						
ONDLY	0614	-1459	1463						
ONDLY1	061A	-1461	1462						
PARKED	0002	-153							
PASTSTP1	03E8	1024	-1030						
PASTSTPH	03D8	975	-1019						
POLARITY	0000	-138	1365	1376					
POSITION	1000	-106	734	950					
POSTN	0000	-93	842	843	955	956	970	971	1068
		1069							
PREID	0048	291	-298						
PREIDL	004C	295	-298						
PREIDLE	003A	-289	837	1065					
PSTSTP1A	03E2	-1025							
PULSETBL	07B5	874	876	879	-1587				
PWRSAFE	0001	-139							
RAMP	02C5	790	-796						
RAMP0	02C9	753	-802						
RAMP00	02C8	749	-803	808					
RAMP1	02D8	744	797	-811					
RAMP11	02DA	-812	815						
RAMP2	028C	-756	759						

READY	0005	-143	307						
REVSTOP	0519	-1277	1330						
REW	0007	-100							
REWIND	1007	-157	1228	1308					
REWIND1	0532	-1302	1316						
REWIND2	0539	1301	-1306	1309					
REWIND3	0544	-1312	1314						
REWINDR	0527	1234	-1298	1299	1304	1327			
REWINDX	0560	1325	-1328						
RUN125F	01F1	598	-608						
RUN125F0	0211	637	-641						
RUN125F1	0213	640	-646						
RUN125F2	021E	636	-656						
RUN125F3	0223	657	-661						
RUN125F4	022C	666	-668						
RUN125FA	021C	651	-653						
RUN125R	04AC	1175	-1186						
RUN125R0	04D9	1221	-1225	1230	1232				
RUN125R1	04EC	1224	-1238						
RUN125R2	04F9	1220	-1249						
RUN125R3	04FE	1250	-1254						
RUN125R4	0509	1260	-1262						
RUN125RA	04F7	1244	-1246						
RUN125RC	04D8	1216	-1228						
RWND	0004	-142							
SEL125	0005	-114							
SEL50	0007	-116							
SEL75	0006	-115							
SHOWA	08BF	-163	263						
SHOWBC	0877	-162	259						
SHOWDE	0842	-161	256						
SPLK0A	0356	911	-916						
SPLK1H	0391	959	-969	972					
SPLK1H1	0381	985	-991						
SPLK1H1A	03AB	-986							
SPLK3H	0383	981	-994						
SPLK3H1A	03BB	-998							
SPLK4H	03C1	992	997	-1003					
SPLK5H	03C7	1004	-1008						
SPLK6H	03D2	1010	-1012						
SPLK7H	03EA	1021	-1033						
SPLK7H1A	03F0	-1036							
SPLK8H	03F6	1031	1035	-1041					
SPLK9H	03FC	1042	-1044						
SPLKAH	0407	1048	-1050						
SPLKTIME	0408	1014	-1056						
SPLKTM1	040D	-1058	1077						
SPOS2	037F	-954	957	985					
SPOS4	041D	-1067	1070						
SSTACK	4000	-214	462	559	588	628	1138	1187	1210
		1439							
ST125F	0175	506	-516						
ST125F1	0197	529	-542						
ST125F1A	0184	547	-558						

ST125F2	01C6	545	-568						
ST125F3	01E5	380	571	-593					
ST125FA	018E	-533	537						
ST125R	0444	364	511	-1110					
ST125R1	0466	1123	-1134						
ST125R2	047E	1137	-1147						
ST125R3	04A0	1154	-1172						
ST125RZ	045D	-1126	1130						
STACK	$ 0000	0							
START	0003	-250	359	899	1430	1464			
STLCKTBL	07C5	987	999	1028	1037	-1611			
STMDEAD	0428	1059	-1081						
STOP125	0266	691	-733	1284					
STOP125A	026C	-736	767						
STOP125B	0297	741	-762	765					
STOP125C	02AC	-779	781						
STOP125E	02BA	785	-788	794					
STOP125F	02E3	760	769	809	-832				
STOP125H	02F6	-841	844	854					
STOP125L	0309	-860	865						
STOP125M	032C	877	-881						
STOP125N	033C	884	-890						
STOP125P	0345	-895	896						
STOPDIR	0000	-213	743	798					
STOPDIST	007D	-212	958	973	982	994	1022	1033	
STOPLI	0314	-868	870						
STOPLCK	0374	-949	974	1087					
STOPLOCK	0348	308	847	850	-908				
STP1	0370	929	-933						
STPLOCK	035A	915	-918						
TABLE1	0760	1121	-1482						
TABLE2	07A1	378	406	409	-1560				
TABLE3	0781	527	553	-1522					
TESTLED	0001	-152							
VELINT	0038	-280							
VELMSB	1001	-112	333	352	393	467	698	1122	1298
		1413	1420	1430					
VELOCITY	1002	-120	346	381	387	463	482	530	560
		1124	1139	1311					
VELTEST	1003	-126	330	1360					
VERSION	07E0	-1620							
VLSB	0002	-95	737	779	780	868	869		
VMSB	0001	-94	763	764	863	864			
VSEQ	0003	-96	739	778					
XDELAY	0431	-1085	1086						

45 50 55 60 65

I claim:

1. A magnetic tape drive comprising:
first and second reels for the supply and take-up of tape;
a read/write head;
a capstan for moving said tape with respect to said read/write head;
a motor driving said capstan;
means for outputting feedback signals indicative of the actual velocity of the motor; and
means for control of said motor, said means for control of said motor comprising:
a microprocessor adapted to receive GO and STOP commands for control of said motor in addition to said feedback signals indicative of the actual velocity of said motor, and to generate responsive signals for control of said motor based on said feedback signals and said commands, said microprocessor examining its previous history upon receipt of a given GO or STOP command so as to determine which of a plurality of possible predetermined control signal sequences, each causing differing maximum rates of change of motor velocity shall be generated in response to said given GO or STOP command, whereby excitation of mechanical resonances in said system can be avoided.

2. The drive of claim 1 wherein said means for outputting feedback signals further comprises velocity and position decoder means for supplying said microprocessor with digital information relating to the position and velocity of said capstan at a given time.

3. The system of claim 2 wherein said digital output signals provided by said microprocessor are converted in digital-to-analog converter means to an analog signal used to control the motor driving said capstan.

4. The system of claim 1 wherein said microprocessor accesses read-only memory means for determination of proper output signal to be given upon receipt of given input commands.

5. In a magnetic tape drive of the type comprising a capstan and capstan motor for accelerating tape in the vicinity of a read/write head, and comprising microprocessor means for control of the motion of said capstan, the improvement which comprises:
said microprocessor comprising means for storing previously received commands and for examining the last previous command upon receipt of a newly input GO or STOP command, and for determining the maximal rate of change of motor current which will avoid excitation of mechanical resonance in said system, and to output one of a plurality of predetermined sequences of control signals to said motor in response to said means for determining.

6. The system of claim 5 wherein velocity profiles corresponding to said predetermined possible courses of action are stored in read-only memory and said microprocessor accesses said read-only memory upon receipt of said input commands.

7. A magnetic tape drive comprising:
spindle and motor means for receiving first and second reels of tape and for rotation of the same;
a capstan for controlling the motion of the tape between said reels;
a capstan motor;
a read/write head for reading and writing data to and from said tape; and
control means for controlling the capstan motor, said control means comprising:
means for responding to GO and STOP commands;
means for supplying current to said capstan motor for control thereof;
means for storing signals representative of the present status of the tape drive; and
microprocessor means for generating a sequence of control signals for controlling said means for supplying current in response to one of said GO or STOP commands and in response to the present status of said tape drive, such that differing sequences of control signals are generated by said microprocessor in response to identical GO or STOP commands in dependence on the present status of said tape drive, and such that the maximum current supplied to said motor varies responsive to said differing sequences.

8. The system of claim 7 wherein said sequences of control signals are stored and are selected by said microprocessor responsive to said signal representing the present status of the drive.

* * * * *