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EMMY/UNIBUS INTERFACE DESIGN SPECIFICATION

by

Mien Shih

January 1977

Technical Note No. 109

Digital Systems Laboratory
Departments of Electrical Engineering and Computer Science
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The work described herein was supported by the U.S. Energy Research and Development Administration under contract No. EY-76-S-03-0326-PA 39.

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ABSTRACT

The interface, named "MATCH" (a bus translation unit), is designed to allow communication between the Emmy system bus and a DEC PDP-11 Unibus. The translation unit consists of five functionally independent modules: an Emmy I/O interface unit, an address translation unit, two-ported data path, a microprogrammed translation sequencer and a Unibus I/O interface unit.

The Emmy I/O interface unit allows the Emmy system to act as bus master on the Unibus. The 32-bit Emmy bus address is truncated to 18-bit for use on the Unibus. The command field provides the control information for the transfer. The Unibus I/O interface unit allows the Unibus device to act as master on the Emmy bus. The 18-bit Unibus address is mapped into the 24-bit Emmy address sapce through the address translation unit where the command field is also generated. A mapping scheme is used which utilizes a page setup register file to dynamically associate one of fifty-four 2K halfword pages with a 1K fullword Emmy page. The microprogrammed sequencer receives commands from the master unit on either bus system and provides all the sequence control for the specified operation. Data path is designed into two parts, one is the halfword part for most of the transfers and the other, fullword part, is used mainly for transfer to/from the control store and other high speed devices.

The address translation facility provides mapping of pages in the Unibus address space other than the base pages (occupied by 4K core memory) and the upper pages which by convention are reserved for use as device registers. The entire address space of each bus system is available to the other system.

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1.0 INTRODUCTION

The "MATCH" provides a means of communication between the 32-bit Emmy bus system and 16-bit DEC Unibus system. Facilities are provided whereby either system may act as master on the other bus, and both systems have interrupt capability. The entire address space of each system is also available to the other system.

Status of each system is available to the other system through "MATCH". The Emmy may interrogate directly any CPU or device register on the Unibus system. The DEC PDP-11 provides all status information directly on the bus, and the DEC PDP-11 may access Emmy status by reading the micro status register (file register 0) via the address translation unit or by reading the status register on the Unibus, which returns the Emmy status information available on the direct status lines (such as RUN/HALT, power, timeout, etc.). MATCH has four 16-bit internal registers, namely, the Translation Status Register (TSR, which indicates bus status on both systems, current status of the translation unit, error information, etc.). The DBRn (Data Buffer Registers where DBR1 and DBR2 together provide the one fullword buffer for the fullword part of the data path. DBR3 is utilized as the halfword buffer for the other halfword part). All sixty-four page setup registers, together with the above four registers, are accessible to both bus systems via the address translation unit, where a unique address for each register is defined.

Fig. 1-1 illustrates the basic structure of the Emulation Lab facility. In this planned structure the PDP-11 will be used as an I/O processor for the more powerful Emmy system. The idea behind the design of this I/O system is to expand the system I/O capability by taking advantage of the currently available PDP-11 peripheral devices.

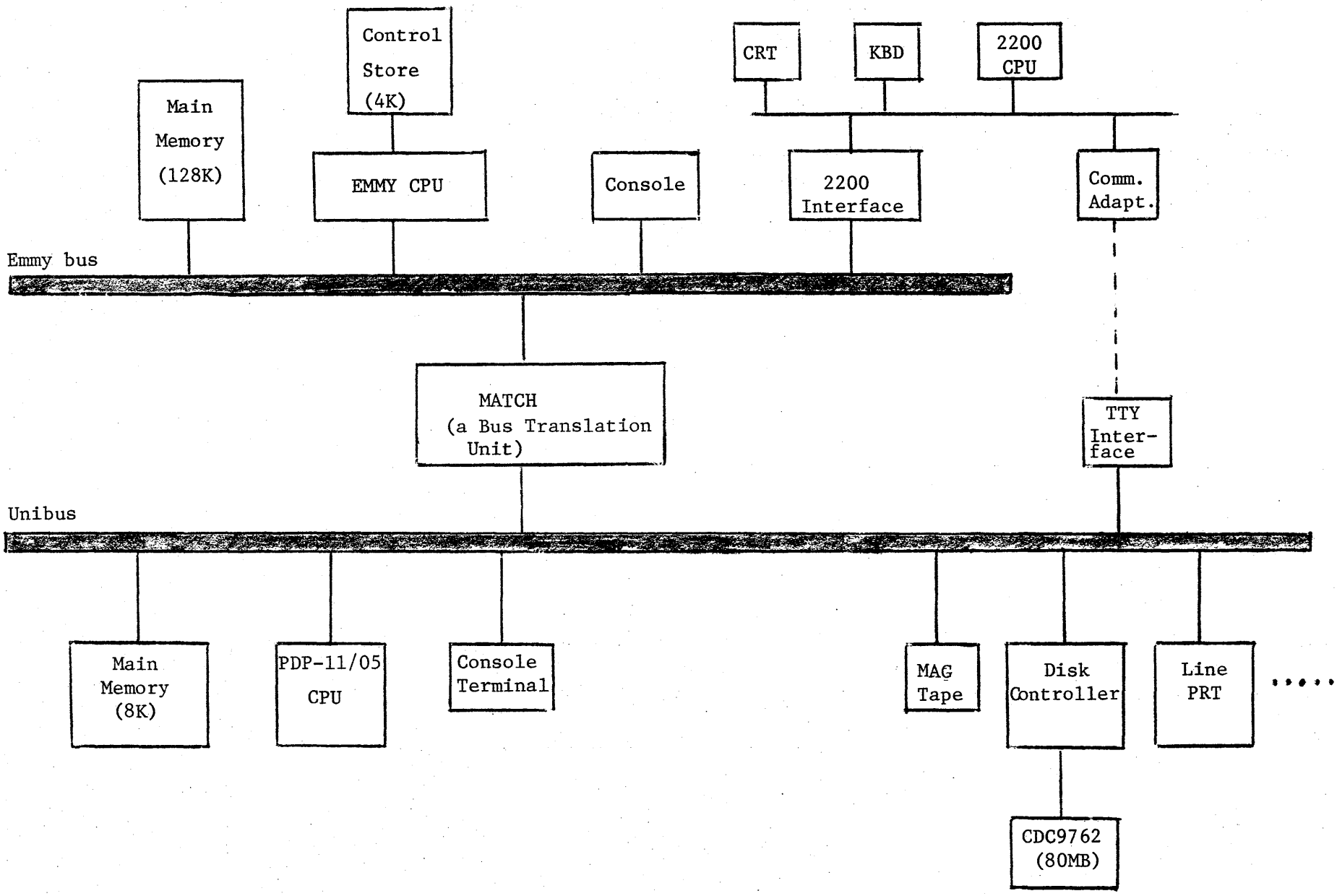


Fig. 1-1: STRUCTURE OF EMULATION LAB FACILITY

2.0 FUNCTIONAL DESCRIPTIONS

2.0.1 Design Overview

"MATCH" consists of five functionally independent modules:

(1) An Emmy I/O interface module which provides the actual handshaking capability for "MATCH" to communicate to the Emmy system and thus allows the Emmy system to act as bus master on the Unibus.

(2) an address translation module which includes the selection logic for both the bus system address and a memory management unit for page mapping and address translation.

(3) Two-ported data path which consists of one halfword (16-bit) channel and one fullword (32-bit) channel, each with its own associated memory address register. The two ports operate independently of each other, nevertheless they are both controlled by the sequencer.

(4) The microprogrammed translation sequencer is the heart and, thus, the most critical, and complicated part of this design. It senses the control/status information from the other four modules and takes the appropriate action. The microstore on the microprogram sequencer (AM 2909) allows immediate action to be taken for bus operations.

(5) The Unibus I/O interface module takes care of the handshaking operation of the Unibus.

The "MATCH" has a heart pulse rate of 10MHB. Since most of the logic is implemented in low-power schottky, the fan currently installed in the system box would be enough to keep "MATCH" happy. Fig. 2-1 illustrates how the five functional modules are interconnected.

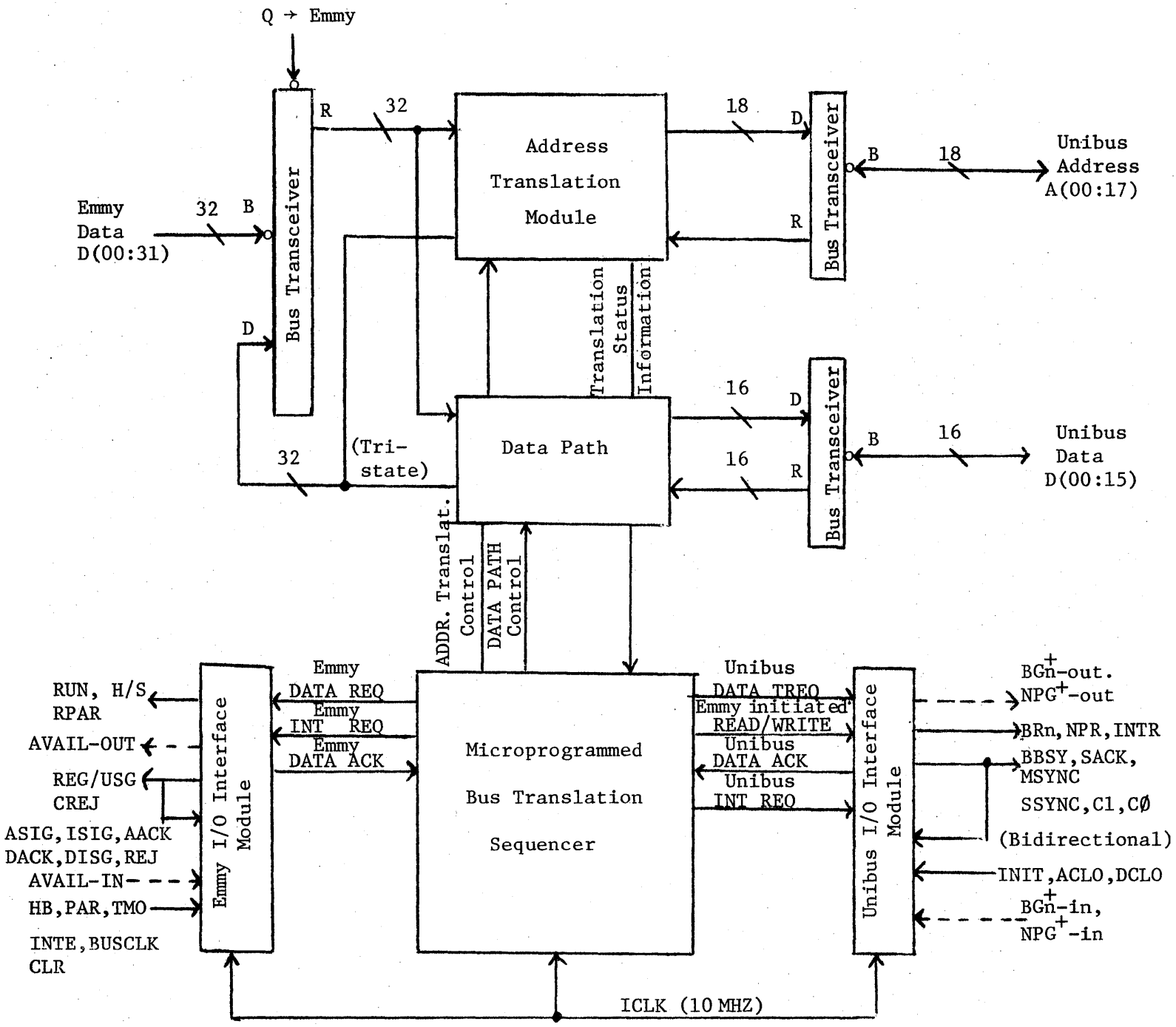


Fig. 2-1: "MATCH" (a bus translation unit) Functional Block Diagram

2.1 The Address Translation Module (ATM)

The address translation module basically handles two tasks: device selection and address translation, if selected. Upon receiving the address from either bus systems, ATM decodes the address and informs the translation sequencer about (1) unit selection, (2) part to be used for the transfer, (3) type of operation (Read, Write or interrupt request), (4) data type (4 byte, 2 byte or 1 byte data), (5) internal register selection. If it is a data Read/write request, then the received address is translated and gated onto the other system bus.

2.1.1 Emmy Initiated Operation

A master on the Emmy bus requests service of the MATCH by specifying an address with its unit address to be FC_{16} (i.e. A(23:16) = 11111100). The lower 16 bits of the Emmy address (its internal address portion) are used as the 16-bit Unibus address. (Since PDP-11/05 does not have a memory management unit, 16-bit address is sufficient for the entire unibut available address space.) In case A(23:16) $\neq FC_{16}$, ATM will just ignore the request and take no action at all.

The command field (bit 24-31) of Emmy address word is interpreted as follows:

31	30						24
L2	L1	1	1	0	0	I	R

R - 1 = Write, 0 = Read
This bit corresponds to C1 control line of the Unibus

I - Indicates an interrupt is to be issued to the PDP-11 if Unibus interrupt is enabled.

L2 L1 - Data length specification

1 1	- Single byte;	for write operation, CØ = 1. For read operation the whole word is gated onto the Emmy bus and it is up to the Emmy master unit to strobe in the low or high byte of the 16-bit data. Halfword port is used for this transfer.
1 0	- 2 byte;	A(00:00) is set to zero, i.e. transfer is only allowed on the halfword boundary. Violation of this rule will set an error bit in the TSR and the transfer proceeds.
0 1	- 3 byte;	not allowed. An address error bit of TSR will be set.
0 0	- 4 byte;	for write operation, the low word is set with A(00:01) = 00 and high word with A(00:01) = 10 for the transfer. The received Emmy bus address should have D(00:01) = 00 since only a byte address is used for communication with "MATCH" violation would set the address error flag. For read operation, MATCH keeps Unibus mastership for two consecutive cycles (by not asserting SACK for the first cycle and keeping BBSY asserted till the end of the second cycle, this will keep the other devices from getting the bus), in order to form a fullword to be transferred to Emmy. Fullword Port is used for this operation.
address spec. = 1 1		i.e. MATCH takes every address received as a byte address. When any other type of address is received, it will still be recognized as byte address while the address error flag is set for future examination and the operation proceeds.
alignment = 0		data is always right-justified
Fill = 0		data is always zero filled violation would set the error flag but the operation will proceed.

Once selected, the command signals from the decoder are latched and sent to the translation sequencer. The port requested for the transfer is checked for its availability at that moment. If the port is available then the lower 16-bits of the address word are latched into the corresponding memory address register (MARX) and a transfer sequence is initiated.

In case the Emmy address D(00:15) = 1674XX then an internal register is selected. A register read/write operation is initiated in the translation sequencer, and the contents of the addressed register is gated onto/loaded from the bus data lines without issuing a data request to the other bus inteface module.

2.1.2 Unibus Initiated Operations

Since the unibus provides only 18 bits of address space, a page table is provided to translate Unibus references to Emmy references. The Unibus address space is partitioned into three regions: the upper 4K halfword is reserved by DEC convention for device and processor registers. (The PDP-11/05 does not have a DEC memory management unit, thus if A(13:15) = 111, then A(16:17) is taken as 11, i.e. A(13:14) = XX111 represents the same 4K halfword pages as A(13:17) = 11111). The lower 4K halfword is occupied by core memory supplied with the PDP-11/05 processor. The rest of the address space is available for mapping into the Emmy address space.

To have this separation built into the hardware guarantees no disastrous overlapping, i.e. no Unibus address would have more than one physical location correspond to it. A command field generator is designed according to the following consideration.

A(12:17)

	17	16	15	14	13	12	assignment	action
(1)	0	0	0	0	0	X	DEC core memory (lower 4K halfword)	not selected
(2)	X	X	1	1	1	X	Upper 4K hw reserved for device Reg. for the lack of a DEC MMU, this area covers actually a total of 16K hw area	Device register selection check is initiated
(3)	0	0	1	0	X	X	This area is reserved for full 32-bit word transfer (4Kfw)	need further test for selection
(4)	Other memory area						available for access	" "

In (3) and (4), the page table is accessed and the content of the corresponding page set-up register is retrieved. If bit 15 = 1 (i.e. VALID), then the unit is selected, a bus data request sequence is initiated immediately and SACK (selection ACK) is asserted by MATCH on the Unibus, in (3) MAR and MARH (Memory Addr Holding Reg.) are compared. If it's recognized as consecutive transfer, then the other hw is gated onto the data lines without requesting data from the Emmy busy system during a read-out-of-Emmy operation. For write-into-Emmy operation, the address is also checked for readiness to initiate the transfer on the Emmy system. It is recommended that the Unibus master should maintain the bus mastership until a full 4 byte word is transferred.

For command field generation, the following convention is taken.

L2	L1	1	1	0	0	*	R

length spec : 11 = byte operation indicated by C0 = 1, available only for halfword port.

10 = hw operation indicated by C0 = 0, available only for halfword port. A(00:00)=0, otherwise, error flaged but operation proceeds with A(00:00) forced to be zero.

01 = 3 byte operation, considered as probably undesirable!

		00 = 4 byte operation; A(00:01)=00, available only for fw port.
address spec	:	again, only byte address is used for communicating with MATCH
Alignment	:	for fw, right-adjusted is always assumed.
Fill	:	and zero filled
*	:	even: reveal mediocrity and longing for companion. odd: unnecessarily expresses the strong inclination for address. (P.S. all my favorite numbers are odd, e.g. 7, 9, etc)
R	:	1 = Read, 0 = Write as indicated by C1

The command field generator is also responsible for device selection. It provides the following indications: (1) unit selected by Unibus, (2) fw/hw port is selected, (3) internal register selected (special action follows).

A 64 x 16 page set-up register file is installed to dynamically map one of sixty-four 2K halfword pages (some are inhibited as described above) with a 1K fullword Emmy page. The Unibus address A(12:17) is used to address the corresponding page set-up register, the lower 12 bits of the register contents are concatenated to the A(00:11) from Unibus address word to form a 24-bit Emmy address. Together with the command field generated, all 32-bits are sent onto data lines with ASIG asserted.

The MSB of a page set-up register is dedicated for selection indication, i.e. this bit is AND-ed with the unit selected line from the command field generator and the resulting TRANS REG is sent to the sequencer where the Data Reg sequence will be initiated.

When MATCH is in the "BUSY" state, requests from Unibus must wait until it is ready to be served. There, is unfortunately, no "REJECT" mechanism.

It is mandatory for the programmer to execute an initialization sequence before he may attempt any data transfer thru MATCH after power-on sequence or power-out interruption. This is because MATCH may be trapped in any arbitrary state, especially the page register file, (since there is no master CLR for the RAM we use) which may contain a random data pattern. The sequence should at least include: (1) dump the whole page register file or reload them all, (2) send a programmed master clear to initialize internal flags to the proper state.

Possibly a micro routine may do this job for the programmer internally. (We're introducing a fancy idea!) In case of power interruption ACLO/DCLO is asserted on the Unibus side. Unfortunately, Emmy gives no pre-warning and it is the Emmy chassis that most of the MATCH logic will reside in), the current contents of the page set-up table may be lost, so it would be a good idea for the programmer to keep a copy of the current table in the core . Nevertheless, a micro routine can be implemented to save the table contents upon receiving ACLO/DCLO.

When any Unibus device sends a INTR to its CPU, the PDP-11 processor acknowledges it and transfers control to its service routine where certain registers contain information on the destination of this interrupt process. In case of disk I/O upon completion, INTR is asserted by the disk controller. A unique bit may be assigned in the control register (CNR) to indicate the interrupt should be directed to Emmy. PDP-11 CPU loads bit Ø of TSR (Transfer Status Register) to indicate an interrupt request to Emmy. If INT EN is also set by the Emmy processor, then an Emmy INTR cycle is initiated. INT vector is assigned to be 04E-04F.

Figure 2-2 illustrates the structure of the address translation module.

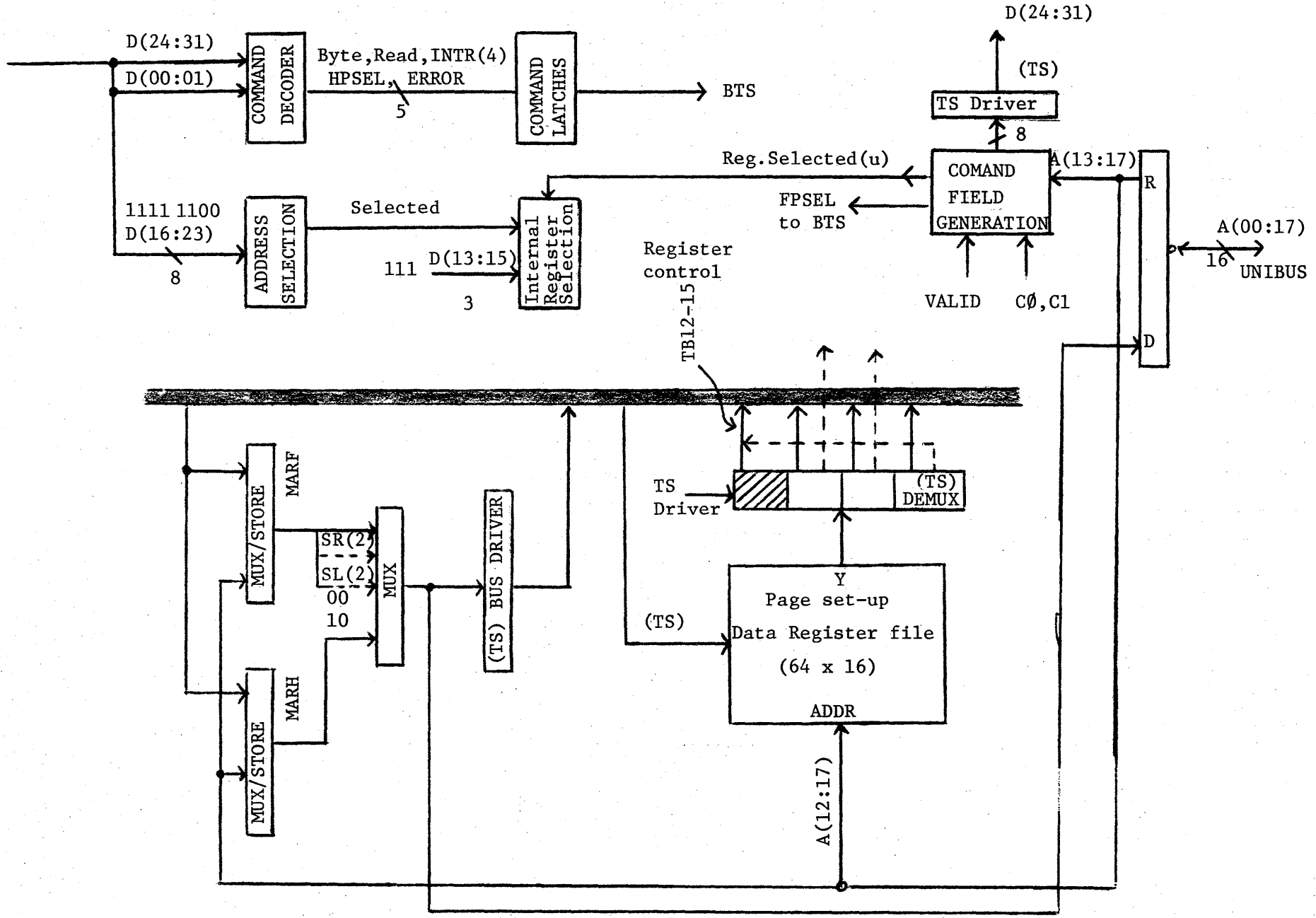


Fig. 2-2: Address Translation Module

There are seven internal registers which are accessible to both bus systems. Namely, they are:

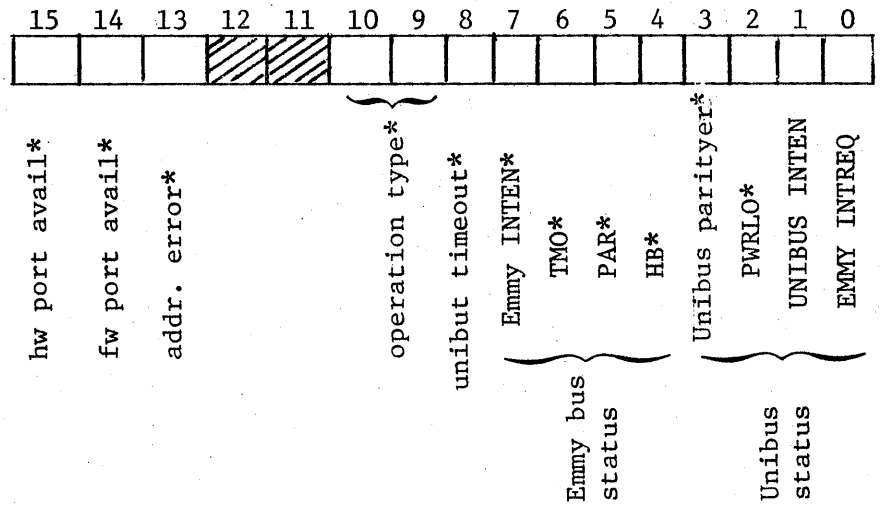
(1) TSR (Translation Status Register)

Emmy bus address 1111 1100 1111 1101 1110 0000 = $FCFDE\emptyset_{16}$

= 777176740_8

Unibus address 1111 1101 1110 0000 = $FDE\emptyset_{16}$

= 176740_8



bit 15 - hw port avail

indicates the current status of the half-word communication channel of MATCH. This bit is checked internally by the sequencer whenever the channel is requested for transfer service. It is read-only for both systems.

bit 14 - fw port avail. For all full-word port, otherwise same as hw port avail.

bit 13 - address error

as described previously, for address from both bus systems. Read-only for both systems. No interrupt of any kind is generated.

bit 10-9 - operation type

indicates the current (or last if MATCH in idle state) operation carried

out by MATCH.

11 = Emmy initiated write

10 = " " read

01 = Unibus " write

00 = " " read

read only by both systems

bit 8 - Unibut time-out

indicates transfer is attempted to/form an inactive unibus location. A microlevel interrupt request is issued to the sequencer. If enabled, an Emmy CPU interrupt request would be generated. Read-only for both systems

bit 7 - Emmy INTEN

write/read - able by Emmy CPU. Read-only for Unibus device.

bit 6 - TMO
bit 5 - PAR } Emmy bus status
bit 4 - HB

bit 3 - Unibus parity error

generated from PA, PB on Unibus

bit 2 - PWRLO (= ACLO V DCLO)

bit 1 - Unibus INTEN

write/read-able by Unibus device but Read-only for Emmy

bit 0 - Emmy INTREQ

write/read-able by Emmy. Read-only for Unibus

bit 12-11 Spare

DBR1 Emmy addr = $FCFDE2_{16}$, Unibus addr = 176742_8

The 16-bit low order data buffer register of the full-word port read/write-able by both systems.

DBR1 176744

The high order DBR for fw port

DBR3 FCFDE4 176746

The 16-bit data buffer register of the half-word read/write-able by both systems.

MAR1 FCFDE6 176750

The 16-bit memory address register for low order half-word of the full-word port

MAR2 FCFDE8 176752

MAR for high order halfword
for full-word port transfer. If initiated by the Emmy system device. then only the MAR1 will be used and bit 0-1 should both be zero. Low order word is sent out first with the given byte address and high order word is sent with the bit 1 = 1. If initiated by Unibus, the contents of MARL is checked with MAR 2 which is updated when the high order word is received for consistency. The transfer may only be on full word boundary.

MAR3 FCFDEA 176754

The 16-bit memory address register for half word port. Read/write-able to both bus systems.

All 16 bits are sent onto Unibus for Emmy initiated transfer. Only the lower 12 bits are updated (the rest are set to zero) and concatenated with the output of the address translator.

The whole register file is read/writeable from the Emmy System device, however it is only readable from the Unibus device. The register file state at the address:

Emmy bus address = 1111 1100 1110 1000 0000 0000 = $FCE800_{16}$

Unibus address = 164000_8

2.2 Microprogrammed Translation Sequencer

The sequencer is the central operation control section which responds to different transfer command and provides the correct sequencing of the operation. There are basically six types of operations (regardless of the data length specification in the command field).

2.2.1 Emmy Master/Unibus Slave

Emmy master unit send address (32-bit) onto the bus, after 60 ns (for deskew) asserts ASIG. BTU examines the address. If BTU is selected, the sequencer first checks TBSY. If TBSY = 1, then a REJ is issued and takes no further action except clearing the selected flag. If TBSY = 0, then the sequencer set TBSY = 1, asserts AACK and sends T-REG to the Unibus Interface Module (UIM). The Address Translation Module (ATM) will provide the corresponding address and control information for the Unibus transfer.

(1) For an Emmy write operation, the sequencer wait for DATA RDY from Emmy Interface Module (EIM) which is set true when DSIG is received and data is stored in the buffer. Upon receiving DATA RDY, the sequencer responds with DATA ACCEPTED which causes EIM asserts DACK and thus releases the Emmy bus. At the same time, the sequencer sends DATA RDY to UIM.

Back at the beginning of the cycle, UIM received TREQ from the sequencer which caused UIM to issue NPR to Unibus Arbitrator, and waiting for the bus master ship to be assigned. Once the bus has been grasped, the UIM is checked for DATA RDY from the sequencer. If RDY, UIM gates Address, DATA and control onto the Unibus after 100 ns (for deskew), asserts MSYN. UIM, after receiving assertion of SSYN, negates MSYN, then deskew for 100ns again to ensure that the negation of MSYN is received by all devices before the A and C lines lose their validity, and then

removes A, C and D lines thus releases the bus. At this moment transfer is completed and reset TBSY = 0.

For transfer requiring more than one Unibus cycle (e.g. transfer data from control store (32-bit) to mag tape (8-bit)), the sequencer issues a SACK INH to UIM until the last cycle started.

(2) For an Emmy read operaton, after TREQ is sent to UIM, the sequencer waits for DATA RDY from UIM, for transfer requires more than one cycle (e.g. read from mag tape into control store). The sequencer assembles data to the required length specified in the command field of the address word. Then it asserts DATA RDY to EIM, at the same time it sends DATA ACCEPTED to UIM and releases the Unibus.

EIM receives DATA RDY from the sequencer, then gates DATA on the bus. After 100 ns (for desckew), it asserts DSIG. EIM, after receiving assertion of DACK, it negates DSIG, and sends DATA ACCEPTED to the sequencer. This completes the transfer and reset TBSY = 0.

2.2.2 Unibus Master/Emmy Slave

Unibus master unit sends address (18-bit) together with control onto the bus (for DATA-OUT operation, DATA (16-bit) is also gated on the bus). BTU examines the dddress. If BTU is selected, the sequencer first checks TBSY, if TBSY = 1, then WAIT until it is cleared. In case TBSY = 0, it then proceeds. The address and control information is latched in the ATU which accordingly provides the 32-bit address word and set TBSY = 1.

(3) For a Unibus write operation, the sequencer latches DATA in the buffer and sents T-REQ to EIM. EIM requests and grasps the master ship of the bus then gates the address word on to the bus. After 100 ns EIM asserts ASIG wait for AACK from the bus slave unit. Upon receiving AACK, EIM checks for the data status is RDY or not.

The Unibus master is responsible to provide the right number of bytes to form the data which length is specified in the Unibus command word. The sequencer checks for T completed. If asserted, it issues DATA RDY to EIM.

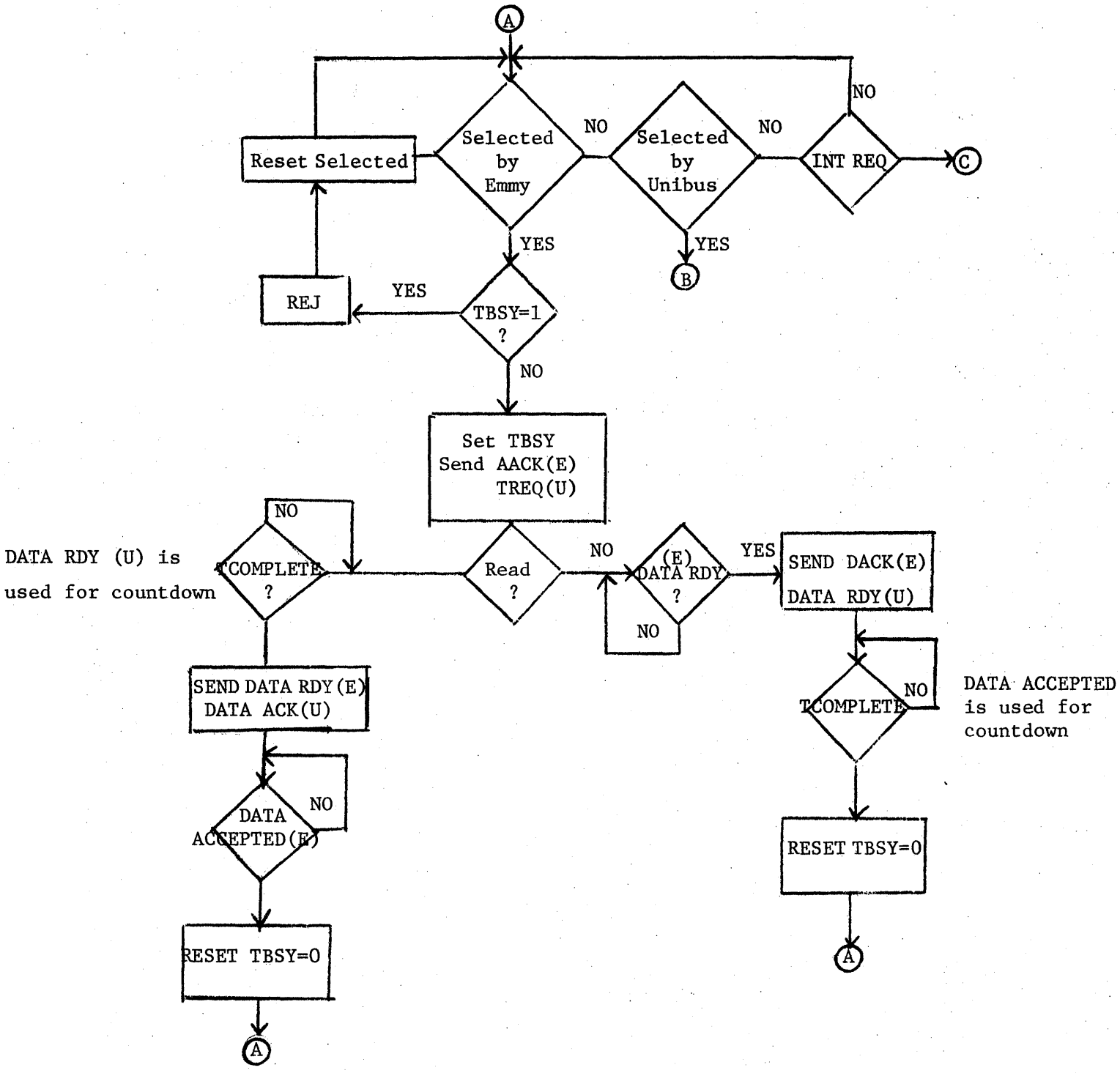
EIM receives DATA RDY, then gates data onto the bus, after 100 ns it asserts DSIG, when DACK is received. EIM sends DATA ACK to the sequencer indicating completion of the transfer. Sequencer reset TBSY = 0.

(4) For a Unibus read operation, the sequencer sends T-REQ to EIM, EIM requests and grasps the bus then gates the address word onto the bus. After 100ns EIM asserts ASIG, waiting for AACK from the bus slave unit and then waiting for the data to be received (signaled by DSIG). When data is received, it issues DATA RDY to the sequencer.

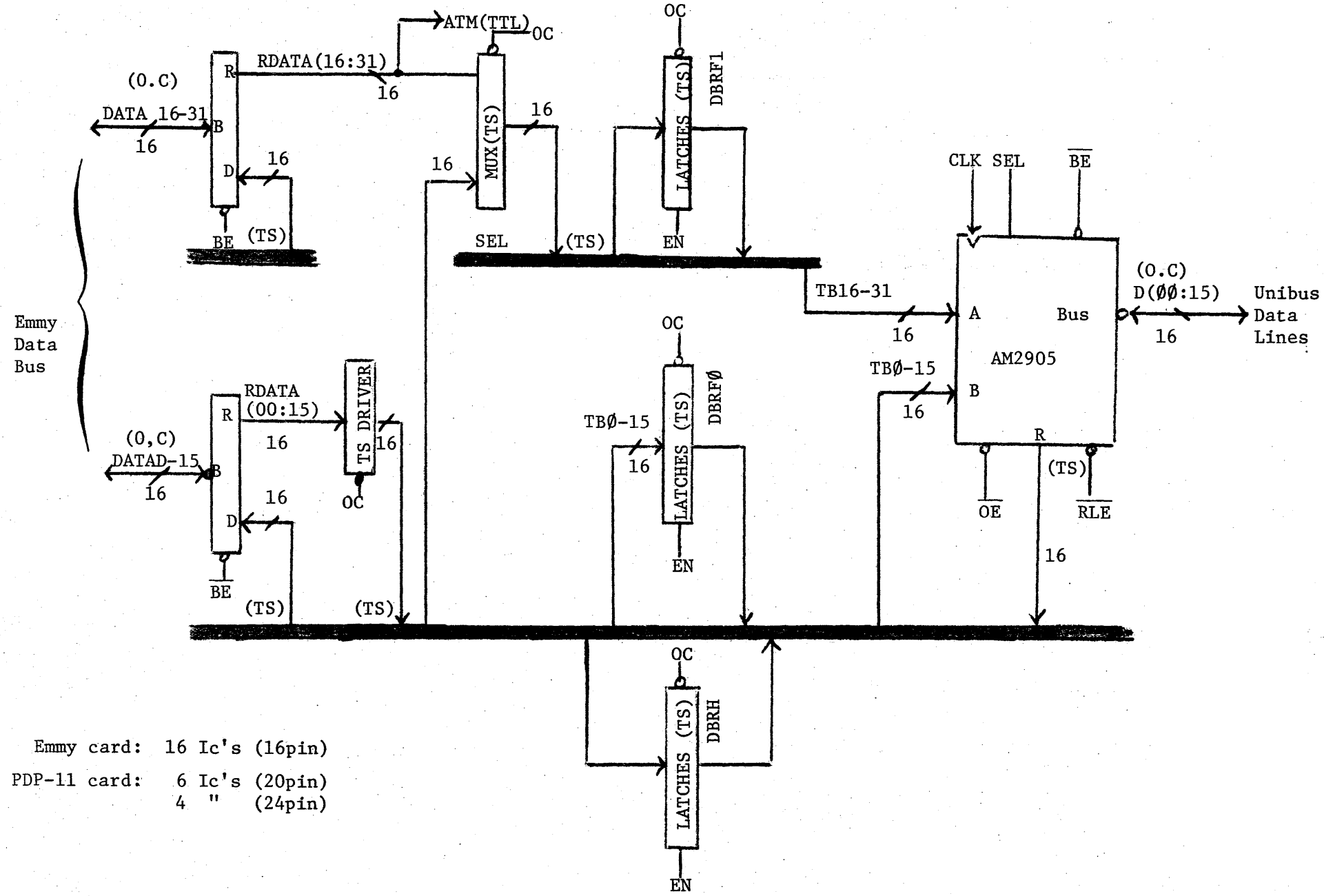
The sequencer disassembled the data into desired form specified on the Unibus command word, then issues DATA RDY, which then gates data on to the bus. After 100ns, assert SSYN. Sequencer check for T complete. IF asserted, then reset TBSY = 0, complete the transfer.

2.2.3 Register Read/Write

The MATCH internal registers are accessible to both bus systems. The requests from one bus system are served without interferring the other. During this service, the TBSY is set to "1" to indicate its status.



Emmy Master/Unibus Slave R/W Microprogram Flow Diagram



Emmy card: 16 Ic's (16pin)

PDP-11 card: 6 Ic's (20pin)
4 " (24pin)

Data Path with Tri-State TB (Transfer Bus)