CT-64 Serial Interface Assembly Instructions

In order for the CT-64 to communicate via a three wire system, a phone line or a magnetic tape data storage system, the parallel ASCII data must be broken down into sequential one bit at a time form both when coming out of the keyboard and going into the terminal. The serial interface or UART (Universal Asynchronous Receiver/Transmitter) provides this conversion from the parallel form into a series of properly timed one's and zero's including not only the serial data, but the start, stop and parity bits as well. The reverse is true during the receive mode. The baud rate or speed at which the serial data is transmittted or received, is 110, 150, 300, 600 or 1200 baud. There is a provision for ECHO off where the data is transmitted to the receiver (computer), but is not displayed on the screen until it is transmitted back by the receiver; or ECHO on where the data is transmitted and simultaneously put up on the screen and is not echoed back by the receiver.

The input/output connections are RS-232 compatable which will attach directly to most couplers and data sets, however, to record on or play-back from magnetic tape it will be necessary to build some kind of FSK encoder/decoder system to get the digital data on and off the tape since this is not provided on the interface. The RS-232 pin connections include transmitted data, received data, terminal "ready" and ground. There are no provisions for transmit/receive switching. Data to be transmitted can either be provided by the screen read board or the keyboard. The interface normally monitors the keyboard, however a "ready to send" command from the screen board locks out the keyboard and allows the screen read board to transmit its data.

The entire circuit is built on a 3 3/8" x 9 1/2" circuit board which is plugged onto the main board at connector strips J3 and J4. Switch connections to the serial interface board are provided by 12 pin connector JS-1, while the keyboard is plugged onto 12 pin connector JS-2 rather than J9 of the main terminal board as is done if the interface board is not used.

PC Board Assembly

NOTE: Since all of the holes on the PC board have been plated thru, it is only necessary to solder the components from the bottom side of the board. The plating provides the electrical connection from the "BOTTOM" to the "TOP" foil of each hole. It is important that none of the connections be soldered until all of the components of each group have been installed on the board. This makes it much easier to interchange components if a mistake is made during assembly. Be sure to use a low wattage iron (not a gun) with a small tip. Do not use acid core solder or any type of paste flux. We will not guarantee or repair any kit on which either product has been used. Use only the solder supplied with the kit or a 60/40 alloy resin core equivalent. Remember all of the connections are soldered on the bottom side of the board only. The plated-thru holes provide the electrical connection to the top foil.

( ) Attach all of the resistors to the board. As with all other components unless noted, use the parts list and component layout drawing to locate each part and install from the "TOP" side of the board bending the leads along the "BOTTOM" side of the board and trimming so that 1/16" to 1/8" of wire remains. Solder.

( ) Install all of the capacitors on the board. Be sure to orient the electrolytic capacitors correctly. The polarity is indicated on the component layout drawing. Solder. Be sure one of the two leads of capacitor C12 is inserted in the center pad of the group of seven holes. (TOP side)

( ) Install the transistors and diodes on the board. The diodes must be turned so the banded end corresponds with that shown on the component layout drawing, and the transistors must be turned so its lead configuration matches with that of the board. Solder. Leave about a 1/8" space between Q2 and the circuit board to prevent the transistor's metal case from shorting to the foil of the PC board.

( ) Install all of the integrated circuits on the board except IC3 being very careful to install each in its correct position. Do not bend the leads on the back side of the board. Doing so makes it very difficult to remove the integrated circuits should replacement ever be necessary. The semicircle notch on the end of the package is used for reference and should match with that shown on the component layout drawing for each of the IC's. Make sure the integrated circuits are down firmly against the board and solder.

( ) Now attach the two fifteen pin female edge type connectors to the board. These must be installed from the "TOP" side of the board and pressed down so the connectors seat firmly aginst the board. Solder.

( ) Attach the 12 pin wafercon connector JS-2 to the circuit board from the "BOTTOM" side making sure to turn it exactly as shown in the component layout drawing. Note that the connector already has the pins installed. Make sure all of the pins are firmly against the nylon support. They can work loose when pressing the connector onto the board. Solder.

( ) The 12 male printed circuit type pins should now be inserted into the blank female connector housing that does not have the nylon insulation between the pins. Do not confuse these pins with the crimp type which look very similar. The pins must be inserted from the back side of the connector into the housing until they snap into place. Orient the connector exactly as it is shown on the component layout drawing and install it in the JS-1 position from the "BOTTOM" side of the board.

( ) Install the crystal on the board. The crystal should be installed parallel to the board approximately 1/4 inch off the surface of the board. It is a good idea to wrap the crystal with a small amount of tape to keep the case from shorting to the board. Solder.

( ) If the CT-S will be used with an AC-30 Cassette Interface or other device which requires access to the UART's 16X clock, the A, B and C jumpers should be left open. If external access to the clock is not desired, jumper point A to point C.

( ) If you want to guarantee that the receiver remains off during a screen read dump, you will probably want to jumper point S to R on the interface board. If high baud rates are used and/or the turn-around time from whatever feeds the terminal is fast you may have to omit this jumper. If so, you must be sure the terminal is not in the "echo" mode and that whatever feeds the receiver of the terminal doesn't transmit during a screen dump. If a screen read is not being used jumper S to R.

( ) It is also necessary to program the interface board for the correct parity and number of bits to be handled. It will be necessary for the user to either know or find out what type of parity and bit number their computer system is using so the correct jumpers may be installed in the interface board. The transmit and receive formats are identical and are programmed with jumpers as follows:

ODD parity, NO bit 8 - jumper J to K and jumper I to H and jumper G to F
EVEN parity, NO bit 8 - jumper I to H and jumper G to F
NO parity, NO bit 8 - jumper I to H
NO parity, 8 bits - NO jumpers (Bit 8 selectable 0 or 1 through external switch)
NO parity, bit 8 = 0 - jumper E to D (correct for use with SWTPC 6800 computer system)

( ) Next program the input characteristics of the 8 th bit. Normally jumper Q to P. If you wish to receive the 8 th bit from your computer (for highlighting) jumper [illegible] to Q.

( ) The appropriate "keypressed" strobe jumper should be installed. If your keyboard's strobe is negative, solder a jumper wire between pads L and N. Our KBD unit will work in this configuration. Jumpering pad M to N instead is used for positive "keypressed" strobes where the pulse is clean and there is no ringing. The board must not be wired for a negative "keypressed" strobe (L to N) unless the keyboard strobe is truly negative going.

NOTE: When using the CT-S with a SWTPC 6800 / AC-30 system and a KBD 3 or 5 keyboard the normal jumpers will be E to D, L to N, Q to P and R to S.

( ) Now that most of the components have been installed on the board double check to make sure that all have been installed correctly in their proper location.

NOTE: MOS integrated circuits are susceptable to damage by static electricity. Although some degree of protection is provided internally within the integrated circuits, their cost demands the utmost in care. Before opening and/or installing any MOS integrated circuits you should ground your body and all metallic tools coming into contact with the leads thru a 1 M ohm 1/4 watt resistor (supplied with the kit). The ground must be an "earth" ground such as a water pipe, and not the circuit board ground. As for the connection to your body, attach a clip lead to your watch or metal ID bracelet. Make absolutely sure you have the 1 Meg ohm resistor connected between you and the "earth" ground, otherwise you will be creating a dangerous shock hazard. Avoid touching the leads of the integrated circuits any more than necessary when installing them, even if you are grounded. On those MOS IC's being soldered in place, the tip of the soldering iron should be grounded as well (separately from your body ground) either with or without a 1 Meg ohm resistor. Most soldering irons having a three prong line cord plug already have a grounded tip. Static electricity should be an important consideration in cold, dry environments. It is less of a problem when it is warm and humid.

( ) Install MOS inetgrated circuit IC 3 following the precautions given. Do not bend the leads on the back side of the board and make sure that it is oriented correctly. Solder.

( ) Working from the TOP side of the board, fill in all of the feed thrus with molton solder. The feed thrus are those unused holes on the board whose internal plating connects the TOP and BOTTOM circuit connections. Filling these feed thrus with molten solder guarantees the integrity of the connections and increases the current handling capability.

( ) Now check very carefully to make sure that all components have been soldered. It is very easy to miss some connections when soldering which can really cause some hard to find problems later during the check out phase. Also check for solder "bridges" and "cold" solder joints which are also a common problem.

( ) Looking at the board from the "TOP" side with the connectors at the bottom, press the nylon indexing plug into J3 pin 4.

( ) This completes the circuit board assembly phase of the instructions. This board should not be installed onto the main terminal board until the main board itself is working and has been completely checked out according to the checkout phase of the terminal assembly instructions.

JS-1 Connector Wiring

Connector JS-1 provides several of the control connections to the interface. Using the wiring table below, attach the wires to the female pins of the 12 pin connector supplied with the interface. All of the wires carry low currents and may be #24 gauge or larger. When all of the pins have been attached, insert each into the 12 pin nylon housing from the numbered side making sure you snap each pin into the appropriate hole. Note that the connector block is marked with the assigned pin numbers. Be sure to insert the pins in the correct hole the first time since the pins cannot be removed after insertion. The connections that select the different baud rates can be connected to a 5 position rotary switch if desired.

JS-1 FEMALE PIN #	LENGTH (in.)	FUNCTION	TO
1	-	Ground bus	computer, etc.
6	-	RS-232 output	" "
7	-	RS-232 input	" "
2	-	"Terminal Ready"	" "
9	-	110 baud enable	ground for 110 b
10	-	150 baud enable	ground for 150 b
11	-	300 baud enable	ground for 300 b
12	-	600 baud enable	ground for 600 b
3	-	1200 baud enable	ground for 1200 b
4	23	Ground for transmitter off	KBD-5 pin T
5	23	Ground for receiver off	KBD-5 pin R
8	23	Ground for echo off	KBD-5 pin E

NOTE: The terminal ready line goes high when power is applied to the terminal and is required by certain computers and modems. No more than 5 mA should be drawn from this line. The SWTPC 6800/AC-30 system does not require the terminal ready line.

Note: If your system requires a "BREAK" key, it can be implemented by connecting +5 volts thru a 100 ohm 1/4 watt resistor to one side of a SPST pushbutton switch. Connect the other side of the switch to the transmit output of the CT-S interface board (JS-1 pin 6).

RS-232 Applications

If you will be using the unit with a standard RS-232 plug, connect the unit as follows:

RS-232		JS-1
Pin 1	ground	Pin 1
Pin 2	transmitted data	Pin 6
Pin 3	received data	Pin 7
Pin 7	ground	Pin 1
Pin 20	"terminal ready"	Pin 2

Checkout and Use

Note that when the interface is used, the keyboard must be plugged into JS-2 on the interface board rather than J9 on the main board. The easiest way to check the unit out is to operate it without anything connected to the output connector. This should display everything that is typed on the screen where it can be seen and checked. Since this mode uses both the transmit and receiver circuitry. it is a good way to check everything on the interface for proper operation.

Parts List - CT-S Serial Interface Board

Resistors

____	R1	22K ohm 1/4 watt resistor
____	R2	22K " " " "
____	R3	22K " " " "
____	R4	22K " " " "
____	R5	22K " " " "
____	R6	22K " " " "
____	R7	22K " " " "
____	R8	1K " " " "
____	R9	47K " " " "
____	R10	180 " " " "
____	R11	1.8K " " " "
____	R12	470 " " " "
____	R13	1.8K " " " "
____	R14	470 " " " "
____	R15	1K " " " "
____	R16	22K " " " "
____	R17	1K " " " "
____	R18	12K " " " "
____	R19	2K " " " "
____	R20	1K " " " "
____	R21	1K " " " "
____	R22	1K " " " "
____	R23	3.9K " " " "
____	R24	22K " " " "
____	R25	27 " " " "
____	R26	2.7K " " " "
____	R27	47K " " " "
____	R28	5.6K " " " "
____	R29	1K " " " "
____	R30	330 " " " "
____	R31	1K " " " "
____	R32	1K " " " "
____	R33	1K " " " "
____	R34	1K " " " "
____	R35	1K " " " "
____	R36	1K " " " "
____	R37	1K " " " "
____	R38	12K " " " "
____	R39	1K " " " "
____	R40	1K " " " "
____	R41	1K " " " "
____	R42	1K " " " "
____	R43	2.7K " " " "
____	R44	1.8K " " " "
____	R45	1K " " " "

Capacitors

___		C1	330 pfd capacitor
___		C2	47 pfd "
___		C3	470 pfd "
___	*	C4	33 mfd electrolytic capacitor
___		C5	0.01 mfd disc capacitor
___	*	C6	33 mfd electrolytic capacitor
___		C7	100 pfd capacitor
___		C8	0.001 mfd disc capacitor
___		C9	330 pfd capacitor
___		C10	0.1 mfd disc capacitor
___		C11	0.1 " " "
___		C12	0.1 " " "
___		C13	0.1 " " "
___		C14	330 pfd capacitor
___		C15	0.005 mfd disc capacitor

Semiconductors

___	*	D1	1N914/1N4148 silicon diode
___	*	D2	" " "
___	*	D3	" " "
___	*	D4	" " "
___	*	D5	" " "
___	*	D6	" " "
___	*	D7	" " "
___	*	Q1	2N5210 silicon transistor
___	*	Q2	SS1122 " "
___	*	Q3	2N5210 " "

Integrated Circuits

___	*	IC1	7497 6 bit rate multiplier
___	*	IC2	7493 4 bit binary counter
___	*	IC3	1013 UART (MOS)
___	*	IC4	74157 data selector
___	*	IC5	74132 quad Schmitt NAND gate
___	*	IC6	7400 quad NAND gate
___	*	IC7	74123 dual one-shot
___	*	IC8	7404 hex inverter
___	*	IC9	7474 dual "D" flip-flop
___	*	IC10	74157 data selector
___	*	IC11	7404 hex inverter
___	*	IC12	7403 quad o.c. NAND gate

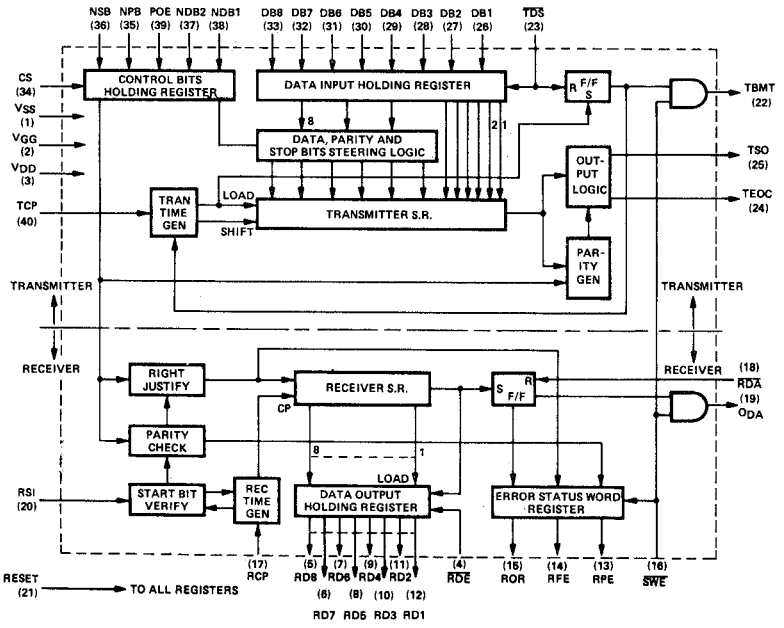
Misc.

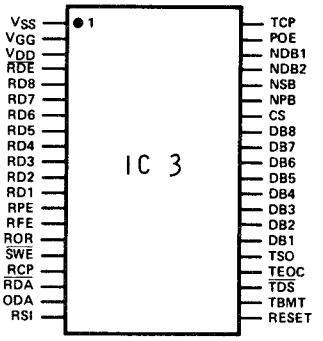
___		Y1	307.2 KHz series resonant crystal

* denotes a polarized part which must be inserted as shown on the component layout drawing

Theory of Operation

The serial interface circuit has been designed around a single UART (Universal Asynchronous Receiver/Transmitter) chip which actually does most of the work. The other circuitry on the interface board interfaces the chip itself to the circuitry on the main terminal board. The diagram below shows all of the pin connections to the integrated circuit as well as a block diagram of its internal structure. This is followed by a brief functional description of each of the pins.





PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ± 5%
(2)	V_{GG}	−12 Volt ± 5%
(3)	V_{DD}	Ground
(21)	RESET	A V_{IH} resets all internal registers and counters. The transmitter status outputs TBMT and TEOC are set to V_{OH} indicating the input transmitter buffer register is empty. The TSO output generates V_{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V_{OL} state.
(38)	NDB1	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS
V_{IL}	V_{IL}	V_{IL}	5	1
V_{IL}	V_{IL}	V_{IH}	6	1
V_{IL}	V_{IH}	V_{IL}	7	1
V_{IL}	V_{IH}	V_{IH}	8	1
V_{IH}	V_{IL}	V_{IL}	5	1.5
V_{IH}	V_{IL}	V_{IH}	6	2
V_{IH}	V_{IH}	V_{IL}	7	2
V_{IH}	V_{IH}	V_{IH}	8	2

(35)	NPB	NO PARITY BIT. A V_{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V_{OL} condition.
(39)	POE	PARITY ODD/EVEN. If the NPB input is V_{IL}, the parity mode is ODD if POE is V_{IL} and EVEN if POE is V_{IH}. The parity mode is the same for both the transmitter and receiver.
(34)	CS	CONTROL STROBE. A V_{IH} loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER. To load the control inputs for static operation CS can be hard-wired to V_{IH}.
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT
(27)	DB2	HOLDING REGISTER by $\overline{TDS}$. Input data must overlap $\overline{TDS}$ by 200 nsec.
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit
(29)	DB4	
(30)	DB5	

(31) (32) (33)	DB6 DB7 DB8	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(23)	$\overline{TDS}$	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH}, the START bit will be generated on the first negative transition of the input clock TCP following the return of $\overline{TDS}$ to a V_{IH} state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a $\overline{TDS}$ is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless $\overline{SWE}$ is a U_{ZL}.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12) (11) (10) (9) (8) (7) (6) (5)	RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when $\overline{RDE}$ is a V_{IL}. The eight data outputs are in a tri-state mode if $\overline{RDE}$ is a V_{IH}. Data is presented at the outputs right justified with RDI the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V_{OL}.
(4)	$\overline{RDE}$	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.

(18) $\overline{RDA}$ RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL}. If ODA is not reset by $\overline{RDA}$ the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.

(15) ROR RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening $\overline{RDA}$. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(14) RFE RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(13) RPE RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(16) $\overline{SWE}$ STATUS WORD ENABLE. A V_{IL} enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When $\overline{SWE}$ is V_{IH} all status outputs are in the tri-state mode.

For output configurations not requiring a tri-state condition for the status outputs, $\overline{SWE}$ may be tied directly to ground.

Transmit Mode

Both the outputs from the keyboard and the screen read board are fed into data selectors IC4 and IC10 which select either one of the two sets of inputs with the screen read taking priority. Normally the keyboard is selected as the input, however if the screen read board starts to send data, the incoming normally low to high transition at J4 pin 13 triggers IC7A, a retriggerable 350 ms one shot which selects the screen read inputs and locks out the keyboard, by driving pin 2 of IC4 and IC10 low. It also blocks any data from being received during a screen read if the jumper from S to R is installed, by forcing pin 8 if IC9A low which gates the "output data available" line into the "reset data available" line of the UART chip. Since the keyboard and receiver are disabled for at least 350 ms after each character dumped during a screen read, there may be problems with a computer sending a return message too soon after the screen read is completed especially when using high baud rates. In these situations, you may not want to lock out the receiver during a screen read transmission and can omit the jumper between pints S and R. You must be sure, however, the terminal is not in the "echo" mode and that the computer does not attempt to send data to the terminal until the screen dump has been completed as indicated by an ! transmission if the auto stop function on the screen read board is being used.

Regardless of whether the data to be transmitted comes from the screen read card or the keyboard, it exits from the data selector IC4 pin 12 to IC5A pin 9 where it is AND ed with the "transmitter buffer empty" output from the UART chip, IC-3, pin 22 where when high, sets the output of the AND gate latch, IC6 pin 11 high. Each time this IC6 A and B latch is set, it generates a 250 nanosecond pulse thru IC7B providing the "transmitter data strobe" for IC3 pin 23 thus loading the data at the output of the IC4 and IC10 data selectors into the input buffer of the UART chip, IC3. At the fall of the same pulse, a "data accepted" pulse is supplied to the screen read until it resets and forces IC6A pin 9 low which resets the IC6 A and B latch. This reset pulse sent to the screen read board allows it to find and store its next character until the UART transmitter buffer is ready for it. This double buffering enables the transmitter to transmit at up to 1200 baud without gaps or hesitations.

The serial data leaves the UART chip, through the "transmitter serial output" IC3 pin 25 where it is AND ed with the transmitter ON/OFF input at IC12C. Transistor Q2 then converts the serial TTL level output to RS-232 formated data.

Receive Mode

The incoming RS-232 serial data is converted into TTL compatable levels by the Schmitt trigger circuitry IC5A and its related components, providing approximately 1.5 volts of hysteresis. The output at IC11C pin 8 is then gated with the "receiver ON/Off" and OR ed with the "echo ON/OFF" and fed onto the UART chip's serial input, IC3 pin 20. When

the UART chip sees the stop bits of the character being received, it raises its "output data available" line, IC3 pin 19. If IC9A pin 8 is high, it means the terminal already has a character awaiting loading and is not ready to accept the new character waiting in the "receiver data holding registers". When the character in the terminal's register is finally loaded, the "character accepted" line feeding IC9A pin 11 pulses low toggling IC9A forcing pin 8 low. This allows IC12 to pulse the output of IC5C low clearing the "output data available" line and generating a negative going "keypress strobe" to load the new character into the terminal's data registers. Note that the "keypress strobe" jumper of the main terminal board must be wired for a negative strobe when the serial interface is being used.

If an error is detected by the UART chip, it drives one of three IC3 outputs high. IC3 pin 14 goes high if a stop bit does not follow after the start bit and the correct number of data bits. IC3 pin 13 goes high if there is a parity error received. IC3 pin 15 goes high if there is a condition where the receiver is being sent characters faster than it can accept them. If any one of these three error conditions occurs. transistor Q1 turns on and deselects the receive outputs from IC3 and present a ? to the terminal as an error indication for the character(s) for which the error was received.

Miscellaneous Circuitry

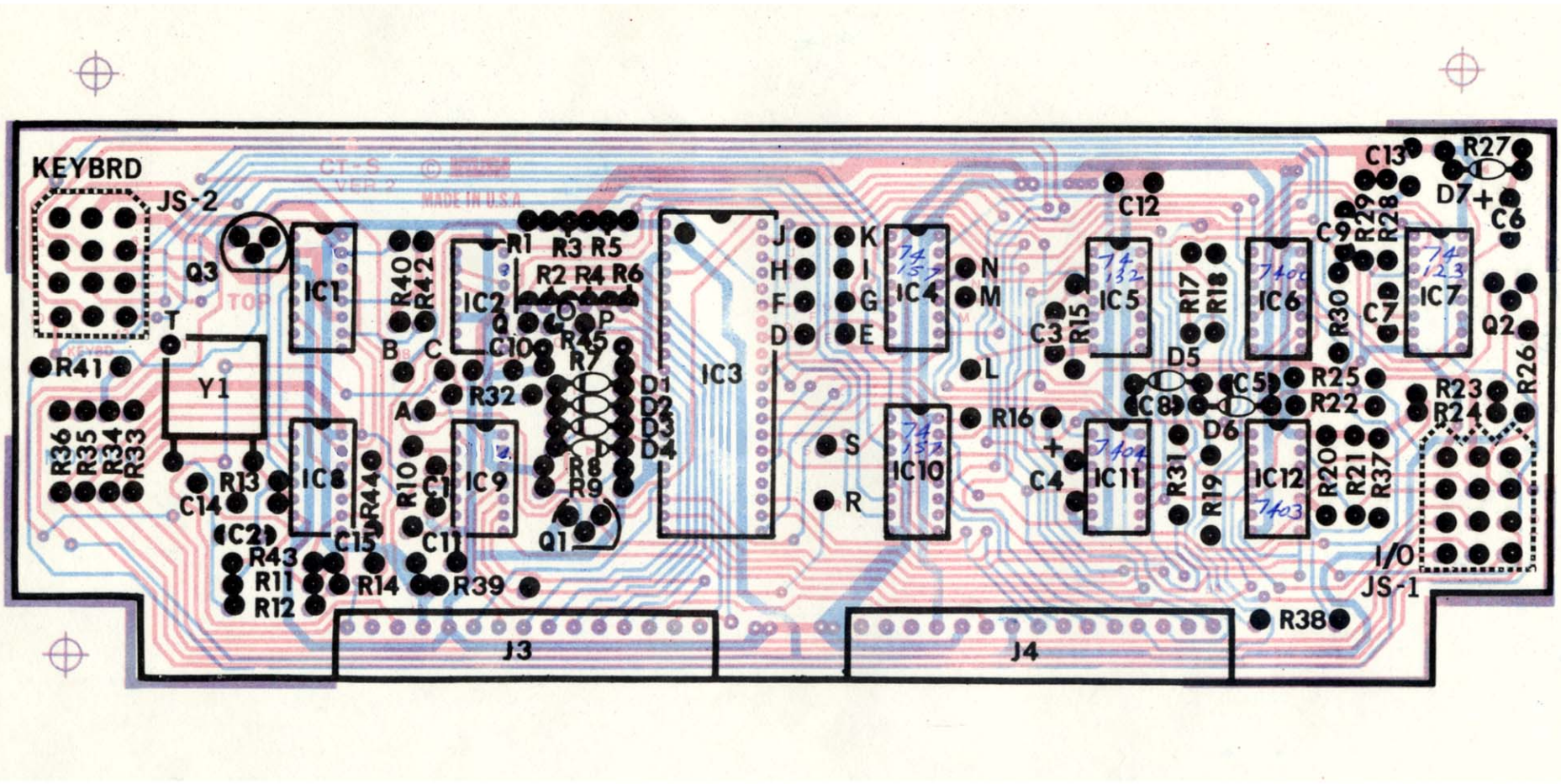
The standard baud rate for the unit is 110 baud and is derived from the 15840 Hz phase locked oscillator on the main board which is brought in through pin 1 of J3. The 15840 clock frequency is divided by nine by IC2 which gives 1760 Hz required by the UART chip for 110 baud. For higher baud rates a crystal oscillator must be used requiring a 307.200 KHz crystal as well as IC1 and IC8. Inverters IC8 A and B form an oscillator with a frequency of 307.200KHz which is fed onto flip-flop IC9B pin 4 where it is divided by two and in turn fed to the programmable divider, IC1 pin 9. By activating the correct select inputs of this integrated circuit, the correct output frequency necessary for each baud rate can be easily set. A five position rotary switch may be attached at jack JS-1 which grounds the selected baud rate line providing easy selection of either 110, 150, 300, 600 or 1200 baud. The 110 baud input inverter also drives the stop bit select line of the UART chip, IC3 pin 36, to select the correct number of stop bits for 110 baud operation.

A "terminal ready" signal is provided at JS-1 pin 2 to tell external devices when the terminal is powered up, however, this output is a sense line only and should not be loaded with anything soucing or sinking more than 5 Ma.

A power up reset is provided by IC11E to clear out the registers inside of UART chip, IC3, when power is applied to the terminal.

Specifications

Receive Format		EIA RS-232 and TTL compatable with a mark equal to + 1.5 to -25 volts and a space equal to +3 to +25 volts. The range from +1.5 to +3 volts is the hysteresis region.
Input Impedence		1.8 K ohms
Transmit format		EIA RS-232 with a mark equal to $\pm$4.7 volts and a space equal to +4.7 volts. (2K ohm load)
Baud Rates		110, 150, 300, 600, 1200 selectable through connector wiring or switch
Stop Bits		Automatic selection of 2 stop bits for 110 baud, 1 stop bit for all other rates.
Parity		
	7 bit	Odd, even or no parity
	8 bit	No parity. Bit 8 can be programmed to a 0 or a 1 or will follow keyboard or computer.


KEYBRD
JS-2
Q3
T
Y1
R41
R36
R35
R34
R33
C14
R13
(C2)
R43
R11
R12
IC1
IC8
R40
R42
R44
C15
R14
IC2
IC9
R10
C1
C11
R39
R1
R3 R5
R2 R4 R6
C10
R45
R7
R8
R9
Q1
R32
A
B
C
D1
D2
D3
D4
IC3
J
H
F
D
K
I
G
E
S
R
IC4
IC10
N
M
L
R16
C12
C3
R15
IC5
IC11
C4
D5
C8
D6
R31
R19
R17
R18
IC6
IC12
C5
R25
R22
R20
R21
R37
C13
R27
D7
C9
R29
R28
C7
R30
IC7
C6
Q2
R26
R23
R24
I/O
JS-1
R38
J3
J4