

PRELIMINARY

OMTI 5098 *CREVISION*
AT COMPATIBLE
INTERFACE CHIP
REFERENCE MANUAL
MAY 1988

OMTI 5098 AT COMPATIBLE INTERFACE CHIP

REFERENCE MANUAL

(PART #20516)

REV.	REVISION HISTORY	PRINT DATE
	Original Issue	May 19, 1987
B	5098C Specified	May 26, 1988

Copyright 1987 by Scientific Micro Systems, Inc.

The information in this publication is subject to change without notice.

Scientific Micro Systems, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Scientific Micro Systems, Inc. product. No other circuit patent licenses are implied.

TABLE OF CONTENTS

Page Number:

SECTION 1. INTRODUCTION	1-1
1.1 General Description	1-1
1.2 OMTI 5098 "AT" Compatible Interface Chip	1-1
1.3 OMTI 5098C "AT" Compatible Interface Chip	1-1
1.4 Functional Overview	1-2
1.4.1 Host Interface and Decode	1-3
1.4.2 Host Data Bus	1-3
1.4.3 Winchester Interface Logic	1-3
1.4.4 Floppy Interface Logic	1-3
1.4.5 Memory Data Interface	1-3
1.4.6 Microcomputer Interface and Decode	1-3
1.5 Functional Overview, REV C	1-4
1.5.1 Host Interface and Decode	1-5
1.5.2 Host Data Bus	1-5
1.5.3 Winchester Interface Logic	1-5
1.5.4 Floppy Interface Logic	1-5
1.5.5 Memory Data Interface (FIFO)	1-5
1.5.6 Microcomputer Interface and Decode	1-5
1.6 Controller Block Diagram	1-6
 SECTION 2. INTERFACING	 2-1
2.1 Pin Descriptions (84 PIN PLCC)	2-1
2.2 Pin Descriptions (80 PIN PFP)	2-9
2.3 Pin Assignment (84 PIN PLCC)	2-16
2.4 Pin Assignment (80 PIN PFP)	2-17
 SECTION 3. INTERFACE REGISTER	 3-1
3.1 Host Interface Registers	3-1
3.2 Host Register Assignment	3-1
3.3 Host Read Register Description	3-1
3.3.1 Data Register 1F0(170)	3-1
3.3.2 Error Register 1F1(171)	3-2
3.3.3 Sector Count Register 1F2(172)	3-3
3.3.4 Sector Number Register 1F3(173)	3-3
3.3.5 Cylinder Register (LSB) 1F4(174)	3-3
3.3.6 Cylinder Register (MSB) 1F5(175)	3-3
3.3.7 Size/Head/Drive Register 1F6(176)	3-3
3.3.8 Status Register 1F7(177)	3-4
3.3.9 FDC 765 Main Status Register (OPTIONAL)	3-5
3.3.10 FDC 765 Data Register (OPTIONAL)	3-5
3.3.11 Secondary Status Register 3F6(376)	3-5
3.3.12 Head/Select Status Register 3F7(377)	3-6
3.4 Host Write Register Description	3-6
3.4.1 Data Register 1F0(170)	3-6
3.4.2 Write Precomp/RWC Register 1F1(171)	3-6
3.4.3 Sector Count Register 1F2(172)	3-6
3.4.4 Sector Number Register 1F3(173)	3-7
3.4.5 Cylinder Register (LSB) 1F4(174)	3-7
3.4.6 Cylinder Register (MSB) 1F5(175)	3-7
3.4.7 Size/Head/Drive Register 1F6(176)	3-7
3.4.8 Command Register 1F7(177)	3-7
3.4.9 Floppy Select/Control Register (OPTIONAL)	3-8

3.4.10	FDC 765 Data Register (OPTIONAL)	3-8
3.4.11	Host Control Register 3F6(376)	3-8
3.4.12	Floppy Data Rate Register (OPTIONAL)	3-9
3.5	Controller Read/Write Registers	3-10
3.6	Microcomputer Register Assignment	3-10
3.7	Microcomputer Read Register Description	3-10
3.7.1	INTRQ/CONTROLLER Status Register F0	3-10
3.7.2	Write Precomp Register F1	3-11
3.7.3	Sector Count Register F2	3-11
3.7.4	Sector Number Register F3	3-12
3.7.5	Cylinder Register (LSB) F4	3-12
3.7.6	Cylinder Register (MSB) F5	3-12
3.7.7	Size/Head/Drive Register F6	3-12
3.7.8	Command Register F7	3-13
3.8	Microcomputer Write Register Description	3-13
3.8.1	Head Select Register F0	3-13
3.8.2	Error Register F1	3-13
3.8.3	Sector Count Register F2	3-14
3.8.4	Sector Number Register F3	3-14
3.8.5	Cylinder Register (LSB) F4	3-14
3.8.6	Cylinder Register (MSB) F5	3-14
3.8.7	Size/Head/Drive Register F6	3-14
3.8.8	Status Register F7	3-15
3.8.9	External Control Register F8	3-16
3.8.10	Drive Control Register F9	3-17
3.8.11	Busy Command Comparater Register FA	3-19
3.8.12	Identifier Register FB	3-19
3.8.13	Additional Control Register FC (REV C ONLY)	3-19
3.8.14	Additional Control Register FD (REV C ONLY)	3-22
3.8.15	Additional Control Register FE (REV C ONLY)	3-23
3.8.16	Additional Control Register FF (REV C ONLY)	3-25

SECTION 4. PROGRAMMING CONSIDERATIONS 4-1

SECTION 5. D. C. CHARACTERISTICS 5-1

5.1	Absolute Maximum Ratings	5-1
5.2	Standard Test Conditions	5-1
5.3	D.C. Characteristics	5-1

LIST OF ILLUSTRATIONS

Page Number:

Figure 1.	Internal Block Diagram	1-2
Figure 2.	Internal Block Diagram, REV C	1-4
Figure 3.	Controller Block Diagram	1-6
Figure 4.	Pin Assignment (84 PIN PLCC)	2-16
Figure 5.	Pin Assignment (80 PIN PFP)	2-17

LIST OF TABLES

Page Number:

Table 1.	Host Register Assignment	3-1
Table 2.	Microcomputer Register Assignment	3-8

LIST OF APPENDIX

Page Number:

Appendix A AT Compatable Logic Diagram. A-1

SECTION 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The OMTI 5098 "AT" Compatible Interface chip provides all the function required for a winchester controller to interface to an AT compatible system when used with the OMTI 5055 Kombo Controller Chip. This chip provides a compatible 8 bit register set for all command, control and status along with a 16 bit data path to and from the host to the Winchester controller. The OMTI 5098 chip also includes the floppy decode logic required for a combination Winchester and floppy controller.

1.2 OMTI 5098 "AT" COMPATIBLE INTERFACE CHIP

- x Direct Interface to "AT" Compatible systems
- x No external logic required with OMTI 5055
- x Support for external floppy controller
- x High current drivers for host interface
- x Schmidt trigger inputs form host interface
- x Configurable primary or secondary address
- x 3 micron SLM CMOS Standard Cell Technology
- x 84-Pin PLCC Package or 80-Pin PFP package

1.3 OMTI 5098C "AT" COMPATIBLE INTERFACE CHIP

- x 100% Rev B hardware and firmware compatible
- x 2 word FIFO
- x Automatic Busy, Intrq and ECC Mode
- x 40 Pin compatible Bus Interface
- x 2 micron SLM CMOS Standard Cell Technology
- x 84-Pin PLCC Package or 80-Pin PFP package

1.4 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the OMTI 5098 'AT' Compatible Interface Chip. Each logic block is discussed in the following sections.

Figure 1. Internal Block Diagram

1.4.1 Host Interface and Decode

This block contains all the logic to interface an AT compatible computer to a winchester controller. This includes all the I/O address decode logic along with all the host read write registers.

1.4.2 Host Data Bus

This block contains the 16 bit bi-directional registers used to interface the Host to the microcomputer on the controllers microcomputer and also the memory data bus.

1.4.3 Winchester Interface Logic

This section controls the select logic for the external winchester, along with directing the disk drive status to the host computer.

1.4.4 Floppy Interface Logic

This section controls the select logic for the external floppy controller chip along with the control of the external floppy speed control logic.

1.4.5 Memory Data Interface

This section controls the transfer of data to and from the external eight bit buffer memory to and from the sixteen bit host computer. It is in this block that the 8 bit to 16 bit packing and unpacking is accomplished.

1.4.6 Microcomputer Interface and Decode

This block interfaces the microcomputer on the controller to the read write registers in which the host interfaces and also allows the microcomputer to initialize the OMTI 5098 Interface chip.

1.5 FUNCTIONAL OVERVIEW, REV C

Figure 2 illustrates the internal block diagram of the OMTI 5098C 'AT' Compatible Interface Chip. Each logic block is discussed in the following sections.

Figure 2. Internal Block Diagram

1.5.1 Host Interface and Decode

This block contains all the logic to interface an AT compatible computer to a winchester controller. This includes all the I/O address decode logic along with all the host read write registers.

1.5.2 Host Data Bus

This blocks contains the 16 bit bi-directional registers used to interface the Host to the microcomputer on the controllers microcomputer and also the memory data bus.

1.5.3 Winchester Interface Logic

This section controls the select logic for the external winchester, along with directing the disk drive status to the host computer.

1.5.4 Floppy Interface Logic

This section controls the select logic for the external floppy controller chip along with the control of the external floppy speed control logic.

1.5.5 Memory Data Interface

This section controls the transfer of data to and from the external eight bit buffer memory to and from the sixteen bit host computer. It is in this block that the 8 bit to 16 bit packing and unpacking is accomplished.

1.5.6 Microcomputer Interface and Decode

This blocks interfaces the microcomputer on the controller to the read write registers in which the host interfaces and also allows the microcomputer to initialize the OMTI 5098 Interface chip.

1.6 CONTROLLER BLOCK DIAGRAM

Figure 3 illustrates a complete controller block diagram using the OMTI 5098 "AT" Compatible Interface Chip along with an OMTI 5055 Kombo controller chip and an OMTI 5070 or OMTI 5027 Encode / Decode / VCD chip.

Figure 3. Controller Block Diagram

SECTION 2

INTERFACING

2.1 PIN DESCRIPTIONS (84 PIN PLCC)

Symbol	Type	Pin #	Name and Function
AEN	I	2	ADDRESS ENABLE (HOST): This signal is asserted during a DMA cycle. It is used to disable the decoding of the HOST I/O ADDRESS BUS during DMA cycles.
$\overline{\text{IORD}}$	I	3	I/O READ (HOST): This input signal is asserted to read data from an I/O address (A9 - A0, AEN is de-asserted).
$\overline{\text{IOWR}}$	I	4	I/O WRITE (HOST): This input signal is asserted to write data from an I/O address (A9 - A0, AEN is de-asserted).
D_(7:0)	I/O	5-11 13	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer data between the HOST and the 5098 internal/external registers. During WORD data transfers, these signals are the least significant byte of the data word.
$\overline{\text{WR_DACK}}$	I/O	12	WRITE DATA/DACK (CONTROLLER, REV C ONLY): This bi-directional signal performs two functions. When programmed as an output, this signal is asserted during a HOST write to the DATA REGISTER 1F0(170). When programmed as an input (DMA MODE), this signal is asserted while the DMA CONTROLLER is performing an I/O. This signal is configured as an input after a RESET.
ALE	I	14	ADDRESS LATCH ENABLE (HOST): This input signal is asserted to indicate that the HOST I/O ADDRESS is valid on the falling edge.

Symbol	Type	Pin #	Name and Function
"DS_0	0	15	<p>DRIVE SELECT ZERO: This open drain, 24 mA, output is asserted when a '0' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.</p> <p>REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this signal is the drive select for both a MASTER or a SLAVE. In the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.</p>
IO_CH_RDY	0	16	<p>I/O CHANNEL READY (HOST): This open drain, 24 mA, output signal is de-asserted to lengthen an I/O data cycle. This signal is only active during WORD MODE data transfers at I/O ADDRESS 1F0(170).</p>
"IO_CS_16	0	18	<p>I/O CHIP SELECT 16 BIT (HOST): This open drain, 24 mA, output signal is asserted to indicate that the present HOST data transfer is a 16-bit, 1 wait-state I/O cycle. It is derived from the 5098 DATA REGISTER 1F0(170) decode.</p>
"DS_1	I/O	19	<p>DRIVE SELECT ONE: This open drain 24 mA, output is asserted when a '1' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.</p> <p>REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this signal is configured as an input while in the MASTER MODE and as an output in the SLAVE MODE. It is used for the "PASSED DIAGNOSTIC signal.</p>
RESET_IN	I	20	<p>RESET IN (HOST): This input signal is asserted to indicate that a power-up or low voltage condition exist.</p>

Symbol	Type	Pin #	Name and Function
~RESET_OUT	O	21	RESET OUT: This output is an inverted copy of the RESET_IN signal or is asserted for a minimum of 1 microsecond indicating that the 5098 has an internal power-on reset.
~RESET_SOFT	O	23	SOFT RESET: This output signal is asserted as long as BIT 2 of WRITE REGISTER 3F6(376) is asserted.
~READY	I	24	READY: This input signal is available on BIT 6 of READ REGISTER 1F7(177). REV C: This signal is also available at BIT(1) of MICROCOMPUTER READ REGISTER F0.
~INDEX	I	25	INDEX: This input signal is available on BIT 1 of READ REGISTER 1F7(177).
DMA_INTRQ	I/O	26	DMA INTERRUPT REQUEST: When enabled, this level sensitive input causes the 5098 to become BUSY. The polarity of this signal is programmable and should be connected to the DMA INTERRUPT signal of the DMA controller. REV C: While in the DMA REQ/ACK MODE, this signal is programmed as an output. It is asserted when the 5098C has completed the block count defined by BITS(6,5) of HOST WRITE REGISTER 1F6(176). The polarity is programmable. If the DMA INTERRUPT REQUEST has been re-routed to the ~COMMAND output, this signal will be programmed as an input but will NOT be used by the 5098C.
DECODE_A	I	27	ADDRESS DECODE A (HOST): This internally pulled-up signal specifies the 5098 HOST I/O address range. If no connection is made to this signal the 5098 HOST REGISTER A range is 1F0 - 1F7 (HEX). If this signal is grounded, the 5098 HOST REGISTER A range is 170 - 177 (HEX).

Symbol	Type	Pin #	Name and Function
DECODE_B	I	28	ADDRESS DECODE B (HOST): This internally pulled-up signal specifies the 5098 HOST I/O address range. If no connection is made to this signal the 5098 HOST REGISTER B range is 3F0 - 3F7 (HEX). If this signal is grounded, the 5098 HOST REGISTER B range is 370 - 377 (HEX).
CONFIG	I	29	PROCESSOR CONFIGURATION (CONTROLLER): This internally pulled-up signal specifies the controller processor strobe inputs. If no connection is made to this signal, the 5098 is configured for a Z8-type processor. In this case, ALE_`AS = `AS, `IORD_`DS = `DS, `IOWR_RW = RW and IO_`MEM_`DM = `DM. If this signal is grounded, the 5098 is configured for an 8051-type processor. In this case, ALE_`AS = ALE, `IORD_`DS = `IORD, `IOWR_RW = `IOWR and IO_`MEM_`DM = IO_`MEM.
DMA_ACK	I	30	DMA ACKNOWLEDGE: This input signal, initiated by the DMA controller, indicates that a DMA transfer is taking place. REV C: While in the DMA REQ/ACK MODE, asserting this signal indicates an acknowledgment to a DMA_REQ.
DMA_REQ	O	31	DMA REQUEST: In conjunction with DMA_ACK, this output signal is asserted by the 5098 on the trailing edge of an IORD or IOWR to HOST ADDRESS 1F0(170) during data transfers. REV C: While in the DMA REQ/ACK MODE, this output is asserted to indicate a DMA transfer request.
RD_DREQ	O	32	READ DATA/DREQ (CONTROLLER, REV C ONLY): When programmed in the DMA MODE, this output signals that the 5098C is requesting a DMA cycle. In the NON-DMA MODE, it is asserted during a HOST read to the DATA REGISTER 1F0(170).

Symbol	Type	Pin #	Name and Function
~INENA	I	33	<p>INPUT ENABLE: This input signal is asserted by the DMA controller to enable the 5098 to drive the MEMORY Data bus.</p> <p>REV C: While in the DMA REQ/ACK MODE, this input has no meaning and can be unconnected.</p>
~OUTCLK	I	34	<p>OUT CLOCK: This input signal is asserted by the DMA controller to save data into the 5098 from the MEMORY Data bus.</p> <p>REV C: While in the DMA REQ/ACK MODE, this input has no meaning and can be unconnected.</p>
MEM_D(7:0)	I/O	35-42	<p>MEMORY DATA: These bi-directional signals are used to transfer data between the HOST and the Controller DMA Buffer Memory.</p>
AD_(7:0)	I/O	44-51	<p>ADDRESS/DATA BUS (CONTROLLER): These bi-directional, tri-state signals are used to transfer address and data between the 5098 and the controller processor. The processors ADDRESS is latched on the falling edge (8051-mode) or the rising edge (Z8-mode) of the ALE_~AS signal. the processors DATA is either read from or written to the 5098 (if selected) on the processors ~IORD_~DS/~IOWR_RW data strobes.</p>
ALE_~AS	I	52	<p>ADDRESS LATCH ENABLE/ADDRESS STROBE (CONTROLLER): This input signal is asserted to latch the controller microcomputers address into the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.</p>
~IOWR_RW	I	53	<p>I/O WRITE (8051) READ/WRITE (Z8) (CONTROLLER): This input signal is asserted in 8051 mode, to gate data from the controller to the 5098 (if selected). If the Z8-mode is selected, this input signal is low to indicate a write function and high to indicate a read function.</p>

Symbol	Type	Pin #	Name and Function
SYS_CLK	I	54	SYSTEM CLOCK (HOST, REV C ONLY): This input is used to synchronize the IO_CH_RDY output to the system clock.
~IORD_~DS	I	55	I/O READ (8051) DATA STROBE (Z8) (CONTROLLER): This input signal is asserted to gate data from the 5098 (if selected) to the ADDRESS/DATA BUS of controller processor (8051-mode). If the Z8-mode is selected, this input signal is used to gate data from (READ) or to (WRITE) the 5098 (if selected).
IO_~MEM_~DM	I	56	I/O ~MEMORY (8051) ~DM (Z8) (CONTROLLER): This input signal is used for as a chip select for the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.
~COMMAND	I/O	57	COMMAND: This output signal is asserted to indicate that a command has been written into WRITE REGISTER 1F7(177). It is de-asserted by writing the INTERNAL CONTROL REGISTER bit 2 with a '1' or a RESET. REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this open drain, 24 mA, signal is configured as an input while in the MASTER MODE during the diagnostic command. In the SLAVE MODE, it is configured as an output at all times. This signal is used for the ACTIVE/SLAVE PRESENT signal. It can also be programmed as the DMA_INTRQ signal. In this case, an external pull-up may be required. Irregardless of how the ~COMMAND signal is programmed, the status of the internal command latch is available at BIT(2) of MICROCOMPUTER READ REGISTER F0.
~WRT_GATE	I	58	WRITE GATE: This input signal is available on BIT 6 of READ REGISTER 3F7(377).

Symbol	Type	Pin #	Name and Function
~DCHG	I	59	DISK CHANGED: This internally pulled-up signal is available on BIT 7 of READ REGISTER 3F7(377). If this signal is not used, BIT 7 of READ REGISTER 3F7(377) can be TRI-STATEd by writing a '1' to BIT 4 of the INTERNAL CONTROL REGISTER F8.
RATE_1	O	60	FLOPPY DATA RATE 1: This output signal along with RATE_0 determine the flexible disk data rate.
RATE_0	O	61	FLOPPY DATA RATE 0: This output signal along with RATE_1 determine the flexible disk data rate.
~FDD_REG	O	62	FLOPPY DATA REGISTER: This output signal is asserted during an IOWR to HOST ADDRESS 3F2(372).
~CS_FDC	O	63	FLOPPY CONTROLLER SELECT: This output signal is asserted during an IOWR or IORD to HOST ADDRESS 3F4-3F5(374-375).
INTRQ	O	65	<p>INTERRUPT REQUEST: This TRI-STATE output signal indicates that the 5098 needs attention. It is enabled or disabled by writing a '0' or '1' respectively to BIT 1 of WRITE REGISTER 3F6(376). It is asserted by writing a '1' to BIT 0 of the INTERNAL CONTROL REGISTER F8 and is de-asserted by writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER F8, reading SYSTEM REGISTER 1F7(177) or writing SYSTEM REGISTER 1F7(177).</p> <p>REV C: Writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER will not de-assert the INTRQ signal. If the 5098C is programmed in the MASTER/SLAVE MODE, this output is only active while selected. If not selected, an internal 200 microamp pull-down can be enabled.</p>
D_(15:8)	I/O	66-73	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer the most significant byte of HOST data to or from the 5098 DATA REGISTER.

Symbol	Type	Pin #	Name and Function
A_(9:0)	I	75-84	I/O ADDRESS BUS (HOST): These input signals constitute the 10 BIT 5098 HOST I/O ADDRESS BUS and are internally decoded for the selection of internal and external 5098 registers.
VSS			GROUND: Pins 1,17,43,74
VDD			POWER: Pins 22,64

2.2 PIN DESCRIPTIONS (80 PIN PFP)

Symbol	Type	Pin #	Name and Function
$\overline{\text{CS_SEL}}$	I	2	CHIP SELECT MODE (REV C ONLY): This internally pulled-up signal programs the 5098C for CHIP SELECT MODE. When grounded, A ₍₉₎ becomes a $\overline{\text{CS_1Fx}}$ input. Asserting A ₍₉₎ along with an address of 0 - 7 on A _(2:0) will select the 5098C and access the appropriate register. A ₍₈₎ becomes a $\overline{\text{CS_3Fx}}$ input. Asserting A ₍₈₎ along with an address of 0 - 7 on A _(2:0) will select the 5098C and access the appropriate register. In the CHIP SELECT MODE, address inputs A _(7:5) can be used as input jumpers. They can be read at MICROCOMPUTER READ REGISTER F0 BITS(7:5). There are no internal pull-ups on these inputs so it is recommended that they be tied either to V _{ss} or V _{dd} . When this input is left open, normal addressing is selected.
A _(9:0)	I	3-12	I/O ADDRESS BUS (HOST): These input signals constitute the 10 BIT 5098 HOST I/O ADDRESS BUS and are internally decoded for the selection of internal and external 5098 registers.
AEN	I	14	ADDRESS ENABLE (HOST): This signal is asserted during a DMA cycle. It is used to disable the decoding of the HOST I/O ADDRESS BUS during DMA cycles.
$\overline{\text{IOR0}}$	I	15	I/O READ (HOST): This input signal is asserted to read data from an I/O address (A ₉ - A ₀ , AEN is de-asserted).
$\overline{\text{IOWR}}$	I	16	I/O WRITE (HOST): This input signal is asserted to write data from an I/O address (A ₉ - A ₀ , AEN is de-asserted).
D _(7:0)	I/O	17-24	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer data between the HOST and the 5098 internal/external registers. During WORD data transfers, these signals are the least significant byte of the data word.

Symbol	Type	Pin #	Name and Function
ALE	I	25	ADDRESS LATCH ENABLE (HOST): This input signal is asserted to indicate that the HOST I/O ADDRESS is valid on the falling edge.
~DS_0	O	26	DRIVE SELECT ZERO: This open drain, 24 mA, output is asserted when a '0' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY. REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this signal is the drive select for both a MASTER or a SLAVE. In the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY.
IO_CH_RDY	O	27	I/O CHANNEL READY (HOST): This open drain, 24 mA, output signal is de-asserted to lengthen an I/O data cycle. This signal is only active during WORD MODE data transfers at I/O ADDRESS 1F0(170).
~IO_CS_16	O	29	I/O CHIP SELECT 16 BIT (HOST): This open drain, 24 mA, output signal is asserted to indicate that the present HOST data transfer is a 16-bit, 1 wait-state I/O cycle. It is derived from the 5098 DATA REGISTER 1F0(170) decode.
~DS_1	I/O	30	DRIVE SELECT ONE: This open drain 24 mA, output is asserted when a '1' is written to BIT 4 of WRITE REGISTER 1F6(176). If the 5098 is in the NON-SELECT MODE, this output is only asserted during reads to REGISTER 1F7(177) or the controller is BUSY. REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this signal is configured as an input while in the MASTER MODE and as an output in the SLAVE MODE. It is used for the ~PASSED DIAGNOSTIC signal.

Symbol	Type	Pin #	Name and Function
RESET_IN	I	31	RESET IN (HOST): This input signal is asserted to indicate that a power-up or low voltage condition exist. While in the CHIP SELECT MODE, this input is inverted.
~RESET_OUT	O	32	RESET OUT: This output is an inverted copy of the RESET_IN signal or is asserted for a minimum of 1 microsecond indicating that the 5098 has an internal power-on reset.
~WR_~DACK	I/O	33	WRITE DATA/DACK (CONTROLLER, REV C ONLY): This bi-directional signal performs two functions. When programmed as an output, this signal is asserted during a HOST write to the DATA REGISTER 1F0(170). When programmed as an input (DMA MODE), this signal is asserted while the DMA CONTROLLER is performing an I/O. This signal is configured as an input after a RESET.
~RESET_SOFT	O	35	SOFT RESET: This output signal is asserted as long as BIT 2 of WRITE REGISTER 3F6(376) is asserted.
~READY	I	36	READY: This input signal is available on BIT 6 of READ REGISTER 1F7(177). REV C: This signal is also available at BIT(1) of MICROCOMPUTER READ REGISTER F0.
~INDEX	I	37	INDEX: This input signal is available on BIT 1 of READ REGISTER 1F7(177).
DMA_INTRQ	I/O	38	DMA INTERRUPT REQUEST: When enabled, this level sensitive input causes the 5098 to become BUSY. The polarity of this signal is programmable and should be connected to the DMA INTERRUPT signal of the DMA controller.

Symbol	Type	Pin #	Name and Function
			<p>REV C: While in the DMA REQ/ACK MODE, this signal is programmed as an output. It is asserted when the 5098C has completed the block count defined by BITS(6,5) of HOST WRITE REGISTER 1F6(176). The polarity is programmable. If the DMA INTERRUPT REQUEST has been re-routed to the ^COMMAND output, this signal will be programmed as an input but will NOT be used by the 5098C.</p>
DECODE_A	I	39	<p>ADDRESS DECODE A (HOST): This internally pulled-up signal specifies the 5098 HOST I/O address range. If no connection is made to this signal the 5098 HOST REGISTER A range is 1F0 - 1F7 (HEX). If this signal is grounded, the 5098 HOST REGISTER A range is 170 - 177 (HEX).</p>
CONFIG	I	40	<p>PROCESSOR CONFIGURATION (CONTROLLER): This internally pulled-up signal specifies the controller processor strobe inputs. If no connection is made to this signal, the 5098 is configured for a Z8-type processor. In this case, ALE_ ^AS = ^AS, ^IORD_ ^DS = ^DS, ^IOWR_ ^RW = ^RW and IO_ ^MEM_ ^DM = ^DM. If this signal is grounded, the 5098 is configured for an 8051-type processor. In this case, ALE_ ^AS = ALE, ^IORD_ ^DS = ^IORD, ^IOWR_ ^RW = ^IOWR and IO_ ^MEM_ ^DM = IO_ ^MEM.</p>
DMA_ACK	I	41	<p>DMA ACKNOWLEDGE: This input signal, initiated by the DMA controller, indicates that a DMA transfer is taking place.</p> <p>REV C: While in the DMA REQ/ACK MODE, asserting this signal indicates an acknowledgment to a DMA_REQ.</p>
DMA_REQ	O	42	<p>DMA REQUEST: In conjunction with DMA_ACK, this output signal is asserted by the 5098 on the trailing edge of an IORD or IOWR to HOST ADDRESS 1F0(170) during data transfers.</p>

Symbol	Type	Pin #	Name and Function
			REV C: While in the DMA REQ/ACK MODE, this output is asserted to indicate a DMA transfer request.
~INENA	I	43	INPUT ENABLE: This input signal is asserted by the DMA controller to enable the 5098 to drive the MEMORY Data bus. REV C: While in the DMA REQ/ACK MODE, this input has no meaning and can be unconnected.
~OUTCLK	I	44	OUT CLOCK: This input signal is asserted by the DMA controller to save data into the 5098 from the MEMORY Data bus. REV C: While in the DMA REQ/ACK MODE, this input has no meaning and can be unconnected.
MEM_D(7:0)	I/O	45-52	MEMORY DATA: These bi-directional signals are used to transfer data between the HOST and the Controller DMA Buffer Memory.
AD_(7:0)	I/O	54-61	ADDRESS/DATA BUS (CONTROLLER): These bi-directional, tri-state signals are used to transfer address and data between the 5098 and the controller processor. The processors ADDRESS is latched on the falling edge (8051-mode) or the rising edge (Z8-mode) of the ALE_~AS signal. the processors DATA is either read from or written to the 5098 (if selected) on the processors ~IORD_~DS/~IOWR_RW data strobes.
ALE_~AS	I	62	ADDRESS LATCH ENABLE/ADDRESS STROBE (CONTROLLER): This input signal is asserted to latch the controller microcomputers address into the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.

Symbol	Type	Pin #	Name and Function
~IOWR_RW	I	63	I/O WRITE (8051) READ/WRITE (Z8) (CONTROLLER): This input signal is asserted in 8051 mode, to gate data from the controller to the 5098 (if selected). If the Z8-mode is selected, this input signal is low to indicate a write function and high to indicate a read function.
SYS_CLK	I	64	SYSTEM CLOCK (HOST, REV C ONLY): This input is used to synchronize the IO_CH_RDY output to the system clock.
~IORD_DS	I	66	I/O READ (8051) DATA STROBE (Z8) (CONTROLLER): This input signal is asserted to gate data from the 5098 (if selected) to the ADDRESS/DATA BUS of controller processor (8051-mode). If the Z8-mode is selected, this input signal is used to gate data from (READ) or to (WRITE) the 5098 (if selected).
IO_~MEM_~DM	I	67	I/O ~MEMORY (8051) ~DM (Z8) (CONTROLLER): This input signal is used for as a chip select for the 5098. In 8051 mode, this input is active high. In Z8 mode, this input is active low.
~COMMAND	I/O	68	COMMAND: This output signal is asserted to indicate that a command has been written into WRITE REGISTER 1F7(177) It is de-asserted by writing the INTERNAL CONTROL REGISTER bit 2 with a '1' or a RESET. REV C: If the 5098C is programmed for MASTER/SLAVE MODE, this open drain, 24 mA, signal is configured as an input while in the MASTER MODE during the diagnostic command. In the SLAVE MODE, it is configured as an output at all times. This signal is used for the ACTIVE/SLAVE PRESENT signal. It can also be programmed as the DMA_INTRQ signal. In this case, an external pull-up may be required. Irregardless of how the ~COMMAND signal is programmed, the status of the internal command latch is available at BIT(2) of MICROCOMPUTER READ REGISTER F0.

Symbol	Type	Pin #	Name and Function
~WRT_GATE	I	69	WRITE GATE: This input signal is available on BIT 6 of READ REGISTER 3F7(377).
INTRQ	O	71	<p>INTERRUPT REQUEST: This TRI-STATE output signal indicates that the 5098 needs attention. It is enabled or disabled by writing a '0' or '1' respectively to BIT 1 of WRITE REGISTER 3F6(376). It is asserted by writing a '1' to BIT 0 of the INTERNAL CONTROL REGISTER F8 and is de-asserted by writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER F8, reading SYSTEM REGISTER 1F7(177) or writing SYSTEM REGISTER 1F7(177).</p> <p>REV C: Writing a '0' to BIT 0 of the INTERNAL CONTROL REGISTER will not de-assert the INTRQ signal. If the 5098C is programmed in the MASTER/SLAVE MODE, this output is only active while selected. If not selected, an internal 200 microamp pull-down can be enabled.</p>
RD_DREQ	O	73	<p>READ DATA/DREQ (CONTROLLER, REV C ONLY): When programmed in the DMA MODE, this output signals that the 5098C is requesting a DMA cycle. In the NON-DMA MODE, it is asserted during a HOST read to the DATA REGISTER 1F0(170).</p>
D_(15:8)	I/O	72 74-80	DATA BUS (HOST): These bi-directional, tri-state signals are used to transfer the most significant byte of HOST data to or from the 5098 DATA REGISTER.
VSS			GROUND: Pins 1,13,28,53
VDD			POWER: Pins 34,70

2.3 PIN ASSIGNMENT (84 PIN PLCC)

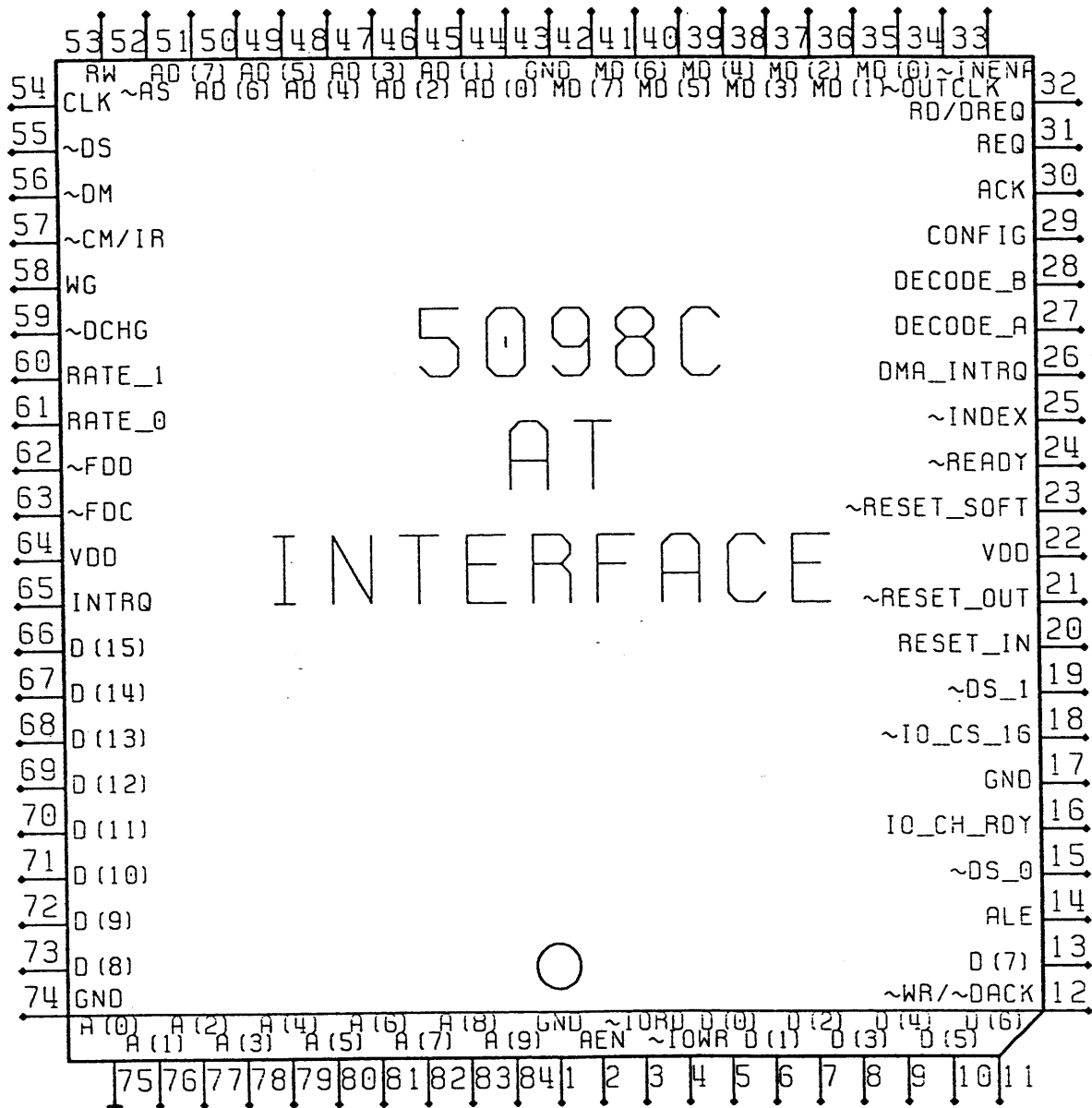


Figure 4. Pin Assignment (84 PIN PLCC)

2.3 PIN ASSIGNMENT (80 PIN PFP)

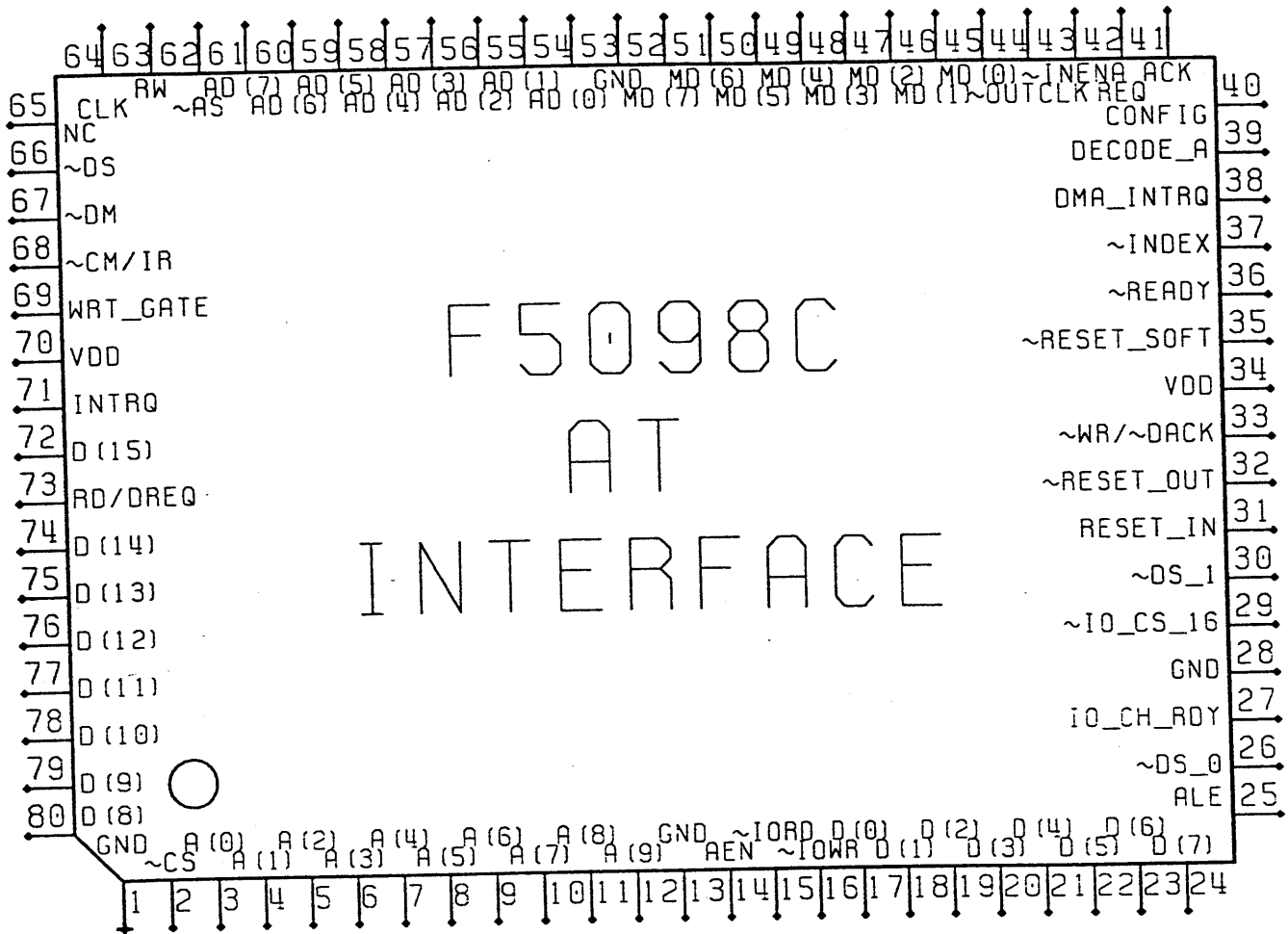


Figure 5. Pin Assignment (80 PIN PFP)

SECTION 3

INTERFACE REGISTERS

3.1 HOST INTERFACE REGISTERS

The OMTI 5098 contains 10 registers by which the HOST can communicate with the controller. The register organization described in this document relate to an 'AT' compatible Winchester/Floppy Controller application. However, these registers are general purpose READ/WRITE registers and except for some hardware specific bits, can be defined to suit other applications. Decoding for an optional FLOPPY SELECT/CONTROL REGISTER and a FDC 765 FLOPPY DISK CONTROLLER is also available.

3.2 HOST REGISTER ASSIGNMENT

I/O ADDRESS PRIMARY(SECONDARY)	READ	WRITE
1F0(170)	DATA REGISTER	DATA REGISTER
1F1(171)	ERROR REGISTER	PRECOMPENSATION REGISTER
1F2(172)	SECTOR COUNT REGISTER	SECTOR COUNTR REGISTER
1F3(173)	SECTOR NUMBER REGISTER	SECTOR NUMBER REGISTER
1F4(174)	CYLINDER REGISTER (LSB)	CYLINDER REGISTER (LSB)
1F5(175)	CYLINDER REGISTER (MSB)	CYLINDER REGSITER (MSB)
1F6(176)	SDH REGISTER	SDH REGISTER
1F7(177)	STATUS REGISTER	COMMAND REGISTER
3F2(372)		FLOPPY SELECT/CONTROL
3F4(374)	FDC MAIN STATUS	
3F5(375)	FDC DATA	FDC DATA
3F6(376)	SECONDARY STATUS	CONTROL REGISTER
3F7(377)	HEAD/SELECT STATUS	FLOPPY RATE SELECT

TABLE 1 HOST REGISTER ASSIGNMENT

3.3 HOST READ REGISTER DESCRIPTION

3.3.1 DATA REGISTER 1F0(170)

This register transfers controller data between the 5098 and the HOST. In WORD MODE, 16 bits of data are transferred requiring $\overline{\text{IO_CS}}_{16}$ to be asserted and possibly de-asserting IO_CH_RDY . In BYTE MODE, 8 bits of data are transferred leaving $\overline{\text{IO_CS}}_{16}$ de-asserted and IO_CH_RDY asserted.

REV C:

The 5098C allows greater flexibility in controlling $\overline{\text{IO_CS}}_{16}$ and IO_CH_RDY . See Microprocessor Write Register FC Description 3.8.13 for programming these signals.

3.3.2 ERROR REGISTER 1F1(171)

This register contains the ERROR STATUS of the last command executed by the controller. It can only be accessed while the controller is in the NOT BUSY state. This register is not affected by RESET. The bit definitions are:

- BIT 7 - BAD BLOCK FOUND. This indicates that the specified track has previously been formatted with the BAD TRACK flag set in the ID field. It is not possible to access data on this track and the command will be terminated.
- BIT 6 - ECC ERROR. This indicates that a NON-ZERO syndrome was detected in a specified data field. If the data error was corrected by ECC, BIT 2 of the STATUS REGISTER will also be SET and the command will continue if more sectors are specified. If the data error was NOT corrected by ECC, BIT 0 of the STATUS REGISTER will be SET and the command terminated.
- BIT 5 - NOT USED. Set to zero.
- BIT 4 - ID NOT FOUND. This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector number. An ID CRC error can also generate this error condition.
- BIT 3 - NOT USED. Set to zero.
- BIT 2 - ABORTED COMMAND. The current command issued by the HOST has been aborted due to an undefined COMMAND OPCODE, or a WRITE FAULT/NOT READY condition exist on the selected drive.
- BIT 1 - NO CYLINDER ZERO. This indicates that during a RECALIBRATION command or if retries are enabled no CYLINDER 000 was detected. This error occurs after the controller issues 2048 step pulses towards cylinder 000 and the selected drive does not respond with the TRACK 000 signal.

BIT 0 - NO DATA MARK FOUND. This indicates that the controller was able to locate the sector but was unable to locate the data mark associated with it.

3.3.3 SECTOR COUNT REGISTER 1F2(172)

This register contains the number of sectors to be processed and is decremented as each sector is processed. It can only be accessed while the controller is in the NOT BUSY state. This register is set to 1 after a RESET.

3.3.4 SECTOR NUMBER REGISTER 1F3(173)

This register contains the current sector number being processed by the controller. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the sector number in error. It is set to 1 after a RESET.

3.3.5 CYLINDER (LSB) REGISTER 1F4(174)

This register contains the least significant byte of the current cylinder number. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the least significant byte of the cylinder number in error. This register is set to 0 after a RESET.

3.3.6 CYLINDER (MSB) REGISTER 1F5(175)

This register contains the most significant byte of the current cylinder number. It can only be accessed while the controller is in the NOT BUSY state. If an error condition exist, this register contains the most significant byte of the cylinder number in error. This register is set to 0 after a RESET.

3.3.7 SDH REGISTER 1F6(176)

This register contains the controller ERROR CODE/SECTOR SIZE parameters along with the current DRIVE/HEAD select. It can only be accessed while the controller is in the NOT BUSY state. This register is set to 0 after a RESET. The bit definitions are:

BIT 7 - ERROR CODE.	This bit indicates the error code selected. If this bit is set to '1', the data field will be appended with an ECC field. If set to '0', the data field will be appended with a CRC field.
---------------------	--

BITS 6, 5 - SECTOR SIZE.

These bits indicate the sector size selected. Their definitions are:

BIT	6	5	
	0	0	- 256 BYTE SECTOR
	0	1	- 512 BYTE SECTOR
	1	0	- 1024 BYTE SECTOR
	1	1	- 128 BYTE SECTOR

BIT 4 - DRIVE SELECT.

This bit reflects the selected drive. If this bit is set to '0', drive 0 is selected. If set to '1', drive 1 is selected.

BITS 3-0 - HEAD SELECT.

These bits indicate the selected head.

3.3.8 STATUS REGISTER 1F7(177)

This register contains the CONTROLLER/DRIVE STATUS. Reading this register de-asserts the INTRQ signal. The bit definitions are:

BIT 7 - BUSY.

This bit indicates the state of the controller. If SET, the controller is busy executing the specified command and is NOT in a DATA TRANSFER state. While set, the STATUS REGISTER is gated on the BUS during any READ to the HOST READ/WRITE REGISTERS. Any WRITE to the HOST READ/WRITE REGISTERS while this bit is set will be ignored. If CLEARED, the controller is either in a NOT BUSY or a DATA TRANSFER state. The DRQ bit will be SET if the controller is in the DATA TRANSFER state.

BIT 6 - READY.

This bit is an inverted copy of the "READY signal of the selected drive.

BIT 5 - WRITE FAULT.

This bit is an inverted copy of the "WRITE FAULT signal of the selected drive.

BIT 4 - SEEK COMPLETE.

This bit is an inverted copy of the "SEEK COMPLETE signal of the selected drive.

- BIT 3 - DATA REQUEST.** This bit indicates that the controller is in a DATA TRANSFER mode. While this bit is SET, the BUSY bit will be CLEARED and the controller will wait for data to be transferred to or from the HOST.
- BIT 2 - CORRECTED.** This bit indicates if a DATA ERROR was corrected. If SET, an ECC error occurred but was corrected. A corrected ECC error will NOT terminate a multiple sector transfer. If CRC is selected, this bit has no meaning and is set to '0'.
- BIT 1 - INDEX.** This bit is an inverted copy of the "INDEX" signal of the selected drive.
- BIT 0 - ERROR.** This bit indicates if an UNRECOVERABLE ERROR has occurred. If SET, an error condition exist and the STATUS REGISTER must be read to determine the error type.

3.3.9 FDC 765 MAIN STATUS REGISTER (OPTIONAL)

Reading this register selects the FDC 765 MAIN STATUS register (if available). For more information, consult the FDC 765 data sheet.

3.3.10 FDC 765 DATA REGISTER (OPTIONAL)

Reading this register selects the FDC 765 DATA register (if available). For more information, consult the FDC 765 data sheet.

3.3.11 SECONDARY STATUS REGISTER 3F6(376)

This register contains the CONTROLLER/DRIVE STATUS. It is identical to the STATUS REGISTER at address 1F7(177) except that reading this STATUS REGISTER has no effect on the INTRQ signal. See section 3.3.8 for bit definitions.

3.3.12 HEAD/SELECT STATUS REGISTER 3F7(377)

This register contains the HEAD/DRIVE SELECT STATUS. The bit definitions are:

- | | |
|-----------------------------|---|
| BIT 7 - "DISKETTE CHANGE. | This bit indicates the state of the floppy "DCHG signal. If SET, no diskette, door open or drive NOT READY condition exist. |
| BIT 6 - WRITE GATE. | This bit indicates the state of the winchester "WRITE GATE signal. |
| BIT 5 - "HEAD SELECT 3/RWC. | This bit indicates the state of HEAD SELECT 3/RWC. |
| BIT 4 - "HEAD SELECT 2. | This bit indicates the state of HEAD SELECT 2. |
| BIT 3 - "HEAD SELECT 1. | This bit indicates the state of HEAD SELECT 1. |
| BIT 2 - "HEAD SELECT 0. | This bit indicates the state of HEAD SELECT 0. |
| BIT 1 - "DRIVE SELECT 1. | This bit indicates the state of DRIVE SELECT 1. If set to '0', DRIVE 1 is selected. If set to '1', DRIVE 1 is de-selected. |
| BIT 0 - "DRIVE SELECT 0. | This bit indicates the state of DRIVE SELECT 0. If set to '0', DRIVE 0 is selected. If set to '1', DRIVE 0 is de-selected. |

3.4 HOST WRITE REGISTER DESCRIPTION

3.4.1 DATA REGISTER 1F0(170)

This register transfers controller data between the HOST and the 5098. In WORD MODE, 16 bits of data are transferred requiring "IO_CS_16 to be asserted and possibly de-asserting IO_CH_RDY. In BYTE MODE, 8 bits of data are transferred leaving "IO_CS_16 de-asserted and IO_CH_RDY asserted.

3.4.2 WRITE PRECOMPENSATION/RWC REGISTER 1F1(171)

This register determines the cylinder at which WRITE PRECOMPENSATION will be applied. The value written is 1/4 the actual precompensation cylinder. A value of 255 will result in no write precompensation/reduce write current. This register should be written prior to the COMMAND REGISTER being written with a WRITE/FORMAT command. It is set to 32 (128) after a RESET.

3.4.3 SECTOR COUNT REGISTER 1F2(172)

This register specifies the number of sectors to be processed. A value of 0 indicates 256 sectors. It should be written prior to the COMMAND REGISTER being written. This register is set to 1 after a RESET.

3.4.4 SECTOR NUMBER REGISTER 1F3(173)

This register specifies the starting sector number. It should be written prior to the COMMAND REGISTER being written. This register is set to 1 after a RESET.

3.4.5 CYLINDER (LSB) REGISTER 1F4(174)

This register specifies the least significant byte of the starting cylinder number. It should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET.

3.4.6 CYLINDER (MSB) REGISTER 1F5(175)

This register specifies the most significant byte of the starting cylinder number. It should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET.

3.4.7 SDH REGISTER 1F6(176)

This register specifies the controller ERROR CODE/SECTOR SIZE parameters along with the DRIVE/HEAD select. This register should be written prior to the COMMAND REGISTER being written. This register is set to 0 after a RESET. The bit definitions are:

BIT 7 - ERROR CODE.

This bit specifies the error code to be selected. If this bit is SET the data field will be appended with an ECC field. If CLEARED, the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE.

These bits specify the sector size to be selected. The sector size definitions are:

BIT	6	5	
	0	0	- 256 BYTE SECTOR
	0	1	- 512 BYTE SECTOR
	1	0	- 1024 BYTE SECTOR
	1	1	- 128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit selects the drive. If this bit is set to '0', drive 0 is selected. If set to '1', drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits select the head.

3.4.8 COMMAND REGISTER 1F7(177)

This register specifies the command to be executed by the controller. It is set to 0 after a RESET. Writing to this register asserts the COMMAND signal.

3.4.9 FLOPPY SELECT/CONTROL REGISTER 3F2(372), OPTIONAL

Writing this register selects the floppy select/control register (if available). This register is external to the OMTI 5098 and is selected by the FDD_REG signal.

3.4.10 FDC 765 DATA REGISTER 3F5(375), OPTIONAL

Writing this register selects the FDC 765 DATA register (if available). For more information, consult the FDC 765 data sheet.

3.4.11 HOST CONTROL REGISTER 3F6(376)

This register allows the HOST to reset the 5098 and enable/disable the INTRQ signal. The bit definitions are:

BIT 2 - RESET. Writing a '1' to this bit places the 5098 in the BUSY state and resets all internal registers to their reset value. A '0' must be written to this bit for normal operation.

BIT 1 - INTRQ ENABLE. Writing a '0' to this bit enables the 5098 INTRQ signal. Writing a '0' to this bit disables (tri-states) the INTRQ signal. Pending interrupts are not affected by tri-stating this signal.

REV C:

This register has been expanded to include a DMA enable/disable function for HOST systems using the 5098C DMA MODE. The bit definition is:

BIT 4 - DMA ENABLE.

If the 5098C is configured in the DMA mode and BIT(2) of MICROCOMPUTER WRITE REGISTER FE is set to '1', writing a '1' to this bit will enable the DREQ signal. Writing a '0' to this bit will disable (tri-state) the DREQ signal. If the 5098C is not configured in the DMA mode or BIT(2) of MICROCOMPUTER WRITE REGISTER is '0' then this bit has no meaning.

3.4.12 FLOPPY DATA RATE SELECT REGISTER 3F7(377), OPTIONAL

This 2 bit register (BITS 1, 0), select the FLOPPY DATA SEPERATOR DATA RATE. These bits are output on RATE_1 and RATE_0 respectively.

3.5 CONTROLLER READ/WRITE REGISTERS

The OMTI 5098 contains 8 registers by which the microcomputer can communicate with the HOST and 4 WRITE ONLY registers which control the internal/external special functions.

REV C:

The 5098C contains an additional 4 WRITE ONLY registers which configure the added features.

3.6 MICROCOMPUTER REGISTER ASSIGNMENT

ADDRESS	READ	WRITE
F0	INTRQ STATUS REGISTER	HEAD SELECT REGISTER
F1	PRECOMPENSATION REGISTER	ERROR REGISTER
F2	SECTOR COUNT REGISTER	SECTOR COUNT REGISTER
F3	SECTOR NUMBER REGISTER	SECTOR NUMBER REGISTER
F4	CYLINDER REGISTER (LSB)	CYLINDER REGISTER (LSB)
F5	CYLINDER REGISTER (MSB)	CYLINDER REGISTER (MSB)
F6	SDH REGISTER	SDH REGISTER
F7	COMMAND REGISTER	STATUS REGISTER
F8		INTERNAL CONTROL REGISTER
F9		DRIVE CONTROL REGISTER
FA		BUSY CONTROL REGISTER
FB		5098 IDENTIFIER REGISTER

REV C ONLY

FC	ADDITIONAL CONTROL REGISTER
FD	ADDITIONAL CONTROL REGISTER
FE	ADDITIONAL CONTROL REGISTER
FF	ADDITIONAL CONTROL REGISTER

TABLE 2 MICROCOMPUTER REGISTER ASSIGNMENT

3.7 MICROCOMPUTER READ REGISTER DESCRIPTION

3.7.1 INTRQ STATUS REGISTER F0

This one bit register (BIT 0 ONLY) contains the status of the INTRQ bit. If this bit is SET, INTRQ is asserted. If CLEARED, INTRQ is de-asserted.

REV C:

This register has been expanded to include drive and command interface status. The bit definitions are:

BIT 7-5 CONFIGURATION.

These three inputs come from the HOST ADDRESS BUS BITS(7,6,5). They can only be used as configuration jumpers when the 5098C is in the "CS_SEL MODE. BIT(7) is an inverted copy of the A_(7) input, while BIT(5) is an inverted copy of the A_(5) input.

BIT 4 - PASS DIAGNOSTICS.

If the 5098C is in the MASTER MODE, this bit is an inverted copy of the "DS_1 input. It is generally used to determine if a SLAVE drive has passed the diagnostic command.

BIT 3 - SLAVE PRESENT.

If the 5098C is in the MASTER MODE, this bit is an inverted copy of the "COMMAND input. It is generally used to determine if a SLAVE drive is present during a diagnostic command.

BIT 2 - COMMAND.

This bit is an inverted copy of the "COMMAND output signal. When this status bit is set to '1', a write to HOST WRITE REGISTER 1F7(177) has occurred. This bit is set to '0' by writing the INTERNAL CONTROL REGISTER bit 2 with a '1' or a RESET.

BIT 1 - READY.

This bit is an inverted copy of the external "READY input signal. When this status bit is set to '1', the selected drive is ready. When set to '0' the selected drive is NOT ready.

3.7.2 WRITE PRECOMPENSATION REGISTER F1

This register contains the cylinder at which WRITE PRECOMPENSATION will be applied. The value read must be multiplied by 4. A value of 255 will result in no write precompensation/reduce write current. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.3 SECTOR COUNT REGISTER F2

This register contains the number of sectors to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.4 SECTOR NUMBER REGISTER F3

This register contains the starting sector number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.5 CYLINDER (LSB) REGISTER F4

This register contains the starting (least significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.6 CYLINDER (MSB) REGISTER F5

This register contains the starting (most significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST).

3.7.7 SDH REGISTER F6

This register contains the controller ERROR CODE/SECTOR SIZE parameters along with the current DRIVE/HEAD select. It is read by the controller processor only after a command has been written into the COMMAND REGISTER (HOST). The bit definitions are:

BIT 7 - ERROR CODE. This bit specifies the error code to be used. If this bit is set to '1', the data field will be appended with an ECC field. If set to '0', the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits specify the sector size to be used. The sector size definitions are:

BIT 6 5
0 0 - 256 BYTE SECTOR
0 1 - 512 BYTE SECTOR
1 0 - 1024 BYTE SECTOR
1 1 - 128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit specifies the drive to be selected. If this bit is set to '0', drive 0 is selected. If set to '1', drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits specify the head to be selected.

3.7.8 COMMAND REGISTER F7

This register contains the command to be executed by the controller. It is read only after the "COMMAND signal has been asserted.

3.8 MICROCOMPUTER WRITE REGISTER DESCRIPTION

3.8.1 HEAD SELECT REGISTER F0

This registers upper nibble (BITS 7,6,5,4) is written with the current head select (BIT 7 - HEAD 2³, BIT 4 - HEAD 2⁰) during head changes on multiple sector reads or writes. BIT 0 of this register enables or disables the 5098 identifier register. If a '1' is written to this bit, the identifier register will be accessed at HOST READ ADDRESS 3F1(371). If a '0' is written, the register is disabled.

3.8.2 ERROR REGISTER F1

This register is written with ERROR STATUS of the last command executed.

REV C: The 5098C will clear this register to '0' when the HOST writes to REGISTER 1F7(177). The bit definitions are:

BIT 7 - BAD BLOCK FOUND. This indicates that the specified track has previously been formatted with the BAD TRACK flag set in the ID field. It is not possible to access data on this track and the command will be terminated.

BIT 6 - ECC ERROR. This indicates that a NON-ZERO syndrome was detected in a specified data field. If the data error was corrected by ECC, BIT 2 of the STATUS REGISTER will also be SET and the command will continue if more sectors are specified. If the data error was NOT corrected by ECC, BIT 0 of the STATUS REGISTER will be SET and the command terminated.

BIT 5 - NOT USED. Set to zero.

BIT 4 - ID NOT FOUND. This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector number. An ID CRC error can also generate this error condition.

- BIT 3 - NOT USED. Set to zero.
- BIT 2 - ABORTED COMMAND. The current command issued by the HOST has been aborted due to an undefined COMMAND OP CODE, or a WRITE FAULT/NOT READY condition exist on the selected drive.
- BIT 1 - NO CYLINDER ZERO. This indicates that during a RECALIBRATION command or if retries are enabled no CYLINDER 000 was detected. This error occurs after the controller issues 2048 step pulses towards cylinder 000 and the selected drive does not respond with the TRACK 000 signal.
- BIT 0 - NO DATA MARK FOUND. This indicates that the controller was able to locate the sector but was unable to locate the data mark associated with it.

3.8.3 SECTOR COUNT REGISTER F2

This register is written with the number of sectors processed. It is read by the host only after a command has been executed by the controller.

3.8.4 SECTOR NUMBER REGISTER F3

This register is written with the sector number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.5 CYLINDER (LSB) REGISTER F4

This register is written with the cylinder LSB number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.6 CYLINDER (MSB) REGISTER F5

This register is written with the cylinder MSB number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

3.8.7 SDH REGISTER F6

This register is written with the size/drive/head number that has an error by the controller. It is read by the host only after a command has been executed by the controller. The bit definitions are:

BIT 7 - ERROR CODE. This bit indicates the error code selected. If this bit is set to '1', the data field will be appended with an ECC field. If set to '0', the data field will be appended with a CRC field.

BITS 6, 5 - SECTOR SIZE. These bits indicate the sector size selected. Their definitions are:

BIT 6 5
0 0 - 256 BYTE SECTOR
0 1 - 512 BYTE SECTOR
1 0 - 1024 BYTE SECTOR
1 1 - 128 BYTE SECTOR

BIT 4 - DRIVE SELECT. This bit reflects the selected drive. If this bit is set to '0', drive 0 is selected. If set to '1', drive 1 is selected.

BITS 3-0 - HEAD SELECT. These bits indicate the selected head.

3.8.8 STATUS REGISTER F7

This register is written with the status by the controller. It is read by the host only after a command has been executed by the controller. The bit definitions are:

BIT 2 - CORRECTABLE. Writing a '1' to this bit sets BIT 2 of HOST READ REGISTER 1F7(177). It is set to indicate that ECC was applied to a data field. Writing a '0' to this bit will clear BIT 2 of HOST WRITE REGISTER 1F7(177).

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177).

BIT 0 - ERROR. Writing a '1' to this bit sets BIT 0 of HOST READ REGISTER 1F7(177). It is set to indicate that an error has occurred. Writing a '0' to this bit will clear BIT 2 of HOST WRITE REGISTER 1F7(177).

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177).

3.8.9 INTERNAL CONTROL REGISTER F8

This register is written by the controller and is used to control of the internal operations of the 5098. This register is set to 0 after a RESET. The bit definitions are:

- BIT 7 - DMA_BUSY. This bit controls if DMA_INTRQ will cause BUSY status. Writing a '1' to this bit will enable DMA_INTRQ to cause the 5098 BUSY status. Writing a '0' will disable the DMA_INTRQ signal. Disabling DMA_INTRQ will not affect the BUSY state.
- BIT 6 - SELECT. This bit controls the \overline{DS}_0 or \overline{DS}_1 output enable. If the DIS_SELECT (BIT 5) is not set, this bit has no meaning. Writing a '1' to this bit will enable the drive select signals. Writing a '0' will disable them.
- BIT 5 - DIS_SELECT. This bit enables or disables the drive select function. Writing a '1' to this bit will enable the drive select function. This causes the drive to be selected only during STATUS reads or the SELECT bit is set. Writing a '0' to this bit disables the drive select function leaving the drive select signals active at all times.
- BIT 4 - DIS_MSB. This bit enables or disables the most significant bit (MSB) of HOST REGISTER 3F7(377) during reads. Writing a '1' to this bit disables (tri-states) BIT 7 of HOST REGISTER 3F7(377). Writing a '0' enables (drives) it.
- BIT 3 - DIS_WORD. This bit enables or disables word (16 bit) data transfers. Writing a '1' to this bit enables word data transfers during read or writes to HOST REGISTER 1F0(170). While in WORD MODE, the $\overline{IO_CS}_{16}$ and IO_CH_RDY signal are enabled. Writing a '0' causes byte (8 bit) data transfers during read or writes to HOST REGISTER 1F0(170). In this case, the $\overline{IO_CS}_{16}$ and IO_CH_RDY signals are disabled.

REV C: This bit has no effect on the $\overline{\text{IO_CS}}_{16}$ or ID_CH_RDY signals. See MICROCOMPUTER WRITE REGISTER FC for the control of these signals.

BIT 2 - COMMAND

This bit is used to reset the $\overline{\text{COMMAND}}$ signal. Writing a '1' to this bit deasserts the $\overline{\text{COMMAND}}$ signal. Writing a '0' leaves the $\overline{\text{COMMAND}}$ signal in its current state.

BIT 1 - BUSY

This bit is used to set or reset the 5098 BUSY STATUS. Writing a '1' to this bit will set the BUSY STATUS. Writing a '0' will clear it.

BIT 0 - INTERRUPT

This bit is used to set or reset the INTRQ signal. Writing a '1' to this bit will set the INTRQ signal. Writing a '0' will clear it.

REV C: Writing a 0 to this bit has no effect on the INTRQ signal.

3.8.10 DRIVE STATUS CONTROL REGISTER F9

This register is written by the controller and is used to control both the 5098 and the drive status. The bit definitions are:

BIT 7 - POLARITY.

This bit specifies the polarity of the DMA_INTRQ input. Writing a '1' to this bit causes (if enabled) the 5098 BUSY STATUS to be set when DMA_INTRQ is a '1'. Writing a '0' causes BUSY STATUS when DMA_INTRQ is a '0'.

BITS 6 - DIS_BUSY.

This bit enables or disables the 5098 BUSY STATUS on HOST writes to REGISTER 1F7(177). Writing a '1' to this bit disables BUSY. Writing a '0' enables BUSY.

BIT 5 - NOT_RDY_1.

This bit allows the controller to override the "READY signal for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate DRIVE NOT READY status for drive select 1 regardless of the "READY signal. Writing a '0' will allow the "READY signal to indicate DRIVE NOT READY STATUS.

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '1'.

BIT 4 - WF_1.

This bit specifies the WRITE_FAULT status for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate WRITE FAULT status. Writing a '0' will signal no WRITE FAULT.

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '1'.

BIT 3 - SC_1.

This bit specifies the SEEK COMPLETE status for drive select 1. Writing a '1' to this bit will cause the 5098 to indicate SEEK COMPLETE status. Writing a '0' will indicate NO SEEK COMPLETE status.

REV C: The 5098C will set this bit to '1' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '1'.

BIT 2 - NOT_RDY_0.

This bit allows the controller to override the "READY signal for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate DRIVE NOT READY status for drive select 0 regardless of the "READY signal. Writing a '0' will allow the "READY signal to indicate DRIVE NOT READY STATUS.

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '0'.

BIT 1 - WF_0.

This bit specifies the WRITE_FAULT status for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate WRITE_FAULT status. Writing a '0' will signal no WRITE_FAULT.

REV C: The 5098C will clear this bit to '0' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '0'.

BIT 0 - SC_0.

This bit specifies the SEEK COMPLETE status for drive select 0. Writing a '1' to this bit will cause the 5098 to indicate SEEK COMPLETE status. Writing a '0' will indicate NO SEEK COMPLETE status.

REV C: The 5098C will set this bit to '1' when the HOST writes to REGISTER 1F7(177) if BIT 4 of HOST WRITE REGISTER 1F6(176) is a '0'.

3.8.11 BUSY COMMAND COMPARATOR REGISTER FA

This register is written by the controller and is used to allow for two commands that will not cause the 5098 to indicate BUSY status. It is organized into two nibbles. Bits 7,6,5,4 represent the first command, bits 3,2,1,0 represent the second. These nibbles correspond to bits 7,6,5,4 of HOST REGISTER 1F7(177). This register must be initialize prior to writing a command to the 5098.

3.8.12 5098 IDENTIFIER REGISTER FB

This register is written by the controller and is used to specify the controller type. It is accessed by the HOST (if enabled, see section 3.8.1) by reading HOST REGISTER 3F1(371).

3.8.13 ADDITIONAL CONTROL REGISTER FC (REV C ONLY)

This register allows extended control over the drive READY status and output signals IO_CH_RDY and IO_CS_16. It also controls DMA transfers between the CONTROLLER DMA and the 5098C. It is set to '0' at POWER-ON RESET or writing BIT(2) of HOST WRITE REGISTER 3F6(376) with a '1'. The bit definitions are:

BIT 7 - ENABLE DATA.

This bit, in conjunction with BIT(0) of MICROCOMPUTER WRITE REGISTER FD, enables data transfers between the 5098C and the CONTROLLER DMA. Writing a '1' to this bit will enable the 5098C to issue DMA requests to the CONTROLLER DMA. When the internal FIFO has 1 byte or word, the DRQ bit will be set in the HOST STATUS REGISTER. At the end of the transfer count, this bit will automatically be reset. Writing a '1' to this bit if BIT(0) of MICROCOMPUTER WRITE REGISTER FD is not set, improper operation will occur.

BIT 6 - DIRECTION.

This bit determines the direction of data transfers between the CONTROLLER DMA and the 5098C. Writing a '1' to this bit will transfer data from the CONTROLLER DMA RAM to the 5098C FIFO. Writing a '0' to this bit will transfer data from the 5098C FIFO to the CONTROLLER DMA RAM.

BIT 5 - INTRQ ENABLE.

This bit determines the tri-state function of the INTRQ signal. Writing a '1' to this bit will cause the INTRQ signal to be active only during command execution. The INTRQ signal will tri-state after the last STATUS READ of the command. An internal 200 micro-amp pull-down keeps the INTRQ signal from floating (if enabled) while in tri-state. If BIT(1) of HOST WRITE REGISTER 3F6(376) is set to '1', the INTRQ signal will be disabled irregardless of the state of this bit. Writing a '0' to this bit will cause the INTRQ signal to operate in the normal mode determined by BIT(1) of HOST WRITE REGISTER 3F6(376).

BITS 4-3 SYS CLOCKS.

These bits define the number of system clocks used to hold IO_CH_RDY de-asserted after the assertion of ~IO_CS_16. They are set to zero clocks (00) on RESET. The clocks are defined as:

BIT 4 3
0 0 - zero clocks (disabled)
0 1 - two clocks
1 0 - three clocks
1 1 - four clocks

BIT 2 - READY STATUS

This bit selects the origin of the drive ready status. It is set to '0' on RESET. Writing a '0' to this bit will cause the 5098 to operate in the REV B mode. Writing a '1' to this bit selects ready status from the internal register F9 bit 5 (drive 1) or bit 2 (drive 0). In this case, writing a '1' to bit 2 of internal register F9 will cause drive 0 to signal NOT READY status irrespective of the $\overline{\text{READY}}$ input signal. Writing a '0' to bit 2 of internal register F9 will cause drive 0 to signal READY status irrespective of the $\overline{\text{READY}}$ signal.

BIT 1 - DISABLE I/O READY.

This bit enables or disables the de-assertion of the IO_CH_RDY signal. Writing a '0' to this bit will enable the IO_CH_RDY logic. Writing a '1' to this bit will disable the IO_CH_RDY logic. In this case, the 5098C will not de-assert IO_CH_RDY even if data is NOT available. Use caution when disabling IO_CH_RDY.

BIT 0 - DISABLE $\overline{\text{IO_CS_16}}$.

This bit enables or disables the assertion of the $\overline{\text{IO_CS_16}}$ signal. Writing a '0' to this bit will enable the IO_CS_16 logic. Writing a '1' to this bit will disable the IO_CS_16 logic. In this case, the 5098C will not de-assert IO_CS_16 even if 16 bit data transfers are required. Use caution when disabling IO_CS_16.

3.8.14 ADDITIONAL CONTROL REGISTER FD (REV C ONLY)

This register programs the NORMAL/DMA REQ-ACK MODE, ECC MODE, and the AUTOMATIC MODE of the 5098C. It is set to '0' at POWER-ON RESET or writing BIT 2 of HOST WRITE REGISTER 3F6(376) with a '1'. The bit definitions are:

BIT 7 - WAIT MODE. Writing a '1' to this bit will cause the 5098C to wait for the HOST to read the STATUS REGISTER 1F7(177) before starting another data phase. Writing a '0' to this bit causes the 5098C to NOT wait for a STATUS READ. In this case, the MICROCOMPUTER should wait for the read.

BIT 6 - COMMAND = DMA_INTRQ. Writing a '1' to this bit will cause the 5098C to place the DMA_INTRQ signal at the COMMAND signal. In this case, the DMA_INTRQ signal will be TRI-STATED. Writing a '0' to this bit will leave the COMMAND signal and the DMA_INTRQ signal at their normal pins.

BIT 5 - ENABLE ECC TRANSFER. Writing a '1' to this bit will cause the 5098C to enable ECC transfer. In this mode, 8 bit transfers are selected. At the end of the transfer, this bit will be cleared to '0'.

BITS 4-3 ECC TRANSFER COUNT. These bits define the number of ECC bytes to transfer. The counts are defined as:

BIT	4	3	
	0	0	- two bytes (CRC)
	0	1	- four bytes
	1	0	- six bytes
	1	1	- eight bytes

BIT 2 - AUTO BUSY/INTRQ. Writing a '1' to this bit will cause the 5098C to automatically set INTRQ and clear BUSY when data is ready to be transferred to or from the HOST. Writing a '0' to this bit will leave this function to the MICROCOMPUTER.

BIT 1 - LEVEL DMA_REQ.

This bit in conjunction with BIT 0 programs the DMA_REQ MODE. Writing a '1' to this bit will cause the 5098C to assert DMA_REQ as long as the FIFO has data (WRITE) or is empty (READ). Writing a '0' to this bit causes DMA_REQ signal to be asserted and de-asserted for each byte transferred.

BIT 0 - DMA REQ/ACK.

This bit in conjunction with BIT 1 programs the DMA REQ/ACK MODE. Writing a '1' to this bit will cause the 5098C issue requests to the DMA CONTROLLER. In this case, the FIFO is used. Writing a '0' to this bit causes the 5098C to use the "OUTCLK"/"INENA signals to transfer data between the 5098C and the DMA CONTROLLER. BIT 1 has no meaning if this bit is '0'.

3.8.15 ADDITIONAL CONTROL REGISTER FE (REV C ONLY)

This register programs the MASTER/SLAVE, DMA MODE. It is set to '0' at POWER-ON RESET or writing BIT 2 of HOST WRITE REGISTER 3F6(376) with a '1'. The bit definitions are:

BIT 7 - IO_CS_16/IO_CH_RDY.

Writing a '1' to this bit will cause the 5098C to use BITS(1,0) of MICROCOMPUTER WRITE REGISTER FC to enable/disable the IO_CS_16 and IO_CH_RDY signals. Writing a '0' to this bit causes these signals to be programmed by BIT 3 of MICROCOMPUTER WRITE REGISTER FB.

BIT 6 - ENABLE PULL-DOWN.

Writing a '1' to this bit will cause the 5098C to enable a 200 microamp pull-down on the INTRQ signal. Writing a '0' to this bit will disable the pull-down.

BIT 5 - SLAVE.

Writing a '1' to this bit will cause the 5098C to be a SLAVE CONTROLLER. A SLAVE is only selected when BIT 4 of HOST WRITE REGISTER 1F6(176) is a '1'. Writing a '0' to this bit causes the 5098C to be a MASTER. A MASTER is only selected when BIT 4 of HOST WRITE REGISTER 1F6(176) is a '0'.

BIT 4 - MASTER/SLAVE MODE. Writing a '1' to this bit will cause the 5098C to enter the MASTER/SLAVE MODE. Writing a '0' to this bit causes the NORMAL operating mode. In this case, BIT 6 has no meaning.

BIT 3 - DRIVE RD/DREQ. Writing a '1' to this bit will cause the 5098C drive the RD/DREQ signal. Writing a '0' to this bit will TRI-STATE the RD/DREQ signal until READ MODE is selected or the HOST writes BIT 4 of REGISTER 3F6(376) with a '1'.

BIT 2 - ENABLE HOST DRIVE RD/DREQ. Writing a '1' to this bit will allow the HOST to enable the RD/DREQ signal. Writing a '0' to this signal disables the HOST'S access to enable/tri-state the RD/DREQ signal.

BITS 1-0 DMA MODE. These bits define the DMA MODE. The DMA MODES are defined as:

BIT 1 0
0 0 - DMA, DEMAND
0 1 - DMA, SINGLE/BLOCK
1 0 - DMA, SINGLE
1 1 - READ MODE

The DMA MODE defined is recommended when using a 8237 DMA CONTROLLER or equivalent. In the READ MODE, the RD/DREQ signal operates as defined in SECTION 2.

BIT 2 - AUTO BUSY/INTRQ. Writing a '1' to this bit will cause the 5098C to automatically set INTRQ and clear BUSY when data is ready to be transferred to or from the HOST. Writing a '0' to this bit will leave this function to the MICROCOMPUTER.

BIT 1 - LEVEL DMA_REQ. This bit in conjunction with BIT 0 programs the DMA_REQ MODE. Writing a '1' to this bit will cause the 5098C to assert DMA_REQ as long as the FIFO has data (WRITE) or is empty (READ). Writing a '0' to this bit causes DMA_REQ signal to be asserted and de-asserted for each byte transferred.

BIT 0 - DMA REQ/ACK.

This bit in conjunction with BIT 1 programs the DMA REQ/ACK MODE. Writing a '1' to this bit will cause the 5098C issue requests to the DMA CONTROLLER. In this case, the FIFO is used. Writing a '0' to this bit causes the 5098C to use the "OUTCLK/"INENA signals to transfer data between the 5098C and the DMA CONTROLLER. BIT 1 has no meaning if this bit is '0'.