OMTI 5070
ENCODE/DECODE CHIP
REFERENCE MANUAL
MAY 1984

Scientific Micro Systems, Inc.

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The OMTI PFM 5070 VCO/Encode/Decode chip provides all of the necessary functions needed to convert disk drives with MFM serial data interfaces (i.e., ST506/412, SA1000) to NRZ data and clock. It contains an internal voltage controlled oscillator, phase-locked loop, encode/decode logic, Address Mark generation and detection, and all the circuitry required for write precompensation.

The PFM 5070 is capable of operation at data rates up to 10 megabits per second by proper selection of the external frequency and loop gain components. The need for delay lines is eliminated by selecting write precompensation values with a constant current controlled RC network.

1.2 5070 VCO/ENCODE/DECODE CHIP CAPABILITIES

* Data rate control to 10 megabits per second
* No external logic required
* Internal VCO and phase-locked loop
* MFM to NRZ and NRZ to MFM conversion
* Internal address mark detection and generation circuitry
* Externally controlled write precompensation
* Internal early, on time, and late timing
* Control for external filter/varactor
* 24-pin plastic package

1.3 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the PFM 5070 VCO/Encode Decode chip. Each logic block is discussed in the following sections.

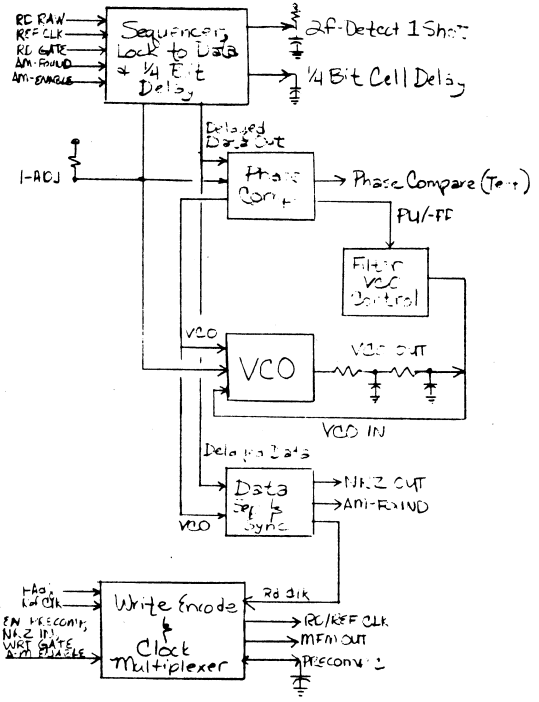


Figure 1. Internal Block Diagram

1.3.1 Sequencer, Lock to Data and 1/4-Bit Delay

This block delays the raw data from the disk by 1/4-bit cell time in preparation for use by the Phase Comparator. It also provides the A-M FOUND signal to the Data Sequencer, which allows it to lock on the data. Figure 2 contains a flow chart describing the Search Sync mode and AM Detect operations performed by this block.

1.3.2 Phase Comparator

The Phase Comparator compares the phase and frequency of the incoming signal with the VCO frequency, and generates an error voltage that is related to the phase and frequency difference between the two signals. The PU/-PD (Pump-Up/Pump-Down) signal communicates the result of the comparison to the VCO via the Filter VCO Control.

1.3.3 Filter VCO Control

The Filter VCO Control attenuates the high-frequency error components of the PU/-PD and inputs the corrected signal to the VCO (via the VCO IN line).

1.3.4 VCO

The Voltage Controlled Oscillator is a voltage to frequency converter used to provide a clock which is at the same frequency and phase as the raw data. The clock's frequency is determined by the PU/-PD signal.

1.3.5 Data Separator and Synchronization

The Data Separator and Synchronization block generates the NRZ output from the delayed data and the clock generated by the VCO.

1.3.6 Write Encode and Clock Multiplexer

This block converts NRZ data (from the Data Sequencer) into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal can then be used to record information on the disk. When AM-ENABLE is active, a clock pulse will be deleted in the outgoing MFM stream in order to record Address Marks on the disk. In addition, precompensation signals are generated, when needed, for use in recording inner tracks.

SEQUENCE AFTER RD GATE TRUE EDGE:

1. Wait for 8 read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
2. Set lock to data: disable VCO for 2 read raw pulses and start VCO in phase with read raw.
3. Wait for 24 more read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
4. Set Search Address Mark and output VCO/2 to RD/REF clock. Wait for a "1" or 96 more read raw pulses. If no "1", restart sequence.
5. If "1" is detected, Adress Mark Found and lock up or 12 raw read pulses and restart sequence.

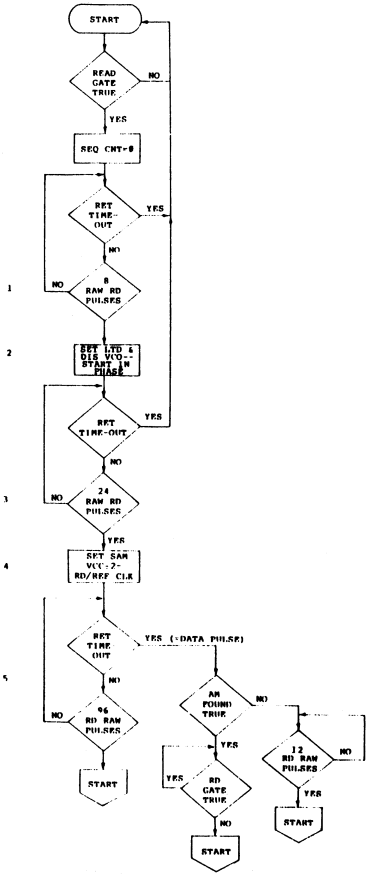


Figure 2. Flow Chart of Search Sync Mode

1.4 SYSTEM CONFIGURATION

Illustrated below is a typical system configuration, incorporating the VCO/Encode/Decode chip, the 5050 Data Sequencer, and the 5060 Memory Controller. Figure 4 shows all the external RC circuitry for a standard 5 MHz interface.

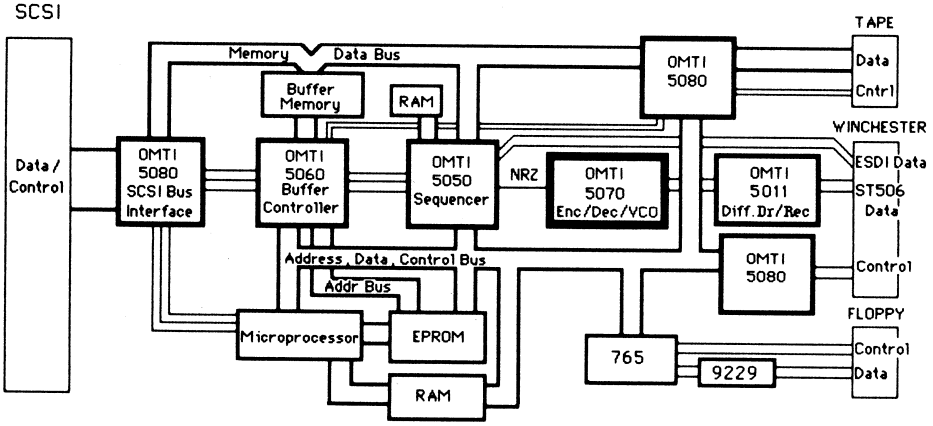


Figure 3. Typical System Configuration

1.4.1 Disk Interface

The disk interface consists of the MFM OUT line containing MFM-encoded data written to the disk, and the RD RAW line containing the MFM-encoded data to be translated to NRZ and input to the Data Sequencer.

1.4.2 Data Sequencer Interface

Three pairs of lines connect the 5070 with the 5050 Data Sequencer. These lines serve to transmit NRZ serial data between the two chips, enable the encoding and decoding of Address Marks, and provide various clock pulses to coordinate the data transfer.

1.4.3 Microprocessor Interface

The ENPRECOMP signal from the microprocessor enables precompensation for write operations on inner disk tracks.

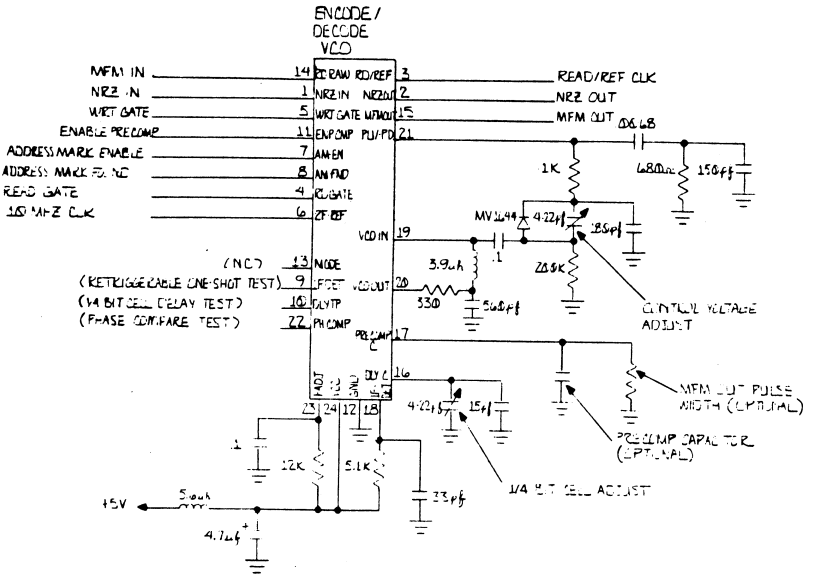


Figure 4. VCO Encode/Decode External RC Circuitry

CHAPTER 2

INTERFACING

2.1 SIGNAL DESCRIPTIONS

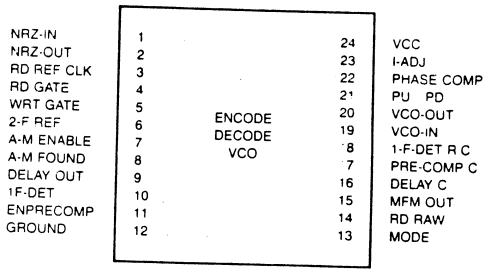


Figure 5. Pin Assignments

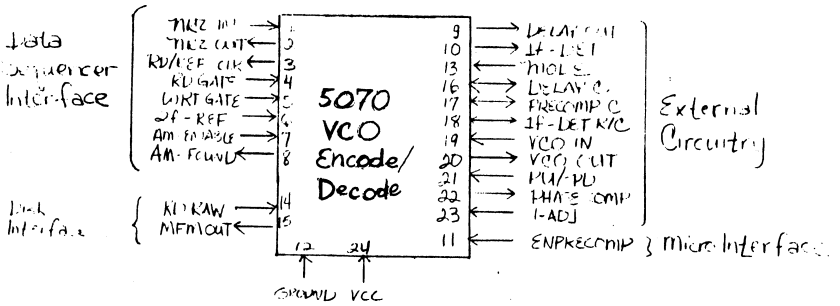


Figure 6. Pin Functions

Table 1. Pin Descriptions

Symbol	Type	Pin #	Name and Function
1-F DET	O	10	1-f Detect. (Active High.) This test output is used to calibrate the retriggerable One-Shot RC used for the Preamble detect circuit.
1-F DET RC	I/O	18	1-f Detect Connect RC. (Active High.) This I/O line is connected to the junction point between a resistor to VCC and a capacitor to GND. This circuit is used for the retriggerable One-Shot that detects the 1-f used for VCO sync in the Preamble.
2-F REF	I	6	2-f Reference Clock. (Active High.) When RD GATE is false, this signal is divided by 2 and output on the RD/REF clock line.
A-M ENABLE	I	7	Address Mark Enable. (Active High.) When both this signal and WRT GATE are active, A-M ENABLE encodes an Address Mark (a special byte with a missing clock pulse). When A-M ENABLE is true and RD GATE is active, the Data Sequencer is locked from resyncing, thus placing the sequencer in external sync detect mode.
A-M FOUND	O	8	Address Mark Found. (Active High.) This output line goes High after RD GATE goes High and the missing clock pattern of the Address Mark is detected. The Data Sequencer uses this signal for byte synchronization during Read operations.
DELAY C	I/O	16	Delay Cell. (Active High.) This I/O pin is connected to a variable capacitor used to generate the 1/4-bit cell delay.
DELAY OUT	O	9	Delay Output. (Active High.) This test output is used to calibrate the One-Shot RC used for the 1/4-bit cell delay circuit.
ENPRECOMP	I	11	Enable Precompensation. (Active High.) When active, this signal enables precompensation for disk write operations on inner tracks. When this signal is inactive, write precompensation is disabled.

Table 1. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
I-ADJ	I	23	Input Adjust. (Active High.) This input provides the current reference for all constant current controlled elements of the chip, i.e. phase comparator, PU/-PD signal, 1/4 bit cell delay, and write precompensation circuitry. An external fixed resistor from 5 V connected to this pin determines the constant current value.
MFM OUT	O	15	MFM Write Data. (Active High.) This signal is the MFM-encoded data output when WR GATE is active.
MODE	I	13	Mode Enable. (Active High.) When Low, this signal enables the VCO lock sequencer to lock to data after 1 clock of 2-f, and also sets Search Address Mode after 8, rather than 32, clock cycles.
NRZ IN	I	1	NRZ Serial Input. (Active High.) This serial data input line is the output from the Data Sequencer. This input must be at the data rate of the read/reference clock.
NRZ OUT	O	2	NRZ Serial Output. (Active High.) This signal is the serial output to the Data Sequencer. This signal must be at the data rate of the read/reference clock.
PHASE COMP	O	22	Phase Compare. (Active High.) This output is used for calibration of the 1/4-bit cell delay.
PRECOMP C	I/O	17	Precomp Capacitor. (Active High.) This I/O line is connected to an external capacitor used to generate the write precompensation delay time when precompensation is enabled.
PU/-PD	I	21	Filter Source/-Sink. (Filter Source active High; -Sink active Low; 3-state.) This 3-state output will be enabled High when the phase comparator requires a VCO increase in frequency, and will be enabled Low when the phase comparator requires a VCO decrease in frequency. The active High or Low current source/sink is proportional to the I-ADJ signal.

Table 1. Pin Descriptions, continued

Symbol	Type	Pin #	Name and Function
RD GATE	I	4	Read Gate. (Active High.) The transition of this signal from Low to High configures the chip in Search Sync mode (see Figure 4). During the Search for Address Mark phase of the Search Sync mode (VCO is locked), this signal selects the VCO clock/2 to be present at the RD/REFCLK line.
RD RAW	I	14	Read Raw Data. (Active High.) This input is the raw data containing both clock and data pulses output from the disk drive.
RD/REFCLK	O	3	Read/Reference Clock. (Active High.) This multiplexed output is used by the Data Sequencer for both read and write clock. The 2-f reference clock/2 will be present at this line when RD GATE is false. When RD GATE is true during the Search for Address Mark phase (VCO is locked), the VCO clock/2 will be present at this line.
VCO IN	I	19	VCO Input. (Active High.) This signal is the output of the VCO controlled by the charge-pump delay of the VCO output.
VCO OUT	O	20	VCO Output. (Active High.) This signal is used for the VCO source with the delay controlled by the charge-pump, and feed-back in the VCO input.
WRT GATE	I	5	Write Gate. (Active High.) When active, this signal enables encoding of NRZ serial data to MFM encoded data.
VCC	I	24	VCC. +5 V.
GND	I	12	Ground.

2.2 TIMING

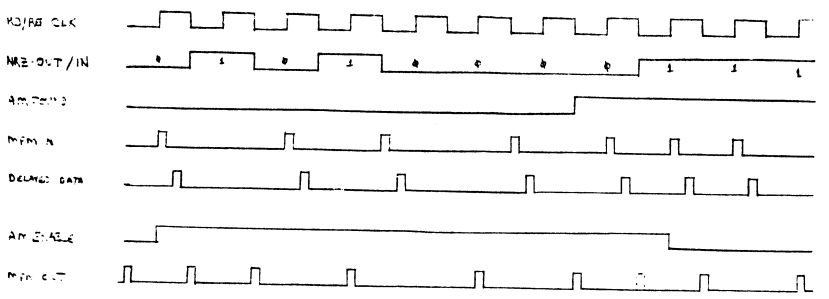


Figure 7. VCO/Encode/Decode Timing

2.3 D.C. INFORMATION

2.3.1 Absolute Maximum Ratings

- Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.
- Ambient operating temperature is 0°C to +70°C.
- Storage temperature ranges from -65°C to +150°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

2.3.2 Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- +4.75 V < VCC < +5.25 V
- GND = 0 V
- 0°C < TA < +70°C

2.3.3 D.C. Characteristics

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2	VCC	V		
Output Low Voltage		0.4	V		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

2.4 PACKAGE DIMENSIONS

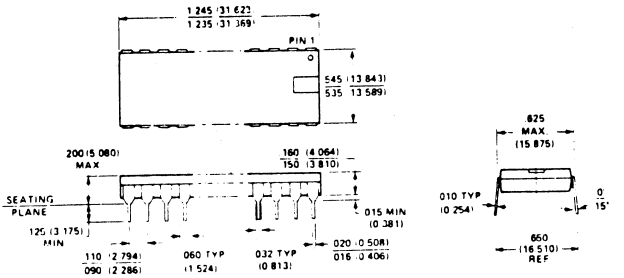


Figure 8. Package Dimensions

APPENDIX A

APPLICATION NOTE

PFM 5070 - APPLICATION NOTE

1) INTRODUCTION

-- The OMTI PFM 5070 VCO/Encode/Decode chip provides all the necessary functions needed to convert MFM serial data signal coming from disk drives interfaces (i.e. ST506/412, SA 1000) to NRZ data and clock signals.

-- The OMTI PFM 5070 performs both read and write modes.

* In the write mode the OMTI PFM 5070 converts the NRZ IN signal in MFM encoded write pulses to be sent to the disk drive interface. It also provides adjustable write precompensation and Address Mark generation.
* In the read mode the OMTI PFM 5070 decodes the incoming MFM signal into a NRZ read data signal. It also provides:
  - A read reference clock signal synchronous with the NRZ read data in order to sample it and drive the deserializer section of the sequencer circuit.
  - An Address Mark found signal to be used as a byte boundary signal for the deserializer section of the sequencer circuit.

-- In order to perform all the above mentioned functions the OMTI PFM 5070 contains:

- An internal PLL (phase locked loop) with its own VCO (voltage controlled oscillator)
- A data separation circuit (MFM decode)
- An MFM encode circuit
- An Address Mark generation circuit
- An Address Mark detection circuit
- A write precompensation circuit
- The PFM 5070 is capable of operation at data rates up to 10 megabits per second by proper selection of external components

2) FUNCTIONAL DESCRIPTION - WRITE OPERATION

2.1.) The two types of write operation.

- A write operation is performed at every time information is to be recorded on the disk.
- There are two types of write operation: Format and sector write or update.
- The Format operation or disk initialization is the only operation that consists in nothing else but a write.
- The Sector write or update operation always begins with a read operation necessary to identify the appropriate sector where the information has to be written, it then involves a read to write switch operation.

2.2.) How is a pure write operation performed by the PFM 5070?

- From a system point of view, a write operation is performed with the following sequence of events:
  * A write command is sent by the CPU to the controller.
  * The controller decodes the write command and depending on command type (Format or sector write) the command decoding will first activate: write (for a Format operation) or read (for a sector write operation) signals.
- Let, then consider that the controller is decoding a format operation (pure write), then the write operation is performed at the PFM 5070 level by:
  a) Enabling the PFM 5070 WRT GATE input (pin 5 high)
  b) Disabling the PFM 5070 RD GATE input (pin 4 low)
  c) Having the PFM 5070 2F REF input (pin 6) fed with a clock signal which period equals half the bit cell time (10 MHz for a 5MHz disk drive)
  d) Feeding the PFM 5070 NRZ IN input (pin 1) with the Non Return to Zero serial data to be MFM encoded and written to the disk. This signal has to be in synchronization with the RD/REF CLK output (pin 3) which is the reference clock for the NRZ IN signal generation. The RD/REF CLK output (half the frequency of 2F REF CLK input in the write mode) can be used as the clock input for the sequencer (i.e. the PFM 5050) that will elaborate the NRZ IN signal (Data + ECC or CRC) for the PFM 5070

e) Enabling the PFM 5070 ENPRECOMP input (pin 11 high) when required in order to reduce predictable bit shift (also called peak shift) due to flux transition crowding at disk inner tracks.
As a rule of thumb it is recommended to enable precompensation for inner tracks at half the way between outside and inside cylinders.
A table of the predictable bit shift patterns automatically compensated by the PFM 5070 is shown on Fig. 1.

Fig.1

- As a rule of thumb the precompensation value is in the order of 6% of the bit cell time (12 nanoseconds for a 5 MHz disk drive). The PFM 5070 is already internally set for a nominal precompensation value of 12 nanoseconds, however larger precompensation times can be obtained by connecting an external capacitor between the PRECOMP C input/output (pin 17) and ground.

- After setting the PFM 5070 according to the above mentioned steps (a through e), then an MFM encoded and precompensated signal will be available at its MFM OUT output (pin 15). This signal has to be fed to the disk drive interface through a differential driver.
- A general block-diagram of the write circuit is shown in Fig. 2.

Fig. 2

3) FUNCTIONAL DESCRIPTION - READ OPERATION

3.1.) General description of a read operation

- First of all a disk read operation is format dependent (the disk having been previously formatted by a write operation).
- The read operation consists in decoding the serial "raw data" coming from the disk and transforming it in "words" of parallel data (i.e. bytes) to be sent to the CPU.
- The read operation is the most complex operation a controller has to perform and the design of the "read bit processor" section of the PFM 5070 is key to the performance of the whole system.

- The PFM 5070 is set up for a read operation by:

a) Disabling the PFM 5070 WRT GATE input (pin 5 low)
b) Enabling the PFM 5070 RD GATE input (pin 4 high)
c) Having the PFM 5070 2F REF input (pin 6) fed with a clock signal which period equals half the bit cell time (10 MHz for a 5 Mhz disk drive)
d) Feeding the RD RAW input (pin 14) with the MFM encoded data coming from the disk.

3.2.) How is a read operation performed by the PFM 5070?

3.2.1. Format (fields and subfields)

- In order to understand how to use the PFM 5070 for a read operation, it is necessary to understand the format written on the disk.

Fig. 3

- As it is shown Fig. 3 the format consists in 5 different functional fields:
  * the synchronization field
  * the Identification field
  * the Sector address field
  * the Data field
  * the Check field

- The synchronization field can only be detected and recognized by hardware (inside the PFM 5070). It consists of two sub-fields: a constant frequency field (sync.) used to synchronize the PLL (phase locked loop circuit, inside the PFM 5070) and, following it, a unique hardware generated character called Address Mark (and also sync. byte, detected inside the PFM 5070) to be used as a "word" bounday indicator in order to start the deserializer circuit (conversion from serial to parallel, outside the PFM 5070, inside the PFM 5050 data sequencer).

- The Identification field consists of one character used to identify the type of field following it (i.e. FEH for a sector address field, F8H for a data field).

- The Sector Address field contains the sector address. This address can be logical (as a RAM memory address) or physical (defining cylinder number, head number, sector number).

- The Data field contains the useful data to be read. This data is organized in blocks or sectors of a given number of characters (i.e. 256 bytes/sector).

- The check fields are appended to both sector address and data field. There are two kinds of check fields:
  * Cyclic Redundancy check (CRC) field used to detect errors.
  * Error correcting code (ECC) field used to both detect and correct erros within a range of given specifications.

- It is a common practice to write a CRC field at the end of a sector address field and an ECC field at the end of a Data field.

- The hardware logic for both CRC and ECC is external to the PFM 5070 and internal to the PFM 5050 data sequencer.

3.2.2. Sequence of events performed by the PFM 5070 during a read operation.

3.2.2.1. Idle Mode

- Before RD GATE input (pin 4) is active, the PLL (phase locked loop) circuit of the PFM 5070 is synchronized to the 2F REF input (pin 6).
  As it was said before, this input is fed with a clock which period equals half the bit cell time (10 MHz for a 5MHz disk drive).
  The PLL being adjusted to track this 2F REF input signal (see adjustment procedure, paragraph 3.2.3), the 2F REF and sync. field signals having equal or very close frequencies (spindle speed variations...) the PLL lock-up time will be reduced to the 3 bit cells time of the start in phase circuit (clamp circuit described in paragraph 3.2.2.2).

3.2.2.2. Sync. field detection and PLL switching

- MFM encoded data can only have 3 frequencies; or in other words, 3 possible bit spacings:
  1 bit cell, 1.5 bit cell, 2 bit cells.
- The sync. field begins with a sub. field of the highest frequency (obtained by writing 00H during the format operation).
- Data = 00H, when MFM encoded, results in a stream of only clock pulses which period equals the bit cell time.
- As soon as RD GATE input (pin 4) becomes active, two simultaneous events take place:
  * A count of incoming RD-RAW data pulses starts.
  * A retriperable mono-shot is fired at every incoming RD RAW data pulse.

ADJ. (SYNC. DET)

- the external RC time constant connected to 1F DET RC Input/Output (pin 18) has to be adjusted in such a way that when reading a sync. field the 1F DET output (pin 10) remains high.
  One of the possible adjustment procedures will be as follows:
  a) Enable the PFM 5070 RD GATE input (pin 4 high)
  b) Feed the PFM 5070 2F REF input (pin 6) with a 2F clock signal (100 nanoseconds period for a 5MHz disk drive).
  c) Connect the 1F DET RC Input/Output (pin 18) to the junction point between a resistor R to Vcc and a capacitor C to ground. At least one of those two components has to be adjustable.
  The nominal RC time constant for a 5MHz disk drive is 168 nanoseconds (can be obtained for example with R = 5.1K and C = 33 pF).
  d) Connect the A channel of an oscilloscope to the RD RAW input (pin 14)
  e) Feed the RD RAW input (pin 14) with the output of a pulse generator and send a pulsed signal with the following characteristics:
  pulse width: 1/4 bit cell.
  pulse period: At least 1.5 bit cell, Maximum 2 bit cells.
  f) Connect the B channel of the same oscilloscope to the 1F DET output (pin 10)
  g) Adjust one or both components in such a way that the signal observed on the B channel remains periodically high for 1.25 +/- .5 bit cell as shown on Fig. 4.

Fig.4

- Recommended values for data rates between 3 and 10 MHz will be R = 5.1K, C adjustable 5-70pF
- The external capacitor being properly adjusted then the following occurs:
- After a count of 8 (normal mode) or 1 (fast acquisition mode) RD RAW pulses - depending on the state of the MODE input (pin 13 high in normal mode) - the input of the internal PLL is switched from 2F REF to RD RAW and, of course, the 2F REF clock being asynchronous with RD RAW, this results in an unpredictable phase relationship and the lock operation on this new signal would take some time. In order to minimize this time a 3 bits long clamp pulse signal is internally generated. For a time equal to 3 bit cells the VCO (voltage controlled oscillator) oscillation is stopped and the phase comparision is disabled.
  Upon the occurrence of the neet RD RAW pulse the phase comparison is enabled and the VCO starts in phase, thus minimizing lock-up time.

- After a count of 16 (normal mode) or 8 (fast acquisition mode) RD RAW pulses the search for the Address Mark is enabled.

- Note: If, at any time, during the previous operation the 1F DET output goes low (out of sync. field), then all counters are cleared and all the process will resume upon sync. field reading.

3.2.2.3. End of sync. field and Address mark search

- Sync. fields are less than 16 bytes in length (generally between 10 and 13 bytes), then a count of more than 128 (16 bytes) RD RAW pulses will indicate something different from a sync. field (it can be a data field of 00H or FFH). If this count is reached before 1F DET output (pin 10) goes low (indicating the end of the sync. field), then all the logic and counters are cleared and a new sync. field search begins.

- At the end of the sync. field (indicated by a low level pulse on the 1F DET output (pin 10) the counters are reset and the output of the internal Address Mark found latch is monitored. If an Address Mark is found in less than 12 RD RAW pulses the sync. field sequence is finished and the MFM decoded signal called NRZ OUT is available on pin 2 and the read clock signal called RD REF CLK is available at pin 3.

3.2.3 Phase locked loop operation and adjustment

- The phase locked loop belongs to the velocity servomechanisms class and, in this specific application it is recommended to use a lag-lead compensation filter matched with the open loop gain such as, in the Bode plot, it shows a phase margin around 40 degrees for 0dB.
- The phase locked loop itself consists of: a phase comparator, a charge pump, a voltage controlled oscillator and a filter. The filter and part of the oscillator components are adjustable and reside outside the PFM 5070. A typical filter and the external VCO circuit is shown Fig. 5.

Fig. 5

- A clamp circuit minimizes the phase error by starting the VCO oscillation in phase with the RD RAW data pulses.
- The phase comparison is made on each and every pulse of the RD RAW data, delayed by 1/4 of a bit cell. This delay is necessary because the phase comparator is reset at the end of each comparison and every direct (non delayed) RD RAW pulse enables the next phase comparison.

ADJ. (DELAY)

- This delay is created by a current source charging a capacitor.
  An adjustable 20 pF capacitor has to be connected between DELAY C Input/Output (pin 16) and ground.
- A recommended way of adjusting this capacitor is as follows:
  a) RD GATE input (pin 4) has to be disabled (low).
  b) Feed a 2F REF clock signal (10 MHz for a 5MHz disk drive) at the 2F REF input (pin 6).
  c) Connect the "A" channel of an oscilloscope to DELAY OUT output (pin 9).
  d) Connect the "B" channel of this same oscilloscope to PHASE COMP output (pin 22).
  e) Adjust the value of the capacitor in such a way that each low to high transition of channel "B" leads by 1/4 of a Bit Cell (50 nanoseconds for a 5MHz disk drive) each low to high transition observed on channel "A".
- In order to obtain the best performances of the PLL both in the lock and track modes the nominal, or free running period of the VCO oscillation has to be equal to the resolution of the encoded RD RAW signal. As an example, if the code is MFM, then the resolution is 1/2 bit cell and the nominal period of the VCO oscillation has to be equal to 1/2 bit cell.
  The nominal VCO frequency is a function of the capacitor value obtained with the parallel combination of a varicap and of an adjustable capacitor (20pF). Because the capacitor value of the varicap is a function of the voltage applied to it, then the nominal VCO frequency is then a function of 2 variables: The input voltage to the variacap and the value of the adjustable capacitor. The applied voltage has to be centered in the linear range of dynamic operation of the PLL.
- The adjustment method recommended will be conducted with the PLL in operation, that is to say the loop being closed. In such conditions the voltage itself becomes a function of the adjustable capacitor.

- A filter and the external VCO components being installed, the procedure is as follows-
  a) RD GATE input (pin 4) has to be disabled.
  b) Feed a 2F REF clock signal (10 MHz for a 5MHz disk drive) at the 2F REF input (pin 6).
  c) Measure the DC voltage obtained at PU/PD (pin 21) and adjust the capacitor in parallel with the varicap in order to have 2.25V +/- .1V.
- For the above described adjustments (DELAY and PLL) it is recommended to use the PFM 5070 ground (pin 12) as a grounding point for the measurement devices.

3.2.4. Data separation and Address Mark detection

- The data separation section has two inputs: the servo controlled VCO oscillation and the incoming delayed RD RAW data.
  Those two signals are synchronous (when the PLL is in the tracking mode) and the servo-controlled VCO oscillation, divided by two becomes then a bit cell period signal used as a window to separate clock and data pulses.
- Clock and data pulses are then separated in NRZ signals, and the occurrence of the unique Address Mark clock pattern (this pattern is written by violating MFM encoding rules and it is characterized by a "missing" clock) is then detected.
- The AM FOUND output (pin 8) then goes high. This signal has to be used as a "word" (i.e. byte) boundary signal to start the deserializing operation (outside the PFM 5070, inside the PFM 5050)
- Internally to the PFM 5070, the AM FOUND signal is fed-back to the sync field detection circuit in order to reset the counters and disable any new sync. field search.
- A general block-diagram of the read circuit is shown in Fig. 6.

Fig. 6

4.) FUNCTIONAL DESCRIPTION - SECTOR WRITE/UPDATE OPERATION

4.1.) General description of a sector write/update operation

- A sector write/update operation consists of two events: a read, followed by a write.
- Let then consider now, that the controller is decoding a sector write operation.

- The controller, then receives from the CPU a command containing the address of the sector to be written or updated.
- In order to find the "targetted" sector the first operation to be performed is a read.
- In order to be able to read the disk, an initial format operation was previously performed (see paragraphs 2.2, 3.2.1, and Fig. 4)
- There a write operation takes place and write or update the data field and check field.

4.2) How is a sector write/update operation performed by the PFM 5070?

- The PFM 5070 is first set up for a read operation according to the procedure a) to d) described in paragraph 3.1. and with the adjustments described in paragraph 3.2 being performed, then the read operation sequence (previously described in paragraph 3.2.2.) takes place.
- Then the RD REF CLK (pin 3) and NRZ OUT (pin 2) output signals are sent to the sequencing section (i.e. PFM 5050) of the controller. The data obtained by deserializing NRZ OUT is then word to word compared with the address contained in the command; if they match, then the CPU is requested to send the data to be written inside the data field of this same sector.
- Then a pure write operation takes place with the following sequence of events:
  a) the PFM 5070 RD GATE input is disabled (pin 4 low)
  b) A short delay (generally 2 bytes in length) after the end of the sector identification information (end of the check field following the address field) the PFM 5070 WRT GATE input is enabled (pin 5 high), see Fig. 4. Steps c) to f) of the write operation described in paragraph 2.2.) have to be performed.
- Then the synchronization field and the identification character have to be re-written (as they were written during the format operation), then the data sent by the CPU is written in the data field, and the check field, computed by a CRC or an ECC circuit (external to the PFM 5070, inside the PFM 5050) is appended to it.

5) Design Recommendations-

- In order to obtain the best results from the PFM 5070 it is recommended that:
  * All external components will be small in size and physically close to chip pins they are connected to.
  * The board lay-out will be designed in such a way that the connections to those components will be as short as possible in order to minimize parasite capacitance and inductance effects.

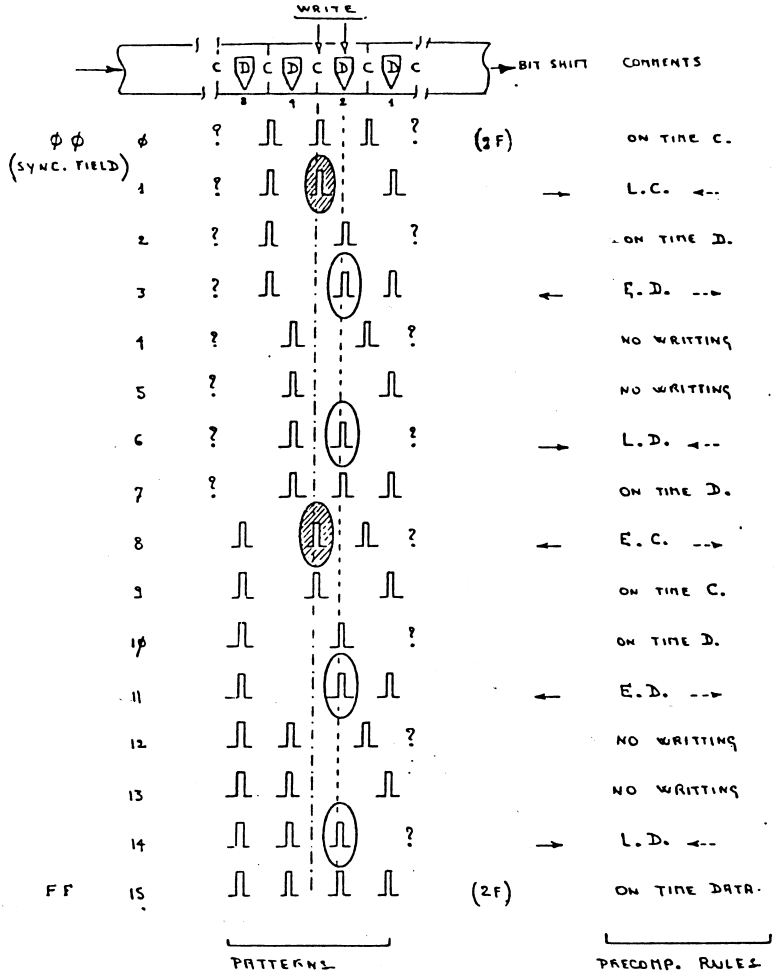


FIG. 1 PREDICTABLE PRECOMP PATTERNS

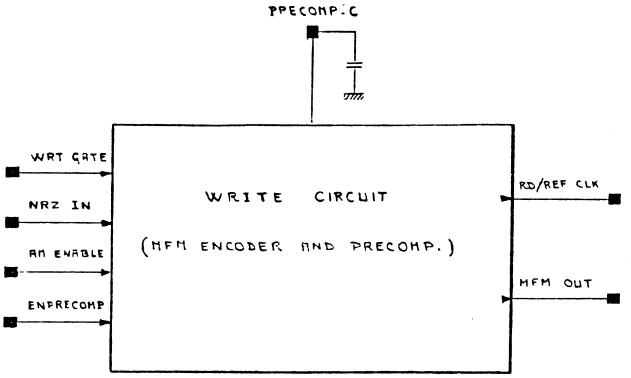
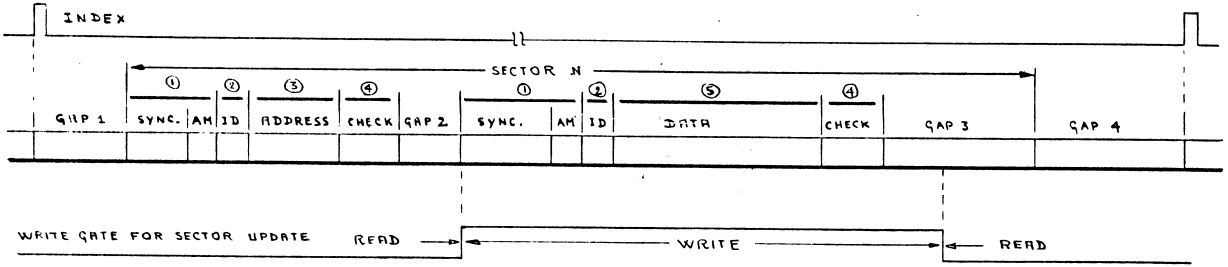
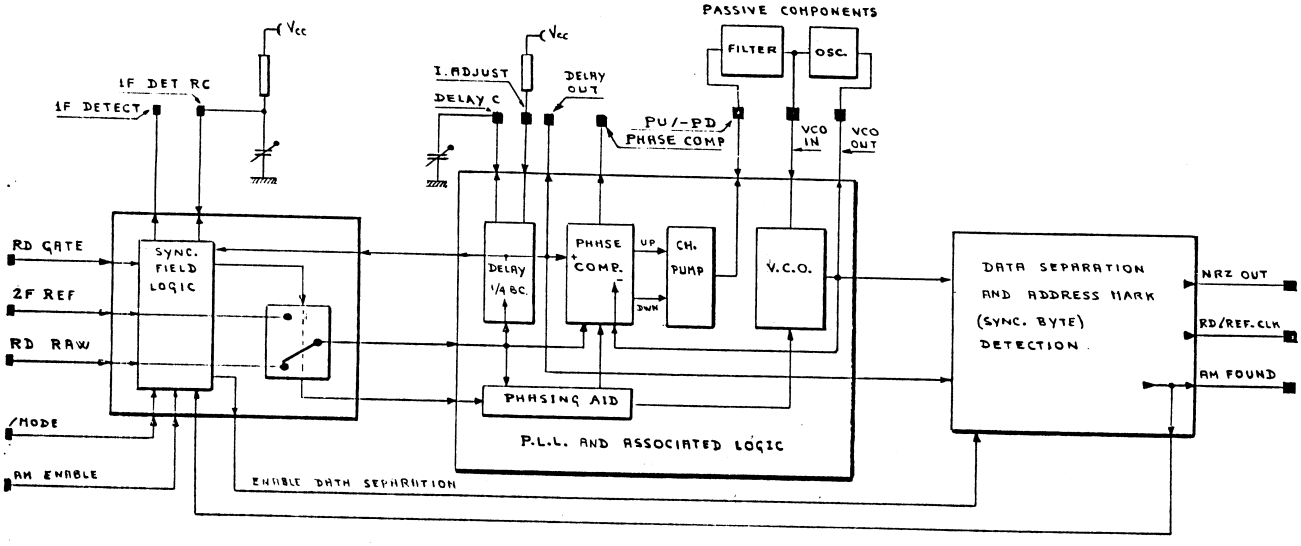

PRECOMP. C
WRT GATE
NRZ IN
AH ENABLE
ENPRECOMP
WRITE CIRCUIT
(MFM ENCODER AND PRECOMP.)
RD/REF CLK
MFM OUT

Fig. 3.



1 SYNCHRONIZATION FIELD
2 IDENTIFICATION FIELD
3 ADDRESS FIELD
4 CHECK FIELD
5 DATA FIELD

Fig 4. FORMAT.



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PFM 5070 READ SECTION - FUNCTIONAL BLOCK-DIAGRAM.

Fig. 5