ST212
PRODUCT MANUAL

Seagate

ST212 PRODUCT MANUAL

March 24, 1986©

36010-001, Revision B

Seagate reserves the right to change, without notice, the specifications contained in this manual.

Seagate ■ 920 Disc Drive, Scotts Valley, CA 95066-4544, USA
Tel. (408) 438-6550 ■ Telex 176455 SEAGATE SCVL

TABLE OF CONTENTS

FIGURES

TABLES

1.0 SPECIFICATION SUMMARY

PERFORMANCE SPECIFICATIONS 1.1

CAPACITY	UNFORMATTED	FORMATTED
Per Drive:	12.76 MB	10.0 MB
Per Surface:	6.38 MB	5.0 MB
Per Track:	10,416 Bytes	8,192 Bytes
Per Sector:	NA	256 Bytes
Sectors Per Track:	NA	32 Sectors

ACCESS TIME DEFINITION AND TIMING 1.1.1

Access time is defined as the time from the leading edge of the last Step pulse received to SEEK COMPLETE (including settling). The Step pulse period must be between 5 μsec. to 500 μsec.

Track-to-Track:	23.0 msec. max.
Average:	65.0 msec. max.[1]
Maximum:	170.0 msec.

FUNCTIONAL SPECIFICATIONS 1.2

Rotational Speed:	3,600 RPM ± 1%
Average Latency:	8.33 msec.
Recording Density:	10,560 BPI/FCI
Track Density:	550 TPI
Cylinders:	306
Tracks:	1,224
Discs:	1
Recording Method:	MFM
Data Transfer Rate:	5.0 Megabits/second

PHYSICAL SPECIFICATIONS 1.3

Height:	1.63 inches max. (41.4 mm)
Width:	5.75 inches max. (146.05 mm)
Depth:	8.00 inches max. (203.2 mm)
Weight:	3.00 lbs (1.4 Kg)

RELIABILITY SPECIFICATIONS 1.4

MTBF:	11,000 Power-on Hours[2]
PM:	Not Required
MTTR:	30 Minutes
Service Life:	5 Years

READ ERROR RATES 1.4.1

Recoverable Read Errors:	1 per 10^{10} bits read [3]
Nonrecoverable Read Errors:	1 per 10^{12} bits read [4]
Seek Errors:	1 per 10^{6} seeks

1. Buffered-Seek
2. Typical usage at 25 °C at sea level. Calculated per *Mil. Spec. 217.*
3. Recoverable within 16 retries
4. Not recoverable within 16 retries

1.4.1.1 BIT JITTER

Bit jitter reduction determines the relationship between the leading edge of Read data and the center of the data window.

The specified Read error rates are based on the following bit jitter specification: The data separator must provide at least -40 dB of bit jitter reduction at 2F with an offset error of less than 1.5 nsec. shift from the center of the data window.

1.4.2 MEDIA DEFECTS

A media defect is a Read error when data, which has been correctly written, cannot be recovered within 16 retries.

A printout will be provided with each drive shipped listing the location of any defect by head, cylinder, sector and byte.[5] It will also specify the number of bytes from Index.

There will be no more than four (4) defects per Read/Write head for a maximum total of sixteen (16) per drive. Cylinder Zero will be free of defects.

1.5 ENVIRONMENTAL SPECIFICATIONS

1.5.1 AMBIENT TEMPERATURE

Operating:	10°C to 45°C (50°F to 113°F)
Nonoperating:	-40°C to 60°C (-40°F to 140°F)

1.5.2 TEMPERATURE GRADIENT

Operating:	10°C/hr (18°F/hr) max.
Nonoperating:	Below condensation

1.5.3 RELATIVE HUMIDITY

Operating:	8 to 80% noncondensing
Maximum Wet Bulb:	26°C (78.8°F)
Nonoperating:	5 to 95% noncondensing

1.5.4 ALTITUDE LIMITS

Operating:	-1,000 ft to 10,000 ft
Nonoperating:	-1,000 ft to 30,000 ft

1.5.5 OPERATING SHOCK

Maximum permitted shock without incurring nonrecoverable errors: 10 G's [6,7]

1.5.6 NONOPERATING SHOCK

Maximum permitted shock without incurring physical damage or degradation in performance: 40 G's[8].

5. Based on a 32-sector, 256 byte/sector format
6. 11 msec. half-sine wave shock pulse.
7. Input levels at the drive mounting screws, drive mounted in an approved orientation.
8. 11 msec., half sine-wave

DC POWER REQUIREMENTS 1.6

The ST212 is listed in accordance with UL 478 and CSA C22.2 (0-M1982), and meets all applicable sections of IEC 380 and VDE 0806/08.81, as tested by *TUV-Rheinland, North America.*

Power may be applied or removed in any sequence without loss of data or damage to the drive.

+12 VDC

Voltage Tolerance (inc. ripple):	± 5% Both seek and non-seek conditions
Maximum Current at Power-on:	3.2 Amp 1.0 Amp typical

+5 VDC:

Voltage Tolerance (inc. ripple):	± 5% Both seek and non-seek conditions
Maximum Current at Power-on:	1.2 Amp 1.0 Amp typical
POWER:	17 Watts typical

INPUT NOISE RIPPLE 1.6.1

The maximum permitted ripple is 50 mV (peak-to-peak) on either +12 Volts or +5 Volts.

INPUT NOISE FREQUENCY 1.6.2

20 MHz max. on both the +12 VDC and +5 VDC lines.

FIGURE 1: Typical +12Volt DC Start-up Current Profile

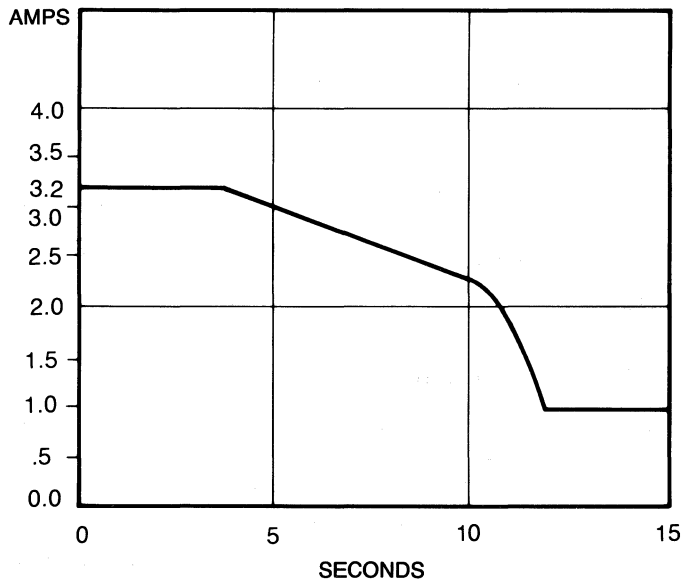
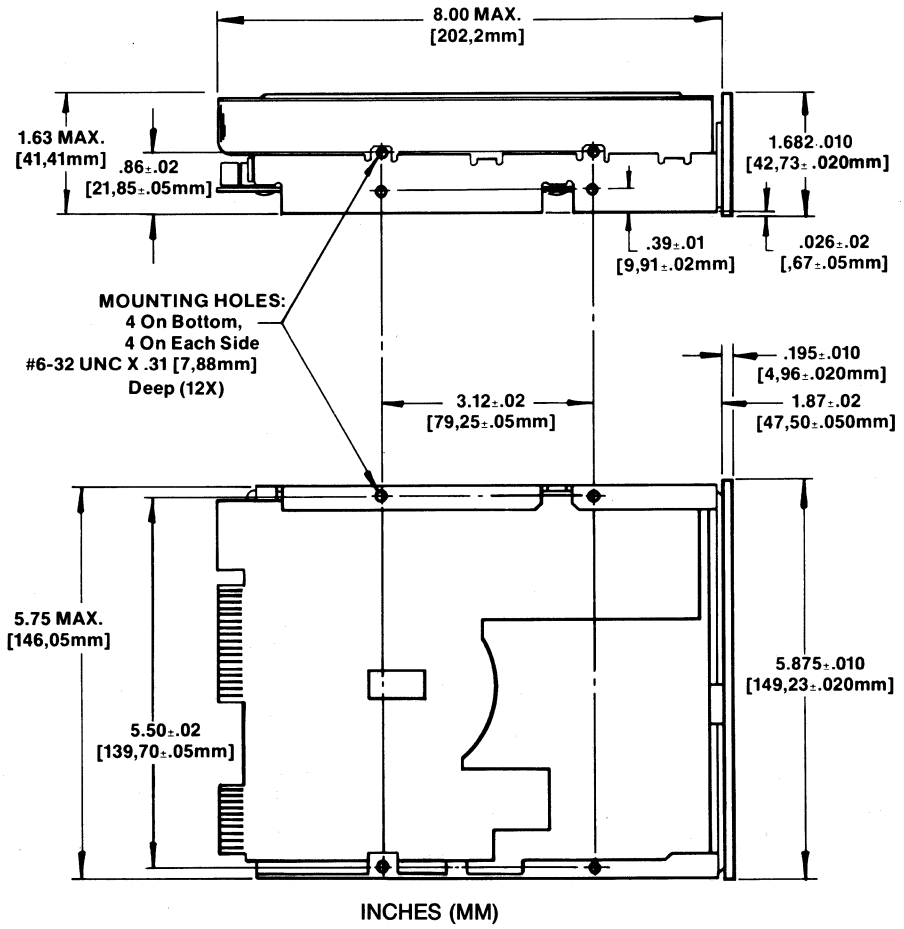


FIGURE 2:
Mounting Dimensions



1.7 MOUNTING REQUIREMENTS

The ST212 may be mounted in the following orientations:

Horizontal:	Spindle motor down
Sides:	Left or right

Refer to *Figure 2* for mounting dimensions.

The drive should not be tilted front to back, in any position, by more than ±5°. For optimum performance the drive should be formatted in the same orientation as it will be mounted in the host system.

A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive to allow for cooling airflow and motion during mechanical shock or vibration.

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25Hz or lower.

HANDLING & STATIC-DISCHARGE PRECAUTIONS 1.7.1

After unpacking, and prior to system integration, the drive is exposed to potential handling and ESD hazard.

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

It is strongly recommended that the drive always rest on a padded surface until it is mounted in the host system.

2.0 ST212 HOST/DRIVE INTERFACE

This section details the physical specifications of the host/drive interface connectors. Connector dimensions and pin assignments follow under each section. Refer below to *Figure 7* for an overall view of the drive interface connectors.

2.1 CONTROL AND STATUS SIGNALS: PCB EDGE-CONNECTOR J1

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Control and status signals between the host and the drive are transmitted through a 34-pin PCB edge-connector, J1. *Figure 3* indicates connector dimensions and *Table 1* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 4.*

With the drive resting on a padded surface, oriented with the Main Control PCB up and the edge-connectors toward you, J1 is to your left and J2 is on the right. Refer to *Figure 7.*

J1 pins are numbered 1 through 34 with the even pins located on the component side of the PCB. All odd pins are ground. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J1 is AMP ribbon connector part number 88373-3.

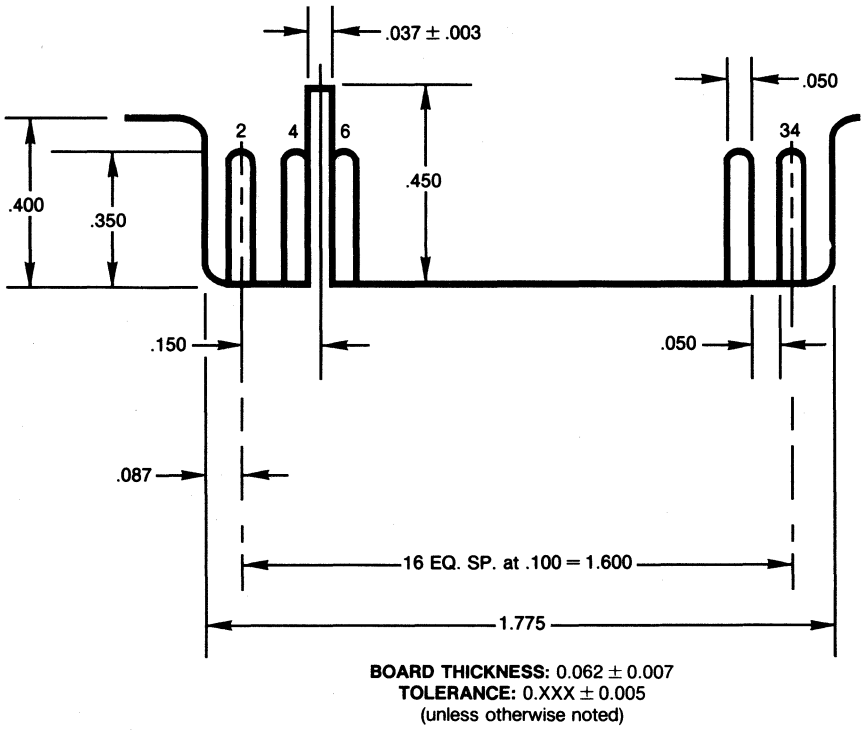


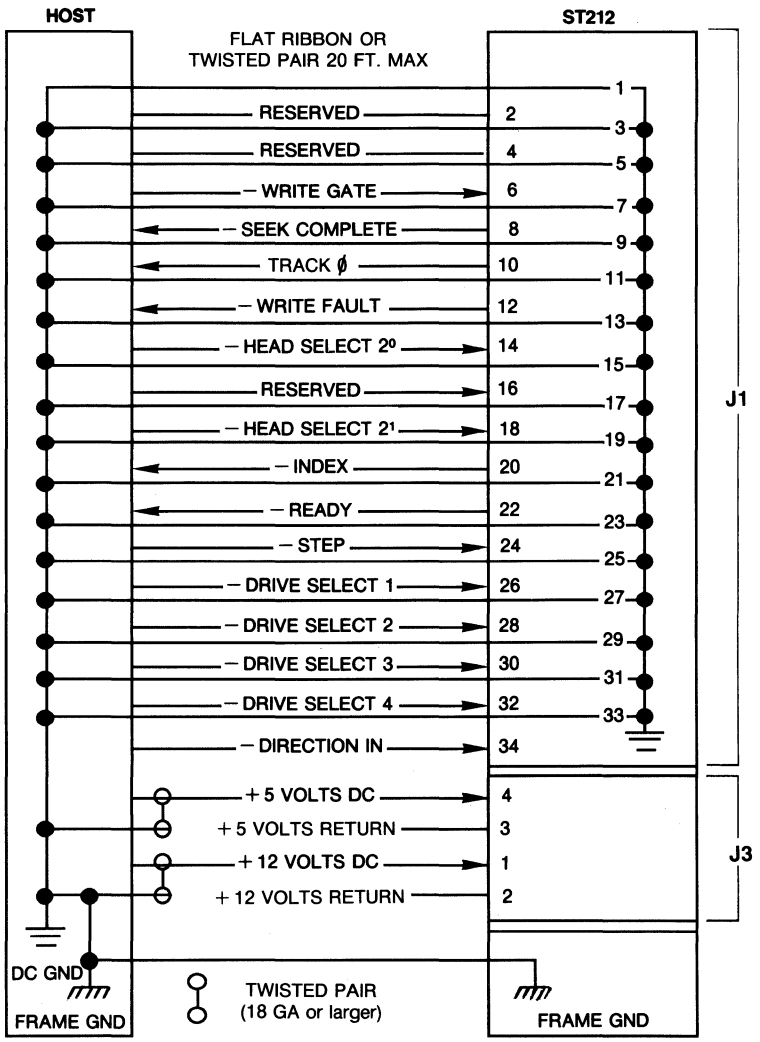
FIGURE 3: J1 Connector Dimensions

TABLE 1: J1 Host/Drive Pin Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	RESERVED
3	4	RESERVED
5	6	-WRITE GATE
7	8†	-SEEK COMPLETE
9	10	-TRACK Ø
11	12†	-WRITE FAULT
13	14	-HEAD SELECT 2^0
15	16	RESERVED
17	18	-HEAD SELECT 2^1
19	20†	-INDEX
21	22†	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN

†STATUS ENABLED WITH DRIVE SELECT

FIGURE 4: Control/Status Signals



2.2 DATA SIGNALS: PCB EDGE-CONNECTOR J2

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Read/Write data signals are received and transmitted over a 20-pin PCB edge-connector, J2. *Figure 5* indicates connector dimensions and *Table 2* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 6.*

With the drive resting on a padded surface, oriented with the Main Control PCB up and the edge-connectors toward you, J2 is to your right and J1 is on the left. Refer to *Figure 7.*

J2 pins are numbered 1 through 20 with the even pins located on the component side of the PCB. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J2 is AMP ribbon connector, part number 88373-6.

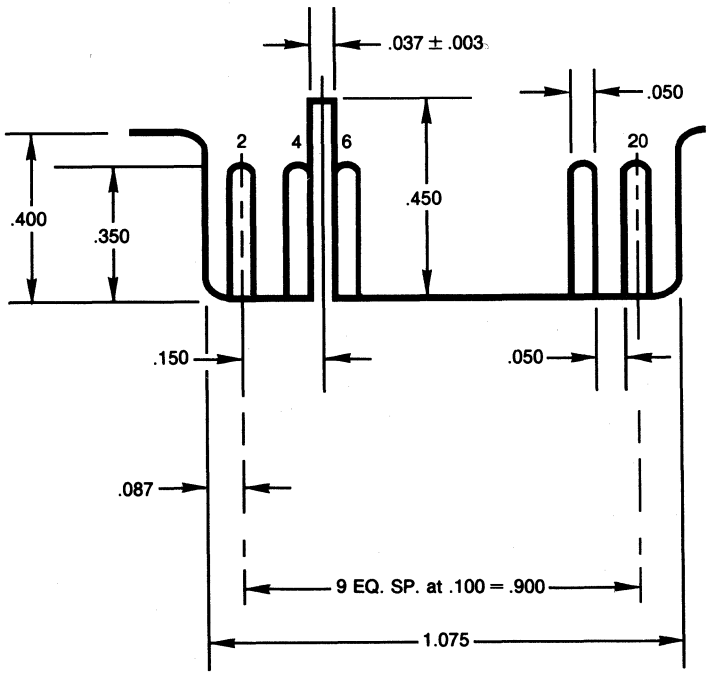
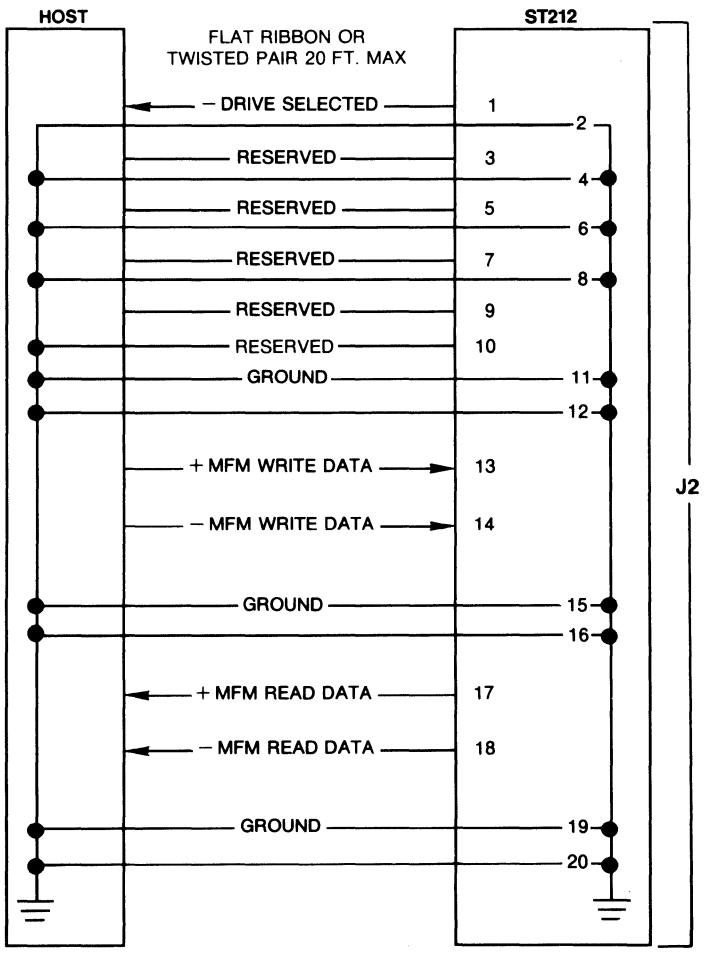


FIGURE 5: J2 Connector Dimensions

TABLE 2: J2 Host/Drive Pin Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
10	9	RESERVED
12	11	GROUND
	13	+ MFM WRITE DATA
	14	− MFM WRITE DATA
16	15	GROUND
	17	+ MFM READ DATA
	18	− MFM READ DATA
20	19	GROUND

FIGURE 6: Data Signals



2.3 DC POWER: CONNECTOR J3

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

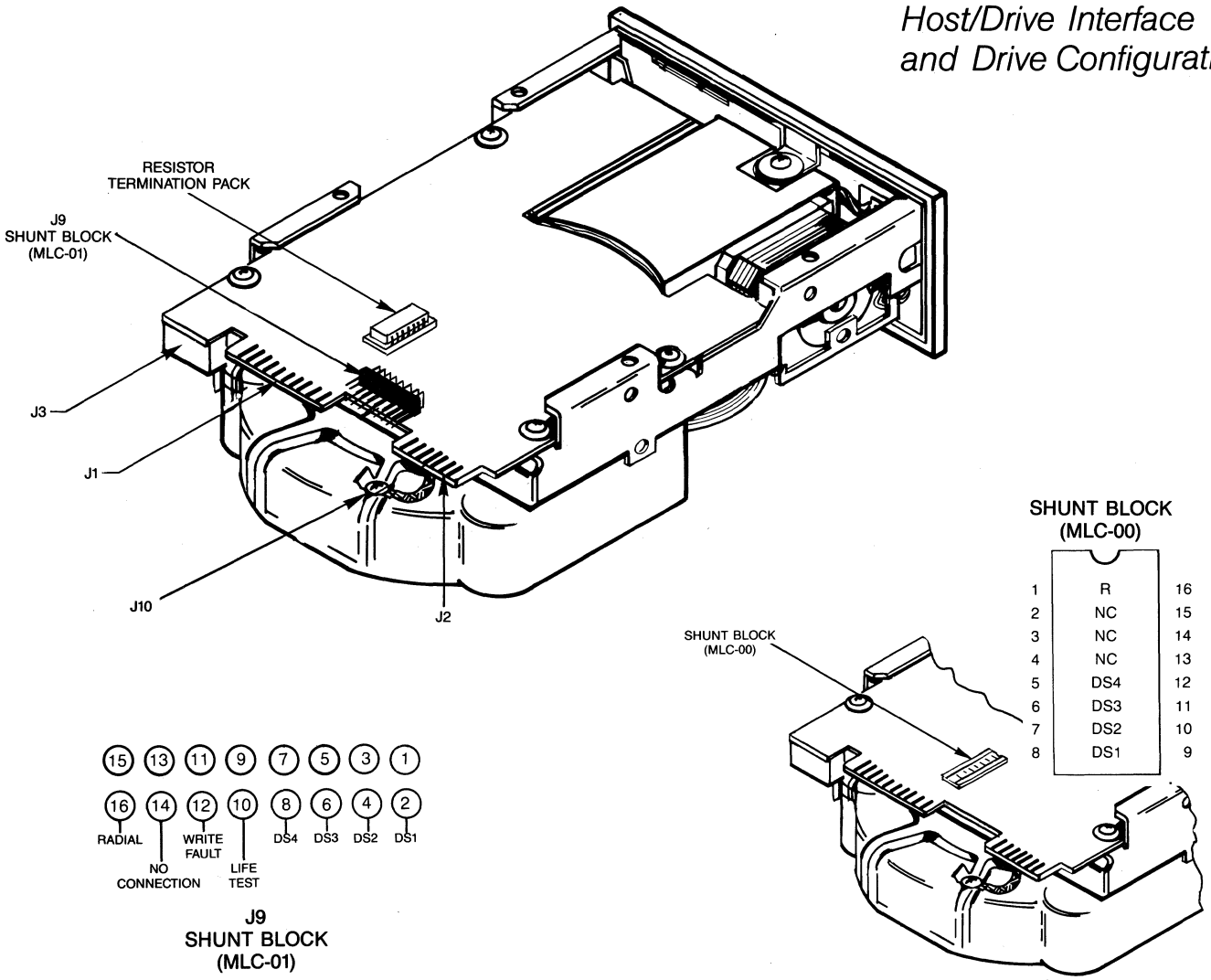
DC power is transmitted from the host to the drive via the power connector, J3. J3 is a 4-pin AMP "Mate-N-Lock" connector, AMP part number 350211-1, mounted on the solder side of the PCB. The recommended mating connector is AMP part number 1-480424-0.

Applications using cable lengths less than five feet, may use #18AWG wire and AMP 61314-4 strip pins. For applications requiring cable lengths greater than five feet, #14AWG wire is recommended using AMP 61117-4 strip pins.

2.4 FRAME GROUNDING: LUG J10

J10 is an AMP "Faston," part number 61761-2. It is located on the casting between and below the host/drive interface connectors. The recommended mating connector is AMP part number 62187-2. Refer below to *Figure 7.*

FIGURE 7: Host/Drive Interface and Drive Configuration



3.0 DRIVE CONFIGURATION

The ST212 may be configured for specific system requirements. These options are detailed in *Sections 3.1* through *3.5.*

DRIVE CONFIGURATION: SHUNT J9 (MLC-01) 3.1

J9 is a 16-pin right-angle shunt located midway between J1 and J2. Use the provided shorting blocks to enable the DRIVE SELECT lines and any required option. *Figure 7* illustrates J9 and indicates pin 1.

Earlier drives employed a shunt which required cutting the jumpers to enable DRIVE SELECT. To enable DS1, for example, cut DS2, DS3 and DS4. Refer to *Figure 7.*

DRIVE SELECT 3.2

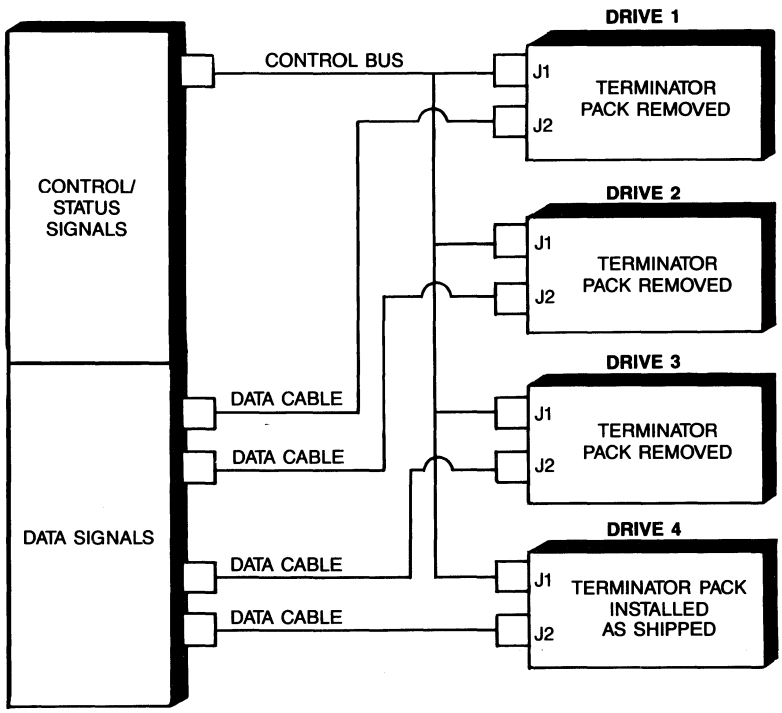
The DRIVE SELECT line enables the controller to select and address the drive.

Pins 1-2 shorted enable DRIVE SELECT 1
Pins 3-4 shorted enable DRIVE SELECT 2
Pins 5-6 shorted enable DRIVE SELECT 3
Pins 7-8 shorted enable DRIVE SELECT 4

DAISY-CHAIN 3.2.1

Each drive in the chain must be selected as either DRIVE SELECT 1, 2, 3 or 4, so that only one DRIVE SELECT LINE activates a device. The last drive in the chain must have the 220/330 Ω resistor termination pack installed on the Main Control PCB.

FIGURE 8: Daisy-chain Configuration



3.3 RADIAL

The Radial option is enabled by shorting pins 15 and 16 at the J9 shunt. Drives configured to this option are always selected and respond to all control signals issued on the attached control cable. The 220/330 Ω resistor termination pack must remain installed on each radially-connected drive. *Figure 9* illustrates a host/drive Radial interconnection.

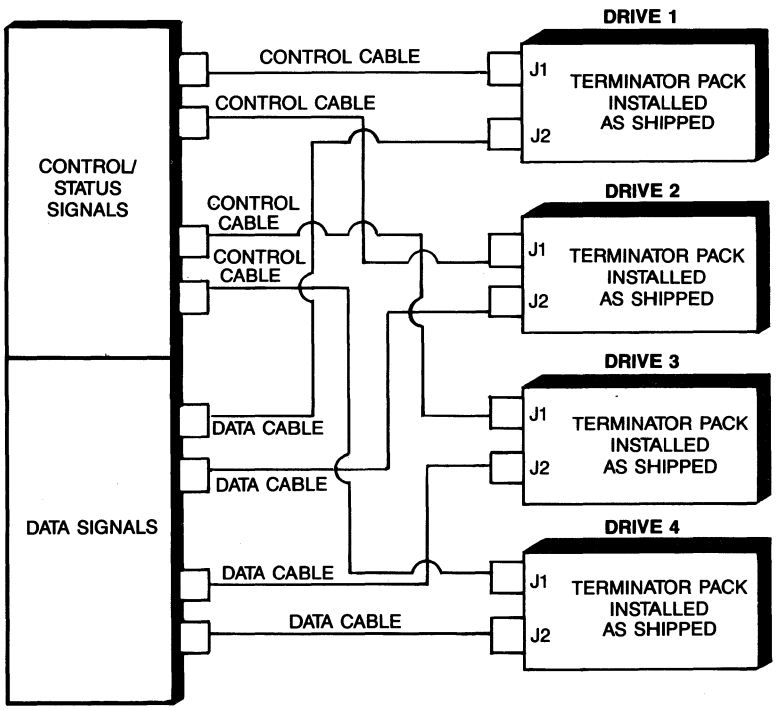


FIGURE 9: Radial Configuration

3.4 WRITE FAULT

The WRITE FAULT signal is internally latched. A selectable option is provided to clear this latch. The standard configuration, with the shorting block removed, resets the WRITE FAULT latch when WRITE GATE is dropped and reasserted after the detected fault has been cleared. With pins 11 and 12 shorted, WRITE FAULT latch is reset when DRIVE SELECT is dropped and reasserted after the detected fault has been cleared.

3.5 LIFE TEST

This function is used during the manufacturing process and is **not recommended for field use.** When pins 9 and 10 are shorted, the stepper motor will continuously seek between Track Ø and the maximum cylinder. When in this mode the drive will ignore control signals sent via the interface.

4.0 CONTROL INPUT SIGNALS

The control signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing.

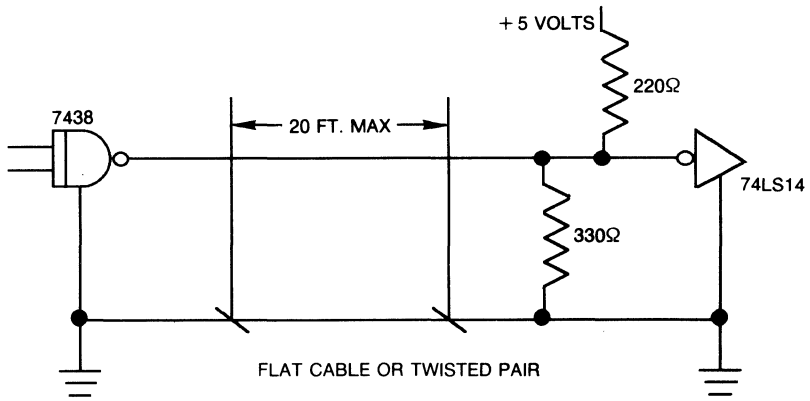
The signals to be multiplexed are WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, DIRECTION IN, and STEP. These lines are terminated with a removable 220/330 Ω resistor pack.

The multiplexing signals are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4. These lines are terminated in a single fixed 220/330 Ω resistor pack.

Control signals are transmitted across the driver/receiver combination illustrated in *Figure 10.* Control input signals are activated in accordance with the following specifications:

True: 0.0 VDC to 0.4 VDC at I = -48 mAmp max.
False: 2.5 VDC to 5.25 VDC at I = +250 μAmp (open collector)
Termination: 220/330 Ω resistor pack

FIGURE 10: Control Signals Driver/Receiver Combination



HEAD SELECT 2^0, 2^1, 2^2, 2^3 4.1

These signals allow the selection of each Read/Write head in a binary code sequence. The lines are numbered 0 through 3. HEAD SELECT line 2^0 is the least significant line. When all HEAD SELECT lines are high on the interface, Head 0 is selected.

WRITE GATE 4.2

The active state of this signal, or low level, enables data to be written to the disc and inhibits carriage motion if WRITE FAULT is active on the receipt of the first Step pulse. When inactive, or high, this signal enables data to be transferred from the drive and enables Step pulses to move the heads. Heads may not be switched while WRITE GATE is active.

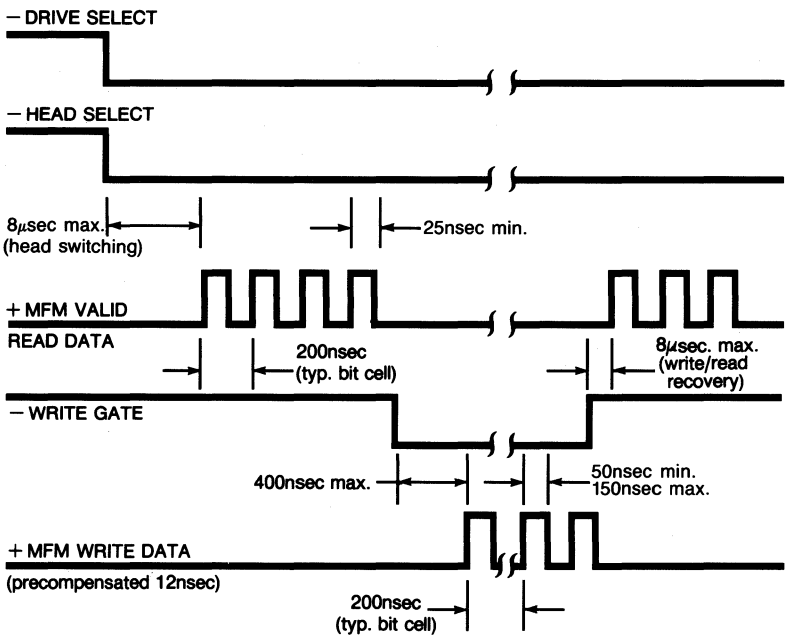


FIGURE 11: Read/Write Timing

4.3 STEP

The STEP signal is a 2 μsec. minimum width pulse that initiates Read/Write head motion. The number of pulses issued determines distance traveled. The rate of Step pulses determines the access method.

If the period between pulses is from 5 μsec. to 500 μsec., the access method will be Buffered-Seek. Slow-Step is employed if the period between pulses is greater than or equal to 3 msec.

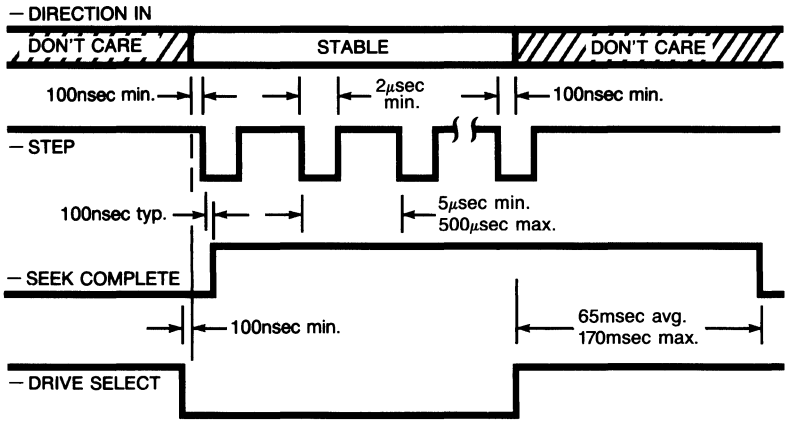
DIRECTION IN must be stable 100 nsec. before the leading edge of the first step pulse and remain stable for 100 nsec. after the last pulse in a string of Step pulses. Step pulses issued between 500 μsec. and 3 msec. may be lost.

If excessive Step pulses are issued which would cause a seek inward beyond cylinder 306 or outward beyond Cylinder Zero, the drive will enter the Auto-Truncation mode. Refer to Section 4.3.4.

4.3.1 BUFFERED SEEK

To minimize access time, pulses may be issued at an accelerated rate and buffered in a counter. Initiation of a seek starts immediately after the first pulse is received. Head motion occurs during pulse accumulation, and the seek is completed following receipt of all pulses.

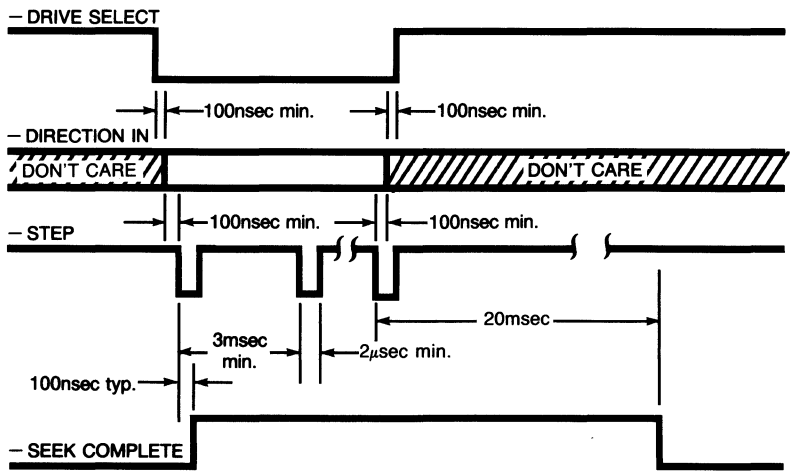
FIGURE 12: General Step Timing



SLOW-STEP (Single-Track) 4.3.2

In Slow-Step, the stepper motor is settled and SEEK COMPLETE is issued 20 msec. max. after the leading edge of the last Step pulse.

FIGURE 13: Slow-step Timing



4.3.3 AUTO-TRUNCATION

The drive will enter the Auto-Truncation mode if the controller issues an excessive number of Step pulses, which would place the Read/Write heads outward beyond Track Ø or inward beyond cylinder 306.

With the Auto-Truncation mode active, the drive disallows additional pulses, takes control of the stepper motor and recalibrates the heads to Track Ø.

CAUTION: If the controller is still issuing Slow-Step pulses after the drive issues SEEK COMPLETE from Auto-Truncation mode, the ST212 will either reenter Auto-Truncation mode with DIRECTION IN false, or step the remaining cylinders with DIRECTION IN true.

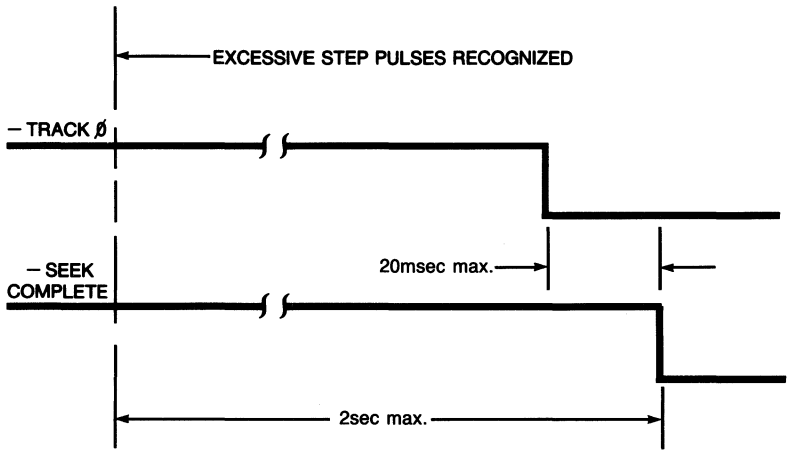


FIGURE 14: Auto-truncation Timing

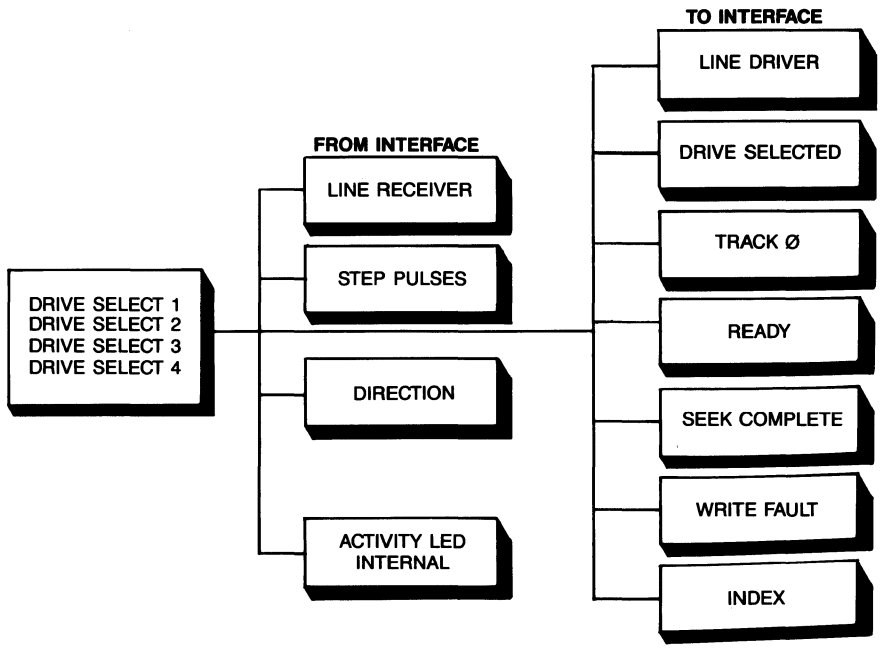
4.4 DIRECTION IN

DIRECTION IN defines the direction the Read/Write heads will move when the STEP line is pulsed. With DIRECTION IN true, each pulse causes the heads to move one cylinder inward toward the spindle. With DIRECTION IN false, each pulse causes the heads to move one cylinder outward toward Track Ø.

4.5 DRIVE SELECT

The DRIVE SELECT line is activated by the controller to select and address the drive. Refer to *Section 3.0.*

FIGURE 15:
Drive Select



5.0 CONTROL OUTPUT SIGNALS

The control output signals are gated to the interface when selected. They are: DRIVE SELECTED, INDEX, TRACK Ø, READY, SEEK COMPLETE and WRITE FAULT.

5.1 DRIVE SELECTED

DRIVE SELECTED is a status signal transmitted over J2, which informs the host system of the selection status of the drive. The signal is driven by a TTL open collector, as illustrated in *Figure 10.* The signal goes low (true) on the interface only when the device is correctly configured (see *Sections 3.1-3.5*) and the DRIVE SELECT line is activated by the host system.

5.2 INDEX

This signal is provided by the drive once each revolution to indicate the beginning of a track. The nominal period is 16.67 msec., with a typical pulse width of 1.5 msec. Normally this signal is at a high level and the transition to low indicates INDEX. Only the transition from high to low, or the leading edge, is valid.

5.3 TRACK Ø

This signal is low (true) only when the Read/Write heads are positioned at Cylinder Zero.

Track Ø is the only cylinder that provides interface recognition. The drive is designed to recalibrate to Track Ø during power-on and Auto-Truncation operations.

Track Ø may also be accessed via conventional Buffered-Seek and Slow-Step modes. After Track Ø is true, no actions may be taken by the controller until SEEK COMPLETE is also true.

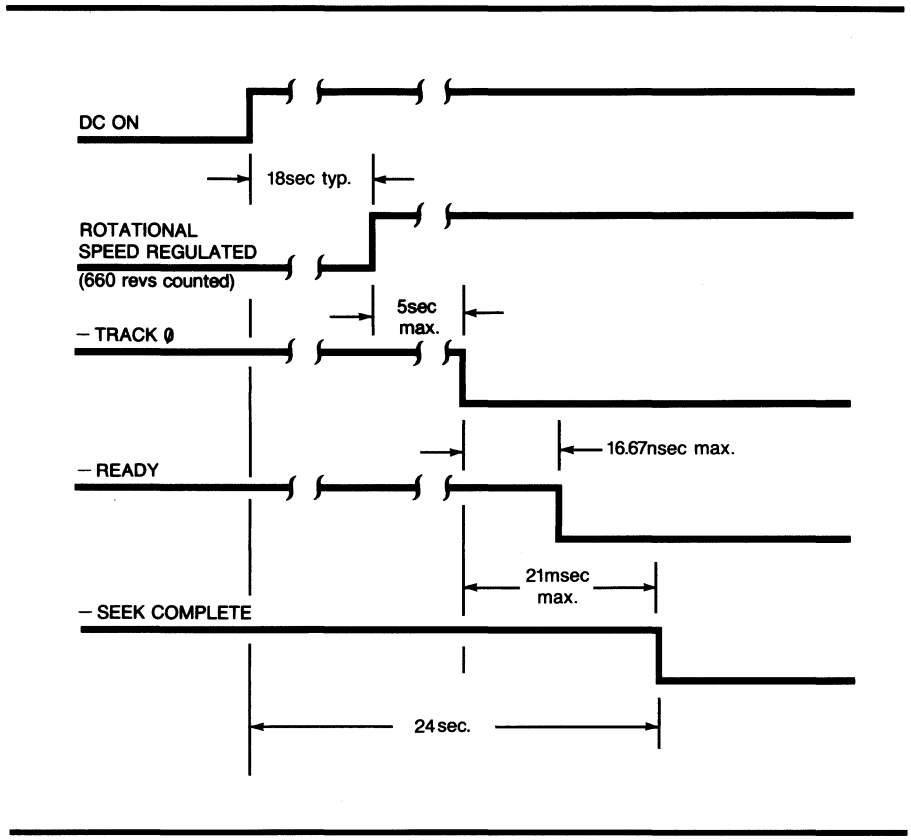
5.4 READY

This signal, when true together with SEEK COMPLETE, indicates that the drive is ready to Read, Write or Step and that all control input signals are valid. When this line is high, all reading, writing and stepping are inhibited. The typical time after power-on for READY to be true is 24 seconds.

READY remains false during the power-up sequence until:

1. The recalibration to Track Ø is complete
2. Spindle speed is stable within ± 1% of nominal
3. Drive initialization routines are complete
4. DC voltages are within tolerance.

FIGURE 16: Typical Power-up Sequence



SEEK COMPLETE 5.5

This signal goes low on the interface when the Read/Write heads have settled on track upon completion of a seek. Seeking, reading or writing should not be attempted when SEEK COMPLETE is false. SEEK COMPLETE goes false in the following four cases:

1. When a recalibration sequence is initiated (by drive logic) at power-on.
2. 100 nsec. max. after the leading edge of a Step pulse.
3. If either +5 Volts or +12 Volts are detected as unsafe.

WRITE FAULT 5.6

This signal indicates that a condition exits at the drive which, if not corrected, may cause an incorrect write operation. WRITE FAULT will remain true until the condition causing the fault is corrected. The controller should edge detect this signal.

WRITE FAULT SIGNAL GENERATION 5.6.1

With DRIVE SELECT active, and one of the following conditions true, the WRITE FAULT signal will be issued to the interface and Write Current will be inhibited.

1. Write Gate true with no Write Current flowing to the head
2. Write Current to the heads with no Write Gate

5.6.1.1 WRITE CURRENT INTERRUPTION

Any of the following conditions will cause Write Current to be inhibited when Write Gate is true:

1. Multiple heads selected
2. No head selected
3. SEEK COMPLETE false
4. READY false
5. DC Voltages out of tolerance
6. A Step pulse is received

5.7 FAULT DETECTION: PC BOARD 20292-XXX

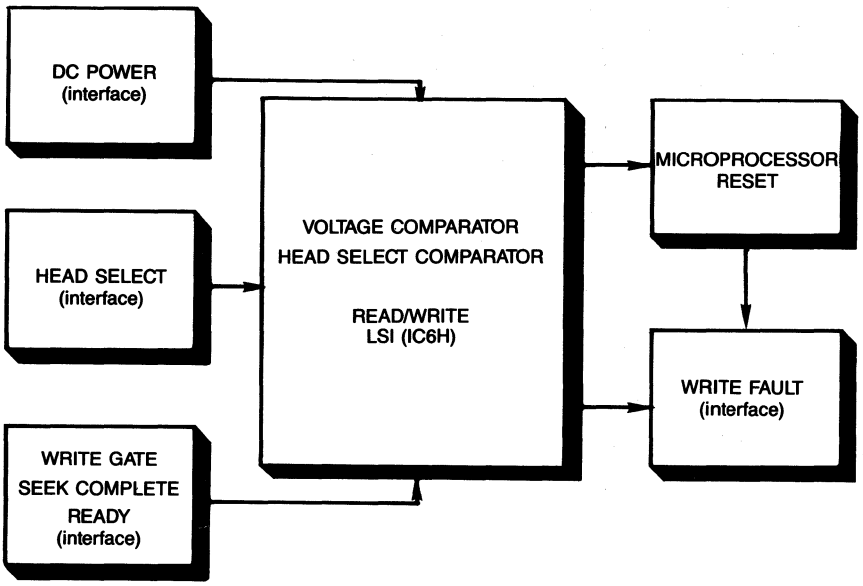


FIGURE 17: Fault Detection PC Board 20292-XXX

5.7.1 VOLTAGE AND HEAD SELECT COMPARATOR

The Read/Write LSI (IC 6H) continually monitors the +5 and +12 Volt lines for a low voltage condition. If + Volts > 15% low or +12 is > 20% low, the DC-unsafe signal is activated (IC 6H, pin 25) causing:

1. Write current to be disabled
2. The microprocessor is reset
3. The fault line is activated (IC 6H, pin 24)
4. The heads are deselected

If multiple heads are selected, the Read/Write LSI will disable the write circuitry and send a Write Fault to the interface (IC 6H, pin 24).

5.7.2 WRITE FAULT RESET

A selectable option is provided to clear a Write Fault. The standard configuration resets the Write Fault latch when Write Gate is dropped and reasserted (after the detected fault has been cleared). Shorting pins 11 and 12 at connector J9 causes the Write Fault latch to be reset when DRIVE SELECT is dropped and reasserted after the detected fault has been cleared.

FAULT DETECTION: PC BOARD 20243-XXX 5.8

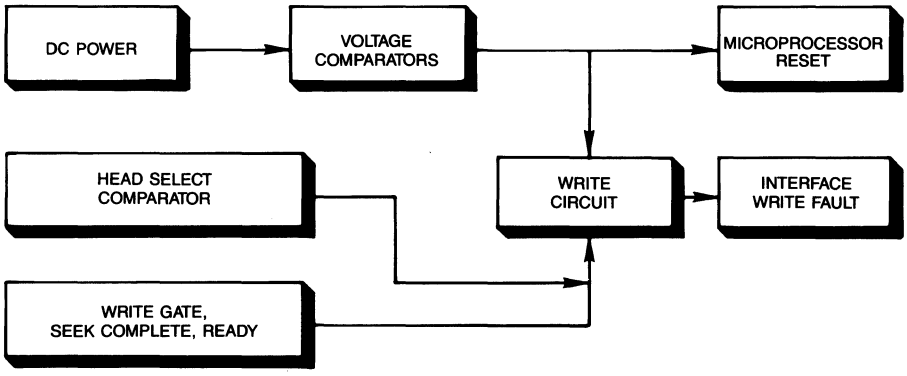


FIGURE 18: Fault Detection PC Board 20243-XXX

VOLTAGE COMPARATOR 5.8.1

Comparators at IC 7G continually monitor both the +5 and +12 Volt lines to detect a low voltage condition. If +5V is > 15% low or +12V is > 20% low, Write current will be disabled, the microprocessor reset, the fault line activated and the heads deselected.

HEAD SELECT COMPARATORS 5.8.2

When a single head is selected (normal operation), IC 7G (pins 1 and 2) will be high. If more than one head is selected, the voltage will increase at 7G (pin 4) forcing its output low. An attempt to write with no head selected will decrease the voltage at 7G (pin 4) forcing its output low. A low on either comparator will disable the Write circuitry and send a Write Fault to the interface.

6.0 READ/WRITE OPERATIONS

Two pairs of balanced signals are employed for data transfer: MFM WRITE DATA and MFM READ DATA. Data transfer lines between the host system and the drive are differential in nature and may not be multiplexed. Refer to *Table 2* for data transfer pin assignments and *Figure 6* for a host/drive interconection example.

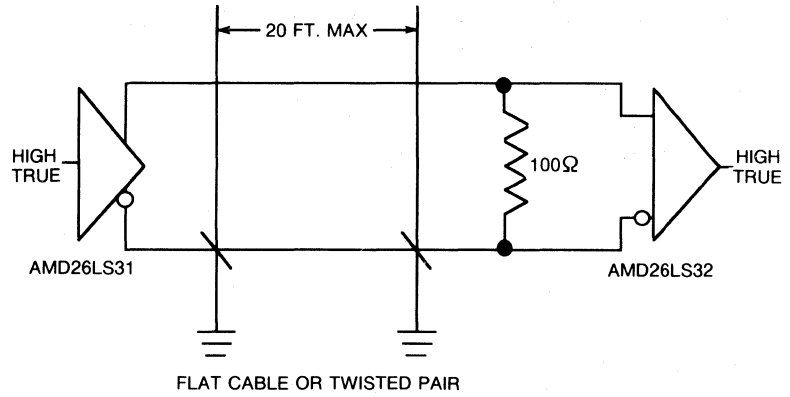


FIGURE 19: Data Signal Driver/Receiver Combination

6.1 WRITE OPERATION: PC BOARD 20292-XXX

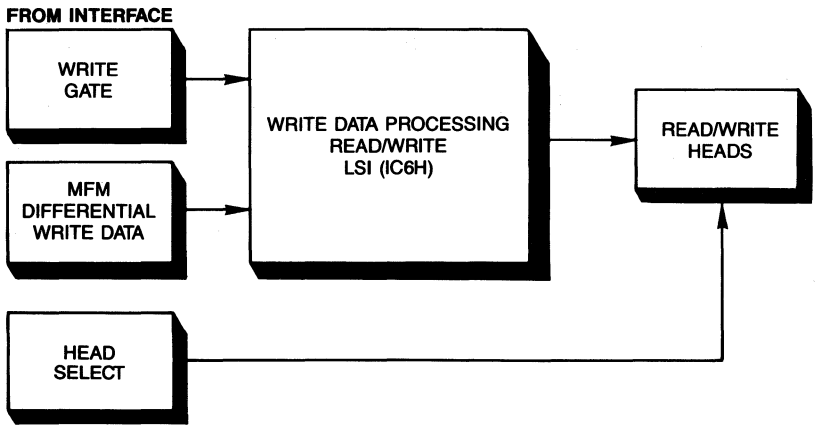


FIGURE 20: Write Operation PC Board 20292-XXX

In order to Write, the following conditions must be satisfied:

WRITE FAULT inactive
SEEK COMPLETE active
READY active
DRIVE SELECT active
Write Gate active

6.1.1 MFM WRITE DATA

WRITE DATA is transmitted by a differential pair which defines the transitions to be written on the disc. The +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line is the active transition. This signal must be driven to an inactive state when in READ mode.

WRITE GATE 6.1.2

A write sequence is initiated when Write Gate is activated which causes the Read/Write LSI (IC 6H, pin 26) to apply +12 Volts to the center tap of the selected head. Concurrently, data is sent to the Read/Write LSI, pins 15 and 16.

WRITE DATA PROCESSING 6.1.3

Differential MFM write data is received from the controller by the Read/Write LSI and changed to digital pulse data. Depending on whether plus or minus data is to be written, the Read/Write LSI (which controls the amount of current to be written) activates either pin 7 or 8 of the preamp LSI (IC 3H). When writing to the inner heads (2 and 3), Write current is reduced to lessen the problems of pulse crowding.

PRECOMPENSATION 6.1.4

Precompensation is recommended on cylinders 128 through 306 in order to achieve optimum performance. The optimum amount of precompensation is 12 nsec. for both early and late bits. *Table 3* below indicates the bit patterns and the direction to be compensated. An **X** denotes a "don't care" state.

TABLE 3: Precompensation Pattern

PREVIOUS		SENDING	NEXT	TIMING
X	0	1	1	WRITE DATA LATE
X	1	1	0	WRITE DATA EARLY
1	0	0	0	WRITE CLOCK LATE
0	0	0	1	WRITE CLOCK EARLY

ALL OTHER PATTERNS NOMINAL

6.2 WRITE OPERATION: PC BOARD 20243-XXX

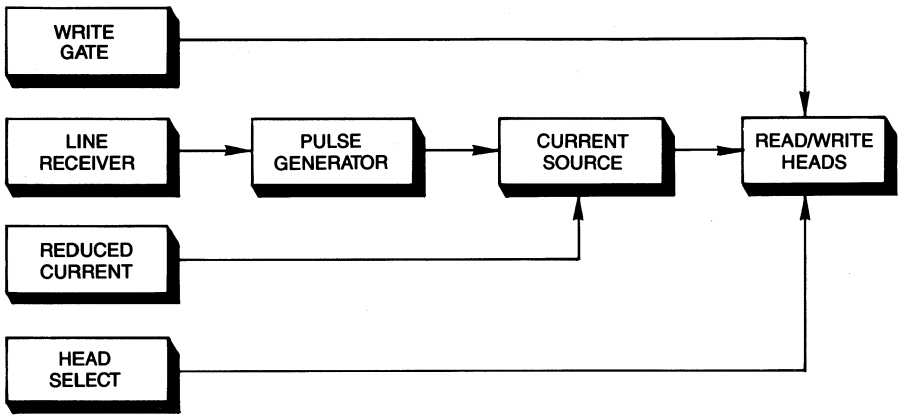


FIGURE 21: Write Operation PC Board 20243-XXX

6.2.1 WRITE GATE

A write sequence is initiated when Write Gate is activated and applies +12 Volts to the center tap of the selected head. At the same time, data is sent to the line receiver 7L.

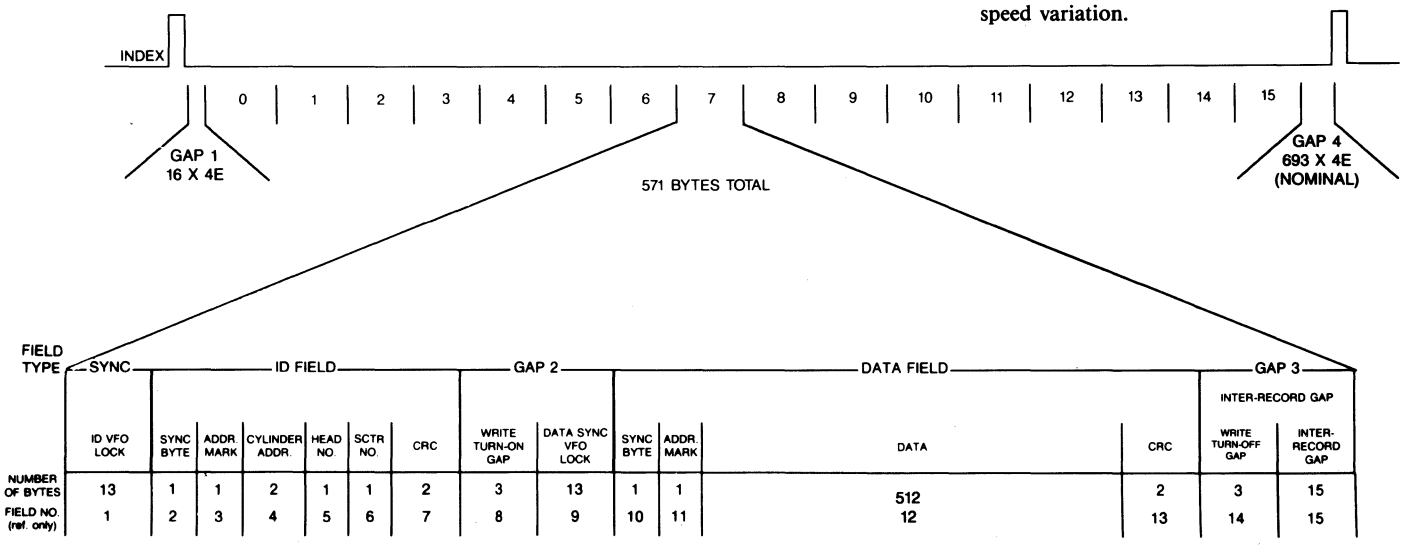
6.2.2 LINE RECEIVER

Differential Write Data (precompensated MFM) is received from the controller and changed to single line. It is then fed into the pulse generator (7K) which changes square wave data to pulse data. Depending on whether plus or minus data is to be written, either pin 7 or pin 9 of 7H is activated. The amount of current to be written is primarily established by R53. When writing to the inner heads, 2 and 3, Write current is reduced by adding R52 in parallel which reduces the problems of pulse crowding.

Figure 22 illustrates a suggested format example.

FIGURE 22: 17 Sector, 512-Byte/Sector Format Example

REFERENCE NUMBER	NUMBER OF BYTES	FIELD NAME	FIELD DESCRIPTION
1	13	ID VFO LOCK	A field of all zeros to sync the VFO for the ID
2	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows.
3	1	ADDRESS MARK	"FE" Hex defining that ID field data follows.
4	2	CYLINDER NUMBER	A numerical value in Hex defining the detent position of the actuator.
5	1	HEAD NUMBER	A numerical value in Hex defining the head selected.
6	1	SECTOR NUMBER	A numerical value in Hex defining the sector for this section of the rotation.
7	2	CRC	Cyclic Redundancy Check information used to verify the validity of the ID field information just read.
8	3	WRITE TURN-ON GAP	Zeros written during format to isolate the write splice created. This field assures valid reading of field number 7 and allows the 13 bytes required for Data VFO lock.
9	13	DATA SYNC VFO LOCK	A field of all zeros to sync the VFO for the data field.
10	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows.
11	1	ADDRESS MARK	"F8" Hex defining that user data follows.
12	512	DATA	This area available for user data.
13	2	CRC	Cyclic Redundancy Check information used to verify the validity of the user data field information just read.
14	3	WRITE TURN-OFF GAP	Zeros written during update to isolate the write splice created. This field assures valid reading of field number 13 and allows the 13 bytes required for VFO lock for the ID field of the next sector.
15	15	INTER RECORD GAP	A field of all zeros which acts as a buffer between sectors to allow for speed variation.



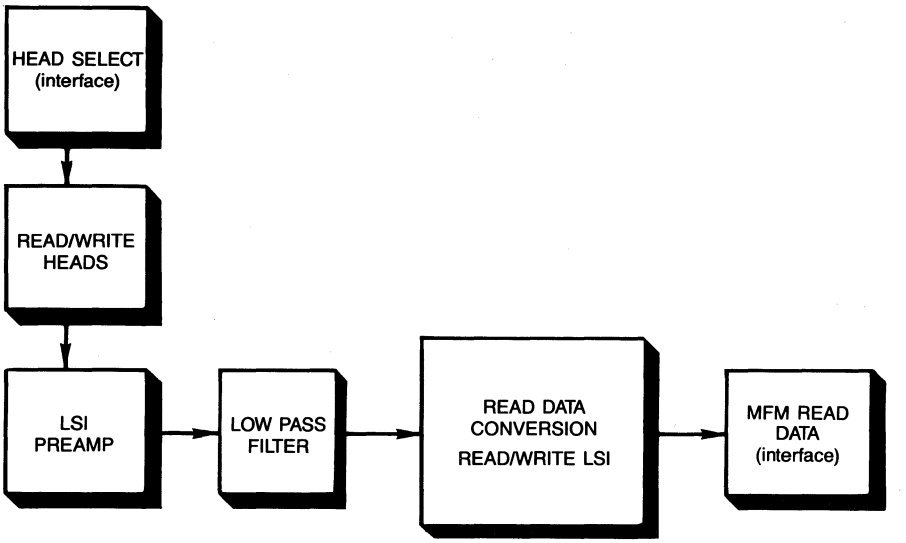


FIGURE 23:
Read Operation
PC Board 20292-XXX

6.4.1 MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system by a differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

6.4.2 HEAD SELECT

The binary decoder (IC 6G) selects the desired head based on the status of the head select lines. If the DC voltages are too low (possibly causing an inaccurate write operation), pin 12 will force the decoder to choose a nonexistent head. During read operations the head center tap is set at approximately +5 Volts by the Read/Write LSI (IC 6H, pin 27). By referencing 0 to +5 Volts, actual ground appears as −5 Volts, which eliminates the necessity of a negative power source normally required by the LSI preamp, IC 3H.

6.4.3 LSI PREAMP

With the head center tap active, data from the selected head will flow into the preamp. This preamp amplifies the read signal and also acts as a high-pass filter.

6.4.4 LOW PASS FILTER

This filter network attenuates high frequency noise, which is outside the normal data signal range.

6.4.5 READ DATA CONVERSION

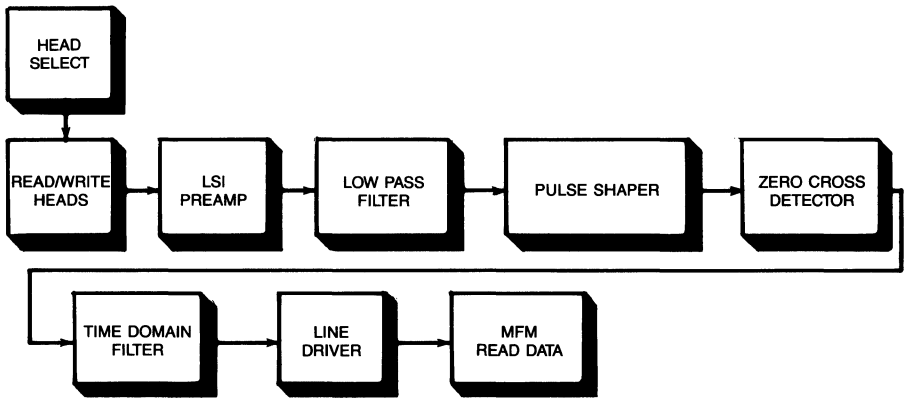
Amplified analog data enters the Read/Write LSI (IC 6H) at pins 1 and 2 and exits as differential MFM Read data at pins 17 and 18. The Read/Write LSI functions are:

1. Read data and shift 90°
2. Analog to digital conversion

3. Erroneous data bits removed
4. Conversion of digital data EIA RS-422 to compatible differential data thereby providing immunity to common mode noise during transmission

READ OPERATION: PC BOARD 20243-XXX 6.5

FIGURE 24: Read Operation PC Board 20243-XXX



HEAD SELECT 6.5.1

The binary decoder (IC 5H) selects the desired head based on the status of the head select lines. If the DC voltages are too low (possibly causing an inaccurate write operation), pin 12 will force the decoder to choose a nonexistent head. During read operations the head center tap is set at approximately +5 Volts by Zener Diode CR2. By referencing 0 to +5 Volts, actual ground appears as −5 Volts, which eliminates the necessity of a negative power source normally required by the LSI preamp.

LSI PREAMP 6.5.2

With the head center tap active, data from the selected head will flow into the preamp. This preamp amplifies the read signal and also acts as a high pass filter.

LOW PASS FILTER 6.5.3

This filter network attenuates high frequency noise, which is outside the normal data signal range.

PHASE SHIFTER 6.5.4

Amplified data enters the circuit and is shifted 90° so peak data, which was detectable over a fairly broad range, is now moved to a highly sloped accurately detectable position at the zero crossing.

ZERO CROSS DETECTOR 6.5.5

This element detects bit position as the slope of read data signals crosses the zero threshold. At this point analog signals are changed to digital.

6.5.6 TIME DOMAIN FILTER

When a high resolution head reads a low frequency pattern, there is a tendency for the head signal to decay between bits. If this decay falls below the zero cross threshold, a spurious data bit will be generated. Such false bits are ignored by delaying the clocking data bit (IC 6L) past the potential point of highest drop.

6.5.7 LINE DRIVER

At this point raw digital data is changed to differential data providing immunity to common mode noise during transmission.

7.0 MICRO-PROCESSOR

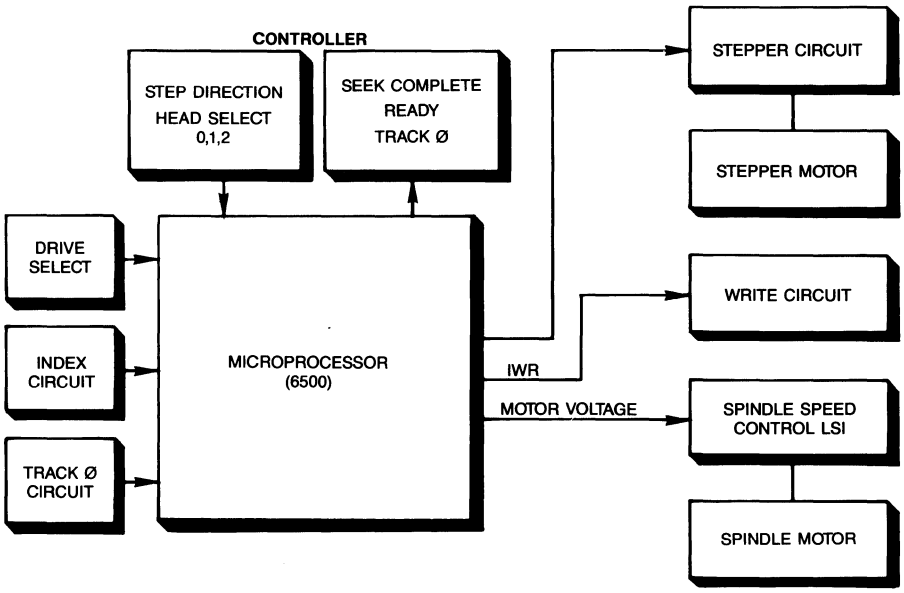


FIGURE 25: MPU: PC Board 20292-XXX

The microprocessor monitors and controls the internal drive functions and the host interface lines. The MPU has only three active modes: **Initializing, Seeking, Waiting.**

As the drive spins-up, 660 revolutions are counted before the MPU assumes that the drive is at nominal speed. The drive then initiates recalibration. If the heads are not over Track Ø, the drive will step at 3 msec./track. When both mechanical Track Ø and electrical phase A are present, the heads are at true Track Ø and stepping will cease.

Within 20 msec. both SEEK COMPLETE, Track Ø and READY will go true and the drive is then ready to accept inputs from the controller.

When in the idle mode, the MPU loops, waiting for step pulses. The MPU also monitors its reset line (pin 39) for a low signal from IC 4D, which causes the MPU to reinitialize.

Upon receiving a step pulse, the MPU pauses for 500 μsec., to allow for additional pulses, before executing the seek operation. Every incoming pulse will reset the 500 μsec. timer. The seek will not begin until the last pulse is received.

When seeking, the MPU counts the number of tracks to be covered and searches the PROM for the optimum acceleration/deceleration algorithim. Steps are accomplished by setting IC1A to sequential phases. It provides both a current source and sink with the motor windings. Near the end of a seek, IC 1C and 2A are set to provide additional current to offset hysteresis.

Upon completion of a seek operation settling time is calculated, based upon the length of the seek, and the interface line is activated in the specified time period. With SEEK COMPLETE, the MPU returns to the idle mode.

Whenever a seek operation crosses the write current boundary switch at Track 128, the MPU reduces the write current to eliminate pulse crowding during write operations.

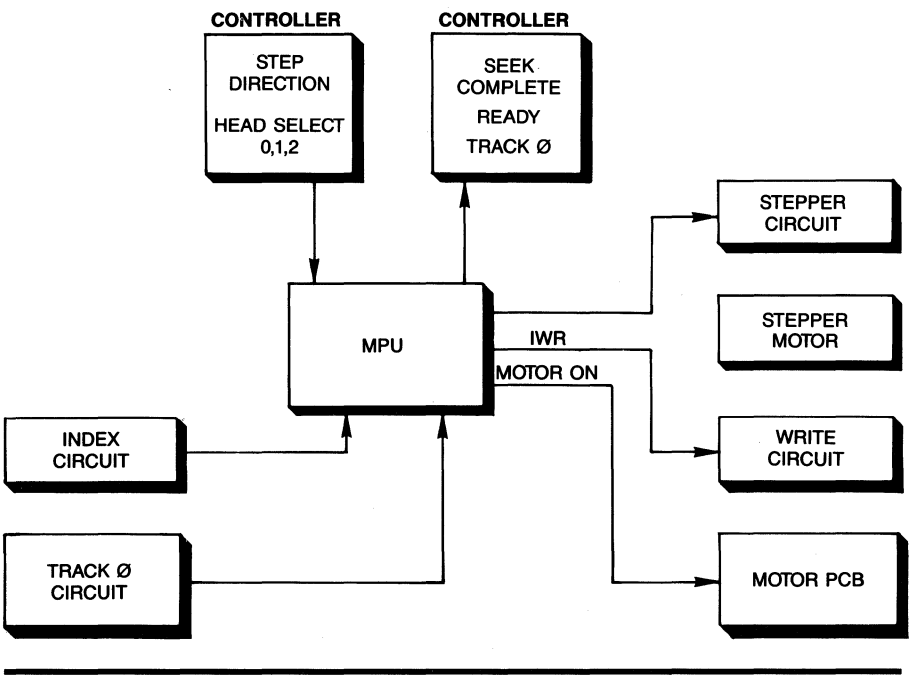


FIGURE 26: MPU: PC Board 20243-XXX

The microprocessor monitors and controls the internal drive functions and the host interface lines. The MPU has only three active modes: **Initializing, Seeking, Waiting.**

At power-on the MPU initializes the stepper circuit to phase A and resets all interface lines under its control. Power is then applied to the Motor Control PCB and the Index line is monitored for spindle rotation. If rotation is not sensed within 15 seconds, the MPU removes power.

As the drive spins-up, 660 revolutions are counted before the MPU assumes that the drive is at nominal speed. The drive then initiates recalibration. If the heads are not over Track Ø, the drive will step at 3 msec./track. When both mechanical Track Ø and electrical phase A are present, the heads are at Track Ø and stepping will cease.

Within 20 msec. both SEEK COMPLETE, Track Ø and READY will go true and the drive is then ready to accept inputs from the controller.

When in the idle mode, the MPU loops, waiting for step pulses. The MPU also monitors power and, should the power drop by approximately 20%, it will revert to the initialization routine described above.

Upon receiving a step pulse, the MPU pauses for 500 μsec., to allow for additional pulses, before executing the seek operation. Every incoming pulse will reset the 500 μsec. timer. The seek will not begin until the last pulse is received.

When seeking, the MPU counts the number of tracks to be covered and searches the PROM for the optimum acceleration/deceleration algorithim.

Steps are accomplished by setting IC 1A to sequential phases. It provides both a current source and sink with the motor windings. Near the end of a seek, ICs 4A and 4B are set to provide additional current to offset hysteresis.

Upon completion of a seek operation settling time is calculated, based upon the length of the seek, and the interface line is activated in the specified time period. With SEEK COMPLETE, the MPU returns to the idle mode.

Whenever a seek operation crosses the write current boundary switch at Track 128, the MPU reduces the write current to the heads to eliminate pulse crowding during write operations.

8.0 MOTOR SPEED CONTROL

MOTOR SPEED CONTROL: PC BOARD 20292-XXX 8.1

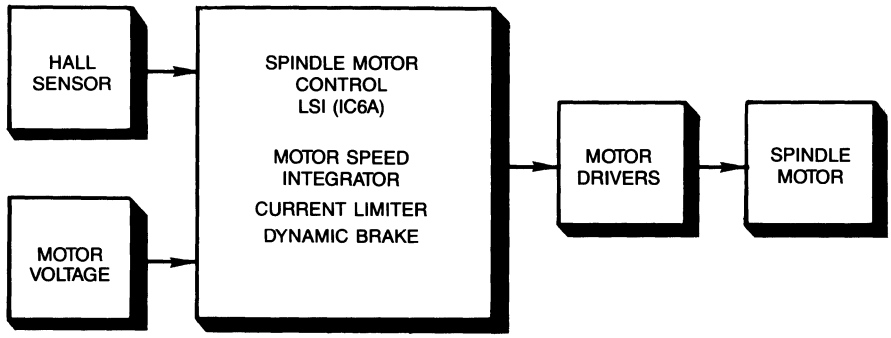


FIGURE 27: Motor Speed Control: PC Board 20292-XXX

HALL EFFECT TRANSDUCER 8.1.1

Located inside the spindle motor hub, this magnetic transducer senses spindle position and provides dynamic feedback proportional to the speed of the motor. Two complete square waves are generated each motor revolution. The positional information is supplied to the spindle motor LSI IC 6A (pin 3). To prevent both phases of the motor from being selected simultaneously, the motor control LSI inverts Hall input to coil A.

SPINDLE MOTOR CONTROL LSI 8.1.2

When power is applied to the drive the motor control LSI pauses until 10 Volts is reached before applying current to the motor drive transistors. If 10 Volts is not achieved within approximately 1 second the motor control LSI will time-out and will not apply power to the motor drive transistors.

When current is applied, the spindle motor control LSI sets the motor speed to 3,600 RPM nominal. The motor speed is crystal controlled (Y1) with a frequency lock circuit. There is no adjustment required for motor speed. The LSI integrates and transforms the error messages from the Hall effect transducer. Using this information, it outputs the correct current flow each revolution and corrects the motor phase driver at output pins 6 and 7.

When power is interrupted, the motor control LSI shorts both phases of the motor to ground allowing the motor-generated back-EMF to brake the spindle motor.

MOTOR SPEED CONTROL PC BOARD: 20249-XXX 8.2

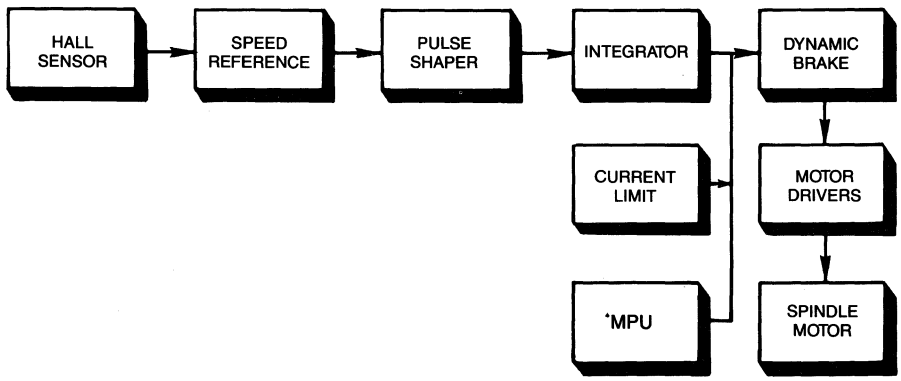


FIGURE 28: Motor Speed Control PC Board 20249-XXX

8.2.1 HALL EFFECT TRANSDUCER

This magnetic transducer is located within the spindle hub. It senses spindle position and provides dynamic feedback proportional to motor speed. Two complete square waves are generated for each revolution. This positional information is supplied to both the speed reference circuits and motor driver control transistors. To prevent both phases of the motor from being selected simultaneously, transistor 2A inverts the Hall input to coil A.

8.2.2 SPEED REFERENCE CIRCUIT

Using the charge time of C5 as a standard, comparator 1A, pin 2, will output a low pulse indicative of speed error. The charge time of C5 is set at the factory by adjusting R2 to 3,600 RPM nominal.

8.2.3 PULSE SHAPER

This circuit smooths out the incoming error pulses for ease of integration.

8.2.4 INTEGRATOR

Speed error information is integrated and transformed into usable levels by IC 1A (pin 7) whose output determines the current flow per revolution through each motor phase.

8.2.5 CURRENT LIMIT

Transistor Q6 senses the current level drawn during motor start-up and limits it to 3.5 Amps by controlling the "on time" of 2A (pins 3, 12).

8.2.6 MICROPROCESSOR: MOTOR ON

This signal is maintained low by the microprocessor as long as the index sensor indicates motor spin-up within a specified period. If the motor does not rotate the signal is set high and motor current is removed. This circuit prevents damage to the PCB and motor if, for some reason, rotation cannot occur.

8.2.7 MOTOR DRIVERS

Current is supplied to both motor phases by IC 3A. Hall information is used to supply current to the correct phase, while the integrator error information controls the current level.

8.2.8 DYNAMIC BRAKE

At power on C12 is charged up. When power is interrupted, C12 becomes the source keeping Q1, Q2 and Q3 on. At this time, transistor Q3 shorts both motor phases to ground allowing motor generated EMF to bring the spindle to a stop.

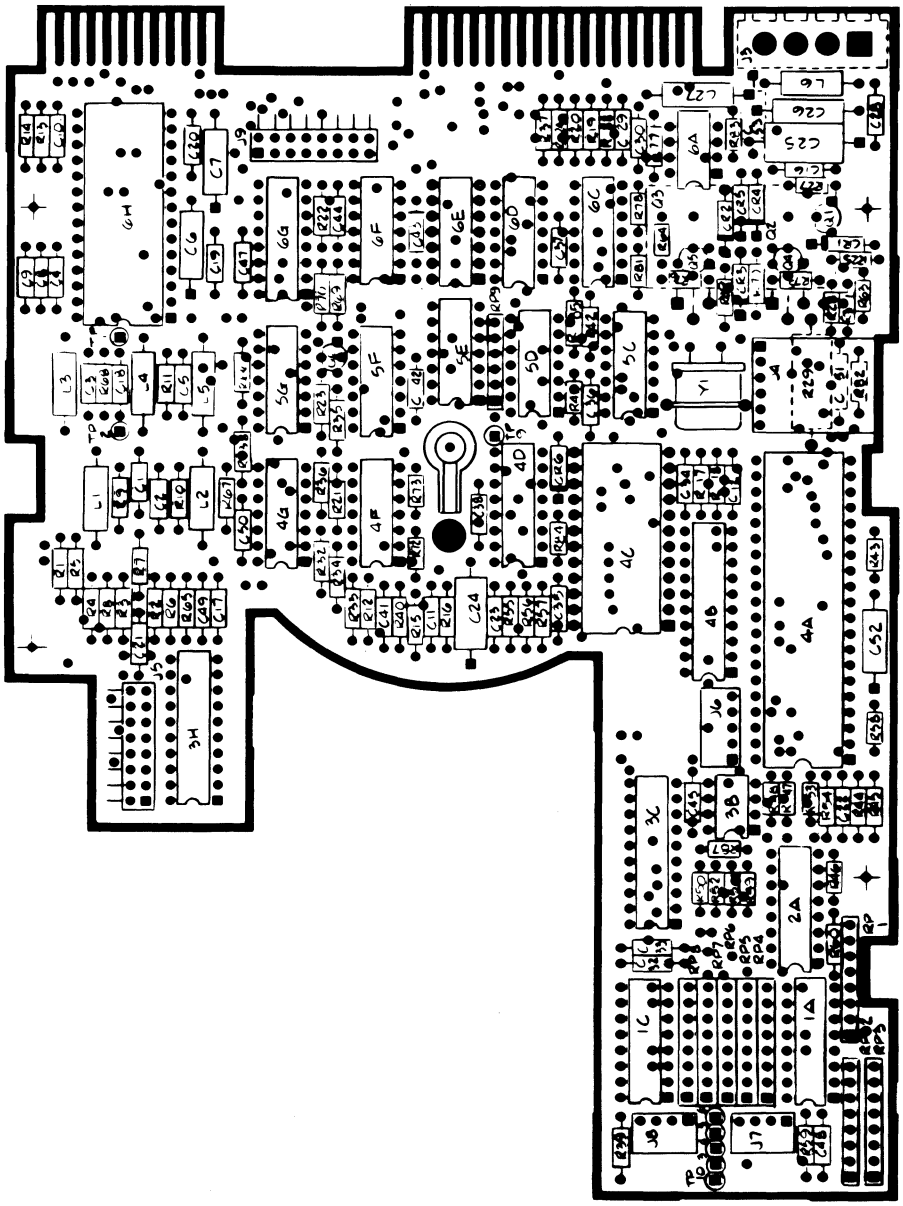
9.0 FIELD SERVICE

The ST212 does not require any preventative maintenance. The HDA is sealed and Seagate will consider a unit to be out of warranty if the seal has been broken. Should a drive require service, consult your distributor or your regional field sales office.

Rough handling accounts for more Winchester drive damage than all other factors combined. Your ST212 is designed for consistent and reliable service across a wide range of environmental factors. It is, however, a precision instrument and when transporting or shipping a unit please ensure that the drive is correctly packed in the original Seagate (or approved substitute) container.

TEST POINT DATA: PC BOARD 20292-XXX 9.1

FIGURE 29: Test Point Locations PC Board 20292-XXX



9.1.1 DIFFERENTIAL READ FILTER: TEST POINTS 1 AND 2

These points may be used to moinitor Differential Read Data. The typical amplitude of the signal resulting from adding the two channels is 160 mVolts. This signal is observed at Cylinder Zero, head 0 or 1. A full track record of high frequency data (0000 or 1111) will typically resemble *Figure 30.*

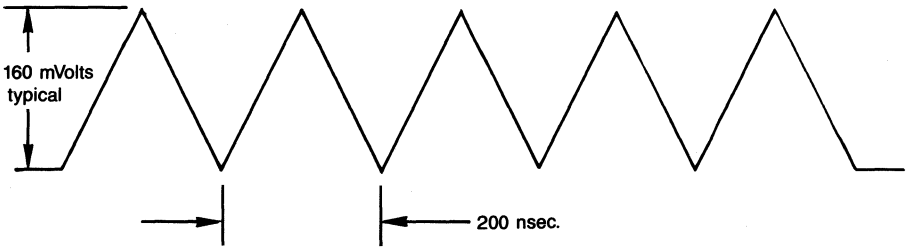


FIGURE 30: Differential Read Filter

9.1.2 TRACK Ø SENSOR: IC 3B, PIN 1

IC 3B, pin 1 may be used to monitor the Track Ø sensor. A high logic level indicates valid Track Ø. The microprocessor requires the stepper motor to be at phase A and the Read/Write heads to be at Cylinder Zero before it will output a valid Track Ø signal.

9.1.3 INDEX SENSOR: TEST POINT 9

Test point 9 may be used to monitor the Index sensor. Only the leading edge of the pulse is valid. A typical signal will resemble *Figure 31.*

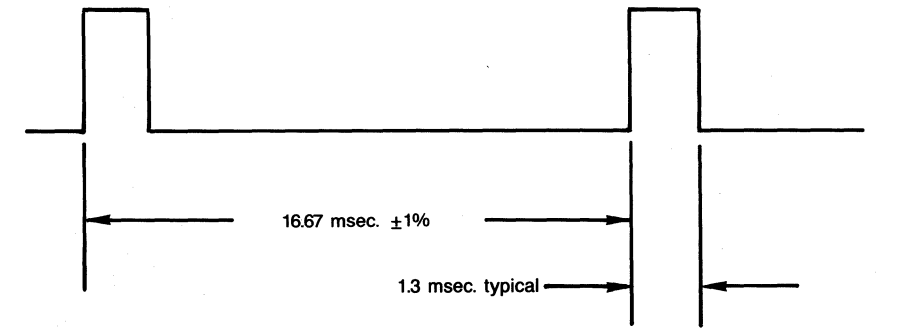
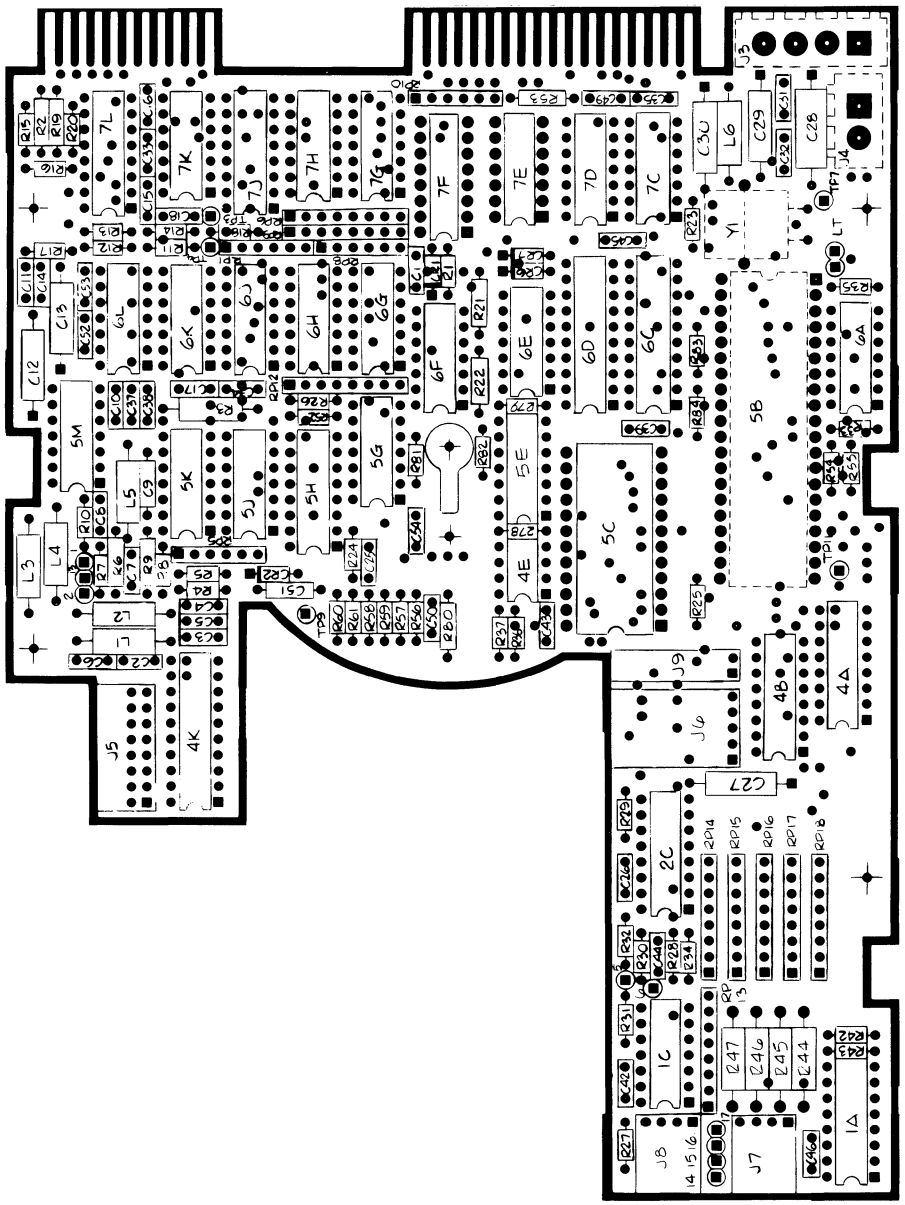


FIGURE 31: Index Sensor

FIGURE 32:
Test Point Locations
PC Board 20243-XXX



DIFFERENTIAL READ FILTER: TEST POINTS 1 AND 2 9.2.1

These points may be used to monitor Differential Read Data. The typical amplitude of the signal resulting from adding the two channels is 160 mVolts. The signal is observed at Cylinder Zero, head 0 or 1. A full track record of high frequency data (0000 or 1111) will typically resemble *Figure 30.*

9.2.2 READ DATA: TEST POINTS 3 AND 4

These points may be used to monitor Read data from the operation of the time domain filter. Trigger off test point 4 and monitor the delay at test point 3. Typically, a 120 nsec. delay will be observed. A full track record of high frequency data (0000 or 1111) will resemble *Figure 33.*

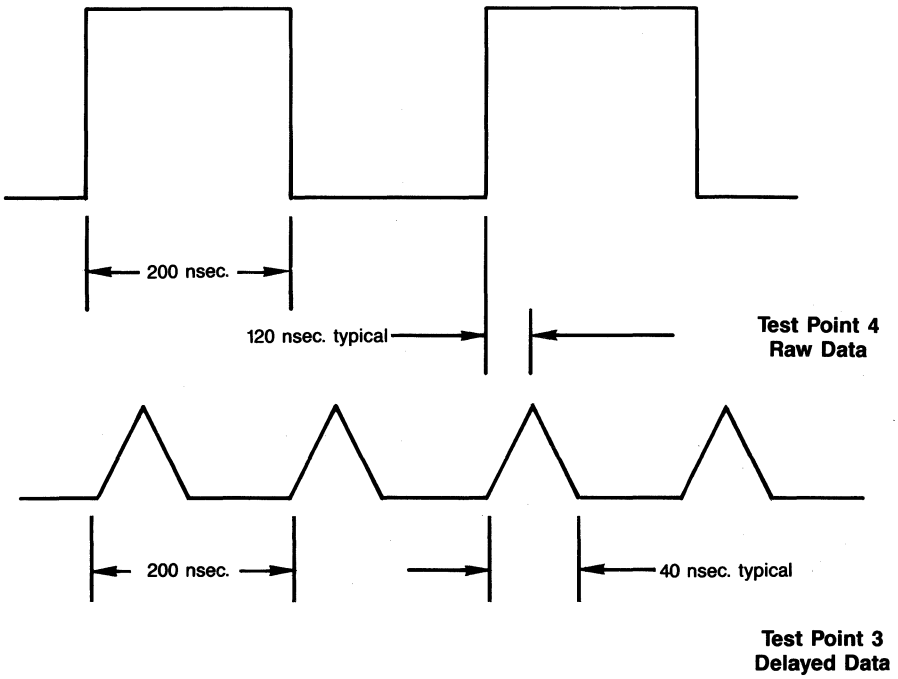


FIGURE 33: Read Data

9.2.3 TRACK Ø: TEST POINT 5

The Track Ø sensor may be monitored at Test Point 5. A high logic level indicates valid Track Ø. The stepper motor must be at Phase A and the Read/Write heads at Cylinder Zero before a valid Track Ø signal will be issued.

9.2.4 INDEX SENSOR: TEST POINT 6

Test point 6 may be used to monitor the Index Sensor. Only the leading edge of the pulse is valid. A typical signal will resemble *Figure 31.*

Test point 6 is used to monitor the spindle motor during speed adjustment. Adjust at R3 (MLC-00, access through the side of the frame) for a period of 16.67 msec. ±1%.

9.3 FIELD ACCESSIBLE COMPONENTS

The procedures covered in this section may be completed without special tools or cleanroom facilities. There are no user-serviceable components inside the head/disc assembly (HDA). The HDA is sealed and Seagate will consider a drive to be out of warranty if the seal is broken.

MAIN CONTROL PC BOARD 9.3.1

Required Tools: T-10 Torx driver or standard blade screwdriver

Rest the drive on a padded surface, oriented with the PCB up and the edge-connectors to your right. Refer to *Figure 34.*

1. Disconnect the Motor Control Board power connector, P3 (MLC-00 only).
2. Remove and retain the four PCB mounting screws.
3. Disconnect the printed circuit cable connector, P5. Do not crease the cable.
4. Disconnect and free the spindle motor connection, P4.
5. Lift the board, allowing the far edge to clear the frame, and disconnect the Index/LED connector, P6.
6. Disconnect stepper motor (P7) and the Track Ø sensor (P8) connections.
7. Lift out the PCB.

Note: It is recommended that a replacement PCB be powered-up with the head cable, P5, disconnected. This will insure that if the replacement is damaged it not alter data on the disc. Avoid creasing the cable and inspect after this operation.

MOTOR CONTROL PC BOARD REMOVAL (MLC-00 ONLY) 9.3.2

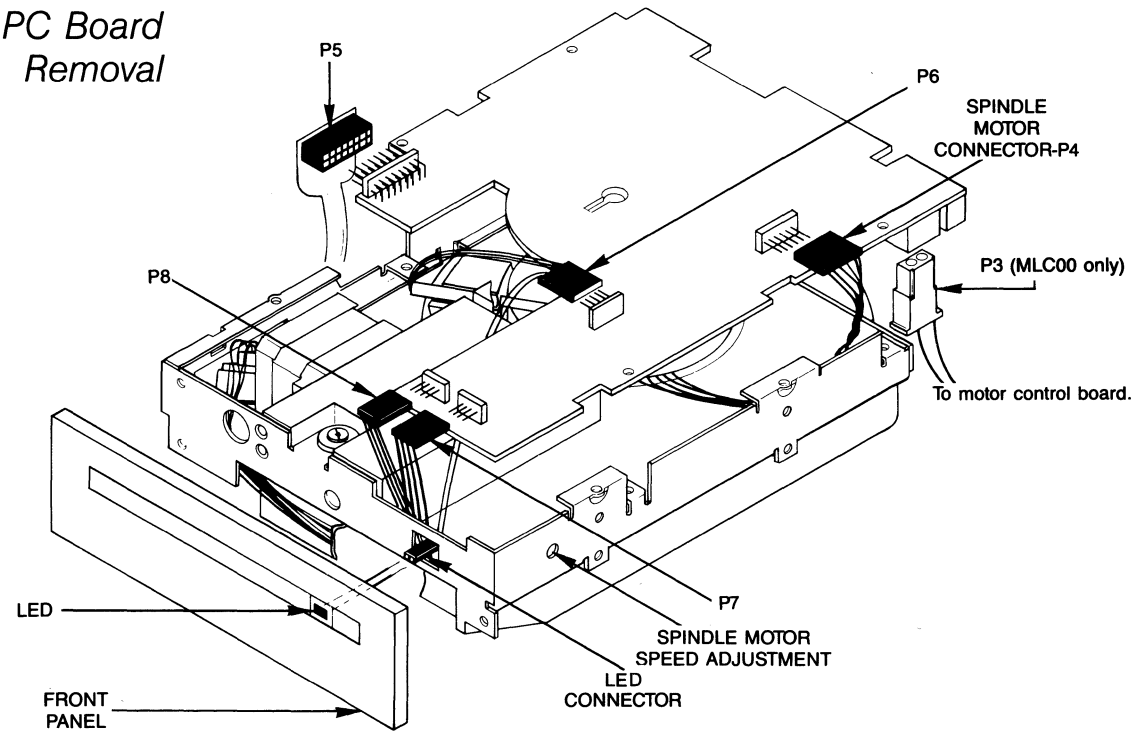
If the motor control board is replaced, the spindle speed must be adjusted. Refer below for adjustment procedure.

Required Tools: T-10 Torx driver or standard blade screwdriver.

1. Remove the Main Control PCB. See *Section 9.3.1.*
2. Disconnect the spindle motor connector.
3. Remove the two mounting screws and lift out the board.

Spindle Speed Adjustment: Warm the drive up for five minutes. Connect a frequency counter to the Index test point and adjust the spindle motor control trimpot (See *Figure 34*) for a period of 16.67 msec. ± 1%. the counter must average 100 samples per minute minimum.

FIGURE 34: ST212 PC Board Removal



9.3.3 INDEX SENSOR REMOVAL

Required Tools: T-10 Torx driver or standard blade screwdriver, 0.030″ shim

1. Remove the Main Control PCB. See *Section 9.3.1.*
2. Disconnect the Front Panel LED. See *Figure 35.*
3. Remove the sensor bracket mounting screw.
4. To install replacement, apply Loctite to the first three threads of the mounting screw. Position the sensor, clamp and screw, but do not tighten.
5. Rotate the spindle motor clockwise until the silver tab aligns with the sensor.
6. Using the shim, verify that the gap is .030″. Tighten the screw.

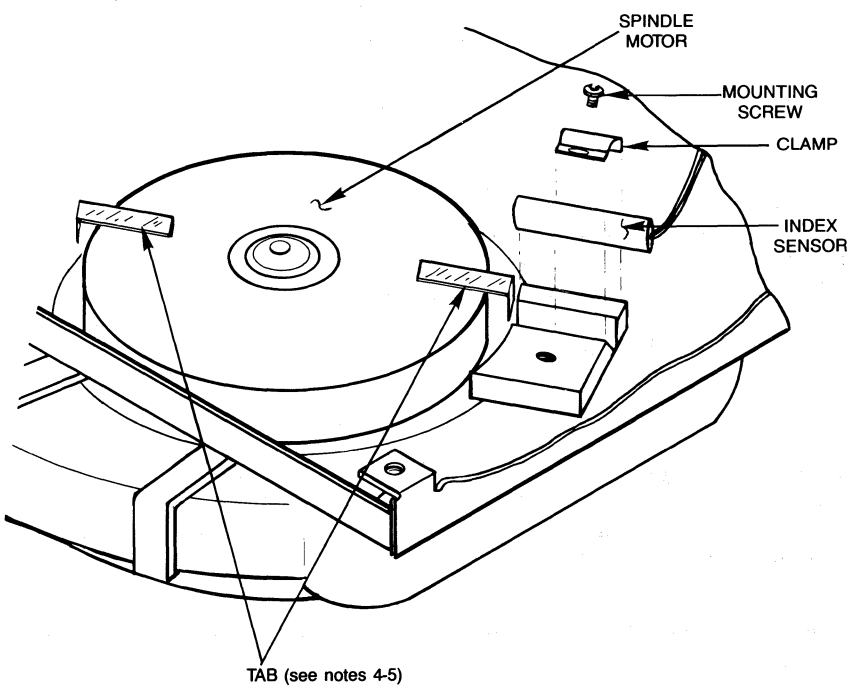


FIGURE 35: Index Sensor Adjustment/Removal

9.3.4 INSTALLING THE OPTIONAL FULL-HEIGHT FRONT PANEL

Required Tools: T-10 Torx driver

Depending on how the unit was shipped from the factory, the unit may have a half-height Front Panel already installed. To remove:

1. Remove the Main Control PCB. See *Section 9.3.1.*
2. Disconnect the LED. Refer to *Figure 34.*
3. Remove the two mounting screws.
4. Reverse the procedure to install the replacement cover.

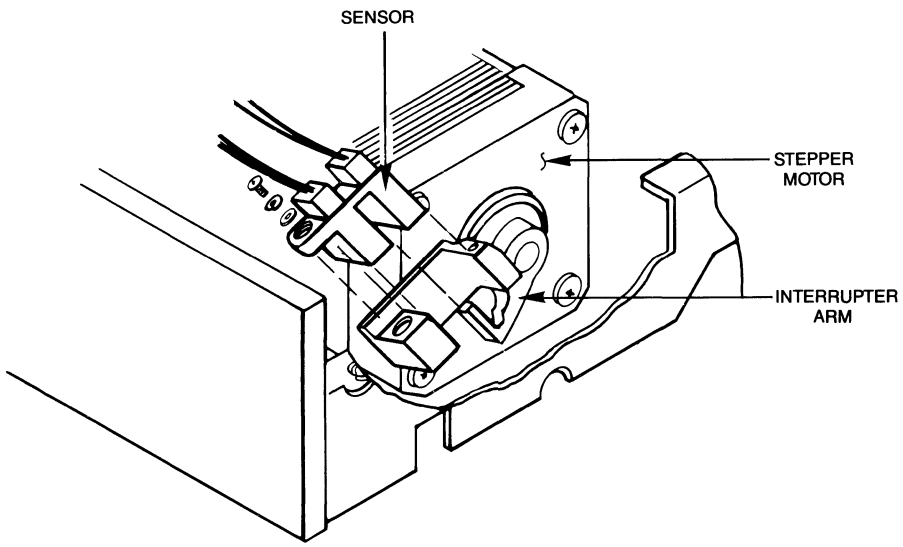
TRACK Ø SENSOR REMOVAL 9.3.5

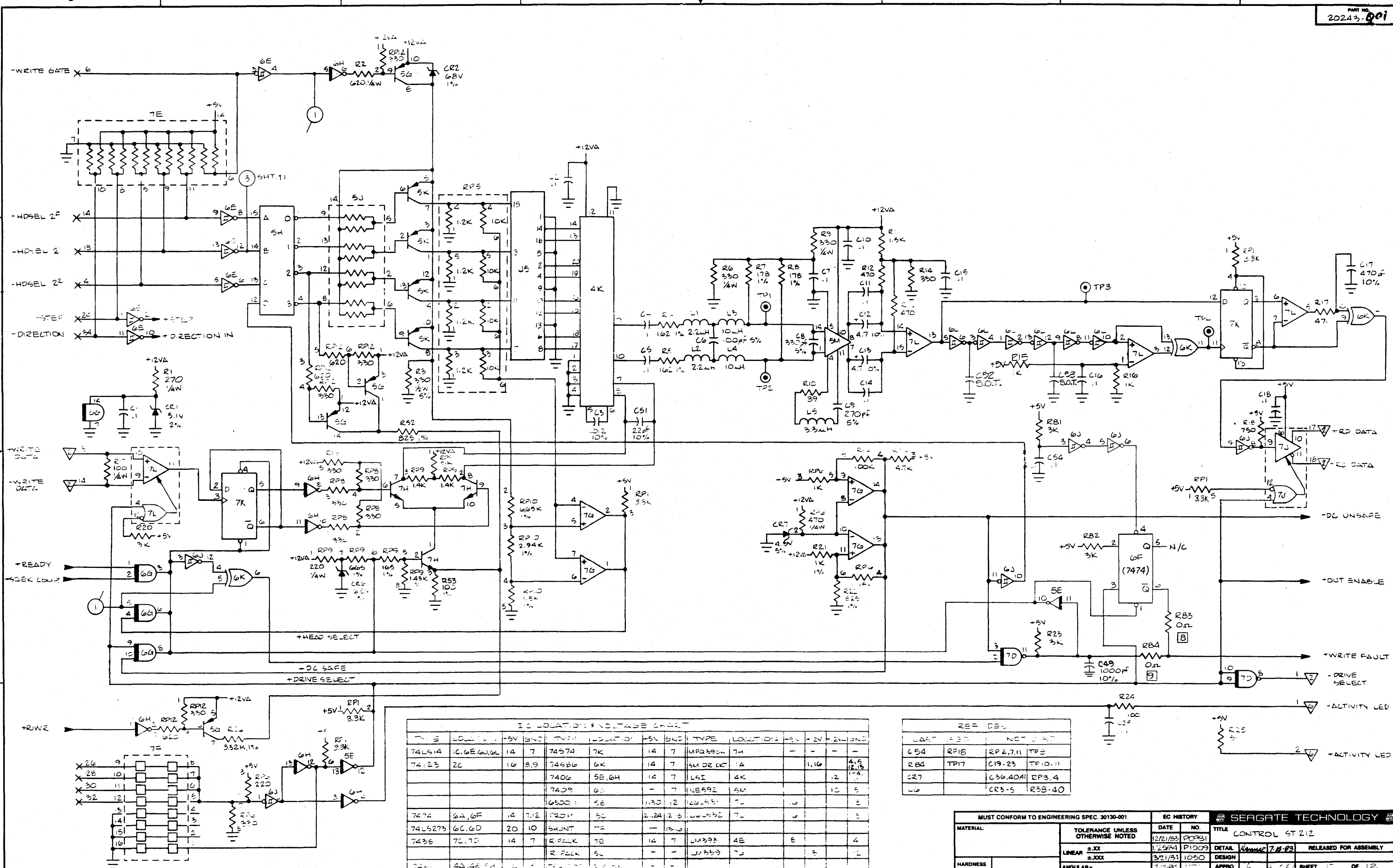
Required Tools: T-7 Torx driver, Loctite™ #242

Proper positioning of this sensor is essential. The Interrupter Arm set screw is set at the factory and should not be tampered with.

1. If installed, remove the Front Panel.
2. Disconnect the Track Ø Sensor connector, P8. Slide the wires down between the casting and the frame. Free the harness from the white retaining clip on the casting. Refer to *Figure 36.*
3. Remove the sensor. Do not tamper with the Interrupter Arm set screw. This is set and sealed at the factory.

FIGURE 36: Track Ø Sensor Removal

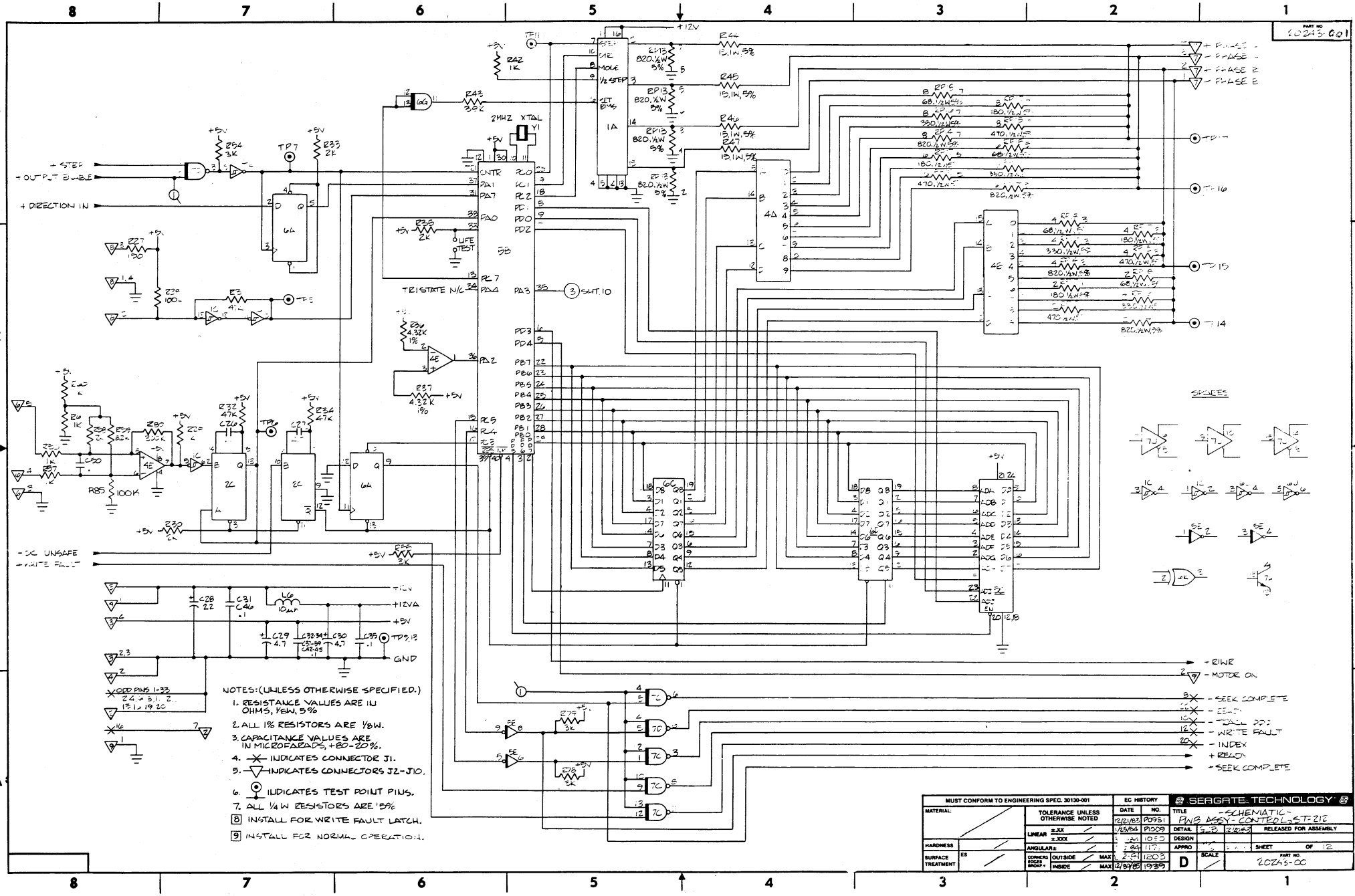




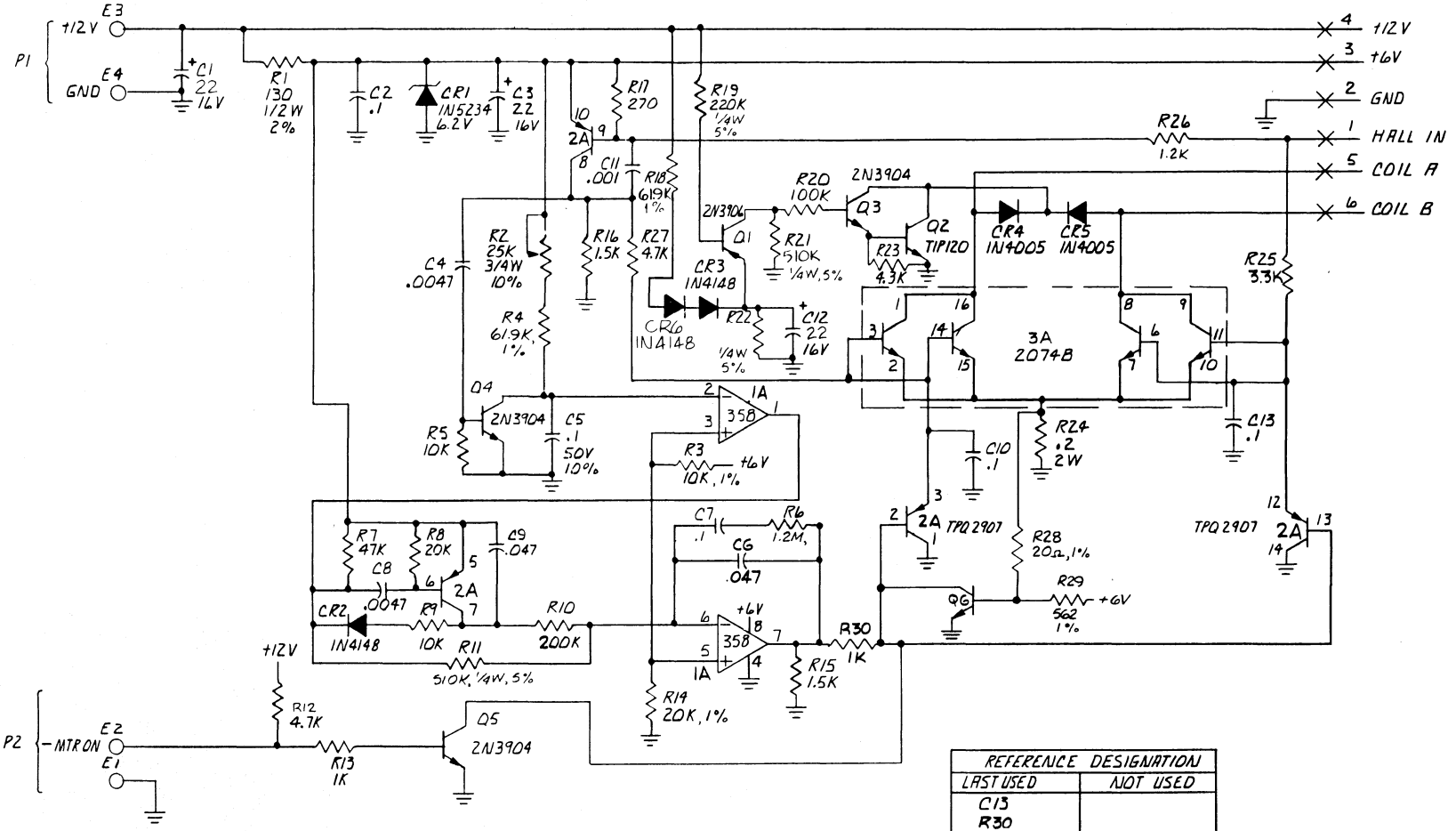
IC LOCATION & VOLTAGE CHART													
TYPE	LOCATION	+5V	GND	TYPE	LOCATION	+5V	GND	TYPE	LOCATION	+5V	+12V	+12VA	GND
74LS14	1C,6E,6J,6L	14	7	74S74	7K	14	7	MPQ3904	7H	–	–	–	–
74123	2C	16	8,9	74S86	6K	14	7	SM DR CKT	1A		1,16		4,5 12,13
				7406	5E,6H	14	7	LSI	4K			12	1-4, [illegible]
				7409	6G	–	7	NE592	5M			10	5
				6500 [illegible]	5E	1,30	12	[illegible]	7J	[illegible]			[illegible]
7474	6A,6F	14	7,12	PROM	5C	2,24	12 [illegible]	[illegible]	7L	[illegible]			[illegible]
74LS273	6C,6D	20	10	SHUNT	7F	—	13,[illegible]						
7438	7C,7D	14	7	R/PACK	7E	14	7	LM393	4E	8			4
				R/PACK	5J	–	–	LM339	7G		3		12
[illegible]	4A,4E [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	–	–						

REF DES			
LAST USED		NOT USED	
C54	RP18	RP2,7,11	TP5
R84	TP17	C19-23	TP10,11
CR7		C36,40A11	RP3,4
L6		CR3-5	R38-40

MUST CONFORM TO ENGINEERING SPEC. 30130-001		EC HISTORY	SEAGATE TECHNOLOGY
MATERIAL:	TOLERANCE UNLESS OTHERWISE NOTED	DATE / NO.	TITLE CONTROL ST 212
	LINEAR ±.XX	12/21/83 P0931	
		1/25/84 P1009	DETAIL [illegible] 7-18-83 RELEASED FOR ASSEMBLY
	LINEAR ±.XXX	3/21/84 1050	DESIGN
HARDNESS	ANGULAR±	[illegible] [illegible]	APPRO [illegible] SHEET 12 OF 12
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX	[illegible] 1203	D SCALE PART NO.
	INSIDE MAX	12/30/85 1939	20243-001


+STEP
+OUTPUT ENABLE
+DIRECTION IN
TRISTATE N/C
LIFE TEST
2MHZ XTAL
+12V
+5V
-DC UNSAFE
+WRITE FAULT
NOTES:(UNLESS OTHERWISE SPECIFIED.)
1. RESISTANCE VALUES ARE IN OHMS, ¼W, 5%
2. ALL 1% RESISTORS ARE ⅛W.
3. CAPACITANCE VALUES ARE IN MICROFARADS, +80-20%.
4. INDICATES CONNECTOR J1.
5. INDICATES CONNECTORS J2-J10.
6. INDICATES TEST POINT PINS.
7. ALL ¼ W RESISTORS ARE 5%
8 INSTALL FOR WRITE FAULT LATCH.
9 INSTALL FOR NORMAL OPERATION.
SPARES
+RWR
-MOTOR ON
-SEEK COMPLETE
-INDEX
+READY
+SEEK COMPLETE
-SCHEMATIC-
PWB ASSY-CONTROLLER
SEAGATE TECHNOLOGY
MUST CONFORM TO ENGINEERING SPEC. 30130-001
EC HISTORY
RELEASED FOR ASSEMBLY
SIZE D
SCALE
SHEET OF 12
PART NO. 20243-001

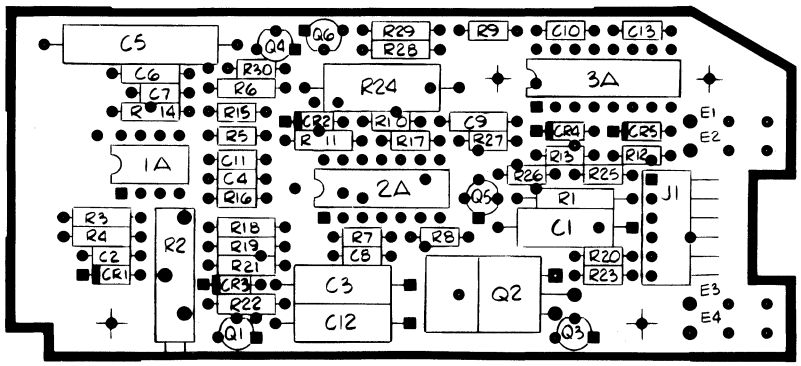
PART NO 20249-001



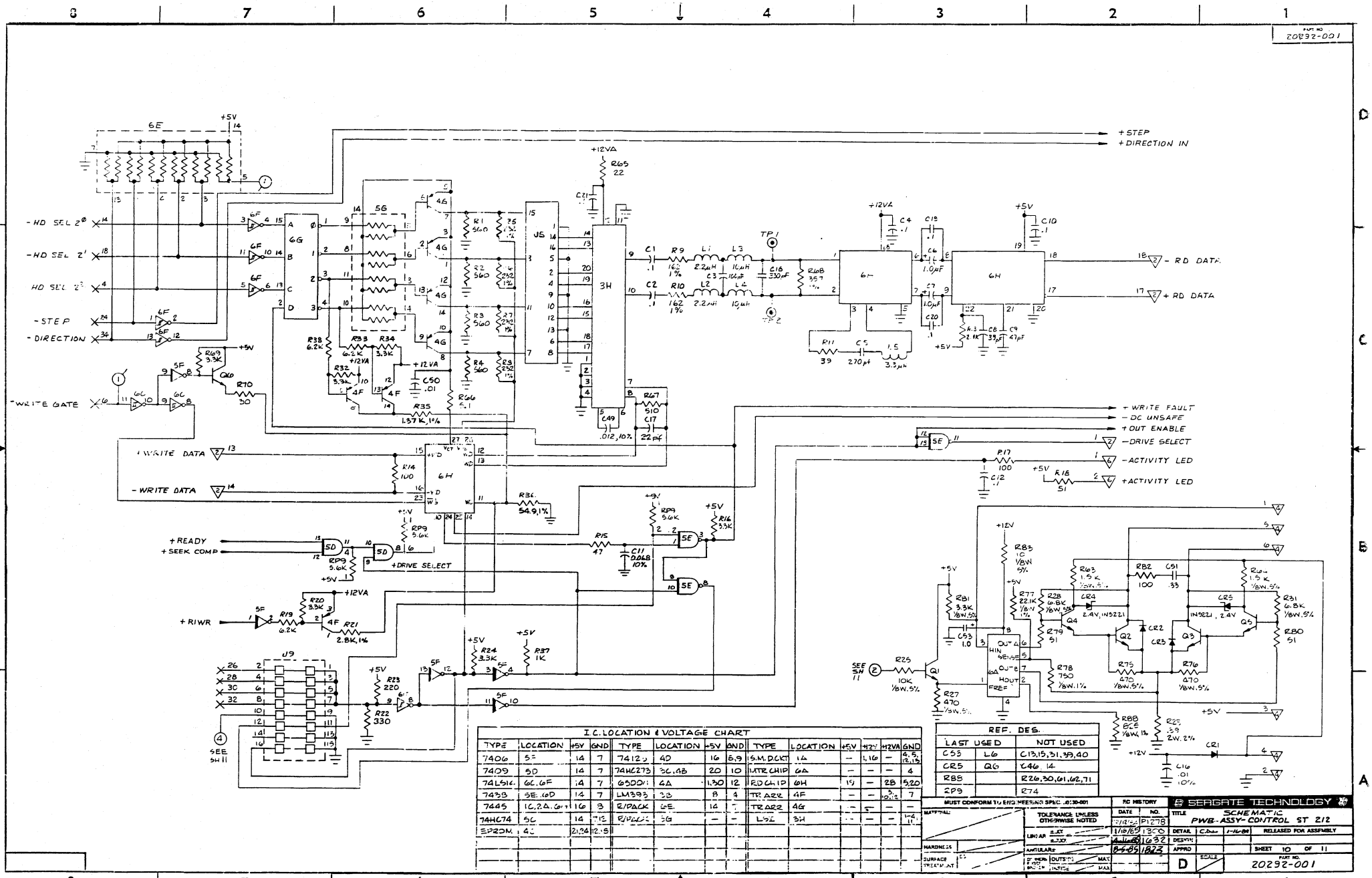
REFERENCE DESIGNATION	
LAST USED	NOT USED
C13 R30 CR6 Q6 3A	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS 1/8W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS 10%.
3. ✕ INDICATES J1.

MUST CONFORM TO ENGINEERING SPEC. 30130-001		EC HISTORY		SEAGATE TECHNOLOGY	
MATERIAL:	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	SCHEMATIC PWB ASSY MOTOR CONTROL ST 212
	LINEAR ± .XX	12/20/83	G		
	± .XXX	2/15/84	H	DETAIL	RELEASED FOR ASSEMBLY 8-12-83
HARDNESS	ANGULAR ±	9/18/84	1190	DESIGN	
SURFACE TREATMENT EB	CONTACT AREA BROKEN OUTSIDE MAX	1-7-85	1389	APPRO	SHEET 7 OF 7
	INSIDE MAX	4-17-85	1684	C	SCALE — PART NO. 20249-001


C5
Q4
Q6
R29
R28
R9
C10
C13
C6
C7
R14
R30
R6
R24
3Δ
E1
E2
R15
R5
C8
R11
R10
R17
C9
R27
C11
C4
R16
1Δ
2Δ
Q5
R1
C1
J1
R3
R4
C2
CR1
R2
R18
R19
R21
CR3
R22
R7
C8
R8
C3
C12
Q2
R20
R23
E3
E4
Q1
Q3

20249-XXX



I.C. LOCATION & VOLTAGE CHART

TYPE	LOCATION	+5V	GND	TYPE	LOCATION	+5V	GND	TYPE	LOCATION	+5V	+12V	-12VA	GND
7406	5E	14	7	7412	4D	16	8,9	S.M.DCKT	1A	—	1,16	—	4,5, 12,13
7409	5D	14	7	74HC273	3C,4B	20	10	MTR CHIP	6A	—	—	—	4
74LS14	6C,6F	14	7	6500/1	4A	1,30	12	RD CHIP	6H	19	—	28	5,20
7438	5E,6D	14	7	LM393	3B	8	4	TRARE	4F	—	—	3 -10.2	7
7445	1C,2A,6F	16	8	E/PACK	6E	14	7	TRARE	4G	—	5	—	—
74HC74	5C	14	7	E/PACK	3G	—	—	LSZ	3H	—	—	—	1,7, 11
EPROM	4C	21,24	12,13										

REF. DES.		
LAST USED		NOT USED
C53	L6	C13,15,31,39,40
CR5	Q6	C46 14
R88		R26,30,61,62,71
RP9		R74

MUST CONFORM TO ENG'NEERING SPEC. #30-001

TOLERANCE UNLESS OTHERWISE NOTED

MATERIAL

LINEAR .X ±.100 .XX ±.030 .XXX ±.010

ANGULAR ±.5°

SURFACE TREATMENT

HARDNESS

P/C HISTORY			
DATE	NO.		
11/16/83	P1278		
1/18/84	1330	DETAIL	C.Dow 1-16-84
8-29-84	1823	DESIGN	RELEASED FOR ASSEMBLY
		APPRO	

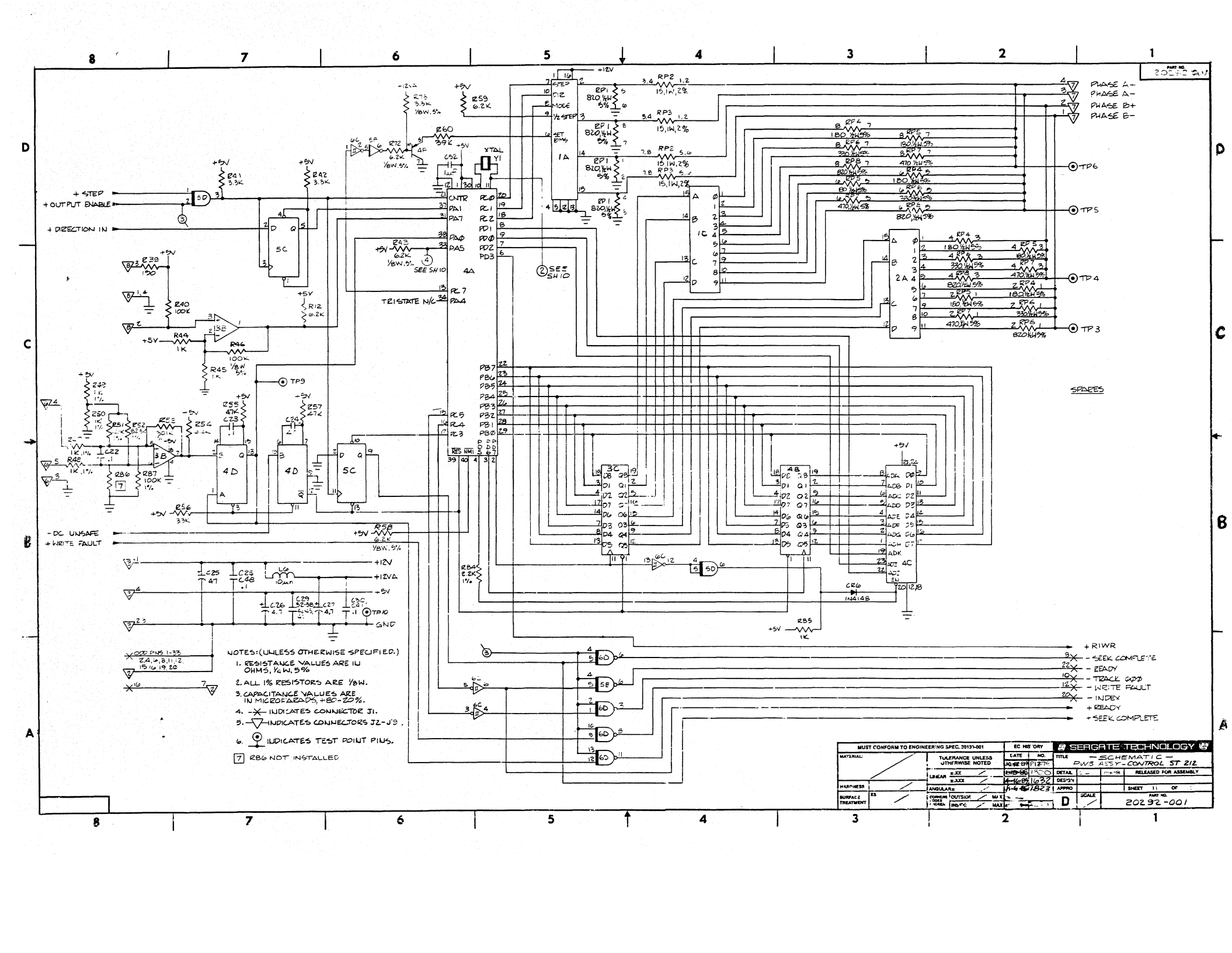
SEAGATE TECHNOLOGY

TITLE: SCHEMATIC PWB-ASSY-CONTROL ST 212

SHEET 10 OF 11

SCALE: D

PART NO. 20292-001


+ STEP
+ OUTPUT ENABLE
+ DIRECTION IN
- DC UNSAFE
+ WRITE FAULT
TRISTATE N/C
SPARES
PHASE A-
PHASE A-
PHASE B+
PHASE B-
TP6
TP5
TP4
TP3
TP9
TP10
GND
+12V
+5V
+12VA
+ RIWR
- SEEK COMPLETE
- READY
- TRACK 000
- WRITE FAULT
- INDEX
+ READY
+ SEEK COMPLETE
NOTES:(UNLESS OTHERWISE SPECIFIED.)
1. RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%
2. ALL 1% RESISTORS ARE 1/8W.
3. CAPACITANCE VALUES ARE IN MICROFARADS, +80-20%.
4. -X- INDICATES CONNECTOR J1.
5. INDICATES CONNECTORS J2-J9.
6. INDICATES TEST POINT PINS.
7 R86 NOT INSTALLED
MUST CONFORM TO ENGINEERING SPEC. 30131-001
EC HISTORY
SEAGATE TECHNOLOGY
TITLE - SCHEMATIC - PWB ASSY-CONTROL ST 212
RELEASED FOR ASSEMBLY
SHEET 11 OF
PART NO. 20292-001
SCALE
D

920 Disc Drive, Scotts Valley, CA 95066-4544, USA ■ 408/438-6550