RAPID ACCESS DISC FILE (RAD)
MODELS 9367B AND C
TRAINING DOCUMENT

OCTOBER 1967

FOR TRAINING PURPOSES ONLY

SDS SCIENTIFIC DATA SYSTEMS TECHNICAL TRAINING SECTION

MT-CH-RAD/9-1

SECTION 1

GENERAL DESCRIPTION

GENERAL

The SDS Rapid Access Disc File Model 9367C (RAD) is manufactured by Scientific Data Systems 1649 Seventeenth Street Santa Monica California. The contents of this manual describe the electrical and mechanical characteristics of the SDS 9376C its operation and basic programming requirements, theory of operation and installation.

PURPOSE OF EQUIPMENT

The SDS Rapid Access Disc File Model 9367C system provides on-line, rapid access, auxiliary data storage for the SDS 92,925,930 and 9300 Computers. Storage capacity is modular, ranging from 524, 288 characters to 1,048576 characters per unit. As many as four storage units may be accomodated in the system. The average transfer rate is approximately 485,000 alphanumeric characters a second.

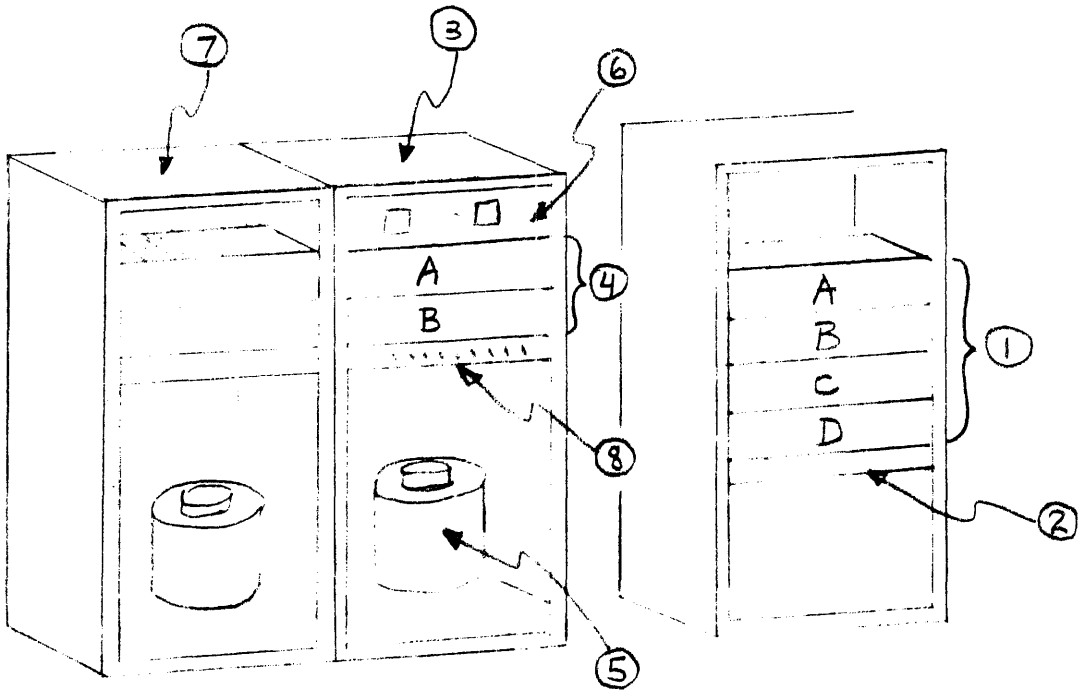
The SDS Disc File Model 9367 is implemented through an Input/Output buffer with Interlace and 12-bit character extension features as prerequisites.

EQUIPMENT FUNCTIONS

Each SDS 9367C RAD sytem consists of four basic functional parts:

a) one disc file coupler (controller)
b) one to four disc storage units
c) one to four disc selection units
d) one power protection panel

The disc file coupler acts as a controller and intermediary between the data disc units and the Input/Output channel. Data is assembled or disassembled and transferred between these units under control of the coupler



1. COUPLER
2. POWER FAIL SAFE CHASSIS
3. BASIC DISC SELECTION UNIT
4. SELECTION UNIT LOGIC
5. DISC STORAGE UNIT
6. POWER SUPPLY PX13/PX14
7. DISC EXTENDER UNIT
8. WRITE PROTECT SWITCH PANEL

FIGURE 1-1 MODEL 9367C RAPID ACCESS DISC FILE

The disc storage units contain mass data in digital form stored under control of the Input/Output channel and the disc file coupler which is randomly retrievable in blocks of 256 alphanumberic characters.

POWER PROTECTION PANEL

The Power Protection Panel is mounted near the Coupler Unit in the existing computer. Two transformers step down the 115 vac primary voltage to 10 vac signals. These signal voltages are connected to detector modules in the Coupler Unit.

The selection units contain the selection and comparison circuits required for accesing the addressed data as well as the read/write circuits and basic timing and registration circuits.

The modular characteristics of the SDS 9367C RAD system permit expansion of the disc storage units and selection units from one to four. Figure 1-2 describes a SDS 9367C RAD System with maximum storage capabilities.

SYTEM CONFIGURATIONS

Two different basic disc memory sizes available with the SDS 9367C Rapid Access File system are listed in Table 1-1.

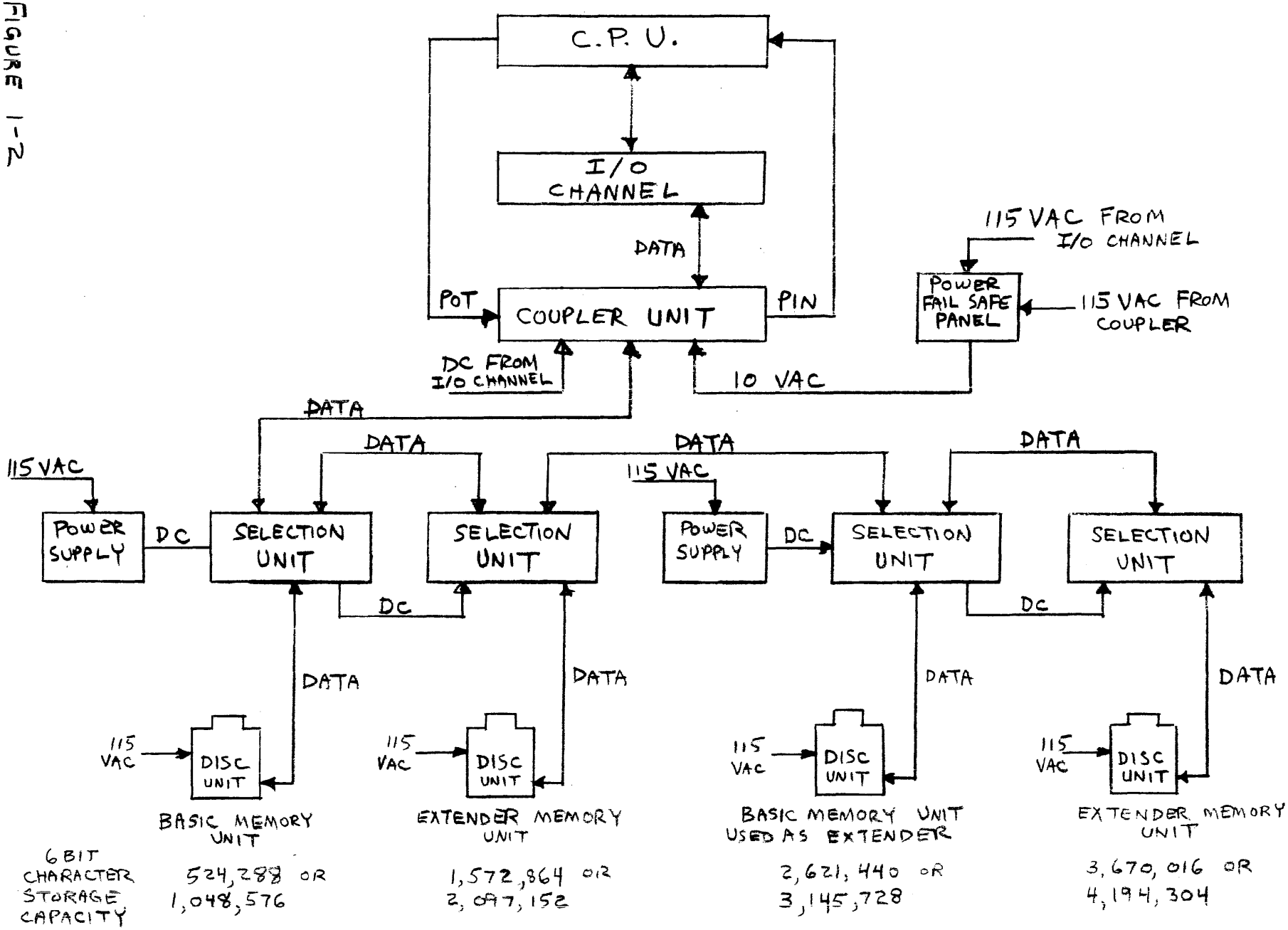
Model 9367C-01	131,072 word capacity, 2discs (524,288 alphanumeric characters)
Model 9367C-02	262,144 word capacity, 4 discs (1,048,576 alphanumeric characters)

Table 1-1, Basic Storage Unit Models

Additional memory is available by adding from one to three extenders to the basic Storage Unit. The available supplemental memory options are listed in Table 1-2.

FIGURE 1-2

RAD SYSTEM CONFIGURATION
MODEL 4367C-(01 – 42)



Model 9367C-11	131,072 word capacity, 2 discs (524,288 alphanumeric characters)
Model 9367C-12	262,144 word capacity, 4 discs (1,048,576 alphanumeric characters)

Table 1-2, Storage Extender Models

MECHANICAL CHARACTERISTICS

Each storage unit or extender comprises two or four discs, a motor control circuit, a shroud for mounting read/write heads, a dust cover and front panel, and support for mounting the unit to the cabinet. It has head mounting boards and mounting fixtures for 16, or 32 head boards depending upon the memory size. In addition, it has head mounts for two special timing tracks. The cables from the basic storage unit to the selection unit are hardwired to the selection unit.

One selection unit is required for each disc storage unit. The basic disc file and its selection unit are located in a separate cabinet and are connected to the coupler via a thirty foot cable.

The basic selection unit comprises three module chassis. Additional extender cabinets are located adjacent to the first, and are connected by 6-foot cables from one unit to the next in a serial manner.

The coupler consists of four module chassis and comprises the interface between the selection units and the computer input-output channel. The cables from the coupler to the channel are part of the coupler measures 19 inches and mounts in the input-output cabinet. Where space in the input-output cabinet is insufficient, the coupler may be mounted in a separate cabinet.

POWER REQUIREMENTS

In model 92, 930 and 9300 computer systems using the PX13 power supplies, and ac input of 1.9 amp unregulated is required for coupler operation. In models 92, 925, 930 or 9300 computer systems using PX22/PX23 power supplies, the regulated ac input requirement is 1.74 amp.

Each disc file configuration has a different total power requirement. The basic storage and selection unit requires an ac input of 7.2 amperes. The requirement is increased by 1.25 amperes for each extender unit added to the system. The extender units have an ac input power requirement of 6 amp each.

DISC ORGANIZATION AND TIMING CHARACTERISTICS

The disc storage units are organized by discs, disc surfaces, bands, tracks, sectors and words. Storage unit organization is described in tables 1-3.

Table 1-4 describes the mechanical and timing characteristics of the disc units.

MODULE COMPLEMENT

The 9367C coupler consists of four module chassis. The coupler module complement is listed in table 1-5. The selection unit consists of three module chassis. Its module complement is given in table 1-6.

GENERAL INFORMATION FLOW

The general information flow from the computer to the disc storage unit during write operations, and the flow from the disc storage unit to the computer during read operations, is shown in figure 1-3. A 15-bit address register is loaded from the computer memory through the C register with data that designates the selection and storage unit, the disc, the band, and the sector address of the information to be transferred. A 12-bit character register buffers the data between the coupler and the I/O channel during both read and write operations. The 12-bit character is assembled (for reading) of disassembled (for writing) by the 12-bit assembler disassembler which acts as a 3x4 serial-parallel register.

Information flow from one of four selection units is controlled by a unit selection register in the coupler. Each selection unit has the capability of protecting memory areas in groups of 32,768 words under manual switch control. If a memory protect switch is in the "up" position, any attempt to write in an area of disc memory corresponding to the switch address will be aborted. The memory protection switches do not inhibit reading from any memory area.

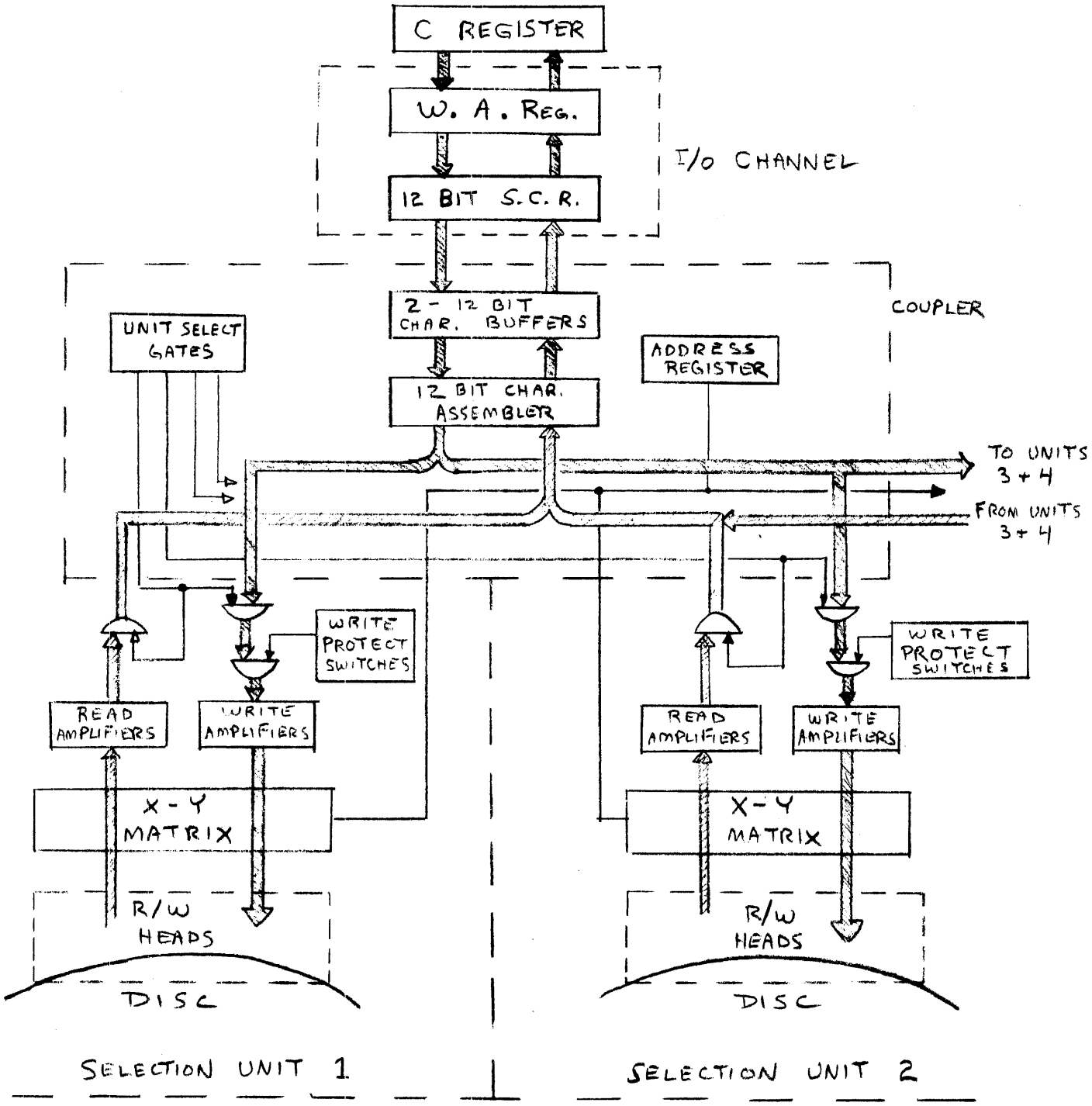


FIGURE 1-3

9367C DISC FILE SYSTEM - GENERAL DATA FLOW DIAGRAM

Discs per Storage Unit	2 or 4
Heads per Disc	64
Heads per Disc Surface	32
Heads per Band	4
Bands per Disc	16
Sectors per Band	64
Words per Sector	64
Timing tracks per Unit	2

Table 1-3 Storage Disc Organization

Disc Rotational Speed	1782 rpm
Maximum Recording Diameter	11.0 in.
Minimum Recording Diameter	8.9 in.
Tracks per Radial Inch	30
Track Width	0.02 in.
Track Pitch	0.033 in.
Sector Time	487 usec
Gap Time Between Sectors	40 usec
Sector plus Gap Time	527 usec
Bit Rate	820 KHz
Bit Density	980 b/i max
Word Transfer Rate	133 kwds/sec
Character Transfer Rate	266,000 12-bit ch/s

Table 1-4 Storage Disc Mechanical and Timing Characteristics

Number of Modules	Type of Modules	Name of Module
5	AH10	Signal Amplifier
5	AX14	Cable Driver
2	AX16	Cable Driver
10	BH10	Buffer Amplifier
5	FH19	DC Flip-Flop
13	FH 20	Basic Flip-Flop
1	FL21	Basic Flip-Flop
19	GK51	Diode Gate
2	IH10	And/or Inverter
8	IH14	Inverter Amplifier
1	MX12	Relay Module
1	OX12	One-Shot Multivibrater
2	SK60	Primary Power Detector

Table 1-5 Coupler Module Complement

Number of Modules	Type of Module	Name of Module
1	AK61	Read Input Control
2	AK62	Y-Select
16	AK63	Write Driver
1	AK64	Index/Sector Amplifier
3	AX14	Cable Driver
1	AK65	Write Clock Amplifier
1	BH10	Buffer Amplifier
4	FL21	Basic Flip-Flop
1	GH14	Gate Expander
4	HK73	Read Amplifier
4	HK74	Limiter
4	HK76	Data Decoder
4	HK75	Clock Discriminator
1	HK77	Index/Sector Decoder
1	IH14	Inverter
1	IL12	Inverter
4	NK59	Read-Write Decoder
1	OX12	One-Shot Multivibrator
1	SX69	Primary Power Detector

Table 1-6, Selection Unit Module Complement

SECTION II

PROGRAMMING

SECTION II

GENERAL

The following discussion of basic programming for the Rapid Access Disc File Model 9376 system applies primarily to the SDS 925/930/9300 computers. The relatively minor difference in programming methods required by the SDS 92 computer will be found in the SDS Reference Manual, 900505B. In general, however, the basic techniques of programming for the RAD system apply to all SDS 900 Series computers including the SDS 92.

INSTRUCTION CLASSIFICATION

Four classes of input-output instructions are required to operate the RAD System and its associated buffer. These instruction classes are:

EOM
SKS
POT
PIN

The assigned EOM and SKS address to direct all RAD operations is 26 octal. Thus, the two least significatint octal digits of any EOM instruction addressing the RAD is 26 for input operations (reading), or 66 for output operations (writing).

EOM INSTRUCTIONS

ALERT TO PIN

The Alert to PIN instruction takes the form EOM 1N226. This instruction operates in the I/O mode and alerts the addressed storage unit that a PIN instruction is to follow. Octal digit "N" addresses one of the four disc storage units, where N=0 addresses storage unit 1; N=2 addresses storage unit 2; N=4 addresses storage unit 3; and N=6 addresses storage unit 4.

ALERT TO POT

The Alert to POT instruction takes the form EOM 10026. This EOM instruction operates in the I/O mode and alerts the disc coupler that a POT instruction is to follow.

This EOM is always followed by a POT that will always be processed, and the band selection matrix will always be set up to the new address at the next sector mark. Gaps can be detected by the Disc Ready SKS 10026 after an operation has been initiated.

NON-INCREMENT MODE

No incrementing of band will follow Alert to POT EOM 11026. This EOM or EOM 11066 is used in the special case that a full band is being transferred, starting at an arbitrary sector, and band incrementing is not desired after sector 77_8. The computer will be programmed to disconnect at sector 77_8, but only reconnecting and resetting of interlace is required to complete the band transfer, as the A register retains the address of the previously transferred sector +1, and another alert EOM POT is not required.

CONNECT DISC MEMORY, READ

The Connect Disc Memory, Read instruction takes the format EOM02226. This EOM instruction operates in the buffer mode and establishes the character packing format of two 12-bit characters per word, and initiates the read operation when the sector corresponsidng to the contents of the sector address register comes under the read head. Two 12-bit characters are transferred for each interlace memory access.

Proper programming practice dictates that this instruction be preceded by an ALC, EOM (IOC), POT sequence. The ALC and POT are needed to set up the interlace and the IOC type EOM is used to specify the IOSD termination mode.

CONNECT DISC MEMORY, WRITE

The Connect Disc Memory, Write instruction takes the form EOM02266. This EOM instruction operates in the buffer mode and establishes the character packing format of the two 12-bit characters per word, and initiates the write operation when the sector corresponding to the contents of the sector address register comes under the write head. Two 12-bit characters are transferred for each interlace memory access.

Like the Connect Disc Memory, Read command, this instruction must also be preceded by the same ALC, EOM (IOSD), POT sequence.

SKS INSTRUCTIONS

SKIP IF DISC READY

The Skip if Disc Ready instruction takes the form SKS 10026. This instruction will cause the computer to skip the next normally sequenced instruction if the coupler is not currently engaged in a read or write operation.

SKIP IF NO DISC ERROR

The Skip If No Disc Error instruction takes the form SKS 11026. This instruction will cause the computer to skip the next normally sequenced instruction if no error condition exists. An error condition can exist for any of the following reasons:

A) An attempt has been made to write into a protected area of disc memory

B) A POT instruction addressing the RAD system was executed while the unit was in the process of reading or writing

C) An attempt was made to continue operation after the final sector of a storage unit had been written or read.

SKIP IF BAND NOT WRITE PROTECTED

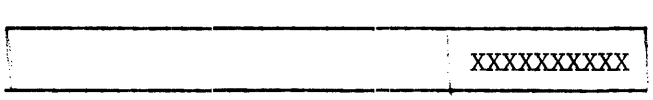
This instruction takes the form SKS 13026. The program skips the next normally sequenced instruction if the band being addressed is not write protected by the memory protection switches. The program does not skip if the band being addressed is write protected. The status of the memory protection switches can be tested by executing an Alert to POT, followed by a POT instruction addressing the memory area under question, programming a delay of 537+ microseconds, and then followed with SKS 13026. The delay is required because the register which is tested with the switch logic is not filled until the sector mark following the POT instruction.

POT INSTRUCTION

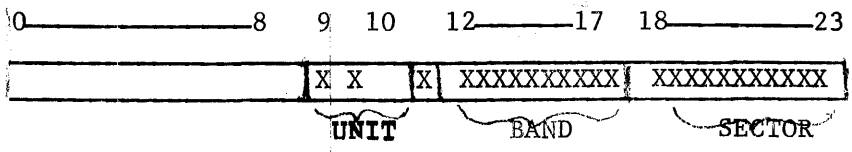
The execution of a POT instruction following an Alert to POT fills the coupler address register with the contents of the specified memory word. At the next sector pulse the band field of the coupler address register is transferred to the matrix register in the Selection unit, replacing the band address from the previous operation.

PIN INSTRUCTION

The execution of a PIN instruction following an Alert to PIN results in the transfer of the contents of the sector counter (which contain the address of the current sector) of the disc unit specified in the Alert to PIN EOM to the specified memory location. The sector address appears in bit 18 through 23 of the memory word; the contents of bits 0 through 17 are not significant.



The information contained in the memory word includes the address of the disc storage unit, the disc, the band, and the sector



LOCATION	INSTRUCTION	ACTION
01202	SKS 10026	Skip if disc ready
01203	BRU 01202	Loop until ready
01204	EOM 10026	Alert to POT
01205	POT 01213	POT address to coupler Unit
01206	EOM 50000	Alert channel interlace
01207	EOM 17200	IOSD Termination mode Also arms end of record and word count zero interrupt
01210	POT 01214	POT to interlace register
01211	EOM 02226	Connect disc memory, read
01212	BRU _ ___	Exit and wait for interrupt
01213	00000773	
01214	30012707	Word count and starting core address

SAMPLE READ PROGRAM

The listing shown in Table 2-1 is a simplified programming example intended to clarify some of the steps required to read information from the disc file into the core memory of the computer. It does not demonstrate sophisticated programming techniques.

The sample program reads sectors 00773 through 01000 (384 words) into core locations 13277 through 13506. Each step of this listed program is explained in detail in the following paragraphs.

The SKS instruction located in 01202 tests the RAD coupler for a ready status. If the coupler is busy in either a read or write operation, the program takes its next instruction from location 01203 which causes the computer to branch back to 01202 forming a two word loop until the disc coupler is no longer busy. When the coupler is ready the program sequences to location 01204 for its next instruction.

The EOM instruction located at 01204 operates in the I/O mode, and alerts the disc coupler that a POT instruction is to follow. The POT instruction at 01205 transfers the contents of memory location 01212 to the address register of the coupler. The contents of the word transferred (00000773) represents the address of the first sector to be read and transferred to computer memory. (Unit 0, Band 07, Sector 73)

The EOM instruction located at 01206 operates in the input output control mode and selects the I/O channels (the W buffer in this example) and alerts its interlace that an EOM (IOC) and POT are to follow.

The EOM instruction located at 01207 operates in the I/O mode and establishes the IOSD extended mode operation (mandatory for Reading or writing), and arms both the zero word count (I1W) and end of record interrupts (I2W) If only one interrupt is to be used. it should be I2w which will always occur. If I1w only were used and the operation were aborted due to an error condition occurring prior to a zero word count condition, the I1w interrupt would not occur.

The POT instruction located at 01210 transfers the contents of core memory location 01204 to the I/O channel interlace. The interlace word contains in bit 0 through 9 a binary number equal to the number of words to be transferred. Bits 10 through 23 of the interlace word contain the address of the first of 384 core memory locations into which the disc data are to be transferred.

If the interlace word count exceeded the 10 bit field the most significant 5 bits would be held in bit 19-23 of the IOSD EOM located in location 01207. Likewise if the starting core memory address required the most significant bit it would be in bit 18 of the same EOM.

The EOM instruction located at 01211 operates in the buffer control mode and selects the I/O channel (W in this example) and connects the coupler to operate in the two character per word mode without leader. The read operation starts 16 microseconds after the sector mark of the addressed sector. The connect instruction is programmed last in order to avoid a computer hang-up condition. If the I/O channel is connected and the Ecw signal (device clock) is sent before the interlace is set up, the computer does not receive the proper signal (Rt) from the channel in response to the interlace POT. This signal is needed the release the computer from the wait phase of the POT command. Thus the safe procedure is to set up the interlace first.

The parameters required to initiate a disc to core transfer have been established. The branch instruction located in 01212 returns program control back to the main program. When the interlace word count reaches zero the interrupt subroutine should then test for any errors that may have occured during the reading and transfer of the data. If the end of record interrupt occurs first, an error obviously occurred and appropriate actions should be taken.

PARTIAL SECTOR READ OR WRITE

It is not necessary that entire sectors of 64 words be written or read. However, certain restructions are placed upon the program if less than a complete sector is to be transferred. For example, if in the sample read program the programmer wanted to read only 32 words of sector 773, he would change the contents of the interlace word 1214 to 02012707 octal. When the buffer word counter reaches a count of zero, the buffer initiates a disconnect and will accept no more data from the disc coupler unit.

If less than a complete sector is written or read, the word boundary ranges from the first word. It is not possible, for example, to read or write the last 32 words of a sector without reading or writing the first 32 words of the sector. If less than 64 words are to be written into a sector, the data in all words following the final data word written will be changed to zeros. If, for example, data is written into only the first 20 words of a sector, the remaining 44 words will be written with all zeros.

IMMEDIATE MODE ACCESSING

Whenever one complete band (64 sectors) is to be transferred, access time can be reduced to a minimum by special programming techniques. If the program addresses the disc file system at random (i.e., without determining where sector 00 happens to be at the time of initiating the transfer) the access time could be as long as 33 milliseconds. For example, if the program is written to read sector 00 through 77, and sector 13 is under the read/write heads at the time the transfer is initiated, about 30 milliseconds will be spent before sector 00 comes under the heads and the transfer can begin. During these 30 milliseconds the I/O channel cannot be used for other input-output purposes. This delay can be eliminated if the program is written in such a manner that the complete 64 sector band can be read in two separate passes; the first pass to read sector n through 77, and the second pass to read sectors 00 through n-1, where n equals the first sector available to the disc storage unit. The starting address in in the immediate mode is obtained by executing a PIN instruction to determine the current sector address, and by adding two to this address. For example, if the PIN instruction indicates that sector 23 is about to come under the read/write heads, the first pass should indicate a transfer of sector 25 through 77, and the second pass should indicate a transfer of sector 00 through 24.

Normally, if 64 sectors are to be transferred and the starting address n does not equal 00, the band address will count up as the sector address changes from 77 to 00. This must be prevented by placing a one in bit position 14 of the alert to POT instruction.

When issuing the first transfer (current sector ≠ 2 to sector 77), the word count and the starting addresses must be properly adjusted. When using the immediate access mode it is necessary to arm the End-of-Record interrupt so that when sector 77 has been read the interrupt signal will cause the computer to enter the interrupt subroutine. This interrupt subroutine must supply the new address paramaters and word count for the core memory locations for the transfer of sectors 00 through n-1. This set up of the second portion of the transfer must occur during the gap time between sector 77 and 00.

PRIORITY INTERRUPT OPTION

Access time can also be reduced by use of the priority interrupt option. This option allows the program to set up initial transfer conditions without connecting the buffer. This permits the selection unit and coupler to search for the first disc address to be transferred without tying up the I/O channel. About 28 microseconds before the addressed sector becomes available to the selection unit, the interrupt occurs. The interrupt subroutine connects the coupler with a Connect to Read or a Connect to Write instruction.

SECTION III

THEORY OF OPERATION

INTRODUCTION

This section of the manual provides theory of operations for the SDS Rapid Access Disc File Model 9367C. The theory of operation is divided into two main sections in the following order:

a. General Theory of Operations

b. Logic Description

The General Theory of Operations describes in non-specific terms the component parts of the coupler, the selection unit, and the disc storage unit, as well as the general timing and data flow for each of the system operations.

The Logic Description describes in more specific terms those subjects covered under the general theory, and provides the logical timing, control, and flow equations as will as detailed flow charts and timing diagrams. Special circuit considerations are also discussed in this section.

GENERAL THEORY OF OPERATIONS

DISC FILE STORAGE UNIT

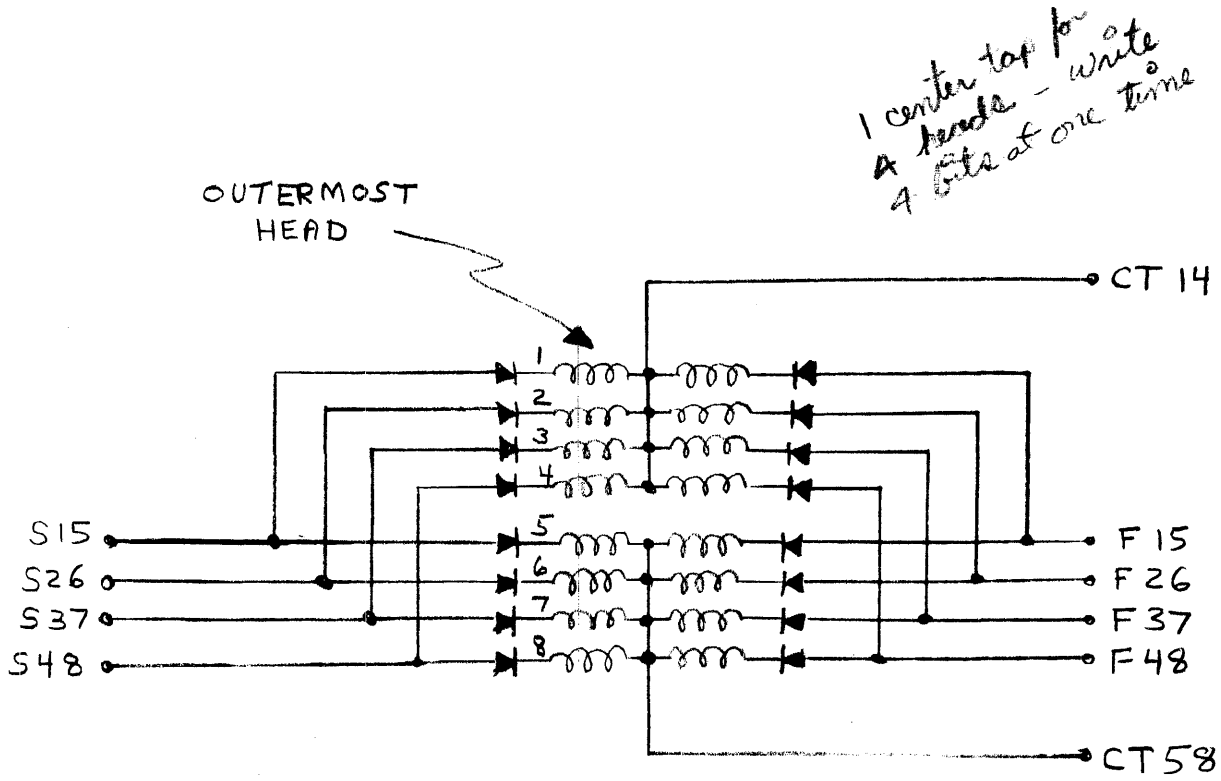
Each disc file storage unit consists of four discs that rotate on a common shaft. The discs are made of a non-ferrous metal, plated with a nickel-cobalt coating having magnetic properties. Disc drive is provided by a 115vac, 60 cps, single phase, induction motor directly connected to a common drive shaft. The motor requires 120 seconds maximum to come up to operational speed of 1780 rpm after power is first applied. No interlock exists to prevent reading or writing during this acceleration time.

The read/write heads are mounted on head boards, eight heads to each board, and are arranged at 90° intervals around the top and bottom surfaces of each disc. Rotation of the disc creates an air flow in close proximity to the disc surface and the dimensionally controlled flying surface of the heads uses this air flow to maintain an air slider bearing that sustains the heads out of physical contact with the disc surface at a uniform spacing of less than .00002 inches. This spacing is not affected by disc runout or by thermal shock. When the unit is at rest, the heads, which are suspended by two pivot bearings on an adjustable flexible reed, make contact with the disc surface.

Each disc mounts 64 heads, 32 on the top surface and 32 on the bottom surface. Data is written four bits in parallel on the disc, and therefore, four heads must be selected for both read and write operations. Each of the four heads reads or writes a track; four tracks make up one band. One band of four tracks extends for 360^{o}, or for the entire disc circumference. Discs are addressed octally as 0, 1, 2 and 3, but are usually referred to as discs 1, 2, 3 and 4 respectively. Eight heads composing two bands are mounted on each head board. The four outer heads on each head board are identified as heads 1, 2, 3 and 4, and are connected by a common center tap, CT14. The four inner heads on each head board are identified as heads 5, 6, 7 and 8, and are connected by a common center tap, CT58. Start and finish windings of the corresponding inner and outer heads are wired in parallel and are identified as S15, S26, F26, S37, F37, and S48, F48. See Figure 3-1. Heads are selected on an X-Y coordinate; the center taps selected by Y select modules and the start and finish windings by the Read/Write Decoder modules through X selection gates. Eight head boards, all mounted on each disc, four on the upper surface, and four on the lower surface. Figure 3-2 shows the head placement on each of the four discs. Note that the top disc, Disc 1, also mounts three special read heads for timing and registration purposes. One reads the sector and index marks and the others read two identical clock tracks. These heads are not selectable through the X-Y matrix. Note that all odd numbered head boards service the upper disc surfaces while all even numbered head boards service the lower disc surfaces.

All head boards are dimensionally identical with each other. The eight heads on each of the head boards would lie on a circular line equidistant from the center of the disc if some provision was not made to prevent this overlapping. Head boards HB5 and HB6 are mounted on a common head board assembly fixture. A single shim is inserted between this head board assembly fixture and the disc housing, displacing the tracks of HB5 and HB2 which are not shimmed. Two shims are used for HB9 and HB10 assembly fixture, and three shims are used for HB13 and HB14 assembly fixture. In this manner, the tracks of all head boards are interlaced with each other.

Table 3-1 shows the head board selection method as the addressed bands (bits 12 through 17 of the address register) progresses from 00 through 77.



LEGEND

CT 14 - CENTER TAP, HEADS 1 THROUGH 4
CT 58 - CENTER TAP, HEADS 5 THROUGH 8
S 15 - START WINDING, HEADS 1 AND 5
F 48 - FINISH WINDING, HEADS 4 AND 8

FIGURE 3-1 HEAD BOARD CONNECTIONS

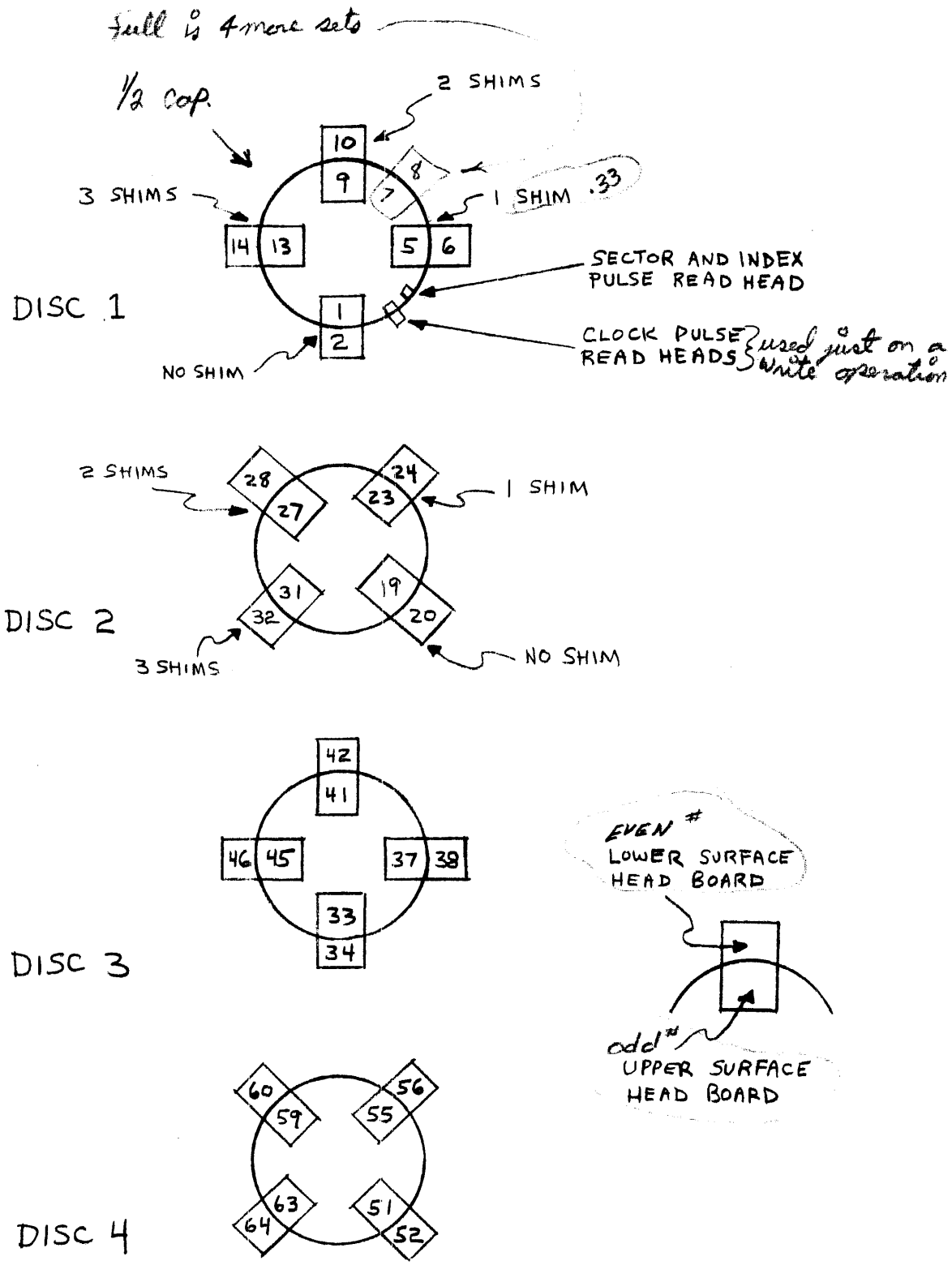


FIGURE 3-2 HEAD BOARD PLACEMENT

Address	HB	Address	HB
U00SS	01	U20SS	05
U01SS	33	U21SS	37
U02SS	19	U22SS	23
U03SS	51	U23SS	55
U04SS	01	U24SS	05
U05SS	33	U25SS	37
U06SS	19	U26SS	23
U07SS	51	U27SS	55
U10SS	02	U30SS	06
U11SS	34	U31SS	38
U12SS	20	U32SS	24
U13SS	52	U33SS	56
U14SS	02	U34SS	06
U15SS	34	U35SS	38
U16SS	20	U36SS	24
U17SS	52	U37SS	56
U40SSS	09	U60SS	13
U41SS	41	U61SS	45
U42SS	27	U62SS	31
U43SS	59	U63SS	63
U44SS	09	U64SS	13
U45SS	41	U65SS	45
U46SS	27	U66SS	31
U47SS	59	U67SS	63
U50SS	10	U70SS	14
U51SS	42	U71SS	46
U52SS	28	U72SS	32
U53SS	60	U73SS	64
U54SS	10	U74SS	14
U55SS	42	U75SS	46
U56SS	28	U76SS	32
U57SS	60	U77SS	64

* U = any selection unit address

SS = any sector address

Table 3-1 Band Address and Head Board Relationship

Disc Data Format

Sector Format

Each band, which is composed of four tracks, contains 64 sectors spaced equidistant around the disc, dividing the disc circumference into 64 equal parts. At a rotational speed of 1780 rpm each sector requires 527 us to pass under the read/write heads. These 527 us are divided into five major parts; gap, preamble, parity, postamble, and data. Each sector is sequentially composed of a 13 clock time leading gap, a 10 bit/track preamble, 64 words of data, a 1 bit/track parity, a 11 bit/track postamble, and a trailing gap. See Figure 3-3. Each sector starts when the sector index pulse counts up the sector counter (D register), and ends when the next sector index pulse arrives. See Figure 3-4.

Word Format

Four bits of each word are written simultaneously on the four tracks that make up a band. Consider the computer word to be 8 octal digits, the most significant called 0 and the least significant called 7 See figure 3-3. The binary information contained in a word is extracted in such a manner that the octal digits 0 and 4 are written on track 1, octal digits 1 and 5 on track 2, octal digits 2 and 6 on track 3, and octal digits 3 and 7 on track 4. The placement of the binary digits of the word in relation to the tracks is shown in Figure 3-3.

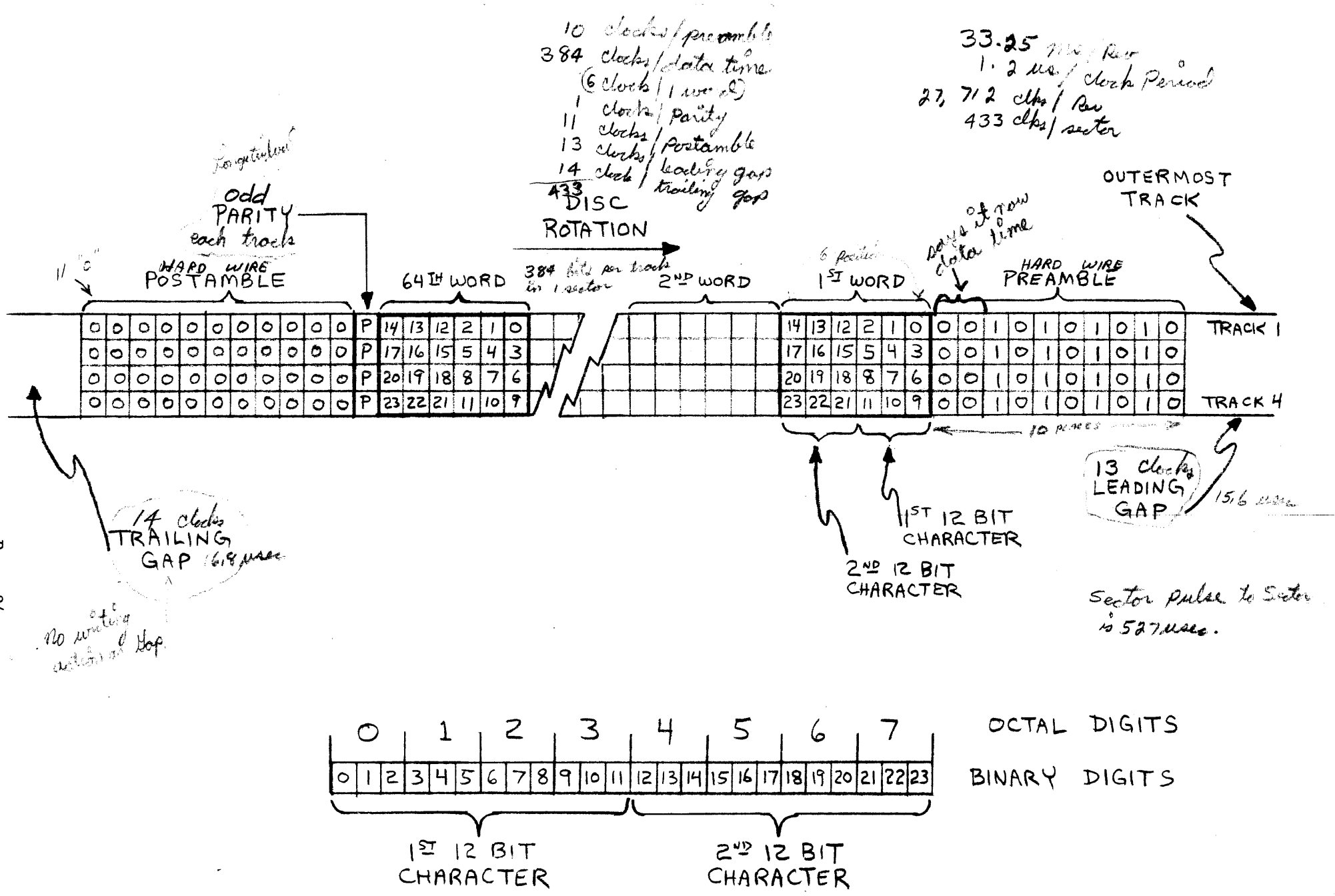


FIGURE 3-3 WORD AND SECTOR FORMAT AND DISC FORMAT

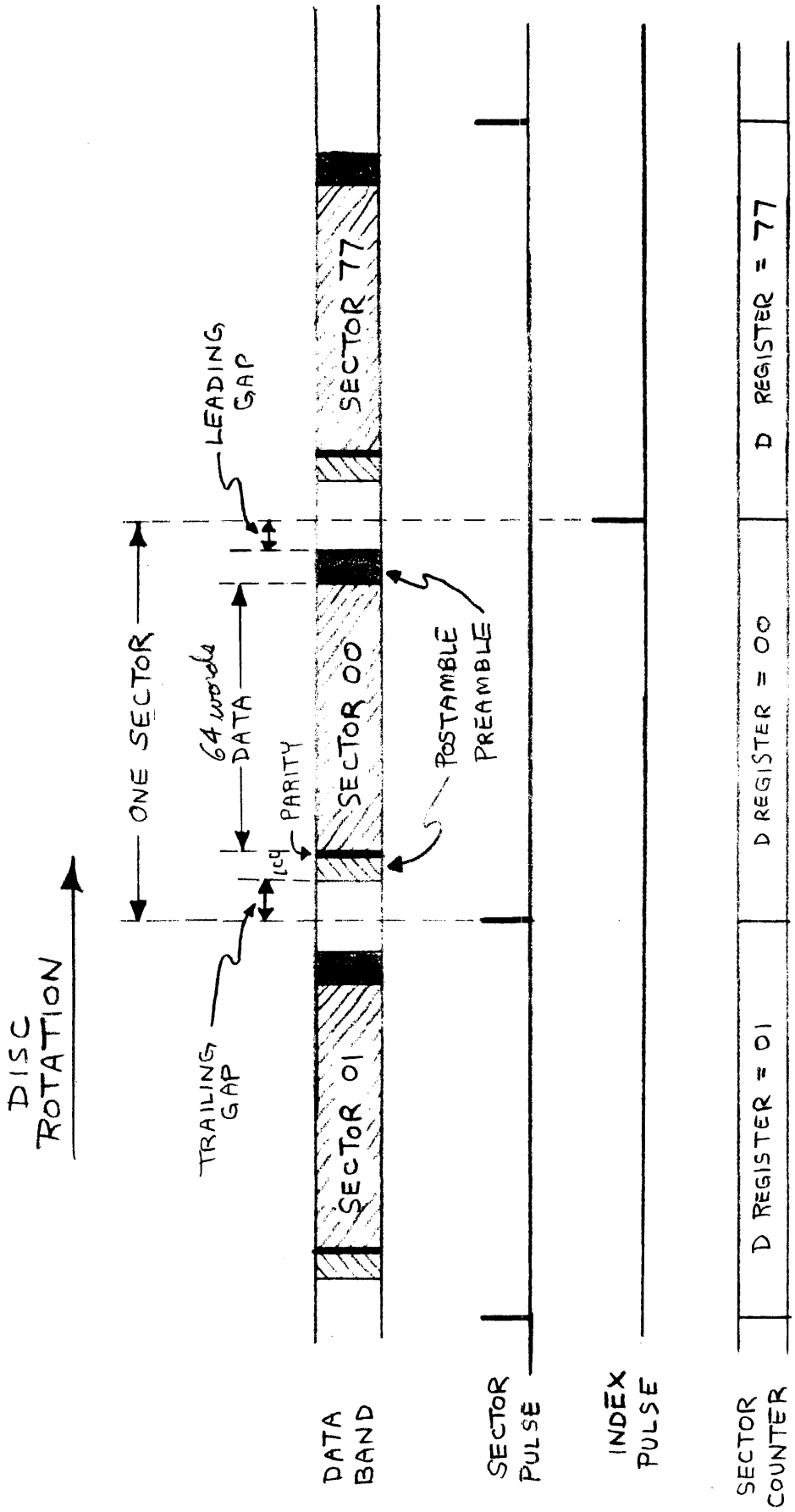


Figure 3-4 Sector Format and Timing

Disc File

Selection Unit

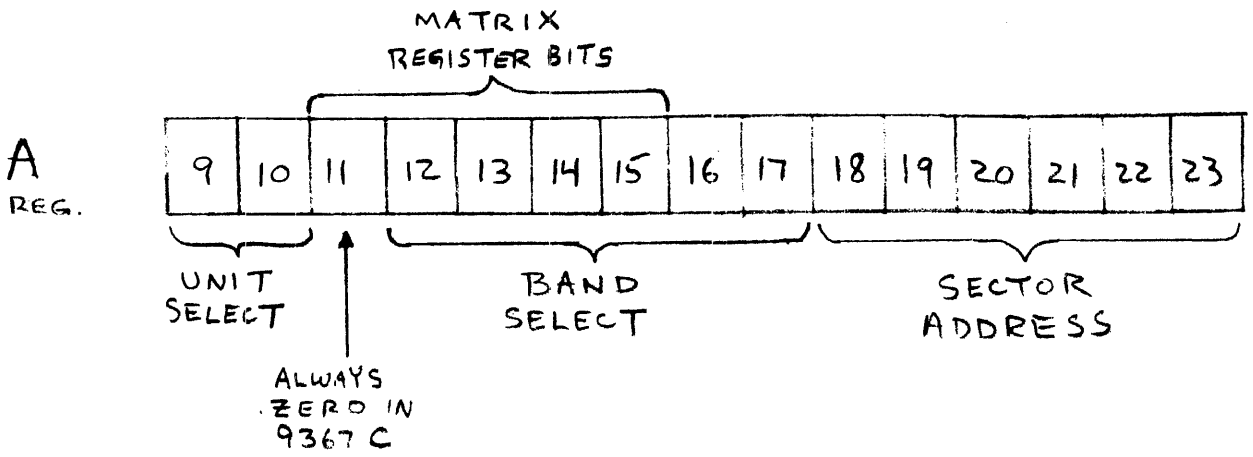
One selection is used with each disc storage unit, and is mounted in the same cabinet with the storage unit. One incoming control cable from the Coupler Unit (mounted in the computer) is used to control the Selection Unit. An output cable is connected between the Basic Storage Unit and the Extender Storage Unit (if used). The power supplies in the Basic Disc Storage Unit have sufficient capacity for one Extender Storage Unit. If additional storage capacity is required, connect a second Basic Storage Unit to the system to provide dc operating voltages for the third storage unit, and the fourth storage unit (if used).

The Selection Unit contains the read/write selection matrix, the write drivers, the read input control moudle, and four read-write decoders, read preamplifiers, and limiters. Table 1-6 lists the modules used in the Selection Unit. Figure 4-7 shows the location of all modules used, including interconnecting cable plug modules. The clock and timing circuit modules are included in the Selection Unit. See Figure 3-7. Storage capacity determines the quantity of Y Select Modules in use. One module is required for each 64 heads, or 2 modules for each 128 heads in the storage unit. Storage capacity may be increased in the field by increasing the capacity of the smaller discs, but additional Y Select Modules must also be installed at the same time.

Selection Matrix

The selection matrix in the Selection Unit, for a 256 head disc memory storage unit (64 bands), consists of four Y-Select circuits on each of four Y Select Modules AK 62 and four read/write coupler circuits on each of four Read-Write Decoder Modules NK59 to provide a 16 x 16 X-Y coordinate matrix to select the 256 possible head combinations in one storage unit.

The X and Y selection circuits receive their information in gated form from the address register (A) located in the Coupler unit and from the matrix register (A) in the Selection unit. This matrix register is a duplication of bits A11 through A15 of the coupler address register. The address register, in turn, receives the initial address from the C register in the computer, bits 9 through 23, during the POT instruction.



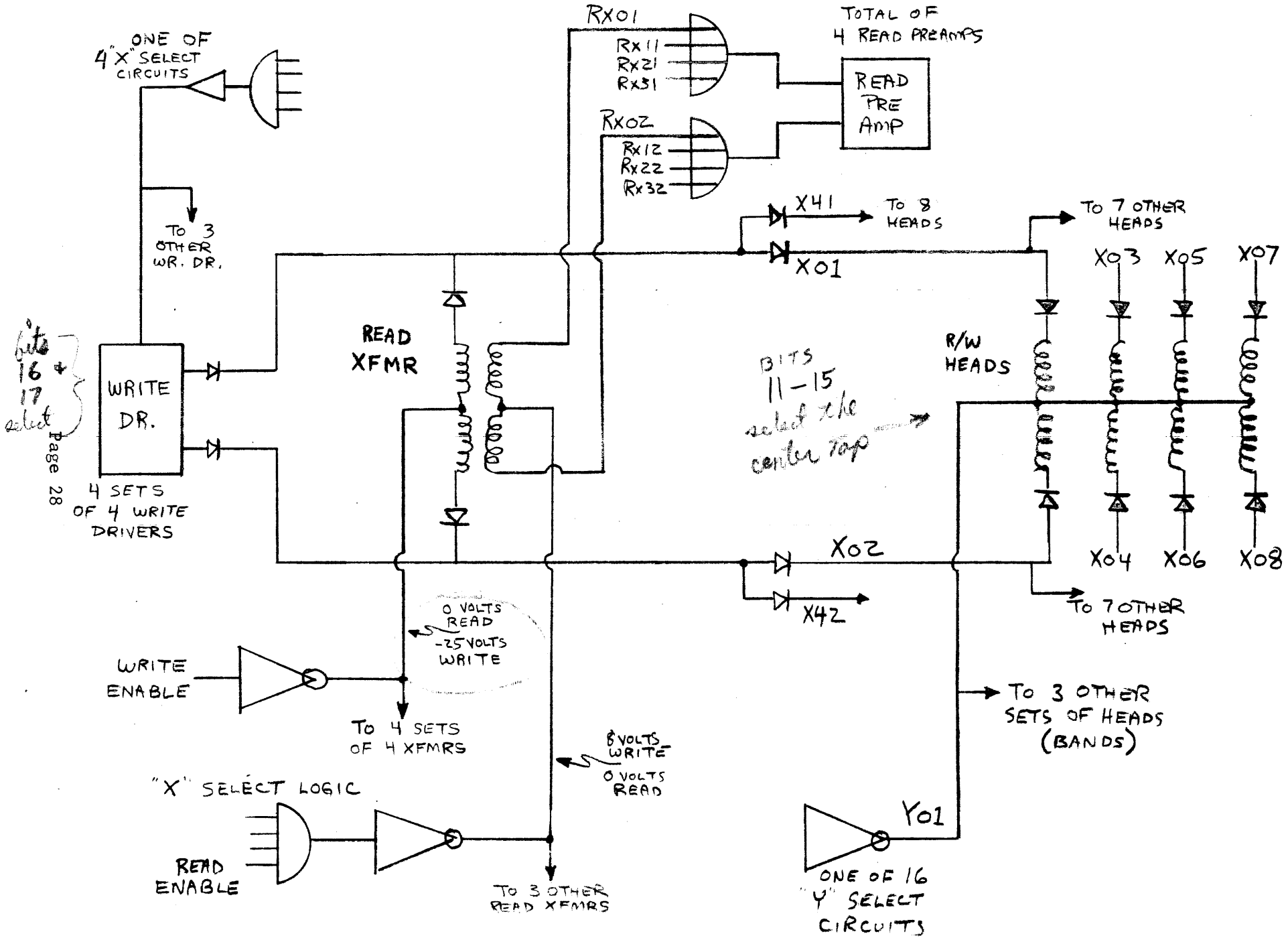
Bits A18 through A23 represent the address of the sector; bits A9 and A10 address one of the possible four storage units, and bit A11 is always a zero in the 9367C. It is used only in the larger capacity 9367B. Bits A11 through A17 are used to select the proper read/write heads. Each address in bits A11 through A17 activates one of the 16 Y Selectors and four of the X selectors so that four X-Y coordinates exist to select the four read/write heads of the addressed band. See Figure 3-5.

Write Drivers and Write Flip Flops

The Selection Unit contains 16 Write Driver Modules AK63 and a Write Flip Flop Module FL21 containing four write data flip flops. For any given band address the data bits in the four write flip flops must be gated to one group of four of the 16 write drivers. This write driver group is selected by address register bits 16 and 17. Thus the write drivers and their associated gates constitute the X selection circuits used during writing.
The write flip flops are varied in such a manner that they unconditionally change their state every 1.2 microseconds and at the clock pulse which occurs between these toggle changes, the flip flop will sample the data bit and either set or reset accordingly. See Figure 3-6. The recording scheme is a phase recording type sometimes called Manchester, Ferranti, Frequency Modulation, Modified Non Return to Zero, or Double Transition. Flux changes may occur as often as every 600 ns although some may be omitted. When reading back the flux changes are sampled for polarity only every 1.2 microseconds at the clock time. The polarity determines the bit significance.

Read Input Control

The Read Input Control module AK61 uses the two least significant bits of the address, A16 and A17, to select the four heads to read. The center taps to select the four heads to read. The center taps of the heads are still



9367 C HEAD SELECTION FIGURE 3-5

selected by the Y selection circuits. The Read Input control circuits select the proper heads by enabling the proper four read Transformers. Thus the four Read Input control circuits and the 16 associated read transformers constitute the X selection circuits used during the read operation.

Read Modules

The read modules consist of four Read-Write Decoder Modules NK59, which contain the read transformers and which are used to separate the write and read circuits from the common head; the four Read Preamplifier Modules HK73 which amplify and square the read signal to square-wave pulses of approximately 2 volts; the four Limiter Modules HK74, which limit the read pulses to essentially this same level; and the four Data Decoder Modules HK76 which decode the recorded data and set the four Read flip flops accordingly. This data is then sent to the Character Assembler register in the coupler where it is assembled into a 12 bit computer half word.

Timing Circuits

The basic timing (clocks) for the read function is taken from the data by the four Clock Discriminator Modules HK75. The timing (clocks) for the write function is taken from the timing track located on the outer edge of the top disc of each storage unit. These pulses from the prerecorded timing marks from the timing head (WCH) are counted down by two in a flop-flop to produce a clock pulse every 1.2 microseconds called WCK. The amplified timing head signal (WCA) and the half-frequency signal (WCK) are used during the write function to provide internal timing and to provide a source of clock signal to generate the Manchester type of recording pulse. Note the delay between writing and reading of the same bit as shown on Figure 3-6.

This delay between the read and write functions is caused by the requirement to wait at least one pulse before mixing the Manchester code, and the necessity to wait at least one pulse for the read clock, derived from the data itself. These two separate timing circuits are required to eliminate any skew which might exist.

Another timing pulse amplifier reads the pulses from the other timing track located on disc 1 of each disc storage unit. This timing track contains 64 pulses distributed equally around the circumference of the disc. The purpose of this pulse is to clock the sector counter to allow it to count in

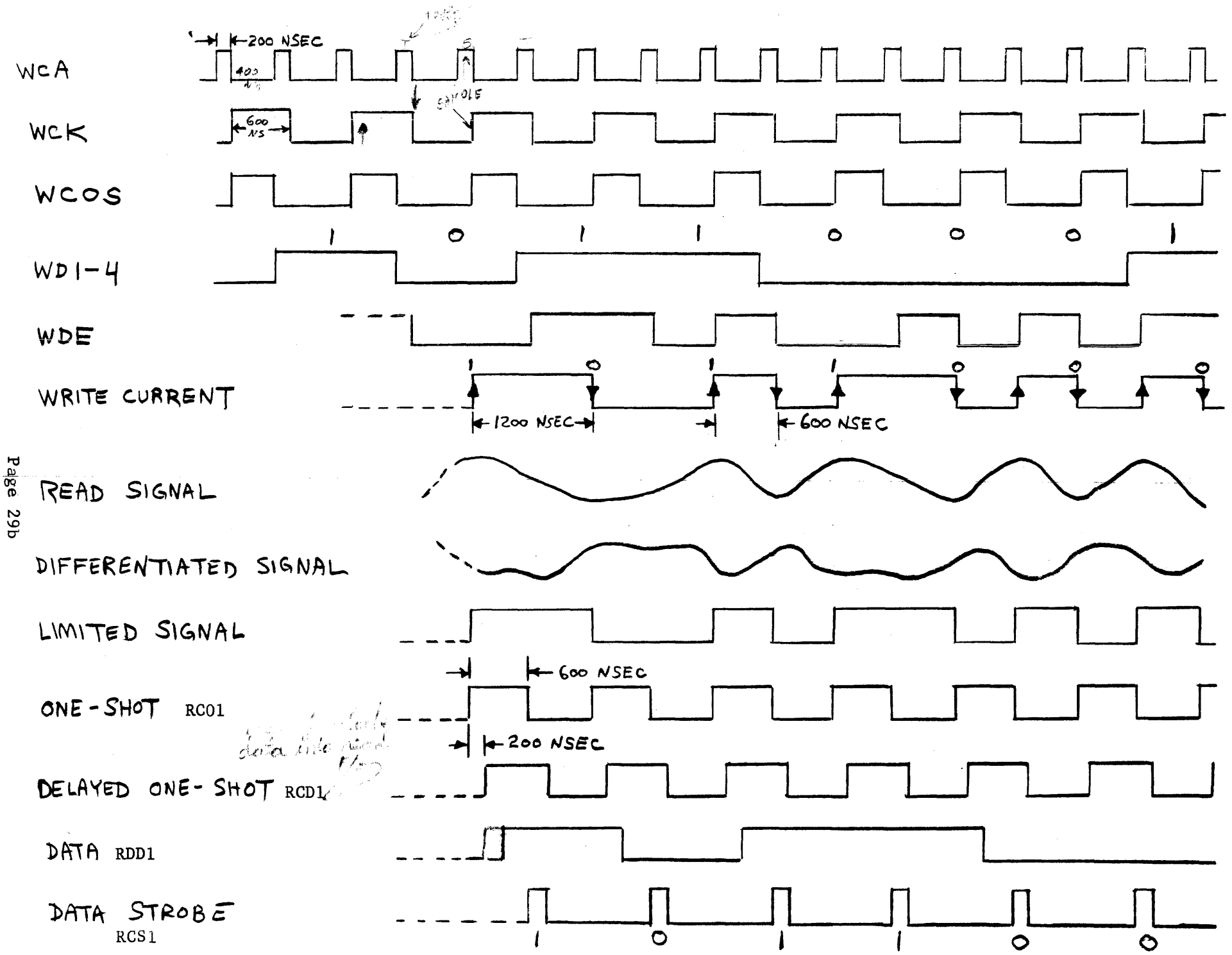


FIGURE 3-6 READ-WRITE DATA TIMING DIAGRAM

step with correspondingly numbered sectors on the discs as they pass under the read/write heads.

One of these 64 sector pulses is a double doublet rather than a single doublet. This is decoded in the Index/Sector Decoder module HK77 and is called the Index pulse (IDX), thus leaving only 63 sector pulses (SEC). The purpose of this index pulse is to establish the location of sector 00 on each disc unit, and to reset the contents of the sector counter register (D) to zero.

Sector Counter

The sector counter (D register) is composed of six flip-flops designated as D01 through D06. This register is set initially to zeros by the index mark when power is first applied to the disc storage unit, and is counted up by one each time a sector pulse is detected. Thus, this register counts octally from 00 to 77 and contains the address of the sector under the read/write heads.

The contents of the D register are gated into the computer C register, bits C18 through C23, during a PIN instruction.

Sector Comparison Gates

The six bits of the address register making up the sector address (A18 through A23) are continually being compared with the six bits of the sector counter register. When the sector addresses of these two registers are equal, a sector comparision term (SAC) comes true. When SAC is true, the next sector about to come under the read/write heads is the sector specified by the address register.

Write Protection Switches

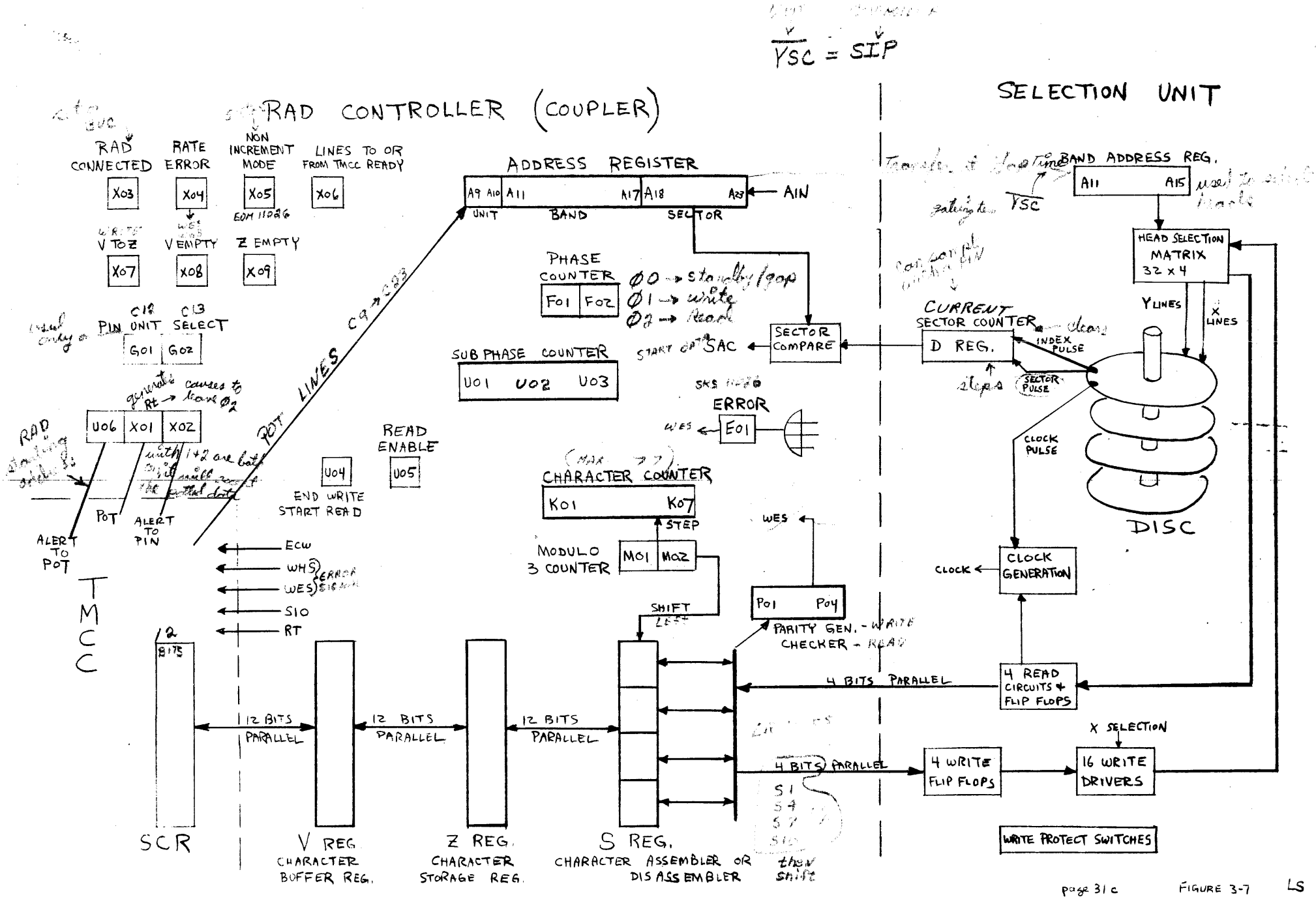
The 16 write protect switches mounted on the selection unit panel guard portions of disc memory. If one of these switches is in the "up" position, that portion of memory associated with the switch cannot be altered by a write operation. An attempt to write on a guarded portion of memory sets the error flip-flop and disconnects the buffer. Write protect switches do not affect reading from any portion of memory.

The panel switches, their logical names, and their associated protected memory areas are listed in Table 3-2. The write protect switches provide true or false logic levels which are used in logic gates to abort any attempt to write into memory locations corresponding to the switch. These switches

are not "hard-wired" into the selection matrix; therefore, it is possible that a malfunctioning gate could allow "protected" data to be destroyed or conversely, to "protect" an unprotected area of memory.

Switch	Logical Name	Bands	Affected Addresses
0-0	SW01	00-07	00000-00777
0-1	SW02	10-17	01000-01777
0-2	SW03	20-27	02000-02777
0-3	SW04	30-37	03000-03777
1-0	SW05	40-47	04000-04777
1-1	SW06	50-57	05000-05777
1-2	SW07	60-67	06000-06777
1-3	SW08	70-77	07000-07777
2-0			
2-1			
2-2			
2-3			
	Not used on 9367C		
3-0			
3-1			
3-2			
3-3			

Table 3-2 Write Protect Switches and Affected Adresses.



page 31c FIGURE 3-7 LS

DISC FILE COUPLER

The 9367C Disc File Coupler is located in the Input/Output cabinet and is connected to the basic selection unit via a 20-foot cable. The Coupler Unit may control as many as four Selection units, each having as many as 256 Tracks. The coupler buffers and controls the data flow between the TMCC (orDACC) and the selection unit. Power for the coupler is provided by the Input/Output unit. The coupler contains registers and flip-flops for control and timing purposes as well as for data handling. The following paragraphs describe the data and control registers that compose the coupler unit. See Figure 3-7.

Character Buffer Register (V01 - V12)

The character buffer register comprises 12 flip-flops, V01 through V12. During write operations the V register is filled in parallel from the 12-bit extended SCR register of the computer I/O buffer. During read operations the V register is filled in parallel from the Z register in the Coupler Unit.

Character Storage Register (Z01 - Z12)

The character storage register consists of 12 flip flops. During write operations the Z register is filled in parallel from the 12 bit V register. During read operations the Z register is filled in parallel from the S register. See Figure 3-7 .

Character Assembler/Disassembler Register (S01-S12)

The S register, made up of 12 flip-flops S01 through S12, assembles each 12-bit character as it is read off the disc in a serial-parallel manner from the four read amplifiers. When the S register contains the complete 12-bit character, its outputs are gated to the Z register. At the same time this new character enters the Z register, the previous character in the Z register is loaded into the V register.
During write operations the S register receives the 12-bit character from the Z register in parallel. The character is then disassembled four bits at a time and is gated into the four write amplifiers to be recorded on the disc.

Track Parity Flip-Flops (P01-P04)

Longtitudinal odd parity is recorded on each of the four tracks of each band such that for each sector recorded there is an odd number of data one bits on each track. The four flip-flops, P01, P02, P03 and P04, generate this

parity bit when writing, and check for odd parity correspondence when reading.

Address Register (A09-A23)

The address reigster (A), consisting of 15 flip-flops, A09 through A23, is located in the coupler, and addresses the unit, the disc, the band, and the sector. The A register receives its address data from the computer C register during a POT instruction. A read or write operation cannot begin until and unless equality exists between the contents of the sector counter register (D) in the selection unit and the contents of the address register bits A18-A23. Whenever equality exists between the contents of the D register and the six least significant bits of the A register the read or write operation will begin, provided, of course, that one of these operations has been initiated by the program.

Module-3 Counter (M01-M02)

The module-3 counter consists of two flip-flops, M01 and M02. This counter is triggered by the gated clock pulse (CNT) and counts from 0 to 2. During read operations the 0-count signifies that one 12-bit character is being loaded into the character storage register (Z), and during write operations the Z-count signifies that one 12-bit character is being taken from the character storage register. As the modulo-3 counter reverts from a count of two to a count of zero, it provides a clock pulse to toggle the character counter register (K).

Character Counter Register (K)

The character counter consists of seven flip-flops, K01-K07, and counts the number of 12-bit characters in each sector being either read or recorded. Since each sector contains 128 12-bit characters (64 24-bit words), when the character counter is full (K = 177) one sector has been read or recorded. The count relationship between the M and K register is shown in Table 3-3.

M01	M02	K01	K02	K03	K04	K05	K06	K07
0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	0	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1

Table 3-3, M and K Character Counter Relationships

Phase Counter (F01-F02)

The coupler operates in one of three phases under control of a phase counter comprising the two flip-flops, F01 and F02. Table 3-4 describes the three phases, and their uses, and provides the logical expression of each of the states or sequences.

F01	F02	Phase	Condition	Logical Expression
0	0	0	Standby	00F
0	1	1	Write	01F
1	0	2	Read	02F

Table 3-4, Phase Counter

Subphase Counter (U01-U03)

Phase one and phase two contain substates or sequences under control of the subphase counter which consists of the three flip-flops, U01, U02, and U03. The functions of this subphase counter will be discussed in greater detail under read and write operations.

Flip Flop U04

Flip flop U04 is the termination of write, and initiation of read flip flop. The termination is accomplished by setting U04 at the clock time before the next to last Z to S transfer. The initiation is accomplished by setting U04 at the first 0-count after the preamble end is detected.

Flip Flop U05

Flip flop U05 is the read enable flip flop. This signal is used in the selection unit to enable the input gates to the read amplifiers 3.6 to 4.8 microseconds after the last possible address change.

Flip Flop U06

The DC flip flop U06 is set by an alert to POT EOM from the computer and reset by a POT command. This flip flop allows a POT to occur during the postamble of a read or write phase.

Flip-Flops X01 and X02

Flip-flops X01 and X02 are used primarily for PIN and POT operations. These functions will be discussed in greater detail when these operations are described.

Flip-Flop X03

Flip-flop X03 is used to designate that the I/O channel is either connected or disconnected to the disc file system.

Flip Flop X04

Flip flop X04 is the rate error flip flop. If the condition exists that a transfer from R to V has not occurred when it should, an error condition exists, and the channel error indicator is set (Write operation). During a read operation, X04 may be set by failure of the previous contents of Z to be transferred when the next character must be transferred out of the S register.

Flip Flop X05

Flip-flop X05, when true, allows the sector portion (A18-A23) of the address register to count each sector, but inhibits the generation of a carry into the band portion after the sector exceeds its count of modulo 64.

Data Shift Flip Flops X06-X09

Flip Flops X06 through X09 are used to control the shift of data between the S, Z, and V registers in both the write and read phases. This control is necessary because of the asynchronous slip between the memory computer cycle and the character data rate of the Disc Memory System. This slip can be as great as two memory cycles.

Flip-Flop E01

The error detection flip-flop, E01, is set true by the following error conditions:

a) the address register is full (A12 through A23 all ONES), the coupler is not in the non-increment mode, and the read/write operation has not been terminated.

b) An attempt is made to write into a switch-protected area of the disc.

c) An attempt is made to POT data into the coupler while it is not in the standby phase (00F $\overline{X03}$) or the read or write postamble.

Unit Select Register (G01-G02)

The unit select register is made up of two flip-flops, G01 and G02. These two flip-flops are used during PIN operations only and are controlled by bits 12 and 13 of the "Alert to PIN" EOM instruction. The configuration of G01 and G02 determine which of the four disc units the PIN instruction addresses.

Timing and Data Flow

The remaining paragraphs of this general theory of operations treats the coupler, the selection unit and the disc storage unit as an entity rather than each unit separately in order to present a continuity in the explanation of the read/write timing and data flow operations.

GENERAL READ/WRITE TIMING

In general the timing characteristics for both read and write operations are similar. A read or write operation must be initiated while the disc file unit is in phase zero standby state - that is, in phase zero with the buffer and coupler not connected. Figure 3-8 shows the general timing for either reading or writing the two sectors, 45 and 46. Note that the standby condition exists only while the buffer is disconnected (X03) in phase zero. If

the buffer is connected (X03) in phase zero, the standby condition no longer exists.

If, after the buffer has been connected, the sector addressed by the address register is not immediately available to the read/write heads, the coupler remains in phase zero until the sector portion of the address register (A18 through A23) and the contents of the sector counter (D01 through D06) do become equal to each other. This comparison is made immediately after the sector counter has been incremented by the Sector Pulse. Equality is determined by the sector compare gate SAC. When SAC is true, the address register and the sector counter register contents are equal, signifying that the next sector about to pass under the read/write heads is the addressed sector.

The contents of the D register are counted up by one each time a sector pulse appears. The address register is counted up by one each time the coupler leaves a read or write phase, unless the address is 7777 which is the highest address of a particular unit. The coupler remains in either phase one for writing or in phase two for reading only long enough to write or read the preamble, the data, the parity bits and the postamble. The read and write operations treat the postamble portion in a slightly different manner which will be made clear when these operations are covered in the detailed theory of operations.

During the leading and trailing gaps the coupler returns to phase zero (with the buffer still connected) until the next sector is located. Because the entire operation has not been completed and the buffer is still connected, this condition of phase zero is referred to as the continuation mode. After the final sector has been written or read, the coupler returns to phase zero until the next read/write operation is initiated. The buffer does not disconnect until after the coupler returns to phase zero following the final sector read/write operation.

Figure 3-8 is a timing diagram showing both the phase zero standby and continuation modes.

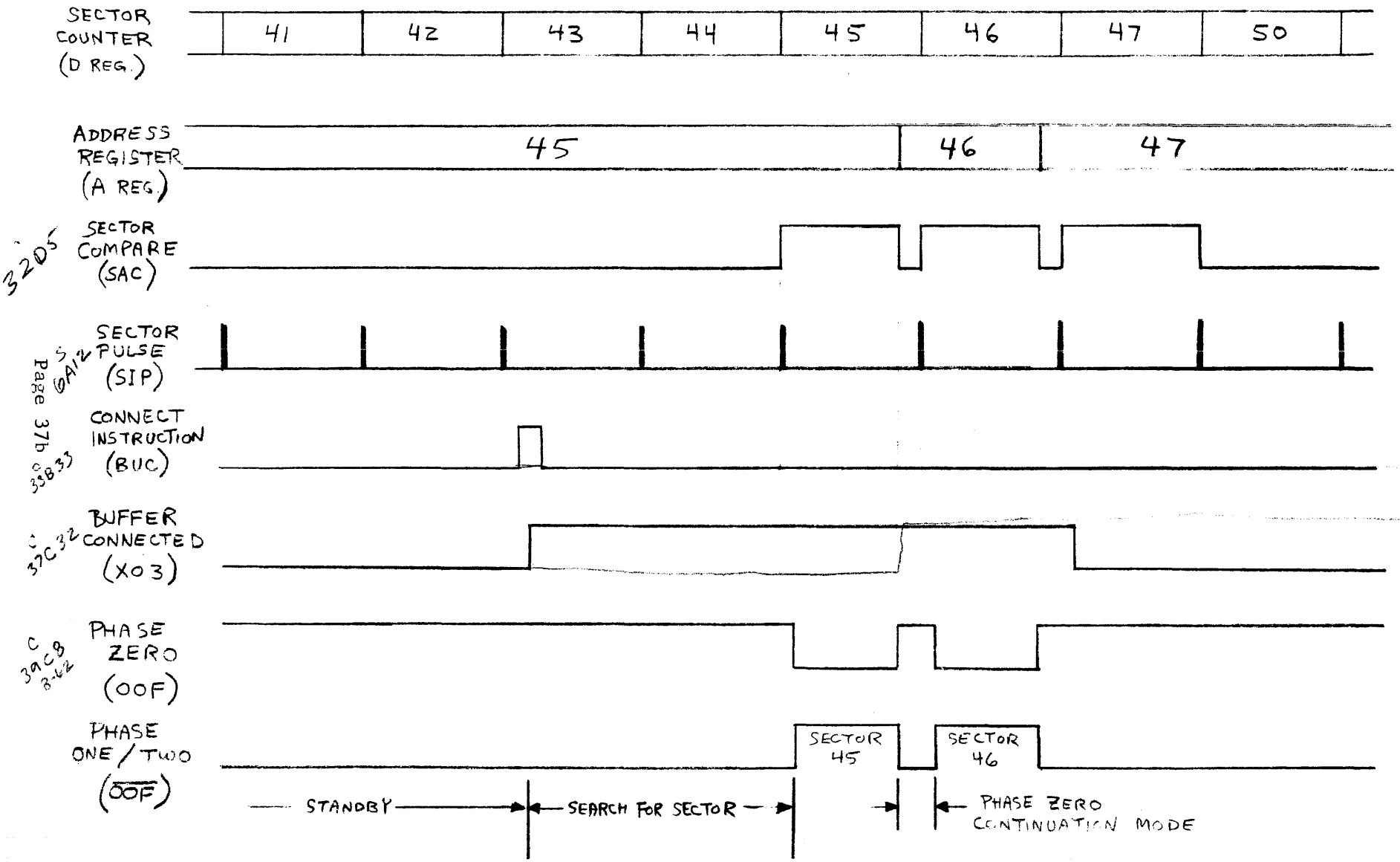


FIGURE 3-8 GENERAL R/W TIMING AND PHASE ZERO

WRITE DATA FLOW

During write operations the 24-bit word is taken from memory and placed into the buffer 24-bit word assembly register WAR. The 12 most significant bits of the 24-bit word are then shifted into the 12-bit single character register SCR of the buffer and then transferred in parallel on lines Rw1 through Rw12 to the character buffer register (V01 through V12) of the coupler. See Figure 3-9. If the character storage register (Z01 through Z12) is empty, the character is transferred into it in parallel from the V register. The 12 bits in the Z register are next transferred in parallel to the S register (S01 through S12) for disassembly.

The S register, which is mechanized in a 3x4 configuration, shifts left one place and the data from S01, S04, S07 and S10 (bits 0, 3, 6 and 9) are transferred in parallel through WD1-WD4 amplifiers and the cable drivers to the write driver circuits, and finally to the four heads selected by the X-Y matrix in the selection unit.

At the next clock pulse the S register again shifts left one place and the data in S01, S04, S07 and S10 (bits 1, 4, 7 and 10) are written in the same manner as described above. This serial-parallel shifting of the S register continues until the entire 12-bit character has been written. Three clock pulses are required to empty the S register of its 12-bit character. As bits 2, 5, 8 and 11 are clocked out of the S register the next 12-bit character (bits 12-23) of the original word is already waiting in the Z register to be transferred in parallel to the S register and the process described above is repeated until the complete sector has been written. The coupler has the ability to store two 12 bit characters while the S register is disassembling a character, provided that the I/O channel was able to access them from the computer memory. After the final character of each sector is recorded, one parity bit is written one each of the four tracks. Each track must contain an odd number of one bits, including the parity bit; therefore, one complete sector will contain an even number of one bits on all four tracks.

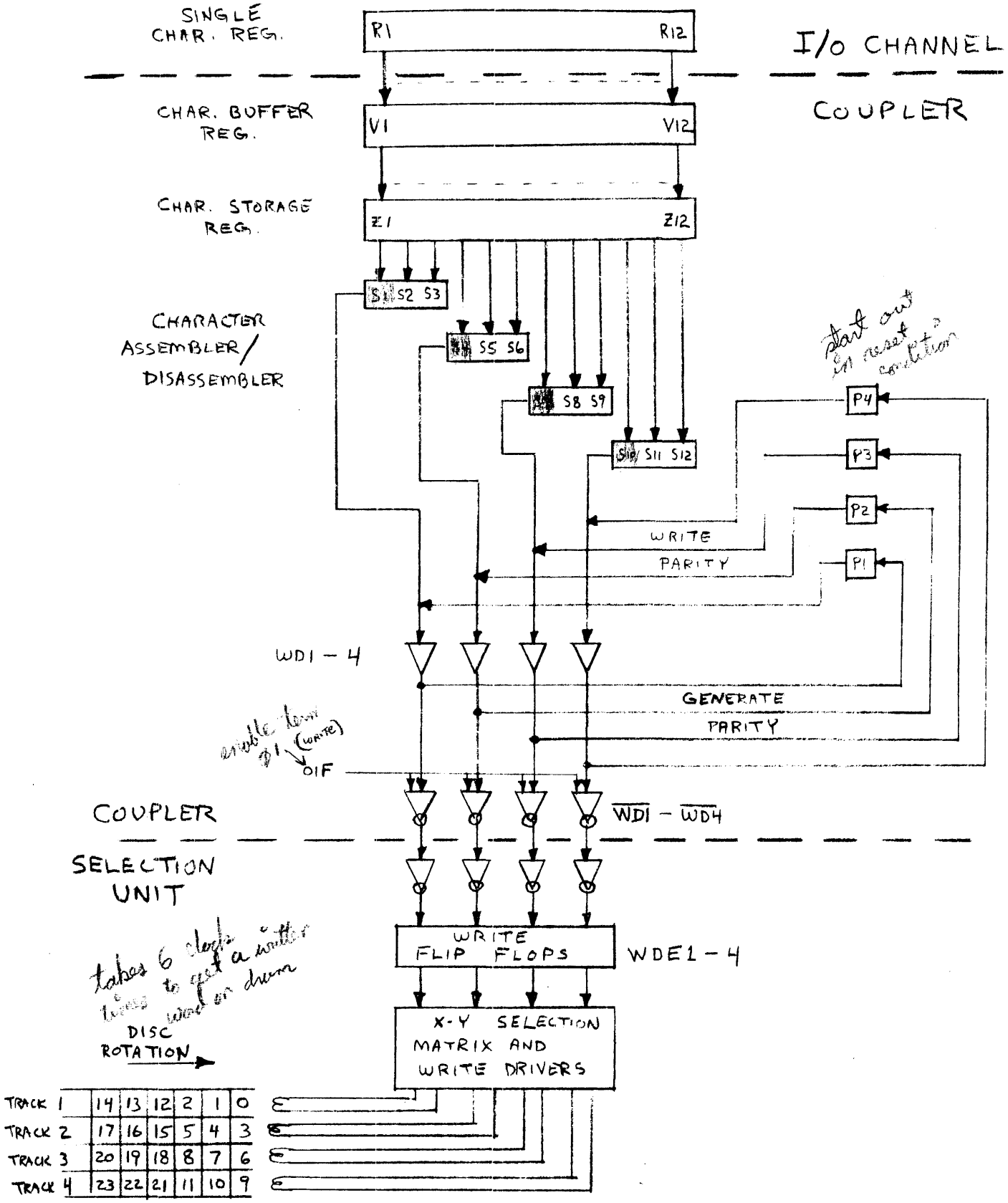


FIGURE 3-9 WRITE FLOW DIAGRAM

LS

READ FLOW

During read operations the information is read four bits in parallel from the disc, is decoded, amplified, and transferred to the S register in a serial-parallel manner. Refer to Figure 3-10, Read Flow Diagram. As each four bits are transferred into the S register, the S register shifts left one place. After three clock pulses the S register is filled with one 12-bit character. At the next clock pulse, the 12-bit character in the S register is transferred to the Z register, and the next four binary digits are read from the disc and transferred to the S register via the input gates to S03, S06, S09 and S12. Also if the V register is empty, this same 12 bit character will pass through the Z in parallel into the V register. As each bit is read from each of the four tracks, parity flip-flops P01 through P04 keep track of parity. After the entire sector has been read these parity flip-flops compare their present states with the odd parity bit previously written on the corresponding tracks. If they do not compare, the error signal WES is sent to the I/O channel. The contents of the Z register are transferred to the buffer on lines $\overline{Zw1}$-$\overline{Zw12}$

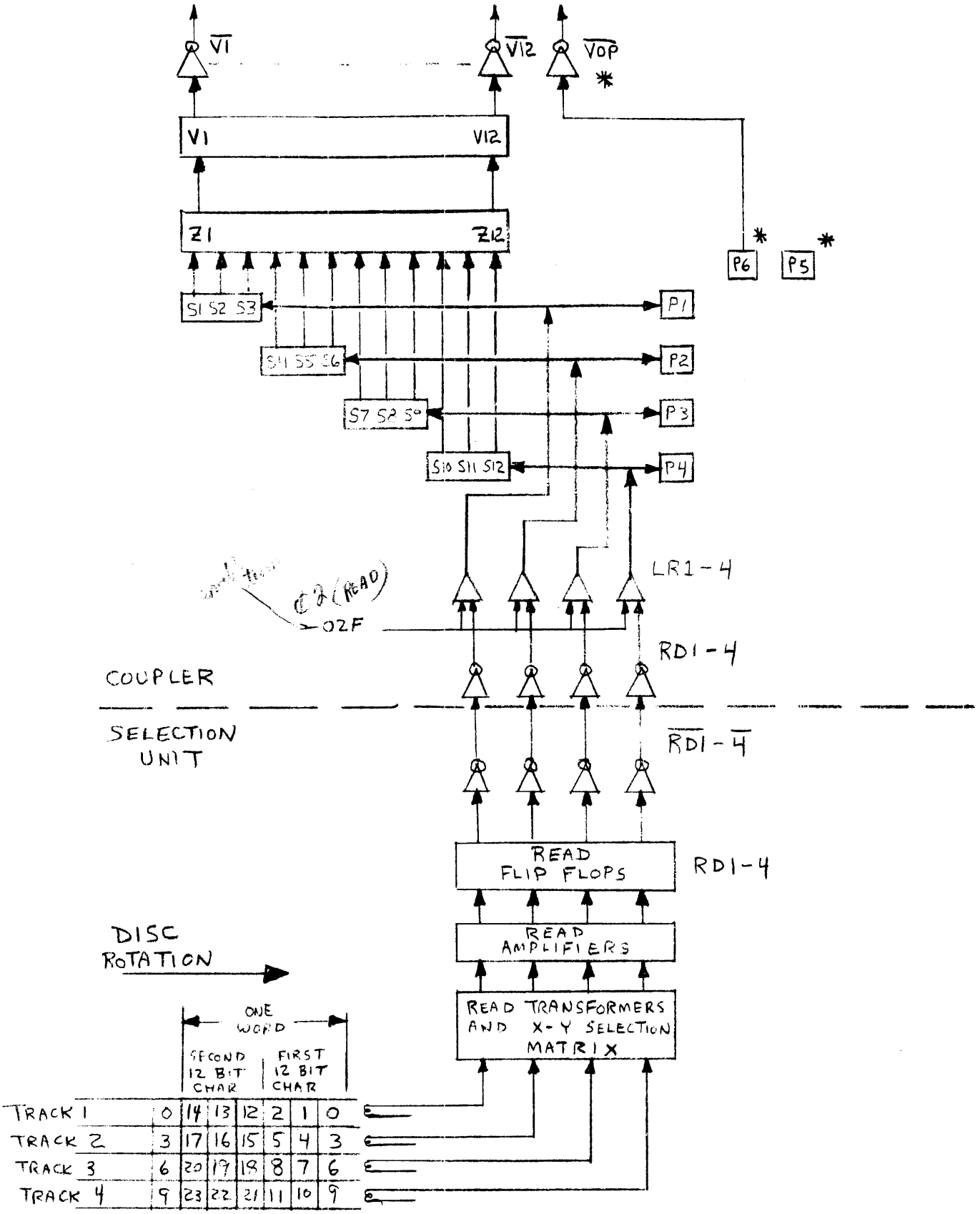


FIGURE 3-10 READ FLOW DIAGRAM

* DELETED ON LATER MODELS

DETAILED
LOGIC DESCRIPTION

The remaining portions of this section treat in greater detail the read and write operations of the Rapid Access Disc File Model 9367C. Logic equations and timing charts are used to implement the text to give a clear picture of each operation or status of the RAD system.

For purposes of simplicity in expressing logic equations in the text, all flip-flop input logic terms use the following symbols: y and z for direct set and direct reset, s and r for dc true and false inputs, and t for toggle flip-flop inputs.

A logic list with appropriate symbols and gate terminology will be found in Section V of this manual.

A glossary of logic terms and input/output signals is also furnished in Section V. Frequent reference to this glossary will be of value in clarifying the RAD operations described in the following text.

Power Failure Detection

The basic power failure detection scheme is shown in Figure 3-11, Power Failure Detection Circuitry. The two SK60 Power Detectors are located in the 9367C coupler chassis. One SK60 detects ac power failure in the I/O buffer which supplies the dc power to the coupler; the other SK60 detects ac power failure in the selection unit. The SK60 Primary Power Detectors require an ac input of approximately 10 volts RMS, therefore, step-down transformers are required at their inputs.

Under normal operating conditions the SK60 outputs are at ground level, the relays are energized, and the PWR term is high. If primary power fails, the filtered dc power supplies in the I/O buffer or in the basic selection unit will maintain usuable dc voltages for several milliseconds to satisfy normal operation for that length of time.

If ac power fails, or drops below a level established by a threshold adjustment on the SK60, the output of the detector goes to +25 volts which deenergizes the relay and drops the PWR term to ground level.

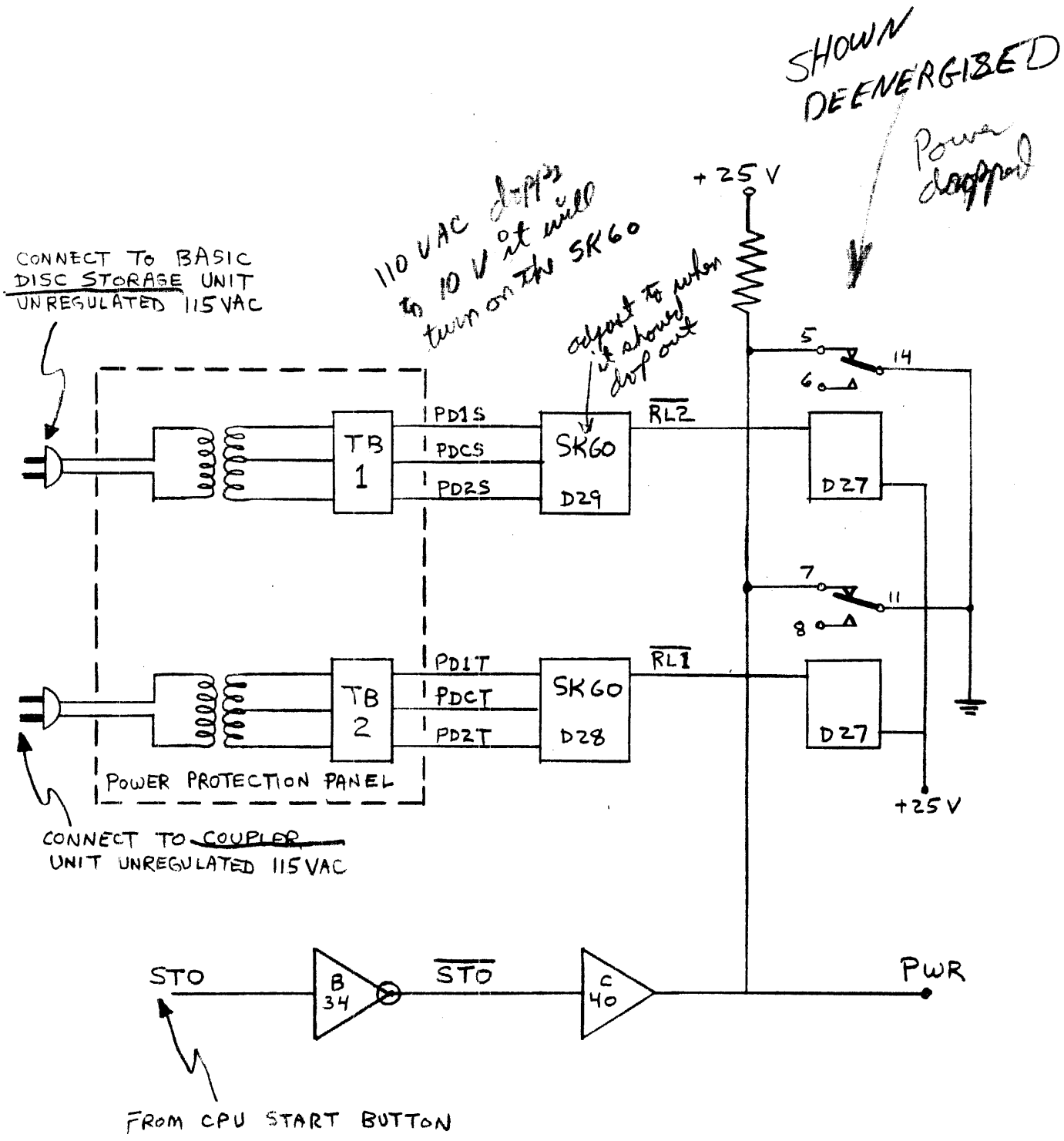


FIGURE 3-11 POWER FAILURE DETECTION CIRCUITRY

LS

As PWR drops to zero volts the output drivers of the write amplifiers are inhibited from further writing, the coupler sequences to phase zero, the buffer disconnects, the address register is cleared to zeros, and flip-flops U01, through U03 and X01 through X04 are reset.

$$zG01\text{-}G02 = PWR$$
$$zF01\text{-}F02 = \overline{DRA}$$
$$zX01\text{-}X04 = PWR$$
$$zU01\text{-}U03 = \overline{DRA}$$
$$zA09\text{-}A23 = \overline{DRA}$$
$$\overline{DRA} = \overline{ACT}\ PWR$$
$$zU04\text{-}U06 = PWR$$

The STO term from the Start button on the computer control panel is effectively "anded" with the PWR term. When the Start button is depressed PWR is grounded and the same action occurs as described for power failure.

Unit Selection Circuitry

If there are two, three, or four disc storage units connected to a disc file system, some means must be provided for enabling the addressed unit and disabling the remaining units. Figure 3-12, Unit Select Gates for Read/Write Operations, shows the method of generating and distributing the unit select terms USL and $\overline{USL}$. Note the precession of pins 40 through 43 within the cables P168 and P169. This permits the proper address signal to be taken from the same pin (pin 43) of each selection unit without changing address selection gates since the gates are originated in the coupler and not in the selection units. This scheme allows any selection unit to be substituted for any other without rewiring address gate circuits.

The selection gate USL is part of the input gating to the write flip flops and x selection circuits.

If USL is not true, no data can be impressed into the write heads by the write drivers. During read operations the unit select term is inverted ($\overline{USL}$) and is used at the disable input of the AX14 cable drivers (RD1-RD4) in the selection unit. The $\overline{USL}$ term enables the cable drivers of the selected unit, and disables the cable drivers of the non-selected units.

Bits A09 and A10 of the address register determine the address of the selected unit for reading and writing.

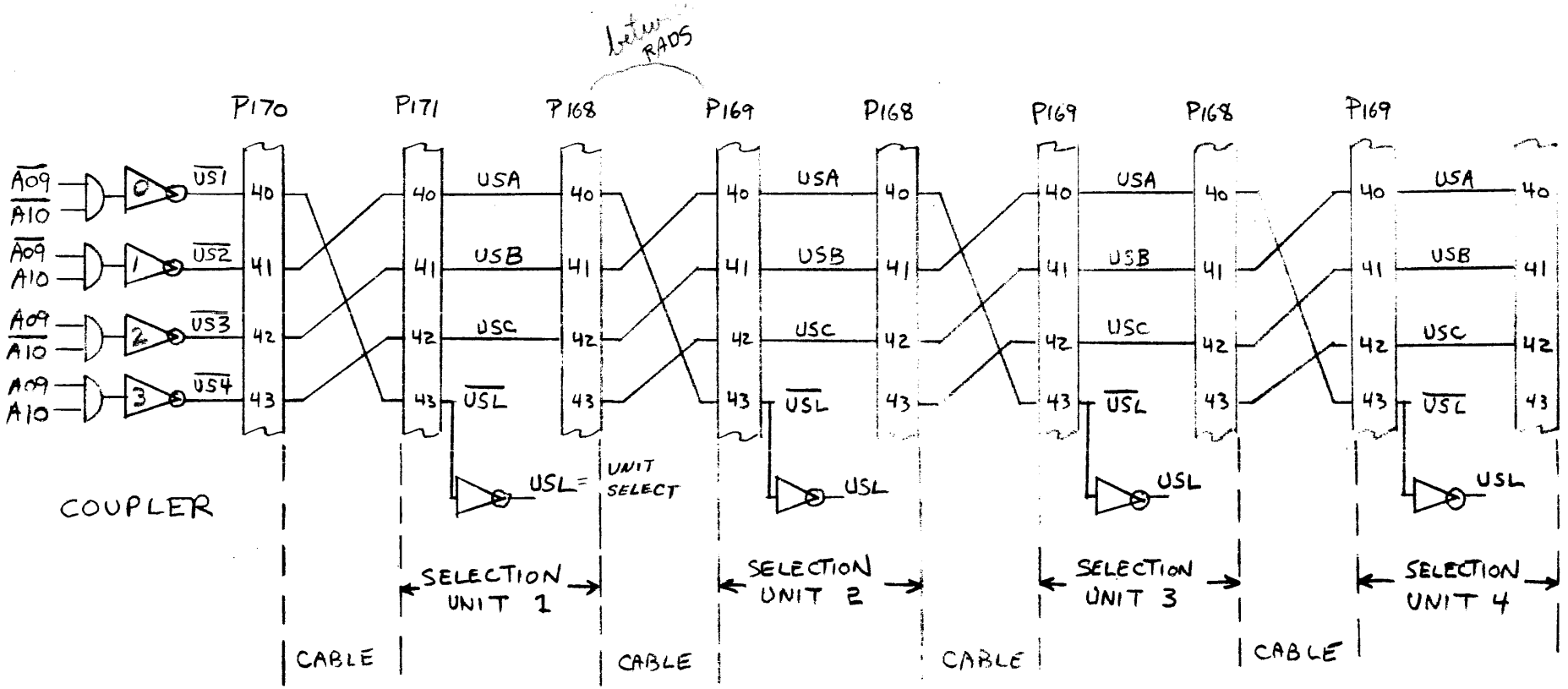


FIGURE 3-12 UNIT SELECT FOR READ/WRITE OPERATIONS

Head Selection Circuitry

Head selection within each of the selection units is similar for both reading and writing. The X-Y matrix in each selection unit is made up of 16 Y-Selector circuits and 16 X-Selector circuits. Because data must be read or written onto the four separate tracks of a band concurrently, one Y-Selector and four X-Selectors are gated in such a manner that four X-Y coordinates exist - one for each of the heads of the selected band.

The 16 Y-Selectors are Y01 through Y16. Input gates to the Y-Selectors are controlled by the status of A11, A12, A13, A14, and A15 of the address register. The output of each Y-Selector is connected to the center tap windings of 16 read/write heads.

There are actually 20 X-Selector circuits that are divided into two groups; sixteen X-Selectors in one group, and four in the other groups. One group is used only for writing, the other group for reading. In the group used for writing, are four sets of four identical circuits, so in effect there are only four X selectors. Thus the matrix is actually 4 x 16, thus selecting only one band out of 64. Each write X select circuit enables one Write Driver circuit. Four are always enabled at one true, one for each bit. The other X selector group is used only for reading and comprises only 4 selector circuits. Each of these X selectors enable four of the 16 read transformers. The address register terms that enable both the read and write X selectors are A16 and A17. See figure 3-13.

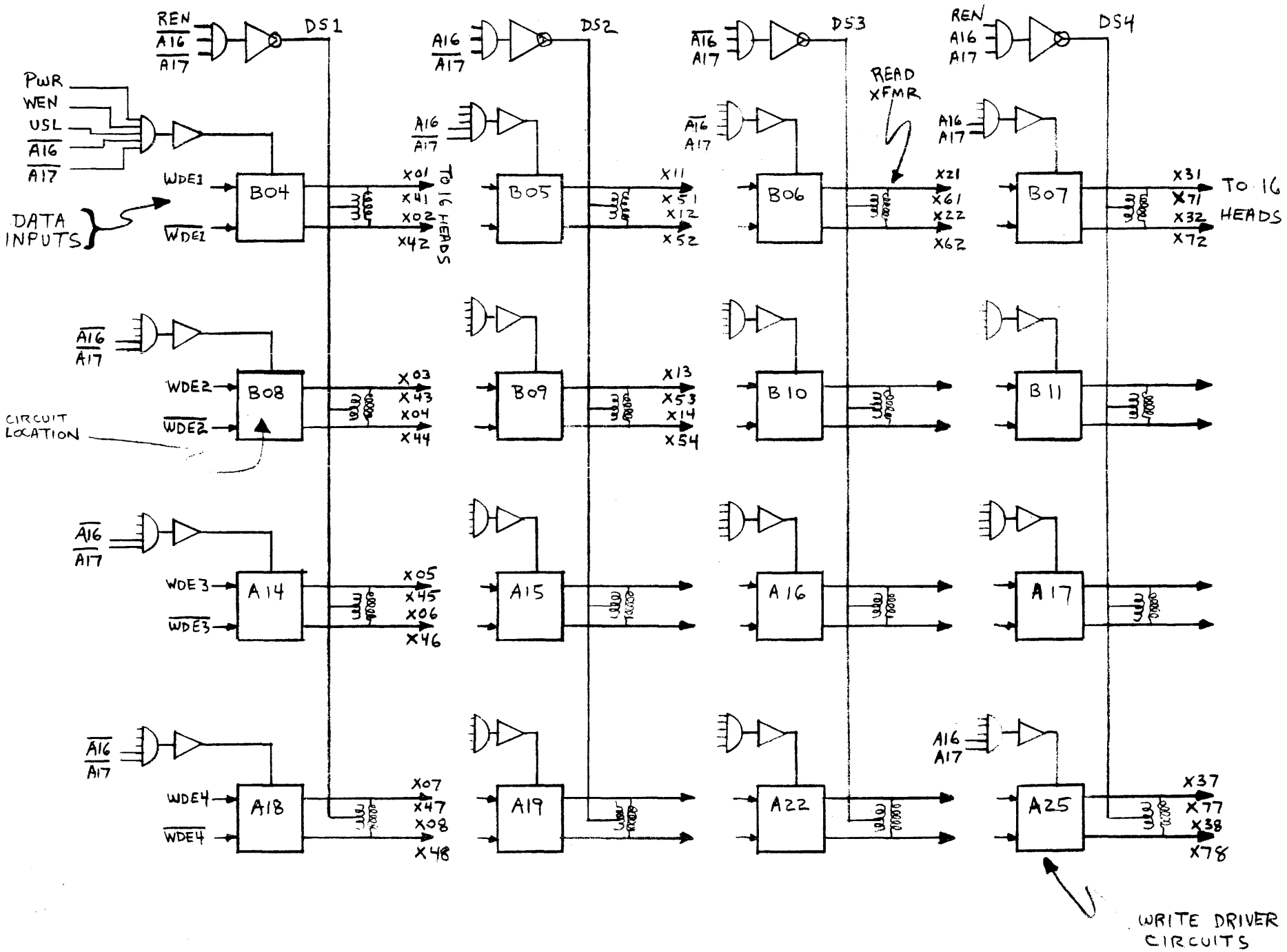


FIGURE 3-13 9367 C "X" SELECTION CIRCUITS

Logic for both X and Y selection is given below. Table 3-5 presents the X-Y coordinates by band address (bits A12 through A17) for both read and write.

Y-Selector Logic

Y01 =	$\overline{A11}$	$\overline{A12}$	$\overline{A13}$	$\overline{A14}$	$\overline{A15}$
Y02 =	"	"	"	"	A15
Y03 =	"	"	"	A14	$\overline{A15}$
Y04 =	"	"	"	A14	A15
Y05 =	"	"	A13	$\overline{A14}$	$\overline{A15}$
Y06 =	"	"	"	$\overline{A14}$	A15
Y07 =	"	"	"	A14	$\overline{A15}$
Y08 =	"	"	"	A14	A15
Y09 =	"	A12	$\overline{A13}$	$\overline{A14}$	$\overline{A15}$
Y10 =	"	"	"	$\overline{A14}$	A15
Y11 =	"	"		A14	$\overline{A15}$
Y12 =	"	"	"	A14	A15
Y13 =	"	"	A13	$\overline{A14}$	$\overline{A15}$
Y14 =	"	"	"	$\overline{A14}$	A15
Y15 =	"	"	"	A14	$\overline{A15}$
Y16 =	$\overline{A11}$	A12	A13	A14	A15

X Selector Logic

	Read			Write					
$\overline{DSI}$ =	REN	$\overline{A16}$	$\overline{A17}$	X01-08, 41-48=	PWR	WEN	USL	$\overline{A16}$	$\overline{A17}$
$\overline{DS2}$ =	"	A16	$\overline{A17}$	X11-18, 51-58=	"	"	"	A16	$\overline{A17}$
$\overline{DS3}$ =	"	$\overline{A16}$	A17	X21-28, 61-68=	"	"	"	$\overline{A16}$	A17
$\overline{DS4}$ =	"	A16	A17	X31-38, 71-78=	"	"	"	A16	A17

Band Address	Write Y Selection	Write X Selection	Read X Selector Outputs	Read X Selector Gate
00	Y01	X01-X08	RX01-RX08	DS1
01	Y01	X21-X28	RX21-RX28	DS3
02	Y01	X11-X18	RX11-RX18	DS2
03	Y01	X31-X38	RX31-RX38	DS4
04	Y02	X01-X08	RX01-RX08	DS1
05	Y02	X21-X28	RX21-RX28	DS3
06	Y02	X11-X18	RX11-RX18	DS2
07	Y02	X31-X38	RX31-RX38	DS4
10	Y03	X01-X08	RX01-RX08	DS1
11	Y03	X21-X28	RX21-RX28	DS3
12	Y03	X11-X18	RX11-RX18	DS2
13	Y03	X31-X38	RX31-RX38	DS4
14	Y04	X01-X08	RX01-RX08	DS1
15	Y04	X21-X28	RX21-RX28	DS3
16	Y04	X11-X18	RX11-RX18	DS2
17	Y04	X31-X38	RX31-RX38	DS4
20	Y05	X01-X08	RX01-RX08	DS1
21	Y05	X21-X28	RX21-RX28	DS3
22	Y05	X11-X18	RX11-RX18	DS2
23	Y05	X31-X38	RX31-RX38	DS4
24	Y06	X01-X08	RX01-RX08	DS1
25	Y06	X21-X28	RX21-RX28	DS3
26	Y06	X11-X18	RX11-RX18	DS2
27	Y06	X31-X38	RX31-RX38	DS4
30	Y07	X01-X08	RX01-RX08	DS1
31	Y07	X21-X28	RX21-RX28	DS3
32	Y07	X11-X18	RX11-RX18	DS2
33	Y07	X31-X38	RX31-RX38	DS4
34	Y08	X01-X08	RX01-RX08	DS1
35	Y08	X21-X28	RX21-RX28	DS3
36	Y08	X11-X18	RX11-RX18	DS2
37	Y08	X31-X38	RX31-RX38	DS4
40	Y09	X41-X48	RX01-RX08	DS1
41	Y09	X61-X68	RX21-RX28	DS3
42	Y09	X51-X58	RX11-RX18	DS2
43	Y09	X71-X78	RX31-RX38	DS4

Table 3-5 X-Y Selection coordinates by band addresses.

Band Address	Write Y Selection	Write X Selection	Read X Selector Outputs	Read X Selector Gate
44	Y10	X41-X48	RX01-RX08	DS1
45	Y10	X61-X68	RX21-RX28	DS3
46	Y10	X51-X58	RX11-RX18	DS2
47	Y10	X71-X78	RX31-RX38	DS4
50	Y11	X41-X48	RX01-RX08	DS1
51	Y11	X61-X68	RX21-RX28	DS3
52	Y11	X51-X58	RX11-RX18	DS2
53	Y11	X71-X78	RX31-RX38	DS4
54	Y12	X41-X48	RX01-RX08	DS1
55	Y12	X61-X68	RX21-RX28	DS3
56	Y12	X51-X58	RX11-RX18	DS2
57	Y12	X71-X78	RX31-RX38	DS4
60	Y13	X41-X48	RX01-RX08	DS1
61	Y13	X61-X68	RX21-RX28	DS3
62	Y13	X51-X58	RX11-RX18	DS2
63	Y13	X71-X76	RX31-RX38	DS4
64	Y14	X41-X48	RX01-RX08	DS1
65	Y14	X61-X68	RX21-RX28	DS3
66	Y14	X51-X58	RX11-RX18	DS2
67	Y14	X71-X78	RX31-RX38	DS4
70	Y15	X41-X48	RX01-RX08	DS1
71	Y15	X61-X68	RX21-RX28	DS3
72	Y15	X51-X58	RX11-RX18	DS2
73	Y15	X71-X78	RX31-RX38	DS4
74	Y16	X41-X48	RX01-RX08	DS1
75	Y16	X61-X68	RX21-RX28	DS3
76	Y16	X51-X58	RX11-RX18	DS2
77	Y16	X71-X78	RX31-RX38	DS4

Table 3-5 (Continued)

OPERATIONAL STATES

The 9367C Disc File system operates in one of three separate phases or sequences which are controlled by flip-flops F01 and F02. These three phases are listed in Table 3-6. Phase Counter.

Flip-Flops		Phase	Logical Name	Condition
F01	F02			
0	0	Phase Zero	00F	Standby/GAP
0	1	Phase One	01F	Write
1	0	Phase Two	02F	Read

Table 3-6, Phase Counter

Phase Zero

If the buffer connect flip-flop, X03, is false in phase zero (00F $\overline{X03}$), the coupler is in a standby or ready state. A read/write operation should be initiated only when the coupler is in this standby condition. When the coupler is in phase zero with the connect flip-flop X03 true (00F X03), either a read/write operation has been initiated, or one is in progress and has not been completed.

Phase One

All write operations occur while the coupler is in phase one. Phase one begins with the preamble and ends eleven clock pulses after the parity bit has been written.

Phase Two

All read operations occur while the coupler is in phase two. Phase two begins with the preamble and ends after the last character has been accepted by the channel.

Clock

When power is initially turned on the coupler assumes the condition representing phase 0.

$$00F = \overline{F01}\ \ \overline{F02}$$

The clock pulses in phase 0 and phase 1 are derived from a write clock track consisting of 27,712 bits permanently recorded around the circumference of the recording surface. The nominal bit frequency in 800K bits/sec. at a 2% slip

of the device motor. The wave form of this clock is a .5 usec. pulse inverted by the line driver and called $\overline{CLK}$ and occurs every 1.2 usec. The clock for the read phase is derived from the data being read.

The signal $\overline{RCN} = \overline{02F}$

is used in the selection Unit to select the write clock.

INITIATING A READ/WRITE OPERATION

The timing considerations in 00F (phase zero) to initiate either a read operation or a write operation are identical. The only difference is whether the coupler enters 01F (phase one) or 02F (phase two) when leaving 00F. This, in turn, depends on the status of W9 in the I/O buffer. If W9 is true, the coupler sequences from 00F to 01F for writing; if W9 is false, the coupler sequences from 00F to 02F for reading. W9 = WRITE $\overline{W9}$ = READ

To initiate either a read or write operation, the program normally presents six instructions in the following order:

a)	EOM, I/O mode	(Alert to POT)
b)	POT	(Load coupler address register)
c)	EOM, ALC	(Alert channel interlace)
d)	EOM, I/O mode	(Establishes termination mode)
e)	POT	(Load interlace word)
f)	EOM Buffer mode	(Connect RAD to channel)

The generalized timing diagram of Figure 3-17 will aid in clarifying the following logical explanation of these instructions and how they affect the disc file coupler and selection unit.

Response to an EOM - Alert to POT

An EOM to POT an address from the computer always sets U06, a dc flip flop.

Data address to Pot → sU06 = IDT

$IDT = DMA\ \overline{C16}\ IOC$ EOM

where

Rad address in Cmp. → $DMA = \overline{C17}\ C19\ \overline{C20}\ C21\ C22\ \overline{C23}$ 26

If the coupler is in Ø0 or in any but the postamble of Ø1 or Ø2, X01 is set on the first PTQ (POT 1 from computer) that occurs due to the execution of the POT instruction, which must follow the EOM Alert to POT which initially caused U06 to set. The PTQ is derived from a delta gate on the cable plug module for the POT cable.

up in Ø2

$PTQ = \overline{POT\ 1\ Q2}$

alert to POT POT = NUF = Ø0 + NOT POSTAMBLE

sX01 = NUF U06 PTQ Page 13 in Print

where $\overline{U01}\ \overline{U02}\ \overline{00F}$ = NUF

and $\overline{U01}\ \overline{U02}$ = postamble of the read or write phase

If the coupler is in the postamble of Ø1 or Ø2, X01 will not be set until the first PTQ to occur after the coupler enters phase 0 immediately after the postamble. The true level of the next PTQ in Ø0 also resets U06.

rU06 = X01 PTQ

The flip flop, X02, is set at the same time as X01 provided that the POT was given at a legitimate time; that is, during Ø0 or in LAST postamble time ~~and the channel is not connected to the coupler~~. If the POT occurs while still in the postamble, X02 will set as soon as the phase counter enters phase 0.

yX02 = 00F $\overline{X03}$ X01 idle condition

The RTO is the response signal to the CPU telling it to leave Ø2 of the POT command. ~~This~~ is generated by X01. The RTO is sent to the CPU any time that X01 is set.

RTO = X01 PT1

rX01 = NUF PT1

The RTO is disabled at the driver whenever $\overline{X01}\ \overline{X02}$ is true. Normally X02 would be in the set state at this time, and the address register loading takes place after the clearing of the A register by ACT.

z(A09-A23) = DRA → direct reset for A register

where DRA = ACT + $\overline{PWR}$

ACT = 00F $\overline{X03}$ U06 = Ø0 · NOT CONNECTED · ALERT TO POT

$\overline{PWR}$ = Power detection circuit indicated that the voltage is going off or that the Start button on the CPU console is depressed.

yA09 = C09 LDA

yA23 = C23 LDA address lines go to the RAD "A" register

where LDA = X01 X02 PTQ

POT ALERT TO PWR POT1

If the POT was given at an illegitimate time, the A register will not be cleared due to the 00F and the $\overline{X03}$ in the ACT equation. If either of these are missing it would signify that the coupler was in some state other than standby and disconnected. Also at this illegitimate time, no setting of a new address into the A register would occur because X02 is false. The error flip flop would then be set upon issuance of the POT command if X01 was set

and X02 reset.

$$yE01 = X01\ \overline{X02}\ PTQ$$

Figure 3-14 shows the timing relationships of the signals used during an Alert to POT and POT sequence executed while the RAD coupler was in Ø0 standby mode. Figure 3-15 shows the same signals occurring while the coupler is in a Ø1 or Ø2 postamble. Note that in this figure that the end of postamble (00F) occurs during PTQ resulting in a shorter ACT. If 00F occured slightly later X01 would have to wait until the following PTQ to set. Thus U06 would have to wait an additional machine cycle before it could reset thus keeping ACT up almost 1.75 us. longer.

Flip flops X01 and X02 are both reset by the end of PT1.

$$rX01 = NUF\ PT1$$

$$rX02 = PT1 + ...$$

Flip flop U01 indicates that the coupler has accepted a new address.

$$yU01 = LDA$$

Flip-flop X05 follows the output of C14 and determines the non-increment mode status.

$$sX05 = C14\ TNI$$

$$rX05 = \overline{C14}\ TNI$$

$$TNI = \overline{X03}\ IDT\ (\overline{NUF} + 00F)$$

The setting of X05 signifies that in the read or write operation that is to follow, the address register cannot alter its current band address as the sector portion (A18-A23) counts from 00 to 77. TNI is a term that specifies the time to set X05, which is during an alert to POT command if given at a proper time.

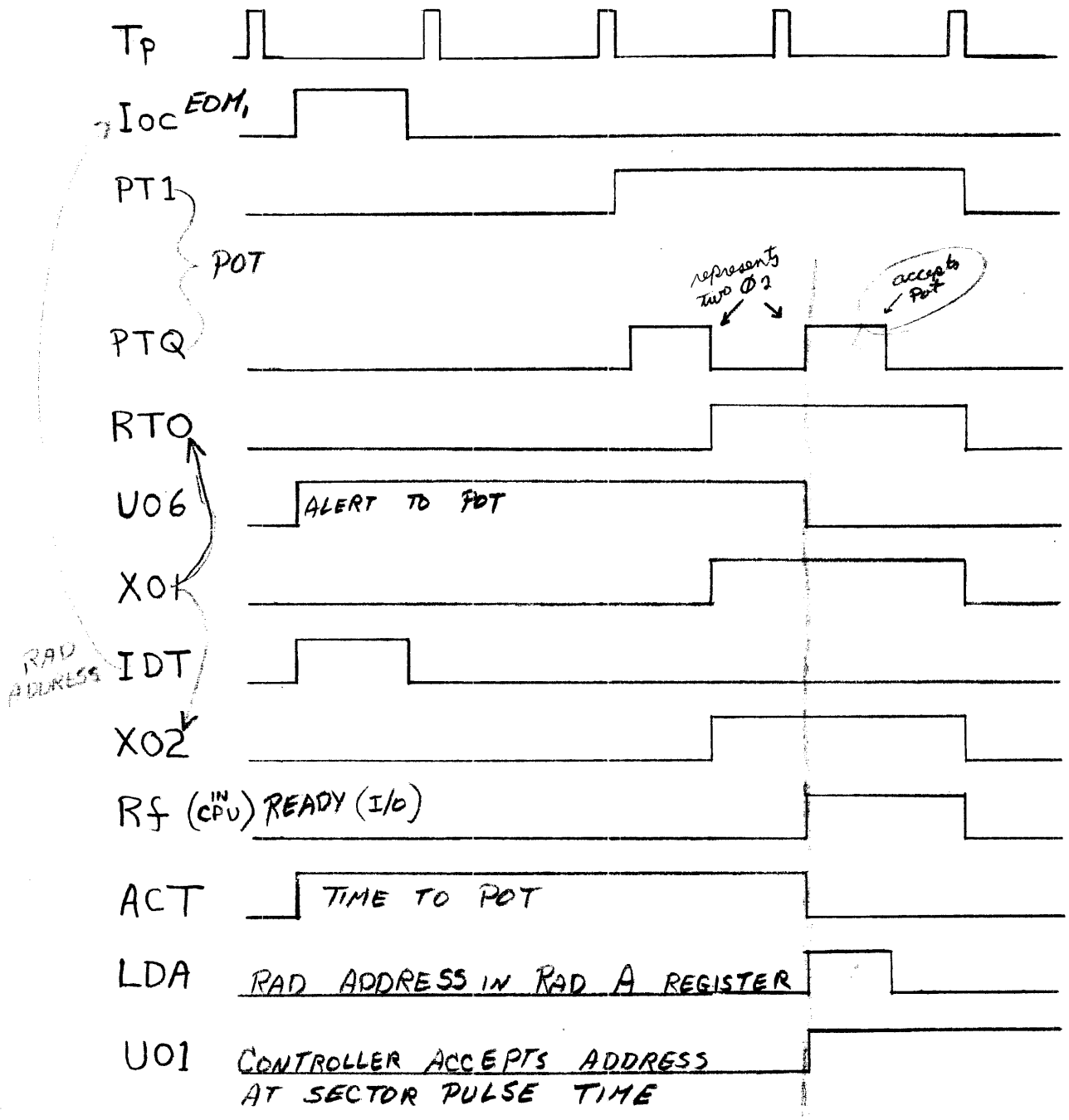


FIGURE 3-14 POT ADDRESS TO A REGISTER WHEN IN STANDBY MODE

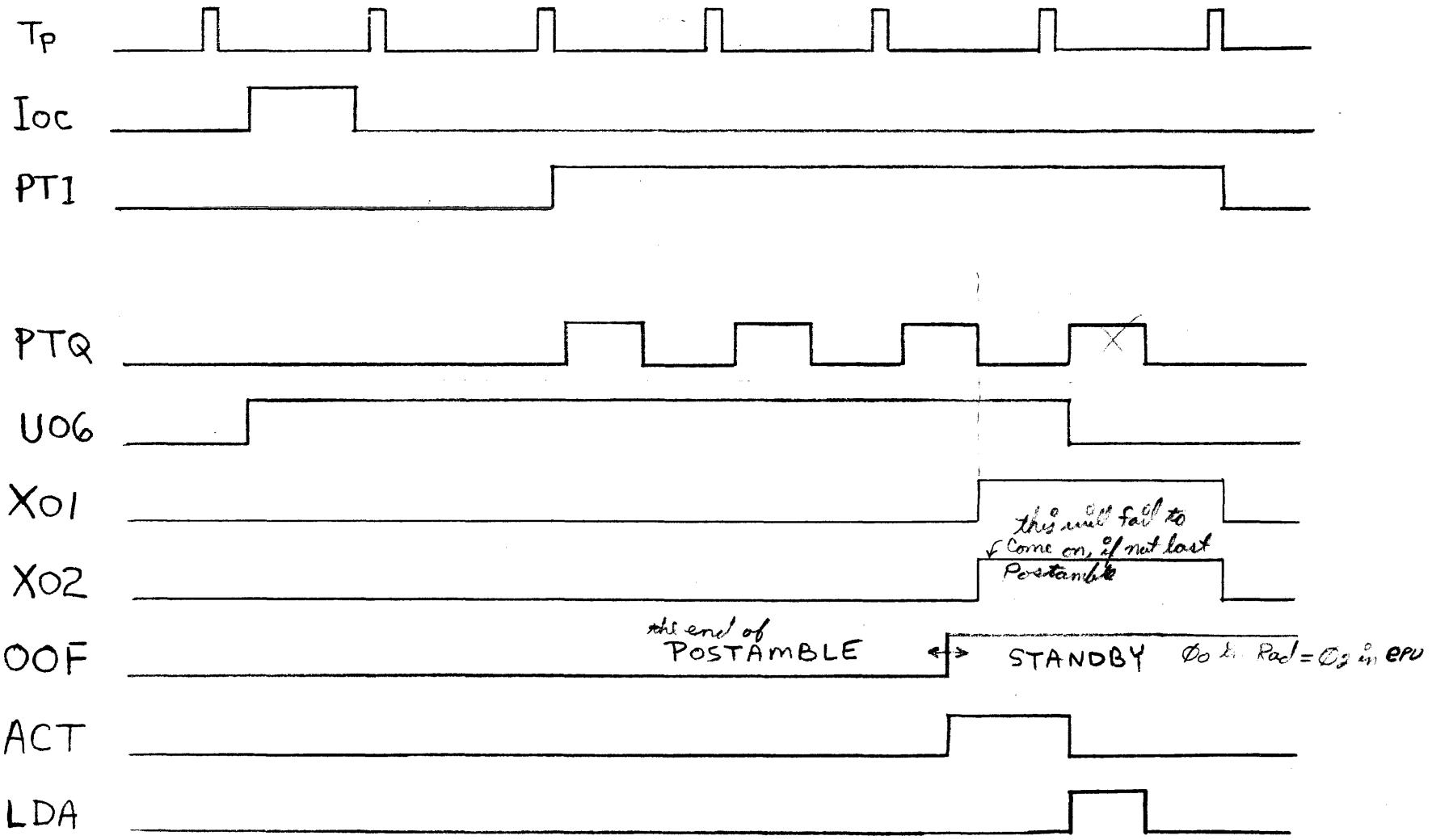


FIGURE 3-15 POT ADDRESS WHILE IN POSTAMBLE

Table 3-7 shows the effects on U06, X01 X02, E01, LDA and ACT as a result of the POT command being executed during various conditions of the coupler.

CONDITION		ØØ KEY TERM IDLE	$\overline{Ø0}$ $\overline{U01}$ $\overline{U02}$ POSTAMBLE	$Ø0 + \overline{Ø0}\ \overline{U01}\ \overline{U02}$ OTHER TIMES
SET	U06	IMMEDIATE	IMMEDIATE	IMMEDIATE
RESET	U06	2nd PTQ	2nd PTQ in ØØ	2nd PTQ
SET	X01	1st PTQ	1st PTQ in ØØ	1st PTQ
RESET	X01	PT1	Wait for PT1 in ØØ	PT1
SET	X02	1st PTQ	1st PTQ in ØØ	NEVER
SET	E01	NEVER	NEVER	2nd PTQ ERROR
ACT		U06	Wait for ØØ	NEVER
LDA =	V01	2nd PTQ	2nd PTQ in ØØ	NEVER

TABLE 3 - 7 POT CONDITIONS

Initiation of a Read/Write Operation

If a new address has been loaded into the A register (U01 = 1) and the POT action is complete (X01 = 0), the next sector pulse, SIP, triggers a 4.0 usec. one shot, BSC.

BSC = 4 μsec

sBSC = 00F HSD SIP

where HSD = U01 $\overline{X01}$ +.....

SIP → SID → SEC (63) → SIM

This sector pulse SIP, is derived from the pulses recorded on the sector track in the following manner. The pulses are read from the disc and amplified (SID) and decoded so as to distinguish the 63 sector pulses (SEC) from the one index pulse (IDX) per revolution of the disc.

The sector and index pulses generate a term, SIM, which is used to reset a flip flop YSC, during the sector/index pulse time. This flip flop generates the SIP pulse used in the coupler and also allows setting the band address flip flops in the selection unit at the sector pulse time. These band flip flops, A11-A15, contain the same band address bits that are in the coupler address register (A reg.) These are used so that the head selection matrix will not be changed during the Data time, even though a POT command may be issued at any time. See Figure 3-16.

SIP = $\overline{YSC}$ SECTOR INCREMENT PULSE

sYSC = $\overline{SIM}$ WCK

rYSC = SEC WCA

SET IN THE BAND ADDRESS

where SIM = SEC+IDX SECTOR OR INDEX PULSE

sWCK = $\overline{SIM}$ WCA NOT SIP AND CLOCKED

rWCK = WCA + IDX CLOCK OR INDEX PULSE

WCA is output of clock pulse read amplifier.

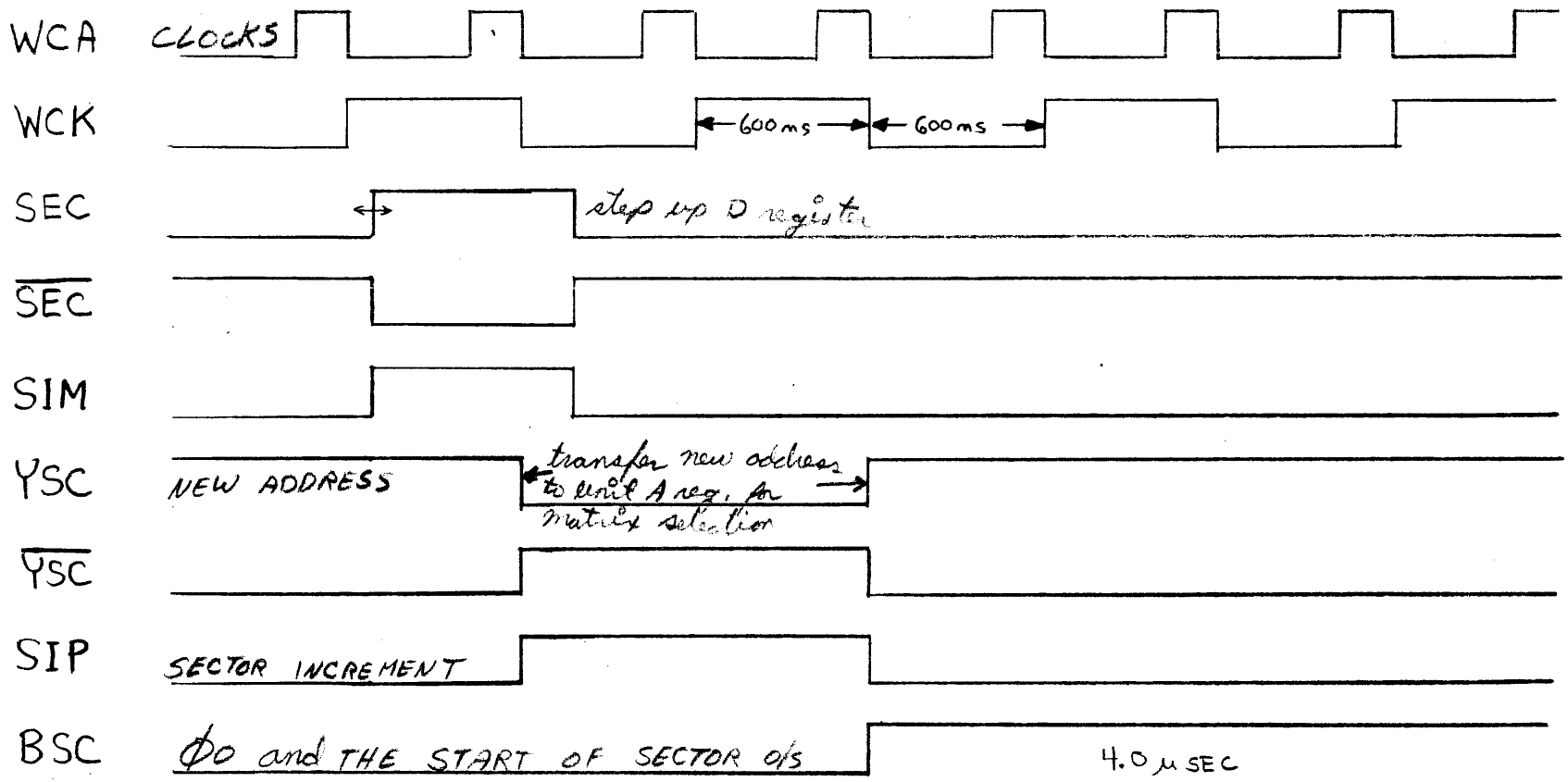


FIGURE 3-16 SECTOR PULSE TIMING

The D register in the selection unit is also incremented by the sector pulse SEC.

$$tD06 = \underline{SEC}$$

$$tD05 = \underline{D06}$$

$$tD01 = \underline{D02}$$

$$zD01\text{-}D06 = \overline{IDX}$$

The one shot BSC defines the time that a comparison between the D register and the sector portion of the A register is made. Therefore both of these registers must not change during the time that BSC is true. To insure this SIP is true for at least 1.2 usec. This is the time that the D register is incrementing. The A register is filled by the POT command or the AIN term and it will be stable for at least 1 usec. before BSC starts. This is insured by the fact that BSC cannot set until X01 is reset and X01 cannot be reset until the end of PT1. During the time that BSC is true the current sector address is compared with the sector address in the A register, and if they are equal the flip flop U02 is direct set by the sector compare gate, SAC.

$$yU02 = 00F\ BSC\ SAC\ HSD$$

where

$$SAC = CUH\ CLH$$

$$CUH = \overline{A18\ \overline{CD1} + \overline{A18}\ CD1 + A19\ \overline{CD2} + \overline{A19}\ CD2 + A20\ \overline{CD3} + \overline{A20}\ CD3}$$

$$CLH = \overline{A21\ \overline{CD4} + \overline{A21}\ CD4 + A22\ \overline{CD5} + \overline{A22}CD5 + A23\ \overline{CD6} + \overline{A23}\ CD6}$$

If the buffer has not been connected by this time, a signal is generated which may be used as an input to the priority interrupt chassis. This signal indicates that the search for desired sector has ended and that there is about 15 usec. before the preamble bits are available to be read or written. This gives the computer time to set up the interlace registers in the Input/ Output channel and connect the RAD to the channel with a BUC type EOM.

$$INT = 00F\ BSC\ SAC\ U01\ \overline{X01}\ \overline{X03}$$

Figure 3-17 shows the most important timing relationships starting from the Alert to POT command to the preamble time.

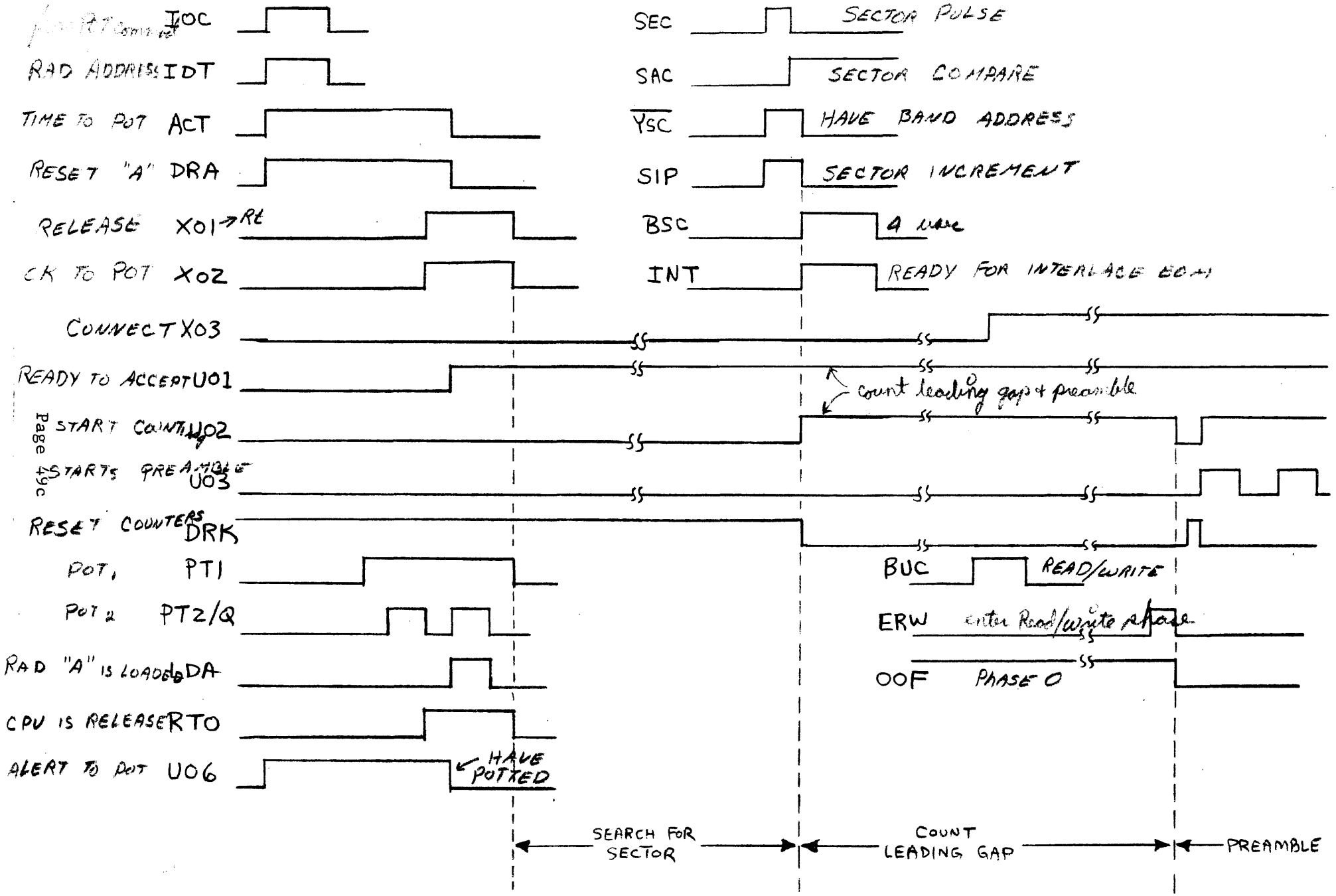


FIGURE 3-17 TIMING DIAGRAM PHASE ZERO

1 2 3
00, 01, 10, 00, etc

Operation of the Counters

This counter is actually made up of two separate counters. One is a two stage modulo 3 counter, that steps through 3 distinct counts. The other is a normal seven bit binary counter with 128 different configurations. Every third state of the modulo 3 counter steps the character counter portion by one. The character counter is re-clocked at about the middle position, K04.

Page 18 in Prints

$$sM02 = \overline{M01}\ CNT\ \overline{M02}$$
$$rM02 = CNT\ M02$$
$$sM01 = M02\ CNT\ \overline{M01}$$
$$rM01 = CNT\ M01$$

CNT = CLK U02

00M = $\overline{M01}\ \overline{M02}$

02M = M01

$$sK07 = \overline{(01F\ U01\ K06)}\ M01\ \overline{K07}$$
$$rK07 = M01\ K07$$

Page 19 + 20 in Prints

$$sK06 = K07\ \overline{K06}$$
$$rK06 = U01\ 01F\ M01 + K07$$
$$sK05 = \overline{(01F\ U01\ K06)}\ K06$$
$$rK05 = K06$$
$$tK04 = K05\ K06\ LSC\ CNT$$
$$tK03 = K04$$
$$tK02 = K03$$
$$tK01 = K02$$

Page 18 where

LSC = M01 K07 (every 6th count) 24 BITS

The term CNT is a gated clock pulse to the counters. It is only enabled during leading gap, preamble, data and postamble time.

The counters are reset by the logic term DRK. The timing relationships of these counter stages can be seen in Fig. 3-18.

Two amplified outputs of the modulo 3 counter are provided. These are count 0 and count 2.

Count 0 = 00M = $\overline{M01}\ \overline{M02}$

Count 1 = M02

Count 2 = 02M = M01

The logic term NXL signifies the last two counts of the character counter portion.

NXL = K01 K02 K03 K04 K05 K06

Page 98 equation

Leading Gap

Once the proper sector has been located it is then necessary to count the 13 clock pulses which define the leading gap. This is done with the M and K counters. These counters are initially reset by $\overline{DRK}$.

$$zK02 - K07 = \overline{DRK} \quad \text{dc reset}$$

$$zM01 - M02 = \overline{DRK}$$

where $DRK = 00F\ \overline{U02} + ...$

The K01 flip flop is also reset by $\overline{DRK}$, but it is accomplished in a different way. $\overline{DRK}$ is tied to true output of K01 (through a buffer amplifier) and when $\overline{DRK}$ goes to OV it resets the flip flop by pulling its true output down to ground. The counter will start to count the clock pulses (CNT) as soon as these are enabled by U02.

$$CNT = CLK\ U02 + ...$$

At the third clock pulse to occur in the leading gap the dc flip flop U05 is set. U05 is the Read Enable signal which is used in the Selection Unit to enable the input gates to the read amplifiers 3.6 to 4.8 usec. After the last possible address change.

$$sU05 = 00F\ U02\ K07\ 00M$$ READ ENABLE

$$REN = 00F\ U05$$

The counting of the leading gap proceeds for 13 clock counts to generate a 15.6 usec. delay period. This delay period is used to insure stabilization of the read amps and the head selection matrix and to allow time to program the required instructions before the data read/write time.

If the BUC wasn't previously issued, it must be done during the leading gap time. When the coupler becomes connected to the I/O channel the X03 flip flop is set and the error flip flop is reset.

$$sX03 = 00F\ BUC\ DMA\ \underline{CLK}$$

where $DMA = \overline{C17}\ C19\ \overline{C20}\ C21\ C22\ \overline{C23}$ ← load address on C lines

$$rE01 = 00F\ DMA\ \underline{BUC}$$

On the 13th count, U02 is reset thus stopping the count and ending the leading gap.

$$rU02 = 00F\ K05\ \underline{CLK}$$

At this time the coupler enters the read or write phase if the buffer is ready (X03 set), and the channel has the RAD address in W10-W14. W9 is used to control the phase counter as we leave Ø0.

sF01 = ERW DMW $\overline{\text{W90}}$ CLK (Read)

sF02 = ERW DMW W90 CLK (Write)

where DMW = W10 $\overline{\text{W11}}$ W12 W13 $\overline{\text{W14}}$ ← RAD ADDRESS on W lines

ERW = 00F K05 X03 (13th count)

If the operation is a write, the read enable flip flop, which was set on the 3rd clock of the leading gap, is reset as the coupler exits phase zero.

rU05 = ERW DMW $\overline{\text{W90}}$ CLK

If for some reason the channel is disconnected ($\overline{\text{DMW}}$) from the RAD at any time except during the leading gap or preamble, the coupler connected flip flop is reset.

rX03 = $\overline{\text{DMW}}$ $\overline{\text{U01}}$ CLK + ...

The flip flops U02, U03, U04 and U05 are initialized at the end of the leading gap, for their roles in the ensuing read or write phase.

Figure 3-18 shows the timing relationships between the various signals used during the leading gap time.

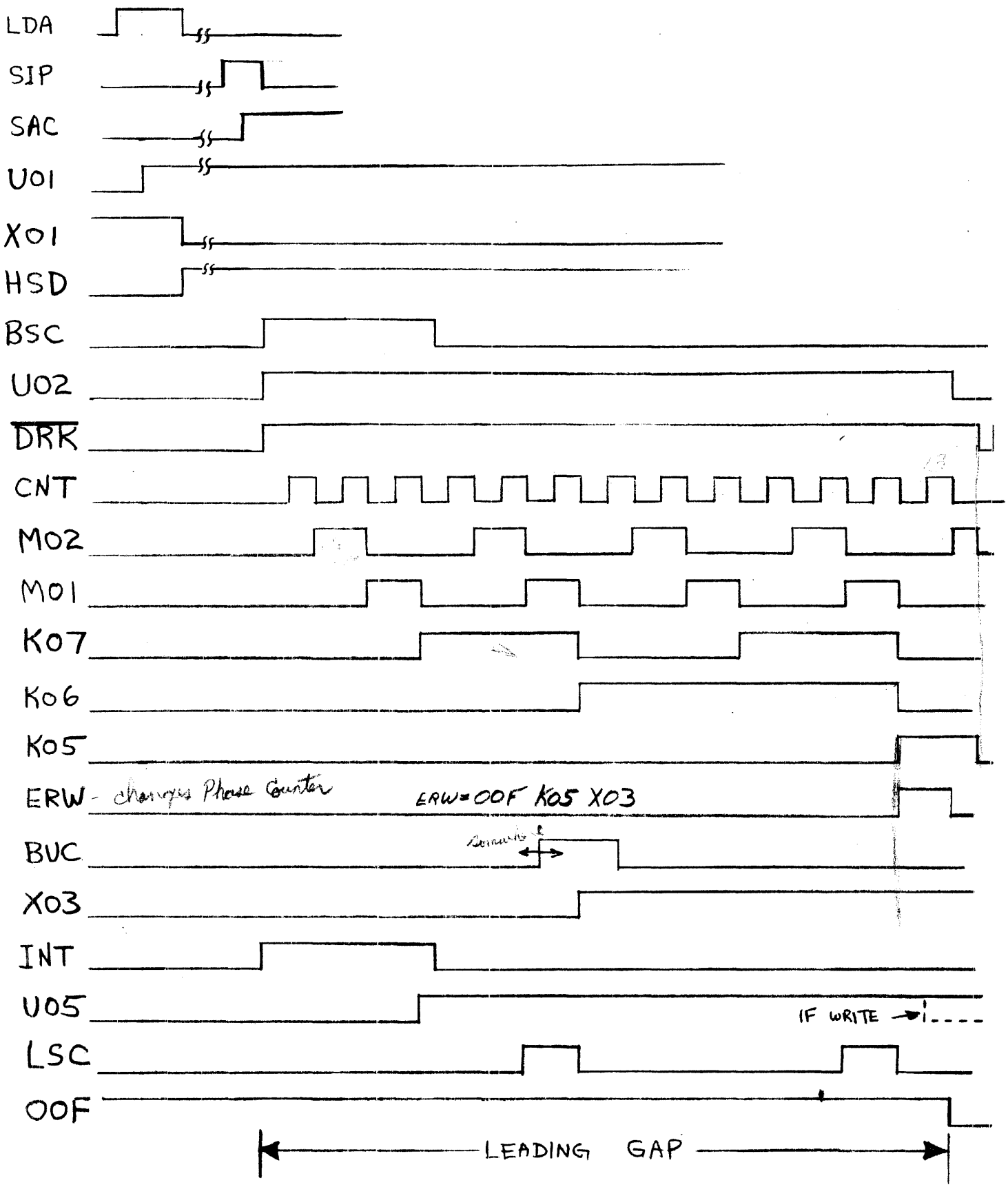


FIGURE 3-18 COUNT LEADING GAP

Phase 1 Write

Phase one is defined by:

$$01F = \overline{F01}\ F02$$

This phase begins at the 13th clock count (15.6 us) after SIP and lasts for a period of 406 clock pulses. (487 usec). However, if the band address selected is write protected, this phase lasts only one clock period during which the error flip flop, E01, is set and the connected flip flop, X03, is reset.

$$sE01 = 01F\ WLK\ \underline{CLK} + \ldots\ldots$$

$$rX03 = 01F\ WLK\ \underline{CLK} + \ldots\ldots$$

$$rF02 = 01F\ WLK\ \underline{CLK} + \ldots\ldots$$

$$rU01 = 01F\ WLK\ \underline{CLK}$$

where WLK is a signal from the selection unit that the band addressed is also protected by the switches.

Write Preamble

A ten bit preamble, 0101010100, is written on each of the four tracks in parallel. The data bits are sent to the selection unit on four lines, WD1-4. It is mixed with the clock signals WCA and WCK, and sets the Write flip flops WDE1-4. It is then amplified and sent to the proper heads. See Figure 3-6.

$$sWDE1 = \overline{WDE1}\ \underline{WCA}\ (WCK + \overline{WCK}\ WD1)$$

$$rWDE1 = WDE1\ \underline{WCA}\ (WCK + \overline{WCK}\ \overline{WD1})$$

$$WD1 = U01\ U03\ 01F + \ldots$$

$$U03 = 01F\ U01\ PNC\ \underline{CLK}$$

$$PNC = \overline{\overline{00M}\ K06}$$

means same condition is on both sides so it will toggle

it inhibits changing U03 at last 2 clocks

when we leave PNC, U03 is off so we get the last 2 i.e.,

Figure 3-19 shows a more detailed data flow and clock generations. The flip flop U03 as toggled with every other count thus generating the pattern used for the preamble. The first clock after entering phase one sets the flip flop U02 which enables the counter (CNT).

$$sU02 = 01F\ U01\ \overline{WLK}\ \underline{CLK}$$

$$CNT = U02\ CLK + 01F\ \overline{U01}\ CLK$$

At the end of the preamble U01 is reset by the counter.

$$rU01 = 01F\ WPC\ \underline{CLK}$$

where $WPC = U01\ K06\ M01$

WPC is true during a count of 9 but since the counter didn't start counting until the second clock pulse in the preamble, because U02 was reset, the preamble is 10 bits in length.

Also at the end of the preamble the counter must be returned to zero so it can then be used to count the 128 characters of data to be written. This is accomplished by inhibiting the setting of K07 and K05 at the end of the preamble by JK57 being false.

$$sK07 = \underline{M01}\ JK57$$

$$sK05 = \underline{K06}\ JK57$$

$$JK57 = \overline{01F\ K06\ U01}$$

Request of Data Characters

At the first clock pulse after the preamble the first four data bits are written. Therefore during the preamble they were requested from the CPU and shifted through the appropriate registers in time to be transferred to the write flip flops.

$$WD1 - 4 = 01F\ 23U\ S01\text{-}4$$

where $23U = \overline{U01\ U02}$ (data time)

U01	U02	
1	1	→ Preamble + leading gap (-1 clk)
0	1	→ Data time
0	0	→ Postamble + Gap
1	0	→ search for sector - after load A

9367 C SELECTION UNIT

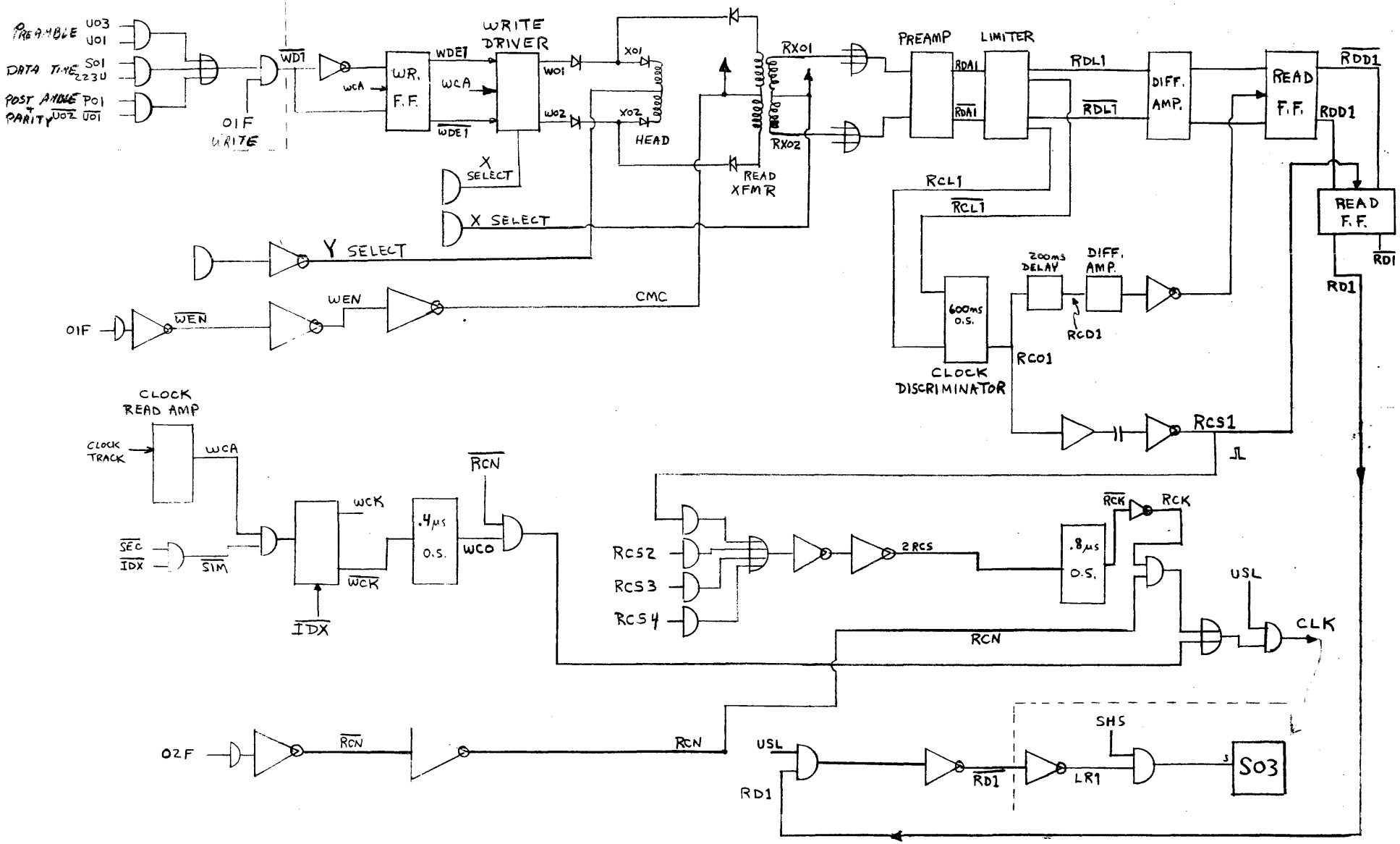


FIGURE 3-19 DATA AND CLOCK SIGNALS

LS

Figure 3-20 is a timing diagram showing all the important signals used during the write preamble and write data time. The first data character is requested from the CPU by setting X08 as phase one is entered.

$$sX08 = ERW\ DMW\ W90\ \underline{CLK}$$

The Z and V registers are 12 bit buffer registers used to hold data for up to 2 memory cycles during the asynchronous slip between the memory computer cycle and the character data rate to the RAD. If the V register can accept a character from the channel as specified by X08 being true, the ECW signal is generated.

$$ECW = 01F\ X08\ \overline{W50}\ \overline{W60}\ X03$$

W50 (W5) and W60 (W6) are included to permit transfer of data at near maximum rate. (286K char/sec). X03 stops data requests if a partial sector is called for in the interlace count register and the interlace count goes to zero, thus disconnecting both the channel and the disc.

$$rX03 = \overline{U01}\ \overline{DMW}\ \underline{CLK} + ...$$

At the leading edge of the first clock after W60 is set in response to the ECW, the R lines ready flip flop, X06 is set and the V empty flip flop, X08, is reset at the falling edge of the same clock, becuase the data was transferred into V at that time. X06 is reset on the leading edge of the next clock.

$$sX06 = 01F\ W56\ \overline{\underline{CLK}}$$

$$rX08 = 01F\ X06\ \underline{CLK}$$

$$rX06 = 01F\ \overline{\underline{CLK}}$$

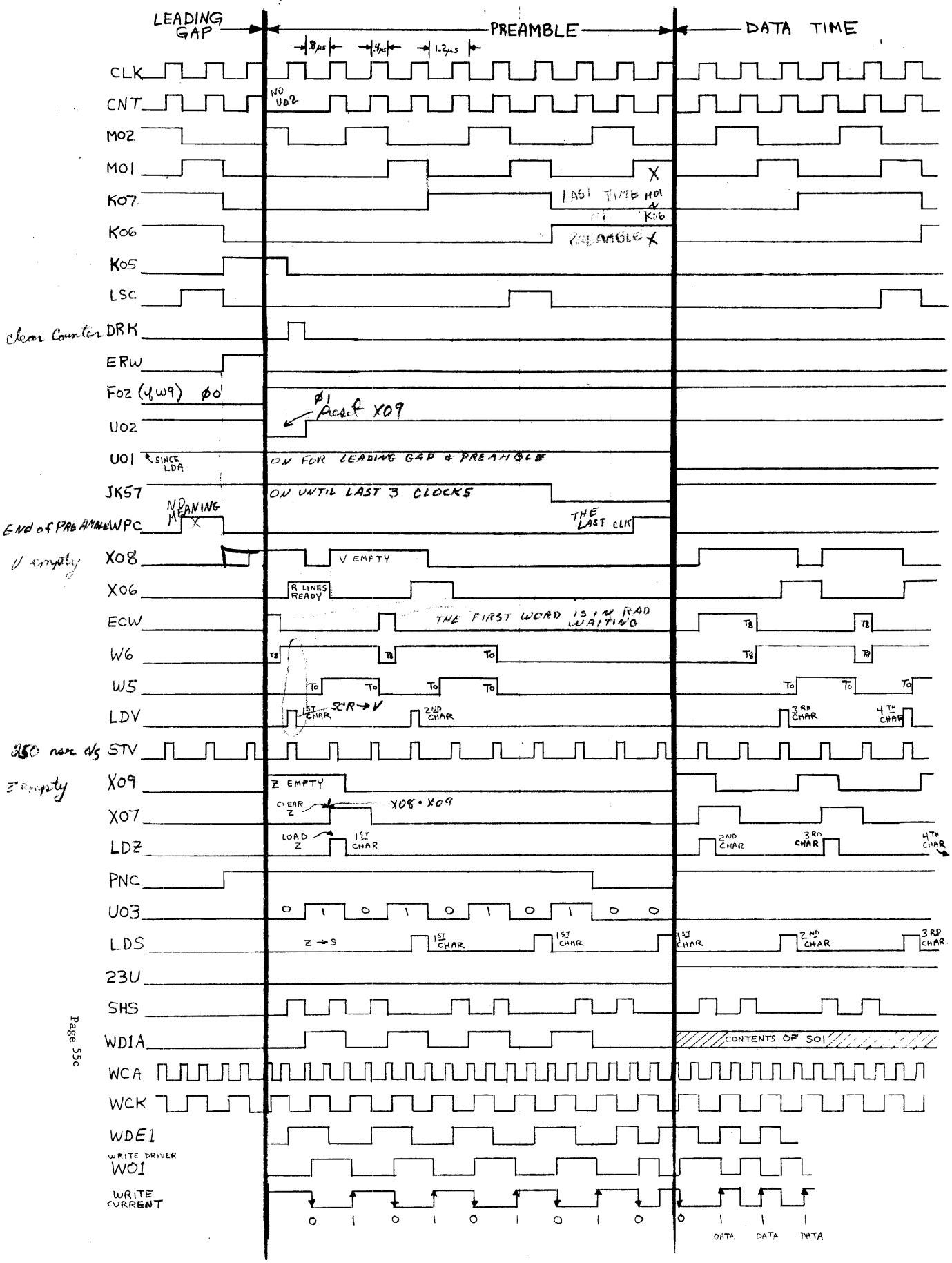


FIGURE 3-20 WRITE PREAMBLE AND DATA ACCESSING

To allow the data transfer by only the true R lines from the I/O channel, the V register is cleared before loading

$$zV1\text{-}12 = \overline{DRV}$$

$$DRV = W56\ \overline{X06}\ \overline{CLK}\ F02$$

where $W56 = \overline{W5}\ W6$

then $sV01 = LDV\ R01$

$\vdots \quad \vdots \quad \vdots$

$sV12 = LDV\ R12$

Where $LDV = 01F\ X03\ X06\ W\ 0\ STV\ CLK$

and STV is a 250ns strobe pulse initiated $\overline{CLK}$

On the next clock leading edge after X08 is reset, that X09 is also true (indicating that Z register is clear), X07 is set and the contents of V are transferred to Z; and also on the leading edge of the same clock pulse, X08 is set again indicating that V is now clear and ready to receive another character from the I/O channel. LDZ is the logic term that enables the data transfer from V to Z.

$$sX07 = 01F\ X09\ \overline{X08}\ \overline{CLK}$$

$$sX08 = 01F\ \overline{U04}\ X09\ \overline{CLK}$$

Again to transfer the data using only the true lines the Z register must first be cleared.

$$zZ1\text{-}12 = \overline{DRZ}$$

where $DRZ = 01F\ \overline{X08}\ X09\ \overline{CLK}$

the data then is set into the Z register

$sZ01 - V01\ LDZ$

$\vdots \quad \vdots \quad \vdots$

$sZ12 = V12\ LDZ$

Where $LDZ = 01F\ X07\ CLK$

On the next clock leading edge X07 is reset

$$rX07 = \overline{CLK}$$

Since the Z register now contains data the Z empty flip flop X09 is now reset. (It was initially set at the beginning of the preamble).

$$yX09 = \overline{U02}\ U01$$

$$rX09 = 01F\ X07\ U01\ \overline{CLK}$$

Although during other than the preamble time ($\overline{U01}$) the Z may transfer its data to the S register at the same time at V to Z transfer takes place. In this case X09 would not reset. This is the reason for the different gating during data write time.

$$rX09 = 01F\ X07\ \overline{M01}\ \overline{CLK}$$

This double transfer can only occur at the clock which occurs when the counter is in its 02M configuration. The Z to S transfer always occurs at this time.

s S01 = LDS Z01 CLK

r S01 = LDS $\overline{\text{Z01}}$ CLK

Similarly for S04, S07 and S10

sS02 = LDS Z02

Similarly for S03, S05, S06, S08, S09, S11 and S12

where LDS = 01F 02M CLK

During most of the preamble X09 is reset because the first 12 bit character of data is held in the Z register. At the last clock of the preamble this character is transferred to the S register and then X09 is set.

sX09 = 01F WPC CLK

where WPC= U01 K06 M01 (end of preamble)

During the data transfer time, X09 also sets each time a character is transferred into the S register.

sX09 = 01F M01 $\overline{\text{U01}}$ CLK

If the condition exists that a transfer from R to V has not occurred, as shown by X08 being true, at the time that a transfer from V to Z to S occurs (02M X09), a rate error condition exists and the channel error indicator is set.

sX04 = 01F X08 X09 02M $\overline{\text{U01}}$ $\overline{\text{CLK}}$

WES = X04 (V empty, Z empty, LDS)

The parity flip flops P01 through P04 are set during the preamble in preparation for the longitudinal parity generation.

y P01 - 4 = SPR

where SPR = 01F U01

WRITE DATA

Each clock time except 02M clock, the S register data is shifted one position in order to write the succeeding 4 bits on the disc.

sS01 = S02 SHS CLK

similarly for S04, S07, and S10

sS02 = S03, SHS

similarly for S03, S05, S06, S08, S09, S11 and S12

where SHS = 01F $\overline{\text{02M}}$ CLK

Since LR1-4 are false in the write phase, zeroes are shifted in S02,3,5,6,8,9, 11, and 12 during the shifting process and so these can be set by the direct set input

when transferring an new character into S.

384 bits of data are written on each of the four tracks during phase one.

WD1 = S01 23U

WD2 = S04 23U

WD3 = S07 23U

WD 4 = S10 23U

where 23U = $\overline{U01}$ U02 (data time)

The termination is accomplished by setting U04 at the clock time prior to the next to last Z to S transfer and inhibiting further setting of X08

sU04 = 01F NNL K07 02M CLK

where NNL = K01 K02 K03 K04 K05

LONGITUDINAL PARITY GENERATION

At the end of the write preamble time the four parity flip flops are all set to their true state.. These flip flops, P01-P04 are used for generating the longitudinal parity bits written at the end of the data time, and they are also used for checking parity on a read operation.

y P01 - P04 = SPR

where SPR = 01F U01 + ...

During phase one data time each of these P flip flops is toggled with the data bits being written on that particular track. P01 corresponds to track one etc.

t P01 = 01F WD1 CLK

t P02 = 01F WD2 CLK

t P03 = 01F WD3 CLK

t P04 = 01F WD4 CLK

When the writing of the data is completed, U02 is reset.

r U02 = 01F NXL LSC CLK

where LSC = M01 K07 (every 6th count)

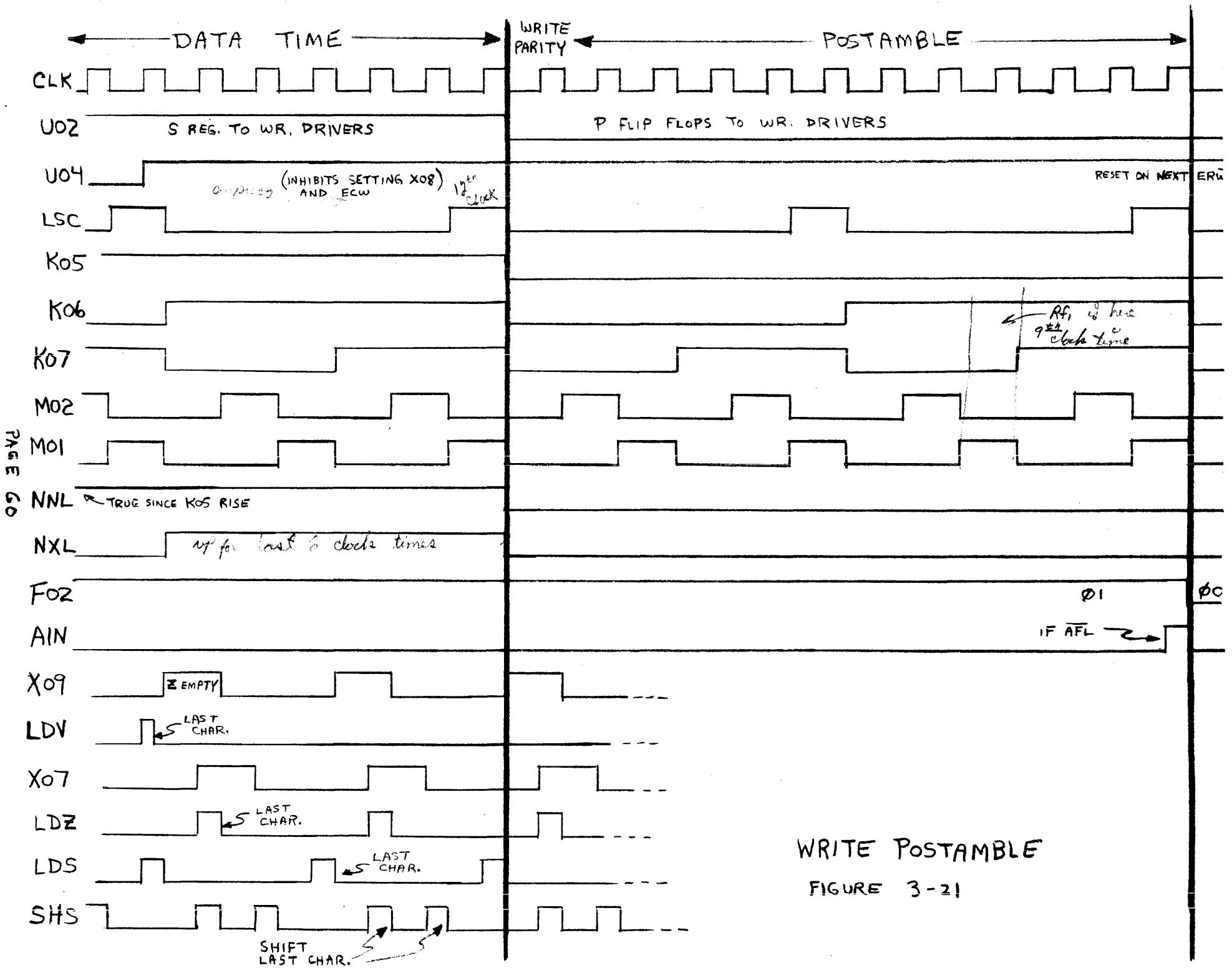
NXL = K01 K02 K03 K04 K05 K06 (last word time of sector)

WRITE PARITY AND POSTAMBLE

A longitudinal parity bit and 11 additional zeros comprise the 12 bit per track postamble. The additional 11 zeros written are used to insure proper read back for the final data and parity bits when in phase two. It is not desirable to shut off the read amplifiers immediately with the final bit. The parity bits are written by gating the contents of the P flip flops into the write circuits.

$$WD1 = 01U\ P01 + \ldots.$$
$$WD2 = 01U\ P02 + \ldots.$$
$$WD3 = 01U\ P03 + \ldots.$$
$$WD4 = 01U\ P04 + \ldots.$$
$$\text{where } 01U = \overline{U01}\ \overline{U02}$$

As the parity is written WD1-4 signals again toggle the parity flip flops as previously described, thus resetting any that were on. The WD gates above then will be all false thus writing zeroes in each track until the coupler goes to phase zero after the counter has counted 11 of these postamble zero bits. See figure 3-21.



WRITE POSTAMBLE

FIGURE 3-21

Now the address register is checked for an overflow condition. If the A register contains all ones in bits 12 through 23, U03 is set, and an error is indicated in phase zero if the buffer is not disconnected by SIP time.

s U03 = 01F $\overline{\text{U02}}$ LSC AFL CLK

where AFL = A12 A13 A14 .....A23

If the A register is not full (band 77 sector 77) at the beginning of the postamble it will then be incremented by one at the time that the eleventh postamble zero is sent to the write circuits.

AIN = 01F $\overline{\text{U01}}$ $\overline{\text{U02}}$ LSC K06 $\overline{\text{AFL}}$ CLK

tA23 = A1N

tA22 = A23

tA18 = A19

tA17 = AFC AIN

tA16 = A17

tA15 = A16

tA14 = A15

tA13 = AFB AFC AIN

tA12 = A13

tA09 = A10

where AFB = A14 A15 A16 A17

AFC = A18 A19 A20 A21 A22 A23 $\overline{\text{X05}}$

This concludes the write phase and the coupler returns to phase zero at the end of the postamble.

rF02 = 01F $\overline{\text{U02}}$ LSC K06 CLK

When writing is is necessary to disable the Z lines to the I/O channel. This is done by disabling the cable drivers with $\overline{\text{F01}}$. The enable term is a 0 volttrue logic. The Z lines therefore are only active during the read phase (Ø2).

Another term X12 is generated in the coupler and sent to the I/O Channel. This signifies to the channel that the RAD is using the 12 bit extended single character register.

X12 = DMW

SECTOR GAP FOLLOWING A READ/WRITE OPERATION

At the end of each sector read or write, the coupler returns to phase zero in both single and multisector operation, and if appropriate, re-enters the read or write phase by the same procedure as previously described in the initiate Read or Write operation. The only difference is that the triggering of BSC will be gated by HSD of a different origin. If the previous sector written was not aborted by an attempt to write in a protected disc area, or an attempt was made to increment the A register across a unit boundary, HSD will be true.

$$HSD = X03\ \overline{U03} + \ldots$$

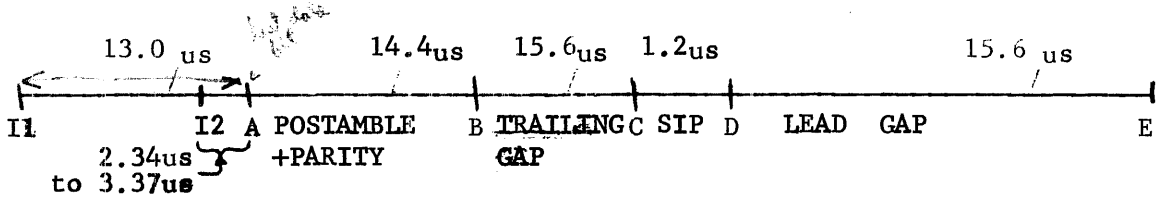
says we haven't gone pass last address

At the following SIP, BSC is triggerred in the same manner as in the initial gap. The conclusion of data transfer is sensed by the disconnection of the device by the channel at the end of the interlace count.

$$r\ X03 = \overline{DMW}\ \overline{U01}\ \underline{CLK}$$

With X03 reset and the coupler in phase zero or postamble time, the coupler is ready and can receive another EOM, Alert to POT.

The following chart shows the incidence of various timing signals occurring at the end of a write operation.



The I1 interrupt occurs at the time the last word is transferred from memory to the channel buffer register, due to the fact that the interlace count reached zero. I1 will not occur if the channel disconnects the device prior to the interlace count equal to zero, due to a Whs signal sent to the channel by the coupler.

The following conditions cause the end if record signal Whs, to be sent to the I/O channel.

1. An attempt was made to increment accross a unit address boundary
2. An attempt was made to write in a write protected area

At point A on the chart, 13 u sec. after I1, the last data bit is recorded on the recording medium and the coupler becomes ready. From point A to point B, the parity bit and eleven postamble bits (zeroes) are recorded. At B the coupler enters phase zero, and responds to any POT that is pending. A POT must occur within 15 u sec. if it is to find sector equivalence with the value that the D register will

attain when it is incremented at SIP time in this particular gap. This is point C on the chart. 2 u sec. later, at point D, the sector pulse SIP trailing edge occurs and the coupler tests for equality between the A register sector and the sector counter of the addressed selection unit. At point E, 15.6 u sec. later, the coupler enters the read or write phase.

If the EOM (BUC) instruction is the last of the RAD instructions to be programmed in the gap, it must be executed by E time or an entire device revolution will be lost. (ERW will not occur because X03 is false)

BAND NON-INCREMENT MODE

This mode of operation is indicated by X05 being set. In this mode, address incrementation is limited to the sector portion only. Thus a full band transfer can be programmed with minimum instructions in the gap at sector 0, if the transfer starts at an arbitrary sector. In this mode, triggering of BSC is gated by HSD of a different source.

$$HSD = \overline{U01}\ X05\ \overline{E01}$$

That is, the qualification that an EOM POT sequence must occur before an operation can occur, is waived for the non-increment mode.

ERROR PROCESSING

The following errors cause a coupler error by setting flip flop E01.

A. Write Error:
When an attempt is made to write on a write-protected band, a write error results. The coupler enters the write phase for one clock period during which E01 is set, X03 is reset, and the coupler returns to phase zero.

B. Address overflow error:
At the end of any sector read or write, if the address bits A12-A23 are all ones, the address incrementation (AIN) is inhibited. The coupler returns to phase zero with U03 set if the coupler is not in the band non-increment mode. If U03 is set an address overflow results if a new address has not been potted by the time the next SIP appears.

s E01 = 00F U03 SIP (read)

r U03 = RF1 $\overline{\text{AFL}}$ CLK

where RFI = Last character read

s U03 = 01F $\overline{\text{U02}}$ LSC AFL CLK (write)

and AFL = A12 A13 .... A23 $\overline{\text{X05}}$

C. POT error:

A POT issued at other than idle or postamble will also indicate an error, regardless of whether a read or write operation is taking place. Even under these conditions the address POT is responded to by sending an RTO signal to the computer, but the contents of the A register are not changed.

yE01 = X01 $\overline{\text{X02}}$ PT2

In the first two error types, the operation is terminated before the interlace count is zero. Therefore I1 will not occur but I2 will, because Whs is sent to the channel based on X03 being false or U03 being true at SIP time.

WHS = 00F ($\overline{\text{X03}}$ $\overline{\text{BUC}}$ + U03 SIP) DMW

Flip Flop U03 will be reset when the buffer is disconnected.

r U03 = 00F $\overline{\text{X03}}$ CLK

The following error cause a channel error to be indicated by sending the WES signal to the I/O channel.

A. Read Error: will keep reading until WC=0

When reading the longitudinal parity bits the parity mismatch signal $\overline{\text{PCP}}$ will cause WES to be true.

WES= 02F $\overline{\text{U01}}$ $\overline{\text{U02}}$ 00M $\overline{\text{K06}}$ $\overline{\text{K07}}$ $\overline{\text{PCP}}$ CLK

B. Rate Error:

If during the transfer of the data in a read or write operation, characters are missed due to infering time shares or the data rate, the error signal WES will be sent immediately and a Whs will be sent at the end of the sector.

WES = X04

where X04= 02F PST $\overline{\text{X09}}$ $\overline{\text{U01}}$ 00M DMW CLK + 01F X08 X09 02M $\overline{\text{U01}}$ CLK

Whs =00F DMW $\overline{\text{BUC}}$ $\overline{\text{X03}}$

and r X03=00F X04 CLK

In the case of the read error, the operation is allowed to continue until the interlace counts is zero, Thus I1 is always generated. In the case of the rate error

I2 is always generated at the next gap after the error occurred.

The flip flop X03 is reset by detecting that W10 through W14 no longer contain the RAD address, 26.

PHASE TWO-READ

Phase two is defined by

$$02F = F01\ \overline{F02}$$

The read phase begins at the 13th clock count (15.6 us) after SIP and lasts until the last character is accepted from the coupler. The clock used in this phase is derived from the data by the read decoder module. The four clocks (one from each track) are "ored" together at the input to the one shot RCK which generates clock pulses of .5 usec width. The switching from the write clock, used in phase 0, to the read clock in phase two, is done in each Selection unit under control of RCN, which is generated in the coupler.

$$RCN = 02F$$

The count registers K02 through K07, and M01 and M02 are reset by $\overline{DRK}$ at two places during the preamble. One is at the beginning of the read phase, until the first clock is detected and the other occurs after six clocks are counted, until the first double zero is detected.

$$DRK = \overline{CLK}\ U01\ \overline{U02}$$

The clock pulses are counted in the count register by the CNT pulses.

$$CNT = U02\ CLK + 02F\ \overline{U01}\ CLK$$

Once the read phase is entered, a complete sector will be read and the longitudinal parity will be checked even though the buffer may disconnect earlier after reading only a part of the sector.

The read phase will be described in three parts in the order of their occurrence. The detection of the preamble, reading of data and transfer of characters, and checking of longitudinal parity.

DETECTION OF PREAMBLE

The first clock detected after entering the read phase sets U02.

$$sU02 = 02F\ U01\ \overline{U03}\ OOM\ \underline{CLK}$$

where U01 was set in Ø 0 by the LDA

$$OOM = \overline{M01}\ \overline{M02}$$

Six clock times later, U02 is reset and U03 is set and the search for the preamble double zero begins.

$$rU02 = 02F\ U01\ 02M\ K07\ \underline{CLK}$$

$$sU03 = 02F\ U01\ U02\ 02M\ K07\ \underline{CLK}$$

Flip flop U02 is set again when the first zero read is in S03 and the second

to check for 2 zeros, we check only 1 track

zero is in RD1. On the basis that U03 is set (search for end of preamble) and U02 is set (found end of preamble), U01 and U03 are reset on the next clock.

sU02 = 02F U01 U03 $\overline{S03}$ $\overline{RD1}$ CLK → 2 zeros are found

rU01 = 02F U02 U03 CLK

rU03 = 02F U01 U02 OOM CLK

The parity flip flop P01 through P04 are set prior to reading data so that the longitudinal parity may be checked at the end of the data read time.

yP01 =SPR

yP04= SPR

where SPR = 02F U01 $\overline{U02}$

READ DATA Figure 3-22 shows the timing relationships used in reading the preamble and data, and also how the character is transferred to the Input/Output Channel. Each track will read 384 bits of data which will set into the S register and be shifted twice. Then it will then contain one 12 bit character.

sS03 = LR1 CLK

rS03 = $\overline{LR1}$ CLK

sS06 = LR2 CLK

rS06 = $\overline{LR2}$ CLK

sS09 = LR3 CLK

rS09 = $\overline{LR3}$ CLK

sS12 = LR4 CLK

rS12 = $\overline{LR4}$ CLK

Where LR1-4 is the output of the read circuits gated by 02F.

P01 through P04 are toggled whenever a one is read in from the corresponding track.

tP01 = LR1 U02 CLK

tP02 = LR2 U02 CLK

tP03 = LR3 U02 CLK

tP04 = LR4 U02 CLK

Two 12 bit buffer registers are supplied to provide the buffering required to operate with the 92 computer as well as with the 930,940 and 9300 computers. These two buffer registers also allow sufficient time for lower priority time share operations to occur when using a TMCC. These two registers are called the Z and V registers. At each OOM clock, a 12bit character is transferred from the S register to the Z register. DC flip flops are used in the Z register and the information is thus transferred at the beginning of the clock pulse, CLK.

$$sZ01 = LRC\ S01$$
$$rZ01 = LRC\ \overline{S01}$$
$$\vdots \quad \vdots \quad \vdots$$
$$sZ12 = LRC\ S12$$
$$r\,Z12 = LRC\ \overline{S12}$$

where LRC is the term which allows this transfer

$$LRC = 02F\ OOM\ CLK$$

The X09 flip flop is used to record the fact that the Z register is full by being reset every OOM time during the data transfer portion of a sector.

$$rX09 = OOM\ \overline{U01}\ 02F\ \underline{CLK}$$

The transfer of data from the Z register to the V register occurs under control of the X07 flip flop in every case except when the response to the ECW (signified by flip flop X06) is so late that X08 flip flop must be used on the other clock phase as described later in this section.

$$sV01 = LVR\ Z01$$
$$rV01 = LVR\ \overline{Z01}$$
$$\vdots \quad \vdots \quad \vdots$$
$$sV12 = LVR\ Z12$$
$$rV12 = LVR\ \overline{Z12}$$

Where LVR enables this transfer

$$LVR = 02F\ X07\ \overline{X08}\ CLK + \ldots$$

Except at the beginning (IS NEXT PAGE, CIRCLE AREA) the sequence of events is initiated by the first clock, CLK, to occur during $\overline{W5}$ W6 time, which indicates that the previous information on the Zw lines (from to V-register to the I/O channel) has been accepted by the I/O channel. Thus X06 is set to indicate this condition.

$$sX06 = 02F\ \overline{W5}\ W6\ U04\ \underline{\overline{CLK}}$$

On the next clock leading edge the X07 flip flop is set if the data presently in the V register had not arrived directly from S (as indicated by X09 being reset) or if it had, it would be at some clock time other than 02M.

$$sX07 = 02F\ X06\ \overline{X09}\ \underline{\overline{CLK}}$$ (Z to V)

$$sX07 = 02F\ X06\ \overline{M01}\ \underline{\overline{CLK}}$$ (S to Z to V)

If the clock time is 02M and X09 is set, V should not be loaded, for the same character would be transferred twice to the I/O channel. The character is then

allowed to be sent to the V register only while X07 is true. On the following clock leading edge X07 is reset.

rX07 = $\overline{CLK}$

The same terms which set X07 also reset X06 if not in the preamble and if the terminati flip Flop U03 has not been set.

rX06 = 02F $\overline{U03}$ $\overline{U01}$ $\overline{CLK}$ ($\overline{M01}$ + $\overline{X09}$)

The ECW clocks to the channel are based on $\overline{X06}$, which indicates that the previous character has been accepted by the I/O channel. The I/O channel terms $\overline{W5}$ and $\overline{W6}$ are included in the ECW logic to allow data transfer rates close to the maximum of 286K bytes/sec.

ECW = 02F U04 $\overline{W5}$ $\overline{W6}$ DMW ($\overline{X06}$ + $\overline{U03}$ $\overline{X09}$)

U04 is included for initialization as described later.

If an interfering time share operation occurs at a time that the I/O channel wants to access memory, the process will be delayed and W5 will stay on for an extra memory cycle ($\overline{W6}$ W5 $\overline{W4}$) and the channel cannot accept another character. In this case, X07 will not become true at OOM clock time and the character transferred from S to Z will not be transferred to V until a later clock. In the case of a second interfering time share, the transfer to V must take place later than the second clock past OOM, but before OOM CLK, in order to prevent the transfer of the next character into Z. This case, which is defined by X08 being true, is clocked differently.

LVR = 02F X08 OOM $\overline{CLK}$

If the X07 is not set on the leading edge of the clock in 02M, X08 is used to transfer the data, if it becomes available before the fall of CLK in 02M. This only occurs with interfering time shares by another device on another I/O channel operation simultaneously.

sX08 = 02F $\overline{X09}$ 02M X06 $\underline{CLK}$

It is reset at the following clock leading edge.

rX08= 02F $\overline{CLK}$ 02M

A rate error is declared if the data is not transferred out of the Z register, as indicated by X09 still being reset by OOM CLK time.

sX04 = 02F $\overline{X09}$ $\overline{U01}$ OOM $\underline{CLK}$ DMW PST

Wes = X04

Flip flop X09 will be set when Z is transferred to [illegible] as determined by X07 or X08

sX09 = 02F X07 $\overline{CLK}$

+ 02F X08 $\overline{CLK}$

To initialize this sequence it is necessary to delay the sending of ECW clocks to to the I/O channel until the leading edge of the second OOM in the read data portion of Ø2 when the first 12 bit character has been read. This accomplished by having

U04 in the ECW logic and not setting U04 until the proper time.

$$sU04 = \overline{U01}\ OOM\ 02F$$

This initial setting of X06 should occur at the leading edge of CLK in the first 02M so that the first S to Z to V transfer occurs on the second OOM CLK to occur in the read data portion of Ø2.

$$sX06 = 02F\ 02M\ \overline{U01}\ \overline{U04}\ \underline{CLK}$$

Termination of the ECW pulses for a sector must occur on the 128th ECW. Flip flop U03 is set to indicate that X06 should not be reset after its setting for the 128th time.

$$sU03 = 02F\ \overline{U01}\ \overline{U02}\ X07\ \overline{X08}\ \underline{CLK}$$

The condition of $\overline{U01}\ \overline{U02}^{X07\ \overline{X08}}$ indicates the clock at which S is transferred to Z for the 128th time.

$$rU02 = 02F\ NXL\ LSC\ \underline{CLK}$$

where LSC = K07 M01 (every sixth count)

and NXL = K01 K02 K03 K04 K05 K06

In the case in which the next to last character is transferred to V in the first part of the same OOM that the last character is transferred from S to Z, there will be two ECW's required to transfer out all of the data. By including X07 $\overline{X08}$ in the set U03 equation, U03 does not get set until the last character is transferred to the V register.

LONGITUDINAL PARITY CHECK

The longitudinal parity bit which immediately follows the last data bit of the sector is compared against that which has been formed in the P flip flops while reading the Data. If they fail to compare, the error signal, WES, is generated.

$$WES = 02F\ \overline{U01}\ \overline{U02}\ OOM\ \overline{K06}\ \overline{K07}\ \overline{PCP}\ CLK$$

The time that the parity bits are ready is defined by U01 U02 OOM K06 K07. PCP is the gate in which the comparison is done.

$$\overline{PCP} = \overline{P01}\ LR1 + P01\ \overline{RD1}$$
$$+ \overline{P02}\ LR2 + P02\ \overline{RD2}$$
$$+ \overline{P03}\ LR3 + P03\ \overline{RD3}$$
$$+ \overline{P04}\ LR4 + P04\ \overline{RD4}$$

When the last character is accepted, if an address overflow condition does not exist (not band 77 sector 77), the address increment signal AIN is generated, which adds one to the address in the A register. It's generated if in the non-increment mode due to the X05 term in the AFL.

we do not spend as much time in the Postamble in Read as we do in Write (9) (12)

AIN = RF1 $\overline{\text{AFL}}$ CLK

The read phase ends when the last character is accepted by the I/O channel, and the coupler returns to phase 0.

rF01 = RF1 $\underline{\text{CLK}}$

where RF1 = 02F $\overline{\text{U01}}$ $\overline{\text{U02}}$ 02M K06

AFL = A12 A13 .... A23 $\overline{\text{X05}}$

The flip flop U03 is reset unless AFL is true in the non-increment mode.

rU03 = RF1 $\overline{\text{AFL}}$ $\underline{\text{CLK}}$

If U03 fails to reset, it will then be on at the time that the next SIP pulse occurs, thus indicating an address overflow error by setting E01.

sE01 = 00F U03 SIP

Flip flop U05, the read enable signal, is reset at the time the last character is accepted by the channel, in order to prevent any transtions into the read circuits at the time that the A register increments.

rU05 =RF1

Flip flop U04, which signifies the time for read ECW's, is also reset by RF1

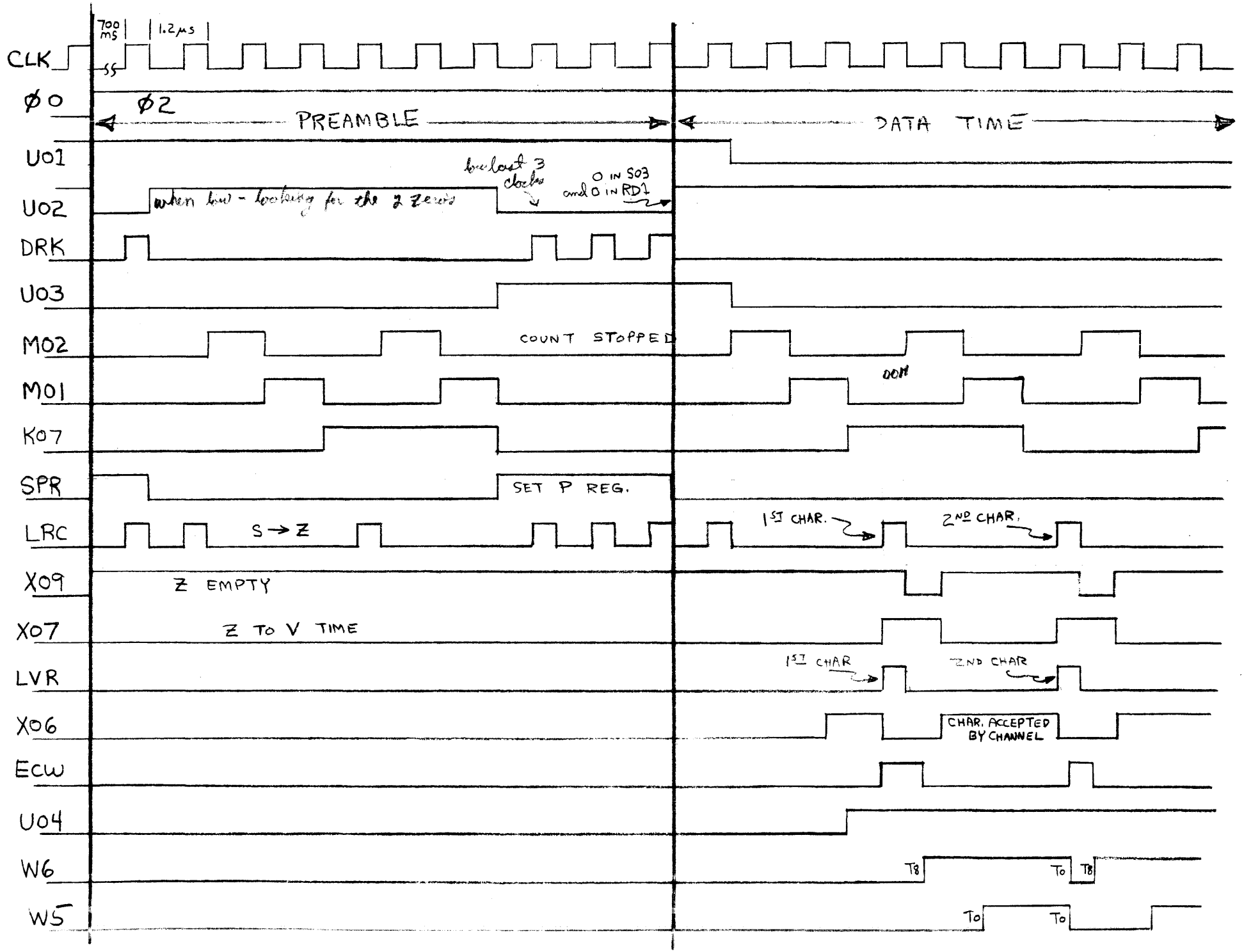


FIGURE 3-22 READ PREAMBLE AND DATA

X01 X02
0 0 → nothing
0 1 → alert to pin
1 0 → pot at bad time
1 1 → alert to POT

If a rate error has occured in phase one or two the flip flop X04 is in the set conditon. To prevent any further reading or writing beyond that sector in which the error occurred, the **connected** flip flop X03 is reset in the next Ø0 and the operation terminates.

rX03 = 00F X04 CLK

X04 is also reset at the same time

rX04 = 00F CLK

PIN OPERATIONS

A PIN instruction transfers the contents of the D register (current sector address) to the specified core memory location. The contents of D01-D06 are transferred to memory word bits 18 through 23 respectively by the computer C register C18-C23 See Figure 3-23, **Sector** Counter PIN Flow.

The PIN instruction does not affect the current **status** of the addressed selection unit or the coupler, and may be executed during any phase or operation of these units.

ALERT TO PIN

An EOM, Alert to PIN instruction must **preceed** the PIN Operation. This EOM alerts the coupler that a PIN is to follow by setting flip-flop X02 true.

sX02 = IDN

IDN = C16 IOC DMA

RTO = $\overline{X01}$ X02 $\overline{ENP}$ ← last sample clr D register

X02 will remain true until $\overline{Rti}$ from the computer signals that the PIN instruction has terminated.

rX02 = RTI +....

The Alert to PIN EOM instruction also selcts the addressed selection unit by setting the address code into the unit address regiser, G01-G02.

sG01 = IDN C12

rG01 = IDN $\overline{C12}$

sG02 = IDN C13

rG02 = IDN $\overline{C13}$

The outputs of G01 and G02 are gated to be used as cable drive inhibit terms in each of the selction units.

$GS1 = \overline{GO1}\ \overline{GO2}$ Selection Unit 1

$GS2 = \overline{GO1}\ GO2$ Selection Unit 2

$GS3 = GO1\ \overline{GO2}$ Selection Unit 3

$GS4 = GO1\ GO2$ Selection Unit 4

In each selection unit the GS address term unique to the unit becomes the term $\overline{PSL}$. See Figure 3-24, Unit Select for PIN Operations. The $\overline{PSL}$ term is precessed on the cable connector modules in the same way as they are for unit selection during read and write selection. See Figure 3-12, Unit Select for Read/Write Operations.

If the contents of the D register happened to be transferred into the buffer at the instant the register is counting up, an erroneous sector address could be obtained. To prevent this possiblity, the RTO signal will be delayed by the YSC flip flop to allow the D register to settle. The term $\overline{YSC}$ comes from the false output of the sector increment flip flop which is triggered by the sector pulse SEC. Normally the false output of YSC is low. When the sector pulse SEC appears, YSC goes to Ov for 1.2 microseconds which causes the signal $\overline{ENP}$ to delay $\overline{RTO}$.

$RTO = \overline{X01}\ X02\ \overline{ENP}$

$\overline{ENP} = YSC + \overline{PSL}$

$\overline{PSL} = GS1 + GS2 + GS3 + GS4$

If the Sector increment pulse is not present during a PIN operation, the YSC flip flop will be in its normally true state and $\overline{RTO}$ will not be delayed.

The current secotr address in the D register is transferred to the C register on lines Cd18-Cd23.

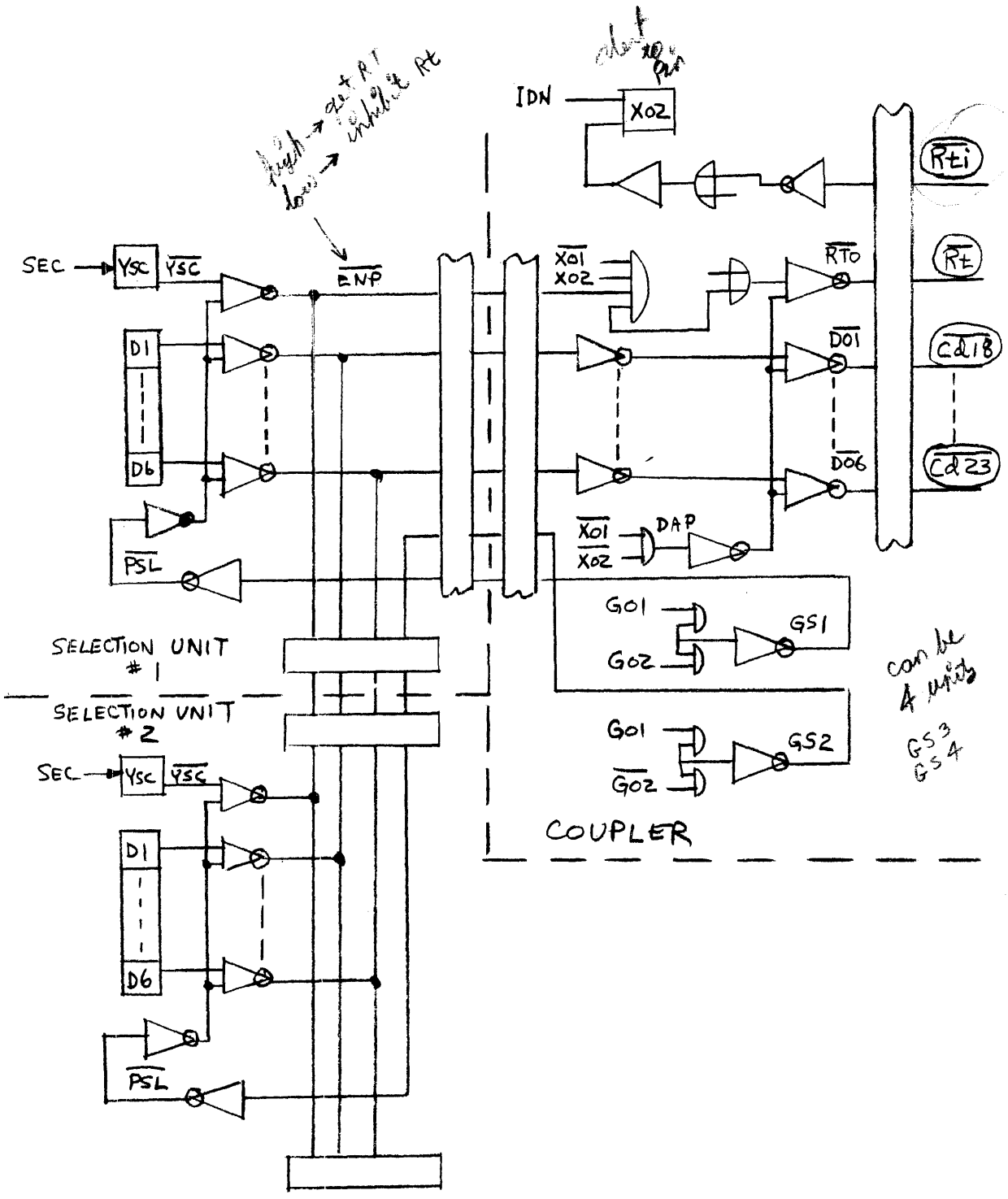


FIGURE 3-23 SECTOR COUNTER (D REGISTER) PIN FLOW DIAGRAM

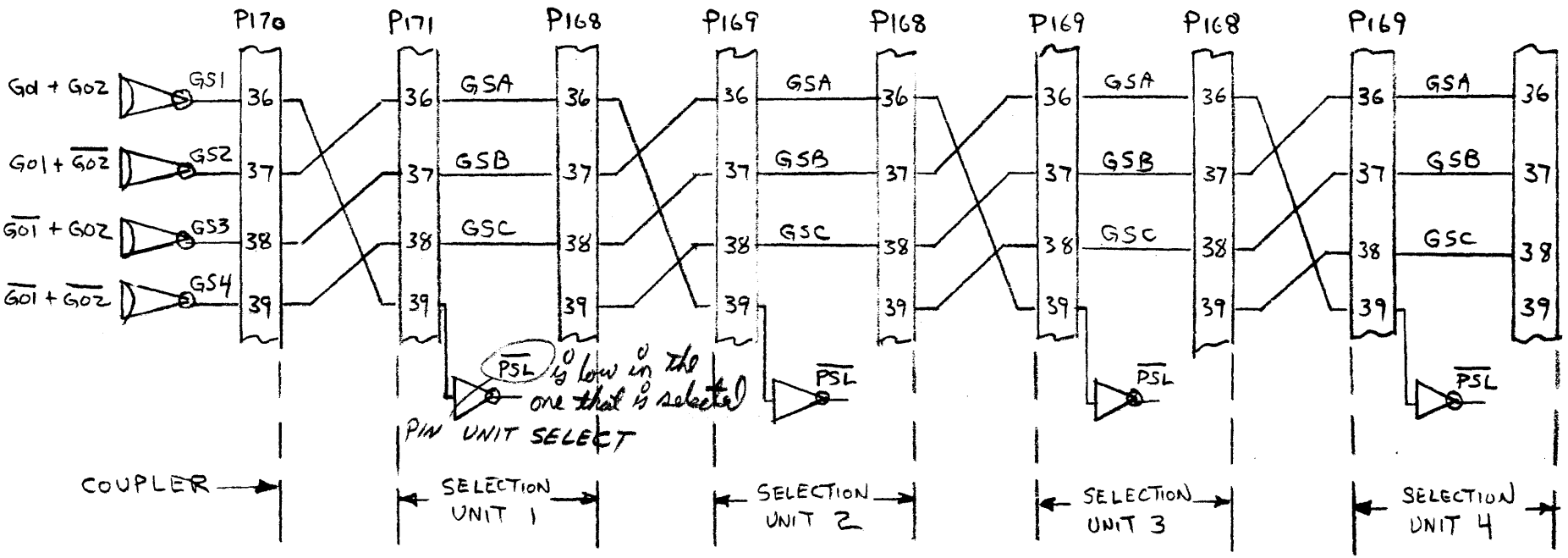


FIGURE 3-24 UNIT SELECTION FOR PIN OPERATION

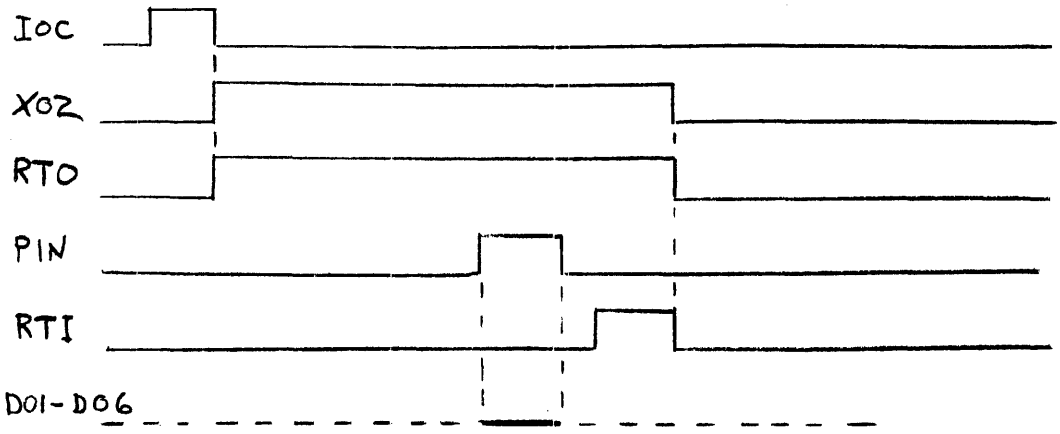


FIGURE 3-25 TIMING DIAGRAM, NORMAL PIN OPERATION

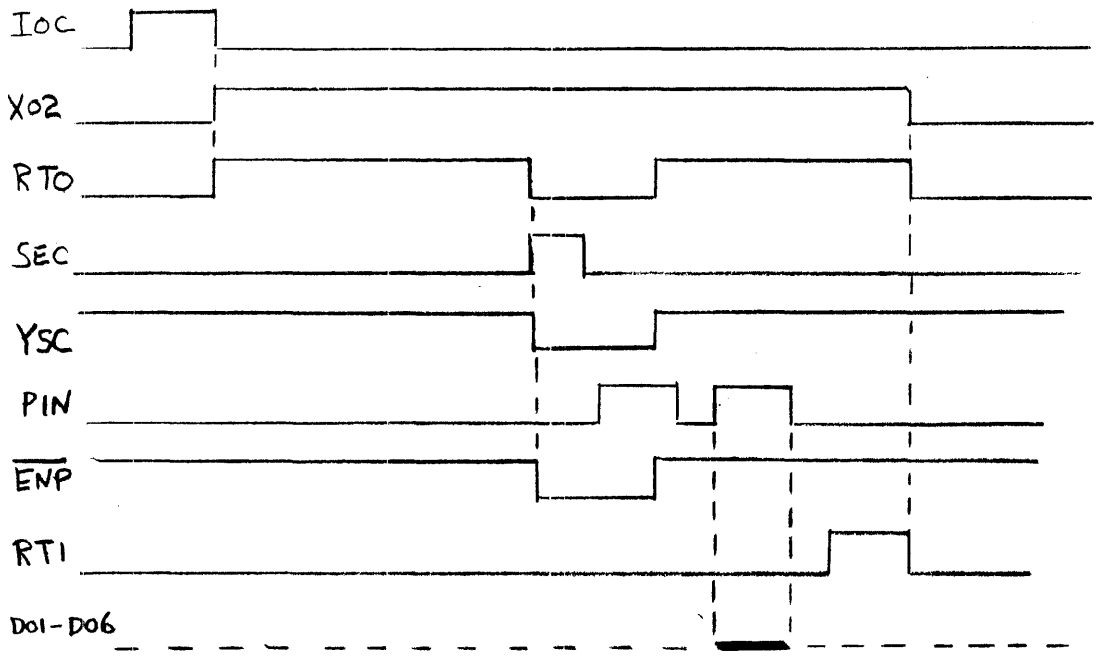


FIGURE 3-26 TIMING DIAGRAM, PIN OPERATION DURING SECTOR INCREMENT.

$$Cd18 = DO1\ \overline{DAP}$$

$$\vdots \qquad \vdots \qquad \vdots$$

$$Cd23 = DO6\ \overline{DAP}$$

$$\overline{DAP} = XO1 + XO2$$

Normal PIN Operation timing is shown in the timing diagram of Figure 3-25. Figure 3-26 timing diagram shows the timing when a PIN operation occurs as the D register is incrementing.

SKS INSTRUCTIONS

The SKS instructions do not affect the current operation of the coupler in any way; thus, and SKS instruction may be executed while the disc file is reading, writing, or while it is in the standby condition. Each of the SKS instructions tests the status of the $\overline{SIO}$ line for a true or false condition. The logic levels of the $\overline{SIO}$ term are inverted. If $\overline{SIO}$ is at ground level, the computer skips the next sequential instruction; if the $\overline{SIO}$ signal is at a positive level, the computer executes the next sequential instruction.

When $\overline{SIO}$ is not being tested it is positive. It can go to ground level only when it is being sensed and the condition being tested exists. The conditions tested and the corresponding control terms are:

Skip if Disc Ready	$00F\ \overline{X03} + \overline{00F}\ \overline{U01}\ \overline{U02}\ \overline{X03}$
Skip if No Disc Error	$\overline{E01}$
Skip if Track Not Protected	$\overline{WLK}$

SKS Operations

$$SIO = DMA\ \overline{C13}\ \overline{C14}\ PUF\ \overline{X03}\ PWR$$
$$+ DMA\ \overline{C13}\ C14\ \overline{E01}$$
$$+ DMA\ C13\ C14\ \overline{WLK}$$

where $PUF = 00F + \overline{00F}\ \overline{U01}\ \overline{U02}$

and WLK = (Band Protected by switch).USL

$$USL = US1 = \overline{A09}\ \overline{A10} \quad \text{Selection Unit 1}$$
$$+ IS2 = A09\ \overline{A10} \quad \text{Selection Unit 2}$$
$$+ U53 = \overline{A09}\ A10 \quad \text{Selection Unit 3}$$
$$+ US4 = A09\ A10 \quad \text{Selection Unit 4}$$

SECTION IV
INSTALLATION AND MAINTENANCE

SECTION IV INSTALLATION AND MAINTENANCE

The 9367 RAD is provided with a comprehensive diagnostic program (594003) that provides an extremely useful and versatile tool for testing and trouble-shooting the RAD system. However, to effectively use this tool, it is first necessary to determine that the RAD can perform the basic functions outlined below:

1. Respond properly to computer tests.
2. Accept an address correctly.
3. Communicate with a TMCC or DACC.

This section is intended to provide guidance in testing these functions. It should be remembered that total testing of the RAD requires the use of the RAD apocalyptic Diagnostic and that the procedures herein will test only basic operation.

The following instructions control the 9367 RAD operation and are configured for operation through the E channel of the DACC. Operation through channels other than E require instruction modification for channel selection.

SKS 50026 Skip if RAD ready

This SKS instruction shall cause the program to skip if the RAD error Flip-Flop is not set. The RAD Error Flip-Flop is set by the following conditions:

1. An attempt is made to POT new address and the controller is not ready.
2. An attempt is made to write in a write protected area.
3. The address register increments across a unit boundary.

SKS 53026 Skip if band not write protected.

This SKS instruction shall cause the program to skip if the currently addressed band is not located in a write protected area. A minimum of 0.6 milliseconds must elapse between the potting of a new RAD address and the write-protect SKS for the SKS response to be valid.

EOD 10026 Alert to POT

EOD 11026 Alert to POT, inhibit band incrementing.

Either instruction shall enable the controller to accept a potted addresss provided the instruction is performed when the controller is in the ready

state. The address is located in C09 to C23 of the potted word.

Unit	Band	Sector
C09, C10,	C11, C12, C13, C14, C15, C16, C17,	C18, C19, C20, C21, C22, C23

Should the alert to POT instruction be performed when the controller is not ready the subsequent POT shall not alter the address but will set the RAD Error Flip-Flop.

When the alert to POT, inhibit band incrementing is used to alert the coupler, band incrementing is inhibited during the subsequent write or read operations.

EOD 1N226 Alert to PIN

This instruction enables the controller to gate the contents of the sector counter located in unit "N" to the computer by a PIN instruction.

N	Unit
0 or 1	Ø
2 or 3	1
4 or 5	2
6 or 7	3

Contents of effective PIN address

Ø's	Sector
C0----------C17	C18----------C23

EOD 02266 Connect RAD memory write.

This instruction shall cause the RAD to connect to the channel and write a consecutive number of words as defined by the contents of the interlace registers. Operations involving less than a multiple of 64 words result in the unused portion of the last sector being filled with all zeros. An attempt to write on a write protected band shall cause the RAD to disconnect from the channel and shall set the RAD Error Flip-Flop.

EOD 02226 Connect RAD memory, Read.

This instruction shall cause the RAD to connect to the channel and read a consecutive number of words as defined by the contents of the interlace registers. Parity is tested at the end of each sector. A parity failure will result in the Channel Error indication.

The following test loops may be used to test basic RAD functions:

SKS 50026 Skip of RAD ready test.

This loop tests the RAD response to the Ready Test.

Insert Program

100	04050026	SKS test ready
101	00100100	BRU return, not ready
102	00100100	BRU return, ready

Step through the program. The program shall skip from 100 to 102.

Ground 37A03 in the coupler. The RAD shall now test busy and the program shall step through 100 and 101.

SKS 51026 Skip of no RAD error test.

This loop tests the RAD response to the Error test.

Insert program

100	04051026	SKS, test no error
101	00100100	BRU, return, error
102	00100100	BRU, return, no error

Step through the program. The program shall skip from 100 to 102.

Ground 31D23 in the controller. The RAD shall now test errors and the program shall step through 100 and 101.

SKS 53026 Skip if band not write protected test.

This loop tests the RAD response to the write protect test.

Insert program

100	04053026	SKS, test not write protected
101	00100100	BRU, return, write protected
102	00100100	BRU, return, not write protected

Push start. Check that the write protect switches are down. Step through the program. The program shall skip from 100 to 102.

Set the first write protect switch. The program shall now step through 100 and 101.

EOD 10026 Alert to POT test.

This loop tests the ability of the RAD to accept ones and zeros into its' address register.

Insert Program

```
100     00610026     EOD, alert to POT
101     01300105     POT, zeros
102     00610026     EOD, alert to POT
103     01300106     POT, ones
104     00100100     BRU, return
105     00000000     Constant, zeros
106     77777777     Constant, ones
```

Step through the program and observe the contents of the Address Register following each POT.

EOD 10226 Alert to PIN and PIN test.

This test verifies that the RAD releases the computer from the PIN operation and displays the result of the PIN in the A register. The validity of the PIN data is not tested.

Insert Program

```
100     00610226     EOD, alert to PIN
101     03300104     PIN, input sector address
102     07600104     LDA, display result
103     00100100     BRU, return
104                  PIN, data area
```

Display the A register. Step through the program. The data displayed in the A register shall vary between 00_8 and 77_8.

EOD 02266 and EOD 02226 Connect to Write or read test.

This program loop can be used to write or read from any location in the RAD units. The starting RAD address can be changed by altering the contents of location 130. Locations 131 and 132 respectively contain the write and read interlace values that may be modified to test multiple sector transfers. BP1 reset enables the write operation, BP1 set enables read.

Insert Program

100	04050026	SKS, test busy
101	00100100	BRU, return, busy
102	00610026	EOD, slert RAD for POT
103	01300130	POT, RAD address
104	04020400	BPT1, test breakpoint 1
105	00100113	BRU, branch to read
106	00650000	EOD, alert interlace
107	00614200	EOD, set conditions
110	01300131	POT, load interlace
111	00602266	EOD, connect to write
112	00100100	BRU, return to start
113	00650000	EOD, alert interlace
114	00614200	EOD, set conditions
115	01300132	POT, load interlace
116	00602226	EOD, connect to read
117	00100100	BRU, return to start
130	00000000	Constant, disc address
131	04001000	Constant, interlace data, write
132	04002000	Constant, interlace data, read
1000 - 1777		Data area, write
2000 -		Data area, read

Run this loop with various record lengths and patterns, first by loading the write area with a known pattern then writing in on the disc and calling it back. When the RAD can be operated without error, using this program, the RAD Apocalyptic Diagnostic should then be used to complete testing.

A

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P 168	FL 21	FL 21	HK 75	HK 76	HK 76	HK 75	AK 63	HK 76	HK 75	AK 63	HK 76	HK 75	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	SX 69	SX 60	OX 12	IL 12	IH 14	GH 14	BH 10	AX 14	AX 14	AX 14	FL 21	FL 21	P 171

B

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
NK 59	HK 73	HK 74	NK 59	HK 73	HK 74	NK 59	HK 73	HK 74	NK 59	HK 73	HK 74	AK 61	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 62	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	AK 63	HK 77	AK 64	AK 65

FIG 4-1 SELECTION UNIT MODULE COMPLEMENT

A

45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	LOCATION
FH 20	FH 20	FH 20	GK 51	FH 20	FH 20	FH 20	FH 20	BH 10	GK 51	GK 51	FH 20	FH 20	FH 20	FH 20	FH 20	AX 14	AX 14	AX 14	AX 14	MODULE

B

45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	LOCATION
BH 10	IH 14	GK 51	GK 51	GK 51	GK 51	GK 51	AH 10	AH 10	AH 10	BH 10	IH 14	IH 14	GK 51	GK 51	GK 51	BH 10	AX 14	AX 16	AX 16	MODULE

C

45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	LOCATION
FH 19	FH 19	OX 12	BH 10	BH 10	AH 10	IH 14	IH 14	FL 21	AH 10	FH 19	FH 19	FH 19	IH 14	IH 14	P 162	P 158	P 160	P 156	P 170	MODULE

D

45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	LOCATION
GK 51	GK 51	GK 51	FH 20	IH 10	BH 10	IH 10	BH 10	BH 10	GK 51	GK 51	GK 51	IH 14	BH 10	GK 51	GK 51	SK 60	SK 60	KX 12		MODULE

FIG 4-2 COUPLER MODULE COMPLEMENT

SECTION V

LOGIC EQUATIONS

GENERAL

This section contains a listing of all the logic equations that apply to the operation of the 9367C RAD coupler and selection units. This section is divided into the following three parts:

a) Logic Symbol Convention. A brief explanation of input gating structure, mechanization and terminology.

b) Logic Equations. Input equations for all register and control flip-flops, and output equations of unbuffered gates or gates buffered by logic amplifiers or inverters.

c) Glossary of terms.

LOGIC SYMBOL CONVENTION

A complete logic term is made up of three parts: a one-digit polarity or function identifier; a three-digit mnemonic; and a one-digit source tag. These three parts are described in the following paragraphs.

First Digit.

The first digit, when numeric, serves to identify the signal with its polarity and the type of connection it is making within the system. An odd number is assigned to a false or negated signal (true when at 0v). An even number is assigned to a true or assertive signal (true at +8v). The numbers "0" and "1" are reserved for flip-flop outputs only, "0" being reserved for the set and "1" being reserved for the reset side. The numbers "2" through "5" are used for buffer amplifier and inverter outputs; "4" and "5" being the second stage outputs, "6" and "7" for diode gate outputs, and "8" and "9" for cable signals.

A letter instead of a number is used when a signal is generated or gated for the sole purpose of connecting to one of the inputs shown in figure 5-1. The first digit is left blank for signals whose polarity is either undefinable or insignificant such as write driver outputs and ground jumpers.

Middle Three Digits

Three alphabetic characters from the basic mnemonic of the signal. Signals of external origin, such as those from the computer buffer, retain their

identity as much as possible with the addition of zeros when necessary to make up the three digits.

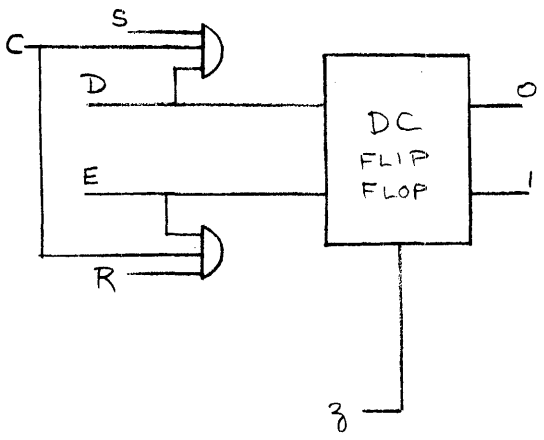
Last Digit

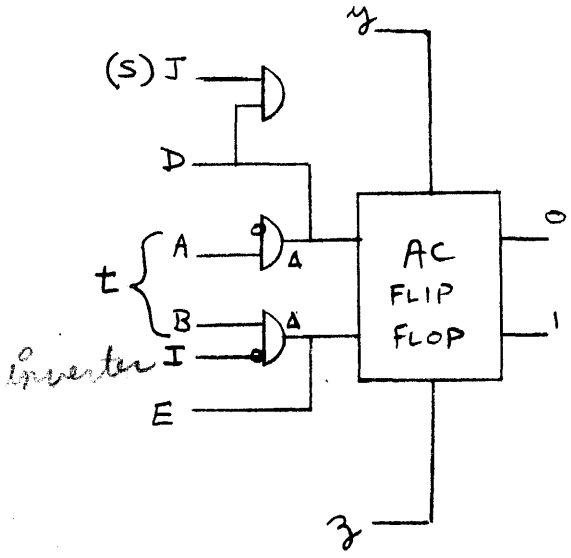
The last digit is a letter, or source tag, that defines the unit in which the signal is originally generated. The letters are assigned as follows:

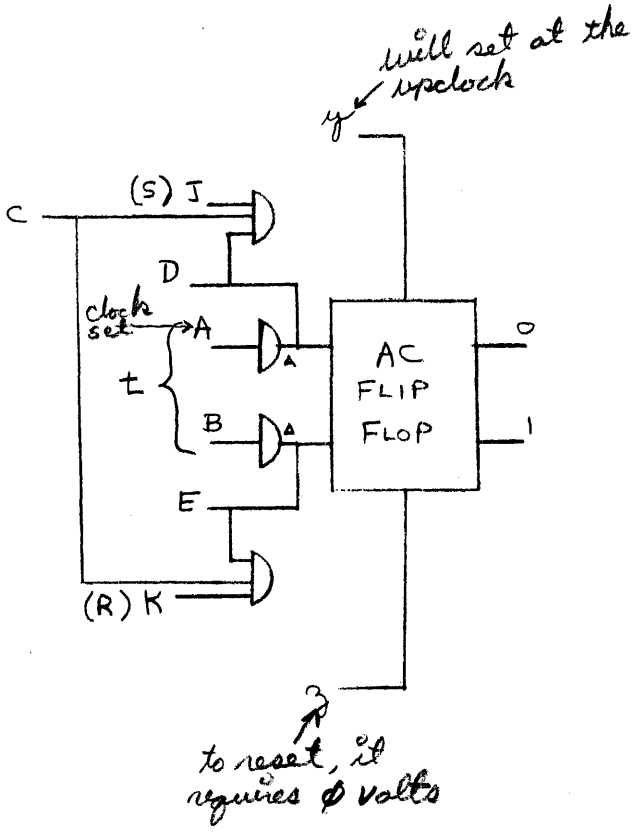
A	Coupler signals
C	Computer signals
S	Selection unit signals
W	Computer buffer signals

D → Delayed signal

The last digit is a numeric for a ground or jumper wire where the above convention is not used.







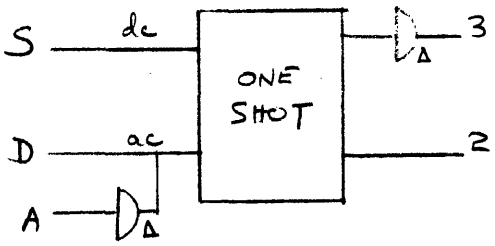


FIG. 5-1 CIRCUIT INPUT/OUTPUT CONVENTION

LOGIC EQUATIONS
9367 D
SELECTION UNIT

$$2SIPS = 2SECS$$
$$yREVS = OREVS$$
$$sREVS = \overline{2IDXS}$$
$$\sim REVS = \overline{2IDXS}$$
$$2IDXS = \overline{9IDXS}$$
$$2SECS = \overline{9SECS}$$
$$3RDYS = \overline{8RDYS}$$
$$2WENS = \overline{9WENA}\ \overline{9USLA}\ \overline{3RDYS}\ \overline{2WLKS}$$
$$8WENS = 2WENS$$
$$2CL1S = \overline{3CL1S}\ \overline{2USLA}$$
$$2CL2S = \overline{3CL2S}\ \overline{2USLA}$$
$$3CL1S = \overline{8CL1S}$$
$$3CL2S = \overline{8CL2S}$$
$$2USLA = \overline{9USLA}$$
$$2CLKS = 1MCCS\ 2CL1S$$
$$sMCC = \overline{2CL2S}$$
$$\sim MCC = \overline{2CL2S}$$
$$tMCC = 9SECS$$
$$2SFTS = 2WENS\ OMCCS \quad \text{(SHIFT)}$$
$$2LDWS = 2WENS\ 1MCCS \quad \text{(LOAD)}$$
$$\overline{3DRDS} = OREVS\ 2IDXS$$

$$3A11S = \overline{8A11A}\ \overline{9USLA}$$
$$3A12S = \overline{8A12A}\ \overline{9USLA}$$
$$3A13S = \overline{8A13A}\ \overline{9USLA}$$
$$3A14S = \overline{8A14A}\ \overline{9USLA}$$
$$3A15S = \overline{8A15A}\ \overline{9USLA}$$
$$3A16S = \overline{8A16A}\ \overline{9USLA}$$
$$3A17S = \overline{8A17A}\ \overline{9USLA}$$
$$3A18S = \overline{0D01S}\ \overline{9USLA}$$

$$\overline{4A11S} = \overline{3A11S}\ \overline{9USLA}$$
$$\overline{4A12S} = \overline{3A12S}\ \overline{9USLA}$$
$$\overline{4A13S} = \overline{3A13S}\ \overline{9USLA}$$
$$\overline{4A14S} = \overline{3A14S}\ \overline{9USLA}$$
$$\overline{4A15S} = \overline{3A15S}\ \overline{9US2A}$$
$$\overline{4A16S} = \overline{3A16S}\ \overline{9USLA}$$
$$\overline{4A17S} = \overline{3A17S}\ \overline{9USLA}$$
$$\overline{4A18S} = \overline{1D01S}\ \overline{9USLA}$$
$$\overline{5A11S} = \overline{8A11A}$$
$$\overline{5A12S} = \overline{8A12A}$$
$$\overline{5A13S} = \overline{8A13A}$$
$$\overline{5A14S} = \overline{8A14A}$$

TO WRITE PROTECT CIRCUITS

$$\overline{2DS1S} = 4A11S + 4A12S$$
$$\overline{2DS2S} = 4A11S + 5A12S$$
$$6WP1S = S01S\ 2GP1S + S02S\ 2GP2S + S03S\ 2GP3S + S04S\ 2GP4S + S05S\ 2GP1S + S06S\ 2GP2S + S07S\ 2GP3S + S08S\ 2GP4S$$
$$3WP1S = \overline{6WP1S}$$
$$\overline{2DS3S} = 5A11S + 4A12S$$
$$\overline{2DS4S} = 5A11S + 5A12S$$
$$6WP2S = S09S\ 2GP1S + S10S\ 2GP2S + S11S\ 2GP3S + S12S\ 2GP4S + S13S\ 2GP1S + S14S\ 2GP2S + S15S\ 2GP3S + S16S\ 2GP4S$$

```
3WP2S  = 6WP2S
2WLKS  = 3WP1S 3WP2S
2GP1S  = 4A14S + 4A13S
2GP2S  = 5A14S + 4A13S
2GP3S  = 4A14S + 5A13S
2GP4S  = 5A14S + 5A13S

SDO1   = ODO2S
~DO1   = ODO2S
±DO1   = 3DRDS
SDO2   = ODO3S
~DO2   = ODO3S
±DO2   = 3DRDS
SDO3   = ODO4S
~DO3   = ODO4S
±DO3   = 3DRDS
SDO4   = ODO5S
~DO4   = ODO5S
±DO4   = 3DRDS
SDO5   = ODO6S
~DO5   = ODO6S
±DO5   = 3DRDS
SDO6   = 2SECS
~DO6   = 2SECS
±DO6   = 3DRDS
9CD1S  = ODO1S 9USLA
9CD2S  = ODO2S 9USLA
9CD3S  = ODO3S 9USLA
9CD4S  = ODO4S 9USLA
9CD5S  = ODO5S 9USLA
9CD6S  = ODOGS 9USLA
9SIPS  = 2SIPS 9USLA
```

9D01S = 0D01S 3PSLS
9D02S = 0D02S 3PSLS
9D03S = 0D03S 3PSLS
9D04S = 0D04S 3PSLS
9D05S = 0D05S 3PSLS
9D06S = 0D06S 3PSLS
9ENPS = 2SIPS 3PSLS
3PSLS = $\overline{8PSLA}$

PIN SECTOR COUNTER

sTC1 = 2LDWS 2WD3S 2CL1S
+ 3WENS 2RL1S 2CL1S
$\sim$TC1 = 2LDWS 9WD3A 2CL1S
+ 3WENS 3RL1S 2CL1S
+ 2SFTS 2CL1S
sTC2 = 2LDWS 2WD1S 2CL1S
+ 3WENS 0TC1S 2CL1S
+ 2SFTS 0TC1S 2CL1S
$\sim$TC2 = 2LDWS 9WD1A 2CL1S
+ 3WENS 1TC1S 2CL1S
+ 2SFTS 1TC1S 2CL1S
sTC3 = 2LDWS 2WD4S 2CL1S
+ 3WENS 2RL2S 2CL1S
$\sim$TC3 = 2LDWS 9WD4A 2CL1S
+ 3WENS 3RL2S 2CL1S
+ 2SFTS 2CL1S
sTC4 = 2LDWS 2WD2S 2CL1S
+ 3WENS 0TC3S 2CL1S
+ 2SFTS 0TC3S 2CL1S
$\sim$TC4 = 2LDWS 9WD2A 2CL1S
+ 3WENS 1TC3S 2CL1S
+ 2SFTS 1TC3S 2CL1S

TRACK CONVERTER

sPC1 = 0PC2S
∩PC1 = 0PC2S
± PC1 = $\overline{9SECS}$
s PC2 = 0PC3S
∩ PC2 = 0PC3S
± PC2 = $\overline{9SECS}$
s PC3 = 1PC1S 2WD1S
∩ PC3 = 1PC1S 2WD1S
± PC3 = $\overline{9SECS}$

PREAMBLE CONVERTER

$\overline{2RL1S}$ = 3RL1S 3WENS
$\overline{3RL1S}$ = 8RL1S 3WENS
$\overline{2RL2S}$ = 3RL2S 3WENS
$\overline{3RL2S}$ = 8RL2S 3WENS
2WD1S = 9WD1A
2WD2S = 9WD2A
2WD3S = 9WD3A
2WD4S = 9WD4A
$\overline{8WL1S}$ = 1TC2S + 0PC1S
$\overline{8WL2S}$ = 1TC4S + 0PC1S
9RD1S = 0TC2S 9USLA
9RD2S = 0TC4S 9USLA
9RD3S = 0TC1S 9USLA
9RD4S = 0TC3S 9USLA
9CLKS = 2CLKS 9USLA
9WLKS = 2WLKS 9USLA

LOGIC EQUATIONS
9367B, C Selection Unit.

$9CDnS = \overline{ODOnS}$ (enable term on cable driver is 9USLA, low true logic)

$6CLKS = 9RCNA \cdot 2WCOS + 2RCNS \cdot 2RCKS$

$9CLKS = \overline{6CLKS}$ (enable term on cable driver is 9USLA, low true logic)

$tDO1S = 0D02S$
$tDO2S = 0D03S$
$tDO3S = 0D04S$
$tDO4S = 0D05S$
$tDO5S = 0D06S$
$tDO6S = 2SECS$

$3DO1S-DO6S = 3IDXS$ (low true logic)

$9ENPS = \overline{1YSCS}$

$9DOnS = \overline{ODOnS}$
n = 1 through 6

(enable term on cable driver is 3PSLS, low true logic)

$sRCKS = 2RCSS$
$rRCKS = 0.55\mu S$

$sRD1S = 0RDD1 \cdot RCS1$
$rRD1S = 1RDD1 \cdot RCS1$
$sRD2S = 0RDD2 \cdot RCS2$
$rRD2S = 1RDD2 \cdot RCS2$
$sRD3S = 0RDD3 \cdot RCS3$
$rRD3S = 1RDD3 \cdot RCS3$
$sRD4S = 0RDD4 \cdot RCS4$
$rRD4S = 1RDD4 \cdot RCS4$

$9RD1S = \overline{0D01S}$
$9RD2S = \overline{0D02S}$
$9RD3S = \overline{0D03S}$
$9RD4S = \overline{0D04S}$
$9SIPS = \overline{2SECS + 2IDXS}$

} cable driver enabled by 9USLA (low true logic)

$sWCKS = 2WCAS$
$rWCKS = 2WCAS$

dc reset = 3IDXS (low true logic)

$sWCBS = 1WCKS$
$rWCBS = 0.45MS$

$sWDE1 = 2WD1S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$rWDE1 = 9WD1S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$sWDE2 = 2WD2S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$rWDE2 = 9WD2S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$sWDE3 = 2WD3S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$rWDE3 = 9WD3S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$sWDE4 = 2WD4S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

$rWDE4 = 9WD4S \cdot 1WCKS \cdot 2WCAS + 0WCKS \cdot 2WCAS$

6WLKS = Or combination of the 4-uples of A11, A12, A13 and A14, each pulled over by the switch sw-n where

n	A comb
1	$= \overline{A11} \cdot \overline{A12} \cdot \overline{A13} \cdot \overline{A14}$
2	$= A11 \cdot \overline{A12} \cdot \overline{A13} \cdot \overline{A14}$
⋮	⋮
16	$= A11 \cdot A12 \cdot A13 \cdot A14$

$9WLKS = \overline{6WLKS}$ (cable driver enabled by 9USLA, low true logic)

94b

LOGIC EQUATIONS CONTROLLER

2ACTA = 200FA · 0406A · /X03A

2AFLA = 2AFAA · 2AFBA · 2AFCA

2AFAA = 0A12A · 0A13A

2AFBA = 0A14A · 0A15A · 0A16A · 0A17A

2AFCA = 0A19A · 0A20A · 0A21A · 0A22A · 0A23A · 0A18A · /X05A

2AINA = 201FA · 2014A · 2LSCA · 0K06A · 3AFLA · 2CLKA
+ 2RF1A · 2CLKA · 3AFLA

tA09A = 0A10A

yA09A = 2LDAA · 8C09C

tA10A = 0A11A

yA10A = 2LDAA · 8C10C

tA11A = 0A12A

yA11A = 2LDAA · 8C11C

tA12A = 0A13A

yA12A = 2LDAA · 8C12C

tA13A = 2AFBA · 2AFCA · 2AINA

yA13A = 2LDAA · 8C13C

tA14A = 0A15A

yA14A = 2LDAA · 8C14C

tA15A = 0A16A

yA15A = 2LDAA · 8C15C

tA16A = 0A17A

yA16A = 2LDAA · 8C16C

tA17A = 2AFCA · 2AINA

yA17A = 2LDAA · 8C17C

tA18A = 0A19A

yA18A = 2LDAA · 8C18C

tA19A = 0A20A

yA19A = 2LDAA · 8C19C

tA20A = 0A21A

yA20A = 2LDAA · 8C20C

tA21A = 0A22A
yA21A = 2LDAA·8C21C
tA22A = 0A23A
yA22A = 2LDAA·8C22C
tA23A = 2AINA
yA23A = 2LDAA 8C23C
sBSCA = 200FA·2HSDA·2SIPA
2CNTA = 201FA·3U01A·2CLKA
+202FA 3U01A·2CLKA
+2U02A 2CLKA
2DMAA = 9C17W·8C19W·3C20A·8C21W·8C22W·3C23A
2DMWA = 8W13W·3W14A·8W10W·3W11A 8W12W
6DRKA = 200FA 3U02A + 2U01A·3U02A·2CLKD
2DR/A = $\overline{1F02A}$(2W56A·1X06A·3CLKA + 1X03A)

6DRZA = 201FA·1X08A·0X09A·5CLKD
6ECWA = 201FA·0X08A·2X03A·3W50A·3W60A
+202FA 0U04A·3W50A·3W60A·2DMWA(1X06A+1U03A·1X09A)

2ERWA = 200FA 0K05A 2X03A

sE01A = 201FA·2WLKA 4CLKA
+200FA·2U03A·2SIPA·4CLKA address overflow error on R/W
yE01A = 0X01A 1X02A·8PT2C
rE01A = 200FA·2BUCA·2DMAA
sF01A = 2ERWA·2DMWA·3W90A·4CLKA
rF01A = 2RF1A·4CLKA
sF02A = 2ERWA 2DMWA 8W90W 4CLKA
rF02A = 201FA·2LSCA·3U02A 2K06A·4CLKA
+201FA·2WLKA 4CLKA

sG01A = 2IDNA · 2C12A

rG01A = 2IDNA 3C12A

sG02A = 2IDNA · 2C13A

rG02A = 2IDNA · 3C13A

7GS1A = 0G01A + 0G02A

7GS2A = 0G01A + 1G02A

7GS3A = 1G01A + 0G02A

7GS3A = 1G01A + 1G02A

2HSDA = 1U01A · 0X05A · 1E01A
+ 2U01A 1X01A + 0X03A · 1U03A

2IDNA = 2DMAA · 8C16W · 8IθCW

2IDTA = 2DMAA 3C16A · 8IθCW

8INTA = 200FA · 2SACA · 0BSCA · 2U01A · 1X03A · 1X01A

tK01A = 0K02A

K01A flip flop is pulled false by 7DRKA buffered and tied to 0K01A

tK02A = 0K03A

tK03A = 0K04A

tK04A = 0K05A · 2K06A · 2LSCA · 2CNTA

sK05A = 0K06A · JK57A

rK05A = 0K06A

sK06A = 0K07A

rK06A = 2K07A + 201FA · 0M01A · 2U01A

sK07A = 0M01A · JK57A

rK07A = 0M01A

JK57A = $\overline{201FA \cdot 2K06A \cdot 2U01A}$

2LDAA = 0X01A · 0X02A · [redacted] 2PTQA

2LDSA = 201FA · 202MA · 2CLKD

2LDVA = 201FA · 2X03A 0X06A · 2W60A · 2CLKA · 0STVA

2LDZA = 201FA · 0X07A · 2CLKA

2LRCA = 202FA · 200MA · 2CLKA

2LSCA = 0M01A · 2K07A

2LVRA = 202FA · 0X07A · 1X08A · 2CLKD
+ 202FA · 0X08A · 200MA · 3CLKA

sM01A = 0M02A · 2CNTA

rM01A = 2CNTA

sM02A = 1 M01A · 2CNTA

rM02A = 2CNTA

(last 2 words) 2NNLA = 0K01A · 0K02A · 0K03A · 0K04A | 0K05A

(last word) 2NXLA = $\overline{3NNLA + 1K06A}$

NUFA = $\overline{300FA \cdot 201UA}$

PUFA = $\overline{300FA \cdot NUFA}$

NUF = Ø0 + NOT POSTABLE
PUF = Ø0 + POSTAMBLE

2PSTA = $\overline{1U02A \cdot 2K06A}$

3PCPA = 3P01A · 2LR1A + 2 P01A · 9RD1S
+3P02A 2LR2A + 2 P02A · 9RD2S
+3P03A · 2LR3A + 2 P03A · 9RD3S
+3P04A · 2LR4A + 2 P04A · 9RD4S

8PWRA = $\overline{8STOC}$ + level from power protection cct which is true if ac voltages are within normal range

tP01A = 201FA · 4WD1A · 4CLKA
+2LR1A 2U02A · 4CLKA

yP01A = 2SPRA

tP02A = 201FA · 4WD2A · 4CLKA
+2LR2A · 2U02A · 4CLKA

yP02A = 2SPRA

tP03A = 201FA · 4WD3A · 4CLKA
+2LR3A · 2U02A · 4CLKA

yP03A = 2SPRA

tP04A = 201FA · 4WD4A · 4CLKA
+2LR4A · 2U02A · 4CLKA

yP04A = 2SPRA

2RF1A = 202FA · 3U01A · 3U02A · 202MA · 2K06A

PNCA = $\overline{300MA \cdot 2K06A}$

2PTQA = 8PT1C · 8Q20C

9RENA = $\overline{0U05A}$

9RCNA = $\overline{2021FA}$

6RTOA = 1X01A·0X02A·9ENPS
+0X01A·2PT1A

2SACA = 2CUHA · 2CLHA

2CUHA = 0A18A·9CD1S + 1A18A·2CD1A
+0A19A·9CD2S + 1A19A·2CD2A
+0A20A·9CD3S + 1A20A 2CD3A

2CLHA = 0A21A·9CD4S + 1A21A 2CD4A
+0A22A 9CD5S + 1A22A 2CD5A
+0A23A 9CD6S + 1A23A 2CD6A

2SHSA = 201FA·302MA·2CLKA
+202FA·2CLKA

6SI0A = 2DMAA·1X03A·3C14A·3C13A·PUFA
+2DMAA·3C14A·2C14A·1E01A
+2DMAA 2C13A·2C14A·9WLKS

2SPRA = 201FA·2U01A
+202FA 2U01A·3U02A

sSTVA = 5CLKD
rSTVA = 250 ns

sS01A = 2SHSA·0S02A·4CLKA
+2LDSA·0Z01A·4CLKA

rS01A = 2SHSA·1S02A·4CLKA
+2LDSA·1Z01A·4CLKA

sS02A = 0S03A·2SHSA

yS02A = 2LDSA·0Z02A

rS02A = 2SHSA (0S03A on inhibit reset)

sS03A = 2LR1A·2SHSA

yS03A = 0Z03A·2LDSA

rS03A = 2LR1A (2LR1A on inhibit reset)

sS04A = 0S05A·2SHSA·4CLKA
+0Z04A 2LDSA·4CLKA

rS04A = 1S05A·2SHSA·4CLKA
+1Z04A·2LDSA·4CLKA

sS05A = 0S06A·2SHSA

yS05A = 0Z05A·2LDSA

rS05A = 2SHSA (0S06A on inhibit reset)

sS06A = 2LR2A · 2SHSA

yS06A = 0Z06A · 2LDSA

rS06A = 2SHSA (2LR2A on reset inhibit)

sS07A = 0S08A · 2SHSA · 4CLKA
+ 0Z07A · 2LDSA · 4CLKA

rS07A = 1S08A · 2SHSA · 4CLKA
+ 1Z07A · 2LDSA · 4CLKA

sS08A = 0S09A 2SHSA

yS08A = 0Z08A 2LDSA

rS08A = 2SHSA (0S09A on reset inhibit)

sS09A = 2LR3A · 2SHSA

yS09A = 0Z09A · 2LDSA

rS09A = 2SHSA (2LR3 on reset inhibit)

sS10A = 0S11A · 2SHSA · 4CLKA
+ 0Z10A · 2LDSA · 4CLKA

rS10A = 1S11A · 2SHSA · 4CLKA
+ 1Z10A · 2LDSA · 4CLKA

sS11A = 0S12A · 2SHSA

yS11A = 0Z11A · 2LDSA

rS11A = 2SHSA (0S12A on reset inhibit)

sS12A = 2LR4A · 2SHSA

yS12A = 0Z12A · 2LDSA

rS12A = 2SHSA (2LR4A on reset inhibit)

9US1A = $\overline{1A09A \cdot 1A10A}$

9US2A = $\overline{1A09A \cdot 0A10A}$

9US3A = $\overline{0A09A \cdot 1A10A}$

9US4A = $\overline{0A09A \cdot 0A10A}$

sU01A = 2ERWA · 2CLKA

yU01A = 2LDAA

rU01A = 201FA · 2WPCA · 4CLKA
+ 201FA · 2WLKA · 4CLKA
+ 202FA 2U02A · 2U03A · 4CLKA

2TNIA = 1X03A · PUFA · 2IDTA

sU02A = 202FA · 2U01A · 1U03A · 200MA · 2CLKA
+202FA 2U01A · 2U03A · 1S03A · 9RDIS · 2CLKA
+201FA · 2U01A · 9WLKS · 2CLKA

yU02A = 200FA · 2SACA · 2HSDA · 0BSCA

rU02A = 200FA · 0K05A · 2CLKA
+201FA · 2NXLA · 2LSCA · 2CLKA
+202FA · 2NXLA · 2LSCA · 2CLKA
+202FA · 2U01A · 202MA · 0K07A · 2CLKA

sU03A = 201FA · 0U01A · PNCA · 4CLKA
+201FA · 3U02A · 2LSCA · 2AFLA · 4CLKA
+202FA 0U01A · 0U02A · 202MA 0K07A · 4CLKA
+202FA 1U01A · 1U02A · 0X07A 1X08A · 4CLKA

rU03A = 201FA · 0U01A · PNCA · 4CLKA
+200FA · 1X03A · 4CLKA
+2ERWA · 4CLKA
+202FA · 2U01A · 2U02A · 200MA · 4CLKA
+2RF1A · 3AFLA · 4CLKA

dc sU04A = 201FA · 2NNLA 2K07A 202MA · 2CLKD
+202FA · 3U01A · 200MA

dc rU04A = 200FA · 2ERWA
+2RF1A

dc sU05A = 200FA · 0U02A · 0K07A · 200MA

dc rU05A = 2ERWA · 2DMWA · 8W90W · 2CLKA
+2RF1A

dc sU06A = 2IDTA

dc rU06A = 2PTQA · 0X01A

9V0PA = 0P06A 2W60A · (Enabled by 302FA (low true logic))

9Vn A = 0Vn A · 2W60A · (Enabled by 302FA (low true logic))
n = 01 to 12

dc sVn A = 8RnW · 2LDVA
+0ZnA · 2LVRA

dc rVn A = 1ZnA · 2LVRA
n = 01 to 12

9WENA = $\overline{201FA}$

9WD1A = 201FA(2U01A · 2U03A + 201UA · 0P01A + 2234UA · 0S01A)

9WD2A = 201FA(2U01A · 2U03A + 201UA · 0P02A + 2234UA · 0S04A)

9WD3A = 201FA(2U01A · 2U03A + 201UA · 0P03A + 2234UA · 0S07A)

9WD4A = 201FA(2U01A · 2U03A + 201UA · 0P04A + 2234UA · 0S10A)

PARITY ERROR

6WESA = 202FA·3U01A·3U02A 200MA·1K06A·1K07A·3PCPA·2CLKD
+0X04A = RATE ERROR

6WHSA = 200FA·2DMWA(1XD3A·3BUCA WRITE PROTECT ADDRESS BOUNDARY ERROR
+2U03A·2SIFA)

7W56A = 2W50A + 3W60A

2WPCA = 2U01A·2K06A·202MA

sX01A = NUFA·0U06A·2PTQA

rX01A = NUFA·2PTIA

sX02A = 2IDNA

yX02A = 200FA·0X01A·1X03A

rX02A = 2RT1A + 2PT1A

sX03A = 200FA·2BUCA·2DMAA

rX03A = 200FA·0X04A·2CLKA
+201FA·2WLKA·2CLKA
+(2DMWA·9EDSW)·2CLKA·3U01A

sX04A = 202FA·2PSTA·1X09A·3U01A·200MA·2CLKD·[redacted]
+201FA·0X08A·0X09A·202MA·5CLKD·5U01A

rX04A = 00FA·2CLKA

sX05A = 2C14A·2TNIA

rX05A = 2TNIA (2C14A applied to reset inhibit)

sX06A = 201FA·2W56A·3CLKA + 201FA·3W50A·1X03A·3CLKA
+202FA·3U01A·1U04A·202MA·3CLKA
+202FA·2W56A·0U04A·3CLKA

rX06A = 2ERWA·2CLKA
+201FA·3CLKA
+202FA·5U01A·1U03A·3CLKA(1M01A+1X09A)

sX07A = 201FA·0X09A·1X08A·3CLKA
+202FA·2X06A·1M01A·3CLKA
+202FA·2X06A·1X09A·3CLKA

rX07A = 3CLKA

sX08A = 201FA·1U04A·0X09A·3CLKA
~~+[redacted]·8W90W·2DMWA·2CLKA~~
+202FA·2X06A·1X09A·202MA·2CLKA

rX08A = 201FA·0X06A·2CLKA
+202FA·202MA·3CLKA

yX08A = 2ERWA.

sX09A = 201FA · 2WPCA · 2CLKA
+201FA · 202MA · 3U01A · 2CLKA
+202FA · 0X07A · 3CLKA
+202FA · 0X08A · 3CLKA

4X09A = 2U01A · 3U02A

rX09A = 201FA · 0X07A · 2CLKA ($\overline{202MA \cdot 3U01A}$)
+202FA 3U01A · 200MA 2CLKA

9X12A = $\overline{DMWA}$

DC sZnA = 0VnA · 2LDZA
+0SnA · 2LRCA

DC rZnA = 1SnA · 2LRCA
n = 01 to 12

200FA = 1F01A 1F02A
200MA = 1M01A 1M02A
201FA = 1F01A 0F02A
201UA = 1U01A · 1U02A
202FA = 0F01A 1F02A
202MA = 0M01A
223UA = 1U01A · 0U02A

OUT OF SEQUENCE

3DRAA = 3ACTA · 8PWRA
2LR1A = $\overline{9RD1S}$
2LR2A = $\overline{9RD2S}$
2LR3A = $\overline{9RD3S}$
2LR4A = $\overline{9RD4S}$
6DAPA = 1X01A · 1X02A

$\overline{DAPA}$ enables cable drivers for 9D01A-9D06A

9367 C

RAD

Glossary of Logic Terms

A09-A23	Address Register
ACT	Clear the A register on Alert to POT
AFA	Address bits 12 and 13 both true
AFB	Address bits 14 through 17 all true
AFC	Address bits 18 through 23 all true
AFL	All bits true in A register (12 through 23) (Band 77 sector 77)
AIN	Increment the address in the A register

B

BSC	Beginning of sector pulse triggered by trailing edge of SIP
BUC	A signal from the computer that is true during an EOM buffer control mode instruction.

C

C09-C23	Computer C register terms.
CD1-CD6	Current sector address from the selected unit to be compared against the sector bits in the address register.
CLH	Lower half of sector address compare.
CLK	Basic clock. Derived from clock track in phase zero and one. In phase two it comes from the read data signal from disc.
CMC	Write enable signal inverted to center taps of read transformers.
CNT	A signal that allows the M and K registers to count.
CUH	Upper half of sector address compare

D

D01-D06	Current sector address register.
DAP	Enables D01-D06 cable drivers for PIN
DMA	RAD address contained in C register.
DMW	RAD address contained in Unit Address register.
DRA	Direct reset to A register.
DRK	Reset count registers M and K
DRV	Direct Reset V register
DRZ	Direct Reset Z register

E

E01	Error flip flop
ECW	Data character transfer clock to I/O channel.
EDSW	A signal from DACC when word count =4, used for an early EARLY DISCONNECT SIGNAL interrupt on a scatter read operation.
ENP	True while D register is incrementing at sector pulse time.
ERW	Enter read or write phase from phase zero.

F

F01-F02	Phase counter flip flops

G

G01-G02	Selection unit address register used for PIN operation.
GSI-4	Selection unit address gates. These four lines are used to select the addressed storage unit whose sector address is required for the PIN operation.

H

HSD — A conditional signal level required in phase zero to trigger the beginning of sector one shot, BSC, with the sector increment pulse, SIP.

I

IDL — Address increment period. This one shot is true during the time that the A register is incrementing.

IDN — An Alert to PIN command is in progress.

IDT — An alert to POT command is in progress.

IDX — Index pulse from disc, which is used to reset the sector counter each revolution.

INT — The interrupt signal generated when the sector address equals the current sector location.

IOC — A signal from the computer denoting that an EOM command in the Input/Output control mode is being executed.

J

JK57 — A signal that enables the resetting of the character counter at the end of the preamble.

K01-07 — Character counter register.

L

LDA — A signal to load the address register on a POT command.

LDS — A signal to load the S register with data from the Z register.

LDV — A signal to load the V register with data from the Rn lines from the I/O channel.

LDZ — A signal to load the Z register with data from the V register

LR1-4 Data lines from the controller cable receivers. These four bits of data from the selection unit are placed into the S register during phase two.

LRC A signal to load the Z register with data from the S register.

LSC A signal that denotes two 12 bit characters have been written or read. It is true every six pulse times.

LVR A signal to load the V register with data from the Z register.

M

M01-M02 Modulo 3 count register. Each full count of this register signifies that one 12 bit character has been written or read. Each full count of this register toggles the character (K) counter.

N

NNL A signal which denotes that the character (K) counter has a counted 125_{10} characters. (K01-K05 are all true)

NXL A signal that marks the last (64th) word time of a sector.

NUF Phase zero or not postamble time.

P

P01-P04 Parity checking and generating register for each of the four tracks.

PCP parity compare signal used in checking longitudinal parities of all four tracks at the end of a sector read.

PNC A signal derived from the character and modulo 3 counter which inhibits setting of U03 after the 8th preamble character is written, thus causing the last two preamble bits to be zeros.

PSL — A signal in each selection unit that enables the output of the sector counter during a PIN operation.

PST — Data time or first 6 clocks in postamble. Time for setting rate error flip flop X04 on read.

PT1 — The POT 1 signal from the computer.

PT2 — The POT 2 signal from the computer.

PTQ — The same as PT2 although it is made up in the coupler of POT1 and Q2 signals from the computer.

PUF — Postamble time or phase zero.

PWR — Power on signal. Normally true. It goes false when power fails or when the computer START button is pressed.

Q

Q20 — The Q2 signal from the computer.

R

RC01-4 — The 600 ns one shot output of the clock discriminators.

RCC1-4 — The unused clock compensator flip flop in each of the four read circuits.

RCD1-4 — The 600 ns one shot output of the clock discriminators after it has passed through a 200 ns delay.

RCK — The read clock pulse one shot. This generates the clock pulses used on in phase two.

RCL1-4 — The outputs from the read limiter cicuits which feed the clock dicriminators.

RCN — The signal that is true only during phase two which selects the read clock signal for CLK.

RCS1-4 — The read clock signal out of each of the four read circuits. The first of these to occur generates the coupler clock during Ø2.

RCS — The ORed output of the four track read clocks, RCS1-4

RD1-4 — The data output flip flops of each of the four read circuits.

RDA1-4 — The outputs of the read preamps.

RDD1-4 — The outputs of the read data differential amps which feed the inputs to the read data flip flops.

RDL1-4 — The outputs from the read limiter circuits which feed into the read data differential amps.

REN — Read enable signal to the selection unit which enables the portion of the X selection circuits that allows the read transformers to be used.

RF1 — A signal which is true only at the end of the read phase when the last character has been accepted by the channel.

RTO — The RT signal to the computer that gets a POT or PIN command out of the wait phase.

RTI — A signal from the computer indicating that a PIN command has ended.

S

S01-12 The 12 bit character assembler/disassembler register.

SAC Sector address compare gate which is true when the contents of the sector portion of the address register is equal the sector address (D) register.

SEC Sector timing pulse out of the Index Sector Decoder.

SHS The signal that causes the S register to shift.

SID The output of the Index Sector amplifier.

SIH The output of the Index Sector read head.

SIM A signal that is true during either the sector or index pulse time.

SIO The response signal to the computer during an SKS instruction. When this signal is true to computer skips the next instruction.

SIP Sector increment pulse. The pulse starts at the leading edge of SEC and lasts about 1.2 μs. This delays the start of BSC to allow the D register sufficiently settling time after incrmenting.

SPR Initialize the Parity flip flops at the beginning of the read or write phase.

STO The signal from the START button on the CPU

STV 250 [redacted] one shot which is a strobe pulse to load the V register with the LDV signal.

T

TNI — This signal is true only during the EOM alert to POT and it allows the setting of the non-increment mode flip flop X05 from C14.

U

U01 — This flip flop sets when the controller accepts a new address at the sector pulse time after an EOM, POT sequence, or when phase one or two is entered. Essentially it defines leading gap and preamble time, and search for starting sector.

U02 — This flip flow enables the character and module 3 counters to be clocked.

U03 — This flip flop generates the preamble pattern during write preamble time. During read preamble time it defines the search for end of preamble time. It also signifies end of data transfer time on a read operation. Another use is to detect an overflow condition.

U04 — This flip flop defines end of write time and also initiates read ECW's during phase two

U05 — Generates the read enable signal

U06 — Recognizes an EOM alert to POT command and remains set until a POT is executed.

US1-4 — Four unit select circuits in controller which sample each of the four configurations of A09 and A10.

USL — Unit select signal in selection unit.

V

V01-12 — V register (character buffer register).

W

W01-38	Write driver outputs
W9-W14	Signals from the I/O channel unit address register
W50	Signal from W5 flip flop in I/O channel
W60	Signal from W6 flip flop in I/O channel
W56	A signal true when W6 is set and W5 is reset (Data transfer time)
W90	Signal from W9 flip flop in I/O channel. True on outputs from CPU only
WCA	Output of clock read amplifier
WCK	A clock signal used in the selection unit during phase zero and one.
WCH	Outputs from the clock read head
WCO	Output of phase zero and one one shot which generates CLK.
WD1-4	The four write data lines from the controller to the selection unit.
WDE1-4	The four write data flip flops
WEN	Write enable signal to the X selection gates.
WES	The error line to set the I/O channel error flip flop.
WHS	The halt signal to the I/O channel.
WLK	An attempt was made to write in a protected disc area.
WPC	End of preamble signal

X

X01	Generates RT signal to computer on a POT command
X02	True if POT given at legitimate time or an alert to PIN command was executed.
X03	RAD connected indicator
X04	Rate error flip flop

X (Cont'd)

X05 Non-increment mode indicator. This inhibits the incrementing of the band address with the index pulse.

X06 The R lines from I/O channel are ready with data on a disc write operation or the character on the Z lines to I/O channel has been accepted by the channel on a disc read operation.

X07 Time to transfer V register to Z register on a disc write operation or time to transfer Z register to V register on a disc read operation.

X08 Allows a late Z to V transfer on read if the I/O channel was temporarily delayed in accepting a character.

X09 Z register empty indicator.

X12 12 bit Single Character Register selection line to I/O channel.

Y

YSC The inverse of this signal allows setting the band address in the controller to the band address register in the selection unit during sector increment pulse time.

Z

Z01-12 Character Storage Register (Z Register).

00F Phase zero signal

00M Module 3 counter flip flops both reset

01F Phase one signal

01U U01 and U02 flip flops both reset which is phase 0 or postamble time of phase one or two

02F	Phase two signal
02M	Flip flop M01 is set
223U	Flip flop U01 is reset and U02 is set which signifies data read or write time.

Appendix A

9367 B Differences

The Model 9367 B utilizes a drum memory rather than a disc. The 9367 B is available in three different capacities.

9367B-01	131,072 word capacity (524,288 alphanumeric characters)
9367B-02	262,144 word capacity (1,048,576 alphanumeric characters)
9367B-04	524,288 word capacity (2,097,152 alphanumeric characters)

Additional memory is available by adding from one to three extender units. These have the same capacities as above but are called:

9367B-11, 9367B-12 and 9367B-14

Mechanical Characteristics

A standard Bryant Auto-Lift drum consists of a drum and spindle assembly, a high-performance plated magnetic medium on the drum surface, an induction motor, a housing, dust-tight removable panels, and magnetic read/write Uni-Just data heads which can be adjusted radially.

The drum is 10 inches in diameter and vertically mounted and comes with a maximum of 512 data heads plus 6 pre-recorded timing tracks. It utilizes a 3 phase induction motor and rotates at approximately 1730 RPM There is actually room to mount 640 data heads.

Recording Media

Surfaces of standard Auto-Lift drums are coated with Bryant's super-finished magnetic plating. This plating has a tough, abrasive-resistant surface, and gives extremely uniform playback and resolution characteristics over large drum surfaces with a low noise level.

Magnetic Heads

Uni-Just aerodynamic data heads are used to optimize drum performance through a broad range of operating frequencies and recording densities. These heads can be adjusted for proper playback and the heads can be replaced, if required, without taking the unit out of operation.

Electrical and mechanical specifications are given in Table 1.

TABLE A-1 SPECIFICATIONS

Pole Piece Gap Length	0.00025 inch
Pole Piece Frequency Range	Up to 2 MC
Inductance-half-coil (at 140 KC)	17-22 microhenries
D-C Resistance	1 ohm
Drive Current	to fit application (Up to 250 ma)
Balance-half-coil to half-coil	10%
Resonant Frequency	3.8 megacycles (minimum)
Track Width	0.020 inch
Track-to-track Spacing	0.035 inch
Surface Speed Limits	1,000 to 3,500 inches per second

The drum heads are mounted on head bars around the outer surface of the drum. These head bars are mounted in a vertical position and each can hold 20 heads. There are 16 of these head bars mounted around the upper half of the drum and 16 more head bars around the lower portion of the drum. These bars are numbered from 1 to 32 starting in the back of the drum on the top row and coming around the left side to the right side. There are four upper and four lower head bars in each quadrant.

Each bar has the capacity of holding 20 heads but only 16 are mounted. Eight are at the top with a space for two under these; then eight more are mounted with two more spaces at the bottom of the head bar. The 6 pre-recorded timing tracks and their heads are located at the bottom position of head bars 26, 27, 28, 30, 31 and 32.

The clock and sector data is brought out on a separate cable than the data. The spare timing tracks are wired to separate connectors. Thus, changing from one set of timing tracks to another is accomplished by moving one cable plug to a different connector.

Auto-Lift Concept

Magnetic drum memory design dictates that a magnetic pickup be maintained at a relatively fixed distance from a recording media and in extremely close proximity to it under all conditions of system environment as dictated by the particular circumstances. These conditions include **shock**, vibration, thermal changes and extremesteady-state conditions, and different atmospheric densities and humidity levels. Bryant has successfully achieved this goal with the Auto-Lift Series of flying head drums.

The Auto-Lift Head-Drum Spacing Concept

Auto-Lift drums feature a simple, automatic head-drum spacing mechanism which **wworks** together with an adjustable flying head to assure reliable operation Wholly different in concept and design, these devices have been operationally integrated with the drum to assure the ultimate in fail-safe performance by completely eliminating the prime cause of drum failure - **inadvertent** head-to-drum contact.

Flying heads were devised to maximize temperature performance capability as well as to expand the data storage density of the drum The major temperature problem with drums is the rapid shrinking of the housing when the drum is turned off because then the heads are moved closer to or in contact with the drum surface. This condition results in head-to-drum contact if the drum is restarted before the drum shrinkage has caught up with the housing shrinkage and has restored the proper head-to-drum spacing.
Some types of flying heads used with conventional drums can "fly" only when drum speed is sufficient to produce a laminar film of air capable of supporting them. Therefore, the heads rub on the drum surface during stop/start cycles and remain in contact throughout down periods. Obviously, the tension of the heads against the surface and the resultant friction varies with temperature. The former condition leads to wear and eventual failure of the drum coating and/or the head polepieces; the latter provides an opportunity for the heads to freeze to the drum surface under operating conditions where frost might be produced - a condition that almost always leads to motor failures and coating damage.

The Auto-Lift drum-head spacing mechanism overcomes these disadvantages by bringing the recording surface into close proximity of the heads only when the drum has reached a speed high enough to provide an adequate laminar air film (or "air bearing" support).

An essential design feature of the Auto-Lift drum is its tapered recording surface design, a proprietary Bryant structural arrangement which has long permitted technicians to adjust fixed heads by manually positioning the drum rather than the heads. In the case of Auto-Lift Drums, however, flying heads are used and the drum is automatically moved up and down by the self-regulating drum-head spacing mechanism which is contained entirely within the drum itself.

Operation of the Auto-Lift Mechanism

The mechanism for moving the drum axially comprises a pair of simple scissor links which are straightened out by centrifugal force as the drum accelerates to approximately 75% of its operating speed. Straightening of the links raises the drum against a precision stop which defines its operating position. Thus, repeatability of the track location is exact. Spring tension is used to collapse the links and lower the drum as it slows down to approximately 65% of operating speed.

In the static, or down position, the drum surface is 0.010 inch or more from the heads. By the time the drum rises to the up position, the heads have gone into a flying attitude approximately 0.0002 inch from the surface.

Logic Differences

The 9367B uses the same coupler and selection unit as the 9367C. The only difference in logic would occur on the largest capacity drum, 9367-04. This drum thus contains 512 heads which utilize 128 bands. (Addresses 00-177) therefore the head selection matrix must be larger. This is accomplished by the addition of 16 more Y selection circuits.

See page 43 for the equations for the first 16 Y selection circuits. The additional logic required is given on the following page.

$$Y17 = A11\ \overline{A12}\ \overline{A13}\ \overline{A14}\ \overline{A15}$$

$$Y18 = A11\ \overline{A12}\ \overline{A13}\ \overline{A14}\ A15$$

$$\vdots$$

$$Y32 = A11\ A12\ A13\ A14\ A15$$

The following table may be used for finding the X and Y selection circuits utilized for any given band address in the RAD Model 9367B.

X SELECT	Channel #1	X01 X02	X21 X22	X11 X12	X31 X32	
	Channel #2	X03 X04	X23 X24	X13 X14	X33 X34	
	Channel #3	X05 X06	X25 X26	X15 X16	X35 X36	
	Channel #4	X07 X08	X27 X28	X17 X18	X37 X38	
Y SELECT	Y01	0	1	2	3	BAND SELECTED
	Y02	4	5	6	7	
	Y03	10	11	12	13	
	Y04	14	15	16	17	
	Y05	20	21	22	23	
	Y06	24	25	26	27	
	Y07	30	31	32	33	
	Y08	34	35	36	37	
	Y09	40	41	42	43	
	Y10	44	45	46	47	
	Y11	50	51	52	53	
	Y12	54	55	56	57	
	Y13	60	61	62	63	
	Y14	64	65	66	67	
	Y15	70	71	72	73	
	Y16	74	75	76	77	
X SELECT	Channel #1	X41 X42	X61 X62	X51 X52	X71 X72	
	Channel #2	X43 X44	X63 X64	X53 X54	X73 X74	
	Channel #3	X45 X46	X65 X66	X55 X56	X75 X76	
	Channel #4	X47 X48	X67 X68	X57 X58	X77 X78	
Y SELECT	Y17	100	101	102	103	BAND SELECTED
	Y18	104	105	106	107	
	Y19	110	111	112	113	
	Y20	114	115	116	117	
	Y21	120	121	122	123	
	Y22	124	125	126	127	
	Y23	130	131	132	133	
	Y24	134	135	136	137	
	Y25	140	141	142	143	
	Y26	144	145	146	147	
	Y27	150	151	152	153	
	Y28	154	155	156	157	
	Y29	160	161	162	163	
	Y30	164	165	166	167	
	Y31	170	171	172	173	
	Y32	174	175	176	177	

Table A-2
X & Y Driver Selection Chart
For Bryant Drum (9367B)